Study, optimization and silicon implementation of a smart high-voltage conditioning circuit for electrostatic vibration energy harvesting system

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THÈSE DE DOCTORAT DE L'UNIVERSITÉ PIERRE ET MARIE CURIE

Spécialité: Informatique, Télécommunication et Électronique

École Doctorale Informatique, Télécommunication et Électronique

Présentée par:

Andrii Dudka

Pour obtenir le grade de

Docteur de l'Université Pierre et Marie Curie

Étude, optimisation et implémentation en silicium du circuit de conditionnement intelligent haute-tension pour le système de récupération électrostatique d'énergie vibratoire

Soutenue le 18/02/2014

devant le jury composé de:

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Ph.D. THESIS OF THE PIERRE AND MARIE CURIE UNIVERSITY

Departament: Electronics, Telecommunications and Computer Science

Presented by:

Andrii Dudka

Submitted to obtain the Ph.D. degree from:

University of Pierre and Marie Curie

Study, optimization and silicon implementation of a smart high-voltage conditioning circuit for electrostatic vibration energy harvesting system

Defense date: 18/02/2014

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Abstract

Vibration energy harvesting is a relatively new concept that can be used in powering micro-scale power embedded devices with the energy of vibrations omnipresent in the surrounding. This thesis contributes to a general study of vibration energy harvesters (VEHs) employing electrostatic transducers. A typical electrostatic VEH consists of a capacitive transducer, conditioning electronics and a storage element. This work is focused on investigations of the reported by MIT in 2006 auto-synchronous conditioning circuit, which combines the diode-based charge pump and the inductive flyback energy return driven by the switch. This architecture is very promising since it eliminates precise gate control of transistors employed in synchronous architectures, while a unique switch turns on rarely.

This thesis addresses the theoretical analysis of the conditioning circuit. We developed an algorithm that by proper switching of the flyback allows the optimal energy conversion strategy taking into account the losses associated with the switching. By adding the calibration function, the system became adaptive to the fluctuations in the environment. This study was validated by the behavioral modeling.

Another contribution consists in realization of the proposed algorithm on the circuit level. The major design difficulties were related to the high-voltage requirement and the low-power design priority. We designed a high-voltage analog controller of the switch using AMS035HV technology. Its power consumption varies between several hundreds nanowatts and a few microwatts, depending on numerous factors - parameters of external vibrations, voltage levels of the charge pump, frequency of the flyback switching, frequency of calibration function, etc.

We also implemented on silicon, fabricated and tested a high-voltage switch with a novel low power level-shifting driver. By mounting on discrete components the charge pump and flyback circuit and employing the proposed switch, we characterized the wideband high-voltage operation of the MEMS transducer prototype fabricated alongside this thesis in ESIEE Paris. When excited with stochastic vibrations having an acceleration level of 0.8 g rms distributed in the band 110-170 Hz, up to 0.75 μW of net electrical power has been harvested.

Key words

Vibration energy harvesting, optimization, adaptive algorithm, power management, modeling, integrated circuit, high-voltage, controller, switch, MEMS transducer.

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Abbreviations

E-VEH	**E**lectrostatic **V**ibration **E**nergy **H**arvester
RF	**R**adio **F**requency
WSN	**W**ireless **S**ensor **N**ode
MEMS	**M**icroelectromechanical **S**ystem
PZT	Lead zirconate titanate (piezoelectric material)
ICP	**I**ntegrated **C**ircuit **P**iezoelectric
DRIE	**D**eep **R**eactive-**I**on **E**tching
OPGP	**O**ut-of-**P**lane **G**ap-closing **P**late
IPOP	**I**n-**P**lane **O**verlap **P**lates
IPOC	**I**n-**P**lane **O**verlap **C**omb
IPGC	**I**n-**P**lane **G**ap-closing **C**omb
SESAM	**S**mart multi-source **E**nergy **S**cavenger for **A**utonomous **M**icrosystems
CC	**C**onditioning **C**ircuit
EM	**E**lectro-**M**agnetic
SAR ADC	**S**uccessive **A**pproximation **R**egister **A**nalog-to-**D**igital **C**onverter
AMS	**A**ustria **M**icrosystems and **A**nalog **M**ixed **S**ignals
MP	**M**icroprocessor
CAD	**C**omputer-**A**ided **D**esign
ASIC	**A**pplication-**S**pecific **I**ntegrated **C**ircuit
ESD	**E**lectrostatic-**D**ischarge
LS	**L**evel-**S**hifter
DCC	**D**ynamic **C**harge **C**ontrol
PTAT	**P**roportional-**T**o-**A**bsolute **T**emperature
SBCS	**S**elf-**B**iased **C**urrent **S**ource
SCM	**S**elf-**C**ascode **M**OSFET
ACM	**A**dvanced-**C**ompact **M**OSFET
MIM	**M**etal-**I**nsulator-**M**etal
PIP	**P**oly-**I**nsulator-**P**oly
JLCC	**J**-**L**eaded **C**hip **C**arrier
ESR	**E**quivalent **S**eries **R**esistance
RMS	**R**oot **M**ean **S**quare

Symbols

Symbol	Name	Unit
I	current	A
V	voltage	V
W	energy	J
t	time	s
P	power	W
A_{ext}	acceleration of external vibrations	ms^{-1}
X_{lim}	displacement limit	m
A	overlap area of the plates	m^2
d	gap distance between the plates	m
Q	electrical charge	C
C	capacitance	F
L	inductance	H
R	resistance	Ω
f	frequency	Hz
T	period	s
m	mass	g
k	stiffness	Nm^{-1}
T_{abs}	absolute temperature	K
ω	angular frequency	$rads^{-1}$
ε_0	dielectric constant	
τ	time constant	s
η	efficiency	
μ	damping coefficient	Nsm^{-1}
ϕ	thermal voltage	V
κ_B	the Boltzmann constant	JK^{-1}
μ_e	electron mobility	$m^2(Vs)^{-1}$

Résumé en français

Cette thèse résume nos travaux de recherche sur la récupération d'énergie vibratoire (REV) pour l'alimentation des systèmes embarqués/implanté autonomes ultra-basse consommation. Ces travaux ont été possible grâce à un projet de recherche ANR SESAM[1], dont l'objectif était le développement d'un microsystème de récupération et de management de l'énergie ambiante (vibratoire, solaire et thermique), adaptable, reconfigurable et robuste. Le projet regroupe 4 partenaires (responsabilités): le LIP6 (partie électronique pour le REV capacitive), l'ESIEE (convertisseur REV capacitive), le TIMA (convertisseur REV piézoélectrique) et le CEA-LETI (partie management de l'énergie convertie et les convertisseurs solaires et thermique). Notre recherche sur la partie électronique du REV à base d'un convertisseur capacitive se porte sur l'étude théorique, la modélisation et la conception d'un circuit intelligent adaptative et autonome.

Le manuscrit présente des généralités sur les systèmes de récupération d'énergie vibratoire en résumant nos contributions, expose le problème de conditionnement des transducteurs capacitifs, présente le travail de conception et de modélisation des circuits de conditionnement intégrés et, finalement, expose la partie expérimentale des prototypes fabriqués (une puce électronique à LIP6 et un dispositif MEMS à l'ESIEE Paris).

Introduction: système de récupération d'énergie vibratoire

Fig. 1 présente un schéma général d'un système de récupération d'énergie vibratoire. Deux éléments font toujours partie d'un récupérateur d'énergie vibratoire (REV) : une masse mobile (masse sismique) dont le rôle est d'emmagasiner une partie d'énergie de l'environnement et un transducteur électromécanique réalisant une interface physique entre le domaine mécanique et le domaine électrique. La masse mobile est couplée par un ressort avec le système extérieur vibrant. La conception d'un REV consiste à optimiser la partie mécanique et la partie liée au transducteur de sorte à ce que l'ensemble convertisse le plus d'énergie possible.

Transduction électromécanique et son conditionnement

Le rôle du transducteur est la conversion d'énergie du domaine mécanique vers le domaine électrique. Pour cela, le transducteur génère sur la masse mobile une force

[1]Smart multi-source Energy Scavenger for Autonomous Microsystems

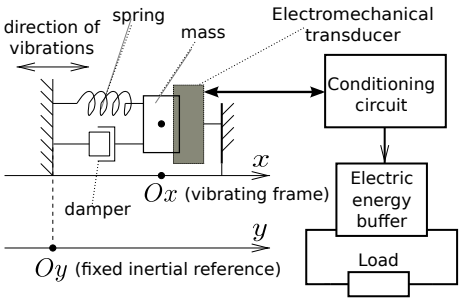


FIGURE 1: Architecture générale d'un récupérateur d'énergie vibratoire [Galayko11a].

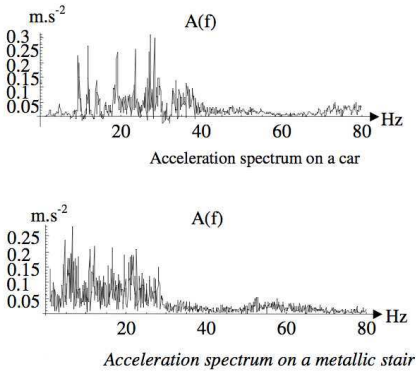


FIGURE 2: Spectre typique des vibrations ambiantes [Despesse05].

mécanique qui amortit le mouvement, de sorte à réduire son énergie cinétique moyenne. De part la physique du transducteur, l'énergie retirée de la masse se retrouve dans le domaine électrique. Il existe trois types de transducteurs électromécaniques: capacitif (électrostatique), électromagnétique et piézoélectrique [Beeby06, Mitcheson08].

La conversion d'énergie mécanique par voie électromagnétique et piézoélectrique est bien étudiée et est utilisée depuis un certain temps, notamment [Shenck01, Glynne-Jones01, Ottman02, Roundy04b]. Les défis principaux de ces dispositifs sont liés à la technologie et la miniaturisation.

La transduction capacitive a pu se généraliser grâce à l'avènement des technologies MEMS permettant une fabrication d'une capacité à électrode mobile de taille micrométrique [Lee82] : cette technique est donc relativement jeune (15-20 années de maturité). Utilisée d'abord pour la mesure, l'actionnement mécanique et le traitement du signal, elle s'est avérée la première candidate pour une conversion d'énergie mécanique à micro-échelle [Meninger01]. Parmi les trois mécanismes de conversion électromécanique, la conversion capacitive se prête au mieux à une réalisation en technologie MEMS silicium: il s'agit de fabriquer deux pièces de conducteur dont une est mobile. Au contraire, la transduction piézoélectrique nécessite un dépôt de matériau pas toujours compatible avec l'environnement de fabrication de circuits silicium [Marzencki05]. Quant à la transduction électromagnétique, celle-ci se prête mal à la miniaturisation en règle générale [Arnold07].

La simplicité structurelle et la facilité de fabrication d'un transducteur capacitif sont contrebalancées par la complexité du conditionnement électrique requis pour la conversion d'énergie. En 2006 il s'est avéré que les problèmes liés au conditionnement étaient complexes et qu'il y existaient de nombreuses lacunes conceptuelles et théoriques. En particulier, plusieurs circuits électriques permettant ce conditionnement ont été proposés à l'époque ; cependant, les questions concernant leur optimisation, comportement dynamique, les phénomènes non linéaires associés et leur modélisation étaient ouvertes. De nombreuses études s'arrêtaient au niveau de preuve de concept "laboratoire", sans apporter une réflexion sur les aspects tels que la réalisation de l'électronique de commande, de l'interface avec la charge ou d'une adaptation aux variations des conditions de l'environnement.

Partie mécanique

La partie mécanique du REV inclut une masse sismique et un mécanisme permettant un couplage de la masse avec le cadre vibrant (avec les vibrations externes). Le plus souvent, ce mécanisme est réalisé avec un ressort. Jusqu'à présent, la plupart des REVs utilisent un ressort linéaire ou avec une faible non-linéarité non voulue: ainsi, le système masse–ressort forme un résonateur du second ordre, le plus souvent sélectif, à facteurs de qualité supérieurs à 10. L'inconvénient de tels systèmes est leur sélectivité fréquentielle: la bande des fréquences de fonctionnement est étroite, ce qui est contraire aux caractéristiques réelles des vibrations ambiantes (Fig. 1.3, [Roundy03b, Despesse05]). Ainsi, depuis peu, les chercheurs s'orientent vers des mécanismes de couplage plus complexes permettant d'ouvrir la bande passante: utilisation de ressorts non linéaires [Blystad10], bistables [Cottone09], utilisation des systèmes non linéaires à double masse permettant une conversion de fréquence [Galchev12], exploitation de résonance stochastique, etc.

Une relation fondamentale caractérise la puissance P_{max} qu'il est possible d'extraire des vibrations ambiantes à amplitude d'accélération et à fréquence données A_{ext} et ω, en utilisant un REV avec la masse m qui peut se déplacer avec amplitude maximale de X_{lim} (c'est une limitation imposée par les gabarits du système):

$$P_{max} = \frac{1}{2} m A_{ext} \omega X_{lim}. \tag{1}$$

Cette formule donne une limite absolue de puissance convertible quel que soit le mécanisme de transduction électromécanique [Mitcheson08, Basset09]. Elle permet d'estimer la puissance maximale qu'il est possible de convertir avec un dispositif de dimensions de 1 cm^3 (un gabarit "cible" des capteurs autonomes [Roundy04b]): pour $m = 100 \cdot 10^{-6}$ kg, $X_{lim} = 250$ μm, $\omega = 2\pi \cdot 50$ ms^{-1}, $A_{ext} = 10$ ms^{-2}, nous avons 37 μW pour P_{max}.

La conception et la fabrication de la partie mécanique des REVs est un thème de recherche à part, qui n'est pas notre sujet de préoccupation. Cependant, une interaction étroite est nécessaire entre les concepteurs des différentes parties d'un REV. Notamment, la modélisation comportementale au niveau du système nécessite une prise en compte de la partie mécanique. La conception de la partie électrique et l'optimisation du rendement énergétique nécessite également une connaissance de la partie mécanique. Pour cette raison, nous avons travaillé en étroite coopération avec l'équipe de Philippe Basset du laboratoire ESYCOM (l'ESIEE Paris).

Jusqu'à présent, nous nous sommes focalisés sur les REVs résonants: par défaut, ce type de REV est sous-entendu dans ce manuscrit, sauf indication contraire. Depuis deux ans, l'équipe de Philippe Basset s'intéresse aux structures mécaniques résonantes non linéaires permettant d'élargir la bande de fréquences de fonctionnement et permettant de capter des vibrations de type bruit. Cela pose des défis nouveaux pour le circuit de conditionnement et pour les méthodes d'analyse; il s'agit d'un axe de recherche en cours d'exploration.

Résumé de notre contribution

Notre contribution au thème de la récupération d'énergie est structurée autours des points suivants:

– **Étude globale du système de REV: analyse et optimisation**. Un REV est un système fonctionnant dans deux domaines physiques fortement couplés. Son optimisation nécessite une approche globale, prenant en compte à la fois la partie mécanique, la transduction et la partie électrique. La plupart des études précédentes sont focalisées sur un de ces aspects. Dans nos publications, nous avons défendu la vision selon laquelle un transducteur électromécanique doit être considéré en un bloc uni avec son circuit de conditionnement; l'étude d'un REV se réduit alors à analyser l'interaction entre ce bloc et le résonateur mécanique.

– **Techniques de modélisation multiphysique à différents niveaux de raffinement**. L'objectif d'une démarche de modélisation est de pouvoir étudier le comportement d'un système dont les phénomènes sont trop complexes pour être décrits analytiquement. La modélisation est également un précieux outil de conception. Elle permet une approche de conception "top-down". Selon cette approche, la conception se fait d'abord au niveaux de blocs représentés par leurs macromodèles comportementaux. Ensuite, chaque bloc est détaillé au fur et à mesure. Une modélisation à différents niveaux de raffinement permet de mélanger les niveaux d'abstraction dans une même simulation : un bloc représenté par un modèle structurel très précis (par ex., une netlist SPICE extrait d'un dessin de masques d'un circuit intégré) et des blocs représentés par des modèles de haut niveau d'abstraction (par ex., un modèle VHDL-AMS d'un résonateur).

– **Circuits de conditionnement intégrés: analyse et conception** La conception de l'électronique de conditionnement pour transducteurs capacitifs représente le plus grand défi parmi ceux posés par les REVs. Comme il sera présenté, un circuit de conditionnement doit ordonner des interrupteurs selon un protocole précis permettant une conversion d'énergie en mode optimal. La situation est compliquée par deux contraintes qui s'opposent. Une haute tension est nécessaire pour le fonctionnement des transducteurs capacitifs, en même temps, le circuit doit être ultra basse consommation (des microwatts). Nous avons étudié plusieurs circuits de conditionnement, et par la suite nous avons proposé une nouvelle architecture basée sur une pompe de charge, qui s'adapte aux conditions réelles de l'environnement. Ce circuit est conçu dans une technologie de circuits intégrés CMOS haute tension et représente une contribution significative au domaine des circuits intégrés de puissance.

REV capacitifs: présentation globale et problèmes associés

Description d'un REV capacitif

Un schéma général de REV capacitif est identique à celui présenté Fig. 1, avec, à la place du transducteur générique, un condensateur à une électrode mobile (Fig. 3a). La masse mobile du résonateur est associée à l'électrode mobile du transducteur capacitif, ce qui fait que la capacité du transducteur varie avec le mouvement de la masse. En même

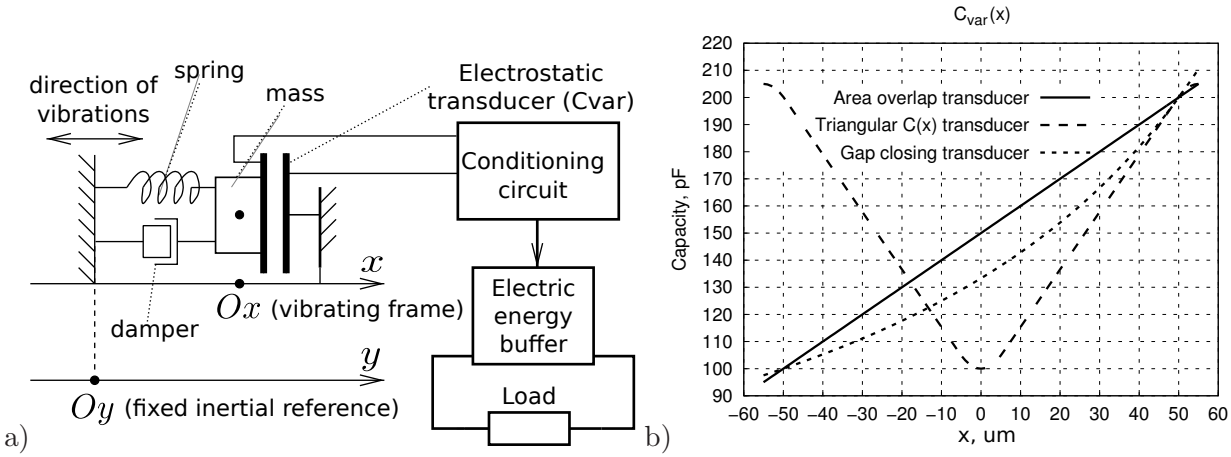


FIGURE 3: REV capacitif: a) architecture typique, b) trois exemples de caractéristiques $C_{var}(x)$.

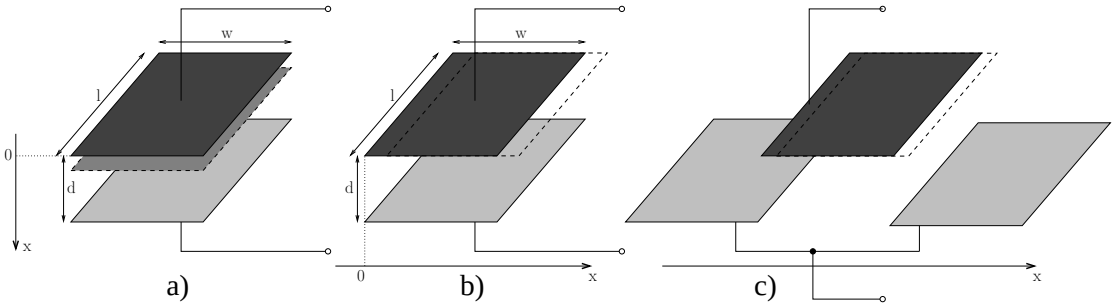


FIGURE 4: Géométries des transducteurs capacitifs: a) transducteur à rapprochement des plans (*gap closing*), b) transducteur linéaire à mouvement dans le plan (*in-plane area overlap*), c) transducteur à mouvement dans le plan ayant une caractéristique $C_{var}(x)$ de type dent de scie.

temps, le transducteur génère entre ses électrodes une force mécanique qui s'applique à la masse. Cette force dépend de la tension (charge) aux bornes de la capacité du transducteur. De cette manière, un transducteur électrostatique assure un couplage bidirectionnel entre les domaines mécanique et électrique.

Un transducteur capacitif est caractérisé par la relation entre la position de l'électrode mobile x et la valeur de sa capacité, $C_{var}(x)$. Cette fonction dépend de la géométrie du transducteur: le plus souvent c'est une capacité plane dont une des électrodes se déplace parallèlement ou dans le sens normal par rapport aux plans. Fig. 3b présente trois caractéristiques typiques des transducteurs capacitifs: une caractéristique hyperbolique obtenue pour un transducteur à rapprochement normal des électrodes, une caractéristique linéaire obtenue pour un transducteur à mouvement parallèle de l'électrode mobile, et une caractéristique de type "dent de scie" obtenue pour un transducteur à mouvement parallèle et à plusieurs segments (cf. Fig. 4).

Le transfert d'énergie du domaine électrique vers le domaine mécanique s'effectue lorsque

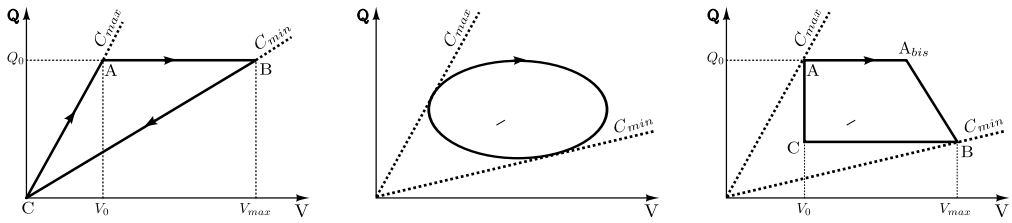


FIGURE 5: Trois cycles QV de conversion d'énergie par un transducteur capacitif: a) cycle QV à charge constante, b) cycle QV obtenu avec circuit de conditionnement primitif c) cycle QV obtenu avec une pompe de charge.

la capacité de transducteur diminue alors qu'elle reste chargée. L'énergie W du transducteur se calcule comme:

$$W = Q_0^2/(2C_{var}), \tag{2}$$

ainsi, si le transducteur reste chargé à la charge Q_0 pendant que sa capacité diminue, l'énergie électrique du transducteur augmente. En même temps, dans le domaine mécanique, le transducteur génère une force mécanique sur la masse mobile. Cette force s'oppose au mouvement de la masse (c.a.d., la direction de la force est opposée à celle de la vitesse). Ainsi, le mouvement de la masse est amorti et le domaine mécanique perd de l'énergie.

Ce processus de conversion d'énergie se décrit par un diagramme désignant l'ensemble des états de la capacité variable dans les axes charge–tension (QV). Dans le cas d'un REV soumis aux vibrations périodiques, le diagramme QV est un cycle dont l'aire est numériquement égale à l'énergie convertie durant ce cycle. Fig. 5a présente un exemple du cycle le plus commun qui s'appelle "cycle à charge constante". Les trois lignes du cycle correspondent au chargement du transducteur lorsque la capacité est maximale (CA), au mouvement de l'électrode mobile alors que la charge Q_0 est gardée constante (AB) et à la décharge du transducteur (BC). D'après la formule (2) on a pour le gain d'énergie:

$$\Delta W = \frac{Q_0^2}{2C_{min}} - \frac{Q_0^2}{2C_{max}} = \frac{1}{2}Q_0^2\left(\frac{1}{C_{min}} - \frac{1}{C_{max}}\right) = \frac{1}{2}V_0^2 C_{max}\left(\frac{C_{max}}{C_{min}} - 1\right), \tag{3}$$

où V_0 est la tension appliquée au transducteur lorsque sa capacité est maximale, $V_0 = Q_0/C_{max}$. On note que pour une configuration de géométrie donnée, un seul paramètre électrique V_0 (ou Q_0) définit l'énergie convertie. Ici C_{max} et C_{min} sont les valeurs extrêmes que prend la capacité du transducteur durant le cycle. La puissance convertie est obtenue en multipliant ΔW par f_e, la fréquence de variation de la capacité. On note que f_e n'est pas forcement la même que la fréquence de vibration de la masse, au cas où la fonction $C_{var}(x)$ n'est pas monotone (cf. Fig. 3b).

Les Fig. 5b,c présentent deux autres exemples de cycles QV qui correspondent à d'autres protocoles de conversion d'énergie, et qui seront discutés à l'occasion des circuits de conditionnement qui leurs sont associés.

A partir de cette présentation, on peut tirer deux conclusions importantes. Premièrement, la gestion de la charge–décharge du transducteur est nécessairement complexe. En effet, ce processus doit être strictement synchronisé avec les mouvements de la masse mobile ; ainsi, une mesure directe ou indirecte de la position de la masse est nécessaire. De plus, le cycle QV à charge constante nécessite au moins deux commutations par période de vibration. L'électronique de commande est donc complexe et coûteuse en terme de l'énergie consommée [Mitcheson12]. La deuxième conclusion concerne la nécessité pour un transducteur capacitif d'avoir une précharge initiale (une énergie initiale) permettant d'initier le processus de conversion d'énergie.

Ces deux aspects mettent à part le transducteur capacitif par rapport à ces homologues piézoélectriques et électromagnétiques, qui génèrent une énergie utilisable à partir du moment où des vibrations sont présentes. Pour les REVs piézoélectriques et électromagnétiques, le circuit de conditionnement sert essentiellement à assurer une interface électrique avec la charge utile tout en garantissant une extraction maximale de l'énergie mécanique [Lefeuvre09].

Circuit de conditionnement: principes et enjeux

Le rôle principal du circuit de conditionnement dans un REV capacitif est de charger et de décharger le transducteur capacitif selon un protocole assurant un cycle de conversion d'énergie. Nous présentons ici une série de circuits de conditionnement que nous avons étudiés durant nos recherches, pour aboutir à celui que nous avons choisi pour la base de nos développements.

Circuit de conditionnement primitif

Il s'agit d'un système composé d'une capacité variable, d'une capacité de réservoir de forte valeur préchargée à tension V_0 et d'une résistance de charge (Fig. 6a, [Basset09]). On peut voir que si la capacité C_{var} varie, il y a un flux de charge entre C_{var} et C_{res}; l'intensité de ce flux est fonction de la résistance R_{load}. Ce courant traversant une résistance dissipe de l'énergie: celle-ci est extraite du domaine mécanique grâce aux variations de la capacité C_{var}. Le cycle QV réalisé par un transducteur conditionné par ce circuit est donné Fig. 5b ; il est caractérisé par sa trajectoire lisse (absence d'"angles"), le circuit ne contenant pas d'interrupteurs.

Le fonctionnement de ce circuit est basé sur l'hypothèse que la somme des charges de C_{var} et C_{res} est constante dans le temps. Autrement dit, on fait l'hypothèse de l'absence de toute fuite sur ces deux capacités, ce qui est clairement pas réaliste. Ainsi, ce circuit ne présente pas d'intérêt applicatif. Cependant, il peut être utile dans un contexte de laboratoire par exemple, pour une caractérisation d'un transducteur fabriqué. Alors, la capacité C_{res} peut être remplacée par une source de tension continue. Cette technique a été utilisée pour caractériser les dispositifs MEMS (micro résonateur avec interface capacitif) conçus et fabriqués à l'ESIEE Paris.

Un autre problème de ce circuit est l'absence de mécanisme de précharge de la capacité C_{res}. En effet, il est connu qu'un transducteur capacitif nécessite souvent des tensions de

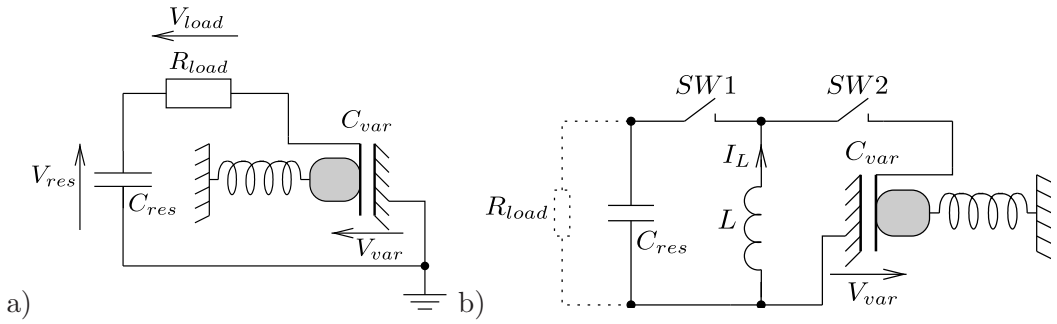


FIGURE 6: a) Circuit de conditionnement primitif [Basset09]; b) Circuit de conditionnement réalisant le cycle QV à charge constante [Meninger01].

polarisation élevées pour être efficace (des dizaines des volts). Or, les tensions disponibles initialement dans un système autonome sont souvent basses (quelque volts). Ce circuit ne contient pas de moyen permettant d'accroître sa tensions de polarisation à partir d'une (faible) tension initiale.

Il faut ajouter que ce circuit se prête difficilement à une analyse. Par exemple, un calcul analytique de la résistance R_{load} correspondant à la puissance maximale est impossible même pour de simples configurations; il met en jeu une équation différentielle non linéaire qu'il convient d'étudier en mode de grand signal. Il faut également ajouter que ce circuit retrouve son intérêt lorsqu'une couche d'électret est utilisée pour la polarisation initiale de la capacité variable [Yamashita10, Sterken07, Boisseau11]. Par conséquent, nous notons un potentiel inexploré que peut contenir une étude analytique de ce circuit.

Circuit réalisant un cycle à charge constante

Une architecture typique d'un circuit réalisant le cycle triangulaire à charge constante (Fig. 5a) est donnée Fig. 6b. La capacité de réservoir C_{res} est préchargée. Lorsque la capacité C_{var} est maximale, une énergie W_0 est transférée de C_{res} à C_{var} en utilisant L comme un réservoir d'énergie intermédiaire (il s'agit d'un procédé typique pour convertisseurs DC-DC). Ceci est fait à l'aide des interrupteurs $SW1$ et $SW2$ commandés par un circuit de commande non montré ici. Le temps que prend ce transfert doit être négligeable comparé à la période de variation de C_{var}. Ensuite les deux interrupteurs sont bloqués et C_{var} diminue en gardant la charge constante. Lorsque C_{var} arrive à sa valeur minimale C_{min}, le circuit de conditionnement effectue un transfert d'énergie inverse de C_{var} à C_{res}. Comme illustré par les formules (3) et (7), la capacité C_{res} reçoit plus d'énergie qu'elle ne contenait au début.

À la différence avec le circuit précédent, les capacités C_{var} et C_{res} s'échangent de l'énergie et non des charges. Par conséquent, il n'y a pas de problèmes de fuites ; au contraire, les fuites de C_{res} sont assimilées à une charge utile connectée en parallèle avec C_{res} (en pointillées).

Ce circuit réalise le cycle QV à charge constante; il en possède dont les inconvénients. En particulier, on note un timing précis nécessaire pour la commande des interrupteurs, et le fait d'avoir 4 commutations par cycle de variation de C_{var}.

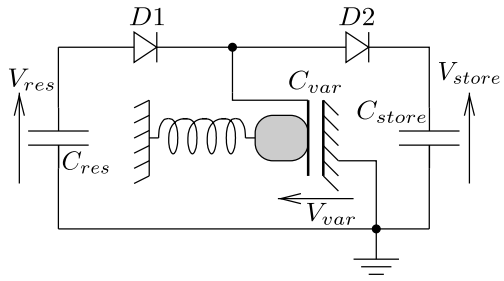


FIGURE 7: Pompe de charge utilisée pour conversion d'énergie mécanique en électricité.

L'architecture présentée Fig. 6b et ses variantes sont les mieux étudiées par la communauté des concepteurs des REVs. Il existe, à notre connaissance, trois réalisations complètes et fonctionnelles de ce circuit. La première, la plus ancienne et la plus proche de l'architecture de la Fig. 6b est réalisée à MIT[2] par S. Meninger [Meninger01]. Un autre circuit fonctionnant selon le même principe a été réalisé par G. Despesse [Despesse05]. Le circuit utilise un transformateur plutôt qu'une inductance pour le transfert d'énergie, et fonctionne avec un dispositif résonateur/transducteur de taille macroscopique. Une des plus récentes réalisations d'un REV de type à tension constante a été présentée par E. Torres [Torres09]. Le système présenté utilise une batterie à la place de la capacité réservoir C_{res} ; cela permet de recharger la batterie lorsqu'il y a des vibrations externes.

Pompe de charge comme circuit de conditionnement

Le problème de la commande du flux des charges sur le transducteur est absent dans les circuits de conditionnement basés sur une pompe de charge (Fig. 7). Celle-ci est composée de deux diodes et trois capacités, dont l'une est une grande capacité réservoir C_{res}, la deuxième est une capacité de taille intermédiaire C_{store}, et la troisième est la capacité variable du transducteur, de valeur maximale la plus petite de trois:

$$C_{res} >> C_{store} >> C_{var\ max} \tag{4}$$

À l'état initial, la capacité réservoir est préchargée à la tension $V_{res} = V_0$. Grâce aux variations de la capacité C_{var}, les charges électriques se transfèrent de la capacité C_{res} à la capacité C_{store}. Un tel transfert des charges d'une grande capacité vers une petite capacité s'accompagne d'une accumulation de l'énergie électrique du système capacitif $C_{store}C_{res}$, en vertu de la formule (2). L'énergie vient du domaine mécanique: ainsi une partie de l'énergie des vibrations externes est convertie en électricité.

Ce circuit très simple a cependant un mécanisme de fonctionnement complexe. Nous en donnons ici quelques éléments principaux.

Partant de l'état initial correspondant à l'égalité des tensions V_{res} et V_{store}, l'état du système $C_{res}C_{store}$ évolue comme présenté Fig. 8. On y voit les tensions V_{store}, V_{res} et l'énergie ΔW_i convertie en chaque cycle de variation de C_{var}. On constate que l'énergie

[2]Massachusetts Institute of Technology

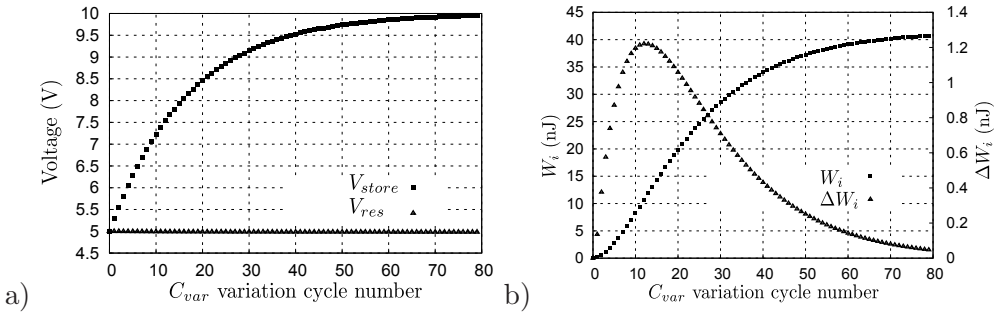


FIGURE 8: Évolution de l'état de la pompe de charge: a) Les tensions V_{store} et V_{res}. V_{store} évolue de la tension V_{res} (5V dans cet exemple) jusqu'à la tension de saturation (10 V dans cette exemple), V_{res} ne change presque pas (C_{res} est large) b) l'énergie convertie par cycle de vibration ΔW_i et depuis le début du pompage W_i

convertie par cycle augmente au début, atteint un maximum et puis diminue jusqu'à zéro. En même temps, la tension V_{store} tend asymptotiquement vers une valeur appelée "tension de saturation" égale à:

$$V_{store\ sat} = V_{res}\frac{C_{max}}{C_{min}}. \tag{5}$$

Lorsque la pompe de charge est saturée, il n'y a plus de conversion d'énergie. Il est donc nécessaire de retourner la pompe de charge vers un état où la génération d'énergie est proche du maximum. D'après la Fig. 8, il s'agit de réduire la tension V_{store}. Cela est fait à l'aide d'un circuit de retour (*flyback*) dont deux versions sont présentées dans les deux sections suivants.

Circuit de retour résistif

Un circuit de retour élémentaire est réalisé par une résistance branchée entre C_{res} et C_{store} (Fig. 9). Dans ce cas, il y a deux flux de charges: l'un, source d'énergie électrique, de C_{res} vers C_{store} poussé par les variations de C_{var}, l'autre, consommateur d'énergie électrique, celui de la résistance R_L. En régime établi, il est possible de choisir une valeur R_{load} pour laquelle la puissance d'énergie convertie est optimale (i.e., correspond au maximum de ΔW_i à la Fig. 8b). La résistance R_{load} peut être vue comme une charge utile.

Les faiblesses de ce circuit sont similaires à celles du circuit de la Fig. 6a : son fonctionnement est basé sur l'hypothèse de l'absence de fuites dans les capacités. Dans le cas contraire, la précharge de C_{res} finit par devenir nulle et le circuit devient inactif. Ce problème peut être résolu par des techniques de compensations proposées par H.R. Florentino [Florentino11]. Il y est proposé d'adjoindre un générateur d'énergie supplémentaire à base d'un transducteur piézoélectrique, qui compenserait les pertes dans les capacités. Alors que cette solution peut être envisageable dans certains cas, elle n'est cependant pas très commode, car cela revient à utiliser deux REVs dont l'un alimente l'autre. Une des difficultés que l'on y voit est un nécessaire accord en fréquence des deux résonateurs, ce qui est difficile en pratique car les bases technologiques pour leur fabrication sont nécessairement différentes.

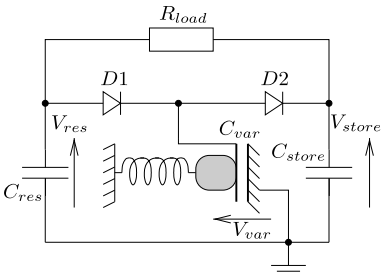


FIGURE 9: Pompe de charge avec un circuit de retour résistif.

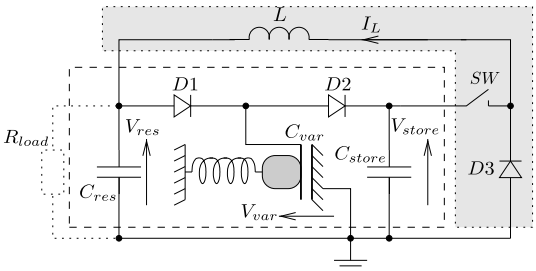


FIGURE 10: Circuit de conditionnement à base de la pompe de charge utilisant un circuit de retour de type convertisseur DC-DC BUCK, proposé par Yen [Yen06].

On note une absence du mécanisme d'élévation de la tension de polarisation, de même que pour le circuit de conditionnement primitif de la Fig. 6a.

Ces difficultés nous amènent au circuit de retour de type convertisseur DC-DC de type BUCK qui est exempt des inconvénients mentionnés.

Circuit de conditionnement proposé par Yen

Ce circuit a été proposé par B. C. Yen et J. H. Lang en 2006 à MIT [Yen06], son schéma est donné Fig. 10. Le circuit de retour est basé sur un convertisseur DC-DC de type BUCK. Ce circuit de conditionnement fonctionne en deux phases. Durant la première phase, l'interrupteur SW est bloqué et seule la pompe de charge fonctionne comme présenté plus haut. Ensuite, lorsque la pompe de charge approche la saturation ($V_{store} = V_2$), un circuit de commande (non montré) rend l'interrupteur passant, en activant le circuit de retour. Le retour se fait en deux étapes. D'abord, une partie de charges de C_{store} retourne vers C_{res}, en abaissant ainsi la tension de C_{store}. Pendant ce processus, la capacité C_{res} retrouve ses charges, et l'énergie transférée du domaine mécanique est emmagasinée dans l'inductance L. Lorsque la tension V_{store} a baissé jusqu'à V_1, l'interrupteur se bloque et l'inductance se décharge sur la capacité C_{res} via la diode D_3 empêchant un retour de charges. Puis le cycle recommence (Fig. 11).

Ce fonctionnement présente une série d'avantages qui nous ont fait choisir ce circuit comme base pour notre étude.

a) Accumulation de l'énergie convertie. En absence de charge utile, l'énergie convertie s'accumule sur la capacité C_{res}. Il est donc possible d'élever sa tension jusqu'au niveau nécessaire, en démarrant par une faible précharge qui peut être fournie avec une source de tension existante dans le système.

b) Présence d'un seul interrupteur fonctionnant rarement et qui ne nécessite pas une synchronisation avec les mouvements de la masse. L'interrupteur commute une fois durant plusieurs périodes de vibration de la masse: donc, la commande se fait à des

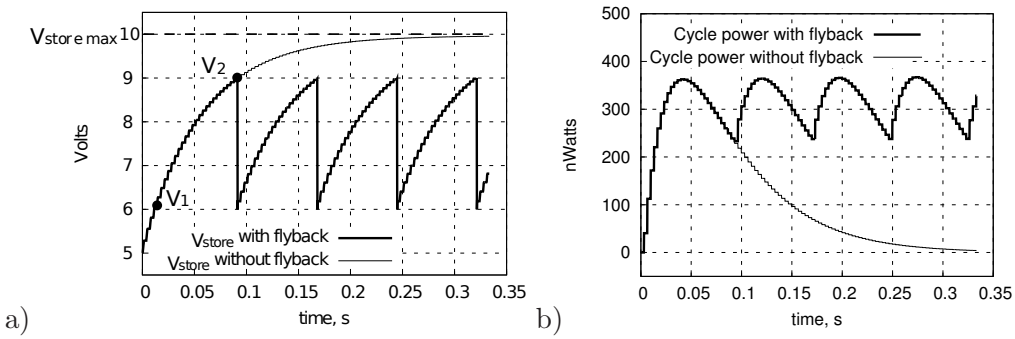


FIGURE 11: Évolution de l'état de la pompe de charge avec circuit de retour: a) La tension V_{store}. b) Puissance moyenne de conversion d'énergie par cycle de vibration ΔW_i.

fréquences bien plus basses que dans le cas du circuit de Meninger (Fig. 6b). Moins d'énergie est donc nécessaire pour la commande.

c) La commutation pompe de charge/circuit de retour se fait en fonction de la valeur de la tension V_{store}. Il est en effet bien plus simple d'utiliser une tension pour le contrôle, plutôt qu'une valeur de capacité ou une grandeur mécanique.

Ce sont surtout les deux derniers points qui nous ont fait choisir ce circuit pour la base de nos développements pratiques d'un REV capacitif avec conditionnement intelligent. Les problèmes associés à ce travail et le résumé des résultats sont présentés dans la suivante section.

Circuit de conditionnement adaptatif intégré

Ce paragraphe résume nos idées sur le circuit de conditionnement adaptatif et intelligent, et résume nos travaux de conception d'un circuit de démonstrateur.

Analyse du circuit de Yen: recherche du fonctionnement optimal

L'article de Yen publié en 2006 [Yen06] présente un premier démonstrateur d'un circuit de conditionnement basé sur la pompe de charge et utilisant un circuit de retour de type BUCK DC-DC. L'interrupteur SW est réalisé par un transistor MOS commandé par une source externe. Cette source génère un train périodique d'impulsions indépendantes de l'état du circuit. Cette expérience a démontré la faisabilité de cette technique. Cependant, ce travail a ouvert un vaste champs de problèmes, notamment, en ce qui concerne la définition d'un régime optimal et la conception d'une commande garantissant ce régime. La théorie du circuit était incomplète: par exemple, il manquait une expression de la puissance maximale convertible par ce circuit. Il n'était alors pas possible d'établir une comparaison des performances avec le circuit réalisant un cycle QV charge constante (circuit de la Fig. 6b).

Afin de combler ces lacunes, la première étape a été d'analyser le circuit en identifiant des conditions optimales de fonctionnement. Il était également important de comparer ce

circuit avec le circuit réalisant une conversion d'énergie à charge constante, qui était une approche dominante à l'époque. Enfin, il a fallu proposer un algorithme de commande pour l'interrupteur, qui tiendrait compte de l'état électrique du circuit et des conditions d'environnement. Ici nous résumons les résultats de cette étude.

Nous souhaitons citer ici le travail d'une équipe de Rensselaer Polytechnic Institute, (USA) [Kempitiya12], qui s'est intéressé à l'analyse et à l'amélioration du circuit avec flyback de type BUCK à peu près à la même période que nous. Une série de publications récentes présentent une réalisation d'un REV avec un transducteur capacitif de taille macroscopique (30×15 cm^2), avec un interrupteur réalisé par un transistor MOS commandé par un circuit de commande, avec une puissance maximale obtenue de 308 nW.

Efficacité théorique du circuit de conditionnement de Yen

Pour évaluer l'efficacité de la pompe de charge avec circuit de retour de type BUCK, nous avons identifié la puissance maximale que pouvait convertir une pompe de charge [Basset09] :

$$P_{max} = \frac{1}{4} V_0^2 C_{min} \left(\frac{C_{max}}{C_{min}} - 1 \right)^2 \cdot f_e \approx \frac{1}{4} V_0^2 C_{max} \frac{C_{max}}{C_{min}} \cdot f_e. \tag{6}$$

La dernière approximation est valable si $C_{max} >> C_{min}$, ce qui est le cas dans la plupart des cas en pratique. f_e est la fréquence de variation de la capacité de transducteur. Nous avons calculé que cette puissance est uniquement convertie lorsque la tension V_{store} vaut:

$$V_{store_{opt}} = \frac{1}{2} V_0 \left(\frac{C_{max}}{C_{min}} + 1 \right) \approx \frac{1}{2} V_0 \frac{C_{max}}{C_{min}} \tag{7}$$

On note qu'en cas de grand rapport C_{max}/C_{min}, à paramètres égaux le circuit de Yen produit exactement deux fois moins d'énergie que le circuit réalisant un cycle QV à charge constante (comparer eq. (6) avec (3) en posant $V_0 = V_{res}$). Ceci est un inconvénient manifeste. Cependant, un autre facteur doit être considéré: la tension maximale générée sur le transducteur et qui doit être supportée par les circuits de contrôle. Dans le cas du circuit de Yen, la tension maximale supportée par le transducteur est $V_{store\ opt}$. Elle est donc donnée par (7), et elle est 2 fois plus petite que la tension maximale dans un cycle QV charge constante $V_0 C_{max}/C_{min}$. Ainsi, *à même tension maximale le circuit de Yen fournit* 2 *fois plus de puissance*, car celle-là est proportionnelle au carré de la tension. Puisque les technologies des circuits électroniques imposent une limite sur la tension supportée, cet avantage du circuit Yen est sans doute très important du point de vue de sa réalisation pratique.

Scénario permettant un fonctionnement optimal

On constate qu'à la différence du circuit de Meninger (Fig. 6b), deux paramètres électriques définissent l'énergie convertie en un cycle de conversion : V_{res} et V_{store}. Comme le montre la Fig. 8b, à chaque cycle de pompage l'énergie convertie est différente.

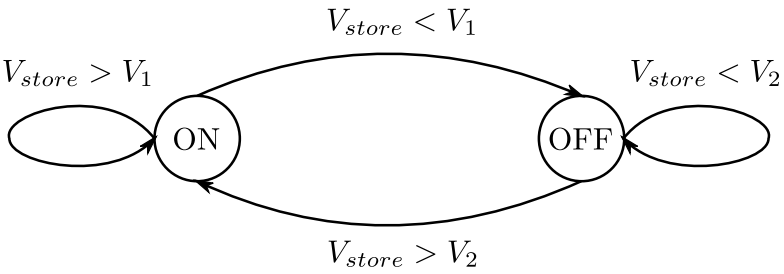


FIGURE 12: Automate d'états finis régissant le fonctionnement de l'interrupteur du circuit de retour.

Elle n'est maximale que pour la valeur V_{store} donnée par l'expression (7), qui est respectée uniquement sur un cycle de pompage. Ainsi, garantir un fonctionnement optimal à ce circuit revient à activer le circuit de retour une fois par cycle de variation de C_{var}. Ceci est possible si le circuit de retour est réalisé par une résistance (cf. Fig. 9): cette technique a été utilisée pour tester les dispositifs MEMS fabriqués à l'ESIEE Paris par Raphaël Guillemet [Guillemet13]. Cependant, dans le cas d'utilisation du circuit de retour de type BUCK, cela fait perdre les avantages principaux de l'architecture, qui sont l'absence de synchronisation du retour des charges/énergie avec les mouvements de la masse et une faible fréquence de ces retours.

Pour trouver un compromis entre la maximisation de la puissance convertie et le coût d'activation du circuit de retour, nous avons proposé de maintenir la puissance convertie à un certain niveau ne dépassant pas le niveau maximal moins quelques pour cents, comme c'est affiché sur la courbe ΔW_i de la Fig. 11b. Cela permet de définir un intervalle des valeurs de V_{store} pour lesquelles le circuit peut fonctionner en mode optimal (V_1, V_2) (Fig. 11a), et ainsi de définir les moments de commutation de l'interrupteur en mesurant la tension sur une grande capacité C_{store}, plutôt qu'en détectant les extrema de variation de la faible capacité C_{var} [Galayko07]. Nous avons établi une équation empirique permettant une estimation de seuils de commutation:

$$V_1 = V_{res} + 0.2(V_{res} - V_{store\ sat}), \quad V_2 = V_{res} + 0.7(V_{res} - V_{store\ sat}) \tag{8}$$

Il est maintenant possible de construire un automate d'états finis qui commandera l'état de l'interrupteur. Cet automate est commandé par les événements de croisement des seuils V_1 et V_2 par la tension V_{store}. Le diagramme de l'automate est présenté Fig. 12.

Besoin d'autocalibration

Les points 1) et 2) présentés dans la sous-section précédente amènent sur la conclusion suivante: l'intervalle des valeurs optimales de (V_1, V_2) est défini par V_{res} et la tension de saturation de la pompe de charge qui dépend de C_{max}/C_{min}. Alors que V_{res} se mesure sans difficulté, les valeurs C_{max} et C_{min} dépendent, en général, de l'amplitude des vibrations. Par exemple, au cas où la fonction $C_{var}(x)$ est de type hyperbolique

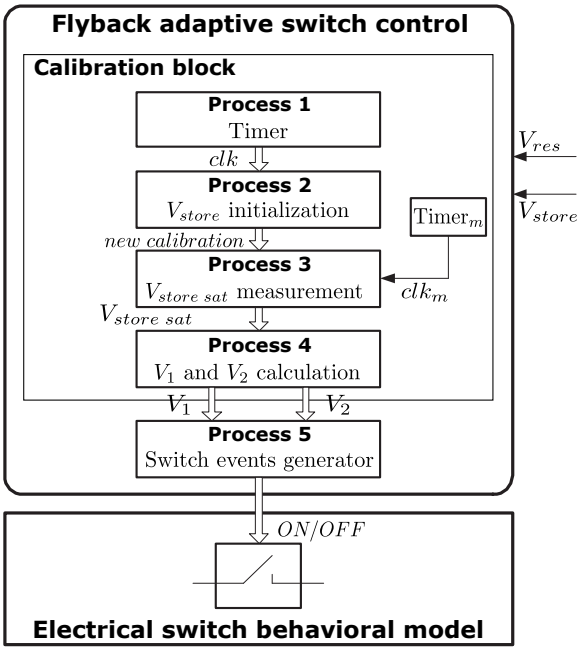


FIGURE 13: Algorithme de fonctionnement du circuit de conditionnement intelligent [Dudka09b].

(transducteur à rapprochement des électrodes, C_{max} et C_{min} sont définis comme :

$$C_{max,min} = \epsilon_0 \frac{S}{d - X_0 \pm X_1} \tag{9}$$

où X_0 est une éventuelle position moyenne de la masse mobile, X_1 est l'amplitude des mouvements de la masse.

Les paramètres X_0 et X_1 dépendent des paramètres des vibrations externes (l'amplitude et la fréquence) qui sont sujettes aux variations. De même, les paramètres du système ne sont connus qu'avec une certaine précision, notamment, les paramètres du résonateur et du transducteur. Ainsi, a priori, il n'est pas possible de connaître le rapport C_{max}/C_{min}, et donc, de trouver les valeurs V_1 et V_2 optimales dans un contexte pratique.

Ces conclusions mettent en évidence la nécessité de prévoir un système d'autocalibration pour un REV utilisant le circuit de Yen. Cette autocalibration doit se faire périodiquement, tout au long du fonctionnement du circuit, car l'amplitude des vibrations externes est susceptible de changer à tout moment. Durant la phase d'autocalibration, la mesure de C_{res}/C_{store} peut se faire à travers la mesure de la tension de saturation de la pompe de charge. Pour cela on doit désactiver le circuit de retour et laisser évoluer la tension V_{store} selon la courbe de la Fig. 8a, tout en détectant la saturation et en mesurant la valeur $V_{store\ sat}$ (cf. eq. 5). Cet algorithme proposé dans cette thèse est présenté à la Fig. 13, [Dudka09b]. Il est à la base d'un modèle VHDL-AMS utilisé pour la conception du circuit.

À partir de ces réflexions, nous avons établi un cahier de charge pour le circuit de commande du circuit de conditionnement de Yen.

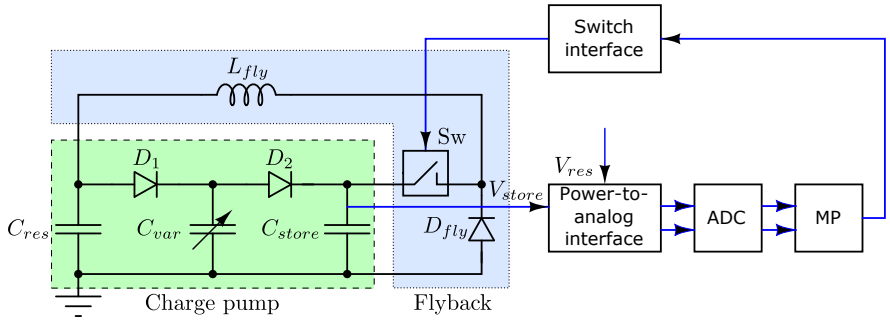


FIGURE 14: Architecture générique d'un circuit de conditionnement intelligent.

Circuit de conditionnement et intelligence

L'étude du circuit de Yen présentée ci-dessus suggère que le circuit de conditionnement doit être adaptatif. Il s'agit d'une fonction "intelligente" qui suppose un traitement d'information complexe, nécessairement consommateur d'énergie. L'adaptation doit dépendre du contexte applicatif et globalement, doit pouvoir gérer le flux d'énergie extérieur disponible - par exemple, faire "endormir" le système si l'énergie disponible est trop faible.

Pour ces raisons, nous contestons la vision des dispositifs de récupération d'énergie vibratoire comme étant primitifs et nécessitant des solutions analogiques optimisées *ad hoc* pour un contexte particulier. Nous pensons que les REVs ne peuvent devenir réellement pertinents pour les applications que s'ils intègrent une complexité et une intelligence. À l'état actuel des technologies, cette vision est peu réaliste: la puissance délivrée par les micro générateurs étant de quelques microwatt, ce niveaux est à peine suffisant pour alimenter la charge utile (c.a.d., le fonctionnement de l'application). Cependant, les études sur la récupération d'énergie à micro échelle sont basées sur un pari selon lequel dans le futur, les niveaux d'énergie requis par les microsystèmes électroniques de traitement continueront à baisser. Ainsi, arrivera un moment où l'intelligence se trouvant dans le circuit de conditionnement ne nécessitera qu'une petite partie de l'énergie récupérée. Cela a motivé et justifié notre étude, dans laquelle nous avons proposé et développé une approche de la conception d'un système de REV capacitif avec comportement complexe et auto adaptatif.

Cette vision idéalisée et futuriste de circuit de conditionnement intelligent est donnée Fig. 14, qui présente une boucle de contre-réaction prenant la mesure des tensions V_{res} et V_{store}. Les résultats de ces mesures sont numérisés et analysés par un bloc de traitement numérique représenté ici par un microprocesseur (MP), qui ensuite génère une commande pour l'interrupteur.

Les recherches sur le développement d'un circuit de conditionnement adaptatif et intelligent sont les objectifs principales de cette thèse. Pour atteindre ces objectifs, ce travail s'est fait en deux étapes: conception d'un algorithme de fonctionnement du circuit et conception du circuit réalisant cet algorithme. Dans les sous-sections suivantes nous présentons les problèmes auxquels nous avons été confrontés et les choix stratégiques que nous avons faits.

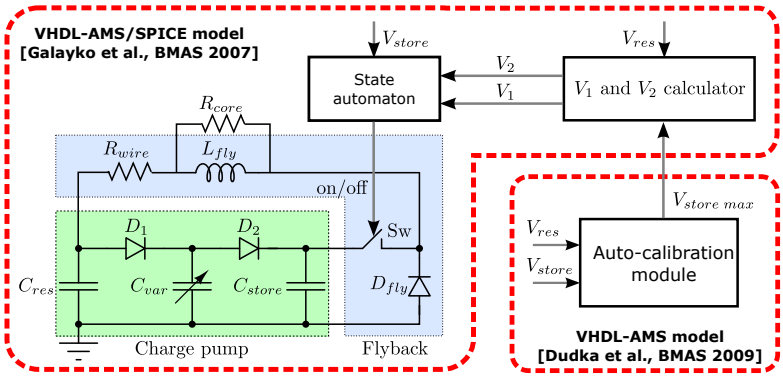


FIGURE 15: Architecture du circuit de conditionnement développé, avec mention des outils de modélisation utilisés pour chaque partie.

Circuit de conditionnement auto adaptatif: architecture

Une conception au niveau de système a été la première étape du développement. Il s'agit d'une élaboration de l'algorithme de calibration, d'un choix de l'architecture du circuit de commande et d'une validation par modélisation comportementale du système de REV complet.

L'idée de base consiste à entrecouper la phase de conversion d'énergie par des phases d'autocalibration. L'hypothèse suivante a été faite: les paramètres d'environnement sont supposés évoluer lentement, et donc les valeurs V_1 et V_2 trouvées lors d'une phase d'autocalibration restent actuelles jusqu'à la prochaine phase. La vitesse d'évolution des conditions d'environnement détermine la fréquence avec laquelle il faut calibrer le circuit. Cette fréquence dépend du contexte applicatif, et peut aller de quelques secondes à quelques minutes.

Fig. 15 présente l'architecture du circuit de conditionnement adaptatif que nous avons développé [Dudka09a], avec l'indication des outils permettant une modélisation de chaque bloc. L'étude qui a permis un choix approprié des outils de modélisation est résumée dans une des sections suivantes.

Conception de circuit intégré

La deuxième étape consiste à concevoir un circuit électronique réalisant cette architecture. L'objectif étant la miniaturisation, le circuit de conditionnement doit être intégré sur silicium autant que possible. Sans rentrer dans les détails de la conception, donnés dans nos articles [Dudka09b, Dudka12, Dudka13b], nous énumérons les verrous auxquels nous étions confrontés.

- *Hautes tensions nécessaires pour le fonctionnement du transducteur électrostatique.* La plus grande difficulté de ce projet résulte des hautes tensions auxquelles fonctionne le circuit de conditionnement. Nous nous sommes donnés une limite de 50 V pour la tension maximale que ce circuit doit pouvoir supporter (les tensions sur

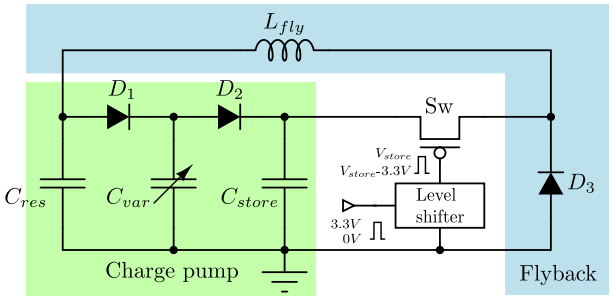


FIGURE 16: Illustration du problème de la commande d'un interrupteur "flottant" haute tension.

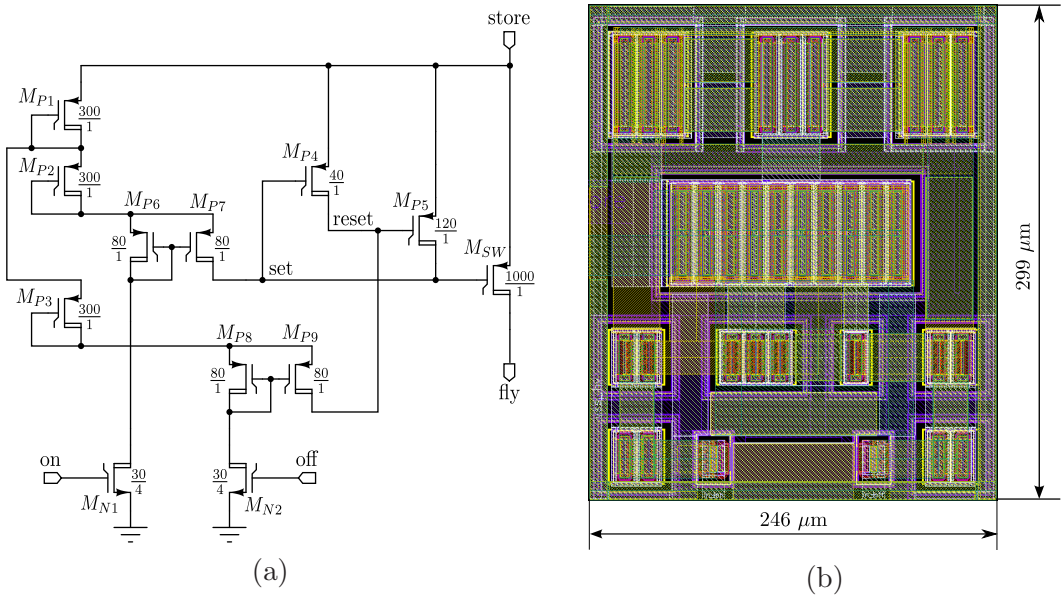


FIGURE 17: Circuit de commande de l'interrupteur avec un nouveau élévateur de tension, circuit réalisé en technologie AMS035HV [Dudka12]: (a) schéma (b) layout.

le transducteur et sur C_{store}). Les difficultés mentionnées plus bas sont toutes plus ou moins liées à cette contrainte.

- *L'interrupteur SW flottant à haute tension.* L'interrupteur SW n'est pas raccordé à la masse: lorsqu'il est coupé, il subit une tension flottante. Cet interrupteur est réalisé par un transistor PMOS haute tension, dont la tension de commande doit être générée par rapport à la haute tension de la source du transistor (cf. Fig. 16). Un élévateur de tension (*level shifter*) est donc nécessaire, avec une contrainte de consommation statique proche de zéro. Cette difficulté est un des plus étroits goulets d'étranglement de ce projet, car le coût énergétique de la commutation de SW a un rôle central dans l'efficacité de la conversion d'énergie par le circuit. La conception d'un élévateur de tension ultra basse consommation a été effectuée avec succès en s'inspirant de l'architecture utilisée par P. Basset [Basset03]. Un prototype intégré de l'interrupteur associé au dispositif de contrôle et de l'élévateur de tension ultra basse consommation (cf. Fig. 17) a été réalisé, fabriqué en technologie 0.35 μm haute tension et testé.

- *Une large plage de la tension de fonctionnement.* Comme il a été mentionné, au démarrage le circuit de conditionnement possède une énergie fournie par le système. Ainsi, les tensions V_{res} et V_{store} sont basses au début, avec $V_{res} \approx 2-3$ V, et $V_{store:;max} \approx 6-10$ V. En régime optimal, selon les paramètres des vibrations externes, la tension V_{store} peut atteindre la valeur maximale autorisée par le système ($50\ V$). Ainsi, le circuit de commande doit être efficace pour toute la gamme des tensions de fonctionnement, ce qui est difficile à atteindre. Par exemple, pour mesurer les hautes tensions V_{res} et V_{store}, la première approche consiste à utiliser des diviseurs à base de diodes ou transistors MOS en régime sous le seuil. Cependant, compte tenu de la plage de tensions à mesurer (facteur min/max de 5), cette solution ne convient pas. L'utilisation des résistances de très haute valeur s'impose alors, ce qui oblige à utiliser des résistances discrètes [Dudka12].

- *La contrainte ultra basse consommation.* Un des objectifs de l'étude est d'estimer le niveau de consommation minimale que peut avoir un circuit de conditionnement intelligent comme celui de la Fig. 15. *A priori*, il était difficile de se donner un chiffre plafond précis. Néanmoins, on peut dire que la consommation des blocs du circuit de conditionnement ne doit pas dépasser $1-3\ \mu W$. C'est une contrainte très forte qui a marqué la plupart des choix d'architecture. Par exemple, la division des hautes tensions pour la mesure se fait non pas en continu, mais par échantillonnage.

Le circuit complet conçu au niveau transistor est donné Fig. 3.9. Ce circuit est validé par simulation de son modèle ELDO (Spice) dans le contexte du modèle VHDL-AMS/ELDO mixte du récupérateur (Fig. 15). Les performances sont satisfaisantes, en particulier, la consommation moyenne est entre 1 et 2 μW, selon le régime électrique. Il utilise la technologie CMOS 0.35 haute tension d'Austria Microsystems. Compte tenu de la maturité de cette technologie et par conséquent de la fiabilité des modèles de transistors, nous avons un haut degré de confiance en résultats de simulation.

Conception du circuit de conditionnement: travaux futurs

Pour que la preuve de concept soit complète, les questions suivantes doivent être abordées dans la suite de l'étude.

Les blocs "périphériques" nécessaires au fonctionnement autonome du circuit. Il s'agit des sources d'alimentation, de polarisation et d'horloge. Ces fonctionnalités sont primordiales pour tout circuit intégré. Or, dans le contexte de la récupération d'énergie, la conception des blocs périphériques représente un projet de recherche à part entière. En effet, le REV est un système auto alimenté: amorcé par une énergie fournie par le système, il doit procurer l'énergie pour son alimentation à partir de son propre fonctionnement. Une solution possible a été proposée dans cette thèse, permettant de générer une (basse) tension d'alimentation stable à partir de la tension de la capacité C_{res} qui peut varier de 3 à 15 V [Dudka09a]. Cette solution n'a pas encore été réalisée au niveau des transistors: cette tâche sera l'objet des travaux futurs.

Le circuit de conditionnement de la Fig. 3.9 nécessite deux horloges de basse fréquence: l'une a le même ordre de grandeur que la fréquence des vibrations (≈100 Hz), l'autre doit permettre de cadencer la succession des phases de calibrations et a donc une période

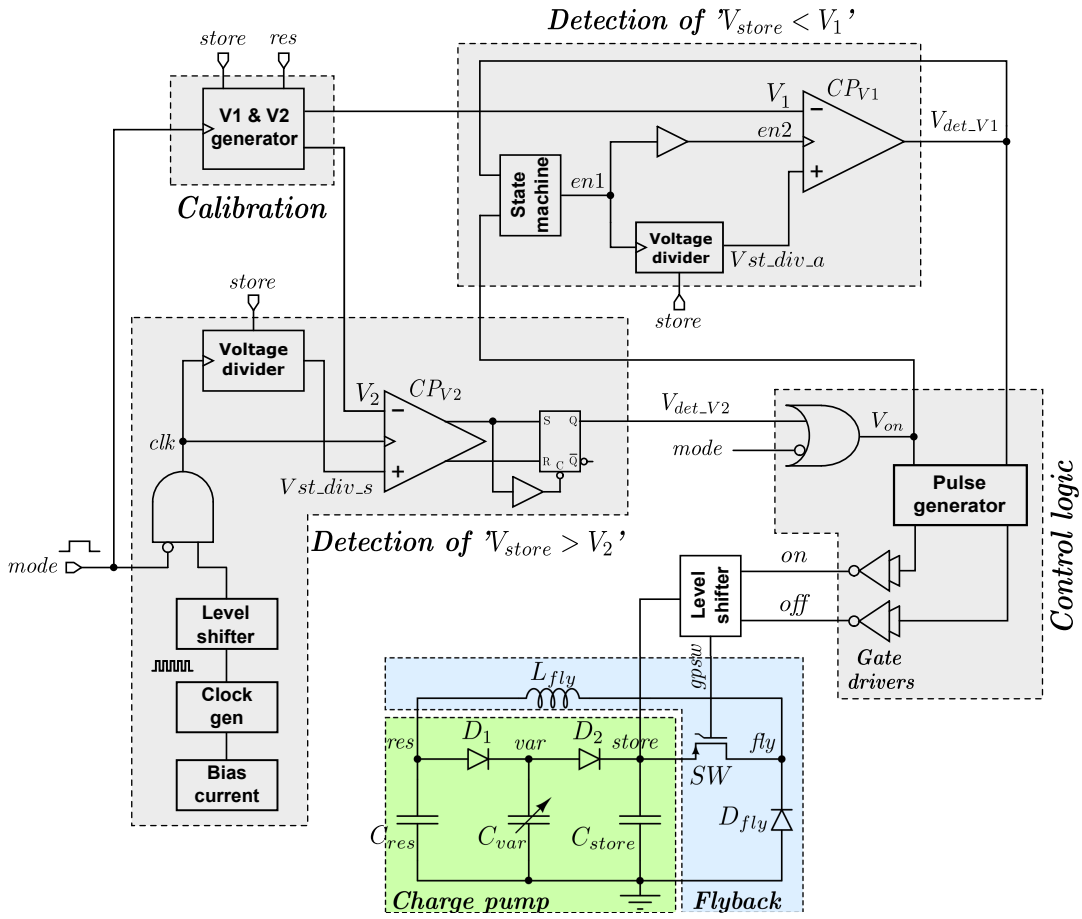


FIGURE 18: Schéma électrique du circuit de conditionnement intelligent conçu [Dudka13b].

de 1 à 100 secondes. Une étude bibliographique sur le sujet a mis en évidence un grand intérêt de la communauté envers de tels circuits, pour les applications de type capteurs autonomes et systèmes biomédicaux embarqués dans du vivant. Par exemple, un capteur se trouvant en veille et devant s'activer de temps en temps a besoin d'une telle horloge. Ici, la contrainte principale est la basse consommation, qui doit être respectée quitte à sacrifier la précision du timing. Une première approche de ce travail été faite dans le cadre du stage de master recherche d'Anthony Déluthault à LIP6.

Interface avec la charge. Le problème dé génération d'une alimentation stable basse tension pour les circuits de traitement est lié à un problème plus fondamental, celui de l'interface avec une charge utile. Cela inclut au minimum une génération de tension stable qui peut être utilisée par la charge. De plus, il est nécessaire de proposer un mécanisme capable de gérer une situation où l'énergie disponible ne serait pas suffisante pour alimenter la charge. Ce problème a été abordé durant cette thèse. Il a été proposé de réutiliser le convertisseur DC-DC du circuit de retour afin de générer une tension de sortie stable. Il s'agit d'un convertisseur DC-DC à sorties multiples: une structure fréquemment utilisée dans les circuits d'alimentation multi tensions. Le principal avantage de cette solution est la réutilisation de l'inductance L déjà présente dans le circuit de retour [Dudka09a].

Modélisation des REVs

Motivations

Les techniques de modélisation occupent une place centrale dans la conception de circuits et systèmes électroniques, principalement, à cause du coût élevé du prototypage physique, de la complexité des systèmes et de la puissance des calculateurs actuels. La particularité de nos problèmes vient du caractère multidisciplinaire du système, et de l'hétérogénéité des signaux qui y sont présents. On s'intéresse à la modélisation pour les objectifs suivants:

– *Une exploration du système.* Une modélisation comportementale représente un excellent outil d'expérimentation virtuelle, lorsqu'il s'agit de répondre rapidement à une question relative au comportement du système dans un contexte particulier. Ainsi, la découverte des régimes stochastiques et irréguliers [Galayko11b] du REV de la Fig. 6b a été faite grâce à la modélisation comportementale.

– *La conception du système et de ses blocs.* La méthodologie dominante de conception est "top-down": cela signifie que d'abord le système est conçu sur le plan fonctionnel, à haut niveau d'abstraction. Ensuite chaque bloc/fonction sont conçus d'une manière de plus en plus détaillée, jusqu'au niveau des composants élémentaires de la technologie. La modélisation accompagne ce processus en descendant les niveaux d'abstraction, afin de valider chaque étape de conception.

Les spécificités de la micro fabrication font que les concepteurs des MEMS ont moins de libertés de conception que les concepteurs de circuits électriques et de logiciels. Pour cette raison, souvent un dispositif MEMS existant constitue une donnée lors de la conception du système. Dans notre projet, les dispositifs MEMS constitués d'un résonateur associé à un transducteurs ont été fabriqués et caractérisés par le groupe de Philippe Basset à l'ESIEE Paris. Nous avons construit des macromodèles de ces dispositifs et nous les avons ensuite utilisés dans le modèle du système global.

Choix de la plate-forme

La question que nous nous sommes posé au début du projet concerne le choix de la plate-forme de modélisation. Une étude comparative a été faite par Ken Caluwaerts dans le cadre de son stage de master recherche à LIP6, au cours duquel trois environnements ont été testés pour une modélisation du système présenté Fig. 15 : Matlab/Simulnk, SystemC-AMS et la plate-forme AdvanceMS de Mentor Graphics. La plate-forme SystemC-AMS était, à l'époque, une nouveauté dans l'univers de modélisation de systèmes hétérogènes, et elle était en pleine évolution. Étant une plate-forme libre, elle suscitait un grand intérêt dans la communauté de concepteurs de systèmes électroniques. Nous avons voulu évaluer son potentiel pour la modélisation de systèmes de REV, sur l'exemple du système de la Fig. 15.

La version de l'époque (2008) de la plate-forme SystemC-AMS s'est avérée peu adaptée à la simulation de système de ce type[3], principalement, en raison du nombre limité de méthodes de résolution d'équations non linéaires qu'elle offrait. En effet, la plate-forme a utilisé des méthodes d'intégration à pas temporel fixe, ce qui était un facteur fortement limitant pour les systèmes fonctionnant simultanément à multiples échelles de temps comme dans le cas d'un système de REV.

C'était la plate-forme AdvanceMS de Mentor Graphics qui s'est avérée le plus appropriée pour nos besoins. Elle permet de mélanger les modèles VHDL-AMS (analogiques comportementaux), VHDL (numériques) et ELDO (une variante commerciale de SPICE développée par Mentor Graphics), et offre une large palette des méthodes numériques pour l'intégration des équations du système [Pêcheux05]. De plus, l'interface utilisateur est bien plus évoluée que celle des deux autres plates-formes testées. C'est donc cet outil qui a été choisi pour la simulation et la conception de nos REVs.

Modélisation du bloc transducteur/résonateur

Un transducteur capacitif est modélisé par un système de ses équations :

$$i_{var} = \frac{\mathrm{d}q_{var}}{\mathrm{d}t}, \quad q_{var} = C_{var}(x)V_{var}), \quad f_{var} = \frac{1}{2}V_{var}^2\frac{\mathrm{d}C_{var}}{\mathrm{d}x} \tag{10}$$

Ici q_{var} est la charge électrique du transducteur, i_{var} est le courant qui le traverse, x est la position de l'électrode mobile. $C_{var}(x)$ est une fonction connue caractérisant la relation entre la capacité du transducteur et la position de son électrode mobile.

Ces trois dernières équations possèdent 5 inconnues: q_{var}, i_{var}, V_{var}, f_{var} et x. Les deux relations manquantes doivent être définies par les sous-systèmes mécaniques et électriques associés au transducteur. Du coté mécanique, l'équation manquante est donnée par celle du sous-système mécanique. En prenant comme exemple un résonateur du second ordre avec une masse m, un amortissement μ et une constante de raideur k, on a :

$$-\mu\dot{x} - kx + f_{var} + F_{ext} = m\ddot{x}, \tag{11}$$

Ici F_{ext} est la force générée par les vibrations extérieures. Elle est égale à $-ma_{ext}$, où a_{ext} est l'accélération connue des vibrations extérieures. Cette équation est facilement adaptable aux différents types de structures mécaniques analysées.

Le système (10), (11) pour être complet ne nécessite plus qu'une relation, celle entre les grandeurs électriques. Celle-ci est fixée par le circuit qui est connecté aux bornes électriques du transducteur. Ainsi, le modèle du système "résonateur–transducteur" est présenté comme un dipôle électrique, prêt à être utilisé dans un modèle de type Spice.

[3]Depuis cette étude, la plate-forme SystemC-AMS a beaucoup évolué, et notre expérience n'est plus représentative de la réalité.

TABLE 3: Les caractéristiques principales de l'élévateur de tension et de l'interrupteur fabriqués : mesures versus simulation.

Caractéristique	**Mesuré**	**Simulé**
Gamme des tensions (V)	3−31	3−50
Résistance R_{dson} de l'interrupteur (Ω)	32−46	39
Puissance statique (nW) (selon la tension V_{store})	0.8−44.8	0.44−111.7
Énergie dynamique par un cycle on/off (nJ) (selon la tension V_{store})	0.065−1.38	0.05−2.92
Temps de l'élévation de tension (ns)	73	40
Durée max. de l'état "ON" sans régénération du niveau (s)	5.8	11.2

Le modèle VHDL-AMS est constitué par les 4 dernières équations écrites telles quelles. Une interface électrique est décrite selon les règles de syntaxe du langage, et présente une paire de terminaux électriques (modélisant une capacité variable) et un terminal recevant la fonction de l'accélération des vibrations externes [Galayko07].

Modélisation des blocs électroniques de commande

Une modélisation VHDL-AMS a été utilisée pour concevoir l'algorithme de commande pour le circuit de conditionnement adaptatif [Dudka09b]. En particulier, le VHDL-AMS a été utilisé lors du développement de l'algorithme d'autocalibration pour modéliser l'interrupteur, les blocs de mesures des tensions V_{res} et V_{store}, l'automate d'état et l'échelonnement des phases de conversion d'énergie et d'autocalibration. Ce modèle a été utilisé conjointement avec le modèle ELDO du circuit de Yen (Fig. 10) avec le transducteur/résonateur modélisé comme présenté dans les deux sous-paragraphes précédents.

De cette manière, le circuit de conditionnement auto-adaptatif a été modélisé au niveau fonctionnel, chaque bloc étant représenté par son macromodèle (par ex., l'interrupteur SW). Lors de la conception des circuits correspondant à ces blocs, les modèles comportementaux sont remplacés par les modèles ELDO des circuits correspondants, et testés dans le contexte global du système. Cette méthodologie de modélisation des REV s'est avérée très efficace, et donc, la modélisation est le principal outil de nos recherches sur les systèmes de récupération d'énergie.

Mesures et caractérisation des prototypes fabriqués

L'interrupteur/l'élévateur de tension

Un prototype de l'interrupteur/l'élévateur de tension réalisé a été caractérisé sur une large gamme des tensions (de 3 à 30 V) ; les résultats de mesures sont en bonne conformité de celles de simulation (Table 3), ce que confirme la fiabilité des modèles de AMS035HV.

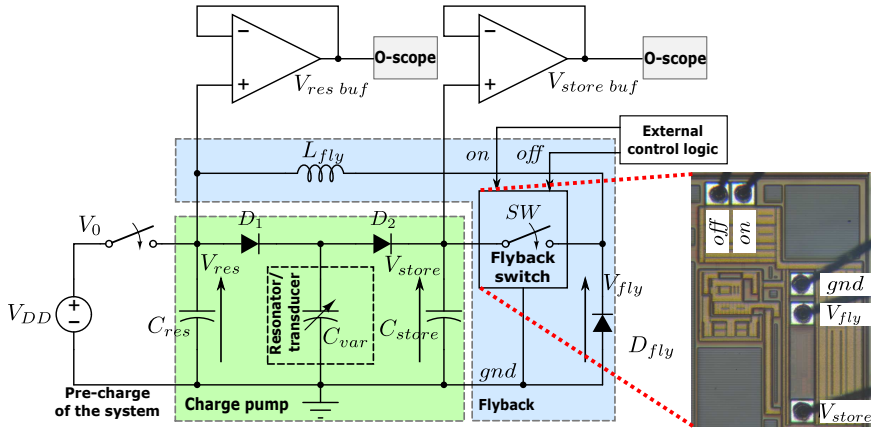


FIGURE 19: Schéma d'un REV étudié et micro-photographie du bloc de l'interrupteur/driver fabriqué.

Mesure du REV capacitive conditionné par le circuit de Yen

Le but des mesures est de tester le fonctionnement de REV capacitive dans le contexte de circuit de conditionnement de Yen avec l'utilisation de l'interrupteur/bloc pilote conçu et fabriqué. Procédé de conversion d'énergie est caractérisé par les charges accumulées sur le condensateur réservoir C_{res}, qui peut être visualisé par la mesure de la tension sur ce condensateur.

Le schéma de la configuration de test du système de REV est donnée sur la Fig. 19. Le circuit est initialement pre-chargé à basse tension $V_0 = 5.5$ avec une source de tension externe, qui a été connectée pendant un court instant à C_{res}. L'interrupteur de flyback, dont la micro-photographie est illustrée Fig. 19, est entraîné par la logique de contrôle externe qui génère une séquence des signaux à déclenchement périodique *on* et *off*. Des amplificateurs opérationnels à l'impédance d'entrée élevée et faible offset sont utilisés pour la mesure des tensions à travers C_{res} et C_{store}.

Le dispositif résonateur/transducteur MEMS utilisé dans les testes a été fabriqué et entièrement caractérisé à l'ESIEE Paris [Guillemet13]. La fréquence de résonance du résonateur est 162 Hz. Dans le mode de grande amplitude (1g d'accélération des vibrations externes), on a une bande passante à mi-puissance de plus de 30 % de la fréquence centrale. La capacité du transducteur varie entre 45 pF et 74 pF.

Lorsque la source externe de tension V_{DD} est déconnectée de C_{res}, le REV devient électriquement autonome, à l'exception de la source d'alimentation pour le circuit logique de commande externe (commande de l'interrupteur SW). Le résonateur mécanique est soumis à des vibrations externes stochastiques dont l'énergie est répartie dans la bande de fréquences 100-180 Hz.

Expérimentation.
Les testes décrits ci-dessus ont été répétés avec trois ensembles de l'amplitude de l'accélération et de la bande passante de vibrations. Pour la première, deuxième et troisième expérimentations, les paramètres de vibrations sont de $0.7 g_{rms}$@$100 - 180 Hz$, $0.8 g_{rms}$@$110 - 170 Hz$, et

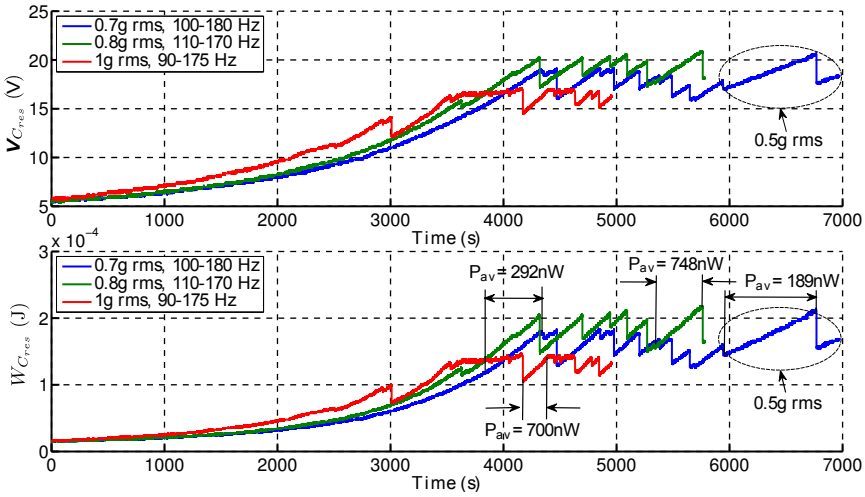


FIGURE 20: Évolution de l'état du système étudié en mode autonome soumis à des vibrations externes stochastiques avec trois stimuli différents. En haut : tension aux bornes de $C_{res} = 1\mu$F, en bas : énergie de C_{res}.

$1g_{rms}@90 - 175Hz$, respectivement. Tous les trois testes ont démarré avec V_0=5.5 V. La fréquence d'activation de l'interrupteur a été fixé à 5 Hz.

Fig. 20 présente l'évolution dans le temps de V_{res} (graphique du haut) et de l'énergie de C_{res} (graphique du bas). Après 3000-4000 secondes de fonctionnement de système autonome V_{res} monte jusqu'à 15-20 volts. Des chutes subites de V_{res} peuvent être observées. Cela se produit quand V_{res} atteint un niveau auquel un "pull-in" dynamique se produit. Les chutes de V_{res} sont dues au court-circuit entre les plaques de condensateur variable C_{var} : quand ça se passe C_{res} se décharge très vite à travers la diode D_1 jusqu'à moment où la tension au cours de laquelle le pull-in disparaît. Il s'agit d'un effet indésirable lié à la physique du dispositif MEMS présenté dans [Guillemet13]. La tension de pull-in dynamique dépend de l'amplitude de l'accélération des vibrations externes : à des amplitudes d'accélération inférieurs, la tension de pull-in est plus élevée. En conséquence, les niveaux plus élevés de V_{res} peuvent être obtenus à l'amplitude d'accélération inférieur, comme indiqué par la mesure. Le court-circuit "émule" une charge consommant l'énergie du condensateur de stockage, et on peut voir que la production d'énergie sur C_{res} est stable sur l'intervalle de temps observée (4000-7000s).

Au cours de trois testes, la tension maximale V_{res} produite est de 21 V, 21.5 V et 17 V, ce qui correspond à l'énergie sur C_{res} de 220 μJ, 230 μJ et 145 μJ, respectivement (à comparer avec l'énergie initiale de 15 μJ correspondant à $V_{res} = V_0$=5.5 V). Le taux de conversion d'énergie moyenne maximale (puissance) mesuré par la pente des segments droits de la courbe d'énergie est comprise entre 190 et 750 nW (cf. Fig. 20). Ces chiffres donnent les valeurs de l'énergie nette et la puissance disponible pour l'alimentation de la charge, y compris la consommation de l'interrupteur/driver, ainsi que les pertes dans les éléments réactifs et dans les diodes.

Conclusion et perspectives

La récupération de l'énergie des vibrations est un concept relativement nouveau qui peut être utilisé dans l'alimentation des dispositifs embarqués de puissance à micro-échelle avec l'énergie des vibrations omniprésentes dans l'environnement. Nos études sur les récupérateurs d'énergie vibratoire (REV) ont contribué au développement d'une vision moderne sur tels systèmes basés sur le principe de conversion d'énergie électrostatique (capacitive). Cette vision se résume en deux mots: "complexité" et "non-linéarité". La complexité de l'électronique et de la commande permettent d'obtenir le maximum des performances d'un transducteur/résonateur; nous considérons que jusqu'à récemment la voie de la complexité a été peu explorée par la communauté.

Les travaux sur l'analyse et l'optimisation de circuit de conditionnement pour les REVs capacitives ont abouti le développement d'un algorithme de conversion d'énergie optimale et adaptatif ; cette étude a été validée par la modélisation comportementale. Les travaux de conception électronique ont abouti l'implémentation d'un algorithme adaptative au niveau transistors et la réalisation et la fabrication d'un des bloc clefs (l'interrupteur/driver haute tension) en technologie CMOS AMS035HV. Enfin, en se servant d'un bloc fabriqué, la validation expérimentale des résultats obtenus par la théorie et par simulation a été faite.

Il a été conclu que la validation expérimentale de la théories est compliquée par une maîtrise insuffisante des paramètres des systèmes fabriqués par les procédés MEMS, ce qui fait que les systèmes réels sont différents des modèles utilisés pour la théorie. Les mesures précises de la dynamique d'un microsystème sont également problématiques, or la validation rigoureuse de la théorie exige une mesure exacte de la position de la masse mobile. Ceci est un point que nous envisageons d'aborder dans un futur proche, en coopération avec le groupe de recherche de Philippe Basset de l'ESIEE Paris.

La plupart des questions sur les REV capacitives restent ouvertes ; les axes de recherches possible que nous envisageons dans le futur proche sont résumés ci-dessous:
– *Élargissement de la bande fréquentielle des REVs.* Cette étude concerne des structures résonantes exploitant une non-linéarité.
– *Réalisation d'un prototype électronique de REV intelligent et adaptatif.*
– *Développement de l'analyse sophistiqué des REVs.* Cet axe concerne l'exploration théorique et le développement de l'analyse des REVs, l'étude des phénomènes dus à la complexité et à la non-linéarité prenant en compte le couplage mutuel électromécanique.

Chapter 1

Introduction

1.1 Overview

Energy is presented everywhere in the environment surrounding us - available in the form of thermal energy, light (solar) energy, wind energy, mechanical energy and many others. Throughout the history people used to derive benefit from different ambient energy sources so to apply them for their daily needs. Thus appeared windmills and waterwheels that date back to many hundreds and thousands years. Before the electricity era and before discovering of electrical energy sources (invention of batteries, Volta, 1799, dynamo machines, Faraday, 1831), energy harvesting was the only way to get any useful power. Hence, the concept of energy harvesting is not new. Except that the methodology and principles of converting energy evolve, as well as the number of potential energy sources has been growing up.

Today, the energy harvesting is considered with a new focus: generation of electrical supply for powering miniature devices, like those used in wearable electronics and wireless sensor networks. These devices need small amount of energy (up to milliwatts), however, there is a strong requirement on the size and reliability of the supply generation. The energy sources presenting a practical interest for microscale energy harvesting are: mechanical vibrations, thermal gradients, light (solar) and electromagnetic (RF). These energy sources are virtually unlimited and essentially free, if they can be captured at or near the system location.

This chapter presents a general overview of energy harvesting, including different sources and applications of use as well as various conversion techniques presently employed and documented in the literature. Furthermore, this chapter discusses reasons and motivations for our research in energy harvesting topic, specifically based on a mechanical vibration energy harvesting. Finally, our contribution to the existing study will be summarized.

1.2 Thesis outline

Chapter 1 introduces the problem of supply of autonomous systems and discusses the solution which can be provided by the energy harvesting techniques. The motivation for harvesting the mechanical vibration energy is discussed. The chapter describes different conversion methods and explains the need of associated conditioning electronics. The state of the art of electrostatic harvesting systems is presented and our contribution to the existing study completes this chapter.

1.3 Concept of energy harvesting

We start this chapter by defining the meaning of 'energy harvesting'. Fundamentally, **energy harvesting** (also known as **power harvesting** or **energy scavenging**) is the process of capturing energy from one or more of environmental energy sources, accumulating them and storing them for later use. Energy harvesting devices must efficiently capture, accumulate, store, condition and manage this energy, and supply it in a form compatible with the needs of the electrical load.

1.4 External energy sources and applications

Among numerous energy sources widely used for harvesting today are:

- **mechanical kinetic energy** (from sources such as vibration, mechanical stress and strain);
- **thermal energy** (waste energy from furnaces, heaters and friction sources);
- **light energy** (captured from sunlight or room light via photo sensors, photo diodes or solar panels);
- **electromagnetic energy** (from ambient RF waves);
- **natural energy** (from sources such as wind, water flow, ocean currents, and solar);
- **human body** (a combination of mechanical and thermal energy naturally generated from bio-organisms or through actions such as walking and sitting);
- **other energy** (from chemical and biological sources).

All of the above ambient energies are available for the electric energy generation for powering various appliances from **mega-watts** to **nano-watts** range, which are summarized below:

- **Mega-watt applications** comprise power supply in residential and industrial domains. Typical renewable sources suitable for these domains are hydraulic potential energy (by using the gravitational force of falling water [Warnick84]), solar energy (by using photo-voltaic panels [Hamakawa87, Prasad05]) and wind energy (by using wind turbines [Ackermann05]).
- **Milli-watt to micro-watt applications** involve low power applications such as calculators powered by solar cells [Roen77] and micro-solar power sensor networks [Taneja08], vibration powered wrist watches [Starner03], micromachined thermopiles [Wang07], shoe-mounted piezoelectric generators [Shenck01], vibration electromagnetic [Williams01] and electrostatic generators [Roundy02], etc.
- **Nano-watt applications** having size between molecular and microscopic dimensions are based on emerging nanotechnologies. Examples of energy harvesting in such applications are the piezoelectric nanowires [Gateway], photovoltaic cells based on nanometer-scale heterojunctions [Aydil06], carbon nanotubes [Aroudi13], noise harvesters for nanosensors [Neri11], etc.

Present study concerns the micro-watt power applications for the autonomy of the micro-scale devices.

1.4.1 Self-powered microsystems

Advancements in microelectronics technologies have increased power efficiency of microsystems by reducing power consumption requirements. At the same time, these progress resulted in growing interest in autonomous microsystems using environmental energy for self-supplying. The "ideal" applications are the microsized devices for monitoring and sensing operations with a requirement to operate in difficult-to-reach environments. Wireless communication ability of such devices allows a deployment of numerous distributed sensing nodes simultaneously. For example, such microsensors can be employed in monitoring environmental conditions like temperature, humidity, air pressure and Earth's crust fluctuations from remote or inaccessible areas [Barroca13], can diagnose from the inside the state of health of industrial machines (e.g. motors, turbines and pumps), cars and aircrafts [Benedettini09], electromagnetic interference shielding [Chung00] and large-scale structures like bridges [Caicedo01]. Furthermore, in bio-medical field, small implantable or wearable devices supervise essential vital functions of patients (e.g. intracranial pressure, blood pressure, heartbeats), diagnose and stimulate the functions of inner organs (heart pacemakers, defibrillators, etc.).

All of these examples have a common challenge of maintenance and battery replacement due to either their large distribution in a network, or microscopic size, or inaccessibility. For these reasons, ideally each microsensor node must be autonomous and self-powered from the environment, so to comply with the requirement of long lifetime.

The block diagram for the core of a typical wireless sensor node (WSN) is shown in Fig. 1.1. It is composed of a sensor, an analog-to-digital converter, a signal processing and storage unit, a transmitter and receiver, an antenna, as well as a power supply and

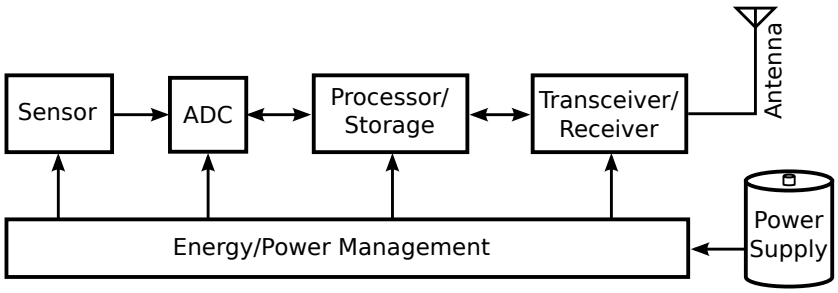


FIGURE 1.1: Block diagram of a wireless sensor node (WSN).

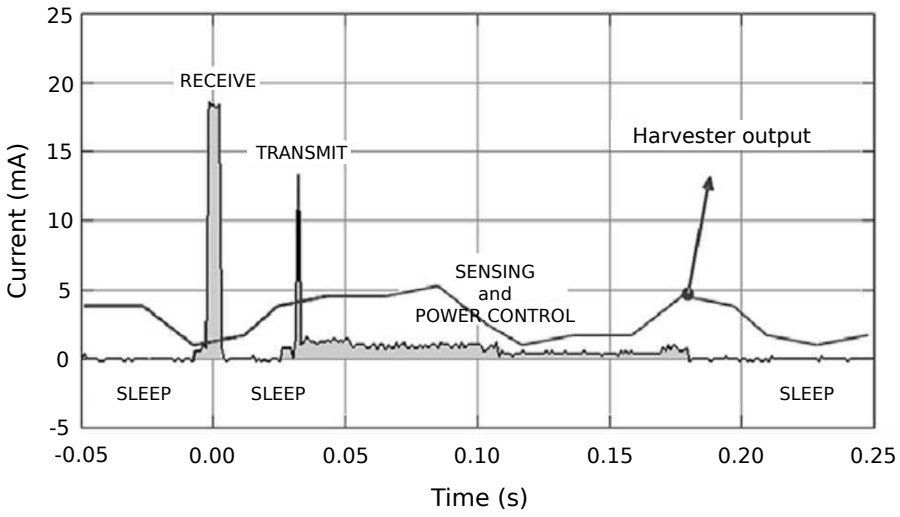


FIGURE 1.2: A typical scenario for the power consumption of a sensor node [Vullers09].

a energy/power management circuit. The system energy dissipation is usually dominated by sensing and wireless data transmission as shown in Fig 1.2. Fortunately, these operations occur rarely or/and periodically in response only to sporadic events or slowly changing variables like temperature or air pressure. As a result, most of the time the system operates in an idle mode consuming a tiny amount of energy (in nW – μW range), while the duty-cycle of power-hungry sensing and transmitting tasks (of mW order) last a short part of the entire period. The system's average power consumption is, thereby, relatively low, typically of μW order. Even though a smart timing management of high-power functions allows a reduction of the average power consumption of the node, the problem of attenuation of peak power consumption may exist. The energy may be extracted from the environment at slow rates, and therefore at low power level inadequate for high-peak power requirements. Moreover, ambient energy is naturally variable and often unpredictable, and might not be always available. This issue can be overcame by accumulating the harvested energy in a storage element for further supplying when needed.

TABLE 1.1: A comparison of energy sources according to [Rabaey00, Roundy03a, Stordeur97, Vullers09, Zelenay04]

Energy Source	Power Density	Energy Density
Fuel cells		4890 mWh/cm^3(methanol) 2700 mWh/cm^3(hydrogen)
Batteries (zinc-air)		1050–1560 mWh/cm^3
Batteries (rechargeable lithium)		300 mWh/cm^3(3–4 V)
Electrodynamic	1–200 mW/cm^3	
Solar (outdoors)	15 mW/cm^2 (direct sun) 0.15 mW/cm^2 (cloudy day)	
Solar (indoors)	0.006 mW/cm^2 (standard office desk) 0.57 mW/cm^2 ($< 60W$ desk lamp)	
Vibrations	0.01–0.1 mW/cm^3	
Thermal gradients	0.015 mW/cm^3 at 10 ^{o}C gradient	
RF	4e-4 mW/cm^2 (GSM station) 15e-6 mW/cm^2 (WiFi)	
Acoustic noise	9.6e-4 mW/cm^2 at 100 Db 3e-6 mW/cm^2 at 75 Db	
Passive human-powered systems	1.8 mW (shoe inserts)	

1.4.2 Ambient energy for autonomous microsystems

Authors in [Roundy03a, Rabaey00, Vullers09] analyzed the commonly used renewable energy sources. Most of them are listed in table 1.1. The table shows the comparison of various energy sources by power and energy densities. Values are estimates taken from literature, analysis and several experiments. The most suitable energy sources in terms of energy levels, sizes and feasibility of harvesting devices are : solar, thermal gradients, mechanical vibrations, fuel cells and RF.

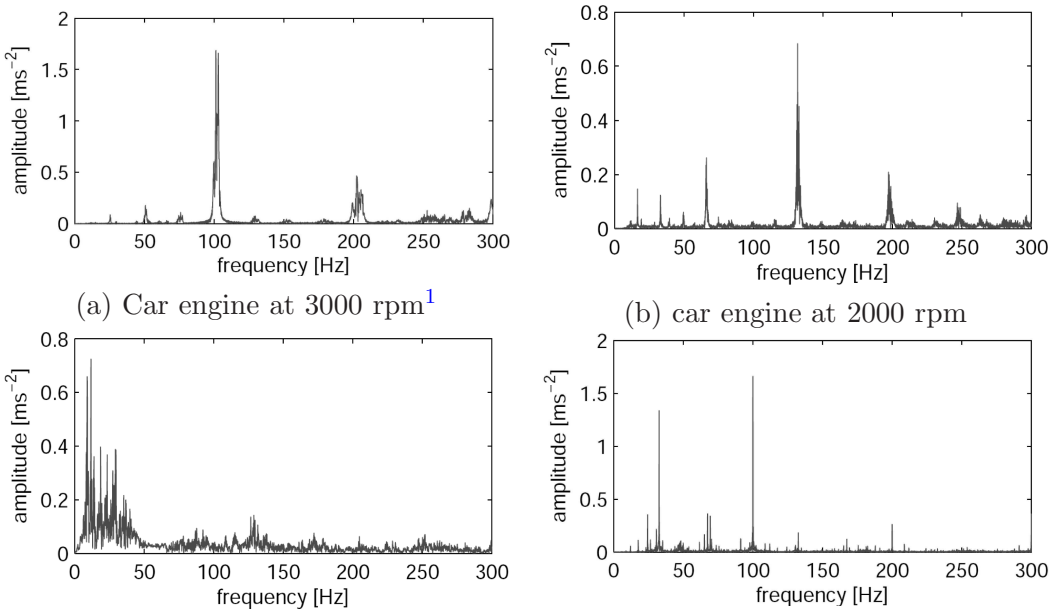
Solar cells are the most widely used and the most mature energy harvesting technology based on the principle of photovoltaic effect. A solar cell uses a PN junction for photovoltaic energy generation. Photons of light hit the depletion zone around the pn+ junction and separate electron-hole pairs within the depletion zone so to free carriers. Under the junction built-in electric field, free electrons and holes jump out from the depletion region so that electrons drift to the n+-side and holes to the p-side of the semiconductor material. Accumulated at the opposite sides of the semiconductor positive and negative charges develop an open-circuit voltage. If the load is connected across the cell, electrons travel through it from the n+-side to the p-side so to recombine with holes, generating the current that is directly proportional to the light intensity. Micro-scale systems employing thin silicon-based films have a significantly poorer efficiency

than macro-scale solar cells [Safa09]. Nevertheless, these microscopic solar cells harvest greater amounts of energy compared to other conversion energy mechanisms. Photovoltaic cells are very effective when a sufficient intensity of light is available (150–15000 $\mu W/cm^2$ in the daytime outdoor applications), however their yield slumps when the light rates are low (e.g. in the nighttime or in different indoors applications where the generated power density is 10 $\mu W/cm^2$ under the best case conditions [Roundy04a]).

Temperature gradients can be converted to electricity by thermoelectric generators that exploits the thermoelectric Seebeck effect. Thermoelectric generators usually consist of an n- and p-type thermoelectric materials electrically connected at the hot ends and disconnected at the cold ends, hence constituting a thermocouple [Toriyama01, Egbert07, Yang13]. The temperature difference occurring across a thermocouple results in the heat flow and, consequently, the charged carriers transporting from the hot end to the low temperature junctions. Concentration gradients of electrons and holes in the materials produces an electric field across n- and p-type materials, respectively. In this way each base electrode is ionized with an opposite charge and therefore a voltage difference is established. If connecting a load across each terminal, an electrical current is thermally induced [Wang08]. Thermoelectric power generators are effective when large thermal gradients are available, since the voltage produced by the generator is proportional to the temperature difference between the two junctions. In microsystems, however, significant temperature differences (greater 10 ^{o}C or 10 K) are unexpected and, as a result, power and voltage levels are relatively small. For instance, maximum 15 $\mu W/cm^3$ can be generated at 10 ^{o}C temperature gradient [Stordeur97].

Radio frequency energy is emitted by sources that generate strong electromagnetic fields such as wireless radio networks, cellular phone towers and TV signal. Power generators linked to a receiving antenna can capture this free flowing energy and convert it into usable electrical energy. RF power generators must operate close to the energy source, otherwise, the captured RF energy and produced voltage levels are extremely low. For instance, power densities in the range of 0.01-0.1 $\mu W/cm^2$ are likely when 25-100 m away from a GSM base station (for cell phones) [Vullers09]. However, in practice, it is not guaranteed that in the application of need an RF radiation source is situated nearby. Consequently, except specific application context, it is difficult to find the benefits of RF energy harvesting over other harvesting mechanisms of available ambient energy sources.

Fuel cells convert chemical energy into electrical energy on the same principle as batteries. Though conventional batteries employ reactions among metals and electrolytes whose chemical nature changes over time, the fuel cells actually consume their fuel such as hydrogen or methanol (a form of alcohol), leaving nothing but an empty reservoir. Fuel cells have high energy density (up to tens times that of lithium-ion batteries) and, hence, they are very attractive for long operation life applications. Fuel cells, on a large scale, have been recently deployed in numerous applications such as motor vehicles [Ehsani09]. Micro-sized fuel cells can be used in WSNs, in laptop computers and cell phones as for example is planed by Toshiba [Tos]. A challenge with fuel cells is the high temperature they must work at in order to obtain a high efficiency. For example, the best reactor in [Holladay02] is capable of 99 % conversion above 320 ^{o}C, however, at 270 ^{o}C conversion is less than 60 %.



(a) Car engine at 3000 rpm[1]

(b) car engine at 2000 rpm

(c) staircase with someone going down

(d) drill

FIGURE 1.3: Typical spectrum of ambient vibrations [Boisseau12]

Mechanical vibrations energy available in many environments and applications can be converted into electrical energy by means of several conversion mechanisms, including piezoelectric, electromagnetic and electrostatic, which are discussed in the next section. Table 1.2 gives results of measurements on various vibrations sources summarized in [Roundy03b]. Vibrations are presented in a relatively large spectrum as shown by a few examples in Fig. 1.3.

It is difficult to adequately compare ambient energy sources, because they have different nature, availability rates and potential energy levels. A common thing however is that all of them are application dependent. Indeed, RF energy harvesting may be possible only if a specific source is introduced, hence it is limited by a location. Fuel cells can not be hermetically sealed that makes them impossible to be used in implantable applications. The same limitation concerns the light or solar energy, due to the non-availability of the light in implantable applications or in the dark indoor or outdoor applications. Conversely, temperature variations are ubiquitous in the environment, but often they are not sufficiently large to generate practically usable voltages and power in micro-scale applications without placing thermocouple cells in series. Mechanical vibrations, however, present a more abundant, stable and relatively high energy source in a wide variety of environments and applications, such as automotive, aircraft, buildings, bridges, industrial tools, moving people, etc. Also, vibration energy harvesting has not been studied so long and so deep as for example photovoltaic cells, and therefore presents a big interest for the research. Mainly for these reasons ambient vibrations energy source has been chosen as a contest of our research project.

[1]Abbreviation rpm - revolutions per minute, is a measure of the frequency of a rotation. It annotates the number of turns completed in one minute around a fixed axis.

TABLE 1.2: Summary of several vibrations sources accordingly to [Roundy03b]

Vibration source	**Peak Acc.** (m/s^2)	**Freq.** (Hz)
Car engine compartment	12	200
Base of 3-axis machine tool	10	70
Kitchen blender casing	6.4	121
Clothes dryer	3.5	121
Door frame just as door closes	3	125
Small microwave oven	2.25	121
HVAC vents in office building	0.2-1.5	60
Wooden deck with foot traffic	1.3	385
Breadmaker	1.03	121
External windows (size 2 ft X 3 ft) next to a busy street	0.7	100
Notebook computer while CD is being read	0.6	75
Washing Machine	0.5	109
Second story floor of a wood frame office building	0.2	100
Refrigerator	0.1	240
Human motion	0.35	1-10

1.5 Mechanical vibration energy harvesting

Mechanical vibration energy harvesting concept consists in converting the energy of the parasitic ambient mechanical vibrations into the useful electrical energy. The study of this concept is a relatively new subject, comparing for example to the harvesting of photovoltaic energy. Scientific research on vibration energy harvesting for WSN applications began to take of on the edge of the 2000's with the growth of microelectromechanical systems (MEMS).

1.5.1 General system

As reported in numerous studies, harvesting of kinetic energy of external vibrations is achieved in two steps. At first, a part of the mechanical energy is captured by the mechanical part of the harvester - the internal movable parts. At a second stage, the captured kinetic energy of the movable parts is converted into an electrical form.

A general model of a Vibration Energy Harvester (VEH) is given in Fig. 1.4. The mechanical part is usually a mechanical resonator, which is composed of a proof mass coupled with external vibrations through an elastic link (e.g. spring). In the mechanical domain, there are two reference frames: the global inertial frame Oy, in which external vibrations take place with acceleration a_{ext}, and the reference frame Ox related to the vibrating system, in which the harvester is located. The relative motion of the Ox reference frame can be modeled by applying a force $-ma_{ext}$ to the resonator (m is a resonator's mass), and then, the Oy reference frame is considered as inertial [Landau76].

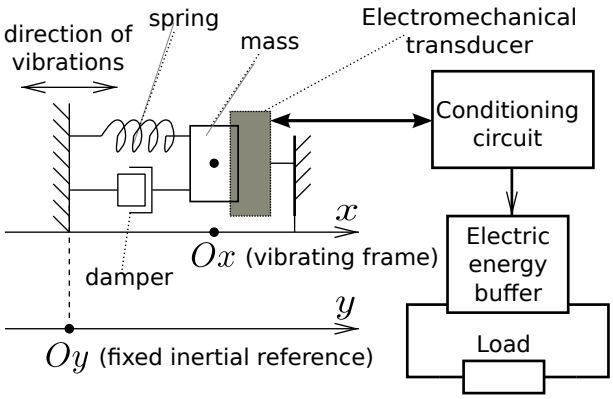


FIGURE 1.4: General structure of a vibration energy harvester

Thanks to the elastic coupling with the vibrating reference frame Ox, the mass moves in this reference system and the resonator accumulates kinetic energy.

To convert the mechanical energy into electrical, an electromechanical transducer should apply an electrically-originated damping force on the mass, i.e. it should perform a negative work on the mechanical system purposely reducing its kinetic energy.

The damping force can be created by a magnetic field, an electric field or a strain on a piezoelectric material. Depending on the nature of the damping force there exist electromagnetic, electrostatic and piezoelectric conversion techniques. Each technique offers different benefits and drawbacks as well as technical challenges that determine its viability and potential for the integration into self-powered microsystems. An associated conditioning circuit manages the electrical energy flow so as to create an electrical context for the desired operation of the electromechanical transducer. The architecture of the electronics depends upon the type of transducer. Furthermore, a conditioning circuit allows an accumulation the maximum of the harvested energy in the reservoir and a regulation of the output power for a load supply.

The design of a VEH requires the optimization of the mechanical part, the transducer and the conditioning electronics so to increase the efficiency of the whole VEH system. To fulfill this requirement, the mechanical resonator must capture as high kinetic energy as possible, the transducer has to convert the energy as efficiently as possible and the associated electronics to consume as low power as possible. Therefore, the design of vibration energy harvester is a complex task submitted to many restrictions and, hence, requiring a careful study and analysis of different issues. Vibration energy harvesting is a multidisciplinary topic that joins specialists from different research fields including micro-technologies and electronics as well as fundamental sciences such as physics and mathematics.

1.5.2 Mechanical resonator structure

The mass-spring mechanical structures can be either resonant or non-resonant. The resonant generators are intended for applications where the source amplitude is small compared to the possible proof mass displacement and are efficient in specific narrow

bands of frequencies. The non-resonant generators, instead, are used in applications where the external vibration power is spread in a large band at low frequencies and where the vibration amplitude is large compared to the allowable proof mass displacement, e.g. harvesting the energy from the human body movement for which the vibration spectrum is between 1 Hz to a few tens of Hz [Büren06, Bowers09].

For a given resonant structure, the maximum displacement of the movable part occurs when the excitation frequency equals its natural frequency. Tiny deviations from this frequency point would eventually result in significant reduction in displacement and output power. In real practical applications [Roundy03b, Despesse05, Najafi11], ambient vibrations are characterized by a large spectrum of frequencies between a few hertz and several hundreds hertz (cf. Fig. 1.3). Moreover, the observed *ambient vibrations are usually variable in time*. Due to the problem of frequency deviation, linear resonators with high quality factors are characterized by a high selectivity of frequencies (i.e. having very narrow bands) may fail to perform optimally in real environment and, hence, are not well suitable for practical applications.

In order to overcome this issue, recently abundant efforts have been devoted by the research community to widen the response bandwidth of resonant energy harvesters. To this end, the research of more complex coupling mechanisms introducing the mechanical non-linearities has been initiated. A number of different solutions have been presented in the literature. Thus, the resonators can employ the non-linear [Blystad10] or bi-stable springs [Cottone09]. Also a common approach is to use the non-linear double-mass systems [Galchev12]. These techniques allows a frequency conversion: the low-frequency poor quality factor Q resonator excites a high-frequency high Q resonator; the latter is used for the mechanical-to-electrical energy conversion. Another approaches consist in eventual impact of the mobile mass with a stopper [Soliman08, Guillemet13], employment of stochastic resonance, and others.

Drastically new approach for capturing nonregular low frequencies has been proposed by [Bu12] in his study of the "liquid" capacitive harvester. This harvester uses flowing liquid rather than conventional resonating structures to induce variable capacitance and it is more suitable for low frequencies (a few hertz) applications. As authors show, up to 2.19 mW of power can be produced at 1 Hz by a small-size device (4cm×1.5cm×1mm).

Another non-conventional capacitive harvester reported in [Naruse09] is a non-resonant low-frequency structure that consists of a mass-spring mechanism with microball bearings rolling with the separation gap control. The separated spring and mass manage to vibrate with long-range movement (about 15 mm) at low frequency and keep the separation gap constant. This concept makes the structure reliable to high mechanical stress and owing to a long-range movement, the resonator harvest up to 40 μW at very low vibration frequency and amplitude (2 Hz, 0.4 g).

An expression characterizing the maximum power P_{max} that can be extracted from the mechanical vibrations at the acceleration amplitude A_{ext} and the angular frequency ω, with a use of a VEH with a mass m, which maximum displacement is limited to X_{lim}, is shown next:

$$P_{max} = \frac{1}{2} m A_{ext} \omega X_{lim} \tag{1.1}$$

TABLE 1.3: Summary of several electrostatic MEMS micropower generators highlighting the maximal harvested mechanical power P_{max} according to Eq. 1.1

Reported in	Device dimensions	m, g	f_{res}, Hz	X_{lim}, μm	P_{max}, μW
[Roundy02]	1 cm^3	0.1	50	250	39
[Mitcheson03]	–	0.1	30	500	47
[Despesse05]	81 mm^2 x 0.4 mm	2	50	95	95
[Paracha09b]	11 x 6.5 x 0.86 mm^3	0.0461	250	50	18.1
[Suzuki10]	11.6 x 10.2 mm^2	0.1	63	70	13.8
[Guillemet13]	0.042 cm^3	0.066	163	46	15.5

This equation gives an absolute limit for the captured mechanical power by the mass-spring resonator independently of the mechanism of electromechanical energy conversion [Mitcheson08, Basset09]. Table 1.3 presents the maximum power estimation calculated with Eq. 1.1 for several micro-generators submitted to vibration acceleration $A_{ext} = 10\ m/s^{-2}$.

Here, f_{res} is the resonance frequency of the mechanical resonator. As can be observed, typical resonator can capture up to several tens microwatts of mechanical power when oscillating at resonance frequency at 1 g acceleration.

Study and design of the mechanical part of the VEH is out of focus of this thesis. Nevertheless, design and optimization of the electrical part of the VEH requires the knowledge of the mechanical part as well, and vice versa. Indeed, modeling of the complete VEH on system level must take into account the mechanical part. Therefore, a close interaction between designers of both mechanical and electrical parts of the system is required. For this reason, we worked in close collaboration with Philippe Basset and his team from ESIEE Paris (ESYCOM laboratory), who are specialized in microelectromechanical systems technology and design (MEMS). This team is responsible for the design and fabrication of the mechanical part and electromechanical interface (transducer).

Our study deals with two resonant capacitive VEH devices fabricated in ESIEE Paris [Basset09, Guillemet13], which are intended to operate at frequencies ranging from one to a few hundreds hertz.

Since almost two years, the team of Philippe Basset, in collaboration with the team of Luca Gammaitoni (univ. of Perugia, Italy), studies the nonlinear mechanical structures allowing to widen the vibration bandwidth and capture the colored noise vibrations (under stochastic resonance). Such nonlinear mechanical prototypes have an impact on the conditioning circuits and analysis methodology of the VEH system. The nonlinear analysis of electrostatic vibration energy harvesters dynamics in the coupled electromechanical mode is investigated by the team of Elena Blokhina from the University College Dublin and my supervisor Dimitri Galayko since 2011 [Galayko11a, Blokhina12].

1.5.3 Electromechanical energy transducers

1.5.3.1 Methods of electromechanical energy conversion

As we mentioned previously, there exist three basic methods used to convert the energy of mechanical vibrations to electricity, namely electromagnetic (EM), electrostatic (ES) and piezoelectric (PE).

An electromagnetic conversion occurs when a coil moves with relation to an external magnetic field, so that there is a variation of magnetic flux crossing the coil section. Typically, the coil is attached to a mobile mass oscillating in the magnetic field created by a stationary permanent magnet as shown in Fig. 1.5a. The variation of the magnetic flux results in inducing an AC voltage on the coil, according to Faraday's law. Conversely, the same conversion principle is applied to a fixed coil and a moving magnetic mass. A number of ED harvesters have been reported in literature, a few to mention: [Williams01, Amirtharajah98, Beeby07, Saha08, Sari10, Cheng07, Kulkarni06, Cao07].

An electrostatic harvester harnesses energy from the work performed by vibrations against the electrostatic force of a vibration-dependent variable capacitor C_{var}. Energy conversion is achieved as the capacitance of the charged capacitor decreases (the gap between the capacitors plates increases) as shown in Fig. 1.5b. Under charge constrained or voltage constrained conditions, the electricity is generated. Both of these techniques will be discussed in section 1.7. Numerous charge and voltage constrained capacitive harvesters have been presented during the last decade as reported in [Meninger01, Roundy02, Tashiro02, Miyazaki03, Mitcheson04, Torres05, Despesse05, Chiu06, Paracha07, Mitcheson08, Kuehne08, Suzuki10].

A piezoelectric harvester converts mechanical energy by straining a piezoelectric material. The deformation of a piezoelectric material causes charge separation across it, producing an electric field and, consequently, a voltage drop proportional to the applied stress. A piezoelectric transducer usually consists of a cantilever beam fixed on one end while a moving mass is attached on the opposite side as illustrated in Fig. 1.5c. A beam is built as a two-layer bimorph structure with two piezoelectric sheets separated by a dielectric shim. As the mobile mass resonates, one side of a cantilever is in tension and the other is in compression, creating an AC voltage. Examples of reported piezoelectric generators can be found in [Shenck01, Glynne-Jones01, Roundy04b, Ottman02, Jeon05, Marzencki05, Sodano05, Shen08, Defosseux11].

1.5.3.2 Comparison of conversion methods

Each type of transducer presents both advantages and drawbacks depending on the application (amplitudes of vibrations, frequencies, etc.). An excellent state of the art of various types of transducers as well as their comparison is provided in a study [Beeby06]. A qualitative comparison of these techniques in terms of power densities, operation conditions, integration potential and so on, is summarized in Table 1.4.

Electromagnetic harvesters have a good power density and do not require a complex power conditioning. However, a fundamental weakness of such transducers is that they

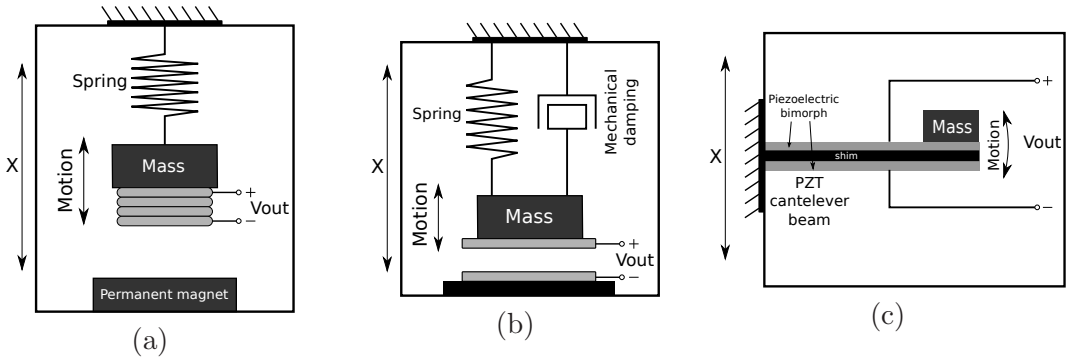


FIGURE 1.5: Commonly employed electromechanical energy transducers: (a) electromagnetic, (b) electrostatic, (c) piezoelectric.

TABLE 1.4: Comparison characteristics of vibration energy harvesting techniques - electromagnetic (EM), electrostatic (ES) and piezoelectric (PE).

	Advantages	**Drawbacks**	**Microsystem Implementation Challenges**
EM	-Robustness	-Low output voltage	-Difficult integration of bulky magnet
	-High output current	-Low efficiency at low frequencies and small sizes	-Possible need of additional transformer
	-No initial energy required -Simple concept		
ES	-Scalable -CMOS compatible	-Need of energy investment -Complex power conditioning	-Possible mechanical instability
	-High output voltages	-High impact of parasitic capacities	
	-High coupling		
PE	-High output voltage and power	-Power conditioning	-Difficult integration of PZT material
	-No initial energy required	-Voltage rectification	-Reduced coupling of of thin-films
	-No need to control any gap	-Fatigue of PZT beams	

are not suitable for miniaturization and are not compatible with CMOS process, because they possess high-volume coils and magnets.

Nowadays breakthrough in studying piezoelectric transducers offers a relatively high output electrical power yield of order of tens-hundreds micro-watts. Also, the piezoelectric transducer may be integrated on chip with built-in electronics; such a system is known as ICP "Integrated Circuit Piezoelectric". Another positive side of piezoelectric transducers is that they do not need of extra energy source for starting. However, a high piezoelectric harvesting efficiency is often obtained with resonant structures, and is limited to a narrow frequency band. Different nonlinear techniques of frequency up-conversion are also widely used for overcome the limitation imposed by resonating and

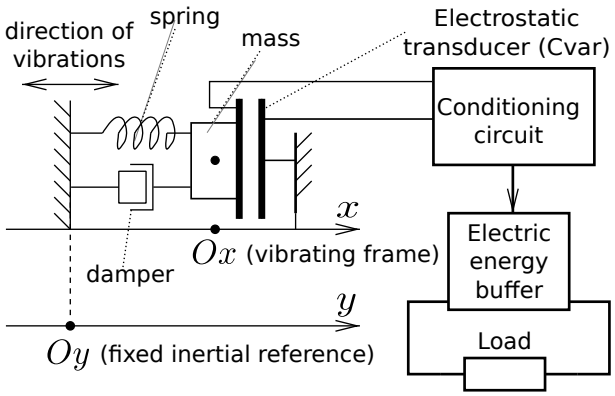


FIGURE 1.6: General structure of an electrostatic vibration energy harvester (e-VEH)

rather high-frequency piezoelectric structures [Kulah08]. These techniques often use permanent magnets, which adds bulk and cost, and prohibit some class of applications (in particular, the medical embedded self-powered devices). Another serious issue related with piezoelectric transducer concerns the lifetime: since in the energy harvesting applications the piezolayer strain should be high, there is a risk of material degradation (fatigue, depolarization, micro-"fissure" [Pillatsch13]). Few work have indicated these issues; further in-depth studies are required to evaluate the reality of this limited lifetime issue.

Electrostatic transducers commonly employ a silicon micromachined MEMS technology, whose fabrication process is similar to those of a standard CMOS. Therefore, because of the process compatibility, it is easier to integrate electrostatic transducers based on mature MEMS technology than either electromagnetic or piezoelectric converters. Although the power levels offered by electrostatic transducers are not high (max. few tens of microwatts), and although electrostatic transducers need an initial electrical biasing, capacitive harvesters are seen as one of the most promising energy generators for future miniaturized autonomous embedded systems. Comparing with piezoelectric transducers, they don't have lifetime issues related with piezoelectric transducers, and they can generate high voltages while having very small size.

1.6 Electrostatic energy harvester

This work deals with electrostatic (or capacitive) transducers. An electrostatic transducer is a capacitor whose plates move relatively to one another. Fig. 1.6 demonstrates the system of electrostatic vibration energy harvester (e-VEH), in which the capacitive transducer is used to transfer the mechanical energy to the electrical domain. For that, the mobile mass of the mechanical resonator is associated with a movable electrode that makes C_{var} vary with the motion of the mass. In other words, the variation of the capacitance is related with the kinetic energy stored by the moving mass.

As was mentioned before, the electrostatic transducer may be directly implemented on chip together with a conditioning electronics. The miniature silicon-based design of a variable capacitor is possible owing to the microelectromechanical systems (MEMS)

technologies which nowadays are mature, such as deep reactive ion etching (DRIE) [Madou02].

1.6.1 Variable capacitor structures

Capacitive transducer is a two-terminal device. The first terminal is attached to the mobile proof-mass. The second electrode is fixed to the vibrating frame linked to the (non-inertial) reference system Ox. Hence the transducer capacitance varies in response to the motion of the mobile mass in the frame Ox. There exist various types of capacitive transducers, differing by the geometries and by the law of the capacitance variation. The displacement of the capacitor's movable plate may occur in plane on the substrate (in the plane parallel to the substrate) or out of plane (in a direction normal to the substrate). For both topologies the capacitance may change by varying the gap between the electrodes or by varying the overlap area of the electrodes.

The Out-of-Plane Gap-closing Plate (OPGP) capacitor as well as the In-Plane Overlap Plates (IPOP) capacitor, shown in Fig. 1.7a-b, suffer from the problem of possible contact of top and bottom electrodes resulting in an electrode stiction, which could cause the collapse of the system and destroy the device due to elevated short-circuit currents. The capacitor plates for in-plane motion are typically fabricated with interdigitated fingers in a comb structure. An In-Plane Overlap Comb (IPOC) structure (cf. Fig. 1.7c) is able to provide a greater mobile mass displacements while achieving a higher capacitance variation and minimizing the minimal capacitance, however it suffers from stability problems. Variation of the gap distance in the In-Plane Gap-closing Comb (IPGC) structure (cf. Fig. 1.7d), alternatively, ensures better stability owing to smaller spring deflections and larger both minimal and maximal capacitance values [Roundy04b].

Regardless on the structure of the MEMS device, the plates of the variable capacitor have parasitic series resistance and parasitic capacitances between the moving plates, the substrate and sidewalls. The parasitic capacitance set a lower bound on the minimal transducer capacitance, so reducing the ratio C_{max}/C_{min}, which determines the transducer efficiency in the energy conversion process [Roundy03b]. Therefore, engineers designing the transducer variable capacitor must take into account these factors and must found the trade-off between the capacitance variation, minimal capacitance and parasitic components, as well as the mechanical stability of the structure.

Capacitive transducers can be divided into two categories:

- **Electret-free** converters, which use conversion cycles made of charging and discharging of the capacitor, and therefore requiring an active electronic circuit to apply the charge/discharge cycle on the structure. The electronics must be synchronized with the capacitive variation.
- **Electret-based** converters, which use electrets giving them the ability to directly convert mechanical power into electricity.

The electret-free devices are passive structures that require an energy cycle to convert mechanical energy into electricity. Electret-based devices are similar to electret-free

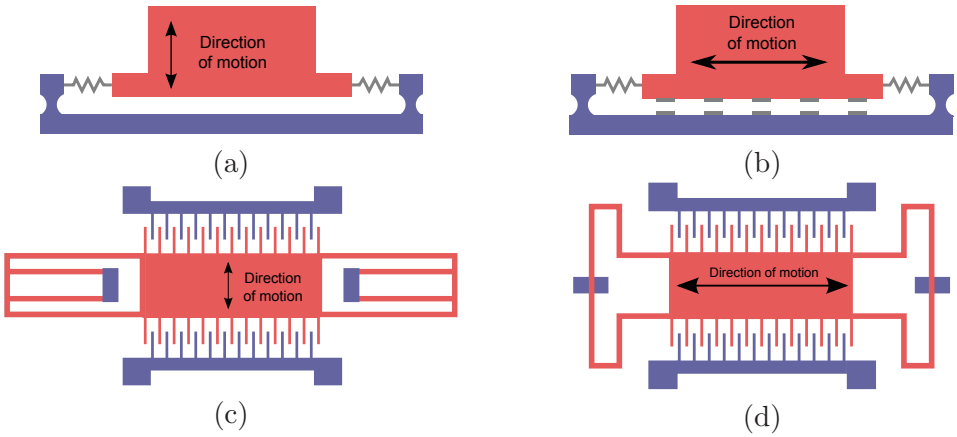


FIGURE 1.7: Typical structures of electrostatic transducer using MEMS process: (a) Out-of-Plane Gap-closing Plate (OPGP), (b) In-Plane Overlap Plates (IPOP), (c) In-Plane Overlap Comb (IPOC), (d) In-Plane Gap-closing Comb (IPGC).

converters, the difference is in an electret level added on one or two plates of the variable capacitor. The electret creates a variable polarization of the electrode, so generating a current providing electrical power for the load. So, such devices enable straightforward mechanical-to-electrical conversion. This PhD study project is focused on electret-free converters for several reasons, mainly because such a category is more interesting in terms of research. An extensive review of the state of the art of electrostatic VEHs devices was presented in PhD thesis of R. Guillemet [Guillemet12].

1.6.2 Conversion principle of electret-free structure

For the simplicity, consider a simple rectangular parallel plate capacitor, given by $C_{var} = \varepsilon_0 S/d$, where ε_0 is the dielectric constant, S - the overlap area of the plates, d - the gap distance between the plates. Depending on structure of the capacitive transducer demonstrated in previous subsection, the decrease of the capacitance can occur either by increasing d, or by reducing S. For example, in the case when the capacitance varies due to the change of the gap distance between the plates ($d = d_0 \pm x$)), the minimum and maximum of the capacitance depends on the amplitude of the displacement of the electrodes:

$$C_{max,min} = \varepsilon \frac{S}{d_0 - X_0 \pm X_1}, \tag{1.2}$$

where X_0 is an eventual average position of the mobile mass, X_1 is the amplitude of the mobile mass displacement, d_0 is the initial gap of the transducer, at zero displacement. Parameters X_0 and X_1 depend on the parameters of external vibrations (amplitude and frequency), which in turn are subjected to variations.

As we mentioned, electret-free converters require a specific charge-discharge cycle. Various types of cycles enable the energy conversion with a capacitive transducer, but the most commonly-used are charge- and voltage-constrained cycles as shown in Fig. 1.8. They both start when the capacitance is maximal (point A). At this point, a charge Q_0 is injected into the capacitor polarizing it thanks to an external source.

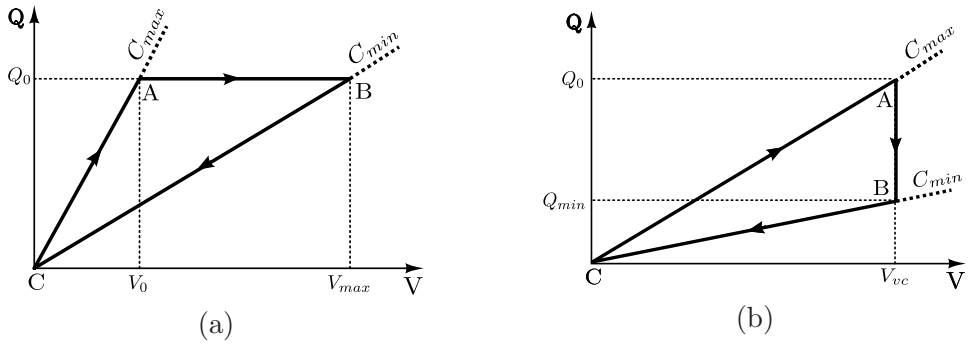


FIGURE 1.8: QV-cycles of electromechanical energy conversion: (a) charge constrained and (b) voltage constrained.

In case of the charge constrained cycle, the energy conversion is initiated as the capacitance decreases so that it remains charged with the same amount of charges Q_0 (Fig. 1.8a). As C_{var} decreases, voltage across it increases so to satisfy $Q = CV$. When C_{var} reaches the minimal value and the voltage becomes maximum V_{max} (point B), the full charge is returned to the reservoir capacitor until the voltage across capacitance becomes zero (point C). The following cycle starts when the the capacitance is pre-charged again with Q_0 to the initial voltage V_0. The converted energy is equal to the surface area of the triangular that can be numerically expressed as:

$$\begin{aligned} \Delta W_{Q\ const} &= \frac{1}{2}(C_{max} - C_{min})V_0 V_{max} = \\ = \frac{1}{2}V_{max}^2 \frac{C_{min}}{C_{max}}(C_{max} - C_{min}) &= \frac{1}{2}V_0^2 C_{max}(\frac{C_{max}}{C_{min}} - 1) \end{aligned} \tag{1.3}$$

In case of the voltage constrained cycle, the energy conversion also starts at the maximum capacitance value (point A in Fig. 1.8b). At this point, the transducer is electrically connected to a constant voltage source V_{vc}. Since the voltage V_{vc} is kept constant and the capacitance decreases, the charge decreases as well, so generating the current which recharge the voltage source with the energy converted from the mechanical domain. When the capacitance reaches its minimum (point B), the remaining charge Q_{min} is completely collected and stored (point C). The following cycle starts when the capacitance is again maximum, and so on. The amount of energy converted at each cycle also corresponds to the area of the triangular:

$$\Delta W_{V\ const} = \frac{1}{2}(C_{max} - C_{min})V_{vc}^2 = \frac{1}{2}(\frac{C_{max}}{C_{min}} - 1)C_{min}V_{vc}^2 \tag{1.4}$$

The comparison of the voltage constraint and the charge constraint cycles can be done if some hypotheses about the available voltage sources are made. If for two schemes the same constant voltage source is available, so that $V_0 = V_{vc}$, obviously the charge constrained cycle provides C_{max}/C_{min} times more energy. By contrast, is the *maximal* voltage is equally limited in the both schemes, for example, for technological limits, $V_{max} = V_{vc}$ and the voltage constrained cycle provides C_{max}/C_{min} times more energy.

Precise implementation of the both cycles is difficult, because of the need of precise synchronization between the charge flow on the transducer and the transducer capacity variations. The conditioning circuits implementing such a variable biasing are discussed in the next section.

1.7 Energy interface conditioning circuits

1.7.1 Needs for energy conditioning

Conditioning electronic circuits are the key elements in energy harvesting systems since they determine the efficiency of the electrical energy generation from the ambient energy, whatever the energy source is. Their role is to assist the energy conversion process and to provide a stable constant DC voltage for the load supply. According to this role, the conditioning circuits are usually divided in two functional parts: interface for the transducer conditioning assisting the energy conversion process and the load interface together with the power management blocks.

Depending on a type of the transducer, functions and topologies of the transducer interface are different. Thus, electromagnetic generators use relatively simple interface circuits achieving a rectification and regulation of a considerably low AC voltage [Beeby07, Rao13]. Piezoelectric generators require the interface circuits for the similar reasons: rectification the generated AC voltage and its regulation according to the load specifications [Sodano04, Lefeuvre06, Miller12]. Note that the voltage amplitude produced by a piezoelectric generator depends on several factors such as the mechanical vibration parameters, characteristics of the piezoelectric element and its dimensions, etc. Therefore, the output voltage must be either increased, or reduced. Electrostatic transducers, in turn, require the adaptation interface circuits to control the charging and discharging events of the transducer capacitance and to manage the converted energy in the optimal way [Mur-Miranda04, Torres06, Mitcheson10].

The power management interfaces are used to merge the energy converted from different sources [Christmann10] and to adapt it to the load needs using switched mode dc-dc converters. For the optimum load resistance matching, typically buck [Kim07], boost [Paing08], buck-boost [Kong10] and flyback [Kasyap02] switching converter topologies are employed. Also, a self-adjustable topology can be used based on charge pump [Maurath08].

Studies [Sodano04, Szarka12] provide a literature review of power conditioning circuits for VEHs, grouping different concepts according to functionality, complexity and efficiency. Although this review examines the circuits assisting only the piezoelectric and electromagnetic transducers (i.e. focusing on various rectification techniques and voltage step-up/down converters), it also states on existing solutions of general issues inherent to all types of generators: start-up, optimum load resistance matching and power management techniques.

As can be seen, designing of conditioning electronics for the VEH is a complex task that requires a wide knowledge in analog and power electronics, but also knowledge in

transducers and storage elements. Furthermore, the conditioning circuits are subjected to several strict limitations as discussed in the following section.

1.7.2 Requirements for conditioning electronics

Taking into account the unpredictability of ambient vibrations and usually the low levels of available energy, conditioning circuits should have adaptive and self-starting properties. Indeed, if for example, the ambient energy is temporarily very low so that the harvester consumes more than it converts, it is desired to turn the harvester into the idle mode for this period. Otherwise, it would consume all the accumulated energy including the energy needed for a start-up. Therefore, at microscale, power conditioning electronics design requires trade-offs different from those for high power applications, where the power overhead of the control electronics is less significant.

The size and volume of the overall system should be minimized, as the VEH will be used in embedded applications. Therefore, the conditioning circuits of the final VEH systems should integrate as much blocks as possible on a single chip.

1.7.3 State of the art of conditioning circuits for e-VEH

The interest of the community in designing the conditioning electronics for the capacitive transducers started to grow in the beginning of 2000th with the development of mature MEMS technologies and progress in CMOS technologies that shrank enough in size and power. The following subsections present the reported conditioning circuits for the capacitive transducers that we have examined in order to select one as a base of our research.

1.7.3.1 Primitive continuous conditioning circuit

The primitive circuit consists of a large pre-charged reservoir capacitor C_{res}, a much smaller transducer variable capacitor C_{var} and a load resistance (Fig. 1.9, [Basset09]). When C_{var} varies, the charge flux occurs between C_{res} and C_{var}, and its intensity depends on the resistance value. The current through resistance dissipates energy, which in turn is replenished by the mechanical energy extracted by the variation of C_{var}.

The functioning of this circuit is based on the hypothesis that the sum of charges of C_{res} and C_{var} is constant in time. In other words, we suppose that that there is no leakage on these capacitors, that is obviously not realistic. Hence, this circuit does not present the application interest.

Two secondary drawbacks of the circuit are the following. First, this circuit is unable to increase the the pre-charge voltage of C_{res}. It is known that capacitive transducers often need high polarization voltages to be efficient (tens of volts), while the initially available voltages are usually low (a few volts). This architecture does not contain the mechanism allowing augmentation of the polarization voltage from a low initial level. The second drawback is the AC voltage supplying the load. By consequence, a rectification is needed.

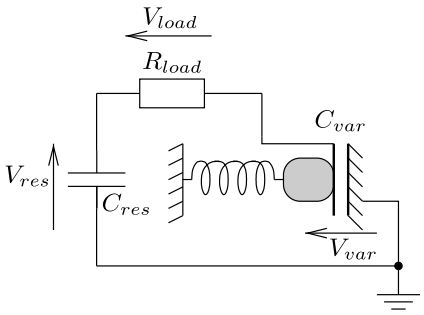


FIGURE 1.9: Primitive conditioning circuit [Basset09].

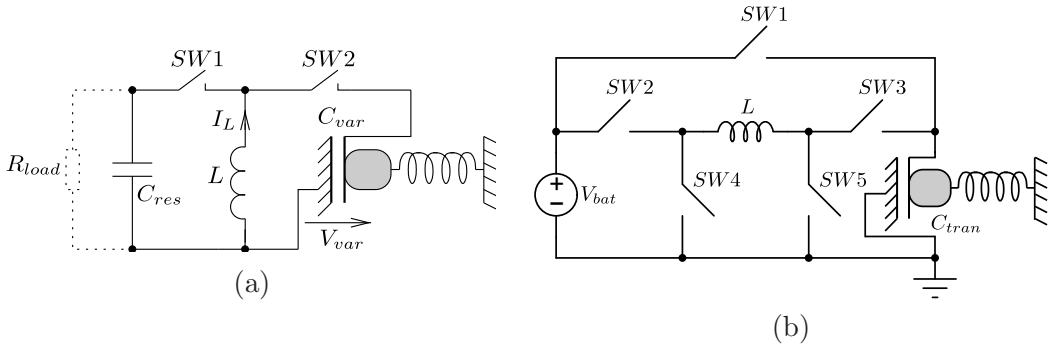


FIGURE 1.10: (a) Charge-constrained conditioning circuit [Meninger01]; (b) Voltage-constrained conditioning circuit [Torres06].

Nevertheless, this circuit can be useful in laboratory tests, for example in characterization of the fabricated transducers. Thus, C_{res} can be replaced by a DC voltage source. Such a technique has been used for measuring the capacitance of the transducer device fabricated in ESIEE Paris (cf. section 4.5.1).

1.7.3.2 Charge constrained circuit

In the charge constrained circuit shown in Fig. 1.10a, a transducer capacitor C_{var} is charged from the pre-charged C_{res} to some initial voltage V_0 when C_{var} capacitance is maximal. The energy transfer uses an inductor as an intermediate energy buffer and two switches. The time for energy transfer is negligible with respect to a C_{var} variation cycle. Then, two switches are open and C_{var} decreases keeping the charge constant (cf. the QV-diagram in Fig. 1.8a). When C_{var} is minimal, the conditioning circuit provides an inverse charge flow (and energy) from C_{var} to C_{res}.

This circuit requires a precise gate clocking of the switches $SW1$ and $SW2$; in fact during one cycle, switches are commutated two times each at exact moments (at C_{var}=C_{max} and C_{var}=C_{min}).

This circuit and its slight modifications are the best studied by the e-VEH designers community. To our knowledge, there exist two complete realizations of it. The oldest

one is realized in MIT in 2001 by S. Meninger [Meninger01]. Another one, implemented with a transformer rather than inductance, is realized by Despesse et al. [Despesse05].

1.7.3.3 Voltage constrained circuit

A simple voltage constrained circuit [Torres06] is shown in Fig. 1.10b. The system employs the battery instead of capacitor C_{res}; this allows recharge the battery The operation of the circuit is described by the QV-diagram in Fig. 1.8b. During the pre-charge condition, $SW2$ and $SW5$ are switched on to store energy in the inductor L. Switches $SW3$ and $SW4$ are turned on by simultaneously turning off $SW2$ and $SW5$ to charge C_{var}. The unidirectional switch $SW1$ is turned on to allow the current to flow from C_{var} to the battery. When the variable capacitor has reached its minimum value, $SW1$ is turned off. In order to completely recover the charge across the variable capacitor, reverse switching sequence of the pre-charge condition is used.

The physical IC realization of this circuit including the control of the switches has been presented in [Torres10].

1.7.3.4 Charge pump circuit

The charge pump employment in energy conditioning circuit was initially proposed by S. Roundy [Roundy02]. This solution eliminates the problem of the control of the charge flow onto and from the variable capacitor. The switches are replaced by the diodes that allow a uni-directional charge flow.

When C_{var} is at C_{max}, diode D_1 is on, and charges are transferred from C_{res} to C_{var}. When the capacitance decreases, both diodes are blocked. Since C_{var} is electrically isolated, its charge is constant and the decrease of the capacitance results in the increase of its voltage. When C_{var} is at C_{min}, diode D_2 is forward biased and the "energized" charges from C_{var} are "pumped" to a small storage capacitor C_{store}, which is larger than C_{var} but much smaller than C_{res}. The mechanical vibrations have done a work on the transducer capacitor causing an increase in the total energy stored in the system that corresponds to the increase of the voltage on C_{store} with respect to C_{res}. A more detailed description of the charge pump will be given in section 2.3.

After several charge pump cycles the storage capacitor eventually saturates that means that it can not receive charges from C_{res}. Subsequently, some method of returning a portion of the charge from C_{store} to C_{res} should be employed.

1.7.3.5 Charge pump with resistive return

This is the simplest return circuit which can be implemented: a load resistance is connected between C_{res} and C_{store} (cf. Fig. 1.12a). In this way, there are two flows of charges: one from C_{res} to C_{store} pushed by the charge pump, and another in the opposite direction through the resistance pushed by the potential difference $V_{store} - V_{res}$.

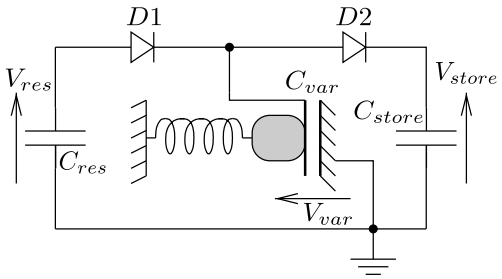


FIGURE 1.11: Charge pump with automatic switches (diodes) used for electromechanical energy conversion [Roundy02].

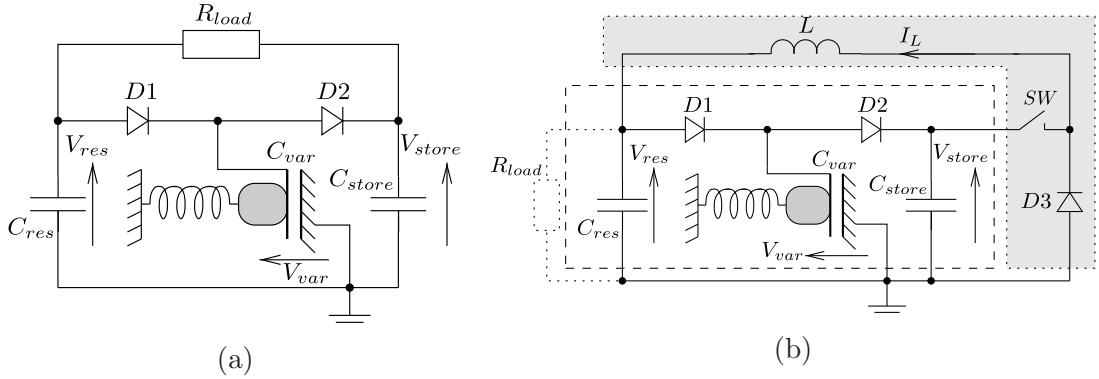


FIGURE 1.12: Charge pump with a return circuit: (a) resistive; (b) inductive flyback [Yen06].

A rigorous analysis of this circuit is difficult: since there is a continuous charge current between V_{res} and V_{store}, and the diodes make the circuit time variable, the exact mathematical model is rather complex.

However, the following hypothesis provides analytical results in good agreement with the simulation and the experiment. In particular, it allows a prediction of the level of the steady-state average value of V_{store} voltage and on the converted energy given the parameters of the circuit. Also, the value of resistance providing the maximal power conversion can be found.

We can consider that the charge pump and the resistance act independently on the capacitive network $C_{res}C_{store}$. It means that the two charge flows can be considered independently, and the steady-state circuit operation is obtained when the two charge flows are equal. Equivalently, instead of the charge flow, the energy flow can be considered: the energy produced by the charge pump is equal to the energy dissipated by the load resistance. It is reasonable to suppose that under such conditions, V_{store} is approximately constant in the steady state operation.

The calculation of the parameters of the circuit operation can be done with a very simple relation between the resistance value, the *average steady-state* value of the voltage V_{store} and the energy $\Delta W(V_{store})$ converted in one cycle by a stand alone charge pump with

the C_{store} capacitor charged to V_{store}:

$$\Delta W(V_{store}) = \frac{(V_{store\ ss} - V_{res})^2}{R_L} T, \tag{1.5}$$

where T is the duration of a vibration cycle (period).

The optimal value of the load resistance can be obtained as a left side of the last equation equals to ΔW_{max} calculated for the a stand-alone charge pump:

$$R_{opt} = \frac{(V_{store\ opt} - V_{res})^2}{\Delta W_{max}} T \tag{1.6}$$

where $V_{store\ opt}$ is the optimal C_{store} voltage at which the charge pump converts the maximal energy.

The calculation of ΔW_{max}, $\Delta W(V_{store})$ and $V_{store\ opt}$ for a stand-alone charge pump will be done in the following chapters.

Although such a conditioning circuit is very simple, it has several drawbacks:

- The load is not connected to the ground,
- If the ratio C_{max}/C_{min} is high, the load voltage can be high. Also, the load voltage depends strongly on the operation conditions of the circuit, and is not stable.
- The energy can't be accumulated during the circuit operation, and hence the pre-charge of C_{res} can't be increased.
- In presence of leakage on the capacitors, the system looses electrical charges and becomes inactive. Since there is always leakage in real system, such a conditioning circuit is not suitable for real applications.

In this way, a resistive return circuit is only suitable for laboratory experiments for the characterization and study of the charge pumps. In particular, this circuit was used in works [Florentino11, Guillemet13].

1.7.3.6 Charge pump with inductive flyback return

The return circuit proposed in MIT in 2006 by Yen [Yen06] is based on an inductive BUCK DC-DC converter topology (cf. 1.12b). The detailed description of this circuit is given in section 2.4.

The flyback return has several advantages.

- *Accumulation of the converted energy.* As the load is not connected, the converted energy is accumulated on C_{res}. This makes possible an increase of the voltage V_{res} while starting at low pre-charge level.

- *Unique swicth operating rarely and not requiring the synchronization with C_{var}.* The switch turns on once per many charge pump cycles. Therefore, the control of the switch will be performed at significantly reduced frequencies relatively to the circuit of Fig. 1.10 [Meninger01, Torres10].
- *The commutation of the switch will be done in a function of the voltage on C_{store}.* It is much easier to control the voltage, rather than the capacitance value or a mechanical quantity.

For these reasons, we have chosen the Yen circuit as a base of our theoretical study and practical design of the e-VEH with an intelligent control.

1.7.4 Discussion

We presented a summarized review of the basic conditioning circuits used for capacitive harvesters. For practical realization we chosen the charge pump circuit with the flyback return, since it has the advantage of potentially reduced complexity and power consumption and it allows a high voltage operation enabling the high converted energy. This circuit, in our opinion, is one of the best candidates for future designs when the operation voltage limitations of MEMS devices and CMOS technologies will reduce. As shows our work, this circuit is also compatible with stochastic input vibrations (cf. sec. 4.5.2.5).

Mitcheson et al. [Mitcheson12] reported on the effectiveness of the charge- and voltage-constrained electrostatic VEHs when coupled with interface circuits. It was concluded that the voltage constrained circuits promise higher efficiency than the charge-constrained circuits (80 % against 30 % of the maximal efficiency). The study uses the models of the power MOSFET devices (Vishay PowerPAK). However, this study does not take into account the energy necessary for the control of the circuit, whose complexity risks to be greater than for its charge-constrained counterpart. This can considerably reduce the high efficiency.

Several studies concerning the adaptive behavior of conditioning circuit have been published. Particularly, the work [Kempitiya13] reports on a complete system of the e-VEH including a capacitive transducer (of macroscopic size) and an integrated circuit in AMI 0.7 μm high-voltage technology realizing an intelligent energy conditioning of the Yen architecture. It was demonstrated a net power of 1 μW generated at the load at a vibration frequency 98 Hz.

1.8 Conclusion and our contribution

In this chapter we introduced the energy harvesting concept, the ambient energy sources and typical applications for energy harvesting. We also presented the harvesting principles of kinetic energy of ambient vibrations, focusing on the existing energy conversion methods using capacitive transducers. Finally, we discussed the needs of the converted

energy conditioning and presented the state of the art study of the interface conditioning circuits assisting the capacitive converters.

This thesis is a part of the research project ANR SESAM, regrouping four partners (LIP6, ESIEE Paris, TIMA[2] and CEA-LETI). The objective of this project is the development of an ambient energy harvesting and power management microsystem that must be adaptive, reconfigurable and robust. This impose to use multiple energy sources taking into account the fluctuations of the environment and availability of the energy. The technical problem addressed by this project is the optimization in terms of real time of the harvesting, utilization and storage of the energy in function of the energy needs of the application and the energy available in the harvesting system. Hence, the project consists in designing of the heterogeneous system composed of:
- several sources of energy of different nature (vibrations, thermal, photovoltaic, rechargeable battery) captured and converted by different harvesters,
- electrical power management unit, which merges all energy converted from different sources and distributes this energy between the load and battery.
ESIEE Paris is responsible for the development of the vibration energy harvesting mechanism by means of electrostatic (capacitive) transducer using the MEMS technology. LIP6 investigates in the design of the power interface electronics assisting the MEMS transducer; this PhD project is an essential part of the LIP6 contribution to the project. TIMA contributes to the development of the piezoelectric vibration energy harvester. CEA-LETI develops the power management electronics and the intelligent integrated interface with the load.

This PhD contributes to the existing body of knowledge on Electrostatic-based Vibration Energy Harvesting (e-VEH) system design. Particularly, this work investigates the low-power high-voltage (HV) design of a e-VEH conditioning electronics in a standard HV CMOS process.

Specifically, this thesis manuscript reports on the following:

- Presents a system-level heterogeneous model of a full e-VEH system allowing a simulation and analysis of the operating conditions of the electrostatic transducer, as well as a choice of specifications for the design of the power processing electronics.
- Develops a new auto-calibration algorithm allowing the e-VEH system to be adaptive in presence of non-stable and non-predictable source of external vibrations.
- Provides a new architecture of ultra-low power level shifter driving the high-voltage PMOS switch connect high-voltage floating nodes.
- Proposes a mixed-signal circuit design of the conditioning electronics implementing the auto-adaptive feature.
- Implements on chip and characterizes by a couple of measurements a driver of a high-voltage floating power switch.

[2]Techniques de l'Informatique et de la Microélectronique pour l'Achitecture des systèmes intégrés

- Laboratory tests of the electromechanical energy conversion by means of the MEMS capacitive transducer[3] operating within the conventional Yen's conditioning circuit, which includes the fabricated in this work integrated high-voltage switch.

Academic contribution of this thesis consists in several international workshops, national conferences and one journal article.

[3]Designed and fabricated by our project partners - ESIEE Paris

Chapter 2

Study, optimization and modeling of electrostatic vibration energy harvesting system

2.1 Overview

This chapter states on the study and modeling of the electrostatic vibration energy harvesting system. Particularly, we investigate the conditioning electronics assisting the capacitive transducer, while the research on the MEMS transducer device is carried out in parallel with this work by our research project partners in ESIEE Paris. Though our work does not cover the study and design of the MEMS generator, we take into consideration all specifications and limitations provided by ESIEE in order to model and analyze the whole system.

Present study concerns an analysis, optimization and modeling strategy of the VEH system. First, we introduce in details the architecture and the principle of operation of the chosen conditioning circuit. Thereafter we present the principle factors and conditions limiting the power generation, and propose a solution of optimization of the VEH operation in order to maximize its energy conversion efficiency. Then we address a problem and propose a solution of the adaptability of the harvester to the occasional fluctuations in the environment. We also show how to interface the output load with the harvesting circuit. At the end we show the behavior modeling of the system and discuss simulation results.

2.2 Auto-synchronous conditioning circuit

As we presented in section 1.7.3, there exist various types of conditioning circuits achieving energy conversion with capacitive transducer. Our study is based on a charge pump circuit proposed by Roundy [Roundy02]) and on an inductive flyback return circuit. This architecture was firstly implemented by B.C. Yen and J.H. Lang in 2006 [Yen06]. Recall

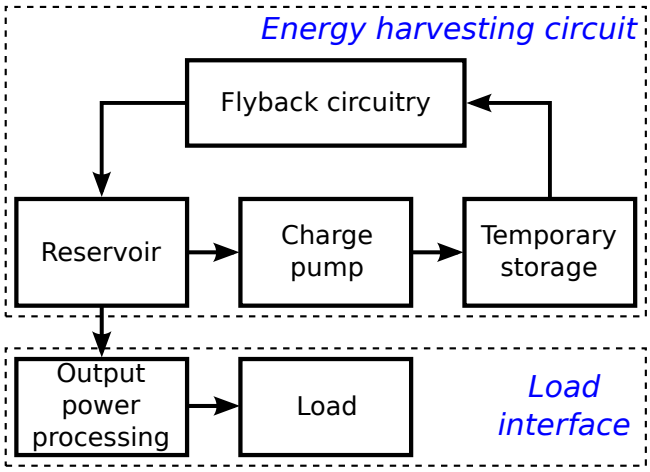


FIGURE 2.1: Block diagram of an electrostatic vibration energy harvester assisted by a *'charge pump and flyback'* conditioning circuit [Yen06].

that the charge pump uses diodes to synchronize the charging and discharging events of the variable capacitor, instead of the switches controlled by the precise electronic circuit [Meninger01, Torres10]. Hence, we call the charge pump based conditioning circuit as auto-synchronous.

The operation of the Yen circuit (Fig. 2.2) can be explained with a functional diagram in Fig. 2.1. The charge pump converts kinetic energy of vibrations into electric energy by moving electrical charges from a large reservoir capacitor C_{res} into a much smaller temporary storage capacitor C_{store}. The energy of a charge q stored on a capacitor is inversely proportional to the capacitance:

$$w = \frac{q^2}{2C}. \tag{2.1}$$

Hence, during the pumping, the energy of the charge increases, and by consequence, the charge pump operation requires additional energy. This energy can only come from the variations of the transducer capacitance, i.e. from the mechanical domain. In this way, the energy accumulated by the capacitive network $C_{res}C_{store}$ increases, and the gained energy is the energy converted from vibrations plus the initial energy stored in the capacitors before the operation.

The flyback return circuit used in Yen circuit transfers the energy accumulated in the network $C_{res}C_{store}$ into the reservoir capacitance C_{res}. This step has two objectives:

– The converted energy is available on a reservoir capacitance C_{res}, and can easily be used for different purposes, including the load. Moreover, as it will be shown below, the converted energy depends on the voltage of C_{res}, so the Yen flyback circuit provides a control on this voltage.

– The charge pump is kept in an electrical state at which a continuous energy production is possible (cf. explanation in the next subsections).

This conditioning circuit has several advantages, in particular:

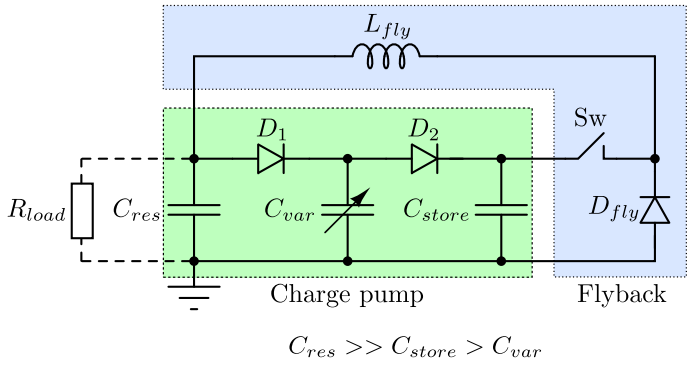


FIGURE 2.2: Schema of the VEH system employing the auto-synchronous conditioning circuit with an inductive flyback return, proposed by Yen and Lang [Yen06].

- self-powering: as we said, it is possible to accumulate the converted energy in the reservoir capacitor. In this way, the operation voltage of the conditioning circuit can be increased and the power conversion optimized. This is particularly useful if only low voltage is available for the system start-up.
- charging and discharging of the variable capacitor occurs automatically by passive switches (diodes), hence precise sensing and control electronics isn't required.
- only one switch is to be controlled: as it will be seen, this switch is synchronized with the voltage on C_{store} capacitance, which varies much slowly than the variable capacitance.

In spite of these positive points, this circuit has been poorly studied by the community, in comparison with another types of circuits. The realization of this circuit is difficult since it requires an implementation of a non-referenced to ground high voltage switch with low power constraints (Sw in Fig. 2.2). However, the progress in the CMOS technologies makes this task realistic, and the goal of our work is to proof the feasibility of that. This circuit was first published in 2006, and this PhD project started at 2008. Since then, several teams worked on this circuit, in particular, A. Kempitiya from Rensselaer Polytechnic Institute [Kempitiya10, Kempitiya12, Kempitiya13]: that proofs the interest of the community to this architecture.

In this section we will present the analysis of the conditioning circuit, explain the difficulties related with its design, modeling and implementation. We will then present the modeling techniques we used to study this circuit. We will also present our ideas about the intelligence which can be added to this circuit so to make it adaptive to the environment conditions. These ideas constitute the basis of the original work of the present thesis.

2.3 Charge pump

2.3.1 Structure and operation principle

The idea of using a charge pump for electromechanical energy conversion with a variable capacitor was proposed by Roundy [Roundy02]. A charge pump consists of two diodes and three capacitors: a large reservoir capacitor C_{res}, a temporary storage capacitor C_{store} of a smaller size, and a variable capacitor C_{var} varying between C_{min} and C_{max}. The values of these capacitances are related as:

$$C_{res} >> C_{store} >> C_{max} > C_{min} \tag{2.2}$$

The charge pump synchronizes the charge/discharge of the variable capacitor with the variation of its value without requiring external command. This is its main advantage in comparison with constant-charge/constant-voltage conditioning circuits [Meninger01, Torres09]. The synchronization of the charge flow with the variation of the capacitance is ensured by diodes D_1 and D_2. As follows from the topology of the network, the charge can be transferred in a unique direction: from C_{res} toward C_{var}, and from C_{var} toward C_{store}.

During the analysis of the charge pump, a hypothesis should be made about the diodes model. To provide a rough understanding of the circuit operation, however, it is enough to represent diodes as ideal unidirectional switches:

$$\begin{cases} I_d = 0, & \text{if } V_d < 0, \\ V_d = 0, & \text{if } I_d < 0. \end{cases} \tag{2.3}$$

A more accurate model is obtained if a non-zero threshold V_t is assumed:

$$\begin{cases} I_d = 0, & \text{if } V_d \leq V_t, \\ V_d = V_t, & \text{if } I_d < 0. \end{cases} \tag{2.4}$$

Although these models are well-suitable for qualitative and analytical circuit analysis, they are not compatible with a numeric modeling of the system. More information about the diodes numeric modeling will be provided in Section 2.3.4. Here, the diodes will be considered as in the model (2.3), unless otherwise isn't specified.

The mobile electrode of the transducer is supposed to be in a steady-state periodic motion, and the transducer capacitance varies periodically with a fixed amplitude (since C_{var} is a function of x). The exact law of the transducer capacitance variation is not important for the analysis presented in this section; it depends on the displacement law $x(t)$ and on the displacement-to-capacitance characteristic $C_{var}(x)$ of the transducer. However we suppose that over a variation period the transducer capacity experiences only one local maximum and one local minimum (C_{max} and C_{min}).

It is important to understand that the hypothesis of a fixed amplitude of the mobile mass vibration means that the force generated by the transducer does not affect the dynamic of motion of the mobile transducer electrode. This hypothesis is not physical:

as it will be shown, it implies a possibility to convert energy with infinite rate. It is useful however for analysis purpose. It allows an isolation of phenomena related with transducer/conditioning circuit operation, and makes an abstraction from mechanical part of the system.

The initial state of the charge pump is defined as follows: all three capacitors are pre-charged to a voltage V_0, so that $V_{res} = V_{var} = V_{store} = V_0$, and the transducer variable capacitor containing a charge Q_0 starts vary from its maximum possible value C_{max}. As all the node voltages are equal, diodes D_1 and D_2 are both off. An exact knowledge of the initial state is only important for the analysis, but not for the system operation.

In practice, this initial condition can be achieved on a circuit with all capacitances discharged by charging C_{res} to a voltage V_0 at the moment when $C_{var} = C_{max}$. Through the diodes, this capacitance shares instantaneously its charge with C_{var} and C_{store}, so equalizing the voltages. The alteration of the voltage on C_{res} due to this charge sharing is negligible, since C_{res} is supposed to be very large.

2.3.2 Energy and charge of the system

In this subsection we show how the energy of the charge pump can be expressed so to make easier and more elegant the analysis of the circuit.

It can be seen that at the initial state, the energy W_0 of the system is

$$W_0 = \frac{1}{2} V_0^2 (C_{res} + C_{max} + C_{store}), \tag{2.5}$$

and the total electrical charge Q_0 of the system:

$$Q_0 = V_0 (C_{res} + C_{max} + C_{store}). \tag{2.6}$$

The only dynamic process happening in the system is related with the variation of the variable capacitance. Obviously, the total electrical charge Q of the system is constant in time, equal to Q_0, and is the invariant quantity of the system. In contrast, the energy w of the system can change in time if the charge distributes over the capacitances.

In the analysis presented below, when considering the total charge and energy of the system, we neglect the the variable capacitance C_{var} since it is much smaller than C_{res} and C_{store}. Under this hypothesis, we can define the system energy as w

$$w = \frac{1}{2} C_{res} V_{res}^2 + \frac{1}{2} C_{store} V_{store}^2 = \frac{1}{2} \frac{Q_{res}^2}{C_{res}} + \frac{1}{2} \frac{Q_{store}^2}{C_{store}}, \tag{2.7}$$

where Q_{res} and Q_{store} are instantaneous charges of the corresponding capacitances. Since the sum of these charges is always equal to Q_0, we can introduce the charge variation ΔQ with relation to the initial charges on these capacitances, Q_{res0} and Q_{store0}:

$$w = \frac{1}{2}\frac{(Q_{res0} + \Delta Q)^2}{C_{res}} + \frac{1}{2}\frac{(Q_{store0} - \Delta Q)^2}{C_{store}} = \\ = W_0 + \frac{1}{2}\frac{\Delta Q^2}{C_{res}} + \frac{1}{2}\frac{\Delta Q^2}{C_{store}} + \frac{1}{2}\frac{Q_{res0}\Delta Q}{C_{res}} - \frac{1}{2}\frac{Q_{store0}\Delta Q}{C_{store}}. \tag{2.8}$$

The last two terms are equal since $Q_{res0}/C_{res} = Q_{store0}/C_{store} = V_0$, and we have:

$$w = W_0 + W = W_0 + \frac{1}{2}\left(\frac{1}{C_{res}} + \frac{1}{C_{store}}\right)\Delta Q^2. \tag{2.9}$$

The second term of the expression (2.9)

$$W = \frac{1}{2}\left(\frac{1}{C_{res}} + \frac{1}{C_{store}}\right)\Delta Q^2 \tag{2.10}$$

represents the energy gained by the system because of transfer of the charge ΔQ from C_{res} to C_{store}. This term is nothing else that the energy of a capacitance composed from a series connection of C_{store} and C_{res} charged to ΔQ. This gained energy can also be expressed through the voltage on this composed capacitor $V_{res} - V_{store}$:

$$W = \frac{1}{2}\frac{(V_{store} - V_{res})^2}{\frac{1}{C_{res}} + \frac{1}{C_{store}}} \tag{2.11}$$

Since $C_{res} >> C_{store}$ and V_{res} does not change much comparing to V_{store}, we can approximate this expression by:

$$W = \frac{1}{2}C_{store}(V_{store} - V_0)^2 \tag{2.12}$$

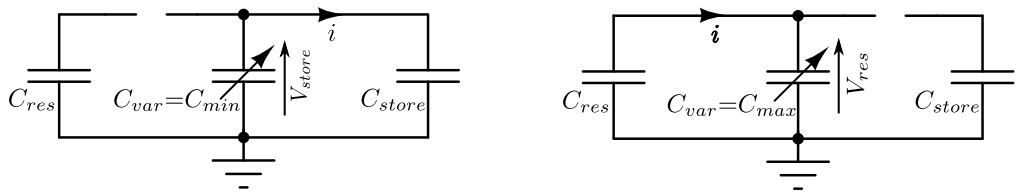
In this way, we can see that the energy of the system increases from the level W_0 by a quantity W depending only on the variation of the C_{store} voltage equal to

$$\Delta V_{store} = V_{store} - V_0. \tag{2.13}$$

The energy W_0 can be taken for a zero energy level of the charge pump, and W can be considered as the energy converted into the electrical domain by the variation of the transducer capacitance.

2.3.2.1 Operation over a harvesting cycle

The first cycle starts from the initial state, at which the transducer capacitance C_{var} is at its maximal value. During the first half of cycle, C_{var} decreases: In order to satisfy $Q = CV$, the voltage V_{var} tends to increase, but in this case the diode D_2 turns on, and the capacitors C_{var} and C_{store} are connected in parallel. This results in charge sharing



(a) First half of cycle (b) Second half of cycle

FIGURE 2.3: Equivalent circuit diagram of a charge pump harvesting cycle.

between C_{var} and C_{store}: since C_{var} decreases, charges are flowing from C_{var} to C_{store} until V_{var}=V_{store} as shown in Fig. 2.3a.

The second half of the first cycle starts when vibrations change direction so that C_{var} increases from C_{min} to C_{max}. As the charge can not flow from C_{store} to C_{var} because of the diode D_2, the charge of C_{var} remains constant and V_{var} decreases, thereby turning off D_2. As V_{var} drops further until V_{var}=V_0, D_1 turns on resulting in charge replenishment from C_{res} to C_{var} as shown in Fig. 2.3b. When C_{var}=C_{max} it is recharged with Q_0 as in the beginning of the harvesting cycle. Since $C_{res} >> C_{store}$, during a charge pumping cycle the voltage drop on C_{res} can be neglected, while V_{store} is considerably increased so that $V_{res} \approx V_0 < V_{store}$.

The second and next cycles of vibrations happen according to a slightly different scenario. Indeed, the initial condition of the network is not the same as before the first cycle: the voltage V_{store} is greater than V_{res}. Hence, the first half of cycle happens as follow: first, C_{var} decreases, its voltage increases and until it reaches V_{store}, both diodes are off. Only after V_{store} is reached, the operation is the same as during the 1st cycle.

In this way, on one cycle the variable transducer operates twice at constant charge (when C_{var} goes up and down), once at constant voltage V_{res} and once at a mode where the voltage is nearly constant and equal to V_{store}. The last statement is true if $C_{store} >> C_{max}$ – that is the case in practice. The only result of one cycle of the charge pumping is a transfer of charges from C_{res} to C_{store}: it can be verified that such operation requires an external energy. The latter comes from the mechanical domain through the variation of C_{var}. As V_{res} evolves slowly and may be considered as constant, only the evolution of V_{store} is significant. The converted electrical energy is accumulated in a closed capacitive system $C_{res}C_{store}$ in a form of the voltage difference between V_{res} and V_{store}.

Each next cycle starts at $V_{store\,n-1}$ achieved at the preceding cycle – in this way, as the charge pump operates, V_{store} increases. As shown in [Yen06], the relation between the V_{store} value at the beginning and at the end of the n^{th} cycle ($V_{store\,n-1}$ and $V_{store\,n}$) is:

$$V_{store\,n} = \alpha V_{store\,n-1} + \beta, \tag{2.14}$$

where

$$\alpha = \frac{C_{store}}{C_{store} + C_{min}}, \text{ and } \quad \beta = V_0 \frac{C_{max}}{C_{store} + C_{min}}. \tag{2.15}$$

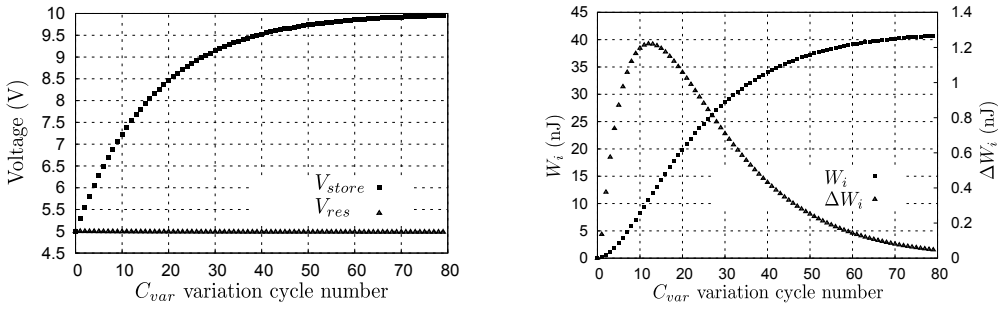


FIGURE 2.4: Example of the evolution of the charge pump state during numerous n C_{var} variation cycles: (a) voltages V_{res} and V_{store}: V_{store} rises from V_0=5 V up to the saturation (e.g. 10 V); (b) instantaneous energy harvested at a vibration cycle ΔW_i and total energy accumulated from the beginning of the charge pumping W_i.

Equivalently, $V_{store\,n}$ can be expressed as:

$$V_{store\,n} = V_0 \left[\left(1 - \frac{C_{max}}{C_{min}} \right) \left(\frac{C_{store}}{C_{store} + C_{min}} \right)^n + \frac{C_{max}}{C_{min}} \right], \tag{2.16}$$

These formulae allow a calculation of the energy converted at cycle n (ΔW_n). This energy is equal to the difference between the energies of the capacitive system at the beginning and at the end of the cycles W_{n-1} and W_n:

$$\Delta W_n = W_n - W_{n-1}. \tag{2.17}$$

W_n is calculated through 2.12. Hence, the expression for ΔW_n is:

$$\Delta W_n = \frac{C_{store}}{2} [(V_{store\,n} - V_0)^2 - (V_{store\,n-1} - V_0)^2] \tag{2.18}$$

In the next section we consider the multi-cycle operation of the charge pump, and discuss the evolution of $V_{store\,n}$ and ΔW_n with time.

2.3.2.2 Operation over numerous harvesting cycles

Considering that the sequence $\{V_{store\,n}\}|_{n\in\mathbb{N}}$ starts with $V_{store\,0} = V_0$, we obtain an evolution shown in Fig. 2.4a). The corresponding evolution of the energy converted at each cycle (the sequence $\{\Delta W_n\}|_{n\in\mathbb{N}}$) and of the accumulated converted energy $\{W_n\}|_{n\in\mathbb{N}}$, is given at Fig. 2.4b.

The energy converted at a vibration cycle ΔW_n rises in the beginning, reaches a maximum and then goes down to zero. This behavior corresponds to the evolution of V_{store} voltage that starts rising with high rate and then tends asymptotically to the value called "saturation voltage". As the charge pump approaches the saturation, diode D_2

is no more capable to be forward biased. The saturation voltage is defined as the limit of (2.16) when $n \to \infty$:

$$V_{store\ max} \approx V_{store\ sat} = V_0 \frac{C_{max}}{C_{min}} \tag{2.19}$$

From the curve ΔW_i it can be seen that the energy conversion rate is not constant, and depend on the number of the pumping cycle n or, equivalently, on the initial voltage $V_{store\ n-1}$. The goal of the circuit is to maximize the energy conversion rate (equivalently, the converted power). We present the calculation of the $V_{store\ n-1}$ value at which the converted energy on a cycle is maximal. Using the equations (2.18) and (2.16), we obtain a quadratic polynomial function $\Delta W_n(V_{store\ n-1})$ expressed in factored form:

$$\Delta W_n(V_{store\ n-1}) = \frac{C_{store}}{2}[V_{store\ n-1}(\alpha - 1) + \beta][V_{store\ n-1}(\alpha + 1) + \beta - 2V_0]. \tag{2.20}$$

This quadratic polynomial has a negative quadratic coefficient, is open downward and by consequence the function has a maximum at $V_{store\ n-1}$ given by:

$$V_{store\ opt} = \frac{1}{2}\left[-\frac{\beta}{\alpha - 1} - \frac{\beta - 2V_0}{\alpha + 1}\right], \tag{2.21}$$

Simplifying this equation and returning to coefficients given by α and β, we get:

$$V_{store\ opt} = V_0 \frac{\frac{C_{max}}{C_{min}} + \frac{C_{min}}{C_{store}} + 1}{\frac{C_{min}}{C_{store}} + 2}, \tag{2.22}$$

The maximal value of ΔW_n corresponding to $V_{store\ opt}$ is:

$$\Delta W_{max} = \frac{{V_0}^2}{2} \cdot \frac{C_{min}(\frac{C_{max}}{C_{min}} - 1)^2}{\frac{C_{min}}{C_{store}} + 2}, \tag{2.23}$$

If $C_{min} << C_{store}$, the optimal value of V_{store} and ΔW_{max} can be rewritten as:

$$V_{store\ opt} = \frac{1}{2}V_0(\frac{C_{max}}{C_{min}} + 1). \tag{2.24}$$

and

$$\Delta W_{max} = \frac{1}{4}{V_0}^2 C_{min}\left(\frac{C_{max}}{C_{min}} - 1\right)^2, \tag{2.25}$$

Taking into account the above assumptions, the maximal power that can be generated by the charge pump is:

$$P_{max} = \Delta W_{max} f_e, \tag{2.26}$$

where f_e is the frequency of variation of the transducer capacitance. This frequency can differ from the frequency of mechanical motion of the mobile mass, depending on the transducer geometry. In this work, we use the transducer device [Guillemet13] having an electrical frequency twice greater than the frequency of mechanical vibrations, f_e=2f_m

(i.e. during a complete cycle of a proof mass displacement, the capacitance performs two variation cycles).

If $C_{max} >> C_{min}$ the following approximation can be done:

$$\Delta W_{max} = \frac{{V_0}^2}{4} \cdot C_{max} \frac{C_{max}}{C_{min}}, \tag{2.27}$$

and

$$V_{store\ opt} = \frac{1}{2} V_0 \frac{C_{max}}{C_{min}}. \tag{2.28}$$

So, to allow the charge pump continuously convert the energy with the maximum rate, the voltage V_{store} should be maintained close to the optimal value $V_{store\ opt}$. This is illustrated in Fig. 2.4: if the voltage V_{store} is kept near $V_{store\ opt}$, the average energy conversion rate is close to maximal. Such operation can only be done by an external circuit called "return circuit". The idea is to return the charges from C_{store} to C_{res} as far as C_{store} voltage goes far from the optimal value. This charge return should be done so to utilize the energy converted from the charge pumping.

2.3.2.3 Optimization of the capacitance values

As we have stated in section 2.3 the reservoir capacitor C_{res}, ideally, must behave as a DC source so that its electric charge remains unaffected for a long time. According to Eq. 2.2, we have chosen the value of 1 μF, so to be 3 order larger than C_{store}, and 4-5 order larger than C_{var}. So in the context of several charge pump cycles, V_{res} is kept constant.

The value of a storage capacitor C_{store} defines the number of pump cycles. During charge pumping the evolution of V_{store} occurs in discrete steps, which depend on the ratio C_{max}/C_{min}, initial voltage on C_{store} (V_0) and the value of C_{store} capacitance itself.

The study on C_{store} capacitance as well as the number of pump cycles effecting the generated power has been done by researchers from Rensselaer Polytechnic Institute (USA), namely A. Kempitiya et al. [Kempitiya12], who started their research on Yen's circuit practically at the same period as we did. From their analysis the following conclusions can be made. For whatever number of charge pump cycle n, an optimal capacitance value of C_{store} exists, at which a peak power is generated. The effect of C_{store} on energy conversion is considered as a parasitic capacitance, accordingly to [Roundy03b], and hence it should be minimized. However a small storage element means less stored energy and higher flyback frequency. A trade off provides an optimal value of C_{store}, at which the harvested and stored energy is maximum. Such an optimal capacitance and the optimal number of cycles n is found from numerous simulations, where both parameters were simultaneously varied (cf. Fig. 2.5). As authors show, the peak power corresponds to n=1 and C_{store}=0 that is the case of the Meninger's circuit (or synchronous), and the power decays as C_{store} parasitically loads down the energy harvesting process by reducing the C_{max}/C_{min}, and consequently the maximum possible voltage during discharge. With the increase of a number of cycles n and simultaneous increase of a storage capacitor value, the generated power decreases slowly. The authors decided to choose

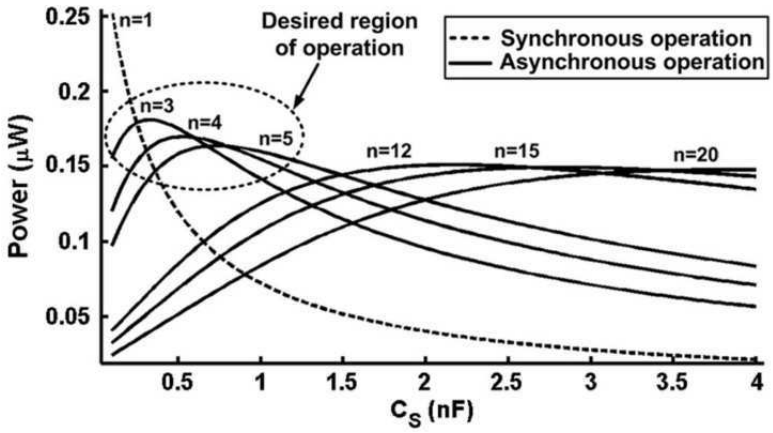


FIGURE 2.5: Power stored in C_{var} and C_{store} as a function of storage capacitor values for various harvesting cycles provided by [Kempitiya12]. Circuit operation parameters: C_{max}=843 pF, C_{max}/C_{min}=3.26, V_0=5 V, R_L=200 MΩ, V_{Diodes}=0.7 V, f_{var}=27.6 Hz.

for their work an optimal zone corresponding to $3 \leq n \leq 5$, and C_{store} less than 1 nF. However, such a low number of cycles results in a high frequency of the energy return events, which relate to considerable power dissipation. At the same time, looking to the figure, we can notice that the power generated for $12 \leq n \leq 20$ and 1.5 nF$\leq C_{store} \leq$4 nF is only slightly lower, while the frequency of the energy return is several times reduced.

In spite of the approach of Kempitya et al. [Kempitiya12], we do not consider C_{store} as a parasitic capacitance; conversely, we look forward to increase it. It is interesting to note that the speed at which the charge pump saturates is the only parameter impacted by C_{store} (as it will be demonstrated below): the energy harvested by cycle, the maximal energy and V_{store} voltage are not affected by this parameter. When we will discuss the return circuit, it will be clear that a large C_{store} is advantageous for the operation of the overall system.

However, there is an upper limit of the C_{store} capacitance value, which is related with the charge that this capacitor will have to transfer during the flyback phase (cf. the next section). Indeed, depending on implementation of the switch, it may be difficult to transfer high electrical energy with one flyback cycle. By consequence, so far, for our research work we fixed the value of C_{store}=3.3 nF, and instead of the optimal number of pumping cycles n, we search for an optimal zone of V_{store} operation, as will be described further, in section 2.4.2.

Let us discuss the influence of C_{store} value on the charge pump operation. The following proposition will be proven:
As far as $C_{store} >> C_{min}$, the number of pump cycles needed to reach a given level V_1 of V_{store} voltage is proportional to C_{store}.

In this proposition, V_1 is any value chosen between V_0 and $V_{store\ sat}$. To prove it, it is enough to consider Eq. 2.16, to set $V_{store\ n-1} = V_1$ and to express n:

$$n = log_{\frac{C_{store}}{C_{min}+C_{store}}} \frac{\frac{V_1}{V_0} - \frac{C_{max}}{C_{min}}}{1 - \frac{C_{max}}{C_{min}}}, \tag{2.29}$$

This formula can be transformed:

$$n = \frac{ln\frac{\frac{V_1}{V_0} - \frac{C_{max}}{C_{min}}}{1 - \frac{C_{max}}{C_{min}}}}{ln\frac{C_{store}}{C_{min}+C_{store}}}, \tag{2.30}$$

The numerator does not depend on C_{store}. Since $C_{min} << C_{store}$, the denominator can be approximated by $-C_{min}/C_{store}$, by using first-order Taylor series development of the $ln(1+x)$ function. Hence, we obtain

$$n \propto C_{store}. \tag{2.31}$$

By consequence, the value of C_{store} has a direct impact on the number of cycles necessary to reach a given level of V_{store}. Since V_{store} evolves within fixed limits $(V_0, V_{store\ sat})$, C_{store} has an impact on the V_{store} increment produced by one pumping cycle (cf. Fig. 2.4a): the larger C_{store} is, the smaller is the V_{store} step.

2.3.3 The QV-plane of the charge pump

A QV-diagram is an alternative tool providing a qualitative insight in the charge pump operation. The QV-diagram is a locus presenting the set of states of the variable capacitance, in the axes "charge" and "voltage". Each cycle on a locus represent an energy generation or absorption by the variable capacitance during the corresponding operation cycle. The area of the locus is numerically equal to the absorbed or generated energy. Fig. 2.6 presents the QV-plane of a variable capacitance operated in a charge pump. The starting state corresponds to the point A.

The pass $A \rightarrow B$ on the QV-diagram corresponds to the decrease of the transducer capacitance from C_{max} to C_{min}, when the capacitances C_{var} and C_{store} are connected in parallel by the diode D_2. The slope of the line AB is equal to :

$$\mathrm{d}Q/\mathrm{d}V = -C_{store}. \tag{2.32}$$

If $C_{store} >> C_{max}$, on the scale of the plot the AB line should be virtually parallel to the Q axis (the slope to be compared with the slope of the locus $Q = C_{max}V$).

The pass $(B \rightarrow C)$ corresponds to the phase in which C_{var} increases, and the voltage V_{var} is still higher than V_{res}, so that the diode D_1 is off. The pass $C \rightarrow A$ corresponds

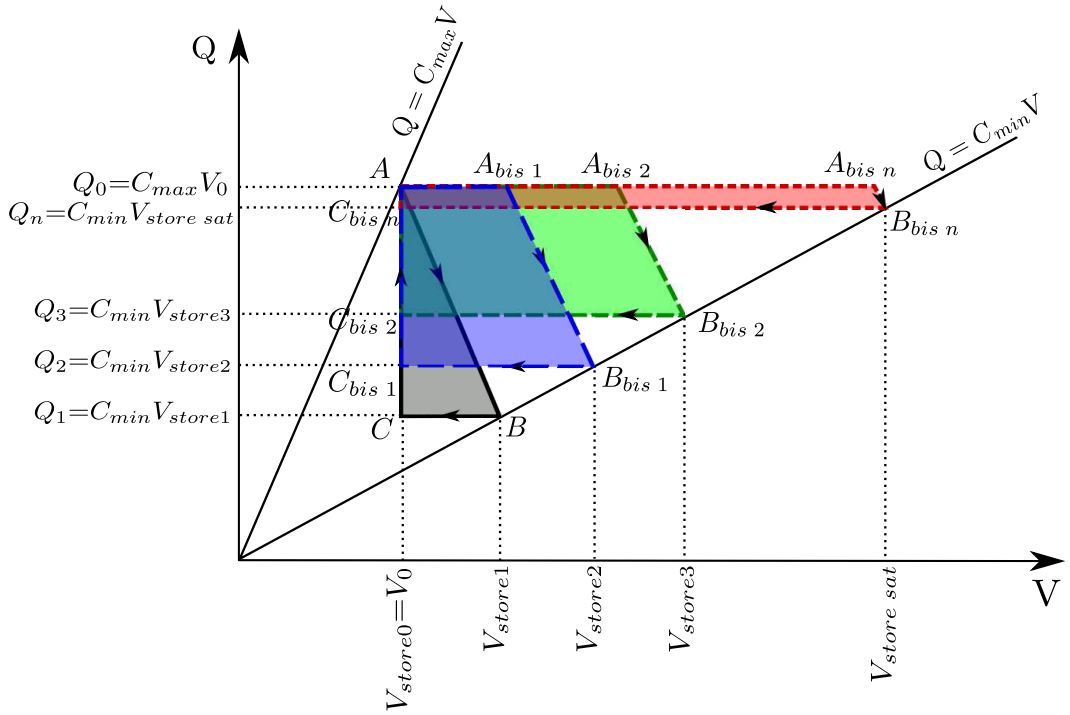


FIGURE 2.6: QV-diagram corresponding to energy conversion by capacitive transducer for each charge pump cycle.

to charging of C_{var} to $Q_{var} = C_{max} V_{res}$ to increase to Q_0 and, thereafter, returning the circuit to its starting point.

In this way, the first cycle is triangular. Since after the first cycle V_{store} is increased, for a second cycle an additional point $A_{bis\ 1}$ appears, hence constituting a trapeze A, $A_{bis\ 1}$, $B_{bis\ 1}$ and $C_{bis\ 1}$. The total surface area of the trapeze is greater than that of a triangle ABC, and it corresponds to the greater amount of converted energy. The third cycle is a trapeze as well with a surface bounded by points A, $A_{bis\ 2}$, $B_{bis\ 2}$ and $C_{bis\ 2}$, whose net surface area is higher compared to the trapeze of a second cycle.

It can be observed that the area of the successive cycles increases, reaches a maximal value and then decreases, representing the evolution of the energy conversion rate. In this way, the analysis presented in subsection 2.3.2.2 is well illustrated by this diagram.

2.3.4 Influence of diodes

In this subsection we present the results for $V_{store\ opt}$ and P_{max} which accounts for losses in the diodes. The calculation presented in section 2.3.2.2 is exactly the same, with two following differences:

- The initial voltages on the capacitors C_{res}, C_{var} and C_{store} are V_0, $V_0 - V_{th}$ and $V_0 - 2V_{th}$, respectively.

- The value of the parameter β in the recursive equation relating $V_{store\ n}$ and $V_{store\ n-1}$ (2.14) is now given by:

$$\beta = \frac{C_{max}(V_0 - V_{th}) - C_{min}V_{th}}{C_{store} + C_{min}}. \tag{2.33}$$

Simplifying the eq. (2.21) and returning to coefficients given by α in (2.15) and β in (2.33), we get:

$$V_{store\ opt} = \frac{V_0(\frac{C_{max}}{C_{min}} + \frac{C_{min}}{C_{store}} + 1) - V_{th}(\frac{C_{max}}{C_{min}} + 1)}{\frac{C_{min}}{C_{store}} + 2}, \tag{2.34}$$

If $C_{min} << C_{store}$, $V_{store\ opt}$ can be rewritten as:

$$V_{store\ opt} = \frac{1}{2}(V_0 - V_{th})(\frac{C_{max}}{C_{min}} + 1). \tag{2.35}$$

Similarly to eq. 2.25, the maximal energy converted at cycle n (ΔW_n) is:

$$\Delta W_{max} = \frac{1}{4}(V_0 - V_{th})^2 C_{min}\left(\frac{C_{max}}{C_{min}} - 1\right)^2, \tag{2.36}$$

Comparing Eq. 2.36 and 2.25, the conclusion is that the influence of the diodes can not be neglected, especially if the bias voltage V_0 is relatively low (several volts).

2.3.5 Comparison with constant charge conditioning circuit

A question of comparison among different conditioning circuits is often risen. Here, we will propose a comparison between the studied charge-pump based circuit and the circuit based on the triangular constant-charge QV-cycle. The operation of this latter circuit is well studied and understood, and it is considered being in theory the most advantageous for energy conversion with capacitive transducer.

To adequately compare two circuits, it is important to fix the conditions in which the circuit performances are evaluated, and well define the figures which are compared.

We suppose that for both circuits, the transducer operates as stated in 2.3, and its capacity variation in time has only one maximum (C_{max}) and only one minimum (C_{min}) on a period. We suppose also that the electronics used for the switches controlling the circuits can support a maximal voltage V_{max}. This limitation is related to the circuit technology used for the control electronic implementation.

Table 2.1 provides a comparison between the performances of the two considered circuits. Aside the figures of the maximal energy conversion rate, we provide the information about the maximal voltage present in the circuit. Expressions for the charge pump are given under hypothesis that $C_{min} << C_{store}$, which is a founding hypothesis of this analysis (cf. section 2.3.2.3). The disadvantage of these expressions is the use of V_0 which is the initial voltage on the transducer when $C_{var} = C_{max}$. Indeed, this voltage

TABLE 2.1: Formulae for the maximal voltage and the maximal power of a charge pump and of the Meninger circuit

	Maximal power P_{max}	Maximal voltage V_{max}
Meninger circuit	$\frac{1}{2}V_0^2 C_{max}\left(\frac{C_{max}}{C_{min}}-1\right)f_e$	$V_0\frac{C_{max}}{C_{min}}$
Charge pump	$\frac{1}{2}V_0^2 C_{min}\left(\frac{C_{max}}{C_{min}}-1\right)^2 f_e$	$\frac{1}{2}V_0\left(\frac{C_{max}}{C_{min}}+1\right)$

is not a constraint, since it can be risen by a DC-DC conversion from a low voltage source (cf. the results of experiments in Chapter 4). Also, this voltage is smaller than the voltage on the transducer when its capacitance is minimal. Hence, we would like to express P_{max} of both circuits through the maximal voltage V_{max} present in the circuit. Using the expressions in table 2.1 we get for the constant-charge circuit:

$$P_{max} = \frac{1}{2}V_{max}^2 C_{min}\left(1-\frac{C_{min}}{C_{max}}\right)f_e, \tag{2.37}$$

and for the charge pump:

$$P_{max} = V_{max}^2 C_{min} f_e, \tag{2.38}$$

where f_e is the frequency of variation of the transducer capacitance.

These formulae suggest a very interesting result. If the ratio C_{max}/C_{min} is large, the charge pump may convert exactly two times larger power than the constant charge circuit, whereas supporting the same maximal voltage. The performance of the constant charge circuit drops even more when C_{max}/C_{min} is not large. For example, the ratio between the maximal convertible powers is 4 if $C_{max}/C_{min} = 2$.

This analysis proves that the charge pump based conditioning circuits are more efficient in the context when the operation voltage level is the main limitation of the used circuit technology. Since the technologies of the electronic circuits are always limited by the voltage that can be supported, this advantage of the Yen's circuit is very important from the point of view of physical realization.

Discussions on the charge pump operation.
The results obtained in the last subsection are very important for this PhD project. Here we summarize them:

- The energy conversion rate of the charge pump is not constant, and depends on two electrical parameters: V_0 (or equivalently V_{res}) and the value of V_{store} at the beginning of the cycle.
- When the charge pump is run "freely", V_{store} increases from V_{res} following an exponential law given by the recurrence relation (2.14), where n can be considered as the dimensionless time normalized by division on the cycle duration.

- For a given value of V_{res}, there is an optimal value of V_{store} guaranteeing a maximal converted energy in the corresponding cycle.
- The energy conversion rate drops to zero as the pumping time goes to infinity.

By consequence, a freely running charge pump is not suitable for a sustainable conversion of mechanical energy. An external circuit is necessary for maintaining the charge pump in the mode where the energy conversion rate is close to the optimal value. This issue motivates the introduction of the return *flyback* circuit.

2.4 Flyback return

The goals of the return circuit based on a Buck DC-DC conversion, sometimes called "flyback circuit", are the following:

- return the charge pump to a state that corresponds to a maximal harvested power according to Fig. 2.4;
- transfer the accumulated energy from the mechanical domain stored in $C_{res}C_{store}$ system to C_{res};

The DC-DC conversion is achieved between the voltage V_{store} (the input) and the voltage V_{res} (the output). The flyback circuit is composed of a switch, an inductor L and a freewheeling diode D_{fly}. The energy that the flyback must efficiently transfer is the energy corresponding to the voltage difference between V_{store} and V_{res}:

$$W_{transf} = \frac{1}{2}C_{store}(V_{store\,n} - V_{res})^2, \tag{2.39}$$

where n is the number of charge pump cycles, and if $n \to \infty$, $V_{store\,n}$=$V_{store\,max}$.

2.4.1 Operation

When the switch Sw in Fig. 2.2 is off, the return circuit is inactive. The switch Sw is turned on by an external control circuit when the charge pump goes out of the optimal energy generation mode close to the saturation.

Considering the flyback actuation time $t = t_0$, we now analyze the flyback operation. It is achieved in two steps. First, due to different potentials appeared at two terminals of the inductor, the accumulated charges from C_{store} travel to C_{res}, so creating a current i_L flow as shown in Fig. 2.7a. In this way, the inductor accumulates an electromagnetic (EM) energy. The first step lasts till V_{store} approaches V_{res} and the current through the inductor becomes maximal I_{max} (cf. Fig. 2.7c).

The second step consists in de-energizing the inductor. At $t = t_1$ the switch Sw goes off: the inductor generates a voltage on a freewheeling flyback diode D_{fly} so that the

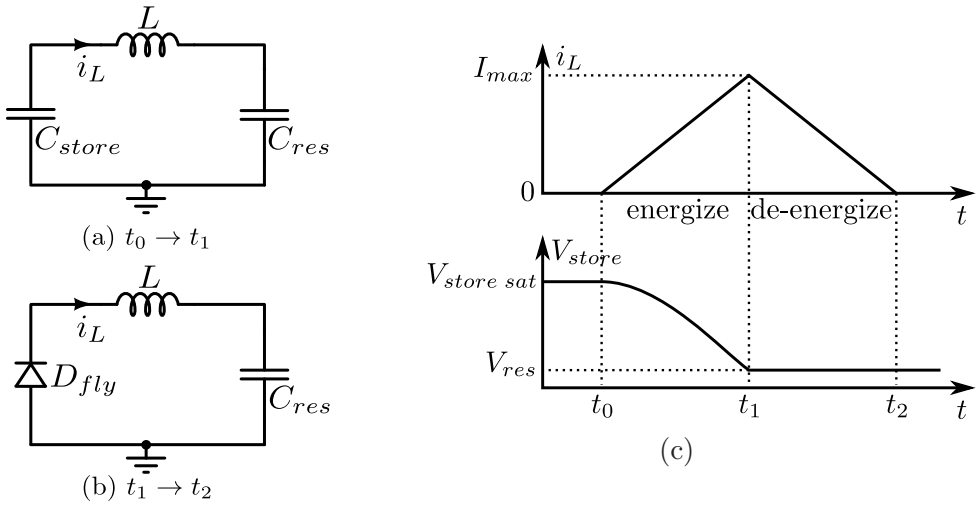


FIGURE 2.7: Equivalent flyback circuit diagram of energizing (a) and de-energizing (b) the inductor; (c) illustration of the flyback operation: current in the flyback path and voltage V_{store}.

inductor current continues flowing through this diode, and the inductor EM energy is fully transferred to C_{res} at $t = t_2$ (cf. Fig. 2.7b). After the inductor is discharged, D_{fly} restricts the current to flow in reverse direction, and the whole system returns to a state close to the initial state of the charge pump.

In this way, during the first stage, C_{res} receives back the charges transferred to C_{store} by the charge pump, and the corresponded converted energy is stored in the inductor. During the second phase C_{res} is being replenished with the energy converted during the charge pumping and temporarily stored in the inductor. Since during the second phase the inductor is connected to the ground through D_{fly}, the charge arriving on C_{res} come from the ground, and not from the capacitances of the circuit. In this way, even if there is some leakage, the latter are compensated by the new charges issued from the ground. It can be considered that the flyback circuit uses the energy converted from the mechanical domain so to rise new electrical charges from the ground and put them onto reservoir capacitor.

The duration of the "on" state of the switch defines the voltage on V_{store} after the flyback. If this duration is equal to the quarter period of the resonator composed from C_{store}, C_{res} and L), after the flyback $V_{store} = V_{res}$. This value is :

$$\tau = \frac{1}{4} \cdot 2\pi \sqrt{\frac{LC_{res}C_{store}}{C_{res} + C_{store}}} \approx \frac{1}{4} \cdot 2\pi \sqrt{LC_{store}} \tag{2.40}$$

If the duration is greater than τ, the result is the same: after the flyback $V_{store} = V_{res}$ since V_{store} can not be less than V_{res} because of the charge pump diodes. If the duration is smaller than τ, the final value of V_{store} is greater than V_{res}, although less than the V_{store} value at which the flyback started. In this way, the duration of the flyback controls the value of V_{store} at which the next charge pumping cycle starts. This important feature will be exploited for definition of the optimal operation mode of the circuit.

The inductor current is zero at the beginning and rises during τ up to I_{max}. If no load is connected to C_{res}, after the flyback operation, V_{res} voltage increases in comparison with the level at the beginning of the charge pumping. The increase of V_{res}, however, is small as the reservoir capacitor receives a tiny portion of charges with respect to the amount of stored charges. Hence, neglecting the slight evolution of V_{res} and assuming that it is constant over one commutation cycle, it is possible to estimate the maximal current of the inductor:

$$I_{max} = \frac{V_{store\_n} - V_{res}}{L}\tau \tag{2.41}$$

Now we consider numerous cycles "charge pumping - flyback". Even though the voltage increment on C_{res} is slow, it is not negligible anymore. Conversely, the increased V_{res} represents the electrical energy converted from the mechanical domain.

If the elements used in the flyback circuits are ideal (no diode threshold, no losses in the inductor, ideal switch), the flyback efficiency is 100 %. In practice, the flyback operation is a wasteful process due to constitutive energy losses in switch, inductor, diode D_{fly} and control electronics. The losses depend on the energy transferred during the flyback, but some losses are fixed (e.g., the losses related to the control electronic). Hence, it is better for the flyback circuit to transfer a large energy at one time. For this reason, C_{store} should be chosen large. Not only the large C_{store} accumulates a large energy, but also the number of cycles of charge pumping before the flyback is large. By consequence, the flyback will be activated with reduced frequency, so saving energy related with the control.

The fundamental challenge consists in the determination of the optimal flyback switching sequence, that affects the overall system performance as can be seen from Fig. 2.4b. This problem is discussed in the following section.

In the work of B. Yen et al. [Yen06] the switch activating the flyback was realized by a MOS transistor controlled by an external source; the latter generated a periodic sequence of control pulses, which were independent of the circuit state. This technique illustrated the operation ability of the proposed architecture. That study, however, did not concern the research of the optimal operation zone for the harvester, neither the adaptation challenge of the system to the realistic vibration parameters. Also, there were a lack of the expression for the theoretic maximum power that can be generated by charge pump with flyback. So, the circuit consists of numerous problems to be studied.

The first stage of analyzing the circuit is the development of the theoretic efficiency of the Yen's circuit. The second stage provides the study about the optimal zone of the circuit operation. The third stage states on the automatic adaptation of the system to the fluctuations in the ambient environment so to keep the system in the optimal operation zone even though vibration parameters change in time. All these analysis we can do by accurate modeling of the system. The behavior model that we developed is described in the end of this chapter.

2.4.2 Generation of flyback switching event

In contrast with the conditioning circuit using a constant charge QV-cycle, the Yen's conditioning circuit has only one switch, which must be controlled externally. As follows from the analysis of the charge pump operation, the timing of the flyback activation has a direct impact on the rate of converted energy. The analysis shows that the switch control sequence must be derived in function of the electrical state of the charge pump.

In this subsection we present our approach to a smart flyback event generation. We will demonstrate that the approach of fixed periodic switched events used in [Yen06] is not suitable for an operation in a realistic environment.

Optimal switch events generation.
As it was shown in section 2.3.2.2, the maximal energy conversion rate is only achieved at one charge pump cycle, when $V_{store} = V_{store\ opt}$ given by Eq. 2.24. Of course, since V_{store} grows by discrete steps during the operation of the charge pump, the optimal $V_{store\ n-1}$ is the closest to this exact value. After one cycle of charge pump started with that value of V_{store}, the V_{store} value changes, and is not optimal anymore. Hence, in theory, only one cycle of a freely running charge pump can provide a maximal energy conversion rate.

By consequence, ideally the flyback circuit should operate as followed. The flyback should be activated immediately after the pumping cycle corresponding to the maximal energy conversion rate. During the flyback, the charge return on C_{res} should be such that after flyback, V_{store} has the optimal V_{store} value. As we explained in section 2.4, the V_{store} value after the flyback is easily controlled by the duration of the switch "on" phase.

However, such an operation is suboptimal. First, a very precise control of the operation is needed. The switch operation should be precisely synchronized with the motion of the mobile mass, since the flyback should be activated exactly after one pumping cycle. Obviously, such a precision costs some energy and a complex electronics. In addition, a frequency activation of the flyback multiplies fixed energy losses. Actually, such an operation has no advantages in comparison with the constant-charge circuit, where the switches are also activated at every cycles, and are also precisely synchronized with the vibrations.

Therefore, a trade-off between the maximal power value and the frequency of the flyback activation should be considered. In other words, the converted power must be the highest and the frequency of the flyback the lowest. In response to this compromise, we propose to allow the charge pump operate in a *range* of V_{store} near the optimal value, instead of its precise optimal value. Thus, maintaining the converted power between its maximal value and some value below it, the flyback frequency can be considerably reduced, while the converted power still would remain high, as illustrated in Fig. 2.8b. This power range corresponds to the interval of V_{store} bounded by V_1 and V_2 parameters on the bottom and the top of $V_{store\ opt}$, respectively. In this way, V_1 and V_2 allow a definition of the optimal operation mode of the circuit. The switch control event generation is obtained from the measurement of the voltage on a large capacitor C_{store}, rather than from detection of extreme variations of a low variable capacitance [Galayko07].

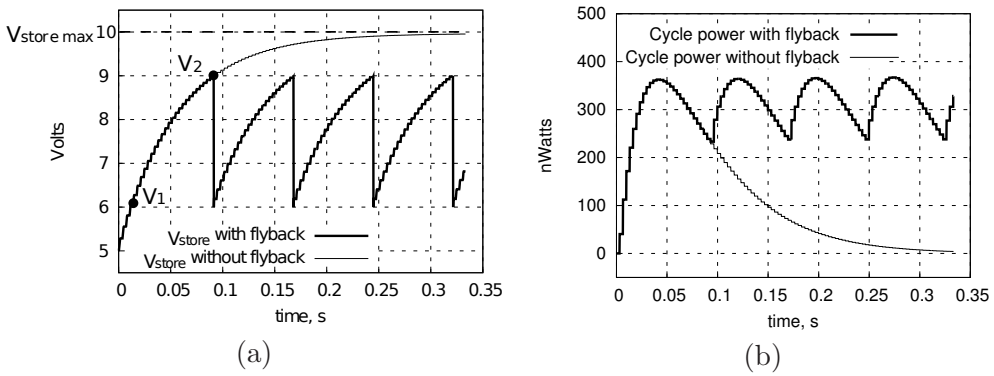


FIGURE 2.8: Behavior of the charge pump with an inductive flyback return: (a) V_{store} voltage; (b) average power of the energy conversion per vibration cycle ΔW_i.

The optimal values of V_1 and V_2 depend on the fixed energy losses associated with each flyback activation, and on the precision of the used control electronics. The formula providing the actual efficiency of the flyback operation is given by:

$$\eta(V_1, V_2) = 1 - \frac{W_{losses\ var}(V_1, V_2) + W_{losses\ fixed}}{W(V_1, V_2)}, \tag{2.42}$$

where $W(V_1, V_2)$ is the energy converted by the charge pump when V_{store} voltage changes from V_1 to V_2, $W_{losses\ var}(V_1, V_2)$ is the variable part of losses related with the operation of flyback, which depends on the parameters V_1 and V_2, and $W_{losses\ fixed}$ is the fixed part of the losses associated with flyback. The optimal values of V_1 and V_2 can be found by numeric maximization of η over V_1 and V_2 in the interval $(V_0, V_{store\ sat})$.

However, the above analysis can only be done at the final stage of the design, when the details about the operation of the whole circuit are known. For the first steps of the system level design, it is enough to use the empirical formula for the calculation of V_{store} thresholds:

$$\begin{cases} V_1 = V_{res} + K_1(V_{store\ max} - V_{res}) \\ V_2 = V_{res} + K_2(V_{store\ max} - V_{res}), \end{cases} \tag{2.43}$$

where K_1 and K_2 are the coefficients determining the fraction, typically $K_1 = 0,1..0,2$ and $K_2 = 0,6..0,8$. $V_{store\ max}$ can be defined following Eq. 2.19.

In order to let the charge pump operate between V_1 and V_2, the flyback switch controller must fulfill three operations at the same time: memorizing the values of V_1 and V_2, monitoring V_{store}, and comparison of V_1 and V_2 with V_{store}. The desirable operation of the flyback switch is modeled by a finite state automaton. This automaton is driven by the events related to the crossing by V_{store} the threshold parameters V_1 and V_2, and it generates the switching signals that drive the flyback switch. The diagram of the automaton is given in Fig. 2.9.

Eq. 2.43 contains one parameter which is not known *a priori*: $V_{store\ sat}$ is the saturation voltage of a freely running charge pump. This voltage is equal to $V_{res}C_{max}/C_{min}$ (cf.

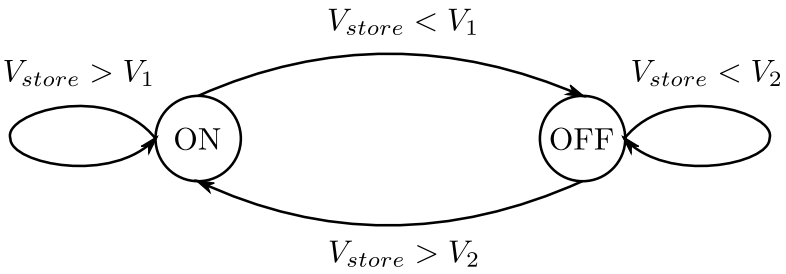


FIGURE 2.9: Finite state automaton driving the flyback switch.

section 2.3.2.2). Notice that this voltage is never present in the charge pump, since V_{store} evolves between V_1 and V_2. However, the calculation of V_1 and V_2 needs the information about $V_{store\ sat}$. The latter depends on the maximal and minimal values of the variable capacitor $C_{max,min}$, and by consequence, on the mobile mass displacement (cf. Eq. 1.2). The displacement of the mobile mass depends in turn on the amplitude of vibrations, which in real ambient environment may vary in time. Therefore, $C_{max,min}$ are not the fixed and known values. If the latter change, $V_{store\ sat}$ changes as well and the pre-defined parameters V_1 and V_2 are no longer optimal.

By consequence, the presented automaton should be supplemented by a mechanism estimating the current $V_{store\ sat}$ and calculating V_1 and V_2. This should be done periodically, in order to keep the circuit in the optimal mode all the time.

The idea of introducing a periodic calibration of the charge pump/flyback conditioning circuit is one of the main innovative contribution of this work, comparing to the state-of-the art at the time when this PhD project started.

2.5 Auto-calibration of the system

As we demonstrated by empirical Eq. 2.43, V_1 and V_2 are calculated as functions of two electrical parameters, V_{res} and $V_{store\ max}$. The latter can be considered as close to the saturation voltage $V_{store\ max} \approx V_{store\ sat}$. While V_{res} evolves slowly and can be easily measured, the determination of $V_{store\ sat}$ presents a challenge, since this voltage is never present in the circuit. Moreover, as we shown in the last subsection, $V_{store\ sat}$ directly depends on several external and internal factors: the acceleration amplitude and frequency of the external vibrations, the voltage applied on the transducer by the conditioning circuit (the electromechanical coupling phenomena). Thus, in practice it is not possible to know *a priori* the relation C_{max}/C_{min} in order to find the optimal V_1 and V_2 according to Eq. 2.43.

Regarding this issue, we propose to determine the saturation voltage of the charge pump without possessing information about C_{max}/C_{min}. We can do it by letting the charge pump reach the saturation from time to time, and considering that the voltage on C_{store} is $V_{store\ sat}$. In this way, the system can be periodically calibrated.

During each calibration, the charge pump is intended to measure indirectly the actual parameters of the external vibrations by generating the maximum V_{store}. Note that

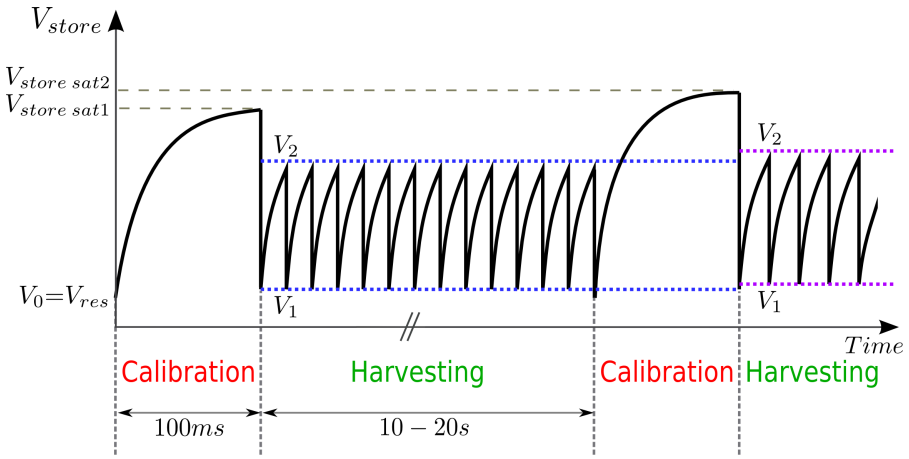


FIGURE 2.10: Example of auto-calibration of the VEH system : V_{store} evolves within V_0 and $V_{store\ sat}$ during periodically repeated calibration phases, and within updated V_1 and V_2 during harvesting phases.

the measured $V_{store\ max}$ can be lower or higher at different cycles depending on the C_{max}/C_{min} ratio, but of course on the internal electrical state of the system as well. Since during the calibration phase energy harvesting is not achieved, the calibration should be done rarely – once for many charge pump-flyback cycles. The actual frequency of calibration depend on the application context (quickly/slowly changing environment, etc.).

In this way, the circuit monitors periodically the environment, by repeated measurements of $V_{store\ sat}$. Subsequently, the operation parameters of the circuit are adjusted, and the circuit operates at the mode at which the energy conversion rate is maximal.

A typical behavior of the conditioning circuit with auto-calibration is presented in Fig. 2.10, where V_{store} plot is presented.

The measurement technique of the saturation voltage and a description of the auto-calibration is given below.

2.5.1 Technique of auto-calibration: a possible algorithm

This subsection proposes a description of a possible calibration process [Dudka09b]. This description can be used for building a system achieving the calibration. This is only one of the possible architectures implementing an adaptive behavior of the charge pump/flyback circuit. In particular, the presented architecture is compatible with an implementation on a digital controller.

Firstly, the charge pump is initialized (V_{store} resets to V_0). Thereafter, the flyback is deactivated and the charge pump is forced to run freely up to the saturation. During charge pumping, V_{store} is sampled. Each sample of V_{store} is temporary stored and compared with the previously measured value as shown on the voltage diagram in Fig. 2.11. As soon as the difference ΔV_{store} between two neighboring measured values of V_{store} becomes lower than a predefined minimal value, it is concluded that V_{store} is

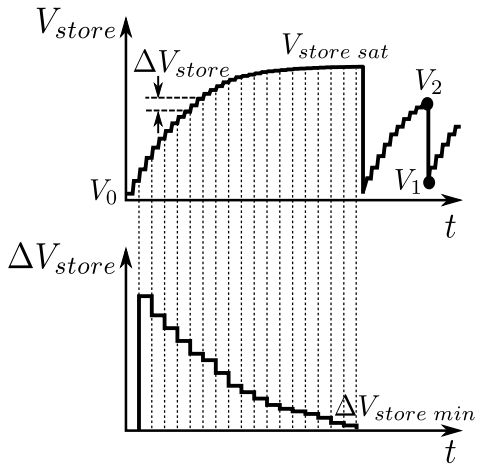


FIGURE 2.11: Voltage diagram illustrating the calibration technique.

saturated and the last measured value is considered as $V_{store\ sat}$. This process is just a digital derivation of V_{store} voltage, and a comparison of the V_{store} derivation with threshold. The obtained $V_{store\ sat}$ is used for updating V_1 and V_2. Hence, between two calibration cycles, the system operates with optimal V_1 and V_2 parameters.

To validate the proposed architecture, the auto-calibration algorithm has been modeled in VHDL-AMS. The corresponding VHDL-AMS model will be discussed in Section 2.7.4.2.

2.5.2 Demonstration of adaptive behavior

In this project, the proposed technique of auto-calibration is first realized as a behavior model. A modeling experiment tested the adaptability of the system to variations of parameters of external vibrations.

To demonstrate an auto-adaptive behavior of the system, we made a simulation experiment, where the acceleration amplitude of vibrations varies over time between 4 and 10 m/s^2 as illustrated in Fig. 2.12a.

Under these conditions we simulated two models of the system. Both of them uses Eq. 2.43 for the calculation of the thresholds V_1 and V_2. However, the one of them uses the auto-calibration which updates periodically $V_{store\ max}$, while another uses a fixed (predefined) value of $V_{store\ max}$. All other parameters/configuration were identical for the both models. In the simulation, we defined the external acceleration having a fixed frequency but the amplitude varying in time (Fig. 2.12a). The fixed value of $V_{store\ max}$ used in the first model was calculated for the external acceleration vibration amplitude of 10 ms^{-2}. Hence, the operation of the model is optimized only for this amplitude.

The average power converted at a vibration cycle by both models is plotted in Fig. 2.12b-c, where the plot (b) corresponds to a model with auto-calibration. It can be observed, that if the acceleration amplitude strongly decreases, the model without calibration can not generate a power, since the model parameters were adapted for a unique case of

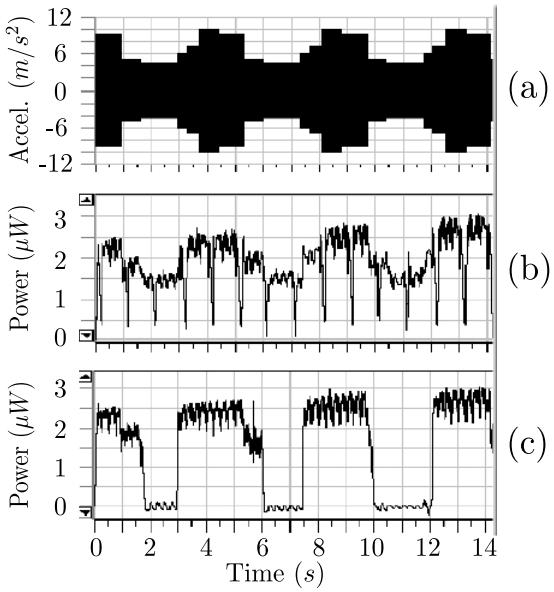


FIGURE 2.12: Comparison of the E-VEH system operation under variable acceleration amplitude of vibration (a) with (b) and without auto-calibration (c). Plots are issued from simulations.

acceleration 10 m/s^2. At the same time, the model with auto-calibration still generates power, as V_1 and V_2 were updated taking into account the actual reduced $V_{store\ max}$. Hence, this simulation example demonstrates that a systematic update of V_1 and V_2 by the use of auto-calibration concept proves the ability to adapt to the variation of the vibrations amplitude.

The periodic decreasing spikes observed in Fig. 2.12b correspond to the auto-calibration phases: during the calibration, no power is converted. It is equivalent to a loss of a part of energy. Moreover, the auto-calibration process costs some energy consumed by the processing electronics. By consequence, the frequency of the calibration should be as low as possible. On the other hand, a very low frequency (every tens, hundreds seconds) of the calibration may result in an undesired situation, when vibration parameters change right after the calibration, and the system operates in a suboptimal mode up to the next calibration. Moreover, such a low frequency may cause some problems in physical realization of the system, such as a long-term storage of V_1 and V_2 values without update.

The optimal frequency of calibration relies on two factors: the application context (the typical dynamic of the external vibrations) and constraints of the physical realization of the circuit. In a smart system, the frequency of calibration may also be a variable parameter whose value is chosen dynamically.

2.5.3 Smart adaptive flyback switch

Fig. 2.13 shows an idealized view of an adaptive conditioning circuit by employing a smart adaptive flyback switch. It incorporates a power-to-analog interface that senses

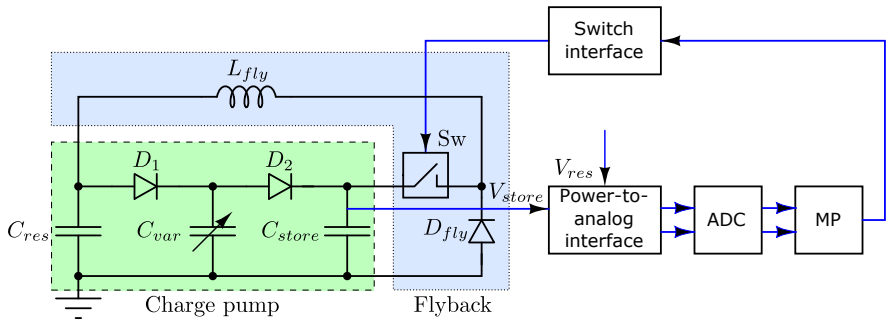


FIGURE 2.13: General architecture of a smart conditioning circuit that implements an auto-calibration.

and divides the voltages V_{res} and V_{store}, an analog-to-digital converter and a microprocessor performing the signals processing and control of the flyback switch through a switch interface (driver).

A low-power ADC has been studied and designed on transistor level by Raouf Khalil [Khalil10] during his PhD research in LIP6 in the framework of a SESAM project. The power saving of the ADC can be achieved by a successive approximation architecture, known as one of the best candidates in terms of power consumption [Scott03, Kwong08]. Designed in AMS 0.35 μm CMOS process, the 8-bit SAR ADC demonstrated a power consumption around 1.25 μW for one step of conversion (according to simulations). This estimation does not take into account the consumption related with purely digital blocks. Such a low power consumption is a very promising result for the use of SAR ADC in energy harvesting circuit. Regarding the low level of the converted power with available models of the transducers (practically of the same order) and considering that the microprocessor block is even more power hungry, the architecture given in Fig. 2.13 remains futuristic and we look forward to return to this structure in future.

An alternative solution to elaborate a smart control circuit consists in designing a purely analog circuit without the ADC and the power hungry digital processor. Hence, the complexity and the power consumption can be decreased at once. We envisage the signal treatment to be performed by analog calculator. The design of such an intelligent analog circuit with an extremely low power is one of the main objective of this thesis work and it will be presented in details in the next chapter. Prior to a transistor level design of auto-adaptive electronics, we made a design on a system level. This study comprises the development and optimization of the algorithm of auto-calibration, the choice of the architecture, behavior modeling, etc. Owing to this study we elaborated the specifications for a set of parameters for a circuit level design, such as the duration and frequency of the calibration phase, optimal coefficients for the calculation of V_1 and V_2, etc. We estimated the voltage limits of the system that are set by a transducer model (in fact, capacitive transducers have a voltage limit due to a pull-in effect that will be discussed later). More extensive results of our system-level study will be presented in section 2.7.

2.6 Power management of the harvested energy

Theoretical investigations presented in [Paracha08] highlight that the optimal power yield of the system requires a high voltage level on C_{res} (tens of volts), whereas the load is usually supplied by low voltages (e.g. 1−5 V). A smart power management must ensure the following functions:

- a high-to-low voltage interface between the harvester (C_{res}) and the load,
- a stabilization of the voltage supplying the load,
- a maintenance of the internal energy of the harvester at the level guaranteeing an optimal power conversion,
- cutting off the load when not enough energy is available for the supply, so preserving the harvester from de-energizing,
- "sleeping" mode of harvester, in a case if no external energy flow is available: the flyback is cut off, and the calibration is activated very rarely, in order to make the circuit wake up when external energy is available again.
- provide a power supply for the control electronic

As it was shown, the charge pump converts energy when its capacitors are charged to some voltages (V_{res}, V_{store}). Hence, it is important to not let the charge pump loose its energy: the cutting off and sleeping mode functions are intended for this purpose.

A simplified circuit diagram of the proposed intelligent e-VEH system is illustrated in Fig. 2.14. The core of a smart unit controlling four switches includes a smart adaptive flyback switch control unit and a power management unit controlling three additional switches, as discussed next. In order to supply the output load with a harvester, first, an additional capacitor C_{load} is added. This capacitor must be charged to a low voltage and is intended to store the energy immediately available for the load. Hence, a low DC voltage level on C_{load} must be generated from the high-voltage across C_{res}. In fact, high voltage V_{res} corresponds to a desired state of harvester operation when a large amount of converted energy has been accumulated on C_{res} given by $W_{res} = C_{res}V_{res}^2/2$.

To generate a low voltage on C_{load} from the high voltage on C_{res} a Buck DC-DC voltage converter may be used, which consists of an additional energy conversion stage. However, the basic architecture already contains a Buck DC-DC converter implemented by the inductor and the diode D_{fly} used in the flyback path, whose role is to transfer the energy from C_{store} capacitor to C_{res}. Proposed solution consists in reusing this DC-DC converter to charge C_{load} as well when it is needed. This is done by introducing a switch SW_2, which allows the inductor to discharge on one of two capacitors. The idea is to allow the flyback circuit return the energy not only to C_{res} capacitor, but to C_{res} or, alternatively, C_{load}. The theory [Paracha08] shows that for each external vibration parameters, there exists an optimal value of V_{res}. If, for example, V_{res} is higher than this optimal voltage, it should be quickly reduced. This is done by adding an additional switch SW_3, which allows C_{res} to discharge directly on C_{load}. The switch SW_1 is added

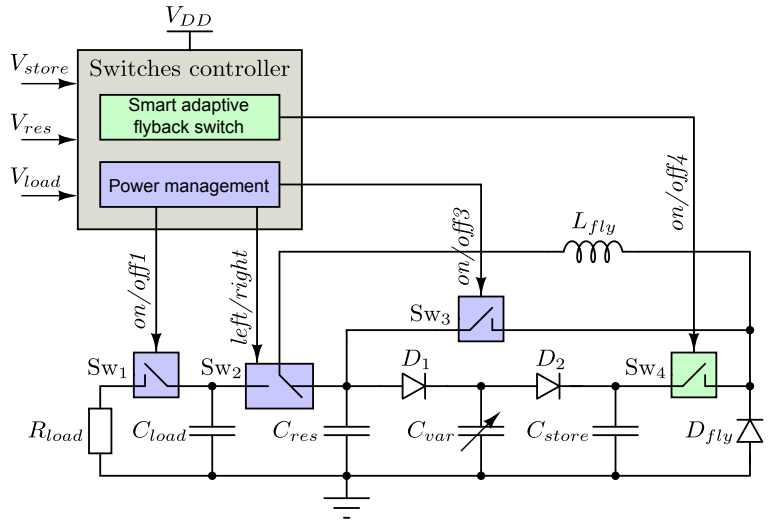


FIGURE 2.14: Conditioning circuit of energy harvester with power management control

to interface the load with the harvester. It allows disconnect the load from the generator, if the harvested power is low, hence, avoiding the discharge of capacitors C_{load} and C_{res}. The switches SW_1-SW_3 are supposed to be controlled by some smart electronics, which senses voltages V_{load} and V_{res} and which depending on the application and the nature of the load, implements some optimal power measurement strategy.

2.7 Modeling of the VEH system

2.7.1 Objectives

Nowadays, modeling occupies a very important place in design of electrical circuits and various heterogeneous systems, mainly, due to a cost for physical prototyping and complexity of systems, but also owing to the high power of calculators and the advancement of computer-aided design (CAD) tools, which become more and more reliable and sophisticated. In our work, we faced difficulties in theoretical study of the VEH that is a consequence of a multidisciplinary nature of the system. Our motivations for modeling can be summarized as follow.

- *Exploration of the system.* Behavior description and simulation of the system is a perfect way to virtually test the VEH operation in particular context with a relatively high level of realism. Owing to modeling we expect to better understand the system operation under various particular conditions, develop an optimal scenario of energy harvesting, elaborate a smart architecture of the system, determine the factors limiting its operation in both mechanical and electrical domains, etc.

- *Design of the system and its blocks.* The common approach of systems design is a so-called "top-down" methodology. First, the architecture of the system is defined as a block diagram with simulation and optimization on a high abstraction level.

> From the high-level simulation the performance requirements for the individual circuit blocks are derived. Circuits are then designed individually on a low level of electrical components to meet these specifications. Finally, the entire chip is laid out and verified against the original requirements.

Specification for modeling of MEMS devices can be provided only by the designers of these devices. In our project two MEMS devices were fabricated and characterized by our colleagues - the group of P. Basset in ESIEE Paris. Each device constitutes a resonator and an associated capacitive transducer with divers structures and parameters. We have developed macro-models of these devices in order to use them in a global model of the harvester, including the model of conditioning circuit.

Prior to perform the modeling of the system, the choice of a suitable platform for modeling must be made.

2.7.2 Choice of modeling platform

In the beginning of our study, we faced the problem of a choice of a modeling tool that satisfy our requirements regarding the accuracy of modeling, simulation speed, simplicity, etc. A comparative study of three different platforms for VEH modeling has been done in 2008 by a student Ken Caluwaerts associated to our lab in a framework of his master internship. The conventional Yen's conditioning circuit has been modeled in Matlab/Simulink, SyctemC-AMS and AdvanceMS platform of Mentor Graphics.

Owing to its open-source and its fast development, SystemC-AMS manifests a great interest of a waste community of analog/mixed signal circuit designers. As we discovered by a study of Ken is that the actual version of the platform of SystemC-AMS was poorly adapted to precise simulation of non-linear physical systems, such as a VEH system, due to a limited number of methods to solve non-linear equations. In fact, the platform of 2008 version[1] used the integration methods with a fixed temporal step. That was a factor limiting the simulation of systems operating simultaneously at multiple time scales like VEHs do.

The platform AdvanceMS developed by Mentor Graphics allows mix together various models such as VHDL-AMS (analog behavioral), VHDL (digital), ELDO (the Mentor Graphic's variation of SPICE). Moreover, this platform offers a large gamma of digital methods to solve complex equations [Pêcheux05]. The user graphical interface is much more comfortable than of two other platforms. Finally, the AdvanceMS platform is basically intended for integrated circuit designers who wish to account the system-level aspects during the circuit design. This was exactly our position: the actual objective of our project is a design of a silicon prototype of a smart conditioning circuit. For these reasons, AdvanceMS platform was chosen for the modeling, simulation and design of our VEH system.

[1] Since 2008, the platform SystemC-AMS has been greatly improved, while our experience on this tool has not been updated.

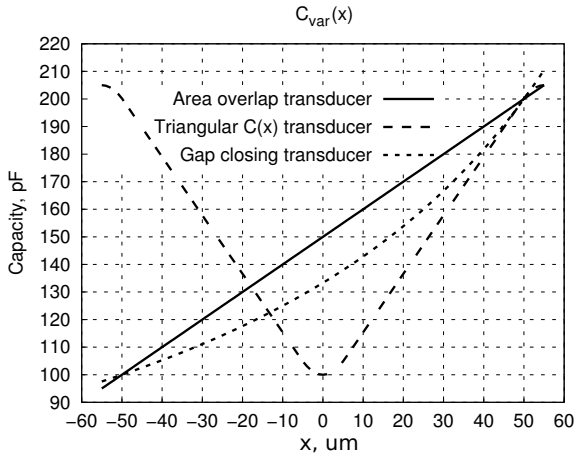


FIGURE 2.15: Examples of capacitance C_{var} variation versus the proof mobile mass displacement x.

2.7.3 Model of MEMS resonator/transducer

Modeling of the resonator and transducer, which constitute the mechanical part of the e-VEH system, is based on measurement results of the real MEMS devices, area overlap [Basset09] and gap closing [Guillemet13]. The behavior models of both of them are described using VHDL-AMS language and modeled through ADvanceMS environment.

As a MEMS device operation occurs simultaneously in mechanical and electrical domains, it is modeled using mechanical and electrical physical equations taking into account the geometry of a real device. The MEMS generator can be modeled as a second-order damped resonator and as a capacitive transducer associated with its mobile mass. The mobile mass is mechanically coupled with the external system (submitted to external vibrations) by the spring which allows a transmission of the external vibrations towards the mass. Hence the model takes into account the inertial properties of the resonator, which is modeled according to the Newton law equation:

$$f_{tran} - ma_{ext} - kx - \mu\dot{x} = m\ddot{x}, \tag{2.44}$$

where k, μ and m are the stiffness, damping coefficient and the proof mass of the resonator, respectively, x is the displacement of the mobile mass, a_{ext} is the acceleration of the external system characterizing the external vibrations and it is a unique input signal of the model. $-ma_{ext}$ is the force of external vibrations affecting the mass through the inertia mechanism. The capacitive transducer generates on the mass a force f_{tran} that represents a coupling between the mechanical domain (resonator) and the electrical domain (conditioning circuit), and it is expressed as:

$$f_{tran} = \frac{1}{2}{V_{var}}^2 \frac{dC_{var}}{dx}, \tag{2.45}$$

where V_{var} is the voltage applied on the transducer. The function $C_{var}(x)$ characterizes the relation between the transducer variable capacitance and the position of its movable electrode, and it depends on the geometry of the transducer. Examples of $C_{var}(x)$ function is plotted in Fig. 2.15. Notice that the frequency of variation of the capacitance

f_{elec} is not necessarily the same as the frequency of the mobile mass displacement f_{mec}, in case when the function $C_{var}(x)$ is not monotone (e.g. for the gap closing transducer, cf. Section 1.6).

The electrical behavior of the transducer is described following usual capacitance equations:

$$i_{tran} = \frac{dq_{tran}}{dt}, \qquad q_{tran} = C_{tran}(x)V_{tran}. \tag{2.46}$$

Here q_{tran} is an electric charge on a variable capacitor, i_{tran} is a current through it. Equations 2.44–2.46 are directly put in VHDL-AMS model.

The resonator model also contains mechanical stoppers limiting the mass displacement by ± 50 μm (the scope of the plot in Fig. 2.15). Stoppers are modeled as highly viscous walls:

$$f_{stoppers} = -\mu_s v, \qquad \texttt{if} \ \ |x| > 50\mu m, \tag{2.47}$$

where μ_s is the viscosity, v is the velocity.

Detailed models of MEMS devices are given in Ph.D. thesis of Ayaaz M. Paracha [Paracha09a] (area overlap) and Raphaël Guillemet [Guillemet12] (gap closing). The VHDL-AMS models of in-plane area overlap and gap closing transducers are given in Appendix A.

The modeled devices have one non-conservative input terminal (external acceleration quantity) and two conservative electrical terminals. No one model contain "output" quantity: it is a dipole, which behaves like a variable capacitor, whose instantaneous capacitance relies on the external acceleration, the dynamics of the mechanical system and the applied electrical voltage.

2.7.4 Model of the flyback adaptive switch

The presented in Section 2.5.1 technique of auto-calibration is described using VHDL-AMS language. The model consists of two parts: a state-driven electrical switch and a "brain" of the switch - the auto-calibration module providing an optimal and adaptive behavior of the whole VEH system. This model implements a two-terminal electrical switch, which can be integrated into existing VHDL-AMS/ELDO model of the conditioning circuit [Galayko07], as shown in Fig. 2.16.

2.7.4.1 State-driven electrical switch

The switch model contains a one-bit memory register, since it stores its binary state - "*on*" or "*off*". Depending on the state, the behavior of the electrical switch is described by the Ohm's law:

$$\begin{cases} V = R_{on} I, & \texttt{if} \ \ on = \text{"1"}, \\ V = R_{off} I, & \texttt{if} \ on = \text{"0"} \end{cases}, \tag{2.48}$$

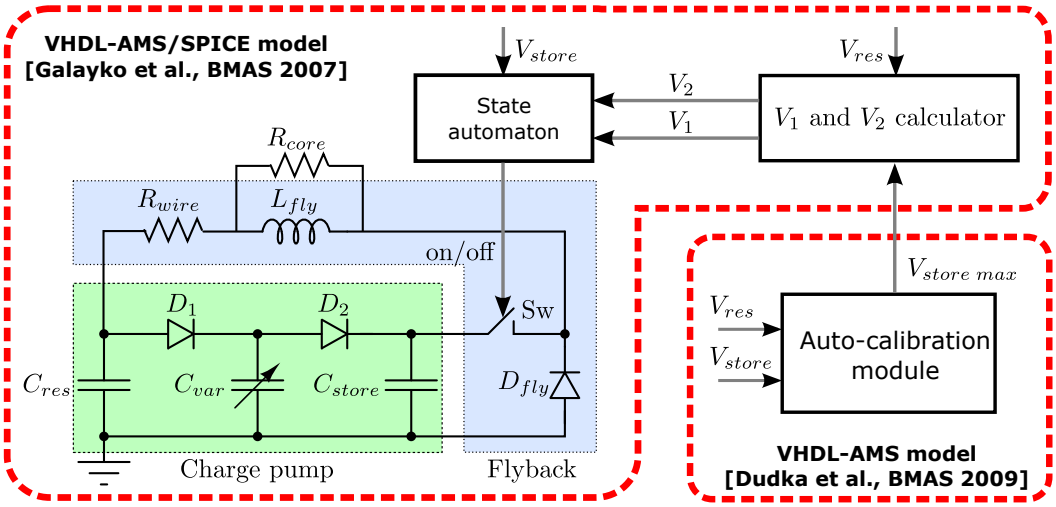


FIGURE 2.16: General model of the harvester developed in LIP6 with illustration of the modeling tools.

where V and I are the switch voltage and current, and R_{on}=10 Ω and R_{off}=1 GΩ are the resistances for on and off states.

2.7.4.2 Auto-calibration model

The model has two input parameters: V_{res} and V_{store} that are used for calculation of switching parameters V_1 and V_2, as described by the algorithm in Section 2.5.1. The structure of the switch model, including both parts (electrical switch and calibration module) is illustrated in Fig. 2.17. It is composed of two functional blocks and uses five processes. The model employs two clocks being generated internally: a slow clock (clk) provokes periodic calibration cycles, and a fast clock (clk_m) is used for V_{store} sampling during the calibration.

The calibration block includes four processes. When the signal clk goes high (**Process 1**), the process that resets V_{store} is activated (**Process 2**). It measures V_{store} and if it is far from V_{res}, V_{store} voltage is reset to V_{res}. After V_{store} is initialized, $V_{store\ max}$ measurement starts in the **Process 3**, and $V_{store\ max}$ is being detected as it was explained in Section 2.5.1. Simultaneously, the **Process 4** calculates V_1 and V_2 values that means the end of the calibration cycle. The calculated V_1 and V_2 values are the input signals of the switching block. In this model, V_1 and V_2 are updated only at the end of the calibration cycle and are kept constant up to the next calibration.

The switch control is implemented in the **Process 5**, which in fact, describes the state automaton. This process is always active. It detects the events of V_{store} crossing V_1 and V_2 and generates "on/off" switching events which, in turn, drive the electrical state of the switch.

The listing of the VHDL-AMS model is given in Appendix B.

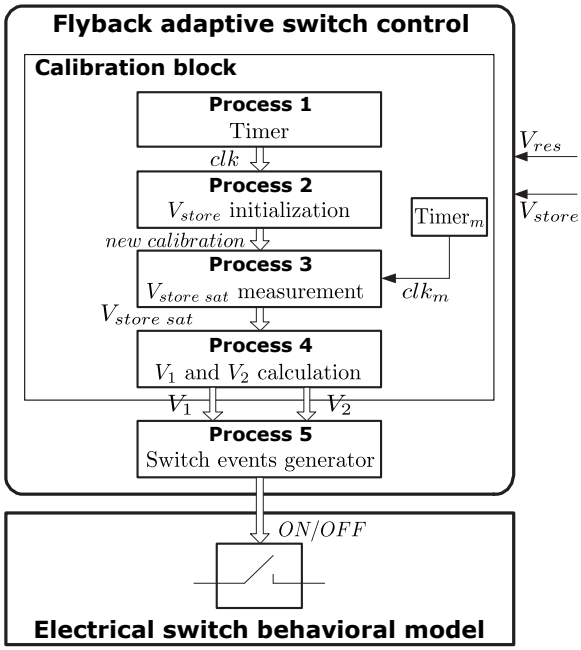


FIGURE 2.17: Calibration algorithm implementing a smart adaptive behavior of the conditioning circuit.

2.7.5 Diodes modeling

Until this work, in the analysis of the system the diodes were idealistic. Now, in modeling the whole system we take into account the properties of realistic diodes. For this, we created the diode model (VHDL-AMS) that behaves following the exponential law and have a realistic threshold voltage.

2.7.6 Inductor modeling

The flyback inductor is modeled using a standard component from a component library of Spice. In order to account the inevitable losses in a real inductor associated with the core and winding, we modeled the inductor together with the wire resistance in series and a core resistance in parallel. Values of parasitic resistances were chosen according to the real inductor from data-sheet. Thus, for a 15 mH inductor (*Murata, 1300R series*) the wire-wound serial resistance R_{wire} (cf. Fig. 2.16) is 31 Ω. The value for the core resistance R_{core}, being unavailable in the datasheet, is chosen as 360 KΩ according to measurement results of an inductor of a quite similar size provided in [Mur-Miranda04]. Capacitive effects, considerable for radio frequency applications, were not took into account since the electrical charge transmission frequency is much lower.

2.7.7 Simulation of the proposed E-VEH system

In this section we provide a few simulation experiments of the global e-VEH system-level model and discuss the obtained simulation results. The main goal of the first experiment

is the validation of the auto-calibration concept under variable parameters of external vibrations. The goal of the second experiment is the validation of the proposed system with a power management of the harvested energy and the interface with the load. Both simulations have identical parameters of the conditioning circuit : C_{res}=1 μF, C_{store}=1 μF, the maximum C_{var} variation ratio is C_{max}/C_{min}=144/73 pF, the flyback inductance L_{fly}=15 mH, the parasitic wire resistance of the inductor is 31 Ω.

2.7.7.1 Validation of the auto-calibration concept

In order to validate the proposed auto-calibration technique we simulated the general e-VEH system presented in Fig. 2.16. Here, we illustrate a simulation experiment, which aims a comparison of two VEH configurations under conditions of variable vibration amplitude. One configuration includes an auto-calibration module, which periodically measures the saturation of the charge pump $V_{store\ sat}$, and another one is a basic configuration in which $V_{store\ max}$ is pre-calculated following Eq. 2.43, 2.19 under hypothesis of constant and known parameters of ambient vibrations. Apart different models of the flyback switch (conventional and auto-calibrated), the rest components of the system model are identical. The initial voltage of the charge pump capacitors is V_0=7 V. Both configuration do not include nor output voltage control (i.e. power management block and associated switches, cf. Section 2.6), neither load resistor. Acceleration amplitude of vibrations varies in time discretely using a piece-wise function within 2.5 and 10 m/s^2 identically for both simulations. The frequency of vibrations is 298 Hz. The calibration repeats every 5 seconds in this example (for the demonstration purpose), however, in reality it is supposed to repeat rarely.

Fig. 2.18 presents the simulation results of both harvester models operated during 315 s. Both systems start with the same initial energy (7 V on C_{res} capacitor). The upper plot shows the acceleration of external vibrations A_{ext} varying in time, which is an input mechanical signal for both models. The variable capacitance response to the external vibrations is plotted below. The maximal capacitance value is fixed by a geometry of the transducer model at 144 pF, while the minimum value depends on the applied mechanical force, or acceleration (i.e., the higher is A_{ext}, the lower is C_{min}, and vice versa). When the acceleration amplitude significantly decreases, and hence so does the ratio C_{max}/C_{min}, it can be observed that no power can be produced by a system without the calibration (red curve) as shown in the bottom plot, while the power is still produced by the auto-calibrated system even if it is reduced. This can be explained as follow. Due to the reduced ratio C_{max}/C_{min}, the new $V_{store\ max}$ value (Eq. 2.19) is less than the limit value V_2, hence the flyback circuit can not be activated. In this sway the charge pump is saturated, since it is not capable to increase V_{store}, as can be observed on the third plot by a straight red line (non-calibrated system). As the flyback can not be activated, C_{res} can not be replenished and its voltage remains constant as illustrated on the fourth plot. On the other hand the auto-calibration technique allows update periodically V_2 and V_1 taking into account the actual ratio C_{max}/C_{min} and not pre-defined. The calibration phases can be observed by periodic spikes of V_{store} (blue curve).

Over equal time (315 s) of VEHs operation, the auto-calibrated system accumulated more energy than its counterpart as can be seen by the voltage level on C_{res}: in the auto-calibrated VEH V_{res} rises from 7 to 17.2 V, while in the non-calibrated system

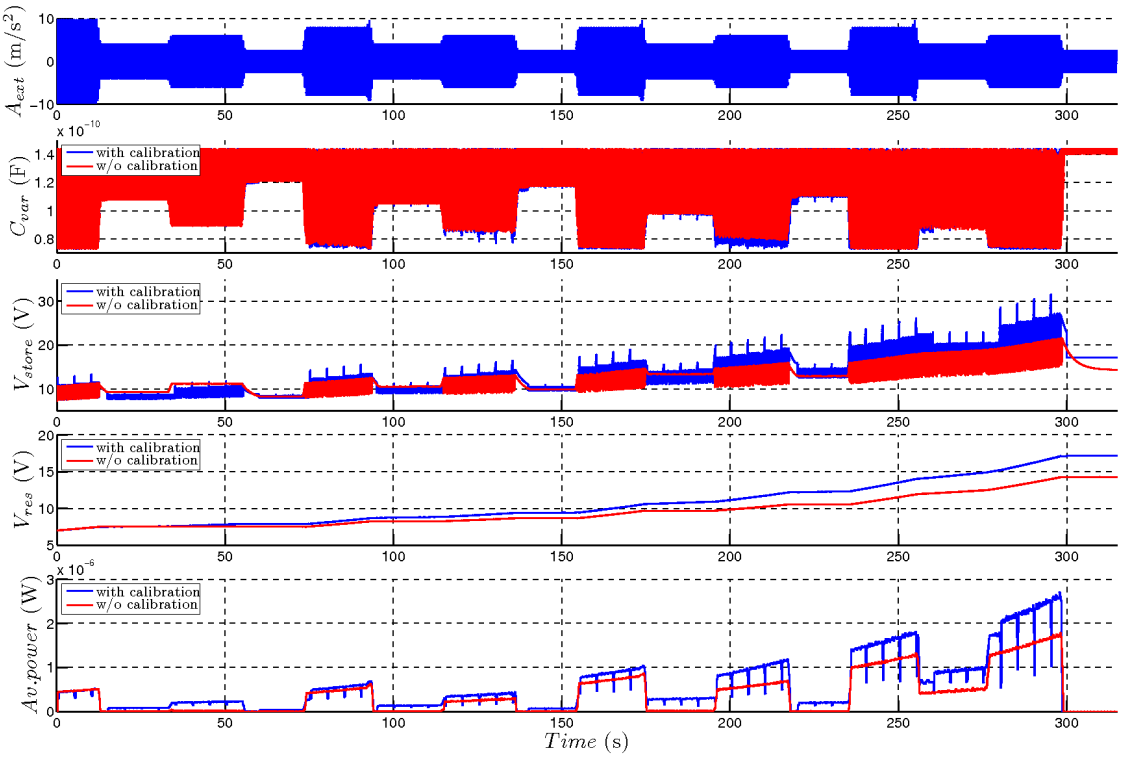


FIGURE 2.18: Simulation results of two e-VEH models (with and without auto-calibration) submitted to identical vibrations parameters with the variable acceleration amplitude.

- to 14.5 V. The difference is due to non energy harvesting in non-calibrated VEH during the moments when the acceleration amplitude is low. The maximum average power per 100 ms obtained from simulations for calibrated and non-calibrated system is 2.8 and 1.8 μW, respectively. It can be noticed that after 300 s the variation of C_{var} becomes very small and, as a result, neither model can operate properly to produce power. This occurs due to a pull-in effect, which is inherent when the electrostatic force is greater than the mechanical force, that happens when a high voltage is applied to the capacitance.

The "pull-in" phenomena is a common effect for electrostatic microactuators (e.g. MEMS devices) and it is summarized as follow. When voltage is applied across the capacitance, electrostatic force works to reduce the plate separation. At small voltages, the electrostatic voltage is countered by the spring force, but as voltage is increased the plates are eventually snap together.

2.7.7.2 Example of power management of the harvested energy

We created and simulated a model of the conditioning circuit architecture shown in Fig. 2.14, which incorporates the control block for all switches, including a power management module and an auto-calibrated flyback switch. Each model of the switch is implemented as an instance of the block electrical switch behavioral model (cf. Appendix B) with an individual control algorithm implemented in a power management

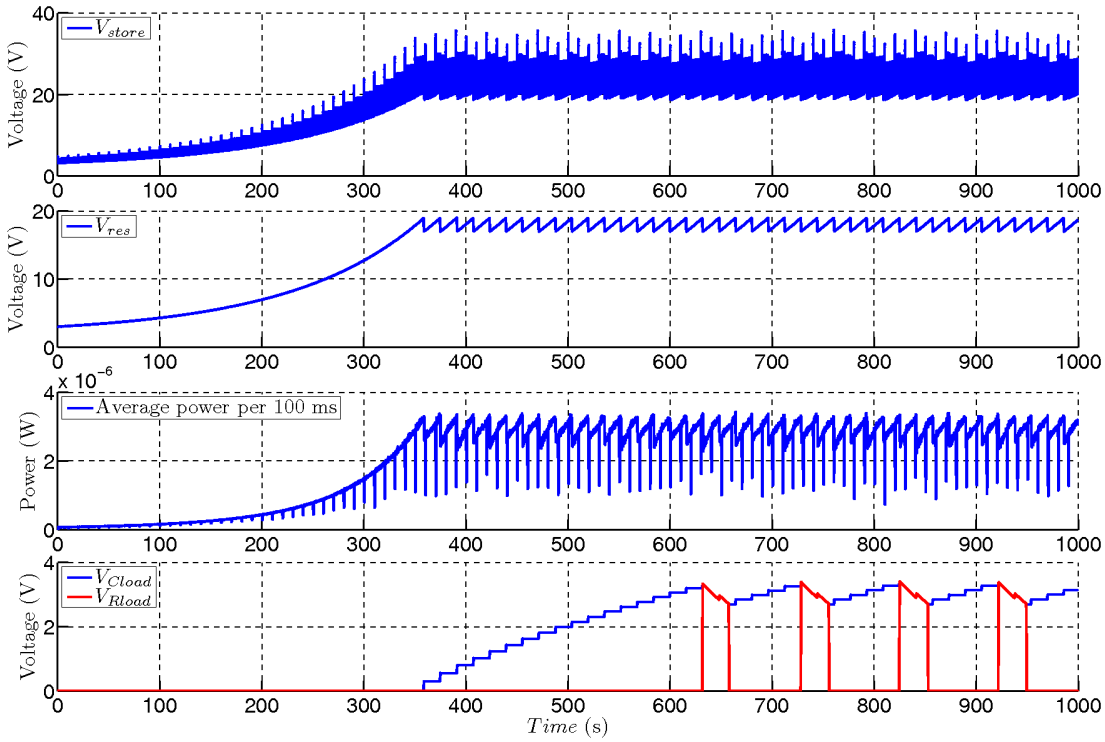


FIGURE 2.19: Simulation results showing an example of a long-term operation of a smart e-VEH system including the power management and the auto-calibration.

control block. Electrical switches are driven by corresponding *on/off*$_i$ and *left/right* (for SW_2). The simulation parameters for this experiment are the same as in previous example (cf. Sec. 2.7.7.1), apart the the following setup parameters: initial voltage V_0=3 V, the amplitude of acceleration is constant 10 m/s^2, the calibration repeats every 10 seconds. The load capacitance C_{load} is 50 μF (50 times greater than C_{res}), the load resistance is 2 MΩ.

Simulation results of a long-term simulation (1000 s) plotted in Fig. 2.19 highlight three strategic stages of functioning of the system: establishment of the mode of sustainable energy harvesting, setup of the output voltage on the desired level claimed by the load, and periodic commutation of the load without direct impact on the harvested energy. Detailed description of obtained results is given below.

The system starts from the state corresponding to a zero energy in C_{load} and a small amount of energy initially stored in C_{res} (about 70 nW), given by V_{res}=3 V. The positions of the switches is as follow: SW_1, SW_3 and SW_4 are *off*, SW_2 is *right*.

The first stage lasts about 355 seconds and corresponds to the accumulation of the converted energy in C_{res} needed for a sustainable high power generation. During this stage only the flyback switch SW_4 is being periodically activated, thus V_{res} rises from 3 V to 19 V, which is slightly below the pull-in voltage.

At the second stage when V_{res} reaches 19 V, in order to avoid the pull-in effect the voltage V_{res} is slightly reduced. This is done by activating simultaneously switches SW_2 in a position *left* and SW_3 in a state *on*. In this way, a part of all charges stored in C_{res}

and the extra energy begins to be transferred toward C_{load}. This transfer is very quick comparing to the average rate of V_{res} evolution, and immediately after this, V_{res} reduces from 19 to 17 V. So V_{res} starts to evolve periodically between 17 and 19 V providing an increased average power per 100 ms between 2.6 and 3.4 μW, respectively. At the same time the voltage on a large load capacitance V_{Cload} slowly increases every time V_{res} reaches 19 V.

The third stage starts as soon as the C_{load} is charged to 3.3 V (at 625 second). The switch SW_1 connects the load R_{load} in parallel to C_{load}. The voltage across the load continuously reduces. Since in this example R_{load} consumes more power (about 5 μW) than the harvester generates (less than 3 μW), the load is periodically disconnected in order to save the harvested energy. To keep the output voltage in a specific range between 2.7 and 3.3 V, when V_{Cload} decreases to 2.7 V, the switch SW_1 turns off disconnecting R_{load} from C_{load}, until the energy on C_{load} is being replenished (voltage re-increases to 3.3 V).

This simulation illustrated one possible scenario of the global e-VEH operation, which constitutes our general vision of the system behavior. However, any other power management strategies may be implied on the proposed architecture, which silicon implementation is a subject of our future work. One of the possible suggestion, is the elaboration of a circuit with a possibility of tuning the output voltage level according to the requirements related with the nature of the load. Also a rectification technique may be used to generate a stable output DC voltage.

2.8 Summary

This chapter presented the general view of the system of electrostatic vibration energy harvester, being focused mainly on the conditioning circuit. We demonstrated that the circuit of Yen proposed in 2006, consisting of a charge pump and an inductive flyback return, still is very rich of problems to be studied, many factors and parameters to be analyzed and optimized. This may lead to possible improvements either in terms of architecture, or operation strategy. In other words, the circuit is considered as a base, to which various optimization strategies can be implied, tested and compared regarding the efficiency of energy harvesting.

Our study of the Yen's conditioning circuit suggested two levels of optimization. On the first level, we determined the optimal zone for the circuit operation, where the harvester should continuously behave so to generate maximal power. On the second level, we made the harvester to determine the optimal zone by itself owing to periodically repeated calibrations. This technique allows the harvester automatically adapt to the environmental fluctuations, when the vibration parameters (e.g. acceleration) vary in time slowly (i.e. not chaotically, but smoothly with a very low frequency, e.g. 0.001-1 Hz). This smart adaptive scenario of VEH functioning allowed the system optimized energy conversion in realistic (continuously altering) conditions that has been confirmed by a behavior simulation. In fact, behavior description of the system constituted our first step for the design of the electronics managing the VEH operation, allowing validate the proposed optimization strategy and create specifications for a circuit level design.

Additionally, we developed an architecture of the power management of the harvested energy and described it in a VHDL-AMS model. As the architecture is developed, various operation strategies can be applied to it, depending on the application and requirements. An example of using the developed power management was proposed. As simulation results shown, when the VEH has accumulated a sufficient energy needed to generate a high power level, a part of this energy can be used to replenish the output accumulator establishing a regulated specified voltage for the load. And this is done with only slight perturbation of the energy conversion process.

Chapter 3

High voltage IC design of a smart flyback switch

3.1 Overview

This chapter presents our investigation in a circuit-level design of the conditioning circuit for the e-VEH. The designed circuit implements a high-voltage smart flyback switch which operates according to the developed auto-calibration algorithm. The proposed IC can therefore be considered as the 'brain' of the capacitive energy harvester based on charge pump/flyback conditioing circuit. The passive elements constituting the charge pump/flyback (C_{res}, C_{store}, L and the diodes D_1, D_2 and D_{fly}, cf. Fig. 2.1) are not included in the designed IC. Because of their large values, they should be realized off-chip.

In the prototype circuit presented by Yen and Lang in 2006 [Yen06], the flyback switch was implemented as an n-channel MOSFET transistor driven with a source-referenced clock. However, such a gate drive is undesirable because the floating high-voltage reference makes the implementation and control strategy difficult. In this work we propose to use a high-voltage PMOS switch controlled by the ground-referenced low voltage levels, with the use of a low-to-high voltage level shifter. The design of the flyback switch must be done with a lot of care, since its configuration determines the control circuit complexity and the power consumption. The proposed high-voltage switch and its controller design is done with an emphasis on ultra low power specifications combined with the challenge of high voltage requirements.

The structure of this chapter is as follow. First, we demonstrate the general system that we are going to implement on chip, then we discuss the constraints and specification for the design, then we present the technology process used for the on-silicon circuit integration. After that, we detail the design of the high-voltage flyback switch in a hybrid high voltage/low voltage IC technology. Then we present the design of the flyback switch controller, which implements the auto-calibration of the conditioning circuit. The chapter ends by discussing simulation results of the designed integrated circuit in the context of the developed model of the complete harvester system.

3.2 Conditioning circuit intelligence: a complexity challenge

The study presented in chapter 2 highlighted a need in smart functions in energy harvesting circuits.

First, a specific module implementing a smart behavior of the flyback switch must be developed. It is supposed to collect the data from the conditioning circuit, to perform a data treatment, to make a decision, etc. However, the supply power available for such a complex functional unit is very small (max. few microwatts), and this constraints increase the complexity of the design and of electronic circuits.

Second, interfacing a low voltage load with a high voltage capacitive vibration energy harvester requires a load control/interface unit with a smart behavior. It must monitor the voltage and energy in the harvester and the load, and automatically supply the load with a specified voltage under condition that a sufficient converted energy is accumulated by the harvester.

Ultra low power available for supply the control blocks of the microscale energy harvester is the main challenge associated to the design of these blocks. Indeed, they are supplied with a part of the energy extracted from vibrations, typically equal to few microwatts or, at best, few tens of microwatts. In the context of capacitive energy harvesters, a low power design is complicated as the conditioning circuit is supposed to operate at high voltages required for the transducer biasing.

In this PhD project, we propose the transistor-level design of the circuitry associated with the smart flyback switch, leaving the implementation of the load interface for further works. This chapter exposes the main steps of this design.

3.3 General system

Fig. 3.1a illustrates a simplified functional block diagram of the proposed e-VEH system. The system is composed of the following parts:

- a MEMS transducer variable capacitance C_{var};
- an off-chip Yen's conditioning circuit (CC) including the *charge pump* and *flyback*;
- an integrated flyback switch SW that will be discussed in section 3.6;
- an integrated *control circuit* of the flyback switch that will be discussed in section 3.7;

As we stated before, the charge pump is intended to provide the high-voltage operation for the electrostatic transducer in order to convert higher amount of energy. In order to monitor the behavior of the charge pump and to drive the flyback switch, the designed control circuit must support high voltages as well. However, in order to reduce the power associated with the "smart" functions (the switch control sequence generation), the corresponding blocks should be implemented with low voltage circuits.

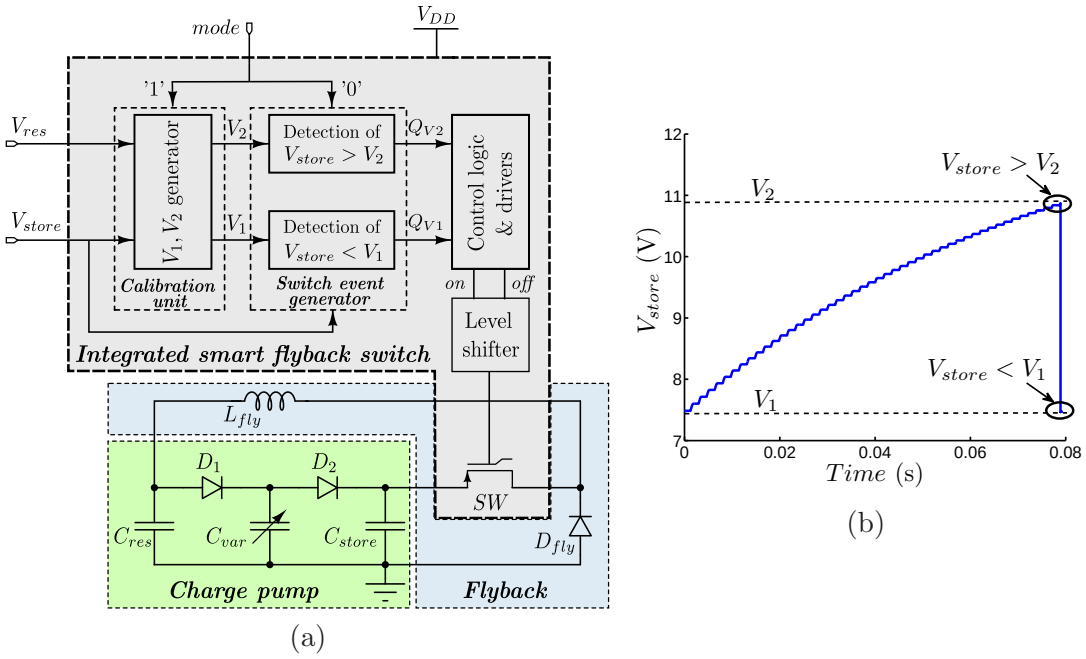


FIGURE 3.1: (a) Functional block diagram of the proposed e-VEH with a smart flyback switch; (b) typical V_{store} curve highlighting the generation of switching events by crossing V_2 and V_1 during the charge pump and flyback, respectively.

For these reasons, the smart flyback switch is implemented on silicon using a hybrid high voltage/low voltage integrated circuit technology, allowing an incorporation on a single chip of low and high voltage blocks. The low voltage (LV) part has two functions:
- determination of the flyback switching events;
- generation of the digital control signals for the switch.
The high voltage (HV) part is required for:
- realization of the HV flyback switch device;
- interface between the LV controller and the HV conditioning circuit.

The power switch is realized as a high side high voltage MOSFET switch. To drive it with a digital logic, a subsequent stage is required to shift the level of the digital signal from the ground to the floating high-voltage source. The integrated design and implementation of a power-efficient level shifter driving the high-side PMOS switch will be discussed in details in Section 3.6.

The controller for the flyback switch performs two tasks. First, during the calibration phase it determines the optimal zone for the charge pump functioning. This is achieved by measuring the saturation of the charge pump and subsequent calculation of the bottom V_1 and the top V_2 limits of this zone, as illustrated in Fig. 3.1b. Secondly, during the harvesting phase the controller keeps the charge pump operating within the pre-defined optimal zone as was illustrated in Fig. 2.10. This is achieved by regular monitoring of V_{store} evolution and generating the corresponding switching events for the flyback switch when the limits of the zone are reached. The full discussion of the controller operation and design will be given in Section 3.7.

The structure of the integrated smart flyback switch is as follow:
- the calibration block;
- the ***Detection of*** *'$V_{store} > V_2$'* block;
- the ***Detection of*** *'$V_{store} < V_1$'* block;
- digital control logic and drivers;
- voltage level shifter - power HV PMOS switch.

Since the integrated circuit consists of the low- and high-voltage sections, the circuit has two different voltage supplies. In this work, the LV section is supplied from the external "infinite" energy source V_{DD}. We make this assumption at a first stage in order to test the feasibility of the proposed system prototype. In our future designs, however, this source must be achieved with a battery regularly replenished with the harvested energy. The HV section is powered with the highest voltage in the system – the storage capacitor voltage V_{store}.

3.4 Constraints and specifications

Hereinafter we summarize the main specifications for the design that we get from the system-level simulations and that are constrained by the CMOS technology, which the choice of is discussed later.

The conditioning circuit must start its operation from a low pre-charge voltage, which can be provided with some external source, such as the battery or a piezoelectric generator. Typically, electrostatic generators can operate starting from 3-4 V. Therefore, 4 V would be our bottom limit for the charge pump operation. Looking ahead, the CMOS technology chosen for the design allows the maximum voltages up to 50 V for the HV transistors and 3.3 V for the LV transistors. In our design, we fixed the maximum voltage not to exceed 30 V, since the very large voltage range may cause substantial design complexity. Hence, for the feasibility of our first prototype we limited the charge pump voltage within the range $3 < V_{store} < 30$ V.

The design of the flyback switch has to deal with severe constraints in power consumption. In order to specify the maximum acceptable power consumption of the circuit, let us estimate the converted power with expression Eq. 2.26 derived in Chapter 2. If we suppose that the variable capacitance is charged with 30 V and it varies in between 150 and 300 pF with a frequency 300 Hz, the maximum converted power is 10.1 μW. This factor can be improved by rising the capacitance variation ratio and/or increasing C_{min}. Comparing to the estimated generated power, the maximum consumed power by the flyback switch with it control electronics should be considerably lower, at least a few microwatts.

In next section we presents the main characteristics of the CMOS technology that we used for the integrated circuit design.

3.5 CMOS technology considerations

The process H35, a CMOS 0.35-μm technology with a high voltage option of Austria Microsystems, is the most appropriate choice for our project: (i) it provides the required component set (high and low voltage transistors, MIM capacitors), (ii) this is a relatively old and very mature technology, with reliable component models, a stable and simple in use Design Kit, and huge design experience accumulated by the community. The technology generation node 0.35-μm offers a good compromise between the power directly consumed by the low voltage circuits (defined by the supply voltage, 3.3 V here) and relatively low leakages, also impacting the global power consumption.

H35 is a so called 2P4M process, which means that two poly-silicon layers and four metal layers are provided for the layout designer. The fourth metal layer is a thick power metal layer necessary for integrated circuits that must handle high currents. H35 offers fully scalable SPICE low- and high-voltage NMOS and PMOS devices, parameterized cells (Pcells) both for core CMOS and HV devices, as well as a best-in-class power-on resistance. For its fully automotive and medical qualified process, AMS delivers its industry benchmark design environment ("HIT-Kit"). H35 technology was released in early 2004 and nowadays it is a mature technology, which comes complete with IO libraries and special utilities optimized for high-voltage CMOS product design. Moreover, the H35 process design kit (PDK) offers a variety of design rule verification routines for ESD and latch-up, which enable robust high voltage design.

The main characteristic values and technology features are assembled in Table 3.1.

The core technology is based on thin-gate oxide 3.3V transistors with a minimum channel length L of 0.35 μm. Furthermore, the process family possesses the 5V and 20V gate modules (5V mid-oxide for LV and HV transistors and 20V thick-oxide for HV transistors).

The two available polysilicon layers (Poly1 and Poly2) are used to layout Poly1-Insulator-Poly2 (PIP) capacitor CPOLY.Since the resistivity of polysilicon is approximately 100 times higher then the resistivity of metal, its equivalent shear resistance is also high. CPOLY characteristics are therefore far away from ideal capacitor. However, CPOLY occupies less area then MOS capacitor of the same capacitance value.

The NMOS and PMOS transistors are also available in isolated wells.The advantage of using such type of transistors is that they have a reduced substrate coupling. During their switching, the substrate voltage swing is lower compared to non-isolated transistors and therefore such transistors provide better electromagnetic interference shielding and better noise performance when used in sensitive analog circuits. In our design we will use the thin-gate oxide 50V-transistors NMOS50T and PMOS50T with the following process parameters: The high voltage extension provides supplementary transistors able to support drain-source voltages up to 50 V. However, HV transistors have several limitations that can severely affect the analog design. First, they require a longer channel length L to achieve a high breakdown voltage, which results in higher ON channel resistance R_{ON} and higher gate charge Q_G. The consequence is a higher power dissipation because of significant conduction and switching losses. Another limitation is that all

TABLE 3.1: Characteristics of AMS H35 technology.

Technology	CMOS 0.35μm H35B4D3
Number of Masks	27
Substrate Type	p
Maximum Die Size	2cm x 2cm
Poly layers	2, High Resistive Poly
Metal layers	4, Thick Metal4
Metal Type	Aluminum
POLY1/POLY2 Current Density	0.34/0.2 mA/μm
High Resistive Poly Current Density	0.07 mA/μm
Metal (MET1,2,3) Current Density	0.67 mA/μm
Thick Top Metal (MET4) Current Density	3.35 mA/μm
Capacitor Types	MOS, PIP
Gate Oxide Capacitance	4.54 fF/μm^2
Threshold Voltage of 3.3V NMOS/PMOS	$+0.59V/-0.72V$ (Typ.)
Core Cells	About 300 Standard Digital Cells
Periphery Cells	A/D LV, HV and Floating LV (I/O, Power, Protection Cells)
Supply Voltage	3.3V, 5V, 20V, 50V, 120V (Gate Voltage 5V, 20V)
Temperature Range	$-40°$ C / $+125°$ C
Special Features	High Performance Analog/Digital/HV Process
Application Domain	Mixed Signal Analog Digital, HV Designs, System on Chip

TABLE 3.2: High-voltage typical transistor parameters in AMS H35 technology

Device	Oxide thickness Tox, m	Oxide capacitance Cox, F/m^2	Electron mobility μ, $m^2/V \cdot s$	V_{th}, V	$V_{gs\,max}$, V
NMOS50T	$7.575 \cdot 10^{-9}$	$4.555 \cdot 10^{-3}$	0.039	0.47	3.3
PMOS50T	$7.66 \cdot 10^{-9}$	$4.506 \cdot 10^{-3}$	0.0128	0.63	3.3

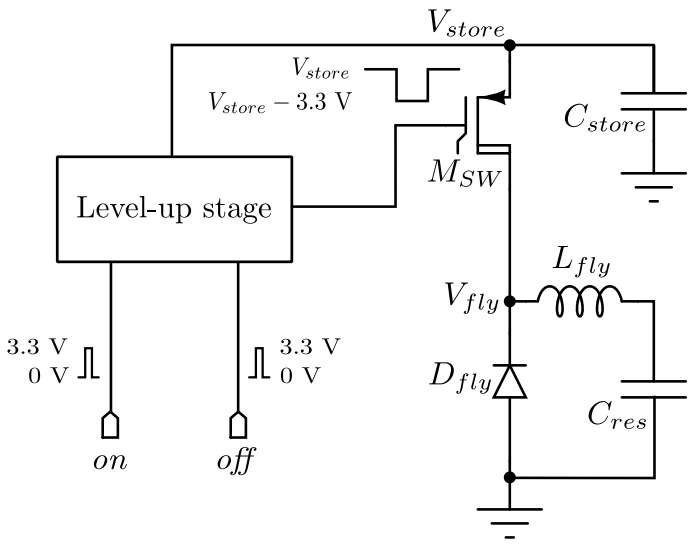


FIGURE 3.2: Schematic diagram of the flyback circuit with a high-side switch employing a level-up shifter

NMOS devices share a common substrate. Additionally, HV devices have poorer matching characteristic than their LV counterparts. Finally, they occupy much more silicon area. Understanding these limitations is important for realizing a reliable and precision HV analog design.

3.6 Design of a high-voltage flyback switch

3.6.1 Technology context

The implementation of the flyback power switch on silicon relies on the circuit topology.

A high-side high-voltage power switch is usually implemented with a PMOS transistor, since in this case the gate is driven with a voltage level lower than the highest potential in the circuit (V_{store} in our case). In contrast, a use of a NMOS switch would require to generate a voltage *above* V_{store}, adding difficulties to the design.

High-voltage MOSFET transistors are able to withstand a high voltage (e.g., up to 50 V in the H35 process) between their source and drain electrodes. However the maximum gate voltage swing with respect to the bulk and source is limited to the low voltage (e.g., 3.3 V). In case of HV-PMOS device, the gate voltage is referenced to the source voltage that is connected to the high-voltage with respect to the ground (V_{store} in out case). Hence, the gate voltage of the HV-PMOS must take values between V_{store} and V_{store}-3.3 V. Since the control of the switch is generated by low voltage circuits referenced to the ground, the HV-PMOS switch control requires a level shifting, as shown in Fig. 3.2.

Considering above consideration, the flyback switch must be composed of:
- the high-side HV-PMOS transistor M_{SW} operating in linear (triode) regime when it is on;

- the level-shifter block translating an external enable low-voltage signal so to generate on or off gate voltage *referenced to* V_{store} to switch the PMOS fully on or off.

3.6.2 Motivation

Why not to use a commercially available high-side driver and power CMOS switch? For that there are two reasons. First, because we target the implementation of the whole control electronics on a chip or, at least, integrate as much blocks and components as possible. Secondly, because the available commercial high-side drivers still consume a relatively high power. We verified that by testing the driver IR2011 from *International Rectifier*. Driven with the 3.3 V input signal, the driver consumes about 10 μA of static current when the high-side output is low (i.e., conducting phase of the high-side switch).

Therefore, we design an own dedicated ultra low-power level shifter. In the following subsections we provide the state of the art study of level shifters, design considerations to realize a new low-power level shifter, and discussions on CMOS implementation of the proposed flyback switch.

3.6.3 Design specifications

The most critical requirement for the flyback switch design is the minimization of the energy consumption. This concerns the conductive losses of HV-PMOS transistor and the dissipated energy by the level shifter. A large channel width of M_{SW} must be used in order to reduce the parasitic channel resistance of the conducting transistor. On the other hand, the larger is the channel of transistor, the higher is the gate capacitance, and consequently the higher dynamic energy losses are related to its recharging. The sizing of M_{SW} must be therefore the trade off result between the conductive losses and losses related to the triggering of the device.

As the conditioning circuit is intended to operate within the large voltage range according to specifications (from 4 up to 30 V), the designed flyback switch must follow the same voltage range specification.

To maximize the current through the closed switch, M_{SW} must be fully on, i.e. its gate must be charged to -3.3 V with respect to V_{store}, but not to exceed this voltage to avoid the gate-oxide breakdown.

Considering that the duration of the flyback phase given by Eq. 2.40 is relatively short (a few to tens microseconds in our model, Chapter 2), the triggering of the flyback switch must occur several order faster, i.e. a few tens of nanoseconds maximum.

3.6.4 State-of-the-art of voltage level shifters

The problem of the level shifting is not new in electronics and dates back to several decades. In state of the art there exist therefore a numerous number of architectures

that perform the level shifting operation. Level shifters are commonly distinguished by the operation technique on static and dynamic typologies.

Static level shifters ensure a stable output voltage at the expense of continuous static current flowing from the supply. If the duration of the level shifting phase is long, the current withdrawal may lead to considerable energy losses. For this reason, static level shifters are not employed in portable and autonomous applications, where the power dissipation is the major criteria.

Dynamically controlled level shifters draw the current from the supply only during the triggering of the output signal from one state to another, while the static current is zero. The state of the shifted level is memorized in the capacitor, which is either discharged (off state), or charged to a low voltage with respect to the high-voltage supply V_{DDH} (on state). If the shifted level is intended to remain, the charged capacitor would eventually discharge due to the leakage current. Therefore, a dynamical refreshing of the output state may be required.

3.6.4.1 Static level shifters

Conventional pseudo-NMOS cross-coupled static level shifter.
A common static level shifter illustrated in Fig. 3.3a is a conventional cross-coupled "voltage mirrors" configuration presented in [Declercq93], where "voltage mirrors" are formed by M_{N1}, M_{P1}, M_{P2} and M_{N2}, M_{P3}, M_{P4}. The idea is to produce the voltage difference $(V_{DDH} - V_H)$ or $(V_{DDH} - \overline{V_H})$, depending on the input signal, so to be equal to the low input voltage V_{in}. Consider a voltage mirror M_{N1}, M_{P1}, M_{P2}. The driver M_{N1} is loaded by M_{P1} connected in diode configuration. A pull-up transistor M_{P2} is connected in parallel to M_{P1} in order to drive $\overline{V_H}$ to V_{DDH} in the high-state, otherwise $\overline{V_H}$ could never reach V_{DDH}. The driving signal of the gate of M_{N1} must be complementary to $\overline{V_H}$. This is achieved by cross-coupling the second identical voltage mirror. In that way, the output voltage V_{out} at the node V_H, swings between $V_{DDH} - V_{in}$ and V_{DDH} depending on the input signal. The major drawback of this architecture is the continuous power dissipation in both output high and low due to fully-on pseudo NMOS (NMOS pull-down and PMOS pull-up) configuration. Another drawback is a non-zero voltage drop of PMOS loads M_{P1} and M_{P4} when they are off. Consequently, M_{P3} and M_{P2} are not driven completely off and the nodes $\overline{V_H}$ and V_H are not fully pulled-up to V_{DDH}.

In order to reduce the power consumption, a current limitation can be added as presented in [Khorasani08].

Pseudo-NMOS cross-coupled static level shifter improved by current limitation.
The static power consumption is reduced by limiting the current flow in the branches. This is achieved by adding the load transistor M_{N3} and the current mirror transistors M_{N4}, M_{N5} and M_{N6}, as shown in Fig. 3.3b. Note, that the current mirror is supplied by a low voltage V_{DDL} in order to reduce the power. By appropriate sizing of transistors in current mirror, the continuous on-current can be reduced by a factor of several orders. While the power consumption is significantly decreased with these modifications, the propagation delay is significantly increased because of the reduced current.

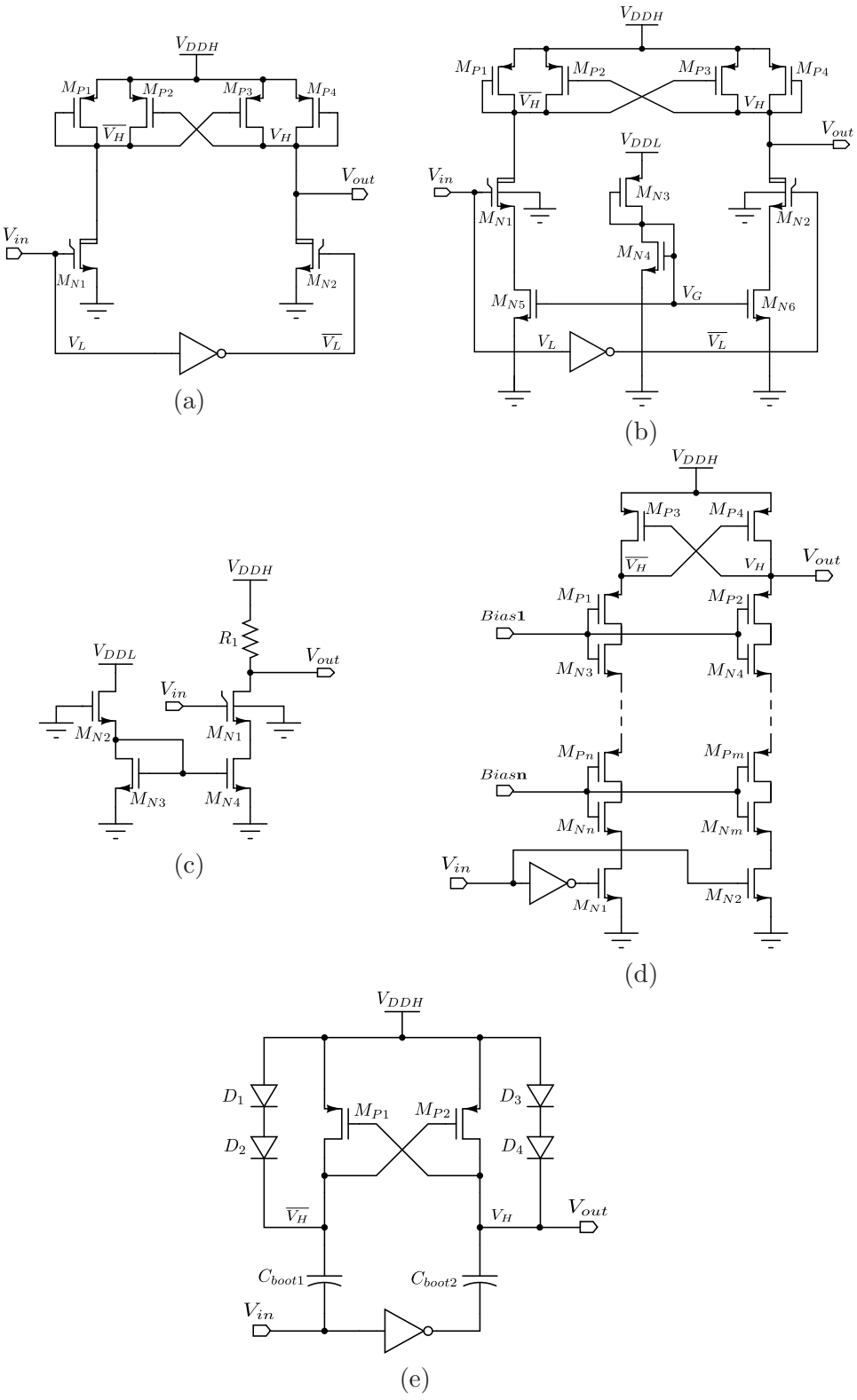


FIGURE 3.3: Static level shifters (LSs) schematics : (a) Conventional pseudo-NMOS cross-coupled LS [Declercq93], (b) Current limiting pseudo-NMOS cross-coupled LS, (c) 3T resistive load LS, (d) Cross-coupled LS based on low-voltage transistors with a set of bias voltages [Pan03], (e) LS by bootstrapping technique [Tan02].

3T resistive load static level shifter.
In order to reduce the current even further and to eliminate the PMOS load effect of the conventional structure, a three transistor (3T) static level shifter with a resistive load can be used. Its schematic is given in Fig. 3.3c. By using the current limit concept introduced in previous circuit in combination with a resistive load R_1, a sufficient voltage drop is achieved at the output. The on-current through M_{N1} can be controlled and reduced. Taking into account a sub-threshold leakage through M_{N1} and appropriately sizing R_1, the output voltage V_{out} can be reliably pulled-up to V_{DDH} when the input is low. The reduced current as in the previous case causes large delays.

Level shifter on low-voltage transistors.
A high-voltage level shifter proposed by [Pan03] uses all standard low-voltage MOSFETs as shown in Fig. 3.3d. It consists of NMOS drivers, series connected NMOS and PMOS pairs and cross-coupled PMOS transistors operating like a current sense circuit. Such a circuit requires a set of bias voltages limiting the voltage swings in each stage, as the maximum voltage across each transistor is restricted by low voltages. Moreover, the larger is the high voltage, the more bias voltages are necessary. Thus, in case of variable high-voltage supply, this circuit is inconvenient.

Level shifter by bootstrapping technique An interesting solution by bootstrapping technique is presented by Tan [Tan02]. The level shifter is based on a cross-coupled PMOS load, similarly to a conventional circuit, but is enhanced by the bootstrapped capacitors, which reduce the voltage swing at $\overline{V_H}$ node and the output node V_H as illustrated in Fig. 3.3e.

Initially, when the input V_{IN} is low, node $\overline{V_H}$ is set to a voltage $V_{DDH} - 2V_{Diode}$, hence C_{boot1} capacitor is charged to a level $V_{DDH} - 2V_{Diode}$ and M_{P2} is turned on. M_{P2} pulls up a node V_H to V_{DDH}, causing M_{P1} to remain off. C_{boot2} capacitor is charged to a voltage $V_{DDH} - V_{DDL}$, where V_{DDL} is a low supply voltage, and which is set at the output of the inverter. As V_{IN} goes high, the node $\overline{V_H}$ is pushed to $(V_{DDL} + V_{DDH} - 2V_{Diode})$, while V_H is pulled down to $(V_{DDH} - V_{DDL})$. Subsequently, the node $\overline{V_H}$ is pulled up to V_{DDH} by M_{P1} and node V_H is pulled down to $(V_{DDH} - 2V_{Diode})$. The voltage on the output level shifter node V_H is restricted to swing from $(V_{DDH} - V_{DDL})$, therefore it is able to switch off in a shorter time, thus minimizing the short circuit current flow that is present in most level shifters. The bootstrapping capacitors should be relatively large in the design, otherwise, the voltage swings at nodes $\overline{V_H}$ and V_H will be reduced owing to the charge redistribution. However, larger capacitors are more power and on-chip area consuming and, therefore, such architecture of level shifter is not very suitable for embedded autonomous devices.

Other variations of static level shifters described in the literature also suffer either from continuous current losses, or delay, and hence are not suitable for autonomous self-powered applications.

3.6.4.2 Dynamically controlled level shifters

Level shifter by dynamic charge control (DCC) on the gates.
One of the zero-static current level shifters proposed in [Doutreloigne01], is a dynamically

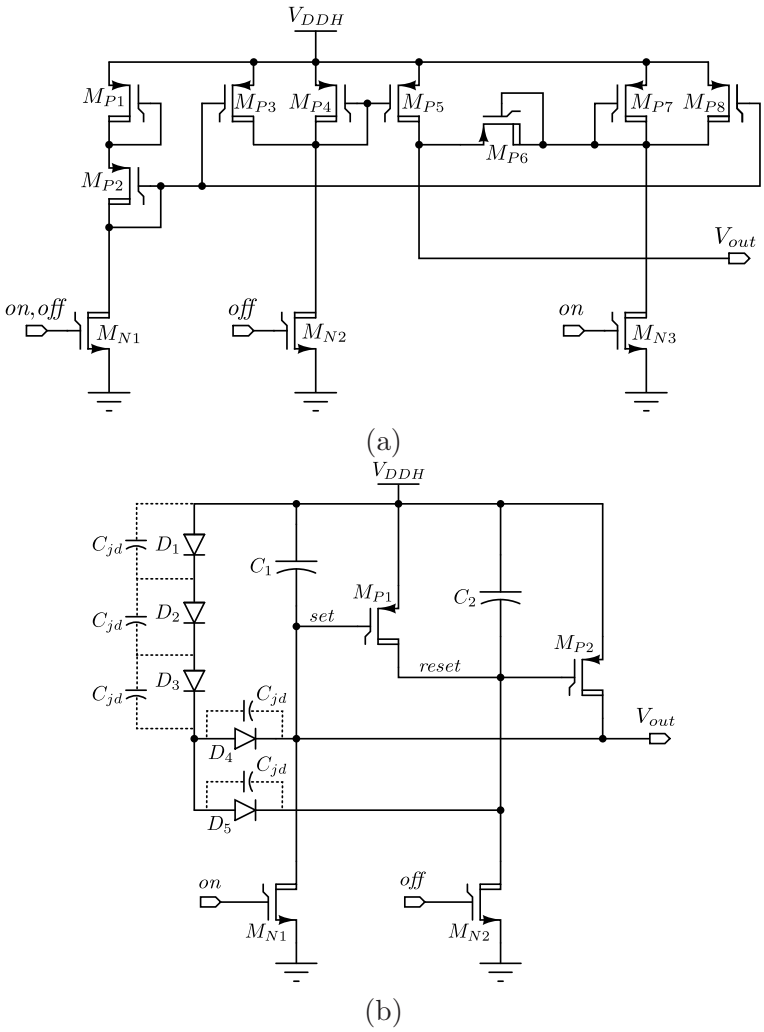


FIGURE 3.4: Dynamically controlled level shifters (LSs) schematics : (a) LS with dynamic charge control [Doutreloigne01], (b) Dynamic LS with high-side flip-flop [Basset03].

charge controlled topology; its circuit diagram is given in Fig. 3.4a. When *on* or *off* strobe signal goes high, M_{N3} or M_{N2} carries a drain current causing a few volts voltage drop over the HV-PMOS M_{P7} or M_{P4}, respectively. When *off* is high, the voltage drop across M_{P4} turns on M_{P5}, which pulls up the output voltage V_{out} to V_{DDH}. On the other hand, when *on* is high, the voltage drop across M_{P7} pulls V_{out} down to $V_{DDH} - V_{in}$ approximately, through the diode-connected transistor M_{P6}. When both inputs *on* and *off* are low, transistors M_{N3} and M_{N2} are off, and the voltage drop across M_{P7} and M_{P4} would be reduced to the threshold voltage of these transistors, keeping M_{P5} at the edge of cut-off operation. Consequently, a small but not insignificant subthreshold current would leak through its channel slowly discharging the total gate capacitance at the output node. As a result, if the charge would not updated on time, the level shifter would not operate properly.

This undesirable phenomena is however eliminated by using two pull-up PMOS transistors M_{P3} and M_{P8}, and two diodes M_{P1} and M_{P2}. On the high-to-low transition of either *on* or *off* signal, M_{N1} carries a current resulting in a few volts voltage drop across the active loads M_{P3} and M_{P8}. As these transistors are switched on, the gates of M_{P7} and M_{P4} are pulled-up to V_{DDH}. Consequently, M_{P5} is driven completely off. In this way, a reliable charge storage is obtained even at a very low input signal pulses frequency.

Although the static current consumption is eliminated, during the pulses *on* and *off* the current flows simultaneously in two branches: through M_{N3} and M_{N1} during *on*, and through M_{N2} and M_{N1} during *off*. The level shifter presented next draws the current through a single branch during the input strobe signal, thus allowing the reduction of power even further.

Dynamic level shifter with high-side flip-flop (FF).
This zero-static power level shifter topology consists of an analog flip-flop [Basset03] on the high side, which is composed of capacitors C_1 and C_2 as well as HV-PMOS transistors M_{P1} and M_{P2}, as shown in Fig. 3.4b. The flip-flop configuration means that the circuit has two opposite output states and capacitors are used to store the state information. Depending on the input pulse *on* or *off*, one of the output nodes *set* or *reset* is connected to V_{DDH}, whereas another one has a voltage potential $V_{DDH} - 3V$. The change of states is achieved by recharging of load capacitors by bias currents, which are provided by saturated transistors M_{N1} and M_{N2} during a short time period.

Assume that at the beginning both inputs *on* and *off* are low, and the state of the flip-flop is so that *set* voltage is V_{DDH}, and *reset* voltage is $V_{DDH} - 3V$. When *on* goes high, C_1 is charged to 3 V so that the *set* voltage become $V_{DDH} - 3V$; this results M_{P1} to turn on, further pulling up *reset* to V_{DDH} and discharging C_2. Consequently, M_{P2} turns off. In that way the state of the flip-flop has changed to the opposite. The reset of the flip-flop occurs similarly when *off* goes high.

A sequence of forward-biased diodes limits the voltage drop across the PMOS transistors, on the one hand. On the other hand, diodes exhibit junction capacitances C_{jd} in reverse bias that withdraw a part of the charge from the state-storing flip-flop capacitors during the high-to-low transition of input signals. Such a charge sharing between capacitors contributes to a decrease of the output voltage at nodes *set* and *reset* with respect to V_{DDH}. The voltage decrease at node *set* driving the gate of the high-side MOSFET leads to increase of the on-resistance of the power switch.

3.6.4.3 Summary

Summarizing the review of level shifters in the literature, one can notice that there exist basically two types of level shifters, namely, based on static and dynamic topology. For autonomous self-powered systems applications where the power consumption is the most critical constraint, static level shifters are not suitable, since they consume continuous static current. Dynamic architectures are more convenient, since their power consumption is only related to the level shifting operation occurring relatively fast, while the static current related to the leakage may be negligible.

Comparing two presented dynamic level shifters, the triggering of the output level in either state requires two current sources for the DCC level shifter and only one for the FF level shifter. Hence the last topology is potentially more power efficient. The first structure however provides a more stable output level, which can be maintained for a longer period without refreshing. In this work, we chose to use the FF level shifter regarding its lower power advantage. Regarding the issue with the output signal distortion, we investigate on a slight improvement of the conventional topology so to attenuate the charge sharing effect in the flip-flop.

3.6.5 Design of the level shifter

The design is based on the flip-flop level shifter [Basset03] that has been briefly presented in previous section. In this section we show the adaptation of this circuit to our needs according to the specifications given in section 3.4. The adaptation concerns the proper sizing of the conventional circuit and the elimination of the charge sharing effect so to provide a stable output voltage.

3.6.5.1 Proposed dynamic flip-flop level shifter

The flip-flop made of the HV-PMOS M_{P1}, M_{P2} and capacitors C_{set}, C_{reset}, is considered as the main block of the level shifter, a simplified circuit diagram of which is given in Fig. 3.5a. The output state of the flip-flop is either V_{DDH} or $V_{DDH} - 3V$, and it is stored in C_{set} and C_{reset} capacitors depending on the input signal *on* or *off*. One of the flip-flop nodes *set* is considered as the output node used to drive the HV-PMOS power switch. The change of the state occurs when one of the strobe input signals *on* or *off* injects a current I_b, which recharges C_{set} and C_{reset}. As soon as capacitors are fully charged to a desired voltage, the current sources are switched off by switches sw_1 and sw_2. Due to relatively high transient currents a significant charge sharing between the flip-flop capacitors and the diodes junction capacities would occur, leading to the decrease of the voltage across the flip-flop capacitors, as we mentioned above. To avoid this undesirable effect, we proposed to electrically isolate C_{set} and C_{reset} from the path of discharge right before the input strobe signal starts to go down as shown in Fig. 3.5b. This is done by the switches sw_3 and sw_4 that cut-off the capacitors from the rest of the circuit (i.e. diodes and input stage). These switches are driven by pulses *on'* and *off'* that are slightly shorter than *on* and *off*, respectively.

This improvement of the conventional level shifter allows the reliable generation and storage of the output levels. The silicon implementation of the proposed solution and simulation results will be discussed in the subsequent sections.

3.6.5.2 CMOS implementation

The circuit diagram of the proposed level shifter implemented in AMS 0.35μm HV-CMOS process is shown in Fig. 3.6 (a) and its layout in (b). According to the technology process parameters, the employed thin gate-oxide high-voltage transistors has the

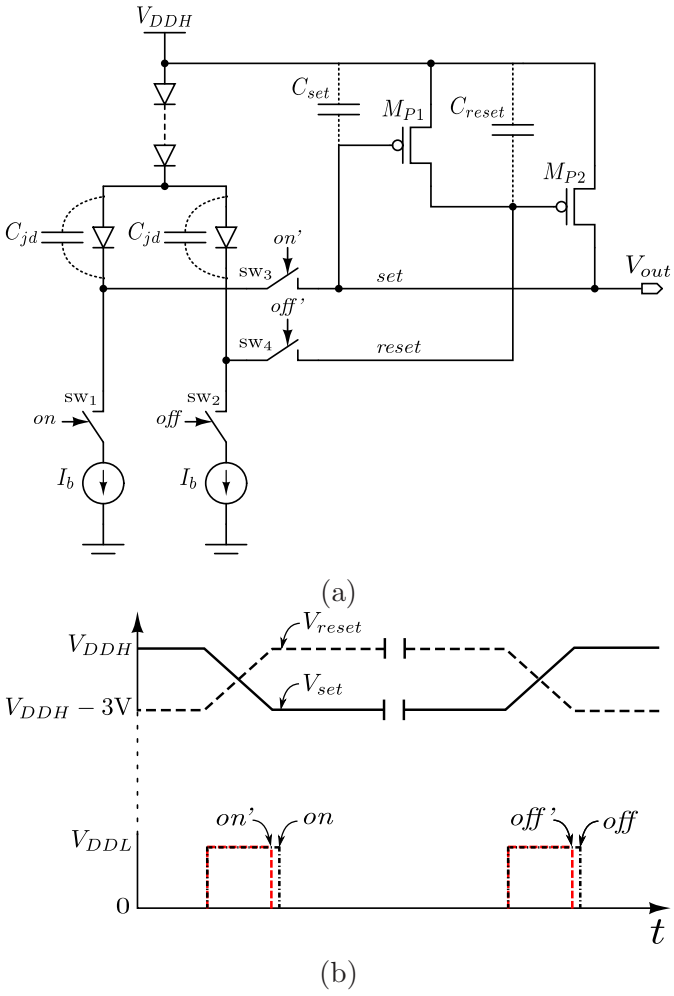


FIGURE 3.5: (a) Proposed dynamic flip-flop voltage level shifter. (b) Voltage diagram of the proposed level shifter operation.

limitation of the maximum V_{gs} voltage equal to 3.3 V, while the reported maximum V_{ds} and V_{db} voltage is 50 V.

The input stage consists of HV-NMOS transistors M_{N1} and M_{N2} driven by 3.3 V logic. The gate of the power HV-PMOS switch M_{SW} is driven by the voltage on the node *set* of the level shifter. The flip-flop stage consists of HV-PMOS transistors M_{P4} and M_{P5}. The over-voltage protection of the gates of HV-PMOS transistors is implemented by diode-connected HV-PMOS transistors M_{P1}-M_{P3}; for each node, *set* and *reset*, a pair of series connected HV-PMOS is employed: M_{P1} and M_{P2} limit the maximum voltage drop across C_{set}, and M_{P1} and M_{P3} - across C_{reset}. The use of PMOS transistors in diode configuration allows a precise adjustment of the voltage swing across them by proper sizing of the transistor.

Switches between the flip-flop and diodes are made of two pairs of transistors M_{P6}, M_{P7} and M_{P8}, M_{P9}. Topologically, these switches are similar to current mirrors, by passing the same current at the output as at the input. The reason of the implementation of switches in such a configuration relates to the operation of transistors close to the

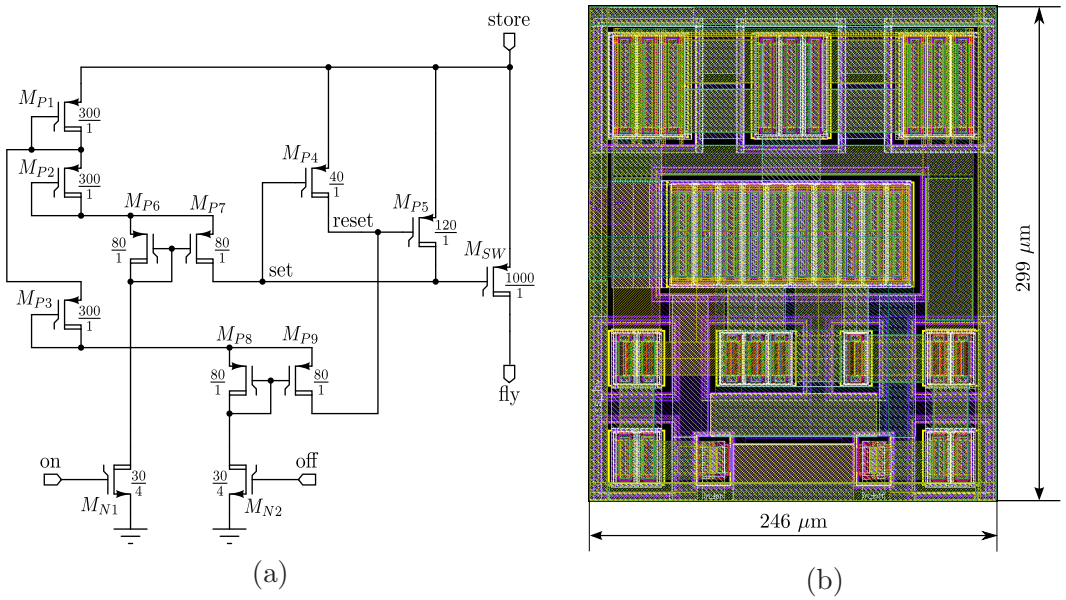


FIGURE 3.6: Proposed dynamic flip-flop voltage level shifter implemented in AMS 0.35μm HV-CMOS process: (a) Schematic (b) Layout.

cut-off region. Thus, when one of the input signals starts its transition from high-to-low, transistors in current mirror turns-off immediately[1], drawing only the sub-threshold leakage current. This technique does not require additional control signals *on'* and *off'* as presented above, and hence presents a more simple and less power-consuming solution.

Design methodology

First, we size the power switch M_{SW} that must conduct a current in a few to tens milli-ampere range, according to Eq. 2.41. To achieve the low on-resistance R_{dson} of the switch, its aspect ratio W/L must be maximized. At the same time, the large channel dimension causes a high parasitic capacitance, and hence high dynamic losses of the driver. The trade off results in the optimal transistor aspect ratio $\frac{1000\mu m}{1\mu m}$. Note that L=1 μm is the minimal length of the HV-PMOS in current technology.

Secondly, we size the flip-flop stage consisting of two transistors M_{P4} and M_{P5}. C_{set} capacitor is represented by the total capacitance of the gates of M_{P4} and M_{SW}, while C_{reset} is the gate capacitance of M_{P5}. C_{set} and C_{reset} can be estimated if knowing the geometry of the flip-flop transistors:

$$C_{set} \approx C_{ox}[(WL)_{M_{SW}} + (WL)_{M_{P4}}], \qquad C_{reset} \approx C_{ox}(WL)_{M_{P5}} \tag{3.1}$$

M_{P4} is sized to be much lower than M_{SW} so to avoid the increase of the total capacitance C_{set} even further. The aspect ratio of M_{P4} is $\frac{40\mu m}{1\mu m}$. M_{P5} is three times larger than M_{P4} so to be able to drive a larger capacitance C_{set} that is estimated as 4.7 pF, according to Eq. 3.1. The estimated C_{reset} capacitor is 0.55 pF.

[1]Means, considerably much faster, since the V_{gs} of the output transistor of the switch is nearly V_{th}, while the V_{gs} of the input HV-NMOS is $V_{DDL} > V_{th}$.

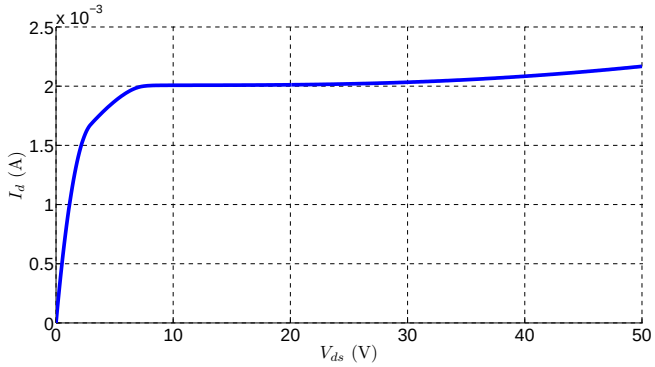


FIGURE 3.7: Voltage-current characteristic of the input stage transistors M_{N1} and M_{N2}

Then, we determine the injected current by the input stage. It must be high enough to quickly recharge C_{set} and C_{reset}, and at once low enough for power preoccupations. Additionally, in order to provide the reliable operation of the level shifter the current must be independent from the HV-supply V_{DDH}, or V_{store} in our case. Hence, M_{N1} and M_{N2} must operate in saturation region behaving as current sources within the full specified voltage range. The provided current is:

$$I_{d1,2} = \frac{1}{2}(\frac{W}{L})_{1,2}\mu_n C_{ox}(V_{gs} - V_{th})^2, \tag{3.2}$$

where μ_n, C_{ox} and V_{th} are the technology related parameters (cf. Table 3.2); W, L and V_{gs} are the design parameters. We size the input transistors as $\frac{30\mu m}{4\mu m}$ so to produce 2 mA current within the whole range as shown by the simulated volt-ampere characteristic in Fig. 3.7. Considering the specified voltage range between 5 and 30 V, the maximum difference of the current is 7 %, and only 2 % between 10 and 30 V.

The duration of the input pulses *on* and *off* is determined by the time of triggering the flip-flop to a new state. Basically, it depends on the current $I_{d1,2}$ charging the capacitor C_{set} or C_{reset} to a V_{gs} voltage of M_{P4} or M_{P5}, respectively:

$$t_{on} = \frac{C_{set} \cdot V_{gsMN4}}{I_{d1}}, \qquad t_{off} = \frac{C_{reset} \cdot V_{gsMN5}}{I_{d2}} \tag{3.3}$$

The value of V_{gs} for both transistors and for M_{SW} is equal and is determined by the voltage drop on two series connected diodes. Ideally, each diode-connected HV-PMOS should be sized so to provide 1.65 V voltage drop across it, and consequently 3.3 V in total. After performing the monte-carlo and process corners simulations of the MOSFET-diodes with 2 mA bias current, it was found that the voltage drop across two diodes exceeds in many cases the attributed voltage. This may lead to unsafe operation zone of transistors where the gate-oxide breakdown may occur. So the diodes were re-sized so to provide the lower total voltage drop - 2.8 V. This is achieved with transistors with an aspect ratio $\frac{300\mu m}{1\mu m}$.

The switches M_{P6}, M_{P7} and M_{P8}, M_{P9} must be small enough in order to turn on and off fast. At the same time, they must be large enough to reduce the on-resistance. The optimal dimensions of each transistor equals $\frac{180\mu m}{1\mu m}$.

Layout
The layout of the improved level-shifter and switch is illustrated in Fig. 3.6(b). The largest transistor in the middle is a HV-PMOS device sizing $\frac{1000\mu m}{1\mu m}$. The rest of transistors constitute the level shifter of the Fig. 3.6a. The silicon area occupied by the layout measures 246 μm x 299 μm.

The layout verification and post-layout simulations using monte-carlo and process corner variations have been done resulting in minor adjustments concerning the output voltage limitation. So we slightly increased the width of PMOS-diodes so to ensure V_{gsmax}=2.8 of M_{SW}. The circuit in this layout was subsequently fabricated and characterized. The full measurement results will be presented in Chapter 4.

3.6.5.3 Simulation results

In this section we summarize the Spice simulation results aiming the comparison of the conventional level shifter (cf. Fig. 3.4b) and the proposed one (cf. Fig. 3.6a) in the context of the flyback circuit (cf. Fig. 3.2) operation. From the obtained results the on-resistance of the switch can be found and the flyback energy transfer efficiency can be calculated. Two simulations of the flyback circuit have been done with identical parameters apart the different level shifters. The main parameters of the flyback circuit model are: C_{store}=3.3 nF pre-charged to 30 V, L_{fly}=15 mH (with 31 Ω parasitic winding resistance), C_{res}=1 μF pre-charged to 10 V, the duration of input signals for the level shifter is t_{on}=t_{off}=60 ns ($t_{rise/fall}$=10 ns), the duration of the high-side switch activation is 10 μs.

The upper plot in Fig. 3.8 illustrates the strobe input signals *on* and *off*. When *on* goes high, the output voltage is shifted so that V_{gs} of M_{SW} changes from 0 to -2.8 V as shown in the plots 2−4. As M_{SW} turns on and *on* pulse goes down, V_{store} decreases. The output level of the conventional LS reduces from $|-2.8|$ to $|-1.8|$, while the improved LS maintains its level. Subsequently, the switch M_{SW} driven by the conventional LS is not fully on as in case with the improved LS, and hence it has a higher on-resistance. Indeed, the voltage drop across the drain and source terminals V_{dson} of the closed switch is higher for the switch driven by the conventional LS. The current flowing through the inductor and switch is shown in the sixth plot. It is possible, thereby, to calculate the switch on-resistance, which equals 60 Ω and 39 Ω when it is driven by the conventional and improved LS, respectively.

Next, we provide the analysis of the efficiency of the flyback circuit relying on the simulation results. For this, we determine the difference between the energy stored in a closed system $C_{res} - C_{store}$ before and after the flyback operation. Before the flyback phase the total energy is:

$$W_{before} = \frac{1}{2}(C_{store}V_2^2 + C_{res}V_{res0}^2), \tag{3.4}$$

where V_2 is the C_{store} voltage before the flyback and V_{res0} is the initial voltage across C_{res}. The total energy stored in the system after the flyback is as follow:

$$W_{after} = \frac{1}{2}(C_{store}V_1^2 + C_{res}V_{res1}^2), \tag{3.5}$$

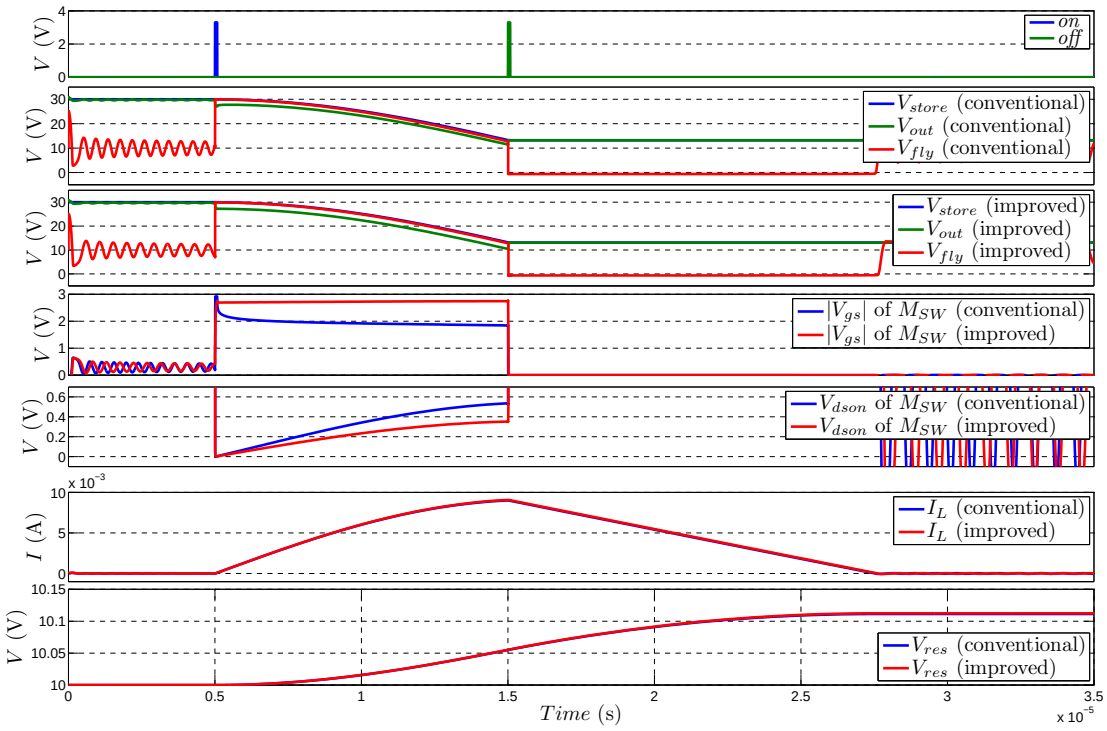


FIGURE 3.8: Simulation results highlighting the difference between the conventional and improved DFF level shifters

where V_1 and V_{res1} are the voltages across C_{store} and C_{res} after the flyback, respectively. The amount of the transferred energy from C_{store} to C_{res} is:

$$W_{transf} = \frac{1}{2} C_{store}(V_2 - V_1)^2, \tag{3.6}$$

The total energy lost during the flyback operation (including losses in the level shifter, switch, diode and inductor) is:

$$W_{loss} = W_{total1} - W_{total2}. \tag{3.7}$$

The efficiency is calculated as:

$$\eta = (1 - \frac{W_{loss}}{W_{transf}}) \cdot 100\%. \tag{3.8}$$

Substituting the obtained data from simulations into above expressions we obtain the following results as presented in Table 3.3.

3.6.6 Conclusions

Prior to design the low-power level shifter, we studied the state of the art of the existing techniques and circuits. For our design we chose the dynamic flip-flop level shifter that has a zero static power dissipation and low power during the level shifting stage. We further improved the conventional circuit topology and redesigned it for our needs. The

TABLE 3.3: Comparison of the efficiency of the flyback circuit that comprises the conventional and improved level shifters driving the switch

Flyback with:	W_{before}, μJ	W_{after}, μJ	W_{transf}, nJ	W_{loss}, nJ	η, %
Conventional LS	51.485	51.3902	435.0043	88.8	79.5
Improved LS	51.485	51.4129	472.0421	72.0226	84.7

proposed level shifter consumes 2 mA current during a very short amount of time (a few tens nanoseconds) when the output level is shifted from one state to another. The rest of the time, the circuit consumes the pico-ampere parasitic current. The output level of the level shifter can vary between 0 and -2.8 V with respect to the high-voltage supply. The power HV-PMOS with the aspect ratio $\frac{1000\mu m}{1\mu m}$ driven by -2.8 V gate-source voltage has the on-resistance 39 Ω. The designed HV switch was employed in the flyback circuit, the energy transfer efficiency of which is 84.7 % according to Spice simulations.

The proposed level shifter and switch was implemented in layout, fabricated and characterized. The full measurements results will be given in next Chapter.

3.7 Design of a flyback switch controller

This section summarizes our investigation on the design of the flyback switch controller on the circuit level. First, we introduce the architecture and operation principles of the controller, then we discuss the design of particular blocks of the controller, and we conclude by simulation results highlighting the performance and consumption of the proposed circuit.

3.7.1 Proposed controller

The proposed flyback switch controller performs two functions.

First, it coordinates the charge pump and the flyback phases following the optimal switch events generation strategy. This strategy claims V_{store} to evolve within a specific optimal voltage range, which is bounded by the upper limit V_2 and the bottom limit V_1, as discussed in section 2.4.2. Thus, one of the functions of the controller consists in monitoring of V_{store}, and generation of *on* and *off* switching events as soon as V_{store} crosses V_2 during the charge pumping phase and V_1 during the flyback phase, respectively.

The second role consists in generation and periodic update of V_1 and V_2 parameters. This function is performed upon the periodically repeated calibration phase. Between two adjacent calibration phases V_1 and V_2 must be kept constant.

The proposed dedicated controller is shown in the system diagram of the complete vibration energy harvesting system in Fig. 3.9. The controller incorporates a ***Calibration*** block, two blocks performing the switch event generation – ***Detection of*** '$V_{store} > V_2$' and ***Detection of*** '$V_{store} < V_1$', and the ***Control logic*** block.

Each block of the controller except the control logic senses the charge pump voltages that may rise up to 30 V, according to specifications in section 3.4. Therefore, each of these blocks includes a voltage divider interface for the signal processing by the standard voltage logic. All dividers have a division factor 12, so that the maximal divided voltage is 2.5 V.

The controller operates in two modes - a relatively short *calibration* and a long-lasting *harvesting* mode as has been illustrated in Fig. 2.10. These modes are coordinated by an external digital signal *mode*: '0'-*harvesting*, '1'-*calibration*.

In the beginning the charge pump capacitors are charged to a voltage V_0 with some external DC voltage bias, so that V_{res}=V_{var}=V_{store}=V_0.

The controller starts in *calibration* mode (*mode* is high) with the intention of measuring the saturation of the charge pump and generating the threshold parameters V_1 and V_2. During the *calibration*, only the ***calibration*** block is enable, while the rest parts of the controller are in idle regime. This block represents an analog calculator, which senses V_{store} and V_{res} and subsequently produces low-voltage V_1 and V_2 according to Eq. 2.43. The calculated parameters are reliably stored. When the *mode* signal goes low, the charge pump is reset to its initial state V_{store}=V_0.

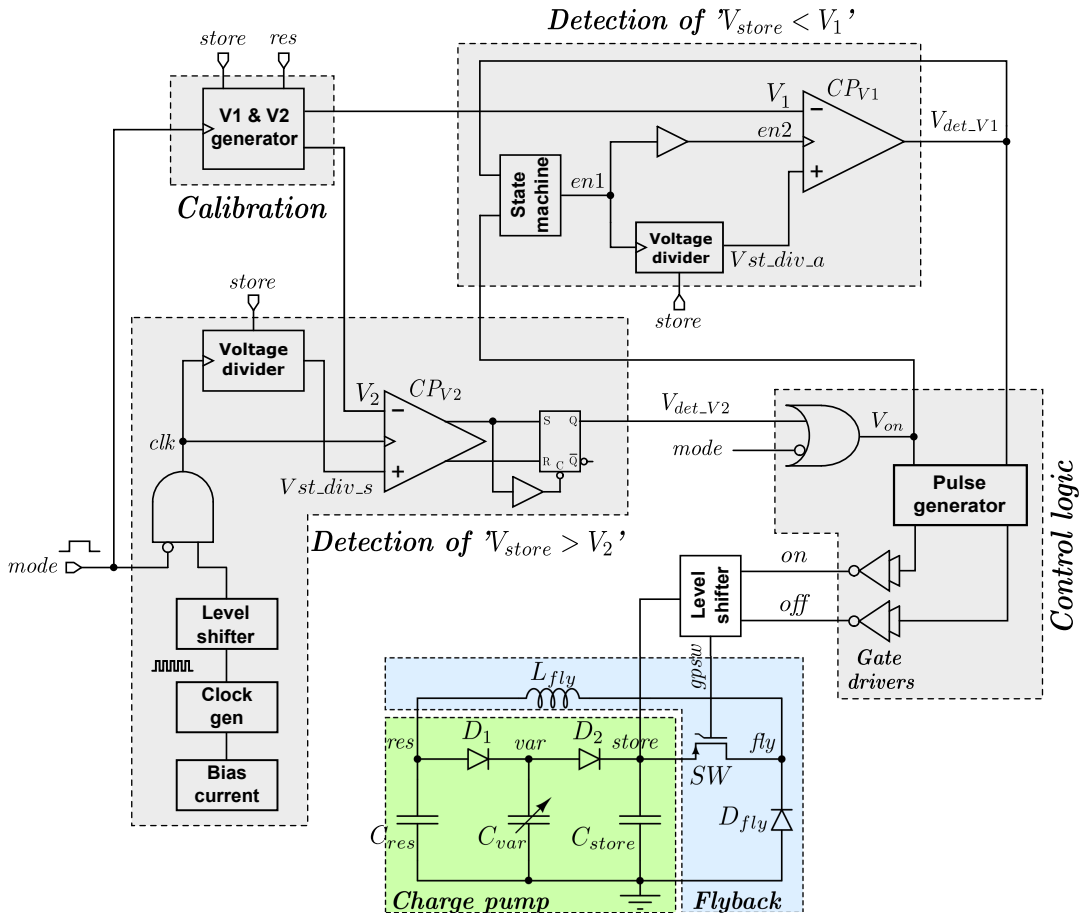


FIGURE 3.9: Complete energy harvester system including the proposed integrated smart flyback switch circuit

The block ***Detection of*** *'$V_{store} > V_2$'* operates during the charge pumping with a purpose to generate the on-switching event when V_{store} reaches V_2. For this, the block senses and divides V_{store}, and compares the divided voltage with V_2. For the power saving considerations, the division and comparison occur with a low-frequency clock *clk* generated inside the block. The frequency of the clock is of the same order as the vibration frequency. To safe the power even further, the clock generator is implemented with a very low voltage level, which is considerably lower than those of the comparator and the gate driving the divider. Therefore, a voltage level shifter is required to translate the voltage level.

The block ***Detection of*** *'$V_{store} < V_1$'* starts right after '$V_{store} > V_2$' is detected, and it operates only during a short-term flyback phase when V_{store} drops fast. This block divides V_{store} and compares its divided counterpart with V_1. When the event is detected the output of the comparator signalizes the state machine to turn this block off.

The digital control logic handles the generation of strobe signals *on* and *off* when the events '$V_{store} > V_2$' and '$V_{store} < V_1$' are detected, respectively. The gate drivers are needed to drive the input transistors of the level shifter.

3.7.2 Integrated circuit design

3.7.2.1 V_1 and V_2 generator

Fig. 3.10 shows the schematic of the generator of V_1 and V_2 that constitutes an analog calculator. The circuit is enable by HV-NMOS transistors driven with a *mode* signal. The calculation V_1 and V_2 is made with resistive voltage dividers that divide V_{store} and V_{res} according to Eq. 2.43. The dividers are implemented off-chip using extra-large resistors to minimize the current withdrawal from C_{store} and C_{res} capacitors. The dividers are calculated as follow:

$$\begin{array}{l} \frac{V_2}{V_{store}} = \frac{1}{12}K_2 = \frac{R_2}{R_1+R_2}K_2, \\ \frac{V_1}{V_{res}} = \frac{1}{12}K_1 = \frac{R_4}{R_3+R_4}K_1, \end{array} \tag{3.9}$$

where $K_2 = [0.6 \dots 1]$ and $K_1 = [1 \dots 1.2]$ are the ad hoc coefficients that allow a fine tuning of the division factor by the designer upon the testing stage. These coefficients can be took into account by modifying one of the resistance in each divider or by connecting an additional trimmer in series, thus changing the division factor.

The produced V_1 and V_2 are sampled and stored throughout the whole calibration phase in relatively large 422-pF capacitors C_1 and C_2, respectively. Such large capacitors (in terms of IC) can be integrated through H35-technology C_{poly} capacitance, which is realized on two poly-silicon layers. The choice of capacitances is a trade-off result: they must be large enough to keep a stable voltage during tens of seconds until the next calibration phase, and low enough to be fully refreshed by a very low current (in nA range) during a relatively short calibration (a few hundreds milliseconds).

The choice of parameters of the circuit is done as follow. Let us suppose that a calibration phase lasts t=200 ms (i.e., 60 mass vibration periods at 300 Hz). This time would be enough for the charge pump saturation according to our model with the parameters of vibrations and of the system as proposed in section 2.7.7. We calculate R_2 and R_4 using the expression of the time for the full charging of capacitors ($t \approx 5\tau$): $R_{2,4} = t/(5C_{1,2}) =$ 200 MΩ. We chose the division factor of V_{store} to equal 14, and that of V_{res} - 11. For this the coefficients are $K_2 \approx 1.16$ and $K_2 \approx 0.92$. Considering these coefficients, R_1 and R_3 from Eq. 3.9 equal 2.6 GΩ and 2 GΩ, respectively.

The energy dissipation of the calibration block in active phase is determined by two currents flowing through the branches of voltage dividers, and two currents charging the holding capacitors. The latter, in turn, is significant only if the capacitors are fully discharged; in principle that is only the case during the first calibration, while thereafter capacitors are supposed to be just slightly recharged. It is difficult to provide the exact numbers of power consumption, since V_{store} changes all along the harvester operation. We will however give some numbers for a particular case studied by simulations in section 3.8.

With maximum 30 V on C_{store} and, for example, 20 V on C_{res}, the estimated peak power of V_1 and V_2 generator is 527 nW. During the calibration phase, however, V_{store} reaches the maximum voltage only at the end of phase, while it starts rising from the level of V_{res}. Hence the average power over the typical calibration phase is considerably lower.

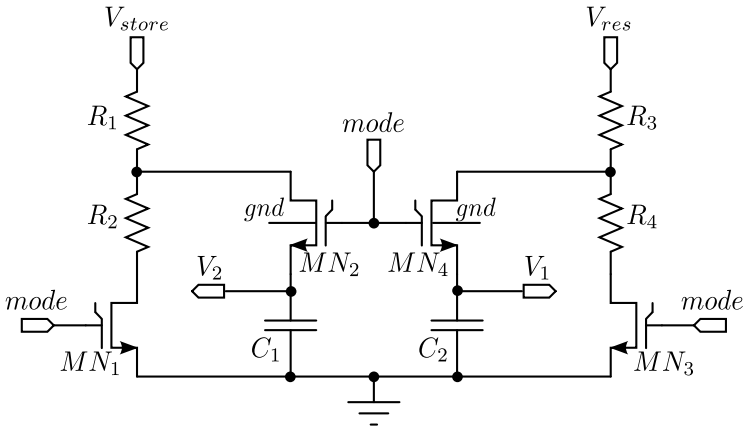


FIGURE 3.10: Auto-calibration block: generation and storing of divided voltage levels V_1 and V_2

Moreover, since the ***Calibration*** block wakes up only for a short duration, the average power of V_1 and V_2 generator over the system operation is few orders of magnitude lower than the peak power calculated from the above considerations.

3.7.2.2 Clock generator

This work employs a CMOS clock generator instead of crystal quartz or LC oscillators, since lasts are either bulky, or not suitable for low-frequencies and low-power applications, or provide a sinusoïdal signal. Prior to design a clock generator, a bibliography study has been done.

There exist two main types of CMOS oscillators with ultra-low power consumption operating in sub-threshold region, and hence consuming a tiny amount of current [Cannillo09]. One of them is a ring oscillator using the principle OTA-C (Operational Transconductance Amplifier-Capacitor) [Linares91], [Mourabit05]. Such oscillators contain either several OTAs or other additional off-chip passive components, resulting in bulky and complex structures. Usually this type of oscillators is used in applications with frequencies in the range much higher than we specified. A relaxation oscillator is an another low-power clock generator with a relatively high accuracy, which can be cheaply implemented without any external components using only CMOS process. Its major drawback is the susceptibility to temperature variations, which can be eliminated, however, by using the bias-current compensation technique. The feasibility of the ultra-low power relaxation oscillator has been demonstrated by Urs Denier [Denier10]; by generating a clock signal of 3.3 kHz only 11 nW was consumed from a 1-V supply over a wide temperature range with low sensitivity to temperature drift.

Inspired by the excellent results reported by Denier in his paper, we decided to employ his architecture of relaxation oscillator in our work. We adapted the proposed circuit to our requirements (frequency, power, supply voltage, etc.) and added the mechanism of programming the output frequency. This work has mainly been done by our master student at LIP6 A. Deluthault in the context of his master thesis project. The employed clock generator that will be discussed below, consists of the relaxation oscillator and bias

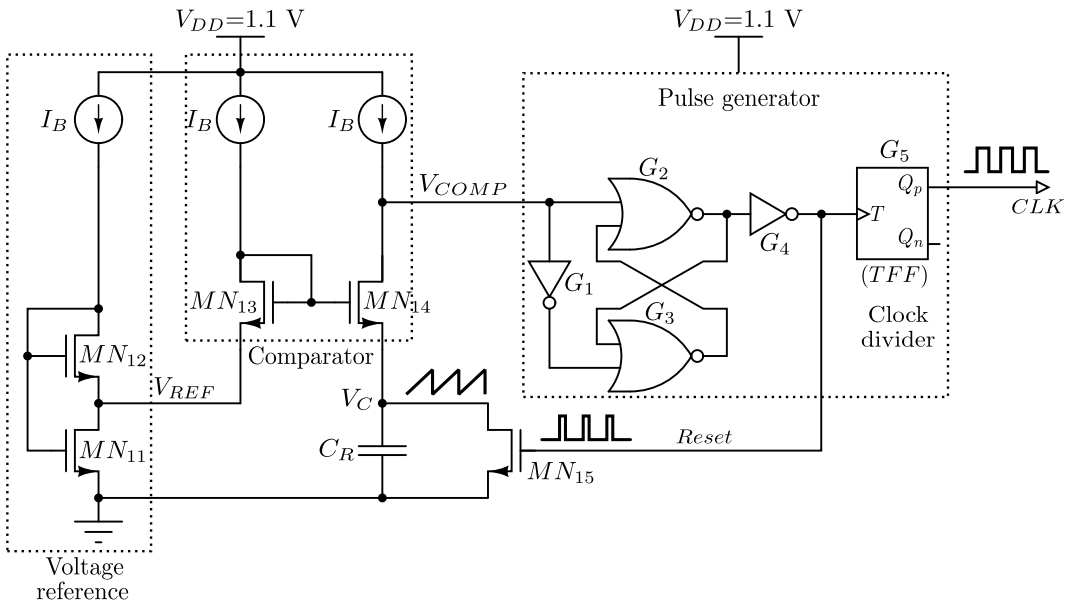


FIGURE 3.11: Relaxation oscillation circuit with current-mode comparator, proposed by Urs Denier [Denier10].

current reference circuit (both are supplied with a reduced voltage - 1.1 V) and a level shifter of the architecture in Fig. 3.3a to shift the high level of the output signal from 1.1 to 3.3 V.

Relaxation oscillator

Fig. 3.11 shows a relaxation oscillator that consists of the following blocks : a generator of the reference voltage V_{REF}, a time constant defining reference capacitor C_R, a voltage comparator, a generator of the bias current I_B and a pulse generator. One of the advantages of this relaxation oscillator circuit is a simple structure, and hence the reduced current consumption, as the number of current-conducting branches is minimized in contrast to previous implementations [Shenghua07], [Flynn92].

The initially discharged capacitor C_R is being charged with a constant current I_B causing the voltage across the capacitor V_C to increase linearly. Simultaneously, V_C is being compared with the reference voltage V_{REF} that is generated by a MOS divider biased by I_B. The voltage reference consists of MN_{11} and MN_{12} operating both in weak inversion. This well-known architecture [Vittoz79] provides a proportional-to-absolute temperature (PTAT) output voltage [Rossi07] that equals:

$$V_{REF} = \phi_t \cdot ln(2 \cdot \frac{S_{MN_{12}}}{S_{MN_{11}}}), \qquad \phi_t = \frac{\kappa_B T_{abs}}{q}, \tag{3.10}$$

where S denotes the W/L ratio of the respective NMOS and ϕ_t is the thermal voltage. A low reference voltage implies a strong inversion level of MN_{11}.

As soon as V_C reaches V_{REF} the comparator output goes high and the digital circuit, made of logic gates $G_1 - G_4$, produces a strobe pulse *Reset*. During the reset, the switch MN_{15} pulls the node V_C down to zero, thus immediately discharging C_R. The recurrent charging/discharging of C_R results in a periodic saw-tooth signal V_C with a

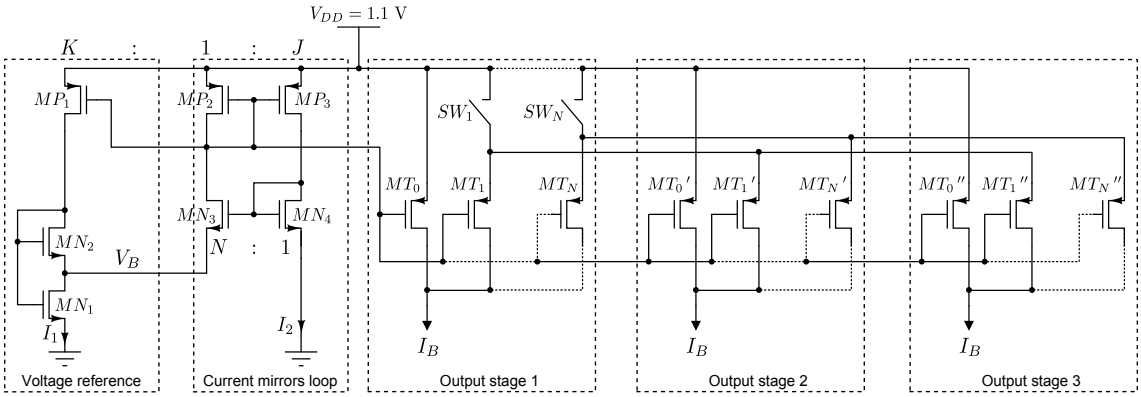


FIGURE 3.12: Bias-current generator with a programmable output current.

period approximately (by neglecting the overdrive voltage of the comparator) equals:

$$T_{OSC} \approx \frac{C_R \cdot V_{REF}}{I_B}. \tag{3.11}$$

To produce a 50 % duty cycle output clock, a toggle flip-flop (TFF) is added. Since TFF changes its output on each edge of *Reset* signal, the output clock CLK is a square waveform with a frequency equal to the half of the oscillator frequency:

$$f_{CLK} = \frac{f_{OSC}}{2} \approx \frac{I_B}{2 \cdot C_R \cdot V_{REF}}. \tag{3.12}$$

The circuit parameters that we calculated and adjusted throughout simulations are provided in Table 3.4. The relaxation oscillator circuit is supplied with a reduced voltage

TABLE 3.4: Key element design parameters of relaxation oscillator

Component	W(μm)	L(μm)	Nominal
C_R			14.8 pF
MN_{11}	4	32	
MN_{12}	4	4	
MN_{13}	0.4	0.4	
MN_{14}	0.4	0.4	
MN_{15}	20	0.35	

$V_{DD} = 1.1$ V. A low V_{DD} allows a considerable power saving; the latter is mainly defined by the current reference generator.

Reference current generator

The bias current generator defines the power consumption of the overall oscillator circuit and its temperature characteristics. In this work we employ the self-biased current source (SBCS) circuit initially proposed by [Mauricio05]. This power-efficient SBCS replaces the resistor given in [Vittoz79] with the self-cascode MOSFET (SCM) operating in moderate inversion.

The schematic of the current reference is shown in Fig. 3.12. The core of the circuit consists of the voltage reference and two current mirrors interconnected in a closed loop (MP_2, MP_3 and MN_3, MN_4) with a gain $N \cdot J$. The goal of the loop is to increase the current in all branches. A third current mirror (MP_1, MP_2) forces MN_1 to operate in the triode region, so to act as a high-impedance degeneration resistance. Consequently, it causes the gain to reduce while the current increases, thus achieving the equilibrium state when the current gain becomes one.

The minimal allowable supply voltage V_{DD} must satisfy the constraints imposed by two leftmost branches in Fig. 3.12. These constraints are presented as:

$$V_{DD} \geq max[|V_{DSsat,P1}| + V_{GS,N1},\ |V_{GS,P2}| + V_{DSsat,N3} + V_B] \tag{3.13}$$

Assuming that the p-channel transistors operate in weak inversion with inversion level close to 1 so to satisfy $|V_{GS,P2}| \cong V_{TP}$ and $|V_{DSsat,P1}| \cong 100$ mV, and that MN_2 operates in moderate inversion so to satisfy $V_B \leq 100$ mV, Eq. 3.13 can be approximated as:

$$V_{DD} \geq |V_{TP}| + 200\,mV, \tag{3.14}$$

where V_{TP} is the threshold voltage of PMOS. Although Eq. 3.14 is a rough approximation, it is useful to find the minimal supply voltage required to turn on the reference current generator. Thus, we chosen $V_{DD} = 1.1$ V.

The design of the core circuit is based on the ACM model (Advanced Compact MOSFET) that employs the concept of inversion level [Cunha98]. According to this concept, the drain current can be split into forward i_f and reverse i_r currents:

$$I_D = I_S(i_f - i_r), \tag{3.15}$$

where I_S is the sheet specific current defined by technological parameters (electron mobility μ_e, gate-oxide capacitance C_{ox}, slope factor n and thermal voltage ϕ). The sizing of transistors using the ACM model is achieved following the methodology presented in [Mauricio05]. This method yields the following dimensions of all transistors in the core bias generator as presented in Table 3.5.

TABLE 3.5: Transistor sizes for SBCS

Transistor	W (μm)	L (μm)
MN_1	1	1515
MN_2	1	2272
MP_1	8	6
MP_2	8	6
MP_3	8	6
MN_3	32	6
MN_4	8	6

The output stage of the circuit consists of a transistor MT_0 that copies the current from MP_2[2] and draws it to the output. It also consists of transistors $MT_1 - MT_N$ placed in parallel so that their sources are connected to the high-side switches and their drains are all connected to the common output node. Closed switches allow source additional current through transistors towards the output branch. The maximum current is given as:

$$I_B = I_{MT_0} + S \cdot \sum_{i=0}^{n} I_{MT_1} \cdot 2^i \cdot C_i, \tag{3.16}$$

where S is the parameters denoting rather any of the switches is on or off: it is "0" when all switches are off, and "1" otherwise; n is the number of transistors in the output stage; C_i is a correction coefficient using for a minor correction of the current during the testing stage. When all switches are off, only MT_0 draws the current to the output and I_B is considered as minimal. Conversely, when all switches are on, all transistors $MT_0 - MT_N$ conduct, thus providing the maximal I_B.

Table 3.6 provides the dimensions of N=6 transistors employed in the output stage and the attributed current through each transistor. From these data, the minimal current I_B is 109 pA and the maximal I_B is 675 pA. Using that currents, the relaxation oscillator in Fig. 3.11 yields the clock signal within 52 and 325 Hz according to Eq. 3.12. As

TABLE 3.6: Transistors sizes and attributed current

Transistor	W (μm)	L (μm)	Attributed current I_D (pA)
MT_0	9	7	109
MT_1	3.2	16	16
MT_2	4.1	10	33
MT_3	7.6	8	73
MT_4	7.8	4	151
MT_5	11.5	3	293

the relaxation oscillator presented in Fig. 3.11 requires 3 current sources to bias the various stages, two identical output stages are connected as shown in Fig. 3.12. It can be noticed that such a configuration allows connect three transistors (one from each stage) to a unique switch, thus providing the control of the current in three branches at once, and reducing the number of the off-chip switches.

The estimated power consumption of the current reference circuit that contains three outputs is given next:

$$P = (I_1 + I_2 + 3I_B)V_{DD}, \tag{3.17}$$

where the first part of the expression designates the power of the SBCS core and the second part of three output stages. Supplied by V_{DD}=1.1 V, the total power is between 700 pW and 2.57 nW depending on the programmed current I_B.

Feasibility testing, layout and final results

The feasibility of the clock oscillator has been proven by simulations using temperature

[2] MP_2 and MT_0 form a current mirror.

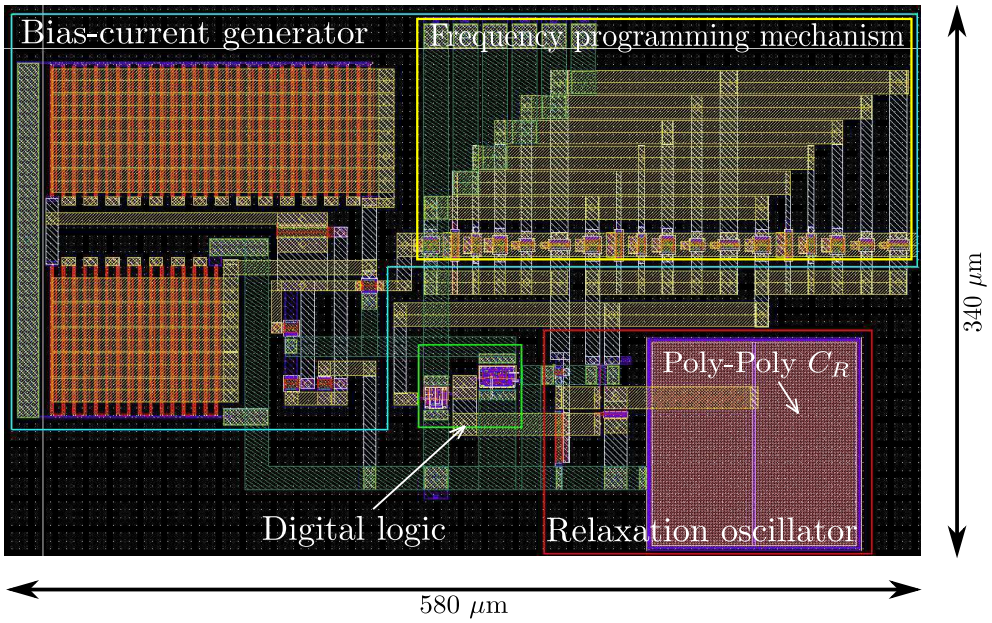


FIGURE 3.13: AMS035HV layout of a programmable frequency relaxation oscillator

and process variations (Monte Carlo). With temperature variation between two extrema -25 and 125 °C, the maximum difference of the output frequency is 17 %. The Monte Carlo analysis performed on 2000 simulation runs has around 72 % results with the error inferior to 30 % with respect to the estimated frequency of the clock. The total power consumption for the desirable 300 Hz is between 2 and 17 nW for more than 75 % of simulations, where the digital blocks in 95 % cases consume 1.2-3.7 nW, and the analog part in 95 % shows the power dissipation in the range 1-15 nW, and in 50 % - less than 6 nW.

Fig. 3.13 illustrates the 580 x 340 μm layout of the designed clock generator circuit. In the left side two long-channel transistors from the SCM core are implemented by division transistors on numerous parts. The big square capacitance C_R in relaxation oscillator is implemented with POLY-POLY capacitor in spite of higher resistivity of the material with respect to MIM capacitor. The latter requires considerably greater surface area for equal capacitance value. The right upper part of the layout illustrates three output stages of the current generator.

The layout was verified, extracted and simulated. The post-layout simulation resulted in insignificantly reduced frequencies and increased power dissipation due to added extracted parasitic components. Thus, the lowest obtained frequency is 41 Hz with a total consumption of 7.3 nW, and the highest frequency of 265 Hz with a total power 32 nW.

3.7.2.3 Clocked resistive voltage divider

The synchronous voltage divider used in the ***Detection of*** *'$V_{store} > V_2$'* block, operates with a clock *clk* as shown in Fig. 3.14. The divider topologically is a half of the circuit

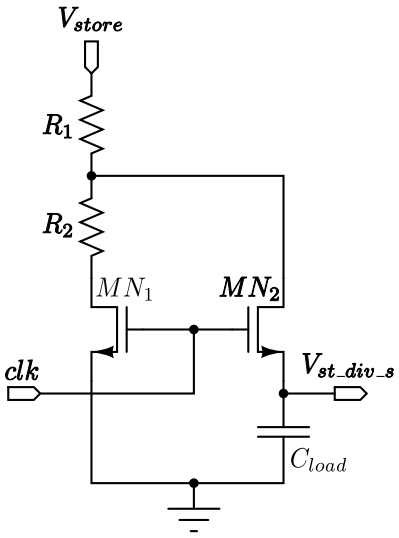


FIGURE 3.14: Synchronous voltage divider with low current consumption

in Fig. 3.10, and it is composed of 2 extra-large off-chip resistors connecting in series, 2 HV NMOS switches and a small capacitor C_{load} of the next input stage.

With a division factor 12, we selected $R_1 = 10$ GΩ and $R_2 = 910$ MΩ. Such large values aim to minimize the current withdrawal from C_{store} occurring during the vast majority of the time of harvester operation. With maximum 30 V on C_{store}, the approximate power consumption of this block is 82 nW.

3.7.2.4 Comparator CP_{V2}

The block ***Detection of*** *'*$V_{store} > V_2$*'* of the controller employs a classical one-stage semi-dynamic latched comparator CP_{V2} [Maloberti07] operating with a low-frequency clock *clk*.

Topologically, the comparator circuit consists of 4 connected blocks (cf. Fig. 3.15a):

- Input block: MP_1 and MP_2
- Switching block: MN_1 and MN_2
- Flip-flop block: MP_3, MN_3 and MP_4, MN_4
- Pre-charge block: MP_5 and MP_6

The comparator operates in two phases: pre-charge (*clk* high) and comparison (*clk* low). At the pre-charge phase the outputs of the comparator (inputs of a flip-flop) *qm* and *qp* are initialized to V_{DD}. At the comparison phase, the voltage difference e_p and e_m is transferred, injected as current at the nodes X and Y of the flip-flop which will then regenerate the outputs to V_{DD} and zero. The pair of switching transistors prevents the

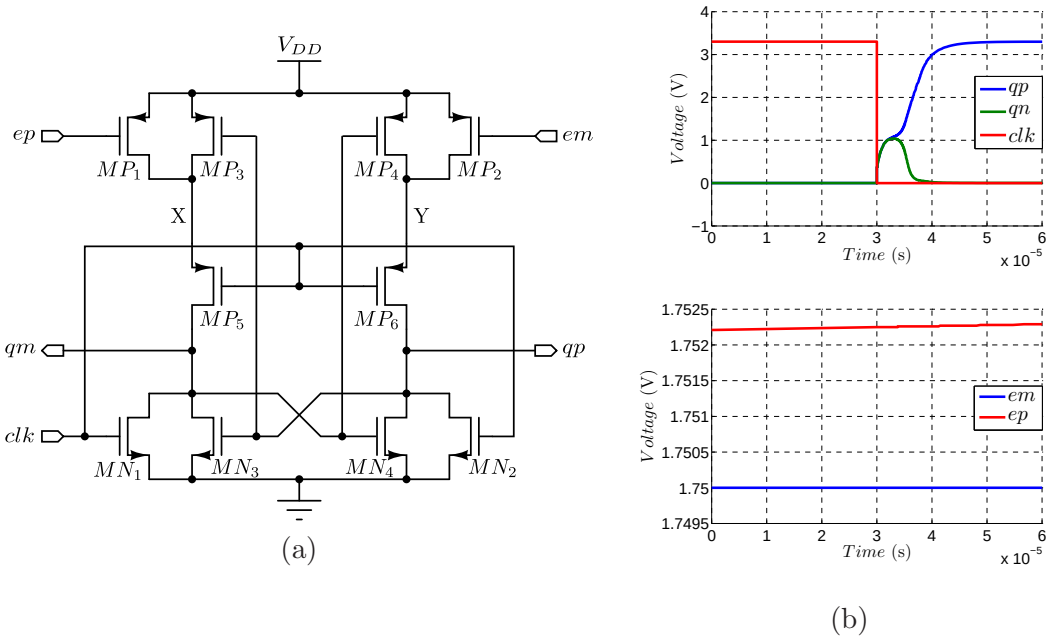


FIGURE 3.15: Semi-dynamic comparator switched at the drains with differential output: (a) schematic; (b) simulated response time and resolution at 300 Hz clock

current to flow in the branches during the high level of the clock. The circuit is classified as semi-dynamic since it does consume the current only during the clock is low.

The comparator is a non-linear circuit as the constituting transistors have different operating points changing dynamically. Unlike the linear devices, it is impossible to consider for each transistor a rest point allowing an analytical determination of the dynamic parameters (gm, gds, etc.) to study the circuit performance (gain, transition frequency, etc.). We can only consider some principles allowing sizing of the devices although the obtained performance parameters can be confirmed with simulations.

The switching and pre-charge pairs can be chosen as minimal size transistors to minimize their parasitic contribution in the comparator settling time. The sizes of the flip-flop and the input pair can not be selected in a similar straightforward way, since many trade-offs might be considered to find the most suitable values. The flip-flop transistors and the input pair transistors are responsible for the current consumption, so they will be sized so to minimize the current flow during the comparison stage. So the lengths L of transistors should be maximized, while the widths W minimized. Too high L, however, will result in a high input capacitance and hence high dynamic power and settling time. With simulations we found the optimal sizes of transistors, which are summarized in Table 3.7.

The maximum current consumption of the comparator is only 58 nA, such a low current is mainly because of the very long channels of transistors in the input pair. Since the comparator operates with a 50 %-duty cycle clock, the average current over one comparison cycle is 29 nA, that results in the average power 96 nW. The settling time of the comparator output is about 10 μs as illustrated in Fig. 3.15b (upper plot), that

TABLE 3.7: Dimensions of transistors

	MP_1	MP_2	MP_3	MP_4	MP_5	MP_6	MN_1	MN_2	MN_3	MN_4
W (μm)	0.4	0.4	0.4	0.4	0.5	0.5	0.5	0.5	0.8	0.8
L (μm)	300	300	100	100	0.35	0.35	0.35	0.35	100	100

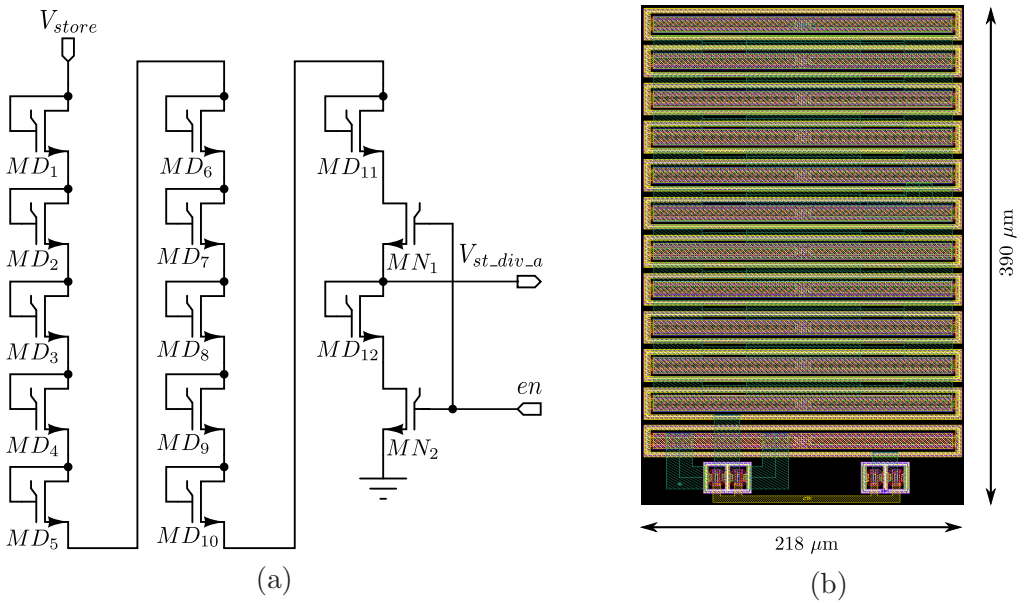


FIGURE 3.16: CMOS voltage divider: (a) Schematic; (b) Layout

is perfectly acceptable regarding the period of a cycle which is 3 orders larger. The resolution of the comparator depends on the frequency of the clock - the higher is the frequency - the higher is the accuracy of the comparison. For two limit frequencies specified in our design the following comparator resolution is obtained: 20 mV@50 Hz and 2 mV @ 300 Hz as shown in Fig. 3.15b (bottom plot).

3.7.2.5 CMOS voltage divider

The voltage divider in the controller block ***Detection of*** *'$V_{store} < V_1$'* is used to divide the V_{store} voltage during the flyback phase, which lasts for a short period of time (a few tens microseconds). Fast and energy-efficient voltage division can be achieved with a CMOS divider, which is implemented by diode-connected high-voltage NMOS transistors. The schematic and the layout of the proposed divider are shown in Fig. 3.16. Diodes MD_1-MD_{12} connected in series perform the voltage division by 12. Transistors MN_1 and MN_2 are used for sampling of the divided voltage and activation of the divider, respectively.

The difficulty of transistors sizing of this divider relates to the desired wide voltage range of V_{store} (3-30 V). At high V_{store}, intense currents through transistors can be decreased

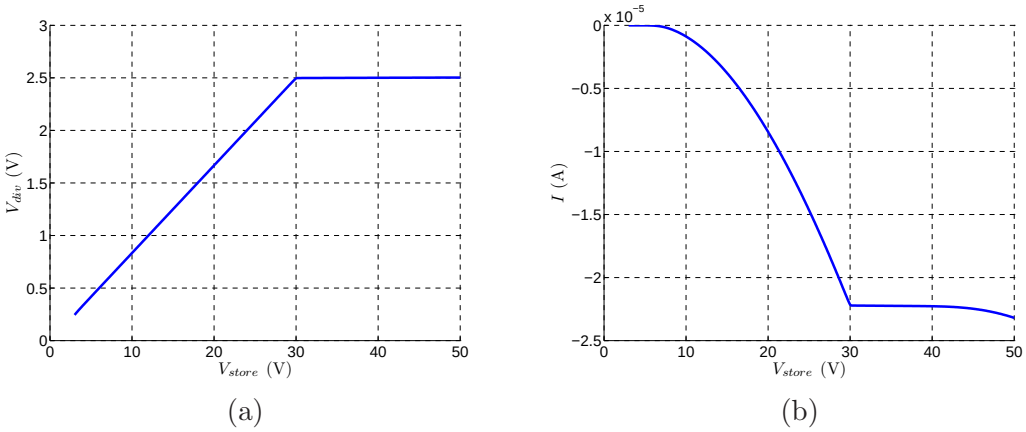


FIGURE 3.17: DC analysis of CMOS voltage divider: (a) divided voltage ; (b) current consumption

by lowering the aspect ratio of transistors, however, too low aspect ratio deteriorates the accuracy of the division at low V_{store} voltage. Conversely, excessively high aspect ratio results in a good accuracy within the full range at the expense of higher currents. Therefore, a trade off must be considered. Relying on the DC analysis of the circuit, the optimal dimensions of transistors are found: the aspect ratio of MD_x is 1μm/120μm. High-voltage switches MN_1 and MN_2 have a minimal size 10μm/1μm to provide a fast switching and to minimize the leakage current, since the vast of the time the circuit is idle.

Fig. 3.17 shows the DC analysis results of the divider scheme within the full operation voltage range. It can be observed that the divided voltage increases linearly with V_{store} up to the specified maximum voltage that means a high accuracy in that range. The current consumption is up to 2.25 μA.

3.7.2.6 Comparator CP_{V1}

As previously mentioned, the CP_{V1} comparator signals the end of the flyback phase when the decreasing divided V_{store} reaches V_1. Comparator in Fig. 3.18 employs an n-type input differential pair with a p-type load mirror to feed the common source transistor and subsequently drive the output stage. The circuit is driven by a signal *en*, which enables the currents biasing each stage of the comparator.

Common-source amplifier MP_3 further amplifies the signal from the first stage to decrease the shoot-through (short-circuit) current in the ensuing inverter because a steeper transition decreases the time pull-up and -down transistors conduct simultaneously. Switch MN_4 sinks additional current from the current mirror MP_1-MP_2 when $\overline{Q}$ goes high. By unbalancing the current flowing from the current mirror, the hysteresis is established. All the NMOS and PMOS bulks are connected to the ground and V_{DD}, respectively, unless otherwise specified.

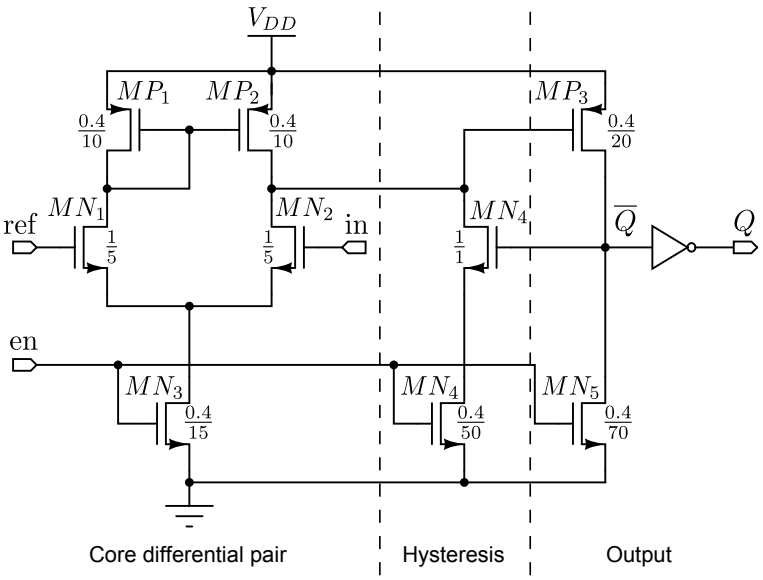


FIGURE 3.18: One-stage OTA with hysteresis employed as a differential to single-ended comparator (transistors dimensions are in μm)

The differential pair transistors feature rather short channel lengths to keep delays short and accuracy high enough. High-impedance current source transistors MN_3-MN_5 bias each gain stage with the following currents: 1.3 μA, 410 nA and 1.64 μA, respectively. The total maximum current consumed by the comparator is therefore 3.35 μA (P_{max}=11 μW with V_{DD}=3.3 V). When $\overline{Q}$ goes low, transistors MN_4 and MN_5 do not conduct, thus the total current consumption is reduced (only MN_3 conducts).

3.7.2.7 Control logic and gate drivers

Strobe pulse generator

As previously discussed, the comparators CP_{V2} and CP_{V1} in Fig. 3.9 signalize that the flyback switch must turn on and turn off, respectively. The digital control logic is employed to generate the strobe pulses from the triggering outputs of comparators; the strobe form of signals is required regarding the specifications of the designed level shifter, which drives the flyback switch.

The pulse generator is built of a rising edge detector circuit, which is shown in Fig. 3.19a. The rise-edge detection circuit senses low-to-high transitions by comparing with an AND gate a digital input signal with its inverted and delayed counterpart. Once V_{in} became high, while another input of the AND gate remains high temporarily as well, the AND gate enables the detection of the high transition. The duration of the strobe that is seen on the output of the AND gate, is specified by the level shifter, and it is set up by the RC delay. To generate the strobe that lasts 50 ns, the values of RC network are as follow: R=50 KΩ and C=1 pF. Both passive components can be easily integrated on chip by occupying a relatively small surface area not larger than 0.2 mm^2.

Gate driver

The level shifter is composed of all high-voltage transistors with two input transistors

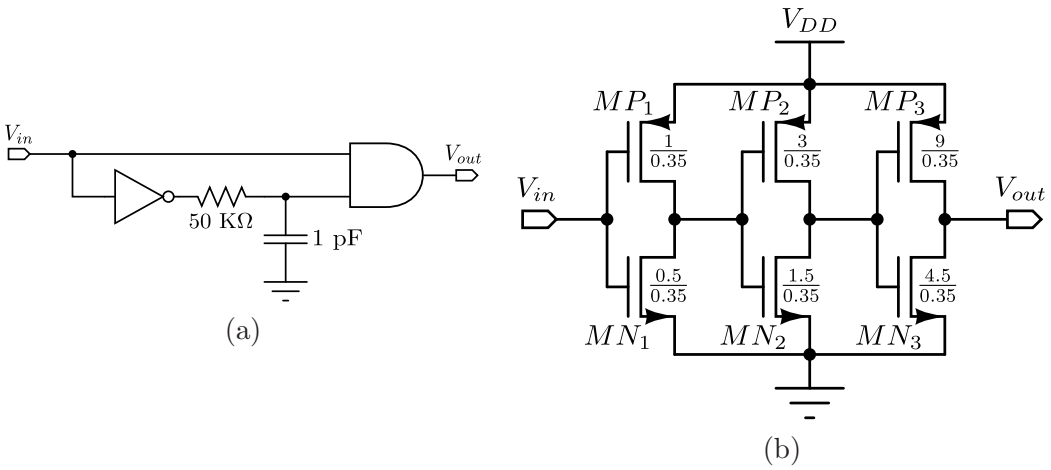


FIGURE 3.19: (a) Digital rise-edge detection circuit for strobe generation; (b) Gate driver (transistors dimensions are in μm).

featuring the size 30/4 μm each. The strobe generator is however composed of low-voltage logic gates with considerably smaller transistors. Inverting gate drivers are therefore added to amplify the signals from the control logic so to be capable to drive the relatively high capacitive load of the input gates of the level shifter. In order to safe energy, the driving circuit features only three series of inverting stages that progressively increase in size, as illustrated in Fig. 3.19b. Let we notice that the first inverter is a part of the AND-gate of the foregoing strobe-generator stage, because usually the CMOS AND-gate is implemented as a combination of a NAND and an inverter.

3.8 Simulation

The proposed e-VEH system presented in Fig. 3.9 was modeled and simulated using AdvanceMS simulator. The model of the complete system includes the behavioral VHDL-AMS model of the MEMS structure presented in Section 2.7.3, the electrical components of the charge pump and flyback circuit and the proposed integrated circuit of the adaptive flyback switch (high-side switch, its driver and controller) designed in HV 0.35μm AMS process.

The main goal of this simulation is to test the feasibility of the proposed smart flyback switch and estimate its power consumption. The simulation parameters and components of the conditioning circuit are identical to those presented in section 2.7.7, apart the frequency of calibration events, which occur every 2 seconds. The designed circuit is able to operate with as low voltage as 4 V on C_{res} and C_{store}. In this simulation example, the start-up voltage on C_{res} is set to 10 V with the purpose to test the high-voltage operation of the system that eventually increases as the system accumulates the converted energy.

After being disconnected from the external energy source pre-charging C_{res}, the designed VEH system operates in semi-autonomous supply mode. Although the conditioning

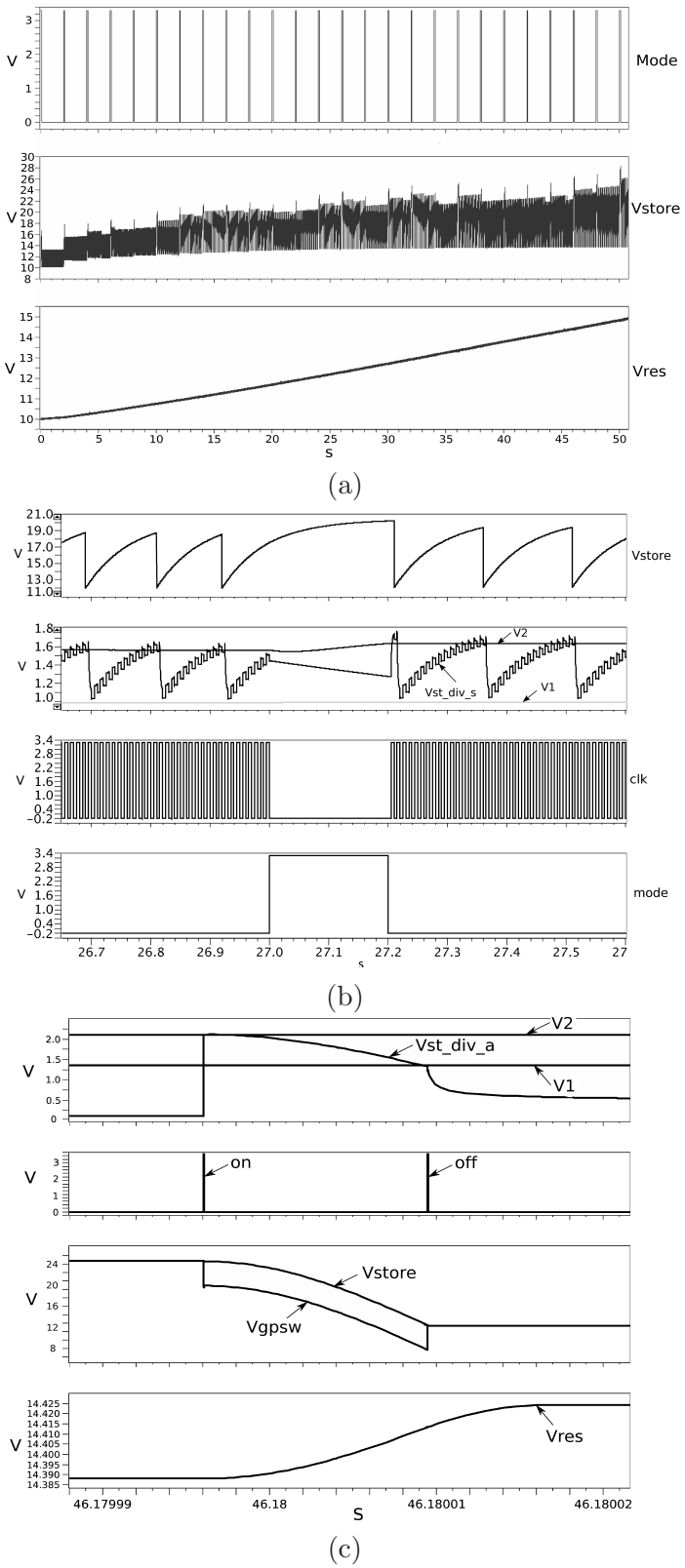


FIGURE 3.20: Simulation results of the proposed VEH IC: (a) Harvester long-term operation; (b) Zoom on the calibration phase; (c) Zoom on the flyback phase.

circuit and high-voltage blocks of the controller are fully autonomous (the power comes from the mechanical vibrations), the low-voltage sub-circuits of the controller are still powered externally. Nevertheless, we can account for the power consumption of these blocks and in future designs supply them with a fraction of the converted energy so to provide a fully-autonomous smart VEH system.

Fig. 3.20 presents the simulation results of the proposed VEH operation. Plots in (a) show the evolution of V_{store} and V_{res} during 50 seconds. It can be seen that V_{res} rises from 10 up to 15 V almost linearly. Hence the reservoir capacitor accumulates the energy with the average power approximately 1.25 μW; this figure includes the losses of the high-voltage blocks - V_1 and V_2 generator, both V_{store} voltage dividers, the flyback switch with its driver, as well as the losses in the non-ideal inductor and diodes. It can be noticed that the voltage limits of V_{store} (V_1, V_2) change after each calibration (the calibration corresponds to a small voltage peak on the diagram), and as V_{res} increases, the boundaries of V_{store} evolution become larger. The calibration/harvesting phases are managed by a digital signal Mode plotted on the top.

Plots in (b) focus on one of the calibration phase and several normal *charge pump-flyback* cycles before and after a calibration phase. It can be observed on the upper plot that after a calibration, the upper limit of V_{store} (V_2) noticeably increased. On the plot below it can be seen the evolution of the synchronously divided V_{store} (voltage $V_{st\_div\_s}$) and compared with V_2. During the calibration event, since the clock is zero the division and comparison of V_{store} do not occur, while V_1 and V_2 slightly increase, thus updating the optimal parameters for the charge pump operation during the next harvesting stage.

Plots in (c) show a zoom on one of the flyback stage. On the upper plot a division of V_{store} by a mos-divider and comparison with V_1 is shown. Both these events start as soon as a strobe signal *on* is high. During this short strobe signal, the gate voltage of the flyback switch V_{gpsw} is set to -2.8 V with respect to V_{store}, subsequently turning on the switch. In this way the flyback starts. V_{store} and its divided counterpart $V_{st\_div\_a}$ decreases. When $V_{st\_div\_a}$ reaches V_1 the comparator signals the end of the flyback and the control electronics generates the *off* pulse that turns off the flyback switch. During the flyback V_{res} increases as is receives the invested charges back via the DC-DC converter. After the switch goes off, V_{res} continues to increase since the freewheeling diode pushes the additional energy from the energized inductor to C_{res}.

The power consumption of the controller depends on many factors at once: frequency and amplitude of external vibrations, calibration frequency, control clock frequency, operation voltage range that depends on the accumulated energy in the system and on the external force of vibrations and, consequently, variation limits of the capacitance, and others. These factors are time-variable and often unpredictable. Also, different blocks of the controller are enable in Therefore, it is almost impossible to determine the exact values or limits of the power, unless using the simulation under a specific and known context.

According to simulation (Fig. 3.20), the average power consumption of the conditioning circuit with an adaptive flyback switch control is 846 nW. The most important conclusion is that this power is lower than the power converted and stored in the reservoir capacitor. Recall that the converted power is 1.25 μW including the losses of the diodes, inductor and all high-voltage sub-circuits of the controller.

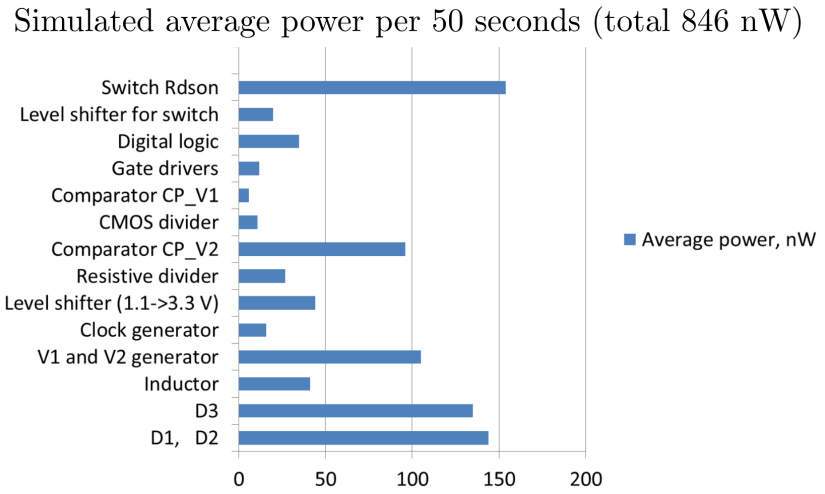


FIGURE 3.21: Contribution to the average power (per 50 seconds) by the conditioning circuit and the proposed adaptive switch controller. Parameters of simulation example: V_{res}=10→15 V, C_{max}/C_{min}=1.6, f_{ext}=298 Hz, A_{ext}=1 g.

The contribution to the power consumption of each sub-circuit or electrical component of the system is summarized in Fig. 3.21. Observing this diagram, we can notice that the most significant power is dissipated by the on-resistance of the flyback power switch and diodes D_1-D_3. One of the conclusion is that in our design we could significantly increase the channel width of the power switch, even at the expense of the increased dynamic power of the level shifting driver (due to larger gate capacitance of the switch). Indeed, the power of the level shifter is much lower. Also, the diodes should be replaced by the controlled CMOS switches so to eliminate the threshold voltage drop in conductive mode and, hence, reduce the losses in both, charge pumping and flyback, energy transfer phases. These corrections may be done in our future designs.

The efficiency of the harvester in this simulation example is less than 32 %, however, it can be further improved by the new enhanced versions of the MEMS transducer.

3.9 Summary

This chapter discussed the circuit-level implementation of a novel idea developed in the first part of this thesis concerning the adaptive optimal algorithm of the E-VEH system operation. This algorithm has been realized in a smart system module- the flyback switch controller. Since the harvester is supposed to operate at high-voltage so to have a high electromechanical coupling, the design of the integrated circuit of the controller evoked several difficulties. First, the problem of driving the flyback high-side CMOS switch appeared, since the gate of PMOS is referenced to the high-voltage source, whose voltage furthermore is variable in a large range. Secondly, a high-to-low voltage interface had to be added, because the signal processing is performed by a standard voltage logic.

Another major difficulty that we have faced, concerned the energy dissipation, which should not exceed the harvested energy.

The design was carried out in AMS035HV CMOS technology able to support voltages up to 50 V. We showed the state of the art of level shifters driving the high-side switch and proposed a novel ultra-low power architecture with a zero static current and a reliably shifted level that can be maintained during a long period without refreshing. This circuit prototype has been successfully fabricated and tested as will be discussed in next chapter. We also proposed a very-low power flyback switch controller IC that implements an auto-adaptive algorithm presented in previous chapter. Several parts of it, however, employ large external components (resistors), thus occupying a bulk volume of the whole system. They can be replaced by the on-chip solutions in our future designs. Nevertheless, the simulated power consumption of the implemented circuit is extremely low (0.85 μW) regarding the complexity of the circuit. To achieve such a low level of power, we used various approaches depending on the block and its function, such as: considerably reduce or eliminate the static current of the circuits, reduce the voltage supply, maintain transistors operation in weak inversion, minimize the frequency of energy wasteful operations, etc. The harvested average power is 1.25 μW (without considering the power of low-voltage sub-circuits); this power corresponds to the approximately linear increase of the voltage in 1μF-reservoir from 10 to 15 V during 50 seconds.

Chapter 4

Measurements of high-voltage switch and e-VEH

4.1 Overview

This chapter presents an experimental part of our research work.

At first, we show an experimental prototype of our ASIC and discuss the characterization of the high-voltage switch being implemented on-chip. Its characterization includes a set of tests measuring the power HV-PMOS, power consumption, and several electrical limitations of the level shifter circuit driving HV-PMOS. Each experiments is performed within a large supply voltage range. The experimental results have a good matching with simulation results, justifying a low power consumption of the circuit.

In the second part, we demonstrate the experimental measurements of a system of electrostatic vibration energy harvester that has been performed in collaboration with our research project partners in ESIEE Paris - Philippe Basset and his Ph.D student Raphaël Guillemet. A MEMS capacitive VEH prototype has been designed, fabricated and characterized in the context of a Ph.D thesis work of Raphaël Guillemet. In this work, we use of his device to test the harvested energy in the conditioning circuit, which structure consists of a charge pump and a flyback circuit, as well as our high-voltage switch. Experimental tests aim to measure, mainly, the harvested energy and the power generated in a charge pump and flyback circuit topology, to define any limitations for the harvester either of mechanical, or electrical nature and to estimate the flyback circuit efficiency.

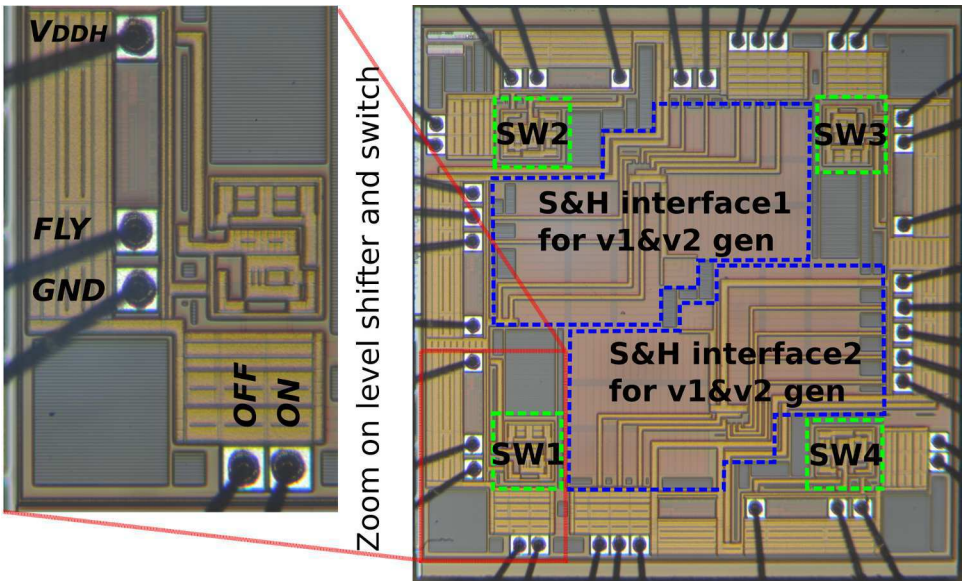


FIGURE 4.1: AMS H35 2.6 x 2.6 mm^2 silicon die micrograph of designed IC and a zoom on level shifter with a HV-PMOS switch and pads.

4.2 High-voltage switch: prototype and packaging consideration

4.2.1 Layout of the chip

The minimum charge for the fabrication in 0.35-μm HV-CMOS process (H35) comprises the price for 7 mm^2 of the die area including the pads ring. The designed high-voltage switch measures only ≈0.1 mm^2. Hence, we may have a very large empty space on a chip. In order to fulfill the minimum charged die area as efficiently as possible, we made the following. First, we replicated the HV switch four times and placed it in four corners of the chip close to I/O pads so as to minimize the routing paths. Secondly, we added a layout of the sample and hold (S&H) circuit interfacing the $V1\&V2$ generator, which schematic is given in Fig. 3.10. This S&H circuit contains four HV-NMOS transistors and two large 422-pF CPOLY capacitors, which represent analog memory elements. Finally, S&H circuit is replicated twice and two duplicates are placed symmetrically relative to the diagonal axis of the chip. Hence, the IC features a test mode that allows each system component to be enabled and evaluated individually, including four independent HV switch circuits (SW1..4) and two independent S&H circuits. From the practical point of view the availability of several identical circuits on the same die may be useful for accounting the process variations, however, this aspect is not addressed in this work.

The fabricated chip occupying 2.6x2.6=6.76 mm^2 silicon area is illustrated in die microphotograph in Fig. 4.1. The chip contains 37 pins including I/O and power pads, as well as ESD protection cells for each of individual circuit. The die thickness is 530 μm, which is a standard silicon thickness for H35 process. The bonding diagram of the chip is shown in Appendix C.

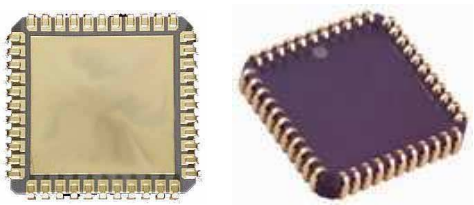


FIGURE 4.2: Ceramic J-Leaded Chip Carrier with 44 pins (JLCC44) package used in packaging this chip.

4.2.2 Packaging

For bonding and testing flexibility (e.g. easy access to the silicon die), the prototype has been packaged in a ceramic package. The choice of the ceramic package is also determined by the lower thermal resistance of ceramic material than that of plastic. Since the silicon die of the designed chip is rectangular (with its pads disposed along the four sides), the most adapted package is a so-called *quad* package, which offers pins on its four sides. Summarizing above considerations, a 44-pin JLCC (*J-Leaded Chip Carrier*) package with removable lids was chosen to encapsulate the designed 37-pins IC. The top and bottom view of such package is given in Fig. 4.2.

4.3 Characterization of the high-voltage switch

The HV switch IC is fully tested and characterized. Experimental measurements include the qualitative example of the circuit operation, power dissipation measurements (i.e. conduction losses, dynamic and static consumption), commutation speed performance, maximum on-state holding time without update and voltage limits determination.

The S&H IC measurements are not addressed in this thesis.

4.3.1 Measurement setup

The IC is tested using a breadboard, and not a PCB, mainly because of flexibility requirements and for the simplicity. Indeed, each experiment requires slight topological modifications, e.g. different test circuit configuration and various external components.

The packaged chip is placed to a socket and is connected to a breadboard using special wires and pins. The rest of testing board components are fully compatible with a breadboard. As mentioned in Chapter 3 the HV switch requires two standard voltage strobe signals ON and OFF in order to turn on and turn off the switch, respectively.

A circuit schematic that generates ON and OFF of the appropriate form is given in Fig. 4.3. Each strobe generator is implemented using a rise edge detector on external logic components and RC circuits. The duration of strobe pulses is set to approximately 400ns in order to guarantee that the state of the level shifter will change. Indeed, this value is several times higher then typical value from simulations. OFF pulse is produced with 17μs delay that is a typical duration of the flyback phase. The generator

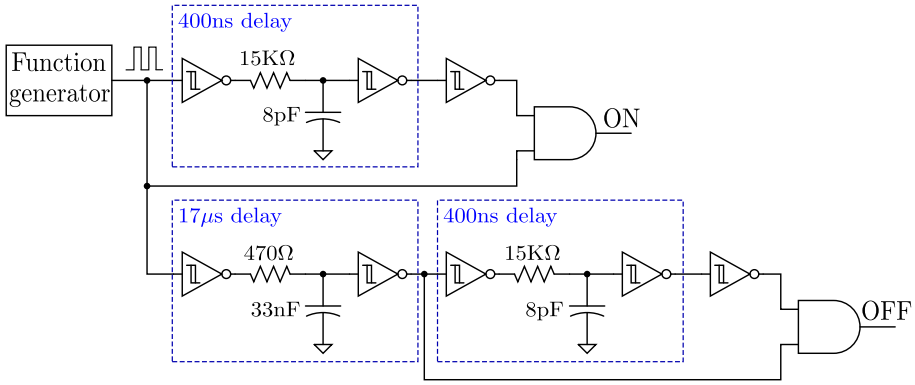


FIGURE 4.3: **ON/OFF Generator** implemented using the rise edge detector on external logic elements and RC-circuits.

is handled by a periodic square wave signal provided by a function generator FLUKE PM5136, which can operate within a frequency range 0.1mHz - 5MHz.

For the logic elements commercial ultra high speed components are employed. Thus, for the inverter gate we choose a high-speed CMOS Schmitt inverter M74HC14 from STMicroelectronics with a propagation delay between 16 and 155 ns (depending on supply voltage). For the logical-AND gate the component SN74AHC08N (Texas Instruments) is used whose propagation delay is typically 10.5ns for 3.3V supply voltage, according to the data-sheet.

All experiments envisage a relatively large range of high voltage DC source (V_{DDH}) – between 5 and 31 V. The top voltage is limited by the maximum supply voltage available in the experimental lab, however, the designed circuit may support up to 50V.

During the majority of experiments electrical parameters are measured with an oscilloscope. Since the probes of oscilloscope have insufficiently high input impedance (about 1-10 MΩ), the most sensitive analog nodes may be substantially affected. To avoid this issue, those nodes signals must be buffered with a special unity-gain operation amplifier with a very large input impedance. To buffer the nodes voltages up to 18 V an external 1 MHz bandwidth low offset (<1mV) operation amplifier AD549 is employed. This OPAMP operates at ultra low input bias current (<250fA). For the voltages higher then 18V, OPA445 circuit is employed, which has a wide-power supply range (from ±10V to ±45V). Its maximum input bias current is 10 pA for 2 MHz bandwidth. OPAMPs are powered with separate supplies that are sufficiently above V_{DDH}.

4.3.2 Qualitative example of the HV switch operation

The first experiment is intended to assure that the fabricated HV switch is operable and it works as expected. That is a simple experiment, during which the HV switch controlled by ON/OFF signals is forced to connect the R_{SH} load to a high voltage DC source (V_{DDH}) as shown in Fig. 4.4.

Fig. 4.5 show six measuring results of HV switch operation, where each plot corresponds to the experiment with V_{DDH} in voltage range [5-31V]. An earliest rough conclusion

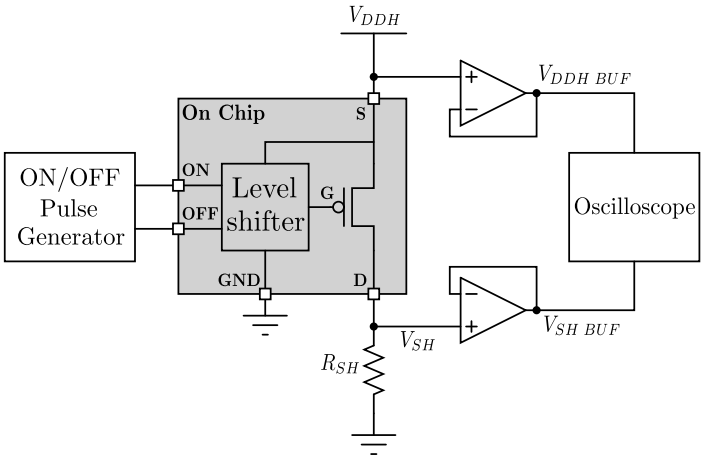


FIGURE 4.4: Experimental setup intended to test the operational capability of the IC. Operation amplifiers buffers V_{DDH} and V_{SH} signals.

obtained through this experiment is that the HV switch operates as expected, it closes and opens with ON and OFF signals respectively. The 3V magnitude of control signals ON and OFF during 400ns is more than enough to change the state of the level shifter, though within a full V_{DDH} range.

It can be observed as well that after the switch is opened V_{SH} decreases slowly. This delay is determined by 10KΩ load resistance and parasitic pF-range capacitance present in pads.

4.3.3 Energy and power consumption

Power and energy consumption of the HV switch are the critical issues for our application and a great amount of effort has been devoted to estimate these parameters in the early design phases using the powerful modeling and simulation tools.

The overall energy dissipation of the HV switch can be split up on three components : the conduction losses associated with a power HV-PMOS transistor, the dynamic losses of the level shifter while triggering to a new state and the static losses of the entire HV switch. Measuring experiments and corresponding results allowing to know the entire energy dissipation of the circuit are described in this section. Additionally, measuring results are compared with the simulation results.

4.3.3.1 Conduction losses of the power PMOS switch

Since the closed CMOS switch corresponds to the ohmic resistance of the channel, the ON resistance (R_{ON}) impacts the voltage dropout across the source and the drain terminals (V_{ds}). The goal of this experiment is the determination of the ON resistance value in order to account to the conduction power consumption of the switch equal $P = {V_{ds}}^2/R_{ON}\ t_{on}\ f$, where t_{on} is the duration of the conduction and f is the switching frequency.

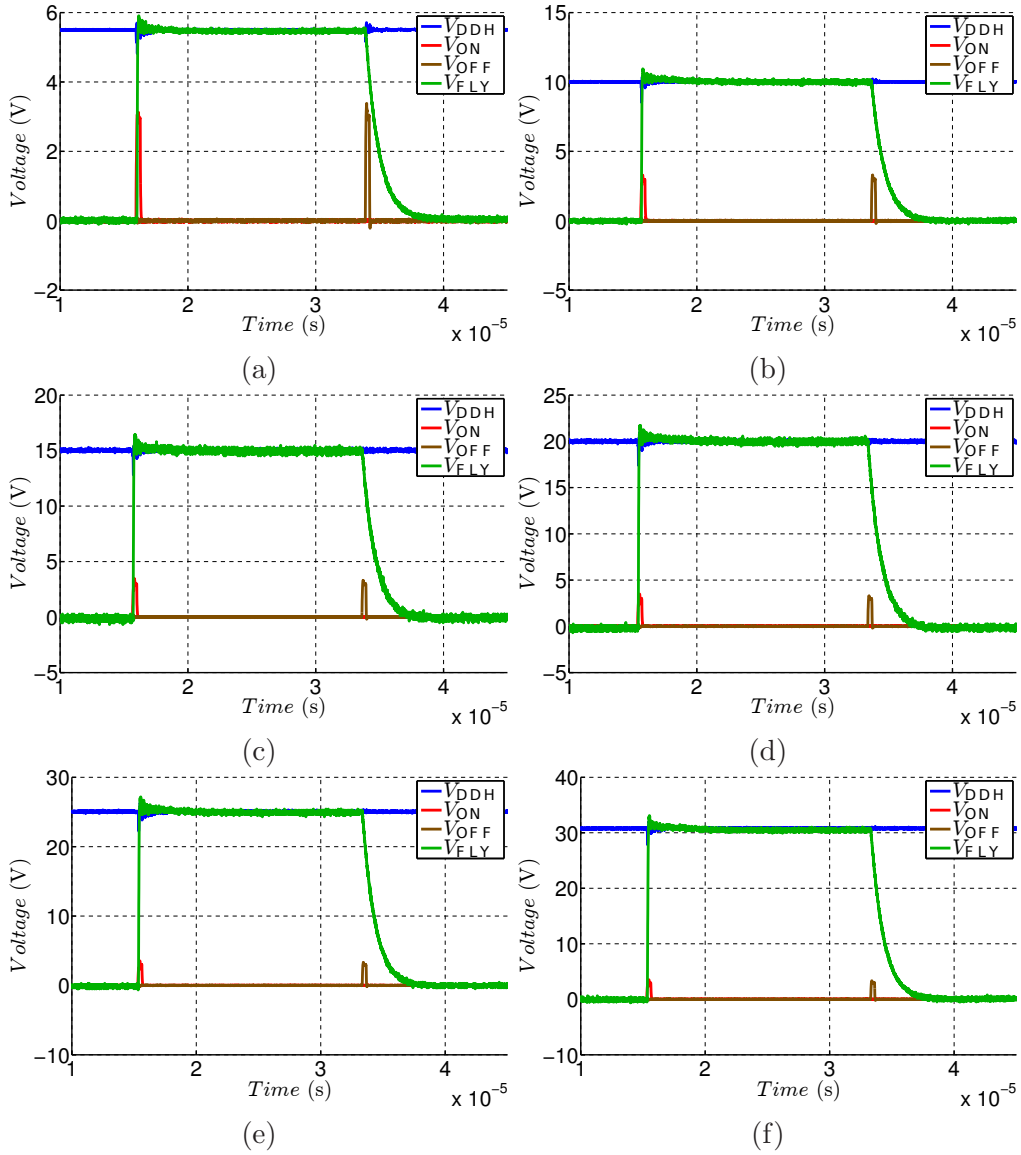


FIGURE 4.5: Qualitative examples of HV Switch operation corresponding to V_{DDH} equal to: (a) 5.5V, (b) 10V, (c) 15V, (d) 20V, (e) 25V, (f) 31V.

An approach of determination of the switch ON-resistance is as follow. Considering that the gate-source voltage (V_{gs}) of the closed HV-PMOS transistor is fixed (set by the level shifter) and that the bulk terminal is connected to the source, the voltage drop on the closed transistor depends mainly on the current flowing through it:

$$V_{ds} = I\,R_{ON}, \tag{4.1}$$

From above expression measuring V_{ds} and I lets to know the value of the ON resistance. As shown in Fig. 4.6 an experimental setup allowing measurements of V_{ds} and I has the following structure. A high supply voltage V_{DDH} is connected to an IC pin, which interconnects a source terminal of HV-PMOS and a level shifter supply. ON pin is connected

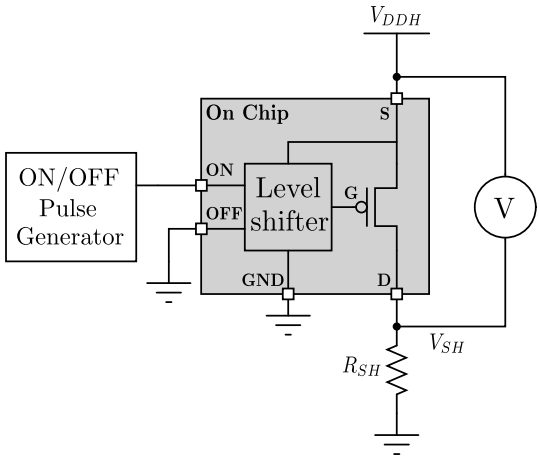


FIGURE 4.6: Measurement setup scheme for measurement of *ON*-resistance of the switch

to a periodic strobe pulse generator, whereas OFF is grounded. Being periodically updated by *ON* pulses the level shifter keeps a steady on-state (with a fixed V_{gs}). In this way HV-PMOS maintains reliably closed drawing a continuous current from V_{DDH} to ground through the switch and the shunt resistor R_{SH}. Because the value of R_{SH} is known, by measuring the voltage drop across the it (V_{SH}) makes possible to calculate the current in the branch using Ohm's law. V_{SH} is measured with a high-precision digital multimeter ($6\frac{1}{2}$ digits) HAMEG HM8112-3. Then, subtracting V_{SH} from V_{DDH} the value of V_{ds} is obtained. Finally, knowing the current in the branch and using Eq.4.1, the ON resistance is calculated.

The characterization of R_{ON} comprises a set of experiments with various operation conditions of the setup. Thus, the circuit is tested within a supply voltage range from 5 to 31 V with 1 V step. Additionally, different nominal shunt resistors (namely, 820Ω, 2.2KΩ, 10KΩ, 15KΩ, 22KΩ, 27KΩ, 47KΩ, 82KΩ) are employed to provide various amounts of current flowing throughout the switch.

A relation between the measured R_{ON} and the high voltage supply (up to 31 V) is given in Fig. 4.7. As can be noticed from those measurements results, for different currents ranges that transistor conducts the ON-resistance is found within 32 and 46 Ω. This is a fair result for such a transistor aspect ratio ($\frac{1000\mu m}{1\mu m}$) and for its input gate-source voltage $V_{gs} \approx 2.7V$, according to simulations.

Also, measurements results are plotted alongside the simulation results in the form of the volt-ampere characteristics as shown in Fig. 4.8(a-h). Presented plots illustrate the HV-PMOS operation in the triode mode. Indeed, drawn characteristic curves have a quasi-linear form, except for the first plot (a), which has a relatively high current, where transistor enters into the saturation regime. The current range for every plot is set by V_{DDH}.

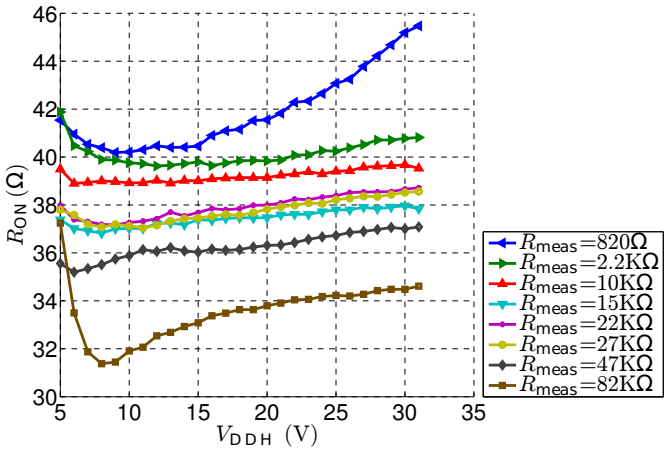


FIGURE 4.7: Switch R_{ON} resistance for different supply voltages V_{DDH} and currents set by R_{SH} load resistors

4.3.3.2 Dynamic losses

As we previously said the level shifter constitutes a dynamic flip flop configuration having two opposite states, which are stored in the internal level shifter's capacitors. The change of states is provided by recharging those capacitors when ON or OFF event occurs. Determining the amount of charge Q injected and redistributed in capacitors during a triggering event allows to know the wasted energy for that event.

Notice that not the entire electrical charge injected to the circuit is used to recharge the capacitors. A part of it is consumed by diodes serving for clamping the gate-source voltage V_{gs} of HV-PMOS when the capacitors are recharged and hence protecting the switch from V_{gs} breakdown. Unfortunately, there is no possibility to measure separately the charge serving for capacitors recharging and the charge consumed by diodes since these elements are inside IC. The methodology of determining the entire charge injected to the circuit consists in indirect measuring and integrating the current drawing from V_{DDH} during a short period when either ON or OFF pulse is high.

The measurement setup allowing to measure the injected charge is given in Fig. 4.9. ON and OFF strobe signals are generated with 17μs delay between them, respectively, and this sequence is repeated periodically. V_{FLY} is a floating node insuring the open circuit behavior during the conduction of the switch. The shunt resistance R_{SH} is connected in series with the IC between V_{DDH} and V_{SH}. In this way when ON or OFF is enabled the level shifter draws a current from V_{DDH}, which can be measured through the voltage drop on shunt resistor. R_{SH} nominal value is a trade-off result. On the one hand it must not be overstated so to avoid significant reduce of V_{SH}. On the other hand it should be high enough to insure a reliable measurements accuracy. A compromise was experimentally found by choosing R_{SH}=1.2KΩ. V_{DDH} and V_{SH} buffering via OAs are sensed by oscilloscope probes. Using mathematical tools of the digital oscilloscope electrical charge Q can be find as follow: the voltage drop on resistance $V_{DDH} - V_{SH}$ is

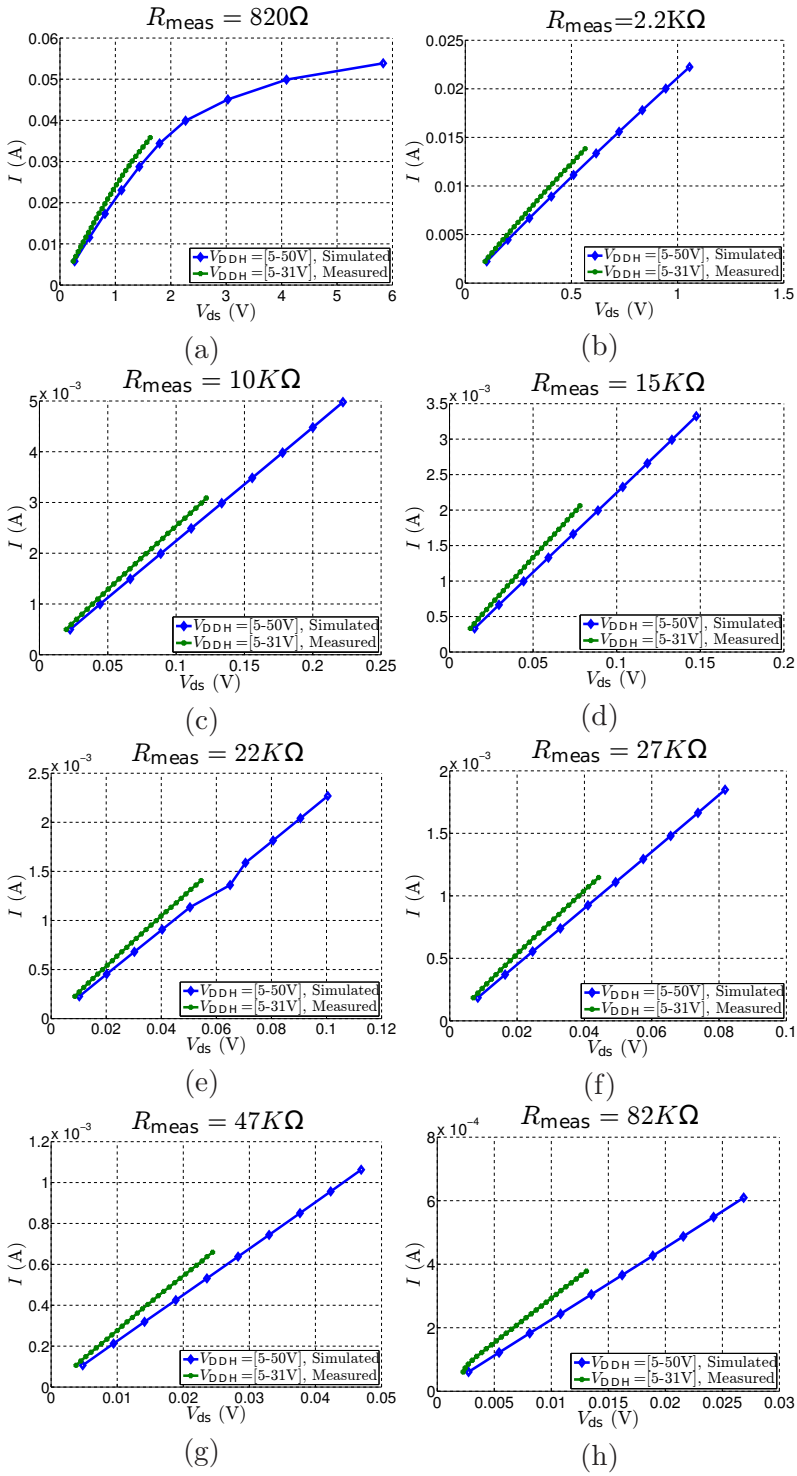


FIGURE 4.8: $I_d - V_{ds}$ characteristics of High-Voltage PMOS transistor at a set of the following load resistors:(a) 820Ω, (b) 2.2KΩ, (c) 10KΩ, (d) 15KΩ, (e) 22KΩ, (f) 27KΩ, (g) 47KΩ, (h) 82KΩ. Transistor parameters: $W = 1000\mu m, L = 1\mu m, V_{gs} \approx 2.7V$.

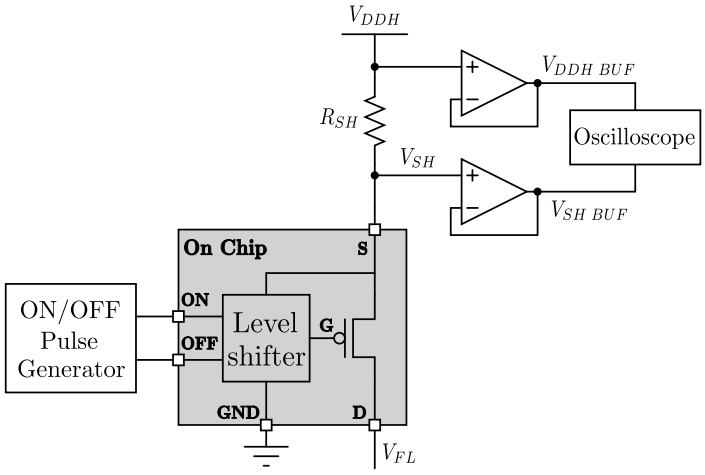


FIGURE 4.9: Experimental setup for measuring the dynamic energy dissipation of the level shifter

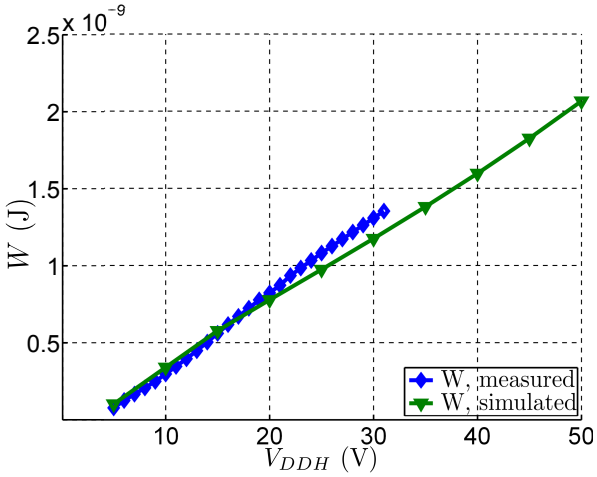


FIGURE 4.10: Energy loss during level shifting from one level to another (ON or OFF)

integrated during one ON pulse and divided by R_{SH} resistance:

$$Q = \frac{1}{R_{SH}} \int_0^{t_{ON}} [V_{DDH}(t) - V_{SH}(t)]\, dt \tag{4.2}$$

The energy wasted to the charge injection is defined below:

$$W = \frac{1}{2} Q V_{DDH} \tag{4.3}$$

The calculated energy is plotted versus V_{DDH} in Fig. 4.10. As illustrated, measuring results have a good matching with the energy values obtained by simulations. The average power consumption for a periodic level shifting can be expressed by multiplying the energy on the frequency. Fig. 4.11 presents an example of the average power at 20Hz switching frequency, which is a typical frequency for the flyback commutation.

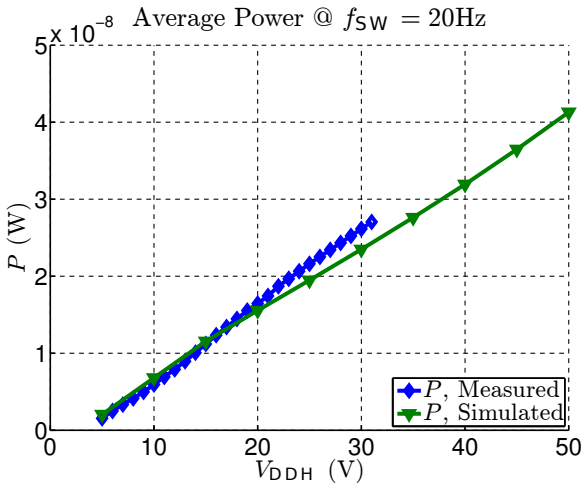


FIGURE 4.11: Dynamic power consumption

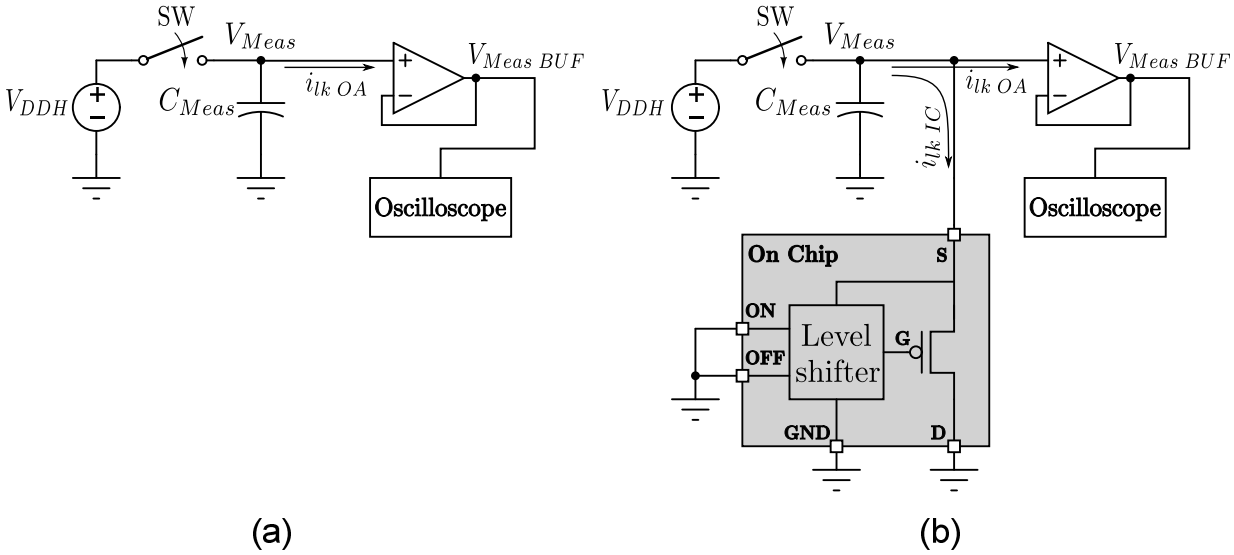


FIGURE 4.12: Experimental setups for measuring the leakage current of the HV switch: (a) measurement of C_{Meas} leakage current via the input of OPAMP; (b) measurement of C_{Meas} leakage current via the input of OPAMP and via the measuring IC pin;

4.3.3.3 Static losses

Leakage currents in H35 process are usually in pA or nA range depending on several factors such as applied voltage, charging period, temperature and others. The difficulties of identification such very small currents concern the issue of insufficiently high input impedance of measuring instruments (e.g. probes of oscilloscope) that draw more current than present leakage. That is why to account for a rough level of the leakage a need of a special operation amplifier with a very high input impedance is mandatory, as mentioned in section 4.3.1. In this way the weak leakage current can be converted to a low output impedance voltage that can be measured. However the measurement of extra low voltages is difficult due to measuring signal noise and hence measurements results may be nullifying.

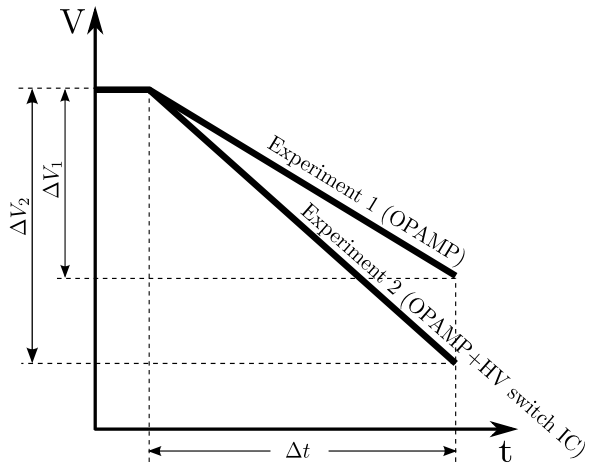


FIGURE 4.13: Illustration of principle of the experiment. Discharge buffered voltages $V_{Meas\,BUF}$ slopes for two experiments (i.e., with and without LS)

A proposed approach of leakage current determination reduces the measuring signal noise error. An experiment consists of two measurements stages.

- First we pre-charge an external measurement capacitor C_{Meas}=33nF with a supply voltage V_{DDH} as shown in Fig. 4.12(a). Then we disconnect the supply. Due to the leakage current $i_{lk\,OA}$ through the input of OPAMP the voltage across the capacitance V_{Meas} decreases. We measure with oscilloscope probe an equivalent voltage $V_{Meas\,BUF}$ during a short time interval Δt corresponding to a quasi linear curve of C_{Meas} discharge as demonstrated in Fig. 4.13. During that time the capacitor discharges by ΔV_1.
- For a second measurement we repeat the same procedure under identical experimental conditions except one modification in the setup. We connect the HV switch IC in parallel to C_{Meas} as shown in Fig. 4.12(b). In this way the leakage current from C_{Meas} is more intensive since it is consumed by the OPAMP ($i_{lk\,OA}$) and the HV switch IC ($i_{lk\,IC}$). As a result during the same time Δt the capacitor voltage decreases by a superior value ΔV_2.

Hence, measuring $V_{Meas\,BUF}$ during each experiment makes possible to find the slopes of voltage curves and so to calculate the total amount of leakage current i_{total1} and i_{total2} following expressions given below:

$$\begin{cases} i_{total1} = i_{lk\,OA} = C_{Meas}\frac{\Delta V_1}{\Delta t}, \\ i_{total2} = i_{lk\,OA} + i_{lk\,IC} = C_{Meas}\frac{\Delta V_2}{\Delta t}. \end{cases} \tag{4.4}$$

In these expressions we neglected the parasitic capacities of input pins and wire parasitic resistance because only the differential value plays the role. The difference between i_{total2} and i_{total1} corresponds to the current consumed only by the IC:

$$i_{lk\,IC} = i_2 - i_1 = \frac{C_{Meas}}{\Delta t}(\Delta V_1 - \Delta V_1) \tag{4.5}$$

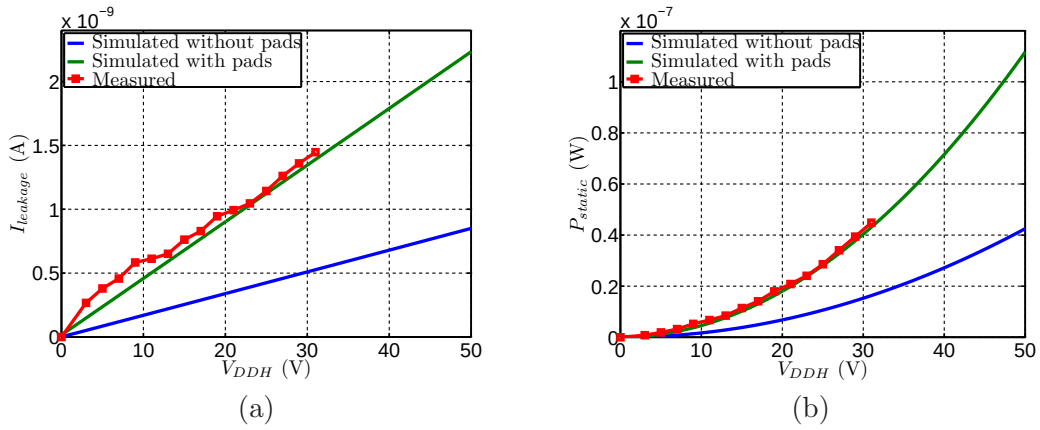


FIGURE 4.14: a) Leakage current of LS; Static power consumption of LS.

The measurements are performed within the V_{DDH} voltage range [3 - 31 V] with 2 V sweep step. The leakage current of the level shifter calculated with Eq. 4.5 is plotted by red curve with rectangular markers in Fig. 4.14a. It can be seen that the measured leakage current is just slightly greater than the leakage current obtained from simulations performed with the use of ESD protection pads. Both curves represent significantly higher leakage current than those obtained by simulation of only the level shifter schematic without the ESD protection pads. It can be concluded that the employed power pads are the source of considerable leakage.

The static power consumption is a product of the leakage current and the supply V_{DDH}. Measured and simulated static power versus HV supply is displayed in Fig. 4.14b.

4.3.4 Maximum ON-state duration without update

The manufactured high voltage switch is particularly designed for a flyback circuit operation, where the switch is intended to conduct mA-current during a short period (i.e. few tens of micro-seconds). Nevertheless, we wanted to know whereas the HV switch suits applications where the time of conduction is much longer.

Ideally, when the switch becomes closed after ON signal, it must remain closed infinitely until OFF becomes high. But in reality, the closed switch after some interval becomes opened without any external command. This undesirable and inevitable issue happens because the gate-source voltage V_{gs} of switch decreases with time (due to the leakage currents from the LS's and HV-PMOS gate capacitance).

The goal of this experiment is to measure how long does the switch can remain closed once being turned on. A single strobe signal ON is provided from the strobe generator while OFF is connected to ground as illustrated in Fig. 4.15. V_{SH} is loaded by $1M\Omega$ shunt resistance and is measured through the buffering amplifier (as in previous experiments).

Fig. 4.16 show a scope of measurements results, where V_{SH} is being connected by the switch to V_{DDH} at time 0. Every curve in this plot corresponds to the experiment

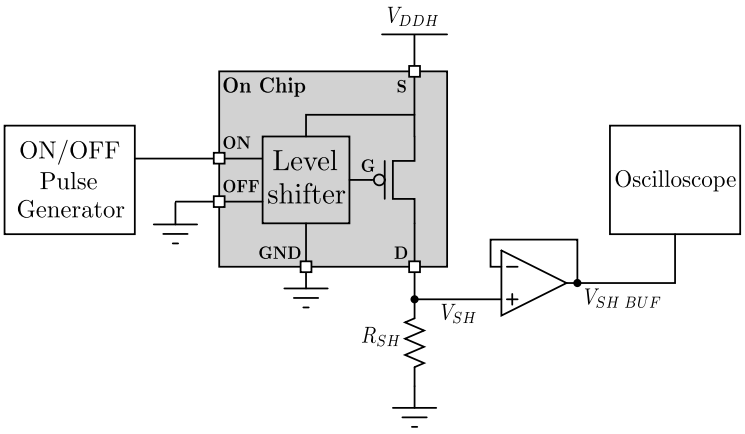


FIGURE 4.15: External amplifiers buffering V_{FLY} for measurement of duration of *on*-state of the level shifter

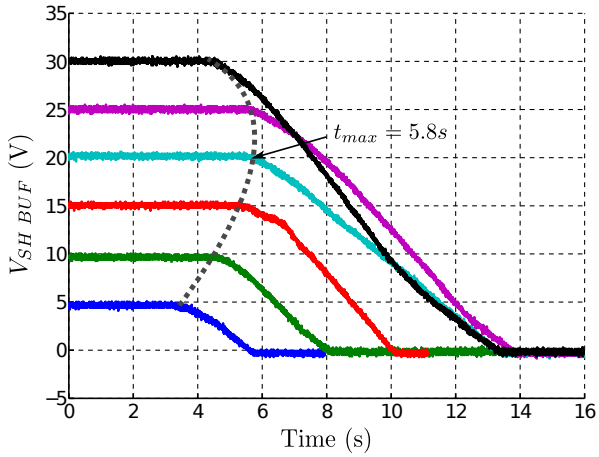


FIGURE 4.16: Experimental measurements showing the maximum time that LS can hold the ON-state, where the switch is close.

with different supply voltage V_{DDH} ranging from 5 to 30 V. From these plots the main conclusion is that LS can keep its on-state during several seconds that is much longer then our μs-flyback application.

From theoretical point of view while the supply voltage V_{DDH} rises the leakage current from capacities must increase as well. This, in turn, must cause them to discharge faster. However, as experiments show such a trend can be observed only for voltages higher then 20 V. A credible explanation is that with voltages lower then 20 V the pre-charge current was smaller and not yet saturated. Hence for equal time for all experiments capacities were charged with lower voltage level that lied in turn in their faster discharge.

4.3.5 Speed performance

The speed of closing and opening the switch is determined by the time needed the level shifter to change its state. To be more precise this time is considered as the difference

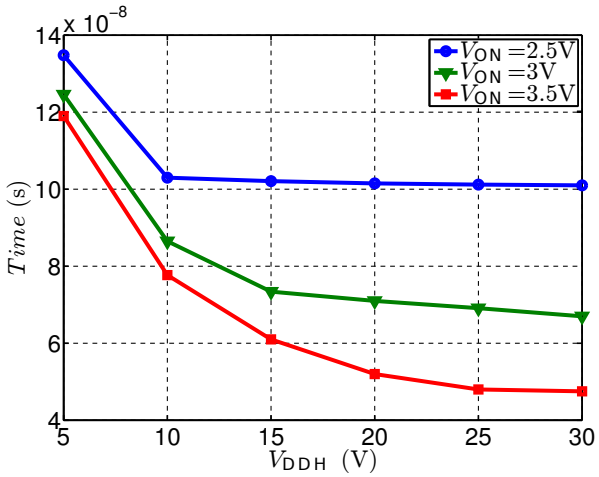


FIGURE 4.17: Level shifting speed performance.

between the moment when the pulse ON or OFF starts to rise and the moment when the level shifter state is reliably reset.

The experimental setup is the same as in Fig. 4.4. A set of measurements is performed for supply voltages ranging from 5 to 30 V with 5 V step and for input strobe voltage magnitudes equal to 2.5 V, 3 V and 3.5 V.

As illustrated in Fig. 4.17 while lower supply voltages are applied longer settling time is needed. This is because of smaller currents recharging the LS's internal capacities. For higher voltages the settling time reduces and becomes less dependent on V_{DDH}. This effect is the consequence of the saturation of input transistors as explained in chapter 3. It is also noticeable that applying lower input voltage (V_{ON}) input transistor saturates faster (e.g. at 10 V for 2.5 V input voltage, at 15 V for 3 V input, and only at 25 V for 3.5 V input voltage).

In Fig. 4.17 the the measured speed performance concerns only the turning-on phase of the switch. However, for the turning-off almost the same performance can be obtained, since the same equivalent capacity must be charged with practically the same amount of charge.

A general conclusion drawn from resulting plots is that the fabricated level shifter is quite fast being capable to turn on/off the switch during tens/hundred ns-range depending on control and high supply voltage levels.

4.3.6 Voltage limits consideration

Fig. 4.18 illustrates the relation between the minimum V_{DDH} voltage to be switched and the magnitude of the input signals V_{ON} and V_{OFF}. Indeed, for lower input voltage a higher V_{DDH} must be applied in order to provide a minimum current able to recharge the LS's capacitance. Thus, for the case of $V_{ON} = 2.1V$ the minimum V_{DDH} must be 10V in order to provide a correct level shifting. At the same time, if V_{ON} pulse has a

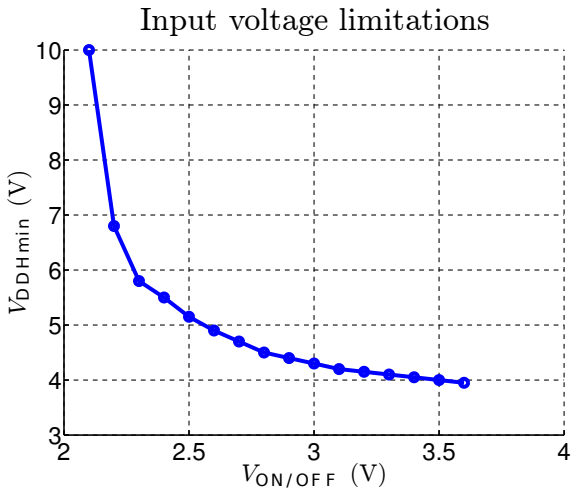


FIGURE 4.18: Minimum V_{DDH} voltage that can be applied to level shifter with respect to the control voltage level of V_{ON} and V_{OFF}

magnitude 3.6V (maximum V_{gs} for 0.35-μm process), the minimum allowed V_{DDH} can be of about 4V.

4.4 E-VEH prototype and measurement setup

As the fabricated flyback switch is fully characterized, it is now placed into the energy harvesting circuit with the goal of measurement the harvested energy. The mechanism of the conditioning circuit described in Chapter 2 consists of two phases: energy accumulation in the intermediate storage unit C_{store} (charge pump) and recharge of a reservoir capacitor C_{res} with an inductive flyback circuit. In this research, we serve the electrostatic transducer based on silicon-based MEMS technology, which was designed, fabricated and tested by our research project partners in ESIEE Paris [Guillemet13] (Philippe Basset and his team).

4.4.1 Experimental setup and goals of tests

The overall experimental setup consists of numerous instruments as demonstrated in Fig 4.19. A vibration environment is reproduced by a low force electro-dynamic shaker LDS 406, which is able to operate in the frequency range of 5 to 9000 Hz. It is controlled by an LDS PA100E power amplifier, which in turns is driven by a sinusoidal AC voltage source provided by an arbitrary function generator TEKTRONIX AFG3102. The vibrating table stress behavior is screening by a vibration controller instrument of Brüel&Kjaer (type 7541), thus providing a graphical interface at a screen of PC's monitor for a precise manual control of the shaker. Moreover, vibration controller features an automated control of the shaker amplifier. Also, a measurement setup employs a digital microscope (Dino-Lite) in order to observe the behavior of the MEMS device as the last is submitted to mechanical stress. The data acquisition of the measured circuit's signals

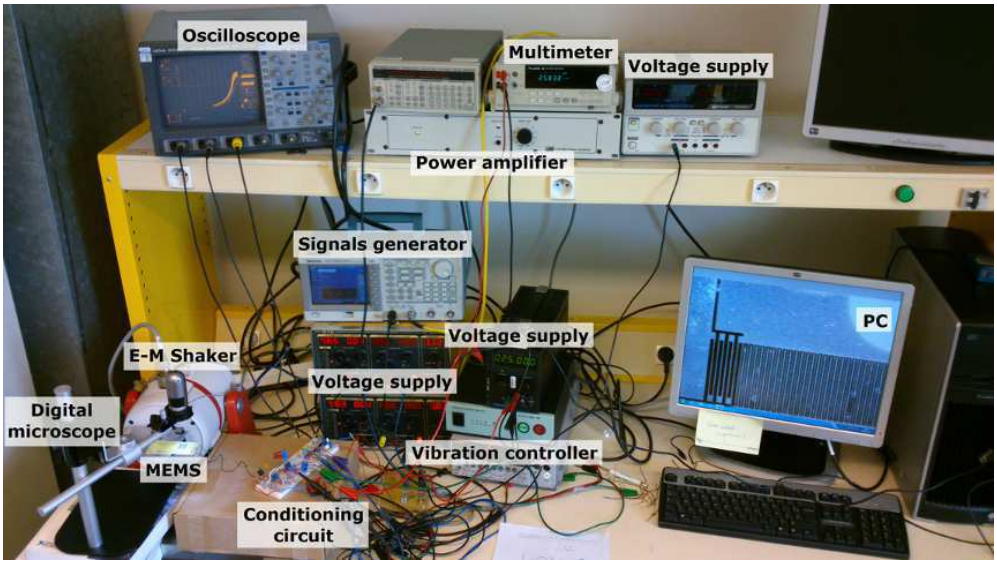


FIGURE 4.19: Picture of the overall experimental setup

is provided by a digital oscilloscope LeCroy 9354AL and a PC with a specific software *Scope Explorer*.

4.4.2 MEMS device prototype

This work deals with an out-of-plane gap-closing electrostatic transducer. The movable mass of the transducer is attached to the rigid frame by 4 linear serpentine springs. Mechanical stoppers located between the mass and the frame prevent from short circuits between fixed and movable fingers. The transducer is designed and fabricated in silicon-based MEMS technology through fully batch fabrication process, which requires only two lithography masks. The movable part is etched by DRIE (Bosh process) in a 380 μm-thick doped silicon wafer using an aluminum hard-mask layer. The silicon etching has an intentional small undercut of about 0.8%, resulting in a trapezoidal cross section of the comb-fingers. Then a glass wafer, which is used only as a handle wafer, is etched by liquid HF below the mobile part in order to allow the displacement of the MEMS. Finally, both silicon and glass wafers are anodically bonded. After dicing, each e-VEH is glued onto a PCB, which, in turn, is glued to a vibrating shaker. Pictures of the MEMS device are shown in Fig. 4.20. The mobile mass is estimated to be equal to 63.3 mg and the total area/volume of the active parts (i.e. mass+springs+comb's fingers) is 1.1 cm^2/0.042 cm^3.

4.5 Measurements of e-VEH

This part discusses tests of the electrostatic vibration energy harvester employed in Yen's conditioning circuit (based on charge pump and inductive flyback), which was described in details in chapter 2. This work represents a complement to the characterization of the

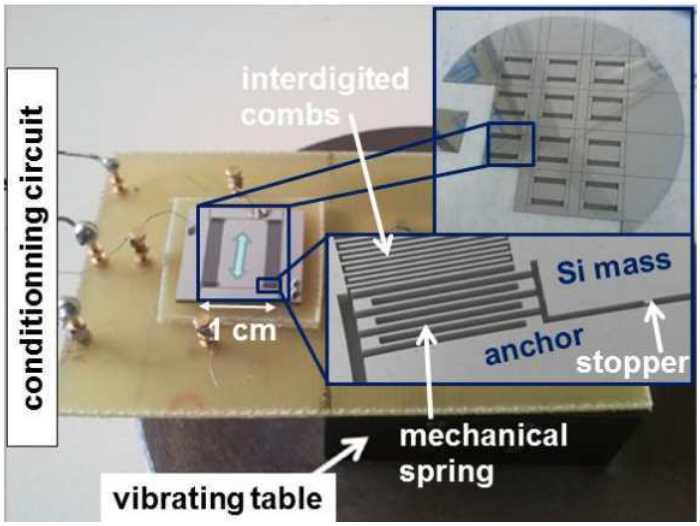


FIGURE 4.20: Picture of the MEMS electrostatic energy harvester harvester [Guillemet13]

fabricated in ESIEE e-VEH recently performed by R. Guillemet, who employed more simple circuits for transducer characterization using the RC_{var} circuit, and a charge pump circuit with a resistive return, where a resistor is connected between the storage and reservoir capacitor, instead of an inductive flyback.

This work includes several experiments. Previous to test the transducer within Yen's conditioning circuit, it is required to determine the variation of the variable capacitance in response to the mechanical excitation. Additionally, since the transducer is a resonant device, it is necessary to measure its resonance frequency and bandwidth at various mechanical accelerations and electrical voltages applied to the structure. Then, as required preliminary tests are done, is is possible to perform the main measurements that consist in characterization of the global system operation within a wide operation voltage range between 3 and 30 V across C_{res} capacitor. A few tests include long-lasting measurements of the harvested energy accumulated in a reservoir capacitor with a transducer submitted to external vibrations in the form of harmonic sinusoidal signal and of the Gaussian noise. The purpose is to initialize the e-VEH system with some amount of electrical energy and let the system to increase its energy level by accumulating the converted energy in a reservoir capacitor. It is required to characterize the harvested power, as well as the electrical and mechanical limits of the system. By these measurements, the flyback circuit efficiency is being characterized as well.

4.5.1 Characterization of MEMS device

In the Ph.D. thesis of R. Guillemet [Guillemet12] the detailed characterization of the fabricated MEMS transducer is provided, including measurements of the capacitance variation, its resonance frequency, quality factor, etc. The quality factor Q of the resonator represents its capacity to conserve its mechanical energy during vibrations. Higher is Q, lower is the dissipated energy, which is caused by various factors such as the damping of the air, internal viscosity of the material, viscoelastic properties of the

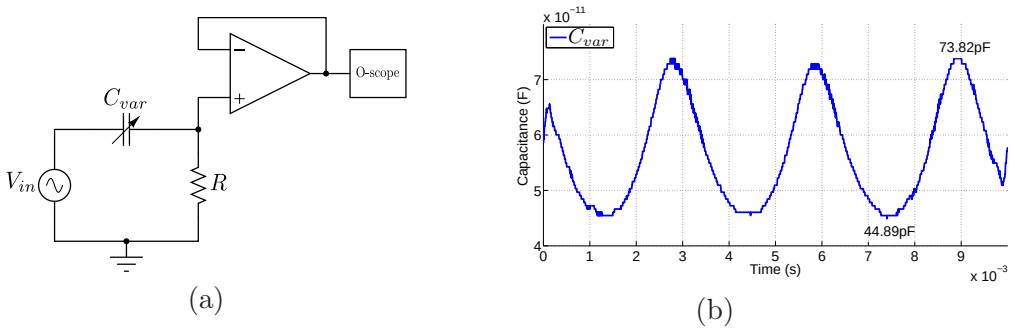


FIGURE 4.21: (a) RC circuit for the dynamic measurement of the transducer variable capacitance C_{var}; (b) Dynamic measurement results of C_{var} variation with time at atmospheric pressure, 1 g acceleration, and with no DC voltage applied.

glue, which connects the resonator to the PCB, etc. According to the measurement of R. Guillemet, $Q = 11$ - is quite poor for a structure vibrating at the air pressure 760 Torr, while this factor can be improved with decreasing the air pressure (e.g. $Q = 17$ at 15 Torr). The resonance frequency of the structure at atmospheric pressure with no voltage applied is 162 Hz, according to test results described in [Guillemet12].

In order to measure the variation of the transducer capacitance C_{var} a simple circuit is mounted; its schematic is shown in Fig. 4.21a. The mechanical resonator gets exited by mechanical vibrations applied in-plane, resulting in variation of the capacitance C_{var}. Dynamic measurement of C_{var} is achieved by measuring the voltage phase shift in a RC_{var} circuit, which is supplied by an AC voltage V_{in} at a frequency several orders higher than the vibrations frequency. This method was described in details by A.M. Paracha in his Ph.D. thesis [Paracha09a]. The dynamic capacitance value is calculated as:

$$C_{var} = \frac{1}{tan(\Theta)R\omega}, \tag{4.6}$$

where ω is the angular frequency of V_{in}, Θ is the phase shift between the voltage across the capacitor and the voltage generated by the source, and its precision is determined by the oscilloscope date sampling period T_s.

The measurement is done at atmospheric pressure (around 760 Torr) with an applied external acceleration 9.8 m/s^2 with a resonant frequency 162 Hz. A series resistance R equals $15K\Omega$. The observed measurement result is shown in Fig. 4.21b. At given mechanical parameters and environmental conditions, C_{var} varies between 45 pF and 74 pF. The precision of the measurement is 1.259 %, that corresponds to the error of 0.7 pF.

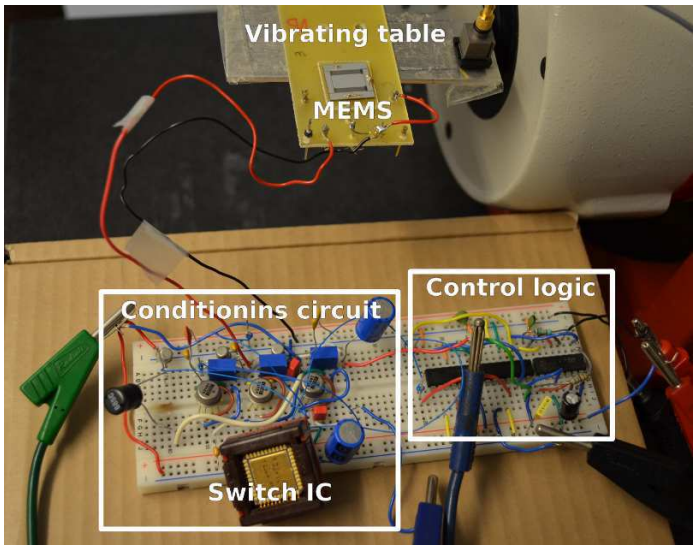


FIGURE 4.22: Picture of the measurement setup, illustrating the conditioning circuit and the control logic mounted on the breadboard and the

4.5.2 Tests of e-VEH within the charge pump and flyback conditioning circuit

4.5.2.1 Conditioning circuit setup

The conditioning circuit is mounted on discrete components on the same circuit board as for testing of the high-voltage switch for the reasons of the simplicity and flexibility. The picture of the experimental circuit setup and its corresponding schematic diagram are given in Fig. 4.22 and 4.23 respectively. The conventional circuit is complemented by a pre-charge circuit (DC voltage source and a switch) in order to energize C_{res} with an initial energy. The flyback switch is driven by the same ON/OFF generator as in Fig. 4.3. Sensitive signals to be measured, such as V_{res} and V_{store}, are buffered by high-input impedance unity-gain OPAMPs, in order to avoid leakage currents through the measuring probes, as discussed in section 4.3.1.

4.5.2.1.1 Passive components selection

The used charge pump capacitors are of the same value as in the model: C_{res}=1 μF, C_{store}=3.3 nF. As our design is intended to operate autonomously, accumulating the energy in the capacitors, the losses associated with capacitors must be minimized by a choose of a proper type of the component. In order to minimize losses in the capacitors we must consider two factors: the leakage currents, flowing through the dielectric due to the influence of the powerful electric fields applied to the plates, and the equivalent series resistance (ESR). According to this requirements we have chosen the metallized polypropylene film capacitor for C_{res} (*PANASONIC - ECWF2105JA*) and a ceramic capacitor for C_{store} (*AVX - MR061A332JTA*).

The main criteria for the use of the inductor was the minimal series wire resistance for a high nominal inductor 15 mH. The most suitable component available for the purchase

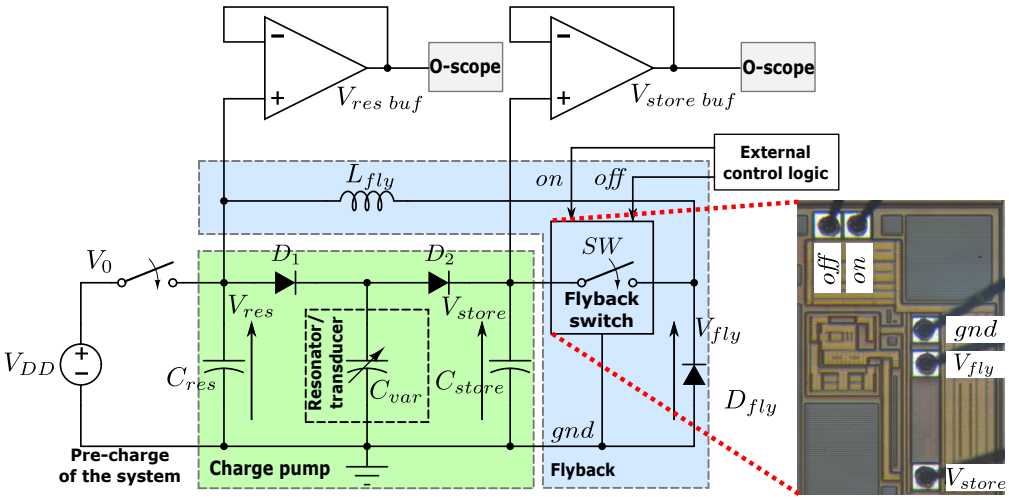


FIGURE 4.23: Schematic of the setup for characterization of both, MEMS-device and integrated flyback switch, in context of the [Yen06] conditioning circuit

was *Murata - 13R156C*, which wire-wound resistance is 31 Ω and, which can support the current up to 80 mA (whereas the specified maximal current of the flyback is less 15 mA).

4.5.2.1.2 Diodes selection

The criterion for selection the diodes was the low reverse leakage current to avoid the discharge of the initial charge stored in the harvester. Suppose that the initial charge stored on C_{res} is Q_0 so that

$$Q_0 = C_{max} V_0, \tag{4.7}$$

The reverse current of the diode for a cycle of the capacitance variation (charge pump cycle of a period T_{cycle}) is then given as:

$$I_{reverse} = \frac{Q_{leak}}{T_{cycle}}, \tag{4.8}$$

where Q_{leak} is the charge loss due to a reverse current. Hence, from Eq. 4.7 and 4.8 diodes must satisfy the following condition:

$$C_{max} V_0 >> I_{reverse} T_{cycle}, \tag{4.9}$$

So the diode with the smallest possible reverse current must be selected.

Suppose that the system can be pre-charged with 20 V, hence, $Q_0 \approx 1.5$ nC (for $C_{max} = 74pF$). The selected diode is a JPAD5 (from *Calogic corporation*), which has 5 pA reverse leakage current. So, with the electrical frequency of 250 Hz, $Q_{leak} = 20$ fC, so the leakage current is negligible.

Initially, the reservoir capacitor C_{res} is pre-charged to some low voltage level with an external DC voltage source ($V_{DD} = V_0$). Then the switch disconnects V_{DD} from C_{res} so that the system is considered to be autonomous in terms of power supply, except the

generation of control signals for the flyback switch. Mechanical vibrations are applied to the resonator at the atmospheric pressure. As the mechanical resonator oscillates causing the variation of the transducer capacitance, the charge pump transfers electrical charges from the energized C_{res} capacitor towards C_{store}. During the charge pumping the voltage across C_{store} increases at each variation cycle. After several charge pump cycles V_{store} is eventually reduced by the flyback circuit so to avoid the saturation effect. The flyback is activated by the switch, which is driven by strobe signals *on* and *off* generated in these measurements by an external control logic.

4.5.2.2 Preliminary measurements and results

For the first test C_{res} is pre-charged to 3 V. Applied vibrations are sinusoidal with the frequency 170 Hz and the acceleration amplitude 1.5 g. The frequency of the flyback is 1 Hz, i.e. the flyback switch is activated every second. It is assumed that with this flyback frequency the charge pump does run up to the saturation. Fig. 4.24 illustrates measurement results: the upper plot presents the evolution of the voltages V_{res} and V_{store}, and the bottom - the energy accumulated on C_{res} capacitor. Notice that W_{res} represents the initial energy $W_{res}(3V)$ plus a net energy harvested from vibrations, i.e. it includes all energy losses, which are associated with capacitors and diodes leakage, flyback switch dissipation, and so on, except energy consumed by switch control circuit and voltage followers. It can be observed that the ratio $C_{max}/C_{min} \sim 2$ (according to 2.19) that corresponds to C_{var} measurements (cf. Fig. 4.21). The measurement is done for 5000 seconds in order to measure the net converted energy that has been accumulated in C_{res} and the speed of the energy accumulation, i.e. the power. As V_{res} voltage increases in time, the energy increases proportionally to the voltage square $W_{res} = 0.5 C_{res} V_{res}^2$. But at a certain moment, the slope of V_{res} curve, and consequently W_{res}, decline. This is the result of a shift of the resonance frequency that occurs because of the increased voltage, and hence electric field, of the system and hence electric field, which excites the resonator structure in addition to mechanical vibrations; it becomes lower with the increase of the pre-charge voltage V_{res}. The average power calculated at the interval, where the energy curve slope is maximum (between 3500 and 4000 s) equals 31 nW. Notice that this power corresponds to the vibration frequency 170 Hz, which is slightly outlying from the resonance frequency, and thus the produced power is relatively small. However, this experiment validates that the system setup comprising different blocks is operational.

4.5.2.3 Measurement of the resonance frequencies of the MEMS device

The next experiment allows find the dependence of the resonance frequency on the pre-charge voltage V_{res}. The technique used to do this is as follow. V_{res} is kept constant (by replacing C_{res} by a DC source) and the maximum (saturation) voltage across C_{store} is measured for different excitation frequencies (by sweeping the frequency up and down with a use of the function generator). As a result for each frequency a maximum $V_{store\,max}$ is measured with a voltmeter with high precision. Since V_{res} is constant, the

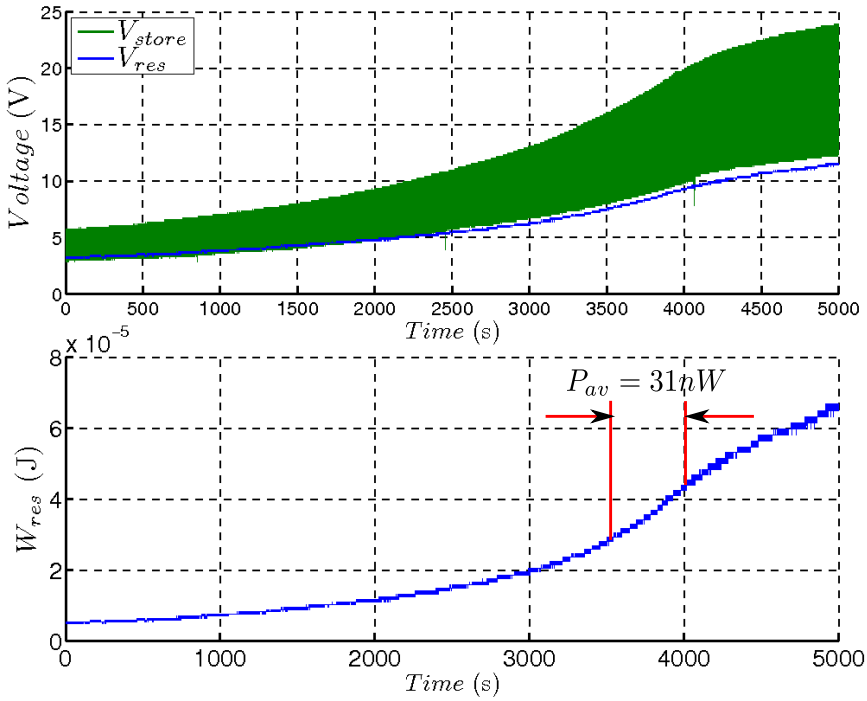


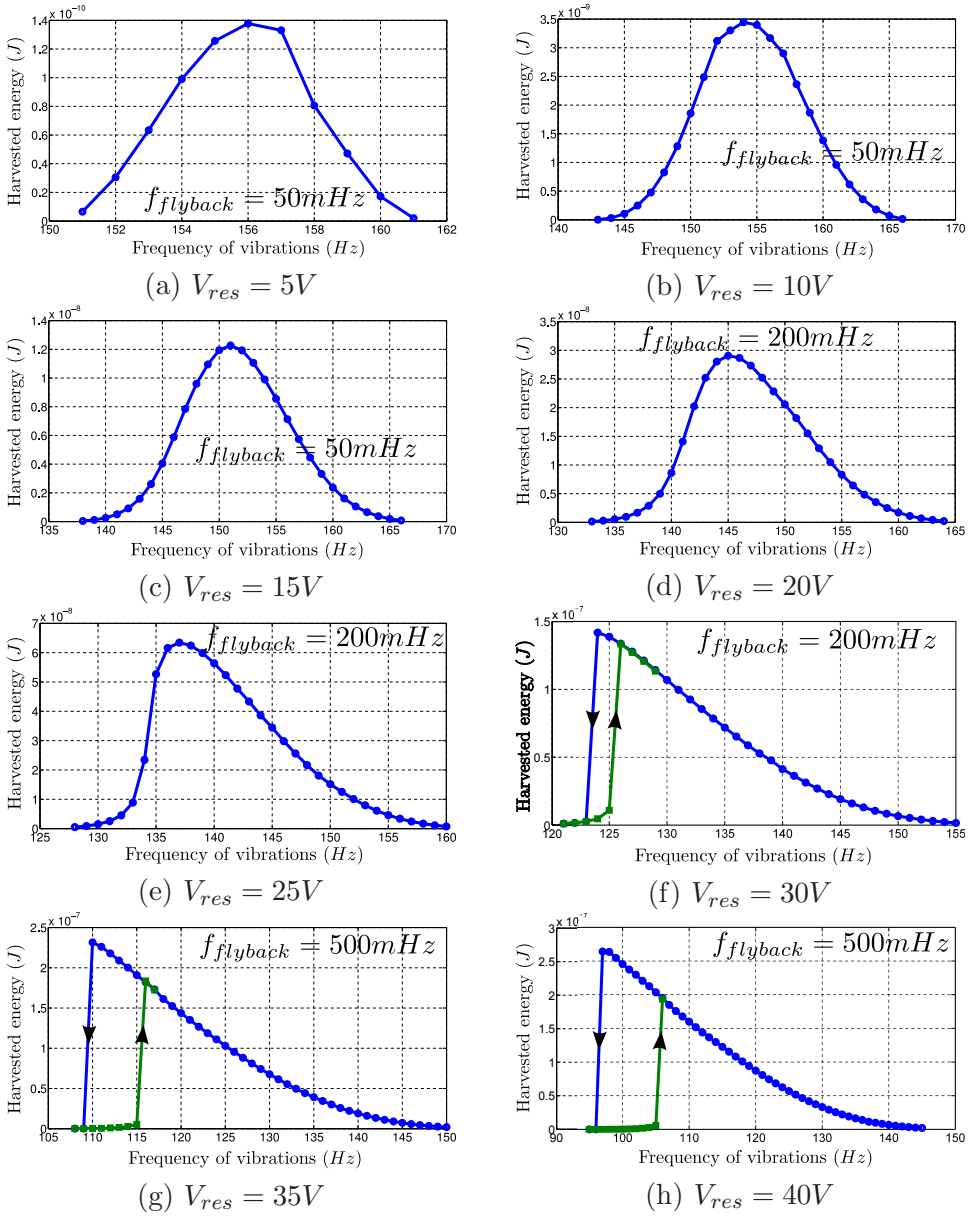
FIGURE 4.24: Evolution of measured voltages V_{res} and V_{store} and of accumulated energy in reservoir capacitor, as the harvester oscillates at the frequency 170 Hz with the acceleration amplitude 1.5 g

difference between $V_{store\,max}$ and V_{res} allows calculate the energy stored in C_{store} according to Eq. 2.39. This experiment is repeated 8 times for different V_{res} voltages ranging from 5 to 40 V, and for the vibration acceleration amplitude 0.3 g.

Fig. 4.25 show the electrical energy accumulated in saturated C_{store} capacitor versus the frequency for frequency sweeping up and down for $0.3g$ base acceleration.

Measurements results shown in Fig. 4.25 are plotted in a form of the energy stored on C_{store} versus the mechanical frequency. For a higher accuracy of measurements the time of the charge pump phase is not the same for the whole voltage range. It is larger for the low V_{res} voltages ($5 - 15$ V), since at acceleration 0.3 g the relation between C_{max} and C_{min} is low ($1 < C_{max}/C_{min} << 2$) and, hence, $V_{store\,\max}$ level is low that causes difficulties of precise measurements. For higher voltages, in turns, $V_{store\,\max}$ measurement causes less problems and hence, the duration of the charge pump operation can be reduced. These results show that as V_{res} increases the peak of energy shifts to a lower frequency. Starting from V_{res}=30 V, the non-linearity phenomena appears leading to an appearance of a hysteresis typical to nonlinear resonators.

Fig. 4.26 shows measurements results for the similar experiment but with vibrations acceleration amplitude 1 g. The energy that is being stored on C_{store} is considerably higher than it was in case of acceleration 0.3 g. The measurement is limited to 25 V, since for higher voltages the "pull-in" effect appears leading to a short circuit between the variable capacitor plates and, consequently, to an instantaneous discharge of C_{res}. The dependence of the resonance frequency on the reservoir capacitor voltage V_{res} when vibrating at 1 g acceleration amplitude is shown in Fig. 4.27.



(a) $V_{res} = 5V$ (b) $V_{res} = 10V$

(c) $V_{res} = 15V$ (d) $V_{res} = 20V$

(e) $V_{res} = 25V$ (f) $V_{res} = 30V$

(g) $V_{res} = 35V$ (h) $V_{res} = 40V$

FIGURE 4.25: Measurement results of the MEMS transducer's resonance frequencies and bandwidths at $0.3g$ acceleration for different initial voltages on the variable capacitor $V_{var\ 0} = V_{res}$:(a) $V_{res} = 5V$, (b) $V_{res} = 10V$, (c) $V_{res} = 15V$, (d) $V_{res} = 20V$, (e) $V_{res} = 25V$, (f) $V_{res} = 30V$, (g) $V_{res} = 35V$, (h) $V_{res} = 40V$.

4.5.2.4 Long-lasting measurements of the energy harvesting with sinusoidal source of vibrations

In order to generate a maximum power at acceleration 1 g within the voltage range of V_{res} 5−25 V, it was decided to fix the frequency of vibrations f_{vibr} corresponding to the average in this range, i.e. corresponding to the resonant frequency of 15 V, which is around 150 Hz. Three similar experiments were made: two of them with f_{vibr}=150 Hz, but with different frequency of the flyback phase f_{fb}, namely 1 and 5 Hz, and the third

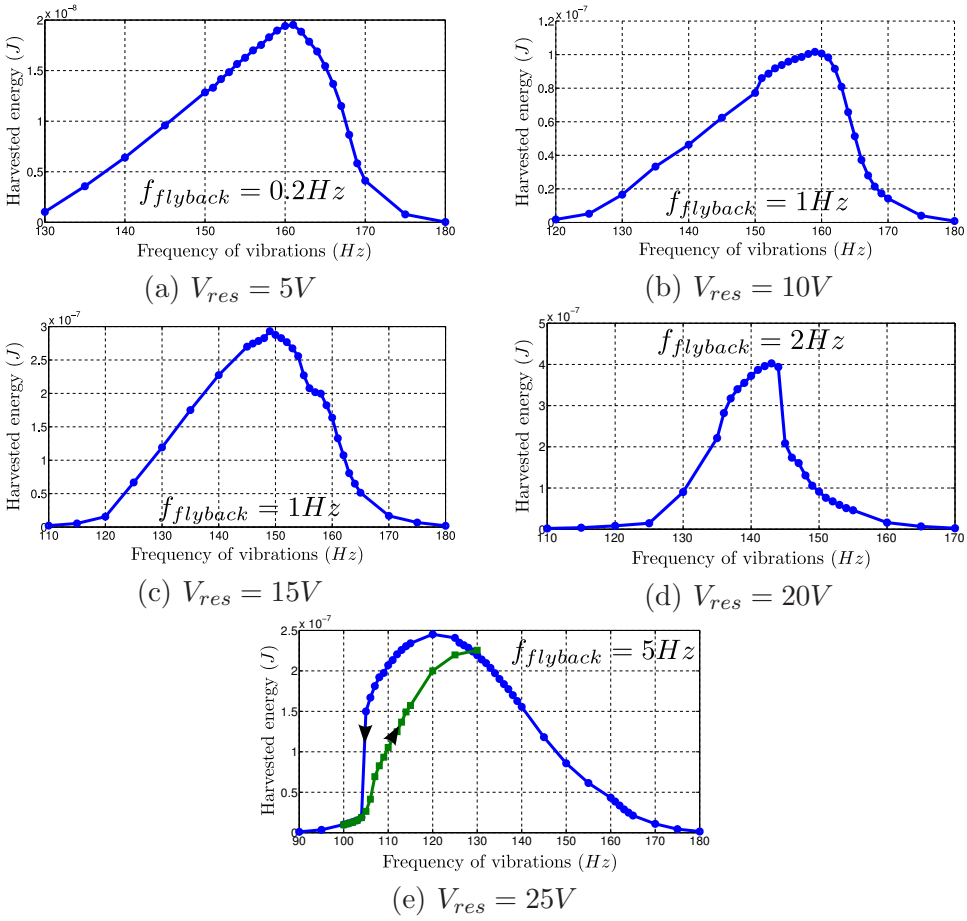


FIGURE 4.26: Measurement results of the MEMS transducer's resonance frequencies and bandwidths at $1g$ acceleration for different initial voltages on the variable capacitor $V_{var\,0} = V_{res}$:(a) $V_{res} = 5V$, (b) $V_{res} = 10V$, (c) $V_{res} = 15V$, (d) $V_{res} = 20V$, (e) $V_{res} = 25V$.

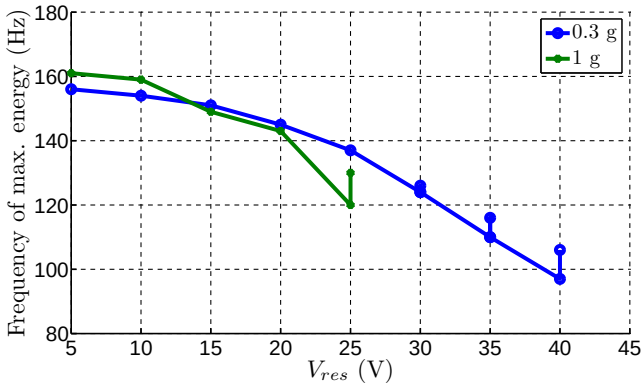


FIGURE 4.27: Dependence of the resonance frequency on pre-charge voltage V_{res}.

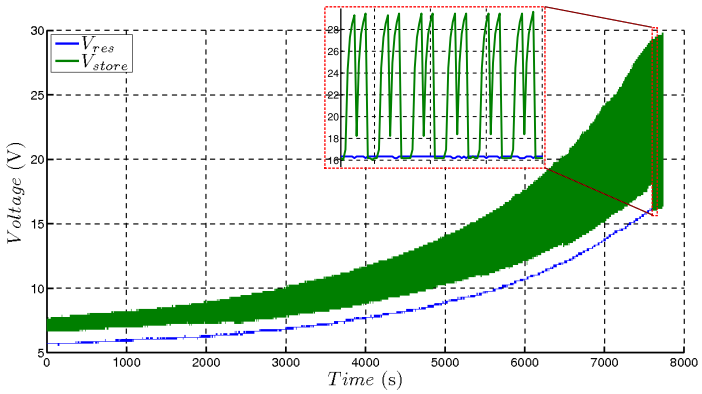


FIGURE 4.28: Evolution of V_{res} and V_{store} as the e-VEH is submitted to mechanical vibrations with 150Hz@1g with a flyback frequency f_{fb}=1Hz.

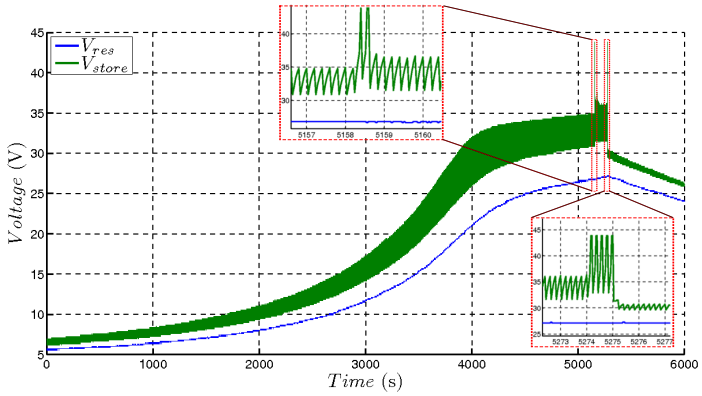


FIGURE 4.29: Evolution of V_{res} and V_{store} as the e-VEH is submitted to mechanical vibrations with 150Hz@1g with a flyback frequency f_{fb}=5Hz.

experiment with f_{vibr}=155 Hz and f_{fb}=5 Hz. All three experiments start with an initial pre-charge of C_{res} to 5 V and aim to test the energy accumulation on C_{res} and to find possible limitations for given system parameters (e.g. pull-in voltage of MEMS, flyback switch limitations, etc.).

V_{res} and V_{store} curves plotted in Fig. 4.28 illustrate the experimental results for a test with f_{vibr}=150 Hz and f_{fb}=1 Hz. This measurement occurs during more than 7000 s. During this time V_{res} increased from 5 to 16.7 V. As can be seen from the Fig. 4.28, starting from the moment t = 7600 s, V_{store}=V_{res} once per two cycles of the charge pump. This situation occurs because the flyback remains activated during the charge pump. The problem consists in the inability of the flyback switch to turn off as a difference between $V_{store\,max}$ and V_{res} is sufficiently high (e.g. $V_{store\,max} - V_{res} > 10$ V) and as it reduces in fast terms (e.g. as upon the flyback phase - $5 - 15$ μs). An explanation is that the level-shifter's internal flip-flop fails to correctly change its state. This issue, however, has not been discovered during the post-layout simulations of the circuit, neither during testing phase of the switch it-self when it has been supplied by a DC high-voltage.

Fig. 4.29 shows the experimental results for a test with f_{vibr}=150 Hz and f_{fb}=5 Hz. It can be see that V_{res} rises from 5 to 27 V in approximately 5300 s. Between 3000

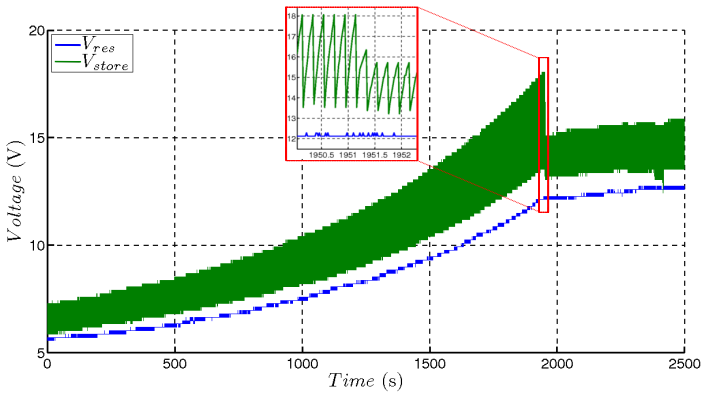


FIGURE 4.30: Evolution of V_{res} and V_{store} as the e-VEH is submitted to mechanical vibrations with 155Hz@1g with a flyback frequency f_{fb}=5Hz.

and 4000 s, the e-VEH has a frequency around resonance, and further the frequency shifts causing the V_{res} slop to decrease. When reaching 27 V, several spikes of V_{store} appear. This happens as the resonator's movable plate touches the stoppers. Hence the capacitance drastically increases, causing the eventual rise of V_{store}. In this plot it is shown that V_{store} reaches 44 V, however this level is limited by the voltage supply of the voltage followers, in reality, V_{store} can increases much higher, since the ratio C_{max}/C_{min} during the contact with mechanical stoppers can be > 10. It can be observed on a zoom at the bottom of figure that starting from $t = 5275$ s, the magnitude of V_{store} is drastically reduced, so that the produced power by the charge pump becomes less than the flyback circuit consumes. C_{res} capacitor starts to loose the accumulated energy as can be seen by the decreasing voltage curve V_{res}. That is a result of a sudden shift of the resonance frequency far from 150 Hz due to the increase voltage that is typical for a non-linear resonator. Fig. 4.30 shows the experimental results for a test with f_{vibr}=155 Hz and f_{fb}=5 Hz. These plots show that V_{res} rises 13 V faster than in previous tests (i.e. in approximately 2000 s). Obviously, this happens because the capacitance starts to oscillate at resonance frequency earlier than in previous cases. However, as V_{res} reaches 13 V, the resonance is suddenly shifted. As can be seen, $V_{store\,max}$ level dropped down and, consequently, V_{res} voltage slop is decreased.

A comparison of the accumulated energy for three experiments is shown in Fig. 4.31. The maximum energy and power is produced during the second experiment, as the flyback is activated 5 times per second and mechanical excitation occurs with a frequency 150 Hz. At regions that correspond to the maximum slop of the energy curves, the average power is calculated. The maximum average power 232 nW is produced at 150Hz@1g with a flyback frequency 5 Hz, and it corresponds to V_{res} rising from 16 to 22 V. This voltage range lies in the pass-band slightly lower than the resonance frequency according to Fig. 4.26. Comparing the energy curves corresponding to tests with f_{vibr} 150 Hz and 155 Hz, it can be observed that the one with 155 Hz rises faster in the beginning, since the resonator oscillates at resonance frequency at lower voltages (approximately between 9 and 13 V). Comparing the energy curves corresponding to tests with f_{fb} 1 Hz and 5 Hz, the one with 5 Hz allows the system accumulate more energy for the same period than with 1 Hz. This is because the flyback phase being activated with a 5-Hz frequency, unlike the case with f_{fb}=1 Hz, prevents the saturation effect of V_{store} and, therefore, the

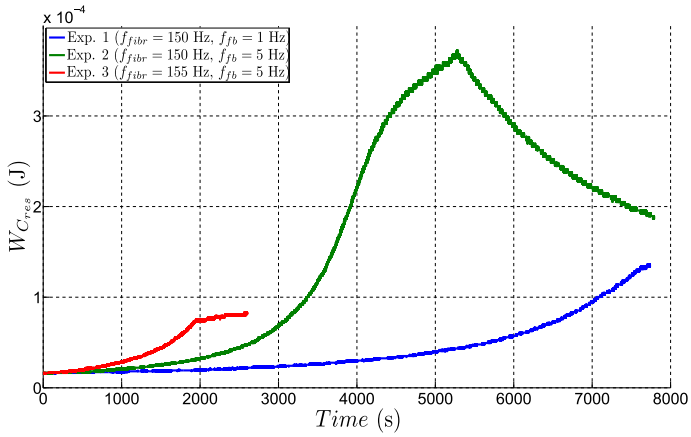


FIGURE 4.31: Evolution of energy corresponding to 3 similar experiments with following setup parameters: (a) f_{vibr}=150 Hz and f_{fb}=1 Hz, (b) f_{vibr}=150 Hz and f_{fb}=5 Hz, (c) f_{vibr}=155 Hz and f_{fb}=5 Hz. Acceleration amplitude for all tests is 1 g.

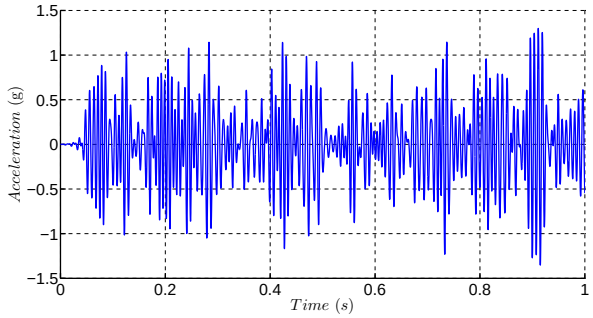


FIGURE 4.32: Exponentially correlated Gaussian noise signal of a 1-second duration comprising frequencies in $100 - 180$ Hz bandwidth.

power is continuously generated (cf. Fig. 2.8). Greater increase of the flyback frequency nevertheless leads to increase of the energy losses as well, since in that case V_{store} may not reach the optimal upper level V_2 (cf. Fig. 2.8). Moreover, higher frequency of the flyback activation is related to higher energy dissipation by the switch, inductor, diodes and so on.

4.5.2.5 Long-lasting measurements of the energy harvesting with a Gaussian noise as source of vibrations

The following experiments aim to test the system subjected to vibrations in a form of an exponentially correlated Gaussian noise, which covers a spectrum of all frequencies that we are interesting in, instead of applying a harmonic sinusoidal signal of only one frequency. By doing so, we expect to provide resonant frequency components for the whole voltage range, and hence to extract a greater power. To this end, we generate an exponentially correlated noise with auto-correlation. The algorithm generates a sequence of random numbers with the following two properties: each number is a Gaussian deviate with zero mean and unit variance; the auto-correlation function of the sequence decays exponentially with a predefined decay time. The generated noise is a 1-second sequence

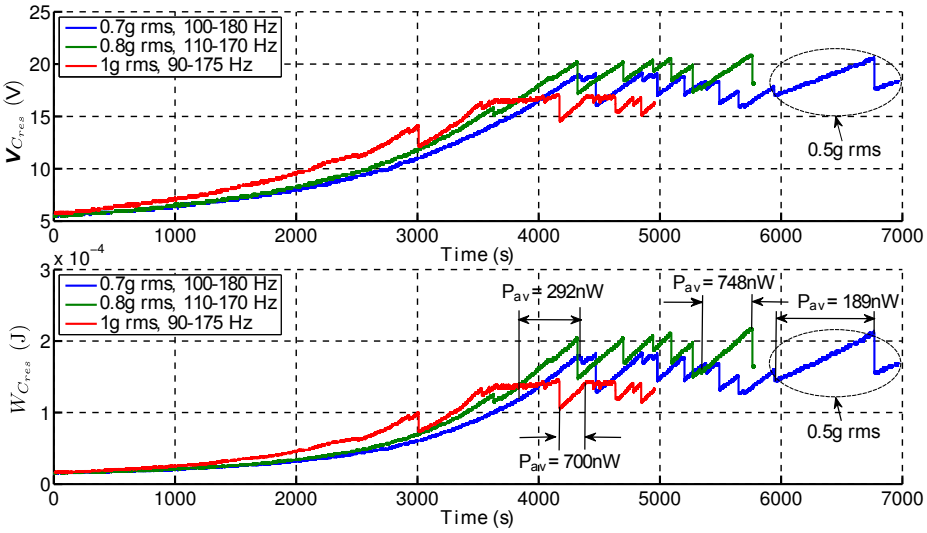


FIGURE 4.33: Evolution of V_{res} and W_{res} curves as the e-VEH is exposed to mechanical vibrations occurring in a form of exponentially correlated Gaussian noise.

of numbers comprising a spectrum of frequencies from 0 to 200 Hz. However, very low-frequency excitations generated by the shaker provide a high displacement amplitude of the vibrating table that may eventually damage the MEMS device - if high acceleration spikes of the noise are applied; moreover, the resonator does not response to very low frequencies. Thus, we cut off unwanted frequencies by applying a pass-band filter. As a result, we obtain three noise signals of 1-second duration with minor differences in the bandwidth: 100−180 Hz, 110−170 Hz, and 90−175 Hz. During the measurements these signals are repeated periodically. An example of the generated noise within a bandwidth 100-180 Hz is illustrated in Fig. 4.32.

Fig. 4.33 presents measurements results for three experiments with 100−180 Hz, 110−170 Hz and 90−175 Hz vibrations noise bandwidths, and with rms values of accelerations 0.7 g, 0.8 g and 1 g, respectively. Each measurement starts with a pre-charge of C_{res} with 5.5 V and occurs with the flyback frequency 5 Hz. A pull-in effect can be observed on the plots, which occurs as V_{res} reaches a certain level (pull-in voltage). Due to a strong electrostatic force variable capacitors plates are stuck together, consequently producing a short circuit. As a result, C_{res} discharges very fast through the diode D_1 until the voltage, at which the pull-in effect disappears. For different acceleration amplitudes the pull-in voltage is different as well: the lower is the acceleration amplitude, the lower are voltage peaks across C_{var}, consequently, the higher pull-in voltage can be achieved. However, that is not obvious at given measurements results, since the frequencies bandwidth for each test is slightly different. Nevertheless, looking at a blue voltage curve (with the following vibrations: 100-180 Hz at 0.7g rms), it can be observed that starting from the time 5900 s, the acceleration amplitude is manually decreased to 0.5 g rms, consequently the pull-in voltage increases approximately from 19 V to 21 V. Illustrated plots show the following relation as well: lower is a frequency in the frequency range of the noise, the lower is a pull-in voltage. Indeed, at lower excitation frequency the greater is the vibrating table displacement and, hence, a mechanical stress. Regarding the accumulated energy and power, these figures are considerably greater than in a case of a single frequency. The average power calculated on the time interval, where

a slope of the energy curve is maximum, is as follow: 189nW@0.5g rms, 292nW@0.7g rms, 748nW@0.8g rms and 700nW@1g rms. Power generated at the experience with the acceleration 1g is less than at the one with 0.8g because the noise at the last experience includes the frequencies from a more narrow band (110−170 Hz), within which the noise spectral density of vibrations is higher.

These results have been presented in PowerMEMS'2013 conference [Dudka13a].

4.5.2.6 Flyback circuit efficiency

Finally, we determine the flyback phase efficiency during the typical operation of the harvester. Recall that the flyback operation consists of two phases: 1) switch is on and the freewheeling diode D_{fly} is off, C_{store} discharges from V_2 to V_1 energizing the inductor; 2) switch is off, diode is on, which de-energizes the inductor. During both phases C_{res} receive the energy, i.e. since C_{res} accumulates electrical charges V_{res} increases. However, the switch, the inductor and the diode dissipate a part of the energy to be transferred from C_{store} to C_{res}.

Using the calculation methodology provided in subsection 3.6.5.3 and data from measurements shown in Fig.4.34, an example of the efficiency of a typical flyback phase is found. Illustrated plots present several cycles of the charge pump and flyback operation: the upper plot show the evolution of V_{store} between 20.7 and 24.4 V; the bottom plot show the AC component of V_{res} in order to measure precisely the rise of V_{res} during the flyback. As can be observe it is about 0.0125 V. A DC voltage component of V_{res} is 20 V. Considering these values, the transferred energy per a flyback cycle is 275 nJ, the dissipated energy is 25 nJ, consequently the flyback efficiency is 90.8 %. The determined efficiency differs from that one obtained in simulations in subsection 3.6.5.3 that equals 84.7 %. The discrepancy is explained by the different experiments conditions and parameters, as well as by accuracy of the data; the later is more precise in simulations. Nevertheless, the measured and simulated efficiency of the flyback circuit is similar to that of typical Buck DC-DC converters that is 80-90%, according to [Sun08].

4.6 Summary

This chapter presented an experimental part of our research work. The first part of the chapter was devoted to the characterization of our fabricated high-voltage switch intended specifically for application in the flyback circuit. The second part discussed the testing of the MEMS capacitive VEH within the conditioning circuit composed of the charge pump and the flyback.

Concerning the first part, as measurements show the designed level shifter and switch satisfy the specifications, mainly, regarding the ultra low power consumption in conductive and stand-by mode, a high-voltage capability, a large current range and a high activation speed. The detailed measured characteristics are summarized in Table 4.1.

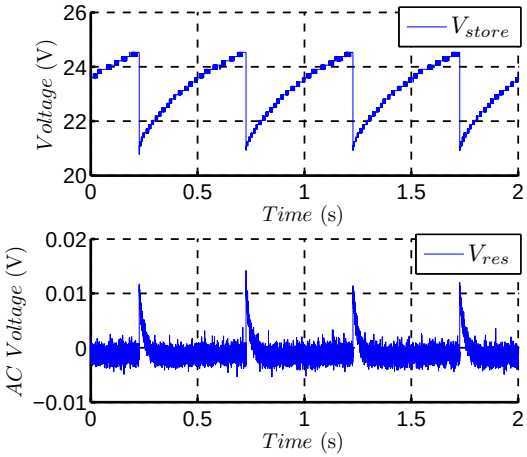


FIGURE 4.34: Demonstration of the VEH's circuit main voltages: V_{store} curve at the upper plot and a corresponding AC component of V_{res} at the bottom.

TABLE 4.1: Level shifter and switch measured characteristics.

Characteristic	**Min**	**Typ**	**Max**
Voltage range	$4V$	–	$31V$
Switch ON-resistance	32Ω	38Ω	46Ω
LS leakage current	0.26 nA @ 3 V	–	1.45 nA @ 31 V
LS static power consumption	0.8 nW @ 3 V	–	44.8 nW @ 31 V
Dynamic energy loss per one level shifting	$65pJ@5V$	–	$1.38nJ@31V$
Level shifting speed:			
$V_{ON/OFF} = 2.5V$	$103ns$	$107ns$	$137ns$
$V_{ON/OFF} = 3V$	$67ns$	$73ns$	$124ns$
$V_{ON/OFF} = 3.5V$	$47ns$	$54ns$	$119ns$
Max. on-state holding time:			
$V_{DDH} = 5V$	–	–	$3.4s$
$V_{DDH} = 10V$	–	–	$4.6s$
$V_{DDH} = 15V$	–	–	$5.7s$
$V_{DDH} = 20V$	–	–	$5.8s$
$V_{DDH} = 25V$	–	–	$5.6s$
$V_{DDH} = 30V$	–	–	$4.3s$
V_{DDH} versus V_{DD}	$4V@V_{ON} = 3.6V$	–	$10V@V_{ON} = 2.1V$
Measured switching current	$60\mu A$	–	$40mA$

Concerning the second part, the main goals of measurements have been achieved. We characterized the fabricated electrostatic harvester in the charge pump and flyback circuit topology. We pre-charged the reservoir capacitor at 5 V supplying the harvester with initial energy and let the system harvest the energy from the vibrations in an autonomous mode (no voltage source has supplied the system, instead the low voltage source supplying the control logic for the flyback switch). After letting the system operate a few hours, the voltage across the reservoir capacitor rises up to 25 V, thus accumulating the harvested energy. We achieved a power generation within 31 nW and 748 nW, depending on a source and nature of the mechanical vibrations, as well as of the voltage across the transducer. Thus, for example, we achieved an average power conversion of 232 nW from the mechanical vibrations at 150 Hz and amplitude of 1 g, flyback commutation frequency of 5 Hz and the voltage range pre-charging the transducer in between 16 and 22 V. Another example gives an average power generation of 748 nW from vibrations in a form of exponentially correlated Gaussian noise (increasing the bandwidth of vibrations) of an amplitude 0.8 g rms, flyback frequency 5 Hz, and pre-charging voltages between 17.5 and 21 V. All these power values is in fact a net power generated by the e-VEH, comprising the losses across the flyback switch, capacitors, inductor, diodes, and so on, excepting the power supplying the control logic driving the flyback switch. Additionally, we calculated the efficiency of a typical flyback operation that draws 90.8%.

We discovered as well several limitations related to the switch and the global system. Concerning the switch, if it must be turned on at a high voltage supply and turned off at a considerably lower voltage, which is a case for the flyback circuit application, the switch can fail to turn off. Unfortunately, this issue has not been discovered in modeling of the level shifter, and it is related to incapability of the level shifter to generate correctly the output level if the high voltage supply drastically changes. The functioning of the energy harvester is limited by a narrow bandwidth, which in turn varies non-linearly in response to the voltage applied to a transducer capacitor. Another limitation relates to the pull-in voltage, which limits the maximum voltage that can be applied between the variable capacitor plates, and which occurs at different voltages according to the acceleration of the mechanical vibrations.

It is worth to notice that presented results of measurements don't comprise the power consumed in the control circuitry (flyback switch is driven by externally generated strobe signals). This is mainly due to the fact that the discrete level realization provided is not the optimum solution regarding the limitation of available components, and it is used mainly to prove our theoretical findings. A custom integrated circuit that drives the flyback switch following the auto-calibration algorithm with minimized power consumption is a subject of our future work.

Chapter 5

Summary, conclusions and perspectives

This chapter summarizes all chapters of the manuscript highlighting our major contributions, provides a general conclusion of the work, and finally discusses the possible future work.

5.1 Chapter summaries

Chapter 1

The first chapter introduced the concept of energy harvesting of ambient energy sources that can be used to supply the low-power microscale autonomous electronic devices in the hard-to-reach environments or the implantable applications.

Today, among the most usable energy sources for the harvesting in the mentioned environments are solar, RF, vibrations and heat energy. This study is focused on vibration energy harvesting (VEH), which is typically achieved using piezoelectric, electromagnetic and electrostatic transducers, or sometimes combinations of them. With the development of MEMS technologies, the use of variable capacitors to convert the kinetic energy of vibrations (electrostatic transducers) has became very attractive, since the MEMS device can be integrated on a single silicon area with the assisting electronics. For this reason, this work deals with the capacitive energy harvester that typically consists of a resonator/transducer device, an electronic conditioning and power management circuit, and a storage element (rechargeable battery) ensuring the regulated output voltage for the load.

A number of studies have been done on capacitive transducers since the early 2000's, e.g. [Roundy03a, Miao06, Paracha09b, Hoffmann09, Naruse09], also a lot of industrial investigations in accumulator developments have been made (e.g. Li-Ion, ultracapacitors, etc.). The power interface circuits, however, received less attention from the community, especially at the moment of the beginning of this thesis in 2009.

The chapter also presented the existing conditioning circuits for the capacitive VEH, such as the charge constrained [Meninger01] and voltage constrained [Torres06] circuits, the charge pump [Roundy02] with resistive [Florentino11] and inductive flyback [Yen06] energy return. The circuit of [Yen06] has been chosen as a base of our research, since it has several advantages that makes the architecture very attractive in future real realizations: it is potentially the least power consuming since it does not require a precise high-frequency control unit, also it allows a high-voltage biasing of the transducer providing a high level of the generated electrical power. The reported circuit by Yen, however, has not been fully analyzed and optimized, the issue of adaptation to the ambient environments has not been addressed, and finally it was not autonomous, since the switch was driven externally. Hence, this dissertation aims to deeper analyze and optimize the Yen's conditioning circuit, and to propose the integrated circuit of the control unit of the harvester following the optimum and adaptive algorithms.

Chapter 2

This chapter presented the theoretical foundations, modeling and optimization of the capacitive energy harvester which employs the charge pump&flyback conditioning circuit [Yen06].

The detailed operation principle and theoretical investigations of the charge pump circuit have been provided. The analysis showed that there exist a unique voltage level of a storage capacitor corresponding to the peak of the generated electrical power. The flyback return circuit has been presented in details. It was concluded that the frequency of the flyback activation plays a key role in the energy yield of the VEH system. Indeed, to maintain the charge pump voltage at a level corresponding to the maximum power conversion, the flyback must be activated at every charge pump cycle. The frequent activation of the flyback, however, is not optimum, since it is related to the non-negligible energy losses in switch, inductor and diode. A trade off was proposed that consists in choosing the optimal zone for the charge pump operation, rather than a unique voltage level. As a result, the frequency of the flyback activation considerably decreased, while the average converted power is only slightly below the peak value. To determine the optimal zone dynamically taking into account the possible variations of the vibration parameters, it was proposed to calibrate the system from time to time. The developed optimum auto-calibration technique was modeled using VHDL-AMS, allowing thus a simulation of the control unit of the switch activating the flyback circuit.

It is desired that the electrostatic VEH circuits operate at high voltages in order to maximize the converted power; at the same time the load such as low power sensors must be powered by low dc voltages. To interface the energy harvesting circuit with a load, the architecture of the dual-input dual output BUCK DC-DC converter was proposed, which reuses the existing inductor and diode in the flyback path.

Finally, to validate this study, the whole system was modeled on a system-level using Spice and VHDL-AMS, and simulated using the mixed-signal AdvanceMS environment. The MEMS resonator/transducer was modeled using VHDL-AMS according to parameters of the real devices fabricated in ESIEE Paris by our project collaborators, particularly P. Basset.

Chapter 3

This chapter stated on the circuit-level design of the electrical part of the harvester and implementation on the chip of a key element - the high-voltage switch with a novel driver.

One of the main objectives of this thesis was the investigation and development of the integrated circuit of the control unit of the conditioning circuit following the developed in Chapter 2 auto-calibration algorithm. The used CMOS technology (AMS035HV) for the design was chosen according to the high-voltage circuit specifications and availability of this one in our research lab. Relying on the fundamental challenge of the harvesters in creation of a net energy gain, the design of the conditioning electronics should fulfill the following requirement: the power consumption of the energy harvesting circuit must not exceed the harvested power, which is often in the order of only a few microwatts.

A special attention has been devoted to the design of the level shifter/driver for the high-side flyback switch, since the existing commercial and reported in literature solutions have not or partly satisfied our needs in ultra-low power, robust, fast and simple architecture. Our design is inspired of a dynamic level shifter based on analog flip-flop topology reported in the thesis of P. Basset [Basset03]. The conventional architecture was improved by adding of the intermediate switches which allow better levels of the shifted signal and, hence, a more robust and efficient commutation of the high-side switch. The designed circuit consumes 2 mA current during only a very short time of triggering of the flip-flop to a new state, typically several tens of nanoseconds, while the rest of time the circuit draws only the leakage picoamper current from the high voltage source. When employed in the flyback circuit, the efficiency of the energy transfer was up to 85 % according to simulations. The circuit was successfully fabricated and tested.

The controller of the switch was designed using the high/low-voltage transistors of the same CMOS process. The primary goal of the controller is to generate the switching events (strobe pulses) to drive the level shifter and consequently the high-side switch so that the charge pump operates in the optimal voltage zone. This optimal zone is periodically calibrated. The controller IC includes the signal processing blocks and interface blocks between the high-voltage charge pump and the low-voltage logic. The design was carried out with the emphasis on low power consumption that was achieved by using several approaches: programmable low frequency clock in the same order as the frequency of vibrations (50-300 Hz), reduced voltage supply for bias current and clock generators (1.1 V), using of zero static power architectures (e.g. level shifter), use of extra-large external resistors (100 MΩ - 10 GΩ) for voltage dividers, relatively small gate drivers, etc. The total average power consumption of the control unit and switch driver can vary between several hundreds of nanowatts and a few microwatts depending on many factors, e.g. parameters of vibrations, voltage levels of the charge pump, frequency of calibration and flyback, etc. A 50s-simulation example revealed the average power consumption of 0.85 μW, while the average converted power was 1.25 μW including the losses in the conditioning circuit (diodes and inductor). These results were obtained with the following electrical and mechanical parameters: C_{res}=1 μF, C_{store}=3.3 nF, L_{fly}=15 mH (R_C=360 KΩ, R_W=16 Ω), V_{res}=10→15 V, C_{max}/C_{min}=1.6, f_{ext}=298 Hz, A_{ext}=1 g.

Chapter 4

This chapter discussed the measurements of a fabricated switch/driver prototype and characterization of the MEMS capacitive harvester employed in Yen's conditioning circuit. The measurements setup for the tests use a breadboard offering the flexibility of manipulation with a set of discrete components. The voltage range for the tests was between 3 and 31 V.

First, the fabricated switch/driver was tested alone in order to explore its characteristics. The measured on-resistance of the high-side CMOS switch is 38±8 Ω. The leakage current of the switch/driver is between 0.26nA@3V and 1.45nA@31V. The dynamic energy dissipation (per a level shift) is between 65pJ@5V and 1.38nJ@31V. The typical level shifting speed is between 54ns (driven by the input signal 3.5V) and 107ns (driven by the input signal 2.5V). The maximum duration of maintaining the on-state by the internal capacitances without refreshing is between 3.4s and 5.8s, that is 5 order longer than the flyback phase actually needs.

After the switch has been tested, it was employed in the charge pump and flyback conditioning circuit mounted on discrete components with a goal to characterize the whole VEH system on a wide voltage range. The MEMS transducer/resonator device employed in the experiment was fabricated and fully characterized in ESIEE Paris [Guillemet13]. The resonance frequency of the resonator is 162 Hz. In large amplitude mode (1g of external vibration acceleration), it has a half-power bandwidth of more than 30 % of the central frequency. The transducer capacitance varies between 45 pF and 74 pF.

C_{res} was pre-charged to 5 V with an external energy source. When this source was disconnected from C_{res}, the VEH system became electrically autonomous, with the exception of the energy source for the external control logic driving the switch. A set of tests has been done with the similar electrical setup to test the accumulation speed (power) of the converted energy and the voltage limits (pull-in effect) of the MEMS structure. The mechanical resonator was submitted to harmonic vibrations with a fixed frequencies close to the resonance (162 Hz) and the stochastic vibrations, whose energy was distributed in the frequency band (100-180) Hz. the interesting results were obtained with the stochastic vibrations. Initially biased to 5.5 V with 15 μJ, the system increased its voltage up to 21.5 V with the accumulated energy 230 μJ. The maximal measured *net* power was 748 nW without considering the power consumption of the switch events generator, which must be replaced by the dedicated flyback switch controller in future works.

5.2 Conclusions

The research on vibration energy harvesting is a wide field of studies, regrouping the specialists from different domains: physicians, technologists, mathematicians and electronics engineers, who must tightly collaborate with each others. Research investigations are carried out in several directions: mechanical structures, conditioning circuit interfaces, storage elements, power management. The modern vision of the vibration energy harvesters is as follow: the mechanical resonators must have the non-linear properties

to enlarge the bandwidth and the electronic circuits must be intelligent and adaptive. These requirements tend to match the realistic applications, where the vibration parameters are unknown *a priori*, varying in time and unpredictable.

This work was focused on the study of conditioning circuits for the capacitive transducers. Our research contributed to the investigation of the intelligent and adaptive circuit based on the charge pump and flyback. The key words of this thesis are the "optimization" and "adaptation". The proposed technique of auto-calibration allow the optimum harvester functioning under conditions of the fluctuations in the environment (e.g. variable acceleration amplitude), as has been observed thanks to the behavior modeling and simulations results. To our knowledge, such an adaptive behavior of the capacitive harvester has never been published before and, hence, evoked the interest of the community [Dudka09b].

To further investigate our research, we designed the integrated circuit of the control unit [Dudka12], which implements the auto-calibration algorithm. The proposed circuit uses the fully analog signal processing and power management, so to minimize the circuit complexity and power consumption, which was the critical parameter to be handled during the design. The circuit design in AMS035HV technology was validated by simulations and layouts of several blocks. Unfortunately, the proposed controller was not realized on chip due to several difficulties encountered during the design stage, such as many trade-offs between the power consumption, high-voltage level of operation and the accuracy. So, this stage took a longer time than it was initially expected. Nevertheless, the layouts of several blocks were done and the most important block that can be tested individually (a novel high-voltage switch/driver) has been implemented, fabricated and tested. Moreover, together with the switch we implemented on the same chip a sample and hold circuit (the part of the controller), which consists of the large capacitors (422 pF), switches and interface with the external resistors. However, we did not test this circuit due to the lack of time, but it can be tested in close future works.

The tests results of the switch have a good matching with simulations. It has been observed a very low power operation of the level shifter. The high-side power switch, however, has a relatively high on-resistance which could be reduced at the expense of the channel width of the MOSFET device.

An excellent compatibility of the studied circuit with stochastic wide frequency band input vibrations, demonstrated by the experiment, is one of the most important practical result of this work. The synchronous circuits, such as voltage constrained and charge constrained, can only efficiently work with regular input vibrations. Indeed, their operation is based on active local maximum/minimum detection of the transducer capacitance. When the input vibrations are wideband, numerous false max/min detections will occur: this will consume the energy of the active control circuits, and will reduce the overall circuit efficiency. In the charge pump based circuit, the direction of the transducer capacitance evolution is done passively by the diodes, so this circuit operates well with noisy vibrations.

5.3 Perspectives

This thesis work has addressed various problematic aspects of the power interface harvesting circuits, however, still many problems remain unsolved in our study, in particular, and in the state of the art harvesters, in general. In this section, we list some of the possible improvements that can be done in the future. This list is arranged by the priorities order.

Realization of the adaptive flyback switch controller on-chip
This is obviously our main priority, since the proposed circuit is already designed and has been simulated, showing the very promising results. The fabrication of the switch controller will be a major step toward the smart and autonomous operation of the capacitive harvesters. Several improvements of the proposed controller and switch, however, can be done. As we already mentioned, the flyback power CMOS switch has a relatively high on resistance (38 Ω). To decrease it, two modifications can be done. First, it is possible to increase significantly the width of the device, e.g. integrated in 0.6μm XT06 CMOS technology power switches measured up to 40000μm/3μm and the measured on resistance was <5 Ω [Szollosy10]. Secondly, the gate voltage of the switch can be slightly increased by slight redesigning of the level shifter. The gate voltage of the fabricated switch is 2.8 V, however it can be increased up to 3 V. Another improvement that can be done, is to replace the external extra-large resistive voltage dividers by the CMOS dividers, despite of the large silicon die area that will be eventually occupied.

On-chip supply from the converted energy
This point concerns the design of a stabilized voltage supply to power the controller itself with a part of the converted energy. This is a complex task, which requires the improvements in both electrical and mechanical parts of the harvester in order to deliver enough converted energy to the conditioning circuit and the load. This can be done, for example, by an additional DC-DC conversion stage, which will act in alternating phases with a flyback. The successful realization of this mechanism, will result in a fully-autonomous adaptive energy harvesting system, as has been recently presented in [Gasnier13].

Power management
To successfully interface the energy harvesting circuit with a real-life load, several aspects must be considered. Most importantly, if the energy accumulated in the reservoir capacitor C_{res} is not high enough to supply the load and the energy harvesting circuit at once, hence the load must be disconnected from the energy source. Otherwise, the load will draw the power until it completely depletes C_{res} causing the energy harvesting circuit to fail. If the load is a rechargeable battery, the load interface unit of the harvester must disconnect the load when the reservoir voltage reaches some critical value. Or, if the load is a smart microsystem or device, it should understand that power delivery cannot be guaranteed at all times and it should decrease its power consumption in case of low energy available. We proposed an architecture of the power management block interfacing the load, based on dual-output dual input DC-DC converter operating following a simple algorithm. This power management block was validated by simulations on a system level [Dudka09a]. The next step will be the investigation on two aspects: propose a more sophisticated and optimal algorithms according to the realistic loads and implement the proposed architecture on a circuit level.

Start-up mechanism

If eventually the energy reservoir C_{res} is empty and subsequently the energy harvesting fails, a start-up mechanism providing an initial energy to the reservoir must be necessarily employed, when used in real applications. One of the possible solution is to use the electret-based electrostatic converters which have the electret layers on one (or two) plate(s) of the variable capacitor, polarizing it. Electrets are dielectric materials that are considered as electrostatic dipoles, equivalent to permanent magnets (but in electrostatic) that can keep charges for a long period. Another solution consists in using piezoelectric harvesters with piezoelectric start-up generator [Florentino11]. This solution is feasible when the electrostatic harvester is a part of a multi-energy source generator [Christmann12], as is in the case of the project ANR SESAM at which we participated. The goal of this project was to merge the photovoltaic energy (solar), electromagnetic (RF), motion (vibrations and deformations) and thermoelectric (heat). In the case of multi-source energy generators, the task is easier and the start-up voltage for the capacitive harvester can be used from all this sources.

Replacement of external diodes by their low-threshold voltage CMOS counterparts

This can be done to decrease the voltage and subsequently energy losses during the charge pumping and the flyback phases. The diode can be replaced by a novel dedicated circuit [Le06] which acts as a very low voltage drop diode. Initially, this technique was developed for the piezoelectric energy harvesters in order to efficiently rectify the AC voltage by the passive full-wave rectifier.

Appendix A

VHDL-AMS models of two MEMS structures

Model of the In-Plane Overlap Plates structure developed in ESIEE Paris in 2008

```
LIBRARY DISCIPLINES;
USE DISCIPLINES.ELECTROMAGNETIC_SYSTEM.ALL;
library IEEE;
use IEEE.MATH_REAL.all;

ENTITY harvesting_resonator_adms_vhdlams_ESYCOM IS
    GENERIC(
        Q0:real:=1000.0e-12; --initial charge, Q0=5V*200pF
        x_init:real:=0.0 --initial mass position
        );
    PORT (
        TERMINAL pos        : Electrical ;
        TERMINAL power      : Electrical ;
        TERMINAL force      : Electrical ;
        TERMINAL e2         : Electrical ;
        TERMINAL e1         : Electrical ;
        TERMINAL capvar     : Electrical ;
        TERMINAL capcharge  : Electrical ;
        TERMINAL Fstop      : Electrical ;
        TERMINAL accel      : Electrical
    );
END;

ARCHITECTURE adms_vhdlams_ESYCOM OF harvesting_resonator_adms_vhdlams_ESYCOM IS
--***********************************
function capa_generic_one_period (x:real) return real is
constant ampl:real:=1.0;
constant Cmax:real:=1.0;
constant Cmin:real:=0.0;
variable d_bord:real:=0.1*ampl;
variable dc_dx:real;
variable a:real;
variable capa:real;

begin
dc_dx:=(Cmax-Cmin)/(ampl-d_bord);
a:=dc_dx/(2.0*d_bord);
if abs(x)<d_bord then
    capa:=a*x*x+Cmin;
elsif abs(ampl-abs(x))<d_bord then
    capa:=-a*(abs(x)-ampl)*(abs(x)-ampl)+Cmax;
else
    capa:=dc_dx*(abs(x)-d_bord)+a*d_bord*d_bord+Cmin;
```

```
end if;
return capa;
end;

--************************************
function capa_generic(x:real; x0:real) return real is
constant ampl:real:=1.0;
variable capa:real;

begin
capa:=capa_generic_one_period((abs(x+x0+ampl) mod 2.0*ampl)-ampl);
return capa;
end;

--************************************
function capa(x:real) return real is
constant ampl:real:=50.0e-6;
constant Cmax:real:=144.0e-12;
constant Cmin:real:=73.0e-12;
variable x0:real:=ampl;
variable capa:real;

begin
capa:=capa_generic(x/ampl, x0/ampl)*(Cmax-Cmin)+Cmin;
return capa;
end;

--************************************
function dc_dx(x:real) return real is
variable dc_dx:real;
begin
dc_dx:=(capa(x+1.0e-8)-capa(x))/1.0e-8;
return dc_dx;
end;

--************************************
constant m: real:=46.0e-6;
CONSTANT k: real:=152.6; --f0=290 Hz
CONSTANT k_stopper: real:=0.0;
CONSTANT kv:real:=2.185e-3;-- for Q=30
CONSTANT mu_stopper:real:=1.0;
CONSTANT xmax:real:=50.0e-6;
CONSTANT delta_t:time:=200.0 ms;
CONSTANT dt:time:=1.0 ms;
--************************
constant kk: real:=4.0e3;
constant VV: real:=0.0021;
--************************
signal clk: bit:='1';
signal p:real:=0.0;
signal tmp:real:=0.0;

quantity vitesse : real:=0.0;
quantity charge : real:=0.0;
quantity Cvar : real;
quantity Felec : real;
quantity Fstoppers : real;
quantity acceleration : real;
quantity dCvar_dx : real;
quantity x:real:=x_init;

quantity vC across iC through e1 to e2;
quantity a_ext across accel to electrical_ground;
quantity forc across iforce through force to electrical_ground;
quantity xx across iX through pos to electrical_ground;
quantity cc across icc through capvar to electrical_ground;
quantity chch across ichch through capcharge to electrical_ground;
quantity pp across ipp through power to electrical_ground;
quantity power1:real;
quantity energy_i:real;

BEGIN

--POWER CALCULATION*****************************
P1: PROCESS (clk)
BEGIN
```

```
clk<=not clk after delta_t/2;
if clk'event and clk='1' then
     p<=(energy_i-tmp)/0.2;
     tmp<=energy_i;
end if;
END PROCESS P1;
--*******************************************

xx==x;
cc==Cvar;
chch==charge;
Cvar==capa(x);
dCvar_dx==dc_dx(x);

vitesse==x'dot;
acceleration==vitesse'dot;
vC==charge/(Cvar+1.0e-20);
forc==Felec;
Felec==vC*vC*dCvar_dx/2.0;

--if (abs(x)>xmax) use Fstoppers==0.0; --model without stoppers
if (abs(x)>xmax) use Fstoppers==-vitesse*mu_stopper;
else Fstoppers==0.0;
end use;

m*acceleration==-k*x-kv*vitesse+Felec-m*a_ext+Fstoppers;
charge==ic'integ+Q0;
--*****************************************************
power1==-Felec*vitesse;
energy_i==power1'integ;
pp==p;
END;
```

Model of the In-Plane Gap closing Combs structure developed in ESIEE Paris in 2011

```
LIBRARY DISCIPLINES;
USE DISCIPLINES.ELECTROMAGNETIC_SYSTEM.ALL;
library IEEE;
use IEEE.MATH_REAL.all;

ENTITY electrostatic_transducer IS
    GENERIC(
        d:real:=1.0e-6;           -- transducer's gap
        d_stoppers:real:=1.0e-6; -- stopper position
        l:real:=1.0e-2;           -- transducer's length
        w:real:=400.0e-6;         -- transducer's width
        N: integer;               -- number of capacitors
        Q0:real:=0.0;             -- initial charge
        x0:real:=0.0;             -- initial position
        mu_stoppers:real:=1.0e1; -- viscosity factor
        k_stoppers:real:=1.0e5   -- coefficient of elasticity of the spring
                );

    PORT (
        TERMINAL C1    : Electrical; -- C1 and C2 are the capacitor's electrodes
        TERMINAL C2    : Electrical;
        TERMINAL Mp    : Electrical;
        TERMINAL Mm    : Electrical;
-- Mp and Mm are the mechanical terminals providing the transducer's force (voltage).
-- Their polarity is important
        TERMINAL pos   : Electrical; -- the x-coordinate of the transducer
        TERMINAL capa  : Electrical; -- an output terminal for capacitance measurement
        TERMINAL power : Electrical;
-- an output terminal providing the calculated converted average power
        TERMINAL test1 : Electrical;
        TERMINAL test2 : Electrical
-- test1 and test2 are used for internal signals measurement
        );
END;
```

```
ARCHITECTURE gap_closing_transducer OF electrostatic_transducer IS

function transd_cap_gap_closing(x:real; d:real;S:real) return real is
variable capa:real;
begin
    capa:=8.85e-12*S/(d-x);  -- Cvar gap-closing
return capa;
end;

function transd_cap_gap_closing_sym(x:real;N:integer;d:real;l:real;h:real) return real is
variable capa:real;
constant a:real:=0.025; -- acceleration of the mobile electrode of transducer
begin
    capa:=8.85e-12*real(N)*l/(2.0*a)*log((d-x+2.0*h*a)*(d+x+2.0*h*a)/(d*d-x*x));
-- Cvar gap-closing symmetrical
return capa;
end;

quantity charge : real:=0.0;
quantity dCvar_dx : real;
quantity uC across iC through C1 to C2;   -- the capacitor voltage
quantity force across v through Mp to Mm; -- the force of transducer
quantity x across ix through pos to electrical_ground;
-- x is the position of the mobile electrode of transducer
quantity Cvar across icapa through capa to electrical_ground;
quantity F_stoppers:real; -- position of the mobile electrode of transducer
quantity test_param1 across itest1 through test1 to electrical_ground;
quantity test_param2 across itest2 through test2 to electrical_ground;

constant dx :real:=0.001e-6; --

--For the average power calculation:
quantity pp across ipp through power to electrical_ground;
quantity energy_i:real;
quantity power1:real;
constant delta_t:time:=200.0 ms;
signal clk: bit:='1';
signal p: real:=0.0;
signal tmp:real:=0.0;

BEGIN

--AVERAGE POWER CALCULATION*****************************
P1: PROCESS (clk)
BEGIN
clk<=not clk after delta_t/2;
if clk'event and clk='1' then
    p<=(energy_i-tmp)/0.2;
    tmp<=energy_i;
end if;
END PROCESS P1;
power1==-force*v;
energy_i==power1'integ;
pp==p;
--*************************************************
-- Mechanical side model : a force generator.
-- The position must be known for the force calculation
-- We integrate the speed (the current through Mp and Mm) to get the position
x==-v'integ+x0;
-- then we calculate the capacitance gradient at x
dCvar_dx==(transd_cap_gap_closing_sym(x+dx,N,d,l,w)-transd_cap_gap_closing_sym(x,N,d,l,w))/dx;
-- and the force

if (x'above(d-d_stoppers)) or not (x'above(-d+d_stoppers)) use
    F_stoppers==mu_stoppers*v-k_stoppers*(x-(d-d_stoppers));
else
    F_stoppers==0.0;
end use;
force==uC*uC*dCvar_dx/2.0+F_stoppers;

test_param1==F_stoppers;
test_param2==v;

-- Electrical side model : a simple capacitor
-- first we calculate the capacitance value at x
Cvar==transd_cap_gap_closing_sym(x,N,d,l,w);
```

```
-- then the charge
charge==iC'integ+Q0;
-- then the capacitor voltage
uC==charge/Cvar;

break on X'above(d-d_stoppers);
break on X'above(-d+d_stoppers);
END;
```

Appendix B

VHDL-AMS model of the flyback switch

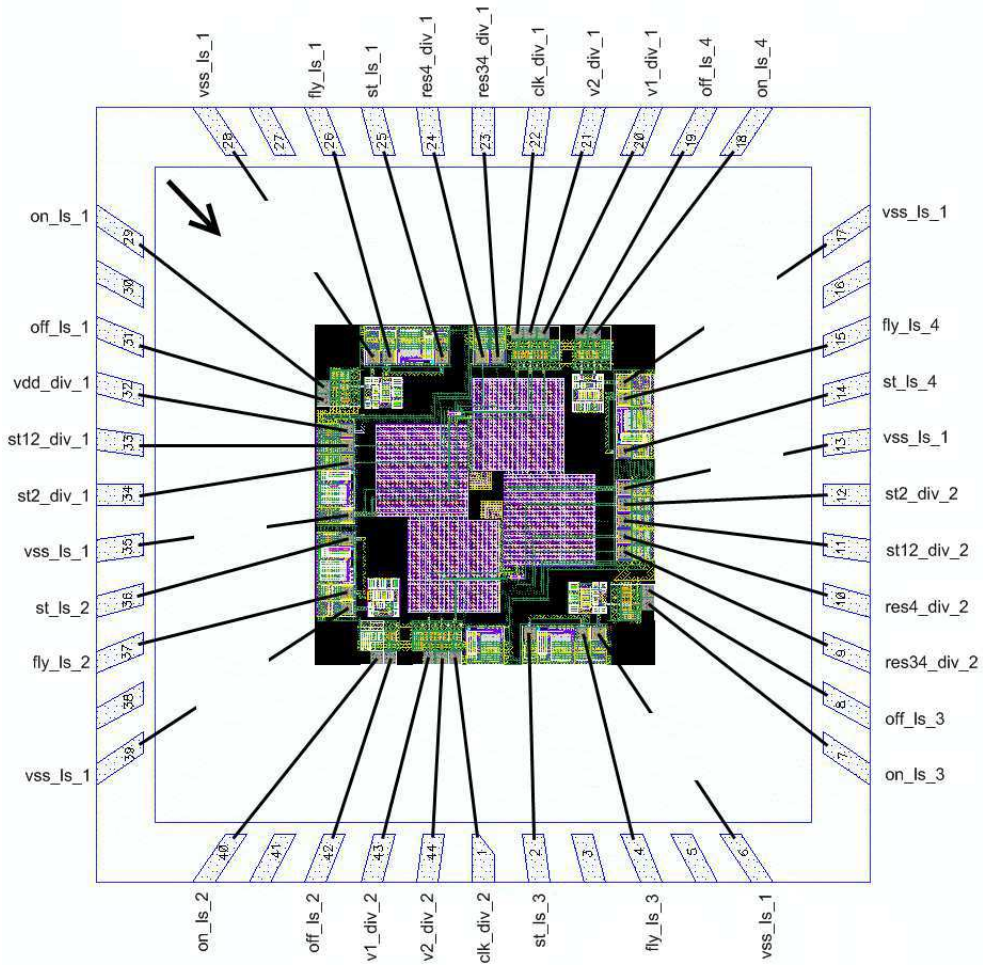
```
LIBRARY IEEE, DISCIPLINES;
USE IEEE.math_real.ALL;
USE DISCIPLINES.ELECTROMAGNETIC_SYSTEM.ALL;

ENTITY adms_vhdlams_voltage_driven IS
     GENERIC (
          ron        : Real := 30.0;            --switch on resistance
          roff       : Real := 10.0e9;          --switch off resistance
          clkp       : time := 10.0 ms;     --period of sampling
          period     : Time := 10000 ms         --period of calibration
        );

        PORT (
                TERMINAL ep       : Electrical ;
                TERMINAL em       : Electrical ;
        TERMINAL store    : Electrical ;
                TERMINAL common   : Electrical ;
                TERMINAL res       : Electrical ;
                TERMINAL debug     : Electrical
        );
END ENTITY adms_vhdlams_voltage_driven;

ARCHITECTURE adms_vhdlams OF adms_vhdlams_voltage_driven IS

quantity v_store across store to common ;
quantity v_res across res to common;
quantity vsw across isw through ep to em;
quantity debug_q across i_debug_q through debug to common;
quantity v1 : real:=5.0;
quantity v2 : real:=5.0;

signal ison : boolean:=false;
signal clk: bit:='1';
signal horloge: bit:='1';
signal v_store_max:real:=10.0;
signal debug_sig:real:=0.0;
signal init:boolean:=false;
signal calibration:boolean:=false;
signal new_calibration:boolean:=false;
signal end_calibration:boolean:=false;
signal first_cycle:boolean:=true;
signal k1:real:=1.0;
signal k2:real:=1.01;
signal kv1:real:=0.1;
signal kv2:real:=0.7;

BEGIN

--**********************CLOCK************************************
```

```
P1: PROCESS(horloge)
BEGIN
horloge<=not horloge after period/2.0;
END PROCESS P1;

--********************START_OF_CALIBRATION*********************
P2: PROCESS(horloge,v_store'above(v_res*k1),v_store'above(v_res*k2))
BEGIN
if horloge'event and horloge='1' then
    if v_store'above(v_res*k1) then
        init<=true;
        calibration<=false;
    else
        init<=false;
        calibration<=true;
    end if;
end if;
-----------------------------------------------------
if init then
    if not v_store'above(v_res*k2) then
        init<=false;
        calibration<=true;
    else
        calibration<=false;
    end if;
end if;
-----------------------------------------------------
if new_calibration then
        calibration<=false;
end if;
-----------------------------------------------------
END PROCESS P2;

--***************Vstore max CALCULATION**************************
P3: PROCESS(new_calibration,clk)
variable v_1: real:=5.0;
variable v_2: real:=5.01;
variable dv: real:=0.0;
variable dv_last: real:=100.0;
variable dv_min: real:=0.02;
variable par: boolean:=true;
variable count:real:=0.0;
BEGIN
-----------------------------------------------------
if new_calibration then
    end_calibration<=false;
    if clk'event and clk='1' then
        dv_last:=dv;
        count:=count+1.0;
        if par then
            v_1:=v_store;
            if v_2>0.0 then
               dv:=v_1-v_2;
            end if;
        else
            v_2:=v_store;
            if v_1>0.0 then
               dv:=v_2-v_1;
        end if;
     end if;
     par:=not par;
-----------------------------------------------------
     if v_res>10.0 then
         kv1<=0.1;
         kv2<=0.65;
         dv_min:=1.0e-1;
     elsif v_res>15.0 then
         kv1<=0.1;
         kv2<=0.7;
         dv_min:=1.5e-1;
     elsif v_res>20.0 then
         kv1<=0.15;
         kv2<=0.75;
         dv_min:=2.0e-1;
     elsif v_res>25.0 then
         kv1<=0.15;
```

```
          kv2<=0.8;
          dv_min:=2.5e-1;
     end if;
-----------------------------------------------------
     if dv<dv_min and count>3.0 then
          count:=0.0;
          v_store_max<=v_store;
          end_calibration<=true;
     end if;
     clk<=not clk after clkp/2;
end if;
debug_sig<=dv;
END PROCESS P3;

P4: PROCESS(first_cycle, calibration, end_calibration, init)
BEGIN
-----------------------------------------------------
if end_calibration then
        new_calibration<=false;
end if;
-----------------------------------------------------
if first_cycle then
        new_calibration<=true;
        first_cycle<=false;
end if;
-----------------------------------------------------
if calibration then
        new_calibration<=true;
end if;
END PROCESS P4;

--*************************POWER SWITCH DESCRIPTION******************
P5: PROCESS
variable off: boolean :=true;
BEGIN
ison <= not off;
CASE off IS
    WHEN true =>
        WAIT until v_store'above(v2);
        off:=false;
    WHEN false =>
        WAIT until NOT v_store'above(v1);
        off:=true;
END CASE;
END PROCESS P5;

--*************************CURRENT CALCULATION***********************
IF ison use isw==vsw/ron;
ELSE isw==vsw/roff;
END use;
BREAK ON ison;
-----------------------------------------------------
debug_q==debug_sig;

--**********************CALCULATIONS of V1 and V2**********************
if init use
    v1==v_res;
    v2==0.0;
elsif first_cycle or calibration use
    v1==v_res;
    v2==100.0;
elsif end_calibration use
    v1==v_res+kv1*(v_store_max-v_res);
    v2==v_res+kv2*(v_store_max-v_res);
else
    v1==50.0;
    v2==100.0;
end use;
-----------------------------------------------------
break on first_cycle;
break on init;
break on calibration;
break on end_calibration;

END ARCHITECTURE adms_vhdlams;
```

Appendix C

Bonding diagram of the fabricated chip



Description of pins of HARVESTER_SW_DIV.

The fabricated chip incorporates 4 high-side switches&drivers and 2 sample&hold circuits for external voltage dividers.

The names of pins are composed of the following template:

[destination]_[instance name]_[instance index]

Instance name for the level shifter – **ls**. Instance name for the divider interface – **div**.

Pin #	Pin name	Description
1	clk_div_2	I/O clock for **S**&**H2**
2	st_ls_3	power-pin to *store* node for **ls3**
3	–	–
4	fly_ls_3	I/O to *fly* node for **ls3**
5	–	–
6	vss_ls_1	common ground
7	on_ls_3	I/O *on* for **ls3**
8	off_ls_3	I/O *off* for **ls3**
9	res34_div_2	I/O between resistors R3 and R4 for **S**&**H2**
10	res4_div_2	I/O between gnd and R4 for **S**&**H2**
11	st12_div_2	I/O between resistors R1 and R2 for **S**&**H2**
12	st2_div_2	I/O between gnd and R2 for **S**&**H2**
13	vss_ls_1	common ground
14	st_ls_4	power-pin to *store* node for **ls4**
15	fly_ls_4	I/O to *fly* node for **ls4**
16	–	–
17	vss_ls_1	common ground
18	on_ls_4	I/O *on* for **ls4**
19	off_ls_4	I/O *off* for **ls4**
20	v1_div_1	I/O between divider and v1 holding cap. for **S**&**H1**
21	v2_div_1	I/O between divider and v2 holding cap. for **S**&**H1**
22	clk_div_1	I/O clock for **S**&**H1**
23	res34_div_1	I/O between resistors R3 and R4 for **S**&**H1**
24	res4_div_1	I/O between gnd and R4 for **S**&**H1**
25	st_ls_1	power-pin to *store* node for **ls1**
26	fly_ls_1	I/O to *fly* node for **ls1**
27	–	–
28	vss_ls_1	common ground
29	on_ls_1	I/O *on* for **ls1**
30	–	–
31	off_ls_1	I/O *off* for **ls1**
32	vdd_div_1	power-pin to supply LV-pads for **S**&**H1**
33	st12_div_1	I/O between resistors R1 and R2 for **S**&**H1**
34	st2_div_1	I/O between gnd and R2 for **S**&**H1**
35	vss_ls_1	common ground
36	st_ls_2	power-pin to *store* node for **ls2**
37	fly_ls_2	I/O to *fly* node for **ls2**
38	–	–
39	vss_ls_1	common ground
40	on_ls_2	I/O *on* for **ls2**
41	–	–
42	off_ls_2	I/O *off* for **ls1**
43	v1_div_2	I/O between divider and v1 holding cap. for **S**&**H2**
44	v2_div_2	I/O between divider and v2 holding cap. for **S**&**H2**

Note! Only instances **ls1** and **ls2** are symmetrically wired.

Bibliography

[Ackermann05] T. Ackermann. *Wind Power in Power Systems*, volume 8. Wiley Online Library, 2005.

[Amirtharajah98] R. Amirtharajah and A. P. Chandrakasan. Self-Powered Signal Processing Using Vibration-Based Power Generation. *IEEE Journal of Solid-State Circuits*, 33(5):687–695, 1998.

[Arnold07] D. P. Arnold. Review of Microscale Magnetic Power Generation. *IEEE transaction on magnetics*, 43(11):3940–3951, November 2007.

[Aroudi13] A. El. Aroudi, M. López-Suárez, E. Alarcón, R. Rurali, and G. Abadal. Nonlinear Dynamics in a Graphene Nanostructured Device for Energy Harvesting. In *2013 IEEE International Symposium on Circuits and Systems*, pages 2727–2730, Beijing, China, 2013.

[Aydil06] E. S. Aydil, D. J. Norris, U. Kortshagen, and X. Zhu. Photovoltaic Devices Based on Nanoparticles and Nanowires. In *NSF Nanoscale Science and Engineering Grantees Conference*, 2006.

[Barroca13] N. Barroca, L. M. Borges, F. J. Velez, F. Monteiro, M. Górski, and João Castro-Gomes. Wireless sensor networks for temperature and humidity monitoring within concrete structures. *Construction and Building Materials*, 40:1156–1166, March 2013.

[Basset03] P. Basset. *Conception, réalisation et test d'un micro système de transport alimenté à distance*. PhD thesis, Univesité de Lille1, 2003.

[Basset09] P. Basset, D. Galayko, A. M. Paracha, F. Marty, A. Dudka, and T. Bourouina. A batch-fabricated and electret-free silicon electrostatic vibration energy harvester. *Journal of Micromechanics and Microengineering*, 19(11):115025 (12pp), November 2009.

[Beeby06] S. P. Beeby, M. J. Tudor, and N. M. White. Energy harvesting vibration sources for microsystems applications. *Measurement Science and Technology*, 17(12):R175–R195, December 2006.

[Beeby07] S. P. Beeby, R. N. Torah, M. J. Tudor, P. Glynne-Jones, T. O'Donnell, C R Saha, and S Roy. A micro electromagnetic generator for vibration energy harvesting. *Journal of Micromechanics and Microengineering*, 17(7):1257–1265, 2007.

[Benedettini09] O. Benedettini, T. S. Baines, H. W. Lightfoot, and R. M. Greenough. State-of-the-art in integrated vehicle health management. *Proceedings of the Institution of Mechanical Engineers, Part G: Journal of Aerospace Engineering*, 223(2):157–170, March 2009.

[Blokhina12] E. Blokhina, D. Galayko, P. Harte, P. Basset, and O. Feely. Limit on converted power in resonant electrostatic vibration energy harvesters. *Applied Physics Letters*, 101(17):173904, 2012.

[Blystad10] L.-C. J. Blystad and E. Halvorsen. A piezoelectric energy harvester with a mechanical end stop on one side. *Microsystem Technologies*, 17(4):505–511, November 2010.

[Boisseau11] S. Boisseau, G. Despesse, T. Ricart, E. Defay, and A. Sylvestre. Cantilever-based electret energy harvesters. *Smart Materials and Structures*, 20(10):105013, October 2011.

[Boisseau12] S. Boisseau, G. Despesse, and B. A. Seddik. Adjustable Nonlinear Springs to Improve Efficiency of Vibration Energy Harvesters. *arXiv:1207.4559*, 2012.

[Bowers09] B. J. Bowers and D. P. Arnold. Spherical, rolling magnet generators for passive energy harvesting from human motion. *Journal of Micromechanics and Microengineering*, 19(9):094008, September 2009.

[Bu12] L. Bu, X. Wu, X. Wang, and L. Liu. Liquid encapsulated electrostatic energy harvester for low-frequency vibrations. *Journal of Intelligent Material Systems and Structures*, 24(1):61–69, September 2012.

[Büren06] T. V. Büren, P. D. Mitcheson, T. C. Green, E. M. Yeatman, A. S. Holmes, and Gerhard Tröster. Optimization of Inertial Micropower Generators for Human Walking Motion. *Sensors Journal, IEEE*, 6(1):28–38, 2006.

[Caicedo01] J.M. Caicedo, J. Marulanda, P. Thomson, and S.J. Dyke. Monitoring of bridges to detect changes in structural health. In *American Control Conference, 2001. Proceedings of the 2001*, pages 453–458, 2001.

[Cannillo09] F. Cannillo, C. Toumazou, and T.-S. Lande. Nanopower Subthreshold MCML in Submicrometer CMOS Technology. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 56(8):1598–1611, 2009.

[Cao07] X. Cao, W.-J. Chiang, Y.-C. King, and Y.-K. Lee. Electromagnetic Energy Harvesting Circuit With Feedforward and Feedback DC-DC PWM Boost Converter for Vibration Power Generator System. *Power Electronics, IEEE Transactions on*, 22(2):679–685, 2007.

[Cheng07] S. Cheng, N. Wang, and D. P. Arnold. Modeling of magnetic vibrational energy harvesters using equivalent circuit representations. *Journal of Micromechanics and Microengineering*, 17(11):2328–2335, 2007.

[Chiu06] Y. Chiu, C.-T. Kuo, and Y.-S. Chu. Design and fabrication of a micro electrostatic vibration-to-electricity energy converter. In *Symposium on Design Test Integration and Packaging of MEMS/MOEMS (DTIP)*, pages 298–303, 2006.

[Christmann10] J. F. Christmann, E. Beigné, C. Condemine, and J. Willemin. An innovative and efficient Energy Harvesting Platform architecture for autonomous microsystems. In *NEWCAS Conference (NEWCAS), 2010 8th IEEE International*, pages 173–176, 2010.

[Christmann12] J. F. Christmann, E. Beigné, C. Condemine, J. Willemin, and C. Piguet. Energy harvesting and power management for autonomous sensor nodes. *Proceedings of the 49th Annual Design Automation Conference on - DAC '12*, page 1049, 2012.

[Chung00] D.D.L. Chung. Materials for electromagnetic interference shielding. *Journal of Materials Engineering and Performance*, 9(3):350–354, 2000.

[Cottone09] F. Cottone, H. Vocca, and L. Gammaitoni. Nonlinear Energy Harvesting. *Physical Review Letters*, 102(8):080601 (4pp), February 2009.

[Cunha98] A.I.A. Cunha, M.C. Schneider, and C. Galup-Montoro. An MOS transistor model for analog circuit design. *Solid-State Circuits, IEEE Journal of*, 33(10):1510–1519, 1998.

[Declercq93] M. Declercq and M. Schubert. Intermediary circuit between a low voltage logic circuit and a high voltage output stage in standard CMOS technology, 1993.

[Defosseux11] M. Defosseux, M. Allain, P. Ivaldi, E. Defay, and S. Basrour. Highly efficient piezoelectric micro harvester for low level of acceleration fabricated with a CMOS compatible process. In *Solid-State Sensors, Actuators and Microsystems Conference (TRANSDUCERS), 2011 16th International*, pages 1859–1862, Beijing, 2011.

[Denier10] U. Denier. Analysis and Design of an Ultralow-Power CMOS Relaxation Oscillator. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 57(8):1973–1982, August 2010.

[Despesse05] G. Despesse, T. Jager, J. J. Chaillout, J. M. Léger, A. Vassilev, S Basrour, and B Charlot. Fabrication and Characterization of High Damping Electrostatic Micro Devices for Vibration Energy Scavenging. In *Proceeding of DTIP of MEMS/MOEMS conference*, pages 386–390, 2005.

[Doutreloigne01] J. Doutreloigne and H. D. Smet. A Versatile Micropower High-Voltage Flat-Panel Intelligent Interface Technology. *IEEE Journal of Solid-State Circuits*, 36(12):2039–2048, 2001.

[Dudka09a] A. Dudka, D. Galayko, and P. Basset. Smart adaptive power management in electrostatic harvester of vibration energy. In *PowerMEMS Workshop on Micro and Nanotechnology for Power Generation and Energy Conversion Applications 2009*, pages 257–260, Washington DC, USA, 2009.

[Dudka09b] A. Dudka, D. Galayko, and P. Basset. VHDL-AMS modeling of adaptive electrostatic harvester of vibration energy with dual-output DC-DC converter. In *2009 IEEE Behavioral Modeling and Simulation Workshop*, pages 13–18, September 2009.

[Dudka12] A. Dudka, D. Galayko, and P. Basset. Design of Controller IC for Asynchronous Conditioning Circuit of an Electrostatic Vibration Energy Harvester. In *IEEE International Conference on Internet of Things , 2012 Workshop on energy and Wireless Sensors*, 2012.

[Dudka13a] A. Dudka, P. Basset, F. Cottone, E. Blokhina, and D. Galayko. Wideband Electrostatic Vibration Energy Harvester (e-VEH) Having a Low Start-Up Voltage Employing a High-Voltage Integrated Interface. In *PowerMEMS*, pages 612–616, London, UK, 2013.

[Dudka13b] A. Dudka, D. Galayko, and P. Basset. IC design of an adaptive high-voltage electrostatic vibration energy harvester. In *Proceeding of the 15th symposium on Design, Test, Integration and Packaging Conference (DTIP'13)*, pages 272–277, Barcelona, Spain, 2013.

[Egbert07] R. G. Egbert, M. R. Harvey, and B. P. Otis. Microscale Silicon Thermoelectric Generator with Low Impedance for Energy Harvesting, 2007.

[Ehsani09] M. Ehsani, Y. Gao, and A. Emadi. *Modern electric, hybrid electric, and fuel cell vehicles: fundamentals, theory, and design*. CRC, 2009.

[Florentino11] H. R. Florentino, R. C. S. Freire, A. V. S. Sá, C. Florentino, and D. Galayko. Electrostatic vibration energy harvester with piezoelectric start-up generator. In *Circuits and Systems (ISCAS), 2011 IEEE International Symposium on*, pages 1343–1346. IEEE, 2011.

[Flynn92] M.P. Flynn and S.U. Lidholm. A 1.2-um CMOS current-controlled oscillator. *Solid-State Circuits, IEEE Journal of*, 27(7):982–987, 1992.

[Galayko07] D. Galayko, R. Pizarro, P. Basset, A. M. Paracha, and G. Amendola. AMS modeling of controlled switch for design optimization of capacitive vibration energy harvester. In *2007 IEEE International Behavioral Modeling and Simulation Workshop*, pages 115–120, September 2007.

[Galayko11a] D. Galayko and P. Basset. A General Analytical Tool for the Design of Vibration Energy Harvesters (VEHs) Based on the Mechanical Impedance Concept. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 58(2):299–311, February 2011.

[Galayko11b] D. Galayko, R. Guillemet, A. Dudka, and P. Basset. Comprehensive dynamic and stability analysis of electrostatic Vibration Energy Harvester (E-VEH). In *16th International Solid-State Sensors, Actuators and Microsystems Conference (TRANSDUCERS), 2011*, pages 2382–2385, 2011.

[Galchev12] Tzeno Galchev, Ethem Erkan Aktakka, and Khalil Najafi. A Piezoelectric Parametric Frequency Increased Generator for Harvesting Low-Frequency Vibrations. *Journal of Microelectromechanical Systems*, 21(6):1311–1320, December 2012.

[Gasnier13] P. Gasnier, J. Willemin, S. Boisseau, G. Despesse, C. Condemine, G. Gouvernet, and J-J. Chaillout. An autonomous piezoelectric energy harvesting IC based on a synchronous multi-shots technique. *2013 Proceedings of the ESSCIRC (ESSCIRC)*, pages 399–402, September 2013.

[Gateway] The Mobile Gateway. Nanoscience and the Mobile Device.

[Glynne-Jones01] P. Glynne-Jones, S.P. Beeby, and N.M White. Towards a piezoelectric vibration-powered microgenerator. *Science, Measurement and Technology, IEE Proceedings*, 148(2):68–72, 2001.

[Guillemet12] Raphaël Guillemet. *Etude et réalisation d'un récupérateur d'énergie vibratoire par transduction électrostatique en technologie MEMS silicium.* PhD thesis, Université Paris-Est, 2012.

[Guillemet13] R. Guillemet, P. Basset, D. Galayko, F. Cottone, F. Marty, and T Bourouina. Wide-band MEMS electrostatic vibration energy harvesters based on gap-closing interdigited combs with a trapezoidal cross section. In *Micro Electro Mechanical Systems (MEMS), 2013 IEEE 26th International Conference on*, pages 817–820, 2013.

[Hamakawa87] Y. Hamakawa. Photovoltaic power. *Sci. Am.;(United States)*, 256(4):87–92, 1987.

[Hoffmann09] D. Hoffmann, B. Folkmer, and Y. Manoli. Fabrication, characterization and modelling of electrostatic micro-generators. *Journal of Micromechanics and Microengineering*, 19(9):094001, September 2009.

[Holladay02] J. D. Holladay, E. O. Jones, M. Phelps, and J. Hu. Microfuel processor for use in a miniature power supply. *Journal of Power Sources*, 108(1):21–27, 2002.

[Jeon05] Y.B. Jeon, R. Sood, J.-h. Jeong, and S.-G. Kim. MEMS power generator with transverse mode thin film PZT. *Sensors and Actuators A: Physical*, 122(1):16–22, July 2005.

[Kasyap02] A. Kasyap, J. Lim, K. Ngo, A. Kurdila, T. Nishida, Mark Sheplak, and Lou Cattafesta. Energy Reclamation from a Vibrating Piezoceramic Composite Beam. In *9th International Congress on Sound and Vibration*, Orlando, FL, 2002.

[Kempitiya10] A. Kempitiya, D. A. Borca-Tasciuc, and M. M. Hella. Low power electrostatic energy harvesting system IC. In *Proc. PowerMEMS*, pages 91–94, Leuven, Belgium, 2010.

[Kempitiya12] A. Kempitiya, D. A. Borca-Tasciuc, and M. M. Hella. Analysis and Optimization of Asynchronously Controlled Electrostatic Energy Harvesters. *IEEE Transactions on Industrial Electronics*, 59(1):456–463, 2012.

[Kempitiya13] A. Kempitiya, D.-A. Borca-Tasciuc, and M. M. Hella. Low-Power Interface IC for Tri-plate Electrostatic Energy Converters. *IEEE Transactions on Power Electronics*, 28(2):609–614, February 2013.

[Khalil10] R. Khalil, A. Dudka, D. Galayko, and P. Basset. High-voltage low power analogue-to-digital conversion for adaptive architectures of capacitive vibration energy harvesters. In *PowerMEMS Workshop on Micro and Nanotechnology for Power Generation and Energy Conversion Applications 2010*, pages 147–150, Leuven, Belgium, 2010.

[Khorasani08] M. Khorasani, L. van den Berg, P. Marshall, M. Zargham, V. Gaudet, Duncan Elliott, and Stephane Martel. Low-power static and dynamic high-voltage CMOS level-shifter circuits. In *2008 IEEE International Symposium on Circuits and Systems*, number 1, pages 1946–1949, May 2008.

[Kim07] H. Kim, S. Priya, H. Stephanou, and K. Uchino. Consideration of Impedance Matching Techniques for Efficient Piezoelectric Energy Harvesting. *Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on*, 54(9):1851–1859, 2007.

[Kong10] N. Kong, D. S. Ha, A. Erturk, and D. J. Inman. Resistive Impedance Matching Circuit for Piezoelectric Energy Harvesting. *Journal of Intelligent Material Systems and Structures*, 21(13):1293–1302, January 2010.

[Kuehne08] I. Kuehne. Power-MEMS - A capacitive vibration-to-electrical energy converter with built-in voltage. *Sensors and Actuators A: Physical*, 142(1):263–269, 2008.

[Kulah08] H Kulah and Khalil Najafi. Energy scavenging from low-frequency vibrations by using frequency up-conversion for wireless sensor applications. *IEEE Sensors Journal*, 8(3):261–268, 2008.

[Kulkarni06] S. Kulkarni, S. Roy, T. O'Donnell, S. Beeby, and J. Tudor. Electromagnetic micro power generator on Silicon for wireless sensor nodes. In *IEEE International Magnetics Conference, 2006. INTERMAG 2006.*, page 317, 2006.

[Kwong08] P. Kwong, K. S. Vincent, V. K. S. An, Y. Susanti, P. K. Chan, and V K S Ong. An ultra low-power Successive Approximation ADC using an offset-biased auto-zero comparator. *IEEE Asia Pacific Conference on Circuits and Systems, 2008 (APCCAS'08)*, pages 284–287, 2008.

[Landau76] L. D. Landau and E. M. Lifshitz. *Course of Theoretical Physics: Mechanics*. Butterworth-Heinemann, Oxford, U.K., 1976.

[Le06] T. T. Le, J. Han, A. V. Jouanne, K. Mayaram, and T. S. Fiez. Piezoelectric Micro-Power Generation Interface Circuits. *IEEE Journal of Solid-State Circuits*, 41(6):1411–1420, 2006.

[Lee82] Y.S. Lee and K.D. Wise. A batch-fabricated silicon capacitive pressure transducer with low temperature sensitivity. *IEEE Transactions on Electron Devices*, 29(1):42–48, January 1982.

[Lefeuvre06] E. Lefeuvre, A. Badel, C. Richard, L. Petit, and D. Guyomar. A comparison between several vibration-powered piezoelectric generators for standalone systems. *Sensors and Actuators A: Physical*, 126(2):405–416, February 2006.

[Lefeuvre09] E. Lefeuvre, G. Sebald, D. Guyomar, M. Lallart, and C. Richard. Materials, structures and power interfaces for efficient piezoelectric energy harvesting. *Journal of Electroceramics*, 22(1-3):171–179, November 2009.

[Linares91] B. B. Linares, A. Rodriguez-Vazquez, E. Sanchez-Sinencio, and J.L. Huertas. CMOS OTA-C high-frequency sinusoidal oscillators. *Solid-State Circuits, IEEE Journal of*, 26(2):160–165, 1991.

[Madou02] M. Madou. *Fundamentals of microfabrication: the science of miniaturization*. CRC press, 2002.

[Maloberti07] F. Maloberti. *Data Converters*. 2007.

[Marzencki05] M. Marzencki, S. Basrour, B. Charlot, A. Grasso, M. Colin, and L. Valbin. Design and Fabrication of Piezoelectric Micro Power Generators for Autonomous Microsystems. In *Symposium on Design Test Integration and Packaging of MEMS/MOEMS (DTIP)*, pages 299–302, 2005.

[Maurath08] D. Maurath, M. Ortmanns, and Y. Manoli. High efficiency, low-voltage and self-adjusting charge pump with enhanced impedance matching. In *Circuits and Systems, 2008. MWSCAS 2008. 51st Midwest Symposium on*, pages 189–192, 2008.

[Mauricio05] C.-G. E. Mauricio, C. Galup-Montoro, and M. C. Schneider. A 2-nW 1.1-V Self-Biased Current Reference in CMOS Technology. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 52(2):61–65, 2005.

[Meninger01] S. Meninger, J.O. Mur-Miranda, R. Amirtharajah, A. Chandrakasan, and J.H. Lang. Vibration-to-electric energy conversion. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 9(1):64–76, February 2001.

[Miao06] P. Miao, P. D. Mitcheson, a. S. Holmes, E. M. Yeatman, T. C. Green, and B. H. Stark. MEMS inertial power generators for biomedical applications. *Microsystem Technologies*, 12(10-11):1079–1083, April 2006.

[Miller12] L.M. Miller, P.D. Mitcheson, E. Halvorsen, and P.K. Wright. Coulomb-damped resonant generators using piezoelectric transduction. *Applied Physics Letters*, 100(23):233901–233901–4, 2012.

[Mitcheson03] P. D. Mitcheson, P. Miao, B. H. Stark, A. S. Holmes, E. M. Yeatman, and T. C. Green. Analysis and Optimisation of MEMS Electrostatic On-Chip Power Supply for Self-Powering of Slow-Moving Sensors. In *Proc. Eurosensors XVII*, pages 30–31, Guimaraes, Portugal, 2003.

[Mitcheson04] P. D. Mitcheson, T. C. Green, E. M. Yeatman, and A. S. Holmes. Architectures for Vibration-Driven Micropower Generators. *Journal of Microelectromechanical Systems*, 13(3):429–440, 2004.

[Mitcheson08] P. D. Mitcheson, E. M. Yeatman, K. G. Rao, A. S. Holmes, and T. C. Green. Energy harvesting from human and machine motion for wireless electronic devices. *Proceedings of the IEEE*, 96(9):1457–1486, 2008.

[Mitcheson10] P. D. Mitcheson and T. T. Toh. Power management electronics. *Energy Harvesting for Autonomous Systems*, pages 1–57, 2010.

[Mitcheson12] P. D. Mitcheson and T. C. Green. Maximum Effectiveness of Electrostatic Energy Harvesters When Coupled to Interface Circuits. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 59(12):3098–3111, 2012.

[Miyazaki03] M. Miyazaki, H. Tanaka, G. Ono, T. Nagano, N. Ohkubo, T. Kawahara, and K. Yano. Electric-energy generation using variable-capacitive resonator for power-free LSI: efficiency analysis and fundamental experiment. *Proceedings of the 2003 International Symposium on Low Power Electronics and Design, 2003 (ISLPED '03)*, pages 193–198, 2003.

[Mourabit05] A. E. Mourabit, G.-N. Lu, and P. Pittet. Wide-Linear-Range Subthreshold OTA for Low-Power, Low-Voltage, and Low-Frequency Applications. 52(8):1481–1488, 2005.

[Mur-Miranda04] J.O. Mur-Miranda. *Electrostatic Vibration-to-Electric Energy Conversion*. PhD thesis, MIT, 2004.

[Najafi11] K. Najafi, T. Galchev, E.E. Aktakka, R.L. Peterson, and J. McCullagh. Microsystems for energy harvesting. In *Solid-State Sensors, Actuators and Microsystems Conference (TRANSDUCERS), 2011 16th International*, pages 1845–1850, 2011.

[Naruse09] Y. Naruse, N. Matsubara, K. Mabuchi, M. Izumi, and S. Suzuki. Electrostatic micro power generation from low-frequency vibration such as human motion. *Journal of Micromechanics and Microengineering*, 19(9):19–22, 2009.

[Neri11] I. Neri, F. Travasso, H. Vocca, and L. Gammaitoni. Nonlinear noise harvesters for nanosensors. *Nano Communication Networks*, 2(4):230–234, December 2011.

[Ottman02] G. K. Ottman, H. F. Hofmann, A. C. Bhatt, and G. A. Lesieutre. Adaptive piezoelectric energy harvesting circuit for wireless remote power supply. *Power Electronics, IEEE Transactions on*, 17(5):669–676, 2002.

[Paing08] T. Paing, J. Shin, R. Zane, and Z. Popovic. Resistor Emulation Approach to Low-Power RF Energy Harvesting. *Power Electronics, IEEE Transactions on*, 23(3):1494–1501, 2008.

[Pan03] D. Pan, H. W. Li, and B. M. Wilamowski. A low voltage to high voltage level shifter circuit for MEMS application. *Proceedings of the 15th Biennial University/Government/ Industry Microelectronics Symposium*, pages 128–131, 2003.

[Paracha07] A. M. Paracha, P. Basset, F. Marty, A. V. Chasin, P. Poulichet, and T. Bourouina. A high power density electrostatic vibration-to-electric energy converter based on an in-plane overlap plate (IPOP) mechanism. In *Symposium on Design Test Integration and Packaging of MEMS/MOEMS (DTIP)*, Stresa, Lago Maggiore, Italy, 2007.

[Paracha08] A. M. Paracha, P. Basset, D. Galayko, A. Dudka, F. Marty, and T. Bourouina. Characterization of a DC/DC converter using an in-plane bulk silicon capacitive transducer for vibration-to-electricity power conversion. In *PowerMEMS Workshop on Micro and Nanotechnology for Power Generation and Energy Conversion Applications 2008*, pages 297–300, Sendai, Japan, 2008.

[Paracha09a] A. M. Paracha. *Conception et réalisation d'un micro-système pour la récupération de l'énergie vibratoire du milieu ambiant par transduction électrostatique*. PhD thesis, Université PARIS-EST, 2009.

[Paracha09b] A. M. Paracha, P. Basset, D. Galayko, F. Marty, and T. Bourouina. A silicon MEMS dc/dc converter for autonomous vibration-to-electrical-energy scavenger. *Electron Device Letters, IEEE*, 30(5):481–483, 2009.

[Pêcheux05] F. Pêcheux, C. Lallement, and A. Vachoux. VHDL-AMS and Verilog-AMS as alternative hardware description languages for efficient modeling of multidiscipline systems. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and System*, 24(2):204–225, 2005.

[Pillatsch13] P. Pillatsch, E. M. Yeatman, and A. S. Holmes. Real World Testing Of A Piezoelectric Rotational Energy Harvester For Human Motion. In *PowerMEMS*, pages 42–46, London, UK, 2013.

[Prasad05] D. K. Prasad and M. Snow. *Designing with solar power: a source book for building integrated photovoltaics (BiPV)*. Images Publishing, 2005.

[Rabaey00] J.M. Rabaey, M.J. Ammer, Jr. da Silva, J.L., D. Patel, and S. Roundy. PicoRadio Supports Ad Hoc Ultra-Low Power Wireless Networking. *Computer*, 33(7):42–48, 2000.

[Rao13] Y. Rao, S. Cheng, and D. P. Arnold. An energy harvesting system for passively generating power from human activities. *Journal of Micromechanics and Microengineering*, 23(11):114012, November 2013.

[Roen77] S. A. Roen. Solar powered portable calculator, 1977.

[Rossi07] C. Rossi, C. Galup-Montoro, and M. C. Schneider. PTAT Voltage Generator based on an MOS Voltage Divider. In *Technical Proceedings of the 2007 NSTI Nanotechnology Conference and Trade Show*, number 4, pages 625–628, Santa Clara, CA, USA, 2007.

[Roundy02] S. Roundy, P. K. Wright, and K. S. J. Pister. Micro-electrostatic vibration-to-electricity converters. In *ASME International Mechanical Engineering Congress & Exposition*, pages 1–10, New Orleans, Louisiana, USA, 2002.

[Roundy03a] S. Roundy. *Energy scavenging for wireless sensor nodes with a focus on vibration to electricity conversion*. PhD thesis, University of California, 2003.

[Roundy03b] S. Roundy, P. K. Wright, and J. Rabaey. A study of low level vibrations as a power source for wireless sensor nodes. *Computer Communications*, 26(11):1131–1144, July 2003.

[Roundy04a] S. Roundy, D. Steingart, L. Frechette, P. Wright, and J. Rabaye. Power Sources for Wireless Sensor Networks. In *1st European Wireless Sensor Networks Workshop*, pages 1–17, 2004.

[Roundy04b] S. Roundy, P. K. Wright, and J. M. Rabaey. Energy Scavenging for Wireless Sensor Networks: With Special Focus on Vibrations. *International Journal of Distributed Sensor Networks*, 2(2), 2004.

[Safa09] K. Safa. *Optoelectronics And Photonics: Principles And Practices (With Cd)*. Pearson Education, 2009.

[Saha08] C. R. Saha, T. O'Donnell, N. Wang, and P. McCloskey. Electromagnetic generator for harvesting energy from human motion. *Sensors and Actuators A: Physical*, 147(1):248–253, 2008.

[Sari10] I. Sari, T. Balkan, and H. Kulah. An Electromagnetic Micro Power Generator for Low Frequency Environmental Vibrations based on the Frequency Up-Conversion Technique, 2010.

[Scott03] M. D. Scott, B. E. Boser, and K. S. J. Pister. An ultra low-energy adc for smart dust. *IEEE Journal of Solid-State Circuits*, 2003.

[Shen08] D. Shen, J.-H. Park, J. Ajitsaria, S.-Y. Choe, H. C. Wikle, and D.-J. Kim. The design, fabrication and evaluation of a MEMS PZT cantilever with an integrated Si proof mass for vibration energy harvesting. *Journal of Micromechanics and Microengineering*, 18(5):055017 (7pp), May 2008.

[Shenck01] N. S. Shenck and J. A. Paradiso. Energy scavenging with shoe-mounted piezoelectrics. *Micro, IEEE*, 21(3):30–42, 2001.

[Shenghua07] Z. Shenghua and W. Nanjian. A novel ultra low power temperature sensor for UHF RFID tag chip. In *Proc. IEEE Asian Solid-State Circuits Conf.*, pages 464–467, 2007.

[Sodano04] H. A. Sodano, D. J. Inman, and G. Park. A Review of Power Harvesting from Vibration Using Piezoelectric Materials. *The Shock and Vibration Digest*, 36(3):197–205, May 2004.

[Sodano05] H. A. Sodano, D. J. Inman, and G. Park. Comparison of Piezoelectric Energy Harvesting Devices for Recharging Batteries. *Journal of Intelligent Material Systems and Structures*, 16(10):799–807, 2005.

[Soliman08] M. S. M. Soliman, E. M. Abdel-Rahman, E. F. El-Saadany, and R. R. Mansour. A wideband vibration-based energy harvester. *Journal of Micromechanics and Microengineering*, 18(11):115021, November 2008.

[Starner03] T. E. Starner. Powerful change part 1: batteries and possible alternatives for the mobile market. *Pervasive Computing, IEEE*, 2(4):86–88, 2003.

[Sterken07] T. Sterken, P. Fiorini, G. Altena, C. Van Hoof, and R. Puers. Harvesting energy from vibrations by a micromachined electret generator. In *Solid-State Sensors, Actuators and Microsystems Conference, 2007. TRANSDUCERS 2007. International*, pages 129–132. IEEE, 2007.

[Stordeur97] M. Stordeur and I. Stark. Low power thermoelectric generator-self-sufficient energy supply for micro systems. In *Thermoelectrics, 1997. Proceedings ICT '97. XVI International Conference on*, pages 575–577, 1997.

[Sun08] J. Sun, M. Xu, D. Reusch, and F. C. Lee. High efficiency quasi-parallel Voltage Regulators. In *High efficiency quasi-parallel Voltage Regulators*, pages 811–817, 2008.

[Suzuki10] Y. Suzuki, D. Miki, M. Edamoto, and M. Honzumi. A MEMS electret generator with electrostatic levitation for vibration-driven energy-harvesting applications. *Journal of Micromechanics and Microengineering*, 20(10):104002 (8pp), October 2010.

[Szarka12] G. D. Szarka, B. H. Stark, and S. G. Burrow. Review of Power Conditioning for Kinetic Energy Harvesting Systems. *IEEE TRANSACTIONS ON POWER ELECTRONICS*, 27(2):803–815, 2012.

[Szollosy10] J. G. Szollosy. *Integrated switches for implantable medical devices, in HV-MOS technology.* PhD thesis, Universidad Catolica del Uruguay, 2010.

[Tan02] S. C. Tan and X. W. Sun. Low power CMOS level shifters by bootstrapping technique. *Electronics Letters*, 38(16):876–878, 2002.

[Taneja08] J. Taneja, J. Jeong, and D. Culler. Design, Modeling, and Capacity Planning for Micro-solar Power Sensor Networks. *2008 International Conference on Information Processing in Sensor Networks (ipsn 2008)*, pages 407–418, April 2008.

[Tashiro02] R. Tashiro, N. Kabei, K. Katayama, E. Tsuboi, and K. Tsuchiya. Development of an electrostatic generator for a cardiac pacemaker that harnesses the ventricular wall motion. *Journal of Artificial Organs*, 5(4):239–245, December 2002.

[Toriyama01] T. Toriyama, M. Yajima, and S. Sugiyama. Thermoelectric micro power generator utilizing self-standing polysilicon-metal thermopile. In *Micro Electro Mechanical Systems, 2001. MEMS 2001. The 14th IEEE International Conference on*, pages 562–565, 2001.

[Torres05] E. O. Torres and G. A. Rincón-Mora. Long-lasting, self-sustaining, and energy-harvesting system-in-package (SiP) wireless micro-sensor solution. In *International Conference on Energy, Environment and Disasters (INCEED 2005)*, pages 1–33, 2005.

[Torres06] E. O. Torres and G. A. Rincón-Mora. Electrostatic energy harvester and Li-Ion charger circuit for micro-scale applications. In *49th IEEE International Midwest Symposium on Circuits and Systems, 2006. MWSCAS'06.*, pages 65–69, Puerto Rico, 2006.

[Torres09] E. O. Torres and G. A. Rincón-Mora. Electrostatic energy-harvesting and battery-charging CMOS system prototype. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 56(9):1938–1948, 2009.

[Torres10] E. O. Torres and G. A. Rincón-Mora. A 0.7-um BiCMOS Electrostatic Energy-Harvesting System IC. *IEEE Journal of Solid-State Circuits*, 45(2):483–496, 2010.

[Tos] http://www.toshiba.com/taec/news/press_releases/2009/dmfc_09_580.jsp.

[Vittoz79] E.A. Vittoz and O. Neyroud. A low-voltage CMOS bandgap reference. *Solid-State Circuits, IEEE Journal of*, 14(3):573–579, 1979.

[Vullers09] R. J. M. Vullers, R. Van Schaijk, I. Doms, C. Van Hoof, and R. Mertens. Micropower energy harvesting. *Solid-State Electronics*, 53(7):684–693, July 2009.

[Wang07] Z. Wang, V. Leonov, P. Fiorini, and C. Van Hoof. Micromachined Thermopiles for Energy Scavenging on Human Body. In *Solid-State Sensors, Actuators and Microsystems Conference, 2007. TRANSDUCERS 2007. International*, pages 911–914, 2007.

[Wang08] Z. Wang, P. Fiorini, V. Leonov, and C. Van Hoof. Characterization Of Poly-Si\70% Ge\30% for Surface Micromachined Thermopiles. In *Proceedings of PowerMEMS*, pages 23–26, Sendai, Japan, 2008.

[Warnick84] C. C. Warnick. Hydropower engineering, 1984.

[Williams01] C. B. Williams, C. Shearwood, M. A. Harradine, P. H. Mellor, T. S. Birch, and R. B. Yates. Development of an electromagnetic micro-generator. *Circuits, Devices and Systems, IEEE Proceedings* -, 148(6):337–342, 2001.

[Yamashita10] K. Yamashita, M. Honzumi, K. Hagiwara, Y. Iguchi, and Y. Suzuki. Vibration-driven MEMS energy harvester with vertical electrets. In *10th Int. Workshop Micro and Nano-technology for Power Generation and Energy Conversion Applications (PowerMEMS 2010)*, 2010.

[Yang13] M.-Z. Yang, C.-C. Wu, C.-L. Dai, and W.-J. Tsai. Energy harvesting thermoelectric generators manufactured using the complementary metal oxide semiconductor process. *Sensors (Basel, Switzerland)*, 13(2):2359–2367, January 2013.

[Yen06] B. C. Yen and J. H. Lang. A Variable-Capacitance Vibration-to-Electric Energy Harvester. *IEEE Transaction on Circuits and Systems–I: Regular papers IEEE*, 53(2):288–295, 2006.

[Zelenay04] P. Zelenay and P. Piela. Researchers redefine the DMFC roadmap. *The Fuel Cell Rewiew*, 1(2):17–24, 2004.

List of publications

[1] A. M. Paracha, P. Basset, D. Galayko, F. Marty, A. Dudka and T. Bourouina, "Characterization of a DC/DC converter using an in-plane bulk-silicon capacitive transducer for vibration-to-electricity power conversion", *Proceeding of PowerMEMS conference*, Sendai, Japan, 2008.

[2] A. M. Paracha, P. Basset, D. Galayko, A. Dudka, F. Marty and T. Bourouina, "MEMS DC/DC converter for 1D and 2D vibration-to-electricity power conversion", *Proceeding of Transducers conference*, Denver, CO, USA, 2009.

[3] A. Dudka, D. Galayko and P. Basset, "VHDL-AMS modeling of adaptive electrostatic harvester of vibration energy with dual-output DC-DC converter", *Proceeding of IEEE BMAS conference*, San José, CA, USA, 2009.

[4] A. Dudka, D. Galayko and P. Basset, "Smart adaptive power management in electrostatic harvesters of vibration energy", *Proceeding of PowerMEMS conference*, Washington DC, USA, 2009.

[5] P. Basset, D. Galayko, A. Mahmood Paracha, F. Marty, A. Dudka and T. Bourouina, "A batch-fabricated and electret-free silicon electrostatic vibration energy harvester", *Journal of Micromechanics and Microengineering*, 19, 115025 (12pp), 2009.

[6] R. Khalil, A. Dudka, D. Galayko, R. Iskander and P. Basset, "Design and modeling of a successive approximation ADC for the electrostatic harvester of vibration energy", *Proceeding of IEEE BMAS conference*, San José, CA, USA, 2010.

[7] R. Khalil, A. Dudka, D. Galayko and P. Basset, "High-voltage low power analogue-to-digital conversion for adaptive architectures of capacitive vibration energy harvesters", *Proceeding of PowerMEMS conference*, Leuven, Belgium , 2010.

[8] D. Galayko, R. Guillemet, A. Dudka, P. Basset, "Comprehensive dynamic and stability analysis of electrostatic Vibration Energy Harvester (e-VEH)", *Proceeding of Transducers conference*, Beijing, China, 2011.

[9] A. Dudka, D. Galayko, P. Basset, "Design of controller IC for asynchronous conditioning circuit of an electrostatic vibration energy harvester", *IEEE Workshop of Energy and Wireless Sensors (e-Wise)*, Besançon, France, 2012.

[10] A. Dudka, D. Galayko, P. Basset, "IC design of an adaptive high-voltage electrostatic vibration energy harvester", *Proceeding of DTIP conference*, Barcelona, Spain, 2013.

[11] A. Dudka, P. Basset, F. Cottone, E. Blokhina and D. Galayko, "Wideband electrostatic Vibration Energy Harvester having a low start-up voltage employing a high-voltage integrated interface", *Proceeding of PowerMEMS conference*, London, UK, 2013.

[12] D. Galayko, E. Blokhina, P. Basset, F. Cottone, A. Dudka, E. O'Riordan and O. Feely, "Tools for Analytical and Numerical Analysis of Electrostatic Vibration Energy Harvesters: Application to a Continuous Mode Conditioning Circuit", *Proceeding of PowerMEMS conference*, London, UK, 2013.

[13] A. Dudka, D. Galayko, E. Blokhina, and P. Basset, "Smart integrated conditioning electronics for electrostatic vibration energy harvesters", *Proceeding of IEEE ISCAS conference*, Melbourne, Australia, 2014 – accepted for a special session.