Chapter III

Passive Elements Modeling and Design

III.1 Introduction

Modeling of three dimensional passive elements and parasitic effects in back-end-process layers of technology is an important issue in mm-wave design. This issue consists of transmission lines, inductors, capacitors, RF pads and interconnections modeling. Accurate modeling is necessary not only for design and optimization of passive elements, but also for analysis and simulation of designed or implemented passive elements and parasitic effects. Although full wave electromagnetic simulation is the most accurate solution in analysis of such three dimensional elements, most of the times, the required simulation time or processing capability is so high that makes this method inefficient in many cases, specially in design and optimization of passive elements. Nevertheless, full wave electromagnetic solvers can be used in final simulation and evaluation steps.

The trend toward integrating various design level of communication systems in a single design and simulation frame work has been leads to new software's and design tools, aiming to offer device level and passive elements design and modeling, circuit level simulation, and system level optimizations facilities in a single design environment. Agilent Advanced Design System (ADS) and Ansoft Designer/Nexxim are two samples of such software's. In addition some of commercial circuit simulators, such as Spectre-RF, have used simple models for transmission lines or some other passive elements.

We started passive elements design in our work using ADS. ADS provides two solutions for design, simulation and optimization of 3-D structures, frequently encountered in RF circuit design. One solution uses 2-dimensinal electromagnetic field solver that is useful in simulation of the structures in which the wave propagation is in TEM or Quasi-TEM mode. The second solution is quasi 3-dimensional (2.5-dimesional) electromagnetic field solver, using MoM[1] technique. The former is run in a schematic circuit representation environment, but the later has a quasi 3-dimentional layout rendering tool, in which 3-dimensional structures are rendered as multi-layer objects. The details will be described later. In continue we developed a simple design tool for modeling, analysis and synthesis of our required passive elements. Then we used ADS MoM simulator to extract model parameters and evaluating the designs. In progress, we encountered with some essential limitations in 2.5-dimensional electromagnetic simulators and hence we switched to full wave electromagnetic field solvers to achieve higher accuracy and more reliable results.

III.2 Inductor Design

Inductors are the most important passive elements that are frequently used in RF and microwave integrated circuits. In old technologies, inductors were designed as off-chip components. More than ten years ago, tremendous advances in CMOS technologies incline RFIC designer toward System-on-Chip (SoC) implementation, by which the excellent potential of CMOS technology for digital circuits could be combined with CMOS RF blocks, to produce low-cost, high performance fully integrated systems. In this way there was an important bottleneck: on-chip inductor fabrication. In old technologies, the parasitic capacitance of MOS transistor was so high that compensating them in amplifiers in about 1GHz frequency, was needed to an inductance as high as 100nH [1]. The first successful

[1] Method-of-Momentum

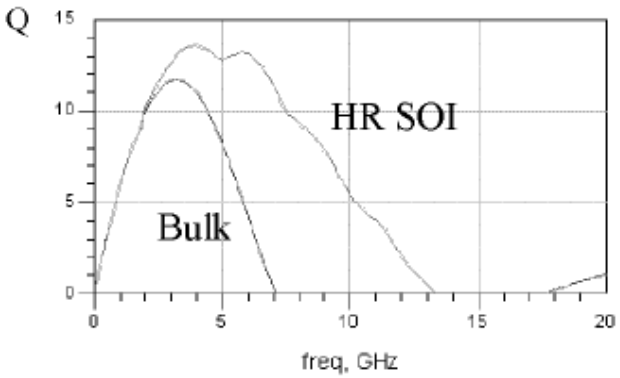


Fig. III-1. Quality factor of 3.4nH inductor in bulk CMOS and High Resistivity (HR) SOI CMOS, optimized for 2.4 GHz [4].

attempts in this way, was reported by Abidi et *al*. in 1993, where they fabricated a 100nH suspended inductor in 2um CMOS technology [2]. Then they renewed their technique in 1960, in design of a 50nH suspended inductor for a 1GHz front end [3]. In recent years, on-chip spiral inductors is widely used in CMOS RFIC's. Quality factor more than 10 and 13 is well achievable in bulk CMOS and SOI CMOS technologies, respectively (see Fig. III-1) [4], [5].

Nevertheless, special post processing techniques have been developed to fabricate inductors with higher quality factor, in design of high performance RF circuits in CMOS technologies. In CMOS technologies, substrate loss is the main reason of quality factor degradation of on-chip inductors [1]. Consequently some CMOS compatible, post-processing technologies have been adopted to reduce the substrate losses.

Using thin film Wafer Level Packaging (WLP) post-processed technique on standard CMOS technology, quality factors up to 35 have been obtained for nano-henry range inductors in few GHz [6], [7], [8], [4]. In this technology, dielectric and metal layers are deposited on the passivation layer, above the standard CMOS wafer. CMOS compatible backside Inductively Coupled Plasma (ICP) dry etching technology is another technology that have been used in recent years to improve the inductors quality factor [9],[10]. In this technology the lossy substrate beneath the inductor is etched and the inductor is suspended in air. CMOS compatible MEMS[1] technology is another way to fabricate high quality large inductors. Fig. III-2 shows a 6.75nH suspended inductor, fabricated in MEMS technology [11]. Embedding the inductors in low cost package has been used in [12] and 7nH inductor with Q grater than 50 has been designed.

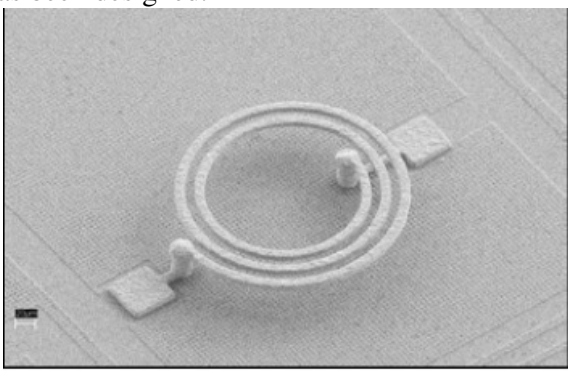


Fig. III-2. 6.75nH high Q spiral inductor, fabricated using CMOS compatible MEMS technology [11]

[1] Micro Electro Mechanical Systems

Post processed technologies are expensive and hence are not suitable for low cost applications, such as wireless network sensor nodes, in which a huge number of sensor nodes is required. Some design techniques have also been addressed to improve the on chip inductors quality factor. [13], [14].

III.2.1 Inductors in mm-wave Band

In mm-wave frequencies there is different condition in designing matching networks. The required inductance is very small and this facilitates the inductor fabrication. On the other hand various coupling and parasitic effects increases and this causes serious problems in design and modelling and degrades the quality factor.

Transmission lines have been widely used in old RFICs and MMICs in various technologies. Designing matching networks with transmission lines requires high chip area and hence in recent years the trend is to use lumped passive elements or combination of lumped and distributed elements in matching network design [5], [15], [16].

Spiral inductors have been used successfully in CMOS mm-wave circuits, in frequencies up to 60 GHz [17], [18]. Unlike the transmission lines that can be modelled accurately and can be designed easily, spiral inductors in mm-wave band have complicated model and design process. On the other hand the inductors in mm-wave frequencies are very small and hence can be designed as small short end transmission line. *Here after we denote the short-end transmission line inductors as line-type inductors.* Using a combination of lumped capacitors and line-type inductors are a good solution to achieve small area, meanwhile preserve the benefit of easy design and modelling process of transmission lines, instead of spiral inductors [19], [20]. Nonetheless some recent reports show the advantages of spiral inductors over combined matching in mm-wave band [15], [17].

Two types of line-type inductors have been used in reported works: Coplanar line [19], [5] and microstrip line [20], [21]. Razavi has designed a folded microstrip line-type inductor for 60 GHz application in 0.13um CMOS technology [21]. Field distribution of these structures have been depicted in Fig. III-3. Wave propagation is in TEM or Quasi-TEM mode, i.e. electric and magnetic field vectors does not have any component parallel to the line length.

required for a given inductance. Increasing the line length, not only increases the inductors area, but also degrades the inductors quality factor. In contrast, in coplanar structure the line inductance increases with increasing the space between centerline and ground strips. Consequently in comparison with microstrip structure, larger inductance can be obtained with a given line length. Unfortunately in high impedance coplanar structures, fabricated in CMOS technology, the substrate losses increases and degrades the quality factor.

III.2.2 Proposed Inductor Structure

For better describing the structure of our inductors, a simple representation of the simplified layer stack of STMicroelectronics 90nm CMOS technology, has been shown in Fig. III-4. The technology provides 5 thin metal layers and 2 thick metal (Cu) layers. In addition an extra aluminum layer is deposited above the top most Cu metal layer, to encapsulate the chip, named ALUCAP. This layer can also be used for routing metal lines. Three different implementation of inductor metal lines have been shown in Fig. III-5. As analyzed in the next sections, the structure in Fig. III-5(a) has small height and low conduction. The structure in Fig. III-5(b) has big height and low conduction. The inductor fabricated with this line structure will have high self resonance frequency and hence is useful in higher frequencies. The structure in Fig. III-5(c) has small height and high conduction. This structure leads to higher quality factor in lower frequencies of mm-wave band. As will be shown by analysis, the line structure in Fig. III-5(c) is the best choice for Ka band (26.5-40GHz).

Although some recently published works have claimed the advantage of spiral inductors against line-type inductors [5], [15], we used a new structure for line-type inductors that contains the advantages of both of coplanar and microstrip lines and eliminates their disadvantages. As explained, microstrip line has low inductance that leads to very long line and low self resonance frequency and coplanar line causes high substrate loss that lowers the quality factor. Thanks with the new structure, we found using lumped elements with line-type inductor structure is the best choice for our work. Note that the inductor structure (spiral

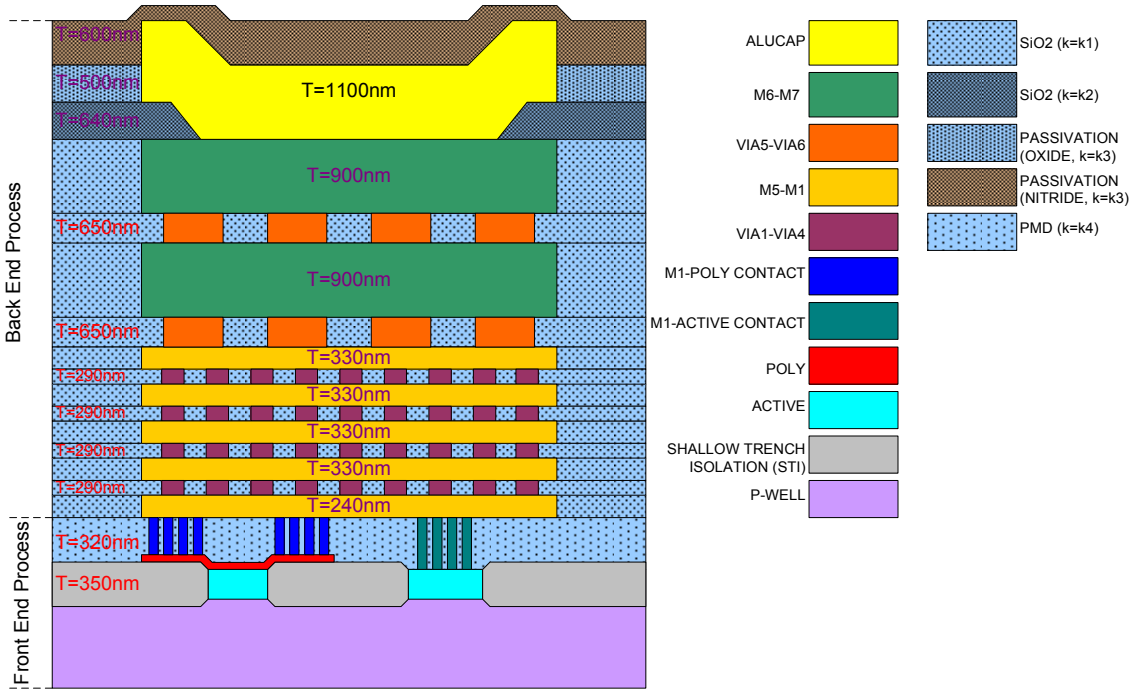


Fig. III-4. The simplified layer stack of STMicroelectronics 90nm CMOS technology [25]

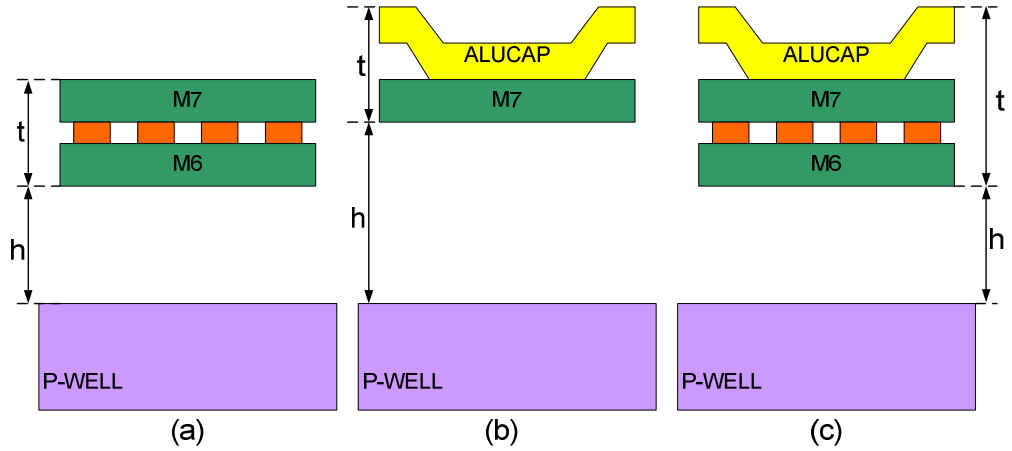


Fig. III-5. Three different line structure for inductors

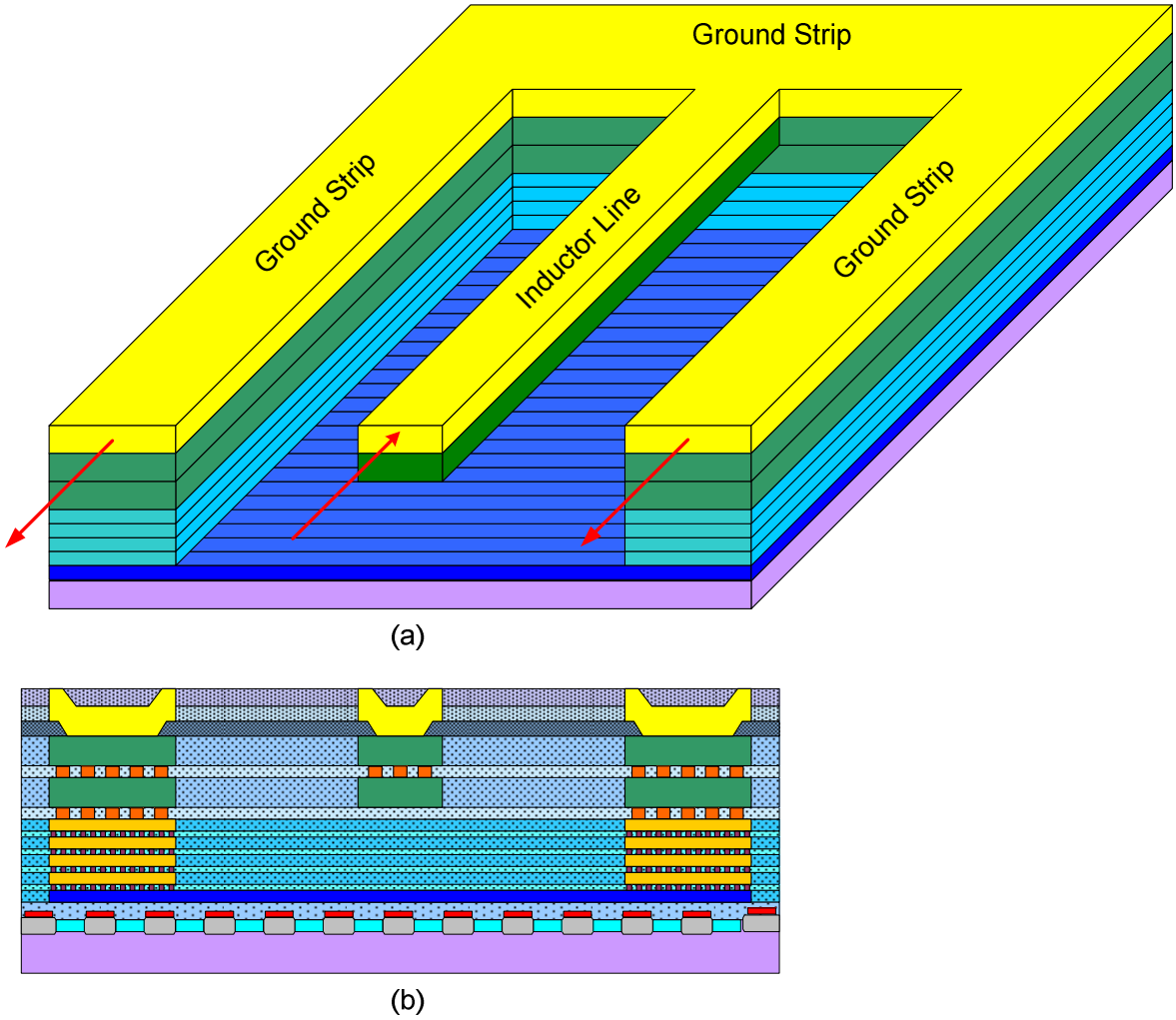


Fig. III-6. Simplified 3-dimensional view (a) and accurate cross section (b) of the line-type inductor structure, proposed in our work. The inductor is fabricated as a short-end transmission line with patterned shield layer.

or line-type) greatly depends on the inductance value and line-type is suitable for inductors as small as few hundreds pico-henry.

Our line-type inductor structure has been shown in Fig. III-6. This inductor is short-end transmission line section and is used as a shunt inductor (grounded in one terminal). Actually the inductance is obtained from the magnetic field around the centerline of Fig. III-6.

The proposed line-type inductor is not a coplanar, as in [19], and not microstrip, as in [20]. The inductor structure is composed of sidewall ground strips, the inductor centerline and patterned shield layer, designed beneath the centerline. The shield layer prevents the electric field to penetrate in the lossy substrate, as in conventional microstrip lines, but in contrast to the microstrip lines magnetic field penetrates into the substrate. This increases the line inductance, without substrate loss due to the electric field coupling to the substrate. Electric and magnetic field pattern of the proposed structure, in Quasi-TEM region (sufficiently far from short end) has been shown in Fig. III-7. Comparison of this figure with Fig. III-3 reveals the difference between conventional line structure and proposed structure.

III.2.3 Inductor Model Development

The inductor can be divided into two sections: one is the section in which the Quasi-TEM assumption is valid, and the other is the section of the inductor near to the short-end. In this region the inductor geometry has sharp variation and hence the electric field distribution deviates from planar wave model. Fig. III-8 shows the electric field pattern in the Quasi-TEM and Non-Quasi-TEM regions. This figure has been obtained based on simulation in Ansoft HFSS full wave electromagnetic solver. However the magnetic field does not significantly change in this region. Based on our simulations, as in this Fig. III-8, the length of the short-end region extends up to the distance between the centerline and the ground sidewall, i.e. S in Fig. III-8. It must be noted that in CMOS technology, due to lossy substrate, the penetration of the electric field in the substrate is small and this causes slow wave condition in which the Quasi-TEM assumption is more accurate [26]. Specially when shield layer is used, the slow wave condition is more confirmed.

Based on the above explanation, we have developed our line-type inductor model, as shown in Fig. III-9. The inductor model is composed of two sections: one for the Quasi-TEM region and the other for short-end region. Quasi-TEM region has been modelled as a lumped scalable RLGC model, as shown in Fig. III-9(b). Model elements in this figure are calculated by scaling the per-unit values of the elements with respect to the length the Quasi-TEM section, denoted as a in Fig. III-9(b). To extract the standard RLGC model elements, a deep physical based view of the inductor structure is necessary. For this purpose we have developed more physical and complicated model, shown in Fig. III-10. Unlike the standard

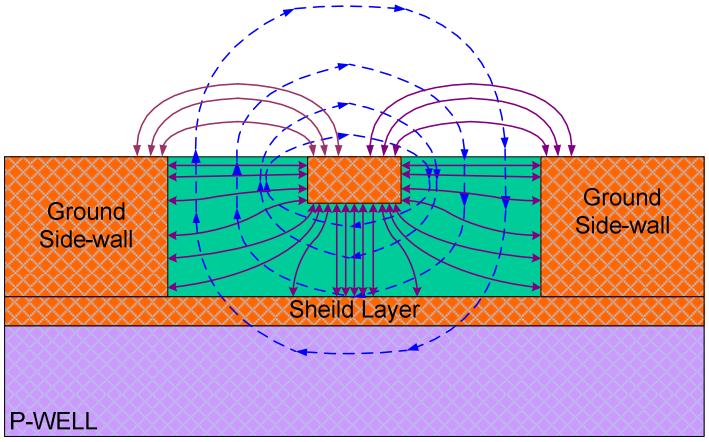


Fig. III-7. Field pattern of proposed inductor structure in Quasi-TEM region

RLGC model, per-unit length value of elements of Fig. III-10 can be calculated using analytic approach. Actually each element reflects a physical effect, as described in the next section.

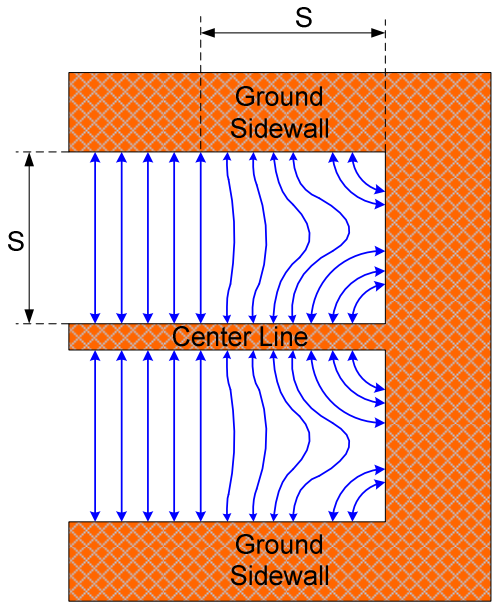


Fig. III-8. Electric field distribution in the vicinity of the short-end, obtained from full wave simulation in Ansoft HFSS

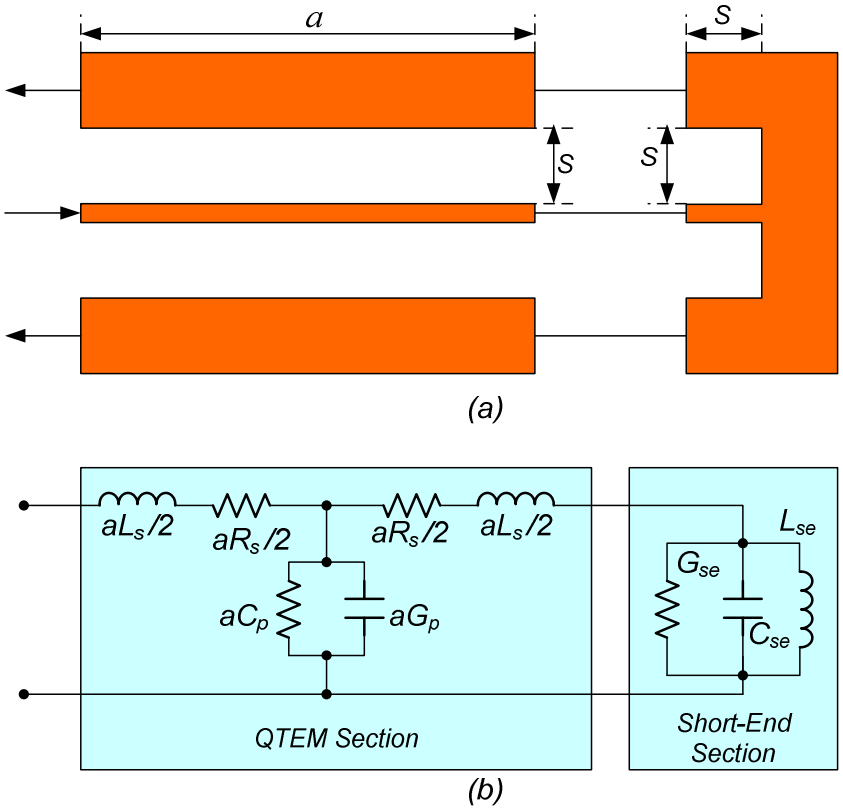


Fig. III-9. Proposed model for line-type inductor: dividing the inductor to two sections (a), and RLGC scalable model of QTEM section and RLC model of short-end section (b)

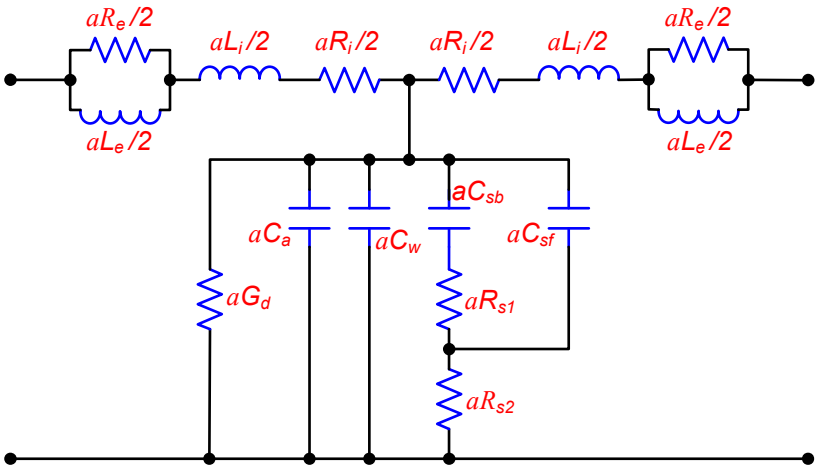


Fig. III-10. Accurate lumped element scalable model of QTEM section

III.2.3.1 Analytic Calculation of Model Elements

A) Inductance and Resistances in Lateral Branches

L_e is the centerline external inductance that is due to the magnetic flux outside the centerline conductor and L_i is the internal inductance, due to the magnetic flux inside the centerline conductor. R_i represents the resistive losses in the centerline conductor and its value is directly related to the reactance of the internal inductance [27]. For an ideal conductor the centerline current flows only in the conductor surface (zero skin dept) and so there is not any magnetic flux inside the centerline and both of R_i and L_i are zero. However in the case of finite conductance, centerline current flows inside the conductor, but crowded toward the conductors outer surface. This current crowding is a frequency-dependent phenomenon and is expressed by the conductor skin dept. Due to this frequency dependency L_i and R_i are frequency dependent parameters.

The internal and external inductances have been calculated in some reports [27], [28], using quasi-static analysis and conformal mapping. We found the analysis in [27] more accurate for our work and we use it with proper fitting parameter, to calculate L_i, L_e and R_i as follows:

$$L_e = \frac{\mu_0}{4F \cdot t_c / 2}$$

$$L_i = \sqrt{\frac{\mu_0}{2\omega\sigma_c}} \frac{F_L^c + F_L^g}{4F^2 \cdot t_c / 2} \qquad \text{(III-1)}$$

$$R_i = L_i \omega$$

F, F_L^c and F_L^g are complicated functions of inductor geometry and technology parameters and have been defined in [27]. t_c is the centerline thickness. ω is the working angular frequency, σ_c is the centerline conductivity and μ_0 is the magnetic permeability of free space.

Eddy current loss has great influence on the quality factor of inductors and has been analyzed and modelled in many works in the case of spiral inductors [29], [30], [31]. In line-type inductor, magnetic coupling between the centerline and the low resistivity substrate causes eddy currents in the P-WELL, beneath the Shallow Trench Isolation (STI) layer in longitudinal direction. These currents cause additional losses in the substrate. In the scalable model of Fig. III-10, the eddy loss has been modelled as a resistance (R_e) parallel with the external inductance. To develop a simple model to capture the eddy loss, consider Fig. III-

11(a). Induced current flows in opposite direction of the current in the centerline. If the line length is very small in comparison with the wave length (otherwise long line should be broken into cascades small lines), current density can be assumed to be uniform in longitude direction. However the current density is not uniform in traverse direction, as depicted in Fig. III-11(a). The current induced in the substrate can be modelled as a mutual inductance between the centerline and the substrate, as shown in Fig. III-11(b). Then this simple circuit can be more simplified as a single resistance, parallel with L_e in Fig. III-11(c). Intuitively we can calculate R_{eddy} in Fig. III-11(b) as follows:

$$R_{eddy} = \frac{k\rho_{sub}a}{2S+W} \tag{III-2}$$

a is the line length, S is the space of the centerline and the ground sidewall and W is the centerline width. k is a coefficient to account for the non-uniform eddy current distribution in substrate and ρ_{sub} is the under STI p-well substrate sheet resistance. We define the quality factor due to the eddy loss as:

$$Q_{eddy} = \frac{E_{stored}}{E_{loss\_eddy}} \tag{III-3}$$

in which E_{stored} is the energy stored in the magnetic field and E_{loss_eddy} is the energy loss due to the eddy current. Assuming that the induced current has not significant reverse effect on the main current, we deduce:

$$Q_{eddy} = \frac{R_{eddy}L_e}{2\pi M_{cs}^2\omega} \tag{III-4}$$

L_e is the line external inductance, ω is the working frequency and M_{cs} is the mutual inductance between the centerline and the substrate. On the other hand, since R_e parallel with L_e in Fig. III-10 models the eddy loss, the quality factor of L_e in this figure, defined as:

$$Q_{Le} = \frac{R_e}{L_e\omega} \tag{III-5}$$

should be equal to the quality factor in (III-4). So we simply deduce:

$$R_e = \frac{kaL_e^2}{2\pi M_{cs}^2(2S+W)} \tag{III-6}$$

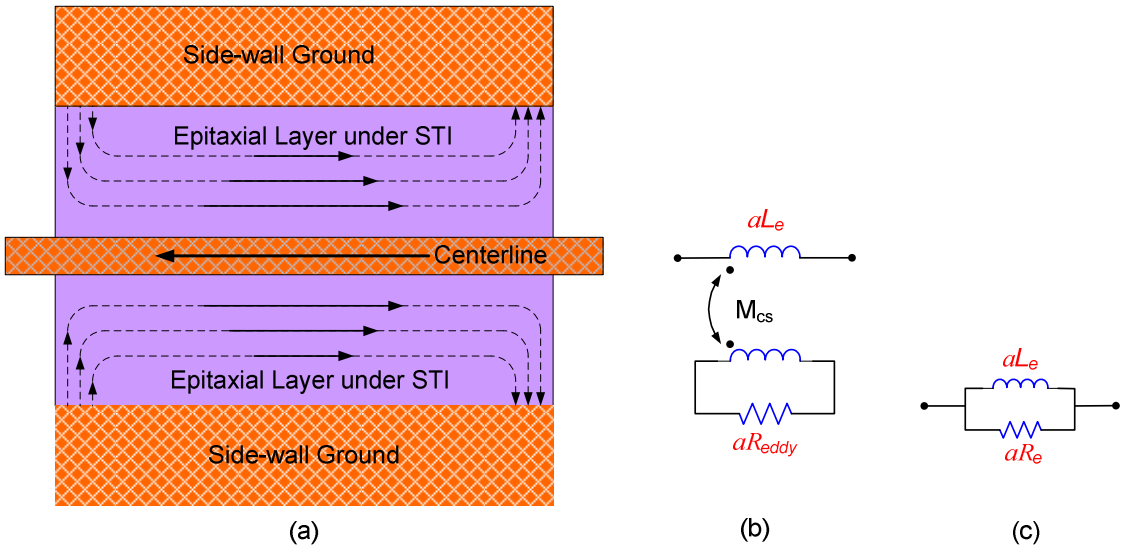


Fig. III-11. Modeling the loss due to the eddy currents in the substrate: (a) eddy currents representation, (b) equivalent circuit model and (c) simplified circuit model

where a is the centerline length and M_{cs} is the mutual inductance of the centerline and the substrate. k is a coefficient to account for the non-uniform eddy current distribution in substrate.

Accurate calculation of M_{cs} is very complicated, but we have derived a simple analytic equation to calculate its approximated value. The basis of our approach has been shown in Fig. III-12, in which the magnetic flux lines have been assumed to be perfect circles in the area between the centerline and ground sidewall. This assumption is valid when S is large and the centerline has square cross section. By this assumption, magnetic flux density at point (x , h) on the p-well surface can be calculated easily using Ampere's low:

$$\vec{B}(x,h)=\frac{\mu I}{2\pi\cdot r}\vec{k} \tag{III-7}$$

Where k is the unit vector in the flux direction and r is the radius of flux circle passing through the point (x , h). Using Fig. III-12, the component of the flux vector normal to the p-well surface is obtained:

$$\vec{B}_n(x,h)=\vec{B}(x,h)\frac{x}{r}=\frac{\mu I x}{2\pi\cdot r^2}\vec{k} \tag{III-8}$$

Now the total magnetic flux of the centerline per unit length is equal to:

$$\phi=\int_{t_C/2}^{S+t_C/2}\left|\vec{B}(x,h)\right|dr=\frac{\mu I}{2\pi}\int_{t_C/2}^{S+t_C/2}\frac{dr}{r}=\frac{\mu I}{2\pi}\ln\left(\frac{2S}{t_c}+1\right) \tag{III-9}$$

Where t_c is the centerline thickness. The mutual magnetic flux passing into the p-well surface per unit length is equal to:

$$\phi_M=\int_0^X\left|\overrightarrow{B_n}(x,h)\right|dx=\frac{\mu I}{2\pi}\int_0^X\frac{xdx}{x^2+h^2}=\frac{\mu I}{2\pi}\ln\left(\frac{S}{h}\right)\qquad S>h \tag{III-10}$$

On the other hand we have:

$$\frac{M_{cs}}{L_e}=\frac{\phi_M}{\phi} \tag{III-11}$$

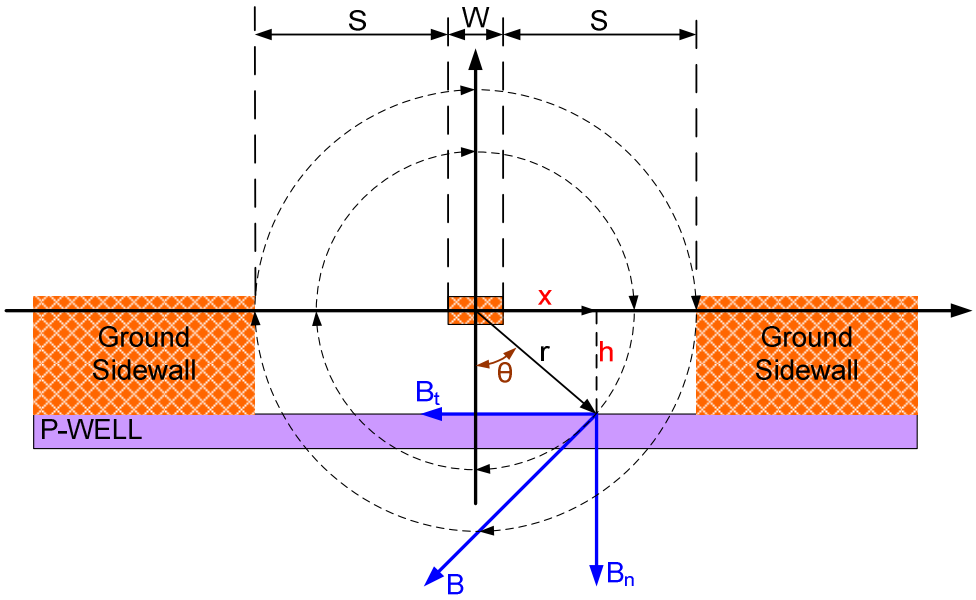


Fig. III-12. Calculation of the magnetic flux passing trough the lossy substrate, assuming that the magnetic field lines are in circular form

where L_e is the per-unit length inductance of the line. So we deduce:

$$M_{cs} = \frac{\ln\left(\frac{S}{h}\right)}{\ln\left(\frac{2S}{t_c}+1\right)} L_e \qquad S > h \qquad \text{(III-12)}$$

S is the space between the centerline and the ground sidewall, W is the centerline width and h is the height of the centerline from lossy substrate and t_c is the centerline thickness.

In deriving the above equation, we assumed square cross section for centerline. However this condition is not valid in all designs and in many cases the line width is larger than the line thickness. In this condition the magnetic flux lines are deviated from circular to parabolic form and hence the flux crossing the p-well surface reduces. To capture this effect, we modify (III-12) as:

$$M_{cs} = \left(\frac{t_c}{W}\right)^q \frac{\ln\left(\frac{S}{h}\right)}{\ln\left(\frac{2S}{t_c}+1\right)} L_e \qquad S > h \qquad \text{(III-13)}$$

q is a fitting parameter. In our design, regarding Fig. III-4 and Fig.III.5 h is equal to 3.8um and t_c is 3.6um. Ration of M_{cs} over L_e as a function of S has been shown in Fig. III-13, for $q=0.5$ and some values of W.

B) Capacitance and Resistances in the Vertical Branch

Capacitances and resistors in the vertical branch of the lunped model of Fig. III-10 have been depicted in Fig. III-12. C_a is the capacitance due to the field coupled from the centerline top surface to the sidewalls top surface, out of the dielectric material in the air. C_w is the capacitance between the centerline and the vertical surface of the ground sidewalls. C_{sb} is the capacitance between the centerline and substrate or shield layer and C_{sf} is the fringing capacitance between the centerline and substrate or shield layer.

Electric coupling between the centerline and the substrate or shield layer causes a current toward the ground sidewall, in the substrate or shield layer. The resistance in the path of this current has been denoted as R_{s1} and R_{s2} in Fig. III-12. The other resistance in this figure is R_d, representing the dielectric loss in the multilayer dielectric stack above the substrate or shield.

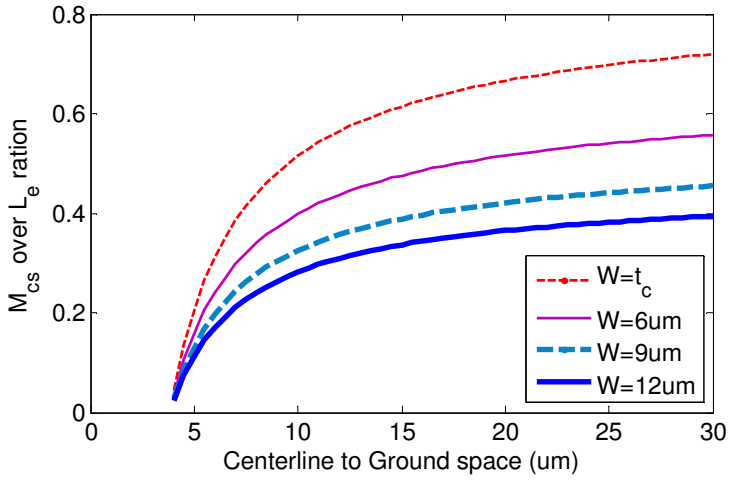


Fig. III-13. Ration of the mutual inductance (M_{cs}) over the line inductance (L_e), calculated using (III-?), for h=3.8um and tc=3.6um

The per-unit length capacitance of a infinite length conductor line with thickness t and width W, placed in the height of h from infinite ground substrate, as shown in Fig. III-13, has been calculated analytically in [32] and has been used in [33] for CPW modeling. The analysis is based on Quasi-TEM and planar wave assumption. The resulted equation comprises the fringing capacitance and is as follows:

$$C_l = \varepsilon_r \varepsilon_0 \left\{ \frac{W}{h} - \frac{t}{2h} + \frac{2\pi}{\ln\left(1 + \frac{2h}{t}\left(1 + \sqrt{1 + t/h}\right)\right)} \right\} \tag{III-14}$$

ε_r is the electrical permittivity of the dielectric material between the line and the substrate. We have used this equation after some modifications, to calculate the capacitance between the centerline and the substrate or shield layer in our model. To explain these modifications consider the electric field profile in Fig. III-13(b), that shows the electric field distribution in the cross section of the line-type inductor. Comparing this figure with Fig. III-13(a) reveals that in Fig. III-13(b) some of the electric field lines have terminated to the ground sidewall. Consequently it is expected that the capacitance between the center line and the substrate in Fig. III-13(b)is smaller than that of Fig. III-13(a). The difference between these capacitors depends on the distance between the centerline and the ground sidewall. Experimentally we have modified (III-14) as below to incorporate the effect of the centerline to sidewall distance:

$$C_{sf} = \frac{\varepsilon_{eff} S}{\sqrt{S^{2.} + S_0^2}} \left\{ \frac{2\pi}{\ln\left(1 + \frac{2h}{t_c}\left(1 + \sqrt{1 + t_c/h}\right)\right)} - \frac{t_c}{2h} \right\} \tag{III-15}$$

$$C_{sb} = \varepsilon_{eff} \frac{W}{h}$$

Where h is the distance between bottom surface of the centerline and top of the poly silicon shield layer or top of the p-well under Shallow Trench Isolation (STI) layer. S_0 is a model parameter and was chosen 20um in our case. ε_{eff} is the effective dielectric constant for the dielectric layer stack above the substrate or shield layer and is calculated as:

$$\varepsilon_{eff} = \frac{h}{\sum_{i=1}^{N_L} \frac{t_i}{\varepsilon_i}} \tag{III-16}$$

where t_i and ε_i are the thickness and dielectric constant of i^{th} dielectric layer and N_L is the number of dielectric layers between centerline and the substrate or shield layer.

The capacitance due to the electrical field in the air, above the inductor structure, denoted as C_a in Fig. III-12(a), is calculated from [34] as follows:

$$C_a = 2\varepsilon_0 \frac{K(k)}{K(k')} \tag{III-17}$$

K denotes complete elliptic integral of the first kind and k is obtained from:

$$k = \frac{W}{W + 2S} \sqrt{\frac{1 - \left(\frac{W + 2S}{W + 2S + 2W_g}\right)^2}{1 - \left(\frac{W}{W + 2S + 2W_g}\right)^2}} \tag{III-18}$$

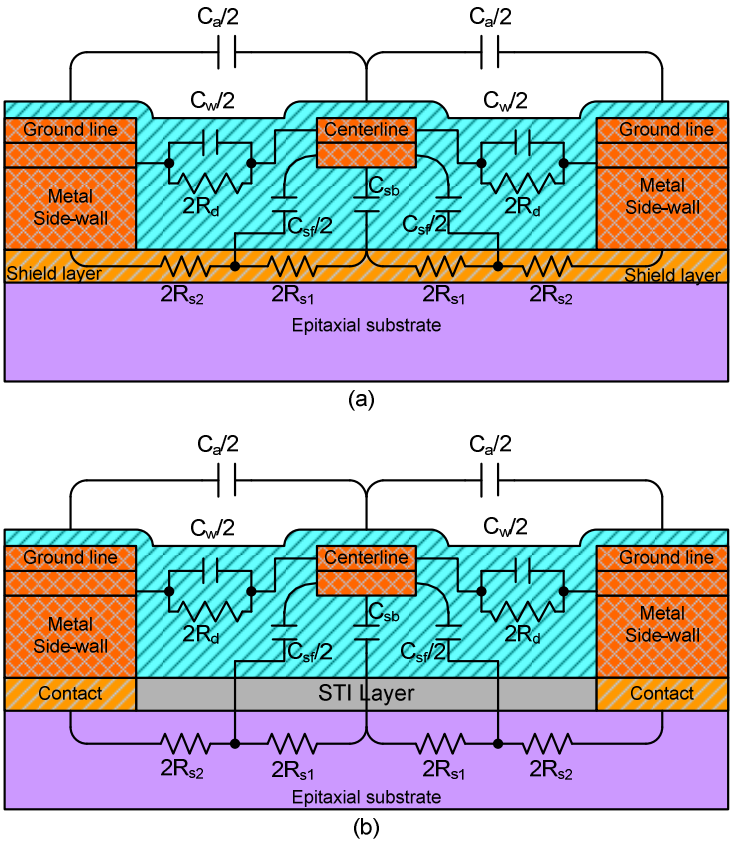


Fig. III-14. Representation of the physical meaning of the elements in the vertical branch f the model in Fig. III-10.

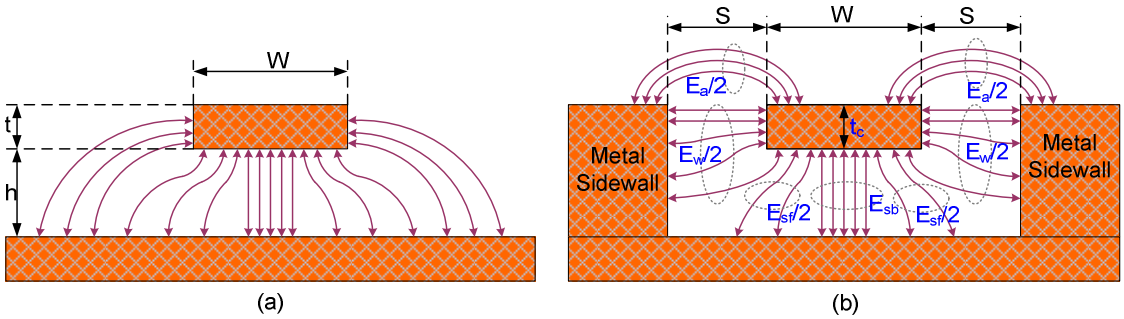


Fig. III-15. Electric field profile of an infinite length conductor above infinite ground plane (a) and of the inductor structure in our work

in which W, S and W_g are the centerline width, the centerline distance to the ground sidewall and the sidewall width, respectively. k' is equal to $\sqrt{1-k^2}$.

To calculate the capacitance between the centerline and the ground sidewall, consider Fig. III-14. Comparing this figure with Fig. III-13(b) reveals that the stored energy in the electrical field between the centerline and the sidewall (E_w in Fig. III-14) is approximately equal to E_w in Fig. III-13(b). Consequently the capacitance between the centerline and the sidewall in the inductor (C_w) is equal to the capacitance between the half of the total capacitance in Fig. III-14. On the other hand we can approximately calculate C_w from (III-?) after substituting t, h, W with $W/2$, S and $2t_c$, respectively.

The substrate or shield layer resistance R_s in Fig III.12, is calculated from [23]:

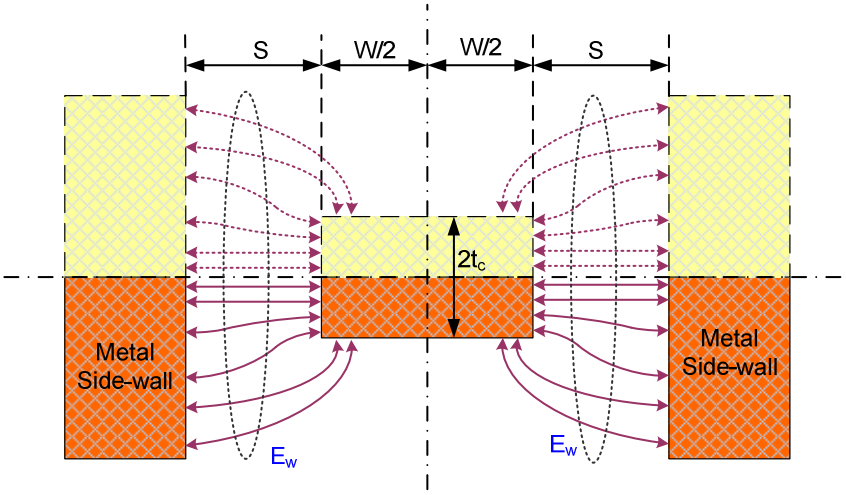


Fig. III-16. Calculation of the capacitance between the ground sidewall and the centerline, using a supposition symmetric structure

$$R_s = \frac{1}{\sigma_s F(W, S, W_g, 0)} \tag{III-19}$$

In which σ_s is the substrate or shield layer conductivity and F is a complicated analytic function, defined in [34]. W and W_g are the width of the centerline and the ground walls, respectively and S is the distance from the centerline to the ground sidewalls.

The dielectric loss effect has been captured by R_d in Fig. III-12. R_d is calculates as:

$$R_d = \frac{1}{(C_{sb} + C_{sf})\omega \tan(\delta)} \tag{III-20}$$

Where C_{sb}, C_{sf} are calculated from (III-15). ω is the working frequency and $tan\delta$ is the effective dielectric loss tangent for the dielectric layer stack. The dielectric material in CMOS technology is mainly silicon-dioxide, for which the loss tangent is 0.01, based on the measurements in [28]. Nonetheless, loss tangent as high as 0.05 has been reported for CMOS technology 24GHz band [5].

C) Short-End Model

Short-end model in Fig. III-9 is an RLC resonance network. However, the resonance frequency of this RLC circuit is well beyond the working frequency and consequently we can use a simple series RL circuit, instead of RLC circuit. Analysis and study of short-end discontinuity in a CPW has been reported in many literatures. However these equations are valid only for low-impedance lines with very simple structure and can not be used in our works, in which the line characteristic impedance is chosen as high as possible [35], [36]. So we have developed a semi-empirical equation to calculate the resistance and a empirical equations to calculate the inductance in the short-end model.

The equation we have developed to calculate the inductor in the short-end model is as follows:

$$L_{end} = \frac{a\sqrt{S}}{W^b} \cdot \sqrt[n]{\left(\frac{S}{S_0}\right)^n + 1} \tag{III-21}$$

S_0, a, b and n are constant fitting parameters and has the value 15um, 1.95, 0.1 and 1.5, respectively. W is the centerline width and S is the distance from the centerline to the ground sidewall.

To calculate the short-end equivalent series resistance we have used the simple equation as below:

$$R_{end} = \rho_{eff} \frac{S}{W} + R_{loss} \quad \text{(III-22)}$$

R_{loss} the equivalent to the substrate loss, and in our work for the geometric sizes we have dealt with, is a constant equal to 0.1. ρ_{eff} is effective sheet resistance of the centerline and we used the equation below to best fit to the simulation results:

$$\rho_{eff} = \rho W^{0.6} \quad \text{(III-23)}$$

in which ρ is the centerline static sheet resistance, given by the foundry design kit.

These equations are fully empirical and their parameters does not have any physical meaning. The equation has been adopted in consequence of investigation of simulation results. Empirical equations are useful in describing the electromagnetic characteristics of complicated structures, such as CPW discontinuities, that can not be simply analyzed [35].

III.2.3.2 Model Evaluation with Simulation

A) Electromagnetic Simulation Tool

Agilent Advanced Design System (ADS) and Ansoft HFSS have been widely used in recent years by the mm-wave IC designers in simulation and design of passive elements [37], [38], [39]. We started our work with MoM simulator using ADS, in the first steps. MoM simulation in ADS can be accomplished in two ways. One way is in which each metal layer with thickness t_m is modelled as sandwich of a via layer and two zero-thickness conductor layers in the upper and lower surface of the via layer, as shown in Fig. III-17(b). The via layer can pass the current only in vertical direction and lateral currents flow only in the zero-thickness conductor layers. Sum of sheet resistance of two zero-thickness conductor layers are equal to the sheet resistance of the metal layer to be modelled. Unfortunately sheet currents can not model the current distribution in the conductors and this causes noticeable errors in integrated design, in which the conductor's thickness is in order of skin dept and current is distributed in the conductor's cross section. For example, when currents are modelled as sheet currents, the internal inductance is zero. In ADS MoM simulator there is another substrate modeling option, named thick metal modeling, depicted in Fig. III-17(c). When this option is enabled, sheet currents can flow in the vertical surface of metal line, besides the lateral surfaces. Note that again in this mode current can not pass inside the metal layer. This option can lead to better accuracy in some cases.

In the next steps of our work we examined the ADS transmission line modelling tool in schematic environment. In this simulator two-dimensional field solver is used and Non-Quasi-TEM parts, such as T-Junctions, are modelled very simply. We found that this technique has some limitations in modeling multi-line, multi-layer arbitrary structures and shield layers.

Finally we switched to full wave field simulators and used Ansoft HFSS. The most challenge in using 3-D field simulators is defining and correctly rendering very complicated 3-D structures, mostly encountered in integrated design. To overcome this problem we developed special programs in VBasic. It must be noted that Ansoft HFSS accepts the simulation projects definition in three ways, i.e. direct GUI[1], DLL[2] interface using C language and scripting facilities using VBasic language. Our 3-D rendering and interface tool is composed of many program objects, up to many thousands lines of high level programs. This interface tool can create very complicated multi-layer 3-D objects, that can never be created by hand. We will show the power of this tool in the rest of this section.

[1] Graphical User Interface
[2] Dynamic Library Link

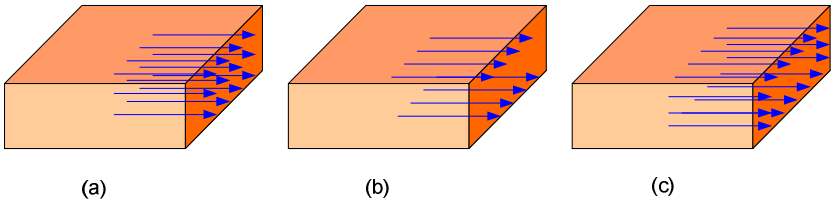


Fig. III-17. Metal layers modeling of ADS for MoM simulation: Currents in real metal layer(a), currents in sheet conductor model of ADS, MoM simulator (b) and currents in thick conductor model of ADS, MoM simulator

B) Model Parameters Extraction

To evaluate the analytic equations, developed in the previous section, we have simulated an inductor with given dimensions, using ADS and HFSS electromagnetic field simulators. Then the model parameters have been extracted from simulation results and have been compared with the analysis results. Extraction is performed in two-step process. In the first step, Quasi-TEM region of the inductor is simulated as a transmission line with ports in both ends. Then the standard RLGC model, corresponding to the Quasi-TEM region is extracted (See Fig. III-9(b)). In the second step, total inductor is simulated and after de-embedding the Y parameter of Quasi-TEM section, Y parameter of short-end section is obtained. Most of the electromagnetic field simulators give the simulation results in different multi-port matrix representation formats, such as S, T, Z or Y matrixes. We have used Y matrix representation in our parameter extraction.

To calculate the elements of standard RLGC model of Fig. III-9(b) from Y parameters, we define:

$$Z_s = R_s + j\omega L_s$$
$$Y_p = G_p + j\omega C_p \qquad \text{(III-24)}$$

Then we obtain the Y parameter of RLGC model is simply calculated:

$$Y_{11} = Y_{22} = \frac{1 + Z_s Y_p}{Z_s\left(2 + Z_s Y_p\right)}$$
$$Y_{12} = Y_{21} = \frac{-1}{Z_s\left(2 + Z_s Y_p\right)} \qquad \text{(III-25)}$$

And we simply deduce:

$$Z_s = \frac{1}{Y_{11} - Y_{12}}$$
$$Y_p = \frac{Y_{12}^2 - Y_{11}^2}{Y_{12}} \qquad \text{(III-26)}$$

Short-end admittance is calculated easily after calculating the Y parameters of the Quasi-TEM section and the admittance to the inductor.

$$Y_{end} = \frac{Y_{12} Y_{21}}{Y_{11} - Y_{ind}} - Y_{22} \qquad \text{(III-27)}$$

where Y_{ij} are Y parameters of the Quasi-TEM section and Y_{ind} is the admittance to the inductor.

To compare the RLGC parameters obtained from analytic equations with that of electromagnetic field simulation, we have simulated the Quasi-TEM section of the inductor using full wave simulation in HFSS and MoM solver in ADS. The results have been shown in Fig. III-18. Centerline width is 5um, ground sidewall width is 30um, centerline-sidewall space is 30um. No shield layer has been used and centerline structure is as in Fig. III-5(c). This figure shows that there is noticeable difference between HFSS and MoM results and our

model is in good agreement with the HFSS full wave results. This figure reveals the importance of using full wave field solver, instead of Quasi-3D MoM technique of ADS. 3-D view of Quasi-TEM section, simulated in ADS has been shown in Fig. III-19. Electric and magnetic field vectors of Quasi-TEM section, obtained from simulation in HFSS have been shown in Fig. III-20. This figure clearly shows that the Quasi-TEM assumption is valid.

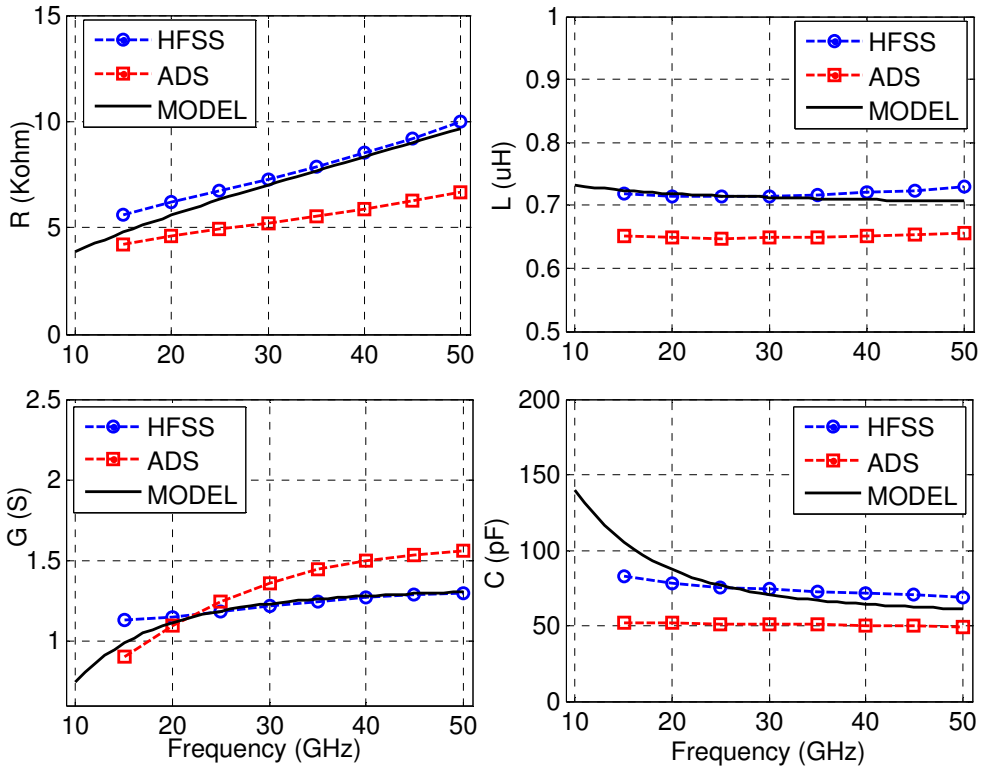


Fig. III-18. Comparison of RLGC parameters of Quasi-TEM section, obtained from our model, MoM simulation in ADS and full wave simulation in HFSS (W=5um, Wg=30um, S=30um).

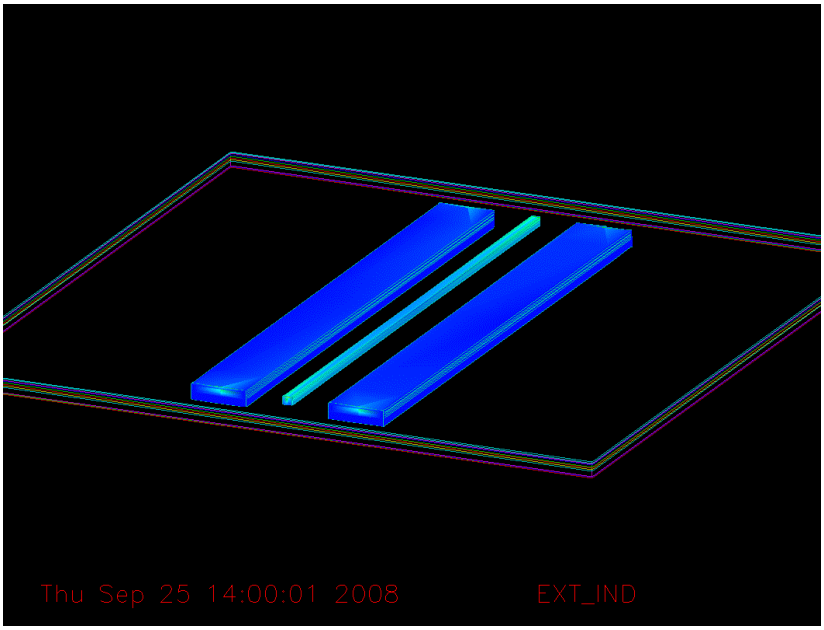


Fig. III-19. 3-D view of Quasi-TEM section, simulated in ADS MoM field simulator

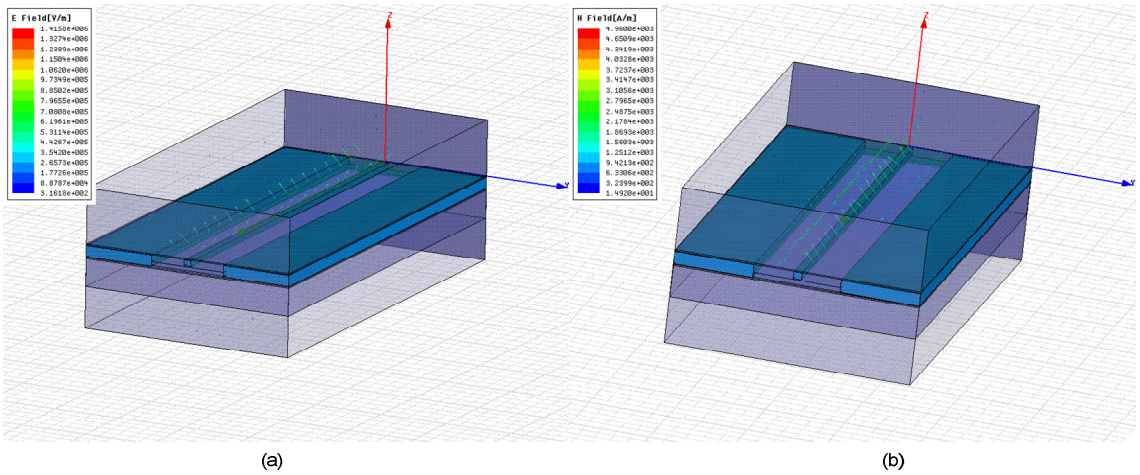


Fig. III-20. (a) Electric field and (b) magnetic field vectors of Quasi-TEM section, obtained from simulation in HFSS

Finally, to show the characteristics of line-type inductors, we have optimized a 225pH line-type inductors using our model and optimization tool. For the optimized inductor, the centerline width is 5um, ground sidewall width is 30um, centerline-sidewall space is 30um and the line length is 300um. We have simulated this inductor using ADS and HFSS. The inductance and the quality factor of the inductor has been shown in Fig. III-21. Again, our model is in good agreement with the HFSS results, but the ADS results have discrepancy with the full wave simulation results. This figure shows that when frequency increases, both of the inductance and quality factor increases, but the quality factor reaches a maximum point at 40GHz. With increasing frequency, the inductance increases rapidly and quality factor drops. At the resonance frequency of the inductor, the quality factor is zero. This means that all of the energy delivered to the inductor is dissipated and the inductor acts as a resistance.

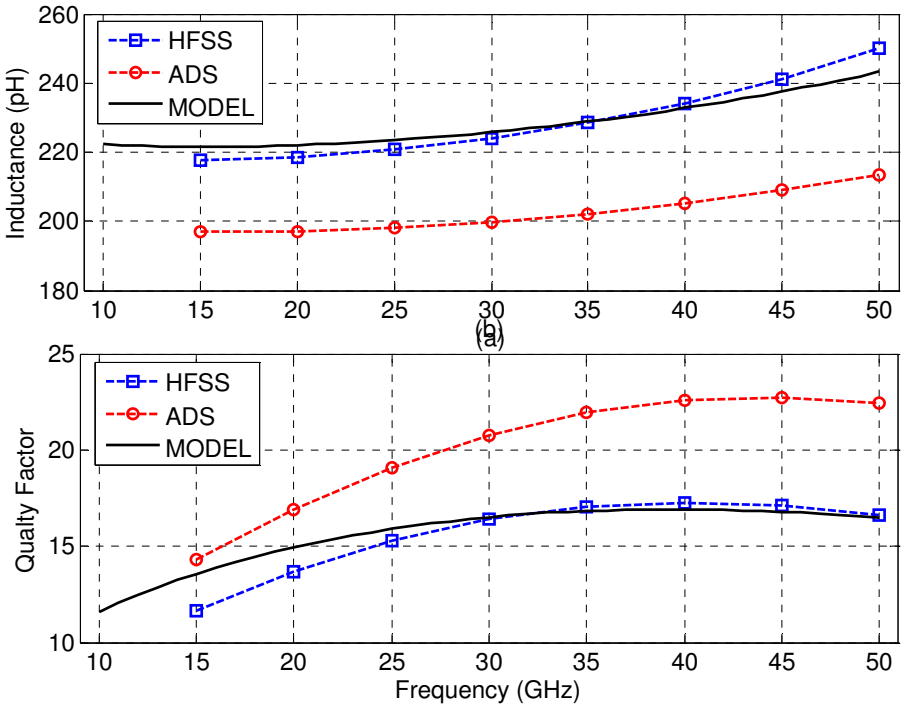


Fig. III-21. Inductance and quality factor of the 225pH line-type inductor, as a function of frequency

III.3 Other Passive Elements

III.3.1 RF Pad Design and Modeling

RF pad is a stack of specially patterned metal layers, with firmly tied density design rules. Each metal layer is a ladder of metal lines, enclosed in a metal frame. Such complicated structure is to ensure the resistance of the pad against high mechanical pressure of probing or wire bonding process. The top most layer of pad is ALUCAP layer that forms a uniform metal layer for probing. Vertical cross section and simplified 3-D view of the RF pad and related ground ring have been shown in Fig. III-22. Lumped element model of RF pad has been shown in Fig. III-23. This model comprises the capacitive coupling between successive metal layers and between top of the pad and ground ring, dielectric loss and substrate loss. Similar pad lumped model has been used in [40]. The capacitive coupling between successive metal layers is calculated as:

$$C_{i,i+1} = \alpha \varepsilon_{i,i+1} \frac{A_{pad}}{t_{i,i+1}} \tag{III-28}$$

A is the pad area, $t_{i,i+1}$ is the thickness of dielectric layer between i^{th} and $(i+1)^{th}$ metal layer, and a is a fitting parameter accounts for the girded metal layer and is equal to 0.9. Dielectric loss is calculated as:

$$R_d = \frac{\beta}{C_p \omega \tan \delta} \tag{III-29}$$

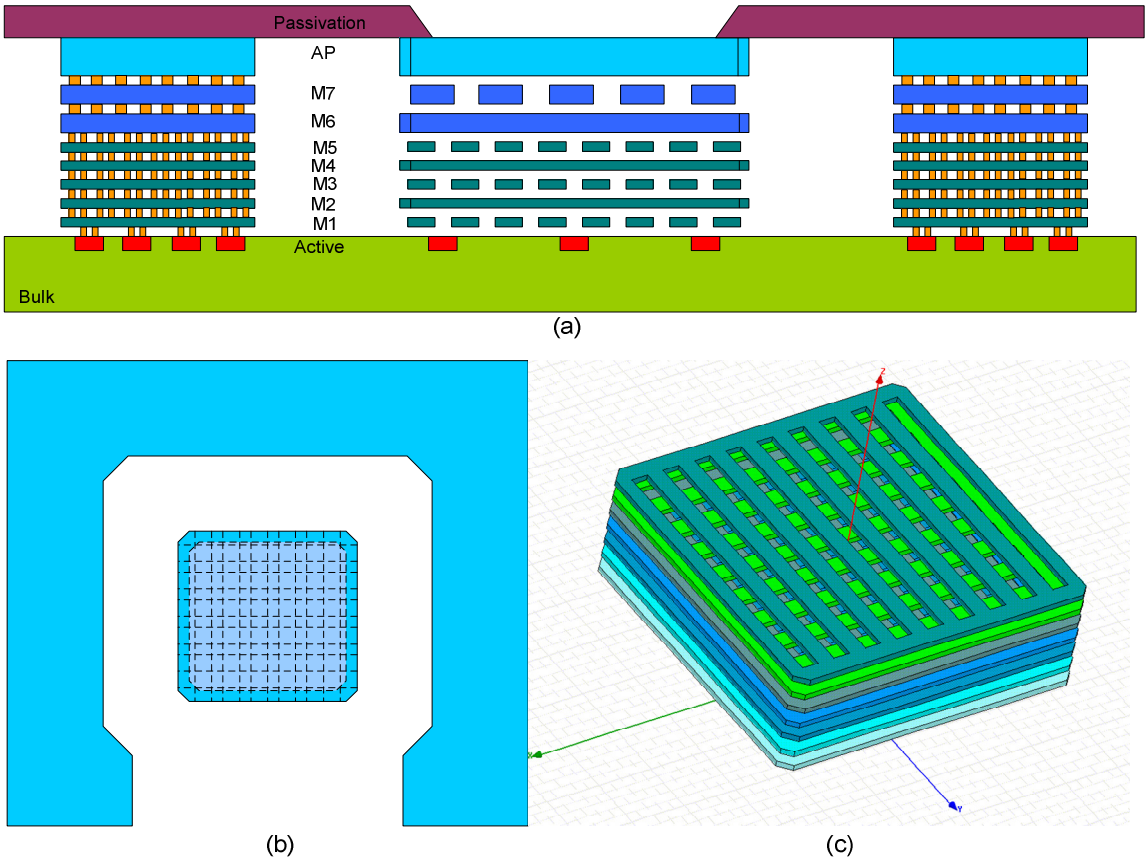


Fig. III-22. Cross section (a) and top view (b) of RF pad and related ground ring, and 3-D view of the metal grid stack in the pad (c)

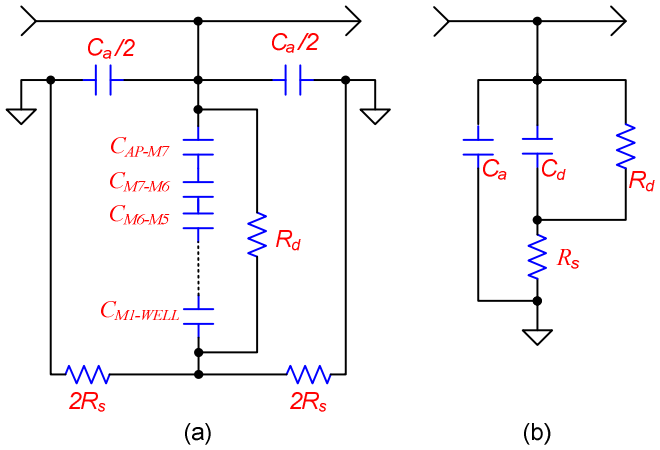


Fig. III-23. Lumped element model of RF pad (a) and its simplified form (b)

β is a fitting parameter accounts for the approximation of Fig. III-23(a) to Fig. III-23(b) and C_d is the equivalent pad-substrate capacitance. Substrate resistance, R_s, and the capacitance between the pad top surface and the ground ring, C_a, is calculated by approximating the pad and ground ring as two parallel lines, with proper length. By this way the C_a is calculated using (III-17) after setting the line length equal to $2(a_{pad}+a_{gnd})$, where a_{pad} and a_{gnd} are pad and ground ring length, respectively. R_s is calculated as:

$$R_s = \rho_{sub}\frac{2(a_{pad}+a_{gnd})}{S} \tag{III-30}$$

In which ρ_{sub} is the substrate sheet resistance and S is the pad-ground space. RF pad lumped model parameters have been tabulated in Table III-1.

TABLE III-1
Elements of the Lumped Model of RF Pad

R_p	R_s	C_p	C_a
2.3 KΩ	100Ω	23fF	1.6fF

III.3.2 T-Junction Model

In our layouts, T-junction is used to connect shorted end line-type inductor to the transmission lines. Top view of T-Junction, its equivalent lumped element circuit models have been shown in Fig. III-24. Lumped element model is used in post layout simulations. The elements of lumped model are extracted from full wave simulation results, using the following analysis.

Regarding Fig. III-24 and used port numbering, we can calculate 3-by-3 Y-matrix of the T-junction.

$$\begin{aligned}
Y_{11} &= Y_{22} = \frac{Z_s + Z_p + Z_s Z_p Y_p}{Z_s\left(Z_s + 2Z_p + Z_s Z_p Y_p\right)} + j\omega C_{13} \\
Y_{33} &= \frac{2 + Z_s Y_p}{Z_s + 2Z_p + Z_s Z_p Y_p} + j\omega C_{13} \\
Y_{12} &= Y_{21} = \frac{-Z_p}{Z_s\left(Z_s + 2Z_p + Z_s Z_p Y_p\right)} \\
Y_{13} &= Y_{31} = Y_{32} = Y_{23} = \frac{-1}{Z_s + 2Z_p + Z_s Z_p Y_p}
\end{aligned} \tag{III-31}$$

Where:

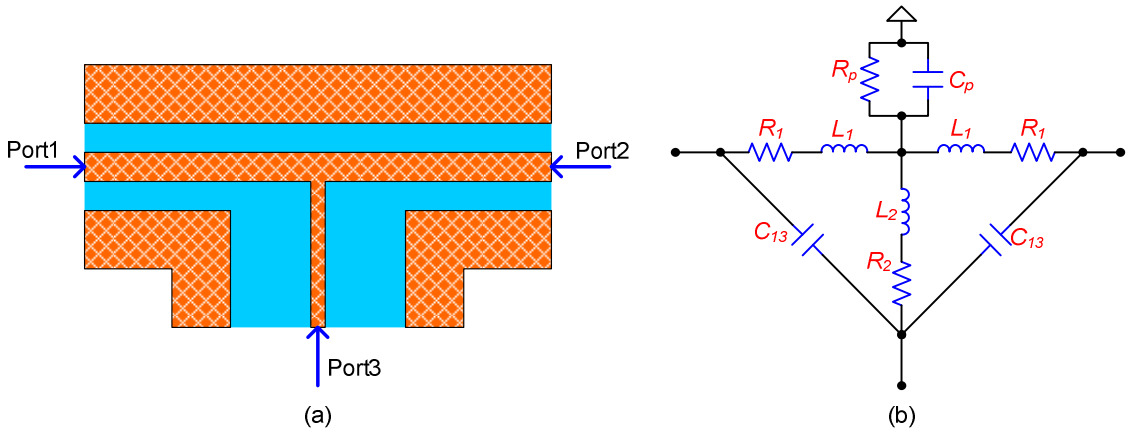


Fig. III-24. T-junction top view (a) and its equivalent lumped elements model (b)

$$Z_s = R_1 + j\omega L_1$$
$$Z_p = R_2 + j\omega L_2 \qquad \text{(III-32)}$$
$$Y_p = G_p + j\omega Cp$$

Then in reverse manner, Z_s, Z_p, Y_p and C_{13} are obtained:

$$Z_s = \frac{Y_{12} - Y_{13}}{(Y_{11} - Y_{33} - Y_{12} - 2Y_{13})Y_{12} + (Y_{13} + 2Y_{12})Y_{13}}$$
$$Z_p = \frac{Y_{12}}{Y_{13}} \frac{Y_{12} - Y_{13}}{(Y_{11} - Y_{33} - Y_{12} - 2Y_{13})Y_{12} + (Y_{13} + 2Y_{12})Y_{13}} \qquad \text{(III-33)}$$
$$Y_p = \frac{(Y_{33} + Y_{11} + Y_{12})Z_s + 1}{-Y_{13}Z_s} - \frac{2}{Z_s}$$
$$j\omega C_{13} = -Y_{11} - \frac{1 + Y_{12}Z_s}{Z_s}$$

And finally the lumped model elements are easily calculated from (III-32).

3-D multi-layer structure of T-junction, used in HFSS full wave simulation has been shown in Fig. III-25. All of the technology layers have been included with their individual materials property.

III.3.3 Transmission Lines Design

Transmission lines are widely used in RF integrated circuits to create signal path between different blocks of design, as well as different points of a circuit block. Two types of transmission lines, i.e. microstrip and coplanar transmission line (CPTL), are conventionally used in mm-wave integrated circuit design [20], [38], [41]. Electric field distribution of microstrip and coplanar lines has been shown in Fig. III-1. Main advantage of coplanar structure is elimination of the coupling between adjacent lines and crosstalk noise. In the case of low-impedance lines, in which the space between centerline and ground strips is small, electric filed lines are concentrated far away from the substrate, as shown in Fig. III-1. In contrast, for high impedance lines, the electric field penetrates in the substrate and can causes substrate losses, if low-resistivity substrate is used. Consequently coplanar structure is not suitable for the technologies with low resistivity lossy substrate. Other disadvantage of this

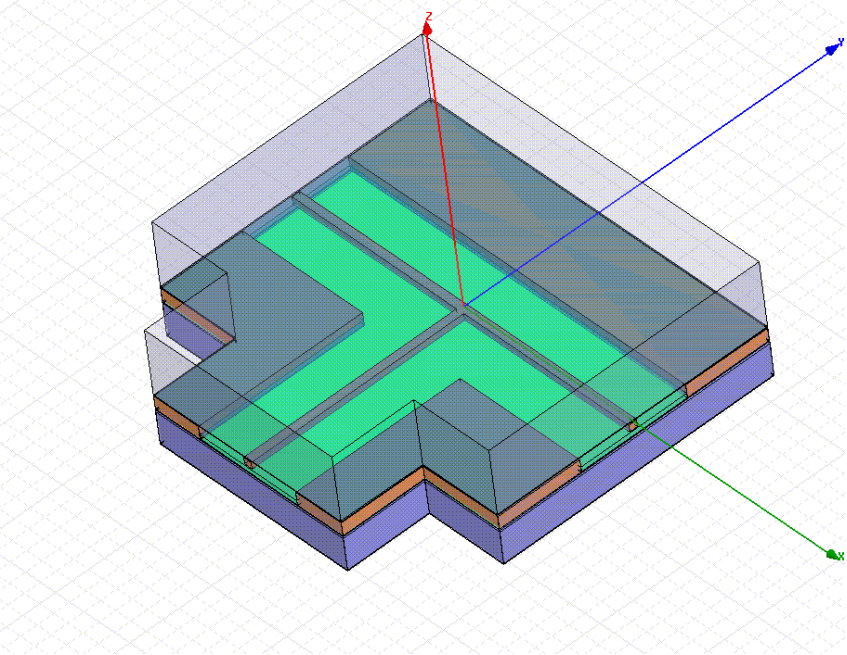


Fig. III-25. 3-D multi-layer structure of T-junction, used in HFSS full wave simulation

structure is wide area required for implementation of ground strips. Meandering CPTL's requires large chip area, but the designer is relax of coupling between adjacent lines [37], [42].

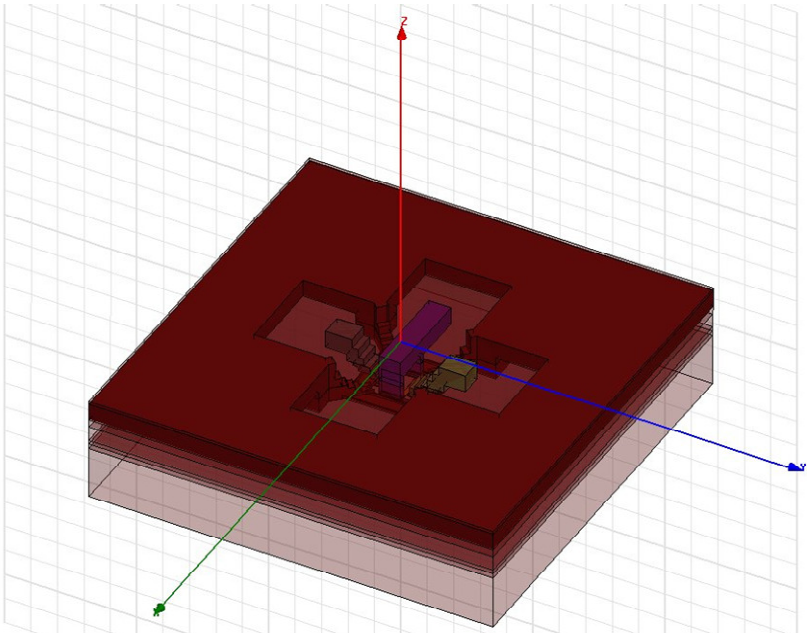
In comparison with coplanar structure, microstrip structure is more prone to the adjacent line coupling and crosstalk [43]. On the other hand in microstrip structure the coupling to the substrate is eliminated and hence it is suitable for CMOS technologies, for which the substrate is low resistivity and very lossy in mm-wave frequencies. The other advantage of microstrip structure is that meandering is carried out in small area, provided that the minimum space between lines is complied [41], [44]

In our work, we have used the line structure described for the line-type inductor for the transmission lines. In this structure the line capacitance is equal to the conventional microstrip line, but the inductance is higher than that of microstrip line. Consequently using our structure wider centerline can be used and this improves the line quality factor. Wide centerline is also achievable using CPW structure, e.g. 10um in [42], but the line-ground space should be increased and this increases coupling to the substrate.

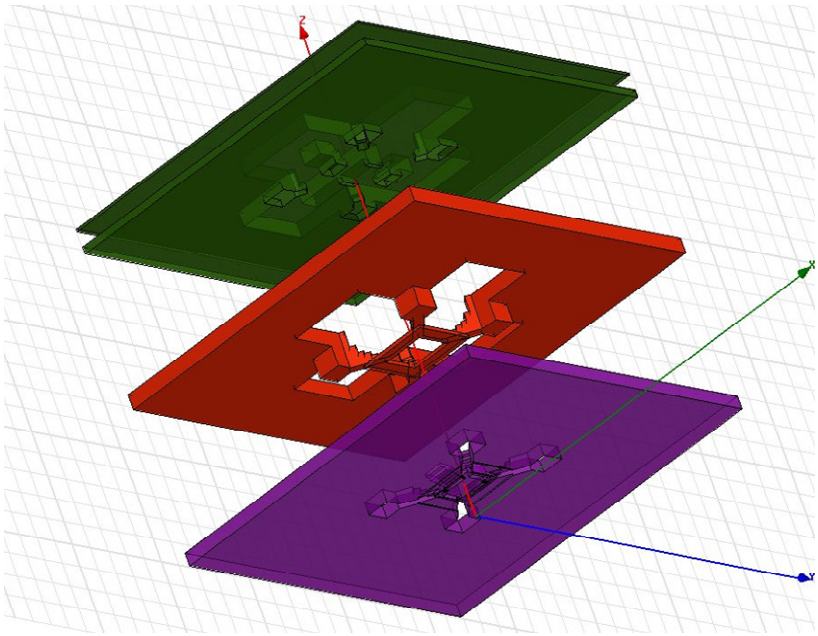
Transmission lines with characteristic impedance from 50Ω up to 60 Ω have been reported in CMOS mm-wave designs. In our work, regarding the RF pad impedance, optimum line impedance is 51 Ω, as used in [42] in 90nm CMOS. Using our optimization tool, the optimum centerline width and centerline-sidewall space are obtained 5um and 15um, respectively.

III.3.4 Transistor Interconnections

The interconnection from transmission line to the transistor nodes, we have used the transmission line structure with gradually reducing centerline, centerline-ground space and centerline height from substrate. To obtain the lumped model of transistor interconnect, as described in Chapter II, we have used our 3-D rendering tool to define very complicated structure of this interconnection for HFSS simulation. Fig. III-26 shows the interconnect structure. To clarify the complexity of this structure, some parts of this structure have been shown separately.



(a)



(b)

Fig. III-26. Rendering 3-D structure of MOS transistor to HFSS, using our interface tool. (a) Complete structure and (b) Some of its incorporated metal and dielectric objects

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