Méthodes et outils pour la conception et la fabrication des microsystèmes

Jean-Michel Karam

THESE

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Jean Michel KARAM

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METHODES ET OUTILS POUR LA CONCEPTION ET LA FABRICATION DES MICROSYSTEMES

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Président	:	Robert PERRET
Directeur de thèse	:	Bernard COURTOIS
Rapporteurs	:	Marta RENCZ
		Manfred GLESNER
Examinateur	:	Nadine GUILLEMOT

Thèse préparée au sein du Laboratoire **TIMA**

L'intelligence ... dépourvue d'égoïsme perçoit des vérités qui coïncident avec l'humilité laquelle permet l'appréhension d'abord, la compréhension ensuite et la réalisation finalement ...

... One night a man had a dream. He dreamed he was walking along the beach with the Lord. Across the sky flashed scenes from his life. For each scene he noticed two sets of footprints in the sand, one belonging to him and the other to the Lord. When the last scene of his life flashed back before him, he looked at the footprints in the sand. He noticed that many times along the path of his life there was only one set of footprints. He also noticed that it happened at the very saddest and lowest time in his life. This bothered him and he questioned, "Lord, you said that once I decided to follow you, you'd always walk with me. But I have noticed that during the most troublesome times in my life, there is only one set of footprints. Why when I need you most do you leave me ? "

The Lord replied, "my son, my precious child, I love you and would never leave you. During your times of trial and suffering, when you see only one set of footprints, it was then that I carried you".

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Il me serait impossible de ne pas remercier ma famille et surtout mes parents à qui je dédie ce travail en témoignage de gratitude. Mon coeur souffrant en silence de ta perte, maman, parle aujourd'hui en ton souvenir...

RESUME

Un des obstacles majeurs pour démarrer une activité dans le domaine des microsystèmes est le fait que des technologies particulières et donc coûteuses sont nécessairement requises. D'autre part, alors que les outils de CAO pour la microélectronique ont acquis un degré de maturité élevé, où toutes les séquences de fabrication sont simulées et le fonctionnement d'un composant ou système peut être complètement prévu, l'art de la modélisation et de la conception des microsystèmes ne fait que débuter.

Le développement de la Microélectronique vers la fin des années 70 a été rendu possible par l'utilisation d'outils CAO et par la mise à disposition de fonderies. Sans apports comparables, les Microsystèmes resteraient des curiosités de laboratoire, des prouesses techniques de chercheurs, mais ne deviendraient pas des produits industriels.

Ainsi, l'objectif de cette thèse est d'assurer un accès à la technologie des microsystèmes en adaptant des lignes de production industrielles pour la microélectronique, de développer un environnement de conception et de simulation basé sur des outils existants étendus et de définir une architecture générique de microsystèmes.

ABSTRACT

Starting from the 70s, Microelectronics development has been made possible because of the use of CAD tools and because of the availability of foundries for Education / Research and a fabless companies, besides large IC manufacturers. Without such similar boosters, Microsystems might easily remain curiosities, top level prototypes manufactured by researchers, but they would not become industrial products.

One of the main obstacles to start with microsystems is the fact that particular, and hence costly processes are needed. Moreover, when in microelectronics, CAD has already attained a highly sophisticated and professional level, the art of microsystem design and modelling is still in its infancy.

The aim of this thesis is to insure access to microsystem technology by the use of existing production lines for micro-electronics, with an additional post-processing for micro-system specific 2D and 3D structures, in order to take advantage of investments made in the past, to develop CAD tools for microsystems based on existing tools and to define a generic architecture that could be used in the design of complex microsystem.

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INTRODUCTION

1.1. Définitions

Beaucoup de définitions du terme "Microsystème" ont été données au cours de ces dernières années; toutes convergent sur le fait qu'un microsystème comporte des capteurs et/ou actionneurs avec de l'électronique de contrôle, intégrés d'une manière monolithique ou hybride. Des microsystèmes plus complexes peuvent demander l'utilisation d'un microcontrôleur. En résumé, un microsystème devrait être capable :

- de percevoir un phénomène particulier de son environnement (mesure),
- d'interpréter et de mettre en forme les signaux correspondants (intelligence),
- d'effectuer l'action conséquente (action),
- de rendre compte de cette action sur l'environnement.

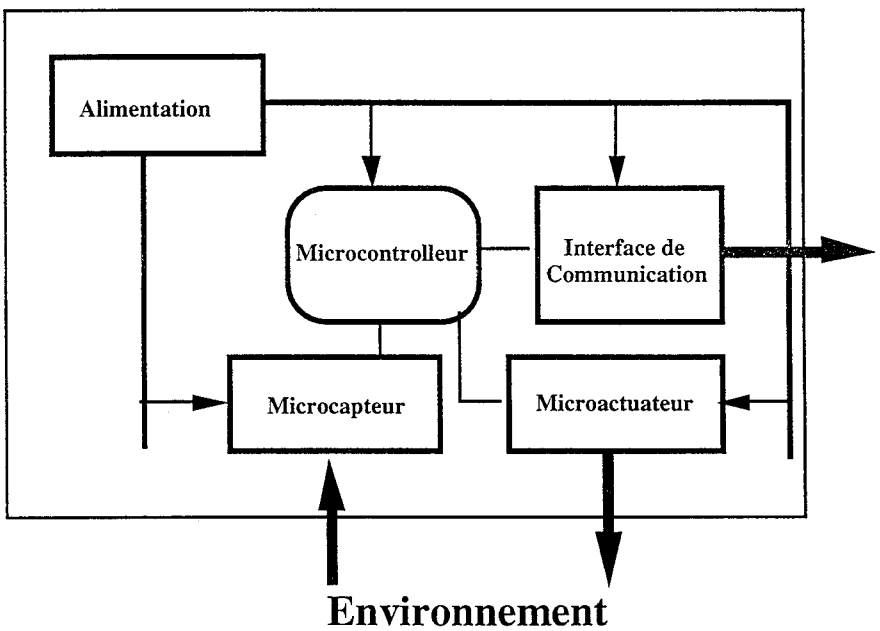

Fig. 1.1.1. Architecture générale d'un microsystème

1.2. Situation économique et applications

Le marché des microsystèmes est en rapide expansion et supposé d'atteindre 14 milliards de dollars à la fin de la décennie (700 millions de dollars en 1990). De nouveaux produits sont en cours de développement et de nouvelles applications identifiées. Les microsystèmes permettent de réduire les coûts, l'encombrement et la consommation tout en améliorant la fiabilité, ouvrant ainsi des marchés économiques importants.

Selon l'étude de marché réalisée par Frost et Sullivan, les secteurs d'applications des miocrosystèmes se répartissent ainsi:

Secteur d'applications	1993 (%)	1998 (% estimé)
Automobile	38.8	54.2
Médical	23.2	24.9
Processus industriels	1.3	0.7
Aérospatial / Militaire	10.3	5.3
Automatismes	22.1	12.5
Energie / Environnement	1.5	1.0
Education / Recherche	0.7	0.4
Applications diverses	2.1	0.9

Table 1.2.1. Répartition du marché européen des microsystèmes

Le marché le plus important en volume est donc celui de l'automobile. Une voiture comporte aujourd'hui entre 7 et 10 capteurs, elle en comportera 50 à 60 d'ici l'an 2000. Le marché mondiale de l'automobile va passer de 1.1 milliard de dollars en 1995 à 3 milliards d'ici la fin du siècle. Les microsystèmes interviennent dans l'automobile au niveau des systèmes de sécurité, de gestion d'énergie / consumables, de diagnostic et contrôle. Ainsi, dans le domaine de la sécurité, l'accéléromètre et/ou le gyromètre trouvent une bonne place dans l'airbag (accéléromètre 50 g, g étant l'accélération de la pesanteur), la suspension active (accéléromètre 2g, gyromètre) et l'ABS (accéléromètres et gyromètres). La pression est un paramètre essentiel dans des applications de contrôle comme l'injection d'essence (pression d'air) et la boîte automatique (pression hydraulique) et des applications de diagnostic comme la pression des pneus, du circuit de freinage et le réservoir d'essence. Dans la navigation, beaucoup de types de capteurs sont nécessaires comme l'accéléromètre, le gyromètre, les capteurs magnétiques et d'autres. La figure 1.2.1 illustre un schéma bloc d'un airbag de voiture. Ces microsystèmes devront résister au conditionnement du groupe micropropulseur : température de -40 °C à +200 °C, vibrations, humidité, poussières, graisses et salissures ... Ils devront être également "compatible électromagnétiquement".

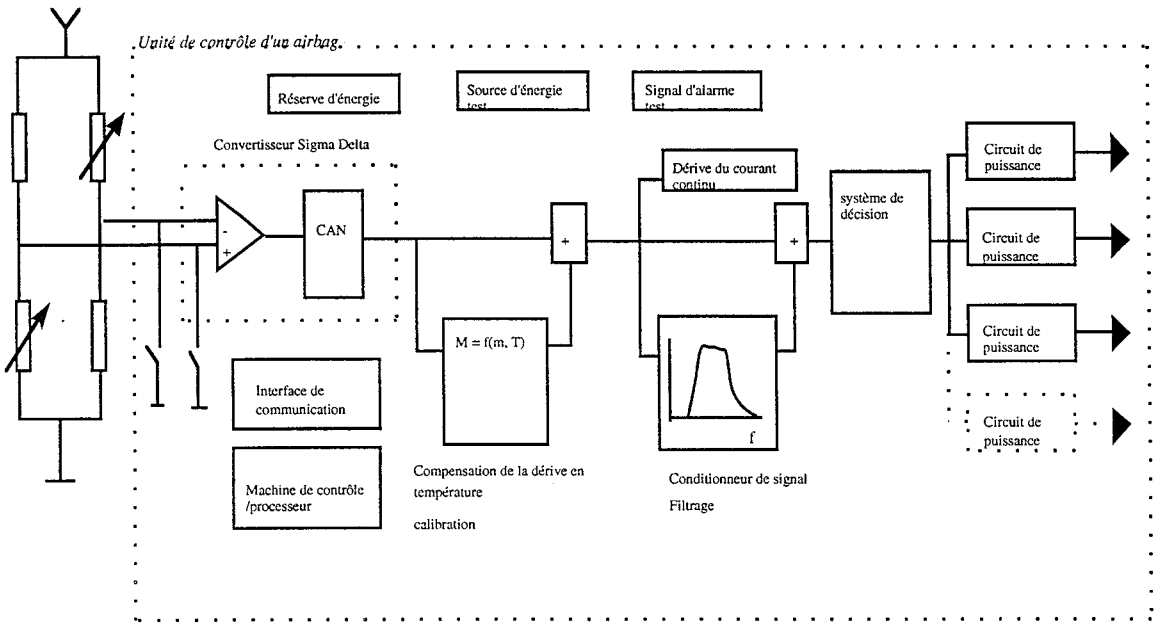

Fig. 1.2.1. Architecture d'un airbag de voiture

Les applications médicales, bien qu'elles n'engendrent pas un marché équivalent à celui de l'automobile, constituent un domaine où les microsystèmes peuvent amener des changements et des évolutions importantes. Des microsystèmes commencent à s'intégrer dans des systèmes comme le

pacemaker, les pompes d'infusion, les systèmes de délivrance de médicaments, et d'autres. Les capteurs de pression sanguine constituent des microsystèmes disponibles sur le marché.

Les applications médicales peuvent être thérapeutiques ou de diagnostic. Le diagnostic implique la perception des signes caractéristiques de certains phénomènes. L'évolution des microcapteurs a considérablement amélioré la qualité de l'information requise par le physicien (par exemple, l'ultrasonographie intra-vasculaire). Certains signaux présentent un intérêt particulier. La lumière est évidement une des sources d'énergie la plus utilisée pour l'analyse d'organe. Elle peut être utilisée pour analyser des cavités, naturelles ou artificielles. Des progrès peuvent être notés dans ce domaine (caméras endoscopiques). Cependant une application potentielle dans ce domaine est la micro-caméra qui fournira des informations quantifiables facilitant le diagnostic, comme par exemple, l'efficacité des broncho-dilateurs (utilisé pour l'asthme). L'ultrason dont l'équipement a été considérablement miniaturisé a prouvé son efficacité quant à l'investigation des tissus. D'autres signaux présentent un grand intérêt pour les physiciens comme la pression dont la mesure est essentielle dans beaucoup d'applications telles que le contrôle ambulatoire de la pression artérielle ou le diagnostic du glaucome, et les signaux chimiques dont la mesure pourrait permettre des analyses locales en temps réel des concentrations de différents ions et corps chimiques. Dans les applications thérapeutiques, il faut distinguer les microsystèmes guidés des microsystèmes autonomes. Diverses applications intègrent le premier ou le second type. La figure 1.2.2 résume les perspectives en applications médicales.

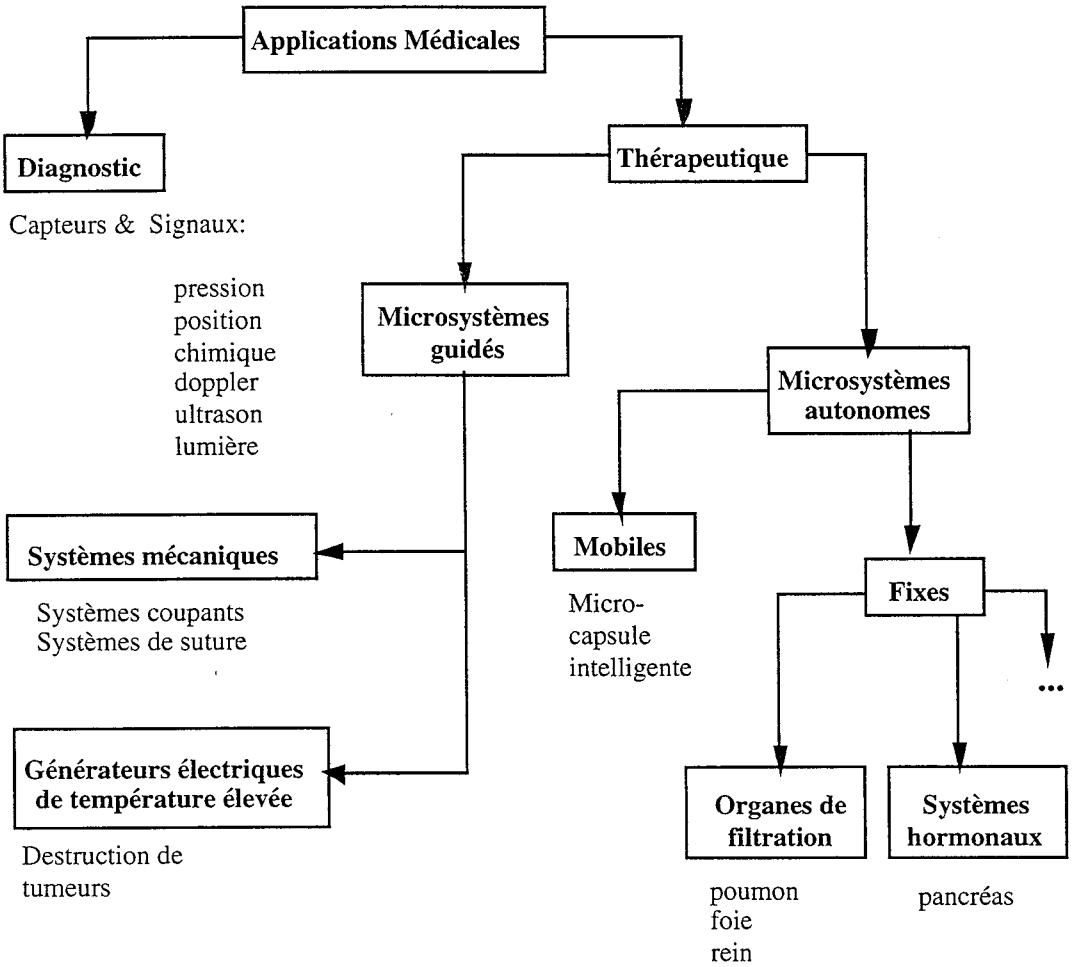

Fig. 1.2.2. Perspectives en applications médicales

Toutes les études de marché montrent que l'aérospatial n'est pas le principal marché de microsystèmes. Cependant, l'industrie de l'aérospatiale a consommé 28.8 millions de dollars en 1992 allant jusqu'à 35.2 millions de dollars en 1997 de microsystèmes.

Dans les applications aérospatiales, il existe deux types de mesures, fonctionnel et de sécurité. Dans les deux types de mesure, l'ensemble des capteurs produit une information redondante, filtrée à travers une logique de décision et effectuant l'action correspondante. On trouve ainsi un microsystème complet répondant particulièrement aux critères suivants : la miniaturisation, la faible consommation et la sécurité. Le coût n'est pas une contrainte particulière.

Les capteurs doivent réaliser les opérations suivantes :

- donner des informations sur le comportement de la fusée durant le vol,
- identifier les pannes ou les anomalies de fonctionnement durant le vol,
- assurer la position de la fusée,
- mesurer les caractéristiques de la fusée sur son orbite,
- donner une cohérence et une standardisation de l'équipement,
- accomplir une part de la mission pour laquelle la fusée a été lancée (images, mesures, ...).

Différents types de capteurs doivent être utilisés, notamment, capteurs de pression, de température, de position, de flux, d'accélération, de vibrations et collisions, de bruit acoustique, des thermocouples et des gyromètres.

Pour tous ces capteurs, les caractéristiques critiques sont :

- une large gamme d'utilisation :
    - i) Température élevée (T allant jusqu'à 1030 °K),
    - ii) pression élevée (P allant jusqu'à 200 bar),
    - iii) haut débit (V allant jusqu'à 560 m/s),
    - iv) niveau de bruit acoustique élevée.
- une fiabilité élevée : Pour maintenir la compétitivité, la fiabilité de la fusée doit avoisiner 0.98, donc une fiabilité de composant de 0.99 ; ceci veut dire une erreur sur 20-25 vols.

Finalement, les microsystèmes doivent ouvrir un éventail de vente attractif si le marché continue à croître. Pour cela, ils doivent être produits à bas coûts et avec une fiabilité assurée.

1.3. Présentation du problème

Pour plus que trois décennies, des technologies pour des capteurs intégrés et actionneurs ont été développées dans nombreuses institutions à travers le monde. Cependant, la production massive de microsystèmes reste bloquée par l'absence de fonderies industrielles (technologies standards) et d'environnements de conception et de simulation.

Un des obstacles majeurs pour démarrer une activité dans le domaine des microsystèmes est le fait que des technologies particulières et donc coûteuses sont nécessairement requises. D'autre part, alors que les outils de CAO pour la microélectronique ont acquis un degré de maturité élevé, où toutes les séquences de fabrication sont simulées et le fonctionnement d'un composant ou système peut être complètement prévu, l'art de la modélisation et de la conception des microsystèmes ne fait que débuter.

En résumé, un accès à la technologie très restreint et des outils CAO non appropriés, le domaine des microsystèmes paraît inaccessible à des structures telles que les PMEs et les institutions à budget limité.

1.4. Présentation de l'étude

Le développement de la Microélectronique vers la fin des années 70 a été rendu possible par

l'utilisation d'outils CAO et par la mise à disposition de fonderies. Sans apports comparables, les Microsystèmes resteraient des curiosités de laboratoire, des prouesses techniques de chercheurs, mais ne deviendraient pas des produits industriels.

L'Enseignement et la Recherche en Microélectronique ont bénéficié des infrastructures mises en place par des pays pionniers : les USA avec MOSIS et la France avec CMP. Ces infrastructures ont permis un accès facile et bon marché à des fonderies industrielles pour l'Enseignement et la Recherche, ce qui a permis de former de bons cadres pour l'Industrie. Par la suite, le secteur industriel à lui-même utilisé de telles infrastructures pour le prototypage et la fabrication en petit volume de circuits intégrés. Ces infrastructures ont été supportées par des développements d'outils de CAO : MAGIC à Berkeley et LUCIE à Grenoble. Par la suite, la plupart des Universités ont pu bénéficier de systèmes de CAO industriels, et ont donc pu se concentrer sur la conception et le développement d'outils CAO avancés, plutôt que se consacrer à des problèmes de CAO résolus par les outils industriels.

En terme de facilités de fonderies, l'expérience acquise en Microélectronique doit être mise à profit pour les Microsystèmes :

• les Microsystèmes doivent être fabriqués sur des lignes de production industrielles, avec un microusinage destiné aux structures micromécaniques. L'utilisation des lignes de production de Microélectronique permet de bénéficier des investissements déjà réalisés ;

• des design kits permettront de lier les outils CAO aux services de fonderie doivent être fournis aux concepteurs ;

• il faut accepter d'utiliser des lignes de production avancées pour les Microsystèmes compatibles avec la Microélectronique car les librairies (Microélectronique) ne sont utilisables que pour des technologies avancées ;

• des bibliothèques de cellules standard et des modules complexes doivent être fournis, avec leur layout et les modèles de simulation.

D'autre part, étant à l'origine des éditeurs de rectangles, les outils industriels de CAO Microélectronique sont devenus des systèmes intégrés permettant d'effectuer des simulations, de la synthèse, de la saisie de schémas, etc,... Le style de conception a également évolué en raison de l'accroissement nécessaire de la productivité : utilisation de plus en plus massive de cellules standards, puis de composants de plus en plus complexes comme des coeurs de microprocesseurs, des mémoires caches, etc... . D'électronicien, le concepteur est ainsi devenu un logicien, pour être de plus en plus maintenant un concepteur de systèmes. Mais ceci n'est rendu possible que parce que des spécialistes conçoivent au préalable des bibliothèques, des modèles, etc...

L'expérience acquise en CAO Microélectronique doit être mise à profit pour les Microsystèmes :

• ne pas re-développer des systèmes CAO Microsystèmes entièrement, mais réutiliser des modules de la CAO Microélectronique lorsque cela est possible ;

• créer un environnement CAO Microsystème qui soit familier aux utilisateurs de la CAO Microélectronique ;

• distinguer l'utilisateur "système" du concepteur de bibliothèques, cellules, etc, qui lui seul sera amené à utiliser des outils complexes spécifiques ;

• fournir aux Universités et Laboratoires de Recherche les même outils industriels de CAO Microsystèmes.

Ainsi, les Microsystèmes ne seront qu'une **évolution** conceptuelle de la Microélectronique, mais ils pourront devenir une **révolution** industrielle de par leur pénétration massive dans divers secteurs

applicatifs.

Ainsi, l'objectif de cette thèse est d'assurer un accès à la technologie des microsystèmes en adaptant des lignes de production industrielles pour la microélectronique, de développer un environnement de conception et de simulation basé sur des outils existants étendus et de définir une architecture générique de microsystèmes.

Le chapitre 2 détaille les méthodes de fabrication de microsystèmes compatible avec la microélectronique. Le microusinage de silicium et de l'arséniure de gallium est expliqué et les technologies développées et validées à travers cette thèse sont présentées. La théorie de conception menant à l'établissement des règles de dessin est aussi établie.

Le chapitre 3 porte sur les outils de simulation et de conception des microsystèmes. Après une introduction générale sur l'état de l'art, la modélisation des microsystèmes est détaillée sur tous ses niveaux : dessins de masques (layout), processus technologique (process), composant (chip) et système. Une structure d'environnement de CAO est proposée et les différents outils intégrés dans cette structure et développés au cours de cette étude sont aussi présentés.

Le chapitre 4 propose une architecture de conception générique pour des microsystèmes complexes comportant plusieurs capteurs et actionneurs. Un exemple de démonstrateur est considéré; c'est le microsystème du projet Européen BARMINT. Ce démonstrateur dont l'architecture globale a été défini à travers cette thèse, est dédié aux applications médicales et comporte une micro-pompe électro-thermo-pneumatique, plusieurs capteurs de pression, de température et chimiques avec un module de contrôle. Le packaging choisi est un MCM-V (cubique) qui permet de réaliser un système en trois dimensions.

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CHAPTER 2

MICROELECTRONICS COMPATIBLE MANUFACTURING TECHNIQUES

2.1. Introduction

There are two ways to manufacture microsystems : to develop processes specific to microsystems (hence these processes can address requirements specific to microsystems) or to use processes that have been developed for microelectronics. Among those later processes, some can be targeted to microsystems, again to address specific requirements, or it is possible to add special process steps to accommodate microsystems within integrated circuits.

One of the main obstacles encountered when starting to use microsystem technology is the fact that specialised, and hence costly processes are needed. In order to get affordable prices and a high flexibility, microsystems should whenever possible be designed in such a way that they can be manufactured on existing microelectronics production lines, with additional post-processing for microsystem specific 2D and 3D structures, to take advantage of investments made in the past. This approach allows designers to integrate microelectronics, needed in most microsystems, on the same chip. This is the monolithic solution which should be considered as the normal evolution of ASIC-foundries to microsystem-foundries.

This work aims at establishing methods, techniques and design rules in order to design and manufacture microelectronics compatible microsystems.

2.2. Silicon micromachining

2.2.1. Silicon as a mechanical material

The basis of micromechanics is that silicon, in conjunction with its conventional role as an electronic material, and taking advantage of an already advanced micromachining technology, can also be exploited as a high-precision, high-strength, high-reliability mechanical material.

The silicon crystal has a diamond like lattice. Each silicon atom is positioned in the centre of a tetraeder. This atom is bonded to his four neighbour silicon atoms sitting on the corners of the tetraeder.

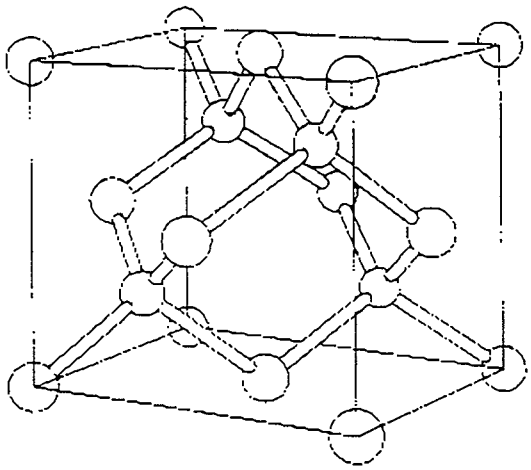


Fig. 2.2.1.1. Silicon crystal lattice

The Bravais network is face centered cubic (FCC), the reciprocal network is body centered cubic (BCC) with a parameter of $4\pi/a$ (a=5.43 °A), and the first Brillouin zone is an trench octaeder. The pattern is composed of two identical atoms, distanced of $\sqrt{3}/4$,the straight line joining the atoms is parallel to an [111] axis. The density of atoms in silicon is $n = 8/a^3 = 5\times10^{22}\, atoms/cm^3$.

The main planes of the silicon crystal, described by the Miller's indices are given by the following figure.

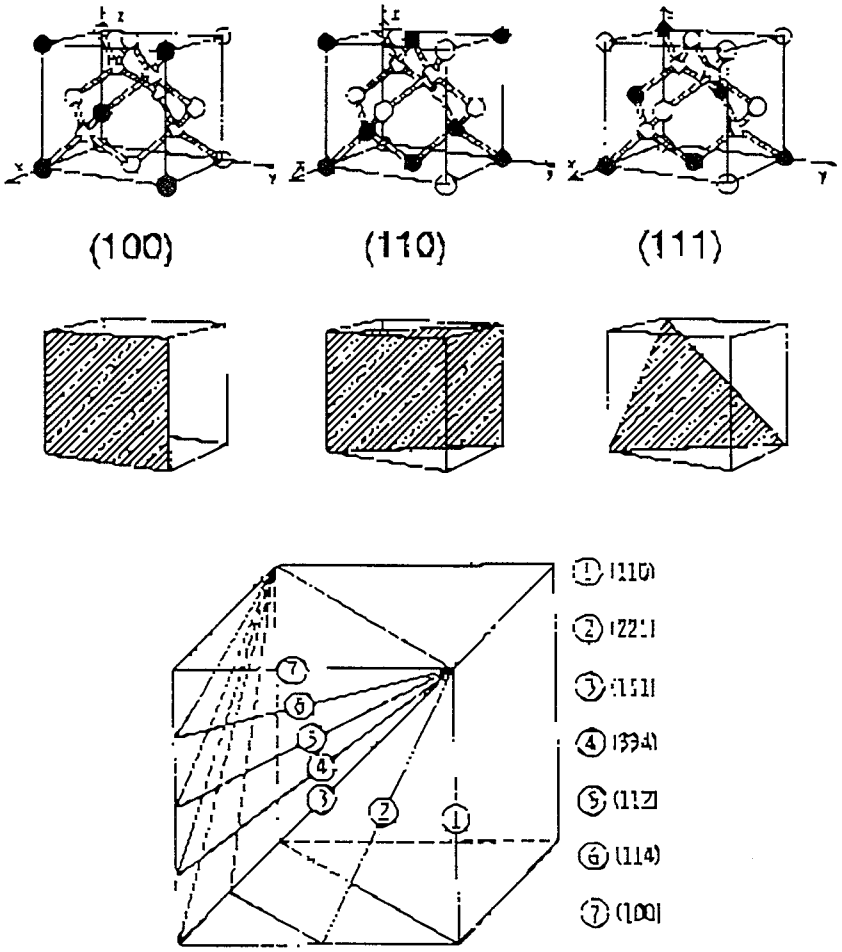


Fig. 2.2.1.2. Main crystal planes

The surface of silicon wafers corresponds in most cases to the three first planes, the others present some interest for micromechanics.

Considering a (100) P type silicon substrate (which is the most currently used kind of substrate), the wafer surface is then contained in a (100) plan. The wafer flats (see fig. 2.3.1.2) are parallel to the (100) and (111) plans intersections.

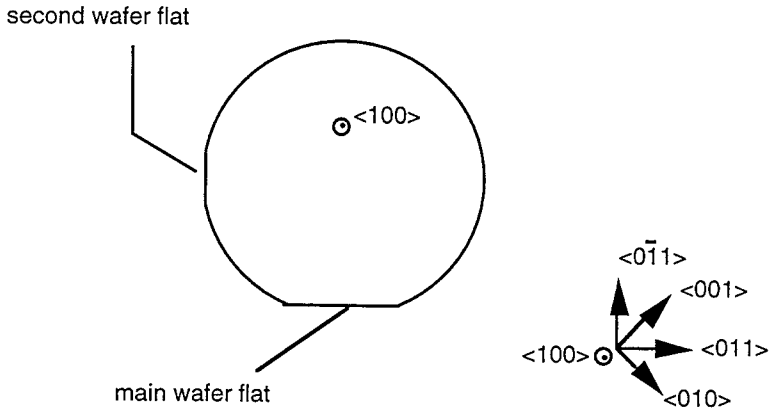


Fig. 2.2.1.3. (100) P-type silicon wafer and its wafer flats

Any mechanical microstructure made from silicon must certainly consider the mechanical behaviour of silicon. Table 2.1, appendix 2.A, gives a comparative list of its mechanical characteristics. Single-crystal silicon is not as fragile as someone can believe. The Young's modulus of silicon (1.9×10^{12} dyne/cm^2 or 27×10^6 psi) [Kel73], for example, has a value approaching that of stainless steel, nickel, and well above that of quartz and most other borosilicate, soda-lime, and leak-alkali silicate glasses [Sha58]. The knoop hardness of silicon (850) is close to quartz, just below chromium (935), and almost twice as high as nickel (557), iron, and most common glasses (530) [Wea80]. Silicon monocristalline has a tensile yield strength (6.9×10^{10} dyne/cm^2 or 10^6 psi) which is three times higher than stainless-steel wire [Kel73, Pea57]. The main difference between silicon and metals is that silicon yields by fracturing while metals usually yield by deforming inelastically. On the other hand, the silicon's thermal expansion coefficient (2.5×10^{-6} /°C) is one-fifth that of steel and its thermal conductivity is about 50 % higher than thermal conductivity of steel.

In addition, silicon is highly stress sensitive and demonstrates a significant piezoresistive effect (100 times greater than in metals). Piezoresistivity is a phenomena in which an external applied stress is manifested in a change in material resistivity.

2.2.2. A basic introduction to silicon micromachining

The fabrication of silicon compatible micromechanical structures involves the deposition, doping of the necessary material and the selective etching of the underlying support. Two main methods can be used; bulk micromachining where structures are etched in the substrate, and surface micromachining where the micromechanical layers are formed from layers deposited on the surface.

Some advantages of these micromachining techniques include VLSI circuit integration, low cost and rapid delivery.

2.2.2.1. Bulk micromachining

Bulk micromachining is a process based on etching wells in the silicon substrate, leaving suspended structures. Using this micromachining technique, devices such as micro-hotplates, infrared sources, thermal flat-panel displays, thermopiles, thermal converters, gas flow sensors, channels for fibres, and piezoresistive sensors can be developed [Kar95].

In bulk micromachining two techniques can be used : etching from the front side or etching from the back side.

2.2.2.1.1. Front-side

In the back-side bulk micromachining the structures are usually large and alignment is difficult. If the bulk micromachining is performed from the front-side this alignment problem is immediately removed and dimensions can be reduced.

The end result after processing is an open in the dioxide or nitride layer that exposes the bulk silicon surface. These chips are placed into an anisotropic etchant, such as EDP (ethylenediamine-pyrocathecol-water) or TMAH (tetramethylammonium hydroxide) or KOH (potassium hydroxide), and the exposed silicon is anisotropically etched. An isotropic etchant could also be used, such as XeF_2 (Xenon difluoride).

2.2.2.1.2. Back-side

The back-side bulk micromachining involves stopping on epitaxial layer. The etch stop often uses electrochemical techniques. The mask on the backside is of silicon nitride and special alignment techniques are required.

2.2.2.1.3. Etchants

The KOH is a commonly used etchant. KOH solutions are the most widely used due to good etched surfaces and low toxicity but compatibility with IC (e.g. CMOS) processes is not good enough. The disadvantage of this etchant is its high etch-rate of silicon dioxide. Usually a PECVD silicon nitride is used as a masking layer protected the included integrated circuits of the design.

The TMAH is IC-compatible, non toxic, has a very good anisotropic etching characteristic. The disadvantage of this solution is the high undercutting ratios which can be reduced by the addition of IPA (isopropyl alcohol).

One of the most suitable etchant for compatible bulk micromachining is the EDP. But this solution presents the disadvantage to be toxic so not easy to handle. The Hydrazine have the same disadvantage.

XeF2 is a white solid which sublimates at room temperature with a vapor pressure of roughly 4 Torr. The etch is performed in vapor phase, at room temperature, with no external energy sources, at between 1 and 4 Torr. Under these conditions, the etch is nearly isotropic and leaves a surface roughness of several microns. XeF2 is extremely selective to aluminum, photoresist, silicon dioxide and silicon nitride.

The table below gives the characteristics of these etchants.

Etchant	Suitable masking	Comments
EDP	SiO_2, SiN, Au, Ag, Cr, Ta	Toxic
TMAH (+ IPA)	SiO_2, SiN	
KOH	SiN, Cr, Au	
Hydrazine	SiO_2, SiN, Metals	Toxic & explosive
XeF_2	Photoresist, Al, Au, SiO_2, Si_3N_4, NiTi	Gas (no adhesion force)

Table 2.2.2.1.3.1. Some characteristics of major etchants

2.2.2.2. Surface micromachining

Surface micromachining is based on the deposition of thin films on the surface of the wafer and

removing one or more of these layers to release the structures.

So a surface micromachining process requires a sacrificial layer which is removed at a later stage (in the post-processing operation) to release the mechanical part. Many materials are used as a sacrificial layer, such as : silicon oxide, polysilicon, porous silicon, aluminium, etc., each requiring a specific etchant.

Usually, silicon dioxide sacrificial layers are the most used and are removed by wet etching in HF. There are various type of oxide (Thermal, LPCVD [LTO, PSG, BPSG], PECVD) having each advantages and disadvantages in term of quality, etch rate, thickness uniformity, etc.

The micromechanical layer is normally polysilicon or nitride. Polysilicon is a material frequently used for both electronics and sensors and a lot of studies have been achieved for its electrical and piezoresistive properties. Nitride is the second main material used as a mechanical layer since it is a mechanically strong material with low optical absorption. The stress level in both materials are highly dependent upon both deposition parameters and subsequent thermal processing.

Another typical sacrificial layer is polysilicon which has the advantage to be etched by EDP without any supplementary mask. In that case, nitride is used to realize the mechanical layer.

2.2.2.3. Summary

The table 1.4.2.1 illustrates the silicon compatible micromachining .

Technology	Surface Micromachining	Bulk Micromachining
Sacrificial layer	Silicon dioxide or polysilicon	Silicon substrate
Post-processing operation	Isotropic wet etching by HF or EDP etching	Anisotropic etching by EDP, TMAH or KOH
Applications	-Pressure sensors, accelerometers, etc (capacitive sensors) - Actuators (micromotors, comb drive actuators, etc)	- Thermal sensors - Gas flow sensors - Thermopiles - Thermal pixels - Pressure, force sensors (piezoresistive)

Table 2.2.2.3.1. Silicon compatible micromachining

2.2.3. Micromachining techniques compatible with IC processing

2.2.3.1. Silicon anisotropic etching principle

One of the most powerful and versatile tool to realise microstructures still etching. Chemical etching for silicon are numerous. They can be isotropic or anisotropic, doping dependent or not, and have different degrees of selectivity for silicon which will determine the choice of the masking layers. We will not discuss hereby plasma, reactive-ion etching, or sputter etching, although these techniques are being to be widely used to perform microstructures.

Since the technology addressed in this thesis is IC compatible bulk micromachining, where suspended bridges, cantilevers and membrane are performed monolithically with the electronic circuits, by front-side bulk micromachining, we will mainly target in this section anisotropic etching of silicon and emphasis on compatibility with ICs. A general design theory will be given which results of a number of design rules implemented in the design kit detailed in chapter 3.

The silicon anisotropic etching principle allows the fabrication of suspended structures. This gives the structures a certain mobility and an isolation with respect to the other devices integrated on silicon.

During an anisotropic etching, the silicon monocrystal is not attacked with the same speed in every

direction : the etching speeds depend on the crystallographic plans and generally decrease in the following order : (100)>(110)>(111). TMAH (tetramethylammonium hydroxide), EDP and KOH (potassium hydroxide) etching solutions follow this rule. For aqueous KOH at 100°C, for instance, (110):(100):(111) etch-rate ratio equals to 50:30:1. A partial explanation of this phenomenon is that these planes have higher silicon atoms density, as illustrated on the figure 2.2.3.1.1.

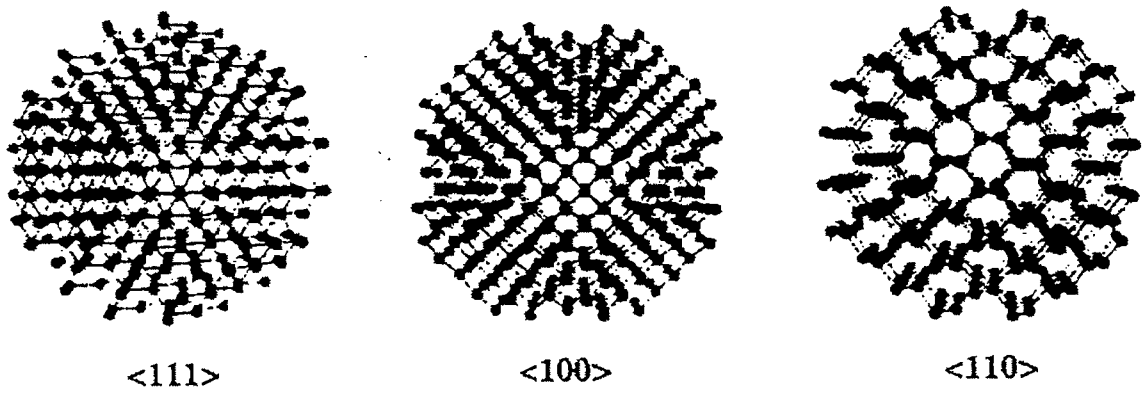


Fig. 2.2.3.1.1. Orthogonal view through the main planes of the silicon crystal

The etched cavities formed are limited by (111) plans, which are the slowest plans etched (see fig. 2.2.3.1.2 and 2.2.3.1.3).

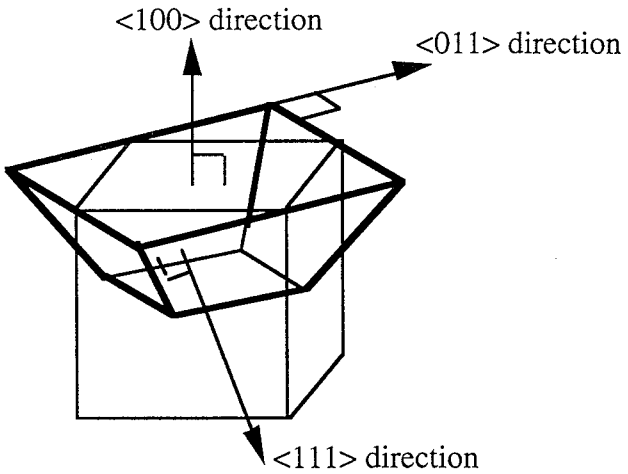


Fig. 2.2.3.1.2. Microscopic consideration of the etching.

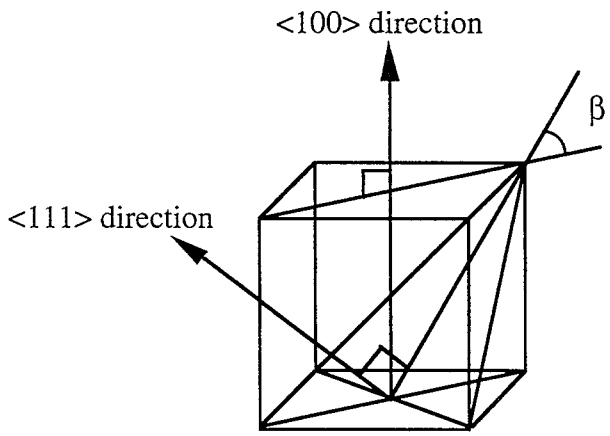


Fig. 2.2.3.1.3. $\tan\beta = \sqrt{2}$

The principle used to achieve suspended structures is detailed in the following sections and is formulated in the form of design rules. With these concepts, the design layout of any structure can be achieved with CMOS compatible front-side bulk micromachining.

2.2.3.2. Design theory

When designing micromachined structures using front-side bulk micromachining, there are some basic concepts to consider, particularly related to the resulting cavity of a single or multiple open area within the mask layer (e.g. open area within the passivation layer when considering EDP etching).

2.2.3.2.1. The resulting cavity of a single open area

The resulting cavity of a single open area takes the shape of an inverted pyramid (or truncated inverted pyramid) with a base being the smallest aligned square (or rectangle) which can enclose the vertices of the defined.

Inverted pyramids (truncated or not) which sides are included in (111) plans, and which bases are rectangles contained in the (100) plan, are obtained by anisotropic etching of monocrystalline silicon, even if the mask has not a rectangular shape (see fig. 2.2.3.2.1.1, 2.2.3.2.1.2 and 2.2.3.2.1.3).

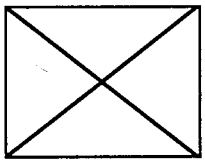


Fig. 2.2.3.2.1.1. Pyramid formed in the silicon etched through a rectangular mask.

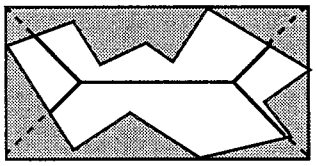


Fig. 2.2.3.2.1.2. Pyramid formed in the silicon etched through a mask of any form.

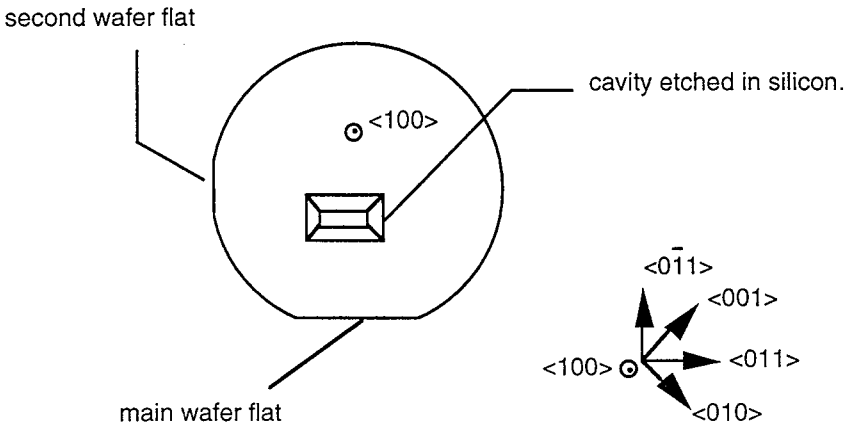


Fig. 2.2.3.2.1.3. Cavity alignment with the wafer flats.

As illustrated in fig. 2.2.3.2.1.2, the resulting cavity of an anisotropic etching in monocrystalline silicon will take the shape of an inverted, rectangular based pyramid, even if the mask through which the etching is done has not this form : the base of the pyramid will then take the shape of the smallest rectangle including the opening of the mask, and which sides are parallel to the wafer flats.

These exposed silicon areas determine the places where monocrystalline silicon will be anisotropically etched and hence will define the generated cavities. These open areas can be created with the superposition of the following masks, as defined on fig. 2.2.3.2.1.4 :

- active area,
- contact cut,
- via,
- passivation opening.

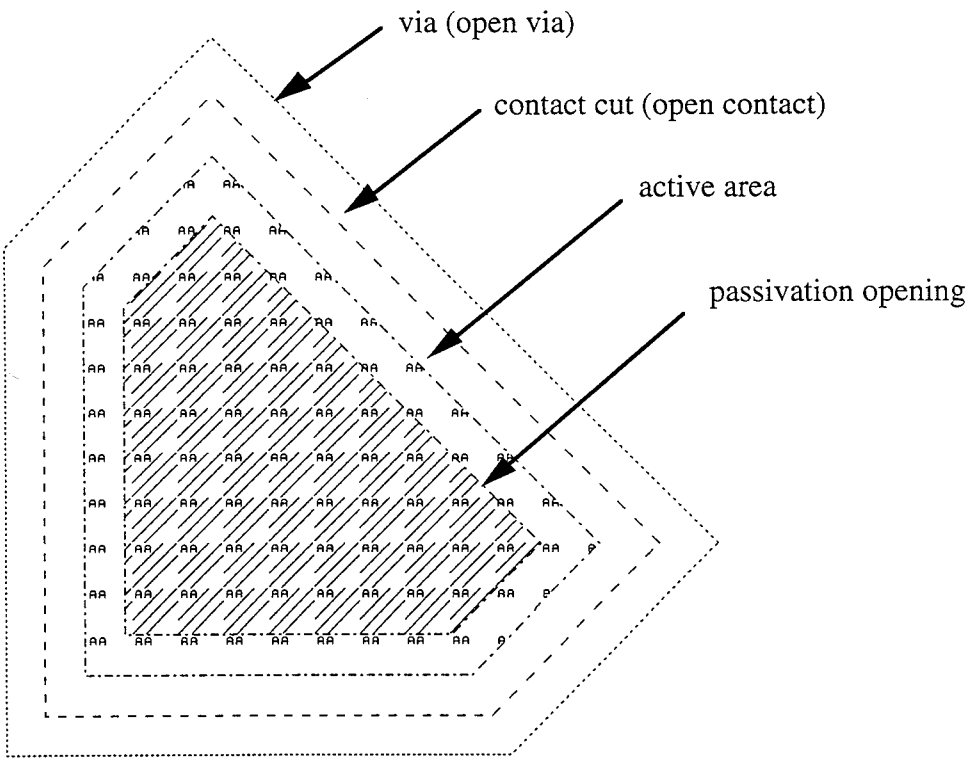


Fig. 2.2.3.2.1.4. Superposition of the masks to define an exposed silicon area.

No other mask level can be present inside the area defined by the masks above since at the end of the CMOS process, exposed silicon, will be directly etched.

2.2.3.2.2. The resulting cavity for multiple open areas

For two or more open areas defined in close proximity, the rule is basically based on whether the cavities resulting from each of the open area merge or remain distinct. Thus, the methodology is described by the following : apply the rule of the one open area to draw the smallest enclosing rectangle around each individual area, then if none of these resulting rectangles intersect, so the cavities remain distinct and are defined by the first rule. If any of the enclosing rectangle touch, then during the anisotropic etching, the cavities defined by these enclosing rectangle merge to produce an inverted pyramid or a truncated pyramid with a base which is the smallest aligned square or rectangle which encloses all the vertices of the individual open area which produce the intersection.

The figure 2.2.3.2.2.1 illustrates this rule for two open areas where the enclosing rectangles intersect. The anisotropic etching produces an inverted pyramid and thus suspends the bridge.

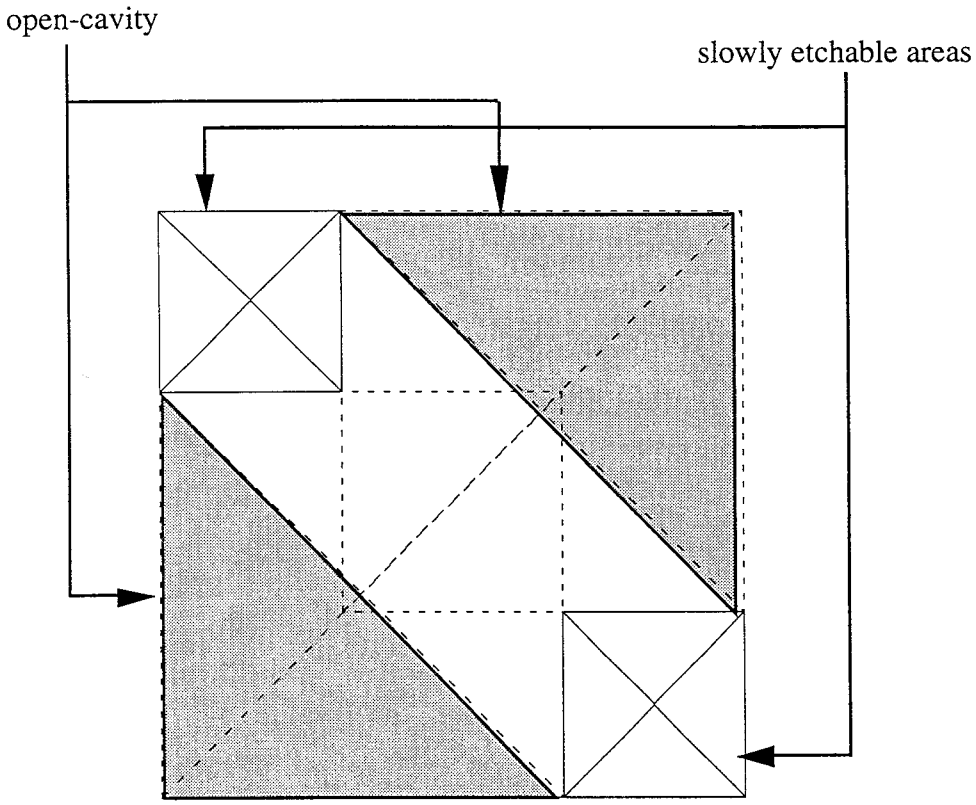


Fig. 2.2.3.2.2.1. auto generation of the open-cavities (each open-cavity is attached to one open area) and of the slowly etchable areas (areas that may be difficult to etch in normal etching conditions)

2.2.3.3. CMOS compatible front-side bulk micromachining

CMOS technology can be represented as a set of layout design rules to be followed in order to fabricate IC chips. Many micromechanical structures can be fabricated by implementing unconventional layout designs in CMOS standard technology without altering the process sequence. As long as the design rule violations don't alter the process sequence, the design can be implemented by an industrial CMOS process. In the frame of this thesis, the foundry process considered is the ES2 - ATMEL process, particularly, the 1.0μ CMOS, Single Polysilicon Layer and Double Metal Layer.

It is important to understand that the ES2 process is primarily intended for manufacturing digital electronics - not MEMS. It's a single polysilicon layer, double metal layer process. This means that MEMS design and fabrication can be done only to the extent that the metal, semiconductor, and dielectric films are used **exactly** as they are made for the integrated circuits: electrically, compositionally and mechanically. These layers have all been optimized with high-yield, robust IC manufacture in view and not with structures or sensor technology in view. It is unlikely that any CMOS process can be used to make thick polysilicon based microsystems devices, such as micromotors. On the other hand, this process can be used to make metal and silicon dioxide/silicon nitride (the passivation layer is a silicon dioxide, silicon nitride mixture which thickness is about 1.5μ) structures, and provides the opportunity to integrate them with high-performance 1.0μ CMOS circuitry.

Simply, the designer must know that he's restricted to thin polysilicon layer (approx. 0.5μ), but can use thick glass and metal layers as free standing structural elements.

2.2.3.3.1. The fabrication methodology

An important consideration when developing a sensor or an actuator with in-built signal processing is

to first establish from where the compatibility problems may arise.

In a monolithic solution, the compatibility factor can be considered in two different ways : the first one is to study the compatibility of the process with the clean room and the second is to achieve the compatibility between the sensor and the integrated circuits. In the case where the process is not compatible with the clean room then this can be carried out only in a post-processing phase. This is the solution normally applied, and particularly in our case, to the EDP etching used to release the structures. The second problem is that of compatibility of the micromachining steps with the electronics.

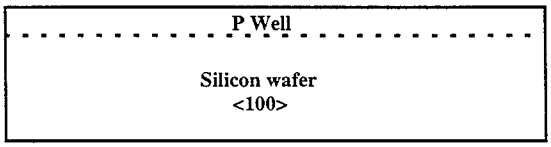
In our case, the structures and the electronics are both fabricated in the same production flow chart. In the end of the CMOS process achieved on a conventional production line (in our case ES2 - ATMEL), the electronics and the structures are fabricated monolithically but the structures are not released. The structures, then are suspended by anisotropic etching operation, outside of the foundry.

Concerning the anisotropic etching operation, we applied to the structures two solutions : TMAH and EDP. The reason for which we didn't consider KOH, except in the beginning phase when we wanted to release the structures without any care to the electronics, is that we wanted to make the post-processing operation as simple as we can to guarantee the yield. This means that we wanted to perform a maskless etching without any supplementary masks bringing to the operation more complexity and additional costs.

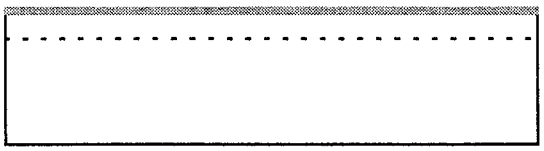
The results of the etching by both TMAH and EDP is detailed in the next section. However, the best results were obtained by the EDP etching.

The following figures show the main technological steps of the monolithic fabrication of a micro-bridge (structure) and an inverter (electronics).

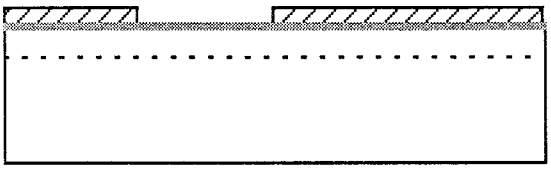
Step 1 : Epitaxy



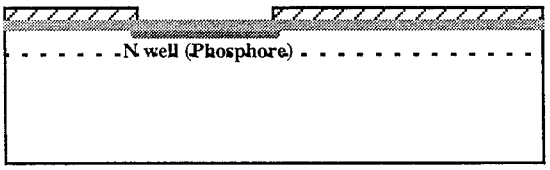
Step 2 : Oxidation



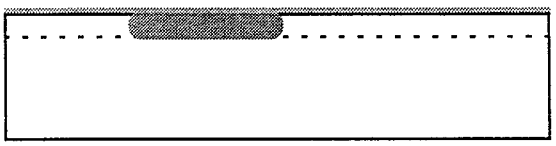
Step 3 : - Photoresist deposition
- Exposure
- Development



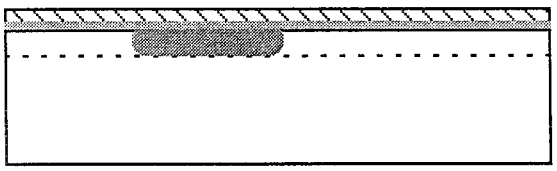
Step 4 : Ion implantation



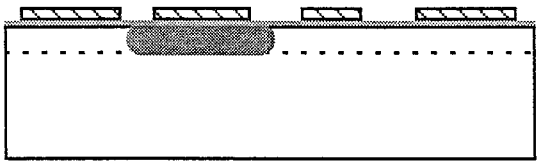
Step 5 : - Photoresist elimination
- Annealing (1200 °C)



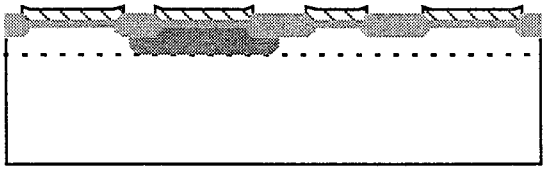
Step 6 : Silicon nitride deposition



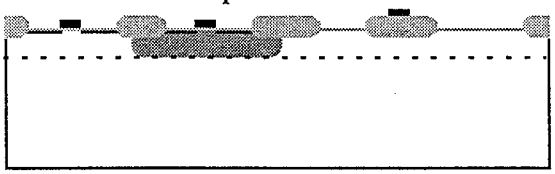
Step 7 : - Photoresist deposition, active zone exposure, development
- Silicon nitride etching



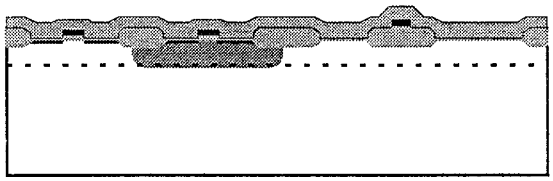
Step 8 : - Photoresist elimination
- Field oxidation



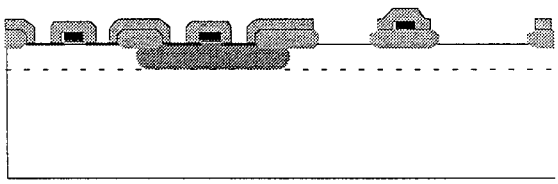
Step 9 : - Silicon nitride elimination
- Polysilicon deposition & etching
- N^+ and P^+ dopant



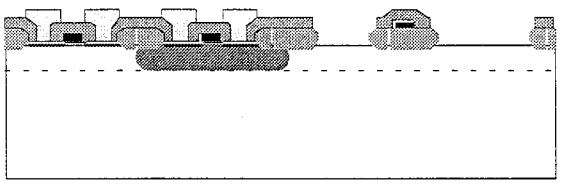
Step 10 : Oxide deposition



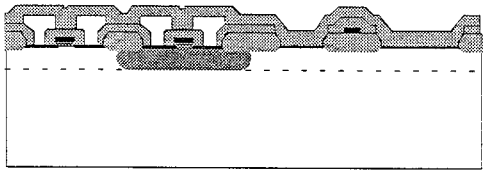
Step 11 : Contact opening



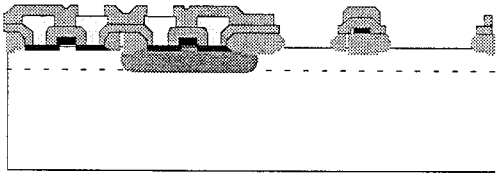
Step 12 : Metal 1 deposition and etching



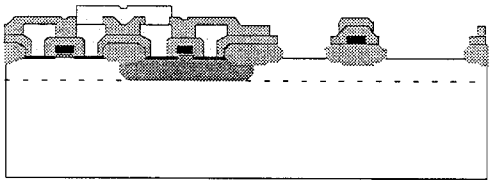
Step 13 : Oxide deposition



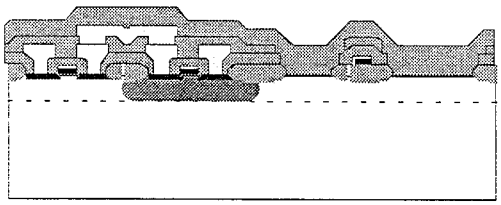
Step 14 : Vias etching



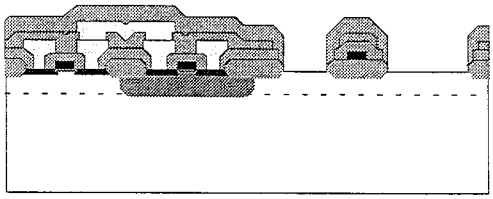
Step 15 : Metal 2 deposition and etching



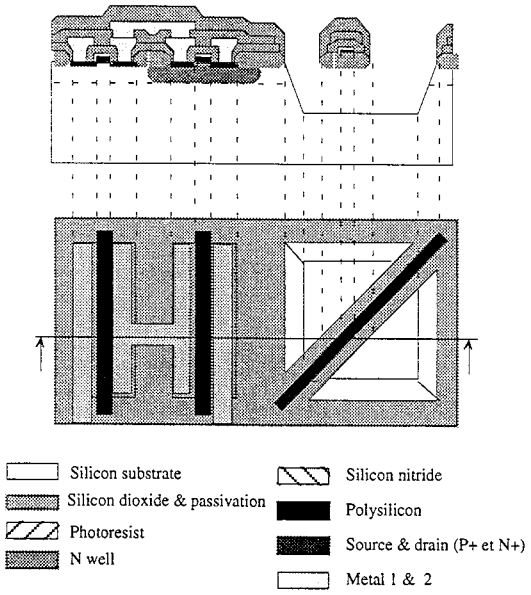
Step 16 : Passivation layer deposition



Step 17: Opening in the deposition layer



Step 18 : Silicon etching (post-processing operation)



2.2.3.3.2. The post-processing operation - EDP and TMAH etching

In this section, we will study the etching operation used to release the structures and performed using TMAH and EDP. As, we mentioned above, these solution were considered for the compatibility that can present with the electronics.

The choice of EDP is due to the fact that silicon dioxide (SiO_2) and aluminum (Al) can be used as a masking materials. During the etch time, the etchant does not attack the surface of the CMOS chips covered by the silicon dioxide and silicon nitride (Si_3N_4) mixture for passivation or the exposed bond pads (more 95 % of aluminum). Therefore, the only areas exposed to the etchant are the open areas defined in the design phase. These elements allows a maskless etching procedure for realizing the suspended structures in standard CMOS process.

The EDP solution contains 1000 ml ethylendiamine, 160 g pyrocathecol and 133 ml DI water. Using this solution, the <100> planes are etched at a speed of approximately 30 µm / h and the <311> planes at the speed of 15 µm / h. The etch rate is slower in the <111> direction compared with the <100> direction by an approximate ratio of 1:35.

The following figure shows that have been post-processed by EDP [Cou96]. This operation shows a complete compatibility with the CMOS process (particularly the ES2-ATMEL 1.0 µ and 1.2 µ CMOS SLP/DLM). The integrated circuits has been tested and kept all the electrical parameters unchanged. The maximum etch-time for the considered solution for which the compatibility with the electronics is insured is 5h30min.

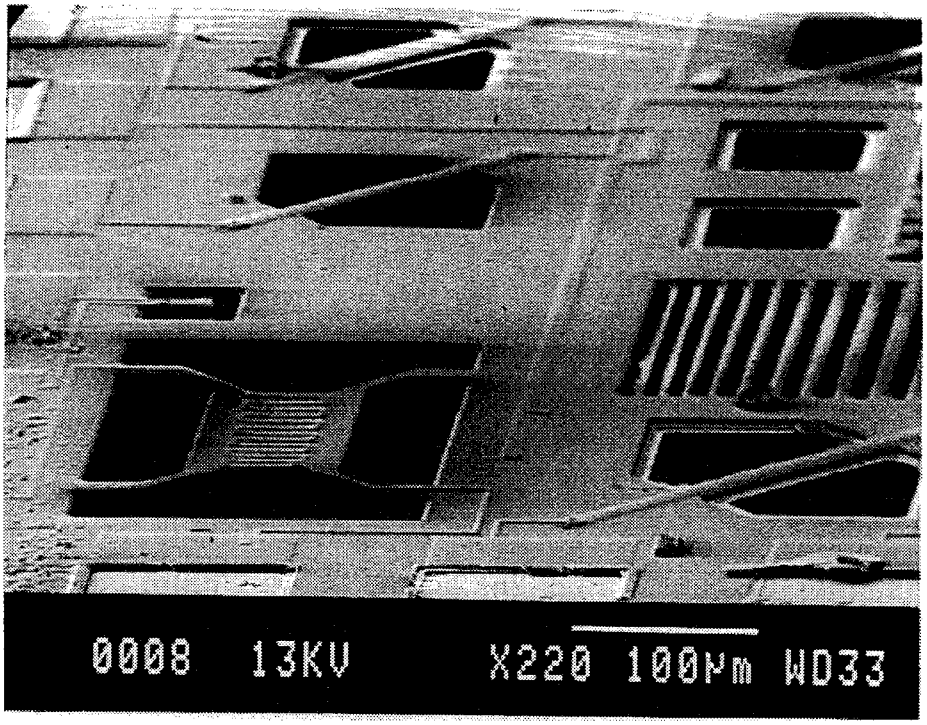


Fig. 2.2.3.3.2.1. SEM photograph of the main structures fabricated monolithically with ICs using front-side CMOS bulk micromachining

When the chips come out from the CMOS processing, the open areas may present some residual silicon dioxide that is eliminated by a 10 seconds wash in hydrofluoric acid (HF) solution. The figure 2.2.3.3.2.2 illustrate these problems.

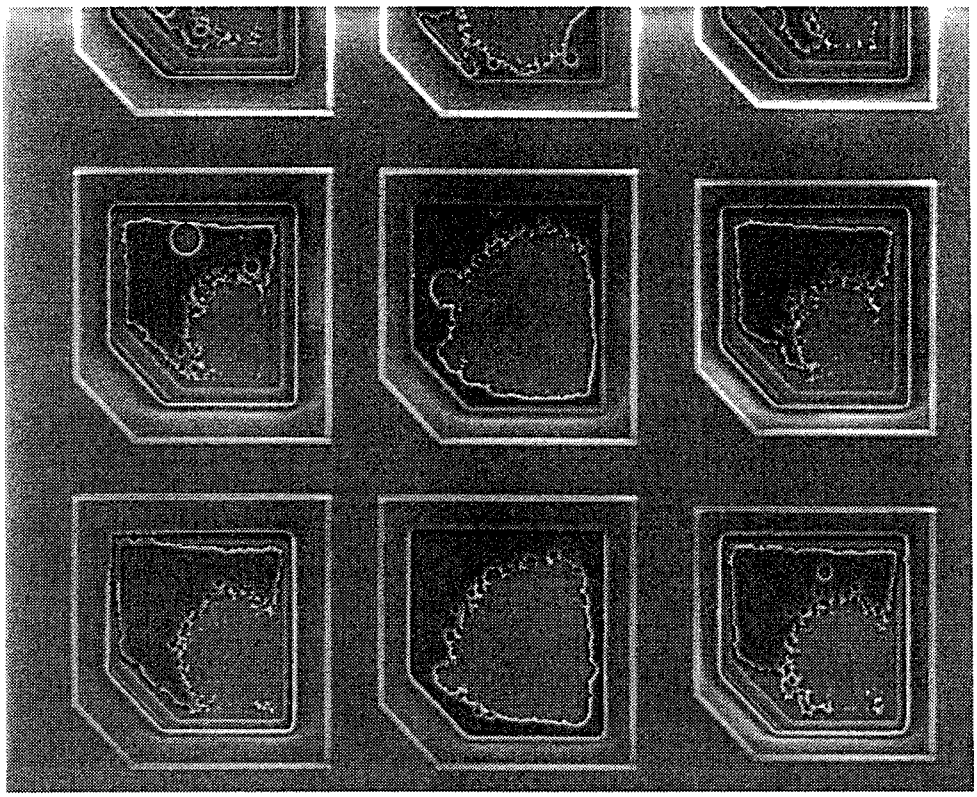


Fig. 2.2.3.3.2.2. Residual silicon dioxide remaining in the open areas after the CMOS processing

In the other hand, the TMAH based solutions were considered for the CMOS compatibility

requirements and easy handling. Silicon nitride and thermally grown silicon oxide show high selectivity. Si_3N_4 etch rates are lower than 20 A°/h and SiO_2 etch rates are below 100 A°/h for the considered solution (20 wt.%). Low temperature deposited silicon oxide etch rate increase up to 400 A°/h.

However, the bonding pads were severely damaged by the TMAH attack as presented in the figure 2.2.3.3.2.3. This bubbling phenomena is due to the fact that neither metal 2 or metal 1 is pure aluminum but a composition which is relatively etched by the solution.

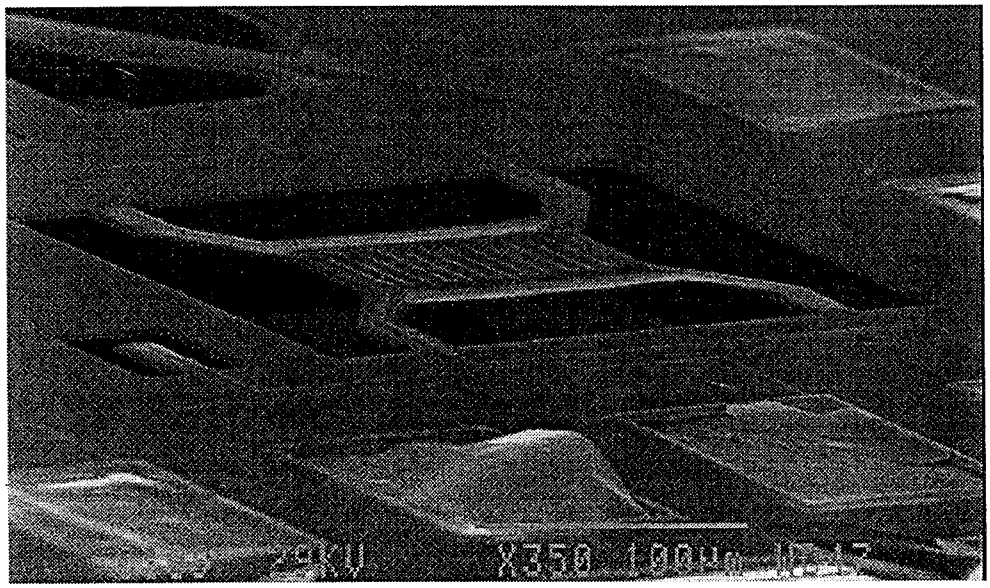


Fig. 2.2.3.3.2.3. SEM photograph of different structures etched by TMAH (the pads have suffered from the attack)

2.2.3.3.3. Example of elementary structures used to perform sensors and actuators

Designs regrouping mechanical structures, such as bridges, membranes, cantilevers, pixels, and integrated circuits have been fabricated and successfully tested. These structures that have been manufactured using the methods and techniques detailed above, are used to perform piezoresistive sensors, thermopiles, gas sensors, gas flow sensors, thermal sensors, thermal pixels and others.

2.2.3.3.3.1. Cantilever structure containing N-doped polysilicon piezoresistors

A common geometry for MEMS sensing and actuation devices is that of the cantilever beam structure. In this structure, either polysilicon beam or a glass/nitride beam is freed from a surrounding matrix by a chemical etch. The underlying crystalline substrate is often etched away as well to permit large amplitudes of movement. Figure 2.2.3.3.3.1.1 is a SEM photograph of a free-standing silicon dioxide cantilever structure containing piezo-resistive polysilicon lines etched by EDP in an ES2 1.0µ CMOS processed chip.

Certain actuating and sensing elements can be incorporated within the cantilever structure as can been seen by a n-doped polysilicon resistor line encapsulated in glass meandering back and forth along the length of the beam. This element can be viewed as either a sensing or actuating layer. For example, since it is piezo-resistive, any flexing of the beam which strains the polysilicon induces a change in the resistance which can be detected electrically. With this transducer, the position of the beam can be accurately determined. Two possible applications are for inertial detectors such as an accelerometer, and a tactile sensor.

The polysilicon can be used as a resistive heater which in turn produces movement for an actuator

application, or for a resonator sensor. Since the cantilever is a multilayer structure consisting of layers of different thermal expansion coefficients, raising the surface temperature by Joule heating will change the moment of force applied to the beam and hence its deformation. Heating and cooling can cause the beam to move up and down. One application of this movement is to cause electrical contacts to be opened and closed, another application is a resonant accelerometer.

This structure can also be used to realise thermopiles where thermocouples could be realized by Seebeck heterojunctions between aluminium and polysilicon in series. This could serve to produce an IR electro-thermal sensor. A bridge or membrane structure is also used to realise such devices and have the advantage to be more robust than cantilevers. Also, combining a polysilicon heater to the design to heat the tip of the cantilever beam and one set of the thermojunctions, compared to the junctions at essentially ambient temperature on the heat-sinked wafer, produces a standard thermopile micro-gas flow sensor.

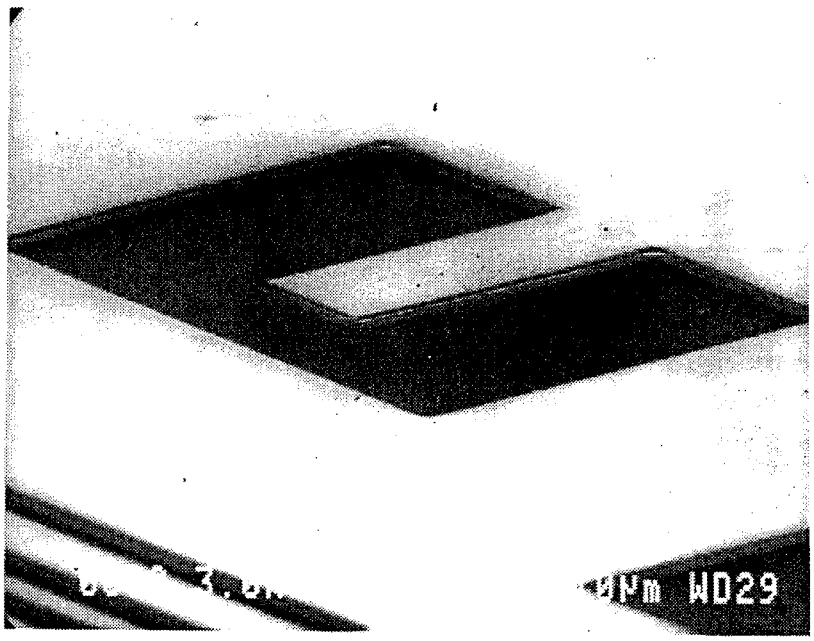


Fig. 2.2.3.3.3.1.1. SEM photograph of a free-standing silicon dioxide cantilever structure containing piezo-resistive polysilicon lines

2.2.3.3.3.2. Thermal pixel

Figure 2.2.3.3.3.2.1 shows a micro-heater structure that is used as an infrared point source and an IR pixel for thermal display. It was fabricated with a CMOS 1.2μ process from ES2. The thermally isolated resistor shown in the figure was brought to incandescence by applying 5 volts across the resistor which caused a current flow of 8 mA. The low power of 40 mW can produce incandescence because heat is not absorbed by the underlying silicon substrate. The radiative intensity can be controlled by the drive current. This device has possible applications in the area of dynamic thermal scene simulation.

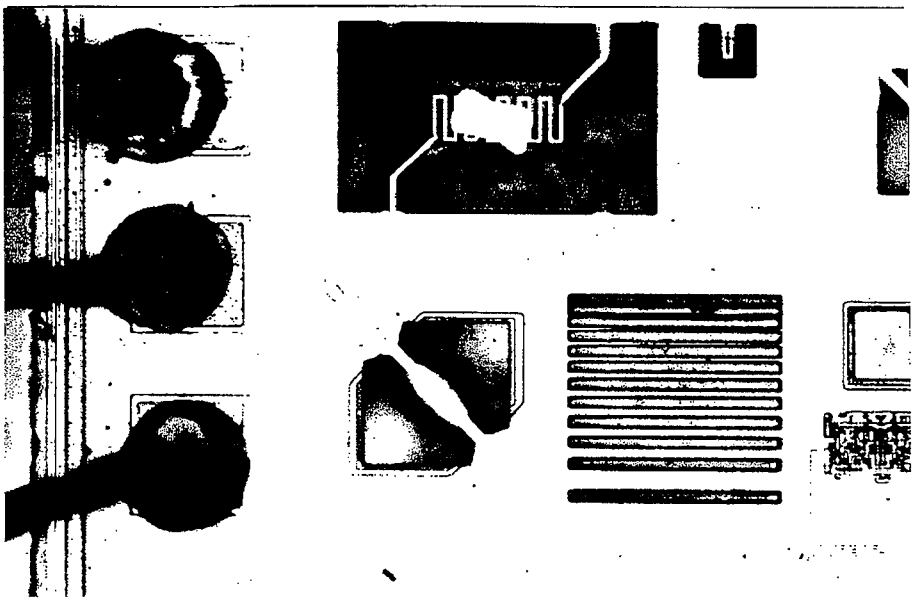


Fig. 2.2.3.3.3.2.1. A photomicrograph of the infrared-point-source pixel operating at incandescence

2.3. Gallium arsenide micromachining

2.3.1. Gallium arsenide micromechanics

GaAs is of many people regarded as being too difficult and expensive for a sensor or actuator application. It is a fact that GaAs is not cheap in comparison with silicon and also it cannot currently be produced with as high purity and few crystalline defects as Si. Therefore, it is preferable to use GaAs where and when one can take advantage of the good properties that it possesses. Possible applications could be where high working-temperature, high frequency, integrated optoelectronics or piezoelectricity are demanded. The following section treats the advantages and disadvantages of gallium arsenide as a micromechanical material in comparison with silicon and quartz. The properties of $Al_xGa_{1-x}As$ are also considered in the comparison since $GaAs/Al_xGa_{1-x}As$ heterostructures are commonly used in, e.g. in HEMT's and lasers.

2.3.1.1. Mechanical and thermal properties

a) Band Gap

As opposed to silicon, GaAs has a direct band gap, which is an interesting property that offers the possibility of integrating optical devices monolithically. GaAs with its rather large band gap (1.4eV compared with 1.1eV for Si) has the ability to be semiconducting at higher temperatures than silicon. GaAs-based electronics have been realized for temperatures up to at least 350°C [Fri89, Fri92], whereas Si transistors can at most reach 200°C. Possible applications are in monolithic integration of preamplifiers for active sensors. SiC has an even wider band gap than GaAs, and SiC-transistors have recently been found to function at temperatures up to about 800°C. Still, since this is an immature technology, it is not clear if it can be possible to develop it satisfactorily with SiC.

b) Fracture strength and fracture toughness

GaAs is a brittle material and it will deform elasticity until brittle fracture. The fracture strength (σ_f) is proportional to the fracture toughness (K_{Ic}), and is limited by the largest stress concentration, i.e. often the largest defect. Therefore, when the mechanically active volume decreases the probability of a strong structure increases. A rough estimate have shown that for a penny-shaped crack, with a

radius c, the fracture strength can be written [Hjo94]:

$$\sigma_f = 1.6 K_{IC} (c\pi)^{-0.5}$$

This estimation of the possible fracture strength could be used to approximate quantitatively how large effects defect sizes that can be accepted for a mechanical application. As shown in table 2.1 in appendix 2.A, GaAs has a higher mechanical strength than quartz, but just half the value of Si. Still, the fracture strength of GaAs, 2.7 GPa, should be compared to the one of construction steel, which is normally below 1 GPa.

c) Piezoelectricity

The crystal of GaAs has a zinc blende structure (figure 2.3.1.1.1). This crystal structure is built up by two face-centered cubic (fcc) lattices, one from the group III (Ga) and the other from the group V (As) of the periodic system, displaced by a lattice-vector < 1/4, 1/4, 1/4>. Because of this structure, GaAs possesses no centre of symmetry and it is therefore piezoelectric. Silicon with its symmetric diamond structure is not piezoelectric whereas quartz on the other hand is. Quartz when used as a reference resonator shows an extremely low temperature dependence and is therefore used as tuning forks for frequency control in watches. This is not possible in GaAs and the main reason is that its elasticity changes with the temperature [Hjo94]. Moreover, the piezoelectric coefficients of GaAs and AlxGa1-xAs are smaller than for quartz. However, piezoelectric quartz lacks the possibility of having driving and sensing electronics on the same substrate as the resonant structure and there is no etch-stop technique for control of etched thickness.

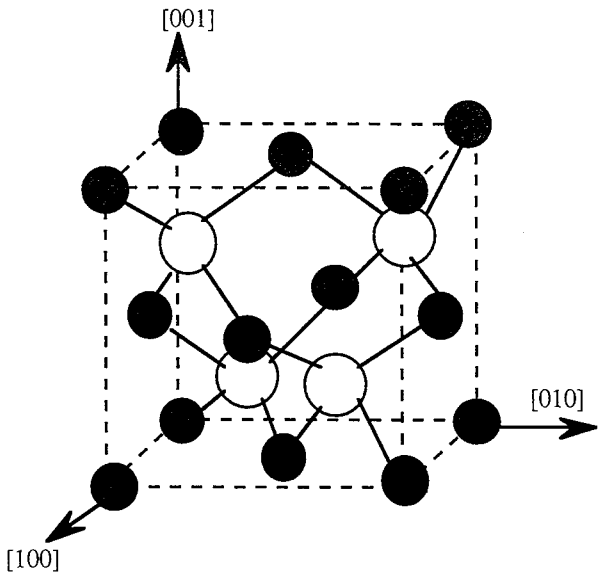


Fig. 2.3.1.1.1. Conventional unit cube for GaAs, zinc blende structure

d) Piezooptic response

When applying asymmetric stress, the crystal symmetry changes, thereby influencing the refractive indices of the crystal. This response is known as the piezooptic effect. GaAs and AlGaAs have about the same piezooptic response as silicon.

e) Piezoresistivity

The piezoresistivity for most metals exhibits a Gauge factor ($G = \Delta R/R_0\varepsilon$, where ε is the strain) of about 1-2. Low-doped silicon can reach ~200, but typical values of the Gauge factor in silicon microsensors are 50-90. The piezoresistive effect in silicon is due to a strongly affected average mobility by application of strain. GaAs and its ternary $Al_xGa_{1-x}As$ show a more complicated combination of different mechanisms. In GaAs (and $Al_xGa_{1-x}As$) there are mainly four of them that have a piezoresistivity response. The first is the observed mobility change due to the change of the electron effective mass with pressure ($G \cong 10$) [Rob91]. The second is a pressure-induced transfer of electrons from the high mobility band gap minimum to low mobility minima X or L, where the energy will not be equal to the others. In $Al_xGa_{1-x}As$ the energy of respective bandgap minimum will change with the composition ($G \cong 100$) [Fri92, Zil91],. The third response mechanism is the pressure-induced freezing of electrons to deep level impurity states, DX ($G \cong 400$) [Fri92]. The fourth response mechanism uses the stress-gradient induced piezoelectric bound charges to change the resistivity in a diffused resistor. By adding stress gradients amplifying stripes on each side of the resistor, a Gauge factor of about 130 has been measured[Hua93].

f) Mechanical endurance

The ability of GaAs to endure wear, thermal shock, and fatigue is inferior to both quartz and silicon. This is due to a lower hardness, a low thermal conductivity, less stable oxides, and environmentally enhanced fatigue in e.g. water. For AlAs the fracture toughness is so high (table 2.1, appendix 2.A) that it should compensate the low hardness and have a higher endurance. Since AlAs is rather chemically reactive, contact with the environment should be avoided. A good compromise between mechanical endurance and chemical reactivity can be obtained for $Al_xGa_{1-x}As$ with x less than 0.50. When it comes to ageing, quartz is superior to the others, having nearly no movable atoms in the crystal, whereas silicon and GaAs have impurity atoms that will slowly diffuse, and there is also a certain oxidation that in the long run changes their dimensions. Moreover, as opposed to silicon, GaAs has no stable oxides and nitrides of high quality.

g) Stiffness and elastic modulus

As shown in table 2.1, appendix 2.A, GaAs and quartz are not as stiff as silicon. This property can be considered as good or bad depending upon the application. The elastic modulus for GaAs is 30% lower than it is for Si. This fact implies e.g. that a beam of GaAs but with otherwise equal dimensions demands an 11% increase, compared to silicon, in thickness for the same bending stiffness. The elastic behaviour of GaAs, as for all single crystalline materials, is anisotropic.

h) Thermal resistivity

The thermal resistivity in GaAs and AlAs is much higher than it is in Si, as shown in table 2.1, appendix 2.A. Figure 2.3 shows the thermal resistivity as a function of composition x for $Al_xGa_{1-x}As$ alloy, after Adachi [Ada85]. The solid line is a theoretical fit to the experimental data (the circles). Of special interest is $Al_{0,48}Ga_{0,52}As$ which exhibits a thermal resistivity of more than ten times the one of Si. Whether this can be regarded a good or an unwanted property depends upon the application, e.g., the bolometer, which is an energy-detector based upon a change in the resistance of

a material exposed to a radiation flux. In this application it is obvious that a sensor fabricated in AlGaAs could be much more sensitive than a sensor realized in silicon. On the other hand, this property could be fatal in applications where a temperature independence is sought.

i) Summary and conclusion

A summary of data for GaAs [Ada85], AlAs [Ada85], Si [INS88] and quartz [Tri80] can be found in table 2.1, appendix 2.A. As found in this table, the lattice difference of GaAs and AlAs is very small, enabling good quality heterostructures of AlxGa1-xAs alloys without high strains in the films.

It has been found that GaAs offers properties that silicon lacks, i.e. direct band gap and piezoelectricity. Furthermore, although GaAs has a lower mechanical strength than silicon, the fracture strength is about three times as high as construction steel. Therefore, it should be sufficient for sensor and actuator applications. Also, piezoresistive Gauge factors up to 400 and thermal resistivities up to 14 times higher than for silicon are obtainable in the AlGaAs system. Finally, the higher bandgap of GaAs and AlGaAs allows higher working temperatures than for silicon.

Considering the properties of GaAs and AlGaAs, these semiconducting materials may be a very good choice in micromechanical applications.

2.3.2. Gallium arsenide micromachining

In this section, the VITESSE MESFET (MEtal Schottky Field Effect Transistor) foundry-process that will be used to realise GaAs based microsystem will be briefly presented. This presentation is followed by an overview of etching processes of GaAs that can be used in post-processing operation to suspend the structures fabricated in the MESFET flow. Finally, the fabrication of the suspended structures using the MESFET process is detailed.

2.3.2.1. Vitesse MESFET

The Vitesse MESFET foundry process is characterized by a 0.6µm effective gate length. As can be seen in figure 2.3.2.1.1, the transistor consists of a GaAs substrate where the channel, source and drain have been ion-implanted. There are two versions of this transistor. One can operate up to 100°C and the other over a wider temperature range from -55°C to +125°C. These values will become the working-limits for a sensor integrated in a Vitesse MESFET process.

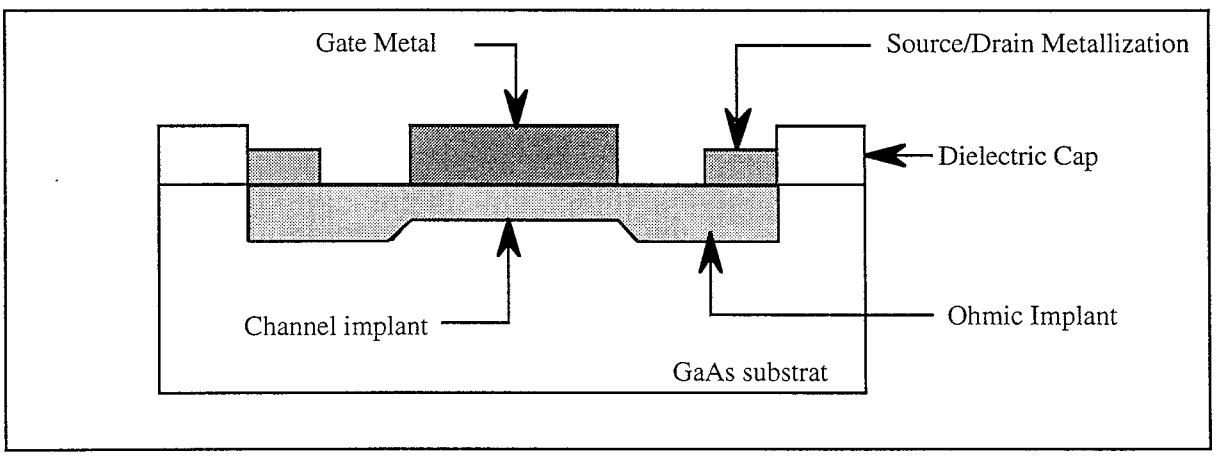


Fig. 2.3.2.1.1. The Vitesse MESFET

2.3.2.2. Etching processes

Etching processes commonly used in microstructuring can broadly be divided into two groups : wet etching and dry etching. A wet or liquid-based etching process could be enhanced by the galvanic effect or by an external supply of electrons (anodic etching). Dry etching is a term for all processes where no liquid is involved. Processes that are basically chemical in nature, but are in need of some surface exciting processes, e.g. in plasma induced etching, RIE and reactive ion beam etching (RIBE), also fall under the category of dry etching.

2.3.2.2.1. Wet etching

Most etchants for GaAs contain an oxidizing agent, a complexing agent, and a diluant, such a water. The oxidizers usually used are $Br_2H_2O_2$ and HNO_3. The oxidized layer is often insoluble in water, and is made soluble by a complexing agent such as H_2SO_4, HCl, NH_4OH, Na OH, HF or citric acid, $C_3H_4(OH)(COOH)_3H_2O$.

GaAs and its related compounds are of zinc blende structure. This makes the etching mechanisms in GaAs differ significantly from those in silicon, which has a diamond structure. For a qualitative understanding of the etching mechanisms in GaAs, consider figure 2.3.2.2.1.1. If assuming electric neutrality, the surface (111) plane atom has one or three bonds to neighbouring atoms under it, the (100) plane atom has two, and the (110) plane atom has one bond to the plane under it and two bonds to neighbouring atoms in the same plane. As shown in figure 2.3.2.2.1.1 the (111)-planes are grouped together two and two with larger distances between the groups. The bonds between the groups are naturally weaker, and are therefore those broken at the surface. This causes a difference in etching rate depending on the direction ; either the surface atoms will be mainly arsenide atoms, (111) As, or they will be mainly gallium atoms, (111)Ga. The gallium atom has three bonding electrons, and the arsenic has five. The more dangling bonds a surface atom has, the more reactive it is. With the aid of arguments like this, one can explain the differences in etching rates which experimentally are found to increase as (111)Ga < (100), (111)As < (110). The consequences of this orientation-dependant etch rate in the GaAs crystal, when the etch is reaction-rate-limited, is depicted in figure 2.3.2.2.1.2. The reverse MESA-shape of the etch in the 011-direction can be used to form a suspended structure (paragraph 3.5.3). For diffusion-limited processes, the etch rate dependence on orientation almost disappears. Table 2.2, in appendix 2B, describes some of the wet etchants used in this section.

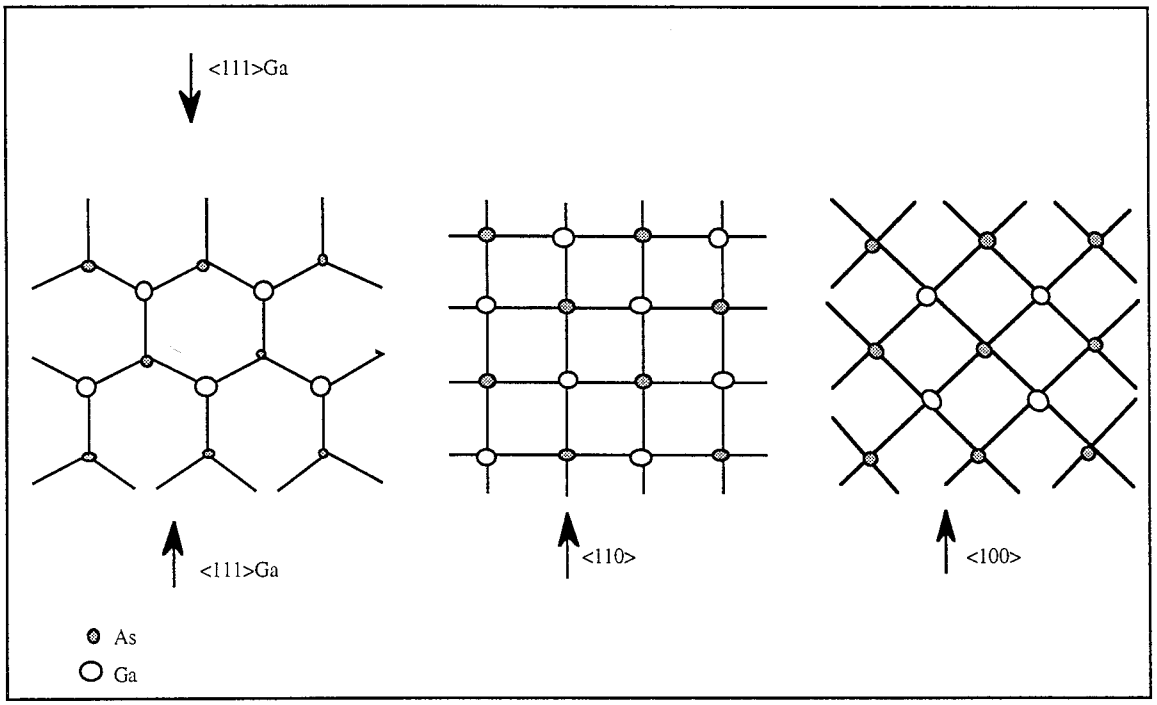


Fig. 2.3.2.2.1.1. Schematic projections of the atoms in the three low-index planes of GaAs

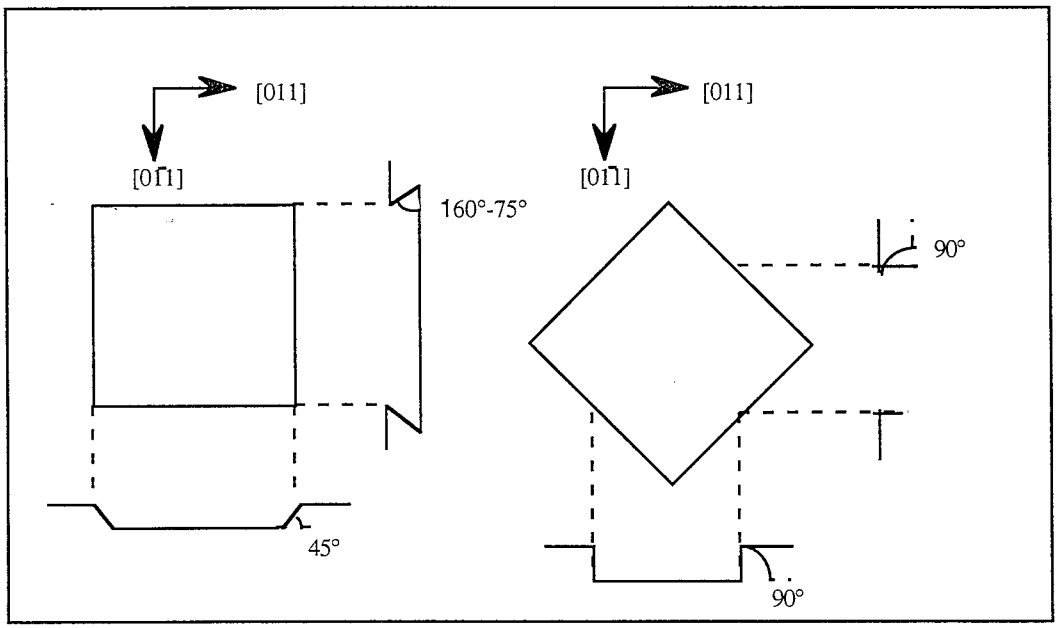


Fig. 2.3.2.2.1.2. The appearance of etched wall for reaction-rate-limited etching on (100) GaAs

2.3.2.2.2. Dry etching

Dry etching, as opposed to wet etching, do not undercut the mask for GaAs. Generally it also provides high aspect ratios ; high purity etchants ; no masking phenomena due to bubbles or surface diffusion ; and much less capillary problems to flush away reactive specimens and reaction products.

The inconvenience with dry etching is that most methods cause a damaged surface layer with built-in stresses. The common etching techniques in micromachining of GaAs are reactive ion etching (RIE), reactive ion beam etching (RIBE), and chemically assisted ion beam etching (CAIBE). Table 2.3, in appendix 2C, summarizes the dry etchants used in this section.

2.3.2.2.3. Fabrication of suspended structures by preferential etching

The etching properties of GaAs, described above, give a possibility to obtain a suspended structure just by taking advantages of the orientation dependent etch velocities of wet etching. The reverse MESA slopes join each other and create a free standing cantilever, depicted in figure 2.3.2.2.3.1. This preferential etching can only be accomplished by etch-rate-limited etchants, as explained before.

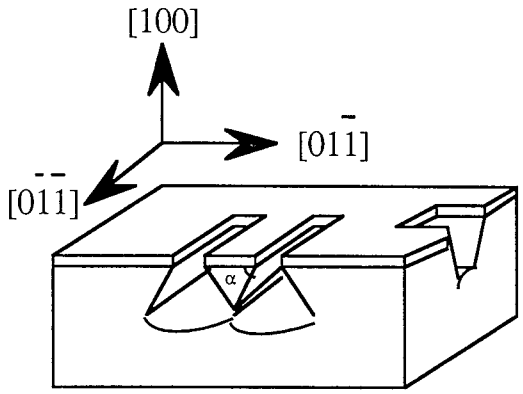


Fig. 2.3.2.2.3.1. Etched profiles in (100) GaAs by the Br_2CH_3OH-system.

The most commonly used etch-rate-limited etch systems for microstructuring GaAs are described and commented in table 2.4., namely the Br_2CH_3OH-system [Tar71], the H_3PO_4:H_2O_2:H_2O-system [Mor78], the H_2SO_4:H_2O_2:H_2O-system [Lid71], the HCL:H_2O_2:H_2O-system [Sha81], the $Kr_2Cr_2O_7$:HCL:H_2SO_4-system [Ada81], the $Kr_2Cr_2O_7$:HCL:CH3COOH-system [Ada84], the NH_4OH:H_2O_2:H_2O-system [Gan74] and the citric acid : H_2O_2:H_2O-system [Ots76].

To achieve a good structure suspension, the etched walls must be of perfect reverse MESA-shape and with a sufficiently low angle, α. The etchants with this property are marked with suitable reverse mesa-shape in the table. The etchants that produce a kind of wedge-shape will create a very small suspended structure (if any at all) because of the increased amount of GaAs to etch for suspending the structure. Enhanced etching at mask edges and at n-doped zones are common phenomena that make it difficult to achieve well defined and reproducible structures and should therefore be taken in consideration when choosing etchant and designing the mask . Furthermore, the etch-rate must not be to high, and it is preferable if the etchant properties do not change with the time. The H_3PO_4:H_2O_2:H_2O-system seems to be a very suitable etchant, exhibiting a slow etching rate with excellent reproducibility, no doping-concentration dependence and photoresist sufficient as mask.

This technique, creating suspended structures by preferential etching, is totally compatible with the Vitesse MESFET processes and no extra mask is needed in the post-process.

2.3.2.3. Fabrication of suspended microstructures using the VITESSE MESFET foundry- process

The simplest way of fabricating suspended structures using the Vitesse MESFET foundry-process was found to be the preferential etching technique, described above. We choose this technique because it demands no extra masking steps, a simple dip in an etch solution is all that is demanded.

The use of the reverse mesa-shape in the $[0\bar{1}\bar{1}]$ direction makes it possible to create bridges and cantilevers, but it is impossible to fabricate membranes for the same reason. Other considerations concerning the layout is explained, as well as the foundry- and post-process. Finally, an overview of the prospects concludes the section.

2.3.2.3.1. Considerations for the design

Since GaAs is a piezoelectric material, charges will appear when it is stressed. These charges have opposite signs if the stress follow the $[0\bar{1}\bar{1}]$ or the $[0\bar{1}\bar{1}]$ axis. Hereby, the orientation of the gates in comparison with the crystal axes of the wafer strongly changes the threshold-voltage of the transistors. This piezoelectric effect makes it impossible to design digital circuits with gates both parallel and perpendicular to these axes. Therefore, the gates are disoriented by 45 degrees from the $[0\bar{1}\bar{1}]$ axis, making two transistors perpendicular to each other respond identically. As we want to use the reverse MESA-shape of the $[0\bar{1}\bar{1}]$ direction, this must be considered when designing the masks. The CAD-program CADENCE is used for the design, and the orientation of the mask in comparison with the wafer is depicted in figure 2.3.2.3.1.1. Thus the bridges and cantilevers have to be parallel with a straight line rotated 45 degrees clockwise from the vertical axis.

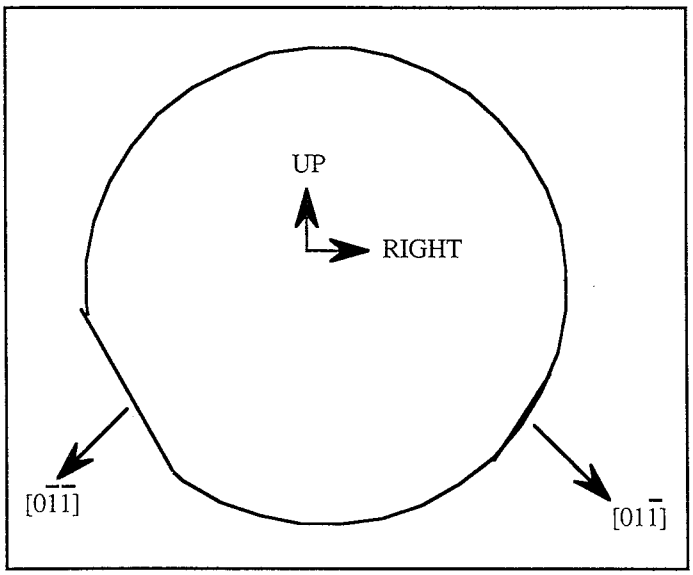


Fig. 2.3.2.3.1.1. The (100) GaAs wafer orientation compared with the layout window in CADENCE (up and right)

One of the big problems in micromachining is the stacking of vias. When the first via hole is covered by dielectric or metal, there will be a thicker layer at the edges. another via is then etched on top of the first one. The thickness of the removed layer is determined by the etch-time, and there is a high probability that the deposited layer will not be totally removed at the edges of the via and a residual dielectric layer will remain. This effect is depicted in figure 2.3.2.3.1.2. Therefore, stacking of vias is forbidden in almost all foundry-processes on substantially diminished. The obvious reason for piling vias is the gain in density on the wafer. Since the Vitesse MESFET process to be used has four interconnection metals, sufficiently large openings in the mask must be designed to obtain openings

reaching all the way to the naked GaAs. Discussions with Vitesse have resulted in minimum openings of 10 μm. Different test of the stacking via etching have been designed; the piled vias have different dimensions compared to each other, making it possible to find the best combination to open window to the GaAs substrate. The post-process etching characteristics can not all be estimated in advance, and a number of structures of different dimensions are therefore designed in order to obtain at least a few well suspended structures. The influence of the ion implantation is also possible to examine. By designing bridges of the same dimensions, doped and undoped, effects such as piezoresistivity, piezoelectricity, etc., can be studied.

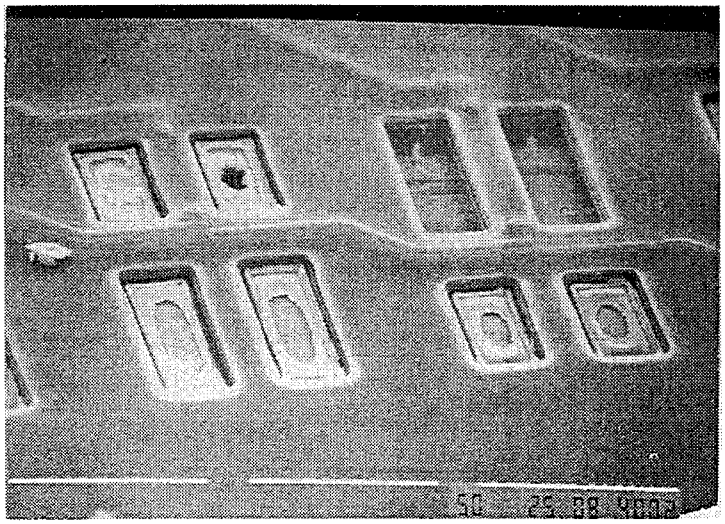


Fig. 2.3.2.3.1.2. Effects of stacking vias (residual dielectric)

2.3.2.3.2. MESFET compatible front-side bulk micromachining

The Vitesse MESFET process provides no less than four interconnection metals. for the purpose of making suspended microstructures, this is undesirable as explained earlier. The transistor has a diffused channel and autoaligned source and drain. The microstructure is defined by openings from the GaAs substrate up through the final passivation by first the "active area" mask, then "via1" to "via4" and finally by the "passivation" mask.

At the beginning of the process a (100) GaAs wafer is passivated by a dielectric (step1). Openings in the dielectric are made, defining the transistor at the left and the microstructure at the right (step2). The dielectric serves as an implantation mask when the channel is Si^+ implanted, hereby also implanting the zones later to be etched in the post-process (step3). The gate is then deposited (step4). the source and drain are implanted by using the gate as a mask (step5). After an activation anneal of the implantation, ohmic contacts are sintered and the first dielectric is deposited (step6). In total four interconnection metals (of aluminium) are sandwiched with interlayer (of SiO_2) dielectrics and finally passivated. The two windows defining the microstructure are achieved by via2 on top of via1, and so on until the final pas opening (passivation mask).

Since all interlayer dielectric are of SiO_2, they are planarized by spin-on glass (SOG) and thereby causing the vias to be notched.

The post-process etch is performed with phosphoric acid, H_3PO_4:H_2O_2:H_2O. The resulting suspended structure is depicted in figure 2.3.2.3.2.1.

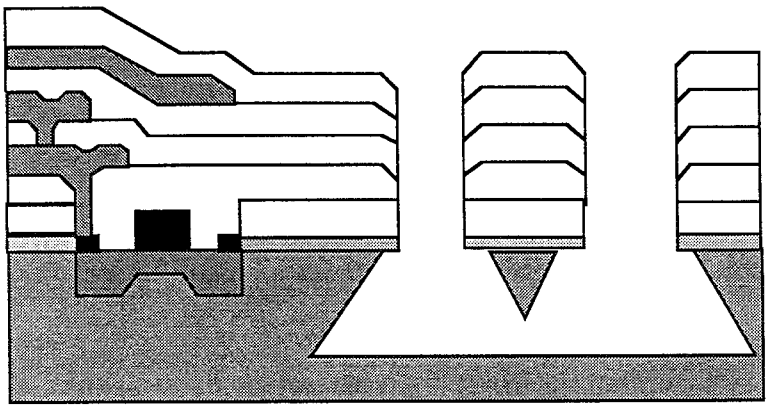


Fig. 2.3.2.3.2.1. Cross-sectional view of a microbridge with a MESFET using the Vitesse process

Designs regrouping mechanical structures, such as bridges, cantilevers, and integrated circuits have been fabricated and successfully tested (figure 2.3.2.3.2.2) using the MESFET process.

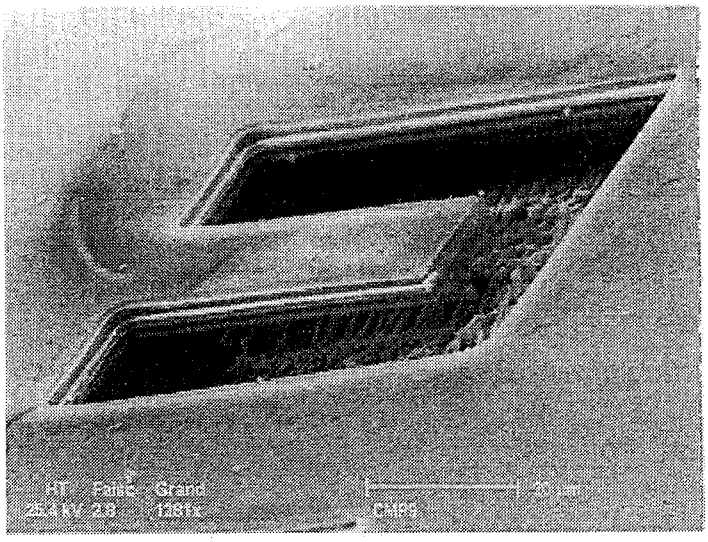


Fig. 2.3.2.3.2.2. Structure manufactured using 0.6μ GaAs MESFET compatible front-side bulk micromachining

2.3.2.3.3. Phosphoric acid etching - post-processing operation

This etchant has preferential etching characteristics for a mole ratio of H_2O_2/H_3PO_4 approximately higher than 2,3 and a mole fraction is 0.83. For this composition etch rates in $[0\bar{1}\bar{1}]$ (er_{I00}), and $[11\bar{1}]$ (er_{III}) directions were founds to be 0.95 and 0.35 [μm/min] at 0°C. The erch rate increases with higher temperature.

The cantilevers and bridges are designed with widths symmetrically distributed around 15μm ; from 10μm to 20μm. The etch-time will be estimated for the 15μm width. The reverse-mesa angle is about 60°-75° for different etchants. According Mori et Watanabe, this angle was found to be about 70°-75° for phosphoric acid, and is an average of 73° in our calculations. The etch-time is calculated by approximating the etch rates as independent of elapsed time and etched depth. To insure the suspension of a 15μm wide beam, the etch-time, t_{free}, is about 15 minutes. Also, enhanced etching at mask edges is not considered.

In another hand, the residual dielectric layer remaining after the opening in the passivation and depicted in figure 2.3.2.3.1.2, make the etching operation more difficult since the window from which the etching will take place is smaller than the the open area designed in the design phase. This problem is illustrated in figure 2.3.2.3.2.3.

To eliminate this residual layer, many solutions were considered, among others, 1 minute etching using HF solution (with or without UV insolation) mixed or not with boiling water. After this operation, the effective etching of GaAs substrate by the Phosphoric acid is performed.

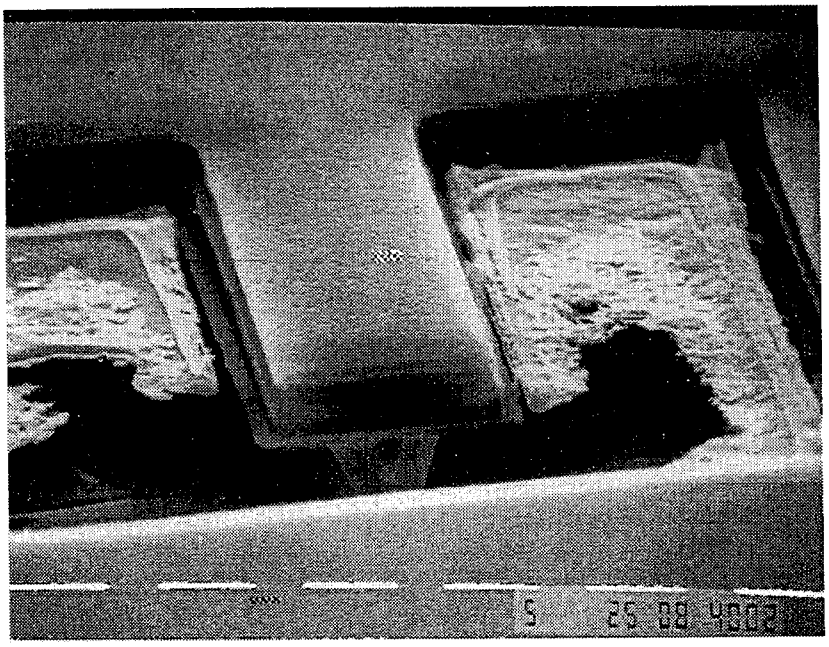


Fig. 2.3.2.3.2.3. The residual dielectric layer remaining after passivation opening brings problem to the etching operation achieved in post-process

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Appendix 2A - Table of properties for GaAs, A1As Si and Quartz

Table 2.1: Structural, micromechanical and thermal properties of GaAs, A1As, Si and Quartz at 300K

Parameter	GaAs	A1As	Si	Quartz
Crystal structure	zinc blende	zinc blende	diamond	quartz
Lattice constant, a [pm]	565.330	566.139	543.106	490.4
Band gap energy [eV]	1.424	2.168	1.12	≈8
Density, ρ [g/cm^3]	5.3165	3.7290	2.3290	2.649
Melting point Tm [°C]	1238	1740	1413	1710
Thermal expansion α_{11} [10^{-6}/K] α_{33}	6.0	4.2	2.6	13.7 7.5
Thermal resistivity [Kcm/W]	2.27	1.1	0.64	8.1-15
Specific heat, C_p [J/g K]	0.35	0.48	0.71	
Debey temperature, θ_D [K]	370	446	463	
Stiffness constants, C_{11}[GPa] C_{12} C_{13} C_{14} C_{15} C_{16}	118.8 53.8 59.4	120.2 57.0 58.9	165.6 63.98 79.51	86.8 7.04 58,2 11,91 -18.04 105.75
Young's modulus for <100> [GPa]	85	84	130	
Dielectric constant	13.18	10.06	11.7	
Piezoelectric coefficient d_{14} [$10^{-12m/V}$]	-2.69	-3.82	0	
Fracture toughness, K_{Ic} [MPam 1/2]	0.44	1.7	0.9	
Fracture strength, σ_f [GPa]	2.7		6.0	1.7
Hardness, Hv [GPa]	7	5	10	12

Appendix 2B - Wet and dry etchants for GaAs

Table 2.2: Wet etchants for GaAs

Etch solutions	Suitable mask	Sacrificial layer	Comments
$NH_4OH:H_2O_2:H_2O$ (1ml:1ml:8ml)	A1GaAs or SiO_2	GaAs	Selectivity up to 500.
citric acid:H_2O_2:H_2O (5g:2ml:5ml)	A1GaAs or photoresist	GaAs	Selectivity about 100.
HF:H_2O	GaAs	A1GaAs	Selectivuty up above 10^8.
KI:I_2:H_2O (8g:2g:40ml)	undamaged GaAs and Si_3N_4	GaAs damaged by ion-implantation	
1*N* NaOH	GaAs	$GaAs_{1-x}N_y$	

Table 2.3: Dry etchants for GaAs

Etch system	Suitable mask	Sacrificial layer	Comments
$SiC1_4/SF_6$-RIE	A1GaAs	GaAs	Excellent selectivity; Isotropic.
$C1_2$/Ar-CAIBE$_4$	Photoresist	GaAs	Selectivity about 10. Anisotropic, smooth vertical side-walls.
$BC1_3$/Ar-RIE	Si_3N_4	GaAs	Isotropic.

Table 2.4: Etch-rate-limited wet etchants for shaping GaAs

Etch system (composition)	Reverse Mesa-shape	Etch rate ($\mu m\ min^{-1}$)	Comments
$Br_2:CH_3:HO$ (4:96)	Suitable	6	Enhanced etching at mask edges. Lower Br_2 concentrations imply more preferential etching. Slowly attacking SiO_2.
$H_3PO_4:H_2O_2:CH_3OH$ (1:1:3) $H_3PO_4:H_2O_2:H_2O$ (1:9:1)	Suitable	2 1	Shiny etched (111)Ga, (111)As not as good. Highly reproductible etch rate. The etchant shows no doping concentration dependence. resist as mask is enough.
$H_2SO_4:H_2O_2:H_2O$ (1:8:1)	Suitable	14,6	Etched surfaces of relatively good quality, often better when cooled to 0°C. Slowly attacking SiO_2.
$HCL:H_2O_2:H_2O$ (1:1:9)	Not suitable	0,20	Small ratio of undercut to etched depth. Reverse mesa angle, α, is higher than 75°.
$Kr_2Cr_2O_7$:HCL:H_2SO_4 (3:1:2) $Kr_2Cr_2O_7$:HCL:CH_3COOH (1:1:1)	Not suitable	2,5 0,7	Small resist attack. High-quality etched surfaces.
$NH_4OH:H_2O_2:H_2O$ (1:1:8)	Not suitable	1,5	Does not attack SiO_2, perceptibly. Dopant dependent etch rate.
citric acid $H_2O_2:H_2O$ (5g:2ml:5ml)	Not suitable	0,3	Photoresist sufficient as mask. The etchant shows no doping concentration dependence.

CHAPITRE 3

OUTILS DE CAO POUR LES MICROSYSTEMES

3.1. Introduction

Pour transformer les microsystèmes, de prototypes de recherche en produits industriels disponibles sur le marché, des facilités de fonderies ainsi que des outils CAO doivent être disponibles.

Alors que les outils de CAO pour la microélectronique ont acquis un degré de maturité élevé, où toutes les séquences de fabrication sont simulées et le fonctionnement d'un composant ou système peut être complètement prévu, l'art de la modélisation et de la conception des microsystèmes ne fait que débuter.

Pour les différentes disciplines d'ingénierie, telles que l'électronique, la mécanique, l'optique, et d'autres, il existe un variété d'outils de conception, de simulation et de vérification pour un composant spécifique ; le manque, aujourd'hui est dans un environnement dans lequel une conception complète de microsystème peut être achevée.

En général, il existe deux approches pour dépasser cette limitation : la première consiste en le développement d'un nouvel environnement spécifique aux microsystèmes ; la seconde, plus réaliste réside dans l'utilisation les outils de CAO existants pour les différentes disciplines requises par les microsystèmes, de les étendre et de les interfacer dans un seul environnement, avec des bibliothèques de cellules standards et paramétrisables, afin d'assurer un flux de conception (design flow) continu. Cette approche, adoptée par cette étude, est gouvernée par la motivation de rendre les microsystèmes accessibles aux institutions de faible capital. Cela nous a imposé une série de contraintes à respecter, qui se résument par :

• coût réaliste : Une approche modulaire est utilisée dans laquelle uniquement les outils incontournables constituent le noyau de l'environnement et les modules dédiées à des applications particulières sont considérés comme optionnels,

• facilité d'utilisation : cette contrainte limite l'intégration d'outils "réputés d'être difficile à utiliser" dans l'environnement,

• les simulations devront avoir des temps courts de réponse. Il s'ensuit que des outils basés sur les méthodes des éléments finis (FEM) ne doivent pas intégrer l'environnement et doivent être utilisés dans la phase pré-conception dans le développement et la caractérisation des bibliothèques de cellules standards,

• l'adaptation aux facilités de fabrication existantes. La technologie supportée sera celle définie dans le Chapitre 2, basée sur l'extension des méthodes de fabrication de la microélectronique.

3.1.1. Facilités de production

Un des plus grands obstacles pour démarrer une activité de développement en microsystèmes est que des technologies particulières et donc coûteuses sont demandées. Afin d'obtenir des coûts abordables et une grande flexibilité, les microsystèmes doivent, dans la limite du possible, être fabriqués sur des lignes de production industrielles existantes pour la microélectronique, suivies par des opérations de gravure (post-processing) spécifiques aux microstructures. Cette approche permet aussi l'intégration

de circuits électroniques sur la même puce. C'est la solution monolithique considérée comme l'évolution normale des fonderies d'ASIC aux fonderies des microsystèmes. Pour cela, la stratégie de CAO est basée sur le support de cette technologie.

3.1.2. Cellules standards

La synthèse automatique des microsystèmes n'est encore pas possible : en microélectronique digitale le circuit peut être transféré du niveau système au niveau hardware automatiquement, cette opération reste impossible pour la microélectronique analogique et mixte, à fortiori pour les microstructures. Pour cela une bibliothèque de cellules standards (générique) devra être disponible pour le concepteur au niveau système (modèles de simulation) au niveau layout (GDSII / CIF). Ces modèles constituent les cellules de base que l'utilisateur peut assembler, avec des éléments qu'il a conçu lui-même, pour réaliser son microsystème. Cette bibliothèque de cellules devra, donc, être organisée à plusieurs niveaux, où une cellule est représentée à tous se niveaux pour assurer un passage continu d'un niveau à un autre au cours de la phase de conception.

3.1.3. Extension d'outils de CAO

Les outils de conception et de simulation de la microélectronique couvrent un besoin large qui peut satisfaire à des phases particulières de la conception d'un microsystème. Cependant, ces outils devront être étendus, et ceci à des niveaux différents :

• Niveau dessin de masque et vérification des règles de dessins :

des règles de dessins nouvelles introduites par les microstructures devront être intégrées, et le vérificateur des règles de dessins devra être capable de différencier un composant électronique d'un autre non-électronique et appliquer à chacun de ces composants les règles correspondantes.

• Bibliothèque de cellules standards et paramétrisables pour les microsystèmes

• Extension de extracteurs de paramètres pour assurer le lien entre un niveau de simulation correspondant à une description schématique et un autre correspondant à un niveau layout où tous les éléments parasites sont pris en compte.

• Extension des simulateurs de technologies pour intégrer les principales nouvelles étapes technologiques introduites par les microstructures, telles que la simulation de la gravure anisotropique du silicium, ...

- Extension des simulateurs systèmes en intégrant de nouveaux modèles de nature non-éléctrique, avec leur interface et le stimuli correspondants.

Les travaux dans cette thèse ont établi ses éléments et les ont intégrés dans un environnement existant pour la microélectronique.

3.2. Principe global de l'environnement

Les travaux de cette étude ont portés sur :

• l'adaptation et l'extension d'outils existants,

• le développement de bibliothèques de cellules à plusieurs niveaux de représentation (symbolique, système / comportementale, layout),

• l'assemblage et l'intégration de ces outils et bibliothèques dans un environnement assurant un flux de conception continu.

L'environnement permet de réaliser un flux de conception continu qui peut être abordé de deux manières différentes : du pont de vue non-spécialiste d'un ingénieur système désirant concevoir un

microsystème comportant des modules provenant de disciplines différentes, et du point de vue expert d'un ingénieur composant qui va apporter ses compétences et son expérience dans le développement de modèles caractérisés et validés pour être utilisés par l'ingénieur système.

Des efforts sont en cours à l'Université de Michigan et au MIT pour développer d'autres environnements conçus d'une manière différente et comportant des simulateurs de process et des outils FEM [Zha 90, Sen92]. Cependant ces outils, à part le fait d'avoir leur propre formats d'interface non-standards, exigent une grande expérience de la part de l'utilisateur.

L'environnement comporte ainsi des éléments pour l'ingénieur composant lui permettant de concevoir des modules, de les simuler et finalement de mettre son expérience dans des cellules standards caractérisées dans la bibliothèque.

L'ingénieur système prend l'avantage de la bibliothèque de cellules standards caractérisées. Il assemble des cellules et les simule au niveau système. Une fois les résultats de la simulation sont validés le layout du système global est générée. Une vérification des règles de dessins étendues aux structures est réalisée, suivie par une extraction de paramètres permettant la réalisation de la simulation comportant les éléments parasites. Une fois le layout finale est réalisé, chacun des ingénieurs système et composant peuvent intervenir pour valider des comportements et des fonctions particulières du système (simulation électro-thermique, ...). Le principe général de l'environnement est donné par la figure 3.2.1.

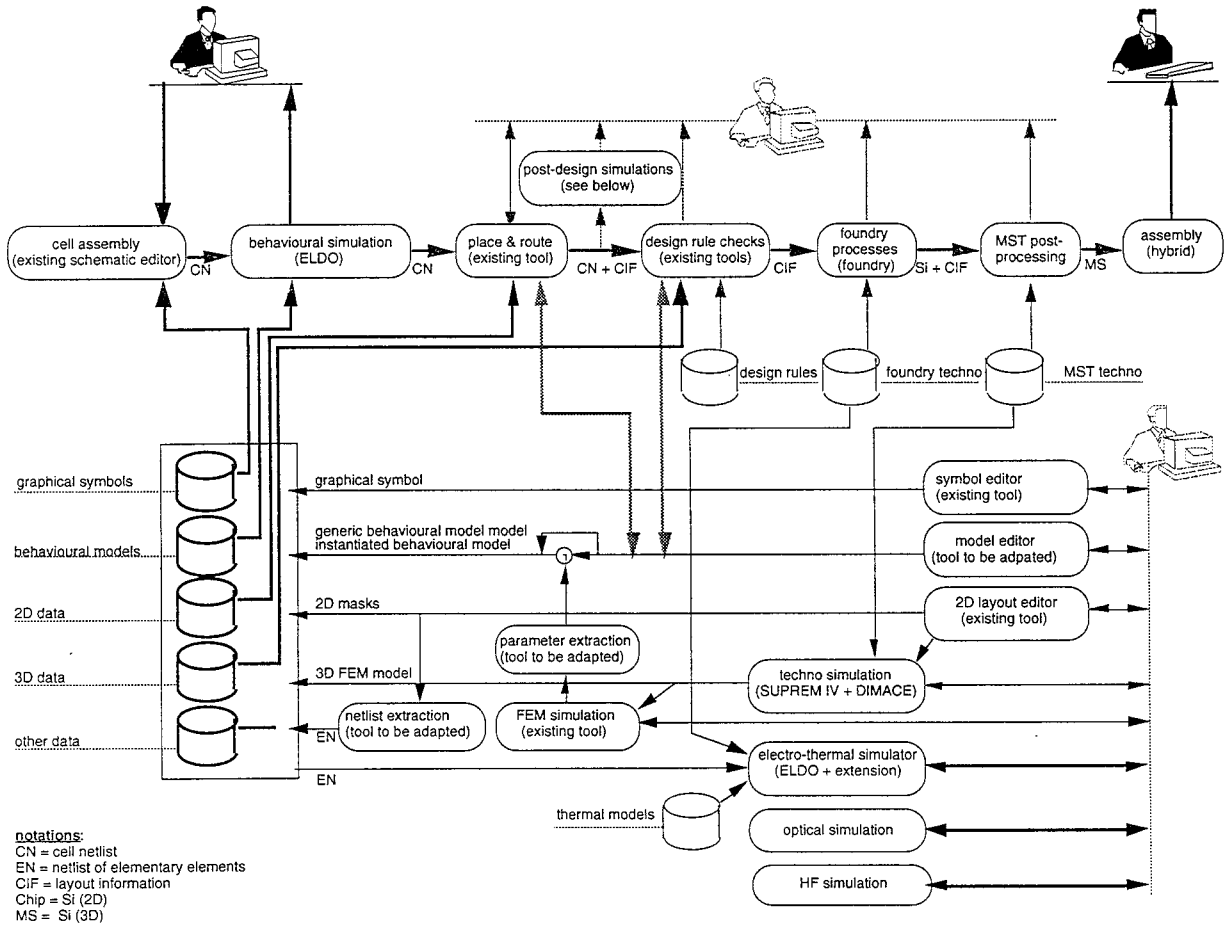


Figure 3.2.1. L'environnement général assurant un flux de conception continu

3.3. Séquence de modélisation et de simulation des microsystèmes

Dans la modélisation des microsystèmes, deux axes principaux doivent être identifiés et traités : la conception et la simulation.

En conception, l'outil de CAO doit permettre :

• la génération des dessins de masque (layout) du microsystème y compris la partie non-électronique, et une vérification des règles du dessin étendues à la technologie des microsystèmes. Ceci doit être donc couplé à une technologie. Dans le cadre de cette étude, la technologie choisie est celle compatible à la microélectronique (cf. Chapitre 2),

• une extraction de paramètres permettant la génération de modèle

Sur l'autre axe, plusieurs types de simulations doivent être disponibles :

• la vérification globale du fonctionnement,

• une simulation électrique qui permet la validation de la conception de la circuiterie,

• une simulation mécanique ,

• une simulation optique qui porte sur les modules optiques du microsystème (guides d'ondes, convertisseurs photovoltaïque, détecteurs, sources optique, ...),

• une simulation thermique,

• des simulations couplées, comme la simulation électro-thermique ou la simulation thermo-mécanique, ...

A première vue, l'environnement doit comporter des simulateurs électriques, optiques, mécaniques, thermiques, ... Ce qui n'est pas forcément le cas, puisque la conception est basée sur des bibliothèques de cellules standards caractérisées dans la phase de préconception durant laquelle l'ingénieur composant a fait appel à toutes les simulations nécessaires pour valider son modèle. Cependant certains simulateurs sont indispensables comme le simulateur multi-niveaux et mixte, et d'autres simulateurs dédiés utilisés dans des domaines de conception particuliers ...

La séquence de modélisation des microsystèmes comprend plusieurs niveaux : niveau layout, niveau process technologique, niveau composant et niveau système. Le travail de cette thèse a porté sur tous ces niveaux afin d'assurer un ensemble d'outils intégrés dans un environnement permettant un flux de conception continu et global. Les paragraphes suivants détailleront le besoin, la méthode et l'outil résultant ...

3.4. Niveau layout

Les travaux à ce niveau ont porté sur le niveau dessins de masques ou layout. Pour une approche descendante (top-down), ils permettent la vérification des règles de dessins du microsystème, y compris la partie non-électronique en étendant les vérificateurs (DRC) existants, et dans une approche ascendante (bottom-up), ils permettent l'extraction des paramètres et des informations significatives du niveau layout aux niveaux d'abstraction plus élevés.

Les environnements de conception existants, tels que l'environnement MENTOR ou l'environnement CADENCE, ont besoin d'être étendus avant qu'ils ne puissent servir pour une conception automatisée de microsystème.

Le travail à ce niveau a abouti à une approche générale d'extension d'environnement existants à la technologie des microsystèmes ; cette approche a été appliquée à l'environnement CADENCE.

Les résultats obtenus permettent la conception de microsystèmes sans une complication et un temps de conception excessives.

Le plan de travail à ce niveau a porté sur les points suivants :

• règles de dessins : l'extension des règles dessins existantes pour la microélectronique vers les règles de dessins pour les microsystèmes incluant des règles relatives aux microstructures,

• génération de layout,

• extraction de paramètres du niveau layout à un niveau de description plus élevé (netlist) permettant des simulations tenant compte tous les phénomènes parasites,

• bibliothèque de cellules : les modèles sont décrits au niveau layout, ils sont standards ou paramétrisables. Ces modèles seront couplés avec leur description système à une étape ultérieure du travail.

3.4.1. Fichier technologique

Le fichier technologique contient toutes les informations qui assure la compatibilité entre les outils de conception et la technologie. Certains outils comme le vérificateur de règles de dessins (DRC) ou l'extracteur de paramètres sont fortement dépendant des données technologiques contenues dans ce fichier. La structure de ce fichier est donnée par la figure 3.4.1.1.

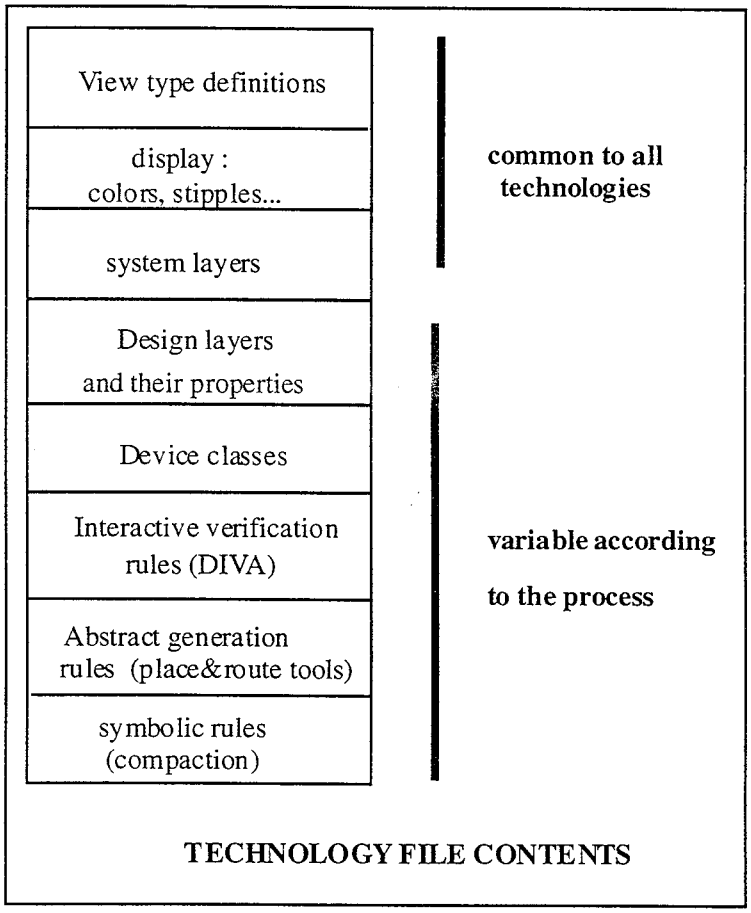


Fig. 3.4.1.1. Structure du fichier technologique

Ce fichier a été adapté à la technologie des microsystèmes, particulièrement à la technologie de microusinage en volume face-avant compatible avec la microélectronique.

3.4.2. Règles de dessins

La génération des règles de dessins est liée à une technologie déterminée. La technologie supportée par ce travail est celle compatible avec la microélectronique (cf. Chapitre 2). Plus particulièrement, les

règles de dessin implémentées dans l'outil de CAO sont relatives au microusinage en volume face-avant compatible avec la technologie CMOS 1.0µ SLP/DLM. Cette technologie a été détaillée dans le Chapitre 2 de ce document. Ces règles de dessins ont été élaborées comme résultats des structures de test fabriquées en utilisant la technologie spécifiée.

Les règles de dessins concernant strictement les couches conductives telles que le polysilicium ou les métaux sont restées inchangées pour la simple raison que leur comportement électrique n'est pas modifié même sur des structures suspendues.

Les règles de dessins qui ont été définies sont particulièrement celles qui sont imposées par la gravure anisotropique du silicium constituant l'opération majeure du microusinage en volume. Des conventions générales ont été choisies :

• création d'une couche fictive appelée "microstructure area" qui définit une zone entourant chaque microstructure avec une marge minimale de 1µm. C'est à l'intérieur de cette zone que les règles spécifiques aux microstructures seront vérifiées,

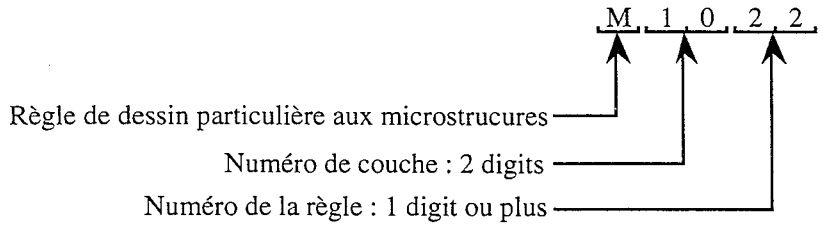
• aucun circuit électronique (structure de transistor) est permis à l'intérieur de cette zone. Seuls des cavités avec ou sans structures suspendues, telles que des poutres, ponts ou membranes, peuvent être conçues à l'intérieur de cette zone,

• les structures suspendues sont composées d'une couche de polysilicium mince, des couches de verre (dioxide de silicium / couche de passivation) et des couches métalliques,

• seuls les couches de métal (Métal 1 et Métal 2) peuvent couper la bordure de la "microstructure area", tous les autres polygones doivent être complètement à l'intérieur ou à l'extérieur de cette zone avec une marge minimale de 1µm,

• dans l'extension des fichiers technologiques de cette technologie (CMOS 1.0 µ SLP / DLM de ES2-ATMEL), les conventions déjà imposées ont été respectées (0.125 µm comme pas de grille, ...),

• une convention d'appellation des nouvelles règles a été définie, toutes ces règles commencent par un "M", comme le montre l'exemple suivant :



Les règles de dessins se basent essentiellement sur les critères suivants :

• obtention des zones d'ouverture (open area) en superposant les quatre couches suivantes : couche active, contact, via et l'ouverture de passivation. Leur configuration détermine la géométrie et les matériaux de la structure suspendue et essentiellement les couches d'oxyde entourant le polysilicium ou les métaux définissant les caractéristiques physiques de la structure suspendue,

• le positionnement relatif des zones d'ouverture (open area) et les couches conductives et celles de transistor, ...

• le positionnement relatif des zones d'ouverture (open area) l'une par rapport à l'autre, cela détermine la forme de la partie suspendue et le temps de gravure correspondant.

A titre d'exemple, la figure suivante donne la règle relative à la couche de Métal 1 :

layer : 80.
name : METAL 1.

Rule Number	Parameter	min. dimension
M800	METAL 1 stripes inside microstructure areas have to follow all the normal ES2 ECPD10 design rules, and also microstructure area specific rules	
M801	diagonal edges of metal 1 margin to microstructure area	1
M802	metal 1 can cut a microstructure area border only perpendicularly	
M803	metal 1 spacing to active area	3
M804	no coincidence between metal 1 and active area	
M805	metal 1 spacing to open contact	3
M806	no coincidence between metal 1 and open contact	
M807	overlap of poly contact	0,75

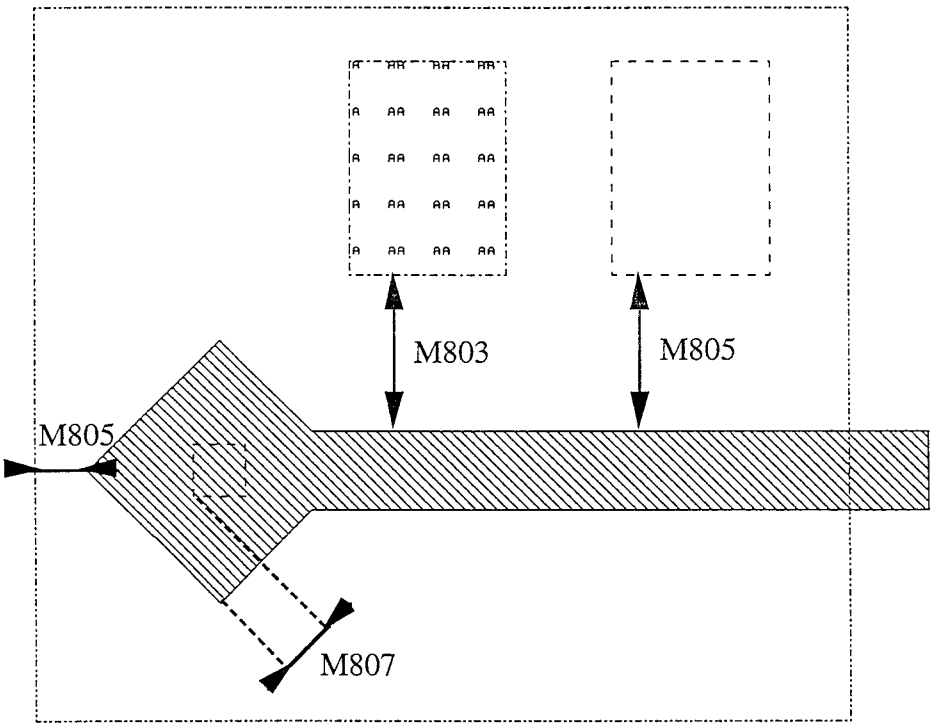


Figure 3.4.2.1. Règle de dessins correspondant à la couche Métal 1

Les règles générales donnant la manière de génération de structures suspendues ont été détaillées dans le Chapitre 2.

3.4.3. Vérificateur des règles de dessins (DRC)

L'extension du vérificateur des règles de dessins a été effectuée par l'introduction des nouvelles règles détaillées dans le paragraphe précèdent dans le fichier technologique, et en rendant ce vérificateur capable de différencier une structure électronique d'une autre non-électronique et d'appliquer les règles correspondantes à chacune d'elles.

L'extension des règles de dessins consiste en la définition de composants par une combinaison

logique de couches, et en y appliquant les commandes de vérification structurale et dimensionnelle associées à l'algorithme de vérification, DIVA, développé par Cadence (équivalent à DRACULA).

Un facteur important dans la conception des microsystèmes est le temps de gravure nécessaire à la suspension des structures. Ce facteur devait être ajouté aux règles de dessins.

Les différentes structures de test fabriquées nous ont permis d'estimer le vitesse de gravure correspondante à la solution de gravure utilisée. Cependant, pour décrire la gravure anisotropique du silicium dans les règles de dessins, il a fallu définir des nouvelles couches fictives dans le fichier technologique afin de traduire "physiquement" les étapes de la gravure. Ces couches permettent de distinguer les différentes microstructures ; "cavity 1", "cavity2" et "cavity3" correspondent aux cavités finales obtenues après la libération d'une poutre (cantilever), d'un pont (bridge) et d'une membrane respectivement. Au niveau du layout, ces cavités représentent l'intersection des plans (111) avec le plan (100) incluant la surface de la tranche (wafer).

Trois autres couches sont introduites qui représentent les différentes étapes de la gravure anisotropique par EDP :

• "open_A" : contours des zones d'ouverture (open areas),

• "open_C" : contours de la cavité intermédiaire juste après que les cavités liées à chaque zone d'ouverture mergent ensemble,

• "slowEA" : contours correspondant aux zones de gravure des plans (311), appelées "zones de gravure lente" (slowly etchable area),

Ces couches sont automatiquement générées par un programme basé sur les règles basiques de la gravure anisotropique du silicium. Ce programme a été écrit en langage SKILL développé par Cadence et dédié à l'environnement OPUS. La figure 3.4.3.1. montre la génération des couches fictives relatives aux microstructures.

L'évaluation du temps de gravure dans ce programme est faite de la manière suivante :

• la gravure des plans (110) : calcul de la distance entre les arêtes diagonalement opposés des zones d'ouverture (i. e. les couches open_A),

• la gravure des plans (311) : calcul de la longueur maximale d'arête des zones de gravure lentes (i. e. les couches slowEA).

Les dimensions maximales sont fixées par le temps de gravure maximal nécessaire en fonction des caractéristiques de la solution de gravure. Si une des dimensions est au-delà des limites, le programme génère dans le dessin des masques (layout) une couche fictive d'avertissement (warning) qui sera détectée lors de la vérification des règles de dessins.

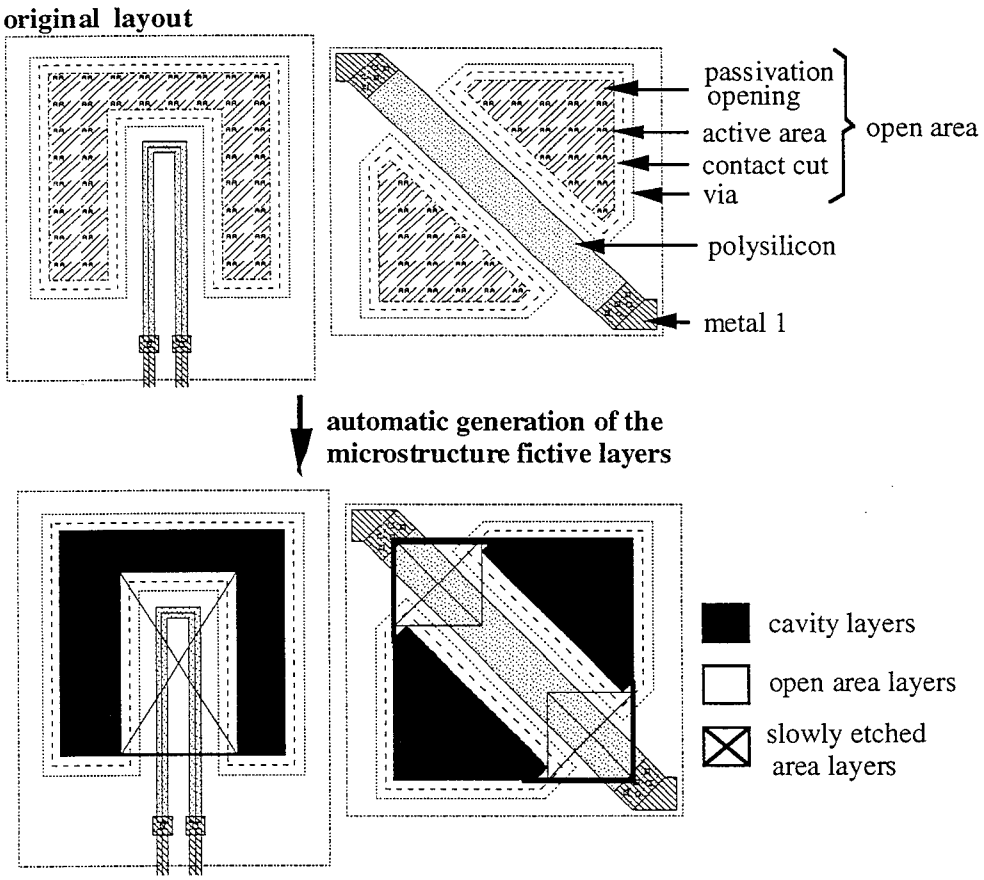


Fig. 3.4.3.1. La génération des couches fictives relatives aux microstructures

Les figures 3.4.3.2 et 3.4.3.3 donnent des exemples de DRC appliqué à des microsystèmes comportant une microstructure et de l'électronique.

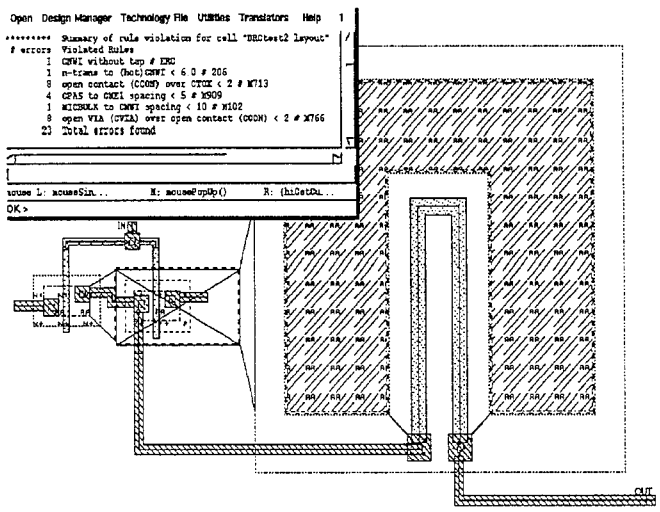


Figure 3.4.3.2. Exemple d'exécution de DRC : règles relatives aux microstructures, à l'électronique et à l'espacement entre la microstructure et l'électronique sont vérifiées simultanément

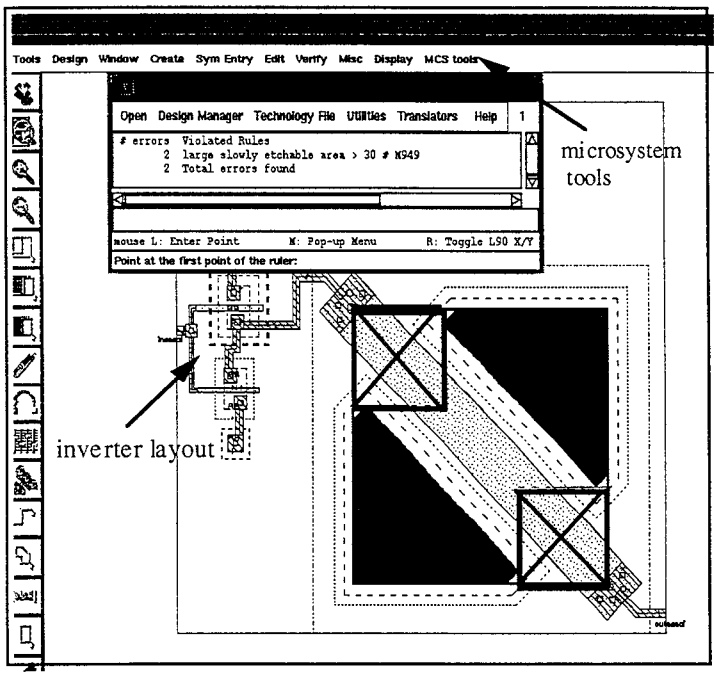


Fig. 3.4.3.3. Prédiction of a post-process etching problem

La vérification de la gravure est une méthode pour avertir le concepteur qui vise la fabrication d'un microsystème monolithique contenant des structures et de l'électronique qu'il a dépassé les limites correspondant à la non-détérioration du fonctionnement des circuits intégrés par la solution de gravure. Au delà de ces limites, le temps de gravure est considéré très long, et on ne peut plus garantir un fonctionnement normal de la circuiterie qui risque d'être endommagé par la solution.

3.4.4. Générateurs de structures - Bibliothèque de cellules paramétrisables

Ces générateurs de structures sont étroitement couplés au fichier technologique et à l'outil de CAO. L'utilisateur est capable d'adapter la taille de la structure élémentaire afin d'obtenir les propriétés physiques souhaitées, sans se préoccuper des problèmes de la gravure et de l'espacement entre les masques des zones d'ouverture. Les cellules paramétrisables permettent de contrôler automatiquement les paramètres secondaires et ne laisse à l'utilisateur que de spécifier les paramètres principaux.

Ce générateur de structure a été développé dans l'environnement CADENCE. Il est associé au fichier technologique détaillé précédemment et décrivant la technologie CMOS 1.0µ de ES2 microusinée en volume face-avant.

Le logiciel OPUS de CADENCE intègre un outil de paramétrisation, appelé Pcell. Cet outil devait être étendu puisqu'il devait être appliqué à des structures non-habituelles, comme des ponts et membranes, qui sont composées de couches à arêtes diagonales et des formes "snaky" (figures). La méthode de paramétrisation de ces structures va être appliquée à toute autre structure.

Tous les paramètres ont été définis en relation avec les propriétés physiques de la structure, mais ces paramètres ont été limités afin de réduire la complexité de conception pour l'utilisateur.

3.4.4.1. La bibliothèque de cellules existantes

Ces cellules paramétrisables sont à utiliser dans une conception full-custom. Les trois principales cellules paramétrisables sont les suivantes :

a) la micro-poutre (cantilever)

La micro-poutre est définie par les paramètres suivants :

- l_canti : la longueur de la poutre suspendue,
- w_canti : la largeur de la poutre suspendue,
- poly_to_edge : la distance entre le haut du polysilicium et le haut de la poutre ; ce paramètre est important pour la réponse piézorésistive de cette couche,
- poly_to_side : la distance entre les cotés latéraux du polysilicium et les cotés latéraux de la poutre ; ce paramètre est important pour ajuster la largeur d'oxyde autour du polysilicium,
- contact_to_poly : la partie non suspendue du polysilicium ; ce paramètre est utile pour ajuster la marge jusqu'à la cavité de gravure et pour calculer la dissipation thermique de cette partie du polysilicium.

La figure 3.4.4.1.1 illustre l'instanciation d'une cellule paramétrisable de micro-poutre.

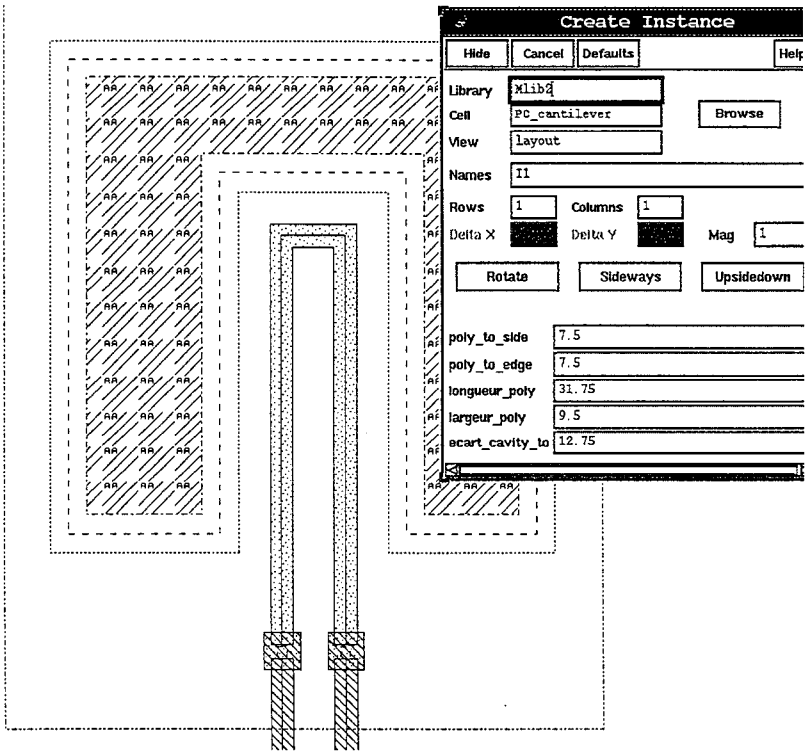


Fig 3.4.4.1.1. Instanciation d'une cellule paramétrisable de micro-poutre

b) la micro-membrane

La micro-membrane est définie par les paramètres suivants :

les paramètres w_memb et l_memb, respectivement la largeur et longueur de la partie suspendue, sont les paramètres ajustables de cette cellules ; la longueur du serpentin de polysilicium (résistance) est ajustée automatiquement. Les bras de la membrane ne sont pas paramétrisables. La figure 3.4.4.1.2 montre l'instanciation d'une cellule paramétrisable de membrane.

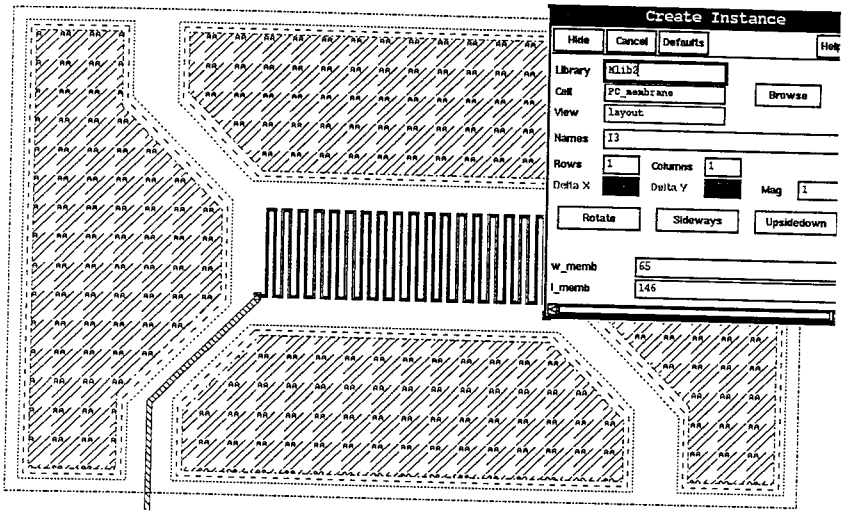


Fig 3.4.4.1.2. Instanciation d'une cellule paramétrisable de membrane

c) le micro-pont (bridge)

Le micro-pont est défini par les paramètres suivants :

- l_bridge : la longueur de la partie suspendue du pont,
- w_bridge : la largeur de la partie suspendue du pont,
- width_of_oxide : la largeur de l'oxyde sur les deux bords du polysilicium suspendue.

La figure 3.4.4.1.3 donne l'instanciation d'une cellule paramétrisable de micro-pont.

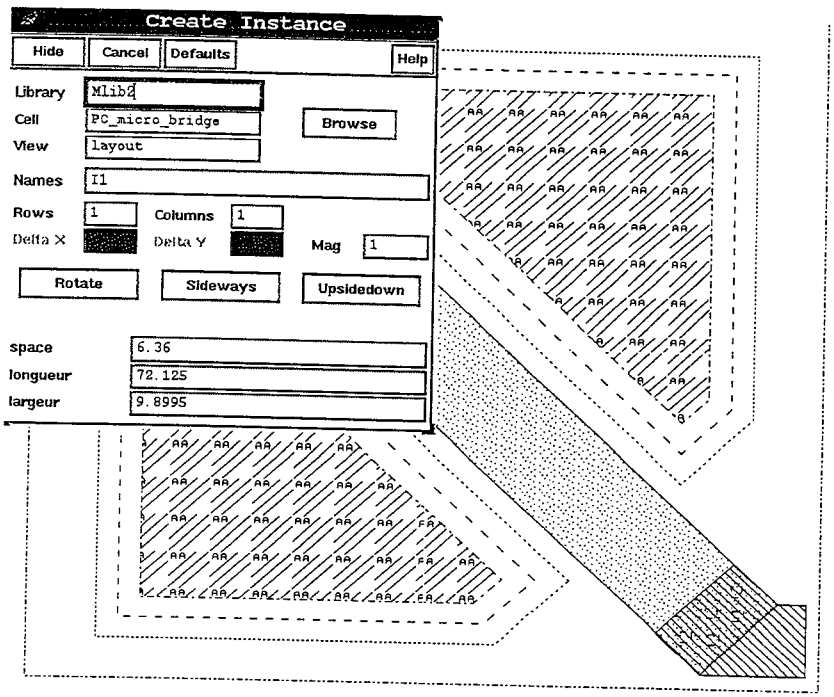


Fig. 3.4.4.1.3. Instanciation d'une cellule paramétrisable de micro-pont

3.4.4.2. L'outil Pcell

a) le menu

Les étapes de base de la paramétrisation en utilisant Pcell sont décrits dans la suite.

- Les lignes d'étirement (stretch lines) doivent être définies et dessinées suivant les axes X et Y. Une fois ces lignes dessinées, tous les points de chaque coté d'une ligne vont être étirés à partir de cette ligne d'une valeur calculée à partir de la nouvelle valeur de paramètre et de la dimension de référence. La figure 3.4.4.2.1 montre un exemple de ces lignes.

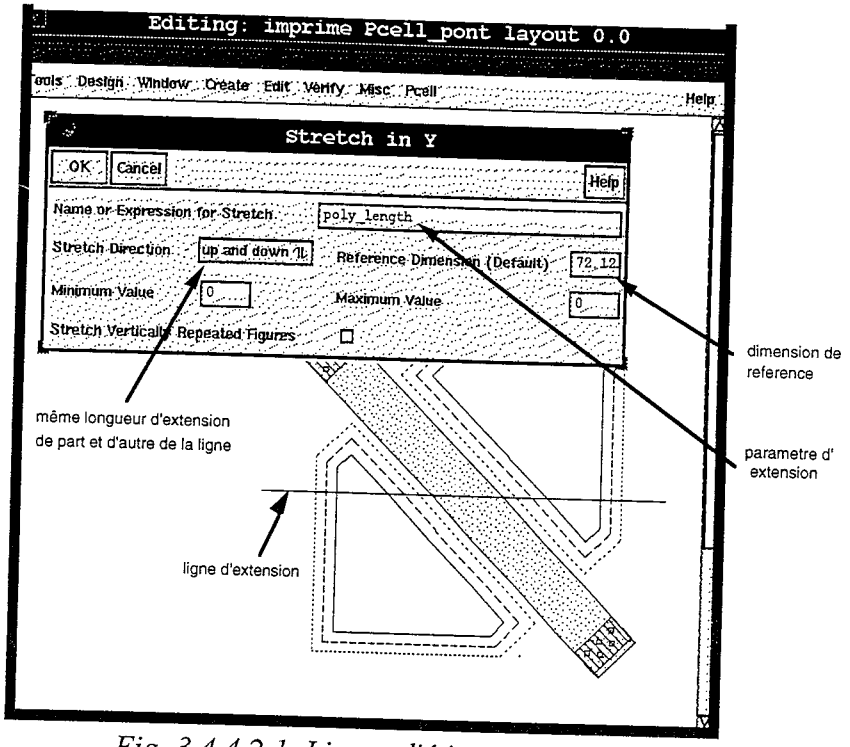


Fig. 3.4.4.2.1. Lignes d'étirement (stretch lines)

- Une fois que l'utilisateur ait défini les "stretch lines", il peut sélectionner les formes sur lesquelles l'allongement ("stretch") devait être appliqué.
- Finalement, l'utilisateur peut répéter des objets selon un paramètre d'étirement ("stretch"),
- Une fois terminé, il ne reste qu'à compiler et sauver.

Cependant, pour les microstructures, on a eu besoin de modifier l'outil pour effectuer le "stretch" suivant l'axe de la diagonale. Ceci a été effectué suivant un "stretch" double suivant l'axe X et Y, mais il a fallu diviser par (racine de 2) pour lire la vraie longueur et ajuster les coordonnées des points dans la gille. Ces modifications ont été apportées dans le fichier SKILL qui a été rechargé dans le Command Interpreter Window (CIW) de CADENCE OPUS.

b) les modifications du fichier SKILL

Le fichier obtenu de l'outil Pcell contient toutes les déclarations de "stretch" et les coordonnées paramétrées des différentes couches comme le montre la figure 3.4.4.2.2.

```
                    ----------------------------------
              ---- EXTENSION OFFSET CALCULATION----
                    ----------------------------------
    (length0 = poly_length)
    (length1 = poly_length)
     if((length0 < 0) then
        (length0 = 0.0)
     )
  ------------------------------------------------------------------------------
 ---- Calculation of the variable "length0offset" which defines the X offset ----
  ------------------------------------------------------------------------------
     (length0offset = float(round(((length0 - 72.125000) / 2) / 1.414214) * 4 ) / 4.0 )
     if((length1 < 0) then
        (length1 = 0.0)
     )
------------------------------------------------------------------------------
---- Calculation of the variable "length1offset" which defines the Y offset ----
  ------------------------------------------------------------------------------

     (length1offset = float(round(((length1 - 72.125000) / 2) / 1.414214) * 4 ) / 4.0 )

     dbReplaceProp(pcCellView "viewSubType" "string" "maskLayoutParamCell")
     dbReplaceProp(pcCellView "drcSignature" "int" 10164804)
     dbReplaceProp(pcCellView "drcChecked" "time" "Feb 16 14:11:58 1995")

     (pcLayer = 25)
     (pcPurpose = "drawing")
     ----------------------------------------
----- Calculation of the new coordinates of the ------
---- passivation mask from the previously calculated offset ------
  ------------------------------------
    (pcInst = dbCreatePolygon(pcCellView
              list(pcLayer pcPurpose)
              list(((33 + length0offset):(-26 - length1offset))
                 ((-26 - length0offset):(33 + length1offset))
                 ((-33 - length0offset):(26 + length1offset))
                 ((26 + length0offset):(-33 - length1offset))
              )
     ))
    (pcLayer = passivation)
------------------------------------------------------------------------------
```

Fig. 3.4.4.2.2. Le fichier SKILL extrait de l'outil Pcell

Il est important de garder les points des polygones étirés alignés à la grille. Notons que l'espace de grille correspond à la résolution du process technologique de la fonderie, dans notre cas celui d'ES2 (fixée à 0.25µ). C'est la raison pour laquelle l'offset a été approximé de la manière suivante :

```
(length0offset = float(round((((length0 - 72.125) / 2) / sqrt(2)) * 4) /4.0))
```

Les modifications du fichier SKILL nous ont permis aussi d'ajuster les coordonnées pour étendre l'option de répétition suivant l'axe de la diagonale et de contrôler le nombre de contacts avec la largeur du micropont. D'autres modifications ont été aussi effectuées pour automatiser quelques opérations afin de garder les règles de dessins inchangées lors d'ajustement de paramètres.

3.4.5. Génération de dessins de masques (layout)

La génération automatique de microsystèmes ne peut pas se faire moyennant des outils de synthèse automatique de dessins de masque (layout), tel que le LAS dans l'environnement Cadence, car ces algorithmes sont basés sur des structures de transistor. En plus, une cellule contenant de l'électronique et une microstructure ne peut pas être considérée par l'outil comme "cellule standard", ce qui empêche toutes les opérations de routage liées à cette cellule.

La solution à ce problème consiste en la déclaration des layout des microstructures comme blocs fixes, avant l'utilisation d'aucun outil de placement et de routage (P & R).

Plusieurs outils de P & R sont disponibles par Preview de Cadence, notamment : Block Ensemble, Cell Ensemble, Cell3 Ensemble et Gate Ensemble. La différence entre ces outils est dans l'algorithme de routage. Dans notre cas, nous avons utilisé l'outil Block Ensemble pour le fait que c'est le seul outil permettant de router des blocs sans tenir compte du layout correspondant.

Block Ensemble peut manipuler des "hard blocks" et des "soft blocks". La différence entre ces deux blocs est dans le fait que les "hard blocks" ont été placés et routés auparavant et possèdent des bornes (boundaries) et des ports (pins) fixes, alors que les "soft blocks" ont des bornes variables et des pins flottants. Ceci permet aux concepteurs de pouvoir, selon leurs besoins, réaliser des conceptions ascendantes (bottom-up) ou descendantes (top-down).

Pour utiliser Block Ensemble pour des microsystèmes, on doit simplement déclarer chaque microstructure, dont le layout a été optimisée, comme "hard block" et la placer entre d'autres blocs de circuits classiques. Le routage des blocs sera ainsi effectué normalement.

La diagramme suivant montre la séquence de tâches à réaliser afin de préparer les données de la bibliothèque en vue de l'utilisation de n'importe quel outil de P & R de Preview de Cadence.

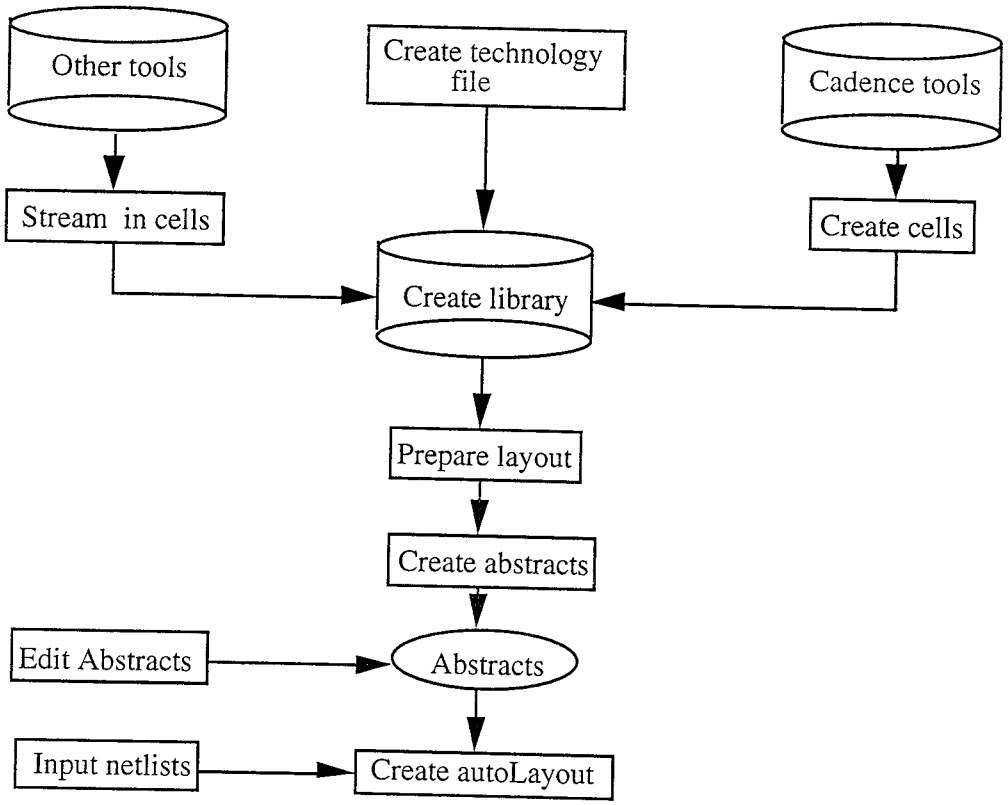


Fig. 3.4.5.1. La séquence de tâches primaires

Etant donné que nous disposons d'une bibliothèque contenant des composants électroniques et des cellules de microstructures réalisées antérieurement, la séquence précédente se trouve réduite et débute

donc par la "préparation des layouts".

3.4.5.1. Génération de la vue "abstract"

La vue "abstract" est utilisée par les outils P & R pour la génération de layout et pour l'analyse. Cette vue "abstract" est créée à partir de la vue layout ou autoLayout de chaque cellule du système. Les ports [pins] (considérés comme points de connexion pou le routeur), les propriétés des ports [pin properties], les limites du placement et du routage, et les propriétés des cellules sont ajoutées aux vues de layout ou autoLayout avant la création des vues "abstract".

La figure 3.4.5.2 montre les étapes nécessaires pour construire une vue "abstract" d'un micropont.

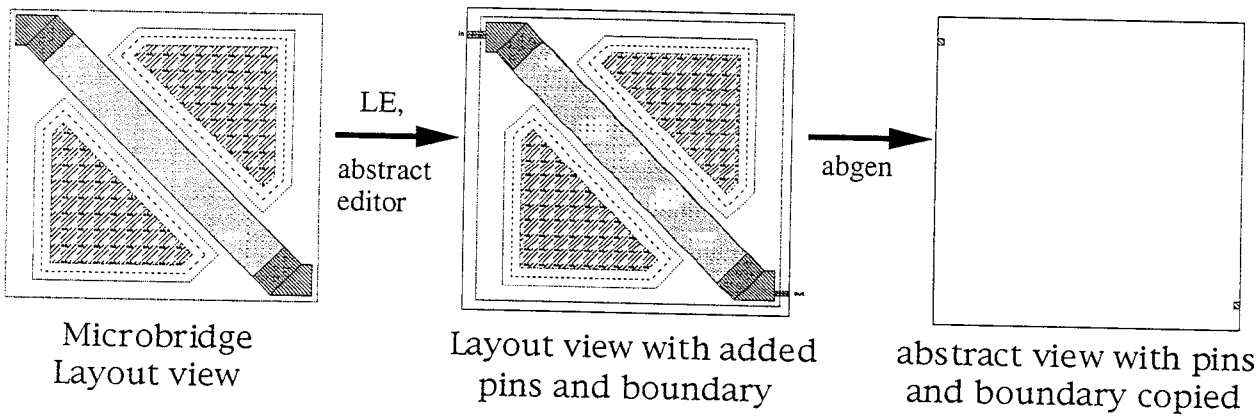


Fig. 3.4.5.2. Construction d'une vue "abstract"

Le menu éditeur de layout est utilisé pour créer des ports d'E/S. Ensuite, le menu éditeur "d'abstract" est utilisé pour ajouter les propriétés et les limites de la cellule. Le type de cellule est fixée à "macro" pour permettre le placement automatique de cette cellule par le placeur de Block Ensemble. La forme de la cellule est fixée à "rectangle" pour empêcher Block Ensemble d'utiliser la zone d'ouverture dans l'opération de routage. Finalement, la vue "abstract" est créée par la commande "Abgen" du menu éditeur "d'abstract".

3.4.5.2. Le netlist d'entrée

Après la génération de la vue abstract, nous créons un netlist logique (illustration schématique) en utilisant l'outil "Composer Design Entry". Ce netlist peut aussi être créer en utilisant des traducteurs comme Edif In ou Verilog In.

Le schéma créé contient les symboles et les informations des connections des microstructures et des circuits utilisés.

3.4.5.3. Création de la vue autoLayout

Lorsque la conversion du netlist logique en netlist physique, une autre vue de cellule, appelée vue autoLayout, est créée. Cette vue est la vue initiale utilisée pour le placement et le routage. Cette vue comporte la vue "abstract" des cellules et les informations sur les connections.

3.4.5.4. Placement et routage du microsystème en utilisant Block Ensemble

Une fois ces opérations sont effectuées, on peut appliquer l'outil de placement et de routage. L'opération de placement et de routage s'effectue de la même manière des circuits classiques.

3.5. Niveau process technologique

Le processus de fabrication des microsystèmes comporte des étapes technologiques contenues dans une séquence de fabrication en microélectronique, plus des étapes ou des opérations technologiques qui leur sont propres. Le microusinage en volume du silicium (ou de l'arséniure de gallium) est l'une des opérations technologiques la plus utilisée dans la fabrication des microsystèmes (cf. chapitre 2). Plus de 50 % des microsystèmes sont fabriqués en microusinage de volume.

Une grande variété de simulateurs de "process" existent aujourd'hui assurant une modélisation de toutes les opérations technologiques ayant lieu lors de la fabrication d'un circuit. Cependant ces outils, tels que SUPREM IV [SUP] ou ISE [ISE], ne permettent pas de modéliser la gravure anisotropique du silicium.

Des simulateurs de la gravure anisotropique du silicium tels que ASEP [Bus91] et SIMODE [Fru93] existent aujourd'hui sur le marché. Cependant, ces simulateurs souffrent de nombreux limitations et restrictions. La modélisation inverse de la gravure anisotropique qui consiste à constituer le dessin de masques (layout) à partir d'une structure 3D ayant subie la gravure est une fonction qui n'existe en aucun des simulateurs disponibles. Ces simulateurs sont aussi limités par le fait qu'ils ne traitent qu'un seul substrat, le silicium ; aucun développement existe pour les autres matériaux comme l'arséniure de gallium ou autres. De plus, les bibliothèques des diagrammes de gravures des solutions utilisées sont très restreintes.

En résumé, l'intérêt de la modélisation de la gravure anisotropique du silicium doit être vu suivant deux angles différents : le premier est une extension des simulateurs de process existants, et le second est que cette opération constitue une transformation 2D - représentant la description layout - 3D dont le résultat peut être traité directement par un outils de maillage ou un outils FEM (méthodes par les éléments finis). Ainsi, les deux flux de conception relatifs au concepteur au niveau système et le concepteur au niveau composant, sont couplés par le fait que le résultat du premier représentant un layout peut être directement interprété et utilisé comme point de départ pour le déroulement du deuxième.

Au cours de cette thèse, le sujet de la modélisation de la gravure anisotropique du silicium a été introduit et un simulateur 2D a été développé. Ce simulateur ne pouvant pas assurer la fonction de transformation 2D - 3D vise l'extension des simulateurs de process, mais l'intérêt essentiel de ce simulateur est dans son couplage avec le kit de conception. Ce couplage doit permettre au concepteur, effectuant une vérification des règles de dessins sur son dessin de masques (layout), de s'assurer du temps nécessaires à la suspension de ses structures et de valider la compatibilité par rapport à la circuiterie de son microsystème. Nous avions spécifié au chapitre 2, que la compatibilité par rapport à l'électronique intégrée dépend du temps de la gravure. Le seuil limite ne doit pas être dépassé.

3.5.1. Le simulateur de la gravure anisotropique 2D

Etant donné que le kit de conception, détaillé auparavant, adresse les microsystèmes monolithiques où les structures sont fabriquées avec les circuits intégrés, un des paramètres les plus importants reste le temps de gravure nécessaire à la suspension des structures. Il est évident que plus ce temps sera long plus l'électronique risque d'être endommagé. Ce temps dépend principalement de la solution de gravure (nature, température, concentration, ...), de la forme des zones d'ouverture définissant la structure et de la position et l'orientation de cette structure. Pour cela, le simulateur de la gravure anisotropique est un outil complémentaire au kit de conception.

Ce simulateur est basé sur une modélisation géométrique en opposition avec la description atomique où le cristal est représenté comme un ensemble d'atomes liés. Dans ce cas, la gravure est considérée comme une association de phénomènes de dissolution et de brisure de liens [Tha94]. Cette méthode est complexe et nécessite un temps de calcul et un espace mémoire considérables, d'où le choix du

modèle géométrique.

La modélisation porte sur la description du comportement des faces cristallographiques de la structure gravée. Chaque face, correspondant à une orientation cristallographique définie, se déplace suivant une vitesse fournit par le diagramme de gravure de la solution. Comme les faces se déplacent simultanément quelques changements topologiques peuvent apparaître, tels que la jonction de deux cavités, croissance ou décroissance de faces, ...

L'organisation générale du simulateur est donnée par la figure 3.5.1.1. Le simulateur requiert trois fichier d'entrée : le fichier du diagramme de gravure (etch rate diagram file), le fichier du diagramme de "lenteur" (slowness diagram file) et le fichier décrivant la structure (structure input file).

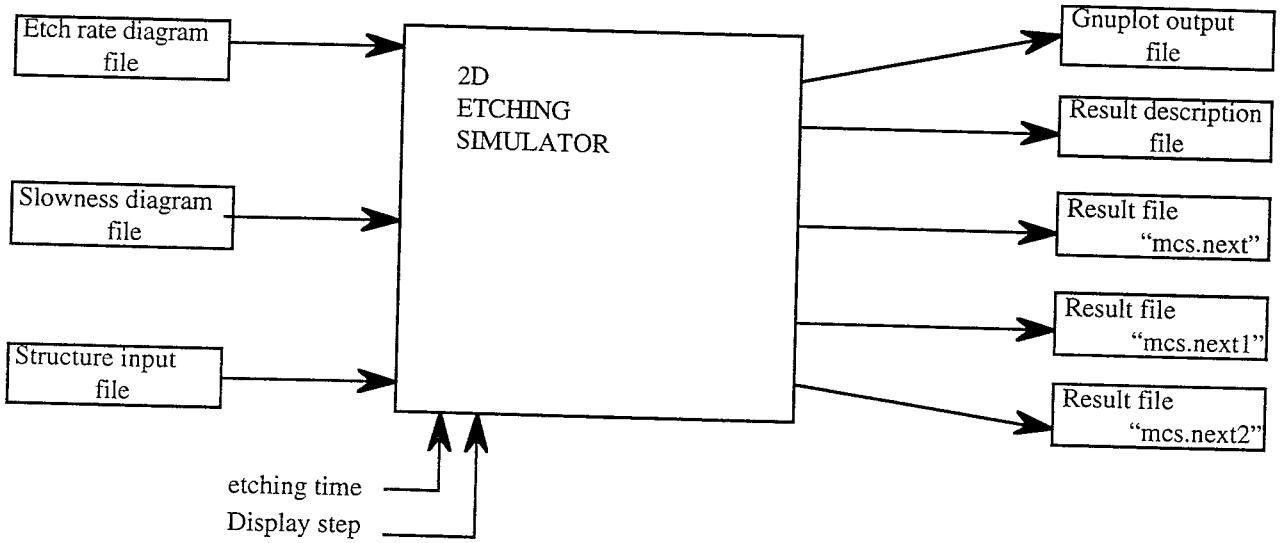


Fig. 3.5.1.1. L'organisation générale du simulateur

Le fichier du diagramme de gravure donne la vitesse de gravure des différents plans cristallographiques en fonction de leurs angles avec le plan (100). La figure 3.5.1.2 montre les diagrammes de gravure pour des solutions de KOH et EDP dans des coordonnées cylindriques.

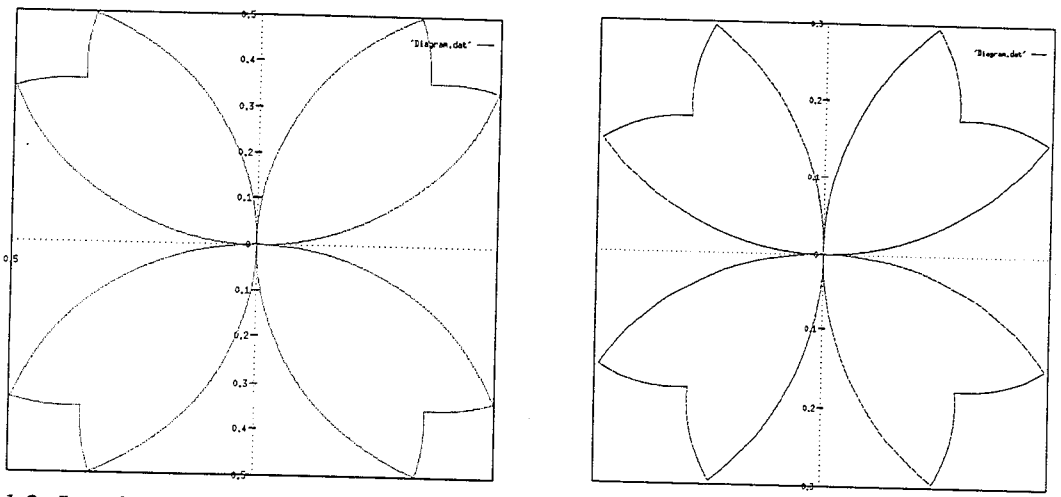


Fig. 3.5.1.2. Les diagrammes de gravure du silicium relatifs au KOH (40%, 50 °C) et EDP (80 °C) respectivement

Le fichier du diagramme de "lenteur" est un fichier calculé par le programme à partir du diagramme de

gravure (ou inversement) par simple inversion des amplitudes des vitesses dans les différentes direction ou angles. Ces diagrammes sont généralement formés de parties linéaires plus faciles à manipuler.

Le troisième fichier, "structure input file", définie la structure qui doit être soumise à l'opération de gravure. Il contient les coordonnées (x, y) de tous les points constituant les faces cristallographiques. L'unité de mesure est le micromètre. En 2D, les faces sont représentées par des segments. Certains de ces segments sont masqués, donc ne seront pas gravés, d'autres ne le sont pas et donc seront soumis à la gravure anisotropique. La figure 3.5.1.3 donne une coupe transversale d'un exemple de microstructure qui doit être soumise à la gravure.

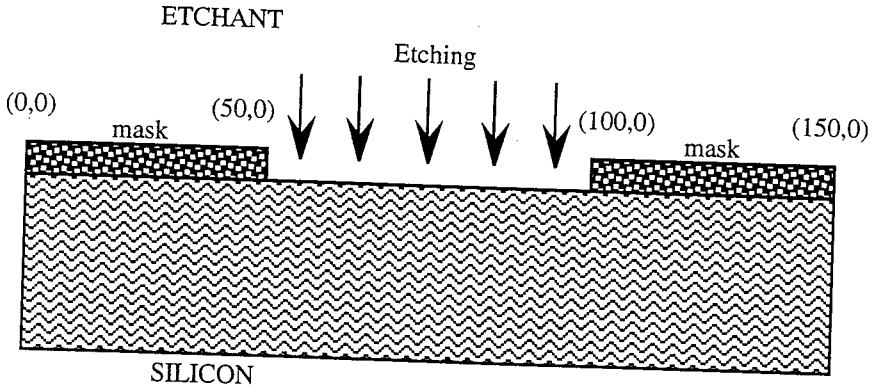


Fig. 3.5.1.3. Coupe transversale d'une microstructure avant la gravure

Finalement, l'utilisateur doit rentrer le temps de gravure et le pas de visualisation.

La figure suivante donne un exemple de structure obtenue après la gravure.

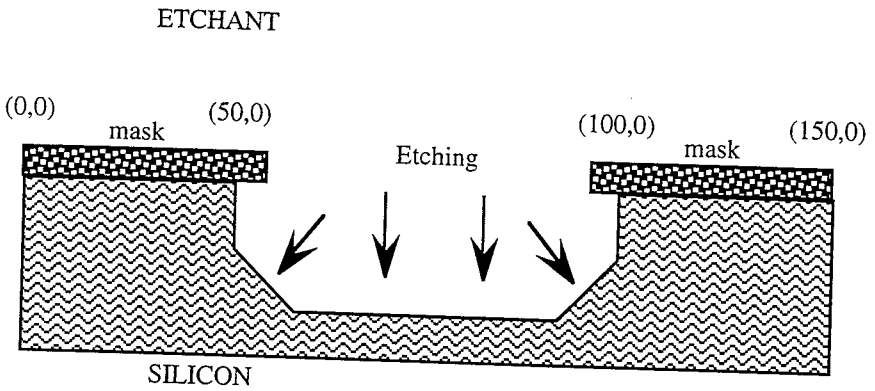


Fig. 3.5.1.4. Exemple de structure obtenue après la gravure

La figure 3.5.1.4 donne l'algorithme décrivant les différentes étapes d'exécution du simulateur.

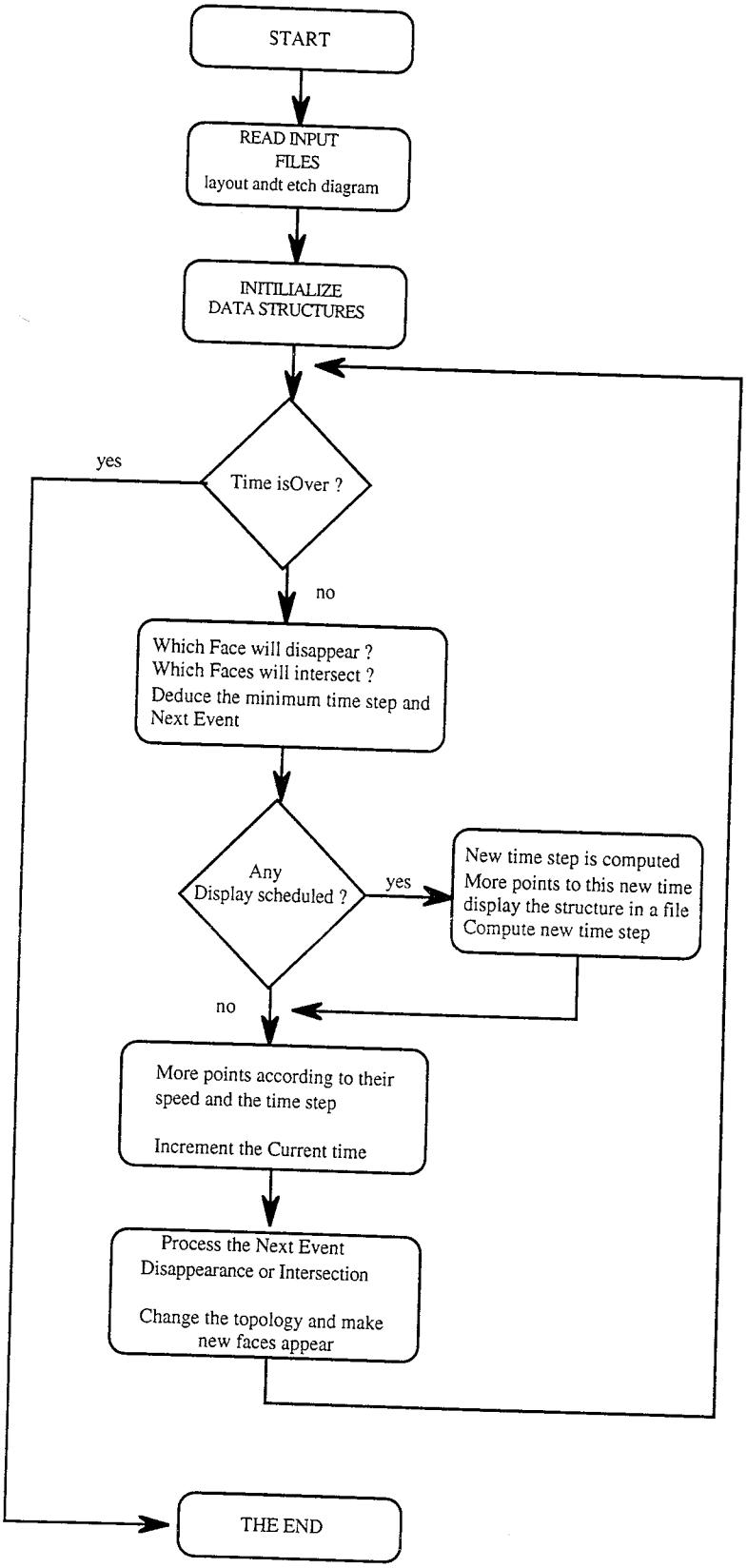


Fig. 3.5.1.4. Les différentes étapes d'exécution du simulateur

Les résultats des simulations illustrés dans les figures suivantes correspondent aux solutions de gravure représentées par la figure 3.5.1.2. La figure 3.5.1.5 donne les résultats de la simulation de la

gravure par ces solutions KOH et EDP d'une micro-poutre (cantilever). La séquence de plans représente la suspension progressiste de la micro-poutre (le pas de visualisation est spécifié en amont).

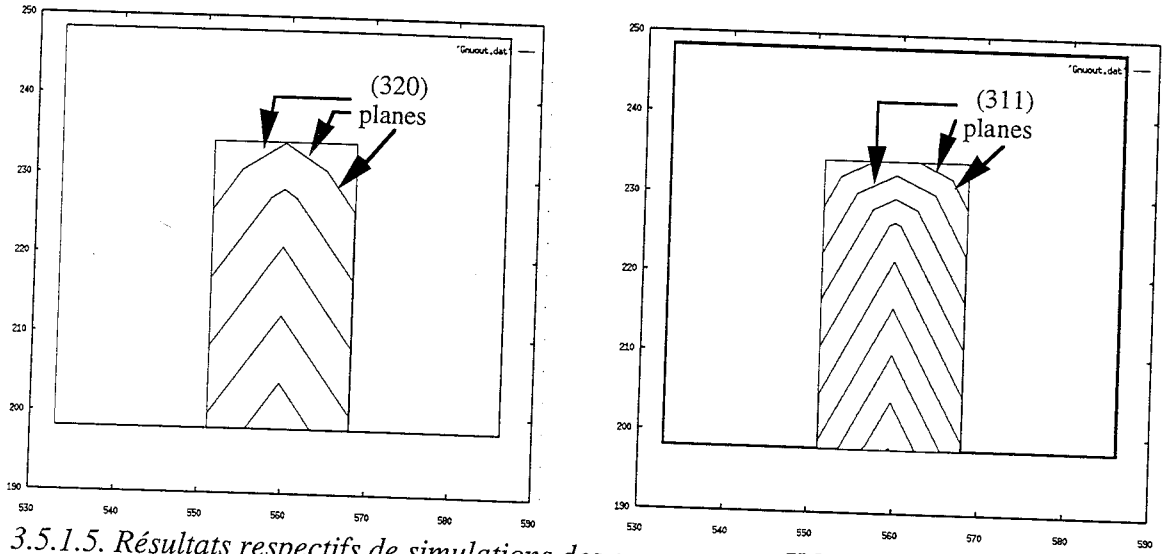


Fig. 3.5.1.5. Résultats respectifs de simulations des gravures par KOH et EDP d'une micro-poutre

La figure 3.5.1.6 montre les résultats de la simulation d'une gravure par une solution EDP d'un micro-pont et d'une micro-membrane respectivement.

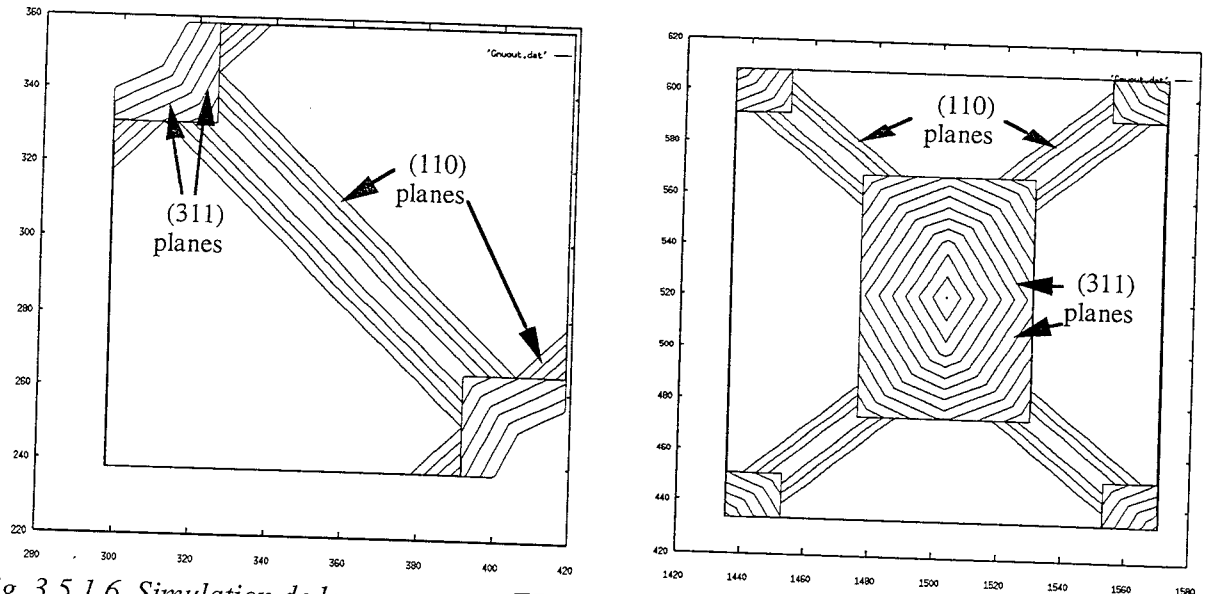


Fig. 3.5.1.6. Simulation de la gravure par EDP d'un micro-pont et une micro-membrane (temps de gravure 120 min et 180 min respectivement)

Comme nous avions mentionné précédemment, l'objectif de développement de ce simulateur (2D) est son couplage avec le kit de conception afin de pouvoir générer le temps ou le résultat de la gravure s'effectuant en post-process. Le but étant d'avertir le concepteur du temps de suspension de la structure afin de pouvoir le comparer au temps limite dans lequel la compatibilité avec l'électronique reste valable. La figure 3.5.1.7 illustre la complémentarité entre le vérificateur de règles de dessin étendu du kit de conception et le simulateur de gravure anisotropique 2D. Le layout a été conçu afin de réaliser des micro-ponts relativement large (250 µm) sans perdre beaucoup d'espace.

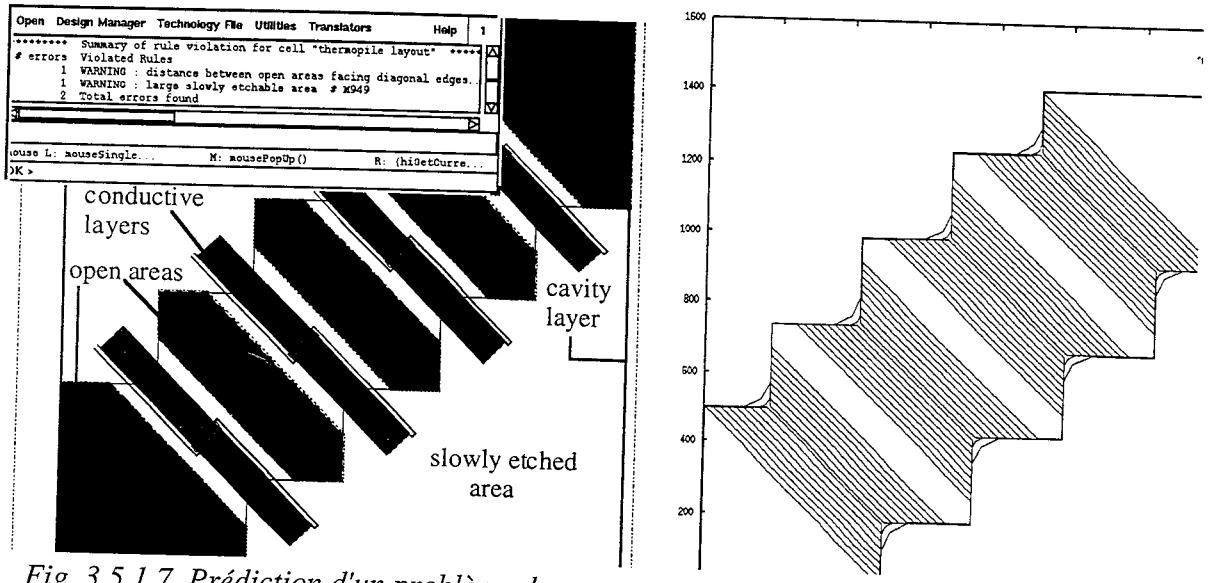


Fig. 3.5.1.7. Prédiction d'un problème de post-process sur un layout d'un capteur infra-rouge (à base de thermopiles) correspondant à une gravure de 5 heures avec une solution EDP à 80 °C

3.6. Niveau Composant

L'objectif de la simulation au niveau composant pour les microsystèmes est de caractériser les relations liant les entrées aux sorties des capteurs ou actionneurs spécifiques. La sortie d'un capteur (généralement de nature électrique) peut être exprimée comme une fonction de stimuli physique (pression, température, humidité, champs magnétique, ...). De la même manière, la sortie d'un actionneur (couple, force, pression, ...) peut être exprimée comme une fonction de la puissance d'entrée.

La simulation au niveau composant est un ingrédient clé de la modélisation des microsystèmes. Une caractérisation précise des composants est un facteur fondamental pour l'analyse du comportement du système global. Cette simulation est généralement effectuée moyennant un outil spécifique ou général basé sur un algorithme de résolution de champs (field solver) tel que les simulateurs par les méthodes des éléments finis (FEM), ... Elle devra aboutir à la génération d'un modèle comportemental ou à la définition de paramètres d'un modèle comportemental assujetti à être utilisé en simulation au niveau système.

La plupart des outils de simulation de microsystèmes existants focalise sur la simulation au niveau composant. Ils sont basés sur les méthodes par éléments finis et les bond graph (particulièrement pour les systèmes fluidiques). Certains outils ont été développés pour certains capteurs ou actionneurs spécifiques tels que les capteurs de pression et les micropompes [Pue89, Fol92, Zen93]. La majorité des outils développés fonctionne comme des programmes "stand-alone" et sont difficilement interfaçables puisqu'ils manipules des données qui ne sont pas standards. En plus, ces outils sont généralement très difficiles à utiliser et relativement cher ce qui représente un sérieux problème aux PMEs / PMIs qui ont une volonté de se lancer dans le domaine des microsystèmes.

A ce niveau, et en se basant sur la stratégie globale de l'environnement de CAO pour les microsystèmes détaillées au début de ce chapitre, nous proposant :

- l'utilisation, dans la limite du possible, des outils existants (field solver) en leur développant des kits de conceptions de capteurs et actionneurs,
- étendre les capacités des simulateurs multi-niveaux (e; g; ELDO) afin de permettre des simulations électro-thermique ou autres,
- développer certains outils limités, tels que le simulateur optique qui doit être limités aux besoins

des microsystèmes [Dum95],

- développer des méthodologies pour accélérer et automatiser la génération des modèles comportementaux dans un langage standard (i. e. VHDL-A).

3.7. Niveau Système

Idéalement, la conception d'un microsystème commence au niveau système. Le comportement du système est modélisé comme un nouveau bloc fonctionnel ou l'assemblage de modèles ou sous-modèles nouveaux ou existants. Le système peut alors être testé par la simulation sur un banc de test.

Pendant le développement, le système peut être raffiné en utilisant des modèles plus précis et plus détaillés en gardant le banc de test inchangé. Ce raffinement peut se faire soit manuellement, soit en utilisant des outils de synthèse automatique (e. g. circuits digitaux), mais aussi le remplacement des certains blocs par des macrocellules de hardware existants.

Moyennant cette méthodologie, il devient possible de vérifier et tester le comportement d'un système. Les spécifications deviennent exécutables et peuvent être discutées pour des usages d'ingénierie ou de marché (marketing).

Les microsystèmes sont multi-disciplinaires par définition. Le choix de langages de modélisation et de simulation adaptées est crucial. Dans notre cas, nous avons choisi les langages comportementaux standards développées initialement pour l'électronique digitale et analogique, précisément VHDL IEEE-1076 et le langage standard émergeant VHDL-A (IEEE-1076.1). Comme VHDL-A ne sera disponible qu'à partir de Q2 1996, nous avons choisi le langage HDL-A d'ANACAD qui se rapproche par sa structure et sa syntaxe du futur standard.

A partir de ce choix et particulièrement à partir des possibilités du langage de décrire des éléments non-électriques, nous sommes capables de modéliser le comportement des circuits électroniques (digitaux et analogiques) ainsi que les parties non-électrique (mécanique, optique, ...).

Des traducteurs du niveau schématique au niveau HDL-A [Mos95] et d'une description FEM à une description HDL-A [Kar95b] doivent exister. Certains sont en cours de développement, notamment à l'Institut de Microtechnologies (IMT, Suisse) et à l'Université Technique de Darmstadt (THD, Allemagne).

3.7.1. Bibliothèque de cellules en HDL-A

La synthèse automatique des microsystèmes n'étant pas encore possible, une bibliothèque de cellules standards (générique) devra être disponible pour le concepteur au niveau système (modèles de simulation) au niveau layout (GDSII / CIF). A ce niveau, les modèles sont décrits au niveau système en utilisant le langage HDL-A.

Une bibliothèque de cellules est en cours de développement au groupe MiCroSystèmes du laboratoire TIMA, dont certains développement se sont effectués à travers cette thèse. Ces modèles sont ensuite encapsulés dans l'environnement de conception et liés à leurs représentations schématique et layout (GDSII).

Les développements achevés à travers cette thèse portent sur les modèles suivants :

- capteur de pression piézorésistif,
- détecteur infra-rouge,
- convertisseur électro-thermique,
- micro-pompe électro-thermo-pneumatique,
- ISFET,
- capteur magnétique à effet Hall.

Ces modèles ont été validés après fabrication et ont été caractérisés par des simulations FEM. Chaque modèle comporte des entrées (I_j) et des sorties (O_j) fonctionnelles et des paramètres fonctionnels et technologiques ($Param_j$).

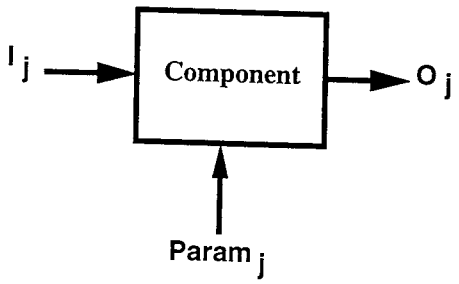


Fig. 3.7.1.1. Modélisation de composant

La figure suivante donne une description d'un capteur infra-rouge.

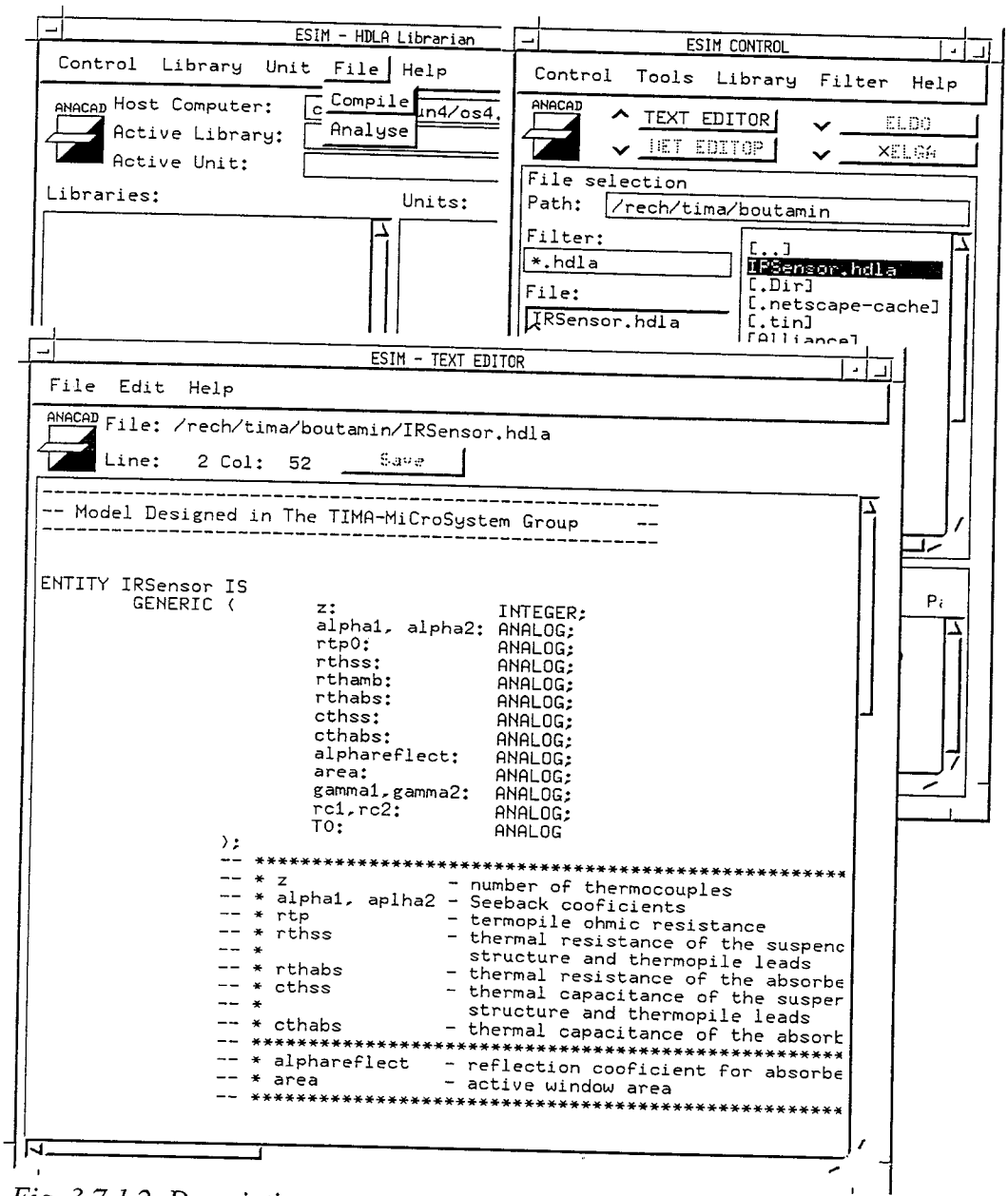


Fig. 3.7.1.2. Description comportemental (en HDLA) d'un détecteur infra-rouge

3.8. Structure globale de l'environnement

L'environnement défini à travers cette étude permet un flux de conception continu qui peut être vu sous deux angles différents : celui du concepteur système n'ayant pas des connaissances pointues dans le domaine des microsystèmes, et celui du concepteur composant ayant l'expérience dans le domaine. De ce fait, l'environnement comporte des éléments utiles pour le concepteur composant lui permettant de concevoir des modules, de les simuler et finalement de traduire ses résultats et son expérience par des modèles standards caractérisés stockés dans la bibliothèque à l'utilisation du concepteur système.

Le simulateur mixte et multi-niveaux (e. g. ELDO), représentant l'engin de simulation central, est capable de manipuler aisément n'importe quel modèle. Tous les outils sont appelés d'une interface graphique commune.

La figure 3.8.1 montre la structure globale de l'environnement CAO ainsi défini.

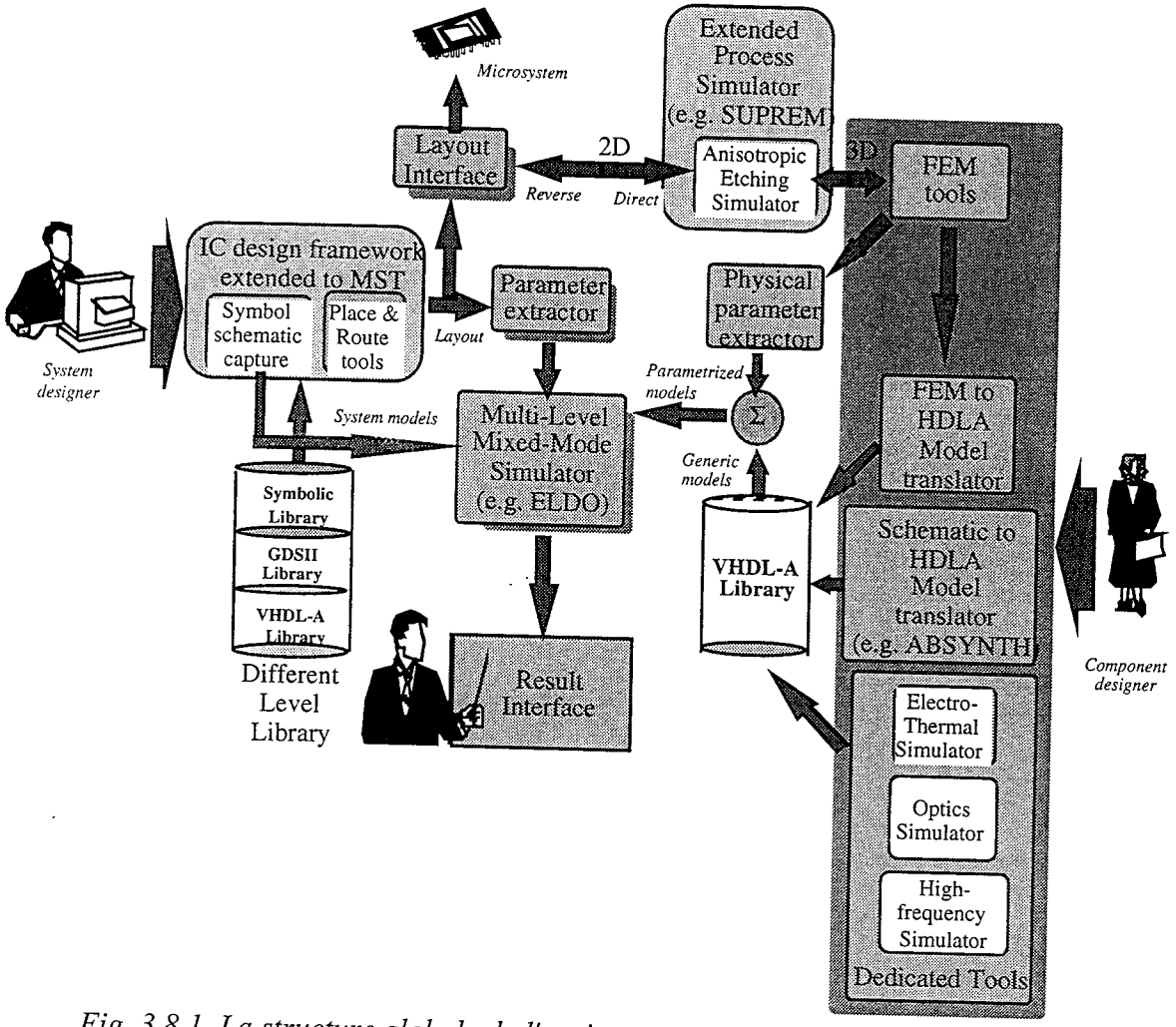


Fig. 3.8.1. La structure globale de l'environnement de CAO des microsystèmes

Cet environnement couvrant les différents niveaux de modélisation et de simulation de microsystèmes permet les fonctions suivantes [Kar96b] :

- un flux continu de conception moyennant l'extension (kit de conception) des outils de conception des circuits intégrés disponibles sur le marché (e. g. MENTOR, CADENCE) permettant :

- la génération de dessin de masques (layout) d'un microsystème comportant des parties électroniques et non-électroniques et la vérification des règles de dessins. Ceci est lié à une technologie, en l'occurrence le CMOS 1.0µ microusiné en volume face-avant,

- l'extraction de paramètres du niveau layout au niveau netlist afin de réaliser des simulations en post-layout (back-annotation),

- une vérification globale de la fonctionnalité du système en utilisant ELDO / HDL-A, en ajoutant des éléments de nature non-électrique, des éléments d'interfaçage et les stimuli correspondants,
- une simulation composant permettant des analyses spécifiques pour une approche de concepteur au niveau composant (e. g. analyse structurale, simulation optique),
- une vérification post-conception, telle que le comportement électro-thermique global du système,
- une bibliothèque de cellules standard et paramétrisables à plusieurs niveaux (schématique/symbolique, système/comportemental, layout/GDSII).

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CHAPTER 4

GENERIC ARCHITECTURE FOR COMPLEX MICROSYSTEMS

4.1. Introduction

In this chapter, we propose a generic architecture that could be used when designing complex microsystems which includes many sensors and actuators with electronics and communication modules. This architecture has been used for the BARMINT medical demonstrator. BARMINT (Basic Research for Microsystem Integration) is a European project (ESPRIT III). Several problems occuring in this kind of microsystems are discussed and correspondant solution are presented.

The BARMINT microsystem consists of several different silicon substrates, forming together a so-called vertically stacked Multi Chip Module (MCM-V). In each substrate one or more different functions is implemented. The distribution of the various functions among the different substrates greatly affects the design of the electrical architecture of the microsystem.

4.2. General presentation of the BARMINT demonstrator

The global concept of the BARMINT medical demonstrator will be presented in this section. The presentation will include a discussion of both the mechanical and the electrical configuration of the microsystem.

4.2.1. The mechanical configuration

The different functions that is implemented in the BARMINT medical demonstrator include optical, mechanical, chemical and micro-electronic functions. One of the most important issues within the BARMINT project is the integration of these functions within one package. After extensive research carried out by several BARMINT participants, the MCM-V packaging technology developed by Thomson has been chosen for the packaging of the microsystem [Val95].

4.2.1.1. The MCM-V packaging technology

The MCM-V (MultiChip Module, Vertically stacked) concept is a technique that offers the possibility to integrate different kinds of chips, using different kind of technologies, into a single package. An example of a vertically stacked multichip module is given in figure 4.2.1.1.1. In this multichip module each chip (produced by a certain technology) is sealed on a standard substrate, which can be made of epoxy or silicon. On each substrate a thin metal film interconnection pattern is deposited. These interconnections lead to the edges of the substrate and give the possibility to make vertical connections between the different vertically stacked substrates. The vertical connections have to be made as a last step in the production of the multichip module by electrochemical deposition of a metal and a laser writing technique. To achieve electrical interconnection between the chip and the substrate, several different bonding techniques can be used. In the BARMINT microsystem the wedge bonding technique using gold wires has been chosen [Val95].

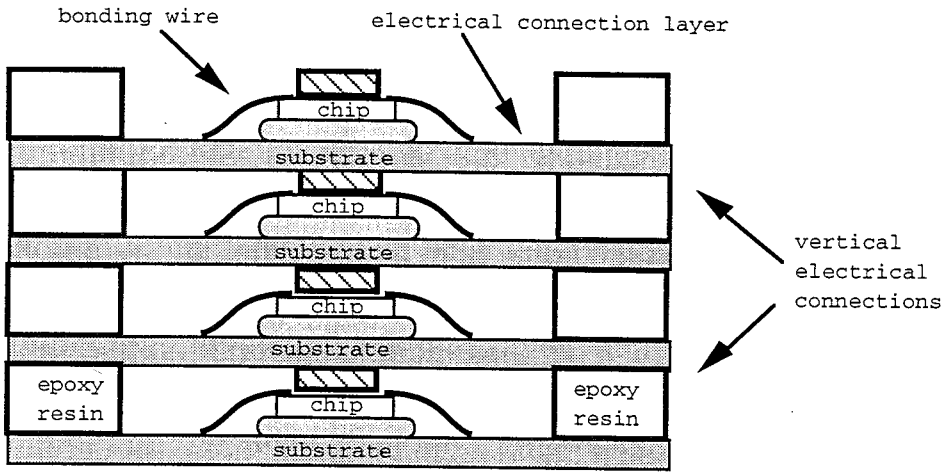

Fig. 4.2.1.1.1. Integrating different chips into one package using the MCM-V technique

In a MCM-V package the different chip/substrate assemblies are glued on top of one another. After that, the complete system is encapsulated using an epoxy resin as a moulding glue. The encapsulated system is trimmed to a cube with smooth surfaces using a diamond saw. Finally the vertical electrical interconnections are made as described above.

Beside the vertically stacked multichip module normal non-stacked versions also exist. The suitability of the MCM concept for microsystems and integrated sensors is extensively discussed in [Las93].

The MCM-V packaging technology gives the opportunity to divide the BARMINT medical demonstrator into subsystems. Each subsystem consists of devices that can be produced with the same technology, so for subsystems a monolithic approach can be used. Afterwards, the different subsystems can be integrated into one package using the MCM concept. According to this principle, the BARMINT microsystem can be divided into the following subsystems [LAA95a]:

- micropump module, consisting of a thermopneumatic micropump,
- sensor module, containing different types of microsensors,
- module containing fluid tanks,
- VLSI module for signal processing and external communication,
- module of mechanical tests,
- module of thermal tests,
- power supply module.

The BARMINT microsystem divided into subsystems is schematically represented in figure 4.2.1.1.2. A great advantage of this division is that it supports a top-down design approach. After the system-level design of the microsystem is divided into different modules, these modules can be developed and implemented independently, using different technologies. The different modules only need to have the same physical dimensions and need to satisfy previously agreed specifications. For the BARMINT microsystem, the physical dimensions have to be as given in figure 4.2.1.1.3.

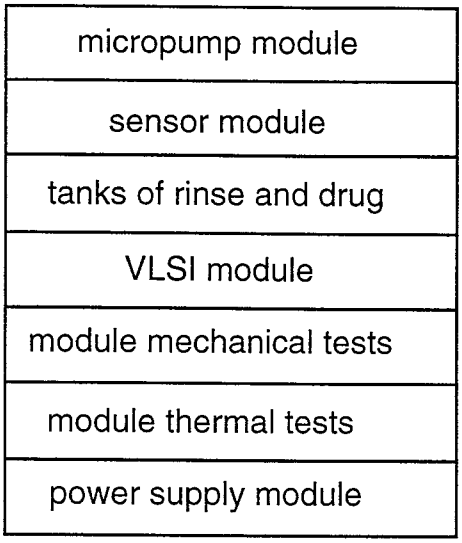

Fig. 4.2.1.1.2. The BARMINT microsystem divided into subsystems

In figure 4.2.1.1.3, it can be seen that besides electrical connections with a microcomputer, the microsystem is also supplied with an inlet and outlet tube for a fluid that has to be analyzed or controlled with the microsystem. By means of the micropump, the fluid is pumped through the system, were it will pass the sensor module and eventually the module containing fluid tanks.

The optical fibers in figure 4.2.1.1.3, connected to the power supply module, have to couple the light emitted by a laser into the microsystem. In the power supply module, the laser light is converted into electrical energy for the microsystem, by means of photo-voltaic cells. The reason for this kind of power supply is to demonstrate the feasibility of implementing an optical function into a microsystem. The development of the photo-voltaic power supply module is extensively described in [LAA95b]. According to the system level specifications, the module has to deliver an output voltage of 3.3 or 5 volts, with a maximum power of some hundred milliwatts.

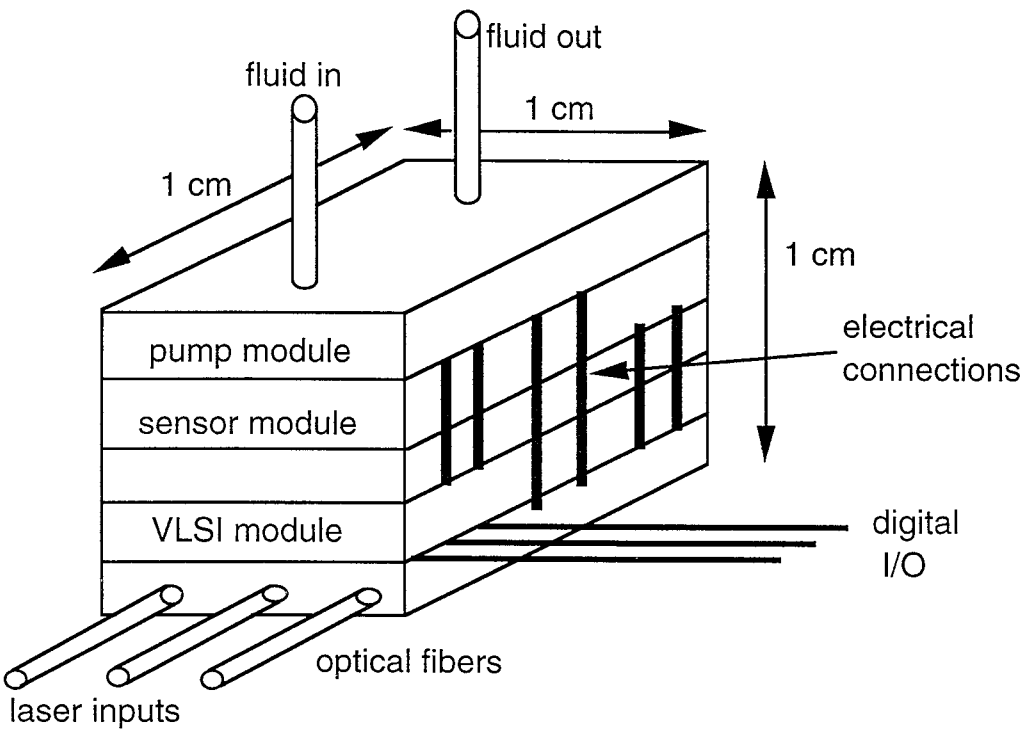

Fig. 4.2.1.1.3. Physical dimensions of the BARMINT microsystem

4.2.1.2. The micropump module

The cross section of the combination of micropump module and sensor module is given in figure 4.2.1.2.1 [LAA95c]. The micropump is located on top of the sensor chip (and on top of the microsystem) and is of a thermopneumatic type. It consists of two bounded substrates. The first one is of Al_2O_3 and carries a Ta_2N heating resistor. The second one is a micromachined silicon substrate with in it a cavity, a flexible membrane, two holes for inlet and outlet of fluid and two valves in polysilicon. By sticking the two substrates, the cavity becomes a closed one. The application of an electric voltage to the heater resistor causes a temperature rise of the air inside the cavity and a related pressure increase, inducing a downward deflection of the silicon membrane. This downward deflection causes an increase of pressure in the fluid measurement chamber. The fluid in this chamber will push the outlet valve open and will flow out.

When the voltage is switched off, the air inside the cavity cools down and the silicon membrane will deflect upward. This deflection causes a pressure decrease in the measurement chamber, which will open the inlet valve; fluid will flow into the measurement chamber. This operation can be repeated by applying a periodical voltage to the resistor, inducing a constant movement of the fluid into one direction. Accurate simulations of the micropump in the BARMINT microsystem have demonstrated that it will only work properly when a periodical voltage with an amplitude of 10 V and a frequency of 10 Hz is applied to the heating resistor [Oel95].

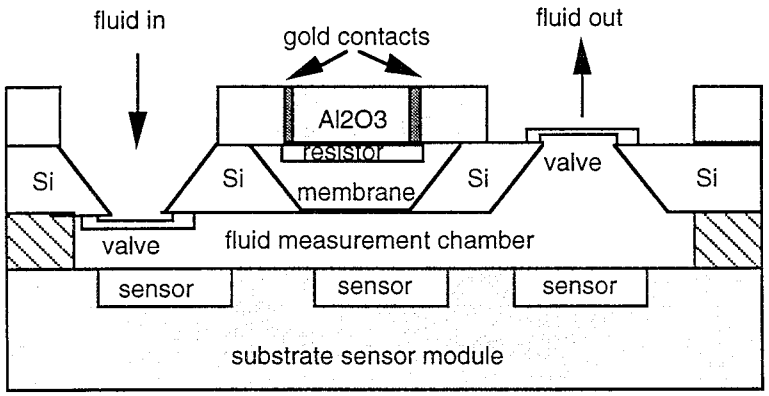

Fig. 4.2.1.2.1. Cross section of the micropump module and the sensor module

4.2.1.3. The sensor module

In the sensor module that is located at the bottom of the fluid measurement chamber, several different types of microsensors are implemented. It concerns the following devices:

- three piezoresistive pressure sensors,
- three temperature sensors,
- two ion-sensitive field effect transistors,

as has been defined in [CNM95b]. An important property of these sensors is that they in principle can be produced with a CMOS technology [CNM95a]. Therefore, within the sensor module a monolithic approach can be used, which means that all the sensors are implemented in the same substrate. The layout of the sensor module is presented in figure 4.2.1.3 [CNM95b].

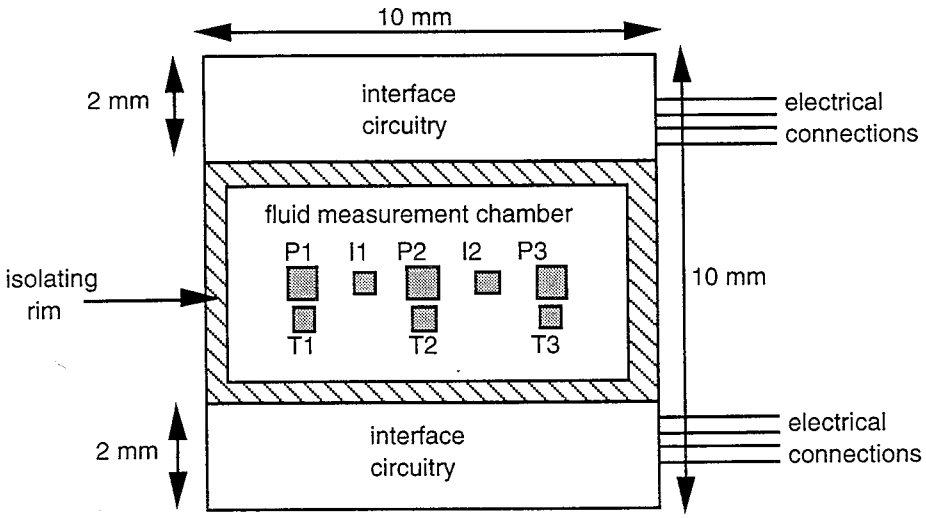

Fig. 4.2.1.3. Top view of the sensor module

The sensor chip is divided in three regions by an isolating rim. Within the rim is the fluid measurement chamber through which the fluid flows. The three pressure sensors in the measurement chamber are located exactly under respectively the pump membrane, the inlet valve and the outlet valve of the micropump module. Close to each pressure sensor a temperature sensor will be implemented. The output signal of these temperature sensors could be used for compensation of the temperature sensitivity of each pressure sensor. Finally two ISFETs (Ion-Sensitive Field Effect Transistors) are implemented between the pressure sensors, for measuring the ion concentration of certain chemical species in the fluid. The use of two instead of one ISFET gives the possibility to put them eventually in a differential measurement configuration.

The two regions outside the isolating rim in figure 4.2.1.3 can be used to implement CMOS compatible signal conditioning circuits. The electrical connections of the sensors in the fluid measurement chamber lead directly to the two regions outside the chamber, where they will be connected to the implemented signal conditioning circuits. Which kind of circuits will be implemented in these two regions will be discussed in the next paragraph. The relatively large available surface (two times 2 x 10 mm) implies that a considerable part of the signal processing can be housed on the sensor module.

4.2.1.4. The VLSI module

The BARMINT medical demonstrator is a microsystem that contains sensing and actuating functions. The sensing functions are represented by the microsensors implemented in the sensor module and an actuating function is represented by the micropump. In a modern measurement and control system, sensor data acquisition and actuator control is performed by a microcontroller or microprocessor. For this reason such a configuration is also chosen for the BARMINT demonstrator, in order to obtain a competitive microsystem with promising future applications [BAR93]. A microsystem will only be of future interest when it offers an advanced sensor management and when it can be directly connected to higher computer levels.

For this reason analog signal communication is no longer suitable, and a microprocessor or microcontroller has to be implemented to take care of communication between the sensors, the actuator and higher computer levels. As can be seen in figure 4.2.1.1.2, in the BARMINT microsystem a special module is reserved for the implementation of these kind of processing and control circuitry, that is called the VLSI module.

As temperature-induced mechanical stress in the microsystem is an important issue for the BARMINT project, some thermal monitoring facility would be desirable [CNM94a, CNM94b]. For this reason it

has been decided to implement eight temperature sensors on different locations of the VLSI module [Kar95]. The output signals of the temperature sensors can be used to map the thermal distribution of the VLSI module or to detect overheating. A possible layout of the VLSI module with temperature sensors is given in figure 4.2.1.4.1.

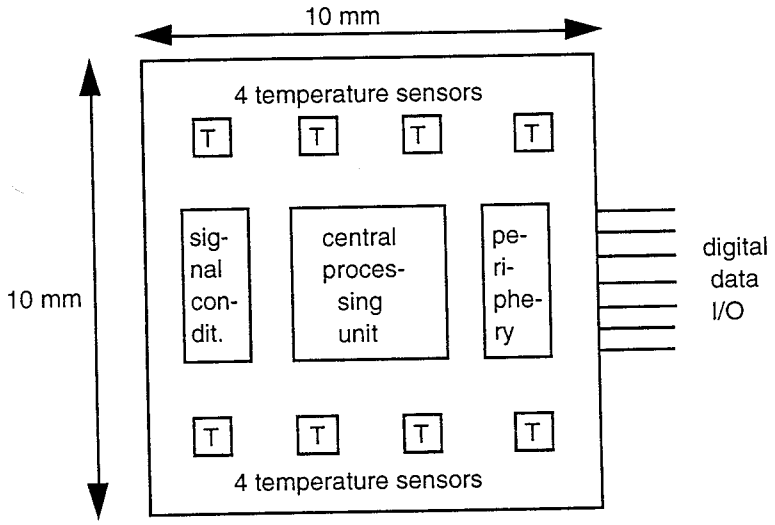

Fig. 4.2.1.4.1. Top view of the VLSI module

With the I/O data lines of the VLSI module of figure 4.2.1.4.1, the microsystem can be connected to an external host-computer. The data measured by the sensors of the microsystem could be monitored on-screen or stored in an external memory by means of the I/O data lines.

4.2.2. The electrical configuration

The first step in designing the electrical system level architecture of the BARMINT medical demonstrator is exactly defining which modules, devices and functions have to implemented in this architecture. When considering the BARMINT microsystem as presented in the preceding paragraph, we can conclude that the following devices have to be taken up in the electrical configuration:

micropump module:
- electrical heating resistor of the micropump,
- electrical power driver for the micropump;

sensor module:
- three temperature sensors,
- three piezoresistive pressure sensors,
- two ISFET sensors,
- signal conditioning circuits;

VLSI module:
- microcontroller / microprocessor,
- peripheral circuitry, internal memory,
- digital I/O interface,
- eight temperature sensors ,
- signal conditioning circuits.

The electrical system level architecture is presented in the figure 4.2.2.1.

The starting point for the design of the BARMINT system level architecture is the configuration of a

typical modern sensing and actuating system, as presented in figure 4.2.2.2. It consists of only one sensor and one actuator, analog signal conditioning circuitry, an AD and DA converter and a microcontroller.

The AD and DA converters form the interface between the analog and the digital domain. The analog signals coming from the sensors have to be digitized before they can be processed in the microcontroller and transmitted to an external memory or host computer. The reverse function is necessary for the actuator. The digital control signals generated by the microcontroller have to be converted into analog signals before they can drive an actuator. Mostly, a driver or buffer circuit is also necessary, because the actuator demands more input power than the DA converter can deliver.

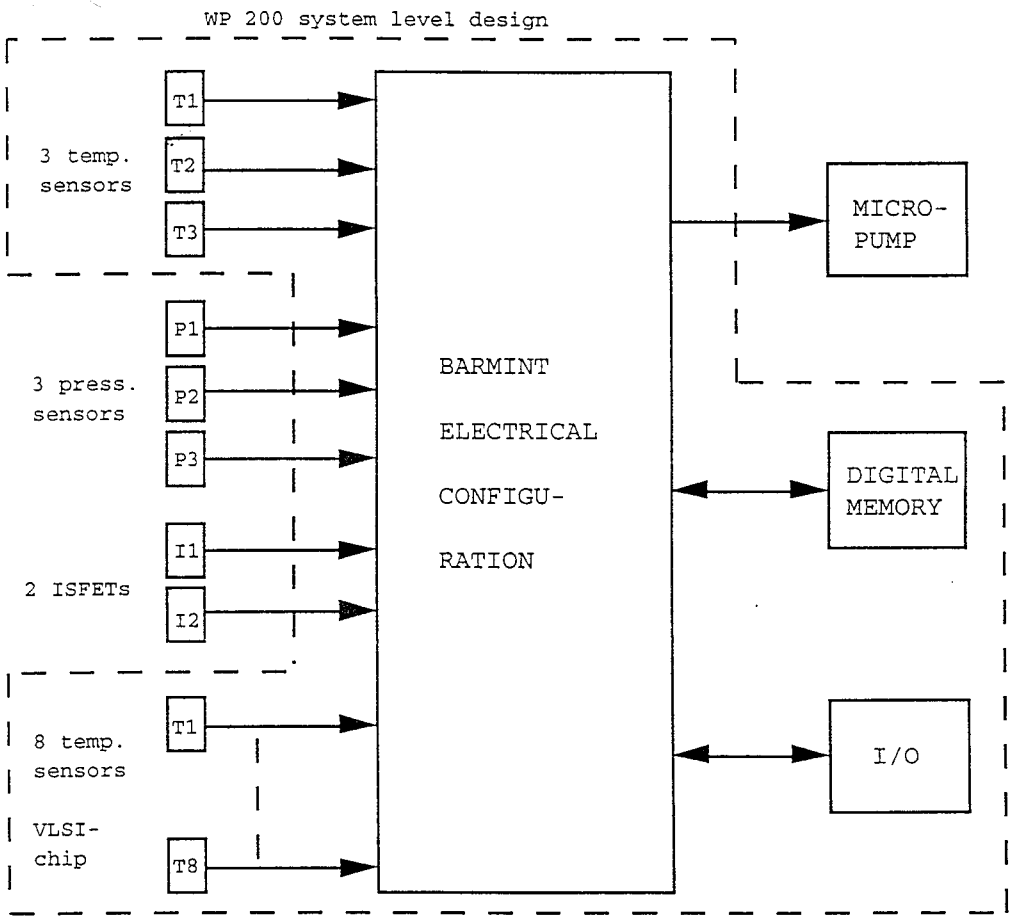

Fig. 4.2.2.1. BARMINT electrical system level architecture

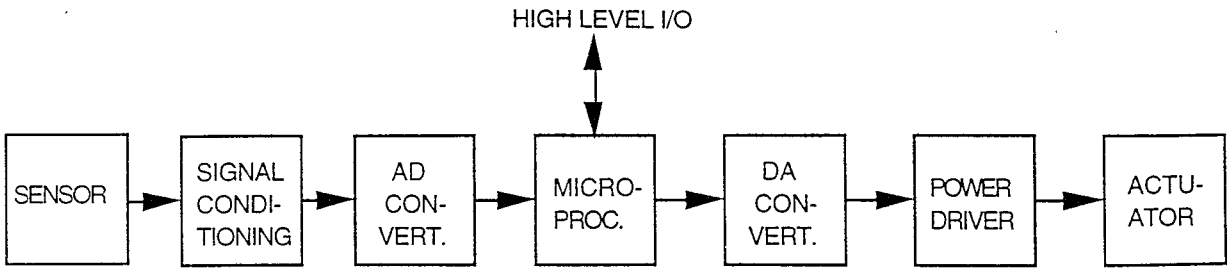

Fig. 4.2.2.2. Basic configuration for a modern sensing and actuating system

4.2.2.1. The signal conditioning circuitry

In the configuration of figure 4.2.2.2 an important role can be assigned to the analog signal conditioning circuitry. The output signal of a typical microsensor is usually very small (few mV's)

and noisy, shows drift as a function of time and is superposed on a considerable offset level. Besides, a sensor is often more sensitive to a second parameter, such as temperature, than the measurand itself. Considering these sensor properties, the analog signal conditioning circuitry (in this report often indicated as sensor interface circuit) should have the following desirable features [Mid88, Hui86, Hui94, Mei94] :

- improvement in sensitivity, linearity and accuracy and effective suppression of noise, drift, offset and cross-sensitivities of the sensor signal,

- conversion of the sensor signal to a standardized output signal format, that is directly suitable for a connection to an AD converter,

- the presence of a certain degree of adaptability, which implies that the conditioning circuits can be adapted to the actual characteristics of the sensor. This adaptibility should be controlled from a higher hierarchical level of the microsystem,

- the presence of a self-test and calibration facility. With a self-test it could be verified if the sensor and its interface is still working properly. This self-test should be periodically activated from a higher hierarchical level of the microsystem. The calibration facility could be coupled to the requirements for adaptibility, as described at item (3). When properly adjusting the characteristic of the interface circuit, the relation between measurand and output signal could be fitted to a calibration curve.

4.2.2.2. The AD conversion technique

Before the design of the signal conditioning circuits can be started, the most suitable analog-to-digital conversion technique for the BARMINT microsystem should be selected. In that way the output stages of the sensor interface circuits can be optimally adapted to the input stage of the selected AD converter. When discussing different AD conversion techniques, two major ways to communicate with microprocessors should be considered.

The first method is with a fully digital code. The binary encoded output signal of an AD converter generating this code can be directly connected to and read by the microprocessor. This kind of AD converter is indicated as the direct converter. Although a direct AD converter offers a high-speed conversion, its accuracy is restricted by on-chip resistor or capacitor matching. It should be realized that a precise direct AD converter is something very complex and may require a different process than available in the microsystem [Mid88, Hui86, Hui92]. Besides, yield requires that as little circuitry as possible should be put on the sensor chip. So within a microsystem as the BARMINT demonstrator, only AD converters which are simple to realize, are feasible [Mid88]. A direct AD conversion technique should therefore be avoided in the BARMINT microsystem. Examples of direct AD converters are successive approximation converters, cascade and flash converters.

The second method to communicate with a microprocessor is with a frequency signal, where the duty cycle or a frequency ratio represents the measurand. Because modern microprocessors are capable of measuring time intervals or frequencies, a frequency signal can be directly coupled to a microprocessor, using a single communication wire. The conversion of time or frequency into a fully digital code is performed in the processor, by counting the number of pulses in a certain time period derived from the processor clock. Assuming that the frequency signal is a square wave, it can be considered as a semi-digital bitstream. Therefore a converter generating a frequency signal is often indicated as a semi-digital converter or bitstream converter.

In general a frequency signal has the same advantages as a fully digital signal. Frequency signals are also highly immune to noise and disturbances and can be easily transported over long distances using a single communication wire. Moreover, when considering microsystems, the frequency signal has the advantage that it can be generated relatively simply. In [Mid88] and [Hui86] the use of frequency (semi-digital) output signals for the sensors in a microsystem is strongly encouraged. When systems are rather small, it has no use to separately convert all the sensor output signals into fully digital

codes. In a microsystem like the BARMINT demonstrator, digital processing power should be kept central for the whole system, whereas locally only sufficient circuitry should be added to a sensor to enable a pulse or a frequency output. This largely increases the feasibility of the integration of microsensors and microelectronics.

Analog sensor output signals can be easily converted into frequency signals by use of free-running Voltage Controlled Oscillators (VCO), Current Controlled Oscillators (CCO) or duty-cycle converters. The circuits necessary for these conversions are relatively simple, have small dimensions and are compatible with standard CMOS processes. Besides, they do not need trimming adjustments [Hui92]. However, a serious disadvantage of these kind of oscillating converters is their high sensitivity to digital interference. As the oscillators are free-running, they tend to track other frequencies, such as clock signals and switching spikes. This effect will introduce large problems in a microsystem like the BARMINT demonstrator, where several different sensors and an actuator are simultaneously operating. Specially the driving current of the micropump could cause serious interference problems. For this reason a converter has to be used that is insensitive to digital interference signals. When choosing a synchronized bitstream converter, the interference problem is avoided.

Synchronized bitstream converters need an external clock signal, to which they synchronize their output signal. In this way a high ruggedness against alien clock signals is obtained. A disadvantage of synchronized converters is that the circuits and the datacommunication will be more complex, enlarging the total chip area. The sigma-delta bitstream converter is the only exception to this rule, as its circuit is usually very simple and its bitstream output signal remains suitable for single wire communication, without a data synchronization protocol [Hui92]. Sigma-delta converters have been shown to be very successful in the implementation of high-resolution A/D conversion systems. The converter has a high resolution and a good linearity [Mei94]. The only disadvantage of sigma-delta converters is that they are relatively slow. However, this is not a great problem, for most sensors measure relatively slow quantities.

When considering the discussion above, it can be concluded that for the BARMINT microsystem a synchronized semi-digital bitstream conversion technique should be prefered above direct AD conversion. Moreover, the sigma-delta bitstream converter has already proven to be an excellent candidate in several different sensor interfaces [Hui92, Cic90, Mal93, Mal94]. They have a very simple structure, are completely CMOS compatible, offer a high resolution, a good linearity and an effective suppression of digital interference.

At the system level, this choice has three consequences:

- because the sigma-delta converter is based on the so-called charge-balancing principle, which means that an internal capacitance is periodically charged and discharged, it has to be made current-driven or a switched capacitor approach has to be used. In order to minimize power consumption and chip area, the current-mode sigma-delta converter should be prefered (see paragraph 7.3). Therefore, within the BARMINT microsystem will seriously be considered if it is possible to design analog sensor interfaces with a current-mode output,

- according to the current-mode approach for the sigma-delta converter, an internal capacitance is charged by a current that represents the sensor output signal, and discharged by a so-called reference current. This reference current is a constant current, that is independent of the quantity to be measured. In the BARMINT microsystem this means that a reference current source has to be implemented, that delivers a current independent of pressure, ion activity and temperature. It will be clear that the latter is the most difficult, as temperature can not be controlled throughout the whole system,

when choosing a suitable microprocessor / microcontroller for the BARMINT micro-system, it

should have a frequency counting input. In that case, the output signal of the sigma-delta converter(s) can be directly coupled to the microcontroller input. Within the microcontroller, the semi-digital bitstream is converted into a fully digital code. The connection between sensor-interfaces, sigma-delta converter(s) and microcontroller will be arranged by a semi-digital bus structure.

When equipping the measurement configuration of figure 4.2.2.2 with a sigma-delta bitstream converter instead of a direct AD converter, it has to be changed into the configuration of figure 4.2.2.2.1.

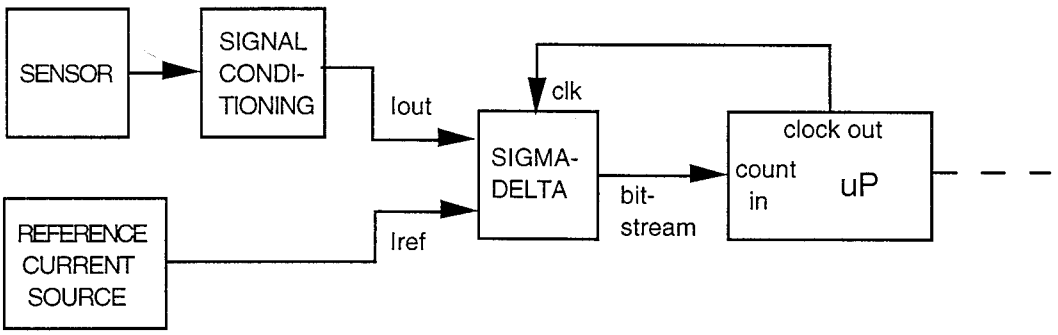

Fig. 4.2.2.2.1. One-sensor measurement configuration using a sigma-delta bitstream converter

4.2.2.3. A multi sensor configuration

As the BARMINT microsystem contains more than one sensor, the basic configuration as presented in figure 4.2.2.2.1 has to be expanded to a multi-sensor configuration. In this paragraph the most suitable multi-sensor configuration for the BARMINT microsystem will be presented and discussed. For large and complex multi-sensor measurement systems, in [Hui94] and [Mei94] the use of the standard I^2C or IS^2 serial bus is proposed. To this bus several different sensors can be connected and the bus can be controlled by a microprocessor. Both the I^2C and the IS^2 serial bus offer a highly flexible and advanced form of communication using a standardized protocol. However, each sensor has to be equipped with a serial bus interface that is rather complex. The bus protocol also requires that each sensor generates fully digital output code. Therefore, within the BARMINT microsystem this kind of bus configuration is far too complicated. Moreover, the I^2C and the IS^2 serial bus is intended to be used for communication with sensors that are not implemented in the same package. For internal communication between sensors and a microprocessor implemented in the same package, as in the BARMINT microsystem, in [Hui86] the use of a more simple semi-digital bus is proposed. The configuration of the semi-digital bus is presented in figure 4.2.2.3.1.

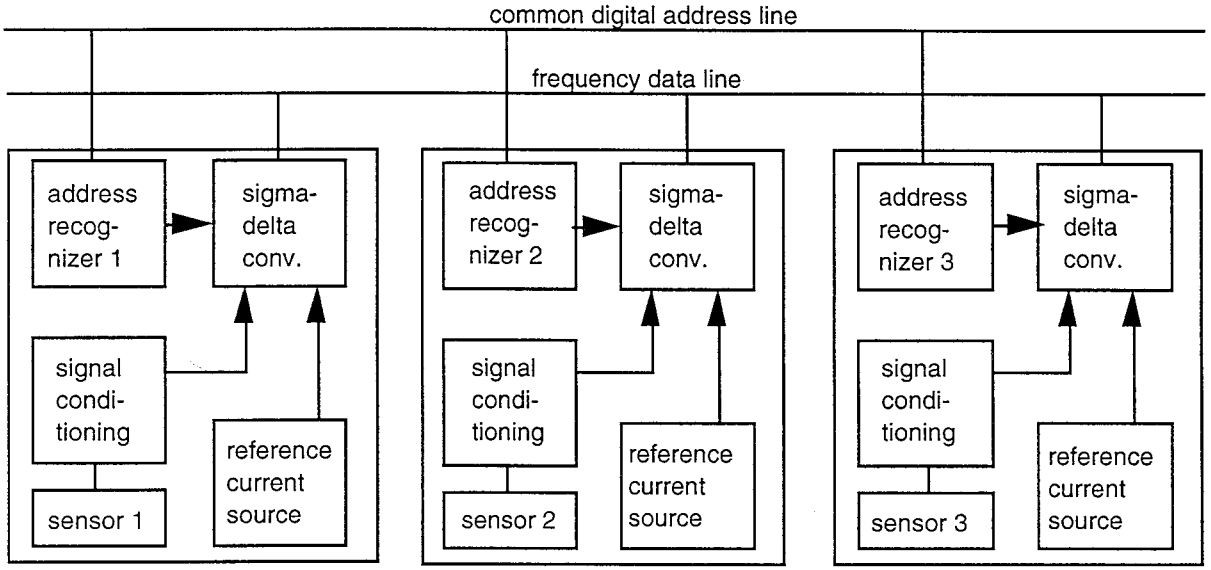

Fig. 4.2.2.3.1. Semi-digital bus structure for internal communication in a microsystem

The semi-digital bus is very suitable for use in combination with the sigma-delta bitstream conversion technique. The frequency output signals of the bitstream converters can be directly connected to the common frequency data line. A sensor module can be selected by putting its digital address on the common address line. The address recognizer of the concerning sensor module switches its bitstream converter to the frequency data line. The microprocessor that controls the semi-digital bus, reads the bitstream on the frequency data line and converts it into fully digital code (by its special counter input). Afterwards, it can be internally processed, stored into a memory or transmitted to a higher computer level.

When using the configuration as presented in figure 4.2.2.3.1 in the BARMINT microsystem, for each sensor a sigma-delta converter would be necessary, which implies a total number of sixteen sigma-delta converters. Moreover, sixteen reference current sources have to be implemented, which will not be an easy task. In order to increase yield and feasibility, this number should be reduced by using additional multiplexing techniques.

For the BARMINT microsystem, we propose the use of one sigma-delta bitstream converter for the eight sensors on the sensor module and one sigma-delta converter for the eight temperature sensors on the VLSI module. Two additional 8-to-1 multiplexers are necessary to obtain a selective connection between the sensor interfaces and the sigma-delta converters. Because the sigma-delta converters are current-driven (thus the sensor interfaces have current-mode output signals) these multiplexers have to switch currents, so should be optimized for this purpose. The multi-sensor configuration for the BARMINT microsystem will then be as presented in figure 4.2.2.3.2.

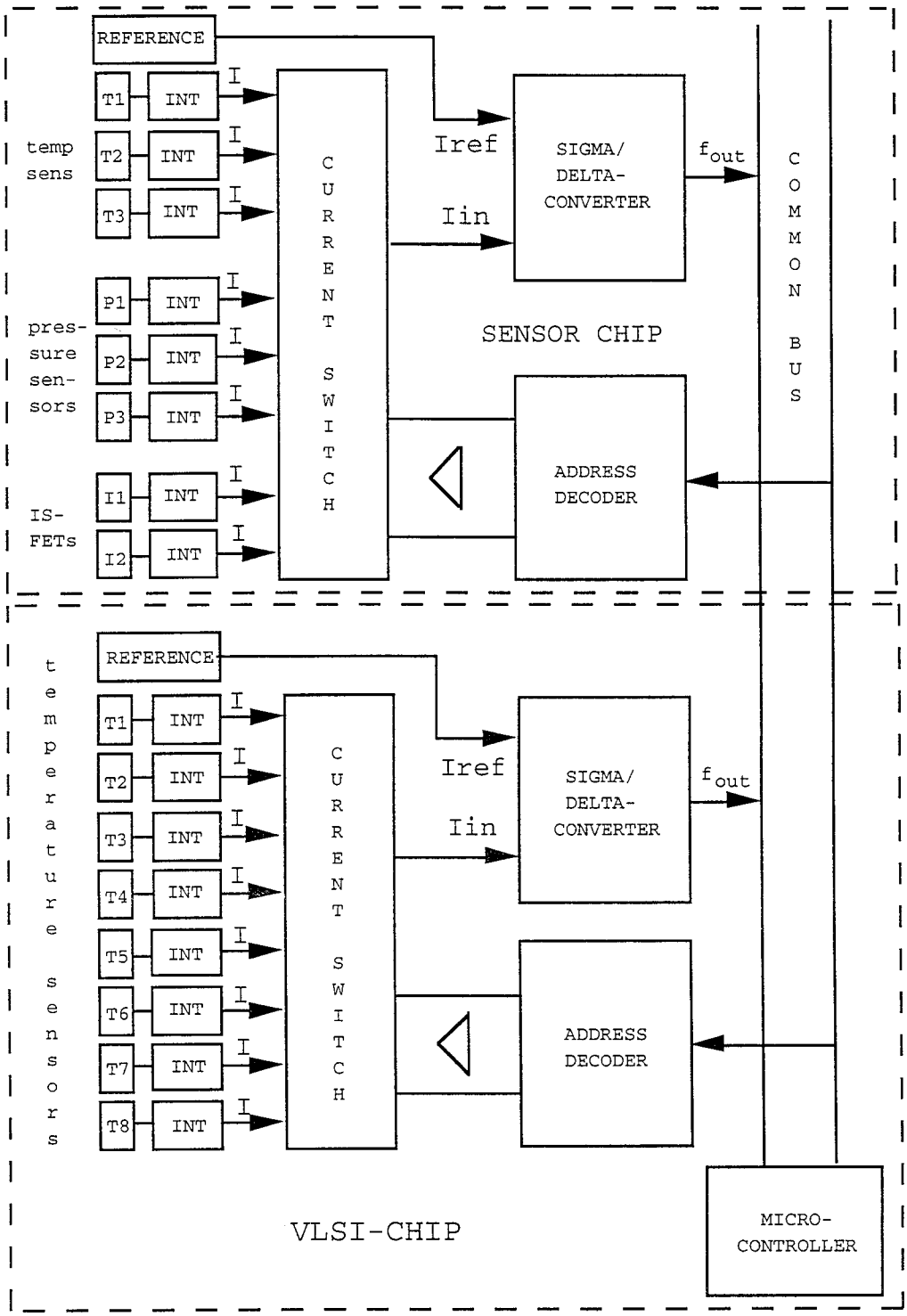

Fig. 4.2.2.3.2. The multi-sensor configuration for the BARMINT microsystem

In the configuration of figure 4.2.2.3.2, each sensor has its own address, which is recognized by the address decoder. When the microcontroller puts an address on the common bus, the address decoder will offer the address as control data to the current switch, which selects the concerning sensor interface. The output current of this analog sensor interface will drive the sigma-delta converter. The sigma-delta converter will generate a bitstream, which represents the semi-digital version of the measurand. The microcontroller will read in this bitstream during a certain time and will convert it into fully digital code, which can be processed further.

4.2.2.4. The actuator part of the electrical configuration

As the BARMINT microsystem has only one actuator, a thermopneumatic micropump, the actuator part of the electrical configuration can in principle be very straightforward.

As stated before, this micropump is properly actuated by applying a square wave with an amplitude of 10 V and a frequency of 10 Hz to the heating resistor. For this reason, a DA converter as presented in the actuating part of figure 4.2.2.2 will not be necessary. The control signal for the micropump can simply be derived from a clock signal of the microcontroller by a frequency divider. The actuator control configuration for the BARMINT microsystem is presented in figure 4.2.2.4.1. The pump can be activated by putting its digital address on the bus, which is recognized by its address decoder. The address decoder will generate an activation signal for the power driver, that starts to supply the periodical pulse voltage to the heating resistor of the micropump.

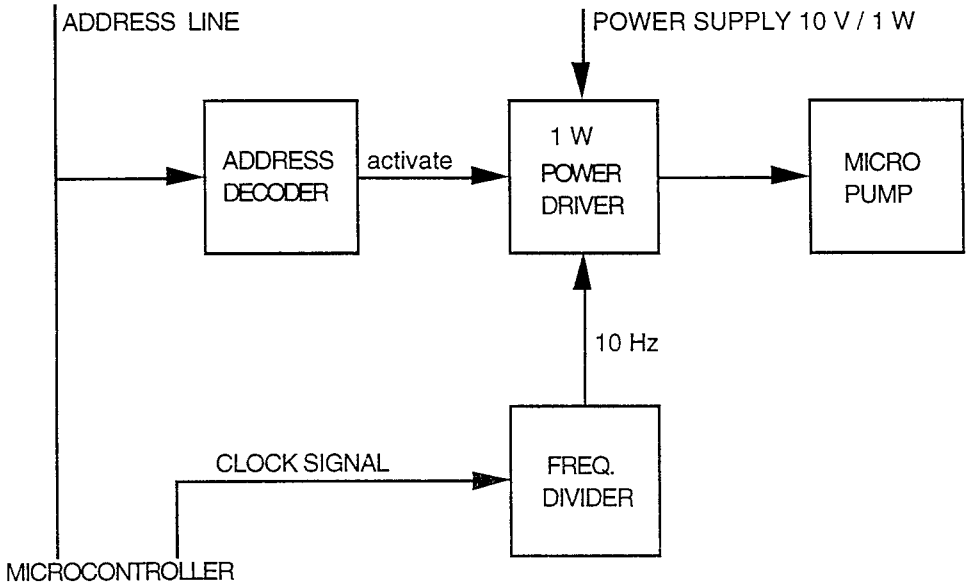

Fig. 4.2.2.4.1. The actuator control configuration for the BARMINT microsystem

The implementation of the 10 V, 1 W power driver is a point of discussion within the BARMINT project. First issue is that the optical power supply module of the microsystem will not be capable to deliver this power. Second issue is how to transport this power through the microsystem and third issue is the availability of devices that can switch this voltage and power.

The power supply module of the BARMINT microsystem is based on photovoltaic conversion, which is a process with low efficiency. It is therefore impossible that this module will be designed to deliver an output power of more than 1 W with a voltage of 10 V [LAA95b]. The micropump can therefore not be supplied by the BARMINT power supply module and has to be fed by an external voltage. In order to avoid electromagnetic disturbances caused by the switching currents of the micropump, this external voltage should be connected as close to the micropump as possible. Because a 10 V, 1 W signal can not be controlled by standard CMOS devices, we propose the use of a hybrid power driver that could be glued on top of the micropump module. This is the only feasible way for supplying the micropump of the BARMINT microsystem. The proposed configuration is schematically represented in figure 4.2.2.4.2.

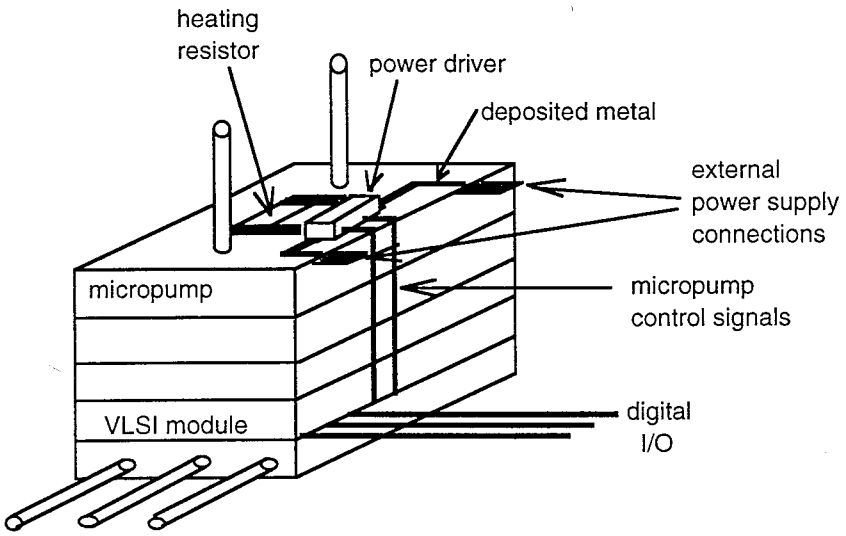

Fig. 4.2.2.4.2. The power supply of the micropump in the BARMINT microsystem

4.2.2.5. The complete concept of the electrical configuration

Finally, the complete concept for the electrical configuration of the BARMINT microsystem can be represented by combining the results of the preceding paragraphs. The concept is given in figure 4.2.2.5.1. In this figure, the microsystem is divided into three parts, the micropump module, the VLSI module and the sensor module. The abbreviation T stands for temperature sensor, P stands for pressure sensor and I stands for ISFET. The sub-modules indicated by INT represent the analog interfaces or signal conditioning circuitry.

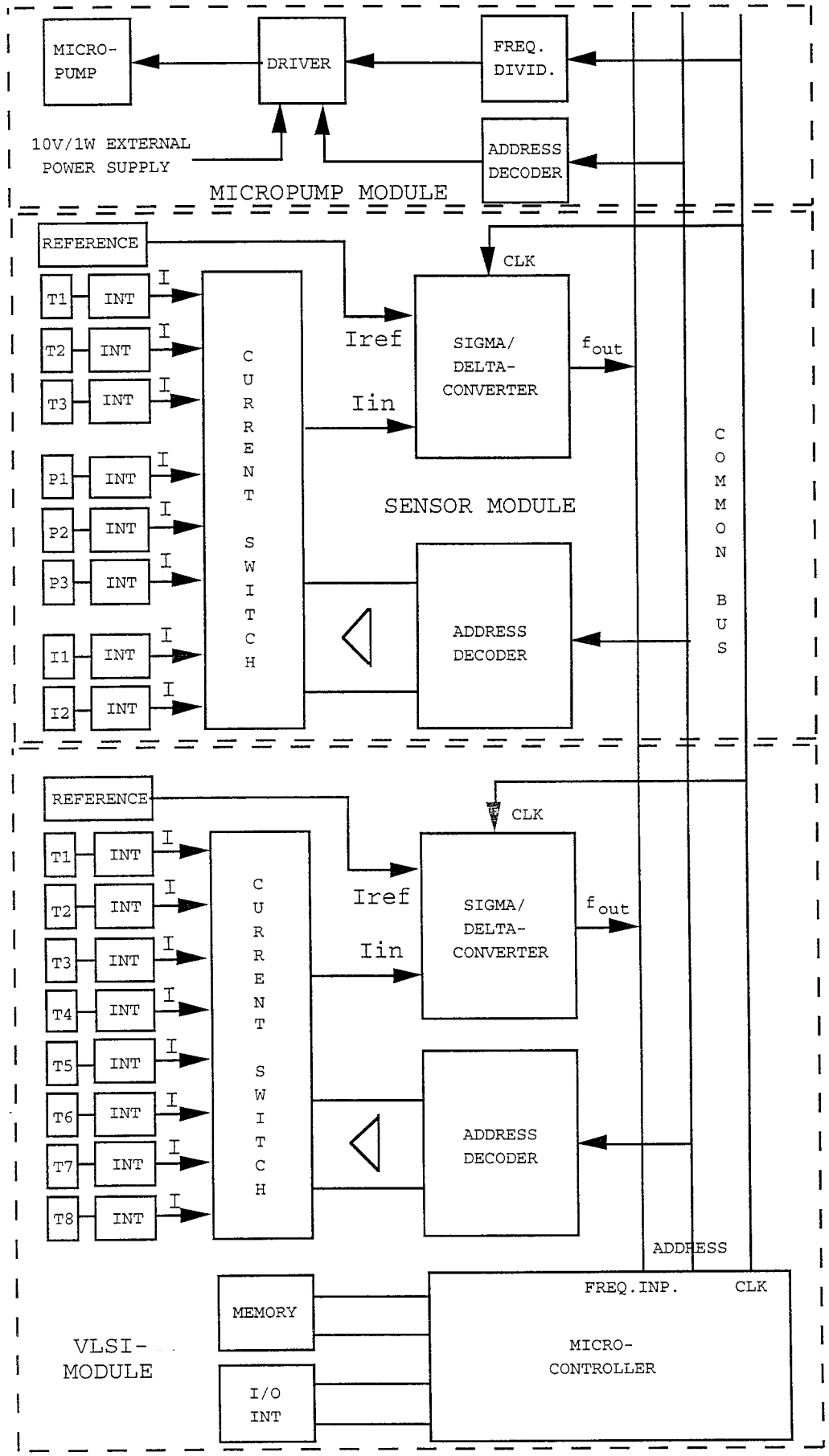

Fig. 4.2.2.5.1. The concept for the electrical configuration of the BARMINT microsystem

4.3. Electrical architecture of the BARMINT demonstrator

In this section, the system level concept of the BARMINT medical demonstrator is worked out in detail. This includes a discussion of the microcontroller, the sigma-delta converter and the common bus structure with additional interface circuitry. This structure can be adopted by any complex system which includes many sensors and actuators. The different choices done take into consideration the restriction and constraints implied by the system specification, in term of limited surface, power consumption, noises, etc.

4.3.1. The microcontroller

In order to reduce power consumption and complexity and to increase flexibility, for the BARMINT microsystem the set of tasks that should be assigned to the microcontroller should be reduced to only elementary tasks [CSE95, Has90].

4.3.1.1. Primary set of tasks for the microcontroller

In modern measurement and control systems, a microcontroller is used for advanced communication with sensors and actuators, for data processing and for communication with higher computer levels. When applying this principle to a microsystem consisting of sensors and actuators, a configuration as presented in figure 4.3.1.1.1 is obtained.

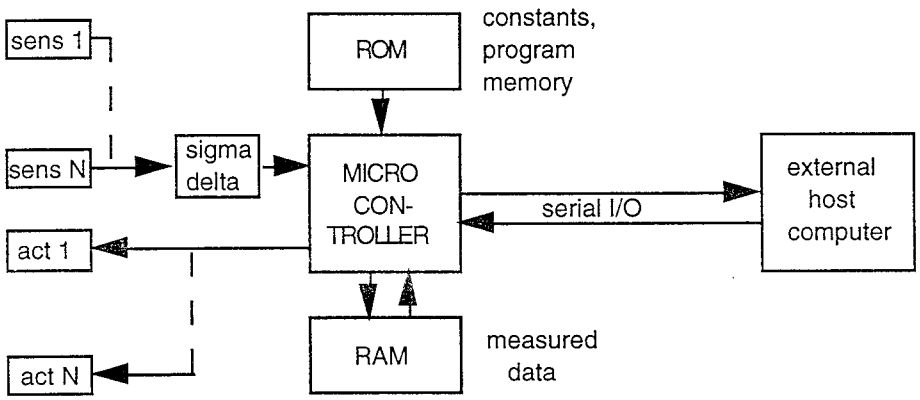

Fig. 4.3.1.1.1. Position of the microcontroller within a microsystem

In the configuration of the microsystem as presented in figure 4.3.1.1.1, the following set of tasks could be assigned to the microcontroller [Has90, Naj88]:

- addressing the sensors in a certain sequence, in order to select them for measuring or calibration purposes,
- converting the semi-digital bitstream, coming from the sigma-delta converter, into a fully digital code, representing the measured value of a certain sensor,
- acquisition and storage of calibration constants, obtained by measurements performed when calibrating the sensors,
- temporary storing the measured value of each sensor into local (on-chip) memory and convert it into correct dimensions by adding or multiplying with calibration constants,
- transmission of measured data to the host computer and reception of control data from the host computer,
- compensation for cross sensitivities, offset and non-linearities of the sensor output signals by performing the necessary calculations or the use of look-up tables,
- controlling the actuators of the microsystem by sending enable or disable signals when certain

measured quantities have reached critical values. These critical values also have to be guarded by the microcontroller,

- regularly performing diagnostic selftests, in order to ensure that the complete system is operating correctly,

- generating synchronization or handshake signals that are necessary for a reliable communication protocol between controller, sensors, actuators and host computer.

4.3.1.2. The implementation of the microcontroller in a microsystem

In the BARMINT microsystem, the microcontroller has to be located on the chip of the VLSI module. For the implementation, two different approaches can be used [Gan92]:

- The monolithic approach, which means that the circuitry of the microcontroller is integrated in the same substrate as the other circuitry on the VLSI chip. This offers the advantage that no additional mounting and bonding steps are necessary, which improves the reliability of the system [Las93]. Besides, no chip surface is lost by the bonding pads and the free space between the pads and the mounted die.

- The hybrid or Multi Chip Module (MCM) approach, which implies that a separate die of a microcontroller is mounted on the VLSI chip. The remaining surface on the VLSI chip can then be used for implementing additional circuitry. This has the advantage that both technology and supplying company of the microcontroller can be chosen independently of the other circuitry on the VLSI-chip.

In the following, we will shortly discuss some issues concerning the implementation of a microcontroller in the BARMINT microsystem:

- physical dimensions: when only limited area is available for locating a microcontroller on a substrate, this could be a factor restricting the complexity of the controller. However, when considering the VLSI chip of the BARMINT microsystem, this should not pose any problem. The surface of the VLSI chip is 100 mm^2 of which at maximum 20 % will be used for bonding pads, temperature sensors and additional interface circuitry. The remaining area is largely sufficient for implementing any kind of microcontroller, with both hybrid and monolithic approach [Sag95, Wei92].
- yield: as the yield goes down when the chip surface increases, there will always be a need to keep circuits implemented in silicon as small and as simple as possible. Naturally, this aim should also be pursued for the VLSI chip of the BARMINT microsystem.
- testability: as soon as a microcontroller is embedded in a larger system (hybrid or monolithic), its I/O connections are no longer physically accessible, which makes testing of the controller difficult or even impossible. In the BARMINT microsystem, this problem can be solved by implementing additional test circuitry on the VLSI chip. Boundary scan chains give the possibility to observe all I/O connections of the embedded microcontroller in a sequential way [Mal94].
- power consumption: in the BARMINT microsystem, power consumption is a very important issue, as the photo-voltaic supply module provides an electrical output power of only a few hundred mW's. Commercially available multi-purpose microcontrollers have a power consumption in the same range [Int88], so this would imply serious problems.

  When implementing a microcontroller in the BARMINT microsystem, its power consumption has to be dramatically minimized. This can be done in three ways: (1) by reducing the complexity of the controller, reducing its instruction set, internal bus width and amount of ROM and register memory, (2) by limiting its operating frequency, as for CMOS circuits the power consumption is proportional to the operating frequency, (3) by switching the controller in a "power down" or "stand by" mode, when it has no processing tasks to perform.

The minimal operating frequency of the microcontroller will mainly be determined by the sampling frequency of the sigma-delta converter at its input. However, for sensor measurements the operating frequency should not pose any problem, as sensor signals are mainly low frequency signals.

The "power down" or "standby" mode is a facility on a microcontroller that gives the opportunity to minimize mean power consumption. As soon as the microcontroller has no processing or measuring tasks to perform, it can be switched into a mode in which it consumes only a fraction of normal electrical power and is not able to operate. It is only able to hold the contents of its RAM cells. The controller goes back into its operating mode by giving an interrupt.

- flexibility and observability: when assigning a large number of data processing tasks to the on-board microcontroller, it will be more difficult to influence and observe sensor characteristics from outside, by for example the external host computer. Calibration constants, compensation coefficients and look-up tables could be stored in local on-chip memory (ROM) of the microcontroller. This gives the opportunity to perform complete sensor data processing in the microcontroller. In the same direction, it is to be expected that there will be a continuous need to observe the sensor characteristics and to adjust and reoptimize compensation coefficients and calibration constants. In order to achieve this desired flexibility, it will be better to perform the sensor data processing in the external host computer, instead of in the on-board microcontroller.

4.3.1.3. Properties and tasks of the BARMINT microcontroller

An important specification determining the complexity of the microcontroller is the word width of the internal and external busses, registers and CPU. When using an N-bit microcontroller, sensor data can be represented by N-bit digital words. This results in a quantization error of:

$$(2^{-N} - 1) \times 100\ \% \qquad (1)$$

Besides, with an N-bit external address bus, a total number of 2^N different I/O devices can be directly addressed. When choosing N=8, which results in the use of a popular 8-bit microcontroller, the quantization error is about 0.4 % and 256 different I/O devices can be directly addressed. When considering the specifications of the temperature-, pressure- and ISFET sensors, a maximum sensor accuracy of about 0.5 % can be expected. Therefore, when using an 8-bit microcontroller in the BARMINT microsystem, the measuring accuracy will not be limited by the controller. Besides, the 256 addressable I/O devices farly exceeds the number of sensors and actuators in the microsystem. An 8-bit microcontroller can therefore be used in the BARMINT microsystem.

The tasks that should be assigned to the microcontroller are the following:

- Sensor measurements: in order to minimize the number of data processing tasks for the BARMINT microcontroller, for the sensor measurement we propose the following cycle. The microcontroller addresses the sensors in a certain fixed sequence and reads in their bitstream output signals. The microcontroller converts the bitstreams into fully digital codes, as discussed before (so a microcontroller with a frequency counter input is required) and stacks every code into local memory. In this way, a small array of digital data (representing the measured values of all the sensors) is stored in the on-chip RAM of the microcontroller. As there are only 16 sensors, only 16 bytes of internal RAM are necessary for the measurements. Then, the complete array of sensor data is serially sended to the external host computer, where it can be processed. The sensor measuring cycle is represented in figure 4.3.1.3.1.
- compensation: compensation means eliminating cross sensitivities, non-linearities, offset and drift in the sensor output signals. In several earlier presented smart sensor structures this is done in the digital domain, by assigning extended signal processing tasks to the microcontroller

[Naj88, Bri83, Bri85]. However, in the BARMINT microsystem these tasks have been displaced to the sensor interface circuits. The interface circuits dispose of digital compensation inputs, which have to be provided with the proper control signals. The only function of the microcontroller hereby is to transfer the compensation data from the host computer to the sensor interfaces.

- calibration: each sensor in the BARMINT microsystem has to be calibrated, which means that a unique relation between input quantity and output signal has to be defined. In the BARMINT microsystem, the sensors can be assumed to give a linear output signal (within the 8-bit resolution) in which cross-sensitivities have been eliminated by compensation. Therefore, each sensor can be calibrated by forcing two (accurately known) different values to the input quantity of the concerning sensor.

  The output signals, measured when forcing the two different input values, can be used to describe the linear relation $Y = A X + B$ between sensor input quantity X and sensor output signal Y. When performing a measurement with the calibrated sensor, the relation $Y = A X + B$ has to be recalled to derive the measured input quantity X from the output signal Y. Therefore, the coefficients A and B of this relation have to be stored as calibration constants.

  For the BARMINT microsystem, we propose to displace the derivation of X from Y to the host computer. This has several advantages: (1) the microcontroller does not need to have any arithmetic instructions, so its instruction set can be considerably reduced, (2) the calibration constants do not have to be stored in the on-chip ROM of the microcontroller, which reduces the amount of required memory and (3) it increases the flexibility when regularly performing recalibrations, as already discussed.

- actuator control: as the BARMINT microsystem has only one actuator, its control function can be very simple. In order to provide simultaneous operation of the micropump when performing measurements, it should be controlled by sending a set or reset pulse to its interface. In that case the pump can be started by sending a set pulse, and it remains running untill a reset pulse is sended. The micropump is controlled by the host computer. This means that in the host computer the decision will be taken to start or stop the micropump. This could easily be changed in a later stadium, as it is implemented software-matic.

Finally, we give an overview of the most important requirements for the microcontroller:

- to be implemented in CMOS technology, in order to reduce power consumption,
- power down or standby facility available,
- 8-bit internal word width,
- frequency counter input available,
- 32 bytes of RAM is sufficient,
- required amount of ROM not yet determined, but only for a simple microprogram,
- serial I/O port available,
- a few interrupt inputs available for starting measurements or control,
- simple set of only data transfer instructions.

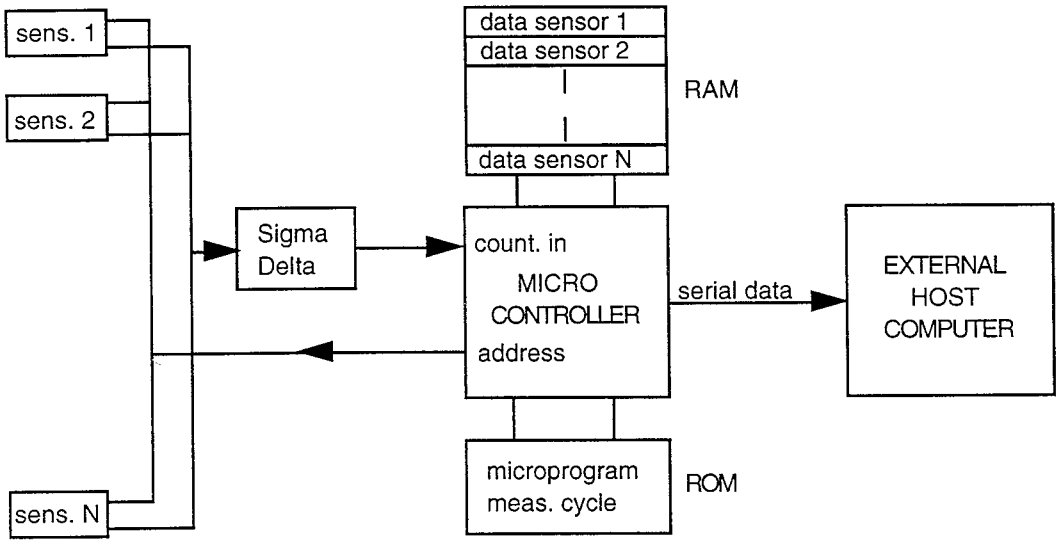

Fig. 4.3.1.3.1. The sensor measuring cycle proposed for the BARMINT microsystem

4.3.2. The Sigma-delta converter

When complete integration of sensing functions and electronic circuits has to be achieved, design techniques have to be applied that show high robustness against deviations in component characteristics and do not rely on high accuracy component matching. When considering the on-chip AD conversion technique for sensor applications, this implies that AD conversion at the Nyquist rate (like flash, recursive and successive approximation AD converters) should be rejected. These direct AD converters use binary weighted arrays and therefore rely heavily on component matching properties [San93].

A typical modern CMOS process offers a speed performance which is often far beyond the requirements and in the future, speed will further improve. Hence, it would be interesting to trade off speed for accuracy and obtain some accuracy advantage at the cost of a speed limitation. This trade off has been achieved by the development of the sigma-delta AD converter, a converter that digitizes its analog input signal at a frequency far above the Nyquist rate (which is called oversampling).

Oversampled data converters form an alternative where a high resolution, independent of component matching properties, is obtained at the cost of a speed reduction and some additional digital postprocessing. As speed is generally not a bottleneck in sensor applications and digital postprocessing can be performed by the central microprocessor of a microsystem, the oversampled AD converter seems perfectly adapted to sensor measurements.

4.3.3. The sensor interface modules

In this paragraph will be discussed how each sensor and its signal conditioning circuit can be completed to a fully equipped sensor interface module that can directly be integrated in the BARMINT multisensor configuration.

First will be discussed how the compensation for cross-sensitivities, offset and drift, as implemented in each signal conditioning circuit, can be controlled by the central microcontroller of the BARMINT microsystem. Besides, it will be shown how the addressable current switches, presented in the BARMINT system level concept of figure 4.2.2.5.1, can be merged with the sensor interface modules. As in a CMOS process very simple current switches with high performance can be made, the sensor addressing facility can easily be integrated in the sensor interface modules.

4.3.3.1. Compensation control for the sensor interface modules

The sensor signal conditioning circuits have a current-mode output signal and an array of digital control inputs. The necessary digital data for these control inputs has to be determined during calibration of the concerning sensor. A digital word has to be found that gives a maximal reduction of cross-sensitivities, offset and drift in the output signal of the concerning sensor interface.

When the optimal values for the digital control signals have been found, they have to be stored in non-volatile memory. As it is technically unfeasible to implement non-volatile memory (ROM) in the interface modules of the sensor chip, it should be stored elsewhere. The compensation data of the sensor interfaces are stored in the memory of the external host computer. In this way, a maximal degree of flexibility is obtained.

When the compensation data is stored outside the microsystem, it has to be transfered to the sensor interface circuits each time the microsystem is started up. This has to be done during a so-called initialization step. During this step, the compensation data that is stored in the host computer, is transfered to the interface circuits of the sensors.

In the sensor interface modules simple memory latches can be implemented, which hold the compensation data during the measurements. A digital latch keeps its information untill the supply voltage is switched off. This means that each time the microsystem is switched on, an initialization step has to be performed. The proposed control configuration for the sensor interfaces of the BARMINT microsystem is schematically represented in figure 4.3.3.1.1.

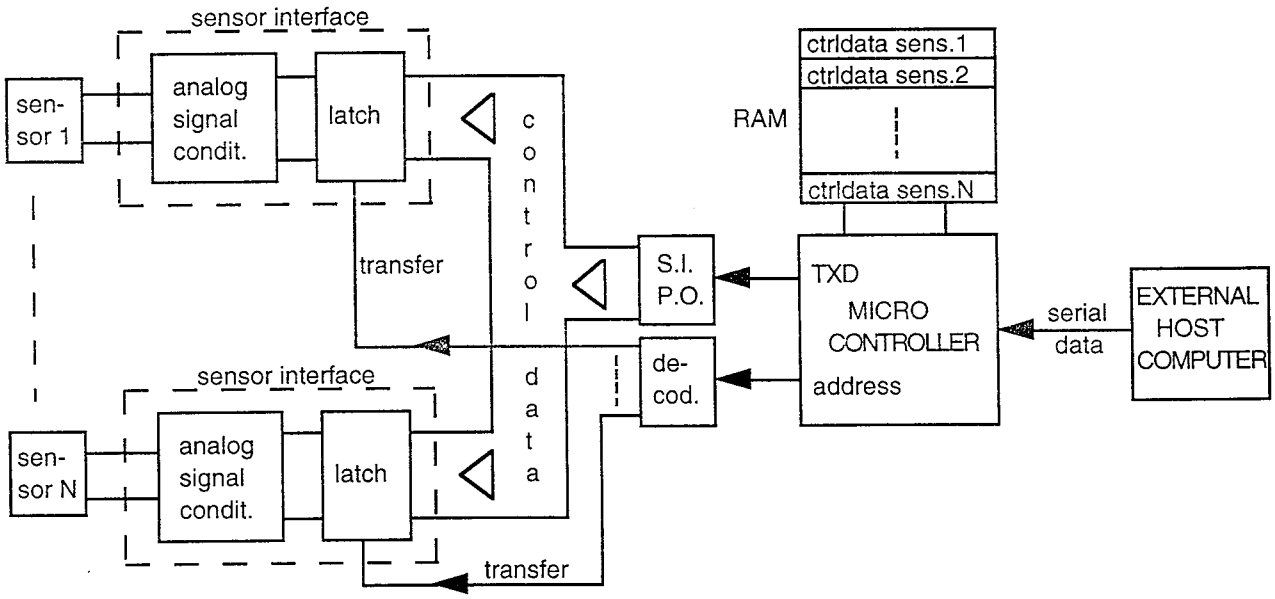

Fig. 4.3.3.1.1. The transfer of compensation control data from host to sensor interfaces

As soon as the BARMINT microsystem is activated, it requests the compensation data of all its sensors from the host computer. The host transmits serially this complete package of compensation data to the microcontroller and the controller stacks the data into its local RAM.

Afterwards, the microcontroller transfers this data word for word to the concerning sensor interfaces. This is also done serially in order to minimize the number of connection wires between sensors and microcontroller. Therefore, close to the sensors a S.I.P.O. register is located (Serial Input Parallel Output) that converts the serial datastream into parallel data.

When the microcontroller has sent one word of compensation data (bound for one sensor), and it is converted into parallel form, the microcontroller selects the concerning sensor interface by sending

(also serially) its address. The addressdecoder decodes the serial address and sends a 'transfer' pulse to the latch of the concerning sensor interface. This latch will read in and hold the word of compensation data, sended by the microcontroller.

The cycle as described above has to be repeated in a fixed sequence, until each sensor interface has read in its word of compensation data. When this initialization step has been completed, the sensor measurements can be started.

4.3.3.2. Addressing facility for the sensor interface modules

In the BARMINT system level concept of figure 4.2.2.5.1, addressable current switches are implemented between sensor interfaces and sigma-delta converters. In this paragraph we will show how these switches can be merged with the interface circuits. As the circuitry for the sensor module is made in a CMOS process, we have the opportunity to implement a current switch with high performance by using only an array of single MOS transistors. For the BARMINT microsystem we propose to merge the array of current switches with the sensor interface modules, as shown in figure 4.3.3.2.1.

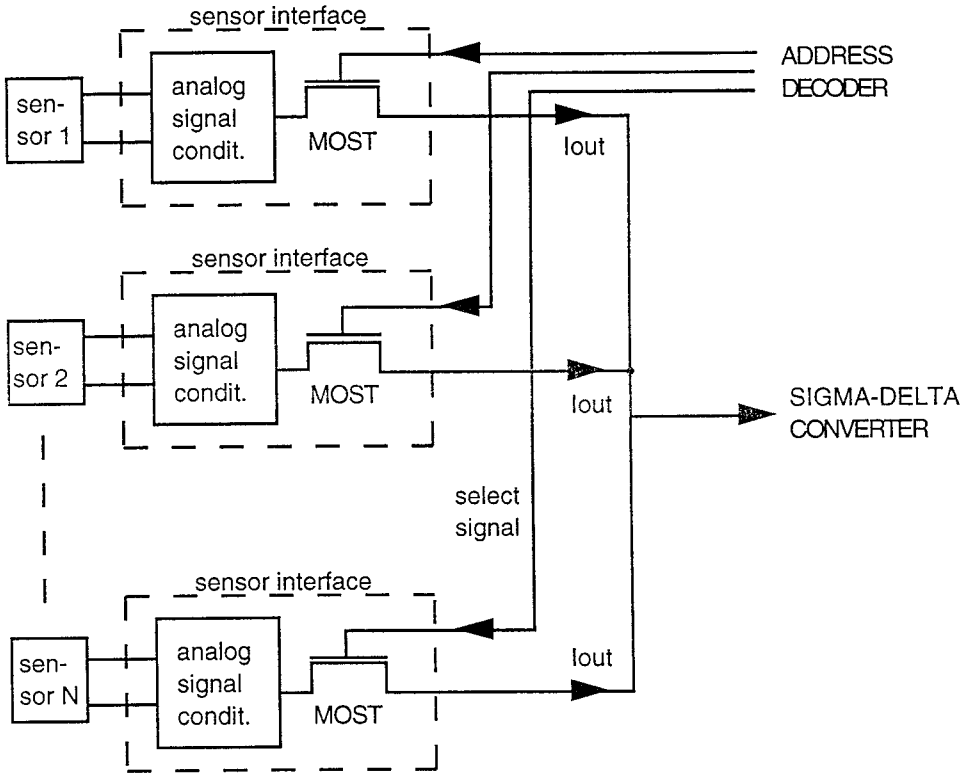

Fig. 4.3.3.2.1. Merging addressable current switches with sensor interface modules

That a single MOS transistor acts as a high-performance current switch, has already been shown in [See89], [Wou94] and [San83]. In these papers high-performance multi-sensor interface circuits are described that use single MOS transistors as a current switching element in a multiplexer.

Finally we can conclude that the sensor interface modules of the BARMINT microsystem have to be extended with two facilities: a digital memory latch, for storing the compensation data, and a MOS current switch for addressing the concerning sensor. Therefore, the configurations for the sensor interface circuits as presented in figures 4.3.3.1.1 and 4.3.3.2.1 have to be combined in order to obtain a fully equipped interface. This will be done for the interface circuits of the temperature sensors, the reference source, the pressure sensors and the chemical sensors.

4.3.3.3. Temperature sensor interface module

It is proposed to provide the signal conditioning circuitry for the temperature sensors with eight digital control inputs. With these control inputs the zero point and the slope of the output characteristic can be adjusted. As the microcontroller of the BARMINT microsystem has an 8-bit wordlength, the compensation data for the temperature sensor interface can be transfered in one cycle and has to be stored in an 8-bit latch. The schematic of the complete temperature sensor interface for the BARMINT microsystem is presented in figure 4.3.3.3.1.

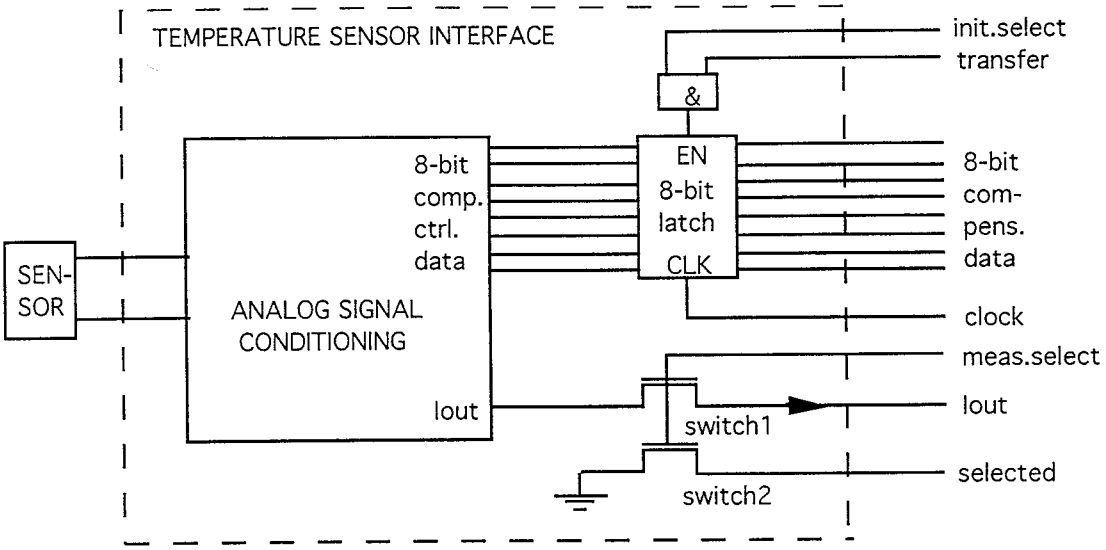

Fig. 4.3.3.3.1. Completely equipped BARMINT temperature sensor interface module

The 8-bit latch will read in the compensation data (provided by the microcontroller) on the active edge of the clock signal when both 'init.select' and 'transfer' are a logical '1'. The signal 'init.select' is controlled by the sensor address decoder and the signal 'transfer' is a pulse, generated by the microcontroller.

Addressing the temperature sensor for measuring purposes is done by the address decoder, that makes the input 'meas.select' a logical '1'. Switch 1 is activated and the output current I_{out} is connected to the sigma-delta converter, and can be read in by the microcontroller. Switch 2 is also activated and makes the high-impedance line 'selected' a logical '0'. In this way the microcontroller can observe that the concerning sensor is selected and can start its measurements.

4.3.3.4. Reference source interface module

A temperature sensor can also be used as a reference current source, when it is properly designed and adjusted.

The reference source choosen in the BARMINT system delivers an output current that can be made independent of temperature by properly controlling its digital compensation inputs. As we proposed to use eight control inputs, for the reference source nearly the same interface configuration can be used as for the temperature sensor (figure 4.3.3.3.1). The only difference is the absence of the current switch for addressing facilities. The reference current source does not need to be multiplexed, as it is constantly connected to the sigma-delta converter. The complete reference source interface module for the BARMINT microsystem will be as presented in figure 4.3.3.4.1.

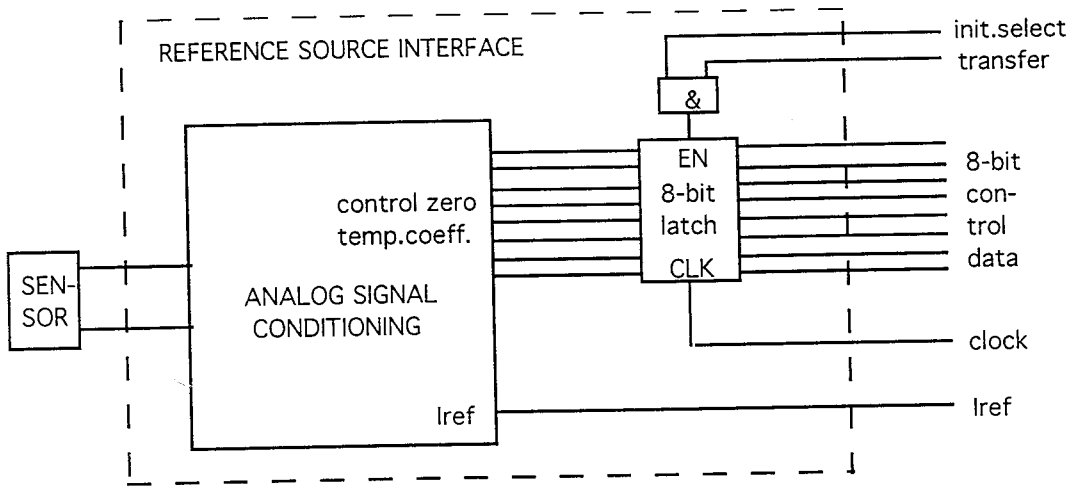

Fig. 4.3.3.4.1. Interface module for the BARMINT reference source

As two sigma-delta converters will be implemented in the BARMINT microsystem (see the system level concept, presented in figure 4.2.2.5.1), also two reference sources as presented in figure 4.3.3.4.1 will be necessary.

4.3.3.5. Pressure sensor interface module

As the circuitry necessary for compensating offset and temperature cross sensitivities is rather extensive, it is proposed to combine these compensation facilities for the three pressure sensors of the BARMINT microsystem. Because of the flexibility of the designed conditioning circuitry, its characteristics can continuously be adapted to the selected pressure sensor. In this paragraph we will present how the three pressure sensors can be interfaced by only one signal conditioning module. Therefore, we consider the configuration of the BARMINT pressure sensor interface module, presented in figure 4.3.3.5.1. In this configuration, that has to be implemented on the sensor module, the three pressure sensors are integrated with one signal conditioning circuit.

One of the three pressure sensors P1, P2 or P3 can be selected for measurement purposes by making the concerning input 'meas.select' a logical '1'. In that case the concerning sensor is supplied by the reference current source and compensated for offset by the offset compensation circuit. These two modules are connected to the concerning sensor as soon as it is selected, by means of MOS switches. The output signal of the sensor bridge is connected to the V-I converter, of which the output current is switched to the sigma-delta converter of the sensor module. The high impedance line 'SD' is also made low, so the microcontroller can observe that a pressure sensor is selected.

The characteristics of the offset compensation module and the reference current source have to be continuously adapted to the concerning pressure sensor. Therefore, both modules have an 8-bit programmable input. The 8-bit input signal for each module is stored in three latches (one for each pressure sensor), and the according latch is automatically connected to the control inputs of the module, by means of 8-bit word multiplexers.

As there are three pressure sensors and two programmable compensation modules, six memory latches are necessary to store all the necessary compensation data. The latches have to be read in during the initialization step, each time when starting up the BARMINT microsystem. Therefore, the pressure sensor interface has six initialization addresses (init.P1A, ... init.P3A, init.P1B, ... init.P3B) to individually select the different latches. In that case, the data on the 8-bit data bus can consequently be stored in one of the latches, when a transfer pulse 'TF' is given. Complete initialization of the pressure sensor interface module will therefore take six address and transfer cycles.

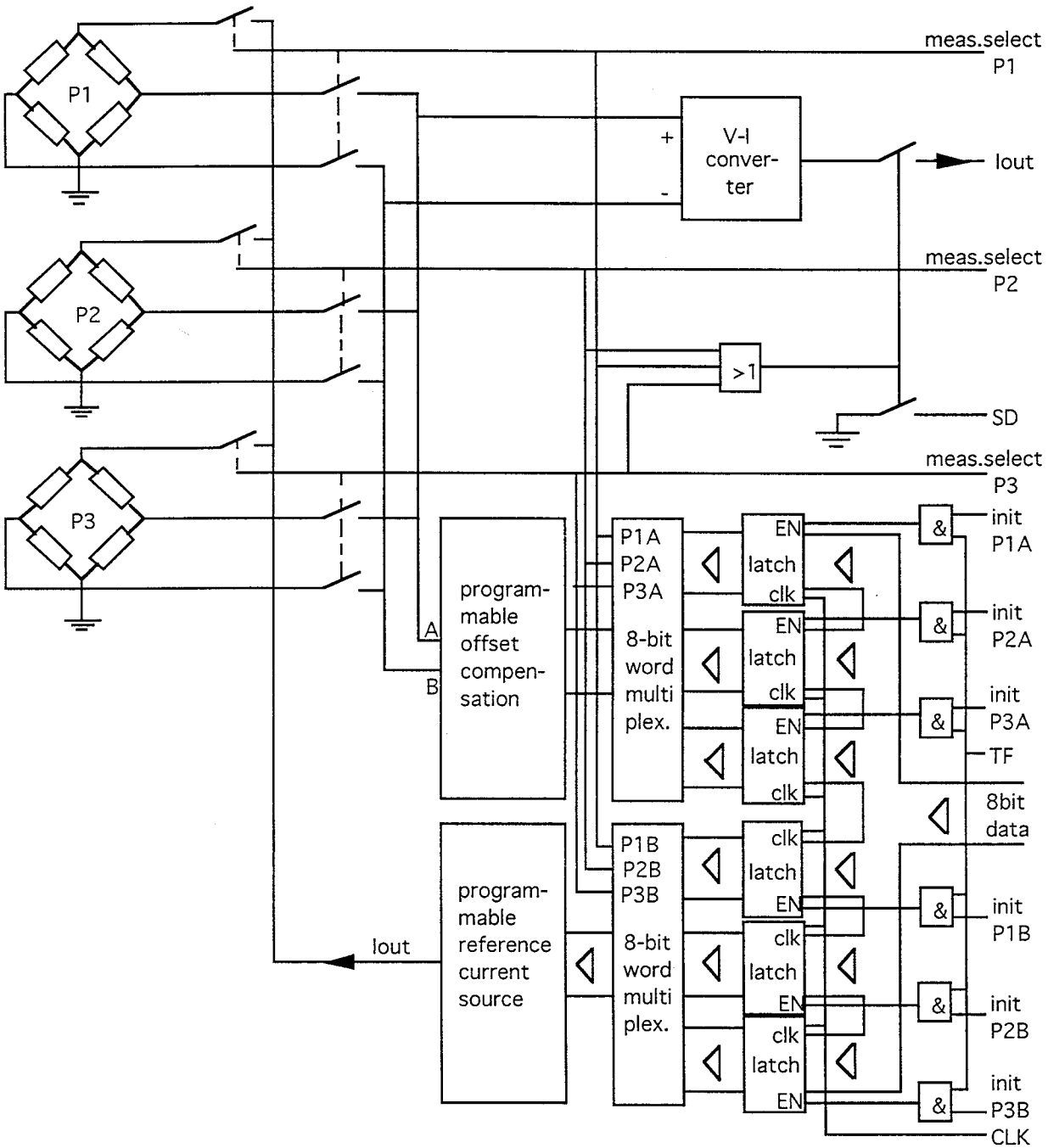

Fig. 4.3.3.5.1. The configuration of the BARMINT pressure sensor interface module

Finally, it should be remarked that of the three temperature sensors that are implemented on the sensor module of the BARMINT microsystem, two will be used within the pressure sensor interface. Both offset compensation circuit and programmable current source in figure 4.3.3.5.1 are based on a temperature sensor.

4.3.3.6. Chemical sensor interface module

The two ISFET chemical sensors of the BARMINT microsystem are implemented in a differential configuration. The internal current sources should be made programmable in order to optimize the output characteristic of this configuration. Therefore, the ISFET interface module will be provided with an 8-bit digital control input. The digital data that controls this input is stored in an additional memory latch, that will also be located in the interface module.

In order to select the ISFET configuration for measurement purposes, its interface module has to be

equipped with an output current switch. The completed chemical sensor interface module for the BARMINT microsystem is given in figure 4.3.3.6.1.

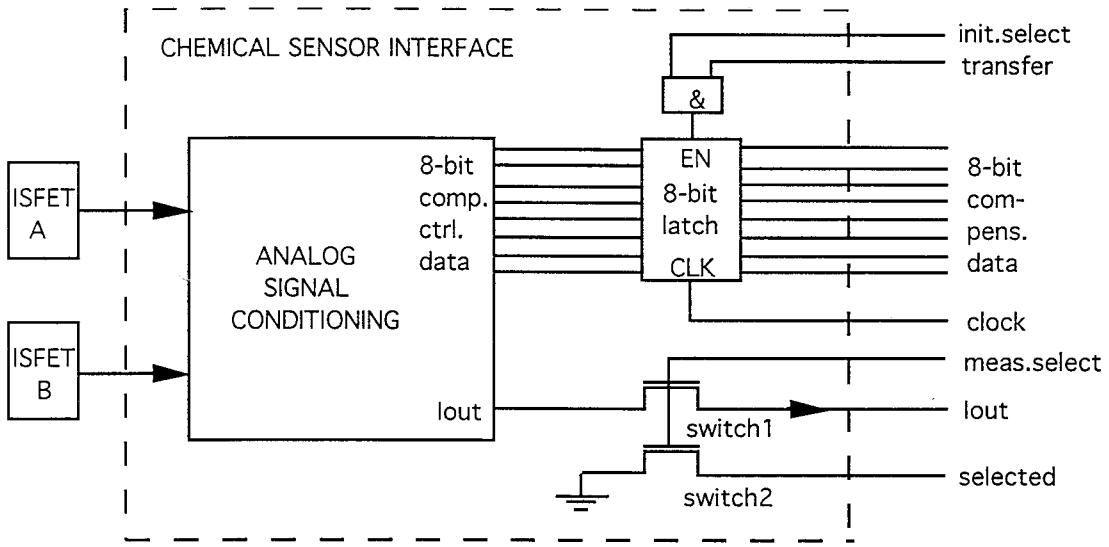

Fig. 4.3.3.6.1. Chemical sensor interface module for the BARMINT microsystem

4.3.4. The common bus configuration

The common bus configuration in which the sensor interface modules have to be implemented is the subject of this paragraph. Starting point for the development of the common bus structure of the BARMINT microsystem, is the system level concept presented in figure 4.2.2.5.1. Connected to the common bus are the sensors on the sensor module, the temperature sensors on the VLSI module and the micropump. The BARMINT common bus has to provide a bidirectional connection between microcontroller and sensors and actuators, for both measuring and initialization purposes.

Beside the bus structure, its peripheral circuits like serial-to-parallel converters and address decoders will also be discussed in this paragraph. On both sensor module and VLSI module these additional circuits are necessary to convert the serial data transmitted over the common bus into a suitable parallel format.

4.3.4.1. Communication with sensors

As presented in the system level concept, on the sensor module will be implemented three temperature sensors, three pressure sensors and two ISFETs. The three pressure sensors are integrated into one interface module, together with two temperature sensors (for compensation facilities). Besides, the two ISFETs are integrated into one interface module, so the configuration for the sensor module has to be changed. On the sensor module, the following circuitry has to be implemented:

- one temperature sensor module (figure 4.3.3.3.1),
- one reference source module (figure 4.3.3.4.1),
- one pressure sensor module (figure 4.3.3.5.1),
- one ISFET sensor module (figure 4.3.3.6.1).

As shown before, there will also be a sigma delta converter and an address-decoder on the sensor module. Moreover, because of the serial communication with the microcontroller, two serial-to-parallel converters have to be implemented. One has to convert the sensor address, that is serially sent by the microcontroller, into a 7-bit parallel form that serves as an input signal for the address-decoder. This means that only seven of the eight sended bits are used for addressing purposes. The bits b0 to b5 are used for selecting the sensor (6 bits = 2^6 = 64 possibilities) and bit b6 is used to

enable the output of the concerning sigma-delta converter. This converter is only connected to the bus when a sensor on the sensor module is addressed.

The second serial-to-parallel converter has to convert the initialization data into an 8-bit parallel form, before it can be read in by the memory latches of the sensor interfaces. The output of this converter has to control an 8-bit data bus that has to be distributed among the sensor interfaces that are located on the sensor module. In this way, the initialization data can be sent to each sensor interface and read in by the selected one. The system level configuration for the sensor module will be as given in figure 4.3.4.1.1.

The common bus for the BARMINT microsystem needs to have six separate lines. These lines are drawn at the right side of figure 4.3.4.1.1 and have the following meaning:

- TF: TransFer line; the microcontroller gives a pulse on this line to enable the sensor latches to read in the initialization data on the data bus.
- SD: SelecteD line; as soon as a sensor is selected by the microcontroller, this sensor makes the SD-line a logical '0'. In this way the microcontroller can detect if a sensor is correctly selected.
- f_{in}: frequency counter input; by this line the bitstream output of the sigma-delta converter is sended to the counter input of the microcontroller, where it is converted into fully digital code.
- -TXD: Transmit Data; over this line, the microcontroller serially transmits the sensor addresses and initialization data (in the form of 8-bit words with start and stop bit).
- -CLR: Clear line; before a measurement or initialization can be started, the registers in the serial to parallel converters have to be cleared, by sending a pulse at the CLR line.
- -CLK: Clock line; the clock signal generated in the central microcontroller is distributed among the sensor interfaces and sigma-delta converters by this line.

The same bus lines are used for the communication with the eight temperature sensors on the VLSI module. When only considering the sensor part on the VLSI module on that module the following circuitry has to be implemented:

- eight temperature sensor modules,
- one reference source module,
- one sigma-delta converter,
- one addressdecoder,
- one address serial-to-parallel converter,
- one data serial-to-parallel converter.

The common bus configuration for the temperature sensors on the VLSI module is presented in figure 4.3.4.1.2. Here, the addressdecoder selects the addresses A16 to A32, that are the addresses for reading out the eight temperature sensors, eight addresses for initialization of the sensor interfaces and one address for initializing the reference source. The VLSI module also has its own 8-bit data bus for distributing the parallel initialization data among the different sensor interfaces.

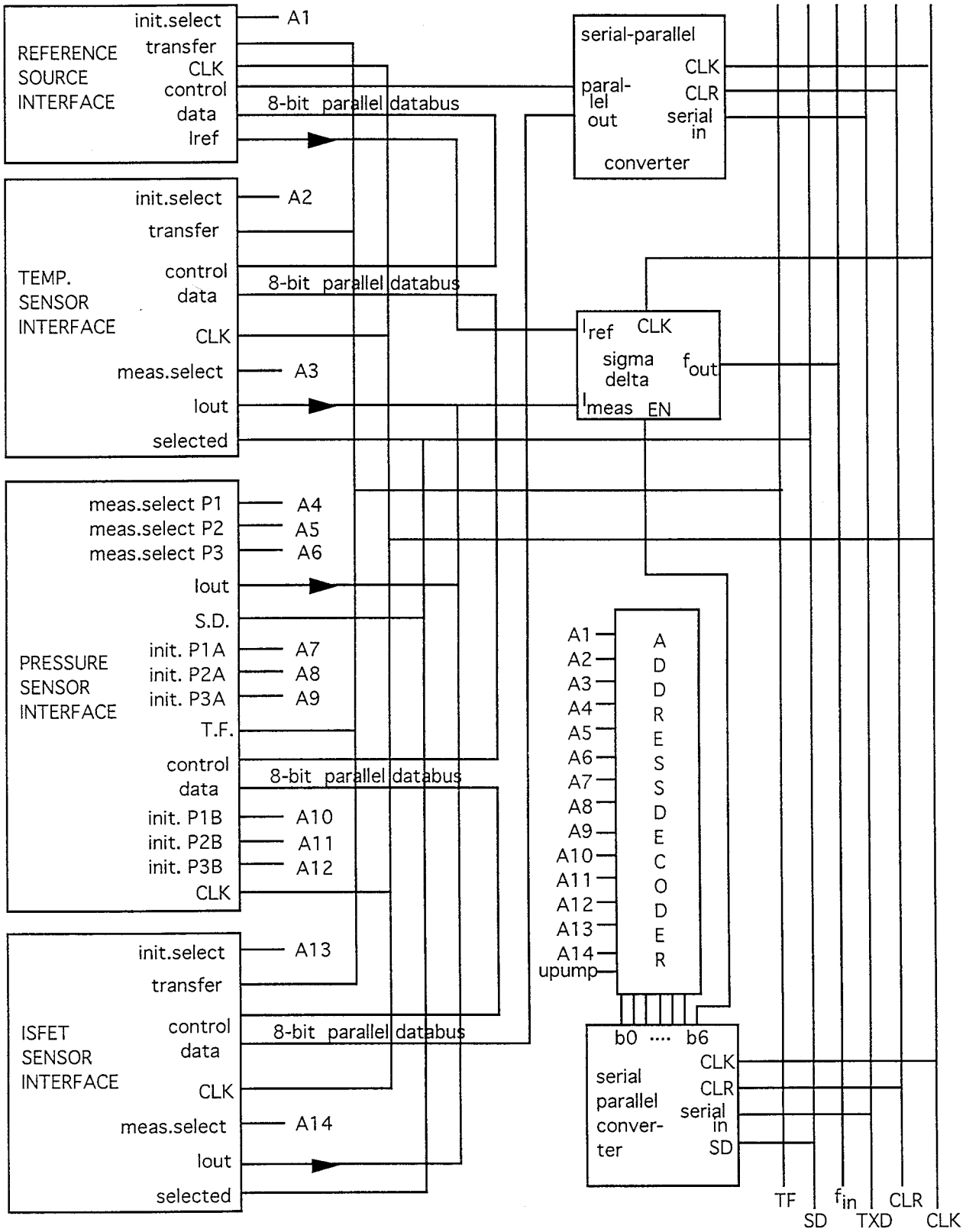

Fig. 4.3.4.1.1. System level configuration of the BARMINT sensor module

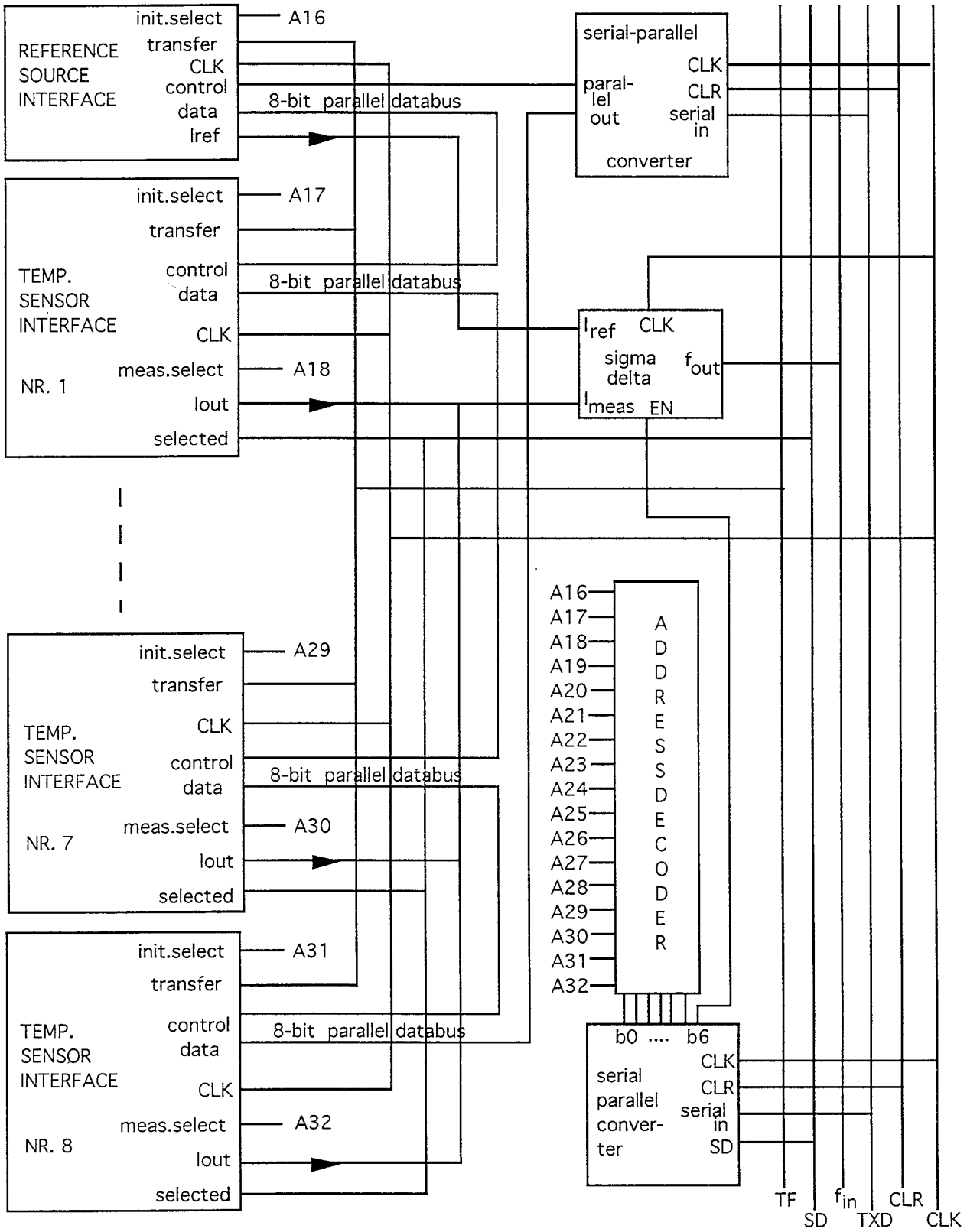

Fig. 4.3.4.1.2. System level configuration of the BARMINT VLSI module

By means of figure 4.3.4.1.1 and 4.3.4.1.2 we will now discuss how a complete measurement cycle and initialization cycle is performed with the sensors of the BARMINT microsystem.

Measurement cycle:

A measurement cycle has to be requested by the host computer. The host sends an interrupt to the on-board microcontroller of the BARMINT microsystem. The microcontroller is woken up and automatically starts the service routine for the measurement cycle. This routine has been stored in local ROM (program memory) and consists of the following steps:

1) The microcontroller gives a CLR pulse, so the contents of the registers in all the serial-to-parallel converters is cleared.

2) The microcontroller makes the TF and SD line a logical '0', so all the connections between sensor interfaces and common bus are disabled.

3) The microcontroller serially sends the measuring address of the first sensor over the TXD line. This address is read in and converted in parallel form by all the serial-to-parallel converters on both sensor module and VLSI module.

4) The microcontroller makes the SD line a logical '1'. Because the SD line is used as an enable signal in the address serial-to-parallel converters, these two converters will provide the parallel data at their outputs. The address is read in by the addressdecoders on both modules, and one of the decoders selects a sensor (according to the sended address A1 to A32). When a sensor is selected, the sigma-delta converter of the corresponding module is also connected to the f_{in} line.

5) As soon as a sensor is selected, it makes the SD line a logical '0'. In that way the address converters are disabled and can not read in new data. Therefore, the concerning sensor will remain selected.

6) When the microcontroller detects the logical '0' on the SD line, it starts counting the frequency of the bitstream coming from the connected sigma-delta converter. In this way, the output signal of the selected sensor is converted into fully digital code.

7) The microcontroller stacks the 8-bit digital code, representing the measured value of the sensor, into its local RAM.

8) The steps 1 to 7 are repeated for each sensor, until all the sensors (on both sensor module and VLSI module) have been polled. At the end of a complete measurement cycle, 13 bytes of measurement data have been obtained and stacked into local RAM (nine temperature sensors, three pressure sensors and one differential ISFET configuration). These 13 bytes will automatically be sended to the host computer, where they are stored and processed further.

Initialization cycle:

An initialization cycle has to be performed each time the power supply of the BARMINT microsystem is switched on. The microcontroller has to start automatically a service routine that is stored in its program memory (ROM) and consists of the following steps:

1) The microcontroller requests the host computer to transmit the initialization data of all the sensor interfaces. This concerns an array of 18 bytes (nine temperature sensors, two reference sources, one differential ISFET configuration and six latches in the pressure sensor interface), that has been stored in the memory of the host computer when calibrating the sensors.

2) The host computer will serially send this array of 18 bytes to the microcontroller, that reads in this data, converts it into parallel 8-bit words and stacks it into its local RAM.

3) The microcontroller gives a CLR pulse on the common bus, so the contents of the registers in all the serial-to-parallel converters is cleared.

4) The microcontroller makes the TF and SD line a logical '0', so all the connections between sensor interfaces and common bus are disabled.

5) The microcontroller serially sends the initialization address of the first sensor over the TXD line. This address is read in and converted in parallel form by all the serial-to-parallel converters on both sensor module and VLSI module. We stress here that a sensor interface has at least two addresses; one to select the sensor for measurements and one to initialize its interface (transfer of initialization data to the memory latch).

6) The microcontroller makes the SD line a logical '1'. Because the SD line is used as an enable signal in the address serial-to-parallel converters, these two converters will now provide the parallel data at their outputs. The address is read in by the addressdecoders on both modules, and one of the decoders selects the latch of a sensor interface (according to the address A1 to A32).

7) As soon as a sensor latch is selected, the microcontroller makes the SD line a logical '0'. In that way the address converters are disabled and can not read in new data. Therefore, the concerning latch will remain selected.

8) The microcontroller pulls the first byte of initialization data from its local RAM and sends it serially over the TXD line. This data is bound for the sensor interface that has been addressed in step 6. As the address serial-to-parallel decoders have been disabled in step 7, the serially sended data is only read in by the data serial-to-parallel decoders on both VLSI and sensor module. Both decoders convert the received data into 8-bit parallel form and put it on the 8-bit data bus.

9) The microcontroller sends a pulse over the TF line, which enables only the latch of the selected sensor interface to read in the parallel data on the data bus. At that moment, the first sensor of the microsystem has been initialized.

10) The steps 3 to 9 are repeated for each sensor interface, until the latches of all interfaces have read in their data (for example six times for the pressure sensor interface). When the initialization cycle is completed for each sensor interface, the measurements can be started.

4.3.4.2. Communication with the actuators

The actuator control configuration of the BARMINT microsystem will not be complicated, as there is only one thermopneumatic micropump. In the system level concept it has been proposed to provide the micropump with an own address decoder. Although this is not impossible, but a more efficient solution is presented in this paragraph. In figure 4.3.4.1.1, it can be seen that one output of the address-decoder on the sensor module has been reserved for the micropump. The micropump should therefore be enabled and disabled by just sending its address over the TXD line. We propose to change the micropump control configuration of figure 4.2.2.5.1 into the configuration presented in figure 4.3.4.2.1.

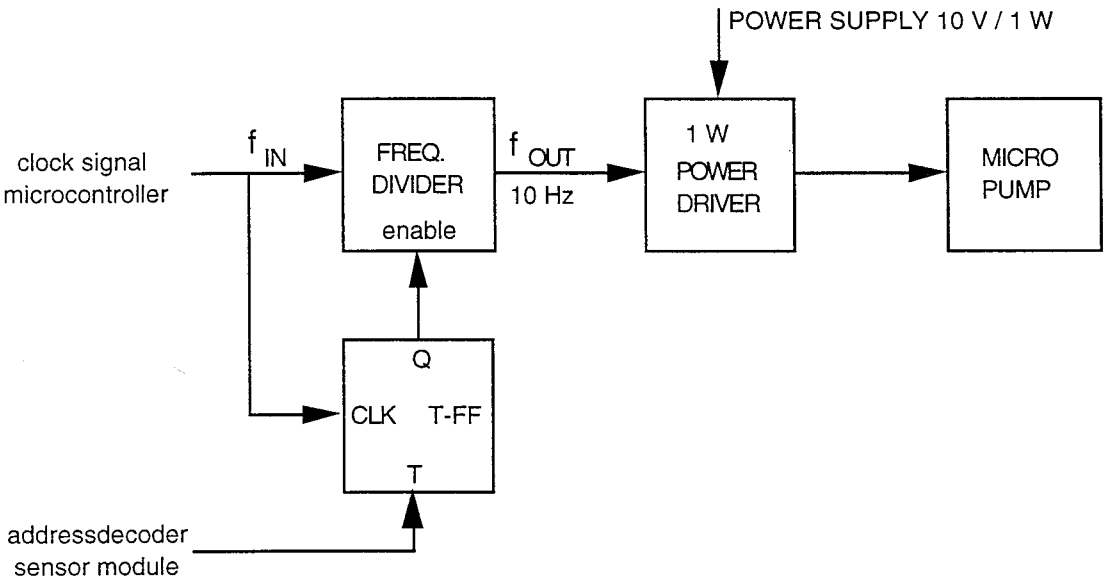

Fig. 4.3.4.2.1. Optimized control configuration for the BARMINT micropump

The 10 Hz square wave that is necessary for driving the micropump can be derived from the clock signal of the microcontroller, by means of a standard digital frequency divider. The factor of division can be determined when the operating frequency of the microcontroller has been defined.

The frequency divider in figure 4.3.4.2.1 will only generate an output signal, when its enable input is made a logical '1'. In this configuration has been chosen to control this enable input by a T-flipflop. When giving a short pulse at the T-input of this flipflop, its output Q will become a logical '1'. The output Q remains '1' until a next pulse is given at the T-input. Then it will return to '0'. This cycle is repeated each time when a new pulse is given.

The pulse at the T-input has to be generated by the microcontroller of the BARMINT microsystem. When the micropump has to be activated, the microcontroller sends the address of the pump to the address decoder on the sensor module. The address decoder makes its 'upump' output (which is connected to the T-input of the flipflop) a logical '1', so the output Q of the T-flipflop is also made a logical '1'. Directly afterwards, the microcontroller clears the addressdecoder (so the T-input returns to '0'), and starts sensor measurements or goes back into the power-down mode. But the micropump remains activated, because of the memory function of the T-flipflop. It can be stopped by sending another time its address to the address decoder. This generates a second pulse at the input of the T-flipflop, which will disable the micropump.

4.3.4.3. Communication with the external host computer

The BARMINT microsystem needs bidirectional serial communication between its on-board microcontroller and the external host computer. This can be arranged by using the serial I/O port of the microcontroller. By this port, consisting of a TXD and an RXD line, data can be transmitted and received using a protocol with start and stop bits. As this serial I/O port is already used for communication with the sensors of the microsystem, the host computer needs to have a unique address. The bidirectional connection with the external host computer is schematically represented in figure 4.3.4.3.1.

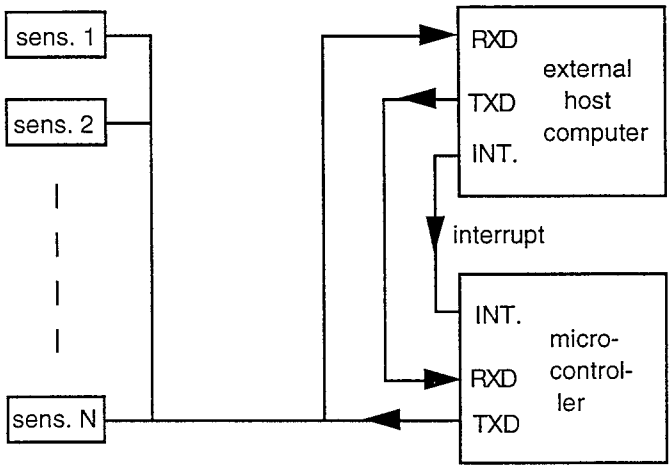

Fig. 4.3.4.3.1. Bidirectional communication with external host computer

Beside the normal data communication lines TXD and RXD, additional interrupt lines could also be desirable to wake up the microcontroller or to request a measurement cycle. The details of the communication with the host computer will not be discussed in this report, as they strongly depend on the type of microcontroller and computer that will be used.

4.3.4.4. The serial-to-parallel converters

In this paragraph will be shown how the serial-to-parallel converters can be realized, that are necessary on both sensor module and VLSI module. The serial-to-parallel converter presented in this paragraph is based on a digital shift register and can be used for the conversion of serial input data to 8-bit parallel words. It is assumed that the serial input data consists of 10-bit packets: a start bit, the 8-bit serial data and a stop bit. The schematic of the converter is given in figure 4.3.4.4.1, and will be discussed with the aid of the signal diagram of figure 4.3.4.4.2.

When there is no data, the 'serial in' line is assumed to be at a logical '1' level. The start bit is then represented by the first 1-to-0 transition on this line. As soon as the 'serial in' line becomes '0', the flipflop FF1 is set (on the active edge of the clock signal CLK), so its output Q becomes '1'. Because of AND gate P1, the output Q can no longer be influenced by the following bits on the 'serial in' input, so Q remains '1'. This enables the counter, so it starts counting the number of positive clock transitions. Each time that the clock has a 0-to-1 transition, one bit of serial data is shifted into the 8-bit shiftregister, so after 8 clock transitions this process has to be stopped. This is done with the counter output b3 and AND gate P2; when the counter reaches the value 8, its output b3 becomes '1', which clears the output Q of flipflop FF1. By means of AND gate P2, the clock signal is disabled and the shift register stops shifting in new data. At the outputs b0 to b7 the 8-bit parallel data is now available.

In figure 4.3.4.1.1 and 4.3.4.1.2, it can be seen that the two address serial-to-parallel converters are also equipped with an additional SD input. The data read in by these converters can only be transferred to the output when SD is made a logical '1'. Therefore, in these two serial-to-parallel converters an 8-bit output latch should be added, that is enabled by the signal SD. This version of the serial-to-parallel converter is presented in figure 4.3.4.4.3.

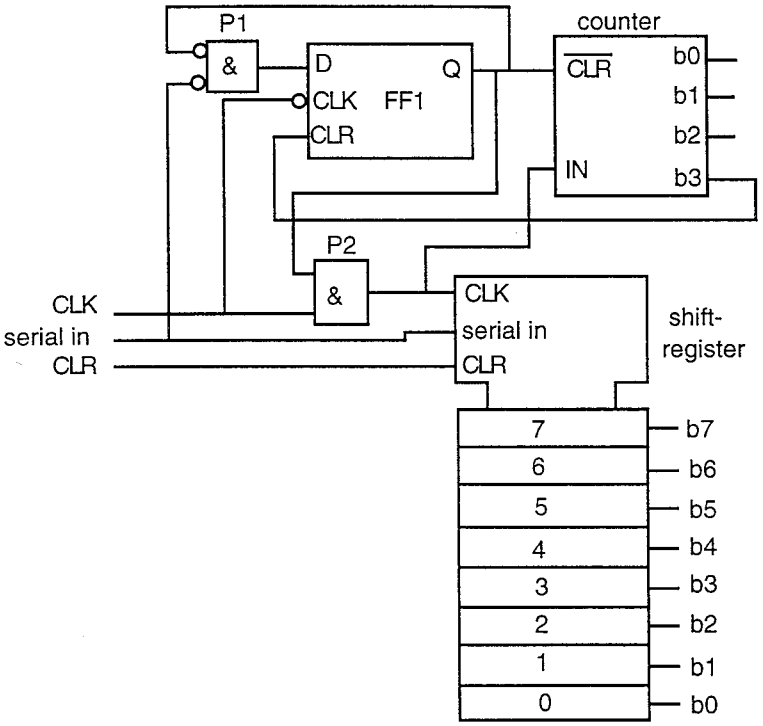

Fig.4.3.4.4.1. Schematic of the serial-to-parallel converter

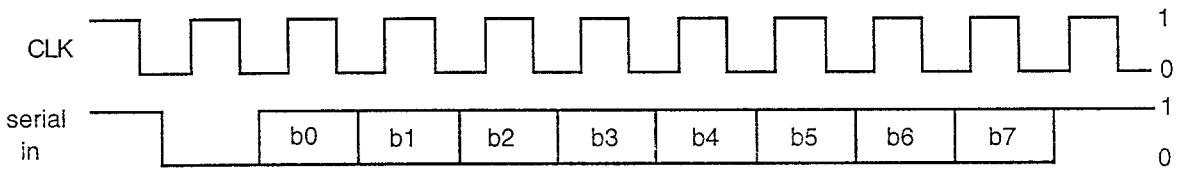

Fig.4.3.4.4.2. Input signals for the serial-to-parallel converter

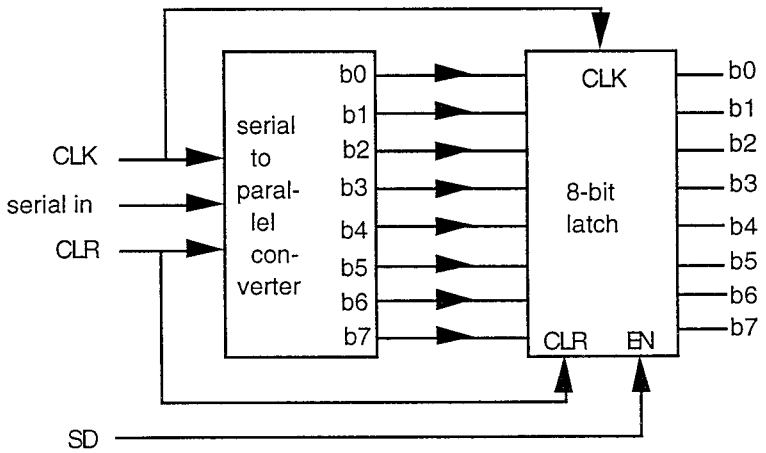

Fig. 4.3.4.4.3. Address serial-to-parallel converters for the BARMINT microsystem

4.3.4.5. The address decoder

On both sensor module and VLSI module an address decoder is located for addressing the sensor interfaces for measuring or initialization purposes. The input signal of the address decoder is a 6-bit digital word, that provides $2^6 = 64$ selection possibilities. When regarding the figures 4.3.4.1.1 and

4.3.4.1.2, it can be concluded that only 32 different addresses are used by the sensor interfaces on both modules. The addresses A1 to A15 are used for the sensors on the sensor module and the addresses A16 to A32 for the sensors on the VLSI module. The address A0, belonging to the input word 000000, can not be used for selection facilities. The complete relation between input address and selected sensor interface is given in table 4.3.4.5.1.

b5...b0	address	selected device	
000000	A0	not connected	
000001	A1	reference source (init.)	
000010	A2	temp. sensor (init.)	
			SENSOR MODULE
001111	A15	micropump	
010000	A16	reference source (init.)	
010001	A17	temp. source 1 (init.)	
			VLSI MODULE
011111	A31	temp. source 8 (init.)	
100000	A32	temp. source 8 (meas.)	

Table 4.3.4.5.1. Selection table of the BARMINT address decoder

This relation between input address and selected output of the address decoder can easily be obtained with combinational logic. The principle of the address-decoder is given in figure 4.3.4.5.1.

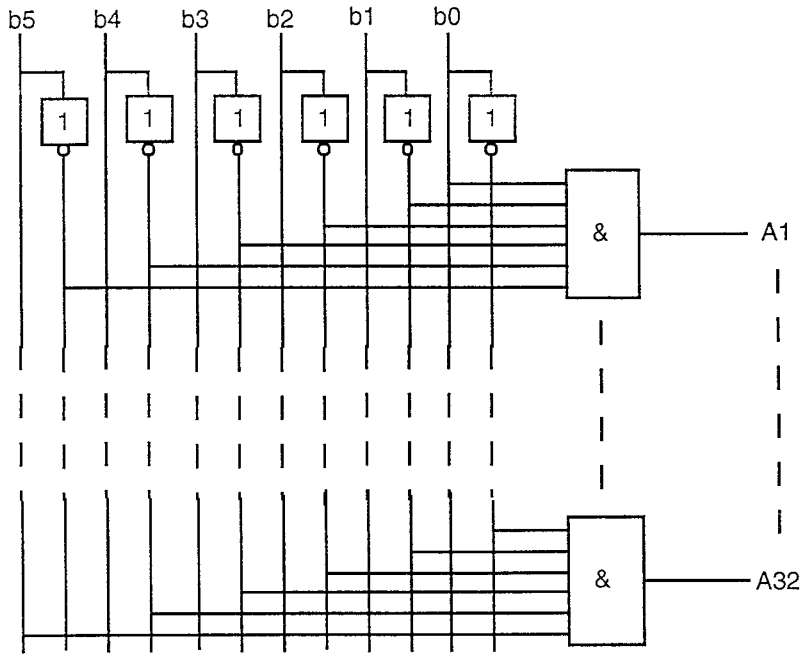

Fig. 4.3.4.5.1. Principle of the address decoder for the BARMINT microsystem.

As the addresses A1 to A15 are used on the sensor module and the addresses A16 to A32 on the VLSI module, the address decoder as given in figure 4.3.4.5.1 has to be divided into two parts. So the control signals b0 to b5 (and their inverse signals) have to be generated separately on each module.

4.4. Conclusion

In this chapter , we detailed the global architecture of the BARMINT microsystem that has been established within this thesis. The motivation of the choices and the solutions adopted in this system is explained in detail. The interest of this architecture is the fact that it could be generic and adapted easily in order to be used for a complex microsystem which includes many sensing and actuating functions. However, it should be noticed that the proposed solution answer to the specification and particularly to the constraints fixed within the BARMINT project.

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CHAPTER 5

CONCLUSION

Avant la fermeture de nos travaux, un bilan peut être présenté afin de synthétiser les avancées proposées dans le domaine et de dégager de nouveaux axes de recherche.

Cette thèse a porté sur trois axes complémentaires dans le but de fournir un accès plus aisé aux microsystèmes. Ces axes sont les suivants :

- les techniques de fabrication compatible avec la microélectronique afin de tirer profit des investissements massifs effectués sur cette dernière et donc pouvoir donner accès à une technologie de microsystèmes à bas coût,
- les outils de CAO pour les microsystèmes permettant la simulation et la conception de microsystèmes sans une grande complexité,
- une architecture générique pouvant être appliquée à des microsystèmes complexes comportant des capteurs, actionneurs, des modules de communication et de contrôle.

Ces travaux ont permis à développer et valider deux technologies compatible avec la microélectronique utilisant deux matériaux différents : le silicium et l'arséniure de gallium. La phase de "process" est réalisée sur des lignes de production industrielles suivie par une phase de "post-process" dont le but est de suspendre les structures sans endommager l'électronique intégrée. Ces deux technologies sont :

- 1.0µ CMOS microusiné en volume face-avant,
- 0.6µ MESFET microusiné en volume face-avant.

La première technologie est aujourd'hui disponible à travers le CMP, service de fabrication hébergé par le Laboratoire TIMA, et la première tranche (run) multi-projets a eu lieu le 19 février 1996 qui comportait 10 projets provenant de 8 participants du monde. L'annexe 5A donne les vues "layout" de ces différents projets distribués sur la tranche.

La seconde technologie va être disponible à travers ce même service courant 1996.

En terme de CAO, le kit de conception développé au cours de cette thèse a été installé avec succès dans une centaine de centres au monde permettant aux concepteurs venant de ces centres de concevoir des microsystèmes selon la technologie supportée (1.0µ CMOS microusiné en volume face-avant) sans complexité et en un délai très court. Ce kit constitue le support CAO pour le service de fabrication de microsystèmes offert par CMP. C'est le premier kit de conception disponible aujourd'hui au monde.

Par ailleurs, le simulateur de gravure 2D est actuellement couplé à ce kit et permet de prédire le temps de gravure nécessaire à suspendre les structures intégrés dans les microsystèmes.

En plus, la structure globale de l'environnement de CAO représente la seule architecture européenne d'outil CAO pour les microsystèmes en opposition avec la structure américaine proposée par le MIT.

Finalement, l'architecture générique proposée dans le chapitre 4 de cette thèse est en cours d'implémentation et de fabrication dans le cadre du projet européen BARMINT regroupant 10 laboratoires européens.

D'autres études et thèses sont émis dans le laboratoire TIMA portant sur l'aspect technologie et outils

de CAO. Elles visent d'accroître le portefeuille technologique au CMP en fournissant aux concepteurs de microsystèmes dans le monde la possibilité de fabriquer leur système, au niveau prototypage et bas volume, à des bas coût. Des travaux portent sur d'autres process CMOS et d'autres technologies compatible avec le CMOS, telles que le microusinage en surface, ainsi que sur le microusinage de la technologie HEMT (AsGa) permettant d'avoir des fonctions opto-mécaniques.

D'autre part, de nouveaux kits de conception sont en cours de développement basés sur d'autres outils de conception de CIs, tels que l'environnement MENTOR GRAPHICS. Il est évident que le kit de conception développé au cours de cette thèse sera entretenu par le Service CMP qui assurera la maintenance et le développement des nouvelles versions.

Le simulateur de gravure 2D sera étendu à un simulateur 3D permettant ainsi de coller avec l'objectif de ce simulateur détaillé par cette thèse le décrivant comme une transformation 2D-3D permettant de passer d'une description "layout" (GDSII) à une description interprétable par un simulateur FEM. Cette transformation permettra de coupler les deux flux de conception système et composant décrit dans le chapitre 3 de cette étude.

Le développement de l'environnement entier sera achevé avec ces études émises à partir de cette thèse.

Annexe 5A - Première tranche multi-projets microsystèmes au CMP