Architectures de convertisseurs DC/DC à fort courant, basse tension avec commande numérique

Adan Simon Muela

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JURY

Prof.Eric MONMASSON (rapporteur)
Prof. Miro MILANOVIC (rapporteur)
Dr. Javier CALVENTE (rapporteur)
Prof. Sigmond SINGER (examinateur)
Prof. Alexandre NKETSA (examinateur)

Ecole doctorale : *GEET*
Unité de recherche : *LAAS-CNRS*
Directeur(s) de Thèse : *Prof. Corinne ALONSO (directrice), Dr. Vincent BOITIER (co-directeur) et M. Jean-Louis Chaptal (co-directeur)*

AUTEUR: Adán SIMON-MUELA

TITRE: Architectures de Convertisseurs DC/DC à fort courant, basse tension avec commande numérique

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RESUME:

La consommation de puissance des microprocesseurs embarqués ne cesse d'augmenter avec la multiplication des fonctions qu'ils doivent assurer Ainsi, les générations actuelles de microprocesseurs ont une forte consommation en courant sous une très faible tension (autour du volt) avec des transitoires contraignants.

Cette thèse est consacrée à la design des systèmes d'alimentation rapprochées des cartes mères des PC où régulateurs de tension (VRMs) qui englobent fort courant et faible tension de sortie ainsi que haute fréquence de découpage. A cet effet, les architectures entrelacées ou multi-phase sont une bonne alternative pour atteindre ces niveaux énergétiques si rigoureux.

Traditionnellement, ces types de systèmes d'alimentation sont contrôlés avec une commande analogique. Cependant, les nouvelles générations de microprocesseurs exigent des performances plus élevées en même temps qu'une régulation plus précise. Alors, la commande classique analogique est de plus en plus remplacée par une commande numérique plus flexible et plus performante.

Cette thèse s'intègre dans le cadre du projet régional LISPA où le LAAS et Freescale Semiconductor collaborent pour développer de nouveaux systèmes d'alimentations pour microprocesseurs de puissance.

MOTS-CLES: PoL, VR, multiphase, mode entrelacé, commande numérique, FPGA, DSC

DISCIPLINE ADMINISTRATIVE: Génie Electrique

ADRESSE DU LABORATOIRE: 7, Av. Colonel Roche, 31077, Toulouse, France

AUTHOR: Adán SIMÓN-MUELA

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ABSTRACT:

The power consumption of embedded microprocessors has increased significantly due to the considerable number of new functions which they should manage. Thus, current generation of microprocessors needs considerable supply currents with very low voltages.

The aim of this dissertation is to study these supply modules and their association to increase the current supply levels delivered to the charge. These power supply systems are oriented to embedded microprocessors like those can be found inside PC motherboards..

Traditionally, this kind of power supplies owns analogue control. However, new microprocessor generation demands faster performances and more accurate and tight regulations. Thus, the present trend is to replace the classical analogue control by a digital control system more flexible and performing likewise.

Then, this dissertation takes part in the LISPA regional project where the LAAS and Freescale Semiconductor collaborate to develop new power supply systems for embedded power microprocessors.

KEYWORDS: PoL, VR, multiphase, interleaving mode, digital control, FPGA, DSC

DISCIPLINE ADMINISTRATIVE: Electric Engineering

ADRESSE DU LABORATOIRE: 7th, Colonel Roche Av, 31077, Toulouse, France

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TABLE OF CONTENTS

TABLE OF ILLUSTRATIONS

ACRONYMS LIST

ACR: AC Resistance

ACS: Active Current-Sharing

ACMC: Average Current-Mode Control

ADC: Analogue-to-Digital Converter

ASIC: Application Specific Integrated Circuit

AT: Advanced Technology

ATX: Advanced Technology eXtended

AVP: Adaptive Voltage Positioning

CCM: Continuous Current Mode

CMC: Current-Mode Control

CMOS: Complementary Metal-Oxide Semiconductor

CPC: Current-Programmed Control

CPU: Central Process Unit

CS: Current-Sharing

DAC: Digital-to-Analogue Converter

DCM: Discontinuous Current Mode

DCMC : Digital Current-Mode Control

DCR: DC Resistance

DPCMC: Digital Peak Current-Mode Control

DPS: Distributed Power Supply

DPWM: Digital Pulse Width Modulator

DSC: Digital Signal Controller

DSP: Digital Signal Processor

DVMC: Digital Voltage-Mode Control

DCS: Democratic active Current Sharing

EMI: ElectroMagnetic Interference

ESL: Equivalent Series Inductance

ESR: Equivalent Series Resistance

FF: Feedforward

FoM: Figure of Merit

FPGA : Field Programmable Gate Array

HDL: Hardware Description Language

HSM: High Side MOS

IC: Integrated Circuit

IMC: Internal Mode Control

IVFF: Input-Voltage Feedforward

LDO: Low DropOut

LAAS-CNRS: Laboratoire d'Analyses et Architecture des Systèmes – Centre National de

Recherche Scientifique

LISPA: Laboratoire pour l'Intégration des Systèmes de Puissance Avancés

LFM: Linear Feet per Minute

LPX : Low Profile eXtended

LSB: Less Significant Byte

LSM: Low Side MOS

LUT: Look-Up-Table

MLCC: MultiLayer Ceramic

MOS: Metal Oxide Semiconductor

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

MS: Master–Slave

NLX: New Low profile eXtended

OCFF: Output-Current Feedforward

OCPC: One-Cycle Predictive Current

PCMC: Peak Current-Mode Control

PFC: Power Factor Correction

PFM: Pulse Frequency Modulator

PI: Proportional Integral

PIC: Programmable Interrupt Controller

PID: Proportional Integral Derivative

PIN: Positive- Intrinsic-Negative

PLD: Programmable Logic Device

PoL: Point-of-Load

PTC: Positive Temperature Coefficient

PWM: Pulse Width Modulator

RAM: Random Access Memory

ROM: Read Only Memory

SAC: Analogue-Controlled System

SDC: Systems with Digital Control

µc: microcontroller

µp: microprocessor

VD: Voltage-Droop

VHDL: Very High-level Design Language

VID: Voltage IDentification

VMC: Voltage-Mode Controlled

VR: Voltage Regulator

VRD: Voltage Regulator Down

VRM: Voltage Regulator Module

WTX: Workstation Technology eXtended

ZOH: Zero Order Hold

Chapter 1

INTRODUCTION

1. INTRODUCTION

Embedded applications have emerged notably during the past few years. Actually, more and more people carry on nomad and traveler lifestyles being the cause of a considerable increase and development of portable and autonomous systems. As a consequence, energy sources, their corresponding storage devices and power management control systems should be improved substantially to obtain optimal and long-duration working modes. In view of that, new issues in the quest for a longer autonomy in embedded systems have appeared recently.

Furthermore, embedded products own strict power supplies design requirements which are becoming more and more critical with the increasing complexity of the functionalities proposed by these new portable devices.

As a matter of fact, some parameters like weight, size, robustness and cost should be taken into account to achieve efficient embedded systems. As a result, manufacturers need more compact, flexible, efficient and cheaper power supplies modules for their embedded applications.

In this context, power management discipline is becoming more and more important for the design and manufacture of embedded systems in the automotive, consumer and other industrial markets. Hence, our principal objective along the three years of this dissertation has been the study of more compact power supplies dedicated to high-current and low-voltage loads. Therefore, our aim is to introduce optimized power supply architectures and their corresponding control systems dedicated to embedded microprocessors. In view of that, a meticulous design methodology of this kind of power supply modules and their control systems has been completed in order to assure adequate robustness and fast system responses as well as enhanced efficiencies for a wide range of loads. In particular, the core of this dissertation is the study of several digital control laws which can be used in new Voltage Regulators (VR) topologies working at high switching frequencies.

Thereby and to evaluate recent advances in this sort of applications, a state-of-the-art of main power conversion architectures used in embedded systems has been developed as well as their corresponding evolutions. In response to this later report, our interest is focused on Point-of-Load (PoL) and VR architectures since

they present innovative power supply features. Nevertheless, these new topologies demand important developments to respond to future power supply requirements imposed by microprocessor manufacturers. At present, digitally-controlled multiphase power converters seems a suitable candidate for this sort of embedded power supplies. Indeed, they solve major problems of efficiency for high-current and high-frequency power supply requirements. On the other hand, digital control allows designers significant benefits due to their flexibility and their numerous possibilities of design as it is illustrated along this dissertation in different examples.

As a result, to face these new challenges in the power management field, our work takes part in the LISPA (Laboratoire pour l'Intégration des Systèmes de Puissance Avancés) project where the LAAS-CNRS and Freescale Semiconductor are associated in this new French regional (Midi-Pyrenean) collaboration. In this context, new solutions for PoL and VR applications are developed in such a way that understand better the problems and limitations of this kind of power supply architectures oriented to embedded power microprocessors.

Therefore, this dissertation has been divided in five main chapters. Thus, the second chapter introduces to the reader the work context of this dissertation and the state-of-the-art of Distributed Power Supply architectures. Then, different possibilities for digital controllers dedicated to manage power converters and their main design trade-offs are listed at the end of this chapter. Moreover, a short chronological evolution of digitally-controlled power converters is disclosed in this part.

Next, a theoretical analysis of the power stage is developed in the third chapter. Here, some technological challenges are treated in order to optimize the efficiency and the robustness of a high-current, low-voltage and high-frequency multiphase interleaved DC/DC converter.

The fourth chapter is focused on the theoretical study of the digital control laws dedicated to VRs. Thus, main control laws used in this field are modeled and adapted for this kind of applications. In addition, some guidelines are given for a correct design of a digitally-controlled DC/DC converter. Furthermore, these control laws have been illustrated in several examples in order to validate our digital control design methodology.

Our last chapter groups the studies disclosed in the previous sections. Therefore, some experimental prototypes developed during these three years are presented in this part. First practical design is based on a Single-Phase Synchronous Buck power converter controlled by a Digital Signal Controller. After, the digital controller has been replaced by a FPGA obtaining our second experimental prototype. The new digital controller allows us to beat the frequency constraints imposed by our previous experimental prototype. Finally, the Single-Phase power stage has been replaced by a multiphase architecture in our third experimental example to obtain an experimental validation of our systems at high currents. In this later prototype, a Current-Sharing control loop has been added in order to complete a full digitally-controlled multiphase DC/DC power converter. This last work will be presented in a near future and it is not included currently in this manuscript.

Chapter 2

Distributed Power Supply Architectures For Embedded Microprocessors

2. DISTRIBUTED POWER SUPPLY ARCHITECTURES FOR EMBEDDED MICROPROCESSORS

2.1 Introduction

Nowadays, power supply requirements for embedded and autonomous applications are becoming more and more severe. On one hand, the apparition of new portable electronic devices like cell phones, GPS, PDAs or MP4 represents an important challenge in terms of power autonomy. Actually, they have instigated the quest for more efficient power supply systems in order to enlarge the duration of their batteries. On the other hand, embedded processing units require higher amounts of energy due to the increasing number of transistors in this sort of devices. Thus, international standards for embedded power supply applications demand robust and compact modules which must be able to accomplish strict requirements on the conversion, transmission and level adaptation of the electrical energy.

As a result, our efforts have been focused on the study and design of power supply systems for embedded microprocessors. To illustrate and validate our purpose, the power supply system for a typical PC motherboard embedded microprocessor has been chosen as example since it owns very specific power supply requirements. However, an important part of our work is based on the theoretical development of digital control laws covering different power converters. Indeed, these control laws can be applied in a wide range of supply powers and working frequencies: from the watt (for portable applications) up to hundred of watts (telecommunication servers or automotive applications) considering frequencies over the MHz. To know exactly how a digitally-controlled power converter can be obtained, the specific parts involving this sort of systems have been investigated as wells as the different control techniques to manage properly these applications in order to find future optimal answers for current technological challenges.

Therefore, the first part of this chapter introduces the work context of this dissertation with a brief state-of-the-art of Distributed Power Supply architectures. Furthermore, a short introduction of current digital controllers

oriented to this kind of applications as well as the chronological evolution of digitally-controlled power converters is disclosed along this section.

2.2 Evolution of power supply architectures for embedded microprocessors

2.2.1 Work principle of Distributed Power Supply architectures

Power conversion chain for an embedded power supply system (from the electrical grid until the load) is composed by several blocks as it can be observed in the simplified schema of Fig. 2-1. The main objective is to complete the global power conversion obtaining minimal losses. In this case a high-efficiency AC/DC converter block is found in first place. Next, a dedicated DC/DC converter which adapts power levels according to the desired supply requirements of each load.

This later block, specially conceived to supply embedded microprocessors, is known as Voltage Regulator (VR). Hence, a VR is a high-efficiency power converter which can deliver the most advantageous power level depending on the conditions required by the load (in steady and also during transient states). Consequently, VRs allow a tight and fast regulation of their output variables.

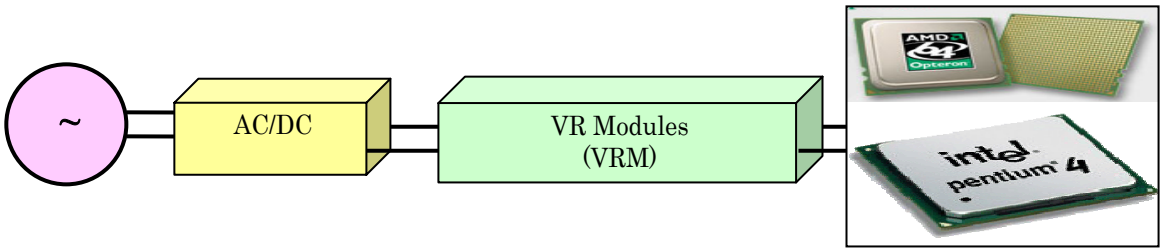


Fig. 2-1 Typical embedded microprocessors power supply chain

VRs can be divided into two main groups named VRM (Modules) and VRD (Down). The main difference between VRMs and VRDs is those later are not integrated in the motherboard design. an example of a commercial motherboard including a built-in VRM for an Intel LGA775 [2.1] socket microprocessor can be observed in Fig. 2-2.

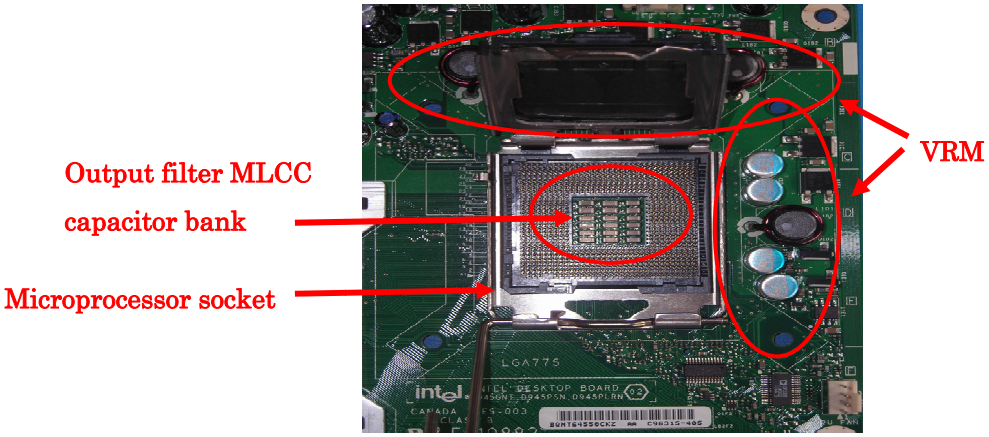


Fig. 2-2 Built-in VRM for an Intel LGA775 socket

In commercial applications, VRs serve as supply module for a wide range of embedded products. As an example, current PDAs or cell phones need supply current levels around 1A. In contrast, typical desktop or server PCs require supply current levels higher than 100A as it is illustrated in Fig. 2-3.

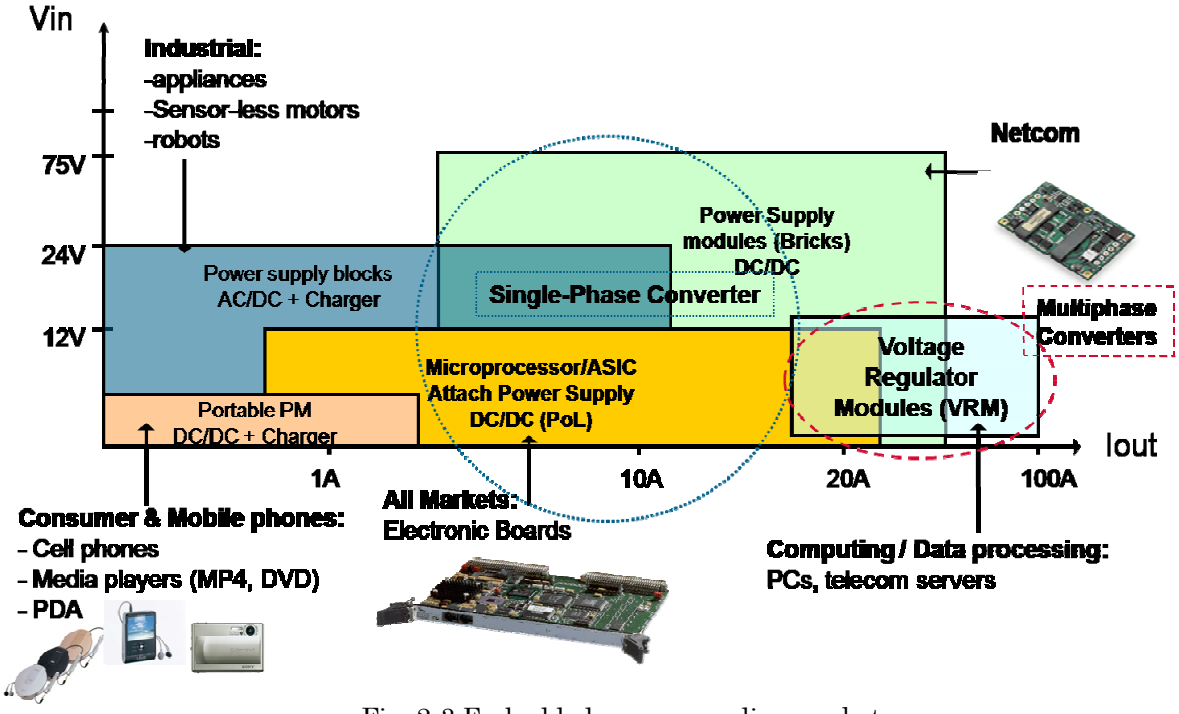


Fig. 2-3 Embedded power supplies market

Our main objective is the analysis and design of high-current VR architectures which can be used as power supply modules for desktop PC microprocessors. This family of products represents a new challenge for Freescale Semiconductor.

At present times, the endless technological evolution of this kind of power supplies motivates that main microprocessors manufacturers like Intel or AMD compete for integrate more and more transistors in a lower silicon surface.

Furthermore, new built-in transistors should work at higher switching frequencies to boost the microprocessor power calculation. However, the increasing trend of the number of transistors as long as the computers progress was predicted already by Gordon E. Moore in 1965. Thus, the Moore's law (see Fig. 2-4) enunciates that the number of transistors per inch in a processor is duplicated each 2 years in order to reply their continuous progress [2.2] . As a result, the microprocessor power supply demands are constantly increasing.

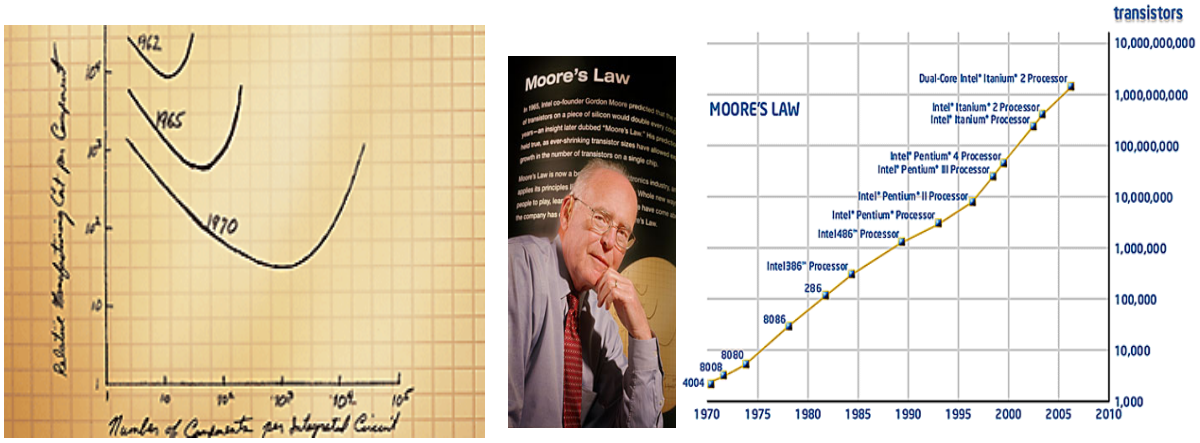
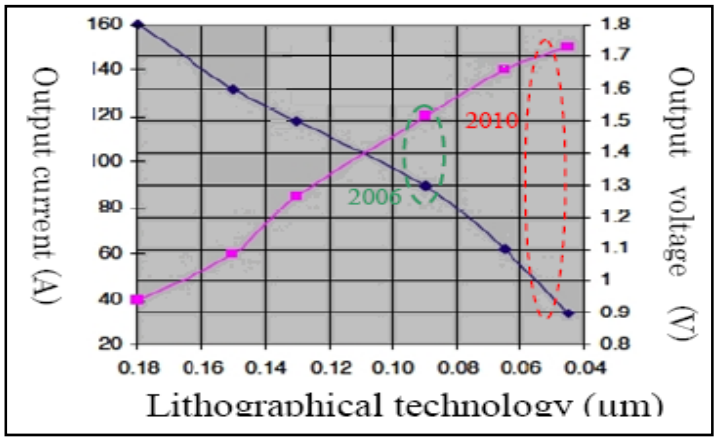


Fig. 2-4 Original Moore's law (left), Gordon E. Moore (center), and current law (right)

In particular, the evolution of present lithographical process requires supply voltages around 1V. In consequence, the foremost trend is to reduce the supply voltage level delivered to the microprocessor to limit the electrical field inside the silicon chip. Actually, as long the lithographical process values are decreased, the voltage supply levels delivered to the IC should be reduced correspondingly.

Anyway, this value will be decreased in the near future as it can be seen in Fig. 2-5. However, this droop in the supply voltage levels is not costless. As a matter of fact, the evident consequence is that supply current levels must be increased in order to deliver to the load a constant supply power [2.3] .



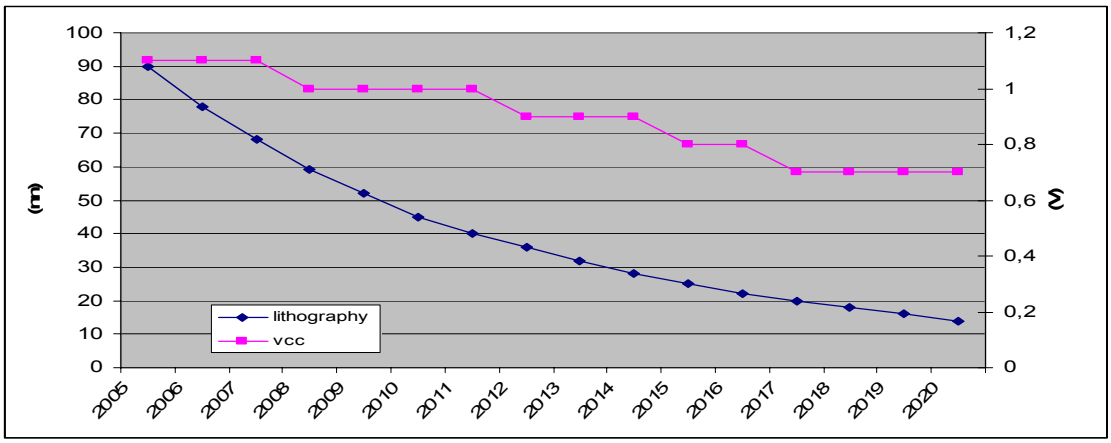


Fig. 2-5 Microprocessors supply power trend

Considering previous supply power requirements, current desktop computers require high efficiency, high power density, high reliability and fast transient responses In the past, a typical power supply system was constituted by a single module adapting AC levels into a large range of DC values (see Fig. 2-6 a).

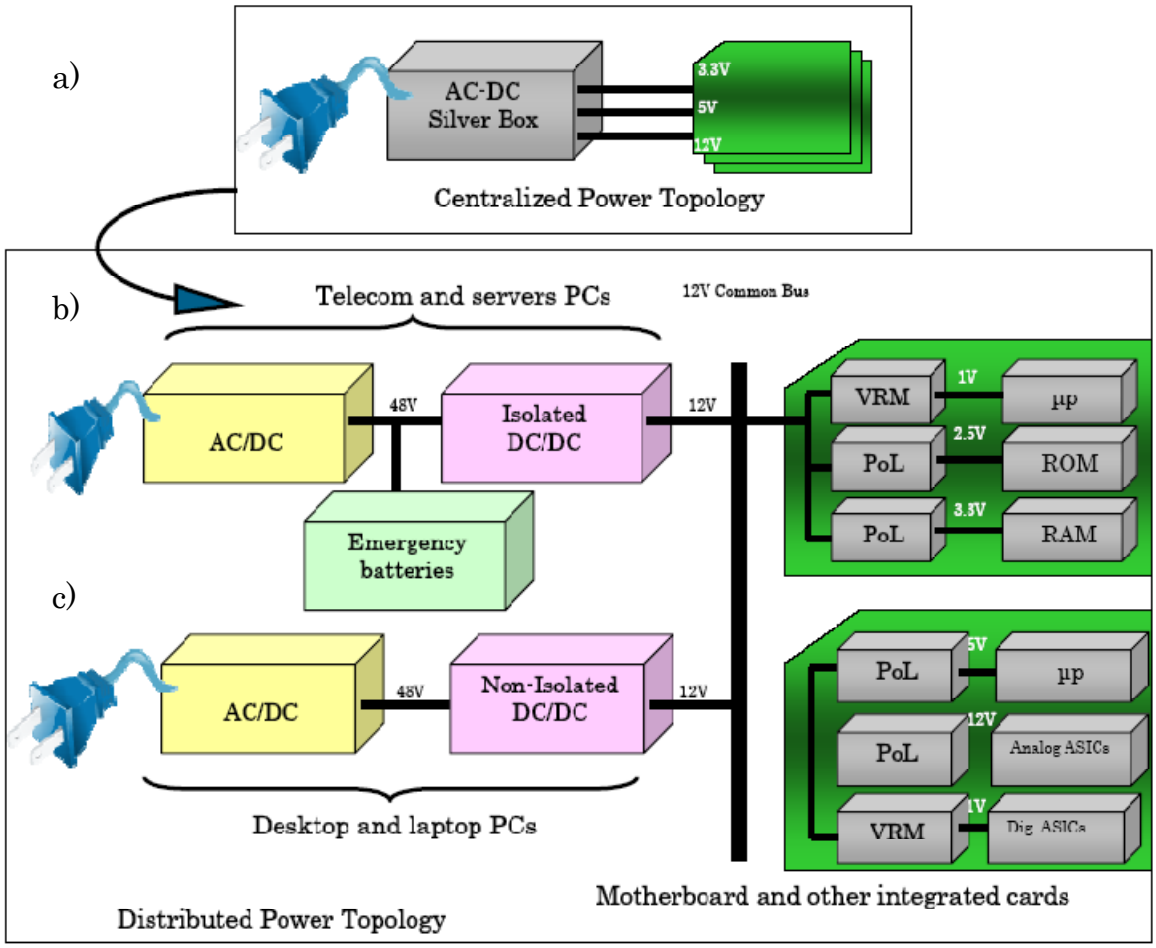


Fig. 2-6 Power Supply architectures for PC motherboard: a) centralized, b) distributed topology for telecom and server PCs, c) distributed topology to desktop and laptop PC

This single module was called 'Silver Box' due to its sheet-metal enclosure. It presented a high consumption due to the large supply power range which should deliver to the different loads of the embedded system. In essence, the efficiency of the conversion block was reduced significantly because of the inductive and resistive parasitic effects produced by the connections between the Silver Box and the microprocessor. Furthermore, the Silver Box was not able to deliver the most convenient supply levels for each load. This was due to its single AC/DC conversion structure which was neither flexible nor well-adapted for several load requirements.

Thereby, classical centralized power supplies were replaced for more efficient Distributed Power Supply architectures (see Fig 2-6 b and c). Indeed, Distributed Power Supply topologies offer important advantages in terms of efficiency, power density and power matching. As a result, losses are appreciably reduced as well as thermal effects. Thus, these power supply structures are constituted by several conversion blocks.

As it can be observed in Fig. 2-6, two conversion principles can be choosen to assure appropriate power levels in the embedded microprocessors supply chain. Therefore, it can be selected either one schema or the other depending on our technical requirements. First chain presented in Fig. 2-6b is found often in networks and telecommunication applications where supply power is important.

In these cases, AC signals (115VAC or 230VAC) are transformed initially into high DC levels by means of an independent bulk AC/DC converter. In spite of 48V is the typical DC value, the telecom range works properly in the 36-75V range. Anyway, the European standards reduce the maximal value to 60V. After the AC/DC conversion, an isolated DC-DC step-down converter transforms the 48V to lower DC levels (typically 12V). These intermediate DC levels are transmitted to a common bus. Typically, isolation is needed to protect the system from dangerous spikes and to prevent ground-loops as well.

On the other hand, typical supplies for desktop or laptop computers are presented in the previous schema (see Fig. 2-6 c). In most of cases, the isolation stage is not necessary. Moreover, for embedded applications, the suppression of this protection implies a reduction of the weight and cost. After, a second non-isolated DC/DC converter completes the voltage level adaptation to the desired

one by the common bus (12V typically) optimizing the global power matching,

Concerning the AC/DC stage, it must assure PFC (Power Factor Correction) role associated to an isolation block (typically a transformer, see Fig. 2-7). Hence, the PFC circuit is used to decrease the harmonic content and to accomplish with some standard requirements (e.g. IEC1000-3-2 or EN 61000-2-3).

Previous block is based classically on a Boost converter configuration with variable regulation depending on the converter conduction mode (CCM or DCM). Thus, the primary stage of the transformer is typically composed by a Forward or a Bridge (half or full) topology depending on the expected power requirements. In the secondary stage of the transformer, Schottky diodes or low-voltage MOSFETs switches (in a synchronous regulation) are found typically to complete the AC/DC transformation.

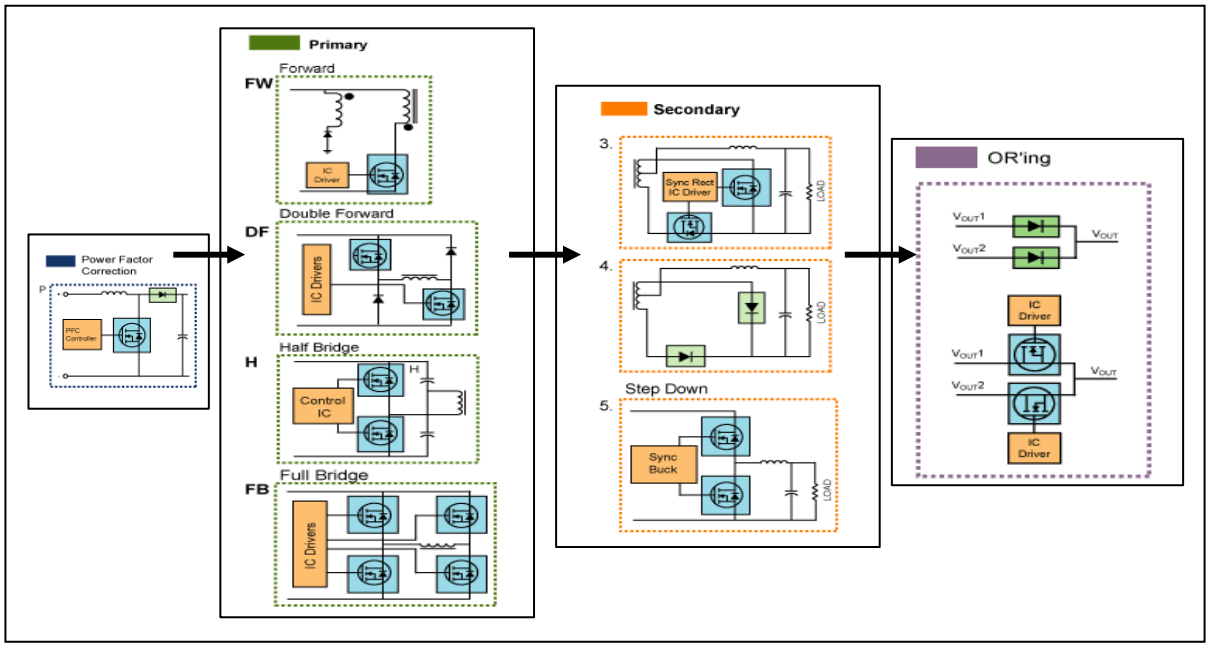


Fig. 2-7 AC/DC Converter architecture.

Some AC/DC systems, which are normally destined to server computers in critical applications, incorporate parallel auxiliary systems to have redundant supply systems in case of failure. These systems are known like “ORing” and they are composed by either Schottky diodes or MOSFET [2.4] . An example of a commercial AC/DC system and its associated technical characteristics is illustrated in Fig. 2-8 [2.5] .

An isolated DC/DC converter is required in telecom and server applications, i.e. like in all applications connected to the electrical grid.

Power Supply Type	AC-DC with PFC		
Power Supply Standard	AT		
AC Input Voltage	115, 230 V		
DC Output Voltage	+5V	+12V	-12V
DC Output Current	14A	4.2A	0.3A
Output Power:	150 W		
Efficiency	65%		
Dimensions	150x81.5x40.5mm		

Fig. 2-8 Commercial AC/DC power supply ACE-815T

This converter does not need a tight output regulation because load requirements are not critical. Forward, Push-Pull and Bridge topologies are the most common choices as it is represented in Fig. 2-9.

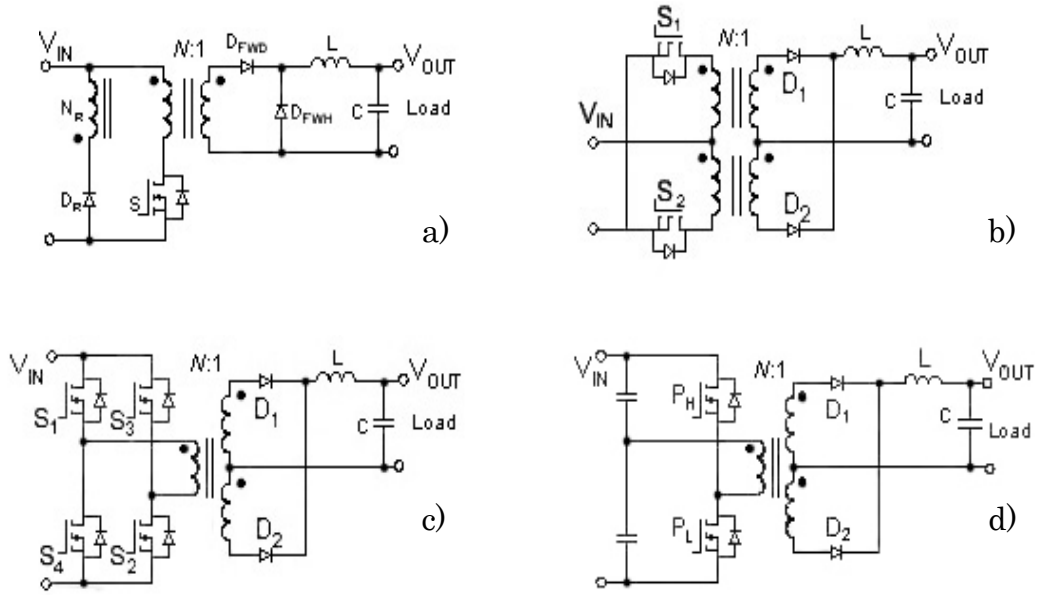


Fig. 2-9. Isolated DC/DC converters: a) Forward, b) Push-pull c) Full-bridge d) Half-bridge

Following the supply chain, the intermediate common bus voltage carries the power levels until different non-isolated switched DC/DC converters known as Point-of-Load (PoL) and/or VR converters. PoL converters are placed as near as possible to their corresponding load completing more efficiently the power transmission and conversion. Moreover, PoLs are used to provide a low and tight regulated DC voltage to the load from the intermediate voltage bus or from the battery. Furthermore, PoLs reduce considerably distribution losses obtaining important benefits like enhanced power matching, high efficiencies and saving space and money as well. Moreover, for applications needing high-powers, PoLs

also can be used in parallel structures offering high current levels without over-sizing active and passive system devices.

Simultaneously, VRs are used to supply the built-in microprocessors of the motherboards following some industrial standards like ATX, FlexATX, microATX, AT, LPX, NLX, and WTX. Each one of these standards corresponds to different power supply requirements [2.6]

By and large, the global efficiency and the power-matching of the system are improved for a wide range of loads thanks to VR and PoL converters. For that matter, these power converter architectures have been chosen to develop new digital control algorithms for our experimental implementations.

2.2.2 Point-of-Load and Voltage Regulator architectures

2.2.2.1 Introduction

Two main conversion principles which give place to two complementary families of commercial products are found in PoL and VRs applications. First family is composed by LDO (Low DropOut) linear regulator and the second one consists of switching converters.

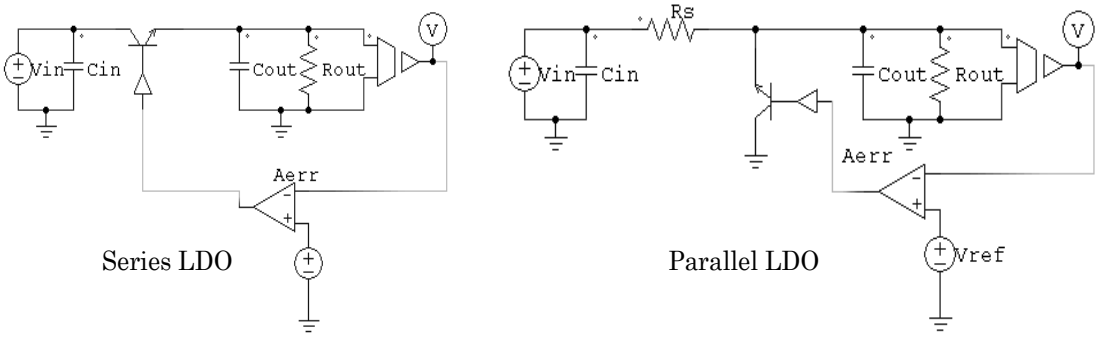


Fig. 2-10 LDO regulators

LDO regulators are used when input and output voltages are near similar. If this condition is not accomplished, their efficiency is punished drastically. LDO are exclusively step-down architectures implying that output voltages values are always lower than input ones. Their main advantages are their simple control (regulation can be achieved easily with a high accuracy) and their good harmonic generation, especially in high-frequency applications. Moreover, they deliver very low ripple values to the load. Nevertheless, these structures are less used

nowadays as embedded power supplies due to its poor efficiency and its important size and weight. Two examples of LDO are represented in previous Fig. 2-10.

To solve the efficiency problem inherent to LDO structures, switching converters have replaced progressively these linear converters during the past few years. Switching converters offers a higher efficiency despite of their more complicate control system. For PoL and VR applications, the Buck converter is the most widespread choice. The Buck converter offers several benefits like good efficiency, easy control and a good stability associated to its minimal-phase behavior. Therefore, the Buck converter represents the basic DC/DC power conversion block and it is described in detail in next sections.

2.2.2.2 The classical Buck Converter

Nowadays, the step-down Buck structure is the widest topology employed in PoL and VRM converters. However, some variations of the classical structure are found to improve the power efficiency. Basically, these variations are introduced in such a way to reduce losses in the active devices. The basic configuration involves one controlled-switch associated to a non-controlled one (freewheeling diode) as it can be seen in Fig. 2-11.

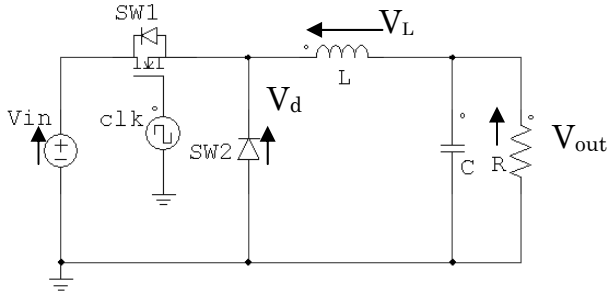


Fig. 2-11 Classical Buck converter

This configuration has considerable conduction losses due to the diode Forward voltage (V_d). As a matter of fact, DC/DC converters delivering low-output voltages to the load own high conversion rates and, therefore, they have small duty-cycles in steady-state. Consequently, the ON-state time of the freewheeling diode is augmented drastically increasing conduction losses and reducing the system efficiency correspondingly. As a result, the classical Buck converter is not recommended for embedded applications.

As a consequence, more optimal architectures based on the classical Buck are used in VR applications. The most widespread architectures used in VRs are described in next points.

2.2.2.3 The Synchronous Buck converter

The losses problem caused by the freewheeling diode of the classical Buck configuration can be reduced replacing this device by a second active switch. In low-power applications, a MOSFET is chosen normally due its resistive behavior pending its ON-state. Consequently, conduction losses are directly proportional to the conduction resistance of both active switches.

This topology called Synchronous Buck owns a power active switch named High-Side MOS (HSM, SW1) associated to a synchronous device named Low-Side MOS (LSM, SW2) as it is illustrated in Fig. 2-12.

The global behavior of this configuration is quite similar than the previous one. However, both MOS should work in a complementary way respecting their corresponding conduction times to avoid destructive short-circuits during their switching periods. To avoid both switches simultaneous conduction, a time delay (known as “deadtime”, see Fig. 2-12) is introduced in-between the activation control signals of both MOS.

As a consequence, the syncrhonous Buck architecture is a little more complex and expensive than the classical one due to the addition of the second MOSFET and its control system. Thus, for embedded applications, a trade-off is made among efficiency, complexity and cost.

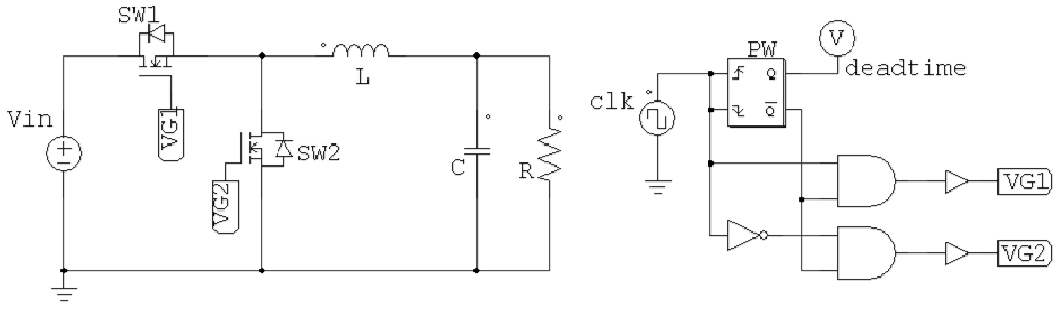


Fig. 2-12 Synchronous Buck and its MOSFET circuit control

Table 2-1 shows a numerical example of the gain in the converter efficiency using the Synchronous Buck configuration for a low-power supply. In this example, an example using a voltage conversion from 5-to1V ratio, i.e. a duty

cycle of 0.2 and delivering 20A to the load is presented. In the classical case, a Schottky diode with a very low Forward voltage (compared to a classical PIN diode where V_d>1V) is choosen. For the synchronous case, a MOSFET with minimal conduction resistance has been selected. Thus, the losses reduction obtained using the synchronous configuration can be observed in this example.

	Theoretical switch losses	Numerical example
Classical	$P_D = V_D \cdot (1-D) \cdot I_L$	$P_D = 0.38 \cdot (1-0.2) \cdot 20 = 6.08W$
Synchronous	$P_{SW} = R_{ds} \cdot (1-D) \cdot I_L^2$	$P_{SW} = 0.0026 \cdot (1-0.2) \cdot 20^2 = 0.83W$
Extract of datasheet specifications	Schottky Diode, IRF42CTQ030PbF : V_d=0.38V at I_d=20A, T_j = 125C MOSFET IRF6609: R_{dsON} = 2.6mΩ at V_{GS} = 4.5V, I_D = 25A [2.6] Buck Converter D=0.2 at V_{in}=5V, V_{out}=1V, I_{out}=20A	

Table 2-1. Comparison of losses in the switch in the Buck converter

2.2.2.4 The Multiphase Synchronous Buck converter

Synchronous topologies are preferred in low-voltage, high-current VR designs due to their enhanced efficiency. Nevertheless, supply requirements of new generation of embedded microprocessors cannot be covered efficiently by single-phase synchronous topologies. As a result, multiphase or parallel converters (see Fig. 2-13) were born to achieve these new power supply necessities.

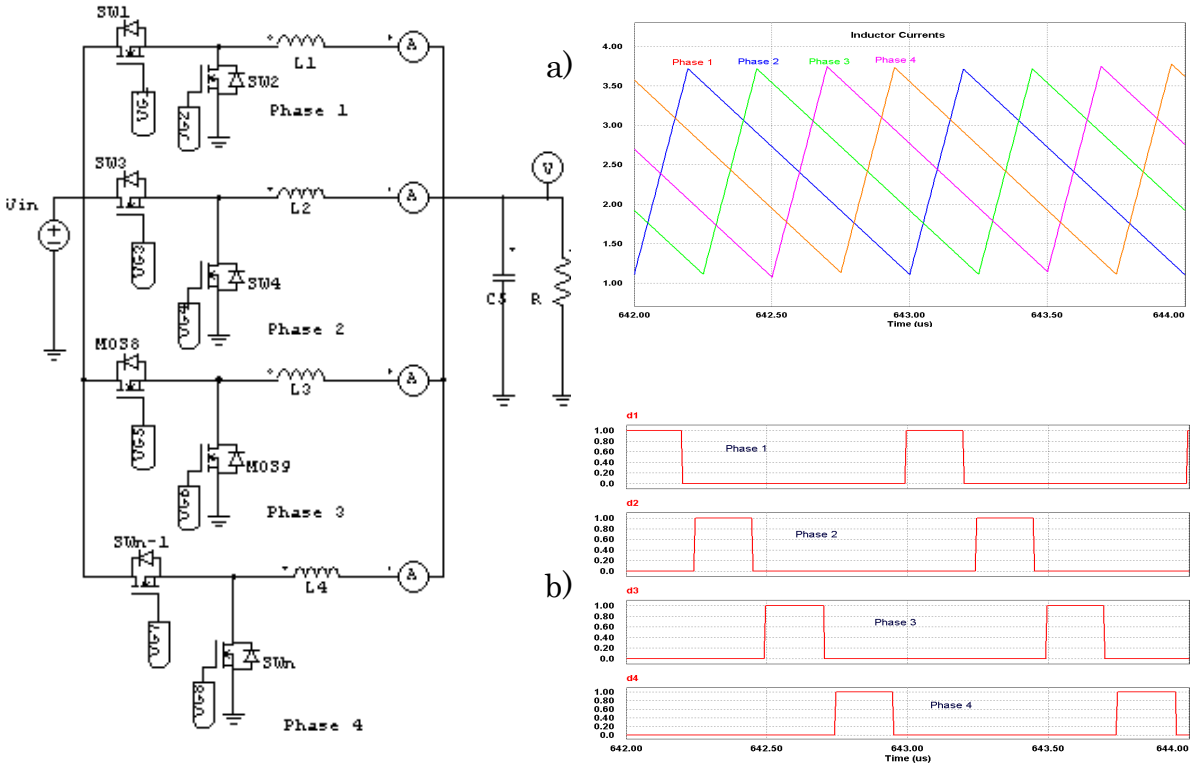


Fig. 2-13 Multiphase synchronous Buck converter working in interleaved mode: a) Inductor current per phase, b) duty-cycle per phase

Then, multiphase converters allow us an important increase of the output current delivered to the load without an excessive over-sizing of the active and passive components of the power converter.

Multiphase converters are composed by basic commutation cells or phases placed in parallel as it is shown in Fig. 2-13. Each phase is activated consecutively after the previous one in an interleaving mode, i.e. with a given time interval corresponding to the number of phases of the power converter. This interleaved operation mode reduces considerably output-voltage and input-current ripples and, consequently, converter losses too. Hence, this time interval or phase-shift is defined by (2.1):

$$\text{Phase shift } (^\circ) = \frac{360^\circ}{\text{number of phases}} \tag{2.1}$$

However, multiphase architectures still present some efficiency droops. This lack of efficiency can be minimized adding some changes to the architecture presented in this point.

2.2.2.5 Modifications in the Multiphase architecture

Multiphase synchronous Buck topologies working in interleaving mode have become an interesting option for VRs thanks to their easy design. Nevertheless, this architecture may become inefficient for large conversion ratios owning very low duty-cycles are used (e.g. 12-to-1V). In fact, low duty-cycles induce large inductor current ripples and, therefore, higher switching constraints. These constraints are translated in important switching and conduction losses in the active devices.

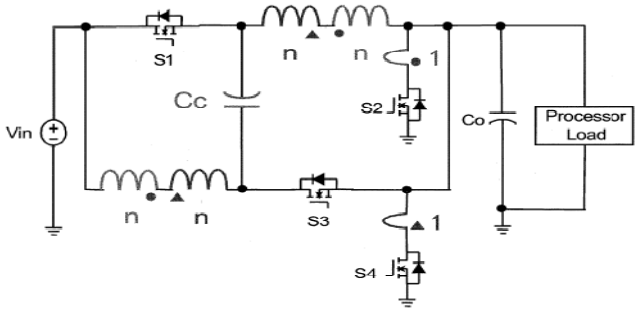


Fig. 2-14 Multiphase Buck converter with coupled-inductors

Therefore, other structures based on the multiphase synchronous Buck try to improve the converter efficiency and to answer to the exigent work environments

of new VR applications. In general, most of variations in the multiphase architecture serve to enlarge the converter duty-cycle reducing converter losses.

The simpler modification is presented in [2.7] [2.8] where classical inductors are replaced for coupled-inductors structures as it is illustrated in previous Fig. 2-14.

However, this variation engages several drawbacks. Firstly, the increase of the number of turns limits the inductor current slew-rate. Moreover, the inevitable leakage inductance existing between both coupled windings causes voltage spikes that may damage active switches or instigate some additional losses. To reduce these spikes, a clamping circuit is added and additional filters are used to smooth inductor currents. In brief, this new architecture becomes quite complicated although some gain in the converter efficiency can be obtained.

Another approach is introduced in [2.9] with the development of a two-stage conversion system as it can be observed in Fig. 2-15. In this work, a high-efficiency, two-phased DC/DC converter makes an initial 12-to-5V conversion. Next, a second high-frequency and high-efficiency multiphase converter completes the conversion from 5-to-1V. In this design, the cost and complexity of the final system is increased widely due to the duplication of the elements of the system. Moreover, the second converter needs a very narrow regulation control system. However, the global efficiency is augmented significantly.

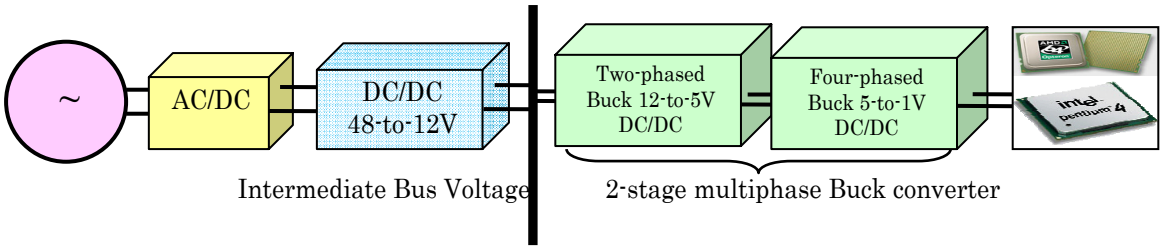


Fig. 2-15 Two-stage Voltage Regulator

In [2.10] a multiphase converter associated to an inductive clamping system is presented (see Fig. 2-16). In this work, authors improve the dynamical behavior of the converter during load transients using the “critical inductance” concept [2.11] . This theory calculates the maximal inductor value which gives the fastest transient response without compromising the efficiency. Thus, for inductor values larger than the critical one, efficiency and dynamical responses cannot be improved.

Therefore, the clamping system varies the inductance value per phase of the multiphase converter to be always under this critical value. In this context, authors force the output voltage to the desired working point. This point is calculated depending on the maximal output-voltage ripple and the maximal load current variation. Actually, this method is a variation of the Adaptive Voltage Positioning (AVP). However, the value of the inductances using this technique is extremely reduced. Hence, switching frequency should be very high to decrease inductance current ripple and to reduce conduction losses as well. Then, a trade-off between conduction and switching losses is present.

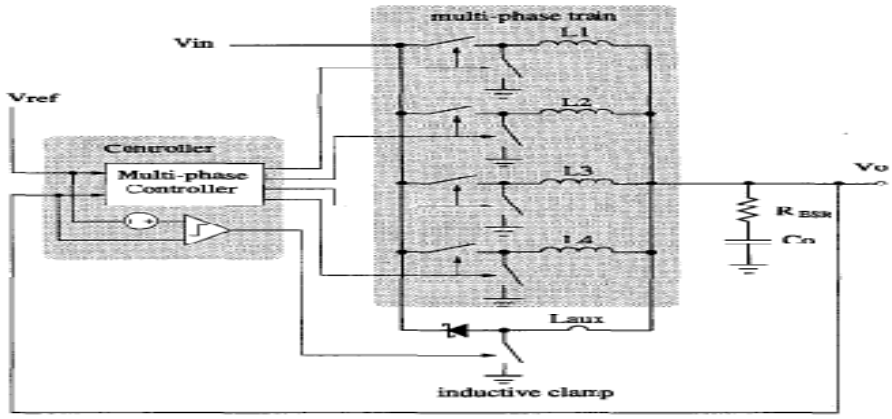


Fig. 2-16 Multiphase Buck converter with inductive clamping system

To sum up, the high supply-current needed by the new generation of embedded microprocessors is obtained thanks to more complex structures with enhanced efficiencies although new more complicate and accurate control techniques are also necessary. In this context, a lot of technological troubles associated to their power structure, their robustness, their corresponding control technique and their accuracy still have not a clear solution.

Therefore, our work methodology consists in a systematic elaboration of digital control laws and their corresponding validation in experimental prototypes. For this reason, the work elaborated during the past few years have required the simultaneous design of the parts concerning a full digitally-controlled multiphase synchronous power converter, i.e. the power stage, the digital controller and the interfaces between power and control boards.

As a result, the multiphase synchronous Buck converter working in interleaved mode has been selected because its behavior is relatively well-known. Thus, our efforts have been focused on the development of performing control algorithms

adapted to a wide range of loads. For that matter, a state-of-the-art of the different parts involving PoL and VR converters is presented in the following section. Moreover, the pros and contras of present current manufactured solutions are disclosed as well as their associated digital control laws.

2.3 State-of-the-art and Evolution of Digital Technologies applied in Embedded Power Supplies

2.3.1 Introduction

Systems owning Digital Control (SDC) offer important advantages versus Analogue-Controlled Systems (SAC). Actually, new commercial designs point towards full-digital architectures replacing current SAC.

Indeed, SDC has lower (or comparable at least) power consumption than SAC thanks to the decreasing scaling in CMOS technologies. Moreover, the number of components in SDC is reduced drastically, then; injurious effects originated by external parameters like changes in the environment temperature, white noises, tolerances of the components or changes in the manufacturing procedures are reduced significantly. This later skill of SDC implies an important increase of the reliability of the system and, therefore, the Mean Time Before Failure (MTBF).

In SDC, integration density is increasing constantly. Then, more functions can be included in the SDC allowing designers to implement less conservative digital control laws. After that, non-linear control techniques which are nowadays unfeasible using analogue controllers can be implemented.

Concerning to multiphase systems, SDC permits a fine synchronization of their duty-cycles. This skill is very useful when the number of phases is high.

In terms of design, HDL techniques allows designer lower design times and higher flexibility to changes in their final applications. Therefore, development costs and implementation times (less Time to Market) are reduced. This is particularly important when environmental conditions of the system are often changed. In this case, new hardware configurations are not necessary implying a reduction of the final surface and cost. As an example, the traditional passive components of the analogue calibration system can be eliminated and replaced for a digital re-programmable regulation. Thus, the re-programmability of SDC

by means of changes in the software code and their high adaptation to different applications make them very practical in industrial applications.

Nevertheless, SDC hold several disadvantages and some technological frontiers still persists in these new digital controllers. Firstly, changes in the environment temperature may still cause mismatches in several devices of SDC like the clock system, the voltage reference or the ADC (Analogue-to-Digital converter). In second place, state-of-the-art digital controllers still do not own the performances enough to replaces analogue controllers. This later issue is especially important in very high-frequency applications due to time constraints. As a result, these time limitations are reflected in a drastic reduction of the bandwidth of the system because of inherent delays of the algorithm and the digital structure.

Moreover, the accuracy of the control system will be fixed by the SDC resolution. In fact, SDC resolution is given by both of ADC and DPWM (Digital Pulse Width Modulator) devices. As a result, to obtain a high-resolution ADC and DPWM involves developing large, complex and expensive structures. Additionally, to work with high-resolution devices engage an increase of the clock frequency of the DPWM and the sampling frequency of the ADC correspondingly. As a consequence, their power consumption and their cost are augmented too. Table 2-2 summarizes the pros and contras of using SDC instead of SAC.

Skill	Digital	Analogue
Power consumption	Lower	Higher
Robustness against tolerances	Higher	Lower
Robustness against delays	Lower	Higher
Flexibility	Higher	Lower
Time-to-market	Lower	Higher
Robustness against failures	Higher	Lower
Communications with other devices	Higher	Lower
Cost	Higher	Lower

Table 2-2 Comparison of Digital vs. Analogue controllers characterisitics

Thus, our main aim is to replace the classical analogue control stage for a digital controller which satisfies the advantages exposed in previous paragraphs. Hence, a digitally-controlled DC/DC converter can be divided in different parts as it can be observed in Fig. 2-17.

The first part corresponds to the power stage followed by the input or acquisition module. In this second stage, state-space variables of the converter are digitalized to be useful for the control stage. The third block is composed by

the digital controller generating the required control law. Finally, an output module or DPWM produces the required duty-cycle to control both switches of the power converter.

Therefore, some solutions to improve the performances of a full digitally-controlled multiphase synchronous power converter designed to supply embedded microprocessors have been studied in next chapters. Actually, the different parts of this sort of architectures have been analyzed in order to respond to the technological problems found along these years of work.

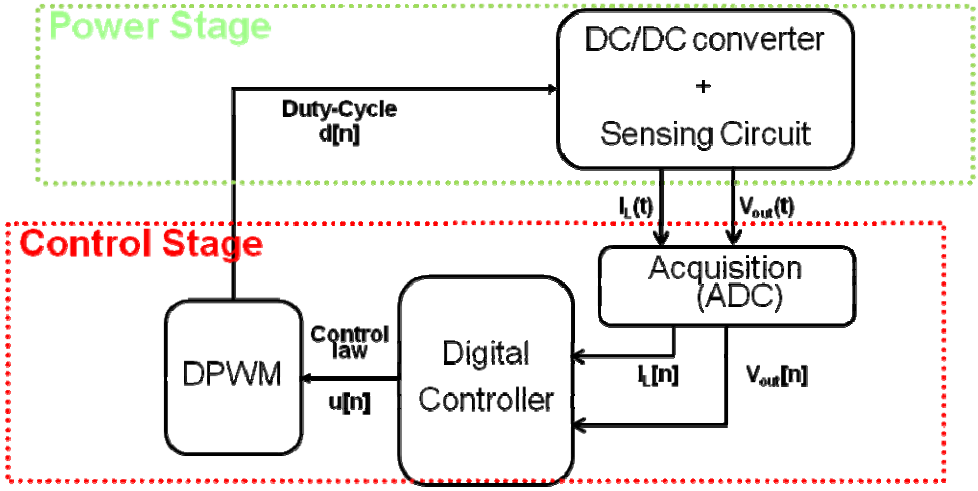


Fig 2-17 General block diagram for a Digital DC/DC converter

2.3.2 Analogue-to-Digital Converters

An Analogue-to-Digital block transforms the power converter continuous-time state-space variables into discrete-time ones for a proper matching with the digital controller.

ADC resolution is a critical factor and an important source of error in digitally-controlled power converters. This parameter (associated with the DPWM resolution) determines the final accuracy of the digitally-controlled power converter. Thus, the ADC resolution is defined by its available number of quantification levels defined by the number of bits of the ADC.

Actually, a trade-off is established between the ADC resolution and its rapidness (conversion times). Normally, a large number of bits involves a large or/and an expensive architecture and also slow conversion times.

For this reason, if the desired application requires low conversion times, the number of bits should be small to avoid large and expensive structures. In consequence, the resolution and topology of the ADC must be selected carefully.

As a general rule, the ADC resolution is defined by the maximal allowed step or variation of its input signal. For instance, to digitalize correctly the output voltage of a digitally-controlled power converter, the ADC quantization step (ΔV_{qADC}) must be lower than the desired maximal output voltage ripple (ΔV_{outMAX}) but higher than the DPWM one as it is illustrated in (2.2) to (2-4):

$$\Delta V_{outMAX} > \Delta V_{qADC} > \Delta V_{qPWM} \tag{2.2}$$

$$\underbrace{\Delta V_{outMAX}}_{\text{maximum voltage variation}} \geq \underbrace{\frac{V_{fsADC}}{2^{n_{ADC}} \cdot H_v}}_{\Delta V_{q\_ADC} = \text{voltage quantification error}} \tag{2.3}$$

$$n_{ADC} = \text{int}\left(\log_2 \left(\frac{V_{fsADC}}{\Delta V_{qADC} \cdot H_v} \right) \right) \tag{2.4}$$

With: ΔV_{outMAX} = maximal variation allowed in the measured variable.

ΔV_{qADC} = ADC voltage quantification level

ΔV_{DPWM} = DPWM quantification level

V_{fsADC} = ADC Full-Scale Voltage

n_{ADC} = ADC bits number

H_v= Sensor gain

By and large, ADC introduces an important delay which should be taken into account in the digital control law design. This delay time (t_d) is composed by the acquisition time (t_{zoh}) and the conversion time (t_{conv}) which varies depending on the ADC structure.

$$t_{d\_ADC}(t) = t_{zoh} + t_{conv} \tag{2.5}$$

Others important factors in ADCs are the slew-rate and the noise immunity since the switching noise generated may weaken the digitalization process.

2.3.2.1 ADC architectures

ADC structures can be classified depending on which conversion characteristic it is desired to be optimized. Thus, the fastest structure is known as “Flash” or “Parallel” ADCs and it completes the analogue-to-digital conversion in only one single clock cycle. However, this small conversion time is obtained by means of complex structure employing a large surface and, consequently, a high cost. This architecture is based on simultaneous parallel comparisons by means of analogue

comparators. Consequently, the higher desired resolution, the higher number of analogue comparators needed (e.g. for n=10 bits, 2^n-1=1023 comparators are needed). As a result, this topology becomes quite expensive for high-resolution ADCs. Additionally, it is quite sensitive to the switching noise.

A simplified version of the previous ADC structure is called "Windowed ADC". In fact, this is a reduced version of the previous one owning a lower resolution and a reduced numbers of digital levels. This architecture is based on a narrow regulation around the average value of the ADC analogue input signal. In VR converters, these ADCs take advantage of the narrow regulation around the voltage reference signal. Thus, digital levels which are far away of this voltage reference and which are not usually employed by the digital controller are eliminated. This topology presents a better trade-off between complexity and size than the previous one. However, the practical implementation of "Flash" or "Windowed" ADC is pretty difficult since very accurate analogue comparators and resistances are required to achieve reliable small quantization levels. In the Fig. 2-18, it could be observed how a 9-bin (less than 4 bits of resolution) Windowed-ADC (bottom trace) gives similar results than a classical 8 bits Flash-ADC (top trace).

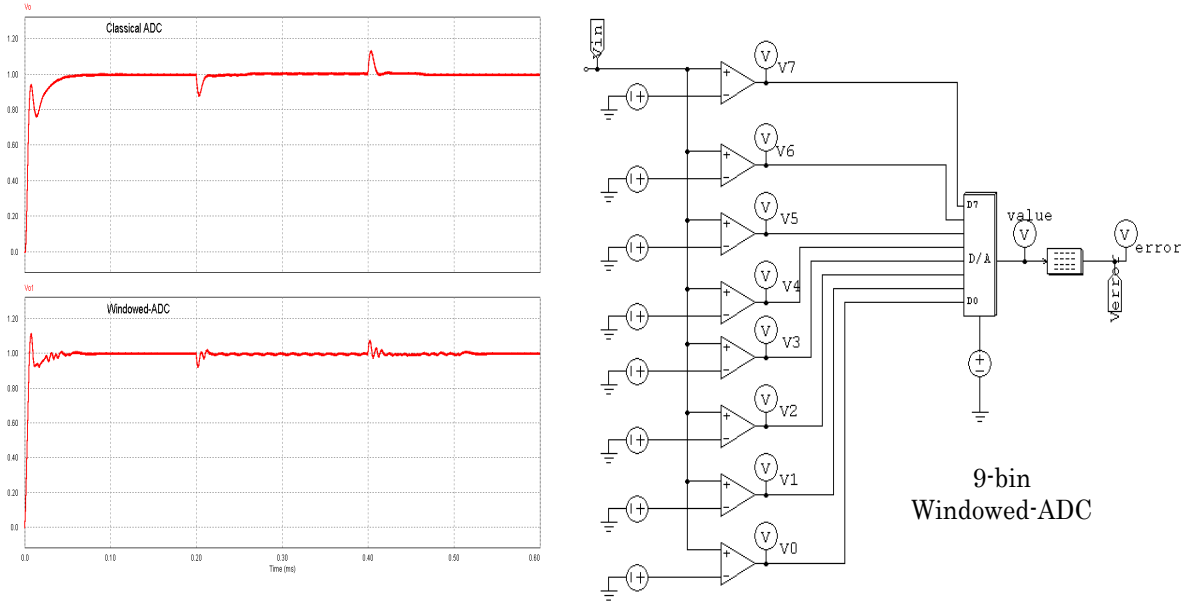


Fig 2-18 Flash Windowed-ADC in a digital voltage-mode controlled Buck converter

In previous structures, fast conversion times take priority over large resolutions. Nevertheless, other architectures are optimized to obtain higher resolutions. This is the case of "Integrator" ADCs where very large resolutions

are obtained despite of conversion times are also very large. Here, the conversion is made by means a double integrator and a pulse counter which defines the ADC resolution. However, these structures are not used in VR designs due to their important conversion times.

A trade-off between Flash and integrator ADC configuration is the "Successive Approximations Register" ADC (SAR). This structure is cheaper than the parallel architecture. In contrast, it needs n clock cycles to make a single analogue-to-digital conversion with n bits of resolution.

Joining some parallel and SAR architectures, another topology called "Pipelined" ADC is found. This last one is employed frequently in commercial digital controllers. Now, the conversion is achieved in a lower time than SAR converters and with a fewer number of analogue comparators (for the same resolution) than parallel ADCs (e.g. for n=10 bits, number of stages=2 and a 5 bits DAC, 2^5-1=62 comparators are needed). A summary of the most common commercial ADCs is illustrated in Table 2-3. Thus, for very high-frequency VRs, flash architectures are preferred due to their lower conversion times. In contrast, for medium and low-frequency applications, pipeline structures are preferred because they assure a good resolution and acceptable conversion times.

ADC architecture	Conversion time - ➔ +	Complex. - ➔ +	Resolution
Flash	1 · Tclk	▲	n bits = 2^n-1 comparators
Pipeline	number of stages · Tclk		n bits = number of stages · x bits DAC number of stages · 2^x-1= comparators
SAR	n · Tclk		n bits = bits number of DAC
Integrator	(2^n+1) · Tclk		n bits = bits number of pulse counter

Table 2-3 Commercial ADC summary

The architectures explained in previous paragraphs are available in commercial ICs. To complete our state-of-the-art, some structures non-conventional and non-commercial products based on a microelectronic full-custom design are presented.

Therefore, the first structure introduced is known as "Delay-line based" ADC. It provides a high resolution keeping a low consumption and a small size. Nevertheless, it presents some linearity problems if the delay line is not well

calibrated. Thus, its working principle relies on a string of delay cells supplied from an analogue voltage composing the delay line. The conversion starts when a pulse is propagated through this line. Then, some cells are sampled and their logic values are stored in a register. Theoretically, this system furnishes zero error. In practical terms, the conversion process, the temperature or voltage reference variations origin differences in the time propagation through the delay line. Consequently, this inconvenient make it useless for multiphase systems. To solve it, a calibration circuit is added employing two matched delay-lines as it is shown in Fig. 2-19. One delay-line is supplied with the voltage that should be digitalized and the other identical delay-line is supplied from an exact reference voltage. Thanks to the calibration system, precision components are not required reducing the cost [2.11]

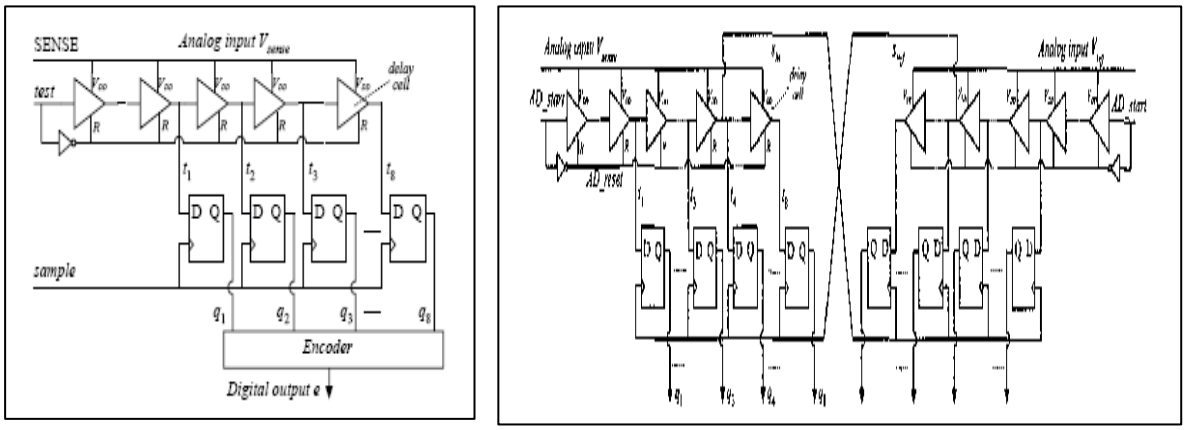


Fig. 2-19 Delay line ADC: simple (left) and with calibration system (right)

2.3.3 Digital Pulse Width Modulators

In digitally-controlled power converters, DPWM performs the digital-to-analogue conversion. Indeed, as in the ADC case, DPWM resolution is a key-point given that the set of duty-cycles and, therefore, the final output voltage of the converter depend on the refinement of this parameter.

In [2.13] and [2.14] a practical design guideline is presented for a correct calculation of the ADC and DPWM resolutions in digitally-controlled DC/DC converters. Thus, DPWM resolution must be high enough to avoid limit-cycle oscillations problem. In these works, authors define limit-cycles as low frequency (inferior than switching frequency) oscillations disturbing the steady-state output voltage in PWM-controlled converters. As a result, there are several rules to avoid limit-cycles oscillations in digitally-controlled power converters which can

be summarized in three main design points:

1. To have a final system owning sufficient open-loop gain.
2. To use a digital compensator filter with an integrator element (i.e. a pole must be placed in z=1).
3. To have a DPWM resolution large enough.

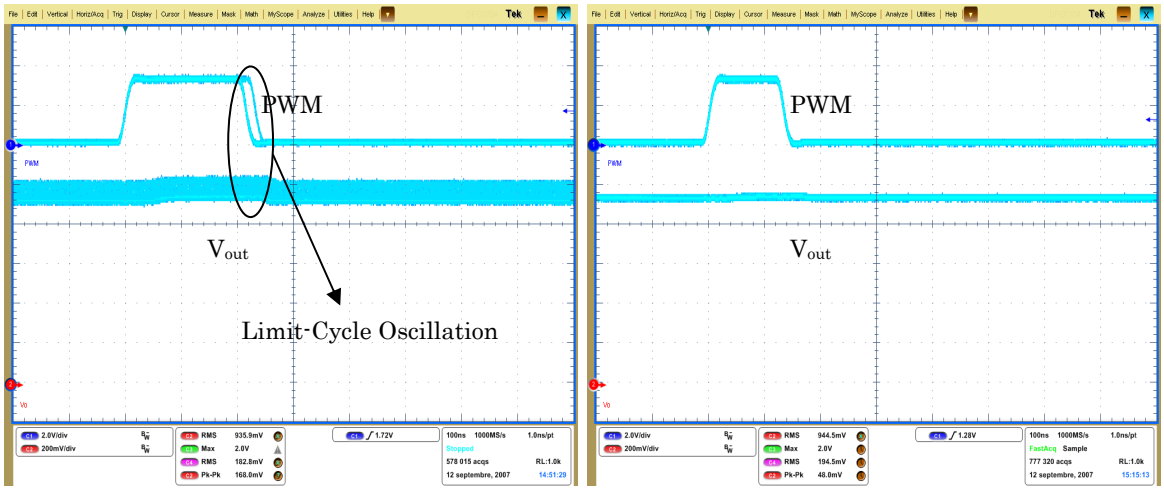
Fig. 2-20 exemplifies the effect of a lack of resolution in the DPWM where undesirable (and often unpredicted) variations of the output voltage are observed.

This scope was captured using the "Fast Acquisition" or "Repetitive" mode of the oscilloscope and it can be observed how the converter duty-cycle varies unnecessarily for an assigned control order. Then, if DPWM resolution is small, limit-cycles are presented. As a consequence, the output voltage jumps between two digital steps. On the contrary, if resolution is high enough, then, limit-cycle oscillations are eliminated (see right side of Fig. 2-20). Therefore, the required DPWM resolution can be calculated as follows:

$$n_{PWM} = \text{int}\left(n_{ADC} + \log_2\left(\frac{V_{out} \cdot H_v}{V_{fsADC} \cdot D_{\min}} \right) \right) = \text{int}\left(\log_2\left(\frac{V_{out} \cdot H_v}{\Delta V_{qADC} \cdot D_{\min}} \right) \right) \quad (2.6)$$

With: V_{out} = Output Voltage

D_{min}= Minimum duty-cycle



Low-resolution DPWM High-resolution DPWM

Fig. 2-20 Influence of the DPWM resolution in the output voltage of a digitally-controlled power switching converter.

In industrial applications, DPWM resolution can be also found like the smallest time required by the DPWM (i.e. defined by the minimal clock period) to vary its duty-cycle value one single step. This time is expressed using the maximal

number of digital levels that the DPWM can generate for an assigned clock frequency (e.g. 60 steps with a time-step of 16ns for a 60MHz clock frequency and a 1MHz DPWM signal).

Similarly than in the ADC case, the DPWM introduces a time delay which should be taken into account by the digital controller. This delay is proportional to the time used to generate the duty-cycle in each switching period and it is variable depending of the value of the duty-cycle for each switching period:

$$t_{DPWM}(t) = d \cdot T_{sw} \tag{2.7}$$

With: T_{sw} = Switching period

d= duty-cycle

2.3.3.1 DPWM topologies

Commercial embedded DPWMs are based on "fast-clock counter" structures. This architecture owns the same working principle than the analogue PWM implementation. Thus, the DPWM input signal is uniformly sampled and later it is send to a Zero Order Hold circuit (ZOH). Finally, the PWM signal is generated comparing the ZOH output with a saw-tooth waveform. This topology presents a good linearity and is quite simple. Nevertheless, its resolution is quite limited since it is associated to the clock frequency. Thus, the problem is that the LSB of the DPWM can only be varied when clock changes. As a result, to have a high resolution, a small clock period is required. In practical terms, the larger clock frequency, the larger power consumption.

In the same way than in the ADC case, the second architecture proposed is known as "Tapped delay-line" or "Ring oscillator". Now, the fast-counter is replaced by a delay-line working at the power converter switching frequency. This schema offers a good resolution with small power consumption thanks to its reduced clock frequency (same than switching frequency). On the other hand, the surface employed due to the multiplexer is quite large. Moreover, asymmetries in the delay-lines may cause important errors in multiphase systems. To solve it, multiple PWM signals can be generated by the addition of various multiplexers to a single delay-line. As a result, the problem of the asymmetry of the delay-lines can be solved in spite of the surface needed to complete this function is increased drastically [2.14]

An acceptable compromise among resolution, consumption and surface is achieved with the "Hybrid delay-line/counter" topology. Here, a counter provides some bits resolution (N_c) and the remaining bits are achieved thanks to the tapped delay-line. Thus, this delay-line consists in a set of resettable flip-flops used as delay cells. Now, the clock frequency is proportional to the digital level numbers of the counter, (e.g. in an 8 bits DPWM with N_c=3 bits, f_{sw}=1MHz, $f_{clock}=2^{Nc} \cdot f_{sw}$=8MHz). Otherwise, this technique presents the classical disadvantages of delay-lines previously exposed in [2.11]

Another structure presented in [2.16] is called "Ring–Oscillator–Multiplexer." This topology is similar to the previous one in terms of area and consumption but it is specially indicated for multiphase systems because of its n-channeled output. Thus, it is composed by a differential ring oscillator yielding a determined set of taps and a multiple output multiplexer selecting the appropriate signal from the ring for each output. At the same time, the multiplexer should control the timing for each phase. The PWM signal generation is started when a square wave is propagated along the ring. Then, when the rising edge reaches the first tap, the rising edge of the PWM signal for the first phase is generated. Otherwise, the falling edge of this PWM signal is generated when the rising edge of the propagating square wave reaches a specified tap in the ring. In short, multiplexer is used to specify the tap for first phase and the remaining PWM signals for the other phases are generated in a similar way.

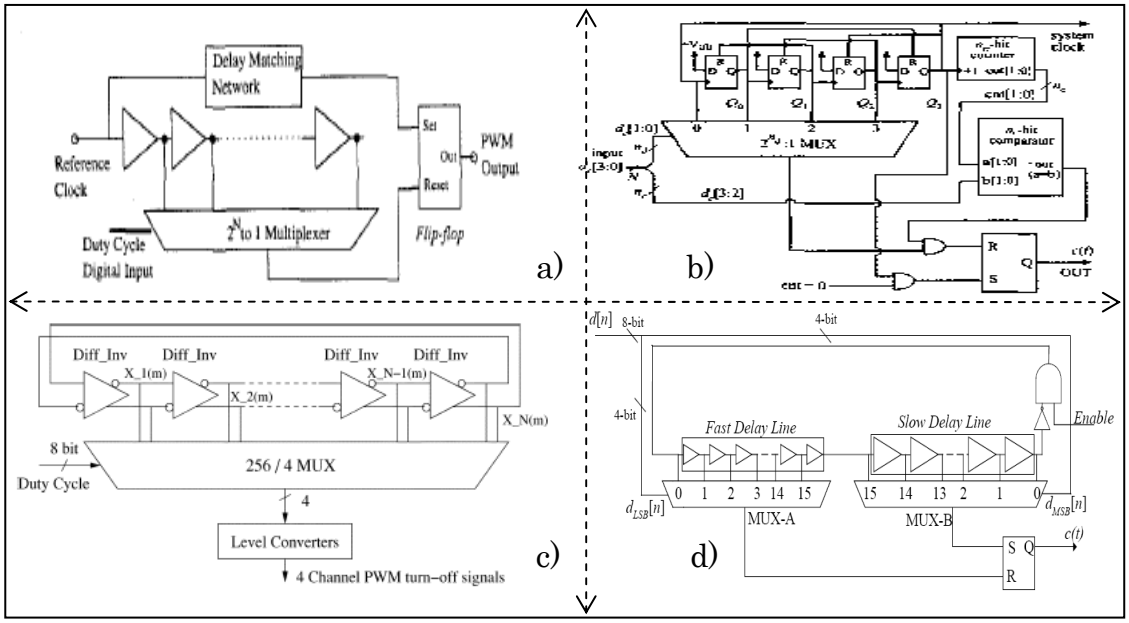


Fig. 2-21 DPWM topologies: a) Tapped delay-line, b) Hybrid delay-line/counter, c) Ring-Oscillator-Multiplexer, d) Ring-based segmented

The last structure presented is quite similar to previous ones but yielding a lower surface. It is called "Ring-based segmented" DPWM. On the contrary, delay-lines still causes non-linearity problems [2.17] These previous DPWM topologies are illustrated in previous Fig. 2-21.

2.3.4 Digital Controllers

Digital regulation applied to DC/DC converters is not a new concept. At the beginning of the 70's, first re-programmable devices appeared. They represented a technological revolution since their functionality can be modified completely changing the software code. Nowadays, digital systems are usual in our lives and in commercial designs.

Referring to our study case, some alternatives can be used to implement the digital controller like PICs, µcs, DSPs, PLDs, FPGA, ASICs or combinations of them as it is shown in the Fig. 2-22. Therefore, the list of digital controllers can be divided in three majors groups depending on their architecture and their functionality. First one is composed by independent logic gates, which means, ICs with fix functionality (AND, XOR…). Their low price and high flexibility in designs makes them sometimes useful. However, these systems are restricted to very easy linear control laws due to the significant complexity of the final design.

In the second group, systems with re-programmable functionality are found. This group can be also separated into two sub-groups more. On one hand, systems owning fix-architecture (like PICs, µcs or DSPs) are placed and, on the other hand, devices holding programmable-architecture (PLDs, FPGA) are found.

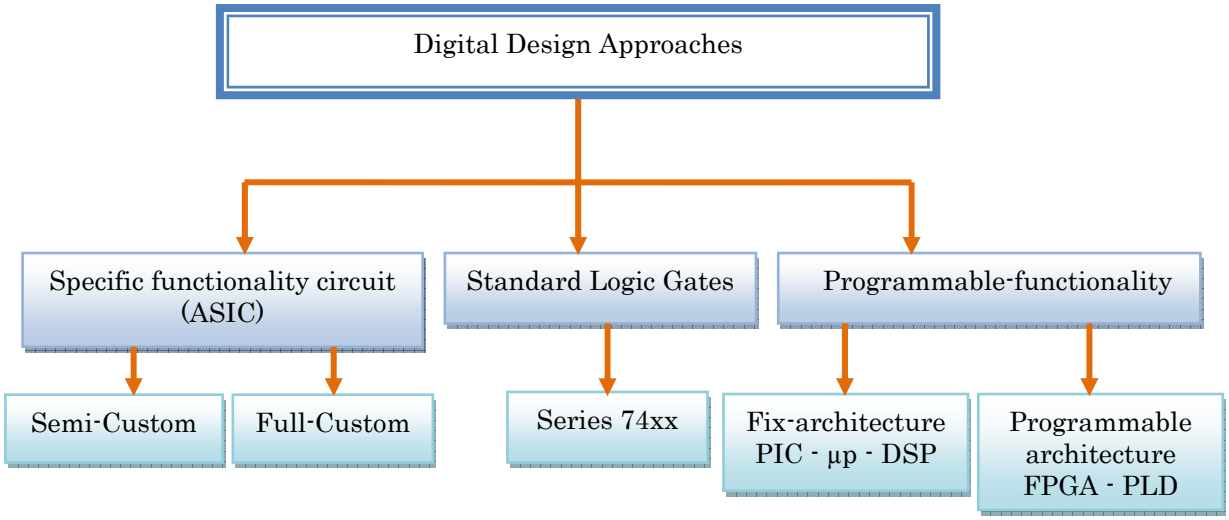


Fig. 2-22 Digital design possibilities

The fix-architecture devices are programmed to accomplish a dedicated function by means of a software code. They are an easy, low-cost and fast way to implement digital control laws. Otherwise, their performances are quite limited since they usually execute sequentially their software instructions and/or functions. As a result, their use is restrained basically to low or medium-frequency applications. One advantage of this sort of controllers is that they can incorporate built-in ADC and DPWM modules making lower the final system complexity. Another remarkable point is their capability to work with fix or floating-point architectures. Traditionally, to work with floating-point architectures allow users to obtain a higher resolution and accuracy in the calculations. On the other hand, this operation mode employs usually a large amount of time to execute each single instruction. Therefore, another trade-off between accuracy (resolution) and speed (frequency) is found again. Due to these later arguments, high-frequency applications are restricted to fix-point controllers in order to decrease the size and the execution time of the control algorithm. Thus, PICs and μcs have not still the performances enough for high-resolution and high-frequency applications. As a result, high-frequency DSPs are used to achieve these high-frequency requirements. The use of these devices makes the system quite expensive and not useful for commercial applications. Moreover, main commercial high-frequency floating-point DSPs have not integrated ADCs and DPWMs in their evaluation board increasing the complexity and price of the final system.

Alternatively, programmable-architecture devices offer greater possibilities to designers because of the parallel execution of the algorithm functions. Hence, an important reduction of the algorithm execution time is achieved. Indeed, these devices are formed by a huge number of logical gates which are programmed using HDL techniques to achieve specific functionalities. Obviously, some drawbacks are present like their important power consumption, price, complexity...

As a result, these programmable-architectures introduce another trade-off among resolution, frequency, power consumption, price and complexity. As a matter of fact, the larger resolution required, the higher clock frequency, power

consumption and number of logic gates. It is worthy to note that to increase the number of logic gates is an additional cost to our final system.

Finally, ASICs are classified in the third group. Here, the IC final functionality is tailored to specific customer requirements. ASICs are divided into Full or Semi-custom designs depending on if its design is completely made Ad-hoc or using some prefabricated modules (logic gates, DSPs, ADCs, ROMs…). By reasons of costs and complexity, ASICs are reserved exclusively to cases where a very large number of the same IC is demanded. Table 2-4 summarizes the characteristics of digital controllers.

	Standard logic gates	Programmable devices				ASIC
		PIC	µc	DSP	FPGA	
Integration density level	Very low	medium	high	high	Very high	Very high
System complexity	High	low	low	medium	high	Very high
Power consumption	low	low	medium	medium	medium	Very low
High-frequency performances	medium	low	medium	high	Very high	Very high
Unity cost	Very low	Very low	low	medium-high	high	Very high
Design cost	Low	low	low	medium	high	Very high
Design flexibility	High	high	high	high	Very high	Very low
Design time	Low	medium	medium	medium	high	Very high

Table 2-4 Comparison of digital controllers

2.4 Evolution of Digital DC-DC Converters

Digital control in DC-DC converters is not a new idea. For the time being, they have progressed rapidly during the few last years and main manufacturers of embedded applications have invested in more reliable, cheaper, flexible and performing systems. This section lists the chronological evolution of digitally-controlled DC/DC converters during last decade.

Thus, first digital DC/DC converter appears in 1999. This was a synchronous multiphase Voltage-Mode Controlled (VMC) Buck with large passives components. As a consequence, it owned a low switching frequency (250kHz). This prototype was implemented using first commercial FPGAs [2.18] .

In the year 2000, a low-frequency (50kHz) synchronous VMC Buck-Boost power converter was implemented using a DSP. This design could switch from full-load

operation mode (12A, using PWM techniques) to low-consumption mode (10-150mA, using PFM) [2.19]

The following year (2001), a synchronous VMC Buck oriented to low-current applications was developed using a DSP too. In this case, the size of passives starts to decrease reaching higher switching frequencies (around 1MHz) [2.20]

A synchronous 1MHz (4·250kHz) multiphase Buck converter appears in 2003. It was implemented in a 0.25µm CMOS process. Despite of its digital voltage regulation, current loop is made by means of estimation techniques [2.21]

Several publications emerged in 2004. The most important work in the digital control field applied to power converters was presented by the University of Colorado. In this work, a high-frequency (1MHz) digital synchronous VMC Buck was implemented in a 0.5µm CMOS standard process and employing a very small surface (1mm^2). Moreover, this design can work in parallel structures thanks to a communication bus [2.22]

First apparition of AVP (Adaptive Voltage Positioning) concept linked to Current-Sharing techniques made possible that the boundary of 1MHZ was exceeded for first time in a mix of analogue and digital structures. It combined two 7 bits DACs and an analogue RC filter in the voltage-loop to assure stability. The control laws were implemented in a FPGA [2.23]

The University of Berkeley developed in 2004 a synchronous VMC Buck in a 0.25µm CMOS standard process (total surface of the converter of 4mm^2) for portable applications. To make optimal its consumption, the converter can switch from PWM (normal mode) to PFM (standby mode) depending on the load demands [2.16]

In 2005, the University of Colorado developed again a predictive control law using a FPGA. This work is especially interesting because it gives a good approach of digital CMC obtaining good results. This control law was called "One-Cycle Predictive Current" (OCPC) control law and it will be studied in detail during next chapters [2.24]

Referring to commercial VRs applications, first digital controllers appear at the beginning of 2006. Up to this moment, all the preceding controllers have been analogue with some digital modules inside the IC. At the present time, some full digital controllers have been commercialised. As an example, Philips launched a

high-efficiency DC/DC converter with built-in active devices for cell-phones or PDAs. It can deliver 1A and to work at switching frequencies around 500kHz. Moreover, the digital control allows switching the working mode from PWM to PFM to save energy [2.25]

By the way, Intersil has launched the series ISL659x of PWM digital controllers that can manage up to 6-phased interleaving converters with a switching frequency up to 1.5MHz per phase [2.4]

Owing to integrated PoL converters, Power One has developed the ZY7120 delivering up to 20A [2.26] . Other enterprises like Texas Instruments or Artesyn are just launching new digital DC/DC controllers for VR applications. These new commercial products show the constant evolution of this field where the power management requirements are increased year by year according to the severe laws of market.

2.5 Conclusion

Along this chapter, main working principles of Distributed Power Supply (DPS) architectures for embedded microprocessors have been presented. Thus, DPS topologies share the energy conversion and electrical level adaption in several blocks obtaining more efficient and flexible architectures. By the way, the last block before the final load to supply (e.g. microprocessor) is a special type of power converter called PoL (for low-power applications) or a VR (for high-current applications) converter. PoL and VR converters are placed as close as possible to its corresponding load reducing transfer losses and improving power matching.

Hence, the PoL and VRs environment has been disclosed as well as the motivation to replace classical analogue control systems for those more efficient, flexible and cheaper digitally-controlled. In general terms, a digitally-controlled power converter is composed by four specific blocks: the power stage, an acquisition or input stage, a digital controller and an output module or DPWM which generates the duty-cycle signal for the power stage. These four blocks and their associated properties have been disclosed in detail along this chapter and some design guidelines have been given for a proper design and a correct calculation of the key parameters like the input and output resolution in order to avoid limit-cycle oscillations problem. Thus, the minimal number of bits of the

input and output modules have been calculated showing that the input module should have a quantization step always lower than the maximal variation of the signal that should be converted into the digital field. As a result, in digitally-controlled power converters, the most critical variation of the analogue values is given by the output-voltage ripple. In our study case, this value is imposed to 1% of the output voltage. Thus, the ADC quantization step should lower than this value. At the same time, the DPWM quantization step should be always lower than the ADC one to avoid limit-cycle oscillations problem.

Therefore, a state-of-the art about new high-frequency, high-current and low-voltage supply modules have been completed in order to understand better the present commercial products in this field. Thus, our work has been decomposed in several chapters corresponding to our scientific contribution along these three years of dissertation taking into account that the technical specifications of our new embedded supply module has been imposed by Freescale.

Thus, the analysis of the power stage analysis is presented in our third chapter where a theoretical study of the elements involving the power converter is carried out. In consequence, the conclusions obtained in this chapter have been used in next chapters to develop the power stages for our experimental prototypes.

Additionally, the theoretical study of several control laws for VR applications is developed in the fourth chapter. This section establishes a design methodology for digitally-controlled power converters based on simulation models.

Finally and in order to illustrate the conclusions obtained in the previous theoretical studies, some experimental implementations of digitally-controlled DC/DC converters are shown in the fifth chapter. Then, the design process for two experimental prototypes using different digital controllers is explained in this part

Chapter 3

Synopsis Of Multiphase Converters

3. SYNOPSIS OF MULTIPHASE CONVERTERS

3.1 Introduction

The multiphase synchronous Buck converter working in interleaving mode has been introduced in the previous chapter. This topology seems a good candidate for VR applications due to the advantages formerly explained. Thus, to face up the exigent power supply specifications imposed by main μp manufacturer, the different components involving the power stage of a multiphase architecture have been studied along this chapter. Indeed, the selection of passives and actives components of the power converter has been made carefully to obtain acceptable performances in our final system. As a consequence, the main design premises disclosed during this chapter are oriented to obtain an acceptable efficiency in a wide range of loads. Moreover, high switching-frequency constraints have been also taken into account in the choice of components. Other relevant parameters for the design of the multiphase converter are the power density, size, price and thermal management. First of all, a study to obtain the optimal number of cells in a multiphase converter oriented to high-current VR applications is presented.

Furthermore, an accurate lossless technique to measure the inductor current in high-frequency power converters is disclosed in the last point of this chapter. This technique is particularly important because of the high current levels delivered by multiphase architectures where classical current sensors are an important source of losses in this kind of applications.

3.2 Technical specifications for the multiphase power converter

The technical specifications for the power converter have been chosen following the supply trends exposed in Fig. 2-5 and also the design guidelines exposed in [2.1] In this last reference, additional steady-state specifications (like maximal output-voltage ripple) and transient requirements (like inductor-current slew rate or maximal voltage deviation under load variations) are proposed. Table 3-1 lists the main technical specifications imposed by Freescale for our prototype.

Specification	Per phase	Total
Output Voltage (V)	-	1
Output Current (A)	30	120
Switching Frecuency (MHz)	1	4
Output Voltage Ripple (%@mV)	-	1@10
Slew rate (A/µs)	-	450
Maximal Overshoot (mV@µs)	-	50@25
Maximal Settling time (µs)	-	350

Table 3-1 Technical specifications for multiphase DC/DC converters

3.3 Selection of the number of phases

The choice of the number of phases of the converter depends on its input/output ratio and the power supply levels desired by our final application. In the automotive field, three-phased architectures are preferred due to their fix power conversion ratio imposed for the input and output voltage.

However, in VR applications, the number of phases is often variable and it varies according to the final application. In general, the higher current to provide, the higher number of phases implemented. The main reason is to distribute uniformly the total current delivered by the power converter among phases. This current distribution allows a reduction of the current flow per inductance and, therefore, a reduction of global conduction losses and failures due to thermal problems.

Another characteristic of multiphase converters is their higher slew-rates and faster transient responses respect to those classical single-phased. This is explained thanks to the reduction of the inductor value per phase as it can be observed in (3-1).

$$\text{Total inductance value of the multiphase converter} = \sum_{i=1}^{n} \text{Inductance value per phase} \quad (3.1)$$

with n=number of phases

Thus, desired transients specifications in the multiphase case can be obtained using reduced inductance values compared to the single-phase case. Nevertheless, inductor-current ripple per phase is kept constant even if the number of phases is augmented.

A direct consequence of (3-1) is that the converter switching frequency is incremented proportionally with the number of phases as it is observed in (3.2). Therefore, multiphase converters work at an equivalent switching frequency of n-times (compared with a single-phase converter working at the same frequency

than one phase of the multiphase one). This is particularly interesting in our studied case since switching frequency of the multiphase converter can be increased without increasing switching losses in the active components of each phase. This skill of multiphase architectures is quite important because it allows reducing the values of the input and the output power converter filters, i.e. the global size of the embedded VR.

$$f_{sw\_MP} = f_{sw\_phase} \cdot n$$

with: f_{sw_MP} = Total switching frequency of the multiphase converter (3.2)

f_{sw_phase} = switching frequency of a phase

The number of phases is also an important criterion as regards EMI considerations. Actually, multiphase converters supply a more continuous input energy flux than single-phase ones. As a result, the harmonic content in the input current is reduced compared with the single-phase case as it is illustrated in [3.1] and [3.2] Moreover, main harmonics are placed at the fundamental switching frequency and their respective multiples as it is illustrated in Fig. 3-1. Obviously, the value of these harmonics depends on the duty cycle and the number of phase how it is disclosed in [3.3]

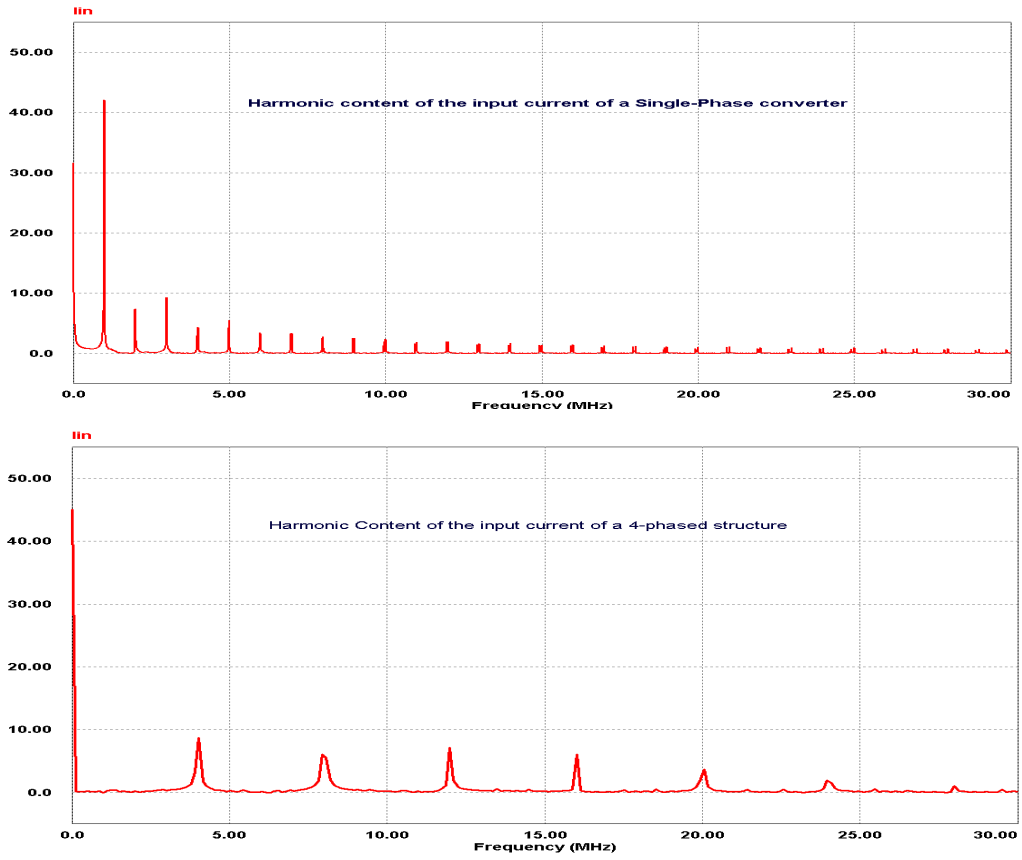


Fig. 3-1 Harmonic content of the input current in a Single-Phase Synchronous (top) and a 4-phased Buck converter (bottom)

Thus, a specific study to find the optimal number of phases for a VR working as power supply for embedded power microprocessors has been completed in [3.3] . Along this study, interleaved multiphase converters are compared with a single-phase example in order to establish a systematic comparison. The main discussion parameters were ripple values, EMI, losses, complexity (number of components and pins of a possible IC), costs and sizes. In short, architectures from 4 to 6-phased are the most indicated ones for this kind of power supplies with the current imposed power levels. A priori, to increase the number of phases is advantageous because better efficiencies and faster transient responses can be obtained. However, to increase the number of phases beyond six is not advantageous in terms of complexity, costs and performances. In spite of the study presented in [3.3] is not exhaustive, the systematic comparison presented in this work can be useful to discern the optimal number of phases in cases different than the presented one in this work.

3.4 Selection of passive components

3.4.1 Introduction

Passive components involving input and output filters should attenuate the switching noise produced by active devices. Accordingly, frequency is a limiting factor in the selection of passives elements. Actually, present technologies of passive components are not well-adapted for high-frequency working modes. In fact, they lose their intrinsic characteristics when they are forced to work to high switching-frequency power converters as it is detailed in next points. Nowadays, the high-frequency performances of passive components are an important frontier to increase the switching frequency of power converters

Traditionally, the value of passive components is chosen according to steady-state ripple requirements (low-ripple hypothesis) associated with size, price and efficiency considerations. Indeed, switching-frequency of the multiphase converter is selected taking into account maximal permitted switching losses and the size of passive elements. In VRs applications, load transient-states cause important deviations in the converter output voltage. As a result, to minimize these voltage droops and to obtain fast transient responses are essential for a proper VR working. In consequence, low-ripple hypothesis is not enough for a

correct calculation of the value of passives in PoLs and VRs applications. Thus, the following section gives basic equations to size correctly multiphase power converter passive elements.

These calculations are particularly interesting since an important reduction of input-current and output-voltage ripples is achieved if current distribution among phases is uniform due to the ripple cancellation factor [3.4] [3.6]

3.4.2 Output filter inductor

In typical inductors, core and conduction losses are incremented as long as frequency is increased. Then, core losses (P_{core}) depend on the material used to manufacture the inductance, e.g. ferrites own the lowest core losses. By the way, conduction losses are composed by the DCR (DC Resistance) and, in high-frequency working modes, by an additional term named ACR (AC Resistance).

The DCR is kept constant for the whole range of frequencies and its associated losses only vary according to RMS inductor current. In contrast, ACR (see Fig. 3-2) is composed by a series (R_2) and a parallel (R_3) resistors which depends on the square of the frequency. As a result, losses caused by the inductance can be decomposed as follows:

$$P_{ind} = \underbrace{P_{core}}_{dependant\ of\ frequency} + \overbrace{\underbrace{P_{ACR}}_{} + \underbrace{P_{DCR}}_{not\ dependant\ of\ frequency}}^{Conduction\ losses} \tag{3.3}$$

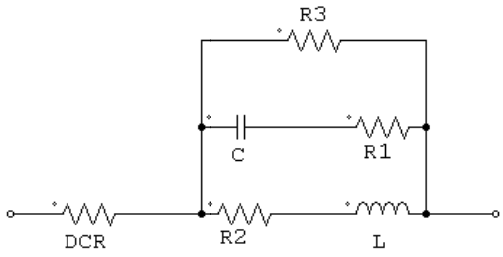


Fig 3-2 Commercial inductance model

In the Fig. 3-3, the parasitic resistance frequency behaviour of a typical commercial inductance used in VRs is measured using a precision impedance analyzer [3.7] . Thus, it can be observed how the value of the parasitic resistance at high frequency becomes not negligible.

In VRs applications, inductor value should provide low losses and fast transient responses. Therefore, a high inductance value enhances the power converter efficiency since its inductor-current ripple is minimized. However, transient response will be slower.

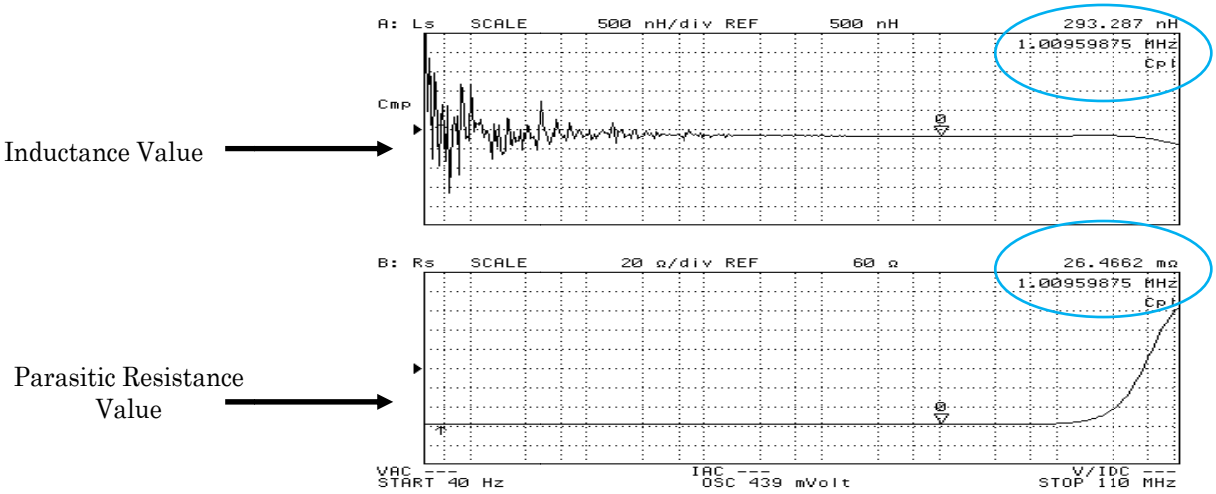


Fig 3-3 Frequency characterization of a commercial inductance using an impedance analyzer

Accordingly, multiphase converter are quite interesting in VRs applications since their effective (total) inductor value can be decreased as long as the number of phases is augmented as shown in (3.1). Hence, the inductance value per phase in multiphase architectures can be calculated as follows [3.8] :

$$L_{out\_phase} = \underbrace{\frac{V_{out}\cdot(1-D_{\min})}{\Delta I_{L\_\max}\cdot f_{sw}}}_{1^{st}\ term}\cdot\underbrace{\left(n\cdot\frac{\left(D_{\min}-\frac{m}{n}\right)\cdot\left(\frac{m+1}{n}-D_{\min}\right)}{D_{\min}\cdot(1-D_{\min})}\right)}_{2^{nd}\ term} \tag{3.4}$$

$$\text{with: } m = \text{floor}\left(\underbrace{n\bullet D_{\min}}_{k}\right)$$

$D_{\min}$ = minimal duty cycle

n = number of phases (3.5)

$\Delta I_{L\_\max}$ = maximal inductor current ripple

m = maximal integer not exceeding k

The first term of (3.4) is based on the classical maximal inductor-current ripple design. Nevertheless, (3.4) owns a second term which depends on the inductor-current ripple cancelation among phases. This ripple cancellation factor is zero for a given number of phases and a specific duty cycle ratio as it can be seen in the example of the Fig 3-4 for a 4-phased converter.

The value of the output inductor should be calculated depending on our design specifications. If fast responses are needed, inductor-current ripple should be as low as possible; then, inductance value per phase should be decreased according to the number of phases keeping the inductor-current ripple constant.

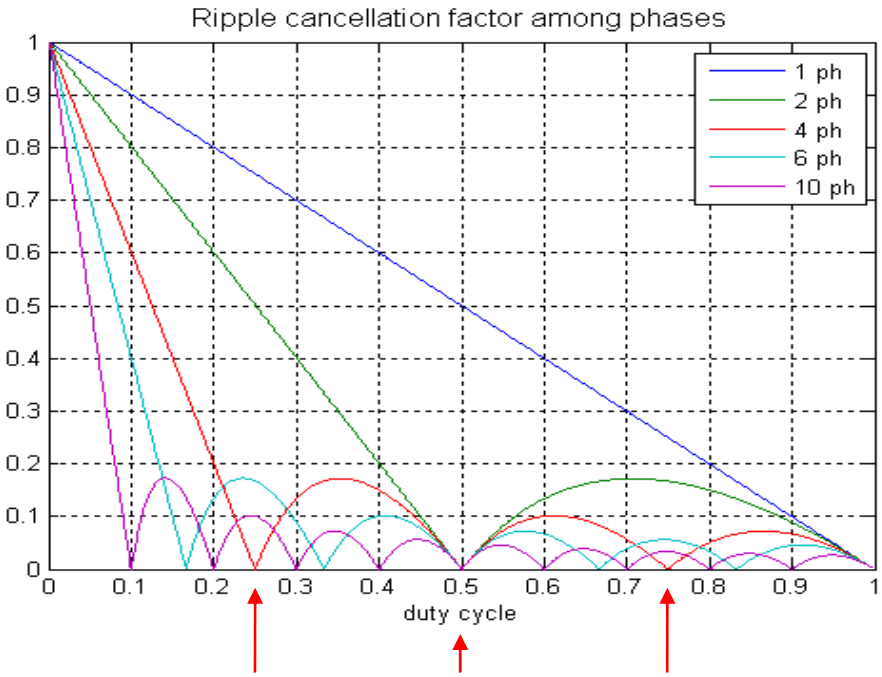


Fig. 3-4 Normalized ripple cancellation factor for a n-phased power converter depending on the duty cycle

On the other hand, the inductor-current ripple is reduced and the efficiency is improved keeping constant the inductor value per phase is spite of transient response is not improved in this case. This last effect can be observed in Fig. 3-5;

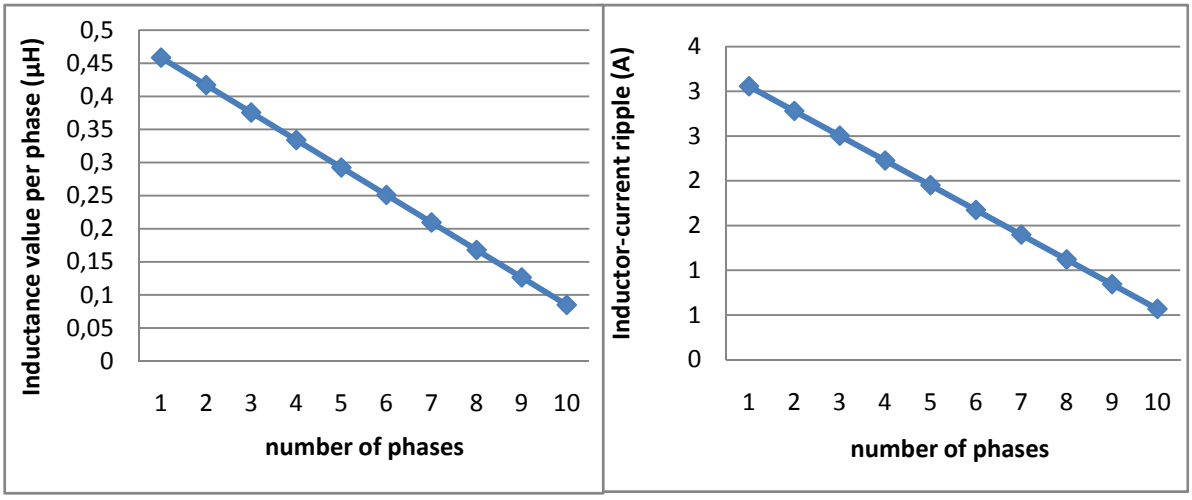


Fig. 3-5 Inductance value per phase for a fix value of inductor-current ripple (left) and inductor-current ripple per phase for a fix value of inductor (right).

Fig. 3-5 illustrates this later design trade-off. In the left side, the inductance is calculated depending on the number of phase and keeping constant the inductor-current ripple. In contrast, in the right side, the decrease of the inductor-current value per phase keeping constant the inductance value per phase depending on the number of phases is shown.

3.4.3 Output and input filter capacitor

At present days, the capacitor technology is an important limiting factor in the quest for higher switching-frequency in power converters. Nowadays, boundaries for electrolytic and tantalum (10µF, in this example) devices are around 300kHz and 1MHz respectively as it is illustrated in Fig. 3-6.

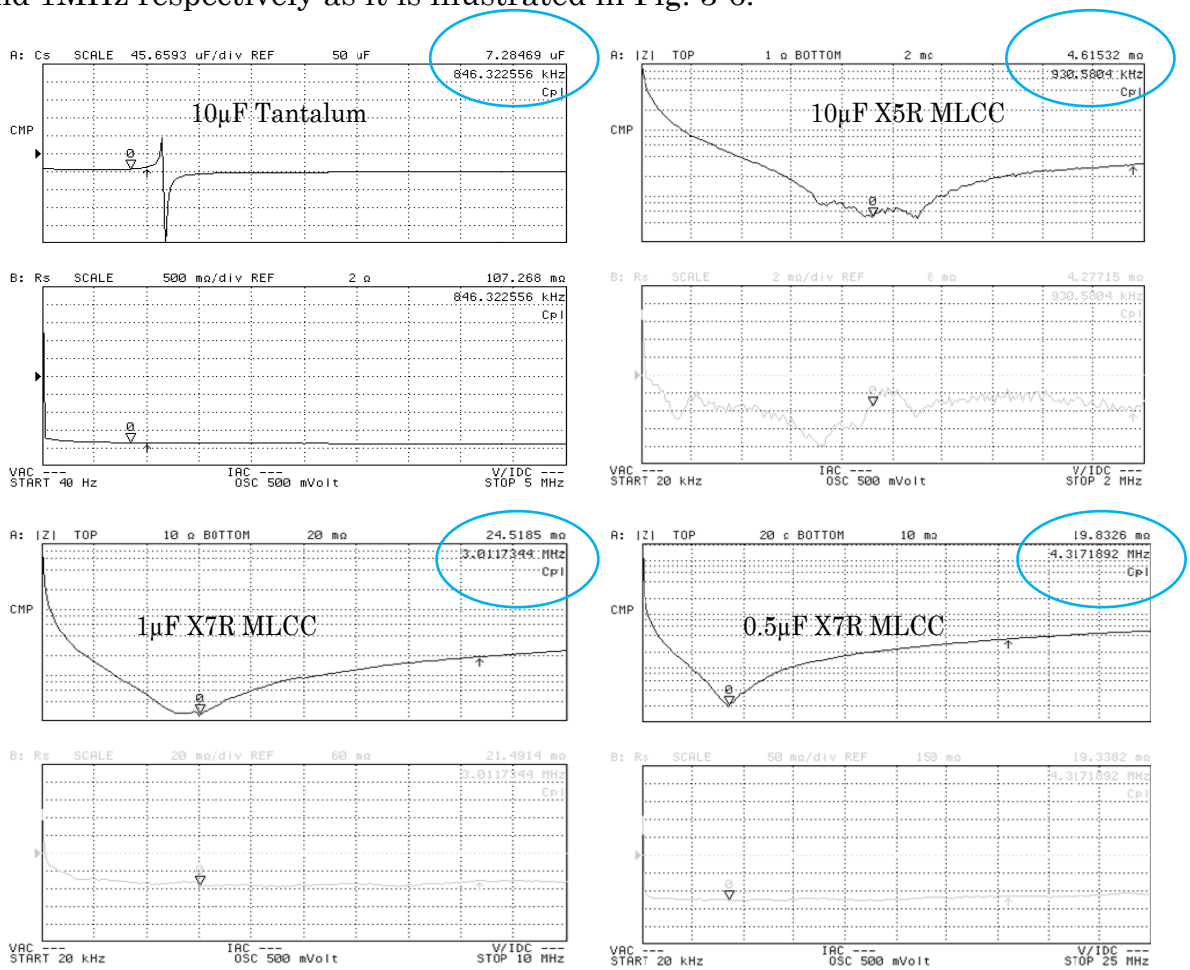


Fig 3-6 Frequency characterization using an impedance analyzer for different capacitor technologies: capacitor value (top) and ESR (top)

Indeed, ESR (Equivalent Series Resistance) resistance of tantalum capacitors is not negligible at this frequency ratio as shown in Fig. 3-4. As a consequence, the technology selected for high-frequency decoupling capacitors of the output filter must be only MultiLayer Ceramic (MLCC) one. This technology offers the largest

margin up to the resonance frequency and, also, acceptable values for the ESR.

For VRs applications, ESR must be as small as possible to reduce capacitor conduction losses as well as the voltage-droop produced by load variations. In fact, this droop is basically imposed by the product of ESR and the load current.

Moreover, the ESL (Equivalent Series Inductance) of the capacitor also imposes the first part of this voltage-droop. Thus, a small ESL is also required to obtain higher slew-rates (dI_{out}/dt) and to manage properly load variations.

Thus, the value of the output-filter decoupling capacitor should be based on the maximal output-voltage ripple consideration. As in the inductor case, the capacitor equation owns two terms. Hence, interleaved effects are present in the second term [3.9]

$$C_{out\_\min} = \underbrace{\frac{V_{out}\cdot\left(1-D_{\min}\right)\cdot T_{sw}^{2}}{8\cdot\Delta V_{out\_\max}\cdot L_{out\_phase}}}_{1^{st}\,term}\cdot\underbrace{\left(n\cdot\frac{\left(D_{\min}-\frac{m}{n}\right)\cdot\left(\frac{m+1}{n}-D_{\min}\right)}{D_{\min}\cdot\left(1-D_{\min}\right)}\right)}_{2^{nd}\,term} \tag{3.6}$$

In previous equation, the value of the output-filter capacitor depends on the number of phases as it can be observed in the second term of (3.6).

Fig 3.7 represents the capacitor value for a given number of phases (right) and for different duty cycles (left). It can be noted that this value can be fixed if inductor value per phase is reduced according to the number of phases (blue trace). On the other hand, using the same inductor value per phase, the value of this capacitor (green trace) can be reduced.

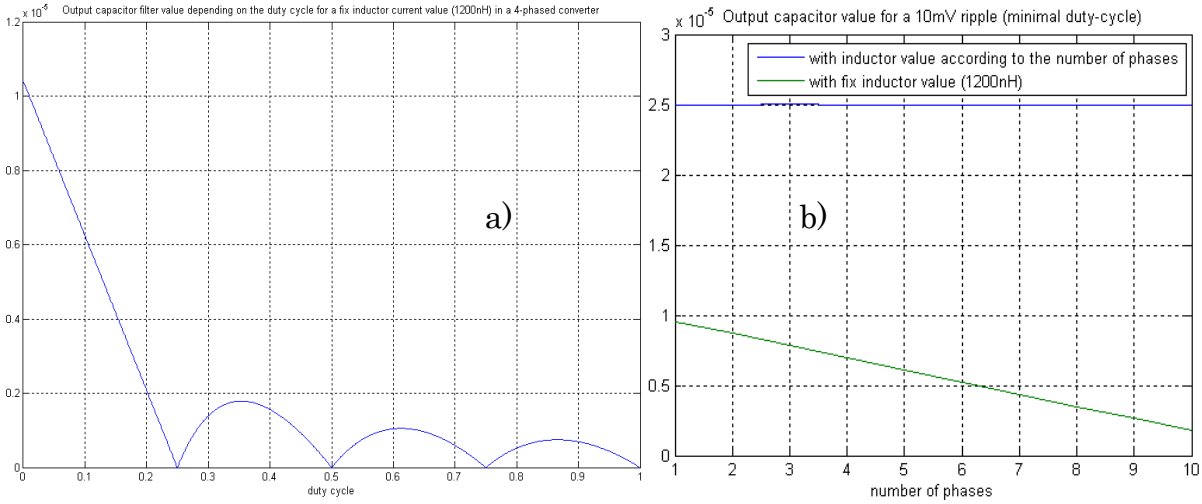


Fig. 3-7 Capacitor value per phase depending on: a) the duty cycle, b) the number of phases for a fix inductor value (green) and a phase depending value (blue).

This last characteristic allows decrease the final value of the output capacitor according to the number of phases and gives us an answer to solve frequency constraints in the selection of the capacitor technology. In consequence, a reduction of the final capacitor value involves a possible increase of the switching frequency of the power converter.

On the other hand, input-voltage ripple is reduced appreciably in multiphase converters thanks to their more constant input-energy flux. As a consequence, the input-capacitor value destined to smooth the input-voltage is reduced significantly compared to the single-phase case. The input-current value can be found with the following equation [3.5]

$$I_{IN\_rms}=\sqrt{\left(D_{\min}-\frac{m}{n}\right)\cdot\left(\frac{m+1}{n}-D_{\min}\right)\cdot I_{out\_max}^2+\frac{n}{12\cdot D_{\min}^2}\cdot\left(\frac{V_{out}\cdot(1-D_{\min})\cdot T_{sw}}{L_{out\_phase}}\right)^2\cdot(m+1)^2\cdot\left(D_{\min}-\frac{m}{n}\right)^3+m^2\cdot\left(\frac{m+1}{n}-D_{\min}\right)^3} \quad (3.7)$$

And the minimal input-capacitor can be calculated as follows:

$$C_{in\_\min}=\frac{0.5\cdot L_{out\_phase}\cdot I_{IN\_rms}}{\Delta V_{in\_\min}\cdot V_{in\_\min}} \quad (3.8)$$

3.5 Selection of active components

3.5.1 Introduction

In the synchronous Buck topology, both switches are traditionally N-channeled MOS transistors since they offer lower conduction resistances and manufacture prices as well as faster response times.

Active components are the biggest source of losses in DC/DC converters. That is why conduction time of both active devices and switching frequency limits should be considered in order to obtain an optimal commutation structure (MOS and their corresponding drivers) in terms of efficiency and rapidness.

In practical terms, there are two key parameters in the losses calculation of these active switches. Both parameters define the quality of the MOS in this kind of power supply applications. These parameters are the gate charge (Q_G) and the drain-to-source (R_{dsON}) or conduction resistance.

The product of both parameters defines the Figure Of Merit (FOM) of an active switch as shown in (3.9). Then, the lowest losses contribution of the active switches is obtained using devices with the lowest FOM possible.

$$FOM = Q_G \cdot R_{dsON} \tag{3.9}$$

Protections in high-current, high-frequency VRs are necessary due to the important voltage peaks produced by the switching behavior of the converter. The simplest solution is to limit the charge current arriving to the MOS gate by means of a gate resistance. However, this passive element limits the gate-charge slew-rate and cause some power dissipation, then, additional losses. Transient protection diodes should be used as it is illustrated in Fig. 3-8.

Thus, D1 is a zener diode protecting the gate from undesired noise peaks which can damage the MOS. The avalanche voltage (V_{br}) of this diode should be lower than the maximal gate-to-source voltage of the MOS. Moreover, D2 is a fast-diode and D3 is a zener diode. Both diodes can replace in industrial applications the source-to-drain parallel Schottky diode. The main advantage is that diodes can be smaller and cheaper than this parallel Schottky diode. By the away, D3 should own a V_{br} lower than the maximal drain-to-source voltage of the MOS.

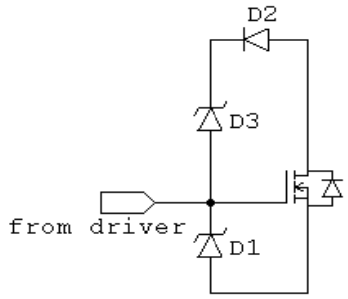


Fig 3-8 MOS Protections

In brief, the choice of both MOS in multiphase synchronous structures is a decisive factor to obtain good results in terms of efficiency and robustness. This selection procedure is described in next point.

3.5.2 Power switch selection

Switching losses are the main cause of power dissipation in the power switch or HSM (High-Side MOS) even in high-current applications. Thus, the Q_G of the HSM should be as small as possible to minimize the gate-charge time and to decrease switching losses as shown in Fig 3-9. Thus, switching losses starts when gate-to-source voltage (V_{GS}) is higher than the MOS threshold voltage (V_{GSth}).

In general, V_{GSth} should be high enough to avoid undesired spontaneous commutations caused by untimely noise peaks. However, it should not be very

high to assure fast switching modes. Once V_{GS} is higher than V_{GSth}, the MOS input capacity (C_{iss}) is charged and the drain current (I_D) grows linearly. As a result, C_{iss} should own low values to make easier faster commutations. When I_D reaches the desired value, drain-to-source voltage (V_{DS}) decreases almost linearly until it reaches zero value and, then, zero losses are obtained again. To sum up, switching losses process can be summarized as:

$$Psw_{HSM} = \left(\frac{V_{in} \cdot I_D}{2}\right) \cdot (t_2 - t_0) \cdot f_{sw} \tag{3.10}$$

Previous time intervals are defined in Fig. 3-9. Then, first time interval is the rising gate-current period and the second time corresponds to the falling one.

$$t_1 - t_0 = t_r = \frac{Q_{g\_tot}}{I_r} \tag{3.11}$$

$$t_2 - t_1 = t_f = \frac{Q_{g\_tot}}{I_f} \tag{3.12}$$

Where:

$$Q_{g\_tot} = Q_{gs2} + Q_{gd} \tag{3.13}$$

$$I_r = \frac{V_{dd} - V_{GSth}}{R_{d\_up} + R_g} \tag{3.14}$$

$$I_f = \frac{V_{GSth}}{R_{d\_dw} + R_g} \tag{3.15}$$

Q_{gs2}, Q_{gd}, R_g and R_{dup_dw} are typically provided by the MOS and driver manufacturers respectively. V_{gsth} can be also extracted from figures of V_{GS} depending on Q_G.

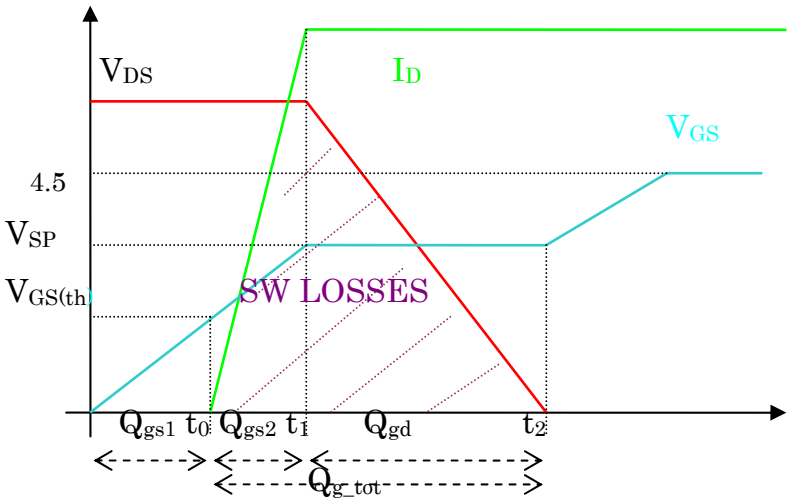


Fig 3-9 HSM Turn-on waveforms

Fig. 3-10 shows the influence of switching losses in a typical commutation cell (HSM, LSM, driver and inductor) with the values exposed in point 3.8.1. Despite of switching losses are dominating in HSM, other sort of losses like conduction (P_{cond}), gate (P_G) and output capacitance (P_{Coss}) losses should be considered. Hence, they are defined by:

$$P_{cond} = I_D^2 \cdot R_{dsON} \cdot D \tag{3.16}$$

$$P_G = Q_G \cdot f_{sw} \cdot V_{dd} \tag{3.17}$$

$$P_{Coss} = \frac{C_{oss} \cdot V_{in}^2 \cdot f_{sw}}{2} \tag{3.18}$$

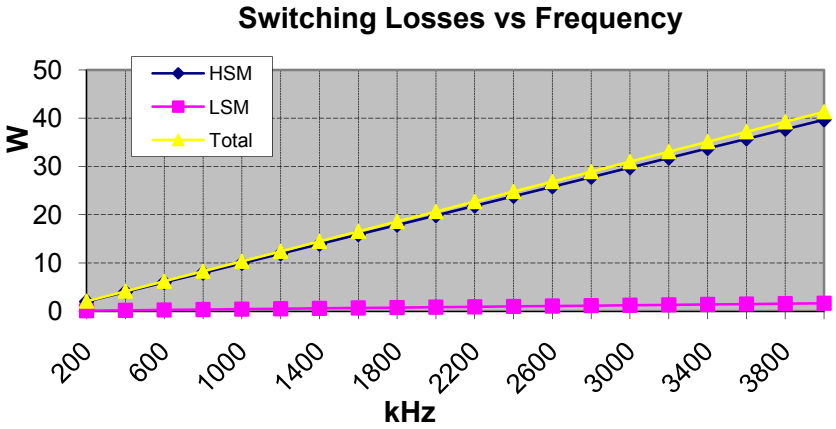


Fig. 3-10 Switching losses contribution in a commutation cell

LSM is also a source of losses which are reflected in the HSM contribution. These losses are produced by the current remaining in the LSM body-diode after the dead-time. Thus, some residual energy remains still on this diode when HSM is turned ON. Afterwards, HSM needs a supplementary current to remove this stored charge producing some extra losses. This undesired effect can be minimized using a Schottky diode specially adapted to low-voltage applications placed in parallel with the LSM. This diode should be fast enough to reduce the recovery time. Moreover, it should own a lower forward voltage than the one of the LSM to minimize these losses. It is important to note that this diode contributes to LSM and HSM losses as it is disclosed in next point. Thus, the addition of a fast Schottky diode can improve considerably the converter efficiency. The effect of this reverse recovery losses can be quantified as follows:

$$P_{rr} = Q_G \cdot V_{dd} \cdot f_{sw} \tag{3.19}$$

3.5.3 Synchronous switch selection

In steady-state, LSM is on conduction the most part of the switching period. In consequence, to minimize its R_{dsON} is essential since the foremost losses contribution is given by conduction ones. Thus, these losses are defined by:

$$P_{cond} = I_D^2 \cdot R_{dsON} \cdot (1 - D) \tag{3.20}$$

In second instance, dead-time losses should be also considered. These losses are produced when both MOS are OFF and the LMS is going to start its conduction period. Thus, this dead-time delay is composed by two time intervals. First one is used by the driver to avoid both MOS simultaneous conduction. After this period, LSM gate is charged during a second interval. These losses can be summarized as:

$$P_{deadtime} = t_{deadtime} \cdot f_{sw} \cdot V_F \cdot I_D \tag{3.21}$$

Where V_F is the diode-droop voltage and:

$$t_{deadtime} = t_{deadtime(R)} + t_{deadtime(F)} \tag{3.22}$$

$t_{deadtime(R)}$ and $t_{deadtime(F)}$ are variable depending on the driver chosen and their estimate values are:

$$t_{deadtime(F)} = t_{delay} + t_{TH} \tag{3.23}$$

$$t_{deadtime(R)} \approx t_{delay} \tag{3.24}$$

$$t_{TH} = \frac{Q_{gs1}}{I_{dr}} \tag{3.25}$$

$$I_{dr} = \frac{V_{dd} - (V_{GSth} / 2)}{R_G + R_d} \tag{3.26}$$

3.6 Cooling system.

In traditional VRs, thermal management was achieved by means of aluminum or cooper heat-sinks associated to fans. These cooling systems take a lot of place and power. An additional drawback is the required thermal conductive pad or gel in-between the heat-sink and the VR. As a result, this system becomes expensive and quite complex. In embedded applications, the CPU fan is used to cool the VR module. Hence, the VR only receives some residual airflow. For instance, a classical CPU fan delivers a 2m/s airflow approximately (400 LFM, Linear Feet per Minute). In numerous desktop applications, 0.75 – 1m/s airflows (150-200

LFM) is an accepted range for VRs cooling. Note that airflows greater than 1m/s may produce some acoustic noise. Modern VRs use low-electrical conductivity liquids as cooling system. This cooling method is based on the heat exchange among the cooling liquid, the different elements of the motherboard and the air. As a result, if the liquid system is well isolated, this cooling system becomes quite efficient in spite of it should be refilled with regular periodicity due to the liquid evaporation.

In practical terms, the switching devices of the commutation cell (active elements and switch driver) of our power converter should be cooled to avoid thermal problems as it is shown in Fig. 3-11. In this thermal image, the hotspots (in red) of the commutation-cell corresponding to a multiphase converter and, therefore, the critical places that are needed to cool can be detected clearly.

These hotspots depend on the steady-state duty cycle (D) and it can be observed how heat distribution changes considerably according to this last parameter. As a result, HSM (IRF3715) is affected mainly by switching losses and LSM (IRF6609) by conduction ones for low duty cycles. As long as the duty cycle is augmented, losses distribution is changed. In our study case, HSM is not featured to work with very high duty cycles since it is optimized for obtaining fast commutations due to its low Q_G.

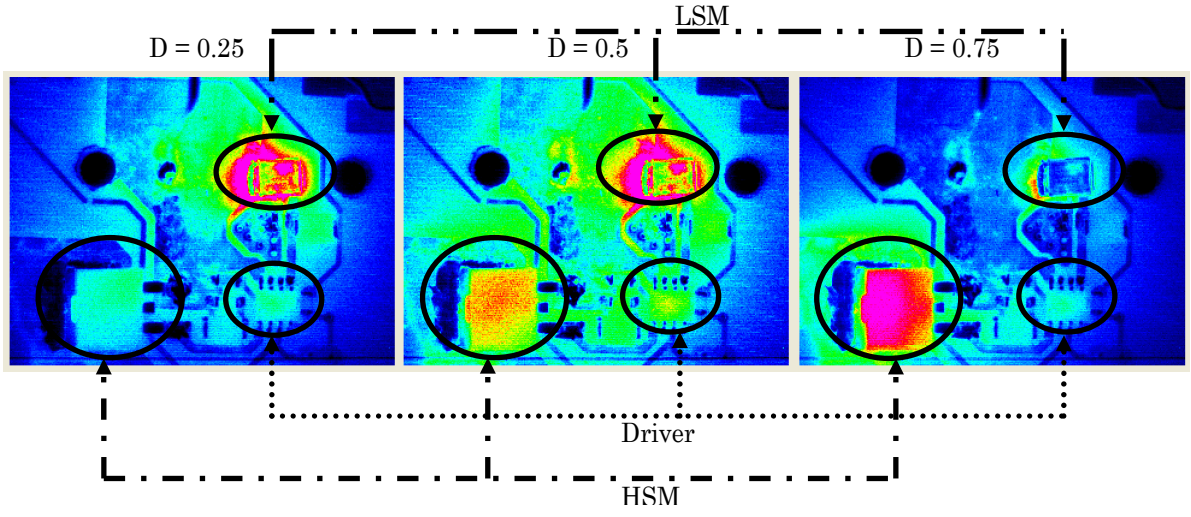


Fig 3-11 Thermal image of the driver and active devices of a typical multiphase converter commutation cell working at 10A/phase and 1MHz/phase

In short, long ON-time HSM operation modes may cause important conduction losses due to R_{ds_ON} is not normally minimized in this active device. In consequence, HSM is the main heat contribution for duty cycles higher than 0.5.

To sum up, a heat-sink and a fan are needed to cool these devices. Thus, the heat-sink should own a low ambient-to-junction thermal resistance (θ_{ja}) for a better power dissipation. Moreover, the junction temperature (T_j) of the device to cool should be lower than a maximal value specified by the manufacturer. This T_j corresponds to:

$$T_j = T_a + P_{dis} \cdot (\underbrace{\theta_{jc} + \underbrace{\theta_{cs} + \theta_{sa}}_{\theta_{ca}}}_{\theta_{ja}}) \tag{3.27}$$

With: T_a= ambient temperature (25° normally), P_{dis}= dissipated power by the device in W, θ_{jc} = junction-to-case thermal resistance in °C/W, θ_{cs} = case-to-sink thermal resistance in °C/W, θ_{sa} = sink-to- ambient thermal resistance in °C/W and θ_{ca} = case-to-ambient thermal resistance in °C/W.

The maximal thermal resistance, $\theta_{ca,}$ which the IC package is able to resist, has been calculated in Table 3-2 where a practical example of heat dissipation in two typical packages used in active devices for VRs [2.6] is exposed. Once the maximal heat-sink θ_{ca} is found, its required surface can be calculated. As a general rule, the lower θca, the larger heat-sink surface required.

Package / Calculations	DirectFET		DPAK	
	HSM IRF6612	LSM IRF6609	HSM IRF3715	LSM IRF3711
T_j (max)	150°C		175°C	
P_{dis} (max)	3.03W	3.13W	2.94W	7.09W
θ_{jc}	1.4°C/W		3.3°C/W	
$\theta_{ja} = \frac{\Delta T}{Pdis}$ (3.28)	$\theta_{ja} < 41.2°C/W$	$\theta_{ja} < 39.9°C/W$	$\theta_{ja} < 51.0°C/W$	$\theta_{ja} < 21.1°C/W$
$\theta_{ca} \le \theta_{ja} - \theta_{jc}$ (3.29)	$\theta_{ca} < 39.8°C/W$	$\theta_{ja} < 38.5°C/W$	$\theta_{ca} < 47.7°C/W$	$\theta_{ca} < 17.8°C/W$

Table 3-2 Heatsink sizing design guidelines

3.7 Current Sense

3.7.1 Introduction

Current tracking is an important topic in the control of DC/DC converters. As a matter of fact, the quality of a current-mode controlled converter depends strongly the accuracy of the current sensor and its adaptation stage. This issue is

particularly important in multiphase VRs applications where high switching frequencies and high output-current values are required. Therefore, an accurate inductor current sense is fundamental for a fine regulation of our converter.

Classically, current sense was obtained thanks to a shunt resistor placed in series with the inductor. This method lets to obtain an accurate voltage image of the inductor current (although accuracy was linked to the shunt resistor tolerance and its non-inductive behaviour). However, this technique is not recommended for high-current VRs due to their significant conduction losses. For instance, considering a Buck converter providing 30A and a shunt resistor of 2.5mΩ, losses can induce a 7.5% droop in their nominal efficiency.

Sensorless techniques try to solve these losses problem. For example, in [3.10] [3.12] several techniques are proposed where authors replace the inductor-current measurement by software current-observers. These techniques avoid problems associated to losses, frequency and differential measurements. Nevertheless, others problems associated to the choice of the converter and observer models are present since both models must be sufficiently accurate to get a reliable regulation.

Another alternative are lossless techniques. They offer good accuracies without compromising the efficiency in modern VRs. First lossless technique was proposed in [3.13] In this work, authors achieve current-sense through the inductor DCR. In spite of it is a very easy concept, tolerances of the components and the influence of the frequency and the temperature in the DCR may cause considerable errors reducing significantly the accuracy.

Another lossless technique is based on sensing the current circulating through the LSM in synchronous topologies [3.14] . This current is measured when the LSM is on conduction taking advantage of its R_{dsON}. However, this technique was proved to be more complicated than previous ones due to the pulsating behaviour of the MOS. On one hand, the reduced accuracy due to the influence of the temperature in the R_{dsON} is an additional drawback. On the other hand, the R_{dsON} value is not exactly known since typical and maximal values are usually given in commercial datasheets. Finally, R_{dsON} depends on the V_{GS} applied and the V_{DS}. In consequence, tolerances in these magnitudes may origin huge errors causing very poor accuracy.

Therefore, state-of-the-art PWM commercial controllers for VRs applications employ another lossless technique in order to achieve a trade-off between efficiency and accuracy. This sensing method is called "Inductor DCR current sense" [3.16] . The main advantage of this lossless technique is a better accuracy than previous methods as it is described in next points.

3.7.2 The Inductor DCR current-sense technique

3.7.2.1 Working principle

This lossless technique can be seen like a current hardware observer placed in parallel to the inductor. This current observer is composed by a RC filter structure as shown in Fig. 3-12. Then, the main idea is to recover a differential voltage image around the filter capacitor which is directly proportional to the inductor current. Next figure shows the current sense chain placed in parallel to the output inductor of a Buck converter:

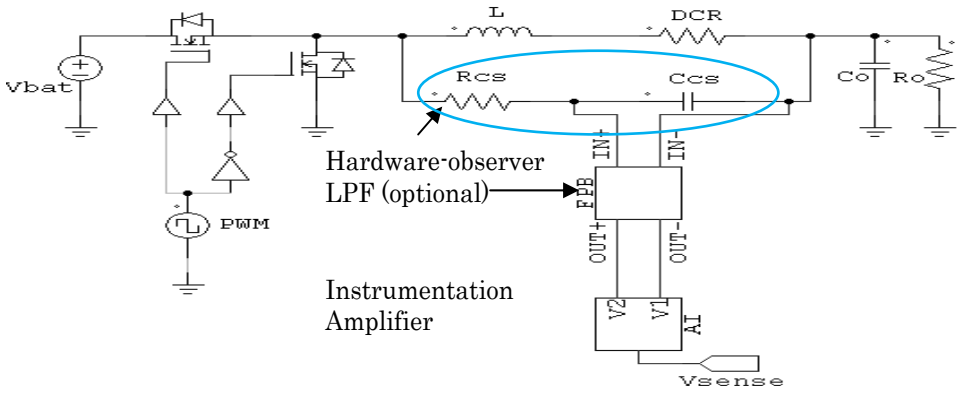


Fig 3-12 Synchronous Buck converter with inductor DCR current sense circuit

Hence, the transfer function of the current sensor is:

$$Vc(s) = DCR \cdot I_L(s) \cdot \left(\frac{1 + \frac{sL}{DCR}}{1 + s \bullet C_{cs} \bullet R_{cs}} \right) \tag{3.30}$$

To obtain a linear voltage image of the inductor current (see Fig, 3-9a), both time constants should be perfectly matched as follows:

$$\frac{Vc(s)}{I_L(s)} = DCR \quad \text{if} \quad \frac{L}{DCR} = C_{cs} \cdot R_{cs} \tag{3.31}$$

3.7.2.2 Effects of the temperature

Temperature changes may affect the accuracy of the current sensor since the DCR value is modified at a rate of ±0.39%/°C (i.e. ±3900ppm/°C). This coefficient corresponds to the cooper temperature factor modifying the expression (3.31).

Then, if temperature increases, DCR values will be also greater obtaining the case presented in Fig. 3-9b. This means that system works as a low-pass filter. As a result, only average inductor current values can be obtained but the inductor ripple is not gathered. Another consequence is that bandwidth of the filter is reduced obtaining slower systems and introducing and extra delay to the system.

On the contrary, if temperature decreases, system will work as a high-pass filter. This case involves worse consequences than the previous one because inductor-current average value may not be detected. In fact, AC ripple value is recovered only being useless to track the full inductor current. Moreover, high-frequency current-peaks may perturb the system behavior. To solve this problem and to minimize the temperature effects, a compensation circuit using a PTC can be placed near the inductor balancing the ±0.39%/°C variation of the DCR obtaining cases a) or b) of Fig. 3-13 [3.16]

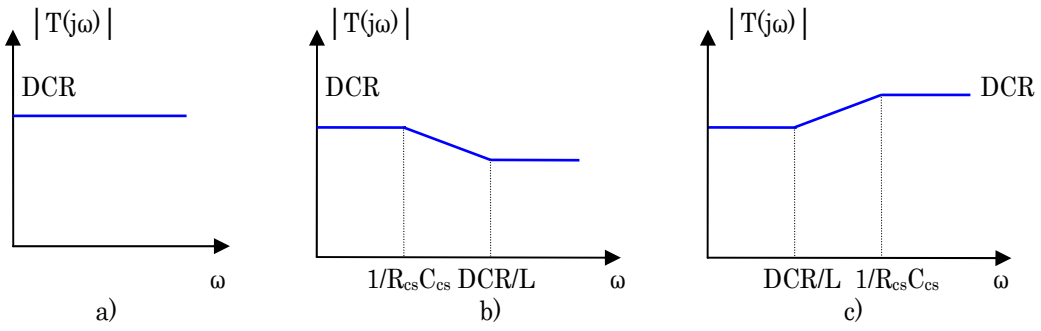
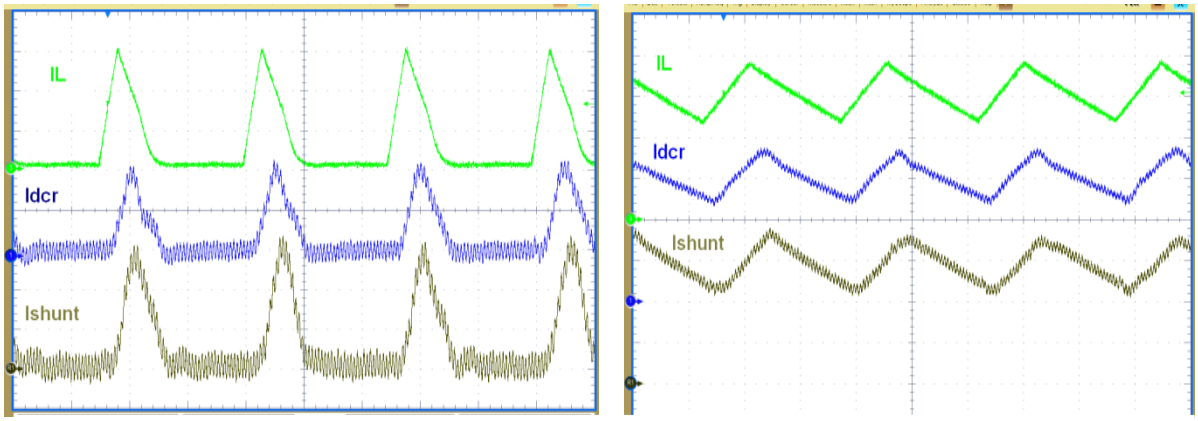


Fig. 3-13 Magnitude Bode Plots of the current-sense circuit for different DCR values

3.7.2.3 Experimental examples.

Some experimental results obtained using the DCR Inductor current sense tecnique are illustrated in this point. First example is implemented in a single-phase synchronous Buck converter commercialized and optimized for portable applications powered from 1-cell Li-ion batteries giving a maximal output-current of 400mA. In this graphic, the real current measurement made by a current scope (green) and the voltage image obtained using the Inductor DCR technique (blue)

and a shunt resistor (grey) for DCM and CCM modes (see Fig.3-14) are compared.



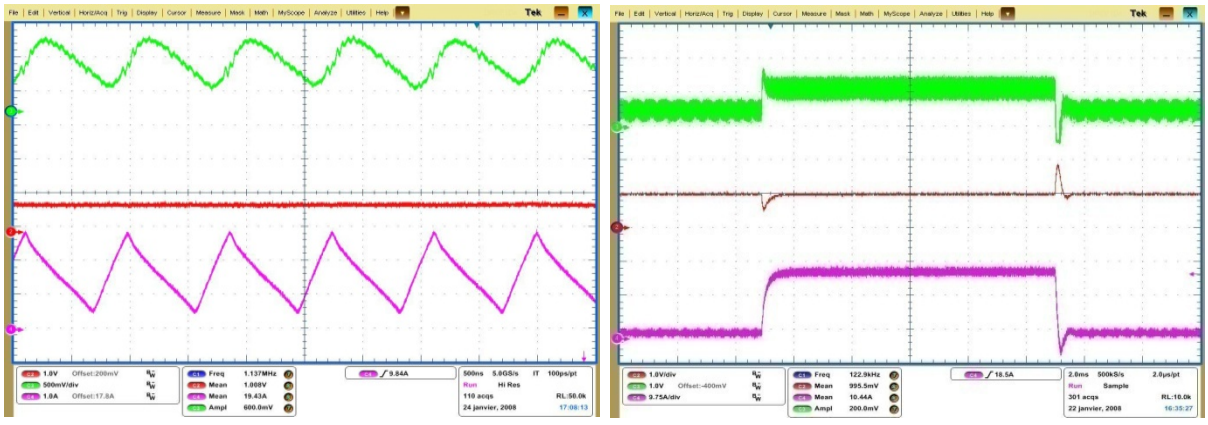
I_L 20mA/div, I_{dcr} 50mV/div, I_{shunt} 20mV/div
DCM

I_L 100mA/div, I_{dcr} 200mV/div, I_{shunt} 100mV/div
CCM

500ns/div

Fig. 3-14 Low.current Inductor DCR current sense example

Next example is conceived for PoL converters oriented to medium-current applications (up to 20A). Then, Fig. 3-15 shows its static behavior in the left side and the dynamical behavior of the current-sensor face a load variation of 10A in the right side. In this graphic, the output voltage (red) is obtained using a digital current-mode controlled as it will be explained in next chapters. Then, the real current measurement is shown in pink and the voltage image obtained using the Inductor DCR technique is illustrated in green.



I_{dcr} 500mV/div, V_{out} 1V/div I_L 1A/div,
Static mode

I_{dcr} 500mV/div, V_{out} 1V/div I_L 10A/div,
Dynamic mode with ΔI_{out}=10A

500ns/div

Fig. 3-15 Medium.current Inductor DCR current sense example

Last example is shown in Fig. 3-16 is obtained using an interleaved 4-phased converter with the specifications shown in Table 3.1. In this last scope, the real inductor currents are shown in the top side and in the bottom one, their

respective voltage images are illustrated. More information about all these experimental tests can be found in [3.17] [3.18] .

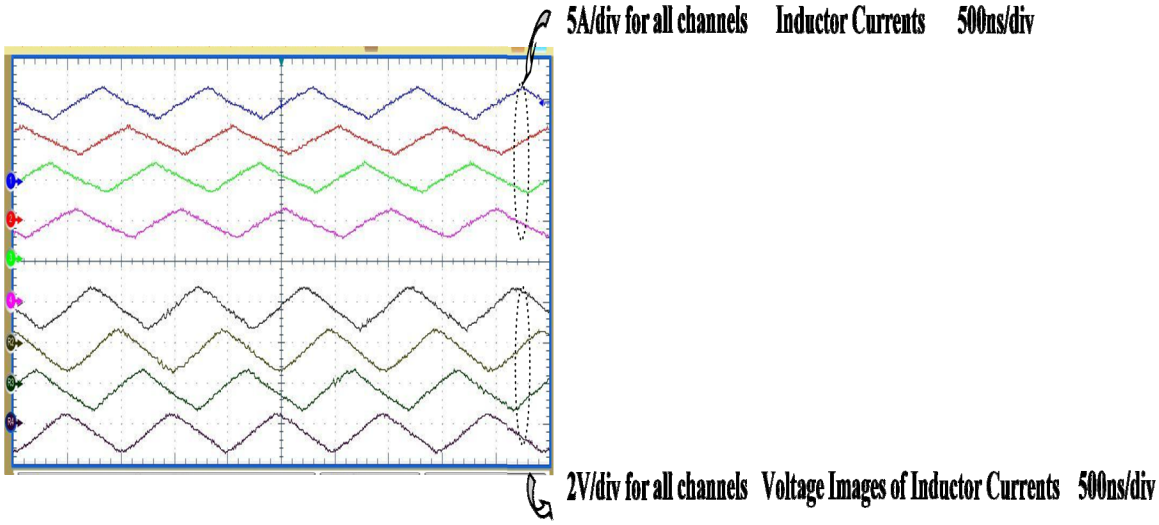


Fig. 3-16 Inductor DCR current sense example in an interleaved converter

3.8 Power converter sizing

3.8.1 First experimental prototype.

The technical specifications for this power converter are exposed in [5.1] and summarized in Table 5-1. These power requirements are oriented to supply embedded microprocessors of laptop computers. In particular, supply specifications are focused on the Dual-Core Intel Xeon® processor. Therefore, the value of the elements involving this power stage is calculated using the guidelines exposed in points 3.4.2 and 3.4.3 and summarized in Table 3-3. Nevertheless, the value of bulk capacitors has not been found in chapter because it is proposed in [5.1] .

Losses	HSM (W)	LSM (W)	Total (W)
Conduction	0.52	0.73	1.25
Switching	1.29	0.62	1.90
Gate	0.06	---	0.06
Output Capacitor	0.02	---	0.02
Reverse Recovery	0.03	---	0.03
Deadtime	---	1.08	1.08
DCR	---	---	0.47
Total			4.81

Table 3-3 Values of the components for the power stage of first prototype

Losses distribution per type and per device in this power stage is calculated thanks to equations given in point 3.5 and shown in Table 3-4 and Fig. 3-17.

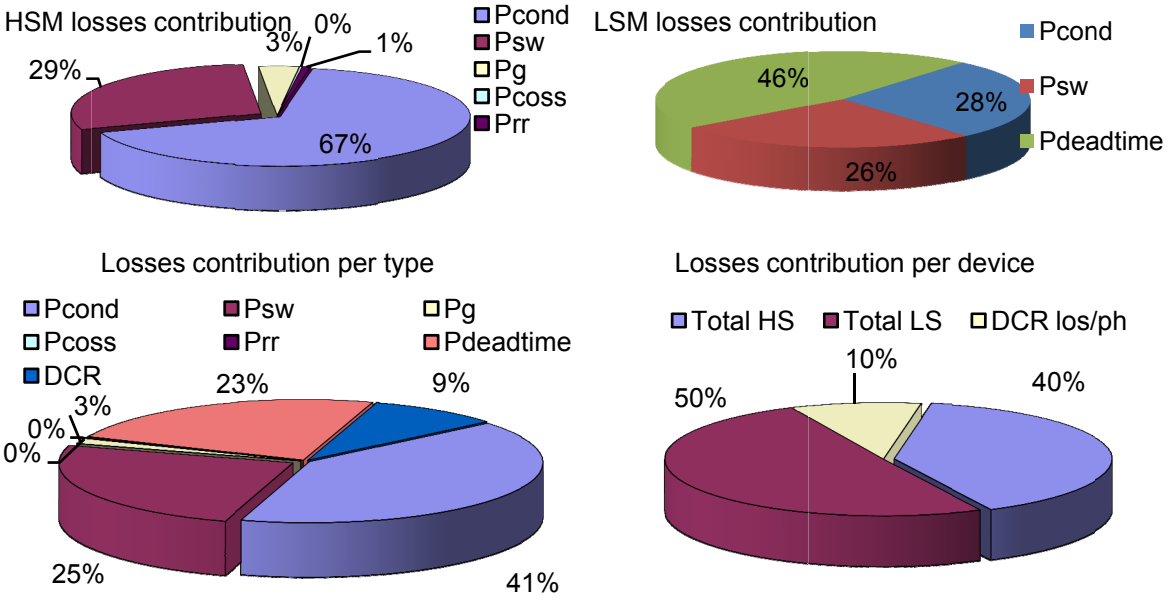


Fig. 3-17 Theoretical losses distribution in the power stage of the first prototype

Parameter	Val.	Parameter	Val.	Parameter	Val.	Parameter	Val.
MLCC Output Capacitor (C_{out_MLCC})	80µF (used) 38µF (3.6)	MLCC Output Capacitor ESR (ESR_{out_MLCC})	0.8mΩ	Bulk Output Capacitor (C_{out_Pol})	1530µF	Bulk Output Capacitor ESR (ESR_{out_Pol})	6.85mΩ
MLCC Input Capacitor (C_{in_MLCC})	80µF	MLCC Input Capacitor ESR (ESR_{in_MLCC})	0.8mΩ	Bulk Input Capacitor (C_{in_Pol})	660µF	Bulk Input Capacitor ESR (ESR_{out_Pol})	8mΩ
Output Induct. (L_{out})	300nH (used) 458nH (3.4)	Output Inductance Serial Resistance (DCR, R_L in Fig. 5-1)	0.6mΩ	HSM	IRL3715 [3.19]	LSM	IRF6609 [3.19]
R_{cs}	10kΩ (var.)	C_{cs}	100nF	Instrum. Amp.	Burr-Brown INA103 [3.21]		

Table 3-4 Theoretical maxinal losses contribution in the power stage of the first prototype (V_{in}=12V and I_{out}=20A)

Fig. 3-18 shows a comparison of the efficiency of our theoretical and experimental prototypes revealing a good matching between them.

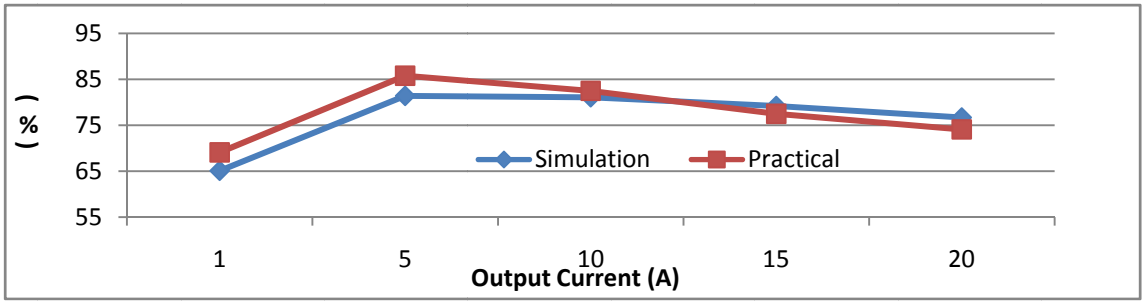


Fig. 3-18 Comparison of the theoretical and practical efficiency in the power stage of the first prototype of VR made in the LAAS (V_{in}=5V)

Finally, the power stage for this first power prototype is shown in Fig. 3-19

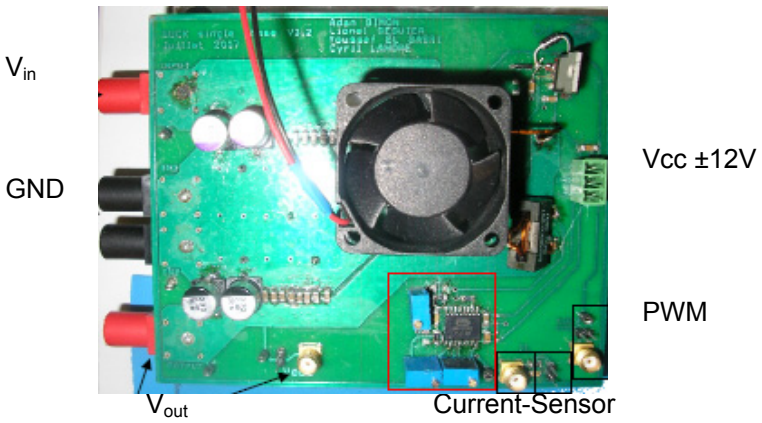


Fig. 3-19 Power stage for the first experimental single-phase prototype

3.8.2 Second experimental prototype.

Once more, the technical specifications are exposed in [5.1] and summarized in former Table 5-1 with the difference that now the maximal supply current delivered to the load is 36A. This increase of the power converter output current permits supplying whichever embedded laptop microprocessors exposed in [5.1] Thus, the values for the components of this second experimental prototype are summarized in Table 3-5 and illustrated in Fig. 3-20.

Parameter	Val.	Parameter	Val.	Parameter	Val.	Parameter	Val.
MLCC Output Capacitor (C_{out_MLCC})	80µF (used) 38µF (3.6)	MLCC Output Capacitor ESR (ESR_{out_MLCC})	0.8mΩ	Bulk Output Capacitor (C_{out_Pol})	2400µF	Bulk Output Capacitor ESR (ESR_{out_Pol})	6mΩ
MLCC Input Capacitor (C_{in_MLCC})	80µF	MLCC Input Capacitor ESR (ESR_{in_MLCC})	0.8mΩ	Bulk Input Capacitor (C_{in_Pol})	990µF	Bulk Input Capacitor ESR (ESR_{out_Pol})	5.3mΩ
Output Induct. (L_{out})	300nH (used) 458nH (3.4)	Output Inductance Serial Resistance (DCR)	0.6mΩ	HSM & LSM	IP2003A [3.22]		
R_{cs}	10kΩ (var.)	C_{cs}	100nF	Instrum. Amp.	Burr-Brown INA103 [3.21]		

Table 3-5 Values of the components for the power stage of the second prototype

Finally, the experimental efficiency of this power stage is shown in Fig. 3-21 where an improvement of the efficiency can be note compared with the previous power stage.

Fig. 3-20 Power stage for the second experimental single-phase prototype

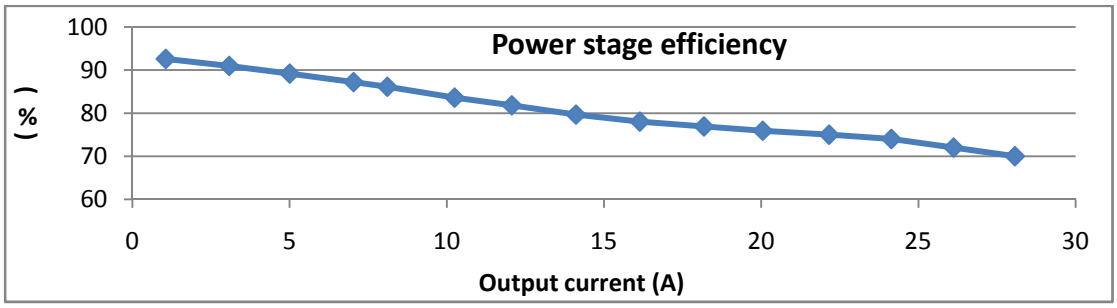


Fig. 3-21 Experimental losses distribution in the power stage of the second prptotype of VR made in the LAAS (V_{in}=5V)

3.8.3 Multiphase experimental prototype.

Out last experimental prototype is based on a 4-phased power converter and it is shown in Fig. 3-22. The same technology than in the previous single-phase case has been used in order to complete this experimental prototype [3.22]

Parameter	Val.	Parameter	Val.	Parameter	Val.	Parameter	Val.
MLCC Output Capacitor (C_{out_MLCC})	8 µF (used) 6.9µF (3.6) 10µF max.	MLCC Output Capacitor ESR (ESR_{out_MLCC})	1.2mΩ	Bulk Output Capacitor (C_{out_Pol})	2400µF	Bulk Output Capacitor ESR (ESR_{out_Pol})	6mΩ
MLCC Input Capacitor (C_{in_MLCC})	80µF	MLCC Input Capacitor ESR (ESR_{in_MLCC})	0.8mΩ	Bulk Input Capacitor (C_{in_Pol})	990µF	Bulk Input Capacitor ESR (ESR_{out_Pol})	5.3mΩ
Output Induct. (L_{out})	300nH (used) 334nH (3.4)	Output Inductance Serial Resistance (DCR)	0.6mΩ	HSM & LSM	IP2003A [3.22]		
R_{cs}	10kΩ (var.)	C_{cs}	100nF	Instrum. Amp	Burr-Brown INA103 [3.22]		

Table 3-6 Values of the components for the power stage of the third prototype

Thus, the technical specifications have been established in [2.1] and summarized in Table 3-1. It is worthy to note that phases should be placed symmetrically to avoid different propagation times among them.

Therefore, the values for this multiphase power stage are given in Table 3-4 and they have been calculated using the equations previously disclosed.

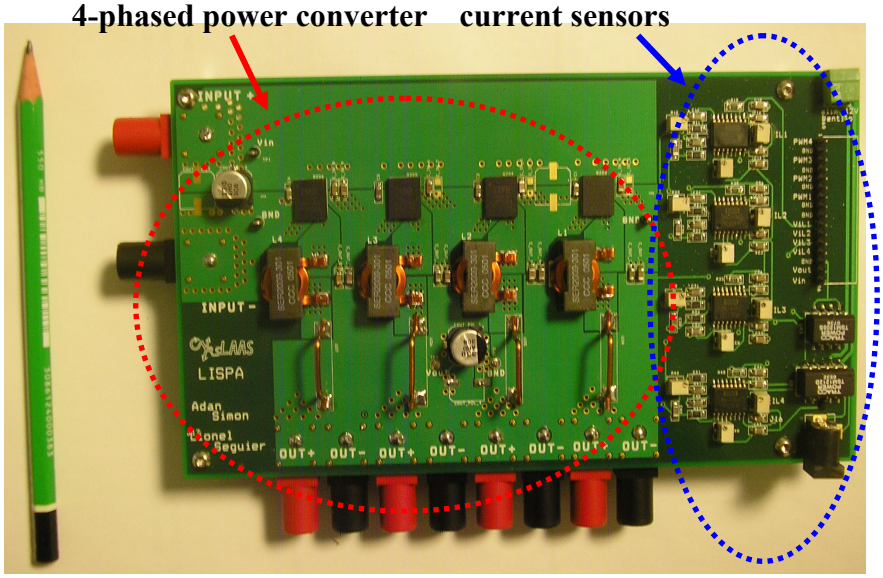


Fig. 3-22 Power stage for the multiphase experimental prototype

3.9 Conclusion

Voltage Regulators are not classical DC/DC power converter since they require explicit design specifications. Actually, the sizing of its main components cannot be made using classical methods, i.e. the low-ripple hypothesis is not enough to calculate correctly the output-filter passive devices.

In response to these specific requirements, the theoretical calculation of the devices involving a high-frequency, high-current and low-voltage VR has been disclosed giving some examples of how to calculate the power stage for a single and a multiphase synchronous Buck power converter. The calculation of these elements has been made in order to accomplish the supply power specifications imposed by main manufacturers of embedded laptop and desktop µps. In relation to multiphase converters, ripple cancellation effect among phases plays an important role in the sizing of this type of architectures since this cancellation factor is maximal for a given number of phases and duty-cycle.

Moreover, the main source of losses of these power stages has been estimated in order to obtain an accurate forecast of their efficiency. Along this point, critical

parameters like the gate charge of HSM and the drain-to-source resistance of the LSM should be optimized to improve the power converter efficiency.

On account of thermal management, the importance of dissipating the heat of active devices as well as the switch driver to enlarge the life of the converter has been discussed.

In addition, the optimal number of phases for a typical multiphase VR application oriented to supply embedded μps has been studied proving that 4, 5 and 6-phased structures give us the best trade-off among efficiency, complexity, ripple values, harmonic content and cost.

In keeping with the power converter inductor-current tracking, different ways to sense the inductor current have been disclosed. As a result, the lossless "Inductor DCR current-sense" technique has been studied in detail since it seems the most interesting candidate for VR applications. The feasibility of this technique with some high-frequency VRs examples has been illustrated in a wide margin of loads, i.e. since very-small load currents until those quite high. Furthermore, this technique has been verified in a real multiphase converter.

Current tracking is a critical point in current-mode controlled converters since the knowledge of the inductor current is a crucial point to obtain an accurate regulation and also to obtain an equilibrated current distribution among phases.

Thus, the next chapter is focused on the theoretical study of digital control laws for VR applications. These laws are applied in the experimental prototypes disclosed in chapter 5.

Chapter 4

Analysis Of Digital Control Laws For Voltage Regulators

4. Analysis Of Digital Control Laws For Voltage Regulators

4.1 Introduction

Digital regulation in VRs is obtained classically using Voltage-Mode Control due to its easy implementation. In addition, Current-Sharing (CS) techniques are required to obtain a uniform current distribution among converter phases in multiphase architectures. Thus, our aim is to design several performing control laws for VR systems. For that matter, different control techniques used in this kind of applications have been studied. In return, a systematic design method based on simulation models has been developed. These theoretical and simulation models allow us to evaluate our algorithms before to be implemented in the final digital controller using the same work conditions than in the real case. As a result, these algorithms can be applied in single and multiphase structures with minor differences in their final implementation.

As it has been commented previously, multiphase topologies need specific CS loops for a proper work. Therefore, a theoretical study of the most widespread techniques to achieve uniform power distribution is disclosed along this chapter.

Nevertheless, before to model these digital control laws, the small-signal model of the desired power converter should be obtained. This step is necessary to design correctly the digital filter of the feedback loop. According to last conclusion, the continuous-time and discrete-time small-signal models of the power converter are formulated in next section.

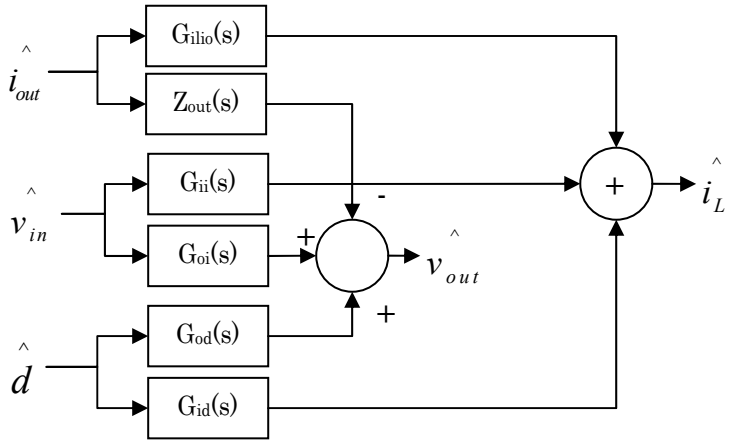
4.2 Small-Signal Analysis of the Power Converter.

4.2.1 Introduction

The open-loop small-signal behaviour of a PWM-controlled DC/DC converter can be described by a set of six transfer functions (see Table 4-1) which defines source, load and control disturbances effects as it is illustrated in Fig. 4-1.

In general, these transfer functions are useful up to the Nyquist frequency (half of switching frequency).

There are several ways to find this set of transfer functions for PWM-controlled converters. First method is based on the application of the Kirchoff laws and the energy-conservation method where non-linear elements are replaced with their corresponding averaged models as shown in Fig. 4-2 [4.1] . The main drawback of this method is that averaged models are only approximated for some elements like switches, then; ripple effects are not taken into account.



$$\begin{pmatrix} \hat{i}_L \\ \hat{v}_{out} \end{pmatrix} = \begin{pmatrix} G_{ii} & G_{id} & G_{ilio} \\ G_{oi} & G_{od} & -Z_{\text{out}} \end{pmatrix} \cdot \begin{pmatrix} \hat{v}_{in} \\ \hat{d} \\ \hat{i}_{out} \end{pmatrix} \quad (4.1)$$

Fig. 4-1 Set of small signal transfer functions defining a power converter

Input voltage to inductor current	$G_{ii(s)} = \left.\frac{\hat{I}_L}{\hat{Vin}}\right\|_{\hat{i}_{out}=\hat{d}=0}$ (4.2)	**Input voltage to output voltage**	$G_{oi(s)} = \left.\frac{\hat{V}_{out}}{\hat{V}_{in}}\right\|_{\hat{i}_{out}=\hat{d}=0}$ (4.3)
Control to inductor current	$G_{id(s)} = \left.\frac{\hat{I}_L}{\hat{d}}\right\|_{\hat{i}_{out}=\hat{V}_{in}=0}$ (4.4)	**Control to output voltage**	$G_{od(s)} = \left.\frac{\hat{V}_{out}}{\hat{d}}\right\|_{\hat{i}_{out}=\hat{V}_{in}=0}$ (4.5)
Open-loop output impedance	$Z_{out(s)} = \left.\frac{\hat{V}_{out}}{\hat{I}_{out}}\right\|_{\hat{d}=\hat{V}_{in}=0}$ (4.6)	**Output current to inductor current**	$G_{ilio(s)} = \left.\frac{\hat{I}_L}{\hat{I}_{out}}\right\|_{\hat{d}=\hat{V}_{in}=0}$ (4.7)

Table 4-1 Set of small signal transfer functions defining a power converter

The second method to find the small-signal power converter model is based on the average time-invariant circuit calculation depending on the different conduction modes of the converter for a given duty-cycle ratio. Using this model, the state-space matrix and theirs corresponding linear and small-signal models can be formulated [4.2] . The calculations for the open-loop continuous-time small-signal model and their corresponding transfer functions are developed in the point 8.1.1 of the Appendix A [4.3] In next points, the formulation of the open-loop discrete-time small-signal of a synchronous Buck converter is shown.

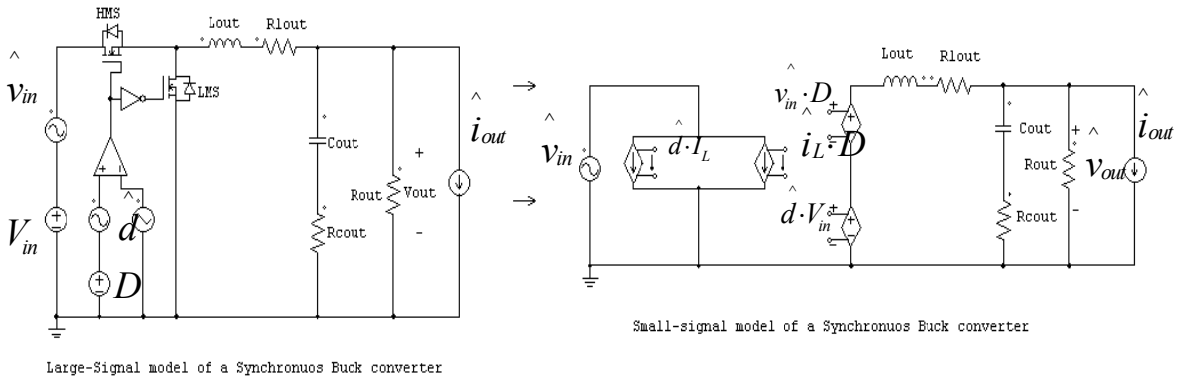


Fig. 4-2 Small-signal Buck converter average model

4.2.2 Delay effects in the digitally-controlled power converter.

As it has been commented in the first chapter, the delay introduced by the digital control system is an important design constraint. This delay may cause that our system become unstable due to the considerable reduction of phase and gain margins of the closed-loop system.

Thus, a delay term denoting the total time-delay of the digital structure can be condensed in one single block as it is shown in (4.8). This delay block is composed by the time propagation of the driver ICs gates (t_{prop}), the sensor delay (t_{sens}), the execution time of the algorithm of the control law (t_{alg}), the ADC time (t_{ADC}) and the time employed by the modulator (t_{DPWM}) to generate the duty-cycle shown in (2.7). Moreover, the ADC time is composed by the acquisition time (t_{zoh}) and the analogue-to-digital conversion time (t_{conv}).

$$t_d = t_{prop} + t_{sens} + t_{alg} + t_{ADC} + t_{DPWM} \quad (4.8)$$

This block (G_{td}) corresponds in the z-field to an integer multiple of the switching period (k) according to the delay value:

$$G_{td}(z) = z^{-k} \quad (4.9)$$

with k as an integer multiple of the switching period

Table 4-2 shows the delay effect in a Buck converter controlled by means of digital Voltage-Mode Control (see more details about the system in point 4.3.2.4) where it can be noticed how the system becomes unstable beyond a maximal delay value.

In consequence, the delay introduced by the digital control system should be considered in the small-signal control-to-output voltage transfer function of the power converter to avoid stability problems in our closed-loop system.

Delay (µs)	Loop-gain frequency response		
	GM (dB)	PM (◦)	Crossover frequency (kHz)
0	36.2	82.3	34.7
2	8.0	57.3	
4	2.9	32.2	
6	0.4	7.23	
8	-0.9	-17.8	

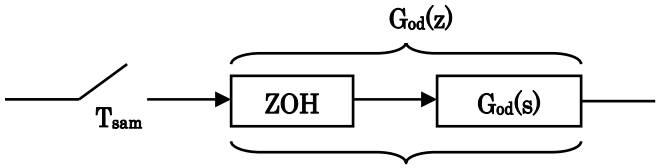
unstable →

Table 4-2 Delay effect in the stability margins of the digitally-controlled system

4.2.3 Analogue-to-digital conversion.

The open-loop small-signal power converter model is necessary for the design of the external voltage-loop compensation network. Two possibilities are available to find the corresponding discrete-time small-signal models.

The first approach is based on the continuous-to-discrete time conversion of the ZOH, power converter and delay models as it is illustrated in Fig. 4-3. The main drawback of this approach is that only integer time-delays are accepted using this approach when numerical tools like Matlab are used.



$$Z\left\{L^{-1}\left(\left(\frac{1-e^{-s\cdot T_{sam}}}{s}\right)\cdot G_{od}(s)\right)_{t=n\cdot T_{sam}}\right\} \tag{4.10}$$

Fig. 4-3 Continuous-to-discrete time conversion of the control-to-output voltage small-signal transfer function

The second approach relies on the direct calculation of the discrete-time small-signal transfer function of the power converter using geometrical approximations of its continuous-time behaviour. This approach tries to correct some errors associated to the continuous-to-discrete time mapping in the power converter. The discrete-time small-signal model for the synchronous Buck converter is disclosed in the next point.

4.2.4 Discrete-time formulation

Two basic approaches can be found to formulate the discrete-time model of a PWM-controlled power converter. First technique defines the sampled-time behaviour of the state-space variables during one switching period. This technique is grounded on the previous knowledge of the power converter and its target behaviour for next switching period [4.4] , [2.24]

Second alternative is based on the direct formulation of the discrete-time state-space matrix considering the power converter as a sampled-data system [4.5] [4.6] . Both approaches are detailed in next points.

4.2.4.1 Discrete-time model based on the predictive behaviour of the continuous-time model

Inductor current can be sampled in equally-time intervals which means constant sampling frequency. Thus, the inductor current at the end of the present switching period is considered like the predictive goal reference (see Fig. 4-4).

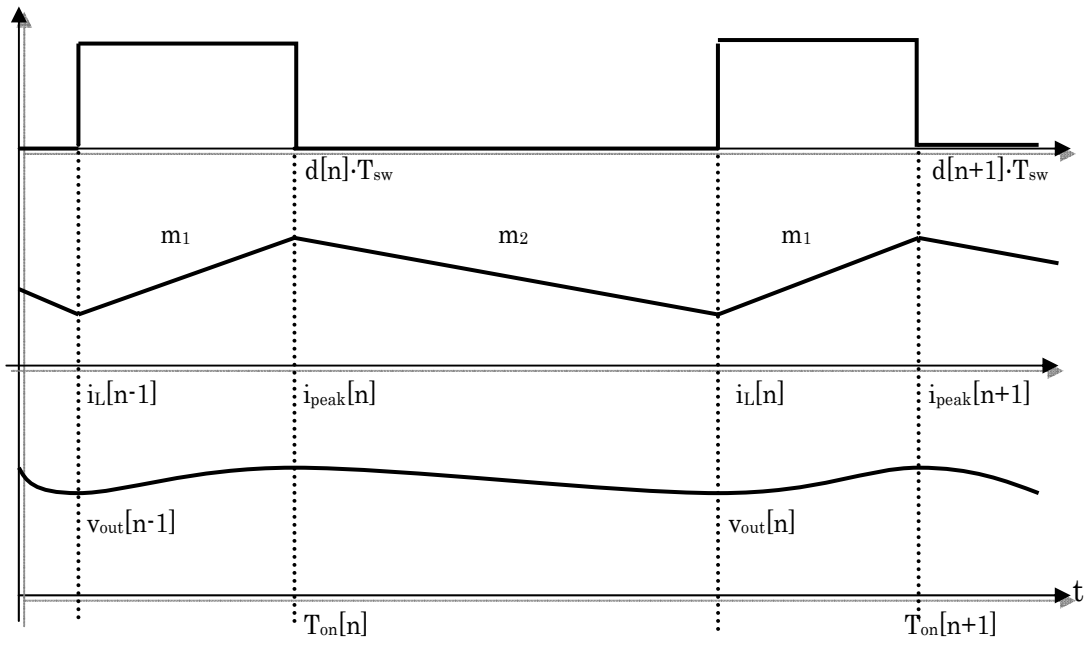


Fig. 4-4 State-space variables evolution

Observing previous figure, the inductor current can be described as follows:

$$i_L[n] = i_L[n-1] + \frac{V_{in}}{L_{out}} \cdot d[n] \cdot T_{sw} - \frac{V_{out}}{L_{out}} \cdot T_{sw} \tag{4.11}$$

Considering low-ripple hypothesis, that means, input and output voltages are almost constant during several switching periods, the inductor current behavior

for next switching period can be written as follows

$$i_L[n+1] = i_L[n] + \frac{V_{in}}{L_{out}} \cdot d[n+1] \cdot T_{sw} - \frac{V_{out}[n]}{L_{out}} \cdot T_{sw} \tag{4.12}$$

Similarly than in the inductor current case, the output voltage can be obtained:

$$V_{out}[n+1] = V_{out}[n] + \frac{T_{sw}}{C_{out}} \cdot \left(i_L[n+1] - \frac{V_{out}[n]}{R_{out}} \right) \tag{4.13}$$

Next step is to find the discrete-time state-space matrix for the converter. Thus previous equations should be combined to find the discrete-time space-state system. The complete formulation can be found in point 8.1.2.1 of the Appendix A obtaining next results:

$$G_{od}(z) = \frac{\dfrac{T_{sw}^2 \cdot V_{in}}{R_{out} \cdot C_{out}} \cdot \dfrac{1}{1 + \dfrac{T_{sw}}{R_{out} \cdot C_{out}}} \cdot z^2}{z^2 - z \cdot \left(1 + \dfrac{R_{out}}{L_{out}} \cdot \left(\dfrac{L_{out} \cdot C_{out} - T_{sw}^2}{R_{out} \cdot C_{out} + T_{sw}} \right) \right) + \dfrac{R_{out}}{L_{out}} \cdot \left(\dfrac{L_{out} \cdot C_{out} - T_{sw}^2}{R_{out} \cdot C_{out} + T_{sw}} \right) + \dfrac{T_{sw}^2 \cdot R_{out}}{L_{out} \cdot \left(R_{out} \cdot C_{out} + T_{sw} \right)}} \cdot D(z) \tag{4.14}$$

$$G_{id}(z) = \frac{\left(z - \dfrac{1}{1 + \dfrac{T_{sw}}{R_{out} \cdot C_{out}}} \right) \cdot \dfrac{T_{sw} \cdot V_{in}}{L_{out}} \cdot z}{z^2 - z \cdot \left(1 + \dfrac{R_{out}}{L_{out}} \cdot \left(\dfrac{L_{out} \cdot C_{out} - T_{sw}^2}{R_{out} \cdot C_{out} + T_{sw}} \right) \right) + \dfrac{R_{out}}{L_{out}} \cdot \left(\dfrac{L_{out} \cdot C_{out} - T_{sw}^2}{R_{out} \cdot C_{out} + T_{sw}} \right) + \dfrac{T_{sw}^2 \cdot R_{out}}{L_{out} \cdot \left(R_{out} \cdot C_{out} + T_{sw} \right)}} \cdot D(z) \tag{4.15}$$

4.2.4.2 Sampled-data formulation of the continuous-time model

A discrete-time or sampled-data system can be expressed with the following equation system [4.5] .

$$\begin{aligned} \hat{x}[n+1] &= \Phi \cdot \hat{x}[n] + \gamma \cdot \hat{d}[n] \\ \hat{y}[n] &= C \cdot \hat{x}[n] \end{aligned} \tag{4.16}$$

With:

$$\begin{aligned} \Phi &= e^{A_1 \cdot D \cdot T_{sw}} \cdot e^{A_2 \cdot (1-D) \cdot T_{sw}} = e^{A_e \cdot T_{sw}} \\ \gamma &= \Phi \cdot \alpha \cdot T_{sw} \end{aligned} \tag{4.17}$$

Equations (4.16) and (4.17) summarize the discrete-time power converter model. Next, matrix exponentials of previous equation are replaced by their first order approximation as follows [4.6]

$$\Phi = e^{A_2 \cdot T_{sw}} \approx I + A_2 \cdot T_{sw} \tag{4.18}$$

In this case, the delay term should be added to (4.17) in order to be taken into account in the duty-cycle generation.

$$\gamma = e^{A_e \cdot (T_{sw} - t_d)} \cdot \alpha \cdot T_{sw} \tag{4.19}$$

With:

$$\alpha = (A_1 - A_2) \cdot x[n] + (B_1 - B_2) \cdot V_{in} = B_1 = \begin{pmatrix} \frac{V_{in}}{L_{out}} \\ 0 \end{pmatrix} \tag{4.20}$$

Replacing (4.18) and (4.19) in (4.16) and considering the capacitor ESR like the dominant parasitic effect $(R_{cout} << R_{out}; R_L << R_{out})$, the control-to-output voltage and the control-to-inductor current transfer functions can be obtained as follows:

$$G_{od}(z) = \frac{\frac{V_{in} \cdot T_{sw}}{L_{out} \cdot C_{out}} \cdot (m + C_{out} \cdot R_{cout}) \cdot \left(z + \frac{T_{sw}}{m + C_{out} \cdot R_{cout}} \cdot \left(\frac{R_{cout}}{R_{out}} - \frac{C_{out} \cdot R_{cout}}{T_{sw}} - \frac{R_{cout} \cdot m}{L_{out}} + \frac{t_d}{T_{sw}} \right) \right)}{z^2 + z \cdot \left(\frac{T_{sw}}{R_{out} \cdot C_{out}} - 2 \right) + 1 - \frac{T_{sw}}{R_{out} \cdot C_{out}} + \frac{T_{sw}^2}{L_{out} \cdot C_{out}}} \tag{4.21}$$

$$G_{id}(z) = \frac{\frac{V_{in} \cdot T_{sw}}{L_{out}} \cdot \left(z - 1 + \frac{T_{sw}}{R_{out} \cdot C_{out}} - \frac{m \cdot T_{sw}}{L_{out} \cdot C_{out}} \right)}{z^2 + z \cdot \left(\frac{T_{sw}}{R_{out} \cdot C_{out}} - 2 \right) + 1 - \frac{T_{sw}}{R_{out} \cdot C_{out}} + \frac{T_{sw}^2}{L_{out} \cdot C_{out}}} \tag{4.22}$$

Evaluating previous equations, it is observed that last method diverges in the delay term compared to the analogue-to-discrete using the ZOH approach. Thus, delay in (4.21) only takes effect in the position of the zero of the control-to-output voltage transfer function keeping constant its denominator. Otherwise, in the ZOH method, delay is reflected in the denominator with the addition of several units delays (z terms) corresponding to an integer multiple of the switching-period and remaining the numerator unalterable.

4.3 Modeling of Digital Control Laws for Voltage Regulators

4.3.1 Introduction

Digital regulation in VRs is classically obtained by means of linear output voltage feedback, i.e. Digital Voltage-Mode Control (DVMC). By the way, DVMC is an easy and low-complexity control technique which avoids current measurement. This is particularly interesting in high-frequency applications where current sense could be problematic. Nevertheless, a proper tracking and control of the converter inductor current is especially important in non-constant load current applications like VRs. Furthermore, multiphase architectures require CS loops to obtain their intrinsic characteristics. In consequence, inductor current data should be available.

Digital Current-Mode Control (DCMC) repairs the previous lack of information giving several advantages over conventional DVMC. In point of fact, DCMC possess the same advantages that analogue CMC. Thus, the inductor-current is tightly controlled cycle-by-cycle allowing enhanced robustness face load variations and instant inductor over-current protection. Another advantage is that DCMC offers higher flexibility in the design of the output voltage feedback control loop due to the reduced model of the current-mode power converter. In fact, this model only contains a low-frequency pole instead of the two complex poles of DVMC power converters. Thus, the inner current-loop controls the inductor-current in such a way that system only has one low-frequency pole. This pole is defined by the output capacitor and load impedance. Moreover, DCMC designs own improved immunity to line disturbances since they are included in the small-signal model of the power converter. Thus, control-to-output voltage transfer function of DCMC is not depending on the input voltage as happened in the DVMC case.

In short, DCMC or a CS loop at least is recommended for multiphase VRs. Therefore, DVMC, DCMC and CS techniques are studied along next sections.

4.3.2 Digital Voltage-Mode Control

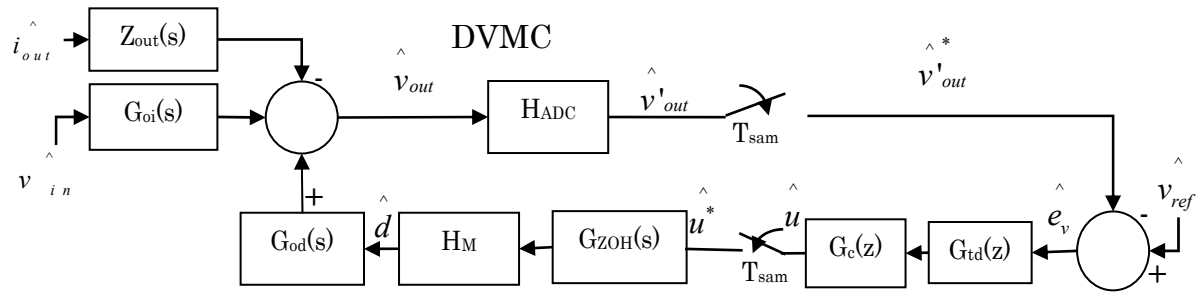
4.3.2.1 Introduction

In DVMC, the converter output voltage is sensed first and after transformed into the digital word. Modern VRs incorporates a communication interface with the microprocessor. This "dialogue" module is used by the power converter to know the desired supply voltage by the µp. Thus, this later delivers a digital word to the power converter known as VID (Voltage IDentification) containing the supply levels required. This digital reference word is compared with the digital output voltage to generate the digital voltage error signal. This VID varies between a minimal and maximal value depending on the power consumption of the µp. Next, a digital filter working as linear voltage-compensation network computes the digital error signal and the result is send to a DPWM where the duty-cycle signal controls the switches of the power converter.

In previous points, the power converter small-signal model has been found. Now, these power converter small-signal models are used to define the digital control law small-signal models in next points.

4.3.2.2 Small-signal model of Digital-Voltage Mode

The small-signal model for DVMC is illustrated in Fig. 4-5. Using this model, the small-signal output-voltage of the power converter can be calculated as it is shown in (4.26).



With:
G_c: Digital compensation network
H_M: modulator gain
Z_{out}: Output impedance transfer function
V_{fs_DPWM}: modulator Full-scale voltage
K_{sense}: output voltage sensor gain
V_{peak} : Peak-slope voltage of the analogue PWM
G_{od}: Control-to-output voltage transfer function
H_{ADC}: Output voltage sensor & linear ADC gain
G_{oi}: Input voltage-to-output voltage transfer function
V_{fs_ADC}: ADC Full-scale voltage
G_{ZOH}: Zero Order Hold transfer function

Fig. 4-5 Small-signal model of Digital Voltage Mode Control

Hence:

$$H_M = \frac{V_{fs\_DPWM}}{2^{n\_DPWM}-1} \text{ (DPWM)} \qquad \text{H}_M = \frac{1}{V_{peak}} \text{ (PWM)} \quad (4.23); \qquad H_{ADC} = K_{sense} \cdot \frac{2^{n\_ADC}-1}{V_{fs\_ADC}} \quad (4.24); \qquad ZOH(s) = \frac{1-e^{s \cdot T_{sam}}}{s}$$

(4.25)

Finally, the small-signal output voltage is calculated as follows:

$$\begin{aligned} \hat{v}_{out}(z) = \hat{v}_{in}(z) \cdot \left(\frac{G_{oi}(z)}{1 + G_c(z) \cdot G_{td}(z) \cdot Z\left\{ L^{-1}\left(H_{ADC} \cdot G_{od}(s) \cdot H_M \cdot G_{zoh}(s) \right)_{t=n \cdot T_{sam}} \right\}} \right) - \\ \hat{i}_{out}(z) \cdot \left(\frac{Z_{out}(z)}{1 + G_c(z) \cdot G_{td}(z) \cdot Z\left\{ L^{-1}\left(H_{ADC} \cdot G_{od}(s) \cdot H_M \cdot G_{zoh}(s) \right)_{t=n \cdot T_{sam}} \right\}} \right) + \\ \hat{v}_{ref}(z) \cdot \left(\frac{G_c(z) \cdot G_{t_d}(z) \cdot Z\left\{ L^{-1}\left(G_{od}(s) \cdot H_M \cdot G_{zoh}(s) \right)_{t=n \cdot T_{sam}} \right\} H_{DPWM} \cdot G_{od}(z)}{1 + G_c \cdot G_{td} \cdot Z\left\{ L^{-1}\left(H_{ADC} \cdot G_{od}(s) \cdot H_M \cdot G_{zoh}(s) \right)_{t=n \cdot T_{sam}} \right\}} \right) \end{aligned} \quad (4.26)$$

Where $G_{oi}(z)$ and $Z_{out}(z)$ can be obtained in a similar way than (4.10). The model presented in Fig. 4-5 can be simplified as it is represented in Fig. 4-6 to obtain the open-loop and the closed-loop gains exposed in (4.27) and (4.28) respectively. In these transfer functions, $G_{od}(z)$ can be whichever transfer function shown previously, i.e., (4.10), (4.14) or (4.21).

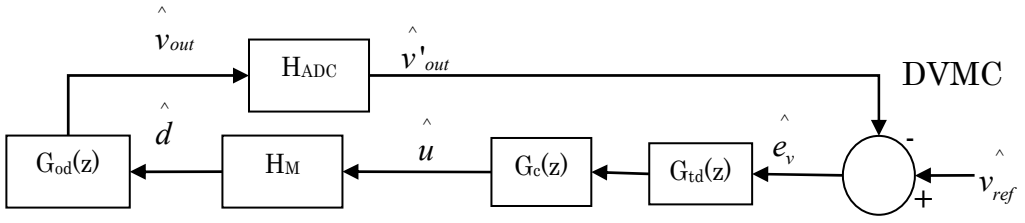


Fig. 4-6 Discrete-time small-signal model of Digital Voltage Mode Control

$$T_{ol\_DVMC}(z) = H_{ADC} \cdot G_{t_d}(z) \cdot G_c(z) \cdot H_{DPWM} \cdot G_{od}(z) \quad (4.27)$$

$$T_{cl\_DVMC}(z) = \frac{v_{out}(z)}{v_{ref}(z)} = \frac{G_c(z) \cdot H_{DPWM} \cdot G_{t_d}(z) \cdot G_{od}(z)}{1 + H_{ADC} \cdot G_c(z) \cdot H_{DPWM} \cdot G_{t_d}(z) \cdot G_{od}(z)} \quad (4.28)$$

4.3.2.3 Digital filter implementation

The digital filter of the external voltage loop is the focal point of DVMC design. In general, it is based on a digital PI/PID structure. Thus, the main problem is to find a suitable tuning method. Classically, the compensation network for the external voltage regulation loop is calculated in the s-domain since designers are most used to continuous-time tuning techniques. After, this compensation network is mapped in the z-domain using some analogue-to-discrete time method technique. A guide to select the most suitable analogue-to-discrete time method in this case is found in [4.7] .

Thus, there are several ways to tune correctly the compensation network. Hence, analytical techniques (IMC, lambda tuning) based on algebraic relations between the power converter and the required response specifications need a very accurate power converter model to find suitable filter coefficients [4.8] .

Another possibility is trial-and-error or experimental methods like Ziegler-Nichols techniques. These methods are the easiest way to find the filter coefficients although they are not accurate in most of cases. Moreover, they require a former knowledge of the converter to determine the gain and the speed of the system.

Another kind of tuning is based on frequency methods where the filter is designed using the open-loop Bode diagram of the power converter. These methods normally privilege the system robustness against disturbances to other design specifications.

Other tuning possibilities are based on online (adaptive) or offline (optimal control) tunings in which previous tuning techniques are combined. For instance, LUT (Look-Up-Tables) can be used to store a set of filter coefficients which has been previously calculated using one of the cited techniques [4.9]

In relation to the digital filter architecture, it influences directly in the converter behavior. Thus, some topologies privileges system robustness and others are preferred by their lower computational cost. The choice of the filter architecture should be made depending on the application, the architecture of the digital controller and the desired performances.

Then, the first digital architecture is known as “parallel” or “position”

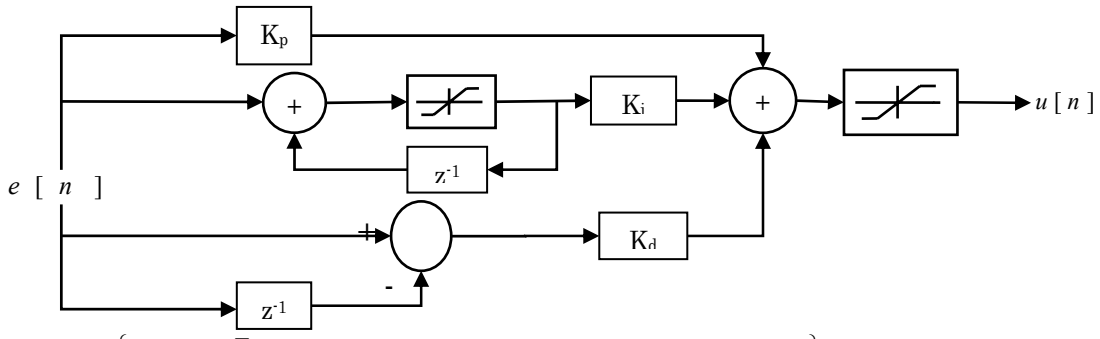
algorithm. This configuration owns an integral part based on an accumulation of the past errors.

$$u[n] = K_p \cdot e_v[n] + K_i \cdot s[n] + K_d \cdot (e_v[n] - e_v[n-1])$$
$$with: s[n] = s[n-1] + e_v[n] \tag{4.29}$$

With:

$$K_d = K_p \cdot \frac{T_d}{T_{sam}};\ K_i = K_p \cdot \frac{T_{sam}}{T_i}; \tag{4.30}$$

With K_p as the proportional gain, K_i as the integral gain, K_d as the derivative gain, T_d as the derivative time, T_i as the integral time and T_{sam} as the sampling period. Moreover, this architecture allows three variations depending on how the integral part is calculated. Its block diagram can be seen in Fig 4-7.



$$s[n] = \begin{cases} s[n-1] + \frac{T_{sam}}{2} \cdot (e_v[n] + e_v[n-1]) & \leftarrow \text{trapezoidal law} \\ s[n-1] + T_{sam} \cdot e_v[n] & \leftarrow \text{backward Euler law} \\ s[n-1] + T_{sam} \cdot e_v[n-1] & \leftarrow \text{forward Euler law} \end{cases} \tag{4.31}$$

Fig. 4-7 PID position algorithm with backward Euler approximation for the integral term.

Parallel algorithm owns a variation from its classical point known as "Setpoint weighting" [4.9] This algorithm treats independently the three branches of the filter reducing the noise effects in the output. Hence, the values for the three branches are;

$$P[n] = K_p \cdot \left(b \cdot V_{ref}[n] - V_{out}[n]\right) \tag{4.32}$$
$$I[n] = I[n-1] + \left(\frac{K_p \cdot T_{sam}}{T_i}\right) \cdot \left(V_{ref}[n] - V_{out}[n]\right)$$
$$D[n] = \underbrace{\left(\frac{T_d}{T_d + N \cdot T_{sam}}\right)}_{K_{d1}} \cdot D[n-1] - \underbrace{\left(\frac{K_p \cdot T_d \cdot N}{T_d + N \cdot T_{sam}}\right)}_{K_{d2}} \cdot \left(v[n] - V_{out}[n-1]\right)$$

Where b varies between 0 to 1 depending on the weight assigned to load disturbances effect. N is a limiting factor for the derivative term owning values

between 3 to 20. The block diagram of this architecture is represented in Fig. 4-8.

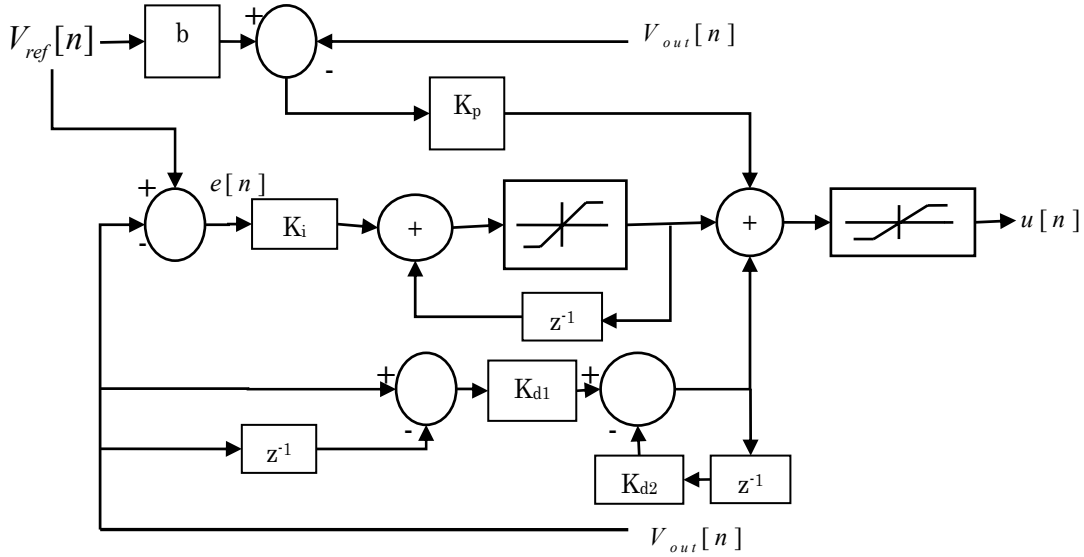


Fig. 4-8 Setpoint Weighting PID algorithm with backward Euler approach for the integral term.

This architecture is quite useful for digital controllers which are able to execute parallel process since the 3 branches can be processed at the same time.

However, digital controllers like DSPs privileges architectures with lower computational than previous parallel structures. Thus, serial or incremental (also known velocity) algorithms, as the one shown in Fig. 4-9, are introduced. These digital filters present IIR structures and they own the advantage of less abrupt output variations. In contrast, these architectures are quite sensitive to coefficients variations. This fact may cause significant differences in the final system behavior affecting its stability. Thus, next figure shows the block diagram for an incremental PID algorithm owning a recurrence equation like:

$$\begin{aligned} &u[n] = u[n-1] + K_1 \cdot e_v[n] + K_2 \cdot e_v[n-1] + K_3 \cdot e_v[n-2] \\ &with: K_1 = K_p + K_i + K_d; K_2 = -K_p - 2 \cdot K_d; K_3 = K_d \end{aligned} \tag{4.33}$$

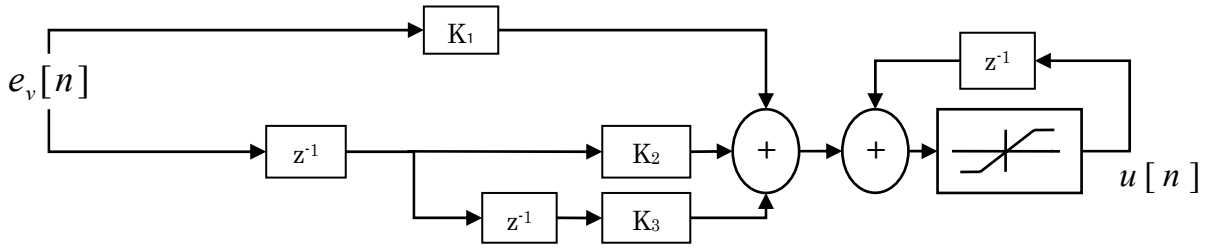


Fig. 4-9 PID incremental algorithm

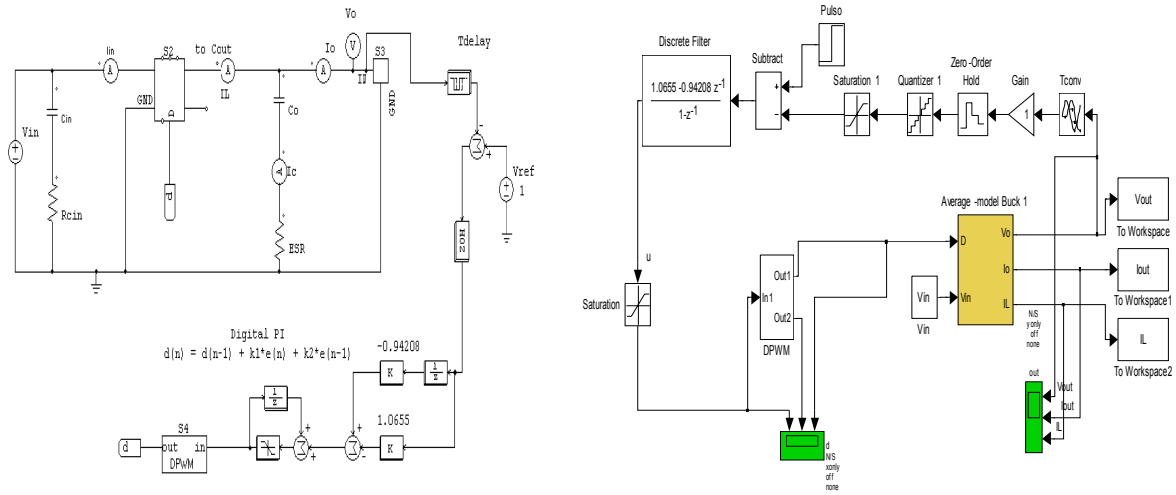
4.3.2.4 Example of Digital Voltage Mode Control.

In this point, an example of DVMC law is modelled for a given single-phase syncrhonous PWM-controlled Buck converter where its specifactions are summarized in Table 4-3.

Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value
Input Voltage (V_{in})	5V	Output Voltage (V_{out})	1V	Nominal Output current (I_{out})	25A	Output Current Variation (ΔI_{out})	5A
Switching frequency (f_{sw})	1MHz	Sampling frequency (f_{sam})	1MHz	Total delay (t_d)	1μs	MLCC Output Capacitor (C_{out})	80μF
MLCC Input Capacitor (C_{in})	80μF	Output Inductance (L_{out})	300nH	Rds Power Switch (R_{ds1})	5mΩ	Rds Synch. Switch (R_{ds2})	3mΩ
Output Inductance Serial Resistance (DCR)	0.6mΩ	MLCC Output Capacitor ESR (ESR)	6.8mΩ	MLCC Input Capacitor ESR (R_{cin})	6.8mΩ	Digital Filter	Serial PI

Table 4-3 DC/DC converter specifications

Firstly, simulation models of the digital system are found using PSIM and also Simulink. This later containis the switched small-signal power converter model (found in previous points, see point 8.1.1). For a simple comparison, a digital filter based on the PI incremental algorithm (backward-Euler type) is used. Both simulation schemas are shown in Fig. 4-10.



PSIM Model Simulink model using the continuous-time description

Fig. 4-10 PSIM and Simulink models of DVMC

Hence, simulations results are represented in Fig. 4-11 where similar results are obtained using both models despite of minor differences in the dynamic response are detected among them when a load variation is produced.

With regards to the stability of the system, Fig. 4-12 illustrates how all the system roots are inside of the unity-radius circle obtaining a gain margin of 30º and a crossover frequency of 40 kHz.

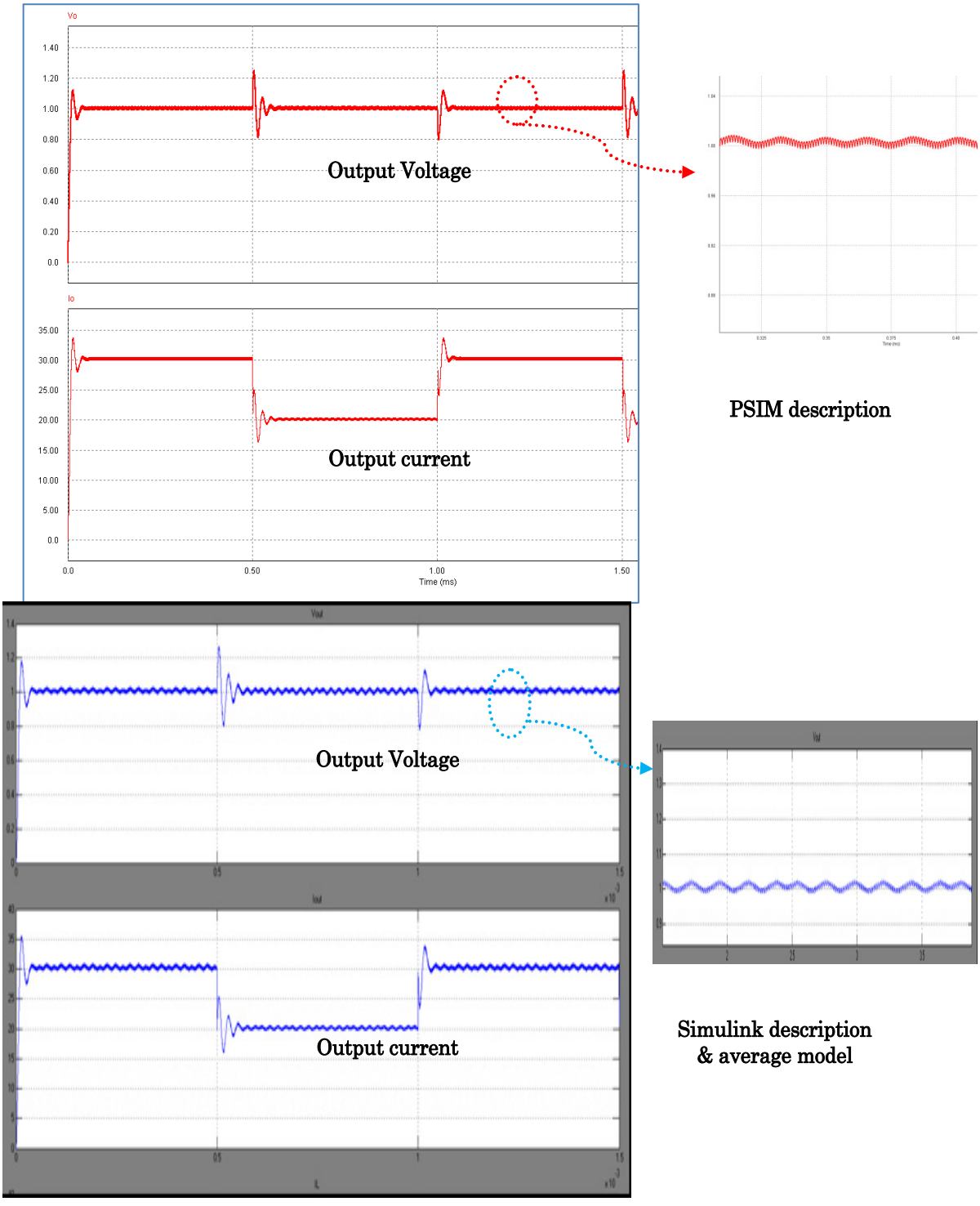


Fig. 4-11 DVMC: Simulation results for a 5A load variation

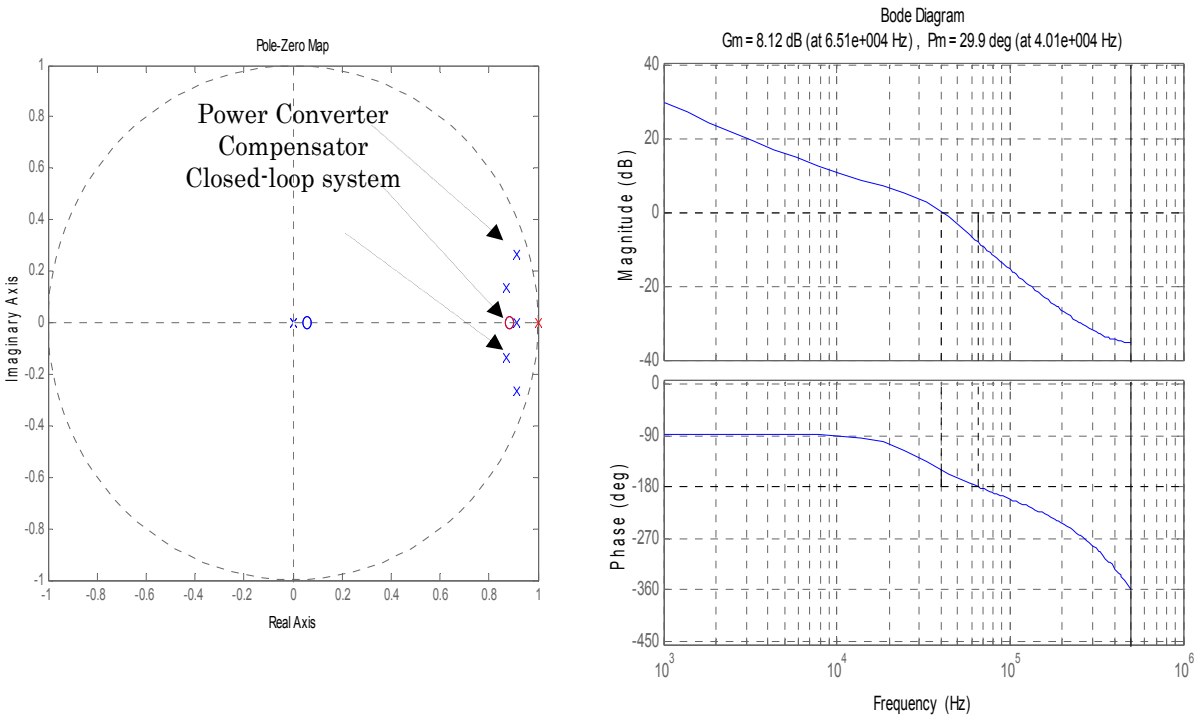


Fig. 4-12 Pole & zero map (left) and frequency response of the loop gain.

4.3.3 Digital Current-Mode Control.

4.3.3.1 Introduction

As happens in the analogue case, DCMC is achieved by means of a double feedback regulation of the inductor current and the output voltage correspondingly.

Thus, in inner current loop, the error signal is obtained by means of the subtraction of the inductor current and a reference current imposed by the external voltage-regulation loop. This kind of regulation is known as Current-Programmed Control (CPC) and can be classified as peak, average or valley current control depending on whether the maximum, average or the minimum point of the inductor current is compared with the reference.

For example, valley-current control follows a reference (i_c) placed at the minimal inductor current point. This later technique does not offer over-current protection and it is often replaced by the peak-current method where the reference is now imposed to be the maximal desired inductor current value. Peak-current method presents an inherent pulse-by-pulse fast over-current protection making it very useful for VR applications. Additionally, average-current mode imposes its current reference to be the average value per period of the inductor current. This last technique is preferred sometimes in some specific applications

as PFC (Power Factor Correction) due to their low harmonic distortion. From a practical point of view, each CPC modulation should be used with their corresponding compensation ramp to avoid instabilities [4.12] .

4.3.3.2 Continuous-time small-signal model.

Numerous works had tried to model correctly CMC. Among them, Raymond Ridley formulated in the late 80's an accurate small-signal model for previous CMC techniques.

Thus, he defined a continuous-time small-signal model for some DC/DC converters which was useful up to half the switching frequency. In this model, the external voltage and the inner current feedback regulation loops were initially treated independently because of the instabilities of the current loop for duty-cycles higher than 0.5. After, a revision of this work solved this problem including the corresponding compensation slope in the model [4.13] .

In the Ridley's model represented in Fig 4-13, K_f and K_r are the feedforward gains representing the disturbances in the input and output voltages respectively. H_i, H_{iv} and H_v are the gains of the inductor current transducer, the control voltage modulator gain and the linear gain of the output voltage sensor. Moreover, $G_{c(}s)$ represents the voltage compensation network and $G_{td}(s)$ symbolizes the total system delay. The PWM gain can be represented as:

$$Fm = \frac{\hat{d}}{\hat{i}_c} = \frac{1}{(S_n + S_e)\cdot T_{sw}} = \frac{1}{m_c \cdot S_n \cdot T_{sw}} \tag{4.34}$$

and:

$$m_c = 1 + \frac{S_e}{S_n} \tag{4.35}$$

Where S_n and S_e are the sensed inductor current and the ON-time compensation ramp slope respectively. Finally, H_e is a gain block defining the effects of the sampling action in the current feedback loop [4.14]

After this model, some revisions based on the Ridley's model have appeared like the one published by D.Tan in 1993 where Average Current-Mode Control (ACMC) small-signal model is formulated [4.15] . This small-signal model was very similar to the Ridley's one as it can see observed in Fig. 4-13.

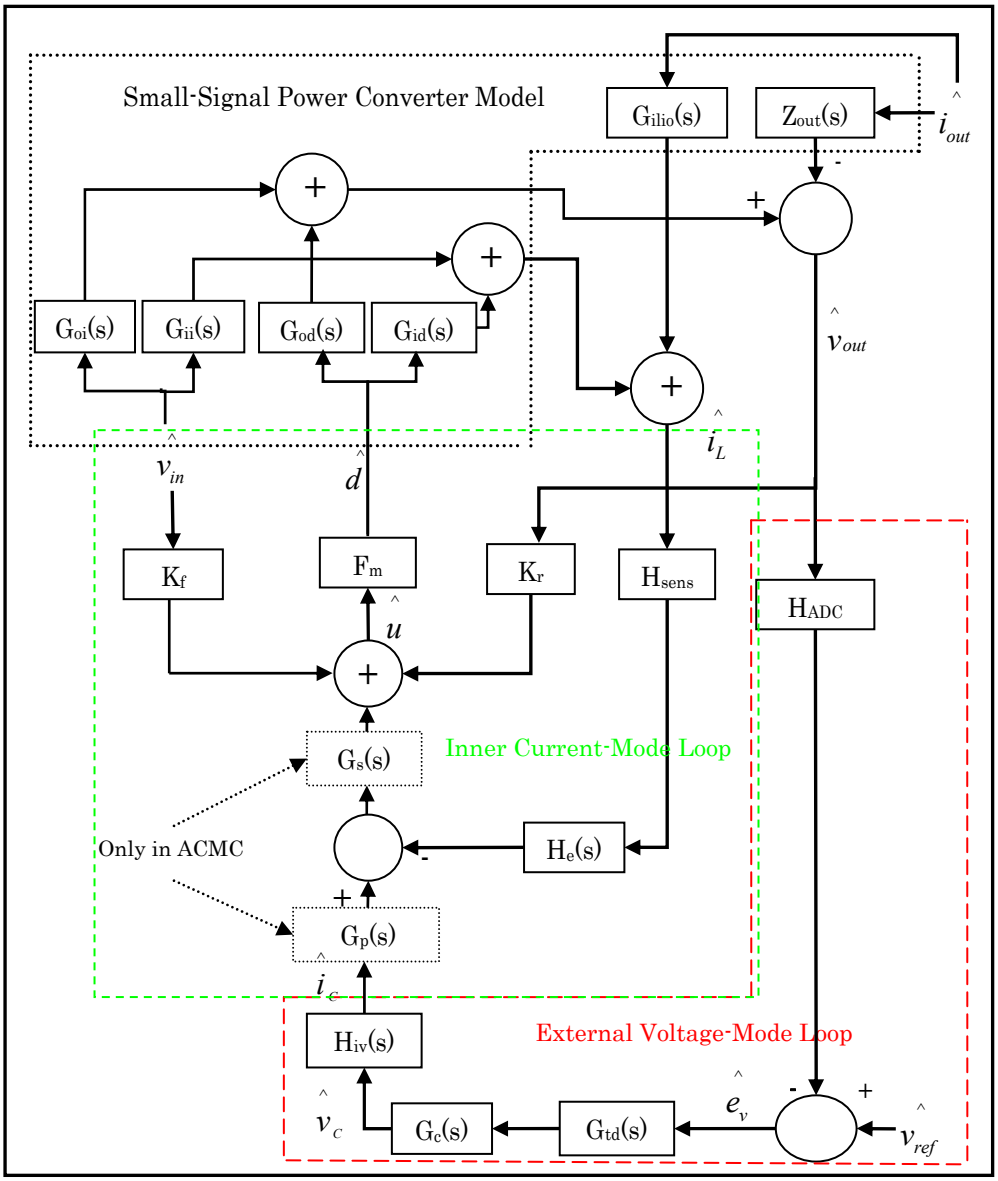


Fig. 4-13 Ridley's small-signal model for CMC

The main difference between PCMC and ACMC is that in this last case a current amplifier is inserted into the current loop to find the average value of the inductor current. This current amplifier ($G_{CA} = G_s \cdot G_p$) is composed by an integrator and a lead-lag network where the zero is placed before the natural frequency of the power converter to assure the stability and to maximize the crossover frequency of the current loop. Moreover, the pole is placed beyond half of the switching frequency to eliminate high-frequency noise.

As well in the VMC case, the control-to-output voltage transfer function should be obtained (the complete calculation is shown in the point 8.2.1). Then, and differently than in the VMC case, the control-to-output voltage transfer function is defined as:

$$G_{oc} = \left.\frac{\hat{v}_{out}}{\hat{i}_c}\right|_{\hat{i}_{out}=\hat{V}_{in}=0} \tag{4.36}$$

$$G_{oc} = \frac{F_m \cdot G_{od}}{1 + F_m \cdot \left(H_{sens} \cdot H_e \cdot G_{id} - K_r \cdot G_{od}\right)} \quad \text{for PCMC}$$

$$G_{oc} = \frac{F_m \cdot G_{ca} \cdot G_{od}}{1 + F_m \cdot \left(H_{sens} \cdot H_e \cdot G_{id} \cdot G_s - K_r \cdot G_{od}\right)} \quad \text{for ACMC} \tag{4.37}$$

Furthermore, the Ridley model allows us to calculate the loop gains for the inner current (T_i), external voltage (T_v) and global loop (T_{ol}) respectively [4.16]

$$\left.\begin{aligned} T_v &= F_m \cdot G_{od} \cdot G_c \\ T_i &= F_m \cdot H_{sens} \cdot G_{id} \\ T_{ol} &= T_v + T_i \end{aligned}\right\} \quad \text{for PCMC} \tag{4.38}$$

4.3.3.2.1 Example of Continuous-time Peak Current-Mode Control

An example of continuous-time PCMC is presented in this point. It has been developed taking the same converter values that in the point 4.3.2.4. The PI compensator for the external voltage loop has been calculated using the continuous-time control-to-output voltage transfer function exposed in (4.36) assuring the stability of the system for the whole range of loads and following the design guidelines exposed in [4.17]

As a general rule, the zero of the PI is placed close to the natural frequency of the power converter and the crossover frequency of the current loop is pushed as high as possible without exceeding half of the switching frequency. PSIM and Simulink (switched-mode) models are shown in Fig. 4-14 and the simulation results obtained with both models are presented in Fig. 4-15 and Fig 4-16 respectively.

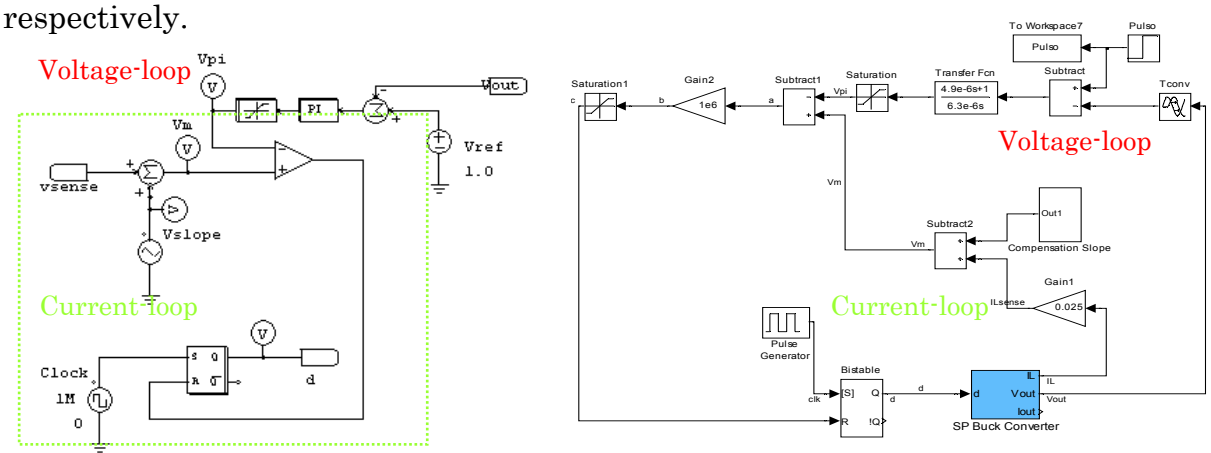


Fig. 4-14 Continuous-time Peak-Current Mode Control

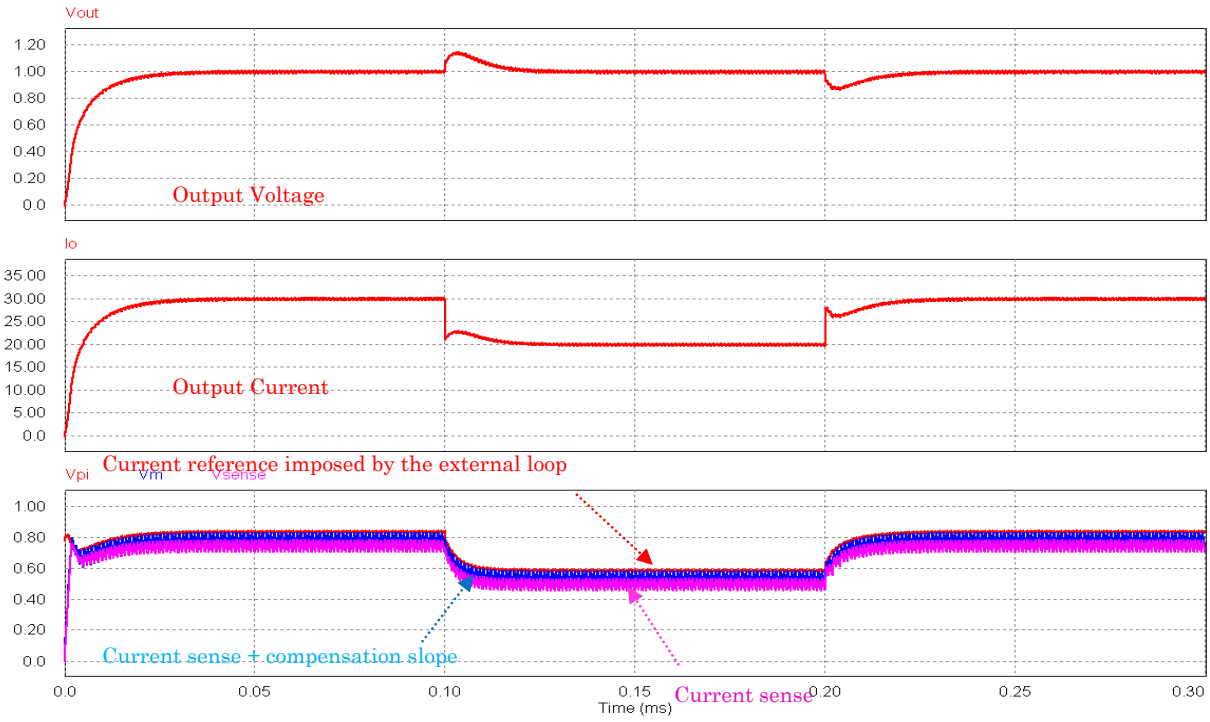


Fig. 4-15 PSIM Simulation of continuous-time Peak-Current Mode

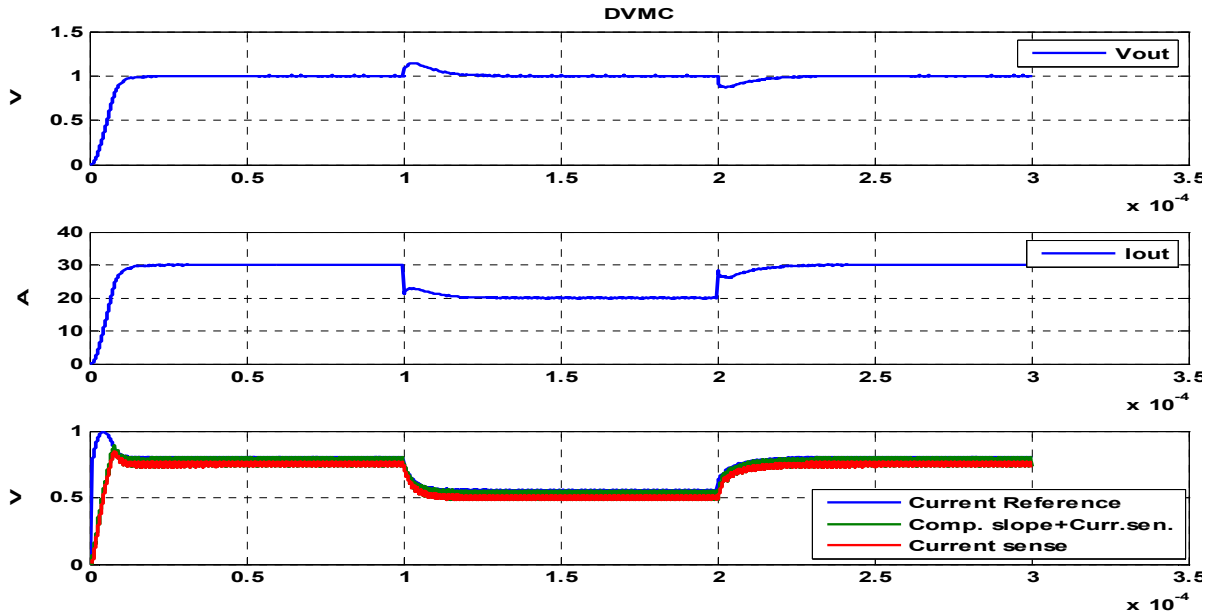


Fig. 4-16 Simulink simulation of continuous-time Peak-Current Mode

Afterwards, the stability of the system is calculated using the set of equations shown in (4.38) giving us a phase margin of 100º and a crossover frequency of 50 kHz. Indeed, all the roots of the closed-loop system are in the left hand of the map. Bode diagrams for the three loops as well as the pole-zero map of the closed loop system are shown in Fig. 4-17.

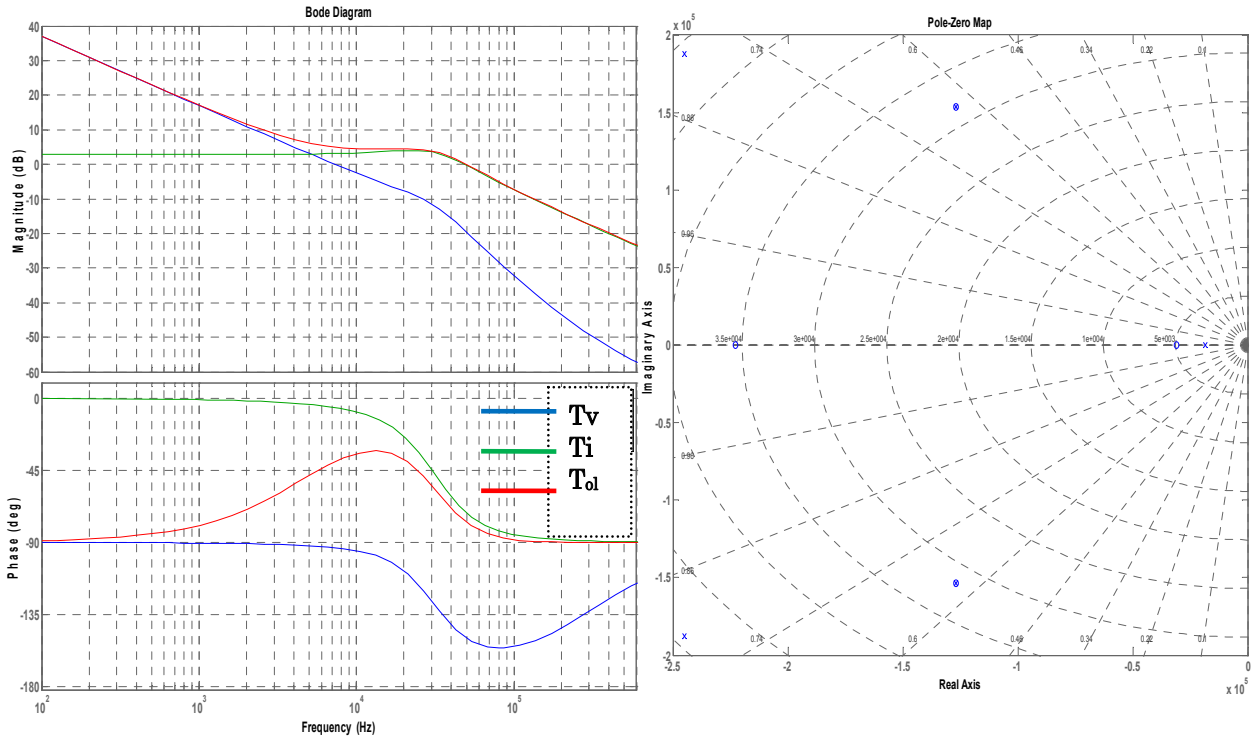


Fig. 4-17 Bode diagram (left) and closed-loop pole-zero map (right)

4.3.3.3 Discrete-time small-signal model

Using the same method described in 4.2.4.1 and [2.24] , the discrete-time equivalent of (4.36) can be found. The complete formulation can be found in point 8.2.1.2.

$$G_{oc}(z) = \frac{T_{sw}}{C_{out}} \cdot \frac{1}{\left(1 + \frac{T_{sw}}{R_{out} \cdot C_{out}}\right) \cdot \left(z - \frac{1}{1 + \frac{T_{sw}}{R_{out} \cdot C_{out}}}\right)} \tag{4.39}$$

Fig. 4-18 establishes a comparison among the frequency responses of the continuous-time Ridley's model exposed in (4.36), the discrete-time Ridley's approach using a ZOH and the direct formulation of the discrete time control-to-output-voltage transfer function found in (4.39). Thus, minor differences are found among models. However, the magnitude response of the model found in (4.39) is a little different of the continuous-time and continuous-time + ZOH approaches owning a maximal deviation of 3dB at the half of switching frequency. However, phase curves of both discrete-time models are quite different from the continuous-time model. Finally, the small-signal model for DCMC is illustrated in Fig. 4-19.

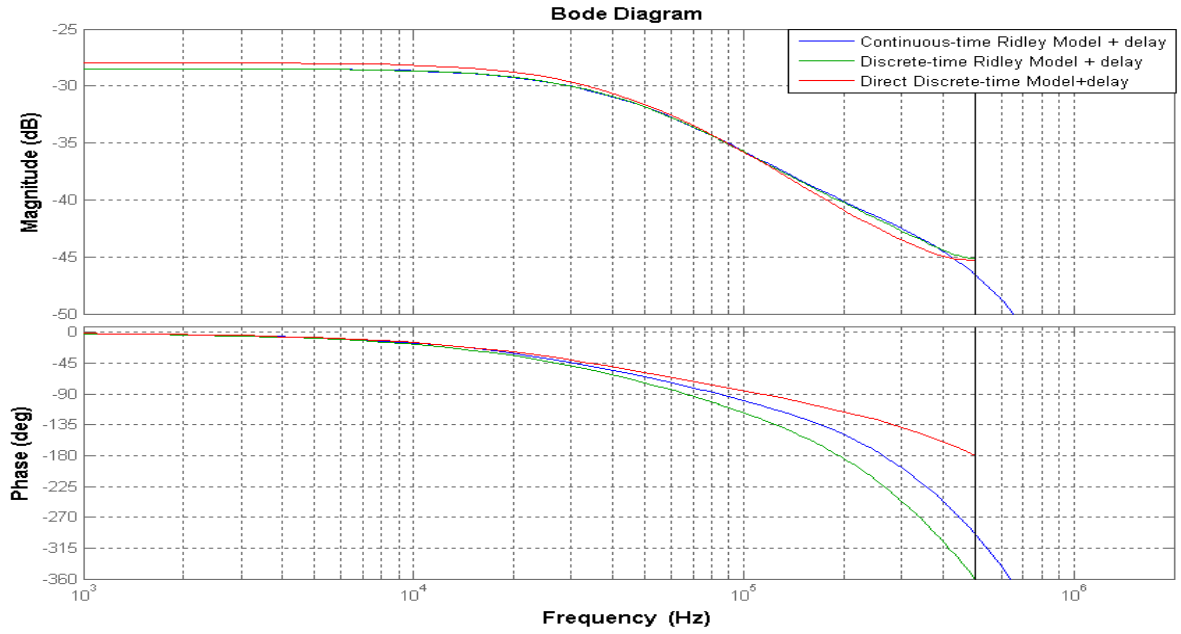
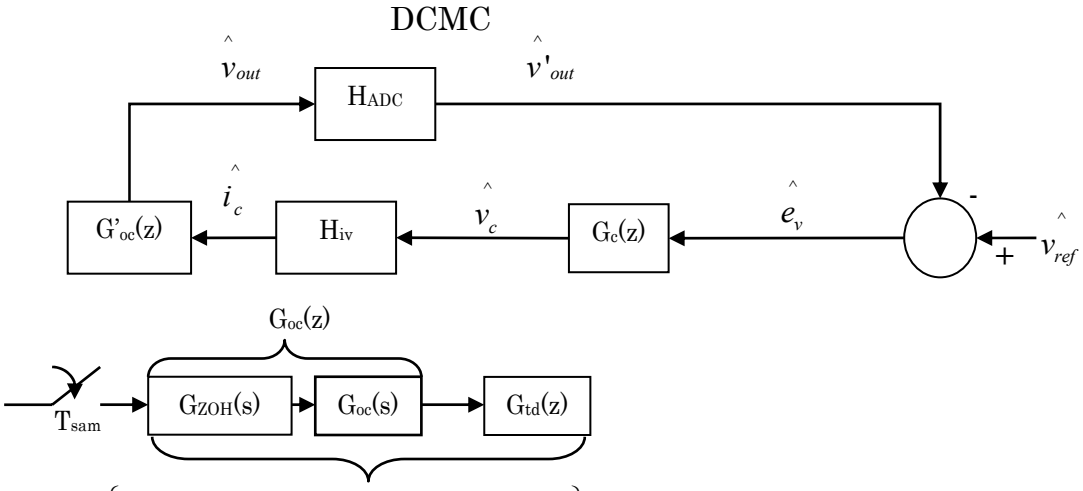


Fig. 4-18 Bode diagram of the control-to-output voltage transfer function in CMC.



$$G'_{oc}(z) = Z\left\{ L^{-1}\left(\left(\frac{1-e^{-s\cdot T_{sam}}}{s} \right) \cdot G_{oc}(s) \cdot e^{-s\cdot t_d} \right)_{t=n\cdot T_{sam}} \right\}$$ or (4.39) with a delay block associated ($G_{td}(z)$)

(4.40)

Fig. 4-19 Small-signal model of DCMC

4.3.3.3.1 Example of Discrete-Time Peak Current-Mode Control

4.3.3.3.1.1 Discrete-time Peak Current-Mode Control issues.

DCMC is not an effortless regulation technique since several critical parameters influence drastically in the final behavior of the converter. In this kind of regulation, the influence of the sampling frequency in the current-loop should be considered. Moreover, the way to obtain the control-to-output voltage transfer function to calculate the inner and external gain loop and the delay of

the whole digital system (as in the DVMC) are also worthy to be taken into account These three effects are exposed in the next point with some simulations obtained thanks our discrete-time PCMC (DPCMC) model using PSIM shown in Fig. 4-20.

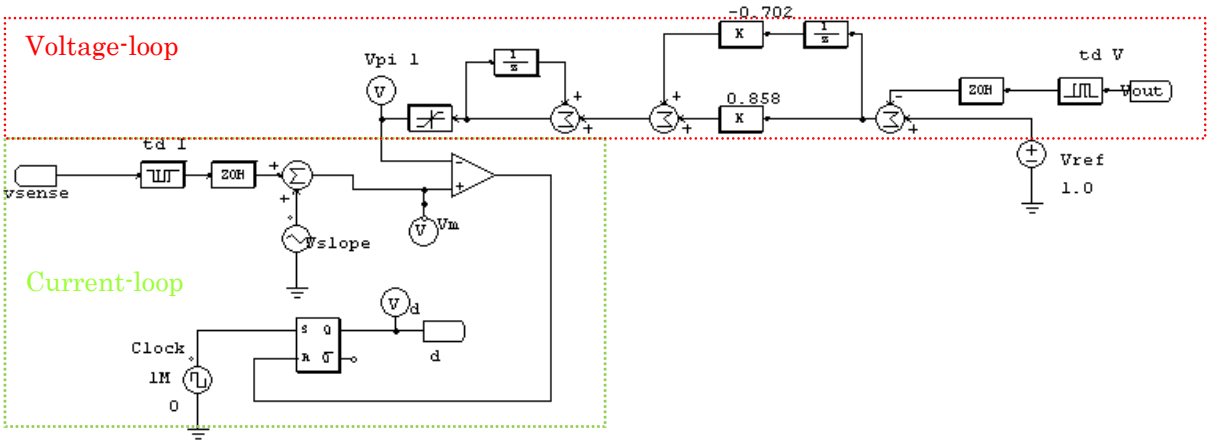


Fig. 4-20 PSIM simulation model of discrete-time PCMC

4.3.3.3.1.2 Influence of the delay of the digital system.

Reduced delays are quite important as it was disclosed in previous points. Delay is an intrinsic characteristic of digital systems and it should be considered in our design in order to have a stable system for the full range of loads. Thus, some conclusions can be extracted from Fig. 4-21 where a 5A load variation is simulated.

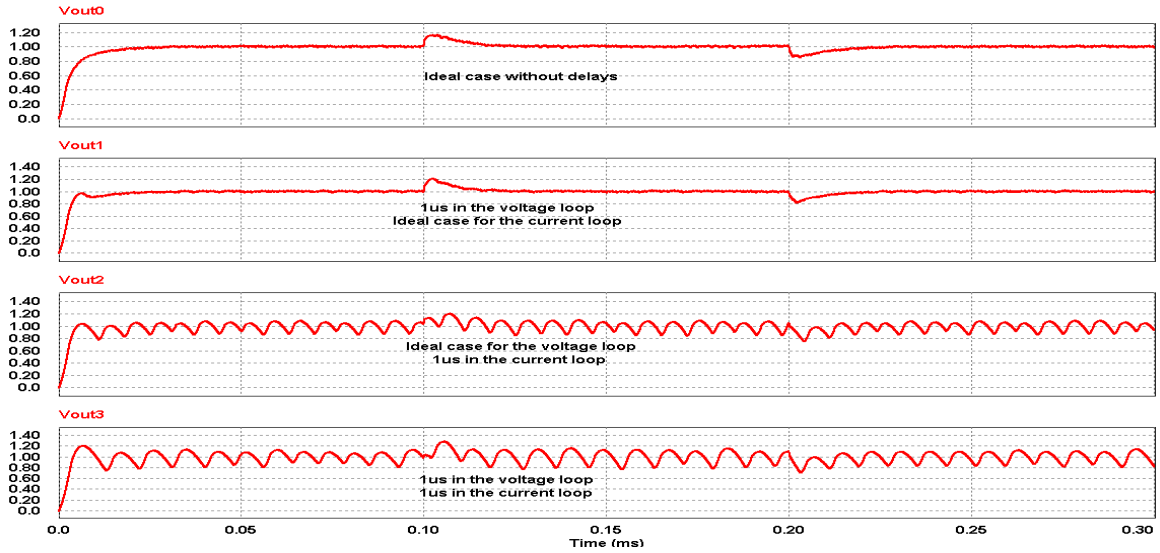


Fig. 4-21 Discrete-time PCMC: Influence of the delay in the output voltage in a 5A load variation

As it can be observed in Fig. 4-21, the delay introduced into the current loop is more critical than the voltage-loop one. This is to some extent usual since current represents the fast dynamics in the energy conversion process whereas the

voltage loop deals with the slow dynamics. For this reason, ADCs in this loop should introduce the minimal possible delay. .

4.3.3.3.1.3 Influence of the sampling frequency in the current loop.

In DVMC, the single feedback loop owns a slow dynamics. As a consequence, sampling frequency should not be necessarily too high for a proper working (the same value for sampling and switching frequency is usually advised although lower rates are permitted). As a matter of fact, this is not true for DCMC because inductor-current progress must be known to be compared with a current reference.

Therefore, a high sampling-frequency for the current loop is required. As a general rule, the inductor current sampling-frequency should be ten times the switching-frequency. This issue with the sampling-frequency is illustrated in the Fig. 4-22 where a detail of the output voltage (when a 5A load variation is produced) is represented.

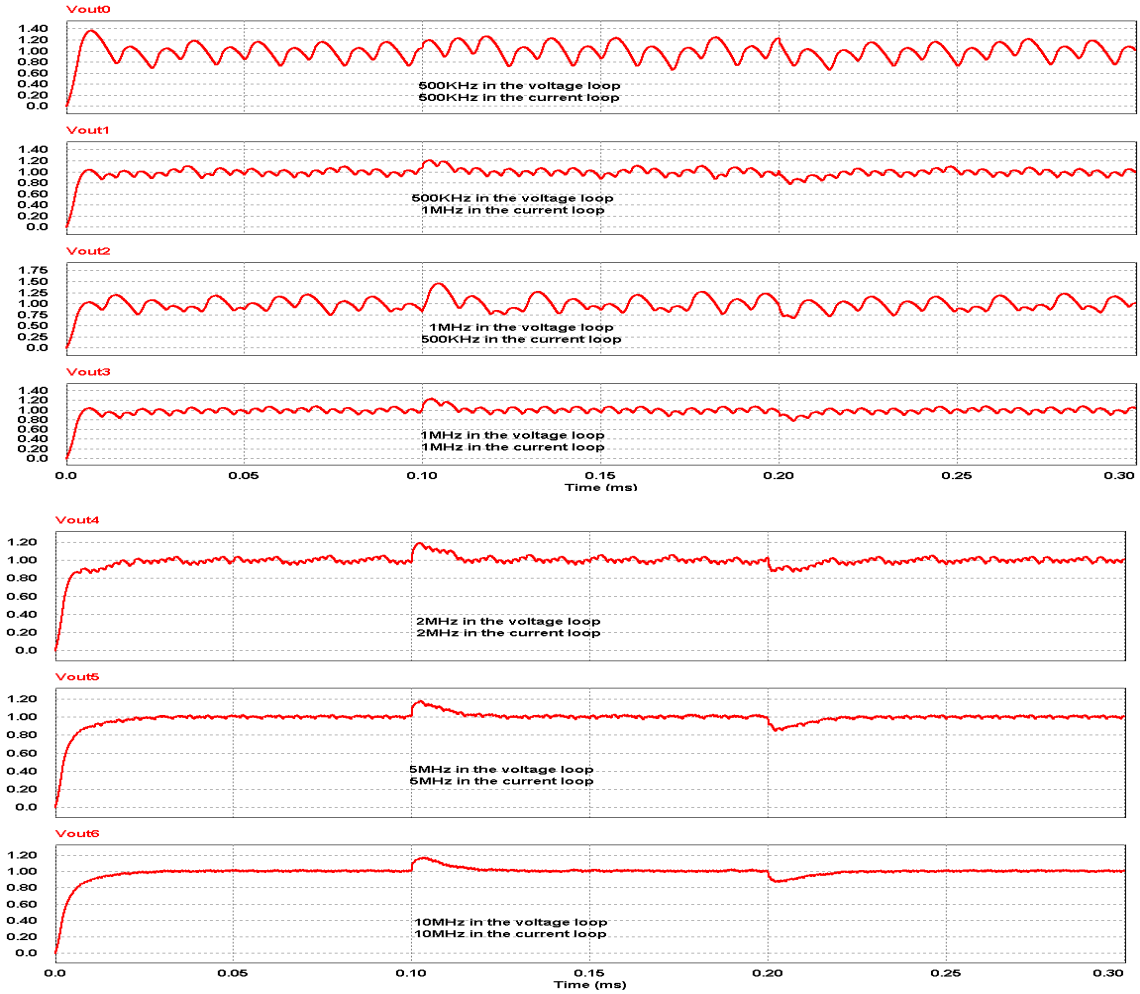


Fig. 4-22 Discrete-time PCMC: Influence of the sampling frequency in the output voltage in a 5A load variation

Thus, it can be also observed in Fig. 4-23 a comparison of the duty-cycle generation for a low-sampling (1MHz) and acceptable sampling-frequency (10MHz) ratio in the current loop. Therefore, the first case reveals how the lack of samples in the sensed inductor-current ramp generates a pulse-skipping effect. That means that some command signals are not generated by the DPWM making that the equivalent switching frequency decreases (1/5 in this case) and weakening the final system behavior as shown in the Fig. 4.23.

In practical terms, the system is only able to work at an effective switching frequency lower than the nominal one and fixed by this new ratio (e.g. the fifth part in this case or 200kHz). On the other hand, if sampling frequency is high enough, the duty-cycle can be generated without problems cycle-by-cycle at the nominal switching frequency (i.e. 1MHz in this case) avoiding undesired pulse-skipping effect.

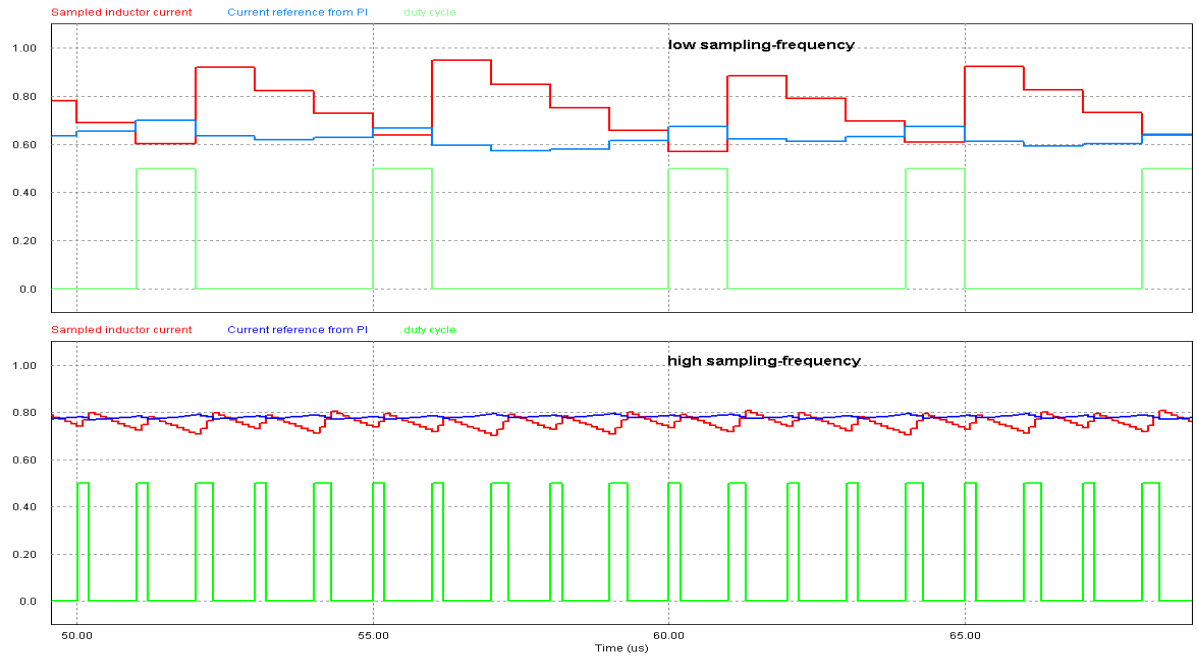


Fig. 4-23 Discrete-time PCMC: Influence of the sampling frequency in the output voltage in a 5A load variation

4.3.3.3.1.4 Influence of the discrete-time power converter model

Thus, as in the DVMC case, several ways are available to find the discrete-time control-to-output voltage transfer function. A simulation example comparing the continuous-time case with the two discrete-time approaches found for DCMC is disclosed in this point. The first discrete-time approach is the one found in (4.36) associated to a ZOH (2nd method) and the second one (3rd method) is achieved

using (4.39). Fig. 4-24 shows minor differences among both discrete-time models and the continuous-time one (1st method). As a result, discrete-time formulation presented in (4.39) gives final performances as satisfactory as the other ones.

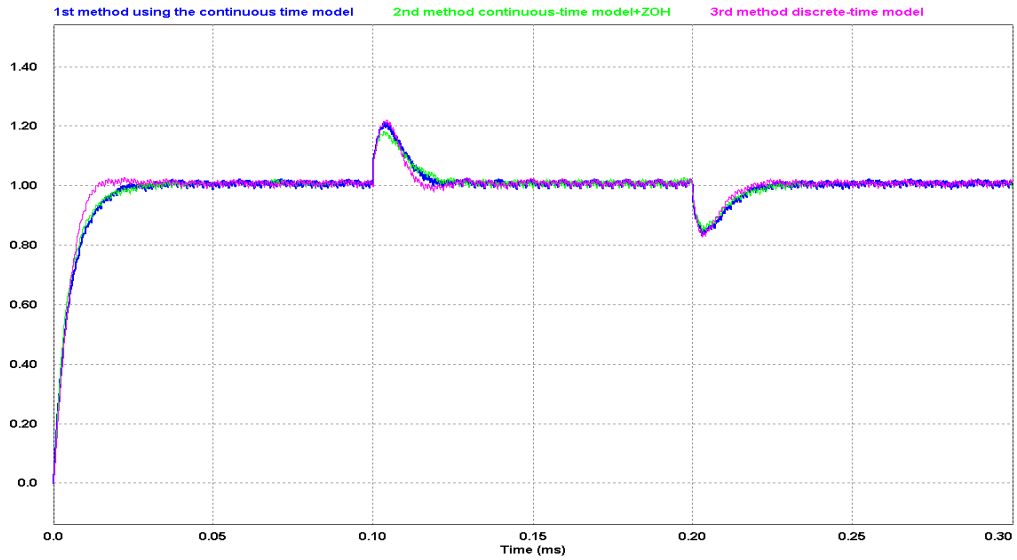


Fig. 4-24 Discrete-time PCMC: Influence of the power converter model in the output voltage in a 5A load variation

4.3.4 Adaptive-control based on Look-up Tables.

Classical Adaptive control in VRs is not normally applied due to its important computational cost. Anyway, some works are found where the digital filter is tuned depending on some pre-stored values in Look-up Tables (LUT). As a consequence, the most efficient set of coefficients is theoretically obtained for different work points of the converter. An example of this kind of regulation is [2.22] where authors presented a DVMC converter based on LUTs.

In relation to the idea of obtaining the most suitable tuning coefficients for the digital filter, classical DVMC can be modified to obtain an adaptive calculation of the duty-cycle of the converter depending on load variations. That means that the digital controller should recover the most performing duty-cycle for each load variation in order to achieve zero-voltage error in steady conditions.

Once, the digital controller had calculated the required duty-cycle, this value is stored in a LUT block. After, the algorithm checks if an inductor-current variation has been produced. This indicates that a new load current has been detected and the system parameters have been changed. Then, a new duty-cycle calculation should be made to reach again the optimal performances.

Differently than in the classical DVMC case where duty-cycle command signal was generated from its last computed value, now, the duty-cycle calculation is obtained thanks to the nearest stocked duty-cycle value corresponding to the last load variation detected by the system.

The algorithm of this control law is presented in Fig. 4-25 and more information can be also found in [4.18] Some simulation and experimental results using this control law are given in chapter five.

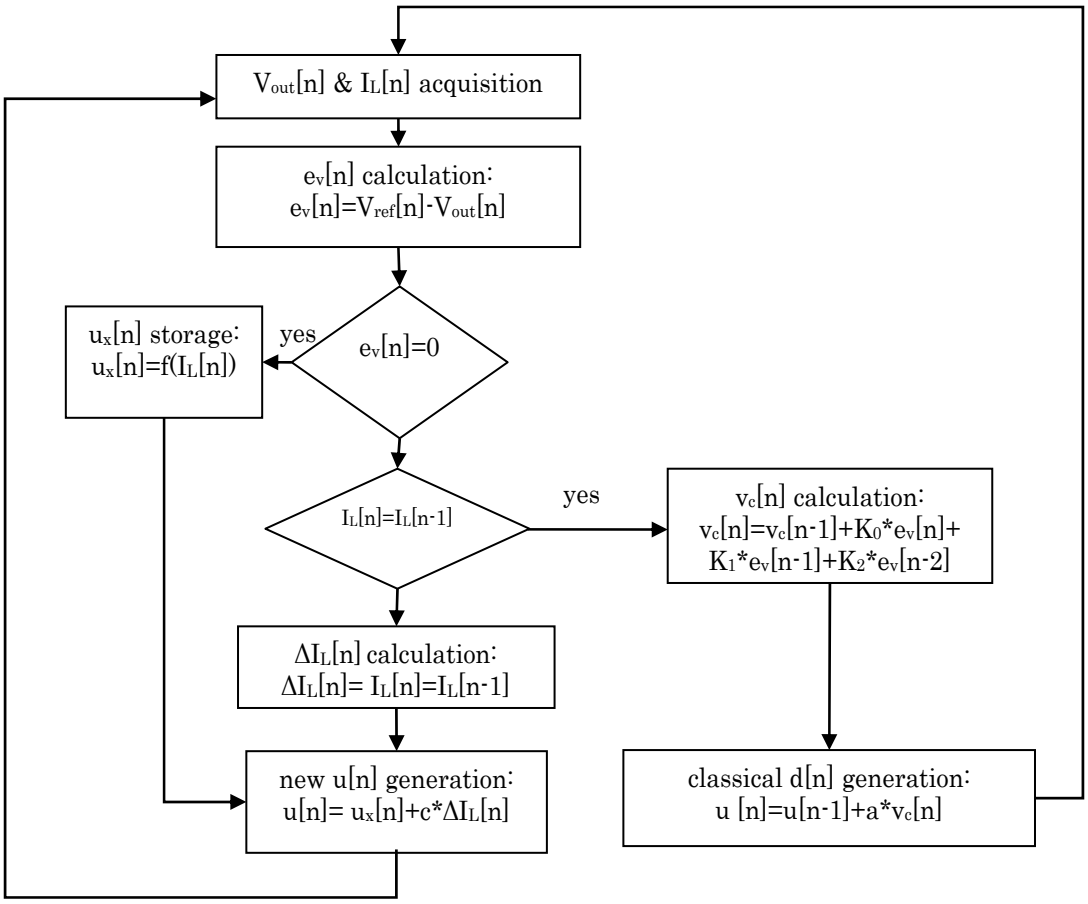


Fig. 4-25 Algorithm of adaptive duty-cycle control law

4.3.5 Predictive Control

In classical predictive control, the user obtains a theoretical cost function based on the differences between the real system and the desired one. Then, this cost function is minimized depending on specific design requirements.

According to this cost function and the desired specifications defining the set-point trajectory, the predictive controller defines the reference trajectories of the state-space converter variables to be followed by our system.

The predictive nature of the digital controller allows calculating ahead of time the trajectories of the state-space variables of the converter from the initial time

until the prediction horizon or final point to attain the desired reference trajectory as it can be observed in Fig. 4-26.

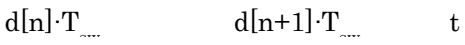


Fig. 4-26 Predictive control principle

The direct approach of predictive digital control applied in DC/DC converters was formulated by the team of the University of Boulder, Colorado in several works [2.24] [4.19] In these publications, the converter trajectories are well known and they are defined using the sampled-time behavior of the inductor current and the output voltage (see Fig. 4-4).

This control law is known as One-Cycle Predictive Current-Mode (OCPC) control and, nowadays, it is the closest approach of continuous-time CPC where inductor current is programmed to follow a reference imposed by the external voltage regulation loop as in the analogue case [4.19] . Thus, the main idea is that inductor current should reach a peak, average or valley reference current in a determined number of cycles. Once the inductor current attains the reference, the current error becomes zero and the system attains the steady-state compensating any possible disturbance produced in the command signal.

The main advantage of this control law is that sampling-frequency might not be as high as in the classical DCMC case to obtain a proper working due to our knowledge if the inductor current. This can be observed in Fig. 4-27 where a comparison between OCPC and DPCMC is established. In this comparison, both techniques have been simulated using a sampling frequency of 1 and 10MHz.

Thus, Fig. 4-27 reveals how OCPC does not need an important sampling-frequency value for a correct working like in the DPCMC case.

In OCPC, inductor current should be sampled in uniformly spaced intervals equal to the switching period and synchronized with the PWM signal for a correct working. Thus, peak-current mode technique can be obtained if the inductor-current ADC is synchronized with the down edge of the PWM signal. Alternatively, valley current is obtained using the rising edge of the PWM. Otherwise, average current is achieved when ADCs takes the sample at either the instant $\frac{d[n]}{2}\cdot T_{sw}$ or $d[n]+\frac{1-d[n]}{2}\cdot T_{sw}$.

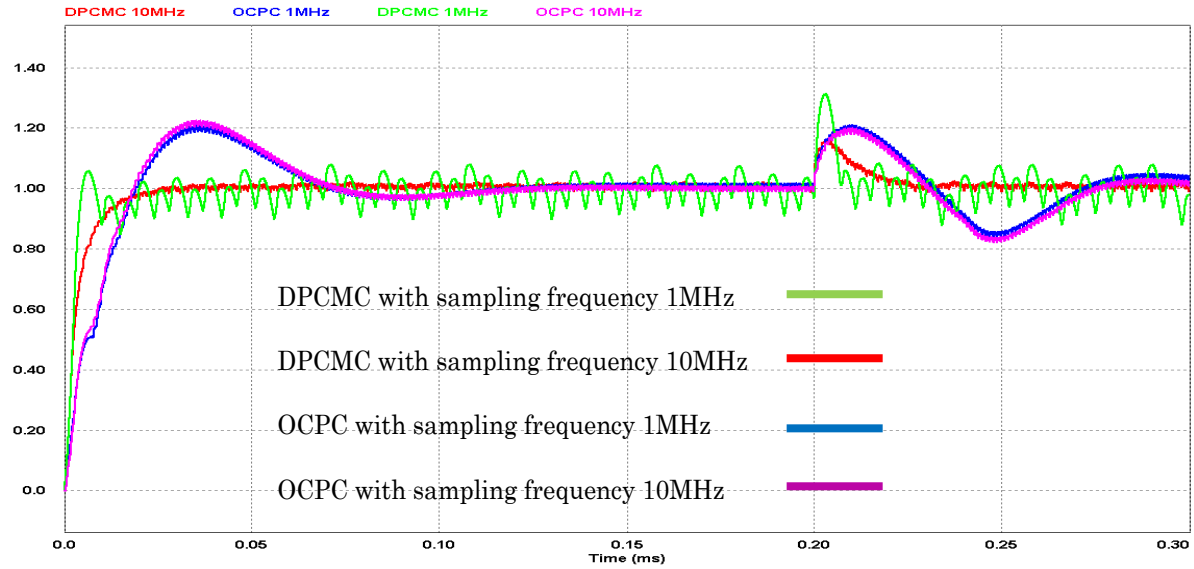


Fig. 4-27 Comparison of OCPP and DPCMC for different sampling frequencies.

However, as in the DPCMC case, peak, average and valley current need their respective compensation slopes [2.12] . Therefore, the digital control laws for valley and peak-current predictive control are illustrated in next equations (the complete formulation is shown in points 8.2.2.1 and 8.2.2.2 respectively). The block diagrams for both digital control laws are shown in Fig. 4-28.

$$d[n+1]=d[n]+\underbrace{\frac{L_{out}}{V_{in}\cdot T_{sw}}}_{k_i}\cdot\left(\underbrace{i_c[n]-i_L[n]}_{e_i}\right)\quad\text{(valley)} \tag{4.41}$$

$$d[n+1]=\underbrace{\frac{L_{out}}{(V_{in}-V_{out})\cdot T_{sw}}}_{k_i}\cdot\left(\underbrace{i_L[n+1]-i_L[n]}_{E_i}\right)+\frac{V_{out}}{V_{in}-V_{out}}\cdot(1-d[n])\quad\text{(peak)} \tag{4.42}$$

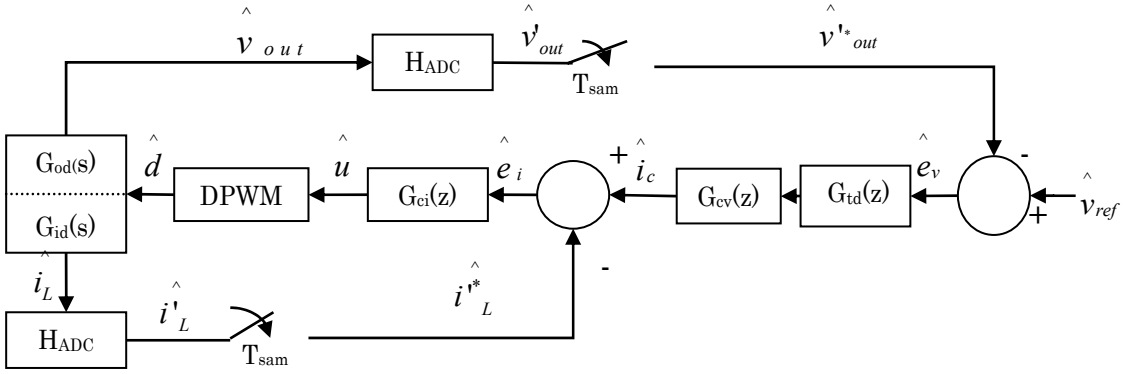
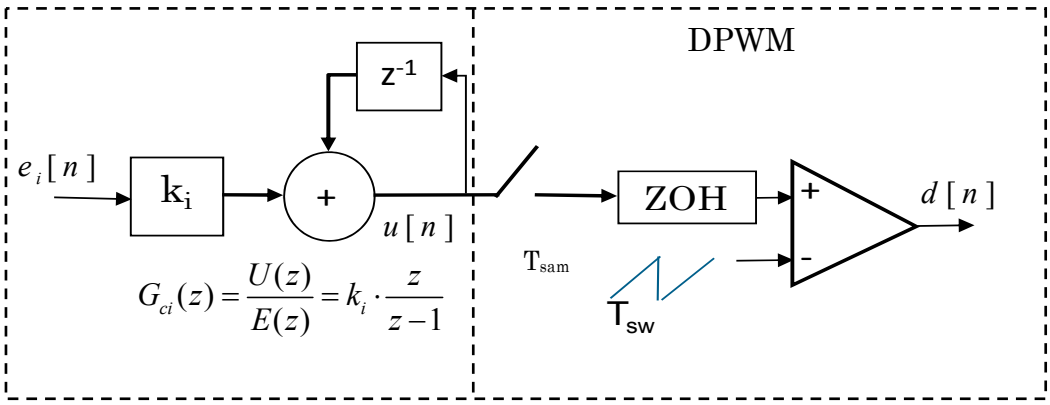


Fig. 4-28 Diagram block model of OCPC control law

As it can be observed in (8.75), this control law depends on some converter parameters (inductance, switching period and input voltage) which should be known a priori. These parameters establish a static gain which determines the final variation to the duty-cycle command, i.e. the change in control effort signal [4.19] . Therefore, the predictive current module $G_{ci}(z)$ is shown in Fig. 4-29.



$$G_{ci}(z) = \frac{U(z)}{E(z)} = k_i \cdot \frac{z}{z-1} \quad (4.43)$$

Fig. 4-29 OCPC: One-cycle predictive control action in the duty-cycle generation

4.3.5.1 One-Cycle Predictive Current-Mode Control example

An example of OCPC control law is illustrated in this point using equations (4.41) and (4.42) for valley and peak current respectively. The design specifications of this example are the same that were used to develop our second experimental prototype (see point 5.3).

Furthermore, the control-to-output voltage transfer function presented in (4.40) is used in this example. Referring the digital filter of the external voltage regulation loop, the "setpoint weighting" algorithm has been employed. Finally, the coefficients of this filter are obtained using the pole-zero matching method following the design guidelines imposed in [4.17] and obtaining:

$$
\begin{aligned}
&u[n] = P[n] + I[n] + D[n] \\
&with: \quad \mathrm{P[n]}=0,2080 \cdot \left(V_{ref}[n] - V_{out}[n]\right) \\
&\qquad \mathrm{I[n]}=I[n-1] + 0,0010 \cdot \left(V_{ref}[n] - V_{out}[n]\right) \\
&\qquad \mathrm{D[n]} = 0,8848 \cdot D[n-1] - 0,5521 \cdot \left(V_{out}[n] - V_{out}[n-1]\right)
\end{aligned} \tag{4.44}
$$

The simulation model for this valley-current OCPC is given in Fig. 4-30 and its closed-loop pole-zero map is represented in Fig. 4-31 additionally.

In this last result, the stability of the system is validated. Moreover, results for valley and peak current mode are shown respectively in Fig. 4-32 and 4-33 where the output voltage and current for a 5A load variation is simulated.

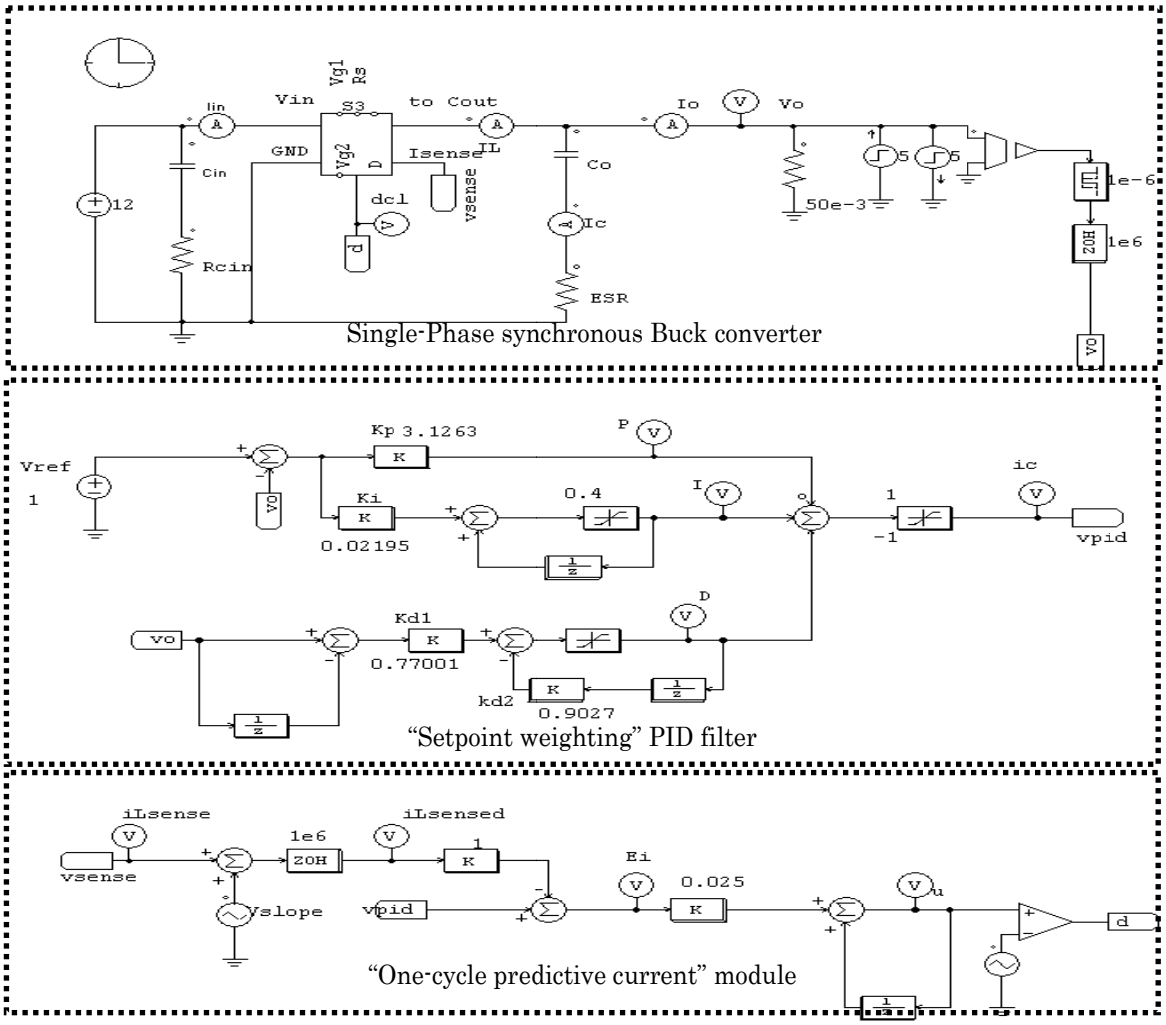


Fig. 4-30 OCPC simulation model

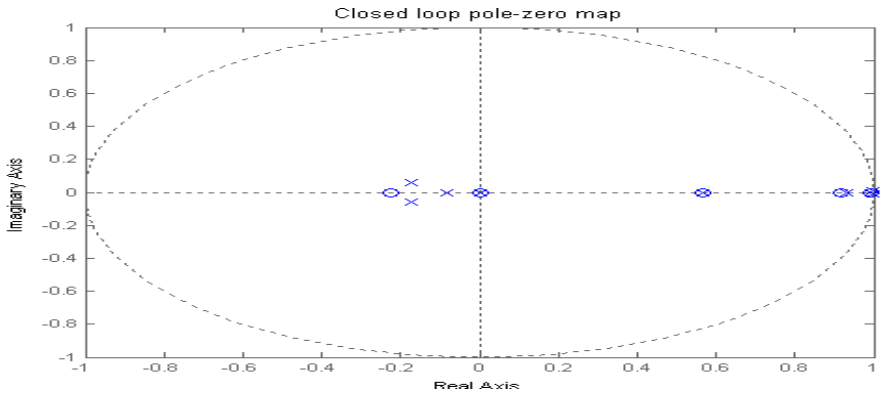


Fig. 4-31 OCPC closed-loop pole-zero map

In addition, the output command signal of the external voltage loop and the sensed inductor reference are compared in the bottom trace of Fig. 4-32 and Fig. 4-33. The result of this comparison is the input signal of the predictive current module. Thus, the duty-cycle generation for the peak-current case is shown in Fig. 4-34. In short, this control law is equivalent to Digital Peak Current-Mode since the maximal inductor current value is fixed by the external voltage loop.

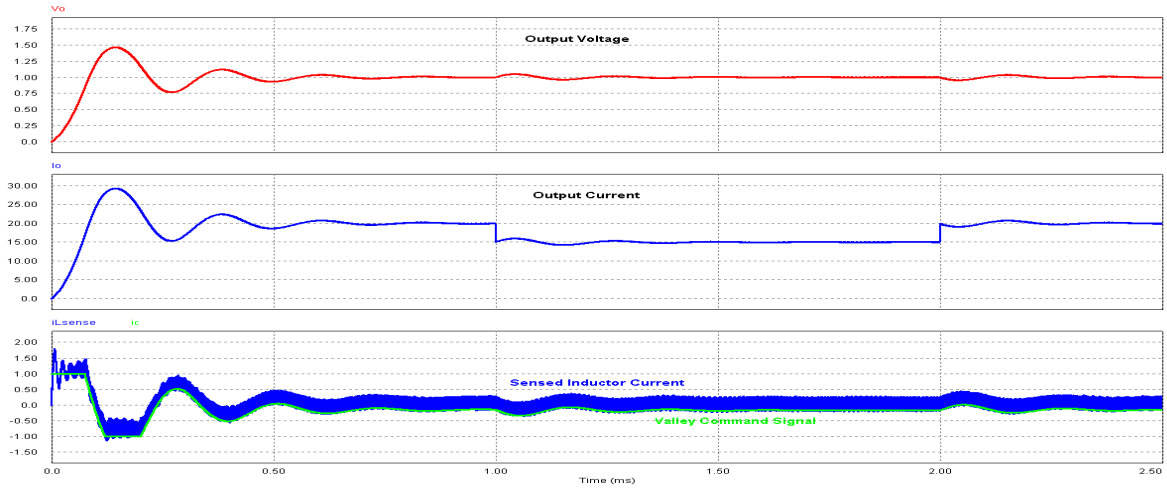


Fig. 4-32 Simulation of valley OCPC for a 5A load step change.

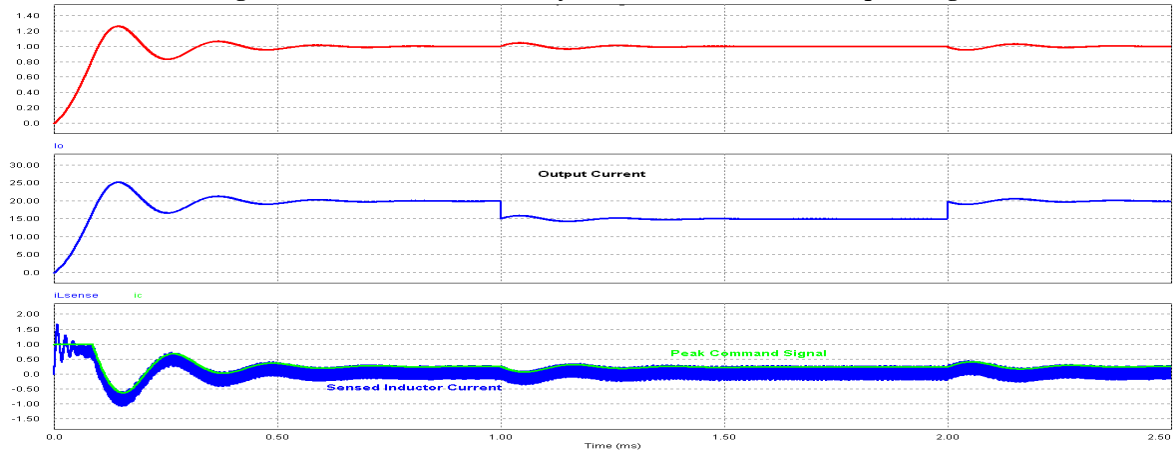


Fig. 4-33 Simulation of peak OCPC for a 5A load step change.

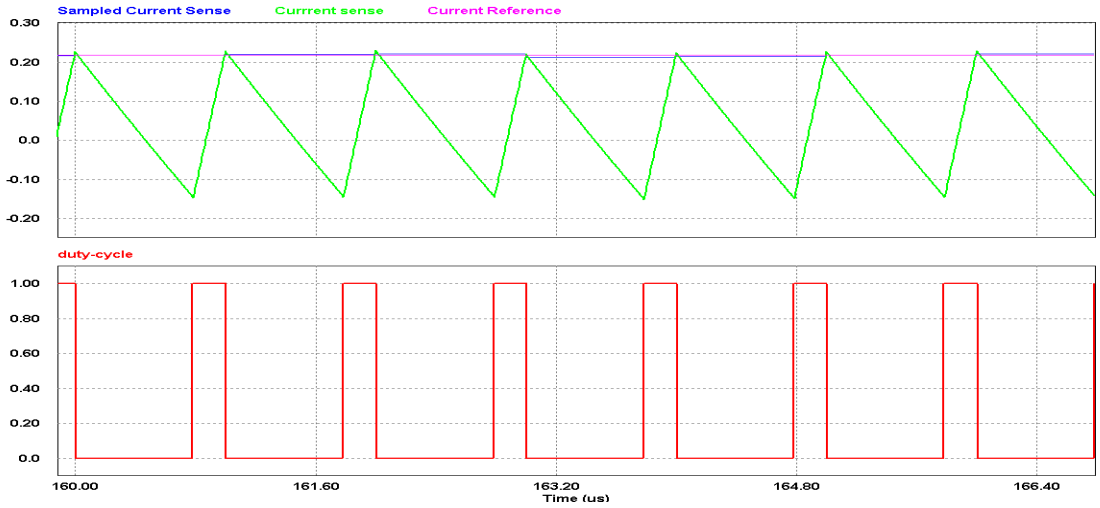


Fig. 4-34 OCPC: duty-cycle generation

4.3.6 Feedforward regulation

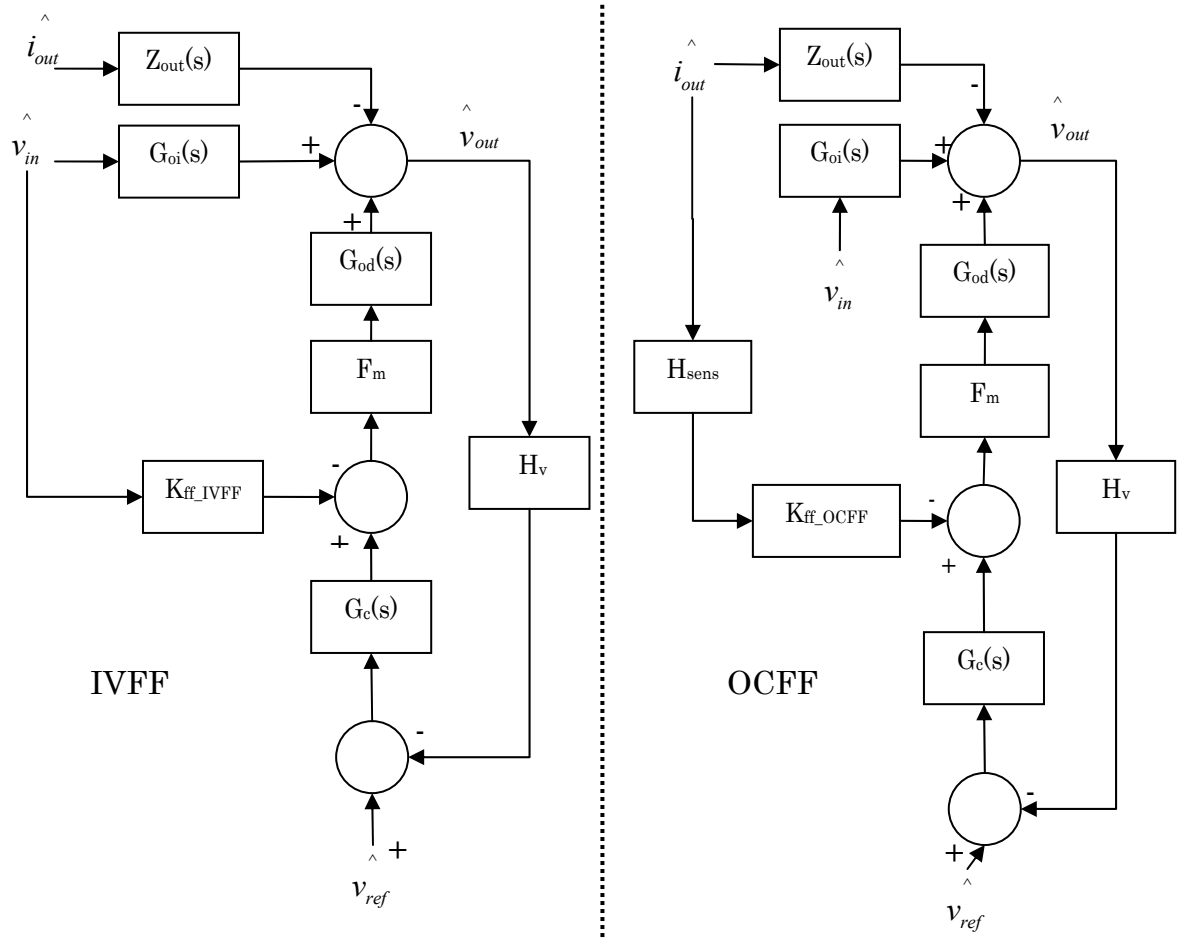
4.3.6.1 Introduction

Feedforward compensation (FF) is employed usually to eliminate or to reduce the effects of source and load disturbances in the converter output voltage. Thus, it has been illustrated in previous points how the control-to-output voltage transfer function of the PWM-controlled Buck converter working in CCM conditions depends on the input voltage (for the VMC case) and on load changes.

In general, FF compensation improves line and load regulation obtaining enhanced steady and dynamic performances. FF general block diagram is represented in Fig. 4-35 where two types of FF regulation for PWM-controlled converters are found: Input-Voltage Feedforward (IVFF) [4.1] and Output-Current Feedforward (OCFF) [4.20]

In IVFF, the PWM gain varies proportionally to the input voltage. Thus, the loop gain is constant for the whole range of input voltages becoming independent of this parameter. In practical terms, the duty-cycle varies inversely with the input voltage keeping constant the product $D \cdot T_{sw} \cdot V_{in}$ and giving constant gain to the input-to-output voltage transfer function [4.21] . Thus, input noise is reduced considerably and line regulation is augmented noticeably.

Otherwise, OCFF method is useful to improve the transients states of the converter, i.e. to get better dynamic responses face up load-current variations. This method is based on the minimization of the open-loop output impedance of the converter to reduce load disturbances effects [4.22] .



Where:

Z_{out}: Open-loop output impedance
G_c: Compensation network
G_{oi}: Input-to-output voltage transfer function
H_V: Output voltage sensor gain
F_m: PWM modulator gain
K_{ff} : feedforward transfer function
G_{od}: Control-to-output voltage transfer function
H_{sens}: Output-current sensor gain

Fig. 4-35 Feedforward block diagram: IVFF (left), OCFF (right)

4.3.6.2 Input Voltage Feedforward

IVFF is applied mainly in VMC to improve the line regulation of the converter compensating input-voltage disturbances. In contrast, it is not normally applied in CMC because of the inherent rejection of CMC to input-voltage disturbances.

Nevertheless, some designers apply this FF technique in CMC to improve the system stability [4.23] . Then, Fig. 4-35 allows finding the output voltage small-signal value which depends on the input-voltage, source and reference disturbances:

$$\hat{v}_{out}(s)=\hat{v}_{in}(s)\cdot\left(\frac{G_{oi}(s)-K_{ff\_IVFF}\cdot F_m\cdot G_{od}(s)}{1+G_c(s)\cdot F_m\cdot G_{od}(s)\cdot H_V}\right)-\hat{i}_{out}(s)\cdot\left(\frac{Z_{out}(s)}{1+G_c(s)\cdot F_m\cdot G_{od}(s)\cdot H_V}\right)+ \quad (4.45)$$
$$\hat{v}_{ref}(s)\cdot\left(\frac{G_c(s)\cdot F_m\cdot G_{od}(s)}{1+G_c(s)\cdot F_m\cdot G_{od}(s)\cdot H_V}\right)$$

Examining (4.45), it can be observed that the first term is only affected by input-voltage disturbances. Thus, this term should be cancelled to reach a good input-noise rejection:

$$G_{oi}(s) - K_{ff\_IVFF} \cdot F_m \cdot G_{od}(s) = 0 \tag{4.46}$$

$$\frac{G_{oi}(s)}{G_{od}(s)} = K_{ff\_IVFF} \cdot F_m \tag{4.47}$$

The required value of K_{ff_IVFF} for the Buck converter is obtained as follows:

$$K_{ff\_IVFF} \cdot F_m = \frac{D}{V_{in}} \tag{4.48}$$

A criteria to design K_{ff_IVFF} is to maximize the open-loop gain at the input PWM when the input voltage is maximal [4.1]

$$F_m(s) = \frac{V_{inMAX}}{(V_{inMAX} - V_{inMIN}) \cdot V_{in}(s)} \tag{4.49}$$

Thus, the new output voltage-to-control transfer function including IVFF is:

$$G_{od}^{IFFF}(s) = \frac{V_{inMAX}}{(V_{inMAX} - V_{inMIN}) \cdot V_{in}(s)} \cdot G_{od}(s) \tag{4.50}$$

To illustrate this point, the FF gain has been added to the example introduced in point 4.3.2.4. This is shown in Fig. 4-36.

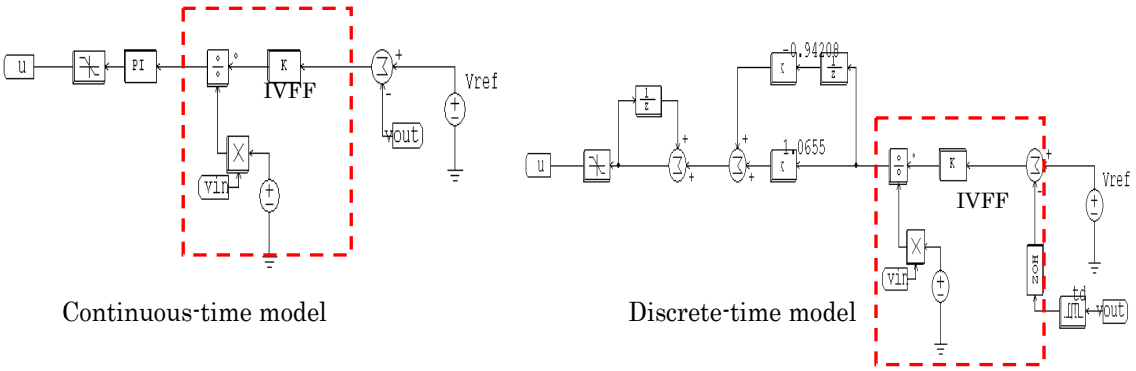


Fig. 4-36 Voltage Mode Controlled-Buck with Input Voltage Feedforward

Fig. 4-37 shows the open-loop frequency responses for several input voltages. Thus, this gain is kept constant when IVFF is used despite of input-voltage variations. In contrast, this is not achieved without IVFF as it is illustrated in the top side of Fig. 4-37. Concerning to transient responses, they are almost equivalent for the whole range of input-voltage using IVFF as shown in the Fig. 4-38 where a 5A load variation is represented. In short, IVFF is quite interesting for VRs converters because it minimizes the influence of the input voltage in our

design obtaining an enhanced line regulation and decreasing considerable the effects of input-voltage disturbances.

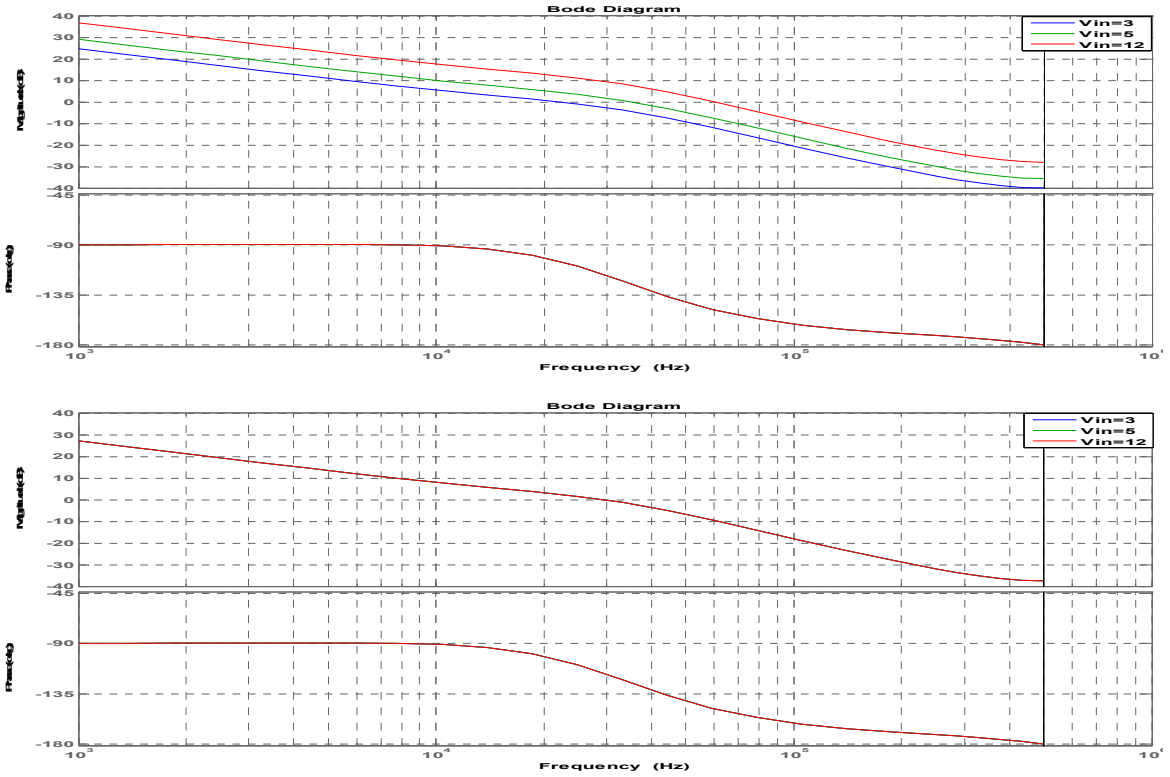


Fig. 4-37 Open-loop gain Bode Diagram: without IVFF (top) and with it (bottom)

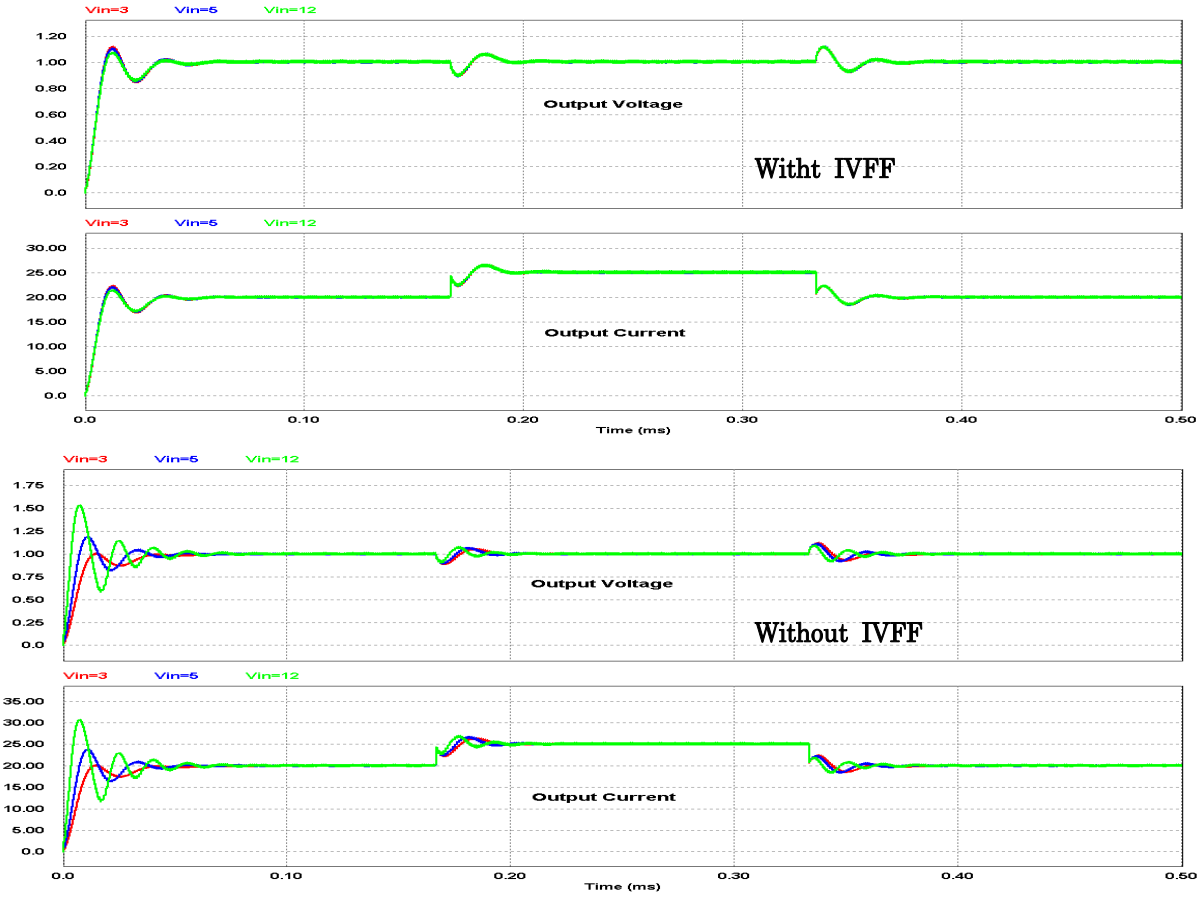


Fig. 4-38 Transient response for different input-voltages: 3V (red), 5V (blue), 12V (green) during a 5A load variation

4.3.6.3 Output Current FeedForward

Load variations are quite usual in VRs and they modify considerably the converter behavior because they are not detected by the internal current loop.

Thus, OCFF is applied in CMC to improve the transient response against load variations. In contrast, some works have verified that OCFF is not useful in VMC due to the resonant behavior of the output impedance [4.24]

Similarly than in the IVFF case, the small-signal output voltage value for OCFF regulation is:

$$\hat{v}_{out}(s)=\hat{v}_{in}(s)\cdot\left(\frac{G_{oi}(s)}{1+G_c(s)\cdot F_m\cdot H_V\cdot G_{od}(s)}\right)+\hat{i}_{out}(s)\cdot\left(\frac{K_{ff\_OCFF}\cdot H_{sens}\cdot F_m\cdot G_{od}(s)-Z_{out}(s)}{1+G_c(s)\cdot F_m\cdot H_V\cdot G_{od}(s)}\right)+ \hat{v}_{ref}(s)\cdot\left(\frac{G_c(s)\cdot F_m\cdot G_{od}(s)}{1+G_c(s)\cdot F_m\cdot H_V\cdot G_{od}(s)}\right) \quad (4.51)$$

As in the previous case, the term depending on the output-current disturbance should be cancelled:

$$K_{ff\_OCFF}\cdot H_{sense}\cdot F_m\cdot G_{od}-Z_{out} \quad (4.52)$$

$$K_{ff\_OCFF}=\frac{Z_{out}}{H_{sens}\cdot G_{od}\cdot F_m} \quad (4.53)$$

In our case a K_{ff_OCFF} values among 0.1 and 1 provides minimal output impedance owning a value equals to [4.24]

$$Z_{out}=H_{sens}\cdot G_{od}\cdot F_m \quad (4.54)$$

Next example illustrates the effects of the addition of OCFF in an Average-DCMC converter. The digital implementation of this technique is shown in Fig. 4-39 and results for a 20A load variation are exposed in Fig. 4-40. In this last figure, it can be stated how transient response is improved thanks to the addition of OCFF loop.

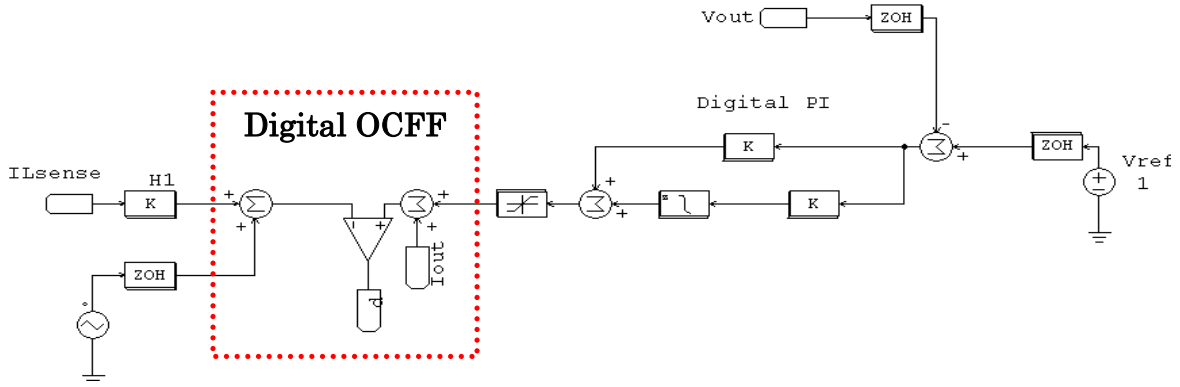


Fig. 4-39 Digital OCFF loop

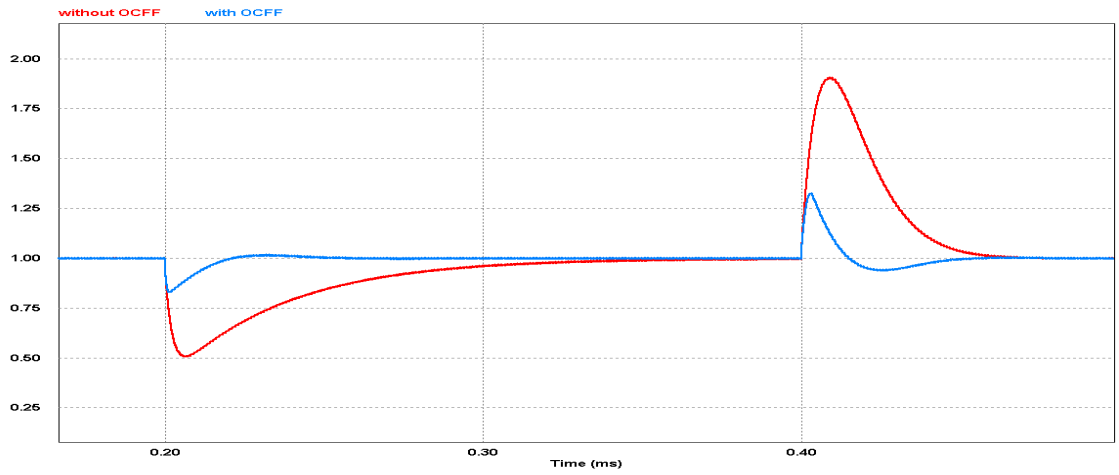


Fig. 4-40 Digital Average-Current Mode Control + OCFF for a 20A load variation

4.3.7 Current-Sharing

4.3.7.1 Introduction

An equilibrated power distribution among phases, i.e. Current-Sharing (CS), is required in multiphase interleaved converters to obtain the intrinsic advantages of this architecture.

Furthermore, CS prevents inductor saturation and reduces thermal stress enlarging the life of the power converter. Theoretically, if symmetric layouts for each phase are used, almost identical propagation times and equivalent trace resistances may be obtained and, therefore, uniform current distribution among phases. In practical terms, commutation cells of a multiphase converter are not perfectly alike.

There are two factors causing non-equilibrated current distribution in steady-state. The first source of mismatching is the tolerances of the components involving each phase. For instance, trace inductors, drain-to-source MOS and inductance parasitic resistances are not exactly equal for each phase causing some differences in the impedance per phase. The second unbalance factor is caused by disturbances affecting the duty-cycles of each phase. These undesired disturbances may cause that each phase own different duty-cycles [4.25]

As a result, several compensation techniques to balance correctly inductor currents are found in literature. These methods are classified into three major groups: "Voltage-Droop" (VD) methods, "Active Current-Sharing" (ACS) techniques and CPC modulations. In general, ACS is the most widespread CS schema.

4.3.7.2 Voltage-Droop Current Sharing

VD methods are based on the variation of the phase impedance to compensate possible divergences among them. Thus, there are several ways to generate the required VD. The simplest method is to try to design the multiphase converter with equivalent impedances per phase. In practical terms, this is hard to achieve due to tolerances of the components. In consequence, this method is used only in non-tight regulated applications. Another variation consists on placing a serial resistor per phase to compensate their impedance mismatching. This second method contains a major drawback due to the power dissipation caused by this series resistor. In short, this technique is not applicable in high-current multiphase converters like VRs.

Nowadays, VRs require variable output impedance according to "loadline" specifications as it is illustrated in Fig. 4-41. As a matter of fact, the higher output current required, the lower output voltage delivered to the load according to the following linear relation:

$$V_{loadline} = V_{out} - I_{out} \cdot R_{droop} \tag{4.55}$$

Then, the output impedance in VRs should be modified depending on load variations. As a general rule, loadline regulation is used for a double reason. The first goal is to deliver a constant supply power to the load modifying the output voltage according to load current changes. The second aim is to reduce transient voltage peaks when a load variation is produced [4.26]

Anyway, this method cannot be independently used to achieve CS and it should be added to some kind of ACS method or CPC to achieve uniform current distribution among phases.

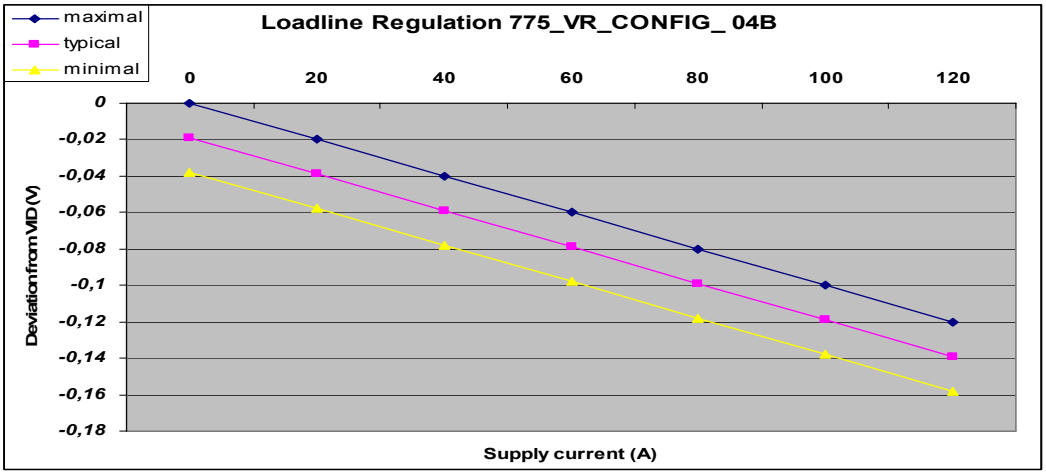


Fig 4-41 Loadline Regulation for 775_VR_CONFIG socket.

4.3.7.3 Active Current-Sharing

ACS varies slightly the duty-cycle of each phase to equilibrate their corresponding inductor currents. Previous studies have verified that ACS obtains enhanced current distribution and output voltage regulation compared with others CS techniques.

ACS is normally achieved thanks to an additional loop associated to one or more principal regulation loops. This supplementary loop imposes almost identical inductor currents for all phases.

ACS can be obtained using two different topologies [4.27] . First architecture is known "Democratic active Current Sharing" (DCS) scheme and the second one is based on a "Master–Slave" (MS) design. Thus, the major difference between both schemas is the weight ($\mu_{1\text{-}n}$) assigned to each phase. Some practical implementations of ACS and MS techniques and their simulation results can be found in the Appendix A. Both ACS working principles associated to VMC are shown in Fig. 4-42.

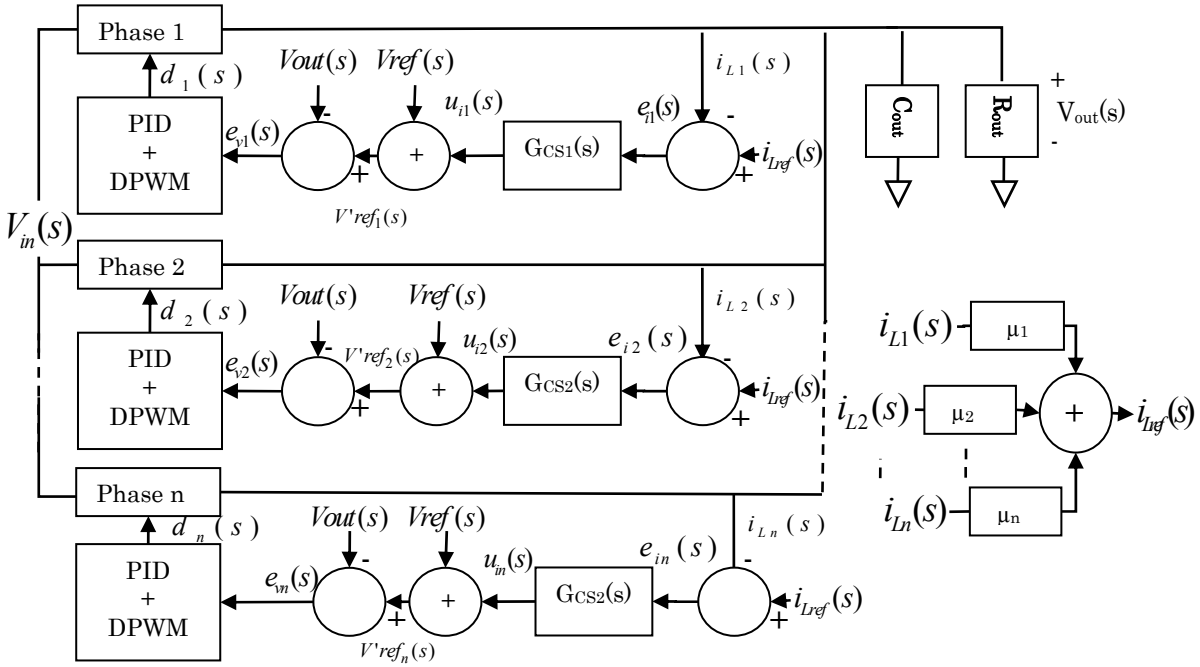


Fig. 4-42 General schema of VMC for a n-phased parallel power converter associated to individual ACS loop for each phase.

However, ACS can be achieved using two approaches. The first topology consists on to design individual CS loops for each phase, i.e. particular compensation networks for each phase. This configuration lets some redundancy in case of failure despite of a higher complexity. This topology is presented in Fig.

4-42 as a general schema of ACS for DCS and MS principles. This architecture is also shown in the left side of Fig. 4-43 for DCS associated to VMC and in the Fig. 4-44 for DCS associated to CMC. These concepts are also functional for MS+VMC and MS+CMC respectively changing the weight of coefficients per phase as it is exposed in next points.

On the other hand, ACS can be also used associated to a single compensation network as it is shown in the right side of the Fig. 4-43 (for DCS+VMC). Then, the output of the common compensation network is modified according to the current mismatch error ($e_{i_L i}$) for each phase in its corresponding CS loop. Thus, this slight modification of the command reference per phase origins different duty cycles in each phase achieving uniform current distribution among phase. On the whole, this approach simplifies considerably the complexity of the system.

4.3.7.3.1 Democratic Current-Sharing

DCS does not discern a "privileged" phase giving identical weights to each phase. Therefore, DCS imposes equal inductor currents among phases by means of a common inductor current reference (i_{Lref}). This reference is imposed to be the average inductor current circulating through the power converter.

$$i_{Lref}(s) = \sum_{i=1}^{n} i_{Li}(s) \cdot \mu_i \tag{4.56}$$

With:

$$\sum_{i=1}^{n} \mu_i = 1/n \tag{4.57}$$

Nevertheless, DCS should be associated with VMC and CMC to complete a full regulation system using individual or common compensation networks as it has been commented in previous point. Thus, DCS can be linked to VMC with individual CS loops as it is shown in the right side of the Fig. 4-43. Hence, each DCS loop works as follows. First of all, current mismatch error signals (e_{i_L}) should be calculated for each phase as follows:

$$\underset{i=1}{\overset{n}{e_{i_L i}}}(s) = i_{L_{ref}}(s) - i_{L_i}(s) \tag{4.58}$$

After, this current error signal is introduced in some kind of compensator (this step is not always required) to create a mismatch command variable.

$$\overset{n}{\underset{i=1}{\hat{u}_{i_i}}}(s) = G_{cs_i}(s) \cdot e_{i_L i}(s) \tag{4.59}$$

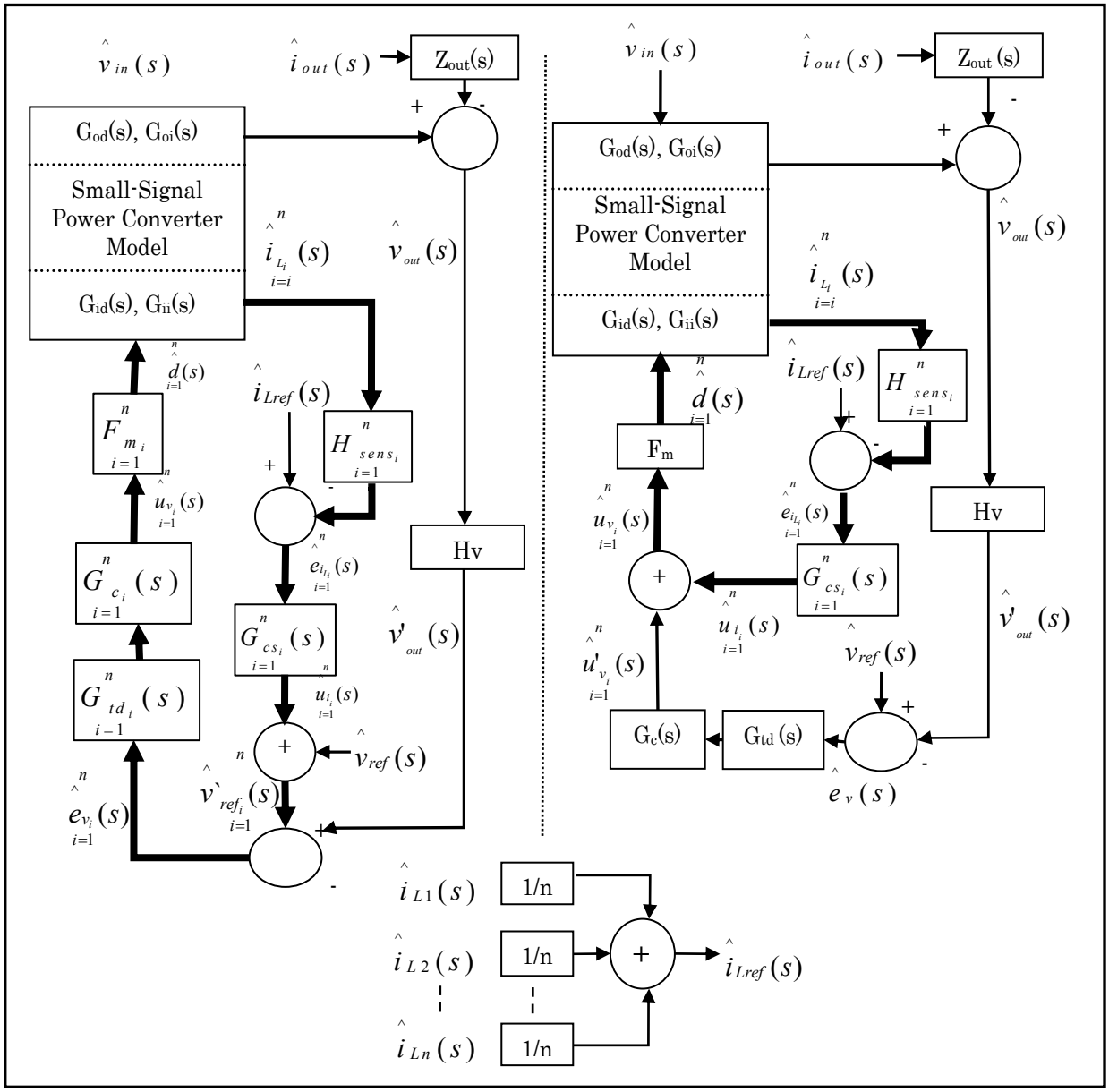


Fig. 4-43 Democratic Current Sharing using Voltage-Mode Control for an n-phased parallel power converter with individual (left) and common (right) compensator network

This mismatch command variable is added to the general voltage reference of the external loop in order to take into account possible divergences in the inductor current in each phase. In this point, different common voltage references are introduced in each single compensation loop as follows:

$$\overset{n}{\underset{i=1}{V'_{ref\,i}}}(s) = V_{ref}(s) + u_{i_i}(s) \tag{4.60}$$

Beyond this point, the voltage regulation of each phase becomes standard as it has been explained in point 4.3.2 with the difference that an individual voltage

regulation is completed for each phase. These individual compensation loops generate slight differences in the final duty-cycle of each phase to compensate the unbalanced currents. Hence:

$$\overset{n}{\underset{i=1}{u_{v_i}}}(s) = G_{c_i}(s) \cdot G_{td_i}(s) \cdot \left(V'_{ref\,i}(s) - V_{out}(s) \right) \tag{4.61}$$

And:

$$\overset{n}{\underset{i=1}{d_i}}(s) = u_{v_i}(s) \cdot F_{m_i} \tag{4.62}$$

In a different way, the working principle changes if a common voltage compensation network is used for all phases. In this approach, first steps are the same that those exposed in (4.56) to (4.59). Now, the mismatch command variable is added to the output of the common voltage compensation network $u'_{Vi}(s)$ to create different command signals for the PWM.

$$\overset{n}{\underset{i=1}{u_{v_i}}}(s) = \left(u'_{v_i}(s) + u_{i_i}(s) \right) \tag{4.63}$$

With

$$\overset{n}{\underset{i=1}{u'_{v_i}}}(s) = G_c(s) \cdot G_{td}(s) \cdot (V_{ref}(s) - V_{out}(s)) \tag{4.64}$$

Finally, these different command signals are introduced in the PWM to generate the duty-cycles per phase as it has been shown in (4.62). Both DCS schema associated to VMC are shown in Fig. 4-43.

On the other hand, CMC can be also used individually or with a common voltage compensator as it is illustrated in Fig. 4-44 and Fig. 4-45 correspondingly. The main difference is the addition of inner current loops and, therefore, inductor-current regulation. Thus, if individual CS loops are used, equations (4.56) to (4.60) can be also used to find new individual voltage references for external voltage loops. Now, the command signal required for the DPWM is:

$$\overset{n}{\underset{i=1}{u_{v_i}}}(s) = i_{c_i}(s) - i'_{L_i}(s) \tag{4.65}$$

With:

$$\overset{n}{\underset{i=1}{i_{c_i}}}(s) = H_{iv_i}(s) \cdot G_{c_i}(s) \cdot G_{td_i}(s) \cdot \left(V'_{ref\,i}(s) - V_{out}(s) \right) \tag{4.66}$$

$$\hat{i}'_{\substack{L_i \\ i=1}}^{n}(s) = H_{e_i}(s) \cdot H_{sens_i} \cdot i_{Li}(s) \tag{4.67}$$

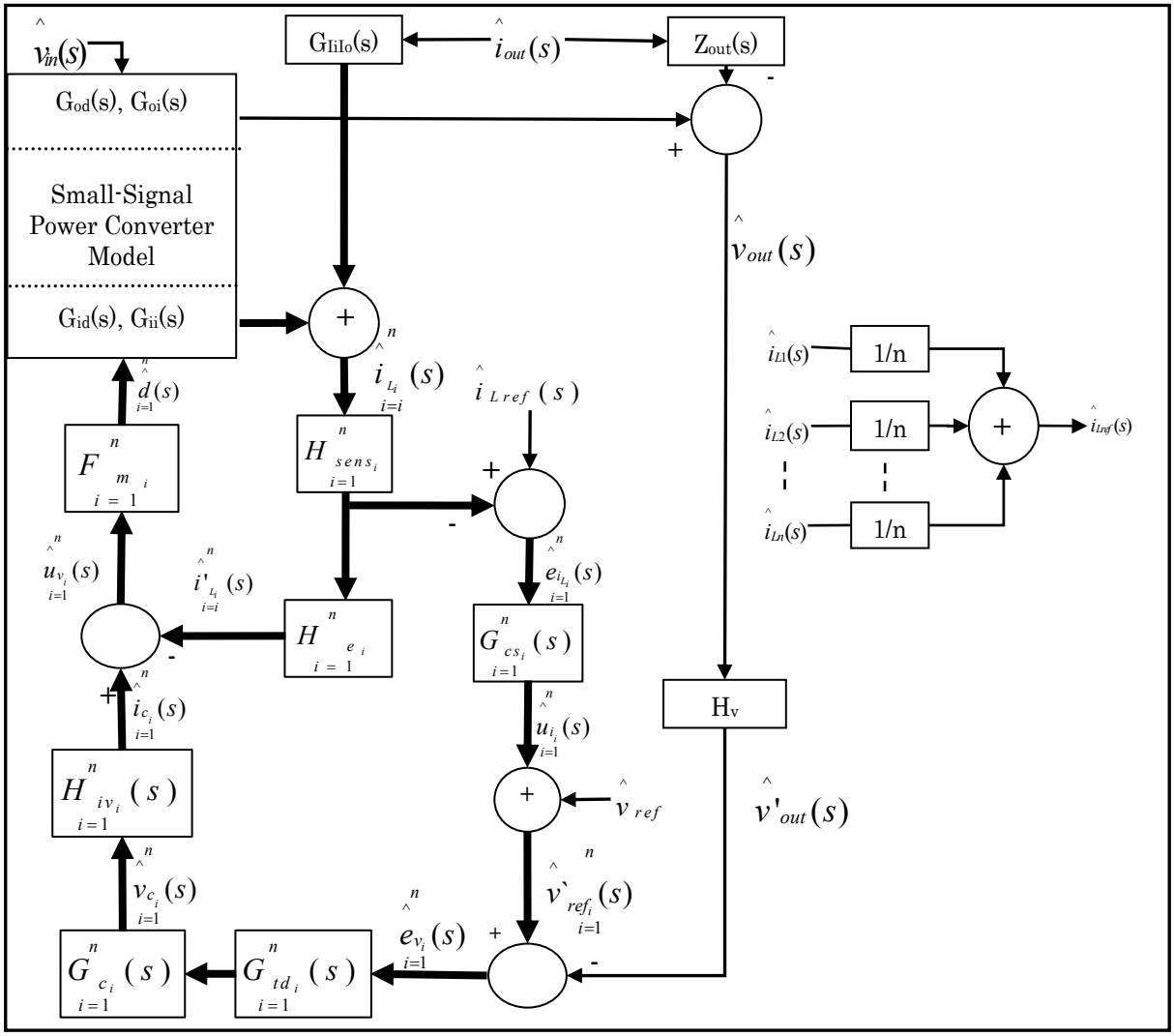


Fig. 4-44 DCS using CMC for a n-phased parallel with individual CS loops

In contrast, if a common voltage compensator network is used to achieve individual DCS loops, the current reference for the inner voltage loop is:

$$\hat{i}'_{\substack{c_i \\ i=1}}^{n}(s) = \hat{i}_c(s) + \hat{u}_{i_i}(s) \tag{4.68}$$

With:

$$\hat{i}_c(s) = H_{iv}(s) \cdot G_c(s) \cdot G_{td}(s) \cdot \left(V_{ref}(s) - V_{out}(s)\right) \tag{4.69}$$

And the command signal for the DPWM is:

$$\hat{u}_{\substack{v_i \\ i=1}}^{n}(s) = \hat{i}'_{c_i}(s) - \hat{i}'_{L_i}(s) \tag{4.70}$$

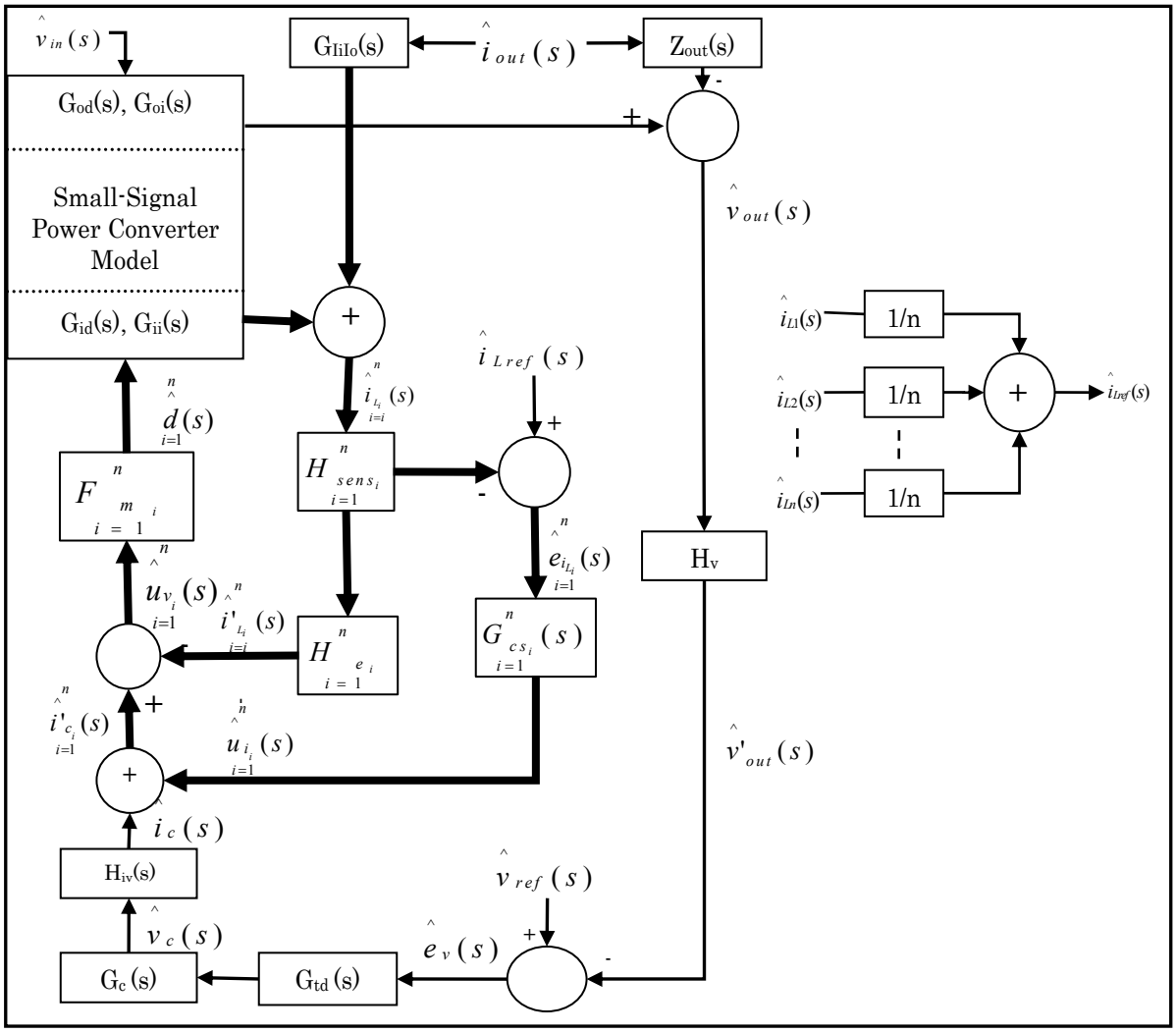


Fig. 4-45 DCS using CMC for a n-phased parallel with common voltage compensator

4.3.7.3.2 Master-Slave Current-Sharing

Some power converters do not require identical weight for each phase as happens in DCS. Thus, MS topology concedes different weights for each branch.

Then, the phase defined with the higher weight is the current reference or master phase for the global system. The weight of phases can be varied easily changing the gain loop per phase. Thus, the other phases try to attain the same current than the master phase. As happened in DCS, the voltage compensation network can be common or individual per phase.

MS topology presents the drawback of a difficult dynamic analysis since each slave loop depends on other loops. Thus, if n is high, the complexity of the analysis is important [4.28]

On the other hand, MS-CS should be associated to VMC or CMC and their corresponding block diagrams do not differs significantly with those of DCS. The

main difference is that its current reference is not the mathematical average current per phase.

There are three main approaches to select the master phase. First method is based on a custom schema where the master phase is selected by the user. This schema is known as “dedicated” master control. The main problem of this topology is that a failure of the master phase disables the whole system.

Second approach gives some redundancy to the system and it is called “automatic” master control. Here, the phase owning the highest current is defined to be the master one. Last variation is to rotate the “master” phase to augment the reliability of the system. Nevertheless, the complexity of the system is augmented considerably. This is known as “rotating master” [4.29] . The simulation schemas and their corresponding results are illustrated in point of the 8.3 Appendix A.

4.3.7.4 Current-Programmed Control in multiphase power converters

CPC can be also implemented using multiphase architectures. Then, a voltage compensation network imposes the inductor current reference as in the single-phase case. Therefore, the reference can be designed to be the peak, average or valley inductor current. Some simulations schemas can be found in the point 8.3.7 of the Appendix A.

4.4 Conclusion

A theoretical analysis of some digital control laws for VRs systems has been presented along this chapter. The main idea was to expose the basis for a systematic design of the digital control laws for power converters. In our study case, the design procedure was completed with practical examples of the synchronous Buck converter.

According to this design method, the continuous-time and discrete small-signal models defining the behavior of the power converter should be found in first place. Concerning these small-signal models, several possibilities to find its discrete-time description have been studied.

The second step was the study of the small-signal models of the digital control

laws. In response to this point, the discrete-time small-signal models of DVMC and DCMC control laws have been developed. In addition, the influence of the delay in the digital system has been disclosed. In short, this delay should be considered in the final design of the feedback regulation loop since an excessive delay weakens completely the system behavior.

With regard to digital control laws, some design guidelines for a proper design have been given and validated with several examples showing the feasibility of such control laws. Moreover, most widespread digital filters used for the compensation network of the regulation loop have been presented.

Thus, for our application, DVMC seems a good candidate whereas current sharing or a strict control of the inductor currents would be not required. In this case, some kind of DCMC should be used. Nevertheless, classical DCMC is difficult to implement due to technological problems, e.g. a high sampling-frequency. Furthermore, it needs very fast ADCs in the current loop and powerful digital controllers in order to reduce the delay introduced by the analogue-to-discrete conversion and the control law algorithm respectively. Later conclusions have been verified giving some simulation examples.

Once the systematic design procedure has been established, several control techniques based on those previous have been formulated. These digital control methods try to improve the behavior of our system and to reduce the drawbacks of classical control laws. To illustrate our purpose, an example of adaptive control has been given where the most efficient duty-cycle depending on the load variation is calculated and stored in LUT to obtain faster dynamical responses. Another example disclosed was “One-cycle Predictive Current” control law. This later technique is revealing as an interesting possibility for this kind of applications. Actually, it owns the advantages of CMC converters and it is less exigent in terms of complexity (sampling frequency) than classical DCMC.

Another point treated in this chapter is the improvement of DVMC and DCMC with the addition of FF techniques. Thus, it has been shown theoretically with some examples how these techniques associated to DVMC or DCMC improve the converter behavior and reduce the effects of input-voltage and load disturbances respectively.

As a final point, different ways to achieve uniform power distribution among commutation cells of an interleaved multiphase power converter by means of CS techniques have been presented giving the diagram blocks of these architectures as well as their main working principle equations.

In short, a theoretical study of the converter and of its digital control laws has been completed along this chapter. The practical application of these conclusions in a real digitally-controlled power converter is illustrated in next chapter

.

Chapter 5

Single-Phase Experimental Prototypes

5. SINGLE-PHASE EXPERIMENTAL PROTOTYPES

5.1 Introduction

The purpose of this chapter is to show the feasibility of a high-frequency digitally-controlled single-phase synchronous power converter. As a result, two different types of digital controllers have been employed in order to reach the desired technical specifications.

In view to validate the systematic design procedure exposed along this dissertation, the calculation of the power stage for each one of our experimental prototypes has been completed in chapter. In the same way, several digital control laws for embedded VRs applications which are applied in the present chapter have been studied and presented in the chapter four. Thus, the conclusions obtained in these previous chapters are the starting point for our experimental prototypes.

To illustrate our purpose, an example of a single-phase digitally-controlled power converter is presented along the following sections. This experimental prototype is designed for embedded applications requiring low and medium supply currents, i.e. embedded laptop μps like those presented in [5.1] .

Before starting with the practical design, some simulation models validating the algorithms exposed in chapter four are presented. The implementation of these control laws is exposed in detail in order to obtain a full digitally-controlled single-phase synchronous power converter with high performances. Therefore, these design steps are developed in deep during next points.

5.2 Single-Phase DC/DC converter using a fix-architecture and variable-functionality digital controller

5.2.1 Introduction

To achieve our first experimental prototype, a digital controller owning fix architecture and variable functionality, i.e. a DSC (Digital Signal Controller) has been selected. This control stage gives to designers some advantages in the

implementation of digital laws algorithm like fast and easy adaptations to changes. The simple reconfiguration of the DSC functionality can be achieved by means of variations in its software code. Therefore, this section starts giving some design guidelines of the most important parts of a digitally-controlled power converter using a Freescale's DSC [5.2] . A general schema of this prototype is shown in Fig. 5-1 and its experimental implementation is illustrated in Fig. 5-2.

The technical specifications for the power converter used to validate our first experimental prototype are exposed in detail in [5.1] and summarized in Table 5-1. These power requirements are oriented to supply embedded microprocessors of laptop computers. In particular, the supply specifications are focused on the Dual-Core Intel Xeon® processor.

Specification	Total
Input Voltage (V)	3-12
Output Voltage (V)	1
Output Current (A)	20
Switching Frecuency (MHz)	1.15
Output Voltage Ripple (%@mV)	1@10
Maximal Overshoot (mV@µs)	50@25
Maximal Settling time (µs)	350

Table 5-1 Design specifications for embedded laptop microproccesors

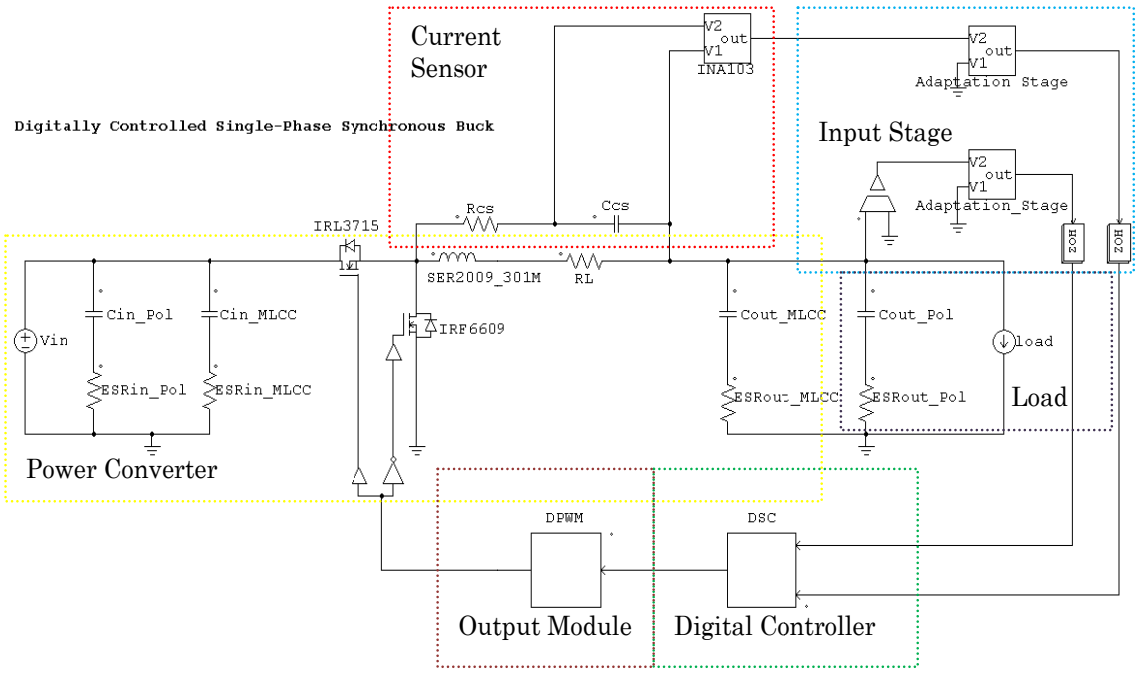


Fig. 5-1 Electrical schema of the first digtally-controlled single-phase power converter

Fig. 5-2 First Experimental prototype made in the LAAS: DSC-controlled single-phase synchronous Buck power converter

5.2.2 The digital controller

The control stage is based on the 56F8367EVM evaluation board of Freescale Semiconductor. This module owns a 16 bits DSC with a clock frequency of 60MHz [5.2] Actually, designers can choose among different programming-modes using this DSC. Therefore, algorithms can be implemented using integer, fix-point, floating-point or "fractional" operations. This later mode is quite interesting because it possesses some mathematical operations which can be used with a similar accuracy than in the typical floating-point case but in a lower time than this last one. Then, using "fractional" mode, finite-word resolution errors can be reduced. Table 5-2 shows the execution times for a simple "add" instruction using this DSC.

"Add" Instruction	Mode		
	Fix-point	Floating-point	Fractional
cycles	6	110	3
time	100ns	1.83µs	50ns

Table 5-2 Example of the execution time of a single instruction

5.2.3 The Input Module

The 56F8367EVM board owns several 12 bits built-in pipeline ADCs. This ADC topology presents an acceptable trade-off between resolution and time conversion (see point 2.3.2.1). Even so, several pulse clocks are needed to complete a single analogue-to-discrete conversion. In the case of the 56F8367EVM board, seven pulse clocks are required introducing a 1.7µs delay in the conversion chain.

Obviously, this large delay makes impossible a correct tracking of the instantaneous inductor current for values around 1MHz in our application.

Therefore, it is added to our system an external acquisition board incorporating high-frequency ADCs (20MHz) to reduce the delay introduced by this module.

This input module and its working principle is shown in Fig. 5-3. The main idea is to take into account the delay introduced for the pipeline architecture (5 pulse clocks in this case) and the propagation time of the inductor DCR current sensor previously measured.

Then, inductor peak-current (shifted by a 15ns delay due to the ADC acquisition time) can be gathered. To assure a correct synchronization, the input module is based on a D latches schema. This circuit adds the delay introduced by the ADC and the current-sensor to the PWM down-pulse time to gather the inductor peak-current. Moreover, this acquisition card incorporates a tuning system to modify the gain of the acquisition system as well as the delay time for a more accurate research of the maximal inductor current value in different working points. An example of the inductor current acquisition obtained with our real prototype is exposed in Fig. 5-4.

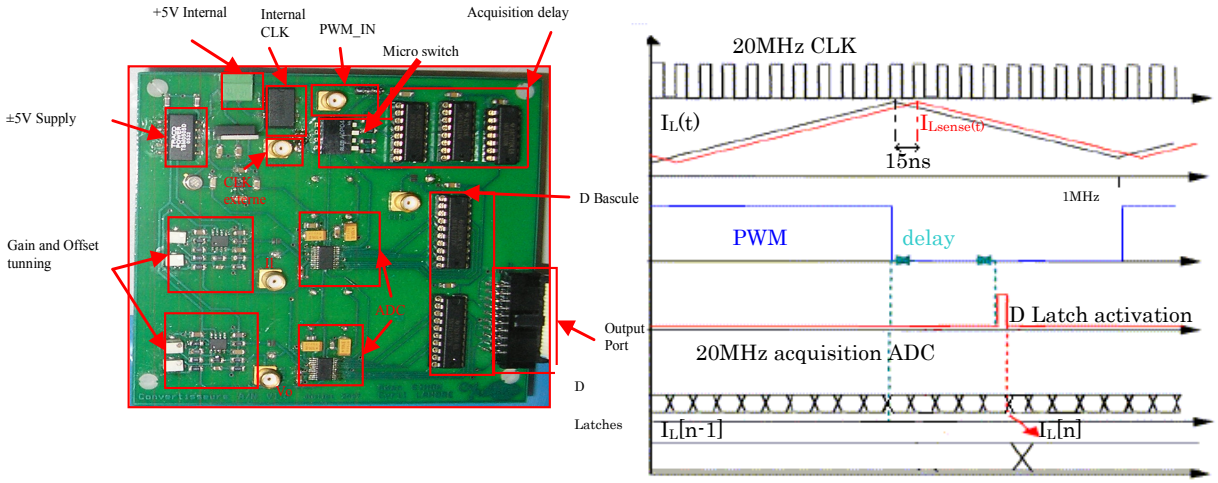


Fig. 5-3 Input module (left) and its working principle (right)

As regards the required ADC resolution, the output voltage analogue-to-discrete conversion is more critical in terms of quantization voltage levels. In our application, the main constraint is given by the small output-voltage ripple imposed in [5.1]

Then, the minimal resolution needed is 8 bits according to equations shown in point 2.3.2. For reasons of simplicity, the same resolution has been selected for

the inductor current ADCs in spite of lower resolution ADCs can be used in this case. As a result, the minimal inductor current variation that can be detected is 122mA as it is illustrated in Fig 5-4.

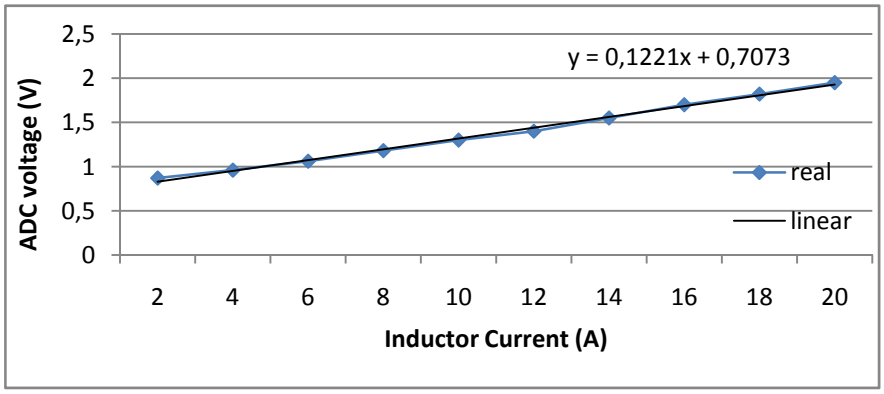


Fig. 5-4 Inductor current ADC characterization.

As it has commented in point 4.3.3.3.1.2, the delay introduced by this ADC should be as small as possible. Hence, there is a design trade-off between the accuracy of our current-mode control (minimal current variation detected) and the ADC rapidness (number of clock required or a conversion). Therefore, the number of bits can be reduced in order to decrease the delay introduced by this ADC. Thus, windowed flash ADCs can be used for applications where the detection of small changes of inductor current is not required.

5.2.4 The Output Module

The main goal of this output module is to generate the duty-cycle of both switches using the command signal delivered by the digital control. The work principle of the output module is based on the "Fast-clock-counter" method (see point 2.3.3.1). Fig 5-5 and 5-6 show its principle working and its real implementation respectively.

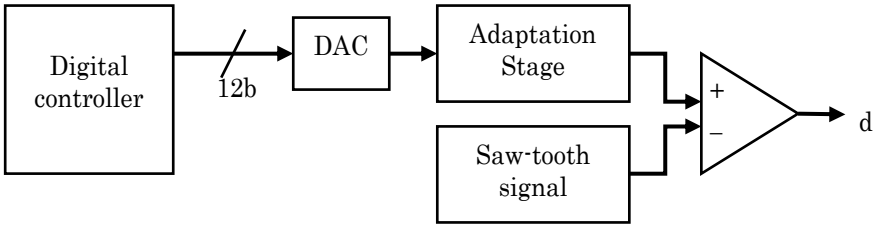


Fig. 5-5 Output module working principle

As happened in the ADC case, the integrated PWMs of the 56F8367EVM are not well adapted for high-frequency applications. For instance, it only owns sixty digital steps for a switching frequency of 1MHz, i.e. a resolution lower than 6 bits. Following (2-6), the required resolution is 11 bits for our application.

However, this resolution implies a clock frequency of 4096MHz. Obviously, this value is not feasible in practical terms in these days. As a result, the generation of the PWM in this module is obtained by means of a 12bits DAC (digital-to-analogue converter) and a comparator. Hence, the working principle is quite simple since the digital command signal delivered by the digital controller is transformed into an analogue value and compared with a saw-tooth signal in order to generate the duty cycle.

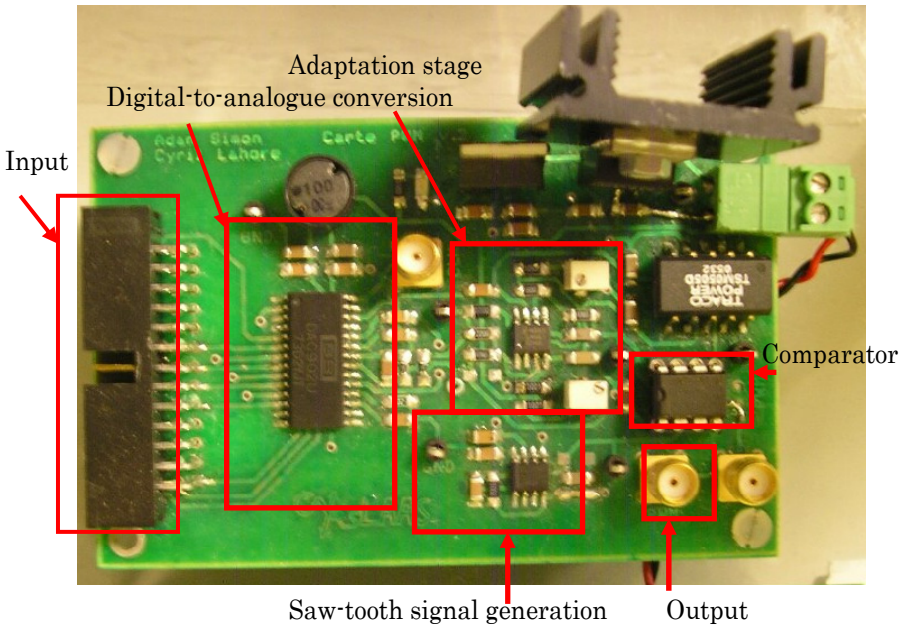


Fig. 5-6 Example of Output module for high-frequency applications made in the LAAS

5.2.5 Digital Control Laws Implementation

5.2.5.1.1 Introduction

Some of the digital control laws disclosed in chapter four have been implemented using this DSC in order to validate their feasibility in a real high-frequency application.

Therefore, the theoretical studies of these digital control laws completed in the previous chapter are the focal point for their implementation. Following our design method, Simulink/Matlab models validate the power converter and the digital control law model in high-frequency applications. These models have been

obtained using the S-Function toolbox of Matlab where the digital control law algorithm can be integrated directly in C code into our simulation model. Thanks to these functions, accurate simulations of the real system are obtained since fix-point, delay and quantification errors are considered in the model.

5.2.5.2 Digital Voltage Mode-Control

DVMC has been explained in detail in point 4.3.2. Thus, the corresponding Simulink simulation model is illustrated in Fig. 5-7.

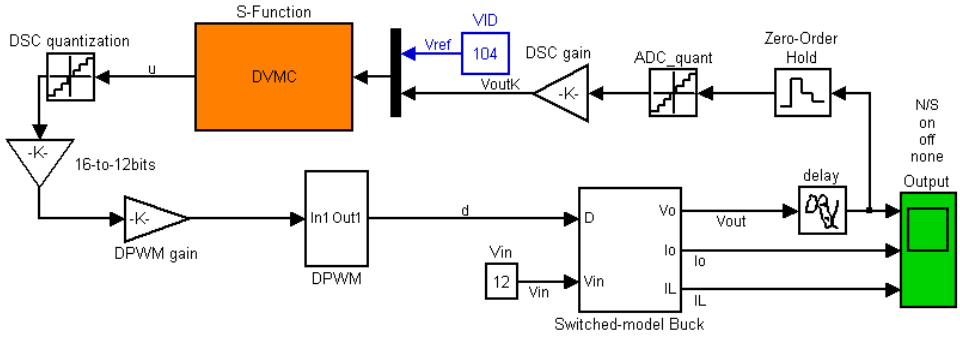


Fig. 5-7 DVMC simulation model

The first step is to identify and to calculate the delay introduced by our digital architecture. Then, this delay is summarized in Table 5-3 for this example. As it has been disclosed in previous chapters, the control-to-output voltage transfer function varies according to the input voltage and the load. The worst case in terms of stability is given by the maximal input voltage (12V) and the minimal load current (e.g. 2A).

In response to the test guidelines proposed in [5.1] , 5.7A load-current steps are simulated to validate our dynamical tests (i.e. from 13.3 to 19A).

Concerning the digital filter of the feedback loop, the incremental PID algorithm (see point 4.3.2.3) has been used. This topology has been selected because its algorithm introduces the lowest delay, i.e. it owns the lowest computational cost. After evaluating several approaches for the design of the digital filter exposed in [5.3] , the filter coefficients have been calculated by means of the pole-zero matching method.

Thus, the poles and zeros have been assigned directly in the z-plane using the discrete-time control control-to-output voltage transfer function exposed in (4.10) with its associated delay.

t_d (maximal) (ns)		
Programming mode	**integer**	**fractional**
PWM	457	457
algorithm	4450	2750
ADC	565	565
t_{sens}	20	20
t_{prop}	158	158
Total	5193	3493

Table 5-3 Delay calculation for DVMC

This delay value is extracted from the Table 5.3 for DVMC and it has been made round to a multiple integer value of the switching frequency. Another possibility is to find the pole-zero assignment directly from the discrete-time models found in point 4.3.2.2 obtaining also suitable and very similar results to the previous case as it was proved in [5.3]

By the way, the guidelines for the pole-zero location in both direct digital designs in z-plane are the same. Then, the filter coefficient are calculated to avoid steady-state error (pole in z=1) and to keep good stability margins in the whole range of frequencies. As a matter of fact, our design should assure a minimum phase margin of 45º for all frequencies above the crossover one. In this frequency, a gain margin higher of 6dB is required [5.3] , [5.4] Actually, the open-loop gain should be decreased up to the crossover frequency placing at pole at z=1 (20dB/dec is recommended). This constant decrease of the open-loop gain allows obtaining better transient responses and good rejection to disturbances. Both filter zeros (f_{z1}, f_{z2}) should be placed near the resonant frequency (f_o) of the power converter to achieve good stabilities margins and to enlarge the crossover frequency value maximizing the open-loop gain around this resonant frequency. Moreover, the second pole of the filter (f_{p1}) should match the zero of the power converter (f_{esr}, determined by the ESR output-filter capacitor) to keep a 20dB/dec roll-off in the open-loop gain. An additional high-frequency pole (f_{HF}) can be added to improve the noise immunity at frequencies around the switching one (f_{sw}) imposing a roll-off of -40dB/dec beyond the pole value. Finally, the filter gain (k_c) should impose the open-loop unity-gain frequency at the desired value respecting the stability margins previously explained. In general terms, the

direct pole-filter assignment in the z-plane can be given by:

$$G_c(z) = k_c \cdot \frac{(z - f_{z1}) \cdot (z - f_{z2})}{(z-1) \cdot (z - f_p) \cdot (z - f_{HF})} \tag{5.1}$$

$$\begin{aligned} &with: \\ &f_{z1} = 0.7 \cdot f_o \; ; \quad f_{z2} = 0.9 \cdot f_o \; ; \quad f_p = f_{esr} \; ; \quad 0.3 \cdot f_{sw} \le f_{HF} \le 0.7 \cdot f_{sw} \end{aligned} \tag{5.2}$$

Obtaining:

$$G_c(z) = 6.5 \cdot \frac{(z\text{-}0.9922) \cdot (z\text{-}0.9542)}{(z-1) \cdot (z\text{-}0.4125) \cdot (z\text{+}0.5)} \tag{5.3}$$

Fig. 5-8 shows the open-loop gain, discrete-time control-to-output voltage transfer function and filter Bode diagrams for this DVMC example. Observing this design, it is obvious that fast system responses will be not obtained due to the large delay introduced by the digital architecture.

On the other hand, the closed-system pole-zero map is shown in Fig. 5-9 validating the stability of the system since all the poles (and also the zeros) of the closed-loop system are inside the unity-radius circle.

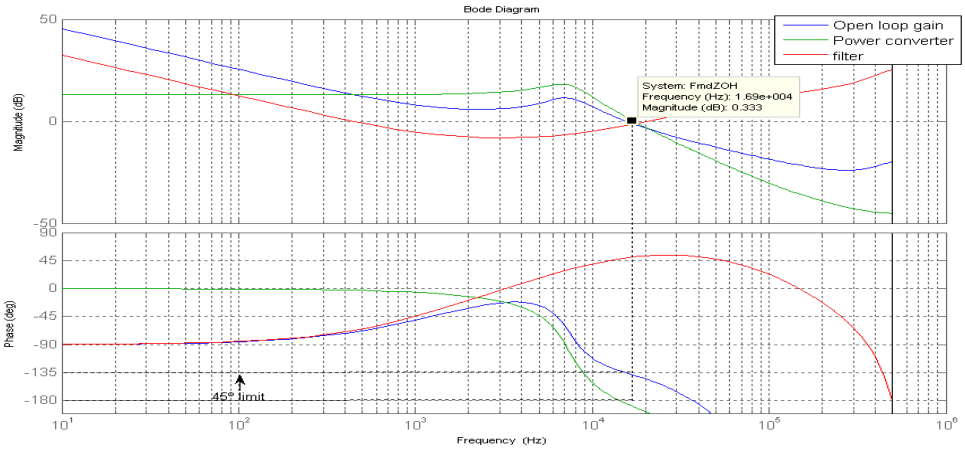


Fig. 5-8 Bode diagrams for DVMC

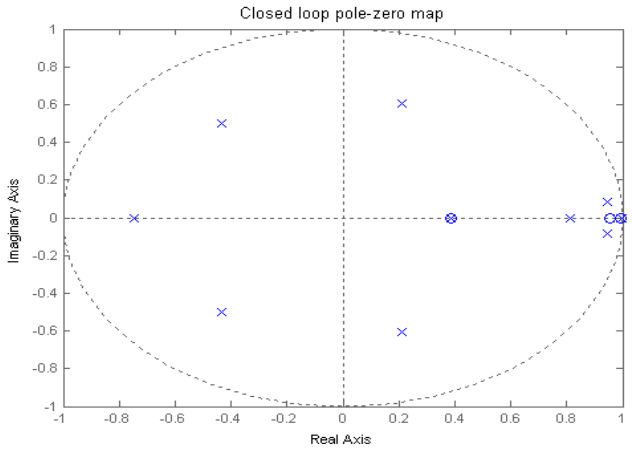


Fig. 5-9 Closed-loop gain pole-zero map

Finally, a simulation result for our single-phase DVMC synchronous Buck converter is shown in Fig. 5-10. It can be noted that line regulation and load regulation are validated in this simulation

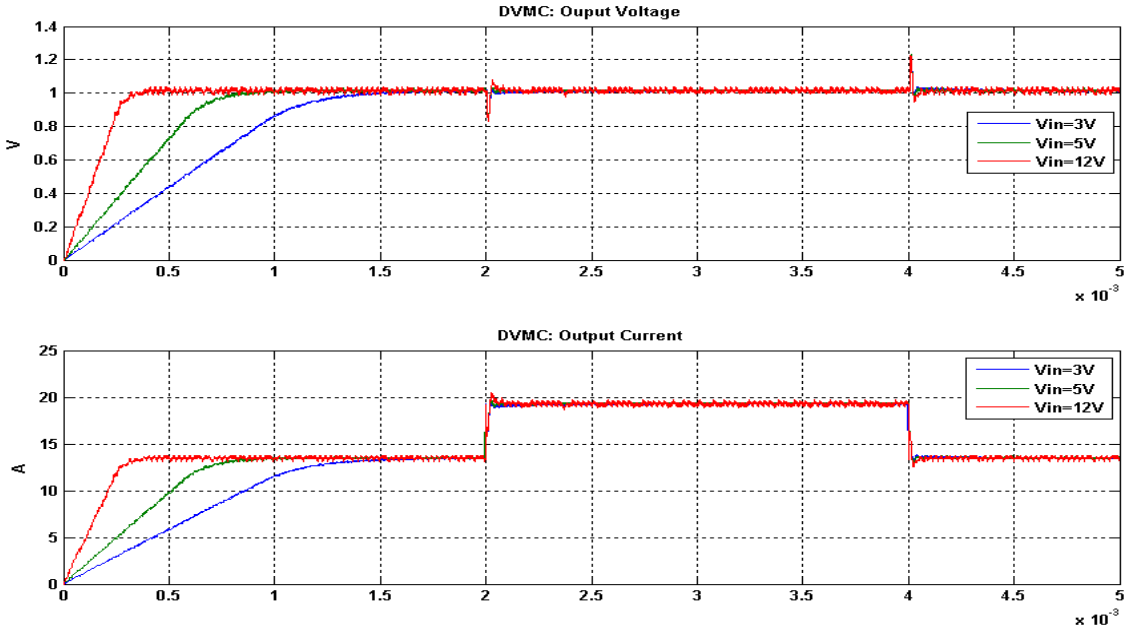


Fig. 5-10 DVMC: Output voltage and output current for a 5.7A load variation

Last figure shows clearly the influence of the input voltage in the system initial transient although its influence is lower than in following transient states produced by load variations.

In consequence, IVFF is required to isolate the control-to-output voltage transfer function from the input voltage disturbances. On the other hand, it is hard to achieve the time responses imposed in Table 5-1. The reduced value of bulk capacitors gives place to higher voltage deviations under transients than those proposed in [5.1] A lower bulk capacitor value has been used in order to compensate the significant influence of the delay introduced by the digital architecture. Therefore, this delay imposes a slow system as it is illustrated in Fig. 5-10 making difficult to reach the desired performances. Thus, open-gain loop may be augmented and this causes some instabilities.

Then, the main problem lies in the low DSC clock frequency. Thus, the algorithm is the main source of delay as it is seen in Table 5-3. In addition, a simple PID digital filter has been chosen to reduce the algorithm delay instead of more complicate filter structures owning better performances. To sum up, the solution is to employ a digital controller working with higher clock frequency.

Next, some experimental results of DVMC obtained with our experimental prototype are presented in next figures. In Fig. 5-11, an example of the steady-state behavior in their critical case (minimal current load and maximal input voltage is shown. Alternatively, the output voltage ripple is given in Fig. 5-12 and a 5.7A load step variation in Fig. 5-13.

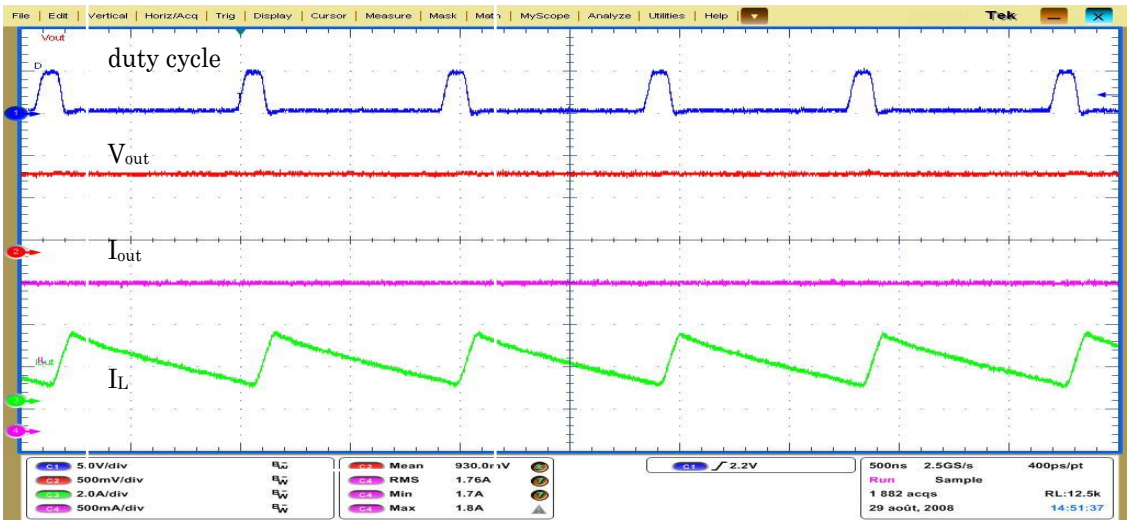


Fig. 5-11 DVMC: Steady-state for I_{out}=1.8A and V_{in}=12V

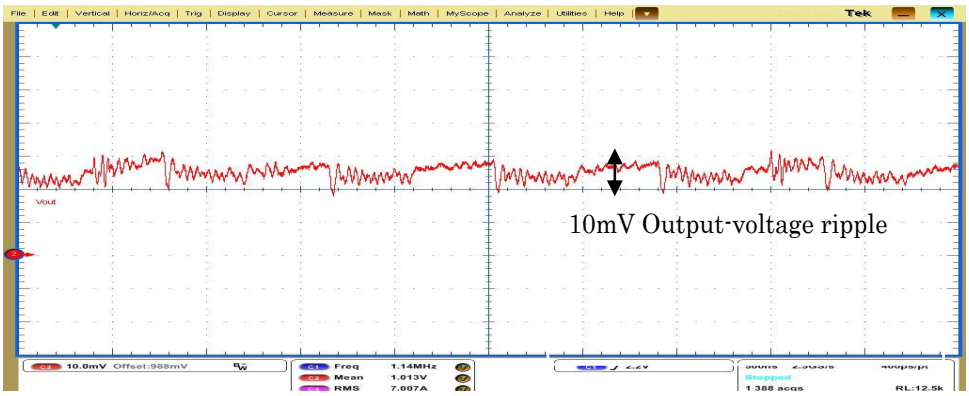


Fig. 5-12 DVMC: Output-voltage ripple in steady-state for I_{out}=1.8A and V_{in}=12V

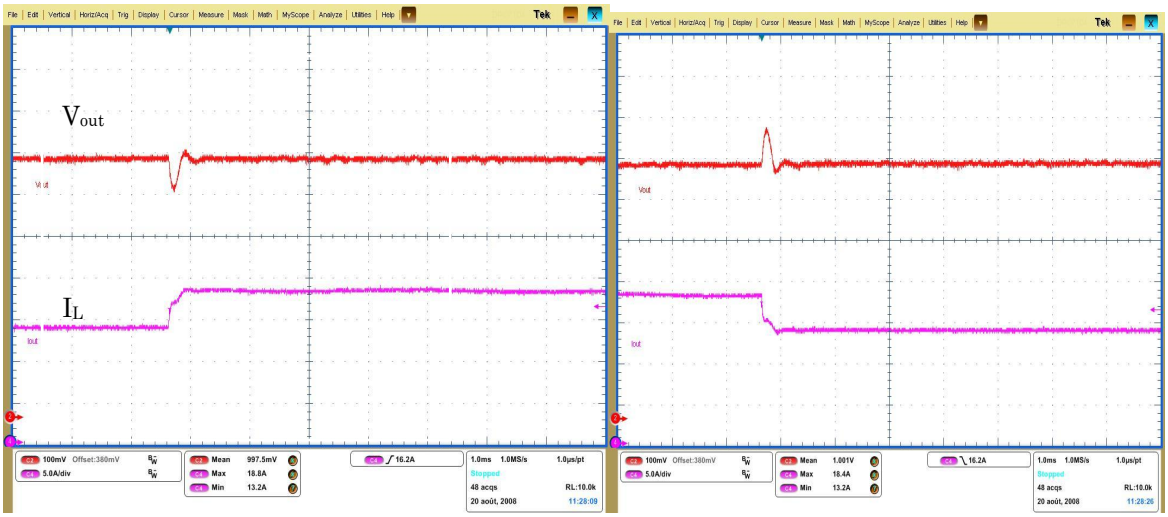


Fig. 5-13 DVMC: 5.7A load variation, Vin=12V

Table 5-4 summarizes the simulation and experimental performances of our digitally-controlled power converter. Note the good matching between both results.

	DVMC		
	GM	**PM**	**Crossover frequency**
	9.95dB	44.3°	17kHz
	Maximal deviation of the output voltage under a 5.7A load step; ΔV_{out} (%)		**Settling time at 2% under a 5.7A load step; t_{set} (µs)**
simulation	15%		450
practical	10%		450

Table 5-4 Comparison of simulation and experimental performances for DVMC

5.2.5.2.1 Digital Voltage Mode Control based on Look-Up-Tables

This variation of DVMC is based on the control law exposed in point 4.3.4. Thus, the built RAM devices of the 56F8367EVM are used to store the most efficient set of duty-cycles depending on load variations. That means the digital controller recovers the most performing duty-cycle for each load variation in order to achieve zero-voltage error in steady conditions.

A comparison of classical DVMC and this new implementation are shown in Fig. 5-14 (simulation) and Fig.5-15 (real implementation). In this example, a 5A load variation is illustrated using a simple PI digital filter to reduce at maximum the delay in both loops. Moreover, in this example, the value of the bulk capacitors has been reduced to 660uF in order to improve the response time of the power converter is spite of the higher deviation under load variations.

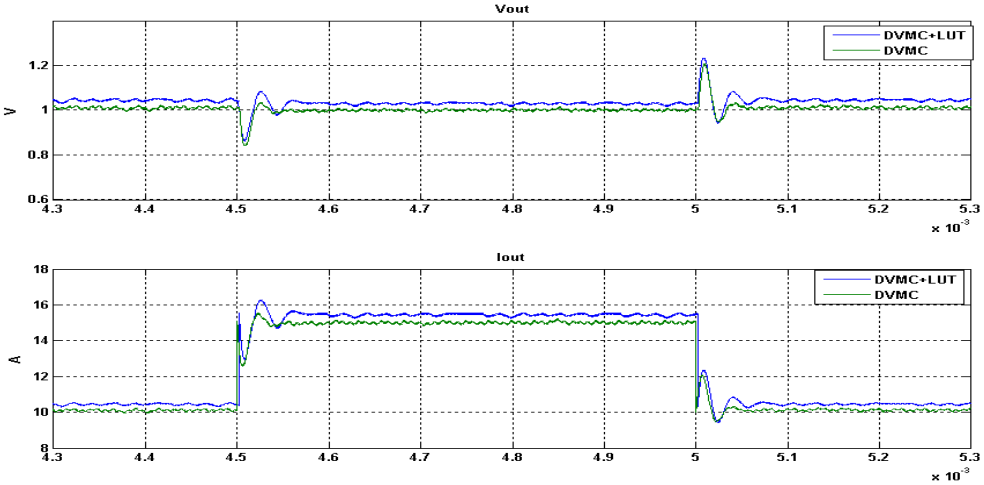


Fig. 5-14 Simulink Comparison of classical DVMC and DVMC using LUT

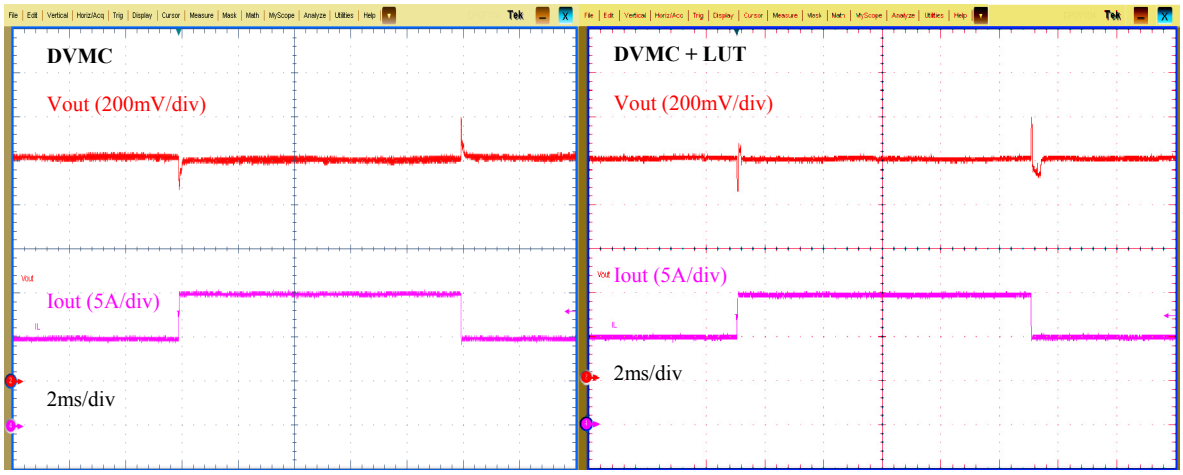


Fig. 5-15 Experimental Comparison of classical DVMC and DVMC using LUT

Thus, it can be observed in the simulation model an important reduction of settling times in the initial transient using DVMC with LUT. However, the initial voltage overshoot are incremented too. In contrast, the transient response to load variations is not improved compared to classical DVMC.

5.2.5.2.2 Digital Voltage Mode Control with Input Voltage Feedforward.

The addition of IVFF associated to DVMC has been studied in point 4.3.6.2 where it has been shown the influence of the input-voltage variations in the power converter transient response. Moreover, it has been proved by means of simulations how the effects of input-voltage disturbances in the converter output can be eliminated by means of the addition of an input-voltage feed-forward loop.

Therefore, this new feature to our prototype has been added obtaining the experimental results shown in Fig. 5-16.

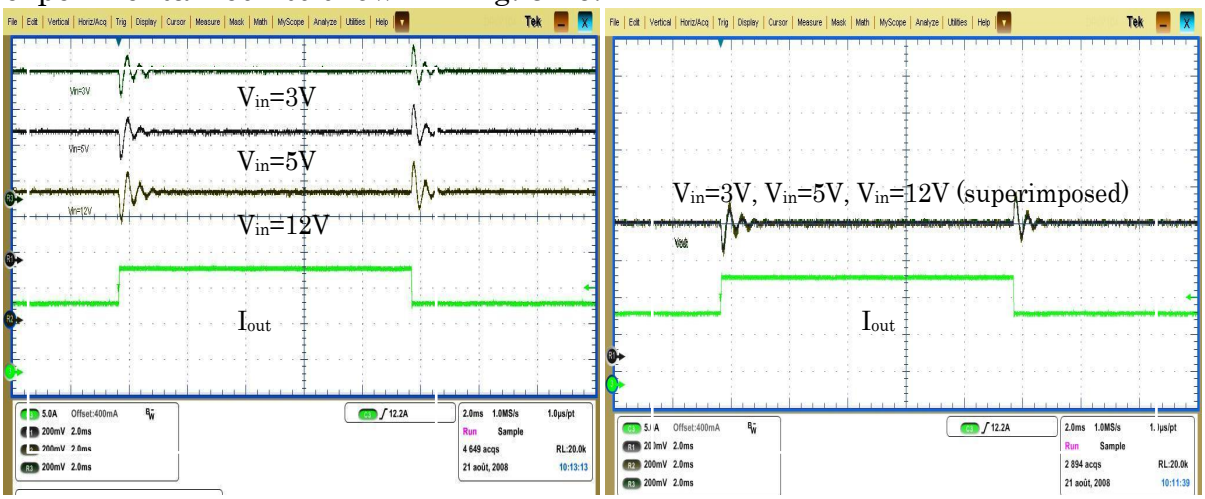


Fig. 5-16 DVMC with IVFF for V_{in}=3, 5 and 12V

5.2.5.2.3 Digital Voltage-Mode Control with over-current protection

The classical DVMC law presented in the previous point owns a major drawback. In fact, inductor current is not tracked and, therefore, the power converter is not protected against over-currents.

To solve this problem and to avoid failures in case of over-currents, a protection based on an inductor-current supervision has been added to the previous control law. This security module calculates the inductor-current and the output-voltage error signals at the beginning of each algorithm execution. Then, if the inductor current is higher than a given value or current reference, the system will work as a DCMC system in order to compensate this undesired current error. The main difference between this variation of DVMC and the classical DCMC law exposed in 4.3.3 is that the reference of this last one is not imposed by the external voltage feedback loop. Thus, this current reference is imposed by the user at the maximal allowed inductor-current delivered to the load. Otherwise, the system works as in the DVMC case.

The working principle is illustrated in (5.4). Therefore, the voltage and current error signals are processed by two different digital filters depending on which error is calculated.

$$\text{supervisory control of } I_L[n]\begin{cases}\text{If } I_L[n] < I_{max} \text{ then} \\ \quad e_v[n]=v_{ref}[n]-v_{out}[n] \quad \rightarrow \text{DVMC} \\ \text{else} \\ \quad e_i[n]=i_{max}[n]-i_L[n] \quad \rightarrow \text{DCMC} \\ \text{end if}\end{cases} \tag{5.4}$$

An experimental result of the current-limitation effect is shown in Fig. 5-17 using our adapted DVMC control law. In this example, an over-current protection is activated when the current tends to be higher than the reference level (15A in this case). Thus, the DCMC loop is used to prevent a failure of the system due to the increase of the output-current levels delivered to the load.

Then, it can be observed how the current compensation is active when inductor-current is higher than this imposed value. On the contrary, when inductor current is under this critical value, the voltage compensation network of the DVMC loop imposes again the desired voltage and current values which are 1V

and 10A in respectively in this example.

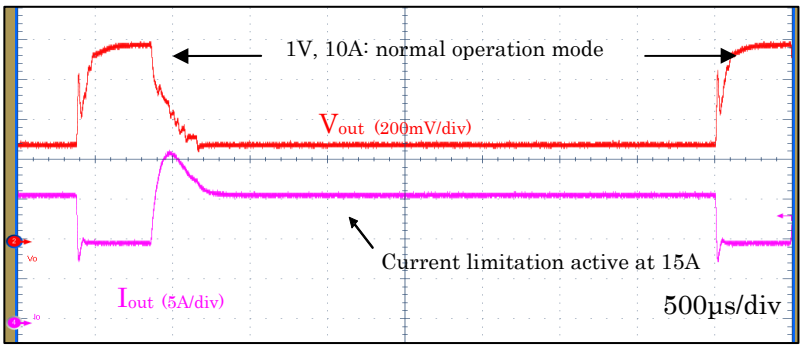


Fig. 5-17 DVMC with a 15A current limitation

This new feature added to classical DVMC allows protecting the system in case of over-currents. However, this control law owns a major drawback when it is implemented in this low clock-frequency DSC. Actually, the output-voltage droop produced when the supervisory control loop is working may own important values as happens in Fig. 5-17. This droop is produced by the lack of the output voltage regulation in this case and it can be solved adding to the inner current loop a cascade voltage regulation loop as in the classical DCMC (see point 4.3.3).

However, it is shown in point 4.3.3.3 that the delay introduced by the algorithm should be reduced as much as possible to avoid problems in the analogue-to-digital conversion of the inductor current. These performances are not achieved using this DSC, therefore; high-frequency classical DCMC is not possible using this digital controller. Therefore, OCPP incorporates a cascade voltage regulation loop which corrects previous problem. The practical implementation of OCPP using this DSC is presented in next point.

5.2.5.3 One-Cycle Predictive Current-Mode Control

OCPC is a good candidate for digitally-controlled power converters since it owns the benefits of DCMC without the necessity of a high sampling frequency for the inductor current as it has been explained in point 4.3.5.

Then, OCPC allows an easy implementation of the cascade output-voltage and inductor-current regulation.

This control law has been implemented in our DSC using the equations (4.41) and (4.42) of the chapter 4 for valley and peak current respectively cases. In this point, an example of valley current is illustrated. Therefore, the coefficients of the

digital filter for the external voltage regulation loop are obtained using the design guidelines imposed in [4.17] . Hence, the pole-zero matching method is used and the control-to-output-voltage presented in (4.40).

$$G_{cv}(z) = 14 \cdot \frac{(z\text{-}0.9990)\cdot(z\text{+}0.04)}{(z-1)\cdot(z\text{-}0.416)\cdot(z\text{+}0.19)} \tag{5.5}$$

$$G_{ci}(z) = 10 \cdot \frac{z}{(z-1)} \tag{5.6}$$

Fig. 5-18 shows the open-loop gain Bode diagrams and the system stability margins. Fig. 5-19 shows the pole-zero maps of the system.

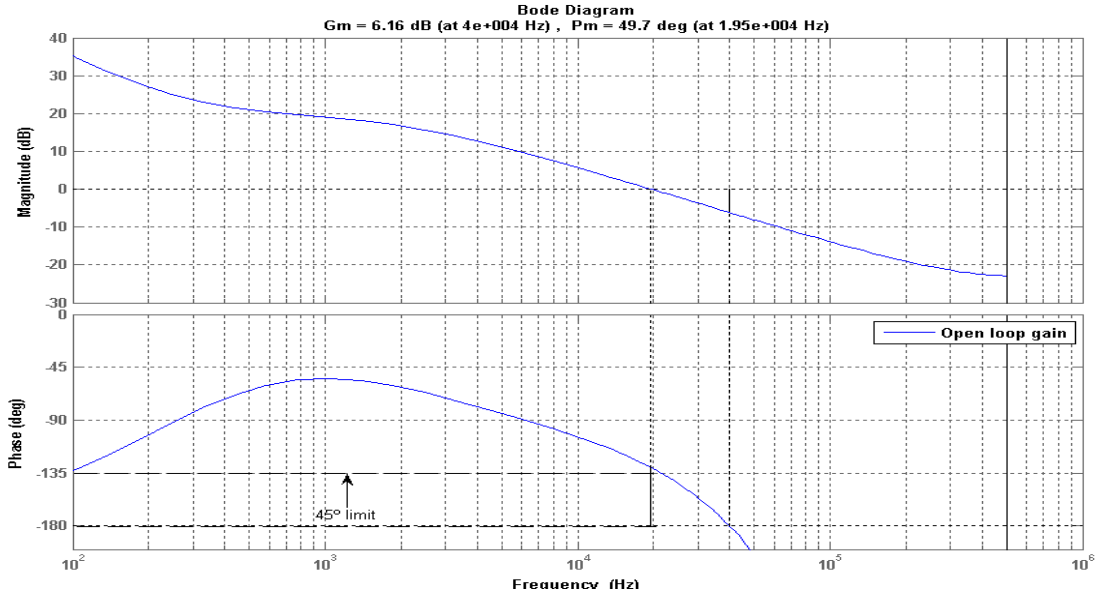


Fig. 5-18 Bode diagrams for OCPC

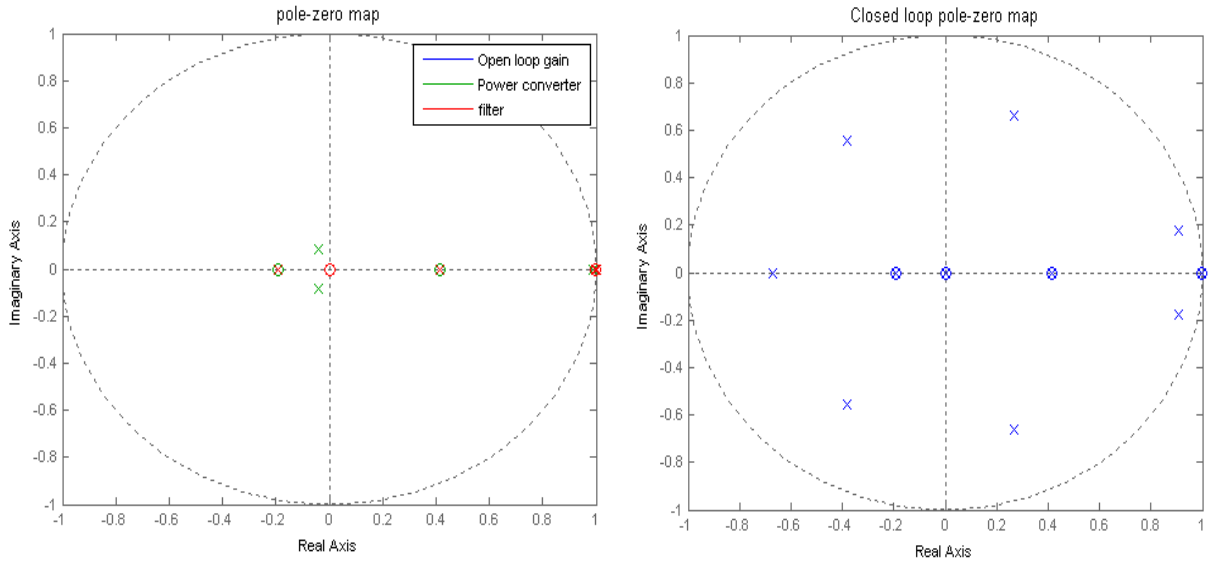


Fig. 5-19 Pole-zero map for OCPC

Hence, the simulation model for this control law is shown in Fig. 5-20 where the addition of the inductor-current regulation loop can be observed.

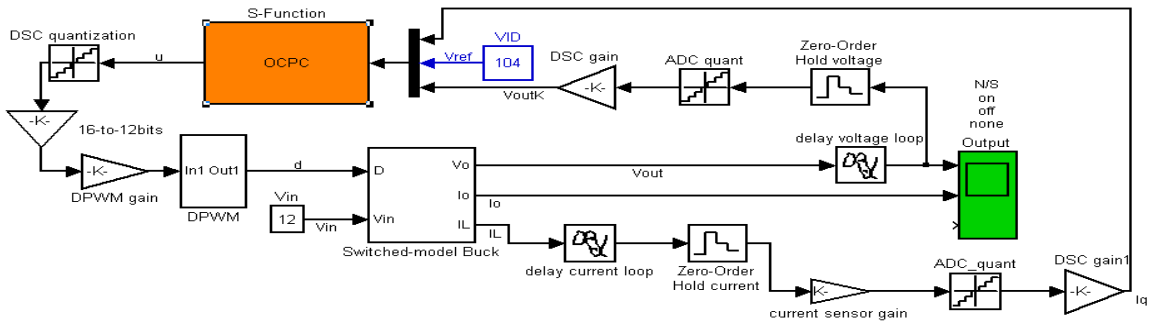


Fig. 5-20 OCPP simulation model

Next figure shows the simulation results for OCPC when an 8A load step is produced in Fig. 5-21. As it can be noticed, results are quite interesting because maximal deviation under transients is reduced considerably keeping the same settling times.

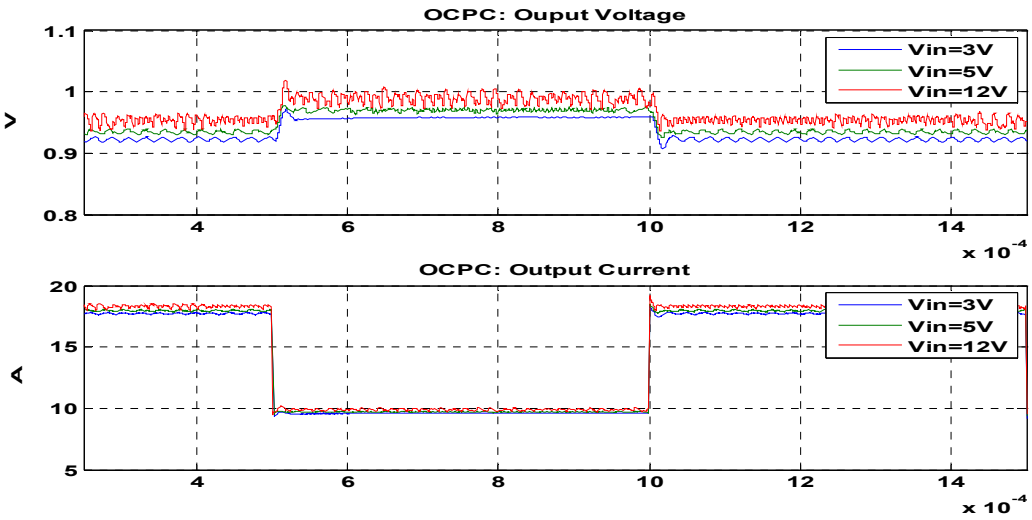


Fig. 5-21 OCPP: Output voltage and output current for a 8A load step

Finally, some results obtained with our prototype are shown in Fig. 5-22 and they are compared with those obtained with our simulation model in Table 5-5.

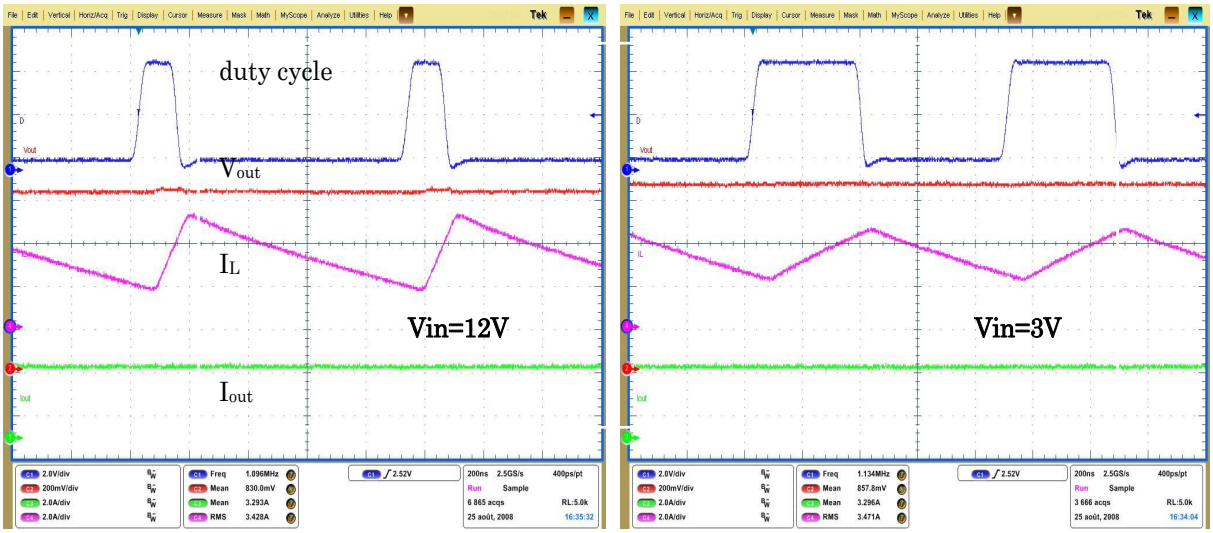


Fig. 5-22 OCPC: Steady-state for I_{out}= 3A

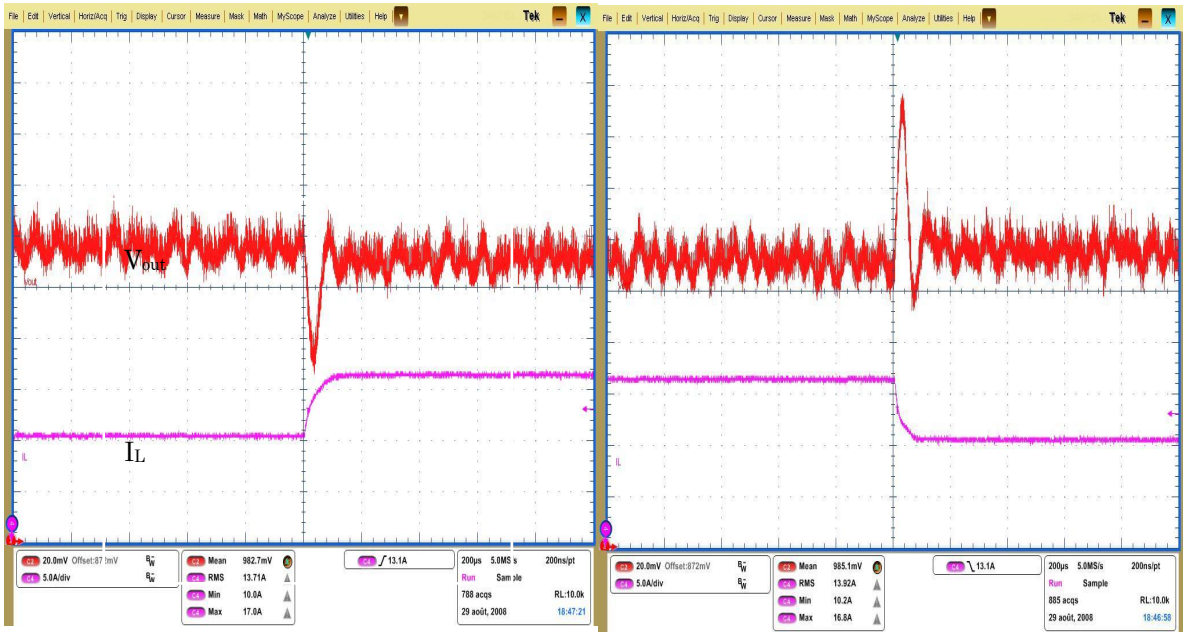


Fig. 5-23 OCPC: 6.6A load variation

	OCPC		
	GM	**PM**	**Crossover frequency**
	6.16dB	49.7°	19.5kHz
	Maximal deviation of the output voltage ΔV_{out} (%)		**Settling time at 2% t_{set} (µs)**
simulation	5%		300
practical	6%		300

Table 5-5 OCPC: Comparison of simulation and experimental results

5.2.6 Synthesis

The purpose of this part of the chapter was to show the feasibility of a high-frequency power converter using a simple digital controller owning fix-architecture and variable-functionality, e.g. a DSC. This controller owns some advantages in the way to implement the algorithm as an easy adaptation to changes by means of variations in its software code. Actually, an example of a digitally-controlled single-phase synchronous power converter designed for low and medium supply currents embedded applications has been presented along this part. These power requirements are oriented to supply embedded microprocessors of laptop computers. In particular, our supply specifications are focused on the Dual-Core Intel Xeon® processor.

To begin with the practical design, some of the digital control laws disclosed in chapter 4 have been implemented using this DSC to validate the theoretical

conclusions exposed along this previous chapter.

As a result, our method to design digital control laws for high-frequency applications based on Simulink/Matlab models has been developed during this part. These simulation models have been obtained using the S-Functions of Matlab where the digital control law algorithm in C code can be integrated directly into the simulation model. Thanks to these modules, accurate simulations of the real system can be obtained since fix-point, delay and quantization errors are considered in the model. In consequence, the validation of our control laws in these models is a previous step before to be implanted in the experimental prototype.

As concerns the control laws, some examples of DVMC and OCPC control are given in this section. Referring to DVMC, some variations of the classical control law in order to try to improve the performances achieved with the classical control law has been presented. For instance, a new feature which protects the system of undesired over-currents has been added to this classical law.

However, DVMC owns a major drawback when it is implemented in this low clock-frequency DSC even if this new module is added. Actually, the output-voltage droop produced when the supervisory control loop of this new feature is working may be important. This droop is produced by the lack of the output voltage regulation during this supervisory mode. This problem can be solved adding to the inner current loop a cascade voltage regulation loop as in the classical DCMC.

Nevertheless, is has been shown in point 4.3.3.3 that the delay introduced by the algorithm should be reduced as much as possible to avoid problems in the analogue-to-digital conversion of the inductor current. These performances are not achieved using this DSC, then, high-frequency classical DCMC is not possible using this digital controller.

According to last conclusion, OCPC digital control law has been implemented using the Freescale's DSC. This technique incorporates a cascade voltage regulation loop which corrects previous problem. In short, OCPC is a good candidate for digitally-controlled power converters since it owns the benefits of DCMC without the necessity of a high sampling frequency for the inductor current loop as it has been explained in point 4.3.5.

Then, OCPC has been implemented in this DSC and it has been proved how this law improves the power converter behavior reducing the voltage deviation and the settling times under load variations.

Nevertheless, these settling times are still important compared with classical analogue systems in spite of the specifications imposed in the introduction of this chapter are almost accomplished. Then, the unique solution is to replace the digital controller for another owning a higher clock-frequency, i.e. a FPGA.

5.3 Single-Phase DC/DC converter using a variable-architecture and variable-functionality digital controller

5.3.1 Introduction

FPGA are nowadays a powerful tool to develop full digitally-controlled applications due to its high-frequency clock. As a result, frequency constraints and delay problems found in our preceding prototype can be solved since the algorithm is processed now in a lower time than in the previous case.

Actually, the total delay introduced by the digital architecture is a fraction of the power converter switching period. This is especially important since the duty cycle can be refreshed in real time rejecting disturbances in a much reduced time than in the previous case.

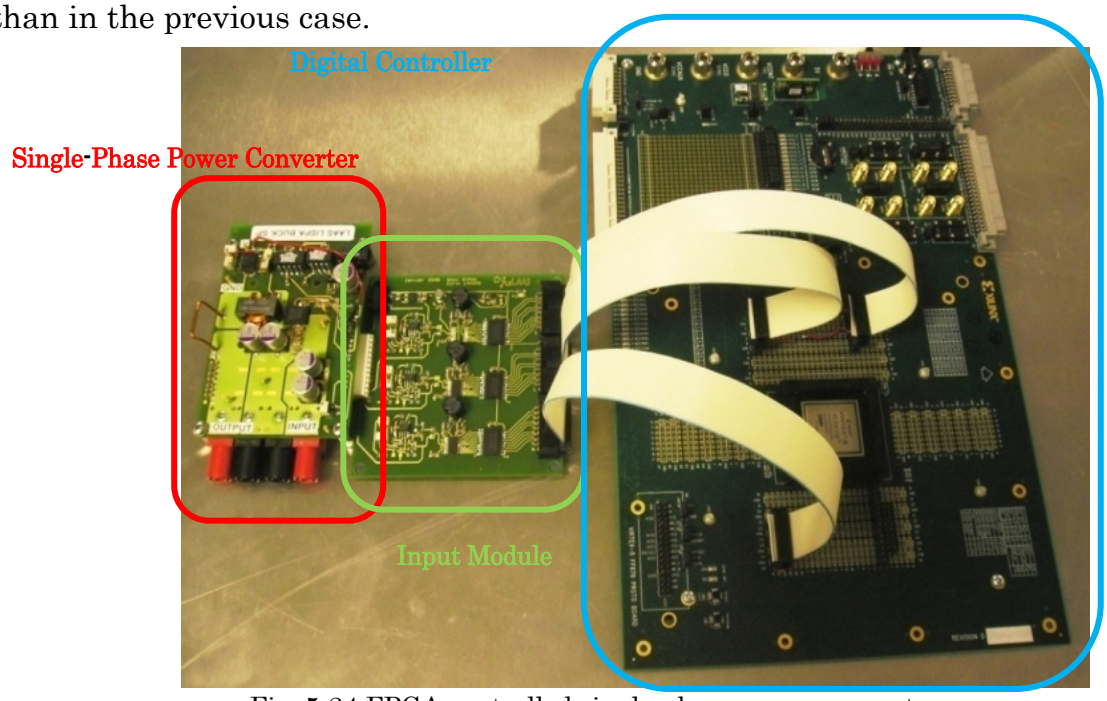


Fig. 5-24 FPGA-controlled single-phase power converter

The general schema of this prototype is quite similar to the one shown in Fig. 5-1 replacing the DSC and DPWM module by the new digital controller. Once more, the technical specifications are quite similar to those exposed in [5.1] . The reader can remind them in Table 5-1.

Nevertheless, in this new prototype, the power stage has been replaced for another which is able to deliver a maximal supply current of 36A to the load [3.22] . This increase of the power converter output current permits to supply whichever embedded laptop microprocessors exposed in [5.1] . Thus, our second experimental prototype is shown in previous Fig. 5-24.

5.3.2 The digital controller

The control stage is based on the Virtex-5 FF676 ProtoBoard which can incorporate different FPGA of the Xilinx's LX series [5.5] . In our case, the XC5VLX50 FPGA [5.6] has been used. This device owns a very-high clock frequency permitting a drastic reduction of the several delays like those of the control law algorithm, DPWM generation and discrete-time signal acquisition.

5.3.3 The Input Module

The Virtex-5 FF676 ProtoBoard does not own built-in ADCs. In consequence, an external analogue-to-discrete conversion stage should be added to the digital controller. In this case, the same input module containing 8 bits ADCs has been used than in the point 5.2.3 employing the same working principle.

5.3.4 The Output Module

The duty-cycle for both switches can be generated directly from the digital controller using HDL techniques. Once more, the "Fast-clock-counter" method (see point 2.3.3.1) has been employed but with a reduced resolution due to frequency and consumption constraints. Thus, the output module owns a final resolution of 8 bits (or 3.9 ns in time domain terms) which is the minimal theoretical resolution available to avoid limit-cycle oscillations in our study case.

5.3.5 Digital Control Laws Implementation

5.3.5.1 Introduction

DVMC and OCPC control laws have been developed using this digital control in order to improve the system performances obtained with our previous experimental prototype. All over again, these control laws has been simulated using Simulink/Matlab models to validate them. After, they have been implemented these control laws using VHDL code in the FPGA. This systematic design procedure is disclosed in next points.

5.3.5.2 Digital Voltage Mode-Control

The simulation model diverges slightly from those used previously. Indeed, the algorithm is not integrated into the simulation model. Moreover, the digital filter is implemented using conventional Simulink blocks (see Fig. 5-25). In this case, the "Setpoint weighting" version (parallel algorithm) has been used [4.9] . This topology has been selected due to the FPGA skill to execute efficiently parallel operations and, therefore, to reduce drastically the delay introduced by the algorithm. This algorithm treats independently the three branches of the filter reducing the noise effects in the output. Nevertheless, an accurate synchronization among branches is required using this digital controller by means of a state-machine.

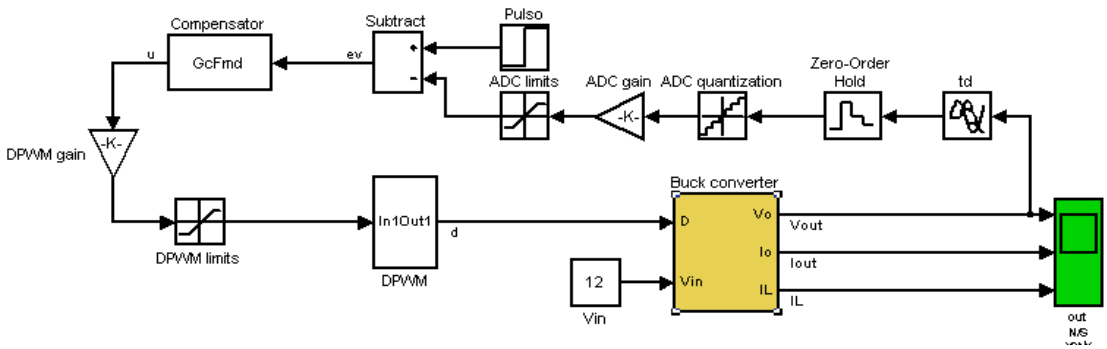


Fig. 5-25 DVMC simulation model

In keeping with the filter coefficients calculation, they are obtained in a similar way than in the previous experimental prototype, i.e. using the pole-zero matching technique. In this case, a conservative delay of 1µs has been considered in our design even if the total delay of the system is lower than this value. Using

(4.32) and (4.33) and giving b=1 and N=3, the filter coefficients are:

$$\begin{aligned} &u[n] = P[n] + I[n] + D[n] \\ &with: \quad \mathrm{P[n]}=0,2080 \cdot \left(V_{ref}[n] - u[n]\right) \\ &\qquad \mathrm{I[n]}=I[n-1] + 0,0010 \cdot \left(V_{ref}[n] - u[n]\right) \\ &\qquad \mathrm{D[n]} = 0,8848 \cdot D[n-1] - 0,5521 \cdot \left(u[n] - u[n-1]\right) \end{aligned} \tag{5.7}$$

It is worthy to note, that these coefficient should be standardized following (5.8) and their quantization should be taken into account

$$k'[n] = \frac{k[n]}{\|k[n]\|} \quad \text{with:} \quad \begin{aligned} k'[n] &= \text{quantized coefficient value} \\ k[n] &= non - \text{quantized coefficient value} \\ \|k[n]\| &= \text{maximal coefficient value} \end{aligned} \tag{5.8}$$

Fig. 5-26 shows the open-loop gain, discrete-time control-to-output voltage transfer function and filter Bode diagrams for this DVMC example. Obviously, a faster system than in the previous case is obtained due to the important reduction of the delay. Moreover, the closed-loop pole-zero map is shown in Fig. 5-27 validating the stability of the system since all the poles (and also the zeros) of the closed-loop system are inside the unity-radius circle.

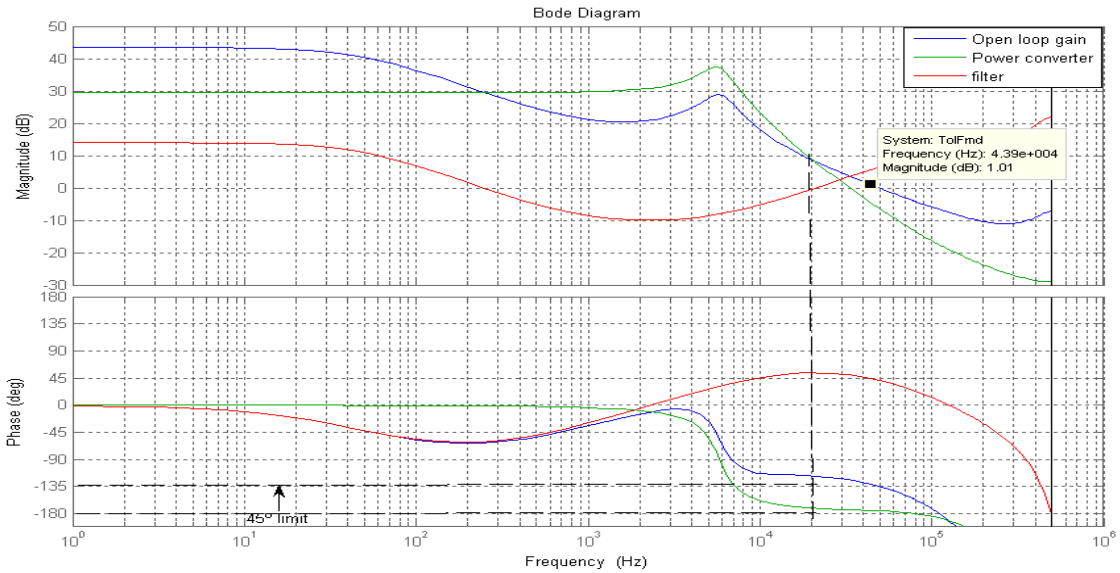


Fig. 5-26 DVMC: Bode diagrams

Next, some simulation results of DVMC are presented in Fig. 5-28. Moreover, the corresponding experimental results are shown in Fig. 5-29 for a steady-state behavior with a 2A static load (keeping V_{in}=12V).

In the Fig. 5-30, the output voltage ripple for this case is illustrated and a 5.8A load step change is represented in Fig. 5-31. It can be observed that performances have been improved respect to the previous case.

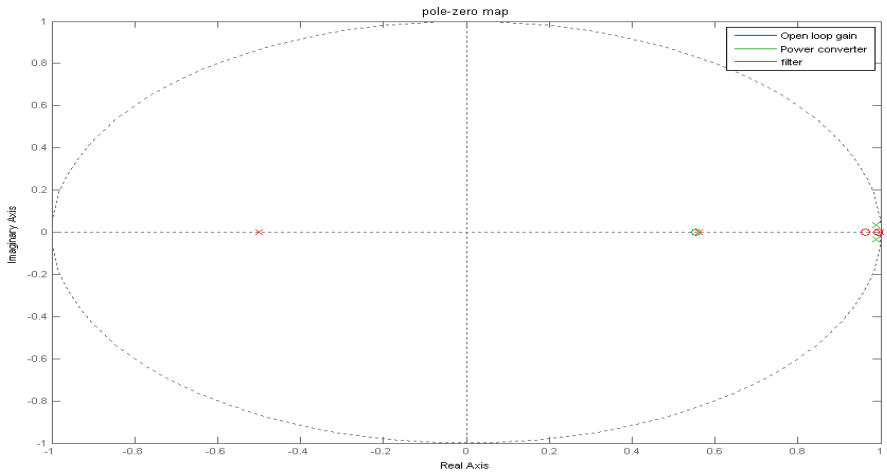


Fig. 5-27 DVMC: Closed-loop pole-zero map

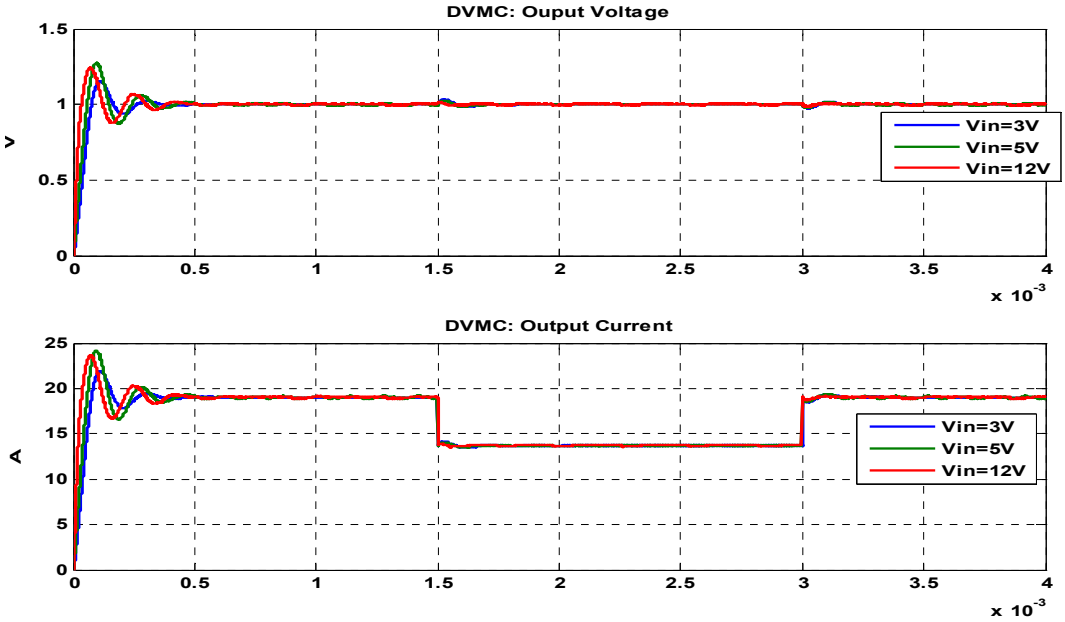


Fig. 5-28 DVMC: Output voltage and output current for a 5.7A load variation

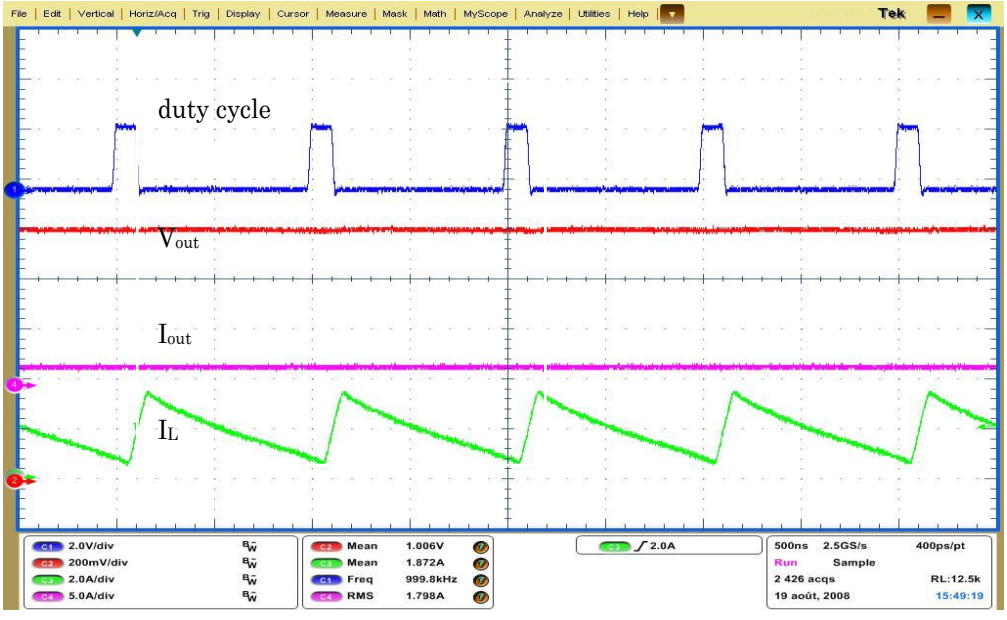


Fig. 5-29 DVMC: : Steady-state for I_{out}=1.8A and V_{in}=12V

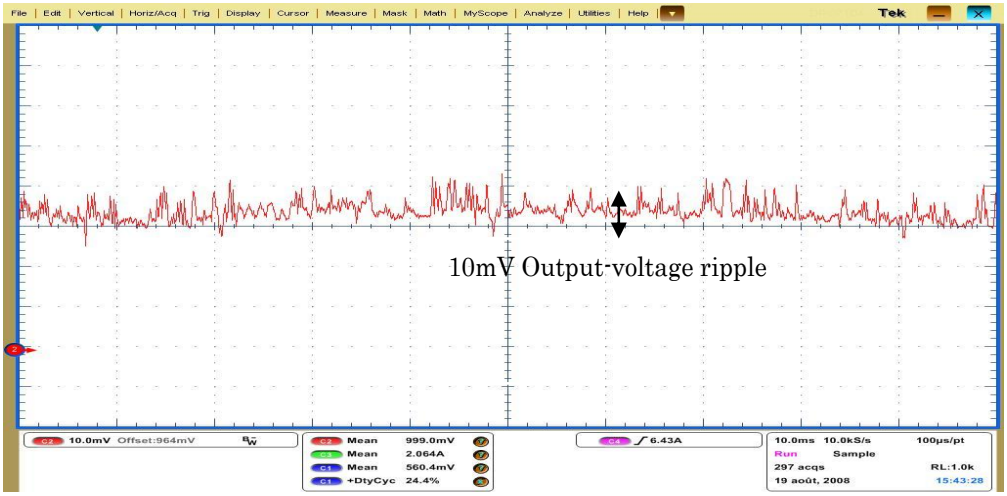


Fig. 5-30 DVMC: Output-voltage ripple in steady-state for I_{out}=1.5A and V_{in}=12V

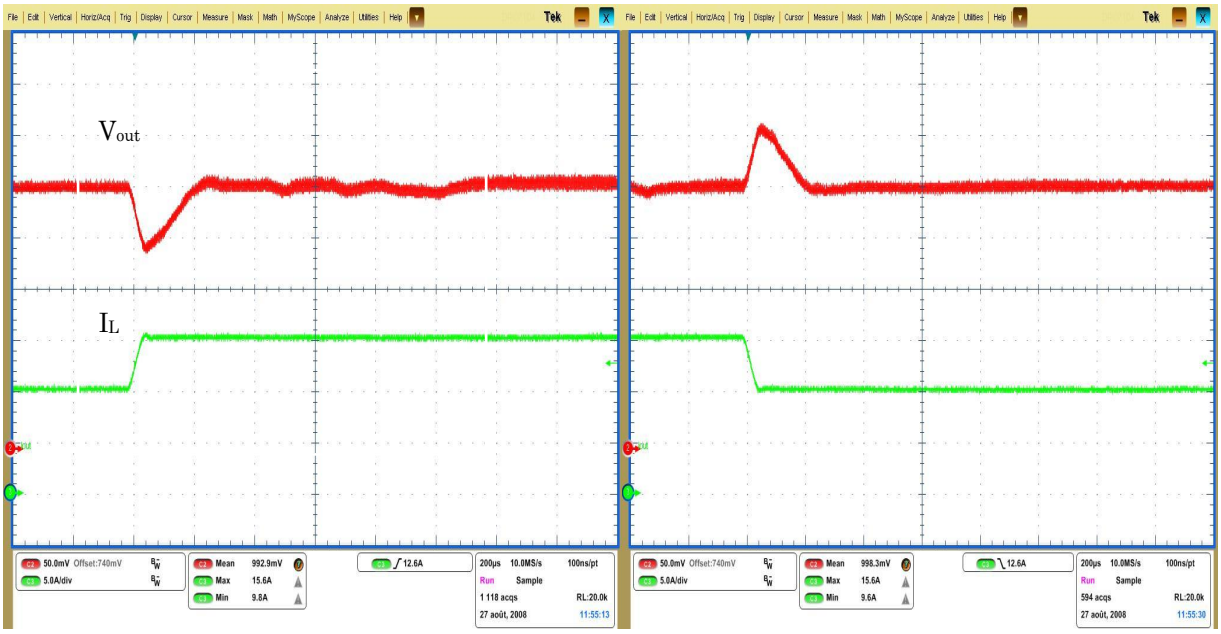


Fig. 5-31 DVMC: Output voltage and output current for a load step of 5.8A

To sum up, the simulation and experimental performances are summarized in Table 5-6 where it can be stated the good matching between both results.

	DVMC		
	GM	**PM**	**Crossover frequency**
	6.97dB	47.9°	47.8kHz
	Maximal deviation of the output voltage ΔV_{out} (%)		**Settling time at 2% t_{set} (µs)**
simulation	3%		250
practical	7%		280

Table 5-6 Comparison of simulation and experimental performances for DVMC

5.3.6 Conclusion

The main motivation of this chapter was to show the feasibility of a single-phase high-frequency digitally-controlled synchronous power converter for low and medium supply current loads. These power requirements are oriented to supply embedded microprocessors of laptop computers. Therefore, two examples for this kind of high-frequency VR applications has been developed.

To illustrate our purpose, the power stage and the control laws disclosed in chapters three and four respectively has been implemented along this chapter.

Referring the digital control laws, a systematic design methodology based on simulation models has been employed to optimize the performances of our experimental prototype.

The digital controller for the first experimental prototype is based on a DSC module, i.e. that its architecture cannot be modified. For this experimental prototype, Simulink/Matlab models have been used to validate the algorithms which are used later in the real prototype. These simulations models have been obtained using the S-Functions of Matlab where the digital control law algorithm in C code can be integrated directly into the simulation model. Thanks to these modules, accurate simulations of the real system can be obtained since fix-point, delay and quantization errors are considered in the model. In consequence, the validation of our control laws in these models is a previous step before to be implanted in the experimental prototype.

As concerns the control laws, some examples of DVMC and OCPC control have been given. Referring to DVMC, some variations of the classical control law have been made in order to try to improve the performances achieved with this classical one. For instance, a new feature which protects the system of undesired over-currents has been added to this classical law. However, the low clock-frequency of this digital controller causes inefficient operation modes of these new control laws.

To solve this problem, OCPC digital control law has been implemented. This technique incorporates a cascade voltage regulation loop which corrects the lack of inductor-current regulation. OCPC is a good candidate for digitally-controlled power converters since it owns the benefits of DCMC without the necessity of a high sampling frequency for the inductor current.

Then, OCPC has been implemented efficiently in this DSC proving how this law improves the power converter behavior reducing the voltage deviation and the settling times under load variations.

Nevertheless, these settling times are still important even if specifications imposed in the introduction of this chapter are accomplished. Then, the most appropriated solution is to replace the digital controller for another owning a higher clock-frequency, i.e. a FPGA.

Therefore, our second experimental prototype is based on a FPGA digital controller. In this case, DVMC control law is implemented for the same VR application than in the previous case. The main difference between both power stages is that last one can supply whichever laptop embedded microprocessor since it can deliver up to 36A.

Then, DVMC has been tested using a FPGA and it has been stated how the static and dynamic performances of the digitally-controlled converter have been improved considerably. Nevertheless, OCPC control law using this digital controller cannot be implemented for reasons of time.

However, our second prototype proves that FPGAs is an appropriate candidate for digitally-controlled power converters, especially for those multiphased. In consequence, our future work will consist in to develop an experimental prototype of a multiphase high-frequency digitally-controlled synchronous power converter for high supply current loads oriented to desktop embedded microprocessors using a FPGA as digital controller.

Chapter 6

CONCLUSION

6. CONCLUSION, PERSPECTIVE AND FUTURE WORK.

To achieve efficient embedded power supply modules, several parameters like weight, size, robustness and cost should be taken into account. In the case of switching DC/DC converters, switching frequencies over the MHz should be considered to reduce their size additionally.

Therefore, our efforts have been focused on the study and design of digitally-controlled power supply architectures covering a wide range of loads from the watt (portable applications) up to hundred of watts (telecommunication servers or automotive applications). As a result, a large variety of embedded supply modules for computer μps have been considered in our work research.

Hence, the first part of this dissertation introduces "Distributed Power Supply architectures" which are replacing progressively classical centralized supply units due to their enhanced efficiency and robustness. These distributed topologies are based on several adaptation blocks to optimize the power conversion chain from the electrical grid up to the load. The last conversion blocks just before the loads and which must be placed as close as possible to them are known as PoL or VR depending on the kind of load to supply.

Indeed, PoL and VR topologies minimize transfer losses and achieve optimal power matching between the converter and its corresponding load. Actually, the parts involving a digitally-controlled PoL and VR as well as their most suitable control techniques have been studied to find future answers for present technological challenges.

In general terms, a digitally-controlled power converter is composed by four specific blocks: the power converter, an acquisition or input stage, a digital controller and an output module or DPWM.

Thus, our theoretical analysis of the power stage and its experimental design is presented in chapter three. As concerns the power converter sizing, VRs are not classical DC/DC power converters since they own specific design requirements.

Therefore, the theoretical calculation of the devices involving a high-frequency, high-current and low-voltage VR power converter has been presented. Moreover, some real examples of how to calculate the power stage for a single-phase and a multiphase synchronous Buck power converter have been given using the design

rules described along this dissertation.

In this point, the optimal number of phases for our application have been studied proving that 4, 5 and 6-phased structures give us the best trade-off among efficiency, complexity, ripple values, harmonic content and cost.

Furthermore, different ways to sense the inductor current are shown. As a result, the "Inductor DCR current-sense" technique has been studied in detail. It seems an interesting method for VR applications because it is a lossless technique in which an accurate voltage image of the inductor current can be obtained. Then, the feasibility of this technique has been validated with some example of high-frequency VRs for a wide range of loads including a real multiphase converter. This last concept is especially important since the knowledge of the inductor current is a crucial point for an accurate control of the converter and also to obtain an equilibrated current distribution among phases obtaining the intrinsic benefits of this architecture

Concerning digital control laws presented in chapter four, their theoretical analysis for VRs applications is explained. Thus, a systematic design methodology based on simulation models is employed to optimize the final performances of our experimental prototypes. In fact, the continuous-time and discrete small-signal models defining the behavior of the Synchronous Buck converter is found in first place. As regards to these models, several possibilities for finding their discrete-time description are compared. The second step following our design method is to find the small-signal models for DVMC and DCMC control laws.

An important point in the control law design is the influence of the delay in digital systems. In short, the importance to take this delay into consideration in the final design of the feedback regulation loop has been shown since an excessive delay weakens completely the system behavior.

Thus, DVMC seems a good option for our application because it is quite simple to implement and reasonably robust to high delay values. On the other hand, classical DCMC is difficult to implement due to technological problems, i.e. a high sampling frequency is required. In consequence, it needs very fast ADCs and digital controllers in order to reduce the delay introduced by the analogue-to-discrete conversion and the control law algorithm. In brief, DCMC is less robust

to high delay values than DVMC.

A promising candidate for digitally-controlled power converters is "One-cycle Predictive Current" control law since it owns the advantages of DCMC converters (inductor-current is tracked in this case) and it is less exigent in terms of complexity (lower sampling frequency is required) than classical DCMC. This technique incorporates a cascade voltage regulation loop which corrects the lack of inductor-current regulation of DVMC. Thus, this control law is recommended for future VR applications. OCPC has been implemented efficiently in our first experimental prototype showing its feasibility and how this law improves the power converter behavior reducing the voltage deviation and the settling times under load variations.

Another point treated along this dissertation is the improvement of DVMC and OCPC techniques with the addition of FF techniques reducing the effects of input-voltage and load disturbances respectively.

In order to illustrate and validate our purpose, the implementation of two experimental single-phase high-frequency digitally-controlled synchronous Buck power converters oriented to supply embedded microprocessors of laptop computers has been shown. Then, the first experimental prototype is based on a DSC module as digital controller associated to an external input and output module. These modules have been added to improve the input and output resolution of our digitally-controlled system and to avoid limit-cycle oscillations problems. For this experimental prototype, Simulink/Matlab models are used to validate the algorithms which will be used after in the real prototype. These simulations models have been obtained using the S-Functions of Matlab which allows introducing the digital control law algorithm in C code into the simulation model. Thanks to these models, accurate simulations of the real system are obtained since fix-point, delay and quantization errors are considered in the model. In consequence, the validation of our control laws in these models is a previous step before to be implanted in the experimental prototype.

Nevertheless, this first experimental prototype cannot reach the technical specifications for VR applications in all the cases due to its low clock-frequency. Thus, the duty cycle cannot be refreshed cycle-by-cycle due to the large delay introduced by the control law algorithm. As a consequence, disturbances cannot

be efficiently rejected in real time. Then, the most efficient solution is to replace the digital controller for another owning a higher clock-frequency, i.e. a FPGA like in our second experimental prototype. Moreover, the power stage of this second prototype can supply whichever laptop embedded microprocessor since it can deliver to the load up to 36A. Thus, DVMC law has been implemented using the FPGA controller obtaining acceptable results since static and dynamic performances have been improved considerably respect to our previous experimental prototype. Nevertheless, OCPC control law has not be implemented using this digital controller for questions of time.

Anyway, FPGAs seem an appropriate choice for digitally-controlled power converters, especially for those multiphased thanks to their high clock-frequency and their possibility to manage several operations in parallel.

With regard to our future work perspectives, it is obvious than an important part of the work still has not been completed. The immediate work is to complete OCPC control law in our second prototype and to implement DVMC and OCPC associated to any CS loop in the multiphase one. These works are currently in progress and it is expected to obtain some results in the few next months. At the present moment, our results are not satisfactory.

On the other hand, the possibilities in this power management field are huge. This dissertation serves as a starting point in order to achieve efficient embedded PoL and VR applications in the coming years. On one hand, the important evolution of digital controllers like FPGAs allows to designers a large margin of possibilities to design high-performance control systems. On the other hand, there are a lot of promising techniques which are very effective in analogue systems and which are not still developed in the digital field. Moreover, the flexibility of digital controllers still allows to push the limits of these control laws and to implement non-conservative control methods which are unfeasible in analogue-controlled systems.

Relating to our experimental work, each block can be improved in the future. For example, the input acquisition board works with high-resolution pipelined ADCs. As it has been proved in Fig. 2-18, Windowed-Flash ADCs owning reduced resolution and, therefore; minimal delay can replace those pipelined without an important loss of accuracy in our feedback regulation. This change would allow

us to reduce considerably the delay introduced by ADCs, especially in the critical case of the inductor current loop. On the other hand, more efficient architectures are necessary for the DPWM. In fact, “fast-clock counter” topology only permits to obtain a reduced resolution as it has been explained along this dissertation. Then, high-resolution DPWM topologies can be implemented using HDL description techniques, i.e. a FPGA as shown in point 2.3.3.1.

As concerns to the multiphase power converter, a more complete small-signal modelling is necessary in order to evaluate the interactions of one phase among others. Furthermore, in our small-signal analysis, the high-frequency effects of bulk and decoupling capacitors as well of the inductance has not been considered. Then, these classical passive element models should be replaced for those more complex including these frequency-dependant effects.

On the other hand, the feasibility to obtain very high-frequency controls using FPGAs has been validated. Thus, the control for each phase could be generated independently without additional CS loops. Moreover, FPGAs allows us to use more complex digital filters in the feedback loops obtaining enhanced stability margins and more efficient transient responses against load variations.

Concerning to PoL and VRs applications, digital control could improve considerably their efficiency if the control law of the power converter is changed according to load conditions. Thus, PFM is advised for low-consumption working mode and PWM is preferred otherwise.

In short, we still have come a long way to go in this interesting power management field where the recent evolution of efficient digital controllers have changed the traditional design of these kind of embedded power supplies. Our work team hopes that this dissertation was useful for the reader and for their future designs.

Chapter 7

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Chapter 8

Appendix A: Small-Signal Models Formulation

8. APPENDIX A: SMALL-SIGNAL MODELS

8.1 Power Converter

8.1.1 Continuous-time

In this point, the equations to discern the continuous-time small-signal model of the synchronous Buck power converter have been developed. A detailed formulation of this continuous-time model can be found in a previous work [4.3] and main steps have been summarized in this appendix. Thus, first step is to find the two working modes of the converter during on the switching period. These modes vary depending on both switch status as it can be seen in Fig. A-1.

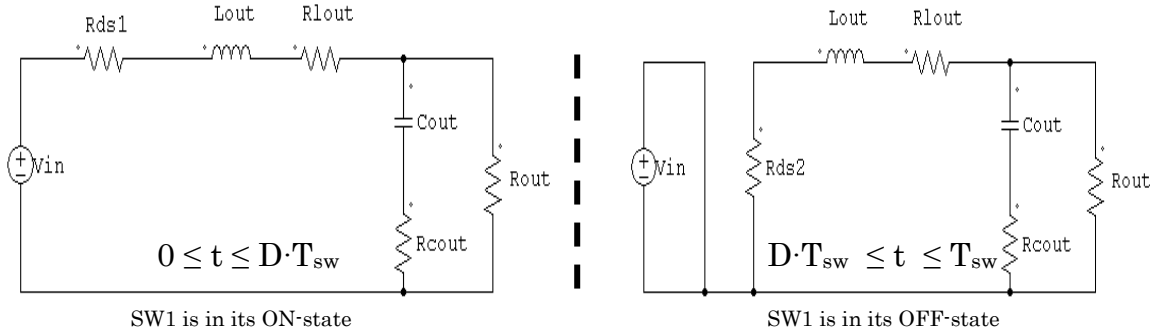

Fig. A- 1 Power converter topologies depending on switch status

The first step is to find the state-space matrix (see Table A-1) in Continuous Conduction Mode (CCM) taking as state-variables the inductor current (il(t)) and the capacitor voltage (vc(t)). Parasitic effects are considered to find the real converter transfer functions.

$$\left.\begin{aligned}\dot{X}(t) &= A\cdot X(t) + B\cdot Vin\\ V_{out}(t) &= C\cdot X(t) + D\cdot Vin\end{aligned}\right\} \quad \text{with} \quad \dot{X}(t) = \begin{pmatrix} \frac{dil}{dt} \\ \frac{dvc}{dt} \end{pmatrix} \quad \text{and} \quad X(t) = \begin{pmatrix} il \\ vc \end{pmatrix} \tag{8.1}$$

Previous to find the open-loop small-signal model, the average-value converter model should be calculated. This model provides an approximated idea of the converter behavior during the whole switching period giving us a description of the average values of the state variables depending on the duty-cycle (d).

To find this average model, (8.5) and (8.7) should be combined finding:

$$\begin{aligned}\dot{X}p &= (A_1\cdot X + B_1\cdot V_{in})\cdot d + (A_2\cdot X + B_2\cdot V_{in})\cdot(1-d)\\ V_{out} &= (C_1\cdot X + D_1\cdot V_{in})\cdot d + (C_2\cdot X + D_2\cdot V_{in})\cdot(1-d)\end{aligned} \tag{8.2}$$

$$\begin{cases} L_{out}\cdot\dfrac{dil}{dt} = Vin - il\cdot(R_{lout}+R_{ds1}) - V_{out} \\ C_{out}\cdot\dfrac{dvc}{dt} = il - i_{out} = il - \dfrac{V_{out}}{R_{out}} \end{cases} \qquad 0 \le t \le D\cdot T_{sw} \tag{8.3}$$

$$\begin{cases} \dfrac{dil}{dt} = \dfrac{1}{L_{out}}\cdot\left(Vin - il\cdot\left(R_{lout}+R_{ds1}+\dfrac{R_{out}\cdot R_{cout}}{R_{out}+R_{cout}}\right) - vc\cdot\left(\dfrac{R_{out}}{R_{out}+R_{cout}}\right)\right) \\ \dfrac{dvc}{dt} = \dfrac{1}{C_{out}}\cdot\left(il\cdot\left(\dfrac{R_{out}}{R_{out}+R_{cout}}\right) - vc\cdot\left(\dfrac{1}{R_{out}+R_{cout}}\right)\right) \end{cases} \tag{8.4}$$

$$V_{out} = il\cdot\frac{R_{out}\cdot R_{cout}}{R_{out}+R_{cout}} + vc\cdot\frac{R_{out}}{R_{out}+R_{cout}}$$

$$\begin{cases} A_1 = \begin{pmatrix} \dfrac{-1}{L_{out}}\left(R_{lout}+R_{ds1}+\dfrac{R_{out}\cdot R_{cout}}{R_{out}+R_{cout}}\right) & \dfrac{-R_{out}}{L_{out}(R_{out}+R_{cout})} \\ \dfrac{R_{out}}{C_{out}(R_{out}+R_{cout})} & \dfrac{-1}{C_{out}(R_{out}+R_{cout})} \end{pmatrix} & B_1 = \begin{bmatrix} \dfrac{1}{L_{out}} \\ 0 \end{bmatrix} \\ C_1 = \begin{pmatrix} \dfrac{R_{out}\cdot R_{cout}}{R_{out}+R_{cout}} & \dfrac{R_{out}}{R_{out}+R_{cout}} \end{pmatrix} & D_1 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \end{cases} \tag{8.5}$$

$$\begin{cases} L_{out}\cdot\dfrac{dil}{dt} = -il\cdot(R_{lout}+R_{ds2}) - V_{out} \\ C_{out}\cdot\dfrac{dvc}{dt} = il - i_{out} = il - \dfrac{V_{out}}{R_{out}} \end{cases} \qquad D\cdot T_{sw} \le t \le T_{sw} \tag{8.6}$$

$$\begin{cases} \dfrac{dil}{dt} = \dfrac{1}{L_{out}}\cdot\left(-il\cdot\left(R_{lout}+R_{ds2}+\dfrac{R_{out}\cdot R_{cout}}{R_{out}+R_{cout}}\right) - vc\cdot\left(\dfrac{R_{out}}{R_{out}+R_{cout}}\right)\right) \\ \dfrac{dvc}{dt} = \dfrac{1}{C_{out}}\cdot\left(il\cdot\left(\dfrac{R_{out}}{R_{out}+R_{cout}}\right) - vc\cdot\left(\dfrac{1}{R_{out}+R_{cout}}\right)\right) \end{cases} \tag{8.7}$$

$$V_{out} = il\cdot\frac{R_{out}\cdot R_{cout}}{R_{out}+R_{cout}} + vc\cdot\frac{R_{out}}{R_{out}+R_{cout}}$$

$$\begin{cases} A_2 = \begin{pmatrix} \dfrac{-1}{L_{out}}\left(R_{lout}+R_{ds2}+\dfrac{R_{out}\cdot R_{cout}}{R_{out}+R_{cout}}\right) & \dfrac{-R_{out}}{L_{out}(R_{out}+R_{cout})} \\ \dfrac{R_{out}}{C_{out}(R_{out}+R_{cout})} & \dfrac{-1}{C_{out}(R_{out}+R_{cout})} \end{pmatrix} & B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \\ C_2 = \begin{pmatrix} \dfrac{R_{out}\cdot R_{cout}}{R_{out}+R_{cout}} & \dfrac{R_{out}}{R_{out}+R_{cout}} \end{pmatrix} & D_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \end{cases} \tag{8.8}$$

Table A- 1 State-Space matrix for the Buck converter

And, reformulating last equations, it can be obtained:

$$\begin{aligned} \dot{Xp} &= Ae\cdot X + Be\cdot Vg \\ V_{out} &= Ce\cdot X + De\cdot Vg \end{aligned} \quad \left\{\begin{aligned} Ae &= A_{1.}\cdot d + A_{2.}\cdot(1-d) \\ Be &= B_{1.}\cdot d + B_{2.}\cdot(1-d) \\ Ce &= C_{1.}\cdot d + C_{2.}\cdot(1-d) \\ De &= D_{1.}\cdot d + D_{2.}\cdot(1-d) \end{aligned}\right\} \rightarrow \left\{\begin{aligned} Ae &= (A_1 - A_2)\cdot d + A_{2.} \\ Be &= B_{1.}\cdot d \\ Ce &= C_2 \\ De &= 0 \end{aligned}\right\} \tag{8.9}$$

With coefficients:

$$\left\{\begin{aligned} A_e &= \begin{pmatrix} \dfrac{-1}{L_{out}}\left(R_{lout} + R_{ds} + \dfrac{R_{out}\cdot R_{cout}}{R_{out}+R_{cout}}\right) & \dfrac{-R_{out}}{L_{out}(R_{out}+R_{cout})} \\ \dfrac{R_{out}}{C_{out}(R_{out}+R_{cout})} & \dfrac{-1}{C_{out}(R_{out}+R_{cout})} \end{pmatrix} \quad B_e = \begin{bmatrix} \dfrac{d}{L_{out}} \\ 0 \end{bmatrix} \\ C_e &= \begin{pmatrix} \dfrac{R_{out}\cdot R_{cout}}{R_{out}+R_{cout}} & \dfrac{R_{out}}{R_{out}+R_{cout}} \end{pmatrix} \quad D_e = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \end{aligned}\right\} \tag{8.10}$$

with : $R_{ds} = R_{ds2} + (R_{ds1} - R_{ds2})\cdot D$ as the steady-state value of the drain-to-source resistance

Last system gives us the average representation of the Buck Converter. This model is reproduced using Simulink in the Fig. A-2. In this model, the steady value of state-space variables is shown. These steady-state values are represented by the average-state matrix, i.e. Ae^0.

$$X = -\left(Ae^o\right)^{-1}\cdot Be^0\cdot V_{in} \tag{8.11}$$

With:

$$\begin{aligned} &\left(Ae^o\right)^{-1} = \frac{1}{\varsigma}\begin{bmatrix} \dfrac{-1}{C_{out}\cdot Re_2} & \dfrac{Re_1}{L_{out}} \\ \dfrac{-Re_1}{C_{out}} & \dfrac{-Re}{L_{out}} \end{bmatrix};\quad Be^0 = \begin{bmatrix} \dfrac{D}{L_{out}} \\ 0 \end{bmatrix} \\ &Re = R_{lout} + R_{ds} + \frac{R_{out}\cdot R_{cout}}{R_{out}+R_{cout}};\quad Re_1 = \frac{R_{out}}{(R_{out}+R_{cout})};\quad Re_2 = R_{out} + R_{cout} \\ &\varsigma = \frac{1}{L_{out}C_{out}}\cdot\left(\frac{Re}{Re_2} + Re_1^{\,2}\right) = \frac{1}{L_{out}C_{out}}\cdot\left(\frac{R_{lout}+R_{ds}+R_{out}}{R_{out}+R_{cout}}\right) \end{aligned} \tag{8.12}$$

And:

$$X_1 = I_L = \frac{1}{R_{lout}+R_{ds}+R_{out}}\cdot Vg\cdot D \tag{8.13}$$

$$X_2 = V_c = \frac{R_{out}}{R_{lout}+R_{ds}+R_{out}}\cdot Vg\cdot D \tag{8.14}$$

$$V_{out} = \frac{R_{out} \cdot Vg \cdot D}{R_{lout} + R_{ds} + R_{out}} \tag{8.15}$$

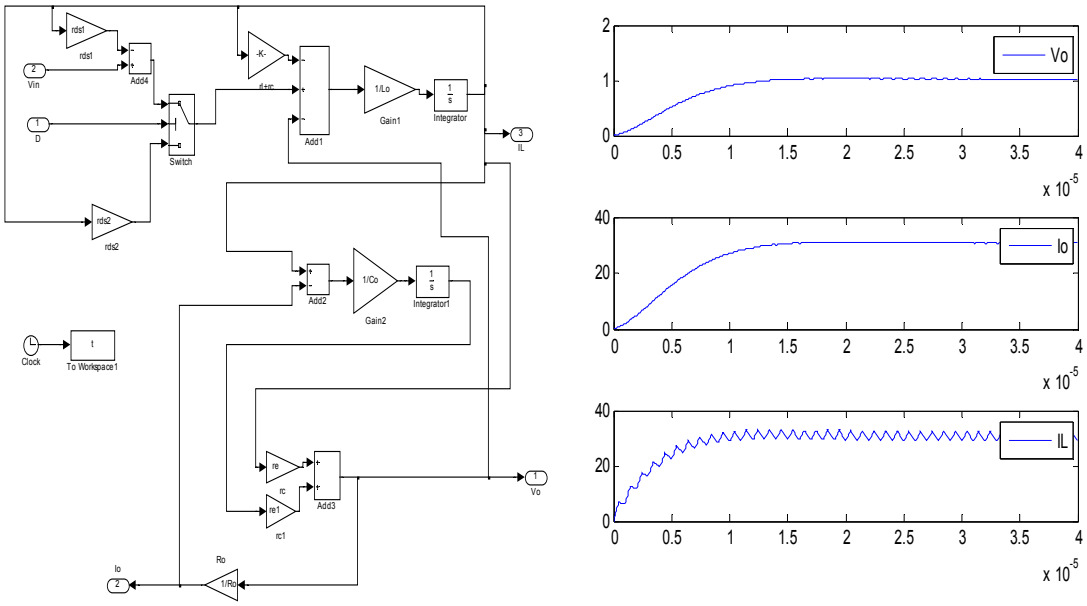

Fig. A- 2 Buck Converter switched-model and output voltage (top), output current (middle) and inductor current (bottom)

The linear-model can be found replacing (8.16) in (8.9):

$$\begin{aligned} &x(t) = X + \hat{x}\ ; \qquad v_{in}(t) = V_{in} + \hat{v}_{in}\ ; \\ &v_{out}(t) = V_{out} + \hat{v}_{out}\ ; \quad d(t) = D + \hat{d}\ ; \end{aligned} \tag{8.16}$$

Obtaining:

$$\begin{cases} \dot{\hat{x}} = Ae^0 \cdot \hat{x} + Be^0 \cdot \hat{V}_{in} + \left[(A_1 - A_2) X + (B_1 - B_2) V_{in} \right] \cdot \hat{d} = Ae^0 \cdot \hat{x} + Be^0 \cdot \hat{V}_{in} + \left[B_1 \cdot V_{in} \right] \cdot \hat{d} \\ \dot{\hat{v}}_{out} = Ce^0 \cdot \hat{x} + De^0 \cdot \hat{V}_{in} + \left[(C_1 - C_2) X \right] \cdot d = \hat{Ce}^0 \cdot \hat{x} \end{cases} \tag{8.17}$$

And, finally:

$$\dot{\hat{x}} = \begin{pmatrix} \dot{\hat{dil}}/dt \\ \dot{\hat{dvc}}/dt \end{pmatrix} = \begin{pmatrix} \frac{-1}{L_{out}} \cdot \left(R_{lout} + R_{ds} + \frac{R_{out} \cdot R_{cout}}{R_{out} + R_{cout}} \right) & \frac{-R_{out}}{L_{out} \cdot (R_{out} + R_{cout})} \\ \frac{R_{out}}{C_{out} \cdot (R_{out} + R_{cout})} & \frac{-1}{C_{out} \cdot (R_{out} + R_{out})} \end{pmatrix} \cdot \begin{pmatrix} \hat{dil}/dt \\ \hat{dvc}/dt \end{pmatrix} + \begin{pmatrix} D/L_{out} \\ 0 \end{pmatrix} \cdot \hat{V}_{in} + \begin{pmatrix} V_{in}/L_{out} \\ 0 \end{pmatrix} \cdot \hat{d} \tag{8.18}$$

$$\dot{\hat{v}}_{out} = \begin{pmatrix} \frac{R_{out} \cdot R_{cout}}{R_{out} + R_{cout}} & \frac{R_{out}}{R_{out} + R_{cout}} \end{pmatrix} \cdot \begin{pmatrix} \hat{dil}/dt \\ \hat{dvc}/dt \end{pmatrix} \tag{8.19}$$

This procedure to find the open-loop small-signal transfer functions was developed in detail in a previous work obtaining next results [4.3] .

- Input voltage-to-inductor current transfer function:

$$G_{ii(s)}=\left.\frac{\hat{I}_L}{\hat{V}in}\right|_{\hat{i}o=\hat{d}=0}=\frac{(1+s\cdot C_{out})\cdot(R_{cout}+R_{out})\cdot D}{s^2\cdot L_{out}\cdot C_{out}\cdot(R_{cout}+R_{out})+s\cdot\left[L_{out}+C_{out}\cdot(R_{ds}\cdot(R_{cout}+R_{out}))+R_L\cdot(R_{cout}+R_{out})+R_{out}\cdot R_{cout}\right]+R_{out}+R_L+R_{ds}} \quad (8.20)$$

- Input voltage-to-output voltage transfer function:

$$G_{oi(s)}=\left.\frac{\hat{V}_{out}}{\hat{V}_{in}}\right|_{\hat{i}o=\hat{d}=0}=\frac{(1+s\cdot R_{cout}\cdot C_{out})\cdot R_{out}\cdot D}{s^2\cdot L_{out}\cdot C_{out}\cdot(R_{cout}+R_{out})+s\cdot\left[L_{out}+C_{out}\cdot(R_{ds}\cdot(R_{cout}+R_{out}))+R_L\cdot(R_{cout}+R_{out})+R_{out}\cdot R_{cout}\right]+R_{out}+R_L+R_{ds}} \quad (8.21)$$

- Control-to-inductor current transfer function:

$$G_{id(s)}=\left.\frac{\hat{I}_L}{\hat{d}}\right|_{\hat{i}o=\hat{V}in=0}=\frac{(1+s\cdot C_{out})\cdot(R_{cout}+R_{out})\cdot V_{in}}{s^2\cdot L_{out}\cdot C_{out}\cdot(R_{cout}+R_{out})+s\cdot\left[L_{out}+C_{out}\cdot(R_{ds}\cdot(R_{cout}+R_{out}))+R_L\cdot(R_{cout}+R_{out})+R_{out}\cdot R_{cout}\right]+R_{out}+R_L+R_{ds}} \quad (8.22)$$

- Control-to-output voltage transfer function:

$$G_{od(s)}=\left.\frac{\hat{V}_{out}}{\hat{d}}\right|_{\hat{i}o=\hat{V}in=0}=\frac{(1+s\cdot R_{cout}\cdot C_{out})\cdot R_{out}\cdot V_{in}}{s^2\cdot L_{out}\cdot C_{out}\cdot(R_{cout}+R_{out})+s\cdot\left[L_{out}+C_{out}\cdot(R_{ds}\cdot(R_{cout}+R_{out}))+R_L\cdot(R_{cout}+R_{out})+R_{out}\cdot R_{cout}\right]+R_{out}+R_L+R_{ds}} \quad (8.23)$$

- Open-loop output impedance transfer function:

$$Z_{out(s)}=\left.\frac{\hat{V}_{out}}{\hat{I}_{out}}\right|_{\hat{d}=\hat{V}in=0}=\frac{s^2\cdot R_{out}\cdot L_{out}\cdot C_{out}\cdot R_{cout}+s\cdot R_{out}\cdot(L_{out}+C_{out}\cdot R_{cout}\cdot R_{lout})+R_{out}\cdot R_{lout}}{s^2\cdot L_{out}\cdot C_{out}\cdot(R_{out}+R_{cout})+s\cdot(L_{out}+C_{out}\cdot(R_{cout}\cdot R_{lout}+R_{out}\cdot(R_{lout}+R_{cout}))+R_{out}} \quad (8.24)$$

8.1.2 Discrete-time

8.1.2.1 First approach. Discrete-time behaviour

In this first approach, the parasitic elements are not considered and the low-ripple approach is used where input and output voltages are almost constant during this switching period

Hence, inductor current should be sampled in equally-time intervals, which means, constant sampling frequency. For an easy formulation, inductor current for present switching period is considered as the goal which should be reached at the end of the current switching period as shown in Fig. A-3.

Thus, the continuous-time behavior of the inductor current is defined by:

$$i_L(t)=i_L(0)+m_1\cdot d\cdot T_{sw}+m_2\cdot(1-d)\cdot T_{sw} \quad (8.25)$$

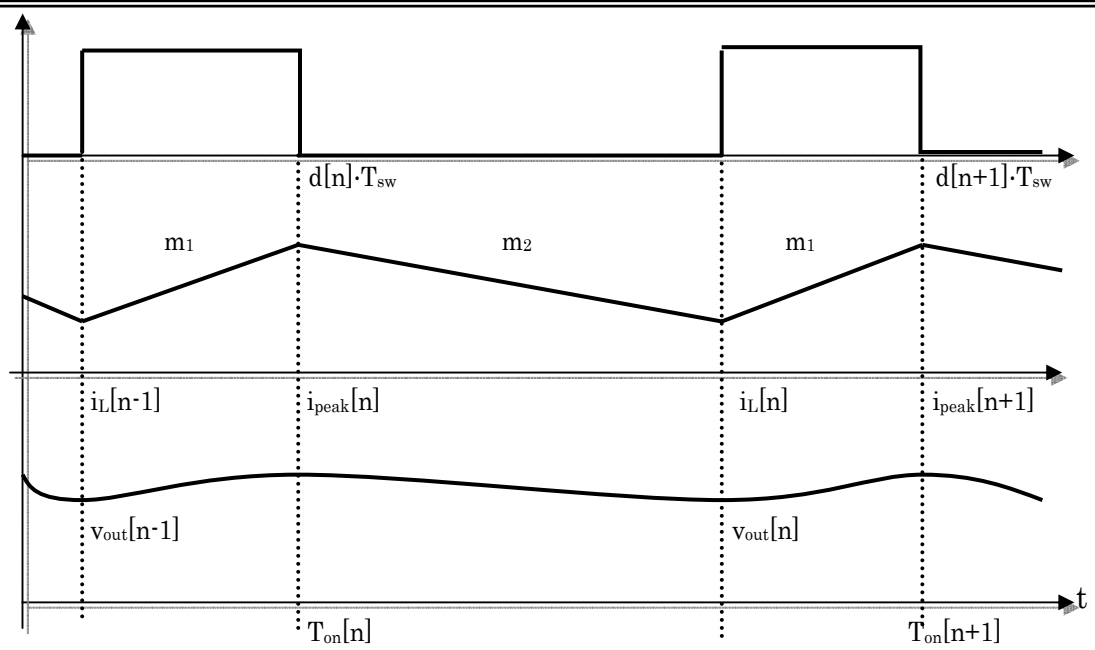

Fig. A- 3 State-space variables evolution in discrete-time

The discrete-time behavior of the converter state-space variables is:

$$i_L[n] = i_L[n-1] + m_1 \cdot d[n] \cdot T_{sw} + m_2 \cdot (1-d[n]) \cdot T_{sw} \tag{8.26}$$

$$i_L[n] = i_L[n-1] + (m_1 - m_2) \cdot d[n] \cdot T_{sw} + m_2 \cdot T_{sw} \tag{8.27}$$

Where m_1 and m_2 are the inductor current slopes for the ON-time and OFF-time periods respectively:

$$m_1 = \frac{V_{in} - V_{out}}{L_{out}};\ m_2 = \frac{-V_{out}}{L_{out}} \tag{8.28}$$

$$i_L[n] = i_L[n-1] + \frac{V_{in}}{L_{out}} \cdot d[n] \cdot T_{sw} - \frac{V_{out}}{L_{out}} \cdot T_{sw} \tag{8.29}$$

In order to formulate correctly state-space matrix, last equation should be put forward in spite of this approach only is valid if low ripple hypothesis is considered; i.e. input and output voltages are almost constant

$$i_L[n+1] = i_L[n] + \frac{V_{in}}{L_{out}} \cdot d[n+1] \cdot T_{sw} - \frac{V_{out}[n]}{L_{out}} \cdot T_{sw} \tag{8.30}$$

Similarly than in the inductor case, the output voltage evolves as:

$$V_{out}[n+1] = V_{out}[n] + \frac{T_{sw}}{C_{out}} \cdot \left(i_L[n+1] - \frac{V_{out}[n]}{R_{out}} \right) \tag{8.31}$$

Next step is to find the discrete-time state-space matrix for the converter. Thus, inserting (8.30) in (8.31).

$$V_{out}[n+1] = V_{out}[n] + \frac{T_{sw}}{C_{out}} \cdot \left(i_L[n] + \frac{V_{in}}{L_{out}} \cdot T_{sw} \cdot d[n+1] - \frac{V_{out}[n]}{L_{out}} \cdot T_{sw} - \frac{V_{out}[n]}{R_{out}} \right) \tag{8.32}$$

Hence:

$$V_{out}[n+1]=\left(\frac{1}{1+\frac{T_{sw}}{C_{out}\cdot R_{out}}}\right)\cdot V_{out}[n]\cdot\left(1-\frac{T_{sw}^2}{C_{out}\cdot L_{out}}\right)+\frac{T_{sw}^2}{C_{out}\cdot L_{out}}\cdot V_{in}\cdot d[n+1]+\frac{T_{sw}}{C_{out}}\cdot i[n] \quad (8.33)$$

Now, the discrete-time state-space matrix can be formulated and Z-Transform should be applied to obtain the discrete-time model.

$$\begin{pmatrix} i_L[n+1] \\ v_{out}[n+1] \end{pmatrix}=\begin{pmatrix} 1 & \frac{-T_{sw}}{L_{out}} \\ \left(\frac{1}{1+\frac{T_{sw}}{C_{out}\cdot R_{out}}}\right)\cdot\frac{T_{sw}}{C_{out}} & \left(\frac{1}{1+\frac{T_{sw}}{C_{out}\cdot R_{out}}}\right)\cdot\left(1-\frac{T_{sw}^2}{L_{out}\cdot C_{out}}\right) \end{pmatrix}\cdot\begin{pmatrix} i_L[n] \\ v_{out}[n] \end{pmatrix}+$$
$$\begin{pmatrix} \frac{V_{in}\cdot T_{sw}}{L_{out}} \\ \left(\frac{1}{1+\frac{T_{sw}}{C_{out}\cdot R_{out}}}\right)\cdot\frac{V_{in}\cdot T_{sw}^2}{L_{out}\cdot C_{out}} \end{pmatrix}\cdot d[n+1] \quad (8.34)$$

$$\downarrow$$

$$\begin{pmatrix} z\cdot I_L(z) \\ z\cdot V_{out}(z) \end{pmatrix}=\begin{pmatrix} 1 & \frac{-T_{sw}}{L_{out}} \\ \left(\frac{1}{1+\frac{T_{sw}}{C_{out}\cdot R_{out}}}\right)\cdot\frac{T_{sw}}{C_{out}} & \left(\frac{1}{1+\frac{T_{sw}}{C_{out}\cdot R_{out}}}\right)\cdot\left(1-\frac{T_{sw}^2}{L_{out}\cdot C_{out}}\right) \end{pmatrix}\cdot\begin{pmatrix} I_L(z) \\ V_{out}(z) \end{pmatrix}+$$
$$\begin{pmatrix} \frac{V_{in}\cdot T_{sw}}{L_{out}} \\ \left(\frac{1}{1+\frac{T_{sw}}{C_{out}\cdot R_{out}}}\right)\cdot\frac{V_{in}\cdot T_{sw}^2}{L_{out}\cdot C_{out}} \end{pmatrix}\cdot D(z)\cdot z \quad (8.35)$$

Like in the continuous-time case, the discrete-time transfer function defining the converter behavior is defined by:

$$G(z)=\begin{pmatrix} I_L(z) \\ V_{out}(z) \end{pmatrix}=\left(z\cdot I-A\right)^{-1}\cdot B\cdot D(z)\cdot z \quad (8.36)$$

$$G(z)=\frac{\left(\frac{\left(z-\frac{1}{1+\frac{T_{sw}}{R_{out}\cdot C_{out}}}\right)\cdot T_{sw}\cdot V_{in}}{L_{out}}\right)}{z^2-z\cdot\left(1+\frac{R_{out}}{L_{out}}\cdot\left(\frac{L_{out}\cdot C_{out}-T_{sw}^2}{R_{out}\cdot C_{out}+T_{sw}}\right)\right)+\frac{R_{out}}{L_{out}}\cdot\left(\frac{L_{out}\cdot C_{out}-T_{sw}^2}{R_{out}\cdot C_{out}+T_{sw}}\right)+\frac{T_{sw}^2\cdot R_{out}}{L_{out}\cdot\left(R_{out}\cdot C_{out}+T_{sw}\right)}}\cdot D(z)\cdot z \quad (8.37)$$

Hence:

$$G_{od}(z)=\frac{\frac{T_{sw}^2\cdot V_{in}}{L_{out}\cdot C_{out}}\cdot\frac{1}{1+\frac{T_{sw}}{R_{out}\cdot C_{out}}}\cdot z^2}{z^2-z\cdot\left(1+\frac{R_{out}}{L_{out}}\cdot\left(\frac{L_{out}\cdot C_{out}-T_{sw}^2}{R_{out}\cdot C_{out}+T_{sw}}\right)\right)+\frac{R_{out}}{L_{out}}\cdot\left(\frac{L_{out}\cdot C_{out}-T_{sw}^2}{R_{out}\cdot C_{out}+T_{sw}}\right)+\frac{T_{sw}^2\cdot R_{out}}{L_{out}\cdot\left(R_{out}\cdot C_{out}+T_{sw}\right)}}\cdot D(z) \quad (8.38)$$

$$G_{id}(z)=\frac{\left(z-\frac{1}{1+\frac{T_{sw}}{R_{out}\cdot C_{out}}}\right)\cdot\frac{T_{sw}\cdot V_{in}}{L_{out}}\cdot z}{z^2-z\cdot\left(1+\frac{R_{out}}{L_{out}}\cdot\left(\frac{L_{out}\cdot C_{out}-T_{sw}^2}{R_{out}\cdot C_{out}+T_{sw}}\right)\right)+\frac{R_{out}}{L_{out}}\cdot\left(\frac{L_{out}\cdot C_{out}-T_{sw}^2}{R_{out}\cdot C_{out}+T_{sw}}\right)+\frac{T_{sw}^2\cdot R_{out}}{L_{out}\cdot\left(R_{out}\cdot C_{out}+T_{sw}\right)}}\cdot D(z) \quad (8.39)$$

Previous results become quite complicated if parasitic effects are taken into account. Now, the ON and OFF-slopes of the inductor current vary as follows:

$$m_1[n]=\frac{V_{in}-V_{out}[n]-i_L[n]\cdot R_L[n]}{L_{out}};\quad m_2[n]=\frac{-V_{out}[n]-i_L[n]\cdot R_L[n]}{L_{out}} \quad (8.40)$$

With: $$R_L[n]=DCR+\left(R_{ds1}-R_{ds2}\right)\cdot d[n]+R_{ds2} \quad (8.41)$$

Repeating last process, the new equations defining the new converter behavior are found. Now, the output capacitor voltage is taken as second state-space variable.

$$i_L\left[n+1\right]=i_L\left[n\right]+\frac{V_{in}}{L_{out}}\cdot T_{sw}\cdot d[n+1]-v_c[n]\cdot\frac{R_{out}}{R_{out}+R_{cout}}\cdot\frac{T_{sw}}{L_{out}}-\frac{R_L\left[n+1\right]}{L_{out}}\cdot T_{sw}\cdot i_L\left[n+1\right] \quad (8.42)$$

$$v_c[n+1]=v_c[n]+\frac{T_{sw}}{C_{out}}\cdot\left(i_L\left[n\right]+\frac{V_{in}}{L_{out}}\cdot T_{sw}\cdot d[n+1]-\frac{R_{out}}{R_{out}+R_{cout}}\cdot\frac{T_{sw}}{L_{out}}\cdot v_c[n]-\right.$$
$$\left.\frac{R_{out}\cdot R_{cout}}{R_{out}+R_{cout}}\cdot\frac{T_{sw}}{L_{out}}\cdot i_L\left[n+1\right]-\frac{R_L\left[n+1\right]}{L_{out}}\cdot T_{sw}\cdot i_L\left[n+1\right]-\frac{1}{R_{out}+R_{cout}}\cdot v_c[n]-\frac{R_{cout}}{R_{out}+R_{cout}}\cdot i_L\left[n+1\right]\right) \quad (8.43)$$

8.1.2.2 Second approach. Sampled-data formulation of the continuous-time model

Hence, a discrete-time or sampled-data system can be expressed with the following system of equation. This later is based on their corresponding continuous-time set of state-space matrix as it is shown in (8.9).

$$\begin{aligned}\hat{x}[n+1] &= \Phi \cdot \hat{x}[n] + \gamma \cdot \hat{d}[n] \\ \hat{y}[n] &= C \cdot \hat{x}[n]\end{aligned} \tag{8.44}$$

In the specific case of the Buck converter and using their average representation shown in (8.9), it can be deduced the values of the discrete-time state-space matrix as follows:

$$\Phi = e^{A_1 \cdot D \cdot T_{sw}} \cdot e^{A_2 \cdot (1-D) \cdot T_{sw}} = e^{A_e \cdot T_{sw}} = e^{A_2 \cdot T_{sw}} \tag{8.45}$$

$$\alpha = \left(A_1 - A_2\right) \cdot x[n] + \left(B_1 - B_2\right) \cdot V_{in} = B_1 = \begin{pmatrix} \frac{V_{in}}{L_{out}} \\ 0 \end{pmatrix} \tag{8.46}$$

$$\gamma = \Phi \cdot \alpha \cdot T_{sw} = e^{A_2 \cdot T_{sw}} \cdot \begin{pmatrix} \frac{V_{in}}{L_{out}} \\ 0 \end{pmatrix} \cdot T_{sw} \tag{8.47}$$

Equations (8.44) to (8.47) summarize the discrete-time Buck converter model. Next, matrix exponentials of previous equation are replaced by their first order approximation as follows [4.6]

$$\Phi = e^{A_2 \cdot T_{sw}} \approx I + A_2 \cdot T_{sw} = \begin{pmatrix} 1 & \frac{-T_{sw}}{L_{out}} \\ \frac{T_{sw}}{C_{out}} & 1 - \frac{T_{sw}}{R_{out} \cdot C_{out}} \end{pmatrix} \tag{8.48}$$

Now, delay can be added in (8.47) to be taken into account. Delay is only added to this block because of the delay effects is considered only in the duty-cycle generation.

$$\gamma = e^{A_2 \cdot (T_{sw} - t_d)} \cdot \begin{pmatrix} \frac{V_{in}}{L_{out}} \\ 0 \end{pmatrix} \cdot T_{sw} = \begin{pmatrix} \frac{V_{in} \cdot T_{sw}}{L_{out}} \\ \frac{m \cdot V_{in} \cdot T_{sw}}{L_{out} \cdot C_{out}} \end{pmatrix} \tag{8.49}$$

With:

$$m = T_{sw} - t_d \tag{8.50}$$

Replacing (8.48) and (8.49) in (8.44) and considering capacitor ESR like the dominant parasitic effect $\left(R_{cout} \ll R_{out}; R_L \ll R_{out}\right)$, it can be obtained:

$$\hat{x}[n+1] = \underbrace{\begin{pmatrix} 1 & \frac{-T_{sw}}{L_{out}} \\ \frac{T_{sw}}{C_{out}} & 1-\frac{T_{sw}}{R_{out}\cdot C_{out}} \end{pmatrix}}_{\Phi} \cdot \hat{x}[n] + \underbrace{\begin{pmatrix} \frac{V_{in}\cdot T_{sw}}{L_{out}} \\ \frac{m\cdot V_{in}\cdot T_{sw}}{L_{out}\cdot C_{out}} \end{pmatrix}}_{\gamma} \cdot \hat{d}[n] \tag{8.51}$$

$$\hat{y}[n] = \begin{pmatrix} R_{cout} & 1 \end{pmatrix} \cdot \hat{x}[n]$$

Like in the previous procedure, the Z-Transform should be applied to obtain the discrete-time model using the sampled-time equivalent of (8.36).

$$X(z) = \begin{pmatrix} I_L(z) \\ V_c(z) \end{pmatrix} = \left(z\cdot I - \Phi\right)^{-1} \cdot \gamma \cdot d(z) \tag{8.52}$$

$$X(z) = \frac{\begin{pmatrix} \frac{V_{in}\cdot T_{sw}}{L_{out}} \cdot \left(z-1+\frac{T_{sw}}{R_{out}\cdot C_{out}} - \frac{m\cdot T_{sw}}{L_{out}\cdot C_{out}} \right) \\ \frac{V_{in}\cdot T_{sw}}{L_{out}\cdot C_{out}} \cdot \left(T_{sw} + m\cdot\left(z-1\right)\right) \end{pmatrix}}{z^2 + z\cdot\left(\frac{T_{sw}}{R_{out}\cdot C_{out}} - 2\right) + 1 - \frac{T_{sw}}{R_{out}\cdot C_{out}} + \frac{T_{sw}^2}{L_{out}\cdot C_{out}}} \cdot D(z) \tag{8.53}$$

Thus, the control-to-inductor current transfer function and the control-to-capacitor voltage are:

$$I_L(z) = \frac{\frac{V_{in}\cdot T_{sw}}{L_{out}} \cdot \left(z-1+\frac{T_{sw}}{R_{out}\cdot C_{out}} - \frac{m\cdot T_{sw}}{L_{out}\cdot C_{out}} \right)}{z^2 + z\cdot\left(\frac{T_{sw}}{R_{out}\cdot C_{out}} - 2\right) + 1 - \frac{T_{sw}}{R_{out}\cdot C_{out}} + \frac{T_{sw}^2}{L_{out}\cdot C_{out}}} \cdot D(z) \tag{8.54}$$

$$V_c(z) = \frac{\frac{V_{in}\cdot T_{sw}}{L_{out}\cdot C_{out}} \cdot \left(T_{sw} + m\cdot\left(z-1\right)\right)}{z^2 + z\cdot\left(\frac{T_{sw}}{R_{out}\cdot C_{out}} - 2\right) + 1 - \frac{T_{sw}}{R_{out}\cdot C_{out}} + \frac{T_{sw}^2}{L_{out}\cdot C_{out}}} \cdot D(z) \tag{8.55}$$

Finally, the control-to-output voltage transfer function is found as follows:

$$Y(z) = \begin{pmatrix} R_{cout} & 1 \end{pmatrix} \cdot \frac{\begin{pmatrix} \frac{V_{in}\cdot T_{sw}}{L_{out}} \cdot \left(z-1+\frac{T_{sw}}{R_{out}\cdot C_{out}} - \frac{m\cdot T_{sw}}{L_{out}\cdot C_{out}} \right) \\ \frac{V_{in}\cdot T_{sw}}{L_{out}\cdot C_{out}} \cdot \left(T_{sw} + m\cdot\left(z-1\right)\right) \end{pmatrix}}{z^2 + z\cdot\left(\frac{T_{sw}}{R_{out}\cdot C_{out}} - 2\right) + 1 - \frac{T_{sw}}{R_{out}\cdot C_{out}} + \frac{T_{sw}^2}{L_{out}\cdot C_{out}}} \cdot D(z) \tag{8.56}$$

$$V_{out}(z)=\frac{\frac{R_{cout}\cdot V_{in}\cdot T_{sw}}{L_{out}\cdot C_{out}}\cdot\left(z-1+\frac{T_{sw}}{R_{out}\cdot C_{out}}-\frac{m\cdot T_{sw}}{L_{out}\cdot C_{out}}\right)+\frac{V_{in}\cdot T_{sw}}{L_{out}}\cdot\left(T_{sw}+m\cdot(z-1)\right)}{z^2+z\cdot\left(\frac{T_{sw}}{R_{out}\cdot C_{out}}-2\right)+1-\frac{T_{sw}}{R_{out}\cdot C_{out}}+\frac{T_{sw}^2}{L_{out}\cdot C_{out}}}\cdot D(z) \quad (8.57)$$

$$V_{out}(z)=\frac{\frac{V_{in}\cdot T_{sw}}{L_{out}\cdot C_{out}}\cdot\left(\frac{T_{sw}\cdot L_{out}\cdot R_{cout}-R_{out}\cdot C_{out}\cdot L_{out}\cdot R_{cout}+z\cdot R_{out}\cdot C_{out}\cdot L_{out}\cdot R_{cout}-T_{sw}\cdot R_{out}\cdot R_{cout}\cdot m}{R_{out}\cdot L_{out}}+T_{sw}+m\cdot(z-1)\right)}{z^2+z\cdot\left(\frac{T_{sw}}{R_{out}\cdot C_{out}}-2\right)+1-\frac{T_{sw}}{R_{out}\cdot C_{out}}+\frac{T_{sw}^2}{L_{out}\cdot C_{out}}}\cdot D(z) \quad (8.58)$$

$$V_{out}(z)=\frac{\frac{V_{in}\cdot T_{sw}}{L_{out}\cdot C_{out}}\cdot\left(\frac{T_{sw}\cdot R_{out}}{R_{out}}-R_{out}\cdot C_{out}+z\cdot C_{out}\cdot R_{cout}-\frac{T_{sw}\cdot R_{cout}\cdot m}{L_{out}}+T_{sw}+m\cdot(z-1)\right)}{z^2+z\cdot\left(\frac{T_{sw}}{R_{out}\cdot C_{out}}-2\right)+1-\frac{T_{sw}}{R_{out}\cdot C_{out}}+\frac{T_{sw}^2}{L_{out}\cdot C_{out}}}\cdot D(z) \quad (8.59)$$

$$V_{out}(z)=\frac{\frac{V_{in}\cdot T_{sw}}{L_{out}\cdot C_{out}}\cdot\left(z\cdot(m+C_{out}\cdot R_{cout})+\frac{T_{sw}\cdot R_{out}}{R_{out}}-R_{cout}\cdot C_{out}+\frac{T_{sw}\cdot R_{cout}\cdot m}{L_{out}}+T_{sw}-m\right)}{z^2+z\cdot\left(\frac{T_{sw}}{R_{out}\cdot C_{out}}-2\right)+1-\frac{T_{sw}}{R_{out}\cdot C_{out}}+\frac{T_{sw}^2}{L_{out}\cdot C_{out}}}\cdot D(z) \quad (8.60)$$

$$V_{out}(z)=\frac{\frac{V_{in}\cdot T_{sw}}{L_{out}\cdot C_{out}}\cdot(m+C_{out}\cdot R_{cout})\cdot\left(z+\frac{T_{sw}}{m+C_{out}\cdot R_{cout}}\cdot\left(\frac{R_{cout}}{R_{out}}-\frac{C_{out}\cdot R_{cout}}{T_{sw}}-\frac{R_{cout}\cdot m}{L_{out}}-\frac{m}{T_{sw}}+1\right)\right)}{z^2+z\cdot\left(\frac{T_{sw}}{R_{out}\cdot C_{out}}-2\right)+1-\frac{T_{sw}}{R_{out}\cdot C_{out}}+\frac{T_{sw}^2}{L_{out}\cdot C_{out}}}\cdot D(z) \quad (8.61)$$

In the final step, it should be considered that:

$$-\frac{m}{T_{sw}}=\frac{t_d-T_{sw}}{T_{sw}}=\frac{t_d}{T_{sw}}-1 \quad (8.62)$$

$$V_{out}(z)=\frac{\frac{V_{in}\cdot T_{sw}}{L_{out}\cdot C_{out}}\cdot(m+C_{out}\cdot R_{cout})\cdot\left(z+\frac{T_{sw}}{m+C_{out}\cdot R_{cout}}\cdot\left(\frac{R_{cout}}{R_{out}}-\frac{C_{out}\cdot R_{cout}}{T_{sw}}-\frac{R_{cout}\cdot m}{L_{out}}+\frac{t_d}{T_{sw}}\right)\right)}{z^2+z\cdot\left(\frac{T_{sw}}{R_{out}\cdot C_{out}}-2\right)+1-\frac{T_{sw}}{R_{out}\cdot C_{out}}+\frac{T_{sw}^2}{L_{out}\cdot C_{out}}}\cdot D(z) \quad (8.63)$$

8.2 Current Mode Control

8.2.1 Power Converter Small-signal Analisys

8.2.1.1 Continuous-time

Table A-2 shows the values for several power converters using the Ridley Model.

	Power Converter		
	Buck	**Boost**	**Buck-Boost**
K_f	$-D \cdot K_i \cdot [1-D/2]$	$-K_i/2$	$-D \cdot K_i \cdot [1-D/2]$
K_r	$K_i/2$	$[(1-D)^2 \cdot Ki]/2$	$[(1-D)^2 \cdot Ki]/2$
G_2	1 (for constant-frequency operation mode)		
He(s)	$1+(s/\omega_n \cdot Q_z)+(s^2/\omega^2_n \cdot Q_z)$ (quadratic approximation valid up to half f_{sw})		
	$s \cdot T_s/(e^{s \cdot Ts}-1)$ (exact sample-data to the whole range of f_{sw})		
Q_z	$-2/\pi$		
K_i	$R_i \cdot T_s/L$		
ω_n	π/T_s		
m_c	$1+(S_e/S_n)$		
$F_h(s)$	$1/[1+(s/\omega_n \cdot Q)+(s^2/\omega_n^2)]$		
Q	$1/[\pi \cdot (m_c \cdot (1-D)-0.5)]$		

Table A- 2. Value of the blocks in the Ridley model.

Thus, the duty-cycle signal for the power stage according to the Ridley's model and neglecting source and load disturbances is defined by:

$$\hat{d}(s) = F_m \cdot \left(\hat{i}_c(s) - H_1 \cdot H_e(s) \cdot \hat{i}_L(s) + K_f \cdot \hat{v}_{in}(s) + K_r \cdot \hat{v}_{out}(s) \right) \tag{8.64}$$

It is known that :

$$\hat{i}_L(s) = \left. \frac{\hat{i}_L(s)}{\hat{d}(s)} \right|_{\hat{io}=\hat{Vin}=0} \cdot \hat{d}(s) = G_{id(s)} \cdot \hat{d}(s) \tag{8.65}$$

$$\hat{v}_{out}(s) = \left. \frac{\hat{v}_{out}(s)}{\hat{d}(s)} \right|_{\hat{io}=\hat{Vin}=0} \cdot \hat{d}(s) = G_{od(s)} \cdot \hat{d}(s) \tag{8.66}$$

Introducing (9.66) and (9.67) in (9.65) and operating, it can be found:

$$\frac{\hat{v}_{out}(s)}{\hat{i}_c(s)} = \frac{F_m \cdot G_{od}(s)}{1 + F_m \cdot \left(H_{sens} \cdot H_e(s) \cdot G_{id}(s) - K_r \cdot G_{od}(s) \right)} \tag{8.67}$$

8.2.1.2 Discrete-time

Following these guidelines, the inductor current reference ($i_c[n]$) is the final goal to achieve:

$$\begin{aligned} & i_L[n+1]=i_c[n] \\ & \quad \downarrow Z \\ & z\cdot I_L(z)=I_c(z) \end{aligned} \tag{8.68}$$

And :

$$I_c(z)=z\cdot\frac{\left(z-\frac{1}{1+\frac{T_{sw}}{R_{out}\cdot C_{out}}}\right)\cdot\frac{T_{sw}\cdot V_{in}}{L_{out}}\cdot z}{z^2-z\cdot\left(1+\frac{R_{out}}{L_{out}}\cdot\left(\frac{L_{out}\cdot C_{out}-T_{sw}^2}{R_{out}\cdot C_{out}+T_{sw}}\right)\right)+\frac{R_{out}}{L_{out}}\cdot\left(\frac{L_{out}\cdot C_{out}-T_{sw}^2}{R_{out}\cdot C_{out}+T_{sw}}\right)+\frac{T_{sw}^2\cdot R_{out}}{L_{out}\cdot\left(R_{out}\cdot C_{out}+T_{sw}\right)}}\cdot D(z) \tag{8.69}$$

Then, the discrete-time control-to-output voltage can be calculated for DCMC as follows:

$$G_{oc}(z)=\frac{V_{out}\cdot D(z)}{I_c(z)} \tag{8.70}$$

Using (9-38) and (9-39) in (9-70), it can be obtained:

$$G_{oc}(z)=\frac{T_{sw}}{C_{out}}\cdot\frac{1}{\left(1+\frac{T_{sw}}{R_{out}\cdot C_{out}}\right)\cdot\left(z-\frac{1}{1+\frac{T_{sw}}{R_{out}\cdot C_{out}}}\right)} \tag{8.71}$$

8.2.2 Digital Control Laws

8.2.2.1 One-Cycle Valley-Current Predictive Control

As regards the Fig. A-3, the sampled-time inductor current along the switching period is formulated in (8.26):

$$i_L[n]=i_L[n-1]+d[n]\cdot T_{sw}\cdot\left(m_1-m_2\right)+m_2\cdot T_{sw} \tag{8.72}$$

Operating (8.30), the duty-cycle for next switching period is calculated as follows:

$$d[n+1]=\frac{V_{out}[n]+i_L[n+1]\cdot R_L[n+1]}{V_{in}[n]}+\frac{L_{out}}{V_{in}[n]\cdot T_{sw}}\cdot\left(i_L[n+1]-i_L[n]\right) \tag{8.73}$$

For an easy practical implementation, parasitic effects are neglected and $V_{out}[n]$ and $V_{in}[n]$ are considered constant for several switching periods obtaining:

$$d[n+1] = \frac{V_{out}}{V_{in}} + \frac{L_{out}}{V_{in} \cdot T_{sw}} \cdot \left(i_L[n+1] - i_L[n] \right) \tag{8.74}$$

Taking the inductor current for next switching period as the goal reference (i.e. the current reference imposed by the external voltage loop) and considering the output-input voltage ratio as the duty-cycle (this is only true for the Buck converter topology), one-cycle valley-inductor predictive current is formulated as follows:

$$d[n+1] = d[n] + \underbrace{\frac{L_{out}}{V_{in} \cdot T_{sw}}}_{k_i} \cdot \left(\underbrace{i_c[n] - i_L[n]}_{e_i} \right) \tag{8.75}$$

8.2.2.2 One-Cycle Peak-Current Predictive Control

In this case, the inductor current reference is calculated in a similar way than in the previous one:

$$i_L[n+1] = i_L[n] + m_2 \cdot T_{sw} \cdot \left(1 - d[n]\right) + m_1 \cdot d[n+1] \cdot T_{sw} \tag{8.76}$$

It can be obtained introducing (8.28) in (8.76):

$$i_L[n+1] = i_L[n] - \frac{V_{out}}{L_{out}} \cdot T_{sw} \cdot \left(1 - d[n]\right) + \frac{V_{in} - V_{out}}{L_{out}} \cdot d[n+1] \cdot T_{sw} \tag{8.77}$$

Hence, the duty-cycle for next switching period is:

$$d[n+1] = \underbrace{\frac{L_{out}}{\left(V_{in} - V_{out}\right) \cdot T_{sw}}}_{k_i} \cdot \left(\underbrace{i_L[n+1] - i_L[n]}_{E_i} \right) + \frac{V_{out}}{V_{in} - V_{out}} \cdot \left(1 - d[n]\right) \tag{8.78}$$

8.3 Continuous-time Current-Sharing schemas.

This simulation models allows us to compare several CS techniques used in VRs and which have been simulated in a 4-phased interleaved DC/DC converter owning the values exposed in the point 3.8.3 and which is shown in Fig. A-4.

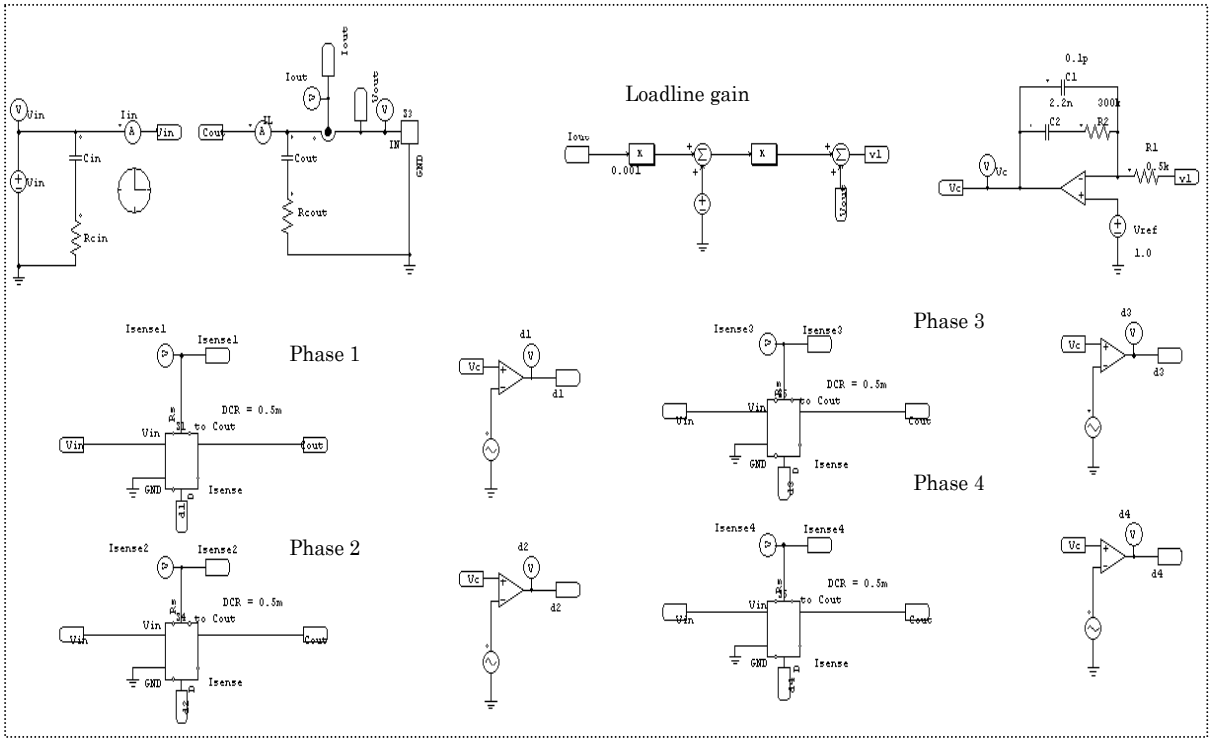

Fig. A- 4 4-phased DC/DC converter with VMC

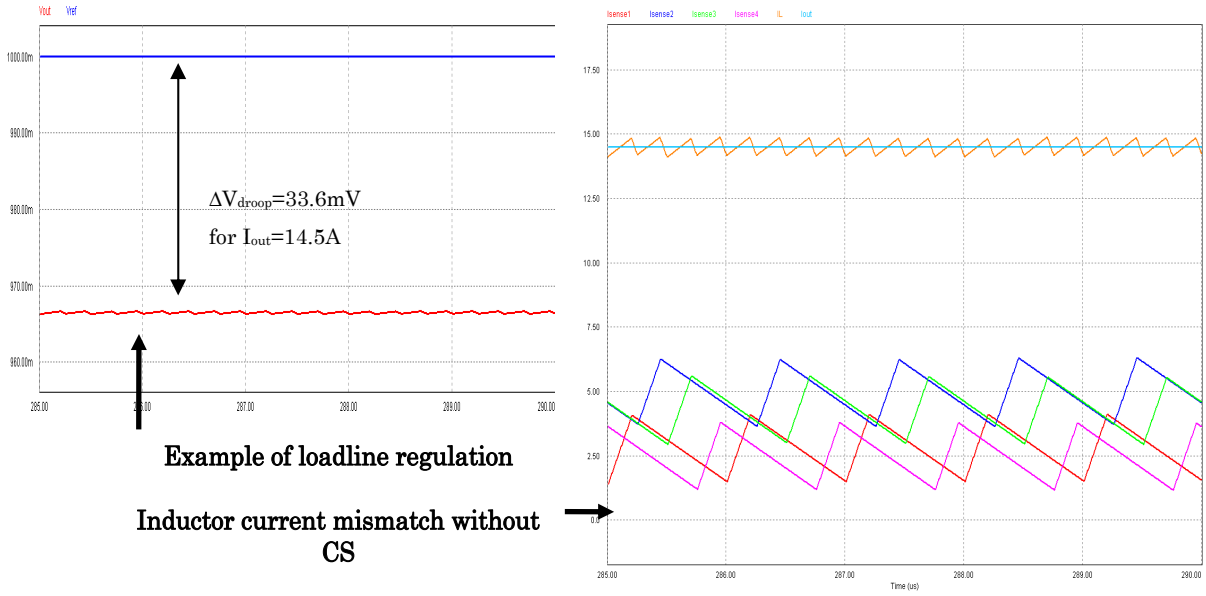

Fig. A- 5 Output voltage (left) and inductor currents (right)

Fig. A-5 illustrates like small variations in the phase impedance causes severe

mismatches in the inductor currents, thus, CS regulation loop is required.

8.3.1 DCS+VMC

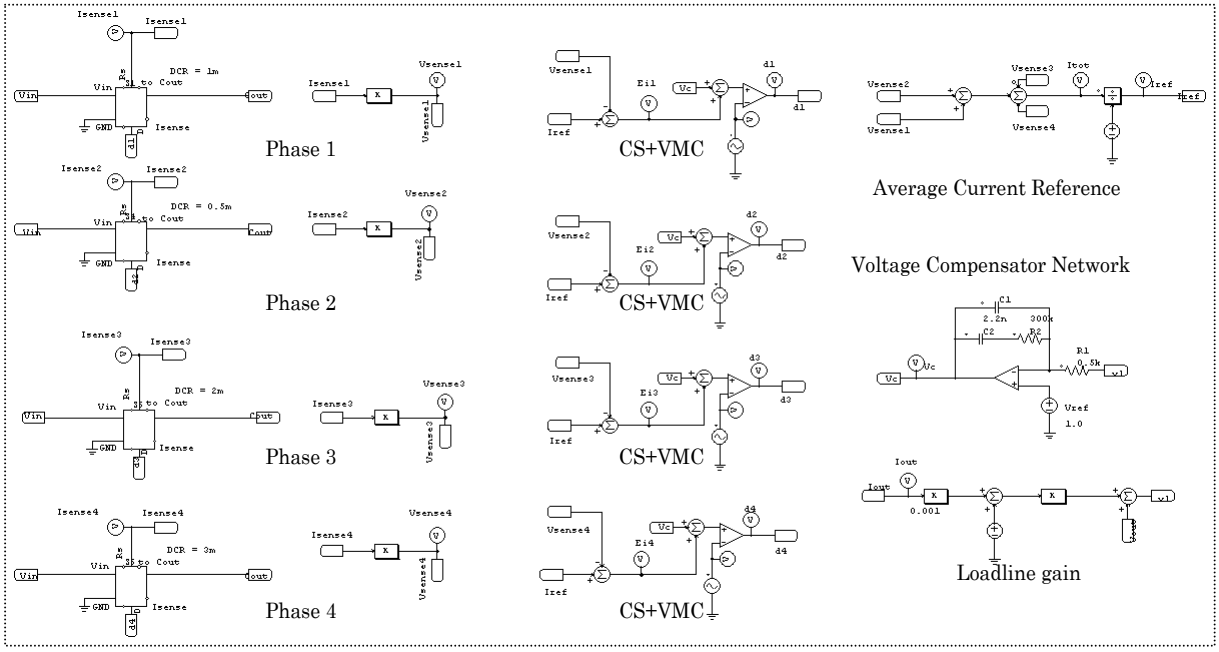

Fig. A- 6 4-phased DC/DC converter with Democratic Current Sharing and Voltage-Mode Control

8.3.2 DCS+CMC

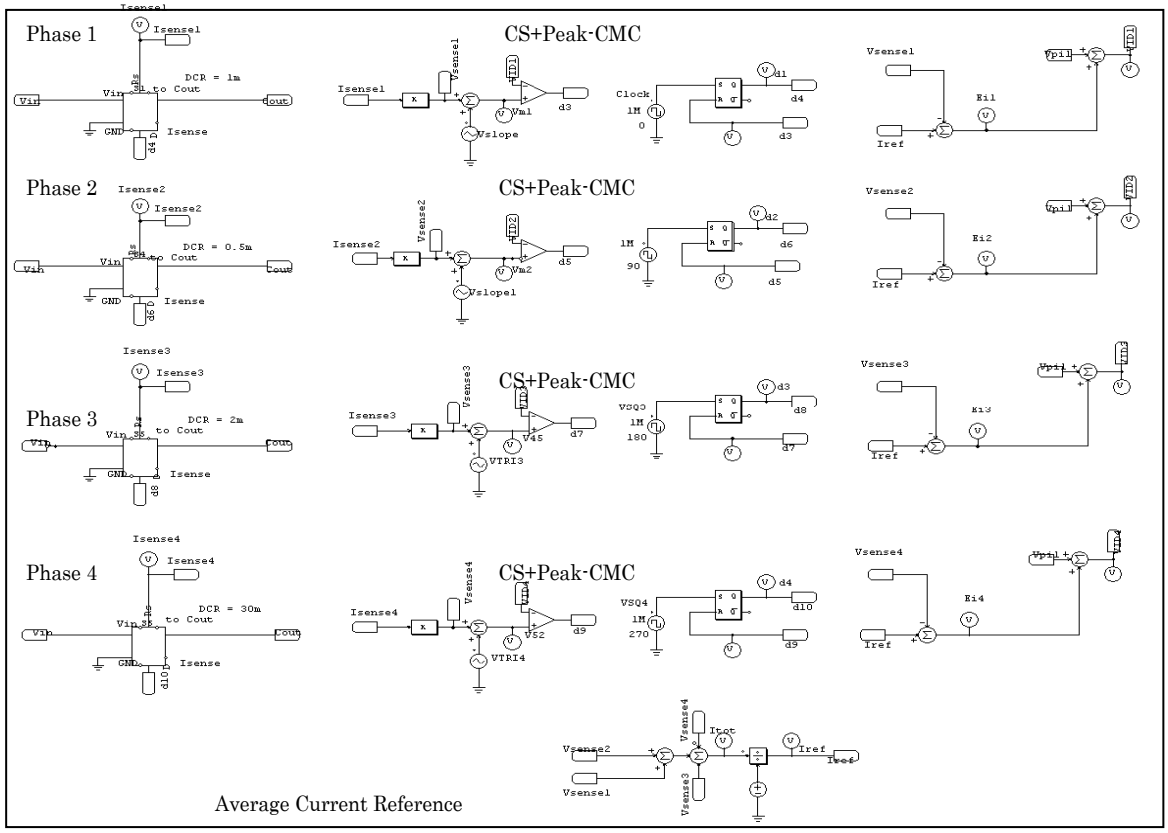

Fig. A- 7 4-phased DC/DC converter with Democratic Current Sharing and Peak-Current-Mode Control

8.3.3 Dedicated MS-CS+VMC

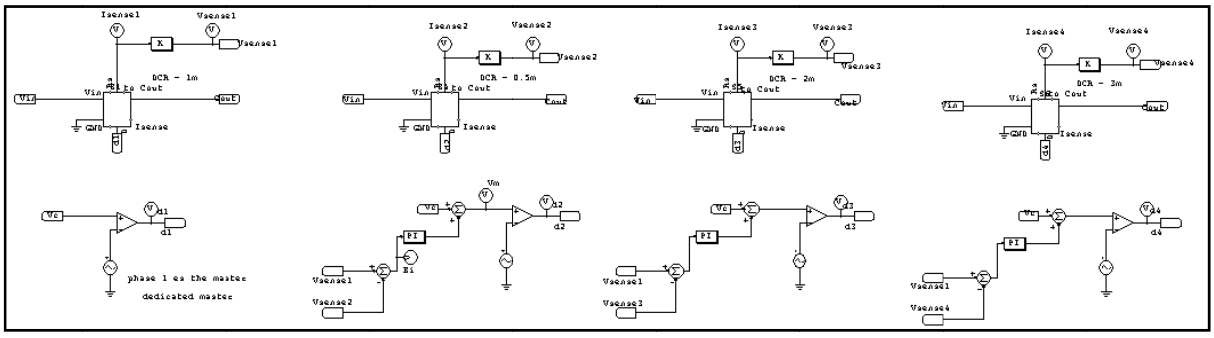

Fig. A- 8 4-phased DC/DC converter with Dedicated Master-Slave Current Sharing and Voltage-Mode Control

8.3.4 Dedicated MS-CS+CMC

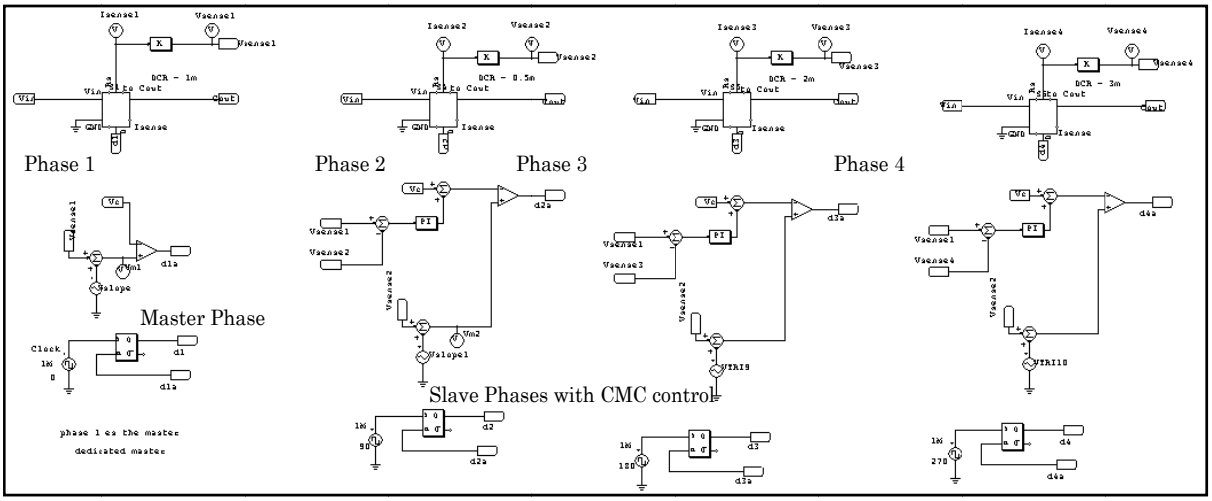

Fig. A- 9 4-phased DC/DC converter with Dedicated Master-Slave Current Sharing and Current-Mode Control

8.3.5 Automatic MS-CS+VMC

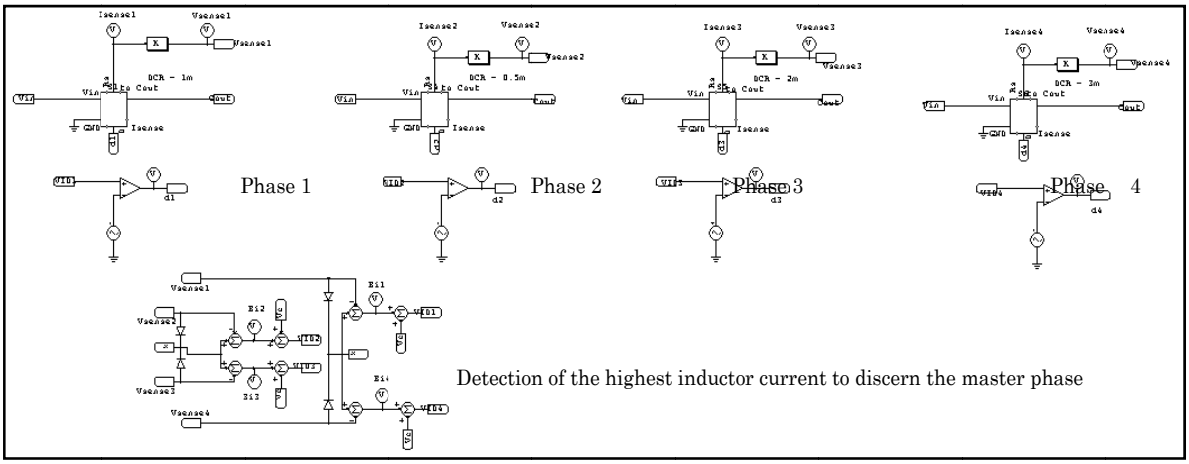

Fig. A- 10 4-phased DC/DC converter with Automatic Master-Slave Current Sharing and Voltage-Mode Control

8.3.6 Automatic MS-CS+CMC

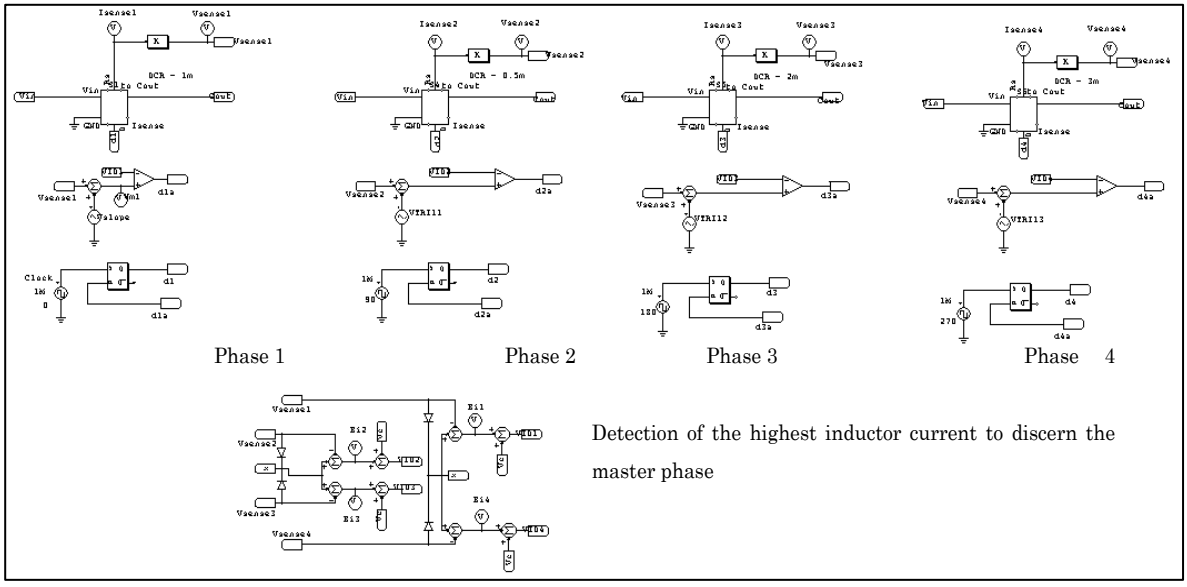

Fig. A- 11 4-phased DC/DC converter with Automatic Master-Slave Current Sharing and Current-Mode Control

8.3.7 Interleaved Peak-Current-Mode CS

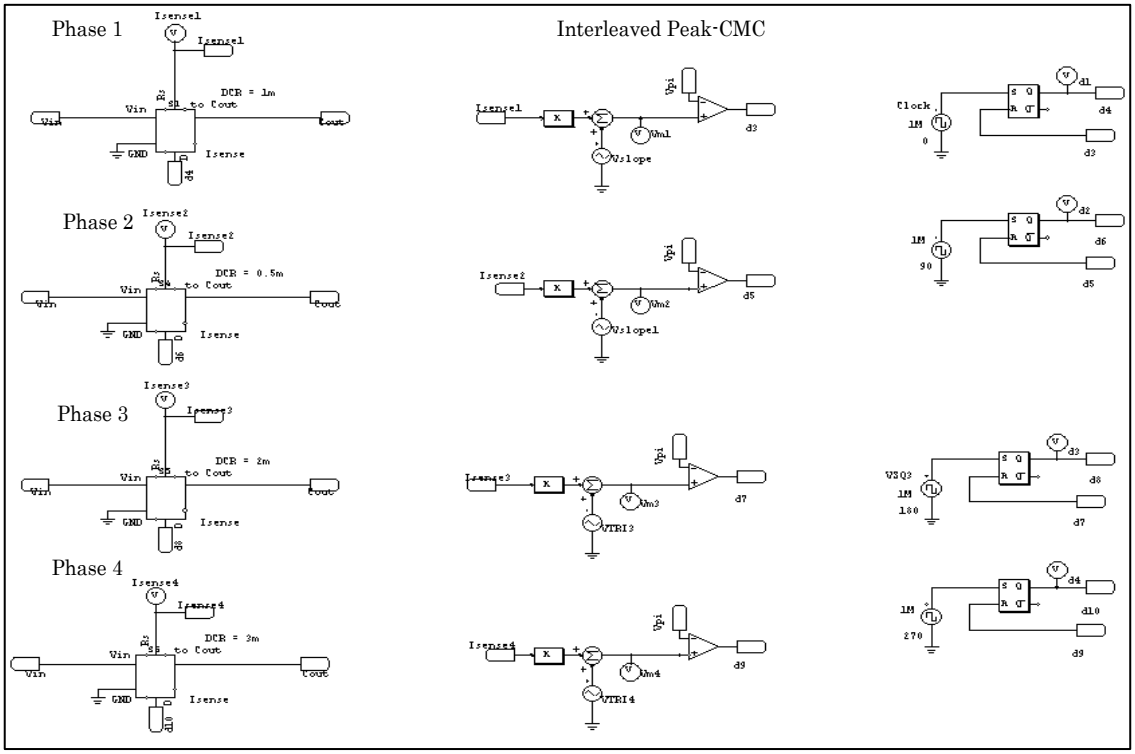

Fig. A- 12 4-phased DC/DC converter with Interleaved Peak-Current-Mode Control

8.3.8 Results for the 4-phased DC/DC converter

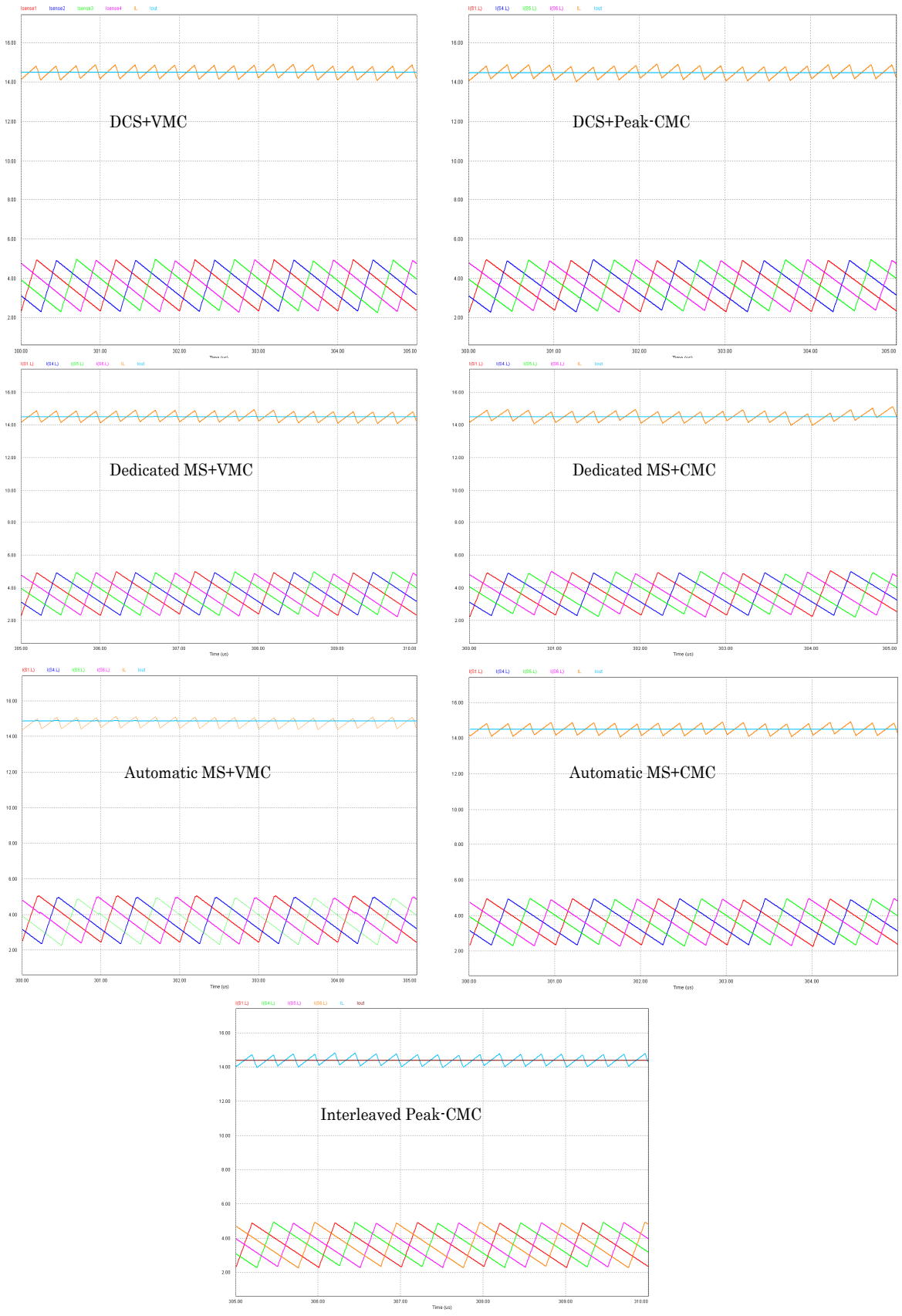

Fig. A- 13 Simulations of a 4-phased DC/DC converter with some Current-Sharing techniques