Design of CMOS analog integrated circuits as readout electronics for high-T_C superconductor and semiconductor terahertz bolometric sensors

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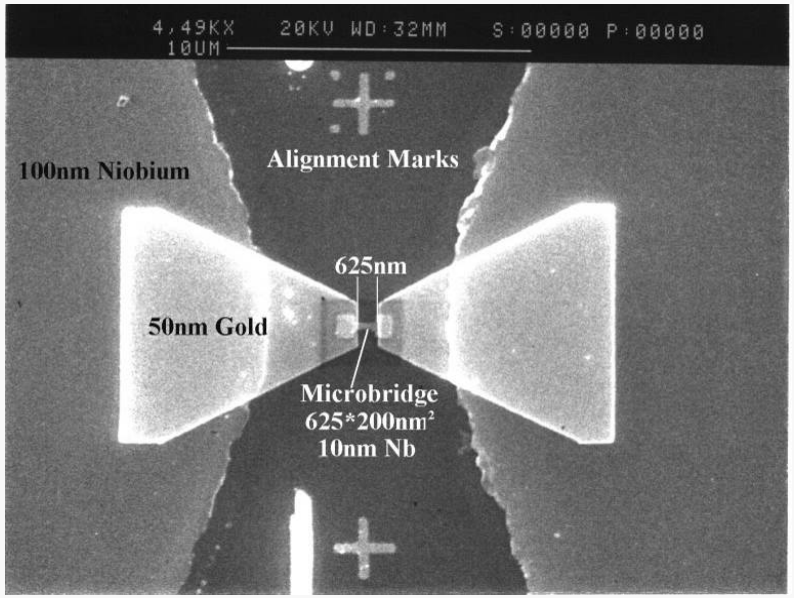
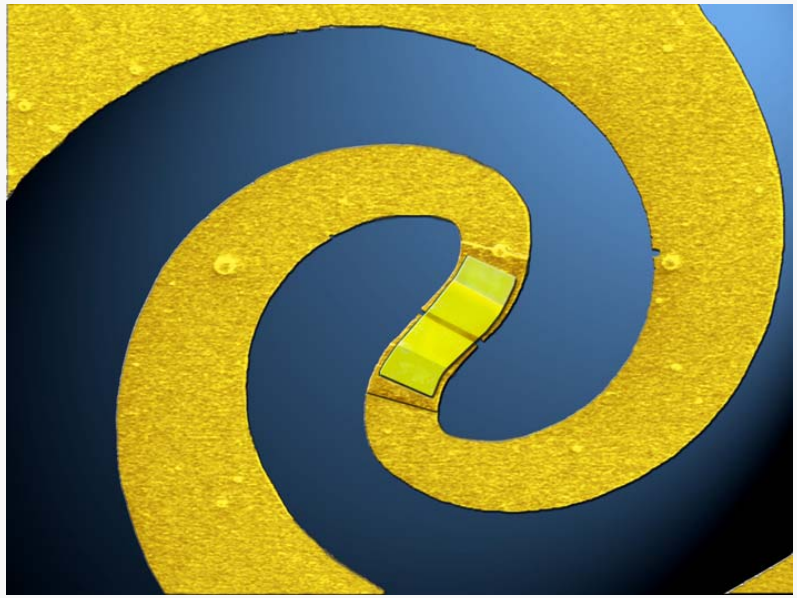
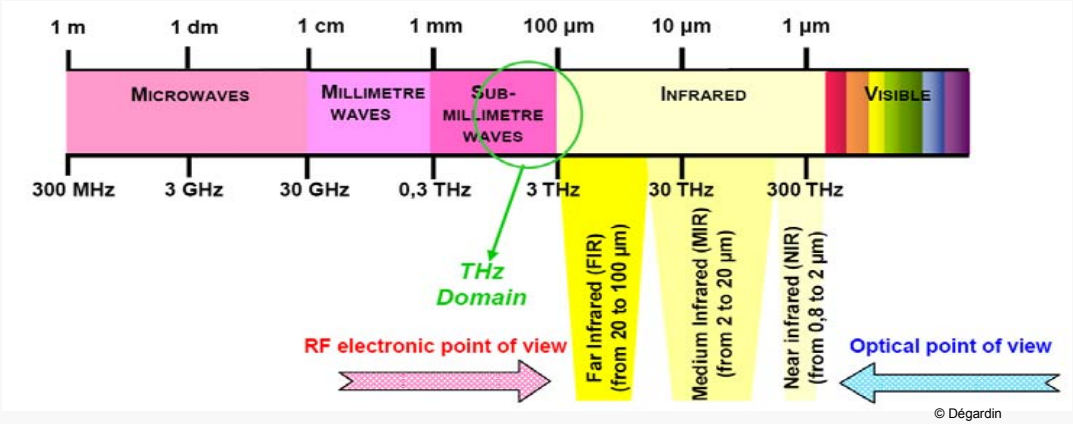
I.
Introduction





THz detection and terahertz imaging



Civil application:

High voltage insulator under discharge

[ulis-ir website]

Other fields of applications:

Spectroscopy

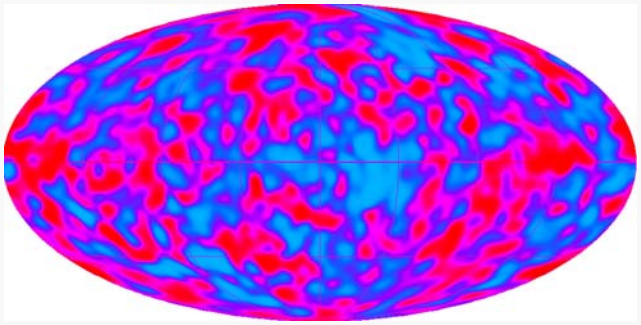
Civil security, medical

Military application etc…

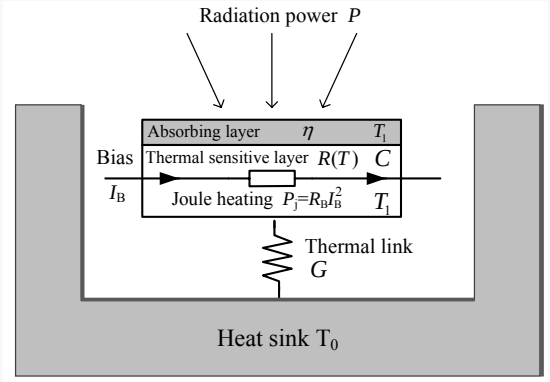
Research application

Cosmic Microwave background exploring

(Nobel price in physic 2006)

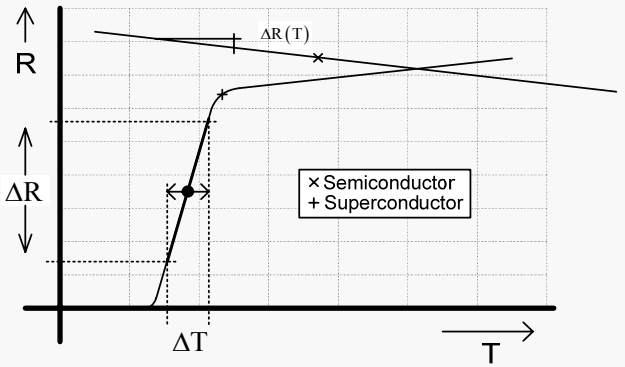


(THz) Bolometric detectors



Bolometric sensor composition

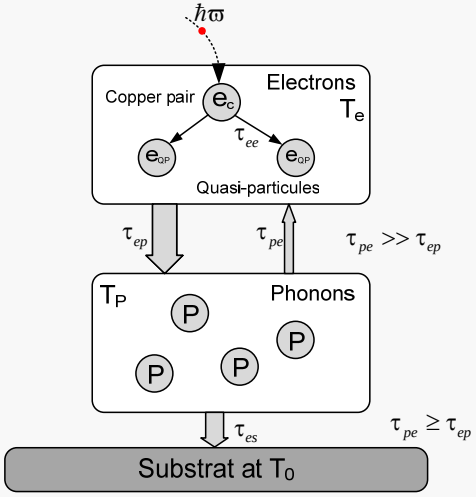
R(T)



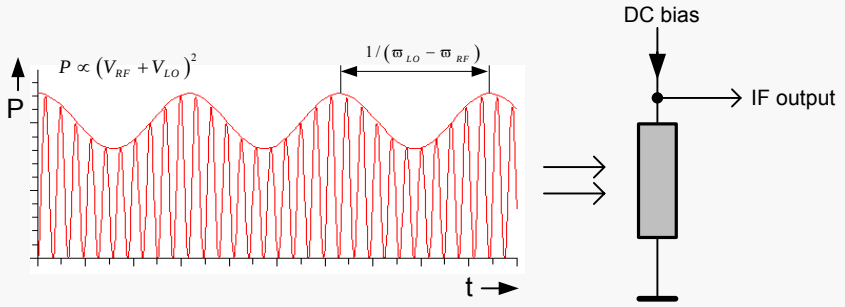
R(T) of superconductor and semiconductor

[subject of M. Aurino et M. Longhin PhD thesis]

Heterodyne detection:

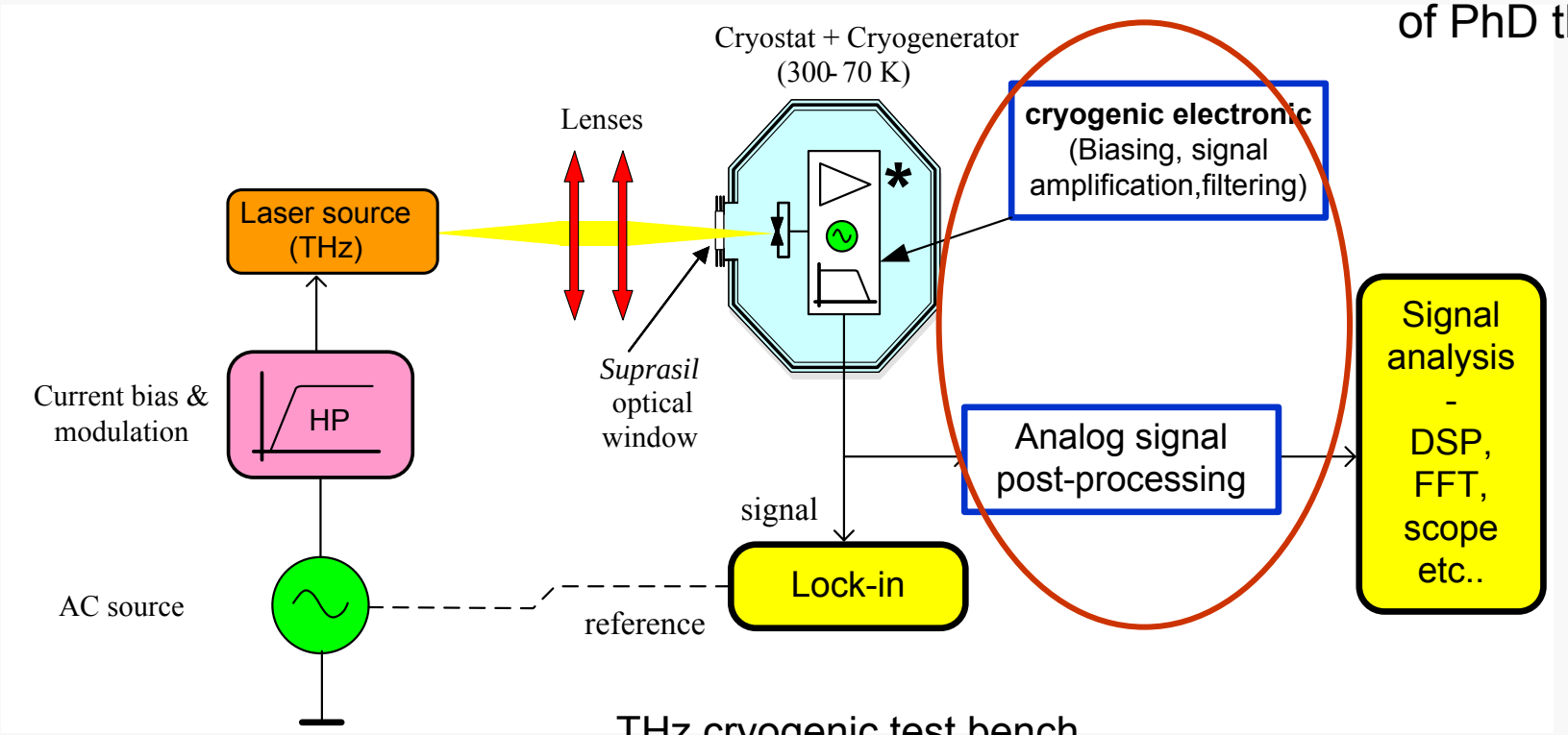


Superconducting Hot Electron Bolometer (HEB)



Characterization of new generation THz detectors: A CRUCIAL ROLE OF ELECTRONICS

blocks developed in the frame of PhD thesis



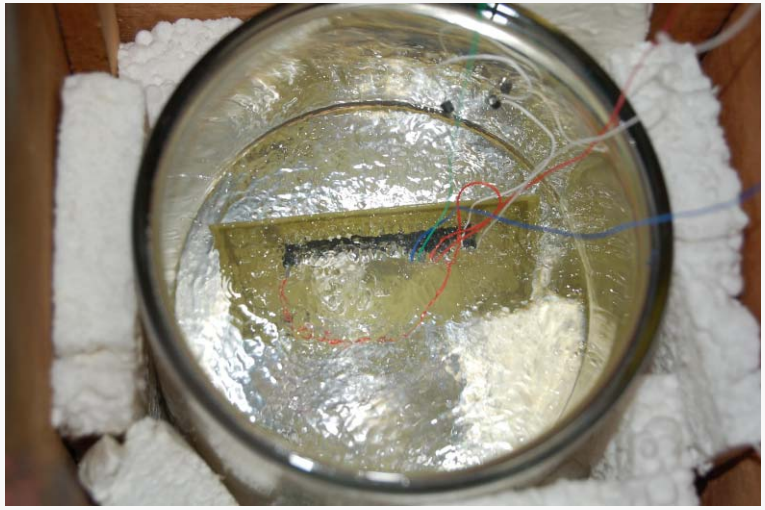
THz cryogenic test bench

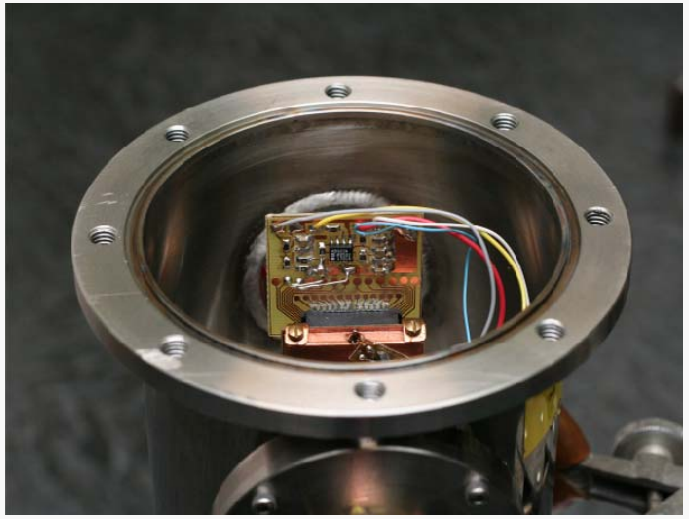
do the electronics follow up?

Research objectives of PhD thesis

- Cryogenic integrated analog electronic for THz detection chain
- New structures of fixed-gain CMOS differential amplifiers compatible with bolometric detectors at room and cryogenic temperatures
- High dynamic range signal processing: Developpement of frequency filters with high attenuation rate

II.
Differential amplifier for cryogenic instrumentation



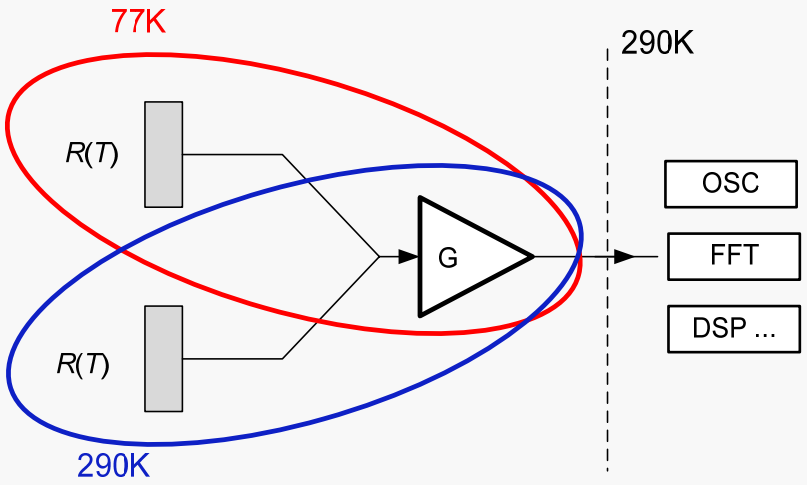


SPECIFICATIONS

Wide temperature range CMOS differential amplifiers for:

i) Room temperature (semiconductor bolometers)

ii) Cryogenic temperatures (superconducting bolometers – high T_C)

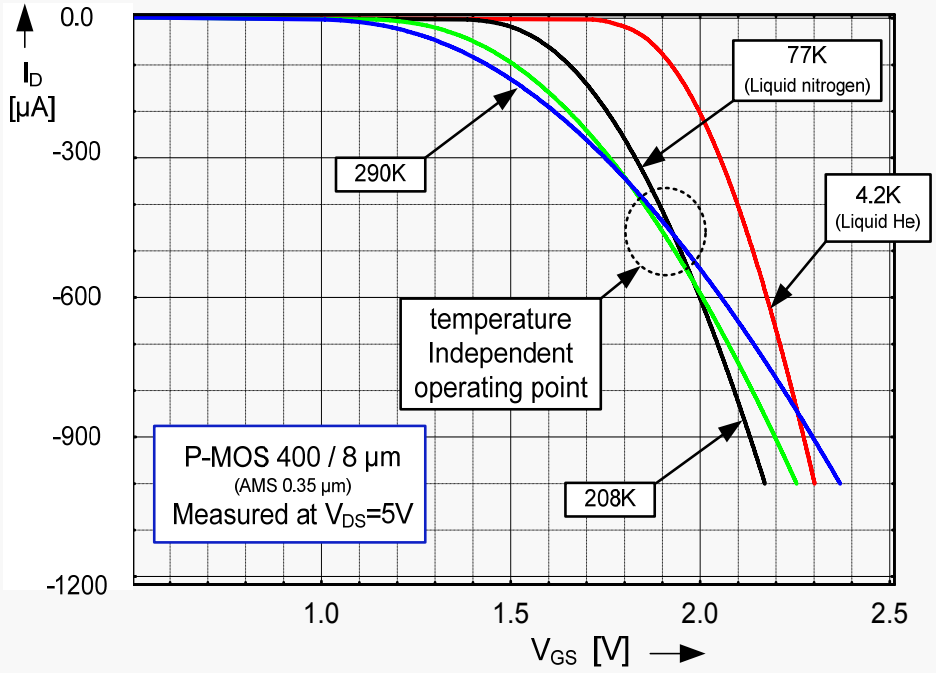


Low noise Differential CMOS amplifier

Requirements:

- 40dB, accurate gain,
- 70K to 300K temperature range,
- Differential gain BW: DC to several MHz,
- Low noise operation,
- Low power consumption
- High (> 100kΩ) input impedance,
- Simple architecture.

MOS cryogenic modeling



Measured I-V characteristics for a PMOS 400/8µm

[measurements provided in CEA-INAC laboratory in Grenoble]

➔ Low field surface mobility:

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-x}$$

➔ Threshold voltage:

$$V_{TH}(T) = V_{TH}(T_0)\left[1 + \alpha_{THX}\cdot(T - T_0)\right]$$

➔ analytical temperature model

$$I_D = \frac{KP}{2}\left(\frac{T}{T_0}\right)^{-x}\frac{W}{L}\cdot\left[V_{GS} - V_{TH}(T_0)\left[1 + \alpha_{THX}(T - T_0)\right]\right]^2$$

➔ **Other effect:** Kink effect, mobility degradation
electron freeze-out

Least Square empirical model

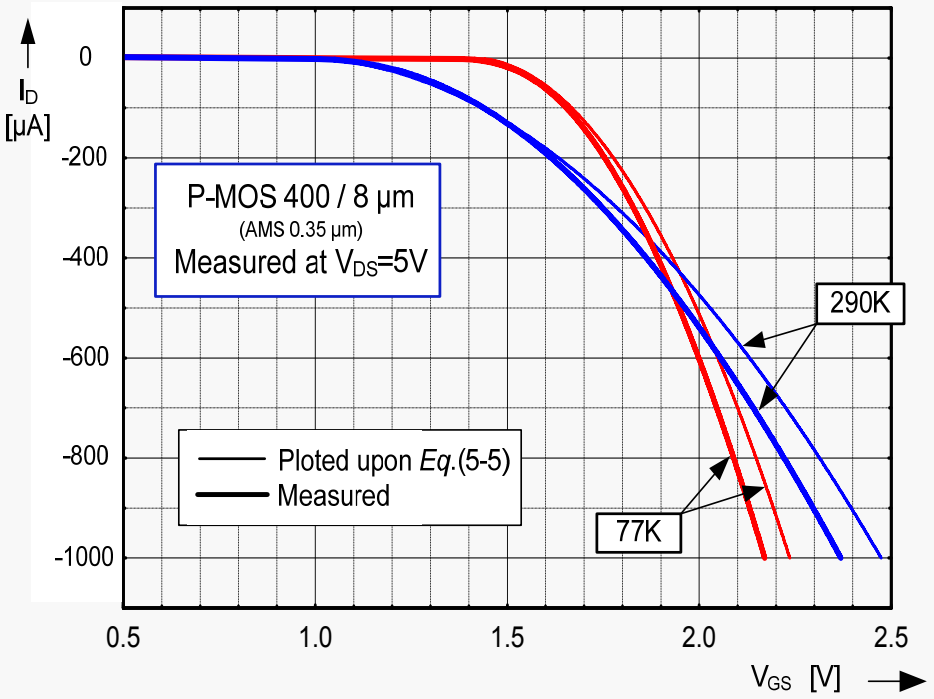
➔ LM fit of $y_i = b\cdot(x_i - a)^2$:

$$R^2 \equiv \sum_{i=0}^{n}\left[y_i - f\left(x_{1,i}, x_{2,i}...x_{m,i}, a_1, a_2...a_m\right)\right]^2 \rightarrow \min \Rightarrow \frac{\partial R^2}{a_{1,2,..m}} = 0$$

Parameters based on LM fit (measurements and simulation SPICE-level 7)

TRANSISTOR	**Simulation 296K**	**Measured 296K**	**Measured 77K**
P-MOS 100/10µm			
KP [A/V²]	20.67×10^{-6}	21.63×10^{-6}	72.43×10^{-6}
V_{TH}[V]	-0.9649V	-0.9534V	-1.40493V

	x	A_{THX}	V_{TH} shift
PMOS 100µm/10µm	0.90	$-2.163\ mK^{-1}$	-2.06 mV/K

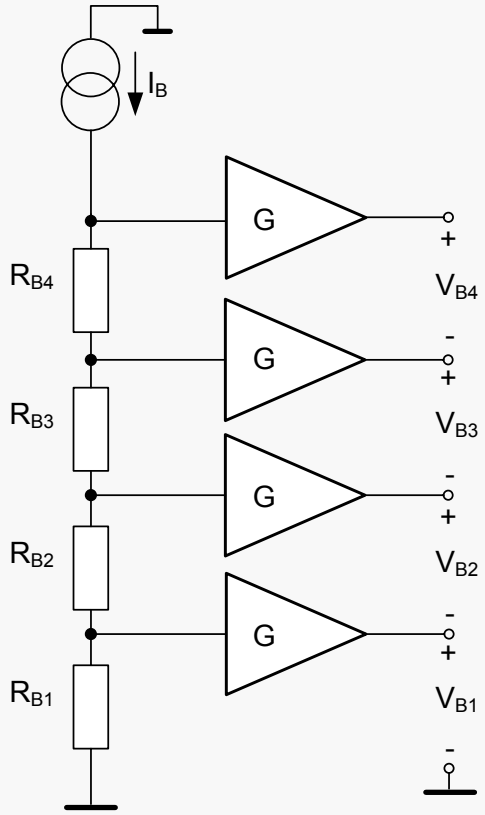


Verification of model: different run

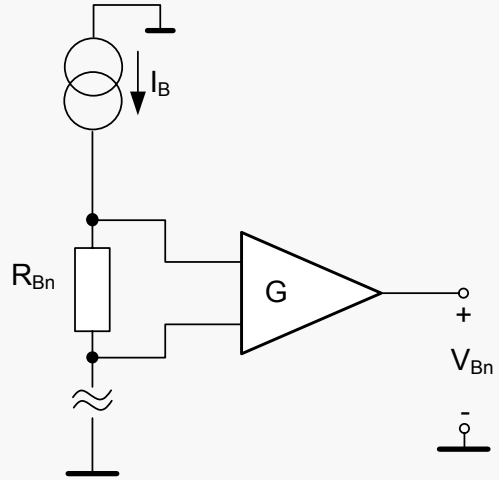
➔ analytical temperature model

$$I_D = \frac{KP}{2}\left(\frac{T}{T_0}\right)^{-x}\frac{W}{L}\cdot\left[V_{GS} - V_{TH}(T_0)\left[1+\alpha_{THX}\left(T-T_0\right)\right]\right]^2$$

DC BIAS, CONFIGURATION



Single ended amplifiers [*]

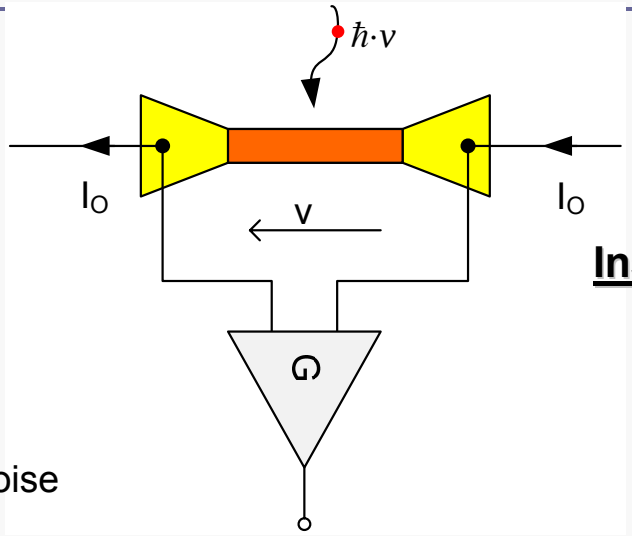


differential read-out amplifier in CMOS

adopted solution

[*] *PhD thesis: F. Voisin, 2005, D. Prêle, 2006, L2E UPMC-P6*

Differential amplifiers

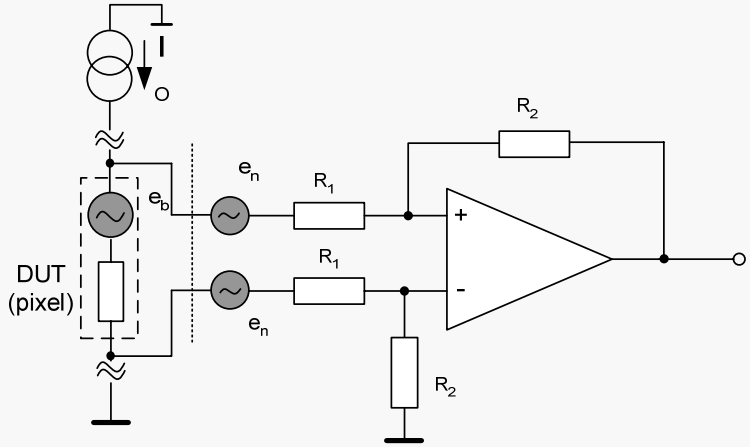


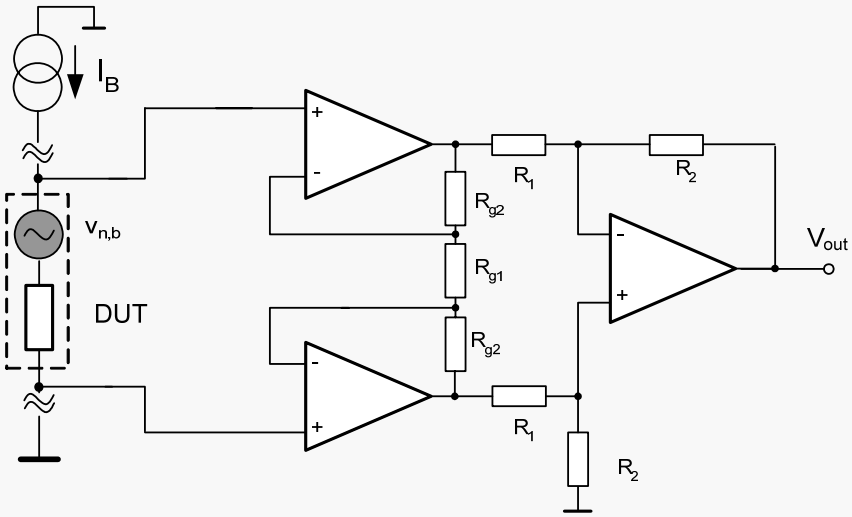
Differential OA

- Low input impedance
- High accuracy
- Higher input referred noise

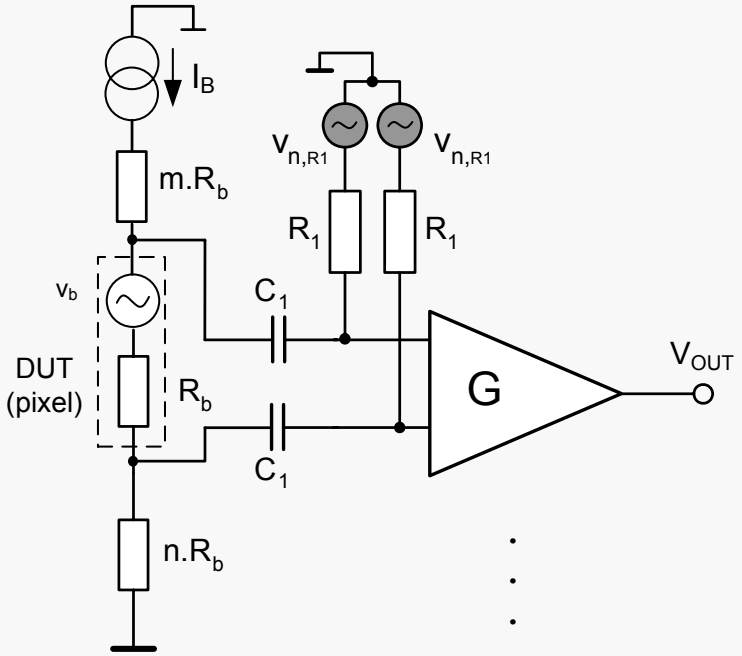
Instrumentation amplifier

- High input impedance
- Very high accuracy
- Higher input referred noise
- Low bandwidth





Solution: feedback-free amplifier



$$v_{n,in} \cong \sqrt{\frac{8k_BT}{R_1}} \cdot \left(\frac{2 + j\omega R_b C_1}{2\, j\omega C_1} \right) \quad *$$

* Bolometer noise voltage is neglected

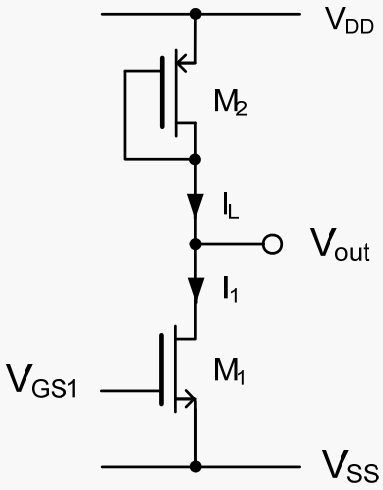
☺ **No resistors in the structure**
➔ simplification, reduced noise, and Iq, silicon surface save

☺ **Absence of compensation**
➔ improves time characteristics (no stability problems) and allows to reach higher BW

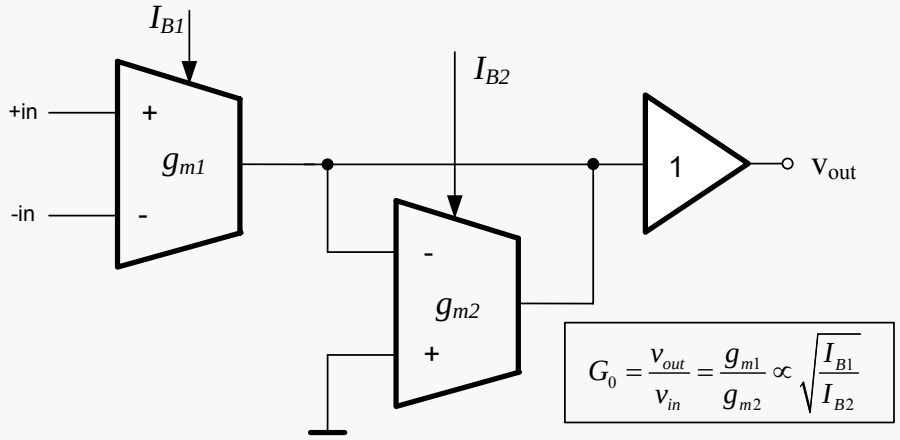
☹ **Linearity, distortion**

☹ **Missing experiences and developed architectures in bipolar and CMOS**

Known structures – low gain



Common source MOS amplifier



OTA Amplifier differential fixed-gain amplifier

The expression of the gain follows a square-root law:

$$G_0 = \frac{dV_{OUT}}{dV_{GS1}} = -\sqrt{\frac{KP_N}{KP_P}}\sqrt{\frac{W_1/L_1}{W_2/L_2}}$$

For 40 dB, the $(W/L)_1/(W/L)_2$ as high as $10\,000 \cdot KP_P/KP_N$

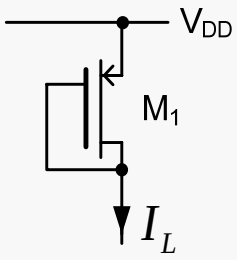
Adopted technique: low g_m load

Voltage gain fixed in the structure by the transconductance ratio

Voltage output is created by the voltage buffer

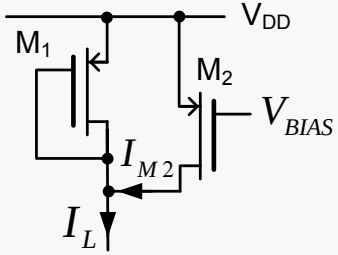
Active loads

MOS diode



$$g_m = \sqrt{2KP\frac{W}{L}I_L}$$

Decreasing the transconductance by current sink *[PhD F. Voisin, 2005]*

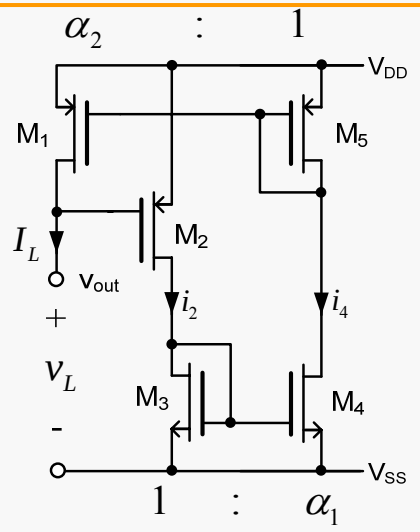


$$g_m' = \sqrt{2KP\cdot\frac{W_1}{L_1}\left(I_L - I_{M2}\right)}$$

Current difference makes the function very sensitive:

$$S_k^{g_m'} = \frac{\partial g_{m(k)}'}{\partial k}\cdot\frac{k}{g_{m(k)}'} = -\frac{1}{2}\frac{k}{1-k}$$

Proposed low g_m composite transistor



Proposed method* for decreasing the transconductance by means of *current scaling:

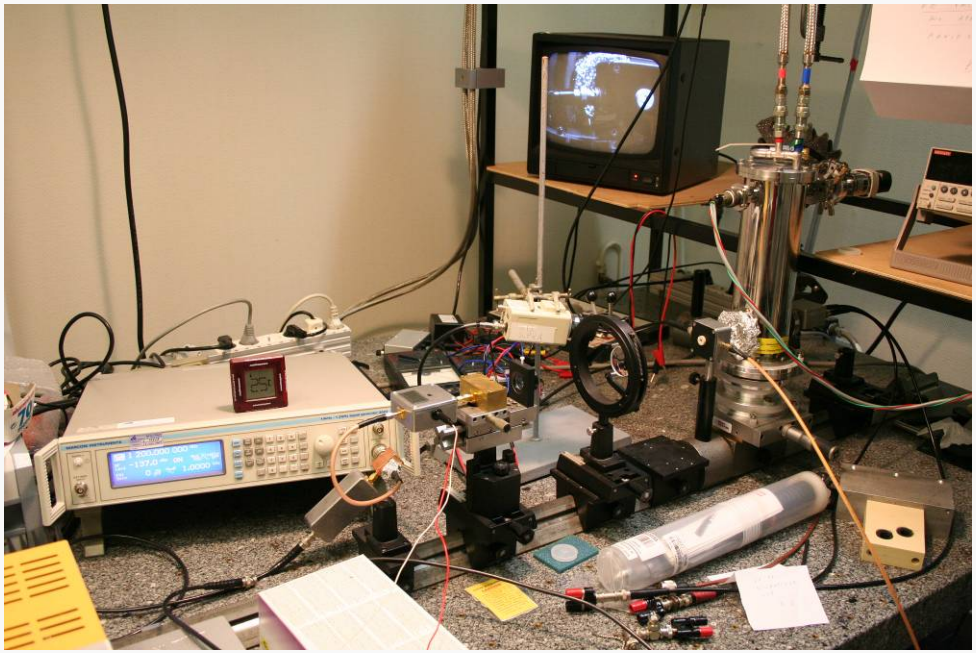
$$g_m' = \sqrt{2 \cdot KP_{(T_2)} \cdot \frac{W_2}{L_2} \cdot \left(\frac{\frac{W_4}{L_4} \cdot \frac{W_1}{L_1}}{\frac{W_3}{L_3} \cdot \frac{W_5}{L_5}} \right) \cdot I_L}$$

Inaccurate

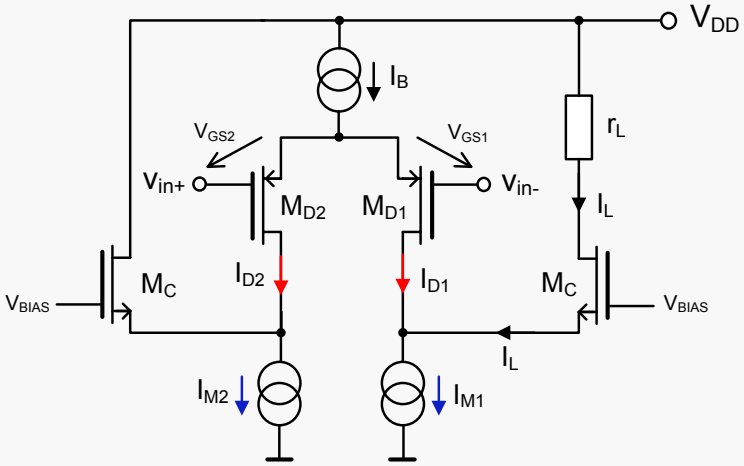
accurate

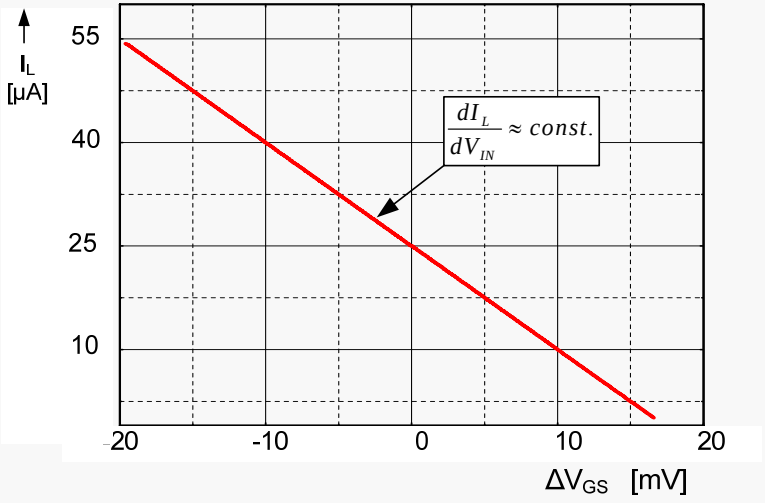
$$g_m' = \frac{i_L}{v_L} = g_{m2} \cdot \frac{g_{m4} \cdot g_{m1}}{g_{m3} \cdot g_{m5}} = \alpha_1 \cdot \alpha_2 \cdot g_{m2}$$

II.1
1st folded cascode amplifier



Folded cascode OTA: analysis



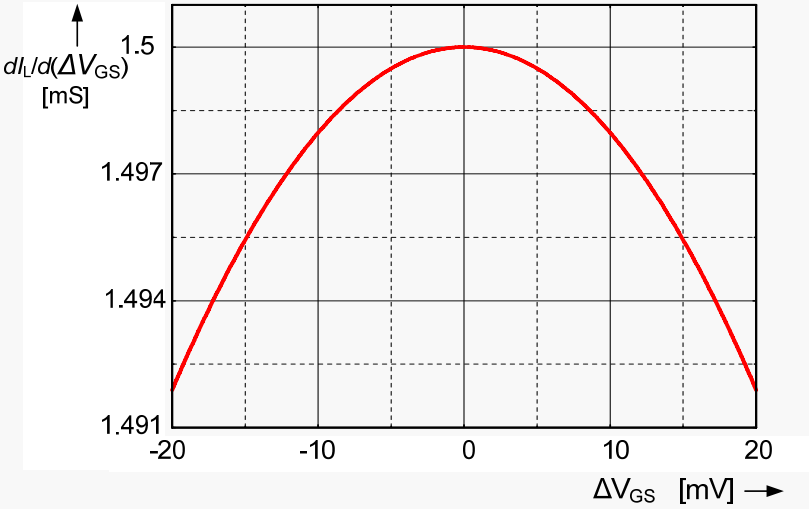


➔ **DC characteristic:**

$$I_{D1} = \frac{1}{8} \cdot \left(\sqrt{4 \cdot I_B - KP \cdot \frac{W_D}{L_D} \cdot \Delta V_{GS}^2} + \sqrt{KP \cdot \frac{W_D}{L_D}} \cdot \Delta V_{GS} \right)^2$$

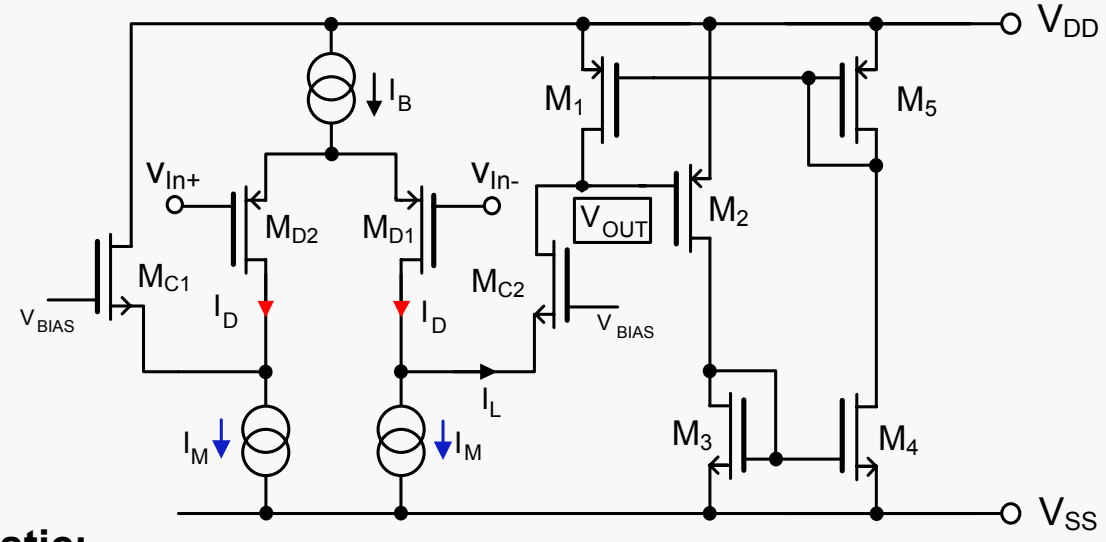
➔ **g_m:**

$$g_{mDiff} = \left. \frac{dI_{D1}}{d\Delta V_{GS}} \right|_{\Delta V_{GS}=0} = \frac{1}{2} \cdot \sqrt{KP_P \cdot \frac{W_D}{L_D} \cdot I_B}$$



For required input voltage range, the stage behaves as quasi-linear current source

Proposed 1st folded cascode amplifier



- **DC transfer characteristic:**

$$V_{OUT} = V_{DD} - |V_{TH,P}| - \sqrt{\frac{2}{KP_P \cdot \left(\frac{W_2}{L_2}\right)} \cdot \left(\frac{\frac{W_3}{L_3} \cdot \frac{W_5}{L_5}}{\frac{W_4}{L_4} \cdot \frac{W_1}{L_1}}\right) \cdot \left[I_{M1} - \frac{1}{8} \cdot \left(\sqrt{4 \cdot I_B - KP_P \cdot \frac{W_D}{L_D} \cdot \Delta V_{GS}^2} + \sqrt{KP_P \cdot \frac{W_D}{L_D}} \cdot \Delta V_{GS} \right)^2 \right]}$$

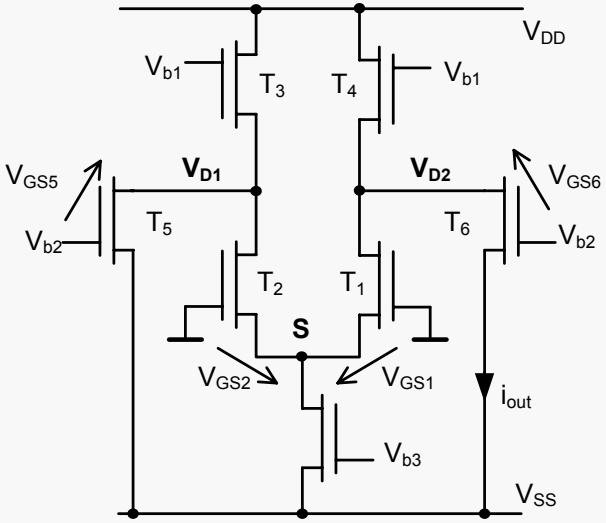
- **Gain is the slope of DC transfer characteristic:**

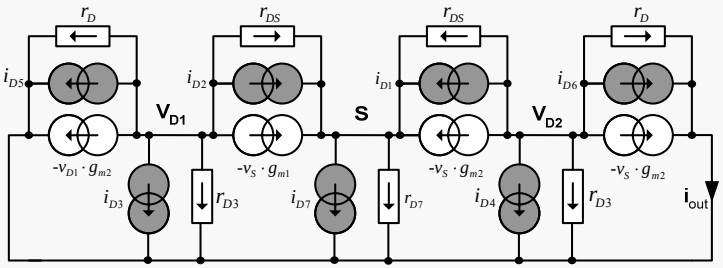
$$G_0 = \left. \frac{dV_{out}}{d\Delta V_{GS}} \right|_{\Delta V_{GS}=0} = \frac{1}{2} \sqrt{\frac{L_{eff}}{W_{eff}} \cdot \frac{W_D}{L_D}} \cdot \sqrt{\frac{I_B}{2 \cdot I_{L(\Delta V_{GS}=0)}}},$$

where:

$$\frac{W_{eff}}{L_{eff}} = \frac{\frac{W_2}{L_2} \cdot \frac{W_4}{L_4} \cdot \frac{W_1}{L_1}}{\frac{W_3}{L_3} \cdot \frac{W_5}{L_5}}$$

Noise analysis of folded cascode





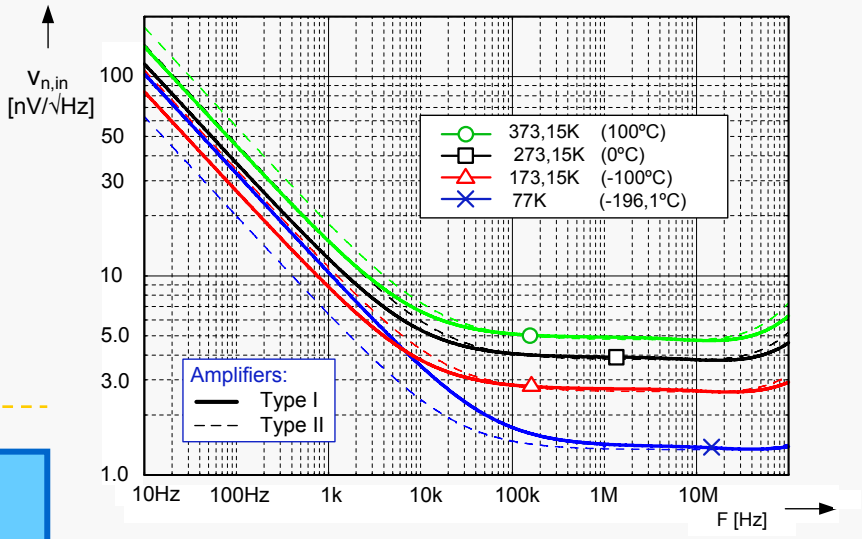
Small signal equivalent circuit.

The equivalent input noise*:*

$$\overline{e}_{in}^2 = \frac{\overline{e}_{OUT}^2}{G^2} = \frac{8}{3} k_B T \left(\frac{1}{2} \cdot \frac{1}{g_{mdiff}} + \frac{1}{4} \cdot \frac{g_{m7}}{g_{mdiff}^2} + \frac{g_{m4}}{g_{mdiff}^2} \right)$$

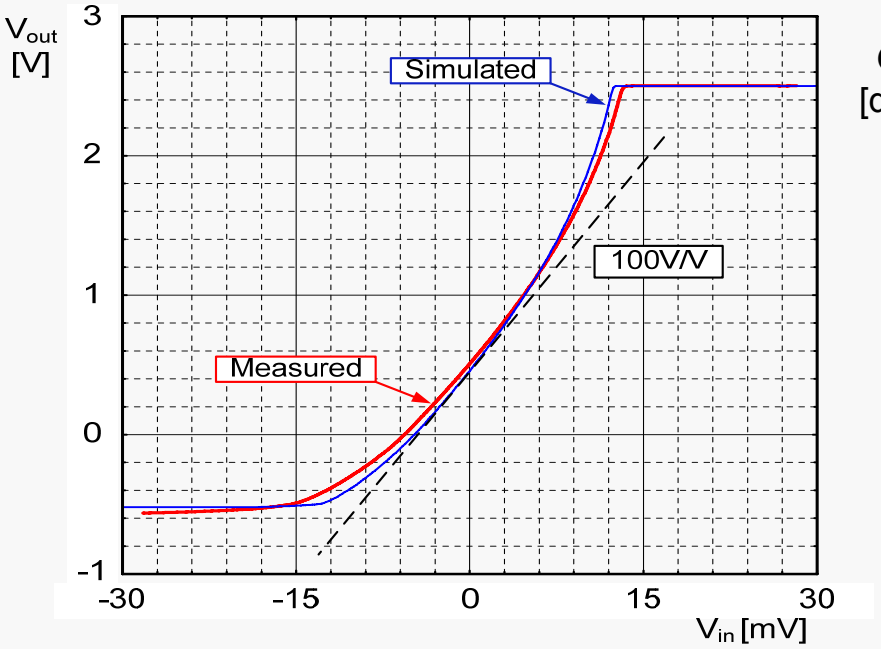
A very low thermal noise is observed at cryogenic temperature (T = 77 K):

$$v_{n,in} = 1.5\ nV/\sqrt{Hz}.$$

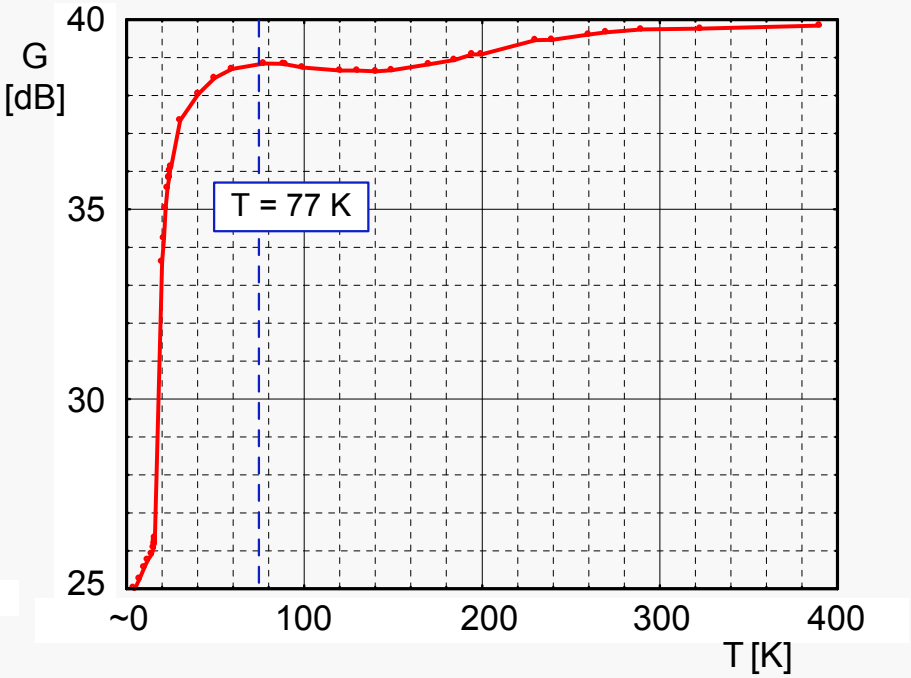


Simulated input-referred noise voltage (both amplifiers)

Measurements: wide temperature results



DC transfer characteristic at 290K

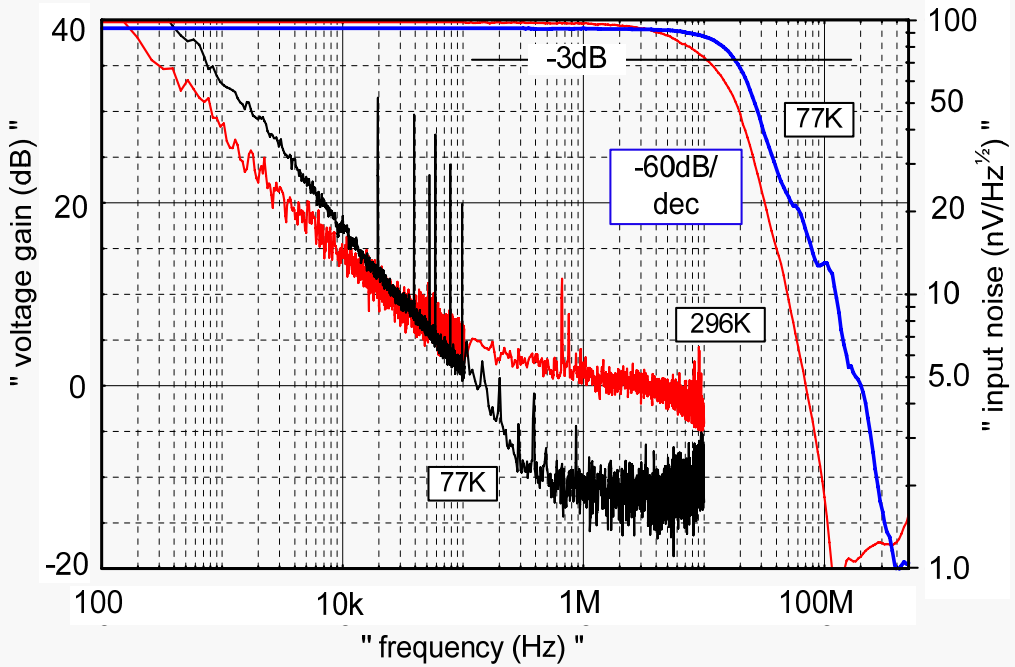


Temperature function of voltage gain

Results DC and AC characteristics

Amplifier	Gain [dB]
A_5	**39.84**
A_{5_2}	39.75
A_1	40.10
A_2	39.62
A_3	39.52
A_4	39.85
AVG	39.78

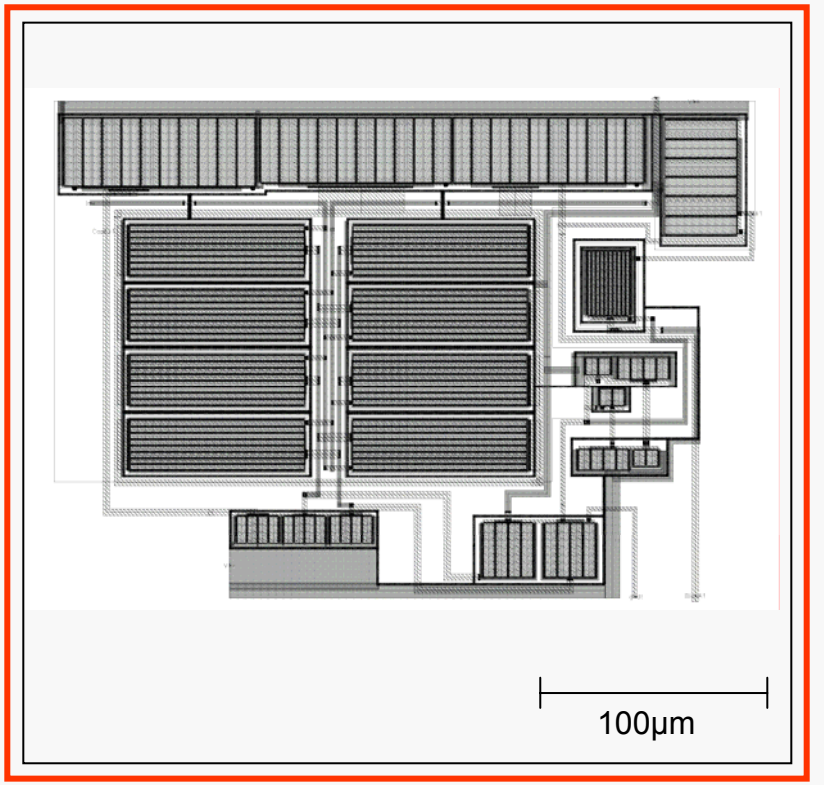
Dispersion *of voltage gain*
(A5_2 refers to chip 2)



AC response and input noise (V_{DD}=5V, I_Q=2mA)

1st amplifier: summary

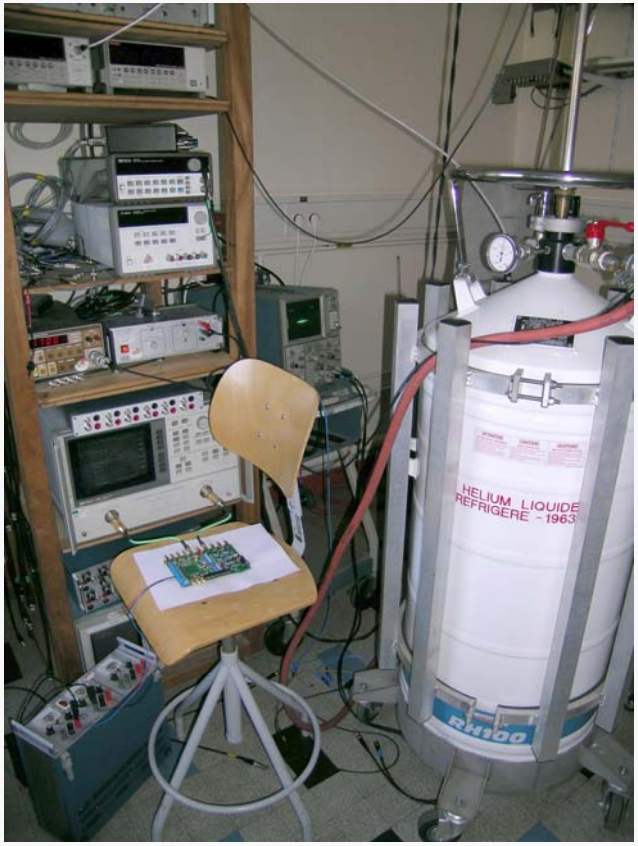
- New amplifier architecture **for extreme temperature range**
- State-of-the art: **low noise and large BW operation (up to 1.7GHz GBW at Iq = 2.1mA**
- **Gain is fixed by means of geometric ratio:** no variation with temperature
- Sufficient linearity **for small signals: DC characteristic** $\propto\sqrt{}$ **Vin**



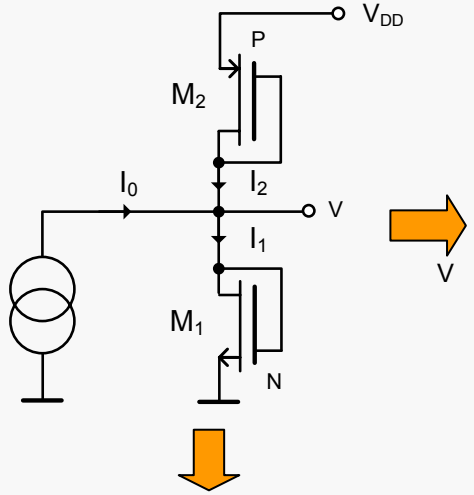
Layout in CMOS 0.35µm AMS process

V. Michal et al. "*Fixed-gain CMOS differential amplifiers with no external feedback for a wide temperature range*", Cryogenic (2009), doi:10.1016/j.cryogenics.2008.12.014

II.2
2st amplifier: linearization and temperature compensation

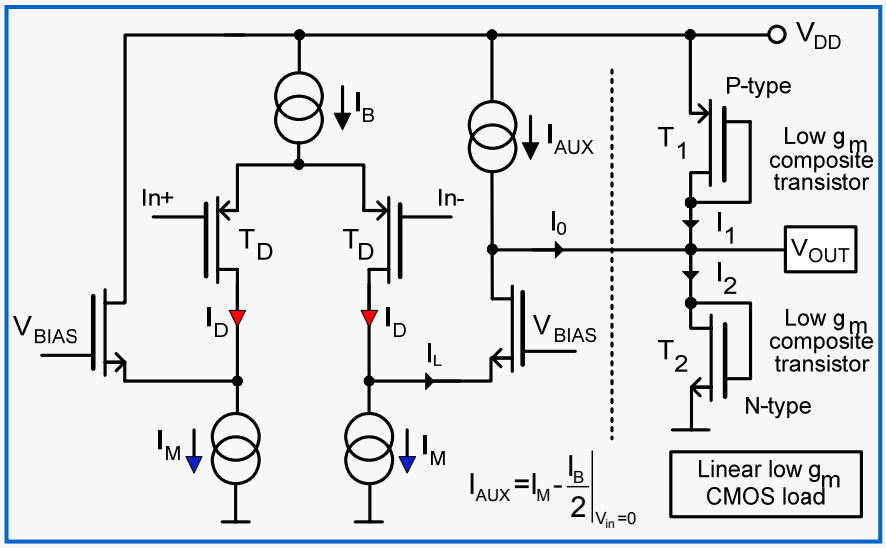


2nd amplifier: new temperature compensation and linearization



Based on cancelling the quadratic terms. The node equation can be written:

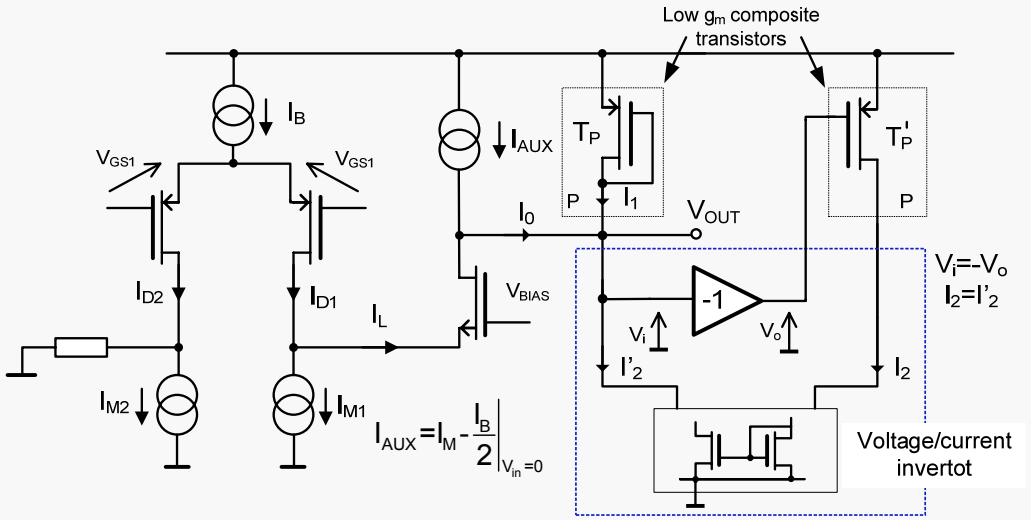
$$\frac{\beta_1}{2}\left(V - V_{TH1}\right)^2 = \frac{\beta_2}{2}\left(V_{DD} - V - \left|V_{TH2}\right|\right)^2 + I_0$$



The extraction of output voltage leads to (assuming $\beta_1 = \beta_2$, $V_{TH1} = V_{TH2}$):

$$V = \frac{V_{DD}}{2} + \frac{I_0}{\beta\left(V_{DD} - 2\cdot\left|V_{TH}\right|\right)}$$

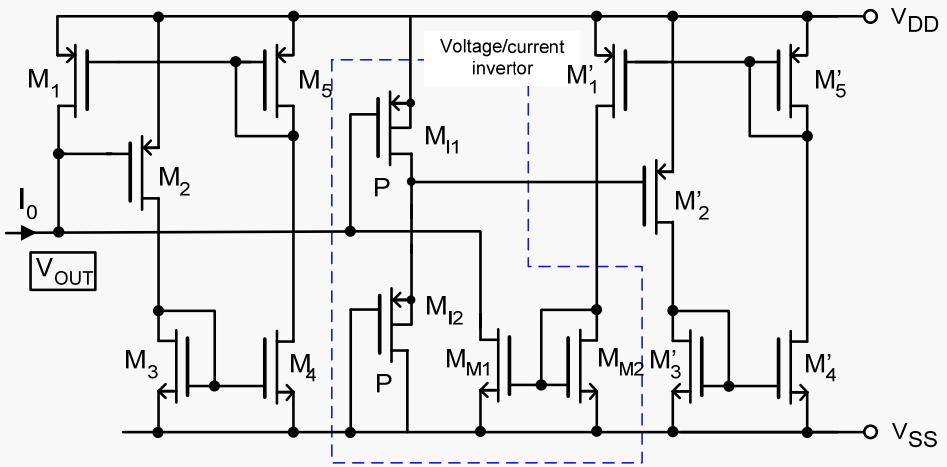
Condition: $\beta_1=\beta_2$, $V_{TH1}=V_{TH2}$: solution



Symmetrisation of the low g_m linear load

Single well

Symmetric low-g_m CMOS load



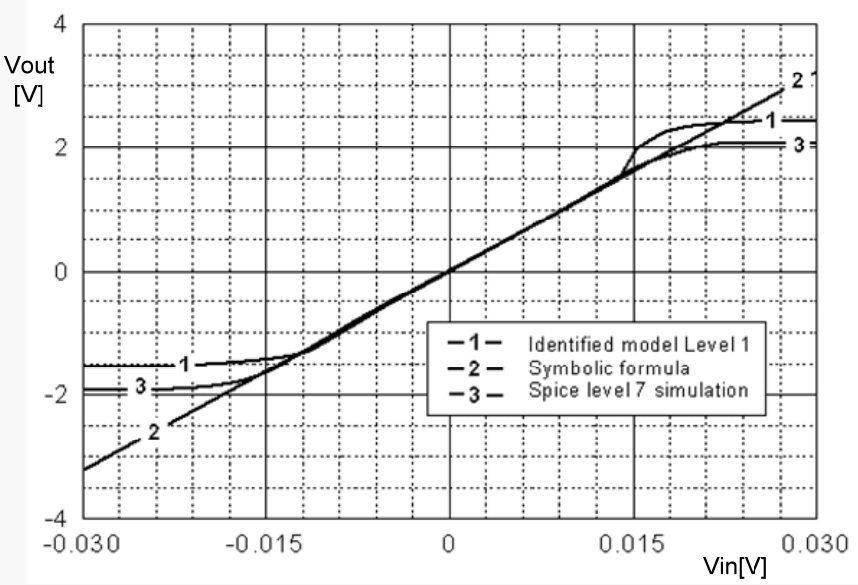
Analysis of DC transfer

➔ **DC transfer function:**

$$V_{out} = \frac{1}{2}V_{DD} + \frac{\frac{1}{2}I_B - \frac{1}{8}\left(\sqrt{4\cdot I_B - KP_P\cdot\frac{W_D}{L_D}\cdot\Delta V_{GS}^2} + \sqrt{KP_P\cdot\frac{W_D}{L_D}}\cdot\Delta V_{GS}\right)^2}{KP_P\cdot\frac{W_{eff}}{L_{eff}}\left(V_{DD} - 2\cdot|V_{TH,P}|\right)}$$

➔ **Gain is given by derivation:**

$$G_0 = \left.\frac{dV_{out}}{d\Delta V_{GS}}\right|_{\Delta V_{GS}=0} = \frac{1}{2}\cdot\frac{\sqrt{I_B\cdot\frac{W_D}{L_D}}}{\sqrt{KP_P}\cdot\frac{W_{eff}}{L_{eff}}\cdot\left(V_{DD} - 2\cdot|V_{TH,P}|\right)}$$



DC transfer characteristics

The voltage gain as the function of:

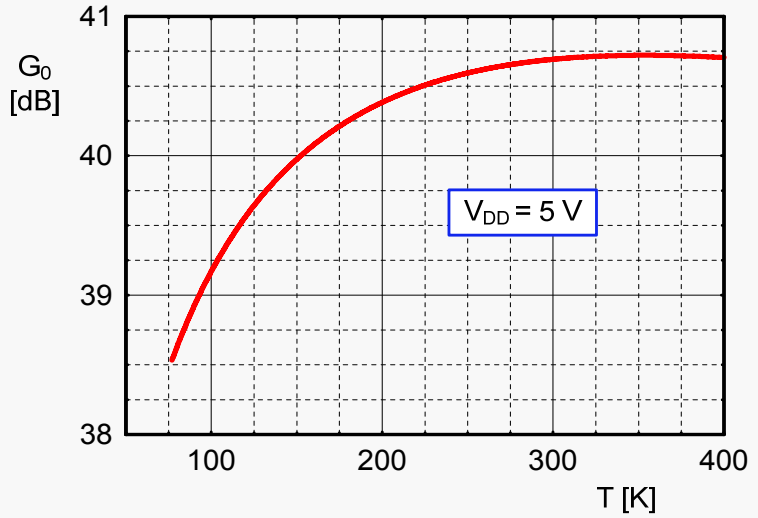
- $\sqrt{(W/L)_D}/(W/L)_{eff}$ ratio,
- Technological parameters: $\sqrt{KP_P}$, V_{THP}.
- Bias current I_B and power supply voltage V_{DD}.

	KP	V_{TH}	V_{DD}	I_B	W_D/L_D	W_{Eff}/L_{Eff}
$S_{x_i}^{G_0}$	$-\frac{1}{2}$	$\frac{2\cdot V_{THP}}{V_{DD} - 2\cdot V_{THP}}$	$-\frac{V_{DD}}{V_{DD} - 2\cdot V_{THP}}$	$\frac{1}{2}$	$\frac{1}{2}$	−1

Temperature compensation principle: current / voltage biasing

➔ **Gain is given by derivation:**

$$G_0 = \left.\frac{dV_{out}}{d\Delta V_{GS}}\right|_{\Delta V_{GS}=0} = \frac{1}{2}\cdot\frac{\sqrt{I_B\cdot\frac{W_D}{L_D}}}{\sqrt{KP_P}\cdot\frac{W_{eff}}{L_{eff}}\cdot\left(V_{DD}-2\cdot\left|V_{TH,P}\right|\right)}$$

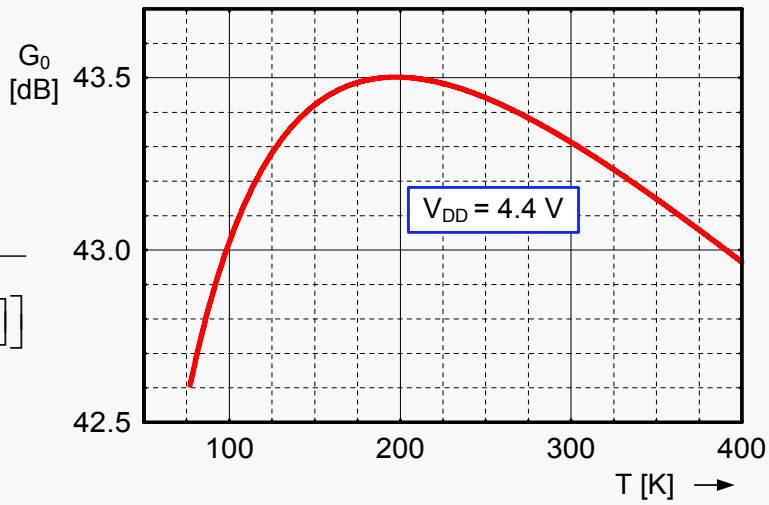


➔ **We replace the elements without temperature dependence by *C*:**

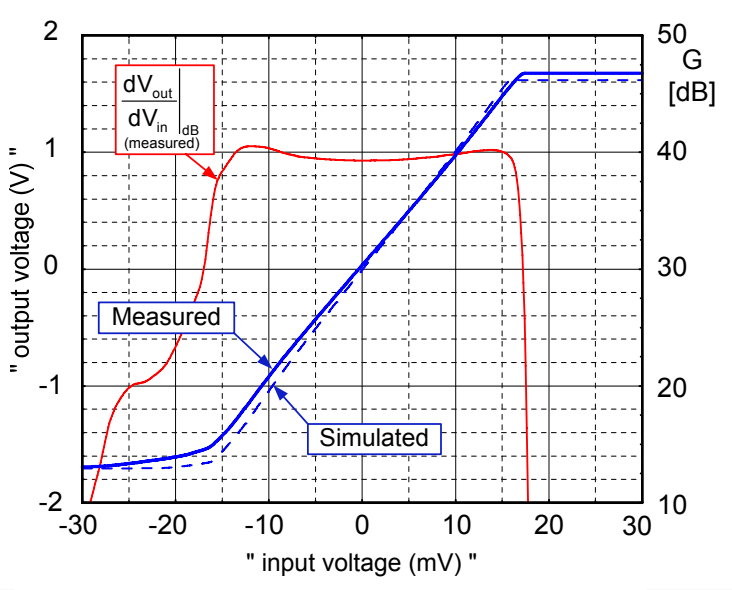
$$G_0(T) = \frac{C}{\sqrt{KP_P(T)}\cdot\left(V_{DD}-2\cdot\left|V_{TH,P}(T)\right|\right)}$$

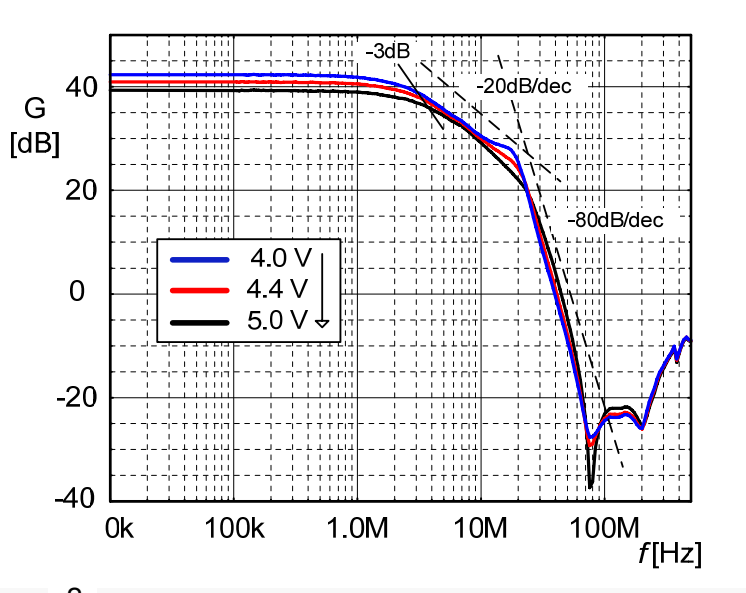
➔ **Which leads to:**

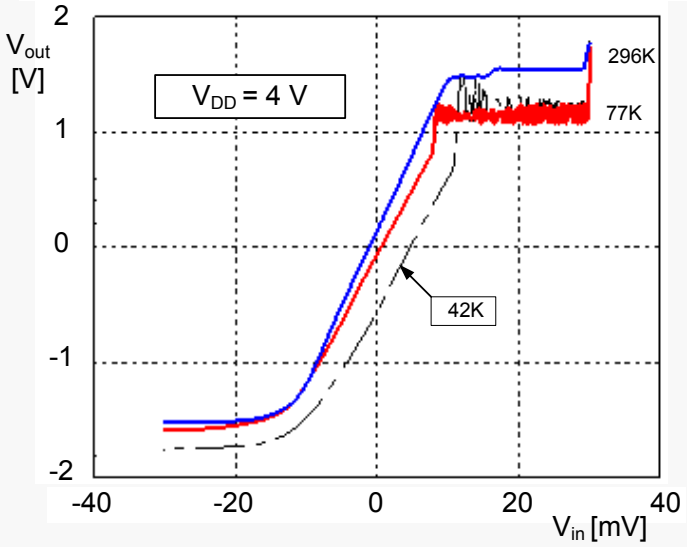
$$\frac{G_0(T)}{C} = \frac{1}{\sqrt{KP_P(T_0)\cdot\left(\frac{T}{T_0}\right)^{-x}}\cdot\left[V_{DD}-2\cdot\left|V_{TH,P}(T_0)\right|\left[1+\alpha_{THX}\cdot(T-T_0)\right]\right]}$$

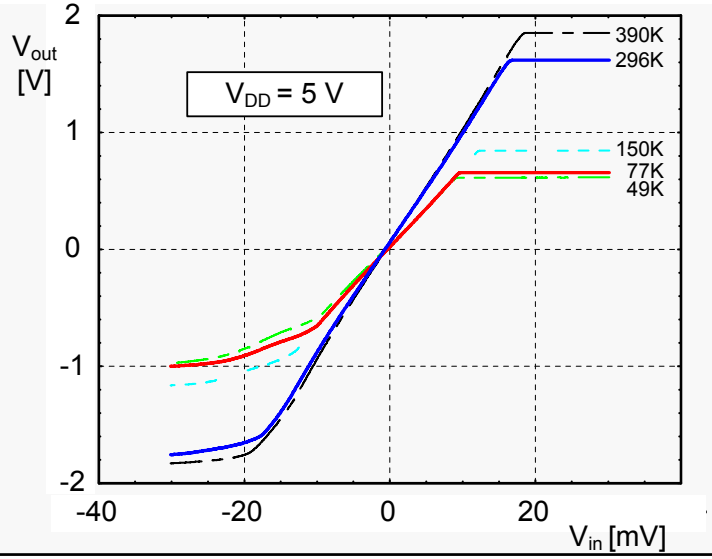


Measurements: wide temperature results

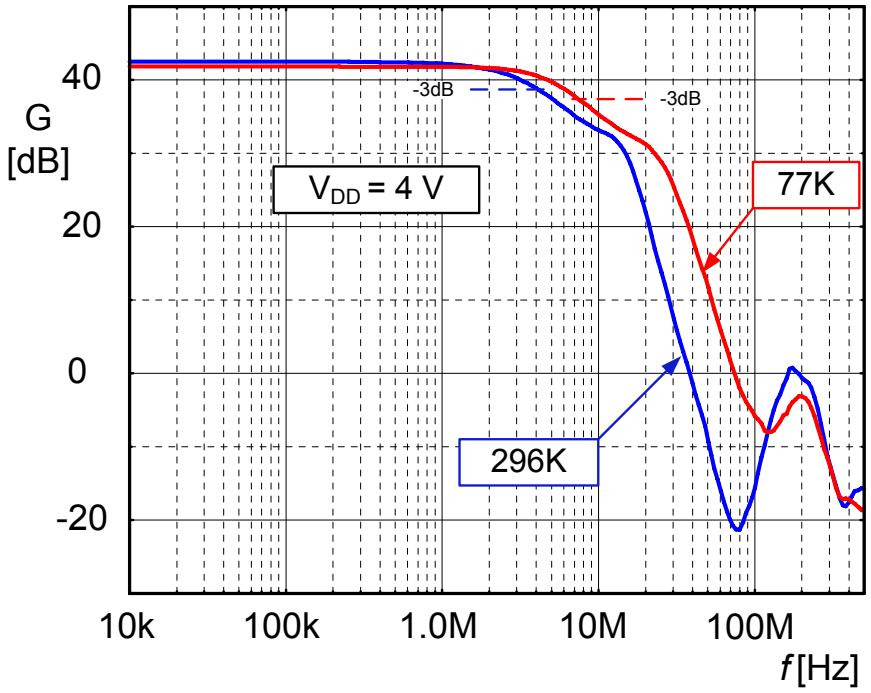




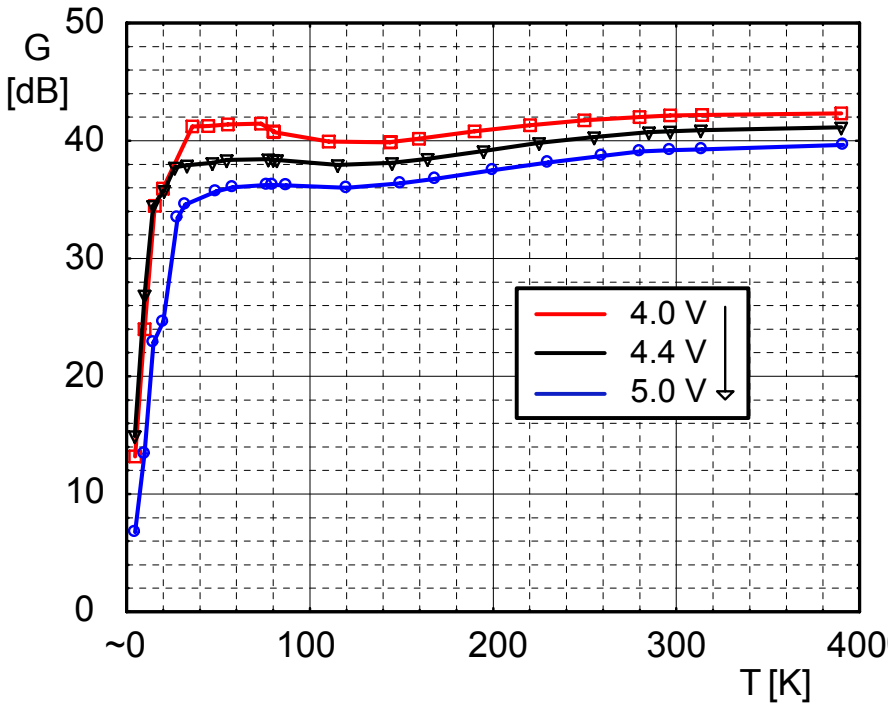




Measurements: wide temperature results



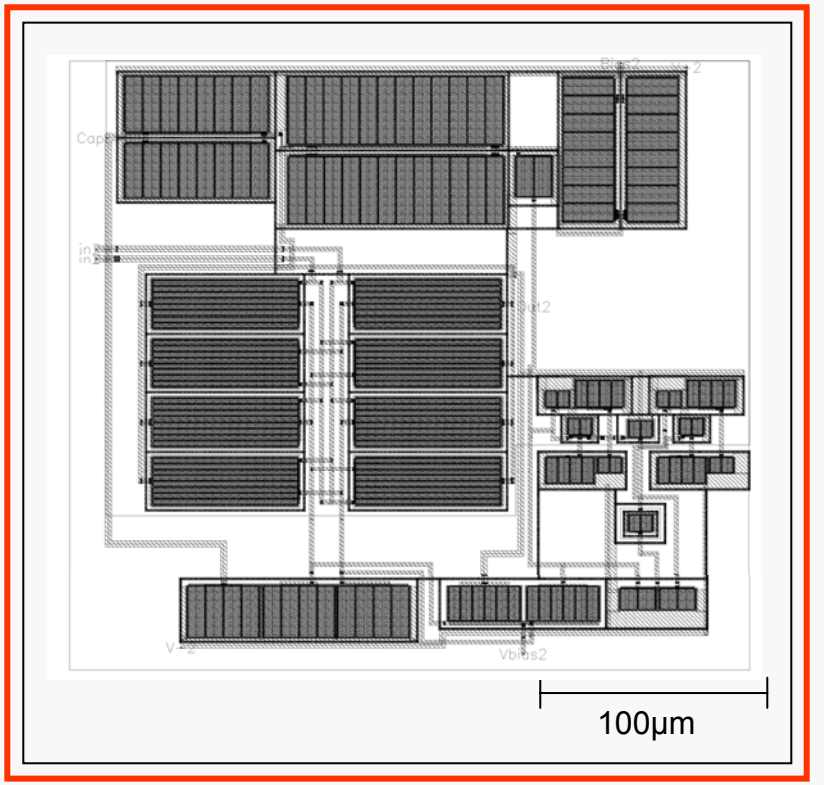
AC transfer @ 2.5V, 290 and 77 K



Temperature gain gunction for three VDD voltages

2st amplifier: summary

- New amplifier architecture for extreme temperature range
- Wide linear operation Temperature compensation
- Low noise, wide BW achieved with low Iq (Up to 1GHz GBW for 1.3mA quiscence current)
- Highly competitivite to bipolar amplifier, promising as compact block for VLSI integration



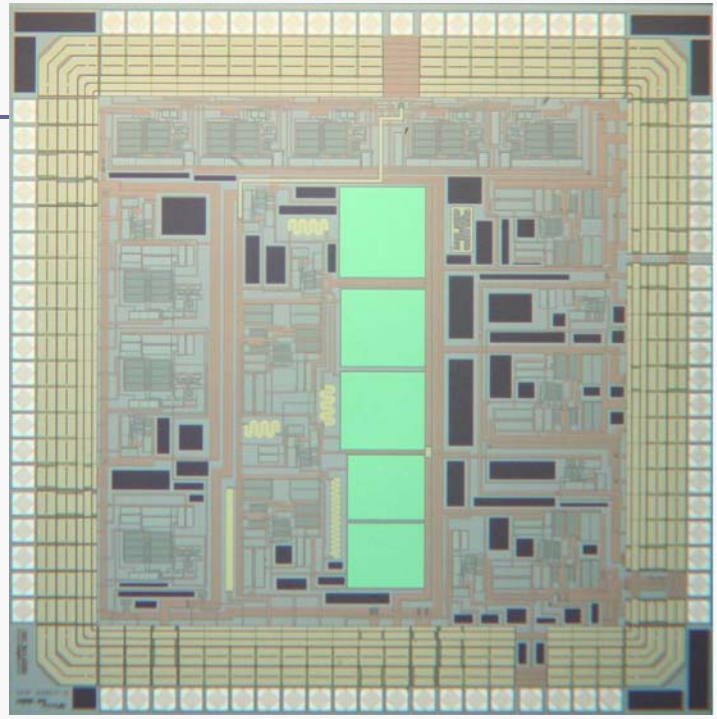
Layout in CMOS 0.35µm AMS process

V. Michal et al. "*Fixed-gain CMOS differential amplifiers with no external feedback for a wide temperature range*", Cryogenic (2009), doi:10.1016/j.cryogenics.2008.12.014

Comparison with industrial state of the art

Key parameters of developed amplifiers

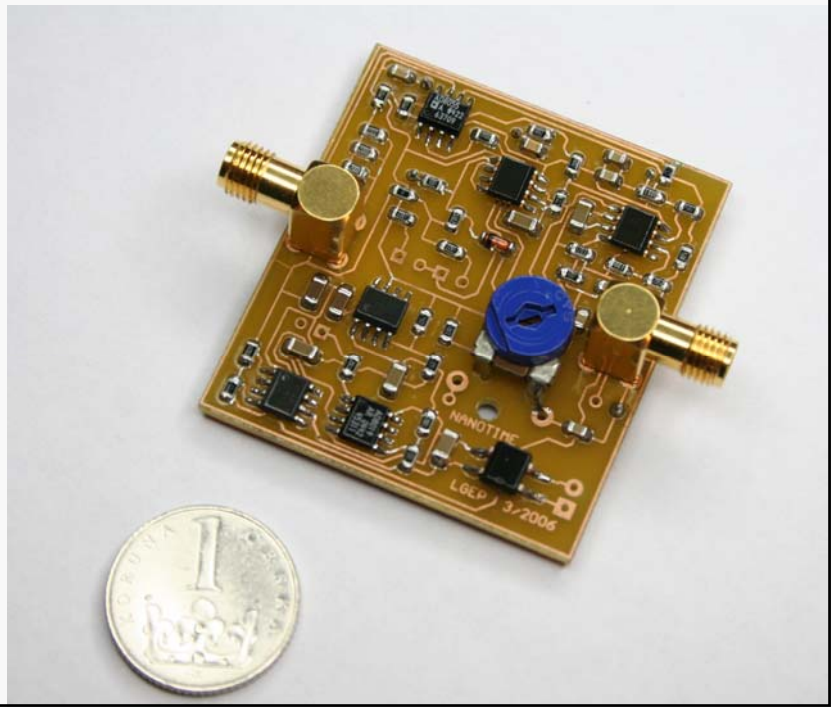
MEASURED PARAMETERS	TYPE *I* AMPLIFIER	TYPE *II* AMPLIFIER
Operating supply voltage	4.1 V to 5.5 V	3.6 V to 5.5 V
Quiescent current	2.1 mA	1.3 mA[1]
– 3 dB bandwidth (T = 290 K)	10 MHz **(GBW=1GHZ)**	4 MHz at V_{DD} = 5 V
– 3 dB bandwidth (T = 77 K)	17 MHz **(GBW=1.7GHZ)**	10 MHz at V_{DD} = 5 V
Input noise (T = 290 K)	5 nV/Hz^{½}	5 nV/Hz^{½}
Input noise (T = 77 K)	2 nV/Hz^{½}	3 nV/Hz^{½}
Gain G_0 (T = 290 K)	39.85 dB	39.3 dB at V_{DD} = 5 V
Δ Gain 270 K – 390 K	– 0.12 dB	– 0.5 dB at V_{DD} = 4 V
Gain error (at T = 77 K)	– 1.2 dB	– 1.3 dB at V_{DD} = 4 V
THD[2] (V_{out} = 0.3 V_{pp})	1 %	0.03 %



Industrial differential amplifiers *(room temperature)*

Type	Configuration	GBW [MHz]	SR [µV/s]	VDD [V]	Iq [mA]	Input noise nV/√Hz	Other
AD8045	OA Bipolar	1000	1350	3.3 - 12	19 × 3	3	
LTC6401-20	Fixed gain 20dB+/-0,6dB Bipolar	1300	4500	2,85-3,5	50 × 3	2,1	R_{in}=200Ω
LT1226	OA Bipolar	1000	400	5-36	7 × 3	2,6	25dB stable
OPA699	OA Bipolar	1000	1400	5-12	22,5 × 3	4,1	12dB stable
OPA2354	OA CMOS	250	150	2,7-5,5	7,5 × 3	6,5	
INA2331	Instrumentation CMOS	50	5	2,5-5,5	0,5	46	
INA103	Instrumentation BIPOALR	80	15	9-25	9	1	

III.
High performances analog frequency filters



Motivation

- Correct analog processing close to the physical sensor is the best way to condition the signal
- Noise is still based on the reduction of the spectrum (Lock-in, FFT …)
- Frequency filters: crucial block

- ➔ Objectives:
  - Optimization of the dynamic range (attenuation)
  - Mastering of the topic, related work not presented in the thesis (goal-lossy active filters [*], adaptive analog signal processing [**], microwave superconductor filters [***])

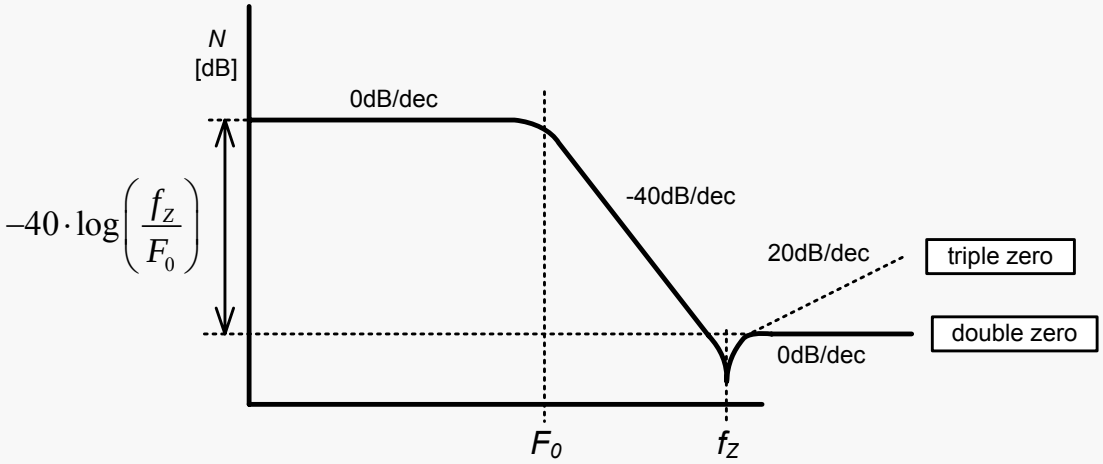
[*] V. Michal et al. "*Active filters based on goal-directed lossy RLC prototypes* ", Speto int conference (2006)

[**] V. Michal et al. "*The analog Filter Design and Interactive Analog signal Processing by PC*" WSEAS (2005)

[***] V. Michal et al. "*Superconducting NbN band-pass filter and Matching circuit for 30GHz RSFQ Data Converters* ", IEEE conference Radioelek, 2009

Real-world frequency filters

- Non-ideal passive components:
  - F_0,Q inaccuracy, higher order effects, can be compensated [*]
- Non ideal active components
  - F_0,Q inaccuracy, DC offset, attenuation



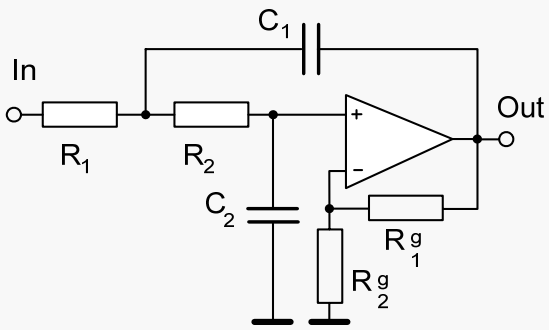
Effect of parasitic zeros in the AC response of frequency filter

Parasitic zeros can not be compensated by predistortion [**]

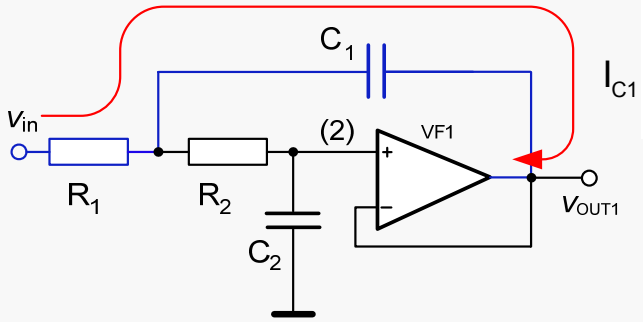
[*] Geffe, P. R., IEEE Trans., Vol. CAS-23, pp.45-55, 1976

[**] see: *Stop-band limitations of the Sallen-Key low-pass filter*", AN Texas instrument, see also Schmid, H. Moschytz, G.S, Circuits and Systems, vol.1, 1998, p. 57-60.

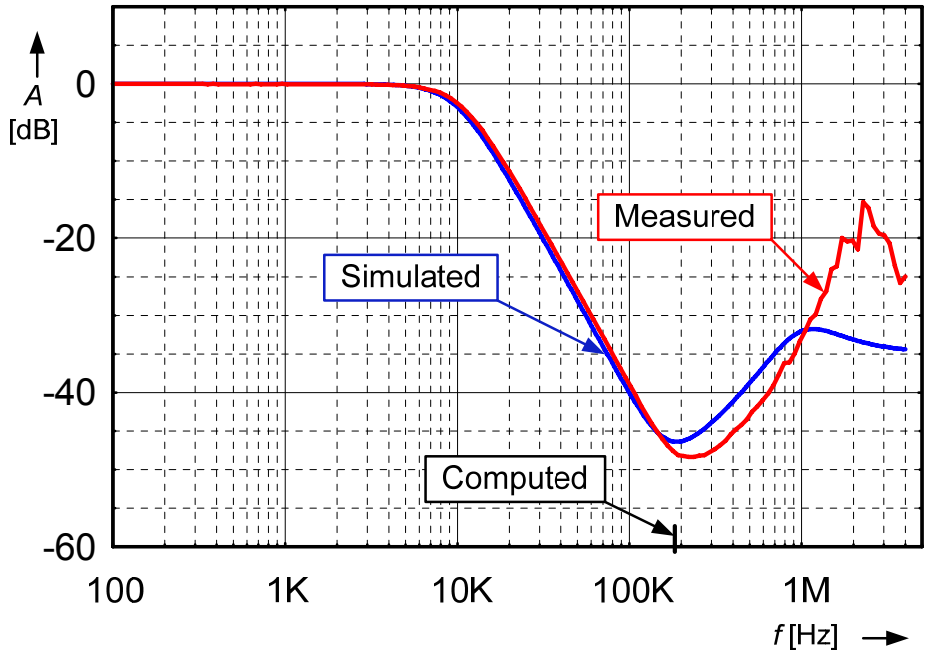
Example: real Sallen-Key filter



LP Sallen-Key biquad [*]



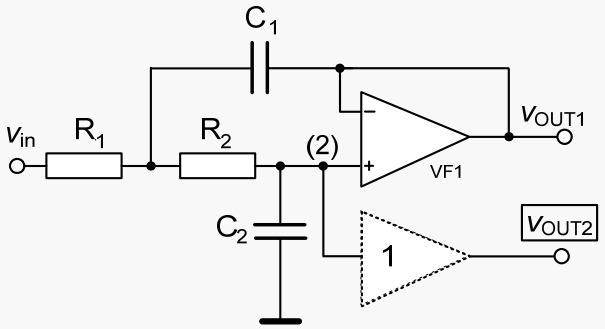
parasitic transfer zeros in the stopband



Parasitic zero occurs at : $f_Z = \frac{1}{2\pi}\sqrt[3]{\frac{2\pi GBW}{R_0 R_2 C_1 C_2}}$

[*] Sallen.R.P-Key.E.I., Circuit Theory. Vol. 7. 1955, p. 74-85.

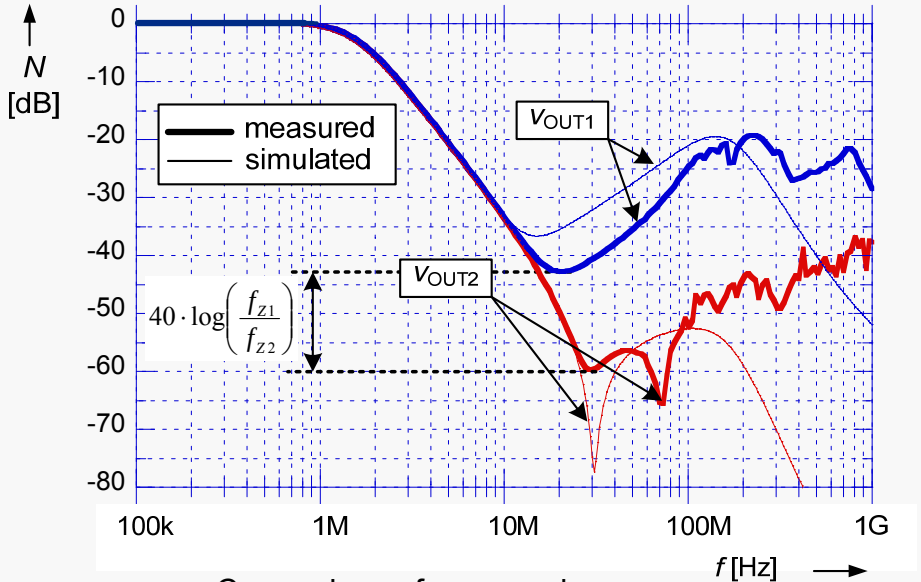
Real Sallen-Key: compensation



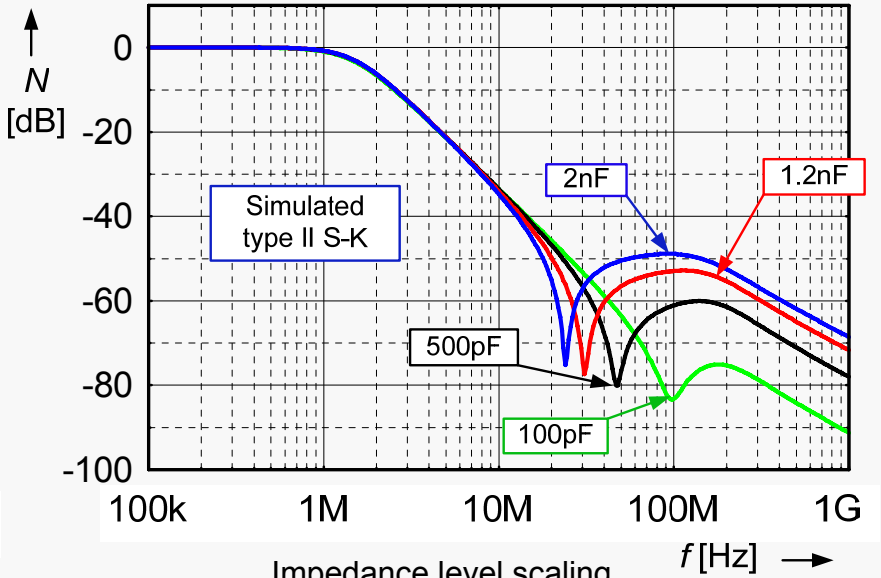
Improved Type II Sallen-Key

$$f_{Z(2)} \cong \frac{1}{2\pi}\sqrt{\frac{A\cdot\omega_P}{C_1 R_{OUT}}}$$

reduced order of the root, only R_{out} and C_1 contribute to the frequency ➔ ***Higher attenuation***

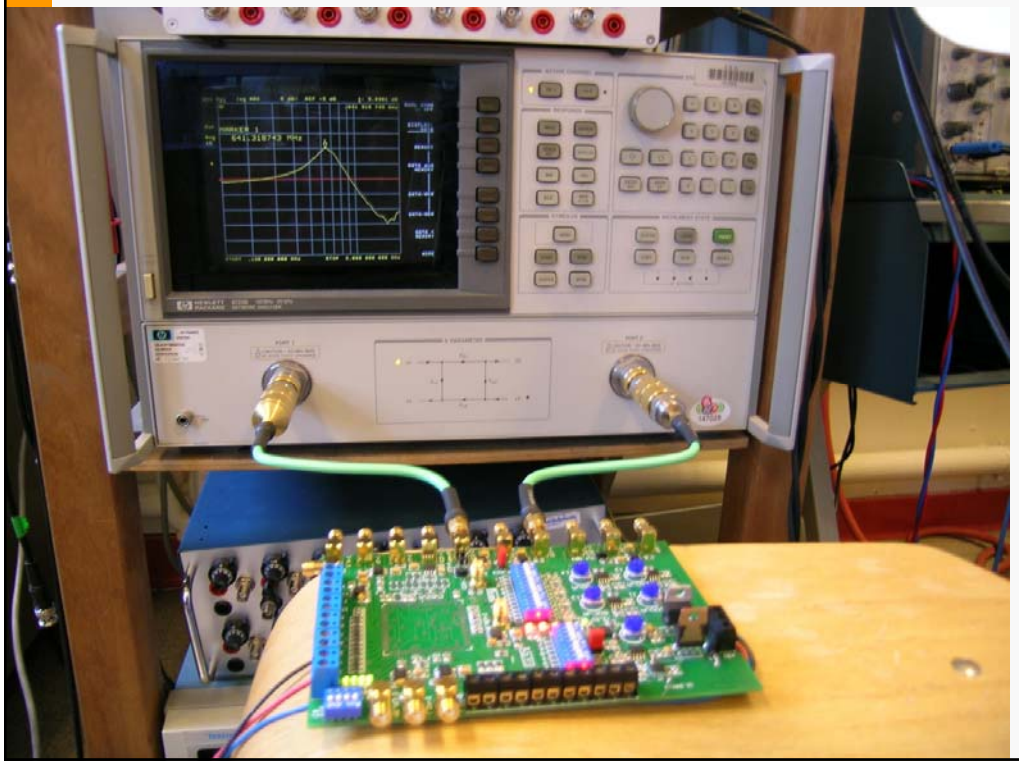


Comparison of v_{OUT1} and v_{OUT2}



Impedance level scaling

III.1
CCII biquadratic section



Proposed solution

Removal of the parasitic zeros ensure constant -40db roll-off

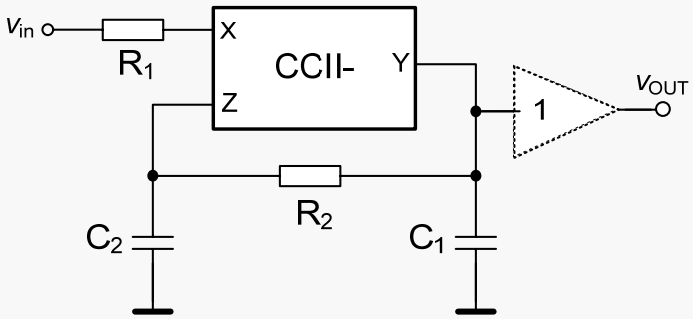
- Division of the frequency band in two regions:
  - **region up to f_0**, whereas the DC transfer and resonance gain is ensured by the active element
  - **region stop-band**, where the high attenuation is ensured by the passive RC filter

- **Design rules:** Interruption of direct signal way,
  Passive filters containing grounded capacitors

Adopted solution: topological transformation of circuits presented in [*]

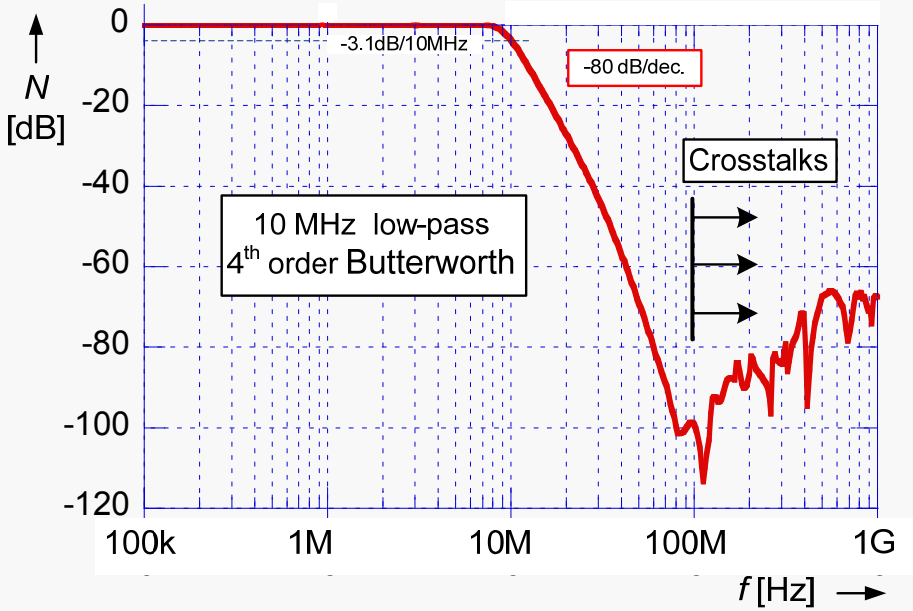
[*] Liu, S-I., Tsao,H-W; Wu,J., Tsay, J-H. "*Realizations of the single CCII biquads with high input impedance*", IEEE Sympoisum on Circuits and Systems, 1991.

New biquadratic section CCII-



CCII- low-pass biquadratic section with eliminated parasitic transfer zero

$$f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \qquad Q = \frac{\sqrt{R_2}}{\sqrt{R_1}} \cdot \frac{\sqrt{C_1 C_2}}{C_1 + C_2} = \frac{1}{2} \cdot \sqrt{\frac{R_2}{R_1}}\Bigg|_{C1=C2}$$



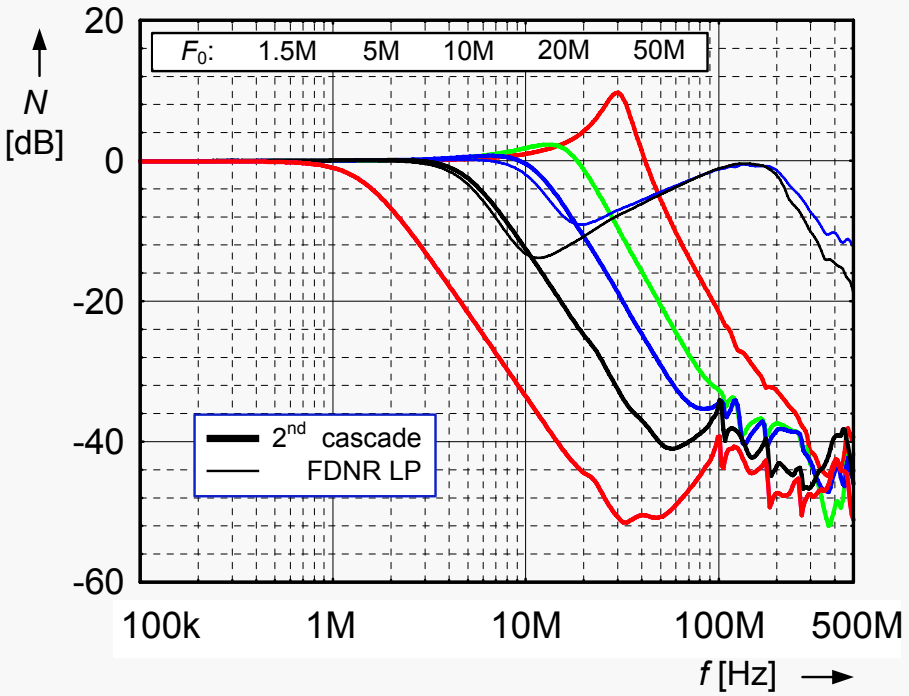
measured AC response of 10MHz 4th order LP filter

Stop band behavior (single pole model of CCII):

$$H(s) = \frac{\Omega_0^2}{\left(s^2 + s\cdot\Omega_0/Q_0 + \Omega_0^2\right)} \cdot \frac{\left(\omega_P \cdot A_0 + s\right)}{\left(\omega_P \cdot (1+\alpha)\cdot A_0 + s\right)}$$

V. Michal et al. "*Low-pass Biquadratic Filters With High Suppression Rate* ", IET journal Electronics Letters, ELL-2009-0416.R1

Summary of achieved features



Attenuation floor independent on the f_0. comparison with lossy R-FDNR biquad [*]

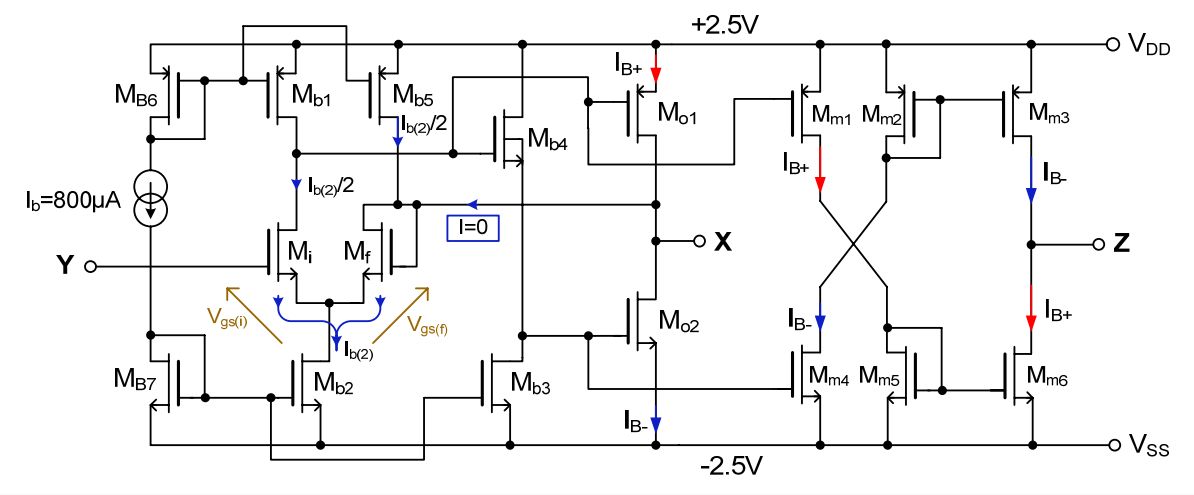
- **The attenuation is only limited by signal leakage**
- **Does not depend on the f_0**
- **Using low-performance voltage buffer is allowed**
- **Direct connection to the DAC input**

➔ **price and consumption are reduced**

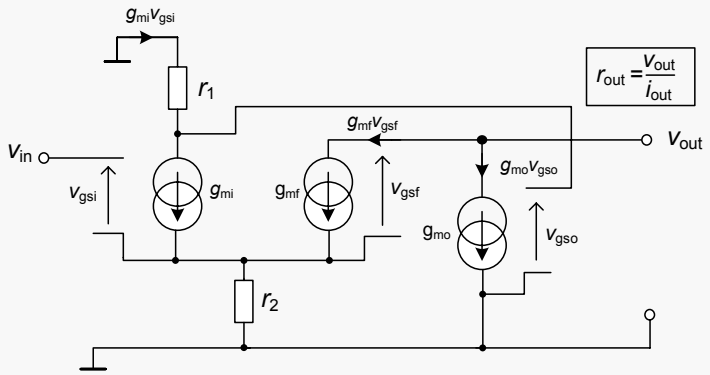
[*] *Martinek, P.* , Proceeding of Radioelek, 2008

III.2
High performances CCII current conveyor

Design of Ultra-low R_{out} CCII-



CCII- with very low output resistance voltage buffer

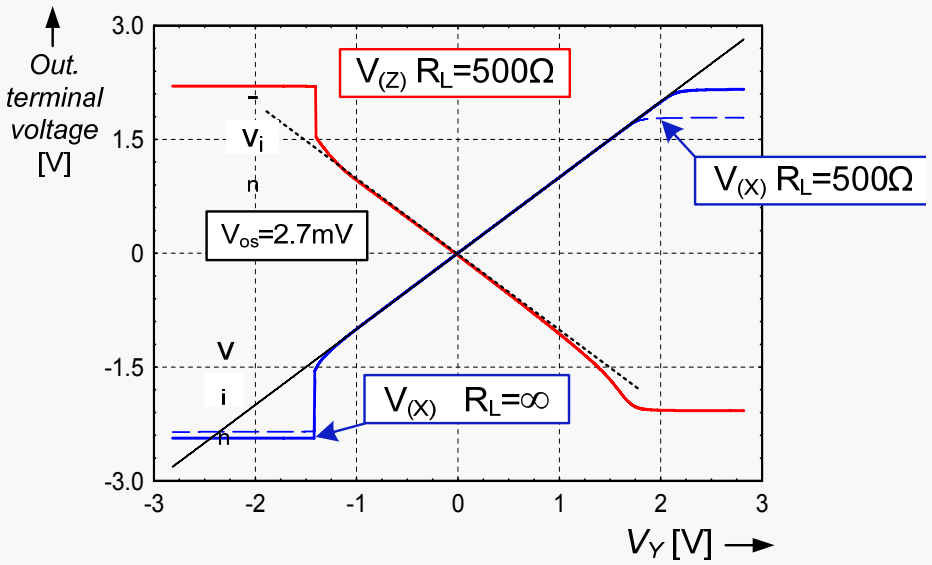


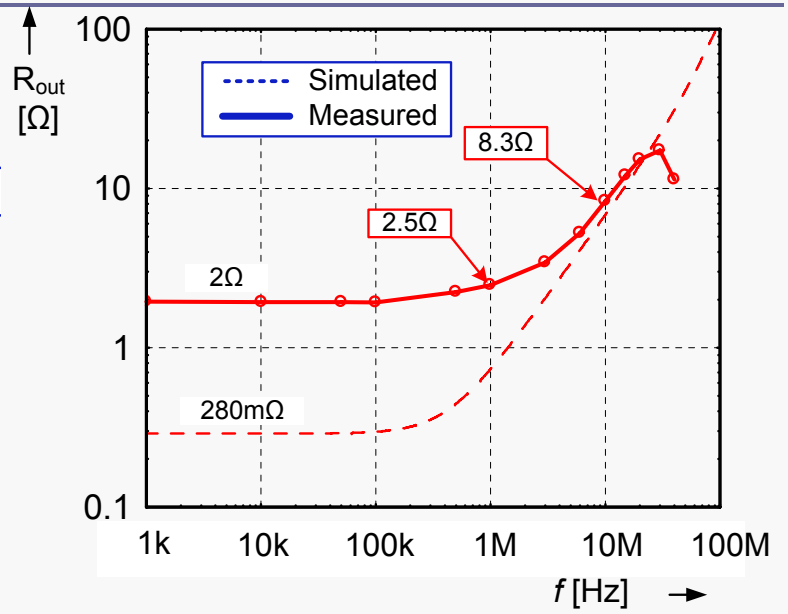
simplified small signal model

$$r_{out} = \frac{v_{out}}{i_{out}} = \frac{2 \cdot r_2 + 1}{r_2 \cdot g_{mf} + r_1 \cdot r_2 \cdot g_{mo} \cdot g_m + g_m}$$

$$\approx \frac{2}{r_1 \cdot g_{mo} \cdot g_m} \Rightarrow 0$$

Global performances: state of the art





V_{DD}	+/- 2.5V
Quiescence current	11 mA
Port X,Z voltage swing	+/- 1.5 V
Port X,Z driving capacity	+/- 20 mA
Port Z DC impedance	~7.5 MΩ
Port X offset voltage	2.7 mV
Port Z offset current	2.25 µA
-3dB AC transfer Y→X	~110 MHz
Port X resistance @ DC	2 Ω
Port X impedance @ 1MHz	2.5 Ω
Port X impedance @ 10MHz	8.5 Ω

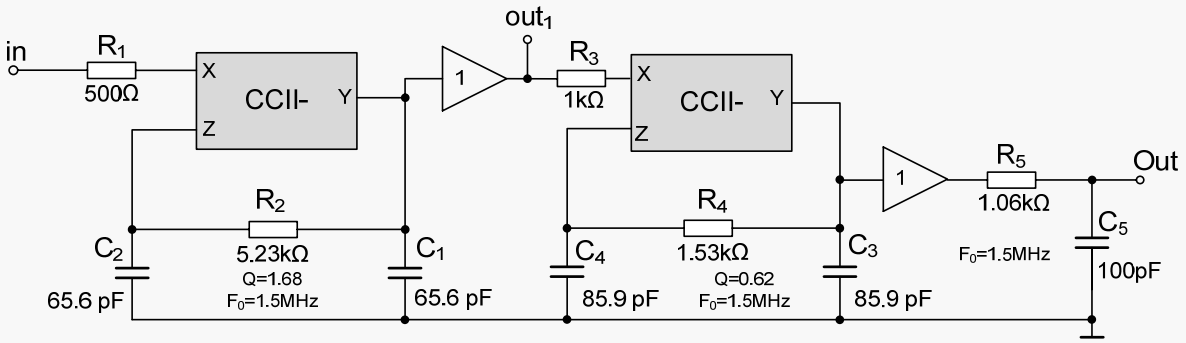
Summary of achieved performances

Recently published results on UVC [*]:

terminal	10kHz	1MHz	10kHz
z+	2.1Ω	10Ω	89Ω
z-	0.9Ω	8.2Ω	76kΩ

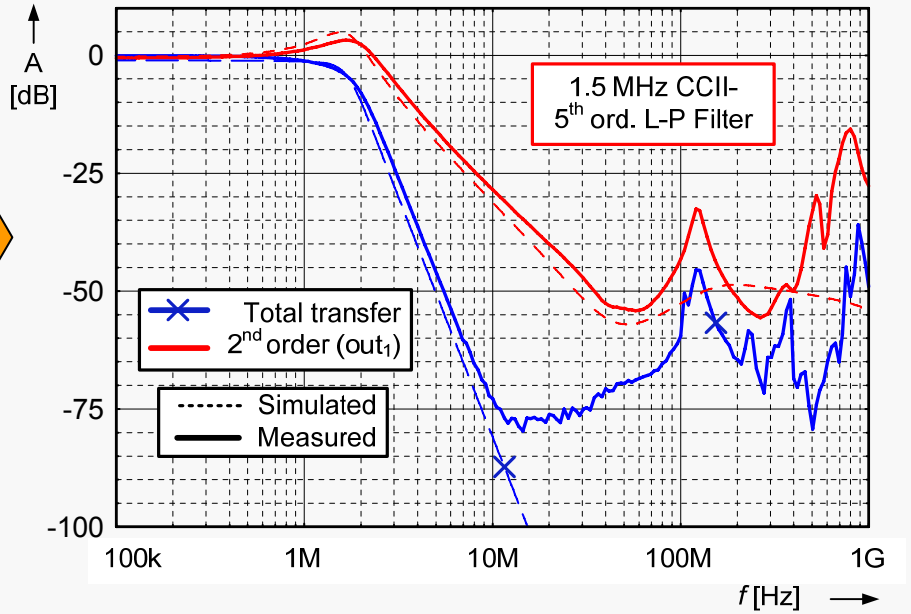
[*] Minarcik,M., Vrba,K. ICN'07

Experimental result: 1.5MHz LPF

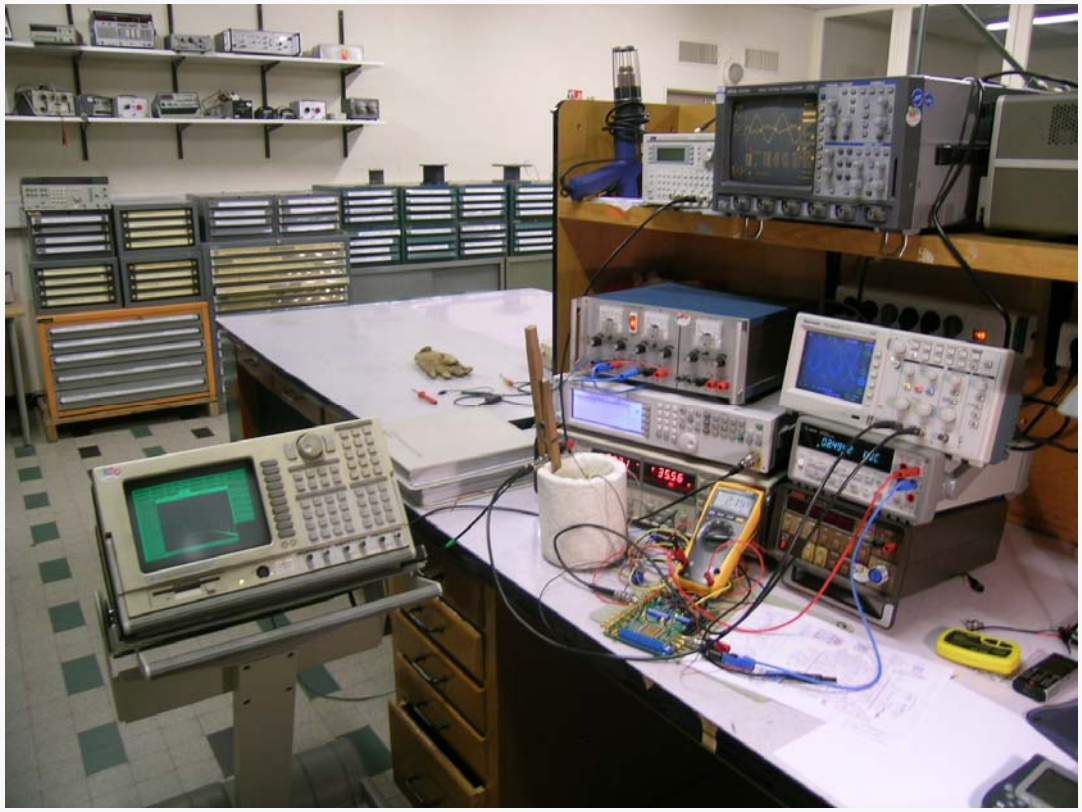


5th order LP filter (Butterworth) using new CCII biquadraic section

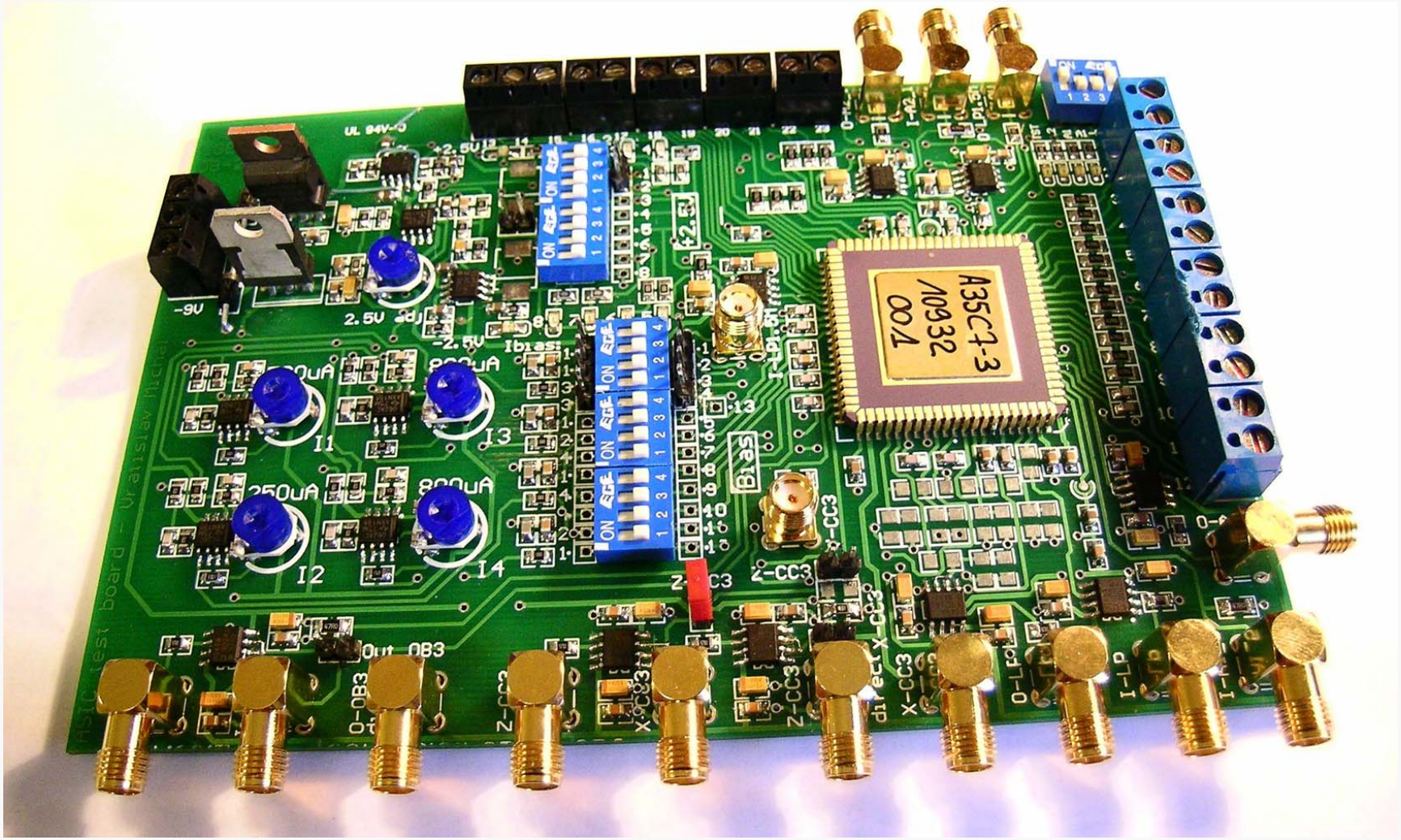
characteristic of 1.5MHz 5th ord. LP filter



IV Summary



Summary: example of test facility



Conclusion: scientific contribution

New generation of differential (instrumentation) amplifiers

Feedback-free architecture. State-of-the-art of the performances, competitives with the bipolar tehcology: High BW, low power consumption, low noise level

Cryogenic instrumentation, innovants design approaches

Analytical thermal model of the MOS, hybrid voltage-current biasing method

Analog front-end circuits optimizing

New structures with improved behavior in stop-band, large extension of band-with

Fabricated circuits redady to use in the new generation THz detector test set-up

Perspectives: Integration of the electronic in the THz test-bench

Implementation of designed circuits in industrial applications

French

Corrections..

Thank you

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