Chapter IV

Low Noise Amplifier Design and Optimization

IV.1 CMOS LNA Design and Optimization Overview

Low Noise Amplifier (LNA) is the most critical part of a receiver front end, in term of the receiver performance. Many circuits with different configurations have been proposed for LNA, in different applications. After choosing proper circuit for LNA, this circuit must be designed and optimized. Various techniques have been proposed for LNA design and optimizations. In this section an overview of available LNA circuits and design and optimization techniques will be overviewed.

IV.1.1 CMOS LNA Circuits

LNA circuits in CMOS technology are designed as Common Source (CS) or Common Gate (CG) stages. Cascode stage that is widely used in CMOS RF LNAs, can be considered as current –reuse configuration of a CS stage, followed by a CG stage. Choosing proper circuit depends on the specific application for which the LNA is designed and the designer experiences. For each application, some of LNA characteristics are more important than the others and this is a guideline for the designer to choose proper circuit for LNA.

IV.1.1.1 CS versus CG configuration

CS and CG are two widely used transistor configurations in CMOS LNA circuits. CS LNA has high gain and good noise performance [1]. Placing an inductor in the source of a CS stage the well known Inductive Source Degenerated is obtained. This inductor affects the gain and noise performance of LNA, as will be discussed in the future. CG configuration leads to low power, robust against parasitic and stable circuit [1], [2]. CG configuration has weak noise performance [3]. Some techniques, such as capacitive cross coupling, has been presented to improve the CG stage noise performance [4], [5], [6].

Wideband input matching is possible for CG configuration and hence this configuration is widely used in broadband LNA circuits [7], [8]. However CS configuration may be used in wideband applications using special feedback or matching circuits. Inductive source degenerated CS configuration is conventionally used in narrowband LNA circuits [9].

IV.1.1.2 Cascode LNA

Cascode LNA promises high power gain, good noise performance, low power consumption and high reverse isolation [10], [11], [12]. In lower bands of microwave frequencies, the noise sources of the upper transistor of cascode stage (cascode transistor) is degenerated by the lower transistor output impedance [13]. Consequently cascode stage has superior noise performance.

Unfortunately excellent noise and gain performance of cascode stage degrades in very high frequencies. This is due to substrate parasitic admittance at the drain-source common node that increases as frequency increases [14], [15]. In consequence of lower impedance in the source of upper transistor, its drain noise appears in the output [3], [16]. As will be explained later, cascode stage has widely been used in mm-wave frequencies.

Like a CS stage, cascode stage is proper for narrowband applications, however using feedback techniques makes possible using of cascode stage in multi band and wide band applications [17], [18]. Another way to use cascode configuration in wideband application is using complicated LC matching networks in the input [19].

IV.1.1.3 Single Stage Versus Multistage

Multi stage LNA proposes higher gain, in comparison with single stage LNAs. The noise performance of multi-stage LNA is not degraded, since the noise performance is mainly determined by the first stage. This can be shown using Frees noise equation [20]:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_N - 1}{G_1 G_2 \cdots G_{N-1}} \quad \text{(IV-1)}$$

Where F is the total noise factor and F_i and G_i are the noise factor and power gain of i^{th} stage. Normally the gain of first stage is high enough to suppress the effect of second stage in the total noise figure.

Based on the above equation, higher gain for LNA is very important to reduce the noise contribution of the mixer (following the LNA) in the NF of receiver front end. Consequently multi stage LNA is used in high performance receivers. Unfortunately two stage LNA needs high DC power consumption and hence is not suitable for low power applications.

Two successive cascode stages have widely been used in various applications, from few GHz to mm-wave bands [21], [22], [23].

IV.1.2 CMOS LNA Characteristics

As its name implies, noise performance and power gain are the most important characteristics of an LNA. Beside these characteristics, the main parameters affecting the selection of a popper circuit for an LNA are DC power consumption, bandwidth, stability, linearity, supply voltage and chip area.

IV.1.2.1 Noise and Power Gain Matching

Using optimum noise matching, minimum achievable noise figure of an LNA (NF_{min}) is obtained. On the other hand, power gain (conjugate impedance matching) yields the maximum available power gain for a circuit. Unfortunately these two matchings are contradictory and hence both of maximum available gain and minimum noise figure are not simultaneously possible. Fortunately, in CMOS technology these two matching conditions are very close together and this is an important advantage of CMOS circuits that can alleviate inherit crucial noise performance of CMOS technologies [23]. Thanks of this property, *simultaneous noise and power matching* becomes possible in CMOS technology [12].

For maximum power gain matching, the input impedance of LNA must have a resistive term. Then matching network transforms this resistance to the real part of the source (generator) impedance. Different classic techniques to produce required resistive term in the input impedance of an LNA has been shown in Fig. IV-1 [24]. In the case of CG stage, the resistive term is part of the input impedance to the source of the CG transistor. For a CS or cascode stage the input impedance is pour capacitive (in very low frequencies) and hence a resistive part should be added to the input impedance. This is done by a resistive feedback, or a parallel resistance in the gate or a degenerating inductance in the source of CS transistor, as depicted in Fig. IV-1.

Parallel resistance in the gate increases the noise figure of LNA and hence does not used in normal designs. The feedback resistor between drain and gate, forms a self-bias mechanism for transistors, as well contributes in the real part of the input impedance to relax the matching circuit [25].

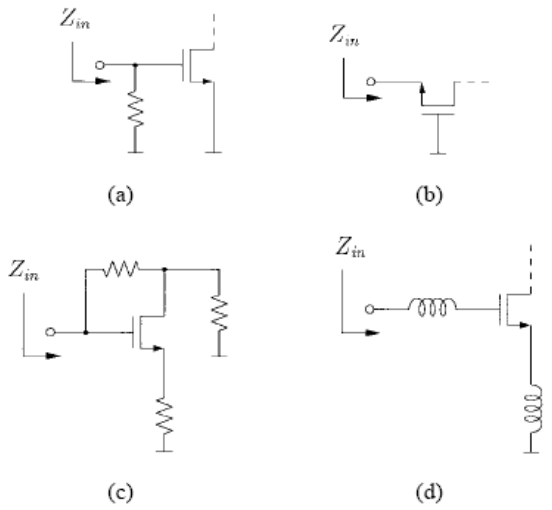


Fig. IV-1. Different classic techniques to produce resistive term in the input impedance of an LNA [24]

Degenerating inductance in the source of CS stage produces a resistive term in the input impedance of MOS transistor. This technique is widely used in CS and cascode LNA circuits [26], [27], [28], [29]. In addition, this inductor makes optimum noise and power points more close together [30]. Gate poly silicon resistance can be used for producing resistive term in the input impedance of a CS stage. In this way the gate resistance is translated to 50 ohm, using an LC network [31]. In [32] a new technique has been proposed that produces a resistive term in the input impedance of a cascode stage, without using degenerating inductor that degrades the gain, in 60 GHz band.

Matching bandwidth is an important factor in designing matching network. CS and cascode stage are proper choices for narrowband designs. Source degenerated cascode or CS stage is exhibits a good narrowband matching, high stability and good noise performance. As mentioned earlier, cascode and CS stages can be used in broadband or multi-standard applications, using resistive feedback or special LC matching networks. In contrast to CS stage, CG stage proposes wideband matching possibility, as described previously. Some special matching techniques have been developed for UWB applications [33].

Direct matching of antenna to LNA in a receiver front end has been considered in recent years [34], [35], [36]. Using this technique, simultaneous optimum noise and power matching of LNA becomes possible.

A part of image frequency rejection is conventionally accomplished by the RF filter in the LNA input. In integrated design, this filter can be designed as a part of input matching network [37], [38], [39].

IV.1.2.2 Noise and Linearity Improvement Techniques

Noise cancellation techniques are used for improvement of LNA noise performance [40], [41], [42]. Many noise cancelling techniques have been developed for CMOS broadband LNAs for UWB[1] applications [43], [7]. These techniques are not necessary in narrowband designs. The reason is that in a narrowband LNA minimum noise figure (NF_{min}) is achievable with proper matching design, however in the case of broadband LNA the matching circuit frequency response varies in the LNAs operation band and can not satisfy NF_{min} in all of the band [7].

[1] Ultra Wide Band

Noise cancelling basis has been depicted in Fig. IV-2 [42]. The noise current due to CS transistors drain thermal noise, and signal current both arrive in the output node from two different paths. Signal current from these paths are in phase, but two arriving noise currents are 180^0 out of phase. Consequently noise current is attenuated in the output, but the desired signal current amplified [7].As shown in Fig. IV-2, noise cancelling techniques are basically feed-forward schemes. Consequently, in very high frequencies, in which the accurate control of signal phase in different paths is not possible, these techniques can not be used. Noise cancelling has been reported for frequencies up to 10 GHz [43].

The external noise originated from other circuits in the chip and coupled through the substrate, affects the noise performance of a CMOS LNA [44], [45]. Noise figure degradation of an LNA, due to power and ground noise, has been analyzed in [46]. Global guard ring around whole of the LNA circuit can be used for reducing penetration of noise of digital circuits into the LNA section. This issue is very important in System-on-Chip (SoC) design [47].

Nonlinearity of a CMOS LNA is due to the nonlinear nature of MOS transistor conductance and trans-conductance and hence the transistor's bias greatly affects the linearity of the circuit. Linearity analysis for CS, CG and cascode stages have been addressed in various papers [48], [3], [49]. Drain current can be explained as:

$$i_{ds} = g_m v_{gs} + \frac{g_m'}{2!} v_{gs}^2 + \frac{g_m''}{3!} v_{gs}^3 + \cdots \qquad \text{(IV-2)}$$

g'' causes the third order nonlinearity and is negative in weak inversion and is positive in strong inversion regime of MOS transistor. Consequently, using two transistors in different

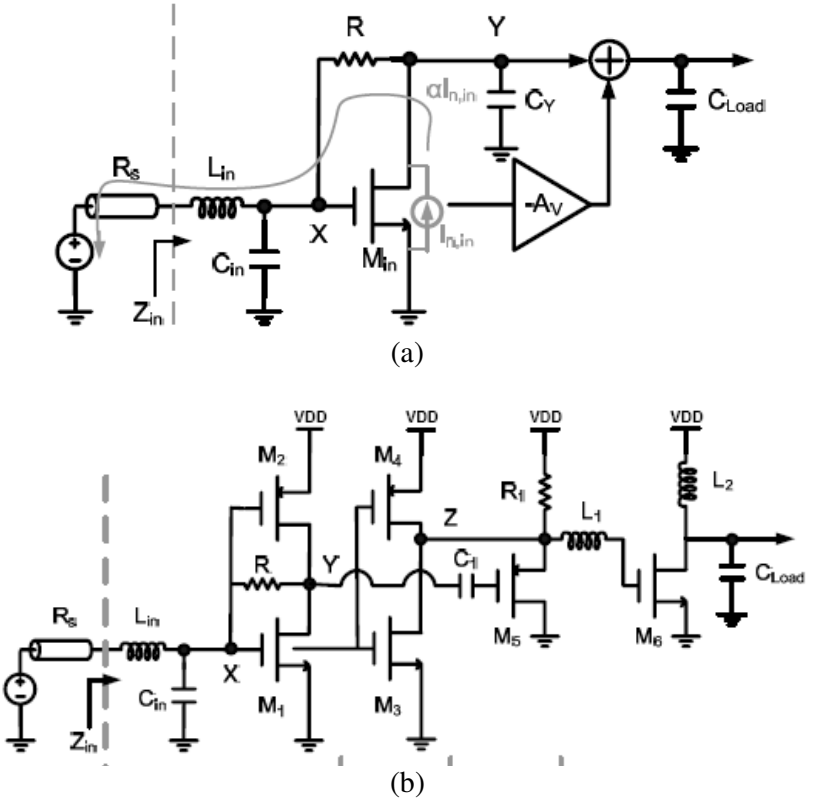


Fig. IV-2. Noise cancelling basis has for a CS stage: Representative diagram (b) Practical circuit(a) [42]

bias regimes gm" can be rejected. The bias value at which g'' is zero, is called *Linearity Sweet Point* [7]. g'_m causes the second order nonlinearity. Although g'_m has not sweet point, it can be eliminated using some techniques. The most popular technique is using differential circuits, in which second order terms appear as common mode signals and hence highly rejected in the differential outputs. The other technique is using Inverter Type Amplifiers, in which NMOS and PMOS transistor pair in CS configuration yields very good second order linearity [50].

In narrowband circuits, second order terms fall out of circuits operating band and hence are not important. However in broadband circuits in which noise cancelling or linearity improvement techniques are used, the second order terms appear as extra third order terms in output [7].

Third order nonlinearity effects can be improvement using some techniques. In [3] a simple method has been presented to improve the linearity of a cascode stage. The third order terms in the drain current of a cascode stage can be absorbed by a PMOS transistor. This technique has been addressed in [51] to improve the IIP3 of a cascode LNA. Active post distortion has been developed in [52] to improve the LNA linearity.

IV.1.3 Other Issues in CMOS LNA Design

IV.1.3.1 Feedback in CMOS LNA Circuits

Feedback techniques can be used in circuits in which the active devices poles are in frequencies well above the feedback loop bandwidth. With increasing f_T of MOS transistors in recent years, it has been possible to use feedback in high frequency LNA circuits [53]. Feedback loop is useful in wideband matching of CS stages [17]. In [18] resistive feedback has been used in deign of cascode multi-band LNA for multi standard transceivers. In [54] RLC feedback has been used in wideband matching of a cascode stage.

Feedback techniques are often adopted in designing low-noise amplifiers in order to shift the optimum noise impedance to the desired point [55]. Feedback reduces the nonlinearity of the circuit and improves IIP3[1] point [48]. Various feedback techniques has been investigated and compared in [56].

IV.1.3.2 Electrostatic Discharge Protection

Due to high input impedance and low gate breakdown voltage in the CMOS circuits, ESD[2] protection in the I/O pads is an important issue in these circuits. In RF circuits, the trend is to use simple ESD protection circuits, to prevent the performance degradation. In the frequencies above 5 GHz, tow diodes are conventionally used between the signal line and GND and the signal line and DC power line [57], [58]. However in some works SCR based ESD protection, beside LC circuits have been used successfully in up to 18 GHz [25], [59].

IV.1.3.3 Power Dissipation and Chip Area

To reduce the LNA power dissipation, special cares should be done in circuit configuration and design steps. Current reuse is one the successful techniques in reducing DC power of integrated circuits. This technique has been widely used in low power RF designs to reduce DC power consumption. [43]. As an example, in [60] a CS stage followed by a cascode stage has been designed in current reuse configuration.

LNA with CMOS transistors in sub-threshold regime is useful in very low power applications [61]. However, by this way the transistors gm is very low and hence can not be

[1] Third order Input Intercept Point
[2] Electrostatic Discharge

used in very high frequencies, in which increased losses in different parts of circuit necessitates high gm for transistors.

The trans-conductance of CMOS transistors decreases with decreasing the drain current. In some cases gm-boosting techniques are used to increase total gm, without increasing drain current [1] [62].

Using active load (PMOS transistor) in drain of NMOS transistor of LNA, high load resistance is obtained, without high DC power dissipation in load resistance [25]. However, parasitic capacitances in the output node in conjunction with high load resistance, limits the maximum frequency. For example, due to this problem, the unity gain of a resistive-load differential pair in 90 nm CMOS technology is limited to 15 GHz [63]. To solve this problem, inductive load is used for absorb the parasitic capacitance. Passive inductors have low Q in CMOS technologies and not only add many difficulties to circuit design process, but also need increase the chip area. To overcome this problems, active inductors are used instead of passive inductors, to obtain very small high-Q inductors [64]. Using active inductor, an LNA has been designed in chip area as small as 0.034 mm^2 [57]. The main problem with active inductors is their limited frequency. Inductor-less LNA has been reported in [7] and in [65] up to 10 GHz.

Using lumped elements, instead of distributed elements leads to smaller chip area. The different aspects of lumped elements versus distributed elements have been compared in [66] and [21].

IV.1.4 CMOS LNA Design and Optimization Principles

Various techniques have been adopted for CMOS LNA design and optimization. Some classified and well known techniques have been reviewed and explained in [55]. The Classical Noise Matching (CNM) technique was reported in [67]. In this technique, the LNA is designed for minimum NF by creating the optimum noise impedance to the given amplifier, which is typically implemented by adding a matching circuit between the source and input of the amplifier. By using this technique, the LNA can be designed to achieve an NF equal to NF_{min} of the transistor, the lowest NF that can be obtained with the given technology. However optimum noise impedance has considerable difference with optimum power gain impedance (complex conjugate matching) and hence the amplifier can experience a significant gain mismatch at the input. Therefore, the CNM technique typically requires compromise between the gain and noise performance.

Simultaneous Noise and Input Matching (SNIM) is obtained using series feedback, without degradation of the NF [55], [12]. The series feedback with inductive source degeneration, which is applied to the common-source or cascode topology, is especially widely used for narrow-band applications [12]. Inductive source degeneration facilitates the simultaneous noise and impedance matching, without degradation of NF_{min} and R_n [30].

Power Constrained Noise Optimization (PCNO) is used for noise optimization, for a given DC power dissipation. The drawback of this method is as CNM, by which the power gain is scarified. Specially in low power designs the power gain degradation is crucial. To overcome this problem, Power Constrained Simultaneous Noise and Input Matching (PCSNIM) technique was addressed [55]. Using this technique, SNIM condition is held for a given DC power.

As we mentioned previously, SNIM is potentially achievable in CMOS technologies. However the problem is a proper optimization method to obtain SNIM for a given DC power dissipation. The PCSNIM technique developed in [55] is an analytic optimization and has been derived using very simple transistor model. This simple model is useful in frequencies up to few GHz, but losses its accuracy for higher frequencies.

In [68] a multi-step simulation based process has been used in optimization of inductively source degenerated cascode LNA. In first step using simulation, F_{min} and noise equivalent resistance (R_n) of cascode stage, without degenerating inductor is calculated for various transistor widths, keeping the DC power dissipation constant. By this way optimum transistor width is determined. Then feedback inductance and matching network is calculated to obtain minimum noise figure, with given DC power. Graphical optimization of a CG LNA has been addressed in [69] and in [70], an LNA design flowchart has been presented, considering linearity performances.

IV.1.5 CMOS LNA in Millimeter Wave Frequencies

IV.1.5.1 CMOS LNA in V-band

In recent years, many mm-wave transceiver sub-circuits have been reported in CMOS technology. Recently published mm-wave LNAs in CMOS technology have been tabulated in Table IV-1. Like old RF LNAs, cascode topology has preserved its excellence in mm-wave frequency range. Cascode stage has been widely used in technologies other than CMOS [71], [72] [73]. Nevertheless, other circuit configurations like CS and CG topologies have been tried in this context [74], [75].

Razavi reported a CG LNA in 60 GHz, in 0.13 um CMOS technology in 2006 [75]. He claimed that cascode stage has difficulties in mm-wave range, due to its pole in the common node that is in order of $f_T/2$. This pole shunts degrades the cascode gain and noise performance in mm-wave frequency. He also investigated that conventional CG stage is not suitable for mm-wave range, due to the capacitive part of the transistor input impedance. Finally he proposed a modified CG configuration, as shown in Fig. IV-3(a). He used an inductor, instead of the CG stage current source, to compensate the capacitive term of the input impedance. By this way the contribution of the current source of CG stage is also eliminated.

Cascode stage again was introduced in mm-wave range by Terry Yao et al. in 2006 [23]. They used a small series inductor in drain of lower transistor, to tune up the cascode pole. This technique was used in earlier generations of RF CMOS [227].

TABLE IV-1
Recently published mm-wave LNAs in CMOS technology

Ref.	Topology	Technology (CMOS)	Freq. (GHz)	Power (mW)	IP_{1dB} (dBm)	IIP3 (dBm)	Gain (dB)	NF	Area (mm^2)	Year
[76]	3-stage Cascode	130 nm	51-65	54	-18 (in)	NA	14.6	8.8	1.3	2005
[22]	3-stage Cascode	130 nm	50-58	72	-23	NA	24.7	7.1	0.46	2006
[77]	2-stage Cascode	90 nm	62	10.5	NA	NA	12.2	6*	0.53	2006
[23]	2-stage Cascode	90 nm	58	24	NA	-6.8	14.6	4.5*	0.14	2006
[78]	2-stage Cascode	90 nm	60	24	NA	NA	12	5.5	0.2	2007
[79]	2-stage Cascode	90 nm	58	24	NA	NA	14.6	4.5*	0.52	2007
[80]	2-stage Cascode	65 nm	60	34*	NA	NA	12.5*	7.3*	0.4*	2007
[81]	2-stage Cascode	90 nm	64	86/48	NA	NA	15.5 /13.5	6.5 /6.7	0.14	2007
[74]	3-stage C.S.	130 nm	65-72	5.4	-17	NA	10.9	5.1*	0.38	2007

* Simulation Results

The modified cascode stage has been shown in Fig. IV-3(b). The modified cascode has superior performance and has been used in the last reported mm-wave LNA by Parsa and Razavi [82]. Nevertheless, standard cascode stage is used yet in CMOS mm-wave LNA design [80].

Performance of CMOS technology in mm-wave band is well comparable with InP-based HEMT, HBT and SiGe technologies. Still the chip size of fabricated LNA in CMOS technology is very smaller than other technologies [22], [23].

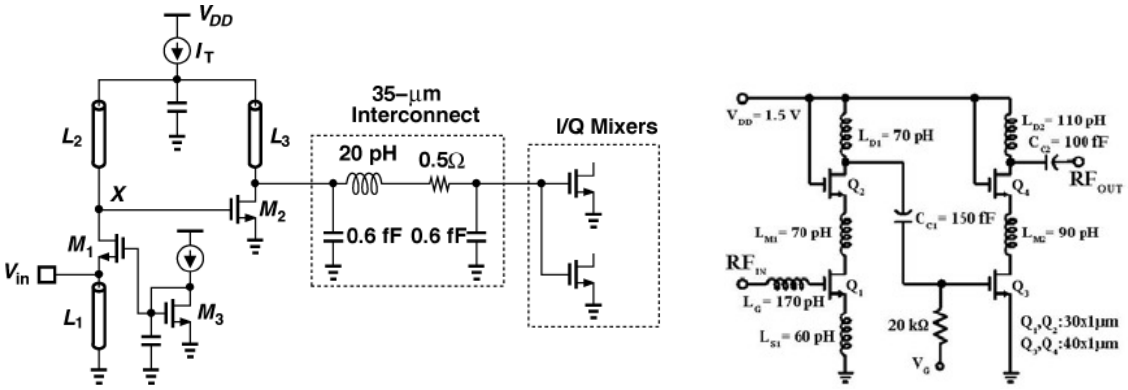
IV.1.5.2 CMOS LNA in Q-band (Ka-band)

In spite of reported V-band LNA's in the last section, where cascode stage was dominantly used by the designers, the reported works in around 30 GHz band shows that CS stage has been considered in many woks. In [83] two LNA's, one in 20 GHz, using a single stage CS, and another in 40 GHz using two CS stages have been reported. Two stage CS LNA with degenerating inductors has been reported in [84] in 24 GHz. A 3-stage CS LNA in 40 GHz band has been reported in [85]. In [86] two cascode stages has been used in design of a 31-34 GHz LNA. In this work shunt inductors have been added to the cascode node, to absorb the parasitic capacitance at this node and to eliminate the cascode second pole, the main drawback of cascode stage in mm-wave design [87], [23]. The second pole of a cascode stage depends on the gain of cascode (upper) transistor and the total capacitance at the cascode common node and is calculated as [86]:

$$\omega_p \approx \frac{g_{m2}}{C_{ds1} + C_{gd1} + C_{gs2} + C_{ds2}} \tag{IV-3}$$

Another way to overcome this drawback of cascode stage has been addressed in [88], by placing an inductor in the gate of upper transistor. By this way very low power 26 GHz LNA has been designed.

Combination of CS and cascode stage is useful in mm-wave LNA design. It has been investigated that CS configuration in the first stage and cascode configuration in the second stage incorporates good noise performance of CS stage and high gain of cascode stage [89], [87]. A summary of recently published Q and Ka band CMOS LNA's have been listed in Table IV-2.



(a) (b)

Fig. IV-3 (a) CG stage used in 60 GHz LNA [75] and (b) 60 GHz LNA with modified cascode stage [23].

IV.2 Our LNA Circuit and its Analysis

As mentioned in section IV.1.5.2, the best topology for a two stage LNA is CS in the first stage and cascode in the second stage. The reason is that cascode stage has poor noise figure in mm-wave band, due to capacitances and parasitic admittances in the cascode node, but has good gain and excellent reverse isolation. Consequently, CS-Cascode topology integrates good noise performance of CS stage, with excellent reverse isolation. However, two stage LNA has high DC power consumption and hence is not suitable for our work, in which low power design is an essential goal. So we have chosen the single stage cascode topology for our LNA, as in Fig. IV-4. Output matching is performed using standard T network [90] and various input matching will be discussed later. The degenerating inductor may be neglected in Fig. IV-4(b), however it is necessary if high linearity is required.

The analysis of the cascode LNA is presented in this section. This analysis is used in development of analytic input and output matching. Then the results will be used in the next section, in analytic design and optimization of LNA.

IV.2.1 LNA Analysis

The small signal model of the cascode LNA in Fig. IV-4 has been shown in Fig. IV-5. Based on this circuit, we will derive equations to calculate the performance characteristics of the LNA.

IV.2.1.1 Input Impedance Analysis

A) Conventional Methods

A simple equation is conventionally used for calculation of the input impedance of (Z_{ingL}) of this equivalent circuit is as follows [13]:

$$Z_{ingL} = j\omega L_s + \frac{1}{j\omega C_{gsL}} + \frac{g_m}{C_{gsL}} L_s + R_g \qquad \text{(IV-4)}$$

TABLE IV-2
Recently published Q and Ka band CMOS LNAs

Ref.	Topology	Technology (CMOS)	Freq. (GHz)	Power (mW)	OP_{1dB} (dBm)	IIP3 (dBm)	Gain (dB)	NF	Area (mm^2)	Year
[86]	2-stage Cascode	90 nm	31-34	10	NA	NA	18.6	3	0.86	2006

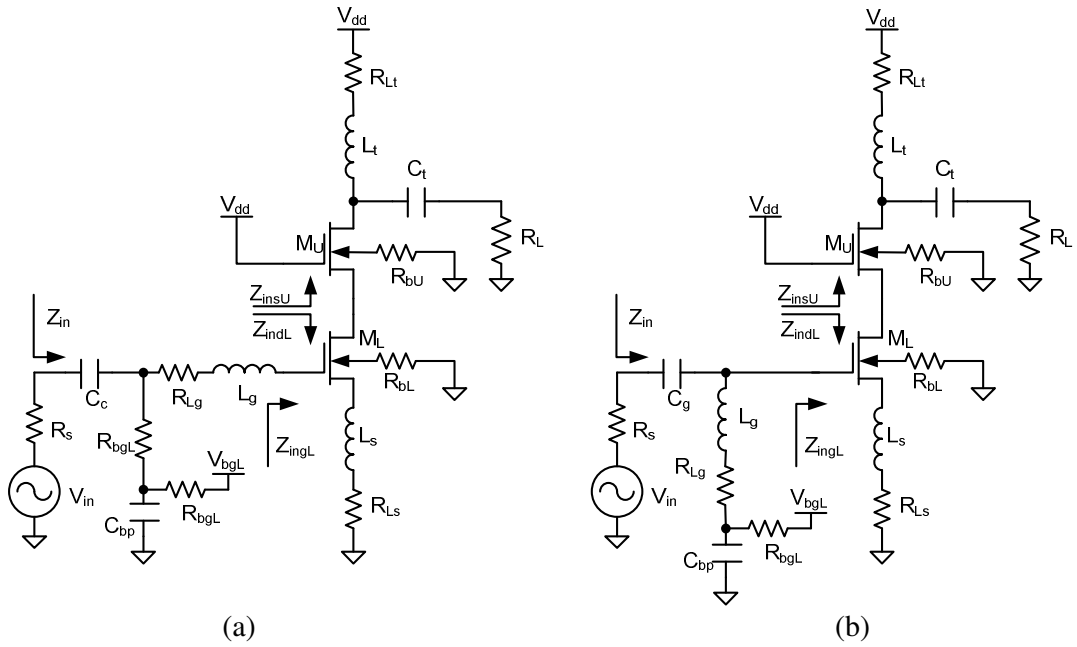


Fig. IV-4. Schematic of our single stage cascode LNA, input matching with serial (a) and parallel (b) inductor in the gate of input transistor.

L_s is the degenerating inductor in the source and R_g is the gate resistance of lower transistor. This simple equation neglects C_{gd} feedback capacitance and drain-source conductance, g_{ds}. In contrast of its simplicity, it has been used in many old and recent works, since can give a good sense about the effect of degenerating inductance or other feed backs in the drain current path [94], [55], [9]. Using this simple equation, one can design the input matching network of cascode or common source LNA. The conventional equation can be used in frequencies up to few GHz.

Scaling down the CMOS technologies, the drain-source conductance increases and gate-drain capacitance becomes well comparable with gate-source capacitances. Consequently, the simple equation of (IV-4) loss its accuracy in mm-wave circuits in modern CMOS technologies. In [95] and [96] an accurate equation has been presented to calculate the input impedance to a CS or cascode stage:

$$Z_{ingL} = \left(\frac{1}{j\omega C_{gsL}} + \frac{L_s \gamma \cdot g_{mL}}{C_{gsL}} \right) \left(1 + \frac{C_{gdL}}{C_{gsL}} \left(1 + \gamma \cdot g_{mL} Z_d \right) \right)^{-1} + R_g \qquad \text{(IV-5)}$$

Where:

$$\gamma = \frac{R_{dsL}}{R_{dsL} + Z_d + j\omega L_s}$$

And Z_d (or Y_d) is the total load impedance (or admittance) for the drain of CS transistor.

B) Our equation: method 1

Although equation (IV-5) calculates the input impedance accurately, it is not suitable for input matching process. Consequently we have rewritten it with some modifications. To calculate Z_{ingL} in (IV-5), first Z_{insU} should be calculated (see the LNA of Fig. IV-4(a)). On the other hand, to calculate Z_{insU} the values of output matching network are necessary. This is the philosophy of *simultaneous input and output matching* [97]. However, in this step we do not have them. This problem is due to the fact that in high frequencies the reverse isolations of the

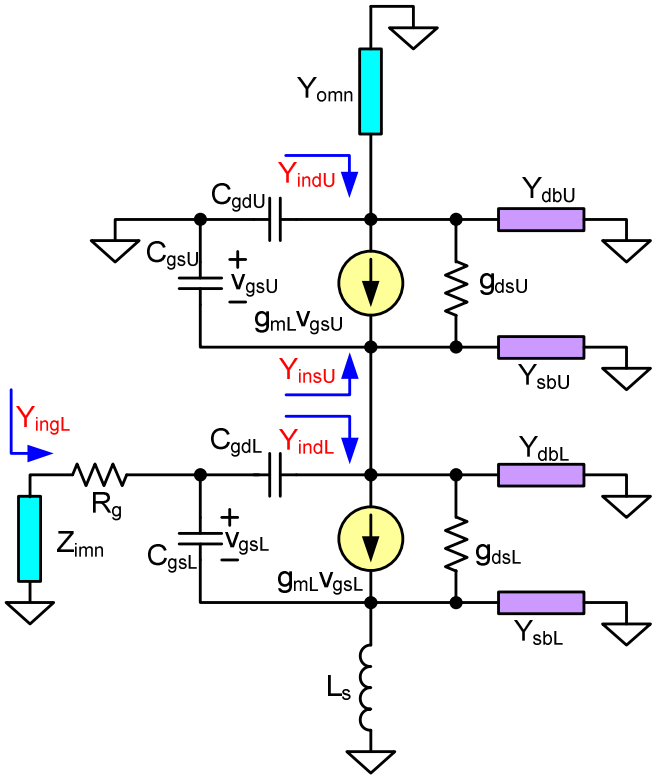


Fig. IV-5. Small signal model of the cascode LNA, with (a) and without (b) degenerating inductance. Subscribes U and L denotes for Upper and Lower transistors, respectively.

circuit is limited. In the second step of our design we will use optimization techniques to perform simultaneous input and output matching. But in the first step we use an approximation. The admittance into the source of upper transistor is calculated as:

$$Y_{insU} = Y_{sbU} + j\omega C_{gsU} + \frac{(g_{mU} + g_{dsU})(y_{ddU} - g_{dsU})}{y_{ddU}} \tag{IV-5}$$

in which:

$$y_{ddU} = j\omega C_{gdU} + Y_{dU} + Y_{dbU} + g_{dsU}$$

However for simplicity, we assume that all of capacitances at the output node completely absorbed by the inductor in the output matching network (L_t in Fig. IV-4). Also we assume that the resistive component of the input impedance to the drain of upper transistor (Z_{indU} in Fig. IV-5) is almost equal to g_{dsU}. With these assumptions the total load of lower transistor is obtained as:

$$Y_d = \frac{g_{mU} + g_{dsU}}{2} + j\omega C_{gsU} + Y_{sbU} \tag{IV-6}$$

Now for simplicity, we define:

$$Y_d = G_d + jB_d$$

$$B_s = \frac{-1}{\omega L_s\left(1 + 1/Q^2\right)} + B_{sbL} \tag{IV-7}$$

And we normalize all admittances to ωC_{gs}:

$$Y_{dN}=\frac{Y_d}{\omega C_{gsL}} \quad , \quad B_{sN}=\frac{B_s}{\omega C_{gsL}} \quad , \quad \mu=\frac{C_{gdL}}{C_{gsL}} \quad , \quad \eta=\frac{g_{dsL}}{g_{mL}} \quad , \omega_\tau=\frac{g_{mL}}{C_{gsL}} \tag{IV-8}$$

After tedious, but straightforward calculations the real and imaginary parts of the input impedance is calculated as:

$$R_{ingL}=\frac{1}{\omega C_{gs}}\frac{a_1B_{sN}^2+a_2B_{sN}}{b_1B_{sN}^2+b_2B_{sN}+b_3}+R_g$$

$$X_{ingL}=\frac{1}{\omega C_{gs}}\frac{c_1B_{sN}^2+c_2B_{sN}+c_3}{b_1B_{sN}^2+b_2B_{sN}+b_3} \tag{IV-9}$$

Where the coefficients a_i, b_i and c_i are calculated as:

$$a_1=\mu\frac{\omega_\tau}{\omega}B_{dN}$$

$$a_2=-\frac{\omega_\tau}{\omega}\left(G_{dN}\frac{\omega_\tau}{\omega}(\eta+\mu+2\eta\mu)+(1+\mu)(G_{dN}^2+B_{dN}^2)\right)$$

$$b_1=(1+\mu)^2(G_{dN}^2+B_{dN}^2)+\frac{\omega_\tau}{\omega}(\eta+\mu\eta+\mu)\left(\frac{\omega_\tau}{\omega}(\eta+\mu\eta+\mu)+2G_{dN}(1+\mu)\right)$$

$$b_2=2\frac{\omega_\tau^2}{\omega^2}(\eta+\mu\eta+\mu)\eta(\mu+1)B_{dN}$$

$$b_3=\eta^2\frac{\omega_\tau^2}{\omega^2}(\mu+1)^2(G_{dN}^2+B_{dN}^2)$$

$$c_1=-(1+\mu)(B_{dN}^2+G_{dN}^2)-\frac{\omega_\tau}{\omega}\left(G_{dN}+\eta\frac{\omega_\tau}{\omega}\right)(\eta+\mu\eta+\mu)-\eta\frac{\omega_\tau}{\omega}G_{dN}(1+\mu)$$

$$c_2=-\frac{\omega_\tau^2}{\omega^2}B_{dN}\left(2\eta^2(\mu+1)+\eta+2\mu\eta+\mu\right)$$

$$c_3=-\frac{\omega_\tau^2}{\omega^2}(\eta+1)(\mu+1)\eta(B_{dN}^2+G_{dN}^2)$$

C) Our equation: method 2

Although the input impedance equation of (IV-5) is the most accurate reported, it is possible to derive more accurate equation. For this purpose, considering Fig. IV-5(b) we define:

$$g_{dd}+jb_{dd}=g_{dsL}+Y_d+Y_{dbL}+j\omega C_{gdL} \tag{IV-10}$$

Where Y_d has been defined in (IV-9) and Y_{dbL} is the admittance from lower transistor drain into the substrate. Now using the notation in (IV-8), and after some simplifications, we obtain a matrix equation for the small signal equivalent circuit of Fig. IV-5(b):

$$\begin{bmatrix}I_g\\I_s\end{bmatrix}=\frac{\omega C_{gsL}}{g_{ddN}+jb_{ddN}}\times\begin{bmatrix}j(1+\mu)(g_{ddN}+jb_{ddN})+j\mu\frac{\omega_\tau}{\omega} & -j(g_{ddN}+jb_{ddN})-j\mu\frac{\omega_\tau}{\omega}\\ -\left(j+\frac{\omega_\tau}{\omega}\right)(g_{ddN}+jb_{ddN})+\eta\frac{\omega_\tau^2}{\omega^2} & \left(jB_{sLN}+j+\frac{\omega_\tau}{\omega}\right)(g_{ddN}+jb_{ddN})-\eta\frac{\omega_\tau^2}{\omega^2}\end{bmatrix}\begin{bmatrix}V_g\\V_s\end{bmatrix} \tag{IV-11}$$

Again after tedious calculations we obtain the equations to calculate the real and imaginary parts of the input impedance to the gate of lower transistor:

$$R_{ingL} = \frac{1}{\omega C_{gs}} \frac{a_1 B_{sN}^2 + a_2 B_{sN}}{b_1 B_{sN}^2 + b_2 B_{sN} + b_3} + R_g$$

$$X_{ingL} = \frac{1}{\omega C_{gs}} \frac{c_1 B_{sN}^2 + c_2 B_{sN} + c_3}{b_1 B_{sN}^2 + b_2 B_{sN} + b_3} \qquad \text{(IV-12)}$$

for which the related coefficients a_i, b_i and c_i are calculated as:

$$a_1 = \mu \frac{\omega_\tau}{\omega} b_{ddN}$$

$$a_2 = \frac{\omega_\tau}{\omega}\left(-\left(b_{ddN}^2 + g_{ddN}^2\right) + g_{ddN} \frac{\omega_\tau}{\omega}(\eta - \mu) + \mu\left(b_{ddN} + \eta \frac{\omega_\tau^2}{\omega^2} \right)\right)$$

$$b_1 = (1+\mu)^2\left(g_{ddN}^2 + b_{ddN}^2\right) + \mu \frac{\omega_\tau}{\omega}\left(\mu \frac{\omega_\tau}{\omega} + 2(1+\mu) g_{ddN} \right)$$

$$b_2 = 2\mu(1+\mu)\left(g_{ddN}^2 + b_{ddN}^2\right) + 2\mu \frac{\omega_\tau}{\omega}\left(\mu g_{ddN} + b_{ddN} \frac{\omega_\tau}{\omega}(\eta + \mu\eta + \mu) \right)$$

$$b_3 = \mu^2\left(g_{ddN}^2 + b_{ddN}^2\right)\left(1 + \frac{\omega_\tau^2}{\omega^2}\right) + \mu^2\eta^2 \frac{\omega_\tau^4}{\omega^4} + 2\eta\mu^2 \frac{\omega_\tau^2}{\omega^2}\left(- g_{ddN} \frac{\omega_\tau}{\omega} + b_{ddN} \right)$$

$$c_1 = -(1+\mu)\left(g_{ddN}^2 + b_{ddN}^2\right) - \mu \frac{\omega_\tau}{\omega} g_{ddN}$$

$$c_2 = -(1+2\mu)\left(g_{ddN}^2 + b_{ddN}^2\right) - \mu \frac{\omega_\tau}{\omega} g_{ddN} - \frac{\omega_\tau^2}{\omega^2} b_{ddN}(\mu + \eta + 2\mu\eta)$$

$$c_3 = -\mu\left(1 + \frac{\omega_\tau^2}{\omega^2}\right)\left(g_{ddN}^2 + b_{ddN}^2\right) + 2\eta\mu \frac{\omega_\tau^2}{\omega^2}\left(- b_{ddN} + g_{ddN} \frac{\omega_\tau}{\omega} \right) - \eta^2 \mu \frac{\omega_\tau^4}{\omega^4}$$

IV.2.1.2 Our Input Matching Method

We have developed separate matching methods for each of the input matching circuits of Fig. IV-4(a), in which a series inductor has been used in the gate, and Fig. IV-4(b), in which a parallel inductor and a series capacitor have been used for input matching. The importance of analytic equations to calculate matching elements is simplification of LNA design and optimization. In the optimization process, provided that they have sufficient accuracy, the analytic equations lead to reduction of some optimization variables.

A) Matching Using a Series Inductor in the Gate

For conjugate matching of the LNA in Fig. IV-4(a) we must have:

$$\begin{cases} R_s = R_{Lg} + R_{ingL} \\ \omega L_g = -X_{ingL} \end{cases} \qquad \text{(IV-13)}$$

L_g is the matching inductor in the gate and R_{Lg} is calculated from:

$$R_{Lg} = \frac{\omega L_g}{Q_g} \qquad \text{(IV-14)}$$

in which Q_g is the inductor quality factor. Now from (IV-10) to (IV-11) we obtain the analytic matching design equations:

$$AB_{sN}^2 + BB_{sN} + C = 0 \tag{IV-15}$$

in which:

$$A = \omega C_{gs}\left(R_s - R_g\right)b_1 + \frac{c_1}{Q_g} - \frac{\omega_\tau}{\omega}a_1$$

$$B = \omega C_{gs}\left(R_s - R_g\right)b_2 + \frac{c_2}{Q_g} - \frac{\omega_\tau}{\omega}a_2$$

$$C = \omega C_{gs}\left(R_s - R_g\right)b_3 + \frac{c_3}{Q_g}$$

The coefficients a_i, b_i and c_i are calculated from (IV-9) or (IV-12). After calculating B_{sN} from (IV-15), the source degenerating inductor is calculated using (IV-7) and (IV-8). Then the gate matching inductor is calculated from (IV-13), in conjunction with (IV-9) or (IV-12).

B) Matching Using a Parallel Inductor in the Gate

Input matching using series inductor in gate has some limitations in mm-wave frequencies. By this method, the degenerating inductor value does not have any freedom. Although in some cases this inductor is necessary to improve the LNA linearity, it has designed as small as possible, to avoid power gain degradation. The other problem is that series inductor in the gate is not suitable for transmission line inductors. Because it is easier to use this type of inductors in shorted-end configuration, to simplify the inductor design process and to reduce the parasitic effects of the inductor [90]. Here we describe another way of input matching, as in Fig. IV-4(b).

In general the input matching of Fig. IV-4(b) can be explained as in Fig. IV-6(a). Considering this figure we deduce:

$$\begin{aligned} Z_{in} &= jX_m + \frac{1}{G_{ingL} + j\left(B_m + B_{ingL}\right)} \\ &= \frac{G_{ing}}{G_{ingL}^2 + \left(B_m + B_{ingL}\right)^2} + j\left(X_m - \frac{B_m + B_{ingL}}{G_{ingL}^2 + \left(B_m + B_{ingL}\right)^2}\right) \end{aligned} \tag{IV-16}$$

For conjugate matching we must have $Z_{in}^* = Rs$ and hence we deduce:

$$\begin{cases} if \quad R_s > \dfrac{G_{ingL}}{G_{ingL}^2 + B_{ingL}^2} \Rightarrow sign\left(B_m\right) = -sign\left(B_{ingL}\right) \\ if \quad R_s < \dfrac{G_{ingL}}{G_{ingL}^2 + B_{ingL}^2} \Rightarrow sign\left(B_m\right) = sign\left(B_{ingL}\right) \\ if \quad R_s > \dfrac{1}{G_{ingL}} \Rightarrow there \quad is \quad no \quad response \end{cases} \tag{IV-17}$$

In practice the resistive term of the input impedance to the gate of the lower transistor is smaller than Rs and hence the first condition of (IV-17) holds. On the other hand the input impedance to the gate of the lower transistor is capacitive. Consequently B_m is an inductive element. Although theoretically the sign of X_m may be positive or negative, based on our experience, X_m is almost capacitive. So we use the matching network of Fig. IV-6(b) in our design. Whenever the sign of X_m is positive, then the designer can use the equivalent inductor.

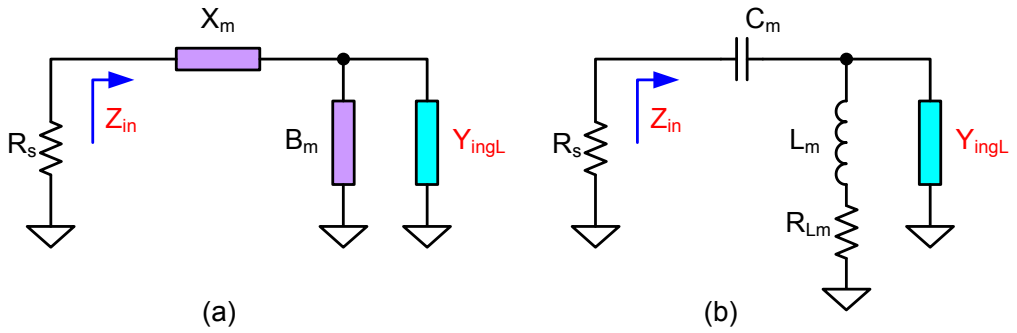


Fig. IV-6. General form of input matching using two matching elements in gate (a) and implementation with LC network (b)

From Fig. IV-6(b) we have:

$$Z_{in} = \frac{1}{j\omega C_m} + \frac{1}{\frac{1}{j\omega L_m + R_{Lm}} + G_{ing} + jB_{ing}} \tag{IV-18}$$

And using the definition of quality factor for the matching inductor we obtain:

$$Z_{in} = \frac{1}{j\omega C_m} + \frac{1}{\frac{1}{j\omega L_m + \frac{\omega L_m}{Q}} + G_{ing} + jB_{ing}} \tag{IV-19}$$

After simplification we deduce:

$$Z_{in} = \frac{1}{j\omega C_m} + \omega L_m \frac{Q + \omega L_m G_{ing}\left(Q^2+1\right) + j\left(Q^2 - \omega L_m B_{ing}\left(Q^2+1\right)\right)}{Q^2 + 2Q\left(G_{ing} - QB_{ing}\right)\omega L_m + \omega^2 L_m^2\left(1+Q^2\right)\left(G_{ing}^2 + B_{ing}^2\right)} \tag{IV-20}$$

For conjugate matching two below conditions must be complied:

$$\begin{cases} R_s = \omega L_m \dfrac{Q + \omega L_m G_{ing}\left(Q^2+1\right)}{Q^2 + 2Q\left(G_{ing} - QB_{ing}\right)\omega L_m + \omega^2 L_m^2\left(1+Q^2\right)\left(G_{ing}^2 + B_{ing}^2\right)} \\ \dfrac{1}{\omega C_m} = \omega L_m \dfrac{Q^2 - \omega L_m B_{ing}\left(Q^2+1\right)}{Q^2 + 2Q\left(G_{ing} - QB_{ing}\right)\omega L_m + \omega^2 L_m^2\left(1+Q^2\right)\left(G_{ing}^2 + B_{ing}^2\right)} \end{cases} \tag{IV-21}$$

Assuming that Q is independent of L, from first equation we derive a second order equation to calculate the matching inductor:

$$A\omega^2 L_m^2 + B\omega L_m + C = 0 \tag{IV-22}$$

where:

$$\begin{aligned} A &= \left(Q^2+1\right)\left(G_{ing} - \left(G_{ing}^2 + B_{ing}^2\right)R_s\right) \\ B &= Q\left(1 - 2\left(G_{ing} - QB_{ing}\right)R_s\right) \\ C &= -Q^2 R_s \end{aligned} \tag{IV-23}$$

So we can simply calculate the matching inductor:

$$\omega L_m = \frac{-B \pm \sqrt{B^2 - 4A \cdot C}}{2A} \tag{IV-24}$$

After calculating L_m we can calculate C_m from (IV-21):

$$\omega^2 C_m L_m = \frac{Q^2 + 2Q\left(G_{ing} - QB_{ing}\right)\omega L_m + \omega^2 L_m^2\left(1+Q^2\right)\left(G_{ing}^2 + B_{ing}^2\right)}{Q^2 - \omega L_m B_{ing}\left(Q^2+1\right)} \tag{IV-25}$$

Please remind that in this case we have freedom in choosing degenerating inductor, since the matching process is valid for each value of L_s. So we can calculate L_s as small as possible to comply the linearity requirement, with minimum power gain degradation. It must be noted that in the above equations, we need to calculate the substrate admittances. The substrate admittances are layout-dependent and hence can not be calculated before laying out the transistors. However in this step, the designer can calculate them based on his/her experience, using the substrate model in Chapter II, or may simply replace it with the drain and source junction capacitances.

IV.2.1.3 Output matching Analysis

For output matching we use the standard T network, as in Fig. IV-7 (a). From this figure, to perform the output matching, we must calculate the input impedance to the drain of upper transistor (Z_{indU} in Fig. IV-5). Using Fig. IV-7 (b) we deduce:

$$\begin{aligned} Y_{indU} = Y_{dbU} &+ \frac{-\left(g_{mU} + g_{dsU}\right)\left(C_{gsU}\, g_{dsU} + C_{gdU}\, y_{ssU}\right)}{y_{ssU}\, C_{gsU}} \\ &+ \left(j\omega C_{gdU} + g_{dsU}\right) + \left(g_{mU} + g_{dsU}\right)\frac{C_{gdU}}{C_{gsU}} \end{aligned} \tag{IV-25}$$

where:

$$y_{ssU} = Y_{sU} + Y_{sbU} + j\omega C_{gsU} + g_{mU} + g_{dsU}$$

and Y_{sU} is the load at the source of upper transistor, equal to the sum of substrate admittance at this node (Y_{bC} in Fig. IV-5) and the input admittance to the drain of lower transistor (Y_{indL} in Fig. IV-5).

Using Fig. IV-7 (c), the input admittance to the drain of lower transistor is calculated as:

$$\begin{aligned} Y_{indL} = Y_{dbL} &+ \frac{j\omega\left(C_{gsL}\, g_{dsL} + C_{gdL}\, y_{ssL}\right)}{j\omega C_{gsL}\left(-j\omega C_{gsL} - g_{mL}\right) + y_{ssL}\, y_{ggL}}\left(-j\omega C_{gdL} + g_{mL} - \frac{\left(g_{mL} + g_{dsL}\right) y_{ggL}}{j\omega C_{gsL}}\right) \\ &+ \left(j\omega C_{gdL} + g_{dsL}\right) + \left(g_{mL} + g_{dsL}\right)\frac{C_{gdL}}{C_{gsL}} \end{aligned} \tag{IV-26}$$

where:

$$y_{ssL} = Y_{sL} + Y_{sbL} + j\omega C_{gsL} + g_{mL} + g_{dsL}$$

$$y_{ggL} = \frac{Y_{gL}}{1 + R_g Y_{gL}} + j\omega C_{gdL} + j\omega C_{gsL}$$

Y_{gL} is the input admittance to the input matching network, seen from the gate of lower transistor, and Y_{sL} is the load at the source of lower transistor, equal to the sum of substrate admittance at this node (Y_{bS} in Fig. IV-5) and the degenerating admittance of the source.

Now we can calculate the output matching network elements. Using Fig. IV-6(b) the output impedance of LNA is calculated as:

$$Z_{out} = \frac{1}{j\omega C_t} + \omega L_t \frac{Q + \omega L_t G_{indU}\left(Q^2+1\right) + j\left(Q^2 - \omega L_t B_{indU}\left(Q^2+1\right)\right)}{Q^2 + 2Q\left(G_{indU} - QB_{indU}\right)\omega L_t + \omega^2 L_t^2\left(1+Q^2\right)\left(G_{indU}^2 + B_{indU}^2\right)} \tag{IV-27}$$

Where Q is the quality factor of L_t. For conjugate matching two below conditions must be complied:

$$\begin{cases} R_{load} = \omega L_t \dfrac{Q + \omega L_t G_{indU}\left(Q^2+1\right)}{Q^2 + 2Q\left(G_{indU} - QB_{indU}\right)\omega L_t + \omega^2 L_t^2\left(1+Q^2\right)\left(G_{indU}^2 + B_{indU}^2\right)} \\ \dfrac{1}{\omega C_t} = \omega L_t \dfrac{Q^2 - \omega L_t B_{indU}\left(Q^2+1\right)}{Q^2 + 2Q\left(G_{indU} - QB_{indU}\right)\omega L_t + \omega^2 L_t^2\left(1+Q^2\right)\left(G_{indU}^2 + B_{indU}^2\right)} \end{cases} \quad \text{(IV-28)}$$

Assuming Q is independent of L, from first equation we obtain a second order equation to calculate L_t:

$$A\omega^2 L_t^2 + B\omega L_t + C = 0 \quad \text{(IV-29)}$$

in which:

$$\begin{aligned} A &= \left(Q^2+1\right)\left(G_{indU} - \left(G_{indU}^2 + B_{indU}^2\right)R_{load}\right) \\ B &= Q\left(1 - 2\left(G_{indU} - QB_{indU}\right)R_{load}\right) \\ C &= -Q^2 R_{load} \end{aligned} \quad \text{(IV-30)}$$

after solving the above equation we obtain:

$$\omega L_t = \frac{-B \pm \sqrt{B^2 - 4A \cdot C}}{2A} \quad \text{(IV-31)}$$

After calculating L_t, we can calculate C_t from (IV-28).

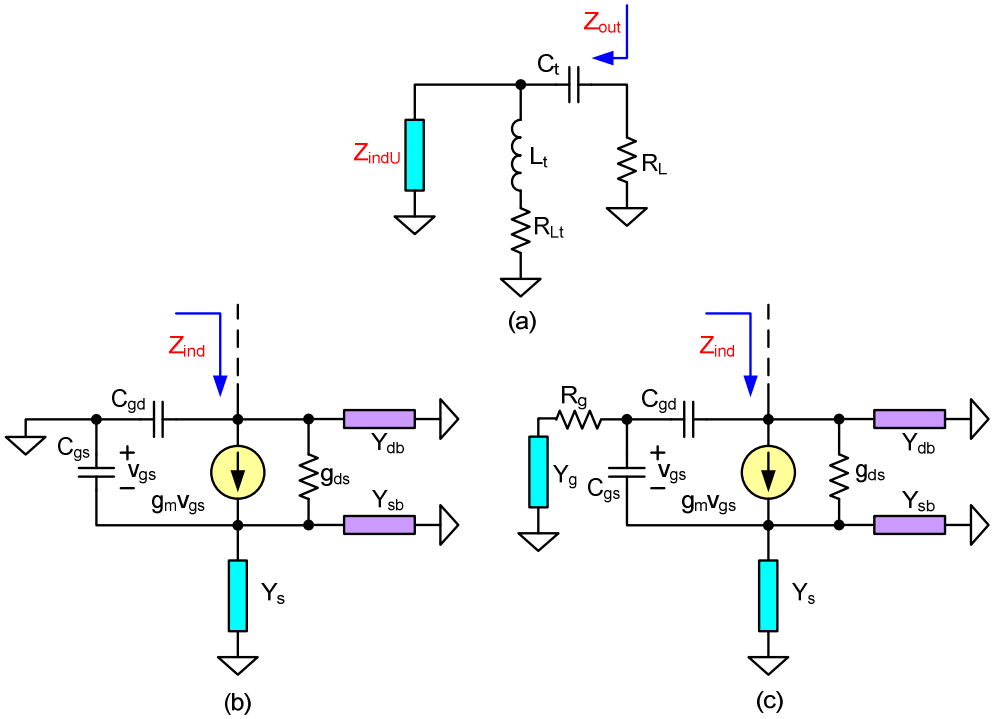


Fig. IV-7. The equivalent circuit to calculate the output matching network (a) and the equivalent circuit to calculate the input impedance to the drain of CG stage (b) and CS stage (c)

IV.2.1.4 Power Gain Analysis

Firstly we calculate the voltage gain of a single transistor common gate and common source stage. Then the results will be used for calculation of a cascode stage power gain, as well as noise analysis in the later issues.

A) Single Transistor Stage

The single transistor stage has been shown in Fig. IV-8. Using the small signal model of common source stage in Fig. IV-8(a) we can write two KCL equations:

$$\begin{cases} (g_m + j\omega C_{gs})(V_{gi} - V_s) + g_{ds}(V_d - V_s) - V_s(Y_s + Y_{sb}) = 0 \\ g_m(V_{gi} - V_s) + g_{ds}(V_d - V_s) + j\omega C_{gd}(V_d - V_{gi}) + V_d(Y_d + Y_{db}) = 0 \end{cases}$$

And after some calculations and defining:

$$y_{ss} = g_m + j\omega C_{gs} + g_{ds} + Y_s + Y_{sb}$$

$$y_{dd} = g_{ds} + j\omega C_{gd} + Y_d + Y_{db}$$

we deduce:

$$A_{dgi} = \frac{V_d}{V_{gi}} = \frac{(g_m + g_{ds})(g_m + j\omega C_{gs}) - y_{ss}(g_m - j\omega C_{gd})}{y_{ss} y_{dd} - g_{ds}(g_m + g_{ds})} \quad \text{(IV-32)}$$

Considering the effect of R_g in Fig. IV-7, we define another voltage gain:

$$A_{gig} = \frac{V_{gi}}{V_g} = 1 - Y_{ingL} R_g \quad \text{(IV-33)}$$

And finally:

$$A_{dg} = \frac{V_d}{V_g} = A_{dgi} A_{gig} \quad \text{(IV-34)}$$

And for the common gate stage of Fig. IV-8(a) we can write:

$$\begin{cases} j\omega C_{gs}(V_g - V_s) + j\omega C_{gd}(V_g - V_d) + V_g Y_g = 0 \\ g_m(V_g - V_s) + g_{ds}(V_d - V_s) + j\omega C_{gd}(V_d - V_g) + V_d(Y_d + Y_{db}) = 0 \end{cases} \quad \text{(IV-35)}$$

Consequently we deduce:

$$A_{ds} = \frac{V_d}{V_s} = \frac{y_{gg}(g_m + g_{ds}) + j\omega C_{gs}(j\omega C_{gd} - g_m)}{j\omega C_{gd}(g_m - j\omega C_{gd}) + y_{gg} y_{dd}} \quad \text{(IV-36)}$$

In which:

$$y_{gg} = j\omega C_{gs} + j\omega C_{gd} + \frac{Y_g}{1 + R_g Y_g}$$

$$y_{dd} = g_{ds} + j\omega C_{gd} + Y_d + Y_{db}$$

Y_g is equal to the admittance into the input matching network from gate side, Y_{imn}. If series inductor is used in input matching network (see Fig. IV-4 (a)), Y_{imn} is equal to:

$$Y_{imn} = \frac{1}{R_s + \omega L_g(j + 1/Q_{Lg})} \quad \text{(IV-37)}$$

And if parallel inductor is used in input matching network (see Fig. IV-4 (b)), Y_{imn} is equal to:

$$Y_{imn} = \frac{1}{\omega L_m(j + 1/Q_{Lm})} + \frac{1}{R_s + 1/j\omega C_m} \quad \text{(IV-38)}$$

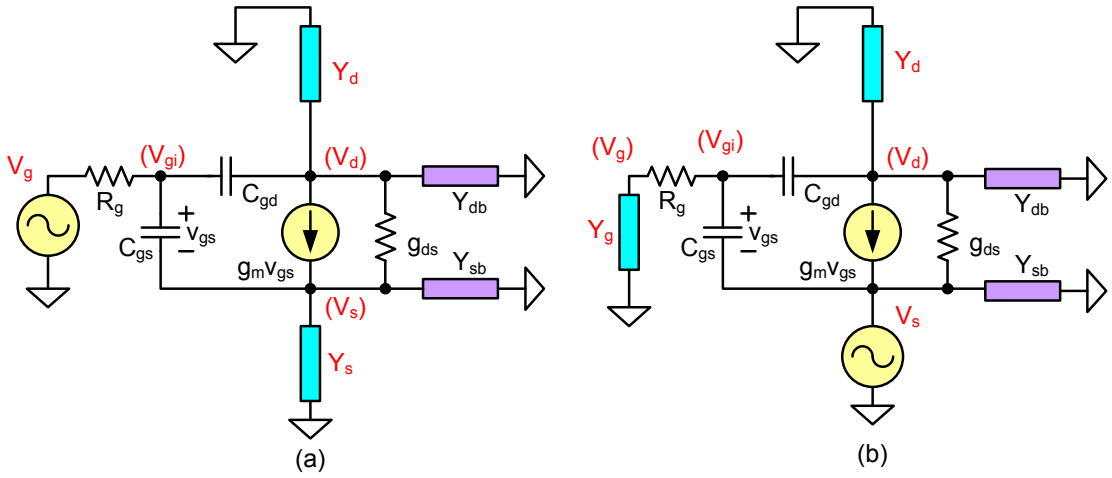


Fig. IV-8. Small signal model of common source (a) and common gate (b) stages

B) Single Stage Cascode LNA

For calculating the LNA power gain, the circuits in Fig. IV-9 have been used. Based on this figure we use a 5-step voltage transfer function to calculate the voltage gain and then the power gain.

Voltage transfer function from source to the circuit input is calculated as:

$$A_{sm} = \frac{V_{in}}{V_s} = \frac{Z_{in}}{Z_{in} + R_s} \tag{IV-39}$$

Voltage transfer function for the input matching network depends on the input matching network topology. For input matching with series inductor, as in Fig. IV-4(a), using Fig. IV-9(a) we obtain:

$$A_{imn} = \frac{V_{gL}}{V_s} = \frac{Z_{ingL}}{Z_{ingL} + \omega L_g\left(j + 1/Q_{Lg}\right)} \tag{IV-40}$$

Where Z_{ingL} is calculated from (IV-12) and Q_{Lg} is the quality factor of the matching inductor.

In the case of input matching of Fig. IV-4(b), using Fig. IV-9(b) we obtain:

$$A_{imn} = \frac{j\omega^2 C_m L_m\left(j + 1/Q_{Lm}\right)}{1 + \omega L_m\left(j + 1/Q_{Lm}\right)\left(j\omega C_m + Y_{ingL}\right)} \tag{IV-41}$$

Again Z_{ingL} is calculated from (IV-12).

To calculate the voltage transfer function for the lower transistor, we use Fig. IV-9(d). So we can use (IV-33) with the lower transistor parameters and after substituting:

$$Y_s = \frac{1}{\omega L_s\left(j + 1/Q_{Ls}\right)} \tag{IV-42}$$

$$Y_d = Y_{insU}$$

Voltage transfer function of the upper transistor is calculated using Fig. IV-9 (e). Considering that in the case of upper transistor gate node is grounded, from (IV-35) we obtain:

$$A_{dsU} = \frac{V_{dU}}{V_{sU}} = \frac{g_{mU} + g_{dsU}}{y_{ddU}} \tag{IV-43}$$

As in (IV-35), y_{dd} is calculated considering Fig. IV-9(e):

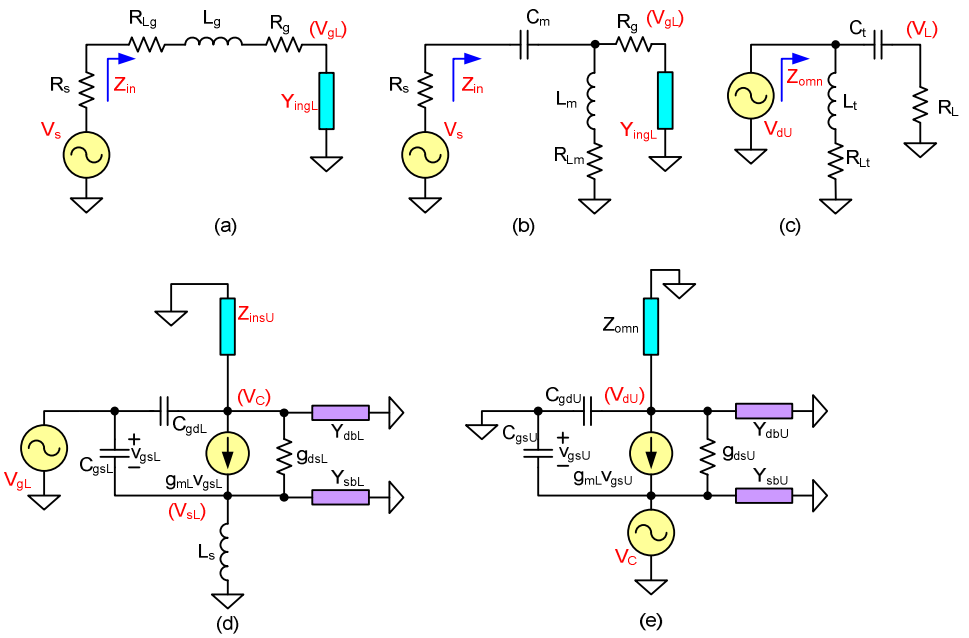


Fig. IV-9. Circuits used in calculation of cascode LNA power gain

$$y_{ddU} = g_{dsU} + j\omega C_{gdU} + Y_{omn} + Y_{dbU} \tag{IV-44}$$

And Y_{omn}, admittance into the output matching network from drain side, is calculated as:

$$Y_{omn} = \frac{1}{\omega L_t\left(j + 1/Q_{Lt}\right)} + \frac{1}{R_{load} + 1/\,j\omega C_t} \tag{IV-45}$$

The voltage transfer function of the output matching network is calculated using Fig. IV-8(c). Considering this figure we can write:

$$A_{omn} = \frac{V_L}{V_{dU}} = \frac{j\omega C_t R_L}{j\omega C_t R_L + 1} \tag{IV-46}$$

Finally the total voltage gain of the cascode LNA is calculated:

$$A = \frac{V_L}{V_s} = A_{ms} A_{imn} A_{dg} A_{ds} A_{omn} \tag{IV-47}$$

The input power from source into the LNA is calculated as:

$$P_{in} = \frac{\mathrm{Re}\left(Z_{in}\right)\left|V_s\right|^2}{2\left|R_s + Z_{in}\right|^2} \tag{IV-48}$$

And the power gain (transducer power gain) of the cascode LNA is obtained:

$$G = \frac{P_L}{P_{in}} = \frac{\left|R_s + Z_{in}\right|^2 \left|V_L\right|^2}{\mathrm{Re}\left(Z_{in}\right) R_L \left|V_s\right|^2} = \frac{\left|R_s + Z_{in}\right|^2}{\mathrm{Re}\left(Z_{in}\right) R_L} \left|A\right|^2 \tag{IV-49}$$

When conjugate matching holds in the input, the signal power into the input matching network is:

$$P'_{in} = \frac{\left|V_s\right|^2}{8R_s} \tag{IV-50}$$

Consequently maximum available power gain, i.e. the power gain in conjugally matched condition, is calculated as:

$$G_a = \frac{P'_{in}}{P_{in}} G_t = \frac{\left|R_s + Z_{in}\right|^2}{4R_s \times \mathrm{Re}\left(Z_{in}\right)} G_t \qquad \text{(IV-51)}$$

IV.2.1.5 Noise Analysis

Different analytic equations have been derived for calculation of noise performance of common source or cascode LNA [94], [7], [3]. Nevertheless, in our knowledge the reported works have some limitations that prevent an accurate noise performance calculation in mm-wave band.

- Very simple transistor model has been used.
- The noise contribution of upper transistor has been ignored. This is a good approximation in lower frequencies, in which the substrate effect is not crucial and hence the upper transistor noise is degenerated by its source impedance, i.e. the input impedance into the drain of the lower transistor. However in mm-wave range the substrate admittance becomes well comparable with the nodal admittance of the cascode node and lowers the noise degenerating effect. Consequently the contribution of the upper transistors noise in the total output noise increases.
- The substrate noise has been ignored. As explained, in mm-wave frequencies the substrate admittance increases and hence the substrate noise penetrates into the circuit.

We have developed our analytic equations to calculate the noise performance of cascode LNA by which the above limitations have been overcome.

The small signal noise equivalent circuit of cascode LNA has been shown in Fig. IV-10. Note that in calculation of noise figure, the load impedance has not any effect and hence for simplicity is substituted by short circuit [13]. Different noise sources in this figure are defined as follows:

- I_{ngL} and I_{ngU} are gate induced noise of lower and upper transistors, respectively. The induced gate noise is correlated with the drain thermal noise and in our noise model is calculated from (II-62).
- I_{ndL} and I_{ndU} are drain thermal noise of lower and upper transistors, respectively. The drain thermal noise in our noise model is calculated from (II-60).
- I_{nsbL}, I_{ndbL}, I_{nsbU} and I_{ndbU} are the substrate thermal noise, due to the real part of the substrate admittance at the lower and upper transistors source and drain nodes, respectively.
- I_{ns} is the thermal noise due to the input signal source resistance.
- I_{nM1} and I_{nM2} are the equivalent current noise sources of the input matching network.
- I_{nRg} is the thermal noise due to the gate poly-silicon resistance. This noise becomes important for small transistors.
- I_{nLs} is the thermal noise due to the effective parallel resistance of the degenerating inductor. This resistance is due to the limited quality factor of the inductor.

Our noise calculation is based on calculation of voltage noise in each node of the circuit in Fig. IV-10. For this purpose we must calculate the nodal impedance of all nodes. The nodal impedance at the input of circuit is:

$$Z_{ii} = \frac{Z_{in} R_s}{Z_{in} + R_s} \qquad \text{(IV-52)}$$

The nodal impedance at the gate of lower transistor is:

$$Z_{ggL} = \frac{1}{Y_{ingL} + Y_{imn}} \tag{IV-53}$$

Y_{ingL} is calculated from (IV-12) and Y_{imn} is the input admittance to the input matching network from gate side, shown in Fig. IV-10. The nodal impedance at the internal gate of lower transistor is:

$$Y_{gigiL} = \frac{Y_{imn}}{1 + R_g Y_{imn}} + \frac{Y_{ingL}}{1 - R_g Y_{ingL}} \tag{IV-53}$$

The nodal impedance at the source of lower transistor is:

$$Z_{ssL} = \frac{1}{Y_{insL} + \dfrac{1}{\omega L_s (j + 1/Q_{Ls})}} \tag{IV-54}$$

L_s is the degenerating inductor. Y_{insL} is the input admittance to the source of lower transistor and is calculated as:

$$Y_{ins} = \frac{I_s}{V_s} = \frac{\begin{pmatrix} j\omega C_{gd}(g_m + g_{ds})(j\omega C_{gs} + g_m) \\ + j\omega C_{gs} y_{dd}(j\omega C_{gs} + g_m) \\ + y_{gg} g_{ds}(g_m + g_{ds}) + \dfrac{C_{gs}}{C_{gd}} y_{dd} y_{gg} g_{ds} \end{pmatrix}}{j\omega C_{gd}(j\omega C_{gd} - g_m) - y_{dd} y_{gg}} + \frac{C_{gs}}{C_{gd}} g_{ds} + y_{ss} \tag{IV-55}$$

In which:

$$y_{gg} = Y_g + j\omega C_{gd} + j\omega C_{gs}$$

$$y_{ss} = j\omega C_{gs} + g_m + g_{ds} + Y_{sb}$$

$$y_{dd} = Y_d + Y_{db} + j\omega C_{gd} + g_{ds}$$

The nodal impedance at the cascode node is calculated as:

$$Z_{CC} = \frac{1}{Y_{indL} + Y_{insU}} \tag{IV-56}$$

Y_{indL} and Y_{insU} are calculated from (IV-26) and (IV-25), respectively. After calculating the nodal impedances, we can calculate the noise voltage at each node, using the noise current sources in Fig. IV-10. In this figure, if series inductor is used for input matching (Fig. IV-4 (a)), I_{nM1} and I_{nM2} are calculated as:

$$\frac{\overline{I_{nM1}^2}}{4KT\Delta f} = \frac{R_{Lg}}{\left|R_s + R_{Lg} + j\omega L_g\right|^2} \tag{IV-57}$$

$$\overline{I_{nM2}^2} = 0$$

And in the case of parallel inductor in the input matching network (Fig. IV-4 (b)) we have:

$$\overline{I_{nM1}^2} = 0$$

$$\frac{\overline{I_{nM2}^2}}{4KT\Delta f} = \frac{R_{Lm}}{R_{Lm}^2 + \omega^2 L_m^2} \tag{IV-58}$$

The noise voltage at the circuit input is calculated as:

$$V'_{ni} = \left(I_{ns} + I_{nM1}\right)Z_{ii} \tag{IV-59}$$

The noise voltage at the gate of lower transistor, due to the noise currents entering into this node is calculated as:

$$V'_{ngL} = \left(-I_{nRg} + I_{nM2}\right)Z_{ggL} \tag{IV-60}$$

The noise voltage at the internal gate of lower transistor, due to the noise currents entering into this node is calculated as:

$$V'_{ngiL} = \left(I_{ngL} + I_{nRg}\right)Z_{gigiL} \tag{IV-61}$$

The noise voltage at the source of lower transistor, due to the noise currents entering into this node is calculated as:

$$V'_{nsL} = \left(I_{nLs} + I_{nsbL} + I_{ndL} - I_{ngL}\right)Z_{ssL} \tag{IV-62}$$

The noise voltage at the cascode node, due to the noise currents entering into this node is calculated as:

$$V'_{nC} = \left(I_{ndbL} + I_{nsbU} - I_{ndL} + I_{ndU} - I_{ngU}\right)Z_{CC} \tag{IV-63}$$

Note that in the above equation, the noise voltage at each node due to other nodes has not been included. To include the transferred voltages, we can use the voltage transfer functions, derived in previous section. Doing this, the total noise voltage at the cascode node is calculated as:

$$V_{nC} = V'_{nC} + A_{dsL}V'_{nsL} + \left(\left(V'_{ni}A_{imn} + V'_{ngL}\right)A_{gigL} + V'_{ngiL} \right)A_{dgiL} \tag{IV-64}$$

Where A_{dsL}, A_{imn}, A_{gigL} and A_{dgiL} are calculated from (IV-36), (IV-40), (IV-33) and (IV-32), respectively. The trans-conductance from the cascode node to the output is simply obtained from Fig. IV-10:

$$G_{OC} = \frac{I_{nO}}{V_{nC}} = g_{mU} + g_{dsU} \tag{IV-65}$$

The total output noise current (I_{nO} in Fig. IV-10) is calculated:

$$I_{nO} = \left(g_{mU} + g_{dsU}\right)V_{nC} - I_{ndU} - I_{ndbU} \tag{IV-66}$$

Substituting the equations (IV-59) to (IV-63) in (IV-64) we obtain:

$$\begin{aligned} V_{nC} = {} & \left(I_{ndbL} + I_{nsbU} - I_{ndL} + I_{ndU} - I_{ngU}\right)Z_{CC} + A_{dsL}\left(I_{nLs} + I_{nsbL} + I_{ndL} - I_{ngL}\right)Z_{ssL} \\ & + \left(\left(\left(I_{ns} + I_{nM1}\right)Z_{ii}A_{imn} + \left(-I_{nRg} + I_{nM2}\right)Z_{ggL} \right)A_{gigL} + \left(I_{ngL} + I_{nRg}\right)Z_{gigiL} \right)A_{dgiL} \end{aligned}$$

and then using (IV-66) and reordering the terms we deduce:

$$I_{nO} = \left(g_{mU} + g_{dsU}\right) \begin{pmatrix} I_{ns}Z_{ii}A_{imn}A_{gigL}A_{dgiL} + I_{nM1}Z_{ii}A_{imn}A_{gigL}A_{dgiL} + I_{nM2}Z_{ggL}A_{gigL}A_{dgiL} \\ + I_{nLs}A_{dsL}Z_{ssL} + \left(I_{ndbL} + I_{nsbU}\right)Z_{CC} + I_{nsbL}A_{dsL}Z_{ssL} \\ + I_{nRg}\left(Z_{gigiL}A_{dgiL} - Z_{ggL}A_{gigL}A_{dgiL}\right) + I_{ngL}\left(Z_{gigiL}A_{dgiL} - A_{dsL}Z_{ssL}\right) \\ + I_{ndL}\left(-Z_{CC} + A_{dsL}Z_{ssL}\right) + \left(-I_{ngU} + I_{ndU}\right)Z_{CC} \end{pmatrix} - I_{ndU} - I_{ndbU} \tag{IV-67}$$

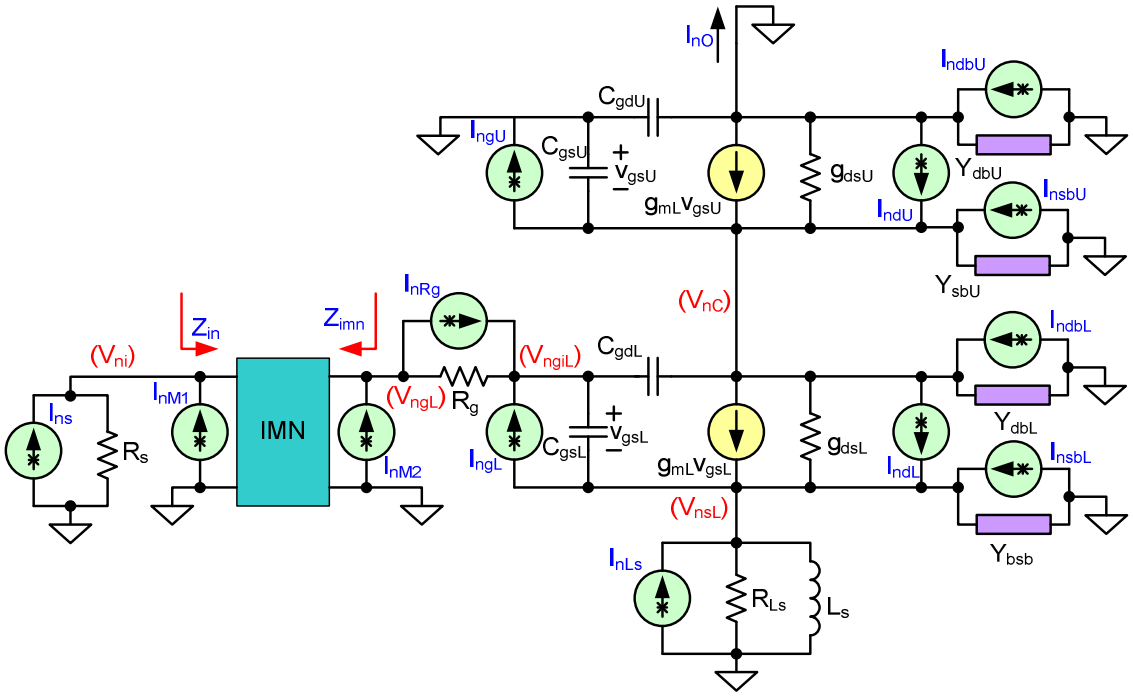


Fig. IV-10. Small signal circuit and noise model of cascode LNA

To analyze the noise performance of LNA, the output noise power must be calculated. This is accomplished by calculating the average power of (IV-67). For simplicity we separate different noise sources in (IV-66). The contribution of lower transistor is:

$$I_{nOL} = (g_{mU} + g_{dsU})\begin{pmatrix} I_{ngL}(Z_{gigiL}A_{dgiL} - A_{dsL}Z_{ssL}) \\ + I_{ndL}(-Z_{CC} + A_{dsL}Z_{ssL}) \end{pmatrix} \quad \text{(IV-68)}$$

The noise contribution of upper transistor is:

$$I_{nOU} = (g_{mU} + g_{dsU})(-I_{ngU} + I_{ndU})Z_{CC} - I_{ndU} \quad \text{(IV-69)}$$

The noise contribution of the signal source is:

$$I_{nOs} = (g_{mU} + g_{dsU})Z_{ii}A_{imn}A_{gigL}A_{dgiL}I_{ns} \quad \text{(IV-70)}$$

The noise contribution of the gate resistance is:

$$I_{nORg} = (g_{mU} + g_{dsU})(Z_{gigiL}A_{dgiL} - Z_{ggL}A_{gigL}A_{dgiL})I_{nRg} \quad \text{(IV-71)}$$

The noise contribution of the input matching network is:

$$I_{nOM} = (g_{mU} + g_{dsU})(I_{nM1}Z_{ii}A_{imn}A_{gigL}A_{dgiL} + I_{nM2}Z_{ggL}A_{gigL}A_{dgiL}) \quad \text{IV-72)}$$

The noise contribution of the substrate is:

$$I_{nOb} = (g_{mU} + g_{dsU})\left((I_{ndbL} + I_{nsbU})Z_{CC} + I_{nsbL}A_{dsL}Z_{ssL} \right) - I_{ndbU} \quad \text{(IV-73)}$$

The noise contribution of the degenerating inductor is:

$$I_{nOLs} = (g_{mU} + g_{dsU})A_{dsL}Z_{ssL}I_{nLs} \quad \text{(IV-74)}$$

A) Output Noise Power

The output noise power is calculated as mean square of the output noise current. I_{ngL} and I_{ngU} are correlated with I_{ndL} and I_{ndU}, respectively. Consequently their correlation coefficient, as in

(II-64) should be considered. Contribution of the lower transistor in the normalized output noise power is calculated as:

$$\frac{\overline{I_{nOL}^2}}{4kT\Delta f\left(g_{mU}+g_{dsU}\right)^2}=\left|A_{dsL}Z_{ssL}-Z_{CC}\right|^2\gamma\cdot g_{d_0L}+\left|Z_{gigiL}A_{dgiL}-A_{dsL}Z_{ssL}\right|^2\delta\cdot g_{gL}$$
$$-2\,\mathrm{Im}\left(\left(Z_{gigiL}A_{dgiL}-A_{dsL}Z_{ssL}\right)\left(A_{dsL}Z_{ssL}-Z_{CC}\right)^*\right)\left|c\right|\sqrt{\delta\cdot g_{gL}\gamma\cdot g_{d_0L}} \quad \text{(IV-75)}$$

A_{dsL} and A_{dgL} are voltage gain, defined in (IV-33) and (IV-35), respectively. The transistor noise parameters, c, g_g, g_{d0}, δ and γ, have been defined in chapter II, section II-2. Contribution of the upper transistor in the normalized output noise power is calculated as:

$$\frac{\overline{I_{nOU}^2}}{4kT\Delta f\left(g_{mU}+g_{dsU}\right)^2}=\frac{\left|\left(g_{mU}+g_{dsU}\right)Z_{CC}-1\right|^2}{\left(g_{mU}+g_{dsU}\right)^2}\gamma\cdot g_{d_0U}+\left|Z_{CC}\right|^2\delta\cdot g_{gU}$$
$$+2\,\mathrm{Im}\left(Z_{CC}\left(Z_{CC}-\frac{1}{g_{mU}+g_{dsU}}\right)^*\right)\left|c\right|\sqrt{\delta\cdot g_{gU}\gamma\cdot g_{d_0U}} \quad \text{(IV-76)}$$

Contribution of the signal source in the normalized output noise power is calculated as:

$$\frac{\overline{I_{nOs}^2}}{4kT\Delta f\left(g_{mU}+g_{dsU}\right)^2}=\left|Z_{ii}A_{imn}A_{gigL}A_{dgiL}\right|^2\frac{1}{R_s} \quad \text{(IV-77)}$$

Contribution of the gate resistance in the normalized output noise power is calculated as:

$$\frac{\overline{I_{nORg}^2}}{4kT\Delta f\left(g_{mU}+g_{dsU}\right)^2}=\left|Z_{gigiL}A_{dgiL}-Z_{ggL}A_{gigL}A_{dgiL}\right|^2\frac{1}{R_g} \quad \text{(IV-78)}$$

Contribution of the input matching network in the normalized output noise power is:

$$\frac{\overline{I_{nOM}^2}}{4kT\Delta f\left(g_{mU}+g_{dsU}\right)^2}=\left|Z_{ii}A_{imn}A_{gigL}A_{dgiL}\right|^2\frac{\overline{I_{nM1}^2}}{4kT\Delta f}+\left|Z_{ggL}A_{gigL}A_{dgiL}\right|^2\frac{\overline{I_{nM2}^2}}{4kT\Delta f} \quad \text{(IV-79)}$$

$\overline{I_{nM1}^2}$ and $\overline{I_{nM2}^2}$ are calculated from (IV-57) and (IV-58), respectively. Contribution of the substrate in the normalized output noise power is calculated as:

$$\frac{\overline{I_{nOb}^2}}{4kT\Delta f\left(g_{mU}+g_{dsU}\right)^2}=\left|Z_{CC}\right|^2\left(G_{dbL}+G_{sbU}\right)+\left|A_{dsL}Z_{ssL}\right|^2G_{sbL}+\frac{G_{dbU}}{\left(g_{mU}+g_{dsU}\right)^2} \quad \text{(IV-80)}$$

Where G_x is the real part of Y_x. Contribution of the degenerating inductor in the normalized output noise power is calculated as:

$$\frac{\overline{I_{nOLs}^2}}{4kT\Delta f\left(g_{mU}+g_{dsU}\right)^2}=\left|A_{dsL}Z_{ssL}\right|^2\frac{R_{Ls}}{R_{Ls}^2+\omega^2L_s^2} \quad \text{(IV-81)}$$

B) Noise Factor

The noise factor due to the lower transistor is calculated as:

$$F_L=1+\frac{\overline{I_{nOL}^2}}{\overline{I_{nOs}^2}} \quad \text{(IV-82)}$$

The noise factor due to the upper transistor is calculated as:

$$F_U=1+\frac{\overline{I_{nOU}^2}}{\overline{I_{nOs}^2}} \quad \text{(IV-83)}$$

The noise factor due to the gate resistance is calculated as:

$$F_{Rg} = 1 + \frac{\overline{I_{nORg}^2}}{\overline{I_{nOs}^2}} \tag{IV-84}$$

The noise factor due to the substrate is calculated as:

$$F_b = 1 + \frac{\overline{I_{nOb}^2}}{\overline{I_{nOs}^2}} \tag{IV-85}$$

The noise factor due to the degenerating inductor is calculated as:

$$F_{Ls} = 1 + \frac{\overline{I_{nOLs}^2}}{\overline{I_{nOs}^2}} \tag{IV-86}$$

Finally the total noise factor of LNA is obtained as:

$$F = 1 + (F_L - 1) + (F_U - 1) + (F_{Rg} - 1) + (F_b - 1) + (F_{Ls} - 1) \tag{IV-87}$$

IV.2.1.6 Linearity Analysis

Different analytic methods have been developed to evaluate the linearity performance of LNA circuits in MOS technology. Some of them uses simple equations to estimate the IIP3[1] or one-dB compression point (P1dB) of LNA [98], [70]. Some other works have developed complicated analysis [3], [7]. The method developed in [70] is based on deriving analytic equation of transistor's g_m as a function of gate-source bias voltage. Then this equation has been used for calculation of higher order terms of g_m in its Taylor expansion around the bias point, in different operation regions of transistor.

We have used similar approach, using our analytic equation for g_m of MOS transistor, developed in Chapter II. The large signal trans-conductance of transistor can be calculated as:

$$G_m = g_m + \frac{\partial g_m}{\partial V_{gs}} V_{gs} + \frac{1}{2}\frac{\partial^2 g_m}{\partial V_{gs}^2} V_{gs}^2 + \cdots \tag{IV-88}$$

Where V_{gs} is the amplitude of AC signal between gate and source nodes and the derivatives are calculated at bias point. g_m is calculated from (II-41). To calculate IIP3, we must drive the circuit with two in-band signals with same amplitude, but small frequency difference. We denote the gate-source voltage due to these signals as:

$$\begin{aligned} v_1(t) &= \frac{V_{gs}}{2}\left(e^{j\omega_1 t} + e^{-j\omega_1 t}\right) \\ v_2(t) &= \frac{V_{gs}}{2}\left(e^{j\omega_2 t} + e^{-j\omega_2 t}\right) \end{aligned} \tag{IV-89}$$

Then the resulted drain current is calculated using large signal trans-conductance:

$$i_d(t) = G_m\left(v_1(t) + v_2(t)\right) \tag{IV-90}$$

Using (IV-89) we deduce:

$$i_d(t) = g_m\left(v_1(t) + v_2(t)\right) + \frac{\partial g_m}{\partial V_{gs}}\left(v_1(t) + v_2(t)\right)^2 + \frac{1}{2}\frac{\partial^2 g_m}{\partial V_{gs}^2}\left(v_1(t) + v_2(t)\right)^3 \tag{IV-91}$$

and substituting (IV-88) in (IV-91) and neglecting out-of-band terms we obtain:

[1] 3rd order Input Intercept Point

$$i_d(t)=\frac{g_m V_{gs}}{2}\left(e^{j\omega_1 t}+e^{-j\omega_1 t}+e^{j\omega_2 t}+e^{-j\omega_2 t}\right) + \frac{3}{16}\frac{\partial^2 g_m}{\partial V_{gs}^2}V_{gs}^3\left(e^{j(2\omega_1-\omega_2)t}+e^{-j(2\omega_1-\omega_2)t}+e^{j(2\omega_2-\omega_1)t}+e^{-j(2\omega_2-\omega_1)t}\right) \quad \text{(IV-92)}$$

Consequently the desired signal power at the output node is calculated as:

$$P^{des}=\frac{g_m^2 V_{gs}^2}{2}R_L \quad \text{(IV-93)}$$

And the power of 3rd order inter-modulation terms at the output node is calculated as:

$$P^{IM3}=\frac{9}{64}\left(\frac{\partial^2 g_m}{\partial V_{gs}^2}\right)^2 V_{gs}^6 R_L \quad \text{(IV-94)}$$

At the 3rd order intercept point the signal power and the power of 3rd order inter-modulation terms are equal. So setting (IV-93) equal to (IV-94)we obtain:

$$V_{gs}^2\Big|_{IP3}=\frac{\sqrt{32}\,g_m}{3\left|\frac{\partial^2 g_m}{\partial V_{gs}^2}\right|} \quad \text{(IV-95)}$$

If degenerating impedance is used at the source node of transistor, we have:

$$V_g=\frac{V_{gs}}{\left|1+g_m Z_s\right|} \quad \text{(IV-96)}$$

Where Z_s is the impedance at the source node. The voltage at the circuit input is calculated as:

$$V_{in}=\frac{V_g}{\left|A_{imn}\right|} \quad \text{(IV-97)}$$

In which A_{imn} is the voltage gain of the input matching network, defined in (IV-41). Using (IV-95), (IV-96) and (IV-97) we obtain:

$$V_{in}^2\Big|_{IP3}=\frac{\sqrt{32}}{3\left|A_{imn}\right|^2\left|1+g_m Z_s\right|^2}\frac{g_m}{\left|\frac{\partial^2 g_m}{\partial V_{gs}^2}\right|} \quad \text{(IV-98)}$$

Now similar to (IV-48) we can calculate the input power to the LNA at 3rd order intercept point:

$$IIP3=\frac{\mathrm{Re}(Z_{in})}{2\left|Z_{in}\right|^2}V_{in}^2\Big|_{IP3} \quad \text{(IV-99)}$$

And finally:

$$IIP3=\frac{\sqrt{32}}{6}\frac{\mathrm{Re}(Z_{in})}{\left|Z_{in}\right|^2\left|A_{imn}\right|^2\left|1+g_m Z_s\right|^2}\frac{g_m}{\left|\frac{\partial^2 g_m}{\partial V_{gs}^2}\right|} \quad \text{(IV-100)}$$

The trans-conductance (g_m), its second derivative and ratio of g_m over its second derivative have been shown in Fig. IV-11, for W=30 um and different bias condition. This figure shows that the second derivative g_m crosses zero. Based on (IV-100) at this point IIP3 goes toward

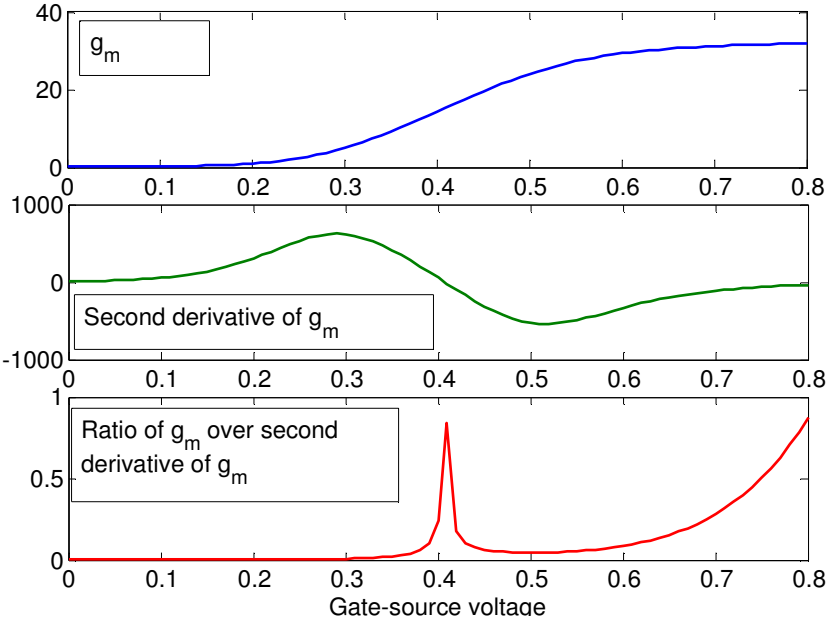


Fig. IV-11. The trans-conductance (g_m), its second derivative and ratio of g_m over its second derivative, versus gate-source bias voltage

infinity. This point is the well known sweet point of 3rd order non-linearity. Also this figure shows that the linearity increases with increasing V_{gs}.

IV.3 Our LNA Optimization Methodology

Various optimization techniques for LNA circuits were discussed in section IV.1.4. Simultaneous noise and power (impedance) matching is the most preferred technique in CMOS LNA and has been used in analytic, numerical or graphical optimization strategies. By this technique the best noise performance is calculated analytically, numerically or graphically, preserving the conjugate matching in both input and output.

We will pursue this technique in our analytic and numerical optimization. We have developed 3-step design and optimization strategy in our work. The first step is based on the analysis results of previous section, in which simple models are used for active devices and passive and parasitic elements. In the second step, we use accurate Y-parameter model for active devices, as well as an accurate model for substrate and other parasitic effects. In this step, mathematical matrix equations are used in calculating matching circuits and LNA performance characteristics. Then graphical optimization is used to optimize the design parameters. In the third step, the layout is designed and final post layout simulation and verification is performed.

All of our optimizations and simulations are carried out by our design tool, briefly presented in section IV.4. Our design tool will be compared in the last section of this chapter, with Spectre RF and the attached foundry design kit for STMicroelectronics 90 nm Global Purpose (GP) CMOS process. Accuracy and performance of our design tool is better than parasitic-aware simulation in Spectre-RF and hence we have used it in our design and simulations.

The optimization goal definition is an important issue in each optimization problem. The goal must cover all of the designer's desired characteristics, with proper weight. In the case of LNA, four characteristics, i.e. noise factor, gain, linearity and band-width should be included in the optimization goal. An standard Figure-of-Merit (FOM) that is conventionally used in literatures to compare different LNA designs, is defined as [99], [86], [61], [31]:

$$FOM = \frac{G \cdot IIP3 \cdot BW}{P_{DC}(F-1)} \tag{IV-101}$$

G is the absolute value of power gain, $IIP3$ is the absolute value of 3rd order input intercept point in milliwats, BW is the LNA band width in GHz, P_{DC} is the LNA DC power consumption in milliwatts and F is the noise factor (absolute value). In some cases IIP3 is replace by P1dB.

However we will use constant-envelope modulations (See Chapter V) in our transceiver design and consequently linearity is of less importance. So we have used the below FOM to be maximized in our optimizations:

$$FOM = \frac{G \cdot IIP3^{\left(\frac{1}{4}\right)} \cdot BW}{P_{DC}(F-1)} \tag{IV-102}$$

IV.3.1 Step I: Analytic Optimization

Analytic optimization is based on the analysis results of the later section. The optimization flow diagram has been shown in Fig. IV-12. In this flow chart we have used simple search method. However other numerical optimizations can be used in conjunction with the analytic equations. Two flowcharts have been shown in Fig. IV-12. The first is for input matching with degenerating inductor and series inductor in the gate. Normally with this matching, the LNA has good linearity. Nevertheless there is no freedom to control the linearity. The second flowchart is applied for LC matching network. In this condition the degenerating inductor has freedom to control the linearity. The design steps are as follows:

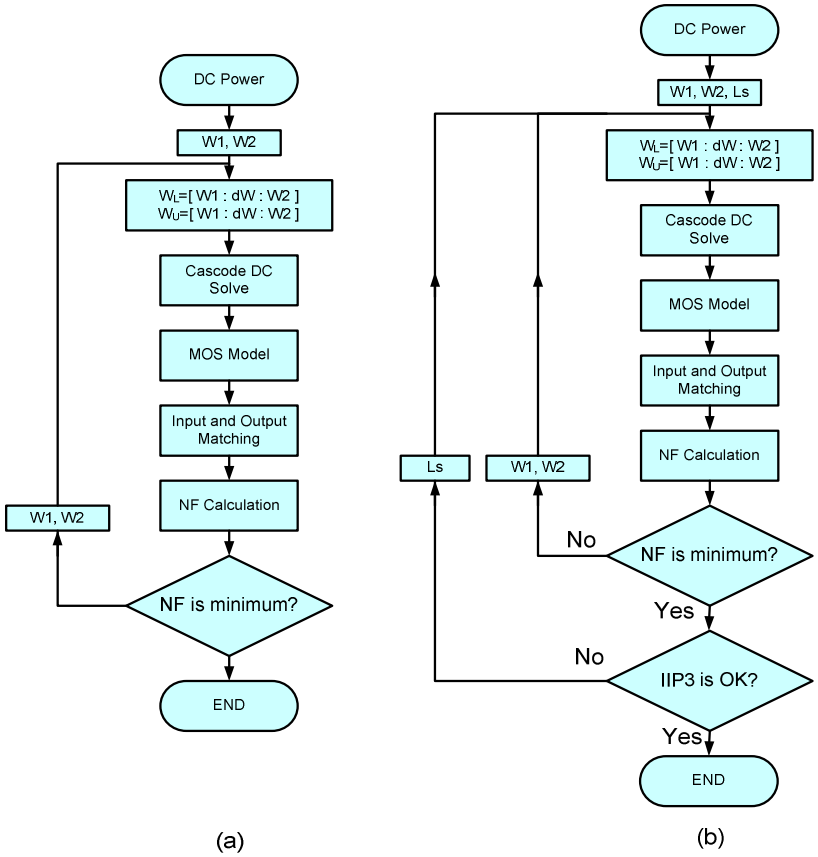


Fig. IV-12. Cascode LNA optimization flowchart, based on analysis results, for input matching with series inductor (a) and input matching with LC network (b)

A) Input Matching Using Series Inductor in Gate

a) Calculate approximated value of Z_{insU} from (IV-6)
b) Calculate the coefficients a_i, b_i and c_i
   - In the case of conventional matching method, these coefficients are not defined
   - In the case of our first matching method , use (IV-9)
   - In the case of our second matching method , use (IV-12)
c) Calculate the degenerating inductance, L_s
   - In the case of conventional matching method , use (IV-4)
   - In the case of our matching method , use (IV-15)
d) Calculate the gate inductor, L_g
   - In the case of our first matching method , use (IV-9)
   - In the case of our second matching method , use (IV-12)

B) Input Matching Using Parallel Inductor in Gate

This matching circuit is not applicable in the case of conventional input matching method.

a) Calculate the degenerating inductance, L_s, using (IV-72)
b) Calculate accurate value of Z_{ingL}
   - In the case of our first matching method , use (IV-9)
   - In the case of our second matching method , use (IV-12)
c) Calculate the matching inductor, L_m using (IV-22)
d) Calculate the matching capacitance, C_m using (IV-25)

C) Output Matching

After designing the input matching network, the output matching network is designed.

a) Calculate accurate value of Z_{indL}, using (IV-26)
b) Calculate accurate value of Z_{indU}, using (IV-25)
c) Calculate the matching inductor, L_t using (IV-31)
d) Calculate the matching capacitance, C_t using (IV-28)

D) Power gain analysis

a) Calculate Y_{insU} using (IV-5)
b) Calculate accurate value of Z_{ingL} , using (IV-12)
c) Calculate the voltage gain of the input matching network
   - In the case of series inductor for input matching, use (IV-36)
   - In the case of parallel inductor for input matching, use (IV-37)
e) Calculate the voltage gain of the lower transistor, with substituting (IV-37) in (IV-33)
f) Calculate the voltage gain of the upper transistor, using (IV-39)
g) Calculate the voltage gain of the output matching network, using (IV-41)
h) Calculate the total voltage gain of cascode from (IV-42)
i) Calculate the transducer power gain from (IV-44)
j) Calculate the available power gain from (IV-45)

IV.3.2 Step II: Y-Parameter Optimization

After analytic design and optimization process, as discussed in the previous section, we use Y-Parameter analysis to optimization of the LNA circuit. In this step 4×4 Y matrix, developed in Chapter II is used as MOS transistor model. In the case of passive elements and parasitic, 3×3 Y and 2×2 Y-Parameter models are used. The details will be given in the next section, in post-layout simulation.

IV.3.2.1 Y-Parameter analysis Basis

Our Y-Parameter analysis is based on two-port network analysis and conversion from Y-Parameter to S-Parameter. However, as described, we encounter with 3-Port and 4-Port models, that can not be manipulated using 2-Port Y-Parameters equations. For simplicity, we have used a simple transform to convert all models to two-port models. Consider the 4-Port network of Fig. IV-12, described by a 4×4 Y matrix and terminated to Y_3 and Y_4, in 3^{ed} and 4th ports, respectively. Simply we can write:

$$\begin{bmatrix} I_1 \\ I_2 \\ -V_3Y_3 \\ -V_4Y_4 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} \times \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} \tag{IV-103}$$

Now we can write:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = Z' \times \begin{bmatrix} I_1 \\ I_2 \\ 0 \\ 0 \end{bmatrix} \tag{IV-104}$$

In which, $Z' = inv(Y')$ and:

$$Y' = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33}+Y_3 & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44}+Y_4 \end{bmatrix} \tag{IV-105}$$

So we have;

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z'_{11} & Z'_{12} \\ Z'_{21} & Z'_{22} \end{bmatrix} \times \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{IV-106}$$

And finally we obtain the equivalent two-port Y-Parameter model:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Z'_{11} & Z'_{12} \\ Z'_{21} & Z'_{22} \end{bmatrix}^{-1} \times \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Y''_{11} & Y''_{12} \\ Y''_{21} & Y''_{22} \end{bmatrix} \times \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{IV-107}$$

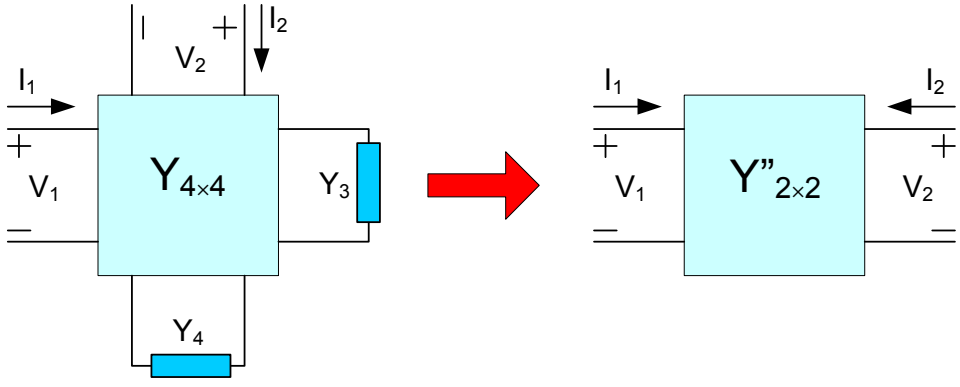


Fig. IV-13. Terminated 4-Port network and its equivalent 2-port model

IV.3.2.2 Input Matching and Gain Calculation

The input matching with degenerating inductor in source and serial inductor in gate can be performed using Y-Matrix analysis, without need for numerical optimization. The details have been reported in our papers [100]. This method reduces one optimization variables and this leads to less complicated optimization process. However this method is not useful for other input matching networks.

The power gain and impedance analysis, the LNA circuit is translated into a set of 2-Port cascaded networks, using the equation of the previous section.

IV.3.2.3 Noise Performance Calculation

We have developed a general method to convert any noisy multi-port network to an equivalent noise-less network plus standard current and voltage noises at the input port. Representing all of the internal noise sources as current noises, general noisy multi-port can be explained as a combination of a noise-less multi-port and some current noises at the ports, as depicted in Fig. IV-14 (a). Without loss of generality, we assign the input and output ports to the ports 1 and 2, respectively. Then the equivalent standard multi-port network will be as in Fig. IV-14 (b).

The problem is to find the equivalent current and voltage noise sources at the input port. Describing the network by Y matrix we have:

$$Y = \begin{bmatrix} Y_{11} & Y_{12} & \dots & Y_{1N} \\ Y_{21} & Y_{22} & \dots & Y_{2N} \\ \vdots & \vdots & \dots & \vdots \\ Y_{N1} & Y_{N2} & \dots & Y_{NN} \end{bmatrix} \tag{IV-108}$$

Now we define a new matrix:

$$Y'' = \begin{bmatrix} Y_{21} & Y_{23} & \dots & Y_{2N} \\ Y_{31} & Y_{33} & \dots & Y_{3N} \\ \vdots & \vdots & \dots & \vdots \\ Y_{N1} & Y_{N3} & \dots & Y_{NN} \end{bmatrix} \tag{IV-109}$$

Then the equivalent current and voltage noises in Fig. IV-14 (b) is calculated as:

$$\begin{cases} I_n = \dfrac{\Delta_{12} I_{n1} + \Delta_{22} I_{n2} + \cdots \Delta_{N2} I_{nN}}{\Delta_{12}} \\ V_n = \dfrac{\Delta''_{11} I_{n2} + \Delta''_{21} I_{n3} + \cdots \Delta''_{N-1,1} I_{nN}}{\Delta_{12}} \end{cases} \tag{IV-110}$$

Where Δ_{ij} and Δ''_{ij} are the determinant of the adjoint matrix of ij^{th} element of Y matrix in (IV-108) and Y'' in (IV-109), respectively.

After calculating the standard equivalent input noise sources, the noise parameters of the multi-port network are calculated [101]. In general V_n and I_n in Fig. IV-14 (b) are correlated. If the correlation coefficient is denoted as c:

$$c = \overline{I_n V_n^*} \tag{IV-111}$$

We can divide I_n into two terms, one of them is correlated to V_n and the other is un-correlated:

$$I_n = I_{nc} + I_{nu} \tag{IV-112}$$

We can write:

$$\overline{I_n V_n^*} = \overline{(I_{nc} + I_{nu})V_n^*} = \overline{I_{nc} V_n^*} \tag{IV-113}$$

Then the correlation admittance is defined as:

$$Y_c = G_c + jB_c = \frac{I_{nc}}{V_n} \tag{IV-114}$$

And hence it calculated as:

$$Y_c = \frac{c}{\overline{V_n^2}} \tag{IV-115}$$

Equivalent noise resistance is defined as:

$$R_n = \frac{\overline{V_n^2}}{4kTB} \tag{IV-116}$$

Equivalent noise conductance is defined as:

$$G_u = \frac{\overline{I_{nu}^2}}{4kTB} = \frac{\overline{I_n^2} - \overline{I_{nc}^2}}{4kTB} = \frac{\overline{I_n^2} - |Y_c|^2 \overline{V_n^2}}{4kTB} \tag{IV-117}$$

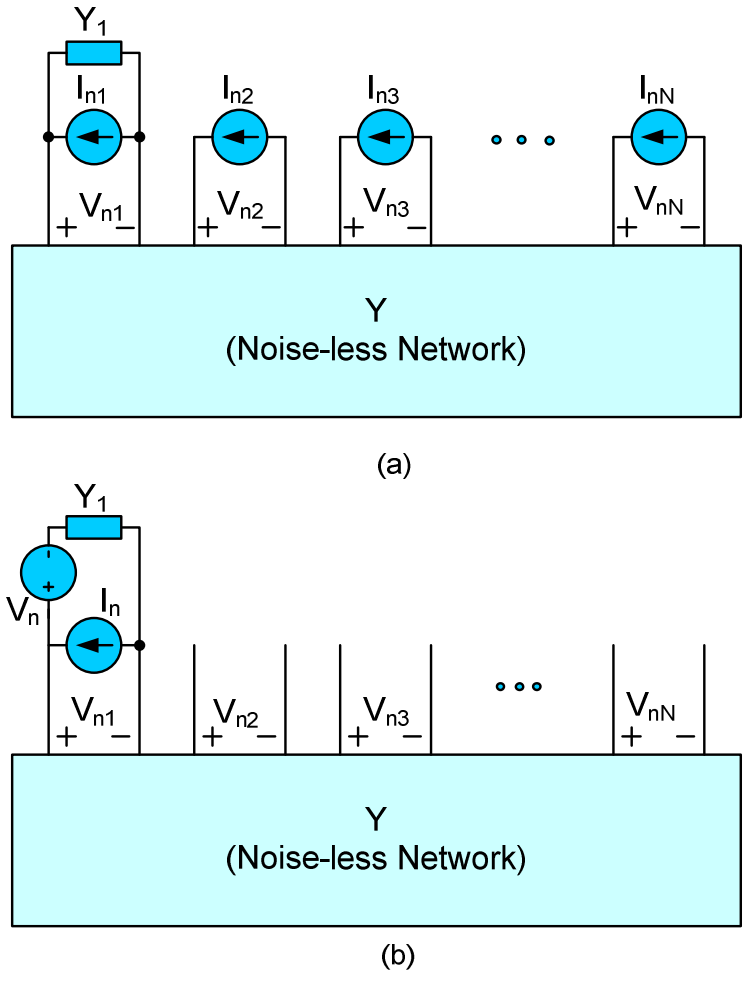


Fig. IV-14. Noisy multi-port (a) and its equivalent noise-less multi-port network, with equivalent current and voltage noise sources at the input (b)

To derive the equation above we have used:

$$\overline{I_{nu}^2} = \overline{I_n^2} - \frac{|c|^2}{\overline{V_n^2}} \tag{IV-118}$$

The optimum source admittance for minimum noise factor is calculated as:

$$\begin{aligned} Y_{s\_opt} &= \sqrt{G_c^2 + \frac{G_u}{R_n}} - jB_c \\ &= \sqrt{\frac{\overline{I_n^2}}{\overline{V_n^2}} - B_c^2} - jB_c \end{aligned} \tag{IV-119}$$

Minimum noise figure is calculated as:

$$F_{\min} = 1 + \frac{G_u + R_n\left(G_{Sopt} + G_c\right)^2}{G_{Sopt}} \tag{IV-120}$$

And finally, the noise factor of the multi-port is calculated as:

$$F = 1 + \frac{G_u + R_n\left|Y_S + Y_c\right|^2}{G_S} \tag{IV-121}$$

IV.3.3 Step IV: Post Layout Simulation

The main difference between post layout simulation and Y-Parameter analysis in the next section is in the modeling of transmission lines and passive devices. Note that all of the MOS transistor parasitic effects are included in Y-Parameter analysis, as well as in post layout simulation. Post layout simulation is performed in two steps. In the first step our design tool is used for final refinement of circuit parameters, to eliminate the deviations in the circuit characteristics, due to the accurate passive elements modeling. The final step is performed in the foundry design kit, after including all passive models and parasitic effects, to final verify the design.

The circuit schematic in the post-layout simulation has been shown in Fig. IV-14. Parallel inductor in gate has been used for input matching, as in Fig. IV-4 (b). 3-type of distributed elements have been used: transmission lines, line-type inductors and T-connectors. In addition, A lumped model is used for modeling RF pads. The details of RF pad modeling will be given in Chapter III. MIM[1] capacitors and all resistors are accurately modeled in the design kit, considering coupling to the substrate.

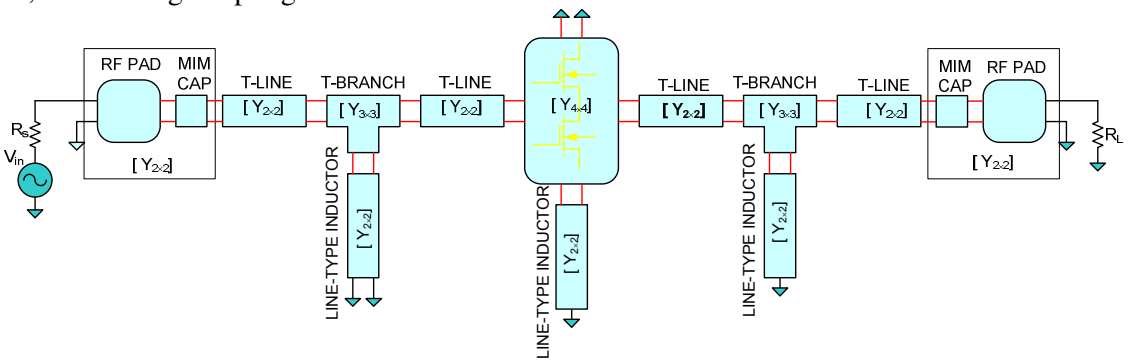


Fig. IV-15. Post-layout model of cascode LNA, with parallel inductor in input matching network.

[1] Metal-Insulator-Metal

IV.4 Practical Design and Fabrication

First step of design is choosing proper circuit and its topology and configuration. This is accomplished based on the designer's experience and the requirements of the system under design, in which the LNA will be used. The next step is determining the DC power consumption of the LNA. DC power is determined based on the system requirements and the designer's experience and investigating the simulation results.

As we explained, our design flow is a power- constrained optimization process and hence, as in all power-constrained LNA optimization techniques, the designer should estimate or choose the proper DC power consumption. We will do the DC power selection based on a logical investigation using our design tool. This design tool has the ability of analysis (simulation) and optimization (synthesis) of cascode LNA with various configurations. Both of simulation and synthesis may be accomplished in two ways: one way is based on the analytic equations derived in section IV.2.1 and the other is based on the numeric method, explained in section IV.3.2. MOS transistor model, described in Chapter II, is used in the design tool. Transmission lines, RF pads, inductors, parasitic elements and other passive elements are modelled as developed in Chapter III. Captured view of the design tool has been shown in Fig. IV-16.

IV.4.1 Design Process

IV.4.1.1 Circuit Topology and Implementation Issues

As discussed in section IV-2, cascode LNA is most suited for low power applications, since it enables the designer to obtain good performance using a single stage LNA. So we use cascode topology in our design, as depicted schematically in Fig. IV-4.

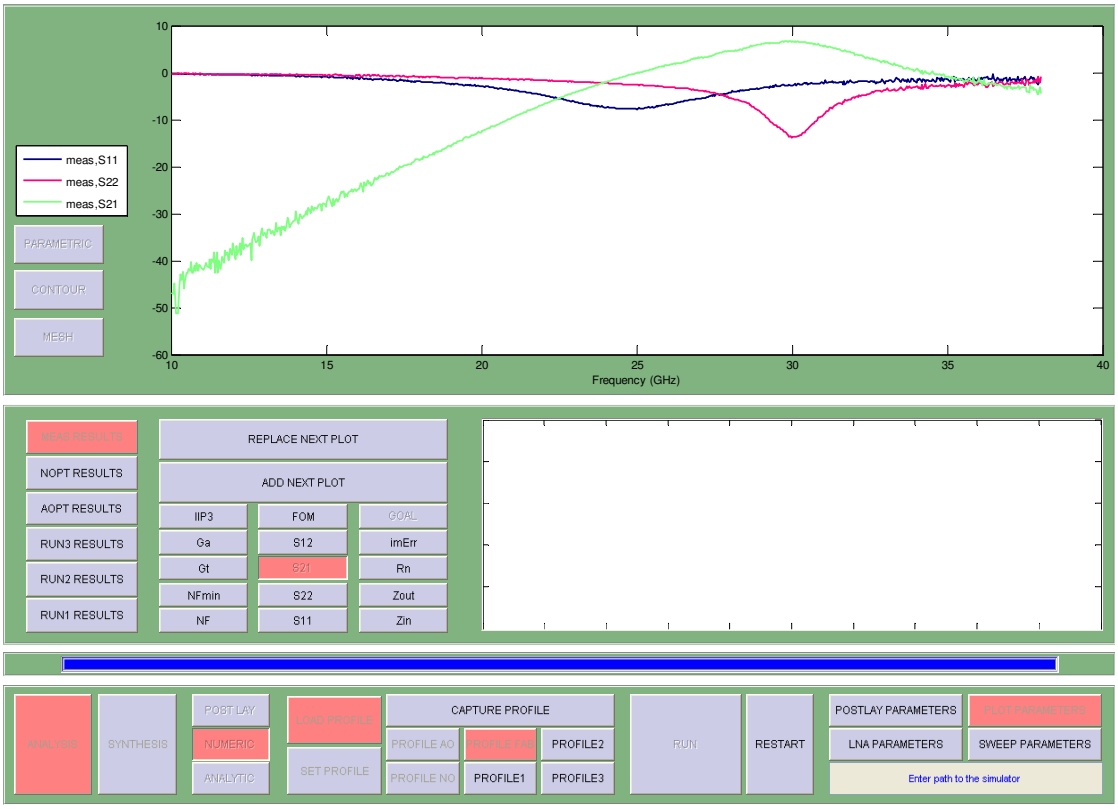


Fig. IV-16. Captured view of our design tool

Input and output matching networks may implemented in three ways:

- Matching using lumped elements (Spiral inductors and lumped capacitors)
- Matching with transmission lines
- Matching using lumped capacitors and line-type inductors

Various implementations have been compared in [66]. Matching using lumped elements is suitable for low frequency applications, although it has been advised and reported in recent years for mm-wave applications [93], [74], [72]. Main problem of this method is difficulties with design of spiral inductors in mm-wave frequencies. Matching with transmission lines is conventionally used in discreet RF circuit designs. This technique also has widely been used in mm-wave integrated circuits [74], [83], [85]. Transmission lines may be implemented as Coplanar Transmission Lines (CPTL) or micro-strip lines. CPTL has the advantage of less unwanted couplings from adjacent lines and higher impedance [87], [79]. However micro-strip lines have narrow lines that can be simply meandered and hence are area efficient. The most advantage of transmission lines are preventing the coupling to the substrate that is essential in CMOS technology, for which the substrate has low resistivity and causes considerable loss in high frequency. From this sense, micro-strip lines are more efficient than CPTL [85]. In general matching using transmission lines leads to very large chip area and hence it avoided, as long as possible.

Matching using lumped capacitors and line-type inductors combines the benefits of lumped element and transmission line matching implementations. By this way very compact and high quality factor matching network is obtained [90], [89]. We will use this implementation in our design. Combination of spiral and line-type inductors can be useful in cases that small and large inductors are used in the same circuit [89], [21].

Based on Fig. IV-4, the output matching network is accomplished using an standard T network. However for input matching, we have two options. One is Fig. IV-4(a), in which a series inductor has been used in gate, as in conventional cascode configuration [23], [94]. The second option is using shunt inductor in gate [90], [60]. To compare these two options, we investigate the practical implementation issue of matching inductors. As discussed, we will use line-type inductors. Line-type inductors can be designed as series or shunt inductors, as shown in Fig. IV-17. As this figure shows, shunt inductor makes possible to use a short-ended line-type inductor that has some advantages over series inductor. Shunt inductor leads to more compact layout, but if series inductor is used, the layout will be very large in one dimension and very small in other one. On the other hand shunt inductor is less susceptible for parasitic effects that can not be accurately modelled in design steps [90]. Another important advantage of shunt inductor over series inductor is the impedance transformation property of shunt inductor that relaxes the input matching offers freedom to choose the degenerating inductor. By this way the degenerating inductor is considered to comply with the linearity requirements and hence smaller degenerating inductor is needed, in comparison with series inductor matching. Using degenerating inductor reduces the gain and hence is a challenge in mm-wave LNA [79].

Based of the above suggestion, we have chosen the parallel inductor in the input matching network and hence our design will be similar to Fig. IV-4(b).

IV.4.1.2 DC Power Consumption

The second step of our design is estimating the required DC power consumption. This is accomplished based on the designers experience and the requirements of the system under design, in which the LNA will be used.

Thanks with our fast design tool that makes possible very fast design and optimization of cascode LNA, we examined many DC power consumptions to find the best value of DC power consumption. For this purpose we optimized our LNA with various DC powers and

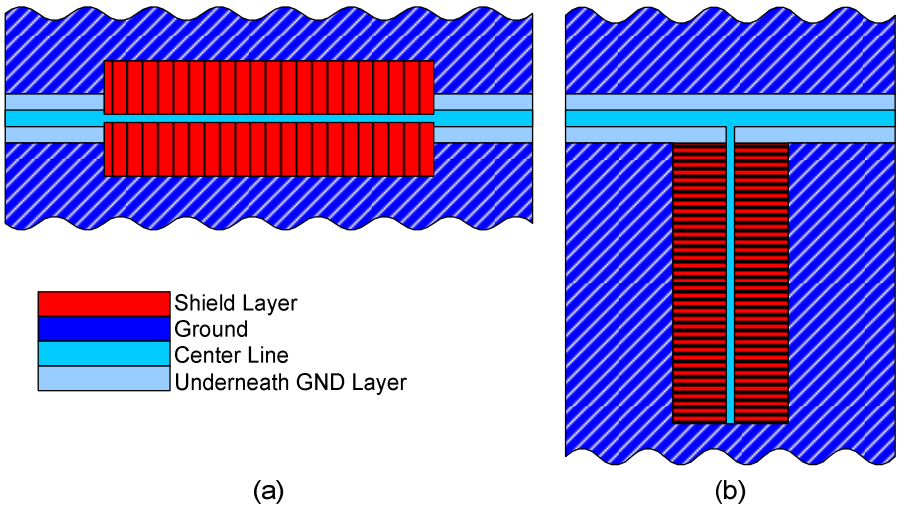


Fig. IV-17. Two different using of line-type inductors: (a)Serial and (b) shunt configurations.

then we compared the resulted maximum FOM of (IV-102) for each value of DC power consumption. The resulted comparison has been shown in Fig. IV-18. From this figure, 3-mW DC power is the best choice and hence is chosen in our design. It must be noted that this result has been obtained using the last version of our design tool that uses complete and accurate model of transistor. In the earlier versions, we had simpler models and different optimization strategy. Consequently we designed our first LNA (the fabricated LNA) for DC power of 4-mW.

IV.4.1.3 Optimization and Verification

After choosing the circuit configuration and DC power consumption, The LNA can be optimized using our design and simulation tool. As explained, the first step in this way is analytic optimization. Then an accurate numerical optimization is performed around the optimization variables value, obtained from analytic optimization. Finally the performance of designed LNA is verified using simulation with frequency sweep.

The performances of the designed LNA have been depicted in Fig. IV-19 to Fig. IV-21. S-Parameters have been shown in Fig. IV-19. This figure shows that minimum value of S_{11} and S_{22} are slightly different from the designed center frequency, i.e. 30 GHz. This is due to the

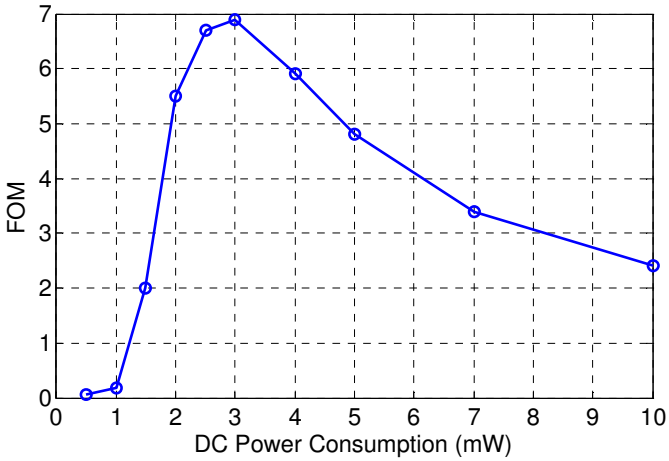


Fig. IV-18. Figure-of-Merit of our cascode LNA with different DC power consumptions

effect of the quality factor of inductors that are modelled more accurately in simulation mode. From this figure, maximum power gain is 14.5 dB and isolation is well acceptable in all of the band. Fig. IV-20(a) shows the operating power gain (G), in comparison with the available power gain (G_a). From this figure, at the center frequency G is equal to G_a. This implies good input and output matching design. Noise figure (NF) and minimum noise figure (NF_{min}) have been shown in Fig. IV-20(b). This figure shows that at the center frequency NF has the smallest difference from minimum noise figure. Note that NF_{min} is achieved if the optimum noise matching is satisfied in the input, that is contradictory with power matching and hence scarify the power gain. Two characteristics in Fig. IV-20, i.e. equal G and G_a, in addition with closest NF to NF_{min} proves the effectiveness of our optimization strategy. Linearity performance of the LNA has been depicted in Fig. IV-21. Although IIP3 equal to -12.5 dBm is not very good linearity, it is sufficient for our application, in which constant-envelope modulations will be used. FOM defined in (IV-102) has been shown in Fig. 21, from which deduced that the maximum FOM has been achieved at frequency slightly higher than the center frequency. However FOM at the center frequency is not so lower than the maximum value. One simple way to obtain maximum FOM at the center frequency is to shift the design frequency slightly lower than the desired center frequency. By this way maximum FOM is obtained, in expense of a little reduction of power gain and matching performance.

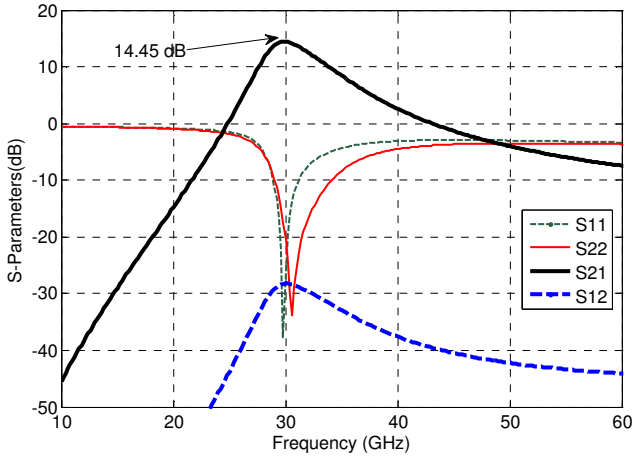


Fig. IV-19. S-Parameters of 3-mW, 30 GHz designed LNA

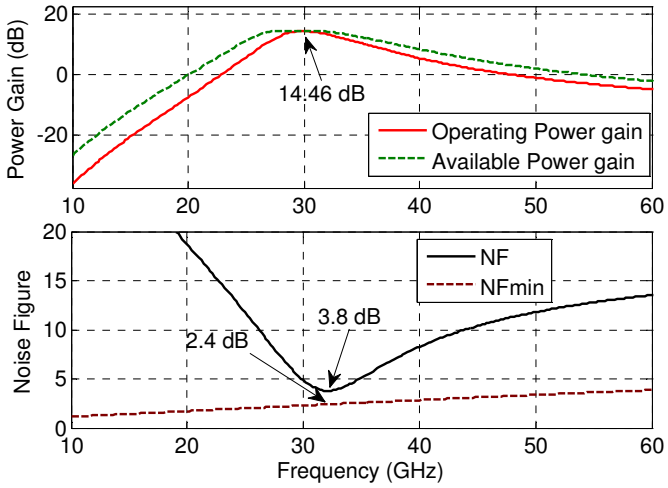


Fig. IV-20. Power gain and noise figure of 3-mW, 30 GHz designed LNA

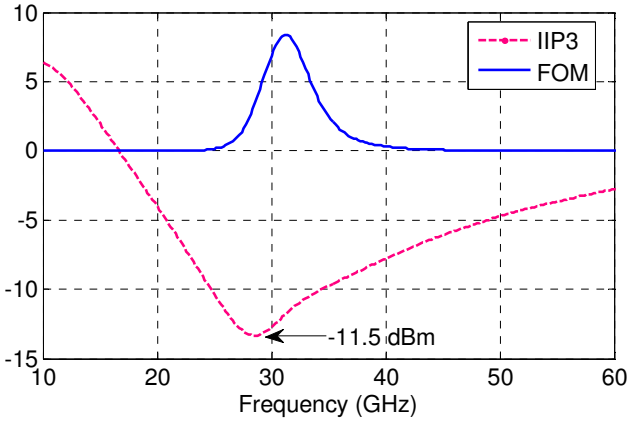


Fig. IV-21. IIP3 and FOM, defined in (IV-102), for 3-mW, 30 GHz designed LNA

IV.4.2 LNA Layout and Post Layout Simulation

IV.4.2.1 Layout Design

Layout design is very important in mm-wave circuits and may greatly affect the performance of the design. In the case of our work, this issue is very sever, since the available design kit for our work is a global purpose CMOS design kit that does not have any layout library or layout design guidelines for RF devices and elements. The catastrophe is that the extraction tool provided by the foundry design kit is not useful for our frequency band of interest. Consequently most of the layout design efforts and modeling layout effects must be accomplished by the designer.

The layout design can be divided into two categories: Active devices and passive elements. The layout issue of MOS transistor was investigated in Chapter II and the layout issue of inductors, transmission lines and RF pads were considered in Chapter III. The layout and layout model of MIM capacitors and different types of resistors are available in the design kit library and are enough accurate to be used in our design. The layout of other devices and elements were designed and modeled by ourselves. We have constructed an individual library of required devices and elements as Parametric Cells (PCELL) in Virtues layout design environment of CADENCE software, to which the foundry design kit has been attached. PCELL design provides the possibility of design of library elements with parameterized aspects and dimensions and each parameter can be redefined in each instantiation of the library part.

All of the layout design rules, provided by the foundry as the Design Rule Manual (DRM) must be complied for all layout elements. The most annoying rule in our design was the density rules for active, poly-silicon and metal layers. Density rules originate from technological points of view and each metal (or active or poly-silicon) layers have their individual maximum and minimum density limits, defined for different density calculation criteria. In a general purpose (digital or low frequency conventional analog designs) the designer uses the design kit layout library, for which all of the layout design rules have been complied and in special cases that one wants to use his/her individual layout, the only problem is to satisfy the maximum density limits. The reason is that the minimum density limits are complied by the automatic dummy insertion tool, provided in the foundry design kit. Unfortunately dummy metals perturbs the performance of devices and elements in RF design and hence automatic dummy insertion can not be used in RF and specially in mm-wave design. The only solution is that the layout be designed manually in accordance with all

of the design rules and the RF area of the layout be covered with no-dummy logical layers that prevent automatic dummy insertion.

Wide ground lines of transmission lines and inductors can not be routed as single wide lines. Instead the structure similar to Fig. IV-22(a) should be used. This figure shows the top and side cross section view. Remind that each ground line is actually a 3-dimentional structure, composed of stacked metal layers, each layer connected to the preceding layer by many via's. The via design is a complicated process and we have used PCELL design technique to correct instantiation of sufficient number of via elements, as well as routing error-less metal lines to construct a ground line with desired length and width. To laying out high impedance transmission lines, incorporated in line-type inductors, we have used the structure shown in Fig IV.22(b). By this way the line capacitance increases, but the line inductance remains almost unchanged. Consequently the reduction of the line impedance due to dummy elements is minimized. We have developed some mathematical procedures to analytical design of metal pieces in ground lines, dummy pats and RF pads.

Density rules are more sever in the case of RF pads. Pad design is an important and very complicated issue in layout design. Different types of pads have their individual requirements. Normally different types of pads are presented as library element in foundry design kit, with different features like optimum routing possibility, electrostatic discharge (ESD) protection, signal or power handling. A common requirement of all types of pads is mechanical strength. This is necessary to make the pad immune against the mechanical pressures due to probing or contacting. Consequently pads have their individual design rules that are more tighten that that of other sections. Due to vast area of pad, it has high coupling with substrate and hence

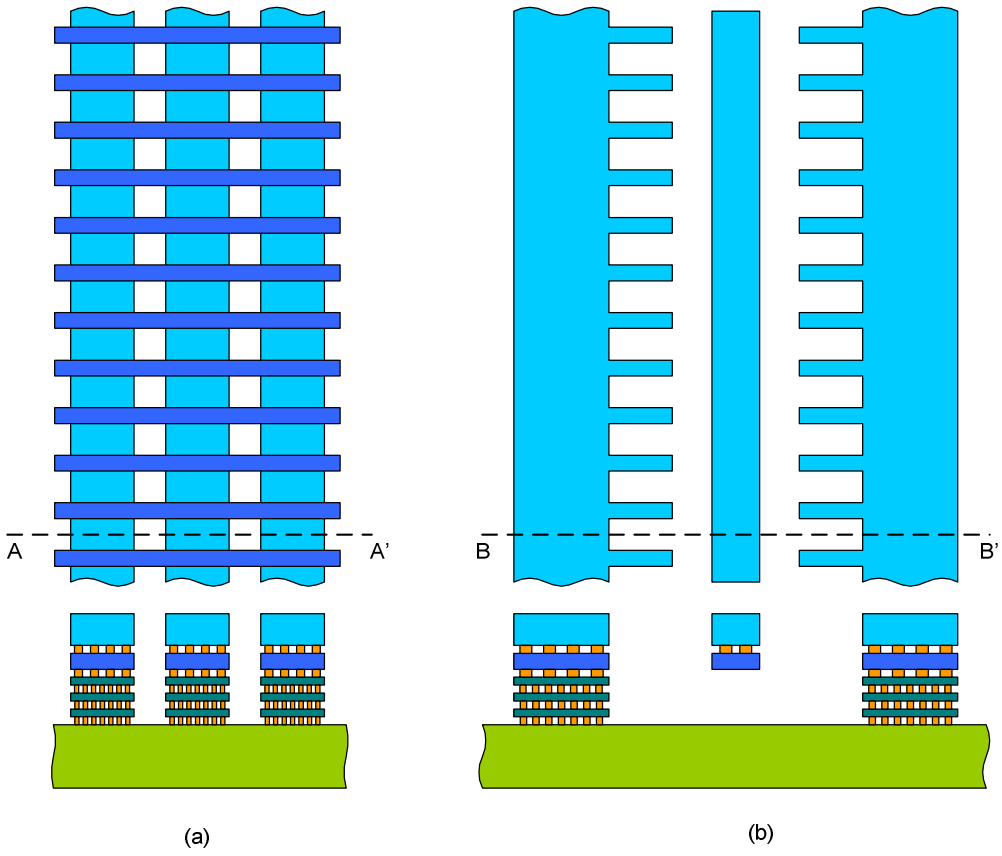


Fig. IV.22. Top view and cross section of wide ground line (a) and high impedance transmission line with special dummies, designed to minimize the line impedance reduction due to dummies.

the pads available in the design kit layout library are not useable for our design. So we have designed our RF pad to minimize the coupling and meanwhile satisfying the pad design rules. A simple representation of RF pad has been shown in Fig. IV.23. To reduce the substrate loss, the RF pad is surrounded by a ground ring of stacked metal line, as in Fig. IV-22(a). More details can be found in Chapter III.

Beside density rules, the rules related to minimum space of metal lines and via's are very important and many frequently cause design rules check error, if do not accurately considered. Metal line branches must be routed only in 900 or 450. This causes limitations in some cases. There is a class of special design rules, referred as Antenna design rules. This class of rules has been intended to consider the current density of metal lines and via's and to prevent the damages due to electro migration. Fortunately these rules are not important in our design, since the current lines are of enough width, very higher than the antenna rules limits. Actually these rules are important in very dense digital or low frequency designs.

The final layout of designed LNA has been shown in Fig. IV.24.

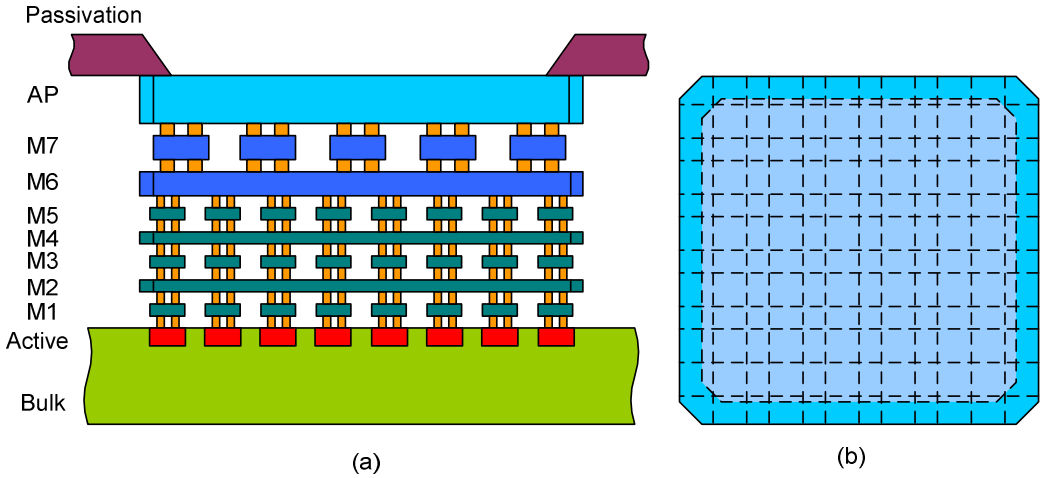


Fig. IV-23. (a) Layer stack (vertical cross section) and (b) top view of RF pad

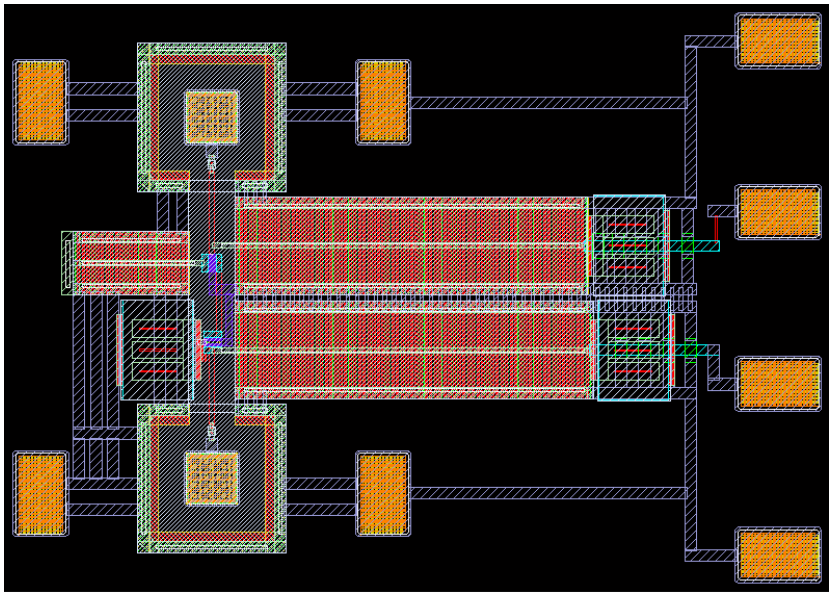


Fig. IV.24. Layout of designed LNA. The vide area outside of LNA core will be field with dummies by automatic dummy insertion process

IV.4.2.2 Post Layout Simulation

Post layout simulation of the designed LNA was performed regarding Fig. IV.15. In this simulation, complete MOS model and related parasitic, developed in Chapter II was used. Accurate modelling of parasitic effects and extraction of related parameters was performed with full wave simulation using Ansoft HFSS. For this purpose, we developed special programs to construct very complicated 3-dimensional structures in HFSS environment. The details have been explained in Chapter III.

The transmission line sections have been optimized using quasi-static models of transmission line, T-junction and line-type inductor, developed in Chapter III. In post layout simulation, the transmission lines and inductors was replaced with their quasi-TEM model. RF pads were modelled using the pad structure of Fig. IV.23, considering the surrounding ground ring, as in the final layout of Fig. IV.24. The details have been presented in Chapter III. The inductance and quality factor of the inductors in the input and output matching networks have been shown in Fig. IV.25.

Due to effect of RF pads, transmission lines and T-branches it is necessary to do some trimming in the length of line-type inductors, to obtain better performance. S-parameters of the LNA, obtained from post layout simulation after trimming, have been shown in Fig. IV.26. For comparison, S_{21} of pre-layout simulation, shown in Fig. IV.19, has been included in this figure. Bandwidth of post layout results is less than that of pre-layout simulation. This can be justified using the inductance and quality factor line-type inductor in Fig. IV.25. Actually and inductor never acts as an ideal inductor in high frequencies. Each inductor has a resonance frequency at which the quality factor of inductor decreases to zero. Beyond this frequency, the inductor acts as a capacitor. As the working frequency nears to the resonance frequency, the inductance and the quality factor has more sharp variations versus frequency and this is why the bandwidth in post layout simulation is narrower that pre-layout simulation, in which the resonance of inductors has not been considered. The input and output matching are holds simultaneously at the center frequency and hence the maximum power gain is achieved at the center of band.

Fig. IV.27 shows the noise figure, obtained from post layout simulation, in comparison with pre-layout simulation. The noise figure is slightly worst in the post layout simulation and the best noise figure is achieved at the frequency slightly higher than the center frequency.

Linearity and stability of the LNA, obtained from post layout simulation has been shown in Fig. IV.28. Rollett stability factor is defined as [101]:

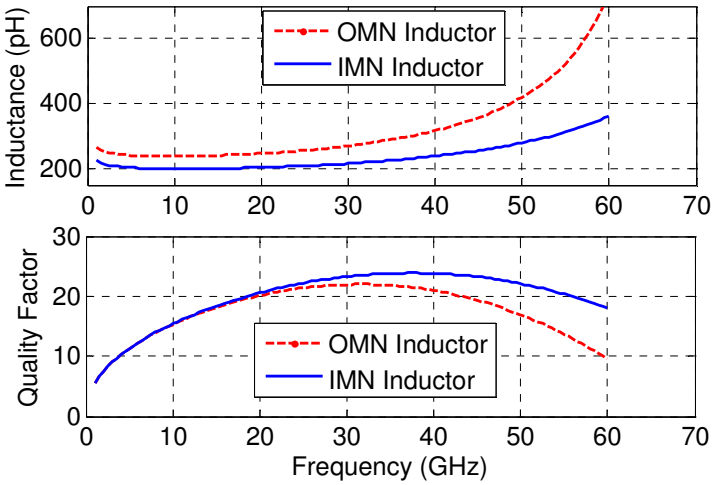


Fig. IV.25. Inductance and quality factor of line-type inductors in the input matching network (IMN) and output matching network (OMN).

$$K_f = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{11}||S_{22}|} \quad \text{(IV-122)}$$

Where:

$\Delta = S_{11}S_{22} - S_{21}S_{21}$

If $K_f > 1$, the circuit is unconditionally stable. Higher value of K_f implies higher stability. From Fig. IV.28 our design is unconditionally stable in all of the frequency below 60 GHz. Performance of designed LNA has been tabulated in Table IV-3.

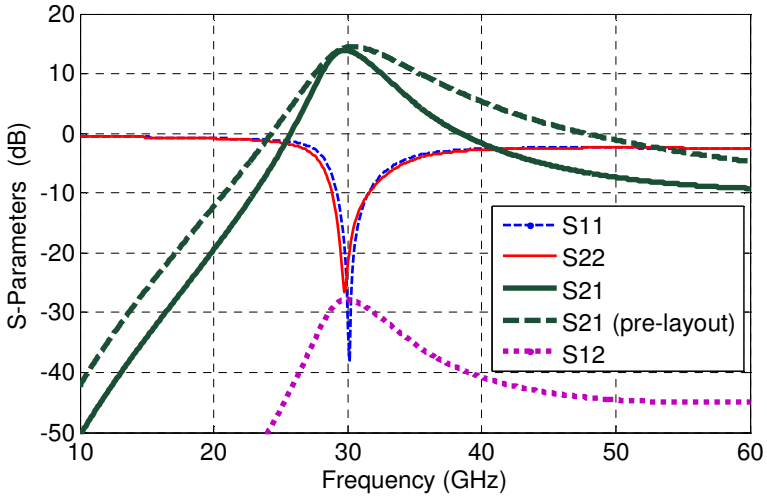


Fig. IV.26. Post layout simulation of optimized 3-mW LNA after trimming of inductors length. S21 of post layout simulation has been compared with pre-layout simulation.

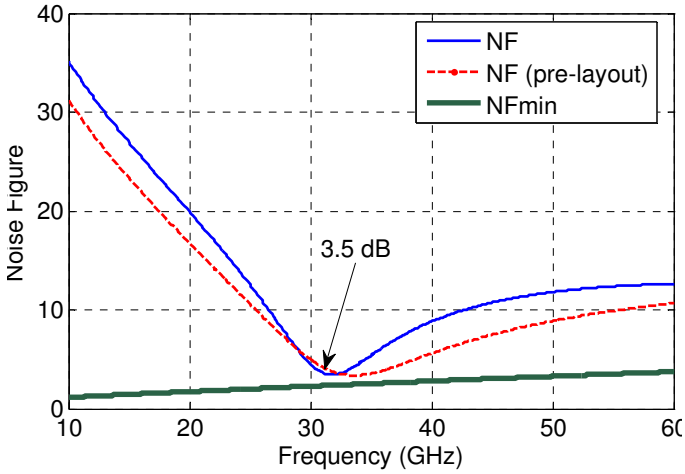


Fig. IV.27. Noise figure of post layout simulation, in comparison with pre-layout simulation

TABLE IV-3
Performance of the designed LNA at 31GHz, from post layout simulation

P_{DC}(mW)	S_{11}(dB)	S_{22}(dB)	S_{21}(dB)	S_{12}(dB)	G_a (dB)	NF (dB)	IIP3(dBm)	Kf	FOM*
3	-25	-26	13.8	-28	13.9	3.6	-9.8	2.8	2.48

*FOM has been defined in (IV-102)

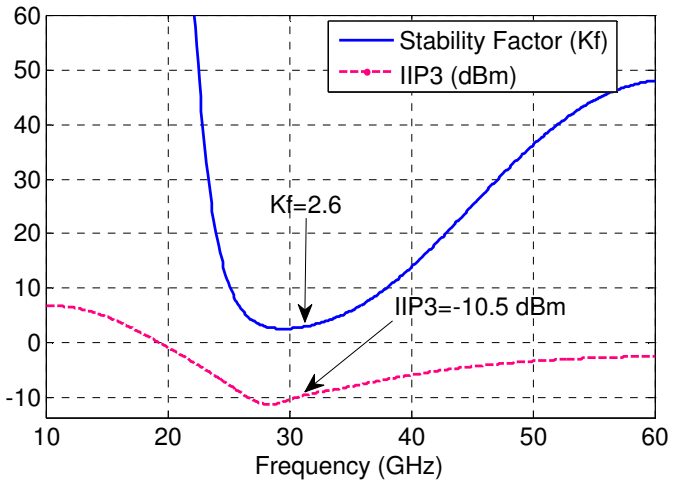


Fig. IV.28. Linearity and stability of the LNA, obtained from post layout simulation

IV.4.3 Fabricated LNA and the Measurement Results

IV.4.3.1 Design and Simulation

In 2006 we completed the design of the first version of our LNA in the STMicroelectronics 90nm Global Purpose (GP) CMOS process. As explained, this was the fist experience in the IMEP laboratory in bulk CMOS technology, in 30GHz band. Consequently we was obligated to develop a framework, consisting circuit design and optimization tool and layout facilities for mm-wave design in bulk CMOS foundry design kit. The layout of the designed LNA was completed in May 2006 and was sent to be fabrication by STMicroelectronics.

Based on our simulations, we found that 4-mW is the best choice for our work, in which power consumption is very important. This was based on the first version of our design tool. As we explained in section IV.4.1.2, we designed the last version of our LNA for 3-mW DC power consumption. The snap shot of the layout has been shown in Fig. IV.29.

Post layout simulation results of the fabricated LNA have been shown in Fig. IV.30. Unfortunately due to a mistake in layout of the input matching network, the performance of LNA was corrupted, as shown in Fig. IV.31. Since our layout process does not have the ability

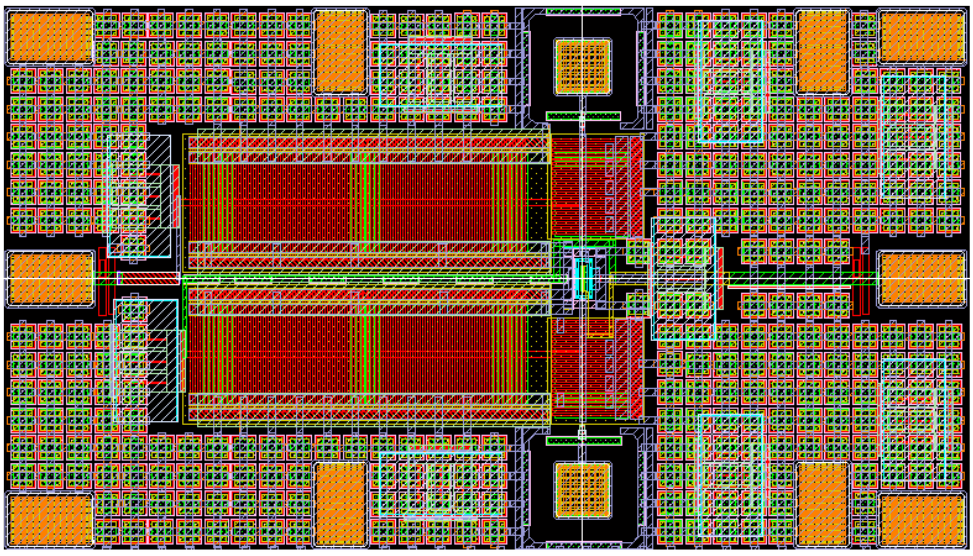


Fig. IV-29. The snap shot of the fabricated 4-mW LNA layout

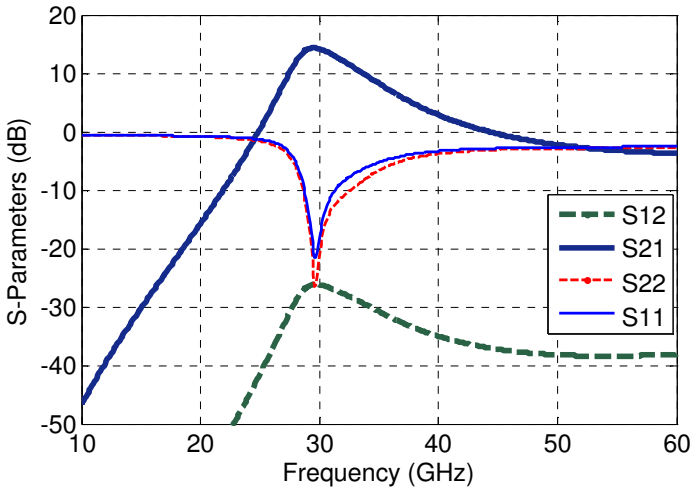


Fig. IV-30. S-Parameters of 4-mw LNA, obtained from post layout simulation

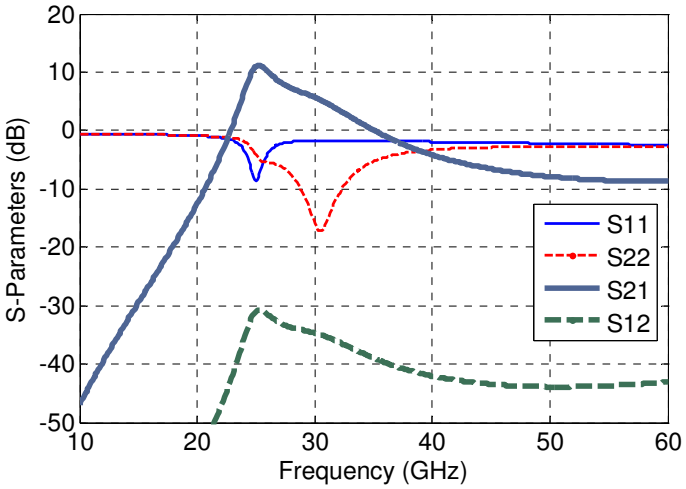


Fig. IV-31. S-Parameters of 4-mw LNA, obtained from post layout simulation, after incorporating the mistake in the input matching network layout

of automatic layout check, the mistake was not recognized. Remind that the standard layout check tools of the CADENCE could not be used in our work. Fig. IV.31 shows that the optimum input matching and the maximum gain has been shifted from 30 GHz to 25 GHz. Nevertheless, as we will show, using the measurement results, we can predict the performance of the LNA, if the mistake did not occur.

IV.4.3.2 Measurement Results

A) S-Parameter Measurement

Die photograph of the fabricated LNA has been shown in Fig. IV.32. LNA core area is equal to 0.1 mm^2 (400um×250um). S-Parameter measurement was performed using the available micro probe set, composed of:

- Agilent 8510C 40 GHz VNA[1],
- Karl Suss (KSM) microprobe system
- CASCADE MICROTECH microprobe tips, with 200 um pitch.

[1] Vector Network Analyzer

Before starting measurement, VNA and probing system must be calibrated. Calibration is very important in on-wafer measurements. Various calibration techniques, such as Short-Open-Load-Through (SOLT), Through-Reflect-Line (TRL) and Line-Reflect-Match (LRM) have been developed for microprobe systems [102], [103], [104]. Each microprobe systems has its individual calibration set for wafer level calibration, compose of (at least) three of four calibration sets, i.e. gold short circuits (Short), gold open pads (Open) and gold plus thin film resistors (Load or Match). These calibration sets, shown in Fig. IV.33, are fabricated on special substrate by the company or may designed as apart of the under-test chip by the circuit designer. Prior to measurements, S parameters of calibration sets are measured and special calibration program is run by VNA and determines twelve-term error model. In our measurement, LRM technique was used for calibration of VNA and probing system. LRM combines the advantages of old calibration techniques, such as SOLT and TRL [104]. In recent years, a new calibration method, named LRM+ has been presented by SUSS Micro Tec System [105], [106].

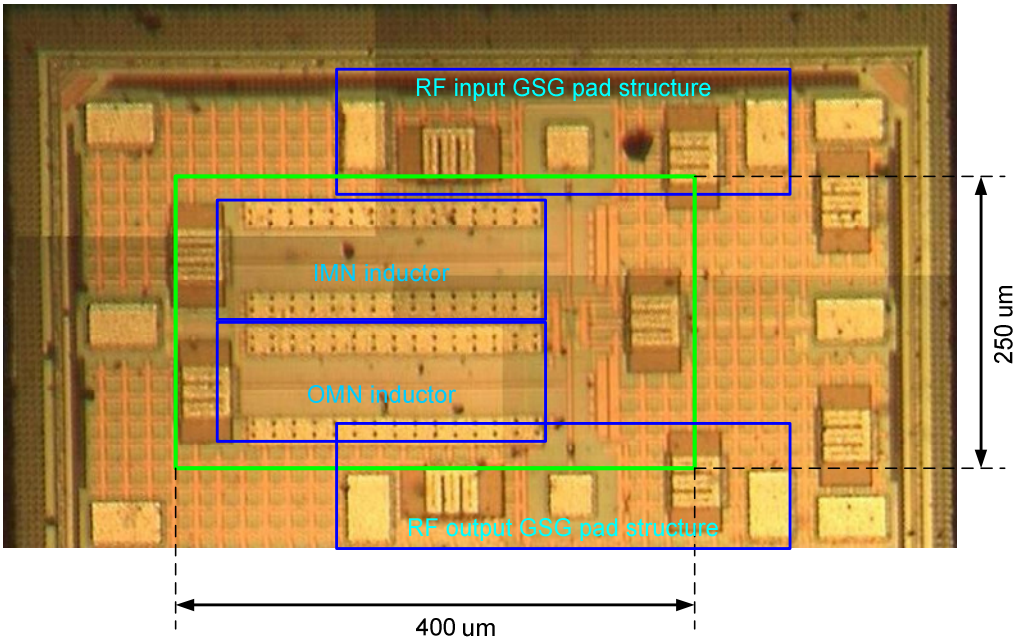


Fig. IV-32. Die photograph of the fabricated LNA. GSG (Ground-Signal-Ground) and matching inductors(IMN and OMN) have been marked on the figure.

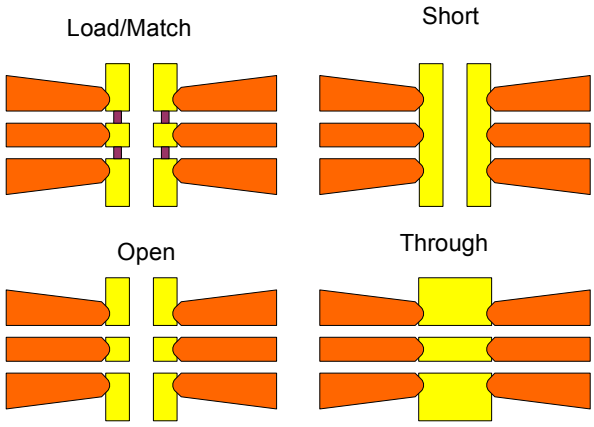


Fig. IV-33. Calibration standards, used for wafer level calibration of on-wafer RF measurement system [106].

The results of S-Parameter measurement have been shown in Fig. IV. 34. The maximum power gain and S_{22} are exactly at 30 GHz, proving the accuracy of our design. However, the optimum input matching (Minimum of S_{11}) has been shifted to 25 GHz. As explained, this is due to the mistake in placement of input matching inductor and was predicted with simulation by our design tool in Fig. IV.31.. The reverse isolation of LNA is very good and this proves the good stability of the LNA, as predicted by our simulation.

Operating power gain is defined as the ratio of power delivered to the load and the power delivered to the amplifier and is calculated as [101]:

$$G = \frac{\left(1-|\Gamma_L|^2\right)|S_{21}|^2}{\left(1-|\Gamma_{in}|^2\right)|1-S_{22}\Gamma_L|^2} \tag{IV-122}$$

Where:

$$\Gamma_S = \frac{Z_s - Z0}{Z_s + Z0}$$
$$\Gamma_L = \frac{Z_L - Z0}{Z_L + Z0} \tag{IV-123}$$

And:

$$\Gamma_{in} = S_{11} + \frac{S_{21}S_{12}\Gamma_L}{1-S_{22}\Gamma_L} \tag{IV-124}$$

Since in our work Z_L and Z_s are equal to the reference impedance, Γ_S and Γ_L are zero and hence (IV-122) reduces to:

$$G = \frac{|S_{21}|^2}{1-|S_{11}|^2} \tag{IV-125}$$

Operating power gain of the LNA, calculated from measured S-parameters, has been shown in Fig. IV.35. From this figure, peak power gain of 10dB occurs exactly at the designed center frequency, i.e. 30 GHz.

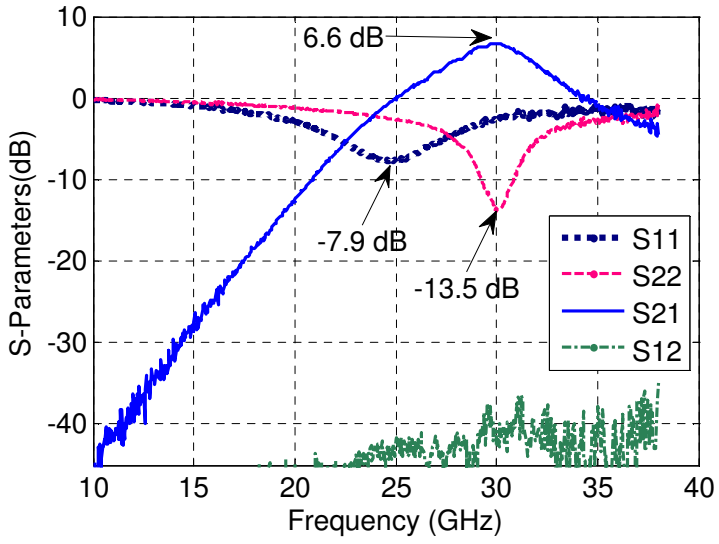


Fig. IV-34. Measured S-parameters of our fabricated 4-mW LNA. Due to the mistake in the input matching network layout, S_{11} has been shifted from 30 GHz and S_{21} has been reduced.

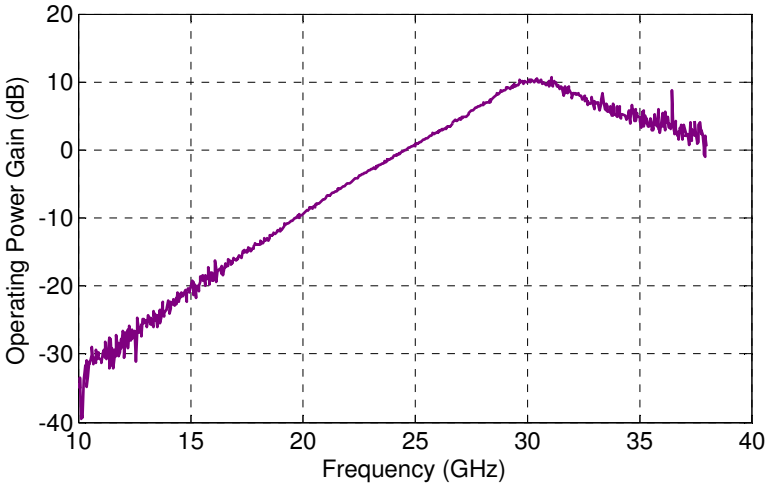


Fig. IV-35. Measured power gain of our fabricated 4-mW LNA

To evaluate the parasitic aware simulation in Spectre-RF and the attached foundry design kit, we have simulated the LNA, after adding post layout parasitic effects and using lumped model of transmission lines and inductors. The simulated circuit has been shown in Fig. IV.36. On the other hand to evaluate our design tool, we have performed the post layout simulation using our design tool.

In Fig. IV-37, S-parameters obtained from measurement have been compared with post layout simulation results, using our design tool and using the foundry design kit, attached to Spectre-RF simulator. This figure shows that the results of our design tool is more close to the measurement results, than the Spectre-RF results. The reason is that although we have added post layout parasitic to the LNA circuit in Spectre-RF, there is inherit limitation in modeling substrate effect in BSIM3v3 model that has been used in Spectre-RF simulation. Actually in Spectre-RF, we have not access to the internal substrate nodes. This comparison validates our design tool and hence we are sure about our last designed LNA.

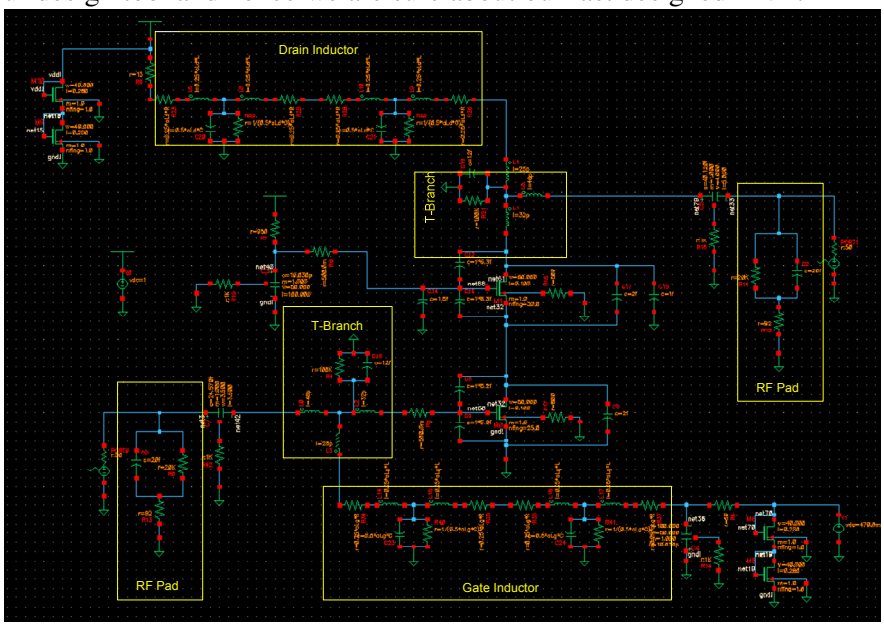


Fig. IV-36. Schematic of the LNA circuit for post layout simulation in CADENCE with SpecreRF simulator

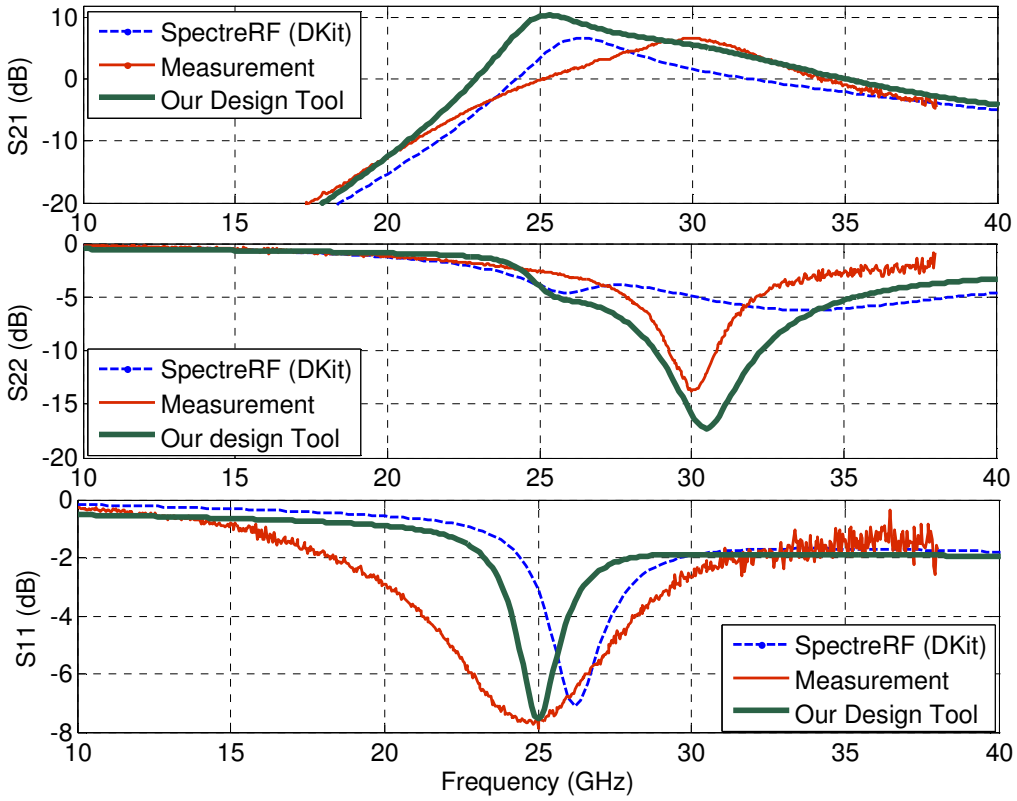


Fig. IV-37. S-parameters, obtained from measurement, in comparison with post layout simulation using our design tool and the foundry design kit, attached to CADENCE.

B) Noise figure measurement

Noise figure measurement was carried out using Agilent N8975A noise figure analyzer. Unfortunately the maximum measurement frequency of this noise figure analyzer is 26.5 GHz. The measurement result has been shown in Fig. IV-38 and has been compared with the simulation results using our design tool. From this figure, the simulation results have very good agreement with measurement results.

We tried to do the measurement with other measurement methods. Besides using standard noise figure analyzer, there are two noise figure measurement methods that are used in practical applications. These methods are named as Y-factor method and gain method [107]. The measurement setups for these methods have been depicted in Fig. IV-39. Y-factor method needs to standard noise source with the maximum frequency more than the DUT[1]. Since such standard noise source was not available for us, we could not use this method. Instead we examined the gain method.

In gain method, the input port to the DUT is terminated to reference impedance (50Ω for RF systems). Then the output of DUT will the amplified noise, due to the 50 Ω source and the inherit noise of DUT. The DUT output is amplified using a high gain amplifier, so that the DUT output noise power can be measured with a spectrum analyzer. Then we have:

$$NF = P_{noDUT} - \left(-174dBm/Hz + 10\log(BW) + G\right)$$

P_{noDUT} is the output noise power of DUT, -174dBm is the noise density of ambient noise (290 K^0) BW is the DUT bandwidth and G is the measurement system gain.

[1] Device Under test

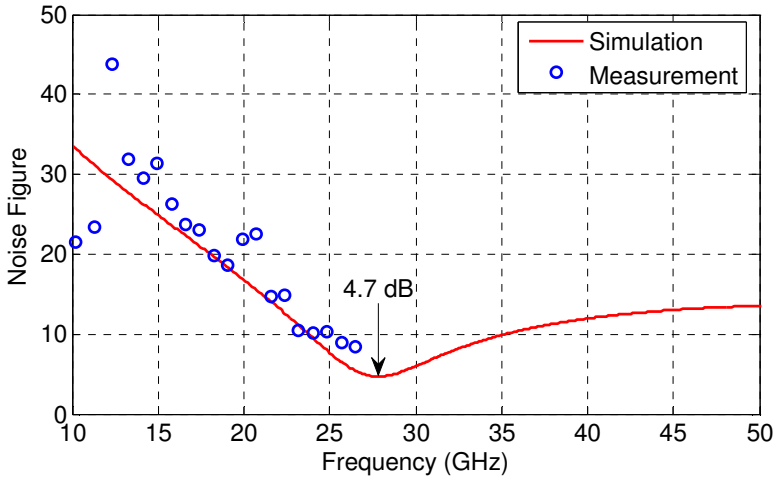


Fig. IV-38. Measured noise figure of the fabricated LNA, in comparison with post layout simulation using our design tool

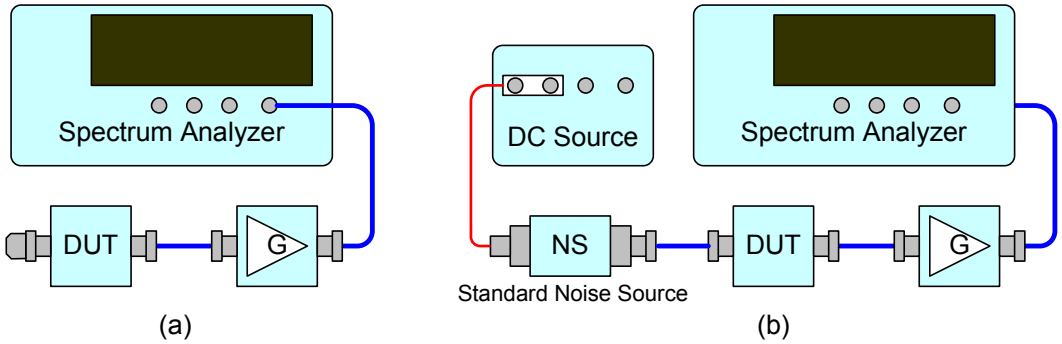


Fig. IV-39. Noise figure measurement with gain method (a) and Y-factor method (b) [107].

If we measure directly the power density, instead of total power, this equation can be simplified to:

$$NF = P_{noDUT}(dBm/Hz) + 174dBm/Hz - G$$

The limitation of gain method comes from the noise floor of the spectrum analyzer. We used Anritsu MS2668C, the available spectrum analyzer in the laboratory, in conjunction with extra 40dB gain. Unfortunately the noise floor of the spectrum analyzer was -84dBm/Hz, and was not sufficient for our measurement. So, an Agilent spectrum analyzer with noise floor of -150dBm/Hz should be used, that was not available for us.

C) Linearity Measurement

IIP3 conventionally is used for express the linearity of LNA. To measure this parameter, the outputs of two RF sources are combined and applied to LNA. The RF sources outputs are same power, in the LNA frequency band and with a small frequency difference. Then the power of desired signal and the 3rd order inter-modulation terms are measured using a spectrum analyzer.

P1dB is also used for express the linearity of LNA. Since two RF sources were not available for our measurements, we measured P1dB, instead of IIP3. The measurement results have been shown in Fig. IV-40. From this figure, at the 1dB compression point, the input power (IP1dB) and the output power (OP1dB) are -9.7 and -3.8, respectively.

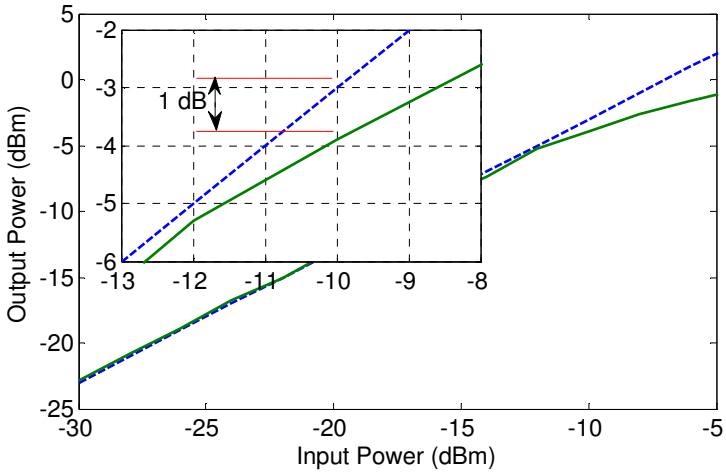


Fig. IV-40. Compression point measurement of the fabricated LNA

D) Comparison with Reported Works

In recent years, many mm-wave LNAs have been reported in different technologies. Among the reported works, we have tabulated the reported LNAs in CMOS technologies, in 30GHz band. For comparison of different designs we have used the conventionally used figure-of-merit of (IV-101). The comparison has been performed in Table IV-4. Due to leak of reported characteristics, FOM can not be calculated for some of listed cases. This table shows that the chip are of our LNA is a record, in thanks with the line-type inductors we have

TABLE IV-4
Comparison of our fabricated and designed LNA with the reported LNAs in 30GHz band

Reference	[90] F. Elinger	[91] Dupuis et *al.*	[85] Tsai et *al.*	[86] Sanduleanu et *al.*	[88] Yu Su et *al.*
Year	2004	2005	2006	2006	2006
Number of Stages	1	1	3	2	1
Process	90nm (SOI) CMOS	90nm (RF) CMOS+WLP	130nm CMOS	90nm CMOS	130nm CMOS
Peak Gain (dB)	11.9@35GHz	7.5@24GHz	20@43GHz	18.6@33GHz	8.4@26.2GHz
NF (dB)	3.6@35GHz	3.2@24GHz	6.3@41GHz	3@33GHz	4.8@26.2GHz
OP1dB (dBm)	4	N/A	4	N/A	N/A
IIP3 (dBm)	N/A	N/A	-5.5	N/A	-13
DC Power (mW)	40.8	10.6	36	10	0.8
3-dB BW	16	7	10	3	3.7
Chip Area (mm^2)	0.18	2.1	0.525	0.856	N/A
FOM	-----	-----	2.397	-----	0.794

Reference	[93] S. Yen et *al.*	[87] Niknejad et *al.*	This Work (Fabricated)	This Work (Simulated)
Year	2006	2007	2006	2008
Number of Stages	3	2	1	1
Process	180nm CMOS	90nm CMOS	90nm CMOS	90nm CMOS
Peak Gain (dB)	10.2@32GHz	20@28.5GHz	10@30GHz	13.9*@30GHz
NF (dB)	4.62@32GHz	2.9@28GHz	4.7	3.4*
OP1dB (dBm)	3.6	2	-3.8	-----
IIP3 (dBm)	3	-7.5	-9.7*	-10*
DC Power (mW)	27	16.25	4	3*
3-dB BW (GHz)	9	2.5	4.7	3.8*
Chip Area (mm^2)	0.37	0.67	0.1	0.1*
FOM	3.671	2.88	0.645	2.618

* Post layout simulation

developed and used in our design. The chip area for all of the cases, is the area of LNA core, excluding the input-output pads area.

Regarding Table IV-4, the reported multi-stage LNAs have higher FOM, in comparison with single-stage LNAs. This can be intuitively explained by noting that for cascaded, identical gain stages, the total gain increases exponentially with the number of stages whereas power consumption increases linearly [108]. This is the basis of the Meindle-Hudson criteria to optimize the number of RF gain stages in a receiver front end [109]. On the other hand, in the FOM defined in (IV-101), both of the gain and power are absolute value. As an example, suppose two LNAs: First LNA is a single stage with 10dB gain and 5mW power consumption and the second one is a two-stage LNA, each stage is exactly the same as the first LNA. So, the gain and power consumption of the second LNA is 20dB and 10mW, respectively. Then regarding (IV-101), FOM of the second LNA is two times of the first LNA, in spite that two LNAs use the same circuits. This explanation reveals that the conventional FOM of (IV-101) is valid only for the LNAs with equal number of stages. It must be noted that two stage LNAs can not be used in ultra-low power applications, due to their inherently high power consumptions.

As a consequence of the above suggestion, we have re-tabulated the recently reported single stage LNAs in Table IV-5. Among the compared LNAs, the FOM is calculated only for the LNA of [88], due to leak of IIP3 performance for the others. Comparison of our fabricated LNA with that of [88] shows that our work is acceptable, as our first experience. Note that this is despite of the mistake of placement in layout of our LNA, as explained previously. Our post layout simulation (last column of the table) shows that if the mistake did not occur, then our design could achieve very good performance. To be able to compare all of the reported works of Table IV-5, we have recalculated the FOM, after dropping IIP3 from FOM definition of (IV-101). This is acceptable in our work, since the linearity is not crucial in WSN applications. Then the table shows that our fabricated LNA has better performance than [90] and [91]. And our last design, has superior performance!! Actually its performance is well comparable with two-stage LNA of Niknejad et *al.*, reported in 2007.

TABLE IV-5
Comparison of our fabricated and designed LNA with the reported single stage LNAs in 30GHz band

Reference	[90] F. Elinge	[91] Dupuis et *al.*	[88] Yu Su et *al.*	This Work (Fabricated)	This Work (Simulated)
Year	2004	2005	2006	2006	2008
Number of Stages	1	1	1	1	1
Process	90nm (SOI) CMOS	90nm (RF) CMOS+WLP	130nm CMOS	90nm CMOS	90nm CMOS
Peak Gain (dB)	11.9@35GHz	7.5@24GHz	8.4@26.2GHz	10@30GHz	13.9@30GHz
NF (dB)	3.6@35GHz	3.2@24GHz	4.8@26.2GHz	4.7	3.4
OP1dB (dBm)	4	N/A	N/A	-3.8	-----
IIP3 (dBm)	N/A	N/A	-13	-9.7*	-10
DC Power (mW)	40.8	10.6	0.8	4	3
3-dB BW	16	7	3.7	4.7	3.8
Chip Area (mm^2)	0.18	2.1	N/A	0.1	0.1
FOM	-----	-----	0.794	0.645	2.618
FOM**	4.705	3.409	15.841	6.022	26.188

* Post layout simulation
** FOM without IIP3

References

[1] Sudip Shekhar, Jeffery S. Walling, Sankaran Aniruddhan and David J. Allstot, "CMOS VCO and LNA using tuned-input tuned-output circuits," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp.1177-1186, may 2008.

[2] Asad A. Abidi, "RF CMOS comes of age," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 4, pp. 549-561, April 2004.

[3] Xiaohua Fan, Heng Zhang, and Edgar Sánchez-Sinencio, "A noise reduction and linearity improvement technique for a differential cascode LNA," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 3, pp. 588-599, March 2008.

[4] W. Zhuo, S. H. K. Embabi, J. Pineda de Gyvez, and E. Sánchez-Sinencio, "Using capacitive cross-coupling technique in RF low-noise amplifiers and down-conversion mixer design," *In Proceedings of the European Solid-State Circuits Conference (ESSCIRC)*, pp. 116–119, Sept. 2000.

[5] X. Li, S. Shekhar, and D. J. Allstot, "Gm-boosted common-gate LNA and differential Colpitts VCO/QVCO in 0.18-_m CMOS," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2609–2619, Dec. 2005.

[6] W. Zhuo, X. Li, S. Shekhar, S. H. K. Embabi, J. Pineda de Gyvez, D. J. Allstot, and E. Sánchez-Sinencio, "A capacitor cross-coupled common-gate low noise amplifier," *IEEE Transaction on Circuits and Systems II: Express Briefs*, vol. 52, no. 12, pp. 875–879, Dec. 2005.

[7] Wei-Hung Chen, Gang Liu, Boos Zdravko and Ali M. Niknejad, "A highly linear broadband CMOS LNA employing noise and distortion cancellation," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1164-1176, May 2008.

[8] Ke-Hou Chen, Jian-Hao Lu, Bo-Jiun Chen, and Shen-Iuan Liu, "An ultra-wide-Band 0.4–10-GHz LNA in 0.18um CMOS," *IEEE Transaction on Circuits and Systems II: Express Briefs*, vol. 54, no. 3, pp. 217-221, March 2007.

[9] Mikaël Cimino, Hervé Lapuyade, Yann Deval, Thierry Taris and Jean-Baptiste Bégueret, "Design of a 0.9 V 2.45 GHz self-testable and reliability-enhanced CMOS LNA," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1187-1194, May 2008.

[10] Asad A. Abidi, "On the Operation of Cascode Gain Stages," *IEEE Journal of Solid-State Circuits*, vol. 23, no. 6, pp. 1434-1437, Dec. 1988.

[11] V. Govind, S. Dalmia, and M. Swaminathan, "Design of integrated Low Noise Amplifiers (LNA) using embedded passives in organic substrates," *IEEE Transaction on Advanced Packaging*, vol. 27, no. 1, pp. 79-89, Feb. 2004.

[12] Hyejeong Song, Huijung Kim, Kichon Han, Jinsung Choi, Changjoon Park, and Bumman Kim, "A sub-2 dB NF dual-band CMOS LNA for CDMA/WCDMA applications," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 3, pp. 212-214, March 2008.

[13] Choong-Yul Cha and Sang-Gug Lee, "A 5.2-GHz LNA in 0.35um CMOS utilizing inter-stage series resonance and optimizing the substrate resistance," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 4, pp. 669-672, April 2003.

[14] Andrea Bevilacqua, Christoph Sandner, Andrea Gerosa, and Andrea Neviani , "A fully integrated differential CMOS LNA for 3–5-GHz ultra-wideband wireless receivers," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 3, pp. 134-136, March 2006.

[15] R. G. Meyer and W. D. Mack, "A 1-GHz BiCMOS RF front-end IC," *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 350-355, March 1994.

[16] H. Samavati, H. R. Rategh, and T. H. Lee, "A 5-GHz CMOS wireless LAN receiver front-end," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 5, pp. 765-772, May 2000.

[17] Junji Wadatsumi, Shouhei Kousai, Daisuke Miyashita and Mototsugu Hamada, "A 1.2V, 0.1-6.0 GHz, two-stage differential LNA using gain compensation scheme," *In Proceedings of the IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF 2008)*, pp. 175-178, Jan. 2008.

[18] Bevin G. Perumana1, Jing-Hong C. Zhan1, Stewart S. Taylor1, Brent R. Carlton1, and Joy Laskar, "A 9.2 mW, 4-8 GHz resistive feedback CMOS LNA with 24.4 dB gain, 2 dB noise figure, and 21.5 dBm output IP3," *In Proceedings of the IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF 2008)*, pp. 206-209, Jan. 2008.

[19] Tamer Ragheb, Arthur Nieuwoudt, and Yehia Massoud, "Modeling of 3.1-10.6 GHz CMOS filter-based lLow noise amplifier for ultra-wideband receivers," *In Proceedings of the IEEE Annual Wireless and Microwave Technology Conference (WAMICON 20'06)*, pp. 1-5, Dec. 2006.

[20] Wang Peng, Hao Qing, Wang Jian, Chen Yaqin, "Design of C-band low noise amplifier with switch," *In Proceedings of the IEEE International Conference on Microwave and Millimeter Wave Technology (ICMMT '07)*. pp. 1-3, April 2007.

[21] Christopher Weyers, Pierre Mayr, Johannes W. Kunze, "A 22.3dB voltage gain 6.1dB NF 60GHz LNA in 65nm CMOS with differential output," *IEEE International Solid-State Circuits Conference (ISSCC 2008), Digest of Technical Papers,* pp. 192-606, Feb. 2008.

[22] Chieh-Min Lo, Chin-Shen Lin, Huei Wang, "A miniature V-band 3-stage cascode LNA in 0.13μm CMOS," *IEEE Solid-State Circuits Conference*, pp. 1254-1263, Feb. 6-9, 2006.

[23] Terry Yao1, Michael Gordon, Kenneth Yau1, M.T. Yang, and Sorin P. Voinigescu, "60-GHz PA and LNA in 90-nm RF-CMOS," *In Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC2006)*, pp. 4, June 2006.

[24] Derek K. Shaeffer, and Thomas H. Lee, "A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 5, pp. 745-759, May 1997.

[25] Yiqun Cao, Vadim Issakov, and Marc Tiebout, "A 2kV ESD-Protected 18GHz LNA with 4dB NF in 0.13um CMOS," *IEEE Solid-State Circuits Conference (ISSCC 2008), Digest of Technical Papers*. pp. 194-606Feb. 2008.

[26] Hong Zhang, Guican Chen, Xiao Yang, "Fully differential CMOS LNA and down-conversion mixer for 3-5 GHz MB-OFDM UWB receivers," *In Proceedings of the IEEE International Workshop on Radio-Frequency Integration Technology*, pp. 54-57, Dec. 2007.

[27] D. K. Shaeffer and T. H. Lee, "Corrections to "A 1.5 V, 1.5 GHz CMOS low-noise amplifier," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 6, pp. 1397-1398, Jun. 2005.

[28] T. K. Nguyen, C. H. Kim, G. J. Ihm, M. S.Yang, and S. G. Lee, "CMOS low-noise amplifier design and optimization tehcniques," *IEEE Transaction on Microwave Theory and Techniques*, vol. 52, no. 5, pp. 1433-1442, May 2004.

[29] T. H. Lee, "*The Design of CMOS Radio-Frequency Integrated Circuits*," Cambridge, U.K., Cambridge Univ. Press, 1998.

[30] Huseyin S. Savci, Zheng Wang, Ahmet Sula, Numan S. Dogan, "A 1-V UHF low noise amplifier for ultralow-power applications," *In Proceedings of the IEEE International Symposium on Circuit and Systems (ISCAS2006)*, pp. 4495-4498, 2006.

[31] Saman Asgaran, M. Jamal Deen, and Chih-Hung Chen, "A 4-mW monolithic CMOS LNA at 5.7 GHz with the gate resistance used for input matching," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 4, pp. 188-190April 2006.

[32] Domenico Zito, Domenico Pepe, Bruno Neri, Thierry Taris, Jean-Baptiste Begueret, Yann Deval, Didier Belot, "A novel LNA topology with transformer-based input integrated matching and its 60-GHz millimeter-wave CMOS 65-nm design," *In Proceedings of the IEEE International Conference on Electronics, Circuits and Systems (ICECS 2007)*. pp. 1340-1343Dec. 2007.

[33] M. Battista, J. Gaubert, M. Egels, S. Bourdel and H. Barthe´lemy, "6-10 GHz ultra-wideband CMOS LNA," *Electronics Letters*, vol. 44, pp. 343-344, Feb. 28 2008.

[34] George S. A. Shaker, Mohammad-Reza Nezhad-Ahmadi, S. Safavi-Naeini1, Gareth Weale, "Direct matching of a miniaturized antenna to an on-chip low noise amplifier," *In Proceedings of the IEEE Radio and Wireless Symposium*, pp. 387-390, Jan. 2008.

[35] U. Alvarado, N. Rodriguez, J. Mendizabal, R. Berenguer, G. Bistue, "A dual-gain ESD-protected LNA with integrated antenna sensor for a combined GALILEO and GPS front-end," *In Proceedings of the IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 99-102, Jan. 2007.

[36] Daisuke Ueo, Hiroshi Osabe, Koji Inafune, Masayuki Ikebe, Eiichi Sano, Masato Koutanit, Masayuki Ikedat, and Koichiro Mashikot, "7-GHz inverted-F antenna monolithically integrated with CMOS LNA," *In Proceedings of the IEEE International Symposium on Intelligent Signal Processing and Communications (ISPACS '06)*, pp. 259-262,Dec. 2006.

[37] Y. T. Lin, T. Wang and S. S. Lu, "Fully integrated concurrent dual-band low noise amplifier with suspended inductors in SiGe 0.35um BiCMOS technology," *Electronics Letters*, vol. 44, Issue 9, pp. 563-564, April 2008.

[38] Ro-Min Wengi, Ron-Chi Kuoi, Po-Cheng Liun, "An ultra-wideband LNA with notch filter," *In Proceedings of the IEEE 17th Radioelektronika International Conference*, pp. 1-4, April 2007.

[39] Yu-Tso Lin, Tao Wang and Shey-Shi Lu, "A fully integrated concurrent dual-band low noise amplifier with suspended inductors in SiGe 0.35um BiCMOS technology," *In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS 2007)*, pp. 425-428, May 2007.

[40] Ahmed Amer, Emad Hegazi, and Hani F. Ragaie, "A 90-nm wideband merged CMOS LNA and mixer exploiting noise cancellation," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 2, pp. 323-328, Feb. 2007.

[41] Chih-Fan Liao, Shen-Iuan Liu, "A broadband noise-canceling CMOS LNA for 3.1-10.6-GHz UWB receivers," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 2, pp. 329-339, Feb. 2007.

[42] Chao-Shiun Wang, Chorng-Kuang Wang, "A 90nm CMOS low noise amplifier using noise neutralizing for 3.1-10.6GHz UWB system," *In Proceedings of the 32nd European Solid-State Circuits Conference (ESSCIRC 2006)*, pp. 251-254, Sept. 2006.

[43] Feng Lu, Lei Xia, "A CMOS LNA with noise cancellation for 3.1-10.6 GHz UWB receivers using current-reuse configuration," *In Proceedings of the 4th IEEE International Conference on Circuits and Systems for Communications (ICCSC 2008),* pp. 824-827, May 2008.

[44] Ameir Fanei, Philippe Pannier, Jean Gaubert, Marc Battista, Yannick Bachelet, "Experimental results and EM simulation of substrate noise in wideband low noise amplifier for UWB systems," *In Proceedings of the International Conference on Design & Technology of Integrated Systems in Nanoscale Era*, pp. 192-195, Sept. 2007.

[45] A. Fanaei, Ph. Pannier, J. Gaubert, M. Battista, and Y. Bachelet, "Substrate noise in LC-matched ultra wide-band low noise amplifier of UWB systems," *In Proceedings of the IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC 2007)*, pp. 469-472, Dec. 2007.

[46] Kyoungchoul Koo, Hyunjeong Park, Yujeong Shim and Joungho Kim, "Noise figure degradation analysis of power/ground noise on 900MHz LNA for UHF RFID," *In Proceedings of the IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC 2007)*, pp. 1021-1023, Dec. 2007.

[47] Seungyong Lee, Kihan Kim, Tae Hyun Oh, Ickhyun Song, Hyungcheol Shin, Moonil Kim, and Jae-Sung Rieh, "Suppression of digital noise coupling on LNA in 0.13um RFCMOS technology by global guard rings," *In Proceedings of the IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF 2008)*, pp. 206-209, Jan. 2008.

[48] A. Abidi, "General relations between IP2, IP3, and offsets in differential circuits and the effects of feedback," *IEEE Transaction on Microwave Theory and Techniques*, vol. 51, no. 5, pp. 1610-1612, May 2003.

[49] Trung-Kien Nguyen, Nam-Jin Oh, Choong-Yul Cha, Yong-Hun Oh, Gook-Ju Ihm, and Sang-Gug Lee, "Image-rejection CMOS low-noise amplifier design optimization techniques," *IEEE Transaction on Microwave Theory and Techniques*, vol. 53, no. 2, pp. 538-547, Feb. 2005.

[50] I. Nam, B. Kim, and K. Lee, "CMOS RF amplifier and mixer circuits utilizing complementary characteristics of parallel combined NMOS and PMOS devices," *IEEE Transaction on Microwave Theory and Techniques*, vol. 53, no. 5, pp. 1662-1671, May 2005.

[51] Tae-Sung Kim, and Byung-Sung Kim, "Post-linearization of cascode CMOS low noise amplifier using folded PMOS IMD sinker," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 4, pp. 182-184, April 2006.

[52] Namsoo Kim, Vladimir Aparin, Kenneth Barnett, and Charles Persico, "A cellular-band CDMA 0.25um CMOS LNA linearized using active post-distortion," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 7, pp. 1530-1534, July 2006.

[53] Ehsan Adabi and Ali M. Niknejad, "CMOS low noise amplifier with capacitive feedback matching," *In Proceedings of the IEEE Custom Integrated Circuits Conference (CICC),* pp. 643-646, 2007.

[54] Zhe-Yang Huang, Che-Cheng Huang, "A CMOS low noise amplifier with RLC-impedance feedback for 3-5GHz ultra-wideband wireless system," *In Proceedings of the IEEE International Symposium on Integrated Circuits (ISIC '07)*, pp. 600-603, Sept. 2007.

[55] Trung-Kien Nguyen, Chung-Hwan Kim, Gook-Ju Ihm, Moon-Su Yang, and Sang-Gug Lee, "CMOS low noise amplifier design optimisation techniques," *IEEE Transaction on Microwave Theory and Techniques*, vol. 52, no. 5, pp. 1433-1438, May 2004.

[56] Mikko Kaltiokallio, Jouni Kaukovuori, Jussi Ryynänen, "Analysis of different feedback topologies to LNA input matching," *In Proceedings of the 18th European Conference on Circuit Theory and Design (CCTD 2007)*, pp. 68-71, Aug. 2007.

[57] Tienyu Chang, Jinghong Chen, Lawrence Rigge, and Jenshan Lin, "A packaged and ESD-protected inductorless 0.1–8 GHz wideband CMOS LNA," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 6, pp. 416-418, June 2008.

[58] Dariusz Pienkowski, Viswanathan Subramanian and Georg Boeck, "A 3.6 dB NF, 6 GHz band CMOS LNA with 3.6 mW power consumption," *In Proceedings of the 9th European Conference on Wireless Technology*, pp. 67-70, Sept. 2006.

[59] J. Borremans'1, S. Thijs2, P. Wambacql 2, D. Linten , Y. Rolain1 and M. Kuijkl, "A 5 kV HBM transformer-based ESD protected 5-6 GHz LNA," *In Proceedings of the IEEE Symposium on VLSI Circuits*, pp. 100-101, June 2007.

[60] Yi-Jing Lin, Shawn S. H. Hsu, Jun-De Jin, and C. Y. Chan , "A 3.1–10.6 GHz utra-wideband CMOS low noise amplifier with current-reused technique," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 3, pp. 232-234, March 2007.

[61] Hanil Lee and Saeed Mohammadi , "A 3GHz sub-threshold CMOS low noise amplifier," *In Proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, June 2006.

[62] Jeffrey S. Walling, Sudip Shekhar and David J. Allstot, "A gm-boosted current-reuse LNA in 0.18um CMOS," *In Proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 613-616, June 2007.

[63] Behzad Razavi, "A millimeter-wave CMOS heterodyne receiver with on-chip LO and divider," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 2, pp. 477- , Feb 2008.

[64] Jenn-Tzer Yang, Yuan-Hao Lee, Yi-Yuan Huang, Yu-Min Mu, and Yen-Ching Ho, "A 0.18um CMOS using high-Q active inductors for multi-band low noise amplifier," *In Proceedings of the IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC 2007)*, pp. 1001-1004, Dec. 2007.

[65] Bevin G. Perumanal, Jing-Hong C. Zhan, Stewart S. Taylor, and Joy Laskar, "A 12mW, 7.5GHz bandwidth, inductor-less CMOS LNA for low-power, low-cost, multi-standard receivers," *In Proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 57-60, June 2007.

[66] M. Challal, A. Azrar, H. Bbentarzi, "On low noise amplifier design for wireless communication systems," *In Proceedings of the 3rd IEEE International Conference on Information and Communication Technologies: From Theory to Applications*, pp. 1-5, April 2008.

[67] H. A. Haus, "Representation of noise in linear two ports," *In Proceedings of IRE*, vol. 48, pp. 69-74, Jan. 1960.

[68] M. Egels, J. Gaubert, P. Pannier and S. Bourdel , "Design method for fully integrated CMOS RF LNA," *Electronics Letters*, vol. 40 no. 24, Nov. 2004.

[69] Thomas Stuicke, Niels Christoffers, Rainer Kokozinski, Stephan Kolnsberg, and Bedrich J. Hosticka, "Graphical optimization of common-gate LNA," *IEEE Research in Microelectronics and Electronics*, pp. 453-456, June 2006.

[70] Jian-Yu Hsieh and Shuenn-Yuh Lee, "Analysis and realization of a low noise amplifier with high linearity and low power dissipation," *In Proceedings of the IEEE Region 10 Conference, TENCON 2007*, pp. 1-4, Oct. 2007.

[71] Ralf Reuter, Yi Yin, "A 77 GHz (W-band) SiGe LNA with a 6.2 dB noise figure and gain adjustable to 33 dB," *In Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 1-4, Oct. 2006.

[72] James Howarth, Jeffrey Harrison, and Anthony Parker, "A 60 GHz diversity LNA in 0.18μm SiGe," *In Proceedings of the 2nd IEEE International Conference on Wireless Broadband and Ultra Wideband Communications*, pp. 35-35, Aug. 2007.

[73] K. To, P. Welch, D. Scheitlin, B. Brown, D. Hammock, M. Tutt, D. Morgan, S. Braithwaite, J. John,J. Kirchgessner, W. M. Huang, "60GHz LNA and 15GHz VCO design for use in broadband millimeter-wave WPAN system," *In Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 210-213, Sept. 2007.

[74] Chung-Yu Wu and Po-Hung Chen, "A low power V-band low noise amplifier using 0.13um CMOS technology," *In Proceedings of the IEEE International Conference on Electronics, Circuits and Systems (ICECS 2007)*, pp. 1328-1331, Dec. 2007.

[75] Behzad Razavi "A 60-GHz CMOS receiver front-end," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 1, pp. 17-22, Jan. 2006.

[76] C. H. Doan, Sohrab Emami, Ali M. Niknejad and Robert W. Broderson, "Millimeter-wave CMOS design," *IEEE Journal of Solid-State Circuits*, vol. 40, no.1, pp.144-155, Jan 2005.

[77] T. Yao, M. Gordon, K. Yau, M.T. Yang and S.P. Voinigescu, "60-GHz PA and LNA in 90-nm RF-CMOS" *In Proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 2006.

[78] T. Yao, et al., "Algorithmic design of CMOS LNAs and PAs for 60-GHz radio", *IEEE Journal of Solid State Circuits*, vol. 42, no. 5, pp. 1044-1057, May 2007.

[79] Stefano Pellerano, Yorgos Palaskas and Krishnamurthy Soumyanath, "A 64GHz 6.5dB NF 15.5dB gain LNA in 90nm CMOS," *In Proceedings of the 33rd European Solid State Circuits Conference (ESSCIRC)*, pp. 352-355Sept. 2007.

[80] Raffaele R. Severino, Thierry Taris, Yann Deval, Jean-Baptiste Begueret , "A transformer-based 60GHz CMOS LNA for low voltage applications," *In Proceedings of the IEEE International Workshop on Radio-Frequency Integration Technology (RFIT 007),* pp. 62-65, Dec. 2007.

[81] B. Heydari, M. Bohsali, E. Adabi and A.M. Niknejad, "Low-power mm-wave components up to 104GHz in 90nm CMOS," *IEEE Solid-State Circuits Conference (ISSCC 2007), Digest of Technical Papers*, pp. 200-201, 2007.

[82] Ali Parsa, Behzad Razavi , "9.6 A 606Hz CMOS receiver using a 30GHz LO," *In Proceedings of the IEEE International Solid State Circuit Conference (ISSCC 2008)*, pp. 191-193, 2008.

[83] M. Anowar Masud, Herbert Zirath, Mattias Ferndahl, Hans-Olof Vickes, "90 nm CMOS MMIC amplifier," *In Proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp.201-204, 2004.

[84] Shih-Chieh Shin, Ming-Da Tsai, Ren-Chieh Liu, Kun-You Lin, and Huei Wang , "A 24-GHz 3.9-dB NF low-noise amplifier using 0.18um CMOS technology," *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 7, pp. 448-450, Jul 2005.

[85] Jeng-Han Tsai, Wei-Chien Chen, To-Po Wang, Tian-Wei Huang, and Huei Wang , "A miniature Q-band low noise amplifier using 0.13um CMOS technology," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 6, pp.327-329, June 2006.

[86] M.A.T.Sanduleanu, G. Zhang, and J. R. Long, "31-34GHz low noise amplifier with on-chip microstrip lines and inter-stage matching in 90nm baseline CMOS," *In Proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 143-146, 2006.

[87] Ehsan Adabi, Babak Heydari, Mounir Bohsali and Ali M. Niknejad , "30 GHz CMOS low noise amplifier," *In Proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 625-627, 2007.

[88] Yu Su, and Kenneth K.O., "An 800-uW 26-GHz CMOS tuned amplifier," *In Proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 151-154, 2006.

[89] M. Egels, J. Gaubert and P. Pannier , "High frequency LNA design in standard CMOS process," *IEEE North-East Workshop on Circuits and Systems*, pp. 5-8, June 2006.

[90] Frank Ellinger, "26–42 GHz SOI CMOS low noise amplifier," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 3, March 2004.

[91] Olivier Dupuis, Xiao Sun, Geert Carchon, Philippe Soussan, Mattias Ferndahl, Stefaan Decoutere and Walter De Raedt , "24 GHz LNA in 90nm RF-CMOS with high-Q above-IC inductors," *In Proceedings of the 31st European Solid-State Circuits Conference*, pp. 89-92, Sept. 2005.

[92] Sébastien Montusclat, Fréderic Gianesello, Daniel Gloria, "Silicon full integrated LNA, filter and antenna system beyond 40 GHz for MMW wireless communication links in advanced CMOS technologies," *In Proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, June 2006.

[93] S.-H. Yen and Y.-S. Lin , "Ka-band low noise amplifier using standard 0.18 lm CMOS technology," *Electronics Letters*, vol. 42 no. 16, Aug. 2006.

[94] Pietro Andreani, Henrik Sjöland , "Noise optimization of an inductively degenerated CMOS low noise amplifier," *IEEE Transaction on Circuits and Systems II: Express Briefs,* pp.835-841, , Sept. 2001.

[95] Robert Hu , "An 8–20-GHz wide-band LNA design and the analysis of its input matching mechanism," *IEEE Microwave and Wireless Components Letters*, vol. 14, no. 11, pp. 528-530, Nov. 2004.

[96] Robert Hu, "Wide-band matched LNA design using transistor's intrinsic gate–drain capacitor," *IEEE Transaction on Microwave Theory and Techniques*, VOL. 54, NO. 3, pp. 1277-1282, March 2006.

[97] Xuezhen Wang, Han-Chi Hsieh, Noshir Dubash, Gregg Zanfino, Armando Mendoza, and Douglas Schucker, "A novel simultaneous input and output matching method for GPS CMOS switched low noise amplifier," *In Proceedings of the 50th Midwest Symposium on Circuits and Systems (MWSCAS 2007)*, pp. 423-426, Aug. 2007.

[98] J.Borremans, P.Wambacq , D. Linten, "An ESD-protected DC-to-6GHz 9.7mW LNA in 90nm digital CMOS," *IEEE Solid-State Circuits Conference (ISSCC 2007), Digest of Technical Papers*, pp. 422-613, Feb. 2007.

[99] Ahmed Amer, Emad Hegazi, and Hani Ragai, "A low-power wideband CMOS LNA for WiMAX," *IEEE Transaction on Circuits and Systems II: Express Briefs*, vol. 54, no. 1, pp. 4-8, Jan. 2007.

[100] J. Yavand Hasani, M. Kamarei, F. Ndagijimana, "Input matching techniques for CMOS cascode LNA for millimeter wave applications" *In Proceedings of the 16th Iranian Conference on Electrical Engineering (ICEE2008)*, May 2008.

[101] Rinhold Ludwig, Pavel Bretchko, "*RF circuit design, theory and techniques*," Prentice Hall, Press 2000.

[102] D. C. DeGroot, K. L. Reed, and J. A. Jargon, "Equivalent circuit models for coaxial OSLT standards," *54th ARFTG Conference Digest*, Atlanta, GA, Dec. 1999, pp. 103-115.

[103] R. B. Marks, "A multiline method of network analyzer calibration," *IEEE Transactions on Microwave Theory and Techniques*, vol. 39, no. 7, pp. 1205-1215, July, 1991.

[104] J. A. Reynoso-Hernandez and E. Inzunza-Gonzalez, "Comparison of LRL(m), TRM, TRRM and TAR, calibration techniques using the straightforward de-embedding method," *In Proceedings of the 59th ARFTG Conference Digest*, June 7, 2002.

[105] Ralf Doerner, and Andrej Rumiantsev, "Verification of the wafer-level LRM+ calibration technique for GaAs applications up to 110 GHz," *65th ARFTG Conference, Digest of Papers*, Spring 2005.

[106] Available [Online]: www.suss.com

[107] Available [Online]: www.maxim-ic.com/legal

[108] D. C. Daly, A. P. Chandrakasan , "Energy efficient OOK transceiver for wireless sensor networks," *In proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, June 2006.

[109] J. D. Meindl and P. H. Hudson, "Low power linear circuits," *IEEE Journal of Solid-State Circuits*, vol. 1, pp. 100–111, Dec. 1966.