Design of a Radiofrequency Front-End module for "Smart Dust" sensor network

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UNIVERSITE JOSEPH FOURIER

N° attribué par la bibliothèque

T H E S E

Pour obtenir le grade de

DOCTEUR De L'Université Joseph FOURIER de Grenoble

Spécialité : **Optique et RadioFréquences**

Préparée à l'Institut de Microélectronique, Electromagnétisme et Photonique MINATEC Grenoble

Dans le cadre de l'Ecole Doctorale Electronique, Electrotechnique, Automatique, Télécommunication et Signal

Présentée et soutenue publiquement
par

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Date : 07 décembre 2008

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In The Name of Allah

In Memory of My Father….

To My Mother
And
My Wiffe

I would like to thank my supervisors, Pprofessor Kamarei in University of Tehran, Iran, and Professor Ndagijimana, in University of Joseph Fourier, Grenoble, French. I appreciate the kindly helps of Professor Jean-Michel Fournier in the IMEP laboratory, especially in the first steps of my work. The helps of my friend, Maxim Bernier and the accommodations of Mr. Nicolas Carroa in measurement of the fabricated LNA is also appreciated. I am grateful of the jury members from Iran and French, for tolerating the efforts and attending in the defence session.

This work was supported in part by the Iranian Telecommunication Research Center (ITRC), under the contract number 500/2983.

CONTENTS

Preface

Wireless Sensor Network (WSN) concept was introduced in 1994 for the first time, aiming at the military application. Then WSNs were considered in many civil applications and many academic and industrial researches were attracted in to WSN concept. The word "Smart Dust" was introduced in the University of California, an imaginary infinitesimal sensor node that can be suspended in air.

This thesis is an attempt toward very small "Dust-Like" sensor node to be used eventually in a short range dense WSN. The planning of the thesis was performed as a co-supervision program between University of Tehran, Tehran, Iran and University of Joseph Fourier, Grenoble, France. Primary studies of the thesis started in University of Tehran and from 2005-2006, the program was continued in the IMEP laboratory, MINATEC, Grenoble.

The definition of the thesis is design of low-power fully integrated RF front end for a mm-wave sensor node. Until now, all of the reported works in WSN context (in our knowledge) were in the frequencies limited to few GHz. For the first time, we introduced the use of mm-wave band in WSN application, targeting the benefits of this band, specially higher network immunity and possibility of antenna-on-chip integration. To obtain low-cost sensor nodes, the STMicroelectronics 90nm Global Purpose (GP) process was considered and the related foundry design kit was provided. Since this thesis was the first attempt in this way, there were not any primary experiences, or guide lines or even predefined parameters and characteristics for the RF front end. Due to cost considerations and some other limitations, global purpose CMOS process was used, instead of RF CMOS process and this was source of many challenges in our work. Actually we were obliged to develop all of the required modeling and design procedure for passive elements, as well as the proper parasitic models for active devices.

Actually the objective of this thesis was investigating the possibility of low-power fully integrated RF front end best performances that are achievable in mm-wave band, in 90nm CMOS technology. This thesis was the first work of mm-wave design in 90nm CMOS technology in the laboratory and hence our work could not be based on the available experiences. On the other hand our planning was to use bulk CMOS technology and we have not access to any pre-designed RF components. Consequently we were obliged to develop proper models for all of active devices and passive elements and tune the models using the foundry design kit, whenever it was possible.

After developing the first versions of our MOS transistor and inductor model, we started the most crucial part of the receiver, i.e. low noise amplifier (LNA). In this way we designed a 3-mW LNA in 2006 and we sent it to be fabricated by STMicroelectronics. We developed a simple design and optimization tool, written in MATLAB, composed of active devices and passive elements models, as well as a simple, but accurate Cascode LNA analyser and designer. After LNA, we studied the other main parts of the transceiver, i.e. VCO, mixer and power amplifier. In 2006 the layout of primary designs of VCO and mixer was completed. Until end of 2007, the next time I returned back to France to perform the measurements, we overviewed and modified our models and design tools and finally a complete LNA design tool, with proper GUI[1] was developed. In the first version of our work, we used MoM

[1] Graphical User Interface

electromagnetic simulator of ADS software in passive elements modeling. In the next versions, we developed our extraction process for passive elements, based on the full wave simulations in Ansoft HFSS.

Since we developed all of our required passive elements as an individual library in the design kit, attached to the CADANCE environment, we could not use the standard layout control and check-up tools and unfortunately a mistake had occurred in the layout of input matching network of the LNA. Due to this mistake, measurement results showed some discrepancy with the simulation results, in some characteristics. However, when we introduced the same mistake in our post-layout simulation of our design tool, we obtained the results in very good agreement with the measurement results and this proved the accuracy of our models and design tool. In spite of the mistake, our LNA has acceptable performance, regarding its only 3-mW power consumption. In addition, the chip are of our LNA is a record, thanks to the line-type inductors we have developed and used in our design. Finally, using the modified version of our design tool, we completed the LNA design and excellent performance was achieved, in comparison the reported works. Although the last designed LNA was not fabricated, it was simulated in post-layout simulation facility of our design tool, in conjunction with the foundry design tool, for which the accuracy was proved by measurement results.

For other parts of the transceiver we studied and examined various possible designs. We investigate different topologies for VCO, mixer IF amplifier, power amplifier and base band circuits, using analysis and simulation. Analysis results showed that among various available VCO circuits, some of them are more preferable for ultra-low power applications. Power amplifier is the most challenging in low-power mm-wave transmitter, specially in CMOS technologies in which the passive elements have low quality factor and high loss. Trying to use high efficiency Class E power amplifiers, we developed novel design methodologies for this class of amplifiers. Unfortunately we encountered difficulties in driving the switches in few-mWs power amplifiers in mm-wave band and finally we used other solutions.

After primary designing the transceiver blocks, we studied the transceiver architectures that are suitable for our application. In this way, the definition of the radio link and a simple communication protocol were necessary. Since we were not supplied by a high-level system design team, we defined the required parameters using our experience of transceiver deign, as well as our experience of achievable performance of transceiver sub circuits. We proposed sub-harmonic mixer topology in the receiver and power-oscillator solution in the transmitter. Performance of the transceiver was evaluated by circuit-level simulation of the transceiver sub-circuits is the first step, and then system-level behavioral simulation in MATLAB, in the second step. The designed transceiver is ultra-low power, in comparison with the reported mm-wave transceivers.

The dissertation composed of six chapters, describing our research form device-level modeling to system level design. In Chapter a brief history of WSN development is presented. Structure of a sensor node in a typical WSN is described and main characteristics and requirements of a WSN are reviewed. Then the transceiver architectures are investigated and the main features of the transceivers in WSN are presented. Chapter II deals with the MOS transistor model. As mentioned, the foundry design kit available for our work was global purpose CMOS process and was not useful for our work. So we developed our MOS transistor model, not only to obtain a simple analytic model, but also a flexible model that can be integrated in our design tool. We developed our model with simple analysis of short-channel MOS device and the model parameters were extracted and tuned in comparison with the simulation results in the foundry design kit. Passive elements and back-end parasitic effects have been described and modelled in Chapter III. In this chapter, we have described the novel line-type inductor structure and its lumped-element modeling basis. The developed

inductor model comprises the losses due to the eddy currents in the substrates, the phenomena that has not been considered in reported models (is not necessary) for transmission lines and coplanar wave guides. Accurate lumped-element models of RF pads, T-Junctions and transistor interconnections have been developed in this chapter and the model parameters have been calculated from full wave electro magnetic simulation. Lumped element models are very important in post layout simulation and make possible to capture the distributed effects in circuit simulators.

Chapter IV has been dedicated for LNA design, optimization and measurement results. To achieve low power consumption, we chose single stage LNA. Then using our analysis and design methodology, we found that cascode topology is very well suited for our objectives: good noise figure, enough power gain and high reverse isolation in mm-wave band and hence good stability. The design and optimization method has been described. Post-layout simulation and measurement results have been presented and analyzed and have been compared with the reported works. Finally, in Chapter V we have exploited the experience obtained in the previous chapters, as well as the new suggestions in this chapter, to propose and design the structure of our transceiver. We have developed analysis guidelines to choose the proper VCO topology and even-harmonic mixer design and optimizations. The desinged transceiver has been simulated using system-level simulation in MATLAB and behavioral model of sub-blocks were obtained from simulation in the foundry design kit and post-layout simulation using our design tool. Finally, the conclusion of the thesis and some suggestions and propositions for future works, have been presented in Chapter VI.

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Chapter I

RF Front End in Wireless Sensor Networks

I.1. Wireless Sensor Network Overview

I.1.1. WSN History

A Wireless Sensor Network (WSN) is composed of a large number of sensor nodes, each node capable of sensing its environment, processing the acquired data and communication with other sensors. The design and implementation of a wireless sensor network requires confluence of many fields, including communication and RF technology, sampling technology, signal processing, networking, power management, embedded systems, information aggregation, and distributed computing [1].

The history of WSN comes back to 1994, when DARPA funded the research projects, Low Power Wireless Integrated Micro-sensor (LWIM) and SensorIT at University of California [2], [3]. In 1998 Wireless Integrated Network Sensors (WINS) project was reported by University of California, Los Angeles, aiming at development of Micro-Electro-Mechanical Sensors (MEMS), efficient circuit design and self-organizing networking [4]. Then they biased toward military and environmental applications. PicoRadio was the other WSN project, reported in 2000, at University of California, Berkley, to support the assembly of an ad hoc wireless network of self-contained mesoscale, low-cost, low-energy sensor and monitor nodes [5], [6].

Advances in microelectronic devices and systems realized the design of very small sensor nodes, with capability of sensing, computing and communication. Such a small platform was referred to as *motes*. Then sensor networks were targeted to use of extremely low cost micro sensors that can be suspended in air. The first attempt in this way was the DARPA/UC Berkeley research project, named "Smart Dust", in which $4mm^3$ nodes was fabricated [7], [8]. Actually the genesis of Smart Dust was a workshop at RAND in1992 in which a group of academics, military personnel, and futurists were chartered to explore how technology revolutions would change the battlefield of 2025 [9]. The other *mote* sensor nodes were MICA2 and TelosA, developed by CrossBow and MoteIV corporations [10], [11]. Today, based on recently the amazing growth of sub-miniature, low-cost and low-powered hardware, the wireless sensor network is strongly researched for the various applications [1], [12]-[15].

I.1.1. WSN Applications

At a glance the application of WSN can be divided into two main category of civil and military applications. Industrial and manufacturing remote control, mechatronics and automation, distributed energy system control, emergency medical care, habitat monitoring , active volcano sensing , structural health monitoring, under ground mining, identification and personalization, aircraft health monitoring, environmental monitoring, environmental control in office buildings, robot control and guidance in automatic manufacturing, high security small homes, cultural property protection are examples of WSN civil applications[1], [16]-[22].

In disaster scene, use of WSN can greatly increase the rescue operation efficiency and rescue crew safety and can provide an intelligent rescue support framework [13], [18], [23]. In consumer electronic domain, WSN can form a warm atmosphere at home and boost the work efficiency in offices [24], [25].

In military applications, the use of these networks can limit the need for personnel involvement in usually dangerous reconnaissance missions. In addition sensor networks can enable a more civic use of landmines by making them remotely controllable and target specific, in order to prevent harming civilians [18], [26]. In tactical communication, Surveillance, Recognition & tracking, On-site, unattended, high-precision and real-time observation over a vast area, in security, intrusion detection and criminal hunting, WSN has been considered to have a good potential [27], [28].

Regarding so vast applications for WSN, many works in recent years have addressed the cooperation of new WSN's with existing networks, specially mobile ones, [29], [30].

I.1.2. WSN Structure and Specifications

Among the existing networks, the Mobile Ad hoc Networks (MANETs) are more similar to the WSNs. However there are some essential differences between them [18]:

Sensor nodes in a WSN can be several orders of magnitude higher than MANET.

Sensor nodes in a WSN are much cheaper than the nods in MANET.

Power resource of a WSN node is more limited.

WSN nodes have limited computational capability.

WSN nodes are more prone to failures.

The topology of a WSN varies more frequently than a MANET.

WSN nodes use normally a broadcasting paradigm, whereas MANET nodes use point-to-point communication.

The architecture of wireless sensor networks needs to accommodate three characteristics [16]:

Scalability: Large-scale wireless sensor networks rely on thousands of tiny sensors to observe and influence the real world. These sensors do not necessarily need to be active at all times, so sensors can be dynamically added to or removed from the network. A durable and scalable architecture would allow responses to changes in the topology with a minimum of update messages being transmitted.

Task Orientation: The sensor networks are always correlative with tasks at current stage. The tasks of wireless sensor networks range from the simplest data capturing and static-nodes to the most difficult data collecting, mobile-node sensor network. The sensor networks for different tasks behave totally differently sometimes. The software structure should be reasonably optimized and tailored, according to predefined task-set of each node, to be adapted to this distinction.

Light Weight: The computing and storage capabilities of sensor nodes are very limited. Lightweight operations, such as data aggregation, reduced message size, and a piggyback acknowledgment mechanism, must be applied to the architecture.

Traditionally, wireless sensor networks devices and corresponding network protocols are designed to handle a small amount of data and most sensor nodes can only sustain an effective data rate of tens of kilobytes/Sec [31]. However, with the increasing popularity of wireless sensor networks in a broad spectrum of applications, higher data transportation capability is in need. In particular, visual information (such as still image or video data) is very valuable in many applications. For instance, wireless devices with video camera can be used to provide video surveillance in battlefield network [32].

I.1.3. Sensor Node Structure

Basic block diagram of a wireless sensor node has been shown in Fig. I-1 [9]. A complete node consists of many blocks, most of which can be integrated onto a single standard CMOS die. Energy storage (batteries, large capacitors, or inductors), energy scavenging, and some sensors will likely be off-chip components. The primary integrated blocks include a sensor

interface, memory, computation, power management, and an RF transceiver. Development of highly integrated sensor mote components started in the mid-1990s and resulted in multi-chip systems that could be assembled to create a mote. At UCLA, MEMS devices were combined with commercial CMOS chips that provided sensor control and readout as well as communication [9]. To minimize energy, passive optical communication was explored for early Smart Dust motes [33]. Fig. I-2 shows the sensor node fabricated as integration of CMOS and MEMS technology for early generations of Smart Dust, at University of California, Berkeley. This node comprises an bidirectional communication system with a MEMS optics chip containing a corner-cube retro-reflector on the large die, a CMOS application-specific integrated circuit (ASIC) for control on the 300 × 360 micron die, and a hearing aid battery for power. The total volume is 63 mm3. [8]. In the next generations highly integrated chips with a complete RF transceiver, microprocessor, ADC, and sensor interface have been reported [34], [35].

Most of the blocks in Fig. I-1 can be implemented in standard CMOS process, suitable for mote sensor node [36], [37]. However still some parts like off-chip battery, a crystal timing element, and an RF antenna, should be off-chip, resulting in a complete package at the centimetre scale. As an example, a $\lambda/4$ patch antenna in the size of $4\times5\times1.64\text{mm}^3$ has been designed for mote sensors, operating at 10GHz [38]. A 6.8mmOD x 1.2mm, 3V and a 5.8mmOD x 1.6mm, l.5V rechargeable Mn-Li cells has been used in the first and second Smart Dust generations, respectively [39]. Fig. I-3 shows complete sensor nodes, with different possible levels of integration. While the cost, size, and power consumption of off-the-shelf sensor nodes is far from optimal, a single-chip system may not be the most advantageous either and the most economical solution is likely to be a hybrid of integrated and assembled parts [9]. The device at the top of Fig. I-3 is the Mica sensor node [10] and the device at the bottom of Fig. I-3 represents a hypothetical 2-mm3 mote-on-a-chip combining cutting-edge process integration and circuit techniques. In [34] a fully integrated 1V wireless SoC that embeds not only a complete dual-band RF transceiver, but also a sensor interface for

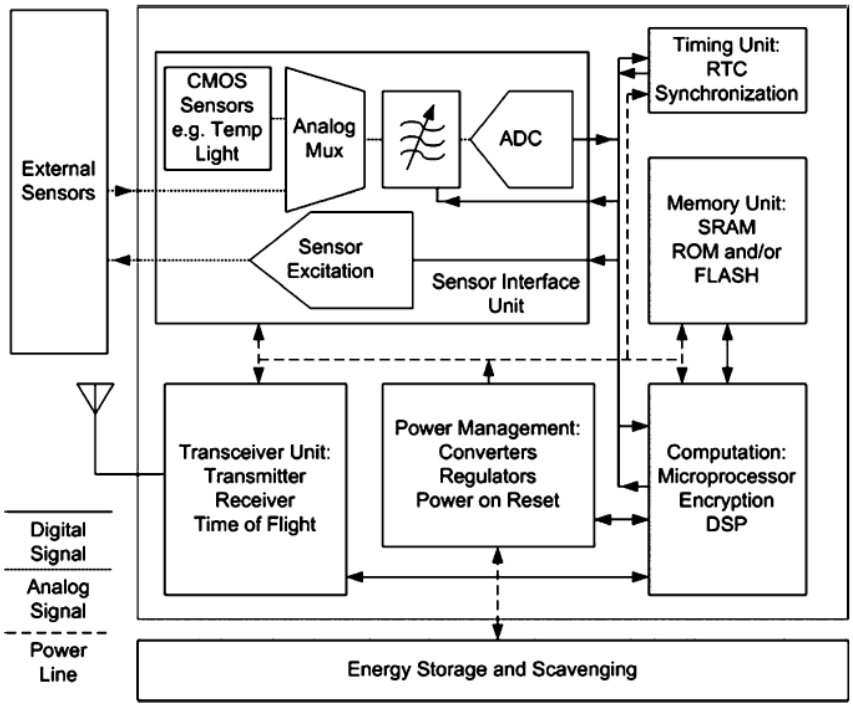


Fig. I-1. Basic block diagram of a wireless sensor node [9]

signal acquisition, a RISC microcontroller and memory-based control unit, and a power-management unit that can generate up to 2.4V for off-chip parts from a 1.0V to 1.6V AA battery, has been described. The RF front-end consists of two RX/TX channels targeting the 433MHz (ISM) and the 868MHz (SRD) European bands. With a different input adaptation scheme, the US 915MHz can also be covered. The RX and TX are built according to a two-step super-heterodyne architecture with LO frequencies set to 8/9 and 1/9 of the RF, and share a common PLL based on a 772MHz VCO and a division chain for the other LO signals. The VCO tank is built with two external high-Q inductors and an on-chip varactor. An integer-N synthesizer PLL uses a 12.8MHz quartz reference and allows the RF frequency to be adjusted with 12.5kHz steps. Scan Electron Micrograph (SEM) of the IC has been given in Fig. I-4. The IC has been implemented on standard digital 0.18µm CMOS and has a size of 3.5×4 mm^2, excluding the "bond-out" pad-ring.

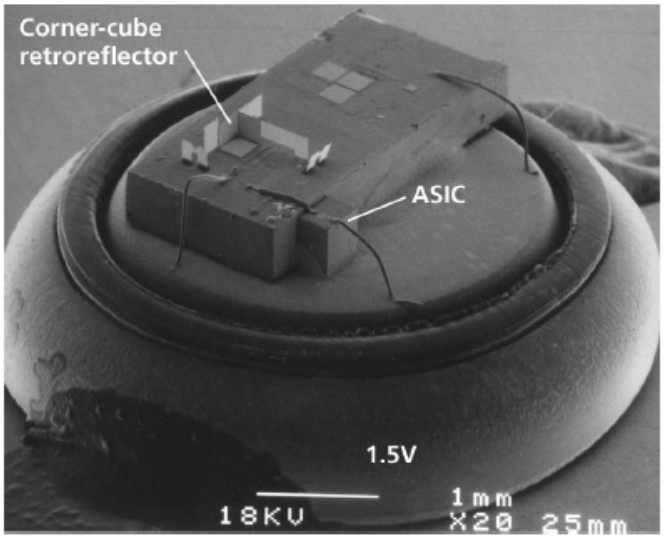
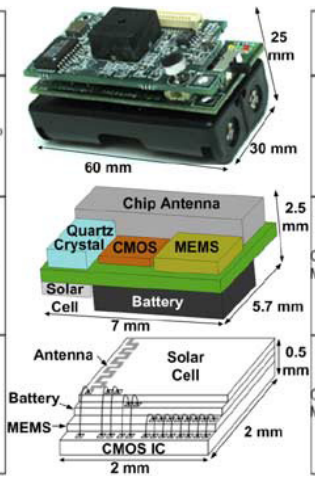


Fig. I-2. The mote sensor node fabricated as integration of CMOS and MEMS technology for early generations of Smart Dust, at University of California, Berkeley. [8]



Power	Volume	Sensor(s)	Processor	Energy Harvesting	Energy Storage	RF	Antenna	Timing Reference
Highest	45,000 mm^3	Off-the-shelf	Atmel Atmega 128L	None	2 AA Batteries	ChipCon CC1000	Straight Wire	Quartz Crystal
Lowest	100 mm^3	CMOS - temp, light MEMS - inertial	Custom CMOS	Off-the-shelf Solar Cell	Off-the-shelf Microbattery	Custom CMOS	Dielectric Chip Antenna	Quartz Crystal
Low	2 mm^3	CMOS - temp, light MEMS - inertial	Custom CMOS	Custom Solar Cell	Custom Thin-film Lithium Battery	Custom CMOS	Custom On-Chip Antenna	MEMS Resonator

Fig. I-3. Complete sensor nodes, with different possible levels of integration [9]

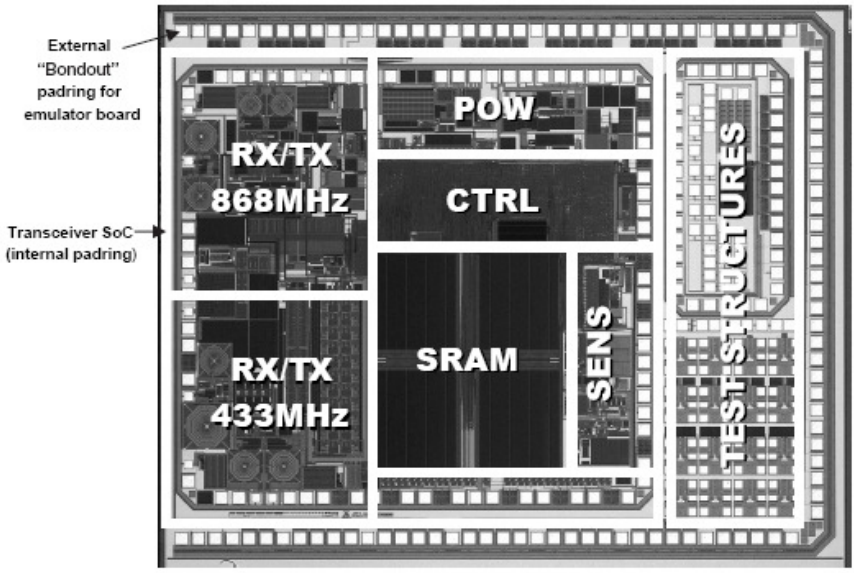


Fig.I.4. SEM of the fully integrated sensor node, presented in [34]

I.1.4. Security and Reliability in WSN

Remote wireless sensor networks are vulnerable to malicious attacks. While wired and infrastructure-based wireless networks have mature intrusion detection systems and sophisticated firewalls to block these attacks, wireless sensor networks have only primitive defences. Different types of attacks and risks for a WSN have been studied [40]. Beside the performance perturbation, malicious attackers can easily target the battery supplies and reduce network lifetimes from years to days [31].

Reliability is another important issue in WSN's. Information theoretic approach has been used to estimate the redundancy in a randomly deployed wireless sensor network and provide the Cramer-Rao bound on the error in estimating the redundancy in a wireless sensor network [41]. Simple source and channel codings, e.g. LDPC[2], have been suggested for WSN's [42]. In AWGN[3] channels the LDPC performance is very close to the Shannon capacity. Also, LDPCs have gained more attention because of its parallelizable, and can be suitable for VLSI implementations [43].

I.1.5. Power Source Limitation in WSN

DC power source is the most critical section of a sensor node. Battery size determines the size and lifetime of a mote sensor node, consequently minimization of power consumption, not only maximizes the sensor life time, minimizes, but also minimizes its size [39].

Among the numerous technologies in terms of the materials used and chemistry and composition that can serve as the basis for rechargeable (or secondary) batteries, the Lithium ion (Li-ion) cells exhibit one of the highest energy densities among the commercially available types—i.e., specific energy density of 80–125 W h/kg (watt hour per kilogram) and volumetric energy of 200–450 W h/l (watt hour per litre). For instance, miniature Li-ion rechargeable battery sources as small as 0.08–0.155cc with capacity ratings of 3–25 mA h are readily available for biomedical implants. These batteries can also accommodate current pulses of 10–15 mA depending upon battery size, which makes them suitable for low power wireless devices [44]. Low-data-rate wireless sensor networks such as WiseNET are built

[2] Low Data rate Parity-check Code
[3] Additive White Gaussian Noise

with nodes that have to achieve from 2 to 7 years operating life on a 1.5V AA alkaline battery [34]. A AA battery contains roughly 250 uA-years of charge or about 12000 J. For some lithium chemistries, the internal leakage is low enough that supplying this charge as a current of 25 uA for a decade is possible while common alkaline chemistries have shorter lifetimes [9].

Energy scavenging and harvesting techniques, e.g. solar cells, have been proposed for sensor nodes [5]. Battery powered wireless sensor nodes can be recharged by harvesting energy from a solar cell [33] or a microwave Radio Frequency (RF) signal source [45]. In such nodes a wireless battery is used to convert wireless RF power into DC power. In [46] an specially designed wireless battery or *rectenna* has been designed, operating at 2.45GHz and the power conversion efficiency of 52% has been achieved for a 0dBm power level received by the antenna.

Aside from battery technology, various power saving methods have been developed for WSN's. Conventional power saving techniques have been investigated in [47] and [48]. Analytic models have been developed for analysis and optimization of power consumption in a WSN [49]. Power consumption in a WSN can be related to three levels of the network: Hardware, protocol and operating system [14]. In other reports this has been divided into Physical layer, Media Access layer (MAC) and Network layer [6].

Power Saving in Protocol level

Medium access protocols which accommodate dynamic voltage and frequency scaling, as well as dynamic or periodical sleeping, have been proposed for minimizing collusion, overhearing and idle listening [1]. Nodes synchronization in the network has important effect on the power consumption of the nodes. Conventionally used Reference Broadcasting Synchronization (RBS) in ad hoc networks, is not suitable for WSN's. In RBS high volume of message packets to be propagated upon the network that waste the energy of the nodes. Consequently new synchronization techniques have been proposed for WSN's [29]. Special clustering schemes for efficient energy consumption and energy aware routing protocols have been developed [50]-[52]. Using Multi-hop access, instead of single-hop access, effectively reduces the energy cost per bit [6]. Different channel codings (modulation) have been investigated in [42]. Various researches have been performed on Mica2 WSN node to evaluate different protocols [53]. In [54] a MAC protocol with Slot Periodic Assignment for Reception (SPARE MAC) has been presented that limits the energy waste due to packet overhearing, packet over-emitting, and idle listening. SPARE MAC is a Time Division Multiple Access (TDMA) based scheme, which implements a distributed scheduling solution that assigns time slots to each sensor for data reception and shares such assignments with neighboring nodes. Package duplication and multi-path package reception problems have been investigated in [55] and a protocol named Receiver Based Forwarding (RBF) has been presented.

I.1.5.1. Power Saving in Operating system level

In operating system level Dynamic Power Management (DPM) has been investigated in [14] and the sentry-based power management has been addressed, in which the nodes are partitioned dynamically into two sets: sentries and non-sentries. The sentries provide sufficient coverage for monitoring and communication services and non-sentries nodes sleep for a designated period of time. An application-driven power control has been proposed in [56] and three states: active, idle and sleep has been defined for nodes.

I.1.5.2. Power Saving in Hardware level

In our opinion, power consumption reduction in physical layer is the most important issue in the power saving of a sensor node. Special design and integration techniques have been used for reducing the power consumption of sensor nodes [57]. To give the scenes about the power consumption in existing wireless sensor nodes, we investigate some available and reported ones. Some commercial IC's have been presented by famous companies in the WSN domain [57]. CC2430 /2431 is a wireless sensor node, fabricated as fully integrated System-on-Chip (SoC) by Chipcon [58]. MC132121 series is another fully integrate sensor node, manufactured by Freescale Semiconductor company [59]. JNS121series are fully integrate wireless sensor nodes, presented by Janic company [60]. The main characteristics of these chips at the working frequency of 2.4GHz, have been tabulated in Table I-1 [57]. The interesting note in this table is that the power consumption in RX mode is more than that of TX mode. This also has been emphasised in [61], in which claimed that 50% of total power dissipation is in the transceiver, of which 80% is consumed in the receiver. Specifications of more RF chipsets, fabricated for WSN applications have been presented in [57]. Crossbow Company has a wide variety of mote sensor nodes, all having the DC power consumptions about the values in Table. I.1 [10]. These sensor nodes have been used in many recent WSN researches [53].

Although power dissipation for commercially available sensor motes is in the range of few tens of mA, such DC power is very high for Smart Dust projects. The desired average DC power consumption is below 100uW [5]. Such value may be achievable, if laser communication is used in a very simple sensor node [36], [33]. However in the case of to days low power radio communication technology, and for a complicated digital processor this seems to be an oxymoron.

Power dissipation in hardware level is divided into three sections: Analog and digital circuits, RF circuits and ADC converters. It is well known that the RF section consumes a largest amount of the energy in a low power communication system [57]. For the first ADC circuits, designed for the first generations of smart Dust, the reported specs were 360 PJ/S (Pico-Jules per sample) with the sampling rate of 100KS/Sec and 8-bit samples that is equivalent to the DC power of 3.6mW in full speed working. For the next generations of this

TABLE I-1
Specifications of 3 fabricated chips for WSN applications [57].

Parameters	CC2430	MC1321x	JN5121
Operating Supply Voltage (Vdd)	2.0 ~ 3.6V	2.0 ~3.4V	2.2 ~ 3.6V
MCU active and RX mode (Icc)	27 mA	37 mA	< 50 mA
MCU active and TX mode (Icc)	25 mA	30 mA	< 40 mA
Maximum Transit Power	0 dBm	2 dBm	1 dBm
Power Down Mode Current (Ipd)	0.9 uA	1 uA	< 5 uA
Receiver Sensitivity	-94 dBm	<-94 dBm	-93 dBm
Microprocessor	32 MHZ 8-bit Low power 8051	40MHz HCS08	16 MHZ 32-bit, RISC
Memory	32, 64, or 128 KB Flash, 8 KB RAM	1-4KB RAM 16-60KB Flash	64 KB ROM, 96 KB RAM
ADC	8-14 bit ADC	8-10 bit ADC	4-12 bit ADC
DAC			2-11 bit DAC

project the reported specs were 31 PJ/S with the sampling rate of 100KS/Sec and 8-bit samples in 0.25um CMOS process, that is equivalent to the DC power of 0.3 mW in full speed working. The DC power consumption of 0.26 mW has been reported in [6] for the processor section of a typical WSN node. In the fully integrated sensor node reported in [34], fabricated in 0.18um CMOS, the processor has two modes of operation: 32 KHz and 6.4 MHz. The required DC power is 60uA/MIPS, that is equal to less than 0.38 mW, in worst case. However the RX power consumption in this work is 2.1 mA with 1~1.6 V supply and the TX power is 27.6 or 32.3 mA, depending on the working frequency. The energy costs of different operations in a typical sensor node have been listed in Table I-2 [9]. However using new technologies, sub-mW CMOS transceivers have been emerged. More details of DC power consumption in RF sections will be given in the next section.

I.2. Transmitter and Receiver in WSN

As we mentioned earlier, a significant part of DC power in a sensor node is consumed by the transceiver. Consequently special attention should be paid for design and optimization of the RF parts. Here we present a preliminary discussion and the details analysis will be presented in Chapter V. Power consumption of the RF front end in a WSN node can be minimized in three levels: Protocol level, Structure level and circuit level.

The highest level is the protocol considerations. Note that the network protocol affects the total power consumption of the network, in two ways. One is the network-related issues, as pointed in the previous sections and the other is its direct influence on the transceiver. Parameters such as working frequency, modulation scheme and the transmitted signal nature are given by the protocol and directly affect the structure and power efficiency of the transceiver. As we explained, WSN's are inherently low data rate systems and hence low-data rate UWB[4] protocols may be useful for WSN's. Such protocols can be considered under the IEEE 802.15.4a standard [62]. Many works have been reported to implement UWB transceivers for WSN's [61], [63]-[67], however in [61] suggested that this standard is not sufficient for WSN applications. Most interest in WSN is very simple modulations, such as OOK[5], BFSK[6] and PPM[7] [68]-[72].

The second level is the structure of the transceiver. Historically used heterodyne transceivers, Low-IF transceivers and Zero-IF (Direct Conversion) transceivers are possible choices for WSN applications [9], [34]. In addition, special transceiver architectures have been presented for low data rate UWB applications [62], [64], [73]. In recent years special

TABLE I-2
The energy costs of different operations in a typical sensor node [9].

Operation	Lowest Energy Published	Commercially Available (off-the-shelf)
8-Bit Analog-to-Digital Conversion	0.031 nJ	13.5 nJ
8-Bit Microprocessor Instruction	0.012 nJ	0.20 nJ
Compute an 8-Bit, 1024 point FFT	80 nJ	-----
Transmit and Receive one 8-Bit sample via RF at up to 20 m Range	32 nJ	2500 nJ

[4] Ultra Wide Band
[5] On - Off Keying
[6] Binary Frequency Shift Keying
[7] Pulse Position Modulation

simple transceiver structures have been developed for WSN applications [68], [70], [74]-[76]. Various structures will be compared in Chapter V.

The third level is the various circuits used in the transceiver. In recent years many circuits have been designed to be used in WSN transceivers. Some propose MEMS or other special technologies to achieve very low power [77], [78] and some other have emphasis on bulk CMOS technology [79], [80]. The technologies other than CMOS also have been considered in design of Class E power amplifiers for WSN's [81].

I.3. Transceiver Specifications

In this section we briefly describe the given specification for the transceiver we have designed and the semiconductor technology we have used in our work.

I.3.1. Semiconductor Technology Issues

Until 1990 few experts believed that CMOS will be a credible RF technology. In 1980 first CMOS RF application emerged: A broadcasting FM radio in 2 um CMOS, however the performance is not acceptable [82]. Then during only one decade, CMOS technology was the best candidate for many below-10GHz RF applications. Generally specking, the speed of analog CMOS circuits climbs by roughly one order of magnitude every ten years. For example, the first 1.4-GHz MOS voltage-controlled oscillator (VCO) was reported in 1988, the first 10-GHz CMOS oscillator in 1999 , and the first 104-GHz CMOS VCO in 2004 [83].

Today, f_T of CMOS transistors has passed 100GHz and CMOS technology experiences the millimeter wave designs. VCO in 114 GHz and LNA in up to 80GHz in 0.13um bulk CMOS have been reported in 2007 [84], [85]. Fig. I-5 shows the outlook of CMOS technology, implying that in the recent decade near-THz circuits will be emerged [82].

We will use STMicroelectronics 90 nm Global Purpose (GP) process in our work. The related foundry design we have used in our work supports only the digital design and hence all of the high frequency issues have been modelled and added specially for our work. Modelling of passive and even active devices have been done individually, using the foundry design kit as the reference. The layout for all the passive devices (except for the Resistors and MIM capacitors) and active devices (except for MOS transistor core) required in our work, have been designed individually, using the foundry Design Rule manual (DRM) data. Special attention has been paid to comply with the density design rule checks. The details will be given in Chapters II and III.

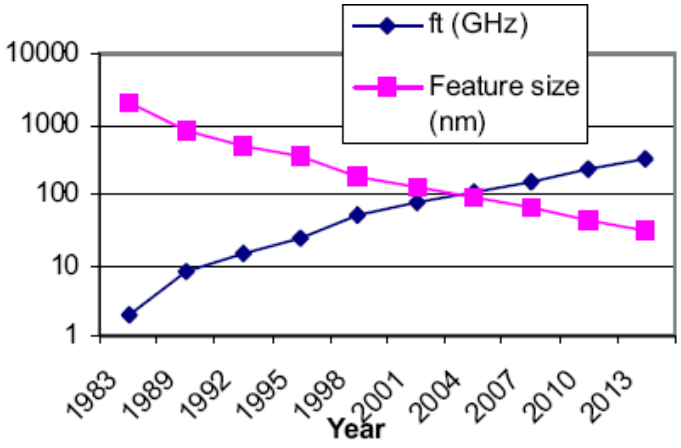


Fig. I-5. The outlook of modern CMOS technology [82].

Our design and optimization has been done in our design tools, we have developed specially for our work. However verifying simulations have been done using the foundry design kit attached to the CADENCE software, using the Spectre RF circuit simulator, Virtuse Layout Editor, Diva Layout Versus Schematic (LVS) check and Calibre extraction tool.

I.3.2. Transceiver Specifications in Our Work

The unlicensed 57-64 GHz was opened as ISM[8] band for new short range, high data rate communications [86]. The ultimate objective of our project is to use this band in Smart Dust wireless sensor network. Using this band, the wireless sensor network will benefit the smaller sensor nodes and higher security. However many problems related to such high frequency must be solved. Our work has been defined to be done in 30GHz band, as a bridge to the ISM 60GHz band. Since our work is the preliminary step of the final project, other specification are not given and we will go toward the best possible results.

[8] Industrial, Scientific and Medical

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