Chapter II

MOS transistor model and layout issues

One of the most important design issues in millimeter wave circuit design in modern MOS technologies is active devices and related parasitic elements modeling. The MOS transistor model that can be used in such high frequency must accurately comprise all of the unwanted parasitic effects that arise in high frequencies, as well as DC and low frequency characteristics.

Professional circuit simulators and foundry design kits provide a complete environment for design, optimization and validation of different circuits, as well as layout tools. However due to many high frequency effects that arises in millimeter wave frequencies and have not been included in available RF design kits, millimeter wave circuit designers need to develop an individual simple design tool. This tools are used in pre-design analysis, design procedure and after-design diagnosis. Then the foundry design kit is used for final design evaluation and probably optimization, after some special considerations by the designer.

In our work the problem is more sever, since the foundry design kit we are working with, is for 90 nm digital CMOS technology and does not provides any RF design facilities. Consequently we are obligated to develop our design and optimization tools, using the foundry design kit data and the foundry confidential Design Rule Manual (DRM). Then we should use the design kit with some special considerations for post-layout simulation and to evaluate the final design. Off course the parasitic extraction tools of the design kit are not useful for our work. An accurate model for MOS transistor is one the most important requirement of our design and optimization tool.

In the STMicroelectronics 90nm global purpose CMOS foundry design kit, BSIM3v3 has been used with some modifications, specially to capture the stress effect [1], [2], [3]. The modifications have been mainly made as pre-calculation of some BSIM3v3 standard parameters. However this model is not sufficient for millimeter wave design and hence we obligatory should develop an accurate model based on the design kit model and the used technology data, given in the foundry Design Rule Manual (DRM). The parts of our model that have been covered by the ST foundry design kit, have been calibrate using the design kit. The other parts have been obtained analytically, using the foundry design rule manual.

In this chapter we will give a brief overview of available models. Then we will describe our model that we have used in our design and optimization tool. Our model consists of some new equations for I-V characteristics, gate resistance, substrate and layout-dependent effects. We also will propose an analytic method for layout optimization. Our model consists of the following main sections:

- Transistor core model, consisting of single equation I-V model, capacitance model, small signal and noise models
- Layout-dependent parasitic elements, consisting of gate resistance model, substrate model, interconnect model and other parasitic elements.
- Y parameter model for small signal and noise analysis

II.1 MOS Modeling Overview

In recent years the MOS technology has been scaled down to nanometer regime and various MOS transistor models have been proposed to best capture the transistor behavior. MOS modeling is always a compromise between two factors: Accuracy and complexity. In a glance, all of the available models can be divided in to two main categories. First category is

the table-based or table-look-up models, directly obtained from measurement results. Second category is the mathematical model that is fully or partially obtained from the study of the physics of the transistor. In other glance, all of the models can be divided in to simple or complicated models. Simple models are used in small primary design tools and are useful in pre-design analysis and after-design diagnosis. These models can give an insight of the behavior of the device, as well as the effect of the device parameters on the final design. These models are also useful for education purposes. Complicated models are used in professional circuit simulators for design evaluation and optimization.

Here we divide all of the models in to three categories:

- Professional physical models
- Professional table-based models
- Simple physical models

II.1.1 Professional Physical Models

These models have been developed based on the accurate study of the related physical phenomena's. In nanometer scale MOS technologies, these phenomena's, specially short channel and quantum effects, are very complicated and hence such models are very complicated. Three main groups of these models have been developed for modern MOS technologies [4], [5]. First and more extended group is based on the threshold voltage. Spice models, Bsim3, BSIM4 and MM9 are examples of this group [6], [7], [8]. Second group is based on the inversion charge approach. EKV [5], ACM[1] [9] and BSIM5 [10] are based on the inversion charge or charge sheet layer methods. Third group are surface-potential-based models. SP [11], PSP [12] and MM11 [13] are the examples of these models. Two last groups are more adapted to the nanometer regime MOS technologies, since threshold voltage based models use many mathematical smoothing functions and fitting parameters, and hence less physical insight to device operation [7].

Extraction of model parameters from measurement results is very essential for professional models [13]. Specially the parameters related to capacitance and trans-capacitance has been a challenge from past to present [14], [15].

II.1.2 Table-Based Models

As the MOS technology goes to nanometer regime, capturing the new physical phenomena's makes the professional physical based models more and more complicated. Such complicated models are computationally expensive and a greatly influence the simulation run time, so that up to 80% of the run time is consumed to model evaluations [16]. On the other hand simple physical models have not enough accuracy for final design evaluation and optimization. So the table-based models have been presented to comprise both of the accuracy and simplicity. Table based models have been developed since the 1970s, in the digital and mixed mode circuit simulators like MOTIS [17]. Then 3D models was born in 1982 [18] and professional circuit simulators based on these models was developed in 1983 [19]. Table base models were applied to RF simulators by Root *et al*. for GaAs FET devices [20].

The accuracy of table-based models is influenced by a large number of factors, such as extrapolation accuracy, data interpolation accuracy and the accuracy of the parameters derived from the table data (such as ac model parameters). Data interpolation from the table data has been discussed in [21]. In [16] different table structures have been considered to obtain the required accuracy with minimum table size.

[1] Advanced Compact MOS Model

II.1.3 Simple Physical Models

Due to their complexity, professional MOS models can not be used in the simple individual design tools. For example, MM11 has approximately 80 parameters [22]. BSIM3v3 has more up to 80 parameters for I-V equation, 22 parameters for capacitances and 12 parameters for thermal effects and 4 control parameters. BSIM4.3.0 has about 136 parameters for I-V model, 20 parameters for RF and layout dependent effects, 18 parameters for thermal effects and 20 control parameters, as well as some parameters for comprise the stress effect [23], [24].

Development of individual design tools need to have a simple, but accurate MOS device model. Such model can give the designer insight of what happens physically in the device and this helps the designer to perform the pre-design analysis and after-design diagnosis [25].

II.2 Our Model for Intrinsic MOS Transistor

In this section we present a simple, but accurate model that can capture the MOS transistor core characteristics in 90nm MOS technology. Our model consists of large signal nonlinear I-V characteristics and capacitance models, a small signal linear model and a simple noise model. I-V characteristic is a set of mathematical equations that describes the drain voltage as a function of four transistor nodes, i.e. gate, drain, source and bulk. Capacitances model are mathematical equations that describe the nodal capacitance and trans-capacitance of the transistor nodes. I-V and capacitance models are directly used in DC or large signal analysis, as well as in the small signal analysis to calculate the small signal model parameters. Continuity of the large signal equations and their derivatives are very important in simulation convergence [26]. So in our model all of large signal equations are unique for both of linear and saturation regions.

II.2.1 I-V Characteristic

The fist ideas in modeling of I-V characteristics of a MOS transistor stems from Shockley studies [27]. Then the basic quadratic equation derived in early 1960 [28]. This equation is as follows:

$$I_d = \begin{cases} 0 & cutoff \\ \mu_n C_{ox} \dfrac{W}{L}\left(V_g - V_{th} - V_d\right)\ V_d & linear\ \ region \\ \mu_n C_{ox} \dfrac{W}{L}\left(V_g - V_{th}\right)^2 & saturation\ \ region \end{cases} \quad \text{(II-1)}$$

where V_{th} is the threshold voltage. For many years, this basic model has been recognized as inadequate and various modifications have been made to fit the basic equation on the modern MOS technologies. Mobility reduction, velocity saturation and channel length modulation are examples of the performed modifications. In the saturation region channel length modulation can be considered simply as:

$$I_{ds} = \frac{\mu C_{ox} W}{L} V_{od}^2 \left(1 + \lambda\left(V_{ds} - V_{eff}\right)\right) \quad \text{(II-2)}$$

Where V_{od} is the over drive voltage, defined as:

$$V_{od} = V_{gs} - V_{th} \quad \text{(II-3)}$$

Mobility degradation and velocity saturation have been considered in many literatures and text books [29], [30], [31]. Mobility degradation is due to the lateral filed due to drain-source voltage, as well as the vertical field due to gate voltage. In most of these literatures the mobility has been considered as a average effect in the channel and hence a multiplicative modifier has been used. The most common way is express the mobility as in [4]:

$$\mu = \frac{\mu_0}{\left(1+\theta_1 V_{od}+\theta_2 V_{od}^2\right)\left[1+\frac{V_d}{E_c L}\right]} \tag{II-4}$$

Multiplicative correction of mobility value has been considered in the physical alpha-power law model and some other physical models [32], [33]. However the field components are not uniform in all of the channel length. The vertical field dominates in part of the channel near to the source and reduces the mobility. However in the drain end of the channel lateral field is dominant and causes the velocity saturation. Consequently considering a average effect can not lead to an accurate model [4].

The nonlinear behavior of drain current has been investigated in many presented models. Although Shockley model predicts quadratic variation of the drain current in saturation region, this diminished in short channel MOS transistors. Alpha-power law model, presented in 1990, was a fully empirical model that proposed a new equation as follows [34]:

$$I_{ds} = B\left(V_{gs} - V_{th}\right)^{\alpha} \tag{II-5}$$

In [34] value of alpha was found 1.2, 1.2 and 1 for 1.2 um, 0.8 um and 0.5um technologies, respectively. Other alpha-power low models have been developed with physical insight in to the transistor behavior. In [32] and [35] with physical analysis of the drain current equations have been derived to calculate the exact value of alpha, as a function of gate voltage. In [35] has been shown that the value of alpha goes toward 2 in long channel case and goes toward 1 in short channel case.

Unfortunately none of the above models have adequate accuracy in today's nanometer scale MOS transistors. Consequently in recent years beside new professional complicated models, some new simple models have been developed for design, analysis and simple simulation tools. Hauser has proposed a physical model, based on the well known sheet charge layer model [4]. Based on this model the drain current and the voltage along the channel obey a simple differential equation:

$$I_{ds} = \mu C_{ox} W\left(V_{gs} - V_{th} - V\right)\frac{\partial V}{\partial x} \tag{II-6}$$

He has used a new approach to calculate the mobility as a function of gate and drain voltages. The obtained result is a single-equation model, well fitted to I-V characteristics of a transistor with 90nm gate length. In [29] a compact model has been developed to calculate the trans-conductance of a deep submicron transistor. This model predicts quadratic relation of the drain current and gate-source voltage for small gate-source voltages and linear relation for large gate-source voltages. Measurement results in [1] show that the drain current is linear function of gate voltage for 0.13 um MOS technology. Simple model of Gray also shows such behavior [31]:

$$I_{ds} = \frac{\mu_0 C_{ox} W}{2L}\frac{V_{od}^2}{\frac{V_{od}}{LE_{sat}}+1} \tag{II-7}$$

For large *L* drain current is quadratic function of gate voltage, and for small values of L the function is linear.

A simple model have been developed in [1] for RF applications. This model is single-equation for both of linear and saturation regions. The basis is Shockley model, but velocity saturation has been included as an empirical correcting term and also channel length modulation and vertical field effect have been considered as conventional multiplicative terms. Another simple model has been addressed in [25], in which channel length modulation has been considered as a function of gate voltage. In [25] has been noted that for small gate voltages, neither their model, nor other available models are not accurate.

A new theory of operation of nanometer scale MOS transistors, i.e. quasi-ballistic transport model has been proposed in [36], instead of conventional velocity saturation theory, and a model has been developed, based on this theory. Measurement results in [1] for sub-0.1 um scale shows that both of velocity saturation and transport models are good for large gate voltage, i.e. in well saturated condition. However for small gate voltages velocity saturation model is not accurate, but the transport model is well fitted to measurement results.

Overview of available I-V models show that various models have been presented for short channel MOS transistors. However each of available models for sub-0.1um MOS technologies is suitable for special measurement results and there is not any conventionally accepted model. In our knowledge, the model presented by Hauser in [4] is the most theoretically acceptable model. However this model has some shortages, as noted in [1]. In addition Hauser model does not capture the stress effect. Consequently we have developed our model based on our requirements.

II.2.1.1 Our I-V model

Our single-equation model is based on the linear dependency of drain current to gate voltage in saturation region in sub-0.1 um MOS technologies. The equation is as follows:

$$I_{ds} = \frac{\mu_0 C_{ox} W_{eff}}{L}(\eta V_{od} + \lambda V_{ds}) \quad \text{(II-8)}$$

V_{od} is the over-drive voltage, defined in (II-3). V_{th} is the threshold voltage. Although complete formulas are available in most text books, it can be calculated as a linear function of the voltage between source and bulk nodes, V_{sb} [37]. We have used a second order polynomial to calculate the threshold voltage:

$$V_{th} = V_{th0} + \gamma_1 V_{sb} + \gamma_2 V_{sb}^2 \quad \text{(II-9)}$$

In which γ_1 and γ_2 are constants. V_{th0} is the threshold voltage when source-bulk voltage is zero. The coefficient η is for capturing the mobility reduction and velocity saturation effects, and is defined as:

$$\eta = \sqrt{\frac{V_{od}}{1 + \frac{V_{dsat}^2}{V_{ds}^2}}} V_{dsat} \quad \text{(II-10)}$$

V_{dsat} is the drain-source saturation voltage. Different equations have been derived for V_{dsat} [38], [39], [40]. We have used the equation of [38] has been rewritten in [39] as:

$$V_{dsat} = \frac{V_{od}}{\alpha_x} \quad \text{(II-11)}$$

Where α_x is a function of gate-source and gate-bulk voltages. However we found an empirical equation to calculate α_x:

$$\alpha_x = \frac{\phi_0^2 + V_{od}^2}{V_{th0}} \quad \text{(II-12)}$$

In which V_{th0} is the threshold voltage when V_{sb} is zero, ϕ_0 is a constant voltage, that in our case is equal to the junction built in potential. The role of η is soft transition from linear region to saturation region, as well as modeling the electron mobility degradation and velocity saturation. Regarding (II-8) and comparing it with Shockley model we can define:

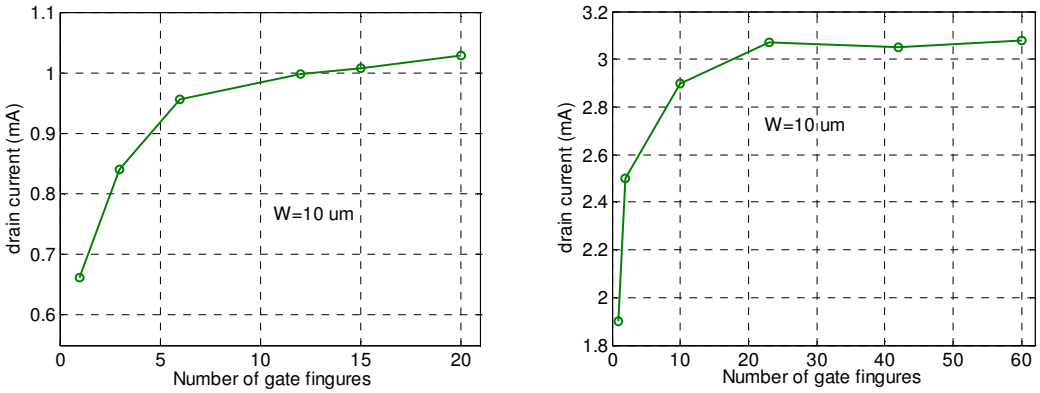


Fig. II-1. Ids for two value of W=10 um and W=30 um, and different finger sizes

$$\begin{cases} \mu_{eff} = \mu_0 \dfrac{V_{dsat}}{\sqrt{V_{od}\left(1+\dfrac{V_{dsat}^2}{V_{ds}^2}\right)}} & V_{ds} > V_{dsat} \\ \mu_{eff} = \mu_0 \sqrt{\dfrac{V_{dsat}^2}{V_{ds}^2 + V_{dsat}^2}} & V_{ds} < V_{dsat} \end{cases} \tag{II-13}$$

The coefficient λ denotes the channel length modulation effect. In [25] λ has been calculated as a function of V_{gs} and in [37] it has been calculated as a function of V_{sb}. However we found empirically that λ is function of both of V_{gs} and V_{sb}. We have adapted the empirical equation as in below to calculate λ:

$$\lambda = \frac{\lambda_0 V_{od}}{\sqrt{V_0^2 + V_{od}^2}} \tag{II-14}$$

V_0 and λ_0 both are constant coefficient. λ_0 is equal to the value of λ for large gate voltages.

W_{eff} is the effective gate width and is different from the drown W, to include the effect of fabrication process on W and to compensate the probable errors due to the stress effects and quasi-two-dimensional assumption in BSIM3v3. To give a view of how much these effects are important, I_{ds} has been shown in Fig. II-1 for two value of *W=10* um and *W=30* um, and different gate finger sizes These results have been obtained from the foundry design kit. We have calculated W_{eff} as follows:

$$W_{eff} = \frac{q_1 N_f}{N_f + q_2} W \tag{II-15}$$

In which q_1 and q_2 are constants and N_f is the number of gate fingers.

To evaluate our I-V model, we have compared it with the STMicroelectronics foundry design kit for 90nm CMOS technology. The results have been shown in Fig. II-2. This figure clearly shows the accuracy of our model. The effect of number of gate fingers on the drain current has been shown in Fig. II-3, for in our model in comparison with the foundry design kit.

II.2.2 Capacitances Model

First capacitance models were derived as a function of transistor nodes voltage [41]. Then in consequence of charge conservation and continuity problems in voltage-based models, charge-based models were introduced [42]. Various developments of charge-based models were presented as threshold voltage based, surface potential based, quasi static and non-quasi

static models [43]-[49]. In recent years CMOS technology has scaled down to the nanometer feature sizes. Accurate analysis of such devices should be performed considering quantum mechanical effects [50]. Many works has been reported on the modeling of C-V characteristic of modern CMOS transistors, based on the quantum mechanical effects [51], [52], [53]. However almost all of the available simple and professional models use charge-based modeling [43], [12], [13], [5]. So we present a review of charge based capacitance models.

Threshold voltage based charge/capacitance models, like in BSIM3 and BSIM4 models are very complicated and have many fitting parameters [44], [5], [6]. Surface potential based charge/capacitance models needs to calculate the surface potential by solving the Poisson's equation, that needs to iterative numerical calculations [14]. Some methods have been presented for this model in which charge-density approximation has been used, instead of direct solving Po equations [39], [45]. Charge-sheet model is another charge-based model in which the channel assumed as a very thin charge layer [4].

One important issue on the capacitance modeling is Non-Quasi-Static (NQS) effects. Early charge based models were derived by Quasi-Static (QS) approach. In QS approach the time dependent behavior of the channel charge build-up is neglected, assuming zero time for charges to reach their steady state condition. In principle this approach is a succession of steady state situations. However in high frequency applications the QS assumption is not valid and the channel charge becomes an explicit function of time. A first order estimate of the

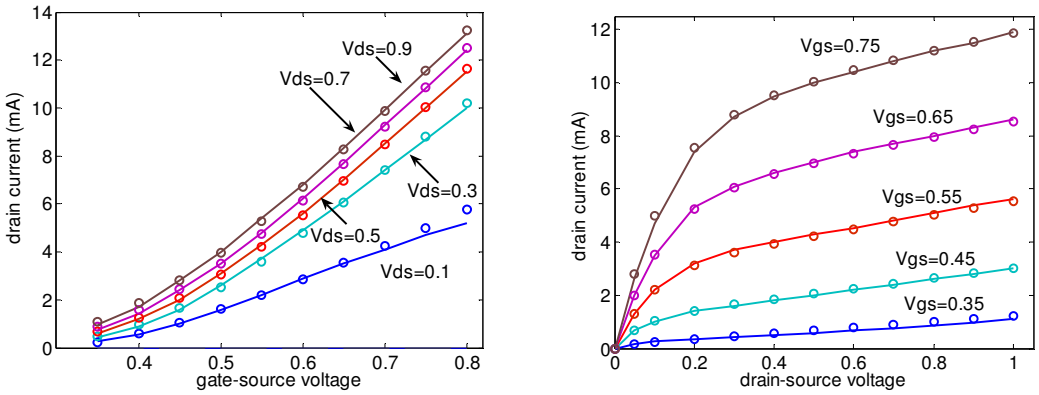


Fig. II-2 The I-V characteristics of our model in comparison with the foundry design kit, Circle data are from design kit.

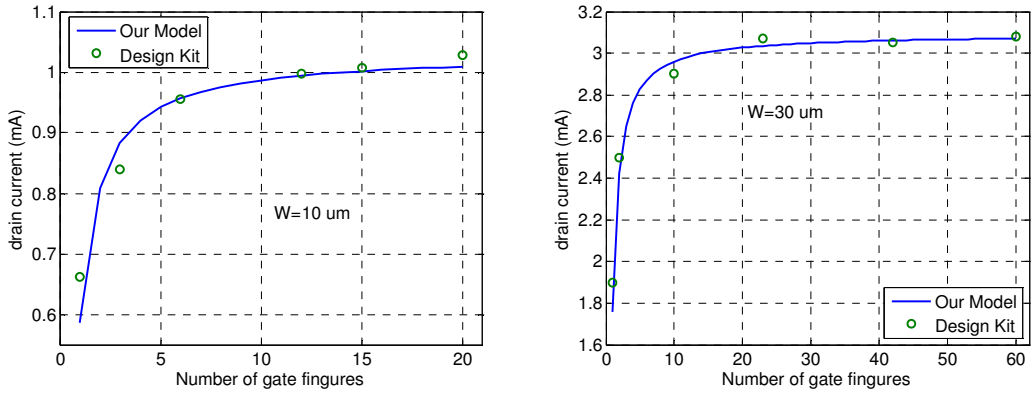


Fig. II-3 The effect of number of gate fingers on the drain current, for in our model in comparison with the foundry design kit, Circle data are from design kit.

scale in which the NQS effect becomes noticeable is the average transit time of the carriers in channel [48]. Many NQS models have been published, in which NQS effects for large signal and small signal analysis have been considered [46], [47], [48], [49]. Most of these models are very complicated and increases the simulation time up to 4 or 5 times [23]. So some approximated and simple models, such as distributed element treating of the transistor have been proposed [54]. In BSIM3v3 a simple physical NQS transient model has been used, based on the Elmore equivalent circuit [55]. This simple circuit introduces the charges build-up time, equal to the time constant of the Elmore equivalent resistance and the gate capacitance [23]. Although bsim3v3 has been used in many professional simulators and foundry design kits, analysis and simulation results in [48] show that this model can not accurately model the NQS effects in high frequencies. Capacitance modeling in BSIM4.3.0 is similar to BSIM3v3. However BSIM4 used two first order modeling for NQS effects for large signal analysis and introduces NQS effect in small signal capacitances and trans-conductance [24]. In [26] a very simple model has been presented. This model is fully empirical and hence is suitable for special cases.

II.2.2.1 Our Capacitance Model

The capacitance equations in our model have been simply derived using some basic analysis and fitting to the design kit. For zero drain-source voltage and neglecting bulk charges in strong inversion (SI) regime [43], we have:

$$Q_{c0}^{SI} = W_{eff} L_{eff} C_{ox} \left(V_{gs} - V_{th} \right) \tag{II-16}$$

And in sub-threshold (ST) region we have :

$$Q_{c0}^{ST} = Q_0 \exp\left(\frac{V_{gs} - V_{th} - V_{off}}{n \nu_t} \right) \tag{II-17}$$

In which Q_0 is determined from technology parameters [4]. V_{off} is small offset voltage to correct the threshold voltage to best fit the measurement results. n is constant between 1 and 2 and v_t is the thermal voltage. These equations are not continued and hence cause problem in calculating the capacitances. One solution is correction of equations (II-16) and (II-17) to obtain the continuity of charge and its first derivative at $V_{gs}=V_{th}$. For this purpose we should correct the first equation as:

$$Q_{c0}^{SI} = W_{eff} L_{eff} C_{ox} \left(V_{gs} - V_{th} \right) + Q_0 \exp\left(\frac{-V_{off}}{n \nu_t} \right) \tag{II-18}$$

And to obtain the continuity of the derivative of charge at $V_{gs}=V_{th}$,we should have:

$$V_{off} = n \nu_t \ln\left(\frac{Q_0}{n \nu_t W_{eff} L_{eff} C_{ox}} \right) \tag{II-19}$$

The normalized charge and its derivatives, calculated from above equations have been depicted in Fig. II-4, in comparison with the derivative of the channel charge, obtained from the foundry design kit. From this figure, the second derivative of the charge is not continuous and this cause large error in calculation of capacitors. So we perform another improvement, with defining V_{gs} in the strong-inversion region as follows:

$$V'_{gs} = \sqrt[p]{V_{gs}^{\,p} + V_{th}^{\,p}} \tag{II-20}$$

And the channel charge in the strong-inversion region is calculated as:

$$Q_{c0}^{SI} = W_{eff} L_{eff} C_{ox} \left(V'_{gs} - \sqrt[p]{2} V_{th} \right) + Q_0 \exp\left(\frac{-V_{off}}{n \nu_t} \right) \tag{II-21}$$

to obtain the continuity of the derivative of charge at $V_{gs}=V_{th}$,we should have:

$$V_{off} = n\nu_t \ln\left(\frac{Q_0}{n\nu_t W_{eff} L_{eff} C_{ox}} 2^{\left(1-\frac{1}{p}\right)}\right) \tag{II-22}$$

the normalized charge and its derivatives, calculated from above equations have been depicted in Fig. II-4. In this figure the charges and the derivatives have been normalized to $W_{eff} L_{eff} C_{ox}$ and C_{ox}, respectively. Now the second derivative is continuous. Note that the difference between the modified equation and the design kit result is due to the bulk charge that has not been included in our equations.

The other approach is to use a unifying function to unify the equations (II-16) and (II-17) into a single equation. In [39] a unifying function has been presented for soft transition from sub-threshold to strong inversion. This unifying function has been widely used in reported models [56], [23], [39]. Here we rewrite after introducing the small offset voltage:

$$Q_{c0} = W_{eff} L_{eff} C_{ox} n\nu_t \ln\left(1+\exp\left(\frac{V_{gs}-V_{th}-V_{off}}{n\nu_t}\right)\right) \tag{II-23}$$

This function goes to (II-16) for large V_{gs} and has semi-exponential increase for small V_{gs}. Fig. II-5 shows this function and its first derivative, normalized to $W_{eff} L_{eff} C_{ox}$ and C_{ox}, respectively, in comparison with the exponential equation of (II-17). The effect of V_{off} has been shown in this figure. From this figure unified equation (II-23) has very good agreement with both of equations (II-16) and (II-17). Due to its accuracy, as well as single equation property, we use it in our model.

A) V_{ds} Effect on the Channel Charge

Now the effect of V_{ds} in the channel charge should be included. For this purpose we use proper approximations separately in linear and saturation regions, and then we will unify the obtained equations to obtain our single-equation channel charge model.

In the linear region we assume that the channel charge density linearly reduces from source to drain, due to drain voltage. So we have:

$$\begin{cases} Q_{c\_lin} = Q_{c0} & V_{ds} = 0 \\ Q_{c\_lin} = \dfrac{Q_{c0}}{2} & V_{ds} = V_{dsat} \end{cases} \tag{II-24}$$

To express this in a single equation we use:

$$Q_{c\_lin} = Q_{c0}\frac{2V_{dsat}-V_{ds}}{2V_{dsat}} \tag{II-25}$$

However this equation is valid in the linear region, so we should restrict V_{ds} to this region. To do so, we define the voltages:

$$\begin{aligned} V'_{ds} &= \sqrt[q]{V_{ds}^q + V_{dsat}^q} - V_{dsat} \\ V''_{ds} &= V_{ds} - V'_{ds} \end{aligned} \tag{II-26}$$

where q is a fix parameter and V_{dsat} is drain-source saturation voltage and was calculated in (II-11), however here we use other equation for it, that is consistent with (II-11), but is more soft function.

$$V_{dsat} = \frac{V_\infty}{2}\left(1+\tanh\left(k\left(V_{gs}-V_{off}\right)\right)\right) \tag{II-27}$$

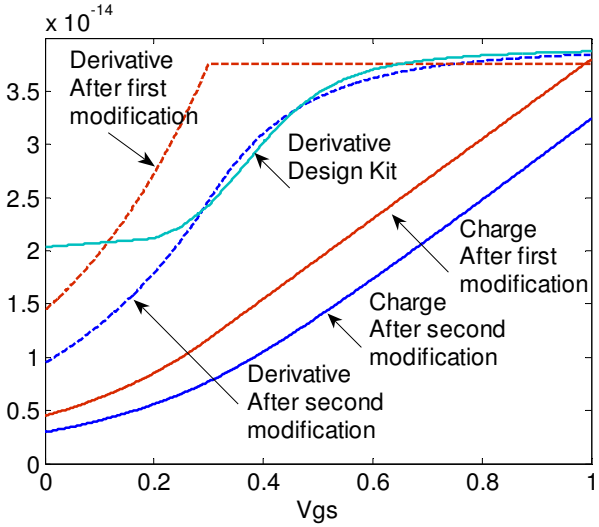


Fig. II-4. Channel charge and its derivative calculated from (II-16) and (II-17), after our first and second modifications. Charges and derivatives have been normalized to $W_{eff}L_{eff}C_{ox}$ and C_{ox}, respectively.

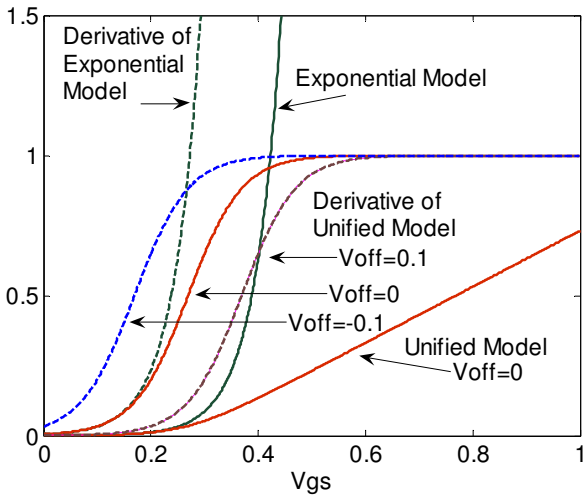


Fig. II-5. The unified function of (II-23) and its first derivative, in comparison with the exponential equation of (II-17). Charges and derivatives have been normalized to $W_{eff}L_{eff}C_{ox}$ and C_{ox}, respectively.

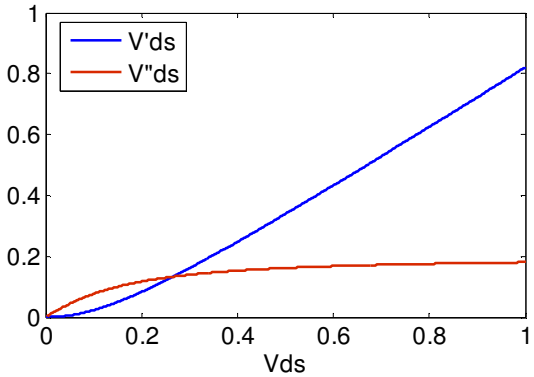


Fig. II-6. V'_{ds} and V''_{ds} defined in (II-26) for q=2 and Vdsat=0.2

V_∞ is the saturation voltage for very large gate voltages and k is constant and V_{off} is constant offset voltage. V'_{ds} and V''_{ds} have been shown in Fig. II-6 for $q=2$. So to restrict V_{ds} in (II-25) to linear region we rewrite (II-25) as:

$$Q_{c\_lin} = Q_{c0}\frac{2V_{dsat} - V''_{ds}}{2V_{dsat}} \tag{II-28}$$

In saturation, for long channel devices V_{ds} has no considerable effect on the channel charge. However in the case of short channel devices the effect must be considered. For this purpose we have used very simple model. Neglecting the charge density of pinched off part of the channel, in comparison with the channel charge density in strong inversion we deduce:

$$Q_{c\_sat} = Q_{c\_lin}\left(\frac{L-x}{L}\right) \tag{II-29}$$

In which x is the length of pinched off part of the channel, that clearly shows the channel length modulation effect. L is the channel length. x is a function of nodes voltages is a function of channel charge, drain-source voltage and saturation voltage, V_{dsat} [40]. We have calculated it as:

$$x = \frac{f\left(V_{ds} - V_{dsat}\right)}{Q_{c0}} \tag{II-30}$$

Q_{c0} in the denominator steams intuitively from decreasing the channel length modulation with increasing the channel charge. We found the approximation of the function f as below, off adequate accuracy:

$$\begin{cases} x = 0 & V_{ds} < V_{dsat} \\ x = \dfrac{\lambda_1\left(V_{ds} - V_{dsat}\right) + \lambda_1\left(V_{ds} - V_{dsat}\right)^2}{Q_{c0}} & V_{ds} > V_{dsat} \end{cases} \tag{II-31}$$

V_{dsat} is the drain saturation voltage, defined in (II-27), λ_1 and λ_2 are constant parameters and Q_{c0} is calculated from(II-23). With using V'_{ds} defined in (II-26) instead of V_{ds}, we can unify (II_31) as:

$$x = \frac{\lambda_1 V'_{ds} + \lambda_2\left(V'_{ds}\right)^2}{Q_{c0}} \tag{II-32}$$

Finally our single equation channel charge model obtained as follows:

$$Q_c = Q_{c\_lin}\left(\frac{L-x}{L}\right) \tag{II-33}$$

In which Q_{c_lin} and x are calculated from (II-28) and (II-32), respectively.

B) Bulk Charge and Junction Capacitance Models

In the case of NMOS transistor for large negative gate voltages, the bulk charge increases linearly with decreasing the gate voltage (being more negative). This is the accumulation phase and starts from a special threshold that we denote it as accumulation threshold, V_{ac}. On the other hand for large positive gate voltages (strong inversion region) the bulk charge is constant, at its minimum value. For the voltages between V_{th} and V_{ac} the depleted region is increased with increasing the gate voltage and hence the bulk charge decreases. However in this phase the charge reduction rate is smaller than that of accumulation phase. These three phases have been shown in the measurement and simulation data in different works [57], [45], [44], [39], [15].

Based on the above three phases we have used the empirical equation as below to calculate the bulk charge:

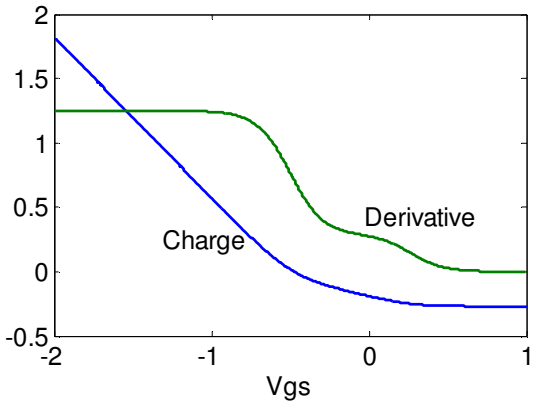


Fig. II-7. Normalized bulk charge and its derivative calculated from (II-34), for n=3, Vth=0.27 and Vac=-0.5

$$Q_b = C_1 V_1 + C_2 V_2 + Q_{bSI} \tag{II-34}$$

In which C_1 represents the gate-bulk capacitance for strong accumulation region, C_2 is the gate-bulk capacitance in vicinity of zero gate voltage and Q_{bSI} is the bulk charge in the strong inversion region and approximately is zero. V_1 and V_2 are calculated as follows:

$$\begin{aligned} V_1 &= nv_t \ln\left(1+\exp\left(\frac{-V_{gs}+V_{ac}}{nv_t}\right)\right) \\ V_2 &= nv_t \ln\left(1+\exp\left(\frac{-V_{gs}+V_{th}}{nv_t}\right)\right) \end{aligned} \tag{II-35}$$

n is a constant parameter and v_t is thermal voltage. Bulk charge and its derivative obtained from (II-34) has been depicted in Fig. II-7.

The source and drain junction capacitors are calculated traditionally as in [31]:

$$C_{jx} = C_{jx0}\left(1+\frac{V_{xb}}{\phi_0}\right)^{-mjx} \tag{II-36}$$

Where x denotes the drain or source nodes. mjx is a technology dependent parameter, near to 0.5. mjx can also be interpreted as $n/(n+1)$ [58]. This equation has also been used in BSIM4.3.0 models with slight difference.

C) Nodal Charges, Capacitances and trans-capacitances

Now we should calculate the nodes charge. Gate charge is equal to the channel charge and depletion layer charge. However in strong inversion the depletion layer charge is negligible and hence the gate charge is simply calculated as:

$$Q_g = Q_c \tag{II-37}$$

To calculate the source and drain charges, we use the charge partitioning approaches, developed by Ward and Dutton [42]. Based on the Wards second approach, we have:

$$\begin{aligned} Q_d &= bQ_c \\ Q_s &= (1-b)Q_c \end{aligned} \tag{II-38}$$

b is a function of drain source voltage. In the linear region we use b=0.5 that means 50/50 charge partitioning. In the saturation region Ward's accurate numerical approach leads to $b=2/5$ or well-known 40/60 charge partitioning. This approach has been widely used in BSIM3, BSIM4 and many other developed models [47], [39]. Smooth transition of change partitioning from linear to saturation has been obtained in [14] with complicated analysis. However to uniformly change of b from 50/50 to 40/60 regimes, we calculate b as follows:

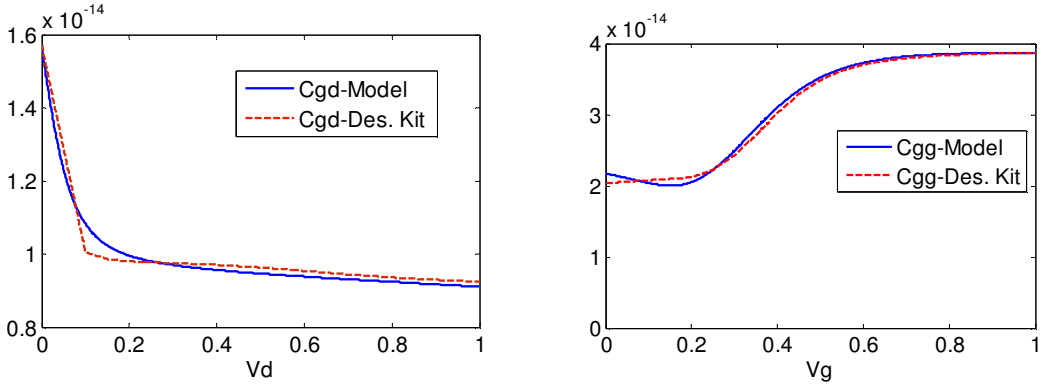


Fig. II-8. C_{gd} and C_{gg} of the transistor capacitances, calculated form our model, in comparison with the foundry design kit data

$$b = \frac{1}{2} - \frac{1}{10}\tanh\left(\frac{V'_{ds}}{V_{cp}}\right) \tag{II-39}$$

V_{cp} is a constant voltage that controls the transition slope.

Having the gate, source and drain charges one can simply calculate the small signal capacitance and trans-capacitances as follows:

$$C_{ij} = \frac{\partial Q_i}{\partial V_j} \tag{II-40}$$

In which i and j stand for gate, source and drain nodes. Different capacitances have been calculated in Appendix A. Here to evaluate our model, some of the calculated capacitances have been shown in Fig. II-8, in comparison with the foundry design kit data.

II.2.3 Small Signal Model

The commonly used small signal model for intrinsic MOS transistor for RF applications has been shown in Fig. II-9 [59], [60]. In this model R_g represents the small resistance due to the distributed resistance of gate interconnects. R_g will be discussed in detail in next sections and we will propose our new model for it. R_{gs} accounts for non-quasi-static nature of the channel and will be discussed in this section. Capacitances in the model were calculated in the previous section. g_m and g_{ds} is calculated in this section using our I-V model in the previous section. Please note that this model is only for transistor core and is too simple to be used as a complete small signal model in MMW frequencies. In future we will describe our small signal and Y parameter model for a complete transistor.

Before small signal analysis, the transistor's bias condition should be calculated with DC analysis, using the large signal model of transistor. Then the bias condition is used for

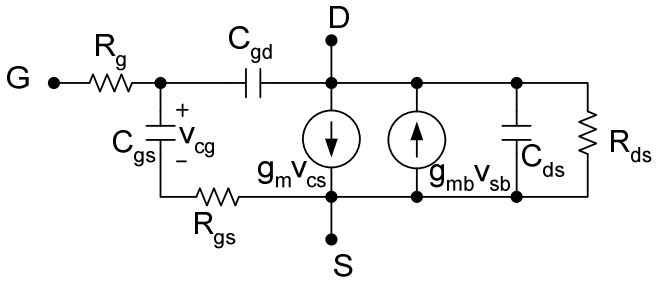


Fig. II-9. Commonly used small signal model for MOS transistor core

calculating g_m, g_{mb} and g_{ds} using mathematical equations, derived from I-V model as well as for calculating small signal capacitors.

Using (II-8) the small signal conductance and trans-conductance of the small signal model is calculated. The small signal trans-conductance is obtained as:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{\mu_0 C_{ox} W_{eff}}{L_{eff}} \left(\eta + V_{od} \frac{\partial \eta}{\partial V_{od}} + \frac{\partial \lambda}{\partial V_{od}} V_{ds} \right) \tag{II-41}$$

where η and λ have been defined in (II-10) and (II-14), respectively. Using (II-14) we have:

$$\frac{\partial \eta}{\partial V_{od}} = \frac{\eta}{V_{od}} \left(\frac{1}{2} + \frac{\eta^2}{V_{dsat}^3} \frac{\partial V_{dsat}}{\partial V_{od}} \right) \tag{II-42}$$

V_{od} is the gate over-drive voltage, defined in (II-3) and V_{dsat} is the drain-source saturation voltage, calculated in (II-11). Using the equation for V_{dsat} we obtain:

$$\frac{\partial V_{dsat}}{\partial V_{od}} = V_{th0} \frac{\phi_0^2 - V_{od}^2}{\left(\phi_0^2 + V_{od}^2\right)^2} \tag{II-43}$$

And using the equation for λ in (II-14) we deduce:

$$\frac{\partial \lambda}{\partial V_{od}} = \frac{\lambda^3 V_0^2}{\lambda_0^2 V_{od}^3} \tag{II-44}$$

g_m calculated from (II-41), has been shown in Fig. II-10 as a function of V_{ds} for some values of V_{gs}.

The small signal drain-source conductance is calculated as:

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} = \frac{\mu_0 C_{ox} W_{eff}}{L} \left(V_{od} \frac{\partial \eta}{\partial V_{ds}} + \lambda \right) \tag{II-45}$$

using the equation for η in (II-10) we obtain:

$$\frac{\partial \eta}{\partial V_{ds}} = \frac{\eta^3}{V_{od} V_{ds}^3} \tag{II-46}$$

Consequently the small signal drain-source conductance at zero drain-source voltage is obtained as:

$$g_{ds0} = \frac{\mu_0 C_{ox} W_{eff}}{L} \left(V_{od}^{3/2} + \lambda \right) \tag{II-47}$$

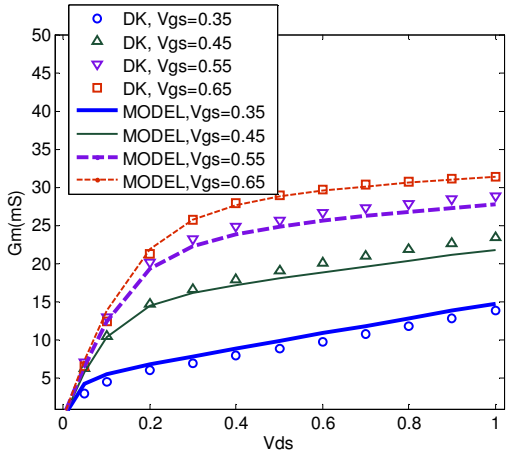


Fig. II-10. g_m versus V_{ds} for various V_{gs}, obtained from our model, in comparison with the 90nm CMOS foundry design kit. (On the figure, DK: Design Kit, MODEL: Our model in II-41))

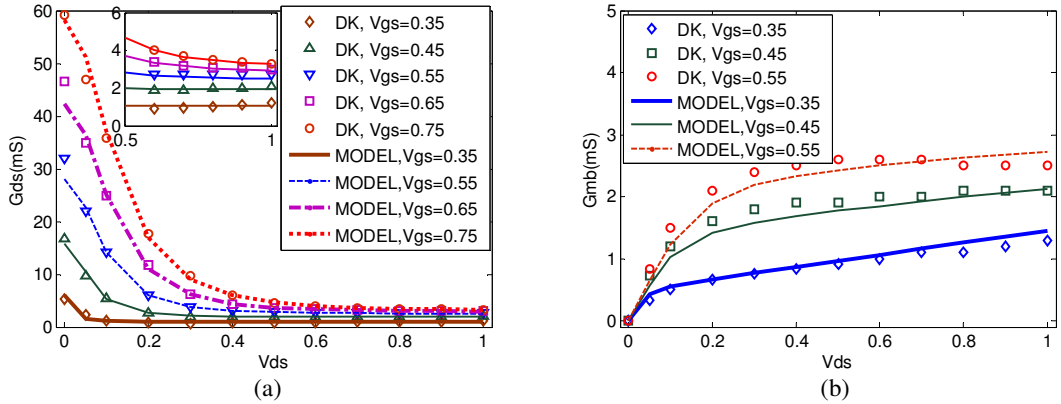


Fig. II-11. g_{ds} (a) and g_{mb} versus V_{ds} for various V_{gs}, obtained from our model, in comparison with the 90nm CMOS foundry design kit. (On the figure, DK: Design Kit, MODEL: Our model in II-41))

And finally the small signal source-bulk trans-conductance is calculated as:

$$g_{mb} = \frac{\partial I_{ds}}{\partial V_{bs}} = -g_m \frac{\partial V_{th}}{\partial V_{bs}} \tag{II-48}$$

Using the threshold voltage equation in (II-9) we obtain:

$$g_{mb} = -g_m\left(\gamma_1 + 2\gamma_2 V_{sb}\right) \tag{II-49}$$

V_{sb} is the source-bulk voltage, γ_1 and γ_2 are constant body effect parameters, defined in (II-9). g_{ds} and g_{mb}, calculated from (II-45) and (II-49), has been shown in Fig. II-11 as a function of V_{ds} for some values of V_{gs}.

II.2.3.1 Non-Quasi-Static Effect

NQS effect is considered as a consequence of the required transport time of the charges along the channel length, from source to drain [38]. As we mentioned earlier, many complicated models have been proposed to deal with NQS effect. However most of practical transistor models use approximated approaches for this effect. In [61] and [40] analytic equations have been developed to express the NQS effects on small signal model. Based on this analysis, the small signal trans-conductance and gate capacitance is scaled as:

$$\begin{aligned} g_{m\_nqs} &= \zeta_m g_m \\ g_{mb\_nqs} &= \zeta_m g_{mb} \end{aligned} \tag{II-50}$$

ζ_m is NQS scaling function, defined as:

$$\zeta_m = \frac{\nu}{\sinh(\nu)} \tag{II-51}$$

In which:

$$\nu = (1+j)\sqrt{3\omega\tau_{nqs}} \tag{II-52}$$

τ_{nqs} is the NQS time constant and in the strong inversion region is calculated as:

$$\tau_{nqs} = \frac{nL_{eff}^2}{\mu_{eff}\left(V_g - V_{th0} - nV_s\right)} \tag{II-53}$$

Where n is a constant parameter. For gate capacitance, the NQS scaling function has been obtained as:

$$\zeta_c = \frac{\cosh(\nu)-1}{\nu\sinh(\nu)} \tag{II-54}$$

Assuming $\omega\tau_{nqs} < 1$ the first approximation of (II-51) and (II-54) is obtained as:

$$\zeta_m = \frac{1}{1 + j\omega\tau_{nqs}}$$
$$\zeta_c = \frac{1}{1 + j\frac{\omega\tau_{nqs}}{2}} \quad \text{(II-55)}$$

These first order approximations can be introduced in the transistor small signal model, simply by adding a resistance in series with gate-source capacitance, as in Fig. II-9. Doing this, from Fig. II-9 we have:

$$g_{m\_nqs} = \frac{1}{1 + j\omega C_{gs} R_{nqs}} g_m$$
$$C_{gs\_nqs} = \frac{1}{1 + j\omega C_{gs} R_{nqs}} C_{gs} \quad \text{(II-56)}$$

This approximation has been used in BSIM3v3 and BSIM4.3.0 models, as well as in other models [60], [38]. R_{nqs} in BSIM3v3 and BSIM4.3.0 has been noted as R_{Elmore} and R_{ii} (Intrinsic Input Resistance), respectively and is calculated as:

$$R_{nqs} = \frac{L_{eff}^2}{\varepsilon \mu_{eff} Q_{ch}} \quad \text{(II-57)}$$

Where ε is the Elmore constant, theoretically equal to 5, μ_{eff} is the effective mobility and Q_{ch} is the equivalent channel charge, calculated in (II-13) and (II-33), respectively. In our case Leff is *(L-x)*, *x* calculated in (II-32). It must be noted that (II-57) and (II-53) have the same origin. This can be shown simply by substituting Q_{ch} with $C_{gs}(V_{gs}-V_{th})$, as in [4] and defining τ_{nqs} as $R_{nqs}C_{gs}$. Equation (II-57) shows the quadratic decrease of NQS effect with decreasing channel length. So in practical measurement of NQS effects, transistors with very large gate length are fabricated, e.g. 300um in 0.5 um technology [60], so that the NQS effect is evident.

To give a sense about the NQS static effects in the technology used in our work, i.e. 90nm CMOS, We have calculated ζ_m from (II-55), using the foundry DRM data. Fig. II-12 shows the amplitude and phase of ζ_m, with respect to frequency. This figure shows that at our design frequency, i.e. 30 GHz, NQS effects are not negligible.

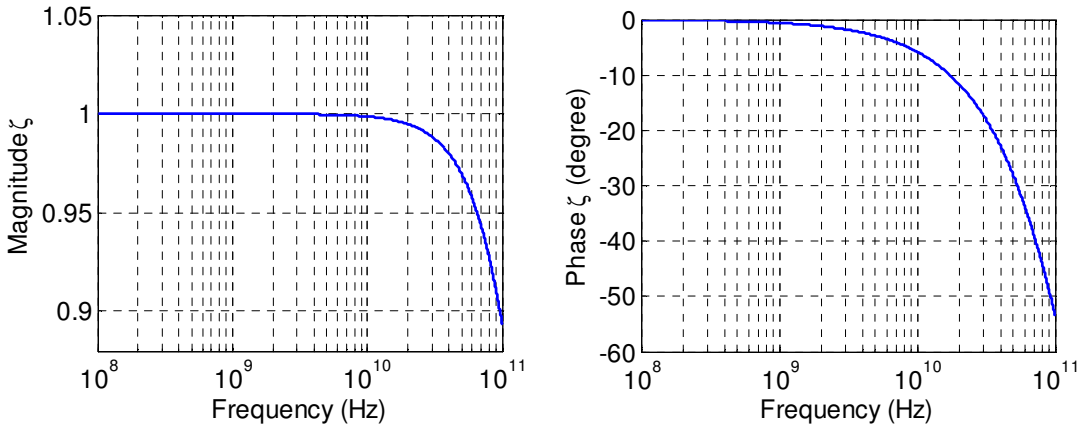


Fig. II-12. Magnitude and phase of ζ_m, calculated using (II-55) and for 90nm CMOS technology

II.2.4 Noise Model

As CMOS technology expands into the RF band, high frequency noise performance of MOS transistor becomes more important and having a good noise model is an essential need. In this context, first modeling was proposed by Van Der Ziel in 1963 in suggestion of noise in FET transistors [62]. Then V.Z. model was proven and accepted as a successful noise model for old CMOS technologies [63], [64], [65], [66]. Based on V. Ziel noise model, the main noise

contribution is due to the channel thermal noise, modeled as a current source between drain and source and calculated as:

$$\frac{\overline{i_{nd}^2}}{\Delta f} = 4kT\gamma \cdot g_{d0} \tag{II-58}$$

In which k is the Boltzmann's constant, T is the ambient temperature. γ is a function of device parameters and bias and its value is between 2/3 for saturation region and 1 for *Vds=0*. g_{d0} is the channel conductance in zero drain-source voltage

The other noise mechanism in V. Ziel model is the induced gate noise, modeled as a shunt current source parallel, calculated as:

$$\frac{\overline{i_{ng}^2}}{\Delta f} = 4kT\delta \cdot g_g \tag{II-59}$$

δ is a bias-dependent parameter and g_g is the noise equivalent conductance in the gate node.

However in short channel MOS transistors this model underestimates the noise performance and hence in many works higher values of γ have been addressed [65], [67], [68], [69]. Chen *et al.* developed a scenario for measurement and extraction of MOS transistor noise parameters, specially the gate induced noise and compared the results with V. Ziel model. They addressed noticeable discrepancy of the V. Ziel model with the measurement results [70].

In recent years many researches have been focused on the noise modeling in MOS transistors. Unfortunately the obtained results are not consistent with each other. The common note accepted by all reports is that the main noise contribution is due to the channel thermal noise, as claimed by V. Ziel [71], [72]. Also it was accepted that the gate induced noise is not important for frequencies below much lower than the transistor cutoff frequency, f_T ($f_T/f > 10$) [72], [73]. Many complicated models have been derived from physical analysis of the channel charge and current. Some of these models express the excess noise (in comparison with V. Ziel model) is due to the velocity saturation and hot electron effects in deep submicron devices [74], [75]. In contrast, some other works declaimed this theory and presented different ideas. Scholten *et al.* found that the experimental data can be explained with considering the noise only in the Gradual Channel Region (GCR) (see Fig. II-13) and hence it not necessary to deal with the high-filed effects at high V_{ds} [76]. Goo *et al.* presented a simulation based technique and showed that the main noise contribution comes from GCR and hence has the ohmic nature [77]. Some other works considered both of GCR and VS (velocity saturation) region, as well as channel length modulation [77]. In [71] a physical based compact noise model was developed with treating the channel as a serious of infinitesimal resistors. Chen *et al.* In [78] claimed that the excess noise is due to CLM, not the velocity saturation, because electrons in VS region has not the ability of random moving.

Induced gate noise has not been considered in BSIM models, prior to BSIM4. The noise model used in BSIM4 is based on the model in [77]. BISM4 noise model was studied in [79] and it is shown that this model may leads to erroneous results, in the case of induced gate noise. In [80] has been shown experimentally that BSIM4 noise model is not accurate in for 90nm CMOS technology, in 1.0GHz to 18GHz, but good agreement was achieved after

adding a frequency-dependent noise source in the gate, as in V. Ziel model. PSP model uses the improved Klassman Prins equation in modeling the channel thermal noise. This model has specially developed for sub-0.1um technologies and has been accepted by CMC[2] as standard MOS transistor model [81]. PSP noise model comprises the induced gate noise and velocity saturation effects. Experimental results in [82] show significant increase of the noise with increasing the drain voltage, in the case of 70nm CMOS technology. The authors explained that this is due to the CLM and increasing the short channel effect. Other noise sources such as the shot-noise due to the impact ionization have been considered in noise modeling [72].

In contrast to the complicate models, presented in recent years, V. Ziel model, although underestimates the noise parameters, but have very good prediction of the noise behavior of sub-0.1um technologies [71]. This can be deduced from the measurement results in [70] for 0.18um technology, in [80] for 90nm technology and in [82] for 70nm technology. The measurement results in [70] shows that the frequency-dependent behavior of the channel thermal noise, the induced gate noise and their correlation coefficient is very near to that of V. Ziel model. The measurement results in [80] shows that adding V. Ziel idea to the BSIM4 model leads to an accurate noise model. The results in [82] reveal significant discrepancy between V. Ziel model and the measured data, however they have used fixed value for γ in V. Ziel model and instead have corrected the error with an extra voltage-dependent resistor. This is exactly equal to defining γ as a function of drain-source bias voltage. Using proper bias-dependent value for γ, very good agreement with the experimental results has been obtained, in the case of 0.18um technology [83].

Beside this, due to its simplicity, V. Ziel model has been widely used in getting insight to the noise behavior of different circuits via mathematical analysis [40], [84], [85].

Consequently we have used V. Ziel model, with defining proper equations to express the bias dependency of noise parameters to capture short channel effects, and using our I-V model to calculate the channel conductance. In summary the noise model is as follows:
The drain current noise is calculated as:

$$\frac{\overline{i_{nd}^2}}{\Delta f} = 4kT\gamma \cdot g_{d0} \qquad \text{(II-60)}$$

Where g_{d0} is the drain-source conductance at zero V_{ds} and is calculated from (II-47). γ is bias dependent noise parameter. The original bias dependency of γ has been derived by V. Ziel for long channel devices and has been used in [83] for 0.18um technology. However based on the measurement results in [70] we have defined an empirical function as below:

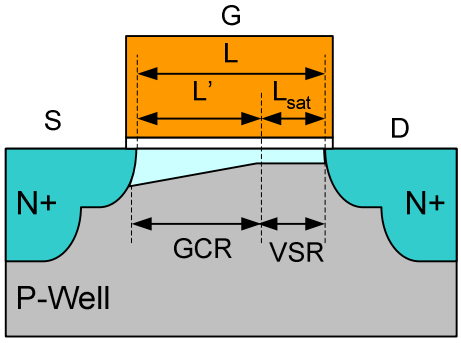


Fig. II-13. Dividing the saturated channel to Gradual Channel Region (GCR) and Velocity Saturation region (VSR) [72].

[2] Compact Model Concile

$$\gamma = \kappa \frac{\sqrt{V_{ds}^2 + V_{dsat}^2}}{V_{dsat}} \tag{II-61}$$

where κ is a constant parameter and V_{dsat} is the saturation voltage, calculated in (II-27). Based on this representation the channel noise increases linearly with V_{ds} for $V_{ds} >> V_{dsat}$ and this corresponds to the measurement results in [82] for 70nm technology. Finally the induced gate noise is calculated as:

$$\frac{\overline{i_{ng}^2}}{\Delta f} = 4kT\delta \cdot g_g \qquad \delta = 4/3 \tag{II-62}$$

in which:

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \tag{II-63}$$

Drain noise and induced gate noises have physically same origin and hence are correlated. As calculated by V. Ziel in the case of long channel device, and proven with measurement results in [70] for short channel devices, the correlation coefficient is pure imaginary and frequency independent:

$$c = \frac{\overline{I_{ng} I_{nd}^*}}{\sqrt{\overline{I_{ng}^2}\,\overline{I_{nd}^2}}} = j0.395 \tag{II-64}$$

II.3 Distributed Analysis

When the frequency increases up to a certain limit, distributed model of transistor should be considered. The limit of frequency depends on the length of different conducting objects in the MOS transistor structure, in comparison with the wavelength in that object. It is emphasized that different objects of the MOS structure have different wave propagation characteristics and hence the related wavelength in different.

The most susceptible part of a MOS transistor to the distributed effects is its gate, due to high resistance and high capacitance. Channel resistance and gate capacitance causes a delay on propagating the charges along the gate length. This is the well known non-quasi static effect that has been modeled in earlier studies as a distributed *RC* network [86], [87]. On the other hand high resistance of the gate finger, coupled with the high gate capacitance reveals slow wave along the gate width and hence the distributed modeling should be used to accurately calculate the gate admittance, as well as the transistor trans-conductance and noise performance, leading to the distributed transistor model.

Distributed nature of a MOS transistor has been considered in many works. In [88] the effect of gate resistance noise was analyzed, considering *RC* distribution along the gate width. In this work a ladder network obtained by treating the single transistor as a cascade of some small transistors via gate resistances. Razavi *et al*. investigated the effect of distributed gate resistance on f_T and f_{max} of MOS transistor [59]. They used the same approach, as in the previous work and showed that the effective gate resistance is about 1/3 of the actual gate finger resistance. In [89] transmission-line treatment and analysis has been used in development of a high frequency small signal and noise model. In our knowledge this model is the most accurate distributed model for MOS transistors. However this model is useful for a single finger transistor and is not sufficient for modeling of multi-finger transistors. On the other hand we will show that such complicated model is not necessary for a very small single finger transistor.

In this section we analyze and discus the distributed effect in the gate resistance, aiming to find:

- Maximum frequency up to which, conventional lumped model can be used.
- Beyond this frequency, can the lumped model be corrected to capture the distributed effects?

We will show that for optimum gate fingers in sub-0.1um technologies, conventional lumped element model can be used beyond the possible frequencies for MOS transistors. In addition, for some special applications the lumped element model can be used with modified element values, obtained from our analysis.

II.3.1 Distributed Model

The distributed model concept has been demonstrated by Fig. II-14. In this figure whole transistor has been broken down to infinitive number of infinitesimal transistors, denoted by δM. Each infinitesimal transistor corresponds to the infinitesimal width of gate, denoted by δx. Using this distributed representation, we deduce the distributed small signal model, shown in Fig. II-15. Y_{gd} is composed of the intrinsic C_{gd} and all of resistive-capacitive parasitics between the gate and drain fingers. Y_{gs} is a RC network composed of the gate-source intrinsic capacitance, as well as the overlap and parasitic capacitances and the Elmore resistance, representing the non-quasi-static effect, calculated in (II-57). Y_{ds} is composed of the total capacitance between drain and source fingers (intrinsic and parasitics) and the drain-source conductance. As a simple approximation one may use:

$$Y_{gs} = \frac{j\omega C_{gs}}{1 + j\omega C_{gs} R_{nqs}}$$

$$Y_{gd} = j\omega C_{gd} \qquad \text{(II-65)}$$

$$Y_{gs} = g_{gs}$$

Assuming that the transistor has been distributed homogeneously along the gate, the elements in distributed model are calculated as follows:

$$\delta g_m = \frac{g_m}{W}\delta x \qquad \delta Y_{gd} = \frac{Y_{gd}}{W}\delta x$$

$$\delta Y_{ds} = \frac{Y_{ds}}{W}\delta x \qquad \delta R_{ge} = \frac{R_{ge}}{W}\delta x = \frac{\rho_p}{L}\delta x \qquad \text{(II-66)}$$

$$\delta Y_{gs} = \frac{Y_{gs}}{W}\delta x$$

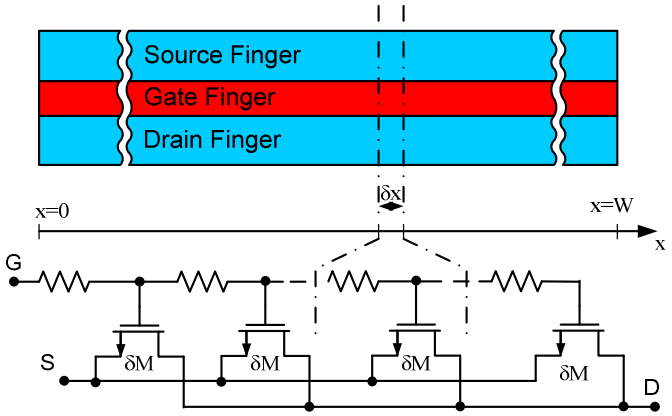


Fig. II-14. Demonstration of the distributed effect in a MOS transistor

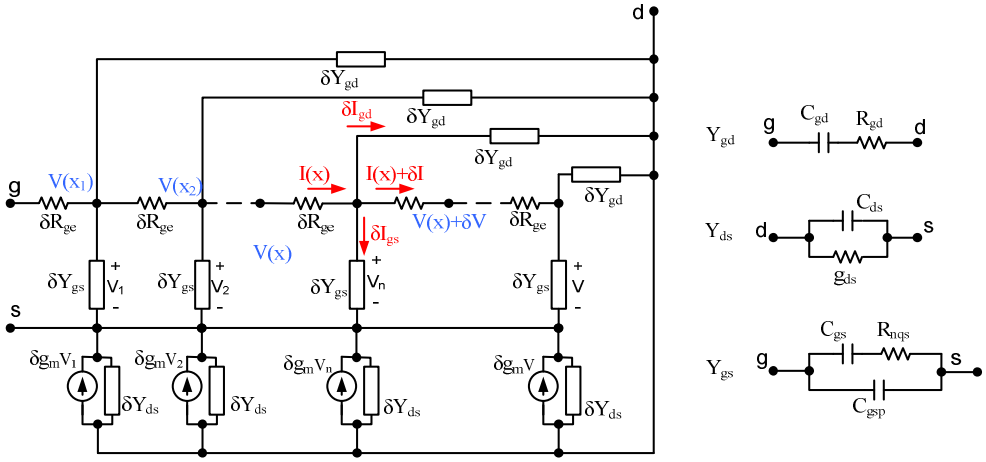


Fig. II-15. Equivalent small signal representation for distributed model of MOS transistor

R_{ge} is the gate electrode resistance, calculated as:

$$R_{ge} = \frac{\rho_p W}{L} \tag{II-67}$$

where W is the gate width, L is the gate length and ρ_p is the gate poly silicon sheet resistance. Note that R_{ge} is different from R_g that is used in the small signal lumped model, as will be described later.

The circuit of Fig. II-15 is described by a second order differential equation (See Appendix B). Solving this equation we obtain the voltage and current along the gate as:

$$V(x) = V^+ e^{-\kappa . x} + V^- e^{\kappa . x} + \frac{\rho_p}{\kappa^2 WL}\left(Y_{gd} V_d + Y_{gs} V_s\right) \tag{II-68}$$

$$I(x) = \frac{\kappa L}{\rho_p}\left(V^+ e^{-\kappa . x} - V^- e^{\kappa . x}\right)$$

In which:

$$\kappa = \sqrt{\frac{\rho_p}{WL}\left(Y_{gd} + Y_{gs}\right)} \tag{II-69}$$

ρ_p is the gate poly silicon sheet resistance. V+ and V- are found from the boundary conditions for the differential equation. To find the boundary conditions, we consider two possible ways of gate finger connection, i.e. connection to single end of the gate finger (single connection), or connection to the both ends (double connection). For single connection gate finger the required boundary conditions are:

$$\begin{aligned} V(x)\big|_{x=0} &= V_g \\ I(x)\big|_{x=W} &= 0 \end{aligned} \tag{II-70}$$

And the required boundary conditions for double connection case are:

$$\begin{aligned} V\big|_{x=0} &= V_g \\ V\big|_{x=W} &= V_g \end{aligned} \tag{II-71}$$

Using these boundary conditions one can solve (II-68) to obtain $V(x)$ and then the currents into the transistor nodes are calculated. Consequently Y parameters are calculated.

For single connection gate Y parameters are as follows (See Appendix B for details):

$$
\begin{aligned}
Y_{11} &= \left(Y_{gd}+Y_{gs}\right)\frac{\tanh\left(\kappa W\right)}{\kappa W}\\
Y_{21} &= \left(g_m-Y_{gd}\right)\frac{\tanh\left(\kappa W\right)}{\kappa W}\\
Y_{31} &= -\left(Y_{gs}+g_m\right)\frac{\tanh\left(\kappa W\right)}{\kappa W}
\end{aligned}
\qquad \text{(II-72)}
$$

$$
\begin{aligned}
Y_{12} &= -Y_{gd}\frac{\tanh\left(\kappa W\right)}{\kappa W}\\
Y_{22} &= \frac{Y_{gd}}{Y_{gd}+Y_{gs}}\left(g_m-Y_{gd}\right)\left(1-\frac{\tanh\left(\kappa W\right)}{\kappa W}\right)+\left(Y_{gd}+Y_{ds}\right)\\
Y_{32} &= -\frac{Y_{gd}}{Y_{gd}+Y_{gs}}\left(g_m+Y_{gs}\right)\left(1-\frac{\tanh\left(\kappa W\right)}{\kappa W}\right)-Y_{ds}
\end{aligned}
$$

$$
\begin{aligned}
Y_{13} &= Y_{gs}\left(1-\frac{\tanh\left(\kappa W\right)}{\kappa W}\right)-Y_{gs}\\
Y_{23} &= Y_{gs}\frac{g_m-Y_{gd}}{Y_{gd}+Y_{gs}}\left(1-\frac{\tanh\left(\kappa W\right)}{\kappa W}\right)-\left(Y_{ds}+g_m\right)\\
Y_{33} &= -Y_{gs}\frac{g_m+Y_{gs}}{Y_{gd}+Y_{gs}}\left(1-\frac{\tanh\left(\kappa W\right)}{\kappa W}\right)+\left(Y_{gs}+Y_{ds}+g_m\right)
\end{aligned}
$$

The equations for Y_{11}, Y_{12}, Y_{21} and Y_{22} are similar to that of [89].

For double connection gate Y parameters are as follows (See Appendix B for details):

$$
\begin{aligned}
Y_{11} &= \left(Y_{gd}+Y_{gs}\right)\left(2\frac{\cosh\left(\kappa W\right)-1}{\kappa W\sinh\left(\kappa W\right)}\right)\\
Y_{21} &= \left(g_m-Y_{gd}\right)\left(2\frac{\cosh\left(\kappa W\right)-1}{\kappa W\sinh\left(\kappa W\right)}\right)\\
Y_{31} &= -\left(Y_{gs}+g_m\right)\left(2\frac{\cosh\left(\kappa W\right)-1}{\kappa W\sinh\left(\kappa W\right)}\right)
\end{aligned}
\qquad \text{(II-73)}
$$

$$
\begin{aligned}
Y_{12} &= -Y_{gd}-Y_{gd}\left(2\frac{\cosh\left(\kappa W\right)-1}{\kappa W\sinh\left(\kappa W\right)}-1\right)\\
Y_{22} &= -Y_{gd}\left(\frac{g_m-Y_{gd}}{Y_{gd}+Y_{gs}}\right)\left(2\frac{\cosh\left(\kappa W\right)-1}{\kappa W\sinh\left(\kappa W\right)}-1\right)+\left(Y_{gd}+Y_{ds}\right)\\
Y_{32} &= Y_{gd}\frac{g_m+Y_{gs}}{Y_{gd}+Y_{gs}}\left(2\frac{\cosh\left(\kappa W\right)-1}{\kappa W\sinh\left(\kappa W\right)}-1\right)-Y_{ds}
\end{aligned}
$$

$$
\begin{aligned}
Y_{13} &= -Y_{gs}\left(2\frac{\cosh\left(\kappa W\right)-1}{\kappa W\sinh\left(\kappa W\right)}-1\right)-Y_{gs}\\
Y_{23} &= -Y_{gs}\frac{g_m-Y_{gd}}{Y_{gd}+Y_{gs}}\left(2\frac{\cosh\left(\kappa W\right)-1}{\kappa W\sinh\left(\kappa W\right)}-1\right)-\left(Y_{ds}+g_m\right)
\end{aligned}
$$

$$Y_{33} = Y_{gs}\frac{g_m + Y_{gs}}{Y_{gd} + Y_{gs}}\left(2\frac{\cosh(\kappa W)-1}{\kappa W \sinh(\kappa W)} - 1\right) + \left(Y_{gs} + Y_{ds} + g_m\right)$$

To validate the accuracy of results, we have simulated the distributed model of Fig. II-15 in ADS, using the foundry design kit data for 90nm CMOS technology. A single transistor with W=15um has broken to 100 sections, as in Fig. II-15. The resulted Y parameters have been compared with the Y parameters obtained from our analysis and that of the lumped model, described in the next section. Y_{11}, Y_{12} and Y_{21} have been shown in Fig. II-16 and Fig. II-17 shows Y_{13}, Y_{23} and Y_{33}.

II.3.2 Comparison With Lumped Model

The lumped small signal counterpart of the distributed model in Fig. II-15 has been shown in Fig. II-18. In this figure R_g is the effective gate resistance, calculated as [90]:

$$R_g = \alpha\frac{\rho_p W_f}{3N_f L} \tag{II-74}$$

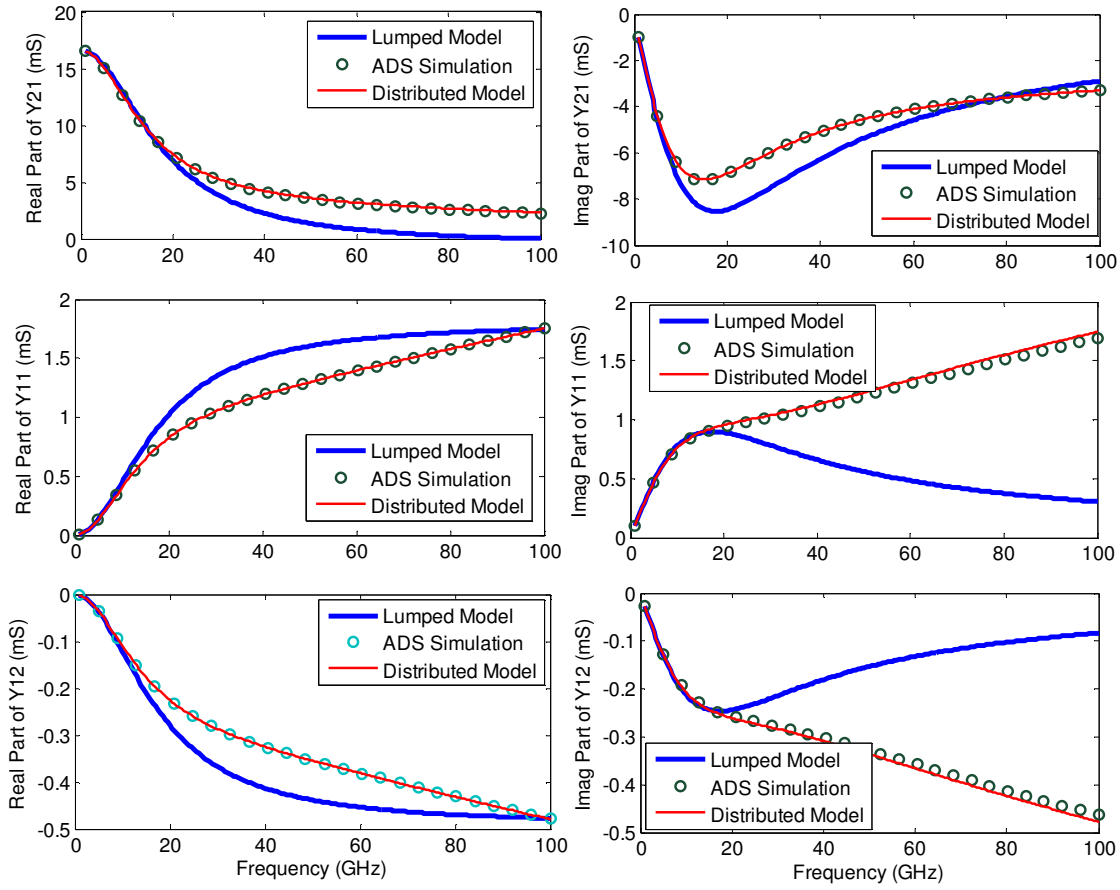


Fig. II-16. Y_{11}, Y_{12} and Y_{21} obtained from lumped model and distributed model, in comparison with the simulation in ADS for 90nm CMOS technology

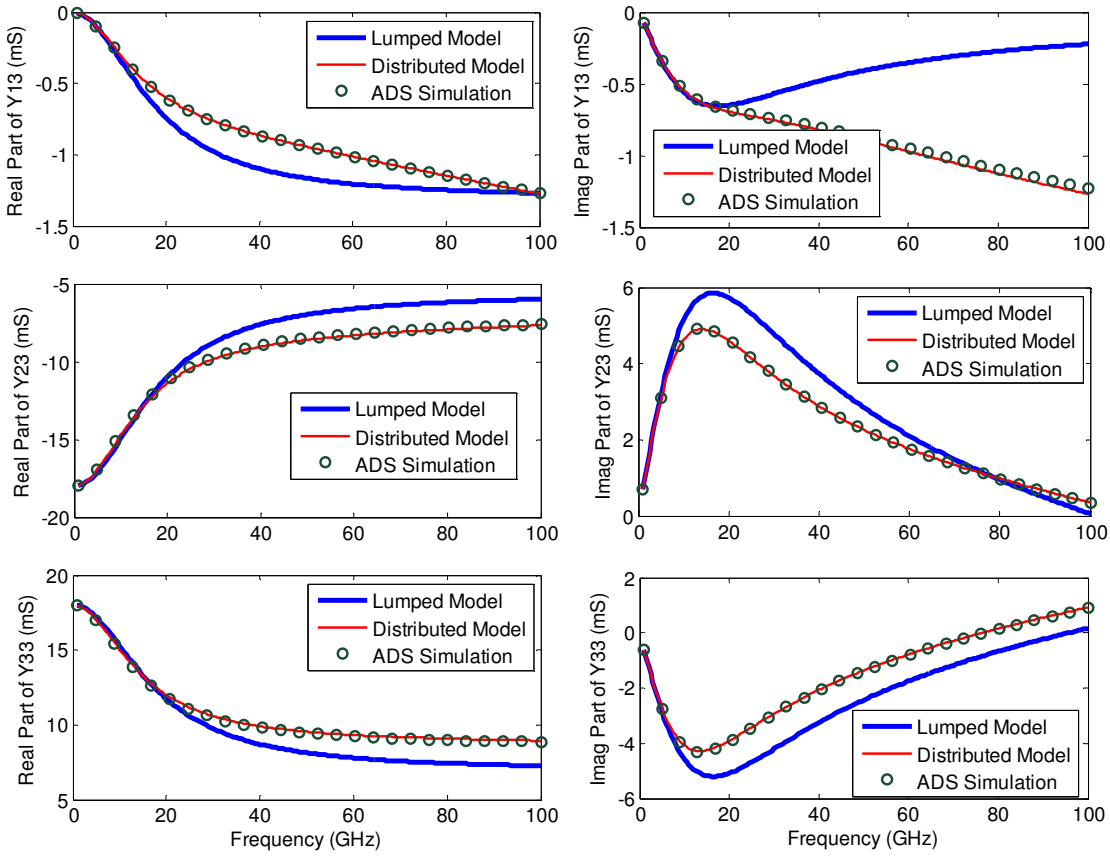


Fig. II-17. Y_{13}, Y_{23} and Y_{33} obtained from lumped model and distributed model, in comparison with the simulation in ADS for 90nm CMOS technology

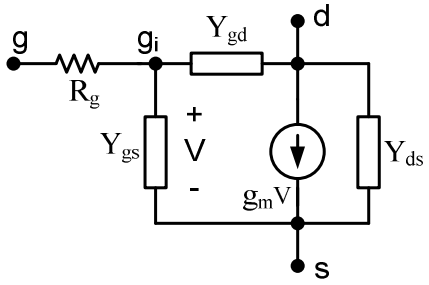


Fig. II-18. The lumped small signal model, counterpart of the distributed model in Fig. II-15

In which ρ_p is the gate poly-silicon sheet resistance, W_f and L are the gate finger width and length, respectively, N_f is the number of fingers. α is a coefficient equal to 1 for single connection gate finger and 4 for double connection. This equation has been used in many reported works and in BSIM4.3.0 model with small modifications [40], [91]. Divide by 3 in (II-74) is due the distributed effect of the gate finger resistance, in conjunction with gate capacitance, *in low frequencies*. This has been derived in Appendix C.

To compare the distributed model of Fig. II-15 with its lumped counterpart in Fig. II-18, we have defined an error measure, named Distributive Effect Error (DEE) as:

$$DEE = 100 \times \sum_{i=1}^{3} \sum_{j=1}^{3} \frac{\left| Y_{ij}^{L} ij - Y_{ij}^{D} ij \right|}{\left| Y_{ij}^{D} ij \right|} \quad \text{(II-75)}$$

Where Y_{ij}^{L} and Y_{ij}^{D} are Y-parameters of the lumped and distributed models, respectively. This measure has been calculated for some values of gate width, in our 90nm CMOS technology, and has been depicted in Fig. II-19. This figure reveals two important notes:

- The distributive effect is reduced with double connecting the gate finger. For small values of W, DEE for single connection with gate width of 2W is equal to that of double connection with gate width of W. This is very important, since the designer can choose the gate finger width for double connection case, twice of that of the single connection. These halves the gate pad length (See the next section) and hence halves the pad parasitic capacitance.
- For small widths of gate finger the distributive effect is negligible and hence the lumped model can be used. For example, in Fig. II-19-b, for W=2um DEE is less than 0.02% at 30GHz. On the other hand, practically there is an optimum value of gate finger width that minimizes the noise figure and the optimum W_f in 90nm technology is about 2um [92]. Consequently in our work distributed model *is not required*.

II.4 Layout Issues

In our knowledge even modern RF-CMOS design kits have been designed for the frequencies well below the millimeter wave frequency band. So for the MMIC's in such frequencies, the designer should have the ability to develop own design tool, based on him or her knowledge to integrate many high frequency effects together with the foundry design kit tools and data. In the case of our work the problem is more sever, since the technology we have used, and the related foundry design kit is digital process, it does not have any proposition for the high frequency effects, as well as layout of MOS transistor for RF applications. So we should design the transistor layout, as apart of our works.

The first issue in the MOS transistor layout is the gate structure. In contrast with digital circuits, in which transistors are normally designed with the minimum size, in analog circuits large W/L is required. Specially in RF applications large W/L is necessary to achieve the required trans-conductance. A transistor with large W/L can not be laid out as simple gate, due to performance reduction for long gate and some technological restrictions [40]. Consequently special layout issues must be considered. The most commonly used configuration in the design of RF IC's is the multi-finger layout [40], [92]. However other gate structure, namely Waffle structure, has been presented and discussed [91], [93]. Two types of Waffle (WF) structure, i.e. Manhattan Gate (MG) and Manhattan Interconnect (MI) have been depicted in Fig. II-20. Two different implementation of Multi-Finger (MF) gate structure have been shown in Fig. II-21. The detail of multi finger structures will be described in the next section.

- Multi-finger structure offers low gate resistance and simple design and parasitic extraction. The main problem of this structure is that increasing the number of fingers causes more parasitic effects. The parasitic effect mainly arises from coupling between the gate pad (to integrates the fingers outside the active area) and the substrate, as well as the drain-gate and (or) source-gate overpasses [93], [92]. The main advantage of WF structure is its compactness. In [93] better noise figure have been reported for this structure in below 10GHz, in comparison with MF structure. Nonetheless WF is not a known gate structure in CMOS RF design. It may be useful in analog designs in which many transistors are used. In our knowledge, the most important problem with this structure is its modeling issues

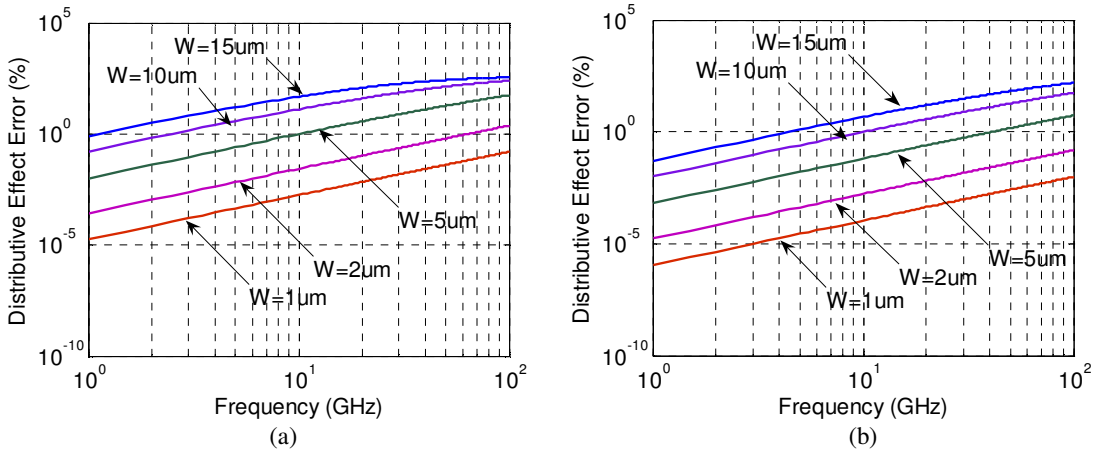


Fig. II-19. Distributive effect error measure, defined in (II-75), for various values of gate width, W(a) for single connection and (b) for double connection

and increased and complicated parasitic effects, specially in higher frequencies. Most of available MOS transistor models like BSIM3 [23] and BSIM4 [24] uses Quasi-Two-Dimensional (QTD) assumption, that is deviated in WF structure. Due to the following reasons, we have chosen the multi-finger gate structure in our layout:

- The models available on the foundry design kit is for multi-finger gate structure
- Parasitic effects modeling is very complicate in WF gate structure

Accurate parasitic effects modeling is very important in our design

II.4.1 Proposed Layout

Four different approaches for laying out the MOS transistor with multi-finger gate structure, has been depicted in Fig. II-22 to Fig. II-25. In Fig. II-22 and Fig. II-23 single connection gate has been used and Fig. II-24 and Fig. II-25 single connection gate has been implemented.

For equal finger width, the single connection strategies leads to higher gate resistance , but decreases the other parasitic effects, in comparison with the double connection gate structure. For example, in the case of single connection gate, the capacitive coupling between the gate pad and substrate is half of that of the double connection gate. Also the gate-drain parasitic capacitance in single connection gate is lower than double connection structure, in consequence of overpass of drain fingers in case of double connection. Consequently for the applications in which the gate resistance is not so important, the single connection is preferred. However the above discussion is true for equal finger number. If the designer aim to achieve a certain value of gate resistance for a given value of transistor gate width, W, then based on (II-74) finger width (W_f) of double connection structure will be 4 times of single connection structure. So we have:

$$W_f^{dc} = 4W_f^{sc} \tag{II-76}$$

Super-scribes dc and sc denote for double and single connection respectively. Also we have:

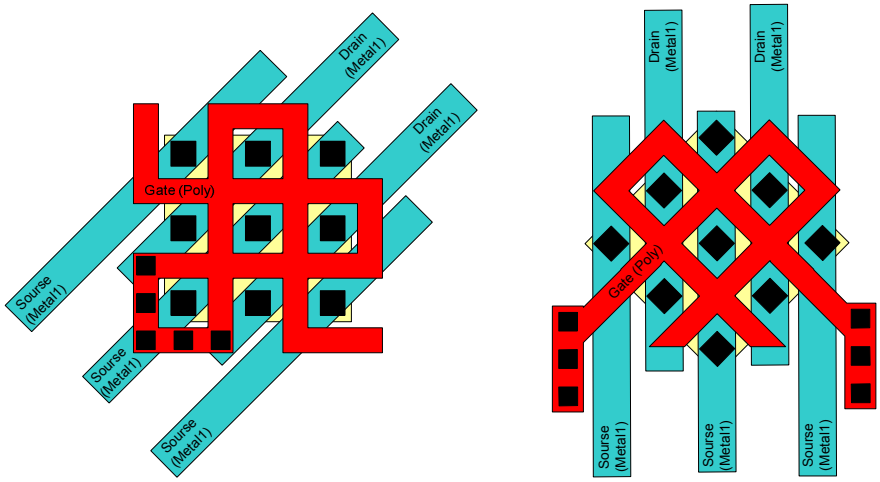
$$N_f^{sc} = 4N_f^{dc} \tag{II-77}$$

Then the length of gate pad is calculated as:

$$L_{gpad}^{sc} = L_{it} N_f^{sc}$$
$$L_{gpad}^{dc} = 2L_{it} N_f^{dc} \tag{II-78}$$

And simply we deduce:

$$L_{gpad}^{sc} = 2L_{gpad}^{dc} \tag{II-79}$$



(a) (b)

Fig. II-20. Manhattan Gate (a) and Manhattan Interconnect (b) implementation for MOS transistor layout. (Reproduced from [91])

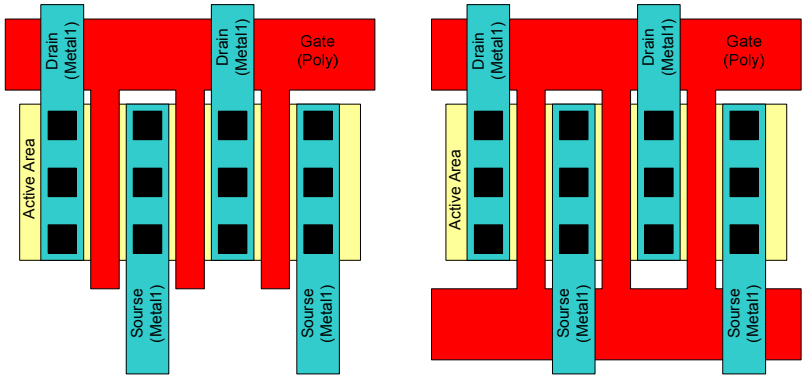


Fig. II-21. Single connection (a) and double connection (b) gate layout for MOS transistor

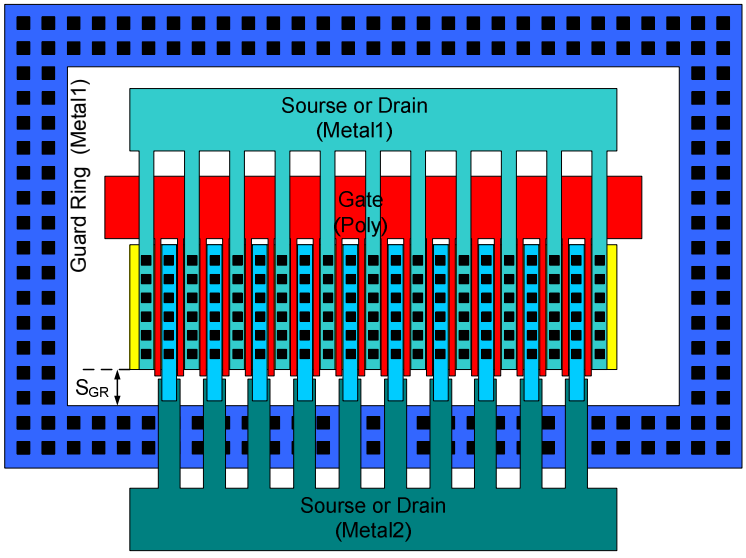


Fig. II-22. Single connection multi finger gate structure, with guard ring close to the transistor core

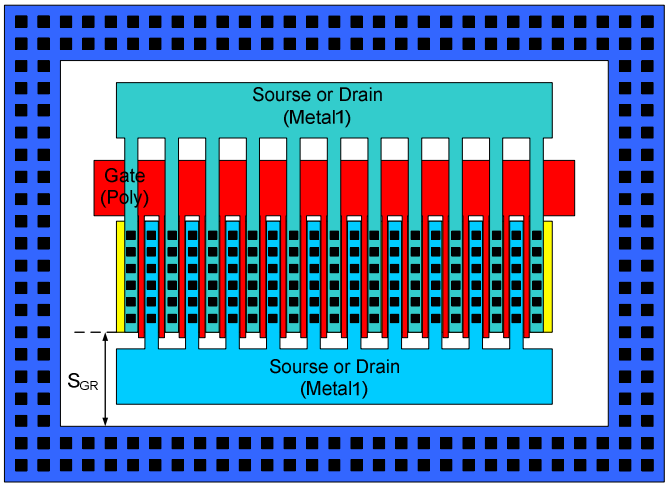


Fig. II-23. Single connection multi finger gate structure, with guard ring far from transistor core

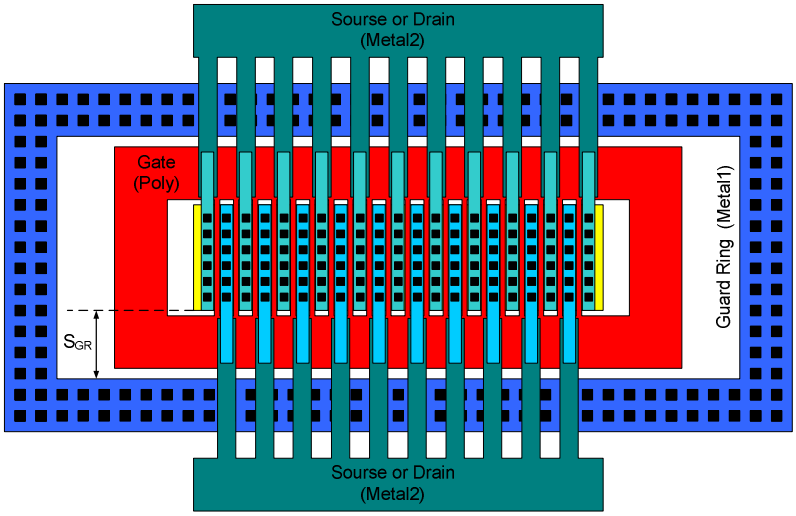


Fig. II-24. Double connection multi finger gate structure, with guard ring close to the transistor core

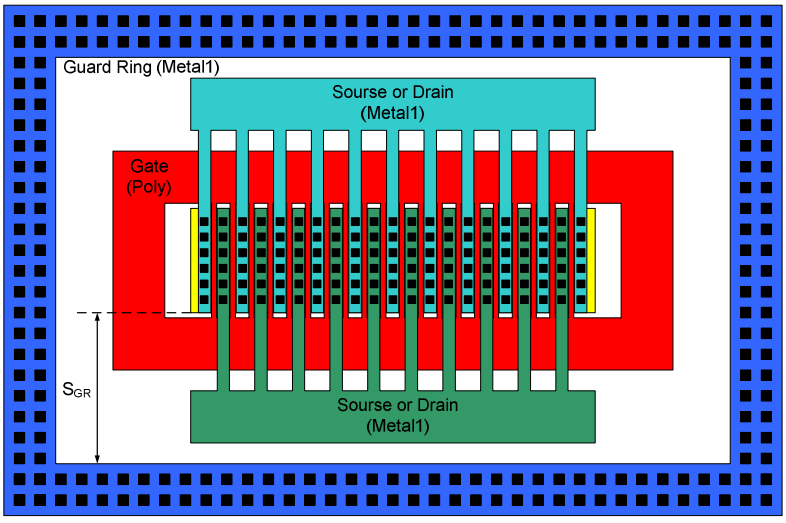


Fig. II-25. Double connection multi finger gate structure, with guard ring from transistor core

In addition, reduced number of gate fingers, reduces the drain/source overpasses and this also reduces the parasitic capacitances. The other important note is distributive effects. As we analyzed in the previous section, the distributed effects in double connection structure are significantly lower than that of single connection structure. Consequently we have chosen the double connection structure in our design.

The difference between Fig. II-24 and Fig. II-25 is in their guard ring. In Fig. II-24 the substrate resistance is less than that of Fig. II-25, but the parasitic capacitance of source pad with the guard ring is high, due to the source fingers overpass. So choosing the proper one depends on the importance of these effects. This is exactly similar in the case of Fig. II-22, in comparison with Fig. II-23. Accurate comparison of different layouts needs complicated analysis and simulation. However we found that the layout of Fig. II-25 is better than Fig. II-24 for LNA in our work.

II.5 Our Comprehensive Model

Our model basis is treatment of each gate finger as a separate transistor, and then connecting them to form the complete model of the multi finger transistor, considering all off the layout dependent parameters. The layout of the complete transistor is also broken to the layout of partial transistors. Hereafter we denote the partial transistors as ΔM. Most of the layout dependent parameters are included in the partial transistor model, and some of them are comprised in the multi finger model. Partial transistor model is derived from our I-V model, capacitance model, noise model, small signal model, as well as physical layout issues. Each partial transistor is composed of an intrinsic transistor, parasitic elements and substrate model. The intrinsic part, itself is composed of the small signal model of Fig. II-9, beside some parasitic capacitors.

To form the complete transistor, either in layout or in model, partial transistors are cascaded via resistances, capturing the gate pad resistance. Finally the interconnections model is added.

II.5.1 Partial Transistor Model

The layout of a partial transistor and related small signal and noise model has been shown in Fig. II-26. This layout is one section of the final layout of Fig. II-25. To be able to model the double-end connection effect, we divide this transistor into two similar parallel transistors and denote each half transistor with ΔM/2. Note that physically this is not possible, because drain and source pads are not symmetrical with respect to the vertival symmetry line in Fig. II-26, however this is possible as a hypothetic model.

As we noted earlier, the partial transistor model is composed of three sections: one intrinsic MOS transistor model, a set of parasitic elements related to the intrinsic transistor and a set of extrinsic layout dependent parasitic elements. The intrinsic transistor small signal model is as Fig. II-9, except for the gate resistance. Here we will analyze partial transistor to develop a small signal and noise model and derive proper equations to calculate the model elements. One important note is that the modeling is a trade between accuracy and complexity. Many complicated model can give high accuracy, but it will be inefficient in simulation. Also the extractability of model elements should be considered in developing model.

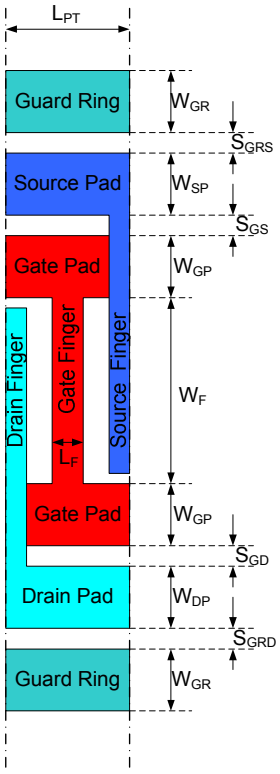


Fig. II-26. the layout of the partial transistor

II.5.1.1 Drain/source resistance

Source and drain resistances are composed of two sections: one is bias independent contact and diffusion resistance (drain/source sheet resistance) and the other is bias dependent Source/Drain Extension (SDE) resistance. In BSIM3 these resistors have been considered as a part of I-V characteristics, but in BSIM4 have been modeled as external asymmetric resistances for source and drain. Since the foundry design kit we have used is based on BSIM3 model, we does not need incorporate drain/source resistances in our model. In this case the drain/source resistance is a hidden resistance and is not seen in AC simulation [94]. However this reduces the accuracy, since some of the parasitic capacitive couplings to the internal drain/source node does not see this resistance and some others see it.

Drain and source resistances have been depicted in Fig. II-27. As in this figure, the drain/source resistance is composed of contact resistance, salicide resistance, and SDE resistance. The contact resistance is dominated by the salicide-SDE contact. In [40] simple equation have been proposed for these resistances.

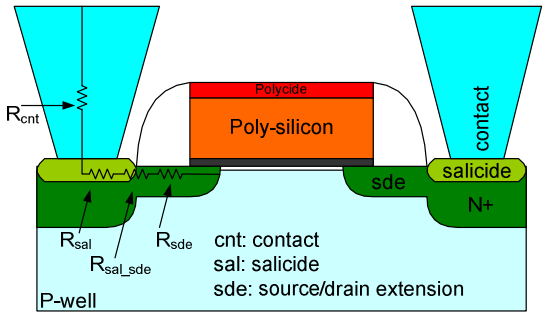


Fig. II-27. source/drain resistance representation for a short channel MOS device [40]

II.5.1.2 Parasitic capacitances

Parasitic capacitances are divided into two main categories: parasitic capacitors in intrinsic part and parasitic capacitors in extrinsic section. In the intrinsic part, parasitic capacitors are among the gate, source and drain fingers. In the extrinsic section parasitic capacitors are between gate pad and source/drain pad, as well as guard ring.

Parasitic capacitances in the intrinsic part, as depicted in Fig. II-28 [51], are three types: One is the capacitance between the top of gate finger and the upper section of sidewall of source/drain finger and related contacts (C_{top} in Fig. II-28). The other is the capacitance between the gate finger sidewall and lower section of sidewall of source/drain finger (C_{side} in Fig. II-28). The third capacitor is due to the field fringing from gate sidewall to the source/drain surface (C_f in Fig. II-28).

Conformal mapping is a powerful method, conventionally used for calculation of capacitances in coplanar and parallel plate and strips, assuming quasi static condition [95]. Basis of this method is transformation of a complicated curve, representing the cross section of a physical structure, into a simple shape in other plane, so that the new shape can be simply analyzed to calculate the capacitance. This method has been used in calculation of gate fringing capacitance and interconnection models in integrated circuits, with different transforming function [51], [96], [97]. Base on conformal mapping from elliptical coordinate system to a linear coordinate system, in [51] a closed form equation has been derived to calculate the gate fringing capacitance:

$$C_f = \frac{\beta_1 W K_{sp} \varepsilon_0}{\pi}\left(M^2-1\right)\left(\frac{M^2}{M^2-1}\right)^{M^2} \tag{II-80}$$

In which β_1 is a fitting parameter, W is the gate width, ε_0 is the free space permittivity and K_{sp} is the relative permittivity of the material between gate and source/drain. M is defined as:

$$M = \frac{L_{sp}}{t_{ox}} \tag{II-81}$$

t_{ox} is the oxide thickness and L_{sp} has been shown in Fig. II-28. However the gate fringing capacitance is comprised in BSIM3v3 and hence we does not need to incorporate it separately in our model. In BSIM3v3 this capacitance is modeled as [23]:

$$C_f = \frac{2\varepsilon_{ox}}{\pi}\ln\left(1+\frac{t_{poly}}{t_{ox}}\right) \tag{II-82}$$

C_{top} in Fig. II-28 has been calculated in [51] as:

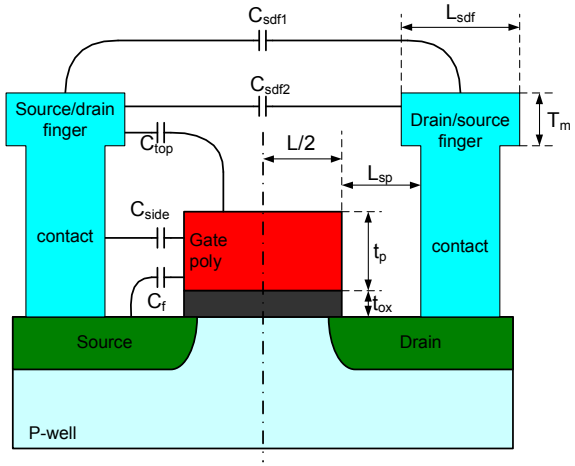


Fig. II-28. Parasitic capacitances in intrinsic part of the partial transistor [51]

$$C_{top} = \frac{2\beta_2 W_{eff} K_{top} \varepsilon_0}{\pi} \ln\left(1 + \frac{L}{2L_{sp}}\right) \quad \text{(II-83)}$$

Where β_2 is a fitting parameter, W_{eff} is the effective length of the source/drain finger, considering the space between contacts, and K_{top} is the relative permittivity of the dielectric material on top of the gate finger. C_{side} in Fig. II-28 is simply calculated as:

$$C_{side} = \beta_3 W_{eff} K_{sp} \varepsilon_0 \left(\frac{t_{ox} - t_p}{L_{sp}}\right) \quad \text{(II-84)}$$

where β_3 is a fitting parameter and t_p is the poly thickness. The capacitance C_{sdf1} in Fig. II-28 is calculated using the analysis in [96]:

$$C_{sdf1} = \beta_2 \frac{K_{top} W \varepsilon_0}{\pi} \ln\left(1 + \frac{L_{sdf}}{S_{sdf}}\right) \quad \text{(II-85)}$$

K_{top} is the relative permittivity of the dielectric material on top of the source/drain finger, β_2 is as in (II-83) and L_{sdf} and S_{sdf} have been shown in Fig. II-28. Finally the capacitance C_{sdf2} in Fig. II-28 is calculated as:

$$C_{sdf2} = \beta_3 W K_{top} \varepsilon_0 \left(\frac{T_m}{S_{sdf}}\right) \quad \text{(II-86)}$$

Extrinsic parasitic capacitances have been demonstrated in Fig. II-29, that is vertical cross section of the partial transistor structure in Fig. II-26. These capacitances are due to the coupling between gate pad, source/drain pad and guard ring. We will use the closed form equation presented in [96] , after small modification, to calculate the capacitances. Note that all of the calculated capacitances are per-unit-length values.

The capacitance between top of the source/drain pad and top of the guard ring (C_{rsd1} in Fig. II-29) is calculated as:

$$C_{rsd1} = \gamma_1 \frac{K_1 \varepsilon_0}{\pi} \ln\left(1 + \frac{W_{av}}{S_{prsd}}\right) \quad \text{(II-87)}$$

γ_1 is a fitting parameter, K_1 is the dielectric constant of the dielectric above the pads, S_{prsd} is the space between the guard ring and source/drain pad. W_{av} is the average width of the guard ring and source/drain pad. The capacitance between top of the source/drain and gate pads (C_{gsd1} in Fig. II-29) is calculated as series of two capacitors, C'_{gds1} and C''_{gds1} that are calculated as:

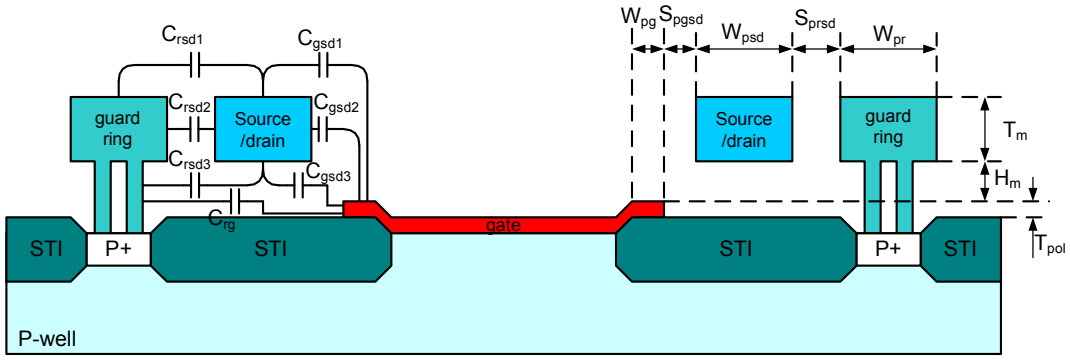


Fig. II-29. Parasitic capacitances between gate, sorce/drain and guard ring pads (extrinsic part of the partial transistor)

$$C'_{rsd1} = \gamma_1 \frac{K_{eq}\varepsilon_0}{\pi} \ln\left(1 + \frac{W_{av}}{S_{pgsd}}\right)$$
$$C''_{rsd1} = K_{eq}\varepsilon_0 \frac{W_{pg}}{T_m + H_m} \quad \text{(II-88)}$$

Where W_{av} is the average width of the source/drain and gate pads, γ_1 is as previous equation, K_{eq} is the effective dielectric constant of the dielectric material on top of gate pad. W_{pg}, T_m and H_m have been shown in Fig. II-29. The capacitance between the sidewall of source/drain pad and the top of gate pad (C_{gsd2} in Fig. II-29) is calculated from [51] with small modification:

$$C_{gsd2} = \frac{2\beta_2 K_{eq}\varepsilon_0}{\pi} \ln\left(1 + \frac{W_{pg} + T_m}{2S_{pgsd}}\right) \quad \text{(II-89)}$$

β_2 is the same as (II-83),K_{eq} is the same as (II-88), W_{pg}, T_m and S_{pgsd} have been shown in Fig. II-29.

C_{gsd3} in Fig. II-29 is calculated using (II-89), replacing K_{eq}, W_{pg} and T_m with K_3, W_{psd} and T_{poly} , respectively. K_3 is the dielectric constant of the dielectric material above gate and under source/drain pads. W_{psd} and T_{poly} have been shown in Fig. II-29. C_{rsd3} in Fig. II-29 is calculated using (II-89), replacing K_{eq}, W_{pg}, T_m and S_{pgsd} with K_3, W_{psd}, H_m+T_{poly} and S_{prsd}, respectively. K_3 is the dielectric constant of the dielectric material above gate and under source/drain pads. W_{psd} and T_{poly} , H_m and S_{prsd} have been shown in Fig. II-29. C_{rg} in Fig. II-29 is very small and we neglect it and finally C_{rsd2} is calculated simply:

$$C_{rsd2} = K_2\varepsilon_0 \frac{T_m}{S_{prsd}} \quad \text{(II-90)}$$

Considering all of the calculated capacitances, we have the equivalent circuit of Fig. II-30 for the parasitic capacitances. In this figure g_i, d_i and s_i are gate, drain and source nodes of intrinsic transistor, respectively. C_{xy_pe} and C_{xy_pi} denote the total parasitic capacitance between nodes x and y (x and y stands for gate, source, drain and guard ring), in the extrinsic and intrinsic parts, respectively. The capacitors in this model are calculated based on our previous calculations, as follows:

$$C_{gs\_pe} = C_{gsd1} + C_{gsd2} + C_{gsd3}$$
$$C_{gd\_pe} = C_{gs\_pe} \quad \text{(II-91)}$$

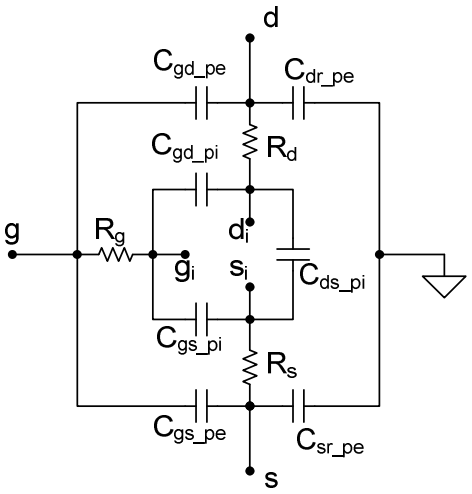


Fig. II-30. Equivalent circuit model for parasitic capacitances of the partial transistor

$$
\begin{aligned}
C_{gs\_pi} &= C_{top} + C_{side} + C_f \\
C_{gd\_pi} &= C_{gs\_pi} \\
C_{rs\_pe} &= C_{rsd1} + C_{rsd2} + C_{rsd3} \\
C_{rd\_pe} &= C_{rs\_pe} \\
C_{ds\_pi} &= C_{sdf1} + C_{sdf2}
\end{aligned}
\qquad \text{(II-92)}
$$

II.5.1.3 Substrate model

Accurate substrate model is necessary for RF applications. Many studies have been aimed in substrate modeling for MOS transistor in RF frequencies and in consequence some models have been proposed. The most commonly used substrate model is three-resistor network, as in Fig. II-31 [98], [99], [94], [40]. This model has been used in BSIM3-RF model and proved to work well up to 20GHz [98]. Simple single resistor substrate modeling has been investigated in [99] presented measurement results show that it is sufficient up to 10GHz. However these measurements are for devices with very large number of fingers and this model is not suitable for the devices with small number of fingers and specially for the frequencies more than 10GHz [94]. In [40] intra-device substrate coupling has been considered and final model has been presented as three-resistor network. BSIM4 uses more complicated substrate network with introducing a 5-resistor substrate network for total device, not for each finger, as shown in Fig. II-31.

As we mentioned, available substrate models have proven to work up to 20GHz. However for MMW applications there is need for more accurate substrate odeling. 3e41-60.1604(h)-2.6738(e)-5.1961

3.91138( )-60.1138( )-w

$$\sigma_{uaw} = \frac{1}{\rho_{uaw} T_{STI}}$$
$$\sigma_{usw} = \frac{1}{\rho_{usw} T_{STI}} \quad \text{(II-94)}$$

ρ_{uaw} and ρ_{usw} are sheet resistance of the under active and under STI p-well, respectively. Lateral resistances in Fig. II-32 are calculated as:

$$R_{b1} = \rho_{uaw} \frac{W_f}{2L_{PT}}$$
$$R_{b2} = \rho_{usw} \frac{W_{GP} + S_{GS} + W_{SP}}{L_{PT}} \quad \text{(II-95)}$$
$$R_{b2} = \rho_{uaw} \frac{S_{GRS} + W_{GR}/2}{L_{PT}}$$

The capacitances in Fig. II-32 are calculated as:

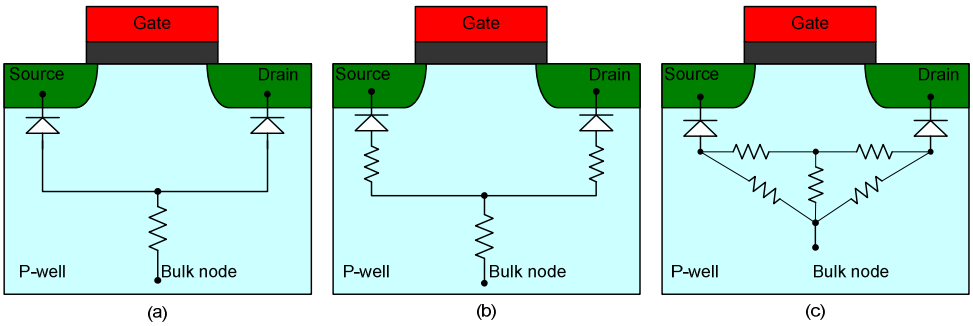


Fig. II-31. Various substrate modeling techniques: single resistor [99] (a), three-resistor [40] (b) and five-resistor [24] (c)

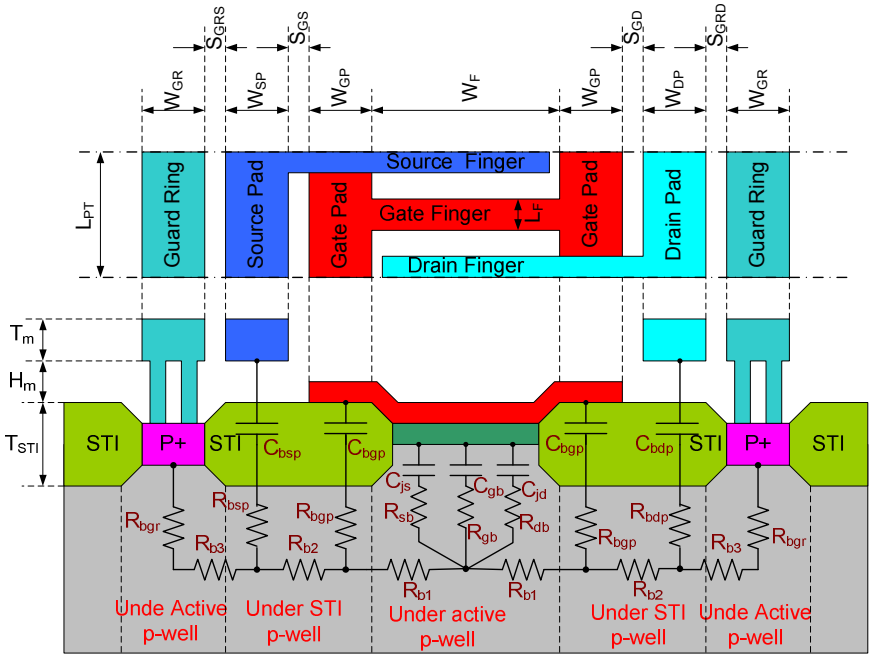


Fig. II-32. Substrate electrical model for the partial transistor in Fig. II-26

$$
\begin{aligned}
C_{bgp} &= K_{STI}\varepsilon_0 \frac{W_{GP}L_{PT}}{T_{STI}} \\
C_{bsp} &= C_{bdp} = \frac{C_1 C_2}{C_1 + C_2} \\
C_1 &= K_d \varepsilon_0 \frac{W_{SP}L_{PT}}{H_m} \\
C_2 &= K_{STI}\varepsilon_0 \frac{W_{SP}L_{PT}}{T_{STI}}
\end{aligned}
\qquad \text{(II-95)}
$$

In which K_{STI} and K_d are the dielectric constants of STI layer and the dielectric above STI, respectively. ε_0 is the free space permittivity.

The substrate model in Fig. II-32 can be represented as a RC network, as shown in Fig. II-33. This circuit is very complicated to be analyzed and increases four extra nodes to the transistor small signal model in Fig. II-18. Consequently it is not suitable for our simple design tool. To simply the circuit, meanwhile preserving the accuracy, we have assumed that extrinsic gate, source and drain nodes, (*b*, *g* and *d* in Fig. II-33), have approximately equal voltage with the intrinsic ones (b_i, g_i and d_i in Fig. II-33). Using this approximation we obtain the equivalent substrate Y model, as in Fig. II-34. As this figure shows with the simplified model, there is not any extra node in the transistor model circuit, in comparison with Fig. II-18.

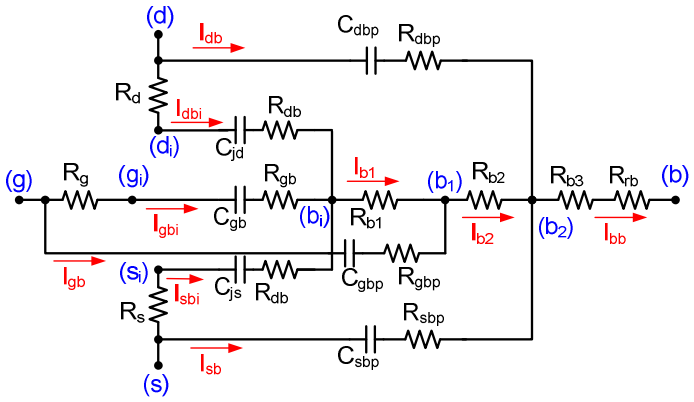


Fig. II-33. Proposed substrate network as a RC circuit, derived from Fig. II-32.

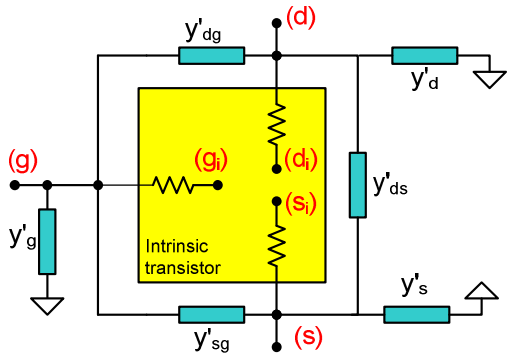


Fig. II-34. Simplified Y-parameter model for substrate model circuit of Fig. II-33

The Y parameters for this figure is calculated as follows. For detail see Appendix D.

$$
\begin{aligned}
y'_d = y'_s &= y_{dbp} + y_{dbi} + \frac{y_{dbp} g_{b2}}{y_{b2}} \frac{\left(\lambda_g g_{b1} y_{b2} + \lambda_{bi} y_{gbp} y_{b2}\right)}{\lambda_{bi}\left(y_{b1} y_{b2} - g_{b2} g_{b2}\right)} + y_{dbi} \frac{\lambda_g}{\lambda_{bi}} \\
y'_g &= y_{gbp} + y_{gbi} + \frac{\left(\lambda_g g_{b1} y_{b2} + \lambda_{bi} y_{gbp} y_{b2}\right)}{\lambda_{bi}\left(y_{b1} y_{b2} - g_{b2} g_{b2}\right)}\left(-y_{gbp} + 2\frac{y_{dbp} g_{b2}}{y_{b2}}\right) + \left(2y_{dbi} - y_{gbi}\right)\frac{\lambda_g}{\lambda_{bi}} \\
y'_{ds} &= -\frac{y_{dbp} g_{b2}}{y_{b2}} \frac{\left(\lambda_s g_{b1} y_{b2} + \lambda_{bi} g_{b2} y_{sbp}\right)}{\lambda_{bi}\left(y_{b1} y_{b2} - g_{b2} g_{b2}\right)} - \frac{y_{dbp} y_{sbp}}{y_{b2}} - y_{dbi} \frac{\lambda_s}{\lambda_{bi}} \\
y'_{dg} = y'_{sg} &= -\frac{y_{dbp} g_{b2}}{y_{b2}} \frac{\left(\lambda_g g_{b1} y_{b2} + \lambda_{bi} y_{gbp} y_{b2}\right)}{\lambda_{bi}\left(y_{b1} y_{b2} - g_{b2} g_{b2}\right)} - y_{dbi} \frac{\lambda_g}{\lambda_{bi}}
\end{aligned}
\tag{II-96}
$$

In which:

$$
\begin{aligned}
\lambda_{bi} &= y_{b1} y_{b2} y_{bi} - g_{b2} g_{b2} y_{bi} - g_{b1} y_{b2} g_{b1} \\
\lambda_g &= g_{b1} y_{b2} y_{gbp} + y_{b1} y_{b2} y_{gbi} - g_{b2} g_{b2} y_{gbi} \\
\lambda_d &= g_{b1} g_{b2} y_{dbp} + y_{b1} y_{b2} y_{dbi} - g_{b2} g_{b2} y_{dbi} \\
\lambda_s &= g_{b1} g_{b2} y_{sbp} + y_{b1} y_{b2} y_{sbi} - g_{b2} g_{b2} y_{sbi}
\end{aligned}
\tag{II-97}
$$

And:

$$
g_{xy} = \frac{1}{R_{xy}} \tag{II-98}
$$

II.5.1.4 Final model for partial transistor

Final model of the partial transistor in Fig 2-35, is obtained combining parasitic capacitances and substrate network with the intrinsic transistor model of Fig. II-9. In addition, noise model of the intrinsic part, as discussed in section II.2.4, is added and the equivalent noise of substrate is considered. Substrate noise is considered as resistive thermal noise [72], due to the real part of each equivalent Y parameter in Fig. II-34. Final model has been shown in Fig. II-35. Note that this model has only four nodes, as the simple model of Fig. II-9. This simplifies all of the analysis and calculations, without need for time-consuming matrix inversions.

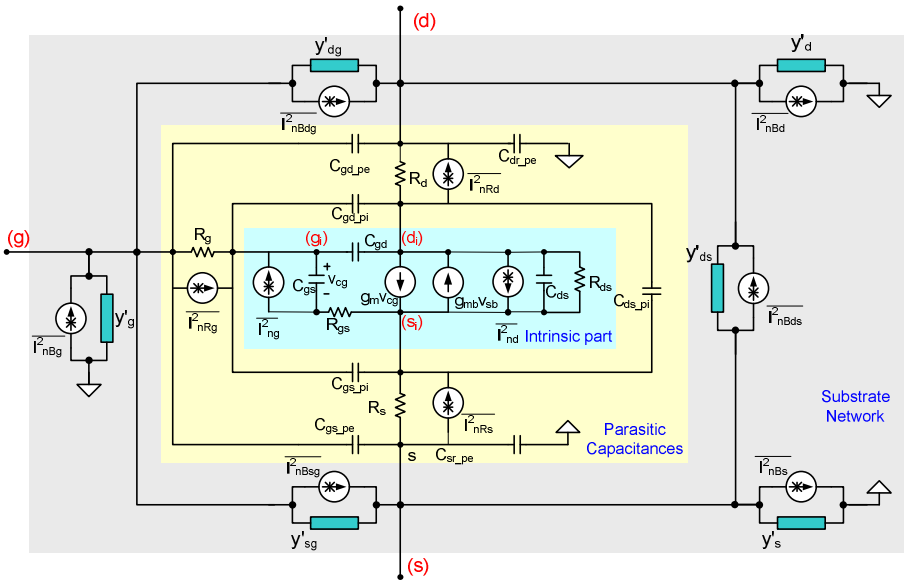


Fig. II-35. Final partial transistor model, composed of intrinsic part, parasitic capacitances, substrate network and noise model

II.5.2 Complete Transistor Model

In section II.3.2 we deduced that the distributed model is not necessary for the single-finger partial transistor model. However distributed nature affect the total transistor (composed of some partial transistors), for which the layout has been shown in Fig. II-25. To capture the distributed effects in our complete transistor model, we have used the model in Fig. II-36, that is cascade of partial transistors via small resistances, showing the poly-silicon gate pad resistance. As we noted earlier in the case of double connection gate fingers, each partial transistor (ΔM) with gate width W_{PT}, is assumed as a parallel of two transistors, (ΔM/2) with gate width $W_{PT}/2$. Considering the symmetry of the layout of Fig. II-25 and related model in Fig. II-36, we can use the circuit in Fig. II-37 to analyze our model. Then Y-parameters of the transistor will be 4-times of that of Fig. II-37. Note that in the case of odd number of fingers, the width of the last partial transistor in Fig. II-37 will be half of the others. The analysis of this circuit leads to a simple difference equation:

$$\begin{cases} I_{n+1} = I_n + V_n \Delta Y_{in} \\ V_{n+1} = V_n - I_{n+1} \Delta R \end{cases} \qquad \text{(II-99)}$$

The required initial condition is:

$$V_0 = V_g$$

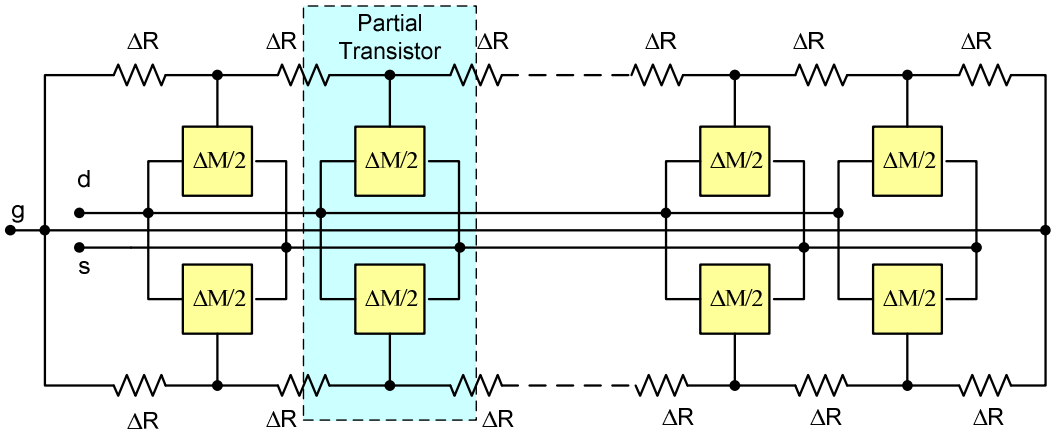


Fig. II-36. Distributed model of the transistor, corresponding to the layout of Fig. II-25

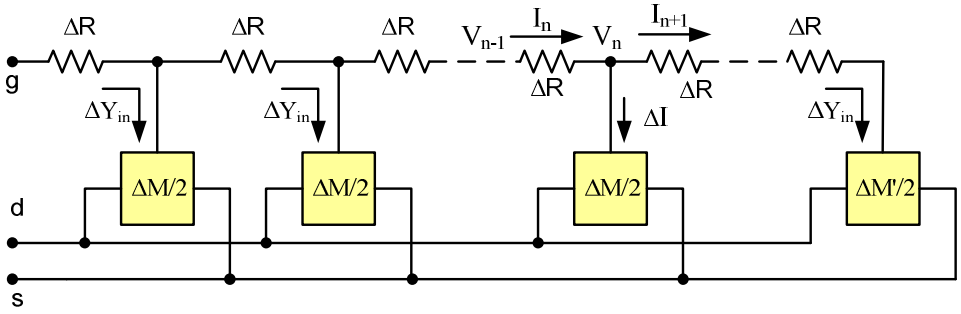
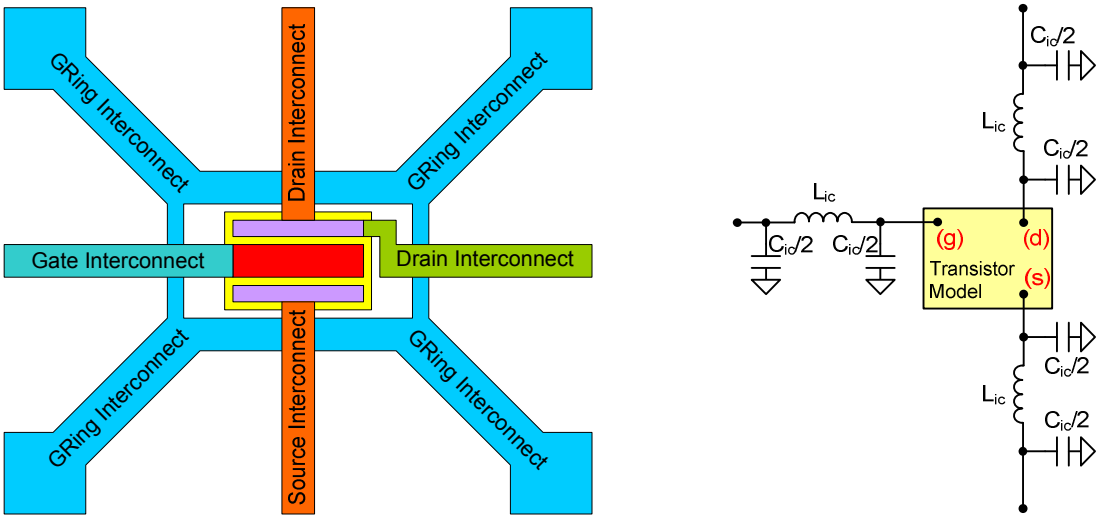


Fig. II-37. Distributed model of the transistor, used in analysis of the Fig. II-36

II.5.2.1 Interconnect model

Since all of the interconnects in our design are implemented as Coplanar Transmission Line (CPTL), we have designed special connections to the transistor pads to best match the CPTL to the transistor inputs. The simplified layout has been shown in Fig. II-38-a. This structure adds some extra parasitic effects to the transistor final model in Fig. II-36. We have used an LC circuit to model these effects. The equivalent circuit for transistor interconnects has been shown in Fig. II-38-b. More details will be given in chapter IV.



(a) (b)

Fig. II-38. Interconnects to the transistor pads (a) and related equivalent LC model as a π section (b)

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