Chapter VI
Conclusion and Suggestions

In this chapter a brief review of the results of the thesis is presented and some propositions are presented for future works.

VI.1 Conclusion

This work is an attempt toward low-power mm-wave transceiver design for low cost, short range, low data rate and dense WSN application. Because of its low-cost and proved ability in mm-wave band, STMicroelectronics 90nm CMOS technology was chosen in our work. In addition, global purpose (GP) CMOS technology was chosen instead of RF CMOS, to achieve lower cost. This technology is the same as bulk CMOS technology, unless it provides MIM capacitors and some types of MOS transistors with high gate breakdown voltage. Obviously the foundry design for the used GP CMOS technology does not contains library models for RF devices and hence we started our work with developing an individual simple design tool for our work. For this purpose we should develop simple and accurate models for both of active devices and passive elements. Again we emphasis that this thesis was the first attempt in design of mm-wave front end in 90nm CMOS technology, in the laboratory and hence our work could not be based on the available experiences. We encountered many difficulties and problems and to overcome them, we used to main way: Study of the reported works, and analytic solutions verified by the foundry design kit.

VI.1.1 Device-Level Modeling

It must be noted that in RF and specially in mm-wave design, the uncertainty of design is mostly originated from parasitic effects and hence the accuracy of I-V model of active devices is not so crucial as in the case of a VLSI design. For example, in VLSI chip with 100,000 transistors, 1uA error in the current of each MOS transistor produces total current error of 100mA!! However in the case of an RF circuit with 100 transistors and 30mA supply current, this causes only 100uA current error that is only 1/300 of the total current and can be easily neglected. Regarding the above discussion, we developed our simple single-equation model for MOS transistor. The term single-equation implies that one I-V equation is used for all regions of operation of MOS transistor. In this way we studied various types of the available models and various short channel effects, specially the ones that become more significant in higher frequencies.

To complete our model, we developed a simple charge model. The capacitance and trans-capacitances was obtained by differentiating the nodal charges with respect to the nodes voltage. This approach well captures the non-symmetric nature of the nodes capacitance, the behaviour that does not considered in most simple small signal models. For example, C_{gs} that is equal to the charge variation of the gate node due to the source voltage variation, is not equal to C_{sg}, that is the charge variation of the source node due to the gate voltage variation. The small signal model was obtained from I-V model and with differentiating the drain current with respect to nodes voltage. Analysis of non-quasi static (NQS) effects showed that this effects becomes noticeable in higher frequencies. Specially, in the case of 90nm CMOS technology, these effects are important in mm-wave band. So we introduced NQS effects in our model. We studied different noise models and the measurement results reported in the literature, specially the ones in the case of 90nm CMOS technology. We found simple noise model of Van Der Ziel is of enough accuracy, even in modern CMOS technologies and hence

we used it in our MOS model. Measurement results of the fabricated LNA showed that this noise model can describe the noise behaviour of the transistors with good accuracy.

We adopted complete analysis of distributed effects in the case of a short channel MOS transistor. Two main types of distributed effects are encountered in MOS transistors. One is the distributed effect due to gate capacitance that affects the gate resistance. Due to this effect, the gate resistance is only 1/3 of the gate contact ohmic resistance. It is interesting that this distributed effect is truth even in low frequencies and in higher frequency the coefficient 1/3 changes slightly. The other distributed effect is related to the distribution of the transistor layout on the chip area and occurs only in very high frequencies. The distributed nature of deep sub-micron MOS transistors has been considered in the some literature. However there is not any implicate suggestion to explain the frequency limit, up to which the distributed effects can be neglected. To obtain an analytic view about the distributed nature of the transistor, we developed a distributed model for MOS transistor. Such models were reported in some literatures, but our analysis is more complete an accurate. Based on this analysis we deduced that the distributed effects can be lowered into a negligible value, by using proper width for gate fingers. We showed that the required finger width is not smaller that the finger width corresponding to the optimum noise performance, reported in the literatures based on the measurement results. Consequently the distributed effects are negligible in the case of MOS transistor core with properly designed layout. However the distributed effect should be considered in the case of the pads that connect the fingers together. To capture this kind of distributed effect, we proposed the partial-transistor concept. Each MOS transistor layout is considered as a set of some small single-finger transistors, named partial transistors. The distributed effects are not considered in partial-transistor level, but are modelled in the case of complete transistor, i.e. the set of partial transistors.

CMOS technologies have low-resistivity substrate that becomes an important bottleneck in mm-wave frequencies. In these frequencies the substrate admittance, specially at the high impedance nodes, greatly displaces the nodal impedances and degrades the circuit's gain and noise performance. In addition, electric and magnetic couplings to the substrate cause noticeable losses that degrade the circuit performance. Consequently, accurate modeling of the substrate is an essential issue in CMOS mm-wave design. Due to low resistivity of the substrate in bulk CMOS technologies, the capacitive effect inside the substrate is negligible and hence the substrate can be modelled with a pure resistive network, connected to the transistor via different capacitance. Based on the reported works, conventional 3-resistor substrate model has good accuracy up to 20GHz. However for mm-wave band more accurate model is necessary. The substrate model is a layout-dependent network. We have developed an accurate substrate network, by investigating the front end process of the used technology. The substrate model parameters can be simply calculated using the DRM data, provided as a part of foundry design kit.

Transistors layout is of great importance in sense of parasitic effects. In mm-wave designs, weak layout can completely degrade the circuit performance. On the hand, to be able to accurately predict the circuit's performance in post-layout simulation, accurate model of layout-dependent effects is necessary. We found that multi-finger layout with 2um-fingers and gate finger with double-end connection is good strategy in mm-wave range, in 90nm CMOS technology. Beside the substrate model network, parasitic capacitive couplings between metal parts of the transistor structure are other layout dependent effects. Finally, the inductive parasitic effects may appear in the interconnections from transmission lines to the transistor nodes. We have modelled all of these effects by proper lumped element models, to be incorporated in post-layout simulation. The model elements have been calculated using analytic equations or extracted by full wave electromagnetic simulation in HFSS. Proper analytic equations, mainly obtained from Conformal Mapping technique, have been used in

calculation of layout-dependent capacitive effects. The 3-dimensional model of the transistor structure has been rendered to the full wave simulator, using our individual interface, developed in VBasic script format.

VI.1.2 Passive Elements Design and Modeling

Passive elements are very important parts of a mm-wave circuit. In mm-wave band, the stray capacitances at the high impedance nodes produce time constants that can easily filter the desired signal out. To overcome this problem, the conventional and the most effective technique is tuning out the capacitances using proper inductors. By this way, not only the stray capacitances are absorbed, but also tuned LC circuits are obtained and hence higher and more selective gain is achieved in the amplifiers. Beside inductors, capacitors and transmission lines are very important passive elements that must be accurately designed and modeled. Transferring signal between different points of the circuit layout needs a proper signal path. In mm-wave band these paths should be designed as transmission lines. We have used MIM capacitors in our design and hence we have not any challenge in term of capacitances.

We have investigated various inductor structures to find a proper structure for the inductors in our design. We found meandered line inductors less area efficient. Although spiral inductors offer good performance even in mm-wave band, their modeling and design is very complicated and hence they were not suitable for our work. Finally we have introduced line-type inductors with patterned shield in 2006. Although line-type inductors have been reported prior to our work, they use different structures that are not suitable for bulk CMOS technology. In the case of SOI CMOS technology, this type of inductors has been used without shield layer, as conventional coplanar structure. In the case of bulk CMOS technology, the line type inductors have been implemented as micro-strip structure, for which a complete metal layer is inserted beneath the inductor structure. Coplanar structure is not useful in bulk CMOS technologies. The reason is that to achieve high inductance, the line impedance should be high and high impedance line has high coupling to the substrate that lowers the quality factor in CMOS technology. On the other hand, microstrip structure is inherently low-impedance and hence very long line length is required for a given inductance. The structure we have proposed uses a patterned shield beneath the inductor. This shield layer prevents the electric field to penetrate into the substrate, but does not affect the magnetic field. This phenomenon simply leads to high inductance with low substrate loss.

To accurately design the line-type inductors, transmission lines and T-junctions we have developed a lumped element RLGC model. The model elements have been calculated in consequence of analyzing the physical origin of the different model elements, and proper analytic equations have been adopted or developed to calculate them. The model makes possible to calculate the optimum dimensions for the inductor's structure, in very short time. In addition, the lumped model can be easily incorporated in post layout simulation. In attempt to verify our model with electromagnetic simulators, we examined the most popular electromagnetic simulators, i.e. ADS and HFSS. We tried with different facilities of ADS and finally we switched to HFSS full wave simulation.

VI.1.3 LNA Design and Measurement Results

In the way toward a complete RF front end, we started with the LNA, regarding its importance in the receiver and the different problems of it's deign in mm-wave band, in CMOS technology. We studied various LNA circuits and their characteristics to find the best proper one for our purpose. Among various choices, we selected the cascode topology. The reason was that to achieve an ultra low-power LNA we should design our LNA in single stage topology and cascode topology was the only one that can ensure enough reverse isolation in

mm-wave single stage LNA. After choosing the LNA topology, we started to develop a reliable design and optimization approach. The available foundry design kit was not for RF design and hence we were obliged to develop our individual design tool. Then we started to develop the framework for a complete LNA analysis and design tool. This design tool was a collection of our models developed for active devices and passive elements, in addition with different analysis and optimization programs, written in MATLAB. We used Power Constrained Simultaneous Noise and Input Matching (PCSNIM) technique to optimize the LNA. In this optimization methodology, the noise figure of LNA is minimized, constrained to the given power consumption and meanwhile, preserving the conjugate matching in the input and out put of LNA. This technique is very efficient in CMOS technology and specially in low-power LNA design. Our optimization is performed in a two-step process: first, the LNA is designed using analytic equations we have derived. In the second step, numerical optimization is used to optimize the design and in the same time analytic approaches are used to simplify the numerical optimization and make it more reliable.

Using our design tool, we designed the first version of the LNA and it was sent to be fabricated by STMicroelectronics in June 2006. Since we designed the layout of all components individually and the design kit library components were not usable in our work (except for basic elements, such as resistors and capacitors) we could not use the layout control facility of the design kit. Unfortunately, due to this limitation and the time limitations, a mistake had occurred in the layout of input matching network of the LNA. Due to this mistake, measurement results showed some discrepancy with the simulation results, in some characteristics. However, when we introduced the same mistake in our post-layout simulation of our design tool, we obtained the results in very good agreement with the measurement results and this proved the accuracy of our models and design tool. Measurement results showed that in spite of the mistake, our LNA has acceptable performance, regarding its only 3-mW power consumption. The fabricated LNA has 10dB gain with only 3mW power consumption. After the first LNA, we completed our design tool and could achieve LNA with better performance. We complete the layout of the final LNA and post-layout simulations in the foundry design kit and in our design tool showed its excellent performance: 14.56dB power gain and 3.6dB noise figure with only 3mW power consumption. Unfortunately, until now this design has not sent for fabrication.

The performance of the fabricated LNA and the final design has been compared with the reported works in Table IV-4 of Chapter IV. The conventionally used figure-of-merit (FOM) defined in (IV-101) has been used for compare different LNAs. Due to leak of reported characteristics, FOM can not be calculated for some of listed cases. This table shows that the chip are of our LNA is a record, thanks to the line-type inductors we have developed and used in our design. The chip area for all of the cases is the area of LNA core, excluding the input-output pads area. Regarding Table IV-4, the reported multi-stage LNAs have higher FOM, in comparison with single-stage LNAs. This can be intuitively explained by noting that for cascaded, identical gain stages, the total gain increases exponentially with the number of stages whereas power consumption increases linearly. In contrast, in the FOM defined in (IV-101), both of the gain and power are in linear scale. So, conventional FOM of (IV-101) is valid only for the LNAs with equal number of stages. It must be noted that two (or more) stage LNAs can not be used in ultra-low power applications, due to their inherently high power consumptions.

As a consequence of the above suggestion, we have re-tabulated the recently reported single stage LNAs in Table IV-5 of Chapter IV. Among the compared LNAs, the FOM is calculated only for the LNA of Y. Su et *al.*, due to leak of IIP3 characteristics for the others. Comparison of our fabricated LNA with that of Su et *al.*, shows that our work is acceptable, as our first experience. Note that this is despite of the mistake of placement in layout of our

LNA, as explained previously. Our post layout simulation (last column of the table) shows that if the mistake did not occur, then our design could achieve very good performance. To be able to compare all of the reported works of Table IV-5, we have recalculated the FOM, after dropping IIP3 from FOM definition of (IV-101). This is acceptable in our work, since the linearity is not crucial in WSN applications. Then the table shows that our fabricated LNA has better performance than the reports of Elinger and Dopuis et *al.* and our last design, has superior performance!! Actually its performance is well comparable with two-stage LNA of Niknejad et *al.*, reported in 2007.

VI.1.4 Designed Receiver and Transmitter

We studied different receiver and transmitter structures to propose a suitable transceiver for our work. Then the main characteristics of the transceiver designed for WSN applications were studied. Prior to proposing proper architecture for transceiver, knowledge of the radio link is required. Actually the there is a two-sided relation between radio link design and transceiver architecture selection. In our work, the only available data was the carrier frequency (30GHz) and that the objective is a short-range WSN. So regarding the common characteristic of WSNs, i.e. low power, simple structure and low data rate, and using our experience in mm-wave design in 90nm CMOS, we developed a simple radio link protocol for our work. Features of the designed radio link have been listed in Table V-3 of Chapter V. After radio link, design, we proposed a simple transceiver structure. Time-division duplexing were used, instead of conventional frequency-division duplexing. The reason is the nature of communication in WSN, in which all of nodes have the ability to communicate with each other and hence all of the nodes must have the same carrier frequency for receive and transmit. The receiver uses an image reject filter, prior to LNA to reject the image band of the input signals. Even harmonic mixer has been used to reduce the LO frequency down to half of the carrier frequency, to gain the benefits of low frequency LO, as well as preventing many leakage effects in the receiver. Multi-slice IF amplifier has been adopted to increase the receiver dynamic range and improve its performance, without any power budget. Finally, a simple differential envelope detector has been use for detecting OOK pulses. The transmitter is simply a power VCO, connected directly to the antenna.

After determining the transceiver structure, we proposed the primary design for all of the required building blocks, unless for the LNA that was designed and finalized previously. We proposed two low power topologies for VCO, i.e. Pierce-like and Miller-like oscillators. We analysed these oscillators, in addition to the low power current reuse cross coupled oscillator, developed for low power applications. Three oscillators were compared using analysis and simulation results. Finally, we proposed the current reuse cross coupled oscillator for receiver LO and Miller-like oscillator for transmitter. We designed these two oscillators and simulated them in the foundry design kit and we achieved the desired performance with only 1.2mW power consumption. The active CMOS even harmonic mixer, available in the reported works, was chosen in our work, after a small modification to integrate the IF filter in the mixer. This relaxed the IF amplifiers from tuned load and simplified the IF amplifier design. We developed simple analysis and the analysis results showed that the active CMOS even harmonic mixer has potentially the same performance as the conventional active CMOS mixer, with VCO in the half of the required LO frequency, the interesting property in mm-wave band. We developed simple analytic equations to calculate the conversion gain of the even harmonic mixer and to optimize some of its parameters analytically. The performance of our mixer has been compared with the published Ka band mixers, in Table V-4 of Chapter V. This table shows that our design has good performance, with extremely low power consumption. Of course our mixer is a primary design, and can not be compared with

fabricated ones, though the results reveal the high potential of our design in low-power applications.

The IF amplifiers have been designed using very simple inverter-like class-A topologies. Since we have integrated the IF filter in the mixer circuit, there is no need for tuned load in the IF amplifiers. On the other hand, the inverter-like class-A amplifier has enough gain in 90nm CMOS in 2GHz band, without need for tuned load. We achieved the required voltage gain for IF stages, with power consumption well below that of other blocks. Total IF stage was designed in 4-slices, with voltage gains equal to 1000, 120, 26 and 4.5. The final stage in each slice has the role of limiting amplifier. Multi-slice structure increases the performance of the receiver for the strong received signals. The importance of the multi-slice structure was described using system level simulation of the designed receiver in MATLAB. The envelope detector has been designed as a differential common-drain stage, capable of detecting signals greater than 80mV. The response curve of detector is linear up to 850mV.

The designed receiver has 6.65mW power dissipation, well below the power dissipation of reported mm-wave receivers (fabricated), as shown in Table V-7. The transmitter was designed as a power VCO, directly connected to the antenna. We found that this structure is more preferable than switch mode power amplifiers. The total power efficiency of the transmitter is better than 25%. Comparisons in Table V-1 show that this efficiency is very good result in mm-wave band. Power dissipation of the transmitter is 24mW and transmits more than 6mW RF power.

VI.2 Suggestions

As mentioned, this thesis was an attempt toward an mm-wave ultra low power fully integrated RF transceiver for WSN application. Since our design was the first work of this kind in mm-wave band (at least in the laboratory we were working in), it inherently has many shortages, and meanwhile it can be a guideline for the future researches. Here we have some propositions to complete this work.

A) Simple Model for MOS Devices

In Chapter I we investigated different models for MOS devices. Based on our study, it is explained that new trend in nm-scale MOS device modeling is mitigation form threshold voltage based models (like BSIM4) toward surface potential based models (like MOS11 or BSIM5). Surface potential based models are physical based models with lower number of model parameters and better accuracy, in comparison with threshold voltage based models. Actually in the case of nano-metric MOS devices, threshold voltage based models have been deviated from a physical model, due to many required fitting parameters. The simple model we developed in Chapter II, was also a voltage threshold based model. However using the basic surface potential equation along the channel of MOS transistor [1], it is possible to develop more simple and more accurate I-V model. In the substrate model we have developed, the resistive elements of the substrate network were calculated using the sheet resistance of the substrate layer, in different conditions. However the sheet resistance method is not accurate for the resistances with short length, specially in higher frequencies. It is possible to find better analytic equations to describe the current distribution in the substrate and hence more accurate substrate model.

Varactors

B) Passive Elements Modeling

The models for passive devices were presented in Chapter III. In deriving our model for line-type inductor and transmission lines, we used analytic equations from the reported works. However the line structure we have used is different from the reported ones and hence we

used proper fitting elements to obtain agreements between the analysis results and that of full wave simulations. Nevertheless, it is possible to derive more accurate analytic equations, individually for our line structure using conformal mapping technique. To obtain an accurate substrate loss model in the transmission lines and inductors, it is necessary to fabricate some test elements. Then the test of this elements needs to accurate on-wafer calibration elements, similar to ones reported in [2]. Although we obtained very good results with line-type inductors, our optimization program shows that these inductors are suitable for the inductors smaller than 300pH. For higher inductances spiral inductors can yield higher quality factor and smaller area. This is why the spiral inductors have been considered in the recently published mm-wave bulk CMOS works [3], [4]. However modeling and design of spiral inductors is very complicated, in comparison with the line-type inductors. Actually a comprehensive study and analysis is required to develop a modeling and optimization tool for spiral inductors in mm-wave band.

We used MIM capacitors, offered by the available technology. This inductors have very good quality factor and high inductance-per-unit area. However in some cases, e.g. the coupling capacitors series with transmission lines, specially designed capacitors may have better performance than MIM capacitors [5]. Design and modeling of such inductors needs its individual mathematical and modeling suggestions.

C) LNA and Mixer

We used common source cascode topology in our work and good results have obtained. However in recent years some literatures have advised the common-gate topology for low-power applications, to obtain better noise figure in CMOS technologies. This may be analysed and suggested via analytic and simulation methods. We used 2um width for gate fingers, based on the reported works and our distributed analysis of MOS transistor in Chapter II. However, the exact value of optimum gate finger width can be calculated using accurate analysis and modeling efforts. We have some difficulties in the measurement process of the fabricated LNA, related to the calibration process of the VAN[1]. To perform more accurate and reliable measurement, it is necessary to fabricated proper calibration structures in the fabricated chip, as explained in [2].

We used active even-harmonic topology for the down-conversion mixer. Some reports have suggested passive CMOS mixers for low power applications [6]. Passive mixers have better flicker noise performance, with zero power dissipation. It is a good idea to analyse the performance of passive mixers in low power applications.

In our simulations in the foundry design kit and in our models, we used only the typical model parameters of the devices available in the design kit library. To investigate the effect of process variations on the performance of the circuits, corner-case model parameters should be used. For this purpose, all of the parameters are our models should be re-extracted form design kit models.

D) Transceiver

We used OOK modulation in our work, based on the study of reported works and simplicity of OOK modulation. However BFSK modulation is also a good candidate and has some advantages over OOK, in expense of more complicated circuit. Accurate analysis and study is required to select one of these modulations.

We studied various transceiver structures reported for WSN application and used heterodyne receiver structure in this work. However, the impulse radio transceiver structure may be another candidate for WSN applications [7]. This structure has been selected in IEEE

[1] Vector Network Analyzer

standards for short range communications. The impulse radio structure is a carrier-less structure and very high data rate (ultra-narrow pulses) are applied directly to antenna and propagated, the technique is practical only for very short ranges. Beside its simplicity, the main advantage of this structure is its very high data rate that facilitates multiplexing of many sensor nodes using Pseudo-Noise (PN) sequence, without need for frequency division multiplexing of sensor nodes. The reported impulse radio systems have power consumptions beyond the limit to be accepted for WSN application, but it is possible to develop simple structures of this technique with lower power consumptions.

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Calculation of small signal capacitances

Here we rewrite the basic equations. From (II-29) we have:

$$Q_c = Q_{c\_lin}\left(\frac{L-x}{L}\right) \tag{A-1}$$

In which x has been defined in (II-32) as:

$$x = \frac{\lambda_1 V'_{ds} + \lambda_2 (V'_{ds})^2}{Q_{c0}} \tag{A-2}$$

And Q_{c_lin} has been defined in (II-28) as:

$$Q_{c\_lin} = Q_{c0}\frac{2V_{dsat} - V''_{ds}}{2V_{dsat}} \tag{A-3}$$

V'_{ds} and V''_{ds} has been defined in (II-26) as:

$$\begin{aligned} V'_{ds} &= \sqrt[q]{V_{ds}^q + V_{dsat}^q} - V_{dsat} \\ V''_{ds} &= V_{ds} - V'_{ds} \end{aligned} \tag{A-4}$$

And Q_{c0} has been defined in (II-23) as:

$$Q_{c0} = W_{eff} L_{eff} C_{ox} n v_t \ln\left(1+\exp\left(\frac{V_{gs} - V_{th} - V_{off}}{n v_t}\right)\right) \tag{A-5}$$

V_{dsat} has been defined in (II-27) as :

$$V_{dsat} = \frac{V_\infty}{2}\left(1+\tanh\left(k(V_{gs} - V_{off})\right)\right) \tag{A-6}$$

E) Channel Charge Derivative With Respect to V_{gs}

Using (A-1) we have:

$$\frac{\partial Q_c}{\partial V_{gs}} = \frac{\partial Q_{c\_lin}}{\partial V_{gs}} - \frac{\partial}{L\partial V_{gs}}\left(xQ_{c\_lin}\right) \tag{A-7}$$

Using (A-2) and (A-3)we obtain:

$$\frac{\partial}{\partial V_{gs}}\left(xQ_{c\_lin}\right) = \left(\lambda_1 + 2\lambda_2 V'_{ds}\right)\left(\frac{2V_{dsat} - V''_{ds}}{2V_{dsat}}\right)\frac{\partial V'_{ds}}{\partial V_{gs}} - V'_{ds}\left(\frac{\lambda_1 + \lambda_2 V'_{ds}}{2}\right)\frac{\partial}{\partial V_{gs}}\left(\frac{V''_{ds}}{V_{dsat}}\right) \tag{A-8}$$

We can write:

$$\frac{\partial}{\partial V_{gs}}\left(\frac{V''_{ds}}{V_{dsat}}\right) = -\frac{1}{V_{dsat}}\frac{\partial V'_{ds}}{\partial V_{gs}} - \frac{V''_{ds}}{V_{dsat}^2}\frac{\partial V_{dsat}}{\partial V_{gs}} \tag{A-9}$$

Using (A-4) we have:

$$\frac{\partial V'_{ds}}{\partial V_{gs}} = \left(\left(V_{ds}^q + V_{dsat}^q\right)^{\frac{1}{q}-1} V_{dsat}^{q-1} - 1\right)\frac{\partial V_{dsat}}{\partial V_{gs}} \tag{A-10}$$

And using (A-6) we have:

$$\frac{\partial V_{dsat}}{\partial V_{gs}} = \frac{kV_\infty}{2\cosh^2\left(k(V_{gs} - V_{off})\right)} \tag{A-11}$$

On the other hand from (A-3) we have:

$$\frac{\partial}{\partial V_{gs}}\left(Q_{c\_lin}\right) = -\frac{Q_{c0}}{2}\frac{\partial}{\partial V_{gs}}\left(\frac{V''_{ds}}{V_{dsat}}\right) + \left(\frac{2V_{dsat} - V''_{ds}}{2V_{dsat}}\right)\frac{\partial Q_{c0}}{\partial V_{gs}} \tag{A-12}$$

And from (A-5) we have:

$$\frac{\partial Q_{c0}}{\partial V_{gs}} = \frac{W_{eff} L_{eff} C_{ox}}{1+\exp\left(\frac{-V_{gs}+V_{th}+V_{off}}{n v_t}\right)} \tag{A-13}$$

F) Channel Charge Derivative With Respect to V_{ds}

Using (A-1) we have:

$$\frac{\partial Q_c}{\partial V_{ds}} = \frac{\partial Q_{c\_lin}}{\partial V_{ds}} - \frac{\partial}{L \partial V_{ds}}\left(x Q_{c\_lin}\right) \tag{A-14}$$

Using (A-2) and (A-3)we obtain:

$$\frac{\partial}{\partial V_{ds}}\left(x Q_{c\_lin}\right) = \left(\lambda_1 + 2\lambda_2 V'_{ds}\right)\left(\frac{2V_{dsat} - V''_{ds}}{2V_{dsat}}\right)\frac{\partial V'_{ds}}{\partial V_{ds}} - \frac{V'_{ds}\left(\lambda_1 + \lambda_2 V'_{ds}\right)}{2V_{dsat}}\frac{\partial V''_{ds}}{\partial V_{ds}} \tag{A-15}$$

From (A-5) we can write:

$$\frac{\partial V''_{ds}}{\partial V_{ds}} = -\frac{\partial V'_{ds}}{\partial V_{ds}} \tag{A-16}$$

Note that using (A-6) we have:

$$\frac{\partial V_{dsat}}{\partial V_{ds}} = 0 \tag{A-17}$$

Using (A-4) we have:

$$\frac{\partial V'_{ds}}{\partial V_{ds}} = \left(V_{ds}^q + V_{dsat}^q\right)^{\frac{1}{q}-1} V_{ds}^{q-1} \tag{A-18}$$

On the other hand considering (A-4) and (A-5) and using (A-3) we obtain:

$$\frac{\partial}{\partial V_{ds}}\left(Q_{c\_lin}\right) = \frac{Q_{c0}}{2V_{dsat}}\frac{\partial V'_{ds}}{\partial V_{ds}} \tag{A-19}$$

G) Source/Drain Charge Derivative With Respect to V_{gs} and V_{ds}

Using (II-38) we have:

$$\begin{aligned}\frac{\partial Q_d}{\partial V_{ds}} &= Q_c \frac{\partial b}{\partial V_{ds}} + b\frac{\partial Q_c}{\partial V_{ds}} \\ \frac{\partial Q_d}{\partial V_{gs}} &= Q_c \frac{\partial b}{\partial V_{gs}} + b\frac{\partial Q_c}{\partial V_{gs}}\end{aligned} \tag{A-20}$$

Using (II-39) we obtain:

$$\begin{aligned}\frac{\partial b}{\partial V_{ds}} &= \frac{-1}{10V_{cp}\cosh^2\left(\frac{V'_{ds}}{V_{cp}}\right)}\frac{\partial V'_{ds}}{\partial V_{ds}} \\ \frac{\partial b}{\partial V_{gs}} &= \frac{-1}{10V_{cp}\cosh^2\left(\frac{V'_{ds}}{V_{cp}}\right)}\frac{\partial V'_{ds}}{\partial V_{gs}}\end{aligned} \tag{A-21}$$

Also we have:

$$\frac{\partial Q_s}{\partial V_{gs}} = -\frac{\partial Q_d}{\partial V_{gs}}$$
$$\frac{\partial Q_s}{\partial V_{ds}} = -\frac{\partial Q_d}{\partial V_{ds}} \qquad \text{(A-22)}$$

H) Bulk Charge Derivative With Respect to V_{gs} and V_{ds}

From (II-39) we deduce:

$$\frac{\partial Q_b}{\partial V_{ds}} = 0$$
$$\frac{\partial Q_b}{\partial V_{gs}} = C_1 \frac{\partial V_1}{\partial V_{gs}} + C_2 \frac{\partial V_2}{\partial V_{gs}} \qquad \text{(A-23)}$$

Where using (II-35) we have:

$$\frac{\partial V_1}{\partial V_{gs}} = \frac{-1}{1+\exp\left(\frac{V_{gs}-V_{ac}}{nv_t}\right)}$$
$$\frac{\partial V_2}{\partial V_{gs}} = \frac{-1}{1+\exp\left(\frac{V_{gs}-V_{th}}{nv_t}\right)} \qquad \text{(A-24)}$$

I) Small Signal Capacitances

Using the previous equations we can calculate the small signal capacitances as follows:

$$C_{gg} = \frac{\partial Q_c}{\partial V_g} + \frac{\partial Q_b}{\partial V_g} = \frac{\partial Q_c}{\partial V_{gs}} + \frac{\partial Q_b}{\partial V_{gs}}$$
$$C_{gs} = \frac{\partial Q_c}{\partial V_s} = -\frac{\partial Q_c}{\partial V_{gs}} - \frac{\partial Q_c}{\partial V_{ds}}$$
$$C_{gd} = \frac{\partial Q_c}{\partial V_d} = \frac{\partial Q_c}{\partial V_{ds}}$$

$$C_{sg} = \frac{\partial Q_s}{\partial V_g} = \frac{\partial Q_s}{\partial V_{gs}}$$
$$C_{ss} = \frac{\partial Q_s}{\partial V_s} = -\frac{\partial Q_s}{\partial V_{gs}} - \frac{\partial Q_s}{\partial V_{ds}} \qquad \text{(A-25)}$$
$$C_{sd} = \frac{\partial Q_s}{\partial V_d} = \frac{\partial Q_c}{\partial V_{ds}}$$

$$C_{dg} = \frac{\partial Q_d}{\partial V_g} = \frac{\partial Q_d}{\partial V_{gs}}$$
$$C_{ds} = \frac{\partial Q_d}{\partial V_s} = -\frac{\partial Q_d}{\partial V_{gs}} - \frac{\partial Q_d}{\partial V_{ds}}$$
$$C_{dd} = \frac{\partial Q_d}{\partial V_d} = \frac{\partial Q_d}{\partial V_{ds}}$$

Y parameters of Distributed Model of MOS Transistor

Assuming that the transistor has been distributed homogeneously along the gate width, the elements in distributed model of Fig. II-15 are calculated as follows:

$$\delta g_m = \frac{g_m}{W}\delta x \qquad \delta Y_{gd} = \frac{Y_{gd}}{W}\delta x$$
$$\delta Y_{ds} = \frac{Y_{ds}}{W}\delta x \qquad \delta R_g = \frac{R_g}{W}\delta x = \frac{\rho_p}{L}\delta x \tag{B-1}$$
$$\delta Y_{gs} = \frac{Y_{gs}}{W}\delta x$$

regarding Fig. II-15 we have:

$$\delta I = -\delta I_d - \delta I_s$$
$$I(x) = \frac{-\delta V(x)}{\delta R_g}$$
$$V(x) - V_d = \frac{\delta I_d(x)}{\delta Y_{gd}} \tag{B-2}$$
$$V(x) - V_s = \frac{\delta I_s(x)}{\delta Y_{gs}}$$

And using the definitions in (B-1) we can rewrite (B-2) as:

$$I(x) = -\frac{L}{\rho_p}\frac{\delta V(x)}{\delta x}$$
$$V(x) - V_d = \frac{W}{Y_{gd}}\frac{\delta I_d(x)}{\delta x} \tag{B-3}$$
$$V(x) - V_s = \frac{W}{Y_{gs}}\frac{\delta I_s(x)}{\delta x}$$

From (B-2) and (B-3) we deduce:

$$\begin{cases} \dfrac{\delta I(x)}{\delta x} = -\dfrac{Y_{gd}}{W}\left(V(x) - V_d\right) - \dfrac{Y_{gs}}{W}\left(V(x) - V_s\right) \\ I(x) = -\dfrac{L}{\rho_p}\dfrac{\delta V(x)}{\delta x} \end{cases} \tag{B-4}$$

These equations are our fundamental transmission line equations. Differentiating the second equation in (B-4) and substituting the first equation of (B-4) we obtain:

$$\frac{\delta^2 V(x)}{\delta x^2} = \frac{\rho_p}{WL}\left(Y_{gd} + Y_{gs}\right)V(x) - \frac{\rho_p}{WL}\left(Y_{gd}V_d + Y_{gs}V_s\right) \tag{B-5}$$

The differential equation (B-5) has the solution of the form:

$$V(x) = V^+ e^{-\kappa . x} + V^- e^{\kappa . x} + \frac{\rho_p}{\kappa^2 WL}\left(Y_{gd}V_d + Y_{gs}V_s\right) \tag{B-6}$$

In which:

$$\kappa = \sqrt{\frac{\rho_p}{WL}\left(Y_{gd} + Y_{gs}\right)} \tag{B-7}$$

Now from second equation in (B-4) we obtain:

$$I(x)=\frac{\kappa L}{\rho_p}\left(V^+e^{-\kappa.x}-V^-e^{\kappa.x}\right) \tag{B-8}$$

To calculate the currents into the gate, drain and source nodes we can write (see Fig. 2-15):

$$\delta I_{gs}(x)=(V(x)-V_s)\frac{Y_{gs}}{W}\delta x$$

$$\delta I_{gd}(x)=(V(x)-V_d)\frac{Y_{gd}}{W}\delta x \tag{B-9}$$

$$\delta I_{ds}(x)=(V_d-V_s)\frac{Y_{ds}}{W}\delta x+(V(x)-V_s)\frac{g_m}{W}\delta x$$

Also we have:

$$\begin{aligned}\delta I_g(x)&=\delta I_{gs}(x)+\delta I_{gd}(x)\\ \delta I_d(x)&=\delta I_{ds}(x)-\delta I_{gd}(x)\\ \delta I_s(x)&=-\delta I_{gs}(x)-\delta I_{ds}(x)\end{aligned} \tag{B-10}$$

Using (B-9) and (B-10) we deduce:

$$\delta I_g(x)=\left(\frac{Y_{gs}+Y_{gd}}{W}\right)V(x)\delta x-\frac{Y_{gs}}{W}V_s\delta x-\frac{Y_{gd}}{W}V_d\delta x$$

$$\delta I_d(x)=\left(\frac{g_m-Y_{gd}}{W}\right)V(x)\delta x-\frac{g_m+Y_{ds}}{W}V_s\delta x+\frac{Y_{ds}+Y_{gd}}{W}V_d\delta x \tag{B-11}$$

$$\delta I_s(x)=\left(-\frac{g_m+Y_{gs}}{W}\right)V(x)\delta x+\frac{g_m+Y_{ds}+Y_{gs}}{W}V_s\delta x-\frac{Y_{ds}}{W}V_d\delta x$$

Integrating (B-11) with respect to x, from 0 to W we obtain:

$$I_g=\left(\frac{Y_{gs}+Y_{gd}}{W}\right)\int_0^W V(x)\delta x-Y_{gs}V_s-Y_{gd}V_d$$

$$I_d=\left(\frac{g_m-Y_{gd}}{W}\right)\int_0^W V(x)\delta x-(g_m+Y_{ds})V_s+(Y_{ds}+j\omega C_{gd})V_d \tag{B-12}$$

$$I_s=\left(-\frac{g_m+Y_{gs}}{W}\right)\int_0^W V(x)\delta x+(g_m+Y_{ds}+Y_{gs})V_s-Y_{ds}V_d$$

So if we have the required boundary conditions to solve (B-6), then we can calculate the nodes current in (B-12). Then Y parameters can be calculated simply. We consider single and double connection structures separately.

J) Single connection gate finger

In this case the boundary conditions are:

$$\begin{aligned}V(x)\big|_{x=0}&=V_g\\ I(x)\big|_{x=W}&=0\end{aligned} \tag{B-13}$$

applying the first condition into (B-6) we obtain:

$$V_g=V^++V^-+\frac{\rho_p}{\kappa^2WL}\left(Y_{gd}V_d+Y_{gs}V_s\right)$$

And applying the second condition into (B-8) we obtain:

$$V^+e^{-\kappa W}=V^-e^{\kappa W}$$

From two above equations we obtain the required parameters:

$$V^+ = \frac{e^{\kappa W}}{e^{\kappa W} + e^{-\kappa W}} \left(V_g - \frac{\rho_p}{\kappa^2 WL} \left(Y_{gd} V_d + Y_{gs} V_s \right) \right)$$
$$V^- = \frac{e^{-\kappa W}}{e^{\kappa W} + e^{-\kappa W}} \left(V_g - \frac{\rho_p}{\kappa^2 WL} \left(Y_{gd} V_d + Y_{gs} V_s \right) \right) \quad \text{(B-14)}$$

Y_{11} , Y_{21} , Y_{31}

To calculate Y_{11} , Y_{21} and Y_{31} we must set V_s=V_d=*0*. So from (B-14) we have:

$$V^+ = \frac{e^{\kappa W}}{e^{-\kappa W} + e^{\kappa W}} V_g$$
$$V^- = \frac{e^{-\kappa W}}{e^{-\kappa W} + e^{\kappa W}} V_g$$

Substituting V^+ and V^- in (B-6) and setting V_s=V_d=*0*, we deduce:

$$V(x) = \frac{e^{\kappa W} e^{-\kappa . x} + e^{-\kappa W} e^{\kappa . x}}{e^{-\kappa W} + e^{\kappa W}} V_g$$

And hence we have:

$$\int_0^W V(x) \delta x = \frac{\tanh(\kappa W)}{\kappa} V_g \quad \text{(B-15)}$$

To calculate Y_{11}, we substitute (B-15) in the first equation of (B-12) and set V_s=V_d=0. So we obtain:

$$I_g = \left(\frac{Y_{gs} + Y_{gd}}{W} \right) \frac{\tanh(\kappa W)}{\kappa} V_g$$

Now Y_{11} is calculated:

$$Y_{11} = \left. \frac{I_g}{V_g} \right|_{V_s = V_d = 0} = \left(Y_{gs} + Y_{gs} \right) \frac{\tanh(\kappa W)}{\kappa W} \quad \text{(B-16)}$$

To calculate Y_{21}, we substitute (B-15) in the second equation of (B-12) and set V_s=V_d=0. So we conclude:

$$I_d = \left(\frac{g_m - j\omega C_{gd}}{W} \right) \frac{\tanh(\kappa W)}{\kappa} V_g$$

Finally we obtain:

$$Y_{21} = \left. \frac{I_d}{V_g} \right|_{V_d = V_s = 0} = \left(g_m - Y_{gd} \right) \frac{\tanh(\kappa W)}{\kappa W} \quad \text{(B-17)}$$

To calculate Y_{31}, we substitute (B-15) in the third equation of (B-12) and set V_s=V_d=0 :

$$I_s = \left(-\frac{g_m + Y_{gs}}{W} \right) \frac{\tanh(\kappa W)}{\kappa} V_g$$

So Y_{31} is calculated:

$$Y_{31} = \left. \frac{I_s}{V_g} \right|_{V_d = V_s = 0} = -\left(g_m + Y_{gs} \right) \frac{\tanh(\kappa W)}{\kappa W} \quad \text{(B-18)}$$

Y_{12} , Y_{22} , Y_{32}

To calculate Y_{12} , Y_{22} and Y_{32} we must set $V_g=V_s=0$. So from (B-14) we have:

$$V^+ = \frac{e^{\kappa W}}{e^{\kappa W}+e^{-\kappa W}}\left(-\frac{\rho_p}{\kappa^2 WL}\left(Y_{gd}V_d\right)\right)$$
$$V^- = \frac{e^{-\kappa W}}{e^{\kappa W}+e^{-\kappa W}}\left(-\frac{\rho_p}{\kappa^2 WL}\left(Y_{gd}V_{ds}\right)\right) \quad \text{(B-19)}$$

Substituting V^+ and V^- in (B-6) we obtain:

$$V(x) = Y_{gd}\frac{\rho_p}{\kappa^2 WL}\left(-\frac{e^{\kappa W}e^{-\kappa x}+e^{-\kappa W}e^{\kappa x}}{e^{\kappa W}+e^{-\kappa W}}+1\right)V_d$$

The integral of gate voltage is:

$$\int_0^W V(x)\delta x = Y_{gd}\frac{\rho_p}{\kappa^2 L}\left(1-\frac{\tanh(\kappa W)}{\kappa W}\right)V_d \quad \text{(B-20)}$$

To calculate Y_{12}, we substitute (B-20) in the first equation of (B-12) and set $V_s=V_g=0$. So we obtain:

$$I_g = -Y_{gd}\frac{\tanh(\kappa W)}{\kappa W}V_d$$

Finally we obtain:

$$Y_{12} = \left.\frac{I_g}{V_d}\right|_{V_g=V_s=0} = -Y_{gd}\frac{\tanh(\kappa W)}{\kappa W} \quad \text{(B-21)}$$

To calculate Y_{22}, we substitute (B-20) in the second equation of (B-12) and set $V_s=V_g=0$. So we obtain:

$$I_d = Y_{gd}\left(\frac{g_m - Y_{gd}}{Y_{gd}+Y_{gs}}\right)\left(1-\frac{\tanh(\kappa W)}{\kappa W}\right)V_d + \left(Y_{gd}+Y_{ds}\right)V_d$$

Finally we reach:

$$Y_{22} = \left.\frac{I_d}{V_d}\right|_{V_g=V_s=0} = \frac{Y_{gd}}{Y_{gd}+Y_{gs}}\left(g_m - Y_{gd}\right)\left(1-\frac{\tanh(\kappa W)}{\kappa W}\right)+\left(Y_{gd}+Y_{ds}\right) \quad \text{(B-22)}$$

To calculate Y_{22}, we substitute (B-20) in the third equation of (B-12) and set $V_s=V_g=0$. So we obtain:

$$I_s = -\frac{Y_{gd}}{Y_{gd}+Y_{gs}}\left(g_m+Y_{gs}\right)\left(1-\frac{\tanh(\kappa W)}{\kappa W}\right)V_d - Y_{ds}V_d$$

And hence:

$$Y_{32} = \left.\frac{I_s}{V_d}\right|_{V_g=V_s=0} = -\frac{Y_{gd}}{Y_{gd}+Y_{gs}}\left(g_m+Y_{gs}\right)\left(1-\frac{\tanh(\kappa W)}{\kappa W}\right)-Y_{ds} \quad \text{(B-23)}$$

Y_{13} , Y_{23} , Y_{33}

To calculate Y_{13} , Y_{23} and Y_{33} we must set $V_g=V_d=0$. So using (B-14) we have:

$$V^+ = \frac{e^{\kappa W}}{e^{\kappa W}+e^{-\kappa W}}\left(-\frac{\rho_p}{\kappa^2 WL}Y_{gs}\right)V_s$$
$$V^- = \frac{e^{-\kappa W}}{e^{\kappa W}+e^{-\kappa W}}\left(-\frac{\rho_p}{\kappa^2 WL}Y_{gs}\right)V_s \quad \text{(B-24)}$$

Substituting V^+ and V^- in (B-6) we obtain:

$$V(x)=\left(-\frac{\rho_p}{\kappa^2 WL}Y_{gs}\right)\left(\frac{e^{\kappa W}e^{-\kappa.x}+e^{-\kappa W}e^{\kappa.x}}{e^{\kappa W}+e^{-\kappa W}}-1\right)V_s$$

The integral of gate voltage is:

$$\int_0^W V(x)\delta x=\left(\frac{\rho_p}{\kappa^2 L}Y_{gs}\right)\left(1-\frac{\tanh(\kappa W)}{\kappa W}\right)V_s \qquad \text{(B-25)}$$

To calculate Y_{13}, we substitute (B-23) in the first equation of (B-12) and set V_d=V_g=0. So we obtain:

$$I_g=Y_{gs}\left(1-\frac{\tanh(\kappa W)}{\kappa W}\right)V_s-Y_{gs}V_s$$

So we can write:

$$Y_{13}=\left.\frac{I_g}{V_s}\right|_{V_g=V_d=0}=Y_{gs}\left(1-\frac{\tanh(\kappa W)}{\kappa W}\right)-Y_{gs} \qquad \text{(B-26)}$$

To calculate Y_{23}, we substitute (B-23) in the second equation of (B-12) and set V_d=V_g=0. So we obtain:

$$I_g=(g_m-Y_{gd})\frac{Y_{gs}}{Y_{gd}+Y_{gs}}\left(1-\frac{\tanh(\kappa W)}{\kappa W}\right)V_s-(Y_{ds}+g_m)V_s$$

Consequently we have:

$$Y_{23}=\left.\frac{I_d}{V_s}\right|_{V_g=V_d=0}=Y_{gs}\frac{g_m-Y_{gd}}{Y_{gd}+Y_{gs}}\left(1-\frac{\tanh(\kappa W)}{\kappa W}\right)-(Y_{ds}+g_m) \qquad \text{(B-27)}$$

To calculate Y_{33}, we substitute (B-23) in the third equation of (B-12) and set V_d=V_g=0. So we obtain:

$$I_s=-Y_{gs}\frac{g_m+Y_{gs}}{Y_{gd}+Y_{gs}}\left(1-\frac{\tanh(\kappa W)}{\kappa W}\right)V_s+(Y_{gs}+Y_{ds}+g_m)V_s$$

Finally we deduce:

$$Y_{33}=\left.\frac{I_s}{V_s}\right|_{V_g=V_d=0}=-Y_{gs}\frac{g_m+Y_{gs}}{Y_{gd}+Y_{gs}}\left(1-\frac{\tanh(\kappa W)}{\kappa W}\right)+(Y_{gs}+Y_{ds}+g_m) \qquad \text{(B-28)}$$

K) Double-end connected finger

Considering double-end connected finger we have equal voltage and current in both ends of the finger and zero current at mid point of gate finger. Denoting the voltage and total gate current with I_g and V_g, we have the boundary conditions as below:

$$V\big|_{x=0}=V_g$$

$$V\big|_{x=W}=V_g$$

applying the conditions (57) into (6) and (8) we obtain:

$$V^+=\left(\frac{e^{\kappa W}-1}{e^{\kappa W}-e^{-\kappa W}}\right)\left(V_g-\frac{\rho_p}{\kappa^2 WL}\left(j\omega C_{gd}V_d+Y_{gs}V_s\right)\right)$$

$$V^-=\left(\frac{1-e^{-\kappa W}}{e^{\kappa W}-e^{-\kappa W}}\right)\left(V_g-\frac{\rho_p}{\kappa^2 WL}\left(j\omega C_{gd}V_d+Y_{gs}V_s\right)\right) \qquad \text{(B-27)}$$

Y_{11} , Y_{21} , Y_{31}

To calculate Y_{11} , Y_{21} and Y_{31} we must set $V_s=V_d=0$. So from (B-27) we have:

$$V^+ = -V_g \frac{1-e^{\kappa W}}{e^{\kappa W}-e^{-\kappa W}}$$
$$V^- = V_g \frac{1-e^{-\kappa W}}{e^{\kappa W}-e^{-\kappa W}} \qquad \text{(B-28)}$$

Substituting (B-28) in (B-6) and setting $V_s=V_d=0$, we deduce:

$$V(x) = \frac{e^{-\kappa x} - e^{\kappa x} - e^{-\kappa(x-W)} + e^{\kappa(x-W)}}{e^{-\kappa W}-e^{\kappa W}} V_g$$

And hence we have:

$$\int_0^W V(x)\delta x = 2W\left(\frac{\cosh(\kappa W)-1}{\kappa W \sinh(\kappa W)}\right)V_g \qquad \text{(B-29)}$$

To calculate Y_{11}, we substitute (B-29) in the first equation of (B-12) and set $V_s=V_d=0$. So we obtain:

$$\frac{I_g}{2} = \frac{\kappa L}{\rho_p}\left(\frac{e^{\kappa W}+e^{-\kappa W}-2}{e^{\kappa W}-e^{-\kappa W}}\right)V_g$$

Now using (B-7) Y_{11} is calculated:

$$Y_{11} = \left.\frac{I_g}{V_g}\right|_{V_s=V_d=0} = 2\left(Y_{gd}+Y_{gs}\right)\left(\frac{\cosh(\kappa W)-1}{\kappa W \sinh(\kappa W)}\right) \qquad \text{(B-30)}$$

To calculate Y_{21}, we substitute (B-29) in the second equation of (B-12) and set $V_s=V_d=0$. So we conclude:

$$I_d = 2\left(g_m - Y_{gd}\right)\left(\frac{\cosh(\kappa W)-1}{\kappa W \sinh(\kappa W)}\right)V_g$$

Finally we obtain:

$$Y_{21} = \left.\frac{I_d}{V_g}\right|_{V_d=V_s=0} = 2\left(g_m - Y_{gd}\right)\left(\frac{\cosh(\kappa W)-1}{\kappa W \sinh(\kappa W)}\right) \qquad \text{(B-31)}$$

To calculate Y_{31}, we substitute (B-29) in the third equation of (B-12) and set $V_s=V_d=0$:

$$I_s = -2\left(Y_{gs}+g_m\right)\left(\frac{\cosh(\kappa W)-1}{\kappa W \sinh(\kappa W)}\right)V_g$$

So Y_{31} is calculated:

$$Y_{31} = \left.\frac{I_s}{V_g}\right|_{V_d=V_s=0} = -2\left(Y_{gs}+g_m\right)\left(\frac{\cosh(\kappa W)-1}{\kappa W \sinh(\kappa W)}\right) \qquad \text{(B-32)}$$

Y_{12} , Y_{22} , Y_{32}

To calculate Y_{12} , Y_{22} and Y_{32} we must set $V_g=V_s=0$. So from (B-27) we have:

$$V^+ = \left(\frac{e^{\kappa W}-1}{e^{\kappa W}-e^{-\kappa W}}\right)\left(-j\omega C_{gd}\frac{\rho_p}{\kappa^2 WL}V_d\right)$$
$$V^- = \left(\frac{1-e^{-\kappa W}}{e^{\kappa W}-e^{-\kappa W}}\right)\left(-j\omega C_{gd}\frac{\rho_p}{\kappa^2 WL}V_d\right) \qquad \text{(B-33)}$$

Substituting (B-33) in (B-6) and setting $V_g=V_s=0$, we deduce:

$$V(x)=\left(-j\omega C_{gd}\frac{\rho_p}{\kappa^2 WL}\right)\left(\frac{\left(e^{\kappa W}-1\right)e^{-\kappa.x}+\left(1-e^{-\kappa W}\right)e^{\kappa.x}}{e^{\kappa W}-e^{-\kappa W}}-1\right)V_d$$

And the integral of gate voltage is calculated:

$$\int_0^W V(x)\delta x=-j\omega C_{gd}\frac{\rho_p}{\kappa^2 L}\left(2\frac{\cosh(\kappa W)-1}{\kappa W\sinh(\kappa W)}-1\right)V_d \qquad \text{(B-34)}$$

To calculate Y_{12}, we substitute (B-34) in the first equation of (B-12) and set $V_s=V_d=0$. So we obtain:

$$I_g=-j\omega C_{gd}\left(1+\left(2\frac{\cosh(\kappa W)-1}{\kappa W\sinh(\kappa W)}-1\right)\right)V_d$$

Now using (B-7) Y_{11} is calculated:

$$Y_{12}=\left.\frac{I_g}{V_d}\right|_{V_g=V_s=0}=-j\omega C_{gd}-j\omega C_{gd}\left(2\frac{\cosh(\kappa W)-1}{\kappa W\sinh(\kappa W)}-1\right) \qquad \text{(B-35)}$$

To calculate Y_{22}, we substitute (B-34) in the second equation of (B-12) and set $V_s=V_d=0$. So we conclude:

$$I_d=-j\omega C_{gd}\left(\frac{g_m-j\omega C_{gd}}{j\omega C_{gd}+Y_{gs}}\right)\left(2\frac{\cosh(\kappa W)-1}{\kappa W\sinh(\kappa W)}-1\right)V_d+\left(j\omega C_{gd}+g_{ds}\right)V_d$$

Finally we obtain:

$$Y_{22}=\left.\frac{I_d}{V_d}\right|_{V_g=V_s=0}=-j\omega C_{gd}\left(\frac{g_m-j\omega C_{gd}}{j\omega C_{gd}+Y_{gs}}\right)\left(2\frac{\cosh(\kappa W)-1}{\kappa W\sinh(\kappa W)}-1\right)+\left(j\omega C_{gd}+g_{ds}\right) \qquad \text{(B-36)}$$

To calculate Y_{32}, we substitute (B-34) in the third equation of (B-12) and set $V_s=V_d=0$:

$$I_s=j\omega C_{gd}\frac{g_m+Y_{gs}}{j\omega C_{gd}+Y_{gs}}\left(2\frac{\cosh(\kappa W)-1}{\kappa W\sinh(\kappa W)}-1\right)V_d-g_{ds}V_d$$

So Y_{31} is calculated:

$$Y_{32}=\left.\frac{I_s}{V_d}\right|_{V_g=V_s=0}=j\omega C_{gd}\frac{g_m+Y_{gs}}{j\omega C_{gd}+Y_{gs}}\left(2\frac{\cosh(\kappa W)-1}{\kappa W\sinh(\kappa W)}-1\right)-g_{ds} \qquad \text{(B-37)}$$

Y_{13} , Y_{23} , Y_{33}

To calculate Y_{13} , Y_{23} and Y_{33} we must set $V_g=V_d=0$. So from (B-27) we have:

$$V^+=-Y_{gs}\frac{\rho_p}{\kappa^2 WL}\left(\frac{e^{\kappa W}-1}{e^{\kappa W}-e^{-\kappa W}}\right)V_s$$

$$V^-=-Y_{gs}\frac{\rho_p}{\kappa^2 WL}\left(\frac{1-e^{-\kappa W}}{e^{\kappa W}-e^{-\kappa W}}\right)V_s \qquad \text{(B-38)}$$

Substituting (B-38) in (B-6) and setting $V_g=V_s=0$, we deduce:

$$V(x)=-Y_{gs}\frac{\rho_p}{\kappa^2 WL}\left(\frac{\left(e^{\kappa W}-1\right)e^{-\kappa.x}+\left(1-e^{-\kappa W}\right)e^{\kappa.x}}{e^{\kappa W}-e^{-\kappa W}}-1\right)V_s$$

And the integral of gate voltage is calculated:

$$\int_0^W V(x)\delta x=-Y_{gs}\frac{\rho_p}{\kappa^2 L}\left(2\frac{\cosh(\kappa W)-1}{\kappa W\sinh(\kappa W)}-1\right)V_s \qquad \text{(B-39)}$$

To calculate Y_{13}, we substitute (B-29) in the first equation of (B-12) and set V_s=V_d=0. So we obtain:

$$I_g = -Y_{gs}\left(2\frac{\cosh(\kappa W)-1}{\kappa W \sinh(\kappa W)}-1\right)V_s - Y_{gs}V_s$$

Now using (B-7) Y_{11} is calculated:

$$Y_{13} = \left.\frac{I_g}{V_s}\right|_{V_g=V_d=0} = -Y_{gs}\left(2\frac{\cosh(\kappa W)-1}{\kappa W \sinh(\kappa W)}-1\right) - Y_{gs} \qquad \text{(B-40)}$$

To calculate Y_{23}, we substitute (B-29) in the second equation of (B-12) and set V_s=V_d=0. So we conclude:

$$I_g = -Y_{gs}\frac{g_m - j\omega C_{gd}}{j\omega C_{gd} + Y_{gs}}\left(2\frac{\cosh(\kappa W)-1}{\kappa W \sinh(\kappa W)}-1\right)V_s - (g_{ds} + g_m)V_s$$

Finally we obtain:

$$Y_{23} = \left.\frac{I_d}{V_s}\right|_{V_g=V_d=0} = -Y_{gs}\frac{g_m - j\omega C_{gd}}{j\omega C_{gd} + Y_{gs}}\left(2\frac{\cosh(\kappa W)-1}{\kappa W \sinh(\kappa W)}-1\right) - (g_{ds} + g_m) \qquad \text{(B-41)}$$

To calculate Y_{33}, we substitute (B-29) in the third equation of (B-12) and set V_s=V_d=0 :

$$I_s = Y_{gs}\frac{g_m + Y_{gs}}{j\omega C_{gd} + Y_{gs}}\left(2\frac{\cosh(\kappa W)-1}{\kappa W \sinh(\kappa W)}-1\right)V_s + (Y_{gs} + g_{ds} + g_m)V_s$$

So Y_{31} is calculated:

$$Y_{33} = \left.\frac{I_s}{V_s}\right|_{V_g=V_d=0} = Y_{gs}\frac{g_m + Y_{gs}}{j\omega C_{gd} + Y_{gs}}\left(2\frac{\cosh(\kappa W)-1}{\kappa W \sinh(\kappa W)}-1\right) + (Y_{gs} + g_{ds} + g_m) \qquad \text{(B-42)}$$

Gate resistance calculation for lumped model

Distributed nature of gate resistance and capacitance has been shown in the Fig. C-I(a). Here the objective is to fine the circuit elements for the circuit of Fig. C-I(b), so that two circuits have equal input admittance. Using a simple analysis, like in the chapter II, the input admittance to the circuit of Fig. C-I(a) is calculated as:

$$Y_{in} = j\omega \frac{\tanh\left(W\sqrt{j\omega cr}\right)}{W\sqrt{j\omega cr}} \int \delta C \tag{C-1}$$

Then two circuits are equal, if we have:

$$\frac{1}{R_{eq}} = \mathrm{Re}\left(\frac{1}{Y_{in}}\right)$$
$$\frac{1}{\omega C_{eq}} = -\mathrm{Im}\left(\frac{1}{Y_{in}}\right) \tag{C-2}$$

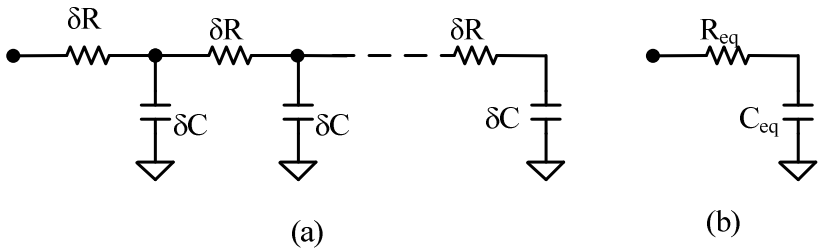

Fig. C-I. Distributed and lumped model for gate admittance

Using Fourier series expansion, one can show that in low frequencies (C-2) is approximated (third order approximation) by:

$$R_{eq} = \frac{1}{3}\int \delta R$$
$$C_{eq} = \int \delta C \tag{C-3}$$

That is the conventionally used equation in (II-74). In the case of double connection gate, as deduced from (II-74), equal admittance is:

$$Y_{in} = 2j\omega \frac{\cosh(\kappa W) - 1}{\kappa W \sinh(\kappa W)} \int \delta C \tag{C-4}$$

again the equality of two circuits is achieved when:

$$\frac{1}{R_{eq}} = \mathrm{Re}\left(\frac{1}{Y_{in}}\right)$$
$$\frac{1}{\omega C_{eq}} = -\mathrm{Im}\left(\frac{1}{Y_{in}}\right) \tag{C-5}$$

In low frequencies this is approximated (third order approximation) by:

$$R_{eq} = \frac{1}{12}\int \delta R$$
$$C_{eq} = \int \delta C \tag{C-6}$$

Y parameters for Substrate Network

Regarding Fig. II-33 we have:

$$I_{db} = y_{dbp}\left(V_d - V_{b2}\right)$$
$$I_{sb} = y_{sbp}\left(V_s - V_{b2}\right) \quad \text{(D-1)}$$
$$I_{b2} = g_{b2}\left(V_{b1} - V_{b2}\right)$$

Writing KCL in node b_2 node we deduce:

$$g_{bb}V_{b2} = I_{db} + I_{sb} + I_{b2} \quad \text{(D-2)}$$

In which $R_{bb} = R_{b3} + R_{rb}$

Substituting (D-1) in (D-2) we obtain:

$$g_{bb}V_{b2} = y_{dbp}V_d + y_{sbp}V_s + g_{b2}V_{b1} - \left(y_{dbp} + y_{sbp} + g_{b2}\right)V_{b2}$$

And defining:

$$y_{b2} = y_{dbp} + y_{sbp} + g_{b2} + g_{bb} \quad \text{(D-3)}$$

We have:

$$V_{b2} = \frac{y_{dbp}V_d + y_{sbp}V_s + g_{b2}V_{b1}}{y_{b2}} \quad \text{(D-4)}$$

Writing KCL in node b_1 in Fig. II-33 we have:

$$I_{b2} = I_{b1} + I_{gb}$$

So we deduce:

$$\left(g_{b2} + g_{b1} + y_{gbp}\right)V_{b1} - g_{b2}V_{b2} = g_{b1}V_{bi} + y_{gbp}V_g \quad \text{(D-5)}$$

Defining:

$$y_{b1} = g_{b2} + g_{b1} + y_{gbp} \quad \text{(D-6)}$$

And substituting (D-4) in (D-5) we obtain:

$$\left(y_{b1} - \frac{g_{b2}g_{b2}}{y_{b2}}\right)V_{b1} = g_{b1}V_{bi} + y_{gbp}V_g + g_{b2}\frac{y_{dbp}V_d + y_{sbp}V_s}{y_{b2}}$$

And hence:

$$V_{b1} = \frac{y_{b2}\left(g_{b1}V_{bi} + y_{gbp}V_g\right) + g_{b2}\left(y_{dbp}V_d + y_{sbp}V_s\right)}{\left(y_{b1}y_{b2} - g_{b2}g_{b2}\right)} \quad \text{(D-7)}$$

In the node b_i we have:

$$I_{dbi} = y_{dbi}\left(V_d - V_{bi}\right)$$
$$I_{sbi} = y_{sbi}\left(V_s - V_{bi}\right)$$
$$I_{gbi} = y_{gbi}\left(V_g - V_{bi}\right)$$

Writing KCL in this node we conclude:

$$\left(y_{dbi} + y_{sbi} + y_{gbi} + g_{b1}\right)V_{bi} - g_{b1}V_{b1} = y_{dbi}V_d + y_{sbi}V_s + y_{gbi}V_g \quad \text{(D-8)}$$

Defining:

$$y_{bi} = y_{dbi} + y_{sbi} + y_{gbi} + g_{b1}$$

And substituting (D-7) in (D-8) we obtain:

$$V_{bi}=\left(\frac{g_{b1}y_{b2}y_{gbp}+y_{b1}y_{b2}y_{gbi}-g_{b2}g_{b2}y_{gbi}}{y_{b1}y_{b2}y_{bi}-g_{b2}g_{b2}y_{bi}-g_{b1}y_{b2}g_{b1}}\right)V_g$$
$$+\left(\frac{g_{b1}g_{b2}y_{dbp}+y_{b1}y_{b2}y_{dbi}-g_{b2}g_{b2}y_{dbi}}{y_{b1}y_{b2}y_{bi}-g_{b2}g_{b2}y_{bi}-g_{b1}y_{b2}g_{b1}}\right)V_d \qquad \text{(D-9)}$$
$$+\left(\frac{g_{b1}g_{b2}y_{sbp}+y_{b1}y_{b2}y_{sbi}-g_{b2}g_{b2}y_{sbi}}{y_{b1}y_{b2}y_{bi}-g_{b2}g_{b2}y_{bi}-g_{b1}y_{b2}g_{b1}}\right)V_s$$

Defining :

$$\lambda_{bi}=y_{b1}y_{b2}y_{bi}-g_{b2}g_{b2}y_{bi}-g_{b1}y_{b2}g_{b1}$$
$$\lambda_g=g_{b1}y_{b2}y_{gbp}+y_{b1}y_{b2}y_{gbi}-g_{b2}g_{b2}y_{gbi}$$
$$\lambda_d=g_{b1}g_{b2}y_{dbp}+y_{b1}y_{b2}y_{dbi}-g_{b2}g_{b2}y_{dbi}$$
$$\lambda_s=g_{b1}g_{b2}y_{sbp}+y_{b1}y_{b2}y_{sbi}-g_{b2}g_{b2}y_{sbi}$$

We obtain :

$$V_{bi}=\frac{\lambda_g}{\lambda_{bi}}V_g+\frac{\lambda_d}{\lambda_{bi}}V_d+\frac{\lambda_s}{\lambda_{bi}}V_s \qquad \text{(D-10)}$$

Now we substitute (D-10) in (D-7) we deduce:

$$V_{b1}=\frac{\left(\lambda_g g_{b1}y_{b2}+\lambda_{bi}y_{gbp}y_{b2}\right)V_g+\left(\lambda_d g_{b1}y_{b2}+\lambda_{bi}g_{b2}y_{dbp}\right)V_d+\left(\lambda_s g_{b1}y_{b2}+\lambda_{bi}g_{b2}y_{sbp}\right)V_s}{\lambda_{bi}\left(y_{b1}y_{b2}-g_{b2}g_{b2}\right)}$$

And defining:

$$\beta_g=\lambda_g g_{b1}y_{b2}+\lambda_{bi}y_{gbp}y_{b2}$$
$$\beta_d=\lambda_d g_{b1}y_{b2}+\lambda_{bi}g_{b2}y_{dbp}$$
$$\beta_s=\lambda_s g_{b1}y_{b2}+\lambda_{bi}g_{b2}y_{sbp}$$
$$\beta_b=\lambda_{bi}\left(y_{b1}y_{b2}-g_{b2}g_{b2}\right)$$

We obtain:

$$V_{b1}=\frac{\beta_g V_g+\beta_d V_d+\beta_s V_s}{\beta_b} \qquad \text{(D-11)}$$

Finally substituting (D-11) in (D-4) and we deduce:

$$V_{b2}=\frac{1}{y_{b2}\beta_b}\left(\ g_{b2}\beta_g V_g+\left(g_{b2}\beta_d+\beta_b y_{dbp}\right)V_d+\left(g_{b2}\beta_s+\beta_b y_{sbp}\right)V_s\right) \qquad \text{(D-12)}$$

To obtain the Y parameter model of substrate network, we should calculate the currents from transistor nodes. From Fig. II-33 we have:

$$I_d=I_{db}+I_{dbi}=y_{dbp}\left(V_d-V_{b2}\right)+y_{dbi}\left(V_d-V_{bi}\right)$$
$$I_s=I_{sb}+I_{sbi}=y_{sbp}\left(V_s-V_{b2}\right)+y_{sbi}\left(V_s-V_{bi}\right) \qquad \text{(D-13)}$$
$$I_g=I_{gb}+I_{gbi}=y_{gbp}\left(V_g-V_{b1}\right)+y_{gbi}\left(V_g-V_{bi}\right)$$

Substituting V_{bi}, V_{b1} and V_{b2} from (D-10), (D-11) and (D-12) we obtain:

$$I_d=\begin{pmatrix} y_{dbp}\dfrac{y_{b2}\beta_b-g_{b2}\beta_d-\beta_b y_{dbp}}{y_{b2}\beta_b} \\ +\,y_{dbi}\left(1-\dfrac{\lambda_d}{\lambda_{bi}}\right)\end{pmatrix}V_d+\begin{pmatrix} -\,y_{dbp}\dfrac{g_{b2}\beta_s+\beta_b y_{sbp}}{y_{b2}\beta_b} \\ -\,y_{dbi}\dfrac{\lambda_s}{\lambda_{bi}}\end{pmatrix}V_s+\begin{pmatrix} -\dfrac{y_{dbp}g_{b2}\beta_g}{y_{b2}\beta_b} \\ -\,y_{dbi}\dfrac{\lambda_g}{\lambda_{bi}}\end{pmatrix}V_g$$

$$I_s = \begin{pmatrix} -y_{sbp}\dfrac{g_{b2}\beta_d + \beta_b y_{dbp}}{y_{b2}\beta_b} \\ -y_{sbi}\dfrac{\lambda_d}{\lambda_{bi}} \end{pmatrix} V_d + \begin{pmatrix} y_{sbp}\dfrac{y_{b2}\beta_b - g_{b2}\beta_s - \beta_b y_{sbp}}{y_{b2}\beta_b} \\ +y_{sbi}\left(1-\dfrac{\lambda_s}{\lambda_{bi}}\right) \end{pmatrix} V_s + \begin{pmatrix} -\dfrac{y_{sbp}g_{b2}\beta_g}{y_{b2}\beta_b} \\ -y_{sbi}\dfrac{\lambda_g}{\lambda_{bi}} \end{pmatrix} V_g$$

$$I_g = \begin{pmatrix} -y_{gbp}\dfrac{\beta_d}{\beta_b} \\ -y_{gbi}\dfrac{\lambda_d}{\lambda_{bi}} \end{pmatrix} V_d + \begin{pmatrix} -y_{gbp}\dfrac{\beta_s}{\beta_b} \\ -y_{gbi}\dfrac{\lambda_s}{\lambda_{bi}} \end{pmatrix} V_s + \begin{pmatrix} y_{gbp}\dfrac{\beta_b - \beta_g}{\beta_b} \\ +y_{gbi}\left(1-\dfrac{\lambda_g}{\lambda_{bi}}\right) \end{pmatrix} V_g \qquad \text{(D-14)}$$

On the other hand we have:

$$\begin{aligned} I_d &= +y'_{dd}V_d - y'_{ds}V_s - y'_{dg}V_g \\ I_s &= -y'_{sd}V_d + y'_{ss}V_s - y'_{sg}V_g \\ I_g &= -y'_{gd}V_d - y'_{gs}V_s + y'_{gg}V_g \end{aligned} \qquad \text{(D-15)}$$

So we conclude:

$$y'_{dd} = y_{dbp}\frac{y_{b2}\beta_b - g_{b2}\beta_d - \beta_b y_{dbp}}{y_{b2}\beta_b} + y_{dbi}\left(1-\frac{\lambda_d}{\lambda_{bi}}\right)$$

$$y'_{ds} = y_{dbp}\frac{g_{b2}\beta_s + \beta_b y_{sbp}}{y_{b2}\beta_b} + y_{dbi}\frac{\lambda_s}{\lambda_{bi}}$$

$$y'_{dg} = y_{dbp}\frac{g_{b2}\beta_g}{y_{b2}\beta_b} + y_{dbi}\frac{\lambda_g}{\lambda_{bi}}$$

$$y'_{sd} = y_{sbp}\frac{g_{b2}\beta_d + \beta_b y_{dbp}}{y_{b2}\beta_b} + y_{sbi}\frac{\lambda_d}{\lambda_{bi}}$$

$$y'_{ss} = y_{sbp}\frac{y_{b2}\beta_b - g_{b2}\beta_s - \beta_b y_{sbp}}{y_{b2}\beta_b} + y_{sbi}\left(1-\frac{\lambda_s}{\lambda_{bi}}\right)$$

$$y'_{sg} = y_{sbp}\frac{g_{b2}\beta_g}{y_{b2}\beta_b} + y_{sbi}\frac{\lambda_g}{\lambda_{bi}}$$

$$y'_{gd} = y_{gbp}\frac{\beta_d}{\beta_b} + y_{gbi}\frac{\lambda_d}{\lambda_{bi}}$$

$$y'_{gs} = y_{gbp}\frac{\beta_s}{\beta_b} + y_{gbi}\frac{\lambda_s}{\lambda_{bi}} \qquad \text{(D-16)}$$

$$y'_{gg} = y_{gbp}\frac{\beta_b - \beta_g}{\beta_b} + y_{gbi}\left(1-\frac{\lambda_g}{\lambda_{bi}}\right)$$

And finally for the equivalent circuit we have:

$$\begin{aligned} y'_d &= y'_s = y'_{dd} - y'_{ds} - y'_{dg} \\ y'_g &= y'_{gg} - 2y'_{dg} \end{aligned} \qquad \text{(D-17)}$$