Technique de BIST pour synthétiseurs de fréquence RF

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BIST Technique for RF PLLs

Anna Asquini

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List of Acronyms

ALC	Automatic Level Control
AM	Amplitude Modulation
AMS	Analog Mixed-Signal
ATPG	Automatic Test Pattern Generation
BICS	Built-In Current Sensor
BIST	Built-In Self Test
CAT	Computer Aided Test
CDF	Cumulative Distribution Function
CEA	Commissariat à l'Energie Atomique
CFC	Catastrophic Fault Coverage
CIFRE	Conventions Industrielles de Formation par la REcherche
CP	Charge Pump
D-FF	D-type Flip-Flop
DfT	Design-for-Testability
DUT	Device Under Test
FM	Frequency Modulation
GEV	General Extreme Value
IC	Integrated Circuit
IP	Intellectual-Property
JTAG	Joint Test Action Group
KDE	Kernel-based Density Estimation
LETI	Laboratoire d'Electronique et des Technologies de l'Information
LF	Loop Filter
LO	Local Oscillator
LP	Low Power

LPF	Low-Pass Filter
NP	Non-Parametric
OTA	Operational Transconductance Amplifier
PDF	Probability Density Function
PFD	Phase-Frequency Detector
PLL	Phase-Locked Loop
PM	Phase Modulation
ppm	part-per-million
RF	Radio-Frequency
RMS	Root Mean Square
SiP	System in Package
SoC	System on Chip
SUT	Signal Under Test
TIMA	Techniques de l'Information et de la Microélectronique pour l'Architecture des systèmes intégrés
UI	Unit Interval
VCO	Voltage-Controlled Oscillator
VDL	Vernier Delay Line
VLSI	Very Large Scale Integration

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Chapter I

Introduction

1.1 Motivation

System on chip (SoC) and system in package (SiP) devices allow integrating more and more functionalities on the same integrated circuit (IC). These systems find a major application in the telecommunication domain and very-large-scale-integration (VLSI) manufacturing makes them cheaper in mass production. Most of the blocks of these devices are digital blocks and memories, analog and mixed-signal radio frequency (RF) blocks make up only a small part of a total SoC. However, test time and resources related to analog, mixed-signal and RF components represents the greatest contribution to the total test of SoCs. The classical test approaches are becoming not viable for many reasons that will be discussed further on, thus new techniques must be conceived and validated. Structural test for digital components together with built-in self test (BIST) techniques for memories are nowadays widely employed by semiconductor manufacturers. BIST techniques in digital domain are based on a wrapper technique. This means that the digital device is first designed and next a BIST circuit is applied over the device (seen as a black box) using only the available inputs and outputs. Solutions for mixed-signal and RF devices are much less developed, though. Moreover, BIST techniques in the mixed-signal/RF domain may not be seen as simple wrappers. The test technique, be it a BIST or design for test (DfT) one, has to be thought at the design stage by designers, since it might impact the operation of the device to be tested. Nonetheless, on-chip testing for new generations of analog, mixed-signal and RF devices will one day replace measurement of specifications on tester that are becoming

too costly or impossible to carry out. On-chip measurements must be transparent to device under test (DUT) operation-mode and highly correlated to specifications. They shall help to reduce test time and resources for production test while maintaining standard quality.

1.2 Goals

This thesis has an industrial basis, thus its aim is the development of analog and mixed-signal/RF on-chip BIST techniques in order to build a set of strategies available for designers to implement according to specific needs. The different BIST blocks for analog, mixed-signal and RF testing should come in form of libraries to designers' advantage. This work is brought forth in collaboration between TIMA laboratory and STMicroelectronics. The validation of a BIST technique for production testing will be based on simulations of defects that may be encountered during silicon fabrication.

The approach has been to demonstrate the applicability of a BIST technique to a complex case-study. The devices that have been taken as case-study are a phase-locked loop (PLL) and its voltage controlled oscillator (VCO) considered on its own (not inserted in the PLL). Both devices are designed and manufactured in STMicroelectronics 65 nm RF LP technology. PLLs are, in fact, mixed-signal blocks used in most mixed-signal and digital applications mainly for frequency synthesis, clock and data recovery, and on-chip clock distribution purposes. Sometimes it is not obvious to think of a PLL as a mixed-signal device since it has a purely digital input and output. Some of its building blocks though are analog, which yields non-deterministic test responses. These building blocks require the same test approach as any other analog device. Nevertheless, testing a PLL on a digital or analog mixed-signal tester is complicated since it requires a very high measurement precision which is time consuming for test purposes. This is the reason why generally PLLs are tested only verifying their lock state, which is not at all sufficient to assure the lock range and the adequate stability in all conditions. PLLs are sensitive to parametric deviations or process defects that may cause them to be malfunctioning. Faults in a PLL can impact

most of the performances of the total SoC, thus, testing the PLL before any other device may be a good start to the whole SoC testing [1]. RF PLL specifications are critical, mostly when these circuits are embedded in high speed digital communication systems. The most significant specifications are given mainly for output duty cycle, output frequency, current consumption, output power, VCO gain, VCO free running frequency, lock and capture range, lock and capture time, phase margin, bandwidth (strongly related to settling time), and for jitter (spectral purity and phase noise).

The choice of an RF PLL as case-study has been made considering that the majority of the new generation of SoCs need internal signals with tunable, stable, and accurate frequency. This is also why PLLs are the most used IPs in STMicroelectronics CMOS 90 nm down to 65 nm products. Yet BIST techniques for RF PLLs are still developed in a very ad-hoc, and sometimes rudimental way, if developed at all. In STMicroelectronics (as in other semiconductor companies in general) there are no universal libraries from which to pick the most suitable BIST block for a specific RF PLL implementation. Moreover, although PLLs are very widespread and crucial IPs on the market, the number of specifications that are actually tested in production is incomplete, sometimes limited to the lock state alone, due to the reduced tester resources to perform low-cost at-speed tests. BIST techniques are thus the only possibility to remain competitive on the market for these kinds of IPs in the future.

A set of on-chip test measures has to be chosen for the DUT. Limits on these test measures must be set in order to appropriately design the embedded monitors making up the BIST technique so as to be robust in the range of operation. Once the limits are set, a first evaluation of the test measures may be carried out. In fact, these limits are set considering process deviations, so that the BIST limits result in a tradeoff between yield loss (rejection of good circuits) and defect level (acceptance of bad circuits). A statistical model of the DUT is necessary to set these limits. Once test limits are set, fault coverage is evaluated for injected faults.

1.3 Hosting Facilities

In this section, a concise description of how and where this Ph.D. thesis took place is presented. This Ph.D. has been financed by a French CIFRE (Conventions Industrielles de Formation par la REcherche) scholarship. The work has been carried out during 50 % of the time in the TIMA Laboratory and the remaining 50 % of the time at STMicroelectronics (Crolles 1 site). Apart from wafer production, the STMicroelectronics Crolles 1 also hosts several R&D teams, including the teams which design and test mixed-signal/RF devices, and the team which develops the associated BIST techniques. Most of the industrial collaboration took place between an RF design team and the AMS BIST team, in particular at Minatec (CEA) research pole in Grenoble hosting the RF design team from STMicroelectronics. A contribution to the Ph.D. work also came from collaboration with the LETI laboratory, also based in Minatec and with strong relationships with STMicroelectronics R&D.

1.4 Contributions

This Ph.D. has the aim to be the first step towards building a set of universal BIST solutions to be applied to frequency synthesizers, according to their operating conditions and to the required specifications (operating frequency, power consumption, area overhead, defect level, yield loss, fault coverage, etc.).

One of the three BIST monitors analyzed in this Ph.D, here named PFD monitor, is completely original and never proposed in the literature. A patent application was proposed to STMicroelectronics for this particular test solution, but it has not been accepted since it was impossible to ascertain if competitors were using the PFD monitor without paying royalties to STMicroelectronics (impossible to apply reverse engineering due to its small surface occupation).

Moreover, the method used to validate the BIST monitors on the PLL used as case-study is not only based on catastrophic fault coverage, as most BIST techniques in the literature are evaluated up to now, but also on parametric test metrics such as yield loss

and defect level. To evaluate these test metrics, a large population of devices is needed. A completely innovative method developed at TIMA laboratory to build a large statistical model has been employed for the first time on an industrial device in this work.

1.5 Document Overview

This document is organized as follows. Chapter II presents the essentials on PLL theory. The structure of a PLL and its operation mode are detailed, and an overview is also given on the way of simulating it. Existing test strategies and the state of the art on DfT and BIST techniques for PLLs, most of which consider jitter measurements but also some others based on non jitter-based techniques, are next discussed in Chapter III. The approach for test metrics evaluation considered in this work is also discussed in this chapter. The generation of a statistical model of the DUT in order to evaluate the test metrics of the BIST technique is discussed in Chapter IV. Here, the PLL case-study is also presented. Next, in Chapter V the BIST technique, thus the BIST monitors proposed in this thesis, will be described and motivated. Validation of the BIST technique by simulation of the DUTs will be discussed in Chapter VI. In Chapter VII conclusions and some suggestions on further research directions will be given.

Some appendixes are also present at the end of this manuscript dealing with more specific theoretical topics mentioned in the manuscript for the reader's interest.

Chapter II

Phase-Locked Loops

Frequency synthesis and phase locking are concepts that exist since the thirties. Their implementation in different technologies and for different applications though, is continuously evolving, challenging designers more and more. PLLs are mixed-signal devices employed in different analog and digital applications, consequently they are considered to be a fundamental component of microelectronic systems. They are mainly employed for clock synchronization and recovery, frequency synthesis (multiplication and division) for channel tuning in television and wireless communication systems, and also for frequency modulation and demodulation. Thus, they can be found in microprocessors and in mixed-signal ICs for communication applications.

This chapter provides a review of the basic PLL theory, building blocks, behavior, specifications, and also some helpful formulas will be given in order to better understand the issues faced for testing purposes.

2.1 PLL Building Blocks and Operation Mode

The main purpose of a PLL is to compare the output phase with the input phase. The comparison is performed by the phase detector (PD) or phase-frequency detector (PFD). As represented in Fig. II-1, the PFD is followed by the charge pump (CP) which has at its output a voltage whose average is proportional to the phase difference between the two input signals. This average voltage value is evaluated by a low pass filter (LPF), called the loop filter (LF) in a PLL, and is used to drive the VCO. One of the PFD input

signals is the reference frequency f_{ref}, while the other (f_{loop} or f_{vco}/N) comes from the frequency divider (divider-by-N) that follows the VCO. The feedback behavior of a PLL allows the output of the VCO to be synchronized with the reference frequency. If the two signals f_{ref} and f_{loop} are skewed (which means they are not phase aligned), the only possible way to achieve the phase lock condition for the PLL is to vary the frequency at the VCO output by varying the input average voltage value (V_{tune}) of the VCO. Once the phase is aligned, V_{tune} may go back to its original value in order to regain the original frequency oscillation which makes f_{ref} and f_{loop} two signals with same frequency and phase aligned. Once this condition is reached, phase lock is achieved.

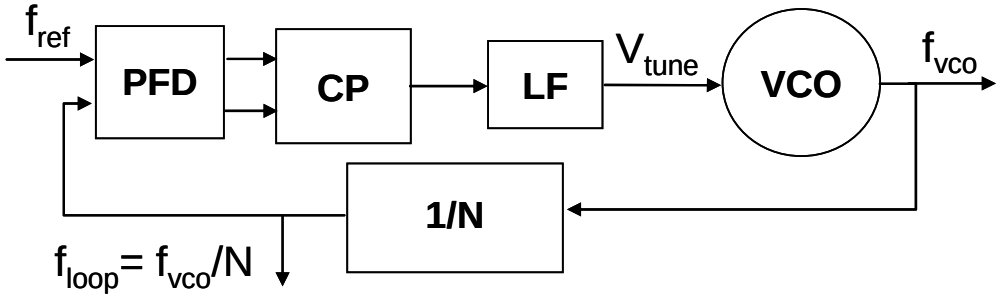


Fig. II-1. PLL basic architecture

Supposing now that a specific application requires several clocks with a precise phase spacing among them, a variant of a PLL, called delay-locked loop (DLL), is employed instead. DLLs are sometimes referred to as digital-locked loops because the VCO structure is all digital and is simply made up of a delay chain. They normally lack the CP block as shown in Fig. II-2. This configuration makes them loose all the mixed-signal essence which is typical of PLLs.

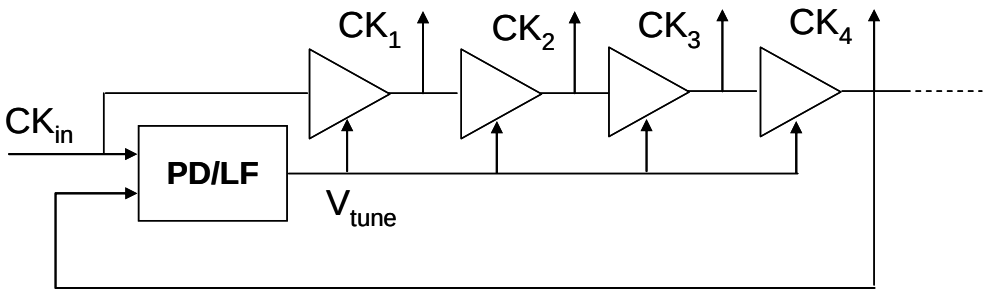


Fig. II-2. Delay-locked loop

Next, a more detailed description of the functionality of the single blocks making up a PLL will be given together with its overall operation principle.

2.1.1 Phase Frequency Detector and Charge Pump

The principle of operation of a phase detector (PD) is graphically explained in Fig. II-3. In this figure, it is clear that the average output $\overline{V_{out}}$ is linearly proportional to the phase difference $\Delta\phi$ between its two inputs.

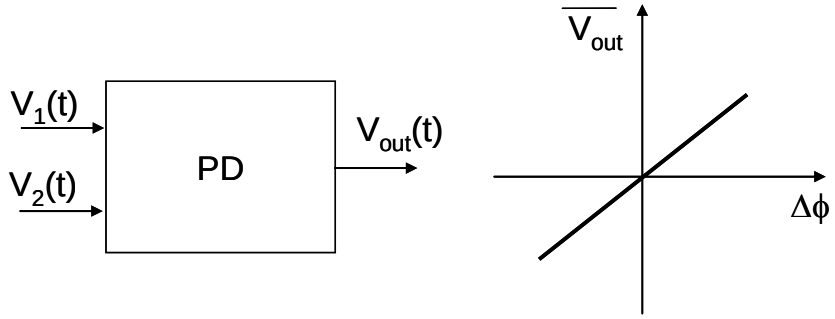


Fig. II-3. Definition of phase detector

There are different types of phase detectors the choice of which will impact several performances of the PLL, such as for example the lock range, the noise and the spurious signals (see section 2.3 for details). The most commonly used phase detectors are the double-balanced mixer (digital, square wave driven, XOR type), the sequential phase-frequency detector (PFD), and the sample-and-hold phase detector. The last two detectors are edge-trigged, therefore, they do not require 50 % duty cycle input signals. Here, only sequential PFDs will be discussed since they have several advantages over the other types, although they are more challenging for designers. In practice, sequential PFDs have a minimal spurious contribution compared to the other two, since they only deliver the amount of energy necessary to compensate for mismatch and leakage currents (see section 2.2.2), thus they are only active during a small fraction of the reference period. They detect both phase and frequency differences and are commonly

combined to CPs to simplify the interfacing to the LF. As depicted in Fig. II-4, the PFD employs sequential logic to create three states and respond to the rising/falling edges of the inputs. When the rising (in this example) edges of the input signals arrive simultaneously, the *UP* and *DOWN* signals become active at the same time. Immediately, the AND gate reacts by generating the *reset* signal for the D-FFs, deactivating the *UP* and *DOWN* signals. I_{out} therefore remains at zero value, ideally, avoiding spectral purity degradation of the VCO. This situation is called in-lock. In non ideal conditions, *UP*, *DOWN* and *reset* signals do have a minimum width also when the PLL is locked. The frequency jump situation depicted in Fig. II-4 happens when f_{loop} becomes lower than f_{ref} (in this example) or vice versa. When the rising edge of f_{ref} arrives earlier than the one of f_{loop} the *UP* signal is activated and will remain active until the next rising edge of f_{ref}. The CP output current, I_{out}, serves to build up a VCO control voltage which will bring the frequency and phase of f_{loop} to match those of f_{ref}.

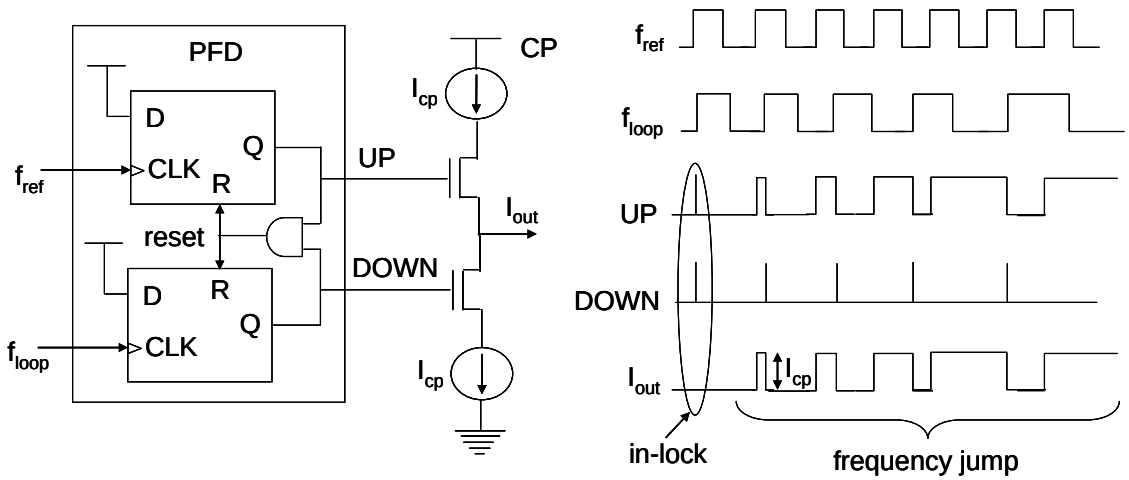


Fig. II-4. Conceptual operation of a PFD combined with a CP

Unfortunately, many CP circuits suffer of a dead-zone in their charge pump currents (section 2.2.4), which results in a degraded spectral purity, which translates in jitter, once the PLL is (almost) in lock. This will be better explored in section 2.3.2.

The duty-cycle of I_{out} and UP signals grows linearly with the phase difference $\Delta\phi$ between the two input signals. The relationship between the average value of I_{out} and $\Delta\phi$ can therefore be written as:

$$\overline{I_{out}} = I_{cp}\frac{\Delta\phi}{2\pi} \tag{II-1}$$

The gain K_{pd} of the PFD/CP block, defined as the average I_{out} for a given $\Delta\phi$, can thus be expressed as:

$$K_{pd} = \frac{\overline{I_{out}}}{\Delta\phi} = \frac{I_{cp}}{2\pi} \quad [\text{A/rad}] \tag{II-2}$$

2.1.2 Loop Filter

Through an integration operation on I_{out}, the LF (which is a low pass filter) provides the current to voltage conversion necessary for the interconnection of the CP to the VCO. The purity of the tuning voltage determines the spectral purity of the VCO output. In the ideal in-lock condition $I_{out} = 0$ and there is no degradation of spectral purity, but this would require a LF with infinite DC gain. A simple capacitor would be enough for integration, but this would bring instability in the loop and thus an oscillatory behavior, thus a resistance is often placed in series with the integrator capacitor. This adds a zero in the transimpedance function $Z_f(s)$ of the LF. The RC combination is the simplest LF topology that allows a stable PLL output signal. Unfortunately, DC leakage currents are very often present in tuning lines of PLLs and since they are proportional to duty-cycle of I_{out}, the latter increases. As Equation (II-12) will show, this will cause the presence of undesired components converted by the LF in the tuning voltage. This is why the minimum configuration of a LF in practice also includes a capacitor in parallel to the RC (or to the R only, depending on the configuration), as shown in Fig. II-5. The purpose of this extra capacitor is to decrease the LF transimpedance at higher frequencies, decreasing the ripple of the tuning voltage (see Equation (II-12)). The difference between the two configurations is basically that LF_2 is preferable for full

integration as the bottom plates of the capacitors are both grounded, eliminating substrate noise coupling into the output node of the filter. This will result in a cleaner V_{tune} and minimized phase noise degradation due to substrate noise. The transimpedance of the LF may be generally written as:

$$Z_f(s) = \frac{k}{s}\frac{1+s\tau_2}{1+s\tau_3} = \frac{k}{s}\frac{1+s\tau_2}{1+\frac{s\tau_2}{b}} \tag{II-3}$$

where k is a gain factor dependent of the specific LF configuration, τ_2 is the time constant of the stabilizing zero, τ_3 is the time constant of the pole which attenuates reference frequency and its harmonics, and b is the ratio of the time constants τ_2/τ_3. Tab. II-1 reports the relationships among parameters and the transimpedances of the two passive LF depicted in Fig. II-5.

Active loop filters will not be thoroughly discussed in this context, but they do exist and are essentially employed when the CP cannot directly provide the required output voltage range (e.g. wide tuning range applications such as terrestrial TV and satellite reception). It is important to remember that these kinds of LF increase complexity and power dissipation of the circuit introducing noise sources in the loop as well [11].

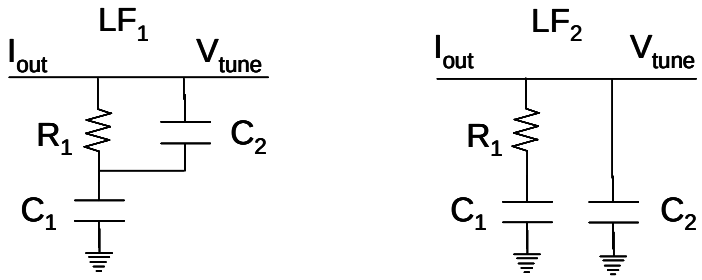


Fig. II-5. Passive LF topologies

The order of the PLL, indicating the number of poles in its transfer function, is always one order greater than the loop filter, since the VCO introduces one extra pole to the ones of the LF transfer function, as explained in the following section.

Parameter	LF1	LF2
τ_2	$R_1(C_1+C_2)$	R_1C_1
τ_3	R_1C_2	$R_1\frac{C_1C_2}{(C_1+C_2)}$
k	$\frac{1}{C_1}$	$\frac{b-1}{b}\frac{1}{C_1}$
b	$1+\frac{C_1}{C_2}$	$1+\frac{C_1}{C_2}$
$Z_f(s)$	$\frac{1+s[R_1(C_1+C_2)]}{sC_1(1+sR_1C_2)}$	$\frac{1+sR_1C_1}{s(C_1+C_2)\left(1+sR_1\frac{C_1C_2}{C_1+C_2}\right)}$

Tab. II-1. Relationships among LF design parameters

2.1.3 Voltage Controlled Oscillator

The output signal of the whole PLL system issues from the VCO. The relation between the frequency of the VCO output signal f_{out} and the tuning voltage at its input V_{tune} is:

$$f_{out} = f\big|_{V_{tune}=0} + K_{vco}(V_{tune})\cdot V_{tune} \qquad \text{(II-4)}$$

where $f\big|_{V_{tune}=0}$ is the output frequency for $V_{tune} = 0$, the so called free running frequency. VCOs may be of essentially two types: ring oscillators, made up of an inverter chain with a number of odd elements as represented in Fig. II-6 (a), or an LC tank represented in Fig. II-6 (b). The problem of VCO frequency covering the whole tuning range of the PLL is common to both VCO configurations, each solves the issue of dividing the tuning range into several frequency bands in a different way. The ring oscillator has selectable numbers of inverters making up the chain to change the oscillation frequency; the LC tank is equipped of a varactor, which consists in multiple capacitors in parallel that will affect the oscillation frequency, each of which is activated by a controlled switch.

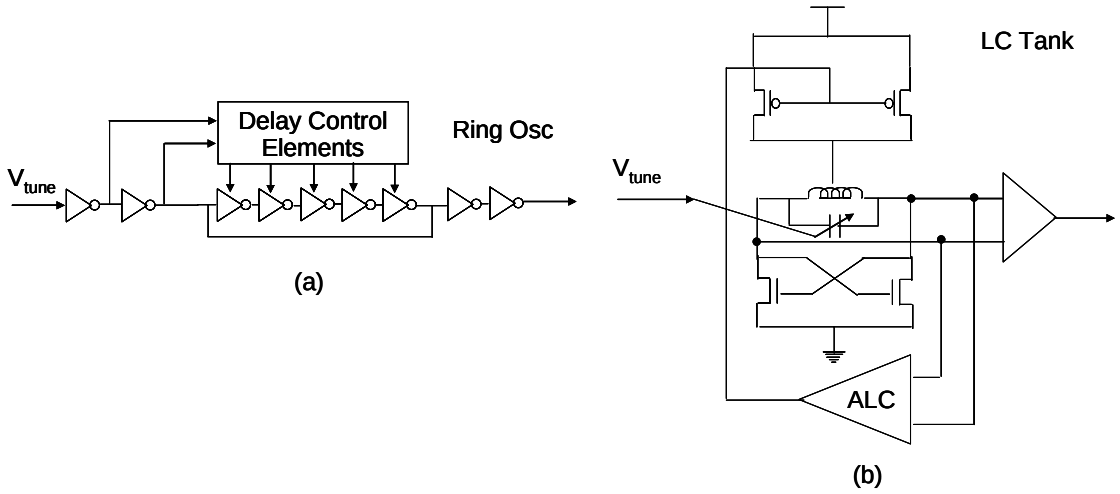


Fig. II-6. (a) Ring oscillator and (b) LC tank oscillator with automatic level control (ALC)

The relationship between the phase of VCO output signal ϕ_{vco}, and the tuning voltage V_{tune}, is of interest to understand the integration characteristic of the VCO [11]:

$$\phi_{vco}(t) = \int 2\pi f_{out}\,dt = \int 2\pi\left(f\big|_{V_{tune}=0} + K_{vco}(V_{tune})\cdot V_{tune}(t)\right)dt \tag{II-5}$$

The free running frequency $f\big|_{V_{tune}=0}$ does not depend on V_{tune} and does not influence the phase so that Equation (II-5) may be written as:

$$\phi_{vco}(t) = \int 2\pi K_{vco}(V_{tune})\cdot V_{tune}(t)\,dt \tag{II-6}$$

When in lock state, V_{tune} may be considered constant, so the dependency of K_{vco} from V_{tune} may be neglected. In the Laplace domain, Equation (II-6) becomes:

$$\phi_{vco}(s) = \frac{2\pi K_{vco} V_{tune}(s)}{s} \tag{II-7}$$

2.1.4 Frequency Divider

There are two different types of division possible in a PLL. One consists in an integer division by N and another in a fractional division by N/M if a non integer multiple of

the reference frequency is required. In this work the integer division by N is detailed, the fractional one introducing no substantial difference. The divider by N is a digital circuit responsible for frequency scaling in the loop. Only PLLs with frequency synthesis purposes require this block in order to assure that f_{loop} is equal to f_{ref} at the PFD input. Not only it scales the frequency, but it is also in charge of putting in square wave form f_{loop} in order to make it coherent with the PFD input. The division factor N is an integer number. The effect of division on the phase shift between input and output is given by the relation:

$$\phi_{loop}(t) = \frac{2\pi f_{vco}}{N} t + \frac{\Delta\phi_p}{N} \sin 2\pi f_m t = \frac{\phi_{vco}(t)}{N} \tag{II-8}$$

the demonstration of which may be found in [11], and where $\Delta\phi_p$ is the peak phase deviation and f_m is the modulation frequency. This means that the modulation frequency is not affected by the division by N and that the transfer function $\phi_{loop}(t)/\phi_{vco}(t)$ of the frequency divider is simply a gain factor with value 1/N.

2.2 PLL Non-Idealities

Let us next explore several types of PLL non-idealities in order to understand the main malfunctioning causes and where they may come from.

2.2.1 Spectral Spurs due to Charge Pump Leakage and Mismatch

The spectral components of I_{out} as a function of the phase difference $\Delta\phi$ will be calculated since they are an important step to understand some BIST techniques presented in Chapter III. Let us first assume that there is no mismatch in the CP currents and thus that the I_{up} and I_{down} of the CP have the same amplitude I_{cp} (as in Fig. II-4). The duty-cycle of I_{out} is equal to $\Delta\phi/2\pi$ and can also be expressed as τ/T_{ref}, where τ is the active time of I_{out} and T_{ref} is the period of the reference signal. The Fourier series development of a periodic train of pulses of amplitude I_{cp} and duration τ is:

$$I_{out}(t) = I_{cp}\frac{\tau}{T_{ref}}\left[1 + 2\sum_{n=1}^{\infty}\frac{\sin\left(n\pi\frac{\tau}{T_{ref}}\right)}{n\pi\frac{\tau}{T_{ref}}}\cos\frac{2\pi nt}{T_{ref}}\right] \quad \text{(II-9)}$$

or as a function of $\Delta\phi$ and considering small values of duty-cycle $\tau/T_{ref} = \Delta\phi/2\pi$ for which the *sinc* function ([*sin(x)*]/*x*) can be approximated as unity:

$$I_{out}(t) \approx I_{cp}\frac{\Delta\phi}{2\pi}\left[1 + 2\sum_{n=1}^{\infty}\cos\left(2\pi n f_{ref} t\right)\right] \quad \text{(II-10)}$$

which shows that the amplitude of the spectral components of I_{out} is constant and twice as large as the DC value $I_{cp}\Delta\phi/2\pi$. Therefore, if duty-cycle equals to zero (PLL in lock state), the CP output theoretically contains no DC or AC signal components whatsoever.

In presence of leakages and mismatches the duty-cycle is never equal to zero, introducing spectral degradation. When in lock condition, the phase difference $\Delta\phi$ satisfies the condition $\overline{I_{out}} = I_{lm}$, where I_{lm} stands for the leakage and/or mismatch currents. Duty-cycle in presence of leakages and mismatch may therefore be written as I_{lm}/I_{cp}, since it is equal to $\overline{I_{out}} / I_{cp}$. In Equation (II-10) duty-cycle was expressed as $\Delta\phi/2\pi$. Inserting this last expression in presence of mismatch and leakages, the spectral components of I_{out} as a function of $\Delta\phi$ may be rewritten as:

$$I_{out}(t) = I_{lm}\left[1 + 2\sum_{n=1}^{\infty}\cos\left(2\pi n f_{ref} t\right)\right] \quad \text{(II-11)}$$

from which two important conclusions may be derived:

a) the amplitude of the spectral components of I_{out} is twice the value of the DC leakage and/or mismatch currents I_{lm},

b) the amplitude is not dependent on the nominal CP current I_{cp} unless leakage current depends on I_{cp} itself (e.g. if the CP is main source of leakage and its impedance is a function of I_{cp}).

The next important step is to link the leakage and/or mismatch current to the magnitude of the spurious components at the VCO output. This will allow later on relating leakages and mismatch currents to PLL specifications for BIST purposes. The peak frequency deviation is the product of the magnitude of the spectral components $V_{rip}(nf_{ref})$ of the ripple voltage at the tuning line (VCO input) with the VCO gain K_{vco}. Referring to Equation (II-11):

$$V_{rip}\left(nf_{ref}\right) = 2I_{lm}\left|Z_f\left(j2\pi nf_{ref}\right)\right| \tag{II-12}$$

with n ranging from 1 to ∞ and $\left|Z_f\left(j2\pi nf_{ref}\right)\right|$ the magnitude of the transimpedance function of the LF at the corresponding frequency. The peak phase deviation $\Delta\phi_p(nf_{ref})$ due to each of the frequency components nf_{ref} of the ripple voltage can be written as:

$$\Delta\phi_p\left(nf_{ref}\right) = \frac{\Delta f_p\left(nf_{ref}\right)}{nf_{ref}} = \frac{V_{rip}\left(nf_{ref}\right)K_{vco}}{nf_{ref}} = \frac{2I_{lm}\left|Z_f\left(j2\pi nf_{ref}\right)\right|K_{vco}}{nf_{ref}} \tag{II-13}$$

which derives from the standard modulation theory, for which the relationship between peak phase deviation $\Delta\phi_p(f_m)$, peak frequency deviation $\Delta f_p(f_m)$, and the modulation frequency f_m is given by:

$$\Delta\phi_p\left(f_m\right) = \frac{\Delta f_p\left(f_m\right)}{f_m} \tag{II-14}$$

Each of the baseband modulation frequencies nf_{ref} generates two RF spurious signals which are located at offset frequencies $\pm nf_{ref}$ from the carrier frequency f_{LO} (where LO in subscript stands for local oscillator).

The amplitude of each spurious signal A_{sp} is related to the magnitude of the carrier A_{LO} and to the peak phase deviation $\Delta\phi_p$ by:

$$A_{sp}\left(f_{LO} \pm nf_{ref}\right) = A_{LO}\frac{\Delta\phi_p\left(nf_{ref}\right)}{2} = A_{LO}\frac{I_{lm}\left|Z_f\left(j2\pi nf_{ref}\right)\right|K_{vco}}{nf_{ref}} \qquad \text{(II-15)}$$

Dividing by A_{LO} and expressing this Equation in decibels with respect to the carrier (*dBc*) as it is common to express the magnitude of undesired signal components:

$$\left.\frac{A_{sp}\left(f_{LO} \pm nf_{ref}\right)}{A_{LO}}\right|_{dBc} = 20\log\frac{\Delta\phi_p\left(nf_{ref}\right)}{2} = 20\log\frac{I_{lm}\left|Z_f\left(j2\pi nf_{ref}\right)\right|K_{vco}}{nf_{ref}} \quad [dBc] \qquad \text{(II-16)}$$

From Equation (II-16), it can be concluded that the relative amplitude of the spurious signals is not dependent on the absolute value of the loop bandwidth or on the nominal CP current I_{cp}. Spurious signals are instead determined by the transimpedance of the LF, by the magnitude of the leakage and mismatch currents, by the VCO gain, and by the value of the reference frequency. As stated before, theoretically, if $I_{lm} = 0$ there are no spurious reference breakthrough signals in the spectrum of the oscillator signal [11].

2.2.2 PLL Behavior Under CP Current Mismatch

In Fig. II-7 a non-ideal operation mode of a PLL is depicted. Non-idealities are generated in the CP, where it is actually difficult to design pmos and nmos current mirrors that give the exact same charging/discharging currents, with the result that I_{down} differs from I_{up} of a slight amount in amplitude. The difference between I_{down} and I_{up} is known as mismatch. This non-ideality in CP currents will not prevent the PLL from locking since the PLL is a closed-loop feedback device, capable of compensating non-idealities. In Fig. II-7 it may be seen how the nonideality in dotted arrows (mismatch on I_{down}) produces a reaction (bold arrows) in the whole PLL that will eventually allow the system to reach lock state. The PLL reaction is evident at the PFD output, where the *UP* signal lasts a bit longer than the *DOWN* signal in order to keep the average value of V_{tune} constant and the average value of the overall CP current, I_{out}, equal to zero, which guarantees lock state [12].

The equation that provides the rule for mismatch compensation is:

$$I_{up} * t_{up} = I_{down} * t_{down} \tag{II-17}$$

where t_{up} is the duration of I_{up} and t_{down} the duration of I_{down}. This plainly states that the area of the signals I_{up} and of I_{down} must be equal in order to obtain an average overall charge pump current I_{out} equal to zero.

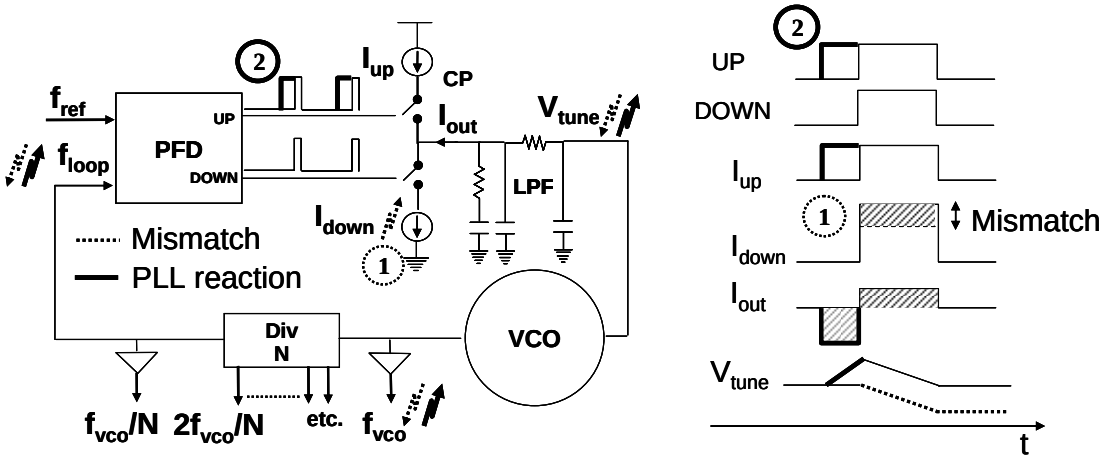


Fig. II-7. PLL operation under charge pump current mismatch

2.2.3 VCO Phase Noise

Ideally, a VCO produces a single frequency $\omega_0 = 1/\sqrt{LC}$. Its output has thus a frequency spectrum consisting of a line of zero width, as shown in Fig. II-8 (a). In practice, the frequency is modulated by noise: thermal, shot and flicker noise originating within the oscillator itself. This causes the spectrum to have some width, as shown in Fig. II-8 (b). The modulation by noise is inversely proportional to the quality factor $Q = r_p / \omega_0 L$, where r_p is the parallel loss resistance of the LC tank. So the spectral width decreases as Q increases. Recalling ideal Equation (II-7) and introducing the concept of phase noise in the VCO phase definition, yields:

$$\phi_{vco}(s) = \frac{2\pi K_{vco} V_{tune}(s)}{s} + \phi_n \tag{II-18}$$

where ϕ_n is the phase noise factor.

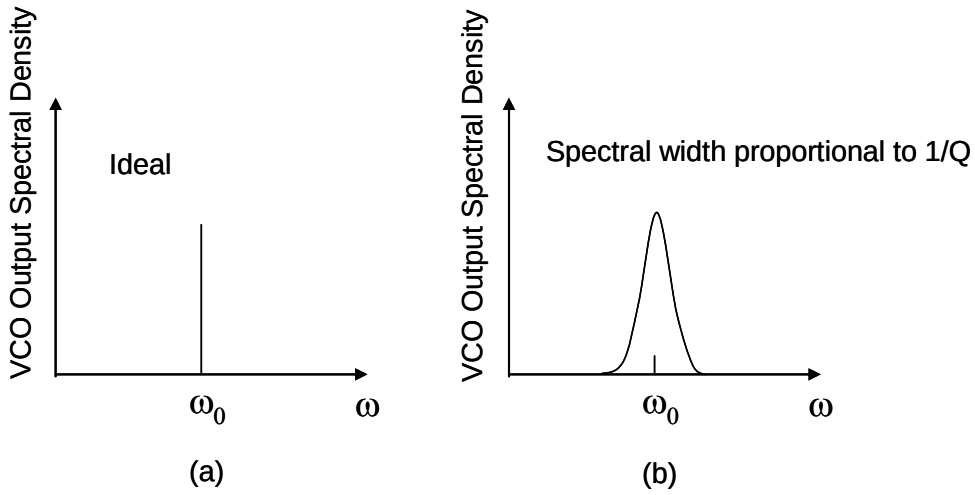


Fig. II-8. VCO output spectrum: (a) ideal and (b) with internal noise

Let the spectrum of the noise source $n(t)$ in the VCO be $\Phi_n(\omega_0 + \omega)$, where ω is the offset frequency from the carrier ω_0. In Φ_n thermal and shot noise contribute with a flat spectral density ($\omega > \omega_a$ in Fig. II-9 (a)), here referred to as N_0. Flicker noise instead, becomes dominant at frequencies close to ω_0 ($\omega < \omega_a$ in Fig. II-9 (a)), with a spectral density of $N_0\ \omega_a/\omega$. The frequency ω_a may not be calculated: it has to be measured, it is dependent on construction, materials, and environment of the VCO, but it is typically around $10^{-5} \cdot \omega_0$ [13]. In Fig. II-9 only half the spectrum is represented, being the portion for $\omega < 0$ symmetrical about ω_0. Applying the VCO equation whose proof may be found in [13], it is possible to relate the noise spectral density Φ_n to the VCO phase spectral density Φ_ϕ as follows:

$$\Phi_\phi(\omega) = \frac{2}{V^2}\Phi_n(\omega_0 - \omega) \tag{II-19}$$

where V is the VCO voltage oscillation amplitude. From Equation (II-19) and the above statements:

$$\Phi_\phi(\omega) = \Phi_0 \frac{\omega_a}{\omega}; \qquad \omega < \omega_a \tag{II-20}$$

$$\Phi_{\phi}(\omega) = \Phi_0; \qquad \omega > \omega_a \tag{II-21}$$

where $\Phi_0 = 2N_0/V^2$. Spectral components of $n(t)$ that fall into the spectral bandwidth ($\omega < \omega_b$) cause frequency modulation, where $\omega_b = \omega_0/2Q$ and corresponds to half the tank bandwidth. The VCO frequency deviation due to phase noise is $\omega_n \approx \omega_b \phi_{vco}$ (see [13] for proof). Being the phase modulation the integral of the frequency modulation, the VCO phase noise factor can then be written as $\phi_n(s) = \omega_n(s)/s$. Therefore, the corresponding spectral densities are related by:

$$\Phi_{\phi n}(\omega) = \frac{\Phi_{\omega n}}{\omega^2} \approx \frac{\omega_b^2}{\omega^2}\Phi_{\phi}; \qquad \omega < \omega_b \tag{II-22}$$

and substituting in Equations (II-20) and (II-21) yields:

$$\Phi_{\phi n}(\omega) = \Phi_0 \frac{\omega_a \omega_b^2}{\omega^3}; \qquad \omega < \omega_a \tag{II-23}$$

$$\Phi_{\phi n}(\omega) = \Phi_0 \frac{\omega_b^2}{\omega^2}; \qquad \omega_a < \omega < \omega_b \tag{II-24}$$

$$\Phi_{\phi n}(\omega) = \Phi_0; \qquad \omega > \omega_b \tag{II-25}$$

Thus $\Phi_{\phi n}$ may be divided in three regions, as depicted in Fig. II-9 (b).

The phase noise spectral density actually follows the Leeson formula:

$$\Phi_{\phi n}(\omega) = 10\log\left[\Phi_0\left(1+\frac{\omega_b^2}{\omega^2}\right)\left(1+\frac{\omega_a}{|\omega|}\right)\right] \tag{II-26}$$

The flat portion beyond ω_b does not extend forever, otherwise the phase noise would have an infinite power. In practice, the curve breaks at some cutoff frequency ω_c as in Fig. II-9 (b).

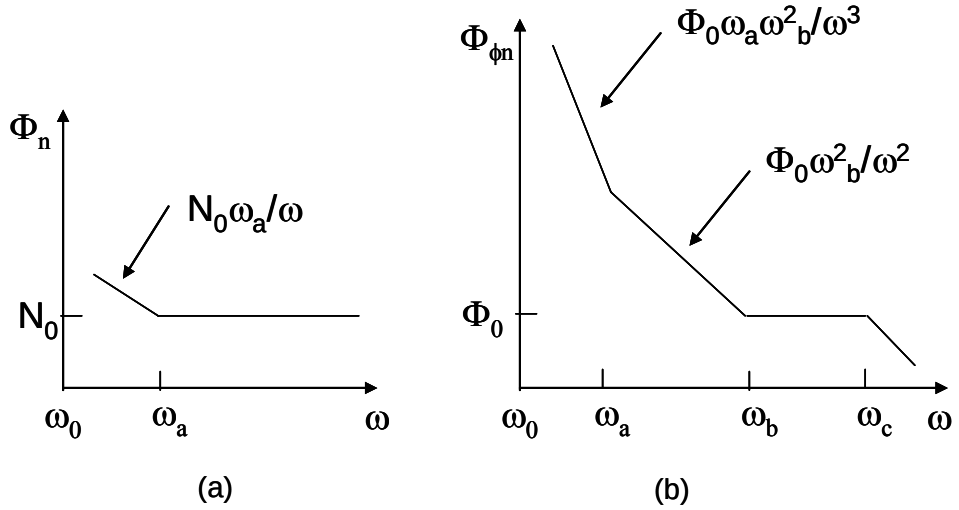


Fig. II-9. Spectral density (a) of noise source in the VCO (b) of VCO phase noise

2.2.4 Other Non-Idealities

PFD/CP imperfections may lead to a high rippled voltage control signal V_{tune}, although the PLL is in lock condition. This ripple modulates the VCO output frequency producing a non periodic output waveform. This effect comes from the non-ideality of the PFD output pulses discussed in section 2.2.2 where it has been stated that in non ideal conditions, *UP*, *DOWN* and *reset* signals have a minimum width (narrow pulse) also when the PLL is locked. This non-ideal behavior of the PFD would cause the dead-zone effect depicted in Fig. II-10. The dead-zone is due to the fact that the capacitance seen at the *UP* and *DOWN* nodes prevents the narrow pulses to reach the logic level 1 owing to the finite rise and fall times, failing to switch the CP on. Thus, if the $\Delta\phi$ falls below a certain value ϕ_0, the output voltage V_{tune} of the PFD/CP/LPF block is no longer a function of $\Delta\phi$. Since, for $|\Delta\phi| < \phi_0$ the CP injects no current, the loop gain drops to zero and the output phase is not locked. This temporary lack of corrective feedback allows the VCO to accumulate as much random phase error as ϕ_0 with respect to the input, which is a highly undesirable circumstance.

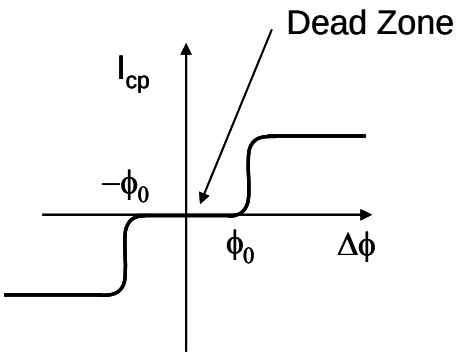


Fig. II-10. Dead-zone phenomenon

Some techniques to limit the dead-zone effect exist, but they tend to limit the maximum operation frequency as well. See Appendix 1 for more detail on very high frequency (VHF) PFD/CP architecture and design [11], [12].

Many other non-idealities (such as those due to different types of loop filters and the divider-by-N) and other different phenomena (such as output phase noise due to input noise) that translate in sources of jitter at the output signal of the PLL exist and are reported in the literature with detailed evaluation of each contribution to the noise budget. In this section, non-idealities of the digital blocks of a PLL have not been detailed since this Ph.D. work focuses mainly on mixed-signal RF blocks of a PLL. Further details on this topic can be found in [11], [13].

2.3 PLL Performances

In this section, PLL performances such as open-loop bandwidth f_c, phase margin ϕ_m, spectral purity, phase noise, etc. will be defined. First, open-loop and closed-loop transfer functions must be introduced.

In Fig. II-11 a linear, phase domain model of the PLL is given thanks to Equations (II-2), (II-3), (II-7), and (II-8) previously found for each PLL block. When in lock state the phase of the output signal of the divider ϕ_{loop}, tracks the phase of the reference signal ϕ_{ref}. The open-loop transfer function $G(s) = \phi_{loop}(s)/\phi_{ref}(s)$, can thus be expressed as:

$$G(s) = K_{pd} Z_f(s) \frac{2\pi K_{vco}}{Ns} = I_{cp} Z_f(s) \frac{K_{vco}}{Ns} \tag{II-27}$$

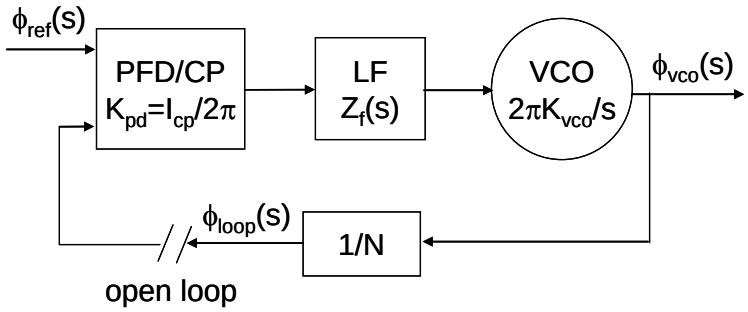


Fig. II-11. Linear model of a PLL

The closed-loop transfer function $H(s) = \phi_{loop}(s) / \phi_{ref}(s)$ can be expressed as:

$$H(s) = \frac{G(s)}{1+G(s)} = \frac{Z_f(s)\frac{2\pi K_{pd} K_{vco}}{N}}{s + Z_f(s)\frac{2\pi K_{pd} K_{vco}}{N}} \tag{II-28}$$

From which derives the low-pass behavior of the close-loop transfer function $H(j2\pi f)$.

2.3.1 Bandwidth and Phase Margin

The open-loop bandwidth f_c, also known as the 0dB cross-over frequency as shown in Fig. II-12, is defined by the condition $\left|G(j2\pi f_c)\right| = \left|G(j\omega_c)\right| = 1$. In Fig. II-12 the definition of phase margin ϕ_m is also given, which is: $\phi_m = \arg\left[G(j2\pi f_c)\right] + \pi$. Substituting Equation (II-3) in Equation (II-27), and imposing the condition on the open-loop transfer function in order to obtain the open-loop bandwidth yields:

$$\left|G(j\omega_c)\right| = \frac{I_{cp} K_{vco} k}{N\omega_c^2} \frac{\left|1 + j\omega_c \tau_2\right|}{\left|1 + j\omega_c \tau_3\right|} = \frac{I_{cp} K_{vco} k}{N\omega_c^2} \frac{\left|1 + j\omega_c \tau_2\right|}{\left|1 + j\omega_c \frac{\tau_2}{b}\right|} = 1 \tag{II-29}$$

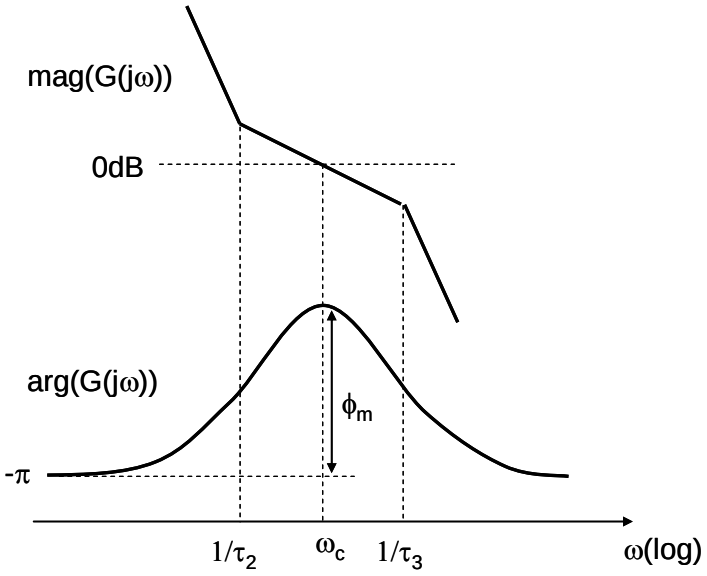


Fig. II-12. Bandwidth and phase margin

Once the LF determined, Equation (II-29) allows expressing I_{cp} as a function of the open-loop bandwidth ω_c. The phase of the open-loop transfer function is given by:

$$\Phi(j\omega) = -\pi + \arg(1 + j\omega\tau_2) - \arg(1 + j\omega\tau_3) = -\pi + \arg\tan\omega\tau_2 - \arg\tan\omega\tau_3 \qquad \text{(II-30)}$$

The derivative of Equation (II-30) becomes nil at:

$$\omega_{\max} = \sqrt{\frac{1}{\tau_2\tau_3}} \qquad \text{(II-31)}$$

Finally, the bandwidth ω_c is dimensioned to be equal to ω_{max} and thus ϕ_{max} results equal to the phase margin ϕ_m. It is then possible to express the LF parameters τ_2, τ_3 or b, and thus, R1, C1, and C2 of the LF, as a function of the phase margin ϕ_m and the bandwidth ω_c. Consequently, according to specifications, these conditions will yield the right choice and sizing of the LF [11].

2.3.2 Spectral Purity – Jitter

To establish the value of the LF elements, another condition besides open-loop bandwidth and phase margin is required. This condition is the spectral purity specification. Without reporting the detailed equations to determine LF parameters, let us just consider two important points:

- I_{cp} has to be kept to the lowest acceptable level to decrease power dissipation and simplify CP design,

- LF impedance must be maximized in order to minimize surface occupation, since this would mean small capacitors and a relatively high resistance.

However, a high impedance level leads to higher noise contribution from the LF. For much more detail on spectral purity and phase noise performances refer to [11].

The power spectrum at the output of an RF PLL contains, in addition to the carrier signal, spurious signals that degrade the system performances. These signals originate from basically two different sources: coupling between PLL signals and the output signal, or modulation of the local oscillator by deterministic baseband signals. RF spurious signals result in:

a) Phase modulation (PM) usually due to current leakages and mismatches. Equation (II-15) shows that the amplitude of the spurious signals is related to the peak phase modulation, conversely a peak phase deviation is associated with a pair of phase modulation spurious with amplitude A_{sp}, and is equal to:

$$\Delta\phi_p = 2\frac{A_{sp}}{A_{LO}} \tag{II-32}$$

b) Amplitude modulation (AM) which generates a pair of spurious signals in similar fashion as narrow-band PM does. AM spurious signals are mainly minimized by the use of a limiter, while PM spurious signals remain unchanged passing through a

limiter. A level, or swing, control, also known as automatic level control (ALC) in the VCO is and example of a limiter. It is made up of an envelop detector followed by an amplifier usually present in new generation VCOs to minimize swing variations with process deviations.

c) Non-deterministic spurious phase noise sidebands. These sidebands do not necessarily appear in pairs around the carrier, as they are not generated by a baseband modulation process. Without entering in complicated equations to characterize phase noise, that may be found in [11], [12], and [19], it may be stated that phase noise is made up of many components coming from the different blocks of the PLL and from the sources, the sum of which gives the total phase noise at the PLL output.

Fig. II-13 depicts the consequence of the disturbing effect of phase noise on the VCO output in the demodulation process of an RF signal. In fact, both direct and reciprocal mixing effects contribute adding phase noise to the output S_{dem}. Phase noise present at the local oscillator (LO) output S_{vco} is superposed by direct mixing to the desired signal during frequency conversion from f_d to $f_{if} = f_d - f_{LO}$ and a portion of this phase noise is also superposed to the desired signal by reciprocal mixing of the signal at f_a with S_{vco} at f_{LO} in the process of down conversion of f_a to $f_a - f_{LO}$. Degradation of the desired signal S_{dem} at f_{if} is a function of the amplitude of the adjacent signal at f_a and of the magnitude of the LO phase noise sidebands.

While a) and b) may be also referred to as *deterministic jitter* in the time domain, c) is also known as *non-deterministic jitter*. Jitter is the most important performance of a PLL, but the direct measurement of the sum of all jitter components at the VCO output is becoming unfeasible in the RF domain since the time interval to be measured may well be in the subpicosecond range. The main sources of PLL jitter are basically supply noise, noise on the VCO control line, input noise, and electronic noise in the PLL blocks. Two of them are predominant: input phase noise and VCO phase noise. The transfer functions of each phase noise source to the PLL output are depicted in Fig.

II-14 (a) and (b). The so called "slow jitter" components generated by the VCO are attenuated but the "fast jitter" ones are not. For the input phase noise the opposite is valid. Thus, the VCO phase noise transfer function has a high-pass behavior while the input phase noise transfer function has a low-pass behavior.

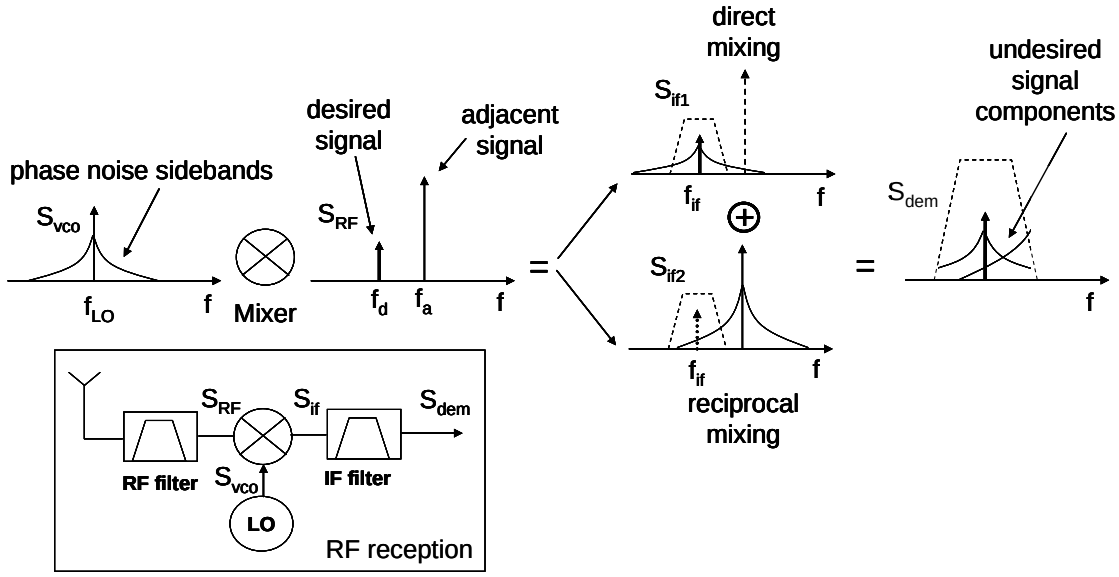


Fig. II-13. Phase noise effects on RF reception

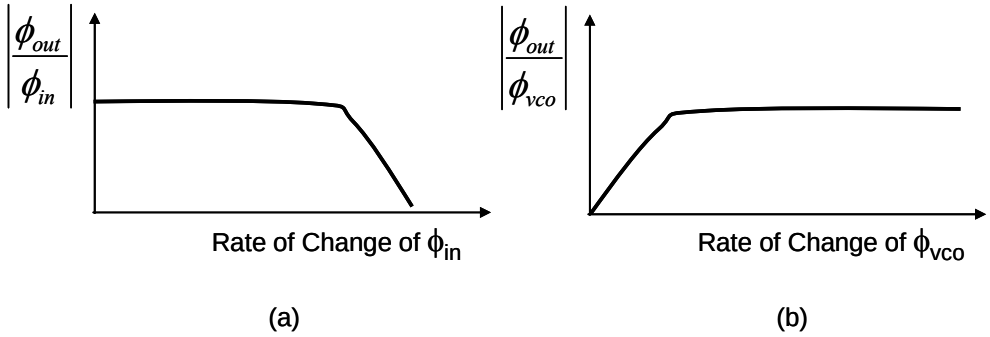


Fig. II-14. Transfer functions to the PLL output of (a) input and (b) VCO jitter

2.3.3 Capture and Lock Range

The settling time is the time necessary for the PLL to settle at the desired frequency f_{lock} within a frequency window $f_{lock} \pm f_{error}$, named capture range, as a result of an abrupt

frequency change. The lock range instead is the maximum frequency window $f_{lock} \pm f_{max}$ in which the PLL may still acquire the lock state without diverging. For frequency synthesizers, this window is also called tuning range. Therefore, the time necessary to acquire the lock state starting from the extreme frequency of the tuning range is called acquisition (or lock) time and it is intuitively much larger than the settling time, as graphically represented in Fig. II-15. For more detail on how to evaluate settling and acquisition times for a PLL refer to [14].

Some PLLs are subject to an operation failure, named false lock for which the PLL tends to lock itself to a harmonic of the input reference frequency instead of locking to the reference frequency itself. This occurs if the free running frequency of the VCO is close to a multiple (or a submultiple) of the reference frequency. Practice shows that this issue may be avoided designing a PFD with a phase detection range that goes beyond $\pm \pi$ at the highest operation frequency of interest [11], [14]. The proof of this may be found in Appendix 1. It is evident that, compared to a simple PD that detects only phase, a properly designed PFD detecting also frequency besides phase will serve the purpose.

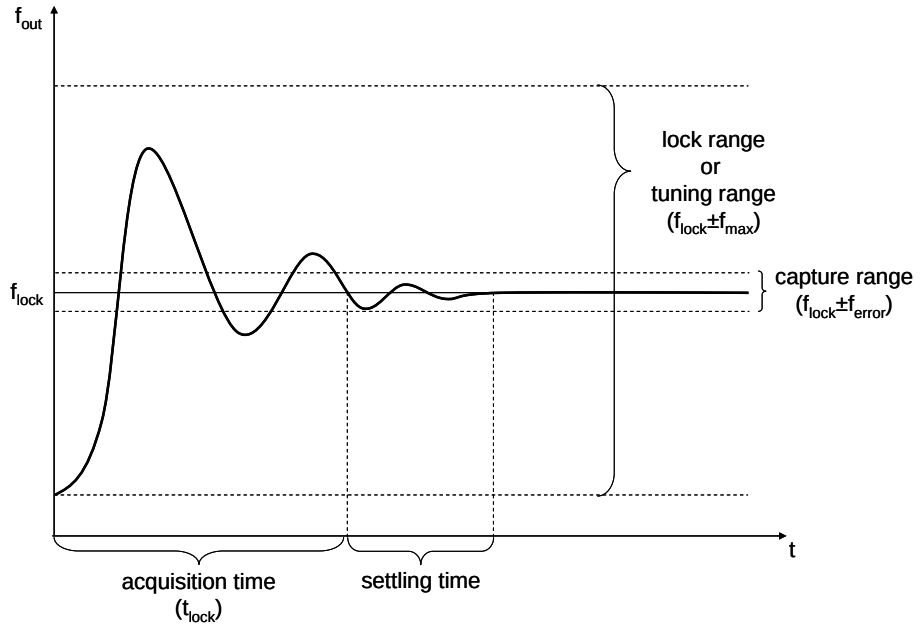


Fig. II-15. Capture and lock ranges with the corresponding settling and acquisition times

2.4 PLL Simulation

Nowadays, PLLs are validated by simulation in Spectre or Eldo environment in the following way. First of all, the small signal model of each block of the PLL is realized in a high level description language such as VHDL-AMS or VerilogA. This is a necessary procedure since the transient simulation to verify stability and lock acquisition of a whole PLL at component level is too time and resource consuming to be performed many times. Once verified the stability and the lock acquisition of the PLL with behavioral models, noise simulations have to be performed. Noise for each block at component level may be evaluated separately and introduced in the small signal model of the PLL as multiple additive sources, named Φ_x in Fig. II-16, where x stands for the block or group of blocks of the PLL.

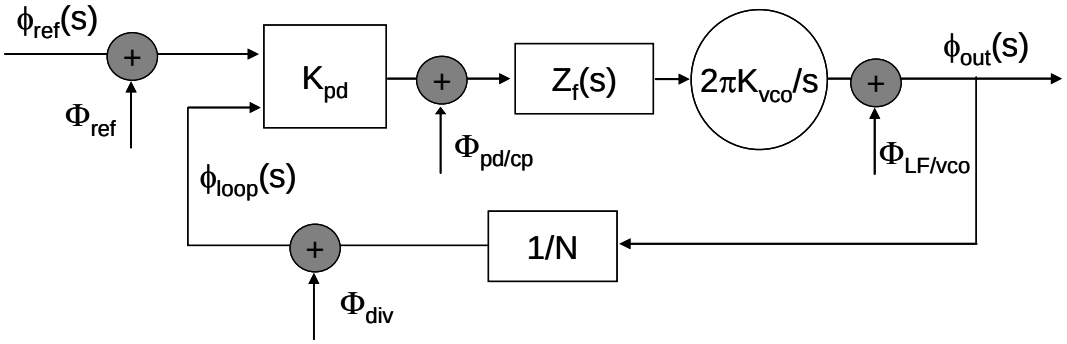


Fig. II-16. Small signal model with noise sources for PLL simulation

The total output noise of the PLL is the result of the contribution of all noise sources modified by the action of the feedback loop upon them. The output phase noise power density $\phi_{out}^2(\omega)$ is expressed as a function of two components:

$$\phi_{out}^2(\omega) = \phi_{olp}^2(\omega) + \phi_{ohp}^2(\omega) \tag{II-33}$$

where $\phi_{olp}^2(\omega)$ stands for the phase noise power density generated by noise sources subject to a low-pass transfer function when transferred to the output node and $\phi_{ohp}^2(\omega)$

represents the effect of the noise sources subject to a high-pass transfer function. Further details may be found in [11], [15].

Chapter III

State of the Art on PLL BIST

3.1 Introduction to IC Test

Historically, when electronic circuits were made up of discrete components mounted on printed circuit boards and tested with a "bed of nails" tester, access to all input and output voltages of components was easily achievable. The introduction of IC technology and the scaling of transistor sizes allow the development of much smaller and cheaper electronic systems, although for testing purposes, access to nodes becomes limited to primary inputs and outputs making it more difficult to detect and locate component failures when device specifications are not satisfied. Moreover, integrated circuit design represents a more significant part of the overall time-to-market of the device [2].

In the IC time-to-market diagram shown in Fig. III-1, test appears in two stages: the design stage and the manufacturing stage. The two types of test are substantially different. The so called characterization test found at the design stage is an extended and thorough test with the aim of locating the fault at component level and making the final design the most robust possible. This test is performed on corner lots of a vast number of prototype lots to obtain a statistically valid population. On the other hand, the production test done after manufacturing of the final devices to be shipped may not be as extended as the characterization one for time-to-market purposes. In fact, each device has to be tested before shipping. Considering the IC production volume, production test must be as fast and efficient as possible. At this stage the detection of a faulty device is

the only issue, location at component level of a fault with the aim of repairing the circuit or replacing a component is rarely an option. Nevertheless, a binning process is still carried out according to the performances of the device under test.

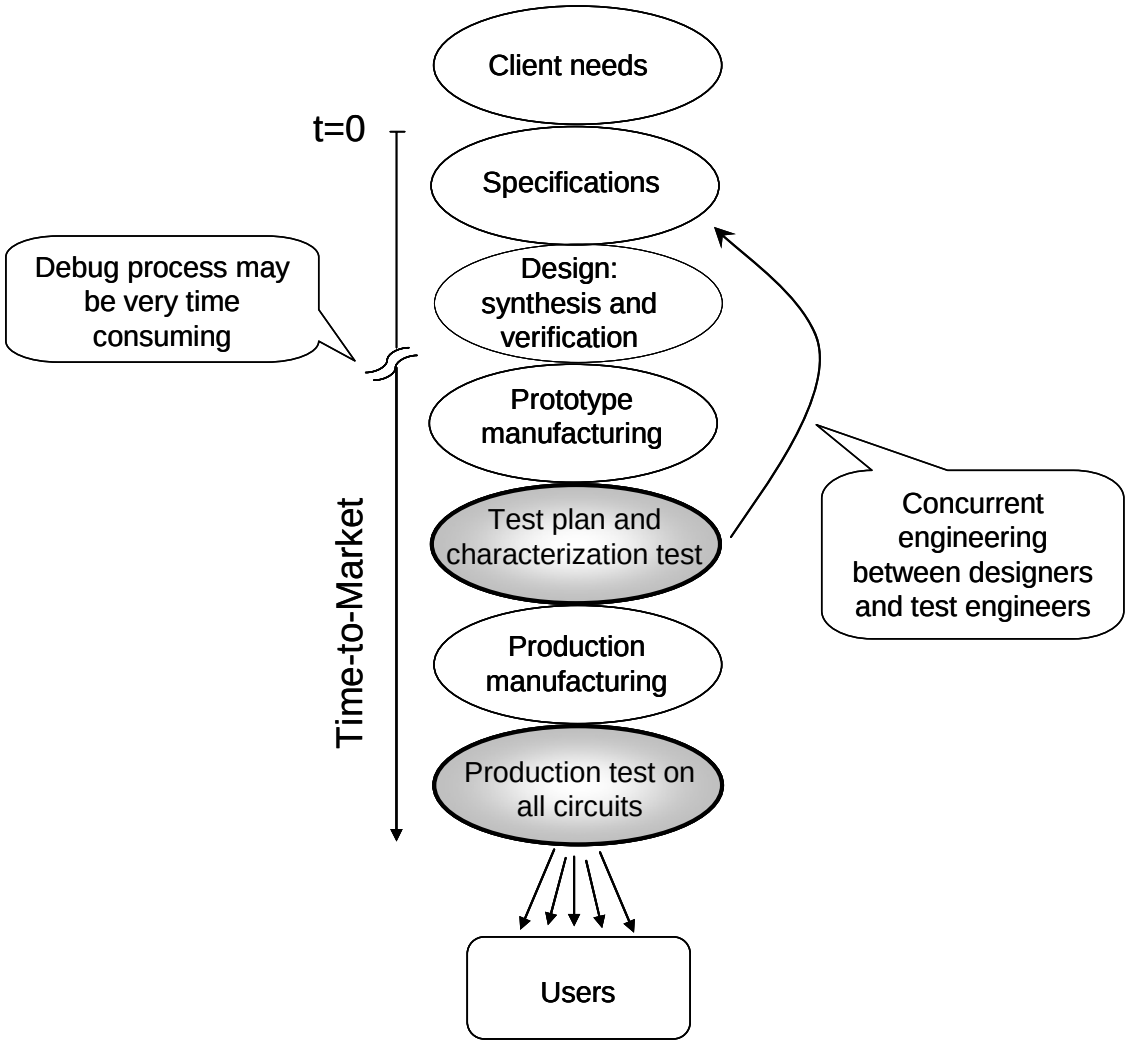


Fig. III-1. Time-to-market of an IC

Production test must thus be fast, cheap and efficient, with the highest fault coverage and the least functional devices rejected possible. For digital, low frequency devices, optimized techniques to accomplish this task are already largely in use, since they have been the object of extended studies up to now and are also more generalized. The same task is far from being accomplished in the analog, mixed-signal and RF domains, though. Actually, in testing digital devices the aim is basically to detect opens and

shorts (stuck-at faults). These are often easily-detectable catastrophic faults according to the robustness of digital design. Some of these known test techniques include: applying digital test vectors at the inputs and observing the corresponding output signature for the detection of stuck-at faults, the Iddq test which is based on the measurement of current consumption, and the well known scan chain which consists in flip-flop chains that can scan in test vectors from an ATPG and scan out test responses. Digital test is thus classified as a fault oriented structural test. On the other hand, besides considering catastrophic faults, circuit testing must address parametric faults as well, which are more difficult to detect with low-cost, fast test techniques. In this work a parametric fault is defined as the deviation of one or more parameters which leads to the non-compliance of one or more device specifications. The less robust the design is, the more complicated it is to detect these kinds of faults [2], [3].

3.1.1 Test Cost

The total cost of a chip is made up of different factors: manufacturing, packaging, assembling, and test. The cost of manufacturing, packaging, and assembling tends to lower, contrary to the cost of test which tends to increase. A rule of thumb states that the cost of detecting a malfunctioning device increases by a factor of ten at each step of integration, as shown in Tab. III-1 [1].

Device integration level	**Cost in $**
wafer	0.01 – 0.1
package	0.1 – 0.3
board	0.3 - 3
system	3 - 30
application	30 - 300

Tab. III-1. Cost of detecting malfunctioning devices as a function of their integration level

Clearly, the detection of malfunctioning devices at the manufacturing stage before further integration may save much money and, at the same time it may save the public image of the company with respect to the customer. In addition, production test

optimization saves test cost and decreases time to market. The goal is, in fact, to distinguish good circuits from faulty ones with minimum cost, where cost is influenced by test time, throughput, and the cost of test equipment.

3.1.2 Mixed-Signal/RF Test Strategy

A typical configuration used to test mixed-signal devices is shown in Fig. III-2. The main idea is to have access to, and excite, all analog blocks of the device and to test them separately from the digital blocks that will be driven by digital inputs.

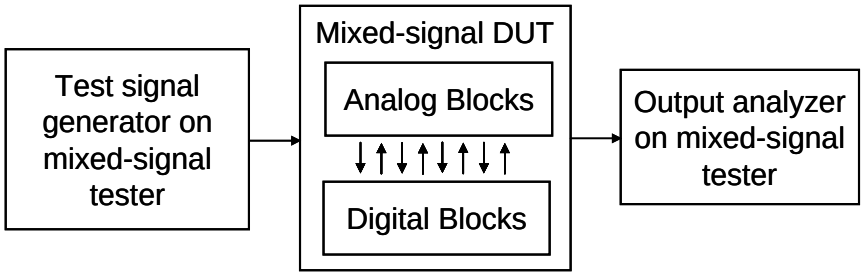


Fig. III-2. One possible test configuration for mixed-signal devices

Many factors limit the straightforward application of such an approach. First, mixed-signal circuits need to pass on digital testers as well as on mixed-signal test equipment for complete testing. Moreover, the inputs to the analog components of a mixed-signal circuit may not be accessible to the tester. In fact, it is not feasible for a designer to bring all of the analog inputs and outputs out to the package pins. There again, probe loading effects can degrade measurements made on naked die. Consequently, extra components are often required to access internal nodes through primary inputs and outputs. But in this case, the parasitics introduced when accessibility is augmented can degrade some circuit performances [2]. Finally, in RF applications, it is sometimes required to check not only the functionality of the analog components, but also the at-speed operation of the entire system, since the interactions between the digital and analog portions of the chip are complex and unique to each application. With ever increasing frequencies, at-speed testing of some device specifications is becoming unfeasible in particular for RF circuits that require dedicated test equipment. Given the

high cost of mixed-signal/RF dedicated testers, coupled with the time that each device spends on each tester (although numerous test stations may work in parallel), this testing approach can highly contribute to the cost of a device.

3.1.3 DfT & BIST

The demand for complex SoCs has pushed testing tools capabilities beyond their practical limits to keep pace with production and time-to-market constraints. In particular, IC verification and test are making SoC design more complex, time consuming, and less efficient. As a result, research in analog and mixed-signal testing is facing new concerns. In fact, analog and mixed-signal devices frequently cannot be tested using methods developed in the past anymore, due to the time and dedicated equipment required and the lack of accessibility to analog components embedded in large mixed-signal chips. Research addressing these problems was up to now preliminary and is evolving rapidly. Nevertheless, in the digital domain these techniques have been object of research since 1968, as shown in Fig. III-3.

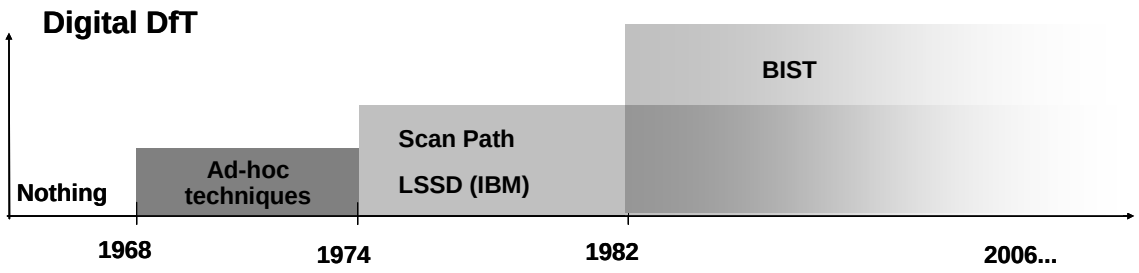


Fig. III-3. Evolution of Digital DfT for test improvement [3]

There is an increasing use of DfT techniques in the digital domain that focus on testing the structure of a design rather than its functionality. DfT with the purpose of testing the structure of the device is called structural DfT. DfT introduction in IC design is driven by the long-established need of improving controllability and observability of internal nodes for design diagnostics and system check-out, while still achieving acceptable fault coverage in reasonable time. Moreover, DfT techniques permit in some cases a more comprehensive test that may totally replace traditional functional test. Finally,

DfT is being used to provide test portability. As a consequence of this progress, DfT techniques are considered the best solution for lowering test costs. These non-traditional methods are more and more taking over traditional methods in digital domain. On the contrary, up to now, analog and mixed-signal DfT techniques mainly focus on facilitating functional testing of the DUT by means of test busses and scan methods, for example. This trend may change if the structural DfT techniques turn out to be decidedly more cost and time saving also in the analog and mixed-signal domain. In fact, the increasing complexity of analog and mixed-signal SoCs and the reduced access to internal nodes are making it not only more difficult to diagnose and locate faulty components, but also single IC functionality may become less transparent [3], [7].

Testability can also be improved by means of BIST techniques, which some consider as an "improved" version of a DfT technique, where signal generators and response analyzers are implemented on-chip. DfT techniques such as test busses and scan chains used to improve testability require transmitting signals through long wires and/or passing them through transmission gates before they can be actually measured. DfT techniques such as these are not well suited for analog and mixed-signal devices, since analog signals can result corrupted after long wire transmission, due to parasitic loading and coupling, and distortion may occur before measurements are made. BIST techniques help overcome this problem by going beyond just controlling and observing ICs inputs and outputs. In fact, in BIST applications, analog measured signals do not have to be routed off-chip and thus they are likely to suffer less distortion. Consequently, dynamic tests can be performed at full-speed, without external test equipment. The only signal that needs to be routed off-chip is a Go/No-Go bit indicating the test result. On the other hand, one major problem faced by BIST circuit designs is the area overhead. A way of optimizing area overhead is to reuse the same BIST monitors for testing different blocks on the same chip. Moreover, some BIST techniques, mainly for on-line test purposes, aim at on-chip measurements only, relying on external signal sources and not necessitating embedded signal generators, thereby minimizing the hardware overhead. Such BIST techniques tend to be less effective in detecting global parametric faults and component degradation since component

variations in the BIST monitors are likely to track those in the DUT. Hence, only catastrophic faults or major changes in component values are likely to be detected. To conclude, it may be stated that analog and mixed-signal BIST techniques go beyond simply improving controllability and observability of internal nodes by attempting to reduce the need for high-performance dedicated test equipment through implementing test signal generators and analyzing test results on-chip. In fact, analog and mixed-signal BIST techniques also allow more flexibility to make the tradeoff between the increased silicon area needed for BIST circuitry and external tester requirements [2].

3.2 Evaluation of Analog/Mixed-Signal BIST Techniques

In order to evaluate test techniques, analog test metrics estimation is essential. The estimation of test metrics such as fault coverage (rejection of malfunctioning circuits), defect level (acceptance of malfunctioning circuits), test yield (number of accepted circuits), and yield loss (rejection of functional circuits) is necessary in order to quantify performance and cost of a test approach. For DfT and BIST purposes, test metrics allow the choice of the most suitable test measures. This choice must be imperatively done at the design stage, before production.

In order to evaluate the test metrics for a given BIST technique, it is necessary to set limits for each test measure considered by the embedded BIST monitors. A statistical model of the DUT is required for setting these limits. This model is obtained through process deviations, by using data obtained via Monte-Carlo circuit simulation [4]. Test limits are set by considering the best trade-off between parametric defect level and yield loss for the model obtained, as will be better detailed further on and shown in Fig. III-5. Other test metrics such as fault coverage will be evaluated after a fault injection simulation campaign of the DUT in order to complete the BIST technique evaluation. The optimized set of test measures can then be chosen according to different criteria: the expected test metrics, area overhead of each monitor versus its fault coverage contribution, and test time in case a particular BIST monitor needs previous calibration and/or test time for measurement.

Faults to be injected may belong to either of the two following families: catastrophic faults and parametric faults. In Fig. III-4 a resistor *R* with a nominal value of 100 kΩ has been taken as an example. Catastrophic faults are faults that appear very far on the Gaussian tail, while parametric faults are defined in [5] as a variation of a parameter from its nominal value due to process deviation large enough to bring the device out of specifications. Examples of catastrophic faults are opens and shorts on a net or in a component. A catastrophic fault is not usually a consequence of a deviation of a parameter (too far from its nominal value), but rather the result of a deposited dust particle or a bad etching during fabrication. A parametric fault instead, is a parameter deviation located quite close to the nominal value but far enough in the Gaussian tail to make the circuit fall out of specifications, as shown in Fig. III-4.

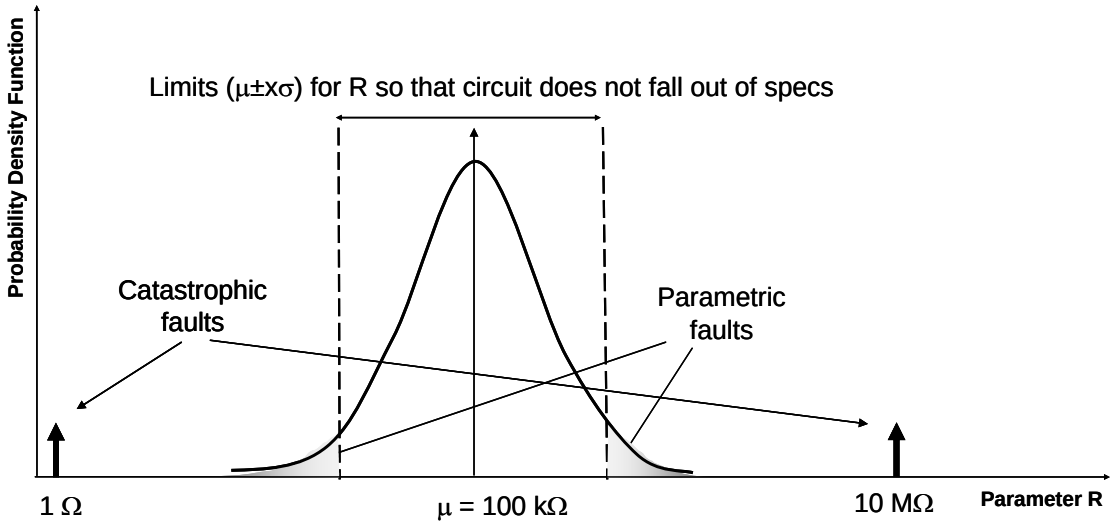


Fig. III-4. Catastrophic versus parametric faults

3.2.1 Parametric Test Metrics Definitions

The parametric analog test metrics considered to set test limits are [5]: Yield (*Y*), Test Yield (Y_T), Yield Coverage (Y_C), Yield Loss (Y_L), Defect Level (*D*), and Faulty Circuit Coverage (*F*). An exponent *D* will indicate that these metrics are estimated at the design stage, considering process deviations. Let $A = \{A_1, A_2, ..., A_n\}$ be the set of the *n*

specifications and $B = \{B_1, B_2, \ldots, B_m\}$ the intervals of the accepted values of the m test measures. The test metrics are defined and calculated theoretically as in Tab. III-2.

Name	Definition	Symbol	Theoretical calculus
Yield	$\frac{\text{Number of functional circuits}}{\text{Total number of circuits}}$	Y^D	$= \int_A f_S(s)ds$
Test Yield	$\frac{\text{Number of pass circuits}}{\text{Total number of circuits}}$	Y_T^D	$= \int_B f_T(t)dt$
Yield Coverage	$\frac{\text{Number of pass functional circuits}}{\text{Number of fuctional circuits}}$	Y_C^D	$= \frac{\int_A \int_B f_{ST}(s,t)dsdt}{Y^D}$
Yield Loss	$\frac{\text{Number of fail functional circuits}}{\text{Number of fuctional circuits}}$	Y_L^D	$= 1 - Y_C^D$
Defect Level	$\frac{\text{Number of pass faulty circuits}}{\text{Number of pass circuits}}$	D^D	$= 1 - \frac{Y_C^D Y^D}{Y_T^D}$
Faulty Circuit Coverage	$\frac{\text{Number of fail faulty circuits}}{\text{Number of faulty circuits}}$	F^D	$= 1 - \frac{Y_T^D D^D}{1 - Y^D}$

Tab. III-2. Parametric test metrics

In the table above $f_S(s)$ is the joint probability density function (PDF) of the performances, $f_T(t)$ is the joint PDF of the test measures, and $f_{ST}(s,t)$ is the joint PDF of the performances and the test measures. A fitted probability distribution function can then be used to estimate test metrics at the design stage for process deviations using the equations in table Tab. III-2. However, a direct integration of these equations is normally not feasible when several performances and test measures are considered. To overcome this problem the fitted PDF is directly sampled to generate by software (MatLab) a larger population that has the same statistical behavior [9]. The parametric test metric Faulty Circuit Coverage is different from the typical Catastrophic Fault Coverage which corresponds to the number of detected faults (fail faulty circuits, as for

F^D) divided by the number of total faults injected, which is not always equal to the number of faulty circuits (as in F^D).

3.2.2 BIST Evaluation Methodology

Fig. III-5 illustrates the BIST evaluation methodology [16]. First, a statistical model of the performances and test measures of the DUT is built using the following steps:

- Monte-Carlo simulation of the DUT (1000 instances) under process and mismatch deviation.

- Estimation of the joint PDF of performances and test measures. Different techniques can be used for density estimation:

    - Copulas-Based method
    - Non-Parametric method
    - Multi-Normal method

- Generation of a large population (>1e6 instances) by sampling the statistical model to obtain ppm precision for test metrics.

Once a large population of devices has been generated, test limits $\mu \pm x\sigma$ can be evaluated on the statistical population. Test limits for test measures are fixed as a tradeoff between parametric defect level and yield loss considering process and mismatch deviations. This procedure is shown in the example of Fig. III-5 for a test measure with a Normal PDF.

Finally, test metrics are evaluated fore the case of simple parametric faults and catastrophic faults for the test measures and the test limits considered. It must be noted that these faults are not covered by the statistical model and thus they need to be simulated one by one.

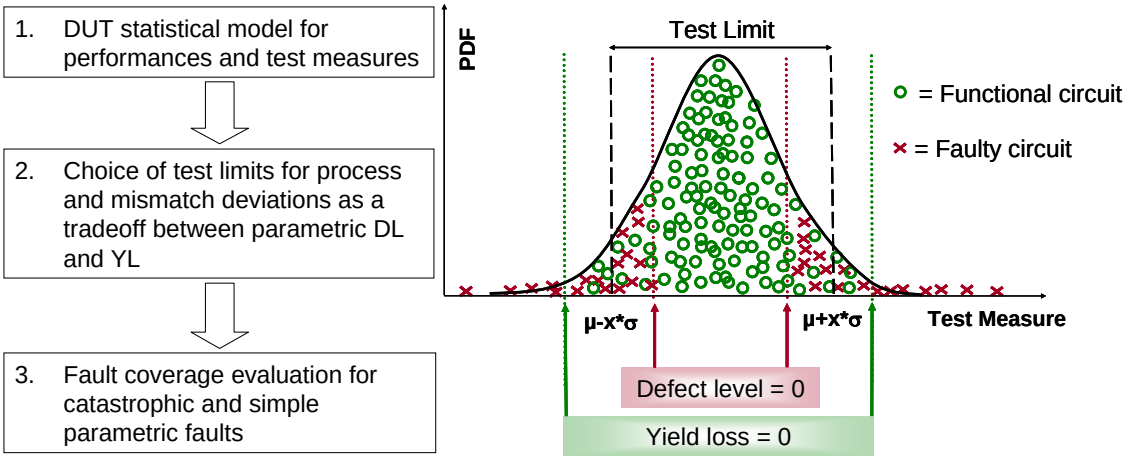


Fig. III-5. BIST evaluation methodology

3.2.3 Density Estimation

For test metrics evaluation purposes, an initial population of the DUT using Monte-Carlo simulation is generated, producing a statistical sample of the DUT. However, only a limited number of circuit instances can be generated in a reasonable time with this technique. These Monte-Carlo generated instances are often insufficient to set test limits with enough precision, since few faulty instances are generated. Thus, a probability density estimation technique is necessary in order to obtain a representative population. The joint PDF of the DUT performances and test measures is obtained from the Monte-Carlo instances using density estimation techniques. This statistical model is next sampled in order to generate a great amount of instances from which test limits can be set with part-per-million (ppm) accuracy, as represented in Fig. III-6. The generated population will be compared with the original one to verify if the statistical model, and consequently the density estimation technique chosen, is suitable. Some density estimation techniques include the normal multivariate distributions, the kernel-based density estimation (KDE), and the Copulas theory.

In this work, Copulas theory will be used for estimating the multivariate joint PDF of performances and test measures for different DUTs.

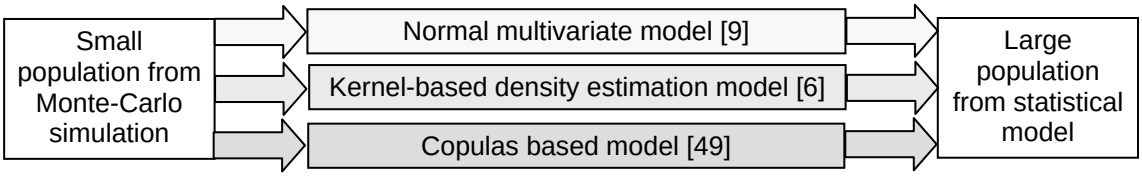


Fig. III-6. Density estimation techniques to obtain a significant population

3.2.4 Density Estimation Using Copulas Theory

The notion of copula was introduced by A. Sklar in 1959 when studying the relationship between a multidimensional probability function and its lower dimensional margins. To give an idea of what a copula is (but not a definition) as stated in [57], copulas are "functions that join or copule multivariate distribution functions to their one-dimensional marginal distribution functions" or "distribution functions whose one-dimensional margins are uniform." At the beginning, copulas were mainly used for probabilistic metric-spaces theory development. Later, they have become of interest to define non-parametric measures of dependence between random variables, and since then, they began to play an important role in probability and mathematical statistics.

Since dependence measures other than Copulas are scale-invariant (they remain unchanged under strictly increasing transformations of the random variables), they give no clue on the invariant properties of the joint PDFs of the random variables. Some of these dependence measures are discussed in Appendix 2. It is a particular characteristic of copulas "to capture those properties of the joint distribution which are invariant under almost surely strictly increasing transformations". Therefore, all scale-invariant properties and measures are expressible in terms of copula of the random variables.

Let us then define a copula. Let $\boldsymbol{I}$ be the unit interval [1 ; 0]. An n-dimensional copula (or just copula) C is a multivariate distribution function with uniformly distributed margins whose domain is the unit n-cube $\boldsymbol{I}^n = \boldsymbol{I} \times \boldsymbol{I} \times \boldsymbol{I} \times \ldots \times \boldsymbol{I}$. A copula is thus a function C from $\boldsymbol{I}^n$ to $\boldsymbol{I}$ which has the following properties:

1) For every $\boldsymbol{u}$ in $\boldsymbol{I}^n$, $C(\boldsymbol{u}) = 1$ if all coordinates of $\boldsymbol{u}$ are 1, otherwise $C(\boldsymbol{u}) = 0$.

2) For every $\boldsymbol{a}$ and $\boldsymbol{b}$ in $\boldsymbol{I}^n$ such that $\boldsymbol{a} \leq \boldsymbol{b}$, the volume of the copula $V_C([\boldsymbol{a}, \boldsymbol{b}]) \geq 0$.

An explanation on how copulas relate to the link between multivariate distribution functions and their univariate margins is given by Sklar in the following theorem, that represents the crucial basis of all Copulas Theory applied to statistics. Let F be a n-dimensional distribution function with margins F_i for $i \in [1,n]$, then there exists a copula C such that for all $x_i \in [-\infty,\infty]$,

$$F(x_1, x_2, ..., x_i, ..., x_n) = C\left[F_1(x_1), F_2(x_2), ..., F_i(x_i), ..., F_n(x_n)\right] \quad \text{(III-1)}$$

If F_i are continuous, then C is unique; otherwise, C is uniquely determined in the range of values of the marginal distributions. Reciprocally, if C is a copula and $u_i \in [1,0]$ are cumulative distribution functions, then the function F defined by Equation (III-1) is a joint distribution function with margins F_i:

$$C(\mathbf{u}) = F[F_1^{-1}(u_1), F_2^{-1}(u_2), ..., F_i^{-1}(u_i), ..., F_n^{-1}(u_n)] \quad \text{(III-2)}$$

The proof may be found in [57].

The Copulas theory requires a density estimation of the distribution function F. The marginal PDFs f_i for each performance and test measure x_i can be easily estimated from the original data using well known univariate laws or KDE techniques. The copula can often be chosen from a set of known functions and calibrated for a given case-study. For a multivariate n-dimensional PDF $f(x_1, ..., x_n)$, the univariate marginal PDFs $f_i(x_i)$ and the variable dependence structure $c\left[F_1(x_1), ..., F_n(x_n)\right]$, where $F_i(x_i)$ are the CDFs, can be completely separated using Sklar theorem:

$$f(x_1, ..., x_n) = c\left[F_1(x_1), ..., F_n(x_n)\right] \cdot \prod_{i=1}^{n} f_i(x_i) \quad \text{(III-3)}$$

where $c\left[F_1(x_1), ..., F_n(x_n)\right] = \dfrac{\partial^n C\left[F_1(x_1), ..., F_n(x_n)\right]}{\partial F_1(x_1) ... \partial F_n(x_n)}$ is the copula density function.

Fig. III-7 illustrates how to apply copulas for density estimation purposes [49]. While the distribution of x_{cc} and x_{of} $F(x_{cc}, x_{of})$ and the PDFs $f_{cc}(x_{cc})$ and $f_{cc}(x_{of})$ all have a dependence on the scale of the variables (where x_{cc} is the current consumption and x_{of} is the output frequency for V_{tune} at 0.8 V of the VCO case-study), the copula of x_{cc} and x_{of} $C(u_{cc}, u_{of})$ obtained using the transform $u_i = F_i(x_i)$, is completely independent from scale, thus it allows to establish the invariant relationship between the variables x_{cc} and x_{of}. The copula function is also n-dimentional as the multivariate joint PDF, but thanks to the fact that a) it is scale invariant, b) its marginals are uniformly distributed between 0 and 1, c) making the hypothesis that the copula fits a Gaussian copula, it is much easier to estimate than the n-dimentional joint PDF. In order to generate a large sample of $F(x_{cc}, x_{of})$, called $F_L(x_{cc}, x_{of})$ in Fig. III-7, the estimated copula function (in this example a Gaussian copula function) is sampled and the inverse transform $x_i = F^{-1}(u_i)$ is used.

Multivariate Gaussian Copula

A Gaussian copula $C_R(\mathbf{u})$ belongs to the elliptical family of copulas and is constructed from the multivariate normal distribution via Sklar's theorem as follows:

$$C_R(\mathbf{u}) = F_R\left(F_G^{-1}(u_1), F_G^{-1}(u_2), ..., F_G^{-1}(u_i), ..., F_G^{-1}(u_n)\right) \tag{III-4}$$

where F_R is the multivariate normal cumulative distribution function with Pearson's correlation matrix R, which is a symmetric, positive-definite matrix with $diag(R) = 1$ and $\rho_{xi,xj} = \dfrac{\mathrm{cov}(x_i, x_j)}{\sigma_{xi}\sigma_{xj}}$ for $i \neq j$, F_G is the standard univariate normal cumulative distribution function and $\mathbf{u} = \{u_1, u_2, .. u_i, .. u_n\}$ with $u_i \in [0,1]$. Differentiating C_R yields the copula density function:

$$c_R\left(F_G(x_1), ..., F_G(x_i), ..., F_G(x_n)\right) = c_R(\mathbf{x}) = \frac{f_R(\mathbf{x})}{\prod_{i=1}^{n} f_G(x_i)} = \frac{1}{\sqrt{|R|}} e^{-\frac{1}{2}\mathbf{x}^T(R^{-1}-I)\mathbf{x}} \tag{III-5}$$

Where $f_G(x_i)=\frac{1}{\sqrt{2\pi}}e^{-\frac{1}{2}x_i^2}$ is the standard normal density, $f_R(\mathbf{x})=\frac{1}{\sqrt{(2\pi)^n|R|}}e^{-\frac{1}{2}\mathbf{x}^T R^{-1}\mathbf{x}}$ is the density function for the standard multivariate Gaussian distribution where the correlation matrix R is used in place of the variance-covariance matrix S since they are equivalent for normalized distributions, and $\mathbf{x}$ is the vector of the Gaussian univariate inverse cumulative distribution functions $\mathbf{x}=\{x_1,x_2,...x_i,...x_n\}=\{F_G^{-1}(u_1),...,F_G^{-1}(u_i),...,F_G^{-1}(u_n)\}$. For details on density estimation for a multinormal distribution refer to Appendix 3.

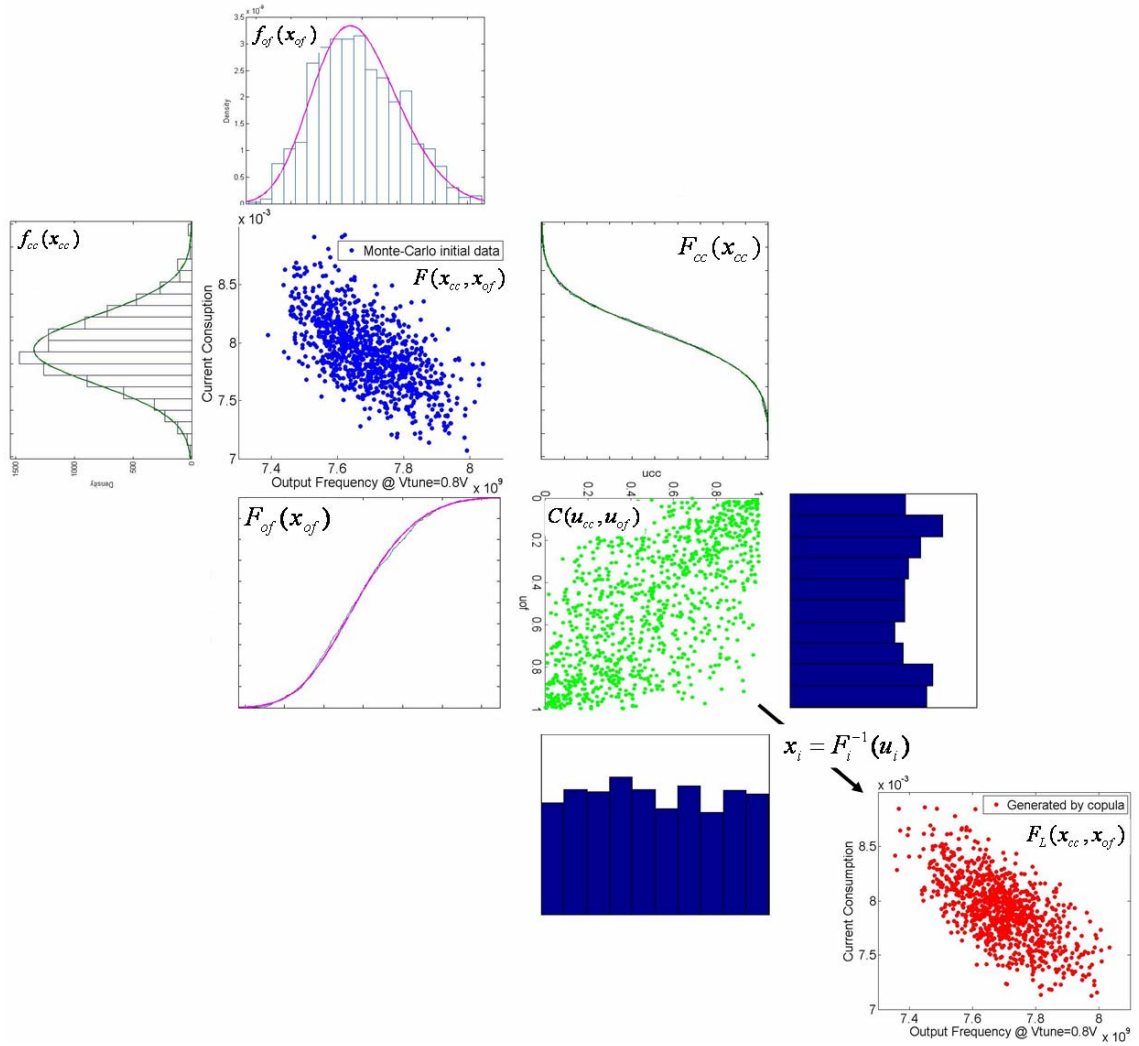


Fig. III-7. Copulas application to density estimation

3.3 PLL Functional BIST Techniques

Recent research efforts have sought to find accurate ways of measuring on-chip PLL functional parameters. Sunter and Roy have developed several works on this subject, the most recent being the ULTRA technique. Thanks to the undersampling technique already proposed by Huang in [20], this technique by LogicVision is capable of evaluating jitter with subpicosecond resolution [1], [21]. Nevertheless, this technique requires a clean reference in order to generate a frequency close, but not equal to, the PLL output frequency. Previous interesting techniques were based on phase shifting the output frequency with delay lines, sampling with a D flip-flop and counting the times the clock edge would lag/lead the frequency edge [8], [25], [26], [27]. On the same principle, but with finer, sub-gate resolution, are based all techniques using Vernier delay lines [29], [30] or Vernier ring oscillators [31]. Techniques based on delay elements require previous thorough calibration, since delay elements are very sensitive to process deviations [30], [32], [33]. Most works based on jitter measurement do not provide any information on fault coverage and test metrics of the BIST technique applied to a DUT. In the following sections, a more complete overview of these techniques will be given.

3.3.1 Gain, Lock Range, and Lock Time Measurements Using Phase Shifting

In 1999 LogicVision issued a BIST technique [8] capable of measuring the open-loop gain G_{OL}, the lock range and time, and, most important of all, jitter. This technique is based on applying a temporary phase delay at the input $\Delta\phi_{in}$ which, being related to the associated frequency variation of the VCO Δf_{vco}, allows all measurements listed above (except jitter which is described afterwards) to be estimated through simple equations. The block schematic for all measurements except jitter is presented in Fig. III-8.

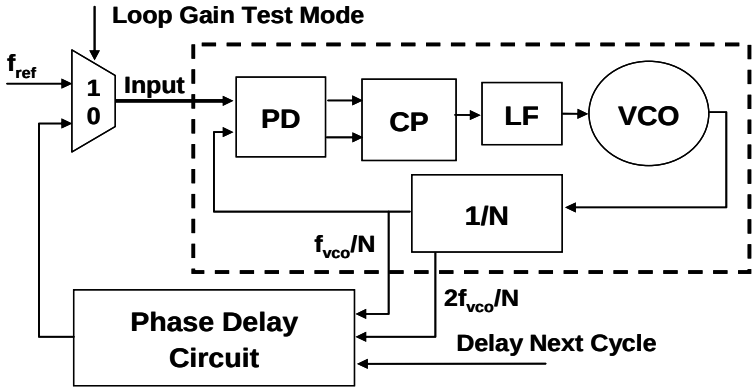


Fig. III-8. PLL BIST for gain, lock range and lock time measurements [8]

The phase delay lasting M clock cycles will cause a rapid frequency variation at the PLL output lasting the whole phase shift duration. When the phase delay returns to zero, the output frequency remains constant at its new value. The equation that relates the phase shift $\Delta\phi_{in}$ with the output frequency variation Δf_{vco} is as follows:

$$\Delta f_{vco} = \frac{MK_{pd}K_{vco}\Delta\phi_{in}}{sC} = \frac{MK_{vco}\Delta\phi_{in}I_{cp}}{2\pi sC} \qquad \text{(III-1)}$$

where Δf_{vco} derives from Equation (II-4) for which $\Delta f_{vco} = K_{vco}\Delta V_{tune}$ and Equation (II-1) for which $\overline{I_{out}} = I_{cp}\frac{\Delta\phi_{in}}{2\pi}$, K_{pd} is the PFD/CP block gain as in Equation (II-2) that states $K_{pd} = \frac{I_{cp}}{2\pi}$, K_{vco} is the VCO gain, C is the LF capacity (supposing the LF is a simple integrator for which $V_{tune}(s) = \frac{1}{sC}I_{out}(s)$), and I_{cp} is the CP current.

To evaluate the open-loop gain the following steps are followed starting from Equation (II-8) and keeping in mind that $\phi(s) = \frac{2\pi}{s}f(s)$:

$$\Delta\phi_{loop} = \frac{\Delta\phi_{vco}}{N} = \frac{2\pi\Delta f_{vco}\big|_{M=1}}{sN} = \frac{K_{vco}\Delta\phi_{in}I_{cp}}{NCs^2} \quad \text{(III-2)}$$

$$\left|G_{OL}\right| = \left|\frac{\Delta\phi_{loop}}{\Delta\phi_{in}}\right| = \frac{K_{vco}I_{cp}}{(2\pi)^2 f_{ref}^2 NC} \quad \text{(III-3)}$$

where $\Delta\phi_{loop}$ is the feedback phase variation evaluated for M = 1 clock cycles and $\left|s^2\right| = (2\pi)^2 f_{ref}^2$. Substituting Equation (III-1) in (III-3) yields:

$$G_{OL} = \frac{\Delta f_{vco}}{MN\Delta\phi_{in} f_{ref}} \quad \text{(III-4)}$$

In this equation, Δf_{vco} may be measured by means of a frequency counter, $\Delta\phi_{in}$ is digitally controlled, and M is also controlled by a counter. The output frequency variation is proportional to the open-loop gain, to the input phase delay applied, and to the number of clock cycles during which the phase shift is applied. By subtracting the frequency change measured when no phase shift is introduced (over a similar time interval), any measurement errors due to an unknown phase offset, leakage current, or similar systematic errors, can be canceled (at first order approximation). This subtraction aspect is very important for tolerance to process variations. Since the value of f_{ref} is known, limits on Δf_{vco} may be set during test or stocked on-chip in order to have a BIST that accepts only devices that comply with G_{OL} specifications.

Concerning lock range, the phase delay block is used to introduce a phase shift large enough to push the PLL output frequency to its maximum value (see Fig. II-15). This may be achieved by connecting the PLL input at the divider output equal to twice the feedback frequency, $2f_{vco}/N$ in Fig. III-8, and measure the output frequency periodically. When its value does not vary significantly anymore within a programmable time interval (i.e. it approaches its minimum or maximum value), the last recorded frequency count is saved. This procedure must be done at a slow rate in order to measure the frequency many times during this frequency transition procedure.

Once the output frequency has reached its maximum value, lock time may be measured closing the loop once again reconnecting the regular input (without forcing any phase shift) and counting the clock cycles until lock is reached. This aspect of changing at slow rate the input frequency to push the output frequency at its maximum level while constantly measuring it makes the BIST technique less interesting under the production test point of view, since production test must be fast in order to be of any interest.

3.3.2 Jitter Measurement Using Phase Shifting

As already explained, jitter is a complex phenomenon for which the phase of a signal with fairly constant frequency deviates randomly with respect to the average frequency. The importance of measuring jitter (or phase noise) is related to the spectral purity of the output frequency as explained in sections 2.2.3 and 2.3.2. The best way to represent this phenomenon is by means of its root mean square (RMS) value.

The higher the frequencies that come into play, the more difficult it is to evaluate jitter without frequency division, which definitely implies a relative loss of information on jitter itself. Most BIST techniques existing in the literature, some of which are described below, are conceived more for PLLs working at relatively low frequencies than for RF PLLs. Although one technique, the ULTRA technique by LogicVision which is also the most credited as BIST technique for RF PLLs up to now, allows jitter measurements with resolution below one picosecond.

For jitter measurement, the BIST technique first proposed in [8] is very similar to the one later proposed in [25]. This technique is based on the principle of Vernier Delay Lines which is explained later in this section. As Fig. III-9 (a) shows, the PLL output is sent to a D-type flip-flop (D-FF) input through a constant delay. In addition, the PLL input is used as the clock signal of the D-FF after passing through a digitally controlled adjustable delay, shown in Fig. III-9 (b), whose maximum value is approximately the double of the constant delay. This delay makes the arrival time of the clock signal vary with respect to the signal *SUT'*, allowing calculating (at the D-FF output) the CDF of

the delay between the two signals. A graphical representation of this is shown in Fig. III-10.

If the rising edge *B* of the clock, CLK'_{ref}, lags the rising edge *A* of the signal under test, *SUT'* (i.e. *B* comes after *A*) with a relative delay Δd, the output of the D-FF, *Q*, is at logic zero in jitter absence conditions. If jitter is present though, it may happen that *B* deviates towards *A* until it starts leading *A* and in this condition *Q* switches to logic one. The probability that *B* leads *A* is the area of the PDF shaded in Fig. III-10, which is expressed as [17]:

$$p_{B\,leads\,A} = \int_{-\infty}^{-\Delta d} PDF(t)dt = CDF(-\Delta d) \qquad \text{(III-5)}$$

The D-FF output is compared to the expected value and each time an error occurs the error counter is incremented by one. If the clock duty cycle is 50 % the expected value is always logic level one. Since the error counter can count up to a maximum value *E*, this value is stored and the counter (not shown in Fig. III-9) is reset every *E* cycles of the PLL input signal.

The D-FF in [25] is followed by a NAND gate, as shown in Fig. III-9, to generate a pulse for every clock event even if the D-FF output stays high. Thus pulses are generated when the signal edge precedes the clock edge, and these pulses are counted by the counter. The CDF is given by the ratio of counts in the error counter to the counts in a clock counter (not shown in Fig. III-9), as a function of the clock delay.

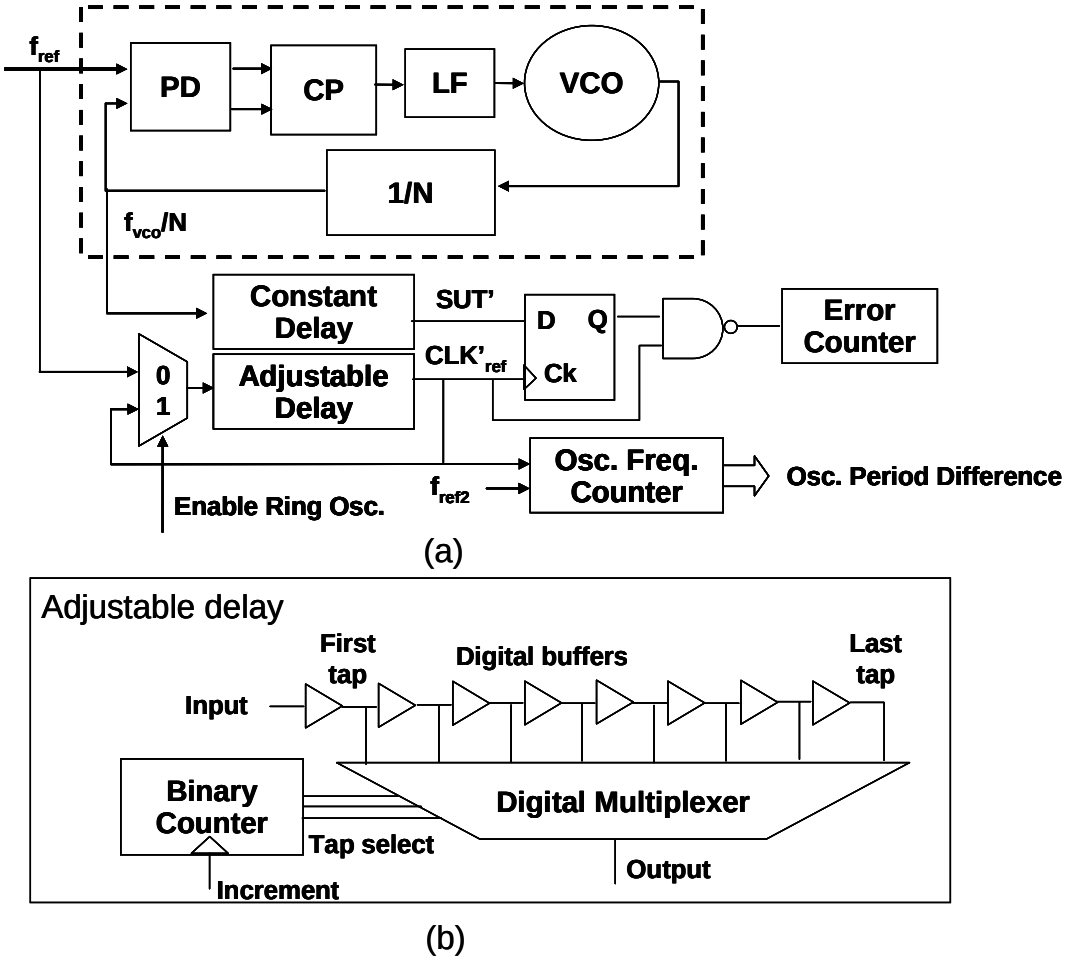


Fig. III-9. PLL BIST for (a) RMS jitter measurement and (b) adjustable delay block [8]

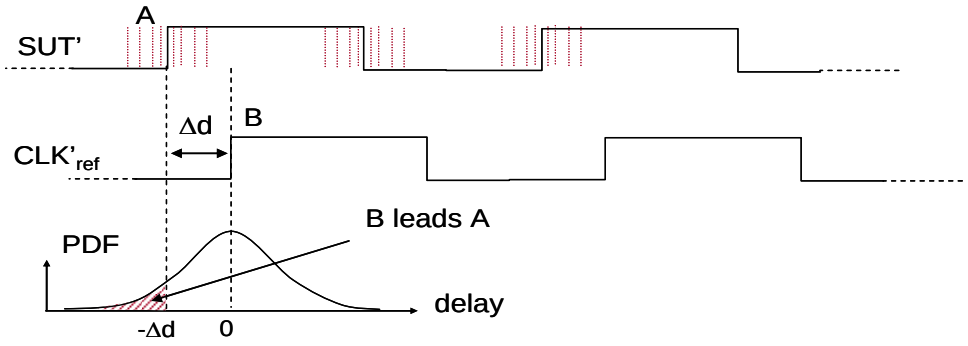


Fig. III-10. Graphical representation of PLL jitter evaluation using adjustable delays

The RMS jitter of a rising edge sensitive PLL is evaluated as follows. First, the adjustable delay is set at its minimum value to impose a zero value at the error count for each group of E cycles. Then, the counter that controls the adjustable delay is incremented after each E cycle of the PLL input signal. The values of the counter that controls the adjustable delay are then registered for values of the error counter equal to 15.9 % and 84.1 % of E (these are the $-\sigma$ and $+\sigma$ points of the CDF supposing a Normal distribution for the jitter). Besides, the adjustable delay block can be reconfigured as a ring oscillator whose oscillation period is measured by means of a frequency counter. Both delays at $-\sigma$ and $+\sigma$ can thus be measured and the difference between them is digitally coded at the output. Since a difference is measured, all constant delays are cancelled, including the D-FF settling time. Finally, Fig. III-9 (a) shows that a second clean reference f_{ref2} is needed for the oscillation counter. This frequency is not specified in [8] and it is in fact one of the major limitations of this BIST technique.

A detail which is not specified in [8], but is of great importance has been highlighted in [25] and in other works dealing with delay lines such as [30], [32], [33]: the delay chains of both the constant delay and the adjustable delay must be calibrated since delay elements are very sensitive to process deviations. A delay chain can be calibrated by reconfiguring the chain into a ring oscillator, and measuring the oscillation frequency. This frequency can be measured by an off-chip frequency counter or by taking the ratio of counts in the ring oscillator counter to the reference clock counter which is operated at a known frequency.

Another work suggests an interesting variant of the previous technique for measuring the jitter of a signal [17], [18]. Supposing that jitter is a random variable with a Normal law trend, the aim is to evaluate the RMS value of the jitter, J_{RMS} of a signal under test *SUT*. The basic idea is represented in Fig. III-11, where the jitter at the i clock cycle is $J_i = d_i - T_{id}$. The principle is similar to the one depicted in Fig. III-10.

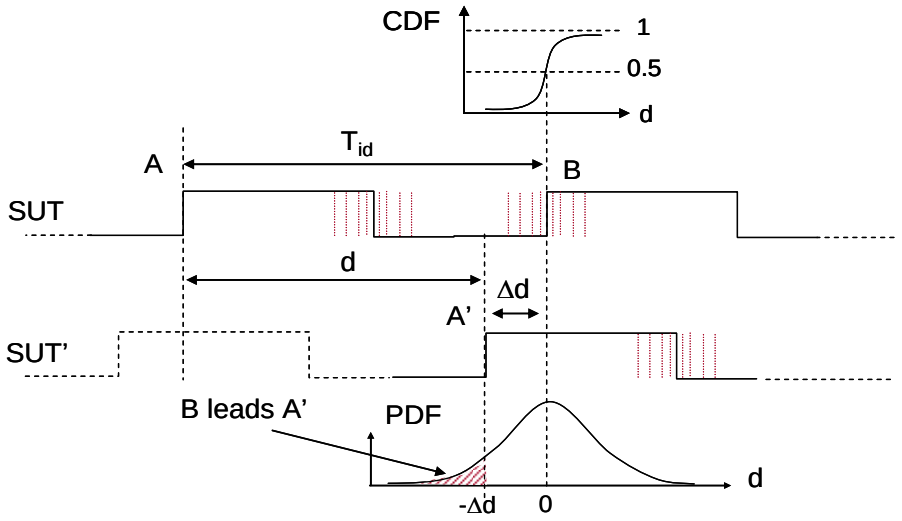


Fig. III-11. Principle of signal jitter measurement by means of its CDF

In Fig. III-11, *SUT'* represents *SUT* delayed of *d* and *A*, *B* and *A'* are the rising edges. Visibly, if *SUT* is jitterless, *A'* will always lead (lag) *B* if *d* is smaller (larger) than the *SUT* ideal period, T_{id}. Nevertheless, in presence of jitter, *B* may change its relative position to *A* and the probability that *B* leads *A'* is a function of *d* and J_{RMS}. If *d* is equal to *T*, this probability is equal to 0.5. With increasing (decreasing) values of *d*, *p* tends to one (zero) and, there again, if J_{RMS} increases, the CDF becomes flatter. The relationship (III-5) between PDF and CDF is clearly shown in Fig. III-11.

To obtain statistical information on jitter the idea is again to compare the phase relations (leading or lagging conditions) between *SUT* and two delayed versions of itself in this case (once for d_1 and once of d_2). For each delay, the probability of *SUT* being in advance (leading) the others, depends on two factors: the delay entity and the jitter entity. As shown in Fig. III-12, these two probabilities correspond to two points on the jitter CDF from which the RMS of jitter can be calculated. The RMS jitter may be derived from the delay difference $\Delta d = d_1 - d_2$ and the two probabilities p_1 and p_2.

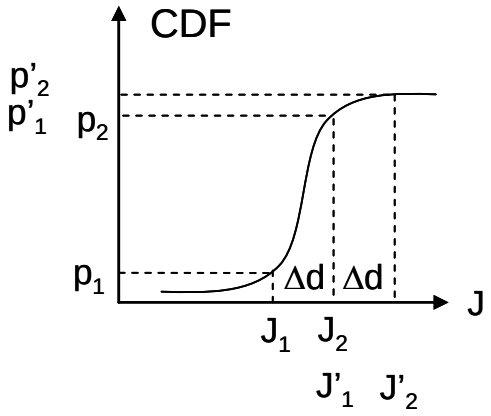


Fig. III-12. Extraction of RMS Normal jitter from its CDF

Since these two probabilities can be calculated with a simple BIST circuitry described below, J_1 and J_2 are thus known, as well as Δd (there is no need to know the absolute values of d_1 and d_2), and the relationship $J_i = d_i - T_{id}$ stands. Resolving for x_1 and x_2 the relations $F_X(x_1) = p_1$ and $F_X(x_2) = p_2$, where $F_X(x)$ is the normalized Normal CDF and since $\Delta J = \Delta d$, the RMS jitter may be evaluated as:

$$J_{RMS} = \frac{\Delta d}{x_1 - x_2} \tag{III-6}$$

Almost the same J_{RMS} result would have been obtained using p'_1 and p'_2 with the corresponding J'_1 and J'_2, but probably with less measurement accuracy since, according to [17], measurement accuracy is maximum for values of delay centered on the CDF and specifically: $d_1 = T - J_{RMS}$ and $d_2 = T + J_{RMS}$.

The BIST circuit that realizes the two delays is depicted in Fig. III-13 and does not differ much from the one described in Fig. III-9. Here, the adjustable delay can take two values d_1 and d_2, the inverter in calibration mode forms a ring oscillator whose oscillation period is measured by a counter, the phase comparator determines if the rising edge of *SUT* leads or lags the one of *SUT'*, and the counter measures Δd in calibration mode and the number of times *SUT* leads *SUT'* in measurement mode.

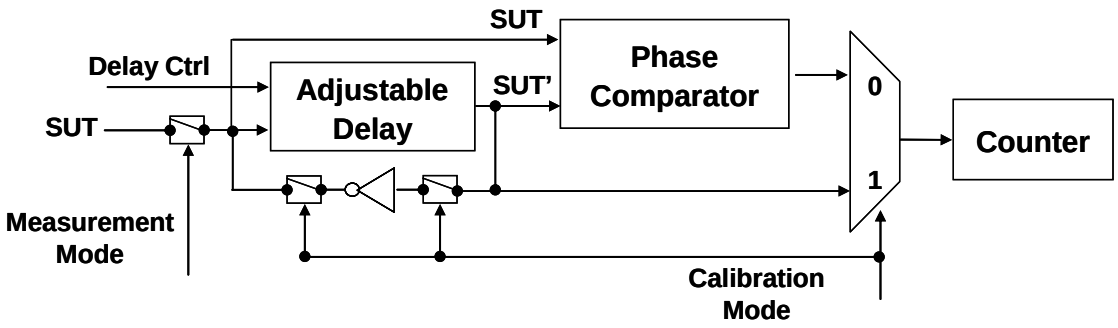


Fig. III-13. BIST circuit for RMS jitter measurement

3.3.3 Jitter Measurement Using Undersampling

Recent works by Sunter, Roy, and Côté [1], [21] present the ULTRA technique, based on the undersampling technique already proposed by Huang in [20]. This technique is capable of evaluating jitter with subpicosecond resolution. The authors acknowledge the fact that the previous techniques for jitter measurement would not allow obtaining a precision better than 1% of the unit interval (UI) which is the precision requested for the test of multi-gigabit data transfers. The principle of undersampling is depicted in Fig. III-14.

The data is serially transmitted at a data rate f_d. In common data recovery applications this data is sampled by the receiver at an exactly equal rate using a clock recovered from the data by the PLL of the receiver. In the ULTRA technique for jitter measurement applications, the data is also undersampled at a rate f_s, slightly lower than the transmitted data rate f_d. This means that if, for example, the data is sampled at $f_s = 0.99 \cdot f_d$, then the resolution of the jitter test is 2 % of the UI[1] regardless of the frequency, where UI is equal to half the data rate period $T_d/2$. Sampling the data flow at a rate slightly lower than the data rate produces a signal at a much slower frequency f_b, called beat frequency. This occurs because the sampling rising edge of f_s will sample a series of the same logic level of the data signal before switching to the other logic level of the data signal, since the two frequencies f_s and f_d are very close to each other. The presence of jitter makes the data rising edges vary relatively to its average position. This

[1] and not 1 % as stated in [21]: to obtain a 1 % of UI the sampling frequency must be $f_s = 0.995 \cdot f_d$

engenders the so called unstable bits (represented in dotted line in Fig. III-14) around the rising and falling edges of f_b, since f_s is sampling around rising or falling edges of f_d that vary because of jitter. The sum of all the groups of these unstable bits allows the evaluation of the CDF of the jitter from which its PDF can be derived. Many groups of unstable bits are necessary to deduce the jitter entity with sufficient accuracy [28].

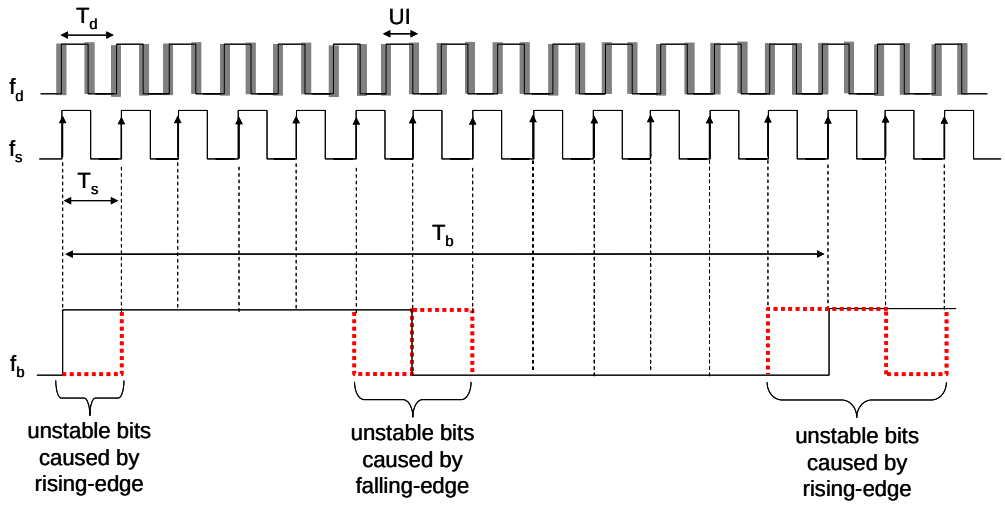


Fig. III-14. Undersampling principle

The BIST circuit that realizes this jitter measurement is shown in Fig. III-15. This technique needs a second PLL or a second clean reference to generate f_s, since this is different from f_d of the PLL under test and a fast D-FF to sample at a frequency of f_s (used as clock) that may easily amount to more than ten GHz! Such a fast flip-flop is obviously subject to metastability issues (see [22], [23], [24], and Appendix 4).

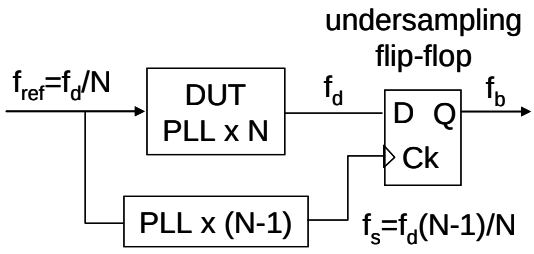


Fig. III-15. Undersampling in the ULTRA module

The output of the sampling latch is conveyed to a jitter analysis circuit which calculates the jitter properties. The analysis circuit, which is a single-clock finite state machine, monitors the signal samples and, when a transition is detected after many same-value bits, captures the unstable bit regions that are caused by jitter.

3.3.4 Jitter Measurement Using Vernier Delay Lines

Vernier Delay Lines (VDL) are based on a principle of measurement invented in 1631 by the French mathematician Pierre Vernier (1580-1637). As in Vernier calipers, this principle consists of delaying both the clock signal and the signal under test by means of delay chains constituted of slightly different delay elements in order to obtain sub-gate resolution. Otherwise, with one simple delay chain on one of the two signals, the resolution would be limited to gate delay, which is technology dependent.

The symbols τ_f and τ_s in Fig. III-16 (a) are the respective propagation delays of the buffers interconnecting each stage of the VDL. Since the propagation delay elements of the clock, τ_f, and of *SUT*, τ_s, differ by an amount $\Delta t = \tau_s - \tau_f$, the time difference between the rising edges of *SUT* and of *CLK* will decrease by Δt after each stage of the VDL. The phase relationship between the rising edges of the two signals at the output of each stage is detected and recorded by a corresponding D-FF. A logical low output will result when *CLK* leads *SUT*, whereas a logical high output will result when *SUT* leads *CLK*. The output of each D-FF is passed to a counter circuit, which simply counts the number of times *SUT* leads the *CLK* (i.e., the number of logical 1's) with a delay difference set by its position in the VDL. As the phase difference between *SUT* and *CLK* at the input of the VDL is a random variable due to jitter present in *SUT*, each time the measurement is performed, a different set of D-FFs are set to a logical high level and the corresponding counters begin to register different values. In the case of the first counter, its count value reflects the number of times the rising edge of *SUT* is ahead of the rising edge of *CLK* with a delay greater than Δt. Likewise, the counter in the next stage will correspond to the number of times the rising edge of *SUT* leads the rising edge of *CLK* with a delay greater than $2\Delta t$. Subsequently, the following stages

correspond to the number of times *SUT* leads *CLK* by $3\Delta t$, $4\Delta t$, and so forth. As an example, the timing relationship between *SUT* and *CLK* is shown in Fig. III-16 (b). In this case, three delayed versions of *SUT* are sampled simultaneously by three delayed versions of *CLK*, resulting in subgate timing resolution. Statistically, the various count values can be collected and used to create a CDF of the jitter present in *SUT* [30].

3.3.5 Jitter Measurement with a Component-Invariant VDL

Since the issue of delay elements being process dependent stands and is of great relevance for VDLs, a component-invariant VDL has been proposed in [30] for jitter measurements purposes. This technique aims at minimizing the number of delay elements and counters needed for jitter measurements.

As previously stated, the original VDL design is sensitive to component mismatches in the delay elements due to process variations. By using only one delay element repetitively, the problem of matching different stages is eliminated and the process deviation issue can be reduced to the calibration of a single element. Such an approach is achieved by modifying the circuit in Fig. III-16 (a) to obtain the component-invariant VDL structure shown in Fig. III-17. In this circuit, inverters instead of buffers are used as delay elements. In addition, when the switches are closed, the two inverters are configured in a ring oscillator structure each oscillating at two different periods of $2\tau_s$ and $2\tau_f$, depending on the propagation delay of the inverter. More importantly, each inverter circuit will delay the rising edge of *SUT* with respect to the rising edge of *CLK* by an amount $2\cdot(\tau_s - \tau_f)$ or $2\Delta t$ for every cycle of the input clock signal.

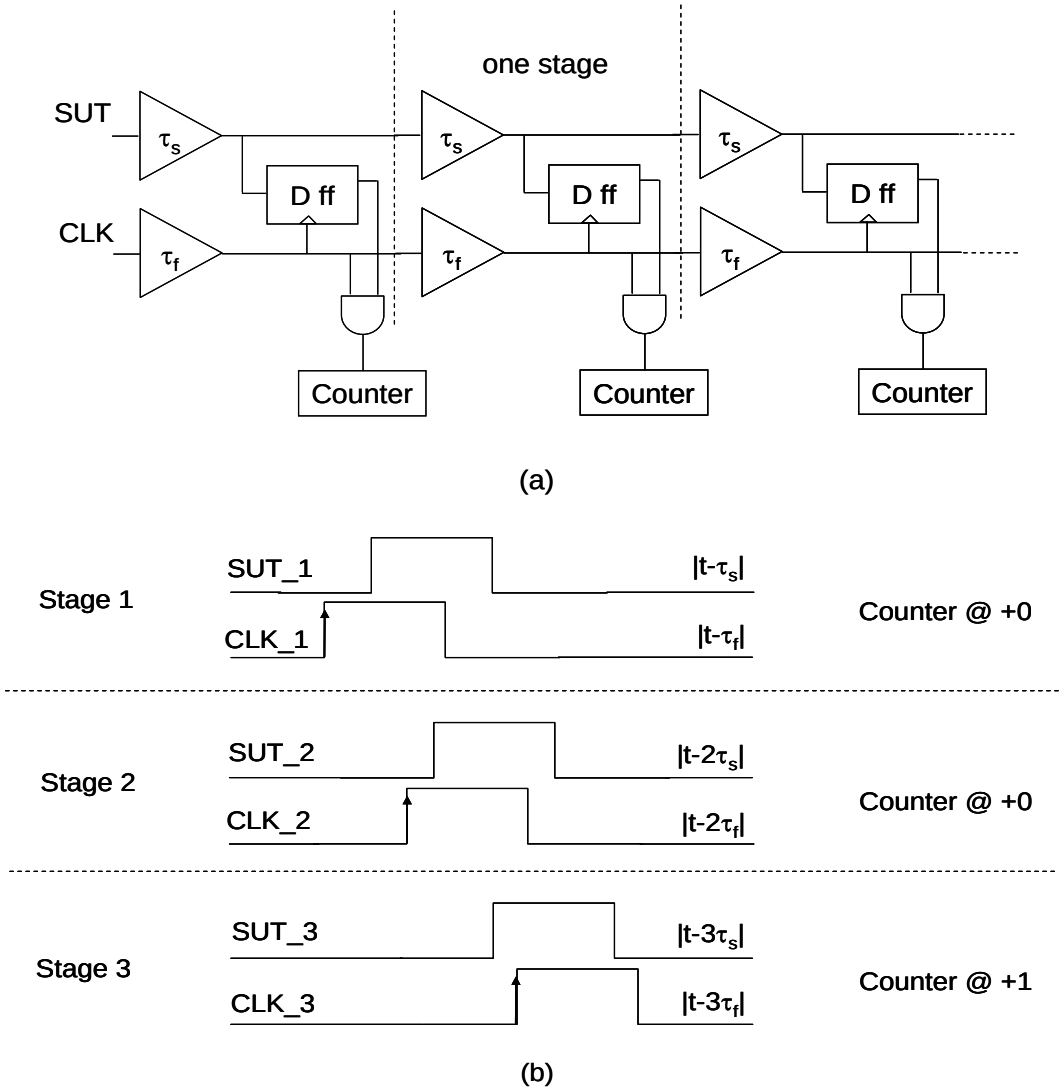


Fig. III-16. Vernier Delay Line (a) schematics (b) chronogram

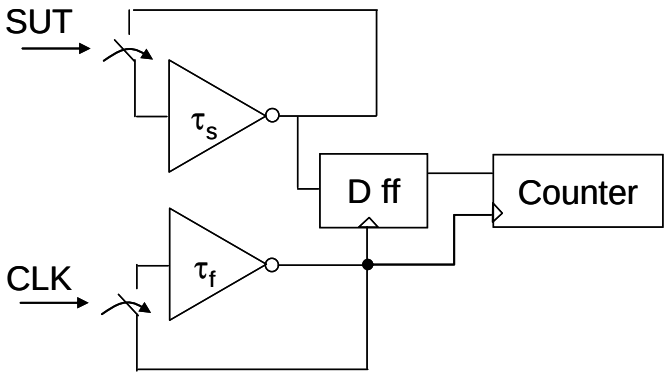


Fig. III-17. Component-Invariant Vernier Delay Line

This configuration also solves the problem of having to use a large number of counters. Assuming that the period, *T*, of *SUT* and *CLK* is larger than the total propagation delay, then the total count of logical high levels at the D-FF output represents the actual time difference between the rising edge of *SUT* and *CLK* taken at a particular instant in time. This is easily achieved by counting the number of logical high levels over the time period *T*. Repeating the measurement *N* times enables a histogram of the jitter signal to be constructed.

3.4 PLL Defect-Oriented BIST Techniques

Some other techniques for PLL testing do not provide jitter measurements and are mainly based on opening the loop to inject test vectors and observing the open loop behavior [34], [35]. These techniques have the advantage of being completely digital and the disadvantage of not considering jitter measurement or correlation of test measures to DUT performances at all.

On the other hand, these works provide the catastrophic fault coverage of the BIST applied to a PLL. All results though are not experimental but originated by fault injection simulation. The author completely understands and shares the great issue of obtaining experimental results, since a massive amount of devices is required to constitute a valid statistical population for BIST evaluation.

Since jitter measurement is becoming a progressively complex task to achieve with the constant increment of frequency operation, some works direct research towards different alternatives in an attempt to avoid increasing precision for measuring jitter. In fact, although the techniques illustrated in the former section seem promising and the idea behind is clever, their real performance as BIST techniques have not been supported by much experimental proof nor even evaluated with some acknowledged method, as the one presented in section 3.2, for example. In this section some of non jitter-based techniques are discussed. Contrary to the ones seen before, these works

provide catastrophic fault coverage of their BIST technique. It is unfortunate that no study on test measures correlation with the PLL performances has been carried out.

3.4.1 Charge-based Frequency BIST

In 2000 [34] proposes a BIST technique based on the simple general method illustrated in Fig. III-18, where *I* is a constant current source used as input stimulus for the DUT, *V* is the output voltage of the DUT that is analyzed by a signature evaluation circuit at the output of the DUT.

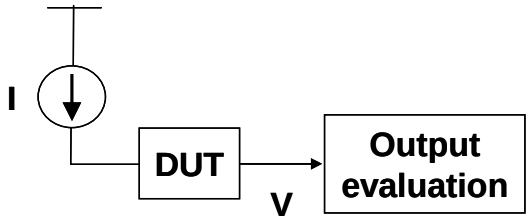


Fig. III-18. Simple general concept of BIST

The DUT is an analog circuit with low input impedance. The output is typically a voltage multiple of the input current through the impedance of the DUT, thus, any change of impedance due to faults in the DUT, physical faults included, will yield a change in the output signature.

In the case the DUT is a PLL, the current source is already present and is represented by the CP. This grants two advantages:

- no introduction of a specific current source is necessary, with the consequent die area overhead saving,

- LF input is not loaded by any circuit insertion with BIST purposes since the CP here serves as BIST circuit but is also part of the PLL. It is known in fact that probing analog nodes in a PLL may impact its whole operation mode [35],

- the CP is tested at the same time as the rest of the blocks, saving overall test time by performing a single test for multiple blocks.

The DUT thus is, in this case, the LF block and the evaluation block is made up of the combination of the VCO, the divider by N and the controller&grabber blocks. The VCO picks up the voltage at the LF output and passes it in form of frequency to the divider that provides a digital signature to the controller&grabber block as shown in Fig. III-19. The advantages of using the existing VCO and divider by N as a measuring device are:

- no introduction of a voltage detector is needed, with the consequent die area overhead saving,

- the VCO and divider blocks are tested at the same time as the LF and the other blocks, saving overall test time by performing a single test for multiple blocks,

- the VCO is tested without any probing at its analog RF sensitive output.

This BIST technique has been named CF-BIST, which stands for Charge-based Frequency BIST.

A multiplexer (MUX) is inserted at the PD output to control the insertion of input stimuli in the LF. In PLL standard operation mode, the MUX is set to pass the output signals of the PD. In test mode, the MUX provides the control signals at the CP input through the controller&grabber block. The VCO will thus oscillate according to the voltage at the LF output and the divider will work as a frequency counter and its digital output signature is stoked in the controller&grabber block. This digital data may either be tested on-chip by a scan chain or passed on to a low-cost digital tester. Faults in the CP, LF, and VCO, in fact, all affect the oscillation frequency, whose deviation from the nominal value clearly indicates the presence of a faulty block in the PLL.

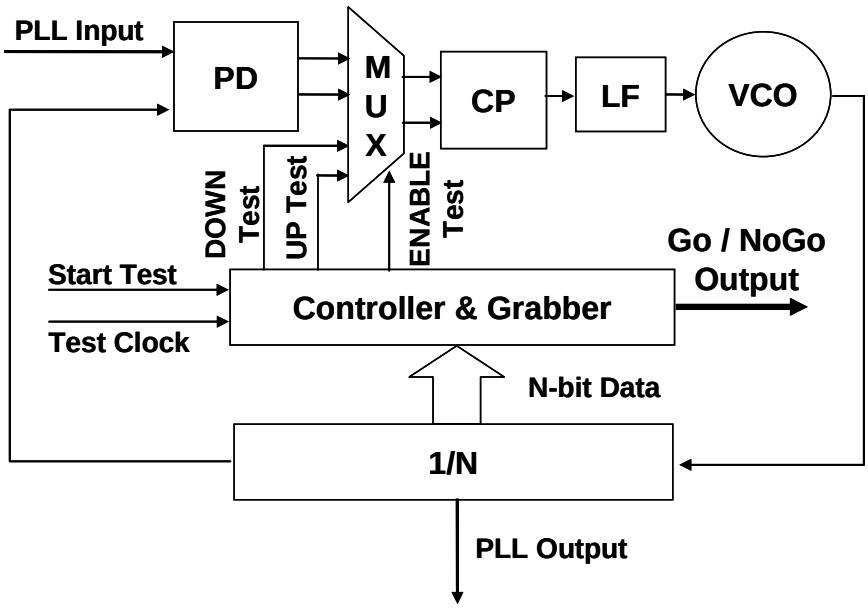


Fig. III-19. CF-BIST technique

The major advantage of this technique is that it uses mostly existing blocks for BIST purposes, thus minimizing the area overhead and avoiding probing sensitive nodes. Furthermore, the test output is digital and can be easily and cheaply tested by means of a low-cost digital tester alone or by an on-chip scan chain, saving time and tester resources. The controller&grabber plus MUX blocks are, in fact, the only BIST blocks, they are completely digital and occupy very little area overhead. The limitations of this work are that the technique does not allow identifying which block of the PLL is the faulty one, although this is not a requested feature in production test, and that it considers only structural catastrophic faults and not parametric faults. As stated before, the study does not explore correlation between chosen test measures (which consist in measuring output frequency for different values of the tuning voltage at the VCO input, V_{tune}) and PLL performances (such as phase noise, VCO gain, spectral purity etc.). Moreover, no information on test metrics such as yield loss or defect level is given. According to the authors, the catastrophic fault coverage attained by simulation is very high, 96.5 % over 395 faults injected, consisting in opens and shorts at each component node.

3.4.2 PLL DfT: Structural Test of the Building Blocks

A DfT technique for PLLs which focuses on catastrophic fault detection by means of the "divide and conquer" principle is presented in [36]. This principle consists in partitioning the circuit in different functional blocks and applying a specific test for each block. The intent is to implement very simple digital test strategies for each block in order to be able to carry out the PLL test on a standard digital tester.

Fig. III-20 shows the DfT applied to a PLL. The functional blocks consist in the PD, the CP and the LF together, and the VCO which needs to be reconfigurable for DfT purposes. The test of each functional block is described in the following sections.

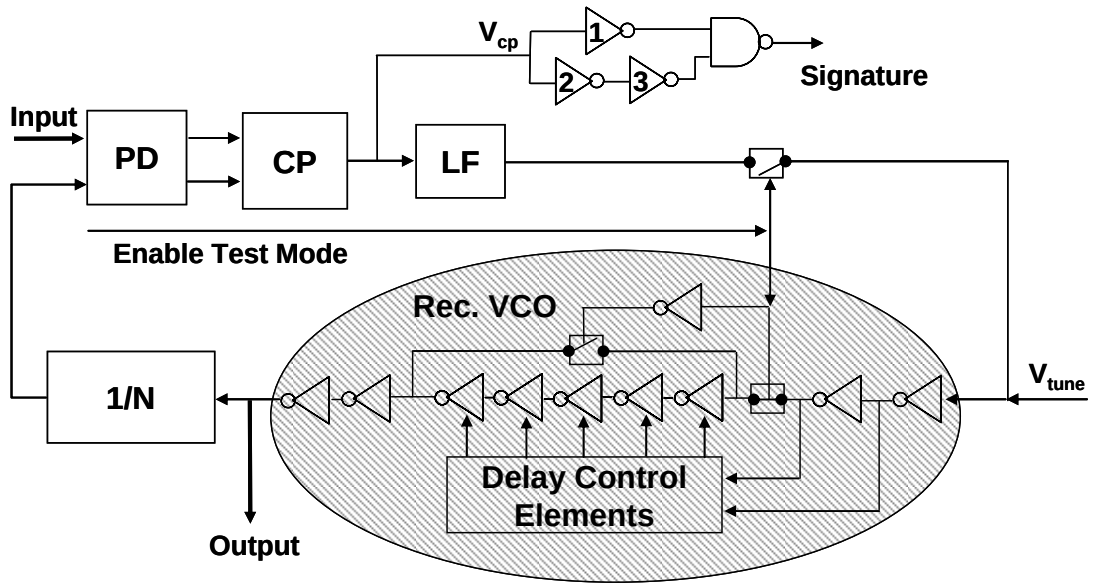


Fig. III-20. PLL DfT: structural test of the building blocks

The phase detector is a typical digital three-state PD (logic high and low levels and high impedance) which can be easily tested by means of existing digital test techniques. The most common one is a Boolean test where a simple sequence of logic levels is introduced in input and the state of the primary outputs of the PD is verified. The input test vectors may either be made up of an ad hoc sequence, or be generated by an automatic test-pattern generator to search for specific structural faults.

The test of the CP and LF is more complicated to carry out since they represent the interface between the digital and the analog parts of the PLL. In fact, the CP converts the logic states of the PD in a ternary sequence which is then transformed in an analog voltage by the LF. This is why a digital test does not directly apply to these blocks without adding extra circuitry that allows generating a digital signature. This circuitry encodes the two logic states (high and low) of the ternary signals at the CP output with the same logic level high. This can be done without risk of ambiguity since to pass from a logic level to the opposite at the CP output, it is necessary to pass through the high impedance state. The working principle of this comparator circuit is better illustrated in Fig. III-21.

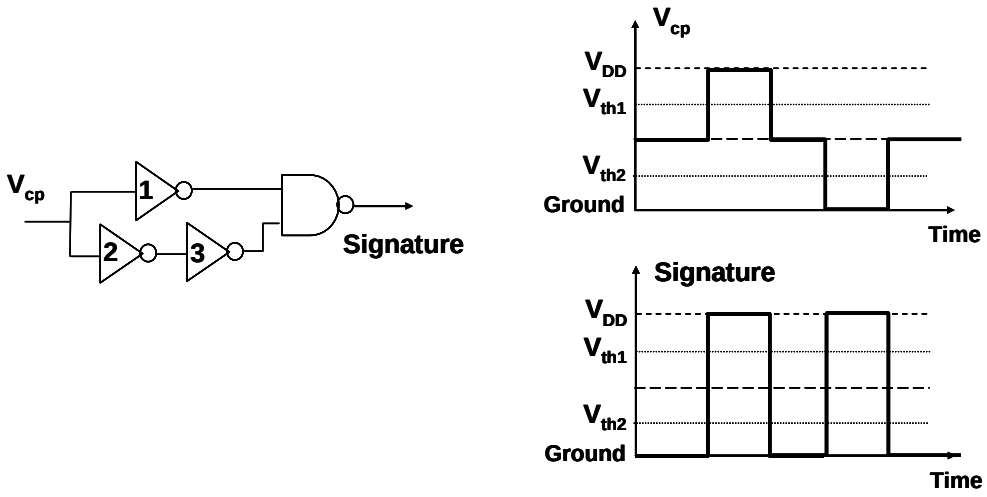


Fig. III-21. Digital signature generation

The DfT circuit is applied at the CP output and encodes in a binary sequence the ternary sequences issued from the CP after the insertion of test vectors that engender all three possible states at the output in order to accomplish the complete test. The binary sequence generated by the DfT circuit may then be passed on to a digital tester that compares the output signature with the golden one.

The author is not yet convinced of how (and if) this kind of DfT allows also the LF test. The authors of [36] do not give further detail on the LF test.

Also the VCO is part of the interface stage between analog and digital parts of a PLL. The same issues for purely digital testing faced for the CP are common to the VCO too. Thus, also for VCO some extra circuitry is needed to allow simple digital testing. The idea is to introduce a test mode which consists in opening the PLL loop and the ring oscillator loop allowing to treat the VCO as an inverter chain. Two switches in the VCO, one in the loop of the ring oscillator and another in input, as in Fig. III-22, will serve the cause. Once opened the PLL loop in test mode, the node V_{tune} remains floating (see the complete schematic in Fig. III-20) and is therefore connected to a control type input to test the inverter chain with a digital input sequence. Testing the logic functionality then simply means verifying that a logic 0 applied on the input causes a logic 1 at the output, and vice-versa.

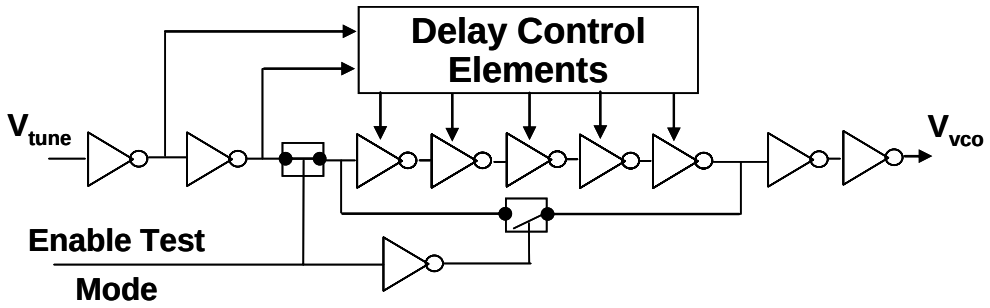


Fig. III-22. Reconfigurable VCO

This DfT technique has to be thought stating from the design stage as it may impact deeply and in different ways the operation mode of the PLL. First, loading the CP output with extra circuitry needs to be considered for specifications fulfillment. Second, the VCO needs to be designed in a reconfigurable mode and has to be an inverter chain ring oscillator type. The author wonders how to reconfigure an LC tank oscillator for test purposes and if this would not also be critical for performances degradation. In general, not loading the CP output in RF PLLs applications is strongly recommended since variations of this load and the parasitic capacitances may vary CP currents adding mismatch and leakages, thus degrading performances such as spectral purity (see section 2.3.2). In [36] a study of the gain degradation due to DfT insertion after design stage has been carried out. Here again, as for the other techniques seen up to know, no

test metric is given, nor any evaluation of the technique except for catastrophic fault coverage obtained by fault injection simulation. The authors of [36] claim that the test detected 224 out of 254 faults in simulation, corresponding to an overall catastrophic fault coverage of 88.2 %. The 30 undetected faults include 19 for the VCO, 10 for the PD, and one for the CP and LF block. The DfT implementation, although delicate for performances degradation issues, is simple and occupies little area overhead.

3.5 Conclusions

The approach that has been followed in this work wants to take the pros of the techniques discussed above trying to avoid the cons, discussed in each related paragraph. Therefore, a DfT technique aiming at a structural test of the building blocks of the PLL has been chosen as in [36], avoiding reconfiguring the building blocks, though. Moreover, this work did not want to neglect jitter measurement as in the PLL functional BIST techniques previously discussed. The suggestion of measuring jitter proposed in [21] is without doubt to be kept into consideration. Nevertheless, this technique requires a clean reference at high frequency (close to the PLL output frequency) which represents one of the major limitations of this BIST technique. This technique also owns a patent, which means that royalties must be paid to use it; this is why industries are exploring other options, hence the aim of this work. Since direct jitter measurement at the PLL output is destined to become unfeasible due to ever increasing frequency, some jitter-related measurements have been introduced in the technique proposed in this work, studying also the correlation with jitter and other performances non-measurable on-chip. Vernier delay lines have also been employed in this work, but not directly at the PLL output, in order to avoid metastability on the flip-flops due to high frequency. An added value given in this work with respect to the previously mentioned ones is a complete analysis of the test metrics of test measures and the full generalized methodology to evaluate them.

Chapter IV

Statistical Model of the PLL

4.1 Introduction

The approach considered for the PLL case-study has been to study and model in particular its analog blocks which were of an interest to this work, such as the VCO and the CP. A complete simulation of the PLL as a whole at component level in order to model its behavior was not a viable option due to simulation duration.

In order to build a statistical model of performances and test measures of each block of the PLL, a population of 1000 VCOs and 100 CPs has been generated by Monte-Carlo simulation under process and mismatch deviations. Unfortunately, it has not been possible to generate more samples for the CP due to time consuming simulation issues that will be discussed in detail in section 4.4. Nevertheless, a study on a statistical model built from a small population of the VCO (300 Monte-Carlo iterations) and the larger population of 1000 VCOs demonstrated that the difference between the two generated models was not significant. This will be explained in section 4.3. Of course, extending this theory to the CP block is quite a stretch, since the two blocks are different. On the other side though, the VCO block is the most sensitive to process deviations, so if a small population is good enough for the VCO, it should be safe to believe it is good enough for the CP also. The joint PDF of performances and test measures has then been estimated using the Copulas-based method. This PDF is next sampled in order to generate a bigger population of each block under test (one million instances).

4.2 The Test Vehicle PLL

The need of an industrial PLL test vehicle has strongly conditioned this work due to the complexity of such devices. At first a Bluetooth PLL had been chosen, but after an accurate analysis of this device, it has proven to be too complex and probably not robust enough for this work's purposes. Thus, a simpler, more robust, and smaller RF SERDES PLL has been chosen as test vehicle for this work. This PLL can work at 7.5 GHz or 9 GHz, according to the switching on or off of the capacitors of the varactor in the VCO. The PLL has been designed and manufactured in CMOS065 RF LP technology at STMicroelectronics. The total surface occupation of the IP is 300 μm * 340 μm = 0.102 mm^2, thus much smaller than the previous one considered. An overall schematic is shown in Fig. IV-1 (as in design review documentation).

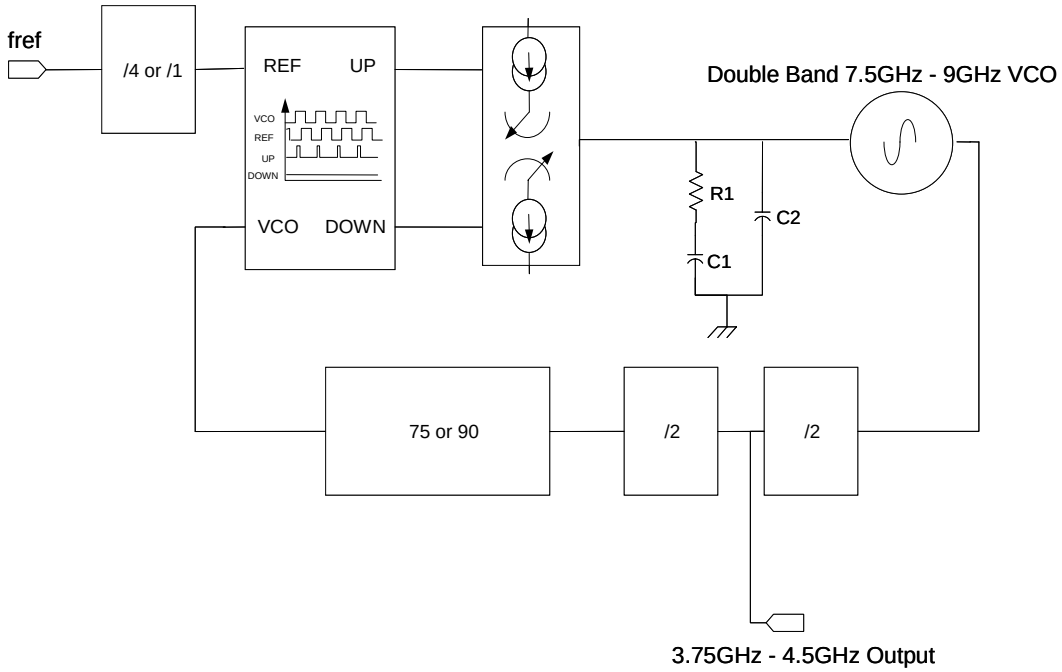


Fig. IV-1. SERDES PLL schematics

The PLL output is taken after division by 2. Its reference frequency may be either 100 MHz (25 MHz after division by 4 as in Fig. IV-1) or 30 MHz, depending on the reference clock present on-chip. The LF is a completely integrated second order low pass filter. Its VCO is an LC tank type with two possible configurations of the varactor

which allow different output frequency ranges. This is why the divider is also configurable on a division by 75 or by 90. The VCO has a free running frequency of 6.9 GHz to 8.9 GHz or 8.3 GHz to 10.3 GHz, with a gain K_{vco} of 0.4 GHz/V to 1.7 GHz/V, a bandwidth of 100 kHz, and phase margin of 55°.

PFD and CP blocks are driven by a Vdd = 2.5 V, while the VCO and the Divider by N are driven by a Vdd = 1.2 V. All BIST monitors also work at Vdd = 1.2 V.

4.3 Statistical Model of the VCO

To build a statistical model of a block, in this case the VCO, it is first necessary to define a set of performances, if not already specified by datasheet. Next an analysis through simulation of these performances is considered.

4.3.1 VCO Performances and Test Measures

Typical performances of a VCO are phase noise (given in dBc/Hz), current consumption, output frequency for different values of V_{tune}, and gain (which is the derivative of the output frequency with respect to the input voltage and is given in Hz/V). All of these have been considered in the analysis of the VCO under study. Some other performances may be specified in the datasheet, such as power consumption, but this was not the case for this particular case study.

4.3.2 Simulation of the VCO

Simulations for validation of the VCO in the 7.5 GHz operation mode have been carried out. Fig. IV-2 shows (a) the output frequency and (b) the gain for different values of input voltage, where the VCO gain K_{vco} is the derivative of the output frequency with respect to the input voltage V_{tune}. The specification range for V_{tune} is between 0.4 V and 2 V. Here, only the 7.5 GHz operation mode configuration is reported (the 9 GHz has been omitted) since it is the one used for BIST validation. In fact, in this configuration

all the capacitances of the varactor must be activated, allowing a more comprehensive test on all components.

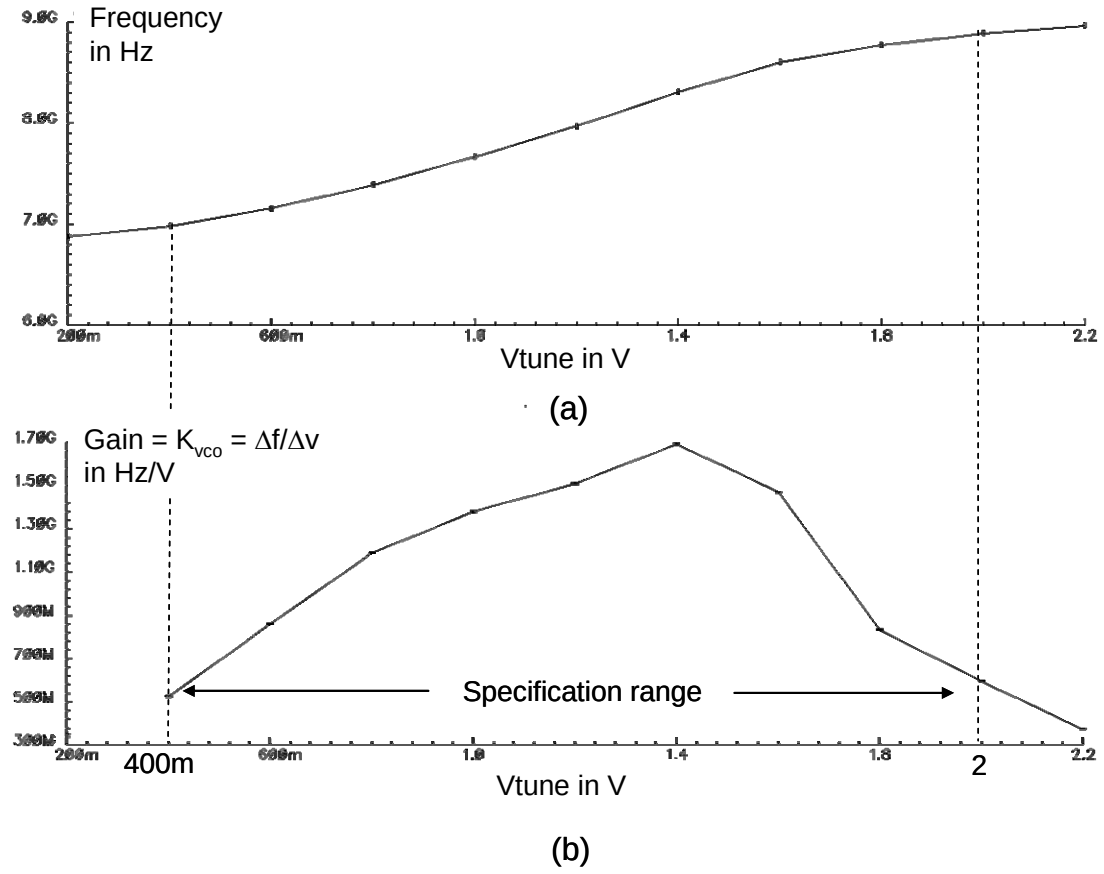


Fig. IV-2. VCO (a) output frequency and (b) gain

4.3.3 Copulas-Based Statistical Model of the VCO

An initial population of the VCO block is first generated using Monte-Carlo simulation. An accurate estimation of test metrics for the VCO cannot be obtained using only results from Monte-Carlo simulation, since only a limited number of circuit instances can be generated in a reasonable amount of time including very few if any faulty devices. In order to have a representative population, a probability density estimation technique will be used. The joint PDF of the VCO performances and test measures is obtained from the initial Monte-Carlo instances using Copulas theory as given in [49].

This statistical model is next sampled in order to generate one million instances. Other density estimation techniques may be employed, including normal multivariate density estimation [48] and kernel-based density estimation (KDE) [6]. In this work, Copulas theory has been applied since the original data did not follow a multinormal distribution and the number of performances and test measures may be too large to use a KDE technique while keeping good accuracy. On the other hand, the original data approximated reasonably well a Gaussian copula as described below.

A first Monte-Carlo simulation with 300 iterations has been run on the VCO block, obtaining the initial population depicted in Fig. IV-3 (a), where *PN* stands for Phase Noise, *OF* for Output Frequency, *CC* for Current Consumption, and V_{alc} for the peak to peak output voltage. The Copulas-based statistical model has been calculated from this population. Next, the model is sampled to generate a large number of instances. Clearly, the statistical model depends on the size of the initial population. In order to see the effect of the size of the initial population, a second Monte-Carlo simulation has been run, this time with 1000 instances. While the Monte-Carlo simulation of 300 instances lasted approximately 18 days on a cluster of dedicated workstations, the simulation of 1000 instances lasted approximately two months. This gives an idea of how time consuming Monte-Carlo simulations may result.

Fig. IV-3 (b) shows the initial population of 1000 instances. Comparing Fig. IV-3 (a) and (b), it may be noticed that the bivariate distributions of performances and test measures are quite similar. For the VCO the initial population of 1000 instances will be used, since, although very alike, the more initial instances are taken, the more precise the statistical model. However, for the case of the charge pump considered later in this chapter, the analysis will be limited to 100 samples for simulation time reasons.

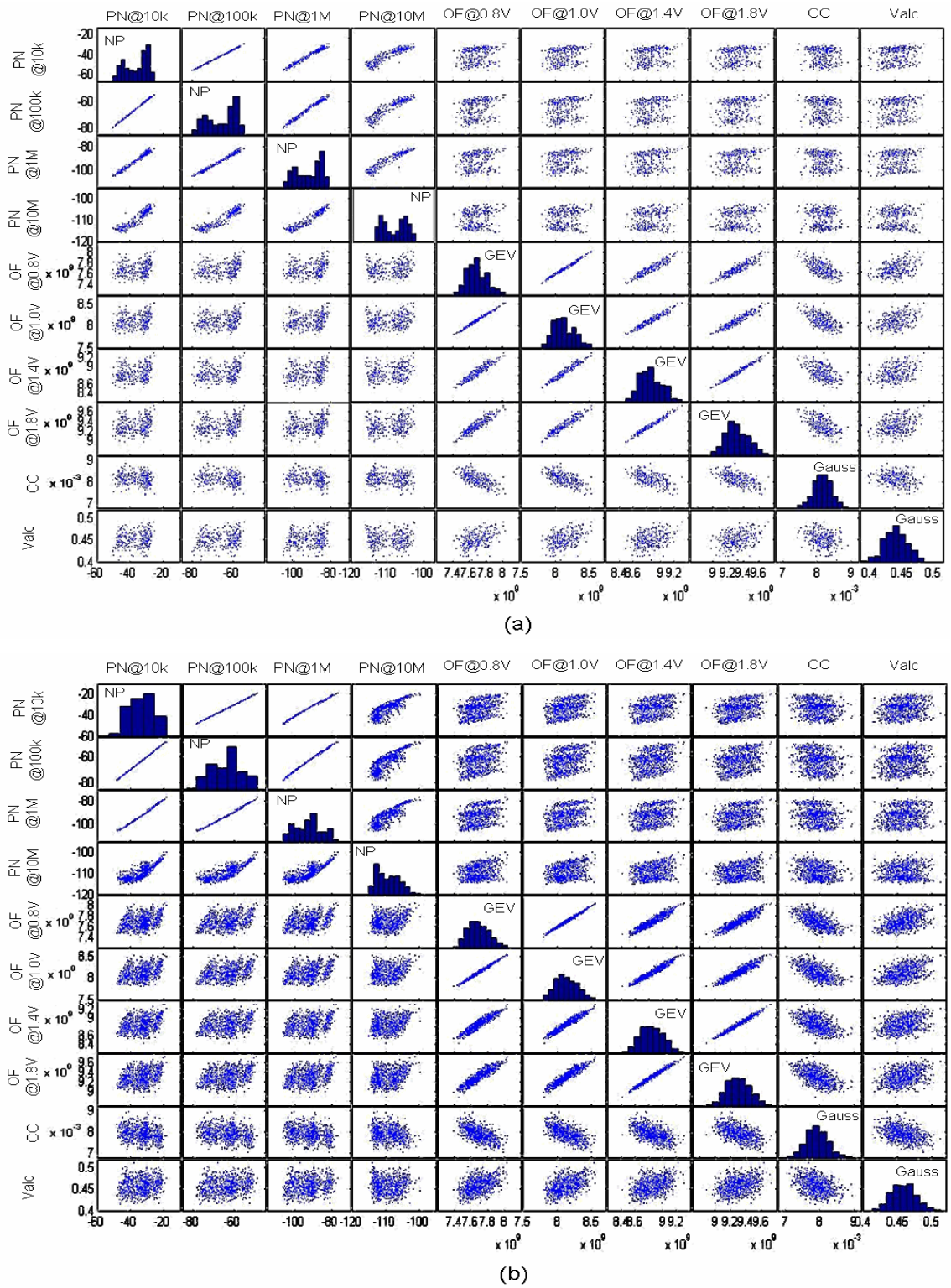


Fig. IV-3. Samples of the VCO performances and test measures obtained from the electrical Monte-Carlo simulation (a) 300 instances and (b) 1000 instances

The Copulas model requires an estimation of the marginal CDF of each performance and test measure and of a multivariate CDF, called a copula, which estimates the relations between the marginals.

The marginal CDFs can be easily estimated from the original data using well known univariate laws or KDE techniques. Tab. IV-3 gives the statistical parameters of each performance and test measure along with the type of estimated PDF and the required parameters. Gauss stands for Gaussian distribution, which requires the mean value μ and the standard deviation σ. GEV stands for General Extreme Value distribution. This kind of distribution needs three parameters, the mean value μ, the standard deviation σ, and the shape parameter k. NP stands for Non-Parametric distribution obtained with a KDE method. The window parameter (width) is necessary to define this distribution. The mean value μ and the standard deviation σ are not parameters of this type of law, they are given in Tab. IV-3 for completeness.

Perf/TM	**Dist**	**Parameters**			
		μ	**σ**	**width**	**k**
PN@10kHz	NP	-33.7 dBc/Hz	7.01 dBc/Hz	1.99 dBc/Hz	-
PN@100kHz	NP	-63.6 dBc/Hz	6.91 dBc/Hz	1.98 dBc/Hz	-
PN@1MHz	NP	-92.6 dBc/Hz	6.92 dBc/Hz	1.97 dBc/Hz	-
PN@10MHz	NP	-109 dBc/Hz	3.12 dBc/Hz	1.01 dBc/Hz	-
OF@0.8V	GEV	$7.69 \cdot 10^{9}$ Hz	$1.20 \cdot 10^{8}$ Hz	-	-0.20
OF@1V	GEV	$8.13 \cdot 10^{9}$ Hz	$1.48 \cdot 10^{8}$ Hz	-	-0.20
OF@1.4V	GEV	$8.84 \cdot 10^{9}$ Hz	$1.53 \cdot 10^{8}$ Hz	-	-0.23
OF@1.8V	GEV	$9.30 \cdot 10^{9}$ Hz	$1.44 \cdot 10^{8}$ Hz	-	-0.24
CC	Gauss	$7.92 \cdot 10^{-3}$ A	$2.97 \cdot 10^{-4}$ A	-	-
Valc	Gauss	$4.58 \cdot 10^{-1}$ V	$1.65 \cdot 10^{-2}$ V	-	-

Tab. IV-3. Fitted distributions of performances and test measures of the VCO

Fig. IV-4, Fig. IV-5, Fig. IV-6, and Fig. IV-7 show, respectively, the marginal PDF and CDF for phase noise measurements, output frequency, current consumption, and output peak-to-peak voltage. The estimated density can be compared with the histogram and the CDF of the initial data.

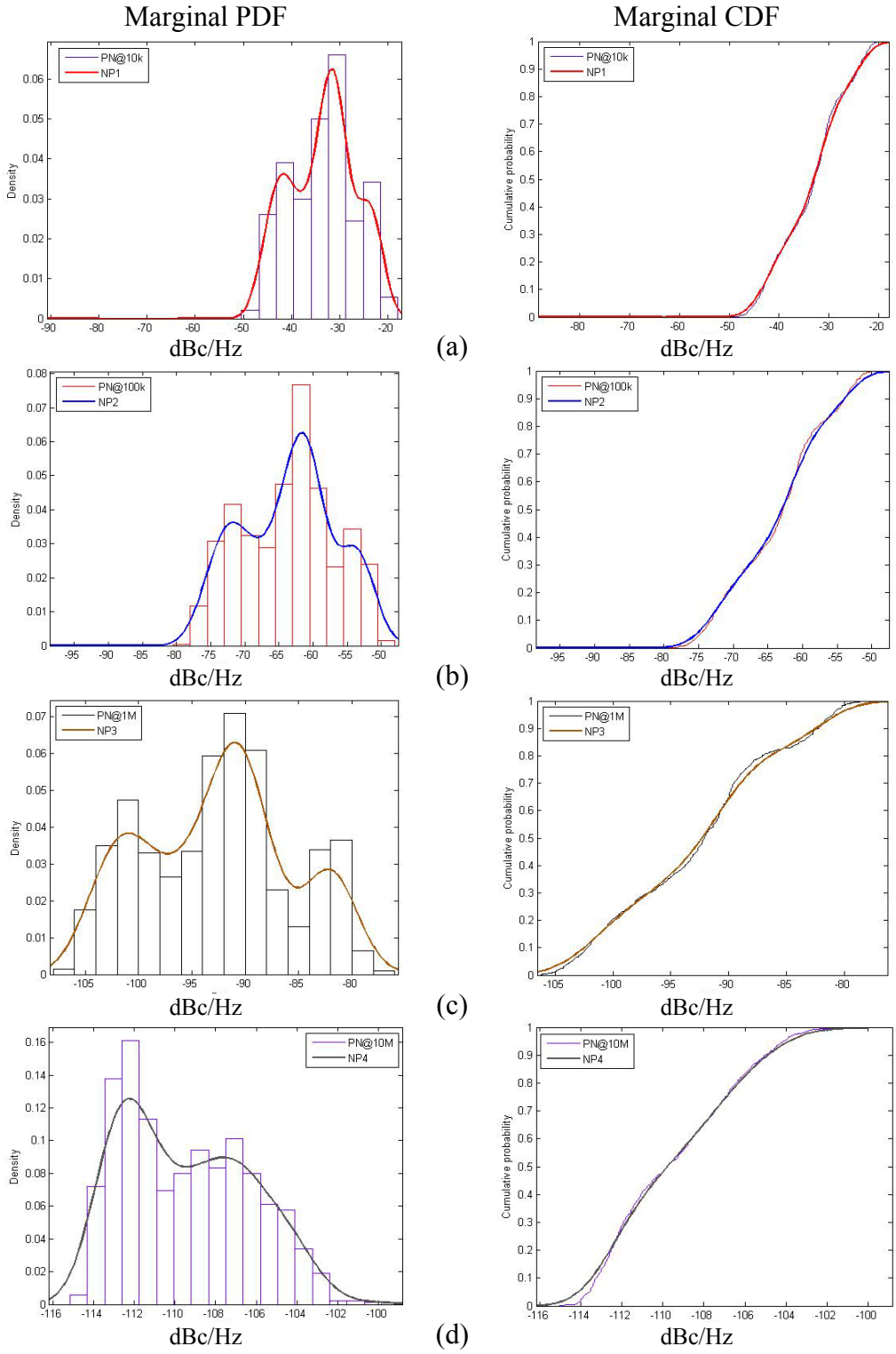


Fig. IV-4. PDFs and CDFs of phase noise at different values of frequency from the carrier

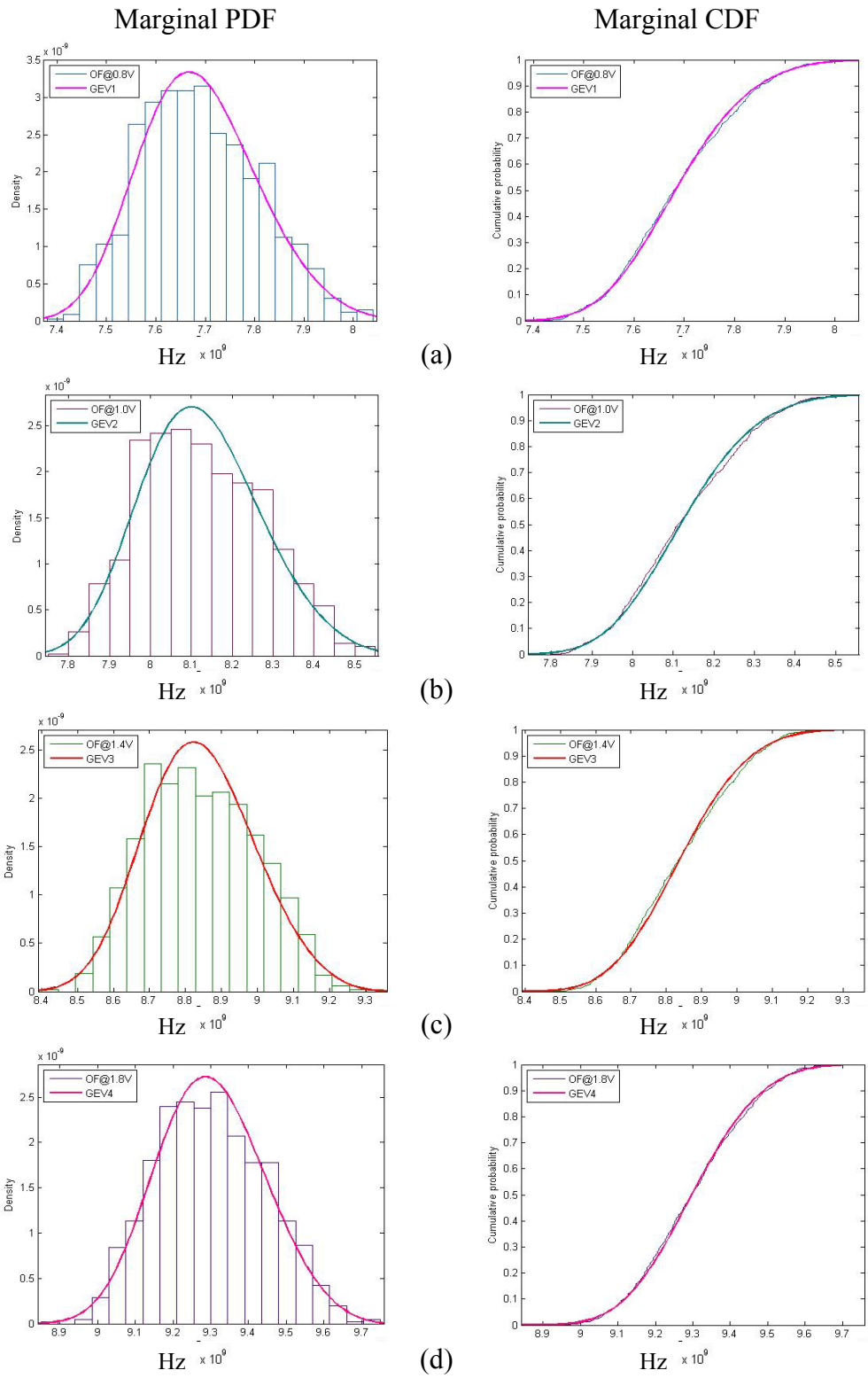


Fig. IV-5. PDFs and CDFs of VCO output frequency at different values of V_{tune}

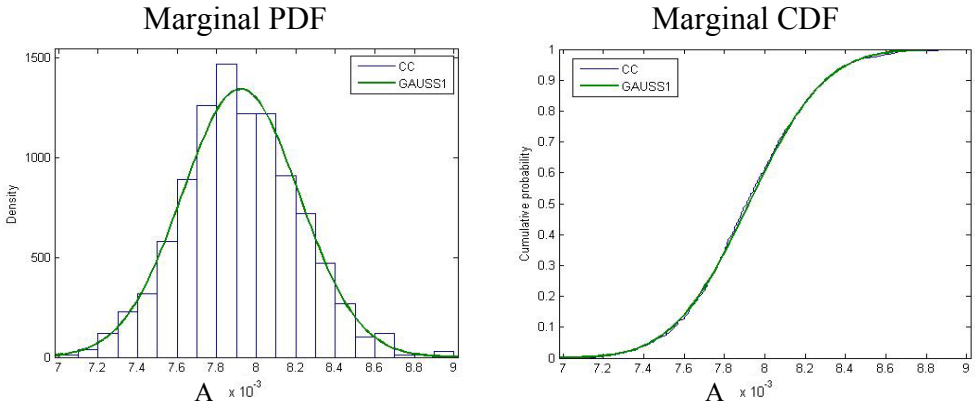


Fig. IV-6. PDF and CDF of current consumption

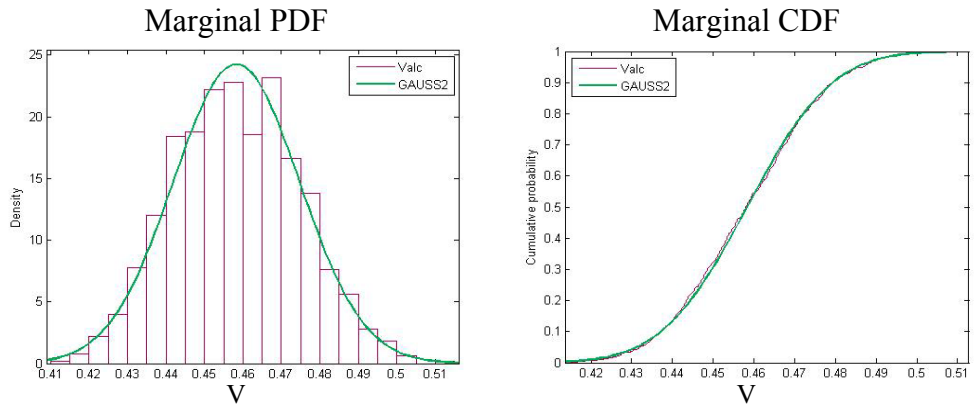


Fig. IV-7. PDF and CDF of peak-to-peak output voltage V_{alc}

As mentioned above, the performances of the VCO considered are phase noise, output frequency for different values of V_{tune}, and current consumption. Some performances are redundant making some columns of the data matrix linearly dependent. This linear dependence is clearly shown in Fig. IV-3, in particular between the different phase noise (PN) measurements and also between the different output frequency (OF) measurements. These strong dependences prevent the generation of the statistical model, since the data matrix is not invertible (determinant equal to zero). Moreover, some performances do not result in a Gaussian copula. Thus performances with a non Gaussian copula and the redundant performances must be omitted from the set of chosen performances for future study. For this reason, only a single phase noise measurement at 1 MHz from the carrier has been kept, and the measurement of output

frequency at V_{tune} equal to 1.0 V has been removed. Fig. IV-9 shows the new restricted data matrix.

The copula can often be chosen from a set of known functions and calibrated for a given case-study. In this work, a Gaussian copula has been used for simplicity. Other non Gaussian copulas could have been used instead. In this case, some eliminated performances could be reconsidered, but the investigation on the application of the Copulas theory in this work is still at an early stage. The parameters of the Gaussian copula are found from the correlation factors of the original data. Fig. IV-8 (a) and (b), represent the copulas matrices of the original data and the generated data respectively. Both copulas show a similar distribution. Fig. IV-9 (a) and (b) plot the bivariate distributions (except for the diagonal which is the histogram of the samples) of performances and test measures of the original data and the generated data respectively. The comparison between the two figures points out that the Copulas model approximates very well the initial data. The performances defined as the output frequency for different values of V_{tune} are obviously highly correlated.

A rigorous justification that the original data fits a Gaussian copula is not an easy task. The reader may refer to [49] for a description of how this can be done. In general, a visual inspection helps to validate the choice of a Gaussian copula. Moreover, a comparison of the correlation factors (ρ) of the original and generated data can also contribute to the validation of the choice of a Gaussian copula. The same may be done for the correlation factors of each 2-dimensional copula of the original data with the 2-dimensional copula of the generated population of 1 million samples. Comparing the ρs of the original data and the generated one, the difference is always smaller than 0.05. Comparing the ρs of all 2-dimensional copulas of the original data with the ones of the generated 1 million data instead, the difference is always below 0.02.

For illustration, Fig. IV-10 (a) and (b) show two bivariate distributions of the original 1000 instances and 1000 generated ones. Both distributions match very well. Similar results are obtained for each pair of performances.

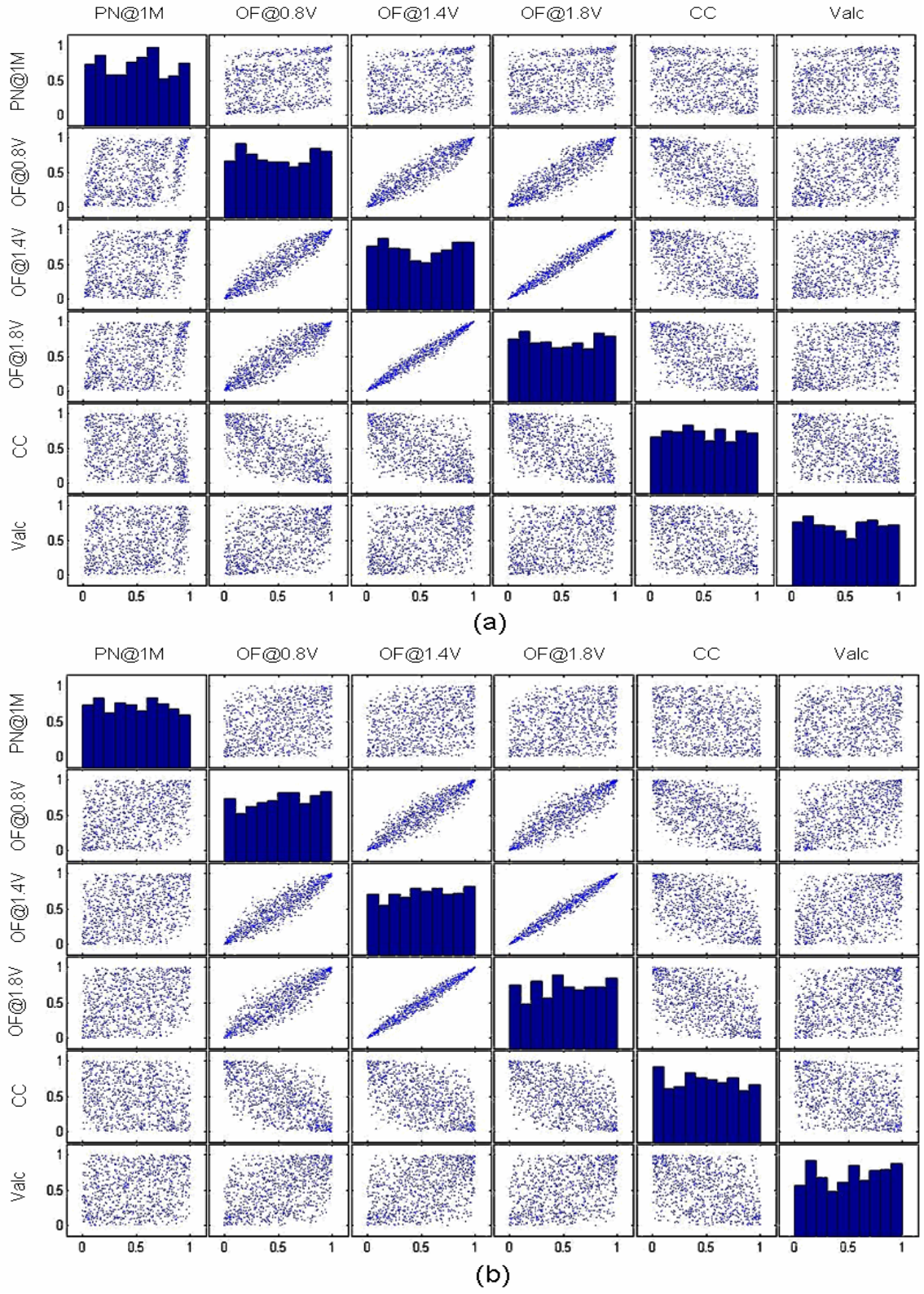


Fig. IV-8. Copula matrix of the VCO restricted number of performances and test measures obtained from (a) the original Monte-Carlo simulation data (b) the generated data (1000 instances)

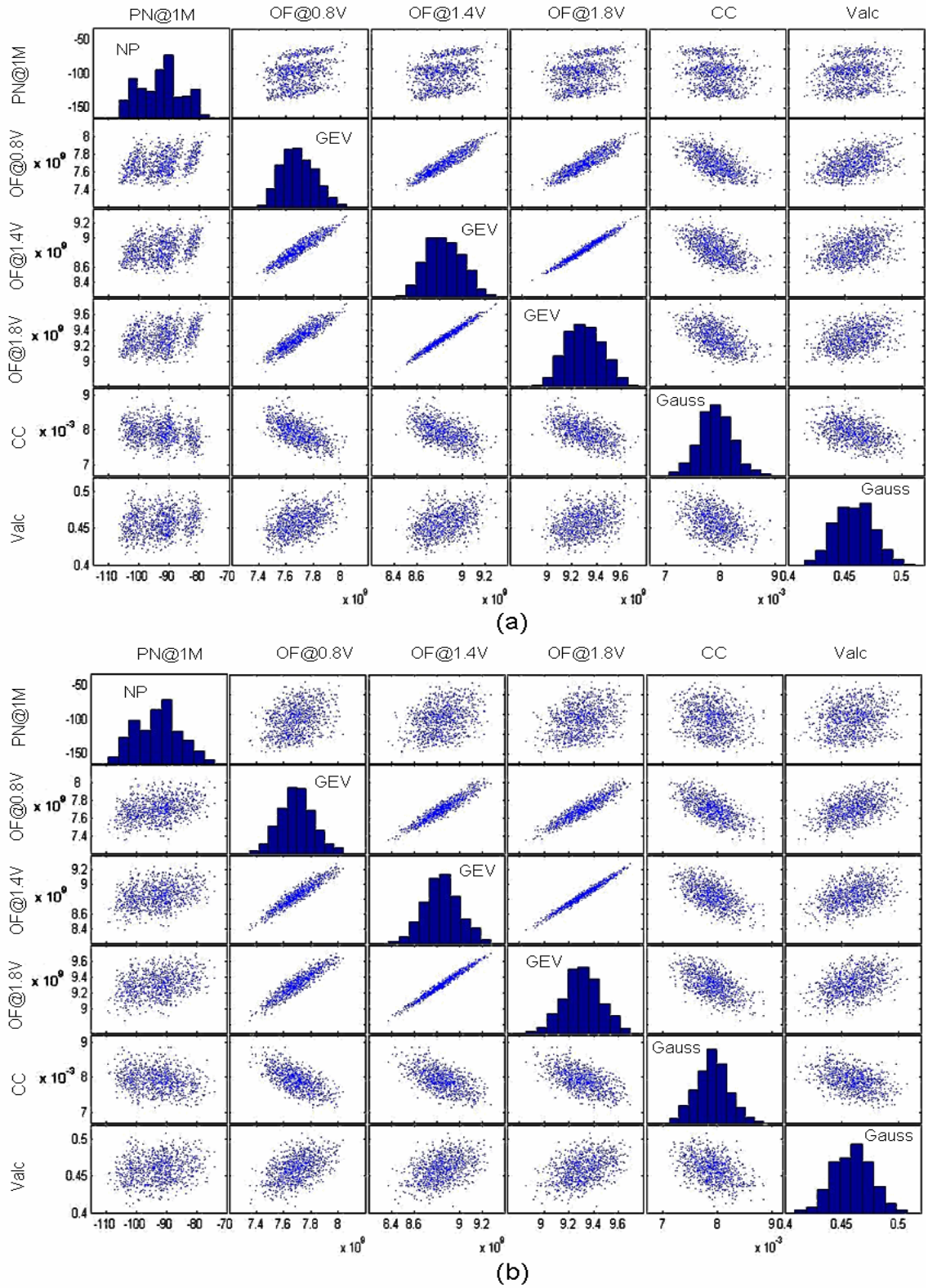
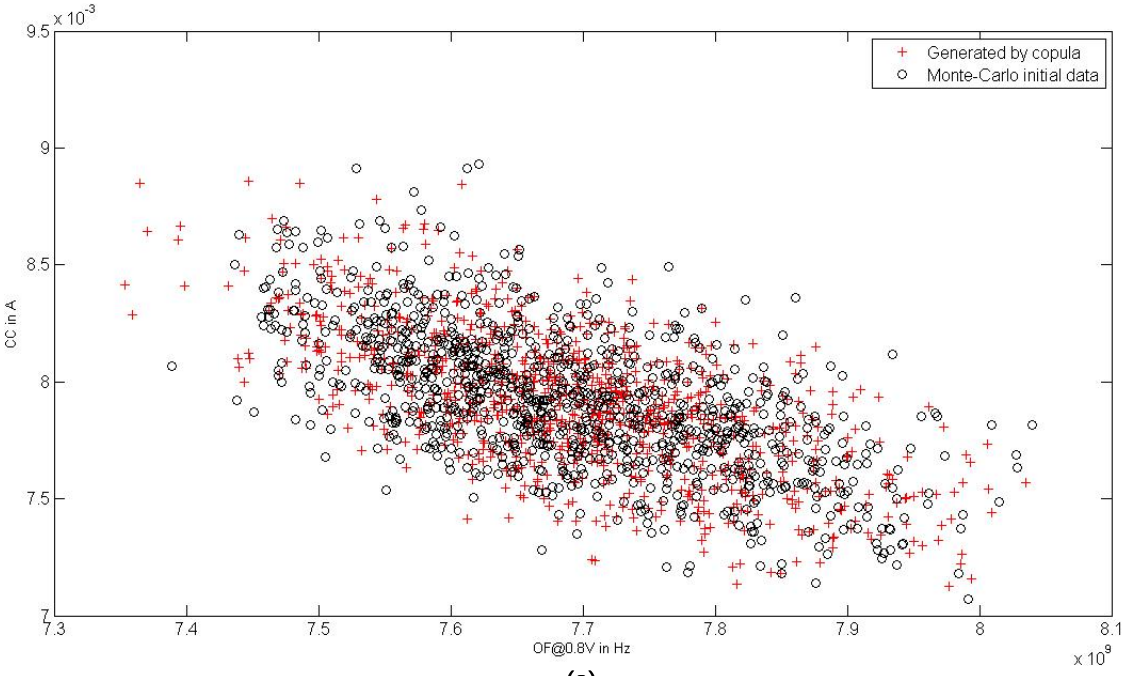
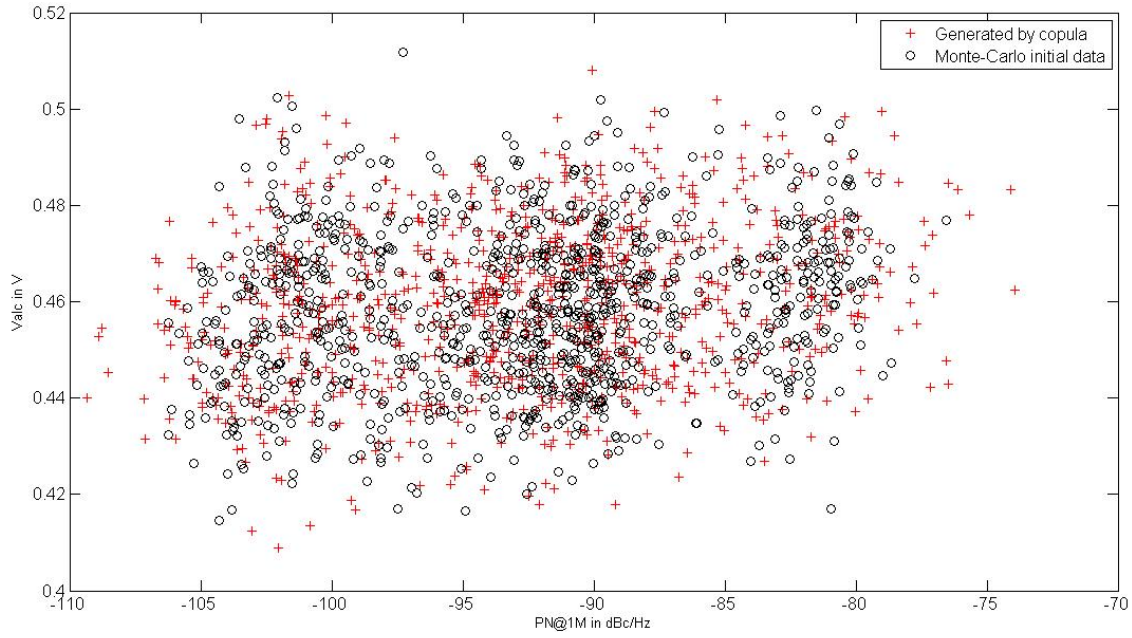


Fig. IV-9. Samples of the VCO restricted number of performances and test measures obtained from (a) the Monte-Carlo simulation (b) the Copulas-based model (1000 instances)



(a)



(b)

Fig. IV-10. Examples of VCO bivariate distributions (1000 instances) using the original data and data sampled from the Copulas-based model: (a) CC vs. OF@0.8V and (b) V_{alc} vs. PN@1MHz

4.4 Statistical Model of the Charge Pump

As for the VCO, to build a statistical model of the CP block, it is first necessary to define a set of performances, if not already specified by datasheet. Next, an analysis through simulation of the CP performances is carried out. In the case of the CP block, simulations must be carried out in a closed-loop configuration in order to measure the real mismatch between the reference frequency and the loop frequency. Sources of mismatch may be found in every block in the loop, and the feedback of the closed-loop configuration of the PLL has the effect of contrasting cumulating mismatch. The PFD+CP+LF block is mainly in charge of this task.

4.4.1 Charge Pump Performances and Test Measures

The performances of a PFD+CP+LF block are basically the difference between the respective positions of the sensitive edges of the PFD signals *UP* and *DOWN* when in lock conditions, CP mismatches between I_{up} and I_{down}, CP+LF leakages, and the VCO control voltage V_{tune}. Some of these performances may be in some cases related, such as the positions of the sensitive edges of the PFD outputs with mismatch and leakage. For CP simulations discussed in the next section it has been possible to measure by hand on the chronogram the distance between the rising (sensitive) edges of the *UP* and *DOWN* signals, but for Monte-Carlo iterations, values I_{out}, I_{up}, I_{down}, and V_{tune} have been taken as performances, since the calculation of a time delay of randomly positioned edges was not directly implemented in the simulator. The test measure for the CP is related to the output of the PFD monitor as explained in section 5.4.

4.4.2 Simulation of the Charge Pump

Different simulations have been carried out on this PLL in order to study process deviations effects on mismatch, here considered as the duration of *DOWN* (t_{down}) minus the duration of *UP* (t_{up}) of PFD output signals. Closed-loop simulations are very time consuming because lock state has to be achieved before measuring mismatch. Since repeated closed-loop simulations with all blocks at component level are not feasible in

terms of duration and data volume, a behavioral block in VerilogA hardware description language has been used for the VCO+Divider block.

In order to speed up the simulation, an additional block in VerilogA (named Starter and presented in Appendix 4) has been introduced in the loop as shown in the test bench reported exactly as in Cadence window in Fig. IV-11. This block receives f_{loop} and generates an f_{ref} at the wanted frequency in phase with f_{loop}. An initial condition imposed on V_{tune} assures that f_{loop} is at the same frequency of f_{ref} forcing the VCO to oscillate at the lock frequency. This "forces/helps" the PLL to achieve lock state almost immediately (a small settlement time is needed in any case). In typical conditions the PLL attains lock in 3 μs (in simulation), but in order to study all possible worst cases 10 μs have been considered enough to attain lock state in any kind of process variation.

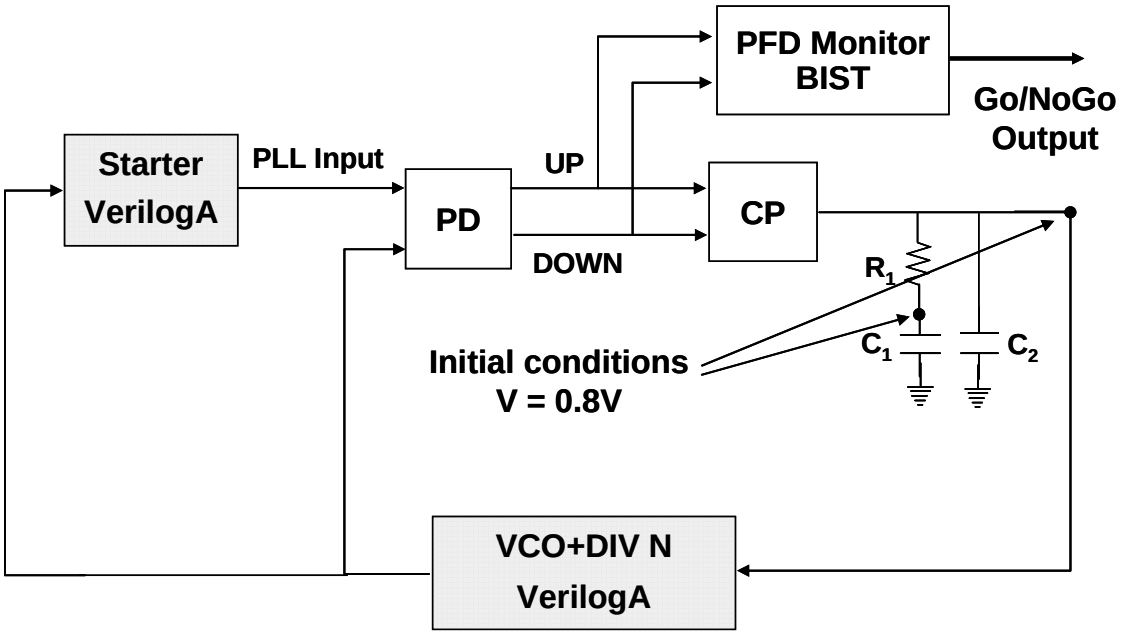


Fig. IV-11. PLL closed-loop simulation test bench

The following simulation strategy has been adopted. First of all, Monte-Carlo analysis have been carried out on VCO alone, at circuit level, to ensure that the expected frequency of 7.5 GHz is always achievable in the tuning voltage (V_{tune}) range of 0.4 V to 2 V.

The results of these simulations are illustrated in Fig. IV-12. The curve MAX V_{tune} corresponds to the Monte-Carlo instance that allows reaching the output frequency of 7.5 GHz with the maximum allowed V_{tune} of 2 V. For this case a VCO gain K_{vco} of 0.6 GHz/V is obtained. Likewise MIN V_{tune} is the Monte-Carlo instance that allows reaching the output frequency of 7.5 GHz with the minimum allowed V_{tune} of 0.4 V. All these results are summarized in the left hand side of Tab. IV-5. These results are used as parameters for the VCO behavioral model in the closed-loop simulations. Note that not only the tuning voltage V_{tune} of the VCO changes with process variations, but also the gain K_{vco} and obviously the free running frequency f_0 (VCO output frequency for V_{tune} equal to 0 V). The behavioral model of the VCO is presented in Appendix 4.

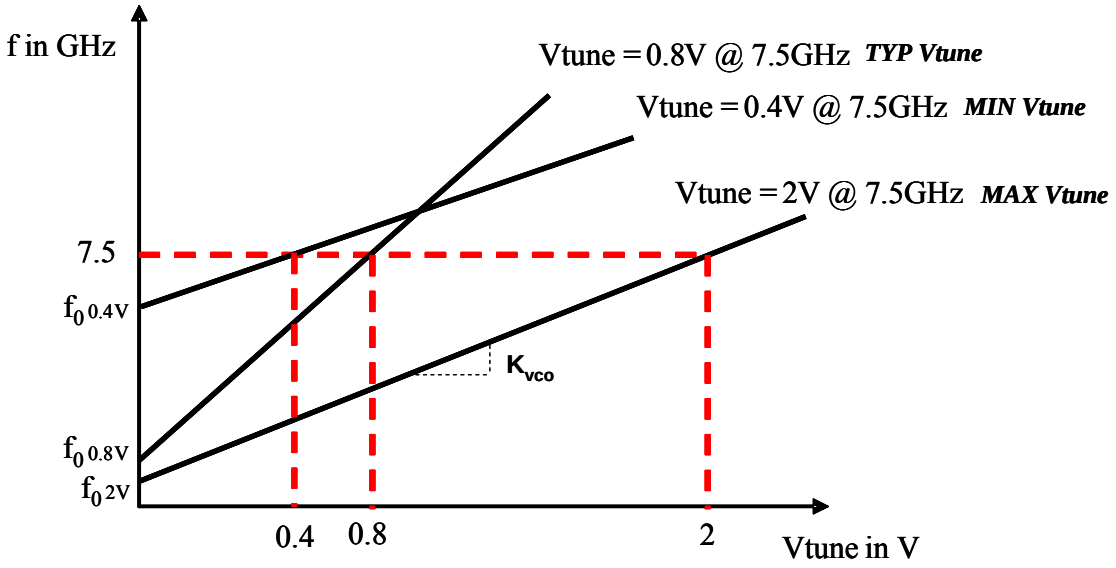


Fig. IV-12. Variations of VCO tuning voltage and gain obtained by Monte-Carlo circuit level simulation of the VCO

Next, worst cases (FFA, SSA) and TYP simulations have been run on the closed-loop PLL in the three configurations of the behavioral model of the VCO shown in Fig. IV-12:

- the VCO oscillates at 7.5 GHz when driven by a V_{tune} = 0.8 V which is the center case for the VCO tuning range called TYP V_{tune},

- the VCO oscillates at 7.5 GHz when driven by a $V_{tune} = 0.4$ V which is one corner case for the VCO tuning range called MIN V_{tune},

- the VCO oscillates at 7.5 GHz when driven by a $V_{tune} = 2$ V which is the other corner case for the VCO tuning range called MAX V_{tune}.

For FFA, SSA and TYP simulations the settings shown in Tab. IV-4 have been used.

	TYP	**SLOW**	**FAST**
T in °C	25	105	-30
Vdd in V	2.5	2.25	2.75
Corners	TT	SSA	FFA

Tab. IV-4. Typical and worst case conditions on temperature, Vdd, and corners

Tab. IV-5 shows the results obtained, where another line for $V_{tune} = 1.9$ V (called MAX OK) has been added because SSA simulation at $V_{tune} = 2$ V (MAX) shows that the CP is not working properly since it gives a value for mismatch out of specification. At $V_{tune} = 1.9$ V mismatch may still be considered acceptable. CP has to be improved in next design in order to comply with specifications. This will be a designers' task.

BEHAVIORAL VCO CONDITIONS				**CP CONDITIONS**		
				t_{down} - t_{up} in lock state in ps		
V_{tune} @ 7.5GHz in V		**K_{vco} in GHz/V**	**f_0 in GHz**	**FAST**	**TYP**	**SLOW**
MIN	0.4	0.54	7.284	221	182	169.5
TYP	0.8	1.2	6.54	121.5	68.6	25
MAX	2	0.6	6.3	-35	-127	-672
MAX OK	1.9	0.6	6.36	-54	-96	-311

Tab. IV-5. Typical and worst case simulations on SERDES PLL

4.4.3 Copulas-Based Statistical Model of the Charge Pump

The same procedure and formalisms described for the VCO in section 4.3.3 is used to build a statistical model for the CP. In this case, since simulations turned out to be very time consuming, it hasn't been possible to generate more than 100 instances, which took a simulation time of 3 months. Nevertheless, as proved for the VCO, models generated starting from 300 samples or from 1000 samples of the same device give similar accuracy for a statistical model. Thus, it may be stated that the procedure used to build the statistical model using copulas will be accurate enough starting from the 100 initial instances of the CP generated by Monte-Carlo simulations.

Fig. IV-13 shows the initial population generated by Monte-Carlo simulations, where I_{out} is the output current of the CP block, I_{up} is the current from the "upper" current mirror (pmos) of the CP, I_{down} the current from the "bottom" current mirror (nmos) of the CP, V_{tune} is the voltage at the output of the CP, and *Sum_BIST* is the only CP test measure. This test measure corresponds to the sum of the 8 intermediate Boolean signals of the digital BIST that monitors the CP mismatches and leakages as will be explained in the next chapter. I_{out} seems to be completely independent with respect to I_{up} and I_{down}, which is difficult to believe since their strict relationship: $I_{out} = I_{down} - I_{up}$. Graphically it is impossible to visualize their relationship since the values of I_{out} are too small (in the order of 10^{-9} A). It is also difficult to assess correlation with V_{tune} visually since this performance has a too small standard deviation (all instances are very close to the nominal value of 800 mV).

Tab. IV-6 gives the statistical parameters of each performance and test measure along with the estimated PDF, also shown in Fig. IV-14 to Fig. IV-16, just as for the VCO.

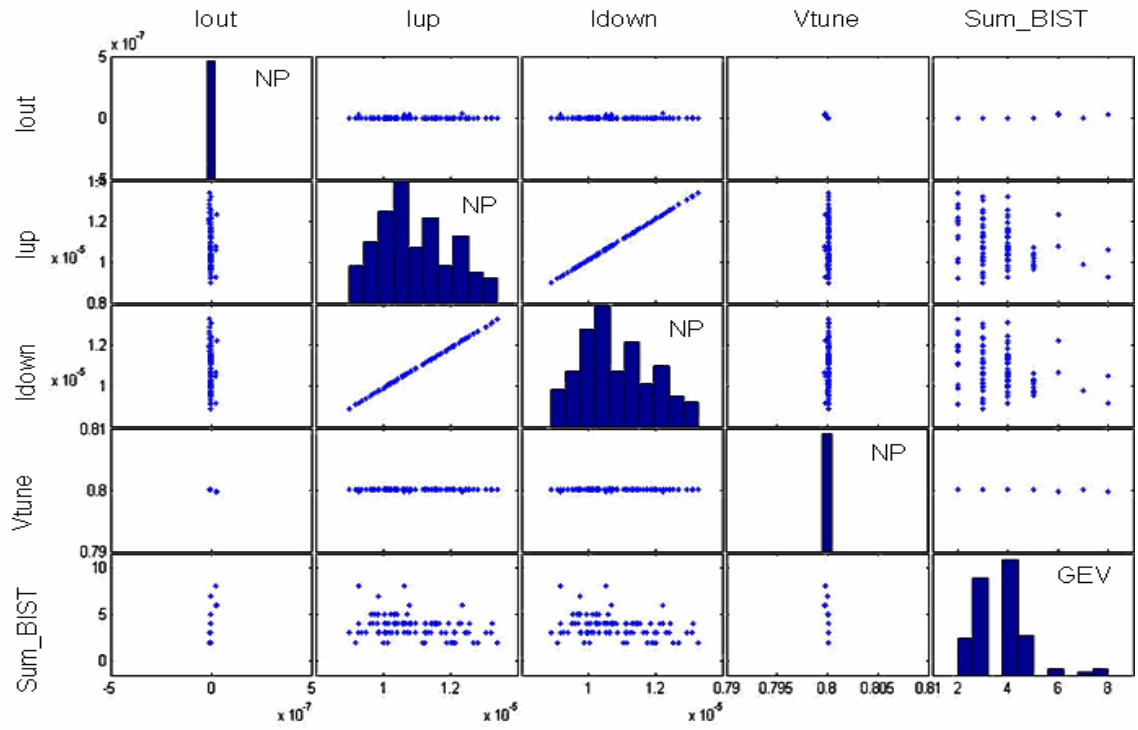


Fig. IV-13. Samples of the CP performances and test measures obtained from the Monte-Carlo simulation (100 instances)

Perf/TM	Dist	Parameters			
		μ	**σ**	**width**	**k**
Iout	NP	$-3.21\cdot10^{-10}$ A	$3.69\cdot10^{-9}$ A	$2.50\cdot10^{-10}$ A	-
Iup	NP	$1.09\cdot10^{-5}$ A	$1.06\cdot10^{-6}$ A	$4.49\cdot10^{-7}$ A	-
Idown	NP	$1.08\cdot10^{-5}$ A	$1.05\cdot10^{-6}$ A	$4.49\cdot10^{-7}$ A	-
Vtune	NP	0.8 V	$6.62\cdot10^{-5}$ V	$3.44\cdot10^{-6}$ V	-
Sum_BIST	GEV	3.72	1.16	-	$-4.36\cdot10^{-2}$

Tab. IV-6. Fitted distributions of performances and test measures of the CP

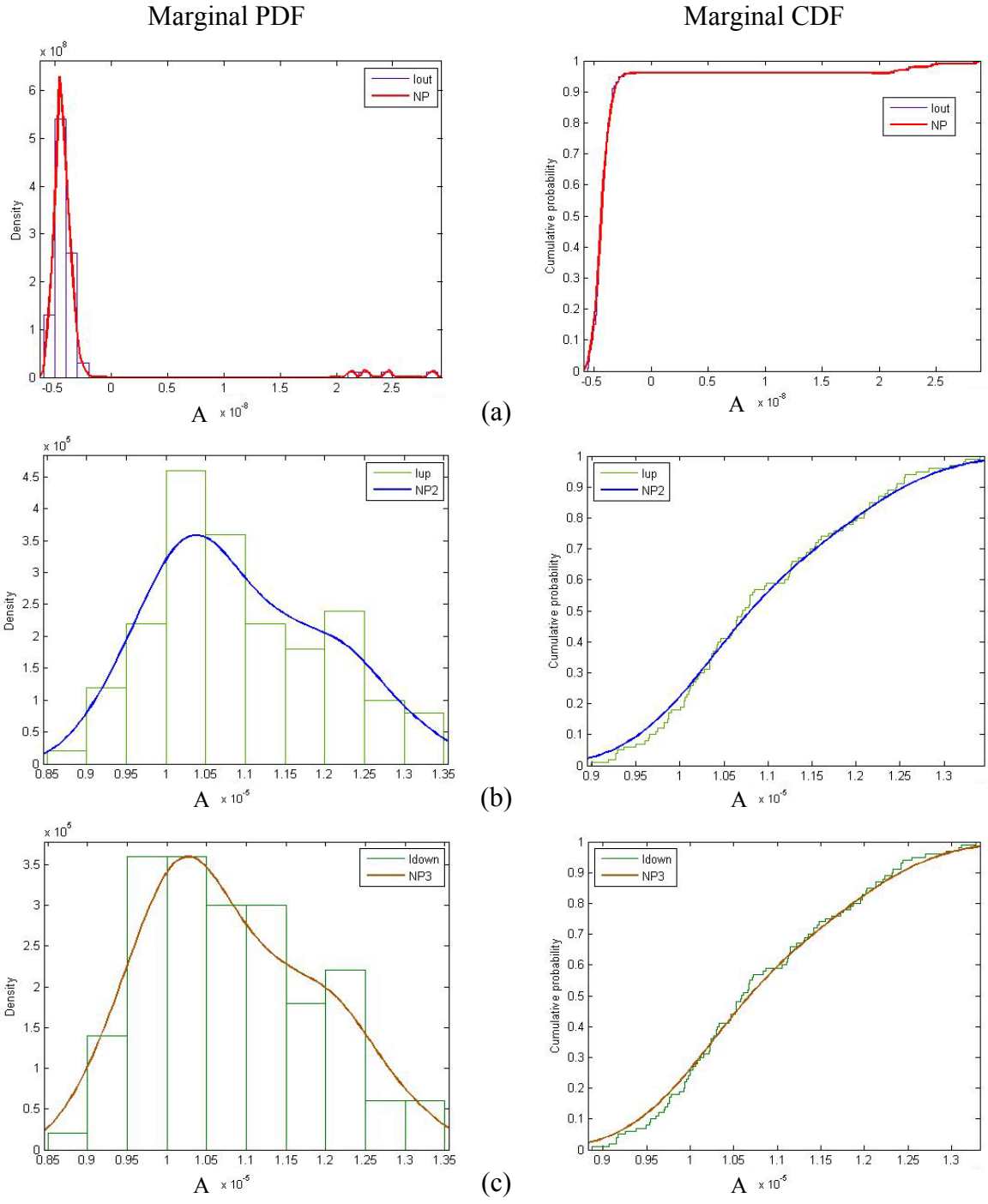


Fig. IV-14. PDFs and CDFs of CP (a) I_{out}, (b) I_{up}, and (c) I_{down}

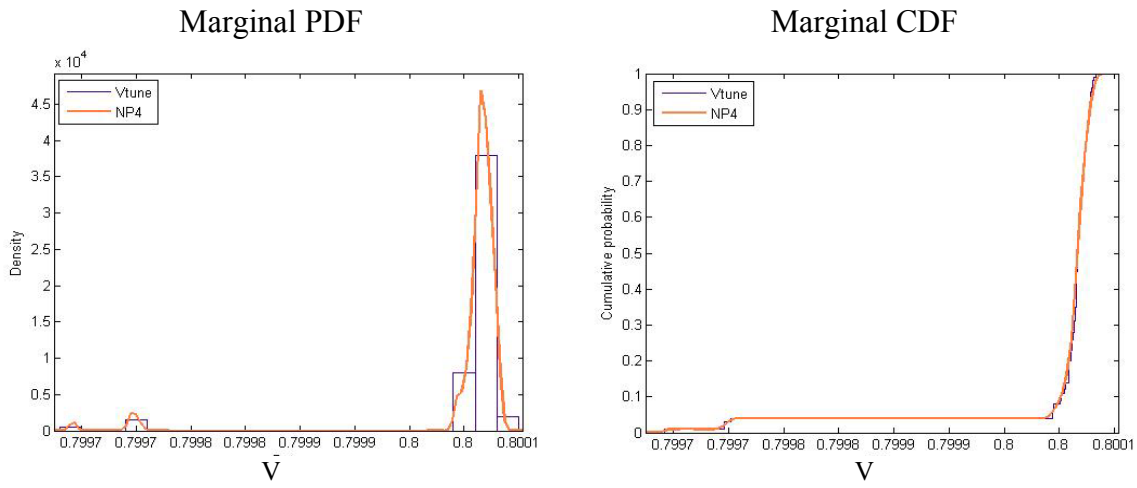


Fig. IV-15. PDF and CDF of CP V_{tune}

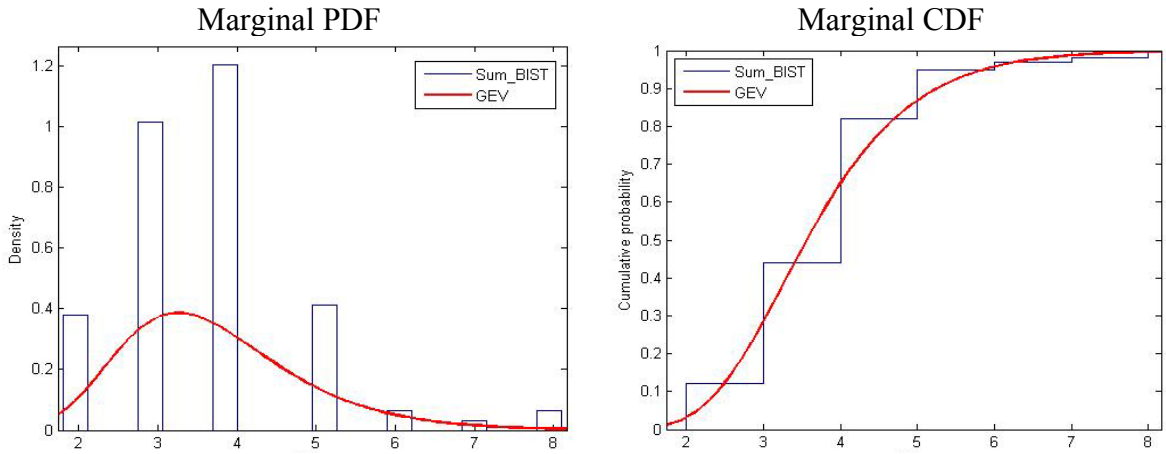


Fig. IV-16. PDF and CDF of CP Sum_BIST

Also for the CP block, one performance turned out to block the generation of the statistical model, since the data matrix was not invertible due to the fact that its value is too small to be put in the denominator (to evaluate the determinant). This performance is clearly I_{out}. In Fig. IV-17 (a) and (b) are depicted the copula matrix of the set of performances and test measures selected from the initial data obtained by Monte-Carlo simulation and the copula matrix of the generated statistical model respectively. Fig. IV-18 (a) and (b) show samples of the performances and test measures obtained by Monte-Carlo simulation and for the data generated from the statistical model, respectively. It may be noticed that up and down currents are highly correlated, as expected. As it may be noticed observing the copula matrix, the test measure *Sum_BIST*

correlated rather well with the performance V_{tune}. This was not visible in the data matrix since the standard deviation of V_{tune} is extremely small and its values were too concentrated around its nominal value of 800 mV. The copula actually gives the absolute dependence between two variables regardless their marginal distributions. Since *Sum_BIST* corresponds to the sum of Boolean variables, and thus is made up of a set of integers, all plots are concentrated on lines corresponding to integers. The copulas matrix obtained with the one million samples to generate the estimated population is not dicretized for the column concerning the *Sum_BIST* test measure. Actually, initially the generated matrix is not discretized either, but a simple data manipulation allows obtaining the discretization needed for this test measure.

Comparing the initial data and the generated instances the statistical model may be considered consistent. For further illustration, Fig. IV-19 (a) and (b) shows two bivariate distributions of the original 100 instances and 200 generated ones. Both distributions match quite well considering that 100 points are very few for comparisons. Similar results are obtained for each pair of performances.

4.5 Conclusions

After having studied the performances of the VCO block in stand alone configuration and the CP block in closed-loop configuration, copulas-based statistical models have been built from an initial population generated by Monte-Carlo simulation. It has been demonstrated that the statistical models are coherent with the initial data obtained by Monte-Carlo simulations both for the VCO and the CP blocks. In the next chapter the BIST sensors designed to measure on-chip the test measures studied in this chapter are presented. The statistical models built in this chapter for the PLL blocks will be used in Chapter VI for settling test limits on the BIST monitors and for estimating test metrics that quantify the validity of the chosen BIST strategy.

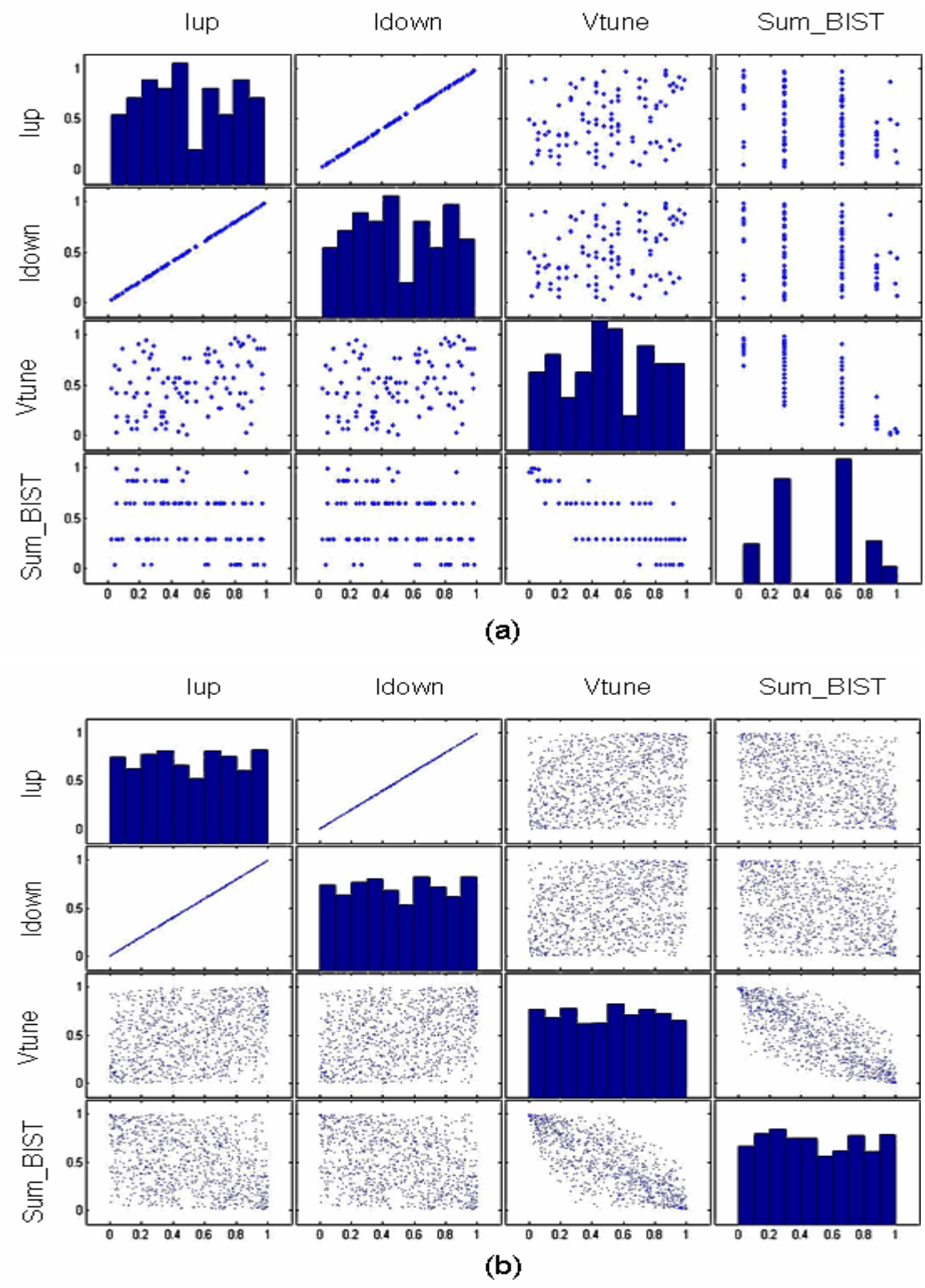


Fig. IV-17. Copula matrix of the CP restricted number of performances and test measures obtained from (a) the original Monte-Carlo simulation data (b) the generated data (1000 instances)

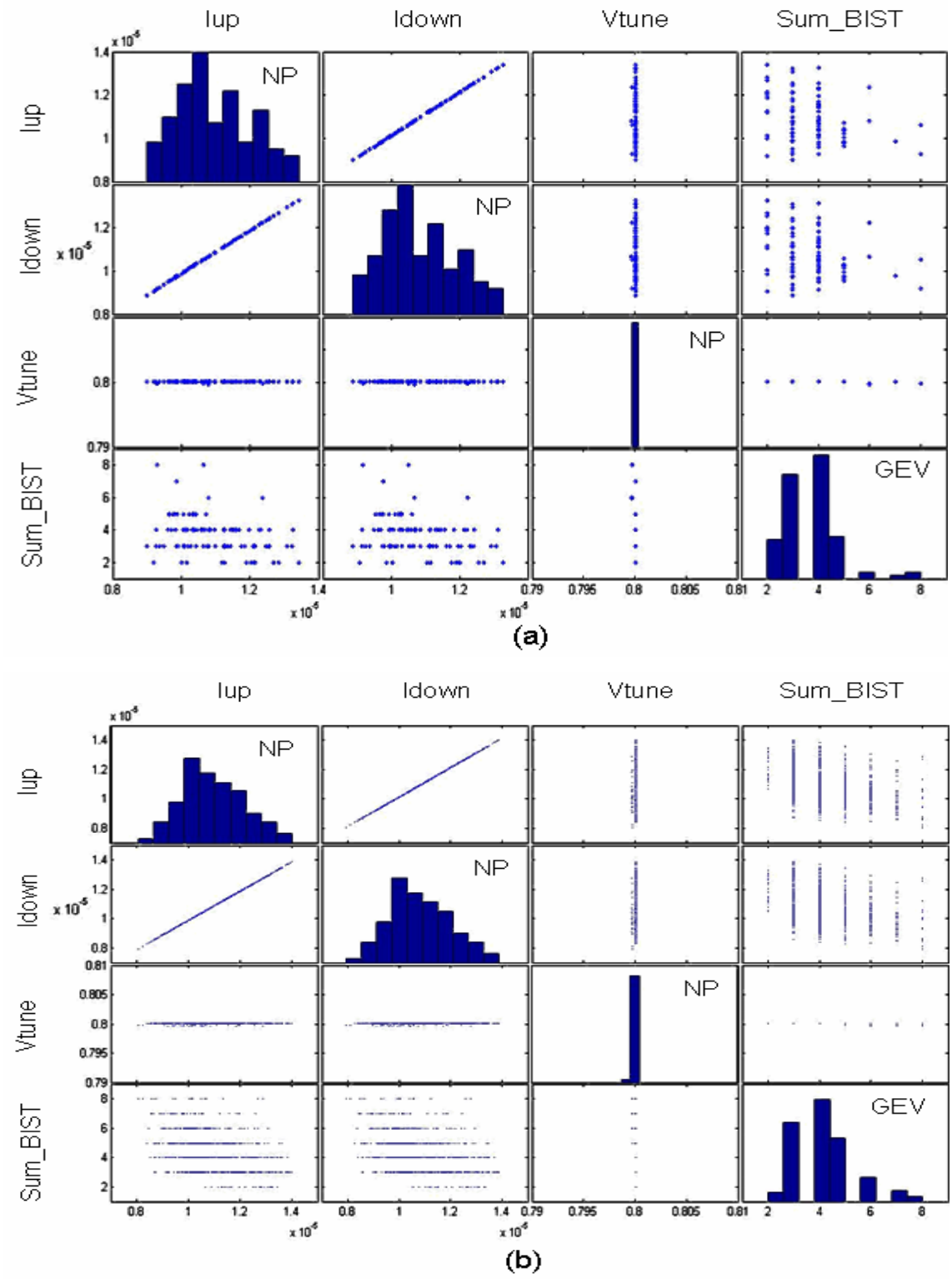
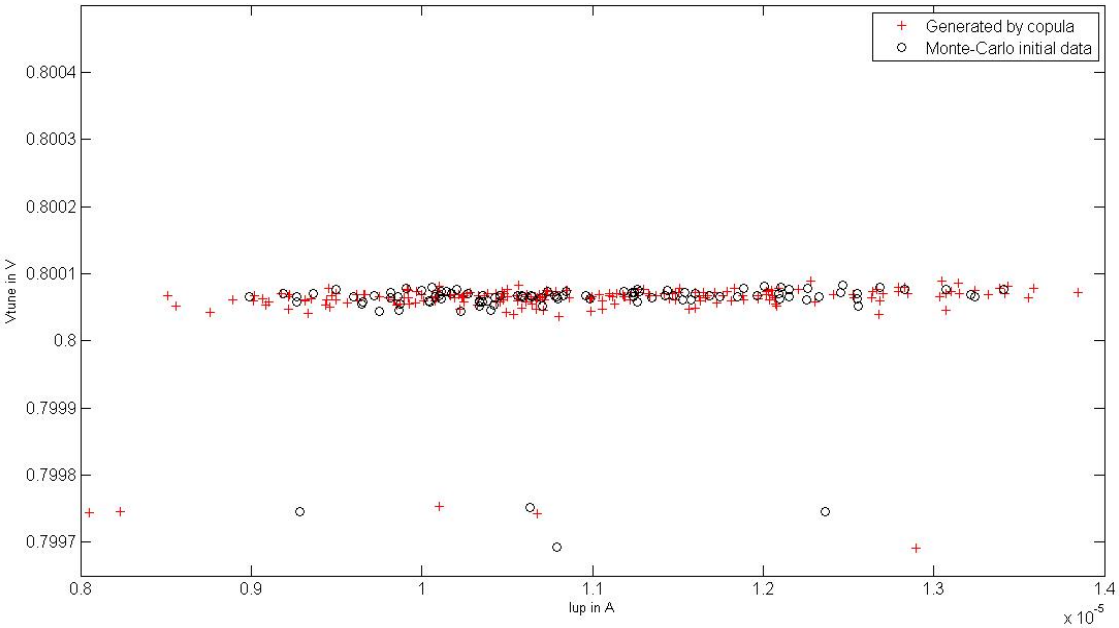
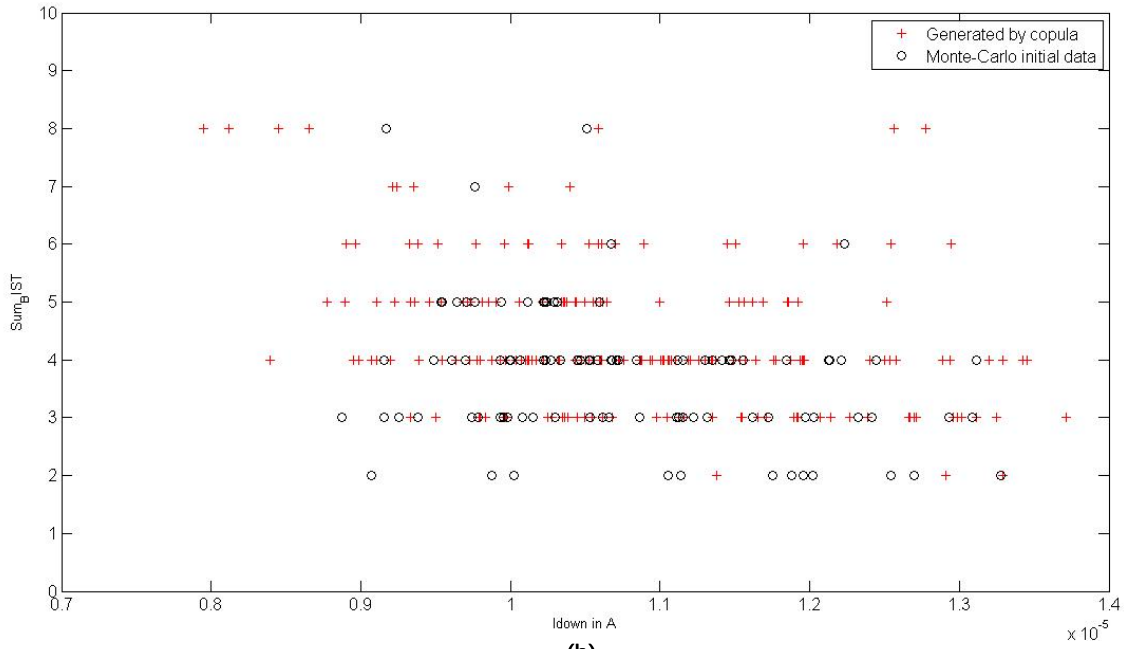


Fig. IV-18. Samples of the CP restricted number of performances and test measures obtained from (a) the Monte-Carlo simulation (b) the Copulas-based model (1000 instances)



(a)



(b)

Fig. IV-19. Examples of CP bivariate distributions from the original data (1000 instances) and from 1000 instances sampled from the Copulas-based model (a) I_{up} vs. V_{tune} and (b) I_{down} vs. Sum_BIST

Chapter V

Embedded Monitors for PLL Testing

5.1 BIST Monitors

The BIST technique proposed is made up of three sensors, two of which are applied to the VCO and one to the PFD output, as shown in Fig. V-1. Standard digital test techniques can be considered for the digital blocks providing an overall Go/No-Go output signal, where 0 = Go and 1 = No-Go. Careful attention has been paid to avoid probing sensitive analog nodes. In fact, probing sensitive analog nodes such as CP, LF and VCO outputs might impact the overall operation of the PLL [35]. Two sensors for the VCO block alone have been chosen since the VCO is known to be the main source of phase noise in a PLL and also because it is mainly in the VCO that most malfunctioning causes may occur. The BIST block at the PFD output will monitor the *UP* and *DOWN* PFD output signals measuring their mismatch. The aim is to avoid a direct jitter measurement at the VCO output, contrary to many existing BIST techniques, since this task is becoming unachievable due to the high frequencies into play. An expensive dedicated tester (if one will be available on the market at the needed frequency) should be employed for jitter measurements.

The degree of correlation between the chosen test measures and the device performances has been investigated by simulation. For the VCO, the performances considered include phase noise, output frequency at different values of V_{tune} (related to VCO gain), and current consumption. The actual VCO test measures that may be easily obtained on-chip include peak-to-peak output voltage, V_{alc} (strictly related to VCO

output power), current consumption (which is also a performance), and output frequency at nominal value of V_{tune}. Moreover, measuring the difference in duty cycle of the PFD output signals allows obtaining information related to mismatch, leakage, synchronization between the reference frequency and the feedback loop frequency (related to the output frequency), phase deviations due to PM of spurious signals as seen in section 2.3.2, lock time and state.

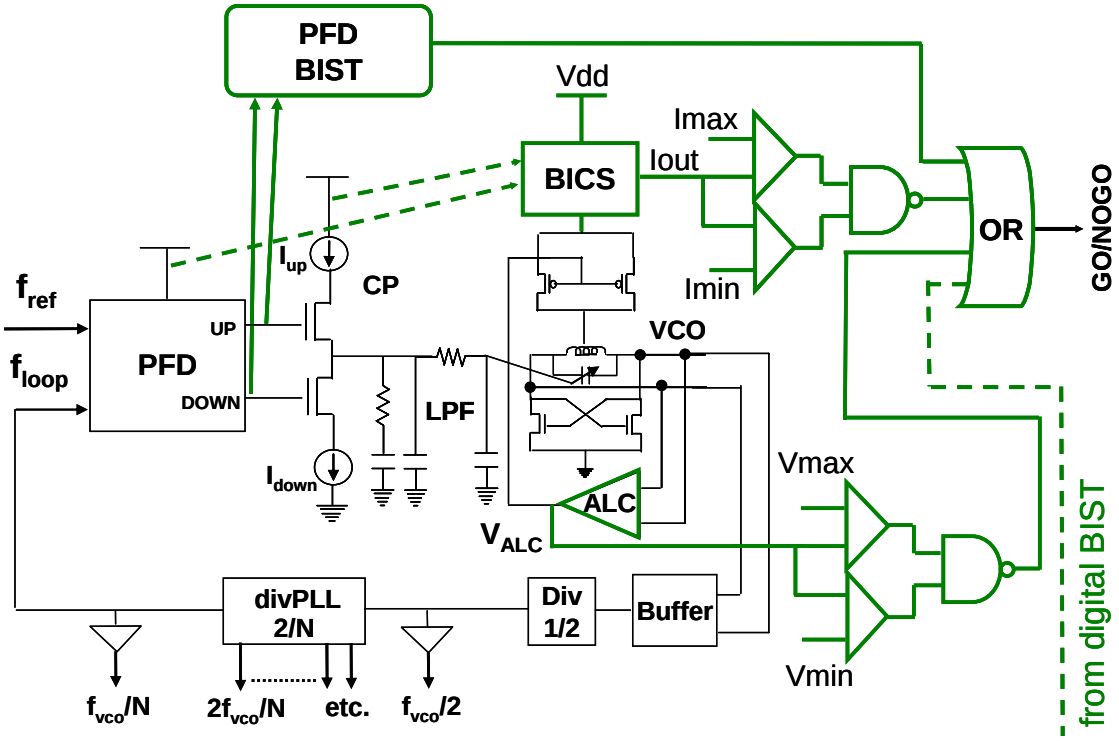


Fig. V-1. PLL with embedded BIST monitors

The sensors proposed are thus [37]:

- BICS for measuring VCO current consumption (the BICS may be also applied to other blocks eventually).

- Voltage window comparator for measuring the dc peak-to-peak voltage at the swing control output. The swing control is an envelop detector followed by an amplifier (called ALC in the VCO, see section 2.3.2). This measure is strictly

related to VCO output power. Another sensor for measuring peak-to-peak output voltage of a VCO without ALC may be found in [38].

- PFD output BIST to measure:
    - CP current mismatch,
    - CP, LF, and VCO varactor leakages,
    - synchronization between f_{ref} and f_{loop} (output frequency),
    - lock time and state.

Other BIST techniques that probe the PFD outputs exist in literature, typically the simple lock detectors. In [39] a technique that probes the PDF outputs for detecting the peak output frequency of the PLL is presented. This technique provides a slight modification of the existing PFD to perform a peak detection function in order to determine the phase response of the PLL. This phase response is obtained by counting pulses between the occurrence of the peak magnitude of the input signal and the peak magnitude of the output signal, and then converting these pulses into phase degrees. The authors suggest adding an additional PFD for the purpose "so that it does not impair PLL operation". Moreover, in this technique a D flip-plop "is clocked from the dead zone glichtes… which is not a generally recommended design practice" as the authors state, but "in the particular application … the circuitry operates correctly". The paper does not propose, however, any method for jitter or phase noise related measurements.

The technique presented in this Ph.D. work is based on mismatch detection with fine resolution, which is a phase noise related measurement. It is meant to be the most general possible in order to be applied to potentially any PLL, without modifying any of its blocks.

5.2 BICS

The principle of measuring current consumption *Idd* for built-in self test purposes is very common for digital devices. [40] suggests to use this test on analog and mixed-signal devices. Some existing BICS for AMS devices existing in the literature have thus been analyzed such as the one in [41] and [42]. This last one seemed the most appropriate since the current *Idd* consumed by the DUT current was taken from the *Vdd* source and not between the DUT and ground as in [41].

The chosen BICS is shown in Fig. V-2 and has been redesigned and scaled from the existing BICS in [42] in order to comply with CMOS 65 nm technology and process deviation issues. Nevertheless, the output should not be a voltage and should not be taken on a resistor (too sensitive to process variations) as in [42]. Instead, the current I_{meas} that flows in the current mirror shown in Fig. V-2 (a) and (b) has been chosen as measure. The idea behind this BICS is to make the *Idd* current consumed by the VCO pass from the supply *Vdd* to the VCO through a low impedance resistor. A very small amount of this current (negligible compared with VCO consumption) passes into the current mirror of the BICS and is amplified to obtain I_{meas}. Besides, the reference current sources I_{max} and I_{min} are used as test limits and compared with I_{meas} by the current comparator of Fig. V-2 (b). These reference sources should vary in the same way as the BICS core with process deviations. To guarantee this, they have an architecture that is similar to the BICS core itself, as depicted in Fig. V-2 (c), where I_{ref} is a stable current source of 9 mA replacing *Idd* of the BICS core. Existing layout in 130 nm technology occupies 0.007 mm^2. Layout in 65 nm STMicroelectronics technology has been carried out for the BICS sensor (a). A rough estimation of the area of the whole BICS is of 3250 μm^2, corresponding to 3.2 % area overhead with respect to the SERDES PLL case-study.

Simulations have been carried out on the BICS core to verify that the proportionality between *Idd* and I_{meas} was always respected in the VCO range of operation. Simulations have also been carried out to verify the correct behavior of the BICS comparator in

nominal conditions and to validate the modifications applied to the previous existing design in 130 nm technology of [42].

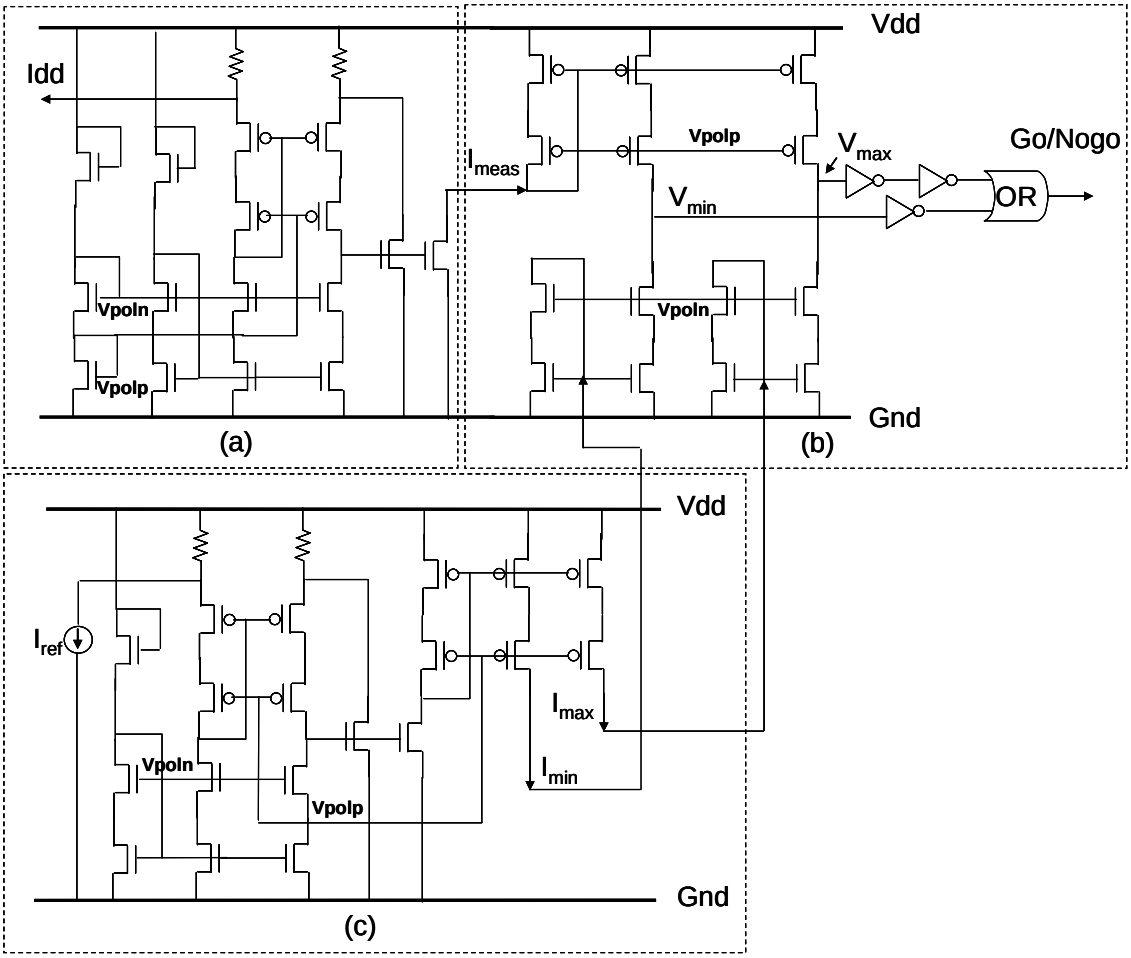


Fig. V-2. Built-in current sensor schematics: (a) core, (b) current comparator, and (c) current reference sources

Fig. V-3 shows the results of a DC parametric sweep of I_{meas}. The current comparator is correctly working since the edges of the Go/No-Go output signal are practically aligned to the imposed limits of I_{meas} ($I_{min} = 745.9$ μA and $I_{max} = 931.7$ μA by design of reference sources). BICS limits have been imposed according to results obtained on the statistical analysis of the VCO, since current consumption *Idd* is a performance and I_{meas} is proportional to it. The voltages at the output of the current mirrors used as current comparators are also depicted in Fig. V-3 (V_{min} and V_{max} in the graph). Obviously the

rising and falling edges of the Go/No-Go are not perfectly aligned to the actual current test limits imposed because the parametric sweep on I_{meas} has been carried out on 40 steps for I_{meas} on an interval of 600 μA (from 600 μA to 1.2 mA) which yields an accuracy of 15 μA.

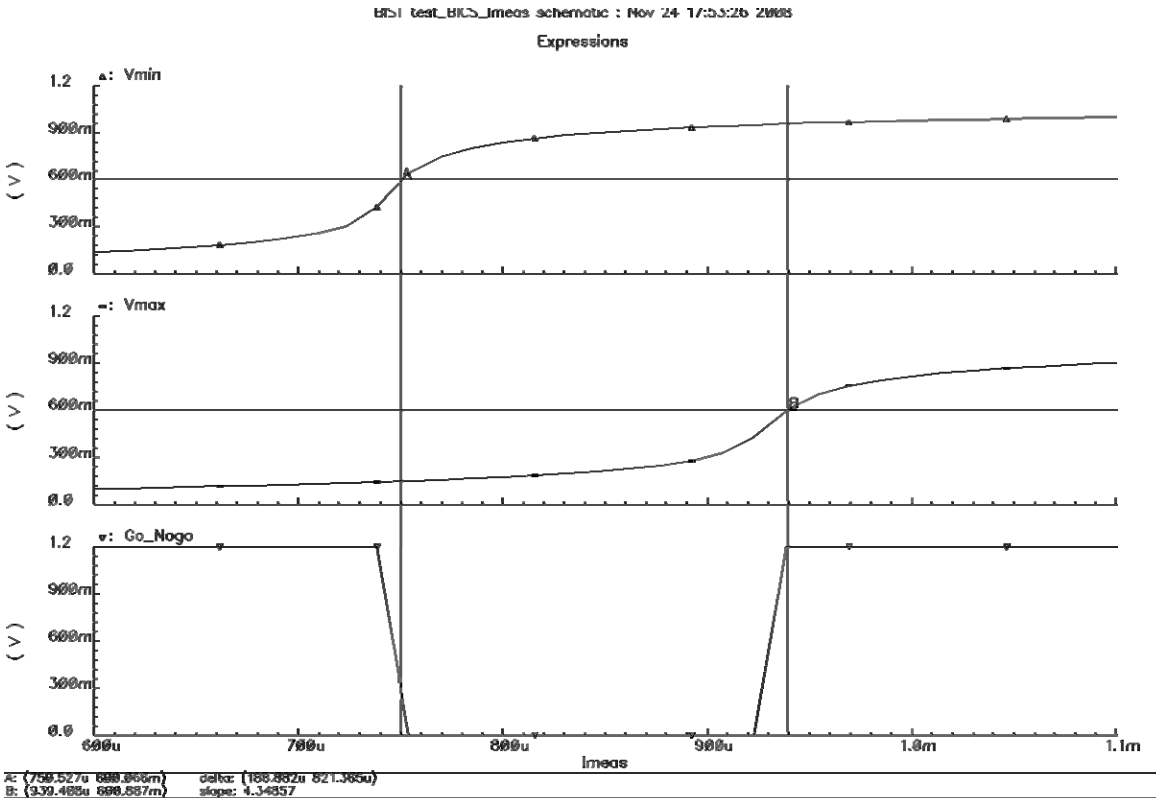


Fig. V-3. BICS comparator operation mode

5.3 Voltage Comparator

The voltage window comparator is shown in Fig. V-4. It uses two comparators and two voltage reference sources V_{min} and V_{max}. The comparator has been chosen from an STMicroelectronics IP library [43]. This is a well known architecture in the literature and is often referred to as symmetrical operational transconductance amplifier (OTA) [44] or push-pull comparator [45]. Design and layout of the comparator already exists in CMOS 65 nm technology, its surface area is of 35.4 μm * 71.18 μm = 2519.772 μm^2 (dummies included) which means 2.47 % area overhead with respect to the SERDES

PLL case-study. The voltage sources are currently external. For BIST purposes they should be built-in and should vary with process deviations in the same way as the voltage V_{alc} at the ALC output. This has not been carried out in this work, but may be object of future work. Moreover, a basically identical task has been already carried out on the BICS for I_{min} and I_{max}.

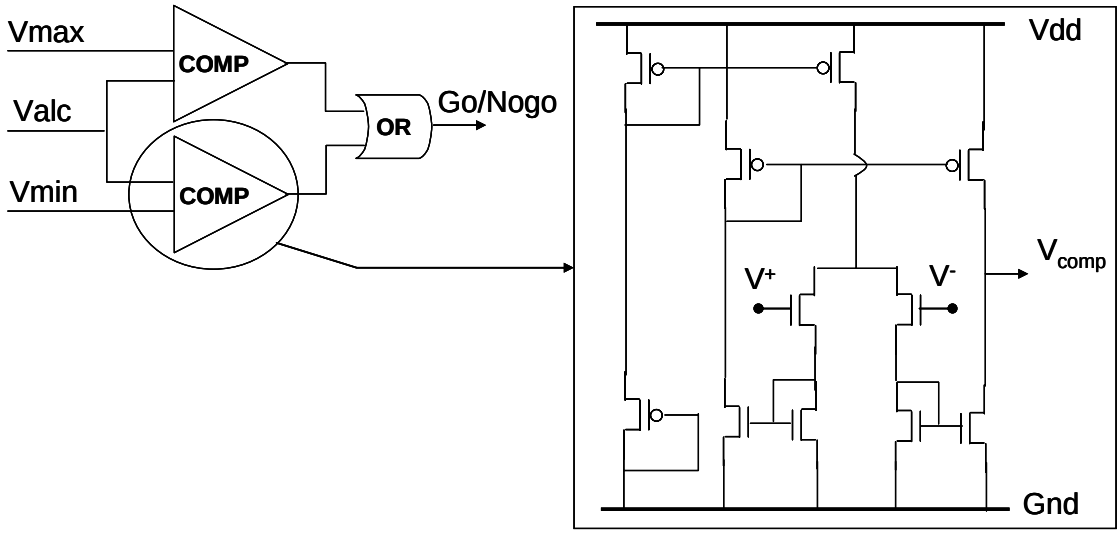


Fig. V-4. Voltage window comparator schematics

As it has been done for the BICS, the operation mode of the voltage comparator has been verified by simulation. Fig. V-5 shows the results of a DC parametric sweep of V_{alc}. The edges are well aligned to the test limits imposed on V_{alc} in the voltage comparator, V_{min} = 500 mV and V_{max} = 700 mV. These limits are not yet the BIST real limits. These will be set after analysis of the VCO test measures (in fact, unlike *Idd*, V_{alc} is not a performance of the VCO). Yet, the limits used can still be considered in the range of V_{alc} values of the VCO. The real limits for V_{alc} test measure are discussed in the next chapter, using the methodology discussed in section 3.2.2. The Go/No-Go output is also as expected, always considering that the parametric sweep on V_{alc} parameter has been carried out with 40 steps on a 400 mV interval which sets a degree of precision of 10 mV.

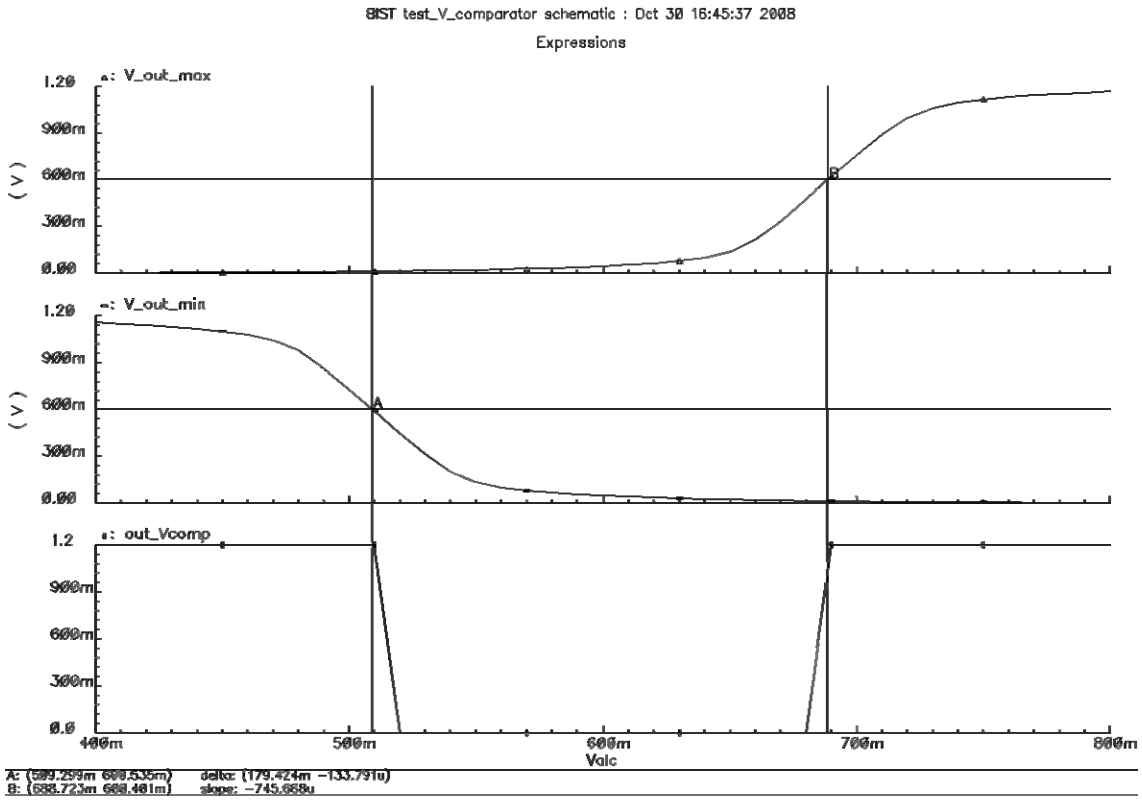


Fig. V-5. Voltage window comparator operation mode

5.4 PFD Monitor

The PFD output gives information not only on its own behavior but also on the whole PLL operation as seen in section 2.2.2. For example, it allows monitoring the synchronization between the reference frequency f_{ref} and the feedback loop frequency f_{loop} that ensures proper VCO and Divider-by-N operation, and the current mismatches and leakages in the CP, LPF and VCO varactor. In the frequency domain, current mismatch in a CP translates into a spur in the noise spectrum that contributes to the whole PLL jitter, as explained in section 2.3.2. Thus, a BIST technique based on monitoring the PFD output is highly related to jitter evaluation.

The PFD output monitor is able to tolerate a current mismatch within specifications that may be set at design stage or from external commands. Let dt_{inv2} be the delay introduced by two inverters in cascade, which will be referred to as a delay element, and $n * dt_{inv2}$

be the maximum delay acceptable between the *UP* and *DOWN* signals. This delay can be derived from the equivalent maximum CP current mismatch given by the specifications.

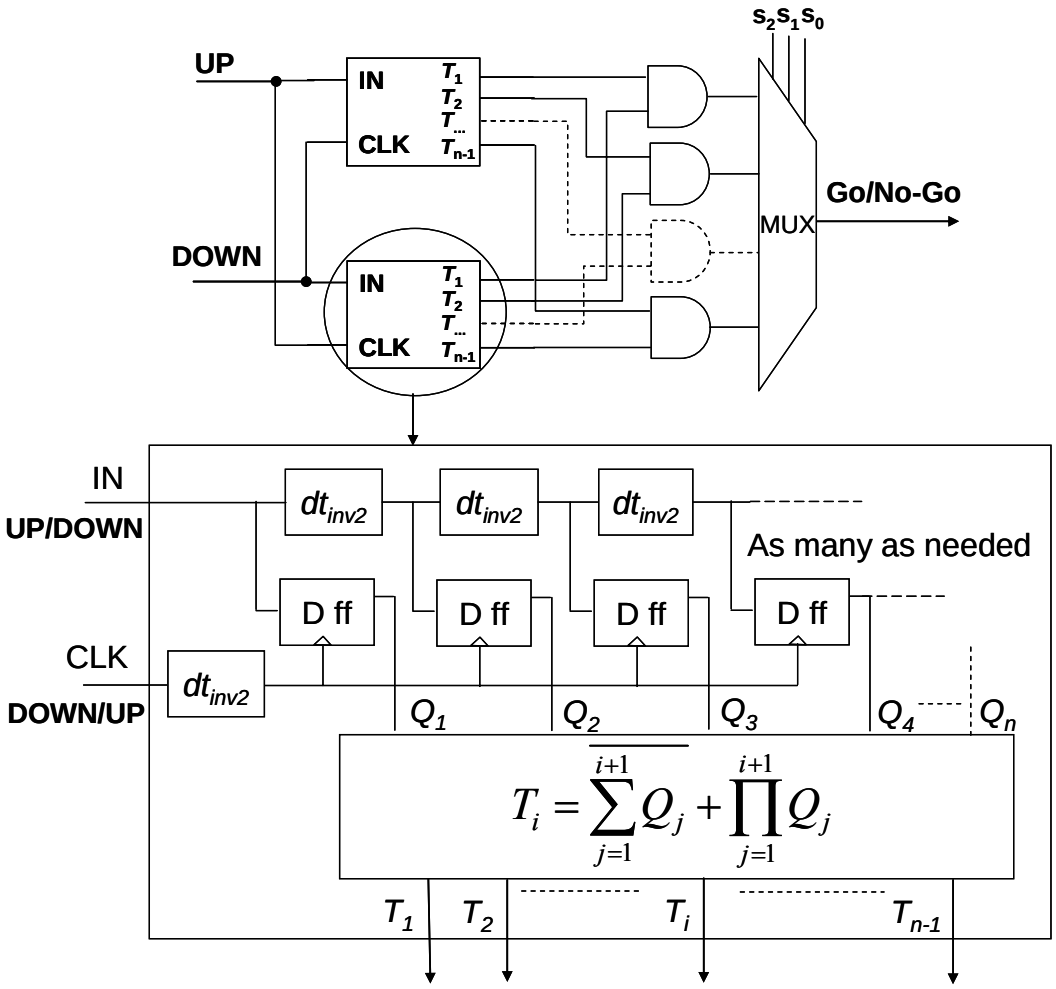


Fig. V-6. PFD monitor schematics

Simulations show that it may occur that $I_{down} > I_{up}$ or that $I_{up} > I_{down}$ in the same CP design according to process deviations. In the first case, the PFD output signal *UP* has a duty cycle which is larger than the PFD output signal *DOWN*. In the second case, the signal *DOWN* has a larger duty cycle compared with the *UP* signal of the PFD. Thus, the BIST needs to consider both configurations: one with the output *UP* signal of the PFD connected to the input *IN* pin of the monitor and *DOWN* signal to the *CLK* pin of

the monitor (top monitor core), and a second one connected the opposite way (bottom monitor core), as in Fig. V-6.

From now on only the case of $I_{down} > I_{up}$ which activates the top monitor core of Fig. V-6 will be treated unless differently specified, due to the symmetry of the configuration (this case was illustrated in Fig. II-7).

Referring to the monitor core detailed in Fig. V-6, the PFD *UP* signal is applied at the *IN* pin of the PFD monitor. This signal is delayed by means of *n*-1 delay elements. D flip-flops are connected at the output of each delay element. The *DOWN* signal of the PFD is applied to the *CLK* pin of the monitor that provides the sampling rate to the D flip-flops to sample the delayed *UP* signal. The *DOWN* signal is also delayed by one delay element in order to respect timing constraints of the first D flip-flop in the ideal case that *UP* and *DOWN* rising edges are perfectly aligned, avoiding metastability phenomenon. The outputs of the D flip-flops, Q_1, Q_2,..., Q_i,..., Q_n in Fig. V-6, give a signature, reported in Tab. V-1, that will be used to take a Go/No-Go decision. The PLL is not working properly and/or mismatch is not within specifications if all D flip-flop outputs are equal to 1 or 0 at the same time. This will be illustrated in more detail later. The logic function to obtain the Go/No-Go test signal is then given by $T_i = \overline{\sum_{j=1}^{i+1} Q_j} + \prod_{j=1}^{i+1} Q_j$ where 0 = Go and 1 = No-Go. T_i in Fig. V-6 is the result of this Boolean operation on the D flip-flop outputs of the number *i* of delay elements. The actual digital signal T_i considered as BIST output will depend on the maximum mismatch tolerated.

A MUX may be used to set the maximum delay mismatch tolerated by selecting a given number *i* of delay elements to compute the Go/No-Go test signal, selecting the wanted T_i output. For example, a MUX with three selection pins (8 possible mismatch delay selectable) gives the range of valid signatures for the PFD monitor shown in Tab. V-1, in the case that 8 delay elements are used on the *IN* signal with $dt_{inv2} \approx 25$ ps and 9 D flip-flops. Note that *X*s represent either 1s or 0s, and only sequences of 1s followed

by sequences of 0s are possible. For instance, if the MUX is set to 011 (maximum tolerated mismatch of 75 ps), the number of delay elements required is $i = 4$ and the Go/No-Go output will be equal to T_4 that will be equal to 0 (Go) if the D flip-flop signatures are 1XXX00000 (mismatch below 75 ps) and 1 for all signatures equal to 11111XXXX (mismatch above 75 ps).

MUX	Max mismatch in ps	Selected T_i	Allowed D ff signatures
000	0	T_1	100000000
001	25	T_2	1X0000000
010	50	T_3	1XX000000
011	75	T_4	1XXX00000
100	100	T_5	1XXXX0000
101	125	T_6	1XXXXX000
110	150	T_7	1XXXXXX00
111	175	T_8	1XXXXXXX0
Step in ps	25		

Tab. V-1. Selection of maximum delay mismatch

When the MUX is set to include all the delay elements present in the monitor, the signature obtained at the D flip-flop outputs can also be used to estimate the actual delay mismatch of the PLL. For instance, referring to Tab. V-1, if the obtained signature is 111100000, the delay mismatch must be in the range from 50 ps to 75 ps. This may be seen as using the monitor in an « inverse sense », evaluating mismatch of the PLL instead of verifying that the PLL has a mismatch below a wanted value selectable by the MUX and obtaining a Go/No-Go output. It is also possible to scan out this signature for off-chip test processing if required. If mismatch specifications need to be programmable externally and the MUX solution appears too limited, a JTAG may be introduced to compare externally programmable words with the D flip-flop outputs.

Nevertheless, if finer discrimination for mismatch detection is desired, Vernier Delay Lines may be used instead of a simple delay line to obtain sub-gate resolution and/or independence from technology, but BIST area overhead will increase and metastability will become an issue eventually (as it always does when high resolution for discrimination is needed). Also, faster D flip-flops and frequency counters will have to be involved.

The following faulty cases, with the associated BIST monitor signatures, may occur at the PFD output once the PLL lock time has been exceeded:

- Case 1: All 1s at D flip-flop outputs

  a) f_{loop} lags f_{ref} : positive phase shift over specification tolerance that activates the top monitor core of Fig. V-6 with *UP* signal as *IN* and *DOWN* signal as *CLK* corresponding to $I_{down} > I_{up}$. Or f_{loop} leads f_{ref} : negative phase shift over specification tolerance that activates the bottom monitor core of Fig. V-6 with *DOWN* signal as *IN* and *UP* signal as *CLK* corresponding to $I_{up} > I_{down.}$

  b) f_{loop} is slower than f_{ref} : top core active. Or f_{loop} is faster than f_{ref} : bottom core active.

  c) *UP* stuck at 1

- Case 2: All 0s at D flip-flop outputs

  d) *UP* stuck at 0

Fig. V-7 illustrates simulation results for the first two fault conditions of Case 1 (all 1s at D flip-flop output), the other ones c) and d), corresponding to stuck-at faults, being evident.

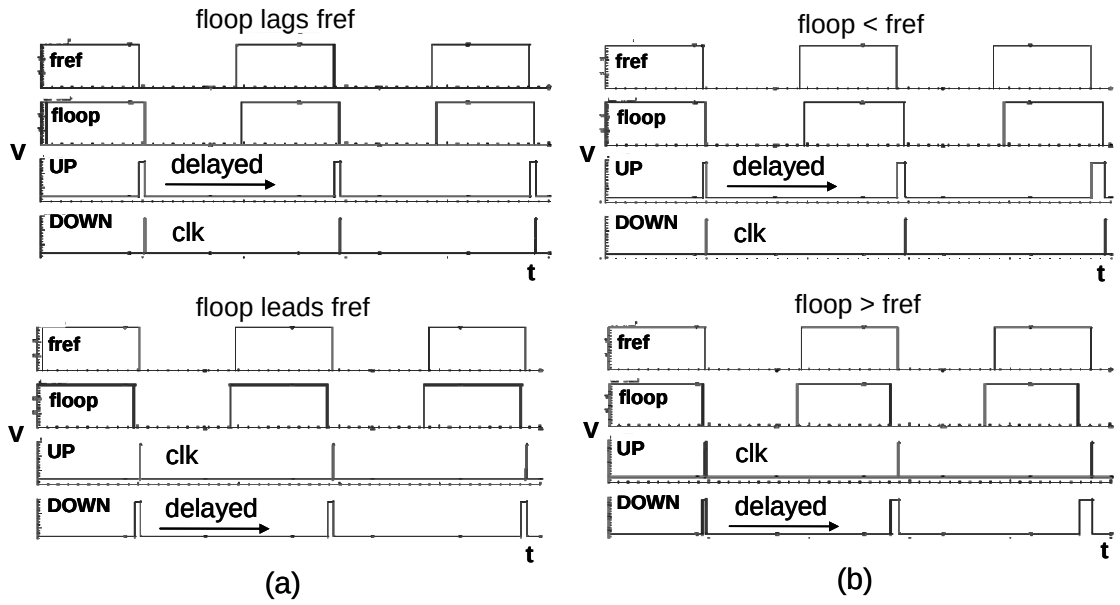
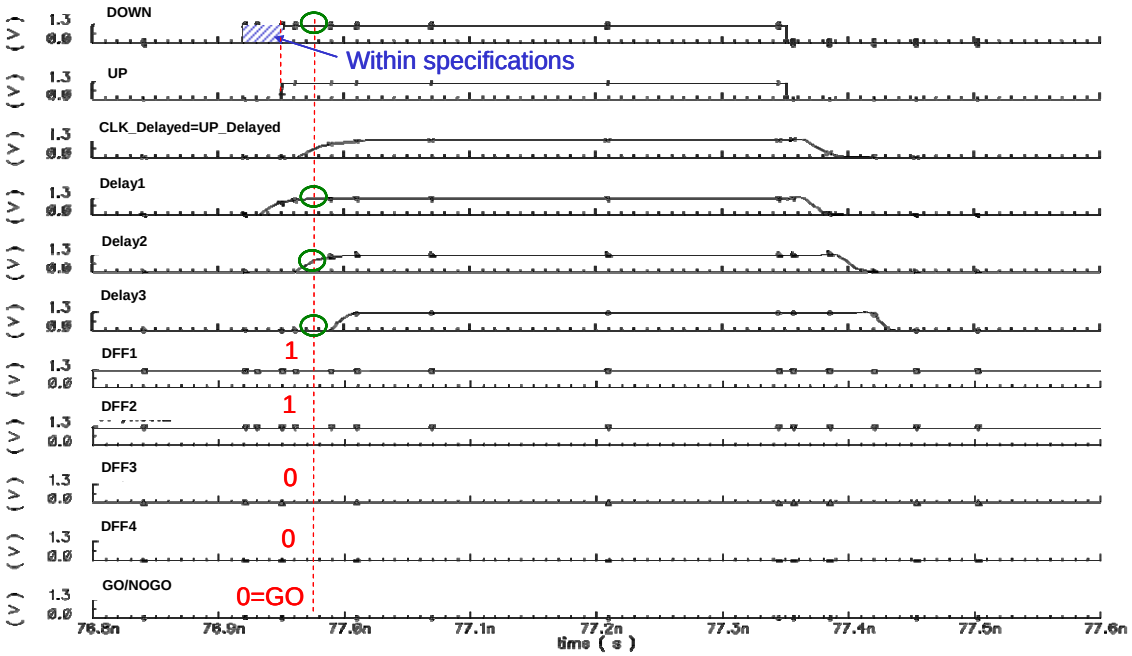


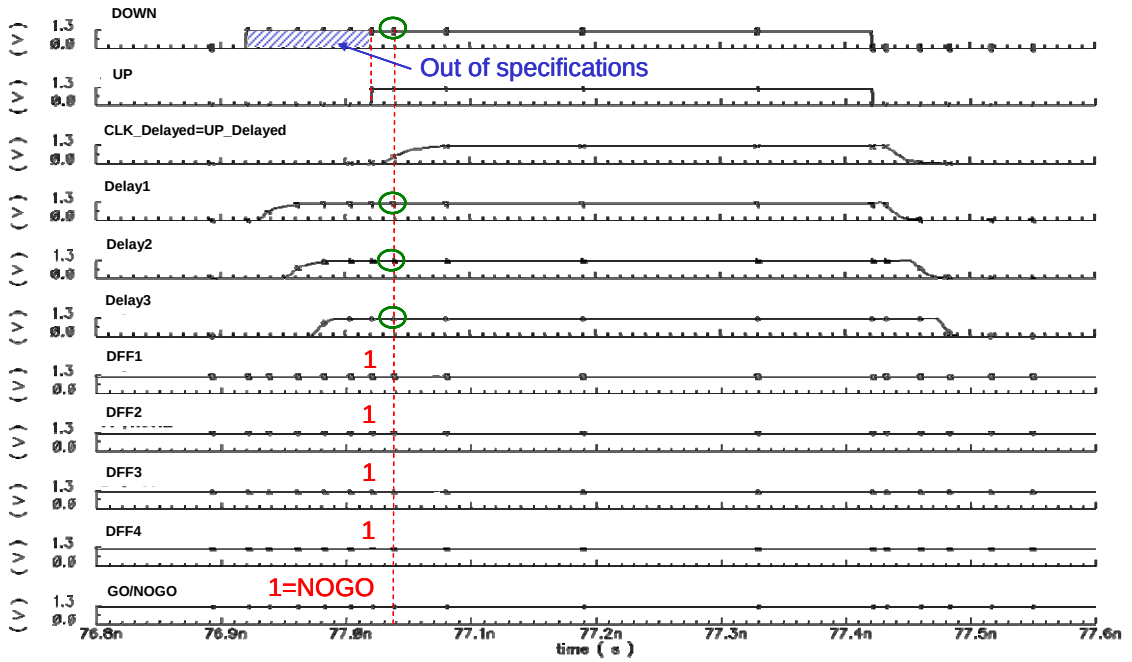
Fig. V-7. Chronogram of the PFD signals under different fault cases: (a) phase difference between f_{loop} and f_{ref}, and (b) frequency difference between f_{loop} and f_{ref}

The falling edges of both signals *UP* and *DOWN* are always aligned under normal PFD operation, the variation in duration of each signal occurs on the rising edges (sensitive edges). In the faulty Case 1 a), depicted in Fig. V-7 (a) the rising edge of the delayed *UP* (*DOWN*) signal is constantly too early with respect to the clock *DOWN* (*UP*) signal which will be in condition of sampling only 1s. In the faulty Case 1 b) of Fig. V-7 (b), the rising edge of the delayed *UP* (*DOWN*) signal is constantly increasing its distance with respect to the clock *DOWN* (*UP*) signal which will be again in condition of sampling only 1s.

In Fig. V-8 all signals of the PFD monitor core with 3 delay elements and 4 D flip-flops (as in Fig. V-6) are simulated. This configuration allows mismatch up to 50 ps. Two cases are shown: in Fig. V-8 (a) mismatch is 30 ps, thus within specifications and in Fig. V-8 (b) mismatch is 80 ps, thus out of specifications.



(a)



(b)

Fig. V-8. PFD monitor core simulations with tolerated mismatch of 50 ps (a) mismatch of 30 ps within specification and (b) mismatch of 80 ps out of specification

By monitoring the Go/No-Go output signal it is possible to identify the time at which the lock state is reached, as shown in Fig. V-9. Thus, this technique may be used also as a lock detect. In fact, the Go/No-Go signal goes to the low logic value (Go) when the rising edges of the *UP* and *DOWN* signals are delayed with respect to each other of less than the maximum tolerated delay mismatch. In the simulation results shown in Fig. V-9 the delay mismatch between the *UP* and *DOWN* signals is of 85 ps (see zoom) and the BIST monitor was set to give a Go (low) output for a delay less than 100 ps.

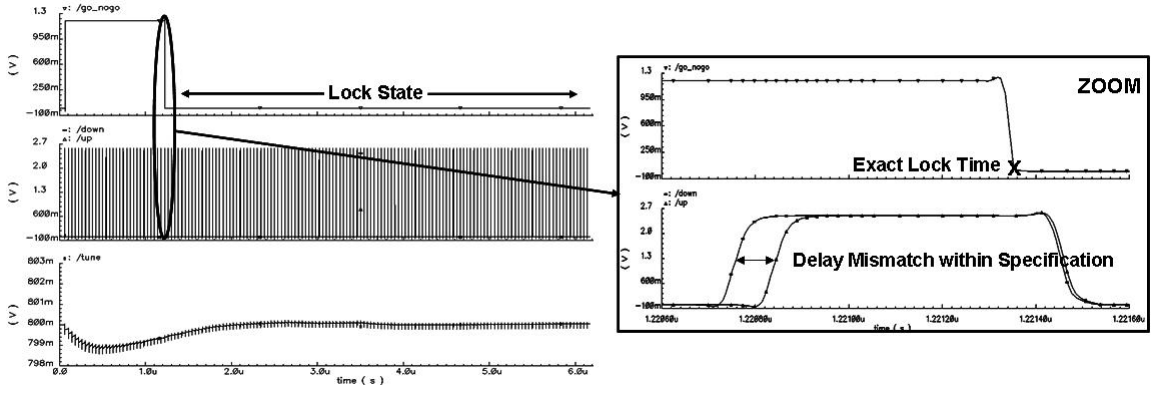


Fig. V-9. Go/No-Go output as lock detector

Nevertheless, the lock time found by the BIST monitor in this specific simulation (1.22 μs) is not the actual lock time of the PLL since a VerilogA block together with an initial condition on V_{tune} have been introduced to speed up the lock state condition of the PLL (see Fig. IV-11). Otherwise simulations lasted too long as already discussed in section 4.4.2. The BIST output will thus be able to give the exact lock time and state information once inserted in the IC. However, lock detectors commonly used on industrial PLLs cannot indicate a lock state with a resolution better than 100 ps. In our case, resolution can be chosen much higher than this (down to 25 ps in our case-study).

At some sampling D flip-flop stage, a metastability phenomenon may occur giving an uncertain result in one bit of the signature (with the exception of the first one thanks to the delay element introduced to avoid metastability in ideal conditions). This is not an issue when the uncertain bit is not at the beginning or at end of the chain, since a

commutation from a 1s' sequence to a 0s' sequence in the signature (see Tab. V-1) will occur anyway. Nevertheless, a yield loss increase may take place in the rare and unfortunate eventuality that metastability occurred at the last D flip-flop of the selected delay chain. A technique similar to the one chosen to avoid metastability on the first D flip-flop may be pictured as future work.

The layout of the BIST monitor of Fig. V-6 has been implemented and the total surface is of 882 μm^2. The layout shown in Fig. V-10 has room for optimization in terms of silicon area.

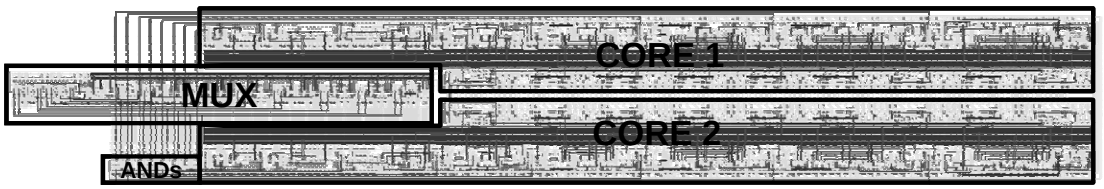


Fig. V-10. PDF output monitor layout

Unlike the other two monitors applied to the VCO and described earlier in this chapter, this monitor is completely digital. By probing only digital, low frequency nodes, this monitor is totally transparent to PLL operation mode. Furthermore, layout dimensions show that the area overhead is very small compared to IP size (less than 0.87 %).

5.5 Worst Case Simulations for BIST Robustness Verification

In Tab. V-2, typical and worst case conditions are reported. They are the same conditions used to analyze the CP behavior (see section 4.4.2). The value of *Vdd* varies accordingly to simulation conditions as shown in Tab. V-2. This is why voltage trends are not completely superposed for worst cases and nominal case conditions.

	TYP	SLOW	FAST
T in °C	25	105	-30
Vdd in V	1.2	1.08	1.32
Corners	TT	SSA	FFA

Tab. V-2. Typical and worst case conditions on temperature, Vdd, and corners

5.5.1 BICS

The BICS in [42] was claimed to be very robust to process deviations. In fact, robustness of the modified BICS is very good for I_{meas}, as depicted in Fig. V-11. In this figure variations with process deviations (SSA, TYP, FFA) of I_{meas}, I_{max}, I_{min}, V_{max}, V_{min}, and the Go/No-Go output of the BICS are depicted versus *Idd*. For *Idd* = 8.07 mA (nominal value of the VCO) the values of I_{meas} in nominal and worst case conditions are given is Tab. V-3, together with the maximum I_{meas} variation $max\Delta I$ among corner conditions. For the robustness of the reference current sources, I_{min} and I_{max}, fast worst case shows little variations with respect to nominal values, although it proves to be a little less good for slow worst case, as depicted in Fig. V-11 and in Tab. V-3. This is clearly seen in the Go/No-Go signal of Fig. V-11. The rising and falling edges of this signal vary significantly in the case of the slow worst case simulation. Probably, design of current sources may still be improved for better robustness in slow worst case conditions.

In all worst case simulations *Vdd* voltage level is different from typical value (± 10 % from nominal value 1.2 V): this is visible on the high logical level of every worst case voltage measure and on the Go/No-Go output.

	TYP	SLOW	FAST	TYP-SLOW	FAST-TYP	maxΔI
I_{meas} in μA (@ *Idd = 8.07* mA)	761.1	728.7	773.9	32.4 (4.3 %)	12.8 (1.7 %)	45.2
I_{min} in μA	745.9	654.9	768.1	91 (12.2 %)	22.2 (3 %)	113.3
I_{max} in μA	931.7	815.3	959.8	116.4 (12.5 %)	28.1 (3 %)	144.5

Tab. V-3. Typical and worst case conditions on BICS currents

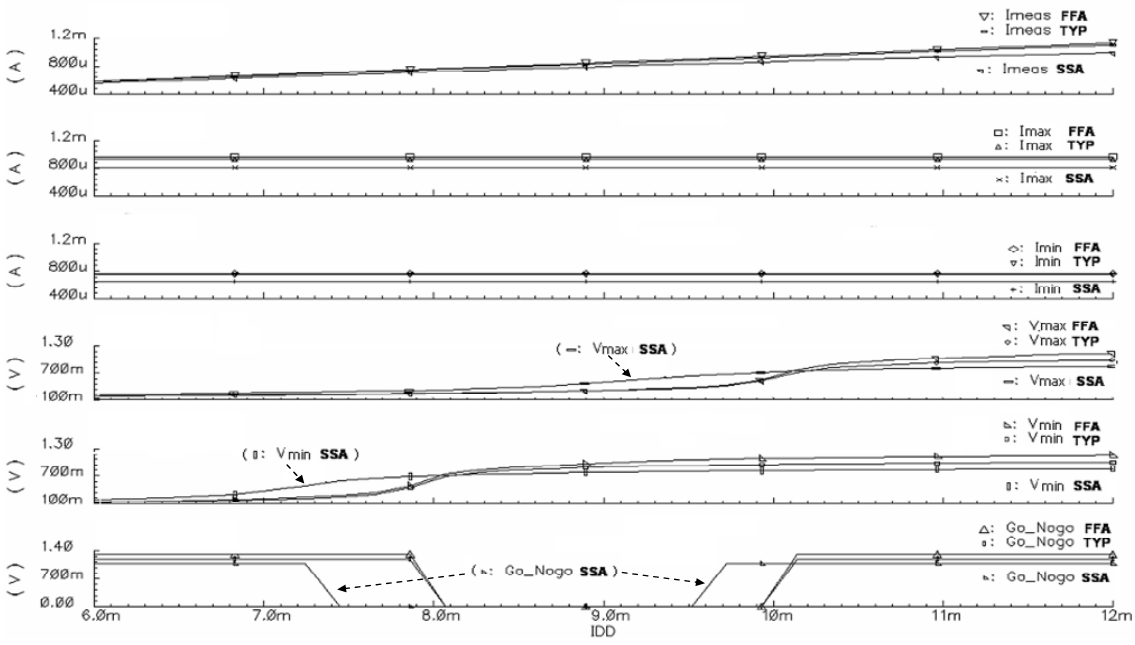


Fig. V-11. BICS variation in typical and worst case conditions

5.5.2 Voltage Comparator

In the case of the voltage window comparator, design is without any doubt extremely robust as shown in Fig. V-12, which depicts variations with process deviations of V_{max}, V_{min}, and the Go/No-Go output of the voltage comparator versus V_{alc}.

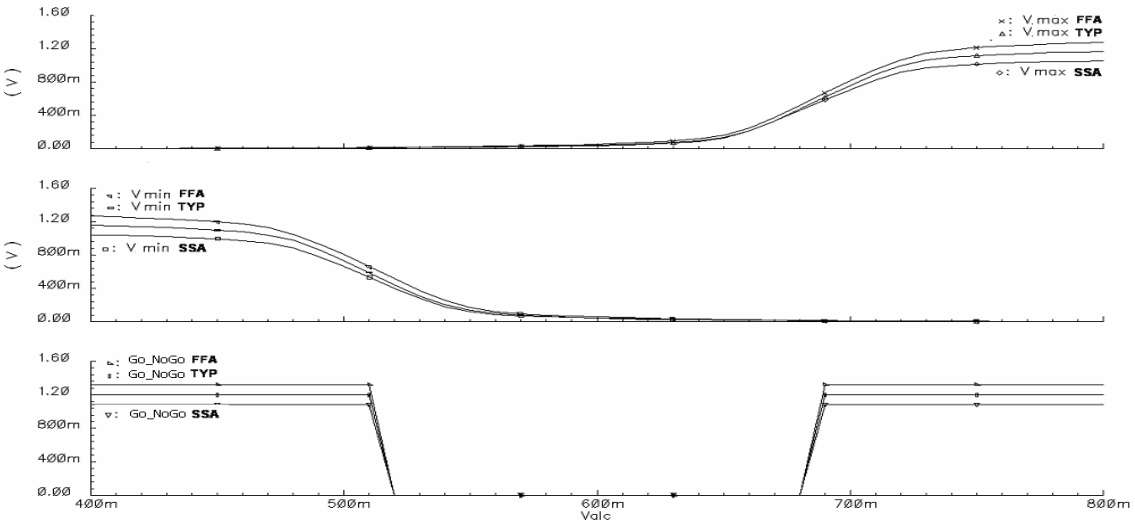


Fig. V-12. Voltage window comparator variations in typical and worst case conditions

5.5.3 PFD Monitor

Worst case simulations have been carried out also on the PFD BIST in order to verify the delay sensitivity of a delay element to process deviations. In this case too the same typical and worst case conditions as in Tab. V-2 have been used. Tab. V-4 shows the results obtained.

MUX (s2_s1_s0)	Delay UP_DOWN TYP in ps	Delay UP_DOWN SSA in ps	Delay UP_DOWN FFA in ps
000	0	15	0
001	25	60	15
010	50	105	30
011	75	150	45
100	100	195	60
101	125	240	75
110	150	285	85
111	175	335	100
Step in ps	25	~45	~15

Tab. V-4. Typical and worst case simulation on delay values of the PFD output monitor

As already stated, process dependency is a typical issue common to all delay lines. Among the multiple solutions well known in the literature to calibrate a delay line, the ring oscillator technique (discussed in section 3.3.5, Fig. III-17) seems the best suited. It may be either applied on the whole inverter chain at once or on each inverter separately, according to the wanted degree of accuracy. Concerning the reference clock for the frequency counter, a stable (process invariant) reference like the quartz may be easily recovered on-chip. Once defined the average delay element value or the single delay element value in the chain by calibration, the desired mismatch may be selected by the MUX keeping into consideration the process variation (a simple table of possible process deviation intervals versus MUX selection may be built on-chip). Since this technique is well known, it has not been designed and simulated on the PFD monitor during this work.

5.6 Impact of BIST Monitors on PLL Performances

Simulations on VCO performances with embedded sensors have been carried out: phase noise degradation and output frequency deviation are negligible. In fact, phase noise degradation is of only 1.2 dBc/Hz at 10 MHz from carrier as shown in Fig. V-13 and VCO output frequency varies from 7.686 GHZ without BIST monitors to 7.664 GHz with BIST monitors, which means a difference of only 22 MHz.

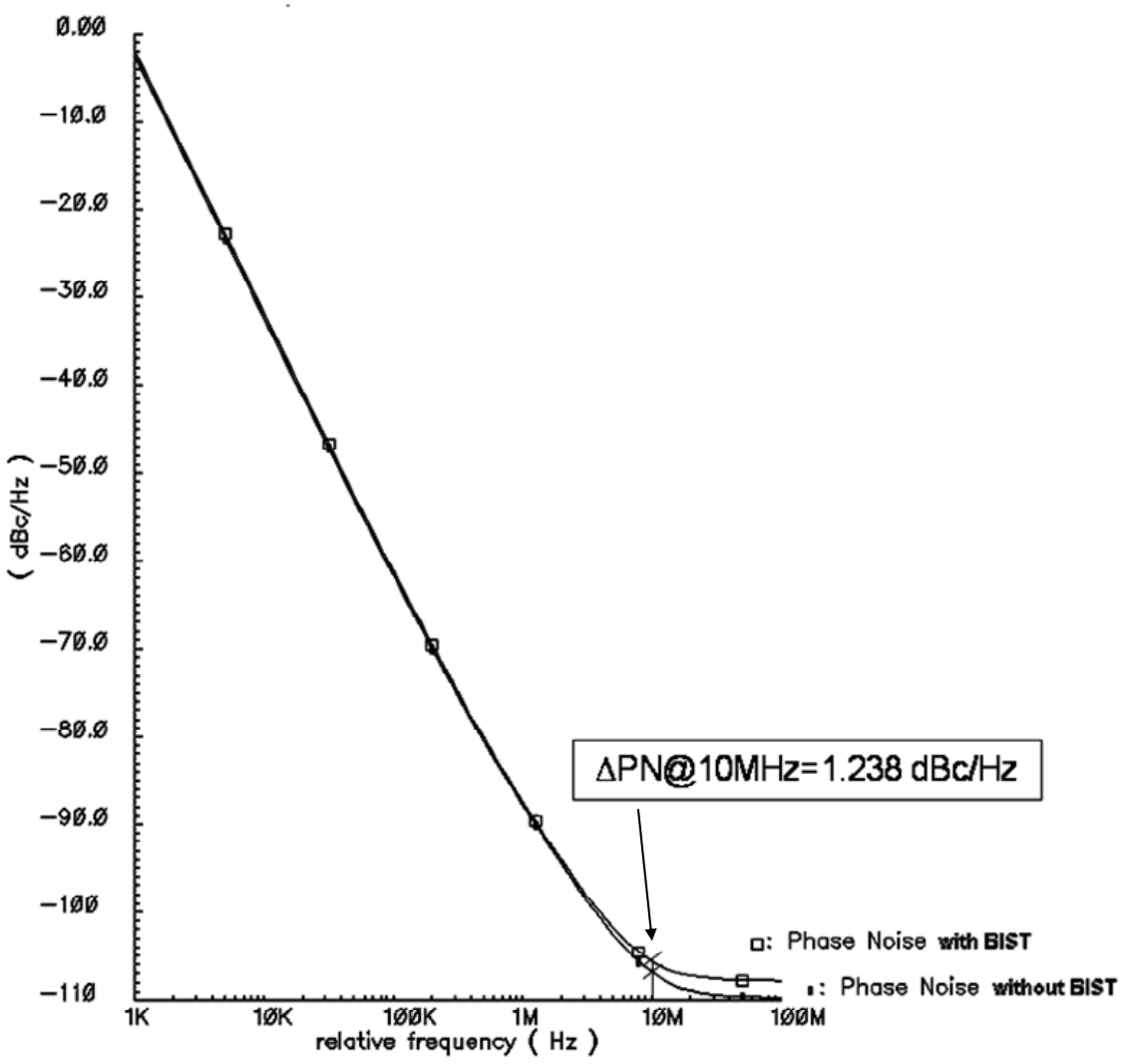


Fig. V-13. VCO phase noise with and without BIST monitors

VCO current consumption is obviously higher in presence of the BIST monitors. Current consumption of the VCO plus the output buffer, without BIST, is of 18.39 mA while in presence of the BIST monitors the overall current consumption becomes 34.84 mA, which means that the BIST monitors consume 16.45 mA.

The BICS is composed of three blocks as in Fig. V-2. The BICS sensor (a) contributes with a consumption of 0.612 mA, the BICS comparator (b) with 2.831 mA, and the reference generator (c) with 12.58 mA, which makes a total contribution to consumption of the BICS of approximately 16 mA. The voltage window comparator contributes to current consumption with approximately 0.5 mA. Current source $I_{ref} = 9$ mA is needed only in case BICS references sources, $I_{min} = 745.9$ μA and $I_{max} = 931.7$ μA, need to be as sensitive to process deviations as the BICS comparator (I_{min} and I_{max} vary the same way as I_{meas} with process deviations). In fact, I_{ref} in the reference generator is there to substitute VCO *Idd* that flows in the current comparator. If only simple references are requested, not varying the same way as the BICS comparator (thus without considering the I_{ref} source contribution to consumption) the additional current consumption of the BIST monitors applied to the VCO is of 7.45 mA + 745.9 μA + 931.7 μA = 9.13 mA. Moreover, the BICS may be conceived as switchable, thus it would contribute to overall current consumption only during the test phase.

The PFD output monitor does not degrade PLL performances since it probes digital, low frequency nodes. The average current consumption over a simulation time of 100 ns of this monitor is 34.27 μA, which is a very low value compared to the other monitors.

5.7 Conclusions

Three BIST monitors have been designed and validated through simulation to measure on-chip the chosen test measures for the VCO and the CP blocks of the PLL case-study. Two of these monitors, the BICS and the voltage comparator, have been applied to the

VCO, which is the most sensitive block of the PLL. The BICS may be applied to any block of the PLL if needed. The PFD monitor has been applied to the whole PLL in closed-loop configuration to detect faults on all the blocks of the PLL that produce a mismatch above specifications between the *UP* and *DOWN* signals at the PFD output. This mismatch may be typically due to current mismatch in the CP block, but also to leakages in the LPF and other faults impacting the phase or the frequency of the loop signal.

The three monitors have proved to be robust to process deviations. Robustness to slow process deviations of the BICS reference sources may yet be improved.

Layout of the BICS core has been carried out leading to a rough estimation of the area of the whole BICS of 3250 μm^2, corresponding to 3.2 % area overhead for the PLL case-study. Layout of the voltage comparator existed in 65 nm technology and its area is 2519.772 μm^2 which means 2.47 % area overhead with respect to the PLL case-study. Layout of the PFD monitor occupies 882 μm^2, corresponding to less than 0.87 % area overhead of the PLL case-study. Area overhead of all BIST monitors is thus about 6.54 % of the SERDES PLL used as case-study.

The three BIST monitors have very small impact on PLL performances with exception of current consumption of the BICS. On the other hand, the BICS may be made switchable in order to limit consumption in ordinary device operation.

Chapter VI

Results of PLL BIST Simulations

6.1 Introduction

Before embedding the monitors on the DUT, limits on test measures must be set in order to appropriately design the monitors so as to be robust in the range of operation. These limits are set considering process deviations, so that the BIST results in the best tradeoff possible between yield loss (rejection of good circuits) and defect level (acceptance of bad circuits). A statistical model of the DUT is necessary to set these limits. This approach for fixing test limits and evaluating yield loss, defect level, and fault coverage has been carried out in different works including [9], [10], [47], [48].

Once test limits are set, fault coverage is evaluated for injected faults. At transistor level, the model adopted is the one suggested by Galiay, Crouzet, and Verginault [46], which includes shorts between the three transistor terminals, and opens on drain and source contacts. Likewise, for passive components, shorts between terminals and opens on contacts have been considered. Opens in transistor gates have not been injected since they may need to include parasitic capacitances of the floating node which must be extracted from the layout. This is quite a long and complicated procedure to carry out on all transistors of the PLL chosen as case-study. Shorts have been modeled as a 1 Ω resistance and opens as a 10 MΩ resistance. Research works in the test community commonly use such catastrophic fault models for analog circuits to judge the effectiveness of a test technique. Thanks to this procedure fault coverage results are obtainable in a reasonable simulation time; considering other models, such as

parametric faults, would lead to a prohibitive simulation time [36]. Thus, in this work, only catastrophic faults have been considered.

All simulations are carried out in the CADENCE SPECTRE RF environment. Fault injections are automated thanks to a CAT platform (RMSCATPlatform [10]) that runs in CADENCE.

6.2 Catastrophic Fault Coverage Results for the VCO

Since the VCO under study is tunable, its configuration is set to enable all transistors in the varactor, in order to carry out a complete test. In this configuration, the number of catastrophic faults injected in the VCO amounts to 108 (shorts and opens).

Limits for the test measures must be set to minimize parametric defect level and yield loss and to optimize fault coverage. A catastrophic fault simulation campaign has been carried out to compute catastrophic fault coverage (CFC) as a function of test limits as shown in Fig. VI-1. The limits of a test measure are given as $\mu \pm x\sigma$ and CFC is plotted as a function of x. The CFC of combinations of performances and test measures may be also considered, various combinations are also shown in Fig. VI-1, where x is the same for all performances and test measures.

The combination of all performances (phase noise, VCO gain, and current consumption) shows the highest catastrophic fault coverage of all (above 80 %) up to 2.5σ from nominal value. Beyond 2.5σ the CFC given by combination of all test measures (current consumption, V_{alc}, and output frequency) becomes higher than the actual CFC of the performances. In this case, a test based on test measures would introduce some yield loss compared to a test based on specifications. Nevertheless, since catastrophic faults are indeed present in the circuit, detecting the ones that do not impact the device operation in the test configuration chosen for simulations will lead to a more reliable device put on the market. In fact, the simulated configuration is conceived to activate the most possible parts of the device under test in order to be exhaustive, but not all

standard operation mode configurations have been simulated. Some faults could have an impact on the device operation in other configurations and thus be detected by the BIST. According to the aim the device has on the market, a choice on test measures may be done also considering the tradeoff between yield loss and reliability.

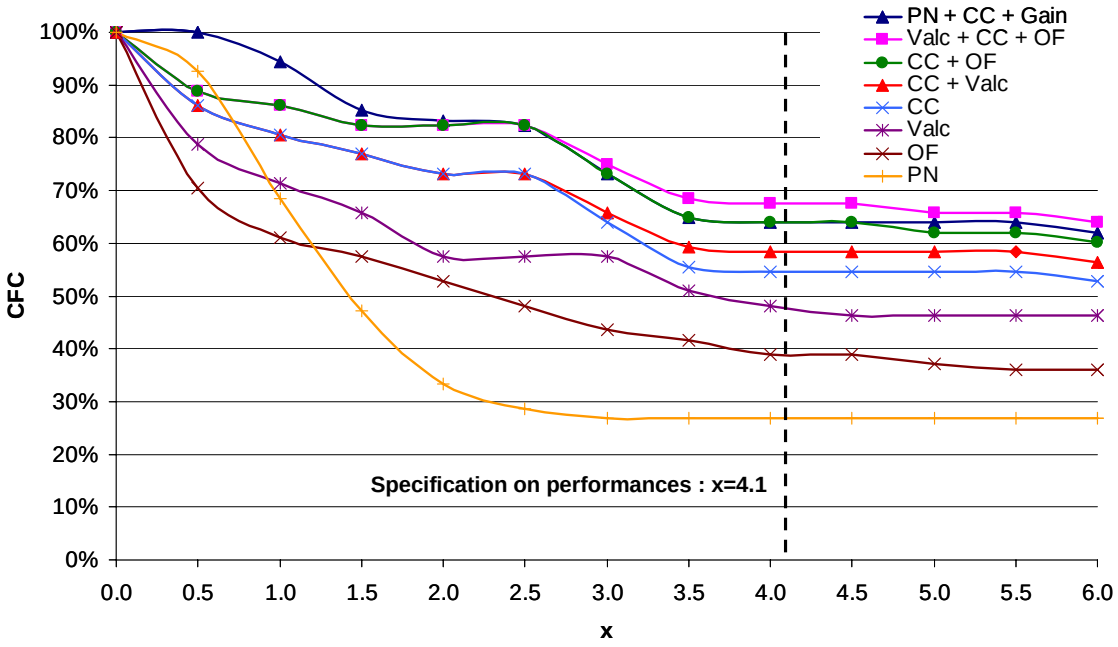


Fig. VI-1. VCO catastrophic fault coverage versus test limits

In order to comply with specifications, limits on performances should be set at 4.1σ. Specifications thus cover only 64 % of all catastrophic faults injected in the simulated configuration. This points out the fact that the circuit is robust to some catastrophic faults, which is indeed possible in some specific cases, such as shorts injected between terminals with the same polarization or faults injected in branches that are not active in the specific configuration, and so on. Moreover, since the datasheet for this device is still at draft stage, it may be possible to either modify specifications or add VCO output power to the set of performances, as it is often done for VCOs, and which has been here considered as a test measure, relating it to V_{alc} measure. This would bring the CFC of test measures and performances to the same level. This may be explored if designers will decide to add output power to specifications.

Examining results obtained for various combinations of test measures, it may be stated that each test measure adds some fault coverage to the others, thus none is redundant. In fact, measuring V_{alc} adds 4 % of CFC to the case in which CC alone is measured, and 3.7 % of CFC to the case in which $CC + OF$ are measured. An overall CFC of more than 65 % is obtained considering all test measures ($CC + V_{alc} + OF$), about 10 % more than considering only $CC + V_{alc}$.

Actually, the analysis carried out on performances and test measures in Fig. VI-1 where all limits vary together, although interesting for certain considerations done up to now, is not formally correct since performances are fixed at 4.1σ by specifications. Varying limits on performances is contradictory since they are defined by specifications, yet it is of some interest in order to study the robustness of the circuit towards performances. Thus, it would make more sense to plot the CFC making only V_{alc} test limits vary and keeping the performances used as test measures fixed at 4.1σ. In Fig. VI-2 this situation has been depicted. CFC remains constant at 67.6 % after 2.5σ of V_{alc}.

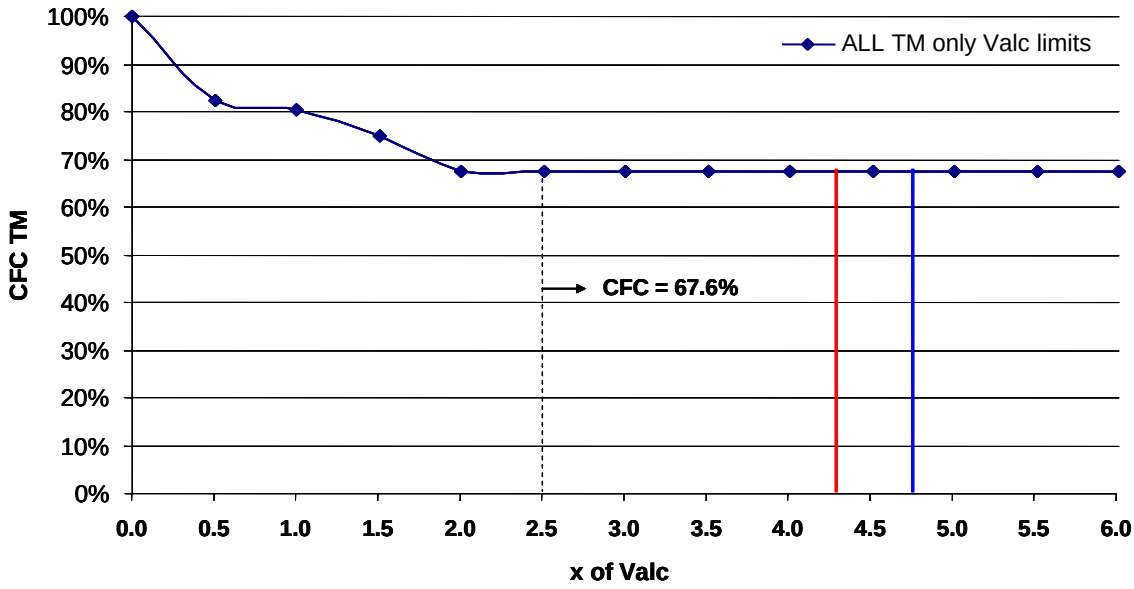


Fig. VI-2. CFC of all test measures versus Valc test limits

At 4.1σ almost all faults that are not detected by performances are not detected by the test measures either, except for 4 faults over 108 (3.7 %) that are detected by the only

test measure which is not a performance: V_{alc}. This is also why the CFC is higher for test measures than for performances. These 4 faults are opens on the pmos transistors used as current sources for the VCO and biased by V_{alc}. These faults are obviously only detectable by a power related measure since if one of the pmos transistors used as current sources (in parallel) is open, the others will continue to inject enough current to guarantee VCO operation, the only drawback being less oscillation stability to process variations. All the other faults are either detected by both performances and test measures, or not detected by either of them. Plenty of these faults are opens on ALC and VCO coupling capacitors. Some are opens on VCO nmos transistors that are not active in this configuration. Others are shorts between terminals of nmos transistors on the VCO that are at the same constant voltage. Non-detected faults may also be redundant, such as non-detected opens on drains and non-detected opens on sources of the same transistor used as a pass transistor. As previously stated, these non-detected faults are due to either robustness of the device, or to the fact that the chosen configuration, although it is the optimal one (being the one that activates the greatest part of the device), may still have some deactivated branches.

6.3 Test Metrics Results and Optimized Test Limits for the VCO

As already mentioned, test limits must be set in order to optimize CFC and parametric defect level and yield loss. Using the statistical model of section 4.3.3 obtained from a population of 1000 Monte-Carlo instances, defect level and yield loss considering all three test measures for process deviations are plotted in Fig. VI-3 as a function of the test limit x of V_{alc}. The optimal test limit must consider a tradeoff between defect level and yield loss and it refers to the V_{alc} test measure only because the limits for the other two test measures (current consumption and output frequency) are set by specifications, being these two test measures also performances. The limit on all the performances has been set to 4.1σ, to comply with specifications. This generates 3985 non functional devices on the population of 1 million devices.

Setting defect level equal to yield loss (right line in Fig. VI-2 and Fig. VI-3), the statistical model gives a value of 1 ppm for V_{alc} at x = 4.75 approximately, which results in a CFC of 67 %. Considering acceptable to have a yield loss ten times larger than defect level according to the rule of ten [51] (left line in Fig. VI-2 and Fig. VI-3), the statistical model gives a defect level of approximately 1 ppm, yield loss of 10 ppm, and CFC always of 67.6 % with the V_{alc} limits set at x = 4.3. In this specific case, the rule of ten is not worth while using since it only adds yield loss without improving significantly either fault coverage or defect level. In generic cases, a choice of test limits has to be made according to product and customer requirements on test metrics.

Considering the performances chosen as test measures (*CC* and *OF* without considering V_{alc}) with limits set at x = 4.1 as imposed by specifications, defect level is equal to 2 ppm and yield loss is equal to 1 ppm. This result is not very different from the one obtained for the three test measures with only V_{alc} test limits that vary, thus V_{alc} would seem to be unnecessary. CFC though, is 3.7 % higher when considering also V_{alc}, as stated in the previous section. So the optimized set of test measures is actually *CC*, *OF*, and V_{alc}.

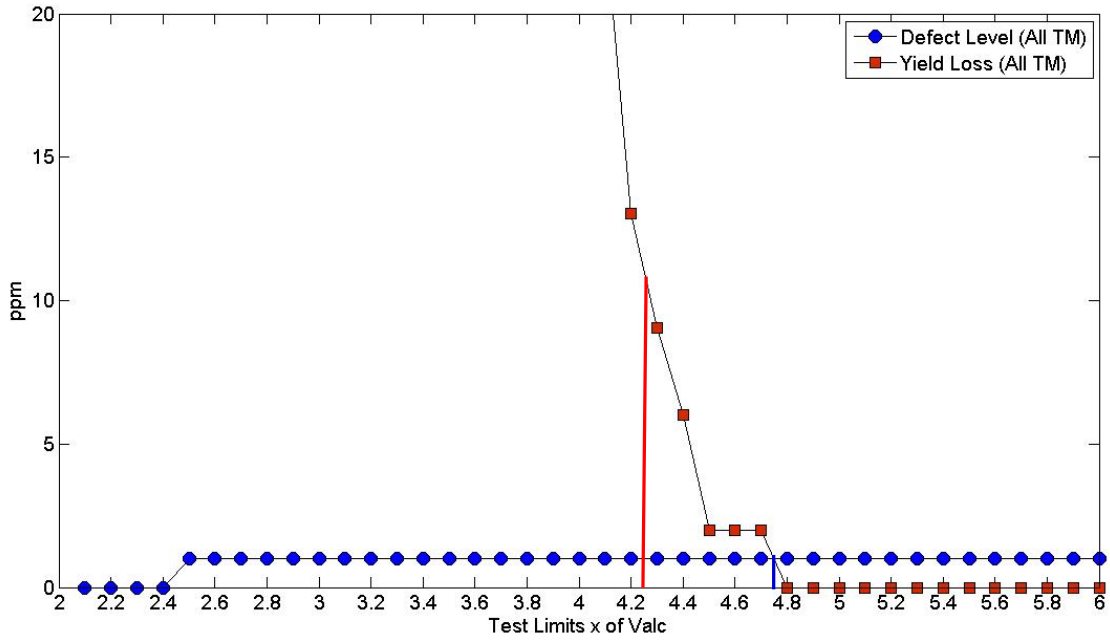


Fig. VI-3. Parametric defect level and yield loss of all test measures versus V_{alc} test limits

In Fig. VI-4, the limits of all test measures vary in the same way with the assumption that test measures are completely independent from performances, despite the fact that two out of three are actually performances and thus their limits are normally set by specifications. This has been plotted to see if yield loss and defect level may increase setting different limits on performances that are used as test measures.

To obtain a yield loss equal to defect level, limits on all test measures must be set at approximately $x = 3.2$ which gives 3100 ppm. According to the rule of 10 instead $x = 2.8$ for which a yield loss of 10850 ppm and a defect level of 1200 ppm are obtained. It is evident that this situation is not optimized, and it was to be expected since specifications on performances are set to be optimum from a metrics point of view.

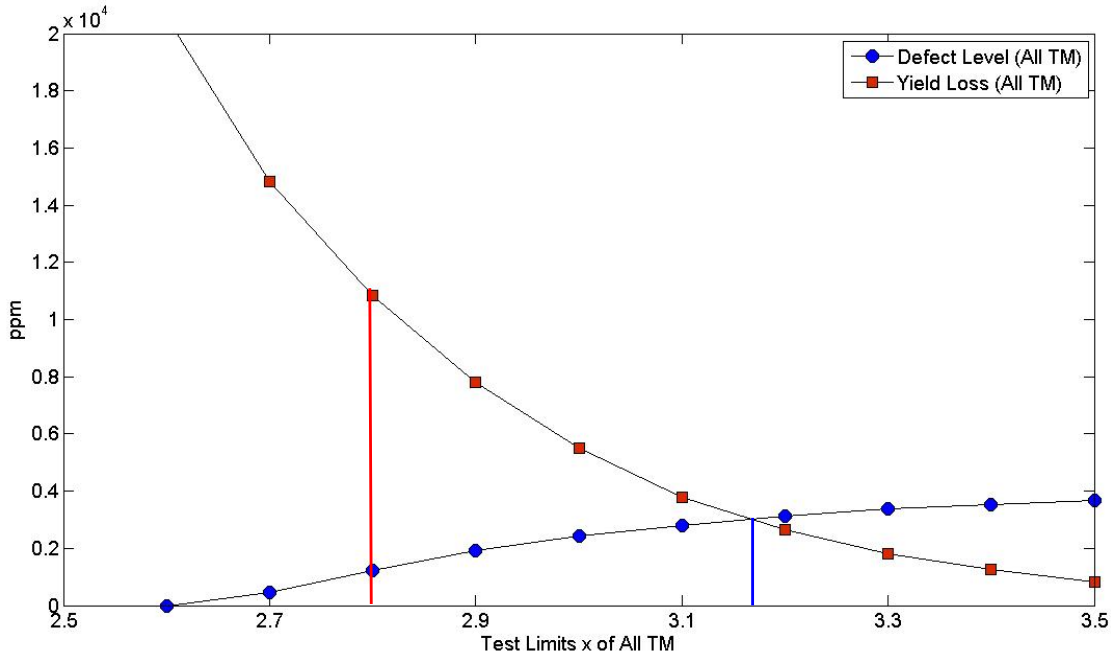


Fig. VI-4. Parametric defect level and yield loss of all test measures versus limits of all test measures

In Fig. VI-5 to Fig. VI-7, parametric yield loss and defect level versus test limits of each test measure alone have been plotted in order to evaluate the chosen test measures separately.

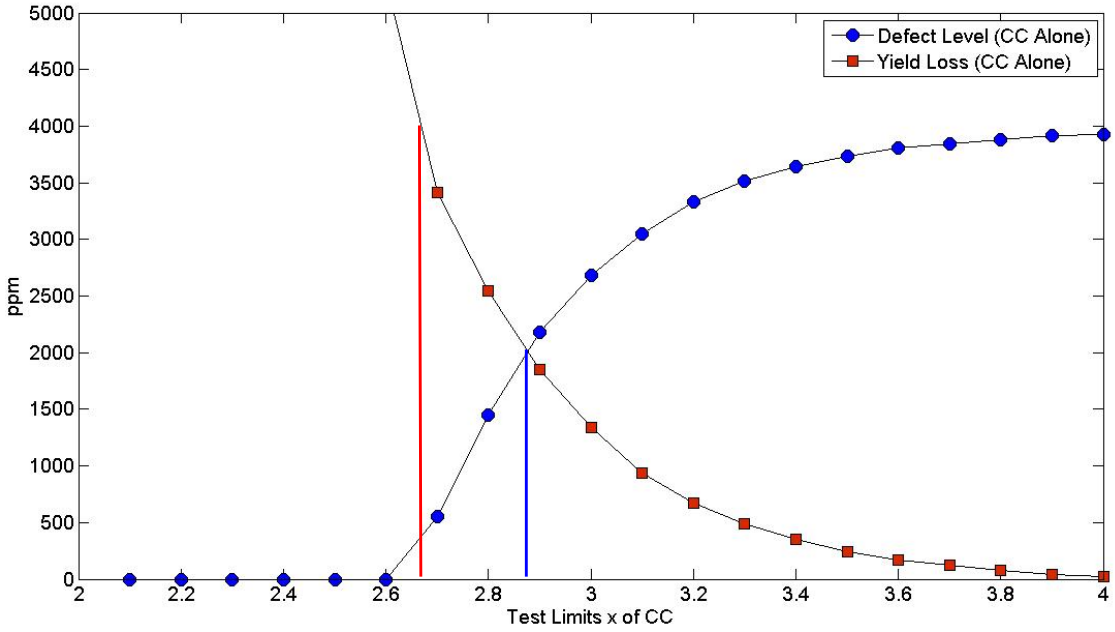


***Fig. VI-5.** Parametric defect level and yield loss of current consumption*

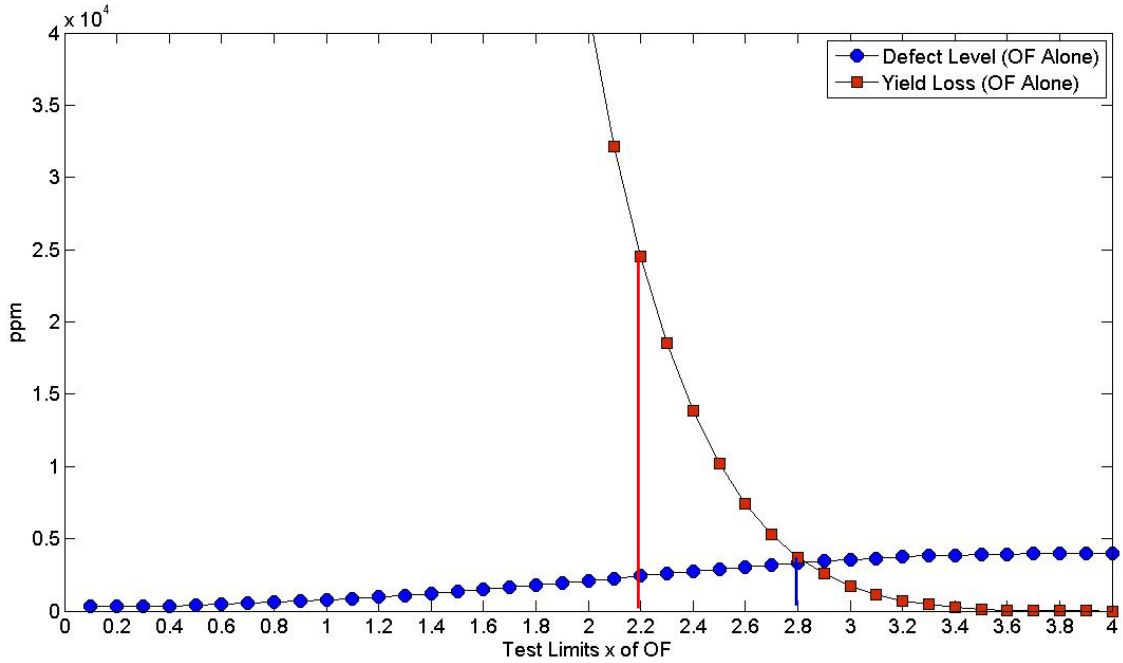


***Fig. VI-6.** Parametric defect level and yield loss of output frequency*

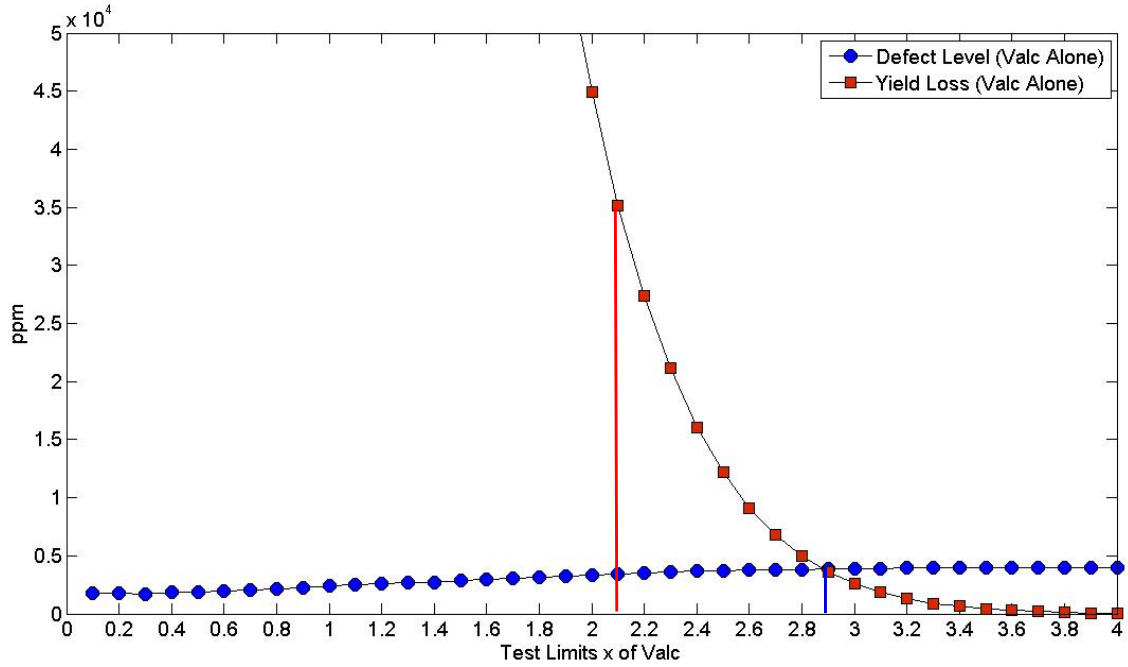


Fig. VI-7. Parametric defect level and yield loss of V_{alc} (alone)

Regardless of the exact values for each limit and the yield loss and defect level that follow, these plots show that choosing all test measures considered and setting limits on current consumption and output frequency according to specifications (x = 4.1) and setting V_{alc} limits to x = 4.75 yields the best result of yield loss equal to defect level equal to 1 ppm, with CFC = 67.6 %. Considering that for V_{alc} $\mu = 0.458$ V and $\sigma = 0.0165$ V as reported in Tab. IV-3 in section 4.3.3, the lower limit of V_{alc} is $\mu - x\sigma = 0.380$ V and the upper one is $\mu + x\sigma = 0.536$ V.

Accordingly, the choice of a set of test measures may be based not only on CFC but also considering other test metrics such as yield loss and defect level. The decision on which metric weighs the most on the choice of the golden set of test measures always depends on the aim of the market.

6.4 Catastrophic Fault Coverage Results for the CP with Embedded PFD Monitor

Due to the nature of the measurement taken by the PFD monitor, the CP needed to be simulated with all the PLL in closed-loop configuration and in lock state. For this reason the VCO block has been modeled in VerilogA hardware description language and other behavioral blocks have been introduced in the PLL schematics in order to speed up lock state in simulation as explained in section 4.4.2. Faults could thus only be injected in the CP + amplifier block (the PFD block being digital, it can be tested by simple digital techniques). The test bench used for simulation is the same one depicted in Fig. IV-11 for PLL validation.

Fig. VI-8 shows the CFC of the PFD BIST according to the tolerance set on mismatch between *UP* and *DOWN* signals. *Sum_BIST* test measure is an integer whose value is between 1 and 7, since it corresponds to the sum of the Boolean outputs of the PFD monitor flip-flops (see section 5.4). Thus, *Sum_BIST* = 1 corresponds to a mismatch tolerance of 0 ps, *Sum_BIST* = 2 corresponds to 25 ps and so on, up until *Sum_BIST* = 7 that corresponds to a mismatch tolerance of 175 ps. In the simulations, the largest window has been taken for BIST limits (from 1 to 7) for which BIST CFC is of 56.88 % of 109 faults injected in CP+amplifier. The amplifier only serves to make the design more robust, thus many faults injected in it may be transparent to operation mode in nominal conditions (but indeed they would be relevant for reliability purposes). Considering the CP alone, without amplifier, the CFC of the BIST is higher: 64.04 % of 89 faults injected. Catastrophic fault coverage for some significant combinations of performances is shown in Fig. VI-9. *Sum_BIST* and performances may not stand on the same plot since the limits are set differently, being *Sum_BIST* an integer variable.

For all performances considered (I_{up}, I_{down}, I_{out}, and V_{tune}) CFC at x = 5 is 59.6 %, Considering the CP alone, without amplifier, CFC for all performances is 67.4 %. It results that I_{out} is a completely redundant performance since it does not add any CFC in both the case of CP+amplifier and CP alone. The other performances, on the other hand, are not redundant as the plot of Fig. VI-9 reveals.

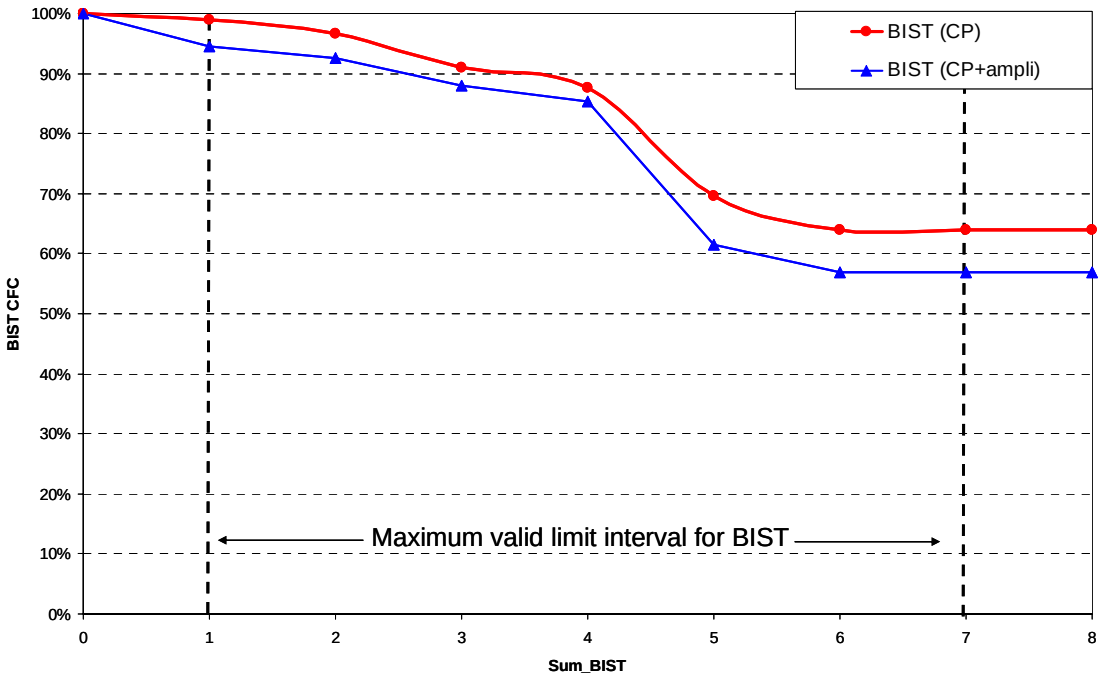


Fig. VI-8. CFC of PFD Monitor

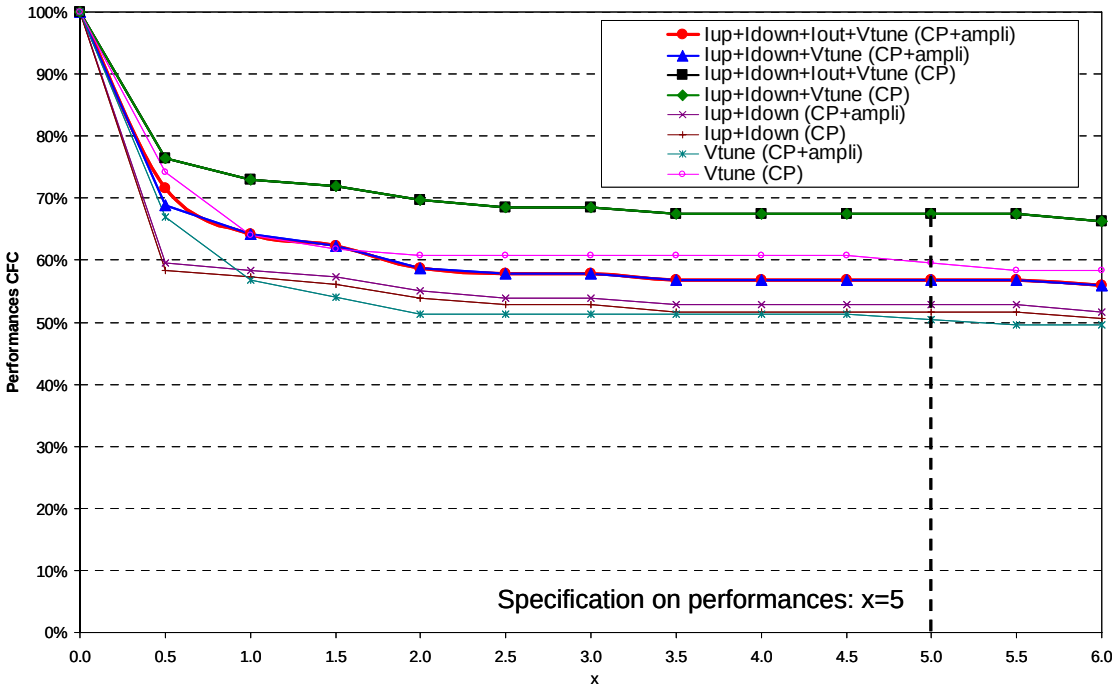


Fig. VI-9. CFC of performances for the CP

The CFC value for the BIST would be very high (between 85 % and 90 %) for Sum_BIST from 1 to 4, which corresponds to limit mismatch to 75 ps, but this will result in unacceptable values for parametric yield loss, as shown in Fig. VI-10 of the next section. The CFC for the chosen BIST limits (1 to 7 for *Sum_BIST* value as in simulations) is very close to the CFC of all the performances considered in this study (I_{up}, I_{down}, I_{out}, and V_{tune}). Actually, I_{up} and I_{down} of the CP have been added as performances to the standard I_{out} performance for two reasons. First, although I_{out} should simply be equal to $|I_{up} - I_{down}|$ it is not granted that there are no leakages (which has also been proved by the Monte-Carlo analysis discussed before). Second, and most important, the values of I_{out} are too small to build a statistical model of this performance, as has been already discussed in section 4.4.3.

6.5 Test Metrics Results and Optimized Test Limits for the PFD Monitor

Monte-Carlo simulations lasted three months approximately and only a population of 100 circuits could be generated in this lapse of time. Over these 100 circuits, 2 of them gave a NoGo output of the BIST and both of them had performance I_{out} being out of specification, the other ones being within specifications. This could mean that there is some leakage that makes the PLL less robust to process deviations and that the BIST is able to detect anyhow. Nevertheless, performance I_{out} is not taken into consideration for the statistical model for the reasons explained in section 4.4.3.

The limit on all the performances was set to 5σ, to comply with specifications using the statistical model. This generates 10205 non functional devices on the population of 1 million devices. Defect level is 5554 ppm and yield loss is 8043 ppm for limits imposed on the BIST test measure *Sum_BIST* such that the test passes if its value is in between 1 and 7. Fig. VI-10 plots defect level versus yield loss for different limits of *Sum_BIST*. As stated before, CFC for an upper limit of 4 for the BIST would be very high (85 % to 90 %), also defect level would be very low (23.13 ppm), but yield loss would be unacceptable with a value amounting to 344800 ppm.

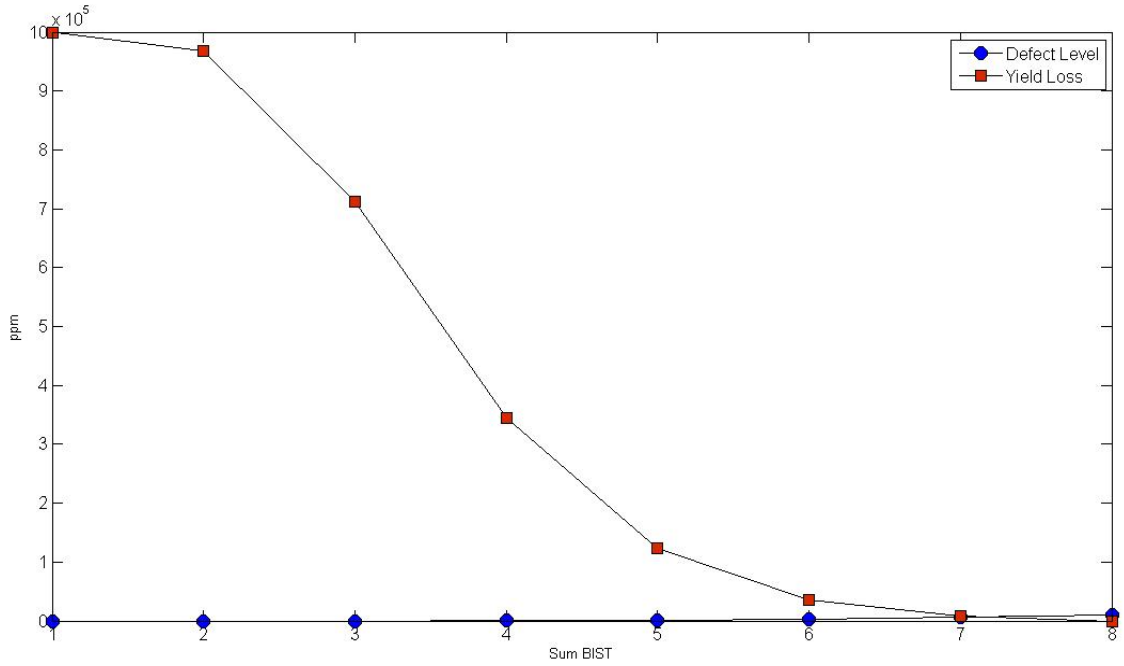


Fig. VI-10. Parametric defect level and yield loss of Sum_BIST

6.6 Conclusions

It has been demonstrated that the optimal set of test measures for the VCO is made up of all the test measures considered: current consumption, output frequency, and the peak to peak VCO output voltage V_{alc}. None of the test measures revealed to be redundant. The PFD monitor has been evaluated for the CP block.

Tab. VI-1 shows a summary that highlights test metrics for different test strategies.

Device	Metric	Specs	BIST
VCO	CFC	64 %	67.6 %
	DL	-	1 ppm
	YL	-	1 ppm
CP	CFC	67.4 %	64.04 %
	DL	-	5554 ppm
	YL	-	8043 ppm

Tab. VI-1. VCO and CP metrics for different test strategies

Although a catastrophic fault coverage between 60 % and 70 % seems quite low for a BIST strategy, it has to be taken into account that a test based on specifications has a catastrophic fault coverage which is very close to the one obtained with the proposed BIST strategy. This could be due to the fact that only one PLL configuration has been simulated to evaluate test metrics. Some of the non-detected faults in the chosen configuration may be detected by performances and/or by the BIST considering other configurations, although they activate less overall components and paths in the blocks under test. Unfortunately, simulations of the blocks under test in all the possible PLL configurations were not achievable in the timeframe at this work's disposal.

If simulations with the BIST monitors applied to whole PLL at component level were possible in all configurations of the PLL in a reasonable timeframe, this would give a more exhaustive evaluation of the BIST technique, and probably better overall results. Facing the complexity of an industrial device, the best configuration for the BIST strategy evaluation has been considered in this work.

Chapter VII

Conclusions and Future Directions

7.1 Conclusions

The aim of this work was to plan a universal BIST strategy to allow the most suitable choice of test solution for production test of AMS devices and to make them self-testable for all their lifetime. The first step was the choice of the test vehicle: a PLL has been considered since it represents one of the most complex AMS circuits to make self-testable. The choice fell on an industrial SERDES RF PLL in CMOS 65 nm technology designed at STMicroelectronics.

All the different concerns on conceiving a BIST for an RF PLL have been thought trough together with the designers. A list of performances has been drawn: phase noise, oscillation frequency, current consumption, output power, and gain. One crucial matter consisted in how to measure phase noise, which is the most important specification of this device. The conclusion that had been drawn was that phase noise is not measurable on-chip and probably soon also off-chip (on tester) for devices operating at constantly increasing frequency. It has thus been decided that it was not realistic to measure all the RF PLL performances on-chip, in particular phase noise. The procedure adopted was to define which were the performances measurable on-chip and which ones needed alternative means (test measures) to be measurable on-chip. Then again, test measures needed to be highly correlated to the performances non measurable on-chip. On-chip measurable performances were current consumption by means of a BICS, current mismatch and leakages and output frequency measurable indirectly (after division) at

the PFD output. Non measurable ones were phase noise, not completely covered by on-chip test measures but still related to mismatch in CP and measured at the PFD output, VCO gain, related to output frequency by a derivative relationship, and output power, for which built-in sensors turned out to be more area consuming than the whole PLL, and for which peak to peak voltage at the ALC output has been chosen instead.

At present, most PLLs are tested in production with a simple lock test, without verifying the degree of mismatch and leakages in currents and not considering phase noise or any correlated measure. So this particular, complex IP which is a PLL is yet far from being self-testable, due also to the complexity of studying solutions for its self-testability. Nevertheless, in this three years' work, a detailed, thorough study of the three sensors making up the BIST technique thought-out during the Ph.D. for making PLLs self-testable has been explored and validate as completely as possible considering simulation time issues.

A block per block approach has been used, first generating a statistical model for each block under test and then evaluating the fault coverage and test metrics of the test measures chosen for the VCO block and next for the CP block. Only these two blocks have been considered since they are the RF building blocks of a PLL. Sensors to be applied to the VCO are a BICS and a peak to peak voltage comparator. A PFD output monitor has been employed to test CP current mismatch (between I_{up} and I_{down}), leakages, and phase and frequency synchronization between reference frequency and feedback loop frequency.

The method employed for BIST evaluation was the method developed at TIMA Laboratory which consists in the following steps:

1) Generating a first "small" population of the DUT (1000 instances) by Monte-Carlo simulation with process deviations

2) PDF estimation of test measures and performances and generation of a larger estimated population (1 million instances) via statistical methods previously discussed

3) Evaluation of test metrics such as parametric yield loss and defect level to set limits on test measures that give the best tradeoff between the two

4) Injecting faults in the DUT and evaluating fault coverage for the chosen limits on test measures, allowing also to choose an optimized set of test measures (eliminating redundant or inefficient ones if any)

Although the procedure employed to evaluate a BIST technique is generally quite efficient and recognized by the scientific community, it resulted not as viable (with respect to industrial time constraints) applied to a real industrial IP such as the PLL used as test vehicle. The method used to evaluate the BIST is based on statistical models of the DUT, thus an original population generated through Monte-Carlo simulation is necessary, which resulted very time consuming for this case-study. Also the fault injection simulations turned out to be quite time consuming depending on how many faults are to be injected (217 in the simple SERDES PLL case-study, but there are much more complex industrial PLLs). In fact, one simulation has to be carried out for each fault injected, which amounts to 5 simulations per transistor and 3 simulations per 2-pin-passive components. Considering that the BIST evaluation has been carried out first on a Bluetooth PLL and next on the SERDES PLL, the simulations described above took more than one whole year in total, which also explains why it has not been possible to simulate the whole PLL at component level with all the three embedded sensors together. This lapse of time is not reasonable in industry for only a BIST evaluation. The conclusion is that another method, either avoiding Monte-Carlo simulations at component level to generate statistically valid populations (as stated several times already [52], [53]), or that does not rely on fault injection would be more practical for BIST evaluation on industrial complex circuits. While techniques to evaluate fault coverage without fault injections exist [54], it is still hard to imagine how to extrapolate

the statistical behavior of test measures and performances avoiding Monte-Carlo circuit simulations completely, although some very interesting work is ongoing in this field such as in [55].

In general, BIST area overhead must be as small as possible, mostly compared to the IP considered: usually a BIST area overhead must not be above 10 % to 20 % of the total IP area. Total production test time for a PLL must not be above ten or so milliseconds to be interesting under a test time reduction point of view. The technique proposed in this Ph.D. work has an area overhead of 6.54 % of the IP without BIST and allows, with a simple lock test, to test at the same time current consumption (the BICS may be applied to any block of the PLL), VCO output power (indirectly), current mismatch and leakages, output frequency, and synchronization between the reference and the feedback loop frequencies.

Results obtained for the BIST test measures give relatively low fault coverage with respect to the expected one (67.6 % for the VCO and 64.04 % for the CP). However, considering that also fault coverage yielding from performances is quite low (64 % for the VCO and 67.4 % for the CP), this shows a fault detection of the BIST technique higher or very close to the one of the performances, which means that the BIST technique may result quite valid if simulations could be carried out in all possible PLL configurations. Actually, if some faults do not impact performances, detecting them with the BIST may yield a higher yield loss (rejection of functional circuits). On the other hand, detecting faults that do not affect performances may result in a more reliable product on the market. According to the kind of product and the market it addresses, a tradeoff between yield loss and reliability must be considered; this will also affect the choice of BIST monitors for the test strategy.

Much better results would be obtainable on a non industrial, simpler PLL test vehicle, although this was not the aim of an industrial Ph.D. such as this work. The idea, in fact, was to exploit an industrial prototype to envisage fabrication, possibly in large scale. Corner lots would have indeed helped evaluating fault coverage and other test metrics

such as yield loss and defect level of the BIST technique. Unfortunately fabrication in large scale turned out to be impossible considering the timing evolution of the BIST evaluation via simulation. Also post-extract simulations have proved to be too time consuming although they would have added useful information on parasitic capacitances introduced by the BIST on the DUT (thus also on degradation of its performances).

7.2 Perspectives on RF PLL BIST

This section points out some additional work that has to be carried out on the proposed BIST technique in order to make it complete and functional.

First of all, for BIST purposes, the reference voltages V_{min} and V_{max} of the voltage window comparator should be designed to be built-in (otherwise the voltage comparator may not be properly referred to as BIST technique but it would be more appropriate to address it as DfT technique) and with the same process variations of V_{alc}. Layout should thus be completed and post-extract simulations should be carried out at least on the sensor alone to verify compliance with schematics simulations.

Second, an adequate built-in current source for I_{ref} must be chosen for the BICS reference current sources. Design of the BICS should be improved also to comply with robustness in slow worst case conditions (if such strict conditions as the ones used for industrial circuit validation have to be respected) which are now less robust than fast worst case conditions.

To complete the BIST technique, the ring oscillator method for delay calibration suggested in section 5.5.3, should be designed and applied to the PFD output monitor. Two possible calibration methods are possible according to the desired accuracy: the more precise one applied on each delay element separately, or the more approximate one applied on the whole delay line.

Some future directions may be suggested also for better completing the BIST technique evaluation. For example, it would be interesting to evaluate the effect of fault injection in the BIST monitors on overall fault coverage of the BIST technique: if the faulty BIST is able to detect itself as faulty or if there are masking effects on faults in the BIST monitors.

Actually fabricating a prototype of the DUT with the embedded monitors is not such a convincing and exhaustive procedure for BIST evaluation since one or a few prototypes will be fabricated centered in process. This would allow only verifying that the BIST gives a Go kind of output when the circuit is centered on the process and a NoGo output if one catastrophic fault per prototype (very limited number) is injected through laser based fault injection techniques, which is not an exhaustive proof for evaluating a BIST technique. It would make more sense and would be for sure more exhaustive to fabricate a whole lot of circuits with the embedded BIST monitors in order to obtain some corner lots. This would allow evaluation of the capability of the BIST to detect faulty circuits (fault coverage), the rejection rate of functional circuits (yield loss), and how many faulty circuits are not detected by the BIST (defect level). As it is understandable, expecting such thing during a Ph.D. is unfortunately a mere delusion.

This Ph.D. will hopefully open the way to building a complete universal library of BIST monitors to be embedded in analog, mixed-signal and RF devices. Different BIST monitors shall be designed for different DUT physical specifications and targets on the market. This procedure is being carried out in parallel in other Ph.D. works, thus a desirable perspective would be to gather all the BIST monitors for analog, mixed-signal and RF devices in order to give designers an exhaustive choice of BIST techniques for each specific design. The aim is to avoid adding BIST techniques after DUT design stage is over, risking alteration of DUT operation mode.

Finally, considering some alternative test measures for BIST purposes for a PLL (that might be added to this technique), some ideas came up during the Ph.D, some have been discarded, some already existed. For example all measures, such as charge pump current

I_{out}, tuning voltage V_{tune}, VCO gain, the cut-off frequency of the loop filter and others, have been considered but immediately discarded for the case-study PLL due to the necessity of probing analog sensitive nodes that would impact its operation mode. Then again, if loading these nodes is taken into account at design stage of the PLL, these test measures might also turn out to be very efficient.

Appendix 1. Very High Frequency PFD/CP Design

Avoiding False Lock

The PFD is made up of elements with finite reset time, which imposes an upper limit to the frequency it is capable of discriminating. The maximum frequency $f_{ref,max}$ for which the frequency difference between f_{ref} and f_{loop} may be discriminated is:

$$f_{ref,\max} = \frac{1}{2t_r} \tag{1-1}$$

where t_r is the reset time of the D flip-flops when the PLL is in phase-lock [56]. The phase-to-current transfer function of a PFD/CP block is shown in Fig. 1-1.

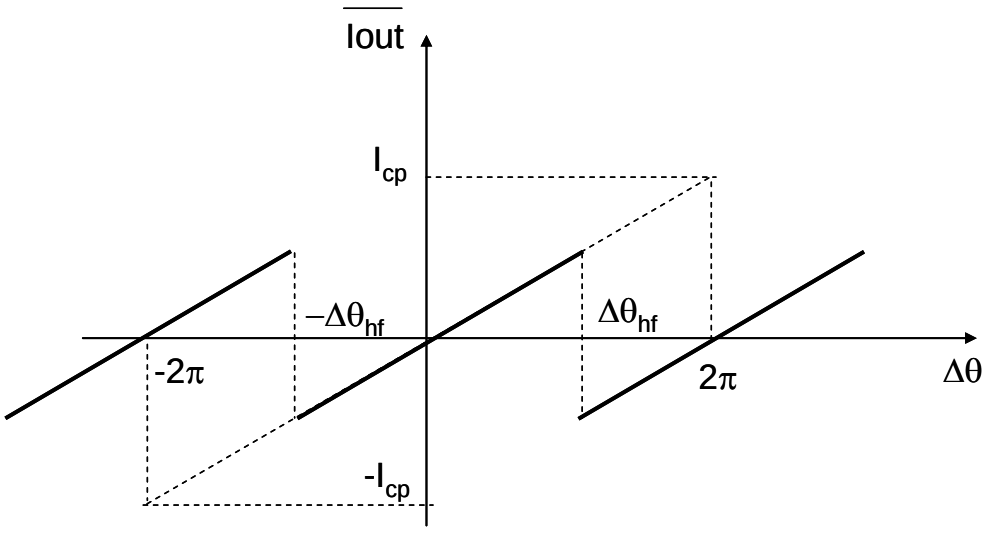


Fig. 1-1. High frequency phase-to-current transfer function of the PFD/CP block

The effect of the finite reset time is to set an upper limit to the maximum phase difference $\Delta\theta_{hf}$ which can be detected before the PFD/CP output changes polarity erroneously. $\Delta\theta_{hf}$ may be expressed as a function of the reference signal period T_{ref} as:

$$\Delta\theta_{ref} = \pm 2\pi\left(1 - \frac{t_r}{T_{ref}}\right) \overset{f_{ref,\max}=\frac{1}{T_{ref,\max}}=\frac{1}{2t_r}}{\Rightarrow} \Delta\theta_{ref,\max} = \pm 2\pi\left(1 - \frac{t_r}{2t_r}\right) = \pm\pi \qquad (1\text{-}2)$$

which means that the PFD must have a linear detection range that goes beyond ±π at the maximum operation frequency. Practice shows that failure to comply with this requirement often translates in a false-lock condition (permanent frequency lock at wrong frequencies).

Avoiding Dead-Zone Phenomenon

The dead-zone phenomenon is described in section 2.2.4, it sets an upper limit on the operation frequency of standard PFD/CP blocks. In this appendix, an architecture to avoid the problem of combining high speed operation with the presence of a dead-zone is presented.

The cause of the dead-zone is the impossibility of the slow CP switches to react to the narrow *UP* and *DOWN* signals of the PFD when the PLL is close to lock state. The usual way to eliminate the dead-zone is to increase the minimum width of the PFD signals when the phase error is close to zero. This is done by adding a fixed delay element in series with the AND gate which generates the *reset* signal to the D-flip-flops of the PFD. Another solution relies is monitoring the output of the current switches and to generate a delay in the *reset* signal until the current switches deliver current to the CP output.

Nevertheless, the operation frequency remains limited by the slow switching speed of the pnp transistors of the CP. Fig. 1-2 shows the structure of a single ended CP that presents no dead-zone phenomenon.

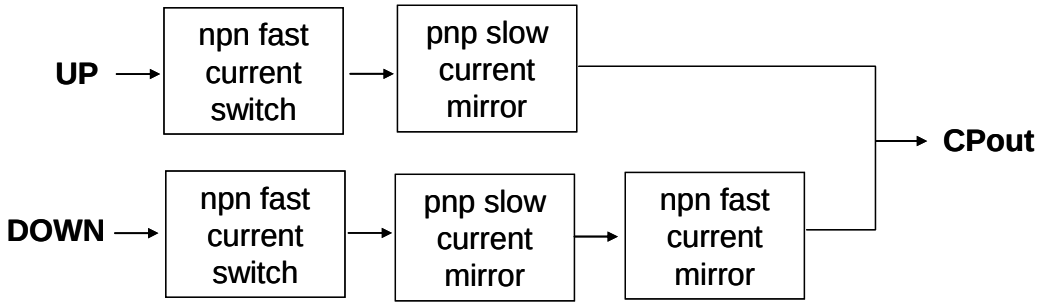


Fig. 1-2. Single Ended CP with no dead-zone

The switching part of the CP should be implemented with fast npn transistors, that are able to follow the narrow PFD signals when the PLL is close to lock state. The current switches of the CP should be followed by two high-performance matched current mirrors using slow pnp transistors. This may distort the shape of the pulses at the output of the slow current mirrors, yet it will keep the average charge intact. For a single ended CP design, an additional npn current mirror should be added in the down branch. The asymmetry introduced by this last npn current mirror is negligible due to the large difference in the cut-off frequencies of the transistors. The charges provided by the current mirror are subtracted at the CP output node before reaching the LF. As the phase error information is present on the average charge difference, this architecture presents no dead-zone.

This appendix refers to [11].

Appendix 2. Measures of Dependence

Different ways of measuring dependence between two random variables exist [49]. Classically, a relationship between two random variables is measured by the correlation factor ρ. Typical measures for dependence are Pearson's correlation factor if the relation between random variables is linear, Spearman's measure of association otherwise (Pearson's ρ and Spearman's ρ are identical for random variables having a linear relation), and the Kendall's τ.

Let us first better explain the concept of measure of dependence. Supposing that:

- at least one of the measured variables is in a semi-quantitative scale,
- interest focuses on a monotonic relation (increasing or decreasing) between quantitative variables,
- this relation is also nonlinear,
- correlation significance needs to be tested when at least one of the variables has not a Gaussian distribution,
- the number of the observations is very small,

non-parametric correlation factors, called grade correlation factors (which are the population equivalents of ranks) are needed. To define two of the most used grade correlation factors (which use a measure of dependence known as concordance), notions of concordance must be provided first.

A pair of random variables may be considered concordant if "large" values of one tend to be associated with "large" values of the other and "small" values of one with "small" values of the other. Formally, let $(x_i ; y_i)$ and $(x_j ; y_j)$ be two observations from a vector $(X ; Y)$ of continuous random variables. Observations $(x_i ; y_i)$ and $(x_j ; y_j)$ are said to be concordant if $x_i < x_j$ and $y_i < y_j$, or if $x_i > x_j$ and $y_i > y_j$ (otherwise formulated as $(x_i - x_j)(y_i - y_j) > 0$), likewise $(x_i ; y_i)$ and $(x_j ; y_j)$ are said to be discordant if $x_i < x_j$ and $y_i > y_j$, or if $x_i > x_j$ and $y_i < y_j$ (otherwise formulated as $(x_i - x_j)(y_i - y_j) < 0$) [57].

Note that the linear Pearson's correlation factor is not a concordance measure. The two main used grade correlation factors before mentioned that use concordance as measure of dependence are the Spearman's ρ and Kendall's τ.

Appendix 3. Density Estimation for a Multinormal Distribution

Given a p-dimensional vector $\boldsymbol{X} = \{X_1, X_2, ..., X_p\}^T$ composed of random variables, with average values $\boldsymbol{\mu} = \{\mu_1, \mu_2, ..., \mu_p\}^T$, the covariance of X_i and X_j is a measure of dependency between these random variables and is defined as $\nu_{XiXj} = Cov(X_i,X_j) = \mathrm{E}(X_iX_j) - \mathrm{E}(X_i)\mathrm{E}(X_j)$, where E(.) is the expected value. If X_i and X_j are independent, the covariance ν_{XiXj} is necessarily equal to zero, but not vice versa. The covariance of a random variable X_i with itself is the variance: $\nu_{XiXi} = Cov(X_i,X_i) = \nu_{Xi}$. The covariances among all the random variables $\boldsymbol{X}$ may be represented in a matrix form called variance-covariance matrix $\Sigma = \begin{bmatrix} \nu_{X1} & \cdots & \nu_{X1Xp} \\ \vdots & \ddots & \vdots \\ \nu_{XpX1} & \cdots & \nu_{Xp} \end{bmatrix}$. The correlation between two variables X_i and X_j is defined from the covariance as $\rho_{XiXj} = \dfrac{\nu_{XiXj}}{\sigma_{Xi}\sigma_{Xj}}$, where $\sigma_{Xi} = \sqrt{\nu_{Xi}}$ is the standard deviation, and the correlation matrix is defined as $\mathrm{P} = \begin{bmatrix} 1 & \cdots & \rho_{X1Xp} \\ \vdots & \ddots & \vdots \\ \rho_{XpX1} & \cdots & 1 \end{bmatrix}$. The advantage of the correlation is being independent of the scale and therefore, more useful as a measure of association between two random variables than the covariance. The correlation is used to establish the dependency of test measures from performances [10].

In order evaluate the PDF of $\boldsymbol{X}$ a number of observations of this vector is required. Let $\{\boldsymbol{x}_1, \boldsymbol{x}_2, ..., \boldsymbol{x}_k, ..., \boldsymbol{x}_n\}$ be a set on n observations of $\boldsymbol{X}$. Visibly each $\boldsymbol{x}_k$ is a p-dimensional vector as $\boldsymbol{X}$: $\boldsymbol{x}_k = \{x_{k1}, x_{k2}, ..., x_{ki}, ..., x_{kp}\}^T$ and corresponds to an observed value of $\boldsymbol{X}$. Let

$\bar{\mathbf{x}} = \{\bar{x}_1,...,\bar{x}_i,...,\bar{x}_p\}^T$ be the p-dimensional vector of the estimated average values evaluated as $\bar{x}_i = \frac{1}{n}\sum_{k=1}^{n} x_{ki}$, the estimated covariance is $V_{XiXj} = \frac{1}{n\text{-}1}\left(\sum_{k=1}^{n} x_{ki}x_{kj} - n\bar{x}_i \cdot \bar{x}_j\right)$, the estimated variance is $V_{Xi} = \frac{1}{n\text{-}1}\left(\sum_{k=1}^{n} x_{ki}^2 - n\bar{x}_i^2\right)$, and thus the estimated correlation is $r_{XiXj} = \frac{V_{XiXj}}{s_{Xi}s_{Xj}}$, were $s_{Xi} = \sqrt{V_{Xi}}$ is the estimated standard deviation. The estimated variance-covariance matrix is $S = \begin{bmatrix} V_{X1} & \cdots & V_{X1Xp} \\ \vdots & \ddots & \vdots \\ V_{XpX1} & \cdots & V_{Xp} \end{bmatrix}$ and the estimated correlation matrix is $R = \begin{bmatrix} 1 & \cdots & r_{X1Xp} \\ \vdots & \ddots & \vdots \\ r_{XpX1} & \cdots & 1 \end{bmatrix}$. The PDF of the vector ***X*** is thus defined as: $f(\mathbf{x}) = \frac{1}{\sqrt{(2\pi)^n |S|}} e^{-\frac{1}{2}(\mathbf{x}-\bar{\mathbf{x}})^T S^{-1}(\mathbf{x}-\bar{\mathbf{x}})}$.

Appendix 4. Starter and VCO Behavioral Models

Starter Block: VerilogA Behavioral Model

```
// VerilogA for verilogA, starter, veriloga

`include "constants.vams"
`include "disciplines.vams"

`define PI      3.14159265358979323846264338327950288419716939937511

module starter(floop, EN, INIT, fref, fref_n);

input floop;
output fref, EN, INIT, fref_n;

electrical floop, fref, fref_n, temp, EN, INIT;

parameter real ref_freq = 1K;
parameter real amp = 1;
parameter real offset = 1;

   real phase, reftime, EN_var, INIT_var, temp_var, state_ref,
state_ref_n;
   integer n, m, num_cycles;

   analog begin

    @ (initial_step) begin
        n = 0;
        m = 0;
        reftime = 0;
        EN_var = 0;
        INIT_var = 0;
    end

    @(cross(V(floop)-offset,+1)) begin
        m=m+1;
    end

    if (m==0) begin
        temp_var = 0;
    end

    if (m>=1)begin
        INIT_var = 2*amp;
```

```
        temp_var = 2*amp;
    end

    @(cross(V(floop)-offset,-1)) begin
        n=n+1;
    end

    if (n==0) begin
        reftime=$abstime;
    end

    if (n>=1) begin
        EN_var = 2*amp;
        phase = 2 * `PI * ref_freq * ($abstime-reftime);
        num_cycles = phase / (2*`PI);
        phase = phase - num_cycles * 2*`PI;
        temp_var = -amp * sin(phase);
    end

    if (temp_var>0) begin
        state_ref = 1;
        state_ref_n = 0;
    end

    if (temp_var<=0) begin
        state_ref = 0;
        state_ref_n = 1;
    end

    V(fref) <+ transition (state_ref*2*amp, 0, 10p, 10p);
    V(fref_n) <+ transition (state_ref_n*2*amp, 0, 10p, 10p);
    V(EN) <+ EN_var;
    V(INIT) <+ INIT_var;
   end

endmodule
```

VCO Block: VerilogA Behavioral Model

```
// VerilogA for verilogA, vco_div, veriloga
`include "discipline.h"
`include "constants.h"


// Based on the OVI Verilog-A Language Reference Manual, version 1.0
1996
//
//

`define PI      3.14159265358979323846264338327950288419716939937511

//--------------------
// vco_div
```

```
//
// -  voltage-controlled oscillator + divider by N
//
// vin:     ocillation controlling voltage [V,A]
// vtyp:    typical value of vtune voltage [V,A]
// vout:    output oscillation [V,A]
// voutdiv: vout/div [V,A]
// voutdivm:    vout/div inverted [V,A]
//
// INSTANCE parameters
//    amp           = amplitude of the output signal divided by 2 [V]
//    center_freq   = frequency of oscillation when 'vin' = 'vtyp'
[Hz]
//    vco_gain      = oscillator conversion gain [Hz/volt]
//
// MODEL parameters
//    {none}
//

module vco_div(vtyp, vin, vout,voutdiv, voutdivm);

input vin , vtyp;
output vout, voutdiv, voutdivm;

electrical vin, vtyp, vout, temp, voutdiv, voutdivm;

parameter real amp = 0.6;
parameter real offset = 0.6;
parameter real center_freq = 1K;
parameter real vco_gain = 1K;
parameter real ampdiv = 0.6;
parameter real offsetdiv = 0.6;
parameter real div = 1884.0;

   real center_pulse;       // center freq in rad/s

   real phase_lin;      // center_pulse*time component of phase
   real phase_nonlin;       // the idt(k*f(t)) of phase

   integer num_cycles;      // number of cycles in linear phase
component

   real inst_freq;      // instanteous frequency
   real trans, transm;

   real phase_lin_div;      // center_pulse*time component of phase
   real phase_nonlin_div;   // the idt(k*f(t)) of phase

   integer num_cycles_div;  // number of cycles in linear phase
component



   analog begin
```

```
      @ ( initial_step ) begin
          center_pulse = 2 * `PI * center_freq;
      end

      //
      // linear portion is calculated so that it remains in the +/-
2`PI range
      // This is to ensure it's value doesn't get too large and cause
rounding
      // problems for calculation of the phase.
      //
      phase_lin = center_pulse * $abstime;
      num_cycles = phase_lin / (2*`PI);
      phase_lin = phase_lin - num_cycles * 2 * `PI;

      phase_nonlin = 2 * `PI * vco_gain * idt ((V(vin)-V(vtyp)),0);

      V(vout) <+ amp * sin (phase_lin + phase_nonlin)+offset;

      //
      // ensure that modulator output recalculated soon.
      //
      inst_freq = center_freq + vco_gain * (V(vin)-V(vtyp));
      $bound_step (0.2/ inst_freq);

      phase_lin_div = center_pulse * $abstime / div;
      num_cycles_div = phase_lin_div / (2*`PI);
      phase_lin_div = phase_lin_div - num_cycles_div * 2 * `PI;
      phase_nonlin_div = phase_nonlin / div;

      V(temp) <+ ampdiv*sin(phase_lin_div + phase_nonlin_div) +
offsetdiv;

      @(cross((V(temp)-offsetdiv), +1)) begin
              trans = 1;
              transm = 0;
      end
      @(cross((V(temp)-offsetdiv),-1)) begin
              trans = 0;
              transm = 1;
      end

      V(voutdiv) <+ transition (2*amp*trans,0,10p,10p);
      V(voutdivm) <+ transition (2*amp*transm,0,10p,10p);
   end


endmodule
```

In this behavioral model, the center frequency f_c obtained as output oscillation frequency for typical value of $V_{tune} = 0.8$ V, is used as parameter instead of the free

running frequency f_0 obtained for $V_{tune} = 0$ V. However, no matter what value may be given in input for '*vtyp*' as long as the corresponding frequency of oscillation for $V_{tune} = vtyp$ is given as input parameter *center_freq*. In this case though, the terminology looses its exact meaning. In other words, one could choose, for example, *vtyp* = 1.25 V instead of 0.8 V providing to give the value of the oscillation frequency for $V_{tune} = 1.25$ V to the parameter *center_freq*. The behavioral model would work in any case. The essential is to give as parameters one operating point of the VCO and its gain at the wanted conditions.

Appendix 5. Metastability

The output of an edge-triggered flip-flop has two valid states: high and low. To ensure reliable operation, designs must meet some timing requirements. Otherwise the result is that the output may behave unpredictably, oscillating several times before settling. Theoretically it can take infinite time to settle down. Clocked flip-flops are in fact prone to a problem called metastability, which happens when the input is changing at the instant of the clock pulse.

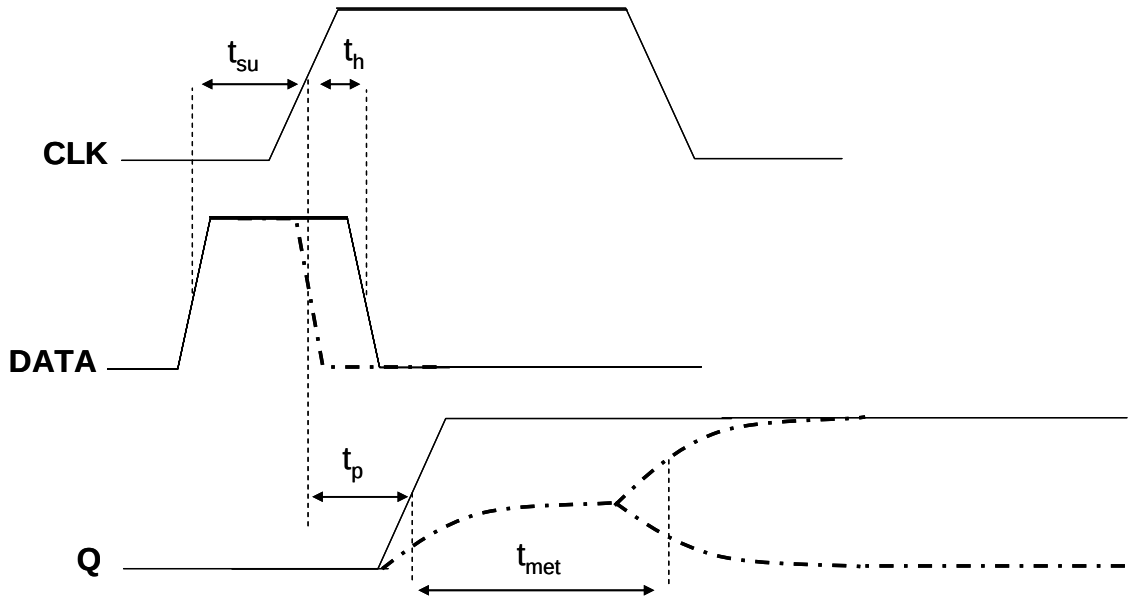


Fig. 5-1. Flip-flop setup, hold, and propagation time

The input should remain stable for specified periods before and after the clock pulse, called the setup time t_{su} and the hold time t_h respectively, shown in Fig. 5-1. A change in the input in this time interval will yield a probability of setting the flip-flop to a metastable state. The clock-to-output delay or propagation delay t_p is the time the flip-flop takes to change its output after the clock edge. The time for a high-to-low transition

t_{phl} is sometimes different from the time for a low-to-high transition t_{plh}. The additional time beyond t_p that a metastable output takes to resolve to a stable state is called the settling time t_{met}.

One technique for reducing metastability is to connect two or more flip-flops in a chain, so that the output of each one feeds the data input of the next, and all devices share a common clock. When connecting flip-flops in a chain, it is important to ensure that the t_p of the first flip-flop is longer than the hold time t_h of the second flip-flop, otherwise the second flip-flop will not receive the data reliably. The relationship between t_p and t_h is normally guaranteed if both flip-flops are of the same type. This structure is commonly known as multiple-stage synchronizer. If the synchronizing flip-flop produces a metastable output, the metastable signal may resolve before it is clocked by the second flip-flop. This method does not guarantee that the second flip-flop will not clock an undefined value, but it dramatically increases the probability that the data will go to a valid state before it reaches the rest of the circuit. With this method, the probability of a metastable event can be reduced to a negligible value, but never to zero. The probability of metastability gets closer and closer to zero as the number of flip-flops connected in series is increased.

Metastability cannot be eliminated entirely, though. This is because when the transitions in the clock and the data are close together in time, the flip-flop is forced to decide which event happened first. However fast the device can be, there is always the possibility that the input events will be so close together that it cannot detect which one happened first. It is therefore logically impossible to build a perfectly metastable-proof flip-flop.

This appendix refers to [22], [23], [24].

References

[1] S. Sunter and A. Roy, *Purely Digital BIST for any PLL or DLL*. 12th European Test Symposium, May 2007, pp. 185-192.

[2] L.S. Milor, *A Tutorial Introduction to Research on Analog and Mixed-Signal Circuit Testing.* IEEE Transactions on Circuit and Systems II: Analog and Digital Signal Processing, vol. 45, issue 10, October 1998, pp. 1389-1407.

[3] L. Anghel, *Test et Conception en Vue du Test de Circuits Intégrés,* Cours à l'INP Grenoble, 2006.

[4] A. Bounceur, *Plateforme CAO pour le test de circuits mixtes*. Ph.D thesis, INP Grenoble, April 2007.

[5] S. Sunter and N. Nagi, *Test Metrics for Analog Parametric Faults.* 17th VLSI Test Symposium, April 1999, pp. 226–234.

[6] H. Stratigopoulos, S. Mir, and A. Bounceur, *Evaluation of analog/RF test measurements at the design stage.* IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 28, issue 4, April 2009, pp. 582-590.

[7] B. Kaminska and K. Arabi, *Mixed Signal DFT: A Concise Overview*. International Conference on Computer Aided Design, San Jose, California, USA, November 2003, pp. 672-679.

[8] S. Sunter and A. Roy, *BIST for Phase-Locked Loops in Digital Applications.* International Test Conference, Proceedings 28-30, September 1999, pp. 532-540.

[9] A. Bounceur, S. Mir, E. Simeu and L. Rolíndez, *On the accurate estimation of test metrics for multiple analogue parametric deviations.* 12th International Mixed-Signals Testing Workshop, Edinburgh, UK, June 2006, pp. 19-26.

[10] A. Bounceur, S. Mir, L. Rolíndez and E. Simeu, *CAT platform for analogue and mixed-signal test evaluation and optimization*. Chapter in VLSI-SoC: Research trends in VLSI and Systems on Chip. G. De Micheli, S. Mir, R. Reis (Eds.), Springer, 2007, pp. 281-300.

[11] C. Vaucher, *Architectures for RF Frequency Synthesizers*. Kluwer Academic Publishers, Boston, 2002.

[12] B. Razavi, *Design of Analog CMOS Integrated Circuits*. McGraw-Hill, 2001.

[13] D. H. Wolaver, *Phase-Locked Loop Circuit Design*. Penitence Hall, 1991.

[14] D. A. Johns and K. Martin, *Analog Integrated Circuits and Systems*. Ch 16 Phase-Locked Loops. John Wiley & Sons, 1997.

[15] J. Craninckx and M. Steyaert, *Wireless CMOS Frequency Synthesizer Design*. Kluwer Academic Publishers, Boston, 1998.

[16] A. Bounceur, S. Mir, E. Simeu, and L. Rolíndez. *Estimation of test metrics for the optimisation of analogue circuit testing.* Journal of Electronic Testing: Theory and Applications, Springer Science+Business Media, vol. 23, issue 6, December 2007, pp. 471-484.

[17] J.L. Huang, *On-Chip Random Jitter Testing Using Low Tap-Count Coarse Delay Lines.* Journal of Electronic Testing, Springer, vol. 22, issue 4-6, December 2006, pp. 387-398.

[18] J.J. Huang and J.L. Huang, *A Low-Cost Jitter Measurement Technique for BIST Applications.* 12th Asian Test Symposium, November 2003, pp. 336-339.

[19] M. Steyaert, B. Razavi, I, Galton, G. Gielen, R. Blauschild, L. Devito, and A. Hajimiri, Electronics Laboratories, *Advanced Course on PLLs and Clock Recovery*. Lausanne, Switzerland, July 2006.

[20] J.L. Huang, K.T. Cheng, *An On-Chip Short-Time Interval Measurement Technique for Testing High-Speed Communication Links*. VLSI Test Symposium, January 2001, pp. 380-385.

[21] S. Sunter, A. Roy, J-F. Côté, *An Automated, Complete, Structural Test Solution for SERDES*. International Test Conference, October 2004, pp. 95-104.

[22] ALTERA, *Metastability in ALTERA Devices*. Version 4, application note 42, May 1999.

[23] D. Grosse, *Keeping Metastability from Killing Your Design*. Electronics Design, Strategy, News Access, June 1994, pp. 1-7.

[24] J. Horstmann, H. Eichel, and R. Coates, *Metastability Behavior of CMOS ASIC Flip-Flops in Theory and Test*. Journal of Solid State Circuits, vol. 24, issue 1, February 1989, pp. 146-157.

[25] K.A. Jenkins, A.P. Jose, and D.F. Heidel, *An On-chip Jitter Measurement Circuit with Sub-picosecond Resolution*. 31st European Solid State Circuit Conference, September 2005, pp. 157-160.

[26] M.J. Burbidge, V. Vaid, J. Tijou, and A. Richardson, *Investigation Of Automatic Built In Transient Step Response Monitoring For Embedded Second Order Charge Pump Phase Locked Loop Frequency Synthesizers.* 8th International Mixed-Signal Test Workshop (IMSTW), Montreux, Switzerland, 2002.

[27] B.R. Veillette and G.W. Roberts, *On-Chip Measurement of the Jitter Transfer Function of Charge-Pump Phase-Locked Loops.* Journal of Solid-State Circuits, vol. 33, issue 3, March 1998, pp. 483-491.

[28] J. S. Sunter, and A. Roy, *On-Chip Digital Jitter Measurements, from Megahertz to Gigahertz.* Design & Test of Computers, vol. 21, issue 4, August 2004, pp. 314-321.

[29] P. Dudek, S. Szczepanski, J.V. Hatfield, *A High-Resolution CMOS Time-to Digital Converter Utilizing a Vernier Delay Line.* IEEE Transactions on Solid-State Circuits, vol. 35, issue 2, February 2000, pp. 240-247.

[30] A.H. Chan, G. Roberts, *A Synthesizable, Fast and High Resolution Timing Measurement Device Using a Component Invariant Vernier Delay Line*. International Test Conference, Baltimore, MD, USA, November 2001, pp. 858-867.

[31] S. Sattler, D. Oberle, and J. Eckmueller, *PLL Built-In Self-Test Jitter Measurement Integration into 0.18u CMOS Technology*. Test methods and Reliability of Circuits and Systems Workshop, 2001.

[32] J. Rivoir, *Fully-Digital Time-To-Digital Converter for ATE with Autonomous Calibration*. International Test Conference, October 2006, pp. 1-10.

[33] M. Sachdev and J. Pineda de Gyvez, *Defect-oriented Testing for nano-Metric CMOS VLSI Circuits*. 2nd Edition, Springer, 2007, pp. 32-45.

[34] S. Kim, M. Soma, and D. Risbud, *An Effective Defect-Oriented BIST Architecture for High-Speed Phase-Locked Loops*. 18th VLSI Test Symposium, May 2000, pp. 231-236.

[35] M.J. Burbidge, *Towards generic charge-pump phase-locked loop, jitter estimation techniques using indirect on chip methods*. The VLSI Integration Journal, Systems-on-Chip: Design and Test, Elsevier, vol. 40, issue 2, February 2007, pp. 133-148.

[36] F. Azaïs, Y. Bertrand, M. Renovell, A. Ivanov, and S. Tabatabaei, *An All-Digital DFT Scheme for Testing Catastrophic Faults in PLLs. Testing Phase-Locked Loops*. Design and Test of Computers, vol. 20, issue 1, February 2003, pp. 60-67.

[37] A. Asquini, A. Bounceur, S. Mir, F. Badets, J. L. Carbonero, and L. Bouzaida, *DfT Technique for RF PLLs Using Built-In Monitors*. Design and Technology of Integrated Systems, Cairo, Egypt, April 2009, pp. 210-215.

[38] L. Testa, H. Lapuyade, Y. Deval, O. Mazouffre, J. L. Carbonero, J. B. Begueret, *BIST Scheme for RF VCOs Allowing the Self-Correction of the CUT*. International Test Conference, November 2009.

[39] M. J. Burbidge, J. Tijou, A. Richardson, *Techniques for Automatic On Chip Closed Loop Transfer Function Monitoring For Embedded Charge Pump Phase Locked Loops.* Design, Automation and Test in Europe, Munich, Germany, vol 1., March 2003, pp. 10496-10502.

[40] M. Dalmia, A. Ivanov, and S. Tabatabaei, *Power Supply Current Monitoring Techniques for Testing PLLs.* Asian Test Symposium, Akita, Japan, November 1997, pp. 366-371.

[41] A. Gopalan, M. Margala, and P.R. Mukund, *A current self-test methodology for RF front-end circuits.* Microelectronics Journal n°36, Elsevier, 2005, pp. 1091-1102.

[42] M. Cimino, H. Lapuyade, M. De Matos, T. Taris, Y. Deval, and J.B. Brequeret, *A Sub 1V CMOS LNA dedicated to 802.11b/g applications with self-test & high*

reliability capabilities. Radio Frequency Integrated Circuits Symposium, June 2007, pp. 343-346.

[43] T. Finateu, *A Direct Digital RF Transmitter Based on Phase-Interpolar Direct Digital Synthesizer and Injection Locking*. Ph.D. thesis, Université Bordeaux 1, November 2008.

[44] K.R. Laker and W. M. Sansen, *Design of Analog Integrated Circuits and Systems*. McGraw-Hill, 1994.

[45] P.E. Allen, *CMOS Analog Circuit Design*. Oxford University Press, 2004.

[46] J. Galiay, Y. Crouzet, and M. Verginault, *Physical Versus Logical Fault Models MOS LSI Circuits: Impact on Their Testability.* IEEE Transactions on Computers, vol. C-29, issue 6, June 1980, pp. 527-531.

[47] A. Asquini, J.L. Carbonero, and S.Mir, *Test Measurements Evaluation for VCO and Charge Pump Blocks in RF PLLs.* SPIE International Symposium on Microtechnologies for the New Millennium, VLSI Circuits and Systems Conference, Gran Canaria, Spain, May 2007, vol. 6590, pp. 1A.1-1A.8.

[48] J. Tongbong, A. Bounceur, S. Mir, and J.L. Carbonero. *Evaluation of Test Measures for Low-Cost LNA Production Testing*. 14th International Conference on Very Large Integration, Ph.D. forum, Nice, France, October 2006, pp. 48-52.

[49] A. Bounceur, S. Mir. *Estimation of Test Metrics for AMS/RF BIST Using Copulas*. 14th International Mixed-Signals, Sensors, and Systems Test Workshop (IMS3TW), Vancouver, Canada, June 2008.

[50] A. Asquini, F. Badets, S.Mir, J.L. Carbonero, L. Bouzaida, *PFD Output Monitoring for RF PLL BIST*. 14th International Mixed-Signals, Sensors, and Systems Test Workshop (IMS3TW), Vancouver, Canada, June 2008.

[51] C. Wegener and P. Kennedy, *Test Development Through Defect and Test Escape Level Estimation for Data Converters*. Journal of Electronic Testing: Theory and Applications, vol. 22, issue 4-6, December 2006, pp. 313-324.

[52] N. Ben-Hamida, K. Saab, D. Marche, and B. Kaminska, *FaultMaxx: A Perturbation Based Fault Modeling and Simulation for Mixed-Signal Circuits*. 6th Asian Test Symposium, November 1997, pp. 182-187.

[53] K. Saab, N. Ben-Hamida, and B. Kaminska, *Parametric Fault Simulation and Test Vector Genration*. Design, Automation and Test in Europe Conference and Exhibition, Paris, France, March 2000, pp. 650-656.

[54] Y. Joannon, *Qualification et génération automatique de stimuli pour le test de systèmes sur puces (SoC) analogiques mixtes et RF*. Ph.D. thesis, INP Grenoble April 2008.

[55] M. Dubois, H.-G. Stratigopoulos, and S. Mir, *Hierarchical parametric test metrics estimation: A ΣΔ converter BIST case-study*. 27th International Conference on Computer Design, Lake Tahoe, USA, October 2009, pp. 78-83.

[56] M. Soyuer and R. G. Meyer, *Frequency Limitations of a Conventional Phase-Frequency Detector*. Journal of Solid-State Circuits, vol. 25, issue 4, August 1990, pp. 1019-1022.

[57] R.B. Nelsen, *An Introduction to Copulas*. Springer, 2006.

Author's Publications

A. Asquini, A. Bounceur, S. Mir, F. Badets, J. L. Carbonero, and L. Bouzaida, *DfT Technique for RF PLLs Using Built-In Monitors*. Design and Technology of Integrated Systems (DTIS), Cairo, Egypt, April 2009, pp. 210-215.

A. Asquini, F. Badets, S.Mir, J.L. Carbonero, L. Bouzaida, *PFD Output Monitoring for RF PLL BIST*. 14th International Mixed-Signals, Sensors, and Systems Test Workshop (IMS3TW), Vancouver, Canada, June 2008.

A. Asquini, J.L. Carbonero, and S.Mir, *Test Measurements Evaluation for VCO and Charge Pump Blocks in RF PLLs.* SPIE International Symposium on Microtechnologies for the New Millennium, VLSI Circuits and Systems Conference, Gran Canaria, Spain, May 2007, vol. 6590, pp. 1A.1-1A.8.

Résumé en Français

Technique de BIST pour synthétiseurs de fréquence RF

1. Sommaire

Les mesures de test sur puce pour la nouvelle génération des circuits analogiques et mixtes RF remplacera performances qui deviennent trop coûteux, voire impossible, à mesurer sur puce et/ou sur testeur. D'une part, ces mesures sur puce ne doivent pas dégrader les performances du circuit sous test pendant le mode de fonctionnement. D'autre part, ils doivent être en stricte corrélation avec les performances du circuit. Elles devraient contribuer à réduire les temps de test et les ressources pour le test de production tout en maintenant la qualité standard. Pour les boucles à verrouillage de phase en radiofréquences, la mesure de performances tels que le bruit de phase, par exemple, devient impossible avec l'augmentation des fréquences. Ce travail présente une technique de design en vue du test pour boucles à verrouillage de phase en radiofréquences (RF) aide de trois moniteurs embarqués qui prennent des mesures fortement corrélées avec les performances des dispositifs. Un simple test de verrouillage sur un testeur numérique faible coût suffit. Les moniteurs embarqués sont destinés à donner un type de sortie numérique (Go/No-Go). Une évaluation de la couverture de fautes catastrophiques de la technique de test est effectuée sur le bloc VCO par simulation de défauts. La perte de rendement paramétrique et le niveau de défaut paramétrique sont évalués en utilisant un modèle statistique du VCO obtenu par une technique d'estimation de densité de probabilité basé sur la théorie des copules. Le cas

d’étude est une boucle à verrouillage de phase RF CMOS 65 nm conçue et fabriquée chez STMicroelectronics.

2. Introduction

Le spectre de puissance à la sortie d'une boucle à verrouillage de phase RF contient, en plus du signal de la porteuse, des signaux parasites qui dégradent les performances du système. Ces signaux proviennent essentiellement de deux sources différentes : le couplage des signaux à la sortie de la boucle à verrouillage de phase et la modulation de l'oscillateur local par des signaux en bande de base déterministes. Les signaux RF « spurious » produisent : a) une modulation de phase, habituellement en raison de fuites et du « mismatch » du courant ; b) modulation d'amplitude qui est principalement évitée par l'utilisation d'un contrôleur automatique de niveau (ALC) dans le VCO (le contrôleur de niveau, ou de swing, est un détecteur d’enveloppe suivie par un amplificateur habituellement présent dans les VCO de nouvelle génération afin de minimiser les variations d’amplitude avec les déviations du procédé ; c) bandes latérales « spurious » non déterministes du bruit de phase [11]. Alors que a) et b) peuvent être aussi appelés « jitter » déterministe dans le domaine temporel, c) est également connu comme « jitter » non déterministe.

Malheureusement, bien que le « jitter » est la performance la plus importante d'une boucle à verrouillage de phase, la mesure directe de la somme de toutes les composantes de « jitter » à la sortie du VCO est de plus impossible dans le domaine RF depuis que l'intervalle de temps à mesurer est de l'ordre de la picoseconde ou sub-picoseconde. La technique de test présenté dans ce travail vise à : a) mesurer les sources les plus importantes du « jitter » déterministe, comme le « mismatch » et les fuites, qui ne peuvent être évité par la conception (par exemple en utilisant le ALC dans le VCO) et b) mesurer des signaux du VCO, car il contribue la partie la plus pertinente du « jitter » non déterministe (bruit de phase). Les mesures du VCO sont censées être en stricte corrélation avec le bruit de phase qui est une performance non mesurable.

3. Etat de l'art

Beaucoup d'efforts ont été fait jusqu'à maintenant pour trouver la façon la plus précise d'évaluation du « jitter » des boucles à verrouillage de phase qui montent toujours plus en fréquence. Sunter et Roy ont mis au point plusieurs ouvrages à ce sujet, la plus récente étant la technique ULTRA. Grâce à la technique de sous échantillonnage déjà proposée par Huang dans [20], cette technique par LogicVision est capable d'évaluer le « jitter » avec une résolution sub-picoseconde [1]. Néanmoins, cette technique nécessite une référence propre, afin de générer une fréquence proche, mais pas égale à la fréquence de sortie de la boucle à verrouillage de phase. Précédents techniques intéressantes ont été basées sur le déphasage de la fréquence de sortie avec des lignes de retard, l'échantillonnage avec une bascule D et comptant les fois que le front d'horloge est en avance/retard du front de la fréquence [8][25]. Avec le même principe, mais avec une résolution plus fine, il existe des techniques basées sur l'utilisation de lignes à retard de Vernier [29][30] ou oscillateurs en anneau de Vernier [31]. Les techniques basées sur les éléments de retard nécessitent d'un calibrage très précis, car les éléments de retard sont très sensibles aux écarts dans le procédé [30][32][33]. Certaines autres techniques pour le test des boucles à verrouillage de phase ne fournissent pas des mesures de « jitter » et reposent principalement sur l'ouverture de la boucle et l'injection de vecteurs de test, en observant le comportement en boucle ouverte [34][36]. Ces techniques ont l'avantage d'être entièrement numérique et le désavantage de ne pas considérer le « jitter » du tout.

4. Technique de test

La technique de test proposé ici est composé de trois moniteurs embarqués, dont deux sont appliqués au VCO et un à la sortie du PDF, comme le montre la Figure 1. La sortie d'une chaîne de scan (ou d'autres moniteurs embarqués numériques) utilisée pour tester les blocs numériques peut être ajoutée à l'ensemble des signaux de sortie. Une attention particulière a été accordée afin d'éviter le sondage des nœuds analogiques sensibles. En fait, le sondage nœuds analogiques sensibles tels que CP, LPF et les sorties du VCO

peuvent influer sur le fonctionnement global de la boucle à verrouillage de phase [35]. Nous avons choisi deux capteurs pour le bloc VCO seul car il est la principale source de bruit de phase dans une boucle à verrouillage de phase et aussi parce c'est dans le VCO que la plupart des causes de dysfonctionnement peuvent se produire. Le capteur à la sortie du PFD sondera les signaux de sortie UP et DOWN du PFD pour mesurer leur « mismatch ». Le but n'est pas de mesurer e « jitter » directement à la sortie du VCO, car cela devient impossible. Par simulation, nous avons étudié le degré de corrélation entre les mesures de test choisies et les performances des dispositifs. Pour le VCO, les performances considérées sont le bruit de phase, la fréquence de sortie à des valeurs différentes de la tension de réglage à l'entrée du VCO V_{tune} (mesure liée à gain du VCO) et de la consommation de courant. Les mesures de test réelles du VCO faciles à obtenir sur puce comprennent la tension crête à crête en sortie V_{alc} (strictement liée à la puissance de sortie VCO), la consommation de courant, et la fréquence de sortie à la valeur nominale de Vtune. En outre, en mesurant aussi la différence de rapport cyclique des signaux en sortie du PFD, nous obtenons des renseignements liés à des performances tels que le « mismatch », le courant de fuite, la synchronisation entre la fréquence de référence et la fréquence de bouclage (lié à la fréquence de sortie), certaines composantes de bruit de phase, le temps et l'état de verrouillage.

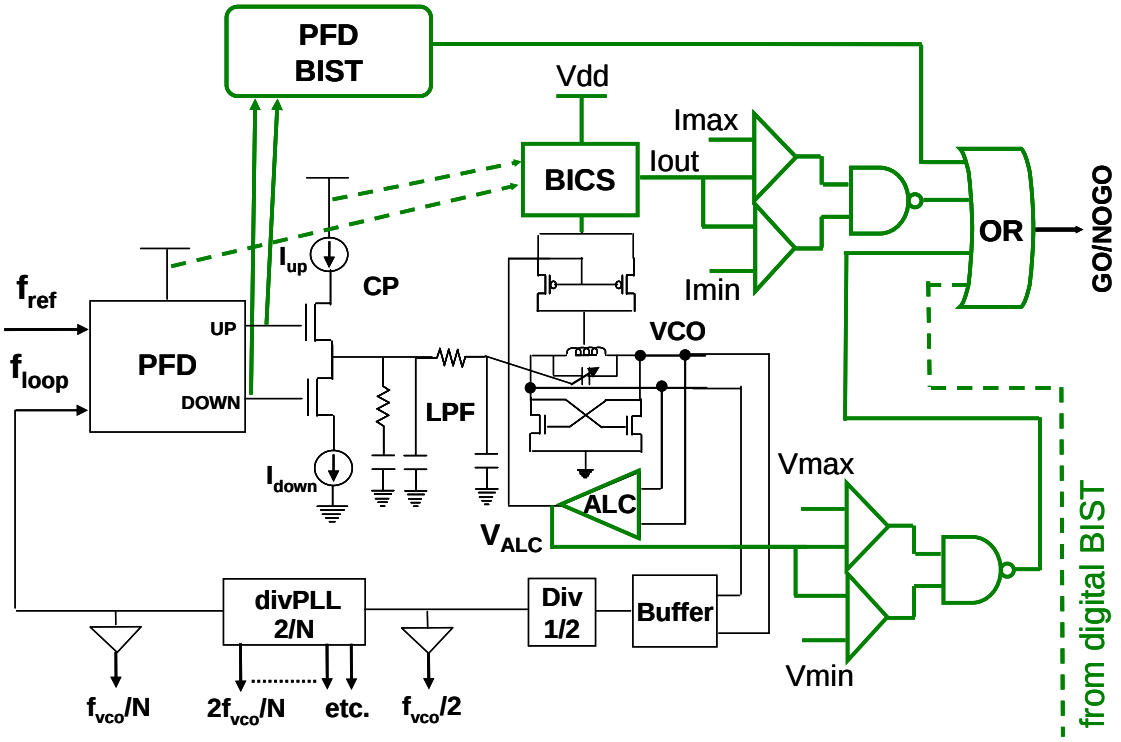


Figure 1. Boucle à verrouillage de phase avec moniteurs embarqués

Les capteurs proposés sont donc :

- Un senseur de courant embarqué (BICS) pour mesurer la consommation de courant du VCO (le BICS peut également être appliquée à d'autres blocs).
- Un comparateur de tension pour la tension continue à la sortie du ALC dans le VCO.
- Un moniteur à la sortie du PFD permettant de mesurer:
  - le « mismatch » de courant du CP
  - les fuites existantes dans le CP, LPF et le « varactor » du VCO
  - la synchronisation entre f_{ref} et f_{loop} (fréquence de sortie)
  - le temps et l'état de verrouillage

5. Moniteurs embarqués

BICS

Le capteur BICS de la Figure 2 a été conçu et redimensionné à partir d'un BICS existant [42] afin de se conformer à la technologie CMOS 65 nm et aux variations du procédé. Néanmoins, la sortie ne doit pas être une tension et ne doit pas être prise sur une résistance (trop sensible aux variations de procédé), comme dans [42]. Au lieu de cela, nous avons choisi comme mesure un courant I_{meas} qui passe dans un miroir de courant comme le montre la Figure 2 (a) et (b). L'idée derrière cette BICS est de faire passer à travers une résistance de faible impédance le courant I_{dd} qui passe de l'alimentation V_{dd} au VCO (courant consommé par le VCO). Une très petite quantité de ce courant (négligeable par rapport à la consommation du VCO) passe dans le miroir de courant du BICS et est amplifié pour obtenir I_{meas}. En outre, la référence des sources de courant I_{max} et I_{min} sont utilisées comme limites de test et comparées avec I_{meas} par le comparateur de courant de la Figure 2 (b). Les sources de référence devraient varier de la même manière que le coeur du BICS avec les déviations du procédé. Pour cela, ils ont une architecture qui est similaire au cœur du BICS lui-même, comme le montre la Figure 2 (c), où I_{ref} est une source de courant stable remplaçant Idd du coeur du BICS.

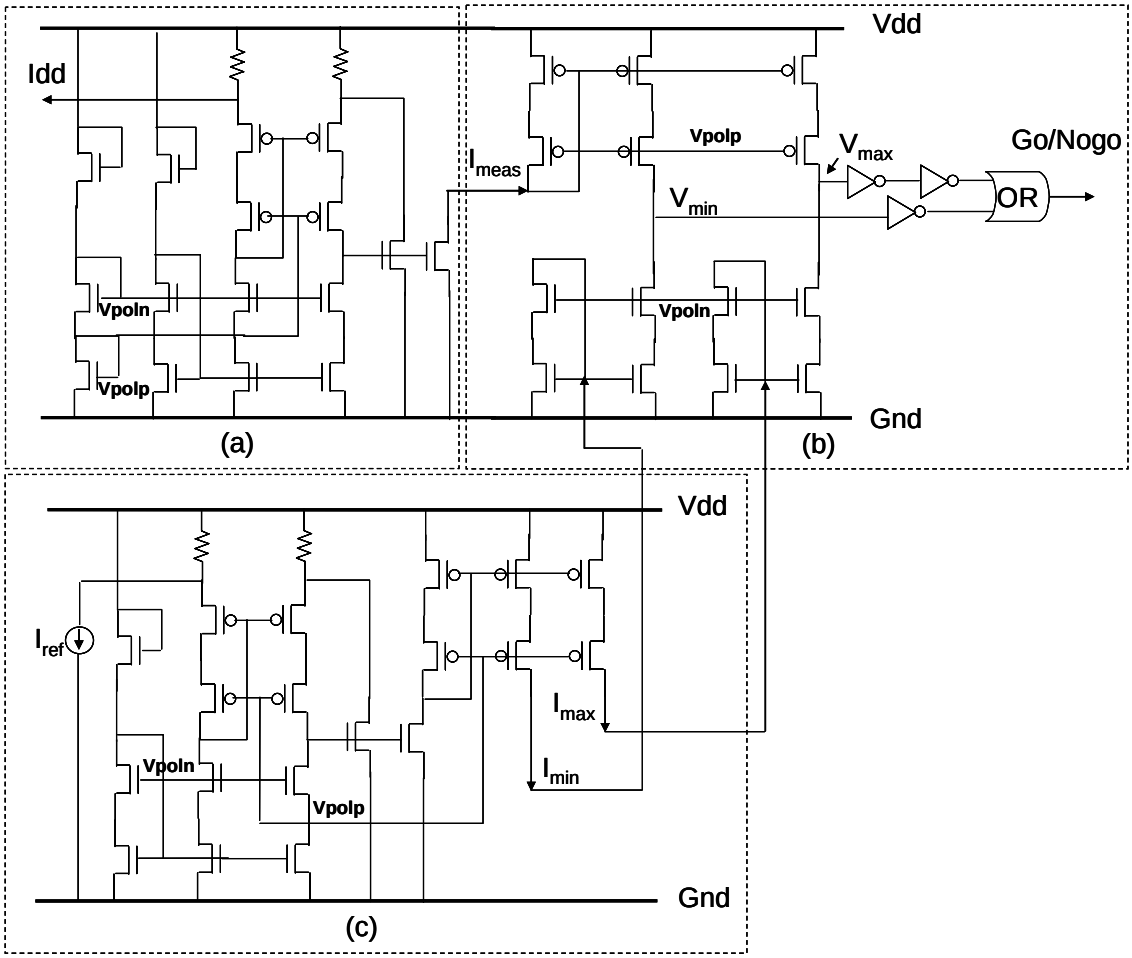


Figure 2. Schéma du senseur de courant embarqué : (a) coeur, (b) comparateur de courant et (c) sources de courant de référence

Comparateur de tension

Le comparateur de tension est montré en Figure 3. Il utilise deux comparateurs et deux sources de tension de référence V_{min} et V_{max}. Le comparateur a été choisi parmi les circuits de STMicroelectronics. La conception et le « layout » du comparateur en technologie CMOS 65 nm existent déjà. Les sources de tension sont actuellement externes. Pour des fins de type BIST elles doivent être intégrées et devraient varier avec les déviations du procédé de la même manière que V_{alc}.

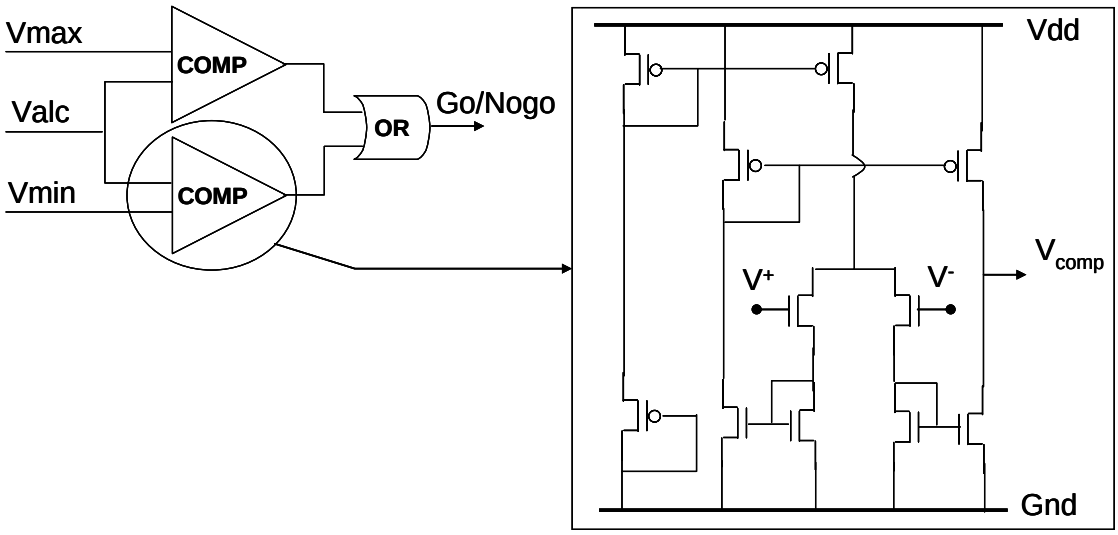


Figure 3. Schéma du comparateur de tension

Moniteur du PFD

Le moniteur du PFD est représenté dans la Figure 4. Ce circuit est capable de détecter si le « mismatch » de courant du CP est conforme aux spécifications. Soit d_{tinv2} le retard introduit par deux inverseurs en cascade (élément de retard) et $n*d_{tinv2}$ le délai maximum acceptable entre les signaux UP et DOWN. Ceci peut dériver du « mismatch » maximal du courant acceptable dans le CP comment expliqué graphiquement en Figure 5 qui illustre le comportement de la boucle à verrouillage de phase sous l'effet du « mismatch » de courant du CP.

Considérons le cas $I_{down} > I_{up}$ qui active le coeur en haut du moniteur de la Figure 4. Se référant au schéma du cœur du moniteur représenté en Figure 4, le signal UP du PFD est appliqué à la pin IN du moniteur du PFD. Ce signal est retardé par n-1 éléments de retard. Des bascules D sont connectées à la sortie de chaque élément de retard. Le signal DOWN du PFD est appliqué à la pin CLK du moniteur qui fournit le taux d'échantillonnage aux bascules D pour l'échantillonnage du signal UP retardé. Le signal DOWN est également retardé par un élément de retard afin de respecter des contraintes de temps de la première bascule D dans le cas idéal que les fronts montants du UP et du DOWN sont parfaitement alignés, en évitant les phénomènes de métastabilité. Les sorties des bascules D, Q_1, Q_2, ..., Q_i, ..., Q_n dans la Figure 4, donner une signature,

rapporté dans le Tableau 1, qui seront utilisés pour prendre une décision de type Go/No-Go. La boucle à verrouillage de phase ne fonctionne pas correctement et/ou de le « mismatch » n'est pas conforme aux spécifications si tous les sorties des bascules D sont égales à 1 ou 0 en même temps. Ceci sera illustré plus en détail plus tard. La fonction logique pour obtenir le signal de type Go/No-Go est alors donnée par $T_i = \overline{\sum_{j=1}^{i+1} Q_j} + \prod_{j=1}^{i+1} Q_j$ où 0 = Go et 1 = No-Go. T_i dans la Figure 4 est le résultat de cette opération booléenne sur les sorties des bascules D de i d'éléments de retard. Le véritable signal numérique T_i considéré comme sortie du BIST dépendra du « mismatch » maximal toléré.

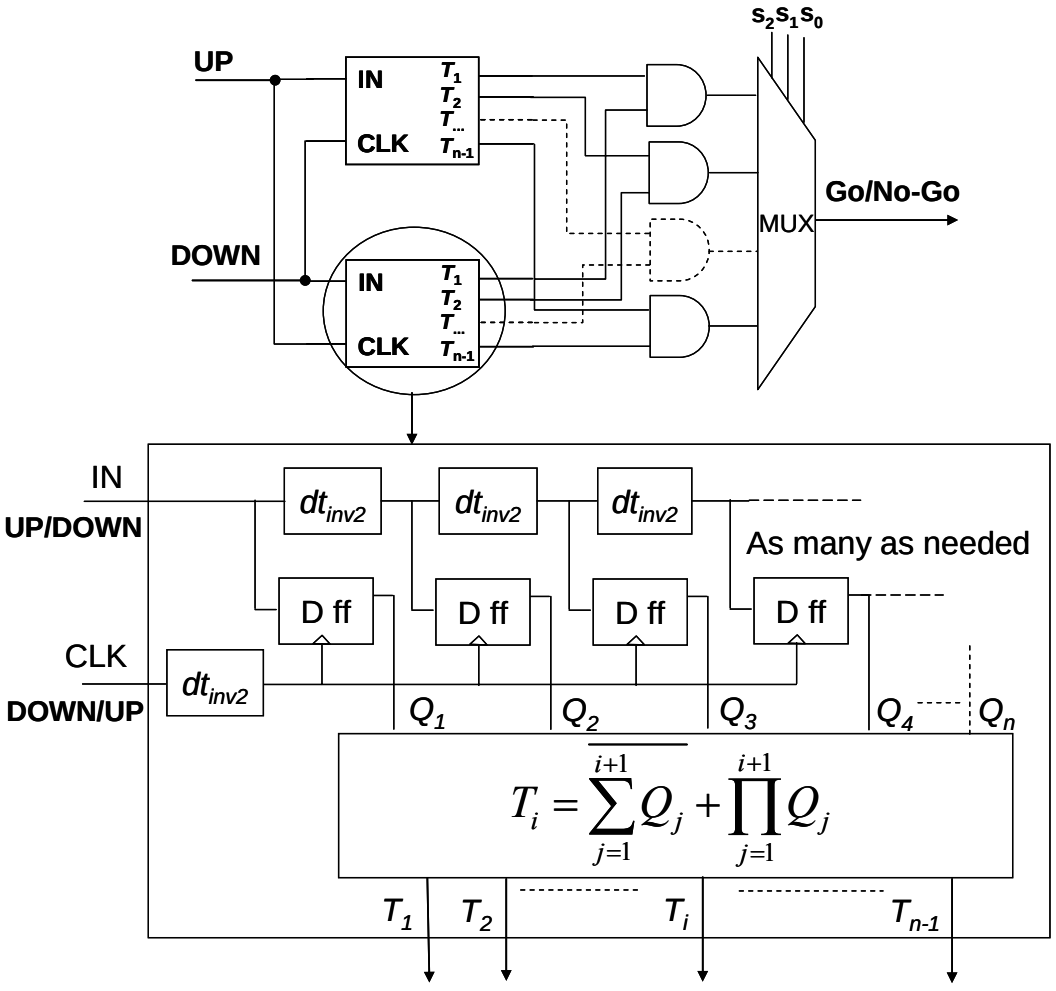


Figure 4. Schéma du moniteur du PFD

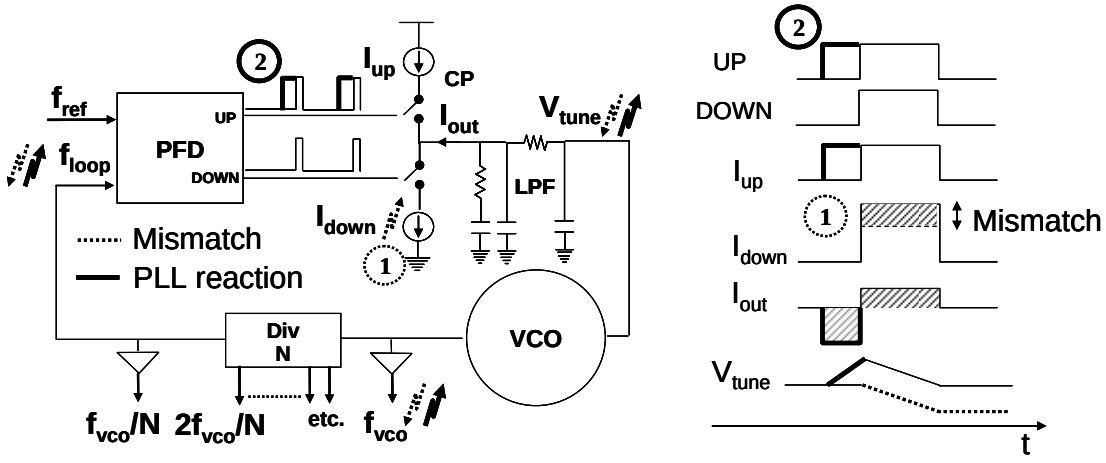


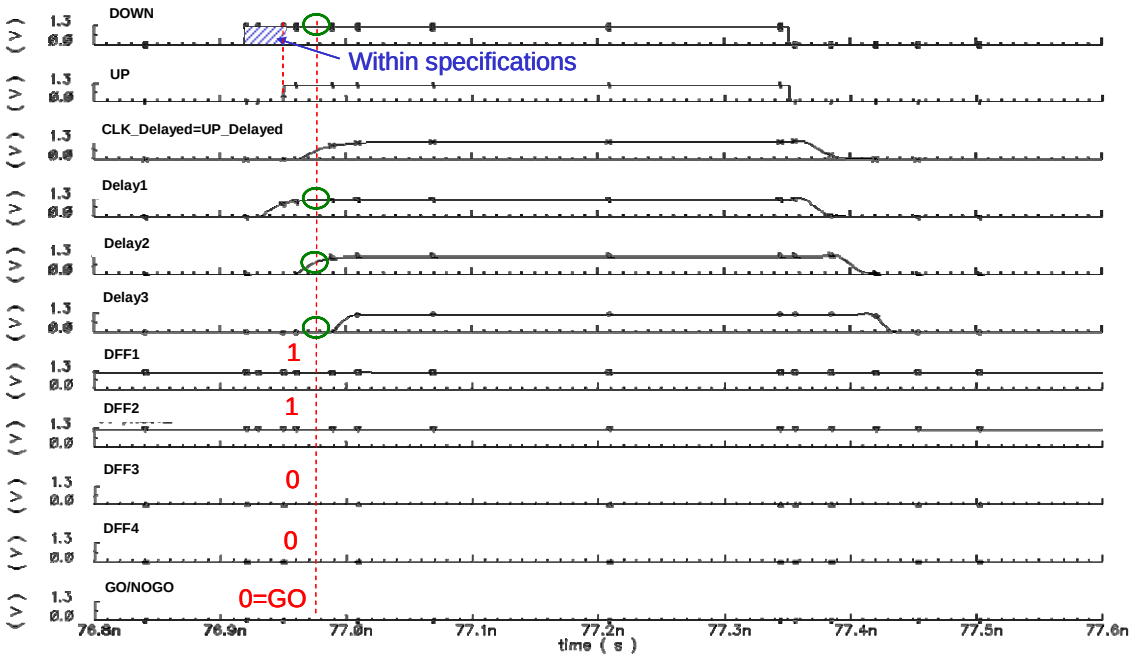
Figure 5. Comportement d'une boucle à verrouillage de phase sous l'effet du "mismatch" du courant de la pompe de charge

Un MUX peut être utilisée pour définir le « mismatch » maximal toléré par la sélection d'un nombre donné d'éléments de retard *i* pour calculer le signal de type Go/No-Go, en sélectionnant la sortie voulait T_i. Par exemple, un MUX avec trois pins de sélection (8 délais de « mismatch » sélectionnables possibles) donne l'éventail des signatures valables pour le moniteur du PFD indiqué dans le Tableau 1, dans le cas où on considère 8 éléments de retard avec $d_{tinv2} \approx 25$ ps sur le signal IN et 9 bascules D. Notez que X représente soit des 1s ou des 0s, et uniquement des séquences de 1s suivie par des séquences de 0s sont possibles. Par exemple, si le MUX est fixé à 011 (« mismatch » maximal toléré de 75 ps), le nombre d'éléments de délai nécessaire est de $i = 4$ et le Go/No-Go de sortie sera égal à T_4 qui sera égale à 0 (Go) si les signatures D flip-flop sont 1XXX00000 (« mismatch » inférieur à 75 ps) et 1 pour toutes les signatures égal à 11111XXXX (décalage supérieur à 75 ps).

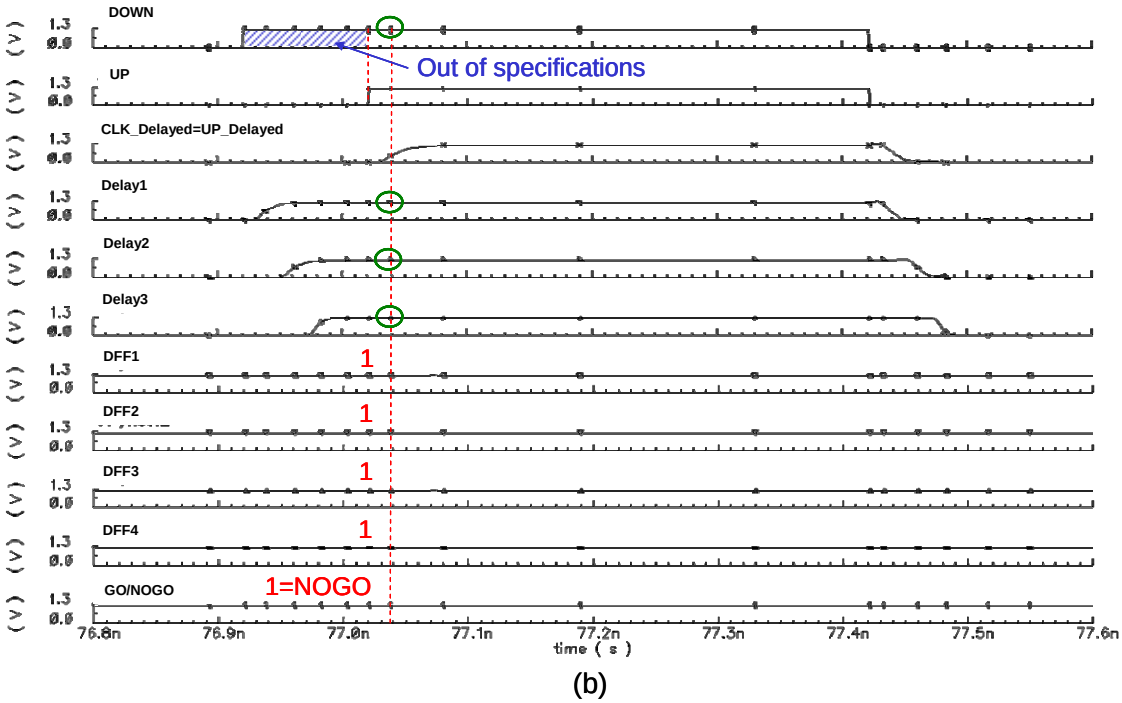
MUX	Max mismatch in ps	Selected T_i	Allowed D ff signatures
000	0	T_1	100000000
001	25	T_2	1X0000000
010	50	T_3	1XX000000
011	75	T_4	1XXX00000
100	100	T_5	1XXXX0000
101	125	T_6	1XXXXX000
110	150	T_7	1XXXXXX00
111	175	T_8	1XXXXXXX0
Step in ps	25		

Tableau 1. Sélection du délai de "mismatch" maximale

Dans la Figure 6 tous les signaux du cœur du moniteur du PFD avec 3 éléments de délai et 4 bascules D (comme dans la Figure 4) sont simulées. Cette configuration autorise un « mismatch » jusqu'à 50 ps. Deux cas sont présentés : dans la Figure 6 (a) le « mismatch » est de 30 ps, ce qui répond aux spécifications et dans la Figure 6 (b) le « mismatch » est de 80 ps, ce qui en dehors des spécifications.



(a)



(b)

Figure 6. Simulations du coeur du moniteur du PFD avec un "mismatch" maximale toléré de 50 ps (a) "mismatch" de 30 ps dans les spécifications et (b) "mismatch" de 80 ps en dehors des spécifications

En surveillant le signal de sortie Go/No-Go, il est possible d'identifier le moment où l'état de verrouillage est atteint, comme le montre la Figure 7. Ainsi, cette technique peut être utilisée aussi comme un détecteur de verrouillage. En fait, le signal Go/No-Go va à la valeur logique bas (Go) lorsque les fronts montants des signaux UP et DOWN sont retardés l'un par rapport à l'autre de moins du « mismach » maximale toléré. Dans les résultats de la simulation de la Figure 7, le décalage entre le retard et des signaux UP et DOWN est de 85 ps (voir zoom) et le moniteur BIST a été conçu pour donner un Go (valeur logique bas) en sortie pour un « mismatch » inférieur à 100 ps.

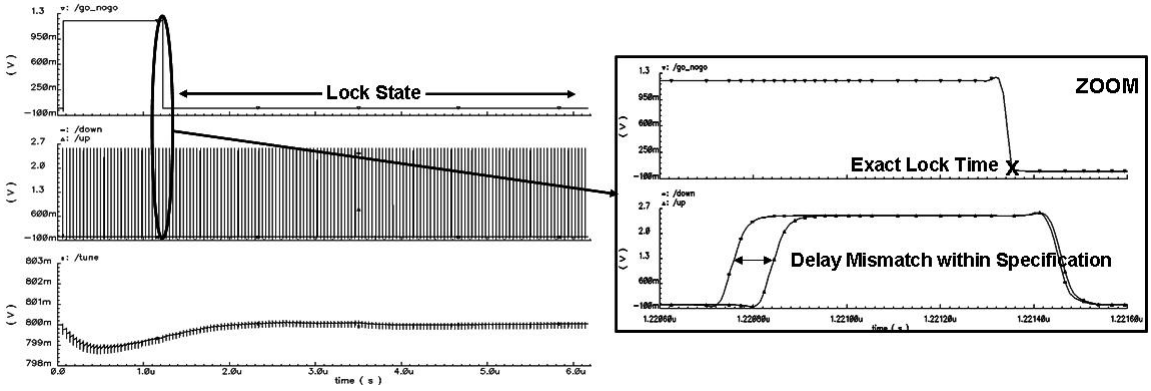


Figure 7. Sortie de type Go/No-Go style détecteur de verrouillage

Effet de l'insertion des moniteurs sur le fonctionnement du circuit sous test

Une dégradation négligeable de performances en raison des capteurs embarqués dans le VCO a été évaluée par simulation : une dégradation de bruit de phase de 1.2 dBc/Hz à 10 MHz de la porteuse et une diminution de la fréquence de sortie de 20 MHz sur 7.5 GHz. La consommation de courant est évidemment plus élevé (16 mA pour la BICS et de 0.5 mA pour le comparateur de tension). Le moniteur de sortie PFD ne se dégrade pas les performances car il sonde nœuds numériques. Le surcoût en surface de tous les moniteurs BIST est d'environ 6.54 % de la boucle à verrouillage de phase SERDES utilisé comme cas d'étude.

Afin de fixer des limites pour les mesures de test, des simulations Monte-Carlo et d'injection de fautes doivent être effectuées et un compromis entre les métriques de test tels que la perte de rendement et le niveau de défaut paramétriques, aussi avec la couverture de fautes doit être trouvée, selon les spécifications fournies.

6. Evaluation des métriques de test du VCO

Le circuit pris comme ces d'étude est le VCO d'une boucle à verrouillage de phase RF qui peut fonctionner à 7.5 ou 9 GHz. La boucle à verrouillage de phase a été conçue et fabriquée en technologie CMOS065 RF LP chez STMicroelectronics. L'occupation de surface est de 0.102 mm^2. Sa fréquence de référence est de 25 MHz ou 30 MHz. Dans

cette section, seuls les simulations du VCO sont discutées. Le VCO a comme fréquence libre de 6.9 à 8.9 GHz ou de 8.3 à 10.3 GHz avec un gain (K_{vco}) de 0.4 à 1.7 GHz/V, avec une bande passante de 100 kHz et une marge de phase de 55 °.

Avant embarquement des moniteurs sur le VCO, des limites sur les mesures de test doivent être fixées de manière à concevoir les moniteurs de façon appropriée pour les rendre robustes dans la gamme de fonctionnement. Une fois que les limites sont fixées, une première évaluation des mesures de test peut être effectué. En fait, ces limites sont fixées compte tenu des variations du procédé, de sorte que la technique de test encourt valeurs minimales de la perte de rendement et du niveau de défaut. Un modèle statistique du circuit sous test est nécessaire pour fixer ces limites.

Une fois les limites de test sont définies, la couverture de fautes est évaluée pour des fautes injectées. Dans ce travail, nous avons considéré des fautes catastrophiques dans le VCO. Étant donné le grand nombre de fautes, il est impossible de considérer la simulation de fautes dues aux déviations du procédé (fautes paramétriques). Ainsi, seuls les simulations nominal ont été effectués. Ces défauts sont des circuits ouverts entre chaque noeud d'un composant et court circuits entre ses nœuds. Les circuits ouverts sont modélisés comme une résistance élevée (10 MΩ) et les courts circuits comme une faible résistance (1 Ω), comme l'a déjà fait dans des travaux précédents [48]. Circuits ouverts dans les grilles des portes n'ont pas encore été injecté car ils doivent inclure des capacités parasites du noeud flottant, ce qui doit être extraite du « layout ».

Toutes les simulations sont effectuées dans l'environnement CADENCE SPECTRE RF. Les injections de fautes sont automatisées grâce à une plate-forme CAT ([10]) qui s'exécute sous Cadence. Etant donné que le VCO à l'étude est réglable, la configuration choisit est de activer à tous les transistors dans le « varactor », afin d'effectuer un test complet. Dans cette configuration, le nombre de fautes catastrophiques injecté dans le VCO est de 108 (courts circuits et circuits ouverts).

Modèle statistique du VCO basé sur les copules

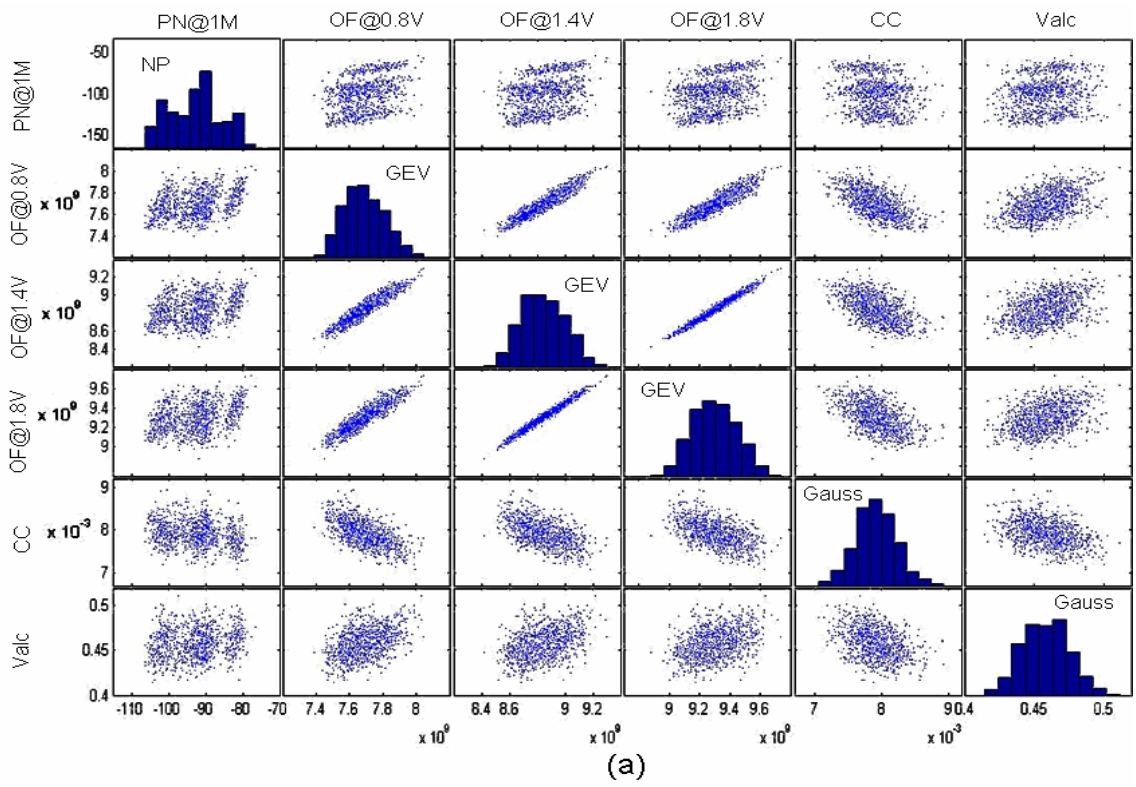
Pour fins d'évaluation des métriques de test, nous générons une population initiale de notre bloc VCO, illustré en Figure 8 (a), en utilisant la simulation Monte-Carlo, où PN représente le bruit de phase, CC la consommation de courant, OF la fréquence de sortie, et V_{alc} la tension de sortie crête à crête.

Un modèle statistique pour le VCO peut être obtenu par simulation de Monte-Carlo. Pour cette analyse, seul un nombre limité de cas de circuits ont été créés (1000 dans notre cas). Ces 1000 cas sont insuffisants pour fixer des limites de test avec une précision suffisante. Afin d'avoir une population représentative, nous allons utiliser une technique d'estimation de densité de probabilité. La fonction de densité de probabilité conjointe (PDF) des performances du VCO et des mesures de test est obtenue à partir des 1000 instances de Monte-Carlo en utilisant la théorie des copules tel qu'il figure dans [49]. Ce modèle statistique est ensuite échantillonné afin de produire un million instances qui permet de fixer les métriques de test avec une précision de parts par million (ppm). La population sera générée à partir de l'original. D'autres techniques d'estimation de densité ont été utilisées dans le passé, y compris l'usage des distributions normales multivariées et l'estimation de densité basée sur le noyau (KDE). Dans ce travail nous avons utilisé la théorie de copules puisque les données d'origine se rapprochent bien à une copule gaussienne telle que décrite ci-dessous.

Comme mentionné ci-dessus, nous avons considéré le bruit de phase, la fréquence de sortie pour différentes valeurs de V_{tune} et consommation de courant comme performances du VCO. Les mesures fournies par les moniteurs intégrés comprennent la consommation de courant, la fréquence de sortie pour V_{tune} à la valeur nominale de 0.8 V, et la tension de sortie crête à crête.

Nous avons ensuite utilisé la théorie de copules pour estimer le PDF multivariée conjointe des performances et des mesures de test. Cela exige une estimation de la PDF marginal de chaque performance et mesure de test et un PDF multivariée que l'on appelle une copule et qui estime les liens entre les marginaux. Le format PDF marginal

peut être facilement estimé à partir des données d'origine en utilisant des lois bien connues comme la univariée ou les techniques KDE. Le Tableau 2 donne les paramètres statistiques de chaque performance et mesure de test ainsi que les estimations des PDFs. GEV représente la distribution General Extreme Value. Ce type de distribution a besoin de trois paramètres, la valeur moyenne μ, l'écart type σ et le paramètre de forme k. NP représente la distribution non paramétrique obtenu par une méthode de KDE. Le paramètre de fenêtre (largeur) est nécessaire pour définir cette distribution. Gauss est une distribution gaussienne.



(a)

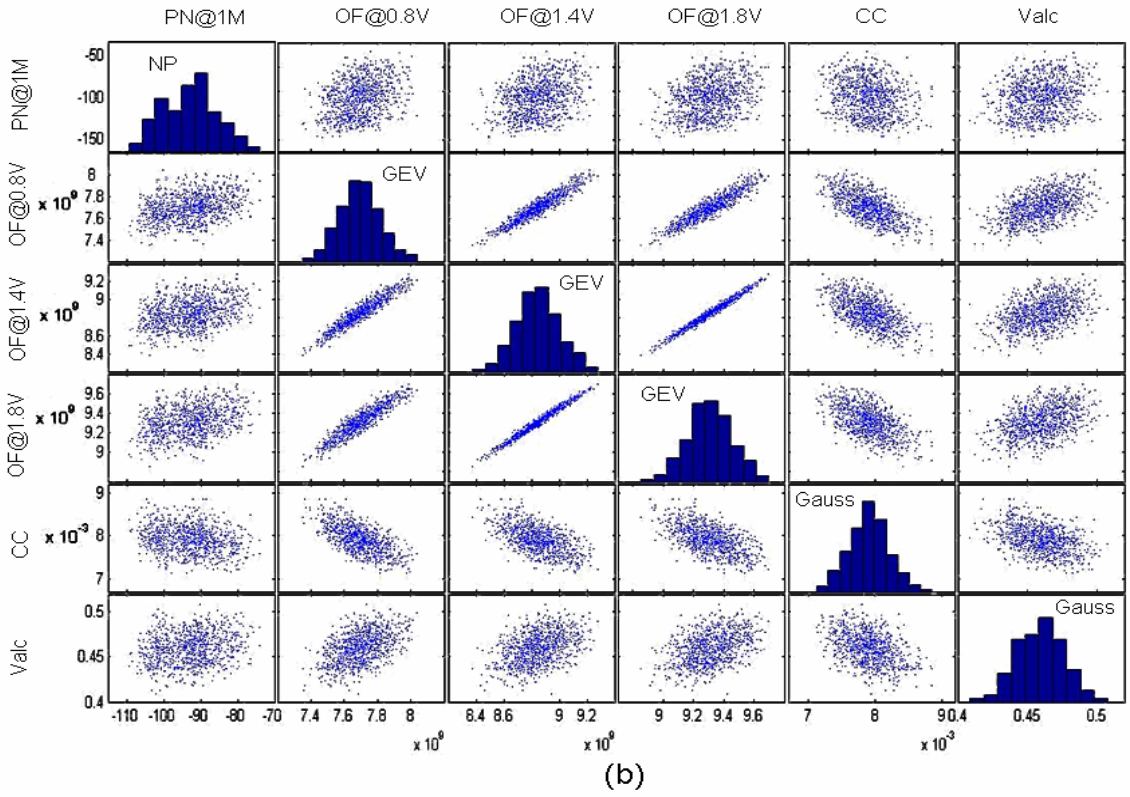


Figure 8. Echantillons des performances et mesures de test du VCO obtenues des (a) simulations Monte-Carlo (b) model base sur les copules (1000 instances)

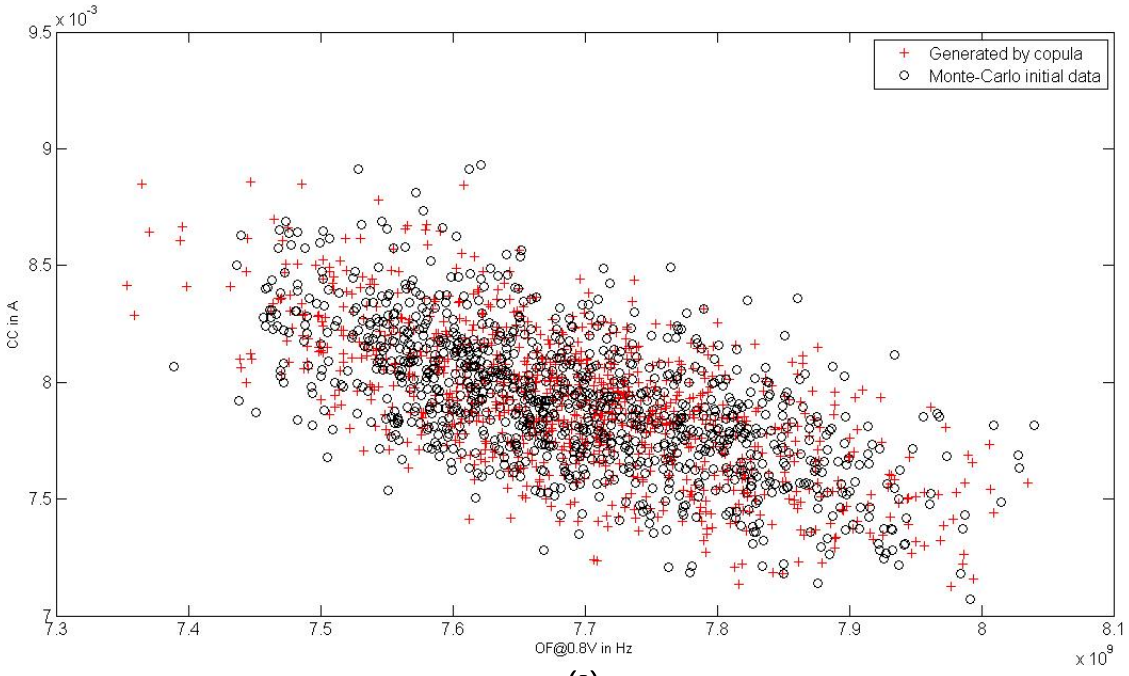
Perf/TM	Dist	Paramètres			
		μ	σ	largeur	k
PN@10kHz	NP	-33.7 dBc/Hz	7.01 dBc/Hz	1.99 dBc/Hz	-
PN@100kHz	NP	-63.6 dBc/Hz	6.91 dBc/Hz	1.98 dBc/Hz	-
PN@1MHz	NP	-92.6 dBc/Hz	6.92 dBc/Hz	1.97 dBc/Hz	-
PN@10MHz	NP	-109 dBc/Hz	3.12 dBc/Hz	1.01 dBc/Hz	-
OF@0.8V	GEV	$7.69 \cdot 10^{9}$ Hz	$1.20 \cdot 10^{8}$ Hz	-	-0.20
OF@1V	GEV	$8.13 \cdot 10^{9}$ Hz	$1.48 \cdot 10^{8}$ Hz	-	-0.20
OF@1.4V	GEV	$8.84 \cdot 10^{9}$ Hz	$1.53 \cdot 10^{8}$ Hz	-	-0.23
OF@1.8V	GEV	$9.30 \cdot 10^{9}$ Hz	$1.44 \cdot 10^{8}$ Hz	-	-0.24
CC	Gauss	$7.92 \cdot 10^{-3}$ A	$2.97 \cdot 10^{-4}$ A	-	-
Valc	Gauss	$4.58 \cdot 10^{-1}$ V	$1.65 \cdot 10^{-2}$ V	-	-

Tableau 2. Distributions des performances et des measures de test du VCO

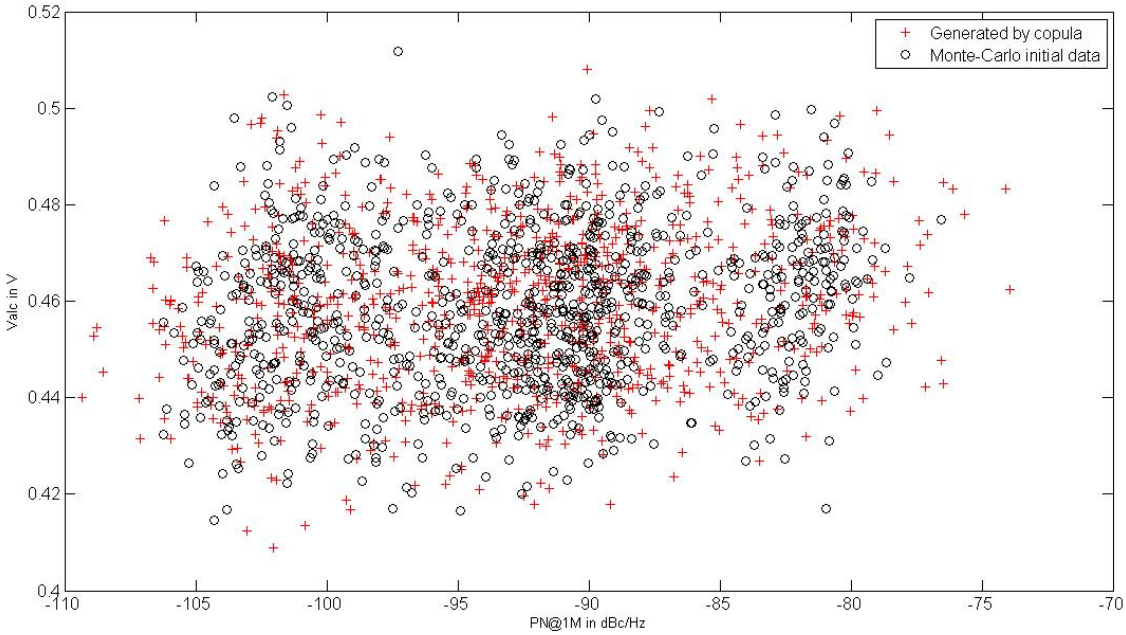
La copule peut souvent être choisis parmi un ensemble de fonctions connues et calibrées pour un cas d'étude donné. Dans notre cas, une copule gaussienne a été utilisée. Les paramètres de cette copule se trouvent à partir des facteurs de corrélation des données

d'origine. Détails sur la validité du modèle statistique sont hors de la portée du présent document. Une inspection visuelle permet d'illustrer la validité de la copule gaussienne. La Figure 9 montre deux distributions bivariées (a) des 1000 instances d'origine et (b) des 1000 instances générées. Les deux distributions correspondent très bien. Des résultats similaires sont obtenus pour chaque paire de performances et/ou des mesures de test. En Figure 8 (b) sont représentées toutes les distributions bivariées conjointes des performances et des mesures de test obtenues avec la méthode de copules. La Figure 8 (a) et la Figure 8 (b) peuvent être comparé.

Les performances définies comme la fréquence de sortie pour différentes valeurs de V_{tune} sont évidemment fortement corrélés. V_{alc} et le bruit de phase sont moins corrélés avec les autres performances et les mesures de test.



(a)



(b)

Figure 9. Exemples des distributions bivariatées du VCO (1000 instances) avec les data originales et les data échantillonnées du model base sur les copules : (a) CC vs. OF@0.8V et (b) V_{alc} vs. PN@1MHz

7. Analyse de la couverture de fautes

Les limites pour les mesures de test doivent être choisîtes de façon à réduire au minimum le niveau défaut et des pertes de rendement paramétriques et d'optimiser la couverture de fautes. Nous avons mené une campagne de simulation d'injection des fautes pour calculer la couverture de fautes catastrophiques (CFC) en fonction des limites de test comme le montre la Figure 10. Les limites d'une mesure de test sont données en fonction de $\mu \pm x\sigma$, où x est tracée sur la Figure 10. Nous pouvons également envisager le CFC de combinaisons des performances et des mesures de test, également montré en Figure 10, où x est la même pour tous les cas.

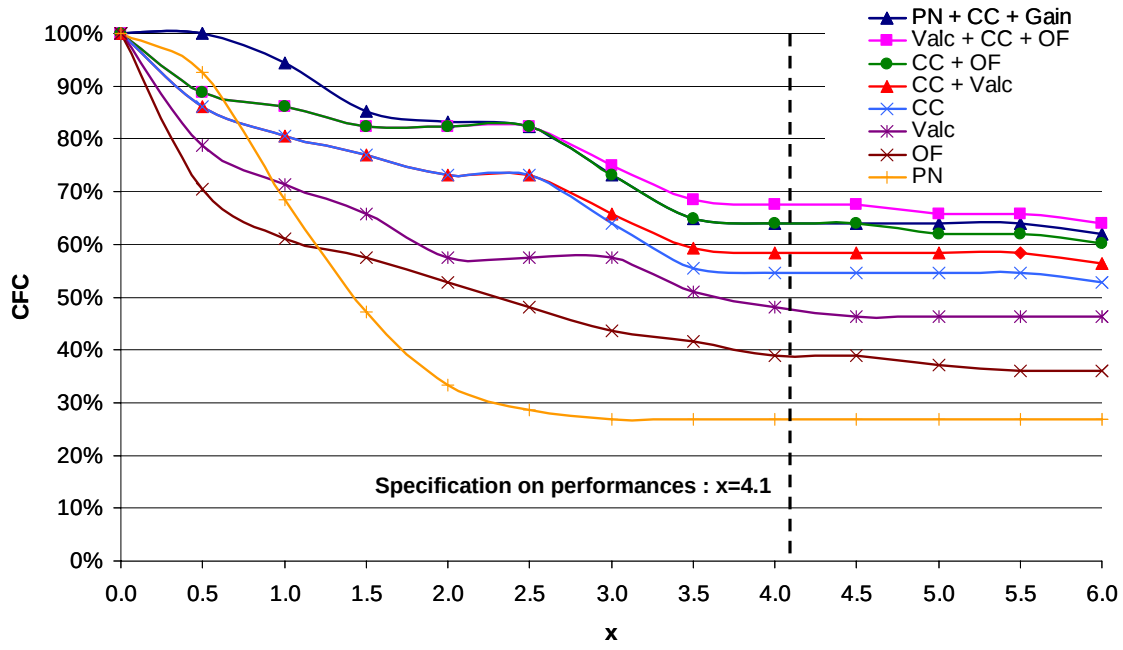


Figure 10. Couverture des fautes catastrophique versus limites de test du VCO

La combinaison de toutes les performances (bruit de phase, gain du VCO, et de la consommation du courant) montre la couverture des fautes catastrophiques la plus élevée de toutes (plus de 80%) jusqu'à 2.5 σ de la valeur nominale. Au-delà de 2.5 σ le CFC donné par la combinaison de toutes les mesures de test (la consommation de courant, V_{alc}, et la fréquence de sortie) devient supérieure au CFC des performances. En outre, afin de se conformer aux spécifications, les limites des performances devraient être fixé à 4,1 σ où elles couvrent 64 % de tous les défauts catastrophiques injecté. Cela souligne le fait que le circuit est robuste à des fautes catastrophiques, ce qui est en effet possible dans certains cas spécifiques. En outre, puisque le « datasheet » de cet circuit est encore au stade du projet, il peut être possible soit de modifier les spécifications ou d'ajouter la puissance de sortie du VCO à l'ensemble des performances, car ceci est souvent fait pour VCO, et que nous avons considérée comme une mesure de test lié à la mesure Valc. Cela amènerait le CFC de mesures de test et des performances au même niveau. Peut-être que si la mesure réelle de la puissance de sortie couvait plus de défauts que la mesure de V_{alc}, le CFC de performances serait encore plus élevé que celui des mesures test. Cela peut être exploré si les concepteurs décident d'ajouter de la puissance de sortie dans les spécifications.

D'après l'examen des résultats obtenus pour diverses combinaisons de mesures de test, on peut en déduire que chaque mesure de test ajoute une certaine couverture des fautes aux autres, donc aucune n'est superflue. En fait, la mesure V_{alc} ajoute 4 % de CFC au cas où seule la CC est mesurée. Un ensemble de CFC de plus de 65 % est obtenu compte tenu de toutes les mesures de test (CC + V_{alc} + OF), environ 10 % de plus qu'en ne considérant que CC + V_{alc}. En fait, l'analyse effectuée en Figure 10 sur les performances et les mesures de test, où toutes les limites varient ensemble, n'est pas formellement exacte, car les performances sont fixées à 4.1 σ par les spécifications, mais elle s'avère intéressant pour certaines considérations fait jusqu'à présent. Les variations des limites sur les performances sont contradictoires car les limites sont définies par les spécifications, mais il est encore intéressant pour étudier la robustesse des circuits vers les performances. Ainsi, il serait plus judicieux de tracer les CFC en faisant varier seulement les limites de test de V_{alc} et maintenir celles des performances utilisés comme mesures de test fixée à 4.1 σ. Dans la Figure 11, nous avons décrit cette situation. Le CFC de Valc reste constante après 2.5 σ à 67,6 %.

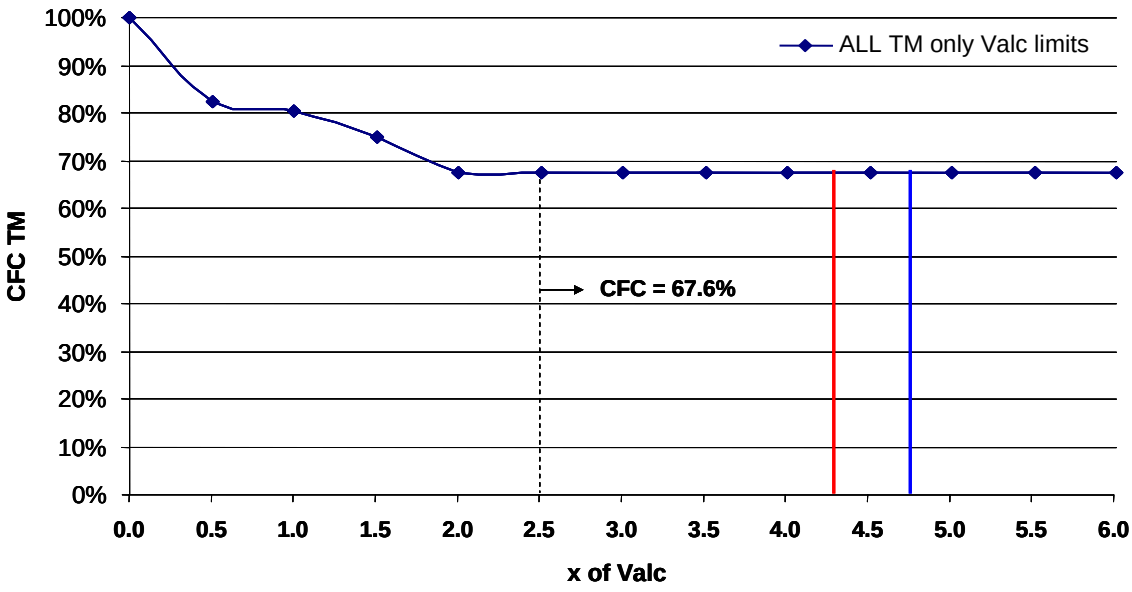


Figure 11. CFC des toutes les mesures de test versus les limites de test de V_{alc}

A 4,1 σ presque tous les défauts qui ne sont pas détectés par les performances ne sont pas non plus détectés par les mesures de test, à l'exception des 4 fautes sur 108 (3,7%)

qui sont détectés par la seule mesure de test qui n'est pas une performance : V_{alc}. C'est aussi pourquoi le CFC est plus élevé pour les mesures de test que pour les performances. Ces 4 fautes sont des circuits ouverts sur les transistors PMOS utilisés comme sources de courant pour le VCO et pilotés par le V_{alc}. Tous les autres défauts sont soit détectés par les performances et les mesures de test au même temps, ou pas détecté par aucune des deux.

8. Mesures de test et limites de test optimisées

Comme mentionné ci-dessus, les limites de test doivent être choisîtes afin d'optimiser le CFC, le niveau de défaut et de pertes de rendement paramétriques. En utilisant le modèle statistique, le niveau des défauts et des pertes de rendement pour les variations dans le procédé sont tracés dans la Figure 12 en fonction de la limite de test x. La limite de test optimale doit tenir compte d'un compromis entre le niveau des défauts et des pertes de rendement et elle fait référence à la mesure de test V_{alc} seulement, car les limites pour les deux autres mesures de test (la consommation de courant et la fréquence de sortie) sont définies par les spécifications. Les spécifications sur les performances sont fixées à 4.1 σ. Cela génère 196 dispositifs non fonctionnels sur la population de 1 million de circuits.

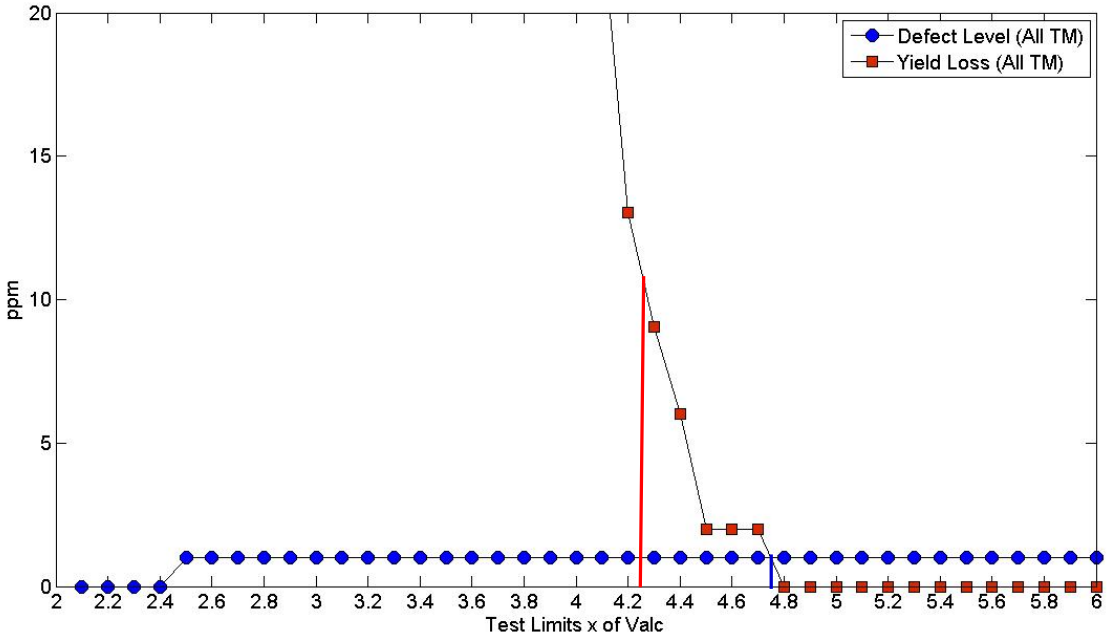


Figure 12. Niveau des défauts et des pertes de rendement paramétriques de toutes les mesures de test versus les limites de test de V_{alc}

Imposant le de niveau de défaut égale à la perte de rendement (ligne bleue dans la Figure 11 et la Figure 12), le modèle statistique donne une valeur de 1 ppm. Ceci définit la limite de V_{alc} à environ x = 4.75, qui se traduit par un CFC de 67,6 %. Considérant acceptable d'avoir une perte de rendement dix fois plus élevée que le niveau de défaut conformément à la règle des 10 [51] (ligne rouge dans la Figure 11 et la Figure 12), le modèle statistique donne un niveau de défaut d'environ 1 ppm, la perte de rendement de 10 ppm, et le CFC toujours de 67,6 % à la limite de V_{alc} fixé à x = 3.87. Dans ce cas précis, il n'est pas utile de recourir à la règle de dix car elle ajoute que de la perte de rendement sans pour autant améliorer la couverture de fautes ou le niveau de défaut.

Dans les cas génériques, le choix des limites de test doit être fait en fonction du produit et les exigences des clients sur les métriques de test.

9. Conclusions

La conception pour le test doit faire face à la difficulté d'évaluer la qualité de test avant la production. Ce travail présente une technique de test pour les boucles a verrouillage

de phase RF qui utilise des moniteurs embarqués et se concentre sur l'évaluation de cette technique pour le VCO et le CP. D'autres travaux du même type de celui mené sur le VCO ont été effectués afin d'évaluer la technique de test pour les autres blocs de la boucle à verrouillage de phase, en particulier le bloc CP. Les limites de test pour les moniteurs embarqués sont optimisées en fonction du niveau de défaut paramétrique, de la perte de rendement paramétrique et de la couverture de fautes catastrophiques. La méthodologie pour l'estimation du niveau de défaut et de perte de rendement paramétriques utilise un modèle statistique basé sur la théorie copules. La couverture de fautes catastrophiques est évaluée par la simulation d'injection de fautes. Il a ensuite été possible de comparer les capacités de détection de défauts de trois simples mesures de test en ce qui concerne les performances fondamentales du VCO et du CP.