

eFPGAs: Architectural Explorations, System Integration & a Visionary Industrial Survey of Programmable Technologies

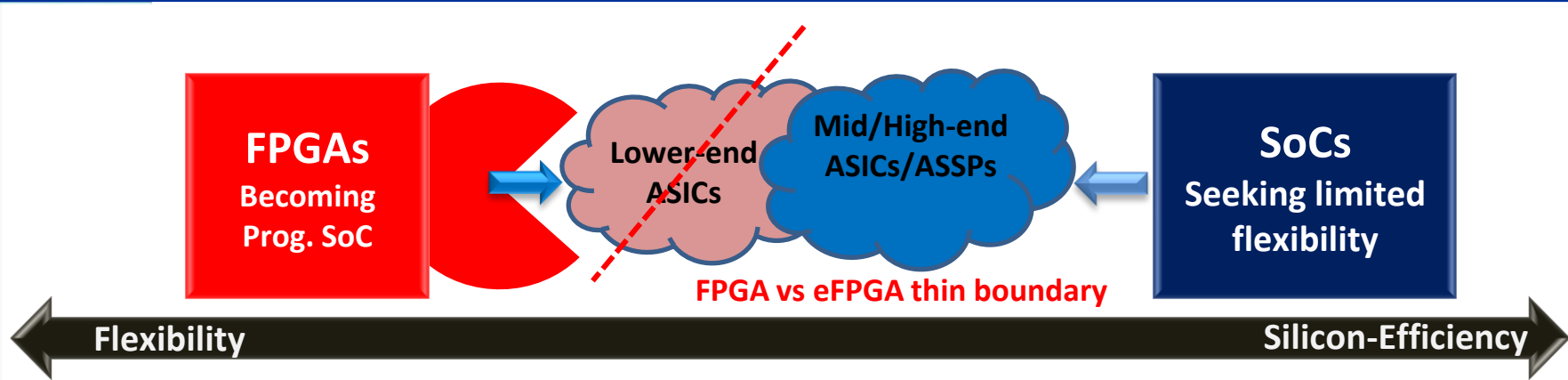
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Wed. June 22, 2011, 14:30h, LIRMM seminar hall
Montpellier, FRANCE



What, Why, Where eFPGAs?



eFPGA: Inverse of FPGA, reduce FPGA vs ASIC gap

Hard for:

- FPGA vendors to become System provider for/to all
- ASIC/ASSP guys to drop their product to FPGAs

Semiconductor Industry (2009-10) (~230B\$)

Segment: FPGAs (~4B\$) , ASICs/ASSPs (~80B\$)

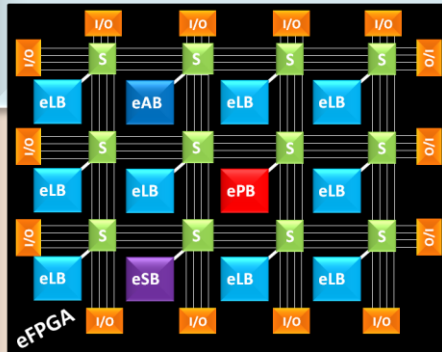
Beyond 65nm SoC Costs: 50+M\$

Global Overview of Thesis Work/Contributions

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Survey & Analysis

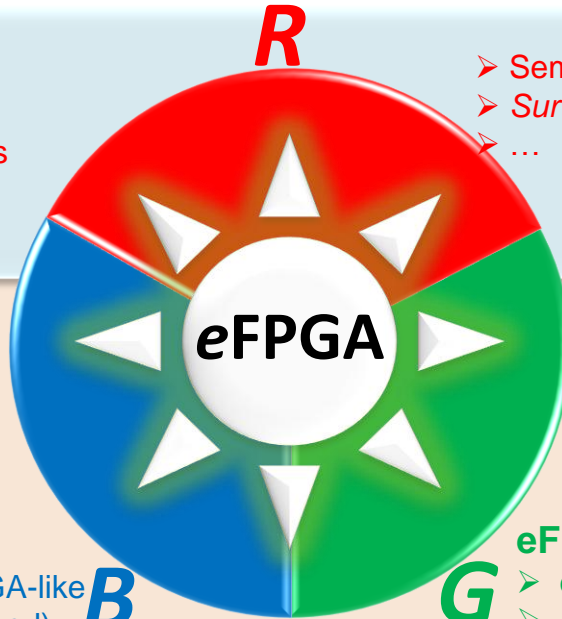
- FPGA State of the Art: literature, patents, press news
- Potentials of emerging trends



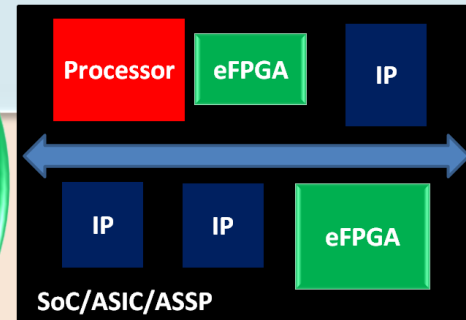
eFPGA architecture

- Exploration of *efficient!* FPGA-like conventional eFPGAs (LUT-based)
- Creation of CAD Tools infrastructure
- Soft eFPGAs (tech. node independent)
- ...

R



- Semiconductor industry analysis
- Survey of Programmable technologies
- ...



eFPGA in system

- eFPGAs applications/challenges
- eFPGAs as Reconf. accelerators
- Case studies for perspectives of beyond classic eFPGAs (MRAM etc.)
- ...

B

G

iPhD

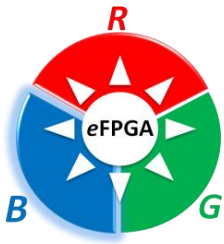
Talk Outline

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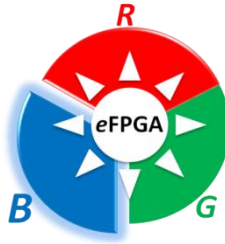
FPGA/eFPGA State of the Art & Industrial Survey



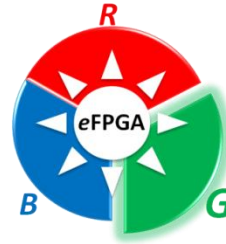
eFPGA Arch. & CAD



eFPGA Arch. Exploration



eFPGA In Systems



Concl. & Future



iTalk

Survey & Analysis

- > FPGA State of the Art: literature, patents, press news
- > Potentials of emerging trends
- > Semiconductor industry analysis
- > Survey of Programmable technologies

eFPGA architecture

- > Exploration of *efficient*, FPGA-like conventional eFPGAs (LUT-based)
- > Creation of CAD Tools, infrastructure
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eFPGA in system

- > eFPGAs applications/challenges
- > eFPGAs as Reconfig. accelerators
- > Case studies for perspectives of beyond classic eFPGAs (MRAM etc.)

IPhD

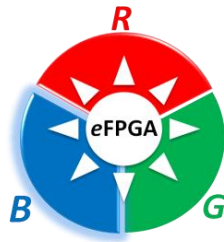
Outline

5

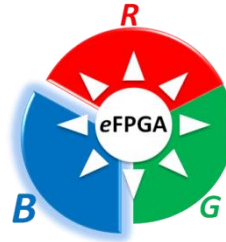
FPGA/eFPGA State of the Art
& Industrial Survey



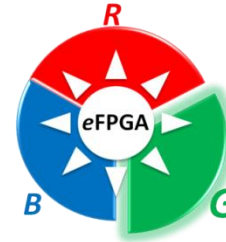
eFPGA
Arch. & CAD



eFPGA
Arch. Exploration



eFPGA
In Systems



Concl. & Future



iTalk

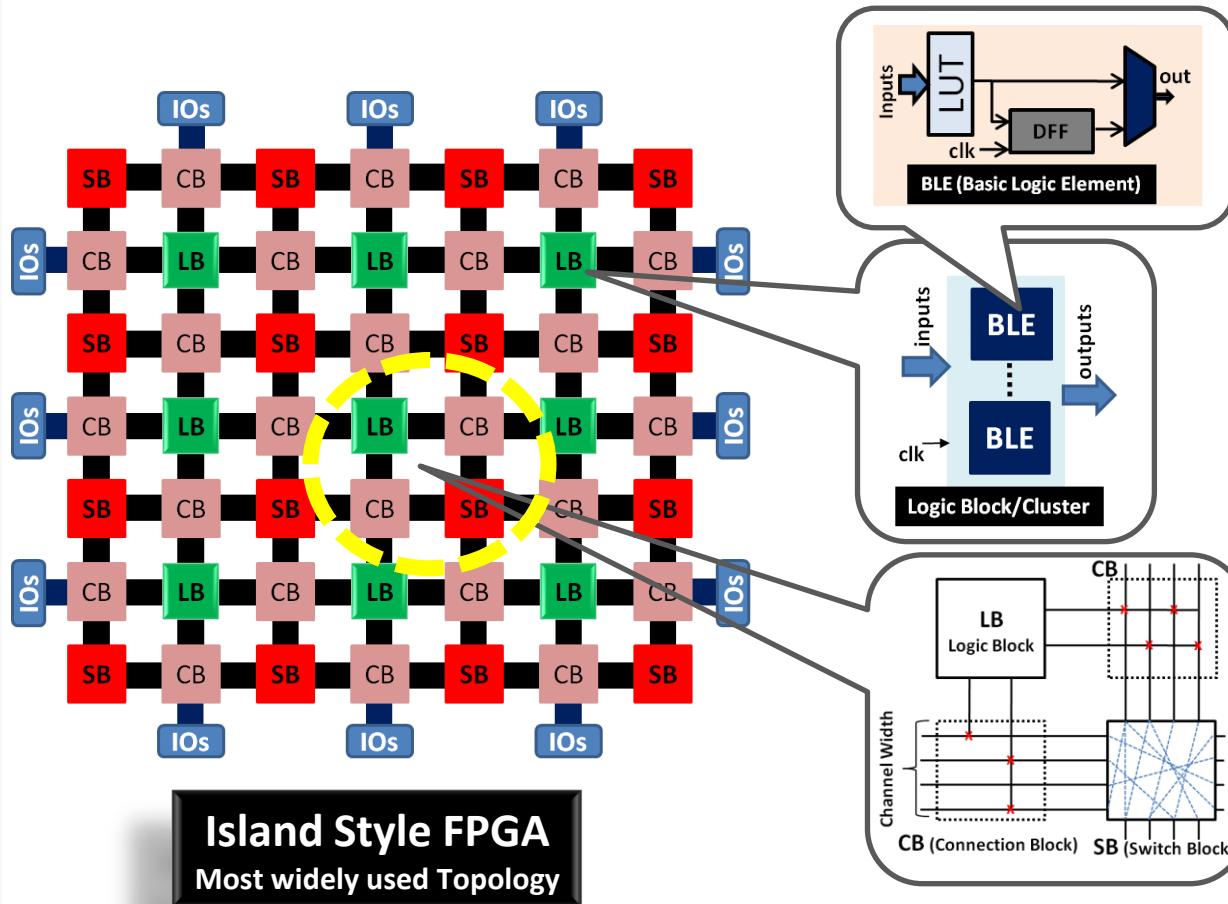
Only Basics

- FPGA Fundamentals
- FPGA/eFPGA State of the Art
- Industrial survey (key conclusions for eFPGAs)
 - ❖ Survey is published in detail in **FPL-10**

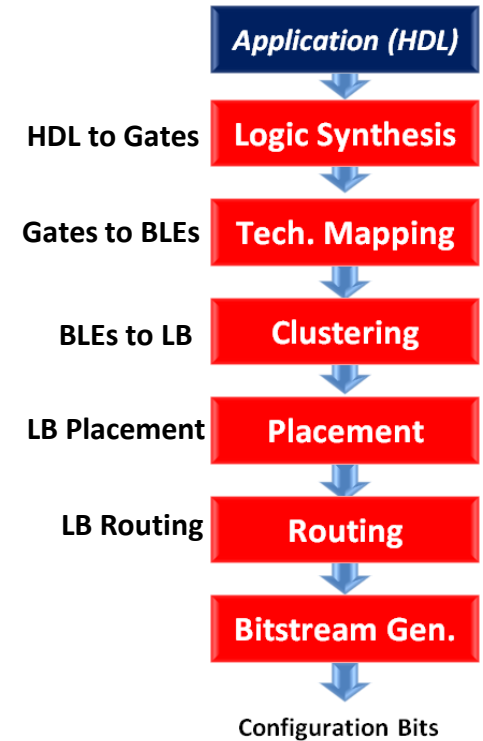
“Survey of new trends in Industry for Programmable hardware: FPGAs, MPPAs, MPSoCs, Structured Asics, eFPGAs and new wave of innovation in FPGAs”

FPGA Fundamentals

(Vendor Independent)



Programming Flow



FPGA/eFPGA State of the Art

Xilinx Altera The **BIG-2** (>80% market share of PLD)

Lattice Actel (MicroSemi) Atmel QuickLogic

Startups {

Achronix (Async. FPGAs)	SiliconBlue (Low Power FPGAs)	Tabula (Time Multiplexed FPGAs)
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**AboundLogic (Ultra high density Low Cost FPGAs)*
 **Tier Logic (3D FPGA, Easy ASIC migration)*
 (**RIP 2010*)

Academics (FPGA Arch.)

Highest Citation: Toronto Univ. VPR work

Some other notable: UBC, LIP6, Cornell Univ., UCLA ...

Key New Trends in leading FPGAs:

Mainstream: Hard Processors, 3D stacking, ESL

Adv. Research: (Async., Packet-based routing, New Memories...)

Some of eFPGAs Attempts

Adaptive Silicon (2001)

Actel Varicore (2001)

Leopard Logic (2002)

IBM-Xilinx (2002)

Last known warrior
M2000/Abound (2008/2010)

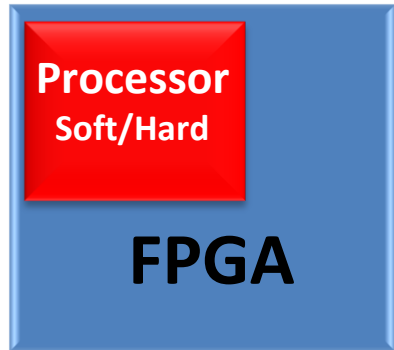
Only one current company
MENTA

(RIP: ~Death year)

Key perspectives for eFPGAs in System

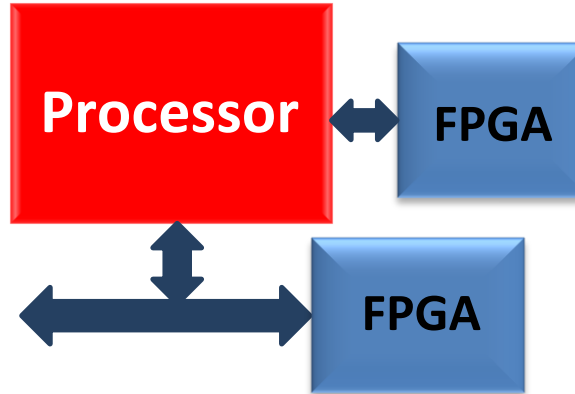
from FPGA/eFPGA survey & visionary industrial survey

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What is right with this one?
(Well known success)

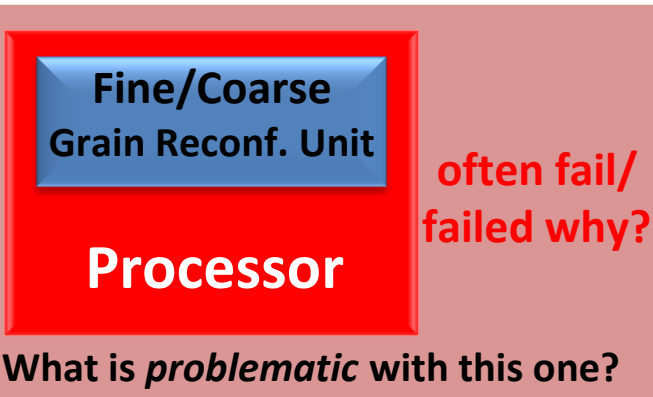
VS



What is better with this one?
(example: Servers, MCUs, Intel's Stellarion)
Potentials of eFPGAs (SIP/SoC)

Pros: Similar more independent modal like FPGAs

Cons: More cycle waste in communication



often fail/failed why?

Pros: Best Performance

Cons: Which Processor???

-Processor/SoC vendor, end customer ok with it?

-Programming challenge?

-Who is end provider?

End result: often Chaos



Key research motivations for eFPGA

from FPGA/eFPGA survey & visionary industrial survey

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FPGA-like Architecture

FPGA-like LUT-based conventional instead of coarse grain (wider applications scope)

Standard Programming

RTL Programming

- Exploitation of ESL
- Exploitation of IP-Ecosystem (migrate/reuse)



Soft Implementation

Pure HDL for quick portability and exploitation by SoC on any Fab/Process node

Customization Infrastructure

GUI infrastructure for exploring Architectural innovations (silicon-efficient arch. in terms of Area, Power, Speed)

Outline

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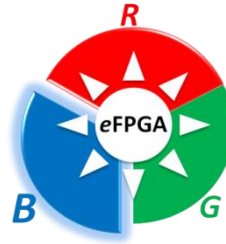
FPGA/eFPGA State of the Art
& Industrial Survey



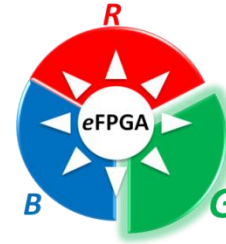
eFPGA
Arch. & CAD



eFPGA
Arch. Exploration



eFPGA
In Systems



Concl. & Future

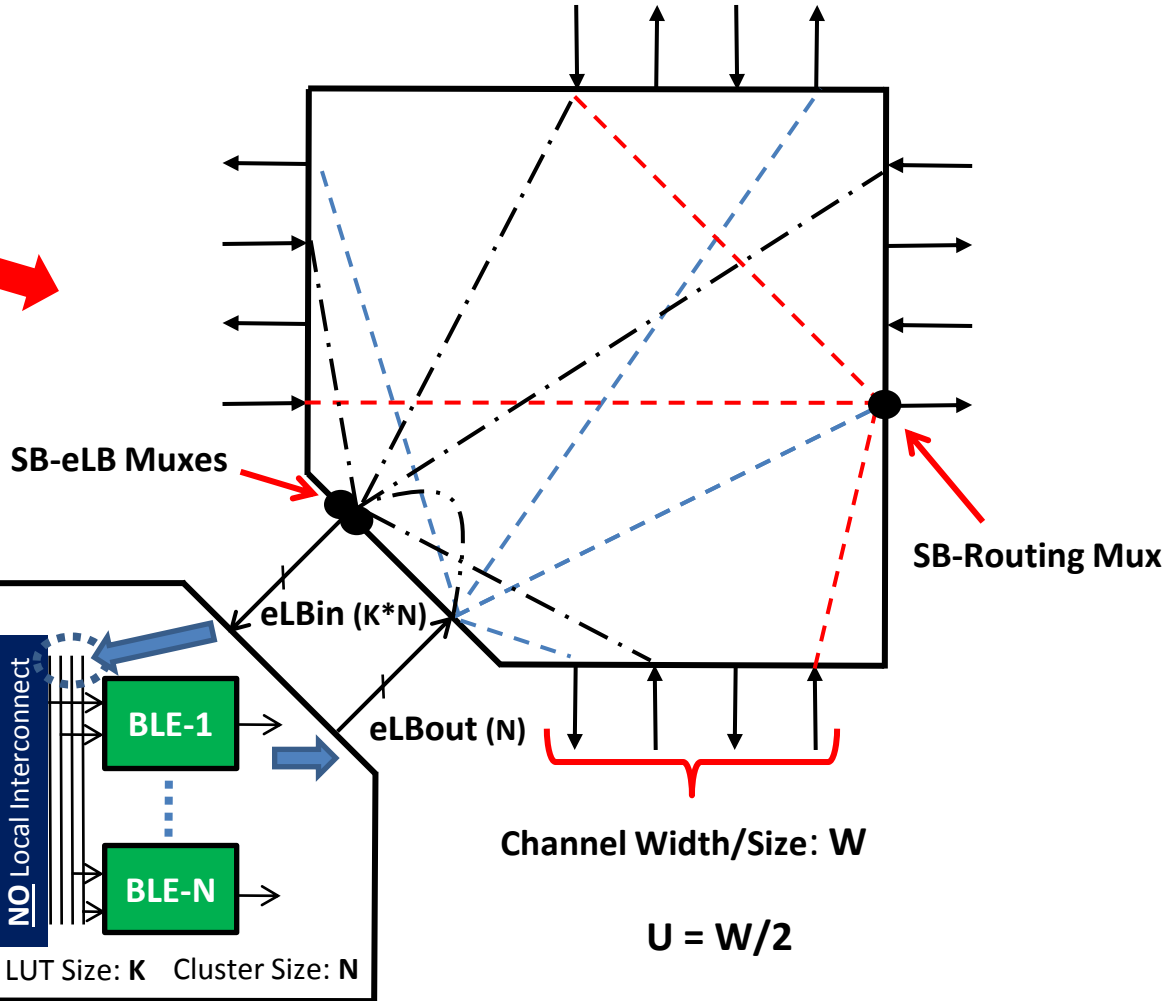
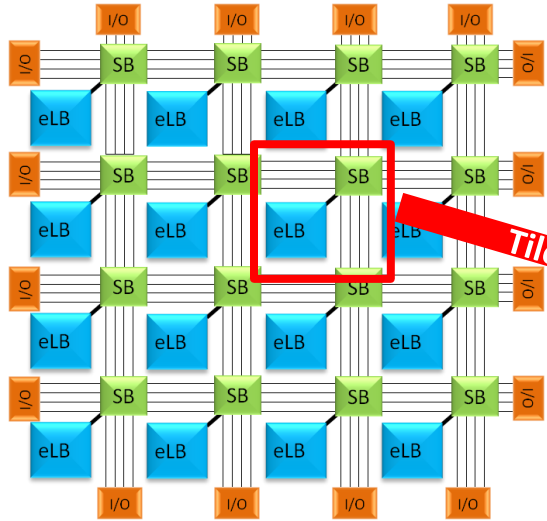


iTalk

- eFPGA Arch. Fundamentals, Differentiations
- eFPGA programming CAD (eFPGA Programmer™)
- eFPGA creation/exploration infrastructure (eFPGA Creator™)

eFPGA Architecture Fundamentals

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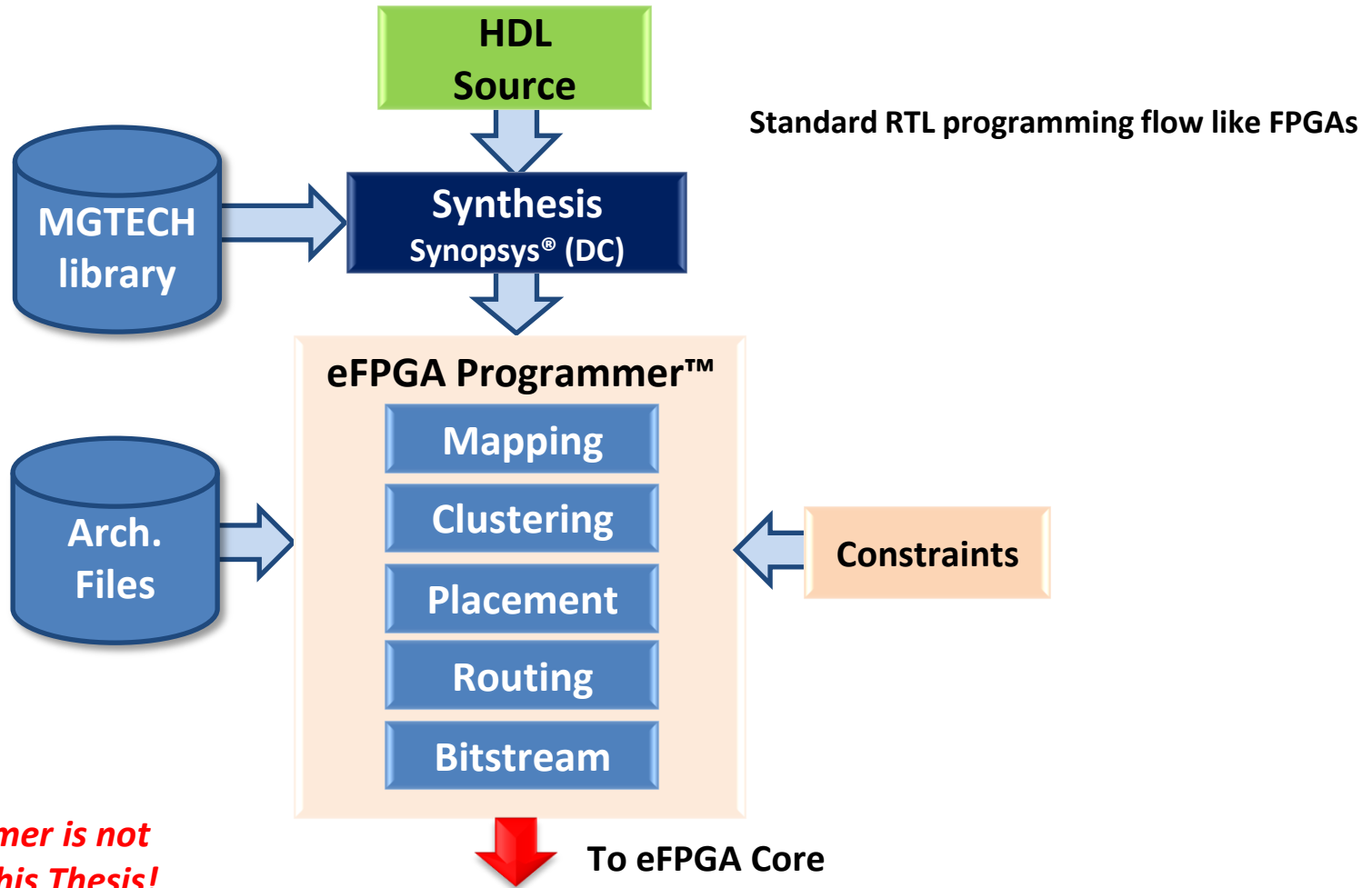


Island-style (2D Mesh) Arch.
Uni-Directional Routing
Unified SB (No Connection Block No classical Local Interconnect)

LUT Size: K Cluster Size: N

eFPGA Programmer™

The programming tools suite of eFPGA

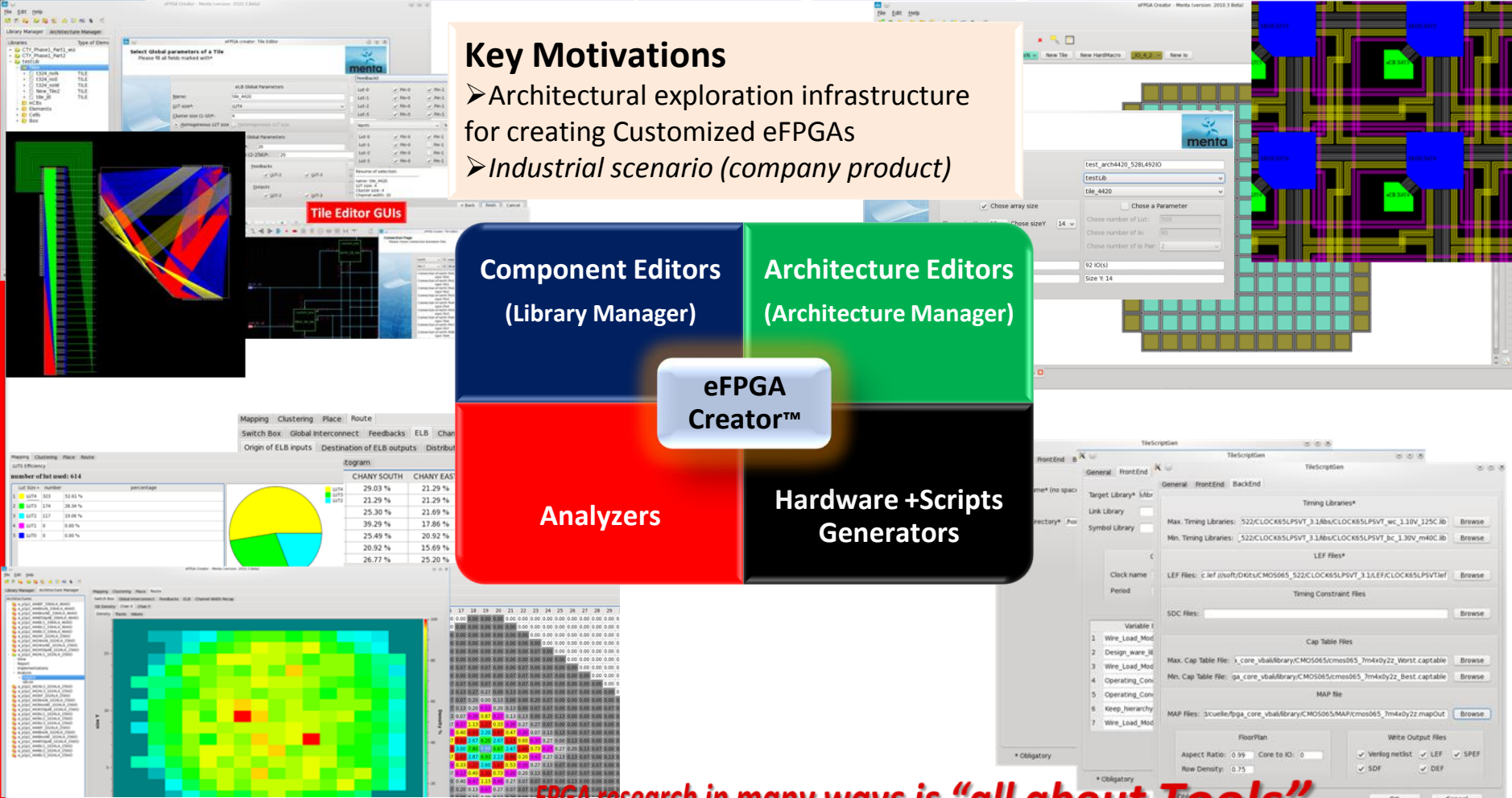


*eFPGA Programmer is not
Contribution of this Thesis!*

eFPGA Creator™ GUI tools suite

some snapshots for general feeling

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Key Motivations

- Architectural exploration infrastructure for creating Customized eFPGAs
- *Industrial scenario (company product)*

Component Editors
(Library Manager)

Architecture Editors
(Architecture Manager)

eFPGA
Creator™

Analzers

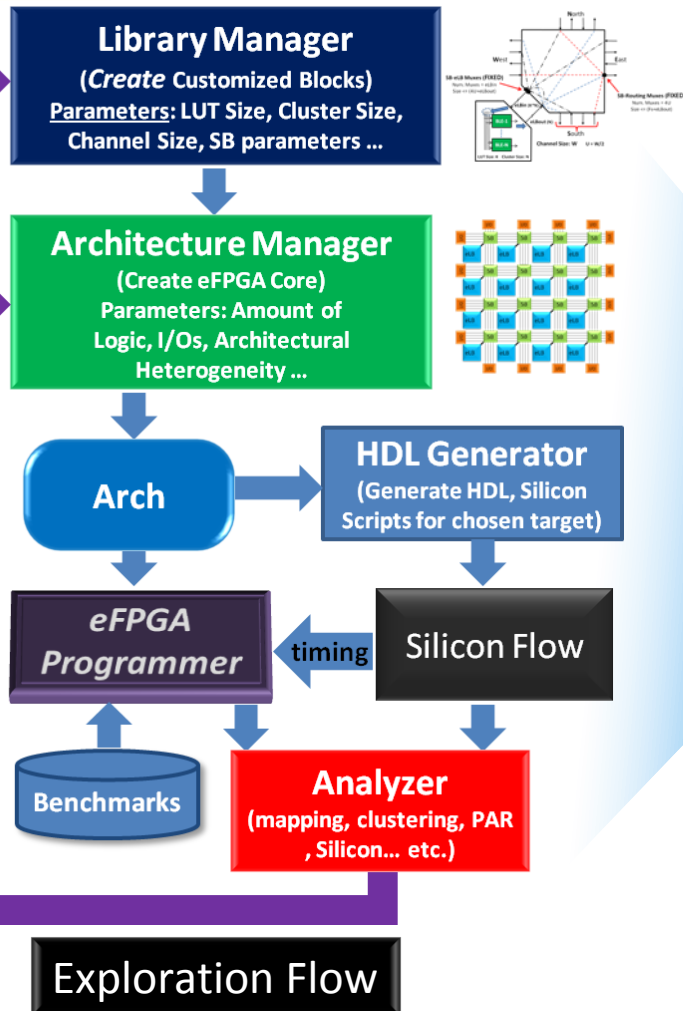
Hardware +Scripts
Generators

FPGA research in many ways is "all about Tools"

eFPGA Creator™

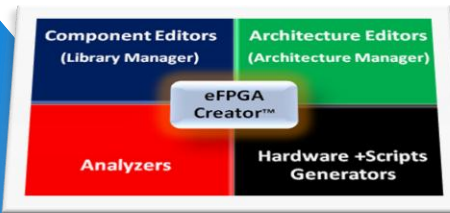
eFPGA architectural exploration/creation GUI tools suite

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Key Differentiations

- Enhanced what-if exploration ease compared to some previous works (e.g VPR)
- Advanced GUI (Qt-based) infrastructure



Key Contributions of this thesis

- General motivations in industrial scenario
- Components customization systems
- Hardware generation system
- Analyzers infrastructure for architectural exploration
- Product marketing ☺

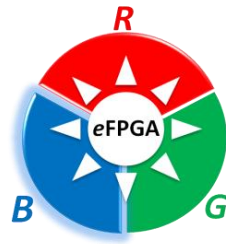
Outline

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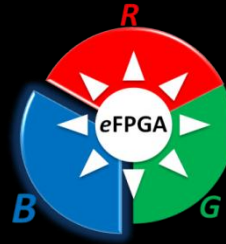
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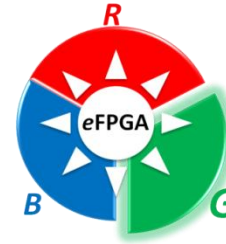
eFPGA
Arch. & CAD



eFPGA
Arch. Exploration



eFPGA
In Systems



Concl. & Future



iTalk

Phase-1: Pre-eFPGA Creator

Basic explorations

LUT size, Cluster size, Channels sizes etc.

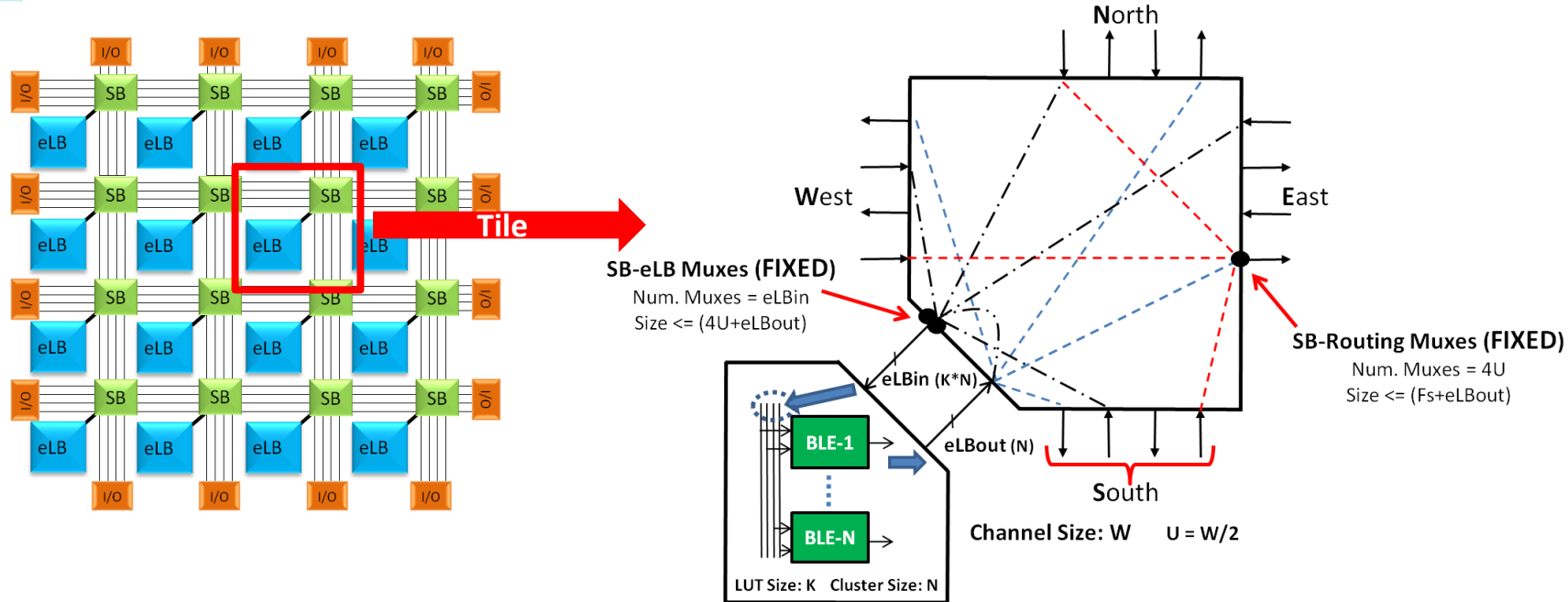
Phase-2: Post-eFPGA Creator

Advanced Customizations

Switch block Depopulation (SB-R & SB-eLB)

Phase-1

eFPGA Architectural Exploration (General)



Key Objectives

Architectural Analysis

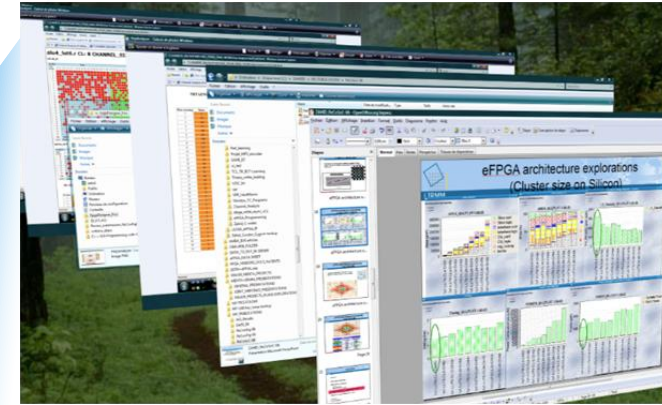
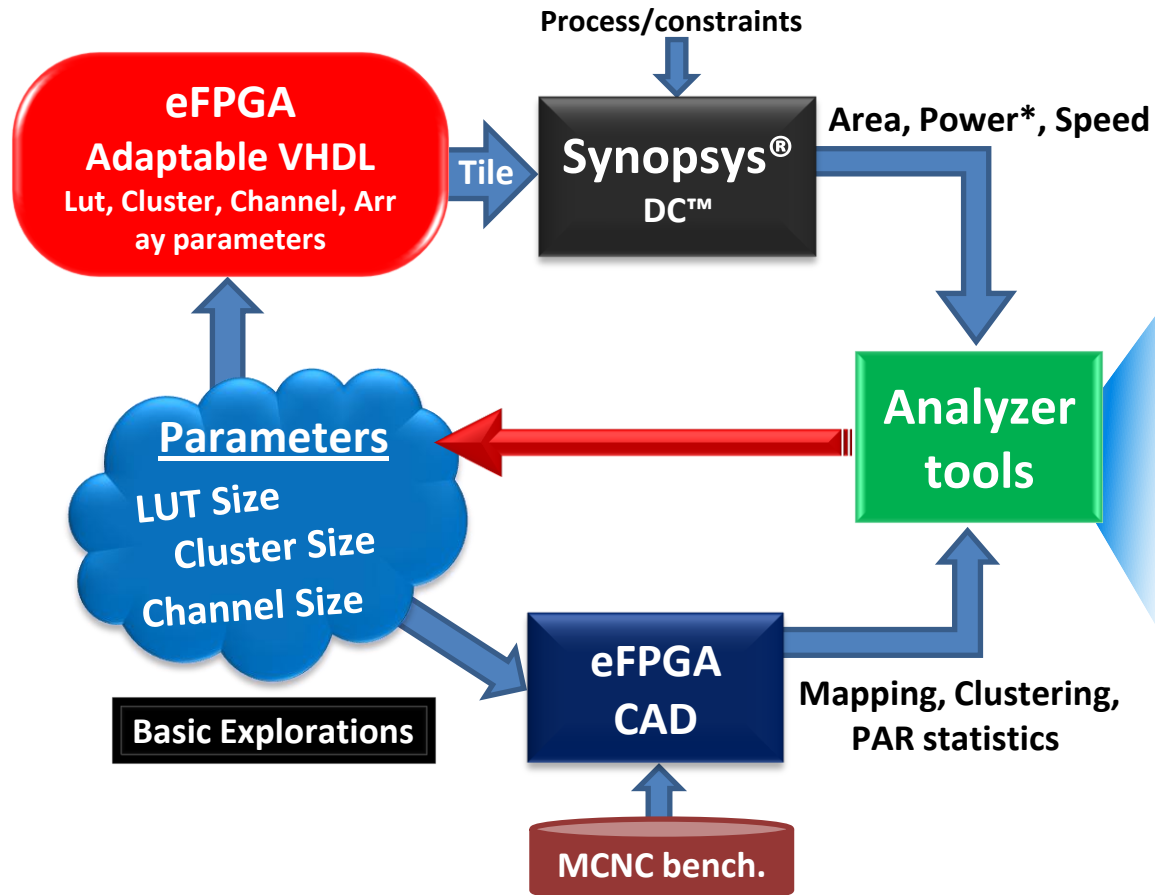
- LUT size/mapping
- Clustering
- Channel width
- Routing (Hop)
- Channel packing
- SB traffic

Silicon Analysis (90, 65, 45nm)

- Area, Area distribution of fundamental elements (LUT, Conf., SB, buffering...)
- Power (Static & Pessimistic Dynamic)
- Basic Timing

Phase-1

Experimentation Methodology



Phase-1

Key Findings

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Most of Phase-1 Results Published in detail in ReCoSoC'08

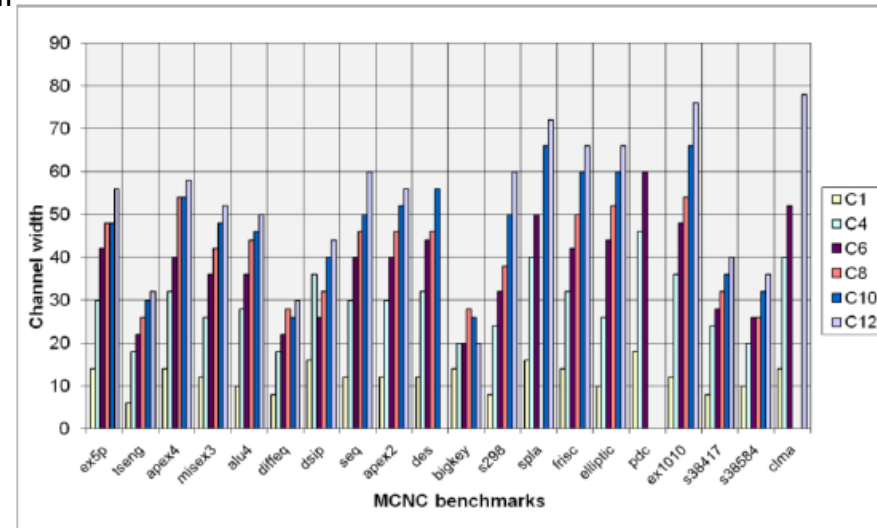
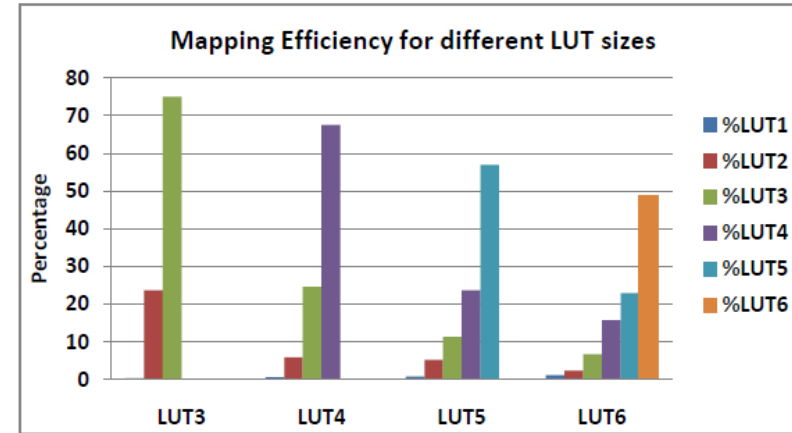
LUT size: Bigger LUTs have poor mapping efficiency

Cluster & Channel size: Channel size demand does not grow in same proportion as cluster size

Routing Challenges: Highly fluctuating channel size requirements of applications (perspectives for beyond classical routing)

Routing HOP: Importance of Heterogeneous routing tracks (long/diagonal wires)

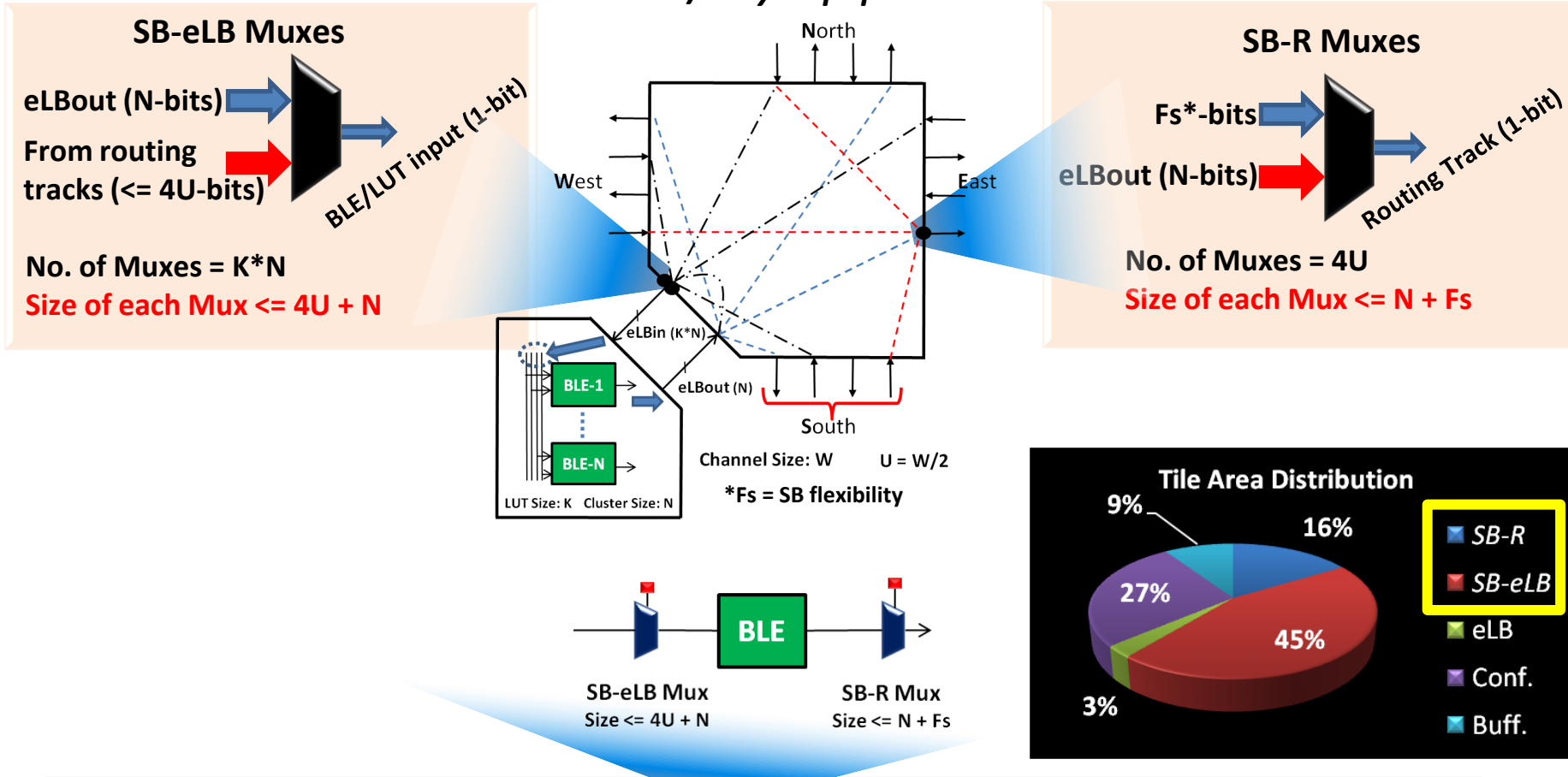
Power vs Speed in beyond 90nm: Effect of threshold voltage on static power and speed



Phase-2

Switch Block Multiplexers Depopulation

What/Why Depopulation?



Key Objective: Reduce SIZE of SB-eLB & SB-R Muxes while maintaining good routing efficiency

Phase-2

Switch Block Multiplexers Depopulation (Methodology)

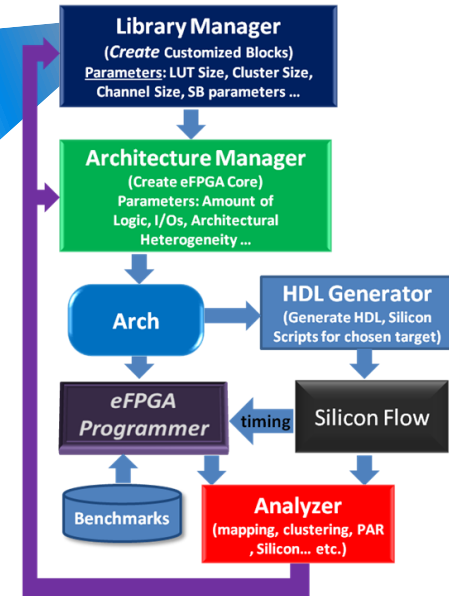
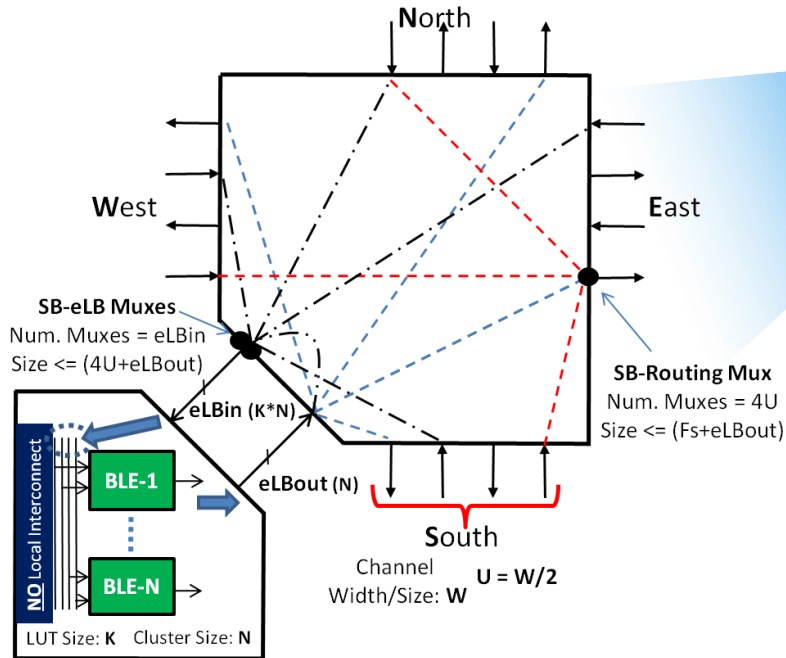
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Fixed Parameters

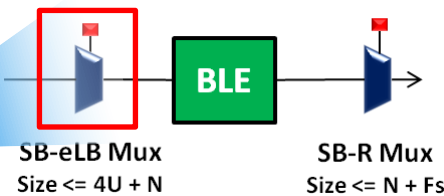
LUT size (K) = 4

Cluster size (N) = 4

Channel size (W) = 48



Only this one will be presented

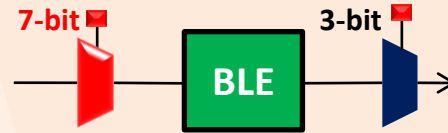
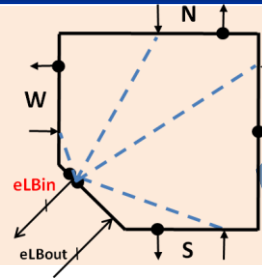


Phase-2

SB-eLB Explorations

Base Case (High Flexibility)

Base



SB-eLB Mux

Size = $4U + eLBout = 100\text{-bit}$

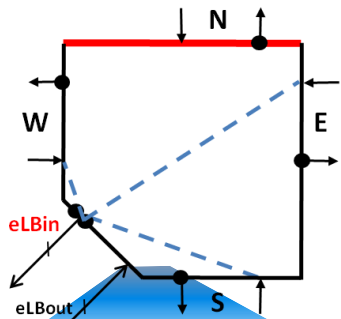
SB-R Mux (FIXED)

Size = $eLBout + Fs = 7\text{-bit}$

STRATEGY-1 : Ports Clipping

Case-1

N Port Cut



SB-eLB

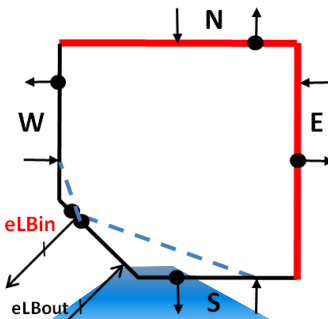
SB-R (FIXED)

$3U + eLBout = 76\text{-bit}$

$eLBout + Fs = 7\text{-bit}$

Case-2

N+E Port Cut



SB-eLB

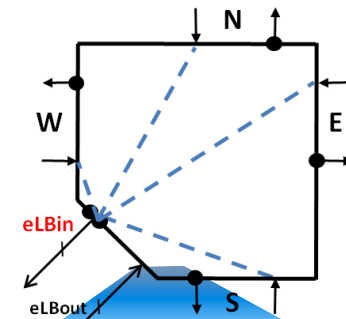
SB-R (FIXED)

$2U + eLBout = 52\text{-bit}$

$eLBout + Fs = 7\text{-bit}$

Case-3

50% of all NSEW Ports Cut



SB-eLB

SB-R (FIXED)

$2U + eLBout = 52\text{-bit}$

$eLBout + Fs = 7\text{-bit}$

Phase-2

SB-eLB Explorations

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STRATEGY-2 : Complex Patterns

Case-1

DIVERSITY

For all BLEs in cluster

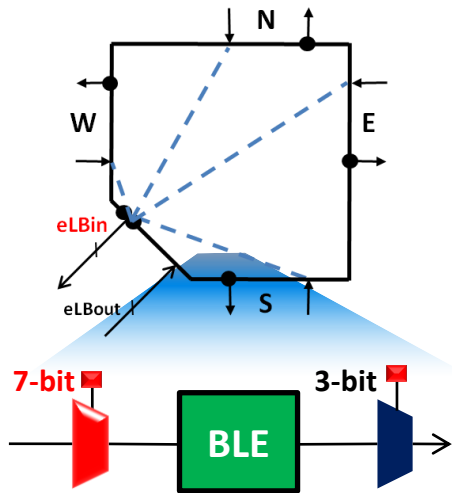
Tracks from all (NSEW)

$In_0 \leftarrow \text{tracks}\{0 \text{ to } (U/4)-1\} + eLBout$

$In_1 \leftarrow \text{tracks}\{(U/4) \text{ to } (U/2)-1\} + eLBout$

$In_2 \leftarrow \text{tracks}\{(U/2) \text{ to } (3U/4)-1\} + eLBout$

$In_3 \leftarrow \text{tracks}\{(3U/4) \text{ to } U-1\} + eLBout$



SB-eLB

SB-R (FIXED)

$U+eLBout = 28\text{-bit}$

$eLBout + Fs = 7\text{-bit}$

Case-2

DIVERSITY+

For all BLEs in cluster

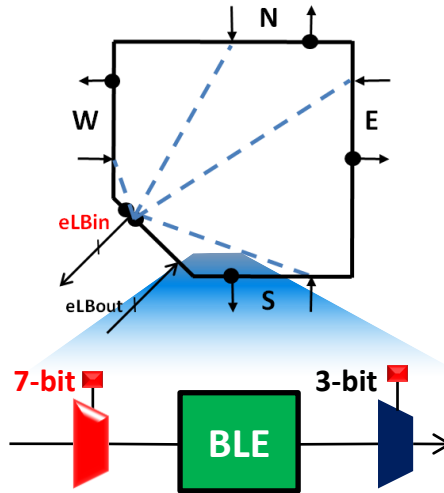
Tracks from all (NSEW)

$In_0 \leftarrow \text{tracks}\{(0+4t), \text{ for } t \text{ to } (U/4)-1\} + eLBout$

$In_1 \leftarrow \text{tracks}\{(1+4t), \text{ for } t \text{ to } (U/4)-1\} + eLBout$

$In_2 \leftarrow \text{tracks}\{(2+4t), \text{ for } t \text{ to } (U/4)-1\} + eLBout$

$In_3 \leftarrow \text{tracks}\{(3+4t), \text{ for } t \text{ to } (U/4)-1\} + eLBout$



SB-eLB

SB-R (FIXED)

$U+eLBout = 28\text{-bit}$

$eLBout + Fs = 7\text{-bit}$

Case-3

VPR-like

One Port per pin

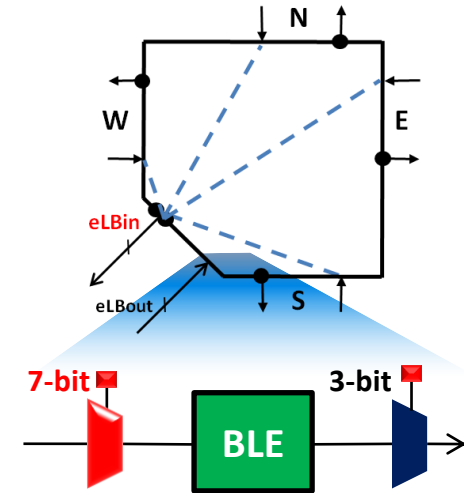
For all BLEs in cluster

$In_0 \leftarrow \text{tracks}\{\text{all } W \text{ port}\} + eLBout$

$In_1 \leftarrow \text{tracks}\{\text{all } N \text{ port}\} + eLBout$

$In_2 \leftarrow \text{tracks}\{\text{all } E \text{ port}\} + eLBout$

$In_3 \leftarrow \text{tracks}\{\text{all } S \text{ port}\} + eLBout$



SB-eLB

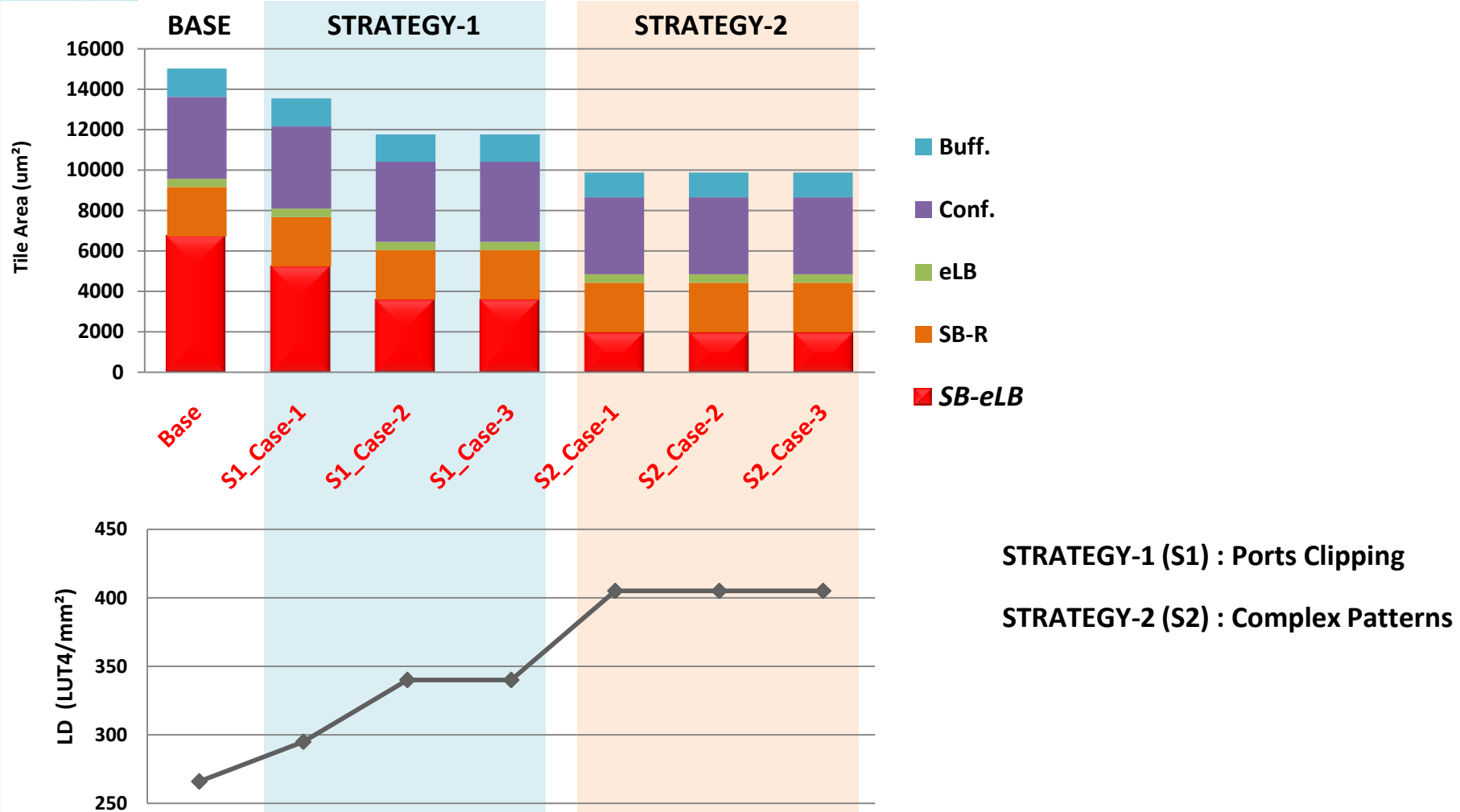
SB-R (FIXED)

$U+eLBout = 28\text{-bit}$

$eLBout + Fs = 7\text{-bit}$

Phase-2

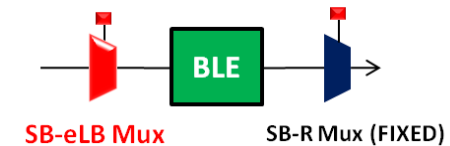
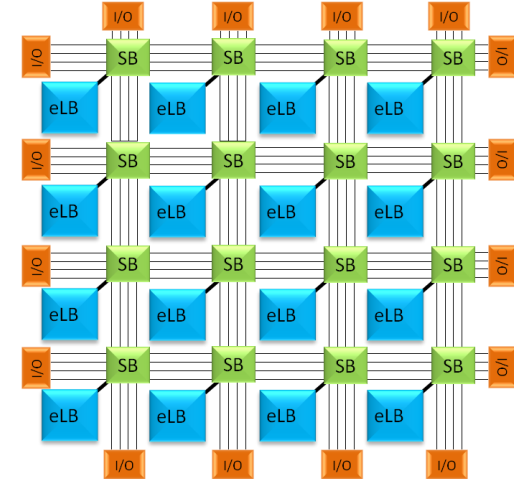
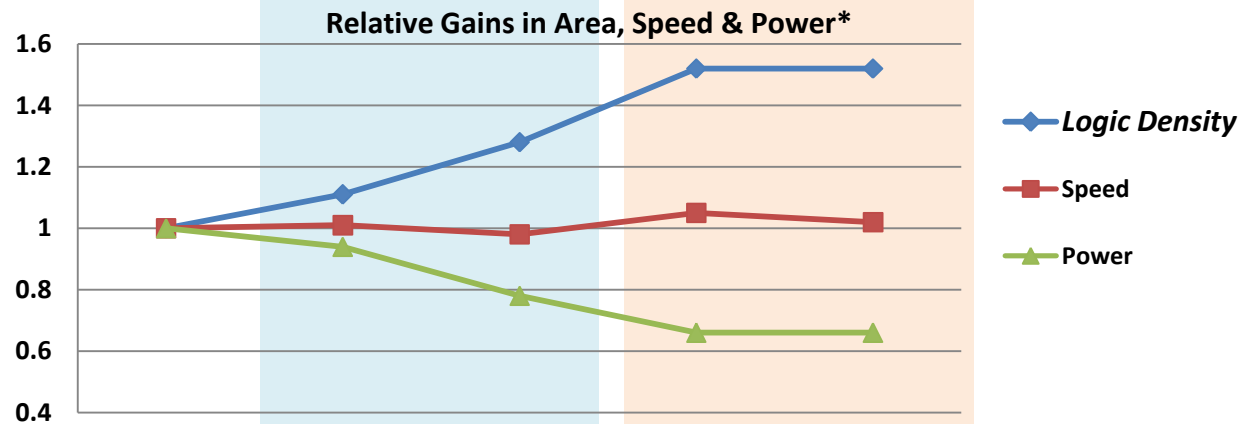
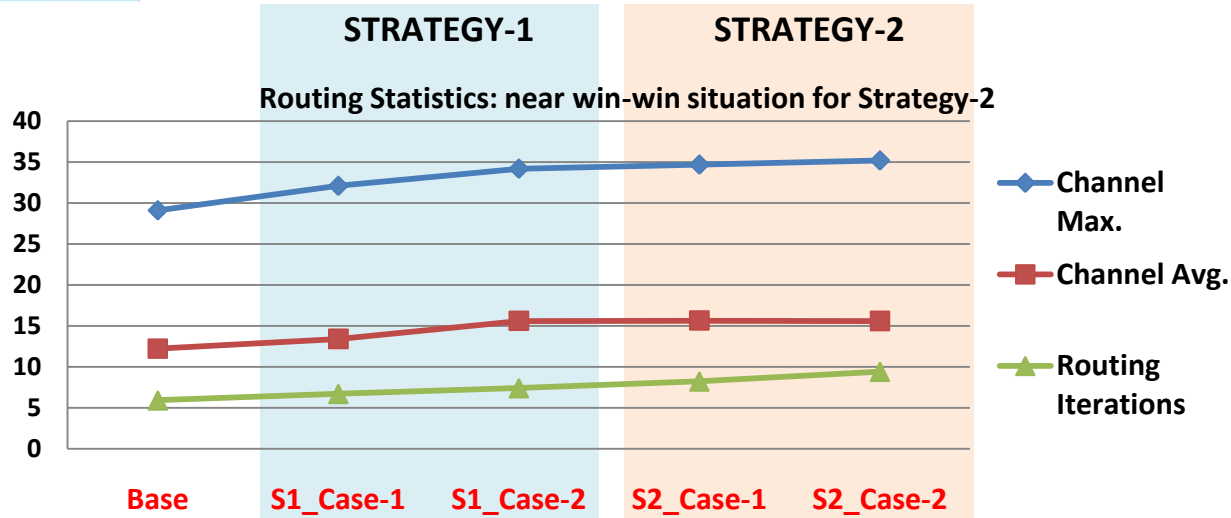
SB-eLB explorations: Silicon Statistics (ST 65nm LP)



Phase-2

SB-eLB explorations: Tradeoffs

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STRATEGY-1 (S1) : Ports Clipping

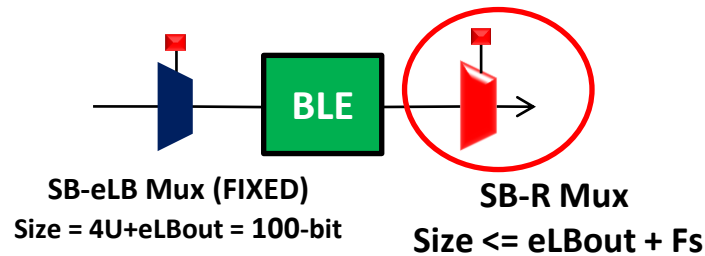
STRATEGY-2 (S2) : Complex Patterns

Phase-2

SB-R Explorations

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In a similar fashion like SB-eLB, SB-R Muxes Explored in Detail



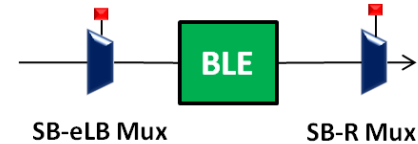
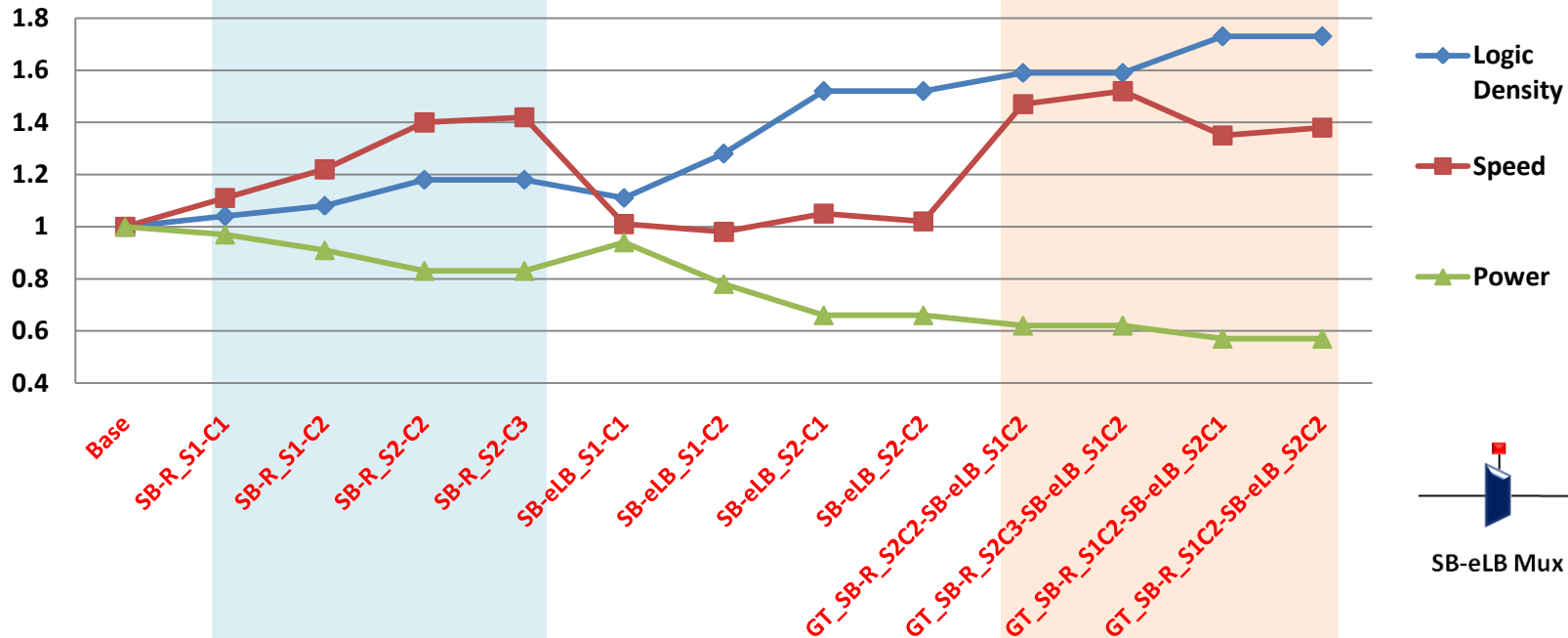
RESULT: ~1.2X AREA Improvement & **~1.45X SPEED** Improvement

Phase-2

Detailed exploration Saga and finding of Golden Tiles

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Relative Gains in Area, Speed & Power *



BASE

SB-R Exploration
Good for Speed

SB-eLB Exploration
Good for Area

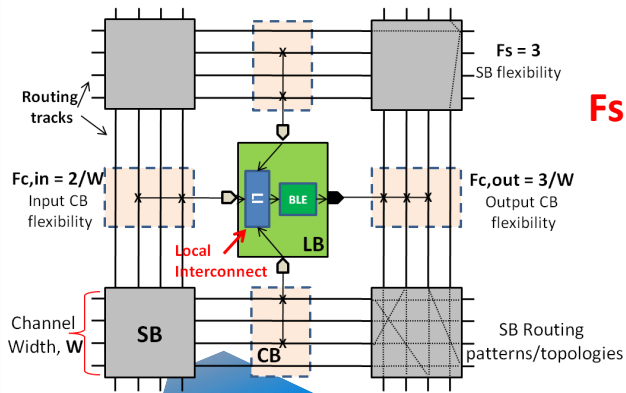
GOLDEN TILES
Exploration of Mix of
best of
SB-R & SB-eLB

STRATEGY-1 (S1) :
Ports Clipping

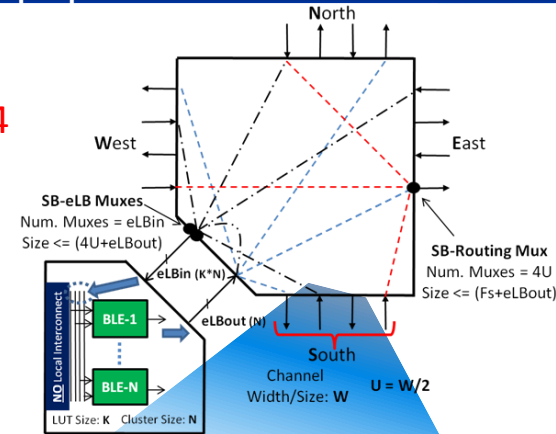
STRATEGY-2 (S2) :
Complex Patterns

Phase-2

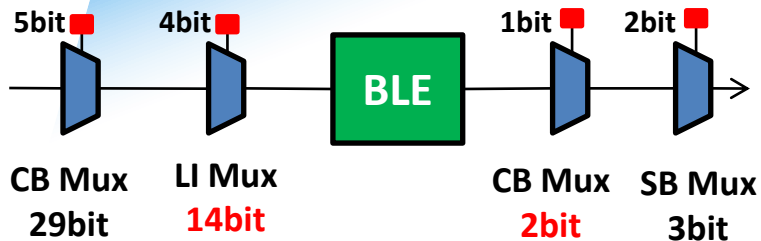
What achieved with SB-R & SB-eLB multiplexers depopulation



$F_s = 3$, K (LUT size) = 4, N (Cluster size) = 4
 W (Channel size) = 48, U ($W/2$) = 24

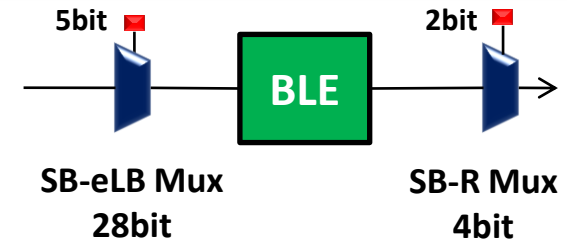


V. Betz & J. Rose VPR Arch ~1997 (Toronto Univ.)
 Widely explored arch. in academics (still is)



Equiv. Soft VPR arch. replica according to published* results:
 $F_c, in = 0.6W$, $F_c, out = W/N$ {combined?}

Unified SB with diverse eLB connections



eFPGA SB-R, SB-eLB best results found
 SB-eLB = $U + N$, SB-R = $F_s + 1$ {separately}

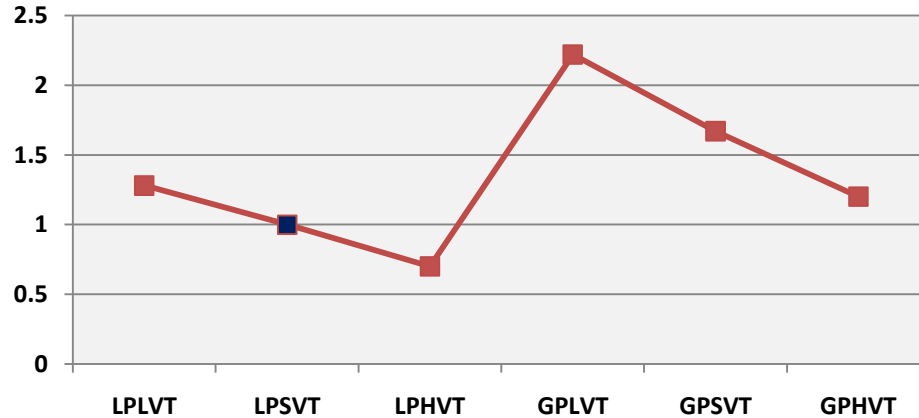
*A. Marquardt, V. Betz and J. Rose, "Speed and Area Tradeoffs in Cluster-Based FPGA Architectures", IEEE Transactions on VLSI Systems, February 2000

Phase-2

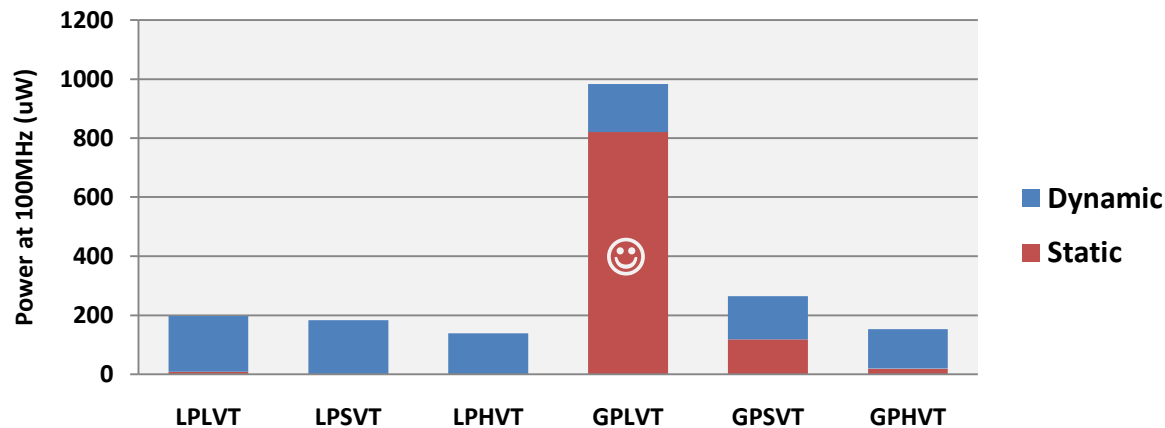
Power vs Speed: Effect of Threshold Voltage and Process type (ST 65nm)

28

Relative Speedup for benchmarks on 65nm process types



Multiple Electrical Implementations
of same Logical Architecture



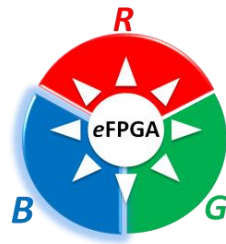
Outline

29

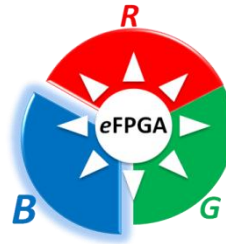
FPGA/eFPGA State of the Art
& Industrial Survey



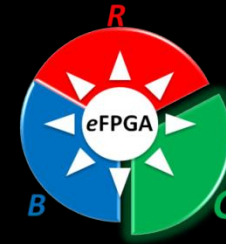
eFPGA
Arch. & CAD



eFPGA
Arch. Exploration



eFPGA
In Systems



Concl. & Future

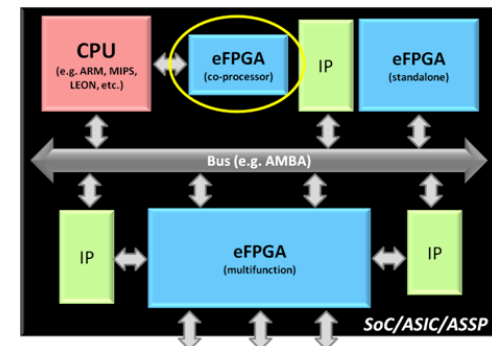


iTalk

Ok Now we got eFPGA, what to do with it!

➤ Reconf. Acceleration Experiments (Usual Suspect 😊)

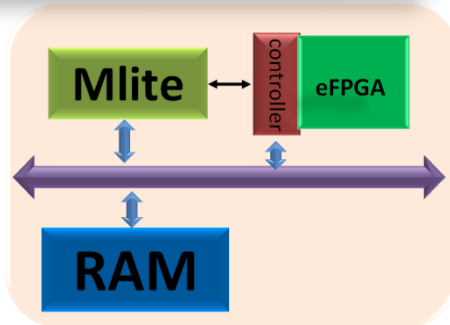
➤ Beyond Classics (MRAMs) case study, Test Chips!



Reconfigurable Acceleration

30

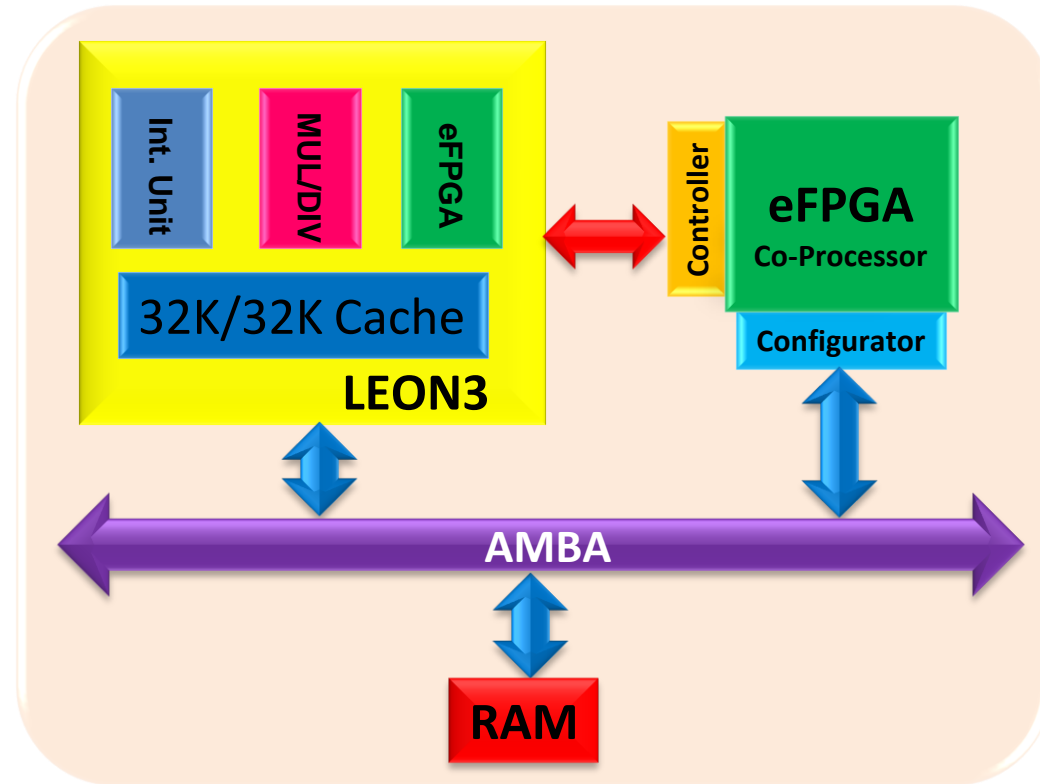
Phase-1 eFPGA used for experiments
LUT-6, Cluster-4, Channel-32



Step-1: eFPGA with Mlite processor
Published in [ReConFig-2008](#)

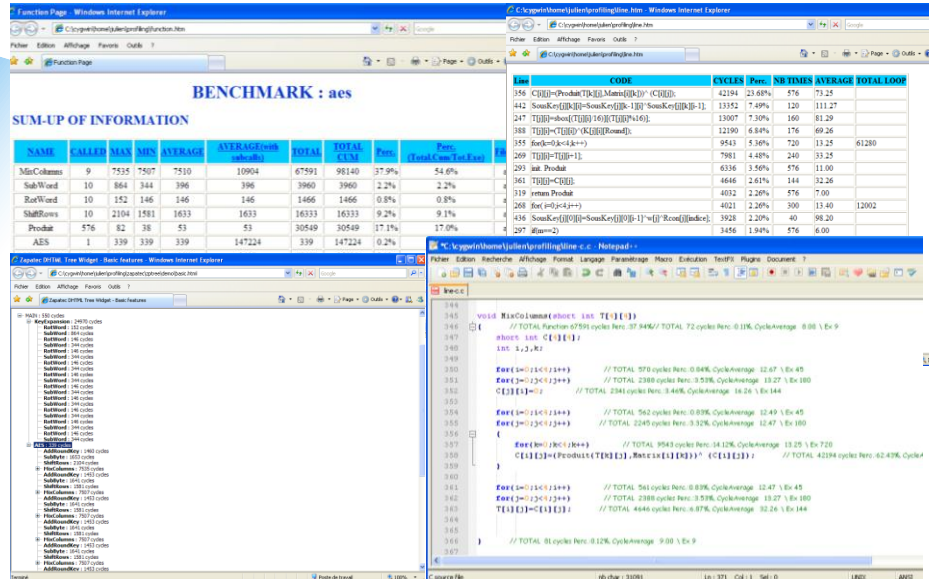
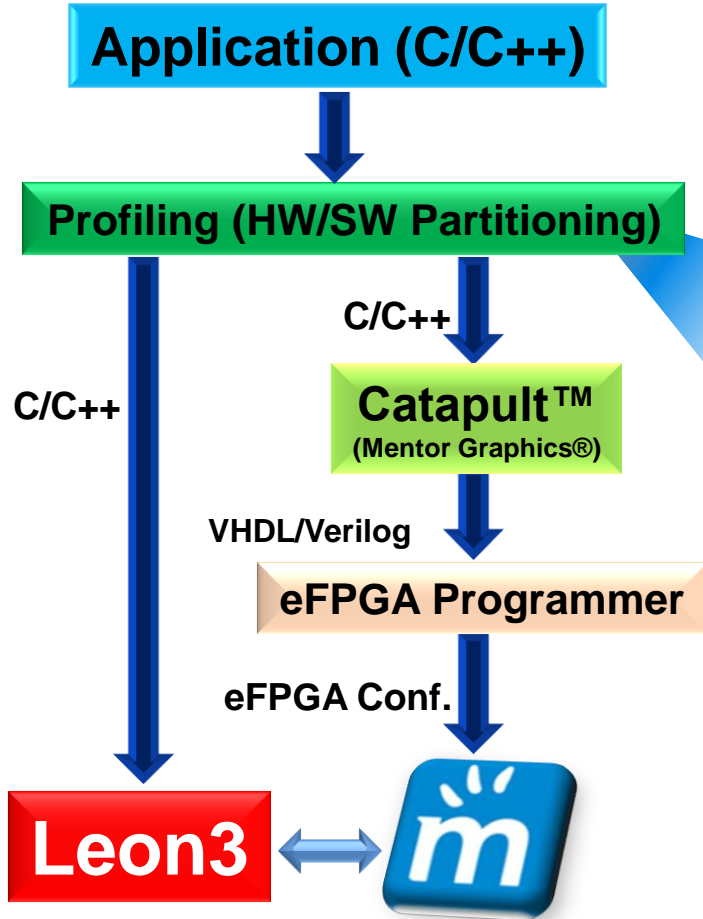
Key differentiation compared to some previous works

- ❖ Conventional FPGA-like eFPGA
- ❖ Standard RTL flow
- ❖ ESL exploitation perspectives (HW/SW co-design ease)
- ❖ Silicon tradeoffs visualization (not just speedup X-factor!)



Step-2: eFPGA with LEON3 (Co-processor & Functional Unit)
Published in [DATE-2009](#)
Only this one will be presented

Experimentation Flow



Application Analysis

AES & DES applications

- Bit level operations
- Suitable for analyzing bit level random logic mapping ability of LUTs of eFPGA
- **AES is explained**

Function name	Called	% of execution
main	1	100.0%
AES	1	81.9%
MixColumns	9	54.6%
Product	576	17.0%
KeyExpansion	1	16.9%
SubByte	10	9.1%
ShiftRows	10	9.1%
AddRoundKey	11	8.9%
SubWord	10	2.2%
RotWord	10	0.8%

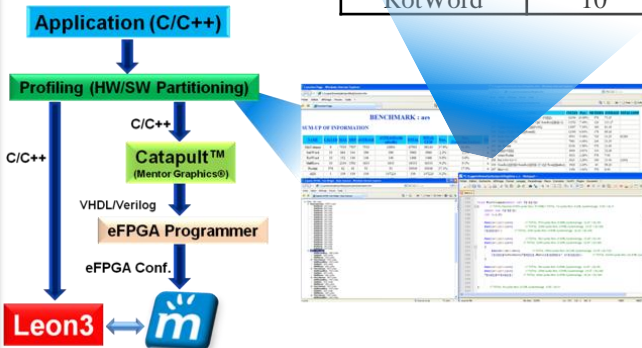
```

void MixColumns(short int T[4][4])
{
    short int C[4][4];
    int i,j,k;

    for(i=0;i<4;i++)
        for(j=0;j<4;j++)
            C[i][j]=0;

    for(i=0;i<4;i++)
    {
        for(j=0;j<4;j++)
        {
            for(k=0;k<4;k++)
            {
                C[i][j]=
                (Product(T[k][j],Matrix[i][k]))^ (C[i][j]);
            }
        }
    }
    for(i=0;i<4;i++)
        for(j=0;j<4;j++)
            T[i][j]=C[i][j];
}

```



HW-SW Partitioning

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```

void MixColumns(short int T[4][4])
{
    short int C[4][4];
    int i, j, k;

    for(i=0; i<4; i++)
        for(j=0; j<4; j++)
            C[i][j]=0;

    for(i=0; i<4; i++)
    {
        for(j=0; j<4; j++)
        {
            for(k=0; k<4; k++)
            {
                Product(T[k][j], Matrix[i][k])
                C[i][j]=
                ( C[i][j] + C[i][k] * T[k][j] );
            }
        }
    }
    for(i=0; i<4; i++)
        for(j=0; j<4; j++)
            T[i][j]=C[i][j];
}

```

Step-4

Step-3

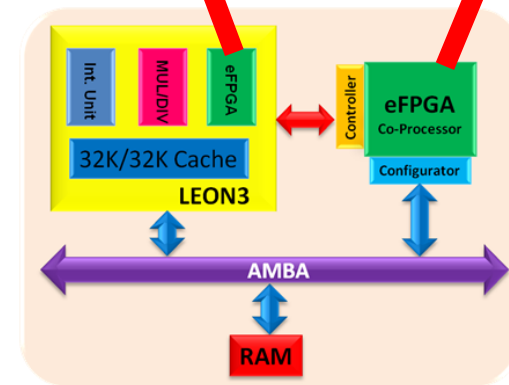
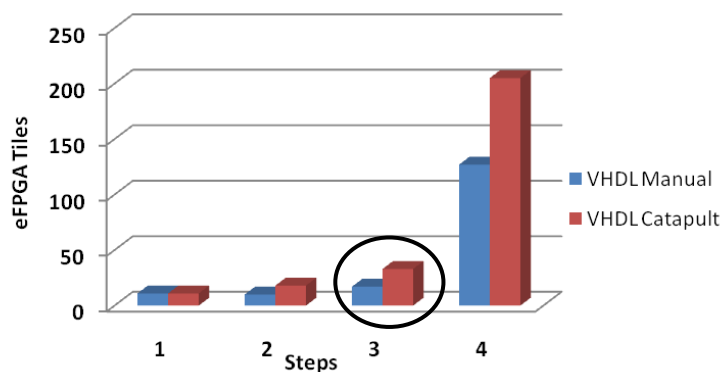
Step-1

Step-2

Why Gains so similar for both cases ?

Pure Soft 40358 (Cycles)	Pipeline eFPGA (Cycles)	Gain X Times	Co-Processor eFPGA (Cycles)	Gain X Times
STEP-1	30430	1.326	30447	1.325
STEP-2	30722	1.313	30735	1.313
STEP-3	23752	1.699	23767	1.698
STEP-4	16244	2.484	16265	2.481

Resources: ESL vs Hand Coded HDL



Attention: Approx. Assumption (but based on rough facts!)
LEON and eFPGA operating at same frequency (100MHz)

Silicon Tradeoffs (65nm)

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Analysis on ST 65nm LP CMOS

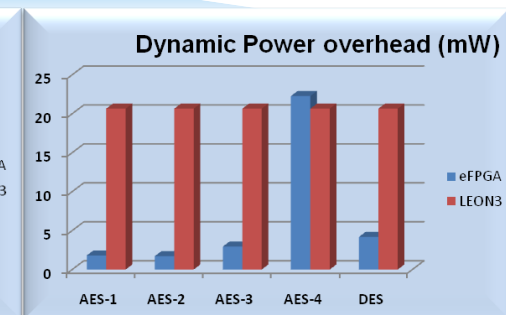
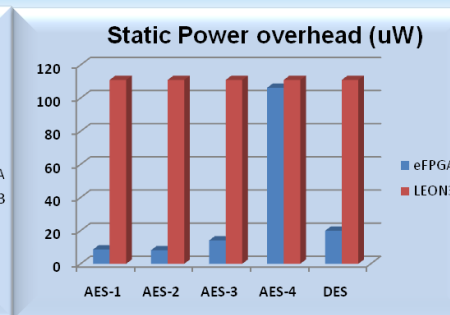
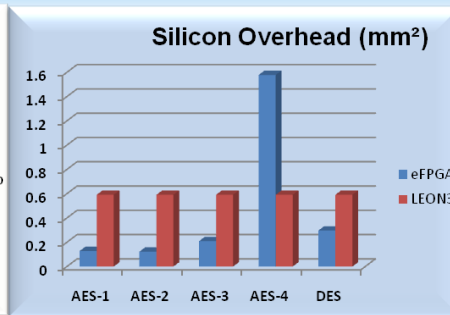
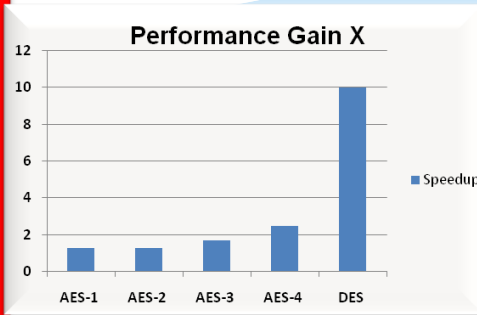
Area and power of LEON3 (Core+Cache)

65nm LP	Area (mm ²)	Static Power 25°C (uW)	Dynamic Power 100MHz (mW)
Core (LPLVT)	0.191	85.3	5.75
32K/32K Cache(LPSVT)	0.4	25.63	14.9
Total	0.591	110.93	20.65

Pessimistic power of eFPGA (484 LUT6)
assuming all inputs of TILES toggling

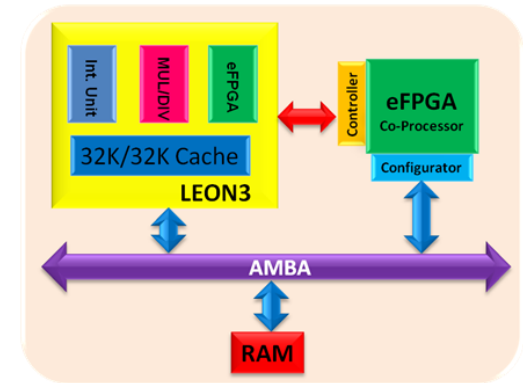
65nm LP process	LVT	SVT	HVT
Static Power (mW)	1.27	0.105	0.011
DP(mW) @ (Tr-0.25,Stp-0.25)	23	22	25
DP(mW) @ (Tr-0.50,Stp-0.5)	47.6	46.6	53.8
DP(mW) @ (Tr-1.0,Stp-0.50)	95.36	93.36	107.8

What will reconfg. acceleration luxury cost!



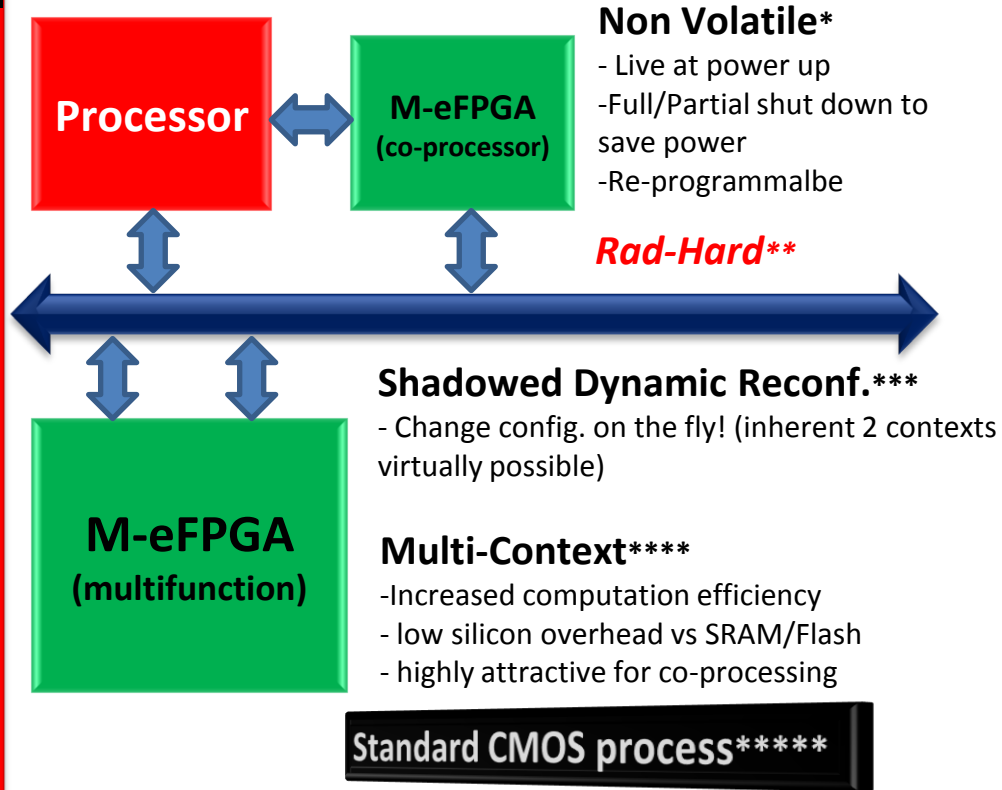
Key Findings from Reconf. Acceleration experiments

- Importance of Silicon Gap
- ESL vs Hand coded RTL
- Functional unit vs Co-Processor

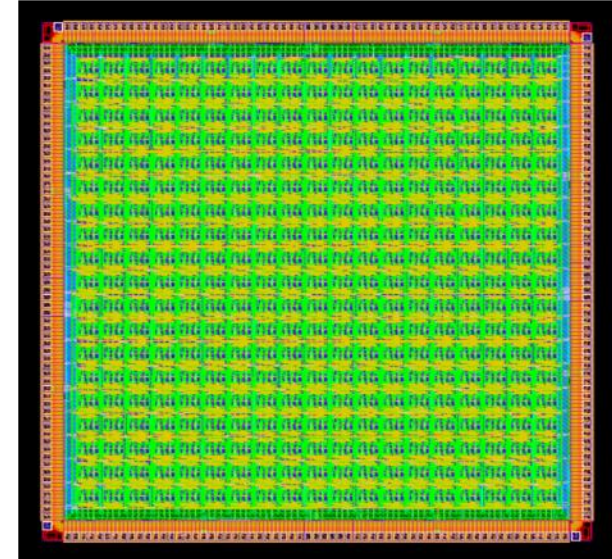


MRAMs

like a dream come true for embedded Computing



World's First MRAM-based FPGA!



Die = 20mm²; Core = 15.64mm²

ST 130nm CMOS + CROCUS 120nm MRAM

1444 LUT4

Arch.: LUT-4, Cluster-4, Channel-16

Chief Competitors of MRAMs
 FRAM (TI is focused)
 PCM (Samsung is focused)

<http://www.eetimes.com/electronics-news/4084935/Updated-Researchers-present-MRAM-based-FPGA-architecture>

<http://www.eetimes.com/electronics-products/other/4200035/First-MRAM-based-FPGA-taped-out>

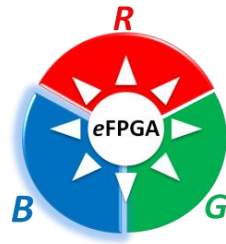
Outline

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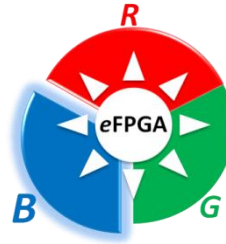
FPGA/eFPGA State of the Art
& Industrial Survey



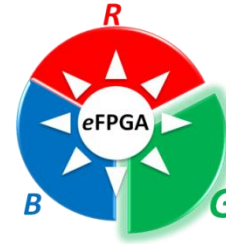
eFPGA
Arch. & CAD



eFPGA
Arch. Exploration



eFPGA
In Systems



Concl. & Future



iTalk

Conclusions & Future

- Importance of Standards in Industry
- Importance and potentials of FPGA-like eFPGAs
- CAD tools Infrastructure for architectural exploration of eFPGAs
- Silicon-efficient soft eFPGAs
 - Innovative architectures with Logic Block connected in diverse depopulated styles to Unified Switch Block
 - Soft eFPGAs with Up to 400+ LUT4/mm² at 65nm were achieved
- eFPGAs have strong potentials for embedded Reconfigurable computing
- Perspectives of emerging technologies for FPGAs/eFPGAs
 - Need to think for beyond classical routing arch. and configuration memories
 - MRAMs have interesting properties for Future FPGAs/eFPGAs
- eFPGAs are key to Future Heterogeneous MPSoC Platforms

Conclusions & Future

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Near Term

Architecture

- Further enhancement of silicon efficiency (depopulation)
- Long wires
- Heterogeneity (general purpose + application specific)
- Enhanced CAD and tools

Mid Term

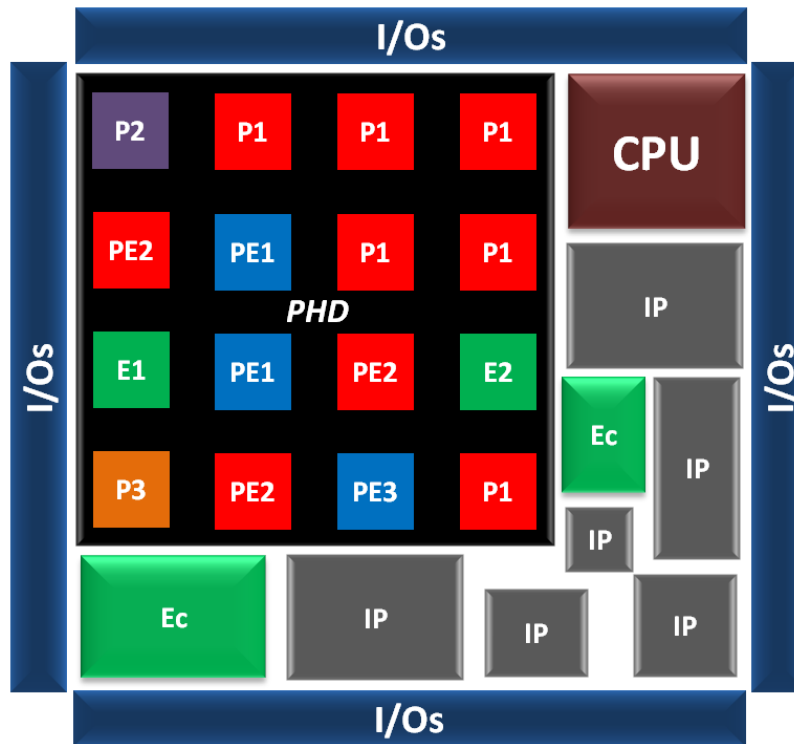
System

- Integration using Industry Standards
- System level experiments + arch. enhancements

Conclusions & Future

Long term future perspectives

We are not too far from them Industrially & Academically!
(eFPGAs are key)



Heterogeneous Reconfigurable MPSoCs

Future SoCs Will have 3 Domains

1- GPD (General Purpose Domain)

Large single/multi core CPU (Big Boss!)

2- ASD (Application Specific Domain)

Specialized IPs

(memories, graphics, analog/mixed, interface , eFPGAs etc.)

3- PHD (Programmable Hybrid Domain 😊)

Heterogeneous processing elements with NoC based interconnectivity

Description of Elements

Px: Plurality of Small RISC + Memory

Ex: Plurality of custom eFPGAs (simple, multi-context, heterogeneous, conventional/beyond-classic architecture/configuration etc.)

PEx: Px with Ex co-processor

Ec: Conventional eFPGA (can have beyond-classic configuration)

Major PhD Contributions

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Industrial Panels

- **IP'08** : “SoC Configurability- Balancing Manufacturing and R/D Costs”. With Gartner, ARM, ST, MIPS, Transmeta and Menta.
- **IP'07** : “IP/SoC Prototyping”. With Bull, ST, Mentor Graphics, EVE, Synplicity and Menta

International Conf. Contributions

- **ReConFig'09, ReConFig'10** : PC member Track HPRC
- **IP'08** : Session Chairman (Prototyping 2)

International Publications

- **FPL'10** : S. Z. Ahmed et al, “Survey of new trends in Industry for Programmable hardware: FPGAs, MPPAs, MPSoCs, Structured Asics, eFPGAs and new wave of innovation in FPGAs” (my precious!)
- **ERSA'10** : L. Torres Y. Guillemenet, S. Z. Ahmed, “A Dynamic Reconfigurable MRAM based FPGA”
- **ReConFig'09** : Y. Guillemenet, S. Z. Ahmed et al, "MRAM based eFPGAs: programming and silicon flows, exploration environments, MRAM current state in Industry and its unique potentials for FPGAs"
- **IPESC'09** : S. Z. Ahmed et al, "FPGA Designer GUI Tools Suite: A complete hardware and software infrastructure for creating customizable eFPGA IP blocks of Menta"
- **DATE'09** : S. Z. Ahmed et al, "Exploration of power reduction and performance enhancement in LEON3 processor with ESL reprogrammable eFPGA in processor pipeline and as a co-processor"
- **ReConFig'08** : S. Z. Ahmed et al, "Power consumption reduction explorations in processors by enhancing performance using small ESL reprogrammable eFPGAs"
- **ReCoSoC'08** : S. Z. Ahmed et al, "eFPGA architecture explorations: CAD and Silicon analysis of beyond 90nm technologies to investigate new dimensions of future innovations"

Thanks for watching: hope u enjoyed ??????

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Tough roads ahead, new dawn and decade of The Ring begins
Competitors will quest for *the Precious* to rule



One Ring will rule them all
One Ring will bring them all
One Ring will force them all
and in the next innovations bind them

In the industry of Semiconductor where **30US \$B**
is expected for another decade and **SD** is on the rise

The Ring of **POWER** is our worst enemy and best hope for new innovations

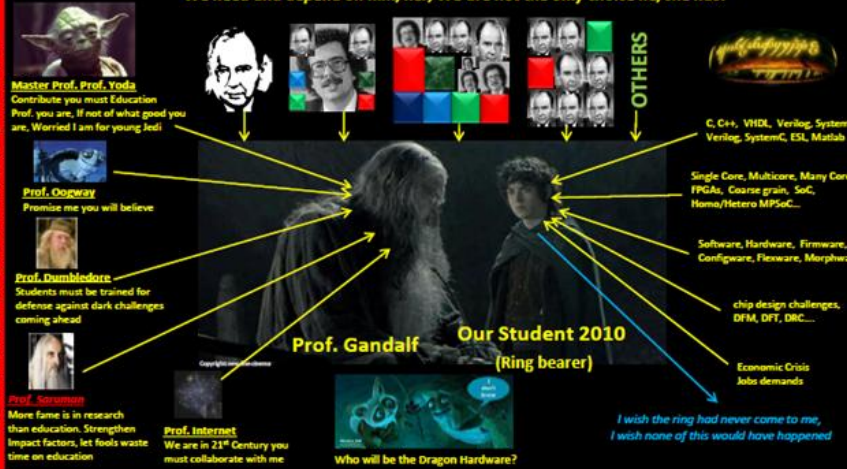


Sadly we lost Freeman and Neumann at their young age! Long will their legacy live in industry & Academics

25

Education Challenge: Our Student is getting Overburdened!

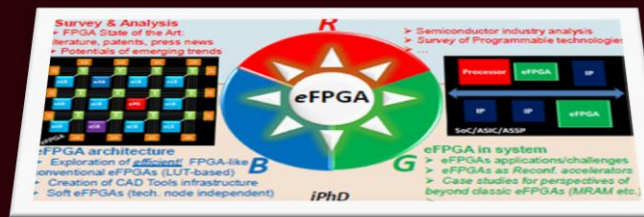
We need the fellowship of Industry and academics to redefine our curriculum
We need and depend on him/her, We are not the only choice he/she has!



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This has dedicated this Slide to Prof. Reiner Hartenstein in inspiration of/from his amazing keynotes and contributions to Education

& now "Return of the **JURY!!**"



The Last act of/as CIFRE (See Epilogue of Thesis draft) Abstracts taken from Industry vs Academics (I/V): the inside story of my PhD

Mentioned in spirit of Industry (grab differentiation) & Academia (we share)

Unbiased Global findings: what I learned/Found/Investigated is

In one embodiment an entity called Semiconductor Industry:

- > We are not primarily doing this for the humanity, it's our business, if we don't do it someone else (competitor) will
- > If one can't control/protect one's market share, he voluntarily enough to foresee future before enemy (needs can/may be created); he ~~will~~ may be dominated, no matter how big/dominant one is (Semiconductor will not take care of itself)
- > There are usually two ways to do business: 1- Have something that no one has, and create dominance of/through that; 2- Find weakness of the enemy, use that as strength and crush him with it
- > Science alone can't/does not run/Wire the industry, it takes TWG (works & holism) to do wonders
- > We protect knowledge (patents), employ/hoard academics, steal ideas, buy ideas, camouflage science for business, even do miracles of science, are often at high risks (market/economy). All is fair in love & war, damn hard we try playing that!

In another embodiment a corresponding* entity called Academia:

- > We love to share, cite and be cited (the heavy & burden of selfless academia)
- > There are two distinct kinds of professors in the world: those who contribute science and those who contribute themselves in the name of science. In real life many of us must have to use a mixture of it for obvious reasons
- > The finest minds of academia (professors) are/made so diversely overloaded that often they don't/can't find fair enough time for what they are/wish/supposed to be overloaded for (homogeneous academia vs heterogeneous industry)
- > RESEARCH paid/downloads business model has gone outdated in/for internet vs Google business model supremacy
- > Only Professors can live happily ever after (beyonds of teaching/learning); it depends on them how happily they enjoy their ever after (the legends not even retire, ever after). No place is more prestigious and safer than the University!

Lords of the Jury

Reviewer

[Mr. Jürgen Becker](#)

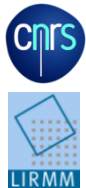
Prof. & Chief Higher Education Officer (CHEO) at KIT
Karlsruhe, GERMANY



Examiner

[Mr. Michael Hübner](#)

Senior Scientist Reconfigurable Technologies at KIT
Karlsruhe, GERMANY



Co-adviser

[Mr. Gilles Sassatelli](#)

Research Director at CNRS
Montpellier FRANCE



President

[Mr. Guy Gogniat](#)

Prof. at UBS
Lorient, FRANCE



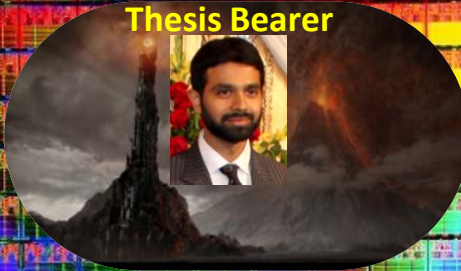
Reviewer

[Mr. Habib Mehrez](#)

Prof. at UPMC
Paris, FRANCE



Thesis Bearer



You
(Public Defense!)



Examiner/co-adviser

[Mr. Laurent Rougé](#)

Founder & CEO Menta
Montpellier, FRANCE



Adviser

[Mr. Lionel Torres](#)

Prof. at UM2/Polytech
Montpellier, FRANCE



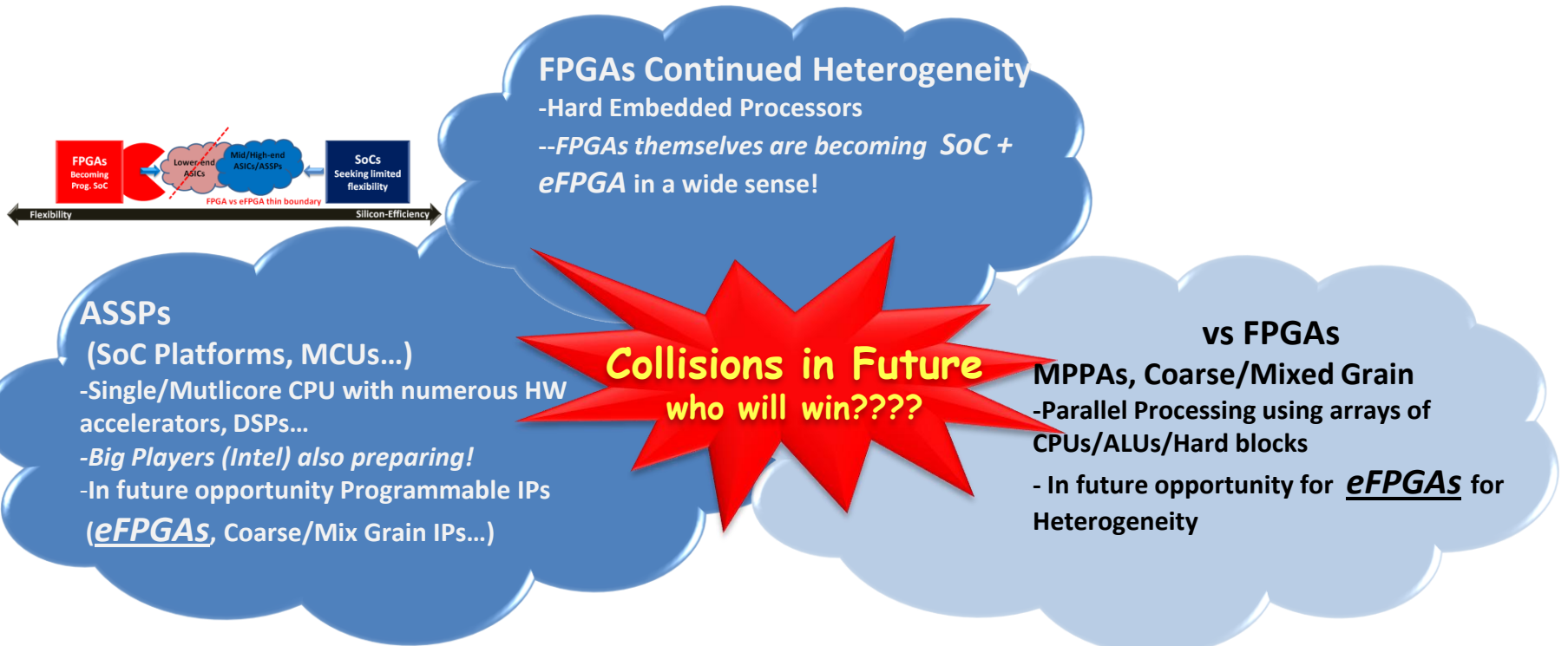
EXTRA SLIDES for Q&A

Future is cloudy, Heterogeneity seems imminent

Industry heading towards platform collisions

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© SZA (linkedin.com/in/SyedZahidAhmed), 22 June 2011: PhD Dissertation: eFPGAs.



*PC/Servers (Stand alone immense market) is not considered in this spectrum

Tales from Proceedings of International Graveyard of Reconfigurable Computing

FPGAs vs CG (Coarse Grain)/CG-like story



FPGAs cleverly enjoyed/exploited:
Nice party Scenario



Coarse Grains unfortunately suffered:
Solo Adventure in Desert
3 wars: Hardware + Language + Near-no-IP

Some Key FPGA Architecture Scientists from Industry & Academia



Ross Freeman (1948-1989)
Xilinx (co-founder)
 Inventor of modern FPGAs



Robert F. Hartmann
Altera (co-founder)



Jonathan Rose
 (Toronto Univ.)
 VPR legend



a gift from this thesis



David Lewis
 (Altera)

Alphabetical Lists & In no way cover all, but indeed many!



Raminda U. Madurawe
 (TierLogic)



Fredric Reblewski
 (m2000/AboundLogic)



Steven Teig
 (Tabula)



Stephen M. Trimberger
 (Xilinx LEGEND)
 150+ Patents



Steven P. Young
 (Xilinx LEGEND)
 150+ Patents



Vaughn Betz
 (Altera)



Kamal Chaudhary
 (Xilinx/Achronix)



Jonathan Greene
 (Actel)



Michael Hutton
 (Altera)



Sinan Kaptanoglu
 (Actel)



Olivier Lepape
 (m2000/AboundLogic)



Jason Anderson
 Toronto Univ.



Jason Cong
 UCLA



Jean-Luc Danger
 Telecom ParisTech



Guy Lemieux
 UBC



***Rajit Manohar**
 Cornell Univ.



Habib Mehrez
 LIP6



Alan Mischenko
 Berkeley Univ.



Tobias G. Noll
 RWTH Aachen



Russell Tessier
 UMASS



Wayne Luk
 Imperial College



Steve Wilton
 UBC



& let's not forget dozens of behind the scene (first authors) hero grad students, junior post-docs ... !



MCNC benchmarks

Phase-1 (LUT mapping with SIS)

Circuit	inputs	outputs	No. of LUT-4
ex5p	8	63	1064
tseng	52	122	1047
apex4	9	19	1262
misex3	14	14	1397
alu4	14	8	1522
diffeq	64	39	1497
dsip	229	197	1370
seq	41	35	1750
apex2	38	3	1878
des	256	245	1591
bigkey	229	197	1707
s298	4	6	1931
spla	16	46	3690
frisc	20	116	3556
elliptic	131	114	3604
pdcc	16	40	4575
ex1010	10	10	4598
s38417	29	106	6406
s38584	38	304	6447
clma	62	82	8383

Phase-2 (LUT mapping with eFPGA Programmer)

S No.	Circuit	inputs	outputs	I/Os	LUT4
1	ex5p	8	63	71	240
2	tseng	52	122	174	743
3	apex4	9	19	28	742
4	misex3	14	14	28	426
5	alu4	14	8	22	614
6	diffeq	64	39	31	714
7	seq	41	35	76	781
8	apex2	38	3	41	714
9	k2	45	45	90	546
10	s298	4	6	10	856
11	ex1010	10	10	20	922

Phase-2 SB-eLB Silicon Stats

		Base	Theme 1			Theme 2		
ST 65LPSVT_1.3V-m40C		tse_4448_F	tse_4448_noN	tse_4448_noNt	tse_4448_50p	tse_4448_c1	tse_4448_c2	tse_4448_c3
				E	All			
Conf. bits	Total	468	468	452	452	436	436	436
	SBOX	400	400	384	384	368	368	368
	eLB	68	68	68	68	68	68	68
Area (um ²)	Total	15023	13550	11769	11758	9881	9881	9881
	SBOX R	2440	2440	2440	2440	2440	2440	2440
	SBOX L	6720	5232	3600	3600	1984	1984	1984
	eLB	418	418	418	418	418	418	418
	Conf.	4043	4066	3960	3960	3810	3810	3810
	Buff.	1402	1394	1351	1340	1229	1229	1229
Logic Density (LUT4/mm ²)		266	295	340	340	405	405	405
Area Normalized to F		1.00	0.90	0.78	0.78	0.66	0.66	0.66
Power	Static (nW)	452	415	365	365	304	304	304
	Dyn. (uW/MHz)	3.67	3.45	2.87	2.91	2.44	2.41	2.42

Phase-2 SB-eLB explorations

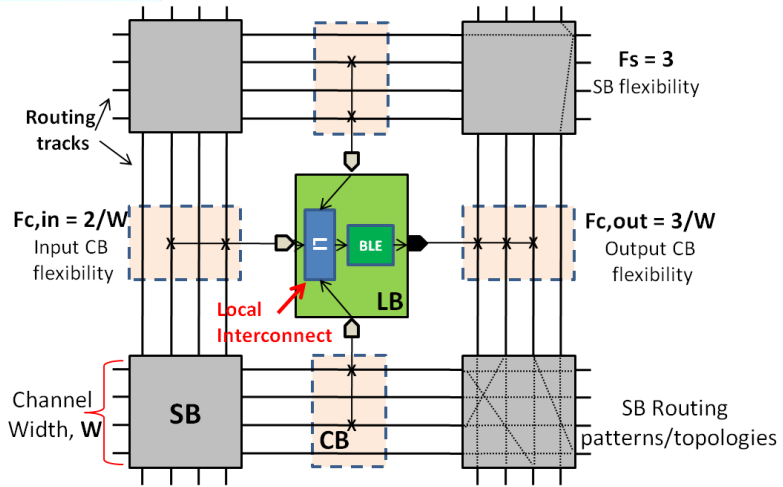
51

Circuit	tse_4448_noN				tse_4448_noNE				tse_4448_50pAll			
	Ch. Max	Ch. Avg	R. Iter	Delay(ns)	Ch. Max	Ch. Avg	R. Iter	Delay(ns)	Ch. Max	Ch. Avg	R. Iter	Delay(ns)
ex5p	23	5	5	11.65	27	5.72	6	12.92	18	4.54	6	11.88
tseng	28	9.2	6	13.44	24	11	7	14.64	20	8.6	6	14.12
apex4	36	17.6	7	20.72	39	20.25	7	19.96	RF			
misex3	28	8.9	6	12.73	31	10.4	8	13.3	23	8.5	7	12.54
alu4	31	12.3	7	17.8	33	14.3	8	17.73	24	12	10	16.98
diffeq	24	9.6	7	15.93	29	11.7	7	17.2	19	9	7	15.6
seq	37	16.9	7	16.13	37	19.2	7	15.84	RF			
apex2	34	15.6	7	19.35	38	18.8	8	19.23	24	16.4	94	22.84
k2	33	12.7	7	14.06	36	14.4	7	16.56	25	13.4	55	18.57
s298	41	19.1	7	24.5	41	21.3	8	28.06	RF			
ex1010	38	20.7	8	21.06	41	24.5	8	21.98	RF			
A. Mean	32.1	13.4	6.7	17.03	34.2	15.6	7.4	17.95	21.86	10.3	26.43	16.08

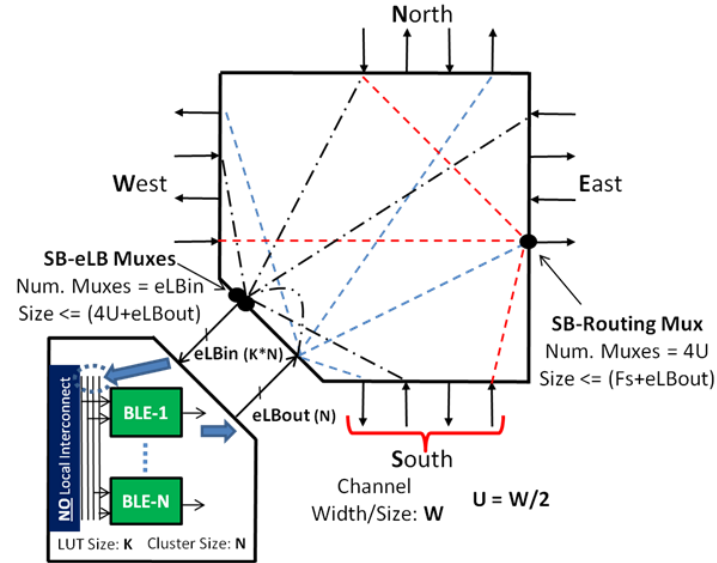
Circuit	tse_4448_c1				tse_4448_c2				tse_4448_c3			
	Ch. Max	Ch. Avg	R. Iter	Delay(ns)	Ch. Max	Ch. Avg	R. Iter	Delay(ns)	Ch. Max	Ch. Avg	R. Iter	Delay(ns)
ex5p	30	6.5	6	10.9	30	6.4	6	12.01	32	7.3	6	12.8
tseng	25	9.4	5	12.76	27	9.4	5	13.1	RF			
apex4	42	23.5	10	20.63	41	23.5	24	21.2	RF			
misex3	34	12.3	6	12.25	33	12.2	7	11.2	33	13.6	8	13.41
alu4	36	16.9	7	15.46	38	16.7	7	17.2	37	18.2	7	16.74
diffeq	27	10.4	6	15.34	26	10.7	6	15.34	RF			
seq	39	23.5	15	15.92	43	23	12	15.3	RF			
apex2	41	22.36	12	17.85	40	22.5	10	19.23	RF			
k2	38	15.8	7	15.4	39	15.78	8	15.63	39	17.6	8	15.9
s298	RF				RF				RF			
ex1010	RF				RF				RF			
A. Mean	34.7	15.63	8.22	15.17	35.2	15.58	9.4	15.58	35.25	14.18	7.25	14.7

eFPGA Architecture Fundamentals

Thesis objective: Soft eFPGA, **NEW** *what-if* experiments



V. Betz & J. Rose VPR Arch ~1997 (Toronto Univ.)
Widely explored arch. in academics (*still is*)

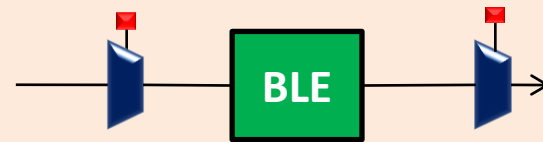


CB Mux Size = $F_{c,in}$

LI Mux Size = $I + N$
 $I = K \cdot (N + 1) / 2$

CB Mux Size $\leq N + 1$

SB Mux Size = F_s



SB-eLB Mux Size $\leq 4U + N$

SB-R Mux Size $\leq N + F_s$

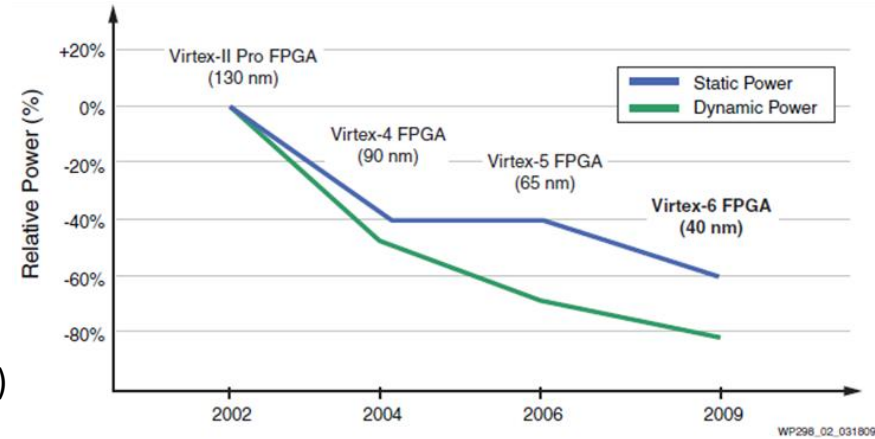
Equivalent Soft Model of Classical (VPR) arch.

eFPGA investigation Model of this work
Unified-SB with eliminated CB and LI

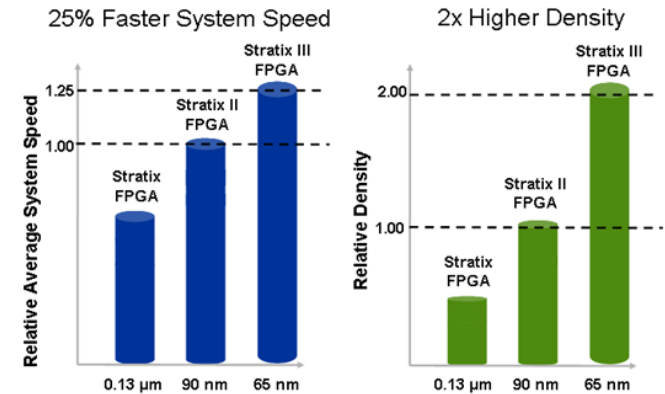
Key FPGA research areas

FPGAs literature (vendors + academics) and patents survey

- Island-style, Column-based arch.
- Challenges of Logic block
- Challenges of Routing arch.
- Heterogeneity at multiple levels
- ASIC vs FPGA Gap* (**35X Area, 3X-5X Speed, 14X Power**)
- *Power vs Performance in beyond 90nm*



Performance and Density Improvement



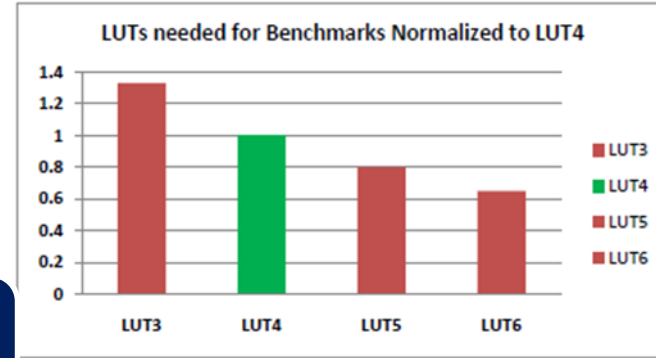
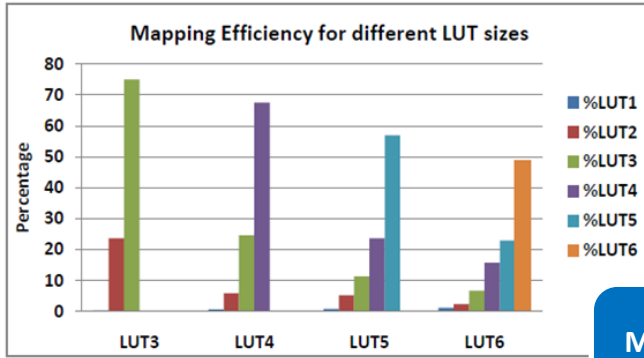
Copyright © 2007 Altera Corporation



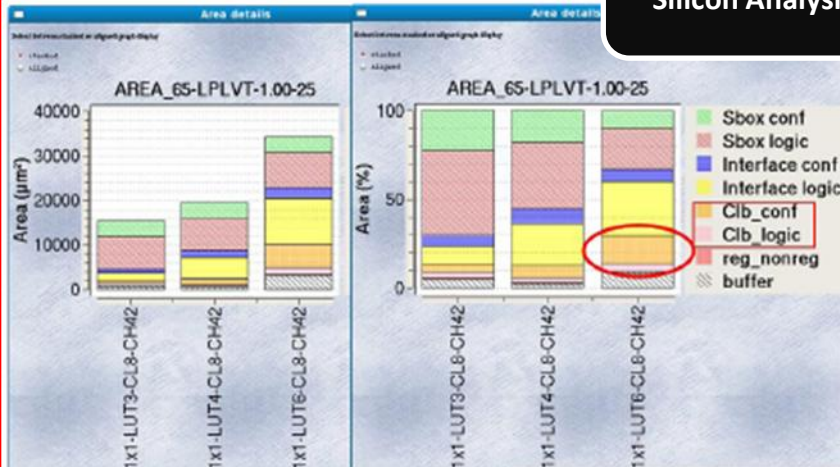
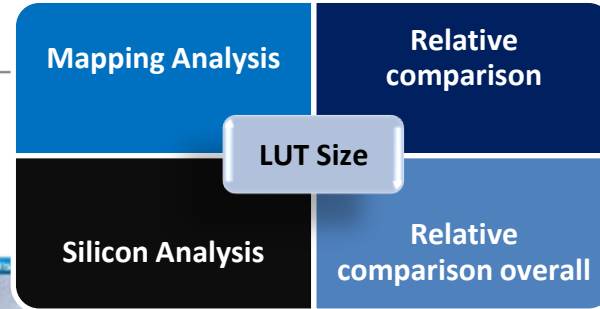
* I.Kuon & J. Rose (Toronto Univ.)

All images from Xilinx, Altera Websites

Phase-1 LUT Analysis



Bigger LUTs have poor mapping efficiency

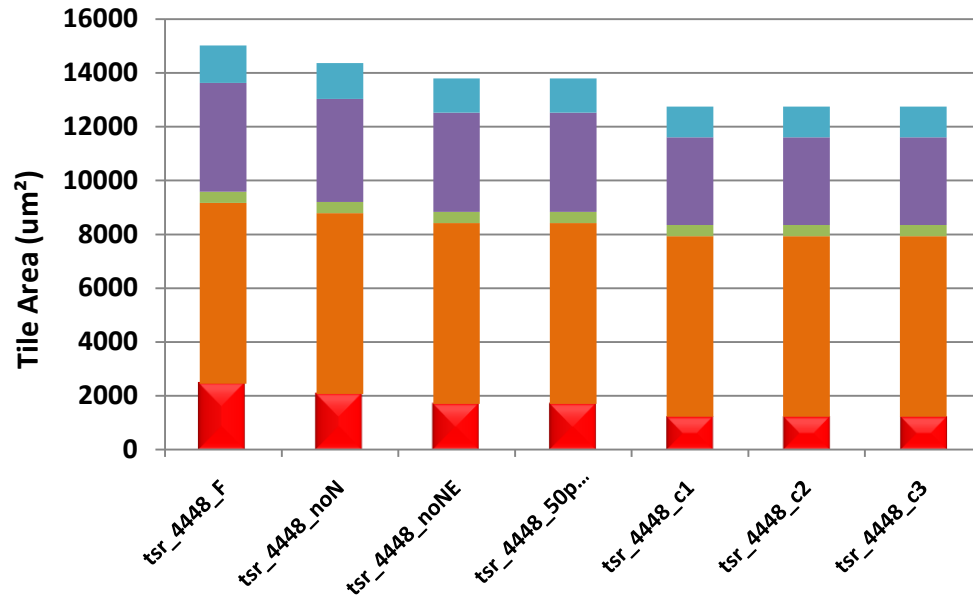


LUT size	% of Tile (Conf.+Logic)	Area Normalized to LUT4 arch.	Logic Capacity wrt LUT4 (mapping efficiency considered)
LUT-3	7.33	0.8	0.75
LUT-4	9.42	1	1
LUT-6	19.95	1.7	1.54

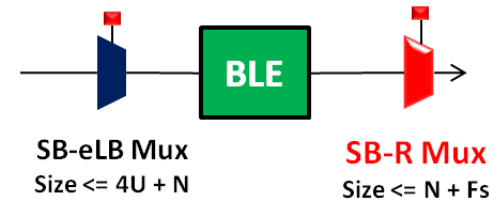
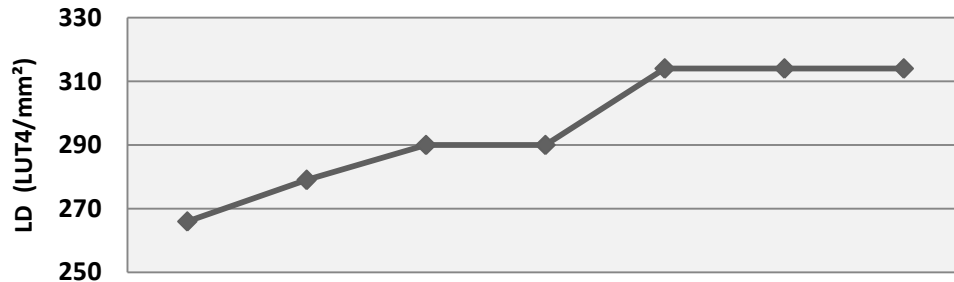
LUT-3 inefficient compared to LUT4

Phase-2

SB-R Explorations: Silicon Statistics (ST 65nm LP)



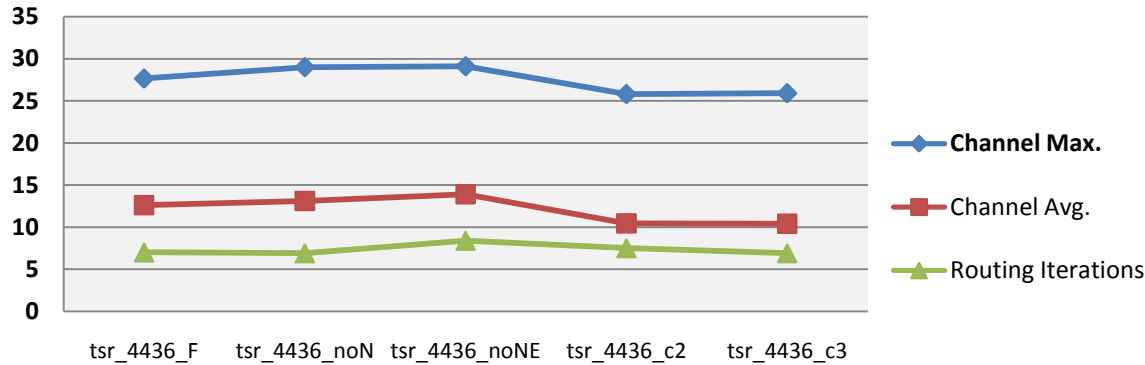
- Buff.
- Conf.
- eLB
- SB-eLB
- SB-R**



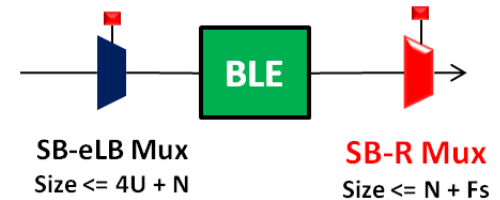
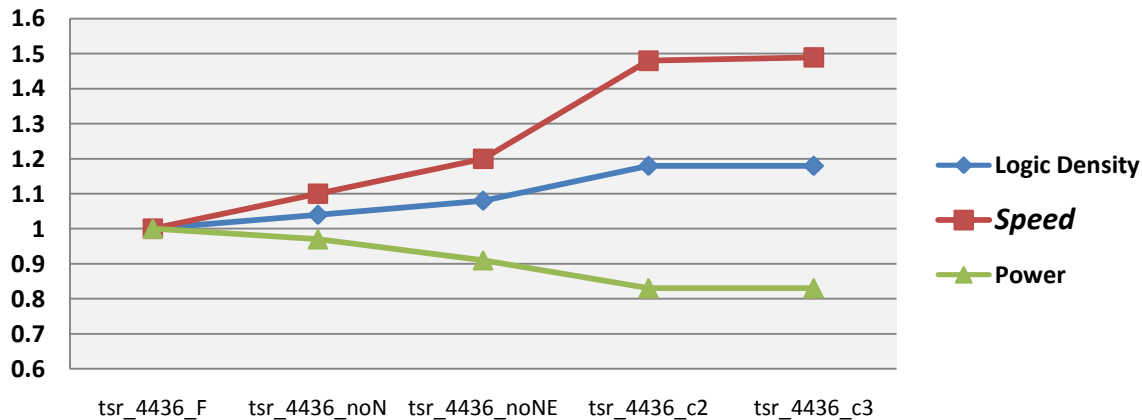
Phase-2

SB-R Explorations: Tradeoffs

Routing Statistics: near win-win situation by Theme 2

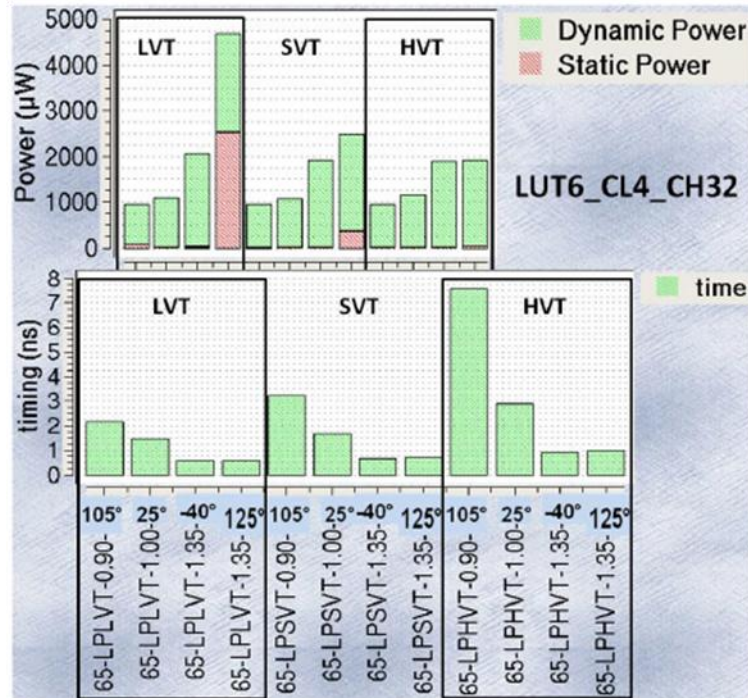


Relative Gains in Area, Speed & Power*



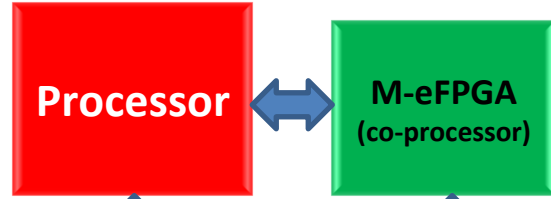
Power vs Performance

Effect of threshold voltage



MRAMs

like a dream come true for embedded Computing



Non Volatile*

- Live at power up
- Full/Partial shut down to save power
- Re-programmable

*Rad-Hard***



Shadowed Dynamic Reconf.***

- Change config. on the fly! (inherent 2 contexts virtually possible)

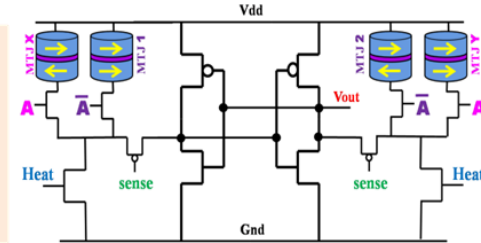
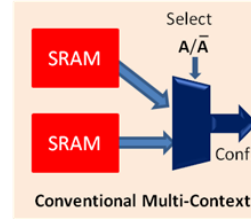
Multi-Context****

- Increased computation efficiency
- low silicon overhead vs SRAM/Flash
- highly attractive for co-processing

Standard CMOS process*****

Chief Competitors of MRAMs

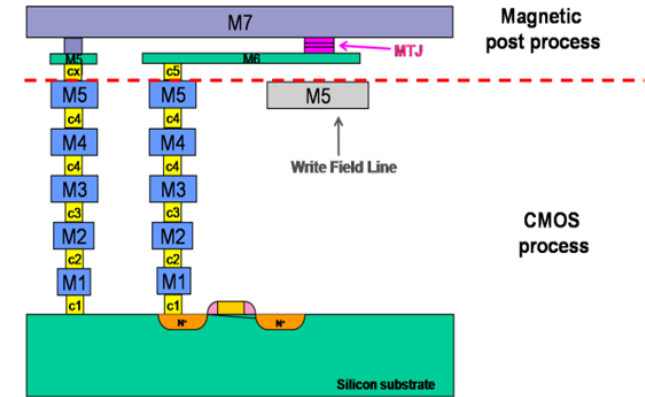
- FRAM (TI is focused)
- PCM (Samsung is focused)



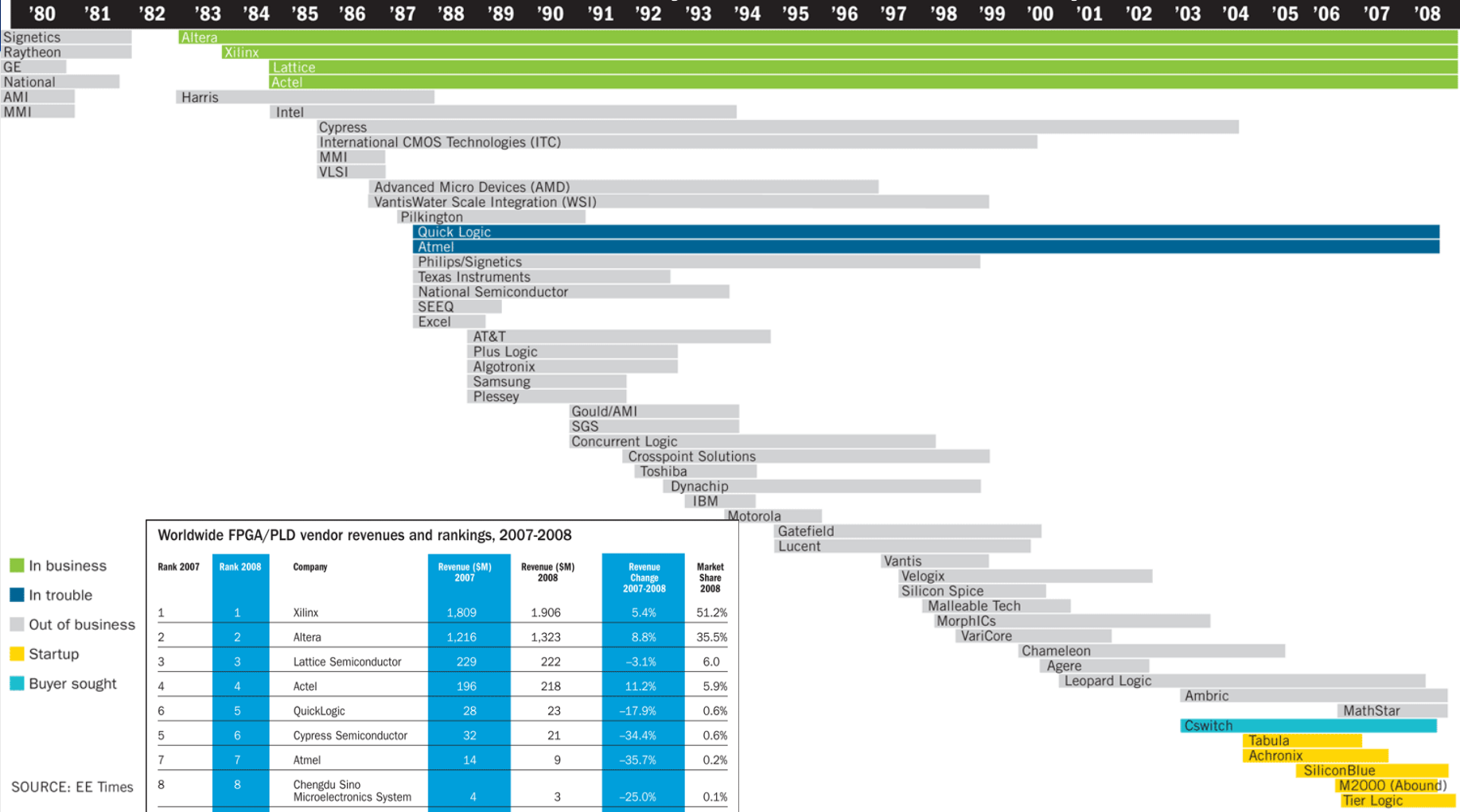
No. Context	1	2	4	8	16
Transistors: SRAM+MUX	6	16	34	68	134
Transistors: MRAM	10	12	16	24	40

MRAM based Multi-Context (low silicon overhead)

LIRMM has filed multiple patents on silicon-efficient MRAM cell structures



The History of PLD startups



Worldwide FPGA/PLD vendor revenues and rankings, 2007-2008

Rank 2007	Rank 2008	Company	Revenue (\$M) 2007	Revenue (\$M) 2008	Revenue Change 2007-2008	Market Share 2008
1	1	Xilinx	1,809	1,906	5.4%	51.2%
2	2	Altera	1,216	1,323	8.8%	35.5%
3	3	Lattice Semiconductor	229	222	-3.1%	6.0
4	4	Actel	196	218	11.2%	5.9%
6	5	QuickLogic	28	23	-17.9%	0.6%
5	6	Cypress Semiconductor	32	21	-34.4%	0.6%
7	7	Atmel	14	9	-35.7%	0.2%
8	8	Chengdu Sino Microelectronics System	4	3	-25.0%	0.1%
		Others	0	0	NM	0.0%
		Total Market	3,528	3,725	5.6%	100.0%

- In business
- In trouble
- Out of business
- Startup
- Buyer sought

SOURCE: EE Times

Industrial Survey on Status of Several Multicore/Coarse Grain companies (2009)

COMPANY	PRODUCT	COMMENTS
Ambric	AM2000 family-344 Processors	Was shipping video chips, but backing dried up
Aspex Semiconductor (U.K.)	Linedancer 4,096 Processors	Silicon killed; now marketing IP for video
BrightScale	BA 1024 Video Processor	Was Connex Technology; now marketing IP
ClearSpeed Technologies	Multithread 96-element array processor	Now selling as subsystems
Coherent Logix, Inc.	hx2100 HyperX-based DSP	Still in development
CPU Technology, Inc.	Acalis7 Field-Programmable MultiCores	Actively marketing
Element CXI	Reconfigurable Array	Showing silicon-actively marketing
Elixent/Panasonic (U.K.)	D-Fabrix Array	Now Captive; status unknown
IMEC (Belgium)	ADRES: Coarse Grain Array for VLIW's	Licensable IP, actively marketing
Intelliasys	Scalable Embedded Array 24 processors	Actively marketing
IP Flex (Japan)	DAP/DNA-955 16-bit processors	Now shipping for video
MathStar	Field Programmable Object Array	Out of business
Motorola Labs	Reconfig. Streaming Vector Processor	Development ceased
NEC (Japan)	Dynamically Reconfigurable Logic Engine	Development appears to have ceased
PACT XPP Technologies	XPP 3C-64 processors	Actively marketing IP
PicoChip Designs (U.K.)	picoArray Massively Parallel Array	Shipping in volume
Plurality (Israel)	Hypercore Processor: 16-256 cores	In Development
Rapport Inc.	Kilocore KC-256 with 256 processors	Appears to have folded
Recore (Netherlands)	Montium Tile Processors	Licensable IP-status unknown
Silicon Hive (Netherlands)	Moustique Block Accelerators	Licensable IP-actively marketing
Stream Processors Inc.	Storm-1 Family-80 32-bit ALUs	Surveillance Video-actively marketing
Tabula	Unannounced	In Stealth Mode** (starts shipping in 2010)
Tilera	TilePro36 & 64	1st generation now shipping

Massively parallel processors: Who's still alive?
by Kenton Williston (2009)

<http://www.eetimes.com/electronics-blogs/dsp-designline-blog/4034360/Massively-parallel-processors-Who-s-still-alive->
<http://www.eetimes.com/design/signal-processing-dsp/4017733/Analysis-Why-massively-parallel-chip-vendors-failed>

Despite numerous failures, and still being a small niche
Reconfigurable Computing will continue inspiring researchers and
industry and will play important role in *dark* challenges ahead



Semiconductor Industry Empire

Top 25 Semiconductor Giants (Foundries excluded)

2008 Rank	2009 Rank	Company Name	2008 Revenue	2009 Revenue	Percent Change	Percent of Total	Cumulative Percentage
1	1	Intel	33,767	32,410	-4.0%	14.1%	14.1%
2	2	Samsung Electronics	16,902	17,496	3.5%	7.6%	21.7%
3	3	Toshiba	11,081	10,319	-6.9%	4.5%	26.2%
4	4	Texas Instruments	11,068	9,671	-12.6%	4.2%	30.4%
5	5	STMicroelectronics	10,325	8,510	-17.6%	3.7%	34.1%
8	6	Qualcomm	6,477	6,409	-1.1%	2.8%	36.9%
9	7	Hynix	6,023	6,246	3.7%	2.7%	39.6%
12	8	Advanced Micro Devices (AMD)	5,455	5,207	-4.6%	2.3%	41.9%
6	9	Renesas Technology	7,017	5,153	-26.6%	2.2%	44.1%
7	10	Sony	6,950	4,468	-35.7%	1.9%	46.1%
10	11	Infineon Technologies	5,954	4,456	-25.2%	1.9%	48.0%
11	12	NEC Electronics	5,826	4,384	-24.8%	1.9%	49.9%
16	13	Micron Technology	4,435	4,293	-3.2%	1.9%	51.8%
14	14	Broadcom	4,643	4,278	-7.9%	1.9%	53.6%
19	15	Elpida Memory	3,599	3,948	9.7%	1.7%	55.4%
24	16	MediaTek	2,896	3,551	22.6%	1.5%	56.9%
13	17	Freescale Semiconductor	4,966	3,402	-31.5%	1.5%	58.4%
15	18	Panasonic Corporation	4,473	3,243	-27.5%	1.4%	59.8%
17	19	NXP	4,055	3,240	-20.1%	1.4%	61.2%
18	20	Sharp Electronics	3,607	2,977	-17.5%	1.3%	62.5%
21	21	nVidia	3,241	2,826	-12.8%	1.2%	63.7%
20	22	ROHM Semiconductor	3,348	2,586	-22.8%	1.1%	64.8%
23	23	Fujitsu Microelectronics	2,978	2,574	-13.6%	1.1%	66.0%
22	24	Marvell Technology Group	3,059	2,572	-15.9%	1.1%	67.1%
26	25	IBM Microelectronics	2,473	2,253	-8.9%	1.0%	68.1%
Other Companies:			85,619	73,445	-14.2%	31.9%	100.0%
Total Revenue:			260,237	229,917	-11.7%	100.0%	

Top Semiconductor OEM Spenders

Rank	Company	2009	2010
1	Hewlett-Packard	10,985	12,613
2	Samsung Electronics	10,252	12,489
3	Nokia	9,080	9,799
4	Apple	7,000	8,448
5	Dell	7,186	7,736
6	Panasonic	5,711	6,325
7	Sony	4,432	5,277
8	Motorola	4,237	4,933
9	LG Electronics	3,922	4,297
10	Kingston Technology	3,389	4,165
11	Acer	3,272	3,754
12	Toshiba	3,209	3,745
13	Hitachi	2,981	3,331
14	Lenovo	2,881	3,115
15	Cisco Systems	2,628	3,113
16	RIM	2,685	3,109
17	NEC	2,752	3,061
18	Fujitsu	2,601	2,780
19	Nintendo	3,061	2,466
20	Sony-Ericsson	2,038	2,200

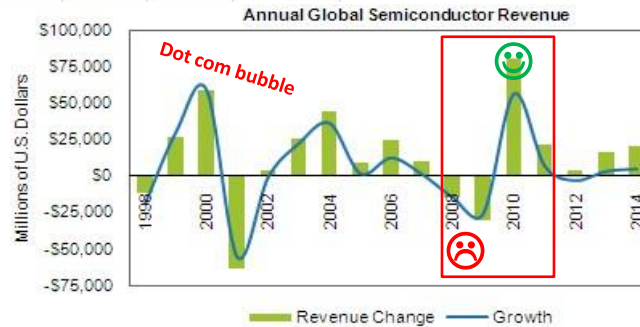
Biggest Stand alone FAB
TSMC: ~10,000 Million \$

~ 85% of FPGA market
Xilinx : ~1,900 Million \$
Altera: ~ 1,400 Million \$

Source: iSuppli Corporation, March 2010

	1955 SILICON/ GERMANIUM	1965 TRANSISTOR/ IC	1977 IC/ MOS MEMORY	1987 MEMORY/ MICROPROCESSOR	1997 MICROPROCESSOR/ SOC	2007 SOC/ FABLESS
Hughes	Texas Instrument	Texas Instrument	NEC	Intel	Intel	
Transitron	Fairchild	Motorola	Toshiba	NEC	Samsung	
Philco	Motorola	NEC	Hitachi	Motorola	Toshiba	
Sylvania	General Instruments	Hitachi	Motorola	Texas Instrument	Texas Instrument	
Texas Instrument	GE	Philco	Texas Instrument	Toshiba	STMicroelectronics	
GE	RCA	National Semiconductor	Fujitsu	Hitachi	Infuneon	
RCA	Sprague	Toshiba	Philips	Samsung	Hynix	
Westinghouse	Philco	Fairchild	Intel	Fujitsu	Renesas	
Motorola	Transitron	Intel	National Semiconductor	Philips	NXP	
Clevite	Raytheon	Siemens	Matsushita	STMicroelectronics	NEC	

Retired from Top 10 semiconductor company list

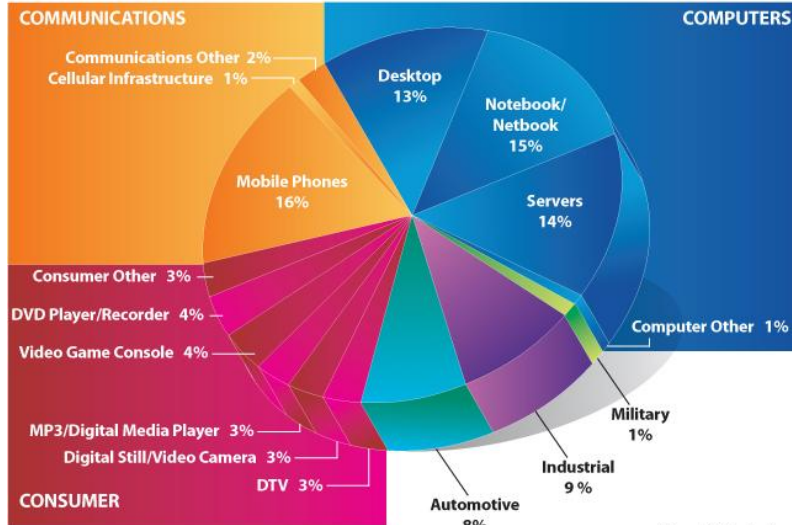


iSuppli: 2010 forecast, highest growth year ever in history

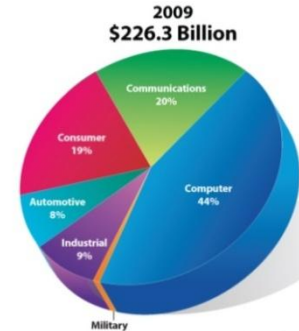
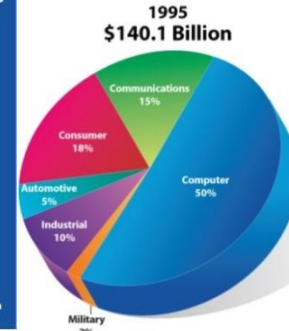
Semiconductor Industry Empire

2009 Semiconductor Revenue Distribution

Computers and Communications Account for >64%



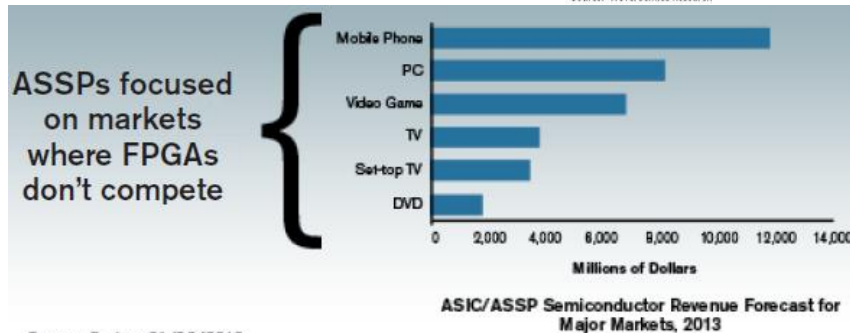
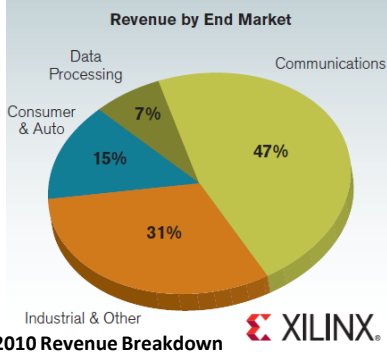
Handheld Wireless is the Only Major Change in the Makeup of the Semiconductor Macro TAM



2009 Rank	2008 Rank	Company Name	2008 Revenue	2009 Revenue	Percent Change	Percent of Total	Cumulative Percentage
1	1	Intel	39,797	32,419	-18.3%	24.1%	24.1%
2	2	Samsung Electronics	18,882	17,486	-7.4%	13.1%	37.2%
3	3	Toshiba	11,681	10,919	-6.5%	8.2%	45.4%
4	4	Texas Instruments	11,068	9,871	-11.6%	7.4%	52.8%
5	5	STMicroelectronics	10,542	9,810	-7.0%	7.3%	60.1%
6	6	Qualcomm	6,477	6,409	-1.1%	4.8%	64.9%
7	7	Infineon	6,031	6,046	0.2%	4.5%	69.4%
8	8	Advanced Micro Devices (AMD)	5,495	5,297	-3.6%	3.9%	73.3%
9	9	Siemens Technology	2,117	2,110	-0.3%	1.6%	74.9%
10	10	Sony	6,990	6,990	0.0%	5.2%	80.1%
11	11	Infraero Technologies	5,054	4,956	-2.0%	3.7%	83.8%
12	12	NEC Electronics	4,368	4,368	0.0%	3.3%	87.1%
13	13	Micro Technology	4,435	4,289	-3.3%	3.2%	90.3%
14	14	Renesas	4,443	4,278	-3.8%	3.2%	93.5%
15	15	Exata Memory	2,199	2,146	-2.4%	1.6%	95.1%
16	16	Hitachi	2,086	2,071	-0.7%	1.6%	96.7%
17	17	Freemove Semiconductor	4,986	3,452	-31.1%	2.6%	99.3%
18	18	Renasonic Corporation	4,071	3,240	-20.2%	2.4%	101.7%
19	19	Infax	4,095	3,240	-20.1%	2.4%	104.1%
20	20	Shiga Electronics	2,997	2,977	-0.7%	2.2%	106.3%
21	21	STMicro	2,241	2,241	0.0%	1.7%	108.0%
22	22	SiMC Semiconductor	3,148	2,098	-33.7%	1.6%	109.6%
23	23	Yuhua Homeelectronics	2,973	2,973	0.0%	2.2%	111.8%
24	24	Marvell Technology Group	3,059	2,972	-2.9%	2.2%	114.0%
25	25	888 Microelectronics	2,472	2,292	-7.3%	1.7%	115.7%
Other Companies			89,819	73,441	-18.2%	55.8%	171.5%
Total Revenue			286,227	228,817	-11.1%	100.0%	

Rank	Company	2009	2010
1	Intel	10,051	12,813
2	Samsung Electronics	10,252	12,489
3	Nokia	9,090	9,758
4	Apple	7,000	9,458
5	Qualcomm	7,198	7,436
6	Panasonic	5,711	6,252
7	Sony	4,433	5,277
8	Motorola	4,297	4,333
9	LG Electronics	3,922	4,299
10	Kingston Technology	3,389	4,105
11	ACE	3,272	3,194
12	Toshiba	3,209	3,742
13	Hitachi	2,661	3,233
14	Lenovo	2,381	3,115
15	Cisco Systems	2,028	3,113
16	IBM	2,055	3,105
17	NEC	2,752	3,001
18	Ruifan	2,001	2,782
19	NetScout	3,051	2,458
20	Sony Ericsson	2,038	2,200

Main Markets of FPGAs



Source: Gartner 01/06/2010

ASSPs focused on markets where FPGAs don't compete

Source: Xilinx Corporate Backgrounder <http://www.xilinx.com/company/about.htm>
<http://phx.corporate-ir.net/External.File?item=UGFyZW50SUQ9NDg3MzR8Q2hpbGRJRUR0MmXUeXBjPTM=&t=1>

<http://www.eetimes.com/electronics-news/4088277/Viewpoint-Is-semiconductor-industry-consolidation-inevitable->

http://en.wikipedia.org/wiki/Semiconductor_sales_leaders_by_year

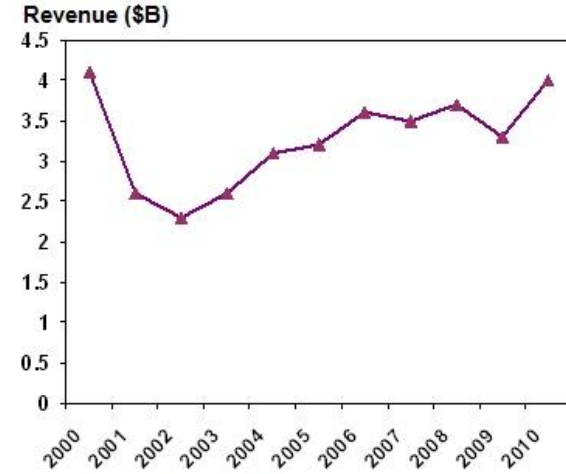
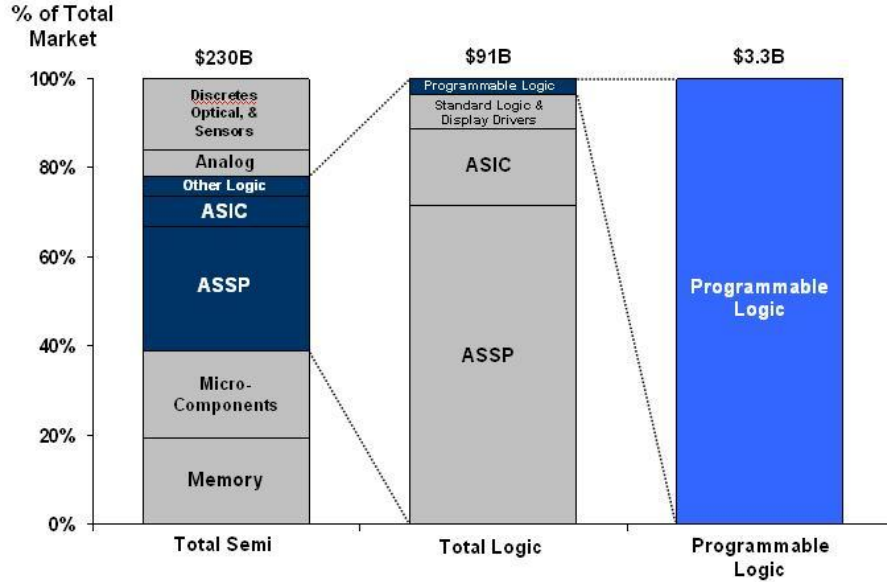
<http://www.eetimes.com/electronics-news/4088113/Who-is-largest-buyer-of-chips->

<http://www.design-reuse.com/news/24061/2010-global-semiconductor-revenue.html>

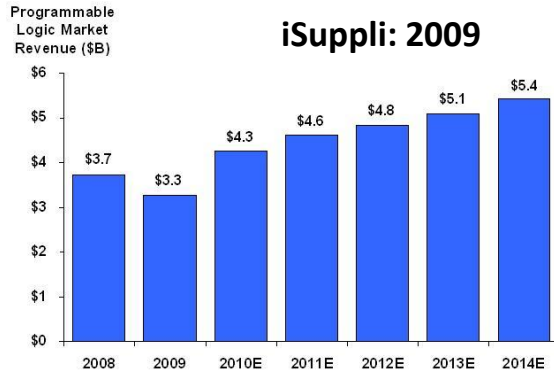
<http://www.isuppli.com/Semiconductor-Value-Chain/News/Pages/Semiconductor-Roid-Rage-Prompts-iSuppli-to-Pump-Up-2010-Forecast.aspx>

Semiconductor Industry Empire

FPGA/PLD Market



Source: Gartner, February 2010



<http://www.latticesemi.com/corporate/about/pldmarketbackground.cfm?source=topnav>

<http://www.eetimes.com/electronics-blogs/programmable-logic-designline-blog/4033356/A-dissenting-opinion-on-the-programmable-imperative->

New Trends in FPGAs

Makimoto's Customization cycle: Domain Specific FPGAs

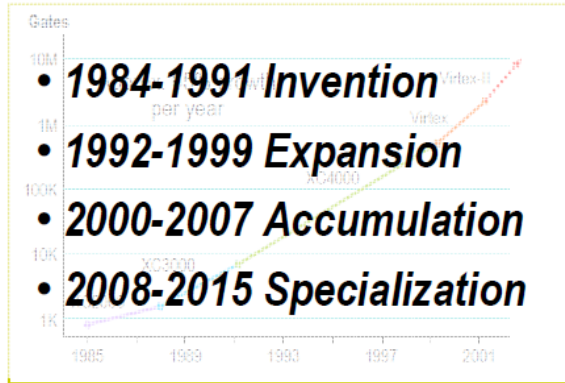


<http://ce.et.tudelft.nl/FPL/trimbergerFPL2007.pdf>

Dr. Steve Trimberger

XILINX

The Four Ages of FPGAs



FPL 2007 4

2007-2015

The Age of Specialization

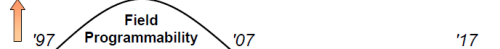
- FPGA capacity and speed exceed typical design requirements
 - Customers won't pay a premium for them
- Application domains have diverging requirements
- Application domains are large enough to justify customized FPGAs
- Domain-specific architecture has a cost advantage
 - Specialized logic blocks
 - Specialized memory and I/O (you *must* not forget the I/O!)
 - Blocks built to meet critical domain-specific attributes



FPL 2007 20



Standardization



Customization

- Mask-Less Technology
- Super Connect
- e-Business

Industry is moving to Makimoto's **Customization** Cycle
More domain specific and Heterogeneous FPGAs and ASSPs will come In coming years and Power will further force that

Global French CIFRE PhD Motivations (for international audience, Universities & Industry)

66

You will become a **doctor** once you have defended your thesis, proving that you are capable of undertaking a substantial R&D project. You will be recognized for your participation in research and innovation, your keen capacity for tackling the problems facing a company, and your interaction with partners from different cultures.

The vocation of the highly popular CIFRE process is to contribute to the competitiveness and innovation of French business. It encourages exchanges between public research laboratories and socio-economic environments and contributes to helping doctors find work in companies of all sizes.

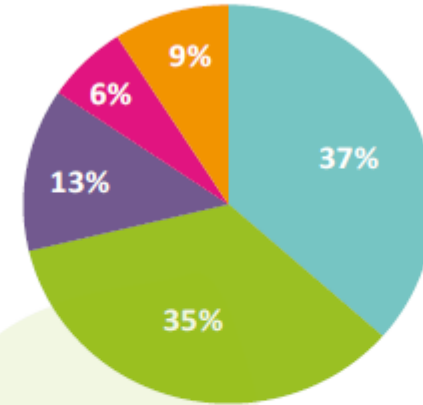
PhD while carrying out research work within the company and academic laboratory. This means you participate in bringing the academic milieu closer to what your company is really looking for. You learn how to evolve instinctively within these two distinct worlds.

Dispositif CIFRE, deux objectifs

- *Placer les doctorants dans des conditions d'emploi scientifique*
- *Concourir au développement des collaborations de recherche partenariale entre le monde entrepreneurial et le monde académique*

Cifre

How doctors are employed after completing a CIFRE



- Remain in the company
- Join another company
- Join a public research or teaching body
- Pursue post-doctoral studies
- Seek employment

Results for 11,808 CIFREs since 1981

http://www.anrt.asso.fr/fr/pdf/plaquette_cifre_complete_avril2009_GB.pdf
http://www.anrt.asso.fr/fr/pdf/diapo_presentation_cifre.pdf

Invitation Flyer to PhD Defense

eFPGAs: Architectural Explorations, System Integration & a Visionary Industrial Survey of Programmable Technologies

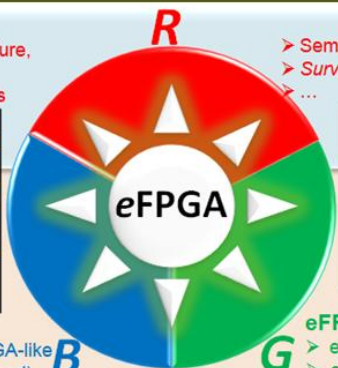
Survey & Analysis

- > FPGA State of the Art: literature, patents, press news
- > Potentials of emerging trends



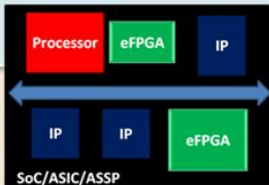
eFPGA architecture

- > Exploration of *efficient!* FPGA-like conventional eFPGAs (LUT-based)
- > Creation of CAD Tools infrastructure
- > Soft eFPGAs (tech. node independent)
- > ...



iPhD

- > Semiconductor industry analysis
- > Survey of Programmable technologies
- > ...



eFPGA in system

- > eFPGAs applications/challenges
- > eFPGAs as *Reconf. accelerators*
- > Case studies for perspectives of beyond classic eFPGAs (MRAM etc.)
- > ...

Welcome Bienvenue Willkommen خوش آمدید مرحبا

to
PhD Dissertation of **Syed Zahid AHMED**

on

Wed. June 22nd 2011, 14:30h

@ LIRMM (Room 2.57): 161 Rue Ada, Montpellier, FRANCE

GPS: 43° 38'.22 N, 3° 50'.42 E

A Premiere Event

"The Grad Student's Speech"

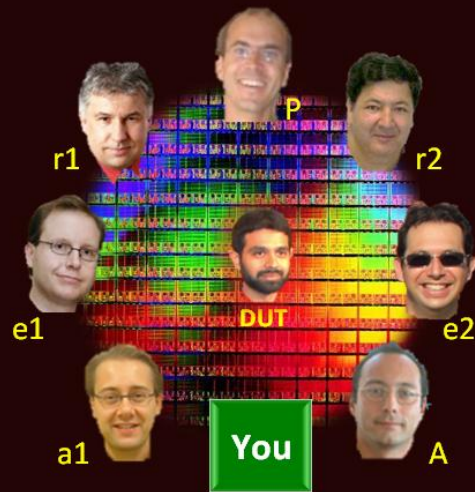
Research Presents

An **Production**

PhD at

Lords of the Jury

- P : Prof. Guy Gogniat (FR)
- r1: Prof. Jüergen Becker (DE)
- r2: Prof. Habib Mehrez (FR)
- e1: Dr. Michael Hübner (DE)
- e2: Mr. Laurent Rougé (FR)
- a1: Dr. Gilles Sassatelli (FR)
- A : Prof. Lionel Torres (FR)



The Last act of/as CIFRE (See Epilogue of Thesis draft)

Abstracts taken from Industry vs Academics (|V|): the inside story of my PhD

68

Mentioned In spirit of Industry (grab differentiation) & Academia (we share)

Unbiased Global findings: what I learned/found/investigated is

In one embodiment an entity called Semiconductor Industry:

- We are not primarily doing this for the humanity, it's our business, if we don't do it someone else (competitor) will
- If one can't control/protect one's market share, be visionary enough to foresee future before enemy (needs can/may be created); he will/may be doomed, no matter how big/dominant one is (tomorrow will/may not take care of itself)
- There are usually two ways to do business: 1- Have something that no one has, use/create dominance of/through that; 2- Find weakness of the enemy, use that as strength and crush him with it
- Science alone can/does not run/drive the industry, it takes TWO (geeks + businessmen) to do wonders
- We protect knowledge (patent), exploit/help academia, steal ideas, buy ideas, can/damage science for business, even do miracles of science, are often at high risks (market/economy). All is fair in love & war, damn hard we try playing that!

In another embodiment a corresponding* entity called Academia:

- We love: to share, cite and be cited (the beauty & burden of selfless academia)
- There are two distinct kinds of professors in the world: those who contribute science and those who contribute themselves in the name of science. In real-life many do/must/have to use a mixture of it for obvious reasons
- The finest minds of academia (professors) are/made so diversely overloaded that often they don't/can't find fair enough time for what they are/wished/supposed to be overloaded for (homogeneous academia vs heterogeneous industry)
- IEEE/ACM paid downloads business model is/has gone outdated in/for internet era: Google business model supremacy
- Only **Professors** can live happily ever after (wonders of teaching/tenure): it depends on them how happily they enjoy their ever after (the legends not even retire, ever after). No place is more prestigious and safer than the University!



*embodiments like CNRS/Fraunhofer-like were not investigated as industry/academia!