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par

Nan Li

**Digital Control Strategies for DC/DC SEPIC Converters towards
Integration**

**Stratégies de Commande Numérique pour un Convertisseur DC/DC SEPIC
en vue de l'Intégration**

Soutenue: le 29 Mai 2012 devant la Commission d'examen

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RÉSUMÉ

L'utilisation des alimentations à découpage (SMPSs : switched mode power supplies) est à présent largement répandue dans des systèmes embarqués en raison de leur rendement. Les exigences technologiques de ces systèmes nécessitent simultanément une très bonne régulation de tension et une forte compacité des composants. SEPIC (Single-Ended Primary Inductor Converter) est un convertisseur à découpage DC/DC qui possède plusieurs avantages par rapport à d'autres convertisseurs de structure classique. Du fait de son ordre élevé et de sa forte non linéarité, il reste encore peu exploité. L'objectif de ce travail est d'une part le développement des stratégies de commande performantes pour un convertisseur SEPIC et d'autre part l'implémentation efficace des algorithmes de commande développés pour des applications embarquées (FPGA, ASIC) où les contraintes de surface silicium et le facteur de réduction des pertes sont importantes. Pour ce faire, deux commandes non linéaires et deux observateurs augmentés (observateurs d'état et de charge) sont exploités : une commande et un observateur fondés sur le principe de mode de glissement, une commande prédictive et un observateur de Kalman étendu. L'implémentation des deux lois de commande et l'observateur de Kalman étendu sont implémentés sur FPGA. Une modulation de largeur d'impulsion (MLI) numérique à 11-bit de résolution a été développée en associant une technique de modulation Δ - Σ de 4-bit, un DCM (Digital Clock Management) segmenté et déphasé de 4-bit, et un compteur-comparateur de 3-bit. L'ensemble des approches proposées sont validées expérimentalement et constitue une bonne base pour l'intégration des convertisseurs à découpage dans les alimentations embarquées.

Mots clés : Convertisseurs DC-DC, SEPIC, Commande par mode de glissement, Commande prédictive, Observateur Kalman étendu, FPGA, MLI numérique

ABSTRACT

The use of SMPS (Switched mode power supply) in embedded systems is continuously increasing. The technological requirements of these systems include simultaneously a very good voltage regulation and a strong compactness of components. SEPIC (Single-Ended Primary Inductor Converter) is a DC/DC switching converter which possesses several advantages with regard to the other classical converters. Due to the difficulty in control of its 4th-order and non linear property, it is still not well-exploited. The objective of this work is the development of successful strategies of control for a SEPIC converter on one hand and on the other hand the effective implementation of the control algorithm developed for embedded applications (FPGA, ASIC) where the constraints of Silicon surface and the loss reduction factor are important. To do it, two non linear controls and two observers of states and load have been studied: a control and an observer based on the principle of sliding mode, a deadbeat predictive control and an Extended Kalman observer. The implementation of both control laws and the Extended Kalman observer are implemented in FPGA. An 11-bit digital PWM has been developed by combining a 4-bit Δ - Σ modulation, a 4-bit segmented DCM (Digital Clock Management) phase-shift and a 3-bit counter-comparator. All the proposed approaches are experimentally validated and constitute a good base for the integration of embedded switching mode converters.

Keywords: DC-DC converters, SEPIC, Sliding Mode Control, Predictive Deadbeat Control, Extended Kalman Observer, FPGA, DPWM.

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RÉSUMÉ ÉTENDU EN FRANÇAIS

Chapitre 1 INTRODUCTION

L'utilisation des alimentations à découpage (SMPSs : switched mode power supplies) est à présent largement répandue dans notre quotidien en raison de leur rendement. Ces alimentations occupent une place importante dans les ordinateurs, téléphones portables et autres appareils électroniques où les exigences technologiques actuelles demandent en même temps un haut niveau de performance de régulation et une compacité importante d'éléments.

SEPIC (Single-Ended Primary Inductor Converter) est un convertisseur à découpage DC/DC qui permet de remplir les fonctionnalités d'une cellule « convertisseur universel ». Ce type d'architecture possède plusieurs propriétés intéressantes. La première et la plus importante est le fonctionnement abaisseur-élevateur avec une tension de sortie ayant la même polarité que la tension d'entrée. Ensuite, la commande de l'interrupteur est référencée par rapport à la masse, ce qui simplifie l'électronique de commande rapprochée du module à commutation. Cependant, la commande de ce type de convertisseur présente plusieurs difficultés. D'une part, l'ordre du modèle est plus important que ceux des convertisseurs classiques (Buck, Boost et Buck-Boost), d'autre part, il présente un caractère non linéaire dont le comportement et la dynamique varient fortement selon le point de fonctionnement.

Généralement, la commande des convertisseurs à découpage est réalisée par des correcteurs analogiques. Les performances dynamiques de ces correcteurs requièrent un réglage souvent délicat voire impossible pour des convertisseurs de nature non linéaire comme SEPIC. En comparant à la solution analogique, la commande numérique offre des avantages potentiels comme une faible consommation de puissance et laisse une flexibilité importante pour la conception. Ainsi il est possible d'implémenter des algorithmes plus sophistiqués pouvant améliorer les performances du système. Dans la gamme de fréquence de découpage vers quelques dizaines de kilohertz, l'utilisation des DSP avec les fonctionnalités comme A/D, MLI... facilite l'implémentation numérique des algorithmes de commande.

Pour un objectif d'intégration, l'accroissement des fréquences de découpage est indispensable afin de réduire la taille des composants passifs du filtre de sortie de ces convertisseurs. Ces fréquences peuvent atteindre la gamme de plusieurs centaines de kilohertz voir de MHz où l'utilisation de FPGA ou d'ASIC est nécessaire. Une des difficultés majeures est la réalisation numérique d'un modulateur de largeur d'impulsion (DPWM : digital pulse-

width modulator) à haute résolution tout en gardant une fréquence d'horloge raisonnable pour préserver les pertes énergétiques qui augmentent avec la fréquence d'horloge.

L'objectif de la thèse est double : d'une part le développement des stratégies de commande performantes mais simples pour un convertisseur SEPIC et d'autre part, l'intégration efficace des lois de commande développées pour des applications embarquées (FPGA, ASIC) où les contraintes de surface silicium et le facteur de consommation d'énergie sont importants.

Le contenu de cette thèse est résumé ci-dessous :

- Présenter les différents types de modèles qu'on peut trouver dans la littérature. Discuter leurs utilisations et leurs limites.

- Proposer différentes approches de synthèse de lois de commande. Deux types de commande ont été développés. Le premier est une commande non-linéaire par mode de glissement (SMC : Sliding Mode Control) à fréquence de commutation constante. Le second est une commande prédictive pour laquelle on propose deux alternatives : une avec la possibilité de compenser le retard induit par la commande, l'autre avec une simplification d'algorithme pour faciliter l'implémentation numérique.

- Développer des observateurs non linéaires pour observer non seulement les états non mesurés dans le but de réduire le nombre de capteurs physiques, mais aussi l'évolution de la charge afin d'améliorer les performances de commande.

- Exposer les problèmes liés à la réalisation d'une DPWM à haute résolution et mettre en oeuvre une solution mixte matérielle et logicielle en utilisant une fréquence d'horloge modérée.

- Implémenter et tester l'ensemble des solutions proposées sur une plateforme FPGA.

Chapitre 2 MODELES DE SEPIC

La modélisation du convertisseur DC/DC a été largement étudiée au cours des décennies passées. Beaucoup de méthodes de modélisation mathématique ont été établies. Cependant, ces méthodes nécessitent d'être adaptées selon l'objectif. Certains modèles sont plus appropriés pour l'analyse des circuits alors que d'autres le sont pour la synthèse de lois de commande.

Dans ce chapitre, après une brève description du principe de fonctionnement de SEPIC, trois modèles sont présentés.

Le modèle hybride est capable de décrire conjointement les comportements continu et discret exposés par SEPIC. Il nous permet la validation en simulation des méthodes développées. Les lois de commande ou les observateurs synthétisés pour SEPIC dans ce mémoire sont testés avec le modèle hybride en simulation.

Le modèle dit « modèle moyenné » suppose que les effets du découpage sont « moyennés » durant une période de commutation. Le modèle moyenné est simple à construire et permet de réaliser un lien entre les sous-modèles du système hybride. Sous une forme d'un système bilinéaire du quatrième ordre, ce modèle donne la possibilité de concevoir une commande ou un observateur non linéaire en s'appuyant sur des outils existants des systèmes non linéaires.

Les modèles linéaires, appelés aussi modèle « petits signaux », sont obtenus en linéarisant le modèle moyenné autour d'un point de fonctionnement donné. Ces modèles permettent de déterminer simplement des fonctions de transfert locales, de synthétiser une loi de commande linéaire et d'analyser des propriétés du convertisseur dans le domaine fréquentiel. Une analyse de la corrélation entre le modèle linéaire et deux circuits réels est réalisée. L'évolution de ce modèle par rapport aux points de fonctionnement est étudiée.

Etant donné que seul le fonctionnement en mode de conduction continue (CCM : Continuous Conduction Mode) a été considéré dans cette thèse, avec le modèle « petits signaux », une étude analytique des frontières entre différents modes de fonctionnement et des limites est établie pour assurer une bonne condition de travail du SEPIC.

Chapitre 3 COMMANDE PAR MODE DE GLISSEMENT A FREQUENCE FIXE

Comme mentionné précédemment, SEPIC est un système non-linéaire du quatrième ordre. L'objectif de la commande est non seulement d'obtenir une très bonne performance du système, mais aussi de limiter la complexité algorithmique. En effet, pour un SEPIC fonctionnant à haute fréquence, le temps de calcul pour chaque période est limité d'une part, et la surface de silicium augmente avec le nombre de calculs et de ressources demandées, d'autre part.

La commande par mode de glissement (SMC) est un bon candidat pour répondre à cet objectif. Le principe de la commande par mode de glissement présente un intérêt très important à la commande des convertisseurs DC-DC qui sont caractérisés par une structure variable. Les méthodes existantes basées sur la modulation à hystérésis (HM : Hysteresis-Modulation) appliquée sur des convertisseurs classiques ont montré des performances très encourageantes, notamment au niveau de la robustesse vis-à-vis de certaines perturbations. Malheureusement, l'utilisation de la modulation à hystérésis conduit à une fréquence de commutation qui n'est pas constante. Une fréquence variable est peu souhaitable pour un convertisseur DC/DC, car elle rend difficile le dimensionnement des filtres. Pour pallier ce problème, nous avons adopté une méthode de SMC à fréquence fixe basée sur la modulation à largeur d'impulsion (MLI) ou PWM. La méthode consiste d'abord à définir une surface de glissement $S(x)$ qui prend en compte les objectifs attendus de la commande. Ensuite on cherche à déterminer la commande équivalente qui considère qu'en mode de glissement, tout se passe comme si le système était piloté par une commande qui rend la surface invariante dans le temps: $S(x) = 0$ et $\dot{S}(x) = 0$. Pour les convertisseurs de puissance, la commande équivalente correspond au rapport cyclique qui, grâce à une simple MLI, va générer une commande discontinue entre 0 et 1. Les conditions d'attractivité et de stabilité en utilisant le théorème de stabilité de Lyapunov définissent enfin les régions d'attraction.

Il existe une infinité de possibilités pour le choix de la surface de glissement. Pour le convertisseur SEPIC, nous avons présenté trois surfaces de glissement. La première est la plus simple. Elle prend en compte l'erreur du courant de l'inductance d'entrée et de la tension de sortie ainsi que l'intégrale de la somme de ces erreurs (ISM integral sliding mode). Malheureusement, la loi de commande correspondante donne une erreur statique sur la tension de sortie. Après une analyse de la cause de cette erreur statique, nous avons proposé

une deuxième surface de glissement (DISM : double integral sliding mode) en ajoutant un terme de double intégrale de la somme des erreurs du courant et de la tension par rapport à ISM. En agissant ainsi, l'erreur statique de la tension est atténuée, voire supprimée complètement. Par ailleurs, pour simplifier le réglage des paramètres et l'implémentation de l'algorithme, une version simplifiée de DISM a été proposée où les termes de l'intégrale et de la double intégrale n'agissent que sur l'erreur de la tension. Cette simplification se fait au détriment des amplitudes d'oscillation plus importantes en régime transitoire. Les performances de ces trois surfaces de glissement sont comparées et testées en simulation.

Pour valider expérimentalement les algorithmes proposés, un banc de test de SEPIC de 100W dont la fréquence de commutation est à 20kHz est construit. A cette fréquence de commutation, l'utilisation d'un prototypage rapide est possible. Nous avons utilisé une carte DS1104 pour réaliser les algorithmes de commande. Les mesures de tous les états par les capteurs sont disponibles sur ce banc. Les résultats expérimentaux réalisés avec ces capteurs vérifient l'analyse théorique et confirment les résultats observés en simulation. Ils montrent que les commandes DISM, ou DISM simplifiée, permettent d'obtenir des performances satisfaisantes.

Chapitre 4 COMMANDE PREDICTIVE POUR SEPIC

La commande prédictive de type « deadbeat control » est une commande en temps discret qui consiste à déterminer le rapport cyclique qui permet d'atteindre la référence en un nombre minimal de période. Elle présente plusieurs avantages : les concepts sont intuitifs et faciles à comprendre ; elle permet d'obtenir une dynamique très rapide comparée à une commande classique ; sa mise en pratique est relativement facile... Cette technique a été déjà utilisée dans de nombreuses applications, notamment pour les entraînements électriques, les alimentations sans interruption (UPS) et les convertisseurs DC/DC de structure simple. A notre connaissance, l'application de ce type de commande prédictive sur les convertisseurs DC/DC d'ordre élevé n'est pas encore référencée dans les publications. Dans ce chapitre, nous nous proposons d'adapter cette technique de commande pour le convertisseur SEPIC. Notre objectif est de tester la faisabilité, la performance de ce type de commandes et la possibilité de la mise en œuvre dans un système embarqué.

Tout d'abord, un modèle hybride en temps discret de SEPIC est établi afin de fournir un modèle de prédiction pour la commande prédictive. Ensuite, une structure de commande multi-boucles est proposée pour SEPIC avec une boucle interne en courant réalisée par la commande prédictive et une boucle externe qui asservit la tension de sortie en utilisant un simple correcteur PI (proportionnel-intégral). Pour la boucle interne, la réalisation numérique de la commande prédictive induit une période de retard qui peut ralentir la performance dynamique du système si ce retard n'est pas négligeable. Afin de prendre en compte ce retard, un algorithme de commande avec compensation est proposé. Pour les convertisseurs à haute fréquence de commutation, l'implantation numérique de la commande se réalise avec un FPGA. Le problème de retard est moins sensible ou négligeable. Par contre, la complexité d'algorithme est un facteur à prendre en compte. Dans ce cas, nous proposons une simplification de l'algorithme qui réduit considérablement le nombre de calculs. Nous avons réalisé une étude de la robustesse vis-à-vis de la variation paramétrique pour cette dernière commande qui est plus intéressante pour répondre à notre objectif. La stabilité par rapport à la variation des valeurs d'inductance d'entrée est analysée du fait que c'est le seul paramètre présent dans la loi de commande.

Les résultats de simulation sont donnés pour comparer les différents algorithmes proposés. Une comparaison entre la commande prédictive conventionnelle et celle avec une compensation de retard pour un SEPIC fonctionnant à 20kHz confirme que l'algorithme avec compensation présente une performance dynamique en suivi de référence supérieure à celle

de la commande prédictive conventionnelle Des simulations pour un SEPIC à 500kHz montrent que l'algorithme avec simplification donne sensiblement les mêmes résultats que ceux d'une commande prédictive avec compensation.

Enfin, l'algorithme de commande prédictive avec compensation est validé expérimentalement sur le même banc de test à 20kHz que celui du chapitre précédent. Une comparaison avec la commande par modes de glissement la plus performante (DISM1) montre que la dynamique de régulation est un peu meilleure avec la commande prédictive. La validation expérimentale d'algorithme simplifié sera réalisée sur FPGA dans le chapitre 7.

Chapitre 5 SYNTHESE D'OBSERVATEURS

Que ce soient les commandes par mode de glissement ou les commandes prédictives présentées dans les deux précédents chapitres, on suppose que tous les états du système sont accessibles. Dans le banc de test à 20kHz, les états sont mesurés avec les capteurs physiques dans le but de valider convenablement les lois de commande proposées. Ceci n'est pas réaliste pour une application industrielle, en particulier pour les applications embarquées. En effet, mis à part le prix et la place occupée par les capteurs, le nombre de convertisseurs A/D, une grande source de consommation énergétique, augmente avec le nombre de capteur. Afin de supprimer le plus possible le nombre de capteur dans l'objectif de l'intégration du système, la technique d'observateur sera utilisée pour estimer les états à partir de la mesure de tension de sortie. Par ailleurs, étant donné que la variation de la charge est importante et qu'elle a une influence significative sur la qualité de la commande, nous avons proposé d'étendre les observateurs d'état à une estimation en ligne de la charge.

Dans ce chapitre, deux observateurs non linéaires sont présentés. L'un est un observateur par mode de glissement. L'autre est un filtre de Kalman étendu. Dans les deux cas, l'état de charge est ajouté à des variables d'état. Les résultats de simulation sont présentés pour valider les observateurs proposés. Ils montrent que les deux observateurs fonctionnent aussi bien pour le suivi des variations de tension ou pour un grand changement de charge. Pour la mise en œuvre de l'observateur, un observateur à temps discret est plus approprié. C'est la raison pour laquelle l'observateur étendu de Kalman sera utilisé pour l'implémentation finale sur FPGA de l'ensemble des algorithmes proposés.

Chapitre 6 CONCEPTION D'UNE MLI A HAUTE RESOLUTION

Pour réduire la taille des composants passifs et obtenir la miniaturisation du système, la fréquence de commutation doit être augmentée. La vitesse de calcul et la capacité de traiter des algorithmes complexes sont les principaux facteurs pour choisir le processeur numérique lors de la mise en œuvre pratique. Par rapport à des processeurs numériques classiques tels que des DSP et des microcontrôleurs, le FPGA présente des vitesses de calcul beaucoup plus rapides. Par ailleurs, l'utilisation d'un langage de description matérielle (HDL) fournit une plus grande flexibilité pour la programmation. La conception peut ensuite être facilement utilisée par un processus différent, intégré à d'autres systèmes numériques, ou modifiée pour répondre à un nouveau cahier des charges. Toutefois, il n'existe pas de ressources disponibles pour des modules ADC et DAC ou le module MLI dans un FPGA.

Pour une commande numérique (digital control) des convertisseurs, la qualité de commande dépend beaucoup de la résolution de conversion A/D et de la MLI. La partie A/D est réalisée par un composant du marché de 10-bit et ne fait pas partie de l'étude dans cette thèse. On montre que pour éviter le phénomène de cycle limite, la résolution de la MLI numérique doit être au moins à 1 bit au dessus de celle de l'A/D, c'est-à-dire à 11-bit minimum. Par conséquent, notre défi majeur est de concevoir une MLI numérique à 11-bit de résolution tout en utilisant une fréquence d'horloge raisonnable.

Les techniques compteurs-comparateurs sont simples à mettre en œuvre, mais demandent une fréquence d'horloge de plus d'1GHz pour une SEPIC de 500kHz. Récemment, plusieurs solutions ont été proposées pour réaliser des MLI à haute résolution en utilisant des structures matérielles, comme par exemple la ligne à retard (delay line). Une structure « delay-line » de 11-bit nécessite 2048 cellules de retard. Ce qui augmente considérablement la surface silicium. Compte tenu des inconvénients de chaque méthode, nous avons proposé, dans un premier temps, une solution mixte dont 7-bit sont réalisés par la solution compteur-comparateur et 4-bit sont accomplis par la technique « delay-line ». La simulation réalisée avec Xilinx ISE 9.2i montre qu'une horloge de 64MHz suffit pour cette solution, ce qui est faisable. Cependant, la précision des cellules de retard dépend de la température, de la tension d'alimentation et du processus de fabrication. Une grande précision ne peut s'obtenir qu'en utilisant des technologies CMOS inférieures à 0.12- μm qui sont plus chères.

Pour cette raison, nous avons proposé une deuxième solution hybride qui combine un modulateur Δ - Σ de 4-bit, un DCM (Digital Clock Management) segmenté et déphasé et un compteur-comparateur de 3-bit.

Pour le modulateur Δ - Σ , un MASH (Multi-stage-noise-Shaping)- Δ - Σ DPWM qui réunit l'avantage d'un modulateur Δ - Σ du premier ordre et celui d'un second ordre a été développé. Les formes d'onde correspondantes des simulations réalisées sont données afin de valider l'architecture proposée.

Chapitre 7 L'IMPLEMENTATION SUR FPGA

Le but de ce chapitre est de mettre en œuvre sur FPGA l'ensemble des éléments de la commande numérique pour un SEPIC à haute fréquence de commutation. Les lois de commande proposée, l'observateur de Kalman étendu et le module MLI hybride seront implémentés dans une carte FPGA de la famille Xilinx. Comme les calculs doivent être réalisés en virgule fixe, des simulations en entiers à virgule fixe de tous les composants développés sont d'abord réalisées à l'aide de la boîte à outils « fixed point » de Matlab/Simulink. Ensuite, chaque élément de la plate-forme expérimentale pour la mise en œuvre du système de commande numérique SEPIC est décrit. Enfin, les résultats expérimentaux sont donnés pour valider la commande par mode de glissement et la commande prédictive réalisées avec l'observateur Kalman étendu et le modulateur MLI hybride proposés. Ils montrent que l'ensemble du système présente de très bonnes performances avec une dynamique rapide en transitoire et en régulation sans avoir un grand dépassement.

Au niveau des ressources du FPGA utilisées, un bilan a été dressé pour comparer les différents algorithmes de commande. La commande prédictive est celle qui consomme le moins de ressources du fait qu'elle a une architecture de calcul plus simple. Elle constitue un bon candidat pour la conception future en ASIC d'un SEPIC à faible puissance.

CONCLUSION ET PERSPECTIVE

Les principales contributions et conclusion de la thèse sont les suivantes :

- D'abord, trois types de modèle de SEPIC sont établis. Pour le modèle linéaire qui est souvent utilisé pour la synthèse de commande, une analyse fréquentielle a été effectuée en comparant les résultats de simulation avec ceux mesurés expérimentalement à partir de deux circuits réels. Elle montre que le comportement statique et dynamique du SEPIC varie beaucoup avec le point de fonctionnement. L'utilisation d'un modèle non linéaire est préférable pour la synthèse de commande pour SEPIC.
- Basé sur le modèle moyen non linéaire, une commande par mode de glissement à fréquence fixe est étudiée. Trois surfaces de glissement originales sont proposées. Leurs influences sur la performance de commande sont discutées. On note que, pour supprimer l'erreur statique de la tension de sortie, la surface de glissement doit contenir au moins une intégrale et une double intégrale de l'erreur de cette tension. L'ajout de l'erreur du courant de l'inductance d'entrée dans ces intégrales améliore la performance dynamique de la commande, mais le réglage des paramètres du correcteur est un peu plus difficile. De plus, il ajoute une opération en multiplication et en addition dans la loi de commande. Les résultats en simulation et expérimentaux sont testés pour un SEPIC de 20kHz où une carte Dspace est utilisée dans le but de valider les lois de commande proposées.
- Une autre commande étudiée dans cette thèse est la commande prédictive qui présente des caractères intéressants comme implémentation facile, dynamique rapide et robustesse vis-à-vis des variations paramétriques. Nous avons développé un modèle de prédiction en nous basant sur la discrétisation du modèle hybride. En utilisant le principe de la commande mutli-boucle, le courant de l'inductance d'entrée est commandé par la commande prédictive tandis que la boucle externe contrôle la tension de sortie par un simple correcteur PI. Etant donné que la commande introduit un retard d'une période, une commande prédictive permettant de compenser ce retard est proposée. Pour les applications à très haute fréquence où la programmation du FPGA est nécessaire, un algorithme simplifié est donné. La stabilité en fonction de la variation paramétrique est étudiée. Elle illustre une méthode pour analyser la robustesse d'une telle commande. Finalement, les résultats en simulation confirment l'efficacité des algorithmes proposés. Les tests expérimentaux sur la plate forme SEPIC de 20kHz vérifient les bonnes performances de ce type de commande.
- Afin de réduire le nombre de capteurs pour les systèmes embarqués, deux observateurs non linéaires sont présentés pour estimer tous les états à partir de la seule mesure de la tension de

sortie. L'un est un observateur à mode de glissement. L'autre est un observateur étendu de Kalman. Dans les deux cas, la synthèse des observateurs est basée sur un modèle d'état augmenté afin de prendre en compte la variation de la charge. Bien que les deux observateurs offrent de bonnes performances statiques et dynamiques, l'observateur Kalman est préférable pour une implémentation numérique du fait qu'il est synthétisé directement en discret.

- Pour implémenter efficacement la commande numérique sur une plateforme FPGA en haute fréquence, une analyse des difficultés liées au compromis entre la résolution et la fréquence de calcul nous conduit à étudier deux solutions de MLI numérique. La première combine la ligne à retard et la technique de compteur-comparateur. Sa faisabilité est démontrée par une simulation. Cependant, la précision est limitée et est sensible aux conditions externes. Pour cela, nous avons proposé un autre MLI numérique hybride à 11 bits de résolution qui se constitue de DCM segmenté et déphasé à 4-bit, un modulateur Δ - Σ MASH à 4-bit et compteur-comparateur à 3-bit. Cette solution nécessite une fréquence d'horloge de $2^3 \cdot f_{sw}$ au lieu de $2^{11} \cdot f_{sw}$ avec une solution classique.

- La dernière contribution concerne la mise en œuvre de l'ensemble des travaux et de développement sur une plateforme à haute fréquence. Un SEPIC à 500kHz de fréquence de commutation ainsi que les interfaces avec une carte FPGA de Virtex-II sont réalisés. Les deux commandes par mode de glissement DISM, la commande prédictive et l'observateur Kalman étendu sont validés suivant des étapes méthodologiques depuis les simulations jusqu'aux expérimentations. Tous les résultats expérimentaux confirment les excellentes performances statiques et dynamiques de l'ensemble des approches proposées.

En conclusion, ce travail nous a permis de développer et tester des commandes numériques performantes pour un convertisseur DC/DC de faible puissance et à haute fréquence de découpage présentant une forte non linéarité. Les méthodologies développées pour la mise en œuvre sur un FPGA peuvent s'étendre à la commande des autres types de convertisseurs de puissance intégrés ou à d'autres applications embarquées.

Perspective

Ce travail pourrait donner lieu à des études complémentaires dans les directions suivantes :

- Seul le mode de conduction continue CCM a été étudié dans cette thèse. Il est nécessaire de travailler avec les deux modes de conduction continue/discontinue.
- Pour les commandes et les observateurs développés, une étude plus théorique de la robustesse et de la stabilité sont à approfondir afin de garantir théoriquement la stabilité globale du point de vue de l'Automatique.

- En plus des algorithmes de commandes proposés, d'autres stratégies de commande non-linéaires peuvent être étudiées. Par exemple, une commande par passivité présente des potentiels pour la commande de SEPIC. Une autre stratégie de commande prédictive directe qui a été appliquée avec succès sur des entraînements électriques serait intéressante à comparer avec la commande prédictive développée ici.
- Pour une application industrielle plus réaliste, l'implémentation en ASIC des algorithmes proposés doit être envisagée. Pour cela, l'effort doit se concentrer sur la simplification des algorithmes afin de réduire la surface de silicium.
- L'observateur de Kalman étendu développé présente de très bonnes performances d'observation. Cependant, son implémentation sur FPGA n'est pas une tâche facile. Il consomme beaucoup de temps de calcul et de ressources. Pour une implémentation future en ASIC, la fréquence de commutation sera augmentée à l'ordre de quelques MHz ou dizaine de MHz, et un observateur plus simple devrait être étudié.

CHAPTER 1 INTRODUCTION

1.1 RESEARCH INTEREST: UNIVERSAL POWER SUPPLY

With the introduction of the transistor in the early 1950's and, especially, with the development of integrated circuits from the early 1960's onwards (Josephson 1967), designers of electronic equipments, computers and instrumentations have increasingly brought up the demand for smaller and more efficient power sources to supply their equipments. Therefore, to meet these demands, the power supply itself has become more and more significant.

The regulated power supply technology can be divided into two distinct forms: firstly, the linear regulator which can be either a series or parallel regulator, secondly, the switched mode conversion technique. Switched-mode technology is multi-faceted with a wide variety of topologies that provide a regulated DC voltage.

Compared with linear power supplies, Switching Mode Power Supplies (SMPS) provide high efficiency, possible integration, small dimensions and weight. Switching regulators are mostly used for low power and/or high current applications. For example, a modern computer power supply is a switch with "on" and "off" supply designed to convert 110-240 V AC power from the mains supply to several outputs both positive (and historically negative) DC voltages in the range of +12V, -12V, +5V and +3.3V. The first generation of computers power supplies were linear devices, but as cost became a driving factor, and weight became important, the universal switched mode power supplies are used. In addition, SMPS have been widely used in numerous personal communication systems and embedded applications.

With the application of DC/DC SMPS in the new generation of portable systems and embedded applications, the size of DC/DC power converters is becoming the primary focus in the design. For example, the power supply for mobile phones needs to have the advantages of light weight, high efficiency and multi-outputs. The size of the passive components, such as output capacitors, transformers and inductors, is further reduced as the switching frequency of operation increases. Therefore, the size of the heat sink to protect the switching elements can be smaller, if losses are restricted.

Control of SMPSs intended for consumer market has been traditionally achieved through analog means. Nowadays, analog control ICs are available at low price and for a variety of power applications and converter topologies. These controllers typically integrate one or more

error amplifiers, modulation circuitry, a temperature-compensated voltage reference, over-voltage/over-current protections as well as soft-start, standby and automatic shutdown features. Depending on the power rating, gate drivers and power switches may be integrated or left as off-chip components. Surrounding passive circuitry is used to program the controller behaviour, define the shape of the compensator transfer function and provide feedback and sensing interfaces between the chip and the power converter. The analog components are sensitive to the environmental influence, such as temperature, aging, noise, tolerance of fabrication, which results in a lack of flexibility, and low reliability. Besides it is difficult to apply sophisticated control algorithms with an analog approach implementation. In addition, the transmission of analog controller signal through the process will suffer from the limitation of band-width and large gain variation when the switching frequency increases to meet the size miniaturization demand. Therefore analog control is becoming less adequate to meet the complex requirements of higher switching frequency for the reduction of passive components and improvement of control performances of an universal power supply.

Digital solutions, on the other hand, are fairly common in environments where intelligent control strategies for power management are required and fully justify the increased cost of a digital control system. Main advantages of a digital control system over an analog solution are represented by the high degree of programmability and computational power, the reduced need for external passive components and the consequent decreased sensitivity, tolerance to sources of parametric variations, the possibility to implement complex control strategies as well as to easily switch through different modes of operation, targeting for highest efficiency or optimized dynamic performances. System monitoring functions are of extreme importance for high-reliability applications and their implementation strongly point to digital solutions able to collect and process environmental data. Self-tuning, also known as auto-tuning functions allow a digital compensator to adapt its parameters to the specific power plant under control, eliminating the need for manual design or calibration and enhancing controller modularity and versatility.

In general, digital control wins where the algorithm of the operation is too complex for analog implementations [PM05, SGG04, EMZ04, ZSP07]. No analog controller exhibits the same degree of programmability and versatility as a digital controller does. Compensator parameters can be stored in a non volatile memory and loaded in a programmable controller at system power-on. In this way, different sets of pre-calculated parameters can be run for many environmental conditions on the same control hardware. More evolved tuning algorithms

literally perform an automatic design of the compensator parameters through a number of online measurements and post-processing operations.

Depending on the specific requirements and cost/performance tradeoffs, the hardware platform for the digital control system may be based on Application-Specific Integrated Circuits (ASICs), microcontrollers, digital signal processors (DSPs) or microcomputers. In all the described applications the increased cost for a digital control system compared to an analog one has negligible impact on the overall project, and is furthermore justified by the savings that come from the increased system robustness and reliability.

In recent years, however, digital solutions have been proposed in the market of consumer applications. Point-of-load power supplies employed in desktop/laptop computers are examples, along with digital control ICs for multiphase converters employed in Voltage Regulation Modules (VRMs). In this context the competition with analog solutions leads to reconsider the previous statements concerning cost and performances tradeoffs. Rather than pointing to expensive microcontroller or DSP platforms, digital solutions for consumer applications are more prone to ASIC implementations which integrate A/D conversion and pulse-width modulation resources, control hardware, conventional protection circuitry and – depending on the application – communication, system monitoring and auto-tuning functions.

Design of a digital control IC in terms of dynamic capabilities, area and power consumption is a challenging issue and has gained increased attention from the scientific community over the last years [WJMS99, PPZM03, Mul04, MZE04]. Leaving apart mixed-signal solutions, pure digital systems for SMPS control invariably require fast A/D converters and optimized digital pulse-width modulators (DPWMs). Accuracy comparable to analog controllers is achieved only by means of sufficient bit resolution. These factors lead to increase the overall area consumption. Other limitations specifically encountered in digital system include reaction times of the digital controller, which are limited by the sampling rate, as well as quantization phenomena such as limit cycle oscillations.

Feasibility of completely integrated digital controllers was demonstrated for the first time in [PPZM03, PXS03], in which innovative solutions for the main constituents of a digital controller, namely the compensator, the A/D converter and the digital pulse-width modulator are presented. Based on a look-up table structure, the PID compensator employed in [PPZM03] presents reduced complexity. Delay-line and windowed ADCs are used in these works for fast conversion times and small area requirements. A ring oscillator-multiplexer DPWM is implemented in [PXS03], while in [PPZM03] a hybrid counter/delay line architecture is considered as a suitable tradeoff between resolution, area and power

consumption. Further works in the area exploit ring-oscillator ADCs [ZS07, XPZS04] and other hybrid DPWM structures. Further examples of DPWM architectures can be found in [OR04, SAM04, CZM06, YWMP04]. Recently, high frequency digital control application to buck converters has been studied more and more widely. DPWM operation has been paid more and more attention, for most applications. Digital linear controllers are adopted and the on-chip implementation has been realised [SAM04, WRLP06, IAKR04]. In contrast, due to the complex topologies, high-order converters like Single-Ended Primary Inductance Converter (SEPIC) demand sophisticated control algorithms, and the need of state measurements bring more difficulty to the integration realization.

1.2 MOTIVATION AND BACKGROUND

The switching mode DC/DC power conversion system can be realized by different circuit topologies [DeFFG08]. Among them the buck, boost, buck-boost and Cuk converter are the basic and the mostly used. Each of the circuit has its advantages and disadvantages and the choice depends on requirements for power conversion system. In general, circuits with the switch referenced to the ground node are preferred to simplify the switch drive circuits. Additionally, the non-pulsating input current is desirable to minimize EMI and reduce the need for additional filter elements. Significant advantage of the power conversion system is also its ability to generate output voltage either above or below the input voltage.

SEPIC topology is the one that fulfils all above requirement (Figure 1-1). The output voltage of the SEPIC is controlled by the duty cycle of the control transistor M1. The output voltage can be greater than, less than, or equal to the input voltage. The buck-boost converter can also step up and step down the input voltage, but the output is inverted. The SEPIC converter can maintain the same polarity and the same ground reference for the input and output. Other advantages of SEPICs are the input/output isolation provided by C_1 and true shutdown mode, when the switch is turned off output drops to 0 V. Besides, it has small input current ripple and easy to extend the multiple-output.

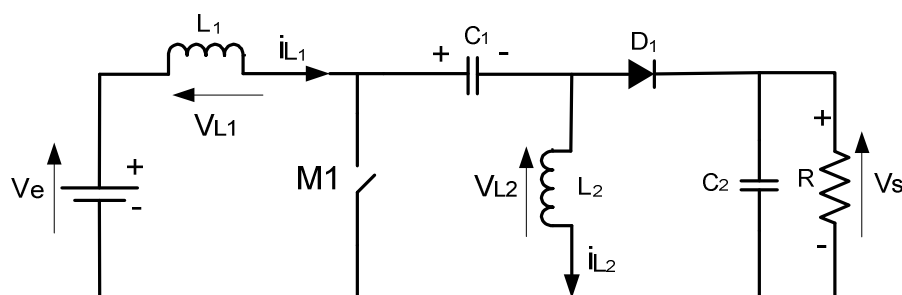


Fig. 1-1 SEPIC schematic

SEPICs are useful in applications where the battery voltage can be above or below the regulator output voltage. It has become popular in recent years in battery-powered systems that must step up or down voltage depending upon the charge level of the battery. For example, a single lithium ion battery typically has an output voltage ranging from 4.2 volts to 2.7 volts. If the load requires 3.3 Volts, then the SEPIC would be effective since the battery voltage can be both above and below the regulator output voltage.

SEPICs also find their applications in the power supplies for power-factor converters (PFCs). Most of such circuits use a simple step-up converter as the input stage, implying that the output stage must exceed the peak value of the input waveform.

The SEPIC is still rarely studied in DC/DC converters for high-frequency SMPS. Being of forth-order system, the SEPIC behaviour is severely nonlinear and depends on operating conditions and load variations. Moreover, the application of control techniques to SEPIC topology leads to difficulties in the design of control parameters for the stabilization of the converter.

PID controllers are widely used for DC/DC digital converters. It can be designed easily for DC/DC converters where the controller parameters are deduced from the approximated small signal model. Their implementation is simple, a so-called Look-up Table PID [[PXS03](#), [SAMA04](#), [PPZM03](#), [TM06](#)] is typically employed to reduce area and/or clock frequency in ASIC standard implementation. However, linear control approaches require a good knowledge of the system and accurate tuning in order to obtain the desired performances. Their performances generally depend on the operating point, so that the presence of parasitic elements, time-varying loads and variable supply voltages can make difficult the selection of the control parameters which ensure a proper behaviour in any operating conditions. Achieving large-signal stability often calls for a reduction of the useful bandwidth which affects the converter performances. Moreover, application of these control techniques to high-order DC/DC converters, e.g. SEPIC topologies, may result in a very critical design of control parameters and difficult stabilization.

The failure of conventional linear control schemes to operate satisfactorily in large signal operating conditions is the main motivation driving the research about nonlinear control methods for high order DC/DC converters.

Nonlinear controller design techniques proposed for SEPIC is rarely reported. A general-purpose fuzzy controller for DC/DC converters is investigated in [[MRST93](#)], for buck-boost and SEPIC. The fuzzy control is a type of heuristic reasoning based on expert knowledge

automatic control method. It does not require a precise mathematical modelling of the system nor complex computations. The control design is simple since it relies on human capability to understand the system behaviour. The works on developing neural network control for SEPIC is reported in [WXD08]. An artificial neural network (ANN) is an information processing method that is inspired by the way of biological nervous systems process information. The main advantage of applying the ANN in the control of SEPIC lies in its intrinsic capability to learn and reproduce highly nonlinear transfer function that enables the control to be done effectively for large-signal conditions. Lyapunov-based control proposed in [ZZQ07] for SEPIC achieves the properties of robustness around the operating point, and good performance of transient responses can be obtained.

However, it is found that the main problems with the application of these controllers are that they consume a lot of memory and processing time to run. Consequently, it's difficult to implement these controllers for high frequency applications.

Sliding-Mode-Control (SMC), a form of the large group of Variable Structure System (VSS) controller was theoretically introduced a few decades ago. SMC offers an alternative way to implement a control action which exploits the inherent variable structure nature of SEPIC converters [MRST95, MRST93]. This control technique offers several advantages. Its major advantages are the guaranteed stability and the robustness against parameter and load uncertainties [UGS99]. Moreover, being a controller that has a high degree of flexibility in its design choices, the SMC is relatively easy to implement as compared with other types of nonlinear controllers.

Despite being a popular research subject, SMC is still rarely applied in practical SEPIC converters. First, unlike classical PID controllers, SM controllers are not available in integrated-circuit (IC) forms for power-electronic applications. Second, there is a strong reluctance to the employment of SM controllers in power converter because of their inherently high and variable switching frequency, which causes excessive power losses, electromagnetic-interference (EMI) generation, and filter design complication. Third, all discussions regarding the usefulness and advantages of SM controllers have been theoretical so far. The practical worthiness of using SM controllers is generally unproven. These explain why the application of SM controllers to SEPIC has only been of academic/research interest but of little industrial value.

Literature about SEPIC studies is pretty thin. Moreover, most of the designs remain in the simulation stage or in the implementation into DSP where the switching frequency is about some ten kHz which is unpractical in high frequency application (hundred kHz or MHz).

1.3 RESEARCH OBJECTIVE

In the research reported in this thesis, our goal focuses in the issue of digital control of SEPIC converter and its practical implementation at high-frequency embedded (Field-programmable Gate Array (FPGA), ASIC) platform where the switching frequency can reach some hundred kHz or more. The design of a digital controller for high-frequency SEPIC focuses on two areas. The first one is to develop high efficient digital control algorithms that can achieve good performance and be easy to realize. The second one is to efficiently implement digital controllers in a high-frequency embedded (FPGA, ASIC) platform where size and energy consumption are important factors.

1.3.1 Control Objectives

For the controller design, the challenge is to develop the most suitable control methods which are implementable on FPGA or ASIC platform and can overcome the main problems arising and affecting the performances of the SEPIC converter.

These problems are:

- Non-linearity due to the non-linear components in the structure of the converter;
- Stability in steady-state and under line and load variations;
- Reduction of the cost by reducing the components such as sensors and A/D converters;
- Reduction of Silicon surface by limiting the algorithm complexity.

In this thesis, two kinds of control have been developed. The first one is a fixed-frequency PWM-based Sliding-Mode-Control. The second one is a predictive control based on a discrete time prediction model. These controllers can improve the dynamic performance, reduce the effect of disturbances (notably load variation), and they are less effected by component variation compared to linear control approaches. They are relatively easy to implement compared with other types of nonlinear controllers which is very useful since the complex control algorithms would cause large resources consumption and may not be realised, when it is applied to high-frequency digital processors.

1.3.2 Integration Objectives

Fig. 1-2 illustrates a digitally controlled SEPIC block diagram which typically consists of an analog/digital converter (ADC), a digital control law and a DPWM generator.

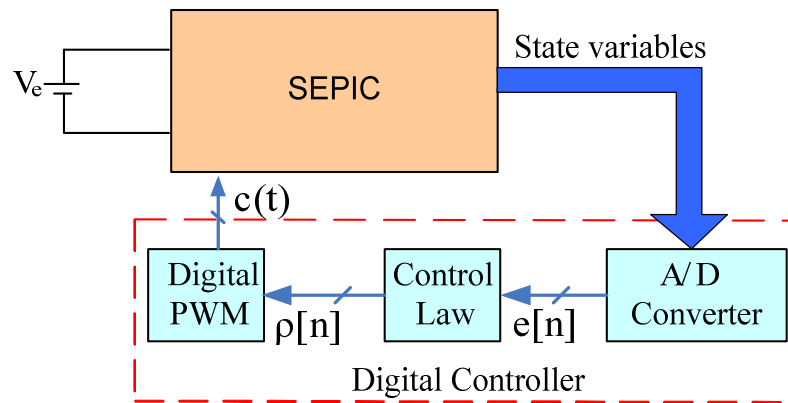


Fig. 1-2 Block diagram of a digitally controlled SEPIC

Large research attention has been paid to improve the performance of ADC. An overview of ADC design in low-power high-frequency digitally controlled SMPS has been given in [SGG04]. In our thesis, the issue of ADC technique will not be re-discussed.

For the digital control law, apart the issue of the performance of control law for a nonlinear fourth order system as underlined in the control objectives, there are some issues to be considered in practical implementation such as algorithm complexity, computation speed and sensor number. For example, the division and square root operations are delicate to be implemented in Very-high-speed Hardware Description Language (VHDL) and increase considerably the equivalent gate number in hardware implementation. Also the controllers developed in this thesis require the knowledge of one part or all of the system states. Due to size and energy consumption factors, sensor number must be limited. For high frequency SEPIC case, only the output voltage is measured. An observer technique must be adopted to estimate the other states. The challenge is to implement efficiently the designed controllers and observer by taking into account the constraints of embedded systems.

The last key issues focus on the design of high-resolution DPWM. To meet the output voltage accuracy requirement, a high resolution DPWM is required to eliminate limit cycle oscillations on output voltage [PM02, TM06]. However the increase in DPWM resolution implies the increase in system clock frequency which reflects the power consumption of the digital control system in future ASIC implementations. The main goal is to generate high-frequency high-resolution PWM signals with low frequency hardware clock and to implement the high-performance digital control-law at low-power consumption.

1.4 THESIS STRUCTURE

The thesis is organised as follows:

In order to analyse the SEPIC behaviour and design its corresponding controllers, an appropriate modelling for SEPIC is required. Chapter 2 proposed three kinds of modelling. First, a hybrid model of SEPIC which can accurately describe the switch characteristics of SEPIC is presented. Then, an averaged state space model is established by averaging the state variable. By linearizing the averaging state space model around an operating point, a small signal model is obtained which can be used for linear analyses or linear control design.

After an introduction of sliding mode control principle, Chapter 3 introduces a fixed-frequency PWM-based digital SMC for SEPIC converter. A detailed study for the choice of the sliding surface is defined and compared. Simulation results are shown to validate the different designs of sliding mode control. Finally, the proposed control algorithms have been implemented on a platform based on dSPACE to validate experimentally the proposed control laws.

Chapter 4 presents the current mode predictive deadbeat control for SEPIC. More specifically, the proposed solution is based on a multi-loop structure with an internal deadbeat current control, which highlights a simple algorithm and an outer voltage control with fast dynamic response. For DSP implementation, to compensate the time delays due to digital control computation, a compensated deadbeat current control algorithm is proposed. For high speed applications like FPGA implementation, a simplification of algorithm is developed. Simulation and experimental results confirm the properties of the proposed approaches.

The proposed controls require the knowledge of all the system states. For the high frequency SEPIC application, only the output voltage is measured. For saving the use of sensors and for improving the robustness against load variation, sliding mode observer and extended Kalman observer which allow to estimate all the states and the load from the output voltage measurement are presented in chapter 5. Simulation results are performed to show the effectiveness of the proposed observers.

For the practical implementation of the digital controller, issues such as resolution of DPWM are detailed in Chapter 6. In order to develop an architecture of low-power digital PWM controller for SEPIC that can operate at programmable constant high-switching frequencies, two kinds of 11-bit high-frequency hybrid DPWM architectures are proposed. One is a hybrid delay-line DPWM which adopts hardware methods. The other is a hybrid

Delta-Sigma (Δ - Σ) DPWM which combines software and hardware methods. The feasibility of these two DPWM is demonstrated by simulation on FPGA.

Chapter 7 presents the practical FPGA implementation of the proposed digital controllers in high-switching frequency SEPIC. A/D board, FPGA board and test bench are described. The proposed DPWMs along with the proposed extended Kalman observer, SMC and predictive controllers are implemented in a Xilinx FPGA. Experimental results with constant switching frequency of 500kHz validate the functionality of whole of the proposed digital controller.

Finally, Conclusions and perspectives are given.

CHAPTER 2 SEPIC MODELLING

Modelling of DC/DC converter has been widely studied through the past decades [GLA10]. Many mathematical modelling methods have been established for power converters. However, each method best fits the converter from a certain point of view, i.e., some models are more suitable for circuit analysis whereas others for control. The implementation of control laws and algorithms requires very accurate models that represent, to a great extent, the behaviour of an electronic circuit. This issue has been the most challenging task for power electronics and control engineers and researchers.

Among different control theories, each one requires a certain mathematical model. In this chapter, after a brief description of SEPIC operation principle, three models are presented: hybrid model for numerical simulations, state space averaging model for nonlinear sliding mode control and small-signal model for frequency-domain characterisation and/or for linear control design. Frequency responses of the small-signal are verified with experimental results of a real circuit for a nominal operating point. The evolution of this model versus the operating points is studied. The operating conditions of two SEPIC circuits are discussed.

2.1 SEPIC TOPOLOGY

The Single-Ended Primary Inductance Converter (SEPIC) shown in Figure. 2-1(a) is built using the boost converter topology and by inserting a capacitor C_1 between the inductor L_1 and the diode D_1 . This capacitor obviously blocks any DC current path between the input and the output. However, the anode of the diode D_1 must be connected to a defined potential. This is accomplished by connecting D_1 to ground through a second inductor L_2 . This inductor L_2 can be separated from L_1 or wound on the same core.

The amount of energy exchanged is controlled by switch M1, which is typically a transistor such as a MOSFET. The two different circuit configurations depending on the state of the switch M1 for the case of continuous conduction mode (CCM) are shown in Fig. 2-1(b) and Fig. 2-1(c).

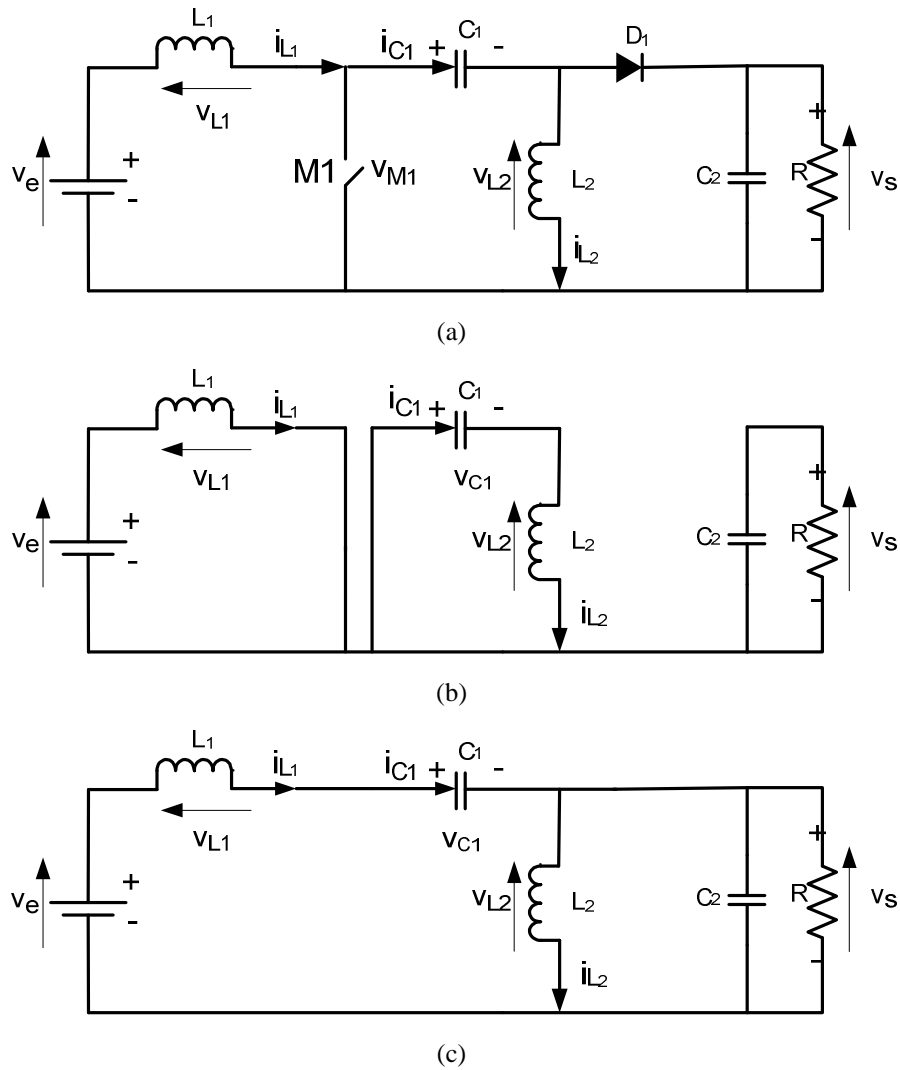


Fig. 2-1 SEPIC schematic (a) SEPIC converter circuit, (b) Equivalent circuit when M1 is ON, (c) Equivalent circuit when M1 is OFF

During a SEPIC's steady-state operation and neglecting the voltage ripple, the average voltage across capacitor C_1 (v_{C1}) is equal to the input voltage v_e . Based on this consideration, we can now easily deduce the voltages in this circuit as shown in Figure 2-2. When M1 is on, and looking to Figure 2-1(b), the voltage across the inductance L_1 is equal to the input voltage v_e . As for the voltage across the inductance L_2 , it is equal to $-v_{C1}$. The energy is being stored into the inductance L_1 from the input. At the same time, the capacitor C_1 feeds the inductance L_2 . So the energy inside the inductances is being increased in this period.

When M1 is off, and looking to Figure 2-1(c), the voltage across the inductance L_2 is the same as the output voltage. In the other side, the voltage across M1 is equal to $v_e (v_{C1}) + v_s$ (v_{L2}). So as far as the voltage of L_1 is considered, it is equal to v_s . This period is characterised by the increase in the energy inside the capacitors. However, as the inductor current never falls to zero, it continues to supply the circuit.

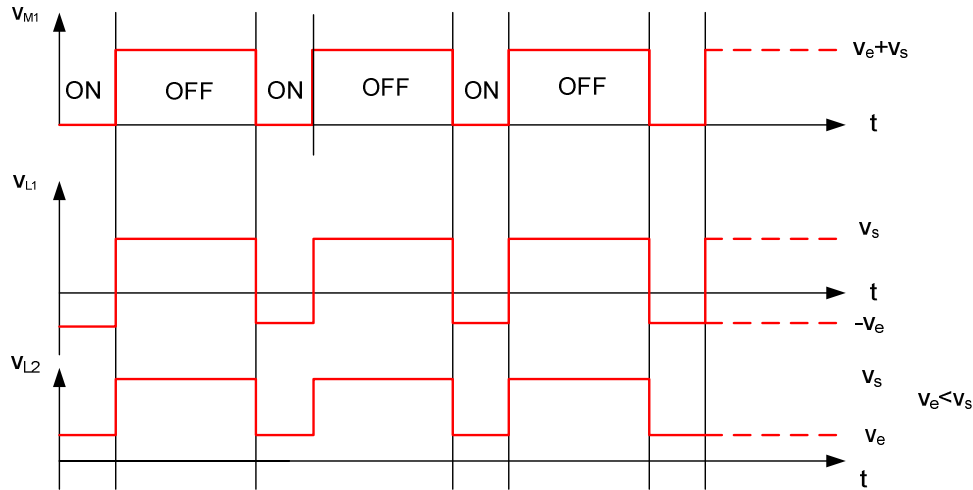


Fig. 2-2 The SEPIC operating mode of component voltages

Because capacitor C_1 blocks the direct current, the average current across the device (i_{C1}) is zero, making inductor L_2 the only source of load current. Therefore, the average current through inductor L_2 (i_{L2}) is the same as the average load current and hence independent of the input voltage.

Since the voltage across the capacitor C_1 is equal to the input voltage, the output voltage is equal to the difference between v_{M1} and v_e . So the output voltage is controlled by the voltage v_{M1} . To have a boost operation (output voltage greater than the input voltage), the voltage across M1 which is controlled by the duty cycle must be greater than twice the input voltage. For buck operation, the voltage across M1 must be less than twice the input voltage. Depending on whether or not the inductor current L_1 falls to zero, the converter will operate in either continuous or discontinuous conduction modes. In this thesis, only CCM is considered. The assumption in term of control is discussed through out the next chapters.

2.2 SEPIC MODELS

2.2.1 Hybrid Model

The term hybrid in the field of dynamic systems is generally applied to systems whose dynamics are characterized by discrete switching among multiple continuous regimes [GLA10, ZRG03]. Continuous-time dynamics are often obtained from physical laws and represent the variations of physical quantities, such as current, voltage, temperature, pressure, etc. Discrete-dynamics are normally switching phenomena that are generated by logic devices, such as switches, digital circuits or software codes. Power electronic converters have been always well known as a type of circuits with big difficulties to be modeled.

Because differential equations that describe them have discontinuities [ZRG03], they are the best examples of hybrid systems. The continuous behaviour of power electronics circuits, such as current and voltage waveforms are generated by the passive elements. Switching devices, such as MOSFETs and IGBTs generate controlled switching actions, however, diodes are sources of uncontrolled switching phenomena.

It is a straightforward task to formulate the hybrid model for the SEPIC. Note that unlike the other modelling techniques, the hybrid model captures the behaviour of the circuit [VRGL10]. In another word, the hybrid model is an accurate model which can describe the dynamic characteristics of the real system except the transient behaviour at the exact time of switchings.

As show in Fig. 2-1, the SEPIC is controlled by its switch (MOSFET). The transistor and the diode are assumed to be ideal so that there is no voltage drop when they are on. We will consider in our work that the converter operates in CCM, i.e., the diode current i_{D1} never drops to zero within the “OFF” time of the MOSFET. This assumption leads to two different circuit states since the switch commutates between “ON” and “OFF”. By assuming that ESR and ESL of capacitances C_1 and C_2 are negligible, the two state space representations can be written as:

State “ON” ($u=1$)

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{v}_{C1} \\ \dot{i}_{L2} \\ \dot{v}_s \end{bmatrix} = \begin{bmatrix} -\frac{r_{L1}}{L_1} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_1} & 0 \\ 0 & -\frac{1}{L_2} & -\frac{r_{L2}}{L_2} & 0 \\ 0 & 0 & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \\ i_{L2} \\ v_s \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} [v_e] \quad (2.1)$$

State “OFF” ($u=0$)

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{v}_{C1} \\ \dot{i}_{L2} \\ \dot{v}_s \end{bmatrix} = \begin{bmatrix} -\frac{r_{L1}}{L_1} & \frac{-1}{L_1} & 0 & \frac{-1}{L_1} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & -\frac{r_{L2}}{L_2} & \frac{1}{L_2} \\ \frac{1}{C_2} & 0 & \frac{-1}{C_2} & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \\ i_{L2} \\ v_s \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} [v_e] \quad (2.2)$$

The state space matrices are calculated by taking into account parasitic losses, represented by the ESRs r_{L1} and r_{L2} of the inductances.

The two state space models ($u=0$ or 1) can be written:

$$\begin{cases} \dot{x} = A_1 x + B_1 v_e \\ y = c_1^T x \end{cases} \quad (2.3)$$

$$\begin{cases} \dot{x} = A_2 x + B_2 v_e \\ y = c_2^T x \end{cases} \quad (2.4)$$

Where $c_1^T = c_2^T = [0 \ 0 \ 0 \ 1]$, and v_e is the input voltage and x the state vector given by:

$$x = [x_1 \ x_2 \ x_3 \ x_4]^T = [i_{L1} \ v_{C1} \ i_{L2} \ v_s]^T \quad (2.5)$$

The elements of the matrices A_1 , B_1 , c_1 , A_2 , B_2 and c_2 are composed of the circuit components, ESRs and the load resistance R .

By introducing the discrete variable $u=\{0,1\}$ in the state space representations, (2.1) and (2.2) can be written as:

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{v}_{C1} \\ \dot{i}_{L2} \\ \dot{v}_s \end{bmatrix} = \begin{bmatrix} -\frac{r_{L1}}{L_1} & \frac{u-1}{L_1} & 0 & \frac{u-1}{L_1} \\ \frac{1-u}{C_1} & 0 & \frac{u}{C_1} & 0 \\ 0 & -\frac{u}{L_2} & -\frac{r_{L2}}{L_2} & \frac{1-u}{L_2} \\ \frac{1-u}{C_2} & 0 & \frac{u-1}{C_2} & -\frac{1}{C_2 R} \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \\ i_{L2} \\ v_s \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} [v_e] \quad (2.6)$$

This is clearly a hybrid non-linear model of the form $\dot{x} = f(x, u) + g v_e$ where the system behaviour is represented by continuous and discrete variables.

The control of a switched mode power converter considered as a hybrid system is an active area of research both in power electronics and automatic control theory. The main difficulty is due to their hybrid nature as the circuit topology changes depending on different modes of operation each with its own associated linear continuous-time dynamics.

2.2.2 Averaged State Space Model

The best popular mathematical model for the converter control design is the averaged model. This kind of modelling consists in combining all the dynamics of the subsystems of a hybrid system using the average value of the state vector. It is assumed that the natural frequencies of the converter are much smaller than the switching frequency f_{sw} .

The average state space model in CCM is obtained by averaging the state space matrices of the “ON” and “OFF” phases of the switch over a period $T_e=1/f_{sw}$. By defining the duty cycle “ ρ ”, the averaged state space model of the SEPIC is obtained as:

$$\begin{cases} \dot{x} = (\rho A_1 + (1-\rho)A_2)x + (\rho B_1 + (1-\rho)B_2)v_e \\ y = (\rho c_1^T + (1-\rho)c_2^T)x \end{cases} \quad (2.7)$$

or

$$\begin{cases} \dot{x}_1 = -\frac{r_{L1}}{L_1}x_1 + (\rho-1)\frac{1}{L_1}x_2 + (\rho-1)\frac{1}{L_1}x_4 + \frac{1}{L_1}v_e \\ \dot{x}_2 = (1-\rho)\frac{1}{C_1}x_1 + \frac{\rho}{C_1}x_3 \\ \dot{x}_3 = -\frac{\rho}{L_2}x_2 - \frac{r_{L2}}{L_2}x_3 + (1-\rho)\frac{1}{L_2}x_4 \\ \dot{x}_4 = (1-\rho)\frac{1}{C_2}x_1 + (\rho-1)\frac{1}{C_2}x_3 - \frac{1}{RC_2}x_4 \\ y = x_4 \end{cases} \quad (2.8)$$

As ρ is the control signal, the state space averaging model of SEPIC is clearly a bilinear model. It is capable of representing the system not only in the neighbourhood of an equilibrium point, but also within a large range of operation. Most nonlinear controllers are based on this bilinear model representation.

2.2.3 Linear Model

Small-signal modelling is a common analysis technique in electrical engineering which is used to approximate the behaviour of nonlinear devices with linear equations [KNM95]. From the previous nonlinear model, a small-signal linear model of SEPIC can be obtained by linearization around an operating point. From a control point of view, the linear model of the SEPIC is used in order to study and analyse the system behaviour around an operating point and to design a linear control law, like PID control, current programmed control, etc.

By assuming that the variables are perturbed around a steady-state operating point:

$$\begin{cases} x = X + \tilde{x} \\ \rho = D + \tilde{\rho} \\ v_e = V_e + \tilde{v}_e \\ y = Y + \tilde{y} \end{cases} \quad (2.9)$$

where X , D , V_e and Y represent steady-state values, \tilde{x} , $\tilde{\rho}$, \tilde{v}_e and \tilde{y} represent small-signal values.

The steady-state values can be obtained by setting the derivative of the steady-state component to zero:

$$\begin{cases} \dot{X} = AX + BV_e = 0 \\ Y = c^T X \end{cases} \quad (2.10)$$

Where $\begin{cases} A = DA_1 + (1-D)A_2 \\ B = DB_1 + (1-D)B_2 \\ c^T = Dc_1^T + (1-D)c_2^T \end{cases}$

The steady-state components of the state variables and output variables are respectively:

$$\begin{cases} X = -A^{-1}BV_e \\ Y = -c^T A^{-1}BV_e \end{cases} \quad (2.11)$$

Substituting steady-state and small-signal quantities into (2.7), we obtain:

$$\begin{cases} \dot{\tilde{x}} = [A_1(D + \tilde{\rho}) + A_2(1 - D - \tilde{\rho})](X + \tilde{x}) + [B_1(D + \tilde{\rho}) + B_2(1 - D - \tilde{\rho})](V_e + \tilde{v}_e) \\ \tilde{y} = c_1^T(X + \tilde{x})(D + \tilde{\rho}) + c_2^T(X + \tilde{x})(1 - D - \tilde{\rho}) \end{cases} \quad (2.12)$$

Considering that the products of small-signal terms $\tilde{x}\tilde{\rho}$ and $\tilde{v}_e\tilde{\rho}$ can be neglected, an overall small-signal dynamic model is obtained as:

$$\begin{cases} \dot{\tilde{x}} = A\tilde{x} + B\tilde{v}_e + [(A_1 - A_2)X + (B_1 - B_2)V_e]\tilde{\rho} \\ \tilde{y} = c^T\tilde{x} + (c_1^T - c_2^T)X\tilde{\rho} \end{cases} \quad (2.13)$$

These equations describe how small ac variations in the input vector and duty cycle stimulate variations in the state and output vectors.

The small-signal model is linear and it is easily used in linear tools to perform analyses of the system. In order to find out the degree of correlation between a real circuit and its small-signal model, the measured open loop frequency response is compared with that of the small-signal model.

Two real SEPIC circuits have been designed in this dissertation: the first one operates at 20kHz which can work with a DSP system for control strategy tests and the second one operates at 500kHz which is adapted for FPGA environment. Specifications and component values are given in Table 2-1 and Table 2-2.

Table 2-1 SPECIFICATIONS AND COMPONENTS of 20kHz

Specifications		Components	
P_{\min}	10W	L_1	2.3mH
P_{\max}	100W	L_2	330 μ H
V_{\min}	15V	C_1	190 μ F
V_{\max}	25V	C_2	190 μ F
V_{ref}	20V	r_{L1}	2.134 Ω
f_{sw}	20kHz	r_{L2}	0.224 Ω

Table 2-2 SPECIFICATIONS AND COMPONENTS of 500kHz

Specifications		Components	
P_{\min}	10W	L_1	185 μ H
P_{\max}	100W	L_2	13 μ H
V_{\min}	10V	C_1	7.6 μ F
V_{\max}	20V	C_2	7.6 μ F
V_{ref}	14V	r_{L1}	1.2 Ω
f_{sw}	500kHz	r_{L2}	0.8 Ω

Since data acquisitions and treatments in FPGA are more difficult than in DSP, the open loop frequency analyses have been only performed for the 20kHz circuit.

To do that, a variable frequency sinusoidal signal is applied around a value of the duty cycle while the input voltage and the load resistance are maintained constant.

For an operating point with the values of $V_e=20\text{V}$, $D=0.5$ and $R=22\Omega$, the Bode diagram of the output voltage to duty cycle transfer function are compared in Fig. 2-3.

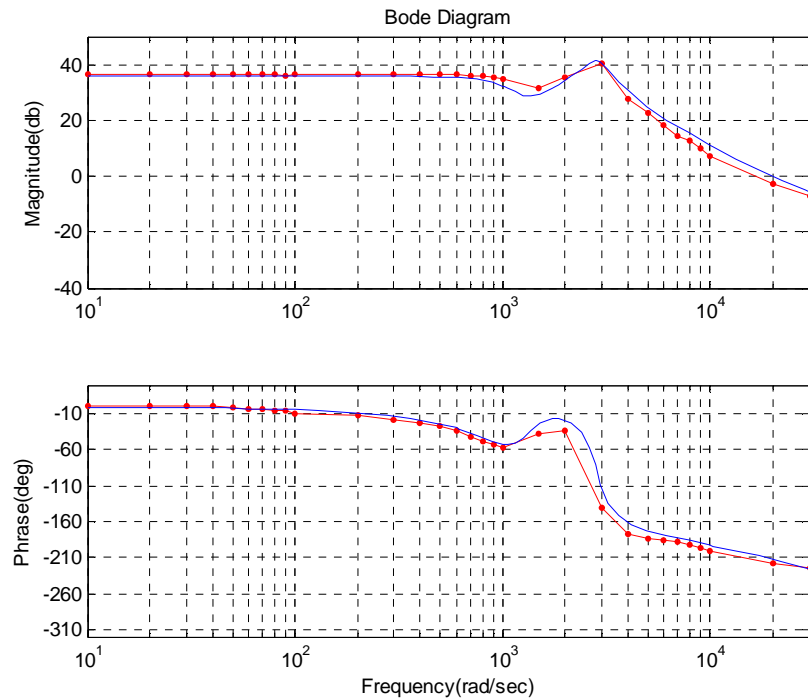


Fig. 2-3 Frequency response of the small-signal model (smooth curve) and measured response (joined dots)

It can be seen that there is a good correlation between the linear model (smooth curve) and the results of the experimental test (joined dots) for the same operating point, where the same behaviour (resonance peaks) is attained. This model is considered as a nominal model which can be used for linear control design.

To know the evolution of the characteristics of the system when the operating conditions change, we have changed the operating point in the linear model for different values of D and R respectively while the input voltage is maintained at $V_e=20V$. Two tests have been performed: the first one consists of varying the duty cycle from 0.35 to 0.7 with a load resistance of 22Ω ; the second one varies the load resistance from 10Ω to 45Ω with a duty cycle of 0.5. Fig. 2-4 and Fig. 2-5 show the simulated converter frequency responses and the evolution of the zeros in the first case. The arrows in both figures show the direction of the evolution of zeros by increasing the values of D . In Fig. 2-4, it can be seen that the resonance frequency is still the same. However, over a threshold value of D , the profile of the phase response widely changes and that of the magnitude response drops significantly. Fig. 2-5 shows that there is one real zero which is always unstable and two complex conjugate zeros which are stable for low values of D . Fig. 2-5(b) indicates that as D increases, the complex zeros become less stable until the value of about 0.68 where it becomes unstable (having a positive real part). This can complicate the design of linear control [Vor06].

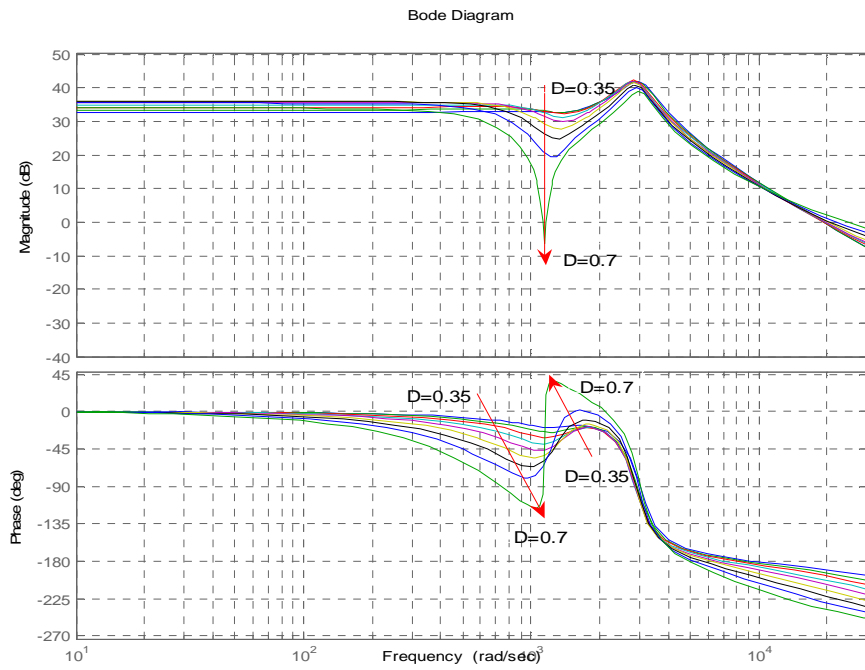
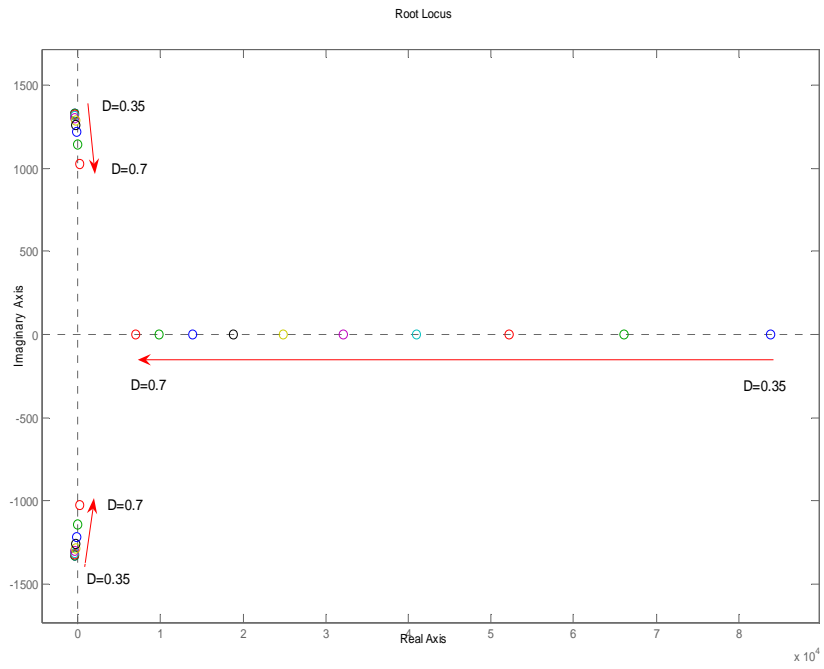
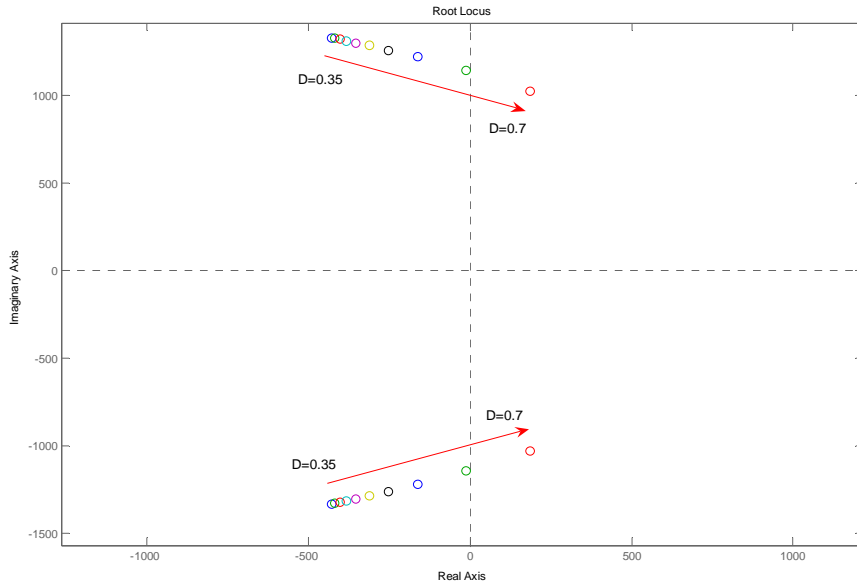


Fig. 2-4 Frequency response under duty cycle variation



(a)



(b)

Fig. 2-5 Evolution of the zeros in the case of duty cycle variation (a) real part and complex pair of zeros (b) zoom on the complex pair of zeros

Fig. 2-6 and Fig. 2-7 show the simulated converter frequency responses and evolution of the zeros in the cases 2. The arrows in both figures show the direction of the evolution of zeros by increasing the values of R . Fig. 2-6 shows that the magnitude and phase profiles remain the same while the load varies (slightly change their curvatures). A variation of magnitude of about 7dB is inside the large part of the system's bandwidth. Fig. 2-7 illustrates the permanent stability of the complex pair and indicates an increase in its stability as R increases.

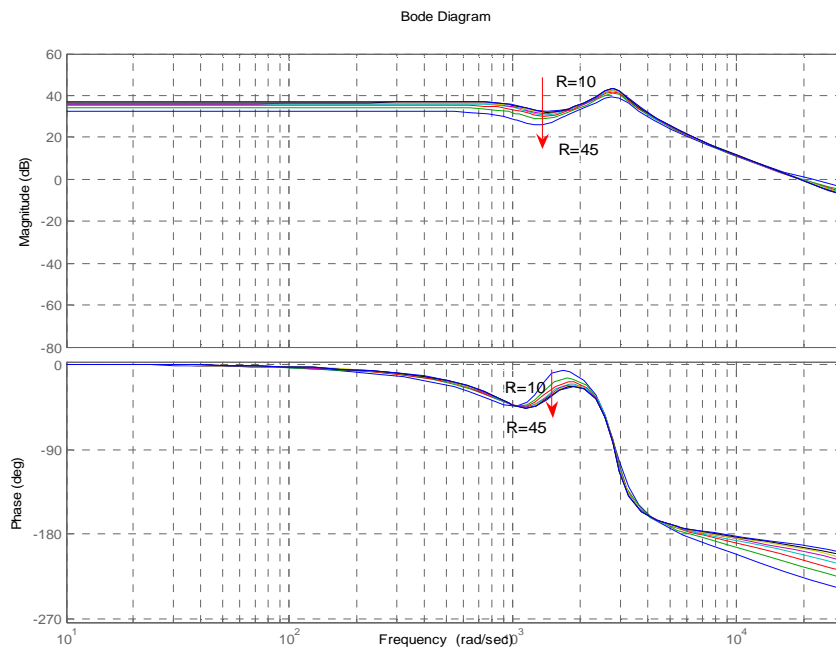
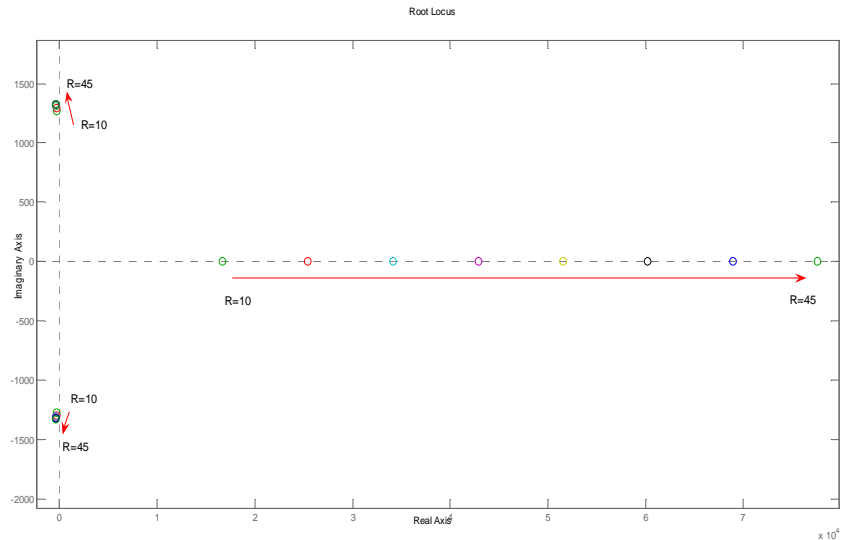
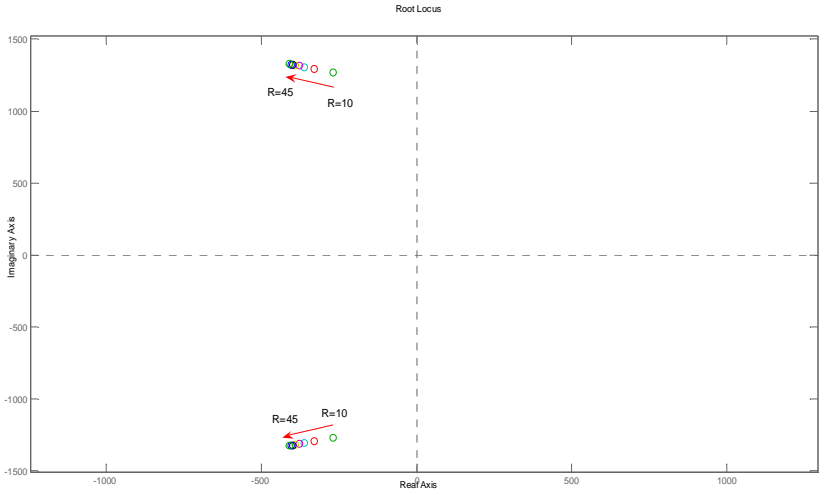


Fig. 2-6 Frequency response of load variation



(a)



(b)

Fig. 2-7 Evolution of the zeros in the case of load variation (a) real part and complex pair of zeros (b) zoom of the complex pair of zeros

The analysis reveals that the linear model when valid for one operating point can not cover large domains of operating conditions, because the frequency response profile significantly changes. Linear control laws designed with the nominal model will be difficult as the number of unstable zeros changes with operating conditions.

Hence, nonlinear control strategies are much more suitable since these controllers are synthesized using nonlinear mathematical models of the system which can cover a large signal domain.

2.3 SEPIC WORKING CONDITIONS

As mentioned in 2.1, only CCM of SEPIC is considered in this dissertation. In order to study the boundary conditions between CCM and DCM which impose duty cycle constraints which are important for the control design, an analytic study of the boundaries among different operation modes is established to have a better appreciation of the working condition of SEPIC. For this, we introduce the static characteristics of SEPIC using linear small-signal models.

The limit between discontinuous and continuous modes is reached when the inductor current falls to zero exactly at the end of the commutation cycle. If we were to stay in CCM, a boundary condition or a lower limit for D can be determined by a static analysis. This boundary expression depending on the elements of the circuit can be expressed as:

$$D_{\text{boundary}}(R) = 1 - \sqrt{\frac{2f_{\text{sw}}L_1L_2}{R(L_1 + L_2)}} \quad (2.14)$$

Using the small-signal model, the expression of the gain can be written as:

$$\frac{V_s}{V_e} = \frac{(1-D)DR}{(D-1)^2R + r_{L2} - 2Dr_{L2} + D^2(r_{L1} + r_{L2})} \quad (2.15)$$

It depends on the load resistance, R , and the ESR r_{L1} and r_{L2} . The evolution of $\frac{V_s}{V_e}$ with respect to D for different values of R is shown in Fig. 2-8 for the 20kHz SEPIC. In the ideal case where the ESRs are neglected, (2.15) is simplified to $\frac{V_s}{V_e} = \frac{D}{1-D}$ (dash line).

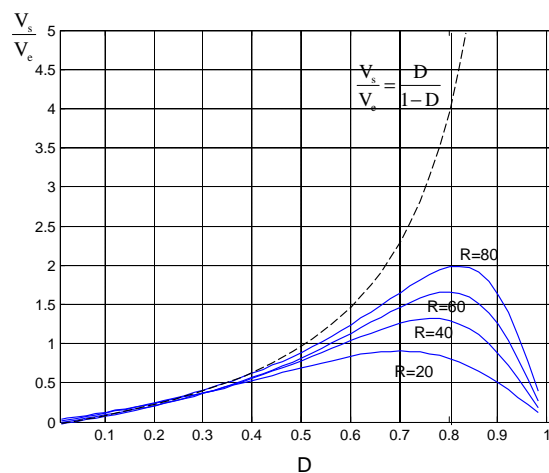


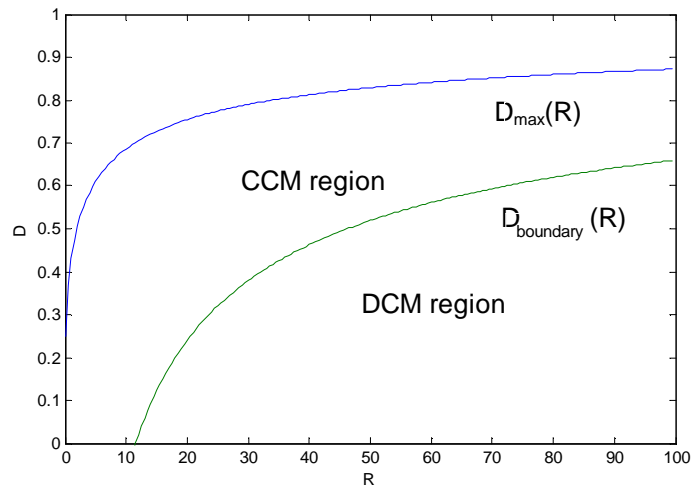
Fig. 2-8 Evolution of V_s/V_e for different values of R

It can be seen that with the ESRs, $\frac{V_s}{V_e}$ has a maximum value below $D=1$. The output voltage will no longer continue to rise up when D exceeds this peak value, but starts falling down, and enters what we call a “voltage drop region” where the converter efficiency becomes very low. This peak thus imposes an upper limit for D which depends on R . Thus the upper limit for D_{\max} at the switching frequency of 20kHz and 500kHz can be found respectively:

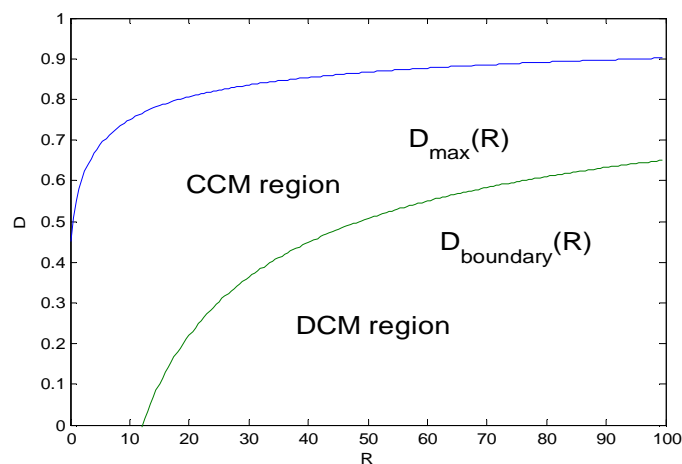
$$D_{\max}(R) = \frac{112 + 500R - 2\sqrt{133375R + 29876}}{500R - 955} \quad (2.16)$$

$$D_{\max}(R) = \frac{4 + 5R - \sqrt{30R + 24}}{5R - 2} \quad (2.17)$$

Fig. 2-9 shows the different regions of operation of SEPIC for a wide range of load resistance.



(a)



(b)

Fig. 2-9 Operating regions and modes depending on R and D (a)20kHz (b)500kHz

The figures show that for each load resistance, it exists a different range for the duty cycle in order to stay in CCM. The operating regions between CCM and DCM can be very useful for control designers for designing or implementing control laws in real cases.

2.4 SUMMARY

Three types of models for SEPIC have been presented in this chapter. The hybrid model is able to jointly describe both continuous and discrete behaviours exhibited by SEPIC. It helps for the simulation study and for designing such circuits. The control methods developed for SEPIC in this dissertation are tested using the hybrid model.

The averaged model is simple to build and takes into account the link between the sub-models of the hybrid system. Unfortunately, the corresponding model is not usually accurate enough at high frequencies where unmodeled dynamics are supposed to appear. To conclude, the averaged model only offers a good estimation of the hybrid system in a defined frequency range but it gives the opportunity to rely on standard tools proposed for nonlinear system. It will be used for the design of two nonlinear observers, topic of chapter 5.

The linear model is the result of linearization of averaged state space model around an operation point, thus it is mainly used to design linear control strategies which is relatively easy to design and widely used. For the nominal condition, the comparison of frequency responses between the linear model and the real circuit shows a high degree of correlation. But this nominal model cannot cover large domains of dynamic behaviour of the converter. Moreover, the analyses of the frequency response of the converter model show that SEPIC is a non minimum phase system where the location of unstable zeros varies with respect to the operating conditions. This unstable zeros' problem constitutes a challenge when designing a control law. At the end of this chapter, we have established analytic equations to define the boundary between CCM and DCM operations of the converter.

CHAPTER 3 PWM-BASED SLIDING MODE CONTROLLERS FOR SEPIC

As mentioned before, SEPIC is a non minimum phase, 4th order, nonlinear system. Nonlinear control strategies are more suitable to apply to SEPIC since they are based on nonlinear mathematical models of the system and by consequence they are able to cover large signal domains. However, the controller should insure a good performance for the feedback loop and should have the minimum complexity to be easily implemented.

The computation time of the controller should be limited as much as we can. On one hand, the SEPIC operates at high switching frequency which forces us to limit the computation time to be less than the switching period. On the other hand, the longer the computation time, the more the power consumption, what is critical in low power area.

Sliding Mode Control (SMC) is the good candidate to meet this objective. SMC is a nonlinear control tool used in many applications especially in nonlinear systems with variable structures. Variable Structure Systems (VSS) is a class of systems where the control law is deliberately changed during the control process according to some defined rules that depend on the state of the system. From this point of view, SEPIC represents a particular class of VSS since their structure is periodically changed by the action of controlled switch and diode. The main advantages of SMC are the guarantee of stability and robustness for large variations of system parameters and against perturbations. Moreover, given its flexibility in terms of synthesis, SMC is relatively easy to be implemented compared to other types of nonlinear control. That is why it is very interesting to study the application of this type of control to SEPIC.

In this chapter, after a recall of principle of SMC, a so-called PWM-Based SMC is applied to SEPIC. A detailed study of the choice of the sliding surface to control SEPIC is carried out in order to determine how and when to use what types of surface regarding performance specifications. Simulations and studies of the different sliding controls are carried out. Finally, the controller is implemented into dSPACE and the obtained results are discussed in order to classify the advantages and drawbacks of this type of control.

3.1 SLIDING MODE CONTROL PRINCIPLE

The sliding mode control is a class of control laws called “Variable Structure Control” based on the concept of changing the structure of controller depending on the state of the system in order to obtain the desired response. The principle of this method is based on using a discontinuous control to maintain the system evolution on a hyperplane, called “sliding surface”, $S(x)$, within a finite time. To maintain the trajectory on the sliding surface from any point of the state space, we must determine the sliding motion range for the SMC, i.e. to determine the existence conditions for sliding surface. This task can be performed using the principle of Lyapunov where the Lyapunov’s function V is defined as $V=(1/2)S^2(x)$ [SV89]. Once the trajectories reach the sliding surface, the stability conditions ensure that the system slides along the sliding surface towards the stable equilibrium in existence regions.

Designing a sliding mode controller consists of two major phases. First of all, we should design a sliding surface containing the equilibrium point. The choice of the sliding imposes the dynamic of the system before reaching the equilibrium point. Next, we have to design a switching control which seeks to make the sliding surface having the following properties:

1. Attractiveness: this property means that wherever the system is in the state space plane, the system will join the sliding surface.
2. Existence: by this property we insure that if the system crosses the sliding surface in the existence region, the system will stay at the surface.
3. Stability: Satisfying this property, we insure that the system will slide toward the desired equilibrium point.

We illustrate the general principle of SMC on a second order system modeled by:

$$\begin{cases} \dot{x}_1 = x_2 \\ \dot{x}_2 = f(x_1, x_2) + u \end{cases} \quad (3.1)$$

Where x_1, x_2 are the state variables, $f(x_1, x_2)$ is an unknown nonlinear function where $|f(x_1, x_2)|$ has a finite upper bound k that is known. We seek to design a controller which makes the system slide on the surface:

$$S(x) = S(x_1, x_2) = a_1 x_1 + x_2 = 0 \quad (3.2)$$

where a_1 is a control parameter and $a_1 > 0$.

In order to insure sliding properties, we refer to Lyapunov stability theory and take the following Lyapunov candidate function which depends on the surface:

$$V(x) = \frac{1}{2} S^2(x) \quad (3.3)$$

Taking the derivative of (3.3) we have $\dot{V}(x) = S(x)\dot{S}(x)$.

Based on the Lyapunov stability theory, $\dot{V}(x) < 0$ is a sufficient condition for the existence of a sliding mode. To achieve $S(x)\dot{S}(x) < 0$, the feedback control law u must be chosen so that

$$\begin{cases} u(x) \text{ makes } \dot{S}(x) > 0 & \text{if } S(x) < 0 \\ u(x) \text{ makes } \dot{S}(x) < 0 & \text{if } S(x) > 0 \end{cases} \quad (3.4)$$

Here $\dot{S}(x) = a_1\dot{x}_1 + \dot{x}_2 = a_1\dot{x}_1 + f(x_1, x_2) + u$. When $S(x) = a_1x_1 + x_2 < 0$, it makes $\dot{S}(x) > 0$, the control law should be chosen so that

$$u > |a_1x_2 + f(x_1, x_2)| \quad (3.5)$$

When $S(x) = a_1x_1 + x_2 > 0$, it makes $\dot{S}(x) < 0$, the control law should be picked so that

$$u < -|a_1x_2 + f(x_1, x_2)| \quad (3.6)$$

By the triangle inequality and the assumption about $|f(x_1, x_2)|$:

$$u = |a_1x_2| + k + 1 > |a_1x_2 + f(x_1, x_2)| \quad (3.7)$$

So the system can be feedback stabilized by

$$u(x) = \begin{cases} u^+(x) = |a_1x_2| + k + 1 & \text{for } S(x) < 0 \\ u^-(x) = -(|a_1x_2| + k + 1) & \text{for } S(x) > 0 \end{cases} \quad (3.8)$$

Which can be expressed in the closed form as:

$$u(x) = -(|a_1x_2| + k + 1) \text{sgn}(S(x)) \quad (3.9)$$

This control law is called sliding mode control.

In summary, the motion consists of a reaching phase during which the system trajectories move towards the surface and reach it in finite time, followed by a sliding phase during which the motion is confined to the surface $S(x)=0$ and the dynamics of the system are represented by:

$$\dot{x}_1 = x_2 = -a_1x_1 \quad (3.10)$$

with $a_1 > 0$, (3.10) has a globally exponentially stable equilibrium at $(x_1, x_2) = (0, 0)$. The speed of convergence depends on a_1 . It also reflects that during the sliding phase, the motion is independent of $f(x)$. This induces the robust nature of the sliding mode control.

Once $S(x)$ is achieved, the resulting closed-loop system moving along $S(x)=0$ is approximated by the smooth dynamics $\dot{S}(x)=0$. The equivalent control law of the sliding mode can be found by solving:

$$\dot{S}(x) = a_1 \dot{x}_1 + \dot{x}_2 = a_1 x_2 + f(x) + u = 0 \quad (3.11)$$

We obtain the equivalent control

$$u_{eq} = -(a_1 x_2 + f(x)) \quad (3.12)$$

That is, even though the actual control u is not continuous, the rapid switching across the sliding mode where $S(x)=0$ forces the system to act as if it was driven by this continuous equivalent control.

The described SMC is considered as ideal. It is assumed that the system must be operated at an infinite switching frequency so that the controlled variables can exactly follow the reference track to achieve the desired dynamic response and steady state operation [UGS99].

3.2 CONVENTIONAL HM-BASED SMC

A review of the literature [MRST93] shows that the previously proposed SMC for SEPIC converter is Hysteresis-Modulation (HM) based, which requires a bang-bang type controller to perform the switching control shown in Fig. 3-1.

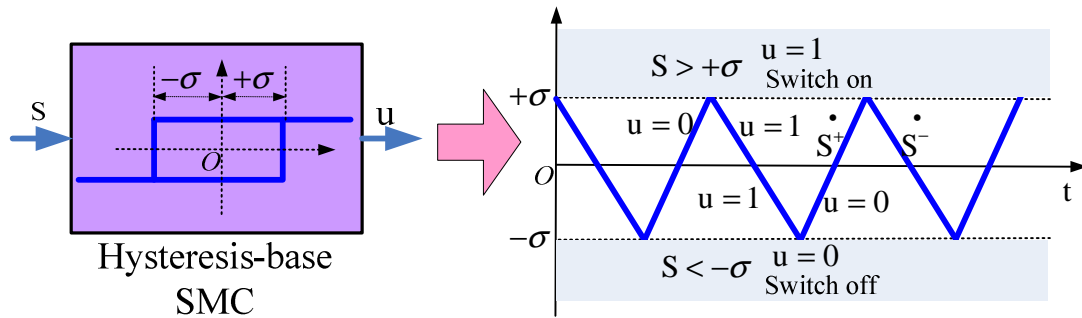


Fig. 3-1 Hysteresis Modulation-based SMC

Since there are only two available choices “ON” ($u=1$) and “OFF” ($u=0$) for switch action in SEPIC, then this method is easily accomplished as shown in equation (3.13):

$$u = \begin{cases} 1 = \text{'ON'} & \text{if } S(x) > \sigma \\ 0 = \text{'OFF'} & \text{if } S(x) < -\sigma \\ \text{previous state} & \text{otherwise} \end{cases} \quad (3.13)$$

where σ is an arbitrarily small value around zero.

The introduction of hysteresis band into the sliding surface limits the infinite high switching frequency. However, due to the lack of systematic design methods and implementation

criteria, the implementation of HM-based SMC for SEPIC still relies on the trial-and-error tuning of the σ magnitude to achieve the desired switching frequency for a particular operating condition. The performance of HM-based SMC depends on the experience of the designer.

3.3 THE NEED FOR FIXED-FREQUENCY SMC

It is known that the infinite high switching frequency is limited by the hysteresis band value σ . The SEPIC operating frequency thus depends on the bang-bang magnitude σ , i.e. HM-based SMC switching frequency is variable. It is well known that HM-based SM-controlled SEPIC generally suffers from significant switching-frequency variation when the input voltage or the output load is varied. This complicates the design of the input and output filters. Obviously, designing the filters under the worst case (lowest) frequency condition will result in oversized filters. Moreover, the variation of the switching frequency also deteriorates the regulation properties of the converter. Furthermore, it is known that switching converters are severe noise generators. The task of eliminating noise can be easier with fixed frequency operation. It is therefore necessary to have the SM-controlled SEPIC operating at a constant switching frequency for all operating conditions.

In order to keep the switching frequency fixed, two basic approaches have been proposed in the implementation of conventional HM-based SMC. The first approach is to incorporate a constant ramp or timing function directly into the controller [MRST93, CMMC92, IV04]. The main advantage of this approach is that the switching frequency is constant under all operating conditions and can be easily controlled through varying the ramp/timing signal. However, this method demands additional hardware circuitries and deteriorate the transient response of the system caused by the superposition of the ramp function upon the SM switching function. The second approach is to include some forms of adaptive control into the HM-based SM-controller to contain the switching-frequency variation [NL95]. For line variation, the frequency variation is alleviated through an adaptive feed-forward control, which varies the hysteresis band with the change of the line input voltage. For load variation, the frequency variation is alleviated through an adaptive feedback control, which varies the control parameter (i.e., sliding coefficient) with the change of the output load. Conceptually, these methods of adaptive control are more direct and less likely to suffer from deteriorated transient response. However, the architecture of the resulting controller is relatively more complex and may increase the implementation cost of the controller.

In [NL96], a constant switching-frequency SM-controller is proposed for a buck converter by employing a so called PWM-based SMC. The advantages are the similarity with classical PWM control schemes and the lack of additional hardware circuitries since the switching function is performed by the PWM modulator.

3.4 PRINCIPLE OF PWM-BASED SLIDING MODE CONTROLLER

The principle of PWM-based SM-controller is based on two key results. First, as mentioned in 3.1, the rapid switching across the sliding mode where $S(x)=0$ forces the system to act as if it was driven by the continuous equivalent control, which can be formulated using the invariance conditions by setting the time derivative as $\dot{S}(x) = 0$ [UGS99]. In other words, the discrete control input (gate signal) u can be theoretically replaced by the equivalent control u_{eq} at an infinite high switching frequency. Second, with a very high switching frequency, the equivalent control can be considered as the averaged value of the switching control, or as the duty cycle introduced by the averaged model [Sir89].

In practice, for a power converter modelled by a nonlinear system $\dot{x} = f(x, u)$, the design of a PWM-based SM control is usually done as follows. Define or select a sliding surface $S(x)$ which takes into account the objectives expected of the state vectors. There are infinite possibilities for choosing $S(x)$. It is generally taken as a linear combination of the state variables [HMPF96, CVLLM00]:

$$S = G^T x \quad (3.14)$$

Where $G^T = [G_1, \dots, G_n]^T$ is the sliding gain vector. In an ideal SM operation, the state trajectory S is always moving along the sliding plane, i.e., $S=0$, and without any high-frequency oscillation, it is also true that $\dot{S}(x) = 0$.

Next, consider that the equivalent control produces a trajectory whereby its motion is exactly equivalent to the trajectory motion of an ideal SM operation. Under such assumptions, the state trajectory equation $\dot{S} = G^T \cdot f(x, u)$, can be rewritten as

$$\dot{S} = G^T \cdot f(x, u_{eq}) \quad (3.15)$$

Then, the solution of the equivalent control u_{eq} can be obtained by solving $G^T \cdot f(x, u_{eq}) = 0$.

Finally, if u_{eq} is substituted back into the original system

$$\dot{x} = f(x, u_{eq}) \quad (3.16)$$

which is the motion equation of the converter under SM operation. This method of deriving the equivalent control signal u_{eq} , as well as the insertion of the signal into the original system to formulate the motion equation as shown in (3.16), is known as the equivalent control method [UGS99]. As the equivalent control signal u_{eq} is equivalent to the duty ratio, u_{eq} is compared to a ramp waveform to generate a discrete gate pulse signal [Mit98].

Finally, what remains is to attract the trajectory towards the surface and stay at the surface which is the characteristic of the sliding mode control. This depends on the existence conditions. To ensure these conditions, we should determine the control vector parameters G which satisfy

$$\begin{cases} u = 1, \dot{S}(x) = G^T \cdot f(x, u) < 0 & \text{if } S(x) > 0 \\ u = 0, \dot{S}(x) = G^T \cdot f(x, u) > 0 & \text{if } S(x) < 0 \end{cases} \quad (3.17)$$

The choice of these parameters defines the regions of existence which must contain the equilibrium point for the sliding mode.

Besides the existence conditions, the sliding mode controller should also comply with the stability conditions to ensure that the sliding surface will direct the state trajectory towards the stable equilibrium point in existence regions.

As we have discussed, to achieve an ideal SMC operation, the system must be operated at an infinite switching frequency so that the state variables' trajectory is oriented precisely on the sliding surface. However, in the practical case of finite switching frequency, the trajectory will oscillate in some vicinity of the sliding surface while moving towards the origin.

3.5 PWM-BASED SM-CONTROLLER DESIGN FOR SEPIC

3.5.1 Integral Sliding Mode Controller Design

The averaged model of the SEPIC under CCM operation can be modelled as: $\dot{x} = f(x, \rho) + gv_e$. The model is given as (2.8).

A. Sliding surface

As the control objective is to keep the output voltage, v_s , tracking the reference voltage, V_{ref} , we can take the most common PID-based surface [CL97] defined as:

$$S = \gamma_1 (V_{ref} - v_s) + \gamma_2 \frac{d}{dt} (V_{ref} - v_s) + \gamma_3 \int (V_{ref} - v_s) dt \quad (3.18)$$

Where $\gamma_1, \gamma_2, \gamma_3$ are control parameters which are to satisfy the existence conditions. This surface cannot be used since if we derive the output voltage v_s , we obtain directly the control ρ in the expression of the sliding surface.

On the other side, since the equivalent control can be obtained directly based on derivative of output voltage, the relative degree of (3.18) is equal to 1, the PID-based sliding surface, containing only one state variable v_s , would give an unstable control law and was inappropriate in the case of the SEPIC converter [JOGLL10].

We propose then to increase the number of state variables as low as possible in the sliding surface. To avoid a large number of tuning gains, we choose a surface containing the input current in addition of the output voltage. The reason for choosing i_{L1} instead of i_{L2} is to allow the sliding surface to directly control the input of the circuit in addition to its output, which is more stable than the other case [JOGLL10].

At an infinitely high switching frequency, the SM controller will ensure that both the output voltage and inductor current are regulated to follow exactly their instantaneous references V_{ref} and i_{ref} respectively, i.e., $V_{ref} = v_s$ and $i_{ref} = i_{L1}$. However, in the case of finite frequency or fixed-frequency SM-controllers, the control is imperfect. Steady-state errors exist in both the output voltage and the inductor current such that $V_{ref} \neq v_s$ and $i_{ref} \neq i_{L1}$.

A good method of suppressing these errors is to introduce an additional integral term of the state variables into the sliding surface. Therefore, an integral term of these errors has been introduced into the SM current controller as an additional controlled state-variable to reduce these steady-state errors. This is commonly known as integral sliding mode control (ISMC).

The sliding surface is proposed as specified by

$$S = \alpha_1 e_1 + \alpha_2 e_2 + \alpha_3 e_3 \quad (3.19)$$

Where α_1, α_2 , and α_3 represent the desired control parameters denoted sliding coefficients, e_1, e_2 and e_3 are expressed as

$$\begin{cases} e_1 = i_{ref} - i_{L1} \\ e_2 = V_{ref} - v_s \\ e_3 = \int [e_1 + e_2] dt \end{cases} \quad (3.20)$$

where V_{ref} and i_{ref} denote the instantaneous reference of output voltage and input current respectively.

B. Equivalent control

Extracting the time derivative of (3.15) leads to

$$\begin{cases} \dot{e}_1 = \frac{d[i_{\text{ref}} - i_{L1}]}{dt} \\ \dot{e}_2 = \frac{d[V_{\text{ref}} - v_s]}{dt} \\ \dot{e}_3 = e_1 + e_2 \end{cases} \quad (3.21)$$

The reference current i_{ref} can be taken as $K(V_{\text{ref}} - v_s)$ where K is the amplified gain of the voltage error, It should be mentioned that the use of integral control here is optional. As in conventional current mode control, a sufficiently large value of K in the outer voltage loop is sufficient to ensure an excellent regulation of the output voltage with a negligible steady-state error, then

$$\dot{e}_1 = \frac{d[i_{\text{ref}} - i_{L1}]}{dt} = \frac{d[K(V_{\text{ref}} - v_s) - i_{L1}]}{dt} \quad (3.22)$$

Considering

$$\dot{v}_s = \frac{dv_s}{dt} = \frac{i_{C2}}{C_2} \quad (3.23)$$

To simplify the calculation, assuming that V_{ref} is constant, substituting equation (3.22) into (3.16), the equivalent control input signal u_{eq} is established as the duty cycle.

$$\dot{e}_1 = -\frac{K}{C_2} i_{C2} - \left[\frac{(u_{\text{eq}} - 1)(v_{C1} + v_s)}{L_1} - \frac{r_{L1}}{L_1} i_{L1} + \frac{v_e}{L_1} \right] \quad (3.24)$$

$$\dot{e}_2 = \frac{d[V_{\text{ref}} - v_s]}{dt} = -\frac{K}{C_2} i_{C2} \quad (3.25)$$

$$\dot{e}_3 = e_1 + e_2 = (K+1)(V_{\text{ref}} - v_s) - i_{L1} \quad (3.26)$$

The equivalent control signal u_{eq} can be formulated using the invariance conditions by setting the time derivative of (3.19) as $\dot{S} = 0$, i.e.,

$$\dot{S} = \alpha_1 \dot{e}_1 + \alpha_2 \dot{e}_2 + \alpha_3 \dot{e}_3 = 0 \quad (3.27)$$

Now solving for equivalent control function yields

$$u_{eq} = \frac{1}{(v_{C1} + v_s)} [K_1(V_{ref} - v_s) - K_2 i_{C2} - K_3 i_{L1} + r_{L1} i_{L1} + (v_{C1} + v_s - v_e)] \quad (3.28)$$

where $K_1 = \frac{\alpha_3}{\alpha_1} L_1 (K + 1)$, $K_2 = \frac{L_1}{C_2} (K + \frac{\alpha_2}{\alpha_1})$ and $K_3 = \frac{\alpha_3}{\alpha_1} L_1$ are the fixed gain parameters in the proposed controller.

C. Attraction and existence conditions

The attraction condition consists to find the regions of attraction given by $S(x)\dot{S}(x) < 0$ throughout the entire domain of operation and which are imposed by the SMC strategy. These regions are found using the following inequalities:

$$\begin{cases} u = 1, \dot{S}(x) < 0 & \text{if } S(x) > 0 \\ u = 0, \dot{S}(x) > 0 & \text{if } S(x) < 0 \end{cases} \quad (3.29)$$

Detailing equation (3.29) leads to

Case 1: $S > 0$, $u = 1$, then $\dot{S} < 0$:

$$v_e - K_1(V_{ref} - v_s) + K_2 i_{C2} - (K_3 - r_{L1}) i_{L1} > 0 \quad (3.30)$$

Case 2: $S < 0$, $u = 0$, then $\dot{S} > 0$:

$$v_e - K_1(V_{ref} - v_s) + K_2 i_{C2} - (K_3 - r_{L1}) i_{L1} < v_s + v_{C1} \quad (3.31)$$

The time varying variables i_{L1} , i_{C2} , v_e , v_s and v_{C1} can be respectively substituted with their expected maximum/minimum or steady-state parameters, which can be derived from the design specification. This gives

$$\begin{cases} V_{e(\min)} - K_1(V_{ref} - v_{ss}) + K_2 i_{C2(\min)} - K_3 i_{L1(\max)} + r_{L1} i_{L1(\min)} > 0 \\ V_{e(\max)} - K_1(V_{ref} - v_{ss}) + K_2 i_{C2(\max)} - K_3 i_{L1(\min)} + r_{L1} i_{L1(\max)} < v_{ss} + v_{C1(\min)} \end{cases} \quad (3.32)$$

where $V_{e(\max)}$ and $V_{e(\min)}$ denote the maximum and minimum input voltages respectively; v_{ss} denotes the expected steady state output voltage which is a small error from the desired reference voltage V_{ref} ; and $i_{L1(\max)}$, $i_{L1(\min)}$, $i_{C2(\max)}$ and $i_{C2(\min)}$ are respectively the maximum and minimum inductor and capacitor currents when the converter is operating in full-load condition. $v_{C1(\min)}$ denotes the minimum voltage of capacitor C_1 .

As the attractiveness condition is insured in the entire domain of operation, it is naturally validated near the sliding surface. That is what we call ‘‘existence condition’’.

D. Stability conditions

Since attractiveness and existence conditions are expressed by inequalities(3.32), there are some degrees of freedom in choosing coefficients K_i . The solutions giving stable and non-oscillatory response of all state variables can therefore be investigated. This is obtained by replacing the equivalent control (3.28) into the original SEPIC model:

$$\left\{ \begin{array}{l} \frac{di_{L1}}{dt} = \frac{V_e}{L_1} - \frac{r_{L1}}{L_1} i_{L1} + \frac{(v_s + v_{Cl})}{L_1} \left[\frac{[K_1(V_{ref} - v_s) + K_2 \frac{v_s}{R} - K_3 i_{L1} + r_{L1} i_{L1} - v_e]}{(v_s + v_{Cl}) - K_2(i_{L1} - i_{L2})} \right] \\ \frac{di_{L2}}{dt} = \frac{v_s}{L_2} - \frac{r_{L2}}{L_2} i_{L2} - \frac{(v_s + v_{Cl})}{L_2} \frac{[K_1(V_{ref} - v_s) + K_2 \frac{v_s}{R} + v_s + v_{Cl} - K_2(i_{L1} - i_{L2}) - K_3 i_{L1} + r_{L1} i_{L1} - v_e]}{(v_s + v_{Cl}) - K_2(i_{L1} - i_{L2})} \\ \frac{dv_{Cl}}{dt} = \frac{i_{L1}}{C_1} + \frac{(i_{L2} - i_{L1})}{C_1} \frac{[K_1(V_{ref} - v_s) + K_2 \frac{v_s}{R} + v_s + v_{Cl} - K_2(i_{L1} - i_{L2}) - K_3 i_{L1} + r_{L1} i_{L1} - v_e]}{(v_s + v_{Cl}) - K_2(i_{L1} - i_{L2})} \\ \frac{dv_s}{dt} = -\frac{v_s}{RC_2} + \frac{i_{L2} - i_{L1}}{C_2} \left[\frac{[K_1(V_{ref} - v_s) + K_2 \frac{v_s}{R} - K_3 i_{L1} + r_{L1} i_{L1} - v_e]}{(v_s + v_{Cl}) - K_2(i_{L1} - i_{L2})} \right] \end{array} \right. \quad (3.33)$$

These equations are nonlinear. Linearization of (3.33) around the operating point gives:

$$\left\{ \begin{array}{l} \frac{d\tilde{i}_{L1}}{dt} = a_{11}\tilde{i}_{L1} + a_{12}\tilde{i}_{L2} + a_{13}\tilde{v}_{Cl} + a_{14}\tilde{v}_s \\ \frac{d\tilde{i}_{L2}}{dt} = a_{21}\tilde{i}_{L1} + a_{22}\tilde{i}_{L2} + a_{23}\tilde{v}_{Cl} + a_{24}\tilde{v}_s \\ \frac{d\tilde{v}_{Cl}}{dt} = a_{31}\tilde{i}_{L1} + a_{32}\tilde{i}_{L2} + a_{33}\tilde{v}_{Cl} + a_{34}\tilde{v}_s \\ \frac{d\tilde{v}_s}{dt} = a_{41}\tilde{i}_{L1} + a_{42}\tilde{i}_{L2} + a_{43}\tilde{v}_{Cl} + a_{44}\tilde{v}_s \end{array} \right. \quad (3.34)$$

The system eigenvalues are then calculated from (3.34) as a function of coefficients K_i in order to find the solutions having eigenvalues with negative real part and suitable dynamic behavior.

E. Simulation of ISMC for SEPIC

According to the existence and stability conditions, arrangement for the variations of parameters K_1, K_2, K_3 is obtained, and the simulation is later performed to study the effects of the various control gains on the response of the output voltage.

Fig. 3-2 shows the schematic of the proposed PWM-based ISMC.

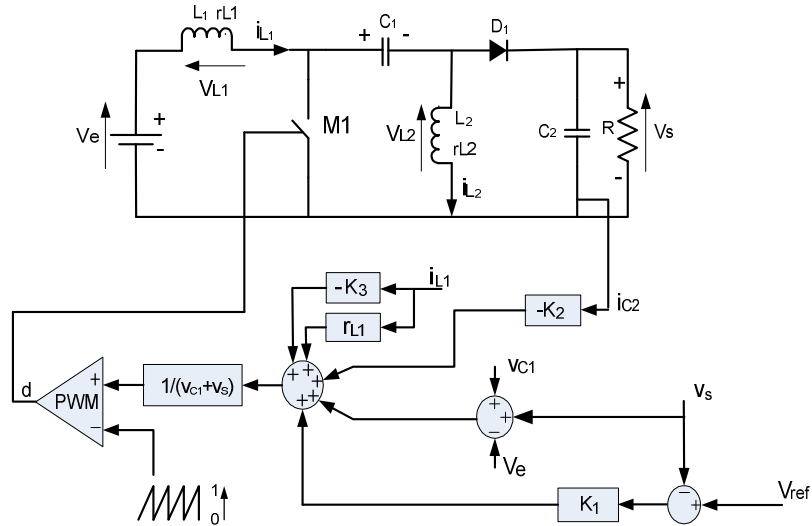


Fig. 3-2 Proposed PWM controller for SEPIC

Verification of the derived control law of SEPIC is performed using MATLAB and Simulink. Simulations have been done with SEPIC hybrid model. Parasitic resistances of inductors are considered. Control signal is obtained from the control law (3.28) with 20kHz triangular wave. The circuit parameters are as follows: input voltage $V_e=20V$, output voltage $V_s=20V$, $f_{sw}=20kHz$, inductors $L_1=2.3mH$, $L_2=330\mu H$, parasitic resistance of inductors $r_{L1}=2.134\Omega$, $r_{L2}=0.224\Omega$, $C_1=C_2=190\mu F$.

Simulation for a load step variation from 44Ω to 22Ω shows that:

- a) an increment in K_1 improves the steady-state regulation with a lower overshoot but causes the transient response to be more oscillatory, thus prolonging the steady-state settling time (see Fig. 3-3);

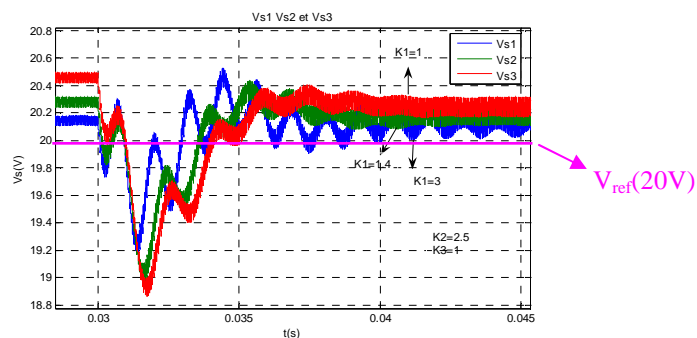


Fig. 3-3 Output voltage (v_s) for different K_1 settings

- b) an increment in K_2 improves the steady-state regulation and reduces the steady-state error, but makes the transient response oscillatory with a higher overshoot. (see Fig. 3-4).

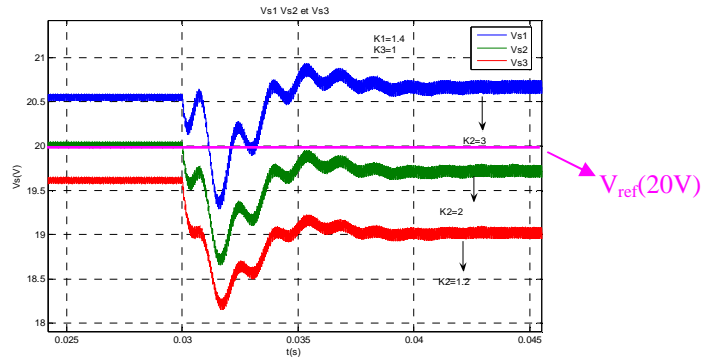


Fig. 3-4 Output voltage (v_s) for different K_2 settings

- c) increasing K_3 can have a moderate reduction in the oscillation of the transient response and also a significant reduction in the steady-state settling time, but increases the steady state error. (see Fig. 3-5).

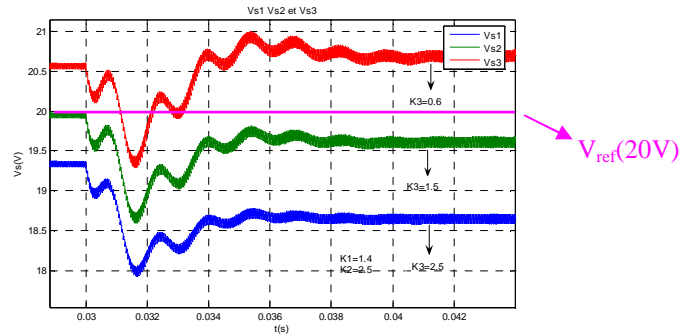


Fig. 3-5 Output voltage (v_s) for different K_3 settings

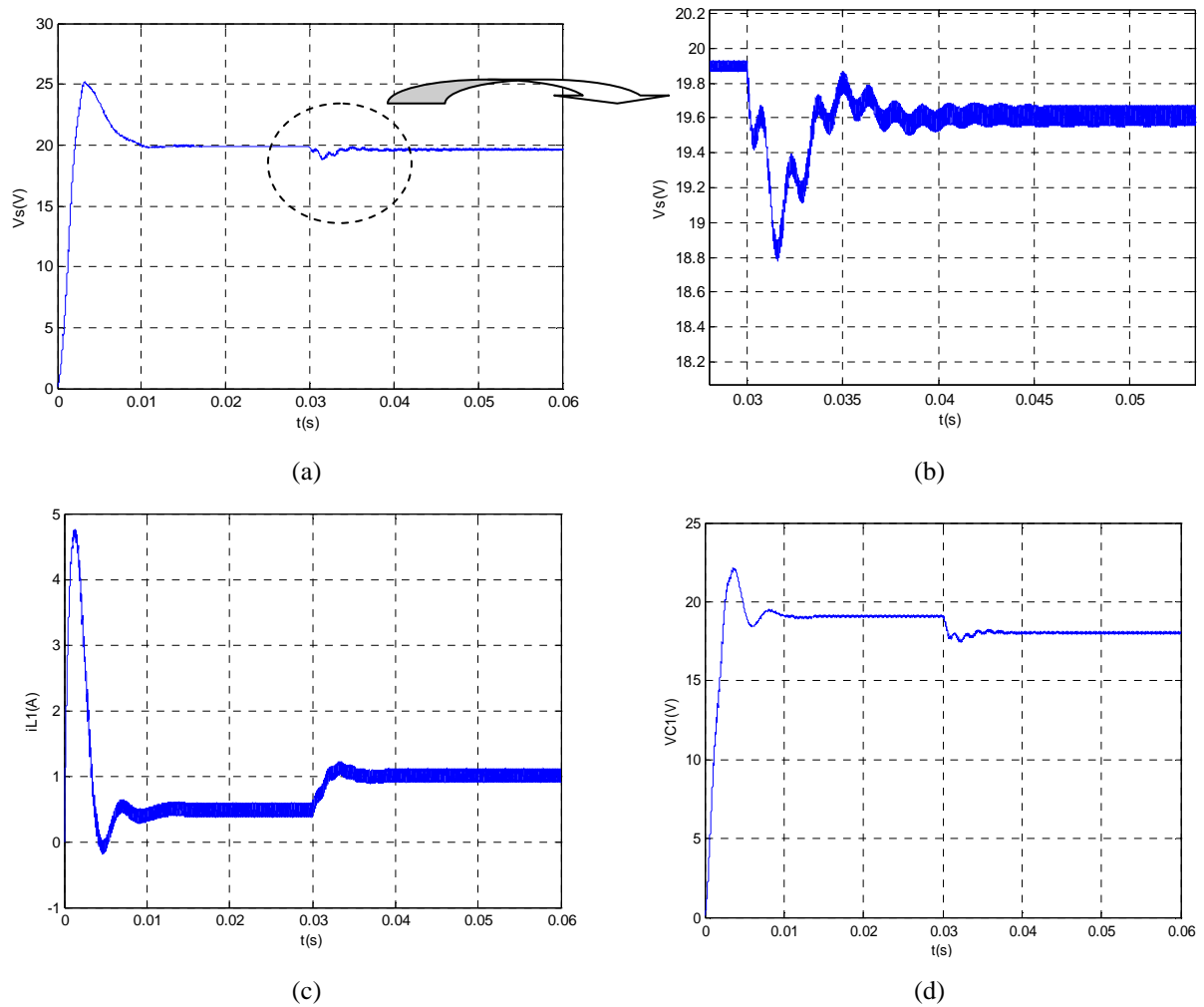
From the above simulation results, the performance comparison of different parameter values can be given in Table 3-1.

Table 3-1: Performance comparison of K_1 , K_2 and K_3

		Overshoot voltage(V)	Settling time (ms)	Steady state error(V)
$K_2=2.5$ $K_3=1$	$K_1=1$	1.4	120	-0.3
	$K_1=1.4$	1.2	140	-0.2
	$K_1=3$	0.8	200	-0.2
$K_1=1.4$ $K_3=1$	$K_2=1.2$	0.8	100	-0.6
	$K_2=2$	0.8	100	-0.2
	$K_2=3$	0.8	100	0.2
$K_1=1.4$ $K_2=2.5$	$K_3=0.6$	1.9	120	0.2
	$K_3=1.5$	0.9	100	-0.4
	$K_3=2.5$	0.7	80	-0.7

Hence, in accordance to the observation, a better group of the value of parameters is chosen: $K_1 = 2$, $K_2 = 2.5$, $K_3 = 1$.

With these parameters, Fig 3.6 shows the results obtained by varying the load between 44Ω and 22Ω . In spite of the large variation of the charge, the system controlled by the proposed method is still stable.



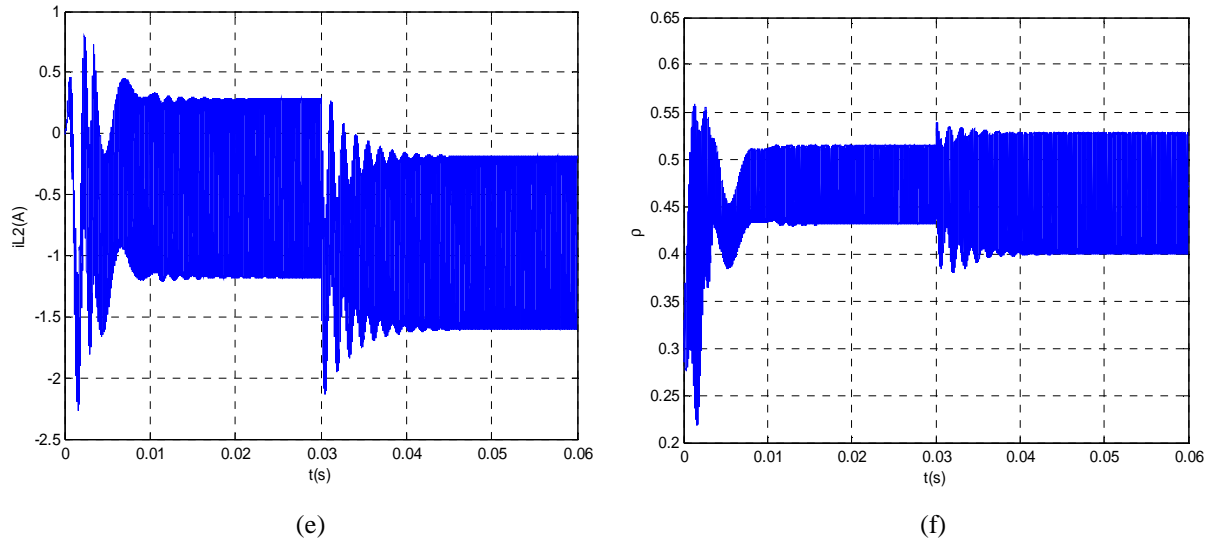


Fig. 3-6 Dynamic response of SMC when load changes from 0.45A to 0.9A (R: 44Ω to 22 Ω): (a) output voltage v_s , (b) (Zoom in) at the step change at $t=0.03$ s, (c) input inductance current i_{L1} , (d) voltage of capacitance v_{C1} , (e) output inductance Current i_{L2} , (f) PWM duty ratio d

It can be noted that the ISMC scheme contains a significant level of steady-state error of output voltage around 300mV (see Fig. 3-6(b)).

As mentioned previously, the PWM-based SMC is based on the equivalent control method, which assumes the invariance conditions that during SM operation, $S = 0$ and $\dot{S} = 0$. From such an assumption, an equivalent control signal u_{eq} is derived by setting the time derivative as $\dot{S}(x) = 0$. However, the time derivative of the component $e_3 = \int [e_1 + e_2] dt$ of $S(x)$ gives $e_1 + e_2$ in the control signal u_{eq} . The effectiveness of the integral control in alleviating the steady-state error deteriorates. Hence, with the ISMC scheme, finite steady-state errors cannot be eliminated.

3.5.2 Double Integral Sliding Mode Controller Design

An additional double-integral term of the state variables, i.e., $e_4 = \iint (e_2 dt) dt$ is introduced in the sliding surface (3.19). This is the so-called double-integral sliding mode (DISM) controller proposed in this work.

Thus, the proposed DISM controller (DISMC) has the following sliding surface:

$$S = \alpha_1 e_1 + \alpha_2 e_2 + \alpha_3 e_3 + \alpha_4 e_4 \quad (3.35)$$

Where $\alpha_1, \alpha_2, \alpha_3, \alpha_4$ represent the desired sliding coefficients and e_1, e_2 , the integral of the current and the voltage errors, e_3 and e_4 are expressed as:

$$\begin{cases} e_1 = i_{\text{ref}} - i_{L1} \\ e_2 = V_{\text{ref}} - v_s \\ e_3 = \int (e_1 + e_2) dt \\ e_4 = \int \left(\int (e_1 + e_2) dt \right) dt \end{cases} \quad (3.36)$$

Substituting the SEPIC behavioural models under CCM into the time derivative of (3.36) gives the dynamical model of the proposed system as

$$\begin{cases} \dot{e}_1 = \frac{d[i_{\text{ref}} - i_{L1}]}{dt} = -\frac{K}{C_2} i_{C2} - \left[\frac{(u-1)(v_{C1} + v_s)}{L_1} - \frac{r_{L1}}{L_1} i_{L1} + \frac{v_e}{L_1} \right] \\ \dot{e}_2 = \frac{d[V_{\text{ref}} - v_s]}{dt} = -\frac{K}{C_2} i_{C2} \\ \dot{e}_3 = e_1 + e_2 \\ \dot{e}_4 = \int \left(\int (e_1 + e_2) dt \right) dt \end{cases} \quad (3.37)$$

The equivalent control deduced from $\dot{S}(x) = 0$ gives:

$$\begin{aligned} u_{\text{eq}} = 1 - \frac{v_e}{v_{C1} + v_s} + \frac{r_{L1}}{L_1} \frac{i_{L1}}{(v_{C1} + v_s)} - \frac{L_1}{C_2(v_{C1} + v_s)} \left(K + \frac{\alpha_2}{\alpha_1} \right) i_{C2} + \frac{\alpha_3}{\alpha_1} \frac{L_1}{(v_{C1} + v_s)} (K+1)(V_{\text{ref}} - \\ - \frac{\alpha_3}{\alpha_1} \frac{L_1}{(v_{C1} + v_s)} i_{L1} + \frac{\alpha_4}{\alpha_1} \frac{L_1}{(v_{C1} + v_s)} \int (V_{\text{ref}} - v_s) dt \end{aligned} \quad (3.38)$$

The proposed DISMC for the SEPIC inherits the expression:

$$u_{\text{eq}} = \frac{1}{v_{C1} + v_s} \left[K_1(V_{\text{ref}} - v_s) + K_4 \int (V_{\text{ref}} - v_s) dt - K_3 i_{L1} - K_2 i_{C2} + r_{L1} i_{L1} + (v_{C1} + v_s - v_e) \right] \quad (3.39)$$

where $K_1 = \frac{\alpha_3}{\alpha_1} L_1 (K+1)$; $K_2 = \frac{L_1}{C_2} \left(K + \frac{\alpha_2}{\alpha_1} \right)$; $K_3 = \frac{\alpha_3}{\alpha_1} L_1$ and $K_4 = \frac{\alpha_4}{\alpha_1} L_1$ are the fixed gain parameters in the proposed controller.

Equation (3.39) shows that the DISMC introduces a component $\int (V_{\text{ref}} - v_s) dt$ in the equivalent control. This allows us to solve the problem of steady-state errors in ISMC algorithm.

As stated previously for the ISMC, to ensure the existence conditions for sliding surface, the existence condition for DISMC is performed by satisfying:

$$\begin{cases} V_e - K_1[V_{\text{ref}} - v_s] - K_4 \int [V_{\text{ref}} - v_s] dt + K_2 i_{C2} - (K_3 - r_{L1}) i_{L1} > 0 \\ V_e - K_1[V_{\text{ref}} - v_s] - K_4 \int [V_{\text{ref}} - v_s] dt + K_2 i_{C2} - (K_3 - r_{L1}) i_{L1} < v_s + v_{C1} \end{cases} \quad (3.40)$$

To determine the parameters K_1, K_2, K_3, K_4 , the same method as with ISMC is used.

$$\left\{ \begin{array}{l}
\frac{di_{L1}}{dt} = \frac{V_e}{L_1} - \frac{r_{L1}}{L_1} i_{L1} + \frac{(v_s + v_{Cl})}{L_1} \frac{[K_1(V_{ref} - v_s) + K_4 \int (V_{ref} - v_s) dt + K_2 \frac{v_s}{R} - K_3 i_{L1} + r_{L1} i_{L1} - v_e]}{(v_s + v_{Cl}) - K_2(i_{L1} - i_{L2})} \\
\frac{di_{L2}}{dt} = \frac{v_s}{L_2} - \frac{r_{L2}}{L_2} i_{L2} + \frac{(v_s + v_{Cl})}{L_2} \left[\frac{K_1(V_{ref} - v_s) + K_4 \int (V_{ref} - v_s) dt + K_2 \frac{v_s}{R} - K_3 i_{L1} + r_{L1} i_{L1} - v_e}{(v_s + v_{Cl}) - K_2(i_{L1} - i_{L2})} + 1 \right] \\
\frac{dv_{Cl}}{dt} = \frac{i_{L1}}{C_1} + \frac{(i_{L2} - i_{L1})}{C_1} \left[\frac{K_1(V_{ref} - v_s) + K_4 \int (V_{ref} - v_s) dt + K_2 \frac{v_s}{R} - K_3 i_{L1} + r_{L1} i_{L1} - v_e}{(v_s + v_{Cl}) - K_2(i_{L1} - i_{L2})} + 1 \right] \\
\frac{dv_s}{dt} = -\frac{v_s}{RC_2} + \frac{i_{L2} - i_{L1}}{C_2} \left[\frac{K_1(V_{ref} - v_s) + K_4 \int (V_{ref} - v_s) dt + K_2 \frac{v_s}{R} - K_3 i_{L1} + r_{L1} i_{L1} - v_e}{(v_s + v_{Cl}) - K_2(i_{L1} - i_{L2})} \right]
\end{array} \right. \quad (3.41)$$

Taking linearization of (3.41) around the operating point, the system eigenvalues are then calculated as a function of coefficients K_i . To get eigenvalues with negative real part and suitable dynamic behaviour, the chosen values of parameters that makes best trade-off between dynamic performance and stability are: $K_1 = 1.2$, $K_2 = 2.5$, $K_3 = 1$, $K_4 = 200$.

Fig. 3-7 shows the comparative simulation results of output voltage waveforms between ISMC and the proposed DISMC for a step response and a step load changes alternating between 44Ω and 22Ω .

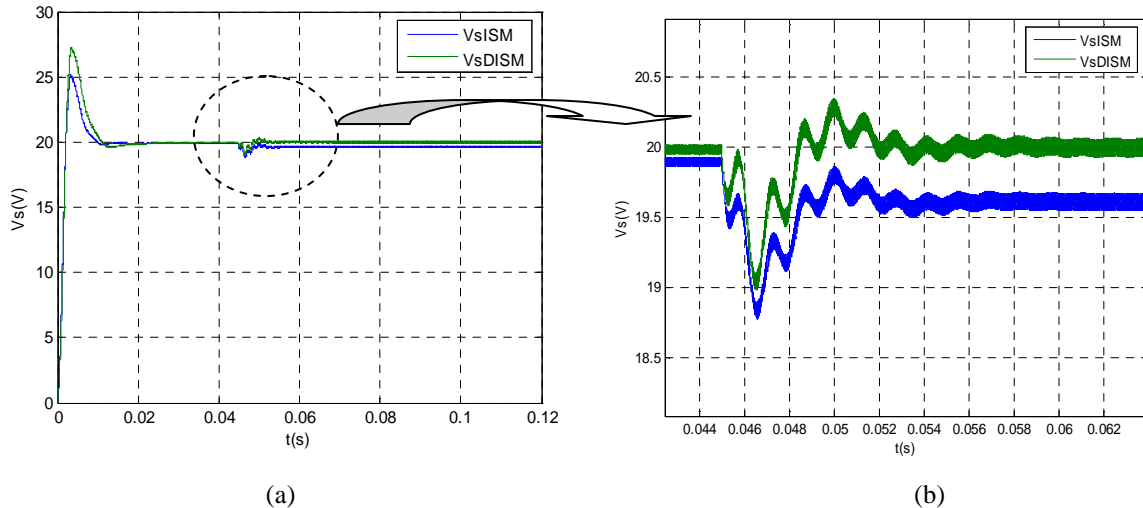


Fig. 3-7 Simulation responses to a load change (ISMC and DISMC):
(a) transient reference (b) step change at $t=0.045$ s

As we can see from the figures, both controllers have excellent large-signal property either for transient reference and load changes. The steady-state error of ISMC is eliminated with

the DISMC as expected. The ISMC and DISMC are chosen to get a trade off between stability and convergence time.

3.5.3 Simplified Double Integral Sliding Mode Controller

For FPGA implementation, simplification of the control algorithm can reduce logic resource consumption. As the steady-state errors in the ISMC are mainly reflected in the output voltage, so we propose to ignore the double integral of i_{L1} in the sliding surface. This last becomes relatively straightforward:

$$S = \alpha_1 e_1 + \alpha_2 e_2 + \alpha_3 e_3 + \alpha_4 e_4 \quad (3.42)$$

With

$$\begin{cases} e_1 = i_{\text{ref}} - i_{L1} \\ e_2 = V_{\text{ref}} - v_s \\ e_3 = \int e_2 dt \\ e_4 = \iint (e_2 dt) dt \end{cases} \quad (3.43)$$

The corresponding equivalent control is expressed as:

$$u_{\text{eq}} = \frac{1}{V_{C1} + v_s} [K_1 (V_{\text{ref}} - v_s) + K_4 \int (V_{\text{ref}} - v_s) dt - K_2 i_{C2} + r_{L1} i_{L1} + (v_{C1} + v_s - v_e)] \quad (3.44)$$

From (3.44), it can be seen that only three parameters have to be adjusted.

Simulation comparisons between DISMC (DISM1) and simplified DISMC (DISM2) are represented in Fig. 3-8 that shows the state variables response with respect to an output reference voltage change from 20V to 22V, and the load is fixed at 22 Ω .

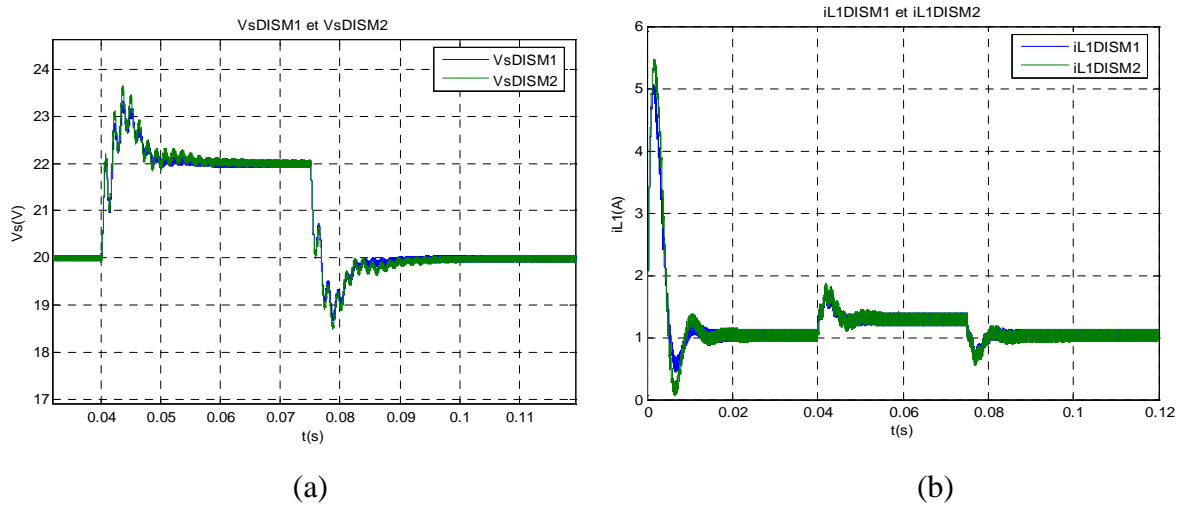


Fig. 3-8 Simulation responses to output reference voltage change (DISM1 and DISM2): (a) output voltage v_s , (b) input inductance current i_{L1}

We can see that in transient operation condition when the reference voltage suddenly varies from 20V to 22V, and returns to 20V. Both DISMC and simplified DISMC can quickly reach the output reference voltage since the transient response time is short and the overshoot is acceptable. For a step load variation between 44Ω and 22Ω, the comparison is shown in Fig. 3-9.

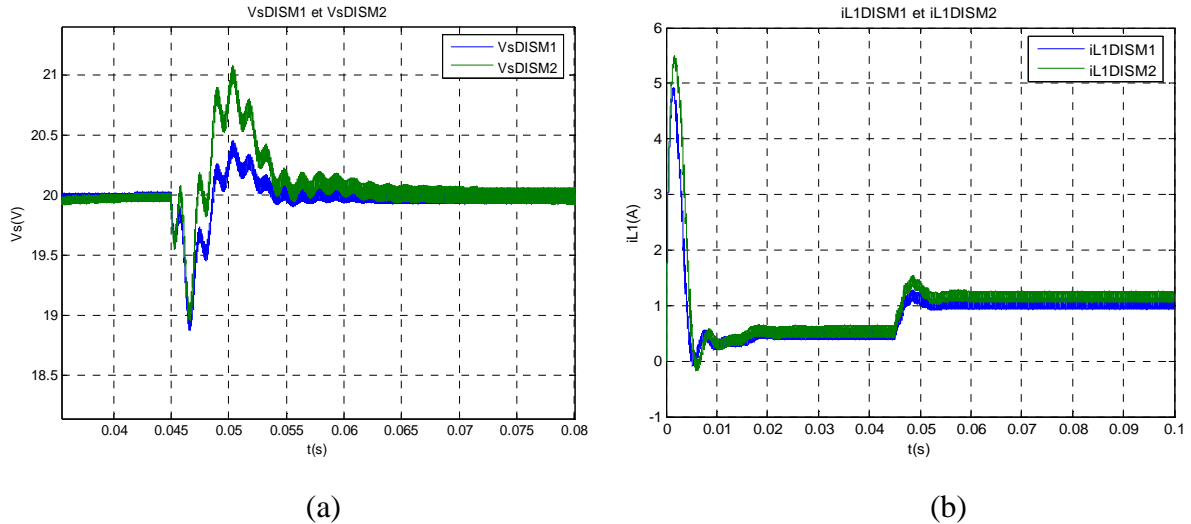


Fig. 3-9 Simulation responses to load change (DISM1 and DISM2):(a) output voltage v_s , (b) input inductance current i_{L1}

Fig. 3-9 shows that the DISMC has better dynamic behaviour compared to simplified DISMC in this case. From the reference voltage change and the step load variation, it can be seen that both DISMCs can eliminate the steady-state errors and display certain robustness. For the simplified DISMC, absence of current double integral in the sliding surface induces more overshoot. However, the dynamics remains acceptable and the parameter tuning and the control algorithm are simplified.

3.6 EXPERIMENTAL VALIDATION OF CONTROLLERS

To experimentally test the SEPIC behaviour and control algorithms, the proposed control algorithms require to measure some state variables, thus sensors are adopted to acquire all the current variables. In our work, we use the current sensor LTS 25-NP. A system working at low-frequency of 20kHz is built and set up, and the control algorithms are implemented in dSPACE platform. The diagram of the system is shown in Fig. 3-10.

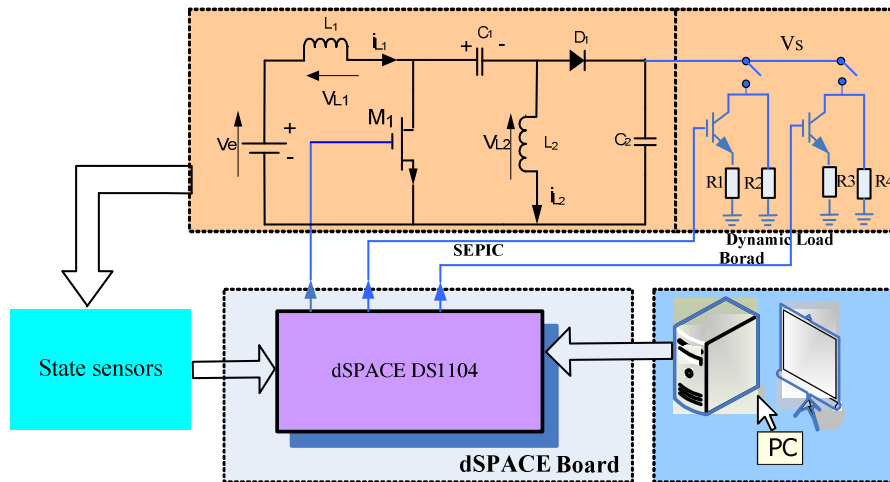


Fig. 3-10 Block diagram of the experimental test platform

3.6.1 DSP Test Bench Description

The proposed controllers are implemented using dSPACE DS1104. The test platform mainly consists of two parts. The detailed functionalities will be discussed in the following section.

A. DSPACE platform

The DS1104 includes a master processor PowerPV 603/250MHz and a slave processor Texas Instruments TMS320F240. It includes different hardware characteristics like timers, counters, PWM generators, etc.[JAG09]. When the control algorithm is created in Simulink, target DSP code must be generated. Matlab's Real-time workshop and the specific builder, installed with dSPACE software package, provide building and downloading of user algorithms directly from Simulink. When the control algorithm is downloaded, real-time debugging, parameters adjustment and signals observation are realized with the Control Desk software package [LRSLP04].

The dSPACE DS-1104 DSP board forms the core of the control system. Aside from the duties of controlling the operator interface, it performs the acquisition of the feedback signals, computes a PWM signal, delivers the PWM signal to the SEPIC model, and determines the feedback signal with SEPIC model. The control algorithm is implemented on the main processor of the DS-1104 board in real-time.

B. SEPIC board

A 10-to-100W SEPIC is fabricated. The SEPIC board is shown in Fig. 3-11 (left part). Table 3-2 summarizes the parameters of the circuit. A MOSFET IRFR3518 is driven by a

PWM control signal from dSPACE via an optical fibre isolation and a driver. As the SMC control algorithms require all state variables, all the voltages and currents of different nodes must be measured by sensors.

In order to test the dynamic performances of the controllers, a load trigger circuit (Fig. 3-11 right part) is used to test the transient response of the SEPIC. It mainly consists of an optical coupler board (**Appendix A** shows the detailed circuit schematic) and an IRF540 driver, while the switch signal is generated via a digital-analog converter provided by dSPACE.

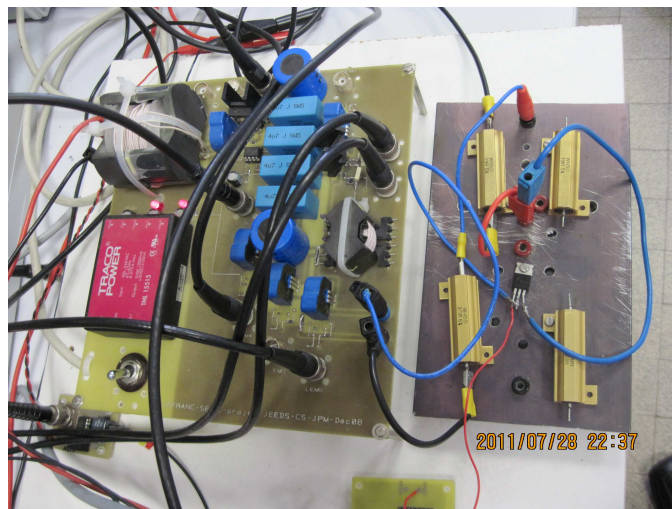


Fig. 3-11 Test platform of SEPIC board

Table 3-2:20kHz SEPIC prototype parameters

Symbol	Parameter name	Value
V_e	Input voltage	20V
V_{ref}	Reference voltage	20V
f_{sw}	Switching frequency	20kHz
L_1	Input Inductance	2.3mH
L_2	Output Inductance	330 μ H
C_1	Capacitor 1	190 μ F
C_2	Capacitor 2	190 μ F
R	Resistor	44 Ω
r_{L1}	Input Inductance ESR	2.134 Ω
r_{L2}	Output Inductance ESR	0.224 Ω

3.6.2 Experimental Validation in DSP Test Bench

To evaluate the performance of the proposed ISMC and DISMC schemes, these approaches are compared in the DSP test bench.

In the steady-state, a 44Ω resistor is connected with the SEPIC output terminal. To test the dynamic response of the controller, another load-line 44Ω resistor will be inserted and results in a final load of 22Ω . Fig. 3-12 illustrates the output voltage response comparison between the ISMC and DISM1. It shows that the ISMC has good response performances with short response time and lower voltage overshoot. However, it produces a steady state error of about 300mV due to the characteristics of ISMC. As introduced previously, the steady-state error is eliminated with DISM1. The input current response with DISM1 is given in Fig. 3-13. In addition, we can observe that the states responses have some noise disturbance, even though the system is stable. We believe that the steady-state noise disturbance is due to the hardware layout.

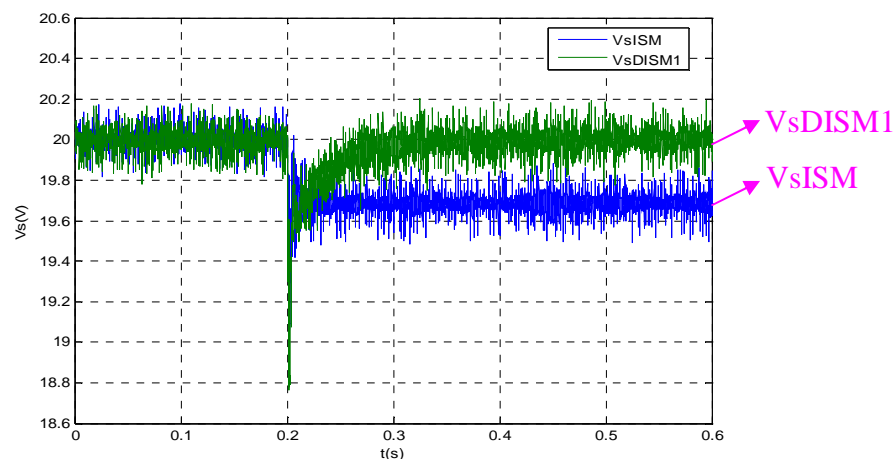


Fig. 3-12 Output voltage response comparison when load changes from 0.45A to 0.91A (44Ω to 22Ω)

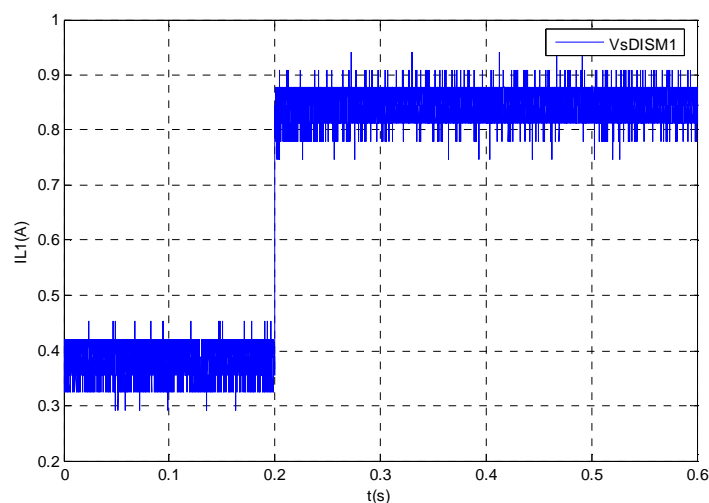


Fig. 3-13 Input current response when load changes from 0.45A to 0.91A (44Ω to 22Ω)

For the DISM1, besides of load variation, a reference voltage variation between 20V and 22V is realised. Fig. 3-14 shows that the DISM1 illustrates a good performance.

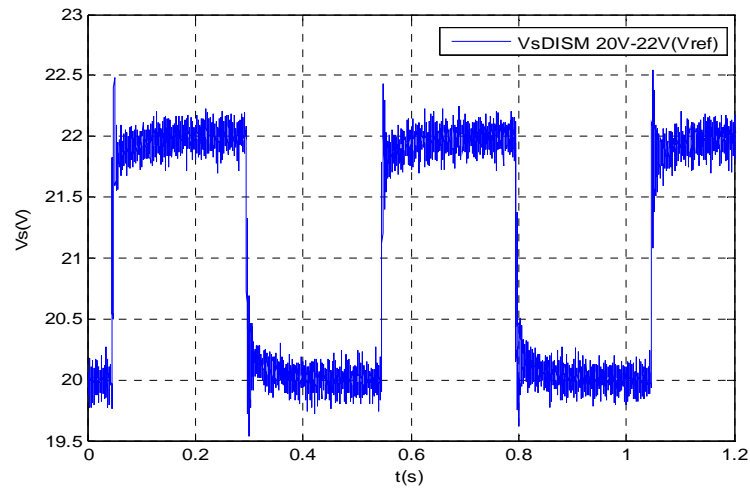


Fig. 3-14 Output voltage response when reference voltage changes between 20V and 22V

Under load changes from 0.45A to 0.91A (44Ω to 22Ω), the comparison between the dynamic behaviour of output voltage with DISM1 and DISM2 is shown in Fig. 3-15. We can see that when the SEPIC is in steady-state operating condition, the controllers maintain the desired output voltage (20V). In the transient condition, the response shows that the overshoot with both of them is less than 200mV, and DISM1 performs a shorter settling time than DISM2.

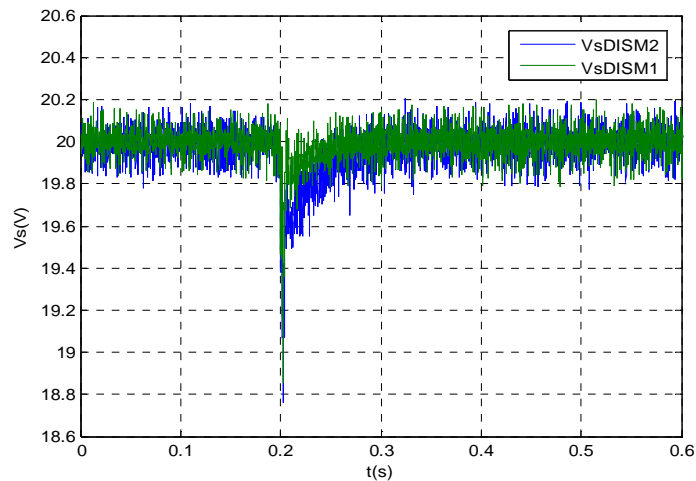


Fig. 3-15 Output voltage response comparison when load changes from 0.45A to 0.91A (44Ω to 22Ω)

3.7 SUMMARY

A general approach of deriving fixed-frequency PWM-based SM controllers is presented which is based on the equivalent control method for SEPIC operation. Different choices of

sliding surfaces have been studied. First, a simple integral sliding mode control is detailed to illustrate the design of this kind of controller. It has been shown that ISMC can't eliminate the static errors of the output voltage. The failure of the ISMC in alleviating the steady-state error of SEPIC has been examined. It is found that the problem is due to the absence of explicit integral term in the equivalent control law. In view of this, it has been proposed to add a double-integral term of the errors in the sliding surface. By including this additional term, the static error of the converter is alleviated. Moreover, to make the algorithm easier to be implemented, a simplified double integral sliding mode controller where the sliding surface only contains the double integral of voltage errors is proposed. Simulation tests have been carried out for both DISMC. Finally, a test platform based on dSPACE is established to validate the simulation results. It has been shown that the proposed DISM controllers are capable of achieving good performances.

CHAPTER 4 PREDICTIVE DEADBEAT DIGITAL CONTROLLER

With the development of faster and more powerful microprocessors, the implementation of new and complex control schemes for SEPIC is possible. In the previous chapter, the application of sliding mode control for SEPIC has been introduced. In this chapter, a new predictive deadbeat control scheme is proposed for the control of SEPIC.

Predictive deadbeat control presents several advantages: concepts are intuitive and easy to be understood; it can be applied to a variety of systems; constraints and nonlinearities can be easily included. Multivariable case can be considered and the resulting controller is easy to be implemented. The deadbeat technique has been used in many applications, especially oriented to motor drives and uninterruptible power supplies (UPS). It is an attractive control scheme for current-mode digital control in SMPS, due to their ability to cancel out or minimize the controlled variable error in one or a few switching periods and give very fast transient response for digital implementation [Dav98, BJ02, XZH09].

The investigation of predictive deadbeat control for DC/DC converter is relatively new. For SMPS applications, a predictive deadbeat technique for inductor-valley current-mode control of a buck DC/DC converter, in which the control action is updated only after two switching periods is presented [BJ02]. A sensorless deadbeat controller for the current control loop, where the current is estimated rather than measured is presented [KR04]. A thorough analysis of the predictive technique for peak, average and valley current-mode control for the three basic converters (buck, boost and buck-boost) and determines the appropriate modulation method to achieve predictive current control without oscillation problems is provided [CPEM03]. A comparative study of the current-control methods applied to DC/DC converters is performed [WLM07], showing that many different named current-mode control techniques are based on the same deadbeat concept.

To our knowledge, predictive deadbeat control has never been employed for the design of a controller for the high-order nonlinear SEPIC converter. This chapter presents a predictive deadbeat control for SEPIC. Our objective is to test the feasibility, the performance of this kind of controls and the possibility of the implementation in an embedded system. First, a discrete-time hybrid model of SEPIC for predictive deadbeat control is presented. Then a

multi-loop control structure is proposed for SEPIC with an internal deadbeat current control with fast dynamic response, which highlights a simple algorithm. A classical PI controller is used for the outer voltage control. In order to compensate the time delays due to digital control computation, we propose, for DSP implementation, a compensated deadbeat current control algorithm which improves the dynamic performance. For high speed applications like FPGA implementation, a simplification of algorithm is favourable. As the overall control delay is quite small with respect to the sampling period, the compensated algorithm is not required. The stability analysis of this simplified deadbeat current control algorithm is studied. Finally, simulation and experimental results confirm the properties of both proposed approaches.

4.1 PREDICTIVE DEADBEAT CURRENT CONTROL FOR SEPIC

The predictive deadbeat control is a discrete time control which consists of finding the input signal that must be applied to a system in order to bring the output to the reference value in the smallest number of time steps. For DC/DC converter application, it works on the principle of predicting the duty cycle of the next switching cycle based on the values obtained from the previous cycles [PF05, CPEM03, ME04]. For this, a discrete-time model is required. Generally, from the DC/DC converter hybrid model, a discrete-time hybrid model is derived that is valid for all the operating regime and captures the evolution of the state variables within the switching period.

4.1.1 Prediction Model

As we can see, the SEPIC converter features two topologies, where each topology has an associated linear continuous-time dynamic. Based on the hybrid model derived in chapter 2.1.1, the goal of this section is to derive a model of the converter that is suitable to serve as a prediction model for the predictive deadbeat control problem. This model should have the following properties: the model and the controller should be formulated in the discrete-time domain, as the manipulated variable given by the duty cycle is constant within the switching period and changes only at the time-instants kT_e , $k \in \mathbb{N}$. Second, it would be beneficial to capture the evolution of the states also within the switching period, as this would enable us to impose constraints in the states not only at time-instants but also at intermediate samples. As the converter is intrinsically hybrid in nature, we aim to retain the structure of the two operation modes and to take into account the hybrid character in designing the controller.

A working period T_e can be divided, by the duty cycle $\rho(k) = \frac{\Delta T_1}{T_e}$ as shown in Fig. 4-1, into two parts corresponding to the two states of the SEPIC.

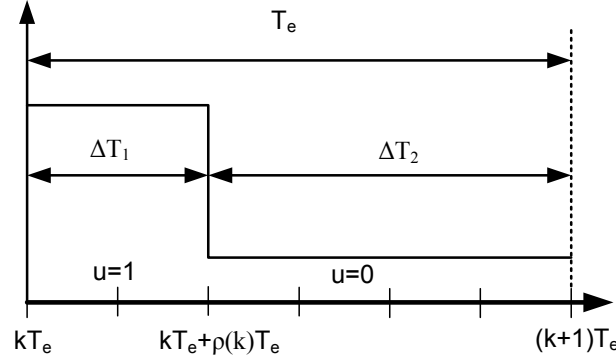


Fig. 4-1 A period of duty cycle $kT_e, kT_e + \rho(k)T_e, (k+1)T_e$

The state at the clock time kT_e is noted $x(k) = x(kT_e)$. We seek to explain the different variables $x(k+1) = x((k+1)T_e)$ at time $(k+1)T_e$ as a function of $x(k)$. For this, we must initially clarify the state at time $(k + \rho(k))T_e$.

When the switch state is “ON”, the duration is ΔT_1 , $\Delta T_1 = \rho(k)T_e$. The SEPIC in CCM mode is described by the same state equation as (2.1) which is a linear continuous system:

$$\dot{x}(t) = A_1 x(t) + B_1 v(t) \quad (4.1)$$

$$\text{with } x(t) = \begin{bmatrix} i_{L1}(t) \\ v_{C1}(t) \\ i_{L2}(t) \\ v_s(t) \end{bmatrix}, A_1 = \begin{bmatrix} -\frac{r_{L1}}{L_1} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_1} & 0 \\ 0 & -\frac{1}{L_2} & -\frac{r_{L2}}{L_2} & 0 \\ 0 & 0 & 0 & -\frac{1}{RC_2} \end{bmatrix}, B_1 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}, v(t) = v_e(t)$$

The discretization of this model between time interval $[kT_e, (k + \rho(k))T_e]$ can be made:

$$x((k + \rho(k))T_e) = F_1 x(k) + H_1 v(k) \quad (4.2)$$

Where $F_1 = \Phi_1(T) = e^{A_1 \Delta T_1} = I + A_1 \Delta T_1 + \frac{A_1^2 \Delta T_1^2}{2!} + \frac{A_1^3 \Delta T_1^3}{3!} + \dots$

$$H_1 = \Psi_1(T) B_1$$

$$\text{with } \Psi_1(T) = \int_{kT_e}^{kT_e + \rho(k)T_e} \Phi_1(kT_e + \rho(k)T_e - \tau) d\tau = I \Delta T_1 + \frac{A_1 \Delta T_1^2}{2!} + \frac{A_1^2 \Delta T_1^3}{3!} + \frac{A_1^3 \Delta T_1^4}{4!} + \dots$$

For the 20kHz switching frequency, the period is 5e-5s. It is a small calculation time, thus the influence of duration ΔT_1^2 and other higher orders of ΔT_1 are tiny, so they can be neglected, and only the first two items of F_1 and the first terms of H_1 are taken into account. Thus, we get

$$F_1 = \begin{bmatrix} 1 - \frac{r_{L1}}{L_1} \Delta T_1 & 0 & 0 & 0 \\ 0 & 1 & \frac{1}{C_1} \Delta T_1 & 0 \\ 0 & -\frac{1}{L_2} \Delta T_1 & 1 - \frac{r_{L2}}{L_2} \Delta T_1 & 0 \\ 0 & 0 & 0 & 1 - \frac{1}{RC_2} \Delta T_1 \end{bmatrix}, H_1 = \begin{bmatrix} \frac{\Delta T_1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

When the switch state is “OFF”, the duration is ΔT_2 , $\Delta T_2 = (1 - \rho(k))T_e$, the system is described by the same state equation as (2.2) which is a linear continuous system too:

$$\dot{x}(t) = A_2 x(t) + B_2 v(t) \quad (4.3)$$

$$\text{with } A_2 = \begin{bmatrix} -\frac{r_{L1}}{L_1} & -\frac{1}{L_1} & 0 & -\frac{1}{L_1} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & -\frac{r_{L2}}{L_2} & \frac{1}{L_2} \\ \frac{1}{C_2} & 0 & \frac{-1}{C_2} & -\frac{1}{RC_2} \end{bmatrix}, B_2 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

The discretization of this model in time interval $[(k + \rho(k))T_e, (k + 1)T_e]$ is written as

$$x((k + 1)T_e) = F_2 x((k + \rho(k))T_e) + H_2 v((k + \rho(k))T_e) \quad (4.4)$$

where $F_2 = \Phi_2(T) = e^{A_2 \Delta T_2} = I + A_2 \Delta T_2 + \frac{A_2^2 \Delta T_2^2}{2!} + \frac{A_2^3 \Delta T_2^3}{3!} + \dots$

$H_2 = \Psi_2(T)B_2$, with

$$\Psi_2(T) = \int_{kT_e + \rho(k)T_e}^{kT_e + T_e} \Phi_2(kT_e + T_e - \tau) d\tau = I \Delta T_2 + \frac{A_2 \Delta T_2^2}{2!} + \frac{A_2^2 \Delta T_2^3}{3!} + \frac{A_2^3 \Delta T_2^4}{4!} + \dots$$

With the same assumption as before, the following approximation is normally used

$$F_2 = \begin{bmatrix} 1 - \frac{r_{L1}}{L_1} \Delta T_2 & -\frac{1}{L_1} \Delta T_2 & 0 & -\frac{1}{L_1} \Delta T_2 \\ \frac{1}{C_1} \Delta T_2 & 1 & 0 & 0 \\ 0 & 0 & 1 - \frac{r_{L2}}{L_2} \Delta T_2 & \frac{1}{L_2} \Delta T_2 \\ \frac{1}{C_2} \Delta T_2 & 0 & -\frac{1}{C_2} \Delta T_2 & -\frac{1}{RC_2} \Delta T_2 + 1 \end{bmatrix}, H_2 = \begin{bmatrix} \frac{\Delta T_2}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

The input voltage is considered as a slow variable between kT_e and $(k+1)T_e$:

$$v((k + \rho(k))T_e) = v(kT_e) \quad (4.5)$$

From equations (4.2) and (4.4), we deduce the expression at time $(k+1)T_e$ as a function of that at time kT_e

$$\begin{aligned} x((k+1)T_e) &= F_2 x((k + \rho(k))T_e) + H_2 v((k + \rho(k))T_e) \\ &= F_2 x((k + \rho(k))T_e) + H_2 v(kT_e) \\ &= F_2 [F_1 x(kT_e) + H_1 v(kT_e)] + H_2 v(kT_e) \end{aligned} \quad (4.6)$$

Thus, the discrete-time hybrid model for SEPIC is written as follows

$$\begin{bmatrix} i_{L1}(k+1) \\ v_{C1}(k+1) \\ i_{L2}(k+1) \\ v_s(k+1) \end{bmatrix} = \begin{bmatrix} -\frac{r_{L1}}{L_1} T_e + 1 & -\frac{\Delta T_2}{L_1} & 0 & -\frac{\Delta T_2}{L_1} \\ \frac{1}{C_1} \Delta T_2 & 1 & \frac{1}{C_1} \Delta T_1 & 0 \\ 0 & -\frac{1}{L_2} \Delta T_1 & -\frac{r_{L2}}{L_2} T_e + 1 & \frac{1}{L_2} \Delta T_2 \\ \frac{1}{C_2} \Delta T_2 & 0 & -\frac{1}{C_2} \Delta T_2 & -\frac{1}{RC_2} T_e + 1 \end{bmatrix} \begin{bmatrix} i_{L1}(k) \\ v_{C1}(k) \\ i_{L2}(k) \\ v_s(k) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} T_e \\ 0 \\ 0 \\ 0 \end{bmatrix} v_e(k) \quad (4.7)$$

This model will be used to develop a predictive deadbeat control in the following.

4.1.2 Predictive Deadbeat Current Control for SEPIC

The predictive deadbeat control for SEPIC is based on the principle of current mode control which is usually implemented in DC/DC converter. The current mode control is a two-loop system where the objective of the inner loop is to control quickly the inductor current so that the outer voltage control loop can be designed easily supposing that the closed loop transfer function of the inner loop is equal to 1. In our work, the inner current loop compensator is based on a deadbeat control law, and the outer voltage loop compensator is based on a digital PI structure. In the following sections, we propose different types of deadbeat current loop control algorithms for SEPIC.

A. Conventional deadbeat control algorithm

As far as the current control is concerned, we take the first equation of model (4.7):

$$i_{L1}(k+1) = i_{L1}(k) - \frac{r_{L1}}{L_1} i_{L1}(k) T_e + \frac{1}{L_1} v_e(k) T_e - \frac{1}{L_1} (v_{C1}(k) + v_s(k)) \Delta T_2 \quad (4.8)$$

By replacing ΔT_2 by $(1-\rho(k))T_e$, we obtain:

$$i_{L1}(k+1) = i_{L1}(k) - \frac{r_{L1}}{L_1} i_{L1}(k) T_e + \frac{1}{L_1} v_e(k) T_e - \frac{1}{L_1} (v_{C1}(k) + v_s(k)) (1-\rho(k)) T_e \quad (4.9)$$

The above equation indicates that the inductor current i_{L1} at the beginning of the next switching cycle depends on the inductor current at the beginning of present switching cycle, on the input voltage v_e , on the capacitor voltage v_{C1} , on the output voltage v_s and on the duty cycle for the present switching cycle $\rho(k)$. Equation (4.9) can be rewritten as:

$$\rho(k) = 1 + \left[\frac{L_1}{T_e} (i_{L1}(k+1) - i_{L1}(k)) + r_{L1} i_{L1}(k) - v_e(k) \right] \frac{1}{(v_{C1}(k) + v_s(k))} \quad (4.10)$$

The duty cycle is calculated in order to make the measurement inductor current to track the reference based on the predictive model. In (4.9), $i_{L1}(k+1)$ is forced to follow the reference current value $i_{L1ref}(k+1)$. By substituting $i_{L1ref}(k+1)$ for $i_{L1}(k+1)$, the duty cycle can be derived as:

$$\rho(k) = 1 + \left[\frac{L_1}{T_e} (i_{L1ref}(k+1) - i_{L1}(k)) + r_{L1} i_{L1}(k) - v_e(k) \right] \frac{1}{(v_{C1}(k) + v_s(k))} \quad (4.11)$$

This is a conventional predictive deadbeat control. It calculates the duty cycle $\rho(k)$ to ensure that the inductor current reaches its reference by the end of the modulation period. As introduced, the difference equation is only one order, so the deadbeat control of $i_{L1}(k+1)$ is obtained in one sampling time. It is worth noticing that (4.11) depends neither on the value of the load, nor on the converter operating point.

B. Compensated deadbeat control algorithm

Comparing to analog control, one of the major disadvantages of digital control is the inherent time delay of the control loop, which comes from the PWM generation during the computation, [HTLCC07, KR04, XZH09, BJ00]. The effects of the control loop time delay can degrade significantly the control loop performances, reducing the controller bandwidth [COMS09, LML09, CPDM03, LS05].

The implementation of deadbeat control induces one sampling-period delay. Indeed, at k^{th} interrupt signal, the AD converter samples the required values such as $i_{L1}(k)$, $v_{C1}(k)$ and the output voltage $v_s(k)$ to calculate the duty cycle $\rho(k)$. This control value is uploaded and

applied at the $(k+1)^{\text{th}}$ interrupt signal. When the sampling period is large, this delay is not negligible and the compensation is needed to ensure the performance of the control. We propose a modified deadbeat control which can compensate one sampling-period delay. This induces that the current reference $i_{L1\text{ref}}$ will be reached at instant $(k+2)T_e$ instead of $(k+1)T_e$ as shown in Fig. 4-2.

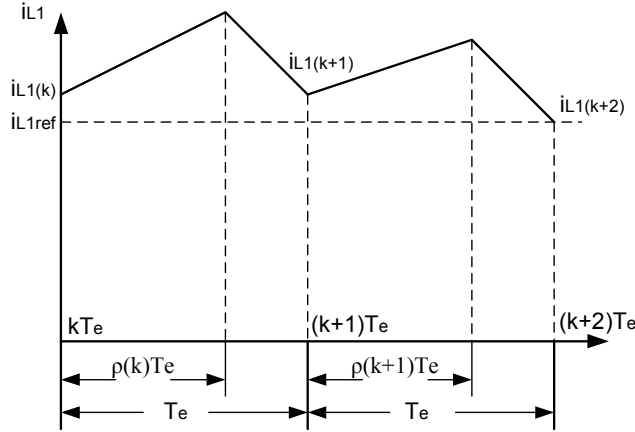


Fig. 4-2 Input inductor current waveform in the SEPIC

The current $i_{L1}(k+2)$ is expressed using (4.11):

$$\begin{aligned}
 i_{L1}(k+2) &= i_{L1\text{ref}} = \left(1 - \frac{r_{L1}}{L_1} T_e\right) i_{L1}(k+1) + \frac{T_e}{L_1} v_e(k) - \frac{1}{L_1} (v_{Cl}(k+1) + v_s(k+1)) (1 - \rho(k+1)) T_e \\
 &= \left(1 - \frac{r_{L1}}{L_1} T_e\right) \left(\left(1 - \frac{r_{L1}}{L_1} T_e\right) i_{L1}(k) + \frac{T_e}{L_1} v_e(k) - \frac{1}{L_1} (v_{Cl}(k) + v_s(k)) (1 - \rho(k)) T_e \right) \\
 &\quad + \frac{T_e}{L_1} v_e(k) - \frac{1}{L_1} (v_{Cl}(k+1) + v_s(k+1)) (1 - \rho(k+1)) T_e
 \end{aligned} \quad (4.12)$$

Equation (4.12) can be solved for the predicted duty cycle:

$$\rho(k+1) = 1 - \frac{\left((L_1 - r_{L1} T_e) i_{L1}(k) + v_e(k) T_e - (v_{Cl}(k) + v_s(k)) (1 - \rho(k)) T_e \right) \left(1 - \frac{r_{L1}}{L_1} T_e\right)}{T_e (v_{Cl}(k+1) + v_s(k+1))} + \frac{i_{L1\text{ref}} L_1 - v_e(k) T_e}{T_e (v_{Cl}(k+1) + v_s(k+1))} \quad (4.13)$$

In the current loop, the voltages can be considered as slowly varying over one period. For the practical application, it can be assumed that $v_e(k+1) = v_e(k)$, $v_{Cl}(k+1) = v_{Cl}(k)$, and $v_s(k+1) = v_s(k)$, thus (4.13) can be simplified as:

$$\rho(k+1) = 2 - \rho(k) - (1 - \rho(k)) \frac{r_{L1}}{L_1} T_e + \frac{\left((r_{L1} T_e - L_1) i_{L1}(k) - v_e(k) T_e \right) \left(1 - \frac{r_{L1}}{L_1} T_e\right) + i_{L1\text{ref}} L_1 - v_e(k) T_e}{T_e (v_{Cl}(k) + v_s(k))} \quad (4.14)$$

(4.14) gives the control law of the compensated deadbeat control where one sampling-period delay has been taken into account.

C. Simplified deadbeat control algorithm

When the converter works at very high switching frequency with fast A/D converters, and control algorithm execution are just a small fraction of the sampling period, which may be the case in FPGA implementation, the influence of delay in the digital implementation is tiny. Thus, the conventional deadbeat control can be applied. However, high switching frequency reduces the maximum duration allowed for computation time. In this paragraph, we propose a simplified predictive deadbeat algorithm which can reduce the computation time, and can easily be realized for FPGA implementation at the same time. The delay in the calculation is negligible.

By assuming that the k^{th} and $(k-1)^{\text{th}}$ period duty ratios are applied at time t_k , the corresponding input inductor current at the end of k^{th} cycle noted $i_{L_1}(k+1)|\rho(k)$ and $i_{L_1}(k+1)|\rho(k-1)$ are written respectively as:

$$i_{L_1}(k+1)|\rho(k) = \left(1 - \frac{r_{L_1}}{L_1} T_e\right) i_{L_1}(k) + \frac{1}{L_1} v_e(k) T_e - \frac{1}{L_1} (v_{C_1}(k) + v_s(k)) (1 - \rho(k)) T_e \quad (4.15)$$

$$i_{L_1}(k+1)|\rho(k-1) = \left(1 - \frac{r_{L_1}}{L_1} T_e\right) i_{L_1}(k) + \frac{1}{L_1} v_e(k) T_e - \frac{1}{L_1} (v_{C_1}(k) + v_s(k)) (1 - \rho(k-1)) T_e \quad (4.16)$$

Define $\Delta\rho(k) = \rho(k) - \rho(k-1)$ and $\Delta i_{L_1}(k+1) = i_{L_1}(k+1)|\rho(k) - i_{L_1}(k+1)|\rho(k-1)$. The difference of (4.15) and (4.16) gives :

$$\Delta i_{L_1}(k+1) = \frac{(v_{C_1}(k) + v_s(k)) T_e}{L_1} \Delta\rho(k) \quad (4.17)$$

With the same assumption as for the compensated deadbeat control, the output voltages can be considered as slowly varying and can be considered as constant between t_k and t_{k+1} . Under this assumption, $\Delta i_{L_1}(k+1)$ can be considered as proportional to $\Delta\rho(k)$. Fig. 4-3 gives a graphical representation of this prediction schemes. The current trajectory, $i_{L_1}(k+1)|\rho(k)$, is represented by the dotted line, and the solid line indicates the predictive current based on the duty cycle of last period, $i_{L_1}(k+1)|\rho(k-1)$. It shows that a variation of the duty ratio induces a proportional variation in the value of the inductor current increment.

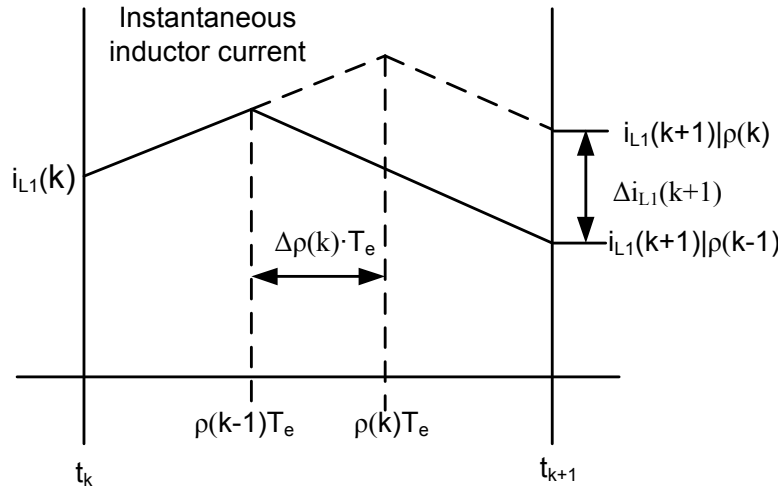


Fig. 4-3 Input inductor current during one switching period

The objective of deadbeat control consists to force that the current reaches its reference, ie $\Delta i_{L1}(k+1)$ represents the inductor current error, $\varepsilon = i_{L1ref} - i_{L1}(k+1)|\rho(k-1)$, that needs to be compensated. The duty ratio increment $\Delta\rho(k)$ can be calculated based on (4.17). The following deadbeat control law is thus obtained:

$$\rho(k) = \rho(k-1) + \frac{L_1}{(v_{Cl}(k) + v_s(k))T_e} (i_{L1ref} - i_{L1}(k+1)|\rho(k-1)) \quad (4.18)$$

This indicates that, if the duty cycle is calculated based on (4.18), then the inductor current at time t_{k+1} will reach its reference value.

A major difficulty in using (4.18) is to calculate $i_{L1}(k+1)|\rho(k-1)$. The idea is to use a linear extrapolation [BJ00] to calculate the current, one switching period after the other. The estimated current is obtained using the following expression:

$$\hat{i}_{L1}(k+1)|\rho(k-1) = 2i_{L1}(k)|\rho(k-1) - i_{L1}(k-1)|\rho(k-2) \quad (4.19)$$

Noting that $i_{L1}(k)|\rho(k-1)$ and $i_{L1}(k-1)|\rho(k-2)$ are available information at k^{th} period. Finally the simplified predictive deadbeat current control can be expressed as:

$$\rho(k) = \rho(k-1) + \frac{L_1}{(v_{Cl}(k) + v_s(k))T_e} (i_{L1ref} - 2i_{L1}(k)|\rho(k-1) + i_{L1}(k-1)|\rho(k-2)) \quad (4.20)$$

This controller will be used on FPGA platform.

D. Stability analysis

The performance of the predictive current controller, which is a model-based controller, depends on the accuracy of the model parameters. Despite the development and derivation of deadbeat control techniques for DC/DC converters, few works have treated the stability

analysis and the influence of converter parameters' mismatches on the stability conditions. Simple equations to show the trend of the controlled variables and current errors to converter parameters' mismatches are developed [KR04, CPEM03]. A more precise analysis is presented [MST05], where a transfer function between the reference current and the sampled current was derived, based on inductance value mismatch, stability analysis of the proposed scheme is studied. These stability analysis methods have been applied to buck or boost converter where the deadbeat controller is relatively simple.

In this section, we try to use these methods to analyse the effects of parameter variation on the stability of the current control loop for the high-order SEPIC. For the sake of simplicity, only the simplified predictive deadbeat control is studied. The same approach can be used for the conventional and compensated predictive control.

From the control algorithm, it can be seen that only the parameter L_1 is involved. Assuming that there is a parameter mismatch between the modelled input inductance and the actual one, we define L_m as the modelled inductor value in the control algorithm, L_1 presents the actual values of the input inductance, and α a factor which accounts for parameter mismatch, where $\alpha = L_m/L_1$. The predictive deadbeat current control for the SEPIC loop can be drawn in Fig. 4-4.

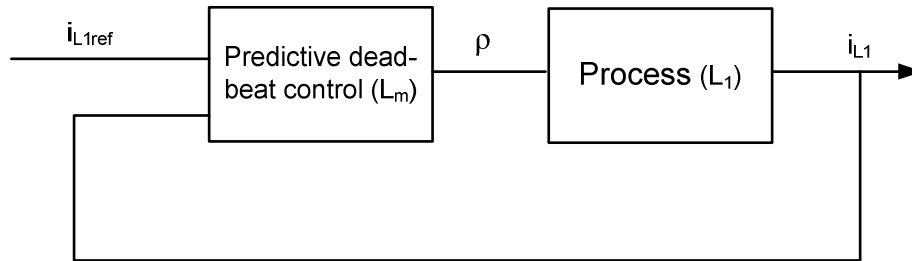


Fig. 4-4 Equivalent block diagram of the current control

Since the input and the output voltage are slowly varying signals, they can be considered constant during a switching period. By substituting L_m for L_1 , the control law (4.20) becomes:

$$\rho(k) - \rho(k-1) = \frac{L_m}{(V_{C1} + V_s)T_e} (i_{L1ref} - 2i_{L1}(k) + i_{L1}(k-1)) \quad (4.21)$$

From equation (4.15), the sampled inductor current and its value of previous cycle are respectively given:

$$i_{L1}(k+1) = i_{L1}(k) - \frac{r_{L1}T_e}{L_1} i_{L1}(k) + \frac{1}{L_1} V_e T_e - \frac{V_{C1} + V_s}{L_1} (1 - \rho(k)) T_e \quad (4.22)$$

$$i_{L1}(k) = i_{L1}(k-1) - \frac{r_{L1}T_e}{L_1} i_{L1}(k-1) + \frac{1}{L_1} V_e T_e - \frac{V_{Cl} + V_s}{L_1} (1 - \rho(k-1)) T_e \quad (4.23)$$

The relation between $i_{L1}(k+1)$ and $i_{L1}(k)$ can be deduced:

$$i_{L1}(k+1) - i_{L1}(k) = \left(1 - \frac{r_{L1}T_e}{L_1}\right) (i_{L1}(k) - i_{L1}(k-1)) + \frac{V_{Cl} + V_s}{L_1} (\rho(k) - \rho(k-1)) T_e \quad (4.24)$$

Substituting (4.21) into (4.24), and to perform the stability analysis of the closed-loop current control system, we can apply the Z-transform to (4.24).

$$i_{L1}(z) \left(z - 2 + \frac{r_{L1}T_e}{L_1} + z^{-1} - \frac{r_{L1}T_e}{L_1} T_e z^{-1} + 2\alpha - \alpha z^{-1} \right) = \alpha i_{L1ref}(z) \quad (4.25)$$

The closed loop transfer function can be obtained:

$$\frac{i_{L1}(z)}{i_{L1ref}(z)} = \frac{\alpha z}{\left(z^2 + (2\alpha - 2 + \frac{r_{L1}T_e}{L_1})z + (1 - \alpha - \frac{r_{L1}T_e}{L_1}) \right)} \quad (4.26)$$

Controller stability may be determined based on the location of the poles of the closed loop transfer function from i_{L1ref} to i_{L1} (4.26). We derive the characteristic polynomial of the closed-loop system and map the closed-loop poles. If the magnitude of the closed-loop poles is equal to or greater than one, the resulting system is, of course, unstable.

The characteristic polynomial is given by

$$z^2 + (2\alpha - 2 + \frac{r_{L1}T_e}{L_1})z + (1 - \alpha - \frac{r_{L1}T_e}{L_1}) = 0 \quad (4.27)$$

Fig. 4-5 gives the closed-loop poles of the system with predictive deadbeat control. It starts with $\alpha = 0.1$, and shows that underestimation of the inductor value L_1 does not cause stability problem. However, severe underestimation decreases the current control bandwidth. When α varies from 0.1 to 0.95, the system has complex conjugate pair, and the system becomes more and more stable. When α reaches the value 1, the system has two real roots. It shows that the system is stable as long as the parameter α is below a factor of around 1.3. When $\alpha > 1.3$, the magnitude of the closed-loop poles is greater than one, the resulting system is unstable.

Therefore, if the parameter α varies between 0.1 and 1.3, system stability is guaranteed. This stability analysis proves the robustness of the proposed control algorithm for parameters inaccuracy.

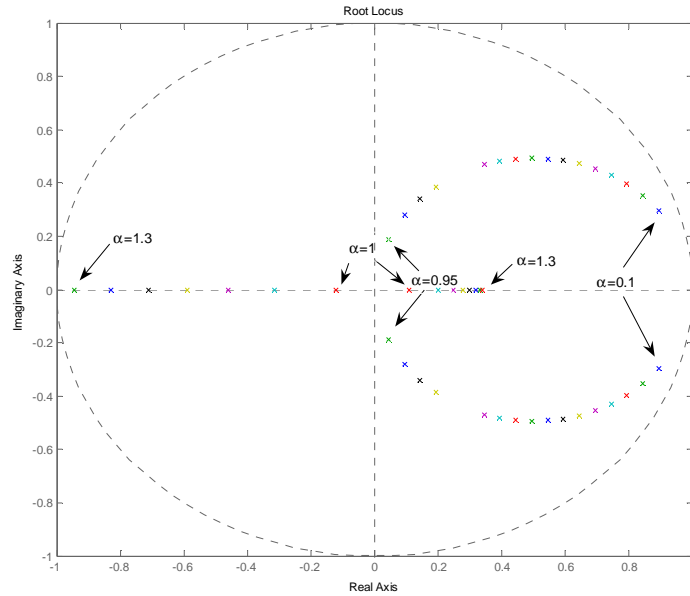


Fig. 4-5 Real and imaginary part of the closed-loop poles, α varies between 0.1 and 1.3

4.1.3 Output Voltage Control for SEPIC

The control of the output voltage is obtained using a compensator that sets the inner current loop reference. As the switching frequency f_{sw} is much higher than the natural frequencies of the converter, a continuous time controller can be designed and then Euler's transformation method can be applied to obtain the corresponding discrete time compensator.

Benefiting from the high inner loop dynamics, a PI compensator $K_p \left(1 + \frac{1}{T_i s} \right)$ is designed for outer voltage loop with using the small-signal model and sisotool in Matlab. The control parameters are chosen to get a good trade-off between the system bandwidth and stability. For 20kHz SEPIC, we choose a open-loop bode diagram with a phase margin of 38.4 degree and gain margin of 15.5dB as shown in Fig. 4-6, and the parameters $K_p=0.013$, $T_i=1/310$ are obtained.

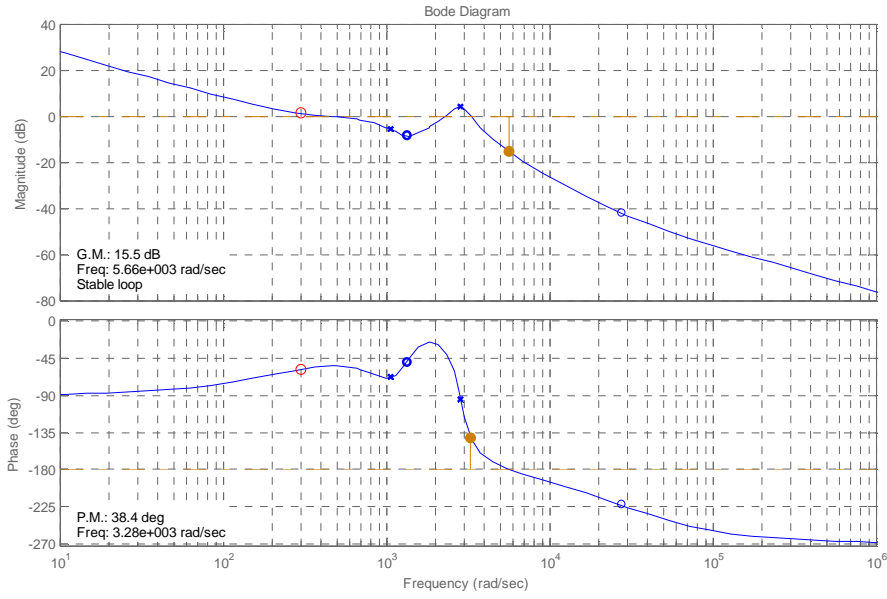


Fig. 4-6 Bode diagram of SEPIC with PI compensator(20kHz)

For 500kHz SEPIC, Fig. 4-7 shows the bode diagram of the system, and the parameters $K_p = 0.67$, $T_i = 1/150$ are obtained.

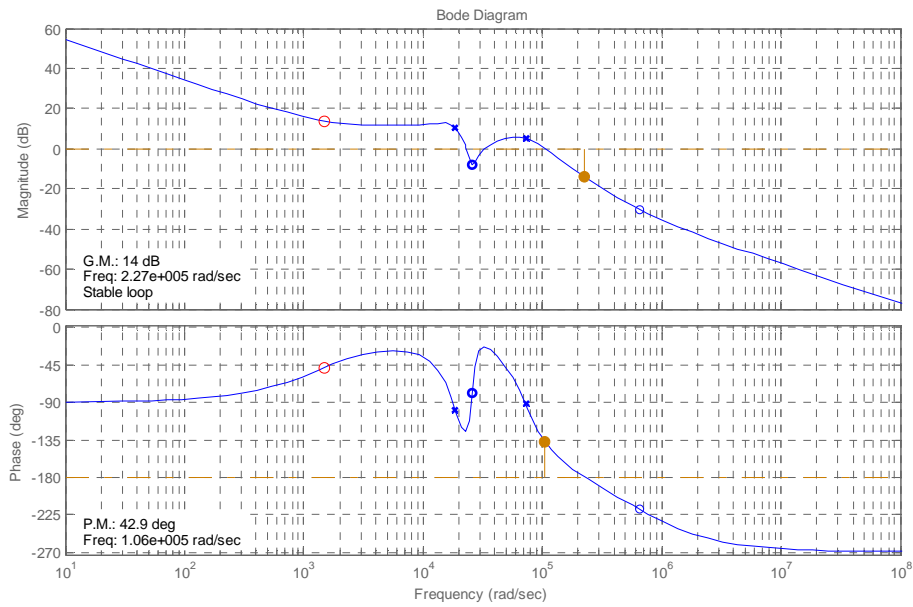


Fig. 4-7 Bode diagram of SEPIC with PI compensator(500kHz)

Fig. 4-8 shows the 2-loop scheme for a SEPIC converter.

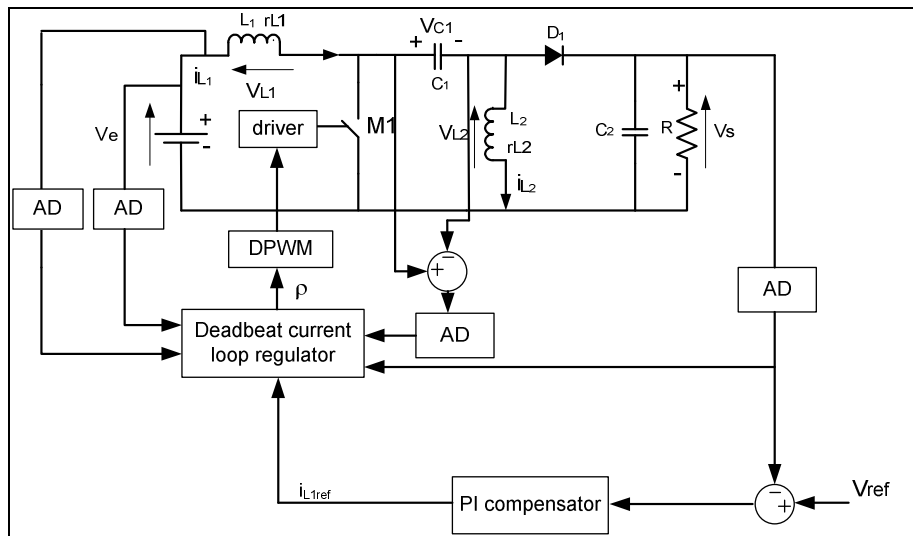


Fig. 4-8 Diagram of predictive deadbeat control for SEPIC

4.1.4 Simulation of Predictive Deadbeat Control for SEPIC

In this section two series of simulation are performed. The aim of the first one is to demonstrate the effectiveness of the proposed compensated deadbeat control algorithm in low switching frequency where the delay is not negligible. The second one validates the simplified deadbeat control algorithm by comparing with the compensated deadbeat control algorithm in high switching frequency condition. Both series are simulated using the same PI compensator for the output voltage control.

For the first series, the compensated deadbeat control algorithm is compared with the conventional predictive deadbeat control algorithm. The model and the parameters of the SEPIC converter are the same as that for SMC simulation test in chapter 3. The switching frequency is fixed at 20kHz that is used for dSPACE implementation. The dynamic responses of the controller with a step load change from 44Ω to 22Ω are shown in Fig. 4-9.

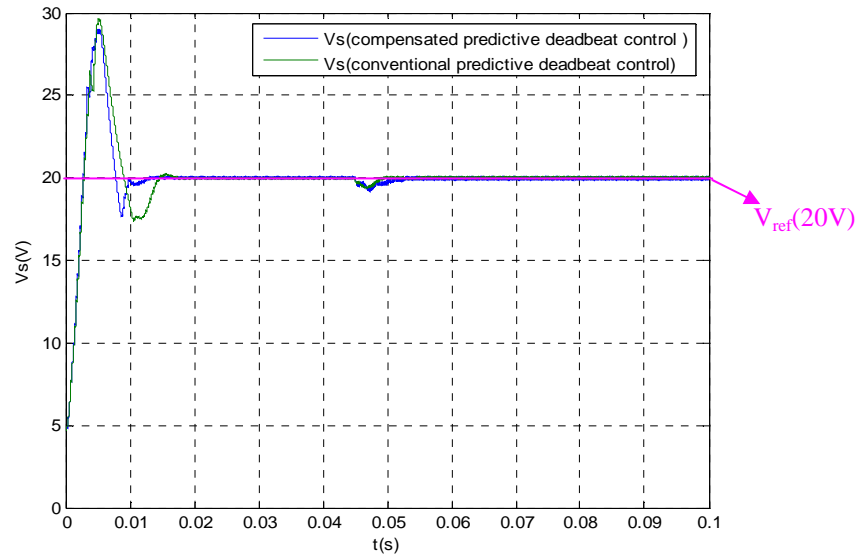


Fig. 4-9 Comparison of output voltage responses with load change from 44Ω to 22Ω at $t=0.045$ s

The simulation results show that both controllers are able to track the reference voltage closely. They show difference in performances in terms of settling time and overshoot obtained with the two controllers. The compensated deadbeat controller gives a better performance with a smaller settling time at the start time. In comparison, the conventional predictive deadbeat control is characterized by a longer settling time. For the dynamic response for load changes, as the simulation results illustrate, there is no big difference between the two controllers.

The second series of simulation correspond to the implementation into FPGA at switching frequency of 500kHz. Details of implementation are given along with chapter 6. The parameters of the SEPIC are given: input voltage $V_e=15V$, reference output voltage $V_{ref}=14V$, inductors $L_1=185\mu H$, $L_2=13\mu H$, parasitic ESRs of inductors $r_{L1}=1.2\Omega$, $r_{L2}=0.8\Omega$, $C_1=C_2=7.6\mu F$. The comparison between the simplified deadbeat controller and the compensated deadbeat controller during the load change transition from 20Ω to 13Ω is shown in Fig. 4-10.

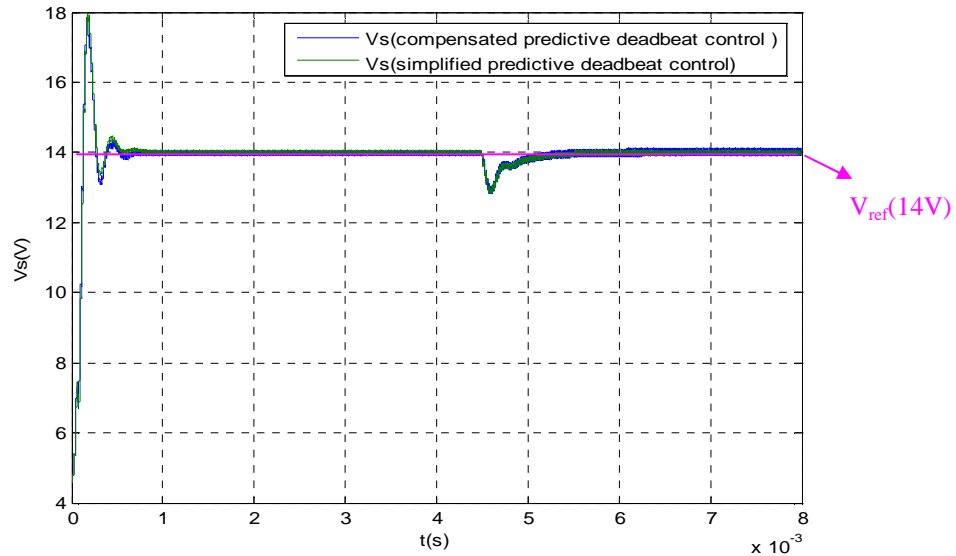


Fig. 4-10 Comparison of output voltage response with load change from 20Ω to 13Ω at $t=0.0045$ s

It is shown that the responses closely match between the two controllers. Thus for the high frequency application, the delay influence for the system can be ignored. So the simplified predictive deadbeat control can be adopted. The simulation results confirm that the two proposed predictive deadbeat control methods effectively guarantee that the instantaneous error between the sampled inductor current and the desired reference current will be reduced to zero quickly.

For the simplified predictive deadbeat control, the influence of model parameter variation is verified, we set α is equal to its ultimate value, $\alpha=0.1$ and $\alpha=1.3$. The output voltage responses under load change are respectively given in Fig. 4-11 and Fig. 4-12.

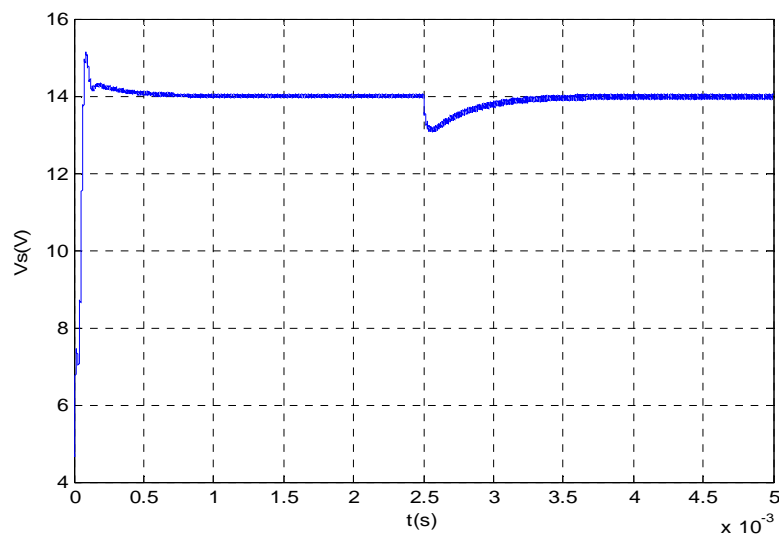


Fig. 4-11 Output voltage response with $\alpha=0.1$ under load change from 20Ω to 13Ω at $t=0.0025$ s

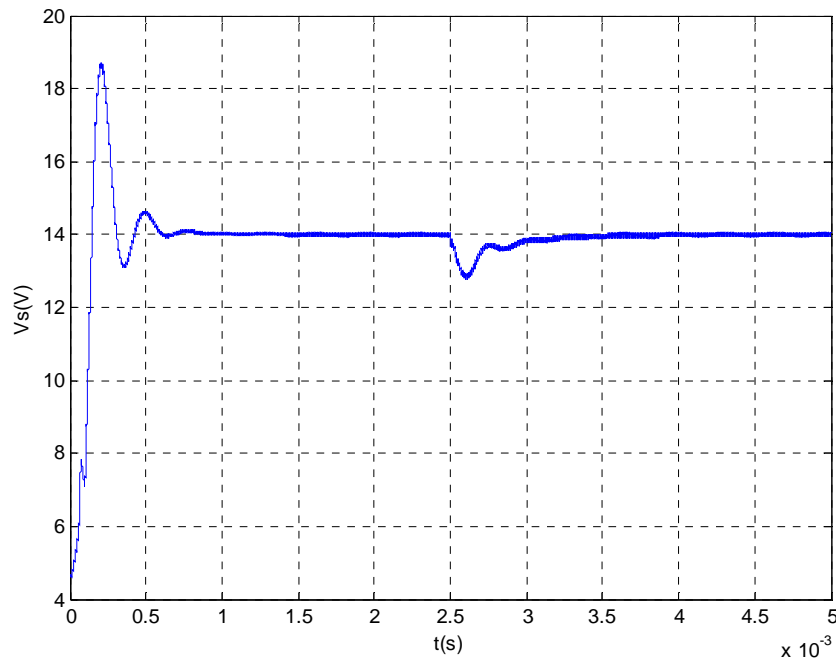


Fig. 4-12 Output voltage response with $\alpha=1.3$ under load change from 20Ω to 13Ω at $t=0.0025$ s

The simulation results show that the simplified predictive deadbeat control is also robust to model parameter variation as analysis.

4.1.5 Experimental Validation of Predictive Deadbeat Control

To evaluate the performance of the developed compensated predictive deadbeat control scheme, the control algorithm is implemented in the Simulink environment using a dSPACE DS1104. A test platform of the system working at low-frequency of 20kHz is established, and the value of the circuit components are the same as in chapter 3.

The transient response with reference voltage changes between 20V and 22V is shown in Fig. 4-13. The experimental results indicate that predictive deadbeat controller has a good performance in the transient response.

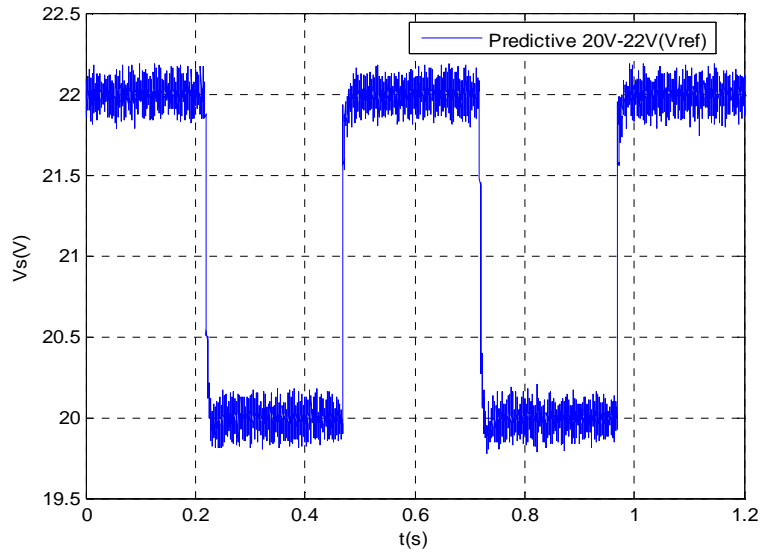


Fig. 4-13 Output voltage response when output reference voltage changes between 20V and 22V

Fig. 4-14 shows the output voltage transient response comparison between DISM1 and predictive deadbeat controller. In transient operation condition, when the load suddenly varies from 44Ω to 22Ω , the results show that the transient response is the same in the two cases. It takes almost 0.1s to recover to the steady-state. The corresponding input current response with predictive deadbeat controller is given in Fig. 4-15.

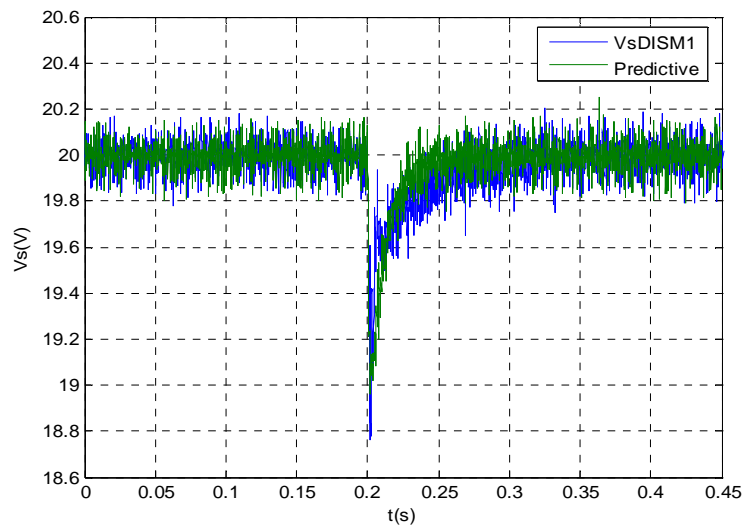


Fig. 4-14 Output voltage response comparison when load changes from 0.45A to 0.91A (44Ω to 22Ω)

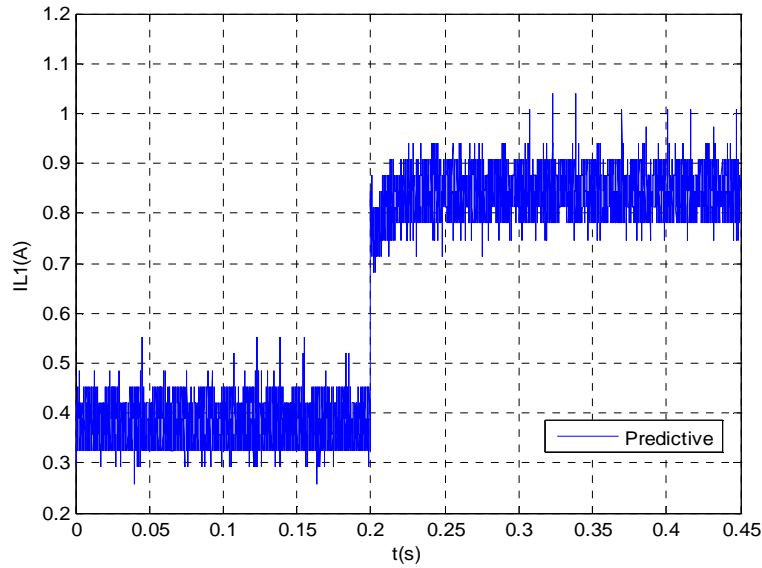


Fig. 4-15 Input current response when load changes from 0.45A to 0.91A (44 Ω to 22 Ω)

4.2 SUMMARY

In this chapter three predictive deadbeat controls have been presented for the inner current loop control of SEPIC. For this, a discrete-time hybrid SEPIC model is established and used as a prediction model. A conventional predictive deadbeat current controller is then determined. As one period delay exists for discrete time control application, a one cycle compensated deadbeat current controller is designed to reduce the influence produced by the delay. To meet the requirement of high switching frequency, a simplified deadbeat current controller is proposed. In order to study the robustness of the proposed simplified deadbeat current controller, the stability with regard to the input inductance variation is investigated, which provides a method for the stability analysis of SEPIC converter with predictive deadbeat control. Finally, the behaviour of the two proposed deadbeat current controllers is verified on a SEPIC converter using Matlab/Simulink. The simulation results verify that the proposed compensated deadbeat controller has a superior dynamic performance than conventional predictive deadbeat controller for a reference tracking, and the simplified deadbeat controller applied in a satisfying manner when SEPIC works at 500kHz. The compensated deadbeat controller algorithm is verified experimentally. The same system as with SMC working at switching frequency of 20kHz is implemented with the dSPACE platform. Experimental results verify the theoretical analysis and the simulation results. Thus we present an original operation of the predictive deadbeat control for SEPIC converter which features simple implementation and fast dynamic response. The FPGA implementation will be presented in the following chapters.

CHAPTER 5 OBSERVER DESIGN

The proposed control requires the knowledge of all the system states. The state vector has often been assumed to be accessible. This can be acceptable for a prototype circuit, but complicated enough in practical industrial application.

Measuring all the states of the system have the drawbacks of increasing the price of the system and making the integration into embedded system complicated. For the high frequency SEPIC application, only the output voltage is measured. Moreover, the load variation is important. An on-line estimation of the load can improve the control performances. Thus an investigation of observers which can observe all the states and estimate the load change is of great interest.

Furthermore, for high frequency SEPIC system targeted to FPGA and ASIC implementation, the numerous computations increase considerably the equivalent gate number in hardware implementation. The size and energy constraints request an observer with simple and realisable algorithms.

In this chapter, two nonlinear observers are presented. The first one is a sliding mode observer (SMO) which is based on sliding mode theory; the second one is an extended Kalman observer. In both cases, the load state is added to the state variables. Simulation results are performed to validate the proposed observers.

5.1 SLIDING MODE OBSERVER

Application of nonlinear sliding mode observers (SMC) for DC/DC converters [XS01, DFL05] is not a new subject. However, few works concerns high order SMO with the possibility to take into account the load variation. In [JOGLL10], a SMO is proposed by considering that the component uncertainties can be summarized and represented by a constant disturbance of the control signal (duty ratio). An additional observed state has been introduced to take into account these uncertainties. Unfortunately, this kind of SMO cannot observe accurately a large variation of load. In this section, we propose a simple SMO by considering the load variation as a new state variable.

As mentioned in chapter 2, the bilinear model of SEPIC can be written as the form:

$$\begin{cases} \dot{x} = (\rho A_1 + (1-\rho)A_2)x + (\rho B_1 + (1-\rho)B_2)v_e \\ y = \rho c_1^T x + (1-\rho)c_2^T x \end{cases} \quad (5.1)$$

Where $x = [x_1 \ x_2 \ x_3 \ x_4]^T = [i_{L1} \ v_{C1} \ i_{L2} \ v_s]^T$.

A reformulation of equation (2.8) gives:

$$\begin{cases} \dot{x}_1 = -\frac{r_{L1}}{L_1}x_1 + (\rho-1)\frac{1}{L_1}x_2 + (\rho-1)\frac{1}{L_1}x_4 + \frac{1}{L_1}v_e \\ \dot{x}_2 = (1-\rho)\frac{1}{C_1}x_1 + \frac{\rho}{C_1}x_3 \\ \dot{x}_3 = -\frac{\rho}{L_2}x_2 - \frac{r_{L2}}{L_2}x_3 + (1-\rho)\frac{1}{L_2}x_4 \\ \dot{x}_4 = (1-\rho)\frac{1}{C_2}x_1 + (\rho-1)\frac{1}{C_2}x_3 - \frac{1}{RC_2}x_4 \\ y = x_4 \end{cases} \quad (5.2)$$

In order to take into account load variation, a fifth state is introduced in (5.2): $x_5 = \frac{1}{R}$. This augments the system's order by one. The new extended system is of fifth order as:

$$\begin{cases} \dot{x}_1 = -\frac{r_{L1}}{L_1}x_1 + (\rho-1)\frac{1}{L_1}x_2 + (\rho-1)\frac{1}{L_1}x_4 + \frac{1}{L_1}v_e \\ \dot{x}_2 = (1-\rho)\frac{1}{C_1}x_1 + \frac{\rho}{C_1}x_3 \\ \dot{x}_3 = -\frac{\rho}{L_2}x_2 - \frac{r_{L2}}{L_2}x_3 + (1-\rho)\frac{1}{L_2}x_4 \\ \dot{x}_4 = (1-\rho)\frac{1}{C_2}x_1 + (\rho-1)\frac{1}{C_2}x_3 - \frac{1}{C_2}x_4x_5 \\ \dot{x}_5 = 0 \\ y = x_4 \end{cases} \quad (5.3)$$

Which can be written as:

$$\dot{x}_e(t) = f(x(t), \rho(t)) \quad (5.4)$$

The output vector is

$$y_e(t) = h(x(t)) = x_4 \quad (5.5)$$

The goal is to design a state observer that uses the output voltage x_4 to estimate the other variables. The proposed SMO is as follows where symbol \wedge means that it is an observed value:

$$\left\{ \begin{array}{l} \dot{\hat{x}}_1 = -\frac{r_{L1}}{L_1} \hat{x}_1 + (\rho-1) \frac{1}{L_1} \hat{x}_2 + (\rho-1) \frac{1}{L_1} \hat{x}_4 + \frac{1}{L_1} v_e + g_1 M \operatorname{sgn}(x_4 - \hat{x}_4) \\ \dot{\hat{x}}_2 = (1-\rho) \frac{1}{C_1} \hat{x}_1 + \frac{\rho}{C_1} \hat{x}_3 + g_2 M \operatorname{sgn}(x_4 - \hat{x}_4) \\ \dot{\hat{x}}_3 = -\frac{\rho}{L_2} \hat{x}_2 - \frac{r_{L2}}{L_2} \hat{x}_3 + (1-\rho) \frac{1}{L_2} \hat{x}_4 + g_3 M \operatorname{sgn}(x_4 - \hat{x}_4) \\ \dot{\hat{x}}_4 = (1-\rho) \frac{1}{C_2} \hat{x}_1 + (\rho-1) \frac{1}{C_2} \hat{x}_3 - \frac{1}{C_2} \hat{x}_4 \hat{x}_5 - M \operatorname{sgn}(x_4 - \hat{x}_4) \\ \dot{\hat{x}}_5 = g_4 M \operatorname{sgn}(x_4 - \hat{x}_4) \end{array} \right. \quad (5.6)$$

g_1 , g_2 , g_3 and g_4 are the observer gains and M is a positive constant. $\operatorname{sgn}(x_4 - \hat{x}_4)$ is a nonlinear function of the error between the measured output y and the estimated output \hat{x}_4 .

Defining $S = x_4 - \hat{x}_4$ as the sliding surface with $\operatorname{sgn}(S) = \begin{cases} 1 & \text{if } S > 0 \\ -1 & \text{if } S < 0 \end{cases}$. The discontinuous control $\operatorname{sgn}(x_4 - \hat{x}_4)$ forces the estimate of the measured state to have zero error in finite time.

The stability of the extended sliding mode observer is a complex work. The stability is demonstrated in [MLPL12] by using the averaged model of a port-Hamiltonian representation of the converter. We use the stability condition to determine the boundaries of observer gains.

As the observer is dedicated to the high-frequency SEPIC converter, we propose to test the observer in simulation at 500kHz. The SEPIC circuit parameters are: $L_1=185\mu\text{H}$, $L_2=13\mu\text{H}$, $r_{L1}=1.2\ \Omega$, $r_{L2}=0.8\ \Omega$, $V_e=15\text{V}$. The observer is designed with the values: $M=1500$, $G_c=(g_1, g_2, g_3, g_4)=(-0.0822, 0.7284, 0.2486, -0.0066)^T$.

The observer was tested without using the observed variables in the control what we call “free-wheel observer”, and the duty cycle ρ is fixed at 0.5. Fig. 5-1 shows the state variables comparison between the actual values and the observed values for the load variation from 20Ω to 13.3Ω at 0.0045s. It can be seen that in the simulation, the dynamics are smoother and follow the actual values, but with acceptable errors.

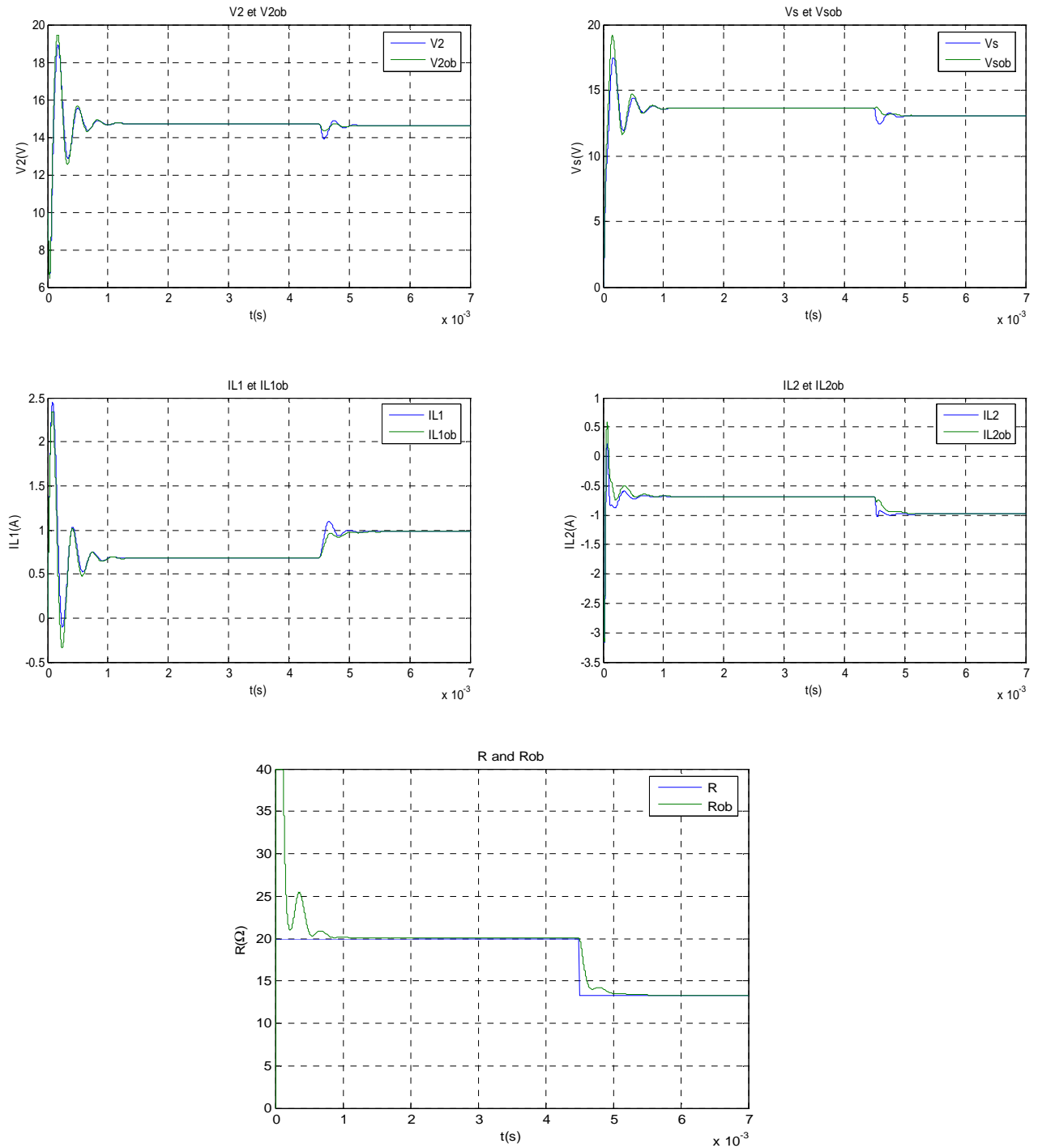


Fig. 5-1 Waveforms of actual and observed state variables for an open-loop SEPIC

In order to test the proposed observer on closed loop with a controller, the DISM1 controller presented in chapter 3 is implemented by using the sliding mode observer with only the measurement of output voltage. To show the performance of the controller, the load is being varied from 20Ω to 13.3Ω at 0.0045s, the dynamic performance of the sliding mode observer based on DISM1 controller scheme is shown in Fig. 5-2.

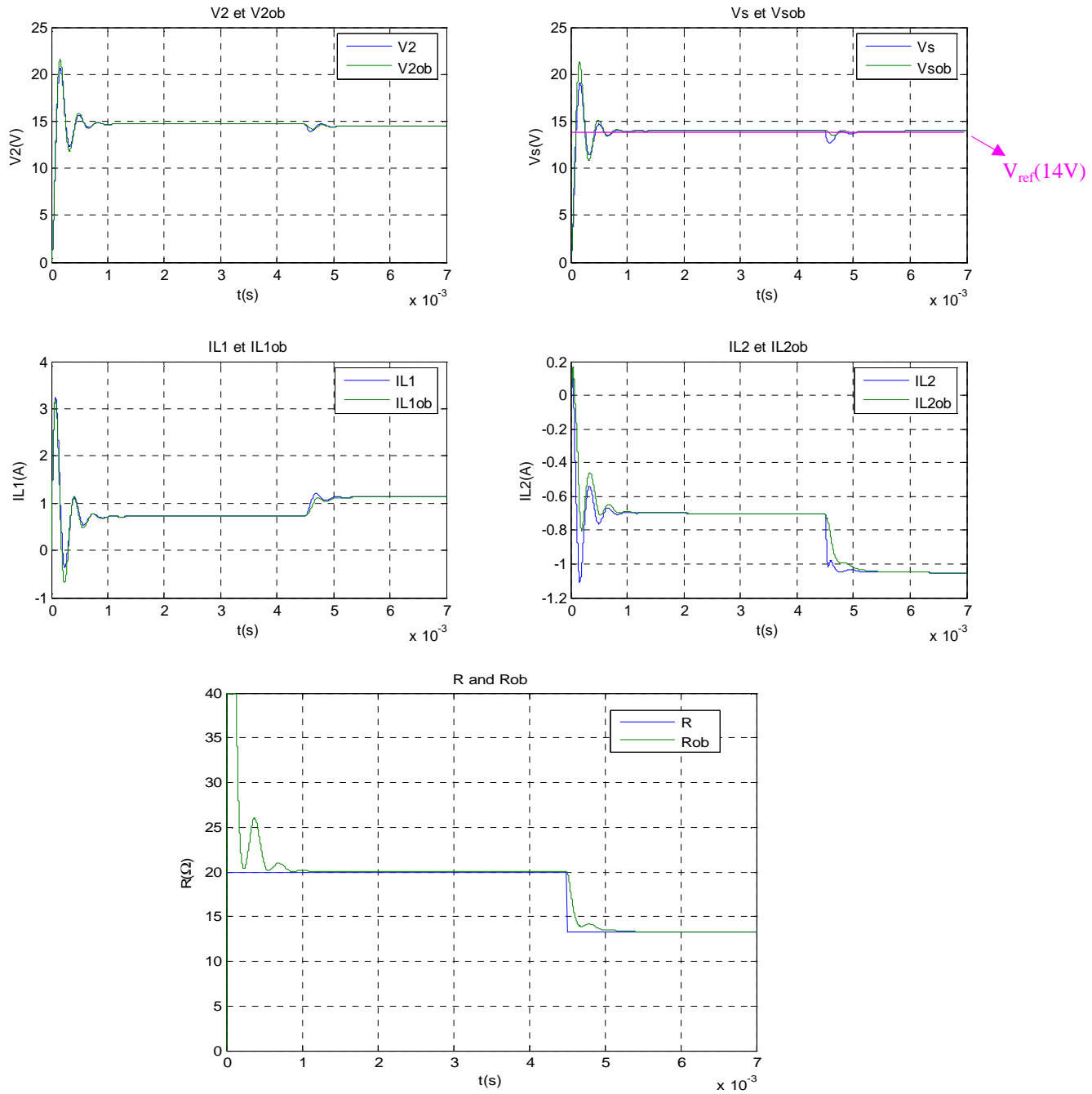


Fig. 5-2 Waveforms of actual and observed state variables with DISM1 controller

DISM1 controller based on extended sliding mode observer gives satisfactory results for this application of SEPIC. Sliding mode observer seems to be a good choice, since it is shown to be robust against load variation. However, in practice, it is found that this class of observers presents the main drawback of sliding mode, i.e. the chattering effect (which appears when “sign” function is used in control law) as the estimation error dynamics directly depend on a discontinuous function. This phenomenon could generate high-frequency oscillations on the observation results, which could be destructive for the control and the system in practical

application. For a FPGA implementation, a discrete-time observer designed by a discrete-time model is preferable rather than continuous time observer.

5.2 EXTENDED KALMAN OBSERVER

One of the most well-known and used discrete-time observers is the Kalman filter [GH92, DFL05]. The Kalman filter is a set of mathematical equations that provide an efficient computational (recursive) mean to estimate the state of a process, in a way that minimizes the mean of the squared error. The filter is very powerful in several aspects: it supports estimations of past, present, and even future states, and it performs successfully when the precise nature of the modelled system is unknown.

Normally, the Kalman filter addresses the general problem of trying to estimate the state of a discrete-time controlled process that is governed by a linear stochastic difference equation. The basic Kalman filter is limited to a linear assumption. More complex systems, however, can be nonlinear. Some of the most interesting and successful applications of Kalman filtering have been in such situations. In those cases, an extended Kalman filter can be applied.

Taking the same extended model as (5.3) and adding the random variables, $w(t)$ and $r(t)$, that represent respectively the process and measurement noises, the extended state equation becomes:

$$\dot{x}(t) = f(x(t), p(t), w(t)) \quad (5.7)$$

$$y(t) = h(x(t), r(t)) \quad (5.8)$$

The process noise is assumed to be drawn from a zero mean multivariate normal distribution with covariance Q , and measurement noise is assumed to be zero mean Gaussian white noise with covariance J . The noise covariance matrixes are defined as follows:

$$Q = \text{cov}(w) = E(w, w^T) \quad (5.9)$$

$$J = \text{cov}(r) = E(r, r^T) \quad (5.10)$$

The system (5.7) is strongly nonlinear. The standard EKF formulation can be used to achieve nonlinear state estimation. The Jacobian matrix is needed to linearize the nonlinear dynamic system in order to implement the Kalman filter calculation. Therefore, the linearization of (5.7) gives

$$\begin{cases} \dot{x} = A'x + B'\rho + I \\ y = c'x \end{cases} \quad (5.11)$$

where A' and B' are the Jacobian matrix defined as partial derivatives of f with respect to x , ρ and I is a constant matrix, $\theta = \frac{1}{R}$.

$$A' = \frac{\partial f}{\partial x} = \begin{bmatrix} -\frac{r_{L1}}{L_1} & \frac{\bar{\rho}-1}{L_1} & 0 & \frac{\bar{\rho}-1}{L_1} & 0 \\ \frac{1-\bar{\rho}}{C_1} & 0 & \frac{\bar{\rho}}{C_1} & 0 & 0 \\ 0 & -\frac{\bar{\rho}}{L_2} & -\frac{r_{L2}}{L_2} & \frac{1-\bar{\rho}}{L_2} & 0 \\ \frac{1-\bar{\rho}}{C_2} & 0 & \frac{\bar{\rho}-1}{C_2} & \frac{\bar{\theta}}{C_2} & -\frac{\bar{v}_s}{C_2} \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}, B' = \begin{bmatrix} \frac{\bar{v}_{C1} + \bar{v}_s}{L_1} \\ \frac{\bar{i}_{L2} - \bar{i}_{L1}}{C_1} \\ -\frac{\bar{v}_{C1} + \bar{v}_s}{L_2} \\ \frac{\bar{i}_{L2} - \bar{i}_{L1}}{C_2} \\ 0 \end{bmatrix}, I = \begin{bmatrix} \frac{V_e}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

With $\bar{\rho}, \bar{v}_{C1}, \bar{v}_s, \bar{i}_{L1}, \bar{i}_{L2}, \bar{\theta}$ the equilibrium point.

After discretization with sampling period T_e , (5.11) becomes:

$$\begin{cases} x_k = A'_{k-1} x_{k-1} + B'_{k-1} \rho_{k-1} + I \\ y_k = c' x_{k-1} \end{cases} \quad (5.12)$$

Since the EKF on-line calculation is quite heavy, the following approximation is normally used.

$$\begin{cases} A'_{k-1} = e^{A'T_e} \approx I + A'T_e \\ B'_{k-1} \approx B'T_e \end{cases} \quad (5.13)$$

The Kalman filter estimates a process by using a form of feedback control: the filter estimates the process state at some time and then obtains feedback in the form of (noisy) measurements. As such, the equations for the Kalman filter fall into two groups: time update equations and measurement update equations. The time update equations are responsible for projecting forward (in time) the current state and error covariance estimates to obtain the “a priori” estimates for the next time step. The measurement update equations are responsible for the feedback, i.e. for incorporating a new measurement into the “a priori” estimate to obtain an improved “a posteriori” estimate.

Defining matrix P as the error covariance of state estimation:

$$P_k = E\{e_k \cdot e_k^t\} = \sum_{i=1}^5 \left\{ [x_i - \hat{x}_i] \cdot [x_i - \hat{x}_i]^t \right\} \quad (5.14)$$

$E\{.\}$ is the computation of expectation value.

The EKF is then derived by the following iteration:

EKF time update equations:

- 1) Prediction of the state

$$\hat{\mathbf{x}}_{k|k-1} = \mathbf{A}'_{k-1} \hat{\mathbf{x}}_{k-1|k-1} + \mathbf{B}'_{k-1} \boldsymbol{\rho}_{k-1} + \mathbf{I} \quad (5.15)$$

- 2) Prediction of the covariance

$$\mathbf{P}_{k|k-1} = \mathbf{A}'_{k-1} \mathbf{P}_{k-1|k-1} \mathbf{A}_{k-1}{}^T + \mathbf{Q} \quad (5.16)$$

EKF measurements update equations:

- 1) Based on statistic methods and in order to minimize the covariance of the error:

$$\mathbf{K}_k = \mathbf{P}_{k|k-1} \mathbf{c}'^T (\mathbf{P}_{k|k-1} \mathbf{c}'^T + \mathbf{J})^{-1} \quad (5.17)$$

- 2) Update estimation with measurement

$$\hat{\mathbf{x}}_{k|k} = \hat{\mathbf{x}}_{k|k-1} + \mathbf{K}_k (\mathbf{y}_k - \mathbf{c}' \hat{\mathbf{x}}_{k|k-1}) \quad (5.18)$$

- 3) Update the error covariance matrix

$$\mathbf{P}_{k|k} = \mathbf{P}_{k|k-1} - \mathbf{K}_k \mathbf{c}' \mathbf{P}_{k|k-1} \quad (5.19)$$

To get the best trade off between stability and convergence time, the matrix \mathbf{Q} and \mathbf{J} are given as

$$\mathbf{Q} = \begin{bmatrix} 0.001 & 0 & 0 & 0 & 0 \\ 0 & 0.001 & 0 & 0 & 0 \\ 0 & 0 & 0.001 & 0 & 0 \\ 0 & 0 & 0 & 0.001 & 0 \\ 0 & 0 & 0 & 0 & 0.001 \end{bmatrix} \quad \mathbf{J} = \begin{bmatrix} \begin{bmatrix} 0.01 & 0 & 0 & 0 & 0 \\ 0 & 0.01 & 0 & 0 & 0 \\ 0 & 0 & 0.01 & 0 & 0 \\ 0 & 0 & 0 & 0.01 & 0 \\ 0 & 0 & 0 & 0 & 0.01 \end{bmatrix} \end{bmatrix}$$

The observer was tested without using the observed variables in the control at the switching frequency $f_{sw}=500\text{kHz}$ with the same parameters as previous SMO.

Fig. 5-3 shows the compared state variables between the actual values and the observed values for the load variation from 20Ω to 13.3Ω at 0.0045s . The figures show the observed values can exactly follow the measurement values with the Kalman filter in the open loop.

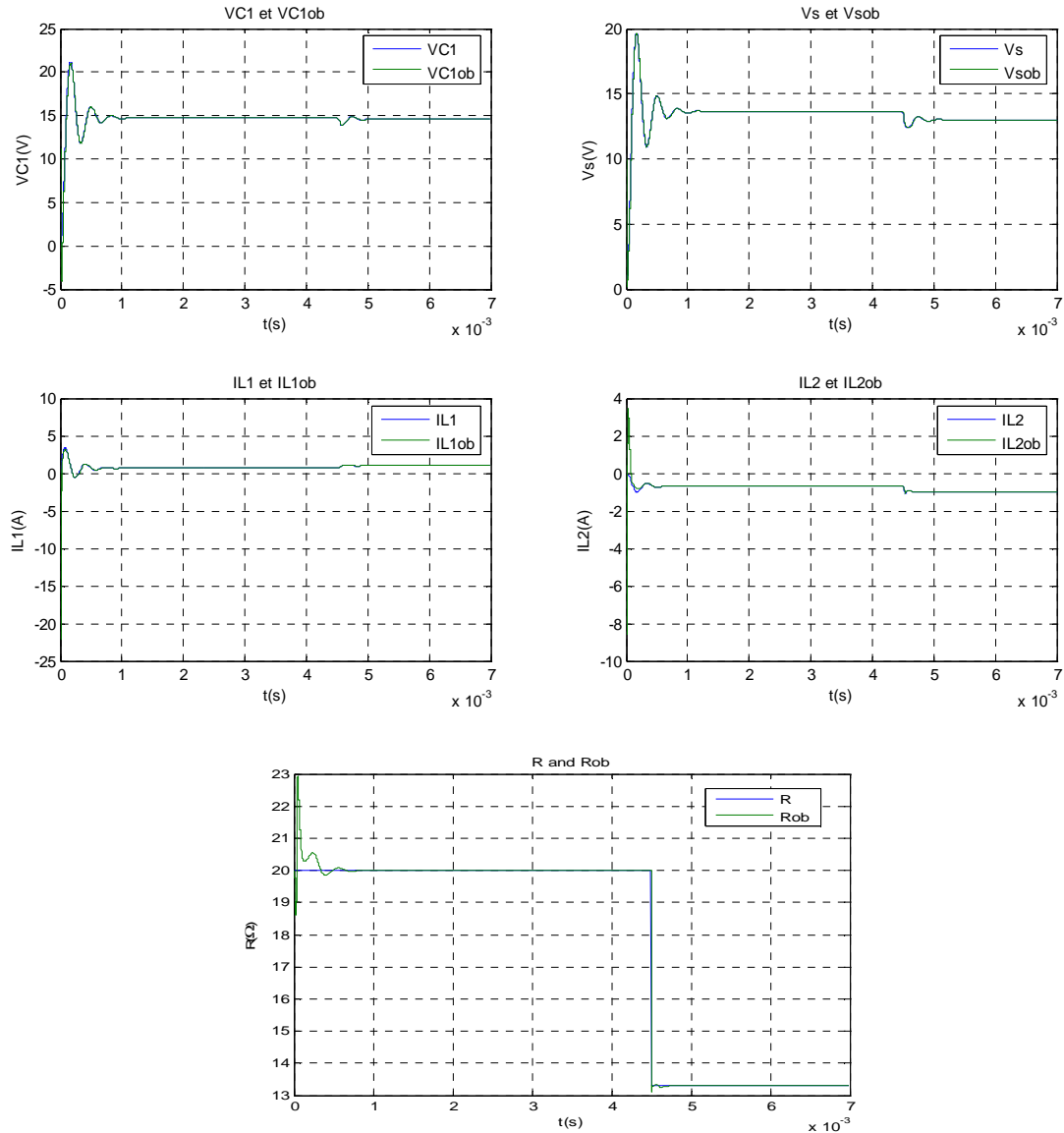


Fig. 5-3 Waveforms of actual and observed state variables for an open-loop SEPIC

The DISM1 controller is implemented by using the observed states from extended Kalman observer. To verify the performance of the controller, a step variation from 12V to 14V in the reference voltage is applied to test the tracking ability of the proposed observer. The high dynamic performance towards reference variation of the controller using observed states rather than measured one is shown in Fig. 5-4. We can notice an excellent performance for the observer which can quickly estimate the state variables.

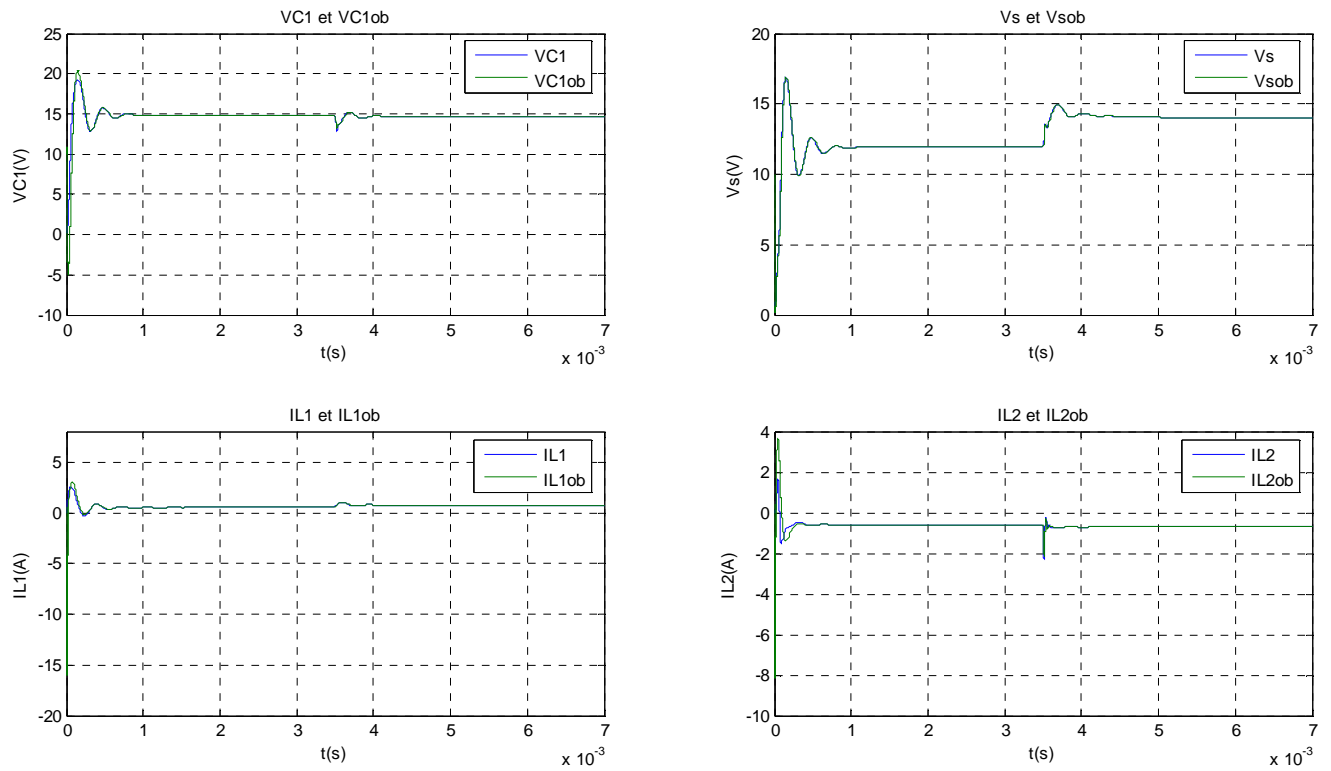


Fig. 5-4 Waveforms of actual and observed state variables for reference voltage variations

For a load variation between 20Ω to 13.3Ω at $0.0045s$, the dynamic performance of the system (controller-observer) is shown in Fig. 5-5. It demonstrates that the converter is able to maintain the output voltage with the output load changes.

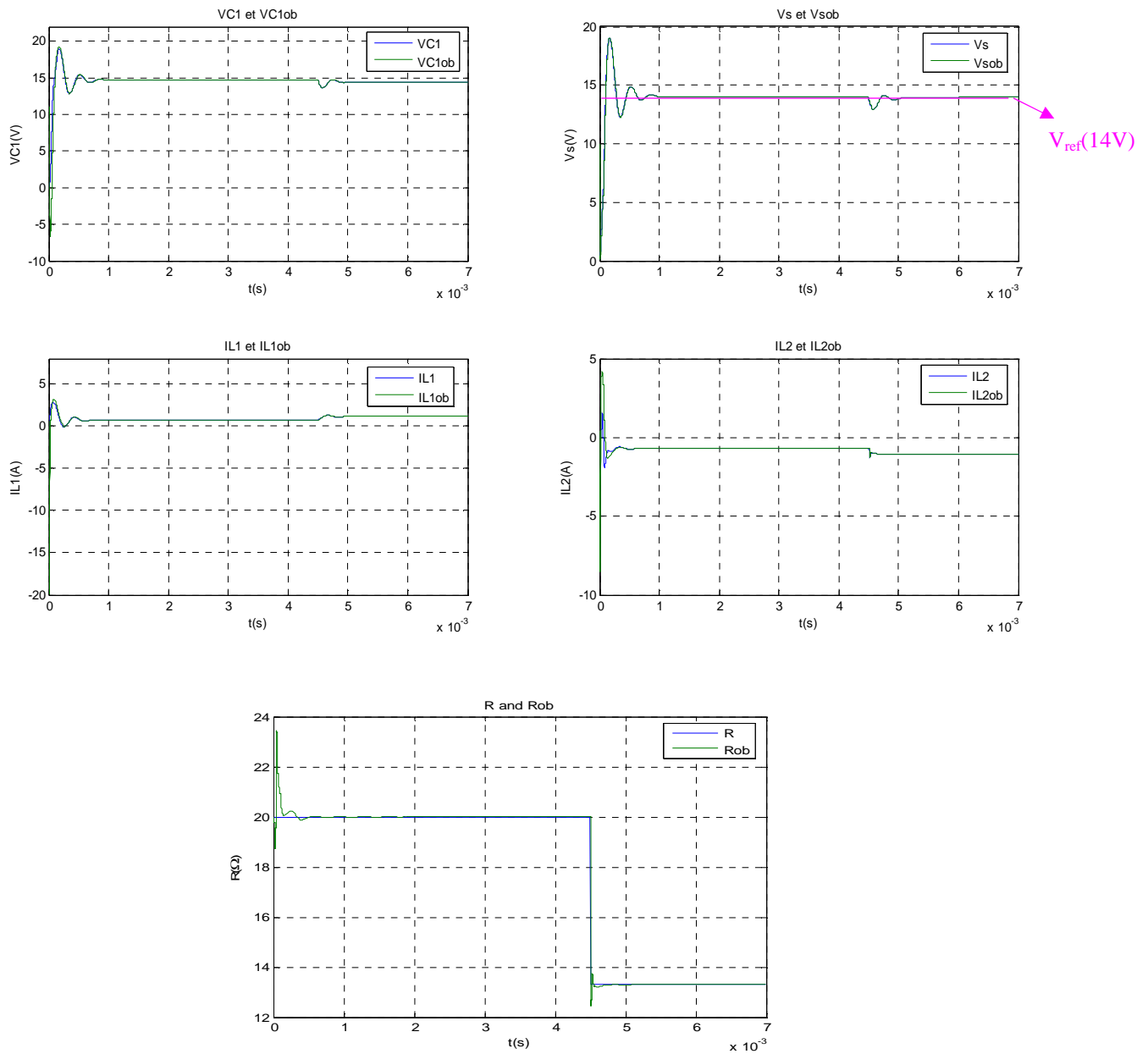


Fig. 5-5 The waveforms of actual and observed state variables with DISM1 controller

Thus, the above results show that the proposed system combining extended Kalman observer scheme and DISM1 controller allows SEPIC converter to operate under reference and load variations. They show the quick convergence and the robustness of the proposed observer against strong disturbance of the load variation.

5.3 SUMMARY

To estimate the state vector and avoid measurement complexities, an observer design for high switching frequency DC/DC converters is very useful. This chapter proposes two kinds of observers. A nonlinear sliding mode observer is introduced to estimate all the states and

load variation from the output voltage. The simulation results prove the effectiveness of the designed observer. Due to the application of the observer in FPGA implementation, a discrete-time observer is more appropriate in our case. Thus a simple and very efficient Kalman observer is proposed. An extended Kalman observer is developed where the load variation is considered as the observed variable. Simulation results show that the proposed extended Kalman observer provides high performance for reference voltage variations and a wide load changes. With the help of the extended Kalman observer, more flexible control methods can be realized. Thus the extended Kalman observer will be used for FPGA implementation rather than the sliding mode observer. The implementation of the proposed extended Kalman observer in FPGA will be detailed in the following chapters.

CHAPTER 6 HIGH-RESOLUTION DPWM DESIGN

In order to reduce the size of passive components and to obtain system miniaturization, the switching frequency must be increased. The computation speed and the capacity to process complex algorithms are the main concerns for the digital processor in practical implementation. Compared to traditional digital processors such as dSPACE and microcontroller unit (MCU), FPGA offers very fast computation speed and more choice in word length for algorithm calculation. Moreover, the design is described at the functional level using a hardware description language (HDL) which provides a better flexibility for programming. The design can then be easily moved to a different process, integrated with other digital systems, or modified to meet a new set of specifications. However, ADC and DAC or Digital Pulse-Width Modular (DPWM) resources are not available in FPGA. The control quality depends much more on the conversion resolution. One major challenge in digital-control implementation in FPGA is how to design high resolution analog-to-digital (A/D) converter and DPWM with reasonable frequency and limited size.

Recently, several solutions have been proposed for high-resolution low-power DPWM architecture. The delay-line [SAM04], segmented delay-line [TWN05, TPPN07], ring-oscillator [WXMS99, PXS03] can be seen as the same type of DPWM structures that use the logic delay cell to get a delay time. With the delay-line based structure, the DPWM minimal time slots are generated by the propagation delay of a pulse through delay cells, and then selected by multiplexers to produce the PWM output.

Unlike those hardware DPWMs which rely on high-power consuming counters and expensive CMOS technologies for tight delay cells, digital dithering [PS03] and Delta-Sigma (Δ - Σ) [ST05, JM97] are practical soft methods to increase effective resolution of DPWM. They both have been proved two effective methods to reduce hardware resource of DPWM and to increase DPWM resolution in a soft way without increasing area and power consumption. Dithering increases the resolution by averaging several adjacent switching periods' duty cycle values [PME01]; hence, a large-magnitude output ripple results although the limit-cycle oscillation could be reduced [PS01]. The Δ - Σ DPWM which is realized using

noise-shaping technology [JM97, ST05] can be implemented with simple low-power hardware.

Our main goal is to present an architecture of low-power digital PWM controller for SEPIC that can operate at programmable constant high switching frequencies. Hybrid DPWM [PPZM03, SAM04, DAC00] is a trade-off between the high clock frequency requirements of the standard counter-based DPWM [GH96], and other hardware or software methods requirements.

After a discussion of resolution requirements and a review of existing DPWM, we propose two kinds of hybrid DPWM architectures which adopt hardware and software method respectively. A hybrid DPWM which combines delay-line and counter comparator is presented. Finally, we propose a hybrid 11-bit DPWM Δ - Σ modulator that combines a Digital Clock Manager (DCM) phase-shift block with a counter comparator. For the Δ - Σ modulator, a Mash Δ - Σ DPWM which combines the advantage of first-order Δ - Σ modulator and second-order Δ - Σ modulator is issued.

6.1 RESOLUTION REQUIREMENTS OF A/D CONVERTER AND DPWM

An analog control system provides an output voltage regulation by comparing the output voltage to a reference voltage and amplifying the difference. In principle, the output voltage can be adjusted to any arbitrary value, which is limited by loop gain and noise levels. However, because of the quantization elements which exist in the ADC and DPWM, the digital controller has a finite set of discrete levels in nature. Thus, the quantization of the A/D converter and the DPWM is critical to both static and dynamic performances of power converters.

6.1.1 A/D Converter Resolution Requirements

The need for a certain amount of accuracy in representing analog signals by their digital equivalents governs the ADC resolution. To satisfy specifications for the output voltage regulation, resolution of the A/D converter should be high enough so that the generated error is lower than the allowed variation of the output voltage.

Therefore, the resolution of the ADC has to be less than the allowed maximum scaled output voltage variation ΔV ,

$$\frac{\Delta V}{V_s} \cdot H \geq \frac{V_{ADCmax}}{2^{N_{ADC}} \cdot V_s}, \quad H = \frac{V_{ADCref}}{V_s} \quad (6.1)$$

where H is the scaled factor of voltage sensor, V_{ADCref} , V_s and V_{ADCmax} are the reference voltage for the ADC, output voltage and full-range voltage of the ADC respectively, and N_{ADC} is the bit number of ADC. Then, the required A/D bit number with respect to a chosen reference voltage level can be obtained by rearranging (6.1):

$$N_{\text{ADC}} \geq \text{int} \left[\log_2 \left(\frac{V_{\text{ADCmax}}}{V_{\text{ADCref}}} \cdot \frac{V_s}{\Delta V} \right) \right] \quad (6.2)$$

where function $\text{int}[\]$ takes the upper rounded integer value of the product.

Equation (6.2) indicates the minimum number of bits of the ADC to meet the output voltage regulation requirement of power converters. For example, if 1% variation of the output voltage is allowed, and if V_{ADCref} is at least 50% of the A/D full-range voltage, then a minimum 7-bit resolution will be required for the ADC.

The higher the ADC resolution, the faster the system response, as errors in the loop can have higher resolution and can be quickly corrected. Another important criterion for the choice of ADC is its conversion time and power consumption from time of measurement at the input to the availability of the digital word at its output register.

As mentioned in chapter 1, in this dissertation, we are interested particularly in the design of DPWM since ADC is only implemented for IC design. In the test platform described in chapter 7, a 10-bit A/D component ADS900 has been used for analog-to-digital conversion out of FPGA part.

6.1.2 Resolution Requirement of DPWM

In the system where a power converter and a digital controller form a feedback loop, the digital pulse-width modulator serves the purpose of a D/A converter.

The discrete set of duty ratios and ultimately the discrete set of achievable output voltages depend on the DPWM resolution. In order to ensure good steady-state behaviour in controlled variable, it is necessary that the resolution of the DPWM output be higher than the resolution of the ADC. If the DPWM resolution is not sufficiently high, an undesirable low frequency oscillation called limit-cycle oscillation, can occur [PS01, PPAM07, ZP07].

Fig. 6-1 shows the output voltage v_s behaviour with DPWM resolution lower and higher than the ADC resolution respectively. It is essential that the resolution of the DPWM is high enough to avoid the limit-cycle oscillation phenomenon.

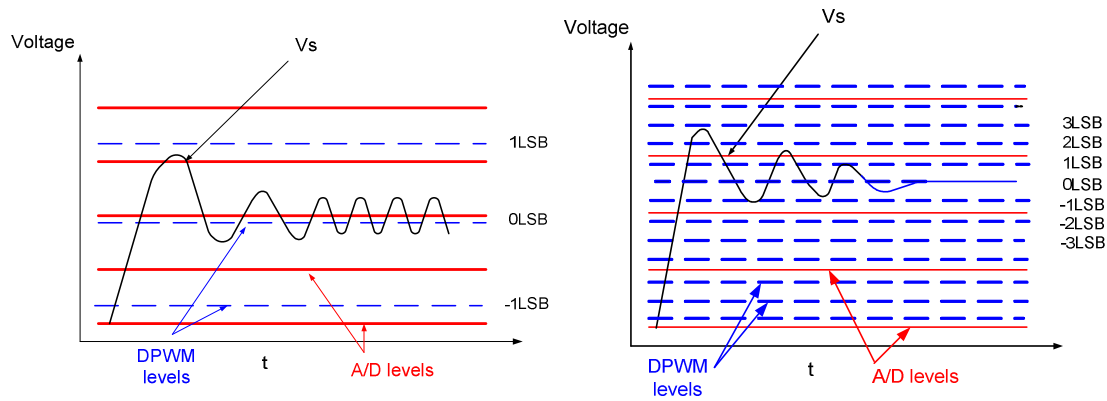


Fig. 6-1 Behavior of output voltage v_s (a) DPWM resolution lower than the ADC resolution (b) DPWM resolution higher than the ADC resolution

A necessary condition to avoid the limit-cycle oscillation is that the output voltage increment ΔV_s that corresponds to one least significant bit (LSB) change in the duty cycle ratio ΔD , must be smaller than the analog equivalent of the LSB of the A/D converter [PS01].

For SEPIC used as a voltage regulator,

$$\Delta V_s = V_e \cdot \frac{\Delta D}{1 - \Delta D} = V_e \frac{1/2^{N_{DPWM}}}{1 - 1/2^{N_{DPWM}}} = \frac{V_e}{2^{N_{DPWM}} - 1} \leq \frac{V_{ADCmax}}{2^{N_{ADC}}} \cdot \frac{V_s}{V_{ADCref}} \quad (6.3)$$

Where V_e is the input voltage, N_{DPWM} is the bit number of DPWM. Thus the minimum bit number of DPWM is given as:

$$N_{DPWM} \geq \text{int} \left[\log_2 \left(\frac{1-D}{D} \frac{V_{ADCref}}{V_{ADCmax}} \cdot 2^{N_{ADC}} + 1 \right) \right] \quad (6.4)$$

Where $D = \frac{V_s}{V_s + V_e}$ is the duty ratio in steady-state.

From chapter2, we know that the limitation boundary of the duty cycle for SEPIC in nominal condition is between around 0.3 and 0.75 working in CCM. In order to avoid limit cycle oscillation, it can be seen from equation (6.4) that the number of bits required for the DPWM generator, N_{DPWM} should be at least larger by one bit than the ADC resolution in steady-state, thus N_{DPWM} is given by:

$$N_{DPWM} \geq N_{ADC} + 1 \quad (6.5)$$

Indeed, if the DPWM resolution is lower than the ADC resolution, there is no DPWM level that maps into the ADC binary code corresponding to the reference voltage. In steady state, the controller will be attempting to drive to the 0 LSB, however due to the lack of a DPWM level there, it will alternate between the DPWM levels around the 0 LSB. If the desired output voltage value doesn't belong to one of these discrete values, the feedback controller will switch among two or more discrete values of the duty ratio. This will result in non-

equilibrium behaviour, such as steady-state limit cycling [PME01]. Therefore, it is very critical to achieve a high resolution in DPWM generation in digital control of DC/DC converters.

6.2 CHOICE OF DPWM TECHNIQUES

For a N_{DPWM} -bit DPWM, the relationship between system clock f_{clk} and switching frequency f_{sw} is shown in Fig. 6-2 and can be written as:

$$f_{\text{clk}} = 2^{N_{\text{DPWM}}} \cdot f_{\text{sw}} \quad (6.6)$$

and the DPWM resolution ΔD is determined by

$$\Delta D = \frac{f_s}{f_{\text{clk}}} = \frac{1}{2^{N_{\text{DPWM}}}} \quad (6.7)$$

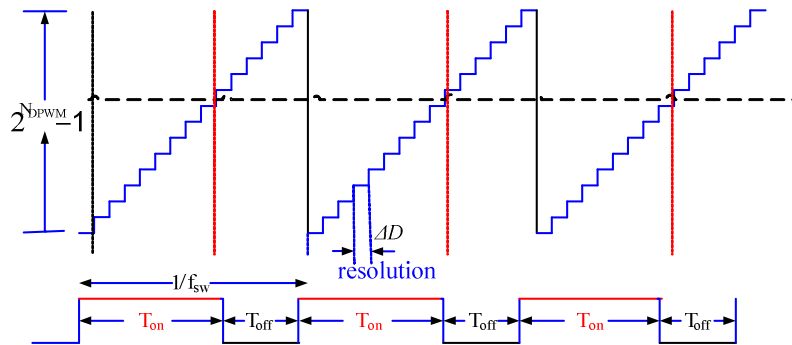


Fig. 6-2 Relationship between DPWM and switching frequency

For instance, considering the SEPIC working at switching frequency of 500kHz as introduced previously, a 10-bit ADC is needed, and then DPWM should be at least 11-bit according to (6.5). In that case a clock frequency larger than 1GHz would be needed. It becomes too high to be practical for FPGA implementation. For ASIC implementation, the system clock reflects the power consumption of the digital control system. Higher frequency would reduce the converter efficiency.

6.2.1 Counter-Comparator DPWM

A simple method to achieve high resolution in DPWM is to use a fast-clocked counter-comparator scheme [LS05, SAM04, DAC00, HCGC07]. Fig. 6-3 shows the structure of fast counter-comparator scheme. This implementation uses a cycling counter and a comparator, setting a set-reset (SR) latch high when the counter value is zero and low when the counter reaches the chosen duty-cycle value, $d[k-1:0]$. In this scheme a system counter (k bits) is used to generate the fixed sampling and the resolution of DPWM signals hereby is $1/2^k$. By

comparing counter value and the numerical duty cycle value (from control law), the switch of the converter is turned on/off. This scheme has high linearity of the digital-to-time-domain conversion and is very simple and easy to implement.

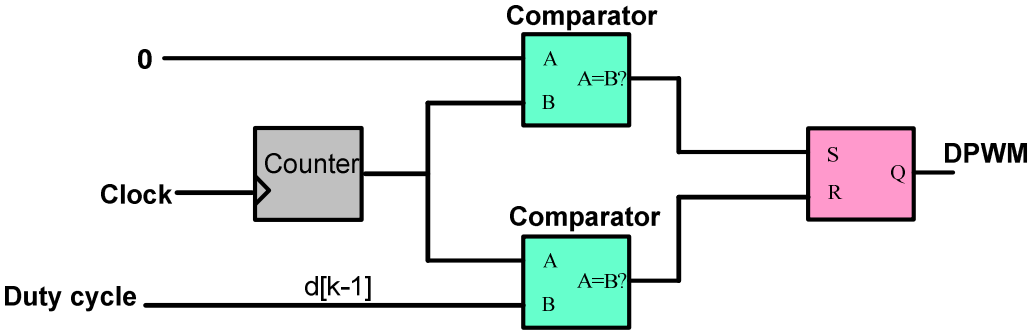


Fig. 6-3 k-1-bit counter-comparator block

However, in this circuit, a very high clock frequency ($2^k f_{sw}$) and related fast logic circuits are needed to achieve sufficient DPWM resolution at high switching frequency. As abovementioned, for a typical 11-bit resolution at a switching frequency of 500kHz, a clock frequency exceeding 1GHz is required, which is impractical in most applications and would also consume excessive power. The drawback of counter-based PWM exists evidently that the power consumption is very high when the DPWM requires a high resolution.

6.2.2 Segmented DCM Phase-shift Technique

DCM functionality block is available in most digital FPGA devices. It can offer multi asynchronous clocks with low skew phase-shift. For instance as shown in Fig. 6-4, the DCM divides the incoming clock f_{clk} (50% ratio) into four equal clocks clk_0 , clk_90 , clk_180 and clk_270 respectively. Then the four-phase-shifted clocks can act as an equivalent $2^2 f_{clk}$ clock with a 4:1 multiplexer. Thus the clock for the DCM architecture can be reduced by 2^2 times for a fixed-resolution DPWM.

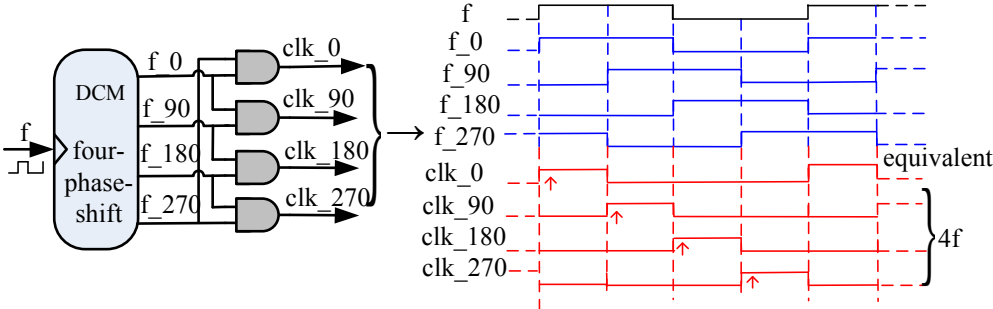


Fig. 6-4 DCM four-phase shift scheme

Based on the advantage of DCM phase-shift module, a segmented DCM phase-shift architecture including two 2-bit DCM phase-shift modules in series is introduced in [BAHIB08]. The similar segmented DCM architecture is also employed as a 4-bit DPWM block. The block diagram of the 4-bit segmented DCM phase-shift architecture is shown in Fig. 6-5, where the input clock f_{clk} , propagates in zero delay through the first DCM block, DCM-I in this case, and the first phase shifted versions, PX0, PX90, PX180 and PX270, are generated. The clock f_{DCM} , four times the incoming clock f_{clk} , is operated at the second DCM block, DCM-II, and further phase shifted signals of the clock are produced, PY0, PY90, PY180 and PY270.

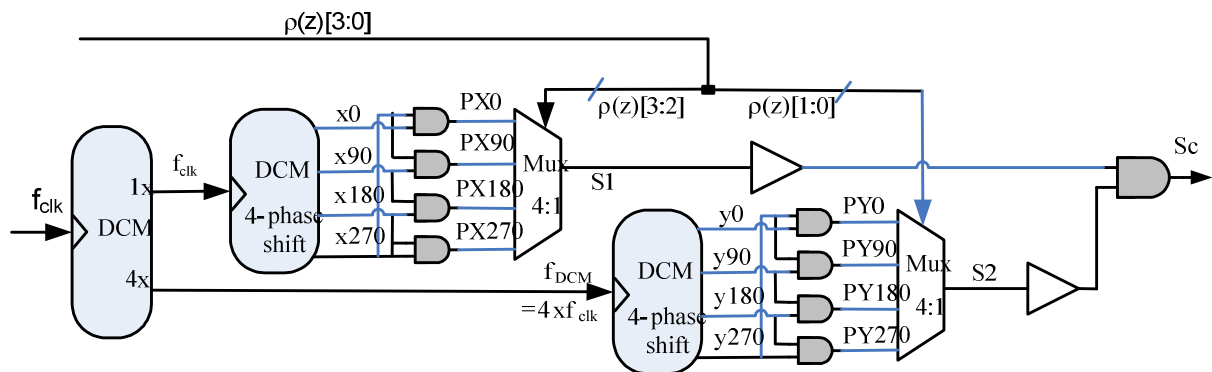


Fig 6-5 A diagram block of 4-bit segmented DCM phase-shift

The most attractive merit of this segmented DCM phase-shift architecture is that the final output signal S_c has 2^4 clock possibilities during each of f_{clk} cycle, where S_1 has 2^2 possibilities of "coarse" phase-shift and S_2 has 2^2 possibilities of "fine" phase-shift. Thus this segmented DCM block can either increase by 4-bit DPWM resolution (for fixed f_{sw}) or increase the switching frequency by 2^4 times (for fixed N_{DPWM}). As observed from Fig. 6-4, the resolution is now increased by 16 times without the need of operating the whole system at 16 times f_{clk} .

6.2.3 Delay-Line DPWM

An alternative method to generate DPWM signal with high resolution at low power is to employ a delay-line structure [SAM04, WXMS99, DAC00] that takes advantage of the latency of common circuit elements (e.g. logic gates, flip-flops, etc.) by connecting them in series, as shown in Fig. 6-6. With the delay-line based structure, the DPWM minimal time slots are generated by the propagation delay through delay cells, and then selected by MUX to produce PWM output. A pulse from the reference clock at the switching frequency f_{sw} will take a finite time to pass through each delay components, so by "tapping" their individual

outputs to the inputs of a multiplexer it is possible to choose an amount by which to delay the signal. A pulse-width modulated output may be generated by setting a SR-latch high when a pulse enters the delay-line and low again when the pulse appears at the multiplexer output, having been delayed by an amount determined by the selected tap. The total delay of the delay line is adjusted to match the reference clock period.

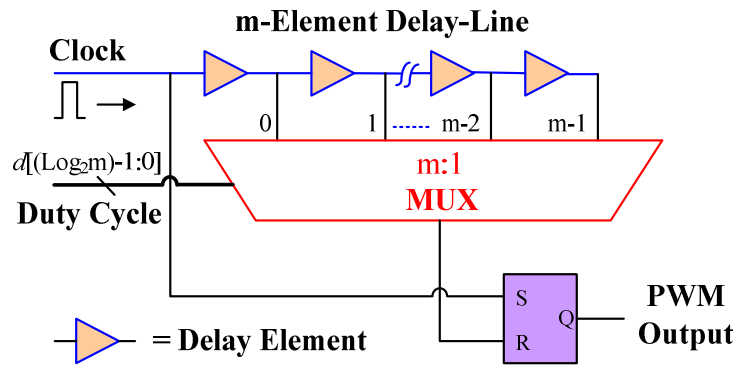


Fig. 6-6 Delay-Line DPWM

The power loss of a delay-line DPWM is significantly reduced compared to the fast counter-comparator scheme as the fast clock is replaced by a delay line, which operates at the switching frequency of the converter. However, the disadvantage of this method is that the size of the multiplexer increases exponentially 2^m with a resolution of m -bit. For 11-bit resolution this requires at least 2048 (2^{11}) delay stages and, consequently a very large silicon area. Besides when the switching frequency f_{sw} is high, this kind of DPWM may be difficult to implement.

6.2.4 Hybrid Delay-Line DPWM

In order to reduce the silicon area taken by large number of multiplexers and to improve the linearity of digital-to-time-domain conversion of the delay-line DPWM, a combination of the fast counter-comparator and delay-line architecture is proposed [TM06, HYM06, YTM06, PPZM03], which makes a trade-off between the high frequency and the chip area. The so-called hybrid delay-line DPWM requires a relatively low frequency counter clock with a short delay-line and, thus, a reduced-area multiplexer. Fig. 6-7 shows an example of a hybrid DPWM with an open loop delay line. This is a 5-bit DPWM with 3-bit counter and 2-bit delay line. The counter provides the most significant bit (MSB) portion of the duty cycle and the delay line provides the least significant bit (LSB) portion. Fig. 6-8 shows a typical timing diagram for the DPWM. The required number of delay cells depends on the number of bits provided by the delay line.

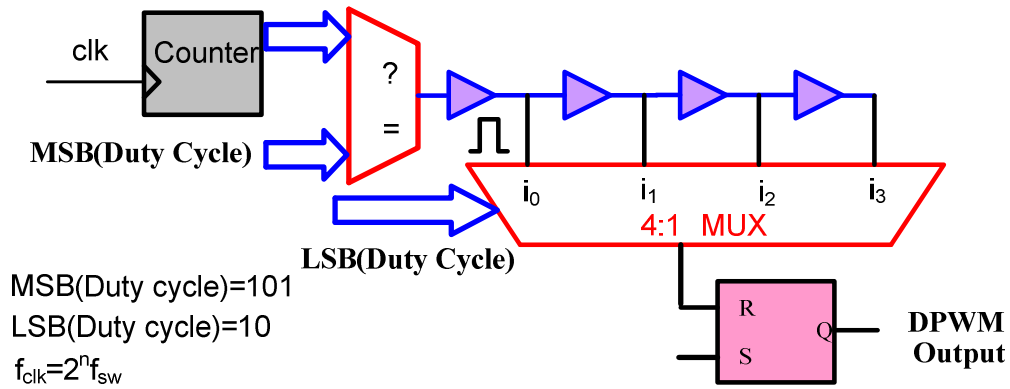


Fig. 6-7 Hybrid DPWM with external clock

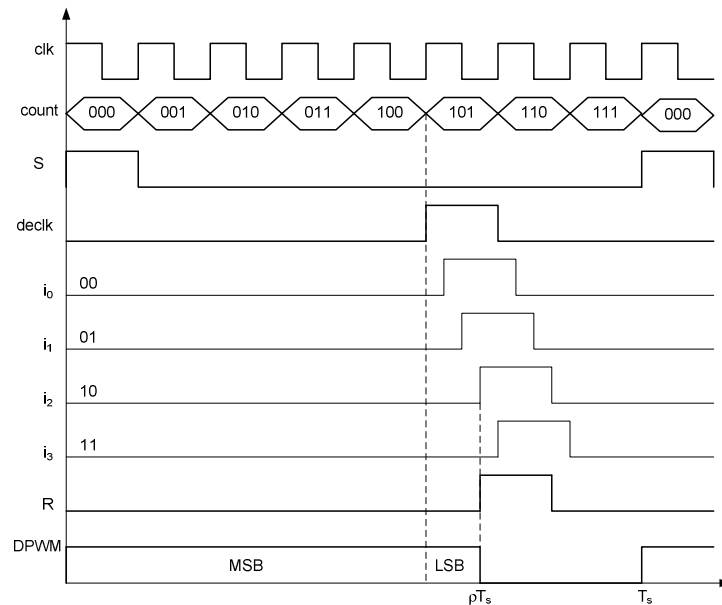


Fig. 6-8 Timing diagram of the 5-bit hybrid DPWM

The counter counts at each clock period of the input, clk . The output DPWM is set at the zero value of the counter (count = “000”). The output of the counter is compared with the 3 most significant bits of the input duty cycle target, MSB(duty cycle). The result is the signal $declk$. The width of $declk$ is equivalent to one clock period of the input clk signal. The signal $declk$ is then propagated through the delay line. The output of each delay cell is connected to a 4:1 multiplexer. The propagated signals, i_0 - i_3 , which are the output of the delay cells are shown in Fig. 6-8. The selection of the multiplexer output is made by observing the least significant portion of the input duty cycle target, LSB(duty cycle). The appropriate input of the multiplexer is then connected to the RS latch input R. In the example shown in Fig. 6-7 and Fig. 6-8, duty cycle = 10110 and, therefore, i_2 is connected to R (LSB(duty cycle) = 10). The signal R resets DPWM. Since a smaller counter is used in the hybrid DPWM, the

required input clock frequency is lower as compared to the counter-based DPWM with the same resolution.

In order to verify the feasibility of the hybrid delay-line DPWM for our application, an 11-bit DPWM composed of 7-bit counter and 4-bit delay-line is designed. The implementation is verified in post-placed-and-route using Xilinx ISE9.2 tool. The time-simulation waveforms of the complete 11-bit hybrid DPWM are illustrated in Fig. 6-9 and Fig. 6-10 with an example duty cycle [100101011] which is divided into LSB[1011] for the delay tapping, and MSB[1001010] for counter-comparator.

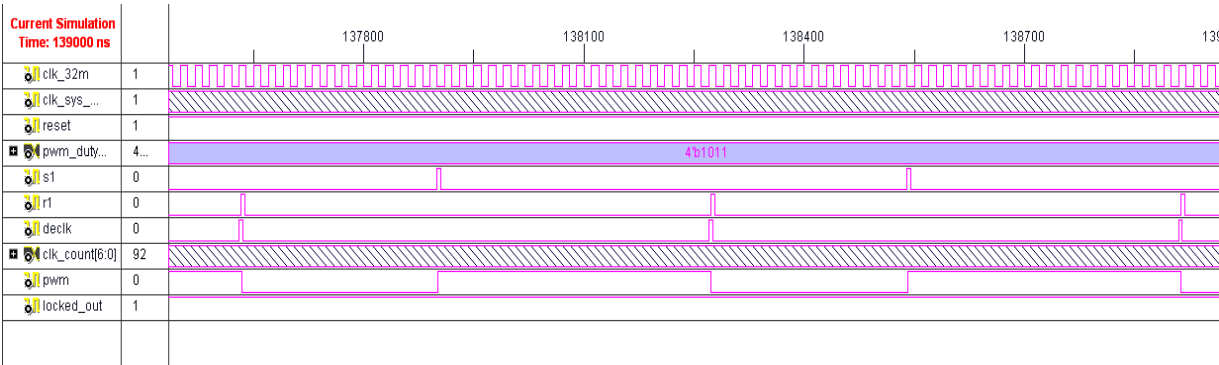


Fig. 6-9 11-bit hybrid DPWM timing-simulation waveforms

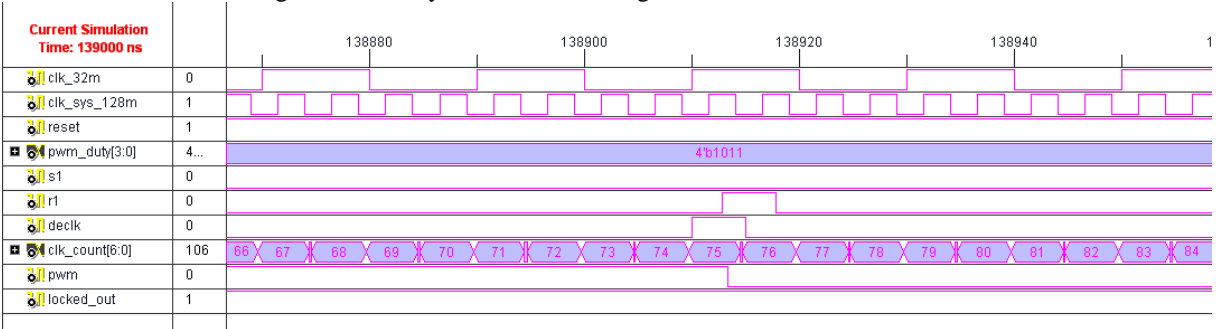


Fig. 6-10 11-bit hybrid DPWM timing-simulation waveforms (within one-duty cycle)

Compared to the 11-bit hybrid delay-line DPWM, the number of delay stages can be reduced from 2^{11} to 2^4 with a counter-comparator at frequency $2^7 f_{sw}$. Thus for an 11-bit resolution at a switching frequency of 500kHz, a clock frequency of 64MHz is sufficient, which is practical in our application.

Although this kind of DPWM can achieve much higher resolution than the counter-based DPWM, however it requires still a large silicon area than the fast counter-comparator one. However, when the switching frequency f_{sw} is higher, the delay cell may be difficult to generate. For instance, a 10MHz Ring-Oscillator DPWM having 10-bit resolution requires cell whose propagation time is less than 100ps. Such small time-delay can be achieved only

with the most advanced and expensive IC fabrication technologies (0.12- μm CMOS or smaller). Moreover, the linearity of digital-to-time-domain conversion depends on the delay cell. The accuracy of delay propagation is sensitive to the various effects such as temperature, manufacture process, voltage supply V_{DD} , etc. Hence, we propose another hybrid DPWM solution in next section.

6.3 DESIGN OF AN 11-BIT HYBRID DPWM

The idea of the proposed hybrid DPWM architecture is to take the advantage of the combination of hardware method and soft method to alleviate the requirement for high frequency clock and reduce power consumption. Delta-Sigma (Δ - Σ) modulator which is based on the well known noise-shaping technology is a practical soft method to increase the effective resolution of DPWM. As an 11-bit DPWM is required, we propose an 11-bit hybrid DPWM module composed of a 4-bit MASH Δ - Σ modulator, a 4-bit segmented DCM phase-shift and a 3-bit counter-comparator.

6.3.1 Design of Δ - Σ DPWM

A. Δ - Σ Modulator application in DPWM

Δ - Σ has been widely used in analog-to-digital and digital-to-analog conversion. It is based on the well-known noise-shaping concept which can be fabricated in low-cost CMOS technologies [ST05, JM97]. For a first order Δ - Σ , the modulator can be transformed into a detailed linear model in z-domain as shown in Fig. 6-11, where $E(z)$ is noise.

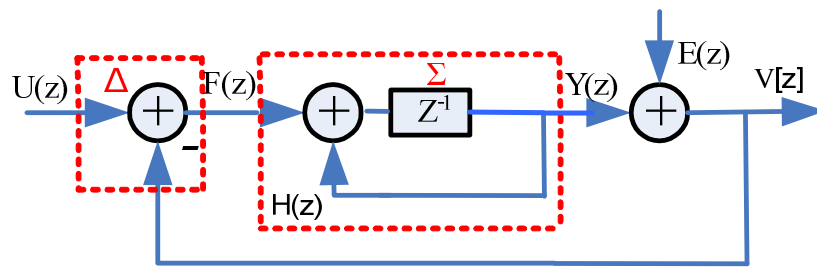


Fig. 6-11 A z-domain block of the first-order Δ - Σ modulator

From the diagram, the transfer function of the inner loop can be obtained:

$$H(z) = \frac{Y(z)}{F(z)} = \frac{z^{-1}}{1 - z^{-1}} \quad (6.8)$$

Thus the output $V[z]$ can be expressed as:

$$V(z) = \frac{H(z)}{1+H(z)}U(z) + \frac{1}{1+H(z)}E(z) \quad (6.9)$$

Equation (6.9) can be rewritten in the digital signal process form

$$V(z) = STF(z) \cdot U(z) + NTF(z) \cdot E(z) \quad (6.10)$$

where STF is the signal transfer function, and NTF is the noise transfer function with $NTF(z) = (1-z^{-1})$. In steady-state, when the Δ - Σ loop has infinite gain at zero frequency, i.e., $z \approx 1$ and consequently $\|NTF(z)\| \ll 1$, it suppresses the quantization noise at and near dc component. Therefore the Δ - Σ modulator can dramatically eliminate the quantization noise and then the input signal can be shaped in a satisfying manner,

$$V(z) \rightarrow U(z) \quad (6.11)$$

For the DPWM application in Δ - Σ digital signal process, the loop architecture function is similar to that of the noise-shaping loop in application of analog-to-digital and digital-to-analogue conversion. It consists of reducing the resolution of the large-bit input signal to a few bit value without significant quantization error-bit in the process. Δ - Σ DPWM consists of a low-resolution low-power DPWM capable of operating at high switching frequencies and a Δ - Σ modulator, which improves the effective resolution of the core DPWM. An architecture configuration for Δ - Σ DPWM is illustrated in Fig. 6-12. An example is given where the effective resolution of a 6-bit DPWM core is improved to 10 bit. It consists of a high-frequency low-resolution DPWM, a delay block, and two adders. For the case shown in Fig. 6-12, the low-resolution DPWM is a 6-bit value that is varied over several switching periods to result in an average value that offers a high-resolution (high effective resolution). The value of the duty ratio is set by the high-resolution digital control reference $\rho[z]$ and the averaging process is performed by the switching converter itself. The fast convergence toward the high-resolution value is provided with the internal loop of the Δ - Σ DPWM.

The modulator itself consists of an adder, a truncator and delay blocks forming two feedback loops [KR05, EM00]. The inner loop can be seen as a forward-Euler integrator, with the transfer function:

$$H(z) = \frac{z^{-1}}{1-z^{-1}} \quad (6.12)$$

$H(z)$ forces the average value of $F[z]$, the difference between high-resolution $\rho[z]$ and the low-resolution value of 6-bit DPWM $\rho_{LR}[z]$, to be zero and effectively increases the resolution of the DPWM.

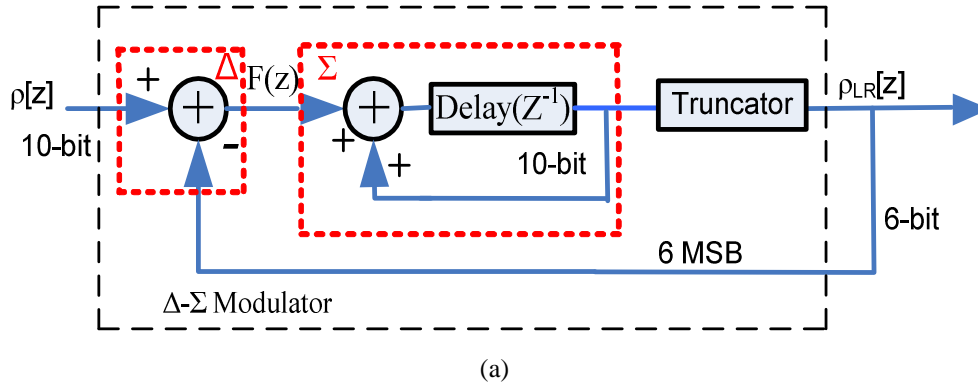


Fig. 6-12 First-order Δ - Σ modulator for DPWM

In this case, z-transform of $\rho_{LR}[z]$ becomes

$$\rho_{LR}(z) = \frac{H(z)}{1+H(z)}\rho(z) + \frac{1}{1+H(z)}E(z) \quad (6.13)$$

This equation shows how the transfer function $H(z)$ influences the truncated signal. When $H(z)$ is large in magnitude, i.e., $\|H\| \gg 1$, the high-resolution input is almost unchanged, the quantization error is suppressed, consequently, $\rho_{LR}[z]$ becomes approximately equal to the high resolution input $\rho(z)$.

Over several switching cycles, the Δ - Σ modulator varies $\rho_{LR}[z]$, the low-resolution input of the core DPWM, to achieve a high-resolution average duty ratio value, equal to the 10-bit input reference. When connected to a switching converter power stage, no additional hardware is needed for averaging. It is naturally performed with the filtering components of the power stage.

B. Second-order Δ - Σ modulator

Several publications [SSM95, GS94, KR05, LQZYC01, LWP05] present DPWM architectures based on various modifications of the first-order Δ - Σ concept. Although the first-order Δ - Σ DPWM has the advantages of simplicity, robustness, stability and simple realization, it still requires a core DPWM with relatively high resolution, and the noise-shaping performance of this DPWM is still limited since it has the potential problems of low-frequency tones and slow convergence [LRP07, ST05, PWG07]. As a result, the dynamic response of Δ - Σ DPWM controllers is often compromised. Additionally, in most of the realizations, the bandwidth of the voltage control loop is significantly reduced.

The problems of slow convergence towards high-resolution input and low-frequency tones existing in first-order-modulators can be solved with second-order-architectures. It has been shown that second-order Δ - Σ architectures suppress low-frequency tones and offers faster

convergences [LRP07]. We show a second-order DPWM architecture that allows operation at programmable constant switching frequencies and also minimizes the abovementioned tone-related problems of first-order architectures using a low-resolution low-power core DPWM to achieve a high switching frequency. The design of a second-order DPWM is shown in Fig. 6-13.

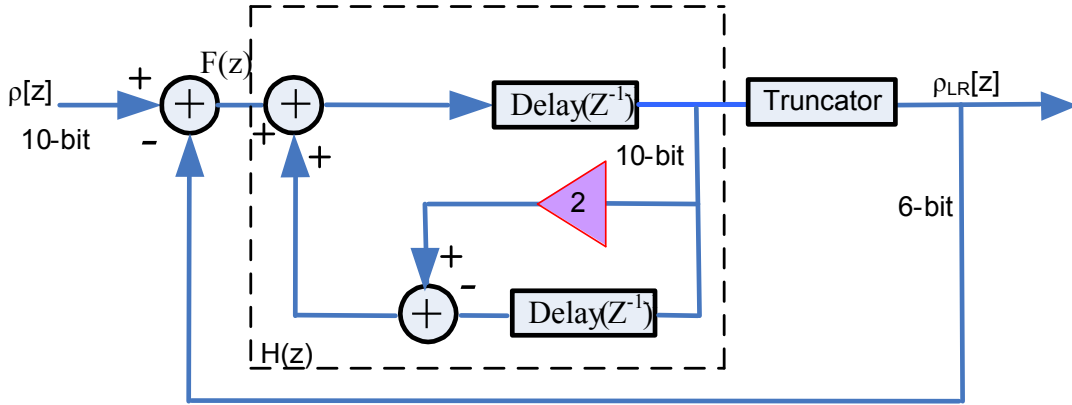


Fig. 6-13 Block diagram of a second-order Δ - Σ modulator

The system in Fig. 6-13 is a 10-bit second-order Δ - Σ with a 6-bit core DPWM. Compared to the previously first order implementation the main difference is in the transfer function $H(z)$ [Fig. 6-12(b)]. In that case, two delay blocks, an adder, and multiplier form the discrete-time transfer function

$$H(z) = \frac{z^{-1}}{(1-z^{-1})^2} \quad (6.14)$$

The rate change of core DPWM, $\rho_{LR}(z)$, described above is much faster than that of the first-order. Moreover, the changes in the core DPWM are more frequent and larger in amplitude. Consequently, higher frequency tones are produced and faster averaging process is achieved. Even though the variations of the duty ratio are bigger, their effect on the switching converter output voltage is smaller.

C. Design of a MASH Δ - Σ DPWM

Based on the useful signal-stage Δ - Σ modulator, a cascade modulator also called Multi-stage-noise-Shaping (MASH) modulator which possesses the function of a second-order Δ - Σ modulator and the stability features of a first-order Δ - Σ modulator is adopted. It has been proven that the MASH modulator has the advantage to ease the stability problem evaluation in high-order Δ - Σ architecture [GLAG09]. The basic concept of the MASH (two-stage) Δ - Σ is illustrated in Fig. 6-14.

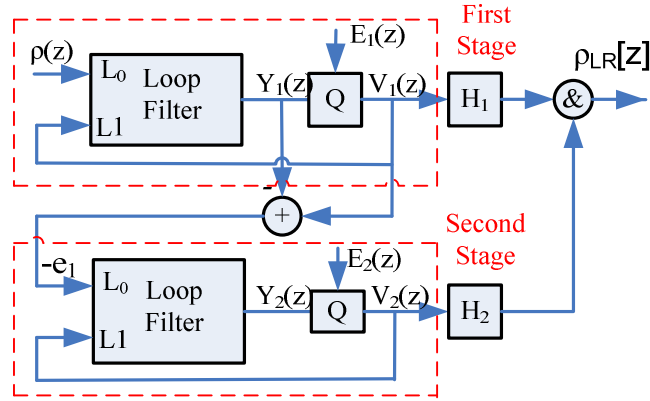


Fig. 6-14 A cascade structure of two-stage MASH Δ - Σ modulator

Where Loop Filter is a noise-shaping modulator that generally is a delay or integrator block, Q is the quantizer, $E_1(z)$, $E_2(z)$ are the noises and $V_1(z)$, $V_2(z)$ are the output signals.

The output signal of the first-stage is given by:

$$V_1(z) = STF_1(z) \cdot \rho(z) + NTF_1(z) \cdot E_1(z) \quad (6.15)$$

Where $STF_1(z)$ and $NTF_1(z)$ are the signal transfer function and the noise transfer function of the first-stage loop respectively. The output signal of the second-stage is given by:

$$V_2(z) = STF_2(z) \cdot E_1(z) + NTF_2(z) \cdot E_2(z) \quad (6.16)$$

Where $STF_2(z)$ and $NTF_2(z)$ are the signal transfer function and the noise transfer function of the second-stage loop respectively. The digital filter stages H_1 and H_2 at the output of the two modulator loops are designed such that the first-stage error $E_1(z)$ is cancelled whatever the output $\rho_{LR}(z)$ of the system, setting $H_1(z) \cdot NTF_1 - H_2(z) \cdot STF_2 = 0$. Usually the choice for H_1 and H_2 is $H_1(z) = k \cdot STF_2$ and $H_2(z) = k \cdot NTF_1$, where k is a constant chosen to give unity signal gain. For $k = 1$, the overall output signal is then given by:

$$\begin{aligned} \rho_{LR}(z) &= H_1(z) \cdot V_1(z) + H_2(z) \cdot V_2(z) \\ &= STF_1 \cdot STF_2 \cdot \rho(z) + NTF_1 \cdot NTF_2 \cdot E_2(z) \end{aligned} \quad (6.17)$$

In a typical case, both stages of the MASH modulator may contain a first-order loop or a second-order loop.

Compared to the single-stage Δ - Σ modulator, the MASH structure extracts the first-stage error $e_1(n)$ without any subtraction, and enters it into the second stage with low distortion. Besides, the remaining error in the output signal $V_1(z)$ is the shaped quantization error $e_2(n)$ of the second stage, operating with an input error $e_1(n)$ which is itself like noise. Supposing the internal loop is first-order, then

$$STF_1 = STF_2 = 1, NTF_1 = NTF_2 = (1 - z^{-1}) \quad (6.18)$$

Setting

$$H_1(z) = STF_2 = 1, H_2(z) = NTF_1 = (1 - z^{-1}) \quad (6.19)$$

Then the output is

$$\rho_{LR}(z) = \rho(z) + (1 - z^{-1})^2 \cdot E_2(z) \quad (6.20)$$

Thus this MASH Δ - Σ modulator has the noise-shaping performance of a second-order loop but the stability issue is that of a first-order loop.

A MASH Δ - Σ modulator which has two internal first-order loops is employed for the proposed DPWM architecture. In practice, to minimize size and power consumption, the modulator processes only the truncation error. From a system perspective, the DPWM behaves like DAC (digital to analog converter), and taking into account the implementation on a FPGA platform, the error feedback structure for DAC is used here for DPWM. The diagram for MASH Δ - Σ DPWM is shown in Fig. 6-15. The 11-bit DPWM duty value from control algorithm is sent to the first-stage loop, and then 5-MSB is as the output and 6-LSB for error-feedback e_1 . After the second-stage loop, 2-MSB are delivered to output and 4-LSB are distributed for error-feedback e_2 . Finally the 7-bit combination PWM signals (5-MSB and 2-LSB) are sent to the hardware core DPWM (DLL phase-shift and counter comparator blocks).

This structure is known as error-feedback [ST05, JM97] and performs the same function as the above described second-order system utilizing much simpler digital hardware.

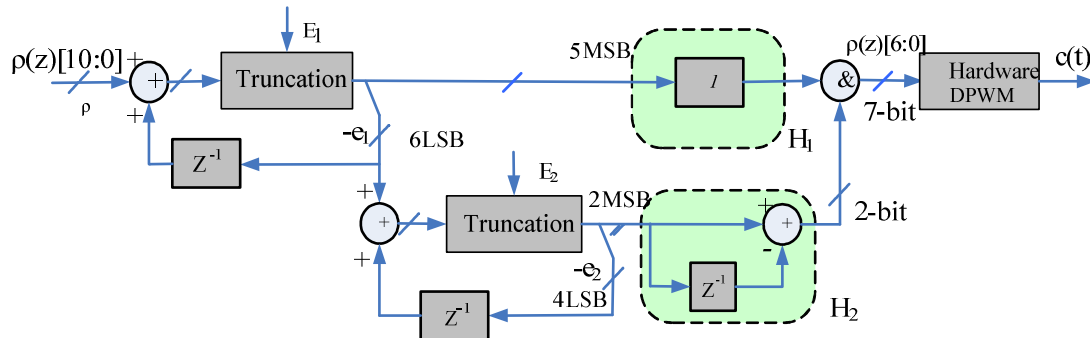


Fig. 6-15 An error-feedback MASH DPWM based on two-stage Δ - Σ modulator

In this case, three adders are used, and with a truncator, two LSBs and five MSBs are generated, respectively. In addition, each delay block is realized with D flip-flops. The modulator is clocked at the switching frequency by a signal created with the core DPWM.

6.3.4 Operation of the Hybrid Δ - Σ DPWM Scheme

The 11-bit hybrid DPWM is implemented by a combination of three blocks as described above: 3-bit counter-comparator, 4-bit segmented DCM phase-shift and 4-bit MASH Δ - Σ modulator. The completed hybrid DPWM architecture is represented in Fig. 6-16. The operation of the hybrid 11-bit DPWM can be described as follows: initially, an 11-bit duty cycle is generated by the digital control law, then with the MASH Δ - Σ modulator, the 4-LSB is realised within it, and a 7-MSB duty value is obtained. Among the 7-bit value, the LSB $\rho[3:0]$ are assigned to the 4-bit segmented DCM phase-shift block, the MSB $\rho[6:4]$ are delivered to the 3-bit counter-comparator block, finally, the switch of the converter is turned on/off via an R-S latch.

The DPWM counter clock is $f_{clk} = 2^3 \cdot f_{sw}$ and the clock frequency for DCM phase-shift is $f_{DCM} = 2^2 \cdot f_{clk} = 2^5 f_{sw}$. For example, when operating at switching frequency $f_{sw} = 500\text{kHz}$, the f_{clk} is merely 4MHz and f_{DCM} is 16MHz, which dramatically alleviates the clock requirement and allows the operation with low power consumption.

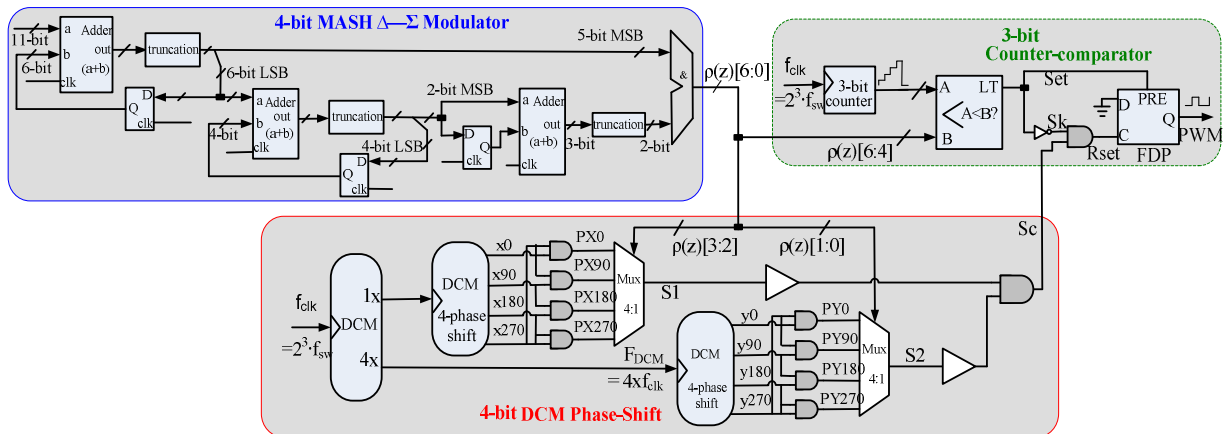


Fig. 6-16 Proposed 11-bit FPGA-based Hybrid DPWM: 4-bit MASH Δ - Σ modulator, 4-bit segmented DCM phase-shift and 3-bit counter-comparator

The timing-simulation for the 11-bit FPGA-based DPWM is shown in Fig. 6-17 with an example of ratio of 935, which is equal to $D[10:0] = "01110100111"$. As it is shown, the multi-bit Δ - Σ DPWM can effectively achieve 11-bit resolution at high-frequency through a 7-bit hardware Core DPWM.

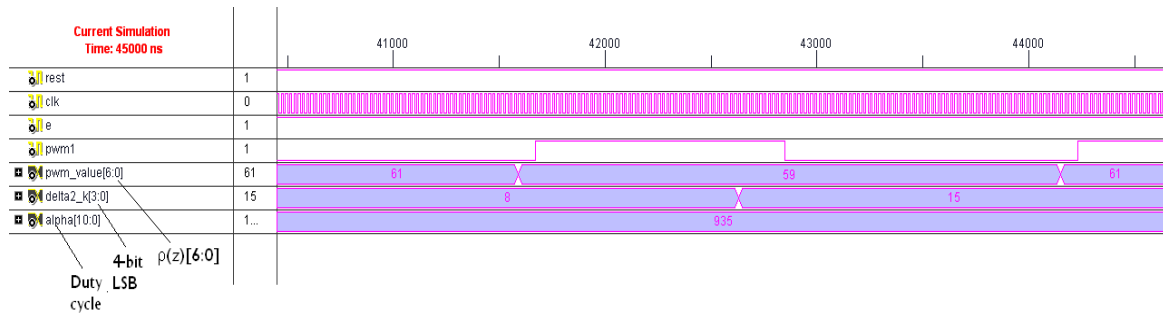


Fig. 6-17 Timing-simulation waveforms of Δ - Σ DPWM

The 7-bit duty cycle is delivered to the 4-bit segmented DCM phase-shift and the 3-bit counter comparator. The timing-simulation waveforms of the 7-bit duty cycle is illustrated in Fig. 6-18 with an example of duty value $D[6:0]=$ “0111110”. As it is shown, with the hardware segmented DCM phase-shift, it can increase 4-bit of the resolution, and finally the 11-bit DPWM signal is obtained.

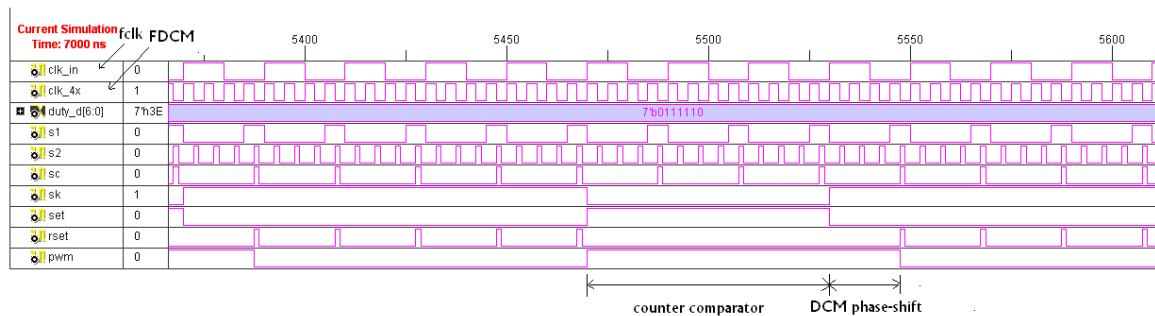


Fig. 6-18 4-bit segmented DCM phase-shift timing-simulation waveforms

The experimental tests of the hybrid DPWM will be detailed in chapter 7.

6.4 SUMMARY

To improve the output voltage accuracy in SMPS, the resolution of the ADC and DPWM is expected to be the highest. In this chapter, a review of different DPWM techniques has been presented. We have shown that a hybrid solution combining the hardware core DPWM and soft methods can improve the resolution of DPWM with reasonable clock frequency. First, an 11-bit hybrid DPWM based on the Delay-Line principle has been proposed and tested in simulation. In spite of silicon area reduction, the accuracy of the delay time, the required IC fabrication technologies and the linearity factors lead to a hybrid Δ - Σ DPWM solution. A first-order Δ - Σ architecture which has the advantages of simplicity for realization is introduced. However, this method has the disadvantage of low-frequency tones and slow convergence in first-order-modulators. To solve the problems, a second-order architecture is presented, and higher frequency tones are produced and faster averaging process is achieved.

Due to the absence of criterion for high-order Δ - Σ modulator, it is difficult to exactly estimate its stability. Based on the useful signal-stage Δ - Σ modulator, a cascaded modulator (MASH) modulator is adopted in this chapter.

CHAPTER 7 FPGA IMPLEMENTATION

The purpose of this chapter is to describe the implementation of the digitally controlled SEPIC system on a high frequency platform. The proposed digital controllers, extended Kalman observer and hybrid DPWM will be implemented in a Virtex-II FPGA board. As the calculation must adopt the fixed-point data format instead of a floating-point format, the digital controllers proposed in chapter 3 and chapter 4, the extended Kalman observer developed in chapter 5 and the proposed DPWM presented in the previous chapter are firstly tested in FPGA environment by using the fixed-point simulation toolbox provided by MATLAB. Then, after a description of each element of the experimental platform, experimental results will be detailed to verify the performances of the system.

7.1 INTRODUCTION TO FPGA

Field-Programmable Gate Arrays (FPGA) have become one of the key digital circuit implementation media over the last decade. A crucial part lies in their architecture, which governs the nature of their programmable logic functionality and their programmable interconnections. FPGA architecture has a dramatic effect on the quality of the final device speed performance, area efficiency, and power consumption. FPGA is a silicon device that can be electrically programmed to become almost any kind of digital circuit or system. FPGAs are configured in less than a second (and can often be reconfigured if a mistake is made) and cost from a few dollars to a few thousand dollars.

There are many FPGA manufacturers including Actel [Act05], Altera [Alt05], Atmel [ACP05], Cypress [CCP05], Lattice Semiconductor [LSC05], and Xilinx [Xil05]. Tools are usually provided from the manufacturer and allow the user to start with an HDL implementation of their hardware and through number of steps, generate the necessary information to configure the FPGA. Typically, the tools will generate a serial bitstream that contains the necessary information to configure the function of the logic cells and routing within the FPGA.

Taking Xilinx FPGAs for example, they are typically composed of the following: Configurable Logic Blocks (CLBs), Input/Output Blocks (IOBs), Block RAMs (BRAMs), multipliers, and clock managers. Other configuration infrastructures include Global Clocks (GCLKs), Input/Output Interfaces (IOIs), and BRAM Interconnect (BRAM INT). All of the

logic elements are connected by a network of complex routing and switch matrices as well as distributed clock resources.

7.1.1 VHDL and Design Entry

For the moment, there are currently available two industry standards related to the development of digital integrated circuits: VHDL and Verilog, which allow designers to specify digital logic. There are more features for high-level modelling in VHDL.

The digital design is generally done in three levels of design description: Behavioural, Structural and Physical. The digital design is generally done in the behavioural and structural domain and doesn't start at physical level.

Design starts with the functional designing at the behavioral level, and then goes to system, algorithmic and the RT level. After top-bottom partitioning, a bottom-up approach is necessary to describe the design flows at the RT levels, then algorithmic and system level. Once the design is written in HDL or drawn through a schematic editor, it is synthesized by a logic synthesizer, which transforms it into a net-list. Synthesis is done using commercial synthesis tools (XST for Xilinx). During synthesis, the HDL code is translated (or compiled) to the corresponding structural elements. At this point, a functional simulation is generally carried out, which checks the correctness of the HDL description.

Next step is the design implementation stage. In this case the implementation tools physically map the gates and logics from the net-list into the FPGA. At this time, the design path reaches the physical level. The implementation consists of three stages: Mapping, Place and Route. The Mapping tool fits the net-list gates into groups that fit into the LUTs (Look-Up Table) inside the CLBs (Configurable Logic Block). Then the Place and Route tool assigns these gates to specific CLBs and interconnects them through appropriate gate arrays. The choice of interconnections and CLBs are guided by the need to meet various optimization targets. Optimization may be done for area/real estate of the design or speed/fastness of the design. At this stage various design verifications can be done through timing simulations.

After implementation, the bitstream which contains the gate and placing information is generated and downloaded to the physical FPGA chip.

Fig. 7-1 shows the design flow chart of the digital controller in the Xilinx FPGA implementation, where the overall design is built on a top-down approach. The design flow includes four parts: Design entry, Synthesis, Implementation and Verification. The design is performed using Xilinx ISE 9.2i tool and verified on Virtex-II Pro FPGA board.

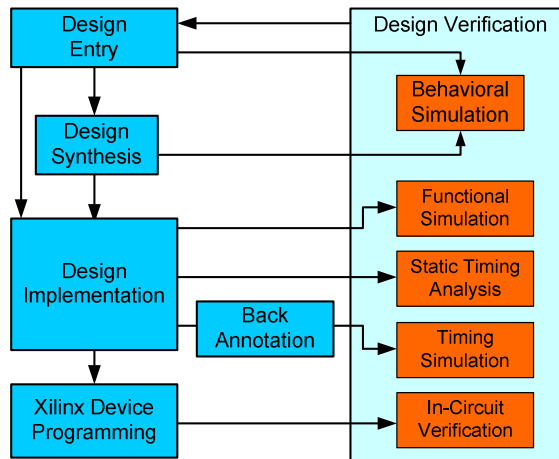


Fig. 7-1 VHDL based Xilinx ISE design flow

7.1.2 Xilinx Virtex-II Pro FPGA Family

The FPGA device used is XC2VP30 from Virtex-II Pro family FPGA of Xilinx [Inc05]. The package used is ft896 with speed grade -7. Xilinx Synthesis Tool (ISE9.2i) and VHDL are used as synthesis tool and programming language respectively. ModelSim Xilinx Edition-II from Mentor Graphics is used as the simulation tool. A Xilinx University Program Virtex-II Pro Development System Board (Xilinx XUP Virtex II Pro) is used. XC2VP30 has 3 million gates, 136 dedicated 18x18-bit multipliers, 8 DCMs, 644 user I/Os. In this work, we employ an external 32MHz clock and use internal DCMs to obtain several clocks for different blocks, such as A/D converter (16MHz), algorithm computation (128MHz), DPWM counter-comparator (32MHz, 64MHz and 128MHz with their four phase-shift 0° , 90° , 180° and 270° , etc.). Compared to DSP, which is tied by unique rigid clock, FPGA facilitates the configuration of clock resource and offers more flexible clock choices for diverse function blocks. The maximum speed of signal process inside Virtex-II Pro family FPGA can reach 400MHz, and interface I/Os signal transfer speed can reach as high as 200Mbs. The number of I/Os can be a determining factor for device or family of FPGA suitable for any particular application. Table 7-1 summaries the resource of Virtex-II Pro Family, where the shadow area is XC2VP30 in this case.

Table 7-1: Virtex-II Pro/Prox Family

Device	RocketIO Transceiver	PowerPC Processor	Logic cells	CLBs (1=4 Slices =max 128bits)		18x18 Bit Multiplier	Block SelectRAM+		DCM	Maximum User I/O Pads
				Slices	Max Distr RAM (kb)		18 kb Blocks	Max Block RAM (kb)		
XC2VP2	4	0	3,168	1,408	44	12	12	216	4	204
XC2VP4	4	1	6,768	3,008	94	28	28	504	4	308
XC2VP7	8	1	11,088	4,928	154	44	44	792	4	396
XC2VP20	8	2	20,880	9,280	290	88	88	1584	8	564
XC2VPX20	8	1	22,032	9,792	306	88	88	1584	8	552
XC2VP30	8	2	30,816	13,696	428	136	136	2448	8	644
XC2VP40	0 or 8 or 12	2	43,632	19,392	606	192	192	3456	8	804
XC2VP50	0 or 16	2	53,136	23,616	738	232	232	4176	8	852
XC2VP70	16 or 20	2	74,448	33,088	1,034	328	328	5904	8	996
XC2VPX70	20	2	74,448	33,088	1,034	308	308	5544	8	992
XC2VP100	0 or 20	2	99,216	44,096	1,378	444	444	7992	12	1,164

7.2 FIXED-POINT SIMULATION

The advances in FPGAs technology have had a big impact on the implementation of digital control algorithms [MC07]. Considering that the digital controllers and extended Kalman observer would be implemented into FPGA/ASIC, the calculation must adopt a fixed-point data format instead of a float-point format. Floating-point to fixed-point conversion may become a difficult and time consuming process. In fact, this process has been identified in a recent survey [Hil06] as the most difficult aspect of implementing a fixed-point algorithm on an FPGA. One key task for the hardware implementation, is to develop a fixed-point architecture for the different algorithms. In order to limit the hardware resources, most communications algorithms are implemented with fixed word-length accuracy. The performance of the algorithms must be analyzed in the fixed-point environment. Moreover, many algorithms are not implementable in their original form and require modifications. The performance of the modified algorithm must be tested and calibrated against the original.

Due to the approximate expression of the real value, the fixed-point data format is required to have a precision as high as possible. In order to obtain high accuracy, the parameter's accuracy is expected to be the highest. However, for a fixed word-width register, the availability of parameter range is contradictory with its accuracy. Furthermore for certain FPGA/ASIC process, the available register word-width is constrained by the algorithm computation speed. Therefore, the relation among the parameters' accuracy, the restraints of word-width and capacity of process must be carefully taken into account.

In our case the ADC model has a 10-bit resolution and the DPWM is set to 11-bit resolution. Thus the precision of the controller parameters are expected to be at least equal to the

precision of DPWM. The choice of parameters accuracy of extended Kalman observer follows the same need.

The modelling of the digitally controlled SEPIC is shown in Fig. 7-2, where the SEPIC is modelled by a hybrid model using Matlab s-function. All the calculations are computed in fixed-point format using Matlab/Simulink.

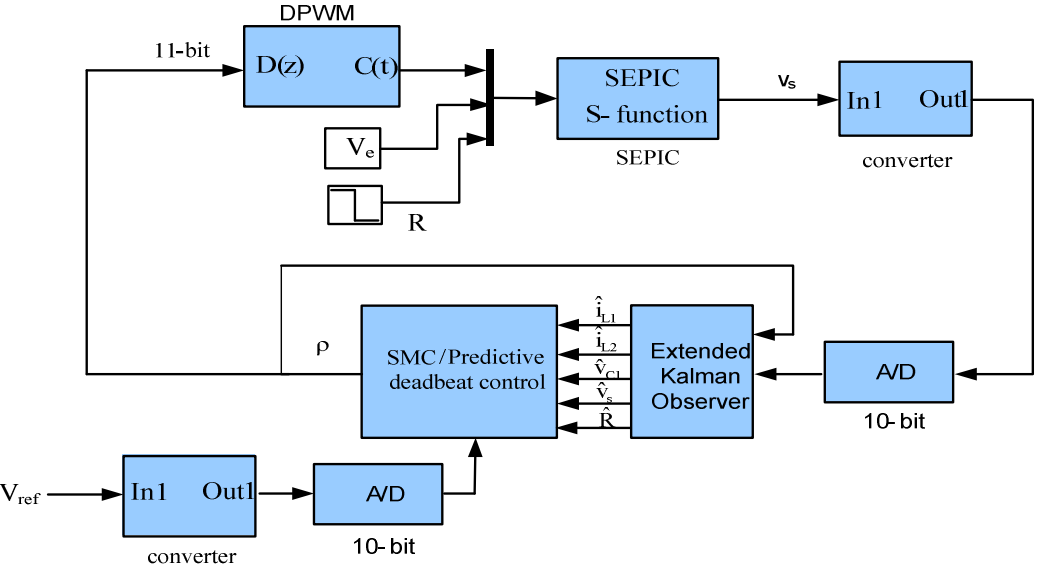


Fig. 7-2 Modelling of the whole system for a digitally controlled SEPIC

Firstly, the output voltage and reference voltage are delivered to the converter to obtain an appropriate voltage range for the A/D converter input. Then the output voltage is converted via A/D converter block to get a 10-bit resolution. The detailed A/D converter realization in Simulink is shown in Fig. 7-3.

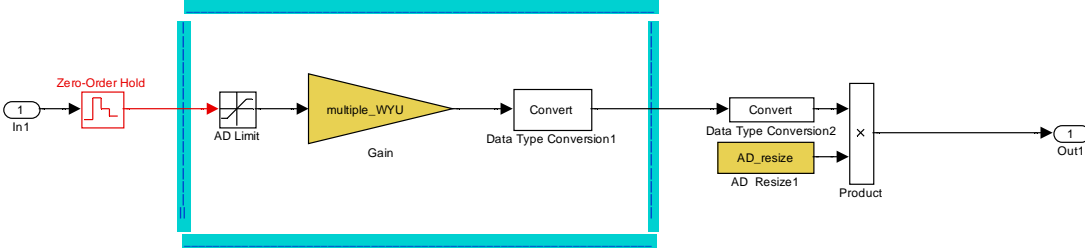


Fig. 7-3 The A/D block in Simulink

Based on the output voltage of A/D converter, the five observed state variables are estimated from the extended Kalman observer as shown in Fig. 7-2. Taking into account the parameters' accuracy and capacity of process, all the calculations are computed in fixed-point

computation with 15-bit fraction. The state variables are set in 21-bit, which possess 6-bit integer and 15-bit fraction giving a precision of $1/2^{15}$. Afterwards, the fixed-point state variables and reference voltage are delivered to the control algorithms (SMC or predictive deadbeat control), through the calculation and treatment in the algorithm block, the 11-bit duty cycle ρ is obtained. Finally, to improve the resolution of DPWM, ρ is transmitted to an 11-bit hybrid DPWM modulator. The segmented DCM is hard to be realized in the simulation, so the DPWM modulator only contains the mash Δ - Σ DPWM and counter comparator. The mash Δ - Σ DPWM block realization in Simulink is shown in Fig. 7-4.

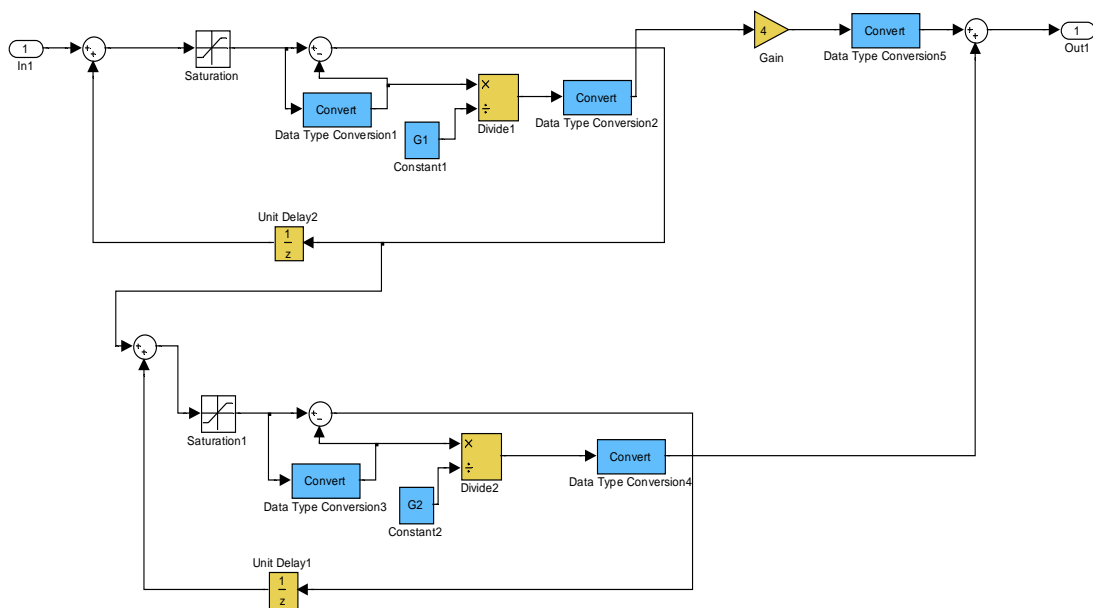
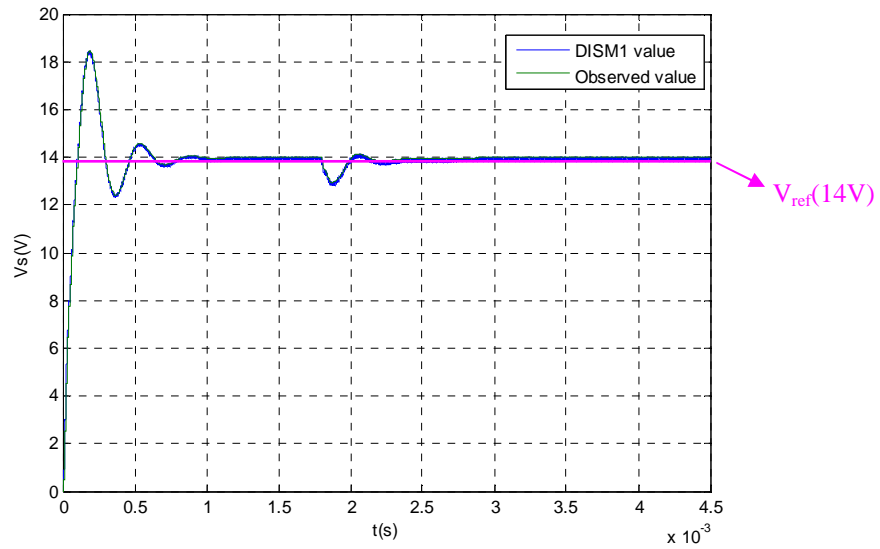


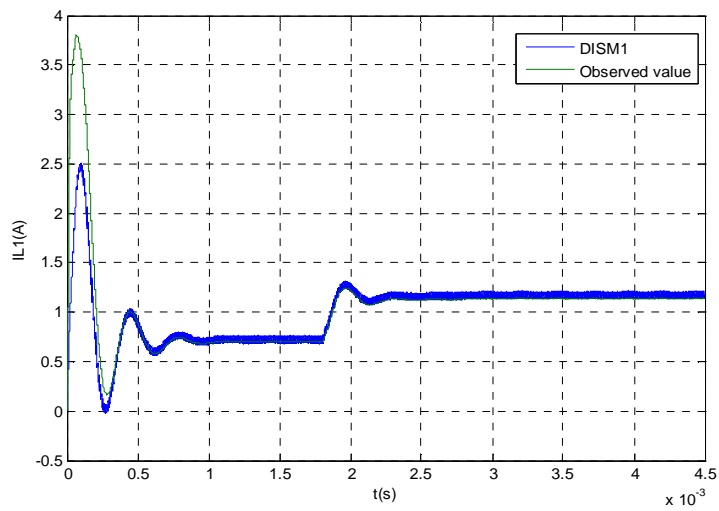
Fig. 7-4 Mash Δ - Σ DPWM block in Simulink

In order to test the SMC behaviour in the abovementioned condition, a DISM1 controller is employed to test the functionality of the proposed hybrid DPWM and extended Kalman observer using Matlab/Simulink.

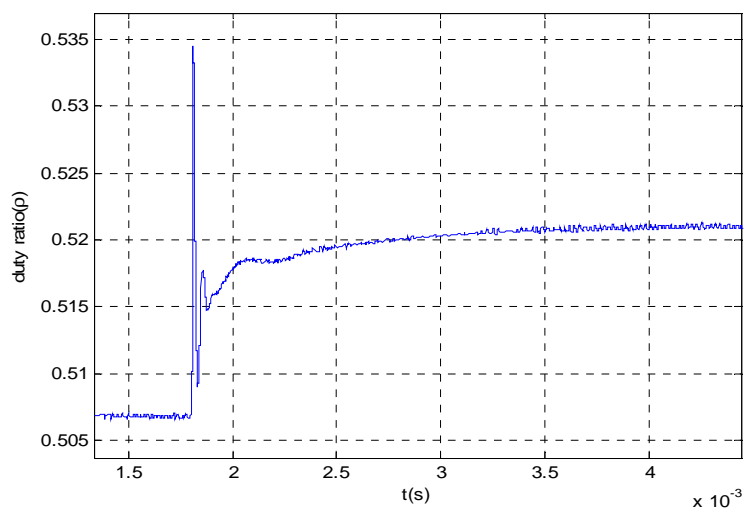
Figure 7-5 shows the comparison of waveforms between the measured and the observed values with DISM1 for a step change in reference (0 to 14V) and a load step variation from 20Ω to 13.3Ω at 0.0018s. Fig. 7-6 shows the dynamic response comparison of predictive deadbeat control with the same load variation at 0.003s. With the fixed-point quantification of controllers and observers, the states still illustrate the quick convergence and the robustness against strong disturbance of the load variation.



(a) Output voltage v_s

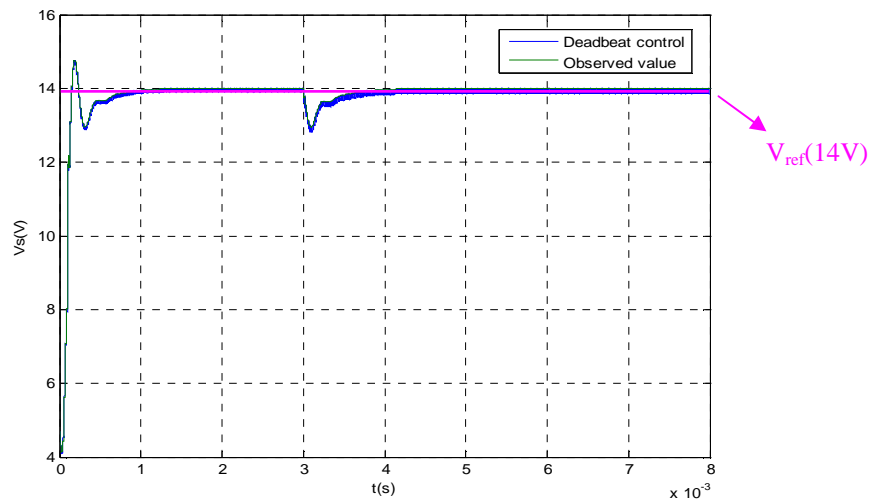


(b) Input inductance current I_{L1}

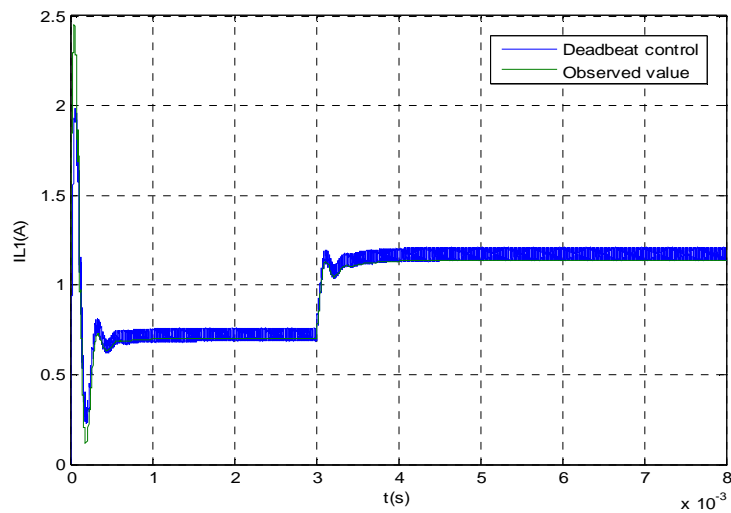


(c) PWM duty ratio

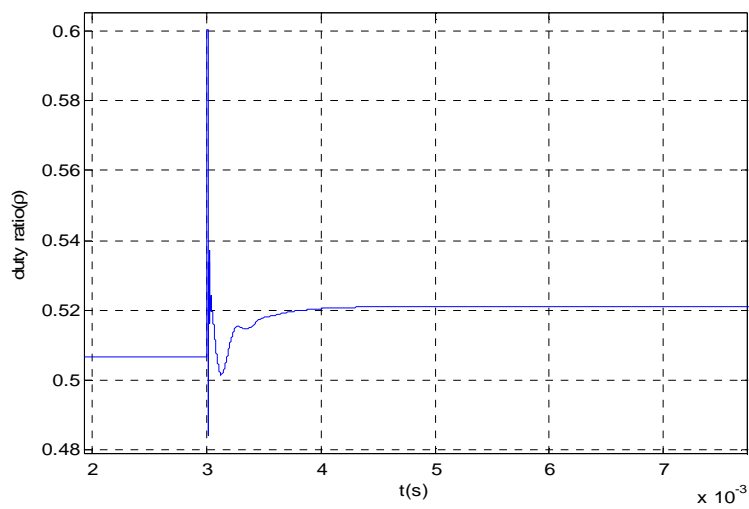
Fig. 7-5 Dynamic response of DISM1 controller for a load change from 0.7A to 1.08A:
 (a) output voltage, (b) input inductance current, (c) PWM duty ratio ρ



(a) Output voltage v_s



(b) Input inductance current I_{L1}



(c) PWM duty ratio

Fig. 7-6 Dynamic response of predictive deadbeat controller for a load change from 0.7A to 1.08A:(a) output voltage, (b) input inductance current, (c) PWM duty ratio ρ

7.3 TEST PLATFORM DESCRIPTION

To demonstrate the functionality of the proposed digitally-controlled prototype SEPIC, the proposed control algorithms are verified through FPGA implementation. A test platform is built and set up as shown in Fig. 7-7. The corresponding system block diagram is shown in Fig. 7-8.

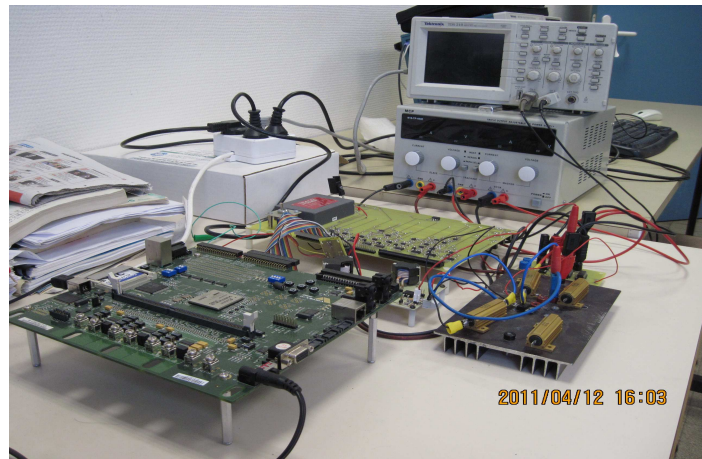


Fig. 7-7 Experimental test platform

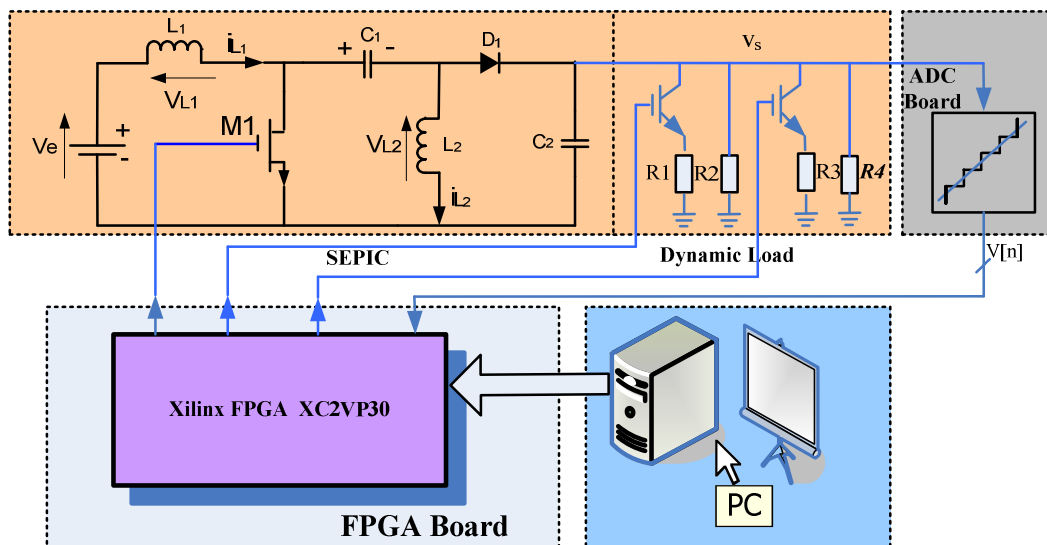


Fig. 7-8 Block diagram of the experimental test platform

The test platform consists of three boards.

- 1). A FPGA board with USB that is used to connect to a host PC, which runs software Xilinx ISE9.2i that can program on-line the digital controller. The implementation of digital algorithm, extended Kalman observer and DPWM is designed in VHDL and schematic editor using Xilinx ISE tool (design, function simulation, time simulation, mapping, placement and route). The USB connector is used to download the final bitstream (routed circuits) to FPGA.

2). A SEPIC which is fabricated with a dynamic load trigger circuit. The dynamic load trigger circuit is used to test the transient response of SEPIC.

3). A third board that serves as the feedback voltage sampling contains an A/D component ADS900, which takes analog-to-digital sample at 16MHz rate and the sampling clock is offered by DCM of FPGA.

The detailed functionalities of these three boards will be discussed in the following sections.

7.3.1 FPGA Board

Fig. 7-9 shows the FPGA development board, where XCV2P30 FPGA supports the DPWM and digital control algorithms. The FPGA board communicates with a host PC through USB which downloads the final synthesized circuit. The software Xilinx ISE9.2i supports the program on-line to modify the function of the digital controller. Since the automatic synthesis, simulation, timing analysis, and verification tools are available for FPGA implementation, it is delightful that these well-established and automated tools can dramatically speed-up the design procedure. Moreover the design can be easily moved to another target or be modified to meet new requirements.

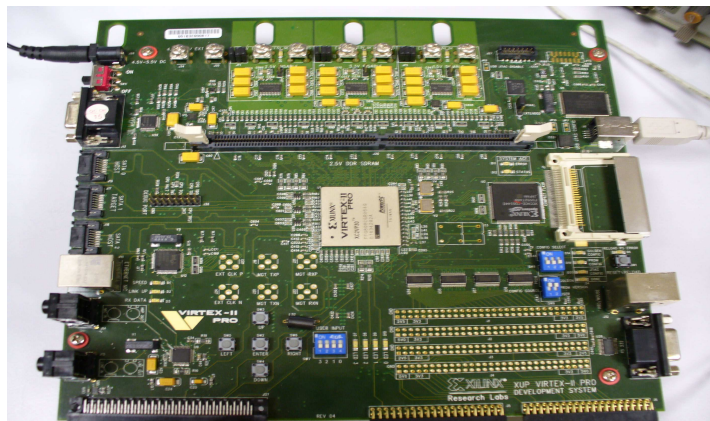


Fig. 7-9 FPGA board

7.3.2 SEPIC Board

The SEPIC board is shown in Fig. 7-10. The low-voltage high-frequency MOSFET IRFR3518 is used with high-speed driver EL7202CS. Currently, the experimental board operates at 500kHz. In future application with the use of proper technique of integrated circuit, the switching frequency can be greatly increased to meet the miniaturization demand.

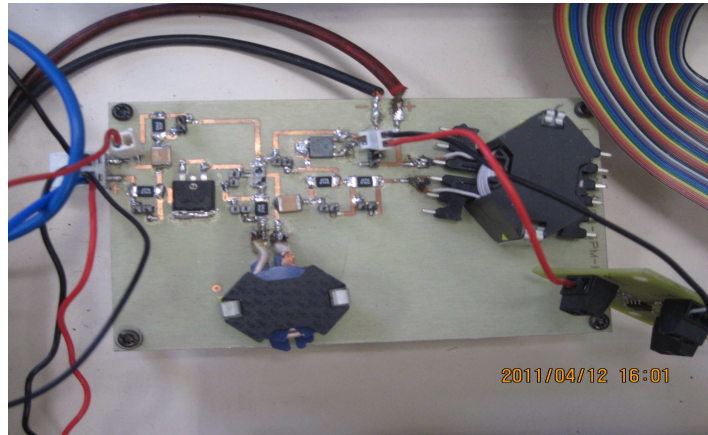


Fig. 7-10 SEPIC board

The state variables can be measured with the corresponding sensor for comparative study with the observed state variables. All the currents are measured through shunt resistors placed in series with the component as show in Fig. 7-11 (R_1 - R_5). The value of R_1 , R_2 , R_3 , R_4 , R_5 is the same of $30\text{m}\Omega$. Remark that for the experimental validation of the proposed control algorithms, only the output voltage sensor is used.

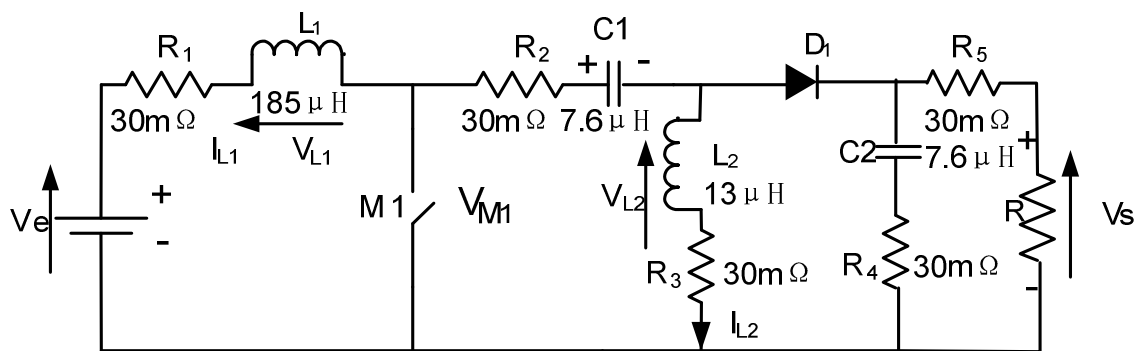


Fig. 7-11 SPEIC scheme with shunt resistors

In order to test the dynamic performance of the digital controllers, an additional transient load variation circuit is also set on the board. The load variation circuit is the same as that introduced in chapter 3, while another different load-line is used. Table 7-2 summarizes the parameters of the voltage regulator.

Table 7-2:500kHz SEPIC prototype parameters

Symbol	Parameter name	Value
V_e	Input voltage	15V
V_{ref}	Reference voltage	14V
f_{sw}	Switching frequency	500kHz
L_1	Input Inductance	185 μ H
L_2	Output Inductance	13 μ H
C_1	Capacitor 1	7.6 μ F
C_2	Capacitor 2	7.6 μ F
R	Resistor	20 Ω
r_{L1}	Inductance ESR	1.2 Ω
r_{L2}	Inductance ESR	0.8 Ω

7.3.3 A/D Converter Board

The A/D conversion is implemented using an A/D component (ADS900). **Appendix B** shows the circuit schematic. Corresponding to the abovementioned sensors, we set up ADCs to convert the SEPIC state variables as shown in Fig. 7-12.

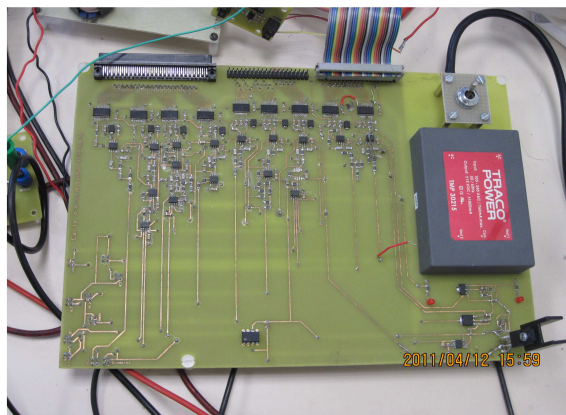


Fig. 7-12 A/D converter board

Table 7-3 lists the configuration parameters of ADC. The ADC device is probably a high energy consuming block in the system, and remains an effort-consuming task in ASIC implementation. This issue is not discussed here.

Table 7-3:ADC configuration parameters

Analog Device	ADS900
Resolution	10-bit
Supply operation	+2.7V ~ +3.7V
Sampling rate	20MHz
Single-ended input range	1V~2V
Internal reference	1.5V

To make the different state vectors appropriate for ADC application, low pass filters are set up. The goal of filter is to attenuate the high frequency (500kHz) introduced by the switching. Sallen-Key is a widely used second-order low-pass filter. Due to the surface constraint of the A/D board, only one OPA (Operational Amplifier) is used for each filter. The Sallen-Key filter topology is shown in Fig. 7-13. The filter design is given in **Appendix C**.

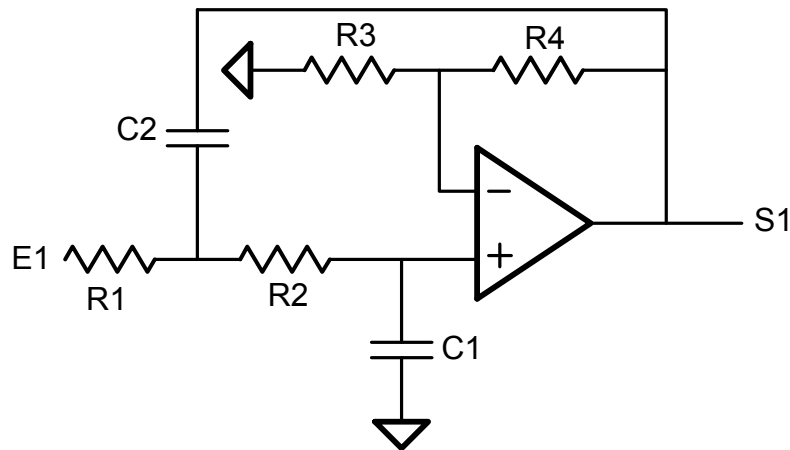


Fig. 7-13 Sallen-Key filter topology

Beside of acting as the filter for ADC, as the input range of ADS900 is limited between 1V and 2V, an adaptation circuit of Sallen-Key filter is introduced for each sensor. The maximum output voltage for SEPIC is limited to 20V. Voltage measurement consists of a simple voltage divider by 25 reducing the voltage to 0.8 V maximum as shown in Fig. 7-14. The values obtained from filters are limited between 0 and 1V. Then an offset of 1V reference voltage is added to adopt the voltage of A/D converter within the boundary of 1V and 2V.

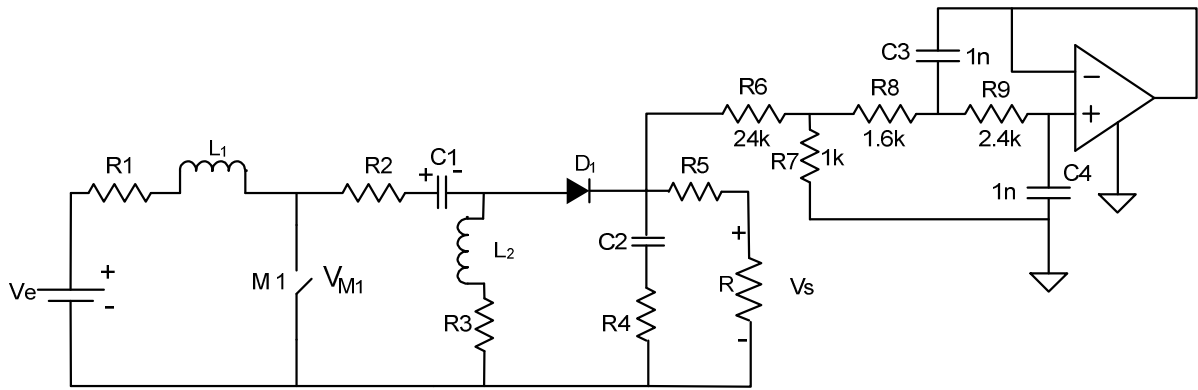


Fig. 7-14 Measurement of output voltage

To avoid damaging ADC by a voltage above the maximum allowed voltage, a protection circuit shown in Fig. 7-15 is used. It is composed of a resistance of 100Ω and a Schottky diode of $0.3V$ as in the diagram. Thus, the ADC input voltage will not exceed $2V$.

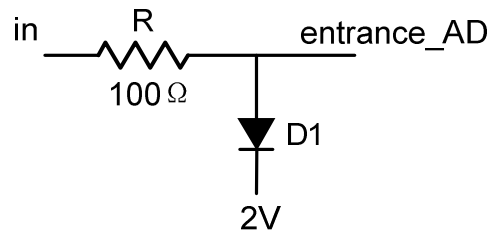


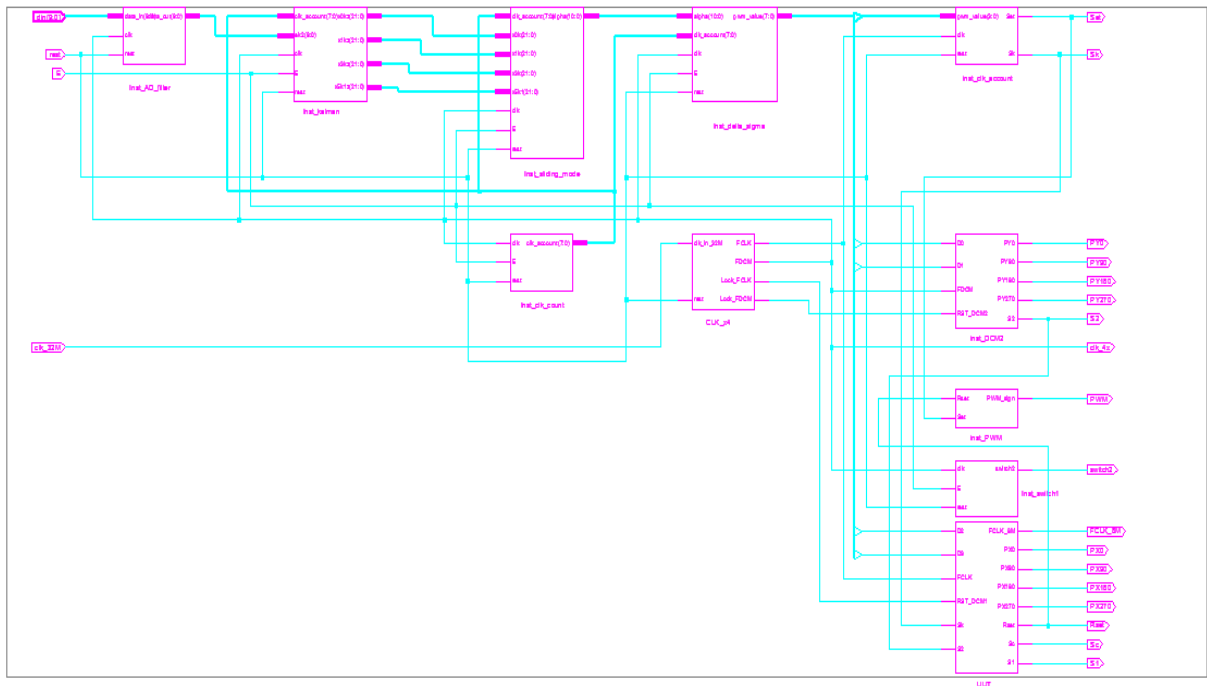
Fig. 7-15 Protection circuit for ADC input

7.4 EXPERIMENTAL RESULTS

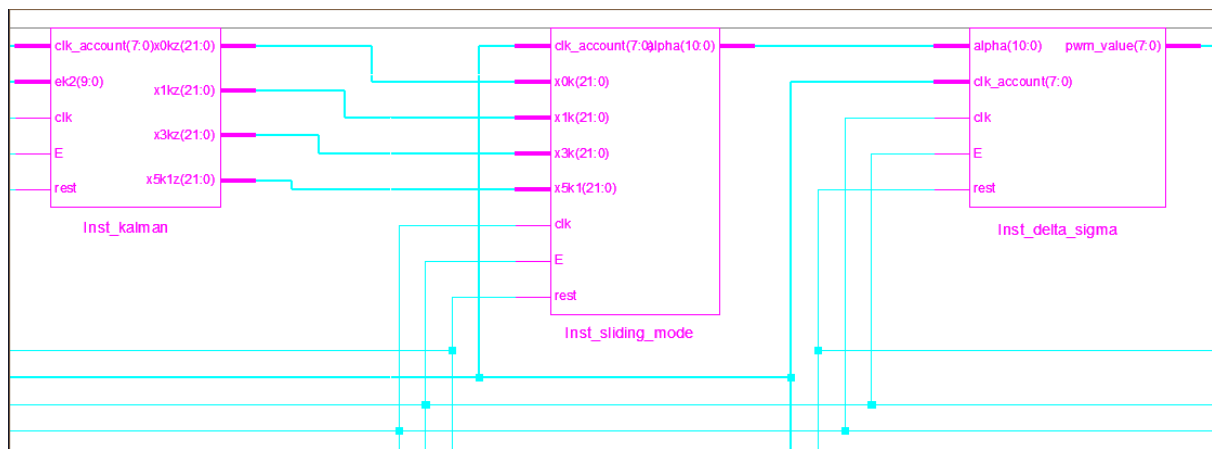
The experimental results obtained with the FPGA test platform will be given in this section, where the 11-bit Hybrid Δ - Σ DPWM (Chapter 6) operates at $500kHz$, SMC(chapter 3) and predictive deadbeat controller (Chapter 4) algorithms are applied respectively and the extended Kalman observer (chapter 5) is used. The specification parameters of SEPIC for the experiment are illustrated in Table 7-2.

Before the experimental results are given, the RTL level schematic map of the whole system implementation including AD_filter, extended Kalman observer, sliding mode controller, 11-bit hybrid DPWM, load switch and other auxiliary circuits are provided as shown in Fig. 7-16(a). The core part of our work is shown in Fig. 7-16(b). It can be seen that the state vectors are obtained with the extended Kalman observer, and then they are sent to the controller, taking the sliding mode controller for example, with the calculation in the controller, we get an 11-bit duty cycle value which is then delivered to Δ - Σ modulator. For the

open-loop system, the extended Kalman observer part and sliding mode controller part are saved.



(a)



(b)

Fig. 7-16 The schematic map in RTL level (a) FPGA-based whole system (b) FPGA-based extended Kalman observer, sliding mode controller, and Δ - Σ DPWM

7.4.1 Open-Loop Operation of DPWM

In this section, the experimental results of open-loop test of DPWM (hybrid Δ - Σ DPWM) are illustrated. As detailed in chapter 6, the hybrid DPWM consists of soft method (MASH Δ - Σ modulator) and hardware core DPWM (counter-comparator and segmented DCM phase-shift block). The hybrid DPWM operates at 500kHz, where the MASH Δ - Σ modulator is the

soft way to deal with the LSB[2:0], and the hardware core DPWM is to implement the MSB[10:3]. The operation condition of the DPWM architecture is illustrated in Table 7-4.

Table 7-4: Summarization of hybrid DPWM

Symbol	Definition	Hybrid Δ - Σ DPWM
N_{DPWM}	Bit number of DPWM effective resolution	11-bit ρ [10:0]
N_{core}	Bit number of counter-comparator	4-bit ρ [10:7]
$N_{phase-shift}$	Bit number of segment DCM	4-bit ρ [6:3]
$N_{\Delta-\Sigma}$	Bit number of Δ - Σ	3-bit ρ [2:0]
f_s	Operation switching frequency in FPGA	500kHz
f_{clk}	System clock for hardware core DPWM	$2^{N_{core}} f_s = 8\text{MHz}$
f_{DCM}	Phase-shift clock inside DCM block	$2^{N_{core}+2} f_s = 32\text{MHz}$

Fig. 7-17 shows the waveforms of hybrid DPWM in open-loop test with duty cycle “10001000010”, the PWM gate signals of MOSFET and output voltage v_s are shown. The performance of Hybrid DPWM is quite satisfying as shown in figure in spite of some noise influence.

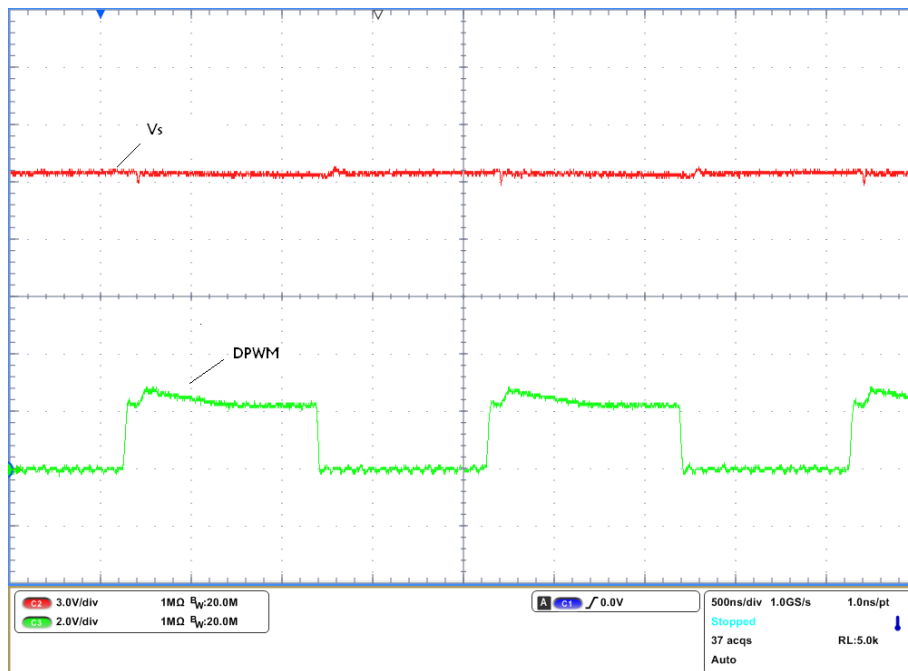


Fig. 7-17 Waveforms of hybrid DPWM in open-loop test for output voltage and PWM signal

7.4.2 Closed-Loop Operation

As abovementioned, only the output voltage is measured for the closed-loop operation. Thus the closed-loop system consists of a 10-bit ADC, digital controllers, extended Kalman observer and an 11-bit hybrid DPWM.

A. SMC control operation

For SMC control operation, the proposed DISM1 and DISM2 are tested respectively for the reference voltage and load variation. The latter is performed by connecting a 20Ω resistor to SEPIC output terminals, where another load-line of 40Ω resistor is connected in parallel. This leads to a 13.3Ω resistor and corresponds to a load variation from $0.7A$ to $1.08A$.

Fig. 7-18 shows the output voltage response of the DISM1 with a reference voltage change between $13V$ and $15V$. It illustrates that the output voltage can precisely follow the output reference voltage changes. The result shows that the settling time is almost $1ms$ and the overshoot on the output is less than $1V$.

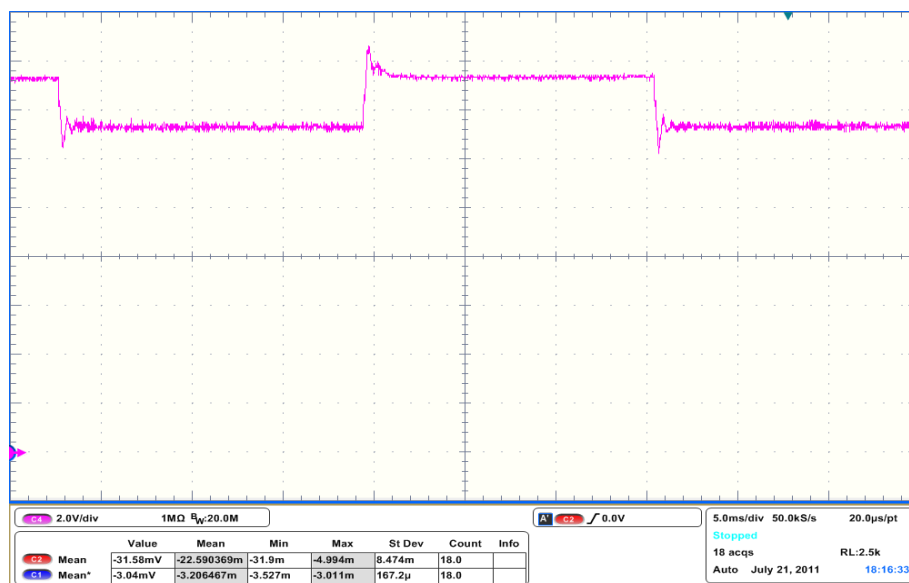
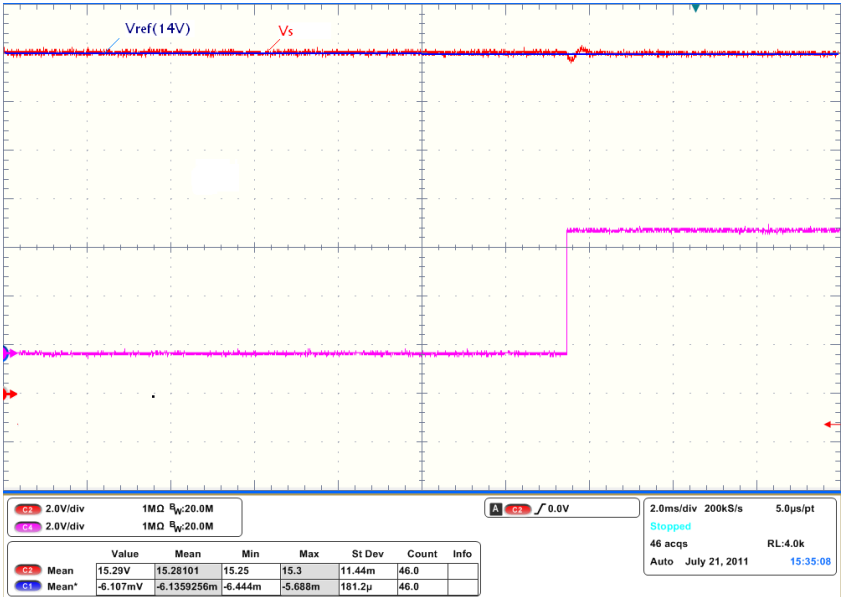


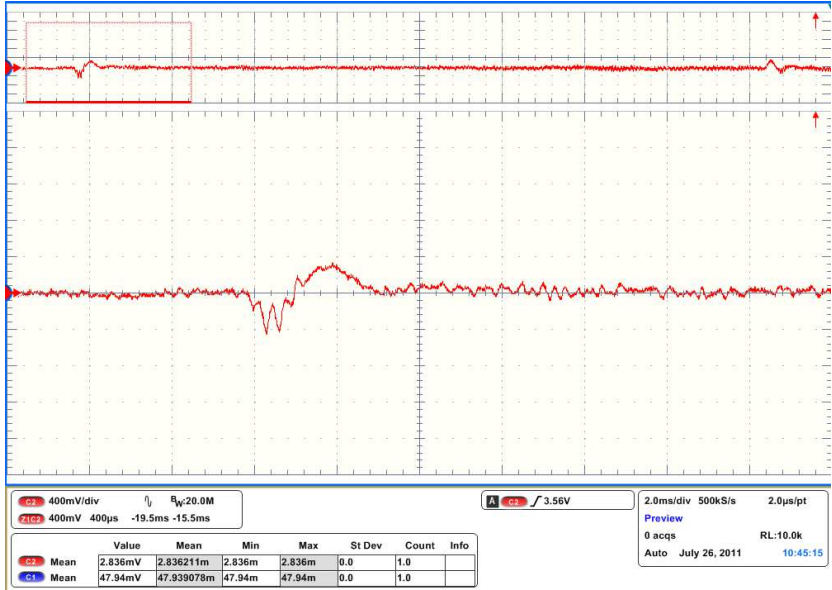
Fig. 7-18 Output voltage response of DISM1 when reference voltage changes between $13V$ and $15V$

To test the dynamic response when the load changes, SEPIC is first in steady-state operation where the controller maintains the deserved output voltage at $14V$. Then the load suddenly varies from $0.7A$ to $1.08A$ (20Ω to 13.3Ω). Fig. 7-19 shows the corresponding output voltage v_s using the proposed DISM1. It can be seen that when the SEPIC is in steady-state operation, the controller maintains the derived output voltage ($14V$). In transient operation, the result shows that the settling time is small, the DISM1 takes about $3ms$ to

recover to the steady state, and the overshoot on the output voltage is almost 400mV, i.e. 3% of the output voltage (14V).



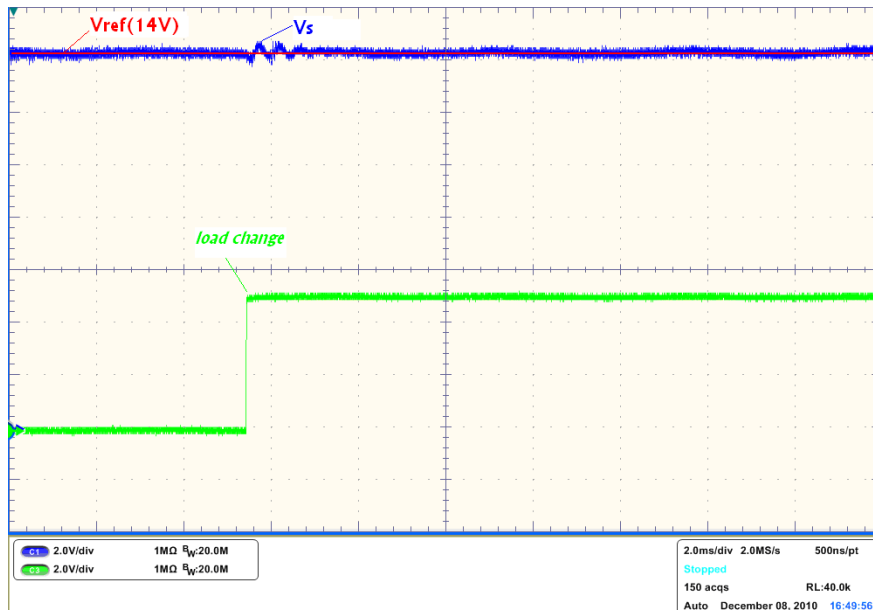
(a)



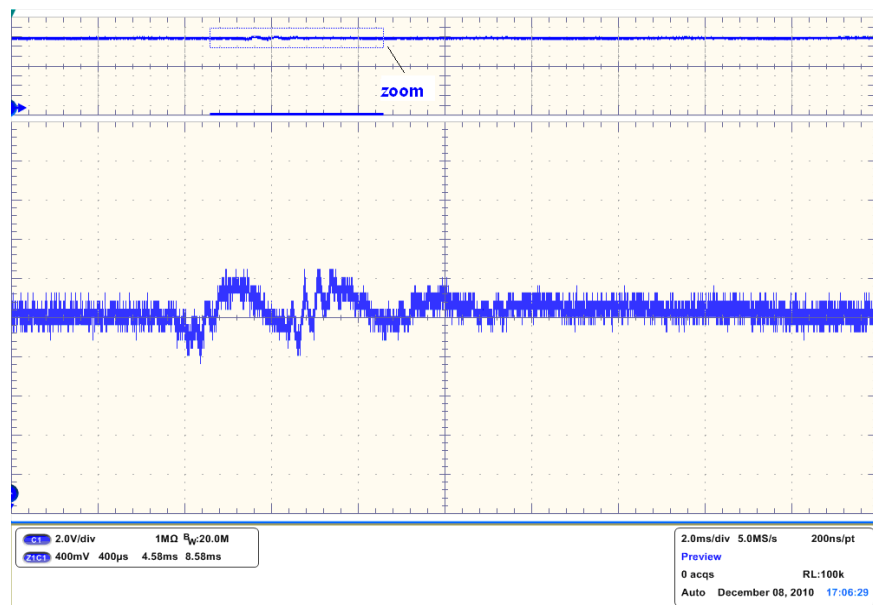
(b)

Fig. 7-19 Experimental waveforms of DISM1 when load changes from 0.7A to 1.08A (a) response of output voltage v_s , (b) zoom of output voltage response

Under the same load variation condition, Fig. 7-20 illustrates the output voltage with the proposed DISM2. It shows that the DISM2 can also eliminate the steady state errors. However, it takes 6ms to attain steady-state.



(a)



(b)

Fig. 7-20 Experimental waveforms of DISM2 when load changes from 0.7A to 1.08A (a) response of output voltage v_s , (b) zoom of output voltage response

B. Predictive deadbeat controller operation

The behaviour of output voltage in the case of output reference voltage variation between 13V and 15V is given in Fig. 7-21. It can be seen that the predictive deadbeat control has better dynamic performances than SMC with lower voltage overshoot.

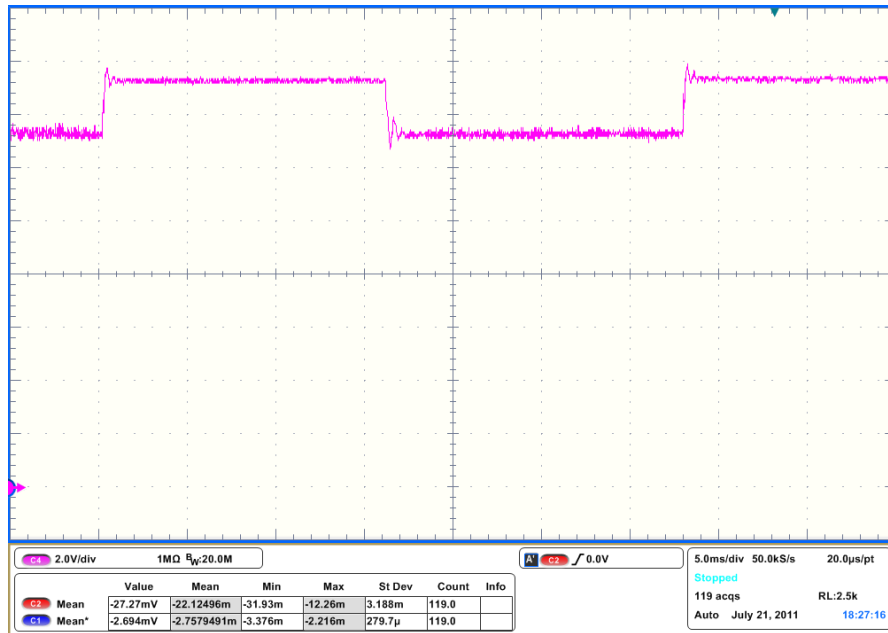
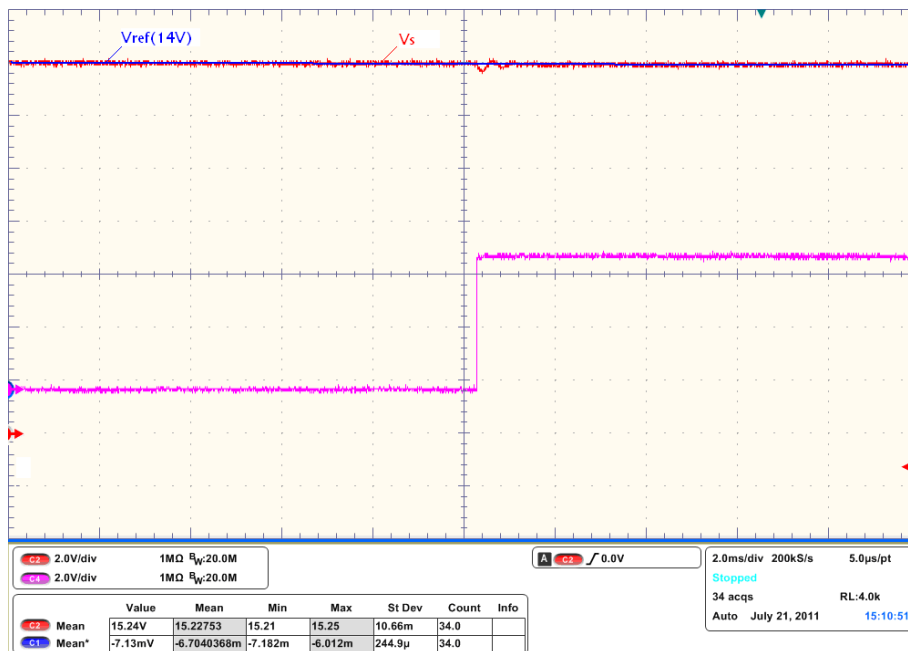
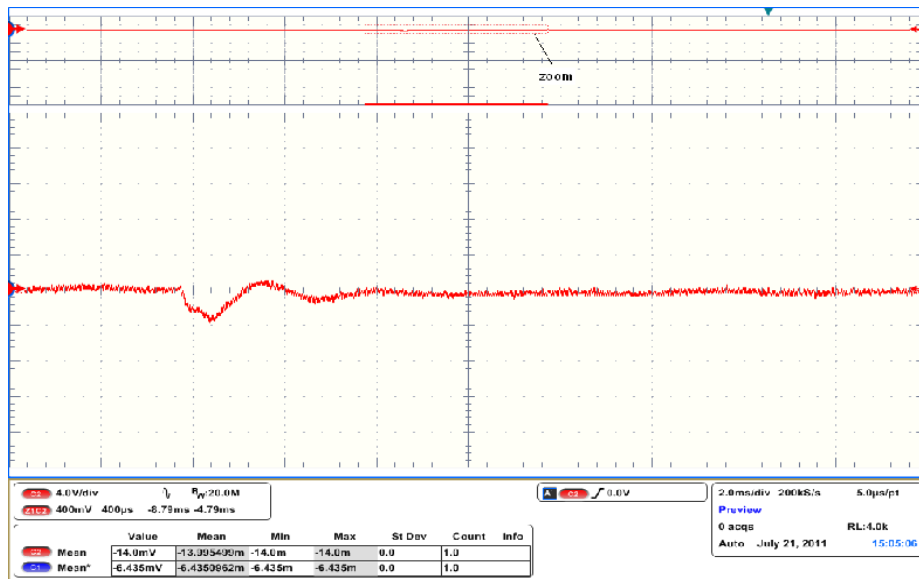


Fig. 7-21 Output voltage response of predictive deadbeat controller when reference voltage changes between 13V and 15V

During steady-state operation, to test the dynamic response towards load variation, the load is suddenly being varied from 0.7A to 1.08A (20Ω to 13.3Ω). Fig. 7-22 shows the corresponding output voltage v_s . The results show that the transient response time is short with predictive deadbeat controller, it takes less than 4ms to recover to the steady state, and produces an overshoot of 400mV.



(a)



(b)

Fig. 7-22 Experimental waveforms of predictive deadbeat controller when load changes from 0.7A to 1.08A (a) response of output voltage v_s , (b) zoom of output voltage response

C. Discussions

From the above experimental results, it can be deduced that both SMC and predictive deadbeat control have good performances. It's interesting to compare their FPGA resource consumption. The FPGA resources consumption of the three controllers is summarized in Table 7-5. As described previously, the predictive deadbeat control requires the least FPGA resources. From the experimental results, it can be seen that DISM1 controller offers a better performances than DISM2 controller. However, DISM2 controller is a simplified form of DISM1, as the Table 7-5 shows, so it consumes less FPGA resources than DISM1. Thus the controllers DISM1 and DISM2 are chosen to get the best trade-off between system performance and FPGA resources occupation. Moreover, the FPGA resources consumption will give a reference for the future ASIC design.

Table 7-5: Performance comparison of DISM1, DISM2 and Predictive deadbeat control

Logic Utilization	Controller	Used	Available	Utilization
Number of Slice Flip Flops	DISM1	2,721	27,392	9%
	DISM2	2,655		9%
	Predictive	2,164		7%
Number of 4 input LUTs	DISM1	2,234	27,392	8%
	DISM2	2,197		8%
	Predictive	1,909		6%
Logic Distribution				
Number of occupied Slices	DISM1	1,682	13,696	12%

	DISM2	1,648		12%
	Predictive	1,442		10%
Number of Slices containing only related logic	DISM1	1,682	1,682	100%
	DISM2	1,648	1,442	100%
	Predictive	1,442		100%
Number of Slices containing unrelated logic	DISM1	0	1,682	0%
	DISM2		1,442	
	Predictive			
Total Number of 4 input LUTs	DISM1	2,323	27,392	8%
	DISM2	2,286		8%
	Predictive	1,975		7%
Number used as logic	DISM1	2,234		
	DISM2	2,197		
	Predictive	1,909		
Number used as a route-thru	DISM1	88		
	DISM2	88		
	Predictive	65		
Number used as Shift registers	DISM1	1		
	DISM2	1		
	Predictive	1		
Number of bonded IOBs	DISM1	17	556	3%
	DISM2	17		
	Predictive	17		
IOB Flip Flops	DISM1	12		
	DISM2	12		
	Predictive	12		
Number of PPC405s	DISM1	0	2	0%
	DISM2	0		
	Predictive	0		
Number of MULT18X18s	DISM1	83	136	61%
	DISM2	81		59%
	Predictive	74		54%
Number of GCLKs	DISM1	4	16	25%
	DISM2	4		
	Predictive	4		
Number of DCMs	DISM1	2	8	25%
	DISM2	2		
	Predictive	2		
Number of GTs	DISM1	0	8	0%
	DISM2	0		
	Predictive	0		
Number of GT10s	DISM1	0	0	0%
	DISM2	0		
	Predictive	0		
Total equivalent gate count for design	DISM1	397,482		
	DISM2	384,522		
	Predictive	348,838		
Additional JTAG gate count for IOBs	DISM1	816		
	DISM2	816		
	Predictive	816		

7.5 SUMMARY

In this chapter, the FPGA based implementations of digital controllers for SEPIC is detailed. First, the feature and design procedure of FPGA is briefly introduced. Then the test platform and experimental conditions for the proposed digital controllers which mainly include FPGA board, SEPIC circuit and ADC are illustrated. With the abovementioned experimental devices, the combination of digital controllers (SMC, predictive deadbeat controller), hybrid DPWM and extended Kalman observer is implemented.

The experimental results are given to validate the performance of SMC and predictive deadbeat control. It shows that the proposed digital controllers can achieve good dynamic response like fast transient response, lower overshoot in the high switching frequency application. Finally, the FPGA resources of the proposed controllers are compared; it is clear that the predictive deadbeat control has the simplest calculation architecture and occupies the least FPGA resources. The simple execution characteristics of the proposed controllers make them candidates for the future ASIC design in low-power SEPIC.

CONCLUSION AND PERSPECTIVE

Digital control is becoming a trend in the field of SMPS, the digital control exhibits the advantages of flexibility and programmability, less susceptibility to component variations, as well as advanced control algorithms implementation. SEPIC presents a great advantage over other converter topologies. However, being of forth-order system, SEPIC is severely nonlinear with a behaviour depending on operating conditions. High frequency digital control applied to SEPIC is seldom reported. Moreover, it should be noted that the digital control in low-power high frequency SEPIC faces several practical problems, such as size miniaturization, power consumption and sensor saving. The research interest of the thesis was to explore practical ways of advantages of digital control in realization. The main objectives of this work were to develop simple control laws which can overcome the main problems affecting SEPIC and can be implemented in FPGA or in future in ASIC for high frequency application. .

The major contributions and conclusions of this work can be summarized as follows:

- First of all, three kinds of SEPIC models are established. For the linear model which is currently used for control design, frequency responses are verified with experimental results of two real circuits. It has been shown that the static and dynamic behaviours of SEPIC vary strongly with regard to the operating conditions. A nonlinear model is more adequate for the design of control law.
- Based on the nonlinear averaged model, a fixed frequency sliding mode control is investigated for SEPIC. Three sliding surfaces are proposed. Their influences on the control performance have been discussed. As a conclusion, a surface containing only the output voltage error cannot stabilize the system. That is why we have proposed to incorporate an inductor current term into the sliding surface. To suppress the static errors of the output voltage, the sliding surface must include at least a double-integral of the voltage error. Addition of the input inductor current error into the double-integral term can improve the dynamic performance but the control parameter tuning is a little more difficult (4 parameters instead of 3). Moreover, an additional multiplication and addition operation is added in the control law. The proposed controller is implemented into dSPACE board to control a developed SEPIC converter having a switching frequency of 20kHz. The experimental and simulation results show the good dynamic and static performances of this type of controller.

- Another control law investigated in this thesis is the predictive dead-beat control since this type of controller is known for its simple implementation, for its fast dynamic response and robustness against parameter variations. We have developed a prediction model based on the discretization of the hybrid model. The adopted controller is based on the multi-loop structure where the input inductor current is controlled by the predictive deadbeat control while the outer voltage loop contains a classical PI controller and generates the reference for the inner loop. Regarding the time delays due to digital control computation, a compensated deadbeat current control algorithm is proposed. For high frequency applications where FPGA implementation is required, a simplified algorithm is developed. The stability versus the parameter variation is investigated, which provides a method for the robust analysis of the predictive dead-beat control. Finally, the simulation results have confirmed the effectiveness of the proposed algorithms. Experimental tests on the dSPACE platform for the 20kHz SEPIC verify good performance towards fast transient response and load variation.
- To reduce the number of sensors used especially in embedded systems, two nonlinear observers are presented for estimating all the states from the only measurement of output voltage. The first one is the sliding mode observer, while the second one is the extended Kalman observer. In both cases, the observer design is based on an augmented state-space model in order to take into account the load variation. Although both observers offer good dynamic and static performance, the Kalman observer is preferable for digital implementation since it's directly designed in a discrete-time form.
- For the implementation of controllers on FPGA platform, an analysis of the technical difficulties associated with the implementation of digital control at high switching frequency has been made. A comparison between the existing DPWM architectures has been established. We have focused on two kinds of hybrid DPWM architectures which combine hardware and software. The first method combines delay-line and counter-comparator which allow us to reduce the silicon area taken by a large number of multiplexers. However, the accuracy of the delay time is limited, and the accuracy of delay propagation is sensitive to various effects. Hence, we propose another 11-bit hybrid DPWM solution which is composed of 4-bit segmented DCM phase-shift modulator, 4-bit MASH Δ - Σ approach and 3-bit counter-comparator. Thus the clock requirement for the system is merely $2^3 \cdot f_{sw}$ instead of $2^{11} \cdot f_{sw}$ required for a classical solution, which dramatically alleviates the high-frequency clock for the digital system.

- The final contribution consists of the implementation of control laws into a high frequency platform. A 500kHz SEPIC and all the interfaces with a Virtex-II FPGA development board are designed. The proposed DPWM, two double integral sliding mode controllers, predictive deadbeat control and extended Kalman observer are validated following a methodological step from simulation to experimentation.

All the experimental results confirm the excellent static and dynamic performances of the proposed approaches.

In conclusion, the proposed digital control system for SEPIC implemented on FPGA can act as a reference for high frequency, low-power, digitally controlled high order SMPS. The methodologies developed for SEPIC in this thesis are general and can be extended to other power converters or other embedded systems.

Perspective

The issues discussed in this thesis opens up many perspectives concerning the improvement of power converter performance digitally controlled at high switching frequency. Some suggestions for future areas of research are given as follows:

- Only the continuous conduction mode (CCM) was studied in this thesis. It would be interesting to work with both continuous/discontinuous conduction modes.
- For the developed controllers and observers, a more detailed study of robustness and stability would be interesting to guarantee the theoretical global stability.
- Beside the proposed control algorithms, other nonlinear control strategies can be studied for further investigation. For example, a passivity-based controller which is typically applied to mechanical systems and magnetic levitation systems is of potential for the SEPIC control. Another direct predictive control strategy which has been successfully used to AC motor drives would be investigated to be compared with the predictive deadbeat control. The obtained results show that the observer consumes a lot of resources in the FPGA realization. For the future ASIC realization, the working switching frequency will be raised to MHz, a simplified extended Kalman observer or other observer design need to be studied for better resource utilization.
- This thesis consists of preliminary research work. The experiment in this thesis is only dedicated to validate the functional performance of digital controller in FPGA. ASIC implementation of the proposed algorithms is a necessary procedure, if the control methods would be applied in industrial power electronics project. Unfortunately the IC fabrication is

not available in time of this work. Future work may focus on the simplification of the proposed algorithms, and on the reduction of resources consumption.

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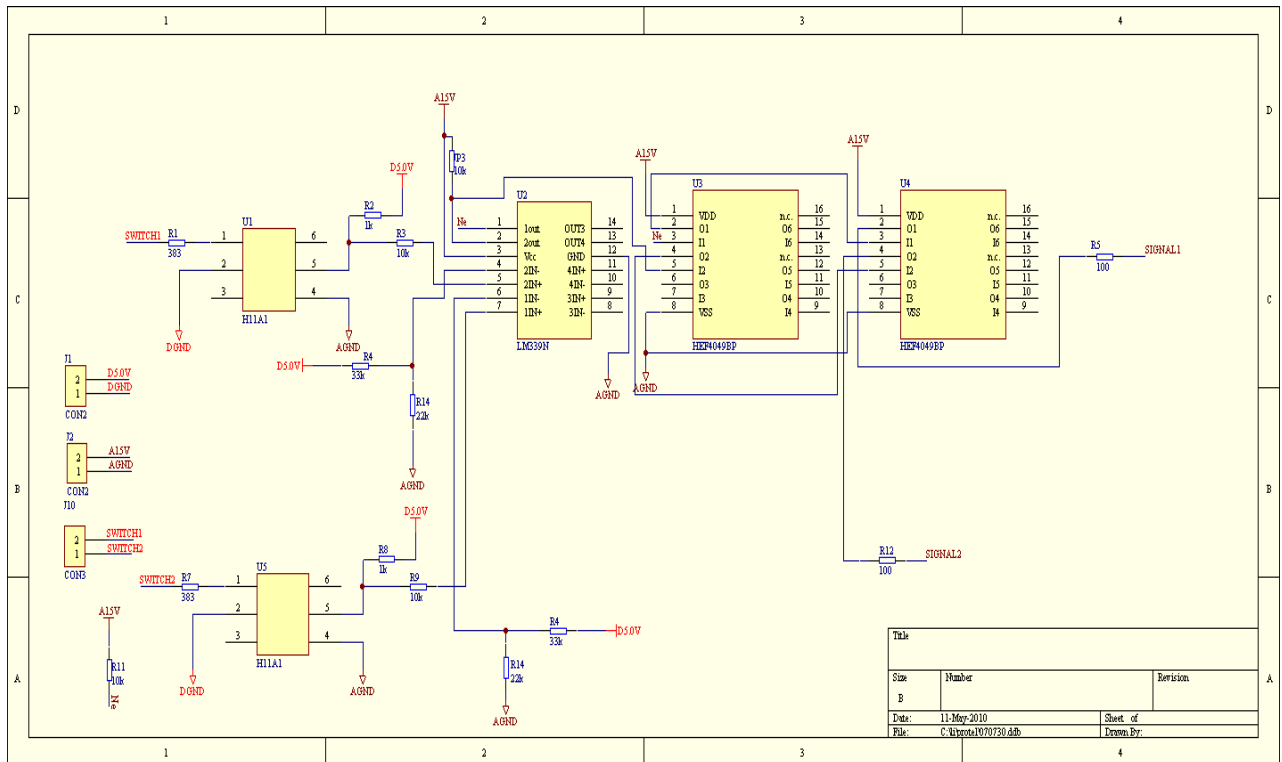
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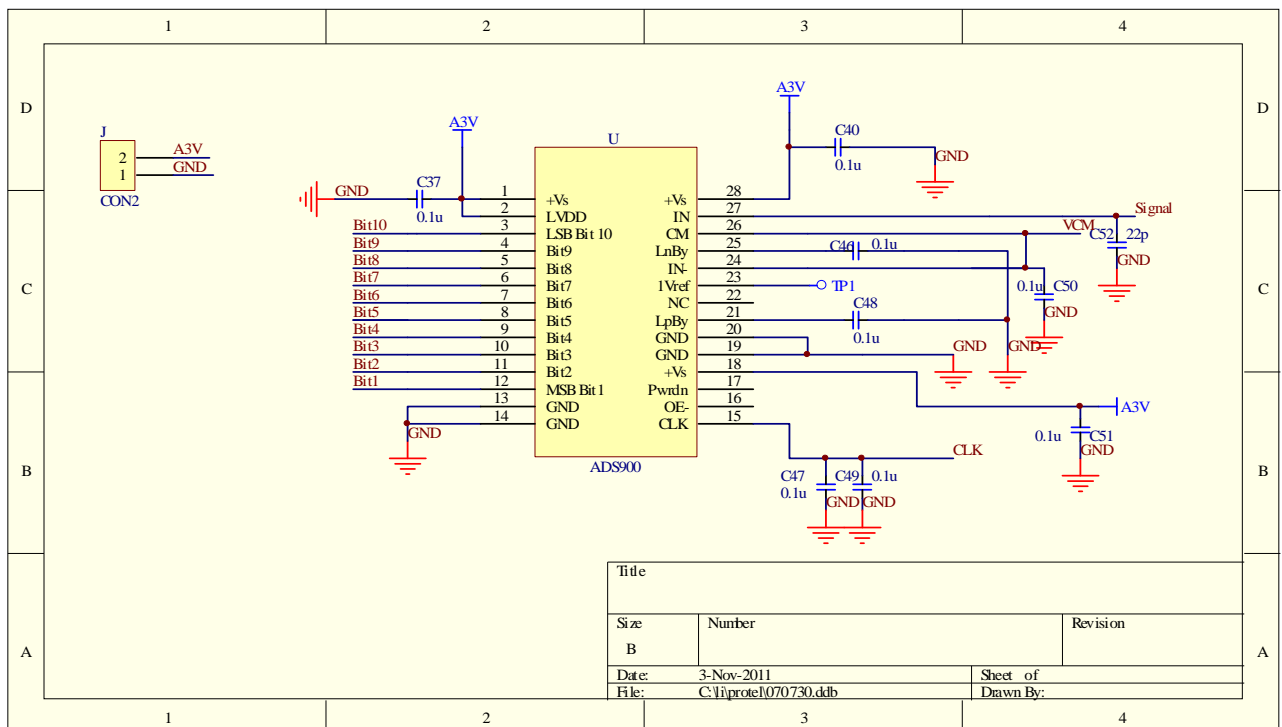
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APPENDIX

Appendix A: Schematic of Drive Circuit for Load Change



Appendix B: Schematic Circuit of A/D Converter



Appendix C: Calculation of Sallen-Key Parameters

Solving for the generalized transfer function from the block analysis gives:

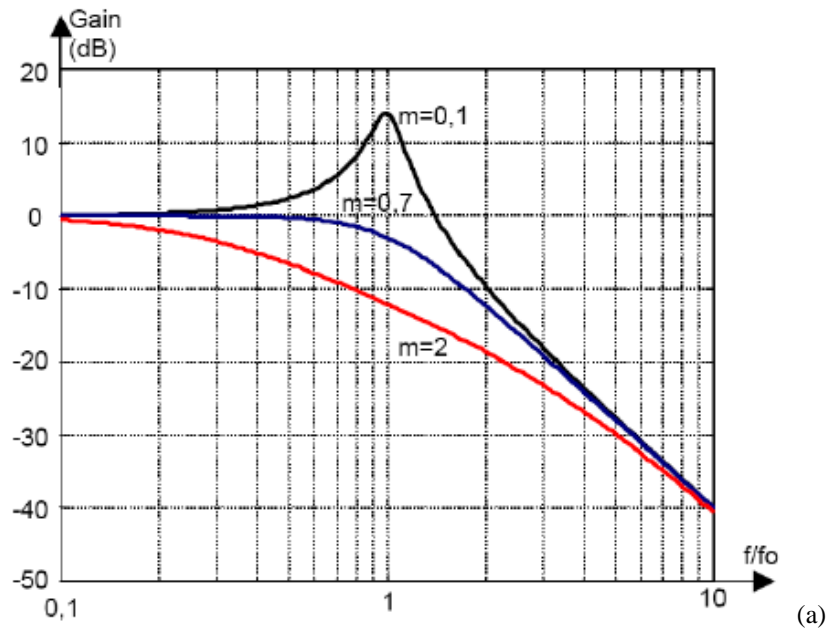
$$\frac{S1}{E1} = \frac{K}{1 + (R_1C_1 + R_2C_2 + R_1C_2(1-K))jw + (R_1R_2C_1C_2)(jw)^2} \quad (C.1)$$

With $w = 2\pi f$, $f_c = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$ and $Q = \frac{\sqrt{R_1R_2C_1C_2}}{R_1C_1 + R_2C_1 + R_1C_2(1-K)}$

Q is defined as the coefficient of quality.

According to the application of simplification of Sallen-Key, $R_1 = mR$, $R_2 = R$ and $C_1 = C_2 = C$.

Through the simulation and calculation of the second-order Sallen-Key, as shown in the Fig. C-1, if one wants a quick phase rotation, it will exceed the gain curve (where $m=0.1$), and if we want a gain curve without exceeding this, it will generate a slow phase rotation (where $m=2$). The second-order filters result in a trade-off between the phase and gain by choosing a good damping coefficient. We can make a trade-off between a phase rotation more or less rapid and a curve with a very low overrun. The trade-off is found by choosing a damping coefficient, $m=0.7$.



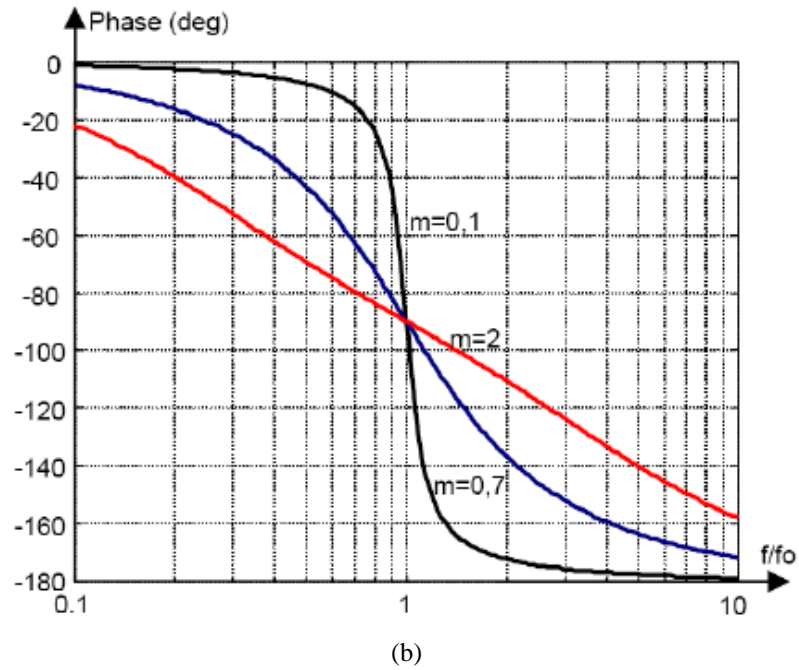


Fig. C-1 Bode plot of a second order system (a) comparison of gain response (b) comparison of phase response

We start by choosing $K=1$ to set the gain and $Q=0.67(m=0.7)$, and choose $R_1=1.6k\Omega$, $R_2=2.4k\Omega$. An appropriate bandwidth finally gives $C=1nF$.

FOLIO ADMINISTRATIF

THESE SOUTENUE DEVANT L'INSTITUT NATIONAL DES SCIENCES APPLIQUEES DE LYON

NOM : LI

DATE de SOUTENANCE : 29/05/12

(avec précision du nom de jeune fille, le cas échéant)

Prénoms : Nan

TITRE : Stratégies de Commande Numérique pour un Convertisseur DC/DC SEPIC en vue de l'Intégration

NATURE : Doctorat

Numéro d'ordre :

Ecole doctorale : E.E.A.

Spécialité : Electronique de puissance et Automatique

RESUME :

L'utilisation des alimentations à découpage (SMPSs : switched mode power supplies) est à présent largement répandue dans des systèmes embarqués en raison de leur rendement. Les exigences technologiques de ces systèmes nécessitent simultanément une très bonne régulation de tension et une forte compacité des composants. SEPIC (Single-Ended Primary Inductor Converter) est un convertisseur à découpage DC/DC qui possède plusieurs avantages par rapport à d'autres convertisseurs de structure classique. Du fait de son ordre élevé et de sa forte non linéarité, il reste encore peu exploité. L'objectif de ce travail est d'une part le développement des stratégies de commande performantes pour un convertisseur SEPIC et d'autre part l'implémentation efficace des algorithmes de commande développés pour des applications embarquées (FPGA, ASIC) où les contraintes de surface silicium et le facteur de réduction des pertes sont importantes. Pour ce faire, deux commandes non linéaires et deux observateurs augmentés (observateurs d'état et de charge) sont exploités : une commande et un observateur fondés sur le principe de mode de glissement, une commande prédictive et un observateur de Kalman étendu. L'implémentation des deux lois de commande et l'observateur de Kalman étendu sont implémentés sur FPGA. Une modulation de largeur d'impulsion (MLI) numérique à 11-bit de résolution a été développée en associant une technique de modulation Δ - Σ de 4-bit, un DCM (Digital Clock Management) segmenté et déphasé de 4-bit, et un compteur-comparateur de 3-bit. L'ensemble des approches proposées sont validées expérimentalement et constitue une bonne base pour l'intégration des convertisseurs à découpage dans les alimentations embarquées.

MOTS-CLES : Convertisseurs DC-DC, SEPIC, Commande par mode de glissement, Commande prédictive, Observateur Kalman étendu, FPGA, MLI numérique

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