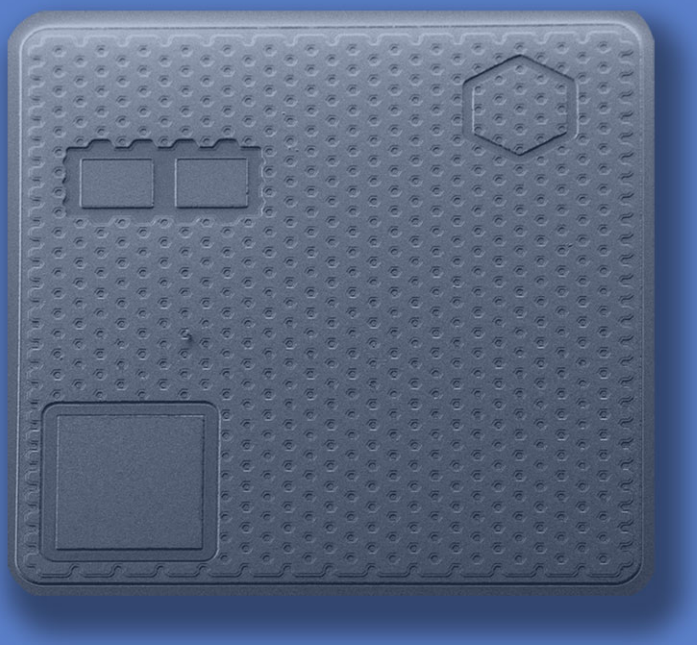
Implementation of high voltage Silicon Carbide rectifiers and switches

Maxime Berthou



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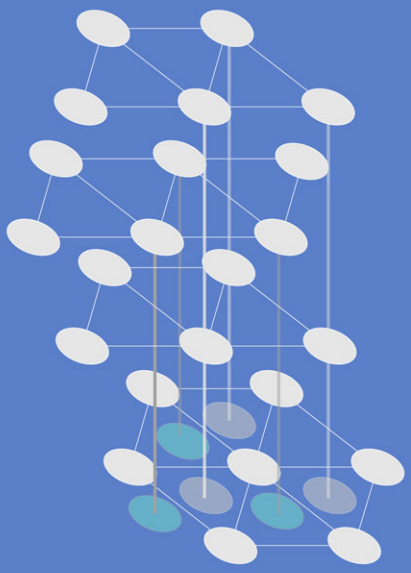

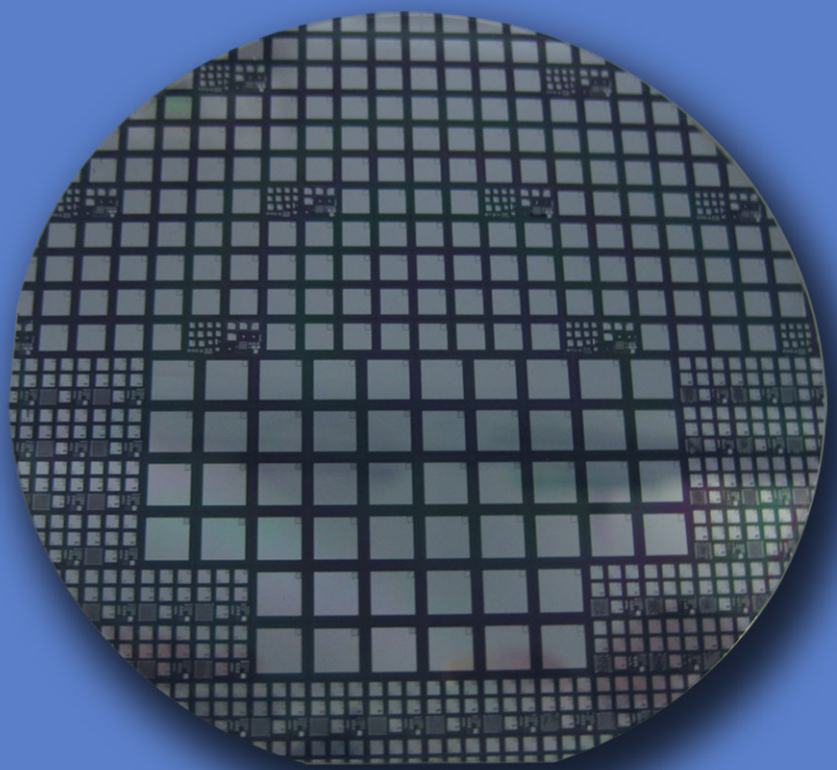

Maxime Berthou

Nº 2012ISAL0008

Thesis

Implementation of High Voltage Silicon Carbide Rectifiers and Switches

Presented before

Institut National des Sciences Appliquées de Lyon

To obtain

the grade of doctor

Doctoral Formation : Energy and Systems

Doctoral School of Electronic, Electrotechnic and Automatic of Lyon

Author :

Maxime Berthou

Submited to the examining board on January 18th 2012

Jury MM.

Pierre Brosselard	Laboratoire Ampère (Lyon)	Examiner
Frédéric Morancho	LASS (Toulouse)	President and Reviewer
Philip Mawby	University of Warwick	Reviewer
Michel Mermet-Guyennet	Alstom transport (Tarbes)	Examiner
Dominique Planson	Laboratoire Ampère (Lyon)	Supervisor
Philippe Godignon	CNM (Barcelona)	Supervisor

Acknowledgments

This work is the result of a collaboration between Alstom Transport, the Ampère Laboratory of Lyon and the Centro Nacional de Microelectrónica (CNM) de Barcelona.

It has been greatly supported by ALSTOM transport through the PEARL laboratory.

It also has been supported by Spanish ministry of Science and Technology with the RUE-consolider grant and SMART-PM project, and all the fabrication and design work has been performed at CNM of Barcelona.

First and foremost, I would like to thank Dr. Dominique Planson, Dr. Pierre Brosselard, Dr. Philippe Godignon, Dr. Michel Mermet-Guyennet for giving me the opportunity to work on such a technological turning point for power electronics, to trust me, and dedicate their time and knowledge allowing me to assume such a challenging project.

As the experiments have been performed in different laboratories, I have met many great people which I would like to thank for their help and welcoming.

All the power group of CNM and especially Dr. Aurore Constant for her valued collaboration and exchanges, Dr. Marcel Placidi, Dr. Xavier Perpiña, Dr. Ignasi Cortes, nearly Dr. Pablo Fernandez and Dr. Christian Caramel whose knowledge on semiconductor physics was precious as was their camaraderie, Dr. Xavier Jorda and Viorel Banu which taught me a lot on the packaging and measurement techniques.

As a large part of this project was dedicated to fabricate chips for the PEARL laboratory (Alstom Transport), I spent some time and worked with people of the laboratory. I would like to thank them all for their warm welcoming and sharing with me their point of view on my work, permitting me to broaden mine. I would also like to thank specially Dr. Selim Dagdag, Philippe Lasserre and Dr. Michel Mermet-Guyennet for their support and encouragements.

Exceptional measurements at very high voltage and high temperature were performed at the Institut franco alemand de recherches Saint-Louis (ISL) thanks to Pierre Brosselard, Sigo Scharnholz and Bertrand Vergne.

And Finally, I would like to thanks the power team of the Laboratoire Ampère in Lyon and in particular Dr. Pierre Brosselard, Dr. Dominique Planson, Dr. Dominique Tournier, Dr. Nicolas Dheily, and Florian Chevalier for their tremendous support from a scientific point of view as well as on the personal one.

Résumé

Cette étude a permis d'explorer de nombreux aspects des composants en Carbure de Silicium depuis leur conception en passant par la fabrication, jusqu'à leur caractérisation. Les travaux menés précédemment dans le cadre du projet européen ESCAPEE et d'autres collaborations ont servi de point de départ pour ce travail.

Notre objectif était de réaliser des transistors VMOS de puissance et diodes Schottky de très haute tension. Nous avons tout d'abord étudié les différentes structures via leur simulation, pour ensuite choisir les dimensions appropriées pour leur réalisation. La simulation des différentes terminaisons planaires nous a permis d'évaluer les qualités et défauts de chacune et de mettre au point une nouvelle terminaison combinant JTE, anneaux de garde dans la JTE (AGR) et anneaux de JTE. Comparée à la JTE classique, cette nouvelle protection montre une meilleure tolérance vis-à-vis de la dose de la JTE, une tenue en tension supérieure et une réduction du champ électrique en divers points sensibles de la terminaison. De plus, la création d'anneaux de JTE ne requièrt pas d'étape de fabrication supplémentaire.

Nous avons aussi étudié l'architecture du VIEMOS par simulation. Bien que sa fabrication eut échoué, cela nous a apporté une meilleure connaissance des particularités du VMOS en SiC qui furent précieuses lors de la conception des VDMOS. Notre premier succès fut la réalisation des diodes unipolaires de très haute tension. Précédemment, l'emploi du tungstène comme metal Schottky nous avait permis de réduire la sensibilité de la barrière Schottky vis-à-vis de la température. L'emploi de la nouvelle terminaison, combinée avec cette nouvelle barrière Schottky a ensuite permis de fabriquer des diodes de très haute tension (>3,5kV). Plusieurs lots de diodes unipolaires de type Schottky pure (SBD) et combinant jonctions bipolaires et Schottky (JBS) furent réalisés. Les composants d'une taille d'environ 4mm^2 permettent de conduire plusieurs ampères et de bloquer jusqu'à 9kV.

En plus des caractéristiques statiques, nous avons mesuré les caractéristiques des diodes de 1,5kV et 6,5kV en commutation et en surcharge de courant. Les diodes JBS de 1,5kV ont montré des caractéristiques en commutation similaires aux diodes Schottky jusqu'a 200°C, avec un courant de pic maximum supérieur et des courants de fuite inférieurs de plusieurs ordres de grandeur.

Les diodes en SiC atteignent, sur une gamme de température plus élevée, des performances en commutation largement supérieures aux composants en Silicium actuels ou aux composants bipolaires en SiC, permettant ainsi d'augmenter les fréquences de commutation des convertisseurs, leur température de fonctionnement et d'augmenter leur rendement.

Les systèmes de conversion ont toutefois besoin d'employer des interrupteurs de puissance présentant les mêmes qualités que les diodes SiC pour exploiter totalement leurs avantages. Grâce à la similitude de fonctionnement du SiC-VMOS avec le Si-IGBT, la substitution est aisée, toutefois la fabrication du VDMOS reste complexe et maitrisée par peu de groupes. De plus, la qualité actuelle des composants permet rarement d'envisager son industrialisation. Le principal frein au développement du VMOS en SiC vient de la faible qualité du canal du MOS, entrainant une augmentation importante de la résistance du canal et de sa dégradation. Les récents progrès dans la formation de l'oxyde de grille ont permis de le rendre plus stable mais sa mobilité reste faible.

Les échantillons de VDMOS précédemment réalisés lors du programme ESCAPEE présentaient différents défauts de fabrication et une mobilité dans le canal très faible. Trois nouveaux lots de VDMOS furent réalisés, dans lesquels la majorité des défauts de fabrication furent éliminés via l'amélioration de leur procédé de fabrication. Nous avons aussi employé un nouvel oxyde de grille de meilleure qualité, réduit la longueur du canal et augmenté son degré d'intégration, ainsi nous avons réduit la contribution du canal à la résistance totale des VDMOS.

La fabrication du canal du VDMOS via la méthode d'alignement classique ne permet pas de créer des canaux de longueur inferieur au micron, c'est pourquoi nous avons mis au point une technique d'auto-alignement du canal en SiC. Cela a conduit à diviser par dix la résistance des composants et nous permettra de réaliser des VDMOS capables d'exploiter le potentiel du SiC.

Bien que la résistance de nos VDMOS classiques reste trop importante pour être comparable aux IGBT en Silicium et qu'il faille encore résoudre quelques problèmes de fabrication, grâce à nos progrès nous avons fabriqué des composants de grande taille, intégrant des capteurs de courant et de température.

Différents composants unipolaires de grande taille en carbure de silicium furent réalisés avec succès après une étude de modélisation précise, de nombreuses améliorations du procédé de fabrication et du design. Les diodes JBS employant la barrière Schottky en tungstène ont montré des caractéristiques exceptionnelles. La résolution du nombre réduit de problèmes lors de la fabrication des VDMOS en SiC, nous permettra d'exploiter pleinement le potentiel du SiC en électronique de puissance.

Abstract

This work is dedicated to the study of SiC potential for the implementation of high voltages SiC rectifiers and switches for traction and energy distribution applications. Previous work done in the framework of European project ESCAPEE and other collaboration between the partners served as starting point of this work.

The junction barrier Schottky diode and the transistor MOSFET studied in this work are unipolar semiconductor devices ; they allow attaining far superior switching frequencies and lower commutation losses compared to Si and SiC bipolar devices. They both present several technological issues ; the commonly used Schottky barriers shows high leakage current and temperature instability, and the mobility of the MOS channel is very low due to its poor interface quality. The improvement of this channel mobility passes through the improvement of the gate dielectric but also on the improvement of the MOSFET design and full technology process. The high voltage capability is also an issue since SiC devices have a large potential for novel applications in the high and very high voltage range applications (>3.5kV). Novel design and technological solutions must be found to be able to implement such large voltage capability.

I will present the state of the art on unipolar SiC devices and some aspects of the SiC technology. Then, we will see simulation investigations performed to conceive innovative high voltage terminations usable both for diodes and transistors. We will also present the modeling and optimization of the VIEMOS device concept, intended later. In the third part are presented the different high voltage Schottky and JBS diodes designed, fabricated and characterized during this work. We investigated a new Schottky metal, and several innovative designs modeled in chapter 2 for the active region and the termination. An analysis and comparison of the different designs and technological tested solutions is done for devices up to 9kV. Finally, I will present the experimental work done on the VMOS devices, where we used innovative designs, refined the fabrication process and increased the devices' size. Three different technologies are proposed and tested.

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Introduction

Next generation of the power electronic devices will see the Silicon Carbide (SiC) components as a revolution. Silicon devices are reaching their physical limits and will not be able to improve further. Several semiconductors with superior properties are being investigated in order to reduce the losses during the electricity's transformation operated during its life cycle.

Silicon Carbide is the most eco-friendly and viable candidate due to the abundance of Si and C on earth, their low toxicity character and the native oxide on SiC. Moreover, its electrical properties make it an ideal semiconductor to produce high voltage devices with lower static losses, higher blocking capabilities, higher switching frequency, higher thermal conductivity and higher thermal stability.

Such devices allow building smaller solid state converters by reducing the cooling system and the passive components. They will also allow working at superior voltage, and thus simplify and increase the efficiency of the transformation systems at high voltage.

The electric vehicles and energy management like the smart-grid are thriving for such technology. On electric vehicles it will essentially allow suppressing the dedicated cooling system for the converters. On the smart-grid, it will permit to reduce the transformation losses at its nodes.

This work is resulting from the collaboration between the Alstom company and the research laboratories Centro Nacional de Microelectrónica de Barcelona in Spain and the Laboratory Ampère in Lyon France. The objective was the study of SiC potential for the implementation of high voltages SiC rectifiers and switches for traction and energy distribution applications. Previous work done in the framework of European project ESCAPEE and other collaboration between the partners served as starting point of this work.

The junction barrier Schottky diode and the MOSFET studied in this work are unipolar semiconductor devices ; they allow attaining far superior switching frequencies and lower commutation losses compared to Si and SiC bipolar devices. Moreover, they will replace the Si devices most easily in the current power electronic systems. The MOSFET integration is also a step toward the realization of the IGBT on SiC.

Both devices present several technological issues ; the commonly used Schottky barriers show high leakage current and temperature instability, and the mobility of the MOS channel is very low due to its poor interface quality. The improvement of this channel mobility passes through the improvement of the gate's dielectric.

The low mobility in the channel increases the channel's resistance contribution to the VDMOS, which can also be reduced by improving the channel integration using a better

MOSFET design and technology process. The high voltage capability is also an issue since SiC devices have a large potential for novel applications in the high and very high voltage range applications (> 3.5kV). Novel design and technological solutions must be found to be able to implement such large voltage capability.

In the first part of this work, I will present the state of the art on unipolar SiC devices and some aspects of the SiC technology. Then, we will see simulation investigations performed to conceive innovative high voltage terminations usable both for diodes and transistors. We will also present the modeling and optimization of the VIEMOS device concept, intended later. In the third part are presented the different high voltage Schottky and JBS diodes designed, fabricated and characterized during this work. We investigated a new Schottky metal, and several innovative designs modeled in chapter 2 for the active region and the termination. An analysis and comparison of the different designs and technological tested solutions is done for devices up to 9kV. Finally, I will present the experimental work done on the VMOS devices, where we used innovative designs, refined the fabrication process and increased the devices' size. Three different technologies are proposed and tested.

Chapitre 1

State of the art

1.1 Introduction

Economic and environmental motivations have pushed countries and companies to look forward to an efficient production, transport and consumption of the electrical energy. During the different stages of its life, the electricity is transformed to different voltages, currents and waveforms.

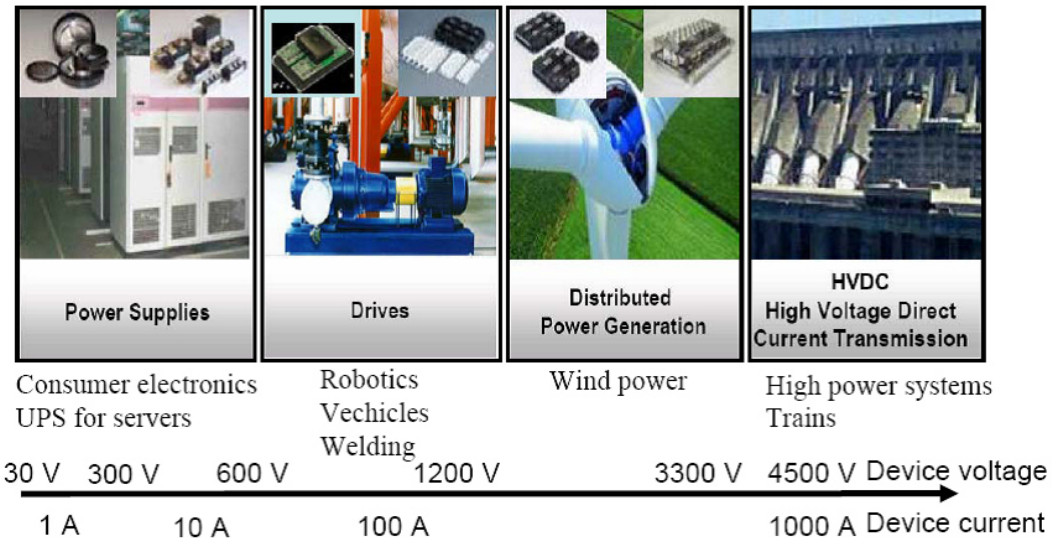

Figure 1.1 – Applications of the power devices [1]

For example, in railways the electricity in transportation lines is at 10kV AC and converted down to 3kV AC or DC for the engines or 220 V AC for domestic use. The figure 1.1 shows the different high voltages appliances ordered by magnitude of the voltage used.

Converters are necessary to perform the conversion to different voltages ; their efficiency will determine the energy losses during the conversion. Up to 10 kV, the conversion can be performed with solid state converter, for the most modern ones, it is composed of Silicon PiN diodes and IGBTs [2] as shown in 1.2.

The energy conversion always generates losses, for example last generation inverter shows efficiency up to 98 % and many HV converters around the world are still very old models with efficiency under 90 %. Energy lost during the conversion is mostly dissipated

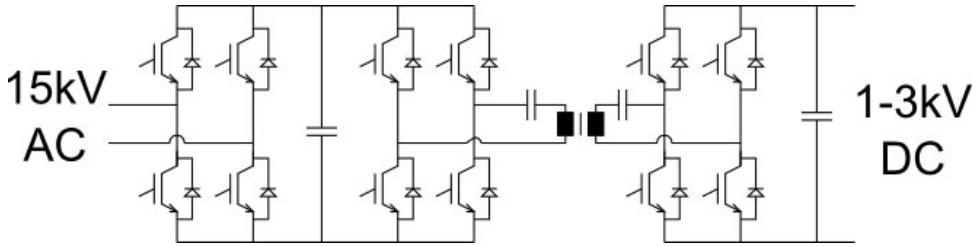

FIGURE 1.2 – Electronic schematic of a high voltage solid-state converter for railways application [2]

thermally, thus requiring cooling systems proportional to the losses and the operating temperature of the devices. Nowadays, the converters size is limited by the losses generated by Si IGBTs and diodes. The Silicon power devices have reached their limit and only optimization can be expected with this technology.

Thanks to the Silicon Carbide (SiC) superior semiconductor properties SiC power devices show far superior characteristics than equivalent Si components. The replacement of conventional Si chips in converters by SiC chips will permit to increase their efficiency, maximum voltage, operating temperature and frequency. Increase of the frequency will permit to reduce the size of passive elements. Lower losses imply less self heating, as the operating temperature capability increase, it will also permit to greatly reduce the cooling system.

The lower size, weight and cooling arguments make it very seducing for transportation applications like trains, tramway and electric cars. In hybrid vehicles, the low operating temperature of Si inverters implies the presence of two cooling system ; one for the thermal and one for the electric engine. Full SiC converters are capable to operate at the same temperature as the thermal engine ; only one cooling system will be required.

1.2 SiC Physical properties

The table 1 compares the main physical properties of Silicon the most commonly used wide bandgap semiconductors. An important property for a semiconductor is the value of the gap between the valence and conduction bands. From this value especially depends the quantity of intrinsic carriers generated thermally ; these are at the origin of the natural leakage current in electronic chips. The larger is the band-gap, the more energy is necessary to transfer an electron from the valence band to the conduction band.

So the large bandgap semiconductors like SiC will present lower intrinsic carriers concentration for the same or superior temperature. In addition, the strong Si-C energy link (5eV) gives to the SiC crystal a refractory character making it chemically stable at high temperature, resistant to radiations, and to corrosion. However, this chemical strength makes it difficult to chemically transform at temperatures used in Si technology during the process (Ohmic contacts formation, oxidation, doping and etching).

One can see in table 1.1 that the 4H-SiC has one of the largest bandgap just behind GaN and Diamond. Diamond is incontestably the best theoretical candidate as a semiconductor. However, its chemical strength and density makes him even more difficult to synthesize and process than Silicon Carbide. The GaN is currently one of the concurrent of SiC. The possibility of growing it on Silicon wafers makes it a seducing alternative for producing lateral structures at lower cost, and nowadays many efforts are put in developing it. However, regarding power devices, the lateral structure limits the GaN possibilities to devices with blocking voltage under 1.5kV.

Property	Unit	Si	3C-SiC	6H-SiC	4H-SiC	GaN	Diamond
E_g	eV	1.11	2.3	2.9	3.2	3.4	5.45
ϵ	ϵ_0	11.8	9.6	9.7	9.7	8.9	5.5
E_c	MV·cm^{-1}	0.6	2	2.4	2.2	3.3	2.7
V_S	cm/s	10^7	$2 \cdot 10^7$	$2.5 \cdot 10^7$	$2 \cdot 10^7$	$2.5 \cdot 10^7$	$2.7 \cdot 10^7$
μ_{B-e}	cm^2/Vs	1350	750	340	950	1000	1900
μ_{B-h}	cm^2/Vs	450	40	120	120	30	1600
K	W/cm·°K	1.5	3.2	4.9	3.7	1.3	22
N_i (25°C)	6.9	$2.3 \cdot 10^{-6}$	cm^{-3}	$1.5 \cdot 10^{10}$	$8.2 \cdot 10^{-9}$	$1.6 \cdot 10^{-10}$	$1.6 \cdot 10^{-27}$
T_m	°K	1690	3100	3100	3100	1800	4270
BFM	BFM_{Si}	1.0	20.6	16.6	34.7	123	128
JFM	WΩs^2	9		2533	4410	15670	73856
KFM	Wcm^{-1}s^{-1}°C	13.8		90.3	229	118	101

TABLE 1.1 – Important properties for power devices of wide bangap semiconductors [14] compared to Silicon

Silicon Carbide exceptional thermal conductivity (compared with Si and GaN), even higher to the copper's, permits to evacuate efficiently the heat generated by electronic devices, limiting thermal runaway of components. Moreover, its chemical stability in

temperature coupled to the high temperature conductivity, makes the chips even more resistant to destruction via hot spots.

Figure of Merit	Definition	Relevance
Johnson's (JFM) [16]	$\frac{{E_C}^2 \nu_S}{4\pi^2}$	High Frequency Power capability
Keyes' (KFM) [17]	$\lambda\sqrt{\frac{C_0 \nu_S}{4\pi\epsilon_S}}$	Switching speed Thermal limitation
Baliga's (BFM) [18]	$\epsilon_0 \mu {E_C}^3$	Low Frequency static losses
Baliga's High Freq. (BHFM) [19]	$\mu {E_C}^2$	High Frequency Switching losses

TABLE 1.2 – Summary of the different semiconductor Figures Of Merit (FOM)

The values of typical figures of merit are shown in the three last lines of 1.1, the detail explanation of each figure of merit being summarized in table 1.2. Recent technological breakthroughs and improvement of the Silicon Carbide quality have permitted to reach a material maturity sufficient for industrialization of cutting edge devices. However, the unique character of the high temperature equipments needed to grow and process the SiC wafers, make both the raw material and the device production more than ten times more expensive than on Silicon.

1.3 Vertical SiC Power Devices

The vertical power devices are composed of two parts : the top one creates the function and the bottom one called the drift layer permits to spread the equipotential lines when the chip is blocked and induces the majority of the chip's resistance. In order to reach higher breakdown voltage (V_{BR}), one must increase the drift layer's thickness and lower its doping level. With Si, building device with high voltage blocking capability above 1.2kV requires thick drift layers with very low doping inducing a major resistance. Using bipolar devices as IGBTs and PiN diodes permits to reduce the static losses but increases the losses during the commutation. For devices with a given forward current and blocking voltage, compared to Si, the superior critical field of SiC permits to use a far thinner drift layer of higher doping concentration and thus greatly reduces the drift resistance's contribution. Thanks to their simplicity and low sensibility to crystal defects, the unipolar rectifiers were the first SiC power devices commercialized. However their performance and reliability can still be improved.

1.3.1 Rectifiers

Progress on SiC technology have permitted to produce SiC rectifiers of large active area up to 0.5cm^2 [20] and breakdown voltage up to 10kV for unipolar devices and 19kV for PiN diodes. The figure 1.3 shows the different notable devices of large area fabricated in the past decade compared to the theoretical unipolar limit of the SiC and Si. It shows that we are already far from the unipolar Si limit and can still ameliorate the performance of unipolar devices with highest blocking capability.

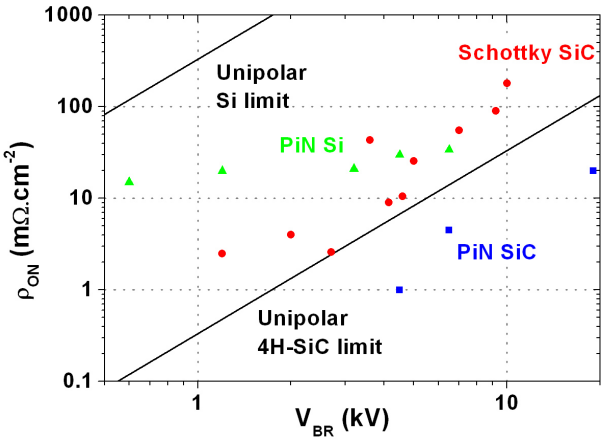

FIGURE 1.3 – Position of the state of the art SiC power diodes on the ρ_{ON} vs V_{BR} graph

Schottky and Junction Barrier Schottky diodes (JBS) made on 4H-SiC have been introduced in the market during the last decade, various companies are now commercializing SiC rectifiers with a blocking voltage up to 1.7kV. The different SiC rectifiers

Company	V_{BR}	I_F
Cree	600V	1-20A
	1200V	5-20A
	1700V	10-25A
Infineon	600V	2-16A
	1200V	2-15A
RHOM	600V	6-20A
	1200V	5-20A
Microsemi	600V	5-50A
	1200V	5-50A
Semisouth	1200V	5-30A
ST Microelectronics	600V	4-12A

TABLE 1.3 – Commercial availability of HV SiC SBD in 2011

commercialized are presented in table 1.3. They are mostly used with Si IGBT to produce hybrid converters or as protective blocking diodes on photovoltaic applications. The coming out of the SiC VMOS will permit to fabricate full SiC converters.

1.3.1.1 Schottky Barrier Diode (SBD)

The figure 1.4 shows the vertical cut of a basic structure for the vertical Schottky diode, the barrier is created by the electronic interface between the contact metal and the semiconductor.

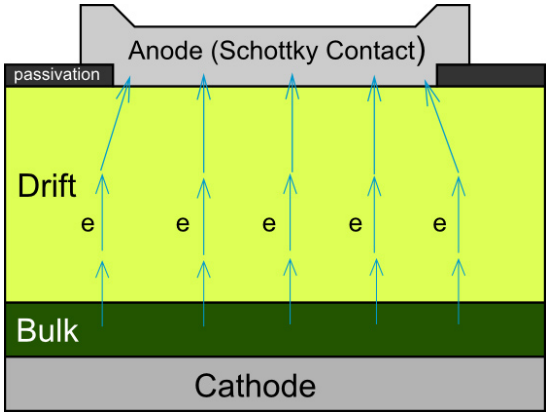

FIGURE 1.4 – Schematic view of a Schottky diode's vertical cut

When contacted, the Fermi level of the metal and the semiconductor align, charges build up at the interface to equilibrate the system and create the barrier seen in figure 1.5a. When forward biased the barrier height is reduced and the current of electrons above the barrier via the thermionic emission [21, 22] increases.

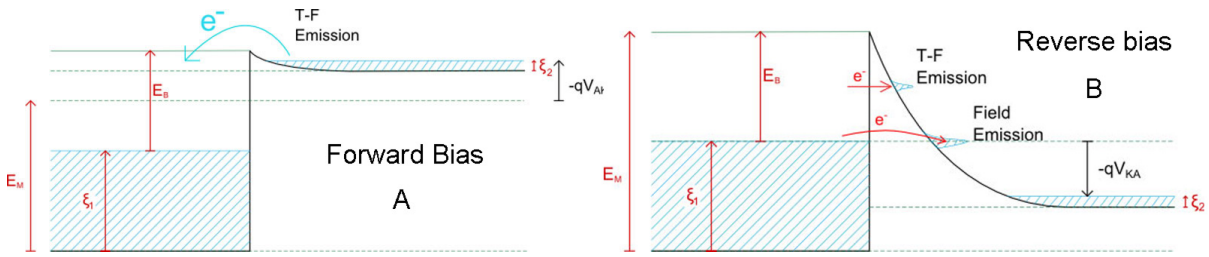

FIGURE 1.5 – Electronic structure of a Schottky contact on n-type semiconductor when forward biased (A) and reverse biased (B)

The expression of the forward current flowing through the Schottky barrier on n-type is given by equation 1.1 ; where A^{**} is the Richardson constant, N_d is the density of ionized donor in the semiconductor, N_c is the density of the states in the conduction band, Φ_B is the barrier height given by $e\Phi_B = q\Phi_M - q\chi$ where Φ_M is the metal work function and χ is the electron affinity of the semiconductor and V_d is the polarization of the barrier.

$$J = A^{**}T^2\frac{N_d}{N_c}exp(-\frac{e\Phi_B}{k_BT}(exp(\frac{eV_d}{k_BT}) - 1)) \tag{1.1}$$

As the temperature increases, the electron mobility in the drift layer decreases, so the contribution of the drift to the global resistance increases. Thanks to the combined

conduction mechanisms through the Schottky barrier and the drift layer we obtain diodes with lower forward voltage than PiN diodes and positive temperature coefficient as shown in figure 1.6. The increase of the device resistance with the temperature prevents thermal runaway and eases the parallelization of the chips in power modules.

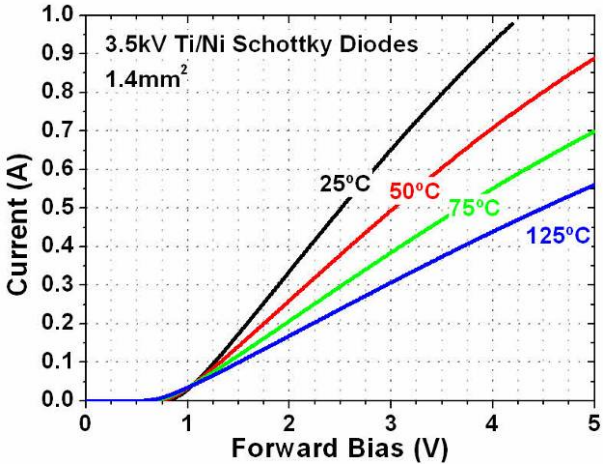

FIGURE 1.6 – Forward I-V characteristics of a 3.5kV Ti-Ni/4H-SIC Schottky diode at different temperatures

In unipolar devices like SBD, the bipolar recombination mechanism is inexistent or quasi inexistent, so the degradation phenomenon seen on bipolar devices does not occur. Moreover the unipolar nature of their conduction guarantees extremely low and temperature independent dynamic losses as shown in figure 1.7.

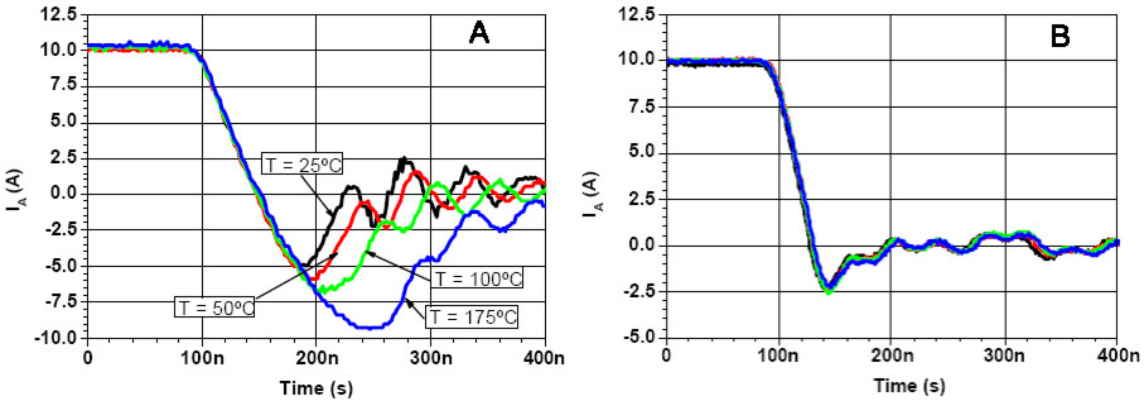

FIGURE 1.7 – Turn-off current waveforms of (a) a 1.2kV Si-PiN diode (A) and a 1.2kV SiC Schottky diode (B) at different temperatures, pictures from [3]

The height of the Schottky barrier is determined by the difference between the electron affinity of the semiconductor and the metal work function. The smaller value of the electron affinity in Silicon Carbide (3.2eV [23]) compared to Silicon (4.05 eV) permits to obtain higher Schottky barrier. The Schottky barrier height will determine the forward

voltage but also the reverse leakage current through it. Its superior value on SiC allows the fabrication of diodes capable of blocking several thousand of volts at high temperatures ; up to 10 kV Schottky diodes have been demonstrated in 2004 [24] and we obtained up to 9kV Schottky diodes during this work.

Metal	Ti	Mo	W	Ag	Ta	Ni	Au	Pt
Φ_M (eV)	3.85	4.15	4.32-5.22	4.52-4.74	4-4.8	5.25	5.1-5.47	5.12-5.93

TABLE 1.4 – Work functions of metal usable as Schottky contact on SiC

The table 1.4 shows the work functions of several metals classically used in microelectronic. On SiC, the Schottky contact is usually made with Ni, Ti, W or Mo. Each one of them exhibits a different barrier and interface chemistry. An elevated barrier is required to limit the reverse leakage current, so Ni is theoretically the best candidates. However, the formation of NiSi at the interface, at high temperatures lowers the barrier height and can create leaky devices. So, special care during the surface preparation and annealing must be taken.

In addition to micropipes, recent studies have shown that crystal defects such as stacking faults and TSD increase the reverse current leaks at the Schottky barrier [25]. Many efforts are still devoted to the identification of defects susceptible to deteriorate the Schottky diodes characteristics and reliability [26] as we will see in the part devoted to the crystal defects.

The Schottky diode presents two disadvantages compared to the PiN diode ; its lower conductivity and superior reverse leakage current. The first is inherent to the unipolar character of the conduction in the SBD but the last can be reduced by using a more complex design as the JBS.

1.3.1.2 Junction Barrier Schottky diode (JBS)

To exploit Schottky diodes' unipolar conduction advantages and push the critical electric field far from the surface like in PiN diodes, Baliga invented the JBS diode [27]. Introducing a diode with small areas of Schottky contacts protected by PiN areas when reverse biased. Ideally the conduction through PiN junctions is not triggered and the conduction is always unipolar. The electrons coming from the drift pass between the P boxes and evacuate through the Schottky contacts as shown in figure 1.8. The anode metal connects the N and P areas, the contact must be Schottky on N-type and very resistive on P-type to impair the bipolar conduction.

If the diode design is made to exploit both the Schottky and bipolar conduction modes, we call it a merged PiN Schottky diode.

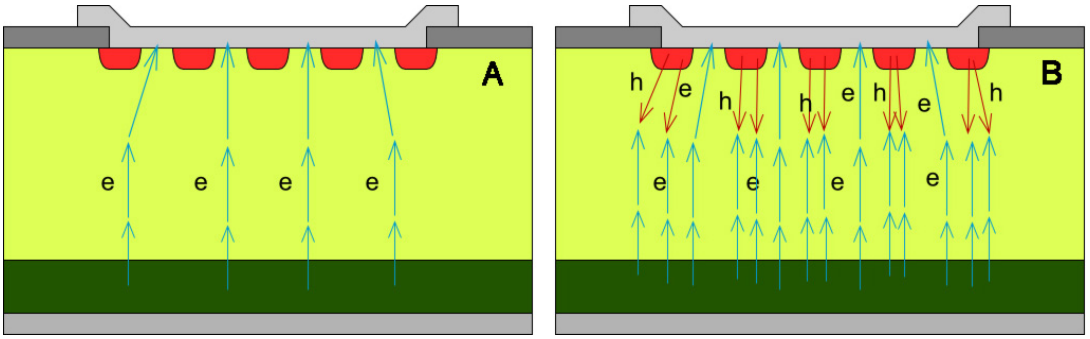

FIGURE 1.8 – Schematic view of JBS (A) and MPS (B) diodes operated at nominal current

When reverse biased, the area under the Schottky contact is screened by the depleted area from the P/N junctions. So the P grid keeps the crowding of equipotential lines in the crystal depth and consequently reduces the surface electric field. When the distance between the P boxes is sufficiently small, the critical electric field is pushed at the vertical P/N junction, in the crystal's depth [28]. The leakage current is mainly due to thermionic emission through the Schottky barrier, which is highly dependent on the electric field. So the JBS design reduces it by several orders of magnitude, as shown in figure 1.9.

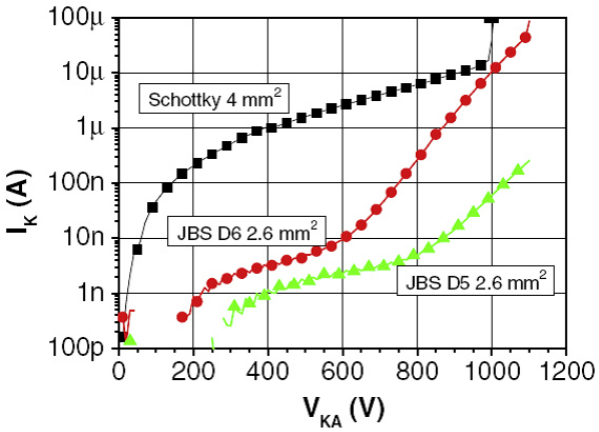

FIGURE 1.9 – Reverse characteristics of 1.2kV 4H-SiC Schottky and JBS diodes, picture from [4]

When forward biased the current flows between the p-wells and then spreads under them. So the device's can be vertically divided in three areas having different resistance contribution as shown in figure 1.10 ; the p-well layer, the spreading layer and the drift layer. The conduction in the p-well layer is rectilinear, so its resistivity can be computed from the depth, spacing and size of the p-type areas. Below, in the spreading layer, the current spreads under the P boxes, so the total resistivity depends on the spreading layer's length (W_S). This length depends on the size of the P boxes [20, 29] and the spreading angle α. In the last layer, the effective drift layer, the density and velocity of carriers

is uniform, so its resistivity can easily be calculated knowing its depth. Then, the total resistivity is not linearly proportional to the Schottky contact area and the JBS diode is only slightly more resistive than a Schottky diode with the same drift layer. However, its lower leakage current and increased reliability makes it a serious challenger for the future high voltage, high current, and fast switching diodes.

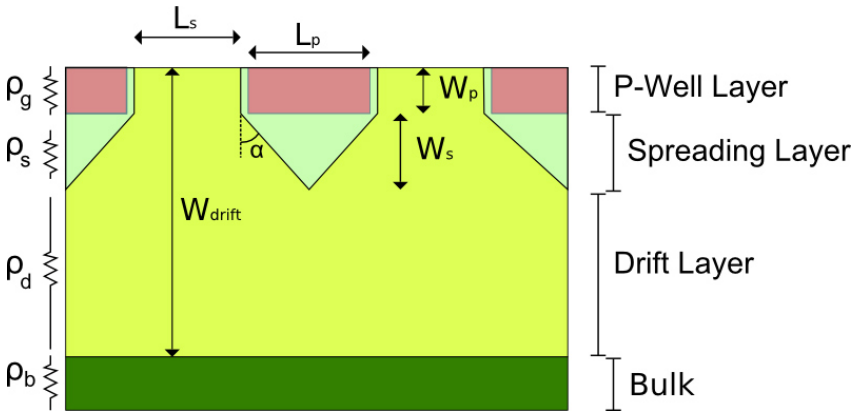

FIGURE 1.10 – Schematic view of a JBS diode' vertical cut in its active region with the equivalent resistances of the different regions

Optimization of the p grid dimensions and geometry permits to maximize the top layer conductivity and obtain devices with high BFOM (see table 1.2). Currently the highest breakdown voltage obtained for JBS diodes [20] reported is 10kV, with a specific resistance of 100mΩ.cm^2 for a leakage current of 5μA.cm^{-2} at 10kV.

The realization of contacts, creating at the same time a highly resistive contact on P with a good Schottky barrier on n-type, requires an adequate metal and process. However, it is possible to obtain a low resistive P contact so that one get a Schottky merged with a PiN diode ; this is the Merged PiN Schottky (MPS) diode [20]. As the JBS exhibits bipolar conduction at high forward bias or temperature, we will distinguish the MPS and the JBS by the following criterion : the MPS diode initiate the bipolar conduction before the nominal forward bias of the diode.

Like the PiN diode, the advantage of superior bipolar current density in MPS is also a disadvantage due to its slower dynamic behavior and bipolar degradation. The figure 1.11 show the degradation after forward bias after several hours of different SiC rectifiers (SBD, PiN and JBS), the JBS diode was operated like a MPS, in bipolar mode, so that we can observe the bipolar degradation. For the MPS diodes, the p-boxes are implanted so the defects created via the implantation increase the bipolar degradation phenomenon compared to fully epitaxied PiN diodes. So the bipolar capability of the JBS diodes is only interesting for surge current capability.

The table 1.5 summarizes the state of the art of these unipolar rectifiers in the literature. Such devices will be initially coupled with high voltage switches as shown in

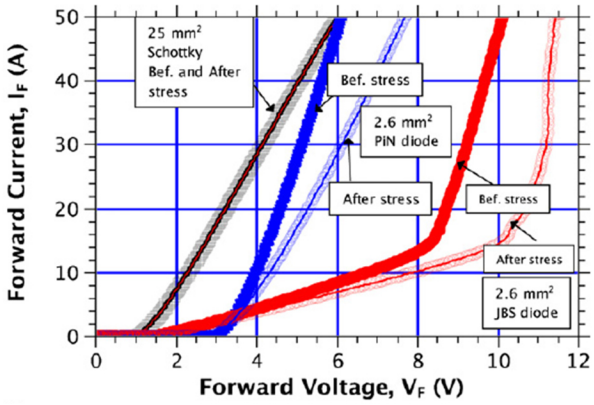

FIGURE 1.11 – Degradation of different types of 3.3kV diodes after stress, pictures from [5]

figure 1.2 with Si-IGBTs, reducing dynamic losses compared to Si PiN diodes. However, their full potential will be exploited when coupled with SiC devices.

Ref.	Type	V_{BR}	R_{ON} (mΩ.cm^2)	Affiliation
[30]	JBS	1.2kV		CNM
[31]	SBD	1.2kV	2.5	AIST
[32]	Super-SBD	2.7kV	2.57	Toshiba
[33]	JBS	2.8kV		ABB, KTH, ACREO
[29]	JBS	3.6kV	43	Kansay Elec. & Hitachi
[34]	SBD	4.15kV	9.07	Kansay Elec.
[35]	SBD	4.6kV	10.5	University of Nottingham
[36]	MPS	5.9kV	24	SiCLAB
[20]	JBS	10kV	180	Cree
[37]	SBD	10.8kV	97	SiCLAB
[38]	MPS	10kV	4mm^2 10V 2A	Cree

TABLE 1.5 – Performance of fabricated SBD, MPS and JBS diodes in the literature

1.3.1.3 SiC PiN Diodes

The SiC wide band-gap induces low intrinsic carrier concentration and higher electronic barrier, so the reverse leakage current of SiC PiN diodes is extremely low. Moreover, the critical electric field is situated at the P/N junction deep into the crystal, superior cohesion and temperature capabilities of the SiC crystal permit to obtain reversible breakdown on PiN junctions [39]. PiN diodes up to 19kV [40] have been fabricated until now.

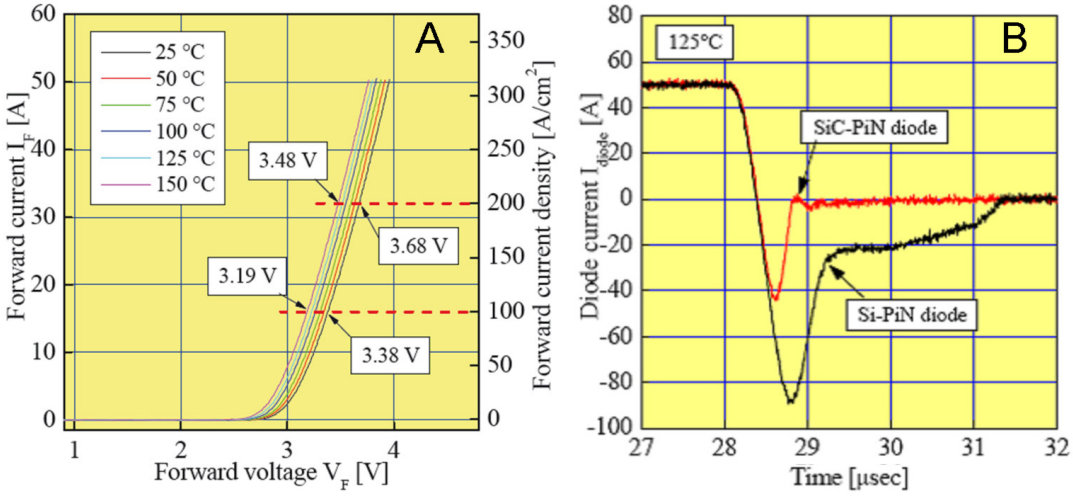

FIGURE 1.12 – (a) Forward I-V characteristics from room temperature up to 150°C of a 6kV 4H-SiC PiN diode and (b) turn-off current waveform at 125°C for the same diode, showing a recovery charge of 11μC, compared to a 6kV Si-PiN diode, showing a recovery charge of 83μC, pictures from [6]

The figure 1.12a shows forward characteristics of a 6kV PiN diode on 4H-SiC at different temperatures, the conduction is purely bipolar and increases with the temperature. The forward voltage (V_F) is related to the bandgap, so it is superior to the Si PiN diodes'. During the turn-off, shown in figure 1.12b, the carriers present in the drift must be removed to create the space charge region and completely block the conduction in the diode. Minority carriers are slow and their lifetime is superior to the electrons and increases with the temperature. So they take more time to evacuate and induce long charge storage delay, increasing with the temperature.

This recovery charges are at the origin of the commutation losses. On the SiC PiN diode, the drift layer and the active area are smaller, moreover the carrier lifetime is inferior, so there are less stored minority charges, which are evacuated faster. All this differences result in a lower recovery charge in SiC PiN diodes compared to Silicon PiN diodes.

In SiC, the recombination of carriers provides enough energy to help the propagation of basal plane dislocations (BPD) [44] and creation of stacking faults (SF) from them.

Ref.	V_{BR}	Forward Characteristics	Affiliation
[41]	3.3kV	3.2V 100A.cm^{-2}	CNM
[42]	4.5kV	3.2V 100A.cm^{-2}	Cree, Powerex
[6]	6kV	3.68V 100A.cm^{-2} (16 mm^2)	Toshiba
[43]	6.5kV	4.5mΩ.cm^2	SiCED, Siemens
[24]	10kV		Cree
[40]	19kV	4.4V 100A.cm^{-2}	Kansai Electric Power, Cree

TABLE 1.6 – Best fabricated SiC PiN diodes in the literature

These phenomena make PiN diodes and bipolar devices unreliable in the long term if the crystal presents BPD. So the production of reliable bipolar component requires limiting the creation of such defects during the fabrication process and screening the unreliable components via extensive preliminary tests.

Until now, progress in SiC growth was not sufficient to obtain yields high enough to make large bipolar devices commercially viable. Hopefully, recent progresses in epi-growth technology may change the situation [6]. The state of the art PiN diodes are shown in table 1.6, more details on the performances and recent progresses are shown in the associated articles.

1.3.2 Unipolar power switches

On SiC devices, the smaller drift layer's resistance permits to perform the same task with SiC-MOSFETs than Si-IGBTs. Unipolar SiC devices can operate at much higher switching frequency with lower switching losses, at higher temperatures. The figure 1.13 shows the benchmarking on the static characteristics of the state of the art SiC unipolar switches.

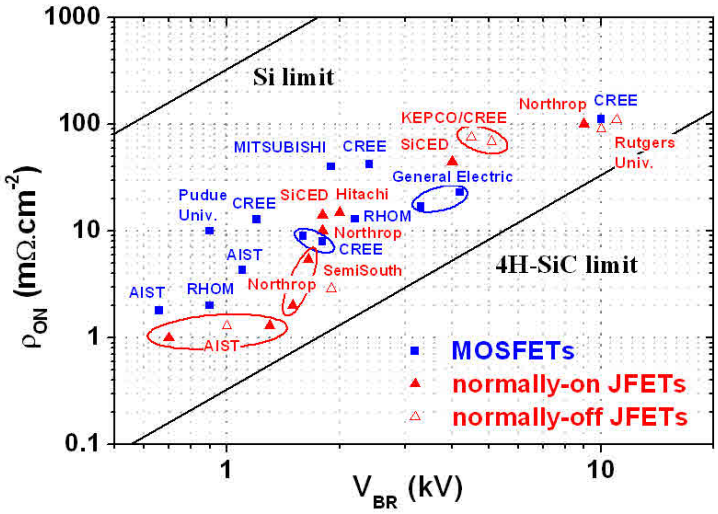

FIGURE 1.13 – Best unipolar power switches in the literature represented on the ρ_{ON} vs V_{BR} graph

1.3.2.1 Vertical MOSFET

Until now, the fabrication on SiC of vertical MOSFETs (VMOS) was a major objective for all the SiC players. Its functional similarities with Si-VMOSs and Si-IGBTs make it very easy to substitute them in many applications.

The SiC VMOS device will revolutionize the power electronic technology in the next decade. Thanks to the progresses in all the SiC fabrication steps, CREE and RHOM are now capable to produce and commercialize them. The table 1.7 summarizes the different VMOS devices available commercially.

Provider	V_{BR}	Current	Year
Cree	1200V	24-33A	2011
RHOM	600V	10A	21/12/2010
	1200V	20A	2011

TABLE 1.7 – Commercially available SiC VMOS

The VMOS structure has been difficult to produce for various reasons. First, the design of high voltage devices, like the VMOS, relies on structures that vertically spread the equipotential lines through the drift layer during the blocking state. In forward mode the vertical MOSFET uses a controlled inversion channel linking the source to the JFET and drift area, the electrons being then free to flow toward the drain as shown in figure 1.14.

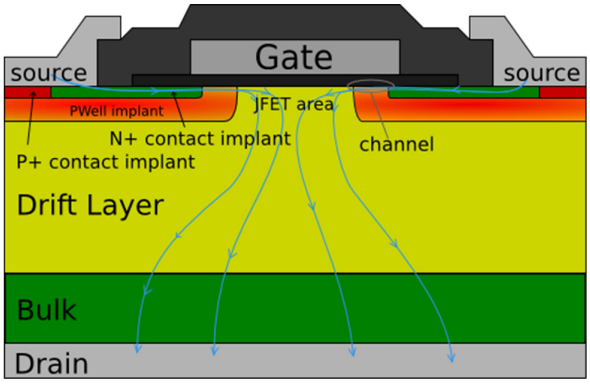

FIGURE 1.14 – Schematic view of the vertical cut of a VMOS cell

The major challenge with the VMOS integration on SiC is to obtain an inversion channel of good quality. This channel is created by the inversion of the p-type area under the gate when positively biased. Typically, the SiC/SiO_2 interface is worst than with Si. Many years of worldwide investigation have permitted to identify certain sources of the degradation and find solutions.

Another issue comes from the creation of p-well, as the diffusion of impurities in the SiC is impossible. The simplest solution is to use use implantation to selectively dope areas and especially the p-well ; this process creates surface crystal defects that will later deteriorate the channel's quality. Special care must be taken with the dose, profile and temperature of the p-well implantation as we will show later. Nowadays, the channel is a major resistivity source ; to reduce it, we must optimize the cell design, by minimizing the channel length and the cells' size so that we integrate the maximum of channel length per surface area.

To do so, one reduces each dimension of the cell to the minimum and uses specific geometries as shown in figure 1.15. The hexagonal cell geometry shown in figure 1.15a&c is theoretically the best solution as it presents the highest channel length to surface ratio. The devices commercialized by CREE have a channel length of 0.5μm [9] aligned with a high precision stepper and the one commercialized by ROHM have a channel length of 0.75μm with a cell pitch of 10μm [45] created with a self-alignment technique.

The SiC VMOS is an unipolar conduction device like the Schottky diode, and should also present a positive temperature coefficient. However, due to the high density of interface charges at the channel interface, the apparent channel mobility increases with temperature [46], reducing the device resistance.

1.2kV VMOS fabricated by CREE [7] show increasing on-state resistance with the temperature as shown on 1.16a. However the threshold voltage drifts from 1.8V at 25°C down to 1V at 200°C. The channel being very short (0.5μm), its contribution to the total resistance is reduced but the fixed charges at channel interface are perceptible in the threshold voltage drift instability phenomena.

The low quality of the gate oxide does not solely deteriorate the stability of the devices but also can reduce its lifetime. DMOSFETs fabricated by ROHM show results when submitted to TDDB test with high QBD of $15C/cm^2$ [45] for large structures. The interface charges can also influence the parasitic components in the structure. The equivalent capacitance between terminals of a power device affects its switching behavior. The SiC MOSFETs are especially developed to work at higher frequency than Si devices so the parasitic components of the device have great importance. The figure 1.17 shows the equivalent capacitances between the terminal of a VMOS and the different parasitic components created by its structure.

Capacitances created in the semiconductor vary with the depletion area created between the junctions. For example, the C_{dsj} on figure 1.17b (created by the p-well/drift junction) will evolve non-linearly with the bias between the drain and the source. As the doping level of the drift layer is superior for SiC devices, the depletion area will be thinner and the capacitance induced by the drift depletion will be superior for the same area. Again, C_{GD} which is composed of C_{oxd} and C_{gdj}, and C_{DS} which is composed of

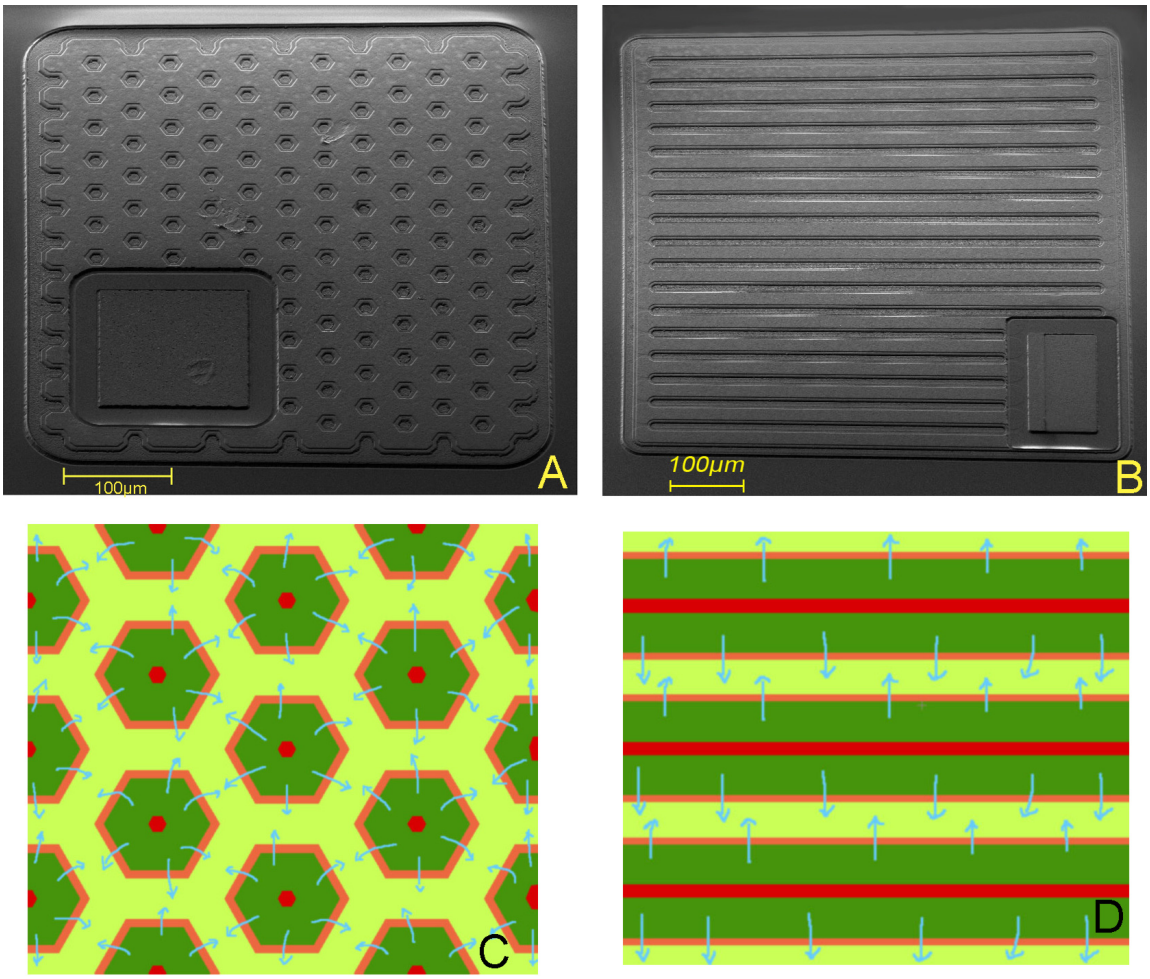

FIGURE 1.15 – Different geometries of VMOS channel fabricated at CNM ; (A) SEM picture of a VMOS with hexagonal cells, which doping structure is shown in (C) with red to represent the p-type impurities and green for the n-type. A SEM picture of VMOS with stripped channel is show in (B), the doping structure is represented in (D)

C_{dsj} and the capacitance p-well/n+ junction, will be also influenced by the drift doping concentration. For C_{GS}, composed of C_{m}, C_{oxs}, C_{oxc} and C_{c}, the drift layer concentration has no influence. However the permittivity of SiC and charges density at the SiC/SiO_2 interface has an influence on C_{GS}. Phankong et al. [8] has demonstrated that the short channel effects and the inversion mode have an influence on the dynamic behavior of the capacitances. Another important parameter is the charge necessary to switch the device. 1.18 shows the gate charge measured on 20A, 1.2kV 4H-SiC VMOS fabricated by CREE [7]. We can see that the gate charge is far inferior to equivalent Si MOSFETs and IGBTs.

The dynamic behavior of the SiC MOSFET is cleaned from all the bipolar effects. When turning-on (see figure 1.19) the device does not have to trigger the internal bipolar transistor and takes less than 70ns to open and close. During the turn-off, due to minority

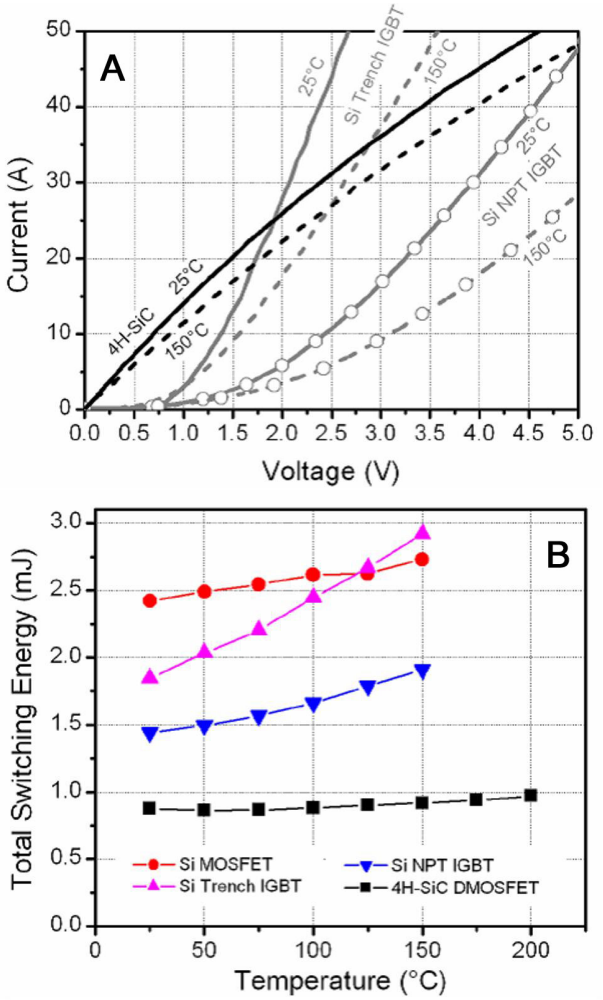

FIGURE 1.16 – Forward I-V characteristics (A) of a 1.2 kV SiC MOSFET by CREE and Si-IGBT at 25°C and 150°C. (B) Total switching energy as a function of the temperature for 20 A, 1.2 kV rated devices. Curves from [7]

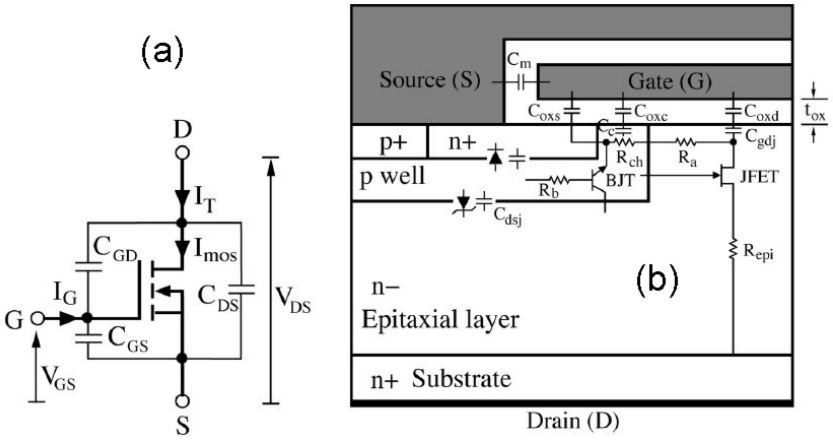

FIGURE 1.17 – (a) Equivalent capacitance between terminal of a VMOS, (b) cross section and associated parasitic components of the VMOS. Pictures from [8]

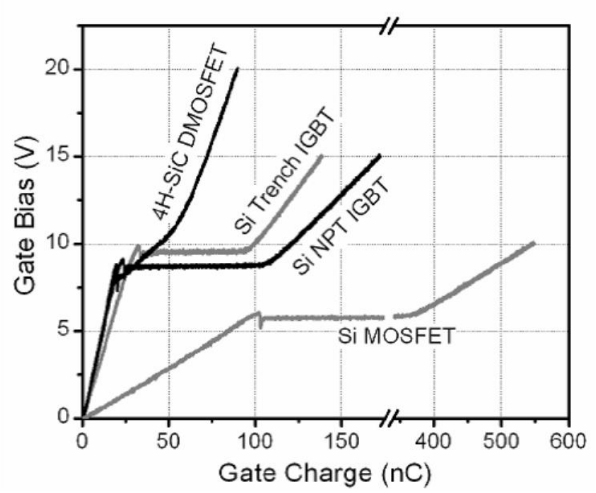

FIGURE 1.18 – Gate bias as a function of the gate charge for 20A-1.2kV 4H-SiC VMOS, Si-VMOS, Si trench IGBT and Si NPT IGBT, graph from [7]

charge storage delay, the IGBTs have a very pronounced current decay tail of several microseconds.

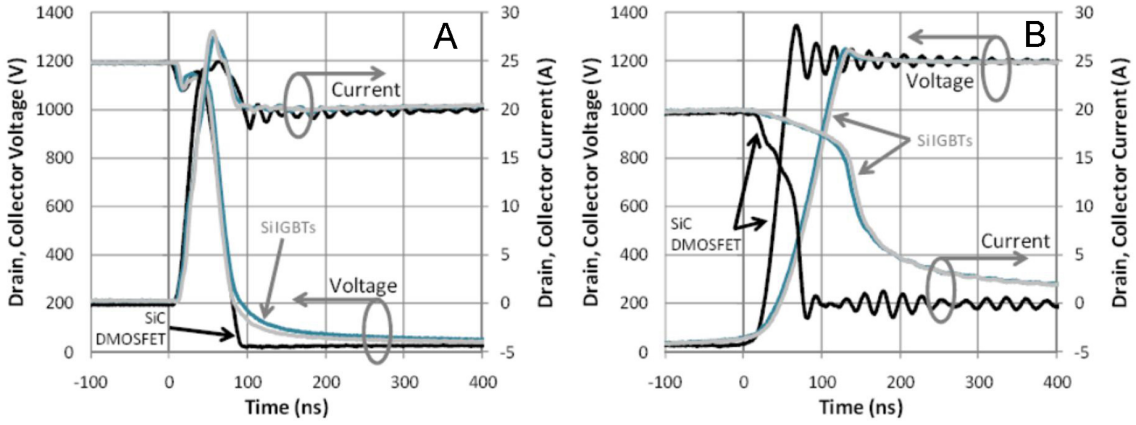

FIGURE 1.19 – Turn-on (A) and turn-off (B) waveform at 100°C of a 20A, 1.7kV 4H-SiC VMOS ($V_{GS} = 20V$) compared to 16A and 32A, 1.7kV IGBTs ($V_{GS} = 15V$) in a clamped inductive load circuit with 4H-SiC JBS diode as freewheeling diode, graphs from [9]

Moreover the dynamic losses of VMOS remain constant with temperature whereas on IGBTs it increases by 25% with a temperature increase from 25 °C to 150 °C as shown in figure 1.16. The table 1.8 summarizes the state of the art of the SiC VMOS encountered in the literature ; many of the devices have been produced by the three leaders : CREE, ROHM and AIST.

Difficulties engendered by the low oxide quality have pushed researchers to look for other solutions independent from the MOS interface to fabricate high voltage unipolar switches and came out with the VJFET.

Ref.	Device	V_{BR} (V)	R_{ON-SP} ($m\Omega.cm^2$)	Observation	Affiliation
[47]	3C-VDMOS	100	17	$30-40$ cm^2/V $-$ s	Acreo, Hoya
[48]	DEMOS	600	8.5	0.008mm^2	AIST
[49]	IEMOS	660	1.8		AIST
[45]	Trench-MOS	790	1.7	0.25mm^2	RHOM
[45]	Trench-MOS	900	2.9	7mm^2	RHOM
[49]	IEMOS	1.1k	4.3		AIST
[50]	IEMOS	1.2k	12.9	$\mu_{EFF} = 20$cm^2/V $-$ s	Mitsubishi
[45]	DMOS	1.3k	7.5	9.2mm^2	RHOM
[50]	DMOS	1.35k	5		Mitsubishi
[51]	DMOS	1.4k	5	20mm^2	GE Global Research Center
[52]	DMOS	1.45k	5.7	1.4mm^2	Toshiba & AIST
[9]	DMOS	1.77k	10	10mm^2	Cree
[53]	VDMOS	2.4kV	42	10mm^2 $\mu_{EFF} = 22$cm^2/V $-$ s $I_F = 10$A $V_F = 7.2$V	Cree
[54]	DMOS	4.2kV 3.3kV	23 17	10mm^2 1.2mm^2	GE & US Naval Research Lab.
[55]	UMOS	5kV	228	0.774mm^2	Purdue Univ.
[56]	DMOS	10kV	111	15.5mm^2	Cree

TABLE 1.8 – Best SiC VMOS in the literature

1.3.2.2 Vertical JFET (VJFET)

The JFET is a switch relying on the depletion region of a PN junction to pinch the source to drain channel and modulate its conductivity. The gate is connected to the P region to control the channel width. Vertical channel structures like the Buried gate JFET (BG-JFET) and Trenched and implanted JFET (TI-JFET) shown in figure 1.20 have the most successful ultimately. They require less fabrication steps than other structures and increase the efficient drift area when forward bias. Their source is located higher than the gate and the current flows vertically. Both structures are created via etching of the gate areas followed by an aluminum implantation to create the gate's p-well.

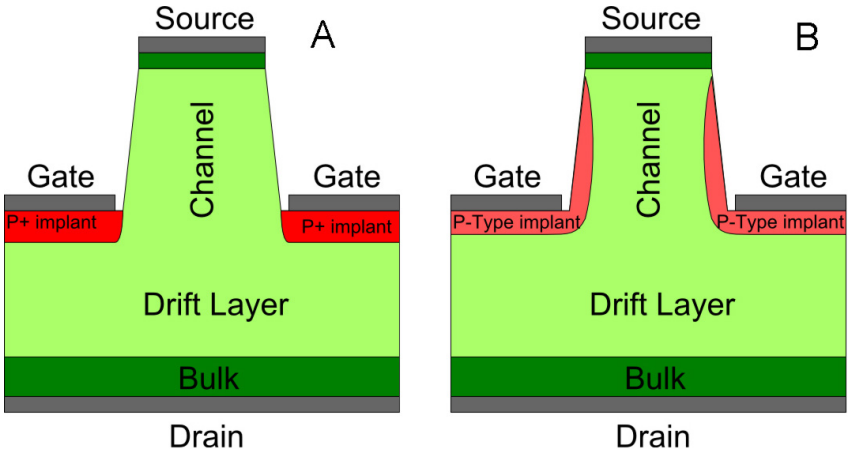

FIGURE 1.20 – Schematic view of a vertical cut through the active cell of a BG-JFET (A) and a TI-JFET (B)

The 1.9 and table 1.10 present the best normally-on and -off VJFET devices in the literature, we can see that a majority is BG-JFET or TI-JFET, and have been created in the last decade.

Ref.	Device	V_{BR} (V)	R_{ON} mΩ·cm^2	Active Area (mm^2)	Affiliation
[57]	VJFET	600	2.5		SemiSouth
[58]	BG-SIT	700	1	1	AIST
[59]	BG-SIT	1.1k	1.1		AIST
[60]	TI-JFET	1.65k	1.88		SiCLAB
[61]	TI-JFET	1.71k	2.7		SiCLAB
[62]	BG-JFET	1.68k	10	14.3	Northrop
[63]	BG-JFET	2k	5.7	6.8	Northrop
[64]		4k	45		SiCED
[65]	BG-JFET	9k	96	0.15	Northrop

TABLE 1.9 – Best normally-On SiC power JFET in the literature

Ref.	Device	V_{BR} (V)	R_{ON} mΩ·cm^2	Active Area (mm^2)	Affiliation
[66]	JFET	600V	2		Hitachi
[67]	TI-JFET	1.2kV	3	$15mm^2$	SemiSouth
[68]	TI-JFET	1.2kV	2.5	$3.15mm^2$	SemiSouth
[59]	BG-SIT	1.27kV	1.21		AIST
[61]	TI-JFET	1.7kV	3	$0.1mm^2$	SiCLAB
[69]	BG-JFET	1.8kV	10	$4.65mm^2$	AFRL, CREE
[70]	TI-JFET	1.9kV	2.8	$2.7mm^2$	SemiSouth
[71]	TI-JFET	4.3kV	40		SiCLAB
[72]	TI-JFET	10kV	87		SiCLAB

TABLE 1.10 – Best normally-On SiC power JFET in the literature

1.4 Defects

As we have seen in the previous chapter, irregularities during the crystal growth lead to crystal defects that can be destructive for the devices or at least deteriorate its characteristics [26, 73]. The most famous defects are the stacking faults (SF) and micropipes (MP). But many other defects are created by dislocations or vacancy in the crystal.

1.4.1 Stacking Faults (SF)

A crystal polytype is defined by its periodicity, the deviation from its specific periodicity as shown in figure 1.21 is called a stacking fault (SF).

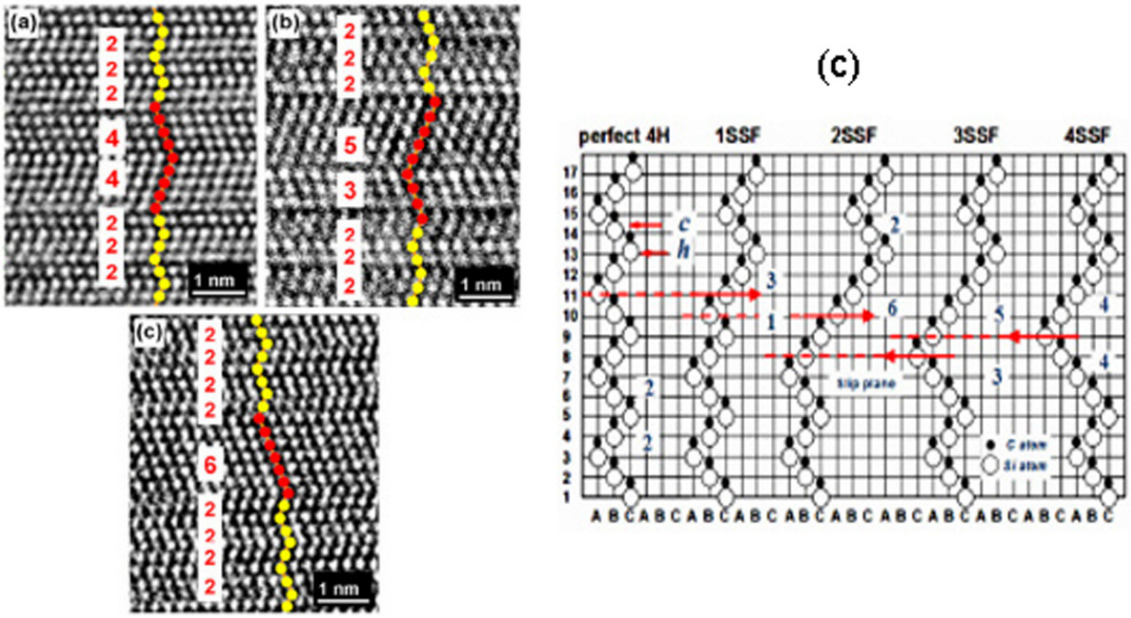

FIGURE 1.21 – (a,b,c) TEM pictures of different stacking faults and (c) schematic view of the stacking faults structure, pictures and schematic view from [10]

In 4H-SiC, the most common SF is an inclusion of 3C stacking which deteriorates the carriers' lifetime and critical electric field of the crystal. Carriers lifetime is a major parameter for the bipolar components as it determines their conductivity, its reduction increase the bipolar chips resistivity.

They are commonly observed by ultraviolet photoluminescence (UVPL) imaging. The SF can be created during the epitaxial growth [74] or by conversion of a basal plane dislocation during bipolar device operation.

1.4.2 Dislocations

In the dislocation, the crystal lattice is distorted along a line while the periodicity of the lattice in not affected.

1.4.2.1 Basal Plane dislocations (BPD)

In a crystal, we call primary slip plane, the plane requiring less energy to dislocate. The primary slip plane for 4H-SiC is the basal plane, thus planar dislocations form most easily in the Basal plane and they are called Basal Plane Dislocations (BPD). They can be evidenced by optical emission microscopy and Ultra Violet Photo-Luminescence [75] (UVPL) or Synchrotron White Beam X-ray Topography (SWBXT).

As the BPDs are metastable states of the crystal, the energy brought by the bipolar recombination permit them to expend and convert to SFs. SFs formation during bipolar devices operation is known to be the principal source of forward-bias-induced electrical deterioration. It has been proven to degrade the PiN diodes, BJTs and MOSFETs characteristics.

During the growth process, they are a nucleation sources for Threading Edge Dislocations (TED) and Schockley-type stacking faults [74–76]. As the TEDs are less detrimental than SFs to the devices, last studies have been focused successfully on converting the BPDs into TEDs during the epitaxial growth process. The influence of the crystal orientation has also been observed ; the 4° and 2°-off wafers present less BPDs than 8° off wafers.

1.4.2.2 Threading Screw Dislocation (TSD)

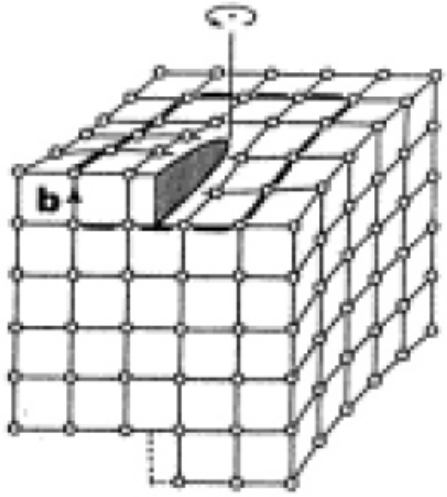

FIGURE 1.22 – Schematic view of a screw dislocation

The Threading Screw Dislocation (TSD) is a distortion created by a helicoidally grown pattern around the dislocation line as shown in 1.22. The Burgers vector ($\vec{b}$) corresponds to the step height of the dislocation.

TSD and their Burger vector can be characterized with atomic force microscopy (AFM) or back reflection geometry in synchrotron white beam X-ray photography (SWBXT). The TSD produce a diffraction effect when interfering with the X-ray beam [77] with a spectrum depending on the Burger vector, so the SWBXT to characterize the TSD.

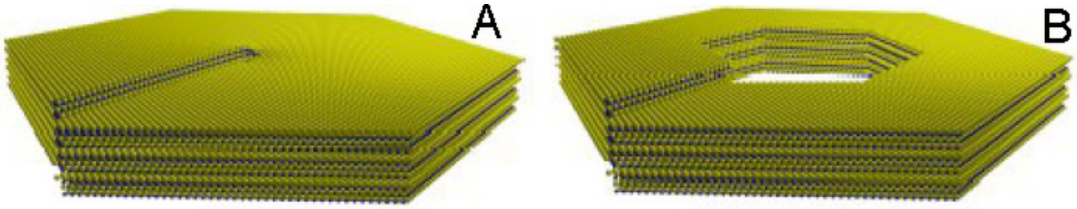

FIGURE 1.23 – Illustration of (A) a closed-core and (B) open-core screw dislocation with a Burgers vector $\vec{b} = 1c$ in the crystal lattice of 4H-SiC, illustration from [11]

When the Burger vector is superior to 3c, the screw dislocation forms a hole along the dislocation line as shown in figure 1.23b, it is also known as an open-core dislocation. When the open-core dislocation is parallel to the c-axis, it is called micropipe (MP).

TSD can also be revealed by selective etching as shown in figure 1.24.The presence of a micropipe in a device induces high level of leakage current or totally destroys its reverse blocking capability, so it is considered as a killer defect.

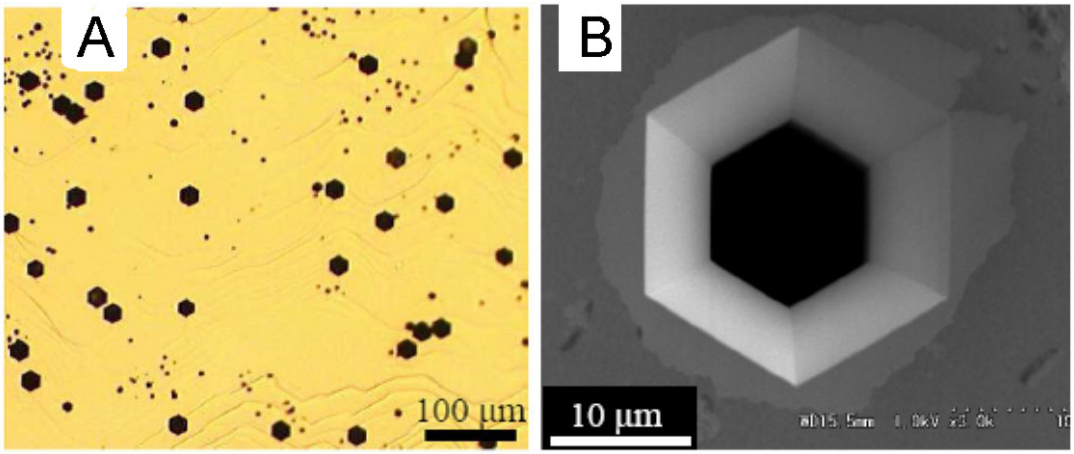

FIGURE 1.24 – Pictures of a TSD revealed by selective chemical etching taken with (a) optical microscope and (b) SEM after chlorine thermal etching during 30min at 980°C, pictures from [12]

A micropipe situated in the termination of a power device is shown in figure 1.25, we can see metal from the process that stay in its core.

FIGURE 1.25 – Picture of a micropipe taken on-wafer during the fabrication process of SiC diodes at CNM of barcelona

Being the most visible and detrimental defect on the wafers, the reduction of its density on wafers has been the principle goal until 2009. Its major density reduction in the last years (down to micropipe-free wafers) has brought in evidence the role of other defects as Stacking Faults and Basal Plane Dislocations in the deterioration of SiC devices' characteristics. The role of the threading edge dislocation in the augmentation of the leakage current in SBD and JBS diodes has also been evidenced recently [26].

1.4.2.3 Threading Edge dislocation (TED)

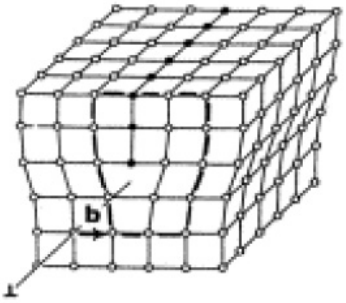

FIGURE 1.26 – Schematic view of a threading edge dislocation

On standard 8° or 4° off 4H-SiC wafers, the screw dislocations and threading edge dislocation parallel to the c-axis can cross the whole wafer. The figure 1.26 shows the TED structure formation in the crystal lattice. Threading dislocations (both edge and screw) are believed to be benign in terms of forward-bias-induced electrical degradation phenomenon or when devices are reverse biased.

1.4.3 Inverted pyramid defect

This defect is visible with the optical microscope as sharp triangular shape at the wafer surface as shown in figure 1.27. No major detrimental effect on the device characteristics has been reported until now. However they are symptomatic of other defects, Shrivastava et al. [78] propose that in grown stacking faults originating primarily from BPDs are nucleation source for the Inverted pyramid.

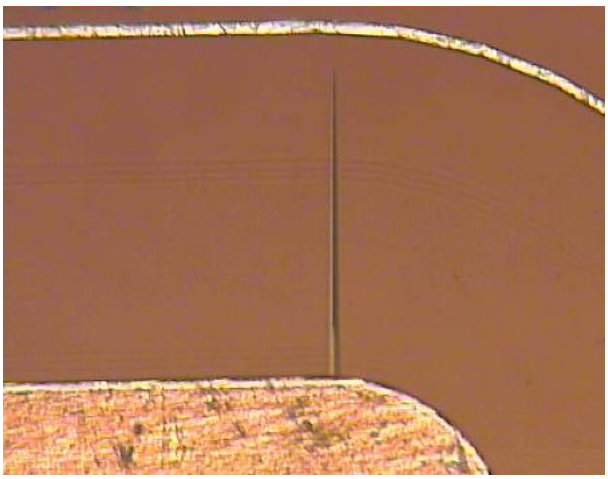

FIGURE 1.27 – Inverted pyramid defect in the termination of a vertical power diode

1.4.4 Vacancies

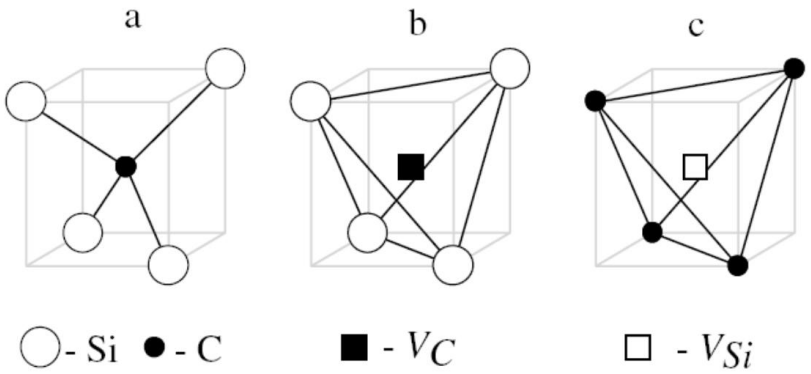

FIGURE 1.28 – Vacancies in SiC ; (a) defect free, (b) carbon Vacancy, (c) silicon vacancy. Pictures from [13]

As its name indicates, this is a point defect characterized by one or more missing atom in the lattice sites that can create traps. Vacancies can associate to create traps with different energy, the most commonly known are : di-vacancy ($V_{SI} + V_C$), antisite pair (SiC + CSi).

The C vacancies create a deep donor with activation energy of 1.4eV ; it is exploited to create Semi-Insulating wafers used to produce high frequency devices.

1.4.5 Summary

The table 1.11 summaries the effects of the different major defects encountered in SiC on the devices. We can see that, except for the TED, they all have negative effect on the devices ; however one must take into account their density. In the table 1.12 we summarize the defects' situation on the state of the art wafers, showing their density and global effect on produced devices' yield and reliability. We can see that the TSD and BPD became a major concern. Now that the micropipes' presence has been minimized, the effect of the other defects could be evidenced and the SiC grower's community is now focalized on their suppression.

		SBD	JBS	PiN	VMOS	VFET	BJT
MP	Leakage Current	+++	+++	+++	+++	+++	+++
BPD	Leakage Current	?	?	?	Source ? Gate ?	?	?
	Bipolar Degradation		+	+++		+	+++
SF	Leakage Current	++	+	?	source ? Gate ++		
	Double barrier	++	+				
	Higher resistance	+	+	++		+	++
TSD	Leakage Current	++	+	?	Source ? Drain ?	?	?
	Double Barrier	++	+				
TED	Leakage current	-	-	-	-	-	-

TABLE 1.11 – Detailed summary of defects effects on SiC devices

Defect	Density (cm^{-2})	Yield Effect	Reliability Effect
MP	< 2	minor	Critical
TSD	10^3	Medium ?	Medium ?
TED	$< 10^4$	none	none
BPD	10^3	none	Critical (bipolar)
SF	1	minor	Critical
Additional Epitaxial defects	$1 - 10$	medium	medium
Technology defects	$1 - 10$	medium	medium

TABLE 1.12 – Overall defect situation on state of the art wafers [15]

Chapitre 2

Simulations

Precise creation of semiconductor devices requires an initial theoretical study to design precisely their structure in function of the different objectives. As the physical properties of the SiC are very different from Si, former studies that determined the ideal dimensions of the Si devices' termination, active area, and etc. are obsolete. So we built a physical model in order to simulate SiC devices with ISE Sentaurus. It allowed us evaluating the different possibilities of terminations, exploring innovative designs and choosing the best suited designs as shown in part 1.5. We also performed simulation of the VIEMOS active area, presented in part 1.6, to choose the different design parameters to be tested in the fabricated devices presented in chapter 4.

2.1 Terminations for vertical devices in SiC

High voltage chips are composed of three parts ; the active area, the drift layer and the periphery. The active area is situated where the current flows and is controlled, on the front side. The drift layer sees current flows but does not control them ; its role is to control the potential distribution between the current emitter and receiver when the device is blocking it.

High voltage chips need an important drift layer length. By using the back side of the wafer as an electrode as shown in figure 2.1, the vertical structure allows simplifying the protection design and exploits the full thickness of the epilayer as a drift layer, which reduces the device' size compared to a lateral structure. When reverse polarized, the equipotential lines are separated horizontally in the drift layer and emerge vertically around the active area. The periphery, around the active area, is composed of two parts ; the termination and the channel stopper (see figure 2.1).

The channel stopper is made of a highly doped area of the same doping type as the drift layer. Surface charges can create conduction channel between chips. It ensures that the potential in this area is the same as the potential of the bulk ; so that other chips on the same wafer do not enter accidentally in conduction, it also ensures a good switching behaviour by constraining faster the potential around the chip.

The termination does not see current flows ; its role is to control the potential's distribution around the device in order to reduce field crowding due to the topologic or electronic variations in the periphery. Various designs already exist for silicon chips [79,80] as

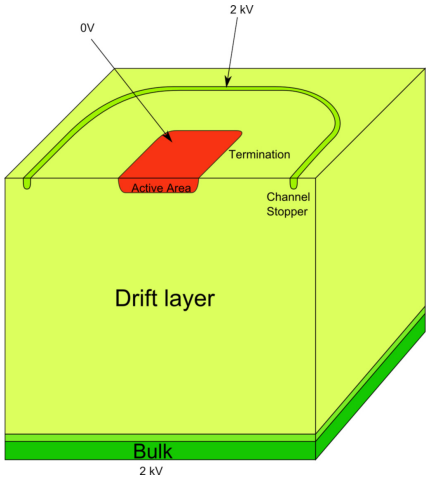

FIGURE 2.1 – Representation of vertical chip when reverse biased at 2kV

shown in figure 2.2, the Silicon Carbide capabilities and properties being much different from the Silicon ones, new terminations have been introduced. The capabilities of the different terminations on SiC and their impact on the device's behaviour must be well considered for the future applications.

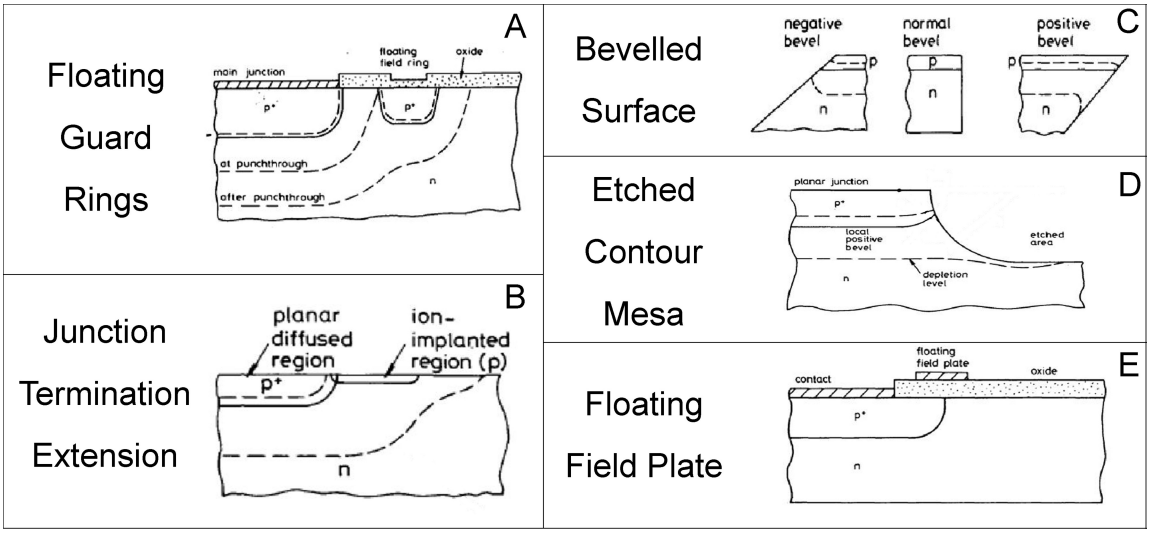

FIGURE 2.2 – Terminations used on High voltage Silicon devices

We will present several planar terminations on SiC, considering their advantages and drawbacks for the chip capabilities and fabrication process.

2.1.1 Junction Termination Extension

The Junction Termination Extension (JTE) is the most popular in SiC.

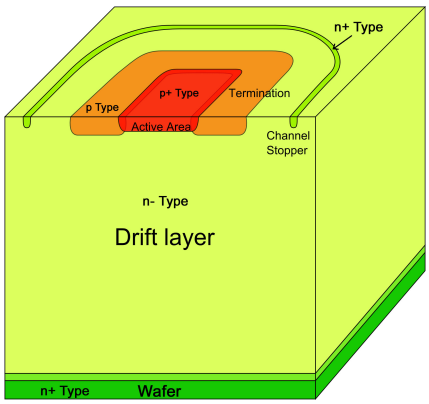

FIGURE 2.3 – Schematic view of the a PiN diode with a JTE termination

It is made of large P-type ring surrounding the active area, as shown in figure 2.3. When the device is reverse biased, the depletion layer spreads into the JTE. Ones totally depleted, the JTE becomes a highly resistive area and the electric potential is distributed over the full length of the JTE as shown in figure 2.4a.

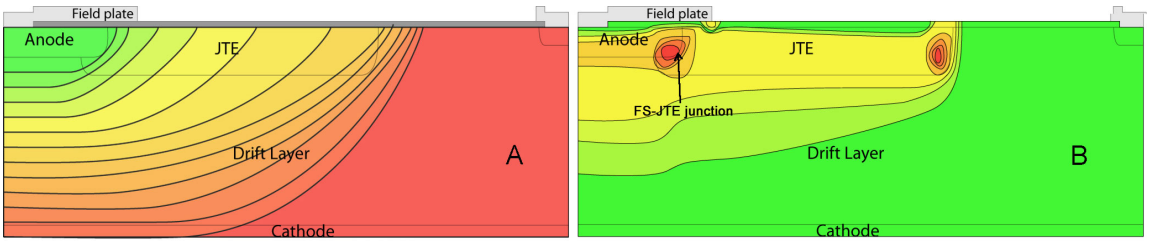

FIGURE 2.4 – Equipotential lines (A) and Electric field (B) repartition in a vertical PiN diode with JTE Termination when reverse biased

The total dose of the JTE must be chosen low enough so that it can be totally depleted before field crowding occurs at the JTE end and high enough so that it stays resistive enough to separate equipotential lines. The figure 2.4b shows a schematic representation of the electric field in an optimized JTE. One can see that the two extremities of the termination show superior electric field ; the FS-JTE junction and the JTE end. These two weak points are created by the field crowding around the junctions and their sensibility varies with the JTE dose.

When the JTE doping is too low, the electric field at FS-JTE junction becomes strong very early. On the contrary if the JTE doping is too elevated, the equipotential lines do not penetrate the JTE and field crowding appears too early at the JTE extremity. Fine optimization of the JTE dose (see figure 2.5) and profile are necessary to attain a maximum breakdown voltage on the overall wafer area.

The JTE is created via the implantation of Aluminium or Boron impurities, which are then electrically activated via high thermal annealing. All the impurities are not activated and this proportion will have consequences on the JTE dose and thus its efficiency.

We performed 2D simulations of JTE termination on a 4H-SiC PiN diode with the structure shown in figure 2.4a, a 12μm thick drift layer doped at $1{\cdot}10^{16}\text{cm}^{-3}$. The JTE profile is 500nm deep and presents a plateau between 100nm and 300nm depth, its lateral junction is a Gaussian profile 100nm wide.

We varied the JTE width between 10μm and 100μm at a constant JTE dose of $1.2{\cdot}10^{13}\text{cm}^{-2}$ and considered the breakdown voltage attained when the maximum electric field was equal to 2.5MV.cm^{-1}.

We report the simulated breakdown voltage as a function of the JTE width in figure 2.5a. One can see that the blocking capability of the termination increases rapidly from 10 μm ($V_{\text{BR}} = 1.5$kV) up to 25μm ($V_{\text{BR}} = 1825$V), then saturates around 1850V. Once the JTE is sufficiently long to separate equipotential lines, its efficiency cannot be increased by increasing its length. A longer JTE permits to reduce the electric field in the termination and above it, and thus reduces the stress operated on the passivation layer.

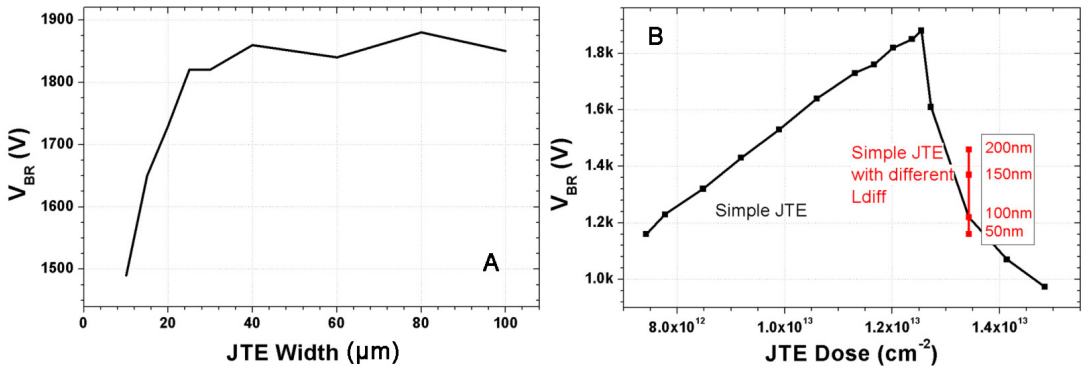

FIGURE 2.5 – Simulated Breakdown voltage as a function of the JTE length (a) and dose (b) for a 4H-SiC PiN Diode with a 12μm $2{\cdot}10^{15}\text{cm}^{-3}$ N-type drift layer

We also varied the JTE dose between $7.5{\cdot}10^{12}\text{cm}^{-2}$ and $1.5{\times}10^{13}\text{cm}^{-2}$ with a JTE length of 100μm as shown in figure 2.5b. Up to a JTE dose of $1.2{\cdot}10^{13}$ cm^{-2}, the diode breakdown voltage increases linearly ; during this regime the diode's breakdown occurs at the FS-JTE junction, due to field crowding around it. When the JTE dose increases, its resistivity increases, consequently the equipotential lines are separation increases and the field crowding decreases. Above $1.2{\cdot}10^{13}$ cm^{-2}, the JTE dose is too high to be depleted before the field crowding at the JTE extremity creates too high an electric field. It is called the JTE dose threshold. After reaching the JTE dose threshold, the maximum electric field is experienced at the JTE end, increasing the JTE dose only makes it worse, so the JTE efficiency violently decreases.

The field crowding around the JTE's end is very dependant on the lateral junction profile. So we also simulated the breakdown voltage for different values of lateral diffusion length (L_{DIFF}) between 50nm and 200nm for a JTE dose ($1.375{\cdot}10^{13}\mathrm{cm}^{-2}$) above the JTE dose threshold, and reported the results in figure 2.5b. The breakdown voltage increases from 1.15kV ($L_{\mathrm{DIFF}} = 50\ nm$) up to 1.45kV ($L_{\mathrm{DIFF}} = 200\ nm$), this result shows a larger lateral diffusion can increase the breakdown voltage by more than 20% when the JTE dose is superior to the dose threshold. The masking technique has much to do with the lateral junction profile and must be chosen wisely. Some people use a special process for the JTE mask [81], in order to obtain sloped side on the oxide and create a larger transitional area at the end of the JTE.

For a breakthrough diode, the optimal dose of the JTE is equivalent to the drift dose if one does not take the activation level and lateral junction into account. A lot of investigations have been conducted previously at CNM and Ampere lab. [82] in order to optimize the annealing process and implantation profiles. We consider that 90% of the implanted impurities are activated.

2.1.2 Guard Rings

The Guard Rings (GR) Termination is a famous alternative to the JTE.

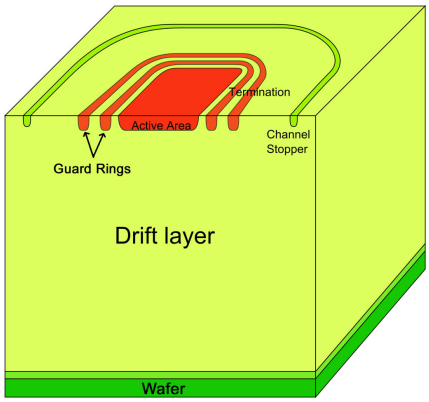

FIGURE 2.6 – Guard rings on vertical PiN Diode termination

It is made of highly P^+-type rings, surrounding the active area (see figure 2.6). Unlike the JTE, the doping level of the rings has no major influence on the termination efficiency. It can be created simultaneously with other parts of the chip requiring highly doped implantation of the same type. The figure 2.7 shows a schematic view of a vertical cross-section through the VDMOS' GR termination and a part of the active area. The two guard rings are created with the same layout and implantation level as the PWell. This shows that the PWell or other P+ implantation of IGBTs and MOSFETs can be used to create the guard rings. Compared to the JTE, it permits to save one process level ; this is the major advantage of the GR termination.

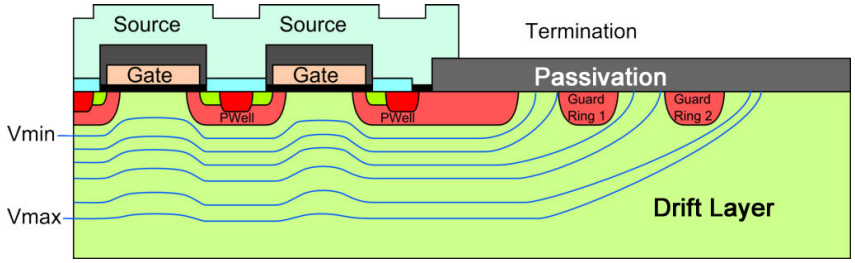

FIGURE 2.7 – Guard rings on VMOS structure

On figure 2.7, we also represented the equipotential lines in the drift layer ; guard rings separate them and consequently reduce the field crowding effect. We performed simulations of GR on a PiN diode with a drift layer of 12 μm doped at $2{\cdot}10^{15}$ cm^{-3}. The simulated guard rings are made of the same P+ implantation profile as the anode ; 400 nm deep, doped at $1{\cdot}10^{19}$ cm^{-3}, and a 100 nm lateral straggling. We first simulated the breakdown voltage of the termination with one ring at different distances from the anode with different values of lateral diffusion ($L_{\mathrm{DIFF}}/T_{\mathrm{P+}}$) ; the result is shown in figure 2.8.

If we look around the optimal spacing, a spacing difference of 0.5 μm decreases the breakdown capability of the termination by 10%, so the termination is very sensitive to the distance between the anode and the ring. We can also see that an increase of the lateral diffusion from 0.2 to 0.5 increases the breakdown capability by more than 30%. The GR are very sensitive to the field crowding due to the inexistent diffusion of impurities in the crystal, the lateral junction profile is essentially due to the lateral straggling during implantation and can be estimated around 20% of the implantation depth. So the optimal distance for one GR is situated around 2.8 ± 0.1 μm, which gives a reverse capability of 400 ± 40 V. However the masking technique used to implant the rings with strongly influence their lateral profiles, with multiple rings the protective efficiency of each ring will influence the next ring's efficiency, so the rings efficiently protect the device only if precisely positioned ; this termination can only be designed with a precise knowledge of the rings' lateral profile and the assistance of numerical simulations.

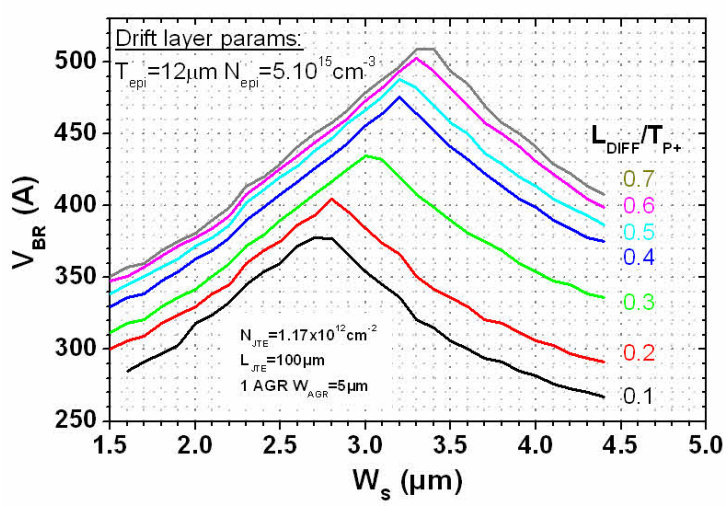

FIGURE 2.8 – Guard ring distance influence on breakdown voltage on termination with one guard ring for a 12μm $5{\cdot}10^{15}$cm^{-3} drift layer with different values of lateral straggling

A PiN diode with this drift layer is theoretically capable to block 2kV ; the maximum reverse bias attainable with one guard ring is 450V. To attain the maximum reverse capability of the drift layer, we need to add more rings. We performed the simulation of the same diode a GR termination with up to 12 rings. The termination dimensions were first simulated and optimized with one guard ring as shown in figure 2.8 ; then, more rings were added progressively, looking for the ideal disposition of rings for each added ring. The rings' position is optimal when field crowding is similar on each ring. So we optimized their position by maintaining the size of the rings constant, and searching the ideal electric field repartition by changing the distance between them. For each ring added to the termination, the rings' spacing had to be reduced to increase the maximum

attainable breakdown voltage. With increasing number of rings, the termination showed increasing sensitivity toward the rings' spacing ; with 10 rings, a variation of 100nm between two rings reduces the termination capability by more than 20%. The figure 2.9 shows a simulated potential and electric field in an optimized GR termination of 10 rings biased at 1.2kV.

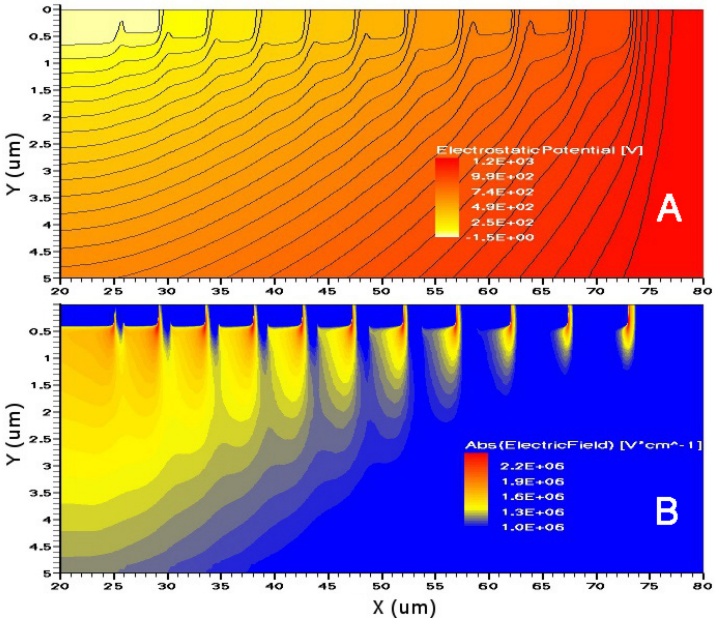

FIGURE 2.9 – Simulated potential (a) and electric field (b) in a guard ring termination at 1.2 kV for a vertical 4H-SiC PiN diode with a n-type drift layer of 12μm $2{\cdot}10^{15}$cm^{-3}

In figure 2.9a, we can see that the equipotential lines emerging on the termination are distributed between the rings as explained previously. In figure 2.9b, we can also see the field crowding effect around each ring due to the equipotential lines' transition from horizontal to vertical at the rings' corner. So the areas of highest electric field are tiny and situated there. We performed a horizontal cut, from the simulation presented in figure 2.9b, of the electric field where it is the most intense, the figure 2.10 shows it.

This representation allows seeing precisely the extreme impact of field crowding on the GR termination. Each ring protects its left neighbour ; consequently, the termination's efficiency is very sensitive to each ring' spacing and geometry. Simulated guard rings had spacing between 3μm and 5μm, which are dimensions next to the precision limit for the Al implantation mask. With an optimized GR termination of 10 rings, the diode attained a maximum blocking voltage of 1.2kV, though the vertical 1D maximum blocking voltage of the drift layer is about 2kV. To increase the blocking capability of the termination, we can add more rings, which induce the reduction of the rings' spacing under 3μm. We can use a different masking technique to increase the lateral straggling [MERR'06] during the implantation and thus reduce the field crowding effect around the

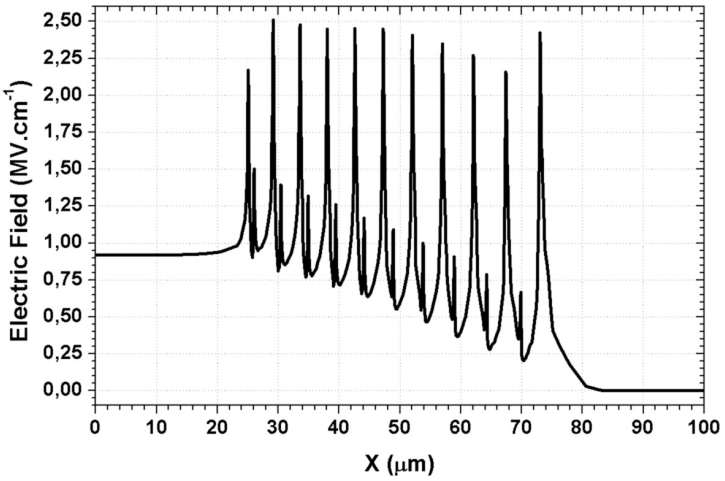

FIGURE 2.10 – Electric field cuts at 400nm from the surface

rings ; it must be compatible with the other structures created via this level. We have seen that the lateral junction's geometry of the implantation has a strong influence on the termination efficiency ; this parameter must be perfectly known and controlled before designing the guard rings termination. By reducing the number of process steps to fabricate the device, this termination allows reducing the costs ; it will be used industrially once the fabrication process is stable and perfectly known so that a fine optimization of the guard rings termination can be done. We included some GR termination trials during VDMOS fabrication but they have shown far lower capability compared to other terminations tested at the same time. These results are presented in the VMOS chapter of this work.

2.1.3 Mesa

This technique is used in Silicon technology and often combined to the JTE [83] (see figure 2.11) to increase its efficiency. In SiC technology, the mesa structure is mostly used for PiN diodes, BJTs, where a P+ layer is created via an epitaxial layer and one must etch it on the outer part of the active area. Thanks to the etched step (see figure 2.11), the depletion layer propagates vertically as for an ideal 1D junction, and there is no lateral P/N junction between the active area and termination of the chip, it suppresses the inherent field crowding effects of such a junction.

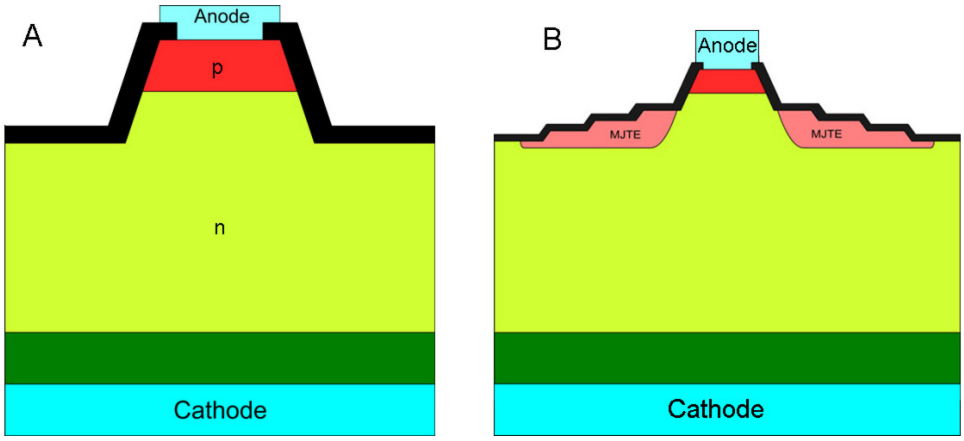

FIGURE 2.11 – mesa (a) and modified JTE (b) structures

The etching process, being aggressive, deteriorates the quality of the crystal surface ; it induces poor SiO_2-SiC interface quality by increasing the surface roughness and interface charge density. This can reduce the termination stability and reliability. The equipotential lines bend at the step corner and create local field crowding in this area. To reduce it, the mesa structure is usually combined with a JTE implantation and multiple etching steps can be created [84] as shown in figure 2.11b. This structure forms a multiple JTE termination with one implantation step. The multiple JTE is difficult to tune, because it is even more sensitive to each JTE dose and SiO_2-SiC interface states. As the chips fabricated during this work did not have an etching step during the process, we did not use such termination techniques.

2.1.4 Assisting Guard Rings

An optimized JTE can achieve a breakdown voltage close to the ideal one. However, the breakdown voltage is too sensitive to the JTE dose. As we have seen in the JTE presentation, when the JTE doping is inferior to its doping threshold, the breakdown will occur when the FS-JTE junction's electric field is too elevated. The Assisting Guard Ring (AGR) termination [11] is using the guard ring termination principle, separating the equipotential lines between highly doped rings after the FS-JTE junction as shown in figure 2.12.

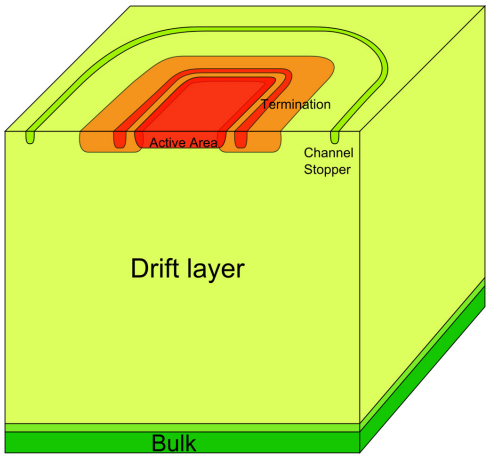

FIGURE 2.12 – PiN Diode with a JTE and an Assisting Guard Ring implanted with the anode implantation level

The AGR permits to reduce the electric field at this junction and thus increases the breakdown voltage for a given JTE dose under the threshold dose as shown in figure 2.13. The figure 2.13 shows the simulated influence of the AGR on the breakdown voltage attained by the termination of a PiN diode with a 12 μm drift layer doped at $2{\cdot}10^{15}\text{cm}^{-3}$; three rings have been positioned at the beginning of the JTE with a size of 3 μm and spacing of 5 μm, 5.5 μm and 6 μm.

The rings' position has been optimized previously so that the electric field on each ring is equal when the maximum voltage is attained for a JTE dose of $8{\cdot}10^{12}$ cm^{-2}. For a JTE dose inferior to the JTE dose threshold, the rings allow increasing the breakdown voltage by approximately 150V, which represents 10% of the optimal breakdown voltage for this drift layer. Two different terminations on a PiN diode with a 12 μm thick drift layer doped at $2{\cdot}10^{15}$ cm^{-3} were simulated when reverse biased at 1600 V ; the first termination has a simple JTE and the second termination is made of a JTE with 3 AGR. Both JTE profiles are similar and their total dose is situated under the JTE dose threshold ($1.05{\cdot}10^{13}$ cm^{-2}). To compare the electric field in the terminations, horizontal cuts at 1.6 kV was performed on both cases at a depth of 400 nm ; they are shown in figure 2.14. We can see that

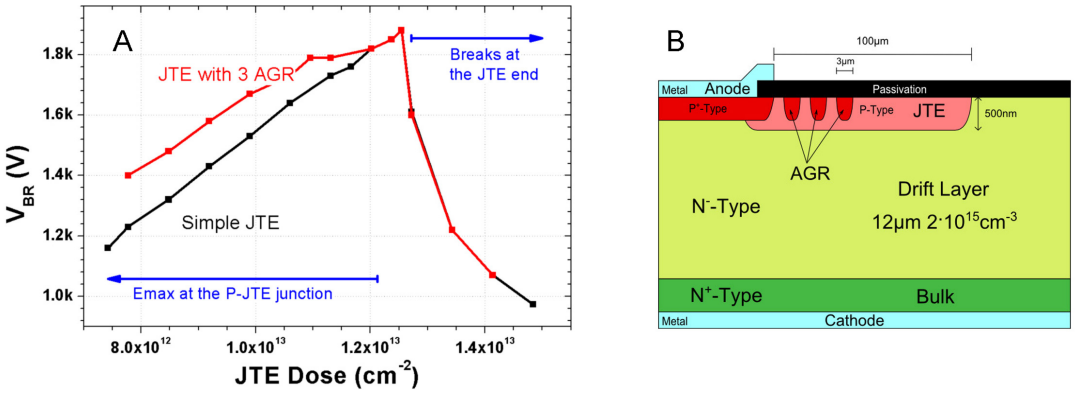

FIGURE 2.13 – (a) Simulated breakdown voltage of a PiN diode with a JTE or a JTE with 3 AGR for different JTE doping concentrations and (b) schematic view of the PiN diode with a JTE and 3 AGR

the electric field at field stopper to JTE (FS-JTE) junction is reduced to 2.2 MV.cm^{-1} compared to 2.4 MV.cm^{-1} with the simple JTE. We can also see that the rings are well positioned as they all exhibit a similar electric field peak.

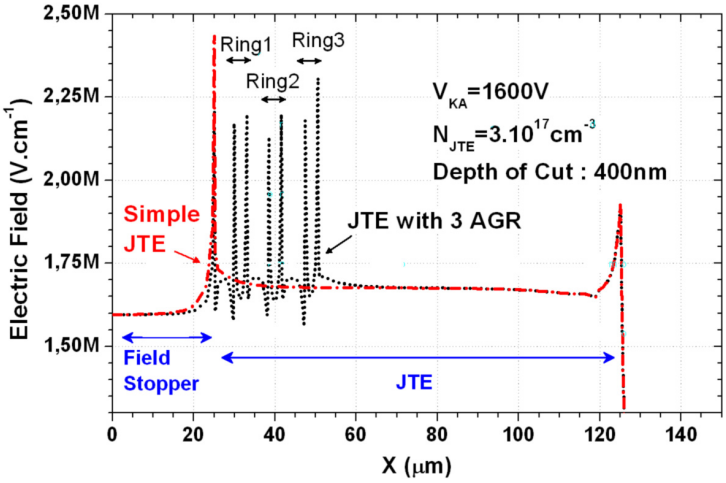

FIGURE 2.14 – Simulated Electric Field inside the termination for a JTE and a JTE with Assisting Guard Rings

Due to the implantation dispersion and masking technique, the FS-JTE junction is not always perfect on the entire periphery, and local electric field peaks can be created by irregularities. Reducing the electric field at this junction permits to minimize those risks and also reduces the stresses applied on the oxide and passivation layer ameliorating the diode's reliability in the long term. To evaluate the influence of the AGR's position on the termination efficiency, a termination with a JTE and one AGR was simulated for different distances between the ring and the FS on a similar PiN diode with the same JTE dose, the result is presented in figure 2.15. We can see that with one ring one can

gain up to 80 V. The step shape of the curve comes from the low time step's resolution of the simulation which moved in steps of 30 V.

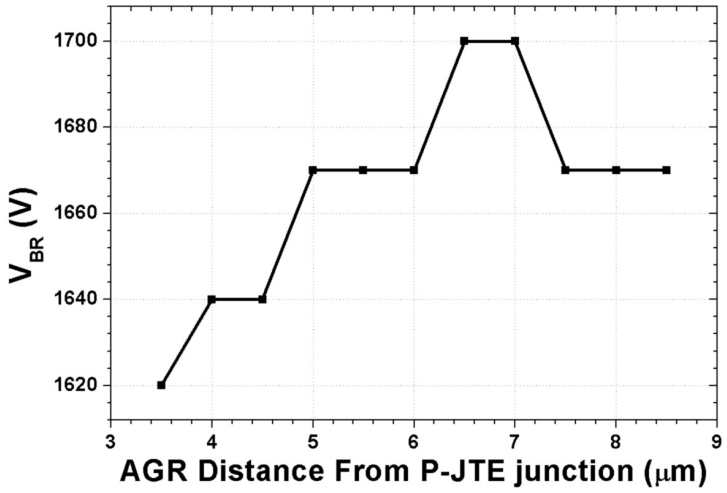

FIGURE 2.15 – Breakdown voltage as a function of the Assisting Ring distance from the FS-JTE junction

Moreover, the termination is tolerant to a variation of more than 1μm toward the rings' spacing for a variation of V_{BR} inferior to 1%. Compared to the GR termination, the AGR is far more tolerant toward the rings position, which makes its fabrication easier. Different simulations of the termination for 1.2kV and 6kV PiN diodes, permitted to optimize the rings spacing for terminations with up to 8 AGR. Those designs were included in several Schottky, JBS diodes and VMOS layouts presented in the next chapters ; the results showed good agreement with the simulation conclusions as will be shown in the chapter 3 and 4. The AGR termination is a reliable design easily created with the classical SiC technology, its tolerance to the process imperfection and its simplicity makes it a promising termination for high voltage chips made of Silicon Carbide.

2.1.5 JTE Rings

The JTE rings, shown in figure 2.16 , have been first reported under the name of guard ring assisted resurf (GRA-resurf) in 2002 [85], where they were utilized on 1.2 kV Schottky diodes. This structure was patented in 2003 by the same author [86]. After the brief appearance of this promising termination, we could not find any report of its use on SiC devices.

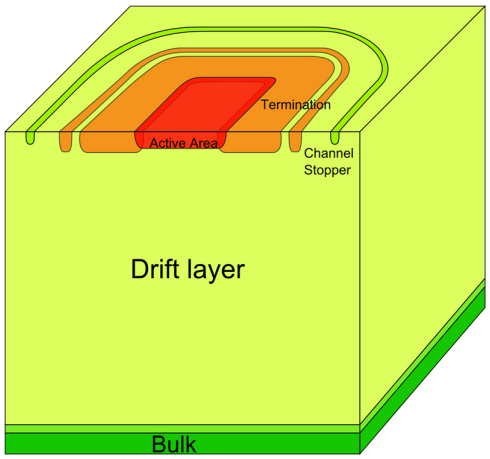

FIGURE 2.16 – JTE Rings termination structure

The figure 2.17 shows the simulated electric field at the end of a standard JTE in a diode biased at 1.2 kV. We chose a JTE dose ($1.3{\cdot}10^{13} cm^{-2}$) above threshold (see figure 2.5b) so that we can observe the electric field repartition in the termination. The limited diffusion of the Al impurities in SiC induces abrupt lateral junctions around the implanted areas. We can see that the abrupt lateral junction at the end of the JTE induces field crowding before the total depletion of the JTE. Thus, the JTE dose threshold of standard JTE is determined by the field crowding at the end of the JTE.

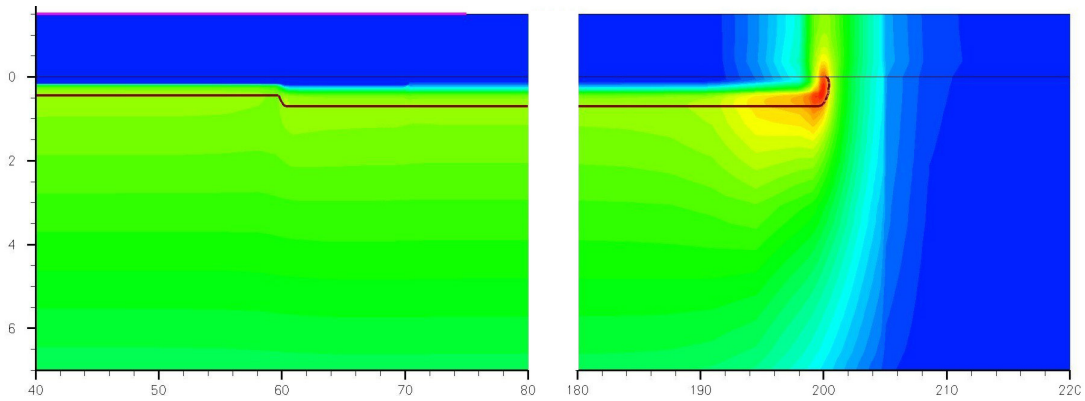

FIGURE 2.17 – Simulated electric field at V_{KA} = 1.2 kV in a simple JTE termination implanted with a dose of $1.3{\cdot}10^{13}$ cm^{-2} on a 4H-SiC PiN diode with a 12 μm $5{\cdot}10^{15}$ cm^{-3} n-type drift layer

The figure 2.18 shows the simulated potential at 1.2 kV at the end of the JTE for the same diode and JTE with JTE rings. We can see that the JTE is not totally depleted as the equipotential lines do not spread in it and the JTE rings act like guard rings by separating the equipotential lines at the end of the JTE.

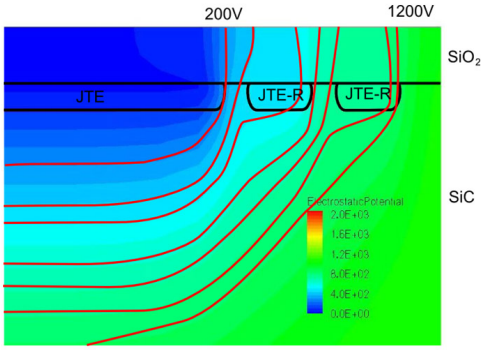

FIGURE 2.18 – Simulated potential on the JTE with JTE Rings at 1200 V

In the figure 2.19, we can see the simulated electric field in the termination with JTE rings at 1.2 kV. We can see that the electric field is fairly reduced by the presence of the JTE rings, so the breakdown voltage of the termination with the same JTE dose is increased. It allows the JTE to reach the reverse bias required to deplete it completely and thus increase the JTE dose threshold.

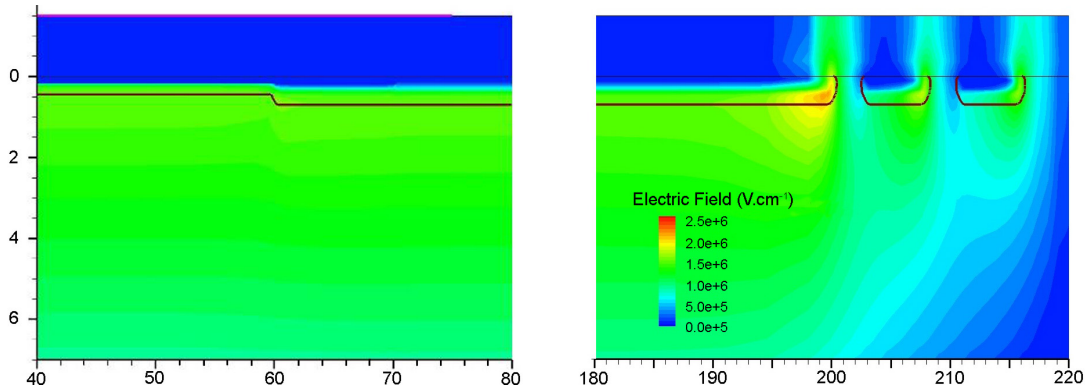

FIGURE 2.19 – Simulated electric field at V_{KA} = 1.2kV in a termination with JTE and JTE Rings implanted with at $1.3{\cdot}10^{13}\text{cm}^{-2}$ on a 4H-SiC PiN diode with a 12 μm $2{\cdot}10^{15}\text{cm}^{-3}$ n-type drift layer

With GR the field crowding effect obliges to reduce the space between the rings and reduce their efficiency at the same time. The low doping level of the rings permits the ZCE area to expend further into the rings and thus creates a wider resistive area around them, reducing the field crowding effect. So we do not need to minimize the distance between them and their efficiency is far less sensitive to it. We performed simulations of the same diode with five JTE rings at different JTE doses in order to compare its dose

tolerance to the simple JTE's. The resulting breakdown voltage versus JTE dose for the JTE with JTE rings compared to the simple JTE is presented in figure 2.20.

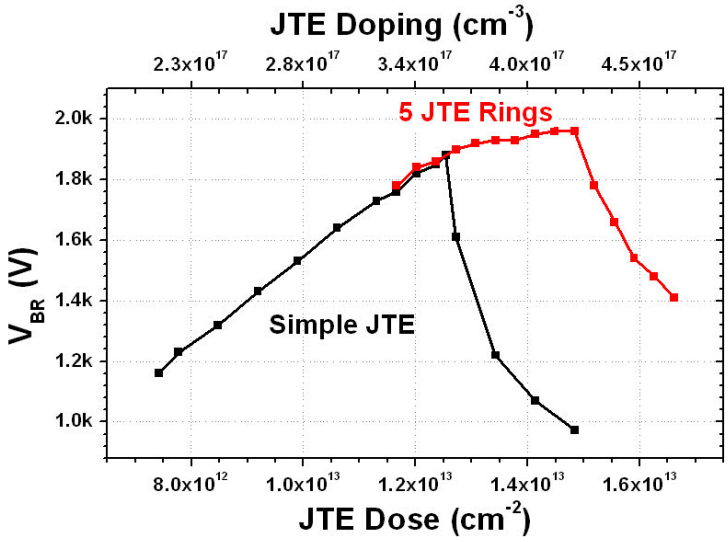

FIGURE 2.20 – Breakdown voltage as a function of JTE dose for a PiN Diode with a 12 μm $2{\cdot}10^{15}$ cm^{-3} n-type drift layer with a simple JTE (black) and JTE Rings (red)

We can see that, compared to the simple JTE, the JTE rings are more tolerant toward the JTE dose. It also shows that the breakdown capability of the termination is not improved under the JTE dose threshold. Whichever the JTE dose, the electric field at the JTE end is reduced by the JTE rings. This will minimize the stresses on the passivation layers and interfaces over the periphery of the JTE. The implanted and associated JTE dose can vary depending on the position on the wafer ; consequently the breakdown capability of the termination varies. Due to annealing non-uniformity, the proportion of associated impurities can vary from 50% to 80% on a whole wafer. One must take this effect into account and implant a JTE dose that will give an active doping concentration under the dose threshold in most cases. This margin obliges to reduce the breakdown voltage in order to assure a good fabrication yield. The JTE rings increase the JTE dose threshold, so that one can increase the implanted dose for the JTE and thus increase the overall breakdown voltage of the terminations. Higher voltage chips have thicker epitaxial layer with lower doping but the implantations depth can not increase lest using higher implantation energies, which is more destrutive to the crystal and requires non-standard apparatus. The JTE depth and lateral junction being similar, the field crowding is even more susceptible to occur at the end of the JTE. Standard JTE terminations and terminations made of JTE with JTE Rings were simulated on PiN diodes with thick epitaxial layers with different JTE doses. The figure 2.21 presents the variation of the simulated breakdown voltage as a function of the JTE dose of both

terminations for two different drift layers. Diodes with these drift layers parameters have been fabricated at CNM and results are presented in the chapter 3.

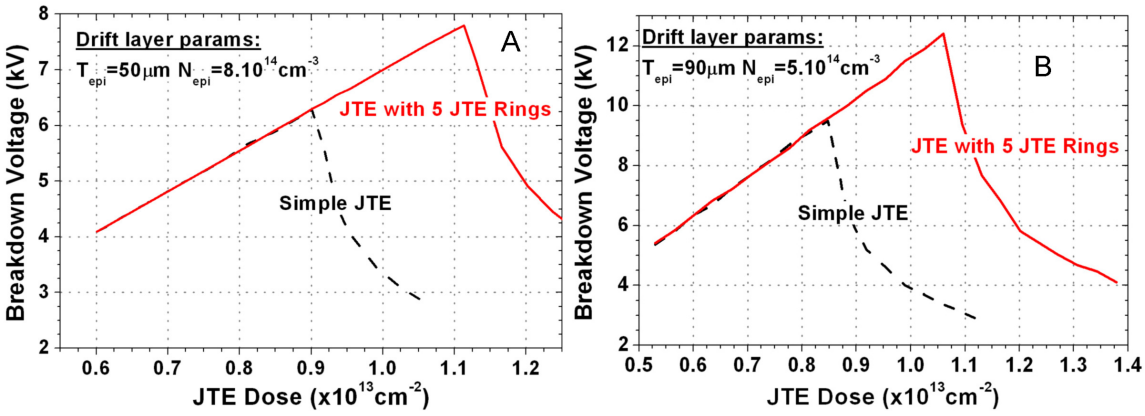

FIGURE 2.21 – Breakdown voltage as a function of the JTE dose for two different drift parameters with a simple JTE and 5 JTE Rings

We see that the JTE Rings' efficiency compared to standard JTE increases with thicker drift layer. 95% of the breakdown voltage of the 1D PiN diode was reached on figure 2.21A.

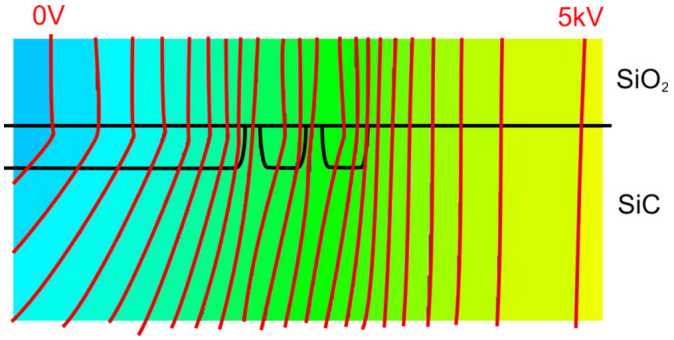

FIGURE 2.22 – Equipotential lines in termination with two JTE Rings on a 6 kV diode reverse biased at 5 kV

The figure 2.22 shows the potential captured a simulated termination with 2 JTE Rings and one JTE with dose above the simple JTE dose threshold, for a PiN diode with a drift layer of 50 μm and doped at $8{\cdot}10^{14}$ cm^{-3}. We can see that the equipotential lines pass through the JTE rings ; when the JTE rings are completely depleted, they create a highly resistive area, so the equipotential lines are separated inside them as shown on the figure 2.22. Usually, high voltage SiC chips above 3 kV are fabricated with Multiple JTE [11, 34] or Modified JTE [84], requiring multiple implantations or etching steps. The JTE rings termination requires only one implantation step with fine layout definition. Schottky diodes fabricated on 4 kV wafers with different JTE dose have proved the functionality of the JTE rings, these experimental results are presented in the

chapter 3. The JTE Rings increase the JTE dose threshold, on very high voltage chips it also increases the maximum reverse bias capability of the JTE termination and reduces the electric field on its periphery. It is a promising termination for very high voltage chips as it reduces the process complexity and increases the chips reliability.

2.1.6 Combination of different terminations

Most of different terminations presented before can be combined in order to take advantages of each one. The Modified JTE (MJTE) is already a combination of the JTE and the Mesa termination, no report has been made of the combination of the MJTE with the AGR or the JTE Rings but this is a termination which surely would function perfectly. We have extensively used the combination of JTE, AGR and JTE Rings as illustrated in figure 2.23 and we obtained good results as will be exposed in the chapter 3.

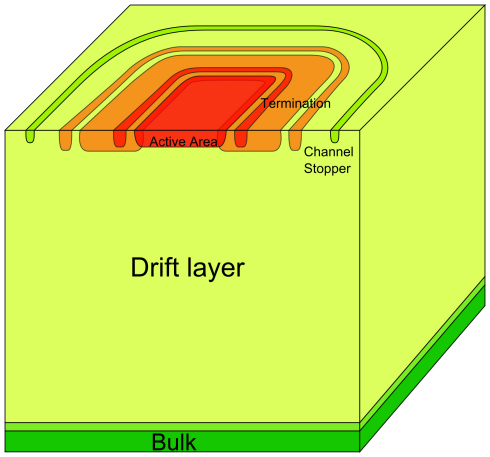

FIGURE 2.23 – Combination of JTE, AGR and JTE Rings on a PiN diode

The figure 2.24 presents the breakdown capability of a PiN diode with JTE, and 5 JTE Rings or/and 3 AGR as a function of the JTE dose. The combination of the JTE, 3 AGR and 5 JTE Rings is represented with the dotted curve, we can see that the different beneficial effect of the JTE Rings and the AGR are combined giving a higher JTE dose threshold, and breakdown voltage for a given JTE dose.

The simple JTE and the JTE Rings terminations were also simulated with two different values of lateral diffusion (L_{DIFF}), the dose threshold is increased with a higher diffusion. However, the JTE rings permit to elevate the JTE dose threshold far higher than any enhanced lateral diffusion can do.

The Table 13 summarizes and quantifies the advantages and disadvantages of the aforementioned planar terminations.

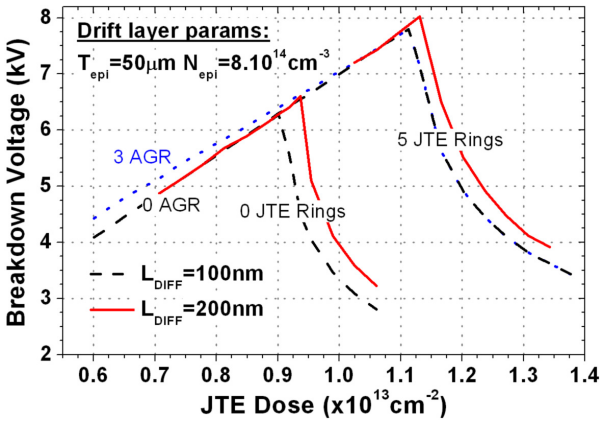

FIGURE 2.24 – Simulated breakdown voltage of different planar termination with a 4H-SiC vertical PiN diode

Termination	JTE Dose tolerance	Position and size tolerance	Number of process steps
GR	No JTE	-	0
JTE	-	+++	1
AGR	+	+	1
JTE Rings	+	++	1
AGR & JTE Rings	++	++	1

TABLE 2.1 – Advantages and disadvantages summary of presented planar terminations

2.1.7 Conclusion

This study has led to the design of planar termination associating JTE, AGR and JTE Rings to protect the periphery of the chips efficiently over 10 kV with a minimum of fabrication steps. Devices have been fabricated with these terminations and have shown very good reverse capability up to 9 kV. Many tuning of the design are still possible, the termination has only been tested on JBS and Schottky diodes with JTE dose barely over the simple JTE dose threshold and should prove to be even more effective in the future experiments. New experiments combining the JTE Rings, the mesa and the JTE on 10 kV PiN diodes have been started and should add exceptional results to the SiC technology.

2.2 Vertical Implanted and Epitaxied Metal Oxyde Field Effect Transistor (VIEMOS)

We conducted simulations of the VIEMOS structure with different dimensions to study their influence on the forward and reverse characteristics of the device. The figure 2.25 shows a vertical cross section of a VIEMOS cell with the different notations used for the design parameters in the results we will present.

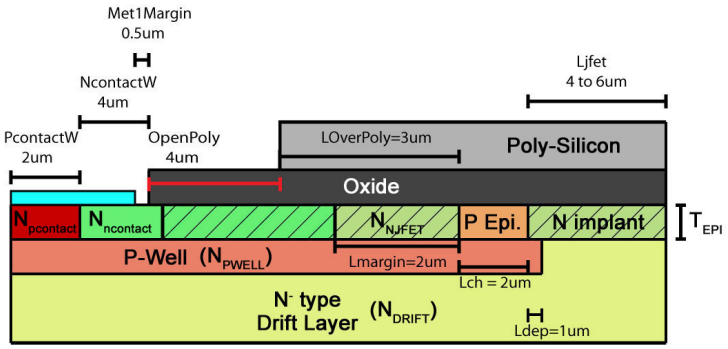

FIGURE 2.25 – Schematic cross section of the VIEMOS cell. The Red and orange areas are the p-type areas, the green and yellow are the n-type ones. The blue is used for the metallic layer, the dark grey for the gate oxide and the light grey for the polysilicon gate

The VIEMOS structure was first presented in 2005 by researchers of AIST [HARA'05] as a mean to fabricate a SiC VMOS without implanting the channel region and thus reducing the generated defects in the channel. The presented devices showed high channel mobility and low on-resistance. The device is created by epitaxying a thin P-type layer after the PWell implantation and compensating the JFET area with an N-type implantation. The rest of the device is fabricated like the VDMOS. As the JFET area is implanted with a higher dose of N-type impurities than the drift layer in order to compensate the P-type epitaxial layer, it makes this area less resistive but, when reverse biased, the depletion region deploys less in this region, which reduces the protective effect of the PWell on the JFET area. So the variation of the JFET length (L_{JFET}) will have a strong impact on the structure. The critical step of the process is the formation of a thin P-type epitaxial layer since its thickness and doping concentration has an influence on the forward characteristics of the MOSFET. In this sense, the PWell area can be extended under the JFET area to protect it, or P strips can be inserted between the PWell to protect the area. These different parameters and structure variations have been simulated with a bi-dimensional model of the VIEMOS under forward and reverse bias. It is known that the Coulomb scattering has a strong negative effect on the channel mobility, as the simulator did not model it, we reduced the channel mobility by the combination of surface roughness scattering and a strong phonon scattering. Initial simulation of the structure

permitted to choose a reference structure. The standard structure parameters are given in the Table 14.

PcontactW	NcontactW	Met1Margin	OpenPoly	LOverPoly	Lmargin
2 μm	4 μm	0.5 μm	4 μm	3 μm	2 μm
L_{CH}	L_{JFET}	L_{DEP}	T_{EPI}		
4 μm	4 μm	0 μm	0.3 μm		
$N_{pcontact}$ (cm^{-3})	$N_{ncontact}$ (cm^{-3})	N_{PWell} (cm^{-3})	N_{p-epi} (cm^{-3})	N_{JFET} (cm^{-3})	N_{DRIFT} (cm^{-3})
$1{\cdot}10^{19}$	$1{\cdot}10^{19}$	$5{\cdot}10^{18}$	$5{\cdot}10^{16}$	$1{\cdot}10^{17}$	$5{\cdot}10^{15}$

TABLE 2.2 – Main design parameters of the VIEMOS reference structure dimension of VIEMOS simulation

All the simulations have been conducted on 2D structures with a channel width of 1μm and a total length of 16μm for the standard cell. One can then make estimation of the future maximum capability of the MOSFET by multiplying the current with the channel width of the active area of the fabricated chip divided by 16μm^2. With those dimensions, a power MOSFET with an active area of 1mm^2 can totalize 40 mm of channel.

2.2.1 Variation of the thin P-type epitaxial layer parameters

We first simulated the forward characteristics of the VIEMOS with different values for the p-type epitaxial layer thickness (T_{EPI}). The figure 2.26 shows the forward characteristics for different thickness of the epi at different gate bias. At V_{GS} = 5 V, we can see that the VIEMOS's resistance does not vary before the drain current saturation ; however the saturation level varies much with the epitaxial thickness. For higher gate bias, the inverted area of the channel is larger, the channel is more difficult to pinch-off, so saturation appears at far higher drain bias (see figure 2.26b).

We then simulated the reverse characteristics of the VIEMOS with different epitaxial layer thickness. In figure 2.27, the obtained breakdown voltage is plotted as a function of the epitaxial layer thickness.

We can see that the breakdown voltage decreases when the epitaxial layer is larger. Looking at the simulated ionization in the structure, we can see that an ionization peak occurs at the p-well corner under the JFET region. By reducing the epitaxial layer thickness, we reduce the equipotential lines bending in the JFET area and thus reduce the field crowding on the p-well corners.

We also simulated the effect of the epitaxial layer doping (N_{EPI}) on the forward characteristics of the VIEMOS. The figure 2.28 shows the simulated I-V characteristics

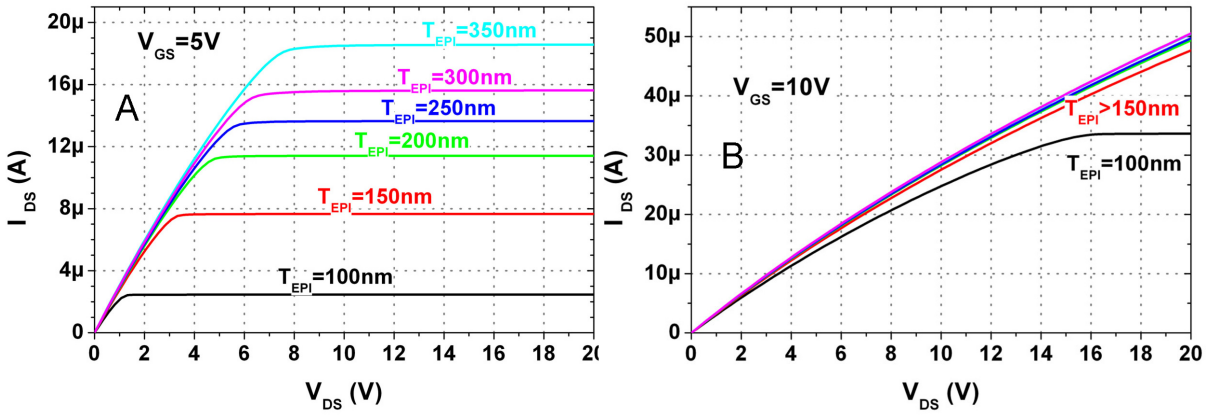

FIGURE 2.26 – Forward characteristics of VIEMOS for different P-type epitaxial layer thickness

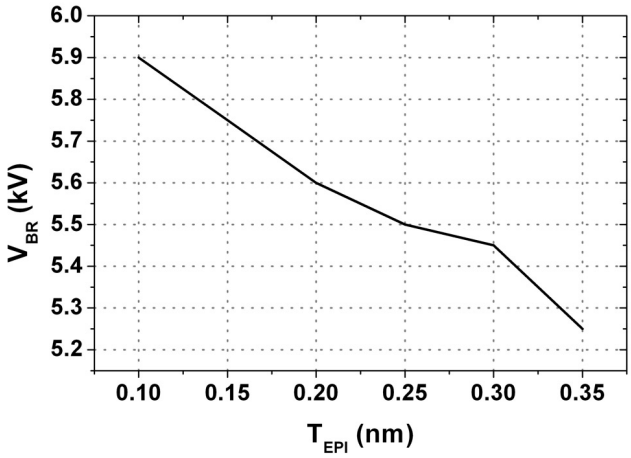

FIGURE 2.27 – Breakdown characteristics of the active area of the VIEMOS for different P-type epitaxial layer thickness

of devices with different P-epitaxy doping concentration at $V_{GS} = 5V$ and $V_{GS} = 10V$. The drift's resistance dominates ($65m\Omega.cm^2$), so we cannot see the variation of the on-resistance.

However, we can see that the channel doping has a strong influence on the saturation level of the drain current.

2.2.2 Impact of JFET's length

On VDMOS, we know that the JFET area induces a parasitic resistance into the device, this resistance can be modulated by the JFET area length (L_{JFET}). However, this distance is also important when the VDMOS is reverse biased ; the depletion layer between the PWell permits to pinch the JFET channel and protect the gate from high electric fields. If the p-wells are too far from each other, the JFET area cannot be fully depleted and the gate is not protected, moreover, equi-potential lines bending around the

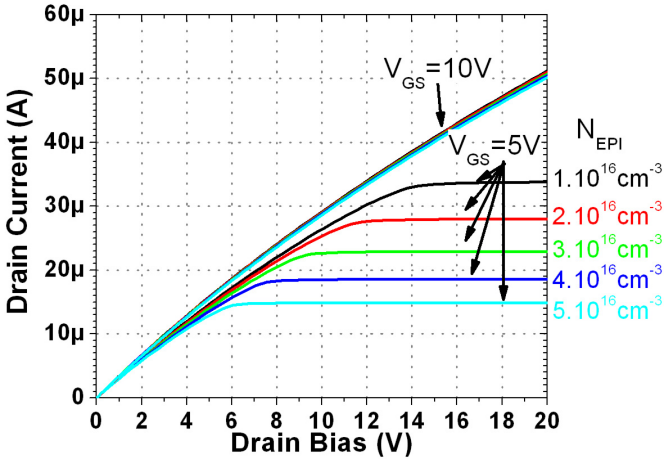

FIGURE 2.28 – forward characteristics of the VMOS simulated with different doping concentration of the thin surface p-type epitaxial layer

p-well tip on each extremity of the JFET area create field crowding. The mechanism is exactly the same on VIEMOS, however the top part of the JFET area is more doped, which can sensitise the VIEMOS structure toward the JFET area's length.

We first simulated the forward and reverse characteristics of the VIEMOS structure with different L_{JFET}. We show the breakdown voltage and on-resistance of the device as a function of the JFET length in figure 2.29a where we can see that the reverse capability and on-resistance of the device decrease with L_{JFET} and both saturate above $L_{\mathrm{JFET}} = 4\ \mu$m around $\rho_{\mathrm{ON}} = 50\ \mathrm{m\Omega.cm^2}$ and $V_{\mathrm{BR}} = 5.3$ kV. So the ideal JFET length is between 3 and 5 μm.

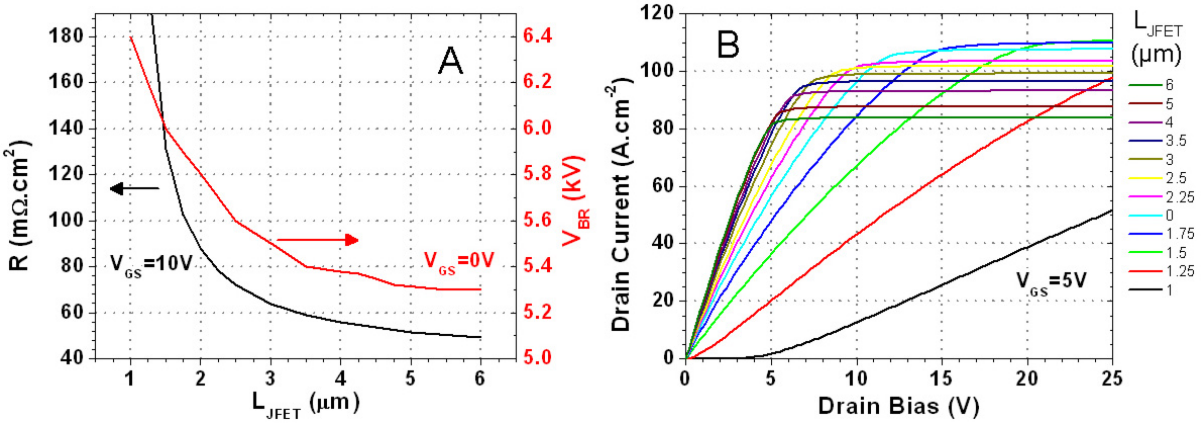

FIGURE 2.29 – JFET Area length influence on reverse and forward characteristics of the VIEMOS

The figure 2.29b shows the I-V characteristics of the devices at $V_{\mathrm{GS}} = 5$V. One can see an increase in the drain saturation voltage and current with the decrease in the JFET area length. The saturation voltage increases because the channel sees a lower voltage

bias as the channel length increases. The saturation of the drain current density increases because the cell's size decreases.

2.2.3 Optimal implantation Dose for JFET area compensation

The JFET area of the VIEMOS must be implanted with N-type impurities to compensate the thin P-type epitaxial layer, so the JFET doping (NJFET) must be higher than the p-type epitaxial layer ($2{\cdot}10^{16}$ cm^{-3}). However, the doping concentration in the JFET area determines the extension of the depletion between the PWell and thus the protection of the gate by the PWell. It also affects the JFET area resistance (RJFET). The forward and reverse characteristics of the VIEMOS structure have been simulated for different values of N_{JFET} between $1{\cdot}10^{17}$ cm^{-3} and $4{\cdot}10^{17}$ cm^{-3}. The breakdown voltage as a function of N_{JFET} is shown in figure 2.30a, we can see that the breakdown voltage of the VIEMOS drops for N_{JFET} superior to $2{\cdot}10^{17}$ cm^{-3}.

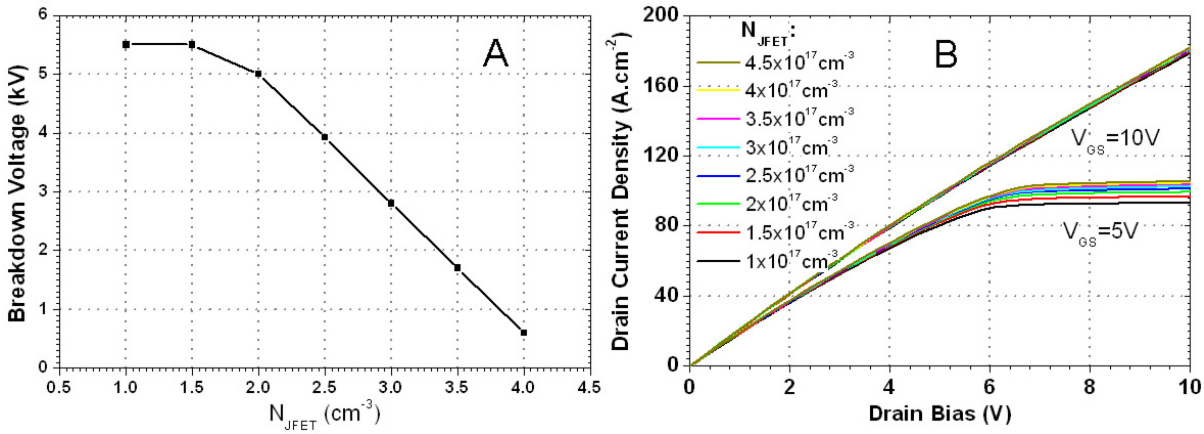

FIGURE 2.30 – JFET doping concentration influence on reverse (a) and forward (b) characteristics

In figure 2.30b, we can see the I-V characteristics of the VIEMOS at $V_{\mathrm{GS}} = 5$ V and $V_{\mathrm{GS}} = 10$ V for different N_{JFET}, we can see that neither the on-resistance nor the saturation current are influenced by the JFET area concentration. We must also notice that by increasing the JFET doping concentration we increase the capacitance between drain and gate. So the JFET compensation must be kept as low as technologically possible to avoid early breakdown in the JFET area.

2.2.4 PWell overlap of the JFET area

In the VIEMOS structure, the p-well and the channel are defined at different steps of the fabrication process with different layouts, so that the end of the p-well does not have to correspond to the end of the channel. Overlapping the JFET area with the p-well (L_{DEP}) can provide a better protection at lower JFET resistance's cost compared to the simple reduction of the JFET area length. If the p-well stops before the channel, the current path is less pinched off at the p-well depth so that the JFET resistance is reduced. The channel and the p-well can be misaligned ; if the channel is short, it could lead to vertical leakage current, the overlapping of the JFET area provides better tolerance toward this misalignment. The VIEMOS structure with different placement of the p-well under the channel has been simulated under forward and reverse bias, and the extracted results are presented in figure 2.31.

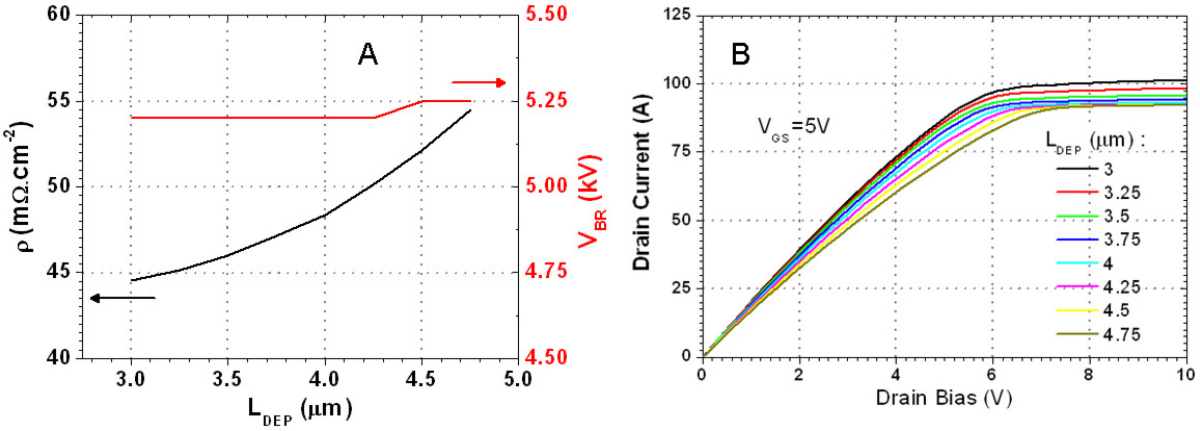

FIGURE 2.31 – P-well overlap dimensions influence on MOSFETs reverse and forward characteristics

The figure 2.31a shows that the reverse characteristics do not vary with the p-well extension under the channel. Since the JFET length is small, it does not need extra protection from the p-well. The p-well location influences the JFET so that its resistance increases by 100% when extending the p-well 0.75 μm after the channel end, and reduced by 50% when stopping 1 μm before it. The figure 2.31b shows that the saturation current increases when the p-well stops before the channel.

2.2.5 Summary

The simulation of the SiC VIEMOS with different dimensions allows seeing the influence of different crucial design parameters on the device's performances. Some of the results obtained of the VIEMOS are also valid for the VDMOS structure.

We have seen that, for a standard JFET area's length of 5 μm, the breakdown capability of the device is reduced when the JFET doping concentration is superior to $2{\cdot}10^{17}$ cm^{-3}. So the compensation of the p-type layer on the VIEMOS must be operated with high precision. On the VDMOS, the JFET area's doping is the same as the drift layer's doping, which is inferior to $1{\cdot}10^{17}$ cm^{-3}, so it is not a problem.

We have also shown that the JFET area's length has concurrent influence on the blocking capability and on-resistance of the VIEMOS. For a JFET concentration of $1{\cdot}10^{17}$ cm^{-3}, a JFET length of 4 μm is a good compromise between the on-resistance and breakdown capability.

The thickness of the epitaxial layer has an influence on both the channel's depth and JFET area's depth. We could see that the variation of the channel depth has no effect on the on-resistance of the device but influences the saturation current's level. The thickness of the epitaxial layer also determines the JFET area's depth, which influences the breakdown voltage of the device when doped at $1{\cdot}10^{17}$ cm^{-3}.

This study allowed us to choose the different dimensions of the VMOS designs created (see Annexe A), which have been fabricated, the electrical characteristics of the devices are presented in chapter 5.

Chapitre 3

High Voltage SiC Schottky and JBS diodes

3.1 Introduction

Rectifiers are key components in electronic and especially in power electronic circuitry. These devices are present in the full range of application, with voltages ranging from several volts up to tenths of kilovolts.

The internal physics of a diode is similar to transistor and integrated circuits but its basic structure is far simpler. So the first sensible step, to develop a novel semiconductor technology, is to optimize the diodes structure and fabrication process, as it is the first technological brick for further complex devices development.

In power devices applications, the diodes must be able to maintain a rectifying function over hundred volts. This requires a different structure and design compared to low voltage diodes used in integrated circuits. As we discussed in Chapter 1, typically, the power diodes must have a large drift region, vertical or lateral, to separate the equipotential lines when reverse biased.

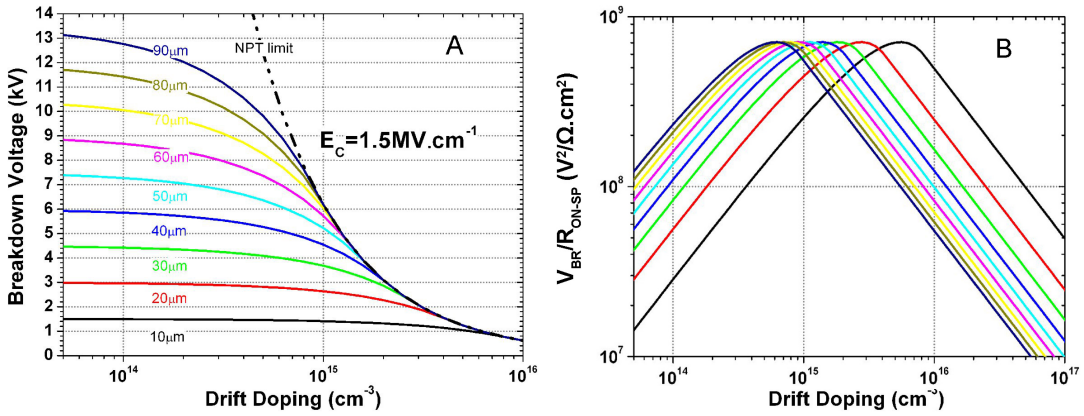

Figure 3.1 – Blocking voltage (A) and Baliga Factor of Merit (see table 1.2) (B) vs drift epilayer doping for a low critical electric field and for different drift layer thicknesses. The colours of the curves on figure 3.1B correspond to the same epitaxial layer thicknesses of the curves on figure 3.1A

As shown in chapter 1, in SiC, there exists three kind of power diodes ; the Schottky diode, the PiN diode and the JBS diode. Compared to PiN diodes, Schottky diodes are

more sensitive to the maximum electric field. On the PiN diodes, the maximum electric field is located at the P-N junction in the semiconductor's crystal, whereas in Schottky diodes, it is located at the metal/semiconductor interface. This interface creates a smaller electronic barrier to carriers, which is more sensitive to defects and charges, and will be subject to higher current tunneling phenomena when reverse biased, thus it will show far more leakage current. High density of leakage current through the schottky barrier deteriorates it, so that most of the SiC Schottky diodes show a soft breakdown.

The leakage current is dissipated thermally and induces reliability problems, so we must limit it when using the Schokttky diodes. Typically, we take a leakage current density limit of 1mA.cm^{-2}. In vertical power devices, the choice of the drift layer thickness is made by considering the graphics on figure 3.1A, which shows the maximum 1D plane breakdown voltage of a device versus its drift region thickness and doping concentration for a given critical electric field.

The V_{br} vs N_{d} graphic (see figure 3.1A) is usually based on calculation using a critical electric field value of 2MV.cm^{-1}, which corresponds to a safe estimation of the maximum electric field that can withstand the 4H-SiC material. However, previously fabricated Schottky diodes [41] reached the maximum reverse current (1mA.cm^{-2}) for a surface electric field value around 1.5MV.cm^{-1}. So we recalculated the ideal breakdown voltage as a function of the drift layer thickness for a critical electric field of 1.5MV.cm^{-1}, which results in the graphs of figure 3.1A.

The figure 3.1B represents the value BFM (see table 1.2) as a function of the drift doping for a given drift layer thickness (W_{drift}). So the maximum of each curve indicates the optimal drift doping to obtain the best BFM for a given drift layer thickness. One can see that the value of the maximum BFM is constant with respect to the epitaxial thickness and is located near the punch-through limit in the punch-through zone.

Previous studies at CNM have shown that Schottky barrier made with nickel shows forward drift voltage at high temperature due to the chemical instability of the interface [87]. Titanium, due to its lower barrier height, exhibits high reverse leakage current. Tungsten on SiC presents a barrier height superior than the titanium and shows very stable behaviour at high temperature [88]. As a consequence, in the new generation of diodes developed in this work, we selected Tungsten as the Schottky barrier metal in order to reduce the reverse leakage current and fabricate Schottky and JBS diodes with very high breakdown voltage and high temperature capability.

The objective of the work presented below was to optimize the design and technology of high voltage diodes with breakdown voltage capability ranging from 3.3kV up to 10kV. For this purpose we followed the methodology described below :

– Design of optimized mask set with variation of the geometrical parameters to observe their influence on the characteristics

– Diodes fabrication optimizing the technological parameters (mainly implantation doses, passivation layers and metallization schemes)
– Devices static electrical characterization at room and high temperature
– Devices dynamic characterization on packaged parts at room and high temperature

3.2 Large area Schottky diodes with Ni Schottky metal

3.2.1 Design and fabrication

The first large series of Schottky diodes we fabricated on 3 inches wafers were 19mm^2 large with a Schottky barrier made with nickel. As an example, I will present the wafer ALS5, where the diodes were fabricated on a 8°-off 4H-SiC wafer with a 30μm thick epilayer doped $1 \cdot 10^{15}$cm^{-3}.

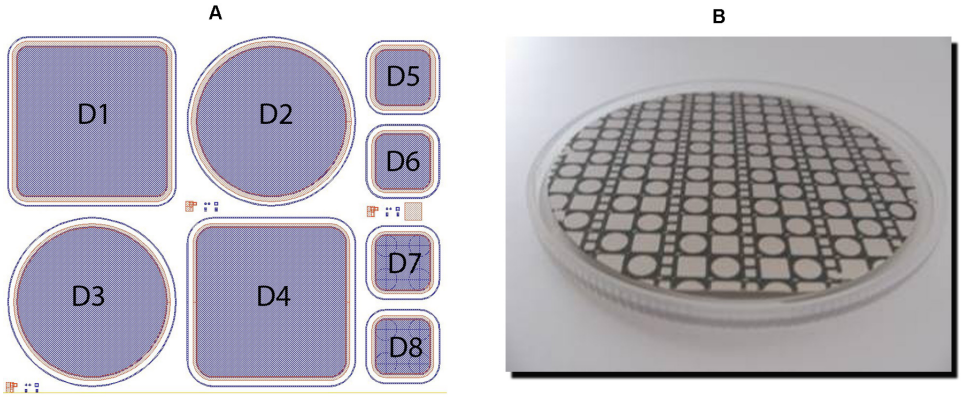

FIGURE 3.2 – Basic field (a) of the layout CNM_SIC016 used on ALS5 wafer (b)

We used the mask CNM_SIC016 to create 8 Schottky diodes by basic field ; two large squared with an active area of 19mm^2, 2 round with an active area of 15mm^2 and four small devices with an active area of 2.48mm^2. The internal structure of the diodes is presented in figure 3.3.

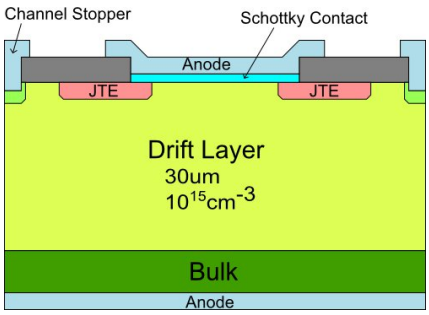

FIGURE 3.3 – Structure of the Schottky diode fabricated with the mask set CNM_SiC016

We can see that the diodes termination is made of a simple JTE. The Schottky barrier is made of a 150nm layer of nickel deposited by sputering and defined by a lift-off, followed by the sputering deposition of thick layer of Aluminum, defined by RIE etching. Its whole fabrication process includes 6 major fabrication steps.

3.2.2 Reverse characteristics

The wafer was immersed in a Galden bath and all the large diodes (D01 to D04) of ALS5 were characterized under reverse bias up to 2kV. The chips were classified in 5 categories depending on the exhibited reverse bias for a maximum leakage current of 10μA. Results are reported in the wafer mapping presented by figure 3.4. The chips coloured in white have not been characterized.

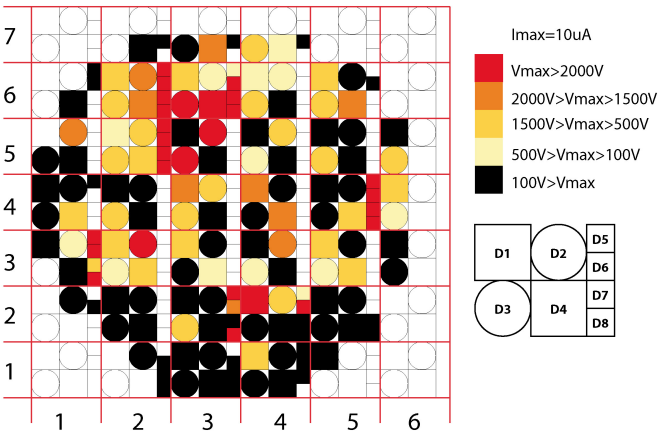

FIGURE 3.4 – Reverse leakage current mapping of wafer ALS5

We can see that only 7 of the large diodes show a leakage current below 10μA for a reverse bias of 2kV (red diodes). The majority of the chips (36 of 97) show blocking capability between 500V and 2kV. Looking at the reverse leakage current of the different class of diodes, one can see that the best type of diodes (see figure 3.5a) show very low dispersion of the reverse characteristics, contrarily to the lower class of chips (see figure 3.5B which show different levels of leakage current.

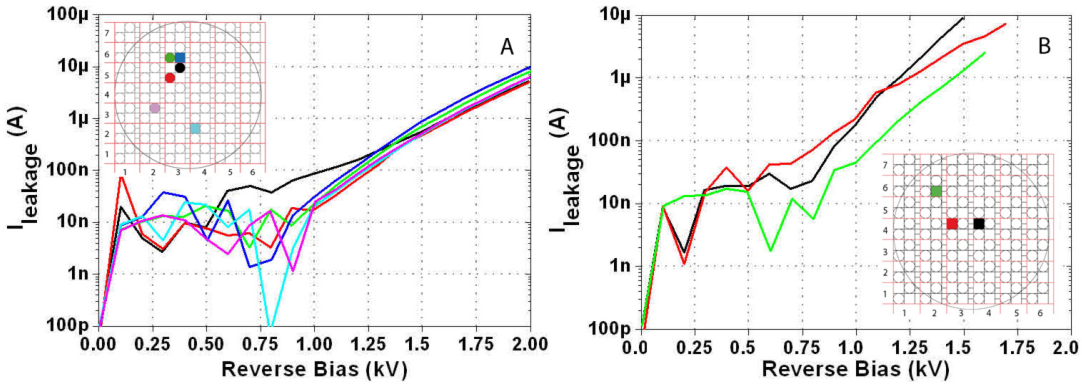

FIGURE 3.5 – Reverse characteristics of the first class (A) and second class (B) of 19mm^2 diodes from ALS5

This effect is due to the defects which locally weaken the Schottky barrier, increase the leakage current and reduce the lifetime of the chips. The probability of having a point

defect on a chip is exponentially proportional with its size, so their is a higher proportion of smaller diodes, on the right side of the field (D5 to D8), that show low leakage current up to 2kV as shown in figure 3.6.

At 2kV, good diodes of 19mm^2 show a reverse current around 10μA while diodes with an active area of 2.48mm^2 exhibit a leakage current around 2μA. The proportionality factor between the leakage current of the large and the small diodes ($I_{\mathrm{D1-D4}}/I_{\mathrm{D5-D8}} = 5 \pm 1$) corresponds well with their Area ratio ($A_{\mathrm{D1-D4}}/A_{\mathrm{D5-D8}} = 6 \pm 1$), and not with the contact perimeter ratio ($P_{\mathrm{D1-D4}}/P_{\mathrm{D5-D8}} = 2.75 \pm 0.3$).

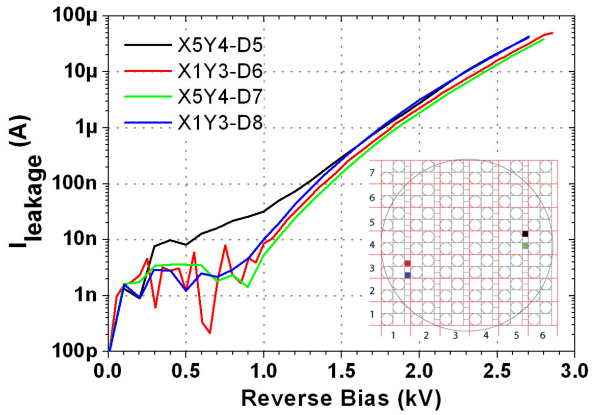

FIGURE 3.6 – Reverse capability of small diodes (2.48 mm^2) on ALS5

The leakage current comes from the Schottky contact area ; it is a combination of the tunneling current and the thermionic field emission through the Schottky barrier. The thermionic field emission mechanism dominates in the working range of the diodes, it is exponentially proportional with the temperature and the Schottky barrier height, so we can reduce it by using a contact metal with a higher Schottky barrier. The diodes production yield is strongly deteriorated by the point defects (material and processing defects), so that it can be increased by reducing the size of the chips as experienced in the next designs.

3.3 Fabricated samples with tungsten as Schottky metal and smaller active area

Considering the previous results we created two new mask sets presented in annexe A (CNM_SIC026 and CNM_SIC027) with smaller devices and innovative designs.

The masks set CNM_SIC026 permits to fabricate planar diodes with an active area of 4.4mm^2 and a termination up to 400μm long, which allows designing terminations theoretically able to sustain more than 10kV.

The second masks set CNM_SIC027 was designed to produce smaller diodes of lower blocking voltage capability, so their active area measures 2.25mm^2 and there is 300μm of space available for the termination.

In order to try different designs of termination or JBS, we realized different versions of certain levels for the two mask sets.

For comparison, innovative planar terminations presented in chapter 2.1, as JTER and AGR (see part 3.7), were included at the same time as simple JTE. We also varied the size of the JTE and the number of JTER and AGR. In the case of JBS, we also optimized the shape and geometry of the p$^+$-wells used to implement the bipolar component of the JBS (see Annexe A).

As explained in the introduction of this chapter, tungsten, as a Schottky metal on SiC, presents several advantages over classically used metals, so we used it for our new generation of diodes. It is also worth mentioning that it had never been used to fabricate JBS diodes on SiC.

3.3.1 1.2kV JBS and Schottky diodes

We fabricated 1.2kV Tungsten barrier Schottky diodes using the masks set of CNM_SIC026 described in the table 1 of the annexe A. The diodes were fabricated on a 3 inches 8° off 4H-SiC wafer with a $12\mu m$ $5\cdot 10^{15}\mathrm{cm}^{-3}$ n-type epitaxial layer. The theoretical epitaxial layer resistance is around $2\mathrm{m}\Omega.\mathrm{cm}^2$, this wafer was referenced as ALS11.

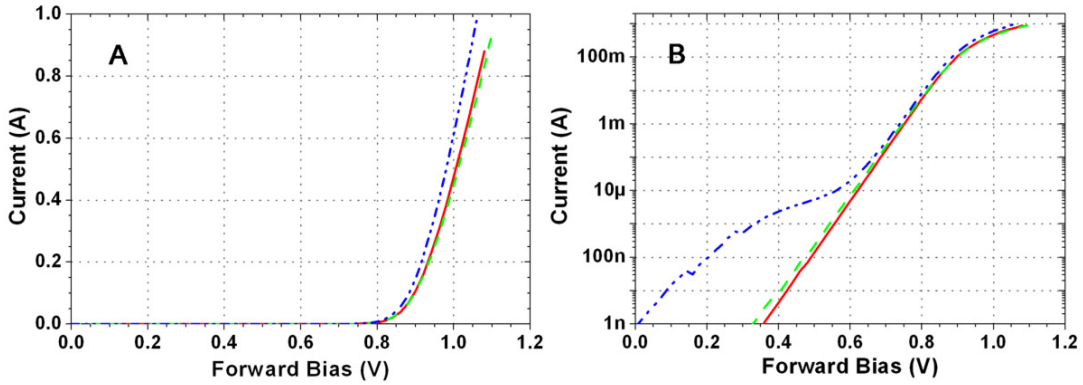

FIGURE 3.7 – Forward characteristics of Schottky diodes on ALS11 represented on (A) linear scale and (B) logarithmic scale

We captured under probe the static forward characteristics of 50 diodes up to 1A with a Keithley ki2410 connected in kelvin configuration. More than 10% of the fabricated Schottky diodes show a double barrier as shown by the blue curve of figure 3.7B. On the Schottky diodes without double barrier, the ideality factor value is between 1.0 and 1.25, with a Schottky barrier of 1.2eV, which is quite similar to the theoretical value of 1.19eV of tungsten. Similar results were observed in other fabricated samples as we will see in the next parts.

We also performed the reverse characteristics up to 600V of all the diodes on ALS11 and we sorted the diodes in five categories depending on their leakage current at 600V and produced the mapping shown in figure 3.8B.

We can notice that, in the center of the wafer, only one diode exhibit a leakage current between 50nA and 100nA and all the other samples show high leakage current or very low leakage current. We will see in the part 3.3.3 that this leakage current threshold permits to perform a screening.

We measured the reverse characteristics up to 1.5kV for the Schottky diodes with a reverse current under 50nA at 600V. To do so we used a 12kV voltage source (HV1200) connected in series with a ki2410 as a current sensor. A majority of these diodes could block 1.2kV and the best devices broke at 1.5kV as shown in figure 3.8A. At 1500V, the calculated electric field present at the Schottky contact is $1.5MV\cdot cm^{-2}$.

We can also see that the leakage current level is similar on those samples, which means that they present a minimal number of irregularities.

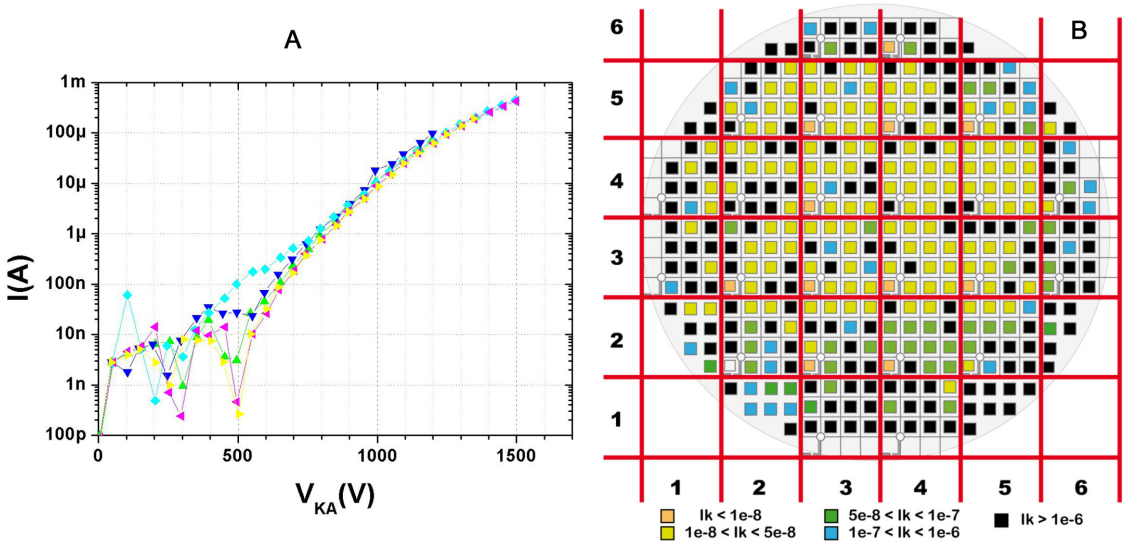

FIGURE 3.8 – (A) Reverse characteristics of 5 Schottky diodes with the same termination design and (B) mapping of the reverse leakage current at 600V on ALS11 wafer

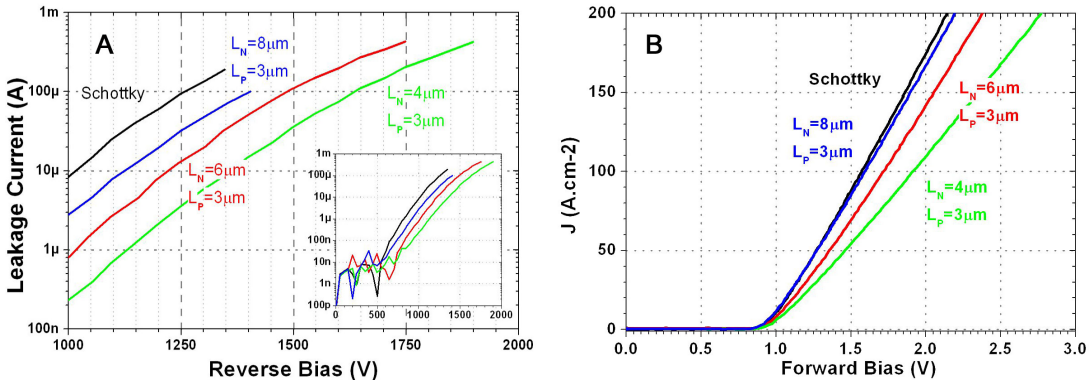

FIGURE 3.9 – Reverse (A) and forward (B) characteristics of JBS and Schottky diodes on ALS11 wafer

The figure 3.9 shows the reverse and forward characteristics of the three types of JBS compared to the Schottky diodes. The JBS diodes show similar leakage current shape, but with a lower reverse current.

As Schottky contact size decreases, the leakage current and the conductivity of the diodes also decreases. So the JBS characteristics depends on their design parameters L_S and L_P. However, one can see in the figure 3.9A and B, that it is not linearly proportional.

To observe the impact of the p-well distance on the devices characteristics, we simulated the active area of the JBS diode when forward and reverse biased.

As can bee seen in figure 3.10B, the Schottky contact is protected from high electric fields by the JBS p-wells, so the leakage current is porportional to the screening effect and not to the Schottky contact area as the standard Schottky.

Moreover, when the JBS is forward biased, the current flows through the Schottky

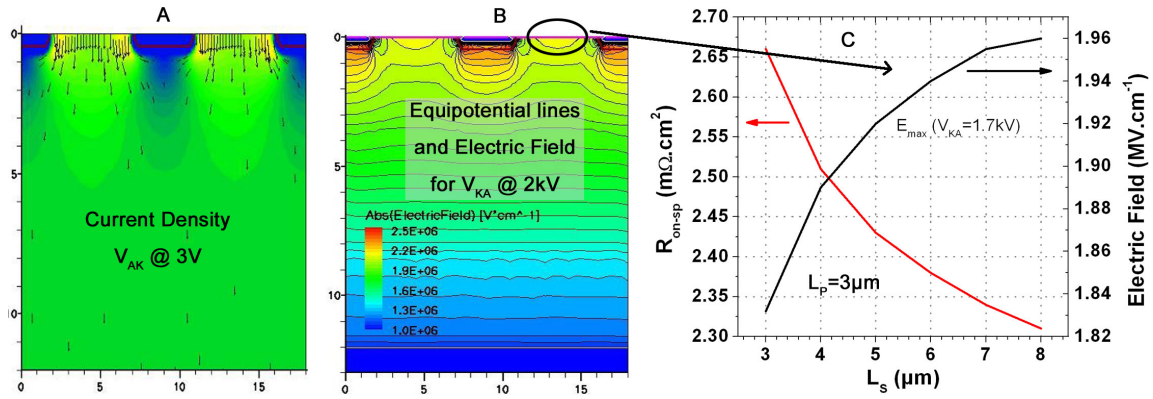

FIGURE 3.10 – Simulation of the current (A), electric field and potential (B) in a 1.2kV JBS diode ($L_S = 6\mu$m and $L_P = 4\mu$m), and resistivity and electric field at the Schottky contact for $V_{\mathrm{KA}} = 2$kV as a function of the distance between the p-wells (C) extracted from simulations

contact (see figure 1.8A), between the p-wells and then spreads under them (see figure 3.10A), taking advantage of the whole epitaxial layer under the active area. Thus, the reduced Schottky contact area is partially compensated by a more efficient current distribution in the drift layer

The figure 3.10C shows that the resistance of the devices and the electric field at the Schottky contact are not linearly proportional to the distance between the p-wells (L_{S}). Moreover, above $L_{\mathrm{S}} = 8\mu m$ the screening effect is minimal for this drift layer. These variations will change with the drift layer thickness and doping.

3.3.2 4kV Schottky diodes

The first step of our study with the 1.2kV tungsten Schottky diodes showed good results, so we decided to fabricate Schottky diodes with higher blocking capability of 4kV, but with smaller active area. We used the first version of the masks set CNM_SIC027 presented in table 4 in the annexe A. This masks set produces only Schottky diodes where we implemented the innovative JTER termination as well.

We processed two 3 inches SiC wafers (named PHL2 and PHL3) with a 8°-off crystal orientation, a 45μm thick epilayer with a n-type impurity concentration of $1.5 \cdot 10^{15}$cm^{-3}. Taking an electron mobility of 800cm^2/V·s in the drift, the theoretical resistivity of the drift layer is 23mΩ.cm^{-2} and the substrate contribution is estimated at 0.4mΩ.cm^{-2}.

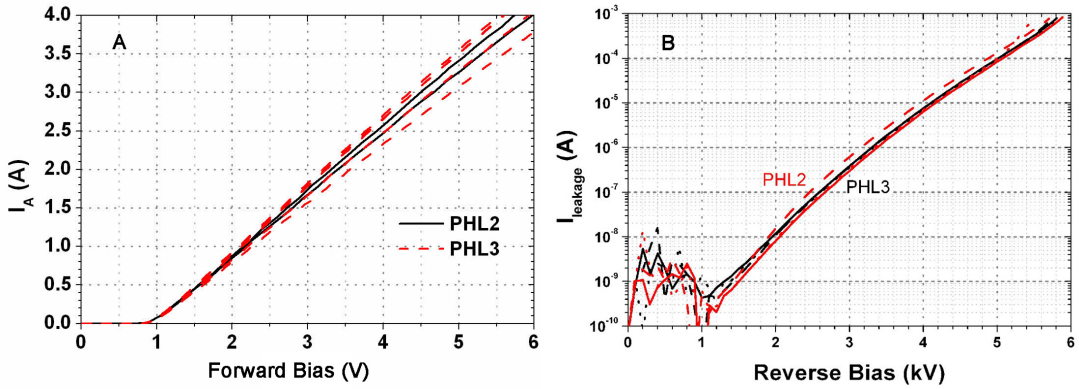

FIGURE 3.11 – (A) Forward and (B) reverse characteristics of Schottky diodes on PHL2 and PHL3 wafers

Both wafers were processed with the same technology as ALS11, which comprises the tungsten as Schottky metal. The only variation operated between the two wafers concerns the JTE implantation dose to study the JTER termination. The results of this experience will be presented in the part 3.7.3.

Forward characteristics of the devices were measured on-wafer with a Tektronixs tracer in Kelvin measurement between the anode and the chuck of the probestation's chuck. Typical forward characteristics on both wafer are shown in figure 3.11A.

The specific resistance, R_{sp}, extracted from the I-V curves of figure 3.11A, is ranging between 1.1 and 1.25Ω for an active area of 1.96mm^2, giving a resistivity between 21.5 and 25mΩ.cm^2. It fits well with the calculated epitaxial layer resistance. The ideality factor and barrier height was extracted on several diodes, and we obtained $\eta = 1.1$ and $\Phi_B = 1.22$eV in majority.

Good diodes on both wafers show similar reverse leakage current waveform and maximum reverse bias as shown in figure 3.11B. The best specimens were able to reach 5.8kV. Considering a specific on resistance of 24mΩ.cm^{-2}, it corresponds to a BFM of 5.6GVΩ^{-1}cm^2.

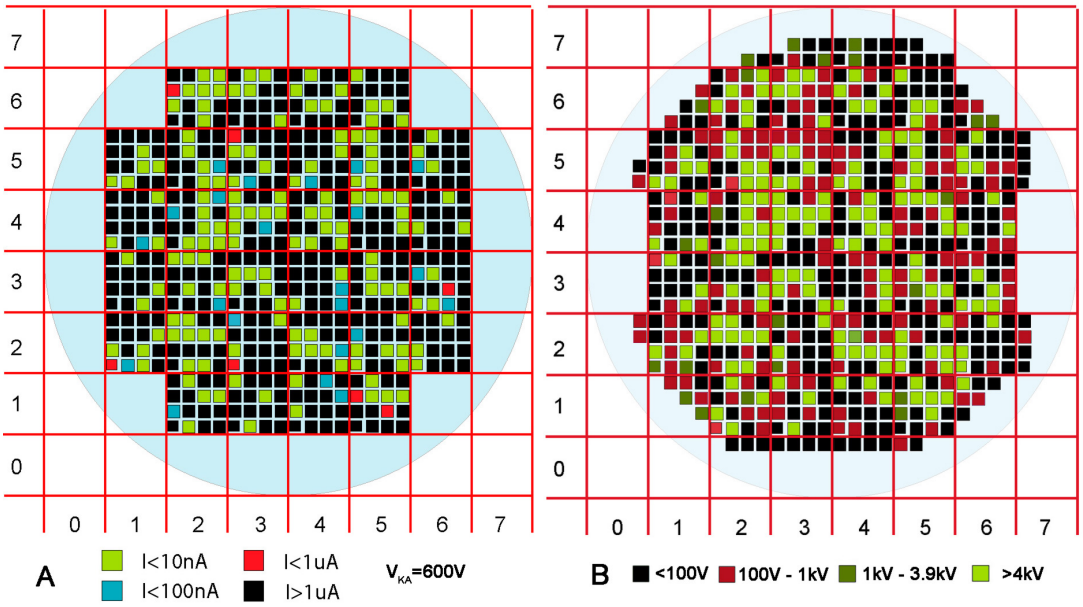

FIGURE 3.12 – (A) Preliminary leakage mapping at reverse bias of 600V and (B) blocking capability of all diodes on PHL3

Before biasing specimen over 5kV, we measured the reverse leakage current of all the diodes up 600V and we classified the diodes in 4 categories to produce the mapping presented in 3.12A. This time we also measured the reverse capability of all the devices up to 4kV and classified the devices in 4 categories to produce the mapping shown in figure 3.12B, which can be compared to the mapping at 600V.

Comparing the two mappings shown in figure 3.12, we can see that the devices showing low reverse leakage at 600V have more than 90% chance of showing reverse capability over 4kV. Screening the devices showing non-ideal leakage current at 600V permits to screen efficiently the defective devices without taking the risks inherent to the characterization at very high reverse voltage.

3.3.3 6kV JBS and Schottky diodes

We then processed three wafers (ALS10, ALS12, ALS15) with an even thicker epitaxial layer with the first version of the masks set CNM_SIC026 (see table 1 of the annexe A). The three 4H-SiC wafers were provided by CREE with an desorientation of 8°, an epilayer of 50μm doped at $8\cdot 10^{14}$cm^{-3}. Taking an electron mobility of 800cm^2/V·s in the drift, the theoretical resistivity of the drift layer is 49mΩ.cm^{-2} and the substrate contribution is estimated at 0.4mΩ.cm^{-2}.

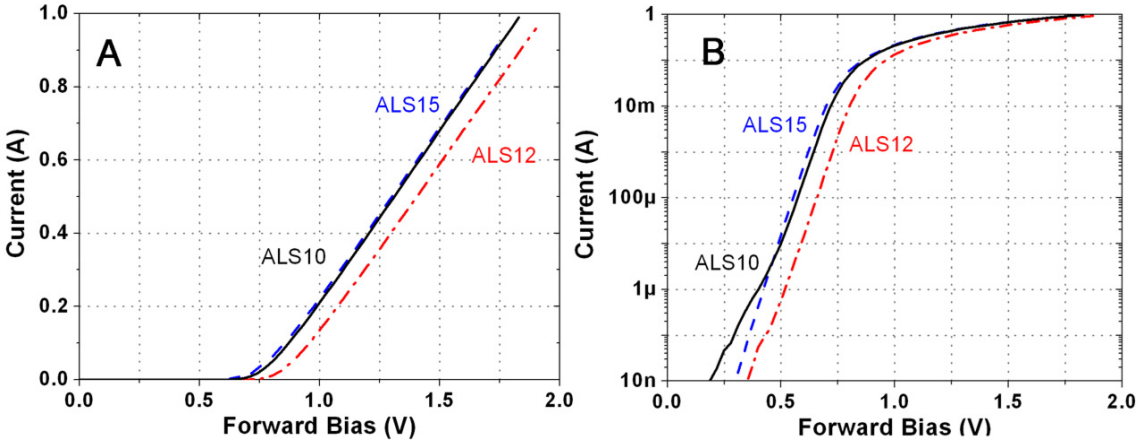

FIGURE 3.13 – Typical Forward characteristics of 4.41mm^2 Schottky diodes on ALS10, ALS12 and ALS15 represented in linear scale (A) and logarithmic scale (B)

The forward characteristics of the diodes were acquired on-wafer with a ki2420 in Kelvin measurement between the anode and the chuck of the probe-station. The devices were forward biased from 0 to 2V with a maximum current of 1A. Typical forward characteristics of the Schottky diodes are shown in figure 3.13, we can see that ALS12 shows a higher Schottky barrier ($\Phi_B = 1.18$eV) than ALS10 and ALS15 ($\Phi_B = 1.08$eV). ALS10, ALS12 and ALS15 were fabricated with the same process but separatly. The difference of barrier height can be explained by a thin native oxide layer at the Schotky metal-SiC interface on ALS12. Schottky diodes on the three wafers show an experimental specific on-resistance comprised between 48 and 50mΩ.cm^2 which corresponds very well with the theoretical drift resistance value.

The reverse characteristics also differ from ALS12 to ALS10 and ALS15 (see fig. 3.14) ; typically diodes on ALS12 show one order of magnitude less leakage current and this result stands also for the JBS diodes.

On each wafer, the reverse characteristics of all the diodes were first measured up to 300V to select the best devices. All the devices presenting low leakage current at 300V were characterized manually in Galden bath up to 4kV. The figure 3.15 shows the two mappings obtained from these measurements. As for PHL3 in the previous section, we

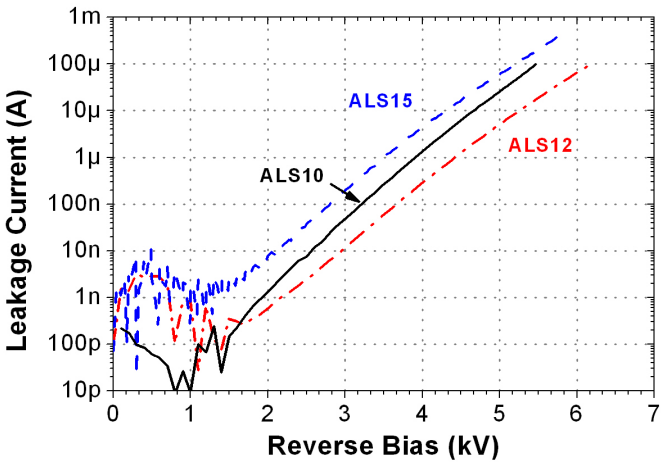

FIGURE 3.14 – Typical reverse characteristics of Schottky diodes on ALS10, ALS12 and ALS15

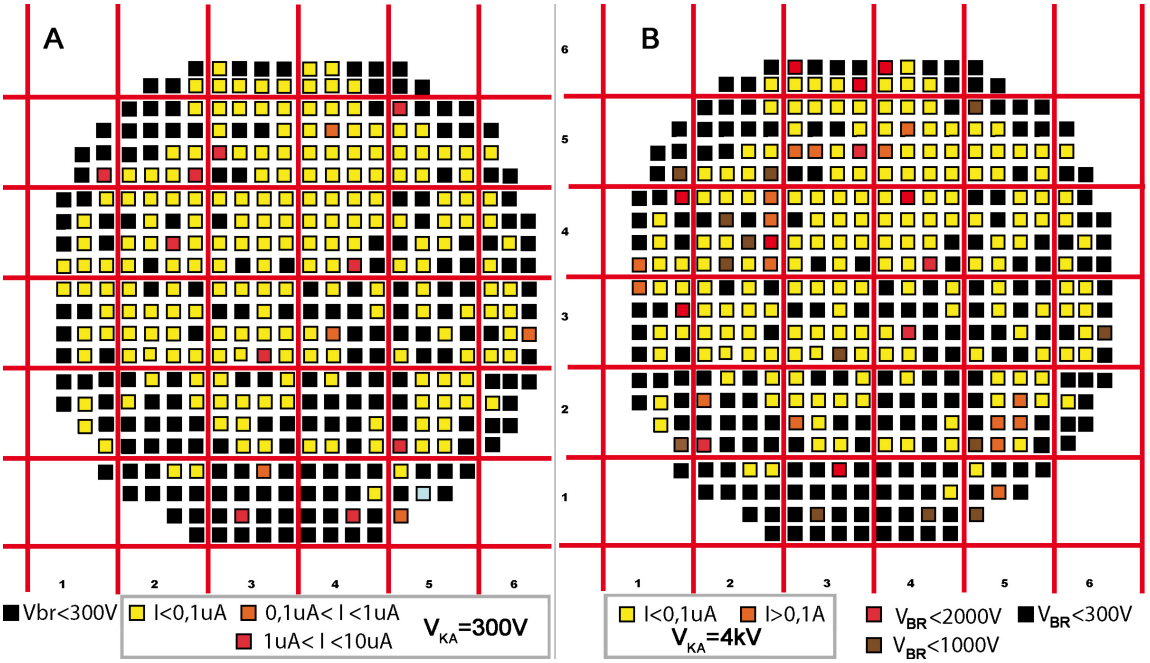

FIGURE 3.15 – ALS10 reverse current mapping at (a) 300V and (b) 4kV

can see that the low voltage characterization gives a good prediction of the results at high voltage.

3.3.4 9kV JBS and Schottky diodes

With this experiment, our goal was to fabricate JBS diodes with a reverse bias capability of 10kV on a wafer (MAX7) with n-type epitaxial layer 90μm thick with a doping of $5 \cdot 10^{14}$cm^{-3}. Taking an electron mobility of 800cm^2/V − s, the theoretical drift layer resistivity is 140mΩ.cm^2.

It was processed with the masks set CNM_SIC026, using the mask level JBS, presented in table 3 of the annexe A instead of the standard PPLUS mask level. With this mask level, 15 of the 16 diodes in a field are JBS diodes and one is a Schottky diode. We tried a new JBS design with honeycomb geometry on 5 of them.

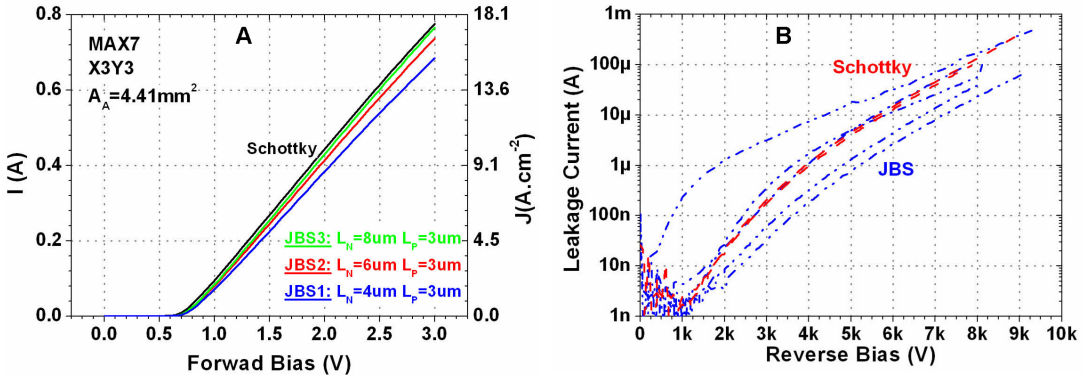

FIGURE 3.16 – (A) Forward and (B) reverse characteristics of Schottky and JBS diodes fabricated on MAX7

Diodes D02 to D16 have an active area of 4.41mm^2 and show a specific resistance between 2.6 and 3Ω. Typical forward characteristics of those diodes are shown in figure 3.16A. They can be used with a nominal current of 1A at 4V. The JBS diodes with the new design show a lower resistance than the other, so we measured the direct characteristics of all the diodes and extracted their resistance, and the Schottky contacts ideality factor and barrier height.

The figures 3.17A and B show the mapping of the ideality factor and barrier height at the Schottky contact on the wafer MAX7. The distribution of the ideality factor is uniform on the whole wafer, however it appears that it is sensitive to the JBS geometry. The table 3.1 shows that the honeycomb design deteriorates less the ideality factor compared to the stripped design.

Concerning the barrier height, we can see that it is not uniform on the whole wafer and it is slightly higher on the right side. This variation might come from a non-uniformity of the fabrication process. Further investigations are necessary to determine the exact reason.

The figure 3.18 shows the mapping of the extracted specific resistance of the diodes. First, we can note that the devices' resistance is higher at the center of the wafer and

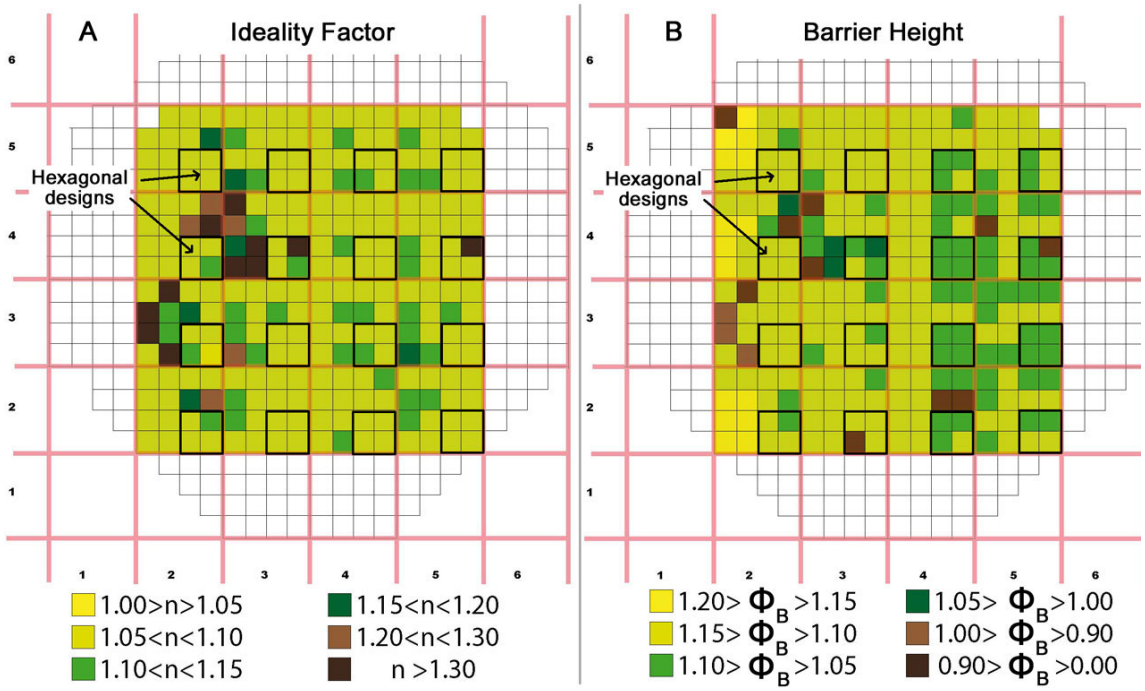

FIGURE 3.17 – mapping of the ideality factor (A) and barrier height of the Schottky contacts on MAX7, the areas containing the JBS diodes with a honeycomb (Hexagonal) designs are surrounded by a black square

	Hexagonal (80)	Stripped (144)	Schottky (15)
$1.00 < n < 1.10$	66 (82%)	68 (48%)	13 (87%)
$1.10 < n < 1.15$	9 (2%)	54 (38%)	1 (7%)
$1.15 < n < 1.20$	0	5 (3%)	0

TABLE 3.1 – Statistical evaluation of the impact of JBS geometry on the ideality factor of MAX7 diodes

decreases progressively toward the edges of the wafer. Since we are dealing with a very thick epilayer and taking into account the current state of the art of SiC CVD growth, it is difficult to obtain, at this stage, a good uniformity of the doping and thickness parameters on the whole wafer area. In our case, it is clear that the center of the wafer is thicker or has a lower doping concentration.

As the drift layer resistivity is dominant on the overall diode resistivity and it is linearly proportional to its thickness, one can estimate the difference of thickness/doping parameters to be around 20% on the overall fabricated diodes.

Concerning the different diodes designs, if we compare the designs to the standard design with p-wells $3\mu m$ large (L_P) and distanced by $4\mu m$ (L_S) as shown in table 3.2, the JBS diodes with the honeycomb design and a large p-well ($L_P = 4\mu$m) are less resistive than those with standard design (stripped p-well). Moreover the new design

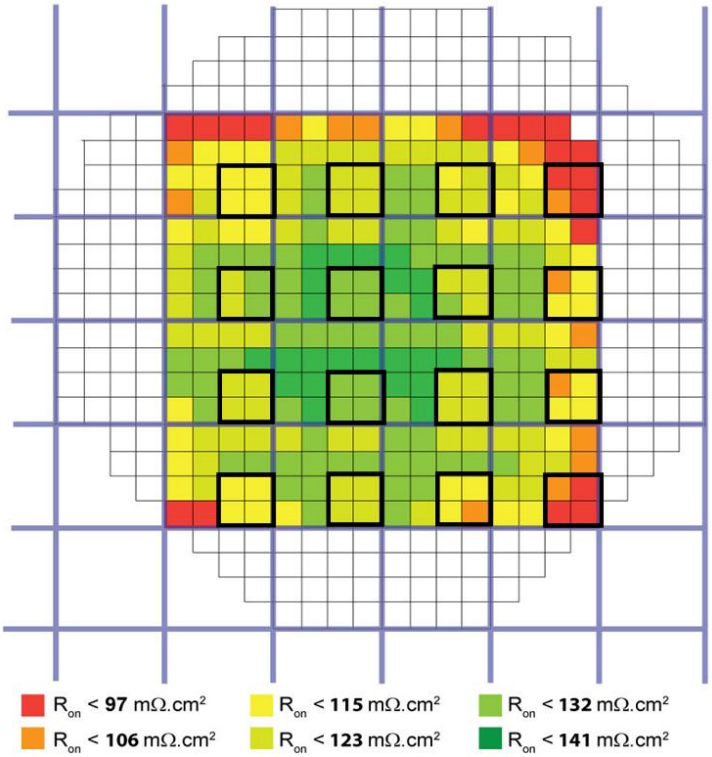

FIGURE 3.18 – mapping of the ρ_{sp} on MAX7, the areas containing the JBS diodes with a honeycomb design are surrounded by a black square

ρ_{sp}	< 123	< 132	< 141
P3/S4 Stripped	00%	21%	79%
P4/S4 Hexagonal	50%	50%	0%
P4/S6 Hexagonal	50%	50%	0%

TABLE 3.2 – Statistical evaluation of the impact of JBS geometry on the resistance of the diodes on MAX7

with $L_S = 4\mu$m and $L_P = 3\mu$m is less resistive than the standard design with $L_S = 8\mu$m and $L_P = 3\mu$m.

The hexagonal design, not used in existing JBS from litterature, seems to be the more efficient in terms of forward behaviour for these high voltage range diodes.

After a mapping of the reverse leakage current at 500V of the diodes on MAX7, we identified the diodes presenting ideal reverse leakage current up to 500V. Then, we measured under probe, in a bath of Galden, the maximum blocking capability of several of these samples.

The reverse I-V characteristic of these devices is presented in figure 3.16B. The best devices were able to handle more than 9kV, and the majority could stand more than 8kV. All the diodes experienced a destructive breakdown at the last biasing point of the curves drawn in figure 3.16B. Due to the epitaxial layer thickness/doping variation, the

best diodes in term of blocking capability were located in the center of the wafer.

Surprisingly, the Schottky diodes' (D15) reverse current is similar to some of the JBS diodes. However, we can observe that we have a strong dispersion in the reverse leakage current between the JBS diodes. Then, we cannot conclude on the screening effect of the JBS p-well and on the impact of the inter-cell distance (L_S). A Schottky diode (X3Y3 D15), located at the center of the wafer, was also able to reach a breakdown voltage superior to 9kV (shown on figure 3.16B).

Diodes of the same size on 6kV wafers presented previously did not shown destructive breakdown at leakage current as low as 100μm, moreover we observed that numerous diodes broke at the field stopper's corner in the JTE. The failure mechanism observed on the JBS and Schottky diodes seems to indicate that their termination is not optimally designed or implemented. Since this mask set layout was designed for 6.5 kV diodes, some design parameters are not optimal for 10kV diodes.

Another possibility could be that the Galden isolation is not sufficient to prevent from premature breakdown above the termination. However, it would not explain the relatively high levels of leakage current exhibited by some of the JBS.

The position of the breakdown indicates that a field crowdind is created at the field stopper's corners because it is too sharp, this problem can be solved by increasing its curvature. However, this also shows that a field crowding is already building up at the FS-JTE junction at 8kV, diodes with such epitaxial layer are theoretically capable of sustaining more than 10kV, so the JTE implantation dose can be increased to reduce the fied crowding created at the FS-JTE junction.

3.4 Influence of temperature on JBS and Schottky diodes

3.4.1 Unipolar conduction stability of 1.2kV diodes at different temperatures

The SiC devices are most appreciated for their high temperature operation capabilities. However, a higher working (or junction) temperature will reduce the electron mobility and thus increase the drift layer resistivity. The drift layer accounts for the majority of the Schottky diodes resistivity, so the Shottky diodes' resistance increases naturally with the temperature. In JBS diodes, the temperature has similar effect in unipolar mode but more subtil mechanism triggers its bipolar conduction.

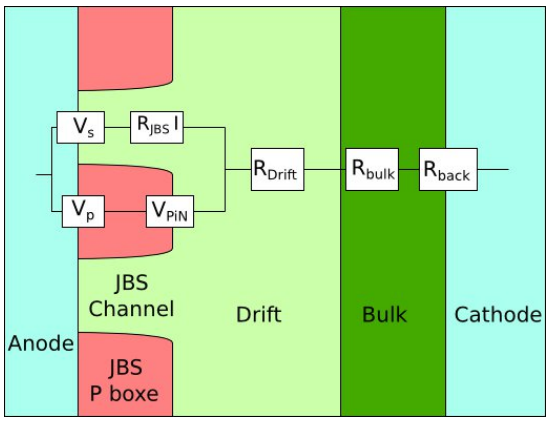

FIGURE 3.19 – Equivalent resistances in the JBS diode

As the Schottky contacts to the n-type channels between the p-wells create a short-circuit to the drift layer, it is harder to overcome the built-in potential at the PN junctions than for pure PN diodes. So the bipolar conduction triggers once the voltage drop through the n-channels is equivalent to the buit-in potential of the PN junctions. The figure 3.19 shows the schematic view of the different voltage drops and equivalent resistances in the JBS diode, with V_{P} being the voltage needed to apply on the contact to access the JBS p boxes, V_{PiN} the built-in potential at the PN junctions, V_{S} the voltage drop at the Schottky contact, R_{JBS} the JBS channel resistance, R_{bulk} is the bulk resistance and R_{back} the resistance induced by the cathode contact to the bulk.

Then, in order to trigger the bipolar conduction, we must comply with the following condition : $V_{\mathrm{S}} + R_{\mathrm{JBS}}I > V_{\mathrm{P}} + V_{\mathrm{PiN}}$. At higher temperature R_{JBS} increases, and V_{P} and V_{PiN} decrease, so the bipolar injection starts at a lower Schottky current density. Between 25°C and 300°C, the carrier mobility value is divided by 5, so the resistivity is at least multiplied by 5 and consequently the current density needed to activate the bipolar injection is divided by 5.

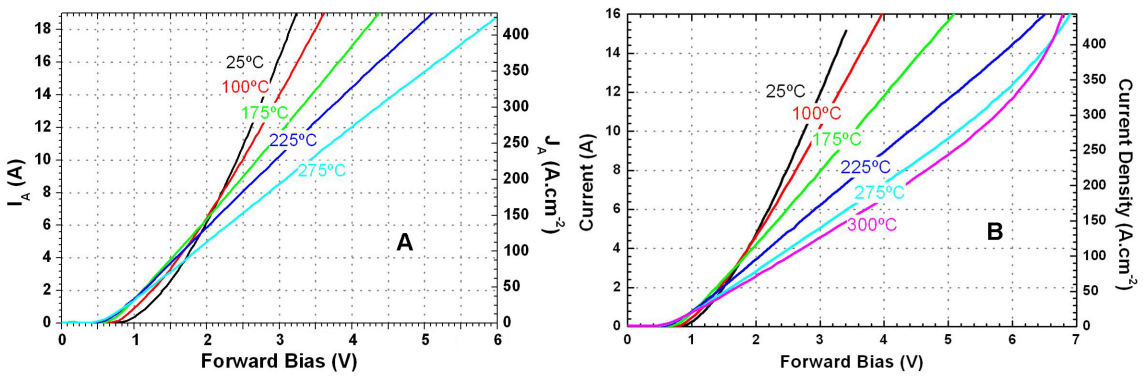

FIGURE 3.20 – Forward bias characteristics of Schottky diode (a) and JBS diode (b) at different temperatures

Using a tektronix inducing current pulses, which reduces self heating during measurement, we could characterized the static forward characteristics of our 1.2kV Schottky and JBS, presented in the part 3.3.1, up to 20A at different temperatures up to 300°C. The results are shown in figure 3.20 with the I-V characteristics of a JBS (JBS1, $L_N = 4/L_P = 3$) and a Schottky diode at different temperatures from 25°C to 300°C.

Eventhough the field stopper of the Schottky diode is contacted by the anode metallization, it does not show bipolar conduction at high current and temperature. Concerning the JBS diode, at room temperature, we did not see bipolar current up to 500A.cm^2 and could not go higher lest damaging the device. At 300°C, we can see the bipolar conduction at a current density of 250A.cm^2.

Previous JBS diodes fabricated with nickel as Schottky metal showed bipolar conduction at lower current density and temperature [41]. Using tungsten as a Schottky metal gives the diodes a better stability at high temperatures and a lower leakage current when reverse biased at any temperature compared to diodes with Ni or Ti as Schottky metal. A disadvantage of tungsten is that, lest a high temperature annealing (> 1000°C) is performed, it forms a bad ohmic contact on p or n-type SiC. However, this property can be used to retard the bipolar conduction of the JBS diodes.

Two transmission line measurement (TLM) structures, one for the p-well and one for the JTE, are present on the layout CNM_SIC026 next to D01 (see figure 1a of the annexe A). So we measured the I-V characteristics between two tungsten contacts on the implanted p$^+$ areas.

The figure 3.21 shows I-V characteristics measured between contacts on TLM at different positions on the wafer ; all the TLMs show that the tungsten on p-type SiC creates a rectifying contact when not annealed at high temperature, as in our process. Thus, the potential difference between the PiN junction and the contact for bipolar injection activation must be even higher than the 2.3V of a standard bipolar diode with

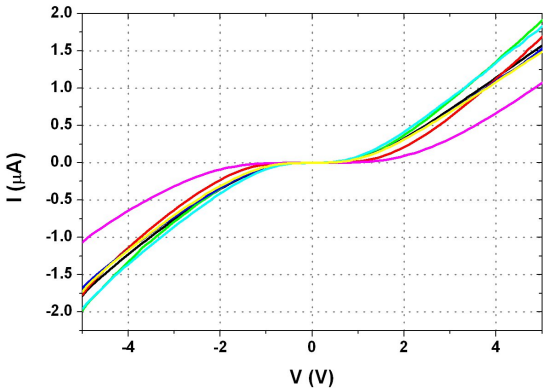

FIGURE 3.21 – TLM characteristics of W contacts on implanted p^+ at different positions of wafer ALS11

a low resistivity ohmic contact on the anode.

So the current density needed to trigger the bipolar conduction in W-JBS is even higher than classical JBS diode with Ni Schottky barrier. It allows using smaller spaces between the p boxes, keeping the unipolar conduction at nominal current and shielding more efficiently the Schottky contact when reverse biased.

3.4.2 Temperature dependance of JBS diode with a low doped drift layer (6kV diodes)

We measured the forward I-V characteristics at differerent temperatures of JBS fabricated on the same wafer as the 6kV Schottky diodes presented in part 3.3.3. The measurement was perform as in previous part up to 10A. The figure 3.22 shows the I-V

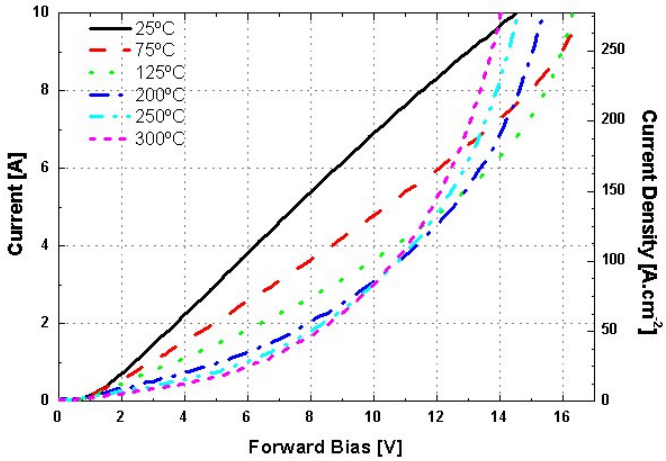

FIGURE 3.22 – Forward Bias JBS characteristics at different temperatures

curves up to 10A from room temperature up to 300°C for a JBS diode with the highest proportion of bipolar contacts ($L_S = 4\mu$m, $L_P = 3\mu$m). We can see that the diode does not exhibit bipolar conduction at room temperature and forward current up to 10A ($J_{DS} = 277$A.cm^{-2}). At 75°C the diode shows bipolar conduction at 8A. For temperatures higher than 125°C the bipolar conduction triggers for current under 4A.

In the 6kV diodes, the lower doping concentration of the drift layer induces a lower conductivity throughout all the diode compared to the 1.2kV diodes (10 times higher). This induces a higher resistance between the p-boxes, so the bipolar conduction begins at a current density ten times inferior.

3.4.3 Temperature effect on leakage current of unipolar devices

3.4.3.1 1.2kV JBS diodes

The majority of the leakage current through the Schottky barrier comes from thermionic field emission. As the thermionic field emission increases exponentiolly with the temperature, the leakage current of devices using Schottky barrier also increases exponentially with the temperature.

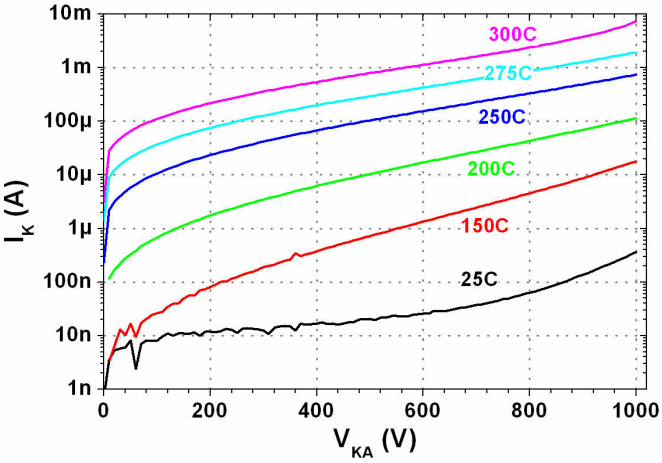

FIGURE 3.23 – Static reverse bias characteristics JBS1 diode from ALS11 at different temperatures

The packaging and the heater used to characterize the diodes in temperature allows a maximum bias of 1kV. So we measured the reverse leakage current up to 1kV at different temperatures on 1.2kV diodes presented in part 3.3.1.

The figure 3.23 shows the reverse leakage current in a JBS1 diode up to 300°C. The JBS being composed of PiN junctions and Schottky contacts, the major leakage current source is the Schottky contact. At room temperature, the reduction of the surface electric field, via the p-boxes of the JBS1, has permitted to reduce the leakage current by a factor of 10 compared to the Schottky diode. This gain remains valid up to 300°C, but is not sufficient to counter the temperature effect on the leakage current increase.

Consequently, to design SiC diodes working at high temperature, one must over-size the area and breakdown voltage of the Schottky or JBS diode compared to its room temperature characteristics to anticipate the higher resistance and leakage current at high temperature.

3.4.3.2 9kV JBS diodes

The exceptional potential of the SiC to work at high temperature (300°C) and very high voltage simultaneously is difficult to test ; no standard packaging is capable of it and Galden oil, used to reverse bias on-wafer at room temperature, would evaporate. As the principal limitation comes from the top isolation of the chip, a common solution is the measurement in vacuum.

A unique apparatus, situated at the German-French Institute of Saint Louis (ISL), allows to characterize devices on-wafer at reverse bias up to 15kV, at a controled temperature up to 500°K, and all this in a vacuum chamber. So this setup permits to characterize the chip when reverse biased at high voltage and temperature without need for Galden or other dielectric protection. Moreover, under vacuum, the metallization will not oxidize at high temperature.

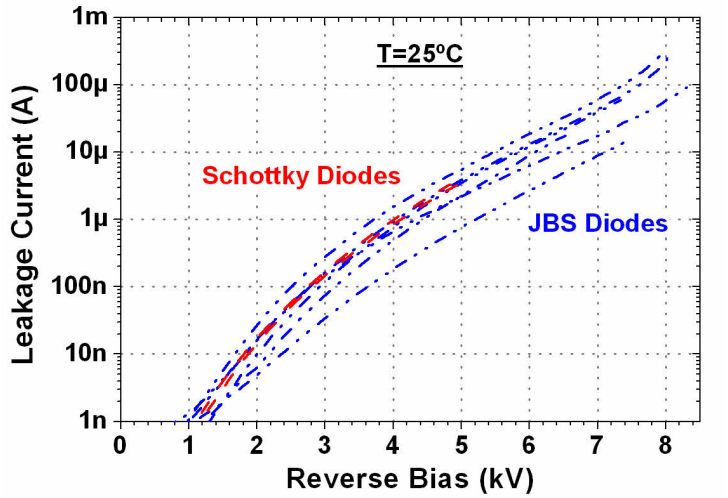

FIGURE 3.24 – Reverse characteristics of the diodes on MAX7 at room temperature under vacuum

As the devices were previously characterized in a Galden bath (see part 3.3.4), after cleaning, we first measured them at room temperature in vacuum to see if any leakage current could have come from the Galden.

Figure 3.24 show several diodes reverse characteristics measured on-wafer at room temperature under vacuum. The set-up is limited to a maximum reverse current of 300 μA. Most of the measured diodes showed a breakdown voltage of 8kV or below. Unfortunately the area where the best diodes were located was previously damaged by metal projection and overheating during the failure of one of the diode.

The leakage currents measured with this tool are not different from the ones measured at CNM in Galden. Then, it confirms that the diodes voltage capability is limited by some of the design parameters.

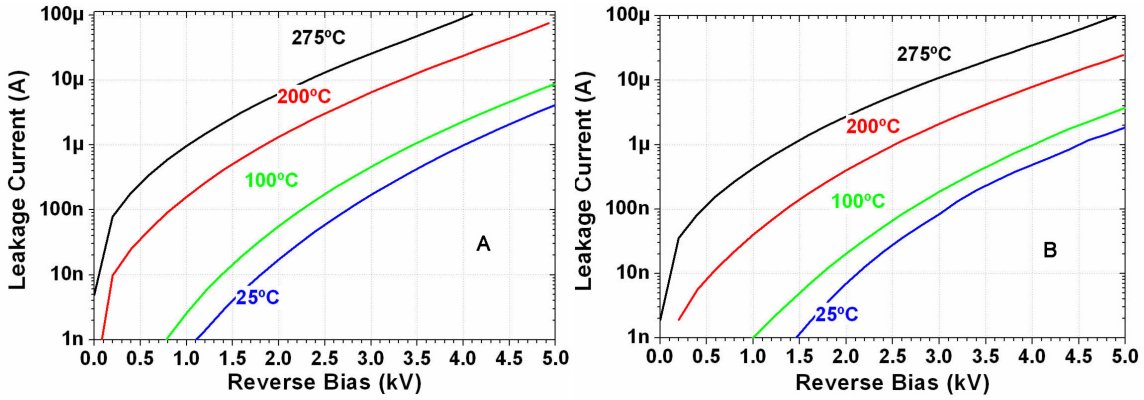

FIGURE 3.25 – Typical reverse characteristics of Schottky and JBS (Stripped 3P/4N) diodes on MAX7 at different temperatures

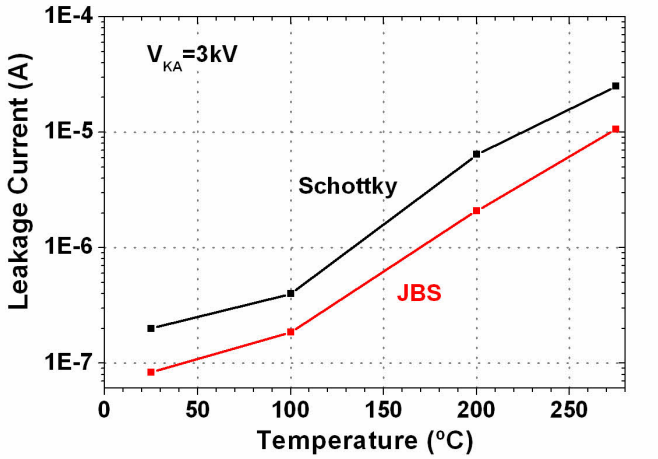

FIGURE 3.26 – Extracted leakage current dependence with temperature at 3kV

The reverse bias characteristics up to 5kV at temperatures up to 275°C have been also captured for 6 JBS and 4 Schottky diodes. Typical evolution of the reverse characteristics of the diodes are shown in the figure 3.25 and we then extracted the leakage current of the Schottky and JBS diodes at 3kV as a function of the temperature and plotted it in the figure 3.26.

The global behaviour remains the same as the one seen on the 1.2kV diodes and confirms the stable behaviour of the tungsten Schottky barrier with temperature, even for very high voltage diodes. The leakage current of the two types of diodes exhibits similar temperature dependence when reverse biased at high voltage. The leakage current increases exponentially with the temperature because the leakage current is dominated by the thermionic field emission at the Schottky interface of both Schottky and JBS diodes.

As the JBS diode protects its Schottky contact from elevated electric field, the leakage current through the Schottky contact should be much lower than the pure Schottky diode's. However, the JBS diode shows a leakage current only 3 times inferior to the

Schottky diode. It is worth noting that the diodes measured here come from different positions on the wafer, the resistance mapping shows that the drift layer thickness varies a lot on the wafer. So this can explain the low difference of leakage current between the JBS and Schottky diodes, the drift layer of the JBS diode being thinner than the Schottky diode.

As some parts failed during the measurement, functional specimen blocking up to 5kV at 275°C and situated in the same area could not be characterized. The reverse leakage measurement at different temperatures permits to study the thermionic field emission through the Schottky contacts of SBD and JBS diodes. We will need more devices with similar drift layer, fabricated on more uniform wafer to assess the gains in terms of leakage current reduction brought by the tungsten JBS diodes at high temperature. Furthermore, the study of the thermionic emission current would allow building a temperature dependant analytical model of the reverse characteristics of the Schottky contact.

3.5 Switching behavior of unipolar rectifiers at high temperature

3.5.1 1.2kV diodes

Schottky and JBS diodes from ALS11 (see part 3.3.1) were packaged in TO220 packed, the anode connected with wirebonding and isolated with silicon.

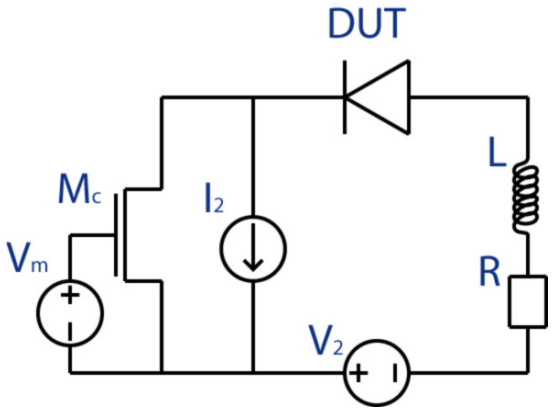

FIGURE 3.27 – Electrical schematic of the setup used to characterize the switching behaviour of the diodes

The switching waveform and more particularly the turn-off waveform of the devices was captured at different temperatures. The switching was performed at 600V, with an inductive load and coupled with a 1.5kV-5A Si-IGBT (see fig. 3.27). The diodes turned-off from a current up to 10A, giving rise to a $Di/Dt = 200\text{A}/\mu\text{s}$ during the turn-off.

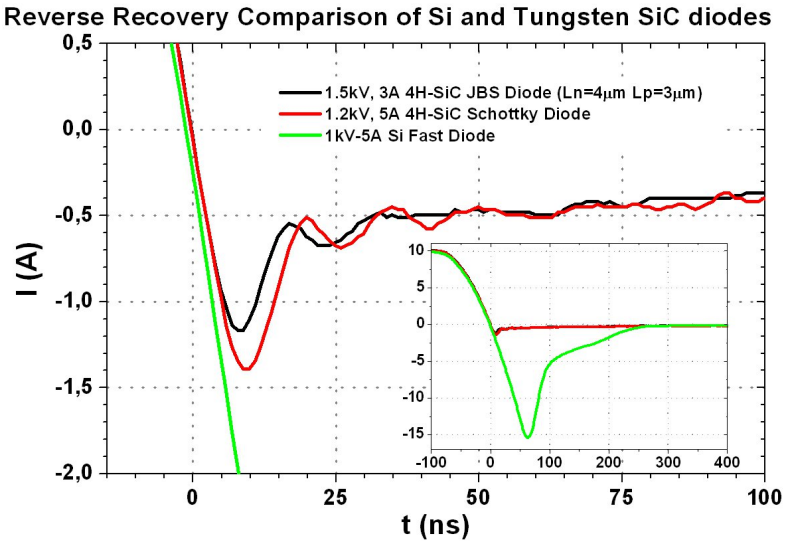

FIGURE 3.28 – Comparison of JBS1 and Schottky diodes from ALS11 with a 1kV fast recovery Si Diode

The figure 3.28 shows the reverse recovery waveform during turn-off of SiC diodes and a 1kV-5A Fast Silicon diode commercialized by ST-Microelectronics. Both SiC diodes show a negligible reverse recovery charge and a much shorter recovery time compared to the silicon diode. The ripples come from the coupling of the diode's capacitance with the circuit parasitic inductance.

In bipolar devices, like the Si diode shown here, the recombination of minority carriers during the depletion induces switching losses. The conduction in Schottky diodes being unipolar, minority carriers are not injected in the drift layer and a great part of the switching losses during turn-off are suppressed. All the free carriers are evacuated toward the cathode and the majority of the switching charge is capacitive. Only at high Di/Dt, capacitive diffusion current can generate a small recovery current during the turn-off of the Schottky diode.

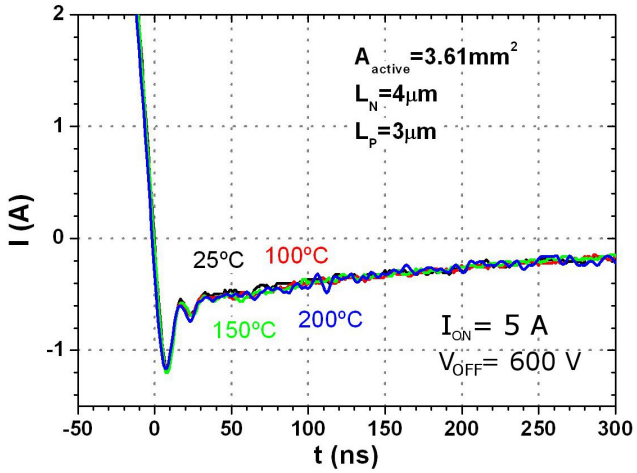

FIGURE 3.29 – Reverse Recovery Current of a 4H-SiC JBS Diode from ALS11 at different temperatures

The reverse recovery charge of unipolar rectifiers being independent from the carrier lifetime and recombination, it is independent from temperature and the apparent reverse recovery charge remains constant with temperature.

The figure 3.29 illustrates this temperature independent phenomenon. A SiC JBS diode is switched off from 5A at 3 temperatures from 25 °C to 200 °C. We can see that the recovery current is similar for all 3 operating temperatures.

Compared to the Schottky diodes, standard Ti or Ni JBS diodes have the advantage of higher blocking voltage and surge current capability, however their bipolar component induces an increase in the recovery charge with the temperature, resulting in a slower turn-off process and higher switching losses.

Our previous static measurement showed that the W-JBS diodes exhibited bipolar conduction only at elevated current density even at 200°C (see part 3.4.1). An interesting

result shown by the figure 3.29 is that in our diodes the turn-off recovery charge at nominal current switching does not increase up to 200°C, which proves that no bipolar conduction is activated at 10A up to 200 °C. Thus, the W-JBS diode offers the Schottky advantages of a very fast switching at the same time as an increased breakdown voltage capability thanks to lower leakage currents and higher surge current capability, with minimal cost on the forward voltage drop.

3.5.2 6kV diodes

The static measurements presented in part 3.4.2 have shown that lowering the drift layer doping concentration lowers the current necessary to trigger the bipolar conduction, however it does not give a precise evaluation of it. The reverse recovery waveform is very sensitive to the bipolar conduction and will permit us to precisely determine the conduction mode in the devices at different temperatures.

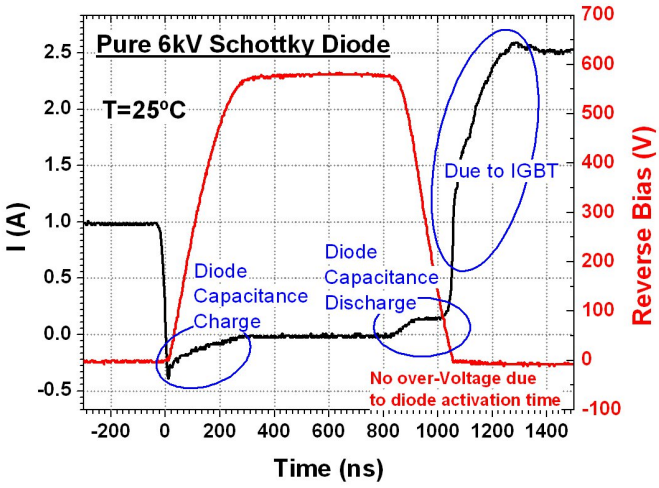

FIGURE 3.30 – full switching waveform of a 6 kV pure Schottky diode

Figure 3.30 shows the full switching waveform of a 6kV tungsten Schottky diode implemented in a DC-DC converter with a 1.5kV IGBT (see fig. 3.27). We can see that the charges stored during the turn-on of the IGBT are returned during the turn-off. Moreover, the over-voltage peak, present during turn-off of the IGBT, which is due to the typically used Silicon PiN free wheel diode, does not occur with the SiC Schottky diodes.

However, when the parasitic inductances of the circuit are too high and coupled with the SiC diode's capacitances, the input capacitance having fast charging and discharging speed is responsible for oscillations at the end of the switching process and can be problematic, especially at high voltages. If the switching is too fast (high DI/Dt), all the capacitive charges are extracted in the first 20ns of the turn-off, while the IGBT turn-on

is still not fully completed, this charge is generating a high current peak and may destroy the IGBT channel. This issue can be solved by slowing down the turn-on waveform of the IGBT and minimizing the parasitic inductances.

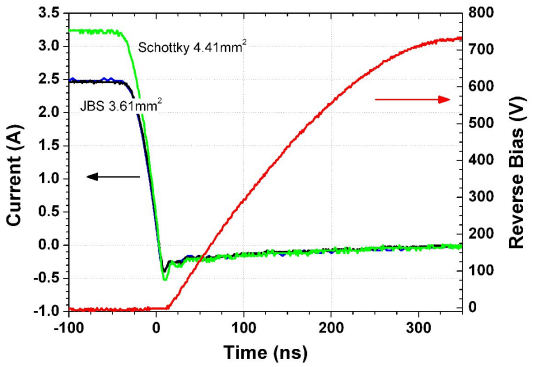

FIGURE 3.31 – reverse recovery waveforms of 6kV SiC diodes

The figure 3.31 shows the comparison of the reverse recovery curve for 6kV JBS and Schottky diodes from ALS10 for a reverse bias polarization of 750V and an equivalent current density at room temperature. We can see that both types of diode exhibit the same reverse recovery charge and turn-off time under nominal current switching.

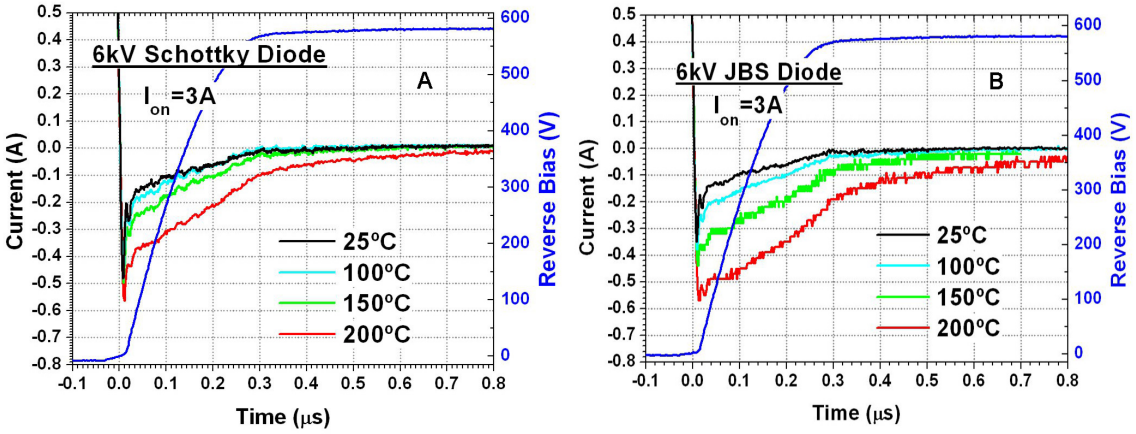

FIGURE 3.32 – Reverse recovery of the Schottky (A) and JBS (B) diodes at different temperatures

Thanks to its unipolar conduction character, the Schottky diode reverse recovery charge does not vary with the junction temperature. However, in our designs, the Schottky diodes have a p^+-type ring on the periphery, in order to act as field stopper and add a better surge current capability to the diode. This ring was not electrically activated (bipolar injection) on the 1.2kV diode for the nominal current at 200°C. We will verify that it is still the case in the 6kV range diodes. If activated, the reverse recovery charge due to bipolar recombination will increase with the temperature. The figure 3.32 shows

the reverse recovery of 6kV Schottky and JBS diodes at different temperatures up to 200°C for nominal current of 3A.

One can see through the reverse recovery peak current and time variation that the bipolar conduction mode in the P ring of the Schottky diode is activated at 3A between 150°C and 200°C. Its influence can be considered as minimal on the total reverse recovery charge. Compared to the Schottky diode, the JBS diodes bipolar conduction component is activated earlier (between 100°C and 150°C) and shows more influence on the recovery charge.

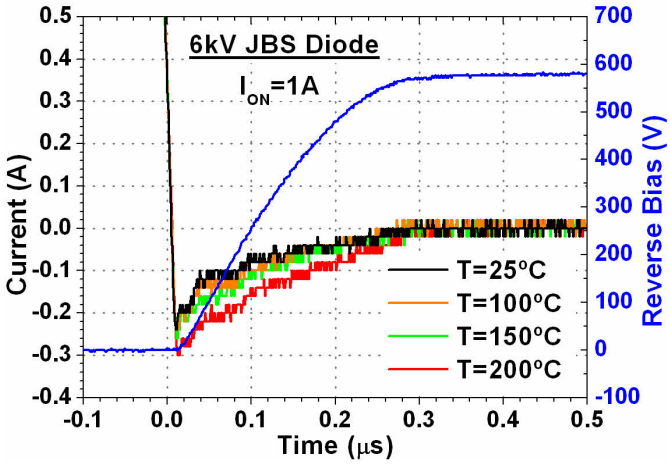

FIGURE 3.33 – Reverse recovery of the JBS diode at 1A and different temperatures

When the bipolar conduction is activated, we can distinguish two slopes in the reverse recovery discharge waveform. The first one corresponds to the capacitive discharge and the second one to the extraction of the stored charges in the drift region, which depends on the minority carrier's lifetime. At 200°C, this charge, inherent to the bipolar conduction, is visible on both diode types when switching a forward current of 3A.

The bipolar conduction of the JBS diodes triggers at different current density depending on the temperature. To observe the reverse recovery charge induced at lower current, we measured it (see figure 3.33) at a nominal current of 1A and temperatures up to 200°C. We can see that the reverse recovery charge increases only slightly between 150 and 200°C and the second slope is not visible. At this current rate, the losses due to switchings would increase by 20% with the temperature.

The unipolar rectifiers are interesting for their very fast recovery, however we cannot reach such limit with the Si-IGBT used in this setup. The fast capability of the W-JBS diode at high temperature must be confirmed with a faster switching waveform. To do so we will need to replace the IGBT by a faster switch as a SiC-MOS. It would permit to better distinguish the two slopes during the turn-off.

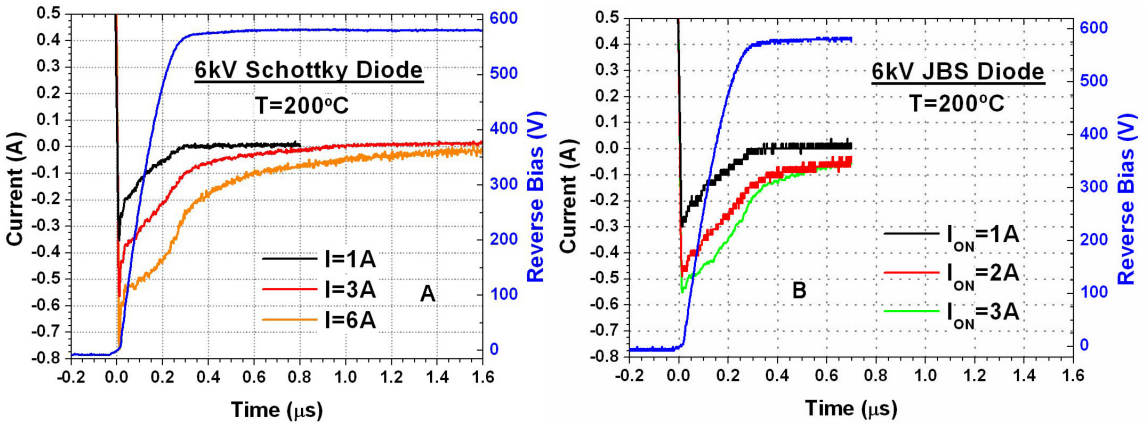

FIGURE 3.34 – Turn-off waveforms of the Schottky and JBS diodes at 200°C for different switched currents

The figure 3.34 shows the turn-off waveform for both the JBS and Schottky diodes at 200°C for different switched current values. One can see that the P ring of the Schottky diode is not activated at 200°C-1A. But we can see that it is activated at 3A and it is even more pronounced at 6A.

We see that the reverse recovery charge of the JBS increases with the current density but it is still far below the one obtained with the Si counterpart.

3.6 Surge current capability of unipolar rectifiers

3.6.1 1.2kV diodes

The surge current capability is one of the main weaknesses of the pure Schottky diode. When submitted to a high peak current, due to the positive temperature coefficient linked with the unipolar nature of the conduction, the diode will strongly heat-up. SiC semiconductor being very resistant to high temperatures, the metallization and bonding will be the first victims of this overheating.

Our 1.2kV Schottky and JBS diodes (see part 3.3.1) were packaged and their surge current capability tested with an home-made generator, which produces half sinusoidale current pulses of 10ms.

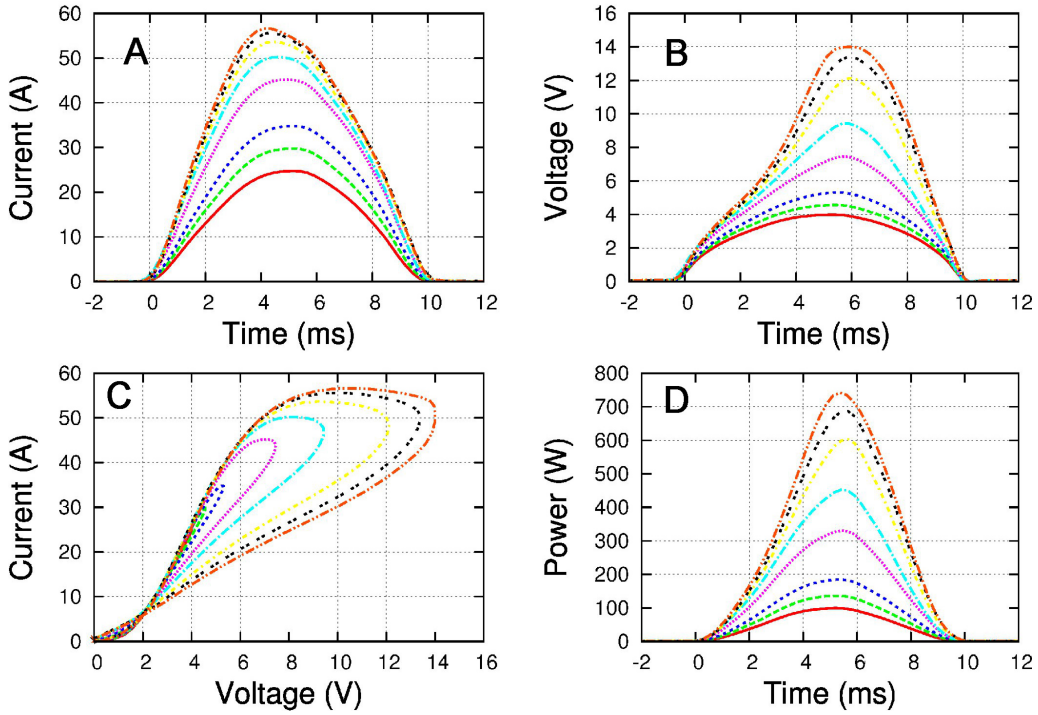

FIGURE 3.35 – 10ms Surge current tests at room temperature on a packaged Schottky diode from ALS11 wafer

Each diode was subjected to pulses with increasing intensity at room temperature, with verification of the diode blocking capability up to 1kV between each pulse. We consider the device broken when it looses its blocking capability. The Schottky diodes with tungsten as Schottky metal stood up to 60A pulses, corresponding to a pulse power up to 700W. The waveforms obtained at the different pulse power are shown in figure 3.35.

On the pure Schottky diodes, the temperature coefficient is positive, so its resistivity increases with the temperature. Consequently the I-V curve (see figure 3.35C) describes

a loop going up left and then the diode warms up with the dissipated energy and the voltage drop increases, as well as the forward voltage.

The Schottky diodes have a p-type ring connected to the anode contact but no bipolar conduction was present until the maximum surge current at room temperature ; the design should be revised to integrate more rings inside the periphery of the contact in order to create a JBS structure and enable the bipolar conduction earlier and around the active area.

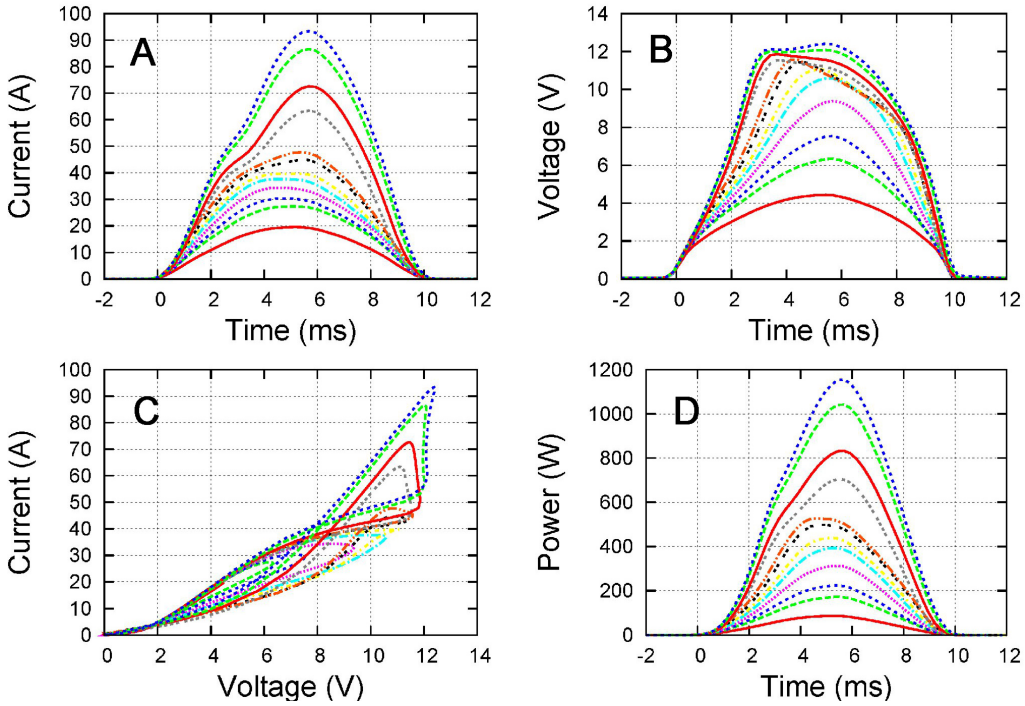

FIGURE 3.36 – Surge current tests on a JBS1 Diode from ALS11

Regarding JBS, we tested a JBS1 ($L_P = 3\mu m$ and $L_N = 4\mu m$) diode, which has the strongest bipolar component. The figure 3.36 shows its surge current capability with similar pulses. The bipolar conduction being enhanced by temperature (negative temperature coefficient), the waveform of the I-t and I-V curve (see figure 3.36A and C) is different compared to the Schottky diodes (see figure 3.35A and C).

During the pulse, the conduction regime changes from unipolar to bipolar, and finally returns to unipolar. At high current, the I(t) surge curves, shown in figure 3.36A, have two peaks ; the first peak corresponds to the saturation of the Schottky current and the second corresponds to the additional bipolar current. It is more obvious in the I-V curve shown in figure 3.36C, where we can see that the bipolar conduction starts at higher current density when the current peak increases.

This comes from a thermal effect ; as the electrons' mobility decreases with the temperature, the device's resistance increases when operating in unipolar mode at higher

temperature. With higher surge current peaks, a given bias is reached faster, so the device heats up during less time. Then, for higher surge current peak at a given bias voltage, the device's temperature is inferior which increases the bipolar threshold voltage and reduces the unipolar resistance of the diode.

Thanks to the activation of its bipolar conduction, the diode could withstand current pulses up to 90A, corresponding to a power of 1100W. The diode first conducts through the Schottky contacts with only majority carriers up to 11.5V and then through the p-wells in bipolar mode.

A remarkable phenomenon was experienced ; the characterized Schottky and JBS diodes always failed the same way. The figure 3.23 shows pictures of the aluminum top metallization of a Schottky diode submitted to a progressive increase in the current peak.

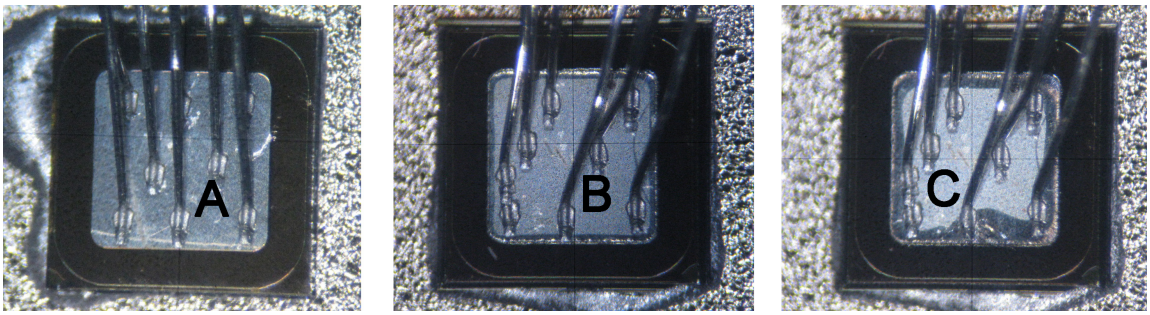

FIGURE 3.37 – Pictures of the Schottky diodes (a) before and (b,c) after failure during surge current tests

The top metal aspect starts to change on the periphery of the anode metallization and the degradation progressively extends to the centre of the diode. As we can infer, the aluminium metallization melts, destroying first the field plate on the contact periphery, and then the Schottky contact area.

This phenomenon has been also experienced by INFINEON [89] on their last generation of Schottky diodes, which anode are made of aluminum over titanium. The proposed solution to increase the surge current capability is then to use metals with a higher melting point like copper. However, copper reacts with titanium when temperature increases and other solution such as a combination of copper-molybdenum must be envisaged.

3.6.2 6kV diodes

The 6kV Schottky diodes (see part 3.3.3) were also tested under surge current pulses of 10ms until the destruction of their reverse blocking capability.

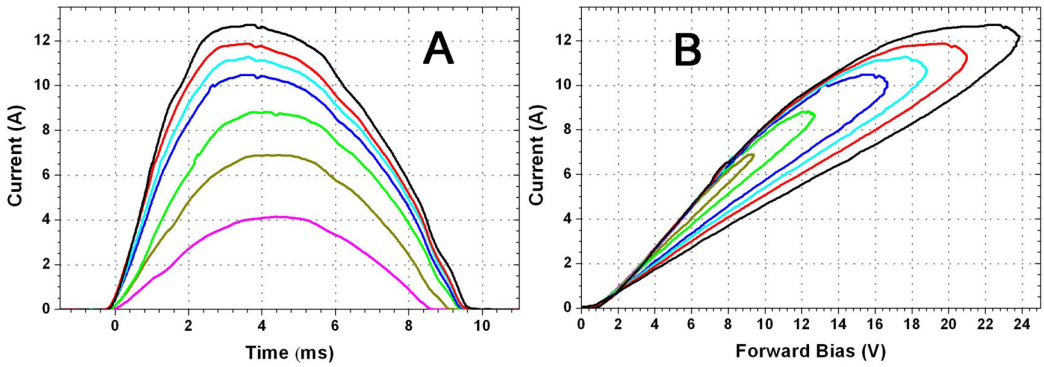

FIGURE 3.38 – Surge Current Waveforms on 6kV Schottky diodes

The figure 3.38 shows the surge current waveform of a 6kV Schottky diode from wafer ALS10 as a function of time (A) and the I-V characteristics of the diode during the pulses (B). The Schottky diodes sustained a maximum current surge of 13A under a forward bias of 24V. The integration of the dissipated power over time gives a maximum total energy of 34 J.cm^{-2}. We can see in figure 3.38B that the temperature coefficient remains positive so the chip does not show bipolar conduction until its destruction.

3.7 Innovative termination for planar devices fabricated on SiC Schottky diodes

Considering the results presented in the part 3.2, we created new mask layouts implementing smaller devices with innovative designs. These masks were employed to fabricate the diodes presented in part 3.3. Typically, a Schottky diode design includes the selection of the size and shape of the active area (Schottky contact), and the termination design. While the former essentially depends on the current capability required, the latter is quite complex since we must take into account the fabrication process and epitaxial layer's properties.

3.7.1 design

High voltage devices fabricated on SiC are majoritarily protected by a JTE termination as presented in part 2.2.1. The drift layer thickness increases with the reverse capability of the device. However the implantation depth cannot be scaled proportionaly and the field crowding effect seen at the end of the JTE increases, as explained in the part 2.2.1. In the part 2.1.5, we presented the possibility to use JTER to reduce this effect.

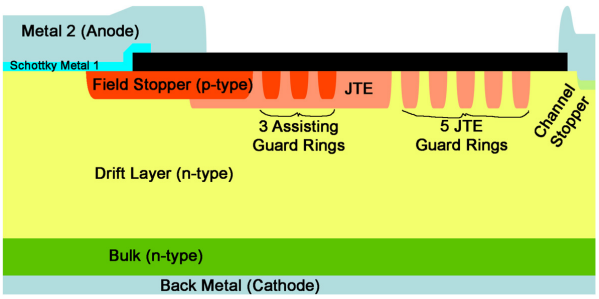

FIGURE 3.39 – Schematic view of the Schottky diodes' vertical structure and termination on CNM_SIC027

To show their efficiency, we designed a new layout composed of a mosaic of fields including 16 diodes, the basic field is shown in figure 3.40.

The basic field includes Schottky diodes terminated by different combinations between JTE, AGR and JTER (see figure 3.40 and table 3.3). The more elaborated one is composed of 3 AGR, 5 JTER and a JTE as shown in figure 3.39.

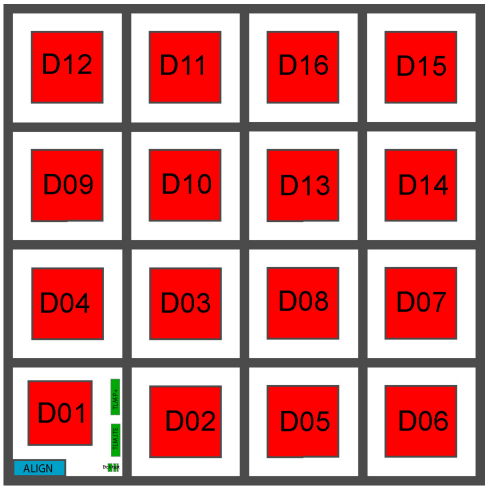

FIGURE 3.40 – Repartition of the diodes in the basic field of new layout CNM_SIC027

	L_{JTE} (μm)	Number of JTER	Number of AGR
D01	190	0	3
D02	190	5	3
D03	170	5	0
D04	170	3	0
D05-D16	190	3	3

TABLE 3.3 – Variations of termination of CNM_SIC027

3.7.2 fabrication

Two 3 inches, 8°-off wafers, named PHL2 and PHL3, with a drift layer of 45μm doped at $1.5 \cdot 10^{15}\text{cm}^{-3}$ have been processed to fabricate Schottky diodes with tungsten as Schottky barrier metal. With a theoretical electron mobility of $800\text{cm}^2/\text{V}-\text{s}$ in the drift layer, the calculated epitaxial resistance is equal to $23\text{m}\Omega.\text{cm}^2$ (without the substrate contribution, estimated to $0.4\Omega.\text{cm}^2$).

The same fabrication process as the diodes presented in part 3.3 was used. The only difference of fabrication process between the two wafers concerns the JTE implantation. An easy way to prove the efficiency of the JTER termination is to increase the JTE dose over the JTE dose threshold (see part 2.1.5) The dose of the implanted JTE was superior to the JTE dose threshold on PHL2 and inferior on PHL3.

3.7.3 results

Diodes on both wafers have shown good reverse capability up to 5.8kV and expected forward characteriscs with similar barrier height on both wafers as shown in part 3.3.2.

Diode	D01	D02	D03	D04	D05-D16
Termination	JTE - 3 AGR	JTE 5 JTER 3 AGR	JTE 5 JTER -	JTE 3 JTER -	JTE 3 JTER 3 AGR
> 4000V	12 (37%)	11 (32%)	7 (20%)	11 (30%)	119 (30%)
1000-3900V	2	1	1	1	10
100-1000V	7	15	19	8	

TABLE 3.4 – Diodes design breakdown voltage statistics on PHL3

Diode	D01	D02	D03	D04	D05-D16
Termination	JTE - 3 AGR	JTE 5 JTER 3 AGR	JTE 5 JTER -	JTE 3 JTER -	JTE 3 JTER 3 AGR
> 4000V	3 (12%)	10 (30%)	8 (25%)	4 (12.5%)	70 (18%)
1000-3900V	1	0	3	0	12
100-1000V	13	9	10	12	121

TABLE 3.5 – Diodes design breakdown voltage statistics on PHL2

We do not see a clear difference of reverse capability between the diodes having JTER and those without it on PHL2. However, the yield statistic is very different from PHL2 to PHL3 as shown in tables 3.4 and 3.5. One can see that diodes from PHL3 wafer generally show a probability of success of 30%. Only D03 diodes exhibit a lower yield (20%). D03 differs by the absence of assisting guard rings in its termination. However, D04 also has no AGR, so the different yield cannot be related to this design specificity. Then, considering the diversity of tested termination designs, and the homogeneity of the results, it seems that the failures must come from defects on the wafer or created during the fabrication process.

The statistical distribution of diodes withstanding more than 4kV on PHL2 (see table 3.5) is very different from PHL3 (see table 3.4). On PHL2, the proportion of diodes withstanding 4kV is lower than 20% for D04, D05-D16 and D01 designs. Moreover, D01 is

the smallest diode, so its probability to be affected by defects is lower. However it shows the lowest percentage of yield, while it should be the highest as in PHL3.

This difference between PHL2 and PHL3 can be explained by the JTERs in the termination ; D01 has no JTER, D03 and D02 have 5 JTER, D04-D16 have 3 JTER. So the quantity of diodes withstanding more than 4kV is proportional to the number of JTERs in the termination. Moreover, diodes with assisting guard rings (AGR) always show a better yield for a same number of JTERs.

Another important point is that PHL2 has a JTE implantation dose superior to the JTE dose threshold (see chapter 2). This experiment shows that the JTERs increase the dose tolerance as predicted by the simulations. However, simulations predicted that 3 JTERs would be sufficient while experiment show that only terminations with 5 JTER is actually effective. The lateral spreading of the implanted species on the JTE mask edge is not well known, if we underestimated it, the JTERs are larger and the space between them is smaller compared to the simulation. A smaller distance between the rings make them less efficient, however the design is made so that the distance between them increases exponentially from the inner to the outter rings, so the last rings can be effective. This explains why the termination with 5 JTERs works better than the one with 3 JTERs.

3.8 Conclusions

Schottky and JBS diodes of different voltage capabilities, terminations and active area design were fabricated successfully. We evidenced that the tungsten Schottky barrier permits to reach high temperatures and withstand high voltages up to 5kV@275°C. Moreover, it permits to produce unipolar components taking advantage of the protective effect of the JBS structures toward the Schottky contacts, reducing the leakage current. The unipolar behaviour at nominal current of the devices was evidenced both with the surge current and switching measurements on 1.5kV and 6kV diodes. Exceptional JBS and Schottky diodes with blocking voltages up to 9.2kV were created to show the maturity and the unique possibilities disclosed by Silicon Carbide technology.

An extensive work of simulation and design of the termination was performed to conceive the fully planar architecture employed in all the aforementioned devices. We could not take risks by implanting the JTE with a dose too high, however the experience with PHL2/PHL3 wafers has permitted to evidence the JTERs role predicted by the simulation.

On the other hand, we have seen that the presence of AGR inside the JTE improves the termination performances. However we could not see the impact of the number of JTERs on the maximum breakdown capability of the termination because the active area of the Schottky and JBS diodes is limiting it.

Different active area designs were included in the different tested layouts, thanks to the different variations we proved the feasibility and potential interest of hexagonal JBS design, especially regarding forward characteristics. More experiments and samples should be processed to confirm our initial observation.

On wafers ALS12/ALS15, the Schottky interface difference induces fluctuation of the electrical properties on the diodes ; the physical difference between them was inferred from the mapping of their electrical characteristics, TEM analysis is the only one to be capable to witness the difference of interface and could not be done here. Further investigation on the subject are needed to perform those analyses to confirm the diagnostic.

The switching characteristics revealed the impact of the JBS design on the reverse recovery behaviour. At high voltage, a pure Schottky switching generates oscillations. Probably a small bipolar component could soften the switching curve, the design of JBS must then take this fact into account.

We also evidenced the high temperature capability of the JBS devices. At 275°C, a reduction of the breakdown capability from 8kV to 5.5kV has to be taken into account in the selection of a diode range for operation at these temperatures.

The figure 3.41 summarizes the breakdown voltage results for the diodes described in this chapter, fitted with the theoretical surface electric field as a function of the breakdown

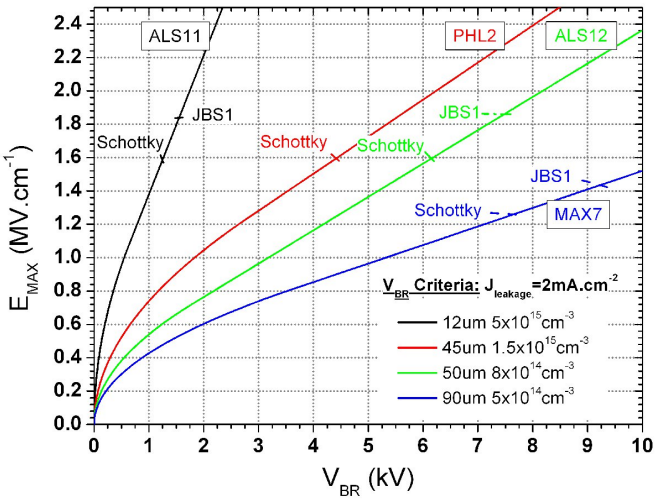

FIGURE 3.41 – Representation of E_{max} as a function of V_{BR} (lines) for the different epitaxial layer parameters employed for the diodes fabricated during this work and situation of these diodes

voltage. The values were extracted for a fixed leakage current density of 2mA.cm^{-2} for all the diodes. One can see that the critical field is situated around 1.6MV.cm^{-1}, which is near the theoretical value we used for modeling. Consequently, the curves of figure 3.1 gives good appreciation of the optimum epitaxial parameters to be selected in order to fabricate Schottky diodes for a given breakdown voltage.

Chapitre 4

4H-SiC Vertical Power MOSFET

4.1 Introduction

The silicon carbide vertical MOSFET (VMOS) is the next generation of power switches with blocking voltage between 1kV and 4kV. Compared to the current generation of Silicon IGBTs, the SiC VMOS can operate at higher frequencies and temperatures, with lower switching losses. They are capable to attain switching frequencies superior to 50kHz [45] and operate at temperatures over 300°C.

However, we are facing a major issue concerning the SiC-SiO_2 interface, the best channel mobility obtained until now are ten times inferior to the bulk mobility. Such degradation is essentially due to interface states and roughness [51]. A lot of investigation has been dedicated to the improvement of this interface's quality at CNM of Barcelona as in many of the laboratories working on elaboration of SiC chips.

The interface states are not only degrading the channel mobility, they are also a concern from a reliability point of view. High voltage MOSFETs and IGBTs can operate well with the obtained channel mobility as far as the long term reliability of the channel is guaranteed. Ultimate investigations have shown that thermal oxide grown under NO ambient was reliable in the long term [90] and two companies have started to commercialize 1.2kV SiC VMOS.

Compared to the silicon technology, the SiC VDMOS structure is similar but the fabrication process is different on many aspects. One main difference is the requirement of high temperature processing over 1500°C, as the activation of implanted impurities (and the formation of ohmic contact) require high temperature annealing. Moreover, the different doping areas are mainly produced by implantation and some of them, like the channel area, require high doping precision. As mentioned previously, the formation of the gate oxide is sensitive and is also performed at high temperature. So the combination of the different process steps must take the effect of the high temperature budget into account.

The first trial of VDMOS' fabrication at CNM made use of the boron's implantation to create the channel [91]. It was successful but the boron diffuses at temperatures around 300°C and present deeper ionization energies. As the Al impurities as a p-type dopant for SiC have the best properties, it was used to create the p-well of VDMOS fabricated during the ESCAPEE European program from 2003 to 2007.

In this work we initially studied the last VMOS samples produced in the ESCAPEE project based on a conventional technology. Then we proposed modifications in the design and the fabrication technology of the VMOS in order to improve the results of preliminary devices.

4.2 First generation of VDMOS

During the ESCAPEE European project, a first generation of high voltage SiC VDMOS were designed and implemented. The targeted breakdown was 3.5kV. This project allowed investigating extensively the implantation, annealing and oxidation processes on SiC at CNM. The VDMOS fabrication process includes more than 4 implantation steps, 2 oxide depositions, two metal depositions and one oxide growth with all the lithographic steps associated (9 levels in total). As we will see in the next parts, any error is catastrophic for the devices and each failed step will have a negative effect on the structure. Simpler structures as lateral MOS and diodes have permitted to greatly progress on the combination of the different fabrication steps ; the realization of VDMOS is the accomplishment of several years of combined efforts. As a first step of the SiC VDMOS design and process' optimization carried out in this work, we extensively characterised the last VDMOS samples of the ESCAPEE project. This characterisation study was used as an input for the novel design and technology choices done during the following steps of the investigation.

4.2.1 Design

4.2.1.1 Cell's structure

The VDMOS were fabricated with the layout developed in the project ESCAPEE and presented in the annexes. It permits to build VDMOS devices with the cell's structure shown in figure 4.1. The layout includes mono and multi-cell VDMOS of small size with different channel's (L_{CH}) and JFET's lengths (L_{JFET}).

The functional part of the devices is located at the top of the VDMOS and is composed of the source contact, the channel and the JFET regions. The channel width must be maximized in a minimum of space. So, the cell size must be minimized and its geometry has a strong influence on the channel's integration. On the other hand, the source contact resistance can become a major contribution if its area is too small.

4.2.1.2 Cell's geometry optimization

In this sense, the hexagonal design, as shown in figure 4.2A, is theoretically the best option. The source contact and p-well areas are concentric hexagons and the channel is

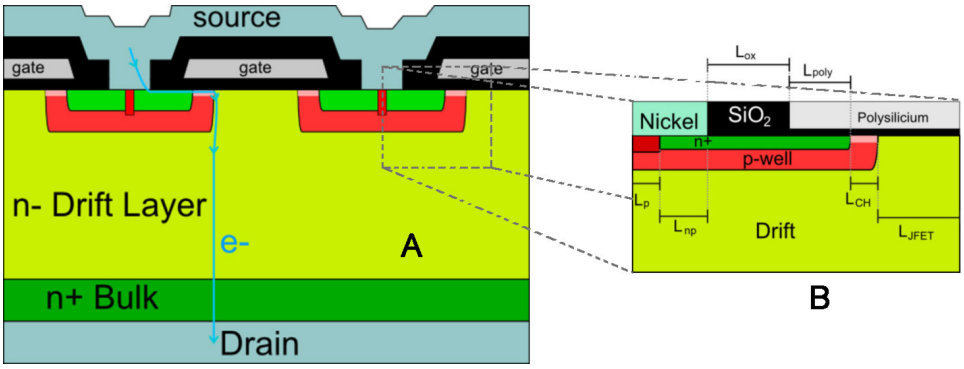

FIGURE 4.1 – Vertical cross section of a simplified VDMOS cell (A) and zoom in the channel region (B) ; the n-type areas are represented in green and the p-type ones are colored in red

located on their periphery. Hexagonal cells are repeated as tiles to multiply the channel length ; a power VDMOS can count thousands of them.

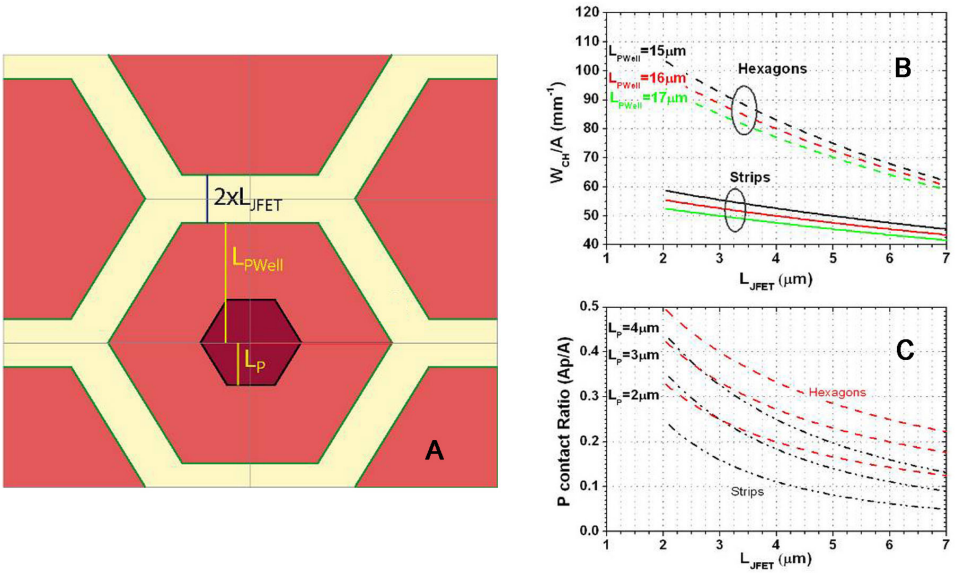

FIGURE 4.2 – Top view of an hexagonal cell (A) and comparison of the channel integration factor (B) and source contact integration factor (C) between hexagonal and stripped designs as a function of the JFET area length for different cell's design parameters

The JFET area is located between the hexagons. Figure 4.2 shows the hexagonal design of a cell with its main geometrical parameters and different integration factors for the hexagonal and stripped cells with respect to the JFET length (L_{JFET}). The ratio of channel width per active area ($W_{\mathrm{CH}}/A_{\mathrm{act}}$) is the best way to quantify the channel integration degree ; it is shown for the hexagonal and stripped geometries in figure 4.2b. As the cell's geometry changes, the contacts' geometry changes too. If the ohmic contact area's size becomes too small, its contribution to the VDMOS' resistance becomes too important.

Figure 4.2c shows the ratio of contact area per active area for stripped and hexagonal cells with different sizes of contacts. In both comparisons the Hexagonal structure is superior, providing higher contact area for higher integration of channel. This design is used on MV03 and MV07 of the ESCAPEE mask layout.

4.2.2 Fabrication Process

The basic fabrication steps of a conventional SiC VMOS are represented in figure 4.3.

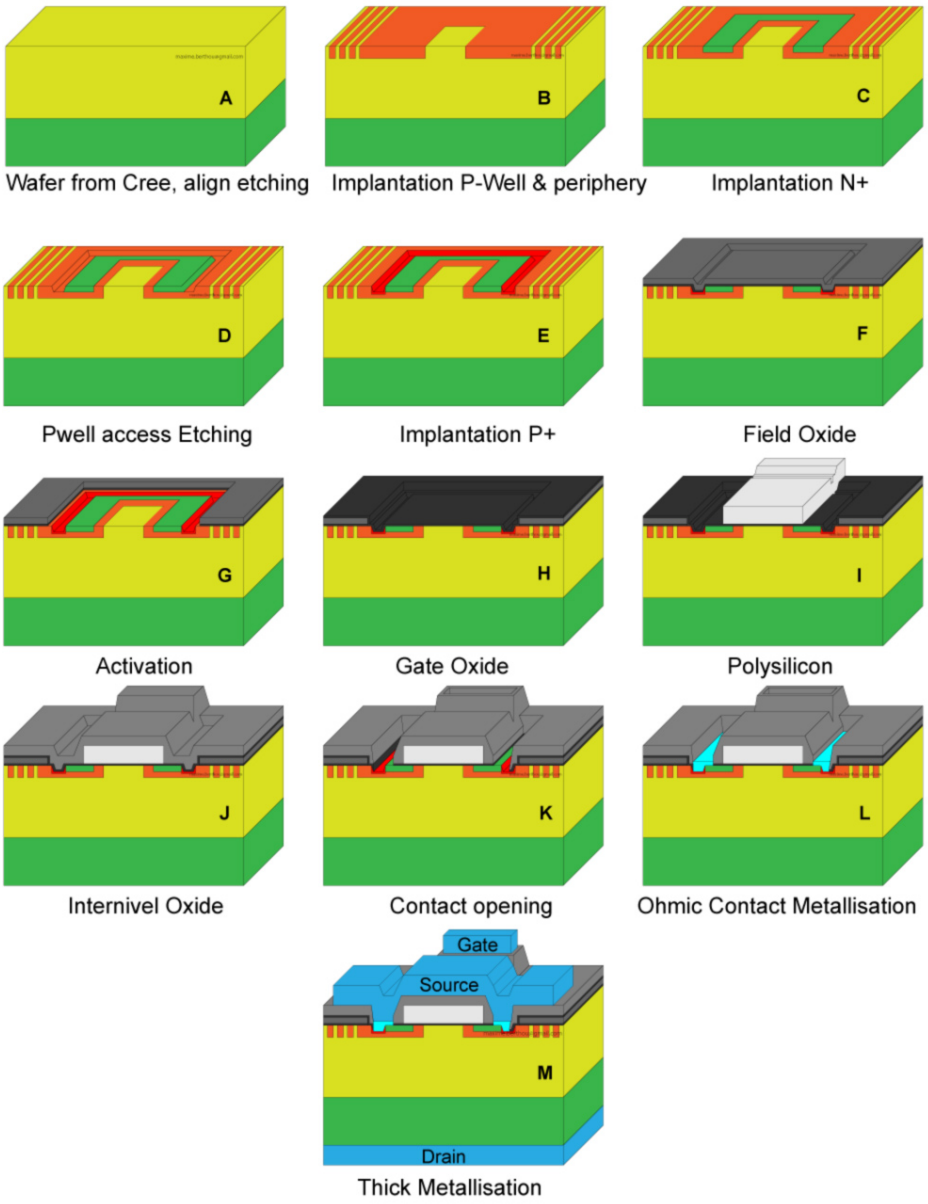

FIGURE 4.3 – Major steps of the SiC VDMOS fabrication process

1. The wafers are first etched to create an alignment pattern ; this level is also used to create the channel stopper and cutting tracks of the wafer. The channel stopper is

a N+ ring done by Nitrogen implantation at the periphery of the device, to ensure the field uniformity around the chips.

2. The JTE areas are then created by the implantation of an aluminium dose of around $1 \cdot 10^{13}\text{cm}^{-2}$ at a depth between 200 and 500nm.

3. The p-well areas were implanted with the profile shown in figure 4.4 to create the internal diode of the MOSFETs and its channel, as shown in figure 4.3b. Guard rings or AGR can also be defined by this step ; in our case the VDMOS termination in made of a JTE with 4 AGR. For the p-well, the wafers have been implanted with aluminium ions at energy up to 1MeV.

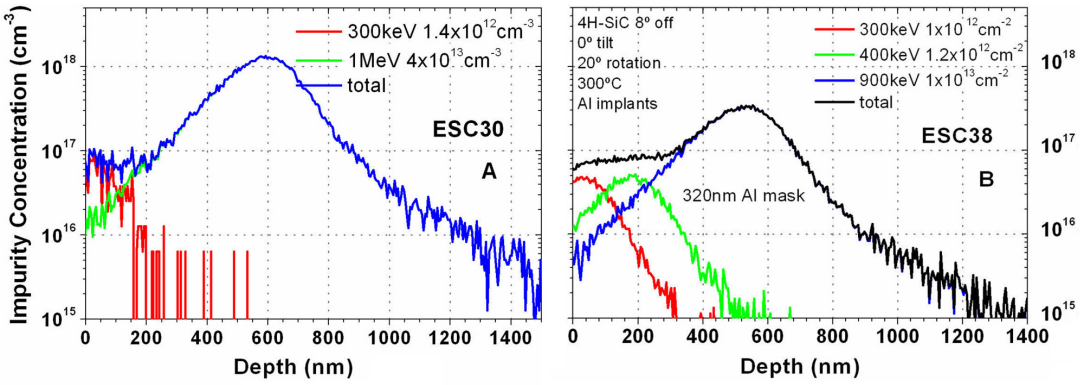

FIGURE 4.4 – Simulated implanted doping profile of the p-well on ESC30 (a) and ESC38 (b)

4. In the next step we implant P+ areas (see figure 4.3e) with aluminium ions of lower energy (50keV) and higher dose of $1 \cdot 10^{14}\text{cm}^{-2}$ to create an electrical access to the p-well from the surface and short-circuit the source to the PWell with the source contact of the MOSFETs.

5. The source was then defined by a Nitrogen implantation of high dose and low energy (see figure 4.3c).

6. After all the implantations, we heal the created defect at the crystal's surface and associate the impurities the samples' crystal by the use of an annealing at 1650°C during 20min.

7. We then deposited a field oxide of 1.5μm to isolate the termination from the active area (see figure 4.3f) and etch it out from the active area (see figure 4.3g).

8. The gate oxide was then grown with a thickness of approximately 45nm (see figure 4.3h)

9. We deposited a 0.6μm thick layer of polysilicon to create the gate and etch the undesired areas (figure 4.3i)

10. We deposited the inter-level oxide with a thickness of 1.5μm (figure 4.3j) and open the oxide at the contact areas of the source and the gate (figure 4.3k).
11. Then we deposited a 100nm thick nickel layer by sputtering and patterned with a lift-off (figure 4.3l) and annealed the contact at a temperature of 950°C during 2min.
12. The back side contact was formed with deposited nickel and titanium layers, annealed at 1050°C with a protective layer on the front side of the wafer, followed by the deposition of a layer of gold or aluminium of 1μm. This step is not shown in the sequence of figure 4.3.
13. We then deposited a 1.5μm thick layer of aluminium on the front side which was patterned by RIE to create the source and gate terminals (figure 4.3m).

4.2.3 Defects induced by the fabrication process

In the processed ESCAPEE samples, an AFM analysis of the surface integrity was performed after the various implantations steps. The samples showed a step of 100nm between the n+ areas and the channel as schematized in figure 4.5 ; this step resulted from a non intentional over-etching of the oxide mask before the n+ implantation. The SiO_2 masking layout used for the implantations was opened by dry etching, which is weakly selective between SiO_2 and SiC. The oxide implantation mask being thick, the accuracy of the etching process was not good enough. This step was believed to be responsible for the high threshold voltage obtained in ESCAPEE VDMOS.

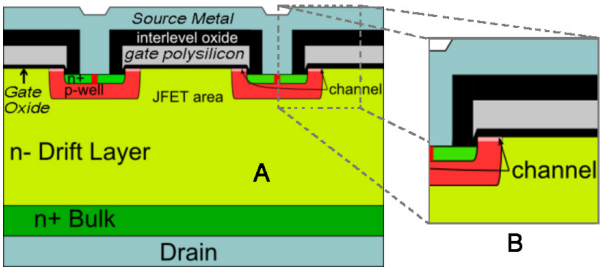

FIGURE 4.5 – Vertical cut of the VDMOS cell structure (A) with an etching step between the source and the channel seen on ESCAPEE wafers and zoom in the channel region (B)

We tried to correct this processing defect via different ways. On three samples, we mechanically levelled the surface by removing the 100nm exceeding crystal. On one sample, we implanted Nitrogen at the surface to create a buried channel at the same level as the source. A last sample was fabricated without modification of the conventional fabrication's process. The different samples are summarised in the table 4.1.

Sample	Process
ESC30a	Planarised -1000Å, annealed with cap layer
ESC30b	Planarised -1000Å, annealed with cap layer
ESC30c	Re-implanted N 20keV $5\cdot 10^{12}$cm^{-2} 1650°C 20min anneal with cap layer
ESC38a	planarized -1000Å, annealed with cap layer
ESC38d	annealed without cap layer 1630°C

TABLE 4.1 – Correction process on the different ESCAPEE 3.5kV VDMOS samples

4.2.4 Electric characteristics

4.2.4.1 Lateral MOSFETs

Lateral n-MOSFETs test devices made on the same wafer as the VMOS have been implemented with the same channel properties and process (figure 4.6). They permit to extract the effective channel's mobility of the VDMOS. As their structure is simpler than the VDMOS, they also permit to diagnose more easily problems linked with the surface area of the VDMOS.

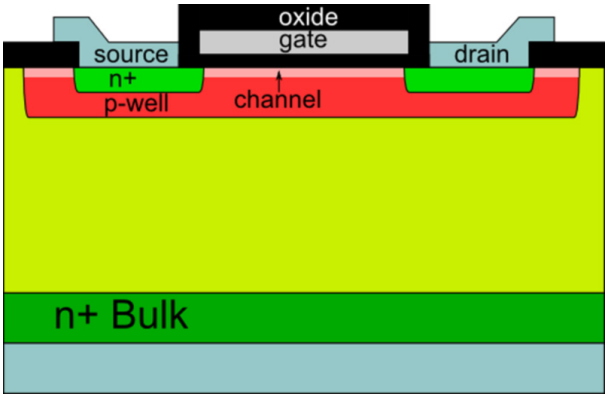

FIGURE 4.6 – implanted LMOS test structure

The forward characteristics of the lateral MOSFETs were extracted on the five samples with $I_{DS}(V_{GS})$ and $I_{DS}(V_{DS})$ measurements. Four notable phenomena are evidenced ; the rectifying source contacts, the variation of the channel properties on different position in the sample, the high value of the threshold voltage, and the low value of the channel mobility.

Table 4.2 summaries the channel's properties for the different samples. The source contact annealing temperature was lowered to 1650°C to avoid the surface damage induced by the high temperature ; unfortunately the metallic contact created thusly has a rectifying character on four of the samples. The effective mobility was grossly calculated by taking the voltage drop induced by the rectifying contact into account.

In table 4.2, we show the mobility, the threshold voltage (V_{th}), drain to source saturation voltage for the on-state (V_{sat}) at $V_{GS} = 40$V and the contact nature to the source and drain. We also indicate an estimation of the variation of the different parameters on the sample as they have an importance in the following diagnostics.

We can note that the sample ESC38d, on which we did not change the fabrication process, shows effective mobility of $1\text{cm}^2/\text{V}\cdot\text{s}$ in the best cases. On the samples with modified fabrication process, ESC38a shows the best results with a maximum effective mobility of $1\text{cm}^2/\text{V}\cdot\text{s}$. Consequently, we see that the effective mobility is similar on device

Sample	μ_{eff} ($\text{cm}^2/\text{V}\cdot\text{s}$)	V_{th} (V)	V_{sat} (V)	Contact	Process
ESC38d	0.8 ± 0.2	10 ± 1	6 ± 0.5	Rectifying	Conventional
ESC38a	0.8 ± 0.2	10 ± 1	6 ± 2	Rectifying	Planarized
ESC30a	0.008 ± 0.002	12 ± 3	3 ± 1	Ohmic	Planarized
ESC30b	0.25 ± 0.05	10 ± 5	6 ± 0.5	Rectifying	Planarized
ESC30b	0.4 ± 0.1	10 ± 2	6 ± 0.5	Rectifying	Re-implanted

TABLE 4.2 – Extracted channel characteristics on the lateral MOSFET of ESCAPEE wafers

with and without the level step at the n+ source, so the low effective mobility is not due to the source's mask over-etching as initially inferred.

On all the samples, the threshold voltage is superior to 9V, which is an indication of low interface quality (roughness) or high channel doping concentration. The threshold voltage on ESC30a and ESC30b varies much more than on sample ESC38a, and the saturation voltage and mobility on ESC30a are far inferior to other samples. The p-well implantation profile on ESC30 produces a thinner channel than on ESC38 ; the planarization process must have reached the p-well doping profile with higher doping concentration on some areas of the samples for ESC30b and on the whole sample for ESC30a.

The re-implantation of nitrogen on ESC30c has permitted to reduce the surface doping level and thus obtain higher channel mobility than on ESC30b, but the step height between the source and the channel is different between the two samples so their comparison is impossible.

In summary, the low mobility of the channel is not due to the etching step between the source and the channel, the source contact still shows rectifying character and the devices with corrected process show lower channel mobility and higher variation over the sample.

4.2.4.2 Vertical MOSFETs

Forward characteristics We measured the forward characteristics of the vertical MOSFETs at room temperature. On this layout, MV09 is the vertical MOSFET with the smallest channel length ; it shows the best forward characteristics. Its Ron-sp and drain saturation voltage was extracted at different positions on each sample and we report the resulting characteristics in table 4.3. The figure 4.7 show the typical characteristics of VDMOS devices fabricated on those wafers.

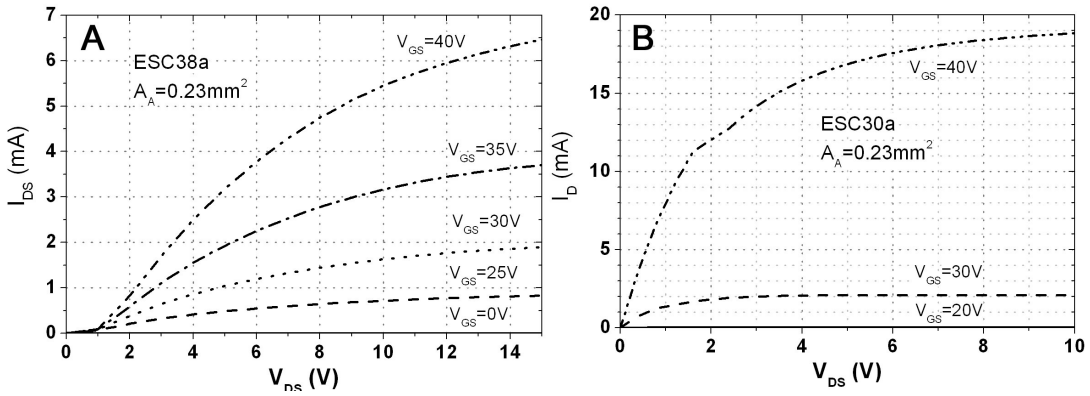

FIGURE 4.7 – Kellog's network for same device with a channel length of 3μm (MV03) on wafer ESC38a and ESC30a

Sample	ρ_{on} MV09 $V_{\text{GS}} = 40\text{V}$ ($\Omega.\text{cm}^2$)	V_{sat} (V)	Contact Nature
ESC38a	0.5	> 10	Rectifying
ESC38d	2.7	> 10	Rectifying
ESC30a	8	2	Ohmic
ESC30b	2.5	5	Rectifying
ESC30d	2.5	5	Rectifying

TABLE 4.3 – Summary of forward characteristics of MV09 on ESCAPEE run

Theoretically, the drift layer contribution to the total resistance of the devices is lower than 40m$\Omega.\text{cm}^2$ (3.5kV devices). So the different samples show specific on-resistance far superior to the theoretical capability of VMOS on 4H-SiC. The only sample that shows ohmic contact to the source is ESC30a as already seen with the lateral MOSFETs.

We can see that the best $R_{\text{on-sp}}$ is obtained on ESC38a, which is the sample that had been planarized and shows the best channel properties on the lateral MOSFETs.

ESC30a is still the worst sample case with the vertical VMOS structure. The other samples showed equivalent channel characteristics and equivalent conductivity on vertical structures compared with test lateral MOS. So the forward characteristics of VMOS are well related with the one measured on the lateral MOSFETs of the same wafers.

We can see that the saturation voltage measured on ESC38's samples are far superior to the one measured on the ESC30. This phenomenon is due to the thicker channel created on ESC38 with a lower p-well dose.

Reverse characteristics We measured the reverse breakdown capability of several devices on the sample showing the best forward characteristics ; ESC38a. Figure 4.8 shows a mapping of the different breakdown voltage attained by the devices measured on wafer. The starting material was selected to get 3.5kV devices.

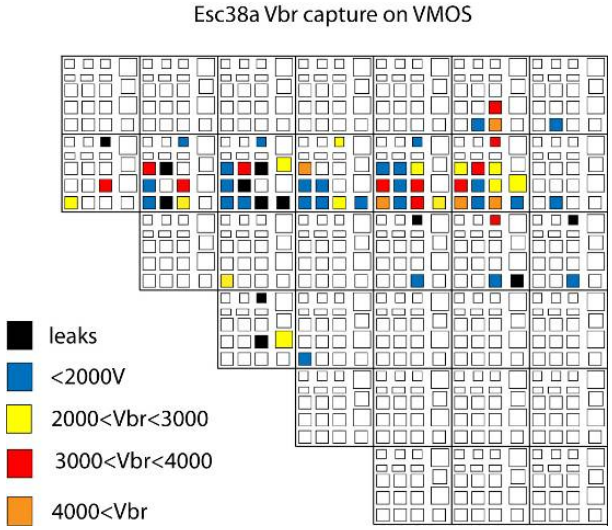

FIGURE 4.8 – Reverse bias mapping on ESC38a

Devices with stripped and hexagonal channels were capable to reach reverse breakdown voltage superior to 3kV. However, many of the devices show reverse capability inferior to 2kV as the polishing process seems to degrade the surface quality of the wafers.

4.2.5 Conclusions

Globally the fabrication process was successful, as the devices show MOSFET characteristics and reverse blocking capability. However, the channel quality is too low and the VDMOS structure requires far lower resistance contribution from the channel. We tried to correct the over-etching of the n-region but the planarization by polishing had even worse effect on the devices. Consequently such MOS channel configuration cannot be used to fabricate good VMOS devices and need further optimization. A new experiment needs to be performed, avoiding the source to channel step, improving ohmic contacts and improving the SiO_2/SiC interface quality. In addition, the high energy Al implantation is too damaging for the surface to get a high channel quality and one must find another way to create the p-well.

4.3 Second and third generation of 4H-SiC VDMOS

In a second phase, we designed two novel VDMOS mask sets implementing new geometries, and we modified the fabrication process taking the previously fabricated VDMOS results into account. As a result, we defined a novel VDMOS process with and without self aligned channel, as well as a VIEMOS fabrication process (see modelling and simulation chapter).

Two new mask sets have been designed with different purposes. The second generation of VDMOS was fabricated with the new mask layout CNM_SIC025 presented in the annexe II. This layout permits to fabricate VIEMOS as well as VDMOS. We processed 3 wafers for VIEMOS and one wafer (ALS7) for VDMOS. The third generation of VDMOS was processed using the new mask set CNM_SiC028. In this mask set, very large area devices are implemented. However, VIEMOS were not considered with this third mask set. For this third generation, 5 VDMOS wafers were processed (PHL5 to PHL9), using the new mask layout CNM_SIC028 presented in the annexe III.

The second and third generations of VDMOS have been fabricated with similar processes but different p-well implantation profiles, making their comparison relevant, so we will present them together. In both technology generations, the etching technique used to open the oxide mask before implantation was optimized. The ohmic contact to the source was improved. We also used a new gate oxide using the Aurore Constant work on optimization of the gate oxide quality using a nitridated thermal gate oxide grown in a RTP oven [90]. The starting wafers used for VDMOS fabrication are listed in table 4.4.

Wafer	Layout	Process	Drift layer	V_{br}
ALS7	CNM_SIC025	VDMOS	30μm $1\cdot10^{15}\mathrm{cm}^{-3}$	4kV
PHL5	CNM_SIC028	VDMOS	12μm $1\cdot10^{16}\mathrm{cm}^{-3}$	1.2kV
PHL6	CNM_SIC028	VDMOS	12μm $1\cdot10^{16}\mathrm{cm}^{-3}$	1.2kV
PHL7	CNM_SIC028	VDMOS	30μm $1\cdot10^{15}\mathrm{cm}^{-3}$	4kV
PHL8	CNM_SIC028	VDMOS	30μm $1\cdot10^{15}\mathrm{cm}^{-3}$	4kV
PHL9	CNM_SIC028	VDMOS	12μm $1\cdot10^{16}\mathrm{cm}^{-3}$	1.2kV

TABLE 4.4 – Samples processed to fabricate the second and third generation of VDMOS

The VDMOS cell structure obtained with both layouts is similar. Other differences of design make each one particular but it will not influence the present analysis. Compared to ESCAPEE, the vertical devices are larger and we used only hexagonal and stripped cell structures with reverse capability superior to 4kV.

4.3.1 Fabrication

In those new wafers, we mainly modified the P-well implantation profiles. The used implantation tools are able of implanting Aluminium from 20keV to 320keV. The p-well profile calculated for the VDMOS is designed to create a n-type channel 50nm deep, doped at $1 \cdot 10^{17}\text{cm}^{-3}$ and a deep p-box doped at $4 \cdot 10^{18}\text{cm}^{-3}$ with the maximum depth attainable with the implanter. The p-well implantation profiles used for the different wafers were simulated with I^2SiC program and are shown in figure 4.9.

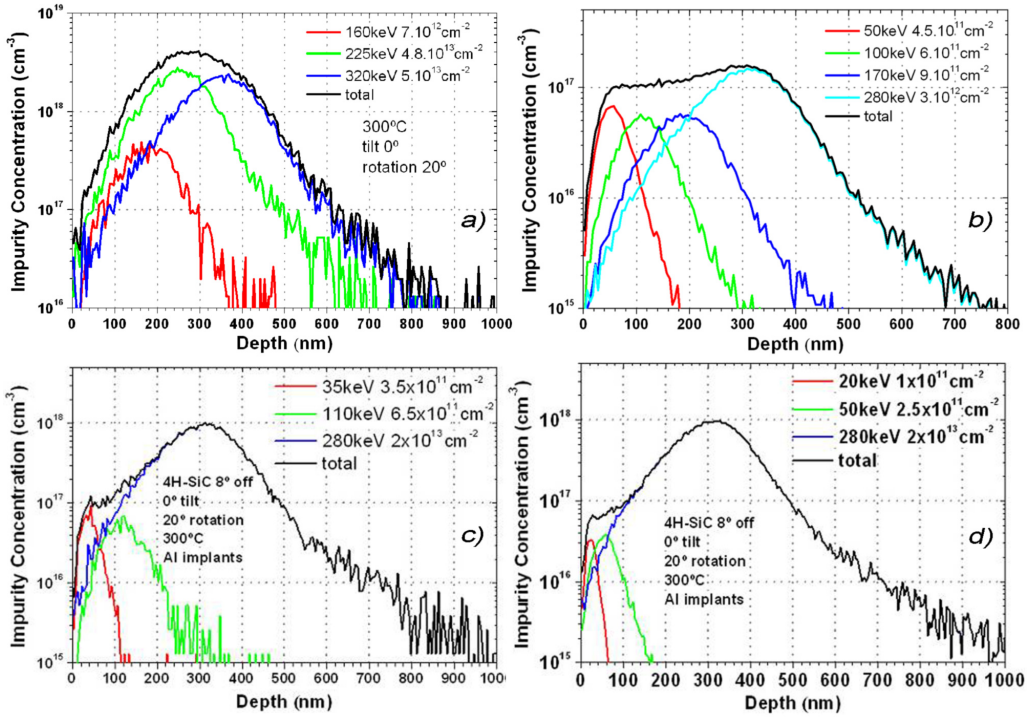

FIGURE 4.9 – Simulated p-well implantation profile used for the VDMOS process on AL8 for (a), PHL5 and PHL6 for (b), PHL7 and PHL9 for (c), and PHL8 for (d)

The SiO_2 masking layer used for the source implantation was removed by wet etching, which has a high selectivity between SiC and SiO_2. The surface integrity of the wafers was then checked by AFM topography and did not show any level difference between the source and the channel areas.

The VDMOS was fabricated with the same process described in figure 4.3, except that the PPLUS contact was not implanted with the same mask as the alignment mask. Moreover the Source contact opening and the Gate contact opening are performed with separate layouts on the second generation.

On both runs, the VDMOS wafers' fabrication was successful and the chips show MOS characteristics as shown in figure 4.10. The contacts to the n+ implantation used to create the source of the MOSFETs show ohmic characteristics. The main incidence

was on PHL5 and PHL6 which shown very leaky characteristics due to the particular p-well implantation profile used on them as we show below.

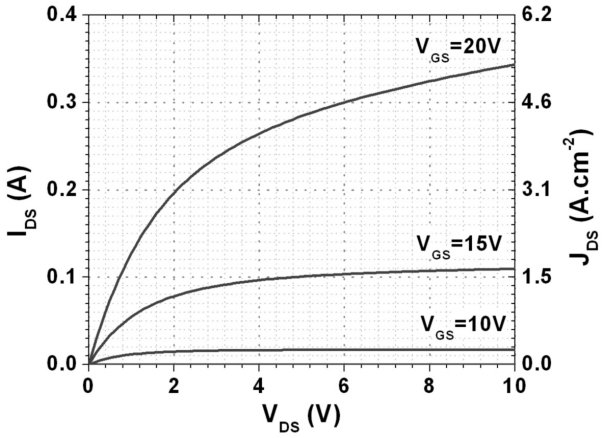

FIGURE 4.10 – I-V curve of a 6.5mm^2 MOSFET of the third generation

4.3.2 Electrical characteristics

4.3.2.1 Leakage current on VDMOS with low-doped p-well

The VDMOS on PHL5 and PHL6 show an asymmetric leakage current from the source to the drain. This leakage phenomenon is also experienced on the lateral MOSFETs. The lateral MOSFET's structure is simpler ; its lateral isolation from the source to the drift layer performed by the p-well implantation is 20um long instead of 2μm on VDMOS structure due to the channel, so the leakage current through the lateral isolation is more limited. Moreover, the gate is not located over n-type epilayer, so the vertical leakage current cannot pass through the gate. These structural differences make the diagnostics easier with the lateral structure.

We first characterized the LMOS laterally and they all showed strong drain leakage current independent from the gate polarisation, and most of them did not show gate leakage current. Then, we measured the leakage current between the source and the back of the wafer. The measured leakage current for LMOS structures on PHL5 at different positions of the wafer is shown in figure 4.11. PHL6 shows the same type of leakage current.

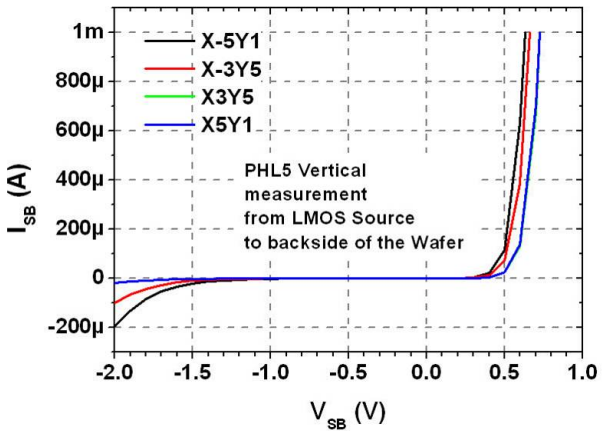

FIGURE 4.11 – Drain to source leakage current on LMOS of PHL5

Other wafers than PHL5 and PHL6 do not show this vertical leakage. Since both wafers share the same low doped p-well implantation profile shown in figure 4.9, we deduce that the p-type area between the source and the drift layer is too thin and too lowly doped. The leakage current starts at approximately 0.5V on this wafer and 0.8V on PHL6. The only possible path for the leakage current is the vertical n+/p/n- junction composed by the source/p-well/drift stack. When the source is biased positively the p-well depletes completely and the leakage due to punch-through begins.

4.3.2.2 Forward characteristics

Regarding forward conduction and channel mobility, on ALS7, the devices show the worst characteristics because the channel is the thinnest one. On PHL8, the channel is thicker and it shows better results than PHL9 & PHL7. Moreover, PHL5 & PHL6 have been implanted with a low-doped p-well profile and present the VDMOS and LMOS devices with the best and most stable forward characteristics we obtained on implanted wafers.

	T_{ch} (nm)	N_{ch} (cm^{-3})	N_{p-well} (cm^{-3})	μ_{eff} ($cm^2/V{\cdot}s$)	ρ_{on-sp} ($\Omega.cm^2$)	V_{br} (V)	V_{th} (V)
ALS7	20	$1{\cdot}10^{17}$	$5{\cdot}10^{18}$	0.06 ± 0.02	10	3000	10 ± 2
PHL5	400	$1{\cdot}10^{17}$	$1{\cdot}10^{17}$	2.5 ± 0.2	0.2	1	4 ± 0.5
PHL6	400	$1{\cdot}10^{17}$	$1{\cdot}10^{17}$	2.5 ± 0.2	0.2	1	4 ± 0.5
PHL7	100	$1{\cdot}10^{17}$	$1{\cdot}10^{18}$	0.3 ± 0.15	1	900	10 ± 1
PHL8	120	$8{\cdot}10^{16}$	$1{\cdot}10^{18}$	1.5 ± 0.5	0.5	700	6 ± 1
PHL9	100	$1{\cdot}10^{17}$	$1{\cdot}10^{18}$	0.5 ± 0.5	1	700	7 ± 3

TABLE 4.5 – Second and third VDMOS generation main electrical results

All the wafers are implanted with profiles having a theoretical surface doping similar to PHL6 and PHL7. Nevertheless, the threshold voltage of the devices on the other wafers are superior, their mobility is lower and not reproducible on the whole wafer. All these effects are explained by the increase in the doping level in the channel area during the fabrication process. We suspect two possibilities : a surface etching during process or the experimental doses and energies of the implanted species in the p-well are not the expected ones due to a drift of the implanter parameters. To find out the cause for these differences in p-well doping profiles, SIMS analysis of the p-well profile of the VDMOS wafer was performed after the fabrication ; the results are presented in figure 4.12.

As we can infer from these SIMS profiles, the actual p-well profile is shifted by more than 100nm toward the surface, so the channel doping is determined by an area of the p-well profile which is more doped. An over-etching of 100nm after the p-well implantation can produce this shift. This reduction of p-well thickness also explains the easy punch-through of the p-well on PHL5 and PHL6.

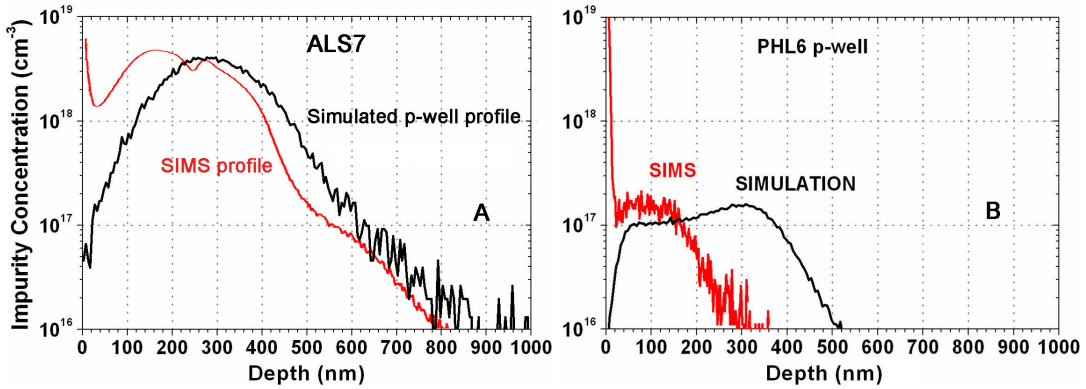

FIGURE 4.12 – SIMS measurement of the p-well profile on ALS7 (a) and PHL6 (b)

4.3.2.3 Reverse characteristics and termination designs

The reverse capability of the devices has also suffered from this p-well depth profile reduction ; only devices on ALS7, which includes a highly doped p-well, were able to withstand reverse bias over 1kV. However, vertical diodes implemented in the mask layout were successfully used to test the termination designs and viability.

The layout CNM_SIC025, used to fabricate ALS7, presents 4 PiN diodes with different termination designs to test their reverse capability separately from the complex design of the VDMOS. The different termination configurations are listed in table 4.6. The anode is created with the p+ implantation used to access the p-well on the VDMOS.

Termination	8 GR	12 GR	JTE & 8 GR	JTE & 12 GR
V_{br}	2.5kV	2.5kV	5.2kV	5.2kV

TABLE 4.6 – Measured maximum Breakdown voltage of diodes with different terminations on ALS7

The reverse bias capability of the different diodes was characterized under probe in a Galden bath. The measurement was performed at CNM with a voltage source of 12kV connected in series with a ki2410, a 50kΩ resistance and the DUT. Considering the drift layer thickness and doping on the wafer, the diode should withstand more than 4kV.

Guard rings The breakdown voltages obtained with the Guard Ring Terminations (see figure 4.23) are spread between 1.5kV and 2.5kV.

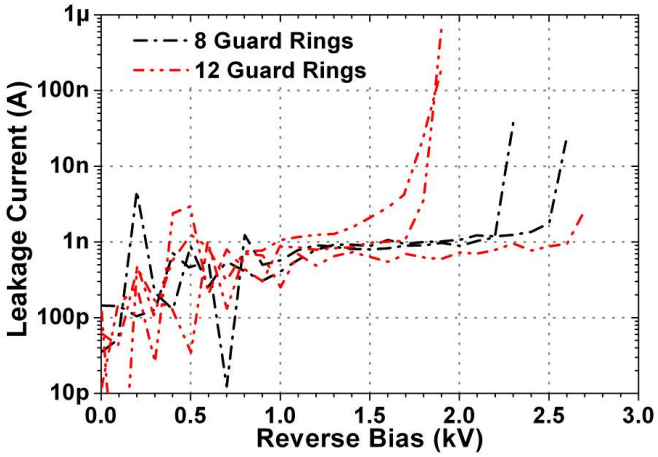

FIGURE 4.13 – Reverse characteristics of PiN diode with guard rings fabricated on ALS7

The diodes with 12 guard rings (D02) show the same reverse capability as the diodes with 8 guard rings (D01). In our design, the distance between the rings increases when going from the centre to the periphery, the distance between the first 8 rings of D02

being similar to D01. If the space between the rings was too small, the equipotential lines' distribution would be controlled on the last rings, and D02 would show higher reverse capability than D01. However, both designs show the same blocking voltage, so the wider spaces between the last rings of D02 do not increase its blocking capability. Then, the space between the first rings on both D01 and D02 is too wide and the GR termination needs to be redesigned with smaller spaces between the rings.

JTE termination The figure 4.14 shows the reverse capability of the PiN diodes with JTE and integrated AGR inside the JTE.

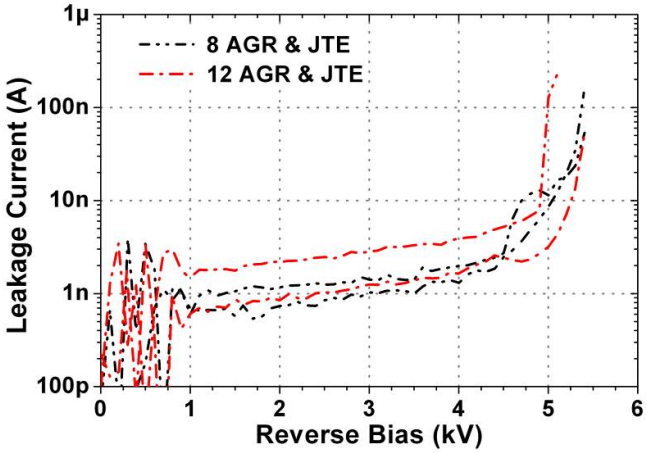

FIGURE 4.14 – Reverse characteristics of PiN diodes with JTE and AGR termination

The two terminations permit to reach a breakdown voltage of 5000V, which corresponds to the maximum breakdown voltage attainable by the drift layer. The optimal termination would be the one with 8 AGR since it occupies a smaller area.

4.3.2.4 Second VDMOS generation (ALS7)

The VMOS of this layout have a JTE with 12 AGR. VDMOS structures are far more sensitive to reverse polarization than diodes as the gate above the JFET must be protected by the depletion region created between the p-well boxes of the VDMOS when the internal diode is reverse biased.

The VDMOS blocking capability was measured, short-circuiting the gate and the source, and applying a positive voltage bias on the drain. Results are shown in figure 4.15 for a large number of structures taken on two different areas of the sample.

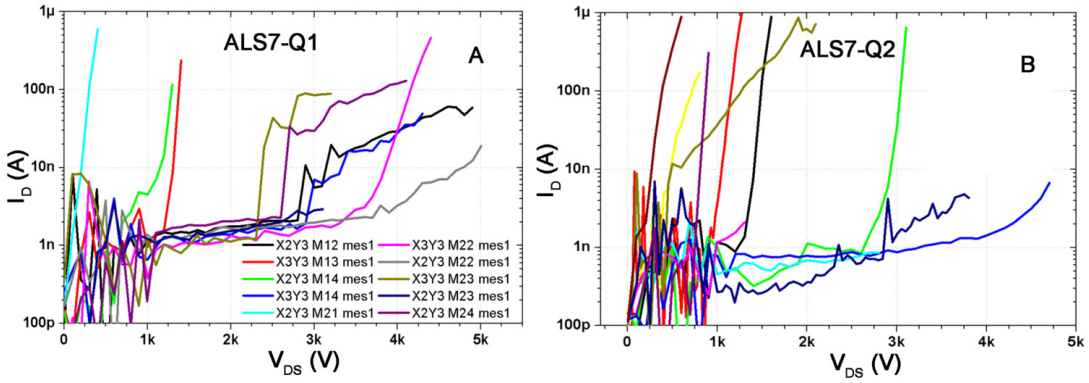

FIGURE 4.15 – Reverse characteristics of VDMOS on ALS7, Quarter 1 (A) and Quarter 2 (B)

We can see that have a strong dispersion of the breakdown voltage values. Some VDMOS were able to withstand voltages over 4kV. However, no VDMOS of $1 \times 1\text{mm}^2$ was capable of standing more than 600V. This difference of results between small and large devices comes from defects in the created structures that have more probability of presence on larger areas.

4.3.2.5 Third VDMOS generation

The figure 4.16 and figure 4.17 show the typical reverse characteristics of VMOS devices on PHL7, PHL8 and PHL9 wafers. The devices were characterized at room temperature, under probes, with the gate shorted to the source.

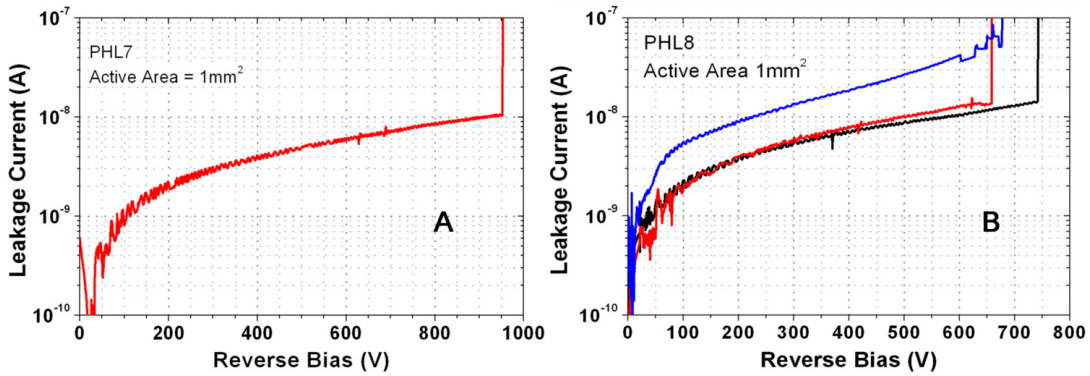

FIGURE 4.16 – Typical reverse characteristics of VMOS on PHL7 and PHL8

They all show far higher leakage current compared to devices on ALS7 shown previously and exhibit reverse capability inferior to 1kV. The devices were characterized again after the breakdown ; they showed lower reverse capability or were inoperative, so the breakdown is destructive. The higher leakage current is due to the punch-through effect in the low doped p-well. It is not yet clear where the breakdown occurs.

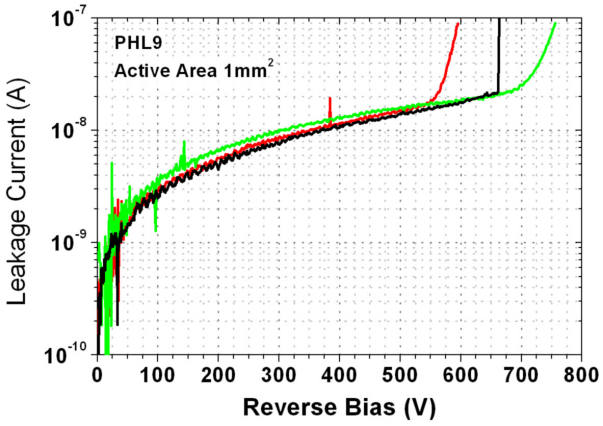

FIGURE 4.17 – Reverse characteristics of VMOS devices on PHL9

Even though the VMOS of the third generation show lower on-resistance thanks to the lower doping of the channel, their reverse capability suffers from the lower p-well doping concentration.

4.3.2.6 Summary and conclusion

Table 4.7 summarizes the forward and reverse characteristics of the different wafers fabricated in the second and third generation. We can see that the devices properties strongly depend on the deep p-well implantation ; the best mobility and conductance have been obtained on the samples implanted with the lowest p-well dose ; PHL5 & PHL6. Moreover, on ALS7, which has the highest p-well doping ; the devices show the lowest effective mobility and conductance but the best breakdown capability.

Sample	T_{CH} (nm)	N_{CH} (cm^{-3})	N_{PWELL} (cm^{-3})	μ_{eff} ($cm^2/V{\cdot}s$)	R_{on-sp} ($\Omega.cm^2$)	V_{BR} (V)	V_{TH} (V)
ALS7	20	$1{\cdot}10^{17}$	$5{\cdot}10^{18}$	0.06 ± 0.02	10	3000	10 ± 2
PHL5	400	$1{\cdot}10^{17}$	$1{\cdot}10^{17}$	2.5 ± 0.2	0.2	1	4 ± 0.5
PHL6	400	$1{\cdot}10^{17}$	$1{\cdot}10^{17}$	2.5 ± 0.2	0.2	1	4 ± 0.5
PHL7	100	$1{\cdot}10^{17}$	$1{\cdot}10^{18}$	0.3 ± 0.15	1	900	10 ± 1
PHL8	120	$8{\cdot}10^{16}$	$1{\cdot}10^{18}$	1.5 ± 0.5	0.5	700	6 ± 1
PHL9	100	$1{\cdot}10^{17}$	$1{\cdot}10^{18}$	0.5 ± 0.5	1	700	7 ± 3

TABLE 4.7 – Second and third VDMOS generation main electrical results

We must increase the p-well's and lower the channel's doping in order to obtain VMOS capable to sustain at least 80% of the theoretical reverse capability like devices on ALS7 and with a higher channel mobility as with devices on PHL5 and PHL6.

However, the channel length provided by the conventional alignment technic is too large and one must further reduce it to obtain a channel contribution inferior to the drift layer's resistivity. The self-alignment technic used in silicon can be used if we don't keep the poly-silicon for the gate afterward.

4.3.3 Self-aligned VDMOS

The third generation VDMOS were fabricated with the new layout CNM_SIC028. One of its principal differences with preceding layouts is that a special source implantation layout level was designed to produce a self-aligned channel.

4.3.3.1 Self aligned Process

In the conventional process, the p-well and Source areas are created with two different masks aligned with an etching pattern created at the beginning of the fabrication process ; this method induces unavoidable misalignment between the p-well and source areas. Due to this precision issue, the channel length cannot be reduced below 2μm (or 0.5μm with the stepper) when using the standard method to create the channel. Moreover the variation of the channel length as a function of its orientation on the wafer will induce a non-uniform distribution of the current in the channels.

The basic self-alignment process is using the same mask to define the p-well and source areas. The p-well masking layer (figure 4.18a) is made of poly-silicon which is oxidized (figure 4.18b) before the implantation of the source (figure 4.18c). When the poly-silicon is oxidized, the polysilicon edge transformed into SiO_2 extends laterally and the opened implantation areas will reduce in size, the difference of width defining the channel length. This technique permits to obtain sub-micron channels without misalignment.

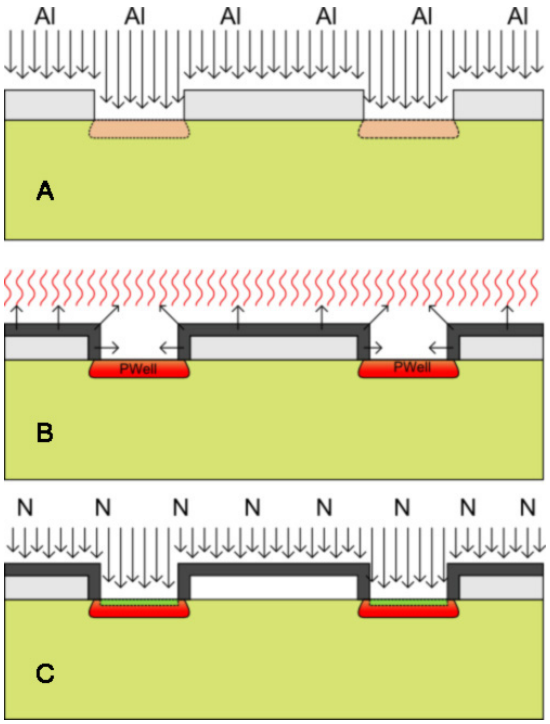

FIGURE 4.18 – Self-aligned source and p-well implantation on the VDMOS

The self aligned and standard processes were tested in the same batch and the sequences of processing steps are compared in the table 4.8. We can see that they use the same number of process and photolithography steps. In the self-alignment process, the p-well masking layer is not removed before the source implantation ; the reduction of the number of mask removal steps can be beneficial to the final surface quality.

Conventional VDMOS	Self-aligned VDMOS
ALIGN mask definition (level1)	ALIGN mask definition (level 1)
100nm SiC etching	100nm SiC etching
Implantation P++	Implantation P++
mask removal and cleaning	mask layer removal and cleaning
JTE mask definition (level 2)	JTE mask definition (level 2)
JTE implantation	JTE implantation
JTE layer removal and cleaning	JTE layer removal and cleaning
PWELL mask definition (level 3)	PWELL poly-silicon mask layer definition (level 3)
p-well implantation	p-well implantation
mask removal and cleaning	oxidation of poly-silicon mask
NPLUS mask definition (level 4)	NPLUS-AA mask definition (level 4)
Implantation of nitride	Implantation of nitride
NPLUS mask removal and cleaning	NPLUS and PWELL masks removal and cleaning
Rest of the process	Rest of the process

TABLE 4.8 – Comparison of the VDMOS process with the classical and auto-alignment method

PHL5 was processed with the self-aligned process. As mentioned before, the devices of this wafer show large leakage current through the p-well of the VMOS due to its low doping concentration. Indeed, the combination of the low doping level of the channel and the short length of the channel permits to obtain VMOS with very low specific on resistance.

4.3.3.2 Channel Mobility

For a drain bias low enough ($V_{DS} < 0.5V$), the devices work as MOSFETs and the channel mobility can be extracted at $V_{DS} = 100mV$. The different MOSFETs were characterized at different positions on the wafer and one can see the obtained effective mobility and drain current of the devices as a function of the gate polarization in figure 4.19.

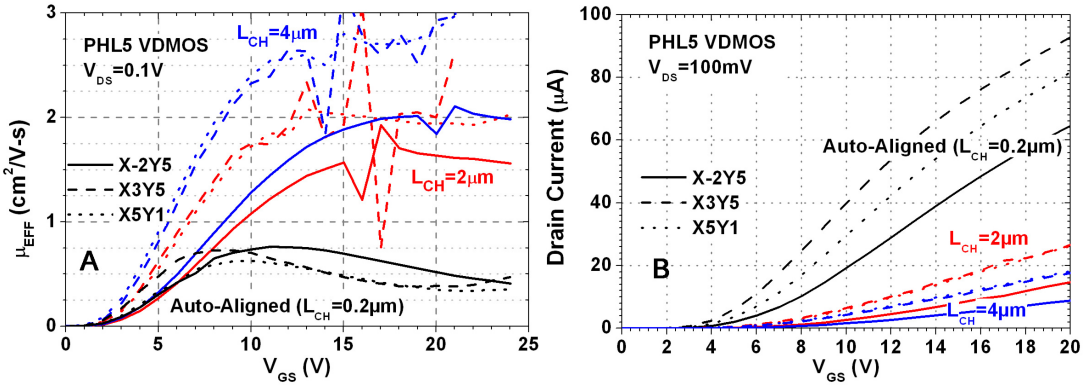

FIGURE 4.19 – Self-aligned channel characteristics compared to classical VDMOS channels on the single channel VDMOS

To calculate the mobility, the gate oxide thickness was approximated in function of the breakdown bias of the gate in a given area and the channel length of the self-aligned devices was approximated to $0.2\mu m$.

We can see that the mobility of the self-aligned channel shows a different behaviour compared to the standard channel ; the maximum peak mobility occurs earlier. Another notable effect is the presence of the roughness degradation of the mobility (on the right part of the curve). This effect can come from a higher roughness in the self-aligned channel, an under-evaluation of the channel length or a parasitic resistance like the JFET area or the drift layer. In conclusion, the self-aligned process provides a shorter channel that is ten times less resistive than standard channel.

VDMOS with an active area of $0.25mm^2$ (see figure 4.20), with multiple stripped channels were characterized to evaluate the impact of the channel size's reduction on multiple channel VDMOS. The figure 4.21 shows the effective mobility and resistivity of multiple-cell VDMOS with and without self-aligned channel.

We can see that the devices with self-aligned channel show the same behaviour than the standard channel VDMOS and the on-resistance is reduced to the order of magnitude of the drift layer resistance. The drift layer contribution to the global resistivity is approximately $5m\Omega.cm^2$ on wafer PHL5, the resistivity of the self-aligned devices reaches values between 25 and $40m\Omega.cm^2$. So the MOS channel area is still a major source of resistance compared to the drift layer.

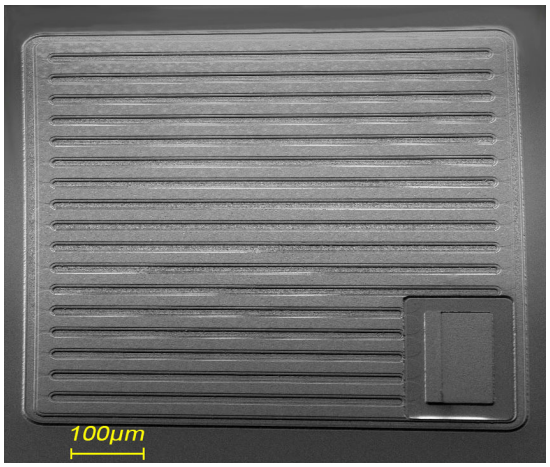

FIGURE 4.20 – 0.25mm^2 VDMOS with multiple stripped channels

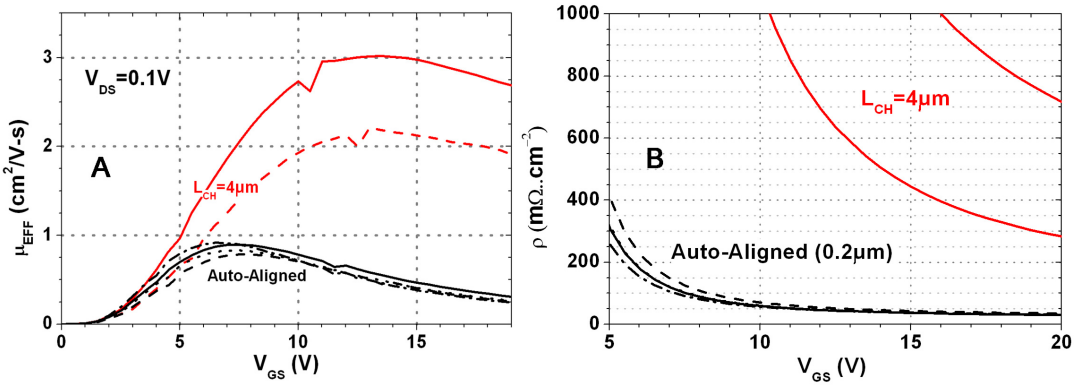

FIGURE 4.21 – Mobility (a) and Resistance (b) of multiple stripped channel VDMOS with self-aligned channel on PHL5

These values have been measured on VDMOS with stripped cell geometry, which is not the best integration option. Moreover, the drift area under the p-well is not fully exploited to conduct the current, so the large size of the cell (30μm) increases the drift layer resistance contribution and limits the integration factor.

4.3.3.3 Self-aligned VDMOS with Hexagonal Cell

The layout CNM_SIC028 includes devices with hexagonal cells of various dimensions. The hexagonal cell design permits to integrate more channel length in the same area. Moreover the reduction of the cell size as tried in Area 2 and Area 3 (see annexes) should reduce further the contribution of the channel and drift layer's resistance to the overall resistance of the devices. Ten VDMOS with different design parameters from AREA 3, as shown in figure 4.22, were characterized at $V_{DS} = 0.1$V with a gate bias sweep from 0 to 20V.

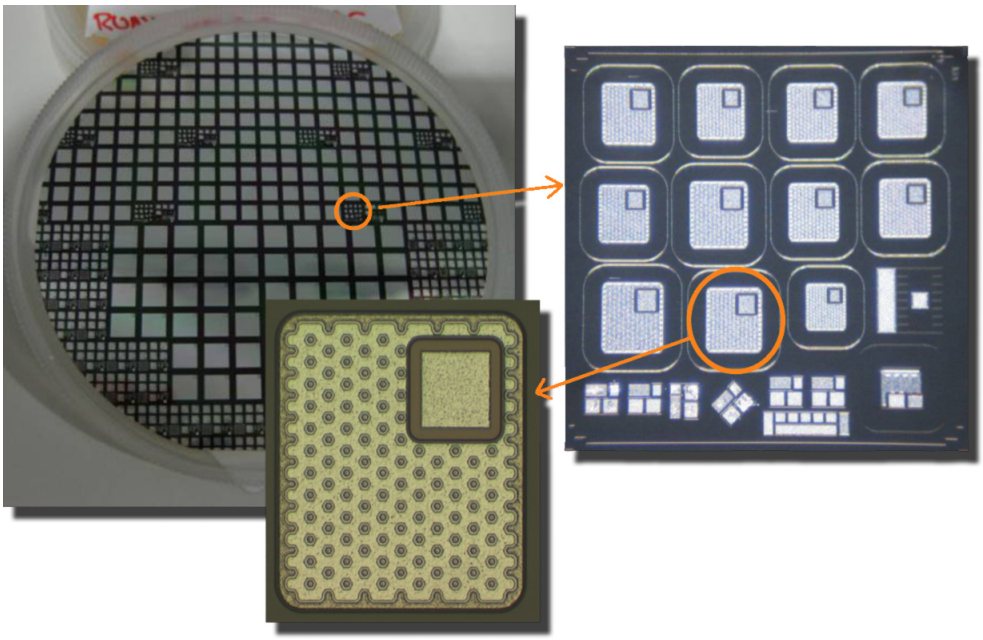

FIGURE 4.22 – Pictures of the VMOS with different cell dimensions in area 3 on PHL5

The devices of the Area 3 have different cell dimensions, with different contact sizes and margins between the alignment levels. It results in different integration factor for the channel and source contact. The table 4.9 summarizes the calculated integration factors for the channel ($R_{CH} = W_{CH}/A_{ACT}$) and source contact ($R_{CN} = A_{CN}/A_{ACT}$) of the VMOS in Area 3.

MOS	04	10	01	09	07	08	03	05	02	11
R_{CH} (cm^{-1})	36.2	46.8	47.3	50.8	50.8	50.8	53	54	57.7	62.8
R_{CN}	5.0	8.6	6.5	4.5	7.2	7.2	7.2	8.1	8.1	7.2

TABLE 4.9 – Channel width to active area and contact to active area ratios for the different MOS with self-aligned channel of AREA 3

The low resistivity of the self-aligned channel permits to reach an overall MOSFET resistivity of the same order as the state of the art devices. Figure 4.23 shows the resistivity

of different devices with self-aligned channel as a function of the channel and contact integration factors shown in table 4.9. As the source contact of the first generation of VMOS was of bad quality, its contribution to the global resistivity can be an issue.

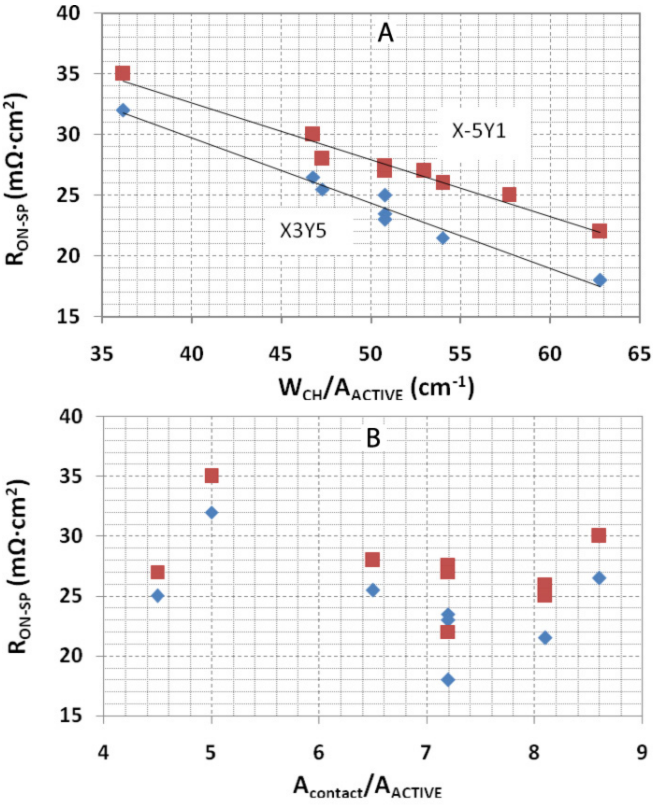

FIGURE 4.23 – Resistivity of VMOS with self-aligned channel as a function of the channel width to active area ratio (a) and contact to active area ratio (b), the squares represent devices in the situated on the left side (X-5Y1) of the wafer and the losanges represent devices on the right side (X3Y5) of the wafer

We can see that the overall MOS resistivity is always proportional to the integration factor of the channel and the contact area has no visible influence. So the channel resistance is still a large component of the chip resistivity. The JFET area length is the unique parameter changing between the VMOS_01, 02, 03 and 04. Increasing the JFET length to 8μm on VMOS 04 increases its overall resistance, the cell being larger ; the integration of channel (R_{CH}) decreases. For the other MOS designs the effect is similar ; the design with the smallest JFET area length (VMOS_02) is always the less resistive one. However, with a lower channel and contact resistance and higher current density, the JFET influence on the resistance will change.

Structures with smaller critical dimension margins have been tested and were functional. The VMOS_11 structure was designed to integrate the maximum channel length in the active area ($L_{\mathrm{CELL}} = 15\mu$m and $R_{\mathrm{CH}} = 63\mathrm{cm}^{-1}$) by reducing channel length, distances between contact opening and metal patterns. It shows on-resistance of 18mΩ.cm^2, which

correspond to a reduction of 33% on the resistivity compared to the standard structure VMOS_01 ($L_{\mathrm{CELL}} = 20\mu$m and $R_{\mathrm{CH}} = 47.3\mathrm{cm}^{-1}$) with an on-resistance of $26\mathrm{m}\Omega.\mathrm{cm}^2$.

The critical dimensions could be used as novel standard parameters in the next generation of devices. Further reduction of the margin is possible with adequate processing equipments. Availability of six inches SiC wafers will permit to use standard tools used in Si technology with higher precision. It will allow reducing alignment margins, thus increasing the channel integration and its contribution to the devices' on-resistance.

These devices have been fabricated on a wafer with a thin drift layer, so its contribution is inferior to $5\mathrm{m}\Omega.\mathrm{cm}^2$ to the devices' on-resistance. With a thicker drift layer used for 3.3kV devices, the channel contribution would be equivalent or inferior to the drift contribution to the total on-resistance of the device.

4.3.3.4 Large VMOS with Self-aligned channel and Hexagonal cells

The CNM-SiC028 layout includes multiple cell VMOS with a large active area of 6.5mm^2 in Area 1 & 2 and 14.2mm^2 in area 5 (see figure 4.34).

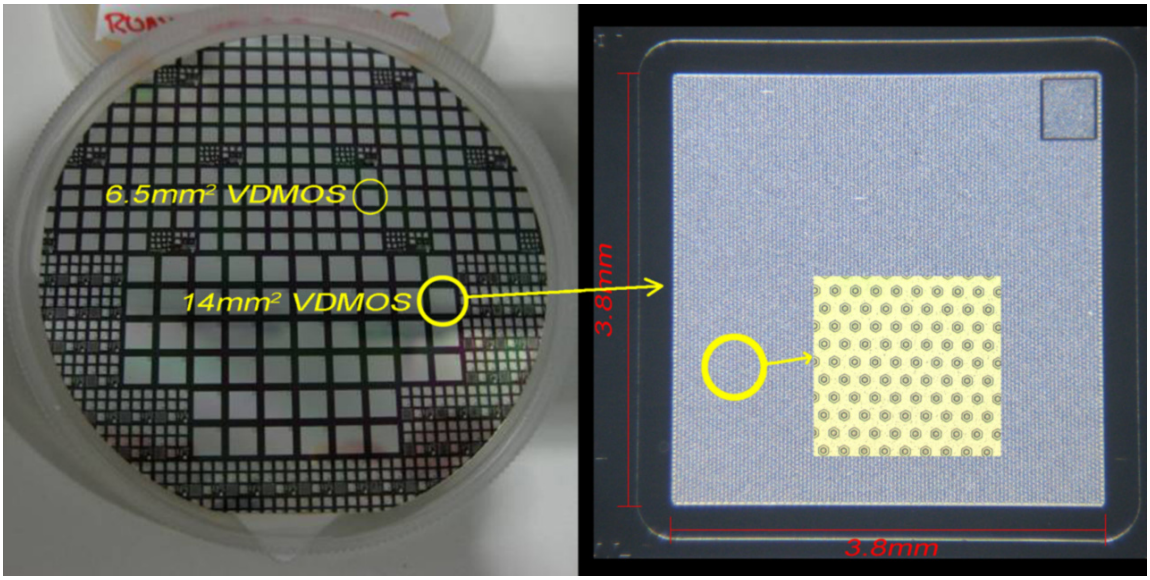

FIGURE 4.24 – Pictures of the large area VMOS on PHL5

We measured the transfer curve of 6.5mm^2 devices at different positions on the wafer PHL5 for a drain bias in the ohmic region (V_{DS} = 0.1V), where the device does not show leakage current. We extracted their specific on resistance versus the gate bias (see figure 4.25b) and reported the specific on resistance for a fixed gate bias (V_{GS} = 10V) in different area of the sample shown in figure 4.25a.

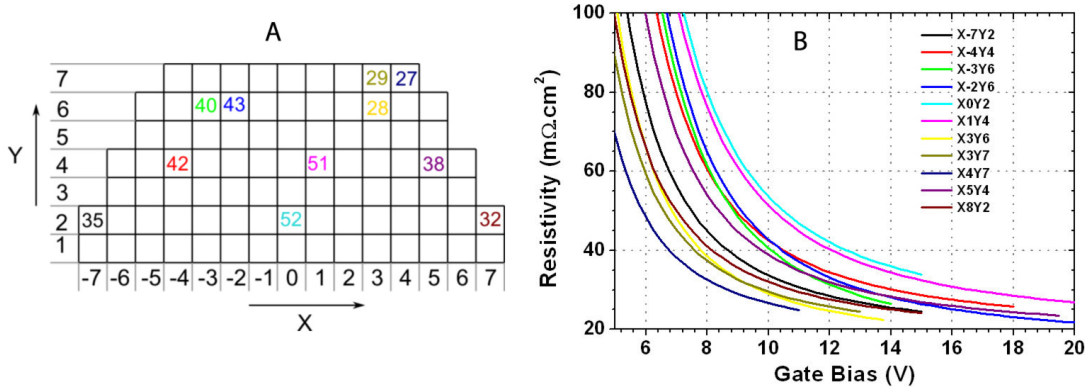

FIGURE 4.25 – Mapping (a) of the measured ρ_{on-sp} at V_{GS} = 10V and corresponding RON-SP (V_{GS}) at V_{DS} = 0.1V in (b) of MOSFETs with an active area of 6.5mm^2 and an self-aligned channel on PHL5

For each device reported in figure 24b, the gate voltage was increased till the breakdown. The last point of each curve corresponds then to the maximum gate voltage ca-

pability. We can observe that devices showing the lower resistivity also show lower gate breakdown and threshold voltage. Then the difference of resistivity between the devices is mostly due to the different gate thickness. The largest devices on the layout (14mm^2, see figure 4.24) are located on the lower part of the wafer. They are multiple hexagonal cells design with both self-aligned and classical channels 4μm long. We measured the transfer characteristics of both types of devices at gate bias from 0 to 15V and drain biased in the ohmic region, and we extracted the resistivity versus the gate bias (see figure 4.26).

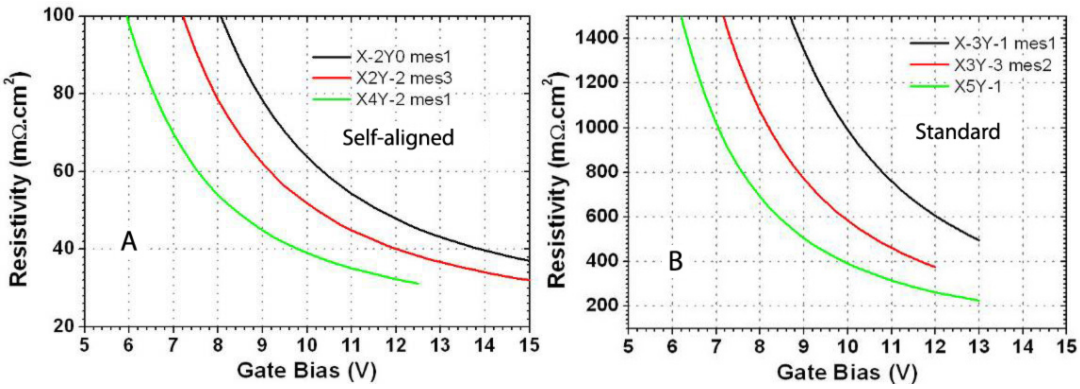

FIGURE 4.26 – Resistivity of standard channel (B) and self-aligned (A) vertical MOSFETs of 14mm^2

We can see that the VMOS with long channel show a high resistivity, between 200 and 500mΩ.cm^2, due to its channel length and that the ones with self-aligned channels are far less resistive.

On 6.4mm^2 and 14mm^2 devices with self-aligned channel, the devices exhibit resistivity between 25 and 50mΩ.cm^2, which fits well with the values obtained on the small area VMOS, demonstrating a good scalability of the devices regarding this parameter. We have to note that the large devices present standard cell size ($L_{\mathrm{CELL}} = 20\mu$m), which is not the optimal one as seen on the small area VMOS_01. We can then improve their forward characteristic by reducing the cell size as shown with VMOS_11 design ($L_{\mathrm{CELL}} = 15\mu$m).

4.3.4 Temperature dependence of the fabricated VMOS' forward characteristics

Silicon Carbide devices present a great interest for its potential at high temperatures. Its chemical stability and large gap allows it to keep its semiconductor properties over 800°C. As VMOS made on SiC are capable to operate up to 300°C, many applications plan on exploiting the full SiC converters at operating temperatures above 100°C, so that the cooling system can be reduced. The figure 4.27 shows the I-V characteristics of a VMOS on PHL8 at room temperature and 150°C. The device biased at V_{GS} = 15V shows an on-resistance of 450mΩ.cm^2 at room temperature and 180mΩ.cm^2 at 150°C with higher saturation voltage.

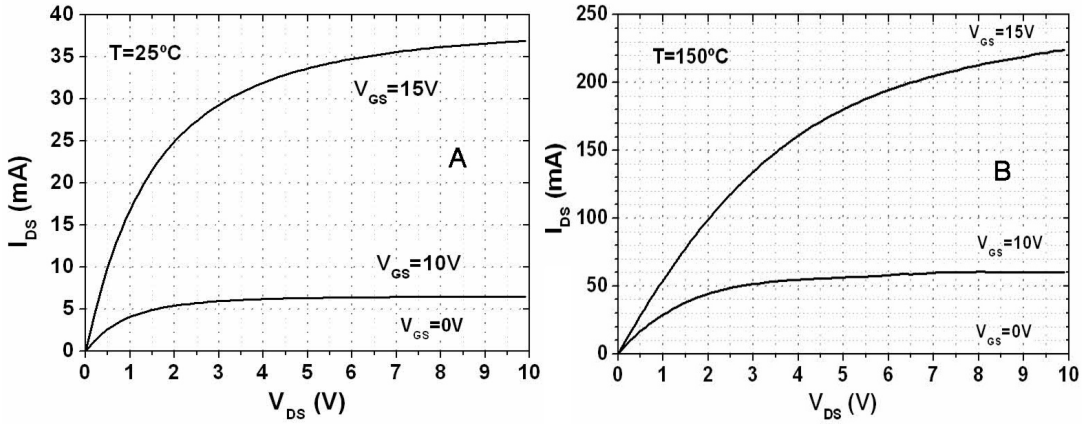

FIGURE 4.27 – I-V characteristics of a 1mm^2 4H-SiC VMOS on PHL8 at 25°C (a) and 150°C (b), and different gate biases

The figure 4.28 shows the transconductance characteristics of the device at V_{GS} = 100mV for both temperatures, we can see that the threshold voltage decreases and the current density increase thanks to the increasing in the channel mobility.

This effect is well known and comes indirectly from the reduction of the bandgap as the temperature increases. As the bandgap is reduced, the effective interface traps density decreases, fewer carriers are captured, which in turn increases the density of free carriers in the channel and the coulomb scattering mechanism is reduced, so the saturation current and the mobility in the channel increase.

Such an effect can be seen as positive, but it shows that the channel's resistance still dominates the VMOS' resistance and the gates' interface presents high density of interface states, which are inducing low mobility and reliability of the MOS channel. Once the interface states density is reduced, this effect will be minimized and the device's resistance will show a positive temperature resistance, like the Schottky diodes, due to the reduction of the mobility in the drift layer.

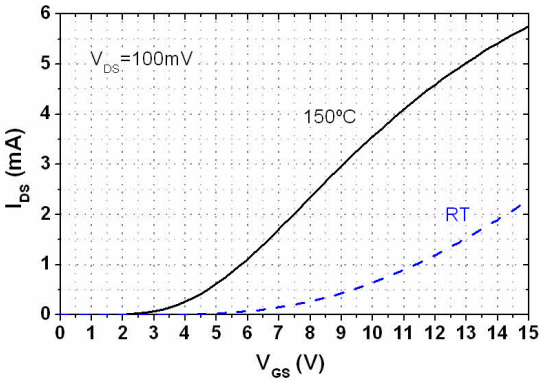

FIGURE 4.28 – Transconductance characteristics at VDS=100mV for the same VMOS device at room temperature and 150°C

4.3.5 Conclusions

The self-aligned channel permits to reduce the channel length so that its contribution to the total device's resistivity can be in the same order as the drift layer contribution. We still experience low effective field effect mobility under $3cm^2/V{\cdot}s$ due to the high channel's doping. By reaching mobility superior to $20cm^2/V{\cdot}s$, as obtained in our gate oxides development works, we would obtain a negligible channel resistivity compared to the drift layer of 1.2kV devices.

The design of the SiC-VDMOS could then be further optimized to reduce the cells size but also integrate sensors usable by smart drivers, which permit to increase the lifetime of the devices and their efficiency.

4.4 Integrated Temperature and Current Sensors in VMOS

In the layout CNM_SIC028 used for the fabrication of the third generation of VMOS, we included experimental VMOS structures with two types of sensors in the area 6 as shown in figure 4.29.

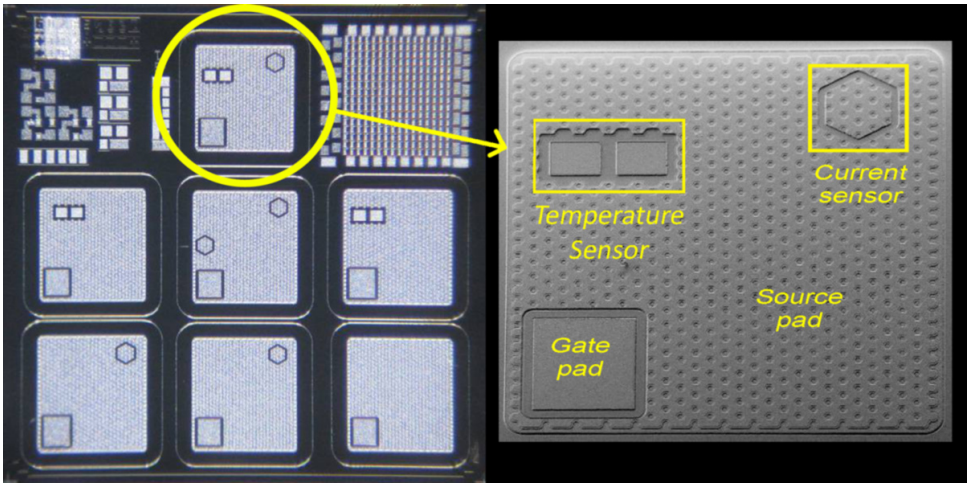

FIGURE 4.29 – SEM picture of VMOS with a temperature and a current sensors and optical photography of the Area 6 after fabrication

4.4.1 Integrated temperature sensor

The temperature sensor is a resistance that varies with the temperature ; the resistance is made of two P+-type ohmic contacts connected by a low doped P-type area (see figure 4.30). The contacts are oversized (134μm $\times$ 100μm) so that the low doped semiconductor area's resistance dominates over contact resistances.

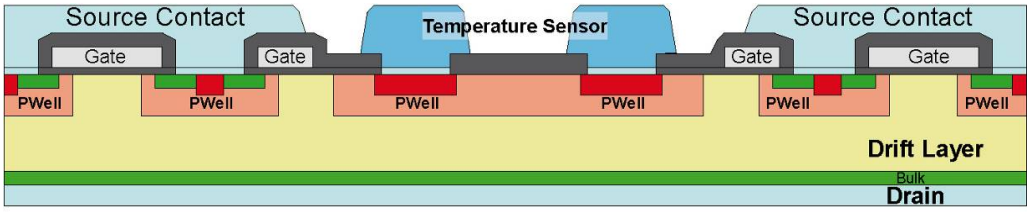

FIGURE 4.30 – Integrated Temperature Sensor within VMOS structure

The P+ areas are separated by 34.8μm. Considering a 0.3μm deep p-well doped at $5\cdot 10^{17}\text{cm}^{-3}$, when the aluminium impurities are totally activated (over 220°C), the mobility is lower than $25\text{cm}^2/\text{V}\cdot\text{s}$, so the resulting conductivity of the layer should saturate at 90μS. The characteristic of the temperature sensor was measured from room temperature to 275°C (see figure 4.31A). We extracted the current value at different temperatures for a sensor bias voltage ($V_{\text{T}-\text{SENS}} = 1\text{V}$) lower than the bipolar junction activation voltage (junction formed by the p-well and the drift layers). We plotted the current versus the temperature to draw figure 4.31B. From figure 4.29A we can check that the contacts show ohmic behaviour. Figure 4.31B shows that the sensors' impedance between RT and 275°C is correlated to the temperature with a bijective function.

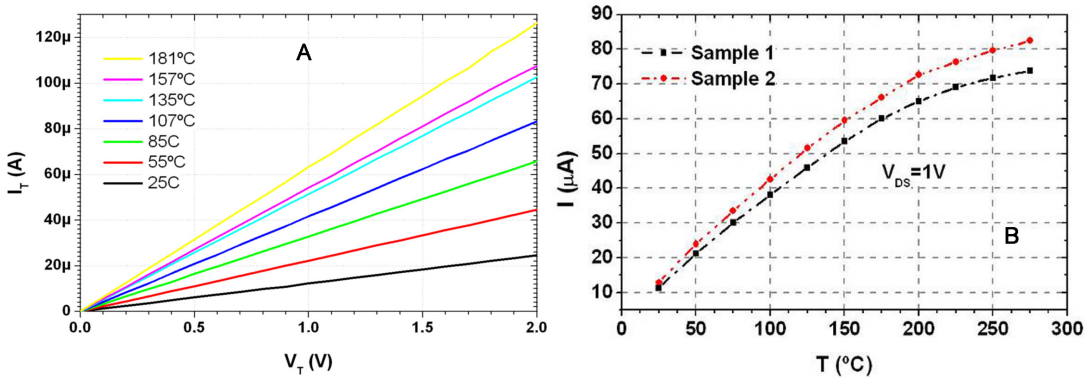

FIGURE 4.31 – Temperature sensor characteristics as a function of the temperature

We measured the forward and reverse characteristics of the VMOS having an integrated temperature sensor on PHL7. The measured reverse characteristics of the VMOS show that the sensor deteriorates neither the forward nor the reverse capability up to 600V.

Other type of sensors can be integrated in the devices, and the current sensor is one of the simplest.

4.4.2 Integrated current sensor

The current sensor is made of several VMOS cells isolated from the rest of the source's cells as shown in figure 4.32. If the channel resistance contribution to the global VMOS resistance is dominant, the current seen by the sensor is proportional to the channel width of the sensor. If the drift resistance is dominant, the current passing through the sensor is proportional to its surface.

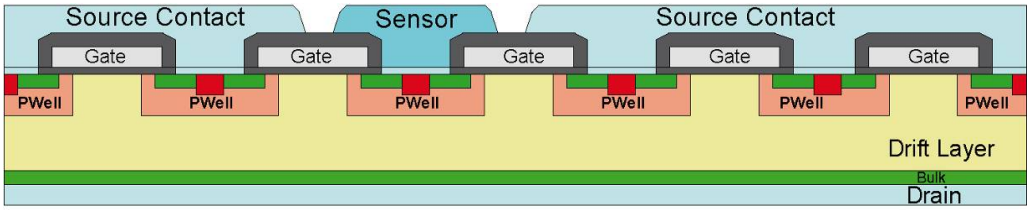

FIGURE 4.32 – Vertical cross section of the integrated Current Sensor within the VMOS structure

The current sensors have been initially characterized biasing both sensor and VMOS as shown in figure 4.33a. The current through the sensor (I_{sens}) is measured separately from the VMOS drain-source current (I_{DS}) using a current source with a low internal impedance. At room temperature, the measured sensors exhibit the same current behaviour as the main VMOS current (figure 4.33b). The current ratio $I_{\text{DS}}/I_{\text{sens}}$ is measured in the ohmic conduction mode and ranges from 35 to 40, depending on the measured wafer area. The expected theoretical ratio, taking into account the channel width on mask, was 40. The small ratio difference between the design and experimental data is linked with the technology process's uniformity (dimensions, channel length and ohmic contacts).

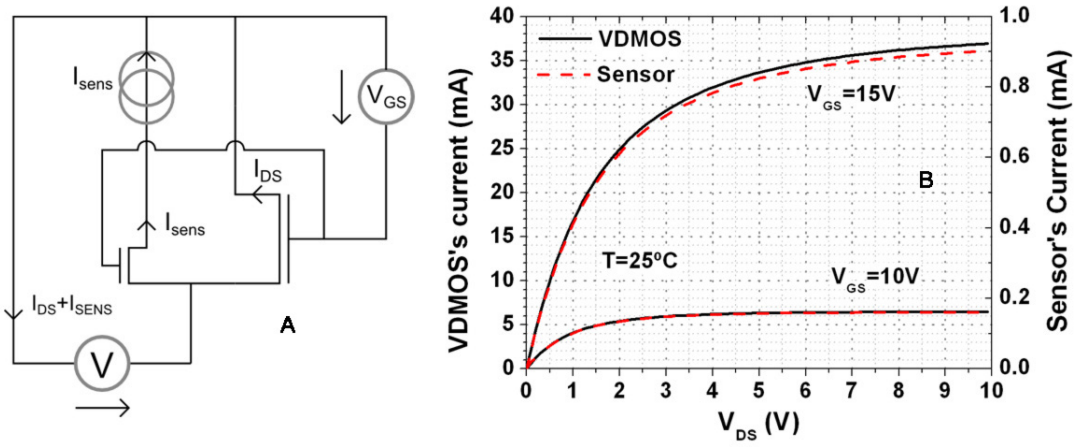

FIGURE 4.33 – Measurement configuration used to characterize the sensor and VMOS (a) and I-V curve measured at 25°C (b)

The devices were also characterized up to 150°C (figure 4.34a). When temperature increases, the current ratio, $I_{\text{DS}}/I_{\text{sens}}$, increases from 40 at RT to 41 at 150°C. This slight

change is due to the reduction of the channel resistance and increases in the drift resistance contribution to the VMOS conduction mode. Then, the impact of current spreading effect explained below is enhanced at higher temperature.

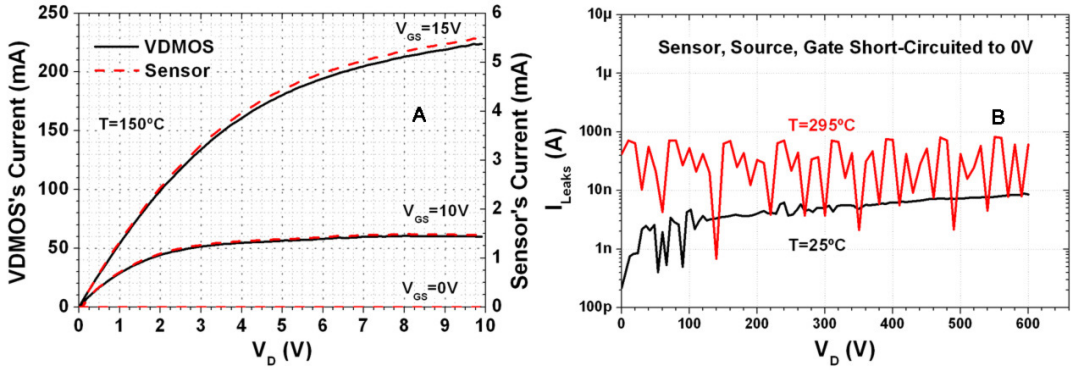

FIGURE 4.34 – VMOS and its Current sensor (a) forward characteristics at 150°C and (b) reverse characteristics up to 600V at room temperature and 295°C with source, sensor and gate shortcut

In addition, in figure 4.34b we can see that the sensor does not degrade the blocking capability of the device up to 295°C.

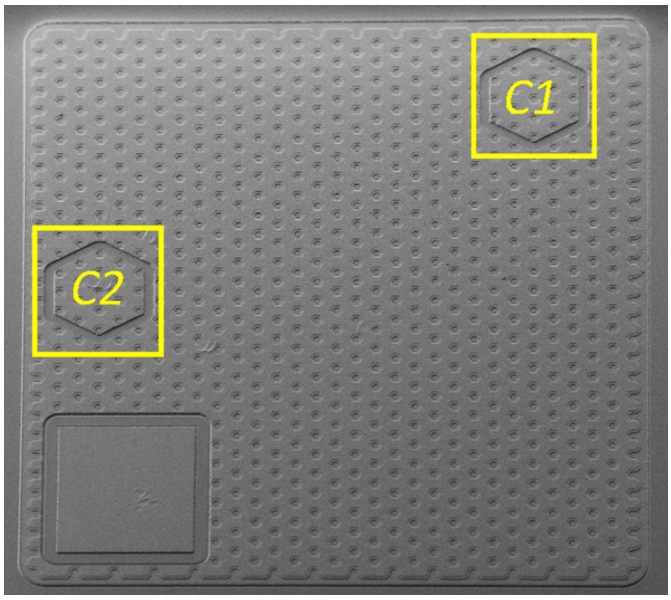

FIGURE 4.35 – SEM picture of VMOS with two current sensors

In another design, two current sensors have been placed on two different areas on the VMOS to check if the cells' conductivity varied with their position on the device. They are marked as C1 and C2 in figure 4.35.

The VMOS and its two current sensors were characterized when forward biased under probe and show the characteristics presented in figure 4.36. Both sensors show characteristics proportional to the one of the device's source with a conversion coefficient of

40 ± 1. Taking the previous results showing good scalability of the forward characteristics on large devices together with this result, we can infer that the current is uniformly distributed over the device's cells, so the channel characteristics are also constant over each device.

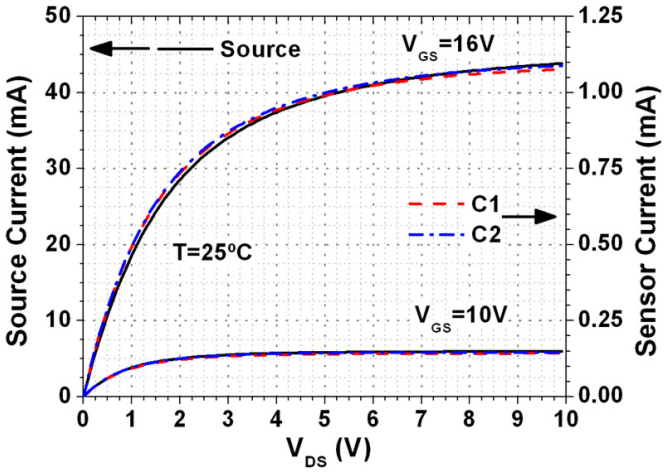

FIGURE 4.36 – Double current sensor VMOS forward characteristics

The implantations of the pwell and channel have a large impact on the VDMOS characteristics, and structures avoiding them have been proposed as a solution.

4.5 VIEMOS

4.5.1 Design

The VIEMOS (Vertical Implanted and Epitaxied MOS) is a VMOS which channel has been epitaxied (p-type) after implantation of the p-well. It is designed to avoid the destructive effect of the p-well implantation in the channel of the VMOS.

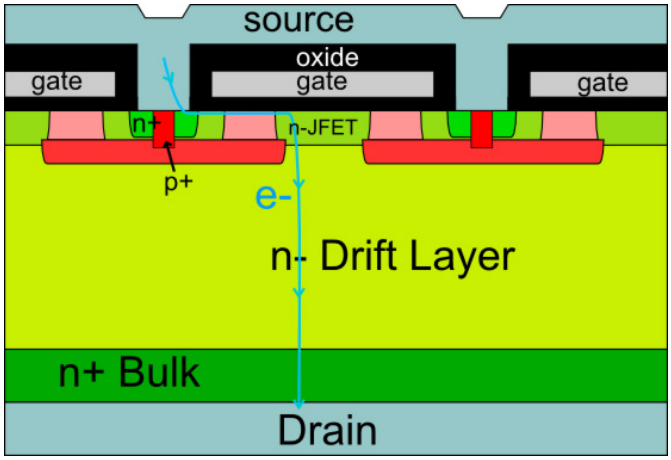

FIGURE 4.37 – Schematic view of the VIEMOS structure

The previous experiment shows that it is very difficult to obtain high channel mobility with the fabrication process of the VMOS, so we decided to investigate the VIEMOS design. The structure was first studied from a simulation point of view with Sentaurus (see chapter 2). It permitted to choose the design parameters for the fabrication. Then, we designed a layout including 9 VMOS and 4 vertical PiN diodes, and fabricated the devices.

4.5.2 Fabrication process

The differences with the standard VMOS process are the thin p-type layer growth (see figure 4.38c) and the JFET implantation (figure 4.38f) to compensate the p-type epitaxy in the JFET area.

We chose to compensate the epitaxial layer on both side of the channel with the JFET implantation. It permits to determine the channel length with one mask (see figure 4.38f), the minimum channel length is determined by the mask's resolution. In the standard VMOS fabrication process shown in figure 4.3, the channel length determined by the distance between the N+ implantation and the end of the p-well. Consequently, the channel length accuracy depends on both masks and alignment precision, using a channel length under 2μm is risky. The VIEMOS process permits to create a self-aligned channel 1μm long without risk.

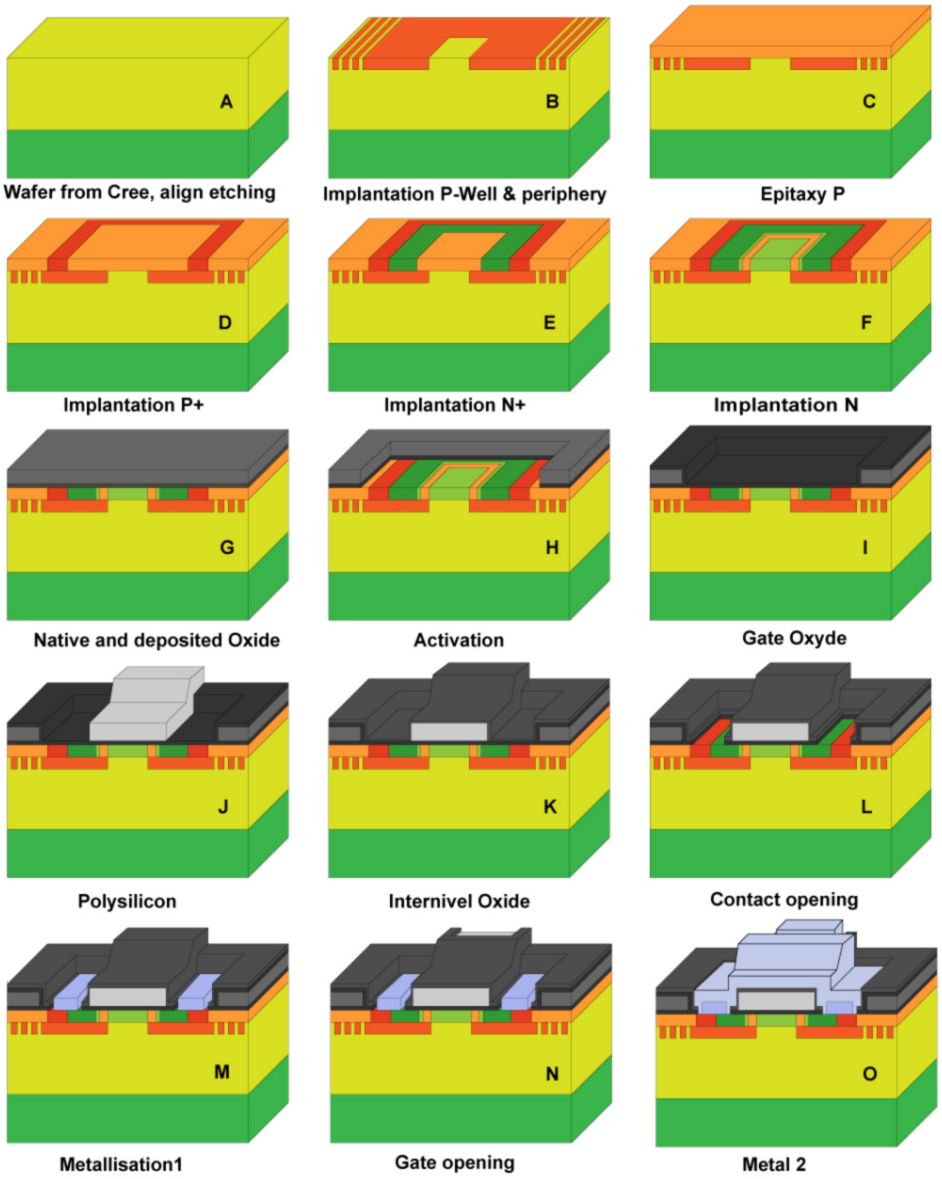

FIGURE 4.38 – Major VIEMOS fabrication process steps

In figure 4.38, the back contact formation has been omitted for the sake of description simplicity, it can be deposited and annealed after the step g and covered with a protective layer to avoid any oxide formation in the subsequent steps. We designed the mask set with the capability to use it to fabricate both VIEMOS and VMOS structures. The fabrication process flow differs by the epitaxial step and the compensation of the JFET area but similar layouts can be used for the other steps.

4.5.3 Electric characterization

The VIEMOS were fabricated on three wafers with the characteristics summarized in table 4.10.

Wafer	Layout	Process	Drift layer	V_{BR}
ALS6	CNM_SIC025	VIEMOS	$12\mu m$ $5\cdot 10^{15}\text{cm}^{-3}$	1.5kV
ALS8	CNM_SIC025	VIEMOS	$30\mu m$ $1\cdot 10^{15}\text{cm}^{-3}$	4kV
ALS9	CNM_SIC025	VIEMOS	$30\mu m$ $1\cdot 10^{15}\text{cm}^{-3}$	4kV

TABLE 4.10 – characteristics of the VIEMOS samples fabricated during the run ALS

Unfortunately the p-type epitaxial layer re-growth process done in ACREO failed on the wafers dedicated to the VIEMOS fabrication. After the epitaxy, we performed SIMS and SEM analysis on the samples, which are presented in the part 4.6. The SIMS analysis did not detect aluminium impurities in the p-well or the JTE areas nor at the surface of the wafer. As a consequence, all the samples showed vertical leakage current as shown in figure 4.39.

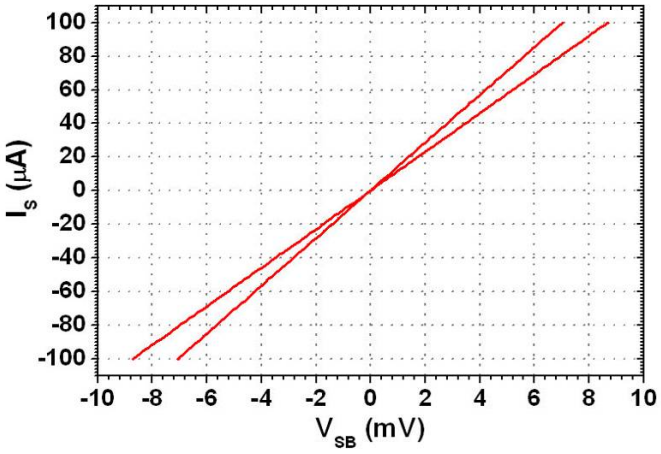

FIGURE 4.39 – Vertical leakage current from Source of a lateral MOS to the bulk at different positions on the wafer

The P+ areas implanted after the p-layer growth to contact the p-well are present, so only the p-type lateral MOSFETs in the CMOS structures are functional on the VIEMOS samples.

4.5.4 Lateral PMOS

The figure 4.40 shows the structure of the fabricated lateral PMOS on ALS8 and ALS7. The channel area of the PMOS devices on ALS8 has been implanted with a doping concentration of $1 \cdot 10^{17} \mathrm{cm}^{-3}$ to compensate the p-type layer. On the wafer ALS7, the channel is created directly on the drift layer, which concentration is $1 \cdot 10^{15} \mathrm{cm}^{-3}$.

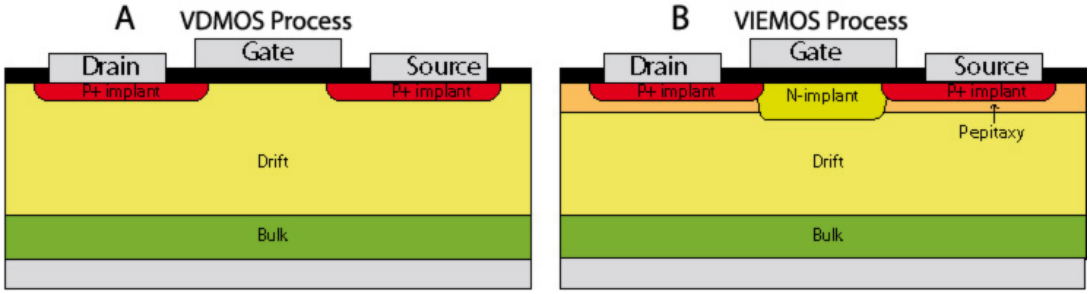

FIGURE 4.40 – Schematic view of the PMOS structure fabricated with the layout CNM_SiC025, for the VDMOS process used on ALS7 (a) and the VIEMOS process (b) used on ALS8

The extracted effective mobility of the lateral pMOSFETs measured on ALS8 and ALS7 are shown on figure 4.41. We can see that the sample that has not been implanted shows nearly twice higher mobility and twice smaller threshold voltage. The damages generated by the implantation process reduce the SiC/SiO_2 interface quality and the high channel doping concentration also increases the threshold voltage.

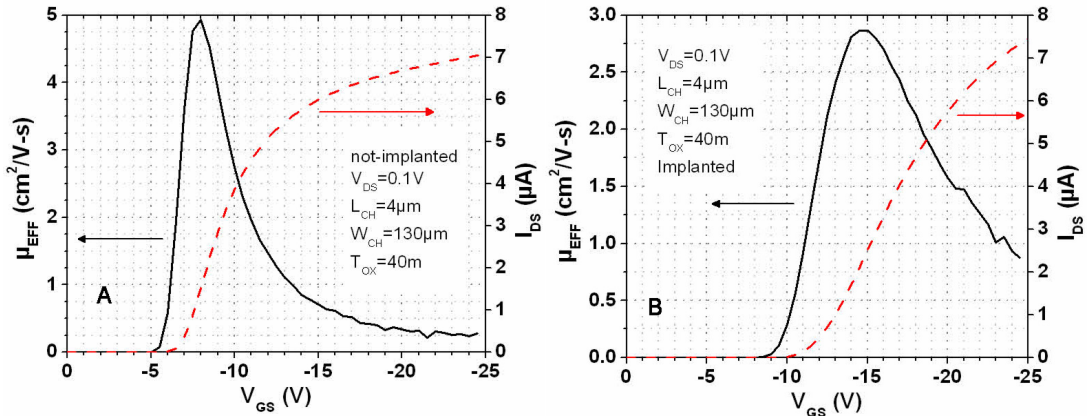

FIGURE 4.41 – Effective mobility in a PMOS of a ALS7 (a) and ALS8 (b)

The figure 4.42 shows the I-V characteristics of the lateral PMOS on ALS7 and ALS8. We can see that the saturation current is far higher on the non-implanted sample, its channel's doping concentration being lower, the inversion region is wider and the pinch-off is less effective on it.

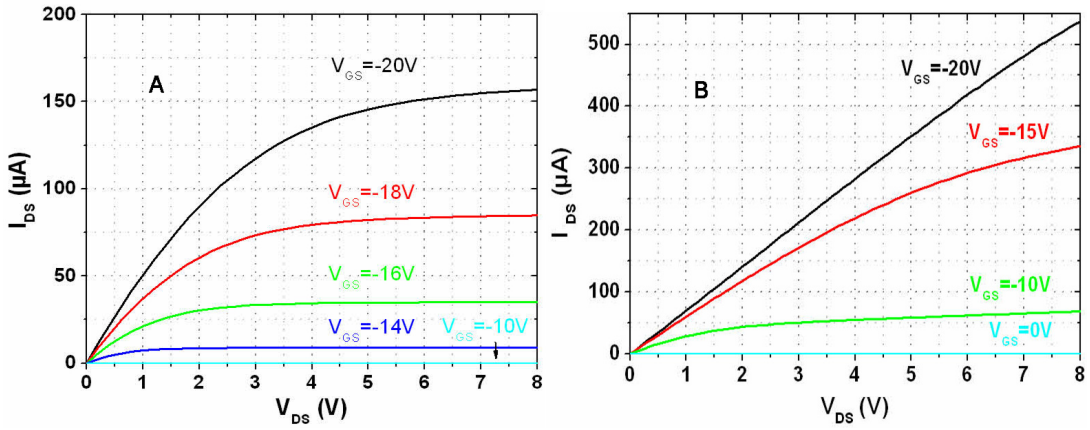

FIGURE 4.42 – I-V characteristics of the lateral PMOS on ALS7 (a) and on ALS8 (b) at different gate biases

Stress tests on these PMOS have shown that the devices without implantation in the channel are more stable. The PMOS devices show higher effective mobility than the NMOS on the same wafer, the interface charges have less deteriorating effect on the devices. For further investigation, this comparison should be performed with a lower channel doping concentration on the implanted samples, and a higher one for the non-implanted one. So that we compare devices with similar channels, minimize the damages induced by the implantation and reduce the channel's threshold voltage of the devices with implanted channel.

The PMOS structure has been rarely investigated although it is an essential part of the CMOS structure, so the integration of logic on SiC requires reliable PMOS and NMOS channels. Moreover, the realization of N-IGBT on SiC is limited by the unavailability of p-type substrates, however the combination of n-type substrates with p-type epitaxial layer allows fabricating very high voltage p-IGBT as shown by Cree in 2007 [92].

The PMOS were the only MOS devices operating on the samples and this is the reason why we first suspected the absence of the P-type epitaxial layer. The observations provided by the FIB and SEM, presented in the next part, permited us to confirm it.

4.6 Nanoscale observation using coupled focused ion beam (FIB) & scanning electron microscope (SEM)

The FIB permits to cut vertically through the cell structure of the devices and the SEM permits to see with accuracy down to 10nm. Moreover we can see the difference of doping type as a difference of contrast in the semiconductor, which allows us observing the vertical cell structure of the fabricated VMOS.

4.6.1 Vertical Double implanted MOS (VDMOS)

We first tried this technique on a VDMOS from ALS7 ; we can see pictures of the VDMOS cell structure captured with the SEM in figure 4.43.

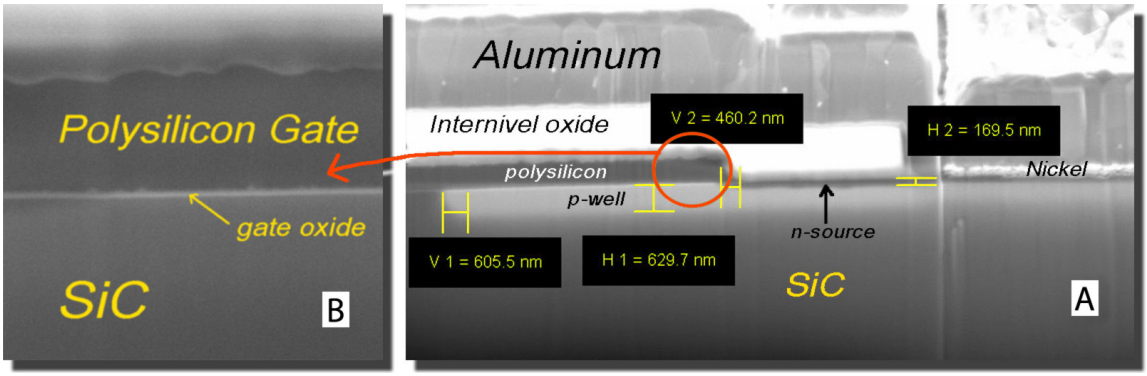

FIGURE 4.43 – SEM image of a vertical cut of a VDMOS cell on ALS7

In general, the SEM picture shows the insulating layers in white grey and the conductive ones in dark grey. On the right part of figure 4.43a, from the top to the bottom, we can distinguish the thick aluminium metallization, then the inter-level oxide, the gate's polysilicon and the SiC on the bottom half of the picture. The gate oxide is too thin to be visible at this scale ; we can see it more precisely on figure 4.43b and we evaluated its thickness to be 23nm.

On the right side of figure 4.43a, we can infer a white area in the SiC. The p-type SiC having a different interaction than the n-type SiC with the electrons, one can differentiate them with the difference of contrast on the SEM picture. Here, we can distinguish the p-well implantation as a grey area at the surface of the SiC. The implantation concentration cannot be evaluated, but we can appreciate the bi-dimensional distribution of the impurities.

We note that the lateral straggling is important (605nm), which is comparable to the p-well depth (630nm). Diffusion of the aluminium impurities in SiC is inexistent at temperatures lower than 1700°C ; this lateral repartition of the impurities is due to the

lateral dispersion of the impurities during the implantation and to the sloped sides on the implantation mask's windows.

On the right side of figure 4.43a, the dark line between the p-well and the source contact is the source implantation ; it is 170nm deep as predicted by the simulation. It overlaps the polysilicon layer by 460nm instead of 1μm. The distance between the n+ implantation and the JFET area defines the channel length that is 5μm long (without the lateral straggling). It corresponds to the dimension designed, so the difference of overlapping comes from a lateral etching of the polysilicon layer by 500nm.

4.6.2 VIEMOS

We performed a similar observation on a VIEMOS structure from ALS8. The SEM pictures (see figure 4.44) show that the 300nm p-type epitaxial layer and the p-well are not present in all the studied samples. We can see only the p^+ implantation in the middle of the source contact. This observation confirms the result of the SIMS analysis on ALS8.

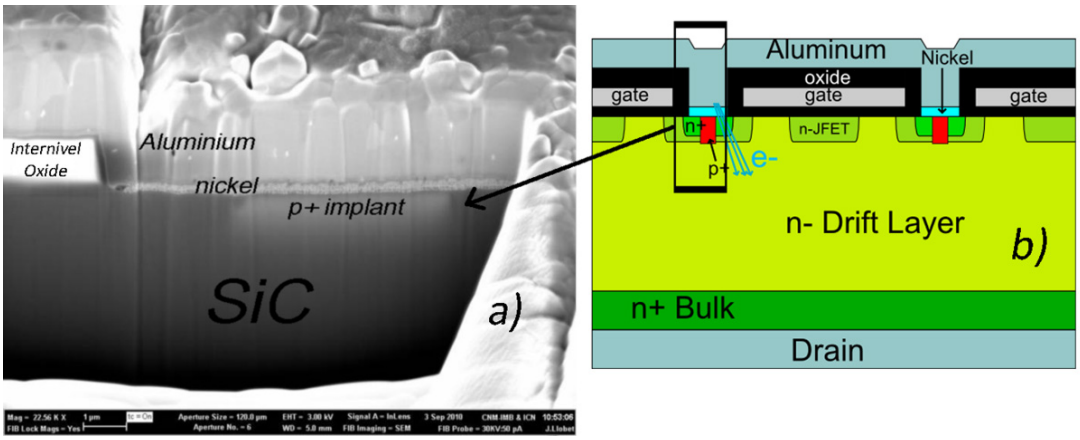

FIGURE 4.44 – FIB cut on VIEMOS structure on ALS8 (a) and schematized structure (b) created without the p-well and p-type epitaxial layer

A layer of SiC, where the JTE and p-well were implanted, must have been removed during the in-situ cleaning in H_2 of the wafer before epitaxial growth, and then the epitaxial layer was not doped with expected type. Their absence destroys completely the VIEMOS devices function and explains the vertical ohmic leakage current between the drain and the source as schematized in figure 4.44b.

4.7 Conclusions

The power MOSFET technology is a complex process with a large number (more than 80) of fabrication steps. In SiC it is even more complex due to the low diffusion coefficients and activation rates of the impurities. Starting from our existing technology, we have identified the new issues in the fabrication (over-etching of contact) as well as in the design (p-well doping) of the SiC VDMOS and tested successfully new solutions for the known issues (Gate oxide) and new issues (wet etching for the contact opening, new p-well profile) we typically faced with MOS devices.

We have proposed and evaluated three different technologies with improved process steps. The two key aspects of power devices, the current capability and the high voltage capability have been assessed. Regarding voltage capability, we obtained devices with breakdown voltages higher than 4kV using a JTE with guard rings periphery protection.

Regarding current capability, we have shown that we can cope with the low mobility in the channel by increasing its integration degree and reducing its length with self-alignment technique. We have analysed the design geometry showing the potential, as for Si devices, of the hexagonal cells design.

All these progresses have permitted to fabricate functional VDMOS of large area (up to 14mm^2) with complex design. Further optimization of the p-well implantation profile and reduction of the cell size will permit to produce state of the art SiC VDMOS. We have also successfully integrated temperature and current sensors in our VDMOS transistors. The forward and reverse characteristics are not affected (except regarding the area consumed by the sensor) by the presence of the sensor. The current sensor accuracy is maintained at high operation temperature. Our novel VIEMOS design was tested but problems during the re-epitaxy growth process did not allowed checking the benefits of this novel concept predicted by the modelling work.

General Conclusions

This work allowed us investigating many aspects of SiC power devices conception and fabrication. Our main objectives were the realization of high voltage VMOS.

We first studied their termination and active area via modeling. Thus, we could assess precisely the capability of different planar terminations, optimized their design and created an innovative termination by the combination of assisting guard rings with the JTE rings termination. Compared to commonly used JTE, this termination has shown higher breakdown capability and tolerance to the JTE dose, without increasing the complexity of its fabrication.

We also explored and modeled a new VMOS structure ; the VIEMOS. Although its fabrication process failed, it allowed acquiring a deeper insight of the SiC VMOS' peculiarities, which was useful during the VDMOS design and fabrication. We believe that this concept should improve the state of the art but more technological work, especially on the epi re-growth must be done.

The optimized terminations have proven their efficiency on the new design of large (4mm2) Schottky and JBS diodes that we fabricated with the tungsten as Schottky metal for the anode. They have shown high reverse capability up to 9kV, depending on the drift layer thickness used as starting material. Comparison of the static devices' characteristics when reverse and forward biased show that their quality is highly dependent on the epilayer's defects.

We have also characterized the switching behaviour and surge current capability of the Schottky and JBS devices for both 1.5kV and 6kV voltage ranges ; the JBS diodes have shown minimal temperature dependency of the reverse recovery charge up to 200°C, far superior surge current capability and lower leakage current compared to the SBD devices. So the tungsten-SiC JBS diode combines successfully the fast recovery of the SBD with the surge current and reverse capability of the PiN diode.

On 9kV JBS, devices with innovative hexagonal cells have been tested and we have seen their positive influence on the forward characteristics of the devices without losses of reverse capability. This design seems more efficient than typically used striped layout.

Nowadays, the most important aspect of the Silicon Carbide semiconductor investigation concerns the design of power switches ; our objective was to fabricate a high voltage SiC power VMOS. Three different versions of VMOS were implemented during this work, which allowed improving the fabrication process by identifying and solve several issues.

The major issue we need to overcome results from the p-well formation by implantation ; our VDMOS presents a channel concentration too high, which reduces the channel

mobility and increases the threshold voltage of the device. Further optimization of the p-well implantation profile is required to obtain state-of-the-art devices.

From a design point of view, we optimized the device's structure and design, and obtained device with active area up to $14mm^2$. We also fabricated functional VDMOS with integrated temperature and current sensors, which will allow monitoring and studying the devices during their lifecycle.

Further amelioration of our current technology will provide large area VDMOS capable of handling over ten amps and several thousand volts. Reliability and dynamic behaviour of the devices will then have to be investigated thoroughly to assess the SiC-VDMOS limits. Pushing the SiC-VMOS limits will pass by the trench structure to increase its forward capability.

Reduction of the generated defect during the JBS implantation will be studied. Amelioration of the SiC wafers quality will permit to increase the devices' yield and lifetime.

With the Integration of our next generation of SiC unipolar devices in a prototype of inverter capable to operate at high temperature and high frequencies, we will be able to further study the devices in a more realistic environment. This will provide us elements to enhance and to adapt the devices toward their application.

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Annexe A. Diodes Layouts

1. CNM_SIC026

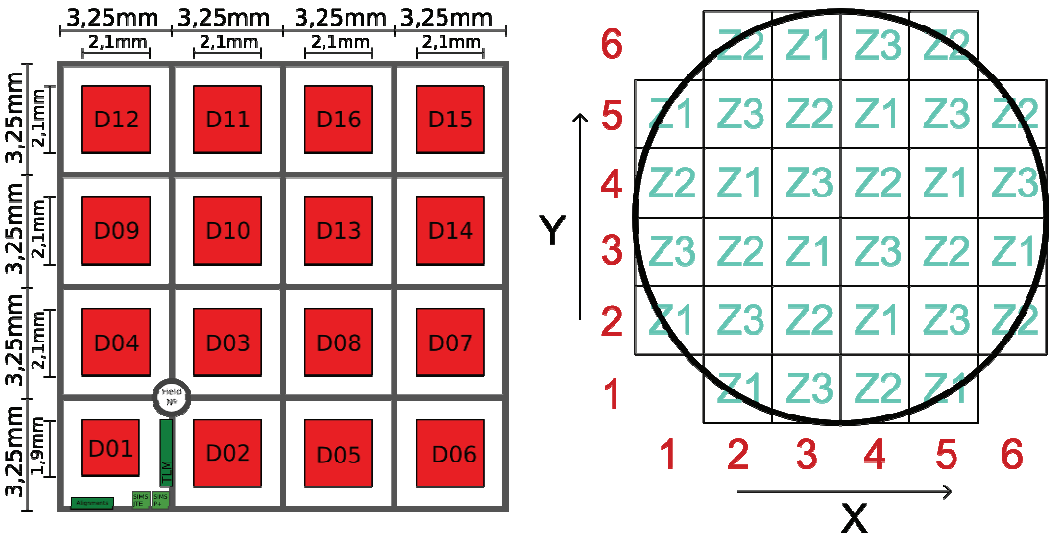


Figure 1 – (a) Basic field with 16 different diodes and (b) fields variation distribution used in mask set CNM_SIC026

1.1. Geometrical parameters of the designed diodes

On the 1st version of the mask layout, we implemented 15 Schottky diodes and 1 JBS on the basic field.

- In the Schottky diodes we varied the termination types; we implemented single JTE of 220µm length, JTE with JTE rings, JTE with assisting P^+ guard rings, and JTE with both types of rings, as developed and modeled in the previous chapter.
- Three different basic field versions (Z1, Z2 and Z3) also permit to vary the JBS diodes design (Diode D01). This distribution allows testing JBS with different Schottky/PiN proportions (parameters L_P and Ls).

A summary of the different design implemented is shown in Table 1. As a consequence, on a 3" wafer, 16 diodes are JBS, 48 are Schottky diodes with different termination designs, and 192 are identical Schottky diodes.

Table 1 - Diodes design with first mask layout set

Diode	Area	Type	JTE Length	Number of AGR	Number of JTE Rings
D01	Z1	JBS 3n/4p	220	3	5
	Z2	JBS 3n/6p	220	3	5
	Z3	JBS 3n/8p	220	3	5
D02	Z1	Schottky	220	3	0
	Z2		220	0	0
	Z3		220	0	0
D03	Z1		220	3	5
	Z2		220	0	5
	Z3		270	3	5
D04	Z1		220	3	5
	Z2		270	3	5
	Z3		170	3	5
D05 to D16	All		220	3	5

1.2. Second version of the JBS mask

In the first version of the mask set, all the JBS have Stripped geometry (Figure 2b). A second version of the mask set was created where the JTE and PPLUS levels were modified in order to obtain only one type of Schottky diodes, as well as a novel JBS design with hexagonal geometry (Figure 2c). In this case, on a 3" wafer we obtain 16 JBS diodes and 240 Schottky diodes with field stopper. A list of the device designs implemented in the second version of the mask set is shown in Table 2.

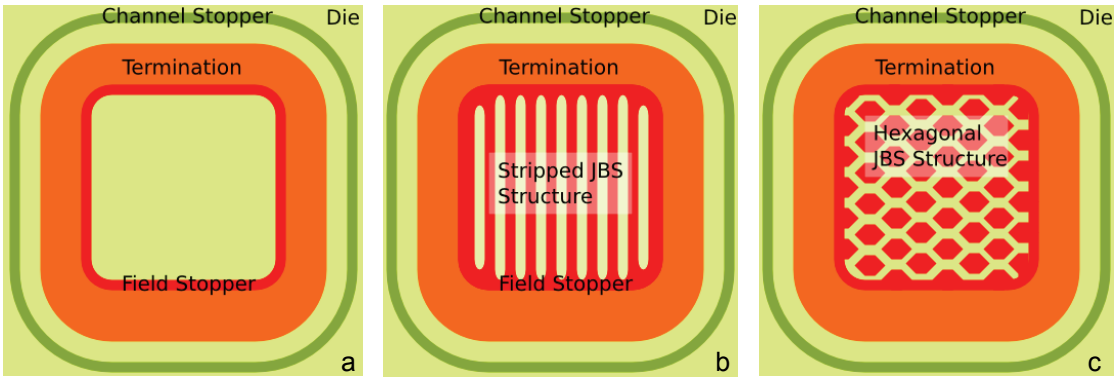


Figure 2 – Schematic top view of (a) a Schottky with field stop, (b) a stripped JBS and (c) an hexagonal JBS implemented in the various versions of CNM_SIC026 mask set

Table 2 - Diodes design parameters with layout level JTE-v2 and PPLUS-v2 instead of JTE and PPLUS of the first layout set

Diode	Area	Type	JTE Length	Number of AGR	Number of JTE Rings
D01	1	Strip JBS 3n/4p	220	3	5
	2	Strip JBS 3n/6p	220	3	5
	3	Hex JBS 4n/4p	220	3	5
D02 to D16	All	Schottky	220	3	5

1.3. Third version of the mask

A third version of the PPLUS Level of the mask set was created to fabricate a majority of JBS diodes with different geometries on the entire wafer. With this level, called CNM_SIC026-JBS, dimensions of stripped design JBS were kept similar to the previous version; L_P=3μm and L_N=4/6/8μm. In addition, new P-well designs with hexagonal geometry were implemented, in order to reduce the proportion of P^+ implantation in the active area for a given L_N and L_P, so that the R_{on-sp} is decreased

for the same active area and blocking voltage. A hexagonal geometry of P-Well as small as L_P=3μm could be difficult to define with typical masking techniques used to implant Aluminium. Hence, we chose to use a safer L_P=4μm for the JBS with hexagonal P-well (D6, D7, D8, D16), except for D05 were we took the risk with a L_P=3μm. JBS diodes with higher number of assisting guard rings (8 AGR) in the termination have also been added in devices D14 and D16. A summary of the main design parameters for the 16 diodes is presented in Table 3.

Table 3 - Diodes design with the level JBS instead of PPLUS

Diode	Z	Type	N	P	Geometry	Number of AGR
D01	1	JBS	4	3	DIG	5
	2	JBS	6	3	DIG	5
	3	JBS	4	4	HEX	5
D02	1	JBS	4	3	DIG	5
	2	JBS	4	3	DIG	0
	3	JBS	4	3	DIG	0
D03	1	JBS	4	3	DIG	0
	2	JBS	4	3	DIG	0
	3	JBS	4	3	DIG	5
D04	*	JBS	4	3	DIG	5
D05	*	JBS	4	3	HEX	5
D06	*	JBS	4	4	HEX	5
D07	*	JBS	6	4	HEX	5
D08	*	JBS	8	4	HEX	5
D09	*	JBS	4	3	DIG	3
D10	*	JBS	4	3	DIG	4
D11	*	JBS	6	3	DIG	5
D12	*	JBS	8	3	DIG	5
D13	*	JBS	4	3	DIG	5
D14	*	JBS	4	3	DIG	8
D15	*	Schottky	-	-	-	5
D16	*	JBS	6	4	HEX	8

2. New mask set design

To obtained high voltage diodes, we designed a new mask set (CNM_SiC027). This layout was designed after the CNM_SIC026 shown in the previous paragraph, which had proven to be very convenient both for processing aspects and for a efficient characterization methodology. The same diode distribution layout as CNM_SiC026 (see Figure 1) was chosen as shown in Figure 3. The main differences rely on the diodes active (contact) area, smaller in this new mask, and on the termination area. This layout is designed for the 4kV-5A Schottky diodes. In this layout, only one field version was created, unlike in CNM_SiC026.

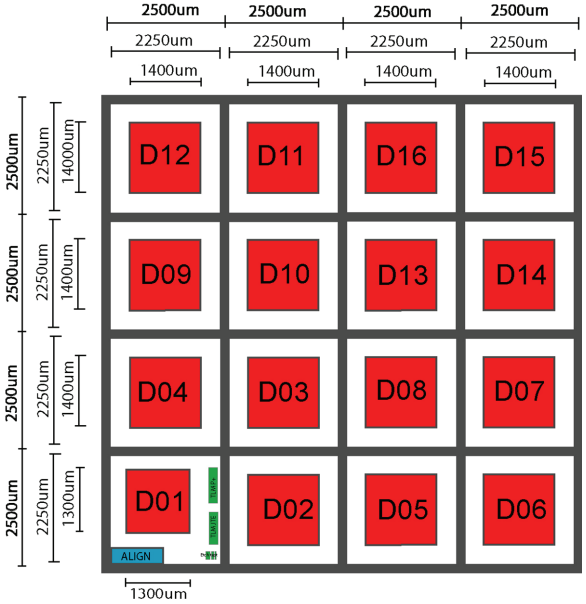


Figure 3 – basic layout used in CNM_SiC027

The innovative termination tested here is composed of a JTE with JTE rings and assisting guard rings (see figure 23 of chapter 2). The distribution of the termination design and parameters is summarized in Table 4. We selected designs with 3 AGR or without AGR and with 0, 3 and 5 JTE Rings. Diodes D03 and D04 have no AGR so the JTE size was reduced to keep the same JTE length after the field stopper compared to the JTE length after the last AGR on other diodes.

Table 4 - Terminations on CNM_SIC027

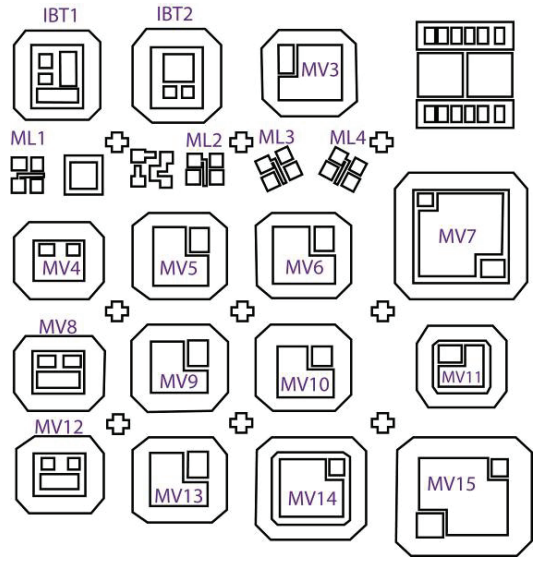
	D01	D02	D03	D04	D05-D16
JTE Length (µm)	190	190	170	170	190
JTE Rings	0	5	5	3	3
AGR	3	3	0	0	3

In addition, in this mask set, one mask level is specially used to implement JBS diodes on the full wafer. If this level is not used in the process, only Schottky diodes with the different termination design parameters are obtained.

Annexe B. VMOS Layouts

1. ESCAPEE

The layout used for the ESCAPEE VDMOS, shown in Figure 1, is composed of a unique field. The field includes 3 mono-cell VDMOS, 10 multi-cell VDMOS, 4 lateral DMOS, 2 IBTs and 6 test structures. The multi-cell VDMOS structure has been declined in various flavours, with different channel length, JFET area length and cell geometry.



MOSFET	L_{CH} (µm)	L_{JFET} (µm)	W_{CH} (µm)	A_A (mm^2)	Geometry
ML01	8	-	170	-	horizontal
ML02	8		170		vertical
ML03	8		170		45°
ML04	8		170		-45°
MV03	3	4	8468	0.23	Hex
MV05	3	4	5810	0.23	Strip
MV06	3	4	5810	0.23	Strip
MV07	3	4	31708	0.71	Hex
MV09	2	5	5810	0.23	Strip
MV10	3	4	5810	0.23	Strip
MV11	3	4	6564	0.19	HexStrip
MV13	2	5	5810	0.23	Strip
MV14	3	5	12942	0.41	Strip
MV15	3	5	21372	0.67	Strip

Figure 1 - ESCAPEE Layout for VDMOS fabrication

2. CNM_SiC25

The layout was designed with Cadence and the VMOS structures have been created entirely with SKILL routines in order to minimize manipulation errors during the design and give the possibility to change rapidly and precisely the design parameters of complex structures as vertical MOSFETs with hexagonal cells. This technique is time consuming during the conception of the script but it has revealed very effective when we changed some design parameters like channel length or guard rings distance.

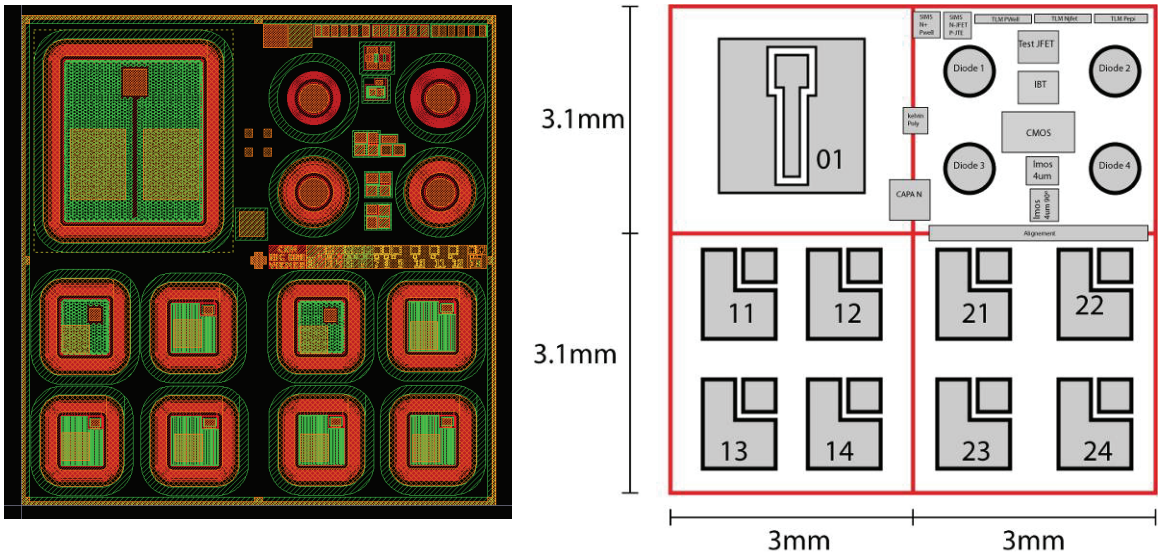


Figure 2 - VDMOS layout, screenshot of the layout on the left and schematic view on the right

This Layout is composed of 4 areas, one for a large multi-cell VMOS of 1.5x1.5mm^2, two for smaller multi-cell VMOS with different design parameters and one for test structures at the top right of the layout area. The design parameters of the different multi-cell VMOS of the layout are summarized in the Table 1.

Table 1 – MOSFETs design parameters for both process alternatives

VMOS	Ch. Geom.	VIEMOS				VDMOS			
		L_{CH} (um)	L_{JFET} (um)	L_{MAR} (um)	L_{DEP} (um)	L_{CH} (um)	L_{JFET} (um)	L_{OVER} (um)	Aa (mm^2)
01	Hex	2	5.5	2	3	5	4.5	1	
11	Hex	2	5.5	2	3	5	4.5	1	0.370
12	Strip	2	5.5	2	3	5	4.5	1	0.327
13	Strip	2	4	2	3	5	3	1	0.304
14	Strip	2	6.5	1	3	4	5.5	2	0.348
21	Hex	1	5.5	2	2	4	4.5	1	0.349
22	Strip	3	5.5	2	4	6	4.5	1	0.344
23	Strip	2	5.5	2	2	4	5.5	1	0.330
24	Strip	2	5.5	2	3	4	4.5	1	0.327

One basic design was chosen considering previous results and simulations and different variations of the design were created by changing one parameter at a time. The VMOS 02 has the basic design, with stripped cells, 2um long channel, 5.5um long JFET area, 2um margin (L_{MAR}) and 1um long overlap of the PWell under the JFET area. The design parameters changing from the basic design is coloured in green in the Table 1. All the terminations of the multi-cell VMOS are composed of a 200um long JTE with 12 AGR. The position of the AGR was optimized by simulation on a PiN diode with a 30um thick layer doped at $1.10^{15}cm^{-3}$ and a JTE with total dose of $1.10^{13}cm^{-2}$.

The four round structures in the top right quarter are PiN diodes with the same PiN area and different terminations. Two diodes have a guard rings (GR) termination of 8 (Diode 01) and 12 rings (Diode 02), and two diodes have JTE with assisting guard rings (AGR) terminations also 8 (Diode 03) and 12 rings (Diode 04). All the terminations where previously simulated on 2D PiN structure and showed reverse bias capability over 4kV. The VMOS have the same termination as Diode 04, as the active area of the PiN is smaller and less sensitive to reverse bias than the VMOS, they permit to verify the functionality of the VDMOS termination and try the GR termination.

3. CNM_SiC028

3.1. Layout Levels

The VDMOS layout is composed of 10 levels presented in the Table 2.

Table 2 - VDMOS layout levels

Level nb	NAME	Align 1	Align 2	Polarization
1	ALIGN			DK
2	JTE	ALIGN		DK
3	PWELL	ALIGN		DK
4	NPLUS & NPLUS-AA	ALIGN	PWELL	DK
5	ACTIVATION	ALIGN		DK
6	POLY	ALIGN		CL
7	CONT	ALIGN	POLY	DK
8	MET1	ALIGN	CONT	DK
9	MET2	ALIGN	ACTIVATION	CL
10	PASSIVATION	ALIGN		DK

Some levels are aligned on two other levels. For example the NPLUS level, which alignment precision with respect to the PWELL level is very important as the channel length uniformity depends on it.

3.2. Global Layout

As the main goal of this layout is to fabricate large VDMOS that will later be packaged, we decided to place the large VDMOS in a unique area and test structures are gathered in the same areas. The final layout was separated in 6 areas as show in Figure 3.

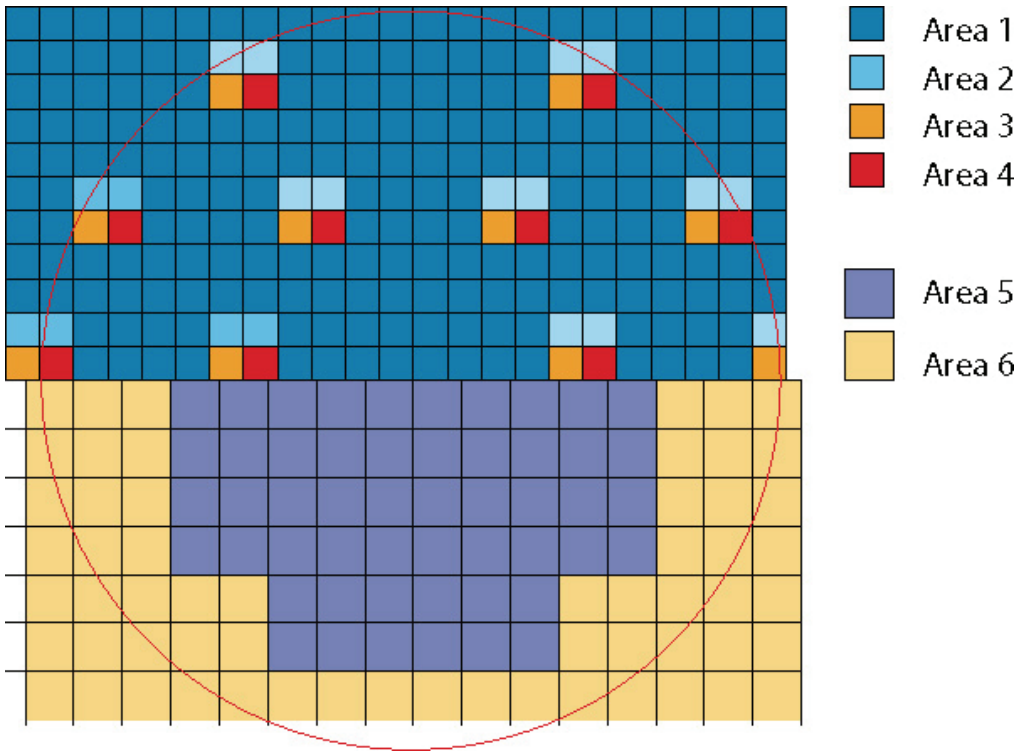


Figure 3 - Global layout scheme

Area 1, 2 and 5 hold one large VDMOS each and Area 3, 4 and 6 hold the area with various test structures. The wafer is divided in two parts; the bottom part is dedicated to the fabrication of the largest structures in Area 5 where VDMOS have an active area of 12.25mm^2. The border of the wafers presents a lot more defects than the centre, only small structures have chances of success there, so the area 6 placed on the periphery of the bottom part of the wafer is filled with small experimental VDMOS with sensors and test structures. The top part of the wafer is dedicated to the fabrication of VDMOS with an active area of 6.5mm^2 in the Area 1. The Areas 1 and 2 contain alignment pattern, test structures, very small vertical and lateral MOS, they are placed at different positions on the top part to provide a spatial analysis of the sample properties.

3.3. Areas

The VDMOS cell architecture and process steps are similar to the VDMOS fabricated previously. The first metallization (MET1) will no overlap the oxide of the MOS cell, as shown in Figure 4. The P+ used to contact the PWell is created with the same mask layout as the alignment layout (ALIGN), so the contact is etched before the implantation.

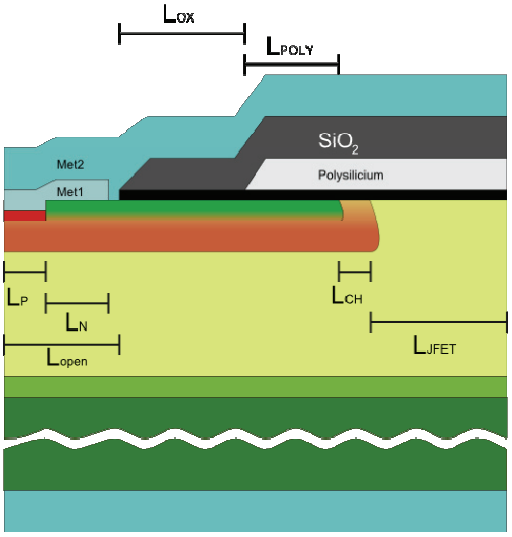
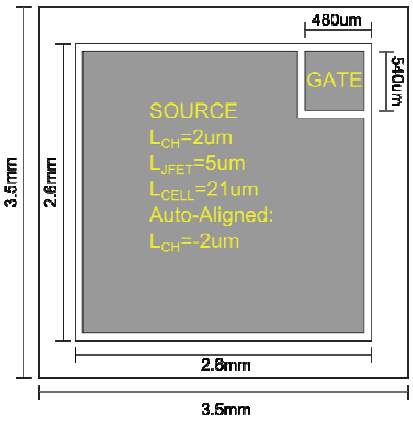


Figure 4 - Vertical cut of the VDMOS Cell

The Figure 4 shows the schematic view of a vertical cut in the VDMOS' cell obtained in this fabrication process, the different dimensions indicated here will be used to describe the different variations of the design.

3.3.1. Area 1

Area 1 die size is 3.5x3.5mm^2 and contains one VDMOS with an active area of 6.2mm^2. If the structure has on resistance of 20mOhm.cm^2, it would have a capability of 6A at V_{DS}=2V.



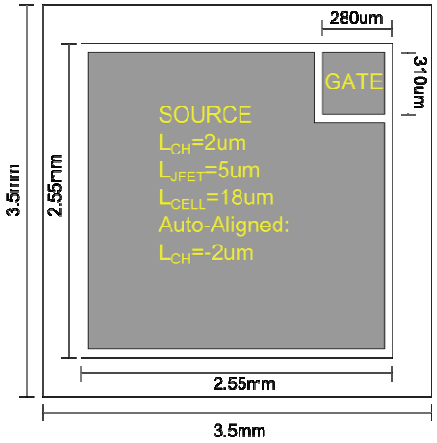
L_{CH}	2
L_{CH-AA}	-2
L_{JFET}	5
L_{POLY}	5
L_{OX}	4
L_N	2.5
L_P	2
L_{OPEN}	5
L_{CELL}	21
W_{CH} (cm)	42

Figure 5 – Area 1

The VDMOS contained by this Area is the standard structure chosen for this layout, with hexagonal cells, a channel length of 2um, a JFET length of 5um and an auto-aligned channel when one employ the adapted layout and process.

3.3.2. Area 2

This area is similar to the AREA 1, except for certain dimension of the MOSFET design. The unit cell size was reduced by 3 and the gate size occupies 3 times less space. The channel and JFET area length are similar, the optimization of the size of the cell have been applied via the reduction of different technological margin as the distance between the gate and the source metallization. This optimization has also been tested on smaller structures in this the area 4.

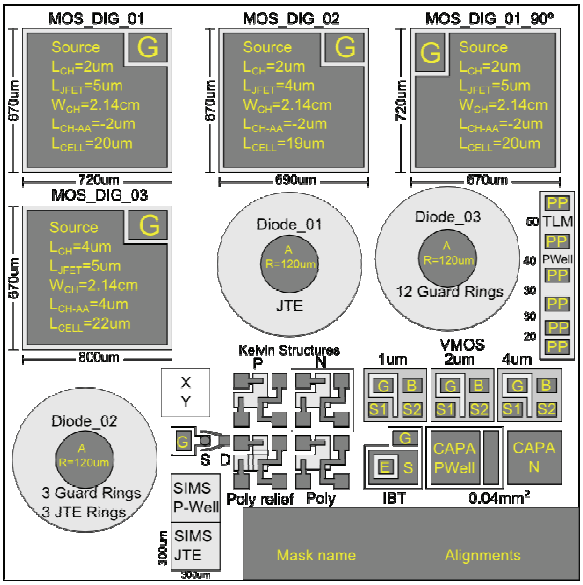


L_{CH}	2
L_{CH-AA}	-2
L_{JFET}	5
L_{POLY}	3
L_{OX}	3
L_N	2.5
L_P	2
L_{OPEN}	5
L_{CELL}	18
Gain/Cell	4 (20%)
W_{CH} (cm)	

Figure 6 – Area 2

3.3.3. Area 3

This area is dedicated to test structures, it contains 4 VDMOS with multiple stripped channels and different dimensions, 3 single channel VDMOS, 3 vertical diodes, 4 kelvin structures, and several other test structures. The diodes permit to compare different terminations; the simple JTE, Guard Rings and JTE Rings, their anode is form with the PWell and JTE implantation. The VDMOS with a single channel and different dimensions have very simple architecture; the gate is not overlapped by the source metallization and the simplified geometry of the channel permit to precisely evaluate the channel contribution to the different properties of the VDMOS. A small IBT and lateral n-IGBT are also included for trial. As physical test structure, there is also a TLM to extract the PWell resistance and PPLUS contact resistance and two SIMS areas; one for the PWell and one for the JTE.



	MOS_DIG_			
	01	02	03	04
L_{CH}	2	2	4	2
L_{CH-AA}	-2	-2	4	-2
L_{JFET}	5	4	5	5
L_{POLY}	3	3	3	3
L_{OX}	4	4	4	4
L_N	3.5	3.5	3.5	3.5
L_P	2	2	2	2
L_{OPEN}	6	6	6	6
Rotation	0°	0°	0°	90°
W_{CH} (cm)	2.14	2.14	2.14	2.14
A_A	0.45	0.43		0.45

Figure 7 – Schematic layout of Area 2

The four VDMOS with multiple channels are the only ones with stripped channel geometry. The hexagonal geometry are more difficult to fabricate and can reduce the reverse voltage capability; comparing them with these structures will be essential.

Table 3 - Termination of the different diodes

Diode	Act Radius	JTE Length	JTE Rings	NO P Rings
Diode_01	120µm	140µm	0	0
Diode_02	120µm	0	0	12
Diode_03	120µm	140µm	3	3

The different VDMOS have been terminated with a JTE, 3 Assisting Guard Rings and 3 JTE Rings, the diodes permit to test the superiority of this termination compared to the simple JTE, the third diode test the feasibility of a pure guard ring termination with 12 rings.

Table 4 - Single Channel VDMOS dimensions

Single channel VDMOS	W_{CH} (µm)	L_{CH} (µm)	L_{JFET} (µm)	L_{ch-AA} (µm)
VMOS_1um	2x110	1	5	-2
VMOS_2um	2x110	2	5	2
VMOS_4um	2x110	4	5	4

The Single channel VDMOS have the same channel and JFET area length as the multiple channel VDMOS in the layout. The auto-aligned channel is tested on the first specimen as the second will keep a 2um long channel so that the three different dimensions can be compared.

Table 5 - Structure trials

Structure	W_{CH} (µm)	L_{CH} (µm)	L_p (µm)	L_{DRIFT} (µm)	L_{JFET} (µm)
IBT	720	4	6		5
LIGBT	220	8		8.75	

The Table 5 shows the different parameters of the structures trials. The IBT has never been successfully fabricated on Silicon Carbide. The channel of previous trials was too resistive to trigger the bipolar conduction of the IBT, the channel length and L_P was reduce compared to previous designs so that the bipolar conduction is triggered earlier. The lateral IGBT was designed to stand up to 1kV.

3.3.4. Area 4

This area is dedicated to test structures and especially VDMOS with multiple hexagonal cells and lateral MOSFETs as shown in Figure 8.

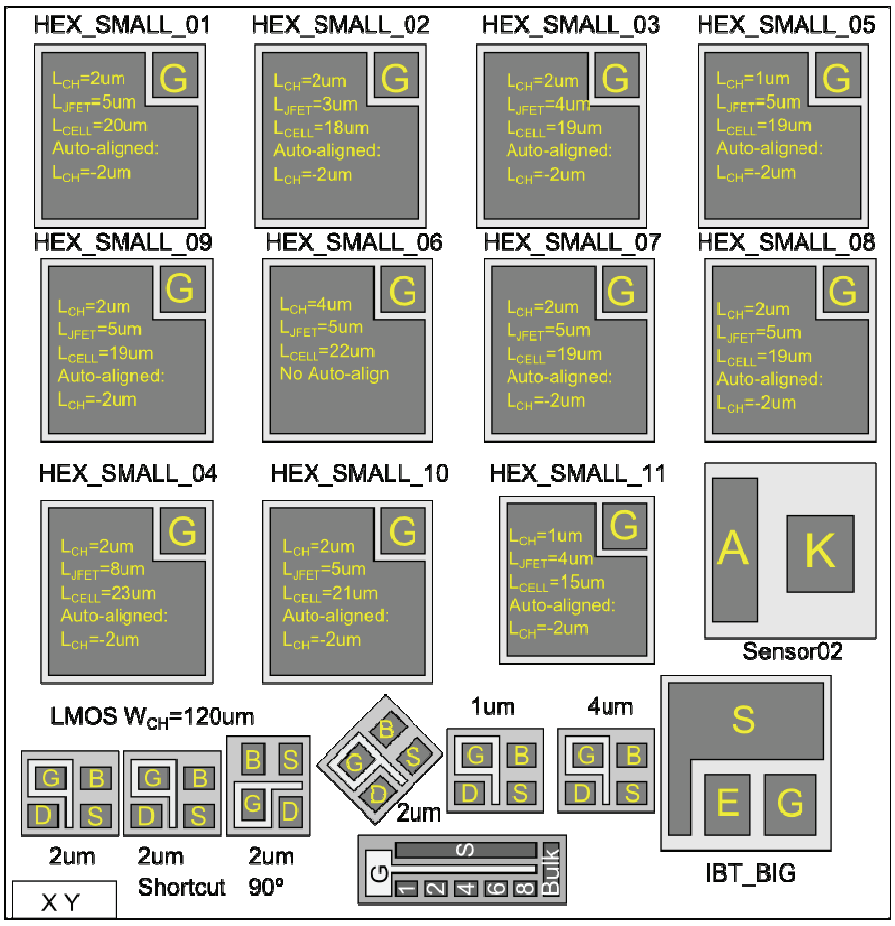


Figure 8 – Schematic Layout of Area 3

The 11 VDMOS designs permit to evaluate the influence of the different design parameters on the MOS properties. The channel length (L_{CH}) was varied in three sizes; 1, 2 and 4um and the JFET length (L_{JFET}) is varied in 4 sizes; 3, 4, 5 and 8um. Other parameters as the distance between the source opening and polysilicon of the gate (L_{OX}), the polysilicon size before the channel (L_{POLY}) and the contact length (L_P and L_N). All the variations are presented in Table 6, the majority of the structures assume only one parameter variation so that their respective influence on the structure is isolated.

Table 6 - Design parameters of the small VDMOS with hexagonal cells

	HEX_SMALL										
	01	**02**	**03**	**04**	**05**	**06**	**07**	**08**	**09**	**10**	**11**
L_{CH}	2	2	2	2	1	4	2	2	2	2	1
L_{CH-AA}	-2	-2	-2	-2	-2	4	-2	-2	-2	-2	-2
L_{JFET}	5	3	4	8	5	5	5	5	5	5	4
L_{POLY}	3	3	3	3	2	3	3	2	3	3	2
L_{OX}	4	4	4	4	4	4	3	4	4	4	3
L_N	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	2.5	4.5	2.5
L_P	2	2	2	2	2	2	2	2	2	2	2
L_{OPEN}	6	6	6	6	6	6	6	6	5	7	5
L_{CELL}	20	18	19	23	18	22	19	19	19	21	15
W_{CH} (cm)	1.23	1.23	1.23	1.23	1.15	1.43	1.18	1.18	1.18	1.34	0.93
A_A (mm^2)	0.26	0.213	0.232	0.34	0.213	0.309	0.232	0.232	0.232	0.286	0.148
R_{CN} (%)	6.5	8.1	7.2	5	8.1	5.4	7.2	7.2	4.5	8.6	7.2
R_{CH} (mm^{-1})	47.3	57.7	53	36.2	54	46.3	50.8	50.8	50.8	46.8	62.8

The parameters L_P, L_N, L_{OX} and L_{POLY} will not have an influence on the conduction in the devices, but their reduction permit to optimize the cell size and thus increase the density of channel in the MOSFET. If the design margins are too small, a misalignment on any level can produce short-circuit, the structure 11 presents much smaller margin than usual on all the parameters so that we can observe feasibility of such dimensions with our fabrication process. The cell length (L_{CELL}), active area (A_A), channel width (W_{CH}), N contact ratio (R_{CN}) and channel length ratio (R_{CH}) depends on the previous parameters. For hexagonal cells, R_{CN} and R_{CH} are calculated as shown in Equation X.

Equation 1 - Ratio of N-type contact and channel length compared to the active area of the MOSFET

$$R_{NC} = \frac{A_N}{A_{CELL}} \times 100 = \frac{(L_P + L_N)^2 - L_P{}^2}{L_{CELL}{}^2} \times 100$$

$$R_{CH} = \frac{W_{CH}}{A_A}$$

They will permit to distinguish which parameter has major influence on the forward characteristics of the devices.

The Lateral MOSFETs are situated in the bottom part; the structures have channel dimensions similar to the VDMOS in the layout; 1, 2 and 4um. The lateral MOSFET structure have large contact areas and does not have drift or JFET area so they do not present parasitic resistance due to them. Its channel properties are extracted easily. So the LMOS is essential to evaluate the channel quality and its contribution to the VDMOS resistance; the different LMOS structures in this area are summarized in the Table 7.

Table 7 - Lateral MOSFETs parameters

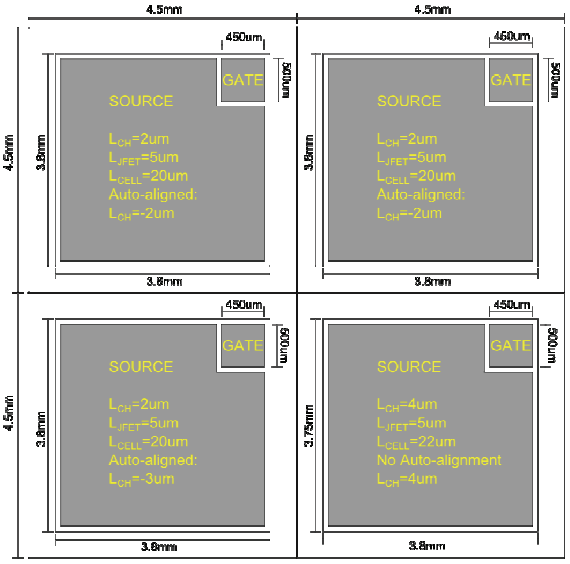
Single channel LDMOS	W_{ch} (µm)	L_{ch} (µm)	L_{jfet} (µm)	AA	L_{ch} AA (µm)
LMOS 2um	120	2	0	No	2
LMOS 2um Shortcut	120	2	0	Yes	1
LMOS 2um 90º	120	2	0	No	2
LMOS 2um 45º	120	2	0	No	2
LMOS 1um	120	1	0	No	2
LMOS 4um	120	4	0	No	2
LMOS Grid	90	1/2/4/6/8	0	No	1/2/4/6/8

As the crystal orientation can have influence on the channel mobility and implantation straggling, lateral MOSFETs with 2um long channel were placed with different orientations.

The LMOS_GRID, situated at the bottom of the layout, is a structure composed of several lateral channels controlled by a common gate and source, and a separate drain; it permits to economize a lot of space.

3.3.5. Area 5

This Area is dedicated to the fabrication of the largest VDMOS of the layout. Their active area totalizes 14.2mm^2. With a specific on resistance of 20mOhm.cm^2, they would be capable to handle 14.2A at 2V.



	01	02	03	04
L_{CH} (µm)	2	2	2	4
L_{CH-AA} (µm)	-2	-2	-3	4
L_{JFET} (µm)	5	5	5	5
L_{POLY} (µm)	3	3	3	3
L_{OX} (µm)	4	4	4	4
L_N (µm)	3.5	3.5	3.5	3.5
L_P (µm)	2	2	2	2
L_{OPEN} (µm)	6	6	6	6
W_{CH} (cm)	105	105	105	95.5
A_A (mm^2)	14.2	14.2	14.2	14.0

Figure 9 - Schematic View and Design parameter of VDMOS in Area 5

All the devices have hexagonal unit cells. Three of the devices are similar, with a 2um long channel, 5um long JFET area and an auto-aligned channel when the appropriate layouts and processes are applied during the fabrication. The Fourth design has a longer channel (4um) which is not auto-aligned in any case. The design margins are standard on all designs, so the unit cell size is not optimized. The position of the different structures is presented in
Figure 9. The gate is large enough to solder a wire bonding with a diameter of 320um. Their termination is made of a JTE 110um long with three assisting guard rings and three JTE Rings.

3.3.6. Area 6

This Area is dedicated to VDMOS with integrated temperature and current sensors. This type of device on SiC has never been seen in the literature. Ultimately, evolution of power IGBTs and MOSFETs have seen their performance and reliability increase but also their functionality via the integration of sensors at the core of the chip. Those sensors permit to monitor the chips at their core and create better protection systems. Integration of sensor in the core the Silicon Carbide chips will also permit to monitor and protect precisely the chips. Moreover, the SiC chips are destined to work with high temperature and current density, the temperature sensor will permit to monitor the chip's temperature and use the chip at high current density with smaller margins on the maximum current density.
Two types of sensor have been tested here; the current sensor shown in Figure 10, is created via the isolation of several cells from the source, the current will be proportional to the number of cells connected to the sensor.

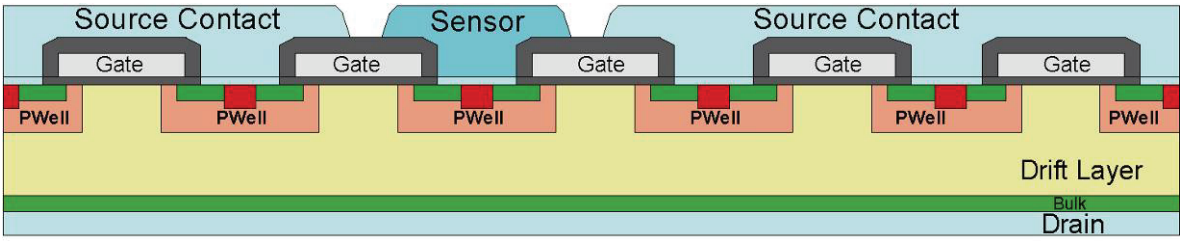


Figure 10 - Current Sensor

The Temperature sensor, shown in Figure 10, is directly fabricated in the silicon carbide, with a P type area isolated from the source, connected with two ohmic contacts. As the temperature increases, the aluminum activation percentage increases and the Al doped area become less resistive. So the resistance between the terminals of the sensor will be proportional to the temperature of the chip.

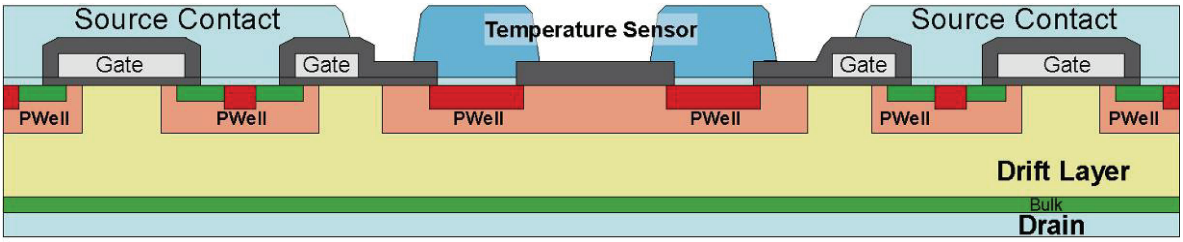


Figure 11 - Temperature Sensor

The current sensor is made of 19 cells connected together and isolated from the Source terminal. The temperature sensor has necessitated the suppression of 32 cells. The MOSFETs originally hold around 650 cells. The Figure 12 shows the disposition of the chips in the Area 6, one MOS has no sensor and the other 6 MOSFETs have one or two sensors. The MOS 1,2,5,6 and 7 have been designed with identical dimensions so that they can be compared. If the gate oxide thickness is not uniform, it induces a difference of conductivity at different position of the chip,

so the current sensor position would have an influence on its forward characteristics. On VDMOS_SENS_05, two current sensors have been created to observe if the sensor position on the active area has an influence on its properties.
Concerning the reverse capability of the chips with sensor; the current sensor formation does not imply the modification of the internal structure of the MOSFET at the semiconductor level.

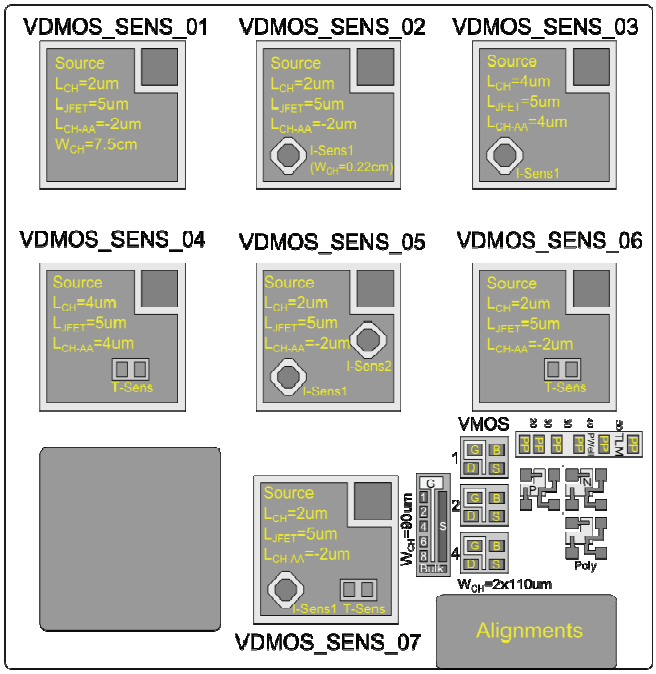


Figure 12 – Schematic layout of Area 6

	VDMOS_SENS_01	VDMOS_SENS_02	VDMOS_SENS_03	VDMOS_SENS_04	VDMOS_SENS_05	VDMOS_SENS_06	VDMOS_SENS_07
L_{CH}	2	2	4	4	2	2	2
L_{CH-AA}	-2	-2	4	4	-2	-2	-2
L_{JFET}	5	5	5	5	5	5	5
L_N	3.5	3.5	3.5	3.5	3.5	3.5	3.5
L_P	2	2	2	2	2	2	2
L_{POLY}	3	3	3	3	3	3	3
N_{SENS-I}	0	1	1	0	2	0	1
N_{SENS-T}	0	0	0	1	0	1	1
W_{CH} (cm)	7.13	6.96	7.74	7.59	6.78	6.68	6.42
A_A (mm^2)	1.15	1.12	1.16	1.1	1.1	1.1	1.08
R_W	-	35	34.5	-	34	-	33.5
R_A	-	45.5	36.5	-	42	-	41

Table 8 –Design Parameters of the VDMOS with Sensors

When reverse biased, the equipotential lines are completely handled by the structure inside the SiC crystal, so, if the current sensor is biased at the same level as the source, it will not affect the reverse capability of the chip. The temperature sensor is made of the same PWell implantation used to create the internal diode of the MOSFET. Moreover, the distance between the sensor and the surrounding cells was designed smaller than the JFET area length of the device so that no field crowding occurs around the sensor. The temperature sensor is more protected than any cell of the structure when biased at the same level as the source.

In Table 8, the proportionality coefficient between the channel length and the area of the current sensor and the actual source of the MOSFETs are noted as R_W and R_A respectively. The channel length of the source and it area are indicated as W_{CH} and A.

Table 9 - Single channel VDMOS in Area 6

Single channel VDMOS	W_{CH}	L_{CH}	L_{JFET}	L_{CH-AA}
VMOS1um	220um	1um	5um	-2um
VMOS2um	220um	2um	5um	2um
VMOS3um	220um	4um	5um	4um

Lateral and vertical MOSFETs with a single channel have been included in this area so that the channel quality could also be evaluated on the bottom part of the wafer. The lateral MOSFETs are also contained in the LMOS_GRID structure and the VMOS are summarized in the Table 9.

The rest of the structures are TLM and Kelvin structures used to evaluate the contact and layer resistances.