



Design for reliability applied to RF-MEMS devices and circuits issued from different TRL environments

Nuria Torres-Matabosch

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Núria TORRES MATABOSCH

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Directeur(s) de Thèse :

Jean Louis CAZAUX - Directeur

Fabio COCCETTI - Co-directeur

Jury :

Thierry CAMPS - Examineur

Philippe FERRARI - Examineur

Lluís PRADELL CARA - Rapporteur

Pierre BLONDY - Rapporteur

Mehmet KAYNAK - Invité

Frédéric COURTADE - Invité

Béatrice ESPAÑA - Invitée

Christophe POULAIN - Invité

Abstract

The first RF-MEMS devices were presented about 30 years ago and widely developed during early 90's. Owing to their superior performance in terms of RF performance, power consumption and cost in comparison with existent technologies (CMOS, PIN...), RF-MEMS was a very promising technology. Reliability issues started to become a serious burden in the early 2000's and actual roadblock toward commercialization. From the beginning very deep studies have been done in order to understand the different physics of failure occurring during device lifetime. The main reliability problems were found out to be dielectric charging, contact degradation and fatigue and stress control in the movable membranes.

The reliability solutions proposed in this work are related with the design and the process steps modification (Design for Reliability). The processes have been classified using its TRL (Technology Readiness Level) which is indentified by means of a deep study of each process. Roughly, three different regions have been identified: low TRL (from 1 to 3), medium TRL (from 4 to 6) and high TRL (from 7 to 9). The relationships between adaptability, process flexibility, complexity, failure mechanisms and on-wafer dispersion have been established determining the suitable Design for Reliability strategy to follow.

In particular, for LAAS-CNRS process (low TRL) the addition of a metal layer over the movable part is proposed in order to reduce the DOWN capacitance dispersion and to increase its stiffness of the cantilever. For resistive switches the proposed solution is the optimization of an annealing step in order to reduce the deflection due to initial stress which prevents the dimples to contact the transmission line. Both solutions were adopted because the in-wafer and wafer to wafer dispersion was too big.

For medium TRL environment (CEA-Leti) the monitoring of the contact resistance was studied under different RF power through the contact. Preliminary results were shown that infer that the lower the number of actuations needed for a stable contact (N_{AC}), the higher the RF power through the contact (P_{RF}). These results were perturbed by the carbon contamination of the contact due to the non-hermetic package. No design for reliability can be applied without the total comprehension of the failure mechanism.

For IHP process (high TRL), the fabrication process dispersion origin was identified. The critical parameter to track is the UP and DOWN state capacitance responsible of the RF performance deviation in the initial state. The long-term reliability tests have demonstrated that the failure mechanism is mechanical fatigue. However, by defining a reliability criteria in pristine devices ($V_{POUT} > 36$ and $V_{PIN} - V_{POUT} \leq 1$) to screen the wafer, the device can afford up to 67h of continuous DC stress in harsh environments (22° and 45% humidity). The methodology proposed in this thesis in order to screen the wafer is by measuring the distance

between membrane and electrode or line without actuating the switch. This technique is non-intrusive and can be implemented in mass-production by defining cells over the wafer (already done by IHP) and testing one device of each cell.

For all three environments more complex RF-MEMS based circuits have been designed and characterized. Different routing circuits with capacitive and resistive switches are shown and a novel absorptive switch is designed using the advantages of a co-integrated MEMS-CMOS process (IHP). These results demonstrate the importance of the adaptability of the process.

The common tool used in all the process to study the RF performance versus time is the lumped-element based equivalent circuit. The models are based on measurements over the wafer in order to track the fabrication process dispersion and to identify the component of the model which affects more to the RF performance (sensitivity analysis). With this method, it has been possible to compute the effect of the roughness of contact dielectric in capacitive MEMS (LAAS-CNRS devices), the contact resistance of resistive switches (CEA-Leti) and the UP/DOWN capacitance dispersion in standard CMOS-MEMS process (IHP). Moreover, in IHP technology the pull-in/out voltage has been identified as the relevant parameter in order to ensure reliability under industrial specifications.

Acknowledgements

I can still remember the day I step into the Telecommunication Engineering School (ETSETB) in Barcelona. The dean of the faculty announced that we were supposed to be the leaders of the society and that we will rock the world. At that time, I thought he was just trying to encourage us by increasing our self esteem but, some years later I got the idea. If you want to really dominate the world you need not only to understand the environment in which you are moving, but also to design the weapons you need to use. Leaving the existence understanding to high-level people, I decided to focalize on the second need by investigating incognito in the research world.

Everything started few years ago, in 2007, when RF-MEMS show up in my career. I was just looking for a grant in my University in order to snoop around the research world and Lluís PRADELL (RF&MW group in TSC-UPC) introduced me my dear allies, also known as RF-MEMS. I would have never imagined that what started with some slides and tutorials for teaching support ended up with such a (good?) thesis dissertation. With his help and the collaboration of Marco Antonio LLAMAS (PhD student at that time) I started to understand how such a strange device could work.

After a couple of years, Lluís sent me to Toulouse where I met Fabio COCCETTI (NOVAMEMS LAAS-CNRS) who supervised my Master Thesis and afterwards introduced me Jean-Louis CAZAUX (Thales Alenia Space) becoming both of them my thesis supervisors. The participation of this *binôme* in my thesis has been capital not only from a technical point of view but also, because they have transmitted me their passion for the research world and their particular way of finding the positive part of everything (even if sometimes it was really hard!). Even if Jean Louis was sometimes astonished that Fabio and me could communicate (and also understand!) each other in French, the very good complicity between the all three has been the key issue towards a *très honorable* outcome. I wish that this very good feeling have been reciprocal and that I will not be the first and the last doctor that is born from this duo.

When I arrive in LAAS I integrate MINC group. I started the PhD adventure together with Dr. Dina, Dr. Mihai and Dr. Mariano with whom I spent really nice moments next to tiramisus, Egyptian food and waiting for the Rumanian specialties. Dr. George has been a very nice support for his particular view of the research and French people while having coffees. Every year new students arrived (Celine, Hong/Patricia, Olivier, Ayoub, Anya, Giancarlo...) making MINC the group with more nationalities in LAAS. Others like Heba, Ali, Jason, Vincent... left but they also contribute to my thesis and I do not want to forget them. I also thank the I2C team (Alex and Tonio) who suffered my characterization campaigns in LAAS and I wish that from now on they will be really relaxed.

After some months in LAAS I met Beatrice ESPAÑA (Thales Alenia Space) with whom I had the pleasure to work with and who has had the patience to assist ALL the monthly meetings with Jean-Louis and Fabio providing his valuable point of view. May be, the Catalan origins have played a role, who knows... In addition, I spent some weeks in Thales Alenia Space facilities where she has assisted me with the measurement setup and also has made me feel as one more in the Hyper frequency Advanced Studies group and LMMIC team (which I want to acknowledge too). The lunches in TAS cafeteria and the coffees in the coffee machine with all of them made the thesis writing stage really fruitful and efficient.

Another interesting experience was working with Mehmet KAYNAK (IHP). His self confidence that RF-MEMS could become a real commercial product has helped me to belief that what I was doing was relevant. We started with (short?) skype meetings, but we ended up with an internship in Frankfurt (Oder) this last summer. This collaboration provided me three important points: 1) technical experiences: with the Technology/Process integration team and with Cadence environment, 2) geography skills: there are two cities called Frankfurt (Main and Oder) in Germany, and 3) new language skills: “Cheers” is “Nasdrovia” in polish, so you can live in Poland while working in Germany. I want to thank all the people that contribute to the exit of this mission (Jana, Folk, Mauricio, René, Matthias, Christian) making this small town in the middle of nowhere a place to come back.

All these adventures finished on 14th January 2013 with the defense (it was also the 2nd anniversary of the Tunisian Revolution but this is another story...). I want to thank again all the members of the jury: Lluís PRADELL and Pierre BLONDY (XLIM) for the reports and the critical point of view, Philippe FERRARI and Thierry CAMPS for accepting to be in the committee and Frederic COURTADE (CNES), Beatrice ESPAÑA, Mehmet KAYNAK and Christophe POULAIN (CEA-Leti) for accepting the invitation. I do not want to forget Bruno REIG (CEA-Leti) who could not assist to the defense but participate also in the work. The discussions during and after the defense have been very interesting. I have to say that I enjoyed myself a lot feeling very comfortable and lucky during my presentation to have all these people in my jury. Thank you again for your efforts and time and for making the defense possible.

During these years I have discovered that RF-MEMS devices are not the only weapon I can use to dominate the world. In fact, I have discovered that my smile can also be a very powerful tool (thank you Roger for your observation! I have never realized this!). This smile has been possible thank to (my father investment☺) and to all my friends over the globe, especially to:

Sofiene and Franck for these *soirées* that started with *on va boire un coup* and ended... well, you know... *Insha'Allah* we will go on with these traditions. I thank also them for the strong support during all this time in *LAAS-Vegas*; you are the best, really!

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fins demà! Les pauses de cafè amb vosaltres i els crits de Ahhh! m'han donat la força per passar les tardes. Sense oblidar els sopars!!

Part of the smile is also due to my family who I want to thank for their unconditional support during these 4 years. Also, to do the effort to come to my thesis defense dealing with all the associated troubles and making this day unforgettable. I have had my PhD, but they have had the “best family” degree: thanks to my *iaia* whom, as Einstein adviced, I could finally explain the reliability problems of RF-MEMS which means that I understood the problem (even if she doesn't). *Avi, per mi també hi eres aquest dia! Tieta, sort dels teus tupperes de croquetes, les teves coques... ets la millor! Tiet, gràcies per ensenyar-me a soldar, Gabi, Jaume i Albert gràcies per vigilar-los a tots, que heu tingut feina! Rosa Mari, gràcies pel teus petons i crits! Finally, Angel, Montse, Cris who I dedicate this thesis... gràcies per les vostres abraçades de força i ànims, aquesta tesi és també vostra.*

I have now the tools, it's time to act!

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To Angel, Montse and Cristina

Introduction

The first RF-MEMS devices were presented about 30 years ago [1] and widely developed during early 90's. Owing to their superior performance in terms of RF, power consumption and cost in comparison with existent technologies (CMOS, PIN...), RF-MEMS was a very promising technology. Reliability issues started to become a serious burden in the early 2000's [2] and an actual roadblock toward commercialization. From the beginning very deep studies have been done in order to understand the different physics of failure occurring during device lifetime. The main reliability problems were found out to be dielectric charging, contact degradation and plastic/elastic deformation in the movable membranes.

The results of the deep investigation in failure mechanisms of RF-MEMS have resulted in the development of materials tolerant to dielectric charging or contact degradation. Despite all these efforts, RF-MEMS are still struggling to reach the mass-market since these failure mechanisms can only be minimized and not avoided even in optimized materials. At this moment, the research community is facing the problem from another perspective: if you cannot solve the problem, remove its cause. This approach takes into account the failure mechanisms and its effects at the very beginning of the device conception. This approach is denoted as "Design for Reliability".

This thesis is intended to deal with reliability of RF-MEMS devices (switches, in particular) from a designer point of view using different fabrication process approaches. This means that the focus will be on how to eliminate or alleviate at the design stage the effects of the most relevant failure mechanisms, rather than focusing on the underlying physics of failure. The knowledge of this latter is on the contrary of crucial important in order to find out the most effective design for reliability solution.

In order to evaluate how the design for reliability applies to different manufacturing process, a well established metrics called Technology Readiness Level (TRL) [3] has been used to sort out the three R&D processes taken hereby in consideration. This raking was originally done by NASA and then widely adopted by other companies and institutions such as ESA, for finally being adopted also from the consumer electronics at large scale. It assesses the maturity of the technology prior to incorporating it into a system or subsystem. There are 9 different levels:

1. Basic principles observed and reported
2. Technology concept and/or application formulated
3. Analytical & experimental critical function and/or characteristic proof-of-concept
4. Component and/or breadboard validation in laboratory environment
5. Component and/or breadboard validation in relevant environment

6. System/subsystem model or prototype demonstration in a relevant environment (ground or space)
7. System prototype demonstration in a space environment
8. Actual system completed and "Flight qualified" through test and demonstration (ground or space)
9. Actual system "Flight proven" through successful mission operations

An analysis of the different R&D approaches will be presented by highlighting the differences between the different levels in the TRL classification (Figure 1). This thesis intends to show how reliability can be faced by taking into account fabrication processes with different TRL starting from a low TRL (LAAS-CNRS) passing through a medium TRL (CEA-Leti) and finishing with a high TRL (IHP)¹.

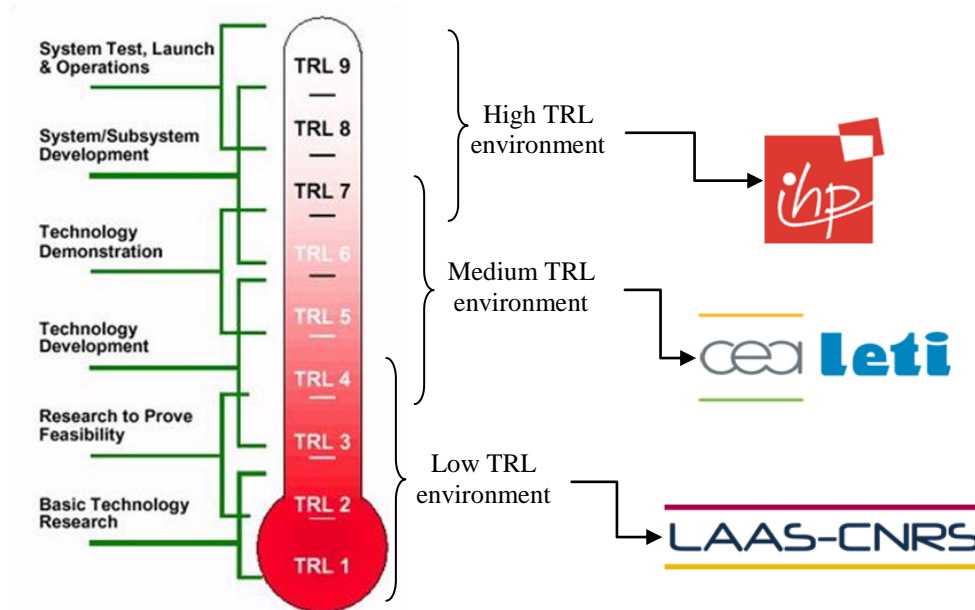


Figure 1: Description of the studied fabrication process in the TRL classification [3]

The main contributions of this thesis are:

- In terms of adaptability of RF-MEMS based circuits:
 - Design and characterization of SP4T and phase shifters using LAAS-CNRS capacitive and resistive cantilevers.
 - Design and characterization of SPDT and design of routing matrices from DC to 50GHz with CEA-Leti devices.
 - Design of SPDT and 2-bit phase shifters at 50GHz: based on a BiCMOS-MEMS co-integrated process (IHP)
 - Design of a novel configuration for absorptive switches at 50GHz: based on a BiCMOS-MEMS co-integrated process (IHP)
- In terms of Design for Reliability:
 - Development of 3rd metal layer for LAAS-CNRS capacitive switches
 - Study of the RF performance evolution of CEA-Leti Ru-Ru contacts
 - Development of equivalent circuit models for:
 - Process dispersion characterization (LAAS-CNRS, CEA-Leti and IHP)

¹ This ranking is uniquely based upon the opinion and experience of the author and does not represent the view of the associated organizations (CNRS - TAS).

- Failure analysis (LAAS-CNRS,CEA-Leti and IHP)
- Process monitoring in real time (IHP)
- Synthesis of new components (Series switch IHP)
- Development of the Design for Reliability strategy depending on the TRL environment for the three fabrication processes

The thesis is divided in five chapters. The first one is an overview of the most relevant reliability challenges encountered in RF-MEMS devices, and how they can be counteracted already at the design phase. Specifically, the techniques are focused on how to solve the dielectric charging phenomena, the contact degradation and the thermal effects from a design point of view. In addition the concept of Design for Reliability and the reliability characterization tools used through the manuscript are described.

From chapter two to four an exhaustive description of the different studied process at different TRL environment is done. Each chapter describes the fabrication process and the devices fabricated and characterized extracting an equivalent circuit which is used a posteriori for failure mechanisms description and study. Once the failure mechanism is detected, different techniques, depending on the TRL environment are proposed in order to minimize its effect. Moreover, different routing circuits are designed, fabricated and characterized in order to demonstrate the adaptability of each fabrication process.

Finally, in the last chapter the comparison between the different TRL environments is done based on the studied process. The comparison is done using five critical aspects of the process:

- Adaptability: this concerns the possibility of integrating different configurations (series/shunt) and topology (resistive/capacitive) in the same run,
- Process flexibility: the possibility to introduce new materials in the original process and/or modifying the process steps.
- Process simplicity: measured by the number of masks used for the fabrication (packaging not included)
- Process Repeatability: this defines the variation of the RF and mechanical performance of the devices over the entire wafer and from wafer to wafer. The tolerances refer to the variation on the physical dimensions (size and roughness of materials) of the structures.
- Device robustness: failure mechanisms with their associated RPN

These results define the strategy to follow when facing reliability from the designer point of view (Design for Reliability). The comparison is extended to nowadays existing manufacturing process of different TRL.

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Chapter 1

Design for Reliability in RF-MEMS

In this chapter an overview of the most relevant reliability challenges encountered in RF-MEMS devices, and how they can be counteracted already at the design phase are presented. Literature has shown hundreds of publications about RF-MEMS components demonstrating very good performance based on original smart ideas and pointing out the reliability shortcomings hampering their commercial exploitation. This chapter is not intended to list them all nor to deepen the underlying physics of failure, but rather to focus on the most relevant example of design tricks and stratagems introduced to date. In order to match application specifications on reliability, in some case, this can be done only at the cost of reduced RF performance. With this aim in mind, after a small introduction about basic concepts of reliability study, two different approaches are pointed out by addressing the Design for Reliability from a component and a circuit point of view.

In the first approach, some examples of RF-MEMS devices which address the main reliability issues are described. In the second one, the first commercial circuit that nowadays exists is presented as an example of how RF-MEMS can be placed in real circuits.

1.1 Introduction: Reliability issues in RF-MEMS

1.1.1 What does Reliability mean?

The word “Reliability” comes from Latin “*religare*” which means hold firmly. This idea of robustness is commonly used in the scientific community when speaking about reliability in devices. Strictly speaking, the exact definition of the word is *the probability of a system or component to perform its required functions under stated conditions for a specified period of time*. This definition involves three important topics which RF-MEMS designers should be aware of and will be depicted below: probability, required functions and conditions during a period of time [4].

Probability: failure mechanisms study

The probability quantifies the confidence of the devices. In other words, it shows how many times the component or circuit will accomplish the expected performance. Consequently, this needs the definition of the “expected performance” and the reason of its not-accomplishment. While the first will be defined by the end-user (maximum losses, power handling ...), the second needs a deeper study basically on the physics of the device.

The failure mechanisms (process which leads to failure) that have more importance in RF-MEMS are charging of dielectric, creep, plastic and elastic deformation, structural short, capillary forces, fusing, fracture, dielectric breakdown, corrosion, wear, equivalent DC voltage, Lorenz forces, whisker formation, fatigue, electromigration and Van der Waals forces. All these mechanisms are caused mainly by the device thermal budget (during manufacturing and in working stage) and the device working environment (humidity, contamination...) [5].

One of the methods used for determining the potential failures that might occur in RF-MEMS and its effect on all other parts of the system is the FMEA (Failure Mode and Effect Analysis). This analysis is able to determine if the failure is related to design, technology, environmental or operational issues and in which moment of the lifecycle it may occur [6]. For each identified potential failure mode on the FMEA, a RPN (Risk Priority Number) is assigned multiplying three factors:

1. Severity (S): From 1 to 10 depending on the affectation of the product performance (1: not noticeable; 10: extreme failure)
2. Occurrence (O): From 1 to 10, it quantifies how often the effect is predicted to be observed (1:unlikely; 10:inevitable)
3. Detection (D): From 1 to 10, it measures the capability of detecting default chips before sending to customer (1: detectable; 10: not-detectable)

Very often, reliability study is stopped in this stage (physical understanding of failure modes). However, as it will be seen in section 1.1.2, this is only the first step and should be followed by long term tests which allow the end user to infer how the performance will evolve versus time. For this reason, this section 1.1.1 is not intended to be exhaustive on this regard but rather to present some tools for lifetime characterization.

Required functions: environment towards the application

RF-MEMS technology has demonstrated to be a very good candidate for high frequency applications. It is mainly due to their inherently low losses, low power consumption and high linearity and isolation with respect to competitive technologies (PIN, MESFET, HEMT...). One of the niche markets which RF-MEMS technology aims to is redundancy, routing and phase shifting circuits for space applications [5]. The space-specific operating conditions are radiation, vacuum, thermal shock and vibrations [7].

In terms of radiation, the mechanical properties of silicon and metals are mostly unchanged. The main failure mode at high radiation is the accumulation of charge in dielectric layers which is critical for electrostatically actuated devices since an actuation at 0V can be achieved. Some experiments has shown devices working under doses between 150 and 300kRad, but others have only reached 10kRad [8]. A radiation tolerant device can be obtained avoiding charge trapping in dielectric layers by means of geometry changes in the electrodes and charge dissipation layers (Fig.1-1).

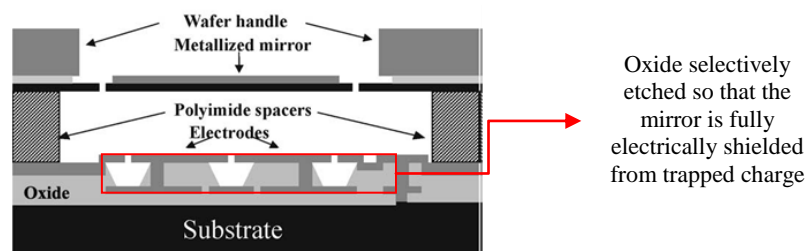


Fig.1-1: Cross section of the solution for avoiding charge trapping proposed in [8]

In space, devices operate in extremely high vacuum which can be a problem if the package is not hermetic and if the device generates few mW of heat². For this reason, the development of a hermetic package (5000ppm of water vapour initially and leak rate of 10^{-8} atm*cm³/sec) is a must in any space application for RF-MEMS. Moreover, it not only avoids outgassing, mass loss and surface contamination, but also allows to test the device in earth at space conditions.

The typical temperature range that the device could suffer is from -80C to 100C per day despite depending on the orbit. Thermal shocks can lead to failure of the die bond, cracking of the chip and delamination of the layers. The solution to this problem is either to use a process whose materials have the same CTE (Coefficient of Thermal Expansion) or to implement sandwich structures which compensate the different CTE of the used materials.

Finally, the vibrations level during launch and separation can reach values from 5Hz to 100Hz and from 3 to 20G. MEMS's mass is typically over few micrograms, so shocks of 1000G produces mN range forces ($F=m*a$). Creating a symmetrically suspended geometry, avoiding stress concentration (no sharp corners) and minimizing strain, mm-scale suspended devices can survive repeated shocks (Fig.1-2) [9].

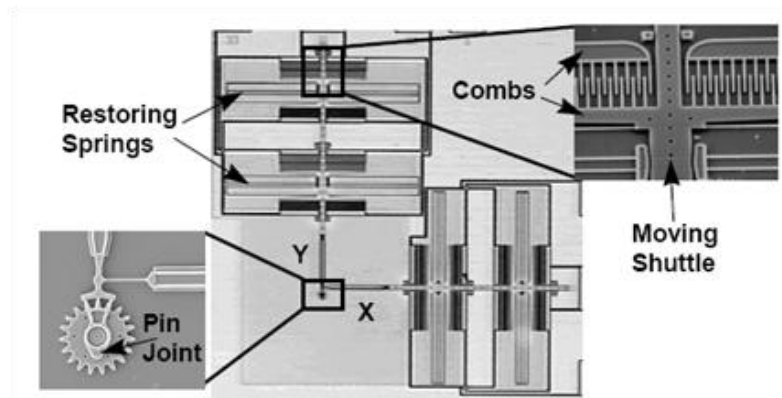


Fig.1-2: Sandia National Labs device that demonstrate 40000G shock

Period of time: long term behaviour of RF-MEMS

The lifecycle of a device and its failure rate is related by the bathtub curve (Fig.1-3) which divides lifetime in three regions: infant mortality, useful life and wear out. When testing reliability in devices, it should be clear in which region of the bathtub curve the device is in order to determine the failure mechanism.

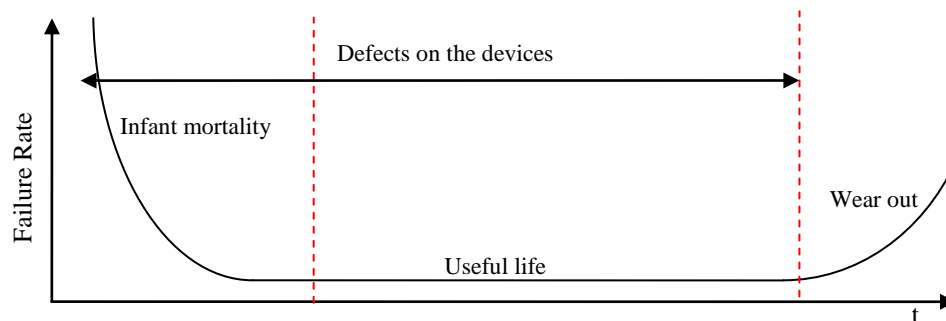


Fig.1-3: Bathtub curve with the different regions associated to the lifetime of the device

The infant mortality region is strongly related with the yield of the fabrication process because it separates “the bad” and “the good” chips regarding the initial mechanical and RF

²Normally dissipation values are around few μ W except for thermally actuated MEMS

performance. In order to consider that this region is passed, a burn-in test is done till the initial performance reach stable value (the criteria of stable value is a defined percentage of variation depending on the application).

In the useful life region, the device reaches its normal behaviour. In fact, the reliability of the device should be tested in this region since any defect due to the fabrication process is expected and only device characteristics (mechanical and electrical) play important role. Within this region random defect can appear and the End of Life (EOL) is defined by the beginning of the degradation of the device.

Finally, in the wear out region the materials start to degrade and the definition of the accelerating factors to reach the end-of-life is required. In this period it is also very important to define which parameters of the design are more sensitive to variations of the material properties (sensitivity study).

In order to know which class of failure (infant mortality, random or wear out) is present, the slope (β) of the Weibull plot is used as indicator [10]. In a typical Weibull probability plot two axes are defined (Fig.1-4):

- Age (X) (operating time, starts and stops, cycles, time at high stress...): it is in logarithmic scale and usually the appropriate parameter is suggested by the specific physics of failure mode. The best choice is the one that makes the data fit to a straight line
- Cumulative Density Function³ (CFD) (Y): the portion of units that will fail up to age t in percent.

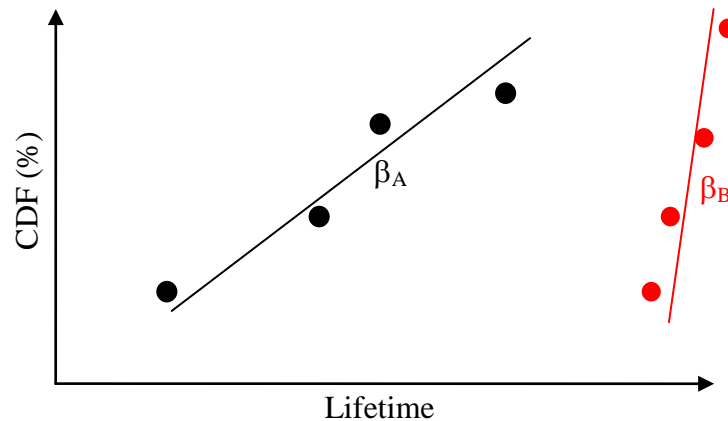


Fig.1-4: Example of Weibull plot for a device suffering from dispersion (black) and near ideal device (red) with the corresponding Weibull curve.

Regarding the slope, if $\beta < 1$, it indicates infant mortality while if $\beta > 1$ it means wear out failure. When $\beta = 1$, it is considered random failure independent of age (useful life) [10]. The ideal process should have a very high slope (near vertical line) which would mean that the lifetime can be predicted exactly and the dispersion of the process is very low. On the other hand, processes with low β (near horizontal line) show failure at any time during lifetime which makes the failure unpredictable (very high dispersion).

³ $CDF(x) = P(X \leq x)$: Probability that the random variable X takes on a value less than or equal to x .

1.1.2 What does Design for Reliability (DfR) mean?

Design for Reliability is a process which includes tools and practices in order to describe how to drive reliability challenges and increase lifetime in products. This improvement does not necessarily imply better performance but rather a compromise between reliability and desired or acceptable performance. In Fig.1-5 a typical design process flow is described showing the two types of reliability depending on the stage of the design flow.

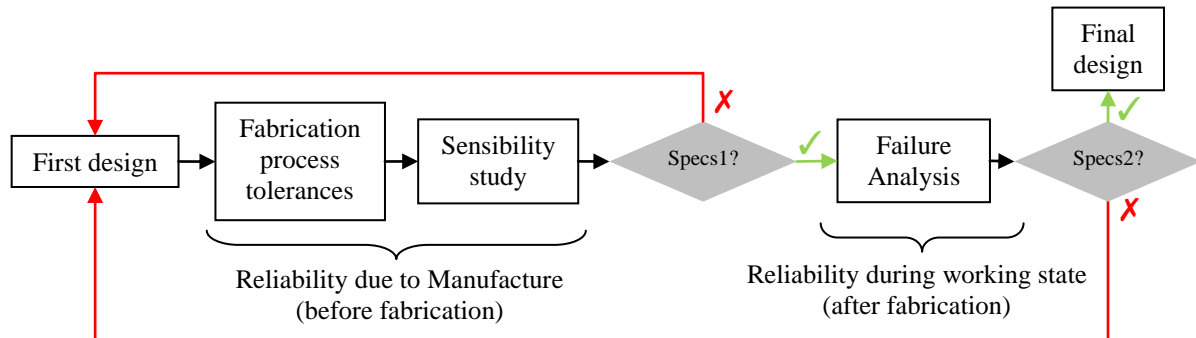


Fig.1-5: Typical design process flow of a device. Specs1 refers to RF performance and Specs2 to lifetime performance

In Table 1-1, an overview of the main failure mechanisms in RF-MEMS is shown with existing solutions proposed either through the process optimization (Reliability due to Manufacture) or through the design taking into account the failure causes (Reliability during working state). They will be discussed more in details in section 1.2

Failure mechanism	Failure cause	FMEA parameters ⁴				Possible solution
		S	O	D	RPN	
Long-term plastic deformation	Thermal induced charges in material properties	7	7	3	147	Push-pull switches
Temperature (T) induced Elastic deformation	Environment T					-Use of same CTE materials or sandwiched ⁵ movable parts -Temperature control systems
	Different CTE					
	Power RF signal induced T	7	7	5	245	
Equivalent DC voltage	Non uniform T					Optimized heat-sink design of metallic bridges
	High RF power (spontaneous collapsing or stiction of the mobile part)	7	4	6	168	
Dielectric charging and dielectric breakdown	Electric field charge					-Complex actuation waveforms -Low-voltage designs -Special dielectric materials Dielectric-less or proximity ⁶ switches
	Radiation					
	Air-gap breakdown	8	10	2	160	
	Electron emission					

⁴ Extracted from Enabling Deployment of RF MEMS Technology in Space Applications (ENDORFINS) ESA Project

⁵ Sandwiched membranes stack different CTE materials producing a compensated stress structure

Failure mechanism	Failure cause	FMEA parameters				Possible solution
		<i>S</i>	<i>O</i>	<i>D</i>	<i>RPN</i>	
Micro welding	Soft metals in contact					
	High current through contact (asperities) ESD	9	7	4	252	Increased restoring force Hard contact materials
Structural Short (electrical and non-electrical connections)	Contamination particles remaining from sacrificial layers					
	Wear particles	9	5	4	180	Holes in movable parts for total release of sacrificial layer
	Fracture					
	Lorenz Force Shocks					
Capillary Forces	Presence of humidity	10	4	4	160	Hermetic package
Fracture	Fatigue					
	Brittle materials and shock	10	4	2	80	Thick movable parts Push-pull structures
Corrosion	Presence of water or fluid materials	7	5	2	70	Hard contact materials
	Corrosive gases					
Fusing	High RF power ESD	10	4	2	80	ESD protection
Wear, Friction and fretting corrosion	Sliding rough surfaces in contact	8	4	6	192	Hard contact materials
Creep	High metal stress and high temperature					
	Creep sensitive metal	6	5	4	120	Creep-resistance materials in movable parts Control stress in movable parts
Fatigue	Large local stress	8	3	5	120	Round shaped membranes
	Large thermal cycles					
Van der Waals Forces (Stiction)	Large very smooth and flat surfaces in close contact	10	1	4	40	Double electrode
Electromigration	High current density in metals	8	2	4	64	Hard contact materials

Table 1-1: Summary of possible solutions to main reliability issues in RF-MEMS [10]

⁶ Proximity switches are capacitive devices that avoid the contact between metal and dielectric in actuated state by changing the air-gap capacitance.

Reliability due to Manufacture (before fabrication)

This subdivision of the DfR is focused on the characterisation of the tolerance of fabrication process and on the sensibility study of the parameters involved in the design. In RF-MEMS, two main sources of dispersions are related to the fabrication process: geometrical (shape and size of the elements) and thickness of the layers (uniformity on the deposition over the wafer). This means that a very accurate control of each step of the fabrication process is needed and it would allow designers to predict possible deviations in the RF performance and carry out the sensitivity analysis.

The first step is to quantify through a probability distribution function a mean and standard deviation value of the dimensions of the elements and the mechanical properties (stress, mechanical resonance frequency, stiffness...) in the movable parts. The first one is strictly related to the deposition conditions which define the resolution of the different patterns which means that they will not vary during the following steps. On the other hand, the mechanical properties on the membrane will depend not only from the deposition technique but also from the following process steps such as etching, liberation of the sacrificial layer and packaging. In particular the thermal budget to which the device undergoes during the deposition and the following steps is paramount to assess the ultimate mechanical properties of movable parts.

When referring to standard commercial fabrication process (high TRL), CMOS for instance, the existing deviations in the dimensions are negligible in terms of RF performance (for example $\pm 30\text{nm}$ in a $0.25\mu\text{m}$ BiCMOS process). However, research processes (low TRL) have higher values of dispersion ($\sim \pm 5\mu\text{m}$ in LAAS-CNRS process) due to not automated and less precise process steps. In [13] it is shown how this dispersion can affect tuneable filter bandwidth and working frequency while doing a yield analysis of the process. In [14], it is demonstrated that the variation of these parameters can affect also the mechanical properties of the suspended structures which will directly impact the actuation voltage thus the $C(V)$ response. In any case, the modelling of these fabrication process uncertainties is the key issue in order to adapt the design to reach the desired performance [15].

Once the fabrication process tolerances are studied and modelled, the sensitivity study is done in order to see which deviation will have higher impact factor to the RF performance. This study allows to isolate the specific process steps which need to be improved in order to meet the expected electrical specification [16]. For this study it is very important to know not only the deviation over the wafer, but also the wafer to wafer dispersion and, nowadays, this is only possible in standard processes (less or not at all in research ones).

Reliability during working state (after fabrication)

This step of the design flow is pretended to point out and predict which will be the evolution of the RF performance over time. The aim of this step is to determine the extreme conditions tolerated by the device and for how long before failure it occurs. The definition of the accelerating factors is a key issue to develop the endurance tests and the optimal operational conditions as far as the same failure can be reproduced as it occurs in normal working conditions. In Table 1-2 the failure mechanisms and their accelerating factors are depicted.

When using acceleration data to predict lifetimes with acceleration models, one must assume that the shape of the curve is the same in the accelerated condition as in the typical working conditions. Lifetime prediction requires:

- Knowledge of environmental (operating and non-operating), lifetime of end product, and manufacturing use conditions such as subsequent processing steps (packaging, printed circuit boards).

- End product packaging and application.
- Customer's acceptable failure rate over the lifetime of the product.
- Stress conditions necessary to identify failure mechanisms.
- Acceleration testing and models for lifetime prediction.
- Statistical manipulation of failure distributions in reliability testing.

Failure mechanism	Accelerating factor
Fatigue	Number and frequency of actuation cycles Maximum applied strain Humidity
Creep	Temperature Applied strain
Van der Waals forces (stiction)	Humidity, shock and vibration
Structural short and electromigration	Electric field Temperature and humidity
Dielectric charging	Electric field and radiation Temperature and humidity
Corrosion	Humidity and temperature Voltage
Fracture	Resonant frequency Vacuum

Table 1-2: Failure mechanisms of RF-MEMS and their accelerating factors

Once the lifetime is characterized and the evolution through the time is known (failure signs and burn-in period mainly), the next step would be to build a BIST (Built-In Self-Test). This technique is able to track the performance of the device detecting correcting, under given limits, for undesired deviation or behaviours. For this reason is essential to identify which parameters of the design are the most suitable indicators in order to monitor the device performance. On the other hand, the implementation of BIST in MEMS process increases the complexity of the needed process thus the cost.

The aim of this solution is to add more reconfigurability to MEMS-based systems since it is possible to decide when the wear out period starts and to switch to a redundant circuit. The implementation of a BIST needs additional intelligence and hence electronic. Normally, it is a switching node based on analog multiplexers and it has already been implemented in accelerometers [17] and optical switches [18]. BIST for RF and microwave applications (LNA, PLL and EVM [19]) have already been developed showing an improvement of the circuit efficiency.

Literature has shown very few examples of BIST in RF-MEMS. There are two main reasons: from one side the co-integration of MEMS with other technologies in a stable fabrication process is still under development. And, from the other side, no standard of reliability has been established for MEMS devices and circuits that determines the range of the acceptable performance. Without these limits the BIST module is very dependent on the application and the control system should be adapted each time.

One of these few examples is proposed in [20] where CMOS circuit is used to control the charging and discharging of capacitive MEMS (developed under the HERMiT program from the US Air Force [21]). The solution is based on sensing the C_{MEMS} and using two switches (S_1 and S_2) to charge and discharge the device depending on the comparison with the reference value C_{REF} (optimal value of C_{MEMS} capacitance) as seen in Fig. 1-6. The challenge of this development is to be able to measure the C_{MEMS} capacitance easily by means of the correspondence between $C_{MEMS}(V_{MEMS})$ and $V_{MEMS}(C_{MEMS})$ [20]. Also in Fig. 1-6 it is shown how the V_{MEMS} is tuned to reach the targeted capacitance. Continuous stress (1h) has been applied demonstrating the capability of the circuit to adapt the C_{MEMS} capacitance enhancing its lifetime.

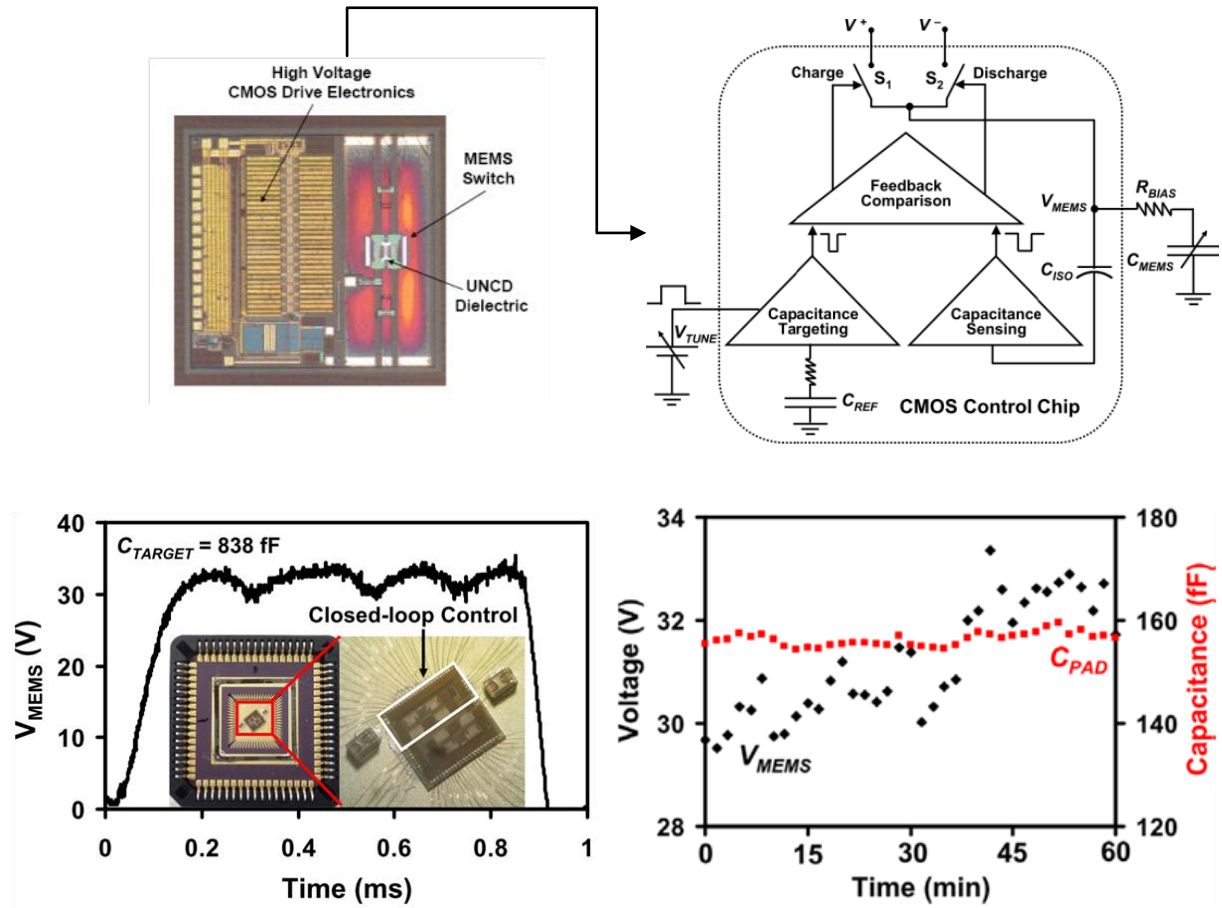


Fig. 1-6: Image of the MEMS+BIST (top-left) and block diagram of intelligent CMOS control circuit (top-right) proposed in [20]. The measured V_{MEMS} (bottom-left) over time to control the desired C_{MEMS} to the target C_{TARGET} and the evolution of V_{MEMS} during 1h of constant stress for a stable capacitance (C_{PAD} is a capacitance for sensing the C_{MEMS} capacitance).

1.2 Component Reliability

This section is a study of how the techniques explained in previous section (1.1.2) are applied to RF-MEMS. Here, reliability is seen from a component point of view which means that the most advanced knowledge about each failure mechanism is taken into account at the design in order to increase the device's lifetime. Normally, when addressing DfR issues by introducing new materials in a previously established fabrication process, each step may need to be adapted and re-optimized. For this reason, in order to explore solutions for reliability processes developed on research platforms (foundries) are more flexible and adaptable to

implement new ideas and validate them before to justify the transfer on a much costly industrial production line.

The three most relevant failure mechanisms of RF-MEMS switches are dielectric charging, contact degradation and temperature induced elastic deformation. While contact degradation is only seen in resistive switches, dielectric charging and temperature induced elastic deformation can be found in both resistive and capacitive devices. In both section 1.2.2 and 1.2.1 they will be studied with the different fabrication process approach (different TRL).

1.2.1 Research solutions

Research fabrication platforms (low TRL) have very high flexibility in terms of process design. They allow proposing some ideas to solve these failure modes even though at a price of limited repeatability of the results (i.e. good for proof of concept).

Dielectric charging

Dielectric charging is observed when the two metallic layers that contact the dielectric are at different potential voltage. This can occur either in the contact region (capacitive switches) or in the actuation electrode due to the isolation layer which avoids the contact between membrane and electrode. There are two main techniques to avoid dielectric charging: avoid the above mentioned contact or control the charges on the dielectric. The first announced solution is more efficient and it does not depend on the material's properties, which would imply a deep study.

However, some work has been done in order to determine which isolating materials have the lowest discharging constants and how the charges can be compensated during useful life. In [22]-[23], for example, ultra-nano-crystalline diamond (UNCD) has been demonstrated to achieve a discharging constant 6 times smaller than others due to its nanostructure. In the same direction in [24], typical dielectric materials in RF-MEMS based process such as Silicon Nitride have been doped with Carbon Nano Tubes (CNT) decreasing the voltage drift from 9V/min (without CNT) to 0.03V/min with 46 CNT/10 μm^2 .

Despite not being a true DfR solution (rather a control of reliability), another method for reduce the induced charge in dielectrics is through a bipolar actuation waveform. Despite being demonstrated that the charge injection and removal are not identical for positive and negative voltages it has been proved that it increases lifetime. In addition, this solution does not account for the possibility of ionizing radiation from environment that is of great interest in satellite and high-amplitude communication systems. The “dual-pulse” waveform used in PIN diodes can also be employed. It consists in a first step at a higher actuation voltage in order to provide enough electrostatic force to actuate the switch followed by lower voltage since the membrane needs less force to be maintained in down state (Fig. 1-7). The main challenge of this type of solution is to know how the capacitance will evolve as it is proposed in [25].

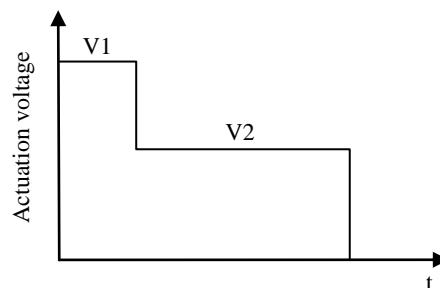


Fig. 1-7: “Dual-pulse” actuation voltage waveform for lower dielectric charging

The solution of avoiding contact needs the development of stoppers and the perfect control of the deformation of the membrane during the actuation. In [26] it is seen that using a thin dielectric layer on the RF line as stopper, a zipper tunable capacitor is developed. The actuation pads are not isolated using a dielectric in order to avoid charging in DOWN state (Fig. 1-8b).

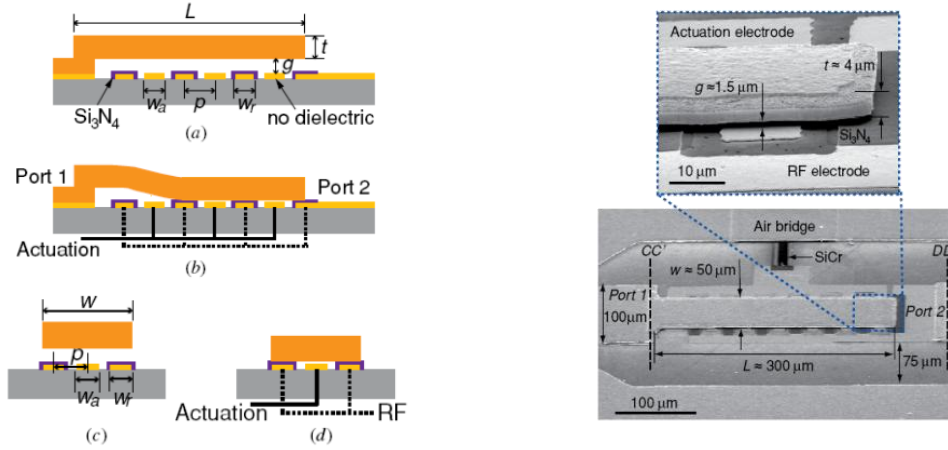


Fig. 1-8: Cross section (left) and photo of the tunable capacitor proposed in [26]

There are three main advantages of this design which demonstrate how the design can be conceived taking into account the reliability and the RF performance at the same time (DfR):

- 1) High tunability: the actuation electrodes are distributed along the beam, and the beam makes an intimate contact with the RF electrodes.
- 2) No dielectric charging: the dielectric layer on top of the RF electrodes serves as a stopper, and due to the short distance between the RF electrodes, the beam does not collapse on the actuation electrodes as the voltage is increased. This means that the dielectric layer is not required on the actuation electrodes thereby minimizing any charging.
- 3) A self-aligned process and a single metal definition are used which results in a simple fabrication process.

The evolution of the solution proposed in [26] is the removal of all the dielectric layers of the design and integrate the stoppers in the membrane. This is the solution proposed in [27] where a dielectric-less capacitive cantilever is presented (Fig. 1-9). The pull-in voltage shift is monitored concluding that, even if the charging is present (following dielectric relaxation law [29]) in the device, the choice of the optimal actuation waveform can yield a drift of 20V in 24 years.

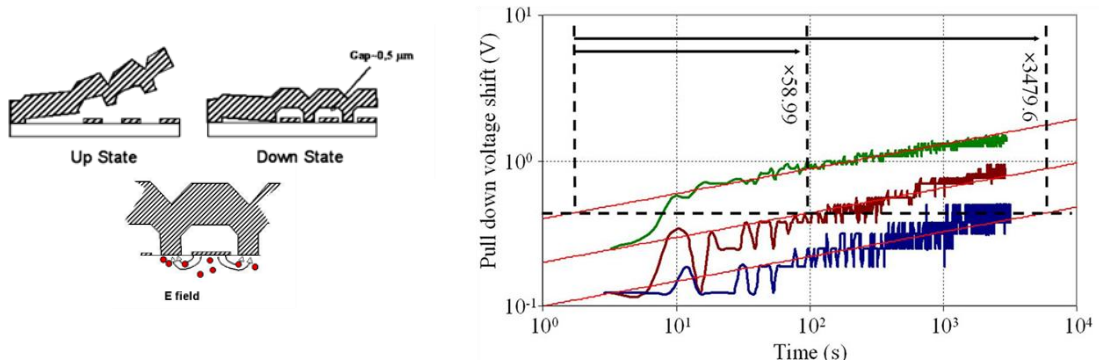


Fig. 1-9: Dielectric-less cantilever (left) and measured pull-in voltage shift versus time for bipolar applied bias (right) with duty cycles of 95.4% (green curve), 47.7% (red curve), 23.4% (blue curve) [27].

The disadvantage of this solution is that the UP and DOWN state capacitance should be completely controlled, through the stress of the membrane, which it is not trivial. Moreover, due to the initial stress on the membrane, the implementation of stoppers on the movable part is very difficult as it is demonstrated in [28] where the same contact-less principle has been developed.

Contact degradation

The most important parameter that should be taken into account for resistive switches is the contact force. At this point two factors are involved: the mechanics of the membrane (stiffness and actuation voltage) and the hardness of the contact material. The stiffer membrane, the higher actuation voltage and the higher contact force, but, due to limitations in terms of actuation voltage availability (less than 100V in space applications) the size of the actuation pads should be enlarged. Moreover, the harder material, the higher reliability, but, higher actuation voltage are needed. Taking into account these two inputs a compromise should be done in terms of contact force and actuation voltage.

Before going in detail with the physics of the contact material, another approach is possible. In [30] a mechanical approach for solving the degradation problem is proposed. In this case, three choices are taken in terms of design for reliability:

- To reduce switch failure: the restoring force should be increased to overcome stiction.
- To assure that the switch can function in a low-voltage environment (60V): reduce the residual stress gradient in the cantilever, increase beam area, reduce gap height, reduce beam stiffness.
- To increase restoring force: increase beam thickness, shorten beam length, or increase beam area.

Taking into account the above considerations, a robust beam design is presented by optimizing the parameters w , d and l (Fig. 1-10). A part from that, a sandwiched membrane is proposed since its materials have very different CTE which leads to high values of residual stress. It is determined that the favorable structure is a short, wide structure with a large electrode area. Compared to similar bi-layer designs, sandwich designs can reduce actuation voltage while remaining the same restoring force.

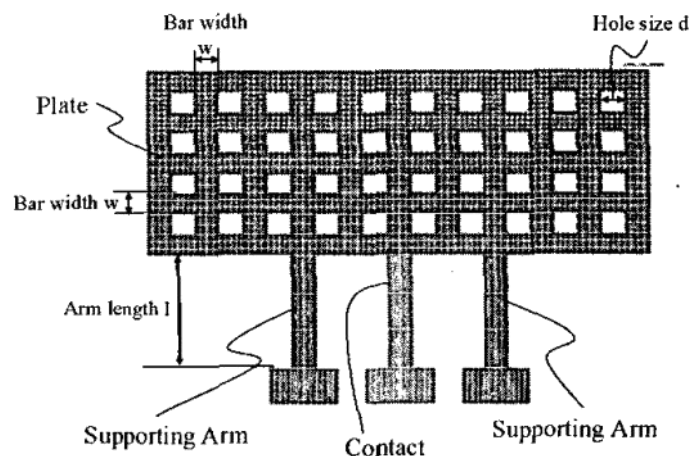


Fig. 1-10: Optimized design proposed in [30] with the mechanical approach

Regarding the contact material, typically gold (Au) has been traditionally used. The advantage is that from the fabrication process point of view; it is very easy to integrate (resistant to surface oxidation and sulfide layers), and, from the performance point of view; it has very low

contact resistance (losses). However, it is a soft material compared with others: copper/tungsten/gold stack (Cu/W/Au), rhodium (Re), tungsten (W), molybdenum (Mo), palladium (Pd), silver/tungsten/rhodium (Ag/W/Re), palladium multilayer structures (Ag/Pd, Au/Ag/Pd, Au/Pd), and Ag/W/CdO. For example, some gold alloys (Au-Pt, Au-Pd and Au-Ag) have been studied in [31]. The considerations on choosing the candidates regarding a consistent and repeatable fabrication process are:

- Avoid two-phase alloy regions
- Avoid intermetallic compounds
- Assure high actuation voltages
- Allow for the testing of unpackaged devices.

In Fig. 1-11 it is seen that with an Au-Pt alloy as a contact material the lifetime is increased. However, the contact resistance is increased and the contact resistance decrease for the Au contact (fail to open) and increase for the Au-Pt one (fail to close).

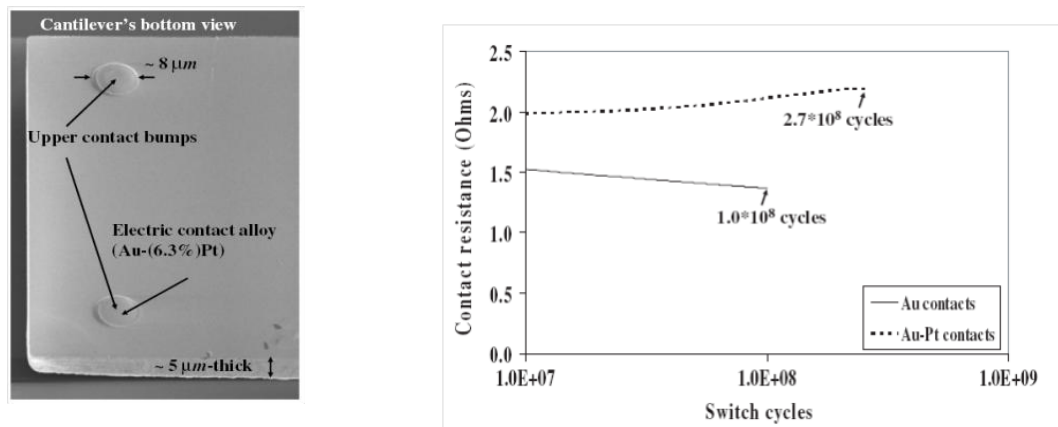


Fig. 1-11: Contact dimples (left) and contact resistance evolution (right) of the proposed alloys in [31]

Another recently used material is ruthenium for his hardness in front of gold which enlarges lifetime (Fig. 1-12). In [32] it is used as a covering material in a stack of Cr/Ru/Au/Ru demonstrating that higher voltages than in Au contacts are needed for similar contact resistance. Specifically for Ru, the contact surfaces have to match to each other during the first switching cycles until the contact resistance is stabilized. At low contact forces (actuation voltage of less than 60 V for Au/Ru–Ru/Au contacts and less than 40 V for Au–Au contacts), the resistance of the first cycles is very unstable (Fig. 1-12 left).

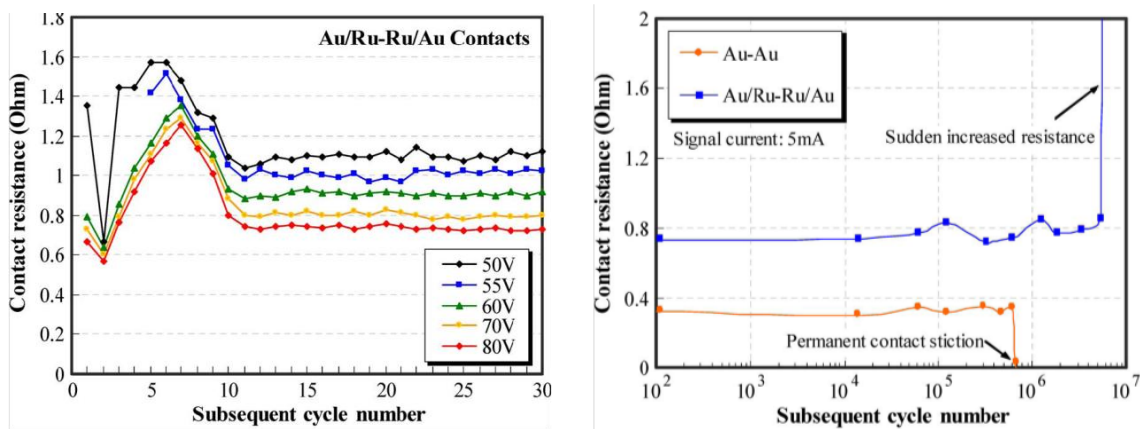


Fig. 1-12: Contact resistance stabilization of Ruthenium contacts (left) and comparison of lifetime between gold and ruthenium contacts (right) extracted from [32]

The Au/Ru–Ru/Au contacts require an actuation voltage of 80 V to result in a stable contact resistance of 730m Ω , whereas an actuation voltage of 40 V is sufficient for a contact resistance of less than 700m Ω for Au–Au contacts. This indicates that Au/Ru–Ru/Au contacts require a force that is at least four times larger than for Au–Au contacts. The contact resistance of the novel ruthenium contacts is much lower as compared with that of pure-ruthenium contacts in the literature [33].

Thermal effects

RF-MEMS devices are submitted to huge variations of operational temperature not only during lifetime, but also during the manufacturing of the devices. This thermal budget needs to be carefully considered since it will impact and determine the operational range and device lifetime.

The parameter that will be directly affected is the pull-in/out voltage since at high temperature, the membrane crumples leading to collapse. In order to prevent this, higher tensile residual stress is needed but at a cost of higher actuation voltage. This compromise is typically solved by identifying membrane geometries and composition that decrease the sensitivity to temperature of the switch.

Regarding temperature tolerant geometries, it has been demonstrated that membranes suspended all over its perimeter (diaphragm) are stiffer. However, the possible residual stress in the film could lead to increase actuation voltage. In [32] it is solved by using a corrugated diaphragm that increases the fabrication-induced stress tolerance and decreases the actuation voltage. Another solution to avoid all over suspended membranes is [34] where the thermal compensation is done by placing the symmetrical anchors at the centre of each face of the membrane (Fig. 1-13). The two anchor points located at opposite sides of the frame, cancel each other's torque. This solution has been used also in [35] for cantilever RF-MEMS devices.

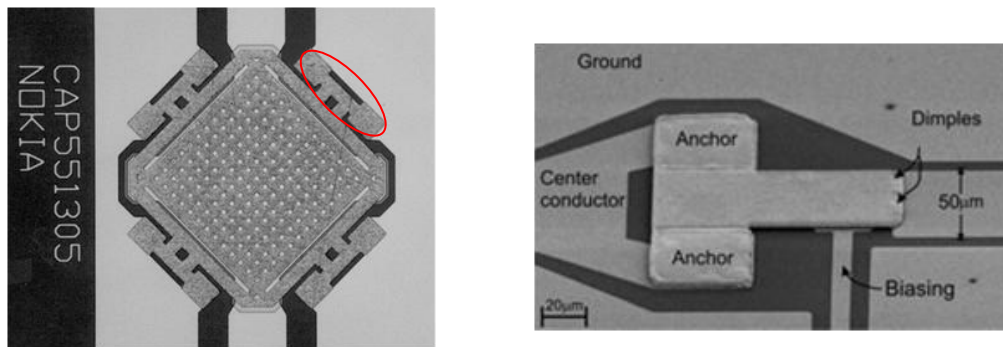


Fig. 1-13: Photograph of the temperature-compensated membrane proposed in [34] with the symmetric anchors (left) and the same principle applied to a cantilever from [35] (right)

The composition of the membrane plays also a very important role in the temperature compensation. The main source of induced-stress is the mismatching of the CTE (Coefficient of Thermal expansion) of the materials involved in the fabrication process. The design cannot avoid this but; the development of sandwiched membranes is the mostly used solution [36].

1.2.2 Industrial solutions

In this section a deep study of the nowadays commercially available (high TRL) RF-MEMS in terms of Design for Reliability is presented. The devices under study are MEMtronics and RadantMEMS.

MEMtronics

MEMtronics was formed in 2001 by Chuck Goldsmith to develop and commercialize packaged MEMS (Fig. 1-14) technology for use in microwave and millimeter-wave applications. Nowadays the company, instead of selling single RF-MEMS devices, is able to integrate the switches into a MMIC process for more complex circuits. The targeted frequency band goes from DC to 50GHz. The switch is designed in order to avoid dielectric charging, to be mechanically robust and to include on wafer packaging. The chosen design decisions will be described below.

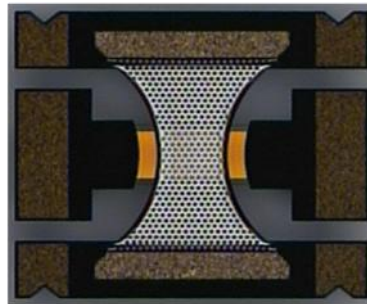


Fig. 1-14: Image of the MEMtronics RF-MEMS switch

In order to avoid charging phenomena, they have patented what they call “proximity switches” (Fig. 1-15) [37]. The principle of proximity switches is to separate the mechanical support structure from that of the electrical coupling mechanism. This allows the switch to operate with little or no dielectric charging, the dominant mechanism that limits the lifetime of MEMS capacitive switches. Dielectric supports made of silicon nitride or silicon dioxide keep the upper electrode supported a short distance above the lower electrode. The electrical coupling of RF energy from the upper plate to the lower plate is accomplished through the air gap between the two plates.

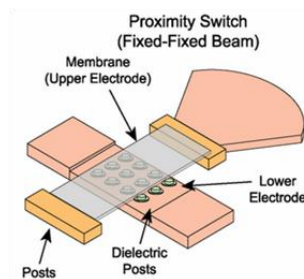


Fig. 1-15: Schematic of MEMtronics proximity switches

The proximity switch has several distinct advantages compared to other designs of capacitive RF MEMS switch:

- No charging of the air occurs between the plates. The only charging that may occur is through the mechanical (dielectric) supports maintaining the spacing between the two plates which represents a very small proportion of the total switch area.
- Increase the environmental robustness of the switch: maintaining an air gap between the plates reduces the sensitivity of switch performance to particle contamination.
- Suitable for space applications: the impact of radiation on the switch would normally be a reliability issue in this environment as it has been explained above (section 1.1.1).

In order to investigate the potential improvements in switch mechanical robustness molybdenum was chosen to replace aluminum as the membrane material in MEMS capacitive

shunt switches. Molybdenum provides a reasonable balance between thermal expansion coefficient and electrical and thermal resistivity. Moreover, for temperature compensation, a corrugated out of plane profile is optimized to control the stress relaxation of the membranes as demonstrated in [38] (Fig. 1-16). This solution maintains also suitable actuation voltages.

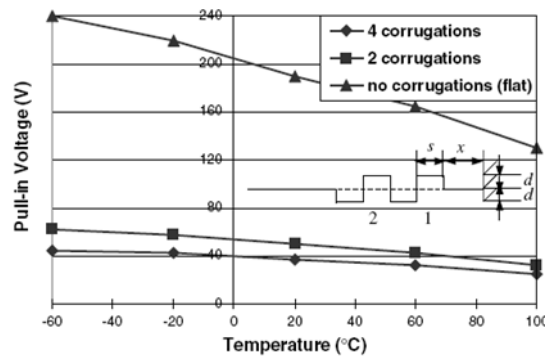


Fig. 1-16: Pull-in voltage for three different corrugated membranes as a function of the temperatures presented in [38]

These switches have the potential for operating for above 100 billion cycles and handling hot switching at multi-watt power levels. At microwave and millimeter-wave frequencies, the reduced capacitance ratio of these switches ($C_{on}/C_{off} \sim 20-40$) is still sufficient for constructing high-performance phase shifters and tunable filters.

Finally, a wafer-level packaging utilizing wafer processing techniques is developed [39] (Fig. 1-17). The packaging possesses a low dielectric constant, requires only moderate temperature ($200^{\circ}\text{C} - 275^{\circ}\text{C}$), and tolerates non-planarity and roughness. This means that:

- No seal ring
- Extremely small volume cavity
- No requirement for a package lid
- No requirement for hermetic thru wafer vias
- No double-wafer alignment required
- Requires only standard MEMS processing
- Substantial increase in the number of devices per wafer
- Packaged devices are thinner/lighter than any existing packaging technique
- Extremely low insertion loss
- No added parasitics
- RF circuit design transparent.

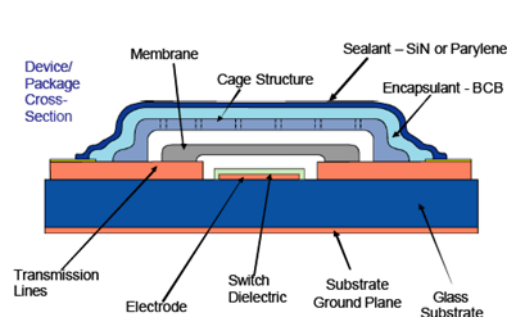


Fig. 1-17: Schematic cross section of the developed package in [39]

Even if the reliability challenges are solved, the process deviations need to be counteracted. In Fig. 1-18 it is shown that despite an improvement of the lifetime has been done from 2006 to

2007, there is a wide variation from switch to switch regarding lifetime (low β). This big variation in lifetime is due to infant mortality ($\beta < 1$) and could be controlled by means of an adaptative control circuit based on a CMOS process [20]. This concludes that the possibility of co-integration MEMS-CMOS is a big opportunity for RF-MEMS commercial possibilities.

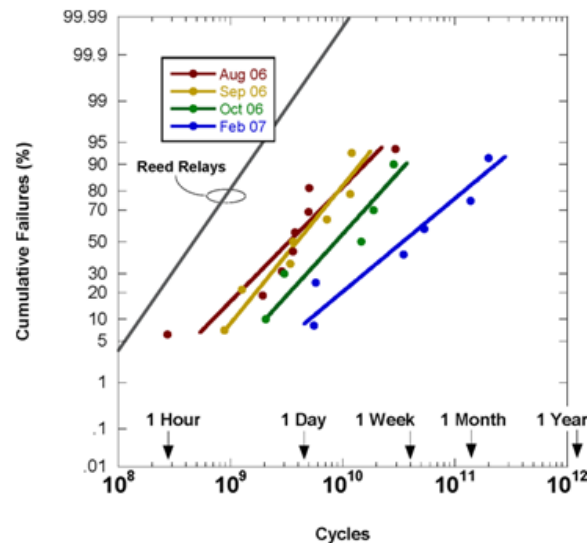


Fig. 1-18: Weibull curve of MEMtronics switch for different evolutions of the device extracted from [40]

Radant MEMS

Radant MEMS was founded by Jean-Claude Sureau and it is providing devices since 1999. This company commercializes not only single switches (SPST) but also SPnT working in wide band from DC to 40GHz. The Radant MEMS device (Fig. 1-19) has a rated lifetime of 100 billion cycles that has been independently validated by the US Department of Defense Laboratories. The targeted applications are telecommunications, automation, PC peripherals and automated test equipments. In this case, the contact material, the mechanically optimized cantilever and the hermetic packaging are the most relevant characteristics that will be explained below.

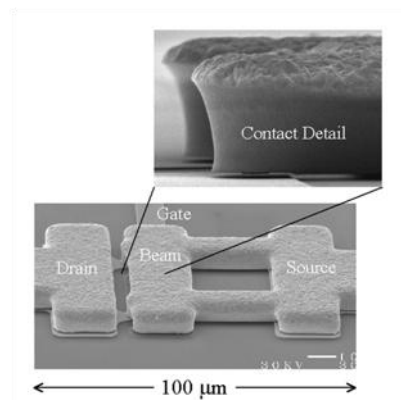


Fig. 1-19: Image of the RadantMEMS switch

The contact material is a thin layer of a proprietary refractory metal (Pt family) deposited on the underside of the beam and on the drain, giving better stiction-free lifetime than the more common gold contacts. Switches typically have 4 to 8 contacts in parallel to yield a total on-resistance, including interconnects, of less than 1 Ω when actuating at 100V. In [41] it has been demonstrated that using an array of micro-contacts instead of a single contact the hot-

switching reliability increases. Moreover, using a very high actuation voltage, the contact stability is assured since the contact force is very high.

Regarding the stress compensation, in this case, as it is a cantilever, only the initial residual stress affects the device through an initial deflection [42]. In Radant switch, the solution adopted is to increase the thickness of the gold cantilever (7-9 μm) which gives a very stiff device ($k > 100\text{N/m}$). In Fig. 1-20 (from [30]) it can be seen how the shape of the cantilever can be modified in order to achieve maximum stiffness. However, this flatness and the small gap (0.6-1 μm) implies that the working frequency range will not be higher than 20-30GHz due to the low isolation.

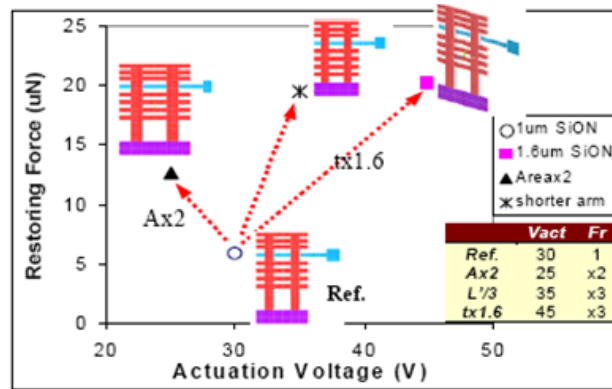


Fig. 1-20: Effect of the beam geometry in the actuation voltage by increasing the area (Ax2) or increasing the thickness (tx1.6) [30]

The switches are packaged with bulk wafer caps (Fig. 1-21) which are robust, hermetic and at wafer level. However, they need a large on-chip area for the sealing ring. Specifically, it is a top silicon wafer and a glass-to-glass seal at 450°C which is compatible with the tolerance to temperature of the device.

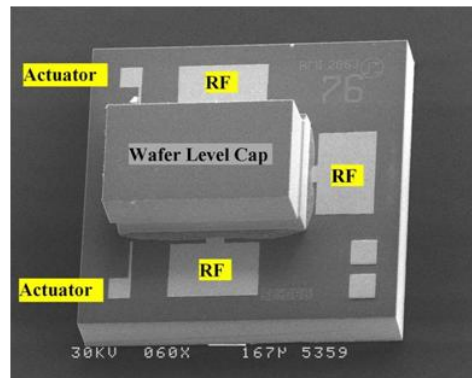


Fig. 1-21: Image of the RadantMEMS packaged switch

Extensive lifetime testing has been conducted by Radant as well as independently laboratories under the auspices of a Defense Advanced Research Projects Agency (DARPA) program. The first version of the RadantMEMS device (Benchmark 3) was tested at 20 dBm, with power applied only during switch closure or open to avoid hot breaks and makes (i.e., cold-switched), was performed at X-band on a batch of 32 switches. This led to a 50 percent passing rate to 100 billion cycles and a median cycle to failure of 280 billion cycles, as shown in Fig. 1-22. The improvements to the switch depicted above to improve contact reliability as well as process refinements to reduce contact contamination were done (Benchmark 4b) and they were tested at 20 dBm (cold-switched) at X-band on a batch of 64 switches. This led to

an 88 percent passing rate to 100 billion cycles and a median cycle to failure of 10 trillion cycles with the longest recorded lifetimes exceeding 1.5 trillion switch cycles before the test was halted after 30 continuous months. The improvements implemented for Benchmark 4 led to an order of magnitude increase in the median cycle to failure [11].

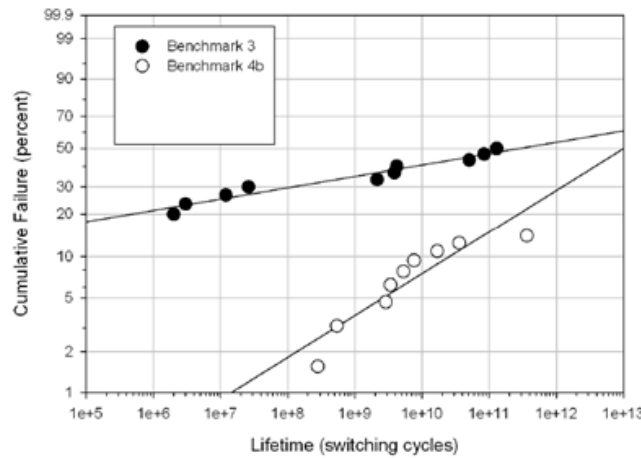


Fig. 1-22: Weibull curve for Radant MEMS [11]. Benchmark 4b is the evolution of benchmark 3

1.3 Circuit Reliability

Reliability in MEMS devices can be taken also into account regarding the circuit from a higher hierarchical level (circuit level and not device level). In this case, the application reliability constraints will be met by carrying out a robust circuit design and hence playing on its several different components and not only the RF-MEMS device one. In the case where it is assumed that the RF-MEMS device suffers from dielectric charging, contact degradation, etc. the design of the circuit will be done assuming the deviations introduced by these failure mechanisms and not trying to avoid them. Given that, these deviations are accurately estimated in advance. This is what it is called “circuit reliability”.

In this section two examples will be shown. The first one is an SPDT developed by Microsystem Technology Laboratory at KTH Royal Institute of Technology using resistive switches. The second one is the first commercial application of RF-MEMS variable capacitor from Wispry. They have been chosen again to compare the research laboratory results with respect to a mass-production device in terms of feasibility and repeatability.

Laterally actuated cantilever for a SPDT switch

Joachim Oberhammer is the team leader of the Microsystem Technology Laboratory (MST) which is a part of the KTH School of Electrical engineering. The group fabricates its silicon structures and devices at the KTH microelectronics laboratory. They are focused on developing innovative micromachined MEMS-tuneable components for RF and microwave applications. The trend is towards higher frequencies (E-bands, W-band, and beyond 100GHz), reconfigurable circuits, system integration with conventional millimeter-wave technology, and new applications.

The design presented in [43] has been fabricated implementing in plane moving MEMS in SOI device layers using bulk micromachining. The advantage of this technique is that enables lateral actuation which will be the key issue of the circuit. As it has been explained above, the degradation of the contact will determine the evolution of the performance since it is a resistive switch. For this reason, the contact stability should be assured and, at the same time,

as it is a research fabrication process, the fabrication steps should be as simple as possible in order to minimize technological dispersions.

The presented SPDT (Fig. 1-23) is based on a mechanically bi-stable SPST embedded in a coplanar waveguide. The end of each cantilever is a hook which is locked allowing the maintenance in actuated state without applying voltage (Fig. 1-23). The mechanical robustness of the laterally actuated switch cantilevers has been verified, at a switching frequency of 3 kHz with a measurement signal of 1.5 μ A, up to 150 million hot-switching cycles, after which the tests were discontinued without observing stiction. The tests were carried out with unpackaged devices and in uncontrolled atmosphere.

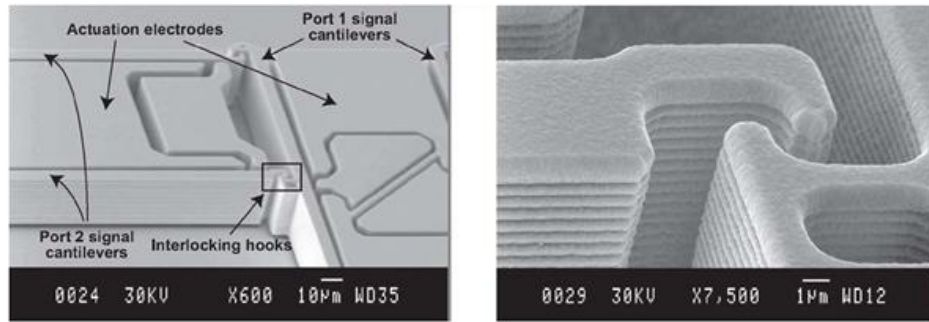


Fig. 1-23: SPDT (left) and detail of the hook (right) presented in [43]

The advantages of this design are:

- *Mechanical multistability*: the mechanical stability of every state is achieved by a mechanism with two perpendicularly arranged cantilevers with interlocking hooks. The actuation sequence has four mechanically stable states
- *Active opening capability*: the transition from the on-state to the off-state is done by actively separating the contacts by electrostatic actuation. The contact force is created passively by the deflected interlocked hooks, and the opening force (2mN) is created actively by applying the actuation voltage for disconnecting the cantilevers.
- *Very low intrusive RF design*: the switch actuation mechanism is completely placed inside the signal line of the coplanar waveguide transmission line
- *Single photolithography step fabrication*: together with the 3-D transmission lines using bulk micromachining deep reactive ion etching, comprising very simple fabrication by a minimum number of standard fabrication steps.
- *Monocrystalline silicon*: used as structural material for all moving parts, providing best possible mechanical reliability
- *Temperature compensation*: the symmetrical Au-Si-Au metallization of the silicon cantilevers eliminates susceptibility to changes in the operation temperature
- *All-metal switch actuators* with stoppers for avoiding short-circuit between the switch elements, providing robust actuation and stable actuation voltages (no charging on the electrodes)
- *3-D micromachined coplanar waveguide*: providing low dielectric substrate losses and low ohmic losses.

Comparing with commercial SPDT (Table 1-3) the RF performance is similar to RadantMEMS and better than OMRON. Specifically, IL and RL better than 1.2dB and 15dB respectively are achieved from DC to 25GHz. Isolation is better than 10dB in the entire band. From reliability point of view, RadantMEMS has better performance considering hot-switching.

This solution is a prototype that demonstrates how the research fabrication process can face up the RF-MEMS reliability problems. However, the facts that it is not packaged and that the repeatability cannot be assured remain the weak point of this device for a future commercialization.

		RMSW220HP RadantMEMS	2SMES-01 OMRON	[43] MST (KTH)
Working band		DC-40GHz	DC-12GHz	DC-25GHz
RL	@8GHz	25dB	10dB	25dB
	@20GHz	18dB		20dB
IL	@8GHz	0.36dB	1dB	0.6dB
	@20GHz	0.5dB		1dB
Isolation	@8GHz	32dB	30dB	25dB
	@20GHz	17dB		15dB
Millions of cycles		1000	100	>150

Table 1-3: Comparison of RF performance between commercial and [43]

Tuneable matching network in mobile phones

WiSpry was founded by Jeff Hilbert in 2002 and it is placed in Irvine (USA). They design and sell RF semiconductor components for the wireless market. The key to WiSpry's technology is the integration of patented RF-MEMS devices with industry standard RF-CMOS process flows, thereby enabling convergence of digital, analog, and RF functionality on a single chip.

After years of development, RF-MEMS have reached the market through a tuneable matching network based on Wispry's devices. It is the first known use of such a part in a volume-shipping product (Samsung smartphone). The interest of this development came out when users start to report problems with signal reception with the iPhone 4 after they held the device in certain ways. The input impedance of the antenna changed depending on the position and the distance with the ear. Apple answered their customers giving them a cover for the phone.

The tunable impedance match (TIM WS2017) device consists of a network of inductors combined with WiSpry's CMOS-integrated, digitally tunable and low-loss MEMS capacitors [44]. The WiSpry single-chip design integrates logic circuits/serial interface for control, on-board high-voltage charge pump and high-voltage MEMS drivers, together with fully encapsulated digital MEMS capacitors on a single chip Fig. 1-24.

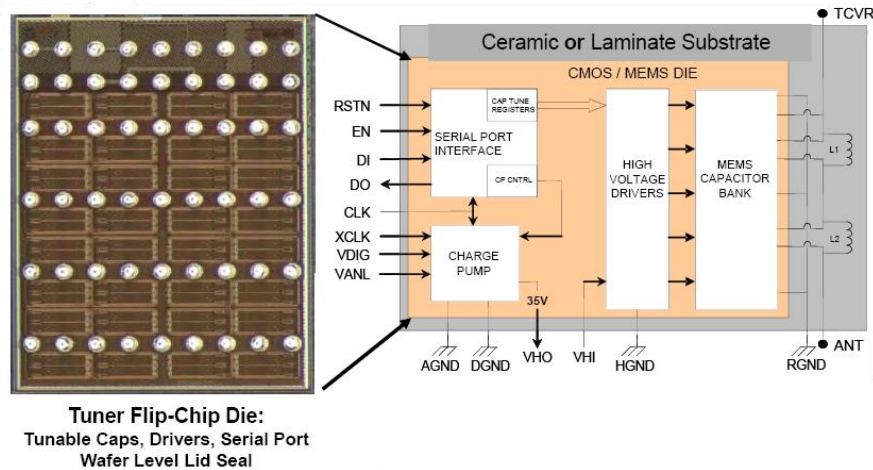


Fig. 1-24: Schematic of the TIM developed by Wispry

The WS2017 can be quickly re-configured to compensate for antenna source impedance changes due to frequency band and different external load to cover hand, head and body effects. Using a serial control interface, the WS2017's high-Q circuits transform mismatched and varying antenna impedances from being poorly matched to well-matched. The result is an improved RF performance and greater energy efficiency. The antenna impedance match is digitally controlled by the programmable capacitive elements (0.125pF steps) implemented in WiSpry's CMOS-RF MEMS structure. The WS2017 features an integrated high voltage charge pump for electrostatic actuation and bi-directional SPI serial control bus. The charge pump, serial bus and driver circuits are all fully integrated on the same CMOS die as the MEMS capacitor elements.

The digital control of the MEMS capacitor, as it was presented in section 1.1.2 (Reliability during working state), is possible thanks to the co-integration CMOS-MEMS (Fig. 1-25). This is the main advantage of this design. It is known how the capacitance value will evolve and the digital control can compensate these deviations as was proposed in [20]. Moreover, the use of symmetric serpentine arms reduces the stiffness of the membrane and increases the temperature tolerance of the device (Fig. 1-25). The membrane is also made of a stress compensated tri-layer patented stack to increase reliability.

In [45] it was shown that long term cycling tests have demonstrated up to $1.9 \cdot 10^9$ cycles (unipolar 35V square wave 50% duty cycle). Hold down tests showed no evidence of failure after three days. The devices were hermetically packaged giving the wafers a soak of moisture at 121°C, 2 atm of pressure and 100% of relative humidity.

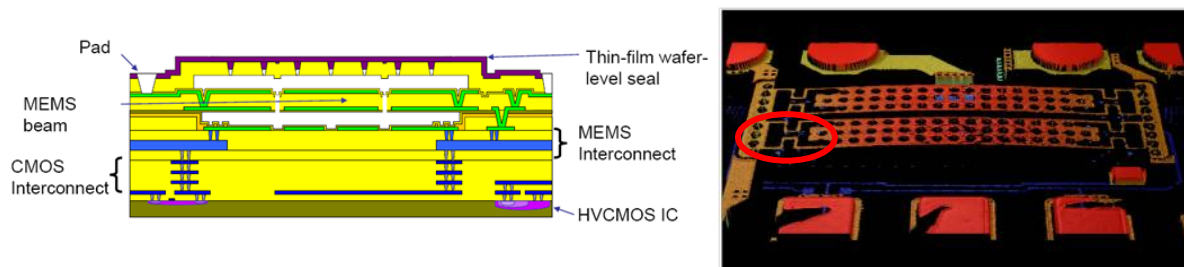


Fig. 1-25: Wispry MEMS based variable capacitor (right) with the serpentine arms for stress compensation and reduced stiffness. Cross-section of the used process for the co-integration (left)

1.4 Conclusions

This chapter has presented an overview of the different reliability issues and the most relevant approaches to deal with them. The attention has been driven on three main failure mechanisms such as dielectric charging, contact degradation and thermal induced phenomena and on how the design can be performed to alleviate their effects and to improve the lifetime. A special emphasis has been given to the role of fabrication processes performed on research platforms or industrial production lines with respect to yield and repeatability.

Dielectric charging is an unavoidable effect that can only be controlled decreasing the effect of the electric field between the electrode and the membrane. For this reason some techniques are developed to avoid the contact (stoppers and proximity switches) and new materials with very short discharging constant (UNCD). Despite these solutions there is also the charging on the substrate which means that a perfect knowledge of the charging/discharging of the different parts is a must in electrostatically actuated RF-MEMS devices. This study can allow the design of control circuits to compensate the possible deviations.

Contact degradation problem is normally solved through the choice of a material that achieves a good compromise between hardness and contact resistance. Materials like Ruthenium, Platinum and Gold-alloys are the most common ones not only for meeting this trade-off but also for its easy integration in standard fabrication processes. In all these cases, a hermetic packaging that avoids the contamination of the contacts is needed. As an alternative, the interlocked hook solution demonstrated by [43] is an example of avoiding it by assuring permanent contact without degradation since any force is applied after actuation for maintaining the state.

The simplest way to make RF-MEMS tolerant to temperature variation is by geometrical modifications of the membranes. The introduction of corrugated membrane or opposite-side anchors allows the stress compensation which leads to higher thermal tolerance. This technique is simpler than the sandwiched membranes which also achieves this goal. This thermal budget needs to be carefully considered since it will impact and determine the operational range and the device lifetime.

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Chapter 2

RF-MEMS in low TRL environment

2.1 Introduction

This chapter describes the different fabrication process developed at LAAS-CNRS for resistive and capacitive RF-MEMS devices. The facilities of this laboratory allow a very high flexibility with a large variety of device topologies and circuit configurations. On the other hand this freedom is paid at the cost of lower process stability and yield. The development of the fabrication process has been the result of several research activities carried out at LAAS in the last 15 years in the field of advance wireless communication systems for defense and aerospace divides in three main axes: device level, circuit level and reliability.

The development of the fabrication process was started by K. Grenier [46] and optimized by C. Villeneuve in Silicon substrates [47] and S. Aouba and P.F. Calmon in Fused Silica substrates. Using this technology, some first devices were designed and optimized for power applications [48] and frequency scalable devices from 20 to 95GHz [49]. More complex circuits such as phase shifters [50] and filters [51] were proposed and, finally above IC integration process was studied [52].

Regarding the characterization of dielectric charging, the study of the charging phenomena in AlN, the electrostatic discharge breakdown and the radiation effect was done in [53]. Moreover, in [54] a new technique based on KPFM (Kelvin probe Force Microscopy) was developed to investigate the charging phenomena. Finally a SiN doped with CNT was developed in order to increase the lifetime of capacitive switches [50]. This deep knowledge of the dielectric charging was used to develop a characterization platform used nowadays by Thales Alenia Space [55].

In terms of characterization of resistive contacts, a deep study of different types of contact material (Au-Au, Ru-Au and Ru-Ru) was done in [56] using nanoindentation techniques. The modeling of this contact, still under study nowadays, was also presented in [57].

This thesis has gone one step forward with respect to the previous work by studying the effects of the fabrication process on the RF performance. This approach was initiated already back in 2010 with the paper on scalable shunt capacitive switch [49] completed later with the series configuration in order to have the complete library available out from the same process. This chapter is organized in two parts: the capacitive and the resistive switches. In both cases, the process steps and the devices are explained showing the strengths and limitations of each solution. Finally, the application of these devices is reported in the development of some basic

circuit module such as phase shifter and routing networks to demonstrate the level of complexity which can be attained.

2.2 Capacitive in LAAS-CNRS fabrication process

2.2.1 Technology and switch description

The used switch is a capacitive series cantilever beam as it is presented in Fig. 2-1. The switch is fabricated in a bi-layer substrate (BCB-Si) on a CPW of $2\mu\text{m}$ of thickness using 300nm Si_3N_4 ($\epsilon_r=7.5$) as a dielectric. It is important to note that the fabrication process allows integrating the monolithic front-end layer with the phase shifter based on this switch and described in 2.2.3 (Above-IC process).

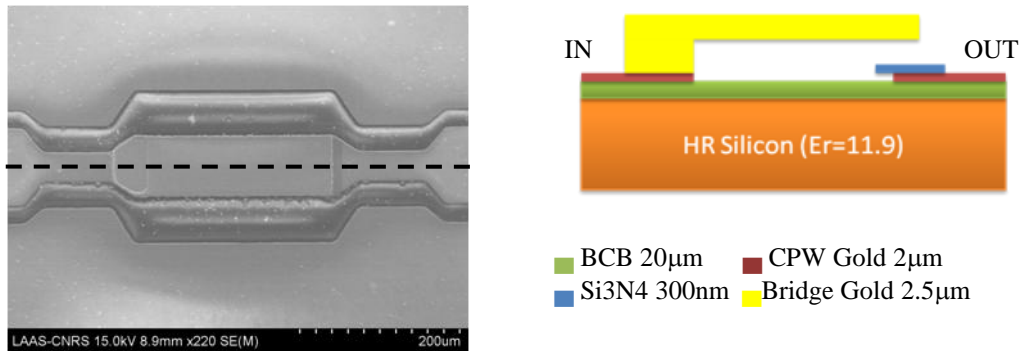


Fig. 2-1: SEM image (left) and cross section (right) of the capacitive switch

The fabrication process flow of RF-MEMS capacitance microswitches has 7 steps [58]:

- 1) Each process begins with a cleaning step to remove the chemical oxide.
- 2) On the clean silicon substrate, a $20\text{-}\mu\text{m}$ -thick benzocyclobutene (BCB) layer is deposited.
- 3) Coplanar waveguide (CPW) fabrication: a Ti/Au bi-layer is evaporated serving as seed layer for a $2.5\text{-}\mu\text{m}$ -thick electroplating gold layer grown in a photoresist mould created previously. The seed layer is then chemical etched between lines.
- 4) A 100-nm -thick Ti layer is evaporated on the Au CPW and a 250-nm -thick Si N layer is deposited by plasma-enhanced chemical vapor deposition (PECVD). These layers are patterned using photolithography, reactive ion etching (RIE), and wet etching.
- 5) Two steps of planarization: a $2.5\text{-}\mu\text{m}$ -thick photoresist layer is spin coated, pre-baked, and after photolithography, hard baked. The same steps are used for gap filling and the sacrificial layer [47].
- 6) Over this sacrificial layer, a 100-nm -thick Au layer is evaporated and $1.9\text{-}\mu\text{m}$ -thick Au is electroplated. This bi-layer, which forms the bridge over the CPW, is patterned with photolithography and chemical etching.
- 7) The final step consists of releasing the switches. The sacrificial layer is removed using successive chemical baths. Finally, the MEMS is dried by supercritical point drier.

Both coplanar accesses are $20/100/20\mu\text{m}$ (G/W/G) in order to achieve 50Ω ohms. Moreover, an inductive section is inserted in order to improve the input matching of the switch in down state. The dielectric surface is $20 \times 80\mu\text{m}$ which is designed to achieve 40GHz as working frequency taking into account surface roughness and dielectric thickness deviation. The total surface area of the switch is $800 \times 600\mu\text{m}$.

Electromechanical simulations were run in CoventorWare in order to infer the pull-in voltage and the result was 45V. The switch is driven applying 40% more voltage than simulated (65V) between the transmission line and the bridge resulting in a measured C_{on}/C_{off} ratio of approximately 17 (100fF/6fF) in the initial state.

The device was cycled during 14000 cycles at bipolar actuation at 65V under nitrogen (1 atm) at 297K. It has been seen (Fig. 2-2) that after the second actuation the device do not recover the initial position and the UP state capacitance is 30fF instead of 6fF. This effect is due to the dielectric charging phenomena (displacement of C(V) curve) and also to the low stiffness of the cantilever that will be solved in next section 2.2.2 with the anchor reinforcements.

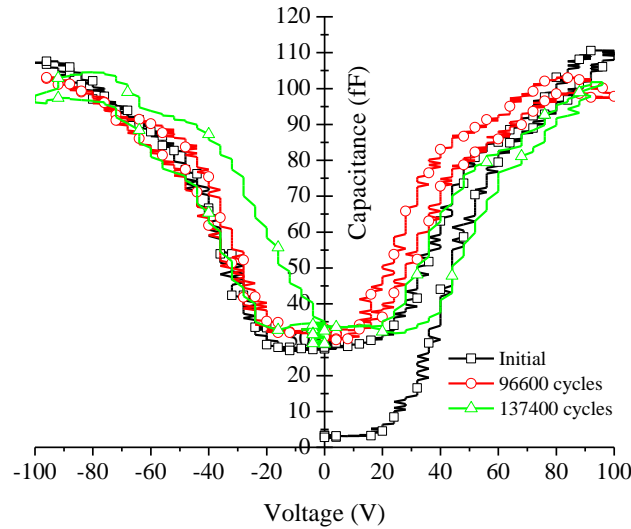


Fig. 2-2: C(V) characteristic of the cantilever at initial state (square) and after stress (triangle)

In Fig. 2-3 the measured S-Parameters of the switch and its dispersion over the wafer are presented. The aim of these results is to give an idea about the differences in terms of RF performance depending on the location on the wafer. It is shown that input matching which is 20 ± 2.4 dB at 40GHz while insertion losses are 0.17 ± 0.02 dB when the switch is actuated at 55V. In the OFF state position, isolation reaches 12 ± 3 dB at 40GHz. The larger deviation in correspondence of 60GHz can be attributed not to the DUT but to the systematic measurement error (mixer switching frequency).

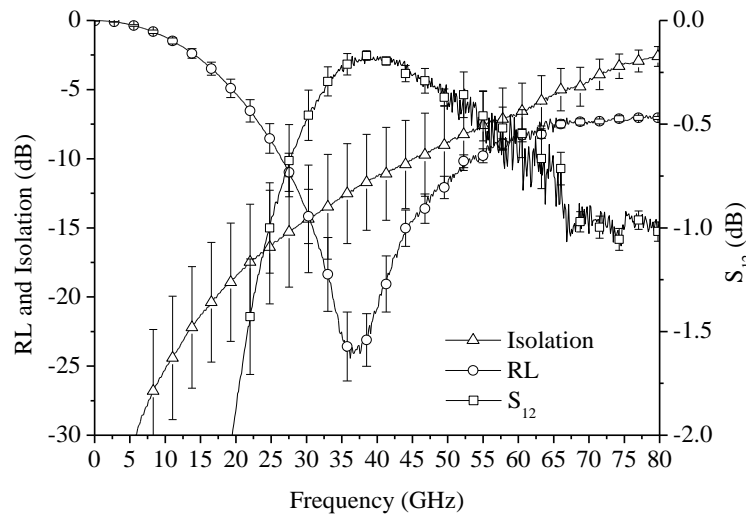


Fig. 2-3: RF performance of 10 devices and its deviation over the wafer

2.2.2 Impact of fabrication process

Contact capacitance deviation

The direct consequence of the dispersion of the DOWN state capacitance (C_{DOWN}) of capacitive switches is the deviation of the resonance frequency f_0 :

$$f_0 = \frac{1}{2\pi\sqrt{LC_{DOWN}}} \quad \text{Eq. 2-1}$$

Since in first approximation the inductance value L depends on the shape of the cantilever, its value is fixed for both states [58]. This deviation from the theoretic value is due to the roughness of the dielectric and the deflection of the cantilever caused by the stress of the bi-metallic layer [47].

In Fig. 2-4 the comparison between the simulated model (considering perfect contact and flat cantilever) and the measurements of the device presented in section 2.2.1 is shown. Applying Eq. 2-1 to the ratio between the measured and simulated working frequency (f_0^{sim} and f_0^{meas}) and the parallel plate formula of the capacitance, it is demonstrated that the contact surface is 2.6 times smaller than expected (Eq. 2-2).

$$\frac{f_0^{meas}}{f_0^{sim}} = \frac{36.6\text{GHz}}{22.5\text{GHz}} = \sqrt{\frac{C_{DOWN}^{sim}}{C_{DOWN}^{meas}}} = \sqrt{\frac{A_{DOWN}^{sim}}{A_{DOWN}^{meas}}} \rightarrow \frac{A_{DOWN}^{meas}}{A_{DOWN}^{sim}} = 0.38 \equiv 61\% \quad \text{Eq.2-2}$$

where A_{DOWN}^{sim} and A_{DOWN}^{meas} are the contact area in simulation and measurements respectively and C_{DOWN}^{sim} and C_{DOWN}^{meas} are the DOWN capacitance in simulation and measurements respectively.

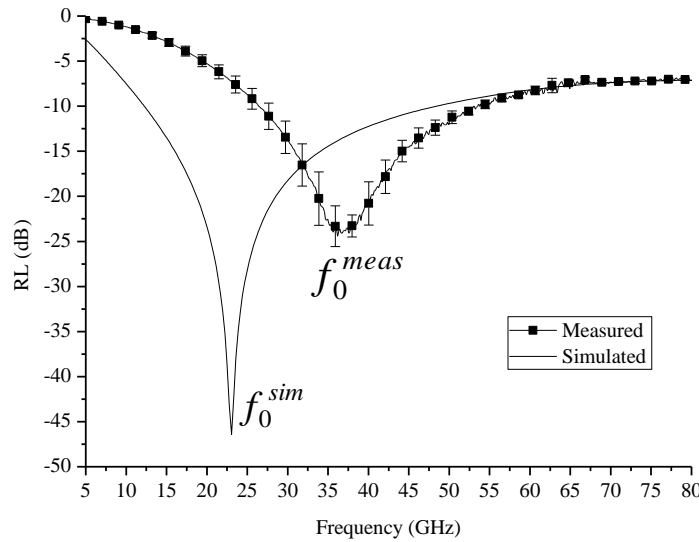


Fig. 2-4: Comparison of the RL of the switch between the model and measurements

The parameter which causes this variation is mainly the roughness of the contact dielectric which is estimated (from previous developments in the same platform) to be responsible of the 50% variation of the area. Despite being a very large dispersion, this fabrication parameter can be controlled and estimated. This means that the designer can use the data for improving the simulation model [47]. Noteworthy is that 11% of variation is due to the deflection of the cantilever, caused by the stress on the cantilever which will be studied in the following section.

Improving the contact capacitance (3rd metal layer development)

The bi-layer cantilever presented in Fig. 2-1 is formed with the same material (Gold) but subjected to different initial stresses due to its different thicknesses and deposition techniques. The out of plane deflection at the end of the cantilever (δ_{\max}) is defined by [60].

$$\delta_{\max} = \frac{3t_1t_2}{(t_1 + t_2)^3} \frac{\sigma_1 - \sigma_2}{E} L^2 \quad \text{Eq. 2-3}$$

where t_i is the thickness of each layer, σ_i is the uni-axial initial stress, L the total length and E the Young's Modulus of the beam (Fig. 2-5). The initial stress and Young's Modulus were measured in [60]. The deflection along the beam is a quadratic equation (Fig. 2-5) whose linear term is related with the anchor rotation (θ) and mean stress (σ_m). The quadratic term is due to the gradient stress (17MPa/ μm in this bi-layer beam).

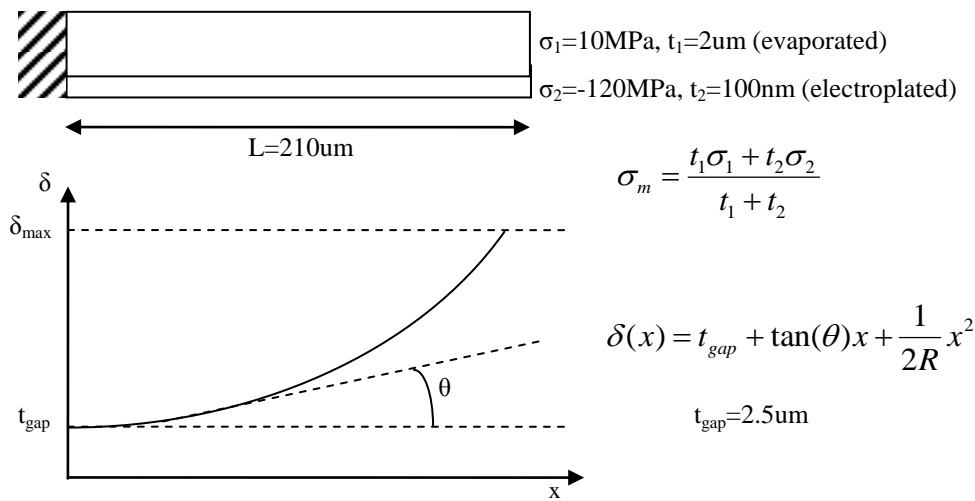


Fig. 2-5: Cross section (top) and deflection (bottom) of the bi-layer cantilever

It is well known that thermal treatment can relax stresses in metallic beams. In LAAS-CNRS fabrication process, this step is done using a low temperature annealing before the realising [58]. The mean stress of electroplated gold is constant with temperature but, for evaporated gold it is not the case. The mean stress can pass from compressive to tensile (negative to positive) finding a zero-stress point at a determinate temperature. This is the method used to eliminate the quadratic term of the deflection equation.

After the optimized annealing, the capacitance variation seen in previous section is only affected by the anchor rotation. This is solved by using reinforcements in the anchor and adding some metallic structures on the point of maximum deflection (δ_{\max}) of the cantilever. The reinforcements on the anchors will not only reduce the anchor rotation but also increase the stiffness of the beam thus decrease the mechanical fatigue. On the other hand, the metallic structures will also reduce the deflection in Y-axis making the down state capacitance higher (flatten cantilever in the contact region).

Due to fabrication process restrictions, the metallic structures are only possible in wide cantilevers. Moreover, it is assumed that the wider the beam the higher deflection in Y-axis and, for the proposed cantilever design of section 2.2.1, the Y-axis deflection is very low. In Fig. 2-6 the different studied anchor reinforcements and metallic structures are shown.

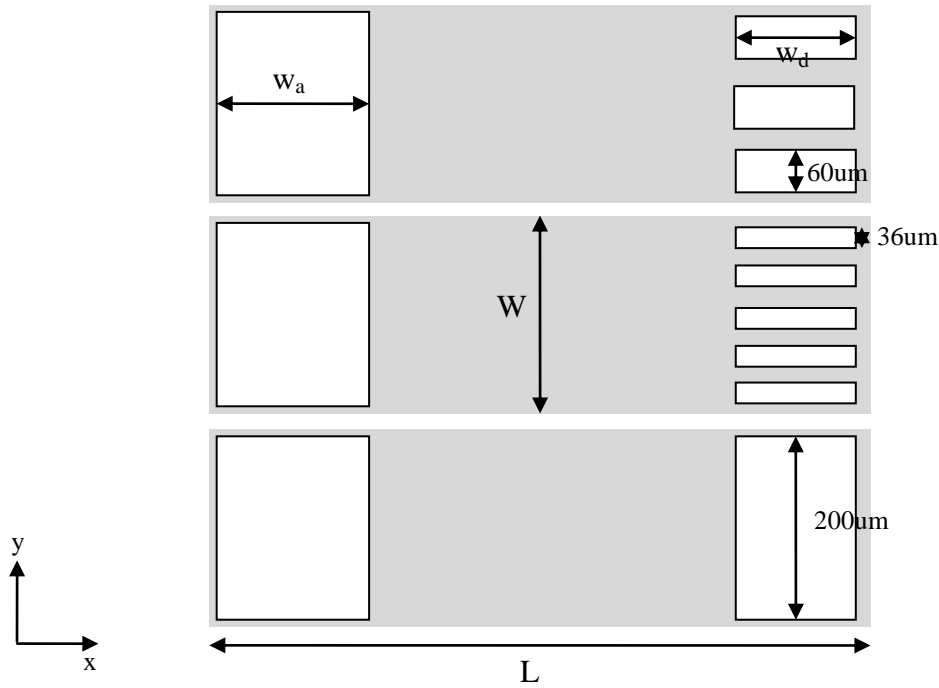


Fig. 2-6: Anchor reinforcements ($w_a=90, 100$ and $120\mu\text{m}$) and types of metallic structures ($w_d=0.25*L, 0.4*L$ and $0.5*L$) for $W=200, 100$ and $70\mu\text{m}$ and $L=500\mu\text{m}$.

In Table 2-1 the maximum deflection of the membrane in X-axe for each of the proposed reinforcements is depicted. For these wide membranes, the anchor reinforcements do not improve the deflection while the reinforcements at the edge do. The optimal structure at the edge is one single bloc of the same width ($W=200\mu\text{m}$) and the half of the length of the cantilever ($0.5*L$). This gives a distance of $3.5\mu\text{m}$ between cantilever and dielectric, only $1\mu\text{m}$ higher than a flat membrane.

For $W=100\mu\text{m}$ and $W=70\mu\text{m}$ an anchor reinforcement of $w_a=120\mu\text{m}$ gives the maximum planarity of the cantilever. In the case of $W=100\mu\text{m}$ the improvement is of $3\mu\text{m}$ while in $W=70\mu\text{m}$ it is $1.6\mu\text{m}$ (Table 2-1).

W	Size of the anchor reinforcement (w_a)		
	$90\mu\text{m}$	$100\mu\text{m}$	$120\mu\text{m}$
200μm	6.1	6	6
100μm	10	7.4	7.1
70μm	7.8	6.3	6.2
Number of structures at the edge ($W=200\mu\text{m}$)	Size of the reinforcements at the edge of the cantilever (w_d)		
	$0.25*L$	$0.4*L$	$0.5*L$
1	7.4	6.8	5.3
3	10.2	7.1	7.1
5	6.3	6.6	6.3

Table 2-1: Maximum deflection of the cantilever (μm) for all the proposed reinforcement structures

The profilometer measurements have shown no deflection in Y-axis in all the proposed structures. The different annealing techniques explained above have compensated this deflection.

2.2.3 Applications in routing circuits

SP4T and phase shifters with capacitive switches

This section presents a narrow band (from 35 to 55GHz) SP4T. The targeted application for this key component is antenna beam-forming, reconfigurable routing circuits and phase shifting in space applications at Q-Band (~ 40 GHz). Using 4 capacitive switches like the ones presented in section 2.2.1 a SP4T is proposed. A microscope image of this design is shown in Fig. 2-7. The following relevant issues have been taken into account in the design:

1. The 1 to 4 junction shape: round corners and airbridges are implemented for optimal input matching and lack of radiation respectively.
2. The distance between the junction and the switch: the distance is minimized in order to avoid that open-ended stubs (not actuated switches) could affect the input matching.
3. The outputs OUT 2 and OUT 3: since the size of the circuit does not allow the use of two single RF-probes one next to the other, two of them are designed such to be measured by means of a differential RF-probe with 100 μ m pitch.

The device is characterized using 3 Single (GSG) (IN, OUT 1 and OUT 4) and 1 differential (GSGSG) (OUT 2 and 3) RF probes at 65GHz. As the device is symmetric, only two paths are measured: the central and the lateral. In order to do this, the non-actuated paths are ended with 50Ohms loads. A small scheme of the set-up used for a lateral path can be seen in Figure 4.

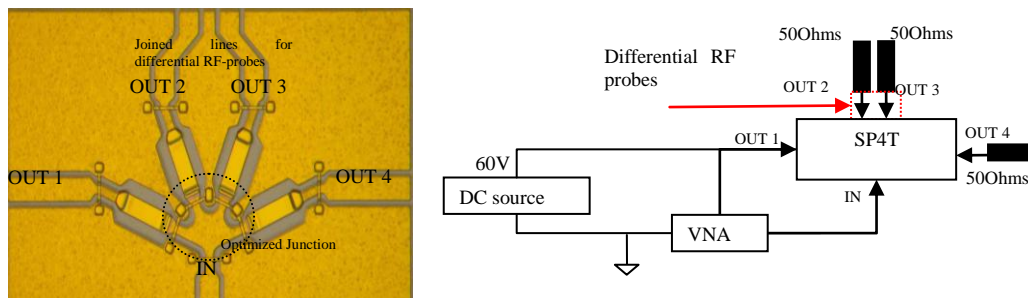


Fig. 2-7: Microscope picture (left) and set-up (right) of the SP4T

Measurement is performed from DC to 67GHz. Two different Thru-Reflect-Line calibrations have been done depending on the measured path. The switches are actuated with a DC supply through the RF-probes using T-polarization blocks in the VNA's outputs. The activation is done by providing 65V at the output of the SP4T and connecting the input with the ground.

In Fig. 2-8, measured and simulated S-Parameters of the lateral (IN to OUT 1) and central (IN to OUT2) are plotted. In terms of input matching 11 ± 1.3 dB at 40GHz is achieved. This limitation originates from the design but it can be addressed for future applications using impedance matching structures. On the other hand, very good performance is seen in insertion loss at the same frequency (0.6 ± 0.13 dB).

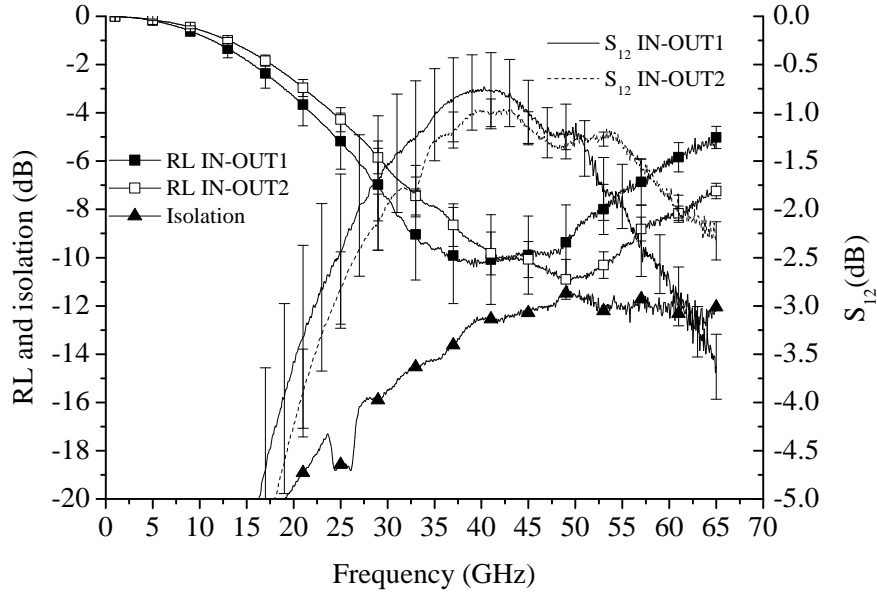


Fig. 2-8: RF performance of the SP4T in both cases: lateral (IN to OUT1) and central (IN to OUT2)

The presented SP4T is suitable for phase shifting applications. The first step is to define the different phase shift that should be implemented and this will depend on the application. In Fig. 2-9, a general block diagram of the structure of the switch is shown.

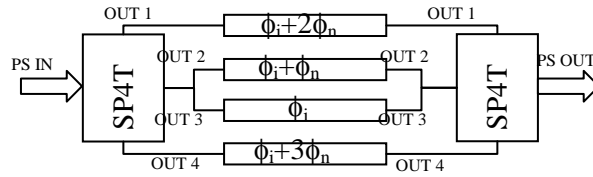


Fig. 2-9: General Schema of a 2-bit phase shifter using switched-lines

This configuration allows improving the input matching of the phase shifter with respect to the one in the SP4T by means of the characteristic impedance of the delay lines. On the other hand, insertion loss of are at least doubled since two SP4T are used in series.

Depending on the resolution of the phase desired, the length of every line is computed. This resolution will define the number of 2-bit phase shifter that will be needed to cover the whole phase range (from 0 to 360°). For example, for a resolution of 5.625°, three cascaded 2-bit phase shifters are needed (0/90/180/270, 0/22.5/45/67.5 and 0/5.625/11.25/17) which will compose a 6-bit phase shifter. These three blocks will imply the need of six series SP4T so the losses will rapidly increase. Using the SP4T presented above, some simulations in ADS taking into account the measured parameters are performed in order to demonstrate the applicability of the switching node. The lengths of the lines are computed using Eq. 2-4.

$$l_n = \frac{n\phi_r\lambda}{4\pi} \quad \text{when } n = 0..3 \text{ and } \phi_r = 5.625^\circ \quad \text{Eq. 2-4}$$

In order to achieve better return losses in all the paths, the delay lines are optimized in terms of characteristic impedance. The central lines (0 and 5.625°) are designed at 40Ohms and the lateral ones (11.25° and 17°) have 25Ohms of characteristic impedance. In the presented simulations in Fig. 2-10, the line loss (conductor and substrate by means of ADS/Momentum simulator) is also taken into account. It can be seen that insertion loss is better than 1dB and input matching is better than 25dB in the different paths. These low losses comparing with the

SP4T are due to the better input matching reached by means of optimization of the delay line characteristic impedance optimization.

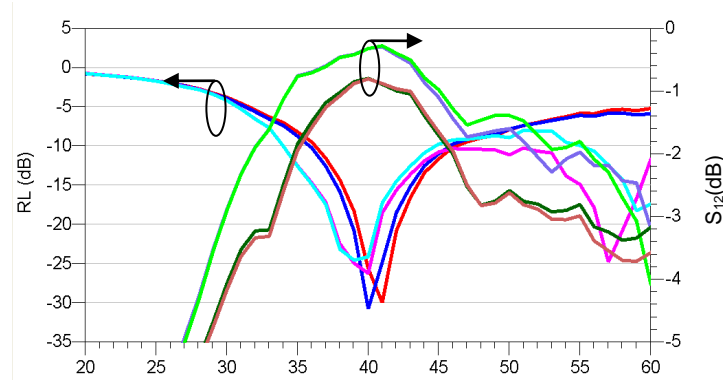


Fig. 2-10: Results of the simulation of a 2-bit phase shifter with a resolution of 5.625deg. The curves with lower losses (green and purple) correspond to the shorter delay lines.

Taking into account the deviation of the S-parameters in the SP4T presented above, a worst-case analysis can be done. This study tries to demonstrate that in the worst case scenario, the performance of the phase shifter remains acceptable. In Table 2-2 the results of the simulation for different number of cascaded 2-bit phase shifter (1, 2 or 3) are shown including the worst case scenario for each design.

	Bits	Mean	Worst case		Best case	
			IL	Shift path	IL	Shift path
	2	0.56dB	0.8dB	$\phi_i + \phi_n$	0.32dB	$\phi_i + 2\phi_n$
	4	1.12dB	1.6dB	$2(\phi_i + \phi_n)$	0.64dB	$2(\phi_i + 2\phi_n)$
	6	1.22dB	2.3dB	$3(\phi_i + \phi_n)$	0.96dB	$3(\phi_i + 2\phi_n)$

Table 2-2: Simulated insertion losses for different number of cascaded 2-bit phase shifter

2.3 Resistive switches in LAAS-CNRS fabrication process

2.3.1 Technology and switch description

The proposed switch is a wide band (DC-65GHz) series resistive cantilever switch on a Fused Silica substrate ($\epsilon_r=3.8$ and $t=500\mu\text{m}$) as shown in Fig. 2-11. The CPW is 13/80/13 μm (G/W/G) achieving 50Ohms of characteristic impedance. The use of Si_3N_4 over the CPW line allows both resistive and capacitive switches in the same wafer. However, this section is focused on resistive contact switches.

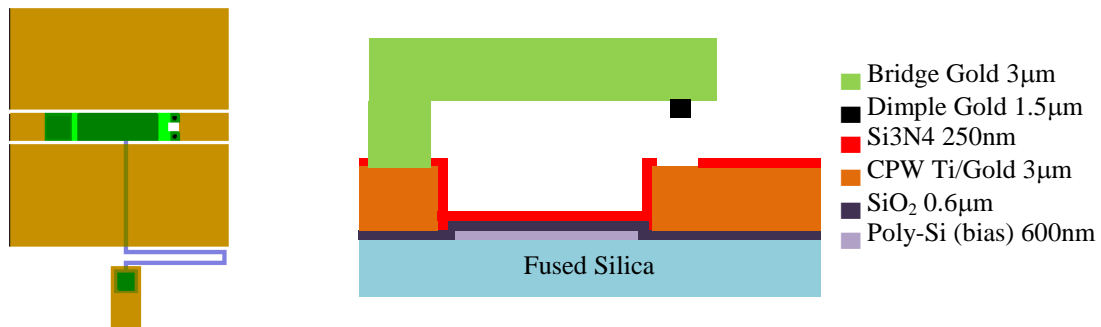


Fig. 2-11: Layout (left) and cross section (right) of the series resistive switch

The fabrication process flow of the cantilever based RF-MEMS switches has 10 steps using 9 masks. The steps in bold are done only for resistive switches in such a way that capacitive and resistive switches can be implemented in the same wafer or circuit:

- 1) Wafer cleaning of the 4 inches wafer (100 orientation and double side polished)
- 2) Deposition and etch of Polysilicon for electrodes, actuations pads and contact pads in both sides of the wafer (the layer is completely removed on the back side). The resistivity of the Polysilicon is $4.5\text{m}\Omega\cdot\text{cm}$ and the stress is -300MPa .
- 3) Deposition of SiO_2 (PECVD) over the entire wafer for electrode and lines isolation. Etching is done only in the DC-pad contact
- 4) CPW circuit (Ti/Gold deposition and seed layer etching):
 - a. Evaporated seed layer : Ti / Au
 - i. Ti : thickness : $0.05\text{ }\mu\text{m}$, stress : 150 MPa
 - ii. Au : thickness : $0.2\text{ }\mu\text{m}$, stress : 100 MPa , resistivity : $2.5\text{ }\mu\Omega\cdot\text{cm}$, roughness: 2 nm
 - b. Electroplated gold on photoresist mould: thickness: $2.5\text{ }\mu\text{m}$, stress: 10 MPa , resistivity: $3\text{ }\mu\Omega\cdot\text{cm}$, roughness: 6 nm
 - c. Evaporated seed layer : Ti: thickness: $0.05\text{ }\mu\text{m}$, stress : 150 MPa
 - d. Etching of metallic layers in CPW gap
- 5) Dielectric openings
 - a. PECVD SiN_x ($T = 200^\circ\text{C}$): thickness : $0.250\text{ }\mu\text{m}$, permittivity : 6.5
 - b. Etching by RIE
 - c. Ti etching (bridge anchor on gold)
 - d. Contact area (only for resistive switches)**
- 6) Stand alone MIM capacitor (if needed for the circuit design)
 - a. Metallic layer by lift off
 - i. Ti: thickness: $0.05\text{ }\mu\text{m}$, stress: 150 MPa
 - ii. Au: thickness: $0.2\text{ }\mu\text{m}$, stress: 100 MPa , resistivity: $2.5\text{ }\mu\Omega\cdot\text{cm}$, roughness: 2 nm
- 7) Sacrificial layer patterning
 - a. Planarization of CPW lines under bridge /cantilever. Resist thickness: $2.5\text{ }\mu\text{m}$
 - b. Sacrificial layer deposition. Resist thickness: $2.6\text{ }\mu\text{m}$
 - c. Full resist exposure for bridge anchor
 - d. When required partial resist exposure defining dimple area (only for resistive switches)**
 - e. Development of the sacrificial layer for the anchorage opening and the bump recess realization
- 8) Cantilever deposition and patterning
 - a. Evaporated gold: thickness: $0.05\text{ }\mu\text{m}$, Stress $\cong -30\text{ MPa}$ (-70 to 0 MPa)
 - b. Electroplated gold: thickness : 1 to $3\text{ }\mu\text{m}$, Stress : 5 to 10 MPa
 - c. Etching in KI/I_2 bath
- 9) Dicing
- 10) Release of structures (resistive dissolution) and CO_2 drying (48h)

In Fig. 2-12 the RF performance of the device is shown. Return Losses and Isolation better than 15dB from DC to 65GHz are achieved. Insertion losses are better than 1.4dB in the entire band. In this case very few devices (2 over 12) are working under expected performance due to a mechanical problem which will be studied in next section 2.3.2.

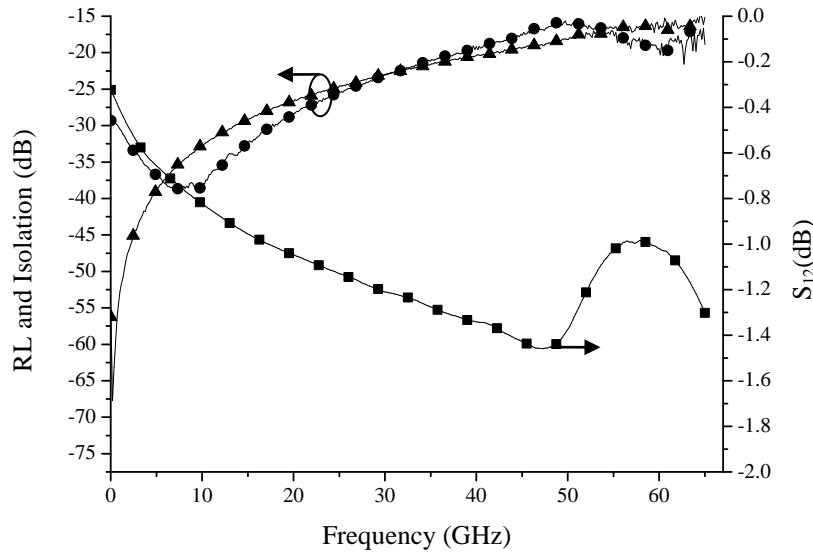


Fig. 2-12: Isolation (triangle) at 0V and Return Losses (circle) and S_{12} (square) at 90V of the fabricated resistive switch

Equivalent circuit for mechanical behaviour description

The two important parameters in resistive switches are the UP state capacitance (C_{UP}) and the contact capacitance (R_{ON}). The proposed method to extract them is the lumped-elements based equivalent circuit which consists of a transmission line (50 Ohms) in series with either a capacitance (UP state) or a resistor (DOWN state) Fig. 2-13. Literature [58] proposes also to model the cantilever using an inductor. In this case, as the width and shape of the cantilever is the same as the transmission line, this step is omitted.

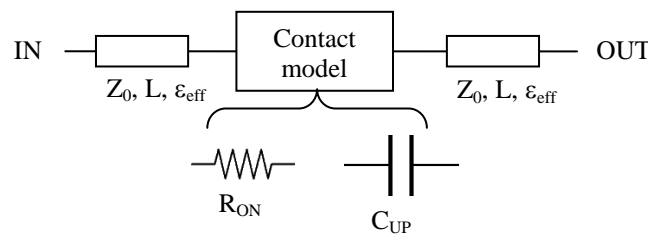


Fig. 2-13: Schematic view and electrical equivalent circuit model of the series resistive switch

The model of the line is extracted from the measurements of a line without cantilever. This method allows separating the substrate and conductor losses from the switch losses. The parameters of the line Z_0 and ϵ_{eff} are tuned using its theoretical value⁷. In Fig. 2-14 the comparison between the line model and the measurements is presented showing very good agreement⁸.

⁷ Theoretical ϵ_{eff} for CPW lines is computed as $\epsilon_{eff} \cong \frac{\epsilon_r + 1}{2}$ where $\epsilon_r=3.8$. Characteristic impedance (Z_0)

depends on G/W/G dimensions (13/50/13 in this case) and the theoretical value is computed using LineCalc (ADS).

⁸ Losses for $f > 20$ GHz are positive due to a calibration problem. However, the positive deviation is very small and it is ignored.

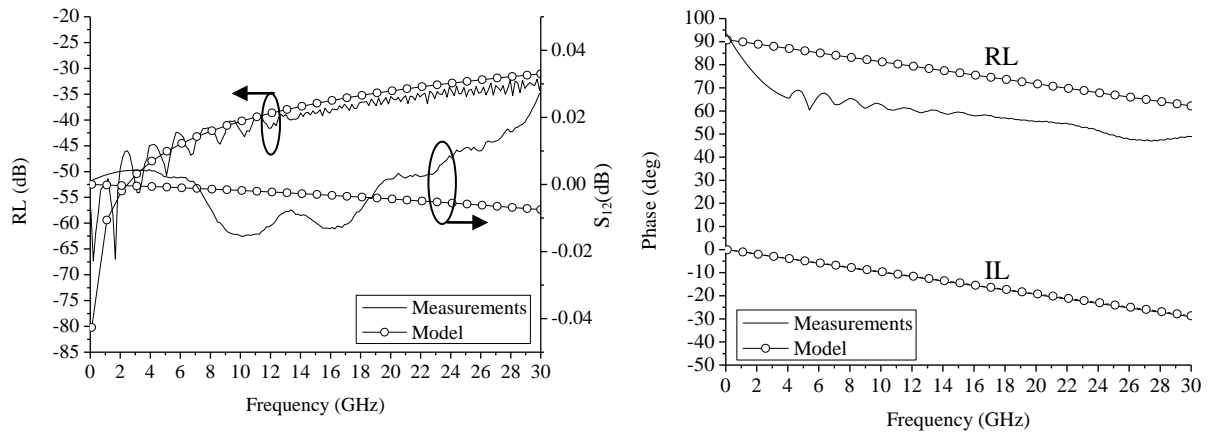


Fig. 2-14: Comparison of magnitude (left) and phase (right) between model (circle) and measurements (line) of the transmission line.

Adding the contact model proposed in Fig. 2-13, the RF performance of the model fits very well with measurements Fig. 2-15. In the case of the UP state the deviation of isolation between measured devices is also shown which is not the case in DOWN state since very few devices were working properly (mechanical problem that will be described in 2.3.2). C_{UP} is $4.75 \pm 1 \text{ fF}$ while R_{ON} is 3.76Ω .

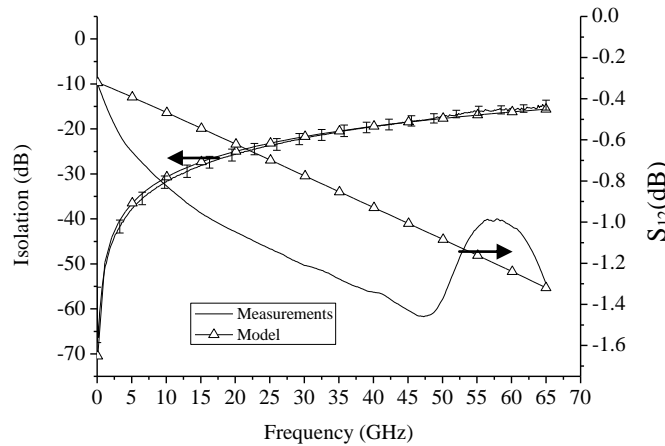


Fig. 2-15: Comparison between model (triangle) and measurements (line) of the RF performance in UP (Isolation) and DOWN (S_{12}) state

2.3.2 Impact of fabrication process

Stress gradient effect on resistive contacts

As it was described in section 2.2.2, the bi-layer cantilever suffers from a high gradient stress which leads to an initial deformation which increases the gap. In this case the maximum initial deformation⁹ is $5.25 \mu\text{m}$ (Fig. 2-16) which is approximately the double of the theoretical¹⁰ gap ($1.1 \mu\text{m}$).

⁹ The measured value is $9.76 \mu\text{m}$ which includes the thickness of the cantilever ($3 \mu\text{m}$) and the size of the dimple ($1.5 \mu\text{m}$). $5.25 \mu\text{m} = 9.76 \mu\text{m} - 3 \mu\text{m} - 1.5 \mu\text{m}$

¹⁰ The theoretical gap is the difference between the sacrificial layer ($2.6 \mu\text{m}$) and the dimple size ($1.5 \mu\text{m}$)

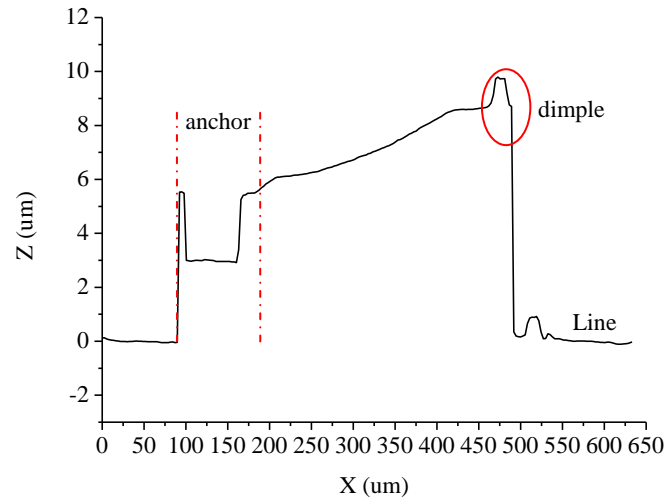


Fig. 2-16: Measured initial deformation (Z) along the cantilever (X) without any actuation (UP state)

The advantage of this deformation is the increase of isolation in UP state. On the other hand, the pull-in voltage increases approximately of 35% from the theoretical value:

$$V_{Pull-in} = \sqrt{\frac{8k}{27\varepsilon_0 W w}} g_0^3 \rightarrow \frac{V_{Pull-in}^{teo}}{V_{Pull-in}^{meas}} = \sqrt{\frac{g_{0teo}^3}{g_{0meas}^3}} \cong 0.73 \quad \text{Eq. 2-5}$$

where g_0 is the gap between the middle of the cantilever and the electrode, k is the spring constant and W and w are the size of the electrode.

The increase of the pull-in voltage is not the only effect of the stressed cantilevers. The other inconvenient is the contact stability of the dimple. This has been verified in the default fabricated devices by inspection of the S_{12} parameter for different actuation voltages (Fig. 2-17). From 0 to 50V no variation is observed in S_{12} , but, a sudden decrease of isolation occurs at 50V followed by a constant value until 65V. For actuation voltages above 75V the improvement of the S_{12} parameter is only of about 0.75dB. Due to restrictions in the set-up the actuation voltage cannot be higher than 90V.

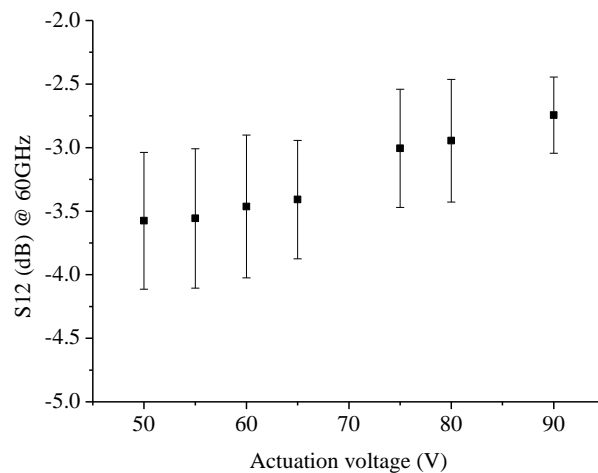


Fig. 2-17: S_{12} at 60GHz for different actuation voltages. The error bars show the dispersion between devices

The mechanical default presented by these switches has a specific signature on the S-parameters. In Fig. 2-18 the transmission parameter (S_{12}) is plotted for the three different regions seen above (0 to 50V, 50 to 75V and above 75V). The correct performance in DOWN state of the switch seen in Fig. 2-15 (resistive behaviour) is not observed at any actuation

voltage. On the contrary a capacitive behaviour is observed which means that the dimple does not contact the line.

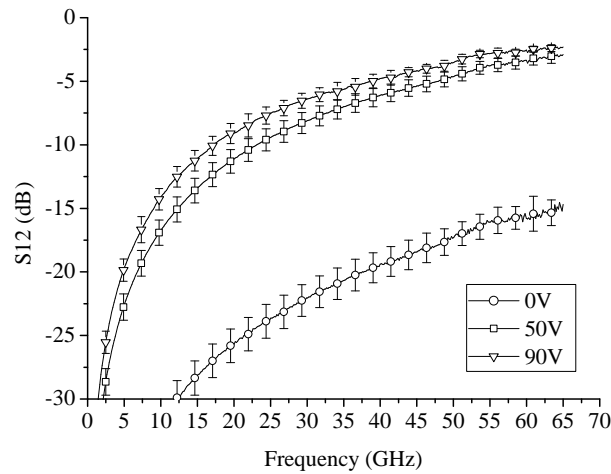


Fig. 2-18: S_{12} for different actuation voltages

Looking in detail what happens when the cantilever is actuated (Fig. 2-19), it was found out that it does not contact the transmission line before the electrode creating a capacitance. The end of the cantilever is so stressed that cannot be gone down.



Fig. 2-19: Schema of the contact between the line and the cantilever in the actuated state. The red arrow show where the electrostatic force is applied

This behaviour is confirmed by the equivalent circuit model presented in previous section 2.3.2 resumed in Table 2-3. The C_{UP} capacitance of the model is varied to match the mean S_{12} parameter at each actuation voltage (Mean C_{UP}). The deviation (ΔC_{UP}) is computed matching the model C_{UP} with the mean plus deviation of the measures S_{12} parameter at each actuation voltage.

V_{act}	Mean C_{UP} (fF)	ΔC_{UP} (fF)
0V	4.75	1
50V	23.86	3.27
55V	24.9	3.27
60V	24.9	3.27
65V	24.9	3.27
75V	31.8	4
80V	32.3	3.8
90V	32.5	2.8

Table 2-3: Capacitance value and deviation extracted from the equivalent circuit

The problem presented by this switch is due to the force on the dimple which is not enough for assuring a good contact. From 50 to 65V a high dispersion on the extracted capacitance and turns out to confirm an unstable contact. This incertitude is reduced when the actuation voltage goes beyond 75V.

Assuring contact stability in resistive switches

Since the electrostatic force is applied in the middle of the cantilever, the increase of the actuation voltage is not the suitable choice to improve the contact stability. This leads to a higher distance between the line and the dimple because the line works as stopper. There are two possible solutions: modify the bias circuit or improve the planarity of the cantilever through the process.

The modification of the bias circuit has the advantage of being very easy to integrate into the design. The fabrication process allows adding actuation pads under the line so a second electrode can be placed after the dimple applying an extra force to the end of the cantilever (Fig. 2-20). Previous developments done in LAAS in R3MEMS project have used similar solutions for capacitive contact [61].

On the other hand, there are two main inconvenient: this solution is very dependent on the cantilever shape (which is not stable over the wafer, see high dispersion in previous section) and the dielectric charging occurs in the extra electrode due to the dielectric that isolates the bias from the line (difference of potential between line and electrode). As the approach of this fabrication process is the high degree of freedom on the design and dielectric charging can occur, this solution is not considered.

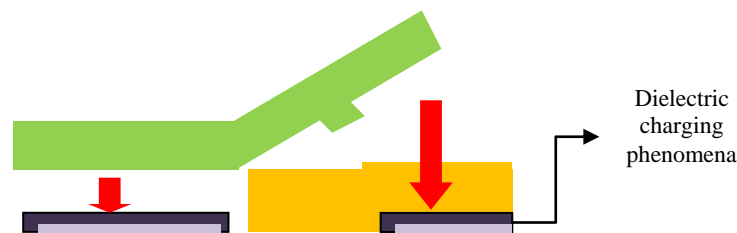


Fig. 2-20: Schema of the solution proposed with an extra electrode

The study option of improving planarity by thermal treatment is the simplest solution. The method of doing it is adding an additional step in the fabrication process before releasing the structures. This step is based on the annealing at a precise temperature and time duration [47]. Temperature and time parameters depend on the length of the structure and can be independently chosen according with the structure type since this operation can be done on diced portion of the wafer before realising.

2.3.3 Applications in routing switches

Very few SPnT have been reported in fused silica substrate. One example is [61] where a SP4T used in a 2-bit phase shifter is proposed. In the case of a SPDT, as mentioned in the introduction, it is used in [63] for a reconfigurable antenna.

The switch presented in section 2.3.1 is applied in two different routing circuits shown in Fig. 2-21. The left one is a SPDT whose outputs are in east (E) and west (W) direction. On the other hand, for the SP4T, a special north output (N1 and N2) should be designed for measurement purposes in order to use a differential RF probe (already mentioned in section 2.2.3).

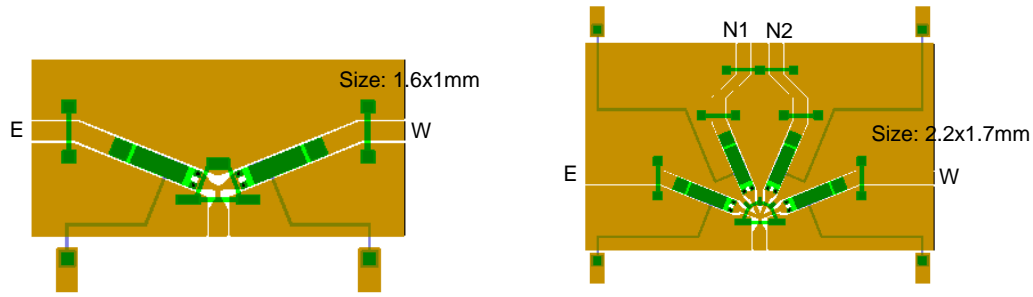


Fig. 2-21: Layout of the SPDT (left) and SP4T (right)

In Fig. 2-22, the simulated performance of the SPDT and SP4T are presented. In the case of the SPDT, input matching and isolation better than 15dB is achieved from DC to 80GHz while losses are over 0.8dB. On the other hand, in the case of SP4T, it is seen similar performance in the different paths. RL better than 15dB and isolation under 20dB is achieved from DC to 60GHz. Insertion losses are better than 1dB in both paths.

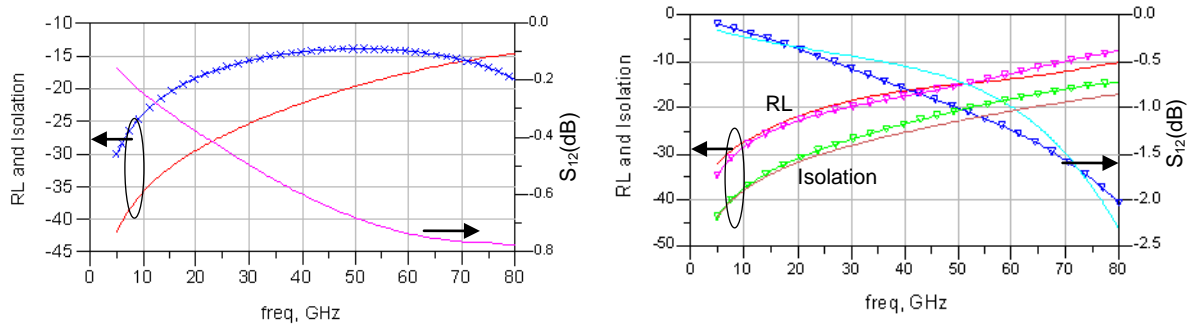


Fig. 2-22: Simulated S-Parameters of SPDT (left: RL(cross), Isolation (line)) and SP4T (right: Lateral path (triangle) and central path (line)).

Comparing the simulations of previous work ([61] and [63] in Table 2-4), it is seen that in the case of the SPDT a larger band is proposed with similar performances in the same range of frequency except on the isolation where [61] uses 2 switches. On the other hand, regarding the SP4T, the expected results are in similar level than [63].

	BW	RL _{min}	IL _{max}	Isolation _{min}
[61] SPDT	18-25GHz	15dB	0.3dB	31.2dB
This work SPDT*	DC-80GHz	17dB	0.4dB	27dB
[63] SP4T	DC-65GHz	18dB	1dB	20dB
This work SP4T	DC-60GHz	15dB	1dB	20dB

*RF performance considered in 18-25GHz

Table 2-4: Comparison of RF performance between this work and state of the art in fused silica based circuits

Using the SP4T presented before, a phase shifter with 22.5° step at 60GHz is designed using switched lines. In future, if the whole range of phases (0-360°) wanted to be covered, the presented phase shifter would be combined with a 4-bit phase shifter with a step of 90°. In Fig. 2-23, a general block diagram of the structure of the phase shifter is shown. This

configuration allows improving the input matching of the SP4T, but, on the other hand, insertion loss of the switching node plays a critical role.

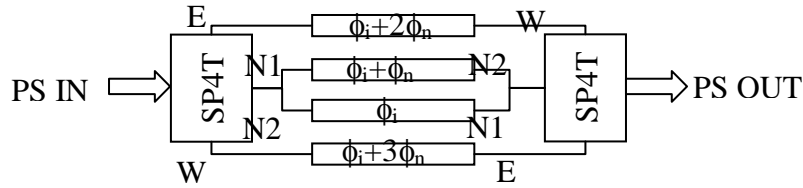


Fig. 2-23: General Schema of a 2-bit phase shifter using switched-lines

A small detail is that in the case of the north outputs (N1 and N2) of the SP4T, they have been modified in order to avoid coupling between them. Moreover, the characteristic impedance of the lines is optimized in order to improve input matching at central frequency. The layout of the phase shifter is shown in Fig. 2-24.

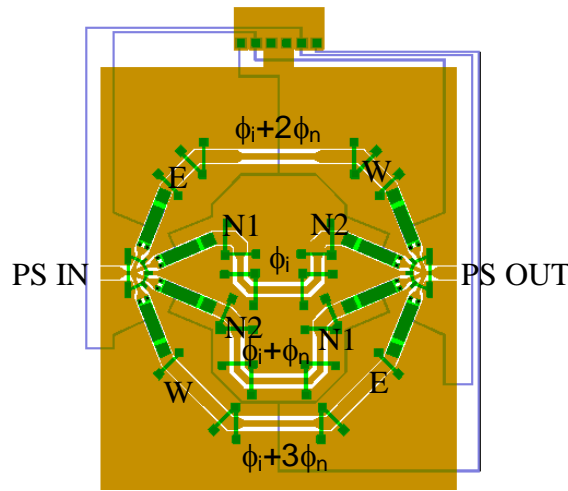


Fig. 2-24: Layout of the phase shifter based on switching

The advantage of using a wide band SP4T is that varying the working frequency, the phase shifting will vary maintaining similar RF performance. Fixing the length of the line l_n , the phase shifting will depend of the frequency.

$$\phi_i = \frac{l_n 4\pi}{n\lambda} = \frac{l_n 4\pi \sqrt{\epsilon_r} f}{nc} \text{ where } n=0..3 \quad \text{Eq. 2-6}$$

In Fig. 2-25 the RF performances of the phase shifter are plotted. In all cases RL better than 15dB and IL better than 2dB are achieved from DC to 60GHz. The losses are due mainly to the losses introduced in each SP4T.

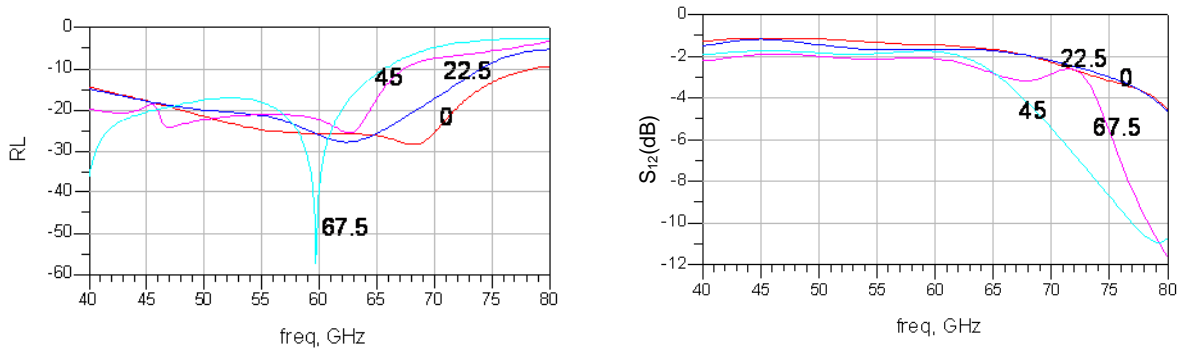


Fig. 2-25: Input matching and S_{12} of the phase shifter

Finally in Fig. 2-26 the phase of each line is plotted. Imagining an application at 60GHz, the phase shifting between lines according to Eq. 2-6, is 22.5° . The results of the simulation show a maximum error of phase of 1.8° at 60GHz for a step of 22.5° . Moreover, for an application at 30GHz, a step of 11.25° is fixed and the phase error is 2° . In fact from 30 to 60GHz this phase shifter can be used since the phase is linear and good RF performances are achieved.

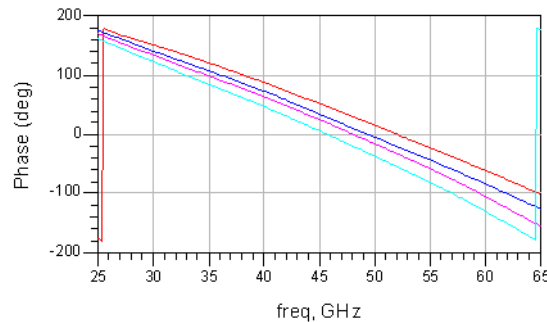


Fig. 2-26: Phase of each switching line

2.4 Conclusions

The presented fabrication process (LAAS-CNRS) has demonstrated to be a good platform for the development of RF-MEMS based circuits. It has been shown that this process is able to solve its problems of dispersion by means of adding new steps and materials to the basic process: development of a 3rd metal layer for improvement of contact capacitance and optimization of the process for flat cantilevers have been demonstrated. Another advantage is that the same platform develops different types of switches (capacitive and resistive). The main drawback of this approach is the low reproducibility of the results. The solution applied in one RUN may not be the adequate in the following one if a change in the design is done.

On the other hand, the adaptability in terms of configuration and topology mentioned above has allowed building complex circuits. The examples are the routing structures based on series switches disposed in such a way (very close to the junction) that the losses and isolation measured is in the state of the art on SPnT and phase shifting circuits.

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Chapter 3

RF-MEMS in medium TRL environment

3.1 Introduction

This chapter describes the CEA-Leti fabrication process of a resistive series switch. The approach implemented in this case is based on the single component optimization to be developed according to a pick and place approach¹¹ [64]. The process steps and material selection has been fine tuned on the specific device choice. Although this approach restrain considerably the design flexibility (since very limited variation on the basic design are allowed), it allows tackling more effectively the reliability issues.

The development of RF-MEMS in CEA-Leti started with capacitive switches [65] [66], but due to dielectric charging problems, poor RF performance in low frequencies and the necessity of focalizing efforts to only one type of switch, the project was stopped. At the same time, a shunt resistive switch with three contact dimples on a SiN membrane and two side electrodes was proposed and investigated over DC-100GHz frequency range in [67]. The main problem of this switch was the difficulty to establish the simultaneous contact of the three dimples. For this reason, the original design was modified to become a series switch with only two gold contacts presented in [68].

The last evolution of the CEA-Leti switch is the use of Ruthenium as a contact material and the elimination of the dielectric of the electrodes to reduce the charging at the actuator [69]. This thesis has used this novel device to implement routing circuits and to study the evolution of the RF performance versus time defining the failure mechanism and the possible solutions.

The chapter is organized starting with the description of the device and our proposed model for contact resistance computation. Afterward the evolution of the contact resistance is shown according to the contact size and current flowing through it. Finally a SPDT is designed, modeled and characterized for being used in more complex routing circuits for redundancy applications (under ESA project REDS [70]-[72]).

¹¹ By means of a wire bonding or flip chip bonding on a hosting circuit

3.2 Resistive contact switches (CEA-Leti)

3.2.1 Technology and switch description

The solution proposed by CEA-Leti is a dielectric-less ohmic switch based on a nitride membrane and electrostatic actuation (Fig. 3-1). The movable part is made of a bridge type nitride membrane suspended over a coplanar wave-guide (CPW), with a central ruthenium (Ru) contact and a pair of electrodes on both sides. When the membrane is in up state, the signal in the RF line is interrupted and the isolation is high. When a biasing voltage is applied between the upper electrodes located under the membrane and the CPW ground plane, the membrane is pulled down. The metallic contact fills the discontinuity on the RF line and the signal is transmitted.

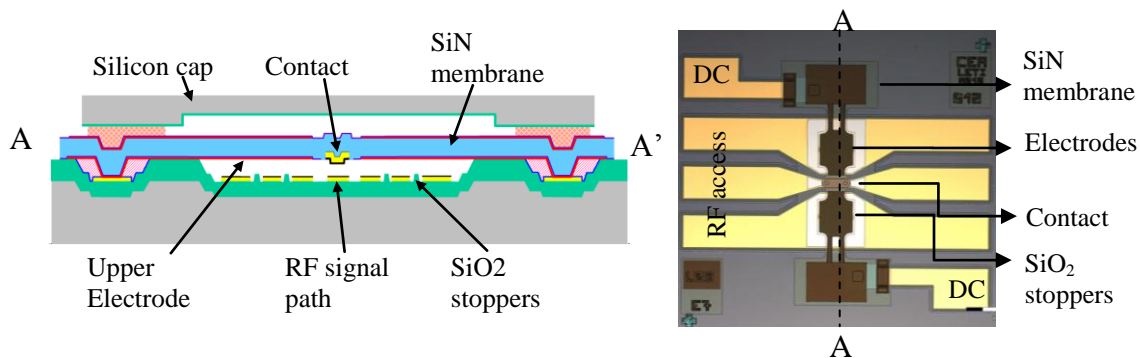


Fig. 3-1: Cross section (left) and top view of the CEA-Leti switch

The process flow developed requires 11 mask levels on CEA 200mm MEMS dedicated fabrication and starts with the realization of the SiO₂ cavities and the stoppers. Then, the metal for the RF and command lines and the silicon sacrificial layer are deposited respectively. Over the planarised sacrificial layer the TiN (Titanium Nitrate) electrodes are deposited and the vias for connecting the electrodes and the DC lines are opened. By etching small bumps on the sacrificial layer contact area, the Ru/Au contact dimples are created. Before releasing, the SiN (Silicon Nitrate) membrane and the top electrode, that symmetries the bridge for better flatness, are realized. The most relevant characteristics of each part are:

- ✓ **CAVITY:** cavities and mechanical stops are realized by thermal oxidation and selective etching of the oxide layer in order to obtain fine accuracy of height and so control functional gaps when the bridge is up and when the bridge is down. The whole RF and command lines are inside cavities and not only the part under the membrane.
- ✓ **METAL:** RF lines are realized with gold (Au) metal. Ruthenium (Ru) is deposited on gold below the membrane in order to avoid hillocks growing on gold. Ru is also deposited at contact level to ensure better reliability of the ohmic contact because it is less sensitive to stiction than pure gold contact. The price to pay for a switch with a reliable Ru contact is the need of a carbon-free hermetic packaging because Ru is highly sensitive to carbon contamination.
- ✓ **SACRIFICIAL LAYER:** A silicon sacrificial layer was used instead of an organic sacrificial layer to avoid carbon contamination of the contact and obtain flat membrane profile before release thanks to planarization process. PECVD deposition conditions and planarization parameters of the silicon layer were studied through technological bricks.
- ✓ **ELECTRODES:** TiN electrodes are deposited directly on silicon sacrificial layer prior SiN membrane deposition. After release of the membrane there is thus no dielectric

between stationary and mobile electrodes except SiO_2 stops that prevent electric contact between electrodes when the bridge is down. This “dielectric-less” actuation area solve charging problems that cause shift of pull-in voltages and failure of switches.

- ✓ **CONTACTS:** Mobile contacts in the membrane are based on Ru/Au/Ti metallization. Ru is the contact material to achieve Ru on Ru contact with the RF line.
- ✓ **MEMBRANE:** Membrane is realized with a tensile SiN that allows the membrane to remain tense and flat after release. A TiN metallization with the same pattern than mobile electrode is realized on top of SiN membrane in order to have a symmetric stacking. Release of the membrane is done by etching the sacrificial silicon using XeF_2 (dry-etching).

Three other mask levels are used to realize a packaging WLP (Wafer Level Packaging) by polymer bonding of a silicon cap. This packaging ensures waterproof mechanical protection of the switch and preserve dry nitrogen (N_2) atmosphere within the switch cavity. The inconvenient of this packaging solution is the carbon contamination of the contact seen in Fig. 3-2. A carbon-free thin-film hermetic packaging is currently under development to guaranty contact reliability during numerous mechanical cycles.

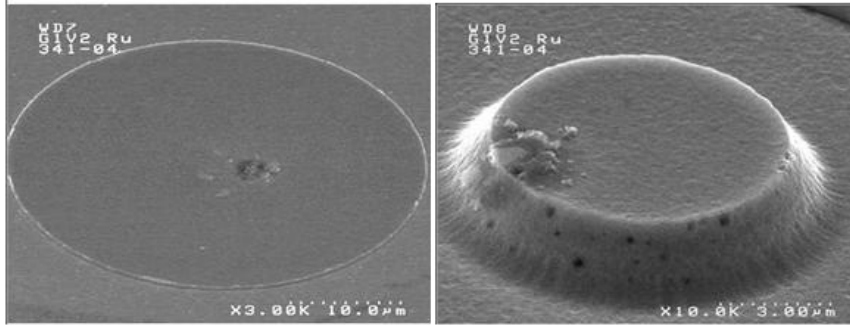


Fig. 3-2: Example of carbon contamination of the contact seen in the devices

The RF performance from DC to 65GHz of this design is plotted in Fig. 3-3. Input matching and isolation better than -25dB and -15dB respectively is observed while losses are better than -0.4dB over the entire band.

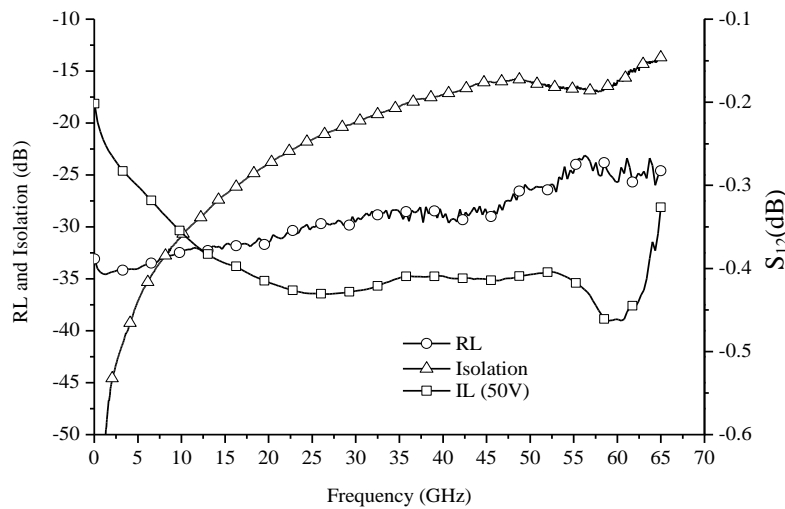


Fig. 3-3: RF performance of the CEA-Leti switch in ON (DOWN) and OFF (UP) state

Equivalent circuit description for contact resistance computation

The most popular technique to measure the contact resistance is the 4-points measurements. The main drawback is the difficulty to separate the different sources of losses (mainly conductor and substrate¹² losses). In order to carefully estimate the contact resistance, the extraction of an equivalent circuit based on RF measurements data has been carried out over the entire frequency band. The advantage of this equivalent circuit is that it can be easily used for constructing more complex circuits as it will be seen in section 0.

Transmission Line Modelling

With the proposed technique, in order to eliminate the conductor and substrate losses from the measurements, firstly, some tests structures consisting in CPW are measured and characterized (Fig. 3-4). Using the model of these test structures, the membrane's effect is added afterwards.

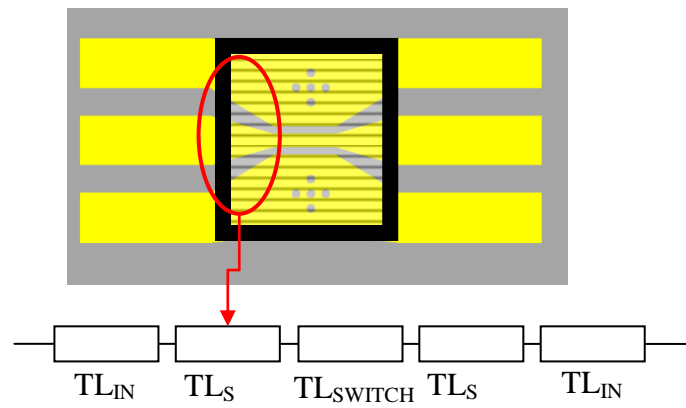


Fig. 3-4: Layout (top) and equivalent circuit (bottom) of the test structures

The model of the RF line is divided in 3 different parts: The access lines (TL_{IN}), the taper including the packaging effect (TL_S) and the switch zone (TL_{SWITCH}). Each part has its own characteristic impedance (Z_0), length (L) and effective epsilon (ϵ_{eff}) as reported in Table 3-1. Noteworthy is that ϵ_{eff} of TL_{PACK} is higher due to the material used for the packaging which is deposited over the line changing the propagation constants of the CPW.

	Z_0	L	ϵ_{eff}
TL_{IN}	44.5	180	6.7
TL_S	53.2	65	11
TL_{SWITCH}	53	98	6.7

Table 3-1: Characteristic impedance, length and epsilon effective of the model

Five identical test structures have been measured by extracting the mean and standard deviation of the input matching and insertion losses. These measurements (Fig. 3-5) show that the dominant loss mechanism is the skin effect in the conductors. Its effect is added to the model by means of an attenuation proportional to $\sqrt{\frac{1}{f}}$. Results reported in Fig. 3-5, demonstrate an excellent fitting of the model with the average mean value from measurements.

¹² In 4-points measurements this source of losses is very low

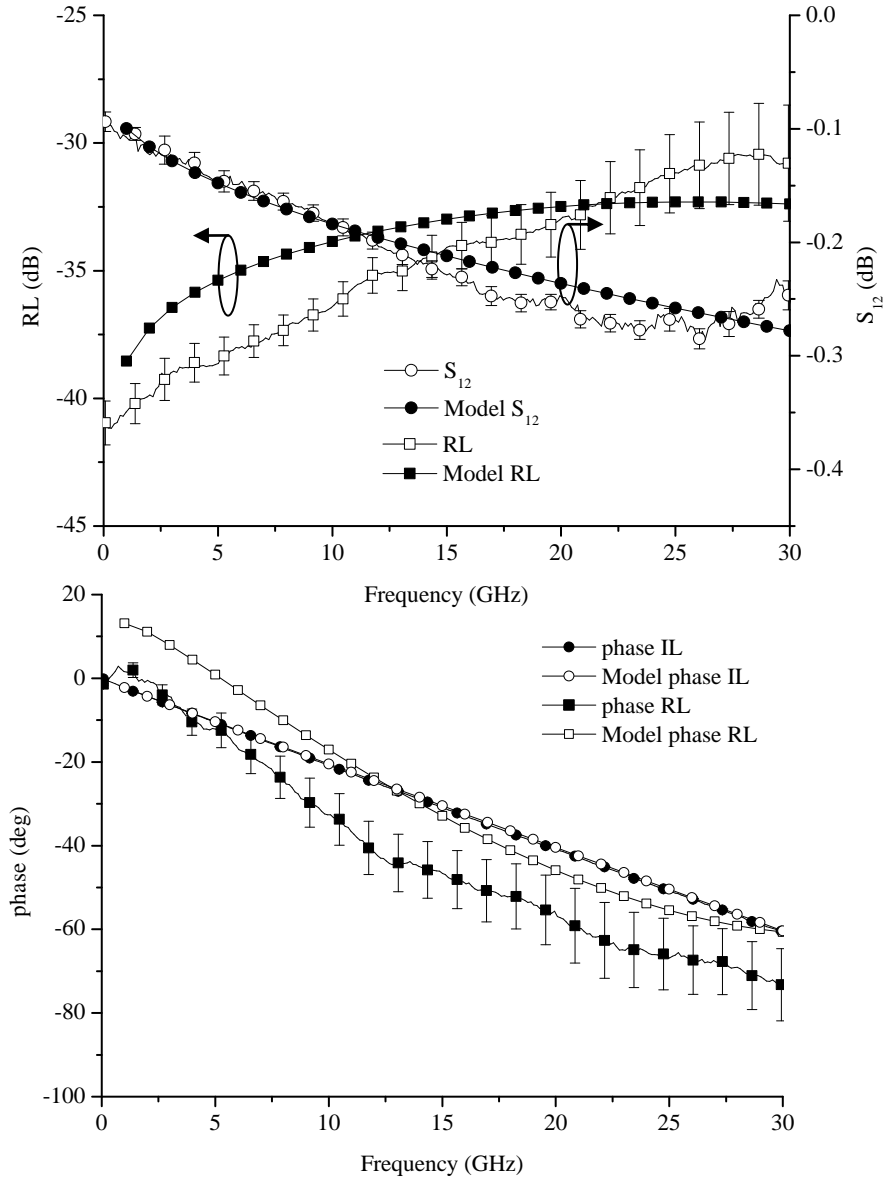


Fig. 3-5: Measured and model RL and S_{12} modulus (top) and phase (bottom)

MEMS modelling

Using the line model proposed above, the contact zone is simulated with a series resistance in DOWN state (ON) and a series capacitance in UP state (OFF). The resistance (R_{ON}) comes from the Ru-Ru contact and the capacitance (C_{UP}) is derived from the parallel plate formula between the line and the contact considering a gap of 0.5 μm . In Fig. 3-6 the comparison between measurements and the model is plotted showing very good agreement with $R_{ON}=1.5\Omega$ and $C_{UP}=5\text{fF}$.

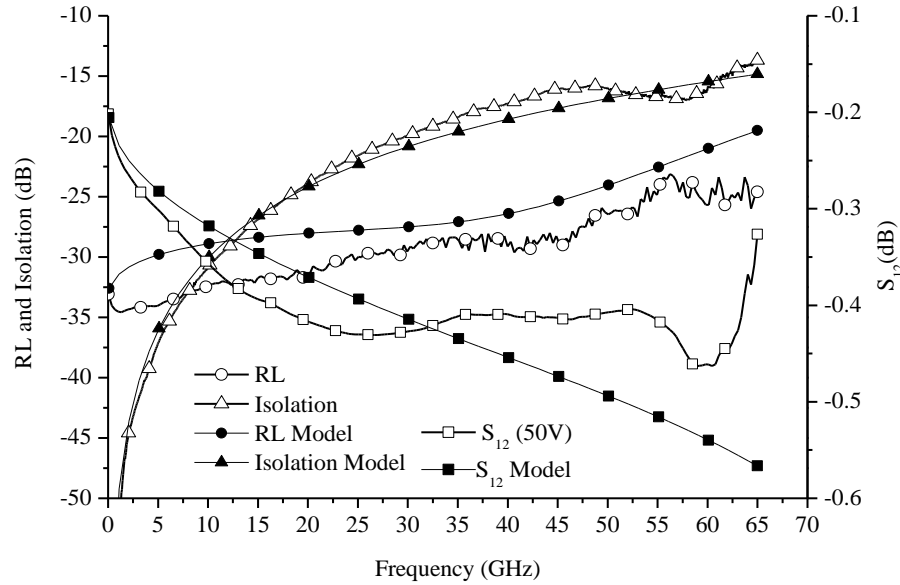


Fig. 3-6: Comparison between modelled and measured S-Parameters of the switch in UP (Isolation) and DOWN (RL and S_{12}) states

3.2.2 Impact of fabrication process and reliability tests

There are two key parameters that define the reliability of contact-based devices: the dielectric charging on the actuator and the contact resistance over lifetime. In the first case, due to the dielectric-less solution explained in the previous section, the charging is avoided. For this reason in this section only the contact reliability problem is considered. First a study of the optimal actuation voltage is done in order to ensure enough contact for repeatable performance versus time. Second, the study of the performance during lifetime is described showing some preliminary results. Finally the failure analysis is depicted using the RF performance analysis.

Actuation voltage for optimal RF performance

Using the equivalent circuit presented above, the contact resistance of the switch is computed. The advantage of this method with respect to the four-point measurements is that the losses due to the substrate and the lines are removed. In Fig. 3-7 the contact resistance is evaluated under different actuation stress. Two different operational regions are indentified with respect to the dispersion of the contact resistance. The same regions were observed in [73] for an AuNi-Au contact. This effect is due to the hardness of the contact material (Ni in [73] and ruthenium in our case) which needs higher contact forces comparing with gold contacts in order to achieve the same contact resistance [74]:

- Contact region ($30V < V_{act} < 45V$): a resistive behavior is observed but the contact resistance dispersion (12-20Ohms) is very high between identical devices in the same wafer.
- Closed region ($V_{act} > 45V$): The contact resistance is stable and with low dispersion (0.4Ohms) between identical devices in the same wafer.

Fig. 3-7 shows that in order to enhance the contact force, so to obtain better RF performance, the device has to be driven at least at 50V. At 45V the mean contact resistance reaches the same value as at 50V but the dispersion is higher (1Ω in front of 0.6Ω at 50V). The chosen

actuation voltage is 40% higher than V_{PI} (30V) and safely below the break-down voltage¹³ ($V_{BD} > 100V$).

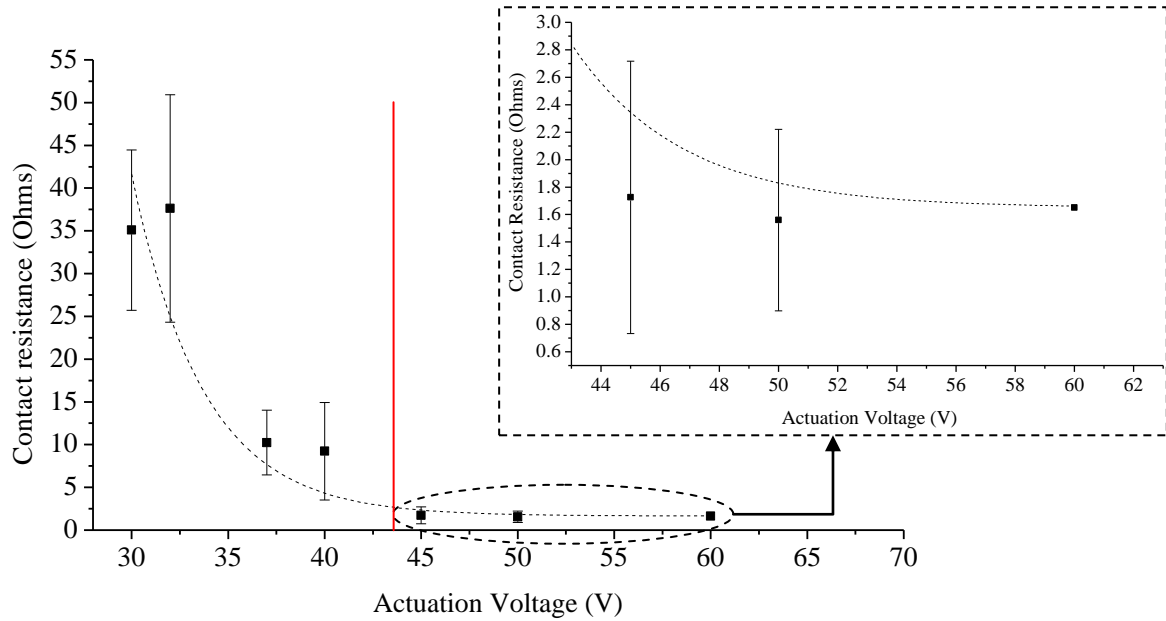


Fig. 3-7: Mean (square), standard deviation (error bars) and exponential fitting (dashed line) of contact resistance for different actuation voltage. The red line separates the contact (left) from the closed (right) region. Inset with the closed region

When the actuation voltage increases, the contact resistance converges toward smaller values until it attains the asymptotic value of circa 1.5 Ohm. The relationship is plotted in Fig. 3-7 with a dashed line. In previous work [74] the same relationship was found between the contact force and the contact resistance for Ru-Ru contacts (Fig. 3-8). The absolute contact resistance values cannot be compared because in our case no DC current is imposed through the contact.

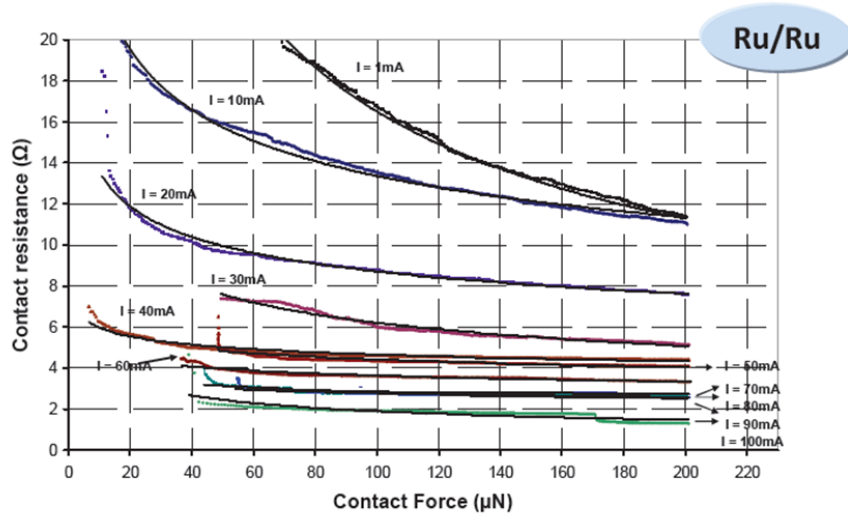


Fig. 3-8: Relationship demonstrated in [74] between contact force and contact resistance

¹³ The break down voltage is supposed over 100V because no failure in the device was observed when increasing the actuation voltage. It has not been specifically computed.

In order to see the effect of the number of stoppers in the actuation voltage, thus in the insertion losses, a variation in their number is proposed. In terms of mechanic behaviour, this is the unique variation that the fabrication process allows, since the membrane design (thermal compensation and planarity) has already been optimized by CEA-Leti previous developments.

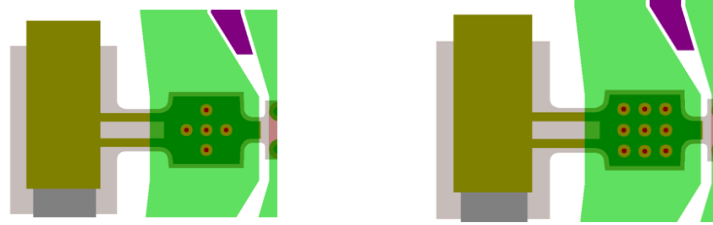


Fig. 3-9: Layout of the membrane with 5 (left) and 9 (right) stoppers

The number of stoppers is varied from 5 to 9 as seen in Fig. 3-9. The direct impact of this change is the actuation voltage since the actuation area decreases by a 9% which means that the contact force on the dimples decreases increasing the insertion losses. This is demonstrated in Fig. 3-10 where the insertion losses are measured at three different actuation voltages (40, 50 and 60V). In the case of 5 stoppers, the insertion losses are stabilized at 50V as it is seen in section 3.2.1 but, using 9 stoppers 60V are needed for an optimum contact.

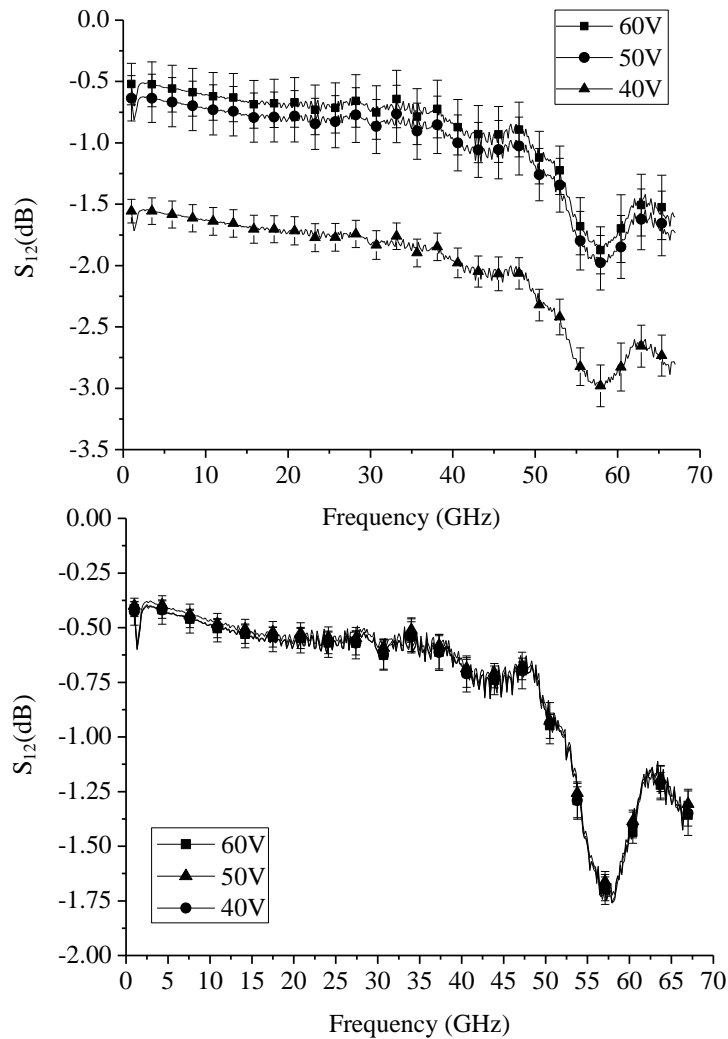


Fig. 3-10: S_{12} of the SPDT with 9 (top) and 5 (bottom) stoppers

Lifetime study

Protocol

The switches are tested in an open environment (22° and 40% humidity) using a VNA (Anritsu MS4647A) for RF characterisation (DC-65GHz), a function generator (Tektronix AFG320) plus an amplifier (Falco Systems) for increasing the dynamic range of the DC biasing. Two bias tee connected to the ground are used in order to protect the VNA and also to ensure that there is no DC voltage through the contact. The ground of the DC-probes and the chuck is also connected to the same ground. The acquisition of the S-parameters and the biasing of the switches are synchronized and automated using a LabVIEW program through a GPIB connection (Fig. 3-11).

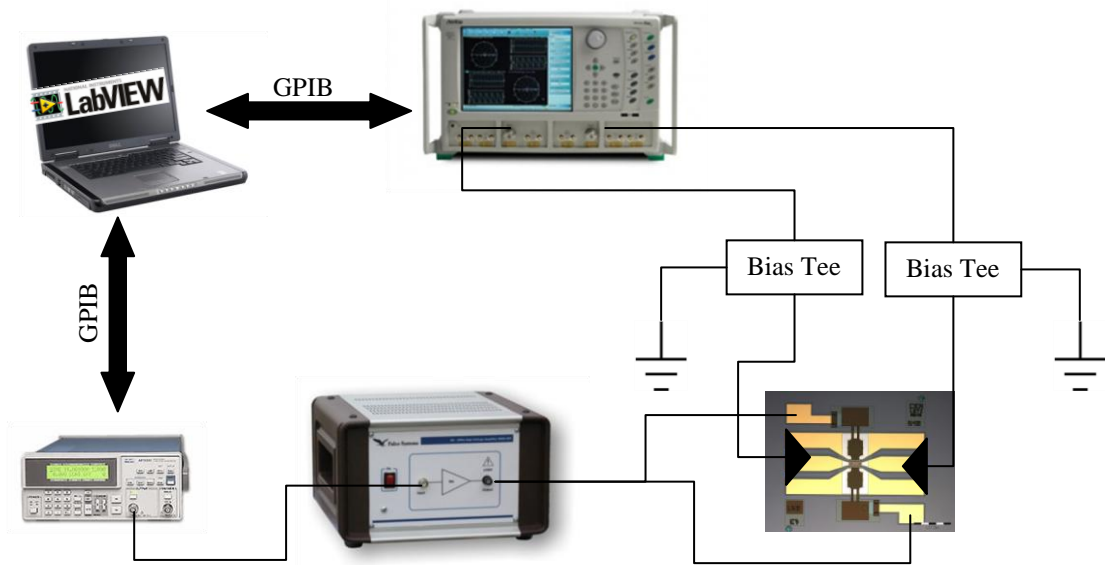


Fig. 3-11: Schematic of the used set-up

The test protocol is presented in Fig. 3-12. The switch is actuated at 50V using a unipolar square signal of 0.02Hz and duty cycle of 50%. The actuation voltage was computed in previous section for optimal RF performance while the actuation time ($T_{ac}=25s$) and the time between actuation ($T_s=55s$) are chosen large enough to ensure a stable contact, and to decouple the effects between consecutive actuations respectively. This procedure is repeated for three different RF power (-30dBm, -10dBm and 0dBm) for a fixed number of actuations ($N_{ac}=1000$). The S-parameters in the entire band (DC-65GHz) are acquired one second before the end of the actuation window.

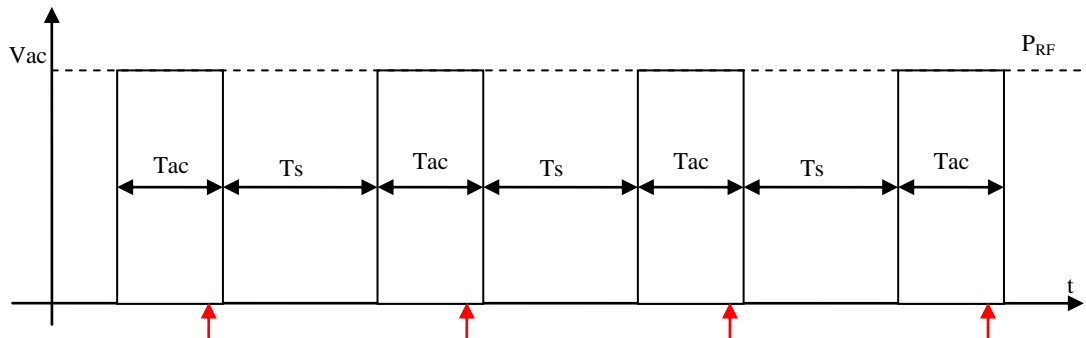


Fig. 3-12: Test protocol for the tested switches. In red the moment of the acquisition of the S-parameters

Two different calibrations of the VNA are done in the following order:

- 1) Power calibration: Using a power meter connected to the VNA, the desired RF power (P_{RF}) is set in the entire band. This ensures the same RF power throughout all the frequencies (which is not normally the case if no specific calibration is done) and it means that the RF current (I_{RF}) through the contact is fixed. Eq. 3-1 shows the relationship between P_{RF} and I_{RF} supposing a perfect matching in the device (better than 25dB in the entire band) which means that all the induced power to the DUT goes to the contact and is not reflected. In Table 3-2 the chosen RF power with the correspondent RF current is computed.

$$P_{RF} = \frac{1}{2} Z_0 I_{RF}^2 \rightarrow I_{RF} = \sqrt{\frac{2P_{RF}}{Z_0}} \quad \text{where } Z_0 = 50\Omega \quad \text{Eq. 3-1}$$

P_{RF}	I_{RF}
-30dBm	200 μ A
-10dBm	2mA
0dBm	6.3mA

Table 3-2: Chosen RF power levels with the correspondent current computed with Eq. 3-1

- 2) RF Calibration: It is done using the “Line” element of the Thru-Reflect-Line calibration kit and only in one direction (from P1 to P2) in order to calibrate the single S_{21} parameter (used for the tests).

As the duration of the tests is very long (aprox. 15h for 1000cycles) it should be taken into account the degradation of the quality of the calibration. For normal S-parameters measurements it is recommended to redo the calibration every 5-6h, but, in the case of long term tests, this calibration cannot be updated.

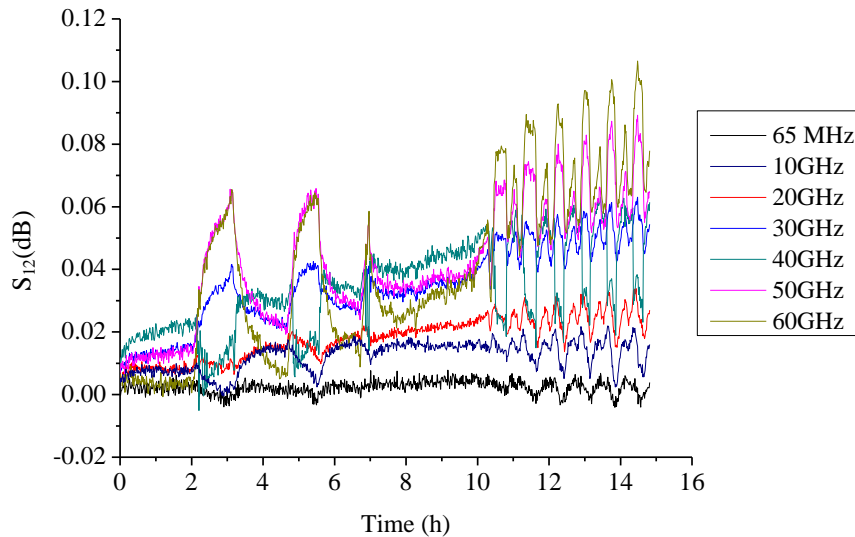


Fig. 3-13: S_{12} of the Line of the calibration kit versus time

In order to have an idea of the deviation of the RF calibration, the line of the Thru-Reflect-Line calibration kit is measured continuously during 15h at the same ambient conditions. In Fig. 3-13 the insertion losses of the “Line” is plotted versus time for different frequencies showing that higher frequencies (40-65GHz) achieve higher dispersion (max. 0.1dB) as was expected. Note that the jitter around the average value (max. 0.05dB) is likely due to external ambient interferences that may have slightly affected the measurement over 15h. In order to

remove the effect of the deviation of the calibration (IL_C) in the switch measurements (IL_S), all the switch measurements presented (IL_D) will be de-embedded according to:

$$IL_D = \overline{IL_S} + \overline{IL_C} \quad \text{Eq. 3-2}$$

Since the setup is automated the RF carrier cannot be disrupted while doing the tests, another limitation of the set-up is the impossibility of doing cold-switching (no current through the contact while the device is actuated). The only way of doing that is by lifting off the RF probes, which however, turns out to affect the contact repeatability hence introducing further incertitude in the measurements. For this reason, the lowest possible RF power (-30dBm) is used to validate the cold-switching mode.

First of all the pristine switch under study undergoes a cold-switching (lifting-off the RF probes) during 30 consecutive actuations. Afterwards the same device is hot-switched (RF probes in permanent contact) during 30 actuations more. From results depicted in Fig. 3-14, it can be seen that the same degradation trend in the insertion losses is observed. The linear fitting curve extracted show very similar slope (m_c and m_h) in both switching conditions. This means that at -30dBm there is no significant difference between hot and cold switching for the considered device. Therefore the switch will be considered as cold switched even if the test is in the hot switching operating mode.

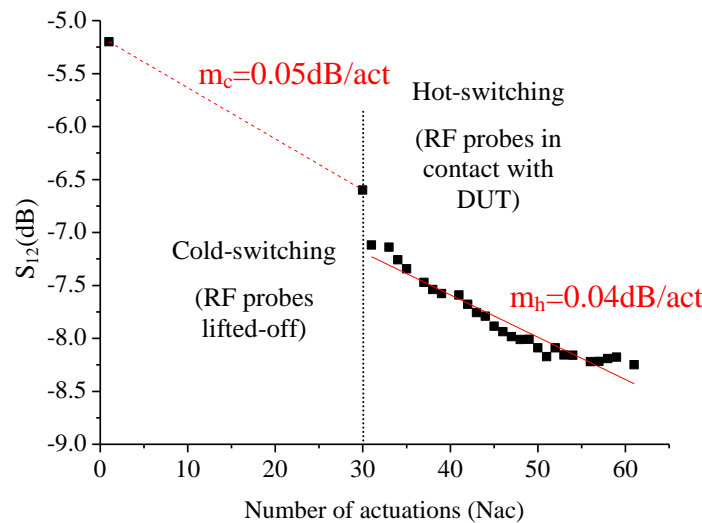


Fig. 3-14: Hot versus cold switching at -30dBm. In red the linear fitted curve for cold (dashed) and hot switching (line).

CEA-Leti has provided 24 switches (5 of a contact diameter of 10 μ m and 19 of 2 μ m) in order to check the evolution of the losses versus time. Due to the small quantity of available devices, the efforts were concentrated on the variation of the RF current as a possible accelerating factor for contact stabilization. The results presented in the following section are preliminary and should be confirmed with a larger amount of devices.

Previous work in contact reliability, such as [74], assumes that the DC current on the contact could have influence on the contact degradation. Others think that is the voltage applied on the contact that is playing the degradation role [75]. In this work no DC current or voltage is applied in order to get rid of these assumptions. In fact, in commercial devices, such as Radant ones, it is advised to their users to avoid any DC current through the contact.

Contact resistance versus time

The first studied type of switch has a contact size of $10\mu\text{m}$ and it presents very high losses. This could be caused by the burn-in¹⁴ and storage at 80°C during one week done beforehand at CEA-Leti which could induce carbon contamination in the device.

In Fig. 3-15 the insertion losses of three identical switches after every actuation are shown. Each switch is tested at a different RF power: -30, -10 and 0dBm. It seems that the number of actuations needed to achieve stable contact depends from the RF power applied through the contact. The higher the RF power, the lower the number of actuations needed for stable contact. However, there are two incoherencies that should be taken into account and that limit the extraction of concrete conclusions:

- 1) An unexpected result for the switch at -30dBm: it is supposed to present higher losses than the other two. In fact, for lower RF power, hence lower current, higher level of contact resistance, hence a higher losses, is expected.
- 2) Different stabilization mechanisms observed: while in -30 and 0dBm a clear straight line with different slopes is observed, in -10dBm a deterioration followed by an improvement of the contact resistance is seen as was observed in [76].

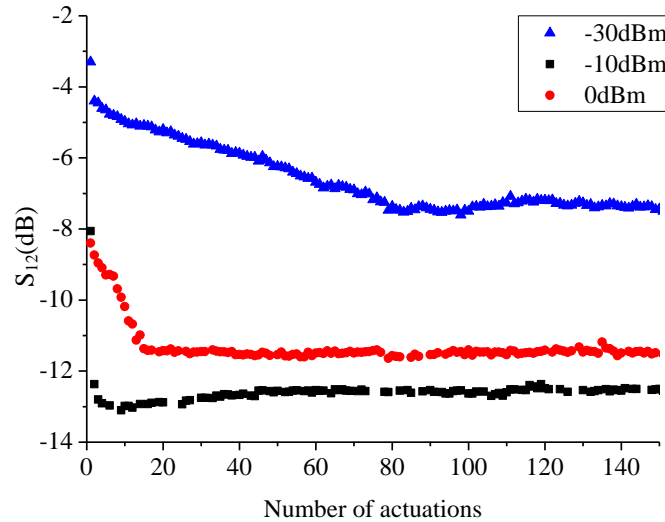


Fig. 3-15: S_{12} (at 30GHz) after each actuation at three different RF power.

The second type of switch ($2\mu\text{m}$ of contact) was never tested before. For this reason the initial losses observed are approximately 0.5dB. In Fig. 3-16 (top) the results of the tests carried out at three identical switches at different RF power is plotted. In this case only at -30 and -10dBm of P_{RF} the repeatability of the contact is assured. In the case of 0dBm, none of the tested switches has achieved repeatable contact (Fig. 3-16 bottom). These results seem to prove that at 0dBm a contact degradation mechanism is activated.

Noteworthy that the first actuation of all the switches in Fig. 3-16 achieves the same S_{12} value (not seen in $10\mu\text{m}$ contact) which shows that the fabrication process is stable and the contact behavior could be modeled. Another proof of the stable fabrication process is that in -10 and -30dBm the insertion losses stabilizes at the same value (-5.4dB).

¹⁴ 10.000 cycles at bipolar actuation of 34V (4V - 100 μA applied on the contact)

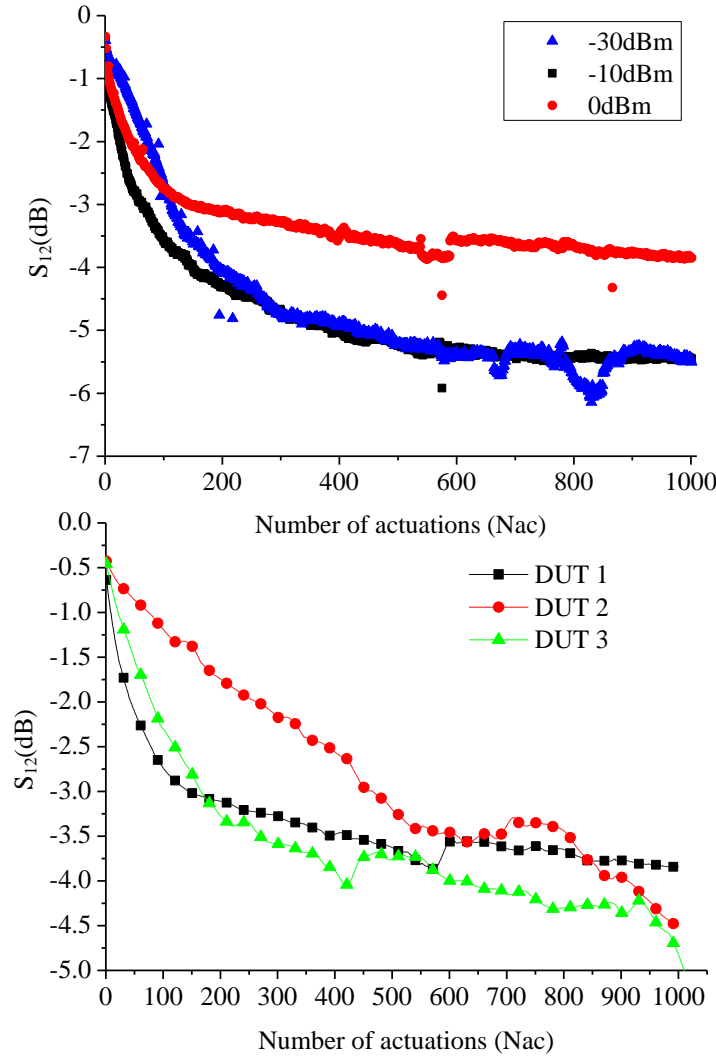


Fig. 3-16: S_{12} (at 30GHz) after each actuation: at three different RF power (top) and at 0dBm for three identical devices (bottom).

The tests presented in this section have demonstrated the reliability challenge that CEA-Leti should afford. The observed results are attributed to the carbon contamination of the contact due to the non-hermetic package. This effect has already been detected in the previous version of the switch based on Au-Au contact [75]. In order to know if a hermetic package would solve this problem, a preliminary test in a controlled environment simulating the hermetic package should be done.

Failure mechanisms

In this section the contact failure is studied by using the S-parameters in the entire band. The lumped-elements based equivalent circuit of the switch is used in order to understand the physical mechanism occurring on the contact dimple. Noteworthy is that the same degradation mechanism is observed when the switch is continuously in the DOWN state than when it is cycled.

In literature [76] it was shown that the failure mark of Ru-Ru contacts is the sudden increase of the contact resistance (fail to close), in contrast with gold contacts (fail to open). In this section the results of the switches that have not supported the tests due to contact failure are presented. As was expected all the switches of both types (2 and 10 μ m contact) have presented the same failure mechanism: fail to close.

In Fig. 3-17 one of the failed switches of type $10\mu\text{m}$ is presented. The insertion losses are plotted at different frequencies (Fig. 3-17 left) in order to demonstrate that the trend of the degradation is the same before failure ($N_{ac}<400$) while after degradation the insertion losses change a lot with frequency. Regarding Fig. 3-17 right, it is seen that at $N_{ac}=450$ the switch response is capacitive while a flat response (resistive behavior) was expected.

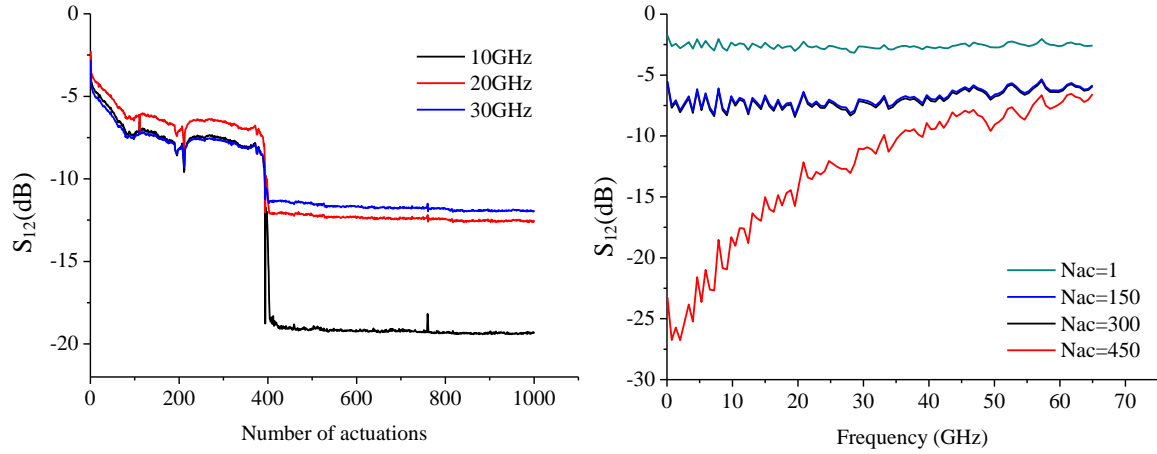
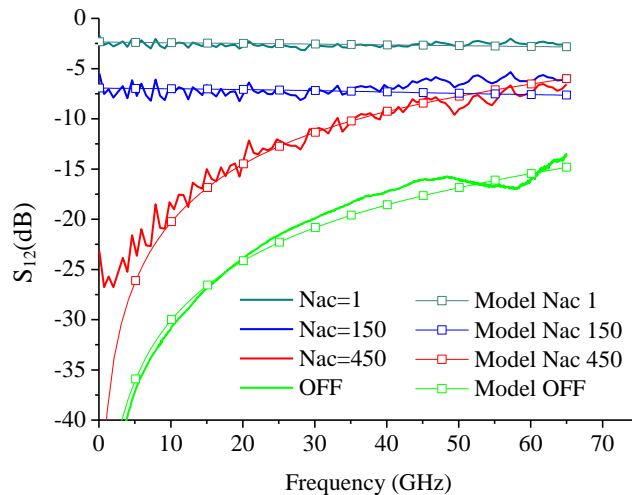


Fig. 3-17: Left: S_{12} versus number of actuations for different frequencies. Right: S_{12} in the entire band for different number of actuations

The failure mode observed could yield two different conclusions: either there is a very high resistance (fail to close) or there is a mechanical failure. In order to discard the mechanical failure, the actuation voltage is increased up to 60V and it is observed that the switch recovers the resistive behavior. However, the contact resistance is approximately 120Ω .

The equivalent circuit model presented in previous section 3.2.1 is used to validate the RF behavior (Fig. 3-18). For N_{ac} under 400, the contact zone is modeled with a resistor and above 400 it is mostly a capacitor whose values are resumed in the table of Fig. 3-18.



Nac	R (Ω)	C (fF)
1	30	
150	121	
300	121	
450		15
OFF		4

Fig. 3-18: Comparison between measurements and model at different N_{ac} at 50V and in OFF state after the test. The table resumes the values used in the model.

The difference between the OFF state and the $N_{ac}=450$ show the possible formation of a dielectric film covering the entire contact dimple creating a capacitor between the dimple and the line when the switch is actuated. On the other hand, the high values of contact resistance for $N_{ac}<400$ is due to the beginning of the contamination phenomena where the created

dielectric contamination is still ongoing and it is only located in some parts and a metal-metal contact.

Conclusions on lifetime study

For optimal RF performance the actuation voltage should be at least 50V which ensures the contact repeatability. The chosen actuation voltage is 40% higher than V_{PI} (30V) and safely below the break-down voltage. In addition, when the number of stoppers is increased, the actuation voltage should also be increased to 60V. Both results demonstrate that the enhancement of the contact force should be done through the actuation voltage.

The minimum number of actuations for stable contact seems to depend on the RF power (i.e. current) through the contact. By increasing the current the minimum number of actuation before stabilization is decreasing. This phenomenon could be explained by attributing to the current a healing role (cleaning). For sake of clearness and efficiency, tests should be done on hermetic packaged devices (no carbon contamination) or wafer level controlled environmental conditions.

The typical failure mechanism of Ru-Ru contacts (fail to close) is observed after several actuations at all the RF power level of the tests. The mechanical failure has been discarded by increasing the actuation voltage which makes the switch operational again. This last result infers the presence of contamination (also seen in the microscope in Fig. 3-2) in the contact which is eliminated by applying higher force in the contact. The presented equivalent circuit is able to describe the capacitive behavior in failed switches, confirming the hypothetical presence of contamination in the contact. All the results found in this section demonstrate the necessity of a hermetic package in order to control the operation environment of the device.

3.3 Applications in routing circuits: mPnT for space applications

3.3.1 DC-50GHz SPDT design, performance and contact study

The switch presented in section 3.2.1 is used for the development of a wide band single-pole double-through (SPDT) redundancy switch (Fig. 3-19). The design is based on one input (Port-1) and two 90-degree outputs (Port-2 and Port-3). The distance between the switch and the T-junction is optimized in order to achieve maximum isolation in Ku-Band. In Table 3-3 the target specifications are shown.

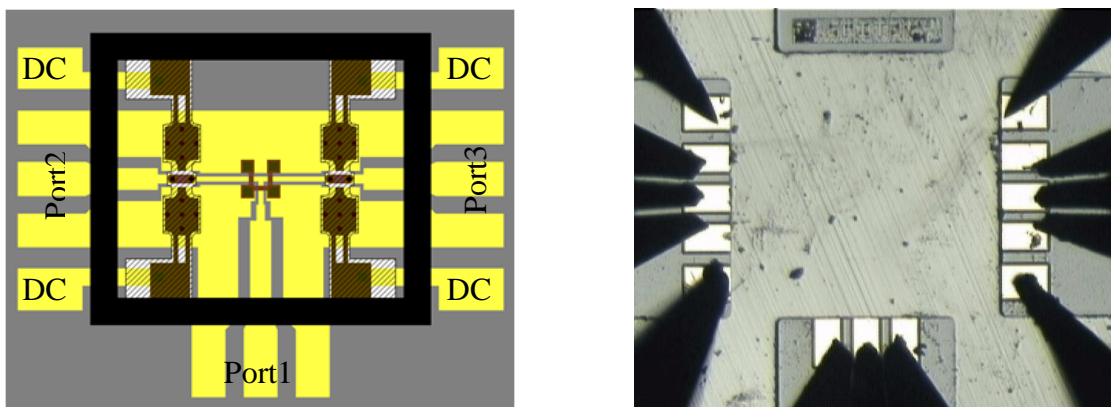


Fig. 3-19: Layout (left) and photo (right) of the measured device

Parameter	Specification
Band	Ku-Band (11.7-14.5GHz)
Bandwidth	Whole Band
Input match (50Ohms)	-15dB max
Output match (50Ohms)	-15dB max
Insertion Losses (unpack)	0.5dB max
Isolation between channels	50dB min
Maximum input power	10dBm

Table 3-3: Desired specifications of the SPDT

Measurements are done with a 4-port PNA (Agilent N5247A) from 65MHz to 65GHz and a DC-supply for the actuation of the switches. These measurements are done on 10 different devices in order to show the dispersion over the same wafer. Moreover, 10 different reference structures (i.e. without contact zone, see Fig. 3-20) have been characterized in order to extract the reference behavior obtained in absence of the contact zone of the membrane. These types of structures are used to separate the contact resistance of the switch from the losses due to substrate coupling, conductor losses and coupling between the membrane and RF ground.

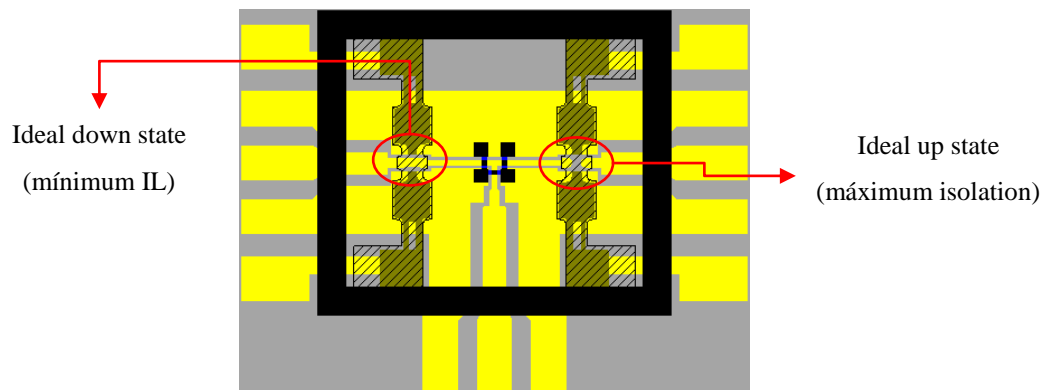


Fig. 3-20: Layout of the reference SPDT structures

In Fig. 3-21 the RF behavior of the SPDT is shown. Input and output matching are better than -20dB while insertion losses are below -0.9dB in the entire band (DC-50GHz). In the same band, isolation between the two outputs and between input and output is better than 25dB. The most promising information that these results show, it is not only the excellent RF performance in comparison with the state of the art but also the fabrication process stability on 8 inches wafers. In fact, the deviation between 24 devices in the same wafer (indicated by the error bars in Fig. 3-21) is very small and translates in 0.05dB for the IL and 0.6dB for the isolation. The larger dispersions observed on the RL below -30dB are due to the dynamic range limits of the PNA.

In Fig. 3-21 the model is compared with the measurements showing very good agreement with $R_{ON}=1.2\pm0.4\Omega$ (same range of contact resistance observed in Fig. 3-7 at 50V) and $C_{UP}=1.3\pm0.3fF$ (up-state capacitance) which gives a cut-off frequency of 102THz [76]. The model parameters of the SPDT are described in next section.

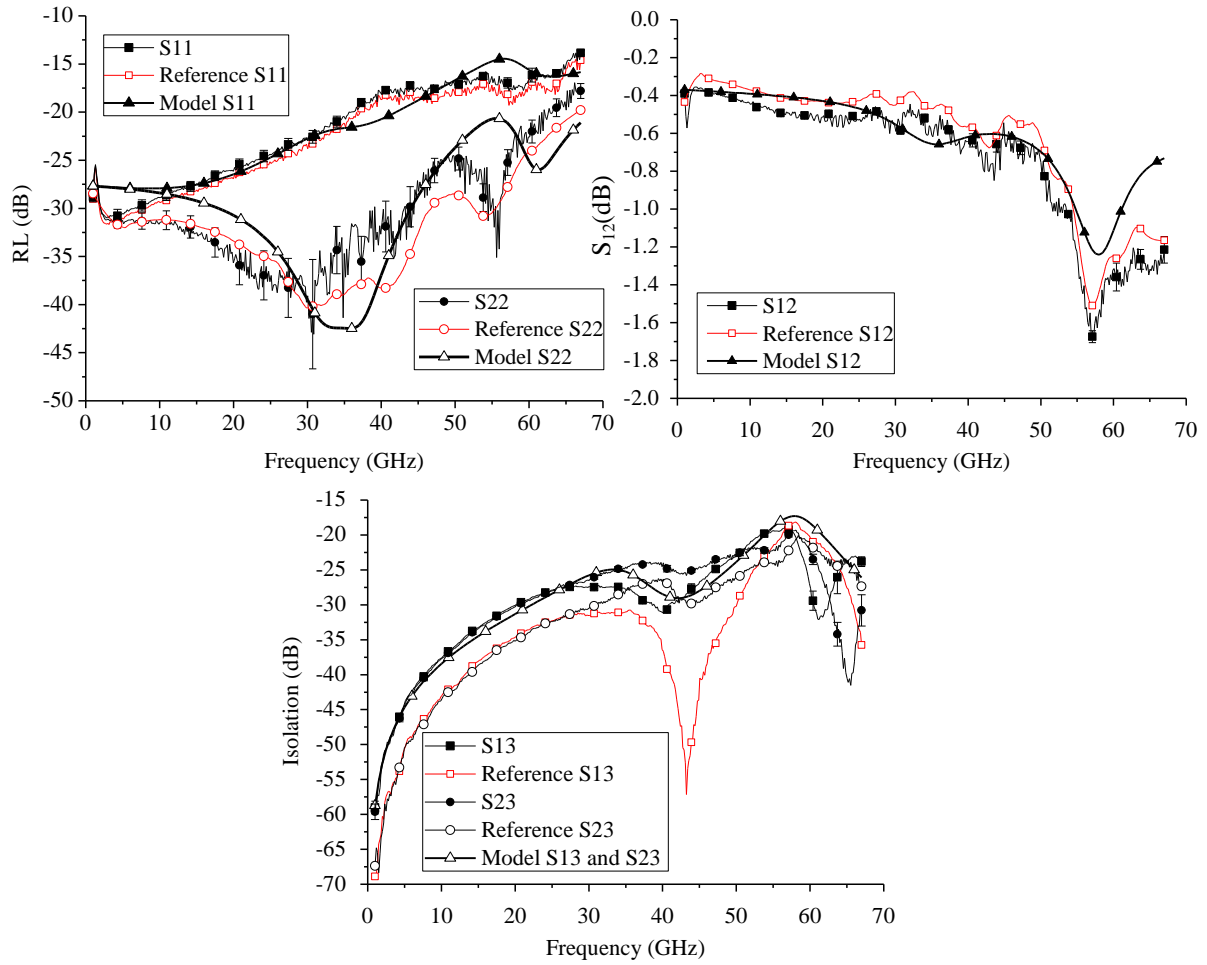
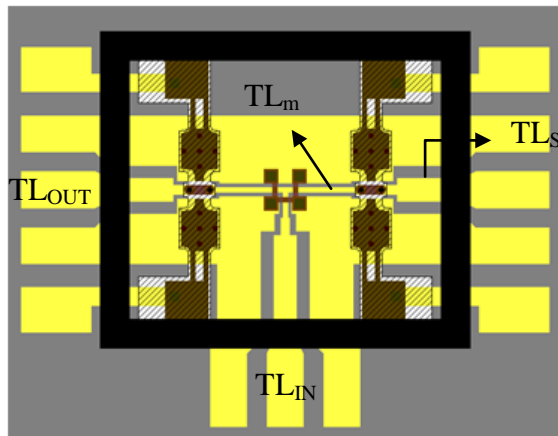


Fig. 3-21: Measured RF performance of the SPDT and the reference SPDT compared with the developed model

SPDT modelling

A lumped elements equivalent circuit is extracted from the RF measurements using the same technique as in section 3.2.1. Again, reference structures (Fig. 3-20) are used to separate the effect of the packaging (TL_S), the line and the substrate losses (TL_{IN} , TL_{OUT} and TL_m) from those coming from the switch (contact resistance R_{ON}). The model of the lines is compared in Fig. 3-23 with the measurements of the reference structures.



Lines parameters			
	Z_0	Length	ϵ_{eff}
TL_{OUT}	50	56.7 μ m	6.7
TL_{IN}	50	56.7	6.7
TL_S	58.6	65 μ m	11.45
TL_m	67.5	105.4 μ m	6.7
Switch parameters			
C_{UP}	1.3 \pm 0.3fF		
R_{ON}	1.2 \pm 0.4 Ω		

Fig. 3-22: SPDT model parameters

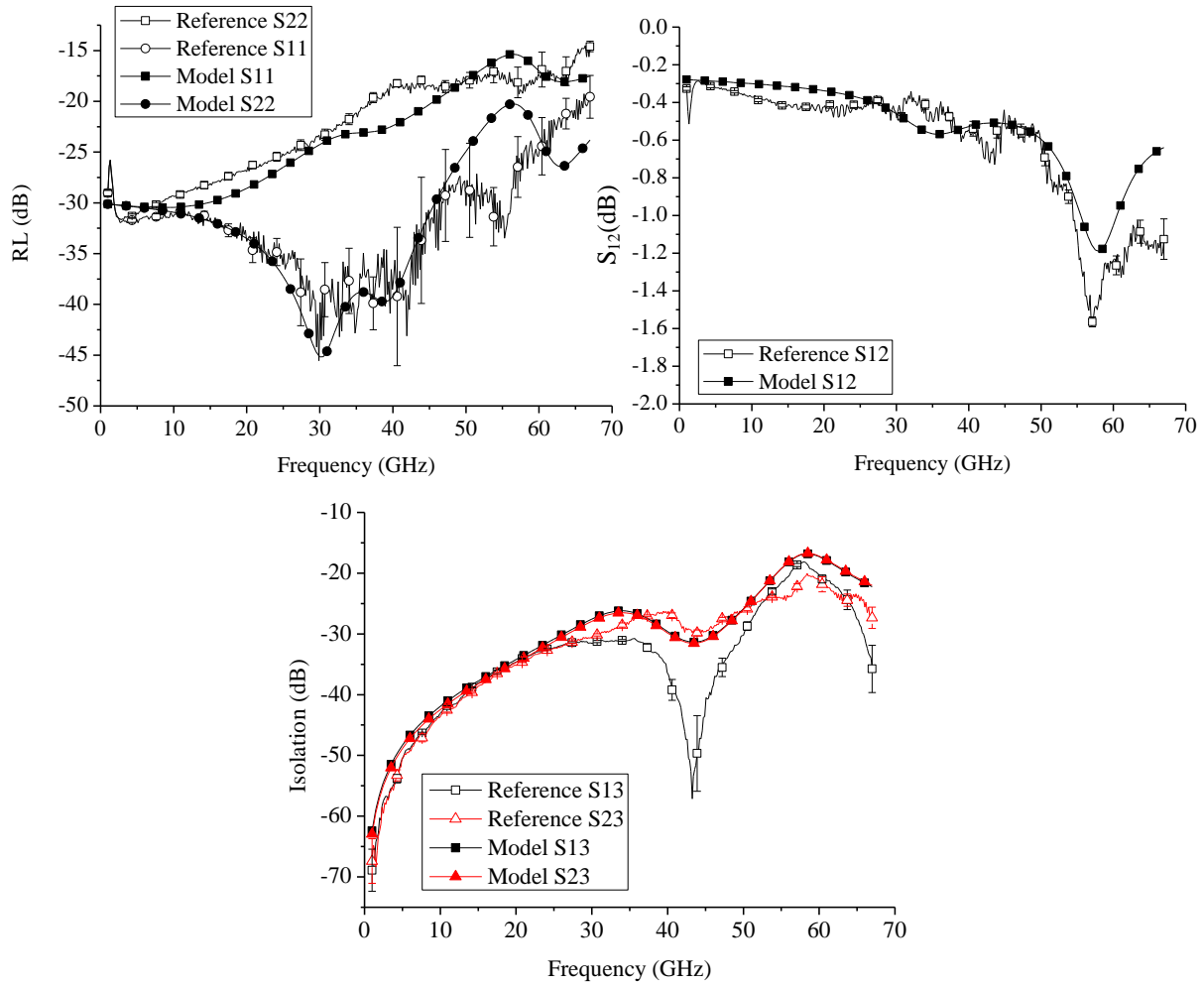


Fig. 3-23: Comparison between the measurements of the reference structures and the developed model for the line of the SPDT (without the contact zone)

3.3.2 Other routing circuits: DPDT and T-switches

The fabricated SPDT is used in the design of a DPDT (Double-Pole Double-Throw) circuit and T-switch (Fig. 3-24). The difference between both routing circuits is that in the case of the T-switch all connections between the other three ports are possible while in the DPDT each port can only be connected to two of the ports.

For the DPDT, four SPDTs, as the ones presented above, are connected by means of 90° bends. The distance between SPDTs has been optimized in terms of input matching conditions. Due to the intrinsic high isolation of the SPDTs, the desired overall isolation (50dB) is achieved for the DPDT. The design of the 90° bend is based on a mitered design. The dimensions of the CPW are 30/50/30 and the chamfered part is cut 13.75 μ m (see Fig. 3-24) over the airbridge in order to satisfy the model proposed in [78].

For the T-switch, a third path should be added to the SPDT. The design of the path is optimized taking into account the whole design of the routing node. The cross-over for the T-switch is done using the same metal as the contact region of the switch. This means that there is a distance of 0.5 μ m between the crossed lines which decreases the isolation in STATE 3 (see Fig. 3-24).

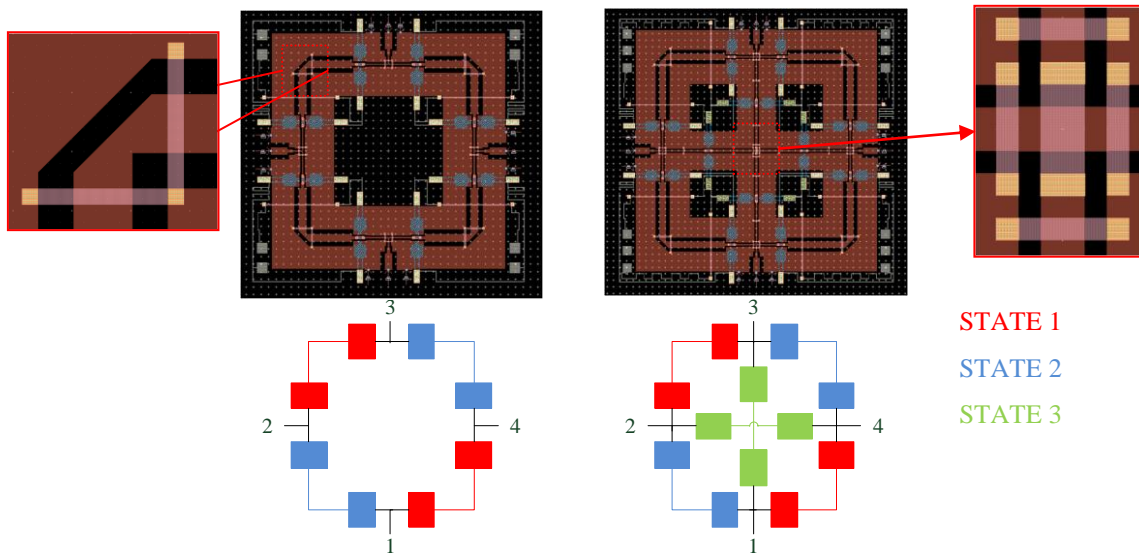


Fig. 3-24: Layout and schema of the states of the DPDT (left) and T-switch (right). Each color define the actuated switches at specific the state

The results of the simulation of the DPDT are plotted in Fig. 3-26. An input matching better than 20dB is achieved in all the ports while the insertion loss remains below 1dB from DC to 14.5GHz. The isolation goes beyond 50dB until 17GHz in adjacent ports and until 20GHz in opposite ports.

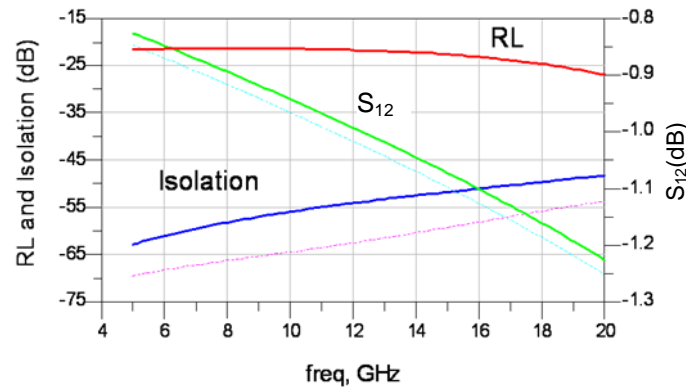


Fig. 3-25: Simulated RF performance of DPDT in state 1 and 2

In Fig. 3-26, the S-parameters of STATE 1 (or 2) and 3 are presented. In STATE 1 (or 2) the results are very similar to the ones presented in the DPDT since the structure is very similar ($RL < 20\text{dB}$, $IL > 1.5\text{dB}$ and $\text{Isolation} > 50\text{dB}$ from DC to 20GHz). On the other hand, in STATE 3 the performances are a little worse in terms of input matching, which is still better than 15dB, and insertion losses which are below 1.7dB over the entire band. In terms of isolation, a maximum of 35dB is achieved at 20GHz. This is the best result than could be obtained by a CPW cross-over using a single metal layer and airbridges.

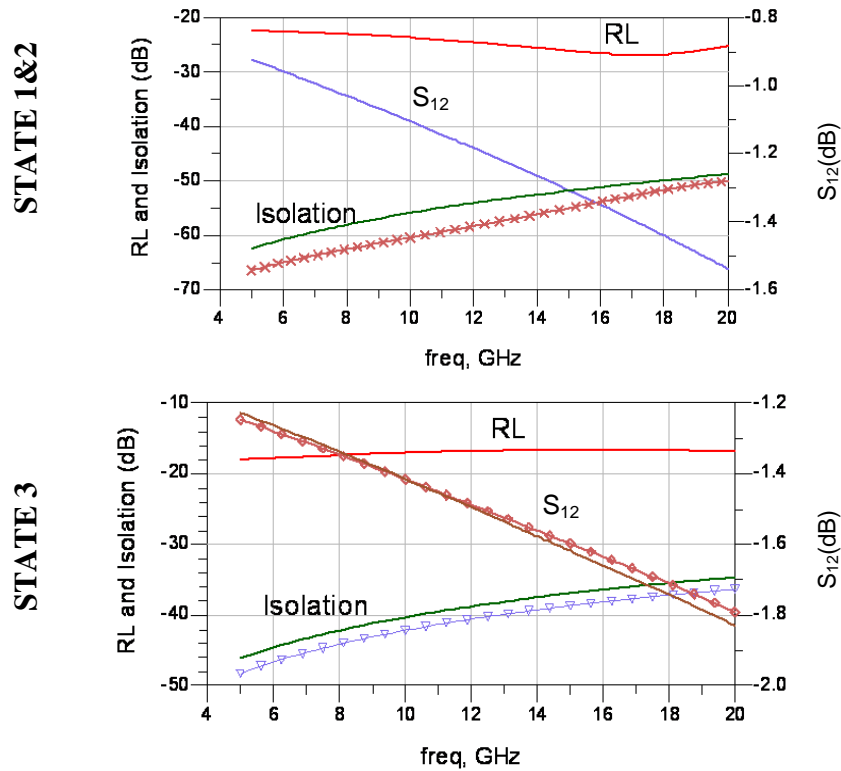


Fig. 3-26: Simulated RF performance of T-switch in state 1 and 2 (top) and 3 (bottom)

In Table 3-4 the comparison between the simulation results and the state of the art of routing switches is presented. This table shows the promising RF performance of the designed circuits. The fact that the model of the SPDT matches very well with the measurements of Fig. 3-21 suggests that the DPDT will likely do so.

DPDT (Double-Pole Double-Throw)						
	<i>This work (DC to 20GHz)</i>	<i>M. Daneshmand et R.R. Mansour (DC to 15GHz) [79]</i>		<i>S. Di Nardo et al. (DC to 40GHz) [80]</i>		
		<i>Sim</i>	<i>Meas</i>	<i>Sim</i>	<i>Meas</i>	
RL _{min} (dB)	-20	-30	-20	-30	-20	
IL _{max} (dB)	1.2	0.2	1	0.1 to 0.8	1 to 3	
ISO _{min} (dB)	-50	-70	-40	-40	-40	
T-switch						
	<i>This work (DC to 20GHz)</i>		<i>Y. Chan et al. (DC to 40GHz)[81]</i>			
	<i>State 1 and 2</i>	<i>State 3</i>	<i>State 1 and 2</i>		<i>State 3</i>	
			<i>Sim</i>	<i>Meas</i>	<i>Sim</i>	<i>Meas</i>
RL _{min} (dB)	-20	-15	-30	-20	-30	-20
IL _{max} (dB)	1.5	1.8	0.2	1	0.2	1
ISO _{min} (dB)	-50	-38	-70	-40	-45	-30

Table 3-4: Comparison of RF performance between this work (simulated) and state of the art (simulated and measured)

These circuits have not been fabricated yet since the manufacturer has decided to further stabilize his fabrication process. There are two potential main difficulties:

- The different orientation of the switches: the deposition of the membrane and contact materials would have to be controlled in both directions
- The different size of the structures in the same run: when structures (SPST, SPDT, etc.) of different sizes are included in the same wafer, it becomes very difficult control the velocity of the CPM (Chemical-Mechanical Planarisation) step of the sacrificial layer (silicon). This velocity can change in function of the local surface.

3.4 Conclusions

The CEA-Leti fabrication process has developed a very advanced solution in order to eliminate the dielectric charging problem in its electrodes. However, the long term tests have demonstrated that the degradation of the contact due to the non-hermetic packaging makes this RF performance not predictable. Despite that, it has been seen that the effect of the current through the contact should be carefully taken into account since it strongly impacts the lifetime and the burn-in time. The higher the current, the lower the number of actuations needed to reach a stable contact resistance, but, at the same time a shorter lifetime. The lumped-elements based equivalent circuit is able to describe the failure mode (creation of dielectric films on the contact) and characterize it at each lifetime time.

The implementation of a hermetic package is a must. This would allow having a large number of contamination free devices on which carry out a systematic investigation of burn-in and lifetime. Noteworthy is that the development of this hermetic package could modify steps of the fabrication process that have already been optimized and the design could be modified again.

This fabrication process approach has demonstrated to be suitable to design SPDT circuits with excellent RF performance with respect to the state of the art, from DC to 50GHz. However, more complex structures like mPnT or T-switches present further challenge for this technology since problems of stabilization and uniformity may appear. For this reason the manufacturing of the routing matrices proposed in this section have been postponed to future fabrications.

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Chapter 4

RF-MEMS in high TRL environment

4.1 Introduction

This chapter describes the IHP's embedded RF-MEMS on a standard BiCMOS process. The component approach seen in Chapter 3 is also used in this case but with the advantage of being integrated in more complex structures without any wire bonding. In fact, the niche market that this approach is aiming is for working frequencies over 50GHz where the losses in interconnections between systems play a very important role. In IHP approach no modification is allowed in the movable membrane since it was already optimized in previous research activity and it is out of the scope of the present work. Due to the five metal layers of the BiCMOS process, the design flexibility is possible and can be used for design tuning and reconfigurability.

The first RF-MEMS development in IHP was shown in [82] in 2009 where the membrane shape was optimized. As the mechanical reliability and repeatability of the process was also previously addressed, the efforts here were focused to increase the scalability and reconfigurability of the device in more complex circuits [83]. In future, the aim of IHP is to provide a RF-MEMS device library as extensive and robust as possible.

In this chapter a very accurate equivalent circuit model based on actual manufactured device has been built. Moreover, the fabrication process dispersion over the wafer has been also taken into account allowing the designer to predict possible deviations in RF performance. The model allows also to track and to identify any problem during fabrication steps and layout error. In terms of reliability, this work presents the failure mechanisms observed and how the chips can be selected for an optimal behavior under industrial requirements (Thales Alenia Space). The proposed equivalent circuit is also capable to identify the observed failure mechanisms.

This chapter begins with the description of the switch and the associated process. Secondly the developed equivalent circuit is shown and validated with a frequency scalable switch. Afterwards the deviations that directly impact the switch are studied and modeled not only in initial time but also versus time with the reliability tests. Finally, the model is used to develop a new series switch that is used for routing, phase shifting applications and a novel absorptive switch.

4.2 Co-integration MEMS-BiCMOS process (IHP)

4.2.1 Technology and switch description

The capacitive RF-MEMS switch is built between Metal2 (M2) and Metal3 (M3) of IHP's 0.25 μ m SiGe:C BiCMOS process named SG25H1 (Fig. 4-1). High-voltage electrodes are formed using Metal1 (M1), while Metal2 (M2) is used as RF signal line. The movable membrane was realized using the Metal3 (M3) layer which is an AlCu layer stacked by TiN layers on top and bottom. The thin TiN layer, which is part of the BiCMOS MIM capacitor zoomed in Fig. 4-1, forms the contact region of the switch.

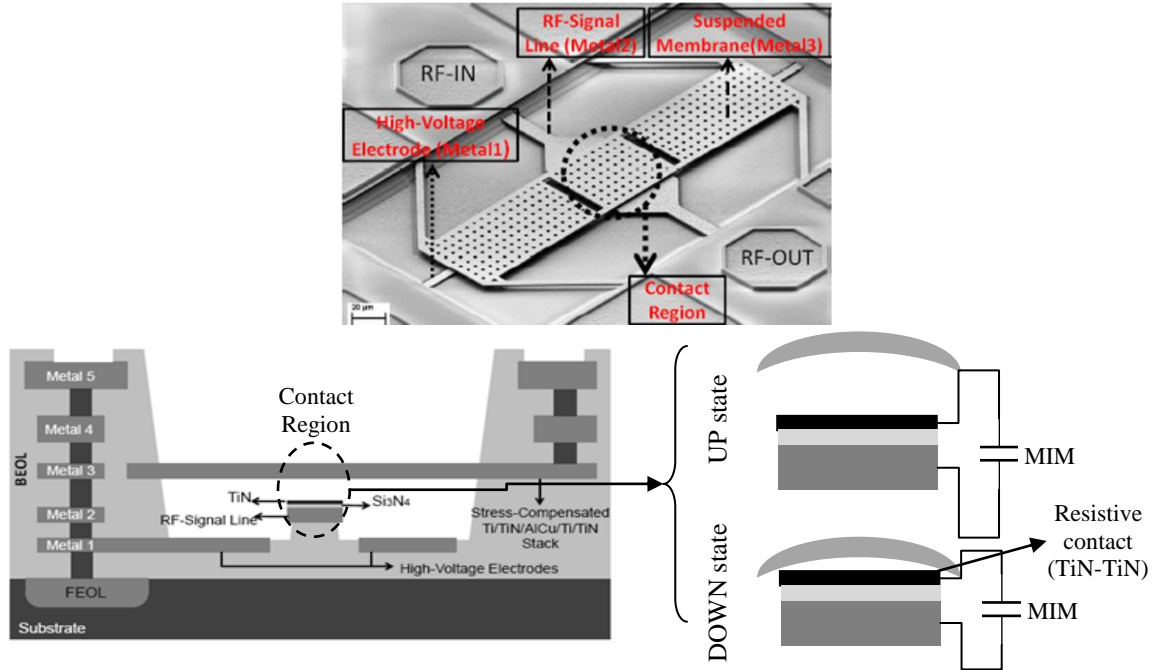


Fig. 4-1: Switch (left) and cross section (right) of the BiCMOS fabrication process

In DOWN state, the bottom TiN layer of M3 touches the TiN layer on top of the MIM dielectric. Due to the high contact resistance between the conductive TiN layers ($\sim 4\text{-}5\text{ K}\Omega$), the down-state capacitance is dominated by the air capacitance between bottom TiN of M3 and the TiN on top of Si_3N_4 . This air gap capacitance is determined by the stress gradient of M3 which has been already optimized. The MIM capacitor between M2 and the thin TiN layer on top of the Si_3N_4 layer is only used to achieve DC isolation between M2 and M3 [82]. When the switch is in UP state (OFF) the RF signal passes along the line while in DOWN state (ON) the signal line is connected to the ground providing high isolation between input and output.

Concerning the actuation voltage, 45V represents the optimal value with respect to the RF performance. This value is obtained by increasing the actuation voltage from pull-in (25V) to a value that ensures a stable contact of the membrane in down position and hence a stable value of isolation at the working frequency.

For capacitive switches, the working frequency is determined by $f_0 = \frac{1}{2\pi\sqrt{LC_{\text{DOWN}}}}$. As the air

gap capacitance in down state can be perfectly controlled, it is desirable to always use the same dimensions of membrane (i.e the same C_{DOWN}) and change L for tuning in frequency. The inductance L is determined not only by the membrane shape, but also by 4 inductors

added to the beam at the anchors location. The inconvenient of this solution is that, for low working frequency (under 60GHz), the bandwidth of the switch decreases. In Fig. 4-2 it is shown 6 switches (V1 to V6) working at different frequencies (85, 75, 65, 48, 42 GHz respectively) which have the same membrane and only change the inductance connected to the anchors.

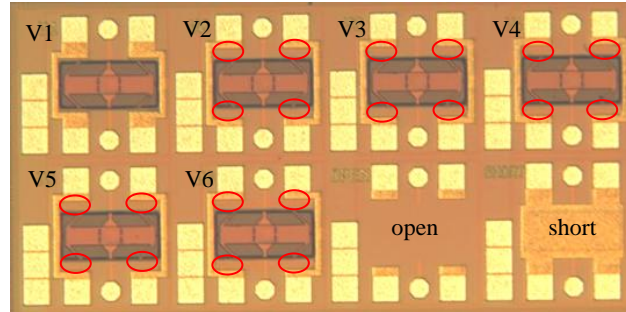


Fig. 4-2: Picture of the 6 fabricated devices at different working frequency. In red, the area occupied by the inductors added for tuning frequency. Open and short are used for de-embedding the RF pads

In Fig. 4-3 the RF measurements of the different versions of the switch (V2 to V6) are shown. These switches present in DOWN state a double resonance: one due to the inductors added at the anchors (main resonance) and another (electrode resonance) due to the capacitance between the membrane and the electrodes, and the inductance of the bias lines. This second resonance does not change with the design because the bias network is always the same.

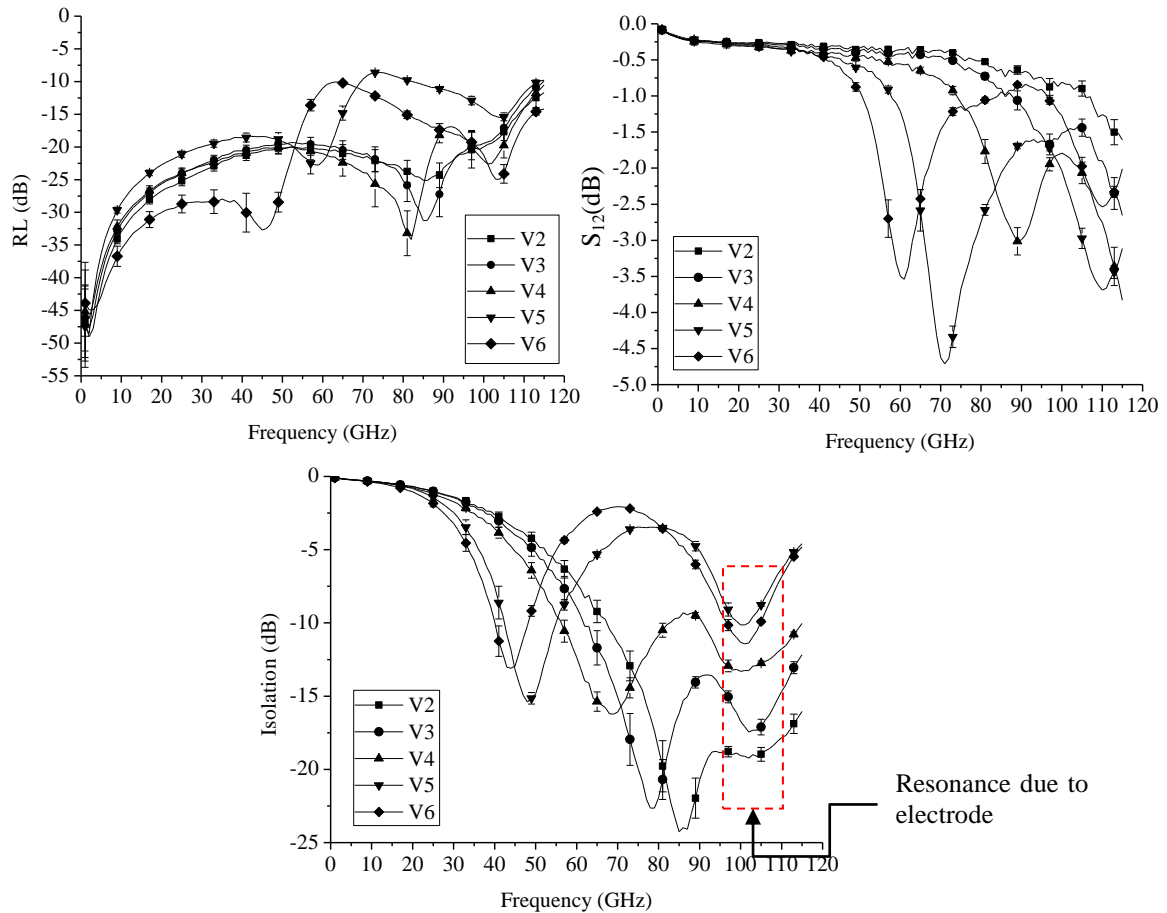


Fig. 4-3: Measured RF performance of the different versions of the switch

When comparing the RF performance of the different switches (Table 4-1) it is seen that, as expected, the higher the resonance frequency, the larger is the bandwidth¹⁵. The bandwidth is also increased by the effect of the second resonance in the switches above 70GHz (V2 and V3).

Parameter	Version of the switch				
	V2	V3	V4	V5	V6
Freq (GHz)	85	75	65	48	42
BW (GHz)	20	15	14	7.8	8
RL	20dB	25dB	30dB	20dB	25dB
IL	0.6dB	0.4dB	0.6dB	0.4dB	0.7dB
Isolation	24dB	19dB	17dB	15dB	12dB

Table 4-1: Measured RF performance of the switches at the working frequency

Equivalent circuit description

A scalable lumped-elements model is proposed for the different switches working at different frequencies presented above. The difference between the switches lies only in the inductance added at the anchors of the switch. In the proposed model, only this inductance is modified in order to tune the desired working frequency. The importance of the proposed model is that all the lumped-elements are associated to a constitutive part (shape and size) of the device, which provides a complete and detailed electrical description. This allows to trace back and to detect possible manufacturing flaw or deviation due to technological dispersion. In addition, it provides information about the quality of the fabricated devices since which can be directly correlated with the performance of the device.

In Fig. 4-4 a cross section of the switch is shown identifying the different lumped elements of the model. Regarding the down state position, it is important to note that the down state capacitance is known with accuracy since the value of the MIM capacitor (stack of Al(M2)/Si₃N₄/TiN) under the contact is always the same and the stress on the membrane is controlled in order to achieve always the same deformation. Due to the shape of the deformation (Fig. 4-4 right), the membrane contacts the top electrode of the MIM capacitor only at the corners of the contact zone (modeled by a high resistance R_{contact}) creating an air gap (C_{MEMS}) [82]. Therefore, one of the most critical issues of capacitive switches, the repeatability of the down capacitance, is counteracted by using this technique.

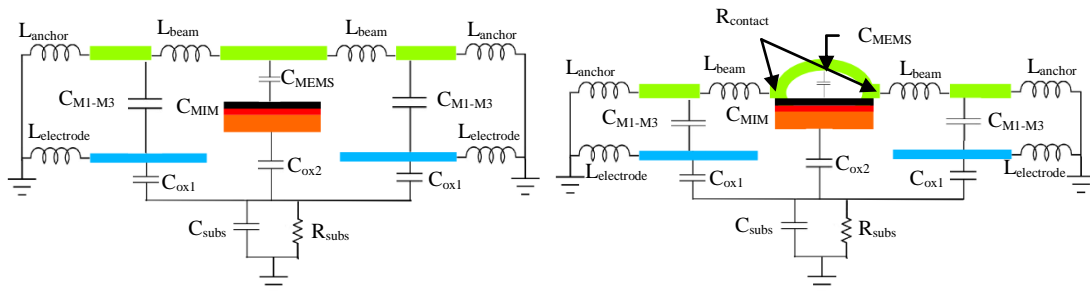


Fig. 4-4: Schematic modeling of the switch at the MEMS cross section for UP (left) and DOWN (right) state: membrane M3 (green), line M2 (orange), electrodes M1 (cyan), dielectric of the MIM capacitor (red) and top electrode of the MIM capacitor (black)

Since the membrane (M3) and the RF signal (M2) are at the same electrical potential, it avoids any dielectric charging phenomena at the contact zone. Moreover, between the

¹⁵ Bandwidth is computed using +/-20% the maximum isolation

electrode and the membrane there is no dielectric. This means that the switch is robust in terms of dielectric charging despite suffering from other failures as it will be discussed in section 4.2.2.

Transmission Line Modelling

The transmission line is a RLCG model combined with a substrate coupling network well-known in the BiCMOS process modeling. The reason of using this approach is due to its simplicity in being used in network simulators (Spice) and the substrate losses already known can be easily added. The values of each parameter of the substrate coupling network (C_{ox2} , R_{subs} and C_{subs}) are deduced from the process specifications as

$$C_{ox2} = A_{line} \cdot C_{M2-sub} = 280 \mu m^2 \cdot 10 \frac{aF}{\mu m^2} = 2.8 fF$$

$$R_{subs} = \frac{\epsilon_r \epsilon_0 \sigma_{Si}}{C_{subs}} = 405 \Omega$$

$$\epsilon_r = 11.9 \quad C_{subs} = 170 fF \quad \sigma_{Si} = 0.5 \Omega m$$
Eq. 4-1

where C_{M2-sub} is the coupling from Metal 2 to substrate per μm^2 (defined by the process), A_{line} is the surface of the line, C_{subs} is measured and σ_{Si} is the resistivity of the substrate. In Fig. 4-5 the lumped elements based model of the line is superposed to the layout. R, L and C are deduced from standard modeling of CPW [84].

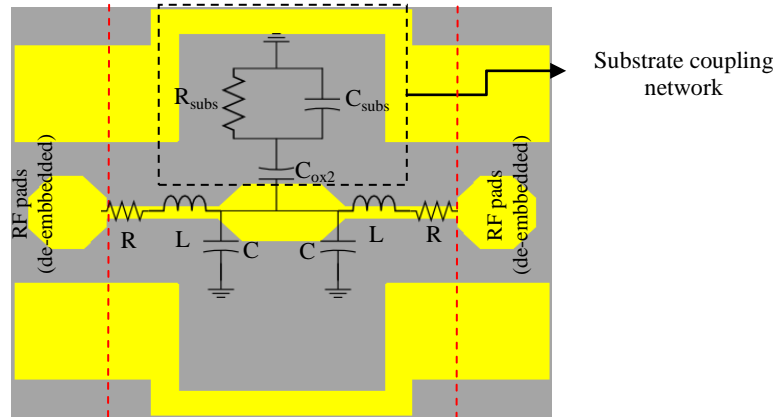


Fig. 4-5: Lumped-elements based model of the Transmission Line

In Fig. 4-6 the comparison between the model and the measurements are plotted showing an excellent agreement in amplitude and phase. The other relevant result that this structure gives is the possibility of computing the phase of the structure.

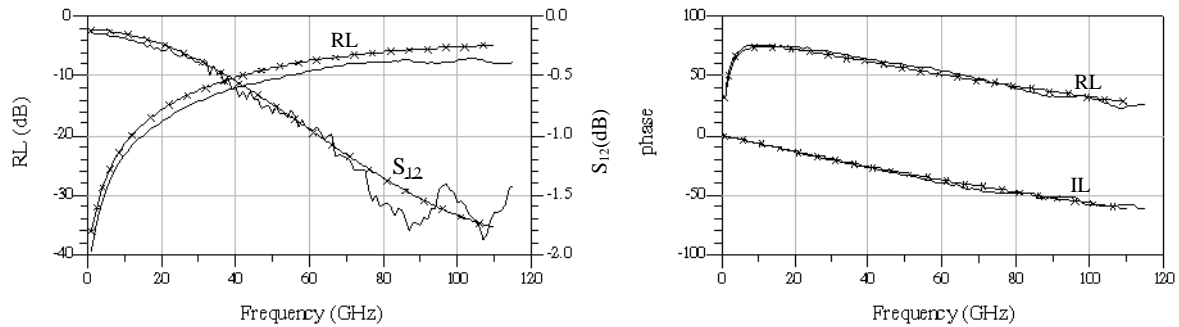


Fig. 4-6: Comparison between model (cross) and measurements

Inductance modelling (L_{anchor})

As it is explained above, the scalability of the switch is done by varying the L_{anchor} inductance. For this reason its modeling is also a key issue in order to predict the resonant frequency. This has been done by combination of EM simulation (Sonnet) and lumped-elements based circuit of inductances [85]. Due to the small size of the inductors, it is very difficult to extract very accurate results since the RF probes are very close (cross coupling starts to be significant). Moreover, the de-embedding of the RF access lines could be also critical (the measured results can be in some range of magnitude than the RF access effect). The EM simulation model (Fig. 4-7) takes into account the conductor (mainly skin effect) losses and substrate effect.

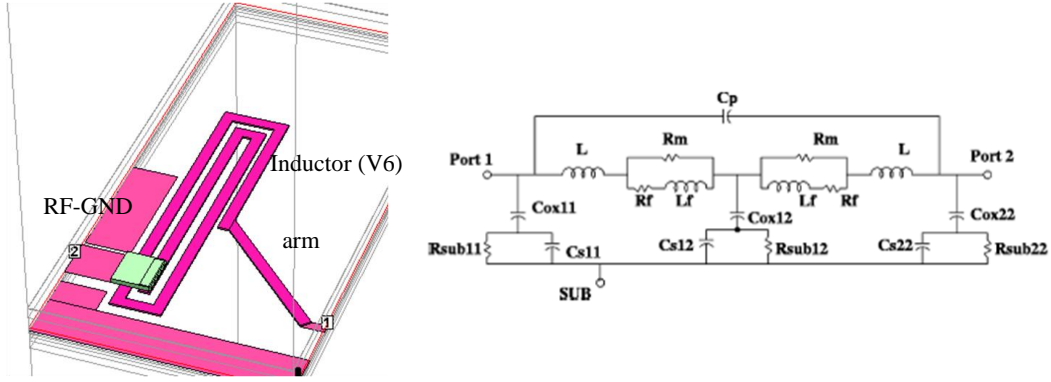


Fig. 4-7: Sonnet model of L_{anchor} (left) and used lumped-elements circuit (right) extracted from [85]

The parameters associated to the substrate ($C_{\text{ox}i,j}$, $R_{\text{subs}i,j}$, $C_{s,i,j}$) are extracted following the formulas proposed in [85] while the other parameters (C_p , L , R_m , R_f and L_f) are fitted with the EM simulation. In Fig. 4-8 the comparison between the EM simulation and the lumped-elements model of the inductance is compared showing excellent agreement with L_{eff} and Q using Y-parameters of each model (EM and lumped elements) where

$$L_{\text{eff}} = \frac{1}{2\pi f Y_{11}} \quad Q = \frac{\Im\{Z_{11}\}}{\Re\{Z_{11}\}} \quad \text{Eq. 4-2}$$

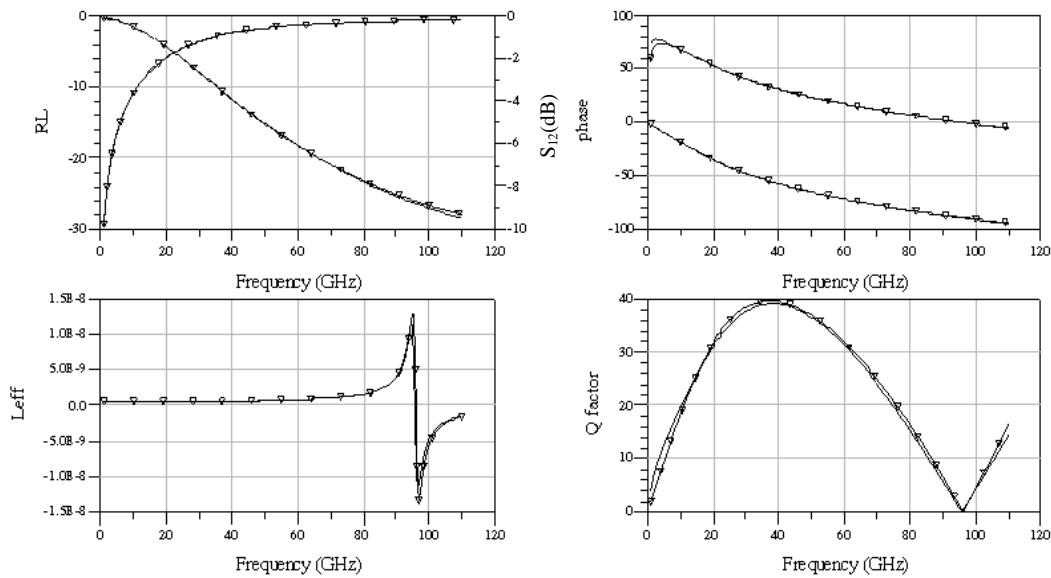


Fig. 4-8: Comparison between EM model and lumped elements model (triangle)

This method is used for the 6 different types of switch (V2 to V6) and the parameters are depicted in Table 4-2. These same values will be added to the MEMS model by adjusting C_p and $C_{ox,i,j}$, which can be affected by the etching step hence change the coupling through the substrate.

	C_p (fF)	L (pH)	R_m (Ω)	R_f (Ω)	L_f (pH)
V2	1.2	40	0.7	3	23
V3	2.2	59.5	2.2	3	19.4
V4	0.3	91.5	5.4	8.1	70
V5	1.4	197	5	8.1	70
V6	0.3	255.8	5.8	8.1	70

Table 4-2: Parameters of the elements for the different inductors

MEMS modelling

In Fig. 4-9 the schematic of the switch is presented. This equivalent circuit is based on two parallel resonant circuits. The main resonance which determines the working frequency is due to the down state capacitance and the inductors in the arms of the switch (C_{MEMS}^{DOWN} and L_{anchor}). The secondary resonance is associated to the capacitance between the membrane and the electrodes, and the inductance of the bias lines (C_{M1-M3}^{DOWN} and $L_{electrode}$). In both cases, an additional series resistor is added in order to compute the losses of the inductors (R_{anchor} and $R_{electrode}$).

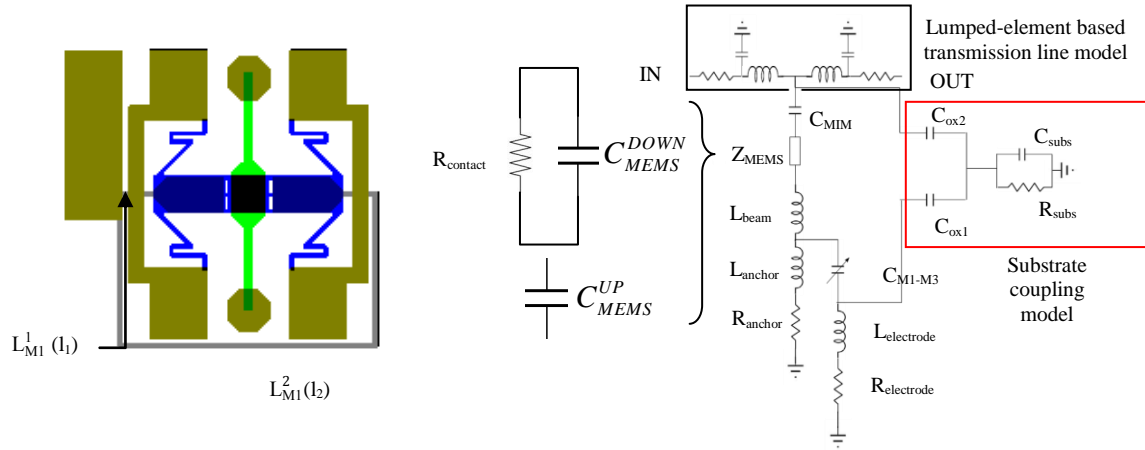


Fig. 4-9: Lumped-elements based model of the switch with the substrate coupling network (red) and the model of the transmission line (black). Z_{MEMS} is the contact zone model in UP and DOWN state

In terms of UP/DOWN capacitance (C_{MEMS}), this value is extracted from $C(V)$ measurements ($C_{MEMS}^{up}=20\text{fF}$ and $C_{MEMS}^{down}=128\text{fF}$), while the MIM capacitor (C_{MIM}) has a value of 2.5pF . The most challenging part to model is the secondary resonance which occurs due to the coupling between the movable membrane (M3) and the high-voltage electrode (M1). This C_{M1-M3} cannot be measured accurately as it was done with C_{MEMS} . For this reason, a parallel plate's formula is used for the UP state capacitance and then tuned to match the measurements (Eq. 4-3). The UP/DOWN ratio of C_{M1-M3} is also theoretically extracted using the distance between the different metal layers in each state (d_{M1-M3}^{up} and d_{M1-M3}^{down} in Eq. 4-4). Finally, $L_{electrode}$ is

computed using the inductance of the bias line (L_{M1}). Depending on the length of the line the obtained range of values for L_{M1} goes from 1.1pH/ μm to 1.3pH/ μm . Noteworthy is that there are two electrodes whose bias lines have different lengths (l_i), so the value $L_{\text{electrode}}$ is the equivalent inductance between the two bias lines (L_{M1}^1 and L_{M1}^2) (Eq. 4-5).

$$C_{M1-M3}^{\text{up}} = \frac{\varepsilon_0 A_{\text{contact}}}{d_{M1-M3}^{\text{up}}} \quad \text{Eq. 4-3}$$

$$\frac{C_{M1-M3}^{\text{up}}}{C_{M1-M3}^{\text{down}}} = \frac{d_{M1-M3}^{\text{down}}}{d_{M1-M3}^{\text{up}}} \quad \text{Eq. 4-4}$$

$$L_{\text{electrode}} = \frac{L_{M1}^1 L_{M1}^2}{L_{M1}^1 + L_{M1}^2} \quad L_{M1}^i = L_{M1} l_i \quad \text{where } i = 1..2 \quad \text{Eq. 4-5}$$

In Fig. 4-10 the measured RF performance of all the presented switches (V2 to V6) is compared with the model adapted with its corresponding L_{anchor} value. The measurement results were taken over an 8-inch wafer for more than 50 samples, therefore also shows the dispersion of the RF performance over the wafer. These results show very good agreement between model and measurements within the entire frequency band (30-110GHz). The values considered for a perfect fitting are resumed in Table 4-3 and they also agree with the expected ones.

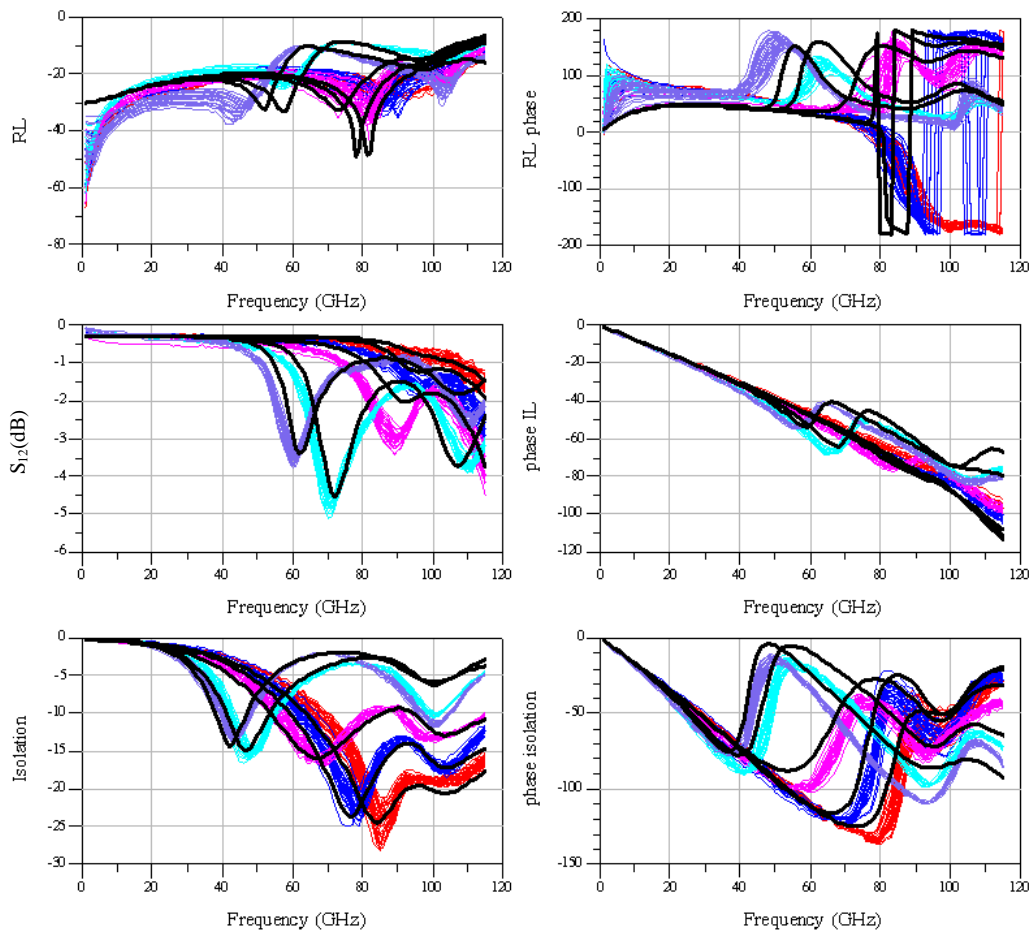


Fig. 4-10: Measured RF performance (colored) and model (black): V2 (red), V3 (blue), V4 (pink), V5 (cyan) and V6 (purple)

Variable parameters for different versions of the switch			
Version	Frequency	L_{anchor}^{16}	R_{anchor}
V2	85GHz	75.7 pH	1.8Ω
V3	75GHz	96 pH	2.9Ω
V4	65GHz	135 pH	3.63Ω
V5	48GHz	255 pH	7.1Ω
V6	42GHz	287 pH	7.1Ω
Constant parameters for all the switches			
	UP state	DOWN state	
C_{MEMS}	20fF	130fF	
$C_{\text{M1-M3}}$	12.76fF	22.16fF	
$L_{\text{electrode}}$		130pH	
L_{beam}		11.1pH	

Table 4-3: Values of the parameters of the analyzed switches

4.2.2 Impact of fabrication process and reliability tests

The fact that the RF-MEMS device is based on a standard BiCMOS process has a dual opposite consequence: On one hand, the dispersions due to the size of the elements and the roughness of the layers are completely known and controlled which makes the variations negligible. On the other, the design of the switch is limited by the constraints of the process. In this specific case there are two limitations: 1) The TiN-TiN contact between the top electrode of the MIM capacitor and the membrane, 2) The higher losses due to the low resistivity substrate. By keeping into account these limitations, the design of the switch has been optimized in order to avoid dielectric charging on the contact zone by using deported electrodes.

Process tolerance characterization

Even if the switches are identical, the RF performance varies over the wafer. In the case of the BiCMOS process used in this section, the geometrical dispersion is negligible as far as RF performance is concerned.

However, due to nm-range thickness variations and the non-uniform deposition of the metals, the stress gradient of the suspended membrane varies over the wafer changing the distance between metals (aprox. 4%) which yields significant variation (5-6%) on the MEMS capacitance (C_{MEMS}) in both states. The same stress variation also affects directly the membrane to high voltage electrode capacitance ($C_{\text{M1-M3}}$) which turns out to be responsible of the device bandwidth. It is therefore apparent that the understanding of these two capacitances, and their variation, enables the direct monitoring of the device RF behaviour. In Fig. 4-11 a histogram of the measured losses and isolation at 85GHz (V2) is plotted showing the RF performance deviation over the wafer for this BiCMOS process.

¹⁶ This value correspond to the effective inductance parameter (L_{eff}) of the equivalent circuit model

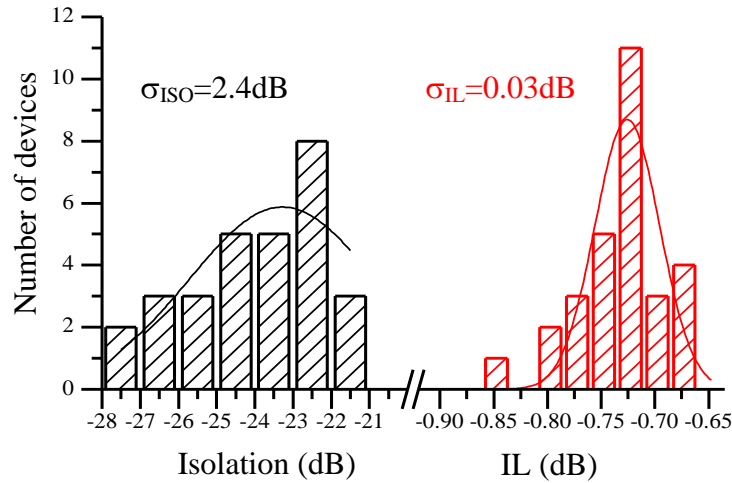


Fig. 4-11: Histogram of isolation (black) and insertion losses (red) measurements at 85GHz

In order to verify the dependency between RF deviation and C_{MEMS} variation, LF measurements (1MHz) using Agilent 4294A Precision impedance analyzer of the UP and DOWN state capacitance (C_{MEMS}) are done. The same devices removing the parasite capacitances of substrate and C_{MIM} by means of de-embedding structures (transmission lines without membrane) are used. These measurements show a Gaussian distribution from the mean value in both states (Fig. 4-12).

Noteworthy is that the relation between, C_{M1-M3} and the RF performance can only be established by using the equivalent circuit since this capacitance cannot be measured experimentally. In order to be measured it would need extra test structures in order to de-embed the coupling effects with other metal layers. These extra structures do not allow the real time monitoring. For this reason, C_{M1-M3} is extracted from the model by exploiting the parallel plate capacitance formula to get a rough first estimation followed by more exact identification by curve fitting of the isolation around the secondary resonance.

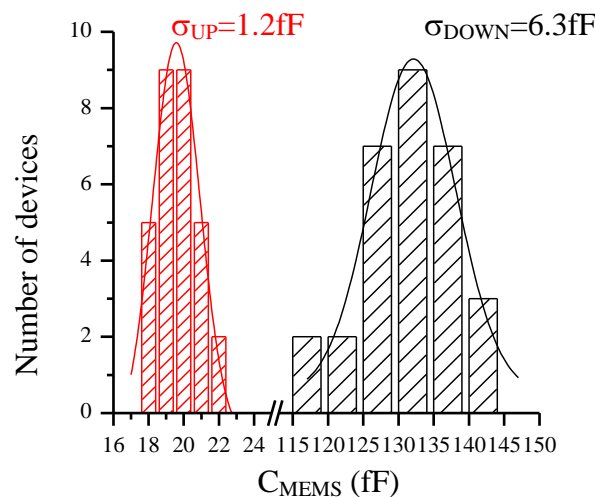


Fig. 4-12 Histogram of C_{MEMS} measurements for UP (red) and DOWN (black) state with the Gaussian distribution function

Fig. 4-11 and Fig. 4-12 demonstrate that the tracking of the C_{MEMS} capacitance during the fabrication process is a key issue since it has a direct impact on the RF performance. A small

deviation of 4.8% from the mean value (130fF) in this capacitance implies 10% of change in the isolation which is a criterion that the designer should take into account during the design phase in order to compensate this possible variation (Design for Reliability). This relationship is also useful to screen over the entire wafer to define the yield of the process and to locate the best yield area on the wafer.

By applying the computed deviations to the lumped-elements circuit model shown above, the effect of the fabrication deviation can be reproduced in the entire band. A Monte Carlo analysis of the model with 50 trials is done with the parameters in Table 4-4 and compared with the measurements of the 50 devices showing very good agreement (Fig. 4-13).

	UP		DOWN	
	<i>Mean</i>	σ	<i>Mean</i>	σ
C_{MEMS}	21fF	1.2fF	131fF	6.3fF
$C_{\text{M1-M3}}$	12fF		19fF	

Table 4-4: Parameters used for the MonteCarlo analysis

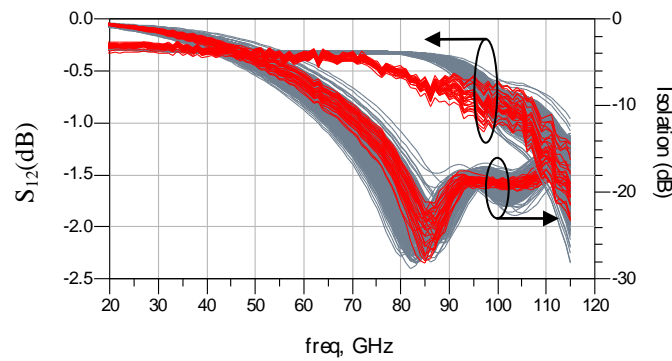


Fig. 4-13 Comparison between the MonteCarlo Analysis (grey) of the model and the measurements (red)

From the LF measurements to RF performance

The model introduced earlier is here used to show the effects of the technology dispersion, which translates into a deviation of the C_{MEMS} , and hence on the RF performance. In Fig. 4-14 the isolation and insertion losses at three different frequencies, are computed for different values of C_{MEMS} (range taken within typical process dispersion).

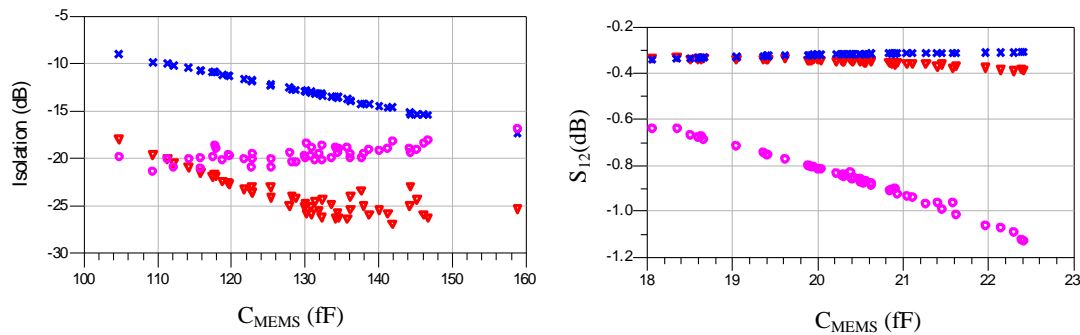


Fig. 4-14 Relation between C_{MEMS} in DOWN state and isolation (left) and S_{12} (right) predicted by the model at three different frequencies: 70GHz (cross), 85GHz (triangle) and 100GHz (circle)

The presented approach offers a twofold advantage: 1) From the RF designer point of view, this model allows to account for the deviations of the technological parameters of simple switches as well as more complex circuits (Design for Reliability). 2) From the process developer point of view, it allows real time correlation between the overall design performance and the actual technological implementation. These advantages reside in the capability to get full RF performance from real-time capacitance LF measurement hence avoiding cost-intensive and time consuming RF test procedures.

Lifetime of the switch

Once the initial performance is checked regarding the fabrication process deviations, the next step is to study how they are going to evolve with time. There are two key issues that are studied in these tests:

- How different degradation signs occur in capacitive MEMS and how they impact the RF performance. In case of unavoidable failure this allows to check whether the device still respects the given application performance.
- Which one of the observable parameters is relevant with respect to the failure detection at wafer level.

The 8-inch wafer is divided in cells within which the switches are replicated (Fig. 4-15). The size of the cell has been previously established and studied by IHP. One quarter of wafer is used for the presented results since horizontal and vertical symmetry is supposed in manufacturing. The availability of this huge amount of devices allows the monitoring of the process dispersion regarding the reliability of the device thus the yield under desired specifications (Thales Alenia Space in this case).

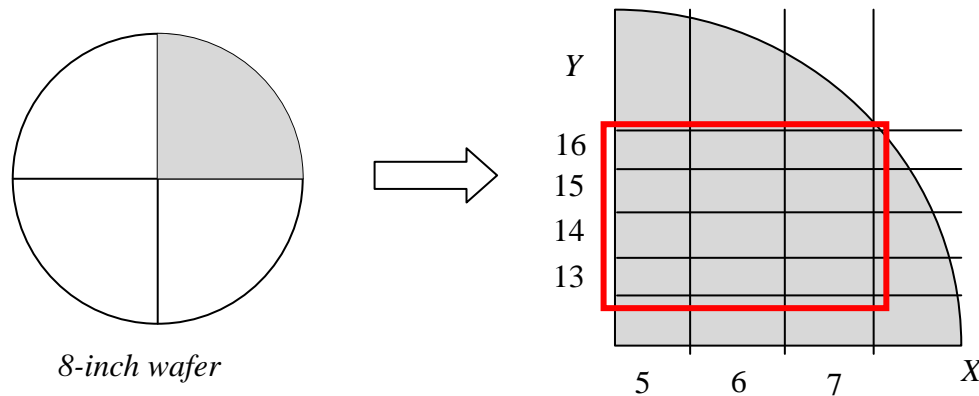


Fig. 4-15: Cells of the quarter wafer used for the reliability tests. X and Y are used in order to identify the device position

Test protocol

Test protocol developed by S. Mellé [86] and currently used by Thales Alenia Space for industrial requirements as was shown in [87]. The tests conditions are depicted in Fig. 4-16 for both types of tests. Actuation voltage is fixed to 40V for continuous and cycling stress while for $|S_{12}(V)|$ measurement, the voltage is extended until 60V (limit to avoid contact between membrane and electrodes which leads to stiction). The RF behaviour of the switch, from 25 to 65GHz, is also measured at the beginning and at the end of each test.

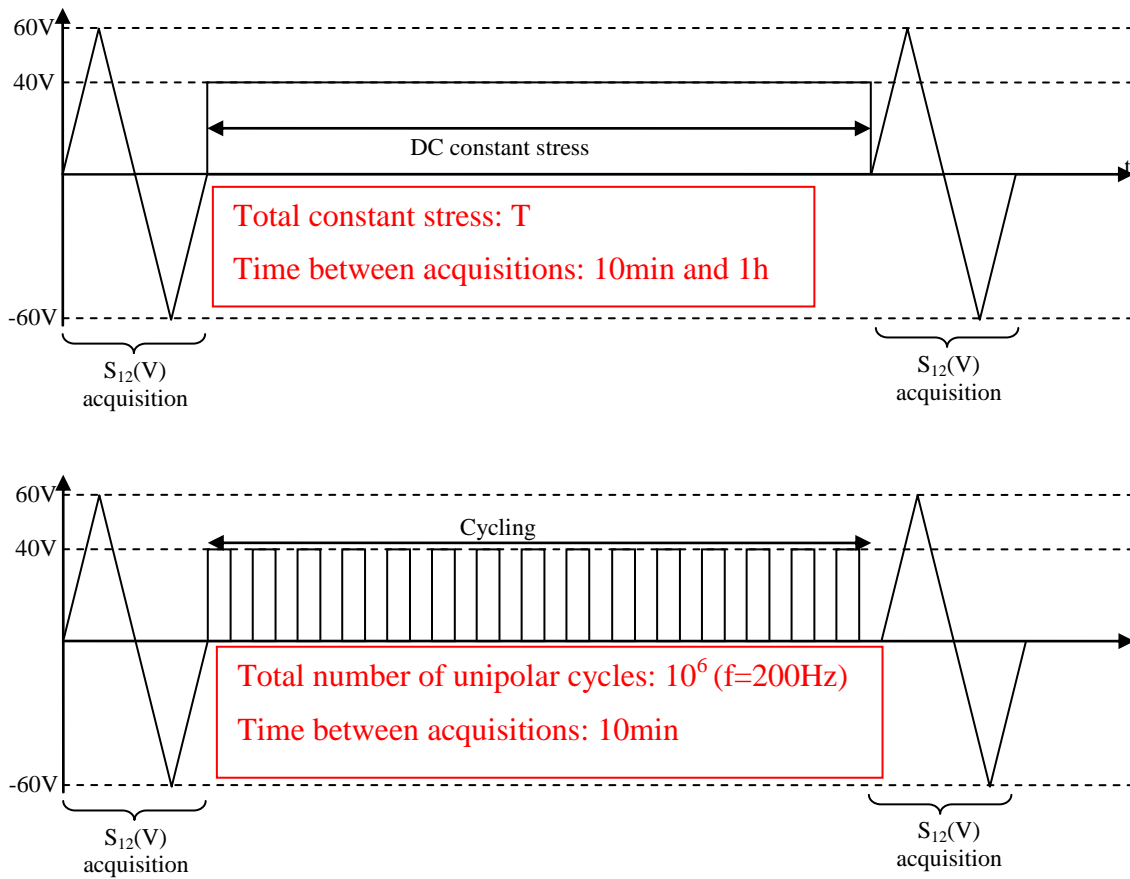


Fig. 4-16: Test protocol for DC constant stress (top) and cycling (bottom) between two measurements.

Regarding the application, two main tests are considered: constant DC stress and cycling. The first one consists on actuating continuously during an established time checking its RF performance periodically. The DC stress test simulates the worst case regarding the dielectric charging. The second test is used to see if the contact resistance between the membrane and the MIM capacitor has an influence on RF performance.

The setup is the same than the one used in contact repeatability study in Chapter 3 but, in this case, the $|S_{12}(V,t)|$ parameter is used to track the switch evolution instead of $S_{12}(t)$. The values of V_{PIN} and V_{POUT} have been measured by means of $S_{12}(V)$ measurements and not using the $2/3 \cdot g_0$ criteria since, as it will be seen later, the DOWN state position is reached below the mechanical V_{PIN} computed with the $2/3 \cdot g_0$ criteria.

I have done these tests in Thales Alenia Space facilities in Toulouse using their own MEMS test protocol for MEMS qualification for space applications defined in Mellé's PhD dissertation [55]. The tests have been carried out in an open-environment at 23°C and 45% of humidity in order to consider a harsh environment. Since all devices are based on the identical MEMS actuation principle and design (as mentioned above only the inductance at the anchors change between designs) the electromechanical test will be identical for all of them. Due to constraints in terms of frequency range for the measurement setup, only the switches working at 30, 40 and 50GHz were selected. The tests specified in Table 4-5 were assigned randomly.

Switch ¹⁷	Test	Failure criteria	
		$\Delta V_{pull-in}$	$\Delta IL_{max} (dB)$ ¹⁸
X5_Y13_50G	DC stress 1h	10%	1dB
X5_Y14_30G	DC stress 1h	10%	1dB
X5_Y14_50G	DC stress 1h	10%	1dB
X5_Y15_50G	DC stress 1h	10%	1dB
X5_Y16_50G	DC stress 14h	20%	2dB
X5_Y16_30G	DC stress >24h	20%	2dB
X5_Y13_40G	Cycling	10%	1dB
X5_Y14_40G	Cycling	10%	1dB
X5_Y15_40G	Cycling	10%	1dB
X5_Y16_40G	Cycling	10%	1dB

Table 4-5: Test done at each switch with the considered failure criteria

Results of DC stress test

In Table 4-6 the results of the DC stress tests are shown. Regarding the 1h tests, there are two devices (X5_Y13_50G and X5_Y14_30G) that collapsed during the test and the others did not reach the expected specifications. A mean deviation of the pull-in and pull-out of 14.5% and 22% respectively is achieved in 1h stress devices. However, the insertion losses remain very stable (0.015dB of mean deviation). When increasing the duration of the test, for example to 14h or 67h¹⁹, it is seen that the pull-in voltage do not vary with respect to the 1h test. On the other hand, the losses increase a little bit more (1dB in mean).

Switch	T(h)	Pull-in (V)			Pull-out (V)			IL (dB)		
		Initial	Final	Δ	Initial	Final	Δ	Initial	Final	Δ
X5_Y13_50G	1	30	0	100%	26	0	100%	1.1	6.5	5.4
X5_Y14_30G	1	34	29	14.7%	20	6	70%	0.86	1.26	0.4
X5_Y14_50G	1	33	27	18.1%	29	20	31%	0.99	1	0.01
X5_Y15_50G	1	37	33	10.8%	33	29	12%	0.99	0.97	0.02
X5_Y16_50G	14	37	32	13.5%	32	22	31%	0.79	1.22	0.43
X5_Y16_30G	67	37	34	8.1%	34	28	18%	0.8	2.6	1.8

Table 4-6: Variation of pull-in, pull-out and IL during the DC stress test

Comparing the RF performance of the switch X5_Y15_50G before and after the test in both states (Fig. 4-17 right) shows a clear correlation with the deviation on the pull-in/out voltage observed in Table 4-6. Since the design has been conceived to avoid charging in the contact area, the main reason of this variation is attributed to the mechanical relaxation of the membrane. These deviations imply:

¹⁷ $X_n_Y_m_XXG$ stands for position (n,m) over the wafer (Fig. 4-15) and XX the working frequency in GHz

¹⁸ Losses are computed at central frequency which is specified in the switch nomenclature by XX GHz

¹⁹ These values correspond to one night and one weekend of continuous test. They are not under any standard protocol

- 1) The decrease of the UP state capacitance which changes the characteristic impedance of the line increasing the losses.
- 2) The increase of the DOWN state capacitance which leads to a decrease of the resonance frequency.

The pull-in/out drift is seen in $|S_{12}(V)|$ (Fig. 4-17 left) where the pull-in voltage decreases due to the lowering of the membrane yielded by the mechanical relaxation, on top of the electrodes. Using the equivalent circuit described in section 4.2.1, it has been possible to observe that a variation about 10% and 9% in the DOWN and UP capacitance respectively is achieved during the first hour of test.

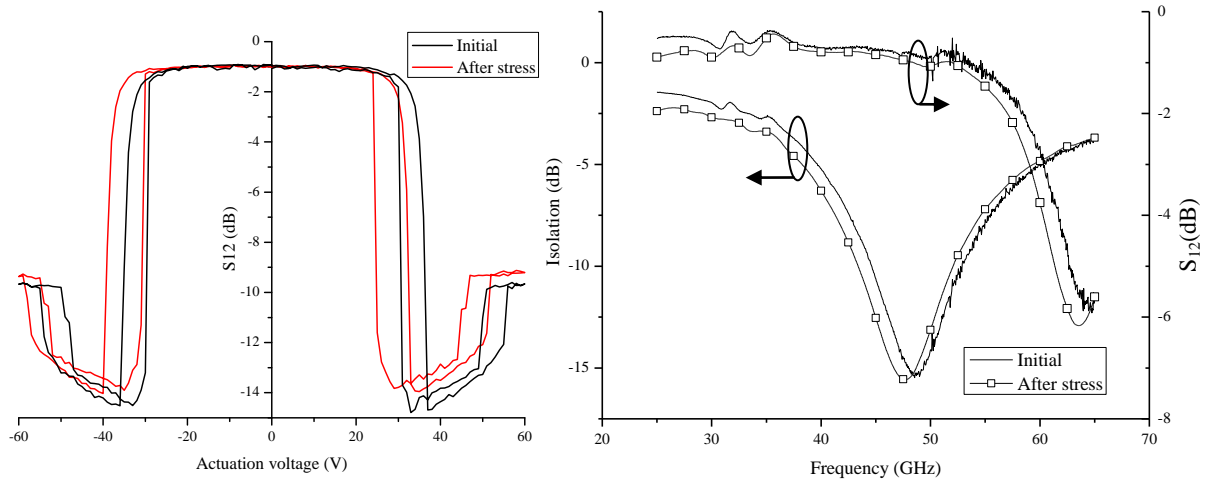


Fig. 4-17: $S_{12}(V)$ at 50GHz (left), isolation and IL (right) of the switch X5_Y15_50G before and after the DC stress during 1h at 40V

In order to see if this variation is only a transient effect, longer tests (14h and 67h) are carried out. The results in Table 4-6 show variations in the pull-in voltage in the same range (12 and 8% respectively) with respect to 1h tests. In Fig. 4-18 the $|S_{12}(V)|$ before and after stress shows also that the losses increase because the membrane do not recover the initial position due to the relaxation.

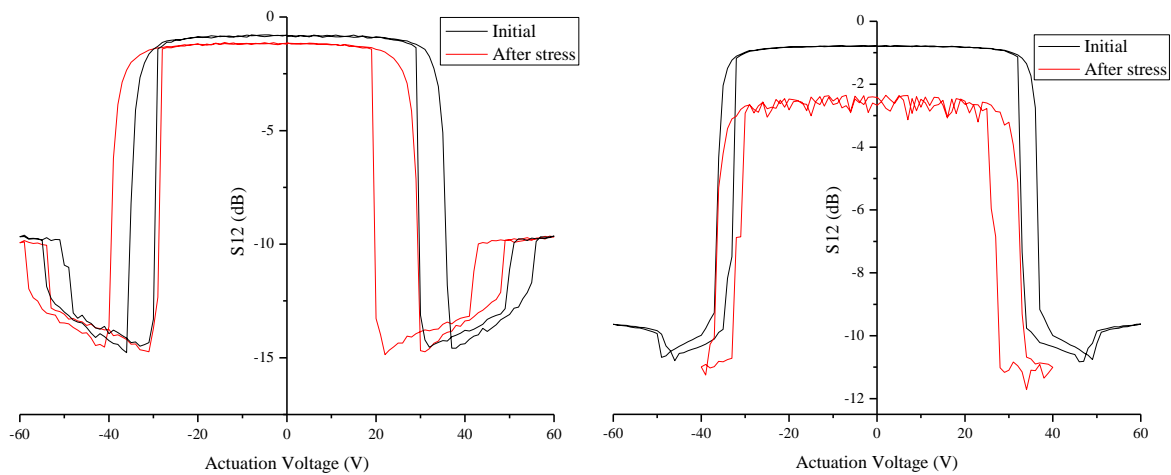


Fig. 4-18: $S_{12}(V)$ for constant DC stress of 14h (X5_Y16_50G) (left) and 67h (X5_Y16_30G) (right)

In Fig. 4-19 the S-parameters before and after the test are also compared. In the case of X5_Y16_50G there is a very small variation while in X5_Y16_30G a small resonance

appears at 30GHz which increase the losses only in this frequency (already seen in Fig. 4-18 right). The same behaviour at the same frequency was observed in X5_Y14_30G and in X5_Y14_50G but in this second case it is not affecting the RF performance in the working frequency.

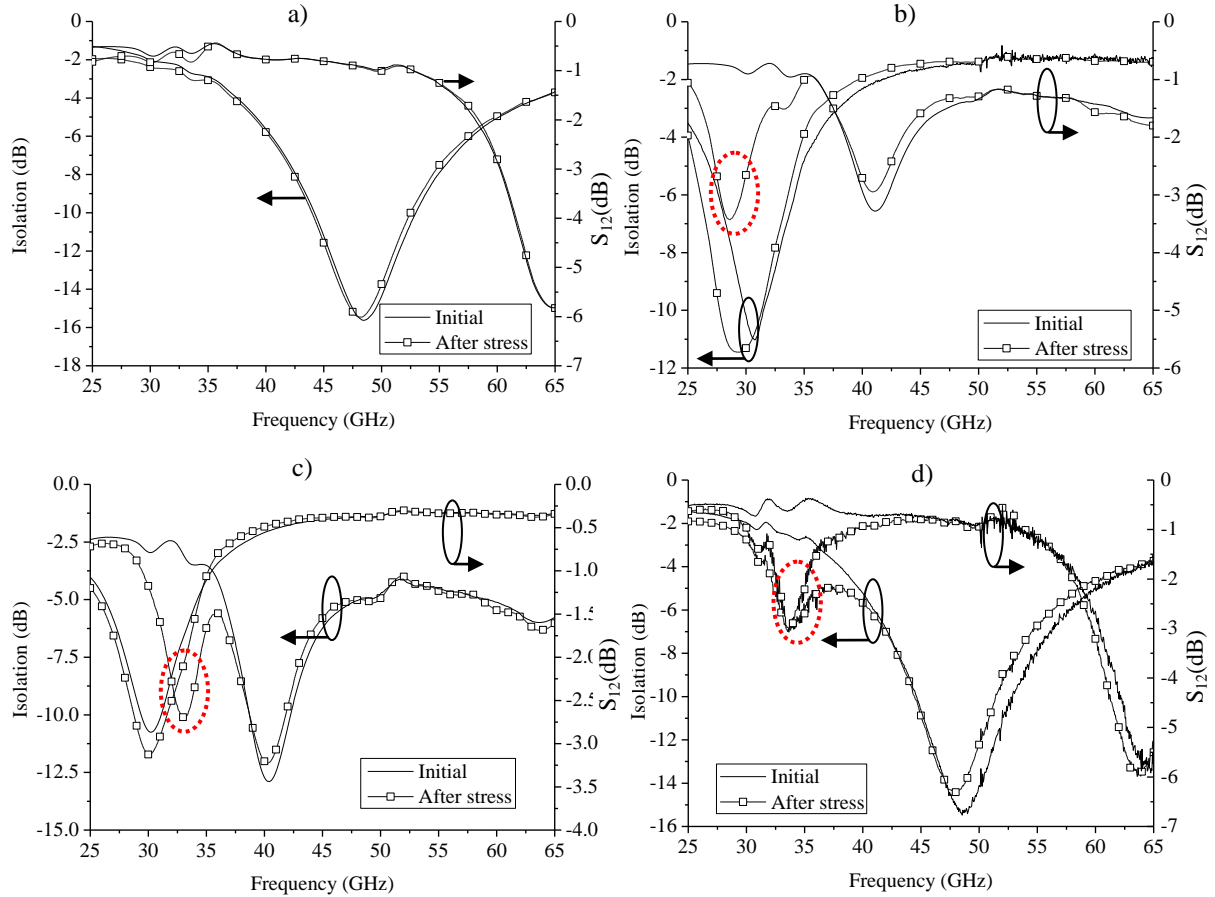


Fig. 4-19: Comparison of S-parameters of the different devices DC stressed: a)X5_Y16_50G b)X5_Y16_30G c)X5_Y14_30G and d)X5_Y14_50G. In red the undesired resonance appeared after stress in some devices

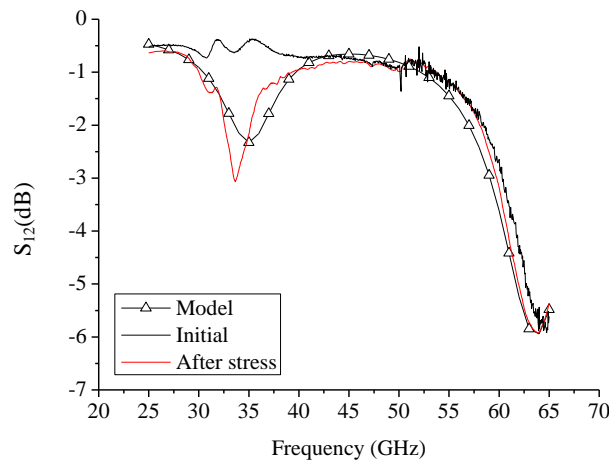


Fig. 4-20: Comparison of IL before (black) and after (red) stress with the model (triangle) of a failed device (X5_Y14_50G) after 1h DC constant stress

The fact of find the same undesired resonance frequency infers that it can come from the rupture of a part of the membrane creating a short circuit with the electrodes not allowing the

a total recovery of the membrane in the initial position. This hypothesis is validated by the equivalent circuit model by means of increasing C_{MEMS}^{UP} to 60fF and C_{M1-M3}^{UP} to 100fF (both values are found by fitting of measurements) as seen in Fig. 4-20. In the case of DOWN state, the model is not able to track the after stress performance because of the difficulty to model the contact between metals and to infer the broken parts.

Finally, comparing the losses versus time (Fig. 4-21) it can be seen that the degradation tendency ($\sim 0.2\text{dB/h}$) is very similar during the first hour in all the devices except for X5_Y14_30G that has presented the undesired resonance. For the 14h test, the losses increase of 0.1dB the first hour and at 0.02dB/h until the end of the test. Both results demonstrate a very good stability and repeatability inside the same cells.

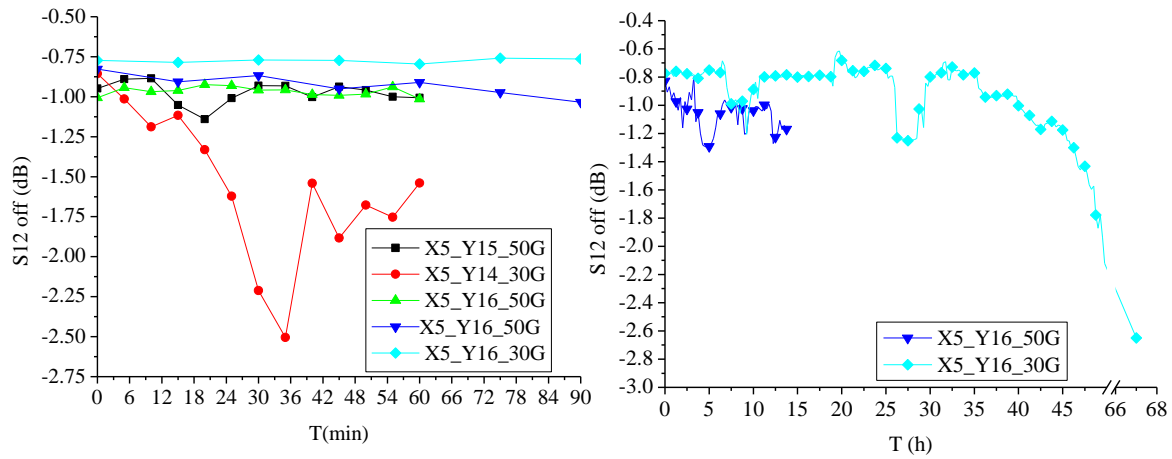


Fig. 4-21: S_{12} in UP state (OFF) versus time for the different DC stressed switches

Cycling test results

Only one of the tested devices at 10^6 cycles have been successful in terms of pull-in and pull-out voltage and insertion losses deviation (Table 4-7). The mean deviation of the tested devices is 13%, 18.3% and 0.28dB respectively. They are comparable to the results obtained in DC stress despite being actuated for less total time (40min). This result infers that the degradation of the TiN-TiN contact between the membrane and the MIM capacitor do not play an important role in the reliability of the device.

Switch	Pull-in (V)			Pull-out (V)			IL (dB)		
	Initial	Final	Dev.	Initial	Final	Dev.	Initial	Final	Dev.
X5_Y13_40G	31	27	14.8%	15	0	100%	2.3	2.4	0.1
X5_Y14_40G	32	29	10%	26	22	18%	0.73	0.95	0.22
X5_Y15_40G	32	29	10%	32	28	12%	0.64	0.97	0.33
X5_Y16_40G	38	36	5%	37	35	5%	0.71	0.99	0.28

Table 4-7: Pull-in, pull-out and IL deviation during the cycling test (10^6 cycles)

In Fig. 4-22 the $|S_{12}(V)|$ characteristic and the RF performance of X5_Y16_40G is plotted showing the evolution of the losses and pull-in/out voltage. In Fig. 4-23 the S-parameters before and after the tests of the failed devices are compared. In X5_Y14_40G and X5_Y15_40G the same undesired resonance than in DC stress is observed. In the low frequency range (between 25 and 30GHz) the degradation of the UP state is higher than in the upper frequencies as was observed in the continuous DC stress tests. This means that the same

failure mechanism (fatigue) is detected and that the contact resistance between the membrane and the MIM capacitor (R_{contact}) do not affect the RF performance.

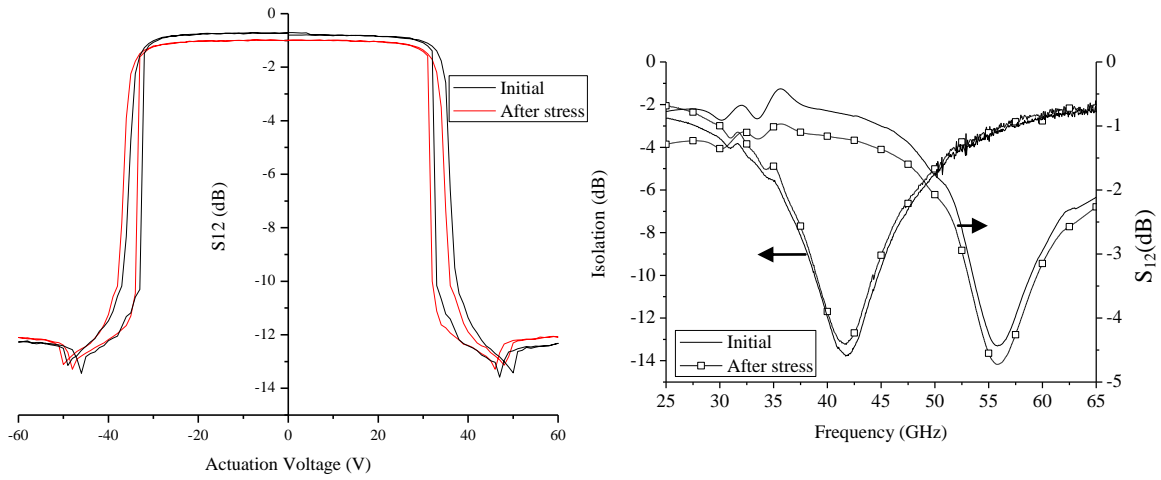


Fig. 4-22: Comparison of $S_{12}(V)$ and RF performance before and after the stress (10^6 cycles) of X5_Y16_40G

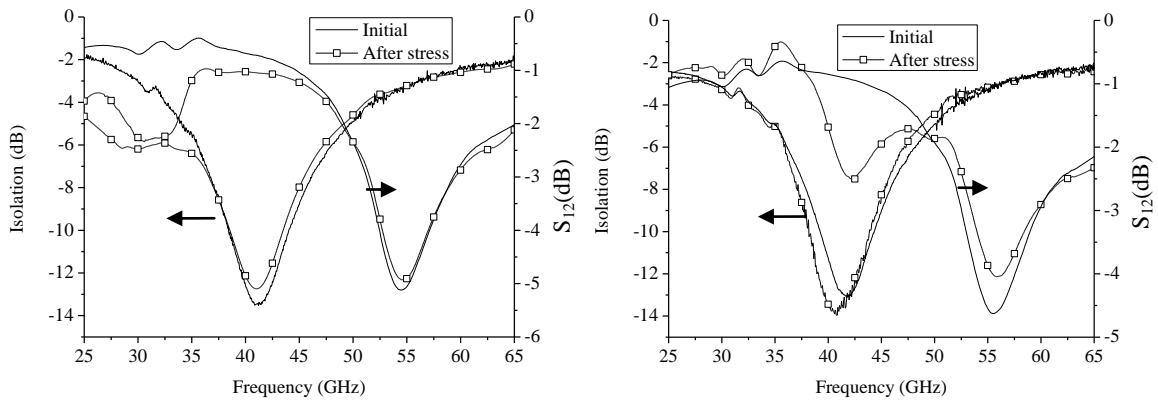


Fig. 4-23: Comparison of RF performance before and after the stress of the tested devices (10^6 cycles): X5_Y15_40G (right) and X5_Y14_40G (left)

The degradation of the S_{12} in UP and DOWN state (OFF and ON) versus time is plotted in Fig. 4-24. While X5_Y15_40G and X5_Y14_40G suffer a constant degradation ($0.4\text{dB}/10^6\text{cycles}$), X5_Y16_40G reaches a constant value at 400.000 cycles (1dB of IL and 12dB of isolation) which indicates the beginning of the normal operation region (burn-in). Noteworthy is that before stabilization, X5_Y16_40G follow the same degradation trend than the failed devices (X5_Y15_40G and X5_Y14_40G).

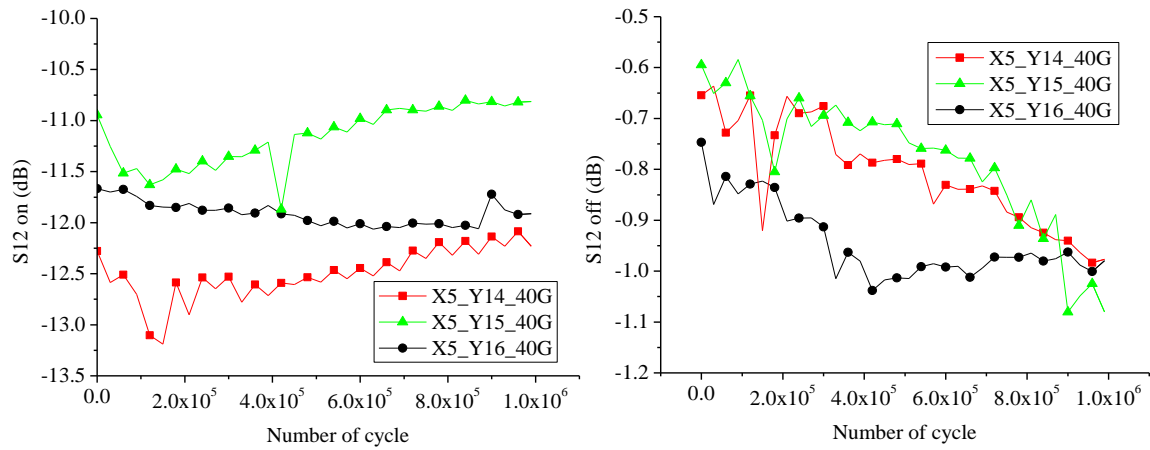


Fig. 4-24: S_{12} in ON (left) and OFF (right) position versus time (10^6 cycles)

Relevant parameters for reliability assessment

Only few switches among those which have been tested and presented above have successfully passed the reliability tests. This does not mean that the switch is not reliable but that a screening of the wafer based on the observed failure signatures should be made so to select the good ones. Some of the tested devices did not present the optimal initial behavior which lately leads to failure (infant mortality). In this part, the selection criteria for optimal mechanical and RF performance are studied in order to guarantee the successful testing.

The two selected parameters are pull-in/out voltage (electro-mechanical) and losses (RF). Doing a screening over a quarter of a wafer the best and worse switches regarding these two parameters are selected for each working frequency (Table 4-8). The chosen switches are DC stressed during 1h.

Family	Worst IL	Best IL
Xm_Yn_50G	X6_Y13 (1dB)	X6_Y15 (0.8dB)
Xm_Yn_40G	X7_Y15 (1.1dB)	X7_Y14 (0.75dB)
Xm_Yn_30G	X6_Y13 (0.78dB)	X7_Y15 (0.6dB)
Family	Lowest pull-out	Ideal
Xm_Yn_40G	X7_Y13 (21V)	X6_Y16 (38V)
Xm_Yn_50G	X7_Y13 (28V)	X6_Y16 (37V)
Xm_Yn_30G	X6_Y14 (31V)	X6_Y15 (36V)

Table 4-8: Selected devices for optimal mechanical and RF performance

The results regarding the loss criteria are shown in Table 4-9. Only the switches with best losses (X7_Y15_30G and X7_Y15_40G) succeeded the test except of X6_Y15_50G. This exception indicates that also other parameters should be checked since the level of losses is not enough to determine the reliability of the switch. Moreover, for a mass-production manufacturing, the measurement of S-parameters is very slow and difficult. Therefore finding

other parameter easy to be measured (time and equipment) is paramount in MEMS device production (it enables in-line test and/or test in very harsh environment).

Switch	T(h)	Pull-in (V)			Pull-out (V)			IL (dB)		
		Initial	Final	Dev.	Initial	Final	Dev.	Initial	Final	Dev.
X6_Y13_30G	1	35	27	30%	29	15	93%	0.78	0.78	0
X7_Y15_30G	1	39	37	5%	38	35	8.5%	0.6	0.6	0
	16	39	33	18%	38	32	18%	0.6	0.8	0.2
X7_Y14_40G	1	38	37	3%	37	35	6%	0.75	0.75	0
X7_Y15_40G	1	38	37	3%	37	35	6%	1.1	1.2	0.1
X6_Y13_50G	0.3	28	22	27%	22	16	37%	1	1	0
X6_Y15_50G	1	37	35	6%	36	32	12%	0.85	0.78	0.07
	16	37	32	15%	36	26	38%	0.85	0.93	0.1

Table 4-9: Results of the tests done to the selected devices under the losses criteria

Using the pull-out criteria, the results (Table 4-10) show that when selecting the highest pull-out voltage the switches succeed the tests (X6_Y16_40G). All the switches with pull-out voltages lower than 37V have not passed the tests. The same relationship is seen with the devices studied in Table 4-9. Regarding also the pull-in voltage, it is seen that, in addition, the difference between the pull-in and pull-out voltage should be very low (maximum 1V).

Switch	T(h)	Pull-in (V)			Pull-out (V)			IL (dB)		
		Initial	Final	Dev.	Initial	Final	Dev.	Initial	Final	Dev.
X7_Y13_40G	1	33	24	37%	21	18	16%	0.8	5.7	4.9
X6_Y16_40G	1	38	37	3%	37	36	3%	0.62	0.93	0.31
X7_Y13_50G	1	32	25	28%	28	15	86%	1.1	1.1	0
X6_Y16_50G	1	36	34	5%	34	29	15%	0.98	1.02	0.04
X6_Y14_30G	1	35	28	25%	31	25	24%	0.97	1.16	0.19
	16	35	30	16%	31	24	30%	0.97	1.5	0.53
X6_Y15_30G	1	35	33	6%	36	30	17%	0.83	0.87	0.04

Table 4-10: Results of the tests done to the selected devices under the pull-in/out criteria

Regarding the RF performance only a slight variation was detected (Fig. 4-25). The observed increase of the losses is due to fatigue in the membrane which yields a decreasing of the distance between the RF line and the membrane changes and hence an increase of the UP state capacitance (8% as seen before). This will be proved by means of the profilometer measurements later on this chapter.

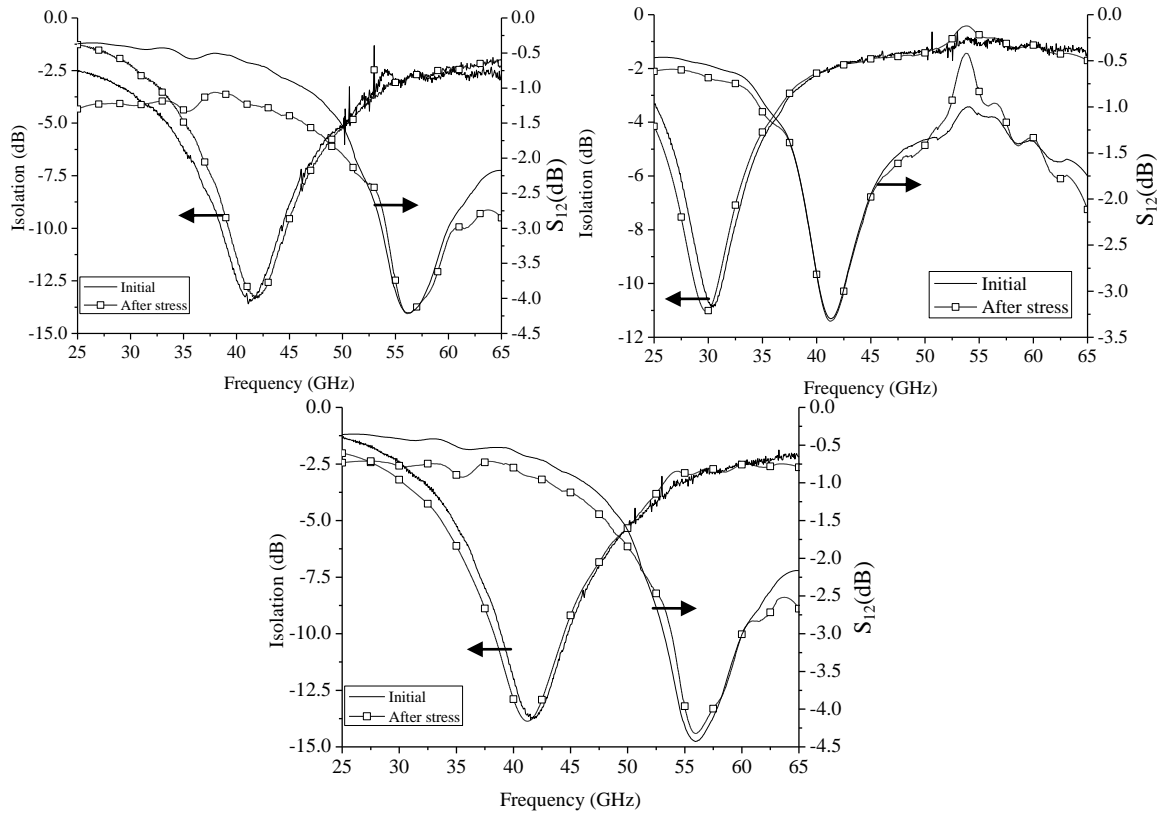


Fig. 4-25: Isolation and insertion losses before and after the test: X7_Y15_40G (top left) X7_Y15_30G (top right) and X6_Y16_40G (bottom).

In Fig. 4-26 the losses and versus time of the same switches are plotted. This plot demonstrates that after 5 minutes of constant actuation the RF performance is stabilized.

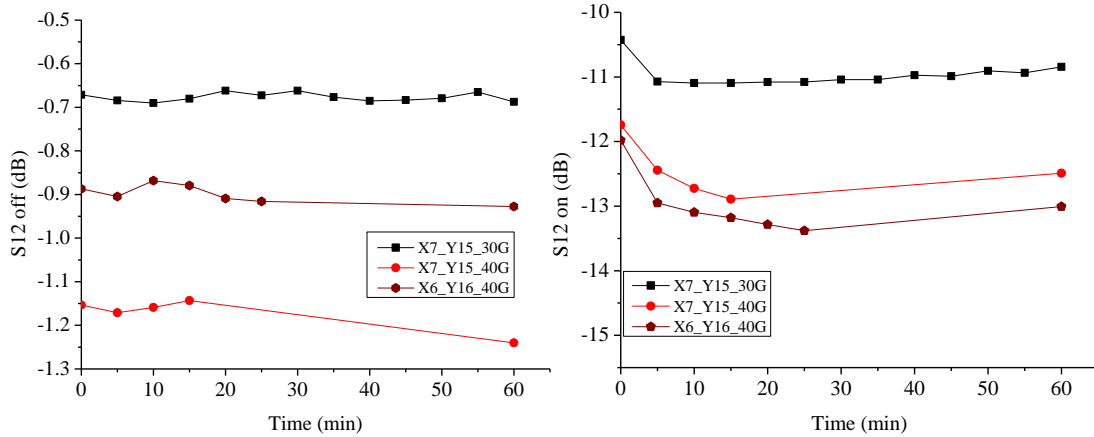


Fig. 4-26: S_{12} in off state (left) and S_{12} in on state (right) versus time for the switches that succeeded the tests

Grouping the results of Table 4-9 and Table 4-10, the plot in Fig. 4-27 resumes the results. This plot shows the deviation of the V_{POUT} voltage after 1h of stress for several identical switches with different initial V_{POUT} . The size of the disk shows the difference between pull-in and pull-out voltage. Applying the industrial requirements (10% of deviation in V_{POUT}) it is concluded that the criteria to be used to identify the reliable switches is: $V_{POUT} > 36$ and $V_{PIN} - V_{POUT} \leq 1$.

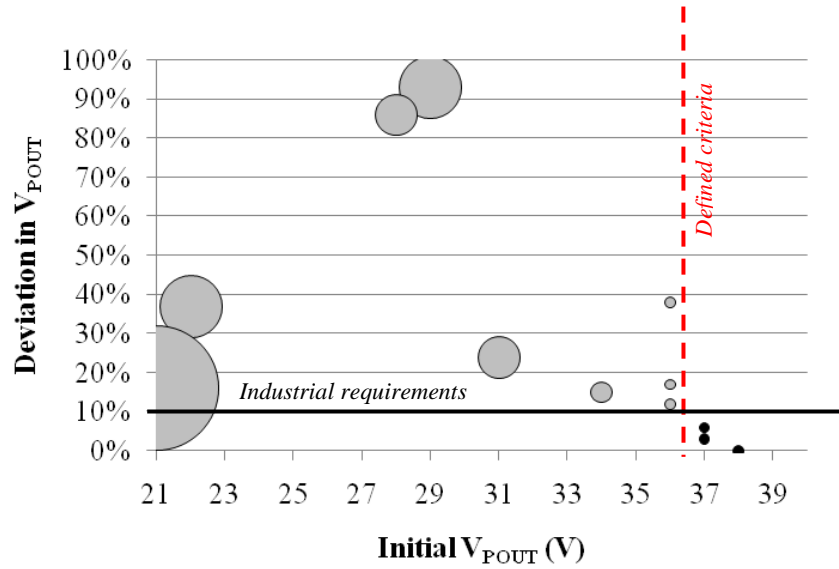


Fig. 4-27: Deviation of V_{POUT} after stress of the tested devices with different V_{POUT} . The size of the disks represents the difference between V_{PIN} and V_{POUT} . In black the devices that accomplish the industrial requirements for 1h of continuous DC stress

The displacement of the membrane (g) is related with the applied tension (V) as it is shown in Eq. 4-4 where k is the stiffness, the gap without actuation between actuator and membrane is g_0 and S is the size of the actuator. Plotting the $g(V)$ curve of the succeeded devices (Fig. 4-28) using (Eq. 4-6), it is proved that they are placed in the linear region (below mechanical pull-in) so the V_{PIN} and V_{POUT} are very similar. The distance between membrane and line is smaller than $2/3$ times the distance between the membrane and the electrode (g_0) which is considered the mechanical pull-in.

$$V = \sqrt{\frac{2k}{\epsilon_0 S} g^2 (g_0 - g)} \quad \text{Eq. 4-6}$$

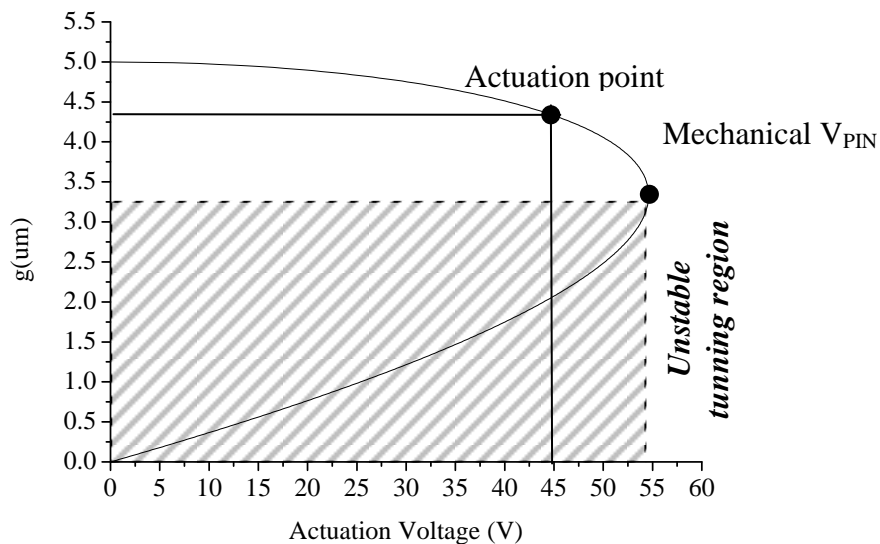


Fig. 4-28: $g(V)$ of a succeeded device with the actuation point when applying 45V and the mechanical pull-in

For this reason profilometer (FOGALE Nanotech) measurements have been done after stress measuring the distance between line and membrane (M2-M3) and between electrode and membrane (M1-M3) without any actuation voltage. In Table 4-11 the results show that the distance between M1 and M3 trends to decrease making the distance between line and

membrane (M2-M3) bigger after stress. This is due to the force applied mainly on the lateral parts of the membrane (electrodes) where more stress is accumulated (Fig. 4-29).

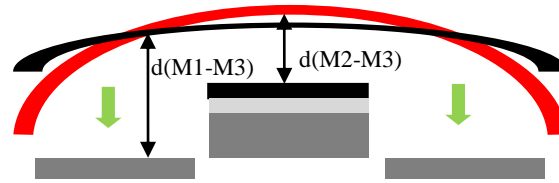


Fig. 4-29: Schema (magnified) of the shape bending: cross section of the membrane before (black) and after (red) stress. The green arrows show where the electrostatic forces are applied

These measurements provide a tool for the manufacturer in order to select the optimal switches over the wafer (Fig. 4-30). If the distance M2-M3 is around $2.8\mu\text{m}$ and the distance between M1-M3 is approximately $4.7\mu\text{m}$, the device is stiff enough to succeed the tests. These distances correspond to the pull-in/out voltages computed above (37V). This can be implemented by a Technology Characterization Vehicle (TCV) inserted in each cell with a single MEMS device in order to check if the optimal distances between metals in the movable part are respected. It can also be implemented in the final device before packaging.

Switch	M2-M3		M1-M3	
	Reference	After stress	Reference	After stress
X6_Y13_30G	2.26 ± 0.06	2.3	5.18 ± 0.09	4.9
X6_Y13_50G		1.5		5
X6_Y14_30G	2.3 ± 0.35	2.5	5.26 ± 0.13	5.1
X6_Y15_30G	2.66 ± 0.12	2.8	5.03 ± 0.14	4.8
X6_Y15_50G		2.6		5
X6_Y16_40G	2.57 ± 0.04	2.7	5.07 ± 0.09	4.9
X6_Y16_50G		2.6		4.9
X7_Y13_40G	2.33 ± 0.05	2.36	5.5 ± 0.7	5
X7_Y13_50G		2.4		4.9
X7_Y14_40G	2.56 ± 0.05	2.7	4.8 ± 0.01	4.8
X7_Y15_30G	2.58 ± 0.06	2.87	4.75 ± 0.2	4.47
X7_Y15_40G		2.8		4.5

Table 4-11: Distance (μm) between M2 and M3 and between M1 and M3 after the tests for the selected devices. In bold the devices that succeeded the reliability tests. The reference is the mean value and standard deviation of the distances for each cell

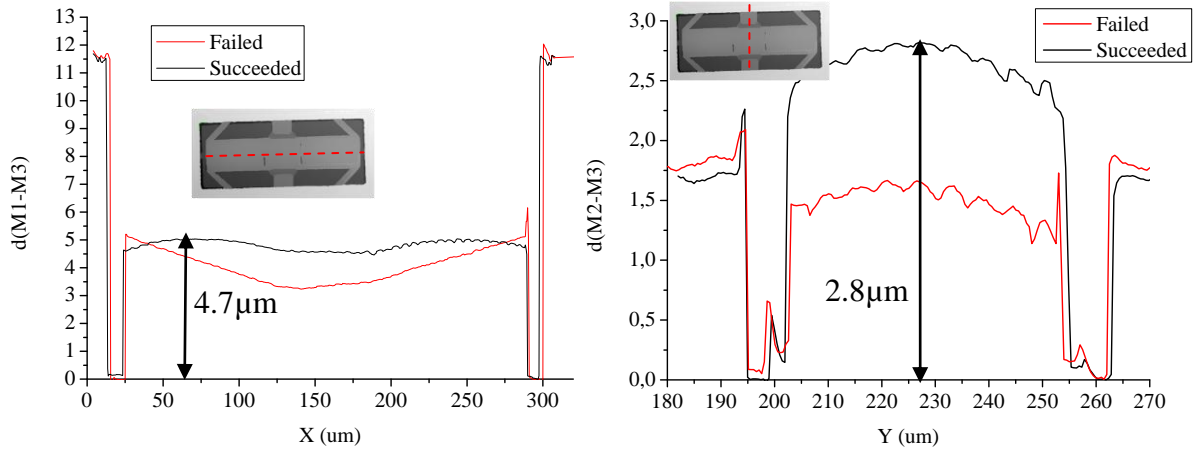


Fig. 4-30: Example of cross section of a membrane for the switches that succeeded (black) and failed (red) regarding $d(M1-M3)$ (top) and $d(M1-M3)$ (bottom)

Noteworthy is that the devices that succeeded the tests are located in the same region of the wafer. The area highlighted in Fig. 4-31 shows the region where the devices with optimal performances are located. If the reliability tests are done in this region, more success is expected (planned to be done in future).

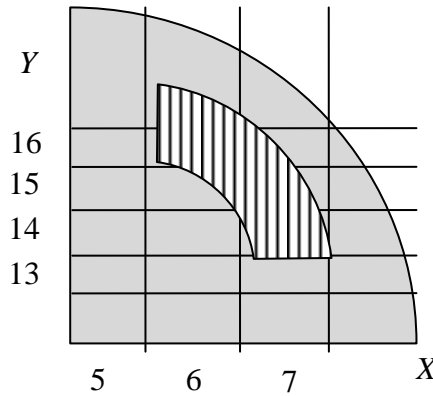


Fig. 4-31: Distribution of the devices that succeeded the tested over the quarter wafer.

With the results of this section, the Weibull curve (introduced in page 8) is shown in Fig. 4-32 for the devices selected randomly (called random) and under specified criteria (called selected). There are 2 considerations to take into account:

- The number of tested devices: 8 devices (random) and 12 (selected). This low number of devices makes the conclusions preliminary and needed to be confirmed in future work.
- The measurement protocol was stopped after the desired time (1h): the devices that passed this period have never been stressed to their end-of-life.

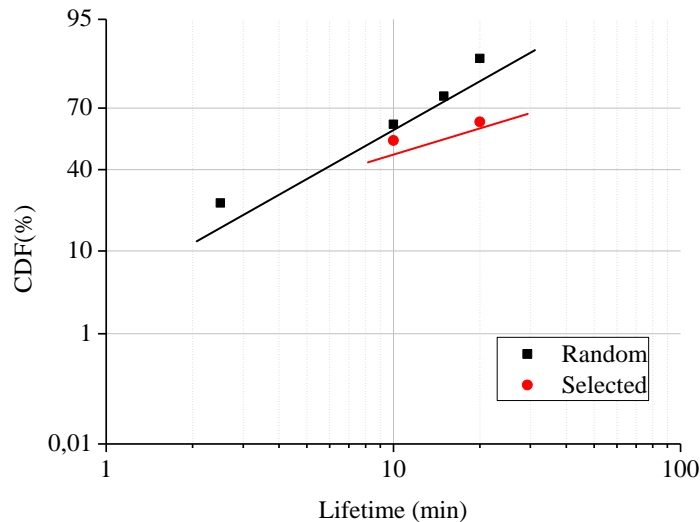


Fig. 4-32: Weibull plot of the tested devices with the regression curve.

The results presented in Fig. 4-32 indicate infant mortality despite selecting or not the devices ($\beta < 1$). The dispersion of lifetime from switch to switch is very high. However, it has been seen that when the devices are selected properly ($V_{\text{POUT}} > 36$ and $V_{\text{PIN}} - V_{\text{POUT}} \leq 1$) all the devices succeed the tests and this infant mortality can be eliminated. In future work, the devices under the specified selection criteria should be stressed until the end-of-life to proof the preliminary result shown in this thesis.

Conclusions of reliability tests

The failure mechanism detected is fatigue observed by stiction of the membrane and/or decrease of the distance between the membrane and the RF line (also seen between electrodes and membrane). The dielectric charging in the contact zone is avoided because the line and the membrane are at the same potential (0V).

It has been seen that the most relevant degradation occurs during the first hour of tests. One device has been tested during 67h in continuous DC stress showing the same deviation in pull-in voltage than for the 1h tests. However, the losses have increased 1.8dB (though still in the specifications!) during the last 20h of test. Another switch has been tested during 14h achieving similar deviations of V_{PIN} and V_{POUT} without reaching the limit difference of 2dB of losses. From a RF designer point of view, it is translated to a deviation of circa 9% in the UP/DOWN capacitance that should be added to the fabrication process deviation extracted from the RLC model.

Another important result that has been shown is the possibility to predict which devices are reliable over the entire wafer, by means of a profilometer measurement. This is possible because pull-in/out voltage has been identified as an indicator of failure and it is related to the distance between membrane and line and electrodes. Keeping these distances in known acceptance value range ($2.6\mu\text{m}$ and $4.7\mu\text{m}$ respectively for a pull-in/out voltage of circa 37V) guarantees the reliability of the switch. Worth of note is that tests have been performed in controlled room conditions (22°C 45%RH) which are far from typical working conditions of packaged device, but are close to fabrication environment conditions where these preliminary test should be carried out (before packaging device screening).

The low deviation of the profilometer measurements inside the same cell implies that the screening of the devices affected by infant mortality can be performed over the wafer. The use of replicas of the same cell, whose size and position was optimized beforehand in IHP; over

the wafer allow the introduction of Technology Characterization Vehicle (TCV) where a single MEMS device can be added to check if the optimal distances between metals in the movable part are respected or directly checked in final devices before packaging.

A preliminary Weibull curve has been presented computed with a small number of switches. The dispersion of lifetime from switch to switch is very high. However, it has been seen that when the devices are selected properly ($V_{\text{POUT}} > 36$ and $V_{\text{PIN}} - V_{\text{POUT}} \leq 1$) all the devices succeed the tests and this infant mortality can be eliminated. In future work, the devices under the specified selection criteria should be stressed until the end-of-life to proof the preliminary result shown in this thesis.

4.3 Applications of co-integrated CMOS-MEMS devices

4.3.1 Synthesis of a new series switch for routing applications

It has already been seen in the previous section that when the designer changes the working frequency (increasing or decreasing the inductance of the anchors), the proposed model can easily describe it. This section demonstrates that the model can be used to carry out the design of a new component based on the same technology and MEMS constitutive part. The equivalent circuit tool is useful not only for RF characterization (failure analysis and fabrication process tolerances) but also to synthesize new layout components (FIG)

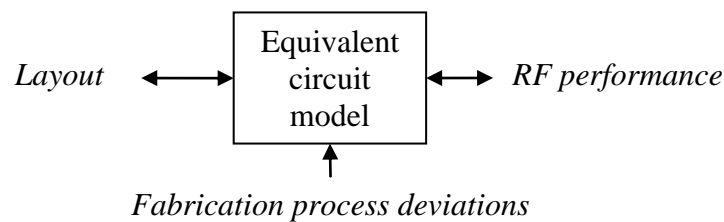


Fig. 4-33: Equivalent circuit role in high TRL environment fabrication process

The series switch is conceived by modifying the metal layer interconnection layout of the V4 switch (48GHz). The membrane is disconnected from the ground in order to connect it to the output Fig. 4-34.

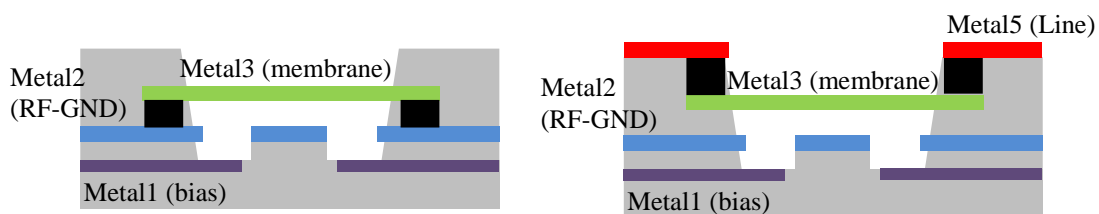


Fig. 4-34: Cross section of the shunt (left) and series (right) switch used for the experiment.

The main advantage of this new design is that the movable part is not modified from the one studied in section 4.2.2. This means that not only the reliability tests done are also valid in this switch, but also that the fabrication dispersion can be taken into account using the same model.

The model of the series switch is presented in Fig. 4-35. In comparison with the shunt model, only a new transmission line is added in order to model the connection of the inductances to the anchors. In order to alleviate this effect and improve the isolation, a shunt inductor is added. Keeping the parameters of the model with the same value as the shunt RF-MEMS switch in previous section only 2 elements are included according to the layout: 1) The

transmission line that connects the membrane with the output (TL1), 2) The inductor (L_{shunt}) that resonates with C_{UP} and yields better isolation at the desired frequency (40GHz).

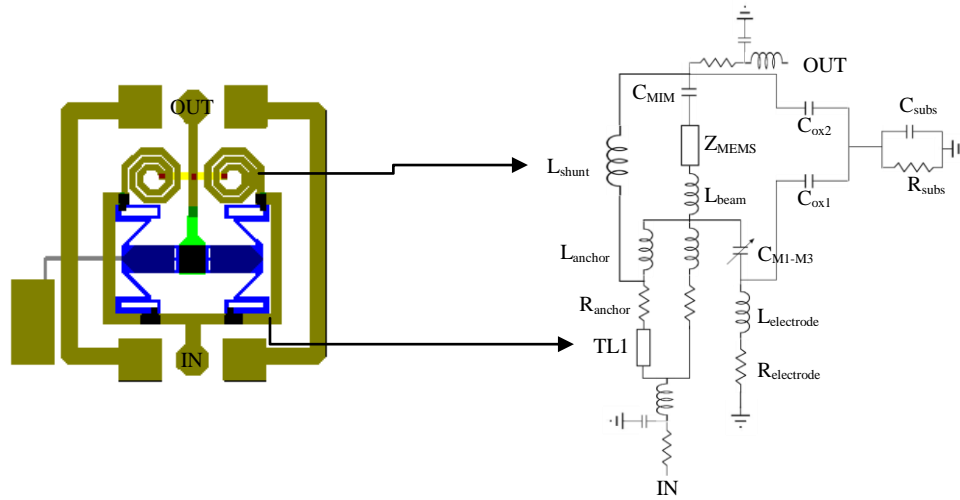


Fig. 4-35: Layout (left) and adapted model (right) of the series switch

The RF performance of the first trial of series switch is shown in Fig. 4-36. Comparing the model with the fabrication process dispersion and the RF measurement of the series switch very good agreement is found. Although the RF performance is not optimized yet, ($RL < 15\text{dB}$, $IL < 2.5\text{dB}$ and $\text{isolation} > 15\text{dB}$), the model fits very well the measurements and demonstrates excellent accuracy and versatility. The high losses ($\sim 2.5\text{dB}$ at 40GHz) observed in the measurements are due to the resonant circuit composed by $C_{\text{M1-M3}}$ and $L_{\text{electrode}}$. This resonance can be easily controlled by increasing the length of the bias line or by adding a resistor to the bias line. The expected performance of both options is plotted in Fig. 4-36.

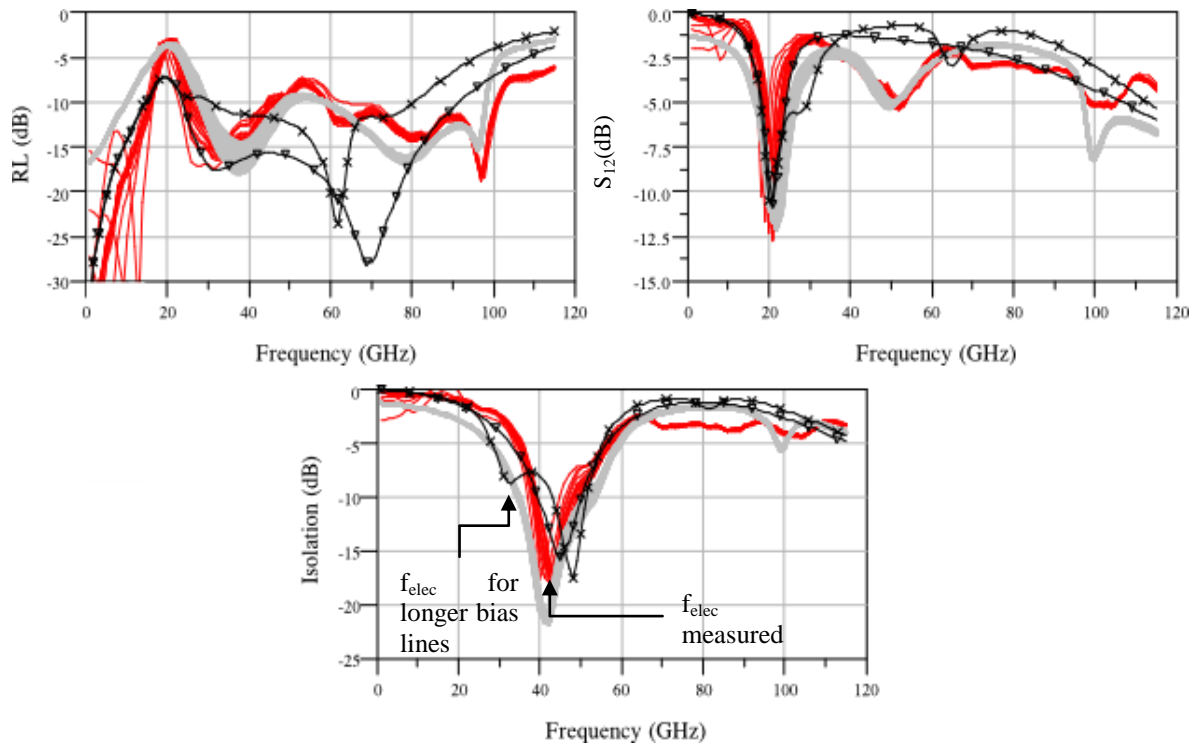


Fig. 4-36: Comparison of RF performance between measurements of 50 devices (red) and model (grey) and expected RF performance of the optimized series switch using the proposed methods: high resistance bias line (triangle) and higher inductance bias lines (cross)

The optimization of the series switch is presented in Fig. 4-37. The option that has been chosen is the increase of the length of the bias lines since it only requires a BEOL run. In contrast, in order to add the resistors on the bias line, a FULL run (including the active part of the BiCMOS process) are needed which means higher manufacturing time and cost. The series switch present 1.7dB of IL and 13dB of isolation at the working frequency (45GHz) and the model fits very well with the measurements in the whole band. Again, this agreement proofs the versatility of the model allowing the design of new components just modifying the equivalent circuit and translating the changes in the layout. This is possible because each constitutive part is based on the physical dimensions of the membrane.

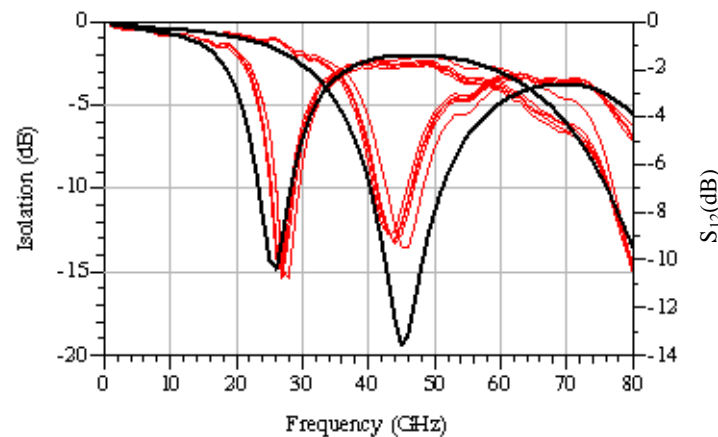


Fig. 4-37: Comparison of RF performance between measurements (red) and model (black)

The development of this new component in IHP library allows the design of SPDT based phase shifters (Fig. 4-38).

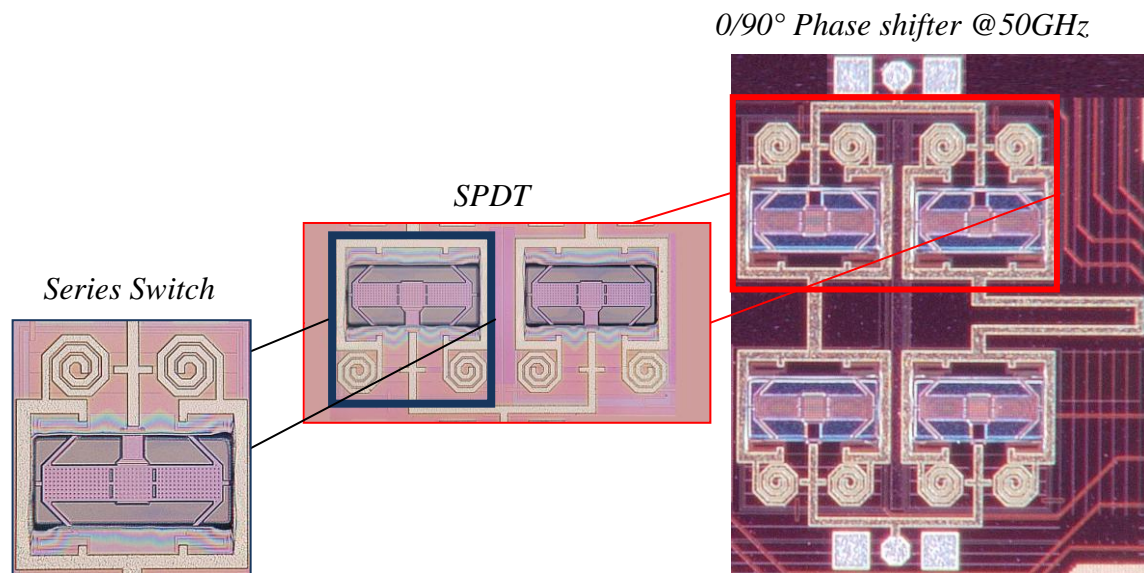


Fig. 4-38: Microscope image of the designed circuits based on the series switch

4.3.2 Absorptive switches

An absorptive switch is a switch that whatever his state is, it is always matched. This means that there is no reflection of the signal when it is in isolation state so, the VSWR is 1 in all states. This matching can be done by using resistive components, by using passive circuits (couplers) or by using micro fluidics. As the standard 0.25 μ m BiCMOS process of IHP includes resistors and the line losses for microstrip lines are 6dB/cm at 60GHz (high losses if

long transmission lines are needed), in this section an absorptive switch using resistors is designed for optimal RF performance.

The potential applications of these switches are in switching matrix telecommunication. One example is shown in [86] where a Butler matrix is used after an absorptive SP4T for beam-forming applications. The aim of having an absorptive SP4T is that the Butler matrix needs to have all the ports matched in order to achieve the phase shift that will change the direction of the beam in the antenna.

Literature shows very few examples of absorptive switch using RF-MEMS [88]-[90]. The main reasons of these few publications are the complexity on the fabrication process (sometimes resistors are required in the design and its integration in the MEMS fabrication process is not easy) and the repeatability of the switches is not assured.

Comparing with other technologies (CMOS, PIN, ...) where some commercial solutions exists, it is seen that the problem is solved by switching between a resistor and a line as it was proposed in [92]. The advantage of using RF-MEMS arises from lower losses and higher frequency range.

Three main different topologies are possible for designing absorptive switches (Fig. 4-39) using resistors. After doing a sensitivity study, the most critical parameter of all the designs is R_o while the switch parameter (C_{MEMS}) remains at the second place. In terms of losses, the pi-network and the SPDT based absorptive switch achieve higher insertion losses due to the long lines used ($\lambda/4$ at 50GHz $\sim 740\mu m$). This was confirmed for the Pi-network in [92] where losses are approximately 3dB at 50GHz. For this reason, the T-network is optimized using the developed series switch.

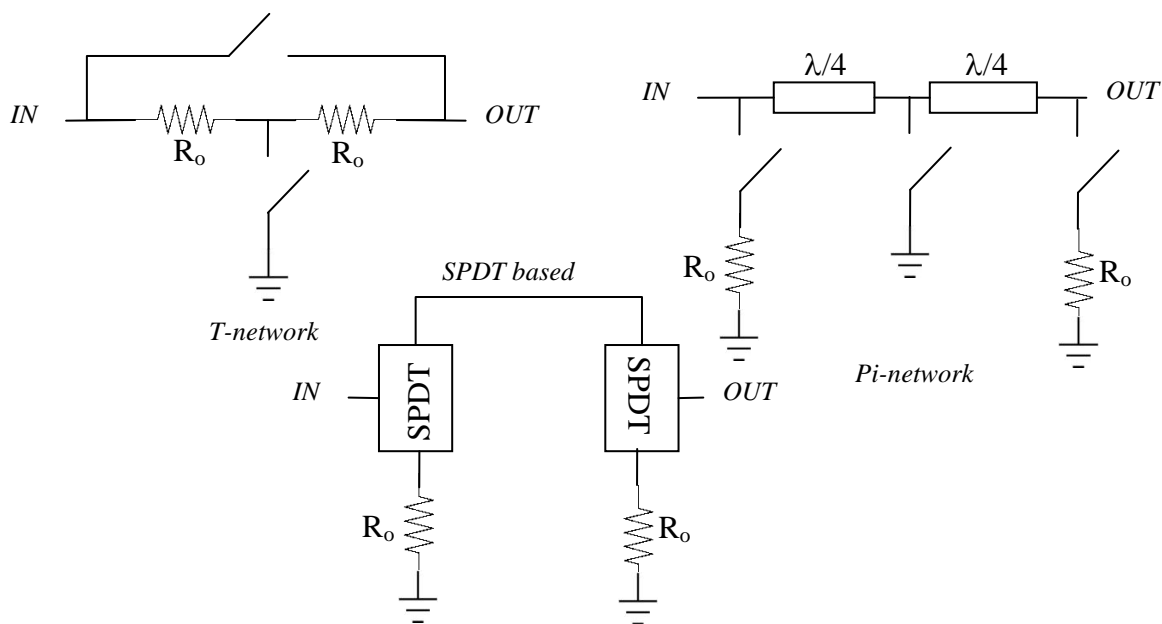


Fig. 4-39: Different topologies using resistors for absorptive switches

The optimization of the T-network is based on the minimum number of switches, the minimum power consumption and the insensitivity to resistor tolerances. The result is a combination of a T-network (with resistors R_o) with $\lambda/4$ lines whose characteristic impedance is Z_L (Fig. 4-40)

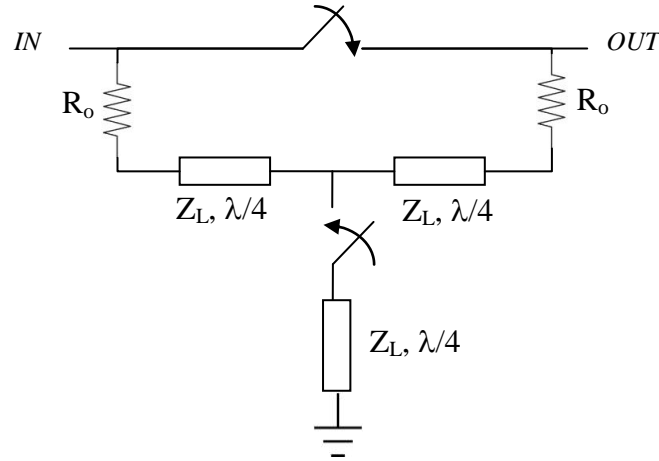


Fig. 4-40: Schema of the designed absorptive switch

In both states input matching is required. Noteworthy is that in isolation state no switch is actuated which implies no power consumption while the circuit is perfectly matched. The two states are defined as:

- 1) Isolation state: all switches are in UP state (OFF)
- 2) Transmission state: all switches are DOWN state (ON).

In Fig. 4-41 the simulated RF performance of the novel absorptive switch is plotted. The simulation has considered the studied fabrication process dispersion of RF-MEMS devices (section 4.2.2), the line losses and also the tolerances of the resistors defined by the standard CMOS process (10%). Input matching better than 10dB and isolation better than 25dB is achieved while losses are above 2dB. Comparing with the Pi-network developed in [92], the whole RF performance is improved.

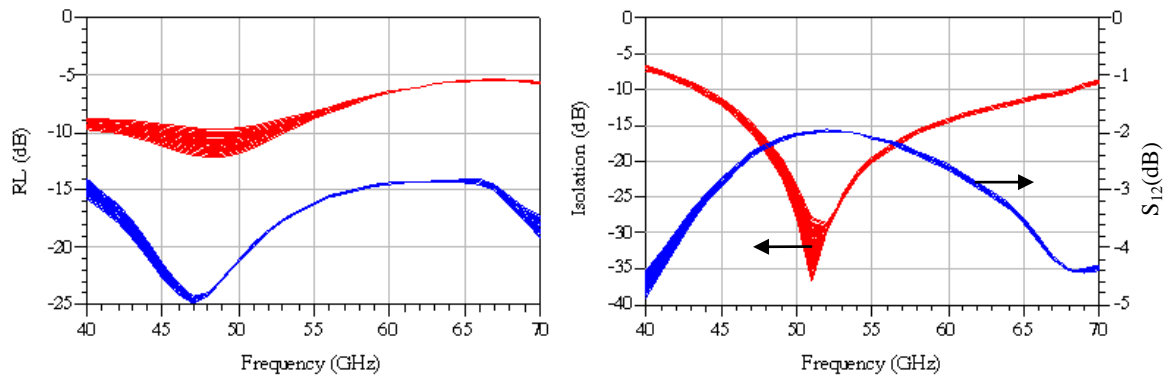


Fig. 4-41: Simulated RF performance in isolation state (red) and transmission state (blue)

4.4 Conclusions

The co-integration of RF-MEMS devices in commercial CMOS process improves the stabilization and controls the fabrication process dispersion. The presented lumped-elements based equivalent circuit is an excellent tool for tracking process deviations and quantification of the yield quality on and between wafers. It is able to identify if the capacitance are acceptable values for a given RF performance. Moreover, for the development of new structures (synthesis), such as series switch, the equivalent circuit has demonstrated also its efficiency showing very good agreement between measurements and model.

The IHP fabrication process uses the component approach to develop reliable RF-MEMS switches. This approach does not allow any change in the membrane design since every process step was previously optimized. By monitoring few specific parameters, it is possible to track reliability shortcoming ahead of final device preparation (e.g. packaging) hence meeting industrial production requirements. The selection criterion is the pull-in/out voltage which should be higher than 37V and the difference between pull-in and pull-out voltage lower than 1V.

This thesis has proposed the method (profilometer measurements) to identify the stiffer (higher pull-in/out voltage) switches over the wafer. The low deviation of the profilometer measurements inside the same cell implies that the screening of the devices affected by infant mortality can be performed over the wafer. The use of replicas of the same cell, whose size and position was optimized beforehand in IHP over the wafer; allow the introduction of Technology Characterization Vehicle (TCV) where a single MEMS device can be added to check if the optimal distances between metals in the movable part are respected.

A preliminary Weibull curve has been presented computed with a small number of switches. The dispersion of lifetime from switch to switch is very high. However, it has been seen that when the devices are selected properly ($V_{\text{POUT}} > 36$ and $V_{\text{PIN}} - V_{\text{POUT}} \leq 1$) all the devices succeed the tests and this infant mortality can be eliminated. In future work, the devices under the specified selection criteria should be stressed until the end-of-life to proof the preliminary result shown in this thesis.

The deep study done in this thesis about this switch has allowed the development of routing circuits (SPDT) and phase shifters. Moreover, the possibility of co-integration with CMOS technology opens other applications such as absorptive switches. Since the process deviations are well known and characterized, the design of a BIST (Built In Self Test) circuit should be the next step.

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Chapter 5

Conclusions and perspectives

5.1 Introduction

The motivation of this thesis is the investigation of possible solutions for reliability improvement by means of the design (Design for Reliability). In previous chapters different RF-MEMS devices and circuits have been implemented and characterized. This has allowed me to identify the advantages and disadvantages of each approach and how the reliability challenges can be solved through the design and process steps. The conclusion is that the most suitable method depends on the TRL of the process.

This concluding chapter has two distinguished parts: a first part where a comparison between the studied processes is done and a second part where an extension to other available RF-MEMS fabrication process is demonstrated. The comparison done in the first part aims to justify the relationship between the degrees of freedom offered by the process with the reliability problems of the device. With this purpose five different indicators are chosen (adaptability, process flexibility, process simplicity, repeatability of the process and device robustness). The connection between them will determine the design flow to be adopted for the development of reliable switch. Using the same indicators (except for repeatability of the process), the studied processes are compared with other existing fabrication process of the same TRL level. Finally, the main achievements of this thesis are reported along with perspectives and personal considerations.

5.2 Comparison between studied processes

In Table 5-1 a qualitative comparison between the studied processes is presented. The aspects compared are:

- Adaptability: this concerns the possibility of integrating different configurations (series/shunt) and topology (resistive/capacitive) in the same run,
- Process flexibility: the possibility to introduce new materials in the original process and/or modifying the process steps.
- Process simplicity: measured by the number of masks used for the fabrication (packaging not included)
- Process repeatability: this defines the variation of the RF and mechanical performance of the devices over the entire wafer and from wafer to wafer. The tolerances refer to the variation on the physical dimensions (size and roughness of materials) of the structures.

- Device robustness: failure mechanisms with their associated RPN (see Chapter 1)
 - o LAAS-CNRS (Chapter 2): temperature induced elastic deformation, equivalent DC voltage, dielectric charging, micro welding, capillary forces, creep, fracture
 - o CEA-Leti (Chapter 3): structural short, capillary forces, electromigration
 - o IHP (Chapter 4): fatigue and creep
- Co-integration: the possibility to integrate or assemble the MEMS part along with other circuit components.

		LAAS-CNRS (low TRL)	CEA-Leti (medium TRL)	IHP (high TRL)
Adaptability	Configuration	Series and Shunt	Series ²⁰	Series and Shunt
	Topology	Resistive and capacitive	Resistive	Capacitive
Process Flexibility	Material level	High	Low/medium	None
	Process level	High	Medium	Low
Process Simplicity ²¹		Simple (7)	Medium (11)	High (21)
Process repeatability	Wafer to wafer	Very low	High	Very high
	On wafer	Medium	Very low	Very low
	Tolerances	High	Very low	Very low
Device robustness	Failure mechanisms	6	3	2
	Maximum RPN	252	180	120
Co-integration		MMIC	Pick and place ²²	BiCMOS

Table 5-1: Comparison between the studied fabrication process

Table 5-1 shows that low TRL processes enable high degree of freedom in terms of adaptability at the price of a high dispersion. The contrary happens for low and medium TRL environments where the restrictions in adaptability improve the fabrication process dispersion. The advantage in terms of adaptability of BiCMOS-MEMS process resides in the interconnection possibilities offered by the availability of different metal layers (five).

In Fig. 5-1 the different aspects compared above in Table 5-1 have been quantified and normalized by using a radar chart. The scales used in each case are:

- Adaptability (a_i): from 0 to 2. 0: one topology one configuration, 1: one topology two configurations or vice versa and 2: two topologies and two configurations. It is normalized as Eq. 5-1

²⁰ Previous developments in CEA-Leti demonstrate the possibility of shunt resistive switches [67]. However it was abandoned due to contact instability of the three dimples

²¹ In brackets the number of masks used

²² The switch can be wire-bonded to other devices fabricated with other technologies

$$\bar{A}_i = \frac{a_i}{2} \quad \text{Eq. 5-1}$$

- Process flexibility (f_i): from 0 to 10. 10 means very flexible fabrication process and 0 means no change is allowed. It is normalized as Eq. 5-2

$$\bar{F}_i = \frac{f_i}{10} \quad \text{Eq. 5-2}$$

- Process simplicity (s_i): using the number of masks²³. It is normalized with respect to the maximum number of masks of the studied processes ($s_1 \dots s_n$) as shown in Eq. 5-3

$$\bar{S}_i = 1 - \frac{s_i}{\max(s_1 \dots s_n)} \quad \text{Eq. 5-3}$$

- Device robustness (d_i): using the highest RPN (RPN_i) of the detected failure mechanisms and normalized as indicated in Eq. 5-4. 40 is the minimum RPN that can be achieved in RF-MEMS FMEA analysis (see Chapter 1) and 212 is the dynamic range of failure mechanisms (from 252 to 40)

$$\bar{D}_i = 1 - \frac{RPN_i - 40}{212} \quad \text{Eq. 5-4}$$

- Process repeatability (r_i): dispersion in RF measurements over the wafer in percentage as indicated in Eq. 5-5

$$\bar{R}_i = 100 - r_i(\%) \quad \text{Eq. 5-5}$$

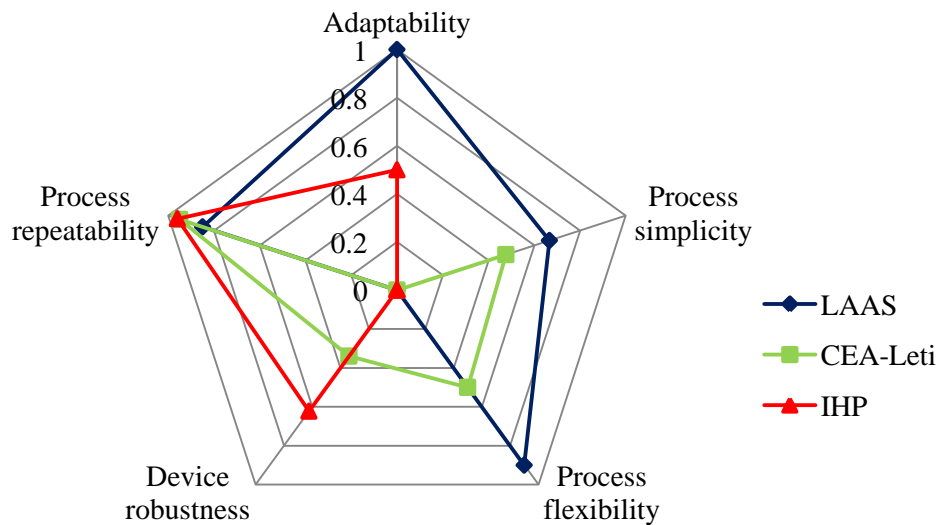


Fig. 5-1: Comparison between the three studied fabrication process in terms of adaptability, process variation, complexity, failure mechanisms and on-wafer dispersion

Fig. 5-1 show that the device robustness and the process repeatability increase when increasing the TRL environment. On the contrary, the fabrication processes are more complex (decrease of simplicity). The price to pay is the adaptability and the process flexibility which

²³ The most suitable parameter to describe the process complexity is the number of steps, but it is not always known. The number of steps is proportional to the number of masks.

are both drastically reduced comparing with low TRL environments. Fig. 5-1 shows also that the increase of complexity is not related with the dispersion. This is due to the use of standard process (BiCMOS) already stable or fabrication processes which have been optimized for a single component.

Regarding the reliability, the plot demonstrates that RPN (and also the number of failure mechanisms detected) tends to decrease when the dispersion of the process decreases. This proves that the stability and repeatability of the process is very important to develop reliability improvements on the design. Moreover, the compromise between adaptability and fabrication process dispersion should be taken into account when assessing Design for Reliability in RF-MEMS devices.

In conclusion, any improvement in the design can be assessed only once the process dispersion is low and under control. This means that the Design for Reliability implementation strategy is different depending on the TRL of the fabrication process.

Design for Reliability in low TRL environments

The most flexible fabrication process allows all types and configurations in the same wafer which is the big advantage for addressing different applications. On the other hand, the dispersion over the wafer and from wafer to wafer is very high. For this reason, in this case the most suitable strategy to improve the reliability is to modify and adapt the fabrication process steps.

This last sentence seems to be contradictory but it is not. When addressing reliability through the design, the first thing that should be assured is the repeatability of the fabrication process. If it is not the case, the modifications in the design could not be efficient enough since from one run to another, the parameter targeted by the improvement could change. This was done in Chapter 2 where the flexibility of the process allow the introduction of annealing steps and 3rd metal layer to compensate the deviations due to stress gradient

In general for high dispersion processes, the design flow for RF-MEMS devices and circuits that should be used in this case is shown in Fig. 5-2. Depending on the application and desired performance (frequency band, RF performance, lifetime...) the type of switch is chosen (resistive and/or capacitive, shunt and/or series). For example, for low frequency wide bands (DC to 30GHz), a resistive series switch will be more suitable than a capacitive series one. On the other hand, if the working frequency band is over 30GHz, either a capacitive switch is used (if bandwidth is small enough) or two series switches are cascaded. When the switch is chosen, the fabrication process steps are defined.

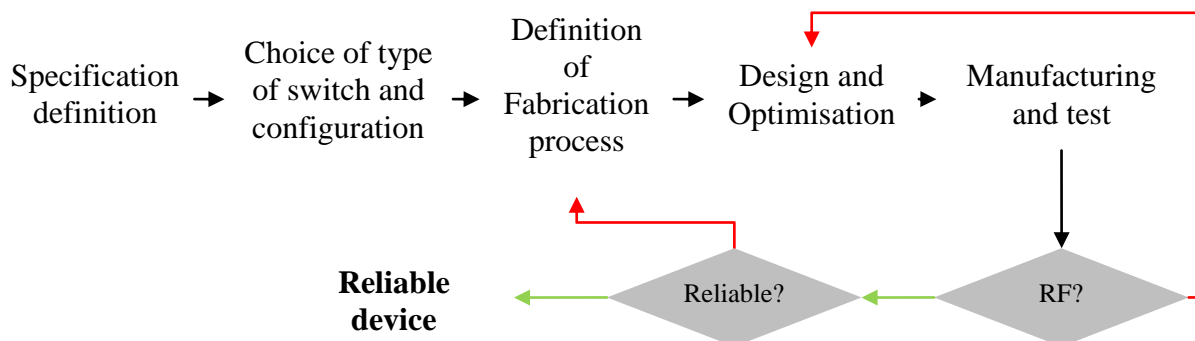


Fig. 5-2: Design flow for a low TRL processes

Afterwards, the design and/or optimization is conceived (from zero or from previous developments) taking into account the reliability challenges of the chosen type of switch and

regarding the desired specifications. Thanks to the high adaptability of these processes, the Rf performance can be optimized through the re-design of the device. Finally, the reliability tests will show the necessity of improvements in the switch which will be done by means of changing specific process steps as was justified above.

In conclusion, the compromise between of adaptable solutions for reliability improvement and the fabrication process dispersion is the most critical point of low TRL environments. That is why the reliability improvements by means of modifying steps of the fabrication process is the best option. This means that these developments should always take into account whether and at which costs/times the proposed process flow could be transferred on an industrial (i.e. high TRL) manufacturing process.

Design for reliability in high TRL environments

Fabrication processes with low dispersion are used in high and medium TRL environments at a price of lower adaptability. The dispersions happen not only over the entire wafer but also from wafer-to-wafer. CEA-Leti for example has dispersions about 5% over the wafer (no information has been reported for wafer-to-wafer dispersion) and IHP has 5% over the wafer and 10% from wafer-to-wafer (see Chapter 3 and 4 respectively). Noteworthy is that bringing this assumption to the limit, the possibility of using professional fabrication process (fabless) can be a solution in order to omit the cost of the optimization process steps.

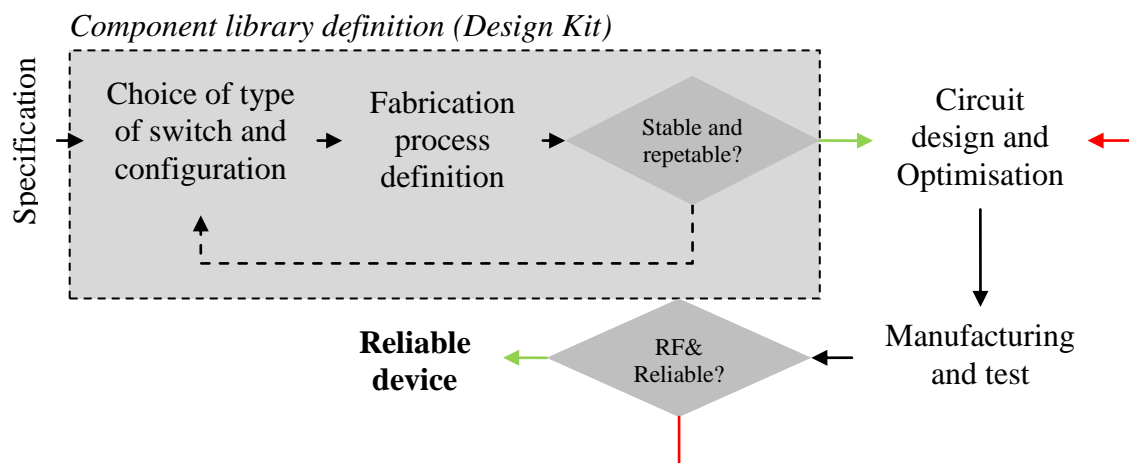


Fig. 5-3: Design flow for medium/high TRL environments. The steps in the dotted square are done only once and provide a design library with the developed components. The designer cannot interact in these steps.

The approach used in this case is the optimization of the switch regarding a fixed fabrication process whose deviations have already been controlled. The suitable design flow in this case is changed as shown in Fig. 5-3.

In this case the fabrication process is developed starting from specific market needs (for example the BiCMOS for mm-wave application in IHP). The MEMS device is conceived upon this process by introducing as minor changes as possible in order to complete the existing component library. This enables the monolithic integration (SOC approach) of MEMS with other technologies. The first step in the design of the library component is to define a mechanically and thermally stable movable part. Afterwards, the general RF performance optimization (losses as low as possible, maximum isolation...) will be carried out. This defines a library of components that will be used in more complex circuits (dotted square in Fig. 5-3).

Once the component library element has been finalized, it can no longer be modified by the designer while conceiving more complex circuits. Similarly, lifetime improvement can be

implemented at circuit level by introducing a BIST solution which does not implies modifications of the MEMS part. At this stage, the desired performance for a specific application will be taken into account. Due to the restrictions in RF configurations coming from the low adaptability of the switch, the design of more complex circuits is basically based on smart and original use of the basic ones available (e.g. use of shunt switch and $\lambda/4$ line to realize an SPDT, instead of using only series switches). An example of this was done for the design of the SPDT in Chapter 3 where the T-junction was optimized for a maximum isolation (35dB in Ku-Band) since the switch reached only 25dB in the same band.

Even if the fabrication process dispersion is very low, it is very important to see if it has a relevant influence on the device performance or reliability. This can be done by means of identifying the parameters that can be used as indicators: for example, a very low pull-in voltage could mean a lack of stiffness on the device as was observed in Chapter 4. Taking into account this, the yield of the process can be improved from an application point of view by means of defining a BIST which could compensate the unavoidable deviations of the device during lifetime.

To sum up, the decision to optimize each step of the fabrication process has a direct consequence on the reduction of dispersions. The main drawback of this approach is the low adaptability. Since the dispersions are controlled, the best way to enhance reliability is through the design or by developing external BIST circuits to control the device or circuit performance over lifetime, never modify the device design.

Co-integration with other technologies

RF-MEMS devices and circuits are supposed to be integrated in more complex systems as was described in Chapter 1. This is not the only reason why the co-integration is important; another one is the opportunity for reliability improvement by means of BIST circuits. It can only have sense to develop a BIST circuits when fabrication process dispersions are known and controlled. For this reason, this section only deals with high and medium TRL environments.

BIST circuits have two constitutive parts (Fig. 5-4): a sensing network in charge of track the critical parameters and a logic control circuit whose aim is determine the optimal actuation conditions during lifetime.

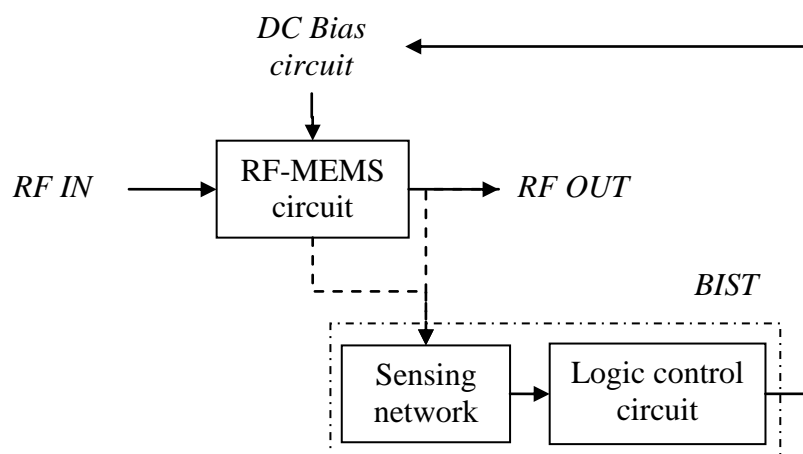


Fig. 5-4: Block diagram of RF-MEMS based circuit with BIST circuit

The sensing network should be able to read at each moment during lifetime the parameter that is used as indicator. It can be either an intrinsic parameter of the device (C_{MEMS} , R_{ON} , $V_{PI}...$) or a specific circuit designed with this aim. An example of a specific circuit could be a

capacitance under the membrane that is able to track the evolution of the UP and DOWN capacitance versus time (solution adopted by MEMtronics [94]). In both types of switches (resistive and capacitive), the easiest parameter to track is the capacitance between the electrode and the movable part in order to disturb as less as possible the normal running of the device.

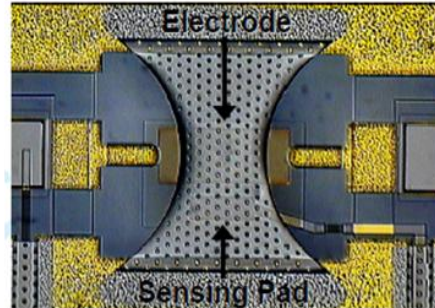


Fig. 5-5: Photo of the MEMtronics switch with the sensing pad extracted from [94]

The component approach used for example by CEA-Leti (medium TRL) directly implies the use of flip-chip or wire bonding techniques for co-integration. This is called “pick-and-place” solution and can be a very adequate for reflect array antennas as was demonstrate in ARASCOM²⁴ project. However, in this case, the combination with a BIST circuit is more difficult and all the reliability issues should be solved beforehand (Design for Reliability) with a robust reliable device.

It is important to note that all the fabrication process which enables the co-integration with BiCMOS processes are in high TRL environment. There are three main advantages of MEMS in BiCMOS processes: the possibility of develop a BIST system, the low dispersion of the process and the flexibility in configuration of the device. The third advantage remains in the possibility of using the different metal levels of the standard BiCMOS process in order to change the configuration (as was done in Chapter 4). Another fourth advantage (considered when working at frequencies over 80GHz) is that the interconnection losses between systems are lower than in flip-chipped/wire-bonded circuits.

5.3 Evaluation of other existing RF-MEMS fabrication process

The conclusions extracted from the comparison done in previous section can be extended to other existing RF-MEMS fabrication processes. The most critical part is the definition of their TRL. This has been relatively easy for the processes of Chapter 2 to 4 but it can be quite subjective for the rest. In this section the justification of the TRL selection is done in order to check the relationships observed on the radar curve observed in Fig. 5-1. Among the large number of available RF-MEMS fabrication processes, only a small but representative number has been considered, spanning from research to industrial and commercial ones as explained in Table 5-2.

The TRL associated to the process have been assigned subjectively from information available at the moment. Rather than the exact value of the TRL, the classification has been done upon the following categories: low (1-TRL to 4-TRL), medium (4-TRL to 7-TRL) and high (7-TRL to 9-TRL). Another remark is that companies which use fabless approach

²⁴ ARASCOM (Agile Reflectarray Antennas for Security & COMMunication) is supported by the European Commission, in the frame of the 7th Framework Research Program "FP7" ("ICT / Micro-Nano Systems" theme / Grant Agreement n°222620). It has begun on May 15th, 2008-2011 and was headed by Thales Alenia Space.

(Wispry, MEMtronics, Baolab...), usually found in high TRL environments, are not considered in this comparison. The only exception which is considered is DelfMEMS where the fabrication process is still proprietary even if they are actually using Tronics facilities [95].

	Foundry	TRL	Comments
Low TRL	KTH	3	Research institute of Royal Institute of Technology Microsystem Technology Laboratory at KTH Different configurations and possibilities are being explored for reliable design of RF-MEMS circuits (see Chapter 1)
Medium TRL	FBK	4-5	Research institute from University of Perugia Spin-off “RF Microtech” All configurations in same substrate (Silicon or Quartz) Prototypes and medium-scale manufacturing
	XLIM	5-6	Research institute from CNRS and University of Limoges Capacitive and resistive switches demonstrators ²⁵ Spin-off “AirMEMS”
	DelfMEMS	7	Spin-off from CNRS Owns manufacture process and has a partner for future mass production (Tronics) No product is nowadays available
High TRL	Omron	9	Develops commercial electronic components such as SPnT.
	Radant	9	Commercial SPnT from DC to 30/40GHz

Table 5-2: Chosen process with the given TRL and its justification

Using the same indicators than in previous section, a radar chart for each group is plotted: low TRL (Fig. 5-6), medium TRL (Fig. 5-7) and high TRL (Fig. 5-8). In this case the dispersion of the process is unknown and for this reason it is removed from the study. The failure mechanisms were determined by the type of switch and the reliability performance available:

- KTH: Ru-Ru based switches [97]: stiction and structural short (RPN: 180). No information provided for [98]
- FBK [99]-[100]: breakdown, dielectric charging, ESD (RPN: 160)
- XLIM: AirMEMS device: creep [101] (RPN: 120)
- DelfMEMS: stiction [102] (RPN: 40)
- Omron: fatigue and stiction [103] (RPN: 120)
- Radant: stiction [104] (RPN: 40)

²⁵ XLIM has participated in MEMO Program (CNES – Centre National d’Etudes Spatiales) which aims at prove in-orbit MEMS reliability [96]

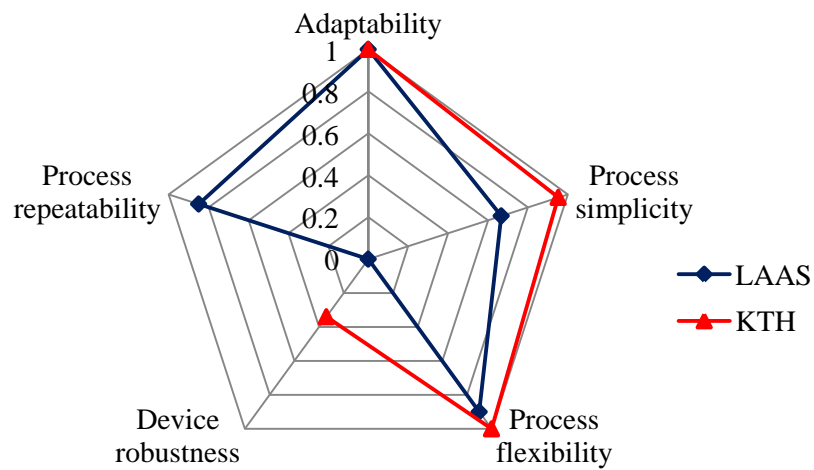


Fig. 5-6: Radar chart for low TRL environment

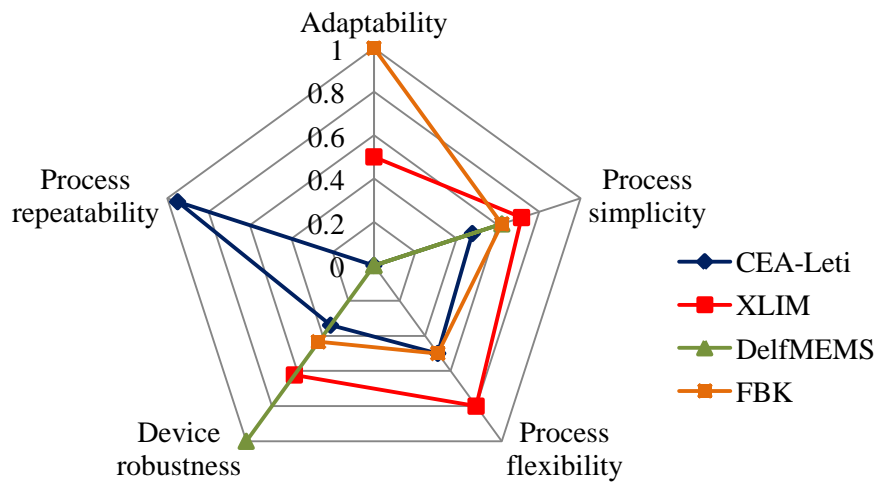


Fig. 5-7: Radar chart for medium TRL environment

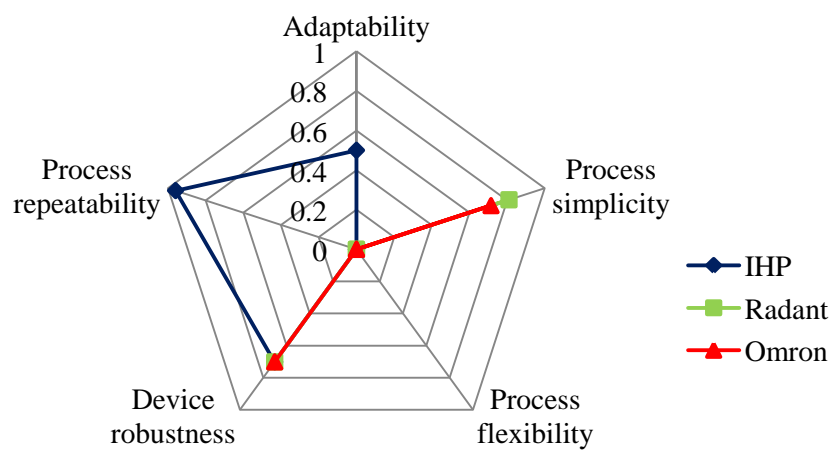


Fig. 5-8: Radar chart for high TRL environment

The curve of each process is very similar when comparing with the same TRL level. For low TRL, the processes are flexible and adaptable but at a cost of higher reliability problems. On the other hand, the processes are simple (low number of masks and steps needed) which means lower development costs²⁶. In the case of DelfMEMS, the curve has similar characteristics as the high TRL processes due to the fabrication process restrictions imposed by the fabless approach. Finally, for high TRL environment, all the parameters are reduced. However, in the case of IHP the complexity of the process is very high due to the co-integration with BiCMOS. In conclusion, the reliability improvement procedure fixed in previous section is also valid for fabrication process of the same TRL environment.

5.4 General conclusions and perspectives

This thesis has presented how reliability can be enhanced in three different RF-MEMS fabrication processes. The development of an equivalent circuit based on the physical characteristics (size, dimensions, materials...) of the different devices have been the chosen tool for RF performance monitoring versus time. Since each component of the equivalent circuit is associated to a particular part of the device, the detection of failure mechanisms has been done by monitoring this component and studying its impact on the global performance of the device.

The proposed reliability solutions are based on the re-design of the structure and its manufacturing process (Design for Reliability). Depending from the process TRL the design for reliability which applies is different. In all cases, the most relevant parameter that should be taken into account to afford Design for Reliability is the process dispersion. For low (1 to 4) TRL processes the optimal strategy remains in the modification of the fabrication process steps. In medium and high TRL environments (4 to 9) the reliability enhancement should be done through the design (for example adding a BIST circuit) but never modifying the standard component.

In particular, for low TRL process (LAAS-CNRS) the opportunity to modify the process steps represents the recommended choice to face reliability. For instance an additional metal layer over the movable part is proposed in order to reduce the DOWN capacitance dispersion and to increase the stiffness of the cantilever. For resistive switches the proposed solution was the optimization of an annealing step in order to reduce the deflection due to initial stress. This prevents the dimples to contact the transmission line. Both solutions were adopted because the in-wafer and wafer to wafer dispersion was too big (15% and over 50% respectively).

For medium TRL environment (CEA-Leti) the monitoring of the contact resistance was studied under different RF power level through the contact. Preliminary results have shown that the higher the RF power through the contact (P_{RF}), the lower the number of actuations needed for a stable contact (N_{AC}). These results were very likely affected by the carbon contamination of the contact due to the non-hermetic package. In order to confirm the relationship between N_{AC} and P_{RF} it was proposed to repeat the same protocol under a controlled environment. No design for reliability can be applied without this total comprehension of the failure mechanism.

For high TRL process (IHP), the fabrication process dispersion origin was identified. The critical parameter to track is the UP and DOWN state capacitance responsible of the RF performance deviation in the initial state. The advantage of using lumped-elements based

²⁶ The cost of the process is related with the cost of the set mask used and the number of steps. The differences in photolithography mask layers, minimum feature size and reticle size determine the price. For example, BiCMOS processes use about 20-26 masks which cost \$100-180k per unit.

circuits in the design of circuits is based on simple DC or LF measurement resides in the dramatic reduction of the testing time.

For the IHP shunt switch, long-term reliability tests have demonstrated that the failure mechanism is the mechanical fatigue and creep. However, a simple device screening procedure based on actuation bias monitoring of pristine devices ($V_{\text{POUT}} > 36$ & $V_{\text{PIN}} - V_{\text{POUT}} \leq 1$) has been proposed. A 67h of continuous DC stress in harsh environments (22° and 45% humidity) was experimentally observed. This approach is based on the measurements of the distance between membrane and electrode or line in rest position (without actuating the switch). This technique is non-intrusive and can be implemented in mass-production by monitoring specific test vehicle device or using the final devices ahead of packaging.

The possibilities in terms of adaptability (five metal levels) that the BiCMOS process from IHP presents have allowed designing a reliable series switch. The same movable membrane previously developed by IHP (shunt switch) was reused as it was, and only the layer interconnect was modified and optimized. This new development has been possible thanks to the equivalent circuit model which allowed carrying out the analysis of existing devices so as the synthesis of the new ones.

Five parameters have been defined in order to compare the different TRL environments: adaptability, process simplicity, process flexibility, device robustness and process repeatability. The processes with similar TRL draw similar correlations between the different parameters. For this reason, for processes with equivalent TRL, very similar conclusions can be drawn and the analysis done for three considered MEMS processes can be extended to other existing fabrication processes.

The adaptability and flexibility of the process has played a very important role in order to obtain optimal RF performance. The best RF behavior for SPnT was obtained with low TRL environment because it was allowed to dispose the switches in different orientations than from vertical or horizontal as was the case in medium and high TRL processes. On the other hand, the repeatability of the process limits the future commercialization of these circuits.

Another RF-MEMS application that has been developed in this thesis is the absorptive switches. It has been developed in the IHP process due to the possibility to integrate resistors. The novel configuration has very low power consumption (the switches either all ON or all OFF), a minimum number of switches (2) and it is insensitive to the resistor tolerances. This circuit is currently under fabrication.

This thesis has intentionally not focused on the packaging issue. In spite of the fact that packaging is instrumental for the correct functioning of the device (An unpackaged RF-MEMS is not a MEMS). The main reason is that in order to carry out experimental observation (e/g. membrane profile), unpackaged devices were often needed. For what concerns effect of the environment it must be pointed out that the tests have been done always under the same conditions so to guaranty a fair comparison of the experimental results. Despite being out of the scope of the thesis, from the designer point of view, the packaging should also be considered from the very beginning of the design stage.

As a very general conclusion, looking at the future of RF-MEMS, two types of research have to be done: the study of the underlying failure mechanisms and the development of stable fabrication processes typically carried out in low and high TRL environment respectively. The close proximity of these two environments is instrumental to accelerate the time to market of future innovative RF-MEMS concepts. The solutions adopted for the low TRL should always take into account if a higher TRL process could, in the future, implement this

solution. From the other side, medium and high TRL processes should always take into account the know-how acquired in lower TRL environments.

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Acronyms List

ADS – Advanced Design System

BCB – BenzoCycloButen

BIST – Built-In Self-Test

CEA-Leti – Commissariat à l’Energie Atomique – Leti

CNT – Carbon Nano Tubes

CPW – Coplanar Waveguide

CTE – Coefficient of Thermal Expansion

DC – Direct Current

DfR – Design for Reliability

DUT – Device Under Test

ESA – European Space Agency

ESD – ElectroStatic Discharge

EVM – Error Vector Magnitude

FBK – Fondazione Bruno-Kessler

FMEA – Failure Mode and Effect Analysis

GPIB – General-Purpose Instrumentation-Bus

IHP – Innovations for High Performace microelectronics

IL – Insertion Losses

KTH – Royal Institute of Technology

LAAS-CNRS – Laboratoire d’Analyse et d’Architecture de Systèmes – Centre National de Recherche Scientifique

LF – Low frequency

LNA – Low Noise Amplifier

MIM – Metal-Insulator-Metal

NASA – National Aeronautics and Space Administration

nPnT – n-Pole n-Through

PECVD – Plasma-Enhanced Chemical Vapor Deposition
PLL – Phase Lock Loop
PNA – Performance Network Analyzer
PS – Phase shifter
R&D – Research and Development
RF-MEMS – Radio Frequency MicroElectroMechanical Systems
RIE – Reactive-Ion Etching
RL – Return Losses
RPN – Risk Priority Number
Ru – Ruthenium
T – Temperature
TCV – Technology Characterization Vehicle
TL – Transmission Line
TRL – Technology Readiness Level
VNA – Vector Network Analyzer
WLP – Wafer Level Packaging

List of Publications

International Conferences

N. Torres Matabosch, F. Coccetti, R. Plana, B. Reig and J.L. Cazaux “High Isolation T-switch for reconfigurable switching Matrix”, *11th International Symposium on RF MEMS and RF Microsystems MEMSWAVE2010*, Otranto, Italy 2010

N. Torres Matabosch, F. Coccetti, M. Kaynak, W. Zhang, B. Tillack, R. Plana, J.L. Cazaux “An Accurate and Versatile Equivalent Circuit Model for RF-MEMS Circuit Optimization in BiCMOS Technology”, *European Microwave Integrated Circuits Conference 2012* , 4 pages, Amsterdam, The Netherlands, 2012

N. Torres Matabosch, F. Coccetti, M. Kaynak, W. Zhang, B. Tillack and J.L. Cazaux, “An Accurate Equivalent Circuit Model for RFMEMS Circuit Optimization and Fabrication Process Monitoring in BiCMOS Technology”, *13th International Symposium on RF MEMS and RF Microsystems MEMSWAVE2012* , Antalya, Turkey, 2012

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