Développement et fabrication de transistors couches minces verticaux en technologie silicium polycristallin basse température

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Development and Fabrication of Vertical Thin Film Transistors Based on Low-Temperature Polycrystalline Silicon Technology

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devant le jury composé de :

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Peng ZHANG

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General introduction

The scale-down of CMOS technology has followed Moore's law for around a half century, especially for the recent two decades, the doubling of transistors has continuously taken place every eighteen or twenty-four months. However, when CMOS is scaled into sub-100 nm regime, it has already shown short channel effects (SCEs), which limits the electrical performance of CMOS devices and circuits. When the micro processor unit (MPU) node shrinks to 16 nm expected in 2013, more problems may emerge. On one hand, quantum tunneling will result in large leakage, regardless of the adopted materials. On the other hand, higher resolution requirements in the lithography and plasma etching techniques prohibit the reliability of the fabricated devices. Therefore, new FET architectures should be proposed.

The three-dimensional (3D) FET has been proposed ahead of time, i.e., *Intel* Corp. proposed the tri-gate FinFET in 2011 and adopted it in the 22 nm node CPU. Due to the wrapped gate of FinFET that could provide better electric field controlling, the leakage current has reduced one order of magnitude due to the coupling of the gates (work as a double-gate FET), in comparison with the 32 nm planar FET. This result has indicated the advantage of the 3D FET, and a lot of other 3D FET structures have also been proposed, including the inverted-T channel FET, the Omega-gate FET, the Pi-gate FET, the four-gate FET, the Gate-All-Around (GAA) FET, and so forth. However, on one hand, due to the more complex process, these alternative 3D structures have not yet been adopted. On the other hand, including FinFET, these 3D structures are still limited by the lithography and plasma etching techniques. In addition, the high sidewall roughness observed from FinFET has been a common technological challenge for the 3D FETs.

Another FET structure has been proposed by rotating the planar FET 90°, so-called "vertical FET". On one hand, the channel length of this vertical structure is determined by the deposited layer thickness between source and drain, thus it is independent of the lithography technique. On the other hand, the ultra-short channel length could be obtained with a large channel width, which enables to increase the drive current. In addition, the vertical architecture also enables to realize a double-gate or multi-gate structure, which further

improves the electrical performance. Therefore, vertical FET is also a promising structure to pursure Moore's law.

In the laboratory of IETR, thin film technology has been well developed, with different thin film materials and deposition techniques. Especially for polycrystalline silicon (poly-Si), mature low pressure chemical vapor deposition (LPCVD) and solid phase crystallization (SPC) techniques have been adopted for low-temperature ($T \leq 600°C$) thin film transistors (TFTs) fabrication. Therefore, our laboratory has proposed a vertical thin film transistor (VTFT) structure based on this low-temperature poly-Si technology. This thesis deals with the research on this special VTFT structure. The organization of this thesis is shown below:

In the first chapter, the state of the art for the new FET structures will be introduced. Initially, the scale-down tedency of MOSFETs will be presented. Afterwards, the fabrication process of the lateral thin film transistors (LTFTs) will be given step by step, and the work principle of a MOSFET will also be presented based on the LTFT. Subsequently, different 3D structures, including FinFET, will be given. At the end of this chapter, vertical FET structure will also be proposed, with its advantages over the planar FET structure.

In the second chapter, the VTFT structure will be proposed by rotating LTFT 90°. Different thin film materials and techniques adopted in the fabrication process will be detailed, especially for the low-tempertaure poly-Si technology. Afterwards, the fabrication process of the classical VTFTs will be presented in detail step by step. Static electrical measurements will be shown and analyzed, highlighting some problems related with the proposed VTFT architecture, and some solutions will also be given to improve the electrical properties by modifying some steps of the technological process.

In the third chapter, a new VTFT structure will be proposed, in order to radically solve the problems in the classical VTFT structure. Initally, the theoretical analysis of this new structure will be presented. Subsequently, the fabrication process of the new VTFT structure will be shown step by step. The technological challenges of the new VTFTs will be given, and the electrical characteristics will be presented and analyzed, in comparison with the electrical properties of the classical VTFTs. Based on the analysis of the electrical characteristics of the

fabricated VTFTs, several attempts will be made to improve the electrical characteristics step by step. Moreover, P and N-type VTFTs will be fabricated, highlighting the feasibility of a CMOS-like VTFT.

Finally, we will conclude the study on poly-Si VTFTs, and we will also present some perspectives for future work on our VTFTs.

Chapter 1 Introduction

I. Development and revolution of MOSFETs

Since the first MOSFET was fabricated in 1960 by D. Kahng and M.M.Atalla of Bell Telephone Laboratory [1, 2], the semiconductor industry has undertaken a tremendous revolution based on CMOS circuits. The scale-down of the planar transistors has followed Moore's law for around half century, especially for the recent two decades, the doubling of transistors has continuously taken place every eighteen or twenty-four months [3, 4]. However, the scale-down tendency will see its restriction when the micro processor unit (MPU) node shrinks to 16 nm expected in the 2013 timeframe of the International Technology Roadmap for Semiconductors (ITRS) shown in figure 1-1 [5]. This limitation is mainly due to two reasons: on one hand, quantum tunneling due to the short channel length would enlarge the leakage as well as serious short channel effects (SCEs), regardless of the adopted materials. On the other hand, the high resolution requirements in the lithography and plasma etching techniques prohibit reliable and mass production. Therefore, new FET architectures should be proposed and adopted in order to break through this limitation.

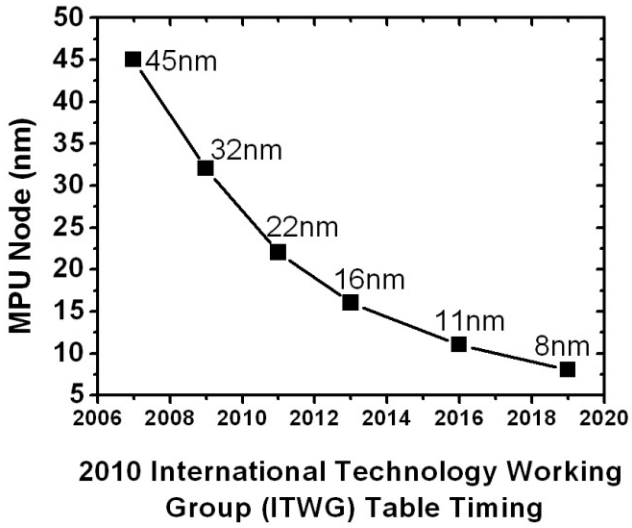


Figure 1-1: Evolution of the MPU node provided by *ITRS* 2010, the 16 nm node was expected in 2013.

Fortunately, the semiconductor industry has found the solution for overcoming the former challenge of leakage ahead of time, by adopting the new three-dimensional transistors (3D transistors), which enable to form wrapping gate structures. *Intel* Corp. announced its tri-gate FinFETs manufactured at 22 nm in 2011 [6, 7], which greatly improves the electrical

characteristics in comparison with its 32 nm planar transistors. FinFETs for 16 nm manufacturing process are also being developed by *Intel*, *IBM*, *Samsung*, *Toshiba* and other corporations [8 - 11].

Another concept of 3D FETs, the vertical MOSFETs has also been proposed by rotating the planar MOSFETs 90°, thus the channel length could be defined by a non-lithography method instead of improving the lateral resolution [12, 13], which would enable to simplify the process. In addition, for the vertical MOSFETs, the leakage could also be well-controlled by introduction of the multi-gate structure. In summary, vertical MOSFETs could be another classification of promising FETs to pursue the Moore's law.

Considering the thin film technology, thin film transistors have also been developed to pursue this scale-down trend. Not only the lateral thin film transistors (LTFTs) have been developed corresponding to the planar MOSFETs, but a lot of 3D thin film transistors have also been proposed, including vertical thin film transistors (VTFTs), which correspond to vertical MOSFETs.

II. Lateral Thin Film Transistors (LTFTs)

III.1 Introduction of LTFTs

Before the description of different three-dimensional FETs, the basic principle of the MOSFETs should be presented by taking the traditional planar transistors as an example. As the wide usage of the thin film technology, the lateral thin film transistors (LTFTs) have been researched for about a half century [14-16]. In the microelectronics laboratory in IETR (Institut d'Electronique et des Télécommunications de Rennes), lateral thin film transistors (LTFTs) have also been fabricated and studied for over a decade [17, 18]. Based on the LTFTs technology, the prototype of the vertical thin film transistors (VTFTs) will be proposed.

In this section, the simplified fabrication process of LTFTs is shown step by step. Afterwards, the basic working principle of transistor will be expressed by taking the LTFT as an example, and the typical transfer and output characteristics of the LTFT will also be analyzed.

III.2 Fabrication process of LTFTs

In our laboratory, the fabrication of the LTFTs (N and P-type) is based on the fabrication process of the planar MOSFETs. For the planar MOSFETs, the source, drain and channel parts are formed in the monosilicon body, and the doping is achieved via high-temperature diffusion or ion implantation methods.

In contrast, all the parts of the LTFTs are formed by using silicon thin film technology. Among the different silicon deposition techniques, LPCVD technique has been proved to have the largest grain size and the best reliability by involving the solid phase crystallization (SPC) technique. In addition, for LPCVD, the source and drain could be *in situ* doped by dopant injection during the deposition process. Therefore, this mature low-temperature LPCVD technology has been widely used for our LTFTs fabrication [19, 20]. Moreover, the process can be fully compatible with the glass substrates, as the maximum temperature can be limited to 600°C. Therefore, it enables the applications in the display field, such as the active matrix liquid crystal display (AMLCD), the active matrix organic light-emitting diode (AMOLED) [21 - 23], and so on.

The fabrication of the LTFTs could be achieved either by a bilayer method, or by a monolayer way [24]. For the bilayer method, the source and drain heavily-doped layers (labeled as "N+") are deposited after the definition of the active layer (labeled as "Undoped") by an etching step (the two layers are not deposited at the same time), while for the monolayer method, the two layers are continuously deposited prior to the definition of the active layer, which can be shown in figure 1-2 (a) and figure 1-2 (b), respectively.

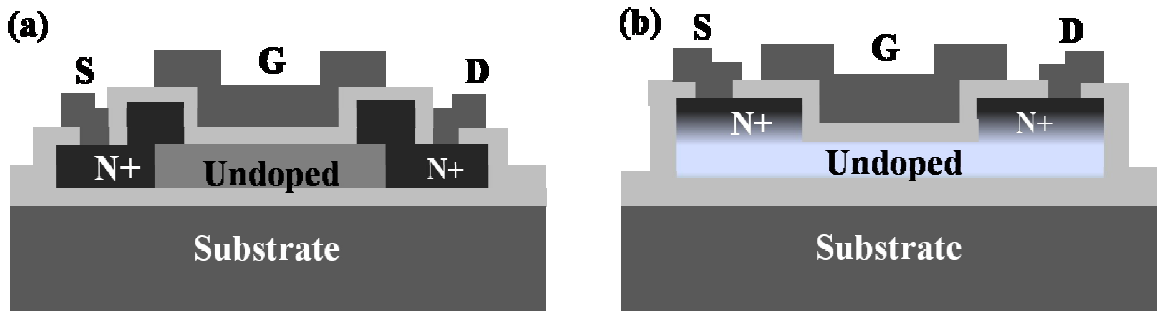


Figure 1-2: Schematic view of *(a)* a bilayer LTFT, and *(b)* a monolayer LTFT [24].

Note that, for the monolayer method, due to the continuous depositions of the two layers, the interfacial defect densities between the two layers are much less than the ones for the bilayer method. Therefore, the fabrication of the monolayer LTFTs will be described in detail with a four-mask process [25].

The fabrication process of the LTFTs begins with the deposition of the buffer oxide. After cleaning the substrates, a thick 500 nm silicon oxide layer is deposited by Atmospheric Pressure Chemical Vapor Deposition (APCVD) method. The LTFTs are fabricated on this buffer oxide layer, and thus the devices could also be isolated from each other.

Afterwards, the polycrystalline silicon (poly-Si) layers are deposited by the Low Pressure Chemical Vapor Deposition (LPCVD) technique. After the deposition of a 150nm undoped poly-Si layer, another 150nm N-type highly-doped poly-Si layer is continuously formed by *in situ* doping using phosphine gas PH_3 (while P-type poly-Si layer is formed by *in situ* doping using diborane gas B_2H_6). Due to the same processing flow of the N and P-type LTFT, the fabrication process of the N-type LTFT is taken as an example, and the schematic structure for the deposited layers is shown in figure 1-3:

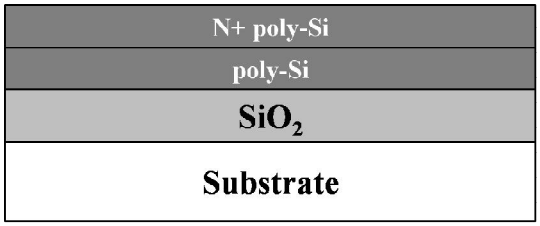


Figure 1-3: Schematic structure after the deposition of two poly-Si layers by LPCVD technique. “N+” stands for the N-type heavily-doped poly-Si layer, and “poly-Si” stands for the undoped poly-Si layer.

After the deposition of the two poly-Si layers, the first mask is used and then the first reactive ion etching (RIE) is carried out to form poly-Si islands, as shown in figure 1-4. For each LTFT, source, drain and the active layer will be included in the same island, thus the size of one single LTFT is determined by the island dimension.

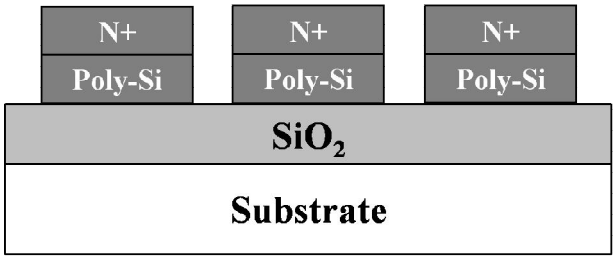


Figure 1-4: The first RIE step to form the poly-Si islands, whose dimensions would determine the sizes of the LTFTs.

After the definition of the poly-Si islands, the second mask is used and a second RIE is carried out to etch the N-type heavily-doped poly-Si layer (labeled as "N+") until reaching the interface between the heavily-doped poly-Si layer and undoped poly-Si layer (labeled as "Poly-Si"), and thus source and drain are formed for each LTFT, which is shown in figure 1-5:

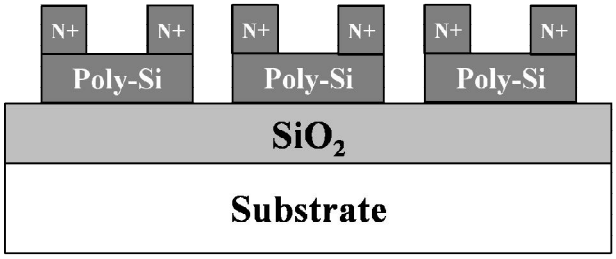


Figure 1-5: The second RIE is carried out to form source and drain of the LTFTs.

Before the deposition of the gate oxide, a standard RCA cleaning is necessary in order to eliminate most of the impurities at the interface between the undoped poly-Si layer and the gate oxide, as the channel would be formed near this interface. Thus, RCA cleaning enables to improve the electrical characteristics of the fabricated LTFTs.

After the RCA cleaning, a 100 nm SiO_2 thin film layer is deposited by APCVD technique followed by a densification process at 600°C for at least 12 hours. Afterwards, a third mask is used and wet etching is carried out to make contact openings for source and drain. The final schematic structure after gate oxide deposition and wet etching is shown in figure 1-6:

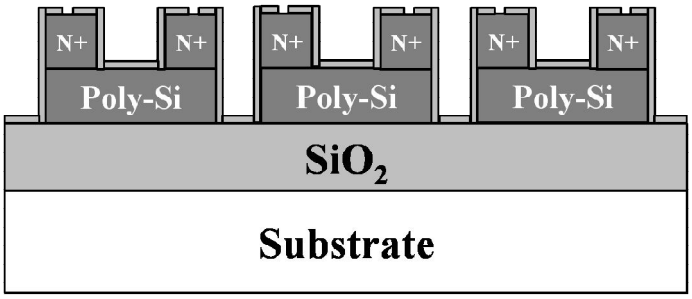


Figure 1-6: Gate oxide deposition and wet etching to make contact openings.

The final step is the formation of aluminum (Al) contacts for source, drain and gate. After the deposition of a 300 nm Al layer by Joule effect evaporation method, the source, drain and gate contacts are formed by wet etching using the fourth mask. The final schematic structure of the fabricated LTFTs is shown in figure 1-7:

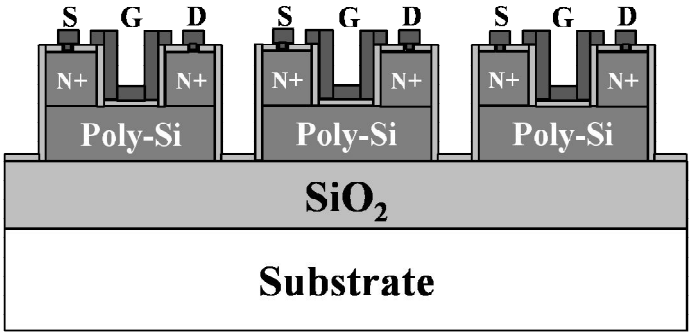


Figure 1-7: Schematic structure of the final LTFTs, the deposited Al is etched and the contacts are formed.

As mentioned above, except for the fabrication of the N-type LTFTs, P-type LTFTs are also fabricated in our laboratory, and thus the P and N-type LTFTs could be complementarily arranged on the same substrate (so-called "CTFTs"), which corresponds to the CMOS technology [26]. Based on the CTFTs technology, the CTFT inverters are achieved, and other circuits based on LTFTs are also fabricated [27].

III.3 Basic working principle of LTFTs

Corresponding to the classical MOSFET, the schematic of a single N-type normally-off LTFT using thin film technology is shown in figure 1-8. For the gate part, the multi-layer Al/SiO_2/poly-Si also forms the Metal-Oxide-Semiconductor (MOS) structure, thus the working principle of the N-type normally-off LTFTs will be explained using the equivalent

planar MOSFETs.

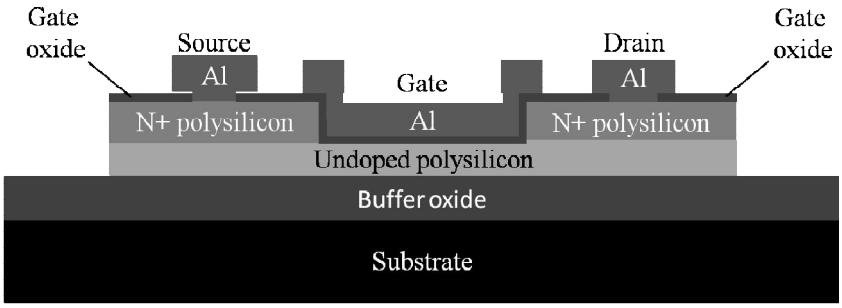


Figure 1-8: Schematic view of the N-type normally-off LTFT.

In order to simplify the explanation of the working principle, the three-dimension schematic for the gate part of the N-type normally-off LTFT is shown in figure 1-9, source and drain are at the left and right part of the undoped poly-Si (not shown in figure 1-9), and the channel will be formed in the area below the gate oxide and the gate metal contact. The important geometric parameters for the LTFT are listed below:

- L: channel length, determined by the gate coverage length from source to drain;
- W: channel width, determined by the gate coverage width perpendicular to the channel length L;
- T_{OX}: the thickness of the gate oxide layer;
- T_{si}: the thickness of the undoped poly-Si layer, determining the depletion type of the LTFT (full depletion or partial depletion).

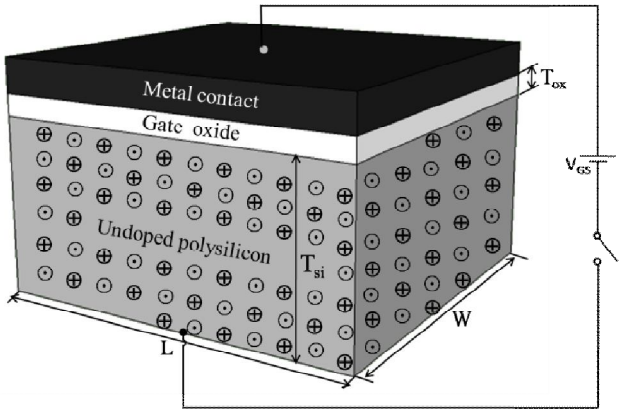


Figure 1-9: The MOS structure of a LTFT, the geometric parameters are shown. No channel is formed, thus the LTFT is at the off-state.

For the N-type normally-off LTFT, when there's no voltage applied at the gate part, i.e.,

V_{GS} = 0 V, the carriers below the gate oxide keep the charge neutral (shown in figure 1-9), and there is no electrons gathering to form the N-type inversion layer. Thus, the LTFT is at the off-state.

When forward voltage is applied to the gate part of the N-type normally-off LTFT, i.e., V_{GS} > 0 V, the electric field at the gate part would repel the positive carriers, i.e., the holes near the top of the undoped channel, and thus the electrons gather below the gate oxide. When increasing V_{GS} to a value known as the threshold voltage V_{TH}, i.e., $V_{GS} > V_{TH}$, the electrons would gather from the source side to the drain side, thus the channel is formed. When certain forward voltage V_{DS} is applied between source and drain, the electrons from the source are attracted into the undoped poly-Si layer, then they pass through the channel, and finally they are captured by the drain. The schematically electronic circuit is shown in figure 1-10. When continuous voltages of V_{GS} and V_{DS} are applied, the electrons would continuously flow from source to drain, thus the LTFT is at the on-state.

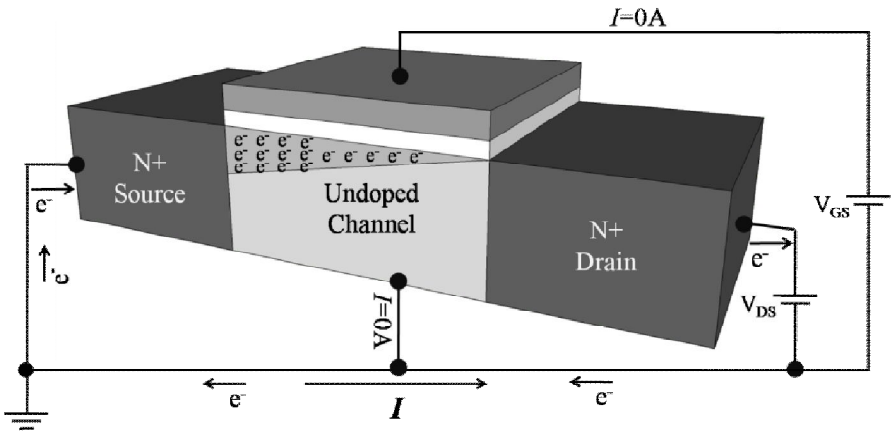


Figure 1-10: The electronic circuit of the LTFT, the channel is formed under the gate forward voltage V_{GS}, and the LTFT is at the on-state.

The typical transfer and output characteristics of the LTFT fabricated in our laboratory are shown in figure 1-11 (a) and figure 1-11 (b), respectively [28]. For the transfer curve, the drain is applied with certain voltage (V_{DS} = 1 V in this case), the signed regions correspond to different states of the LTFT:

① Gate is reverse-biased, thus the LTFT is blocked. The drain current is mainly due to the electron traps and the acceleration of the electrons under the source-drain voltage V_{DS}.

② Drain current I_{DS} reaches the minimum value, which shows the ohmic conduction of the whole active layer.

③ The channel forms and the channel depth increases, which leads to the rapid and linear increase of I_{DS} corresponding to the gate voltage V_{GS}.

④ The channel gradually reaches the maximum depth, thus the drain current I_{DS} reaches the saturation, and the LTFT completely works at the on-state.

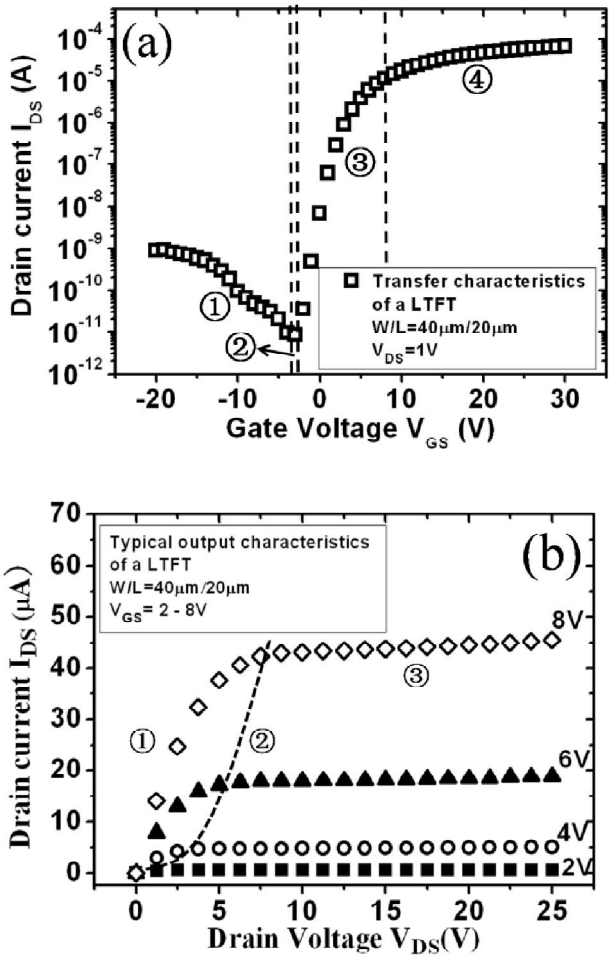


Figure 1-11: *(a)* Typical Transfer characteristics, and *(b)* output characteristics of the LTFT fabricated in our laboratory [28].

From the transfer characteristics curve, the on/off-current ratio I_{ON}/I_{OFF} could be calculated, where I_{ON} corresponds to the maximum value of I_{DS}, and I_{OFF} corresponds to the minimum point. For this example curve, I_{ON} is around 10^{-4} A while I_{OFF} is lower than 10^{-11} A, thus a high I_{ON}/I_{OFF} ratio of more than 10^{7} is gained.

For the LTFT, when the gate is applied with certain voltages higher than the threshold

voltage ($V_{GS} > V_{TH}$), the channel forms. And when the drain is also applied with the bias V_{DS}, the electrons would flow from source to drain via the channel. The outpur characteristics describe the variations of the drain current I_{DS} with the drain-source voltage V_{DS}, which could be divided into three parts with the transition point of $V_{DS\,(sat)} = V_{GS} - V_{TH}$:

① The LTFT works in the linear region. When the drain voltage is low ($V_{DS} < V_{GS} - V_{TH}$), the channel enables the electrons flow from the source to drain, and then the channel works as a resistor, while the drain current I_{DS} increases linearly with the drain-source voltage V_{DS}. With the further increase of the drain voltage V_{DS}, the inversion layer gradually shrink at the drain side when the gate voltage V_{GS} is fixed.

② When the drain voltage is increased to a certain value ($V_{DS\,(sat)} = V_{GS} - V_{TH}$), the inversion layer at the drain side disappears, which is called "pinch-off", and the drain voltage is called "pinch-off voltage".

③ The LTFT works in the saturation region. When the drain voltage V_{DS} exceeds the pinch-off voltage $V_{DS\,(sat)}$, the inversion layer would shrink thus the channel length reduces. However, at the end of the inversion layer, the voltage is kept as the $V_{DS\,(sat)}$, thus the drain current kept as the saturation current $I_{DS\,(sat)}$.

By analyzing the transfer and output characteristics of the LTFT, the quality of the LTFT could be evaluated and the other electrical parameters, such as the threshold voltage V_{TH}, the subthreshold slope S, the transconductance g_m, and the field effect mobility μ_{FE} could also be deduced. The detailed calculation or deduction approaches for these parameters will be presented in chapter 2.

III. Three-dimensional FETs: FinFETs and other alternative structures

III.1 Introduction of FinFETs

In order to satisfy the requirement of the shrinking device size while improving the electrical characteristics, one solution is to develop ultra-thin body silicon on insulator (UTB-SOI) MOSFETs, i.e., fully depleted MOSFETs (FDMOSFETs). A lot of research on

UTB-SOI MOSFETs has been carried out, and promising results have been obtained [29 - 33]. *STMicro* corp. has been pursuing a 14 nm UTB-SOI planar MOSFET, and *IBM* has also proposed a back-gate extremely-thin SOI (ET SOI) solution when using the extremely-thin silicon as the active layer [34]. However, the mass production of the ultrathin body (below 5 nm) requires a high industrial cost.

Another solution, the three-dimensional (3D) FETs have been fabricated and researched since the 80s of last century [35, 36]. Among these alternative structures, the FinFET has emerged as the most representative and promising three-dimensional (3D) FETs, whose development could be traced by the work of Hu Chenming group [37 - 43] in UC Berkeley and Taiwan Semiconductor Manufacturing Company (TSMC). What's more important, the more mature technology and superior characteristics of FinFET over the planar MOSFET enable the semiconductor industry revolution, i.e., *Intel* Corp. announced the 3D FinFET for its CPU technology at 22 nm node in April 2011. The FinFET have been among the most attractive transistor structures for its excellent performance, and a lot of alternative 3D structures similar to FinFET have also been proposed and reported, including Ω-gate FETs, Π-gate FETs, four-gate FETs, gate-all-around (GAA) FETs [44 - 47] and so on.

III.2 Basic working principles of FinFETs

In fact, the 3D FinFET structure has been proposed based on the planar FET structure. Figure 1-12 (a) and figure 1-12 (b) show the planar FET structure and the bulk FinFET structure, respectively, while the SOI FinFET structure is shown in figure 1-12 (c). For planar transistor, source and drain are buried by the Shallow Trench Isolation (STI) layer, thus only the top surface could be used to form the gate structure. In contrast, for the FinFET (bulk or SOI FinFET), source and drain are extruded from the STI plane, thus the gate could be wrapped around the conducting channel that includes the top and two sides of the tall, narrow fin, which enables a better control of the channel. It has been proved that the special double-gate technology has greatly modulated the electric field region, that is, the coupling of the two electric field regions for the two gates has been beneficial for suppressing the leakage and the short channel effects (SCEs).

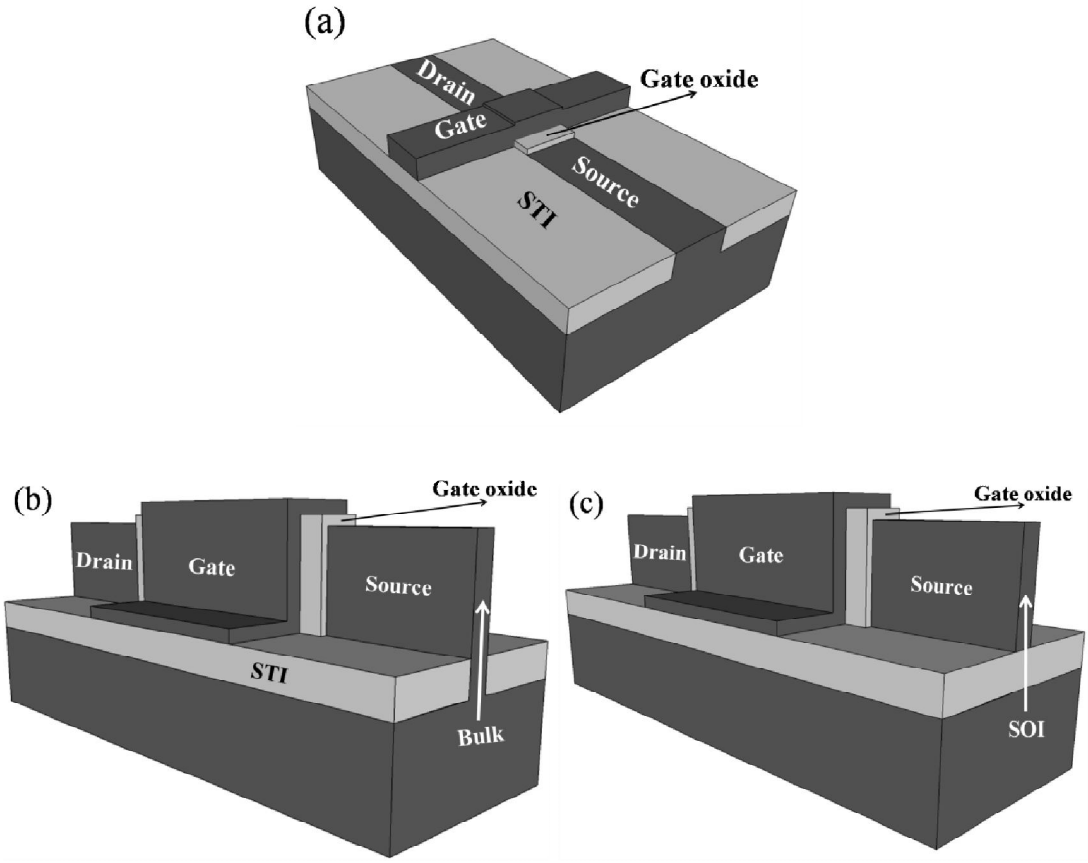


Figure 1-12: Schematic structure of *(a)* a planar FET, *(b)* a bulk FinFET, and *(c)* a SOI FinFET.

In process, the difference between the bulk FinFET and the SOI FinFET, only lies in the definition of source and drain, i.e., for the bulk FinFET, a dry etching process should be undertaken on the silicon body in order to form the tall fin that is protrude from the other part of the body. In contrast, for a SOI FinFET, source and drain are formed in the bonded layer instead of the body, which enables a better isolation from the bulk silicon. Due to the same principle, the bulk FinFET fabricated by *Intel* Corp. will be presented as a representative of the SOI FinFET.

III.3 Advantages of FinFETs and technological challenges

The cross-sectional schematic views of the bulk FinFET gate part and the symmetric source/drain part are shown in figure 1-13 (a) and figure 1-13 (b), respectively, and the channel part of the fin is all surrounded by the oxide layer. For the electrical characteristics, it is shown that the tri-gate structure could control the current at three sides of the channel, thus

it enables to drive a higher current due to the larger total gate width. What's more important, when the fin width is reduced to a certain value, the off-current I_{OFF} could also be decreased due to the coupling of the two side gates (gate 1 and gate 3 in figure1-13 (a)), and the SCEs are also well supressed by better controlling the channel part via coupling the two side gates, which works like a double-gate FET [48, 49]. In summary, the fin part is critical for improving the electrical characteristics of the FinFET: on one hand, the fin height should be increased as it determines the gate width W of the two side gates (gate 1 and gate 3); on the other hand, the fin width should also be reduced in order to reduce the off-current I_{OFF}.

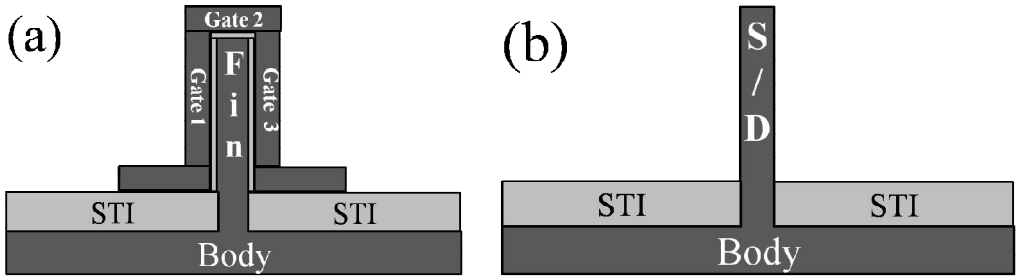


Figure 1-13: cross-sectional schematic view of the FinFET: *(a)* gate part, and *(b)* source/ drain part.

Figure 1-14 shows the electrical characteristics of *Intel*'s 22 nm tri-gate bulk FinFET in comparison with its 32 nm planar transistor. As expected, the leakage current has reduced for one decade in comparison with the planar transistor, and the steeper sub-threshold slope S is obtained, as well as the reduced threshold voltage V_{TH}.

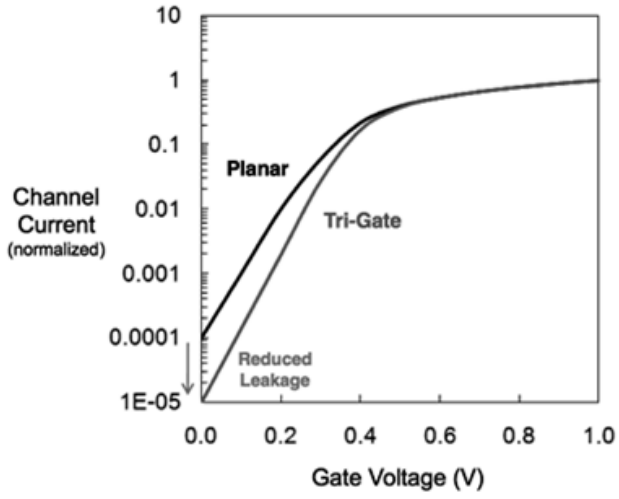


Figure 1-14: *I - V* measurement of *Intel*'s 22 nm tri-gate FinFET in comparison with its 32 nm planar transisitor [7].

Even though much better characteristics have been gained, FinFET have some technological challenges in the fabrication processing. For example, due to the reduced feature size of defining the fin with a good alignment, the high requirement of the lithography tool is still needed, such as the extreme ultraviolet (EUV) lithography. In addition, the comparatively high roughness of the fin also affects the characteristics of the FinFET, as the inversed layer is just positioned near the two rough surfaces of the fin. In fact, this highly rough surface is a technological challenge that generally exists in the 3D FEFs, and for our vertical thin film transistors (VTFTs), it also undergoes such a disadvantage, which will be presented afterwards.

III.4 Alternative three-dimensional structures

Except the FinFET, a lot of other three-dimensional (3D) FETs have also been proposed, including the Inverted-T channel FET (ITFET) [50], the Omega-gate FET [51], the Pi-gate FET [52], the four-gate FET [53], the gate-all-around (GAA) FET [54], and so on.

For the SOI FinFET, the corresponding cross-sectional gate structure is shown in figure 1-15 (a). Except the technological challenges of the FinFET listed above, another processing problem for the SOI FinFET is the undercut of the buried oxide (BOX), which affects the mechanical stability due to the thin fin.

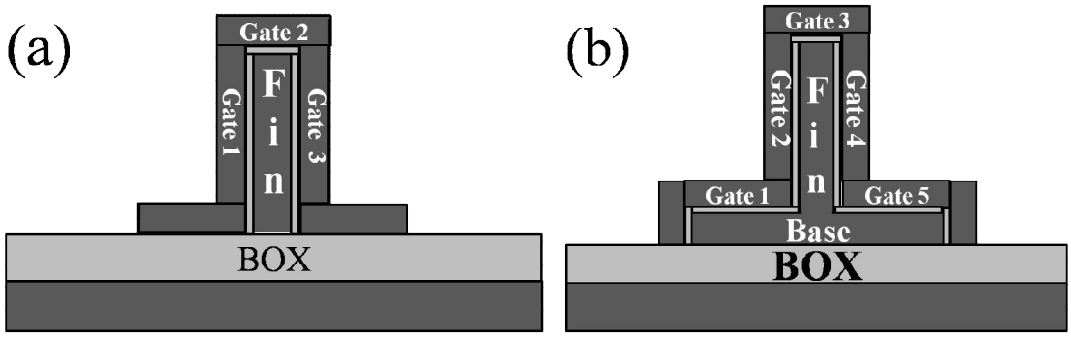


Figure 1-15: cross-section view of the gate part for *(a)* the SOI FinFET, and *(b)* the inverted-T channel FET (ITFET).

The concept of ITFET has been proposed to solve the undercuting problem. As shown in figure 1-15 (b), the ITFET can be seen as the combination of the FinFET (Fin part) and the planar FET (base part), the horizontal ultrathin base body prevents from the undercut of the

BOX. In addition, the ITFET also shows its advantage in the higher integration density for an array structure, as the space between two neighbored fins is filled with the base part, which funtions as a LTFT.

For the FinFET, the wrapped gate covers the two sidewalls and the top of the fin, but there is no control of the channel at the bottom of the fin. Thus some aternative structures have been made to improve the gate control at the bottom of the channel, including the Pi-gate FET, the omega-gate FET, and the gate-all-around (GAA) FET.

As mentioned above, FinFET always have the undercut of the burried oxide (BOX) under the fin. In fact, the undercut could also be utilized to make better gate control at the bottom of the fin by the overetching of the BOX. The Pi-gate FET is proposed by overetching the BOX, while the omega-gate FET is proposed by undercuting and overetching the BOX. The schematic structures of the Pi-gate FET and the omega-gate FET are shown in figure 1-16 (a) and figure 1-16 (b), respectively. The gate extension forms a virtual, field-induced gate electrode underneath the body that can block drain electric field from encroaching the bottom of the body. These gate structures are very effective in reducing SCEs. It is proved that for the improved gate structures, they could obtain the characteristics that are between the tri-gate transitor and the GAA FET, thus this two kinds of FETs are also called triple-plus gate structures [55].

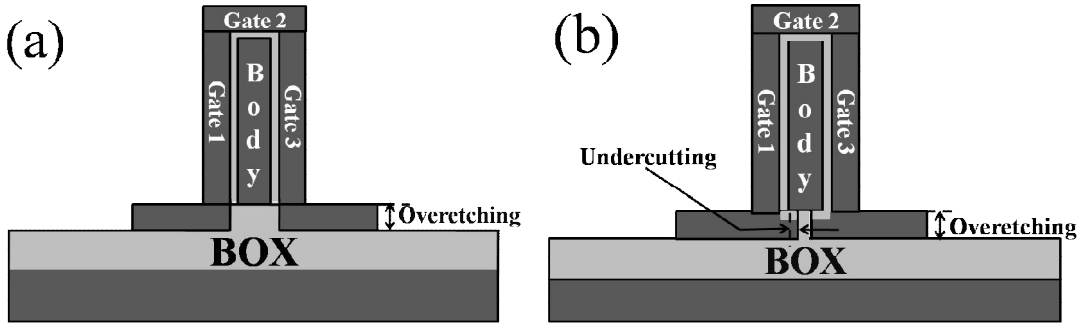


Figure 1-16: Schematic structures of *(a)* Pi-gate FET, and *(b)* Omega-gate FET.

The cross-sectional view of the gate part for the GAA FET is shown in figure 1-17. The four gates could enhance the control of the channel in comparison with the tri-gate FinFET, thus it enables to improve the electrical characteristics [54].

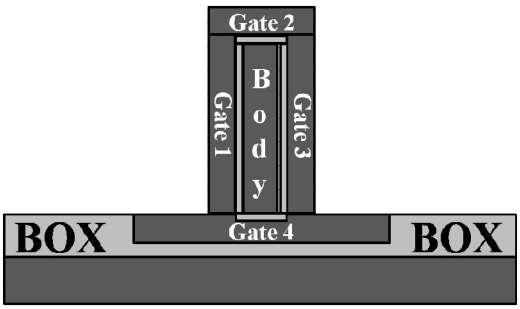


Figure 1-17: Cross-sectional view of the gate part for the gate-all-around (GAA) strucuture.

There's another special four-gate FET, whose gate structure is shown in figure 1-18 (a). It is based on a double-gate FET (with the MOSFET gate 1 and gate 2), while the two junction gates (gate 3 and gate 4) have modulated the threshold voltages of the top gate and the back gate when the double-gate MOSFET is working.

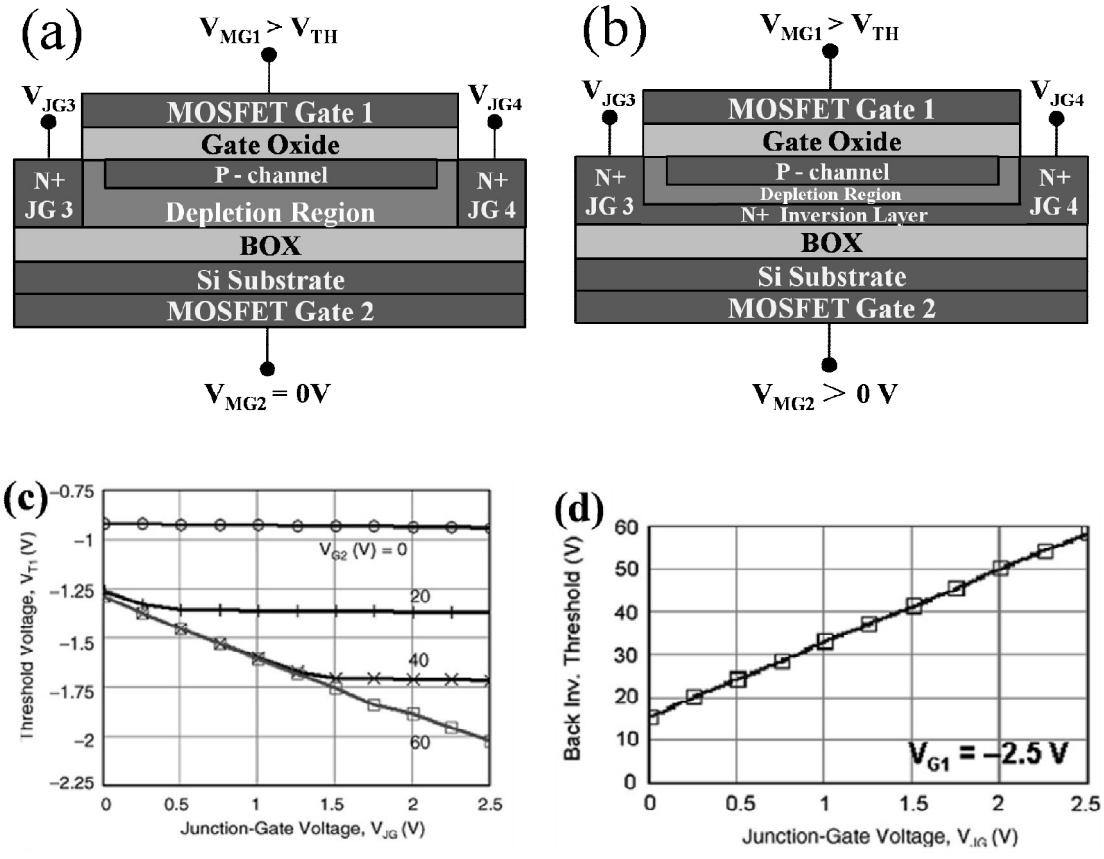


Figure 1-18: The schematic view of four-gate FET *(a)* with the top gate working, *(b)* with the double gate working, *(c)* the top gate threshold voltage V_{T1} and *(d)* the back gate threshold voltage V_{T2} modulated by different junction-gate voltages V_{JG}.

Figure 1-18 (a) and figure 1-18 (b) show different depletion regions when the back gate is

at off-state and on-state, respectively. When the back-gate is at on-state, the depletion region is narrowed when a back-gate bias V_{MG2} is applied, and the two gates are coupled. At this state, the two junction gates (gate 3 and gate 4) could modulate the potential distribution near the junction-gates, thus the threshold voltage V_{T1} of the top gate 1 and the inversed threshold voltage V_{T2} of the back gate 2 could also be modulated, which are shown in figure 1-18 (c) and figure 1-18 (d), respectively. With the increase of the junction gate voltage V_{JG}= V_{JG3}=V_{JG4}, higher absolute value of V_{T1} or V_{T2} is obtained [53].

Note that, even though the alternative 3D structures have been researched to further improve the electrical characteristics, due to the most mature process, the FinFET is still the most popular 3D FET that has been adopted for applications. The advantages of these devices have shown the interest of 3D structure, especially in the better channel controlling in comparison with the planar structure. However, for these 3D devices, the current path is still parallel to the planar surface, which indicates that the channel length is still defined by lithography technque. These 3D devices also demostrate some other drawbacks that need to be solved, especially for the lateral relief of the etched sidewall, which is a general problem for 3D devices. And for our vertical TFTs (VTFTs), it is predictable that this drawback will also be unavoidable introduced.

IV. Vertical transistors: vertical MOSFETs and vertical TFTs (VTFTs)

IV.1 Introduction of vertical MOSFETs

In many domains such as solar cells [56], ULSI devices [57] and random access memories (RAMs) [58], the prior motivation consists in obtaining a higher current density, which could be realized by reducing the channel length of the devices. As mentioned above, for the previous 3D devices, the channel length is limited by the resolution of the lithography technique. Vertical MOSFET is another type of MOSFET that source and drain are located top and bottom instead of on the same plane, with the channel (gate) vertically located between source and drain, as shown in figure 1-19. Therefore, the channel length of a vertical

MOSFET is determined by the thickness of the formed mesa, which is independent of the lithography technique, thus it enables to fabricate an ultra-short channel length.

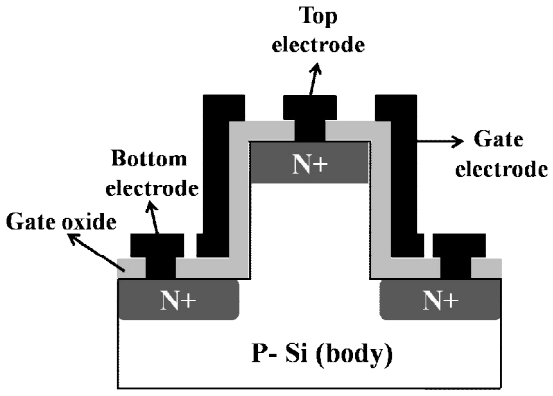


Figure 1-19: Schematic view of a vertical MOSFET.

Vertical MOSFETs have been widely researched, Lothar Risch et al. have fabricated vertical MOSFETs using Molecular Beam Epitaxy (MBE) layers [59, 60], while J. Moers et al. use a Selective Epitaxial Growth (SEG) method to reduce gate to source/drain capacitances [61, 62]. Haitao Liu et al. have also fabricated a vertical MOSFET with an ultra-thin channel layer to provide a better gate control [63, 64]. In addition, delta doping is adopted by C.Fink group in order to obtain sharp channel profiles and thus better control of electric field [65, 66], while the Steve Hall group use a dielectric pocket as the junction stopper [67, 68].

According to the 3D MOSFETs mentioned above, such as the FinFET, ITFET, GAAFET and so forth, the wrapped gates enable better control of the channel. The 3D vertical MOSFETs are also proposed, known as the gate-all-around (GAA) vertical MOSFET [69].

Figure 1-20 (a) shows the 3D schematic view of the GAA vertical FET, with a wrapped gate around the whole channel. Sometimes, the channels are made up of silicon nanowires (SiNWs), which are well known as the SiNW-based GAA vertical FET [70], shown as the figure 1-20 (b). Just as the GAA planar FET, the GAA vertical FET could ensure the control of the channel part, with a better suppression of the SCEs.

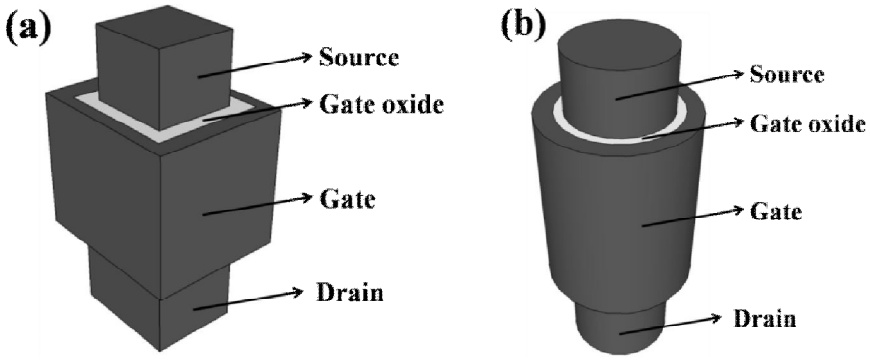


Figure 1-20: Schematic view of the 3D Gate-all-around (GAA) vertical MOSFET, *(a)* the common GAA vertical FET, and *(b)* the SiNW-based GAA vertical FET.

IV.2 Introduction of VTFTs

Corresponding to the vertical MOSFETs, the vertical TFTs (VTFTs) have also been developed using thin film technology for over three decades. The VTFT could also be seen as rotating the LTFT 90°. As shown from figure 1-21 (a), for LTFT, source and drain are on the same plane that is parallel to the substrate, and the channel length *L* is determined by the lithography technique.

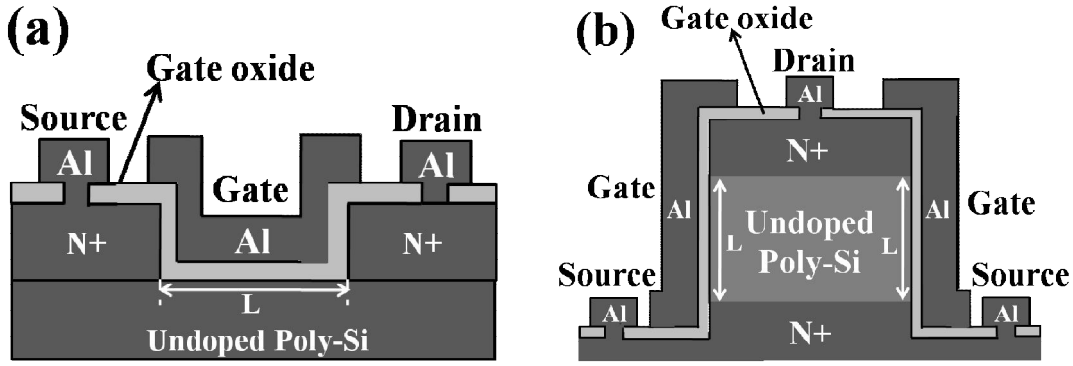


Figure 1-21: Schematic view of *(a)* the N-type LTFT, and *(b)* the N-type VTFT, the two types of TFTs are compatible with the classical CMOS technology.

As shown in figure 1-21 (b), VTFT is gained by rotating LTFT 90°, and source and drain are not on the same plane. Therefore, the channel length *L* could be precisely controlled by the deposition technique (undoped poly-Si thickness), and thus it enables an unltra-short channel length *L* beyond the resolution limitation of the lithography tools. This short channel length *L* enables a higher on-current I_{ON}, as well as a higher integration density of the devices, which are the main advantages of the VTFT [71, 72]. Note that, as it is shown in figure 1-21

(b), due to the etching of the three poly-Si layers' stacking, it is easier to fabricate a double-gate VTFT, which further doubles the on-current I_{ON}. In addition, by narrowing the width of the etched mesa, the double-gate structure is more efficient in suppressing the short channel effects (SCEs) due to the coupling of the potential distributuon of the two gates.

IV.2.1 Comparison between LTFTs and VTFTs

As mentioned above, the vertical structure enables a short channel length L that is determined by the deposition technique instead of the lithography technique, and thus VTFT helps to increase the on-current I_{ON}, in comparison with its lateral conterpart. Figure 1-22 shows a schematic cross-sectional view of the LTFT. The device dimension on the glass substrate is evaluted by the design rule λ. As it is shown in figure 1-22, for a LTFT with the minimin device dimension of $30\lambda^2$, the device length and width are 15λ and 2λ, respectively, while channel width/length ratio $W/L = 2\lambda/2\lambda = 1$.

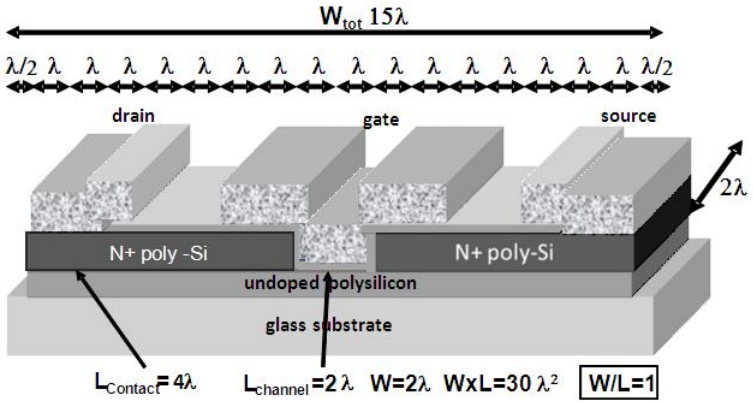


Figure 1-22: Schematic cross-sectional view of a LTFT, the device dimension is $15\lambda \times 2\lambda$, while channel width and channel length ratio $W/L = 2\lambda/2\lambda = 1$.

In contrast, for a VTFT with the same device dimension, the channel width and channel length ratio W/L could be much higher. Figure 1-23 shows the cross-sectional view and the top view of a VTFT, whose device length and width are 3λ and 10λ, respectively, which leads to a same device dimension of $30\lambda^2$. On one hand, due to the special 3D structure, the device length could be reduced to 3λ. As a result, the channel width W could be $2\times6\lambda = 12\lambda$, considering that there are two channels on the two sidewalls. On the other hand, due to the definition of the channel length L by the deposition technique, the channel length L could be shrinked to $\lambda/3$. As a result, the channel width length ratio W/L could be $12\lambda/(\lambda/3) = 36$. In

theory, as the drive current is proportional to *W/L*, VTFT enables to increase the drive current about 40 times [73]. This increased drive current is the main advantage of VTFT in comparison with LTFT, which is beneficial for large-current applications.

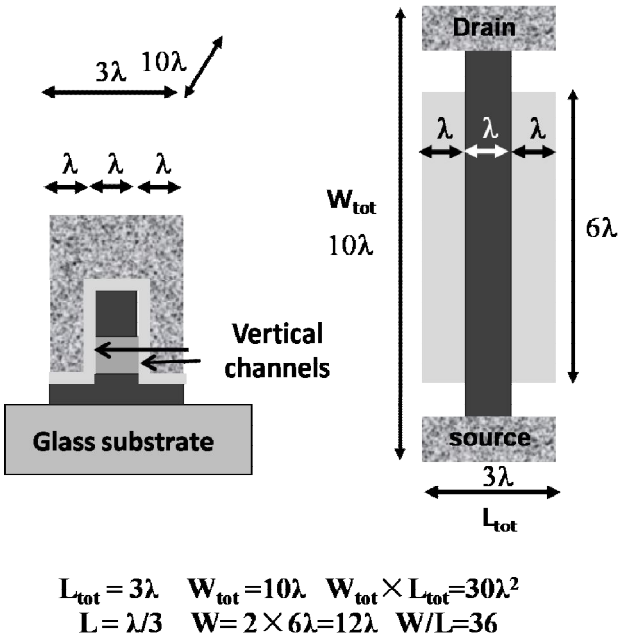


Figure 1-23: Schematic cross-sectional and top view of a VTFT, the device dimension is $3\lambda \times 10\lambda$, while channel width and channel length ratio $W/L = 12\lambda/(\lambda/3) = 36$.

IV.2.2 State of the art for VTFTs

VTFT has been researched over two decades. James D. Flummer group has fabricated a VTFT using the anisotropic As^+ implanted source/drain, however, the dopant diffuses after a long-time annealing [74]. Tan Fulei et al. have fabricated VTFTs with a self-aligned offset, by adopting the inverted structure. However, the adopted high-temperature (T = 850°C) anneling method is not compatible with the glass substrates, while the Ni-silicide induced lateral crystallization technology (NSILC) involves more complex processes [75]. Tan Fulei et al. have also fabricated a novel VTFT using excimer-laser anneaing (ELA) method to form the active layer, the high-cost method is also a challenge for large-size glass substrate applications [76].

In our research work, another VTFT structure is proposed, with more gates arranged in parallel, as shown in figure 1-24 (a). On one hand, this multi-gate structure enables to further increase the on-current I_{ON}, as I_{ON} is proportional to the channel width/length ratio *W/L*.

Taking the VTFT in figure 1-22 (a) as an example, there are two teeth for this VTFT, thus there are four gates on the four sidewalls (four parallel channels), then the channel width *W* is four times of each channel width on the sidewall. In fact, this special 3D structure could enable much more teeth, as long as the tooth width is narrow enough, and this special multi-gate structure is also named "comb-shaped VTFT". On the other hand, in the fabrication process, for all the thin films deposited in our laboratory, especially for the poly-Si layers deposited by LPCVD technique, the maximum temperature is 600°C, which is compatible with the glass substrates (for example, *Corning* 1737 glass substrates). The source and drain layers are *in situ* doped, and no additional diffusion or implantation step is required. Therefore, it facilitates the fabrication process, and the dopant diffusion problem is also avoided. In addition, this multi-gate structure also helps to increase the packing density, which is another advantage of the vertical structure.

Figure 1-24 (b) shows the side view of the multi-gate VTFT, there is a partial etching step at the source side, so that the top and bottom heavily-doped layers could be accessed at the same time. In addition, the large overlap that passes through the undoped poly-Si is also observed.

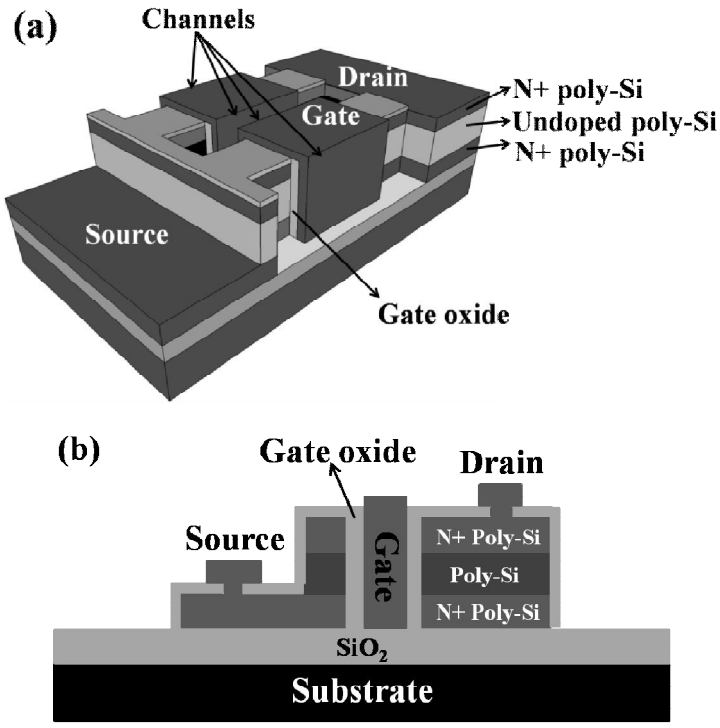


Figure 1-24: *(a)* 3D view, and *(b)* side view of the multi-gate VTFT.

V. Conclusion

The scale-down tendency of the microelectronic devices follows Moore's law, which proposes higher requirement in the lithography and etching techniques. In addition, the serious short channel effects (SCEs) also degrades the electrical property of the devices. Therefore, new device architecture is necessary to pursue Moore's law.

The gate engineering of the FETs, especially for the three-dimensional (3D) FETs, has shown its remarkable superiority in channel controlling. The 3D FinFET structure has been adopted in *Intel*'s 22 nm node CPU technology, which shows a reduced off-current I_{OFF} as well as a decreased threshold voltage V_{TH}. Other alternative structures have also been proposed, including inverted T-shaped FET (ITFET), Pi-gate FET, Omega-gate FET, Gate-all-around (GAA) FET, four-gate FET, and so on. The advantages of these devices show the interest of 3D structure, however, they also give evidence of some drawbacks that need to be solved.

Vertical transistor (Vertical MOSFET or VTFT) is obtained by rotating the planar transistor (planar MOSFET or LTFT) 90°, and it could provide several advantages:

1) Channel length is defined by the deposition technique instead of the lithography technique, thus it reduces the technological dependence on lithography;
2) Ultra-short channel FET could be fabricated with a large channel width, which helps to increase the drive current;
3) Higher packing density could be provided in comparison with its lateral counterpart.

A lot of vertical MOSFETs and vertical TFTs (VTFTs) have been researched for more than three decades. In our laboratory, a new multi-gate VTFT is proposed, which further increases the drive current. A low-temperature fabrication process is employed, with the maximum temperature of 600°C, which is compatible with glass substrates.

In chapter 2, this multi-gate VTFT will be introduced in detail. Initially, different techniques in the fabrication process will be given, especially the mature LPCVD and SPC techniques for poly-Si layers deposition will be presented in detail. After that, the fabrication

process of the VTFT will be presented step by step, and the first electrical characteristics will be demonstrated. Afterwards, some technological modifications on the structure will be proposed, the obtained electrical characteristics will be further analyzed and discussed in detail.

Chapter 2 Related techniques, process flows, and electrical characteristics of the classical VTFTs

In the previous chapter, the basic structure and working principle of the LTFT have been presented, and the VTFT has also been proposed corresponding to the vertical MOSFET, by using thin film technology. In this chapter, we will detailedly describe the fabrication process of the classical VTFT structure, which is fabricated by rotating LTFT 90°. The fabrication process is based on polycrystalline silicon (poly-Si) thin film layers deposited by the low pressure chemical vapor deposition (LPCVD) technique, and the low-temperature ($T \leq 600$°C) process enables to be compatible with glass substrates. This chapter initially describes the related materials and techniques adopted in the VTFT fabrication process, which have also been involved in the previous LTFT fabrication process. First, due to their importance in the fabrication of our classical VTFT, silicon layers deposited by LPCVD and annealed by solid phase crystallization (SPC) technique are especially described in detail. Then, other related materials and techniques are also introduced. Afterwards, the fabrication process flow of the classical VTFT with three poly-Si layers' stacking structure is listed step by step. The key technological challenge for the classical VTFT structure is explained, and devices are electrically characterized and analyzed to highlight the drawbacks of the VTFT structure, for example, the parasitic channel and the large overlapping area. At the end of this chapter, some improvements to solve these problems are also presented.

I. Related materials and techniques in thin film technology

In our laboratory, different thin film materials and deposition methods have been well developed and adopted on different substrates. The mature thin film deposition technologies of semiconductor, insulator, and metallic layers have been involved in the devices and circuits fabrication. The laboratory has great potential and ability in the deposition of thin films by using different techniques, such as LPCVD, plasma-enhanced chemical vapor deposition (PECVD), RF sputtering, thermal evaporation, and so on. Our laboratory also has the know-how in the technological fabrication of devices and circuits in the clean room, as well as the electrical characterization of the devices and circuits.

I.1 Introduction of different silicon structures: mono-Si, a-Si and poly-Si

Silicon is the basic and fundamental material of the semiconductor industry, because of its interesting electrical properties, as well as its abundance on the earth. Silicon could be divided into three categories according to their different crystal structures: the monocrystalline silicon (mono-Si), amorphous silicon (a-Si), and the intermediate state, which is called polycrystalline silicon (poly-Si).

In mono-Si structure, the Si atoms regularly arrange in a long range order. For an ideal silicon crystal, the atoms arrange as the diamond structure, which follows the face-centered cubic Bravais lattice. The schematic tetrahedral arrangement of the silicon atoms in the diamond structure is shown in figure 2-1. For each bond of adjacent atoms, the interatomic distance is 2.35 Å, and the separation angle is 109°28′ between two bonds.

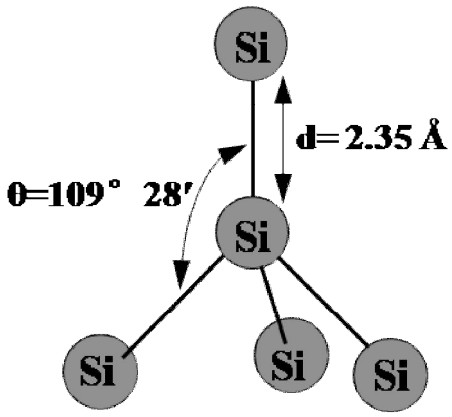


Figure 2-1: Schematic tetrahedral arrangement of the silicon atoms.

In a crystal, this kind of Si-Si bond induces electronic states, leading to the formation of the energy bands. The atomic distance between two atoms determines the width between the energy bands. The last energy level completely filled with electrons is called valence band (VB), and the next allowed energy level is called conduction band (CB). For Si, the energy gap E_g between the two energy levels is 1.12 eV. This low value enables electrons to easily transit from VB to CB. Among the three types of Si forms, mono-Si is an ideal semiconductor material that enables to get the best characteristics. However, the production of mono-Si needs the highest economic cost, which requires an extraction step by melting and

re-solidifying silicon.

The a-Si is the non-crystalline form of silicon. However, it maintains some properties of the crystalline silicon (mono-Si). In fact, the interatomic distance of a-Si keeps at 2.35 Å, while normally every atom is connected with four adjacent atoms. However, for a-Si, the long range order of mono-Si is not present, and the atoms form a continuous random network. Sometimes the fourfold coordinated structure is not strictly followed, and some atoms present dangling bonds. These dangling bonds act as defects in the continuous random network, which act as localized states in the band gap. These localized states trap the carriers and thus modify the transport of the carriers, and thus it is expected that the electrical properties of a-Si seriously degrade in comparison with mono-Si. However, a-Si is much easier to be produced via a low-cost way. In our laboratory, a-Si can be deposited by LPCVD technique or by PECVD method.

Poly-Si is a crystalline structure of silicon that is between mono-Si and a-Si. For poly-Si, the crystal lattices of the whole material is disordered, thus it contains a lot of small silicon crystals (crystallites or grains), with crystalline defects (grain boundaries) between two adjacent crystals. From this point of view, poly-Si can be considered as a combination of mono-Si (grains) and a-Si (grain boundaries), and its properties are determined by the two parts listed below:

- The grain is characterized by its size and its crystalline quality. As poly-Si is a deposited structure, whose grain size cannot be comparable to the one of mono-Si, defects are inevitablely introduced. These defects could be dislocations or macles in the silicon crystals. For the dislocations, they result in the formation of dangling bonds. For the macles, if they end at the surfaces of the grains, they will just divide the grains into more, smaller crystallites. In contrast, if they end in the grains, they would also result in dangling bonds. The defect density determines the grain quality.
- The grain boundary is characterized by its dimension (thickness) as well as its defect density.

The energy states distribution of poly-Si is shown below in figure 2-2. The band tail due to the disordered arrangement of the crystals, and the deep-level traps caused by dangling bonds, are shown in this figure. These defects degrade the electrical properties of poly-Si in comparison with mono-Si.

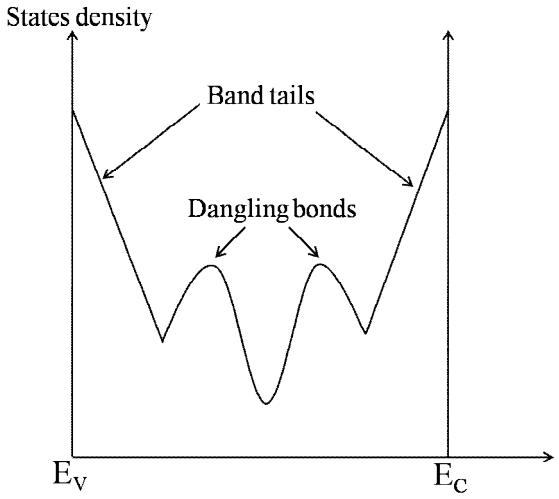


Figure 2-2: Schematic model of poly-Si energy states distribution.

Among the three silicon forms, poly-Si is an essential and fundamental material in the fabrication of the TFTs. On one hand, compared with mono-Si, poly-Si is much easier to be compatible with all kinds of substrates, such as glass substrates, plastic substrates and so on; on the other hand, in contrast with a-Si, the better crystalline structure of poly-Si enables to improve the electrical characteristics, especially the field effect mobility. Therefore, poly-Si is in fact more beneficial to be used in the display fields, such as the AMLCD (Active Matrix Liquid Crystal Display) and AMOLED (Active Matrix Organic Light-Emitting Diode). In summary, being the basic material of TFTs, poly-Si compromises the advantages of mono-Si and a-Si, thus it dominates the semiconductor thin film technology.

For poly-Si thin film deposition, the widely-used techniques also include LPCVD and PECVD methods. For PECVD, the plasma of the reacting gas is generated by RF frequency between two electrodes. The energetic plasma dissociates the precursor molecules, and thus the dissociated molecules (such as silicon) are directly deposited on the sample surface, or react with each other to generate new thin film material (such as silicon nitride Si_3N_4) on the

sample. PECVD technique allows the deposition of materials at a very low temperature. For example, silicon could be deposited under 300°C by PECVD using silane (SiH_4), disilane (Si_2H_6), or dichlorosilane (H_2SiCl_2) as the precursor gases. In fact, in our laboratory, LTFTs have been fabricated based on the low-temperature PECVD process, including the deposition of silicon by SiH_4 (diluted in Argon and hydrogen gases), as well as the deposition of Si_3N_4 by SiH_4 and Ammonia (NH_3) precursor gases (diluted in nitrogen adjunction) [77]. Due to the low-temperature technique, PECVD leads to deposit poly-Si with a smaller grain size, so-called "microcrystalline silicon", which degrades the electrical property, especially the drive current and field effect mobility. However, it enables the process to be compatible with flexible substrates, such as plastic substrates, which reveals its potential applications in soft-substrate display field [78, 79].

LPCVD is a widely used technique in microelectronic industry for poly-Si deposition. For LPCVD technique, there are two ways to deposit poly-Si layers. One way is called "as-deposited poly-Si", which directly deposits poly-Si without a crystallization step. The deposition temperature is usually high to directly crystallize the deposited silicon, while the pressure is low. A typical as-deposited condition could be at the temperature of more than 620°C with the reduced pressure between 120 - 350 mTorr, while the SiH_4 gas flow rate is 50 - 200 sccm, and the grain size is around 40 nm [80].

The other way is the deposition of a-Si by LPCVD followed by a crystallization step. The crystallization step could be variable, and in our laboratory, the combination of LPCVD at 550°C and conventional thermal annealing at 600°C is the commonly used method that enables to obtain poly-Si with a large grain size [81]. The conventional thermal annealing is a kind of solid phase crystallization (SPC) technique, and it has been widely used for the fabrication of LTFTs, which have exhibited excellent electrical characteristics, especially for the high field effect mobility [82]. Therefore, for our VTFTs, the poly-Si thin film layers are also obtained by the combination of LPCVD and SPC techniques.

I.2 Poly-Si deposited by LPCVD technique

I.2.1 LPCVD principle

In our laboratory, the LPCVD technique has been studied for about two decades [83, 84], and it enables the thickness uniformity of the deposited poly-Si layers (the thickness difference is only about 5% for a large deposition area). The schematic view of the horizontal LPCVD system is shown in figure 2-3:

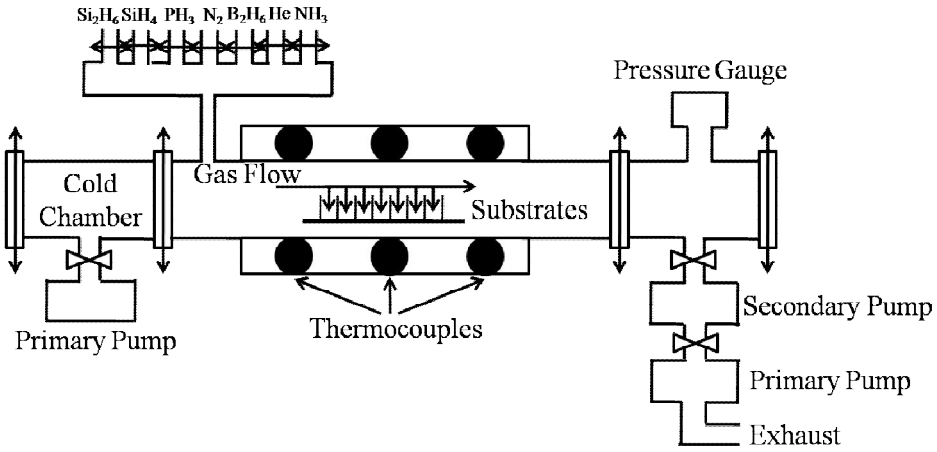


Figure 2-3: Schematic view of a typical horizontal LPCVD system.

In this horizontal LPCVD system, the pure precursor gas is injected into the high-vacuum reactor. Note that, the reactor is always kept under vacuum, even when loading and taking out the samples. The precursor gas (silane SiH_4, disilane Si_2H_6 or dichlorosilane H_2SiCl_2) pyrolytically dissociates into Si atoms due to the high temperature in the reactor, and the decomposed silicon atoms deposit on the sample surface to form silicon thin films. In fact, the dissociation of the precursor gas and the deposition on the sample surface take place at the same time. There are two kinds of reactions during this process, one of which is called "homogeneous reaction", which takes place between the gas atoms, while the other reaction is called "heterogeneous reaction", which takes place between the gas atoms and the sample surface. In our laboratory, SiH_4 is normally adopted as the precursor gas, and the main simplified reaction equation during the LPCVD process is:

$$SiH_4(g) \rightarrow Si(s) + 2H_2(g) \qquad (eq.2-1)$$

In fact, the chain reactions also take place during the process, which could be shown below as the equation 2-2 and the equation 2-3:

$$SiH_4 \leftrightarrow SiH_2 + H_2 \qquad (eq.2-2)$$

$$SiH_2 + Si_nH_{2n+2} \leftrightarrow Si_{n+1}H_{2n+4} \qquad (eq.2-3)$$

In LPCVD process, the most important parameters are deposition temperature, partial pressure of the precursor gas, and the precursor gas flow, which greatly affect the morphology and the grain size of the deposited silicon. Sufficient precursor gas flow is required in order to continuously fill in the reactor and reach the surfaces of all the samples. The more important parameters during LPCVD process are the deposition temperature and the partial pressure of SiH_4, the effects of the two parameters on the silicon state are shown in figure 2-4.

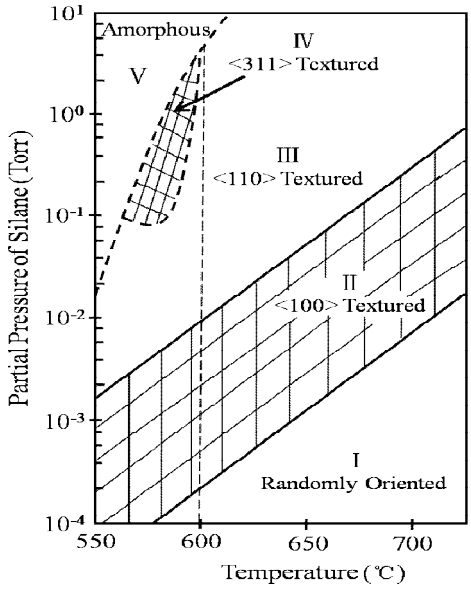


Figure 2-4: Silicon structure deposited by LPCVD under different deposition temperatures and partial pressures of SiH_4 precursor gas [85]. At 550°C and 90 Pa (0.675 Torr), the silicon is in amorphous state (V zone), while at 600°C and 90 Pa (0.675 Torr), the silicon is poly-Si (III <110> Textured zone).

It shows that only at the temperature range between 550°C and 600°C with a higher pressure that is higher than 10^{-2} Torr, the deposited silicon is in the amorphous state. Otherwise, with a higher deposition temperature, or/and with a reduced partial pressure, the

deposited silicon is partially or totally crystallized, which corresponds to the state of as-deposited poly-Si.

As mentioned above, for the LPCVD technique, the adopted deposition temperature is 550°C, and the deposition pressure is set to be 90 Pa (0.675 Torr) using SiH_4 as the precursor gas. The chosen deposition conditions are based on the fact that, Si deposited at 550°C (and crystallized at 600°C) enables to get the Raman spectrum that is closest to mono-Si, and the hall mobility is proved to have the highest value at this temperature [86], thus it enables to improve the electrical characteristics of the fabricated TFTs. At such a deposition condition, the corresponding deposition rates are about 5 nm/min, 3 nm/min, and 4 nm/min for undoped silicon, N-type heavily-doped silicon, and P-type heavily-doped silicon, respectively. However, at this condition, silicon is in the amorphous state, and then an additional crystallization step should be carried out to form poly-Si.

In addition, for our VTFTs fabrication, Si_2H_6 precursor gas is also adopted to form the undoped active layer in one attempt. The corresponding dissociation equation of Si_2H_6 is shown as below:

$$Si_2H_6(g) \rightarrow 2Si(s) + 3H_2(g) \qquad (eq.2-4)$$

For poly-Si deposition using Si_2H_6 precursor gas, the deposition temperature is 475°C, while the pressure is 50 Pa, and the gas flow is 25 sccm. At these conditions, the formed silicon is at the amorphous state, and a crystallization step is also needed. For poly-Si deposited on the planar surface using Si_2H_6 as the precursor gas, it has been proved to have a larger grain size than the one using SiH_4 as the precursor gas [87].

I.2.2 *In situ* doping for LPCVD

In situ doping is an advantage of LPCVD technique. The *in situ* doping is realized by injecting the dopant gas of phosphine (PH_3, for N-type doping) or diborane (B_2H_6, for P-type doping) with the precursor gas (SiH_4 as an example) during the LPCVD process, thus additional steps, such as diffusion or ion implantation, are not needed. The PH_3 and B_2H_6

gases decompose following the simplified reaction equations:

$$PH_3(g) \rightarrow P(s) + \frac{3}{2} H_2(g) \qquad (eq.2-5)$$

$$B_2H_6(g) \rightarrow 2B(s) + 3H_2(g) \qquad (eq.2-6)$$

The deposition of a doped layer is performed by adopting the same conditions as the deposition of an undoped layer, for example, the same deposition temperature of 550°C as well as the same total pressure of 90 Pa when using SiH_4 as the precursor gas. The different doping levels could be realized by adjusting the gas flows ratio between PH_3 (B_2H_6) and SiH_4. The PH_3 dopant level Γ_P (or the B_2H_6 dopant level Γ_B) is defined by the following equation:

$$\Gamma_{P(B)} = \frac{\phi_{PH3}(\phi_{B2H6})}{\phi_{SiH4}} \quad (\phi : gas\ \ flow) \qquad (eq.2-7)$$

For N-type doping, the doping concentration can vary from $2 \cdot 10^{16}$ cm^{-3} to 10^{20} cm^{-3}, while the P-type doping concentration range is from $2 \cdot 10^{16}$ cm^{-3} to $5 \cdot 10^{19}$ cm^{-3}.

I.2.3 Crystallization

As mentioned above, for the silicon deposited at 550°C and 90 Pa using the SiH_4 precursor gas, or at 475°C and 50 Pa using the Si_2H_6 precursor gas, the deposited silicon is mainly at the amorphous state. Thus a crystallization process is necessary in order to crystallize a-Si into poly-Si.

The most commonly used crystallization methods include laser crystallization, rapid thermal annealing (RTA), metal-induced (lateral) crystallization (MILC or MIC), and conventional thermal annealing. For laser crystallization, silicon melts under high laser energy, thus it is called “liquid phase crystallization (LPC)”. The latter three crystallizations take place when silicon is in the solid phase, thus they are called “solid phase crystallization” (SPC).

I.2.3.1 Common crystallization methods

Laser crystallization uses laser irradiation as the intense energy source. Due to the excitement of the laser, a limited surface of a-Si is heated, thus it could be adopted as a kind of selective crystallization method by precisely controlling the crystallization time. The adopted laser could be operated in the continuous wave mode, or in the pulsed mode. The laser source could be generated by He_2, Xe_2, ArF, KrF, and XeCl, which generate ultraviolet wavelength to excite a-Si surface. TFTs have been proved to have very large field effect mobilities by adopting the laser crystallization method [88, 89], which is due to the large grain size (about 1μm) of the formed poly-Si [90]. However, homogeneous crystallization using laser is a technological challenge. For the continuous laser, the sweep of the laser is necessary to crystallize the total surfaces of the sample, while for the pulsed laser, it is very difficult to obtain homogeneous crystallization. In addition, the expensive cost also limits its applications in mass production.

RTA is an annealing method that uses a halogen lamp to generate the high temperature between 700°C and 800°C, and a-Si could be crystallized in a very short time. However, this method requires that the halogen lamp emission spectrum is consistent with the absorption spectrum of the silicon. At such a high temperature, the glass substrate may undergo deformation problem, which also limits the application of RTA [91]. In addition, the silicon layer also contains a lot of crystalline defects. The obtained mobility from this crystallization method is between 25 cm^2/V.s and 28 cm^2/V.s [92].

MILC and MIC are special crystallization ways that take place involving metal catalysts. When metal-silicon is at the temperature above the eutectic point, the silicon could be crystallized by the self-organization of metal-silicon droplet. Usually the eutectic points are much lower than the melting points of silicon and the metals separately, thus they enable a low-temperature crystallization of silicon. Taking Ni as an example, a thin layer of Ni (2 nm – 5 nm) is deposited on the a-Si layer, then the sample is annealed at 500°C for several hours, and the nickel atoms diffuse to crystallize a-Si [93, 94]. These methods provide large grain

size with a reduced annealing temperature, however, due to the participation of metal catalysts, metallic impurities are unavoidable, which could greatly degrade the electrical properties of the obtained poly-Si [95].

I.2.3.2 Conventional thermal annealing

In contrast, conventional thermal annealing avoids the different challenges and shortcomings of the crystallization methods listed above, thus it is the most common way for crystallization, and it is widely used in the industrial mass production. The samples are put in the reactor with the temperature range from 550°C to 650°C for an annealing period from several minutes to several hours. Usually, the samples could be put in the same reactor as the LPCVD. At such an intermediate temperature, the glass substrates usually don't deform. This crystallization doesn't involve any metal catalyst, thus the metallic impurities are also avoided. In addition, due to the uniform annealing for a large area, the homogeneous crystallization could be achieved.

In our laboratory, it has been proved that thermal annealing at 570°C enables to have the best crystalline quality of poly-Si layer. However, due to the long crystallization time at 570°C, the standard crystallization temperature is set at 600°C, while the reactor is under vacuum [81]. The crystallization time depends on the thickness of the deposited film as well as the doping level of the film. For a high thickness or a high doping level, a long crystallization time is required. Usually, the adopted crystallization time is more than 12 hours. Note that, the LTFT based on the combination of LPCVD at 550°C and SPC (conventional thermal annealing) at 600°C using SiH_4 precursor gas, has been proved to have a high field effect mobility of more than 100 $cm^2/V{\cdot}s$ for the poly-Si LTFT [24]. Therefore, for our VTFTs, they will also be fabricated based on this mature technique.

I.3 Silicon nitride (Si_3N_4) films deposited by LPCVD technique

By adopting the same LPCVD technique, silicon nitride (Si_3N_4) layers could also be deposited. Si_3N_4 is well known for its excellent mechanical property and diffusion barrier

property for water and ions, such as Na+, K+, H+, and it is also used as the gate insulator because of its high dielectric constant. However, in our laboratory, due to the temperature limitation of low-temperature process for VTFTs, the crystalline quality of Si_3N_4 deposited at 600°C degrades (whose ideal deposition temperature is between 650°C and 850°C [96]), thus it is not suitable for the gate dielectric material in the low-temperature process. Nevertheless, Si_3N_4 deposited at 600°C could also be used as an insulating layer, and what's more important, for reactive ion etching (RIE) using SF_6 etchant, the low etching selectivity between poly-Si and Si_3N_4 enables to achieve the continuous sidewall for the new VTFTs fabrication, and thus it is beneficial for VTFT fabrication, which could be shown later.

The deposition of Si_3N_4 by LPCVD uses SiH_4 and Ammonia (NH_3) as the precursor gases. The reaction follows the chemical equation 2-8:

$$3SiH_4(g) + 4NH_3(g) \rightarrow Si_3N_4(s) + 12H_2(g) \qquad (eq.2-8)$$

The deposition conditions for Si_3N_4 in the low-temperature process are listed below:

- Deposition temperature: 600°C;
- Total pressure: 400 μbar (300 mTorr);
- Gas flow: 50 sccm SiH_4 and 50 sccm NH_3

Under these deposition conditions, the deposition rate of Si_3N_4 is about 15 nm/h, this low deposition rate is also a disadvantage for the process.

I.4 Atmospheric Pressure Chemical Vapor Deposition (APCVD) technique

For our VTFTs, SiO_2 could be used as the buffer layer as well as the gate dielectric. APCVD is a widely-used low-temperature technique for SiO_2 deposition. Taking SiH_4 and O_2 precursor gases as an example, the main reaction equation during APCVD process is:

$$SiH_4(g) + O_2(g) \rightarrow SiO_2(s) + 2H_2(g) \qquad (eq.2-9)$$

Diluted silane (SiH_4) and oxygen (O_2) are introduced into the reactor with N_2 as the gas

carrier, and thus SiO_2 is deposited by APCVD with a $SiH_4/O_2/N_2$ gas mixture. The standard deposition temperature is 420°C. At this deposition condition, SiO_2 could show its higher insulating quality in comparison with Si_3N_4 deposited by LPCVD at 600°C, especially after a densification step at 600°C for more than 12 hours. In addition, SiO_2 deposited by APCVD enables to get a much higher deposition rate of about 29 nm/min. Using APCVD technique, conformal deposition of SiO_2 layers can be obtained, which is critical for VTFT fabrication. As illustrated in figure 2-5, the SiO_2 thickness on the planar surface is almost the same as on the sidewall.

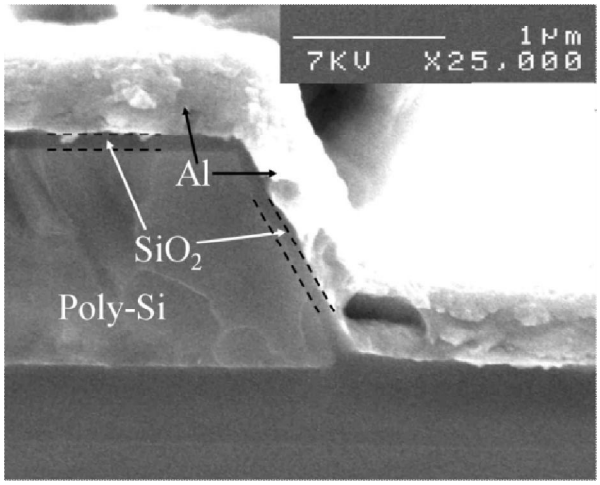


Figure 2-5: The conformal deposition of SiO_2 is shown, whereas the deposited aluminum shows a higher thickness on the planar surface than on the vertical sidewall.

I.5 Joule effect evaporation of aluminum (Al)

In the VTFT fabrication processes, aluminum (Al) is used to define source, drain, and gate electrodes. Joule effect evaporation is a common technique for Al deposition as well as other low melting-point metals, such as Au. The schematic view of the Joule effect evaporation system is shown below in figure 2-6. Al source is put on a tungsten boat (whose melting point is 3422°C), it is evaporated under high current-generated Joule heat and then deposited on the sample surface. Al source is made up of 99% Al and 1% silicon, the 1% silicon is necessary as it enables to make a better Al/silicon contact after the forming gas treatment, which helps to reduce the contact resistance. The deposition thickness of Al is measured by detecting the frequency variation of the crystal oscillator, as shown in figure 2-6.

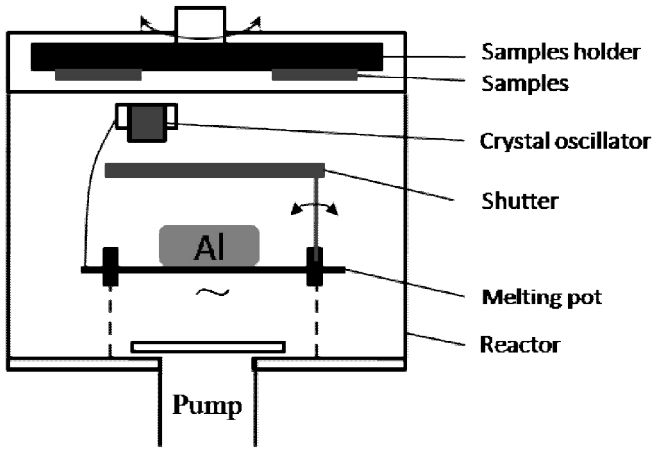


Figure 2-6: Schematic view of Joule effect evaporation for Al deposition.

In fact, the Al deposition shows a little anisotropy, the thickness on the planar surface is a little higher than on the sidewall, which is also shown in figure 2-5. Nevertheless, the thickness difference is not very serious, and when depositing a 400 nm Al layer on the planar surface, the thickness on the sidewall is also sufficient for the applied gate bias.

I.6 Reactive ion etching (RIE) for patterning

Reactive ion etching (RIE) is one kind of widely-used plasma etching method, which combines physical and chemical effects and thus enables the rapid and anisotropic etching. The schematic diagram of the RIE reactor is shown in figure 2-7. The widely-used etchant gases are Sulfur hexafluoride (SF_6) and Tetrafluoromethane (CF_4), and other gases could also be added, such as oxygen (O_2), Argon (Ar), and so on, in order to increase the etching rate or protect the etching surface [97, 98]. Taking SF_6 as an example, RIE begins with the generation of plasma, the SF_6 gas is ionized under RF electromagnetic field, and then the great amounts of generated F free radicals are attracted to the positively charged platter. The physical bombardment anisotropically hits the sample surface and creates a rough surface that accelerates the chemical erosion, while the chemical erosion removes the residue generated by the physical bombardment as well as encroaches the sample surface, which also helps to increase the bombardment rate in reverse. The two actions work together to ensure the anisotropic etching property as well as the higher etching speed.

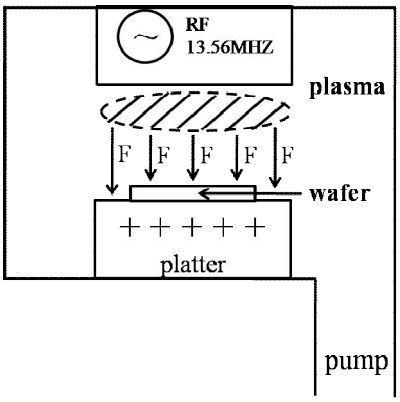


Figure 2-7: Schematic diagram of the RIE reactor, the plasma is generated by RF generator under a low pressure.

The related parameters for the RIE process are: 1) RF power *W*, which determines the intensity of the F free radicals, and thus affects the ion bombardment energy; 2) gas flow *Γ*, which determines the average stay time of the source gas in the reactor; 3) pressure *P*, which affects the particle collision and thus influences the anisotropy of the RIE. The effect of the RIE parameters on the sidewall profile would be discussed after the introduction of the process flow for the classical VTFT.

II. Classical VTFT structure, process and technological challenges in the process

As mentioned in chapter 1, the classical VTFT has been proposed by rotating the LTFT 90°. For the initial trial, three shapes of classical VTFTs have been fabricated, i.e., the U-shaped VTFT [99], H-shaped VTFT [100], and comb-shaped VTFT [101], as shown in the schematic views of figure 2-8 (a), figure 2-8 (b), and figure 2-8 (c), respectively. Except for the short channel length *L* of the VTFT, the special comb shape enables to further increase the drive current, as it could provide more channels arranged in parallel. Therefore, the comb-shaped VTFT is chosen as the most representative VTFT among the three types of VTFTs. The process flow and electrical characteristics for the comb-shaped VTFT will be presented in detail, on behalf of all the three kinds of VTFTs.

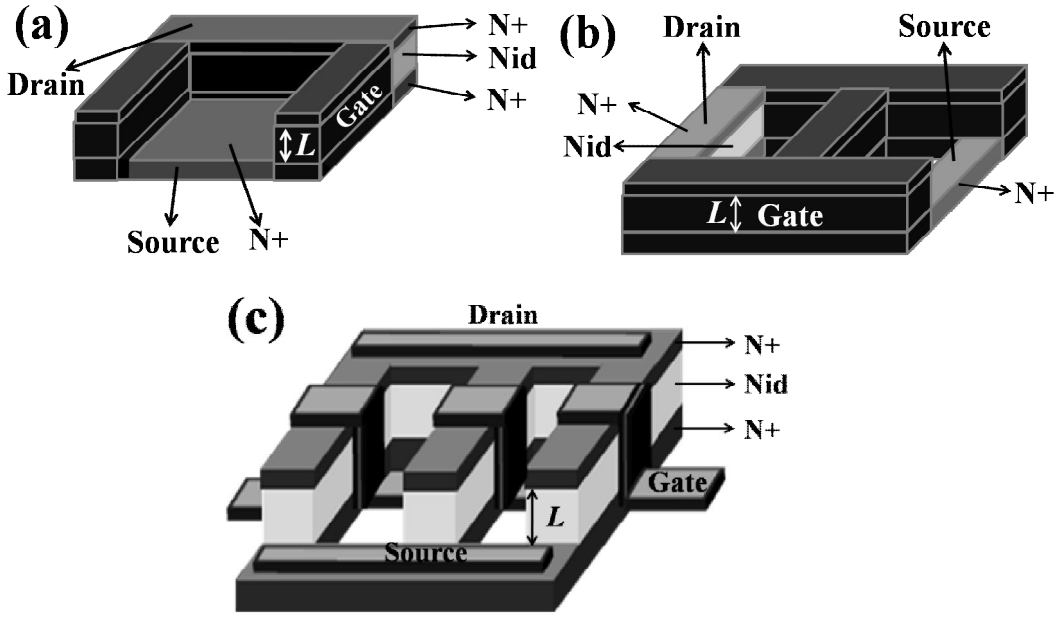


Figure 2-8: Schematic views of *(a)* the U-shaped VTFT, *(b)* the H-shaped VTFT, and *(c)* the comb-shaped VTFT.

II.1 Detailed process flow for the classical VTFT structure

The three-dimensional (3D) view of the classical comb-shaped (multi-tooth) VTFT and its basic tooth structure are shown in the following figure 2-9 (a) and figure 2-9 (b), respectively. The VTFT is made of a source at the bottom, a drain on the top and an active layer in-between. The source and drain could be reversed, and usually we analyze the device characteristics by using a drain-on-top (DOT) structure. As we can see from the 3D view, it is necessary to form the basic teeth structure, and then extend the bottom heavily-doped layer in order to access to source and drain at the same time, thus two masks are needed. In addition, the other two masks are also required, one is for the contact openings after the gate oxide deposition, and the other one is used for the contacts definition after Al deposition. In summary, a four-mask process is needed to fabricate the 3D comb-shaped classical VTFT. The detailed process flow is listed below. Due to the higher doping level and better doping uniformity, N-type VTFTs are usually fabricated. The cross-sectional view of a tooth of figure 2-9 (b) shows the three poly-Si layers stacking.

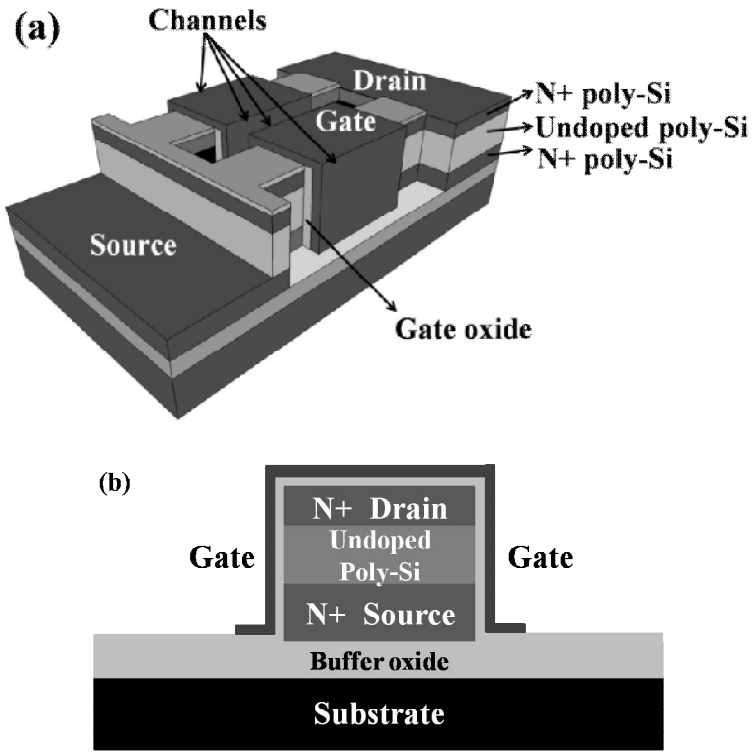


Figure 2-9: The classical VTFT structure: *(a)* the 3D view of a two-tooth VTFT, and *(b)* the basic structure of a VTFT tooth.

The process begins with a basic RCA cleaning for the mono-Si substrates (The detailed RCA cleaning step could be seen in Annex I. For other kinds of substrates, for instance, glass substrates, a basic cleaning is required using alcohol and acetone solutions). After cleaning the substrates, a thick layer of oxide (about 500 nm) is deposited by APCVD technique at 420°C, which acts as a diffusion barrier in order to avoid the possible contamination of the layers by impurities from the substrates. In fact, the required minimum thickness of the buffer oxide layer is 200 nm, and the 500 nm oxide layer is a guarantee for the insulation.

After the deposition of the buffer oxide layer, three poly-Si layers are deposited, i.e., N-type heavily-doped poly-Si layer, undoped poly-Si layer, and N-type heavily-doped poly-Si layer in sequence. In fact, for the undoped layer, it is a little doped due to the structural defects of the poly-Si material, thus it is also called non-intentionally doped (Nid) layers. After each layer's deposition at 550°C, a subsequent SPC step is carried out at 600°C. The three layers' thicknesses are 300 nm, 1 μm, and 300 nm, respectively, and the deposited layers are shown in figure 2-10.

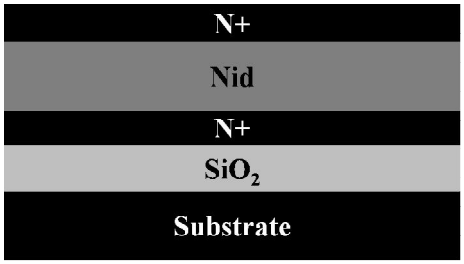


Figure 2-10: The deposited layers for the classical VTFT. The buffer SiO_2 is deposited by APCVD, while the three poly-Si layers are deposited by LPCVD technique, "N+" stands for the N-type heavily-doped poly-Si layer, while "Nid" stands for the undoped poly-Si layer.

As mentioned above, the first mask will be used for the definition of the basic teeth configurations of the VTFT. After the first photolithography step (the detailed photolithography step is explained in Annex II), the three poly-Si layers are etched by a RIE step. Afterwards, the global comb-shaped geometry is obtained, with the top and side views shown in figure 2-11 (a) and figure 2-11 (b), respectively. As we can see from the top view, the three-tooth structure is evident.

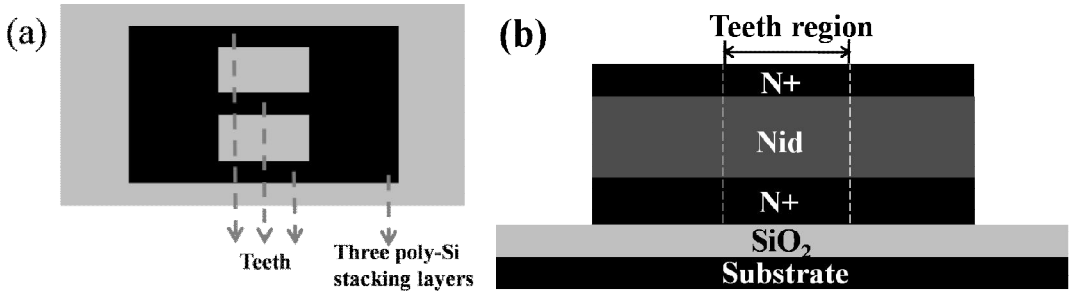


Figure 2-11: *(a)* Top view, and *(b)* side view of the comb-shaped VTFT configuration after the first RIE step.

However, due to the special location of the source (drain) underneath the top two poly-Si layers, an extension of the source (drain) is necessary. As a result, another RIE process is required in order to etch the top two layers and reach the bottom layer. This partial etching is precisely controlled by the aid of the laser interferometer. The corresponding top and side views after the second RIE are shown in figure 2-12. From the side view, the source (drain) extension is observed. For a DOT structure, the top and bottom heavily-doped layers (labeled as N+) are defined as drain and source, respectively, the channel length of the device is determined only by the thickness of the undoped layer (labeled as Nid) between the two

layers, whose thickness is1 μm.

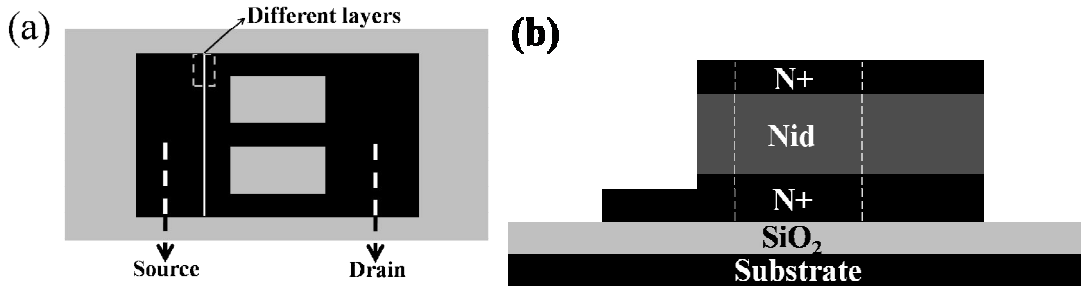


Figure 2-12: *(a)* Top view, and *(b)* side view of the VTFT configuration after the second RIE.

After the two RIE steps to define the tooth configuration as well as source and drain, another basic RCA cleaning is necessary before the deposition of the gate oxide. It is a critical step, which enables to eliminate most of the impurities on the interface of the channel, thus improve the electrical properties.

Then, another APCVD process is performed to deposit a 100 nm gate oxide layer followed by a densification step at 600°C for over 12 hours in order to eliminate most of the defects in the gate oxide. Afterwards, a wet etching process of the gate oxide using the third mask is implemented to make contact openings for source and drain. The corresponding schematic views after the wet etching of gate oxide are shown in figure 2-13. Note that, after making the contact openings, the major part of the VTFT is covered by the gate oxide, including the sidewalls.

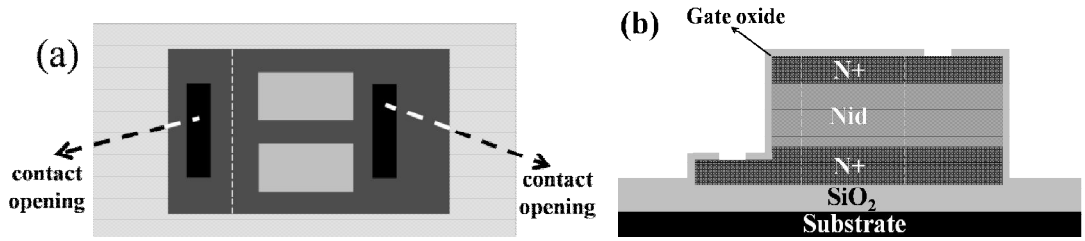


Figure 2-13: *(a)* Top view, and *(b)* side view of the VTFT configuration after the gate oxide deposition and making contact openings.

Finally, a 400 nm Al layer is deposited by Joule effect evaporation, and then the fourth mask is used to define the electrodes by wet etching. The final structure of the VTFT is gained, which is shown in figure 2-14. As the gate electrode is perpendicular to source and drain, it

controls all the channels at the same time. In addition, the gate overlap with the source and drain is evident. Note that, the channel width is defined by the width of the gate electrode passing all the teeth. The top SEM view of the fabricated VTFT is shown in figure 2-14 (c), and the gate electrode passing through all the sidewalls is evidenced.

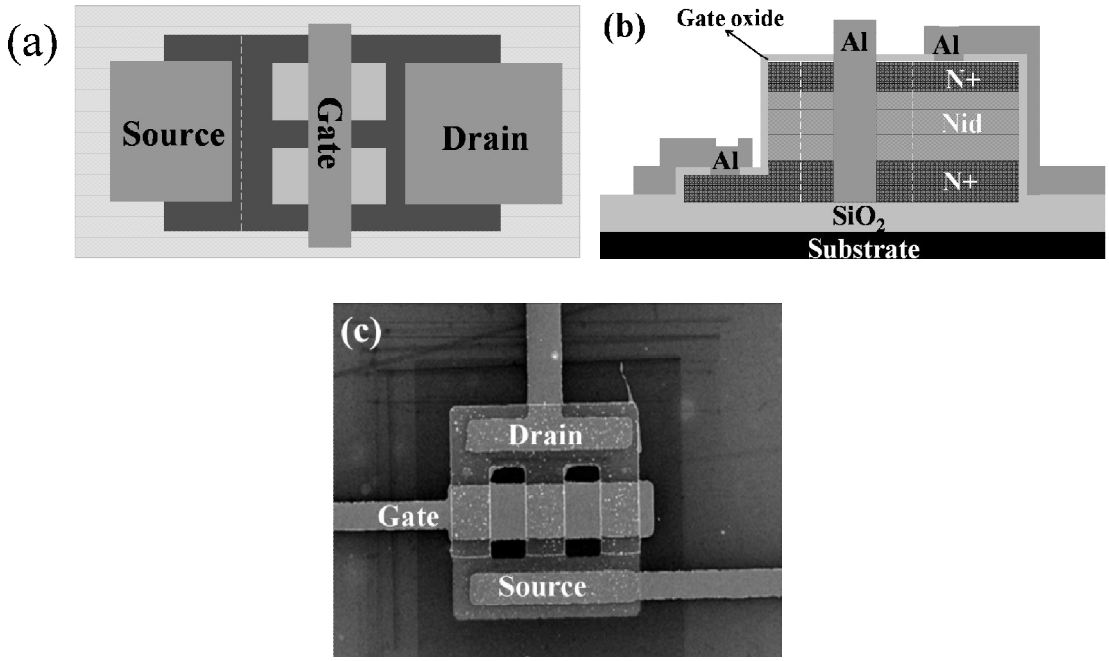


Figure 2-14: *(a)* Top view, *(b)* side view of the final VTFT after etching the deposited Al, and *(c)* SEM image of the fabricated three-tooth VTFT.

II.2 Technological challenges for the sidewalls formation – RIE parameters adjustment

For the VTFT, the gates are located on the sidewalls of the teeth, as shown in the SEM image of figure 2-14 (c). Thus, it is critical and necessary to ensure the continuity and the smoothness of the sidewall. Several tests of the RIE are carried out, the different RIE parameters, i.e., the gas flow Γ, the RF power W, and the partial pressure P are adjusted, and the optimized set of parameters will be adopted in the fabrication process. In our work, the adopted gas source for poly-Si etching is SF_6.

For the gas flow Γ, as mentioned above, it determines the average stay time of the source gas in the reactor, thus it is predictable that the gas flow Γ does not affect the sidewall morphology. For the RIE process of the classical VTFTs, the gas flow Γ of SF_6 is always set

to be 10 sccm.

For the RF power *W*, it determines the intensity of the F free radicals, and thus affects the ion bombardment energy. As a result, higher *W* is needed to increase the anisotropy property of the RIE in order to form high-verticality sidewalls.

For the pressure *P*, it affects the collisions between the F free radicals and the sample particles, thus it reflects the chemical encroachment of the F free radicals, which would lead to the isotropy property.

In order to optimize the etching slope, SEM observations are presented for different powers *W* and pressures *P* in figure 2-15, and figure 2-16, respectively. As shown in figure 2-15, for the same pressure *P* = 4 mTorr, when increasing the power *W*, the physical bombardment is more dominant, while the chemical erosion is weaker, which leads to the gradual elimination of the lateral overetching (the isotropic property).

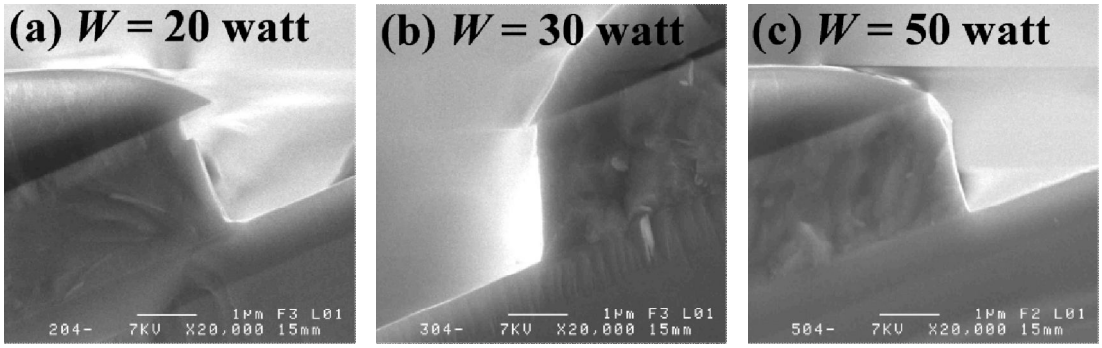


Figure 2-15: SEM images of sidewalls etched by different powers *W*: *(a) W* = 20 watt, *(b) W* = 30 watt, *(c) W* = 50 watt, pressure *P* = 4 mTorr, gas flow *Γ* = 10 sccm.

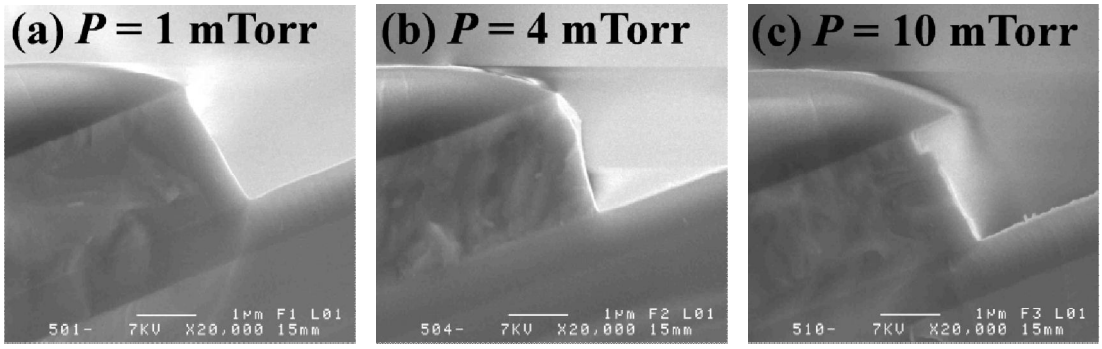


Figure 2-16: SEM images of sidewalls etched by different pressures *P*: *(a) P* = 1 mTorr, *(b) P* = 4 mTorr, *(c) P* = 10 mTorr, power *W* = 50 watt, gas flow *Γ* = 10 sccm.

In contrast, for the same power W = 50 watt, when increasing the pressure P, the chemical erosion is more dominant, which leads to the gradual enlargement of the lateral overetching (the isotropic property), which could be shown in figure 2-16. In conclusion, when etching at a higher power W with the reduced pressure P, the anisotropy RIE profile of the poly-Si could be formed.

III. Electrical characteristics and improvements on the classical VTFTs

III.1 Electrical parameters deduction

Transfer and output characteristics are two important indexes of the transistor's electrical performance. The output characteristics could help to confirm the transistor property, while the transfer characteristics enable to obtain the on/off-current ratio I_{ON}/I_{OFF}. There are also four other electrical parameters to describe the electrical properties of the transistor, i.e., the transconductance g_m, the subthreshold slope S, the threshold voltage V_{TH}, and the field effect mobility μ_{FE}. In theory, g_m, S, and μ_{FE} are defined by the following equation 2-10, equation 2-11 and equation 2-12, respectively:

$$g_m = \left(\frac{\partial I_{DS}}{\partial V_{GS}}\right)_{V_{DS}\ =\ constant} \qquad (eq.2-10)$$

$$S = \left\{\frac{\partial V_{GS}}{\partial(\log(I_{DS}))}\right\}_{V_{DS}\ =\ constant} \qquad (eq.2-11)$$

$$\mu_{FE} = g_m \frac{L}{W}\frac{1}{C_{OX}}\frac{1}{V_{DS}} \qquad (eq.2-12)$$

where C_{OX} is the gate oxide capacitance per unit area.

In fact, the four electrical parameters could also be obtained from the transfer characteristics. As shown in figure 2-17 (a), by plotting the drain current I_{DS} as a function of gate voltage V_{GS} in

the linear coordinate, the threshold voltage V_{TH} could be deduced by the gate voltage V_{GS} intercept value of the fit line for the linear portion. The transconductance g_m and the subthreshold slope S could be deduced from the fit line of the I_{DS} - V_{GS} curve in the linear coordinate system, and in the semi-logarithm coordinate system, respectively, which are indicated in figure 2-17 (a) and figure 2-17 (b), respectively. Therefore, the transconductance g_m corresponds to the slope of the fit line in the linear coordinate system, while the subthreshold slope S corresponds to the reciprocal of the slope for the fit line in the semi-logarithm coordinate system. After deducing the transconductance g_m, the mobility μ_{FE} could also be calculated by using the equation 2-12.

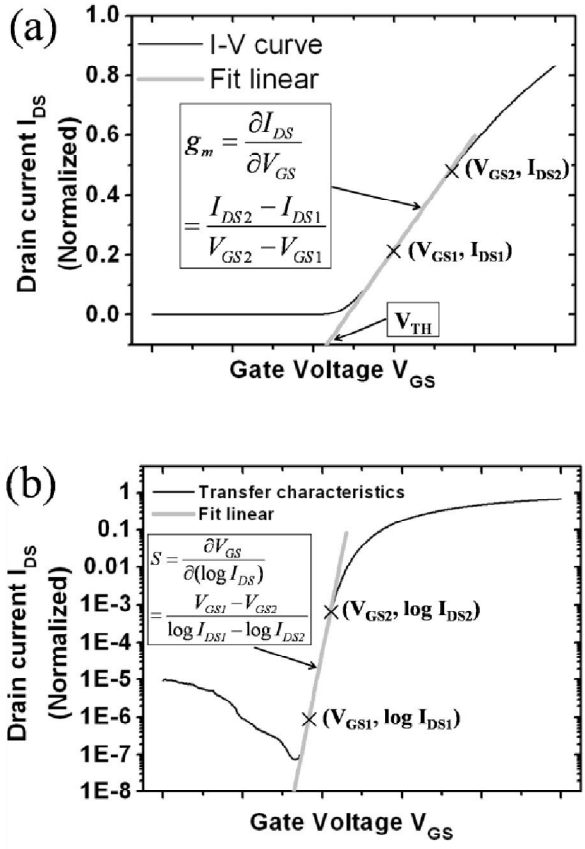


Figure 2-17: I_{DS}-V_{GS} curve *(a)* in the linear coordinate system, and *(b)* in the semi-logarithm coordinate system. The electrical parameters could be deduced from the two curves.

III.2 Electrical characteristics of the first classical VTFTs

After the fabrication of the classical VTFTs, the electrical measurements are carried out. The static current-voltage (*I-V*) measurements are achieved using a probe tester and an *Agilent*

Technologies B1500A semiconductor device analyzer, with the current measurement limitation of 0.1 fA. For the first VTFTs fabricated in our laboratory, among the three shapes of VTFTs, the stable electrical characteristics of the comb-shaped VTFTs are shown in figure 2-18. It shows an on/off-current ratio I_{ON}/I_{OFF} of more than 10^2 for different source-drain voltages V_{DS} of 0.1 V, 1.1 V, and 2.1 V. However, I_{OFF} is rather high due to the large overlapping area A_{OV} between source and drain, especially when using plastic masks for the first attempt with large design rule. Nevertheless, the feasibility of fabricating the classical VTFTs is proved.

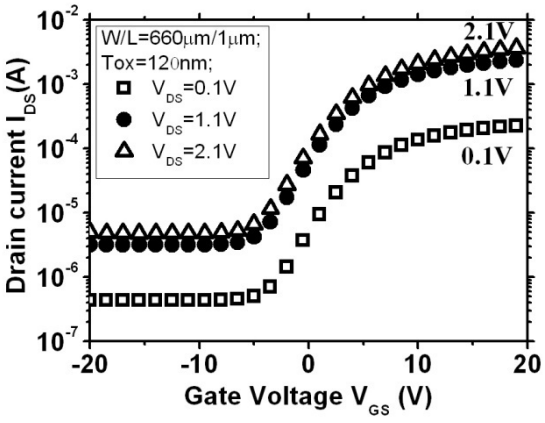


Figure 2-18: Typical transfer characteristics of the first classical VTFT, the high off-current I_{OFF} is due to the large overlapping area and short channel length L.

Drain-source Voltage V_{DS}	Threshold Voltage V_{TH}	Subthreshold Slope S	Trans-conductance g_m	Mobility μ_{FE}
2.1 V	1.51 V	3.82 V/dec	245 μS	6.14 $cm^2/V{\cdot}s$

Table 2-1: The electrical parameters deduced from the transfer characteristics for the classical VTFTs, the drain voltage V_{DS} = 2.1 V.

Table 2-1 shows the other electrical parameters deduced from the transfer characteristics. The low mobility μ_{FE} of 6.14 $cm^2/V{\cdot}s$ is observed, and the large subthreshold slope S = 3.82 V/dec could be improved by reducing the gate oxide thickness T_{ox}.

III.3 Parasitic channel suppression for the classical VTFT structure

As we could observe from the schematic side view of the classical VTFT shown in figure 2-19, the top electrode covers all the three poly-Si layers and thus forms a parasitic channel due to the thin gate oxide layer. This parasitic channel has a great negative effect on the final

electrical properties of the fabricated VTFT, by providing a supplement current when the device is at the off-state that increases the off-current I_{OFF}. Therefore, some work should be done to suppress the parasitic channel.

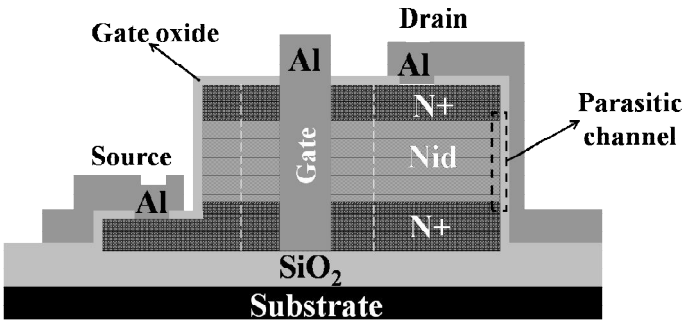


Figure 2-19: Schematic side view of the classical VTFT, the parasitic channel is observed at the backside of the top electrode.

III.3.1 Modification of the fabrication process

In order to suppress the parasitic channel, after the two RIE steps to define the comb shape and form the source and drain regions, a thick oxide layer is deposited at the backside of three layers stacking before the gate oxide deposition, by utilizing one more mask. The resulted schematic views are shown in figure 2-20, and the thickness of the deposited oxide layer is 500 nm.

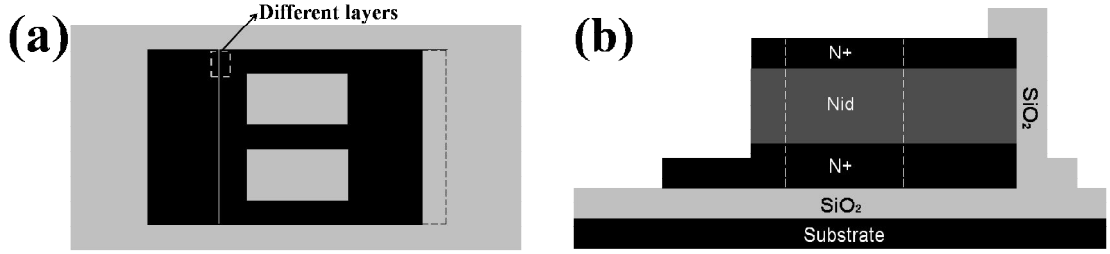


Figure 2-20: *(a)* The top view, and *(b)* the side view of the improved structure for the classical VTFT, a 500nm oxide layer is deposited at the backside of the top electrode, which helps to suppress the parasitic channel after electrodes formation.

Afterwards, the same steps as the original structure of the classical VTFT, including the gate oxide deposition, contact openings, Al deposition and electrodes formation, are carried out in sequence. The schematic images of the improved structure are shown in figure 2-21 (a) and figure 2-21 (b). Figure 2-21 (c) shows the SEM top view of the finally fabricated VTFT,

the four teeth are shown, and the thick oxide layer is also marked at the backside of the top electrode.

Figure 2-21 (d) shows the SEM image of the sidewall after the gate oxide and Al depositions. As the formed sidewall is not strictly vertical, it is also called "quasi-vertical sidewall". In fact, this quasi-vertical sidewall has been beneficial for the layers deposited on the sidewall, which guarantees a conformal deposition of the gate oxide layer and a continuous deposition of the Al layer on the sidewall, as shown in figure 2-21 (d). The only shortcoming of the quasi-vertical sidewall is a little increase of the channel length L due to the tilt angle of about 70°, which is in fact about a 6% increase (1/cos70° = 1.06) of the channel length L.

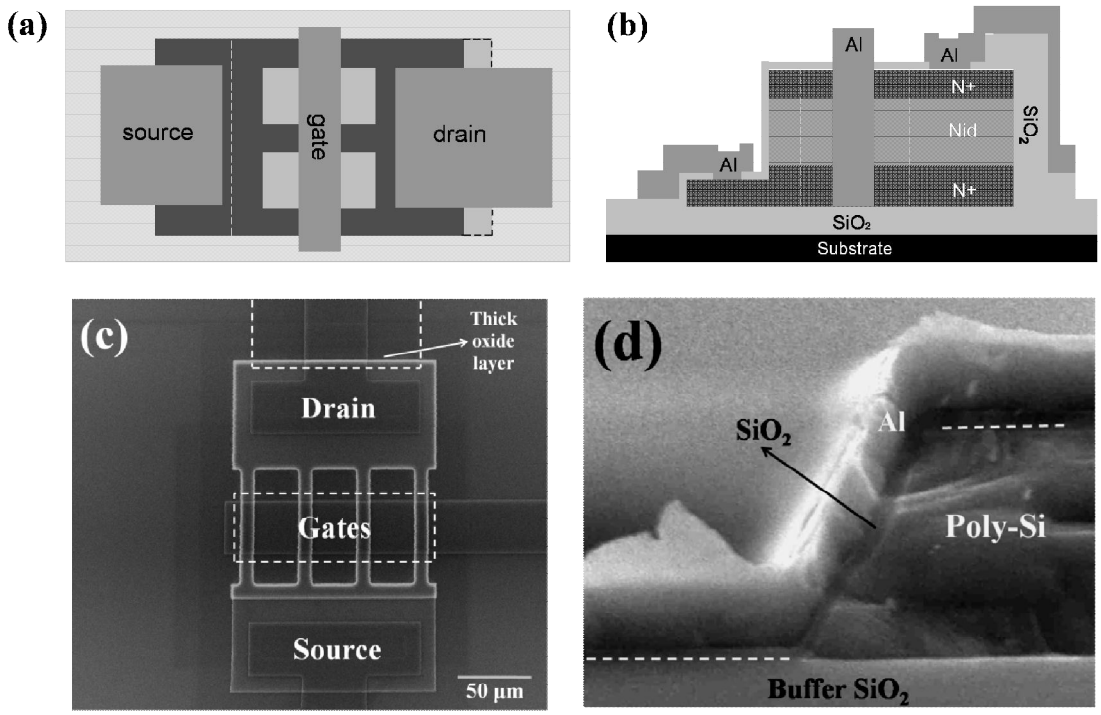


Figure 2-21: *(a)* The schematic top view, *(b)* the schematic side view, *(c)* the SEM image of the improved four-tooth VTFT configuration, the 500 nm thick oxide layer at the backside of the top electrode (signed as drain) enables to suppress the parasitic channel, and *(d)* the SEM image of the sidewall after the gate oxide and Al layers' deposition, the conformal SiO_2 layer and the continuous Al layer on the sidewall are observed.

III.3.2 Geometric definitions of the improved classical VTFT structure

After the basic knowledge of the classical VTFTs rapidly fabricated by using the plastic

masks, a new set of glass masks (five masks) has been designed for the improved structure of the classical VTFT. Device dimensions have been shrinked due to the comparatively smaller design rule of the glass masks. In addition, in order to analyze the effects of the geometric parameters on the electrical properties of the classical VTFTs, different geometric parameters have been defined to describe the three-dimensional (3D) device configurations, which could be seen from the Annex III. In fact, different geometric parameters also help to verify the reproducibility and uniformity of the fabricated VTFTs.

The layout of the masks are designed by the aid of the CADENCE VIRTUOSO software, and the four-tooth definitions for the improved classical VTFT (after parasitic channel suppression) are shown below in figure 2-22, with the key geometric parameters marked in the figure. From the mask design, the five-mask process flows of the improved classical VTFT could also be traced.

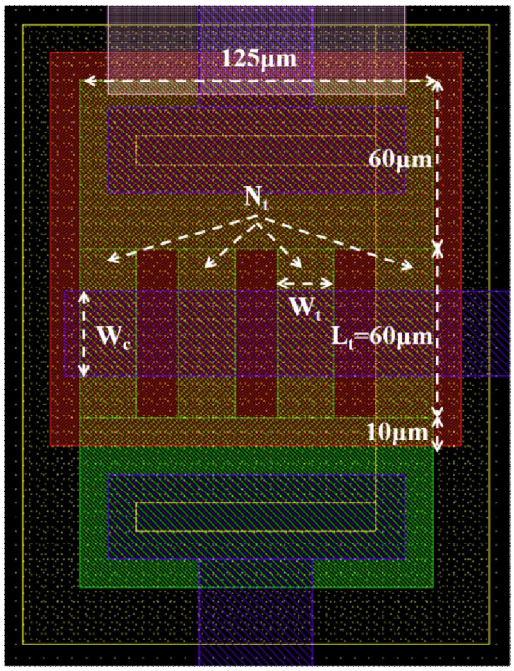


Figure 2-22: The five-mask design of a four-tooth classical VTFT, different geometric parameters are marked in the figure.

The key geometric parameters of the VTFTs are listed below:

- L_t: the length of a tooth, which is fixed at the value of 60 µm.

- N_t: the teeth number, the optional values for N_t are 1, 2, 4, and for the device shown above, $N_t = 4$.
- W_t: the width of a tooth, which has the alternative values of 10 μm and 20 μm. For the four-tooth device shown above, $W_t = 20$ μm.
- W_c: single channel width, it is defined by the width of the gate electrode, as the on/off state is controlled by the gate electrode on the sidewalls. The optional values are set to be 10 μm, 20 μm, and 30 μm in the designs, respectively, and for the chosen devices shown above, $W_c = 30$ μm.
- W: the total channel width, which is defined by the formula $W = 2N_tW_c$, as there are two channels located on the two sidewalls of one tooth.

There are also other geometric parameters marked in figure 2-22, such as the fixed values of 125 μm for the device width, 180 μm for the device length, and especially for the channel length L, it is determined by the thickness of the deposited layer between source and drain, i.e., the undoped (Nid) poly-Si layer.

III.3.3 Electrical characteristics of the improved classical VTFT structure

As mentioned above, by adding a thick SiO_2 layer at the backside of drain, the parasitic channel is suppressed. The typical transfer characteristics of the four-tooth drain-on-top (DOT) classical VTFT are shown in figure 2-23 (a), with the drain-source voltage V_{DS} as the independent variable ($V_{DS} = 0.1$ V, 1 V). The gate leakage current is measured to be low enough (around 600 pA when $V_{GS} = 20$V), so we can conclude the good coverage of the gate oxide on the sidewall. The high on-current I_{ON} of the VTFT is due to the larger channel width/length ratio W/L, in comparison with its lateral counterpart, which has been explained in chapter 1 [73], and the on-current I_{ON} of a VTFT increases in proportion to W/L.

From the transfer curves, several electrical parameters are deduced ($V_{DS} = 1$V) and shown in table 2-2. The low field effect mobility μ_{FE} of 4 $cm^2/V{\cdot}s$ in comparison with the one obtained from LTFT (whose mobility μ_{FE} is more than 100 $cm^2/V{\cdot}s$), is mainly due to the high roughness of the sidewalls caused by the long-time RIE, the defects near the channels

dramatically degrade the electrical parameters for the poly-Si VTFT. Therefore, the mobility μ_{FE} could be enhanced by the modification of the sidewall roughness, either by a low-temperature wet oxidation and a subsequent HF dipping, or simply by a RCA cleaning way. Another factor that affects the electrical characteristics is the gate oxide thickness T_{OX}. The high threshold voltage V_{TH} = 8V and the high subthreshold slope S of 3.6 V/dec could be explained by the high gate oxide thickness T_{OX} = 120 nm.

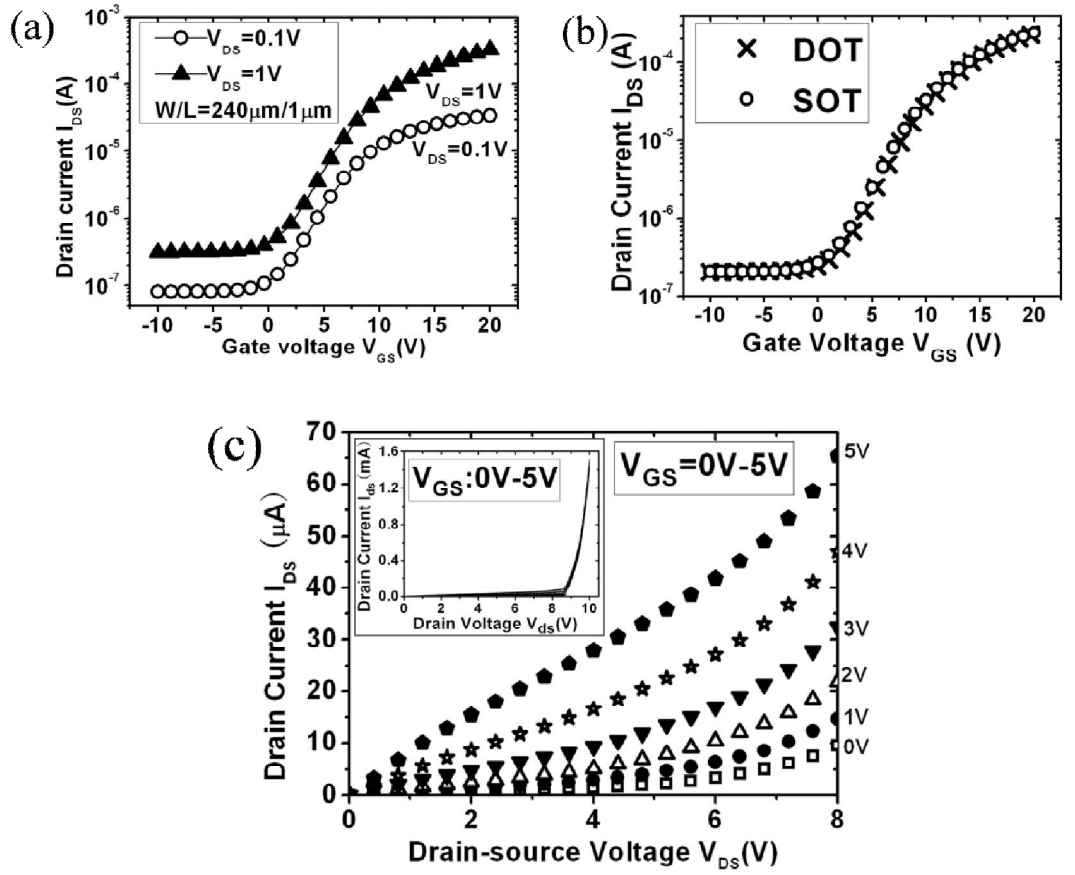


Figure 2-23: *(a)* Typical transfer characteristics, *(b)* symmetric transfer characteristics for DOT and SOT structures, *(c)* output characteristics of the classical VTFTs after the parasitic channel suppression, the inset in figure 2-23 *(c)* shows the strong kink effect when the drain voltage V_{DS} is higher than 8.5V.

V_{DS} (V)	V_{TH} (V)	S (V/dec)	g_m (μS)	μ_{FE} (cm^2/V·s)
1	*8*	*3.6*	*30*	*4*

Table 2-2: The electrical parameters deduced from the transfer characteristics.

By reversing source and drain, the source-on-top (SOT) structure is gained. The similar

transfer characteristics of the SOT and DOT structures are obtained and shown in figure 2-23 (b), which proves the symmetry in the structure, i.e., the similar interface between the heavily-doped layer (source/drain layer) and the Nid layer.

The output characteristics of the four-tooth VTFT are shown in figure 2-23 (c). The saturation region is not observed because of the kink effect, which could be obviously shown in the inset of figure 2-23 (c), when the drain-source voltage $V_{DS} \geq$ 8.5 V. The kink effect is due to the impact ionization at the drain end of the channel, as the short channel length L = 1 μm leads to a high drain field when the device is operating in saturation. Thus the kink effect could be suppressed by depositing a higher channel length (undoped poly-Si layer thickness) or by introducing the drain field relief structures as the lightly doped drain (LDD) [102].

III.3.4 The effect of geometric parameters on the electrical characteristics

For the classical VTFT, the total channel width $W = 2N_tW_c$, where N_t is the teeth number and W_c is the single channel width. Therefore, the on-current I_{ON} is proportional to the teeth number of N_t and the single channel width W_c:

$$I_{DS} = \frac{W}{L}\mu_{FE}C_{OX}[(V_{GS}-V_T)-\frac{V_{DS}}{2}]V_{DS}$$
$$= \frac{2N_tW_c}{L}\mu_{FE}C_{OX}[(V_{GS}-V_T)-\frac{V_{DS}}{2}]V_{DS} \ (\mathrm{V_{DS}} \leq (V_{GS}-V_T)) \quad (eq.2\text{-}13)$$

Figure 2-24 (a) and 2-24 (b) show the relationship between the on-current I_{ON} and the geometric parameters, i.e., the single channel width W_c and the teeth number N_t. As expected, the two figures prove the linear variation of I_{ON} with the total channel width W, according to the equation 2-13, and they also validate the technological fabrication of the VTFT. As a result, the calculated on-current per unit channel width is about 1.37 μA/μm when the drain-source voltage V_{DS} is 1 V.

Figure 2-24 (c) shows the relationship between the on-current I_{ON} and the tooth width W_t, and it is observed that W_t does not affect the on-current I_{ON}, as the total channel width W and channel length L do not change. The abnormal value in figure 2-24 (c) (when the teeth width

is W_t = 10 μm, and the total channel width W = 80 μm) is due to the disabled teeth of the corresponding VTFT.

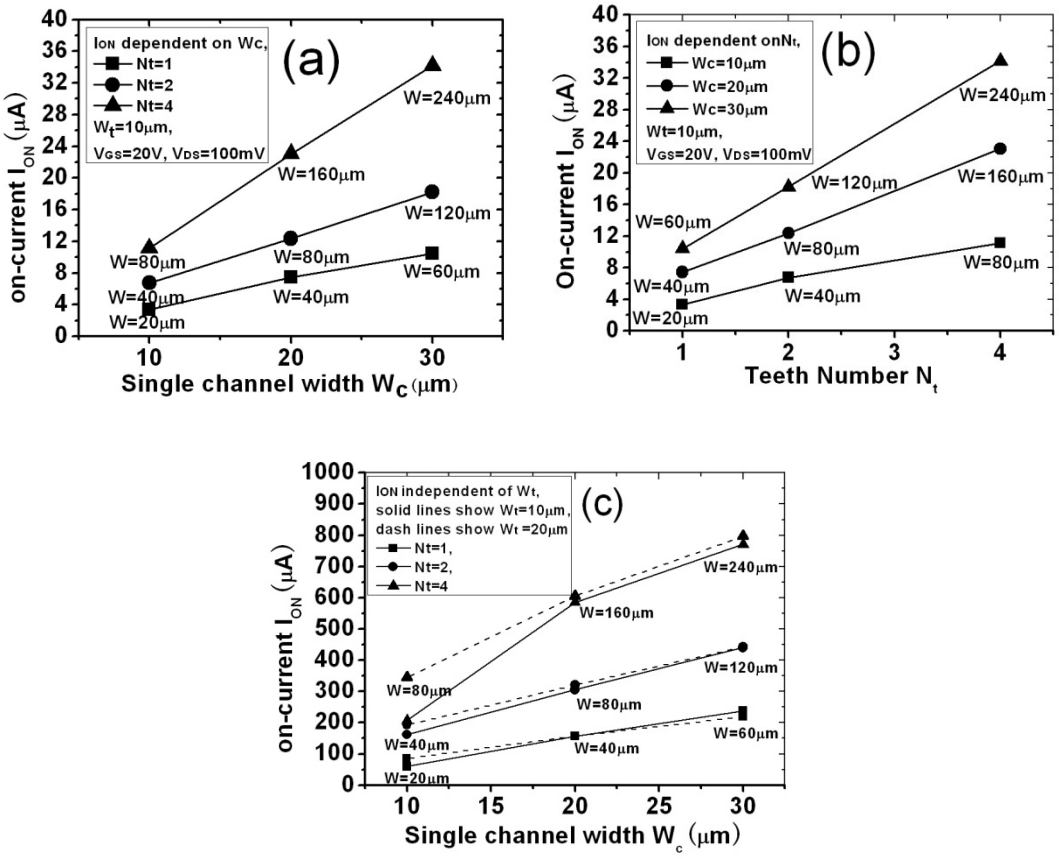


Figure 2-24: The relationship between the on-current I_{ON} and the geometric parameters: (a) I_{ON} is proportional to the teeth number N_t, (b) I_{ON} is proportional to the single channel width W_c. The two relationships confirm the theoretical formula of on-current I_{ON}, and (c) I_{ON} is not affected by the teeth width W_t.

The off-current, I_{OFF}, appears too high that leads to an I_{ON}/I_{OFF} ratio in the order of 10^3. Figure 2-25 shows the off-current I_{OFF} as a function of drain–source total overlapping area A_{OV}, 1.1 x 10^4 μm^2 in the case of the four-tooth VTFT shown in figure 2-21 (c). The different data points correspond to the teeth number N_t = 1, 2 and 4, respectively. In the inset, the region enclosed in the dashed lines shows the total overlapping area A_{OV}, which is made up of two parts: the total area of teeth, the source and drain common area. Therefore, A_{OV} could be expressed by the following equation:

$$A_{OV} = A_{SD} + N_t A_t = A_{SD} + N_t L_t W_t \qquad (eq.2-14)$$

where A_{SD} is the common area of source and drain sides, i.e., the overlapping area out of the teeth (shown in the inset of figure 2-25), N_t is the teeth number, A_t is the area of a single tooth, while L_t and W_t stand for the tooth length and width, respectively. In our design, A_{SD} is fixed at 8750 μm^2, and L_t is fixed at 60 μm, while W_t is chosen to be 20 μm for analysis.

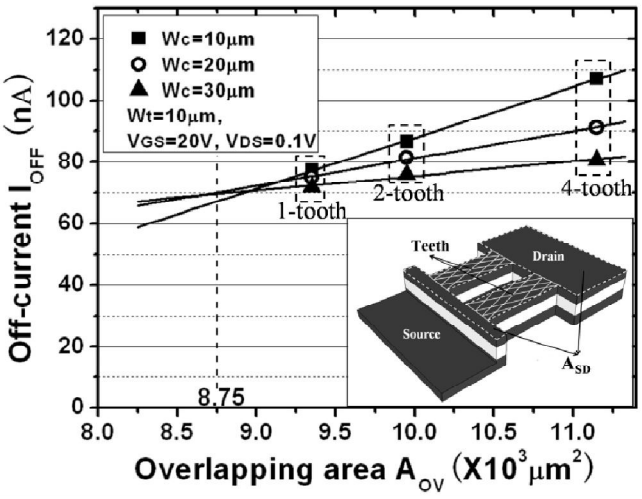


Figure 2-25: The relationship between the off-current I_{OFF} and the total overlapping area A_{OV}: I_{OFF} is proportional to A_{OV}. For the same teeth number N_t, the off-current I_{OFF} is also reduced by the increase of the single channel width W_c. The inset shows the schematic of the classical VTFT structure, the total overlapping area A_{OV} is marked with the dashed lines.

For a fixed value of the single channel width W_c, the variation of off-current I_{OFF} with the overlapping area A_{OV} is linear, which is due to the increase in the teeth number N_t according to the equation 2-14, therefore, I_{OFF} is dependent on the teeth number N_t and thus the total area of teeth (N_tA_t). In fact, the large total overlapping area A_{OV} drastically increases the total off-current I_{OFF} by the leakage current flowing through the undoped poly-Si film.

From the cross points of the straight lines corresponding to the common area A_{SD} of source and drain sides (8750 μm^2), the average off-current density per area unit is deduced to be around 8 pA/μm^2.

The third interesting result is that, for the VTFTs with the same teeth number N_t, while increasing the single channel width W_c, the off-current I_{OFF} decreases. This may be due to the fact that, when the single channel width W_c increases, more part of the teeth is under the control of the gate reverse bias. In other words, as the current is not minimum at V_{GS} = 0 V, the total

leakage current flowing in the channel region out of the gate is higher than the region that is under the gate contact. When the equivalent gate width increases, the complementary part decreases, thus the total leakage current reduces.

As previously mentioned, the rather large overlapping area of the structure, in comparison with the small channel regions, degrades the electrical performances of the VTFT. Therefore, in order to avoid the large overlapping area between source and drain and thus reduce the off-current I_{OFF}, the overlapping area A_{SD} at the source and drain sides could be reduced in two different ways, 1) the larger contribution of the overlapping area (125 μm × 60 μm) at the drain side (shown in the inset of figure 2-25) could be suppressed by the introduction of a thick SiO_2 layer before the deposition of the top drain layer; 2) the overlapping area of 125 μm × 10 μm at the source side could also be reduced. In fact, the major part of the total overlapping area A_{OV} could be eliminated. The improved classical VTFT structure and the corresponding characteristics are given below.

III.4 Overlapping area reduction and corresponding characteristics

III.4.1 Modification of the fabrication process

As it is shown in the inset of figure 2-25, the drain side enclosed in the dashed rectangle occupies the major part of the overlapping area, which dominates the off-current I_{OFF}. In order to eliminate this large drain overlapping area, a thick layer of SiO_2 (400 nm) is deposited by APCVD technique and patterned by wet etching before the top heavily-doped layer deposition. Therefore, by aligning the drain side with this SiO_2 region, the three polysilicon layers' stacking at the drain side is eliminated by the introduction of the thick oxide layer, and thus the total overlapping area is reduced. In addition, the overlapping area at the source side could also be reduced until to the lithography limitation. The schematic and SEM images of the improved structure is shown in figure 2-26 (a) and 2-26 (b), respectively.

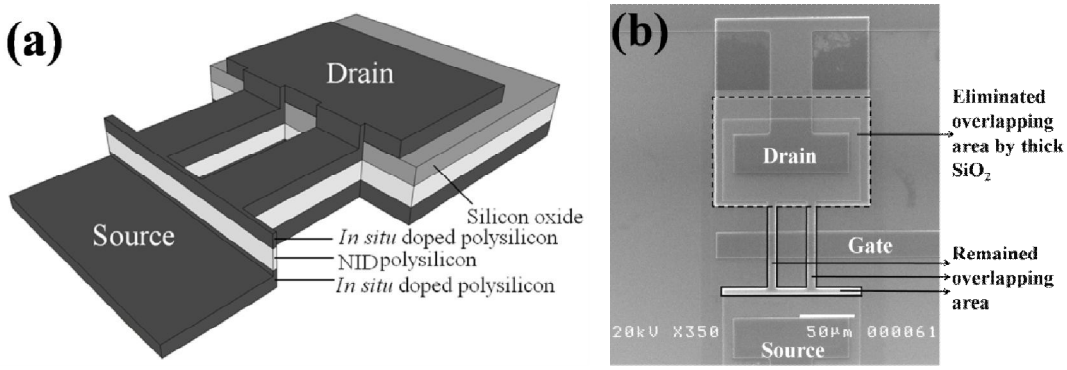


Figure 2-26: *(a)* Three-dimensional, and *(b)* SEM images of the two-tooth classical VTFT after the overlapping area reduction, the reduction is mainly obtained by the introduction of a thick oxide layer at the drain side.

Note that, even the parasitic channel is suppressed at the backside of the drain due to the introduction of the thick oxide layer, the thick oxide deposition originally used for parasitic channel suppression before the gate oxide deposition should also be deposited as a guarantee.

III.4.2 Electrical characteristics of the classical VTFT with reduced overlapping area

As shown from figure 2-25, the large off-current I_{OFF} is proportional to the overlapping area A_{OV} between source and drain. After the reduction of the overlapping area at the drain side, the off-current I_{OFF} should also be accordingly reduced. The remained overlapping area A'_{OV} could also be divided into two parts, the source part area A_S, and the teeth part area N_tA_t, which could be expressed by the following equation:

$$A'_{OV} = A_S + N_t A_t = A_S + N_t L_t W_t \qquad (eq.2-15)$$

According to previous calculation, the off-current per unit area is 8 pA/µm^2 (70 nA corresponding to 8750 µm^2). Table 2-3 shows the drain currents comparison before and after the overlapping area reduction at the drain side, when there is no gate voltage applied on the VTFT, and drain-source voltage V_{DS} = 1V.

It is shown that the drain current has been reduced about 72 nA (I_{DS} - I'_{DS}) on average. However, considering the actual reduced area of about 8000 µm^2 (A_{SD} - A_S) in the process, the reduced off-current I_{OFF} is calculated to be about 64 nA. The larger reduction of drain-source

current I_{DS} (without gate bias) in comparison with the reduction of off-current I_{OFF} (with gate bias), is due to the fact that I_{OFF} is not gained at V_{GS} = 0 V, and the negative gate voltage V_{GS} has suppressed the drain-source current I_{DS} to some degree, as mentioned previously.

Total overlapping area A_{ov} (μm^2)	A_{SD}+ 1×60×10	A_{SD}+ 2×60×10	A_{SD}+ 4×60×10	A_{SD}+ 1×60×20	A_{SD}+ 2×60×20	A_{SD}+ 4×60×20
Total drain current I_{DS} (nA)	***84.5***	***90***	***101***	***90***	***101***	***122***
Reduced overlapping area A'_{ov} (μm^2)	A_S+ 1×60×10	A_S+ 2×60×10	A_S+ 4×60×10	A_S+ 1×60×20	A_S+ 2×60×20	A_S+ 4×60×20
Reduced drain current I'_{DS} (nA)	***12.7***	***18.3***	***27.8***	***18.3***	***28.6***	***49.9***

Table 2-3: Comparison of drain-source currents before and after the reduction of the overlapping area.

This phenomenon could also be shown in figure 2-27, which demonstrates the comparison between the drain-source leakage currents I_{DS} (without gate voltage) and the off-currents I_{OFF} (with gate voltage). Except for the point of 107 nA, the other off-current data are less than the corresponding drain-source current I_{DS} without gate voltage, which indicates the effect of the gate voltage V_{GS} on the reduction of the off-current I_{OFF}.

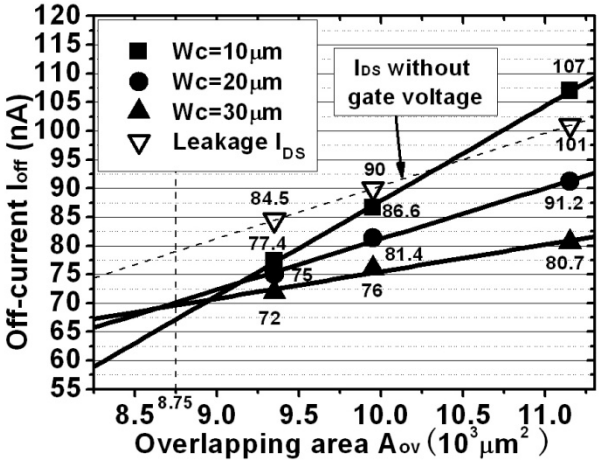


Figure 2-27: Comparison between the drain-source current I_{DS} (without gate voltage) and the off-current I_{OFF} (with gate voltage), the gate voltage helps to suppress the drain current to some degree.

After the overlapping area reduction using a thick oxide layer, the transfer characteristics of a classical VTFT is shown in figure 2-28. The I_{ON}/I_{OFF} ratio almost reach 10^5, however, the

off-current I_{OFF} is in the order of 10 nA when the drain-source voltage V_{DS} = 1 V. This I_{OFF} brought by the remained overlapping area A'_{OV} should be further reduced. In addition, the reproducibility of the improved structure is rather bad because of the complex process (six-mask process).

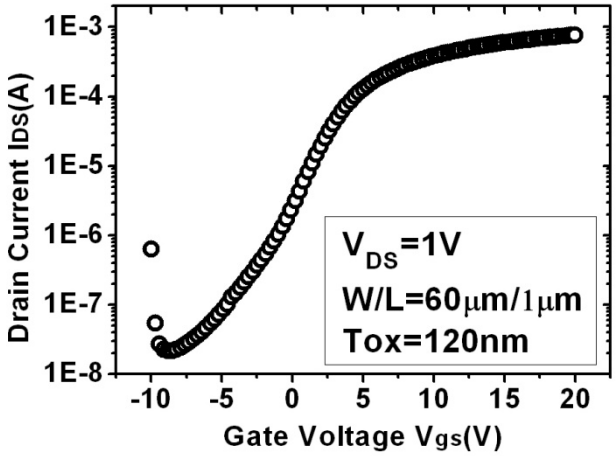


Figure 2-28: Transfer characteristics of the classical VTFT structure after the reduction of the large overlapping area, the off-current reduces that leads to an I_{ON}/I_{OFF} ratio of almost 10^5.

IV. Conclusion

In this chapter, the basic process flow of the classical VTFT and the corresponding electrical characteristics are described. Initially, the related materials, deposition and dry etching methods used in the processes are introduced, including the LPCVD technique for poly-Si and Si_3N_4 deposition, APCVD technique for SiO_2 deposition, Joule effect evaporation technique for Al deposition, and RIE technique for devices patterning.

The widely-used material in thin film technology is poly-Si deposited by LPCVD technique, which shows the compromise between the crystalline quality and the deposition facility. By the a-Si deposition by LPCVD at 550°C and 90 Pa and then a crystallization step (SPC) at 600°C under vacuum, the obtained poly-Si could gain better structural quality, and this mature technique has been used in the LTFTs fabrication in our laboratory. Therefore, our VTFTs fabrication is also based on this SPC-involved technique.

For the VTFTs fabrication, RIE technique is a critical step for the patterning of the basic

VTFT configuration, as the sidewall slope affects the conformal deposition of gate oxide and Al contacts and thus greatly influences the electrical characteristics. For the classical VTFTs, the optimized value is gained at RF power W = 50 watt, pressure P = 1 mTorr, and the SF_6 gas flow Γ = 10 sccm.

The classical VTFT is obtained by rotating LTFT 90°. Initially, four plastic masks are employed to fabricate the VTFTs, and the first characteristics have been obtained. However, there is a parasitic channel at the backside of the device, and a new set of glass masks are introduced. After the elimination of the parasitic channel by depositing a thick oxide layer at the backside, the transfer characteristics and output characteristics have been measured. The on-current I_{ON} shows the linear relationship with the teeth number N_t and the single channel width W_c, i.e., I_{ON} is proportional to the total channel width W, as expected, while it is independent of the tooth width W_t. In a word, very good relationship between on-current I_{ON} and geometric parameters has been obtained. The off-current I_{OFF} is proportional to the overlapping area A_{OV}, and the calculated I_{OFF} density is about 8 pA/μm^2.

Afterwards, the major part of the large overlapping area has been eliminated by the introduction of a thick oxide layer at the drain side (for a DOT structure), and the resulted I_{ON}/I_{OFF} is in the order of 10^5. However, I_{OFF} is still in the order of 10 nA for the drain-source voltage V_{DS} = 1V due to the remained overlapping area, and the reproducibility is rather low due to the complex process.

In the next chapter 3, a new VTFT structure will be proposed to totally eliminate the large overlapping area by introducing a barrier layer between source and drain. For the new structure, the sidewall profile is still very important, and a lot of work will be devoted to the formation of the sidewalls. In addition, some study on the barrier layers will also be made. After the adjustment of the sidewall profiles and the study on the barrier layers, the electrical characteristics of the new VTFTs will be measured, analyzed and discussed. In addition, different active layers of the new VTFTs will also be studied. Finally, the electrical properties of P and N-type VTFTs will also be shown.

Chapter 3 Process flows and electrical characteristics of the new VTFTs

In chapter 2, the detailed process flow of the classical VTFTs has been described, and the corresponding electrical characteristics have also been analyzed. The results have highlighted the high off-current I_{OFF} due to the large overlapping area, which degrades the electrical characteristics of the VTFTs and leads to a low I_{ON}/I_{OFF} ratio in the order of 10^3. Even some efforts have been made to reduce the large overlapping area and the I_{ON}/I_{OFF} almost reaches 10^5, this ratio cannot be further increased. In addition, the complex process also reduces the reproducibility of the improved classical VTFT. Therefore, the new VTFT structure should be proposed in order to improve the transistor properties with a high reproducibility.

I. Transition from the classical VTFT to the new VTFT

I.1 Discussion on the classical and the new VTFTs

For the classical VTFT, due to the high overlapping area between source and drain (as shown in figure 3-1 (a)), which leads to a high leakage current passing through the undoped poly-Si layer from source to drain, the I_{ON}/I_{OFF} ratio is rather low. Even by introducing a thick oxide layer to eliminate the major part of the overlapping area, the resulted I_{OFF} still exceeds 10nA when drain-source voltage V_{DS} = 1 V, while the reproducibility is rather low due to the complex process. New VTFTs structure should be proposed in order to overcome the two problems.

Initially, we propose a structure that introduces a barrier layer not only at source and drain sides, but also at the major part of the teeth. Therefore, the total overlapping area is almost eliminated, and only a limited area for the active layer at the tooth part is allowed. The schematic view is shown in figure 3-1 (b), the active layer is just located at the two sides of the barrier layer in the tooth part, with a negligible area determined by the design rule λ. However, as the tooth width W_t has already reached the design rule limitation, further process on the tooth will increase the complexity of the fabrication process, and thus reduce the reproducibility of the devices.

The other solution is that, by introducing a barrier layer that totally blocks the source and

drain regions (including the teeth part), the overlapping area between source and drain is totally eliminated. Different from the classical VTFT structure, the active layer is deposited after the formation of the source and drain layers. As shown in figure 3-1 (c), the active layers are just deposited on the sidewalls of the tooth, which further highlights the importance of the sidewall profiles, as the sidewall profiles would affect the crystallization of the undoped poly-Si active layer. Nevertheless, the large overlapping area can be eliminated, which helps to reduce the off-current I_{OFF}. In addition, the complex process is also avoided, which should enable a better reproducibility.

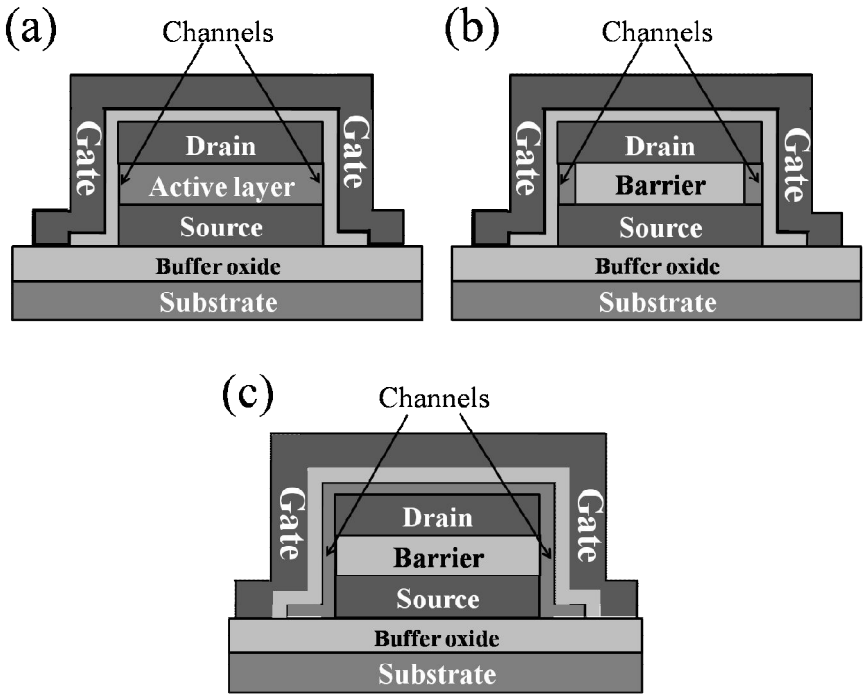


Figure 3-1: Schematic view of the tooth structure for *(a)* the classical VTFT, and *(b)* the improved classical VTFT, and *(c)* the new VTFT.

I.2 Simulation of the two VTFT structures

Prior to the fabrication process of the new VTFT, a simple two-dimensional (2D) simulation has been carried out, in order to theoretically analyze the electrical characteristics of the classical and the new VTFTs. The simulation is made by the aid of the software SILVACO, of which the module ATHENA is used to create the device structure, while the module ATLAS is adopted to apply appropriate material properties for each layer, set the

measurement conditions, and simulate the transfer characteristics of the VTFTs. Note that, the layers' mobility properties are based on the mono-Si layer, and the test temperature is set to be 300 K.

Figure 3-2 (a) shows the simulated structure of the classical VTFT, a large overlapping area between source and drain has been observed. For the heavily-doped poly-Si layers (source and drain, labeled as "N+ poly-Si"), the thicknesses are set to be 300 nm and 600 nm, respectively, and the doping level is set to be 10^{20} cm^{-3}. For the undoped poly-Si layer (active layer), the thickness is set to be 1μm, the doping level is set to be 10^{16} cm^{-3}, due to the non-intentionally doping (Nid) property caused by the poly-Si structural defects. For the new VTFT shown in figure 3-2 (b), the large overlapping area is eliminated by the barrier layer, and the undoped poly-Si active layer is deposited on the sidewall. The barrier layer is a 100 nm SiO_2 layer, while the active layer thickness is also set to be 100 nm, with the doping level of 10^{16} cm^{-3}. For the heavily-doped poly-Si layers, the thicknesses are 300 nm and 600 nm, respectively, with the doping level of 10^{20} cm^{-2}. The detailed program in ATLAS module is given in Annex IV.

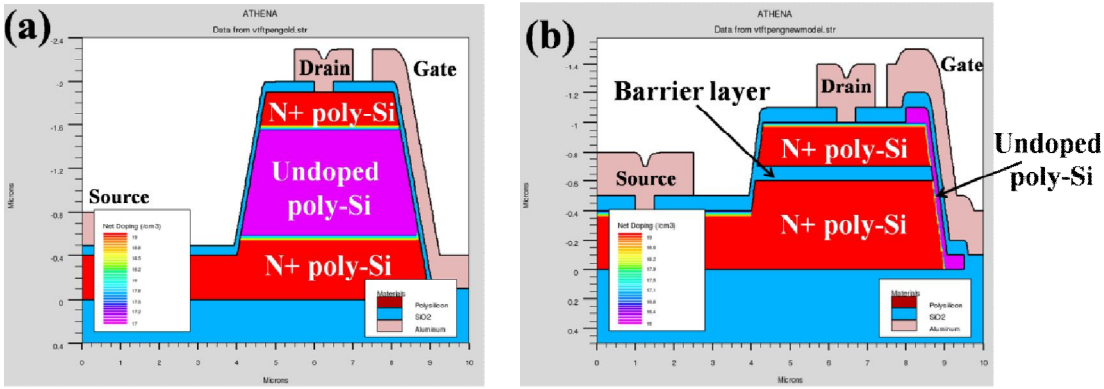


Figure 3-2: Simulated structure of *(a)* the classical VTFT, and *(b)* the new VTFT. The classical VTFT shows a large overlapping area between source and drain, while for the new VTFT, the overlapping area is suppressed by the barrier layer. "N+ poly-Si" stands for the N-type heavily-doped poly-Si.

Figure 3-3 shows the simulated transfer characteristics of the two VTFT structures. It is shown that the on-currents of the two structures keep the same, while the off-current of the new VTFT decreases more than one order in comparison with the classical VTFT, which is

due to the elimination of the large overlapping area. Even though we adopt 2D models for our 3D structures, the trend of the reduced off-current I_{OFF} should be the same, which theoretically validates the feasibility of the new VTFT in I_{OFF} reduction.

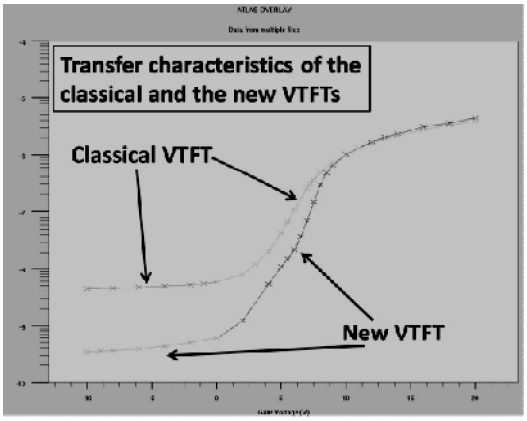


Figure 3-3: Simulated transfer characteristics comparison between the classical and the new VTFTs. The off-current I_{OFF} has been reduced by the barrier layer.

II. Structure, process, and key technique of the new VTFT structure

II.1 Basic process flow of the new VTFT structure

The simulation of the transfer characteristics for the two VTFT structures has validated the effective reduction of the off-current I_{OFF} of the new VTFT, by introducing a barrier layer between source and drain. Therefore, the fabrication process of the new VTFT is carried out. The typical three-dimensional structure of the new VTFT is shown in figure 3-4.

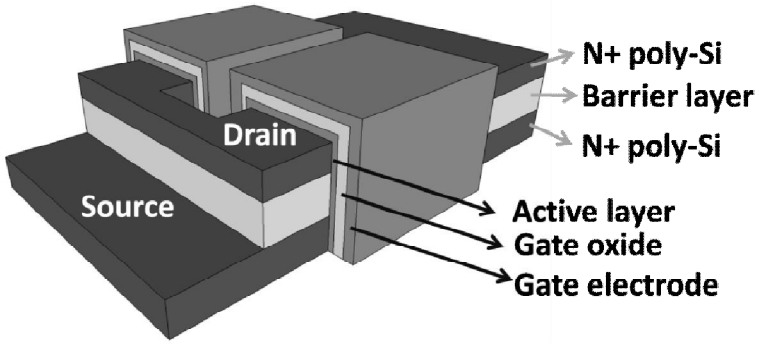


Figure 3-4: Three-dimensional view of the new VTFT structure, "N+ poly-Si" stands for the N-type heavily-doped poly-Si layer.

From the 3D schematic structure, it is shown that there is a barrier layer between source and drain. Therefore, the large overlapping area between source and drain is blocked. The active layer is deposited on the sidewalls after the formation of the teeth, thus the sidewall profile is very important to the electrical characteristics.

As mentioned in chapter 1, the classical VTFT structure could be seen as rotating the LTFT 90°. Note that, the corresponding LTFT is in fact a top-gate LTFT. For the tooth structure of this new VTFT structure, it is in fact evolved from the back-gate LTFT. Figure 3-5 (a) shows the back-gate LTFT structure, and when rotating the back-gate LTFT 90° (the region enclosed in the dashed lines), the basic structure of the new VTFT is obtained, as shown in figure 3-5 (b).

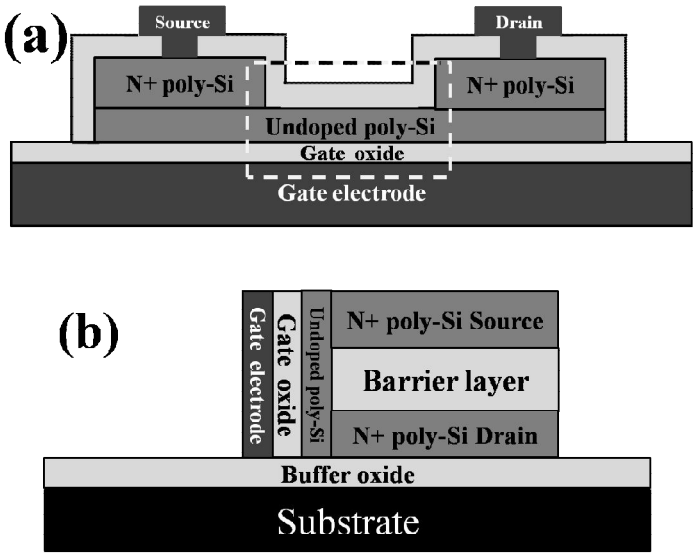


Figure 3-5: Schematic view of *(a)* the back-gate LTFT structure, and *(b)* the new VTFT structure. The new VTFT could be seen as rotating the back-gate LTFT 90°.

In order to fabricate the new VTFT, a five-mask process is carried out. Initially the same steps as the classical VTFT structure, i.e., the basic cleaning and a 500 nm buffer SiO_2 layer deposition by APCVD, are carried out. Afterwards, two heavily-doped poly-Si layers are deposited by LPCVD technique at 550°C with a barrier layer in-between. During the deposition steps, after each LPCVD deposition at 550°C and 90 Pa, a subsequent SPC step is performed at 600°C under vacuum. The schematically side view of the deposited layers'

stacking is shown in figure 3-6:

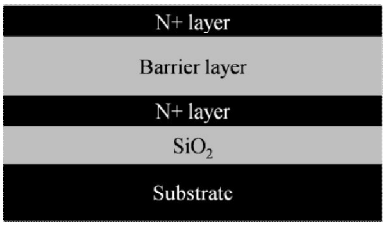


Figure 3-6: The deposition layers for the new VTFT, there is a barrier layer between two heavily-doped poly-Si layers deposited by LPCVD technique.

After the deposition steps, the first photolithography and RIE steps are implemented, the comb shape is formed, with the same geometric dimensions as the previous VTFT. After the first dry etching, the schematic views are presented in figure 3-7 (a) and figure 3-7 (b):

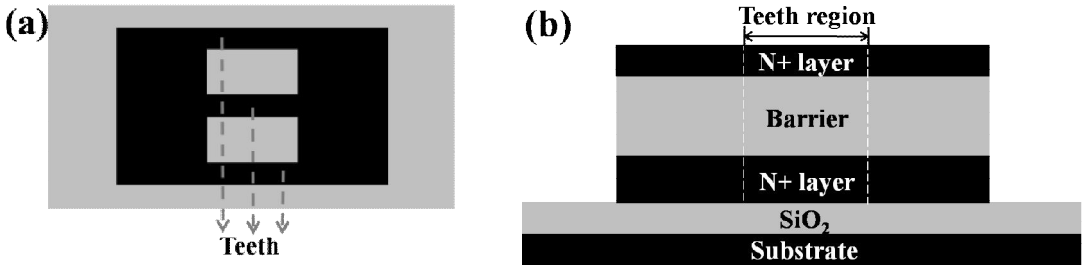


Figure 3-7: *(a)* Top view, and *(b)* side view of the new VTFT after the first RIE, the geometric dimension of the new VTFT is defined.

Then, another photolithography and RIE steps are performed to form source and drain regions, and the channel length of the VTFT is determined by the thickness of the barrier layer between source and drain. Note that, for this partial etching, the etching uniformity should be carefully controlled by the aid of the laser interferometer. The consequent schematics are presented in figure 3-8 (a) and figure 3-8 (b):

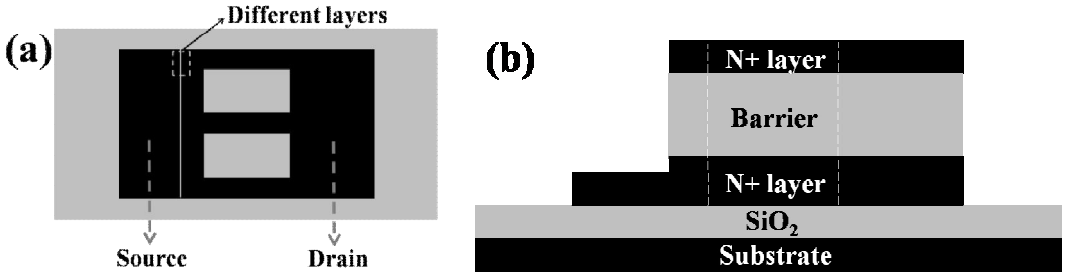


Figure 3-8: *(a)* Top view, and *(b)* side view of the new VTFT after the partial etching by the second RIE, source and drain regions could be accessed to.

Afterwards, an undoped poly-Si active layer is deposited by LPCVD technique under the same conditions and patterned by the third RIE process, which enables to form a channel on each sidewall, i.e., two channels for one tooth. Thus, the precise control of the etching endpoint for the Nid layer is essential in this etching step. The final structure after the third dry etching is presented in figure 3-9:

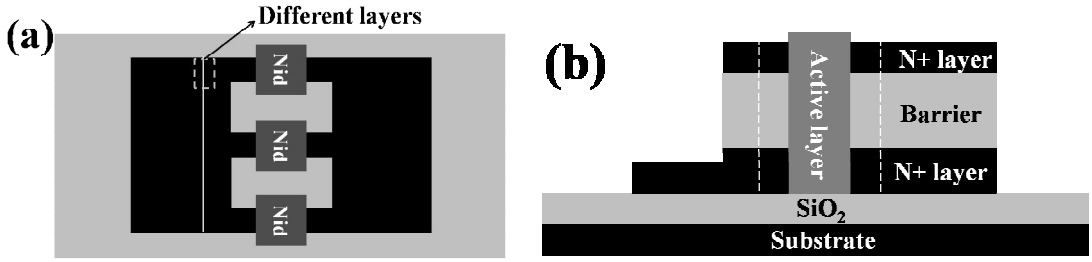


Figure 3-9: *(a)* Top view, and *(b)* side view of the new VTFT after the third RIE of the deposited active layer, which enables to form the channels on the sidewalls, "Nid" stands for the undoped (non-intentionally doped) poly-Si active layer.

After that, an essential RCA cleaning step is performed to eliminate the defects on the interface of the active layer, and thus improve the electrical characteristics of the fabricated devices. After the deposition of a gate oxide layer by APCVD at 420°C, another densification step at 600°C for 12 hours is carried out in order to eliminate most defects in the gate oxide layer. After making contact openings, the configuration of the fabricated device is shown in figure 3-10.

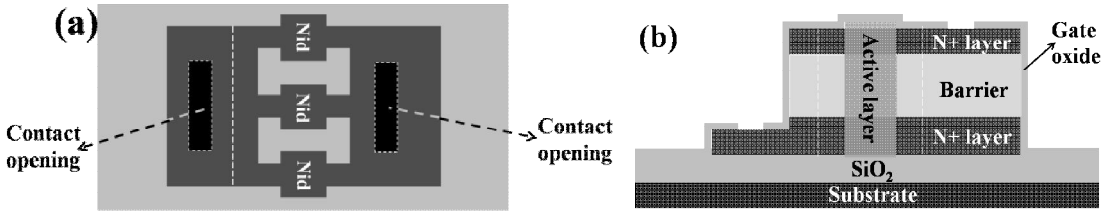


Figure 3-10: *(a)* Top view, and *(b)* side view of the new VTFT after gate oxide deposition and contact openings.

After a 400 nm Al layer deposited by Joule effect evaporation, the electrodes are defined by another wet etching step. The schematic views of the final fabricated new VTFT is presented in figure 3-11 (a) and figure 3-11 (b), and the corresponding SEM image for a four-tooth VTFT is also shown in figure 3-11 (c). The gate electrode also passes through all

the teeth at the same time, which demonstrates the multi-gate structure.

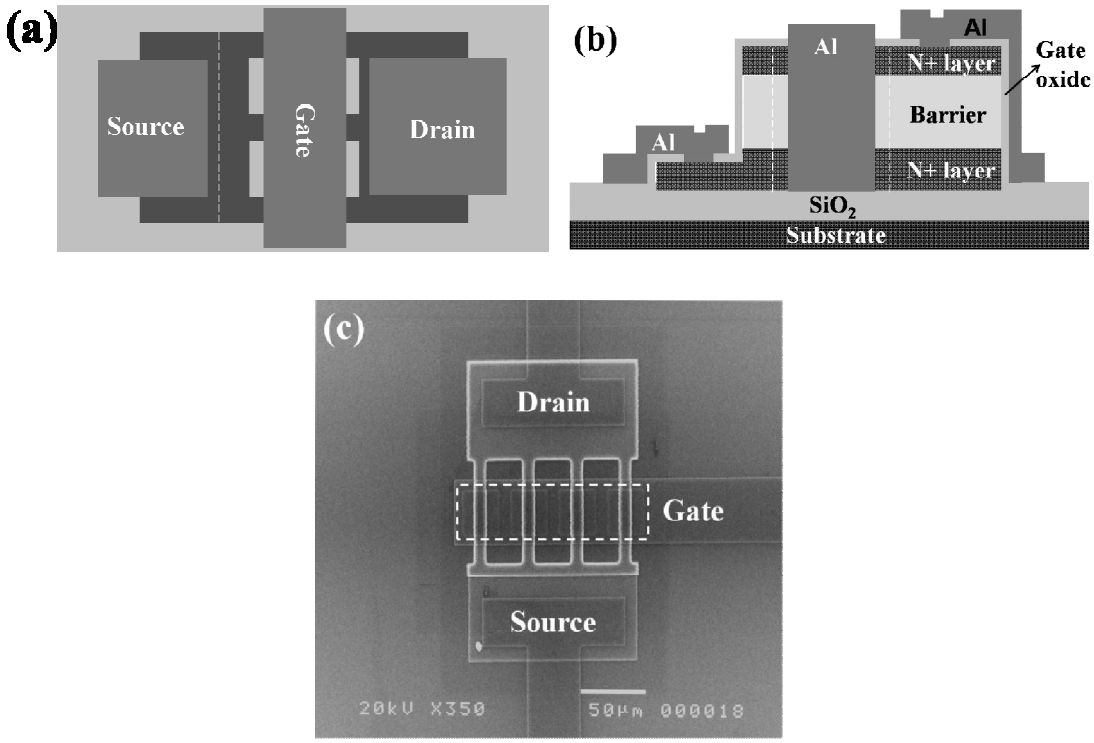


Figure 3-11: *(a)* Schematic top view, *(b)* side view of the final VTFT configuration, and *(c)* SEM top view of the fabricated four-tooth VTFT.

II.2 Geometric definition of the new VTFT

Just the same as the classical VTFT structure, the new VTFTs are defined with different geometric dimensions. The layout of a four-tooth VTFT is listed below in figure 3-12, with the key geometric parameters marked in this figure. The key geometric parameters of the VTFTs are listed below:

- L_t: the length of a tooth, which is fixed at the value of 60 µm.
- N_t: the teeth number, the optional values for N_t are 1, 2, 4.
- W_t: the width of a tooth, which has the alternative values of 10 µm and 20 µm.
- W_c: the single channel width, the optional values are 10 µm, 20 µm, and 30 µm, respectively. W_c shows obvious difference between the classical and the new VTFTs. For the classical VTFT, it is defined by the width of the gate electrode. However, for this new design, it corresponds to the width of the active layer, as shown in figure 3-12.

- *W*: the total channel width, which is defined by the formula $W = 2N_tW_c$, as there are two channels located on the two sidewalls of one tooth.

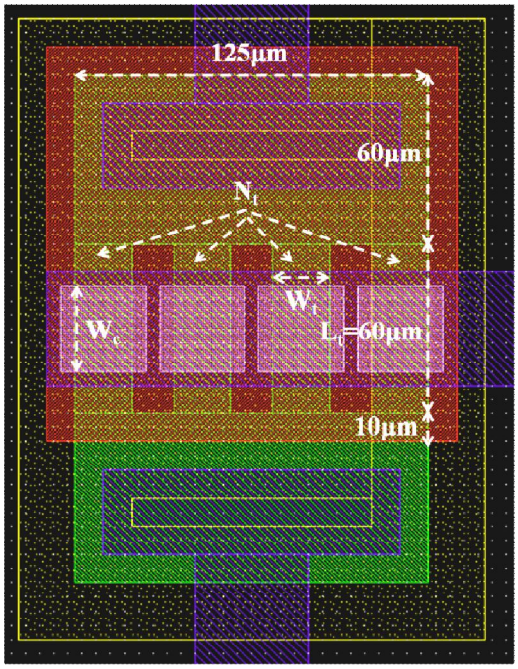


Figure 3-12: The five-mask design of a new VTFT with four teeth, different geometric parameters are marked in the figure.

There are also other geometric parameters marked in figure 3-12, such as the fixed values of 125 μm for the device width, 180 μm for the device length, and especially for the channel length *L*, it is determined by the thickness of the barrier layer between source and drain.

II.3 Key technique: barrier layer selection

For the new VTFT structure, the selection of an appropriate barrier layer between source and drain is very important for the fabrication process, as it affects the formed sidewall profile due to the etching selectivity between different materials. Initially a 400 nm SiO_2 layer is chosen as the barrier layer between source and drain, which is deposited by the APCVD technique. This high thickness is a guarantee for the isolation between source and drain. Much effort has been made to form appropriate sidewalls for the active layer and the gate oxide layer depositions, as shown in the SEM images of figure 3-13.

For figure 3-13 (a), the two poly-Si layers are etched by SF_6, while the 400 nm SiO_2 layer

is patterned by wet etching. It shows a discontinuous profile after the wet etching of the SiO_2 layer. When etching the bottom poly-Si layer, the top poly-Si layer is overetched. In addition, when the bottom poly-Si layer is overetched, the SiO_2 layer is not affected due to the high etching selectivity between poly-Si and SiO_2 layers. It is impossible to apply this discontinuous profile to the fabrication process of the new VTFT, as the active layer needs to be conformally deposited on this sidewall.

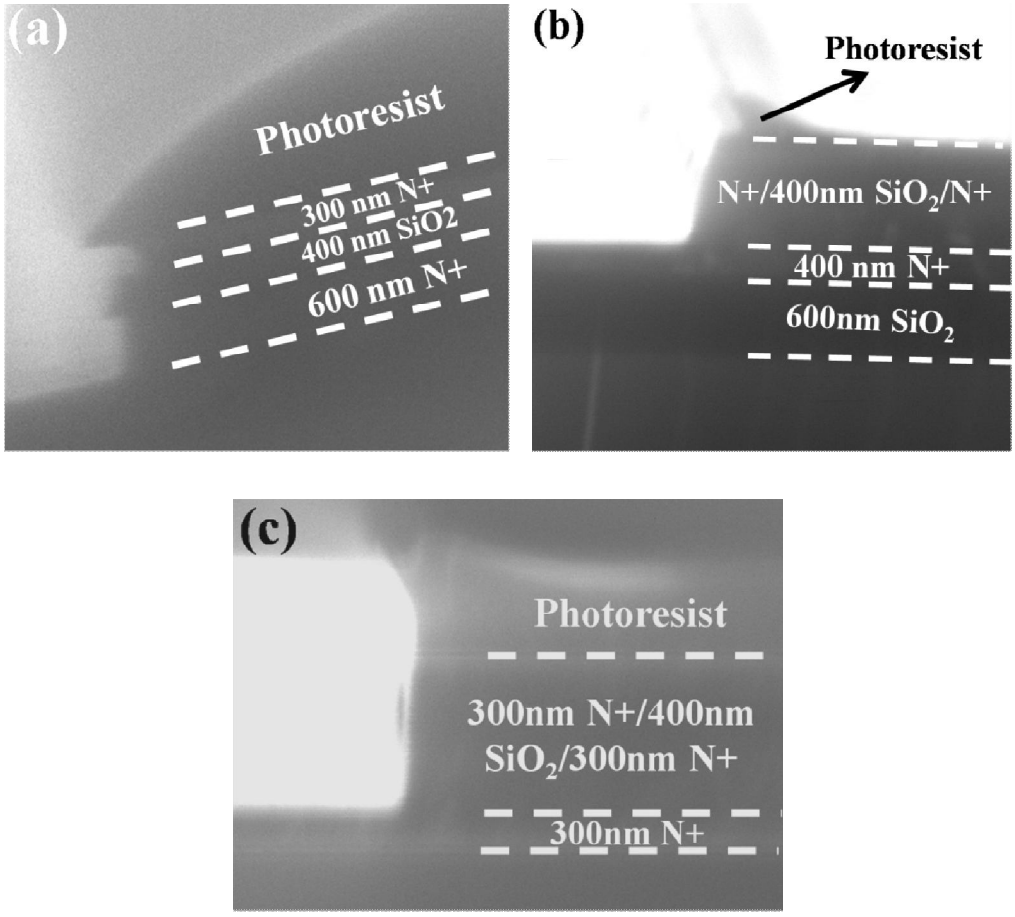


Figure 3-13: SEM images of different RIE tests for the poly-Si/400 nm SiO_2/poly-Si sidewalls. *(a)* poly-Si layers are etched by SF_6, SiO_2 layer is patterned by wet etching, *(b)* all layers are etched by CF_4, and *(c)* the top poly-Si layer are etched by SF_6, while SiO_2 and the bottom poly-Si layers are etched by CF_4.

Figure 3-13 (b) shows the sidewall profile when using CF_4 to etch all the three layers. The etching profile is continuous, which is due to the low etching selectivity between poly-Si and SiO_2 layers when using CF_4 as the etchant. However, the photoresist has been totally etched because of the long etching time, which results in the partial etching of the top poly-Si layer

(the thickness of the three layers has been reduced from 1 μm to 850 nm). This overetching also prohibits the fabrication of the new VTFTs.

Figure 3-13 (c) shows the profile formed by SF_6 and CF_4 etchants, SF_6 is used to etch the top poly-Si layer, while CF_4 is used to etch the 400 nm SiO_2 and the bottom poly-Si layers. The formed sidewall is continuous, while the layers are not overetched, which is suitable for the fabrication of the new VTFT. However, this etching condition is more complex, while the total processing time is very long.

From the three etching conditions, one conclusion could be drawn, that is, the high thickness of the SiO_2 insulating layer leads to a long etching time, and thus prohibits from forming a continuous sidewall profile. Therefore, the thickness of the SiO_2 insulating layer should be reduced. However, as the channel length L is determined by the thickness of the barrier layer between source and drain, the reduced channel length will result in serious SCEs.

The solution for this problem consists in the adoption of a thick undoped poly-Si layer and a thin SiO_2 layer as the barrier layer. The thick undoped poly-Si layer will guarantee a sufficient channel length L to minimize SCEs. The thickness of the undoped poly-Si layer is set to be 1 μm, in order to make sure that the channel length L is more than 1 μm. From previous experience of LTFT, for SiO_2 deposited by APCVD at 420°C, the breakdown voltage V_{BD} is about 0.5 V/nm. Therefore, the SiO_2 layer thickness could be reduced to 100 nm (with the V_{BD} of about 50 V), which is sufficient for ensuring the insulating property without breakdown.

III. New VTFTs based on a 100 nm SiO_2 insulating layer between source and drain

For the classical VTFT structure, the high off-current I_{OFF} is observed due to the large common overlapping area, which leads to a large leakage passing through the undoped polysilicon layer from source to drain. For the new design, by introducing an insulating layer between source and drain, the large drain-source leakage is reduced in theory.

The schematic top view of a four-tooth new VTFT is shown in figure 3-14 (a), the four teeth could provide eight channels arranged in parallel. For one tooth of the new VTFT structure, the schematic cross-sectional view is shown in figure 3-14 (b). For the first attempt, the combination of a 1 μm undoped poly-Si layer and a 100 nm SiO_2 layer is adopted as the barrier layer. For both of the source and drain regions, the thicknesses of the heavily-doped poly-Si layers are 300 nm. Note that, source and drain are not in the same plan of this schematic view. The active layer thickness T_{AC} is also 300 nm, and the gate oxide thickness T_{OX} is 100 nm, while the deposited Al thickness is about 500 nm. The thick active layer, gate oxide layer, and Al layer, are adapted to guarantee a better coverage of the gate part on the sidewall for the first attempt.

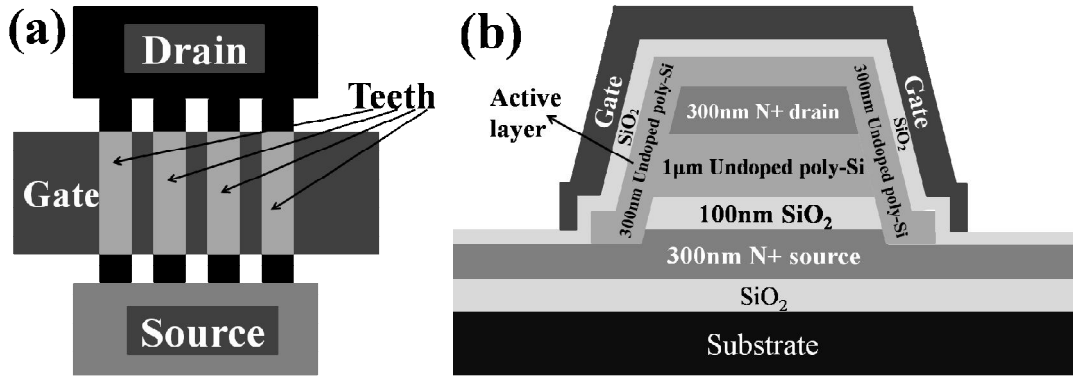


Figure 3-14: *(a)* The schematic top view of the new VTFT structure, *(b)* the schematic tooth structure for the new VTFT with a 100 nm SiO_2 insulating layer.

III.1 Technological challenge in the process - sidewall formation by RIE

Prior to the fabrication process, it is critical to form the continuous sidewall as the active layer is just deposited on it. Different RIE tests have been carried out, shown in figure 3-15. The thicknesses of the N-type heavily-doped layers (labeled as "N+") are 300 nm, while the undoped layer (labeled as "Nid") thickness is 1 μm, and the SiO_2 layer thickness is 100 nm. When etching at a low RF power (W = 20 watt, figure 3-15 (a) and figure 3-15 (b)), the etching rate is very low, and the long-time etching leads to the overetching of the photoresist. The resulted sidewall is so abrupt that it is hard to be applied for the VTFT fabrication. Therefore, the RF power should be increased.

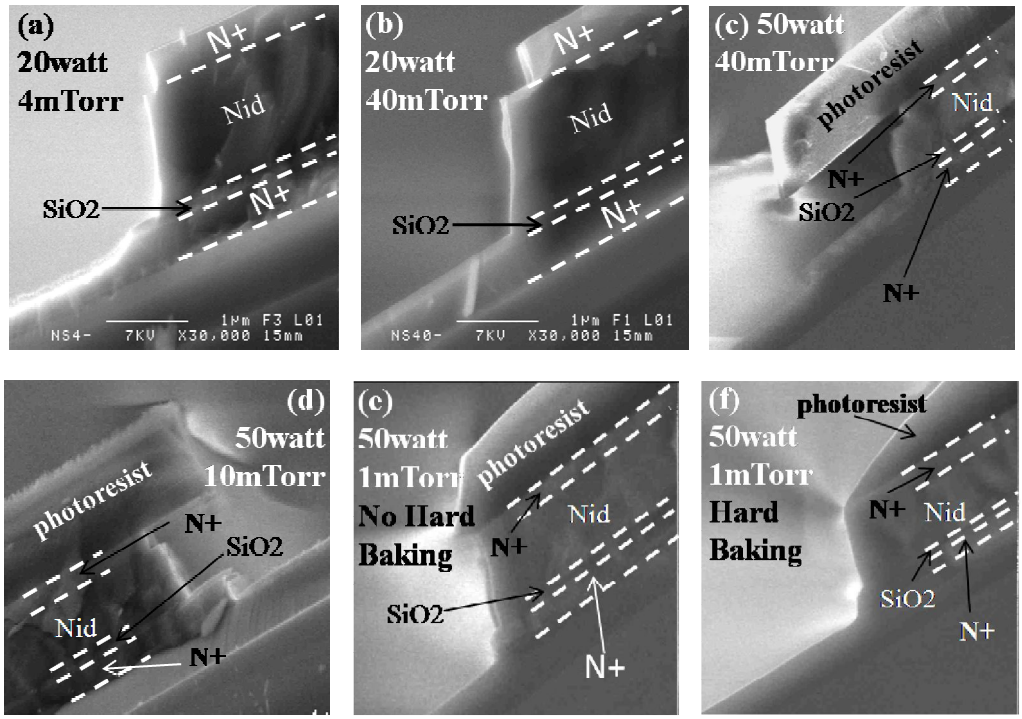


Figure 3-15: SEM image of the sidewalls by RIE under different etching conditions: *(a)* 20 watt, 4 mTorr, no photoresist is remained after etching, and *(b)* 20 watt, 40 mTorr, no photoresist is remained after etching. These two conditions cannot be applied for fabrication due to the overetching of photoresist. *(c)* 50 watt, 40 mTorr, photoresist without hard baking, and *(d)* 50 watt, 10 mTorr, photoresist without hard baking. These two conditions cannot be applied for fabrication due to the large overetching of the sidewall. *(e)* 50 watt, 1 mTorr without hard baking, and *(f)* 50 watt, 1 mTorr with hard baking. These two conditions show better sidewalls, while the sidewall is more linear after hard baking of the photoresist. The SF_6 gas flow is always set to be 10 sccm.

When etching at a high RF power (W = 50 watt, figure 3-15 (c), figure 3-15 (d), figure 3-15 (e), and figure 3-15 (f)), the photoresist remains on top of the sidewall due to the short etching time. However, when etching at a high partial pressure (figure 3-15 (c) and figure 3-15 (d)), the lateral overetching of the sidewall is very serious due to the isotropic chemical erosion. Therefore, these two conditions cannot be applied in the fabrication of the new VTFTs. When reducing the partial pressure P to 1 mTorr (figure 3-15 (e) and figure 3-15 (f)), the lateral overetching is drastically reduced, which is due to the fact that the chemical erosion effect is weakened when the partial pressure is reduced, and the physical bombardment dominates the etching process, thus the isotropy of the etching is enhanced. It also shows that the bottom heavily-doped layer is patterned by the photoresist as well as the 100 nm SiO_2

layer, the latter being a hard mask. In addition, the better continuity of the sidewall profile is obtained with a hard baking step, as the hard baking enhances the stickiness of the photoresist to the sample surface. In summary, when etching at a higher RF power *W* with a reduced partial pressure *P*, we could obtain the best sidewall profile, especially when a hard baking step is performed for the photoresist. In our fabrication process, the adopted etching parameters are: RF power $W = 50$ watt, partial pressure $P = 1$ mTorr, SF_6 gas flow $\Gamma = 10$ sccm, while the photoresist is hard baked. Even though the sidewall is continuous at this condition, there is still a change of slope at the SiO_2 layer due to the etching selectivity.

III.2 Electrical characteristics of the new structure with a 100 nm SiO_2 insulating layer

The new VTFTs are fabricated using a five-mask process. Figure 3-16 shows the etched sidewall profile before the gate part deposition. It gives evidence of a continuous sidewall, which enables a good deposition of the active layer and the gate oxide layer. The channel length *L* approximately corresponds to the total thickness of the undoped poly-Si layer (1 μm) and the SiO_2 layer (100 nm), that is, 1.1 μm, except for a 6% increase for the tilt angle of 70° (1/cos70° = 1.06).

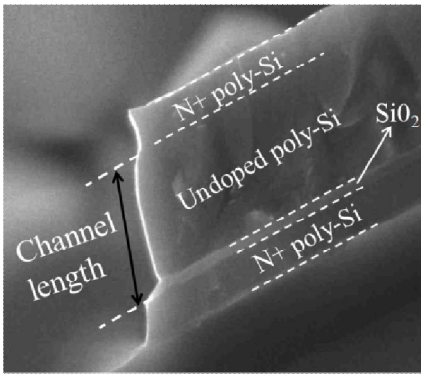


Figure 3-16: SEM image of the sidewall of the tooth after RIE.

The transfer characteristics of the new VTFT structure are shown in figure 3-17 (a). Taking into account of the design that involves several teeth, the equivalent *W/L* ratio is about 220. The transfer characteristics show a higher I_{ON}/I_{OFF} ratio that is about 3×10^4 at a lower drain-source voltage V_{DS} = 100 mV. The inset of the figure 3-17 (a) shows the gate leakage current. It is

observed that the leakage current I_{GS} is about 100 pA when the gate voltage V_{GS} = 20 V, which indicates a good coverage of the gate oxide on the sidewall. This off-current I_{OFF} is still too high, which is mainly due to the short channel length L of the device, where the current could easily pass the channel. In addition, the thick active layer also leads to a leakage current far away from the gate control, which also adds to the off-current I_{OFF}. Therefore, in order to improve the gate control, the active layer thickness T_{AC} and the gate oxide thickness T_{OX} should be reduced. Figure 3-17 (b) demonstrates the output characteristics of the fabricated VTFT, which confirms a good field effect modulation. It also shows the kink effect when V_{DS} ≥ 7 V, which is due to the impact ionization at the drain end of the channel. This SCE could be suppressed by increasing the channel length L.

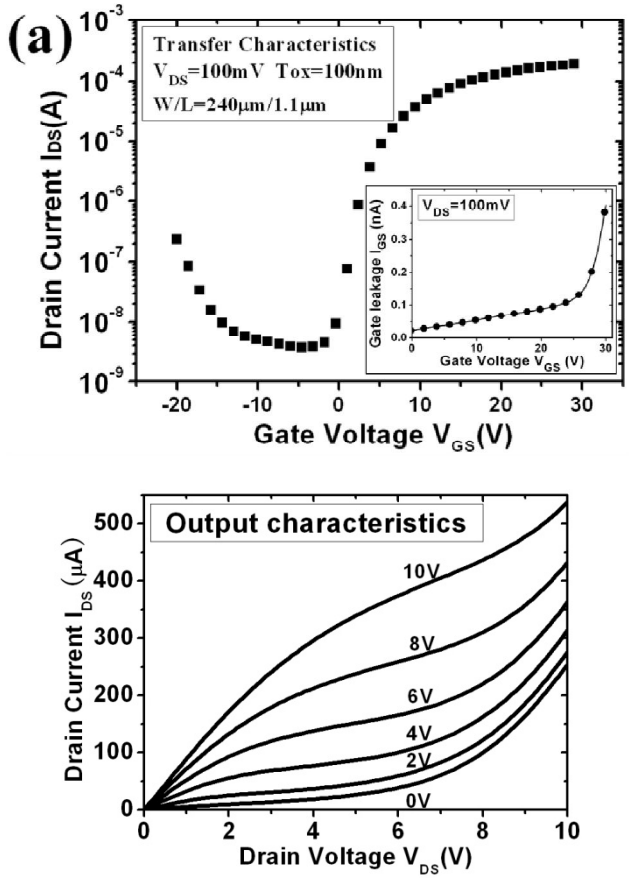


Figure 3-17: Electrical characteristics of the new VTFT involving a 100 nm SiO_2 barrier that limits the drain-source leakage current: *(a)* transfer characteristics, and *(b)* output characteristics.

The first electrical characteristics confirmed the feasibility of such a device, the first aim of

increasing the I_{ON}/I_{OFF} ratio is reached, as seen in figure 3-18, which compares the transfer characteristics of the classical (without the barrier layer) and the new VTFT (with the barrier layer). For the classical VTFT, the I_{ON}/I_{OFF} ratio is in the order of 3×10^2, in contrast, the new VTFT shows an improvement on the I_{ON}/I_{OFF}, which is in the order of 3×10^4, for the same drain-source voltage of V_{DS} = 100 mV. These curves give evidence of the change in the I_{OFF} current in comparison with the classical VTFT, which does not involve the barrier oxide layer between source and drain. The I_{OFF} current significantly decreases (divided by more than 20), that was the first goal of this work, and the on-current I_{ON} enlarges 5 times.

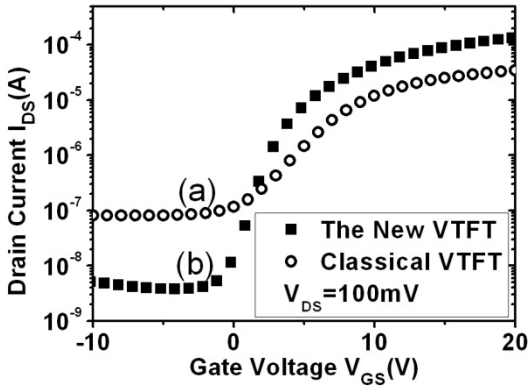


Figure 3-18: Typical transfer characteristics of the classical stacking structure ((a) without an oxide barrier) and the new structure ((b) with an oxide barrier). The first result shows a reduced off-current I_{OFF} and an increased I_{ON}/I_{OFF} ratio.

The electrical parameters of the two VTFTs are deduced from the transfer curves, which are shown in table 3-1. It is shown that for the new VTFT with a barrier layer, all the electrical characteristics have been improved, especially for the reduced threshold voltage V_{TH} and the increased mobility μ_{FE}. Therefore, the advantage of the new VTFT over the classical VTFT has also been shown.

VTFT type	V_{TH}	S	g_m	μ_{FE}
Classical VTFT	8 V	3.6 V/dec	2.7 µS	3.7 $cm^2/V\cdot s$
The New VTFT	5.4 V	1.5 V/dec	8.9 µS	11.8 $cm^2/V\cdot s$

Table 3-1: Electrical parameters for the classical and the new VTFTs with the same *W/L* ratio of 220, the parameters are deduced from the transfer curves.

III.3 Analysis of the field effect mobility

Even though we have increased the field effect mobility μ_{FE} of the VTFT, the value of 11.8 $cm^2/V{\cdot}s$ is rather low in terms of a poly-Si TFT. As mentioned in chapter 2, for the poly-Si LTFT fabricated in IETR, μ_{FE} is more than 100 $cm^2/V{\cdot}s$ [25]. Initially it is assumed that the low mobility is due to the access resistance R_{ACC} of the special comb structure. As shown in the top view of figure 3-19 (a), the access resistance R_{ACC} of source and drain regions is shown as the dashed arrows. Figure 3-19 (b) shows the corresponding schematic circuit diagram of a basic TFT, where $R_{ACC} = R_S + R_D$.

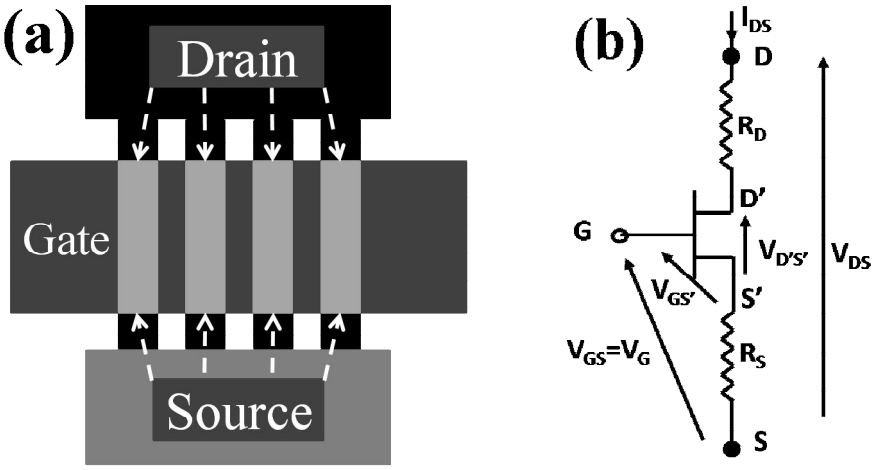


Figure 3-19: *(a)* The top view of a VTFT, where the access resistance R_{ACC} is shown as the dashed arrows, and *(b)* the schematic circuit diagram of a basic TFT.

Based on the schematic electrical diagram of a basic TFT, the drain-source resistance R_{DS} could be expressed as the following equation:

$$R_{DS} = \frac{V_{DS}}{I_{DS}} = (R_S + R_D) + (\frac{1}{\mu_{FE}^{'} C_{OX}} \frac{L}{W}) \frac{1}{V_{GS} - V_T} = R_{ACC} + X \cdot \frac{1}{V_{GS} - V_T} \qquad (eq.3-1)$$

From this equation, for the R_{DS}-$1/(V_{GS}$-$V_{TH})$ relationship, X is the slope of the linear part, the access resistance R_{ACC} and the mobility μ'_{FE} could be extracted. Note that, the extracted mobility μ'_{FE} is the mobility after eliminating the access resistance R_{ACC}. Figure 3-20 shows the R_{DS}-$1/(V_{GS}$-$V_{TH})$ curves for the classical and the new VTFTs, and table 3-2 shows the extracted R_{ACC} and μ'_{FE} values from the two curves. For the classical VTFT, the R_{ACC} is rather

large, which has greatly affected the mobility, by comparing the mobilities before and after eliminating R_{ACC} (μ_{FE} and μ'_{FE}). The large R_{ACC} is due to the fact that, except for the part under the gate control, the large overlapping area out of gate control provides the leakage passing through the undoped, resistive poly-Si layer. In contrast, for the new structure, due to the limited region of the active layer, where the current is more likely to pass the conductive heavily-doped layers (source and drain layers) instead of the undoped poly-Si layer between source and drain, the access resistance R_{ACC} is also reduced. Therefore, for the new VTFT, the mobility μ_{FE} is almost not affected by the access resistance R_{ACC}.

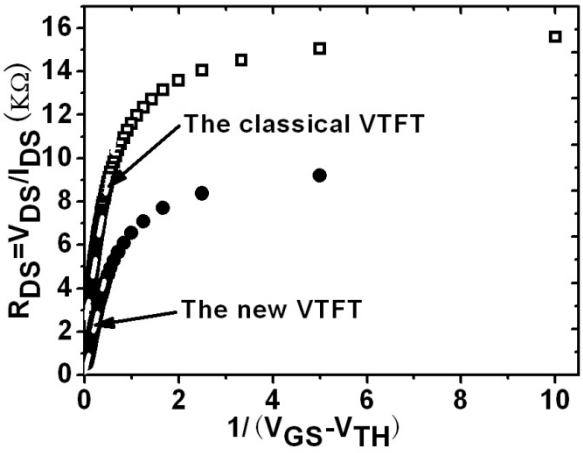


Figure 3-20: The relationship of R_{DS} and the $1/(V_{GS}- V_{TH})$, the access resistances R_{ACC} and the mobilities μ'_{FE} could be extracted.

VTFT type	R_{ACC}	μ_{FE} with R_{ACC}	μ'_{FE} without R_{ACC}
Classical VTFT	2140 Ω	3.7 $cm^2/V{\cdot}s$	11.3 $cm^2/V{\cdot}s$
The New VTFT	56 Ω	11.8 $cm^2/V{\cdot}s$	12.9 $cm^2/V{\cdot}s$

Table 3-2: The access resistance R_{ACC} and the mobility μ'_{FE} deduced from the R_{DS}-$1/(V_{GS}-V_{TH})$ curves, the mobility μ_{FE} deduced from the transfer curves is also shown.

Therefore, for the new VTFT, the low mobility μ_{FE} is more likely to be affected by the active layer quality deposited on the sidewall. There are two possibilities, one possibility is that, as the crystallization of the channel layer starts from the interface between the sidewall and the deposited layer, the high roughness of the lateral relief for the sidewall caused by the dry etching could lead to the formation of a lot of seed sites, which result in the presence of

small grain sizes and more grain boundaries. As a result, these grain boundaries work as the defects in the active layer, which greatly affect the mobility μ_{FE}. The other possibility is that, as there is a change of the sidewall slope at the insulating layer (100 nm SiO_2 layer in this process) due to the etching selectivity, the crystallization of the active layer could also be affected. In fact, the morphology of the active layer on the vertical sidewalls is still unknown, which needs to be further studied. In order to further increase the mobility μ_{FE}, the roughness of the sidewalls should also be reduced, which also helps to decrease the subthreshold slope *S* as well as the leakage current.

III.4 Technological problem in the process – "shadow effect" in Al deposition

Due to the special geometry of the VTFT, Al layer should be deposited on the vertical sidewall, and the thickness of the vertical sidewall could be more than 1 μm. Using Joule effect evaporation for Al deposition, a "shadow effect" can be resulted in due to this special deposition technique. As a result, sometimes, on one side of the sidewall, there is Al deposited on the sidewall, while for the other side, there is no Al deposited on the sidewall. A typical SEM image of the "shadow effect" is shown in figure 3-21. For gate electrode deposited by this method, the shadow effect will result in the disabled teeth that are out of gate control.

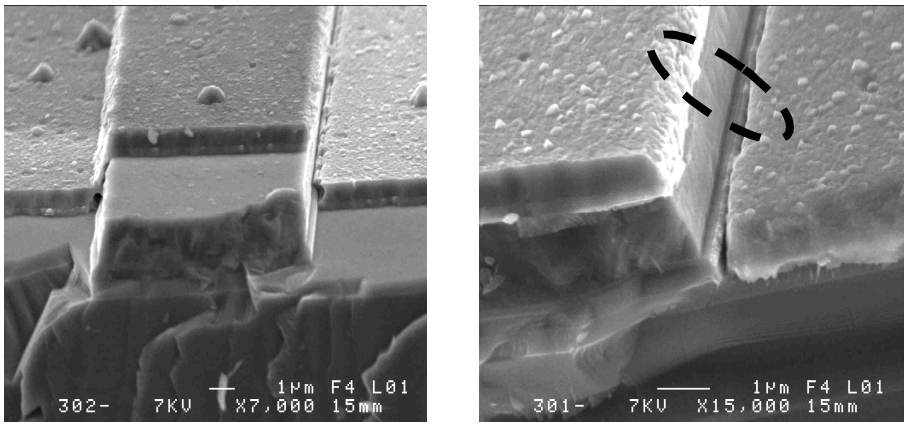


Figure 3-21: *(a)* Al deposition on the two sidewalls, the left sidewall has a good Al coverage, while the right sidewall shows no Al deposited on the sidewall, *(b)* the enlarged image of the right sidewall, and "shadow effect" is obviously shown.

The solution lies in the reduction of the sidewall steepness, by adopting a quasi-vertical sidewall. In addition, the deposited thickness of Al should be increased in order to guarantee a sufficient Al thickness on the sidewall, due to the thinner Al thickness on the sidewall compared with the thickness on the planar surface. By different comparison tests for Al depositions, the continuous Al deposition on the sidewall has been obtained that enables the fabrication of the new VTFTs.

IV. New VTFTs based on a 200 nm Si_3N_4 insulating layer between source and drain

As mentioned above, for the new VTFTs using a 100 nm SiO_2 insulating layer between source and drain, the change of the sidewall slope due to the etching selectivity between the poly-Si layers and the SiO_2 layer, limits the electrical characteristics of the fabricated VTFT. Therefore, another attempt by using Si_3N_4 as the insulating layer is also carried out, which is deposited at 600°C by LPCVD technique. In this process, the thicknesses of the poly-Si layers in the stacking are the same as the one using SiO_2 as the insulating layer, while the adopted thickness of the Si_3N_4 insulating layer is 200 nm. The choice of adopting a 200 nm Si_3N_4 insulating layer, in comparison with a 100 nm SiO_2 insulating layer, is to keep the nearly same capacitance, considering the different relative dielectric constants (3.9 for SiO_2, and 7.5 for Si_3N_4). The other consideration for a thicker Si_3N_4 layer lies in the guarantee of the insulating properties for the Si_3N_4 layer deposited at 600°C, whose ideal deposition temperature is between 650°C to 850°C [96]. The adopted active layer thickness T_{AC} is 300 nm, which is the same value as the previous structure using a SiO_2 insulating layer. The schematic tooth structure is shown in figure 3-22, the barrier layer between source and drain is made up of a 1μm undoped poly-Si layer and a 200 nm Si_3N_4 layer. The channel length L is the total thickness of the undoped poly-Si layer and the Si_3N_4 insulating layer, which is 1.2 μm, except for a little increase due to the tilt angle. The channel length L of this VTFT is comparable to the previous VTFT with a 100 nm SiO_2 insulating layer.

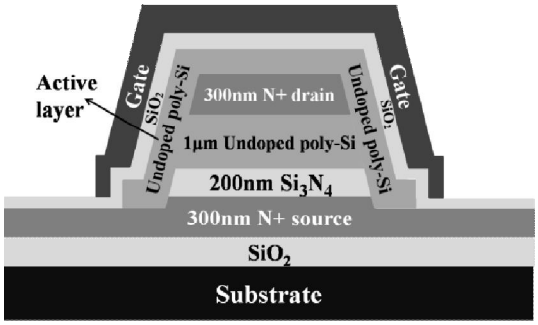
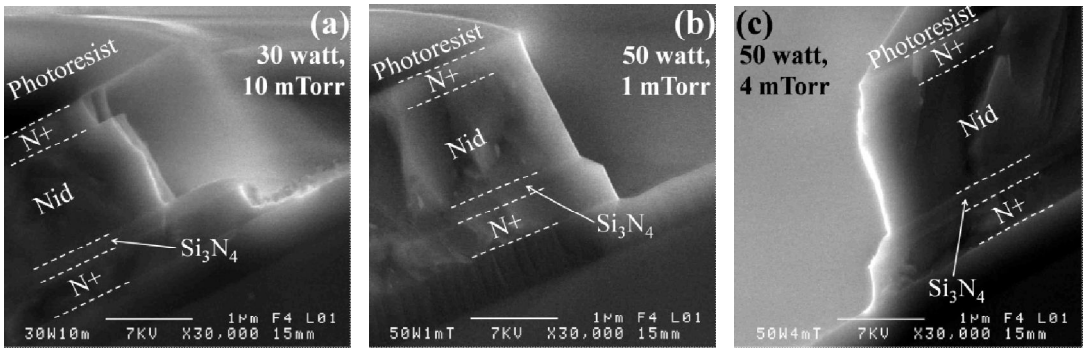


Figure 3-22: Schematic tooth structure for the new VTFT with a 200 nm Si_3N_4 insulating layer.

IV.1) Technological challenges in the process – sidewall formation by RIE

Just the same as the fabrication process of VTFTs with a 100 nm SiO_2 insulating layer, different etching tests for a sidewall with a 200 nm Si_3N_4 insulating layer are also carried out prior to the fabrication process, shown in figure 3-23. Comparing figure 3-23 (a) and 3-23 (d), when etching at the same partial pressure of 10 mTorr, the higher RF power leads to a better sidewall due to that the increase of the physical bombardment reduces the lateral overetching. The same trend is obtained from figure 3-23 (b) to figure 3-23 (e), that is, for the etching at a higher RF power W, when increasing the partial pressure P of the etching gas, the chemical erosion is more obvious, which leads to a more serious lateral overetching under the photoresist. All these conclusions are the same as the previous tests for the VTFT with the 100 nm SiO_2 insulating layer. Figure 3-23 (b) (W = 50 watt, P = 1 mTorr) shows the best sidewall, the quite vertical profile is obtained, even though there is a transition between the poly-Si layers and the Si_3N_4 layer due to the etching selectivity of the two materials. Therefore, in our fabrication process, the adopted parameters are RF power W = 50 watt, partial pressure P = 1 mTorr, while SF_6 gas flow Γ = 10 sccm.



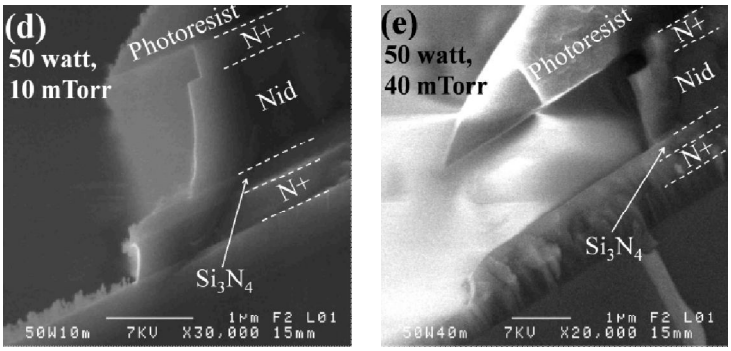


Figure 3-23: SEM image of the sidewalls by RIE under different etching conditions: *(a)* 30 watt, 10 mTorr; *(b)* 50 watt, 1 mTorr; *(c)* 50 watt, 4 mTorr; *(d)* 50 watt, 10 mTorr; *(e)* 50 watt 40 mTorr. For the conditions of *(a)*, *(d)*, *(e)*, they cannot be applied for the VTFTs fabrication due to the large lateral overetching. For the conditions of *(b)* and *(c)*, the former shows a much better sidewall. The SF_6 gas flow is always set to be 10 sccm.

IV.2) Electrical characteristics in comparison with the VTFTs with a SiO_2 insulating layer

The new VTFTs are still fabricated via a five-mask process. Figure 3-24 shows a more linear sidewall than the one with a SiO_2 insulating layer, which is due to the lower etching selectivity between poly-Si and LPCVD Si_3N_4.

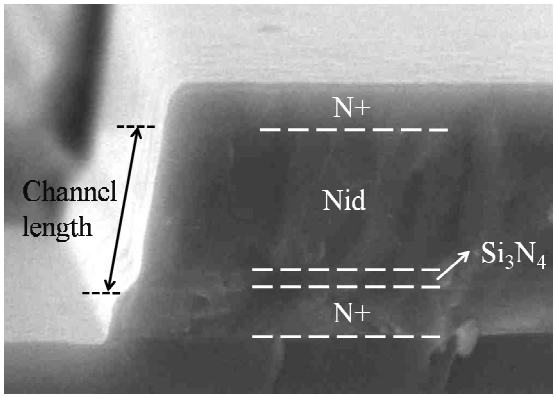


Figure 3-24: SEM image of the etched sidewall for the new VTFT with a 200 nm Si_3N_4 insulating layer.

The electrical characteristics of the fabricated VTFT based on the 200 nm Si_3N_4 insulating layer are shown in figure 3-25. Figure 3-25 (a) shows the transfer characteristics before and after the forming gas treatment, the adopted drain-source voltage V_{DS} is 100 mV, the channel width/length ratio W/L is 200 for the total channel width W = 240 μm, and the active layer thickness T_{AC} equals to 300 nm. From the transfer curves, an I_{ON}/I_{OFF} ratio of almost 10^5 is

gained before the forming gas treatment. However, after the forming gas treatment, the off-current I_{OFF} has increased about two orders of magnitude, which reduces the I_{ON}/I_{OFF} ratio to be in the order of 10^3. The instability of the electrical characteristics confirms the poor insulating properties of Si_3N_4 deposited by LPCVD at 600°C. Figure 3-25 (b) shows the output characteristics of the VTFT, the field effect modulation is observed, while the kink effect is still shown. However, this VTFT shows better saturation in comparison with the VTFT with a SiO_2 insulating layer, and the kink effect is observed until when the drain voltage V_{DS} is higher than 10 V.

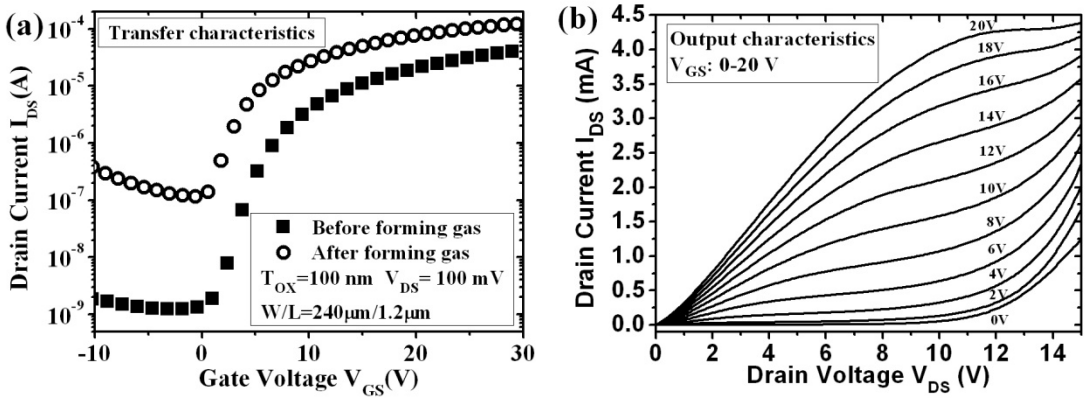


Figure 3-25: *(a)* Transfer characteristics before and after forming gas, an I_{ON}/I_{OFF} ratio of almost 10^5 is shown before the forming gas treatment, and *(b)* output characteristics of the new VTFT structure, better saturation is obtained.

Figure 3-26 shows the electrical characteristics comparison between the new VTFT structures (the VTFT with the SiO_2 insulating layer and the one with the Si_3N_4 insulating layer), when the drain voltage V_{DS} = 100 mV. For the two structures, they show the same I_{ON}/I_{OFF} ratio of almost 10^5 for the same W/L ratio of 200. However, for the VTFT with the Si_3N_4 insulating layer, I_{ON} reduces 3 times as well as I_{OFF}.

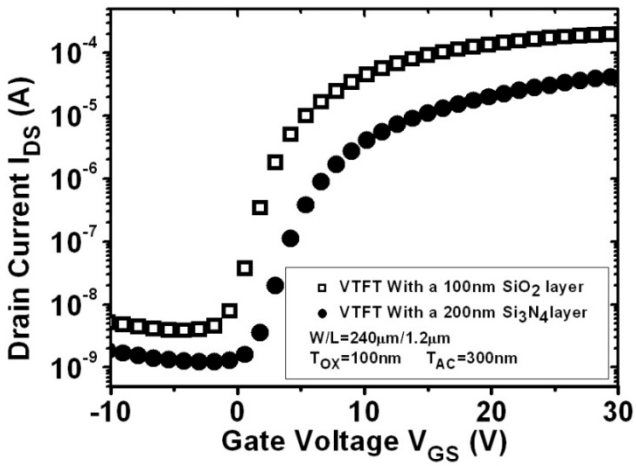


Figure 3-26: Transfer characteristics comparison between the new VTFTs with different insulating layers.

Different electrical parameters for the two VTFTs are deduced and shown in table 3-3. Still due to the high roughness of the sidewall caused by the RIE process, the low mobility μ_{FE} and high subthreshold slope S are observed, as the active layer is just deposited on the sidewalls. In addition, the crystallization quality of the deposited polysilicon active layer on the sidewall is still unknown. Nevertheless, all electrical parameters have already shown a much better electrical property for the VTFT with a 100 nm SiO_2 insulating layer, especially for the higher field effect mobility μ_{FE}, and a lower threshold slope V_{TH}. The worse parameters for the Si_3N_4 insulating layer, should be due to the worse insulating quality of the Si_3N_4 layer deposited by LPCVD at 600°C. Note that, the thickness of the Si_3N_4 insulating layer has already been twice of the SiO_2 insulating layer, which further indicates the worse insulating quality of the Si_3N_4 limited by the low-temperature process. Therefore, for the new VTFTs fabricated afterwards, the SiO_2 insulating layer will always be adopted.

Insulating layer	S (V/dec)	V_{TH} (V)	g_m (μS)	μ_{FE} ($cm^2/V{\cdot}s$)
100 nm SiO_2	1.5	5.2	9.2	12.2
200 nm Si_3N_4	1.64	8.5	1.7	2.3

Table 3-3: Electrical parameters comparison between the two VTFTs with different insulating layers, when V_{DS} = 100 mV.

IV.3) The effect of geometric parameters on the electrical characteristics

For this process, better reproducibility of the fabricated VTFTs has been obtained, by avoiding the Al deposition problem of the previous process. Therefore, for the new VTFTs, the relationships between the electrical characteristics and the geometric parameters could also been obtained. Figure 3-27 (a) and 3-27 (b) show the relationships of the on-current I_{ON} with the teeth number N_t and the single channel width W_c, respectively. As expected, the on-current I_{ON} is proportional to the teeth number N_t, as I_{ON} is related with the channel numbers (there are two channels for each tooth). In contrast, I_{ON} is independent of the single channel width W_c. This is assumed that for the new VTFT, the efficient single channel width W'_c is less than W_c, the current path is more likely to be determined by W'_c instead by W_c, as shown in figure 3-27 (c). For VTFTs with different single channel width W_c, the efficient single channel width W'_c is almost the same.

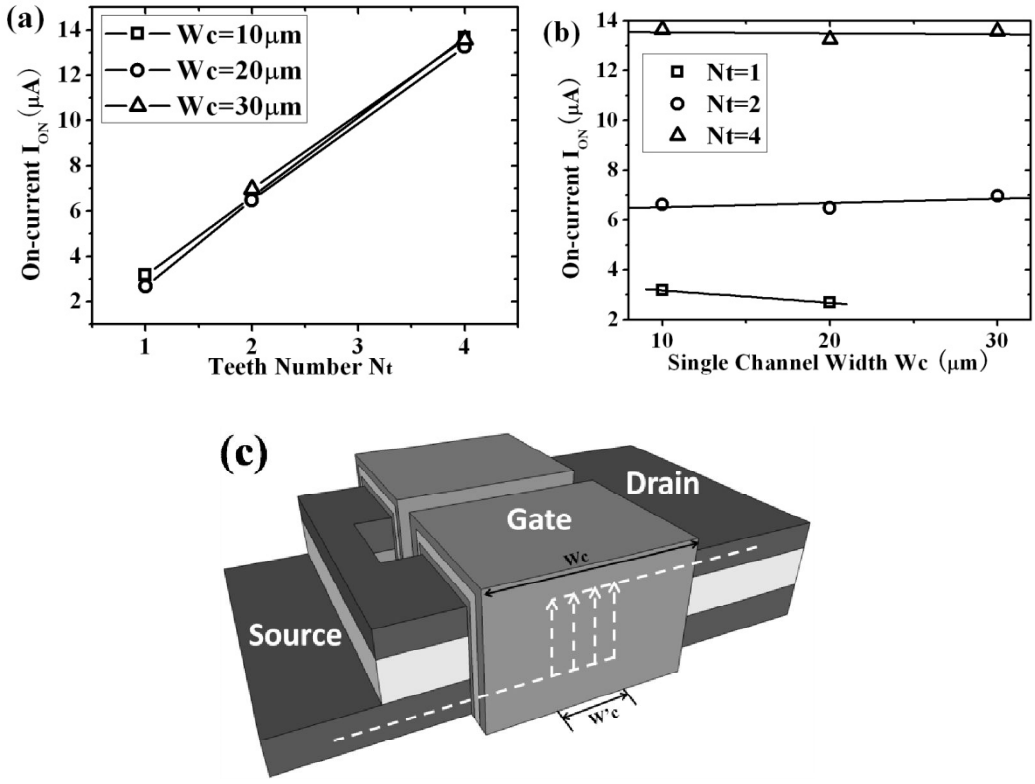


Figure 3-27: On-current I_{ON} relationship with *(a)* teeth number N_t, *(b)* single channel width W_c. The on-current is proportional to N_t, while it is independent of W_c, and *(c)* the efficient current path for the new VTFT, where the efficient single channel width W'_c is marked.

The off-current I_{OFF} relationships with the teeth number N_t and the single channel width W_c are shown in figure 3-28. As expected, I_{OFF} is proportional to N_t as well as W_c, which is due to that I_{OFF} is directly related with the active layer area. Further study about the effect of geometric parameters on the electrical characteristics will be given in detail afterwards.

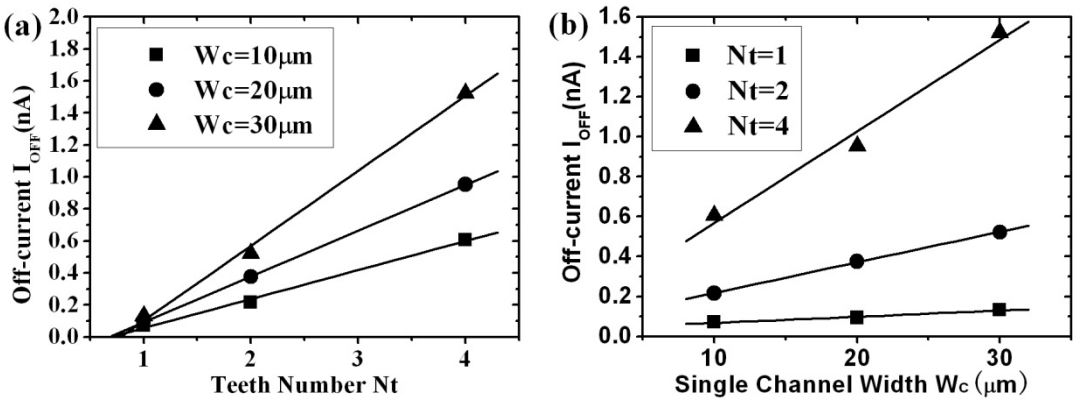


Figure 3-28: *(a)* Off-current I_{OFF} relationship with teeth number N_t, and *(b)* Off-current I_{OFF} relationship with single channel width W_c.

V. New VTFTs with different active layers

Based on the experience of the previous processes, several conclusions and improvements could be made:

1) For the same active layer thickness T_{AC} of 300 nm, VTFT fabricated with a 100 nm SiO_2 insulating layer by APCVD at 420°C shows better electrical characteristics than the one fabricated with a 200 nm Si_3N_4 insulating layer by LPCVD at 600°C, thus VTFTs will always be fabricated using a SiO_2 insulating layer.

2) From the SEM observation, APCVD is a conformal deposition, of which a 70 nm SiO_2 layer should be enough for gate oxide utilization.

3) Considering the risk of overetching the top and bottom heavily-doped poly-Si layers when etching the active layer, which could also reduce the reproducibility of the fabrication process, the thickness of the top and bottom heavily-doped layers should be increased.

For the new VTFT, the active layer is deposited after the formation of the sidewall, thus different active layers could be obtained with the nearly same sidewall profile in the same run.

Therefore, this new structure provides a flexible way to improve the electrical characteristics by adopting different active layers, which is another advantage of the new structure. On one hand, the different active layer thicknesses may affect the VTFT characteristics. On the other hand, the active layer deposited from SiH_4 precursor gas is always adopted, while the active layer deposited from Si_2H_6 precursor gas has never been tried. For LTFTs, the poly-Si deposited from Si_2H_6 precursor gas has been proved to have a large grain size than the one from SiH_4 precursor gas, which is beneficial for the electrical characteristics [86]. In this process, different active layer thicknesses T_{AC} using SiH_4 precursor gas are attempted (225 nm, 150 nm, 100 nm), and a 150 nm active layer using Si_2H_6 precursor gas is also tried. The VTFT structure is still based on a 100 nm SiO_2 insulating layer, as shown in figure 3-14 (b). Note that, the gate oxide thickness T_{OX} has reduced to 70 nm, while the thickness of the top and bottom heavily-doped poly-Si layers has increased to 400 nm and 600 nm, respectively.

Figure 3-29 shows the transfer characteristics for different active layers. For different active layer thickness T_{AC}, nearly the same ratio of more than 10^5 is obtained for a drain-source voltage V_{DS} = 100 mV, which is higher than the ratio obtained from the first process when the active layer thickness is 300 nm (the corresponding ratio is about 3×10^4). This indicates the efficient increase of the I_{ON}/I_{OFF} ratio by reducing the active layer thickness. Table 3-4 shows the electrical parameters deduced from the transfer characteristics of different active layers. For VTFTs using SiH_4 precursor gas, when increasing the active layer thickness T_{AC}, the lower threshold voltage V_{TH}, and the higher field effect mobility μ_{FE} are obtained, which is due to the larger crystal sizes of the active layer deposited on the sidewall when increasing the active layer thickness T_{AC}. For VTFTs deposited from different precursor gases (SiH_4 and Si_2H_6), all electrical parameters show the advantage of SiH_4 precursor gas over Si_2H_6 precursor gas, which is contrary to the previous conclusions based on the poly-Si LTFTs in reference [86].

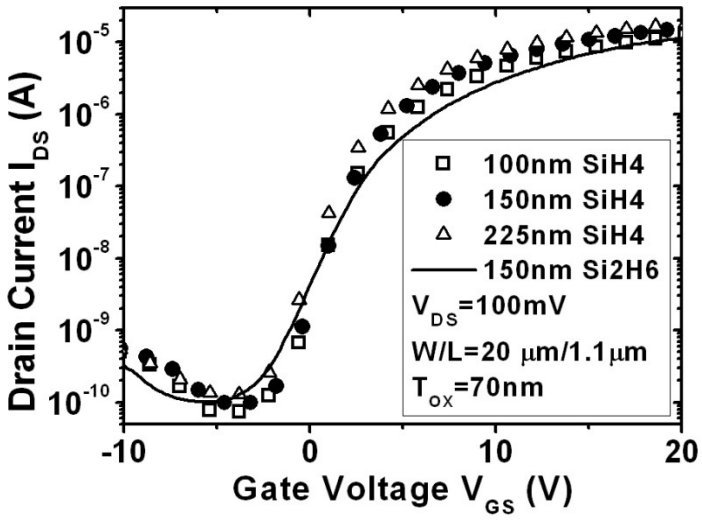


Figure 3-29: Transfer characteristics for different active layers.

Active layer	S (V/dec)	g_m (μS)	V_{TH} (V)	μ_{FE} (cm^2/V·s)	I_{ON}/I_{OFF}
SiH_4 225 nm	1.3	1.2	3.9	13.2	1.74×10^5
SiH_4 150 nm	1.3	1.0	4.4	11.5	1.98×10^5
SiH_4 100 nm	1.2	0.8	5	9.2	2.11×10^5
Si_2H_6 150 nm	1.8	0.9	7.6	10.5	1.32×10^5

Table 3-4: Electrical parameters of VTFTs with different active layers.

Figure 3-30 (a) - (c) shows the relationships of on-current I_{ON}, off-current I_{OFF}, and on/off-current ratio I_{ON}/I_{OFF} with different active layers. For I_{ON} and I_{OFF}, they show the same trend, that is, both I_{ON} and I_{OFF} increase with the active layer thickness T_{AC}. It is due to that when T_{AC} increases, the grain size of the poly-Si crystallized on the sidewall should also enlarge, which helps to increase I_{ON}. In addition, I_{OFF} decreases with the reduction of the active layer thickness T_{AC}, which is due to the better gate control when reducing T_{AC}, as the active layer part far away from the gate control is decreased. Figure 3-30 (c) shows that it is efficient to increase I_{ON}/I_{OFF} by reducing the active layer thickness T_{AC}. From the three figures, the VTFT based on the active layer deposited from Si_2H_6 precursor gas shows a lower I_{ON} and a higher I_{OFF} in comparison with their counterpart VTFT, whose active layer is deposited from SiH_4 precursor gas, and thus the VTFT from Si_2H_6 precursor gas obtain a lower I_{ON}/I_{OFF} ratio. It is also contrary to the previous conclusions based on the poly-Si LTFTs [86]. The crystallization mechanism on the vertical sidewall is still unknown, and we could only conclude that the poly-Si quality crystallized on the sidewall from Si_2H_6 precursor gas is not so ideal in comparison with SiH_4

precursor gas.

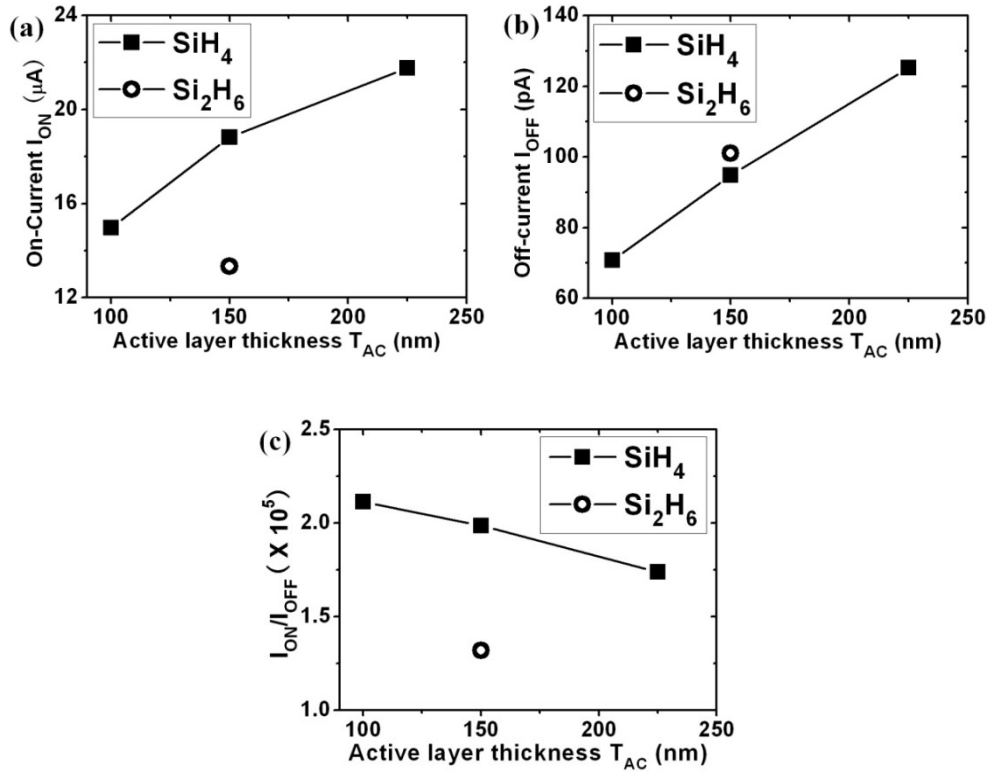


Figure 3-30: *(a)* On-current I_{ON}, *(b)* off-current I_{OFF}, and *(c)* I_{ON}/I_{OFF} relationships with different active layers.

From the analysis shown above, with the increase of the active layer thickness T_{AC}, I_{ON}/I_{OFF} ratio reduces a little, while the field effect mobility μ_{FE} increases a little. Nevertheless, the nearly same I_{ON}/I_{OFF} ratio of more than 10^5 and field effect mobility μ_{FE} in the order of 10 $cm^2/V{\cdot}s$ have been obtained. However, the VTFTs with an active layer thickness of 100 nm tend to degrade. Therefore, the active layer thickness T_{AC} of 150 nm is adopted for the new VTFTs fabrications afterwards, as a compromise between the I_{ON}/I_{OFF} ratio and the mobility μ_{FE}.

VI. P and N-type VTFTs

Due to the advantage of the *in situ* doping during the LPCVD process, P and N-type VTFTs could be easily fabricated in the same run, just by adopting different dopant gases (PH_3 or B_2H_6) for source and drain regions. In order to have a basic study on the electrical characteristics of P and N-type VTFTs, P and N-type VTFTs have been fabricated, based on the previous study on

the $VTFT_S$. The active layer thickness has been chosen as 150 nm, and the other geometric dimensions are the same as the previous process. The schematic view of a basic tooth (P and N-type) is shown in figure 3-31:

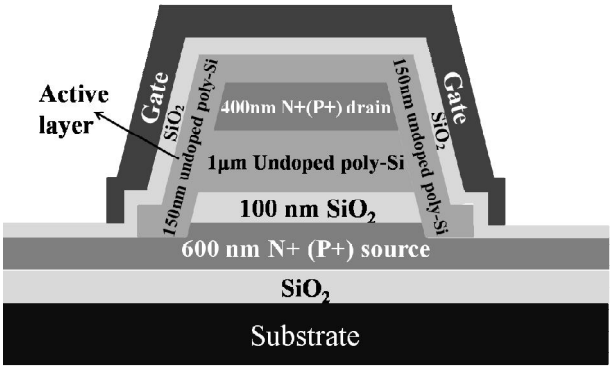


Figure 3-31: Schematic view of a basic tooth for the N(P)-type VTFT, a 100 nm SiO_2 insulating layer is adopted, the top and bottom heavily-doped layers are 400 nm and 600 nm, respectively, the active layer thickness T_{AC} is 150 nm, while the gate oxide thickness T_{OX} is 70 nm.

VI.1 Electrical characteristics of P and N-type VTFTs

The typical transfer characteristics of the P and N-type VTFTs are shown in figure 3-32 (a), with the same W/L = 80 μm/1.1 μm. The I_{ON}/I_{OFF} ratio of about 10^5 is obtained for both P and N-type VTFTs, and the two types of VTFTs also show symmetric I_{ON} and I_{OFF}, which demonstrates the feasibility for CMOS-like VTFT circuit applications as inverters or oscillators. For V_{DS} = 100 mV, the deduced electrical parameters are listed below in table 3-5. The same subthreshold slope S of 1.5 V/dec is obtained for both P and N-type VTFTs. For P-type VTFT, the field effect mobility μ_{FE} = 4.2 cm^2/V.s, while the threshold voltage V_{TH} = -15 V. For N-type VTFT, μ_{FE} = 7.5 cm^2/V.s, while V_{TH} = 9.8V. Note that, for P and N-type VTFTs, the off-currents are obtained when gate voltage V_{GS} are about -3 V instead of 0 V, this is due to that the non-intentionally doped (Nid) active layer is lightly N-type doped (polysilicon structural defects), which reduces V_{TH} for N-type VTFT while increasing V_{TH} for P-type VTFT. The low mobility μ_{FE} and high threshold slope S are due to the high roughness of the sidewalls caused by the long-time RIE. In fact, for this process, a lower field effect mobility μ_{FE} = 7.5 cm^2/V·s and a higher threshold voltage V_{TH} = 9.8 V have been obtained, in comparison with the previous process on the study of different active layer layers (whose field effect mobility μ_{FE} = 11.5

$cm^2/V{\cdot}s$, and threshold voltage V_{TH} = 4.4 V). This could be due to the higher roughness of the sidewall in this process, in comparison with the previous one. In addition, the morphology of poly-Si active layer crystallized on the sidewalls is still unknown, which may also affect the electrical parameters. Nevertheless, in the same process, the symmetric electrical characteristics have been shown.

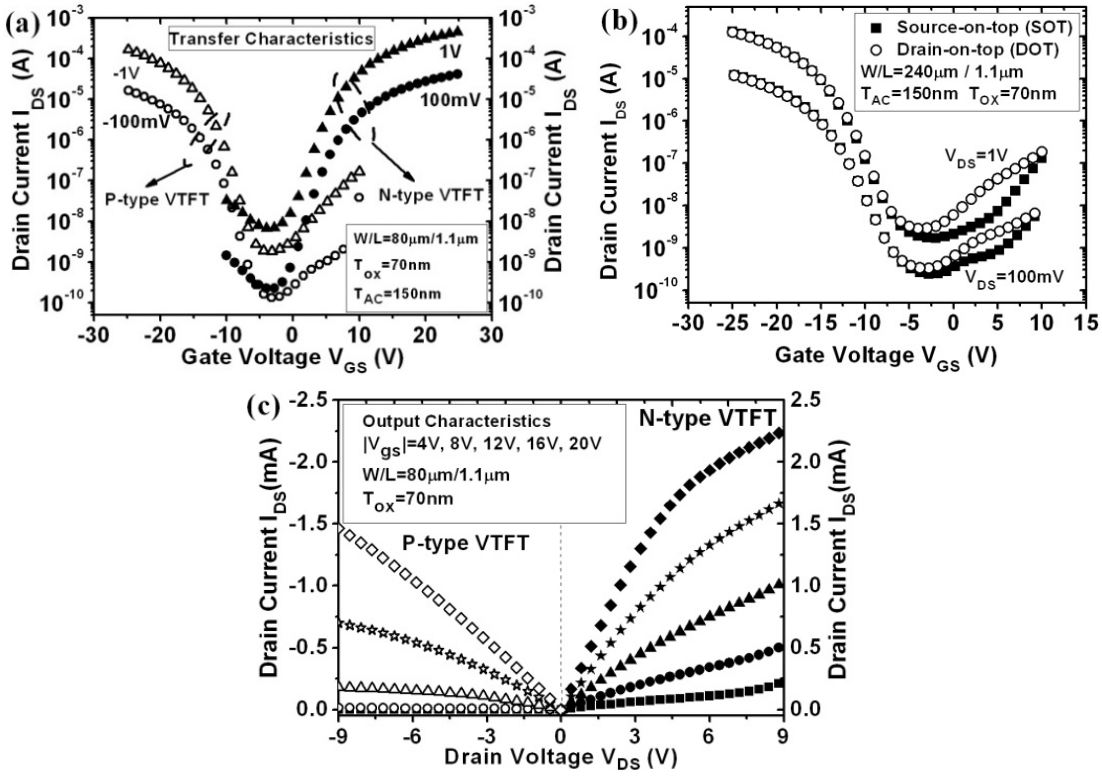


Figure 3-32: *(a)* Transfer characteristics of the P and N-type VTFTs, (b) transfer characteristics for source-on-top (SOT) and drain-on-top (DOT) structure, and *(c)* output characteristics of the P and N-type VTFTs.

VTFT type	S (V/dec)	V_{TH} (V)	g_m (μS)	μ_{FE} ($cm^2/V{\cdot}s$)
P-type	1.9	-15	1.5	4.2
N-type	1.9	9.8	2.7	7.5

Table 3-5: Electrical parameters of P and N-type VTFTs.

Figure 3-32 (b) shows the similar transfer characteristics of the source-on-top (SOT) and the drain-on-top (DOT), which indicates the symmetry in the structure, especially the similar interface between the heavily-doped layer (source/drain layer) and the undoped active layer. Figure 3-32 (c) shows the output characteristics of the fabricated VTFTs, the kink effect prohibits the saturation of the drain current, which could be suppressed by increasing the

channel length L and improving the crystalline quality of the active layer on the sidewalls. Nevertheless, the feasibility of the complementary VTFTs has been demonstrated, which enables CMOS-like applications as inverters or oscillators.

VI.2 The Effect of geometric parameters on the electrical characteristics

VI.2.1 P-type VTFT

For P-type VTFTs, the electrical characteristics are analyzed in function of different dimensions. For the on-current I_{ON}, the relationships of I_{ON} with different geometric parameters are shown in figure 3-33. From figure 3-33 (a), I_{ON} shows a linear relationship with the teeth number N_t as I_{ON} is directly related with the channel numbers (there are two channels for each tooth). From figure 3-33 (b), it is shown that I_{ON} is independent of the single channel width W_c. These two relationships are same as the previous VTFT structure with a 200 nm Si_3N_4 insulating layer. Figure 3-33 (c) demonstrates that I_{ON} increases a little with the tooth width W_t, however, the influence of W_t could be neglectable.

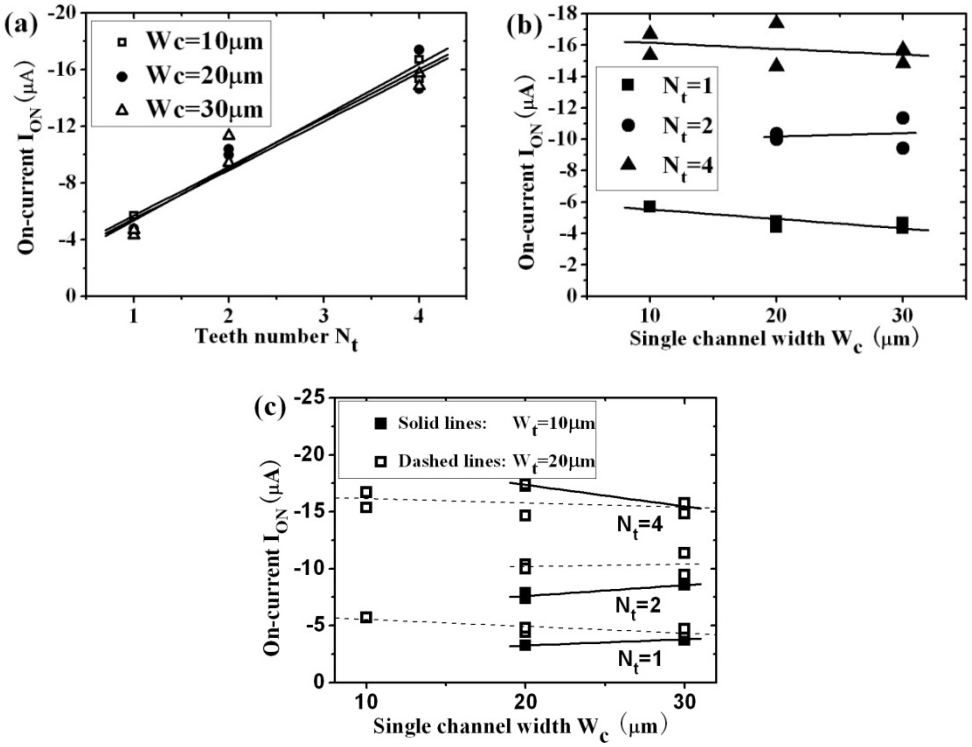


Figure 3-33: The relationships of I_{ON} with different geometric parameters: *(a)* I_{ON} is proportional to the teeth number N_t, *(b)* I_{ON} is proportional to the single channel width W_c, and *(c)* I_{ON} increase a little with the tooth width W_t.

Figure 3-34 gives the relationships between the off-current I_{OFF} and the geometric parameters. From figure 3-34 (a) and 3-34 (b), I_{OFF} shows a strictly linear relationship with the teeth number N_t as well as the single channel width W_c, which confirms that the off-current I_{OFF} is directly related with the active layer region. From figure 3-34 (c), I_{OFF} is independent of the tooth width W_t, which highlights that I_{OFF} is just brought by the active layer part between source and drain, while the active layer on top of the tooth doesn't have any effect on I_{OFF}.

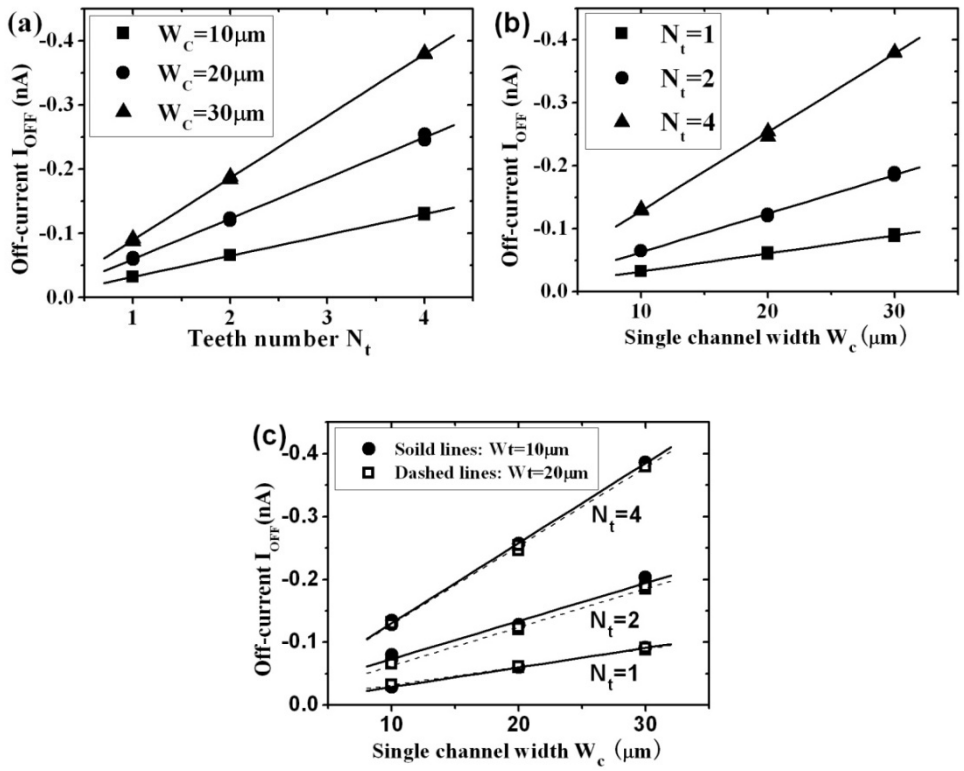


Figure 3-34: The relationships of I_{OFF} with different geometric parameters: *(a)* I_{OFF} is proportional to the teeth number N_t, *(b)* I_{OFF} is in proportion to the single channel width W_c, and *(c)* I_{OFF} is independent of the tooth width W_t.

VI.2.2 N-type VTFT

For the N-type VTFT, the effect of geometric parameters on the on-current I_{ON} is also obtained, shown in figure 3-35. The same relationships have been obtained, I_{ON} is proportional to the teeth number N_t, while it doesn't change with the single channel width W_c. In addition, I_{ON} increases a little with the tooth width W_t.

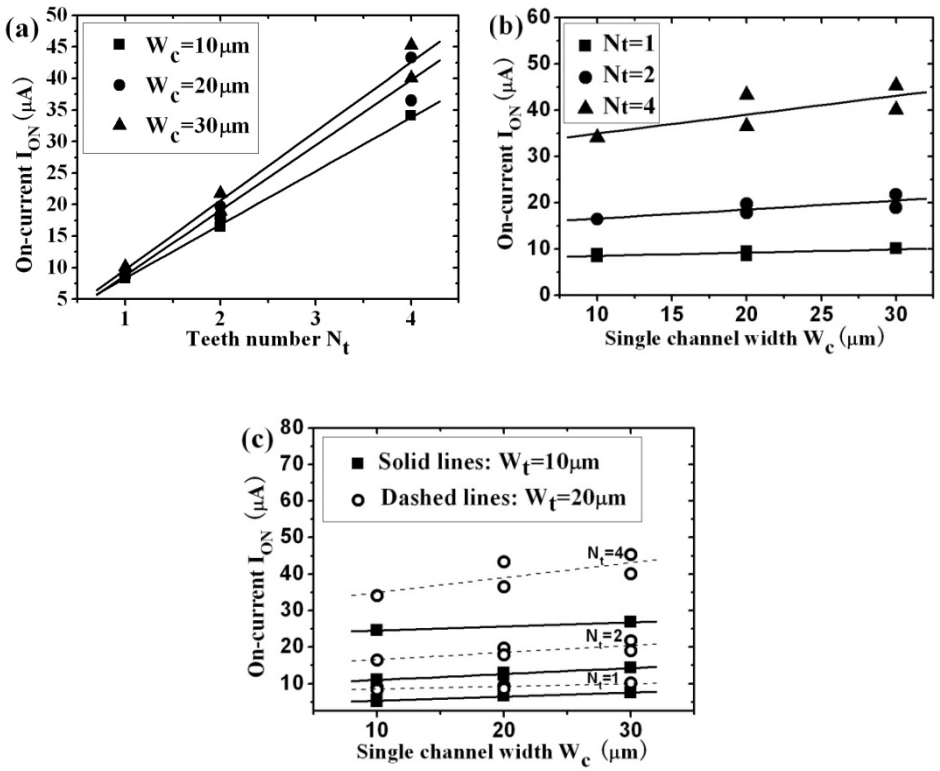
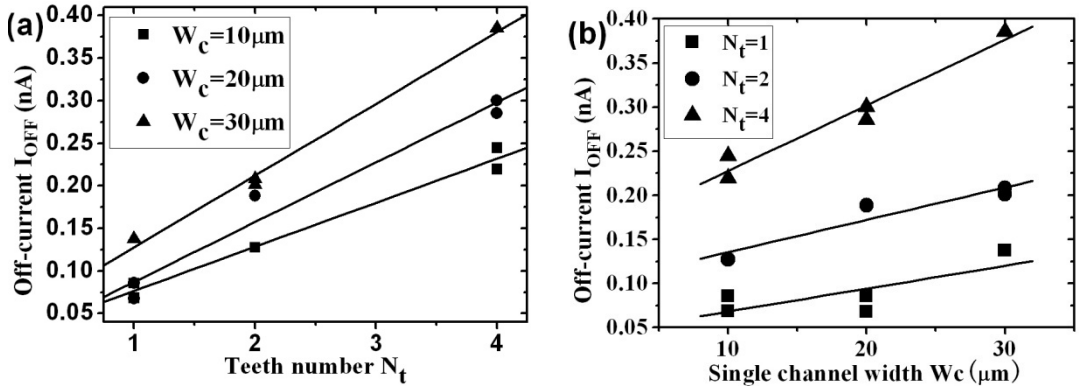


Figure 3-35: The relationship between the on-current I_{ON} and the geometric parameters: *(a)* I_{ON} is in proportion to the teeth number N_t, *(b)* I_{ON} is independent of the single channel width W_c, and *(c)* I_{ON} increases a little with the tooth width W_t.

As well, I_{OFF} is proportional to the teeth number N_t and the single channel width W_c, shown in figure 3-36 (a) and figure 3-36 (b). However, I_{OFF} increases a little with the tooth width W_t, as shown in figure 3-36 (c). However, the increase could be neglected.



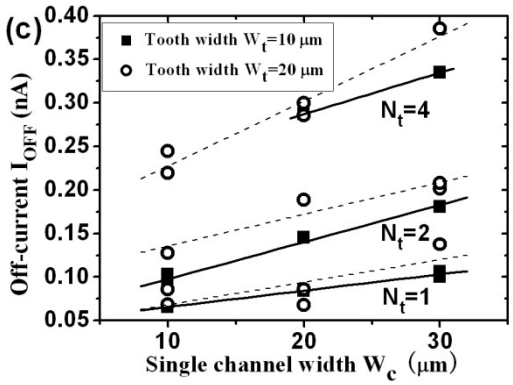


Figure 3-36: The relationship between the off-current I_{OFF} and the geometric parameters: *(a)* I_{OFF} is proportional to the teeth number N_t, *(b)* I_{OFF} is proportional to the single channel width W_c, and *(c)* I_{OFF} increases a little with the tooth width W_t.

VI.2.3 The effect of geometric parameters on the I_{ON}/I_{OFF} ratio

By combining the analysis of on-current I_{ON} and off-current I_{OFF}, we could conclude that, for a fixed tooth width W_t, the I_{ON}/I_{OFF} ratio follows the equation:

$$\frac{I_{ON}}{I_{OFF}} \propto \frac{N_t}{N_t W_c} \propto \frac{1}{W_c} \qquad (eq.3-2)$$

Which means that for the new VTFTs, the I_{ON}/I_{OFF} ratio could be increased by reducing the single channel width W_c, thus a narrow single channel width W_c is required, which is approximate to the design rule. This also indicates a reduction of tooth length, which is fixed at 60 μm for the current mask definitions. In contrast, the teeth number N_t doesn't affect the final I_{ON}/I_{OFF} ratio, as expected, even though the higher teeth number N_t enables to provide a higher I_{ON}, which is the major advantage of our VTFTs. In addition, the I_{ON}/I_{OFF} ratio is not affected by the tooth width W_t.

VII. Conclusion

In this chapter, the fabrication process of the new VTFTs has been introduced, and their electrical characteristics have also been analyzed. The new VTFTs have greatly reduced the off-current I_{OFF} as the large overlapping area for the classical VTFTs have been suppressed. The five-mask process is introduced in the fabrication process, and different geometric parameters

have been defined, including the teeth number N_t, the single channel width W_c, and the tooth width W_t.

The new VTFT structure is based on the introduction of an insulating layer between source and drain, while the active layer is locally located on the sidewall. The 100 nm SiO_2 and 200 nm Si_3N_4 insulating layers are adopted as the insulating layer between source and drain. For the same active layer thickness T_{AC} of 300 nm, the SiO_2 insulating layer enables to realize better electrical characteristics and higher stability for the VTFT, in comparison with the Si_3N_4 insulating layer. This is due to the worse insulating quality of Si_3N_4 deposited by LPCVD at 600°C. Therefore, the SiO_2 insulating layer will always be adopted in the fabrication process of the new VTFTs.

For the VTFTs with a 100 nm SiO_2 insulating layer, for different active layer thicknesses T_{AC}, stable I_{ON}/I_{OFF} ratios in the order of 10^5 have been obtained. When reducing T_{AC}, I_{ON}/I_{OFF} ratio increases a little while the field effect mobility μ_{FE} reduces a little, VTFTs with T_{AC} = 150 nm have obtained the compromise between I_{ON}/I_{OFF} ratio and field effect mobility μ_{FE}. The active layer deposited from Si_2H_6 precursor gas has also been attempted, however, it shows a worse electrical property in comparison with the one deposited from SiH_4 precursor gas.

For the new VTFTs with a 100 nm SiO_2 insulating layer and an active layer thickness T_{AC} of 150 nm, the P and N-type VTFTs have been fabricated in the same run. The symmetric transfer characteristics have been obtained, which demonstrates the feasibility of the COMS-like VTFT applications, such as inverters or oscillators.

The effect of the geometric parameters on the electrical characteristics has also been studied, and several conclusions have been drawn:

1) For the on-current I_{ON}, it is proportional to the teeth number N_t, while it is independent of the single channel width W_c. In addition, I_{ON} increases a little with the tooth width W_t.
2) For the off-current I_{OFF}, it is proportional to the teeth number N_t as well as the single channel width W_c, while it is independent of the tooth width W_t.

3) For the I_{ON}/I_{OFF}, for a fixed tooth width W_t, I_{ON}/I_{OFF} is in reverse proportion to the single channel width W_c, thus a narrow single channel width W_c that is approximate to the design rule is required in order to get a higher I_{ON}/I_{OFF} ratio.

Even though we have fabricated VTFTs with a stable I_{ON}/I_{OFF} ratio in the order of 10^5, the field effect mobility μ_{FE} is still low in terms of a poly-Si TFT, this is mainly due to that the rough vertical sidewalls have affected the crystallization of poly-Si. Indeed, we still do not know the crystallization of poly-Si on the vertical sidewall, and further work will be on the roughness reduction of the sidewall, as well as the study on the crystallization mechanism of the poly-Si on the vertical sidewall.

Conclusion and perspectives

Conclusion

The object of this work was to develop vertical thin film transistors (VTFTs) based on the low-temperature (T≤600°C) polycrystalline silicon technology.

The classical VTFTs were fabricated by rotating lateral thin film transistors (LTFTs) 90°. Initially, four plastic masks were adopted to fabricate VTFTs. The feasibility of the classical VTFTs fabrication had been proved, and the electrical performance was promising, however, VTFT structure needed to be improved. After analyzing the VTFT structure, a parasitic channel was found at the backside of the top electrode, which may affect the electrical performance. Therefore, a thick SiO_2 layer was introduced at the backside, in order to suppress the parasitic channel.

A new set of five glass masks was employed for the fabrication of VTFTs. Different geometric parameters were defined, in order to validate the reproducibility of the VTFTs, as well as to study the effect of geometric parameters on the electrical performance.

After fabricating VTFTs, the electrical characteristics were analyzed. The on/off-current ratio I_{ON}/I_{OFF} of 10^3 was obtained. On-current I_{ON} has confirmed the theoretical formula, and it was strictly proportional to the geometric parameters. Off-current I_{OFF} was proportional to the overlapping area A_{OV} between source and drain, and the large overlapping area greatly degraded I_{ON}/I_{OFF} ratio.

The analysis of the electrical characteristics had led to a feedback on the technological process. A thick SiO_2 layer was introduced to eliminate the major part of the overlapping area. As expected, a higher I_{ON}/I_{OFF} ratio almost in the order of 10^5 was obtained. However, I_{OFF} was still high and the reproducibility was rather low.

Therefore, a new VTFT structure was proposed. Source and drain were entirely isolated by a barrier layer, and the active layer was deposited after the formation of the sidewall. Therefore, this new structure totally eliminated the overlapping area A_{OV}. The key points for the new VTFTs are shown below:

- The sidewalls formation was a technological challenge due to the etching selectivity between the poly-Si layer and the insulating layer.
- The insulating layer between source and drain was important for the electrical characteristics. The adopted insulating materials were SiO_2 deposited by APCVD at 420°C, and Si_3N_4 deposited by LPCVD at 600°C.
- The different active layer thicknesses T_{AC} may also affect I_{ON} and I_{OFF}.

The process for the new structure adopted a 100 nm SiO_2 insulating layer or a 200 nm Si_3N_4 insulating layer, which validated the feasibility of the new VTFT fabrication, and a promising I_{ON}/I_{OFF} ratio of almost 10^5 was obtained. VTFTs with a SiO_2 insulating layer had better electrical characteristics and stability over VTFTs with a Si_3N_4 insulating layer, which was due to the poor insulating properties of Si_3N_4 deposited by LPCVD at 600°C. Therefore, SiO_2 insulating layers were always adopted for the new VTFTs fabrication.

The influence of geometric parameters on the electrical characteristics was analyzed. I_{OFF} was proportional to the geometric parameters, while I_{ON} was only proportional to the teeth number N_t. I_{ON}/I_{OFF} ratio was in reverse proportion to W_c.

VTFTs with different active layer thicknesses T_{AC} were also studied. When reducing T_{AC} (225 nm, 150 nm, 100 nm), the very stable I_{ON}/I_{OFF} ratios of more than 10^5 (with only a little increase) were always obtained, while the field effect mobility μ_{FE} reduced a little.

P and N-type VTFTs were also fabricated with an active layer thickness of 150 nm, the symmetric electrical characteristics revealed the feasibility of CMOS-like VTFT applications as inverters or oscillators.

The low field effect mobility μ_{FE} was always obtained, which may be due to the high roughness of the etched sidewall, and the crystallization of the active layer on the vertical sidewall.

Perspectives

As it is shown from the conclusion part, the new VTFTs have great advantages over the

classical VTFTs. Therefore, future work will be focused on the new VTFT structure. There are several problems and improvements to be addressed for the new VTFT structure:

- The relationship of the geometric parameters and the I_{ON}/I_{OFF} ratio has shown that, a higher I_{ON}/I_{OFF} ratio is obtained with a smaller single channel width W_c. Therefore, in order to further increase the I_{ON}/I_{OFF} ratio, a new mask is required with the reduced single channel width W_c approximate to the design rule.
- For 3D FETs, the high roughness of the sidewalls is a common problem, and the new VTFT structure also undergoes this problem. By taking different reactive ion etching (RIE) tests based on SF_6 etchant, the sidewall profiles of the new VTFTs have been optimized. However, due to the etching selectivity between different materials, there is still a transition on the sidewall, which may have an influence on the electrical performances as the active layer is just deposited on the sidewall. Therefore, one solution could be attempting to reduce the insulating layer thickness, in order to form a smoother sidewall. Another solution could be the further study of the RIE by adopting different etchants (CF_4 as an example) and different additives (for example O_2, Ar). In addition, it is also necessary to choose an appropriate insulating material between source and drain, whose etching rate is approximate to the one of poly-Si.
- So far, even though we have got the first conclusion for the relationship between the active layer thickness T_{AC} and the electrical characteristics, the crystallization mechanism of the active layer on the vertical sidewall is still unknown. In fact, it is very difficult to make the measurements on the vertical sidewall. The crystalline morphology of the active layer greatly affects the electrical characteristics, especially the field effect mobility μ_{FE}. Therefore, except to search an appropriate way for measuring the crystallization on the sidewall in order to optimize the crystallization, other crystallization methods could also be attempted to realize a better crystallization. For example, the metal-induced lateral crystallization (MILC) method could be adopted for the active layer crystallization on the vertical sidewall.
- Except for the VTFTs fabrication, another transistor called “vertical tunneling field effect

transistor (vertical TFET)" could also be fabricated, which theoretically enables to reduce the leakage current. Due to the special vertical structure, the same masks could be adopted, and the only difference of the vertical TFET from the VTFT, lies in the different doping types for source and drain layers.

References

Chapter 1

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[1] D. Kahng, M. M. Atalla, "Silicon-Silicon Dioxide Field Induced Surface Devices", *IRE Solid-State Devices Research Conference*, Carnegie Institute of Technology, Pittsburgh, PA (1960).

[2] D. Kahng, "A historical perspective on the development of MOS transistors and related devices", *IEEE Transactions on Electron Devices*, 23(7) (1976) p 655-657.

[3] G.E.Moore, "Cramming more components onto integrated circuits", *Electronics*, 38(8) (1965) p 114-117.

[4] G.E.Moore, "Progress in digital integrated electronics", *IEEE International Electron Devices Meeting (IEDM)*, (1975) p 11-13.

[5] ITRS, "International Technology Roadmap for Semiconductors 2010 Update overview" (2010) p 6.
http://www.itrs.net/Links/2010ITRS/2010Update/ToPost/2010_Update_Overview.pdf

[6] Jon Cartwright, "Intel enters the third dimension", *nature news*, (2011).
doi:10.1038/news.2011.274
http://www.nature.com/news/2011/110506/full/news.2011.274.html

[7] Mark Bohr, kaizad Mistry, "Intel's Revolutionary 22 nm Transistor Technology", (2011) p 16-22.
http://download.intel.com/newsroom/kits/22nm/pdfs/22nm-Details_Presentation.pdf

[8] Mark LaPedus, "update: Intel to build fab for 14-nm chips", (2011).
http://www.eetimes.com/electronics-news/4213295/Intel-to-build-new-Arizona-fab-

[9] "IBM and ARM to Collaborate on Advanced Semiconductor Technology for Mobile Electronics", *IBM Press release*, (2011).
http://www-03.ibm.com/press/us/en/pressrelease/33405.wss#release

[10] Myung-Soo Noh, Beom-Seok Seo, Suk-Joo Lee, Alex Miloslavsky, Christopher Cork, Levi Barnes, Kevin Lucas, "Implementing and validating double patterning in 22-nm to 16-nm product design and patterning flows", *Proceedings of The International Society for Optical Enginnering (Proc. SPIE)*, 7640, 76400S (2010).

[11] A. Kaneko, A. Yagishita, K. Yahashi, T. Kubota, M. Omura, K. Matsuo, I. Mizushima, K. Okano, H. Kawasaki, S. Inaba, T. Izumida, T. Kanemura, N. Aoki, K. Ishimaru, H. Ishiuchi, K. Suguro, K. Eguchi, Y. Tsunashima, "Sidewall Transfer Process and Selective Gate Sidewall Spacer Formation Technology for Sub-15nm FinFET with Elevated Source/Drain Extension", *IEEE International Electron Devices Meeting (IEDM)*, (2005) p 844–847.

[12] S. Hall, D. Donaghy, O. Buiu, E. Gili, T. Uchino, V.D. Kunz, C.H. de Groot, P. Ashburn,

"Recent developments in deca-nanometer vertical MOSFETs", *Microelectronic Engineering*, 72 (2004) p 230-235.

[13] M. Kittler, F. Schwierz, D. Schipanski, "Scaling of vertical and lateral MOSFETs in the deep submicrometer range", *Proceeding of 2000 third IEEE International Caracas Conference on Devices, Circuits and Systems*, (2000) p D58/1-D58/6.

[14] Paul K. Weimer, "The TFT - A New Thin-Film Transistor", *Proceeding of the Institute of Radio Enginners (Proc. IRE)*, (1962) p 1462-1469.

[15] Robert A. Street, "Thin-Film Transistors", *Advanced Materials*, 21 (2009) p 1-16.

[16] Chun-Ting Liu, Chen-Hua Douglas Yu, Avi Kornblit, and Kuo-Hua Lee, "Inverted Thin-Film Transistors with a Simple Self-aligned Lightly Doped Drain Structure", *IEEE Transactions on Electron Devices*, 39(12) (1992) p 2803–2809.

[17] L. Pichon, F. Raoult, K. Mourgues, K. Kis-Sion, T. Mohammed-Brahim, O. Bonnaud, "Low temperature (≤ 600°C) unhydrogenated *in-situ* doped polysilicon thin film transistors: Towards a technology for flat panel displays", *Thin Solid Films*, 296(1) (1997) p 133-136.

[18] K. Kandoussi, A. Gaillard, C. Simon, N. Coulon, T. Pier and T. Mohammed-Brahim, "Improved microcrystalline silicon TFTs", *Journal of Non-Crystalline Solids*, 352(9) (2006) p 1728-1731.

[19] M. Sarret, A. Liba, and O. Bonnaud, "Low-pressure chemical vapor deposition of low *in situ* phosphorus doped silicon thin films", *Applied Physics Letters*, 59(121) (1991) p 1438-1439.

[20] M. Sarret, A. Liba, F. Le Bihan, P. Joubert, and B. Fortin, "N-type polycrystalline silicon films obtained by crystallization of *in situ* phosphorus-doped amorphous silicon films deposited at low pressure", *Journal of Applied Physics*, 76(9) (1994) p 5492-5497.

[21] Satoshi Inoue, Sumio Utsunomiya, Takayuki Saeki, and Tatsuya Shimoda, "Surface-Free Technology by Laser Annealing (SUFTLA) and Its Application to Poly-Si TFT-LCDs on Plastic Film With Integrated Drivers", *IEEE Transactions on Electron Devices*, 49(8) (2002) p 1353-1360.

[22] Sang-Jin Lee, Seok-Woo Lee, Kum-Mi Oh, Soo-Jeong Park, Kyung-Eon Lee, Yong-Su Yoo, Kyoung-Moon Lim, Myoung-Su Yang, Yong-Suk Yang, and Yong-Kee Hwang, "A Novel Five-Photomask Low-Temperature Polycrystalline Silicon CMOS Structure for AMLCD Application", *IEEE Transactions on Electron Devices*, 57(9) (2010) p 2324 - 2329.

[23] Efstathios Persidis, Holger Baur, Fabio Pieralisi, Patrick Schalberger, Norbert Fruehauf, "A poly-Si AMOLED display with high uniformity", *Solid-State Electronics*, 52 (2008) p 1691 - 1693.

[24] Olivier Bonnaud, Tayeb Mohammed-Brahim, "Improvement of electrical properties of silicon-based thin-film transistors by modifying technological fabrication processes", *Applied*

Physics A, 96 (2009) p 259-269.

[25] L Pichon, K Mourgues, F Raoult, T Mohammed-Brahim, K Kis-Sion, D Briand and O Bonnaud, "Thin film transistors fabricated by *in situ* doped unhydrogenated polysilicon films obtained by solid phase crystallization", *Semiconductor Science and Technology*, 16 (2001) p 918-924.

[26] Gael Gautier, "Conception, Realisation et mise au point d'une tecnologie CMOS en transistors couches minces sur substrat de verre", *Thesis of the University of Rennes1* (2002).

[27] Emmanuel Jacques, "Microsysteme et capteur integres en technologie couches minces basse temperature", *Thesis of the University of Rennes1* (2008).

[28] E. Jacques, F. Le Bihan, S.Crand and T. Mohammed-Brahim, "Hall effect sensors and conditioning circuit for a low cost position sensor", in *Proceedings Eurosensor 2006* (2006) in Goteborg, Sweden, p 198-199.

[29] Chang-Hyun Park, Myung-Hwan Oh, Hee-Sung Kang, Ho-Kyu Kang, "A 15 nm Ultrathin Body SOI CMOS Device with Double Raised Source/Drain for 90 nm Analog Applications", *Journal of Electronics and Telecommunications Research Institute (ETRI Journal)*, 26 (6) (2004) p 575-582.

[30] Joachim Knoch, Min Zhang, Siegfried Mantl, J. Apenzeller, "On the Performance of Single-Gated Ultrathin-Body SOI Schottky-Barrier MOSFETs", *IEEE Transactions on Electron Devices*, 53(7) (2006) p 1669-1674.

[31] Yee Chia Yeo, Vivek Subramanian, Jakub Kedzierski, Peiqi Xuan, Tsu-Jae King, Jeffrey Bokor, Chenming Hu, "Nanoscale Ultra-Thin-Body Silicon-on-Insulator P-MOSFET with a SiGe/Si Heterostructure Channel", *IEEE Electron Device Letters*, 21(4) (2000) p 161-163.

[32] Yang-Kyu Choi, Kazuya Asano, Nick Lindert, Vivek Subramanian, Tsu-Jae King, Jeffrey Bokor, Chenming Hu, "Ultrathin-Body SOI MOSFET for Deep-Sub-Tenth Micron Era", *IEEE Electron Device Letters*, 21(5) (2000) p 254-255.

[33] Jakub Kedzierski, Peiqi Xuan, Vivek Subramanian, Jeffrey Bokor, Tsu-Jae King, Chenming Hu, "A 20 nm gate-length ultra-thin body p-MOSFET with silicide source/ drain", *Superlattices and Microstructures*, 28(5) (2000) p 445-452.

[34] David Lammers, "Tri-gate's fallout" (2011).
http://chipdesignmag.com/sld/blog/2011/05/26/tri-gate%E2%80%99s-fallout/

[35] L. Risch, "Pushing CMOS beyond the roadmap", *Solid-State Electronics*, 50 (2006) p 527-535.

[36] Felice Crupi, Ben Kaczer, Robin Degraeve, Vaidy Subramanian, Purushothaman Srinivasan, Eddy Simoen, Abhisek Dixit, Malgorzata Jurczak, and Guido Groeseneken, "Reliability Comparison of Triple-Gate Versus Planar SOI FETs", *IEEE Transactions on Electron Devices*, 53(9) (2006) p 2351-2357.

[37] Digh Hisamoto, Wen-Chin Lee, Jakub Kedzierski, Erik Anderson, Hideki Takeuchi, Kazuya Asano, Tsu-Jae King, Jeffrey Bokor, and Chenming Hu, "A Folded-channel MOSFET for Deep-sub-tenth Micron Era", *International Electron Devices Meeting (IEDM)*, (1998) p. 1032-1034.

[38] Digh Hisamoto, Toru Kaga, Yoshifumi Kawamoto and Eiji Takeda, " A Fully Depleted Lean-channel Transistor (DELTA) - A novel vertical ultra thin SOI MOSFET", *International Electron Devices Meeting (IEDM)*, (1989) p 833-836.

[39] Digh Hisamoto, Wen-Chin Lee, Jakub Kedzierski, Hideki Takeuchi, Kazuya Asano, Charles Kuo, Erik Anderson, Tsu-Jae King, Jeffrey Bokor, and Chenming Hu, "FinFET—A Self-aligned Double-Gate MOSFET Scalable to 20 nm", *IEEE Transactions on Electron Devices*, 47(12) (2000) p 2320-2325.

[40] Yang-Kyu Choi, Nick Lindert, Peiqi Xuan, Stephen Tang, Daewon Ha, Erik Anderson, Tsu-Jae King, Jeffrey Bokor, and Chenming Hu, "Sub-20nm CMOS FinFET Technologies", *International Electron Devices Meeting (IEDM)*, (2001) p 421-424.

[41] Xuejue Huang, Wen-Chin Lee, Charles Kuo, Digh Hisamoto, Leland Chang, Jakub Kedzierski, Erik Anderson, Hideki Takeuchi, Yang-Kyu Choi, Kazuya Asano, Vivek Subramanian, Tsu-Jae King, Jeffrey Bokor and Chenming Hu, "Sub 50-nm FinFET: PMOS", *International Electron Devices Meeting (IEDM)*, (1999) p 67-70.

[42] Bin Yu , Leland Chang, Shibly Ahmed, Haihong Wang, Scott Bell, Chih-Yuh Yang, Cyrus Tabery, Chau Ho, Qi Xiang, Tsu-Jae King, Jeffrey Bokor, Chenming Hu , Ming-Ren Lin, and David Kyser, "FinFET Scaling to 10nm Gate Length", *International Electron Devices Meeting (IEDM)*, (2002) p 251-254.

[43] Xuejue Huang, Wen-Chin Lee, Charles Kuo, Digh Hisamoto, Leland Chang, Jakub Kedzierski, Erik Anderson, Hideki Takeuchi, Yang-Kyu Choi, Kazuya Asano, Vivek Subramanian, Tsu-Jae King, Jeffrey Bokor, and Chenming Hu, "Sub-50 nm P-Channel FinFET", *IEEE Transactions on Electron Devices*, 48(5) (2001) p 880-886.

[44] Hemant Adhikari, Harlan R. Harris, Casey E. Smith , Ji-Woon Yang, Brian Coss, Srivatsan Parthasarathy , Bich-Yen Nguyen, Paul Patruno, Tejas Krishnamohan, Ian Cayrefourcq, Prashant Majhi, and Raj Jammy Sematech, "High mobility SiGe shell-Si core omega gate PFETs", *International Symposium on VLSI Technology*, (2009) p 136-138.

[45] Jong-Tae Park, Jean-Pierre Colinge, and Carlos H. Diaz, "Pi-Gate SOI MOSFET", *IEEE Electron Device Letters*, 22(8) (2001) p 405-406.

[46] Sorin Cristoloveanu, Kerem Akarvardar and Pierre Gentil, "A Review of the SOI Four-Gate Transistor", *8th International Conference on Solid-State and Integrated Circuit Technology*, (2006) p 31-34.

[47] Yi Song, Huajie Zhou, Qiuxia Xu, Jiebin Niu, Jiang Yan, Chao Zhao, and Huicai Zhong, "High-Performance Silicon Nanowire Gate-All-Around nMOSFETs Fabricated on Bulk

Substrate Using CMOS-Compatible Process", *IEEE Electron Device Letters*, 31(12) (2010) p 1377-1379.

[48] M. Vinet, T. Poiroux, J. Widiez, J. Lolivier, B. Previtali, C. Vizioz, B. Guillaumot, Y. Le Tiec, P. Besson, B. Biasse, F. Allain, M. Cassé, D. Lafond, J.-M. Hartmann, Y. Morand, J. Chiaroni, and S. Deleonibus, "Bonded Planar Double-Metal-Gate NMOS Transistors Down to 10 nm", *IEEE Electron Device Letters*, 26(5) (2005) p 317-319.

[49] Santosh Kumar Gupta, Gaurab G. Pathak, Debajit Das, Chandan Sharma, "Double Gate MOSFET and its Application for Efficient Digital Circuits", *3rd International Conference on Electronics Computer Technology*, (2011) p 33-36.

[50] Weimin Zhang, Jerry G. Fossum, Fellow, IEEE, and Leo Mathew, "The ITFET: A Novel FinFET-Based Hybrid Device", *IEEE Transactions on Electron Devices*, 53(9) (2006) p 2335-2343.

[51] Y. Jiang, N. Singh, T. Y. Liow, P. C. Lim, S. Tripathy, G. Q. Lo, D. S. H. Chan, and D.-L. Kwong, "Omega-Gate p-MOSFET With Nanowirelike SiGe/Si Core/Shell Channel", *IEEE Electron Device Letters*, 30(4) (2009) p 392-394.

[52] J.W. Park, W. Xiong and J.P. Colinge, "Accumulation-Mode Pi-gate MOSFET", *IEEE International SOI Conference*, (2003) p 65-67.

[53] K. Akarvardar, S. Cristoloveanu, M. Bawedin, P. Gentil, B.J. Blalock, D. Flandre, "Thin film fully-depleted SOI four-gate transistors", *Solid-State Electronics*, 51 (2007) p 278-284.

[54] Chen-Ming Lee, and Bing-Yue Tsui, "A High-Performance 30-nm Gate – All - Around Poly-Si Nanowire Thin-Film Transistor With NH_3 Plasma Treatment", *IEEE Electron Device Letters*, 31(7) (2010) p 683-685.

[55] Jean-Pierre Colinge, "Multiple-gate SOI MOSFETs", *Solid-State Electronics*, 48 (2004) p 897-905.

[56] N. Garry Tarr, "A Polysilicon Emitter Solar Cell", *IEEE Electron Device Letters*, 6(12) (1985) p 655-658.

[57] Behammer D, Zeuner M, Hackbarth T, Herzog J, Schafer M, Grabolla T, "Comparison of of lateral and vertical Si-MOSFETs with ultra short channels", Thin Solid Films, 336 (1998) 313-318, *Thin Solid Films*, 336 (1998) p 313-318.

[58] Chun-Yu Wu, Yen-Ting Liu, Ta-Chuan Liao, Ming H. Yu, and Huang-Chung Cheng, "Novel Dielectric-Engineered Trapping-Charge Poly-Si-TFT Memory With a TiN–Alumina–Nitride–Vacuum–Silicon Structure", *IEEE Electron Device Letters*, 32(8) (2011) p 1095-1097.

[59] Lothar Risch, Wolfgang H. Krautschneider, Franz Hofmann, Herbert Schafer, Thomas Aeugle, and Wolfgang Rosner, "Vertical MOS Transistors with 70 nm Channel Length", *IEEE Transactions on Electron Devices*, 43(9) (1996) p 1495-1498.

[60] W. Rosner, E. Landgraf , J. Kretz, L. Dreeskornfeld, H. Schafer, M. Stadele, T. Schulz, F. Hofmann, R.J. Luyken,M. Specht, J. Hartwich, W. Pamler, L. Risch, "Nanoscale FinFETs for low power applications", *Solid-State Electronics*, 48 (2004) p 1818-1823.

[61] J. Moers, D. Klaes,A.Toennesmanna, L. Vescana, S. Wickenhaeuser,T. Grabollab, M. Marsoa, P. Kordosi,H.Lueth, "Vertical p-MOSFETs with gate oxide deposition before selective epitaxial growth", *Solid-State Electronics*, 43 (1999) p 529-535.

[62] D. Klaes, J. Moers,A.Toennesmanna, S.Wickenhaeuser, L. Vescana, M. Marsoa, T. Grabollab,M. Grimma,H.Luetha, "Selectively grown vertical Si MOS transistor with reduced overlap capacitances", *Thin Solid Films*, 336 (1998) 306-308.

[63] Haitao Liu, Zhibin Xiong, and Johnny K. O. Sin, "An Ultrathin Vertical Channel MOSFET for Sub-100-nm Applications", *IEEE Transactions On Electron Devices*, 50(5) (2003) p 1322-1327.

[64] Haitao Liu, Johnny K. O. Sin, Peiqi Xuan, and Jeffrey Bokor, "Characterization of the Ultrathin Vertical Channel CMOS Technology", *IEEE Transactions On Electron Devices*, 51(1) (2004) p 106-112.

[65] M. Born, U. Abelein, K.K. Bhuwalka, M. Schindler, M. Schmidt, A. Ludsteck, J. Schulze, I. Eisele, "Sub-50 nm high performance PDBFET with impact ionization", *Thin Solid Films*, 508 (2006) p 323-325.

[66] C. Fink, K.G. Anil, H. Geiger, W. Hansch, F. Kaesen, J. Schulze, T. Sulima, I. Eisele, "Enhancement of device performance in vertical sub-100 nm MOS devices due to local channel doping", *Solid-State Electronics*, 46 (2002) p 387–391.

[67] D. Donaghy, S. Hall, C. H. de Groot, V. D. Kunz, and P. Ashburn, "Design of 50-nm Vertical MOSFET Incorporating a Dielectric Pocket", *IEEE Transactions on Electron Devices*, 51(1) (2004) p 158-161.

[68] D. Donaghy, S. Hall, V. D. Kunz, C. H. de Groot, and P. Ashburn, "Investigating 50 nm channel length vertical MOSFETS containing a dielectric pocket in a circuit environment," *European Solid-State Device Research Conference*, (2002) p 499-503.

[69] Akihiro Nitayama, Hiroshi Takato, Naoko Okabe, Kazumasa Sunouchi, Katsuhiko Hieda, Fumio Horiguchi, and Fujio Masuoka, "Multi-Pillar Surrounding Gate Transistor (M-SGT) for Compact and High-speed Circuits", *IEEE Transactions on Electron Devices*, 38(3) (1991) p 579-583.

[70] N. Shen, T.T. Le, H.Y. Yu, Z.X. Chen, K.T. Win, N. Singh, G.Q. Lo, and D.L. Kwong, "Fabrication and Characterization of Poly-Si Vertical Nanowire Thin Film Transistor", *world academy of science, engineering and technology*, 8(1) (2011) p 461-463.

[71] S. Hall, D. Donaghy, O. Buiu, E. Gili, T. Uchino, V.D. Kunz, C.H. de Groot, P. Ashburn, "Recent developments in deca-nanometer vertical MOSFETs", *Microelectronic Engineering*, 72 (2004) p 230-235.

[72] Kittler M, Schwierz F, Schipanski D., "Scaling of vertical and lateral MOSFETs in the deep submicrometer range", *3th IEEE International Caracas Conference on Devices, Circuits and Systems*, (2000) D58/1-D58/6.

[73] Olivier Bonnaud, "Vertical Channel Thin Film Transistor Technology: Similar Approach with 3D-ULSI Monolithic Technology", *ECS Transactions*, 22(1) (2009) 293-304.

[74] Tiemin Zhao, Min Cao, Krishna C. Saraswat, James D. Flummer, "A vertical Submicron Polysilicon Thin Film Transistor Using a Low Temperature Process", *IEEE Electron Device Letters*, 15(10) (1994) p 415-417.

[75] Po-Yi Kuo, Tien-Sheng Chao, Jiou-Teng Lai, and Tan-Fu Lei, "Vertical n-Channel Poly-Si Thin-Film Transistors with Symmetric S/D Fabricated by Ni-Silicide-Induced Lateral-Crystallization Technology", *IEEE Electron Device Letters*, 30(3) (2009) p 237-239.

[76] Ming-Zhen Lee, Chung-Len Lee and Tan-Fu Lei, "Novel Vertical Polysilicon Thin-Film Transistor with Excimer-Laser Annealing", *Japanese Journal of Applied Physics*, 42 (2003) p 2123–2126.

Chapter 2

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[77] K. Belarbi, K. Kandoussi, C. Simon, N. Coulon, T. Mohammed-Brahim, "Stability of microcrystalline silicon TFTs", *ECS Transactions*, 16(9) (2008) p121-129.

[78] K. Kandoussi, C. Simon, N. Coulon, K. Belarbi, T. Mohammed-Brahim, "Nanocrystalline silicon TFT process using silane diluted in argon–hydrogen mixtures", *Journal of Non-Crystalline Solids*, 354 (2008) p 2513-2518.

[79] K. Belarbi, K. Kandoussi, I. Souleiman, C. Simon, N. Coulon, and T. Mohammed-Brahim, "Decreasing the thickness of the active layer of microcrystalline silicon TFTs", *Physica Status Solidi C*, (2010) p 1-4.

[80] G. Harbeke, L. Krausbauer, E. F. Steig meier, and A. E. Widmer , H. F. Kaper and G. Neugebauer, "High quality poly-Si by amorphous low pressure chemical vapor deposition", *Applied Physics Letters*, 42(3) (1983) p 249 - 251.

[81] R. Rogel, M. Sarret, T. Mohammed-Brahim, O. Bonnaud, J.P. Kleider, "High quality unhydrogenated low-pressure chemical vapor deposited polycrystalline silicon", *Journal of Non-Crystalline Solids* 266-269 (2000) p 141-145.

[82] M.K. Hatalis, D.W. Greve, "High-performance thin-film transistors in low- temperature crystallized LPCVD amorphous silicon films", *IEEE Electron Device Letters*, 8(8) (1987) p 361-364.

[83] M. Sarret, A. Liba, O. Bonnaud, F. Le Bihan, B. Fortin, L. Pichon, F. Raoult, "*In-situ* phosphorous-doped VLPCVD polysilicon layers for polysilicon thin-film transistors", *IEE Proceedings on Circuits, Devices and Systems*, 141(1) (1994) p 19-22.

[84] L. Pichon, F. Raoult, K. Mourgues, O.Bonnaud, K. Kis-Sion, "A low temperature process (< 600°C) of unhydrogenated in situ doped polysilicon thin film transistors for active matrix applications", *Proceedings of the 26th European Solid-State Device Research Conference*, (1996) p 1059-1062.

[85] P. Joubert, B. Loisel, Y. Chouan, and L. Haji, "The Effect of Low Pressure on the structure of LPCVD Polycrystalline Silicon Films", *Journal of the Electrochemical Society*, 134(10) (1987) p 2541-2545.

[86] Regis Rogel, "Etude de la fasabilete de Diodes PIN Par depots L.P.C.V.D sur substrats de verre en vue d'applications photovoltaiques", *Thesis of University of Rennes1* (2001).

[87] R. Rogel, G. Gautier, N. Coulon, M. Sarret, O. Bonnaud, "Influence of precursors gases on LPCVD TFT's characteristics", *Thin Solid Films*, 427 (2003) p 108–112.

[88] H. Zhang, N.Kusmoto, T. Inushima and S. Yamazaki, "KrF excimer laser annealed TFT with very high field effect mobility of 329 $cm^2/V.s$", *IEEE Electron Device Letters*, 13(5) (1992) p 297-299.

[89] H.Kuriyama, "Excimer laser crystallization of silicon films for AMLCDs", *Second International Workshop on AMLCDs*, (1995) p 87-92.

[90] P.M. Smith, P.G. Carey and T.W. Sigmon, "Excimer laser crystallization and doping of silicon films on plastic substrates", *Applied Physics Letters*, 70(3) (1997) p 342-344.

[91] L. Plevert, "Cristallisation par recuit rapide du silicium amorphe sur verre", *Thesis of the University of Rennes1* (1995).

[92] N. Duhamel and B. Loisel, "Polysilicon technologies for large area displays", *Solid State Phenomema*, 37-38 (1994) p 535-546.

[93] S.W. Lee and S.K. Joo, "Low temperature poly-Si thin film transistors fabrication by metal induced lateral crystallization", *IEEE Electron Device Letters*, 17(4) (1996) p 160-162.

[94] Z. Jin, K. Moulding, H.S. Kwok, and M. Wong, "The effects of extended heat treatment on Ni induced lateral crystallization of amorphous silicon thin films", *IEEE Electron Device Letters*, 46(1) (1996) p 78-82.

[95] Jong-Yeon Kim, Jin-Woo Han, Jeong-Min Han, Young-Hwan Kim, Byeong-Yun Oh, Byoung-Yong Kim, Sang-Keuk Lee, and Dae-Shik Seo, "Nickel oxide-induced crystallization of silicon for use in thin film transistors with a SiN_X diffusion filter", *Applied Physics Letters*, 92(143501) (2008) p 1-3.

[96] A.G. Noskov, E.B. Gorokhov, G.A. Sokolova, E.M. Trukhanov, S.I. Stenin, "Correlation between stress and structure in chemically vapour deposited silicon nitride films", *Thin Solid Films*, 162 (1988) p 129-143.

[97] B. E. E. Kastenmeier, P. J. Matsuo, J. J. Beulens, and G. S. Oehrlein, "Chemical dry etching of silicon nitride and silicon dioxide using $CF_4/O_2/N_2$ gas mixtures", *Jouranl of*

Vaccuum Science and Technology A, 14(5) (1996) p 2802-2813.

[98] Hee Kwan Lee, Kwan Soo Chung and Jae Su Yu, "Selective Etching of Thick Si_3N_4, SiO_2 and Si by Using CF_4/O_2 and C_2F_6 Gases with or without O_2 or Ar Addition", *Journal of the Korean Physical Society*, 54(5) (2009) p1816-1823.

[99] H. D. Toure, T. Gaillard, N. Coulon, R. Rogel, O. Bonnaud, "Optimization of a thin film technology process for quasi-vertical TFTs", *European Materials Research Society (E-MRS)*, (2009).

[100] H. D. Toure, T. Gaillard, N. Coulon, O. Bonnaud, "H-shaped Vertical Polycrystalline Silicon Thin Film Transistor on Insulator", *ECS Transactions*, 19(4) (2009) p 195 - 200.

[101] H. D. Toure, T. Gaillard, N. Coulon, O. Bonnaud, "A Vertical Thin Film Transistor Based on Low Temperature Technology (T<600°C)", *ECS Transactions*, 16(9) (2009) p 165 - 170.

[102] A. Valletta, P. Gaucci, L. Mariucci, G. Fortunato, S.D. Brotherton, "Kink effect in short-channel polycrystalline silicon thin-film transistors", *Applied Physics Letters*, 85 (2004) p 3113-3115.

Publications

International Publications:

O. BONNAUD, P. ZHANG, E. JACQUES, R. ROGEL, "Vertical Channel Thin Film Transistor: Improvement approach similar to multigate monolithic CMOS Technology", *ECS Transactions*, 37 (1) (2011) p 29-37.

P. ZHANG, E. JACQUES, R. ROGEL, O. BONNAUD, "Improvement of a vertical thin film transistor based on low-temperature polysilicon silicon technology by introduction of an oxide barrier between drain and source layers", *ECS Transactions*, 49 (1) (2012) p 491-496.

P. ZHANG, E. JACQUES, R. ROGEL, N. COULON, O. BONNAUD, "Quasi-vertical multi-tooth thin film transistors based on low-temperature technology (T ≤ 600 °C)", *Solid State Electronics*, 79 (2013) p 26-30.

P. ZHANG, E. JACQUES, R. ROGEL, O. BONNAUD, "Decreasing the off-current for vertical TFT by using an insulating layer between source and drain", *ECS Transactions*, 50 (8) (2012) p 59-64.

International Conferences:

O. BONNAUD, P. ZHANG, E. JACQUES, R. ROGEL, "Vertical Channel Thin Film Transistor: Improvement approach similar to multigate monolithic CMOS Technology", *Invited Paper, ULSI vs TFT 2011 ECS Conference,* Hong Kong (China), June 2011.

P. ZHANG, E. JACQUES, R. ROGEL, O. BONNAUD, "Improvement of a vertical thin film transistor based on low-temperature polysilicon silicon technology by introduction of an oxide barrier between drain and source layers", *SBMicro2012*, Brasilia (Brazil), 30 Aug.-2.Sept. 2012.

P. ZHANG, E. JACQUES, R. ROGEL, O. BONNAUD, "Decreasing the off-current for vertical TFT by using an insulating layer between source and drain", *ECS TFTT XI,* Oral Presentation, Honolulu HA (USA), 8-10 Oct.2012.

National conferences:

P. ZHANG, E. JACQUES, R. ROGEL, O. BONNAUD, "Realization of comb-shaped vertical thin film transistors at low temperature (T<600°C)", *14EMEs Journées Nationales du Reseau Doctoral de Micro et Nanoelectronique, JNRDM 2011,* Paris, 23-25 mai 2011.

Annexes

Annex I RCA cleaning

Needed solutions:

NH_4OH: Ammonia solution, to eliminate organic impurities

H_2O_2: Hydrogen peroxide, to form a thin oxide layer that includes the impurities

HCl: Hydrochloric acid, to eliminate the metallic impurities

HF: Hydrogen fluoride, to eliminate the oxide layer that includes the impurities

Cleaning Steps:

a. SC1:

Content:	H_2O (5) + NH_4OH (0.25) + H_2O_2 (1)		
Volume (cm^3):	200	10	40
Adding Temperature (°C):	room	room	70 (cleaning temperature)
Cleaning time (minutes):	10	(put samples in the solution at 70°C after H_2O_2 adding)	

Clean in the de-ionized water for 3, 3, 4 minutes

b. SC2:

Content:	H_2O (5) + HCl (1) + H_2O_2 (1)		
Volume (cm^3):	200	40	40
Adding Temperature (°C):	room	room	80 (cleaning temperature)
Cleaning time (minutes):	10	(put samples in the solution at 80°C after H_2O_2 adding)	

Clean in the de-ionized water for 3, 3, 4 minutes

C. HF: 2% desoxydation HF

Content:	H_2O (25) + HF (1)		
Volume (cm^3):	400	16	
Adding temperature:	room	room	
Cleaning time (seconds):	10 - 20	(observe the hydrophobic phenomenon)	

Clean in the de-ionized water for 3, 3, 4 minutes

Note:

If there's a deposition process just after the RCA cleaning step, it is better to take the cleaning step C (diluted HF) just before the deposition process.

Annex II Photolithography

The total photolithography steps include pre-baking, spin coating of photoresist, soft baking, exposure, developing, cleaning, microscope observation, and hard baking.

a) Pre-baking:

Baking temperature: >100°C;

Baking time: >5 minutes

b) Spin-coating:

Photoresist type: SHIPLEY MICROPOSIT S1818;

Spin-coating speed: 4000 rpm;

Spin-coating acceleration: 5000 rpm/s;

Spin-coating time: 30 seconds;

Photoresist thickness: 1.8 μm

c) Soft baking:

Baking temperature: 100°C;

Baking time: 1.5 minutes

d) Exposure:

Operation machine: Karl Suss MA6 mask aligner;

Lithographic resolution: 0.5μm;

Exposure type: I-line (365 nm);

Exposure time: 55 seconds

e) Developing:

Developer: MICROPOSIT DEV;

Developing time: 40 - 50 seconds

f) De-ionized water cleaning:

Cleaning Time: 3minutes, 3minutes, and 4 minutes

g) Microscope observation

Check the photolithography quality

h) Hard baking:

Baking temperature: 120°C;

Baking time: 1.5 minutes

Annex III Masks design

VTFTs are defined with different geometric parameters, including the single channel width W_c, the teeth number N_t, and the tooth width W_t. The three geometric parameters are signed in the following figure III-1.

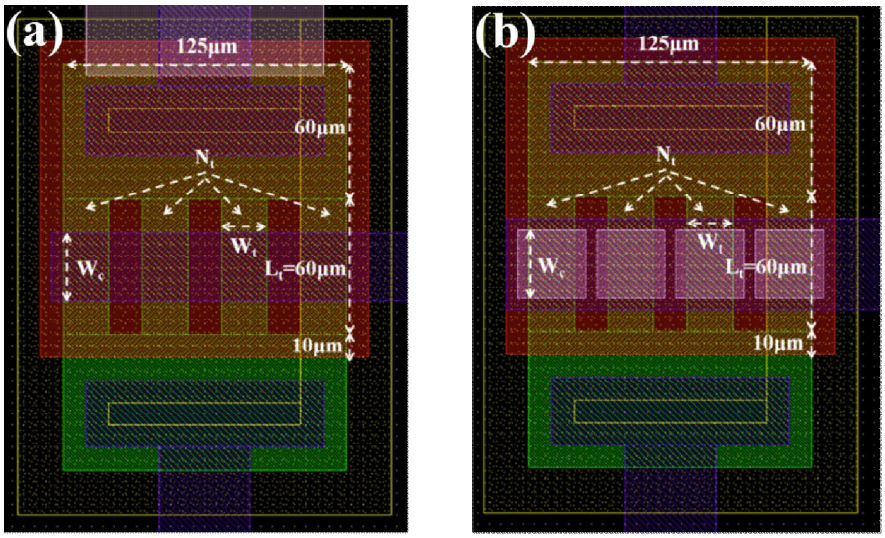

Figure III-1: Masks designs for (a) classical VTFT structure, and (b) the new VTFT structure.

For one cell, the different geometries are defined below in the table III-1.

(*Wc*=10µm, *Nt*=1, *Wt*=10µm)	(*Wc*=10µm, *Nt*=1, *Wt*=10µm)	(*Wc*=10µm, *Nt*=2, *Wt*=10µm)	(*Wc*=10µm, *Nt*=2, *Wt*=10µm)	(*Wc*=10µm, *Nt*=4, *Wt*=10µm)	(*Wc*=10µm, *Nt*=4, *Wt*=10µm)
(*Wc*=20µm, *Nt*=1, *Wt*=10µm)	(*Wc*=20µm, *Nt*=1, *Wt*=10µm)	(*Wc*=20µm, *Nt*=2, *Wt*=10µm)	(*Wc*=20µm, *Nt*=2, *Wt*=10µm)	(*Wc*=20µm, *Nt*=4, *Wt*=10µm)	(*Wc*=20µm, *Nt*=4, *Wt*=10µm)
(*Wc*=30µm, *Nt*=1, *Wt*=10µm)	(*Wc*=30µm, *Nt*=1, *Wt*=10µm)	(*Wc*=30µm, *Nt*=2, *Wt*=10µm)	(*Wc*=30µm, *Nt*=2, *Wt*=10µm)	(*Wc*=30µm, *Nt*=4, *Wt*=10µm)	(*Wc*=30µm, *Nt*=4, *Wt*=10µm)
(*Wc*=10µm, *Nt*=1, *Wt*=20µm)	(*Wc*=10µm, *Nt*=1, *Wt*=20µm)	(*Wc*=10µm, *Nt*=2, *Wt*=20µm)	(*Wc*=10µm, *Nt*=2, *Wt*=20µm)	(*Wc*=10µm, *Nt*=4, *Wt*=20µm)	(*Wc*=10µm, *Nt*=4, *Wt*=20µm)
(*Wc*=20µm, *Nt*=1, *Wt*=20µm)	(*Wc*=20µm, *Nt*=1, *Wt*=20µm)	(*Wc*=20µm, *Nt*=2, *Wt*=20µm)	(*Wc*=20µm, *Nt*=2, *Wt*=20µm)	(*Wc*=20µm, *Nt*=4, *Wt*=20µm)	(*Wc*=20µm, *Nt*=4, *Wt*=20µm)
(*Wc*=30µm, *Nt*=1, *Wt*=20µm)	(*Wc*=30µm, *Nt*=1, *Wt*=20µm)	(*Wc*=30µm, *Nt*=2, *Wt*=20µm)	(*Wc*=30µm, *Nt*=2, *Wt*=20µm)	(*Wc*=30µm, *Nt*=4, *Wt*=20µm)	(*Wc*=30µm, *Nt*=4, *Wt*=20µm)

Table III-1: Different geometric definitions in a cell.

Annex IV ATLAS simulation program

The program of the ATLAS simulation for the VTFT transfer characteristics is shown below:

```
go atlas

mesh infile=vtft.str
material material=polysiliconf.conmun=munpoly.lib nc=7e19

defect nta=1.12e21 ntd=4e20 wta=0.025 wtd=0.05 nga=5.e16 ngd=1.5e18 ega=0.4
egd=0.4 wga=0.1 wgd=0.1 sigtae=1e-16 sigtah=1e-14 sigtde=1e-14 sigtdh=1e-16
siggae=1e-16 siggah=1e-14 siggde=1e-14 siggdh=1e-16

impact an1=7.5e5 an2=7.5e5 ap1=6.71e5 ap2=1.582e6 bn1=1.130e6 bn2=1.230e6
bp1=1.693e6 bp2=2.036e6 betan=1 betap=1 egran=4e5

models conmob consrh bbt.kl fermi incomplete ioniz numcarre=2 temperature=300
method newton itlimit=25 trap atrap=0.5 maxtrap=4 autonr nrcriterion=0.1
tol.time=0.005 dt.min=1e-15

solve init

solve name=drain vdrain=1 outfil=init1
log outf=vtftnzone.log
solve name=gate vgate=0 vfinal=-10 vstep=-2.0

output e.field j.electron j.hole j.conduc j.total ex.field jx.electron jx.hole
jx.conduc jx.total ey.field jy.electron jy.hole jy.conduc jy.total flowlines
e.mobility h.mobility qss e.temp h.temp charge recomb val.band con.band qfn qfp
j.disp photogen impact

save outf=vtft.str

load infile=init1
log outf=vtftpzone.log
solve name=gate vgate=0 vfinal=20 vstep=2


quit
```

Résumé

Ce travail porte sur le développement de transistors en couches minces verticaux (VTFTs), du procédé de fabrication à l'analyse des caractéristiques électriques. Les transistors sont réalisés à partir de silicium polycristallin déposé et cristallisé en utilisant une technologie basse température ($T \leq 600°C$). La première étape de ce travail consiste à la fabrication et la caractérisation de VTFTs obtenus par rotation de 90° des transistors à couches minces latéraux (LTFTs). La faisabilité technologique de VTFTs est alors validée, et un rapport I_{ON}/I_{OFF} d'environ 10^3 est obtenu. L'analyse des résultats de caractérisation électrique a mis en évidence que ce fort courant à l'état bloquant I_{OFF} est principalement dû à la grande zone de recouvrement entre source et drain. La deuxième étape du travail réside dans la suppression partielle de cette zone de recouvrement qui aboutit à un rapport I_{ON}/I_{OFF} proche de 10^5. Dans la troisième partie de ce travail, une nouvelle architecture de transistors verticaux est proposée, qui élimine totalement la zone de recouvrement. Les effets de différents paramètres sont étudiés, notamment l'influence de l'épaisseur de la couche active, de la couche d'isolation, et de la dimension géométrique. Les transistors optimisés mettent en évidence un rapport I_{ON}/I_{OFF} supérieur à 10^5 avec une réduction du courant à l'état bloquant, une grande stabilité et une bonne reproductibilité du procédé technologique. Des transistors verticaux de type P et N ont également été réalisés. Ils ont montré des caractéristiques électriques symétriques, qui les rendent utilisables dans des applications similaires à la technologie CMOS.

Mots clés: transistors couches minces verticaux, silicium polycristallin, dépôt chimique en phase vapeur à basse pression, gravure plasma

Abstract

This work deals with the development of vertical thin film transistors (VTFTs) via the fabrication processes and the analysis of the electrical characteristics. The low-temperature ($T \leq 600°C$) polycrystalline silicon technology is adopted in the fabrication processes. The first step of the work consists in the fabrication and characterization of VTFTs obtained by rotating the lateral thin film transistors (LTFTs) 90°. The feasibility of VTFTs fabrication is validated with an I_{ON}/I_{OFF} ratio of about 10^3, and it is analyzed that the large overlapping area between source and drain leads to a large off-current I_{OFF}. The second step of the work lies in the partial suppression of the large overlapping area, and therefore, an I_{ON}/I_{OFF} ratio of almost 10^5 is obtained. The third step of the work deals with the proposal of a new VTFT structure that absolutely eliminates the overlapping area. Different improvements have been made on this new VTFT structure, especially by optimization of the following parameters: the active layer thickness, type and thickness of the barrier layer, and the geometric dimension. The optimized transistor highlights an I_{ON}/I_{OFF} ratio of higher than 10^5 with a reduced off-current I_{OFF}, high stability and good reproducibility. P and N-type VTFTs have also been fabricated and showed symmetrical electrical characteristics, thus they are suitable for CMOS-like VTFT applications.

Key words: vertical thin film transistors (VTFTs), polycrystalline silicon, low pressure chemical vapor deposition (LPCVD), plasma etching