Etude de fiabilité des jonctions tunnel magnétiques pour applications à forte densité de courant

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Magnetic Tunnel Junction Reliability Study for High Current Density Applications

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To my dear Family !

إلى عائلتي العزيزة !

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Outline

General Introduction

Context and motivation

Nowadays, magnetic tunnel junctions (MTJs) are being extensively studied because they constitute the key elements in a variety of Spintronic devices such as hard-disk-drives read-heads, spin-transfer oscillators and Magnetic Random Access Memories (MRAM). In both Thermally Assisted MRAM (TA-MRAM) and Spin-Transfer-Torque RAM (STTRAM), the tunnel barrier is exposed to a voltage stress in the range of 0.4-0.7V at each write event. Considering that the tunnel barrier thickness is of the order of 1nm and that common oxides experience electrical breakdown when exposed to electrical field larger than 10^9V/m, the MTJ barrier electrical reliability has to be thoroughly investigated. The write endurance in MTJs has already been studied by several groups by time-to-dielectric-breakdown experiments. Different breakdown phenomena have been observed depending on oxide layer thickness, junction resistance area product (RA), and junction area. However, the mechanism and main cause of barrier breakdown in MTJ systems is not yet fully understood, especially when the thickness of the oxide tunnel barrier gets in the range of 1nm-1.4nm. The aim of our research during my thesis was to study MgO-based MTJ breakdown mechanism under pulsed conditions to well understand the phenomena of barrier breakdown in MTJ systems.

Manuscript Organisation

An overview of Spintronic history and domain applications is presented in the first chapter to explain the general context of our research. A more detailed introduction of Magnetic Tunnel Junction and MRAM application is also presented in the first chapter. We outline after that the MTJ electrical reliability issues and we define our thesis objectives which we have focused on during our study.

Lots of studies have been conducted on the reliability of CMOS oxides but not so many in MTJs reliability field. We will benefit in our study from the know-how acquired on this topic.The second chapter treated the previous works done and investigated before to study the oxide thin film electrical reliability. We will show the essential statistical analyses adopted in such study. We will introduce the Weibull distribution usually applied in reliability studies and we will explain the most known failure models in CMOS technologies. We will try also to discuss the breakdown physics and the CMOS reliability characterization techniques. In continuity with these CMOS reliability studies we will discuss the already published results on breakdown mechanisms in aluminum oxide and magnesium oxide based Magnetic Tunnel Junctions.

These two first chapters represent the background of our own investigations.

This know-how will be adopted in the third chapter. An experimental time dependent dielectric breakdown study will be presented and a charge trapping-detrapping model will be developed to explain the observed MTJ breakdown mechanisms. In this section, we will start by explaining the samples preparation and the experimental procedure. Then, we will present the experimental results. We will study the influence of the delay between pulses effect on MTJs endurance for different resistance area product (RA), different pulse durations, different pulses polarities and different pillar sizes. Finally, we will interpret these results and will

detail the model that we have developed. A good consistency between our experimental results and our model will be shown.

In the fourth chapter, we will start by introducing the different noise sources in electronics and then we will show a correlation between the amplitude of 1/f noise of *unexercised* MTJs (*before* any electrical stress is applied) and the MTJ endurance (breakdown *after* applying a large number of electrical pulses). This confirms the expectation that a larger number of defects, inducing earlier breakdown, should correspond to a larger amount of fluctuators contributing to larger 1/f noise amplitude. This chapter confirms that the 1/f noise test could be a predictive tool of barrier quality and the corresponding MTJ endurance.

Finally, after concluding our work and outlining the most important results, we will discuss the thesis perspectives and we will propose some measurements that could be completed to further investigate this charge trapping-detrapping model. An optimization of MgO barrier could be carried out to reduce the density of these trapping sites. Hence, the endurance could reach the extremely high values that we observe in the optimum delay conditions.

Chapter I. Introduction and Thesis Objectives

Content

I.1 An overview of Spintronics

I.1.1 Definition:

Spintronics, a contracted name for spin-electronics started in 1988 with the discovery of Giant Magnetoresistance in magnetic multilayers. Since then, this field has kept growing up with strong synergy between basic research and applications particularly in the field of data storage.

I.1.2 History:

Spintronics aims at using the spin of the electrons in addition to their charge to obtain new phenomena and use these phenomena in innovative electronic devices with improved performances or new functionalities. But the integration of magnetism into semiconductor based circuits is a real challenge.
Ninety years ago, theoretical physicists had a problem: It was a lack of mathematical description of elementary particles. In 1927, Erwin Schrödinger had written down the quantum mechanical equation of motion for the electron, but without taking into account the relativistic character of electrons particles. After one year of research, Paul Dirac has found his well-known equation which was a mathematical *tour de force*, predicting two totally unexpected physical phenomena.
The first finding was the existence of antiparticles as well as particles. This finding was proved in 1932 by the discovery of the positron (an anti-electron). The second discovery was that the electron must have a second degree of freedom, an intrinsic angular momentum or "spin" that has only two possible projections in an applied magnetic field: aligned with the field, or "up"; and anti-aligned, or "down".
Whereas conventional electronic devices rely on only controlling the flow of charge, a "spintronic" device would also control the flow of electron spins (the so-called spin current) within the device, thereby adding an extra degree of freedom.
Over the past 20 years, spintronics has now become a broad field of research merging magnetism and electronics. It now encompasses very different area of research with perspectives of short or long term applications.

I.1.3 Breakthroughs:

Spinelectronics has already found applications outside the semiconductor industry. Metal-based spintronic devices can be found in the hard disks of virtually every computer on the planet. In 1988 Peter Grünberg at the Research Centre Jülich in Germany and Albert Fert at the Université Paris-Sud in France independently discovered that the flow of spin-polarized electrons between two thin layers of ferromagnetic metal separated by a layer of non-magnetic metal can vary by about 50% by changing the relative magnetic alignment of the ferromagnetic layers from antiparallel to parallel. This discovery earned them the 2007 Nobel Prize for Physics. This Giant MagnetoResistance (GMR) made it possible for the magnetic read heads of hard disks to be much more sensitive to changes in magnetic fields, which boosted storage capacity by allowing information to be stored in much smaller regions on the disks' surface. The ability to transport electron spins between two metals also underpins magnetoresistive random access memory (MRAM) — a novel type of computer memory that

can retain information without requiring any power. MRAM is based on a similar effect to GMR known as tunnel magnetoresistance (TMR), which arises when two layers of ferromagnetic metal are separated by a thin layer of insulating material, such as aluminum oxide or magnesium oxide. Instead of the spin-polarized electrons diffusing slowly from one ferromagnetic layer to the other as happens in GMR, in TMR they tunnel quantum mechanically through the barrier layer therefore these devices are called magnetic tunnel junctions (MTJs).

I.2 Magnetic Tunnel Junction

Presently, most of our computers use silicon-based devices to temporarily store the information necessary for the microprocessor's operations. These devices, mostly Static Random Access Memories (SRAM) and Dynamic Random Access Memories (DRAM), allow a fast access to information but rely on electrical power to sustain the data, which means that all information is lost as the power is switched off. This is the characteristic of a volatile memory

FLASH memories are non-volatile memories used typically in USB keys and cell phones, but they are limited in the number of write cycles they can perform, typically 10^4- 10^6.

A new concept of memory, that combines non-volatility, low power consumption and fast read and write cycles with no theoretical limitation, is emerging. These new memories, that integrate a magnetoresistive device with a silicon based selection matrix, are called Magnetic Random Access Memories (MRAM).

The properties of these devices make them potential alternatives to the currently used memory types in specific applications [I.1]. These MRAM devices are basically composed of Magnetic Tunnel Junctions.

I.2.1 Brief History and Fundamentals of MTJ:

A Magnetic Tunnel Junction consists of two ferromagnetic layers separated by a tunnel barrier. Its resistance depends on the relative orientation of the two magnetization directions of the two magnets due to spin-dependent tunneling involved in the transport between the majority and minority spin states. This resistance change is called tunnel magnetoresistance (TMR), and is defined as:

$$\frac{\Delta R}{R} = \frac{R_{AP} - R_P}{R_P} \qquad \text{(I-1)}$$

where R_{AP} and R_P are the resistance for antiparallel (AP) and parallel (P) magnetization configurations between the two ferromagnets (Figure I-1),respectively.

The first experimental results of tunnel magnetoresistance TMR were obtained by Julliere in 1975 at room temperature in an Fe/Ge/Co junction with 14% [I.1] TMR ratio.

Many works had succeeded after to observe the magnetoresistance in Ni/NiO/(Ni, Fe, or Co) junctions at 1980 [I.2] and in 1995 on amorphous Al-oxide (Al-O)-barrier MTJs [I.3], [I.4] at room temperature showing a TMR ratios of over 10%. Many investigations were done since this observation to improve the aluminum oxide based MTJs barrier properties. From 1995 to 2005, the studies succeded to ameliorate the TMR ratio as shown in (Figure I-2) from 10% to 70% which represented the limit of Julliere's formula [I.1], [I.5].

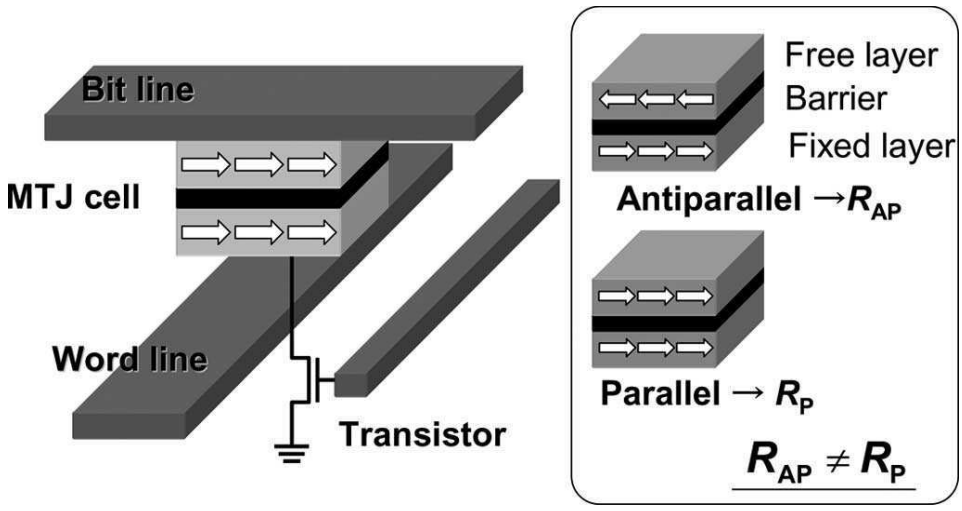

Figure I-1. Schematic diagram of a one MTJ–one Tr MRAM cell. The bit-line and the word-line currents together generate a magnetic field high enough to write a cell. For read operation, the bit-line and the (word) line connected to the Tr is used. Spin-injection write (see text) uses current passing through the MTJ; thus, it does not need the word-line. Right figure shows the two states of an MTJ. Free layer is the layer in which information is recorded. Fixed layer is engineered not to change its magnetization direction. A P magnetization configuration between the free layer and the fixed layer results (usually) in a low-resistance (R_P) state, while an AP configuration results in a high-resistance (R_{AP}) state.

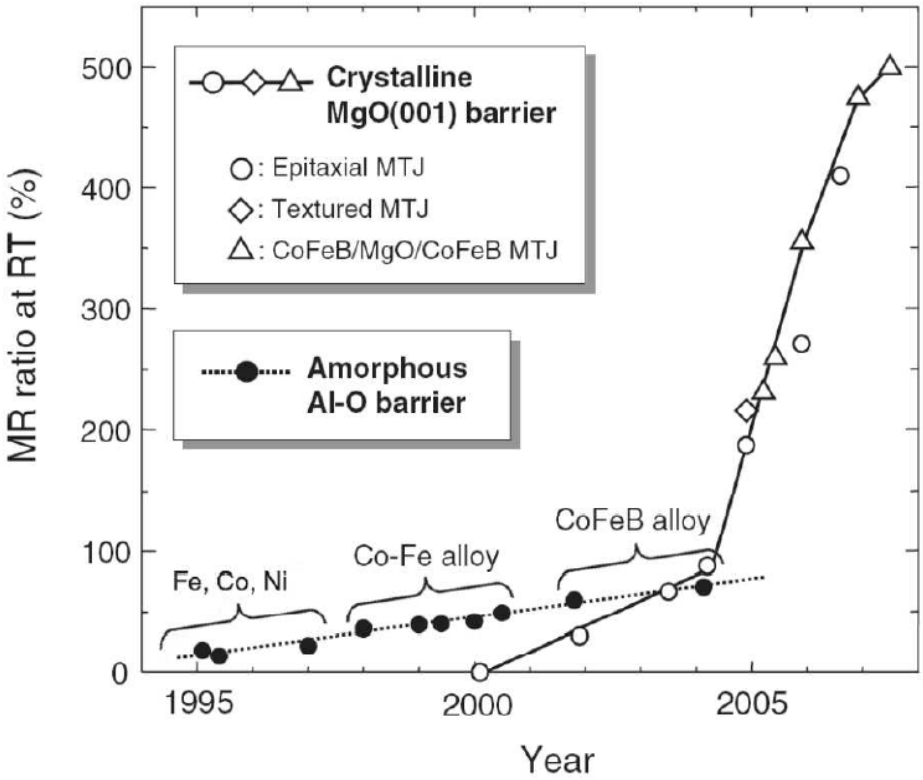

Figure I-2. Temporal evolution of TMR with different typologies of FM electrodes and crystallographic structures of alumina and magnesia tunnel barriers; adapted from [I.14].

A number of technologies have also been developed during the process of increasing the TMR ratio. These include for example spin-valve structure for stabilization of the AP

configuration [I.6], optimization of ferromagnetic–electrode materials [I.7], [I.8]–[I.10], magnetic-field annealing [I.11], oxidization method [I.12], [I.13] and etching technique.
A typical unit structure of one MTJ–one Tr cell for MRAM is schematically shown in (Figure I-1). A modern MTJ has a spin-valve structure (the layer stack, not shown in (Figure I-1), which fixes the magnetization direction of one of the ferromagnetic layer by the use of exchange interaction between the ferromagnetic layer and the neighboring antiferromagnetic layer; thus, the fixed layer is also called as the reference layer.
The other ferromagnetic layer, called the free layer, is the layer that changes its magnetization direction according to the input field/current and stores information. Which of the top or bottom layer is fixed depends on the specific design of an MTJ.

I.2.2 Julliere's model and spin polarization:

Julliere proposed a simple phenomenological model, in which the TMR effect is due to spin dependent electron tunneling [I.15]. According to this model the MR ratio of an MTJ can be expressed in terms of the spin polarizations *P* of the ferromagnetic electrodes

$$MR = \frac{2P_1P_2}{(1 - P_1P_2)} \tag{I-2}$$

Where

$$P_\alpha = \left[\frac{D_{\alpha\uparrow}(E_F) - D_{\alpha\downarrow}(E_F)}{D_{\alpha\uparrow}(E_F) + D_{\alpha\downarrow}(E_F)}\right] \qquad \alpha = 1,2 \tag{I-3}$$

Here $P\alpha$ is the spin polarization of a ferromagnetic electrode, and $D\alpha\uparrow(E_F)$ and $D\alpha\downarrow(E_F)$ are, respectively, the densities of states (DOS) of the electrode at the Fermi energy (E_F) for the majority-spin and minority-spin bands (see (

Figure I-3)).
In Julliere's model spin polarization is an intrinsic property of an electrode material. When an electrode material is NM, $P = 0$. When the DOS of the electrode material is fully spin-polarized at E_F, $|P| = 1$.

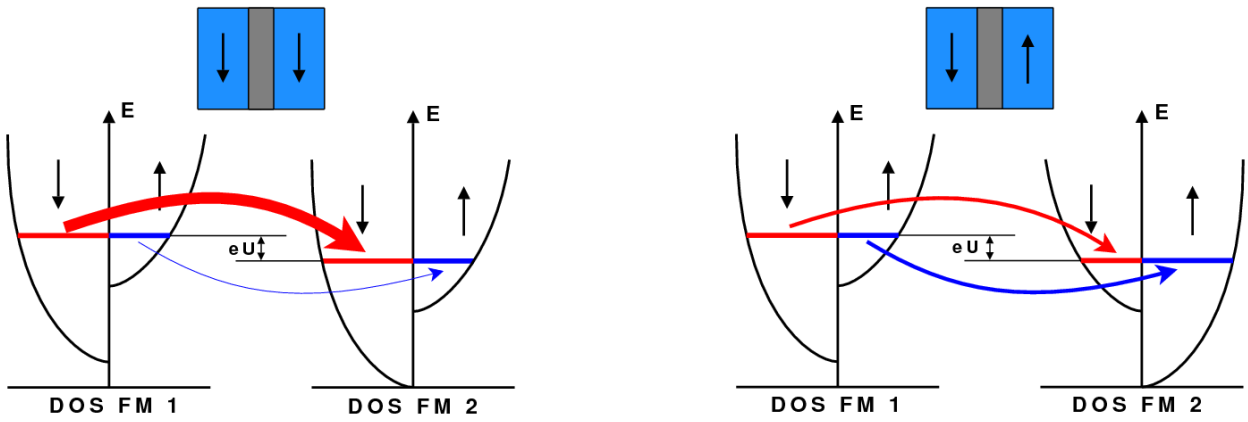

Figure I-3**.** Schematic illustration of the TMR effect in a MTJ. (*a*) Magnetizations in the two electrodes are aligned parallel (P state). (*b*) Magnetizations are aligned antiparallel (AP state). *D*1↑ and *D*1↓, respectively, denote the density of states at *E*F for the majority-spin and minority-spin bands in

electrode 1, and $D_2\uparrow$ and $D_2\downarrow$ respectively denote the density of states at E_F for the majority-spin and minority-spin bands in electrode 2.

The spin polarization of a ferromagnet at low temperature can be directly measured using ferromagnet/Al–O/superconductor tunnel junctions [I.16].
Measured this way, the spin polarizations of 3d ferromagnetic metals and alloys based on iron (Fe), nickel (Ni) and cobalt (Co) are always positive and usually between 0 and 0.6 at low temperatures below 4.2K [I.16], [I.17]. The MR ratios estimated from Julliere's model (equation (I-2)) using these measured P values agree relatively well with the MR ratios observed experimentally in MTJs (Figure I-4), but the theoretical values of P (equation (I-3)) obtained from band calculations do not agree with the measured spin polarizations and the MR ratios observed experimentally (Figure I-4).
Even the signs of P often differ between theoretical values and experimental results.
One way to obtain a MR ratio significantly higher than 70% at RT is to use as electrodes special kinds of ferromagnetic materials called half metals, which have a full spin polarization (|P| = 1) and are therefore theoretically expected to give MTJs huge MR ratios (up to infinity, according to Julliere's model).

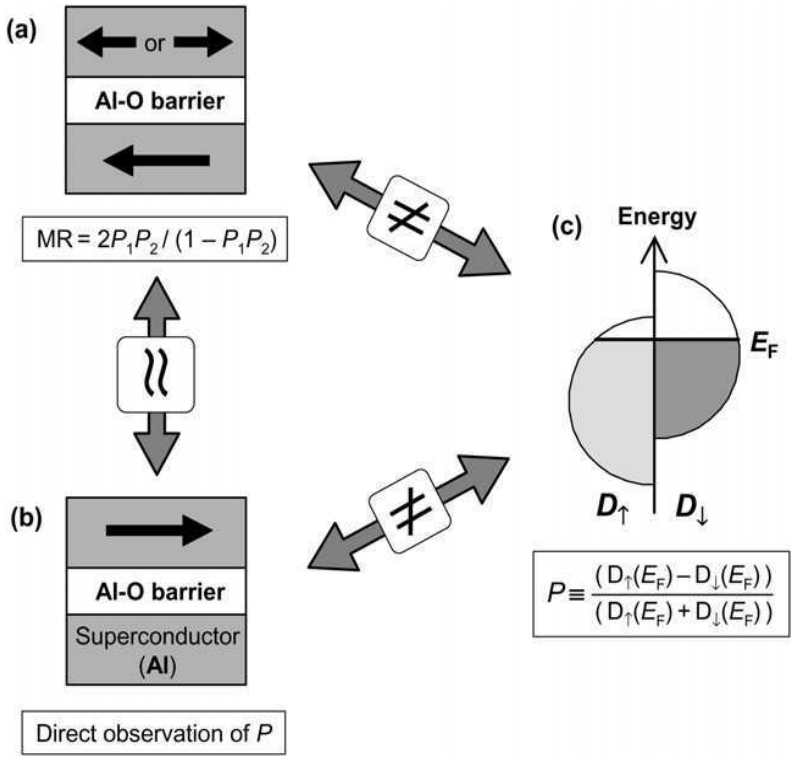

Figure I-4. [I.14] (a) Estimation of spin polarization (P) from the observed MR ratio by using Julliere's model. (b) Direct measurement of P by using ferromagnet /Al–O/superconductor tunnel junction. (c) Theoretical definition of P.

At low temperature, very high MR ratios, above several hundred percent, have been obtained in $La_{1-x}Sr_xMnO_3/SrTiO_3/La_{1-x}Sr_xMnO_3$ MTJs [I.18] and Co_2MnSi/Al–O/Co_2MnSi MTJs [I.19]. However, at RT such high MR ratios have never been observed for half metal electrodes [I.3]. To obtain a very high MR ratio, there is another way, it is to use coherent spin-dependent tunnelling in an epitaxial MTJ with a crystalline tunnel barrier such as MgO (001).

I.2.3 From amorphous Al–O barrier to crystalline MgO (001) barrier:

Since the discovery of room-temperature TMR in 1995, MTJs with an amorphous aluminum oxide (Al–O) tunnel barrier have been studied extensively. Such MTJs exhibit a magnetoresistance (MR) ratio of several tens of percent at room temperature (RT) and have been applied to magnetoresistive random access memory (MRAM) and the read heads of hard disk drives. MTJs with MR ratios substantially higher than 100%, however, are desired for next-generation spintronic devices. In 2001, first-principle theories predicted that the MR ratios of epitaxial Fe/MgO/Fe MTJs with a crystalline MgO(001) barrier would be over 1000% due to the coherent tunneling of specific Bloch states. In highly textured materials, the different tunneling mechanisms and symmetry-related decay rates of the Bloch waves for the majority and the minority spin channels should lead to very high TMR ratios. The first experimental results were obtained in an original work by Bowen et al. [I.20] on single-crystalline Fe/MgO/FeCo(001). Then, the filtering effect has been experimentally shown by Faure-Vincent et al. [I.21],[I.22]. With the same Fe/MgO/Fe (001) multilayer, but deposited by MBE on single crystalline MgO substrate, they obtained a tunnel magnetoresistance up to 100% at room temperature. More recently, also by using MBE growth of single-crystal Fe/MgO/Fe(001) structure, Yuasa et al.[I.23] have measured a TMR up to 250% at low temperature and 180% at RT. Simultaneously, TMR of 300% at low temperature and 220% at RT have been achieved after thermal annealing, by Parkin et al. [I.24] for CoFe/MgO/CoFe polycrystalline MTJ, deposited by sputtering. Moreover, with CoFeB/MgO/CoFeB MTJ grown by sputtering in which the MgO barrier is (001) textured but CoFeB amorphous, Djayaprawira et al. [I.25] found a TMR of 300% at low temperature and 230% at RT.

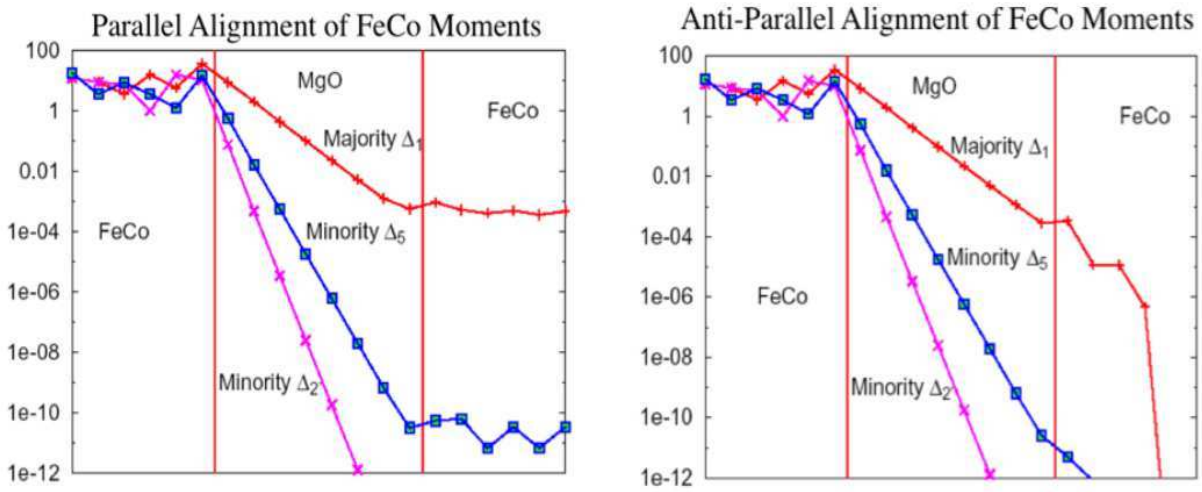

Figure I-5. Tunneling density of states on each atomic layer at Fermi level for a FeCo/MgO/FeCo junction. Left panel: parallel spin alignment, right panel: antiparallel spin alignment.

In order to better understand the origin of the higher TMR values obtained with MgO crystalline barrier compared to amorphous AlOx, we can look at the density of states in the FeCo/MgO system for both cases of parallel and antiparallel alignment of the magnetic layers presented in Figure I-5. In the case of parallel alignment we can see that electrons of Δ_1 symmetry exist at Fermi level just for majority electrons, and readily enter into the MgO and decay slowly inside MgO. So bcc (001) FeCo acts as an half metal for this symmetry. Since there is no present Δ_1 symmetry at Fermi level for the minority electrons, the conduction is dominated by Δ_5. In the antiparallel case the conduction is based on Δ_5 symmetry, since there are no Δ_1 states symmetries present at

the Fermi level for minority electrons. The difference between the highly conductive parallel state (through Δ_1 channel) and the almost insulating antiparallel state (through Δ_5 channel) results in a huge TMR.

I.3 Spintronic devices and applications :

The most important applications developed in spintronics are here presented (see (Figure I-6)):

(1) Magnetic Field Sensors, for example read-head sensors installed in commercial hard disks (HD);
(2) Magnetic Random Access Memories (MRAMs), realised with magnetic tunnel junctions, available as 16 Mb chips with 180 nm scale technology [I.30]. These memories can be written either by pulse of magnetic field or taking advantage of the spin transfer torque phenomenon.
(3) Spintronic Logic Devices, which may be based either on metals or on semiconductors; the difference between the two categories resides in the technology used to process them, which is not compatible, and in the fact that metal-based devices cannot amplify neither a charge transfer signal nor a spin transfer signal; some examples are given: the field effect spin transistor or Datta-Das transistor [I.26], the all-metal spin transistor or Johnson transistor [I.27], the hot electron spin transistor [I.28] and the spin-valve [I.29];
(4) Microwave spin transfer torque nano-oscillators, devices in which a precessional mode of the magnetisation of a FM thin film is stabilised by the injection of a high density DC current and a microwave electromagnetic signal is emitted, often in the GHz range, with remarkable tuning properties of the emitted wave [I.31].

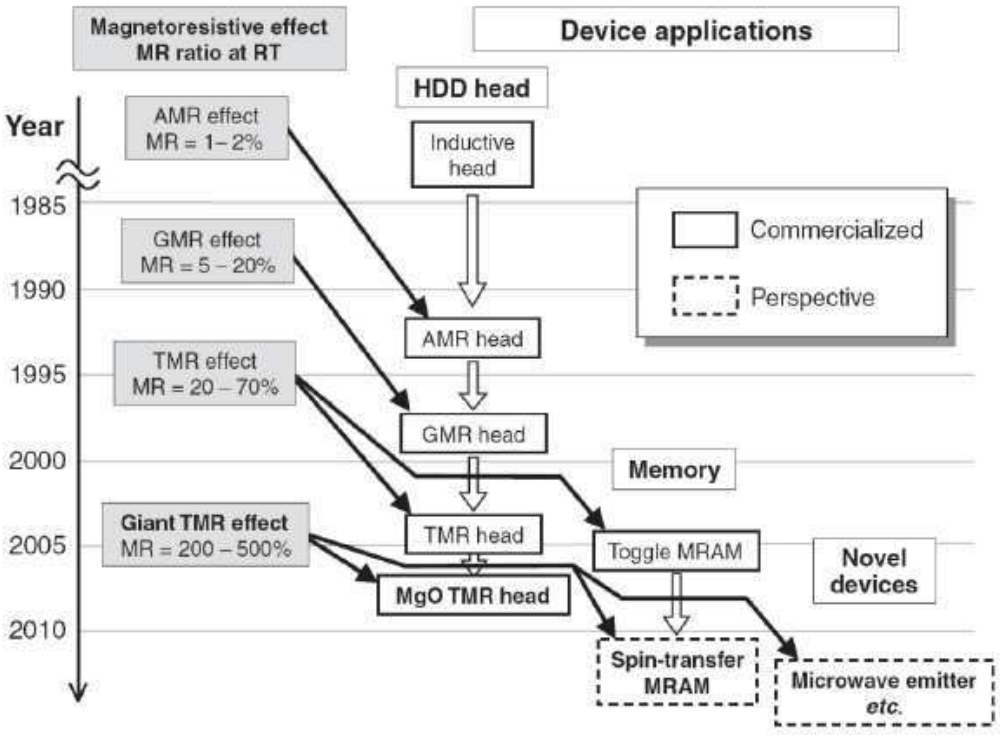

Figure I-6. Temporal evolution of magnetoresistive devices, adapted from [I.14].

Starting from actual commercial applications that propose significant advantages over other available technologies, spintronic devices are addressing perhaps the most important computer subsystems: random access memories and high density non-volatile storage media.
Straightforward applications will be represented by spin-based transistors and logical gates, as soon as new materials will be successfully experimented and the silicon technology will be adapted to spintronic devices. The use of spin currents in semiconductors thanks to spin-orbit coupling will enable dissipationless device operation [I.32], overcoming one of the greatest physical limits against size scaling, the power density growth. The road towards all-semiconductor spintronic devices goes through hybrid devices, like the hot electron transistor prototype which is composed by a tunnel barrier emitter, a semiconductor spin transport layer, a metallic spin filter and a semiconductor collector.

I.4 Magnetoresistive Random Access Memories:MRAM

I.4.1 Introduction:

Magnetoresistive Random Access Memory, or MRAM, shows promising potential for commercial competition among universal memory [I.33]. Existing semiconductor memories all have shortcomings and limitations, and cannot fulfill all the important attributes needed for memory with one solution. MRAM, however, possesses all of these key features. It is the only non-volatile, non charge-based, non destructive memory currently in production.
Magnetic random access memories (MRAMs) integrate a magnetoresistive device with a silicon-based selection matrix. The key attributes of MRAM are non-volatility, low voltage operation and unlimited read and write endurance combined with fast read and write operation. These characteristics give MRAM the potential to replace current memory types in specific applications. The interest in MRAM started some 40 years ago with a cross-tie RAM concept [I.34], followed by the use of the anisotropic magnetoresistance (AMR) materials [I.35], later replaced by higher sensitivity giant magnetoresistance (GMR) devices [I.36] and more recently using spin dependent tunnel junctions [[I.37]-[I.39]].
The MRAM development effort was renewed after the first successful attempts in fabricating spin dependent tunnel junctions showing significant magnetoresistance as mentioned before at room temperature using amorphous AlO_x barriers [[I.40], [I.41].]. Recent studies previously mentionned using crystalline MgO barriers have shown that it is possible to increase the available magnetoresistive signal to more than 200% resistance change at room temperature [[I.42], [I.43].]. In its most simple implementation, an MRAM cell is composed of a magnetic tunnel junction (MTJ) connected to a selection transistor.

I.4.2 Architecture and operation of different MRAM technologies:

I.4.2.a Field written MRAM:

In the memory cells of the first generation of MRAM, the writing of information is done by magnetization reversal of the free layer through the magnetic fields induced by the currents flowing through the lower conductive lines (bit line) and higher (Wordline) orthogonal to each other. This combination of two magnetic fields ensures the write selectivity between the bits of the memory array. The writing is performed by applying a magnetic field with an angle of 45° to the anisotropy axis of the free layer. It is in this configuration that the reversal field

is minimal according to the Stoner-Wolfarth model. Reading is performed by applying a voltage across the MTJ to measure its resistance. The resistance of the memory bit is either low or high depending on the magnetization orientation of the free layer relatively to the pinned reference layer, parallel or antiparallel. To read one bit, the selection transistor is turned on, and a read current flows through the tunnel junction as shown in Figure I-7.
Finally, the nanopillars are elliptical to provide sufficient shape anisotropy to ensure bistability of the magnetization of the free layer.

Table I shows the features of MRAM compared to several other major memory technologies. The key attributes of MRAM technology are shown in this table. They mainly consist in nonvolatility combined with high-speed operation and effectively unlimited read-write endurance.

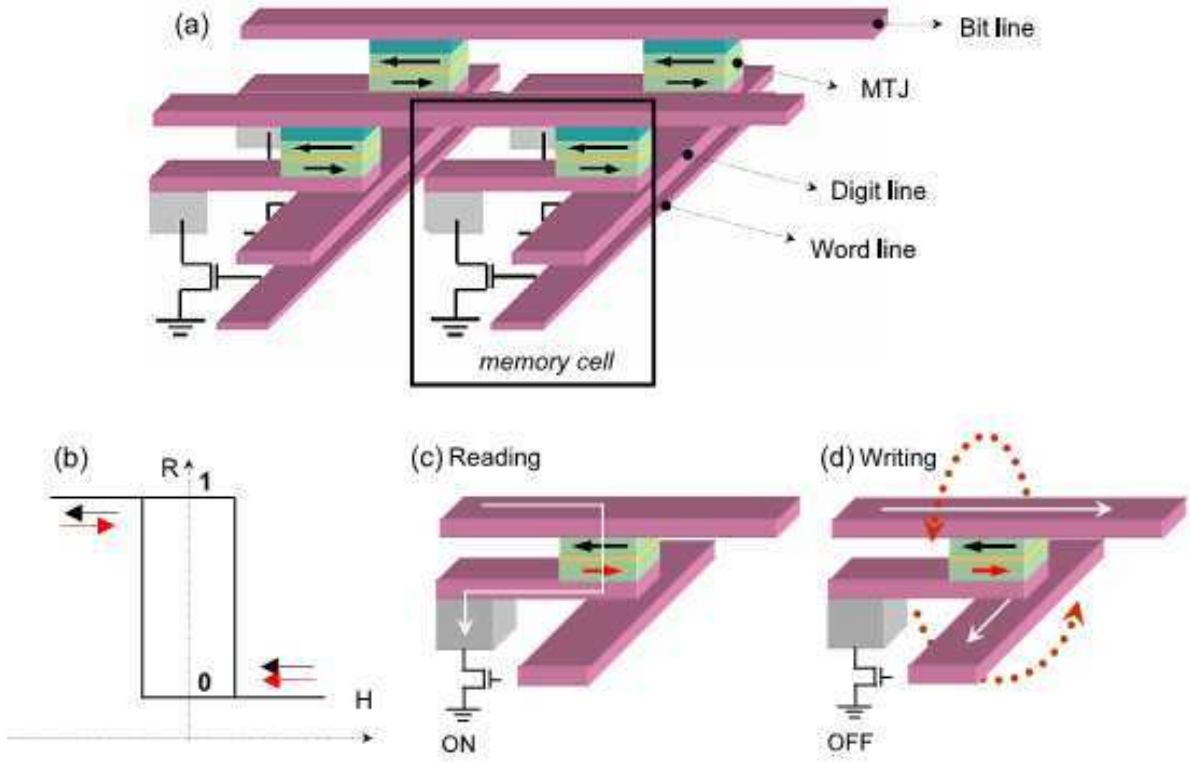

Figure I-7: [I.44] (a) Architecture used in the first field written MRAM generation consisting of MTJ cells at the intersection of orthogonal writing lines (bit and digit lines) patterned on top of an array of selection transistors. (b) Schematic view of a minor hysteresis loop showing the reversal of the storage layer and two corresponding resistance levels: high ‘1’ and low ‘0’. Reading (c) and writing schemes (d) used in the conventional MRAM architecture. At read, the selection transistor is closed (on) and a small electrical current can pass through the MTJ cell, allowing the measure of its resistance. At write, the selection transistor is open (off) and the combination of two orthogonal magnetic fields ensures the selectivity.

Table I. Comparison of MRAM Expected Features With Other Memory Technologies[a]

	SRAM	DRAM	FLASH	FRAM	MRAM
Read	Fast	Moderate	Fast	Moderate	Moderate-fast
Write	Fast	Moderate	**Slow**	Moderate	Moderate-fast
Nonvolatile	**No**	**No**	Yes	**Partially**[b]	Yes
Endurance	Unlimited	Unlimited	**Limited**[c]	**Limited**[b]	Unlimited
Refresh	No	**Yes**	No	No	No
Cell size	**Large**	Small	Small	Medium	Small
Low voltage	Yes	Limited	**No**	Limited	Yes

[a]Bold letters indicate undesirable attributes.
[b]Destructive read and limited read/write endurance.
[c]Limited write endurance.

Each of the existing technologies provides particular functional advantages, but with some significant shortcomings as well. As such, none are suitable as a "universal memory" that would provide desirable performance for all of the most important memory attributes. As can be seen in the table, MRAM possesses the nonvolatility, endurance, speed, and density necessary to function as a universal memory.

I.4.2.b Thermally assisted MRAM (TA-MRAM):

The thermal stability, write selectivity and power consumption was a real challenge in MRAM applications [[I.45]–[I.47]]. A new write approach, called thermally assisted switching (TA-MRAM), was thus recently proposed.
Heating had already been previously proposed to write the bit state of tunnel junctions by circulating a current in the write lines [[I.48]–[I.50]] and heating the magnetic layers in the MRAM cell above their magnetic ordering temperature, greatly reducing the write fields. The first designs proposed use a low Curie point ferromagnetic material as the storage layer [[I.48], [I.49]]. The bit is heated close to the Curie temperature and a small magnetic field generated by the digit line sets the write direction. Another design employs the exchange coupling between an antiferromagnet (AF) and a ferromagnetic (FM) layer as the storage mechanism [I.51]. The two films are heated above the Néel temperature of the AF layer and written by cooling down in the presence of a magnetic field. In this design, two orthogonal current lines are used to heat the cell and generate the write field. The coincident heating from two lines can be used to select one cell for thermal writing. The main disadvantage of such write architectures is that the heating is indirect and relies on heat diffusion, meaning high power consumption and long write cycles. A better approach to TA-MRAM [[I.50], [I.51]] is to heat directly with the current flow through the MTJ, after turning the selection transistor ON during the write procedure (see Figure I-12 (b)). Since the heat is generated locally inside the junction this is a more efficient solution than the indirect diffusive heating.
An efficient way to implement this thermally assisted write approach in in-plane magnetized MTJ consists in using a bilayer ferro-antiferromagnetic storage layer [I.51]. Indeed, in such structure, the energy required to return a bit is given by:

$$E \approx K + (AR-1) \times \left(\frac{t}{L}\right) \times M_S^2 + \frac{J_{eb} \times M_S^2}{t} \times \left(1 - \frac{T}{T_B}\right) \qquad \text{(I-4)}$$

The first two terms are common to all in-plane magnetized MRAM concepts. They represent the magnetocristalline anisotropy and shape anisotropy. In contrast, the latter term is specific to the TA-MRAM and shows a strong dependence on temperature. To write this layer, one must apply current through the magnetic tunnel junction simultaneously with the application of a magnetic field through a single line field. The Joule effect at the tunnel barrier heats up the storage layer up to the ferro/antiferro blocking temperature. As a result, the magnetization of the ferromagnetic layer gets unpinned. The magnetic field created by the field line becomes greater than the coercive field of the ferromagnetic layer (which is of the order of a few Oersted), so that its magnetization can oriente itself along the applied field. Switching off the heating pulse results in the cooling of the storage layer and pinning of its magnetization in the new direction. The antiferromagnetic will then freeze in the new direction of magnetization imposed by the magnetic field. The reference and the storage layer must be exchange biased at different blocking temperatures. This has multiple advantages and solves the limitations of the conventional MRAM architecture.
This mode of writing is called TAS (for Thermally Assisted Switching). It is at the origin of the creation of start-up Crocus Technology in 2004, whose purpose is to market TA-MRAM.

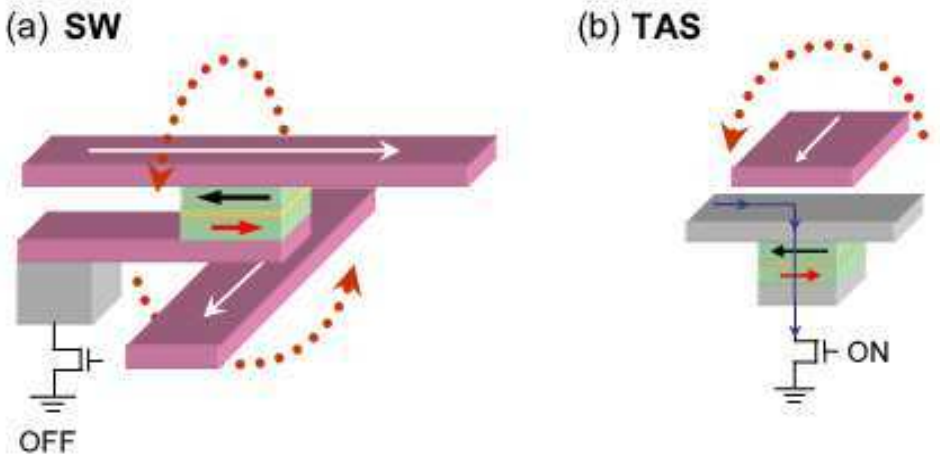

Figure I-8. [I.46] The writing procedure in a conventional MRAM architecture (a) and in the TA-MRAM architecture (b).

I.4.2.c Spin Transfer Torque MRAM (STTRAM)

In field written MRAM, the magnetization of MTJ is switched by the current induced magnetic field. When the size of MTJ scales down, the amplitude of the required magnetic field increases correspondingly. The high write power consumption severely limits the scaling of conventional MRAM.
In 2000, a new write mechanism based on spin polarization current induced magnetization switching, was introduced in MRAM design. This new MRAM design, called spin-transfer torque random access memory (STT-RAM), is believed to have a better scalability than the conventional MRAM. In this new generation of MRAM, the spin polarized current is directly used to reverse the storage layer magnetization by spin transfer torque. This design, called Spin Transfer Torque RAM (STT-RAM), has the advantage of eliminating the need for a field line thus greatly reducing the power consumption when compared with the previously described designs.
Programming the memory bit in STT-RAM is realized by passing electric current through the MTJ elements. The flow direction depends on the state to write. To write a “0”, the parallel

state, the current flows from the reference layer to the storage layer (see Figure I-9) and it flows in the opposite direction to write a “1”, which corresponds to the anti-parallel state.
Due to the need of ensuring a stability of the data of the order of 10 years, a limit in the reduction of size of this type of memory cells was found. This limit has led researchers to pursue research using new configurations. At the moment, the efforts are focusing on STTRAM cells based on out-of-plane magnetized MTJ in which the magnetic anisotropy is larger yielding longer memory retention as well as on designs combining thermal assistance with spin transfer torque switching.

Figure I-9. Schematic of an STT-RAM memory cell.

I.5 MTJ electrical reliability issues

I.5.1 Fabrication problems

The fabrication of the tunnel barrier, and also the pillar fabrication are critical for the final device. Several problems can occur during deposition and processing that cause the memory cell not to function properly. A particularly serious problem is the formation of pinholes in the barrier. A pinhole is a region of the insulating layer where its thickness is so reduced that a short-circuit is created between the two electrodes. If, for example, the layer where the tunnel barrier is to be deposited is too rough, the irregular surface may lead to the creation of pinholes [I.15]. Another possible cause for the formation of pinholes is a change in lattice parameter while the Mg is oxidized to obtain MgO.
The process used to pattern the pillars, to build the memory cells, as described above, sometime involves the use of Ion Beam Etching (IBE). During this phase of the process, ions are accelerated towards the wafer with a defined angle to progressively give shape to the pillars. However, due to the angle of the beam, a part of the removed matter is re-deposited on the walls of the pillars, which acts as a resistance in parallel with the MTJ.
The re-deposition on the side walls creates a path for the current, therefore reducing the resistance of the junction and degrading its TMR. The angle used is also responsible for the creation of a “shadow” around the pillar in the engraving process where the material is not removed. Consequently the dots obtained after patterning will have a diameter larger than the nominal value, the difference being designated by extension.

$$d_{real} = d_{nominal} + extension$$

Another effect that also degrades the TMR of the junction is the serial resistance, associated with contacts and interfaces, which causes an increase of the resistance of the junction but doesn't contribute to its TMR. A simple model of the three resistances involved - the junction, the serial resistance and the shunt created by the re-deposition - and their effects in the value of TMR are presented in Figure I-10.

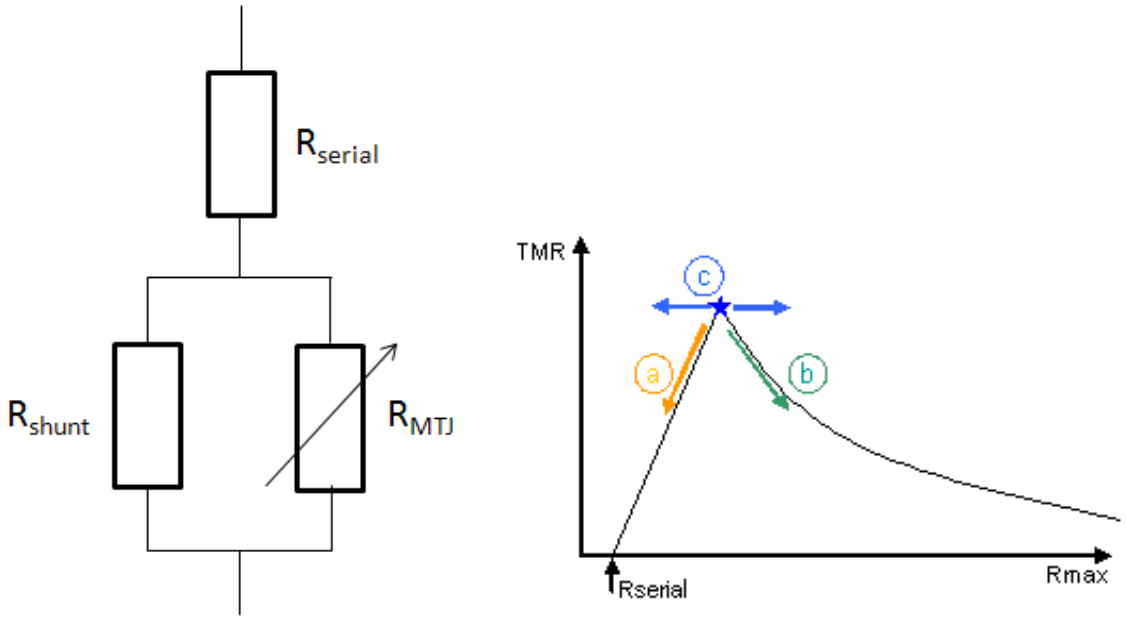

Figure I-10: Simple schematic representation of the three resistances - MTJ, R_{serial} and shunt - and graphical representation of the effect of each resistance. The line corresponding to *a* shows the effect of a serial resistance, *b* corresponds to the effect of shunt and, finally, *c* corresponds to the effect of change in nominal diameter.

I.5.2 Physical issues:

The cyclability of MTJ up to 10^{16} write cycles has already been tested during the development of field induced magnetic switching FIMS-MRAM. These earlier studies have shown that there is no MTJ aging associated with the switching of the storage layer magnetization. This represents a significant advantage over alternative technologies based for instance on ferroelectric or phase change materials. However, this FIMS write mode requires a rather large write current (several mA) and is not scalable below the 65nm node due to ***electromigration*** issues.

For this reason, we want to focus on the spin-transfer torque (STT) write mode. In STT, the magnetization is switched by a bipolar pulse of current flowing through the MTJ. The switching is caused by the torque exerted by the spin-polarized current on the magnetization of the storage layer. The current threshold above which switching takes place is determined by a critical current density j_c depending on the properties of the magnetic material, on its thickness and on the duration of the current pulse. In state of the art junctions, this threshold is in the range 2.10^6-10^7A/cm². STT switching offers a very attractive scalability since the write current scales as the junction area. However, a *drawback* is that at each write event, the MTJ is submitted to an important electrical stress due to write voltage of the order of half of the electrical breakdown voltage (V_{write}~0.4-0.8V whereas $V_{electrical\ breakdown}$~1V-1.6V for 10ns pulse duration).

The cyclability of MTJ in STT write mode has been demonstrated up to 10^{12}cycles but we need to improve it up to 10^{16} cycles for the purpose of many applications. Lots of studies have been conducted on the reliability of CMOS oxides. We benefit from the know-how acquired in the field keeping in mind that however, we are working in totally different conditions (lower oxide thickness, different oxide materials).

The key reliability issues for the Hybrid CMOS/Magnetic Integrated Electronics technology are the following:

- Tunnel barrier lifetime, role of electron trapping sites in the barrier, role of defects due to process.
- Influence of edge defects due to etching on magnetic and transport properties of sub-45nm cells.
- Variability of Resistance x Area product and TMR from cell to cell on multi Mbit chips

I.6 Thesis Objectives:

The field written magnetic random access memories (or MRAM) are already in production while STTRAM are still under development because reliability issues have still to be solved before entering in mass production.
The use of spin transfer torque switching in STTRAM imposes much more stringent constrains in terms of electrical and magnetic properties than in the already demonstrated MRAM application which is based on field induced magnetic switching (FIMS). This is due to the fact that at each write event, the tunnel barrier is exposed to a quite large electrical field which may damage the dielectric properties of the tunnel barrier. This brings a significant risk in memories applications as well as in hybrid CMOS/magnetic non-volatile logic applications using the same technology. STTRAM are envisioned to be able to replace DRAM below the 20nm technology node and moderate speed SRAM (1-5ns access time). For these applications, the cyclability i.e. a **number of write cycles that the device is able to endure must be larger than 10^{16}**. To achieve this goal and reduce the associated risk, the **MTJ resistance to electrical breakdown should be improved. This is the main goal of this thesis.**
To improve cyclability in STT-MTJ up to 10^{16} cycles by improving their resistance to electrical breakdown, we first developed a special procedure to test the resistance of our junctions to electrical breakdown.
We then used this procedure to characterize a large number of MTJ deposited in various sputtering units and under different conditions. This allowed us to get a good basic understanding of the fundamental reliability mechanism in these MTJ Based on a large statistics of measurements.
We then developed a quantitative interpretation of the obtained results based on a charge trapping/detrapping model.
We then searched for a predictive characterization technique allowing to know a priori i.e. before applying any electrical stress on the barrier what will be its write endurance. Based on the know-how on reliability studies in CMOS oxides, we observed a correlation between 1/f noise and endurance.
At the end, based on our understanding of the breakdown mechanism in MTJ, solution to improve the MTJ endurance are proposed.

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Chapter II. Oxide Thin Film Electrical Reliability

Content

II.1 Tunneling in CMOS oxides

II.1.1 Introduction

To understand the physics of CMOS oxides breakdown, we have first to explain the tunneling in this technology. Thus we can look at the example of the metal oxide semiconductor system. In a basic MOS transistor, the channel beneath the gate region is controlled by the voltage on the gate. In an n-channel transistor, a positive voltage on the gate causes the channel to invert, permitting charge flow from source to drain. In a p-channel transistor, a negative voltage on the gate causes the channel to invert, permitting charge flow from drain to source. The voltage across the gate produces an electric field across the dielectric. It is this electric field that we need to understand to determine the reliability of the dielectric.
Figure II-1 shows an energy band diagram depicting the voltage across the dielectric. The electric field across the oxide is given by the simple equation $E=V_{ox} / t_{ox}$. Because today's semiconductor processes use ultrathin gate oxides, the electric field across the dielectric can be quite high. For example, the gate oxide might be 20Å thick on an IC with a 1.5 V power supply voltage. This means that the electric field across the oxide is 7.5 MV/cm. This high electric field requires a high quality gate oxide material to reach the required reliability for applications.

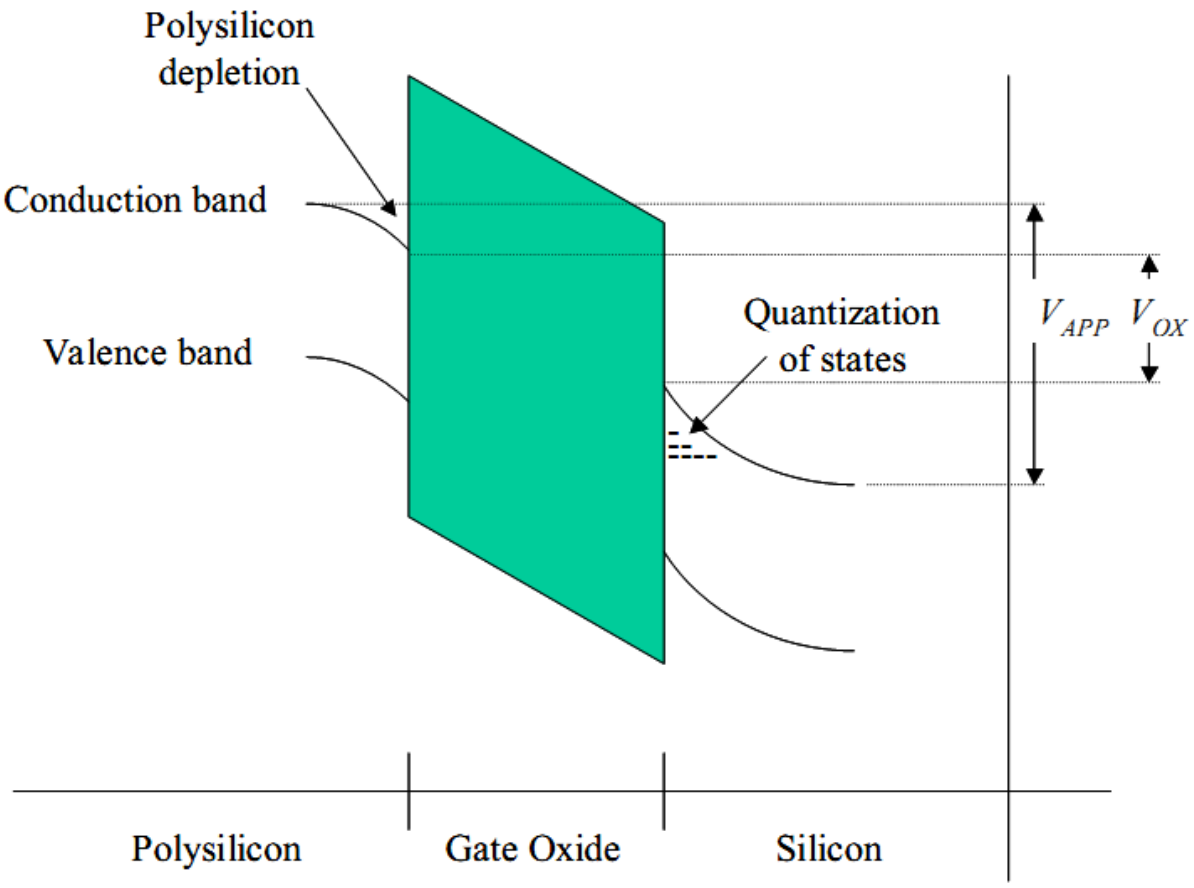


Figure II-1: Energy band diagram for a gate oxide with a large applied electric field. Note that the voltage across the oxide (V_{OX}) is less than the applied voltage V_{APP}.

Not all the voltage drop occurs across the dielectric in a high field situation. There is a voltage drop due to the quantization of states in the silicon, and there is a voltage drop due to depletion of the polysilicon material (see Figure II-1). In a high electric field, the channel region becomes inverted. This means that individual electrons get caught in states immediately adjacent to the interface between the silicon and the oxide. As the states become fully occupied, the valence band and the conduction bands bend. As the field becomes even higher, the states in the polysilicon become depleted, which causes the valence and conduction bands to bend downwards. The net effect of this is to reduce the voltage across the dielectric.
Ideally, an oxide doesn't allow charge to pass through, but this is not the case when the electric fields become high and the oxide becomes thin. There are several mechanisms that allow charge to pass through the oxide: Fowler-Nordeim tunneling, Direct tunneling, and Trap Assisted tunneling.

II.1.2 Fowler-Nordeim Tunneling

Fowler Nordeim tunneling is a quantum mechanical tunneling process which takes place at relatively high voltage. The electrons penetrate through the oxide barrier and are directly injected into the conduction band of the oxide (see Figure II-2). The equation for Fowler-Nordeim tunneling is shown below.

$$J_{FN} = AF_{ox}^2 \exp\left[-\frac{B}{F_{ox}}\right], \text{ where } A = \frac{q^3}{16\pi^2 h \phi_b} \text{ and } B = \frac{4}{3}\frac{(2m_{ox})^{1/2}}{qh}\phi_b^{3/2} \qquad \text{(II-1)}$$

Where Φ_b is the tunnel barrier height, m_{ox} the effective mass of the tunneling electron, q the electric charge and F_{ox} is the electric field.
Fowler-Nordeim tunneling is dependent on the voltage across the gate oxide; it increases exponentially with the applied voltage. Fowler Nordeim tunneling can occur in almost any gate oxide exposed to voltages comparable to the barrier height.

II.1.3 Direct Tunneling

Direct tunneling is also a quantum mechanical tunneling process (see Figure II-2). Direct tunneling is a phenomenon that is important to understand in ultrathin oxides. It occurs when electrons tunnel through the gate oxide region directly from the gate to the channel region. The equation for direct tunneling is shown below.

$$J_D = \frac{AF_{ox}^2}{\left[1-\left(\frac{\phi_b - qV_{ox}}{\phi_b}\right)^{1/2}\right]^2} \exp\left[-\frac{B}{F_{ox}}\frac{\phi_b^{3/2} - (\phi_b - qV_{ox})^{3/2}}{\phi_b^{3/2}}\right] \qquad \text{(II-2)}$$

Direct tunneling is dependent on the thickness of the gate region; it increases exponentially as the thickness of the oxide decreases. Direct tunneling is relatively independent of the electric field across the gate oxide.

II.1.4 Trap Assisted Tunneling

The other tunneling mechanism that can occur in a gate oxide region is trap assisted tunneling. Trap assisted tunneling occurs when electrons tunnel through the oxide into traps (empty bonding sites) and then from the traps into the silicon. Trap assisted tunneling is not easily reduced to an equation since the phenomenon is rather complex. However, it is dependent on the density of the traps and the electric field. A diagram describing trap assisted tunneling is shown below.

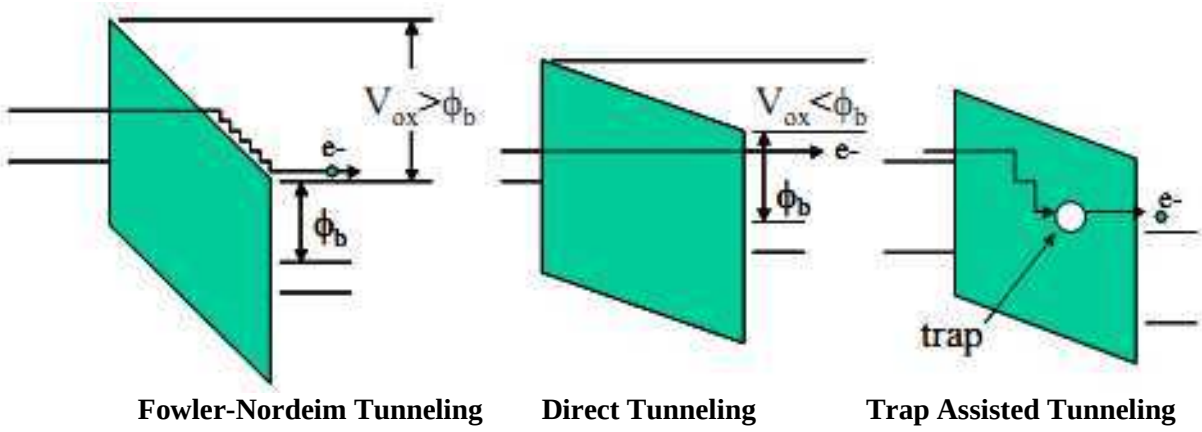


Figure II-2: Diagram showing the concept behind Fowler-Nordeim tunneling (left), Direct tunneling (center) and Trap Assisted tunneling (right).

We understand now the CMOS functionality and how electrons tunnel through the thin gate oxides. As CMOS Tunneling strongly depends on the applied voltage across the gate oxide and also on the oxide thickness, we will focus in next section on reliability analyses and failure models adopted to understand the oxide thin film electrical breakdown which represents a live challenge in Hybrid CMOS/Magnetic Integrated Electronics technology.

II.2 Statistical analysis:

II.2.1 Reliability analyses using Weibull distribution:

Product reliability can be defined using a 4 point list:

- The product does not fail.
- The product maintains its function.
- The product lifetime is achieved.
- The product expectations are met.

In reliability studies, a so-called “bathtub curve” often describes the evolution of device reliability in time. It consists of three distinct periods (see Figure II-3). The first period is called infant mortality period. It is characterized by a few initial failures and subsequently a decrease in the failure rate at the early life of the studied devices. Most of the devices reach

the flat portion of the graph, representing the device normal life. Failures occur in a random sequence. It is not possible to predict when failure will occur, but the rate of failure is predictable. The slope increases, when the devices expected life-time is reached and the failure rate increases rapidly.

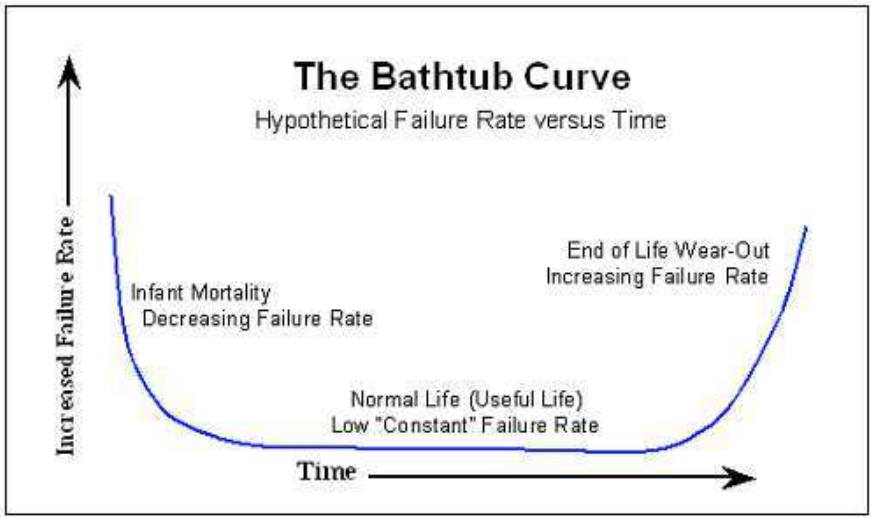


Figure II-3 - Reliability Bathtub Curve.

II.2.1.a Definition (Use ref: Wikipedia):

Reliability is a probability of failure which is predicated on “intended” function. This means that failure is regarded as a random phenomenon taken to mean operation without failure. Reliability applies to a specified period of time which means that a system has a specified chance that it will operate without failure before breakdown. It is restricted to operation under stated conditions as it is impossible to design a system for unlimited conditions. To conclude one can say simply that ***reliability*** is the capacity of a device or system to perform its required functions under stated conditions for a specified period of time.

II.2.1.b Background:

Waloddi Weibull invented the Weibull distribution in 1937 and published his known paper on this subject in 1951. Mathematically, the statistical fundamentals of Weibull and the associated distribution in particular are used to define reliability. Weibull placed particular emphasis on the versatility of the distribution and described 7 examples where it could be applied: life of steel components or distribution of the population physical height.
Today, the Weibull distribution is also used in such applications as determining the distribution of wind speeds in the design layout of wind power stations. The initially disputed Weibull distribution is today recognised as an industrial standard.

II.2.1.c An overview of Weibull Analysis:

The lifetime distributions in reliability are mostly studied and described by a Weibull distribution. It is a universal distribution that can take on the characteristics of other types of distributions, based on the value of the shape parameter, β. This paragraph provides a

description of Weibull distribution through illustration plots. In probability theory and statistics, the Weibull distribution is a continuous probability distribution.

Weibull Probability Density Function:
The probability density function of a Weibull random variable *t* is: [II.1]

$$f(t) = \beta(\frac{t}{\eta})^{\beta-1} \exp(-(\frac{t}{\eta})^{\beta}) \qquad \text{(II-3)}$$

Where $\beta > 0$ is the shape parameter and $\eta > 0$ is the scale parameter of the distribution. Its complementary cumulative distribution function is a stretched exponential function. The Weibull distribution is related to a number of other probability distributions; in particular, it interpolates between the exponential distribution ($\beta = 1$) and the Rayleigh distribution ($\beta = 2$). If the quantity *x* is a "time-to-failure", the Weibull distribution gives a distribution for which the failure rate is proportional to a power of time. The ***shape* parameter**, β, is that power plus one, and so this parameter can be interpreted directly as follows:

- A value of $\beta < 1$ indicates that the failure rate decreases over time. This happens if there is significant "infant mortality", or defective items failing early and the failure rate decreasing over time as the defective items are weeded out of the population.
- A value of $\beta = 1$ indicates that the failure rate is constant over time. This might suggest random external events are causing mortality, or failure.
- A value of $\beta > 1$ indicates that the failure rate increases with time. This happens if there is an "aging" process, or parts that are more likely to fail as time goes on.

In the field of materials science, the shape parameter β of a distribution of strengths is known as the Weibull modulus.
The form of the density function of the Weibull distribution changes drastically with the value of β.

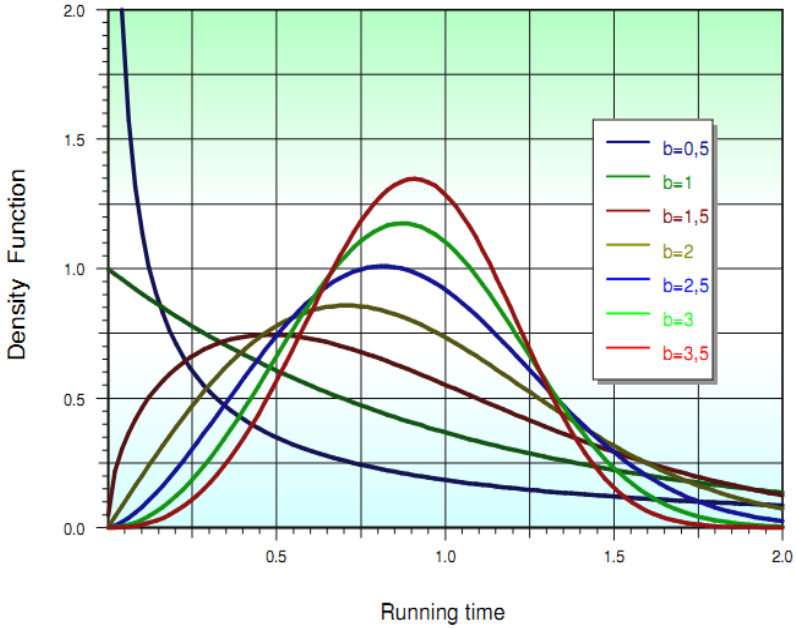


Figure II-4 –Probability density function.

For $0 < \beta < 1$, the density function tends to ∞ as *t* approaches zero from above and is strictly decreasing. For $\beta = 1$, the density function tends to $1/\eta$ as *t* approaches zero from above and is

strictly decreasing. For $\beta > 1$, the density function tends to zero as x approaches zero from above, and exhibits a maximum for an intermediate characteristic time (Figure II-4).

Cumulative Distribution Function:
The Weibull cumulative distribution function is obtained by integration:

$$F(t) = \int_0^t f(t)dt = 1 - \exp\left(-\left(\frac{t}{\eta}\right)^{\beta}\right) \qquad \text{(II-4)}$$

Cumulative failure probability or failure frequency. (Figure II-5).

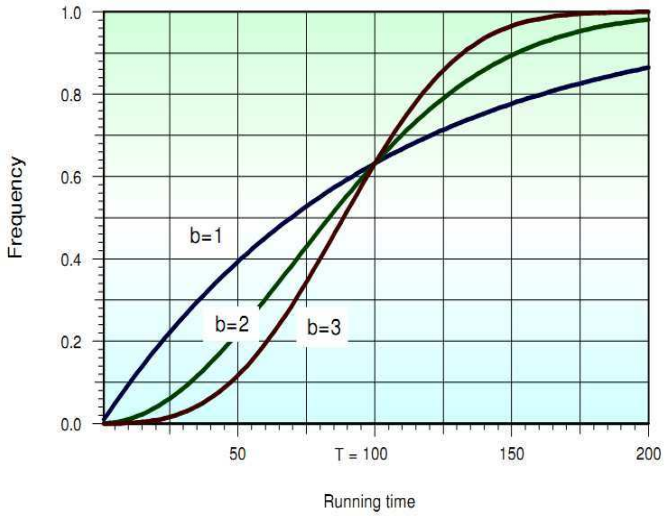


Figure II-5. Cumulative distribution function.

Weibull Plot:

The quality of date fit to a Weibull distribution can be visually assessed using a Weibull Plot [II.2]. The Weibull Plot is a plot of the cumulative distribution function $F(t)$ plotted as $\ln(-\ln(1-F(t)))$ versus $\ln(t)$.
The reason for this change of variables is that the cumulative distribution function can be linearised:

$$\begin{aligned} F(t) &= 1 - e^{-\left(\frac{x}{\eta}\right)^{\beta}} \\ -\ln(1-F(t)) &= \left(\frac{x}{\eta}\right)^{\beta} \\ \ln\left(-\ln\left(1-F(t)\right)\right) &= \beta\ln(t) - \beta\ln(\eta) \end{aligned} \qquad \text{(II-5)}$$

which can be seen to be in the standard form of a straight line. Therefore if the data corresponds to a Weibull distribution a straight line is expected on this type of plot. Linear regression can also be used to numerically assess the fit quality and estimate the parameters of the Weibull distribution. The shape parameter β and the scale parameter η can be extracted.

In chapter 3, when we will represent our experimental results we will fit our data with this Weibull distribution and we will extract the two corresponding parameters: the shape parameter β and the scale parameter η. We will then interpret and discuss these obtained values. We will benefit from this distribution advantages to well understand the MTJs failure.

II.2.1.d Advantages of Weibull Analysis:

The Weibull Analysis are usually used in reliability thanks to its advantages. The most important advantage of Weibull analysis is the possibility to study the failure and the reliability of samples with very different sizes, particularly the ones with a small number of elements. Early indications of a problem can be quickly identified without having to "burn a few more." Small samples also allow for cost effective component testing. For example, "sudden death" Weibull tests are completed when the first failure occurs in each group of devices. If all the devices had to be tested to failure, the time required would be much greater. Another advantage is that it provides a simple and useful graphical plot of the failure data. The data plot is extremely important to analyse and sum up the conclusion. The Weibull data plot is particularly informative as Weibull pointed out in his 1951 paper. (Figure II-6) is a typical Weibull plot.

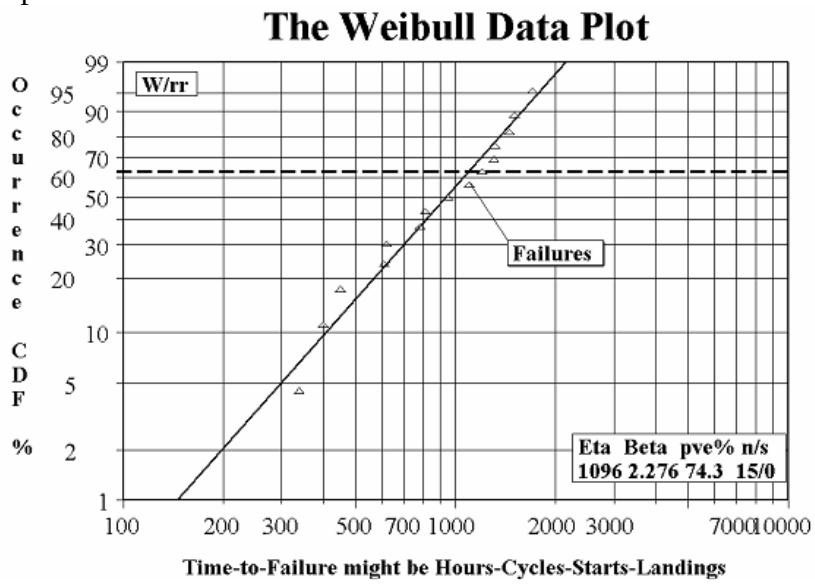


Figure II-6- The Weibull Data Plot.

The horizontal scale is a measure of life or aging. The vertical scale is the cumulative percentage failed. The two defining parameters of the Weibull line are the slope, beta, and the characteristic life, eta. The slope of the line, β, is particularly significant and may provide a clue to the physics of the failure. The characteristic life, η, is the typical time to failure in the Weibull analysis.

II.2.2 Statistics and Physics of Breakdown:

The statistics associated with the breakdown process in CMOS oxides and particularly SiO_2 has been extensively studied. For dielectric breakdown, two scenarios are distinguished, extrinsic and intrinsic breakdown. Extrinsic breakdown is due to defects in the dielectric

which can be introduced during different processing steps while intrinsic breakdown is because of the nature of the dielectric itself. It occurs at a certain electric field, defining the dielectric strength. As the insulating layers are getting thinner the probability of an external defect and therefore the probability of an extrinsic failure are decreasing. Hence intrinsic failure is the most likely problem for today's dielectrics.

II.2.2.a Extrinsic Breakdown

Extrinsic breakdown are breakdown events attributable to defects in the oxide rather than the oxide itself failing. Extrinsic breakdown distributions usually look much different from intrinsic breakdown distributions. The following graph (Figure II-7) shows extrinsic breakdown events grouped into an intrinsic breakdown distribution. Notice that the distribution is bimodal (Figure II-7).

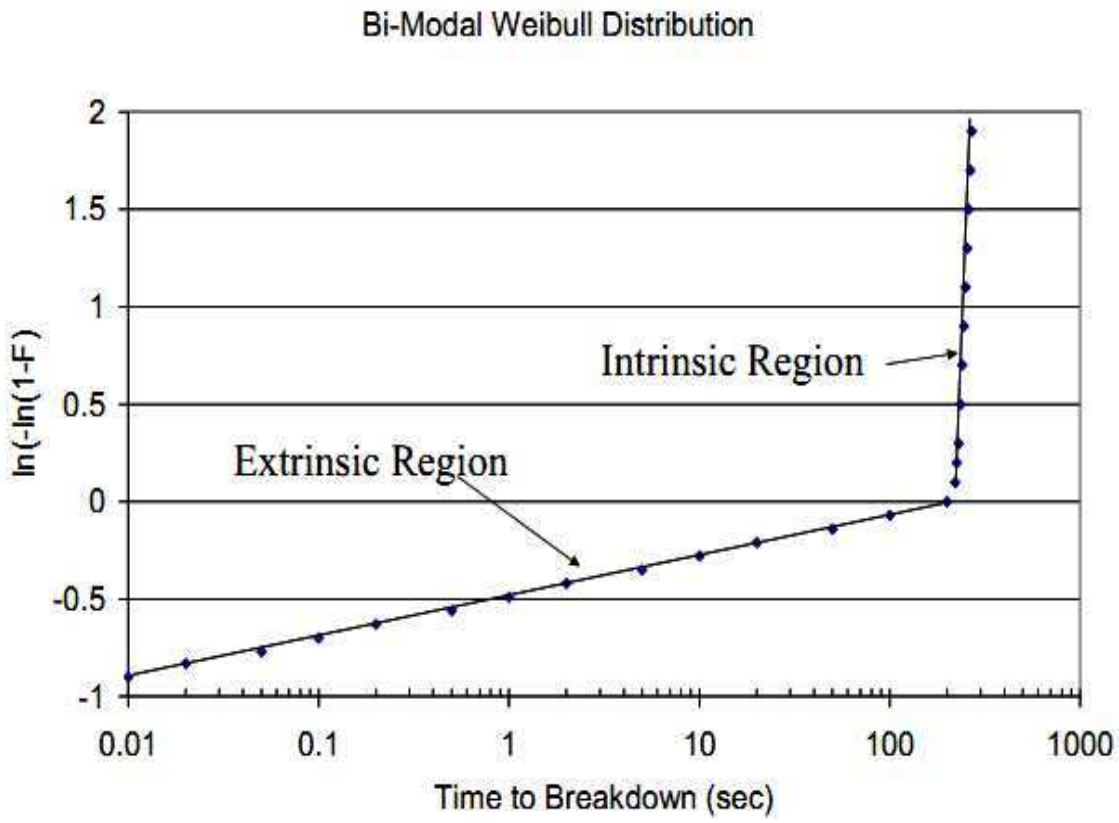


Figure II-7: Graph showing oxide breakdown data that includes both intrinsic and extrinsic failures [II.3].

Many causes for extrinsic breakdown tend to be process related. These causes can include oxide roughness, oxide deposition parameters, particles, etc. Extrinsic failures are usually observed as early failures in a bimodal failure distribution, and are difficult to model [II.4]. Researchers have observed variable field and temperature dependencies in experimental studies. It is more productive to eliminate these types of failures than to model and screen them out of a population. This point of view will be later applied in our study.

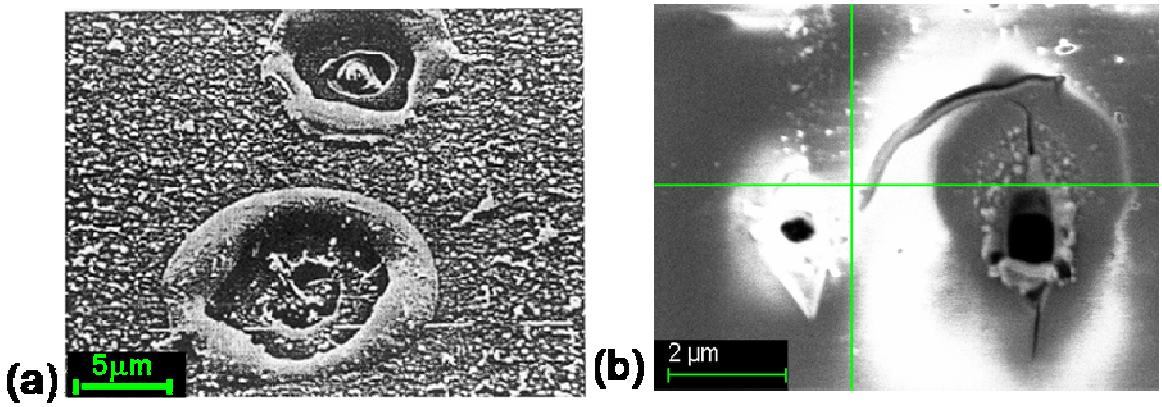
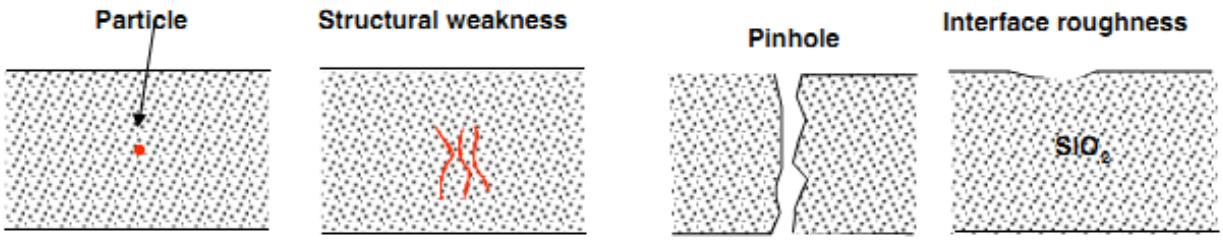


Figure II-8. (a) Oxide surface after destructive Breakdown. Ref D. Wolters, ('Instabilities in silicon devices,'chap.6). (b) Cross section TEM image of an Example of Hard destructive oxide Breakdown observed for an MgO based-MTJ.

As we have explained before, extrinsic breakdown is associated with the presence of extrinsic defects present in the oxide which initiate the irreversible damage of the dielectric. Once initiated, the damage eventually spreads throughout the body of the dielectric causing breakdown. The pre-existing defects can be impurities present within the oxide, structural weaknesses, pre-existing pinholes, interfacial roughness, etc.



II.2.2.b Intrinsic breakdown

In a dielectric, the charge displacement increases with increasing field strength. When the electrical field reaches a critical value, an electric breakdown occurs due to the physical deterioration of the dielectric material. The dielectric strength is defined as the breakdown voltage per unit thickness of the material. When the applied electric field is large, some of the electrons in the valance band cross over the large conduction band across the band gap giving rise to large conduction currents. Under this condition, the strength of the local field is of the order of 1 MV/cm. This value justifies the breakdown risk in CMOS previously mentioned in paragraph II.1. The movement of electrons from valence band is called internal field emission of electrons and this breakdown is called the ***Intrinsic Breakdown.***

One of the most popular statistical models associated with intrinsic dielectric breakdown is the Percolation or Spheres model [II.5] of breakdown. The Percolation theory postulates that defects can be modelled as spheres that affect electrical behaviour within the oxide.

These “spheres” occur randomly within the oxide. As the number of spheres increases, spheres in close proximity to one another can transfer charge. Once a sufficient number of

spheres develop, there will be a location where the spheres bridge from one edge of the oxide to the other. At this point a micro-breakdown can occur (see Figure II-9).

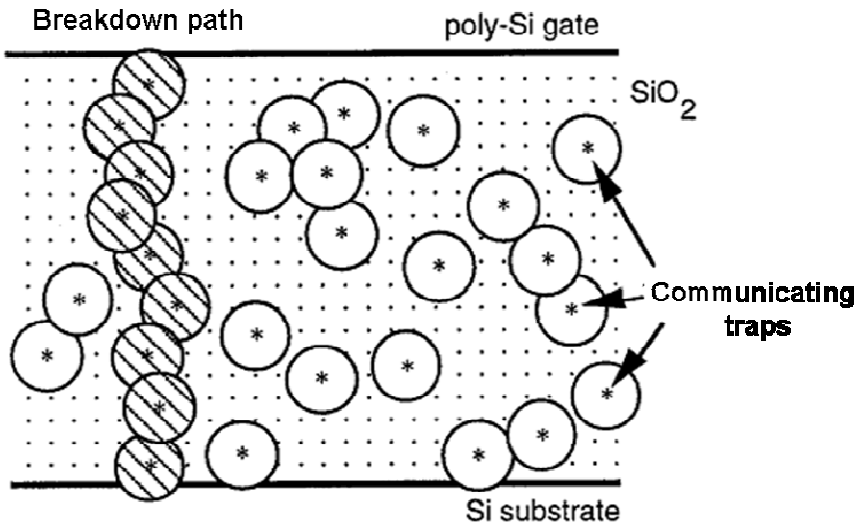


Figure II-9. Schematic illustration of the spheres model for intrinsic oxide breakdown based on trap generation and conduction via traps [II.6].

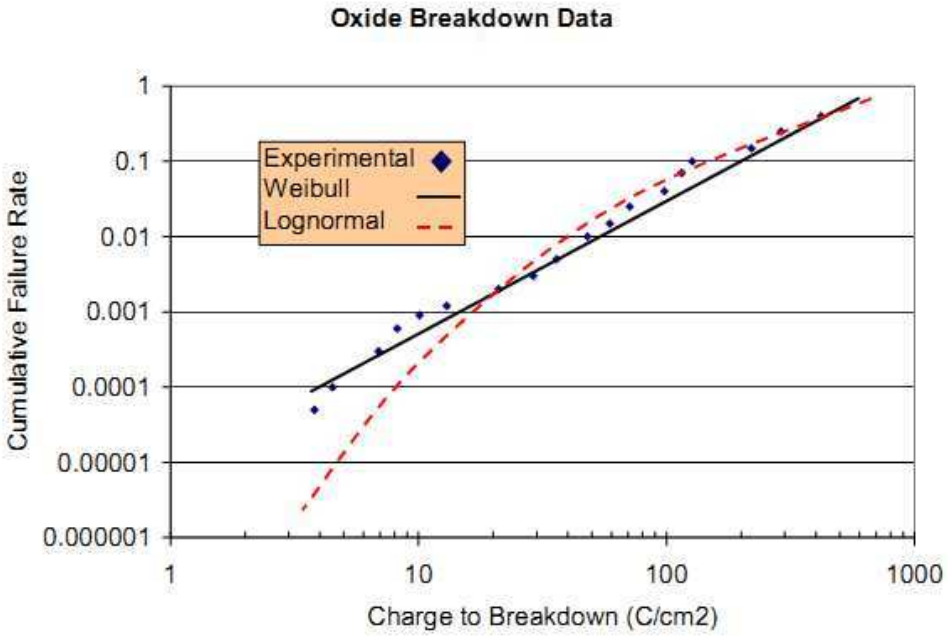


Figure II-10: Example of Weibull Plot.

Two different types of distributions can be used to model the statistics of thin film electrical breakdown, lognormal and Weibull previously introduced in details in section II.2. Lognormal distribution best describes chemical and thermally occurring mechanisms, while a Weibull distribution can be made to fit a wide variety of conditions. For studying reliability in microelectronic devices, the Weibull distribution is generally the most appropriate technique to adopt. The Weibull slope tends to be dependent on the oxide thickness, especially for ultrathin oxides. The Percolation model of breakdown can be used to predict this behaviour as well. For the thinnest oxides there is a large statistical spread, presumably because the conductive path consists of only a few traps long.

II.2.3 Failure Models:

In this section, we present the adopted failure models in CMOS reliability studies so as to try later in chapter 3 to see which of these models could fit better our experimental data. Intrinsic failures are due to breakdown in defect-free oxides. Intrinsic failures determine the true life of a high-quality, defect-free oxide. There are four oxide breakdown models currently used: the band-gap ionization model, the classic anode hole injection (1/E) model, the thermochemical (E) model and the hydrogen release model. Each of these models has its strengths and weaknesses. The scaling of oxides introduces effects and properties that the models cannot adequately predict. Nevertheless, they provide a way to describe a complex phenomenon as a relatively simple mathematical expression that allows reliability calculations and predictions.
To explain how defects are generated in transistor gate-oxides, different theories and models were adopted and developed. The thermochemical model (E model) and the anode hole injection (AHI) model (1/E model) are the two main models, and there has been an ongoing controversy as to which model is correct, as there is data to corroborate both [II.7]. Studies have shown that the 1/E model agrees well with experimental data when high electrical fields are applied. In contrast, at low fields the E model showed better agreement with the experimental data. Other models include the hydrogen release (HR) model, and the role of irradiation and channel hot-carriers.
This section will provide the underlying physical interpretations of these different models; and will develop a mathematical extrapolation of the models to reliability measurements

II.2.3.a Fabrication Defects:

During the fabrication step of a device, there is a risk of creating oxide defects. These defects are heavily dependent on the actual process. Defects can arise due to ion implantation during the oxide formation, plasma damage by subsequent processing, mechanical stress or from process contaminants [II.8].

II.2.3.b Bandgap Ionization Model

In 1990s, DiMaria (IBM Microelectronics) developed the band-gap ionization model. He postulated that oxide defects could be caused by the generation of an electron-hole pairs when the energy of an electron approaches the energy of the bandgap (~ 9eV). This was more likely to occur for dielectrics which are thicker than ~ 20nm at fields higher than ~ 7 MV/cm, and is associated with the high-energy tails of the electron distribution. Although this model was popular in the early to mid 1990s, it is no longer widely used. Data on ultrathin oxides can not be explained by the Bandgap Ionization model, with its validity being restricted to thicker oxides.

II.2.3.c Anode Hole Injection Model (1/E model):

In transistor gate-oxides, the injection of electrons into the oxide could generate holes at the electrode which then get trapped in the oxide [II.7]. The AHI model is based on such a process. At high electric fields, this model shows better agreement to experimental data because at such fields electron tunneling is significant, and hole generation dominates over the thermochemical model.

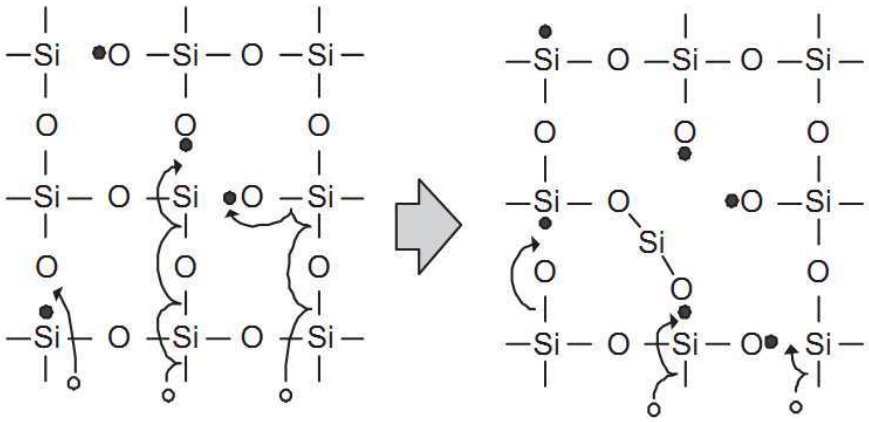


Figure II-11. SiO_2 Bond Breakage due to Hole Current [II.9].

As explained in “Gate Oxide Breakdown” by Navid Azizi and Peter Yiannacouras, the anode hole injection process is as follows:
At high electric field, the electrons arrive at the gate with high kinetic energy (> 8MV/cm) [II.9]. These hot electrons transfer their entire energy to a deep-valence band electron when they reach the gate electrode, and then this electron is promoted to the lowest available electron energy state, which is the conduction band edge of the anode [II.10]. Once the electron reaches the conduction band, it creates a hot hole, which tunnels into the oxide[II.10]. The holes which enter the oxide, allow for increased current density due to *hole-induced trap generation* [II.10]. Once the trap has been created, the current density increases. As a result, more high energy electrons enter the gate which can create more hot holes, etc. This creates an avalanche effect until breakdown occurs [II.7]. An example of how a hole can create a trap in the oxide is shown in Figure II-11, where the holes induce two bond breakages at a single Si atom.

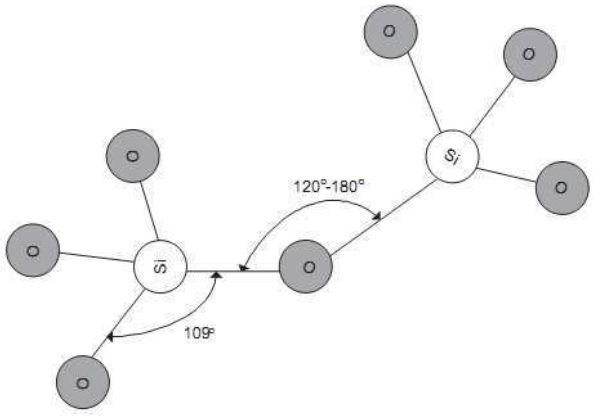


Figure II-12: Chemical Structure of SiO_2 [II.11].

Schuegraf and Hu developed the classic anode hole injection model in the mid 1990s. The Anode Hole Injection Model, commonly called the 1/E model, was the source of some controversy in the late 1990s as researchers cited either it or with the Thermochemical (E) model. Schuegraf and Hu postulated that a fraction of the electrons entering the anode have enough energy to create a “hot” hole which can tunnel back into the oxide. These holes then in turn create defects in the oxide (see Figure II-11). Their equation modeling the process predicts a 1/E dependency, hence the name 1/E (see equation (II-7) below).

$$Q_{bd} = \frac{Q_p}{\alpha_p} \exp\left(\frac{B}{E_{ox}} \left[\phi_p (V_{ox}) \right]^{3/2} \right) \qquad \text{(II-6)}$$

All parameters in the equation can be calculated from quantum physics with the exception of a_p, which is the probability that a hole is generated. Q_p is the critical hole fluence at breakdown known to be 0.1 C/cm²,

Some researchers have suggested based on both theoretical and experimental evidence that significant injection and trapping of anode holes does not occur until the electron obtains a sufficiently high energy (~7.6 eV) in the anode. Recent studies using improved models for impact ionization suggest that anode hole injection can occur at low energies and that the dependence of anode hole induced breakdown on voltage is linear. However, there are no known studies conclusively showing that anode injected holes at low voltage are trapped in the oxide and lead to breakdown.

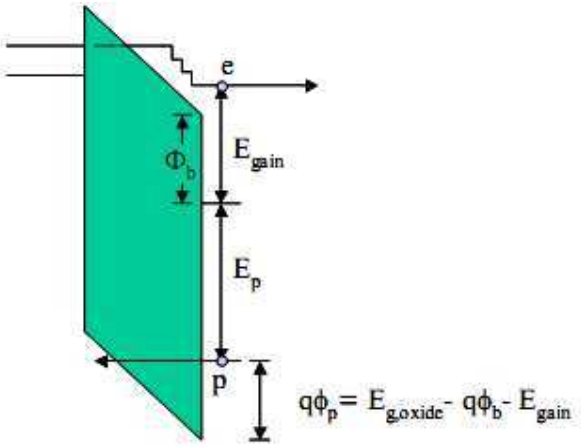


Figure II-13: Diagram showing the principle behind the Classic Anode Hole Injection Model.

II.2.3.d Thermochemical Model (E model):

The 1/E model presented above ignores important thermal processes which degrade all materials over time [II.11], and some recent work which covers ranges of temperature and field conditions shows better agreement with the E model(Thermochemical model) [II.11].

Amorphous SiO_2's primary structural unit is the SiO_4 tetrahedron shown in Figure II-12. The angle between O-Si-O is always 109°, but the angle between the bond linking the tetrahedra ranges from 120° to 180° [II.11].

When the linking bond angle is above 150°, the bond's strength is severely weakened and an oxygen vacancy results where the Si-O-Si bond is replaced with a Si-Si bond as shown in Figure II-14 [II.11]. This oxygen vacancy is thought to be the defect that leads to oxide breakdown [II.11]. The remaining O-Si bonds within the oxide are highly polar bonds; 70% of the total energy is due to ionic contribution [II.11]. Furthermore the Si-Si bond is a very weak bond [II.11].

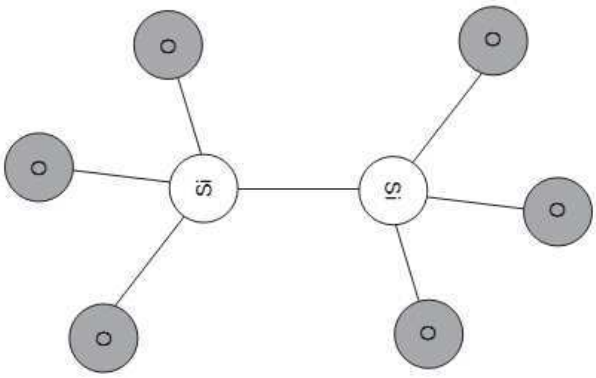


Figure II-14: Oxygen Vacancy in SiO2 [II.11].

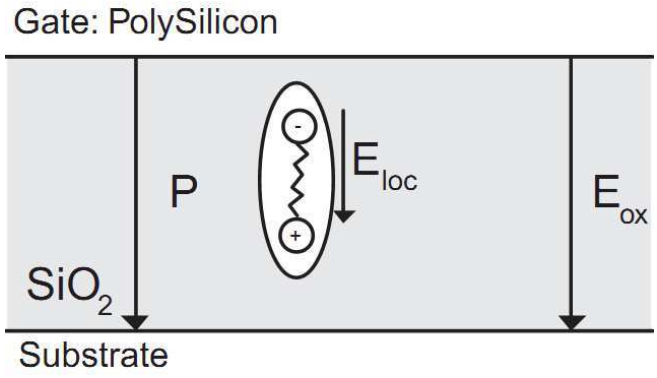


Figure II-15: Local Electric Field in SiO_2 [II.11].

When an electric field is applied to the oxide, there is a distortion of the lattice due to the polar nature of the O-Si bond [II.11]. Furthermore, this distortion induces a polarization ***P*** as shown in Figure II-15. Thus each molecule of SiO_2 not only experiences the externally applied electric field, but it also experiences the dipolar field due to the polarization [II.11], and thus the local electric field, E_{loc}, can be significantly larger than the applied field E_{ox}. Thus the Si-Si bonds are heavily strained due to this large local electric field, and bonds may occasionally gain enough thermal energy to cause the Si-Si bond to break, creating a hole trap as shown in Figure II-16. As noted above in paragraph II.2.2.b the generation of many traps will finally lead to breakdown.

The Thermochemical Model, developed by McPherson and Mogul [II.12],[II.13] in the late 1990s, is an attempt to develop an empirical model based on hydrogen release data, trap generation data, and other observed effects. The model is often referred to as the E model, since the failure rate is proportional to the electric field. Traps are generated uniformly throughout the oxide by applying an electric field. The electric field acting on the bridging oxygen creates an oxygen vacancy (see Figure II-16) or a displaced oxygen atom. The angle of the bond affects this process. Because the strength of the bond is related to the ambient temperature, higher temperatures will cause the bonds to break more readily. Low electric field measurements are possible at 25°C if very long time-to-breakdowns are used. High temperatures can therefore be used to accelerate the low field dependence of breakdown. Finally, McPherson and Mogul suggested that trap generation may be catalyzed by hydrogen, or possibly holes.

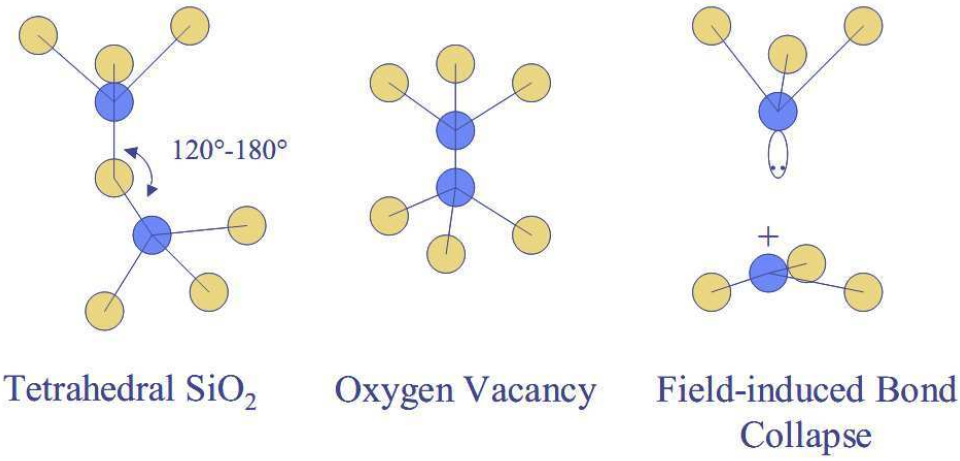


Figure II-16: Diagram explaining the types of defects that can occur with the Thermochemical model.

The Thermochemical model is popular because the model permits a simple acceleration equation. Researchers have used both the Arrenehius equation,

$$T_{BD} = t_o e^{(-E_a/kT)} \tag{II-7}$$

Where E_a the activation energy is proportional to the electric field, and the Erying equation,

$$T_{BD} = t_o e^{(\Delta H - E_a/kT)} \tag{II-8}$$

Where E_a the activation energy is proportional to the electric field or another driving force.
In addition to the basic models described above other factors affect reliability. For example, a strong dependence of breakdown on anode and cathode type has been observed. This dependence is explained by the difference in current density between an n-type cathode and a p-type cathode. This shifts the trap creation threshold relative to the Si anode Fermi level. Plotting Q_{BD} versus V_g normalizes the polarity dependence to first order. Furthermore, hot carrier effects can convolute the time to breakdown data. Hot electrons can increase the trap generation rate, causing accelerated breakdown. These effects need to be taken into account when performing accelerated breakdown studies and estimating reliability lifetimes.

II.2.3.e Hydrogen Release Model:

DiMaria and his colleagues developed The Hydrogen Release Model after physically observing the behavior and properties of the oxides during and after stress. They observed hydrogen release and buildup after stressing various oxide structures. They postulated that energetic electrons create oxide damage by interacting with the oxide lattice itself or with a secondary species such as hydrogen. Based on data taken at IBM [II.14],[II.15] he determined that hydrogen release requires electrons with energy levels of at least 5 eV in the anode, and 2 eV in the oxide (see Figure II-17).

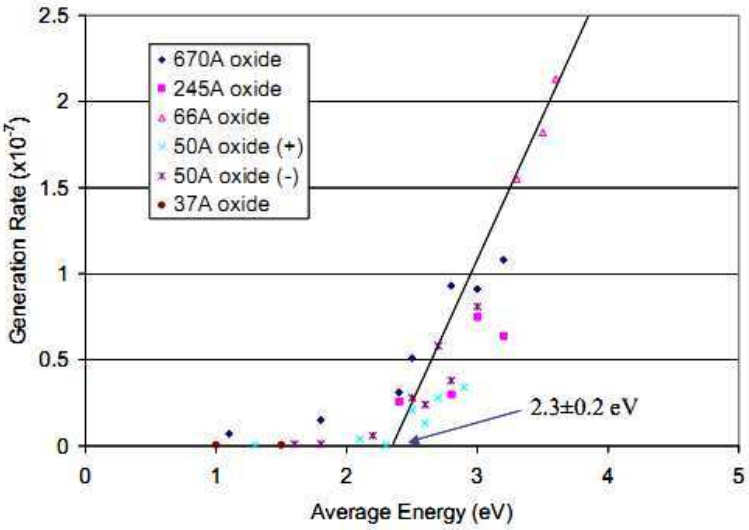


Figure II-17: Data showing trap generation rate versus electron energy. Notice that the generation rate increases when electron energy is greater than ~2.3 volts (after DiMaria).

The process for the HR model is very similar to the AHI model except that instead of holes being produced at the anode; protons (H^+) are generated and reintroduced into the oxide [II.16]. There is evidence that the AHI rate is too small to produce the defects that lead to breakdown, and thus the HR model has been explored [II.16].

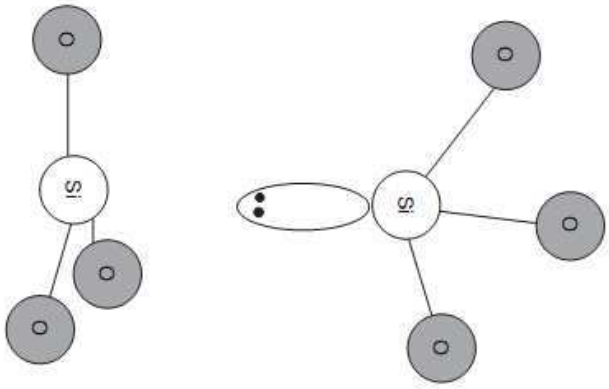


Figure II-18: A Hole Trap in SiO_2 [II.11].

Just as in AHI, high energy electrons tunnel through the oxide, but instead break the Si-H bonds at the interface [II.17]. Thus a H^+ ion is released into the oxide, and there is a dangling silicon bond at the interface. Once the proton enters the oxide, it reacts with oxygen vacancies (Si-Si) to produce a trap: (Si-Si) + H^+ → Si-H^+-Si [II.16].

Discussion:

The various models of breakdown presented in this section were developed specifically for CMOS oxides and particularly SiO_2. When comparing with the situation of magnetic tunnel junctions, several differences arise:
-The oxide used in MTJ is most often MgO which has not been much studied as CMOS gate oxide in contrast to SiO_2 or High K dielectrics (HfO_2, $SrTiO_3$…).

-In MOSFET gate dielectric, one tries to avoid as much as possible tunneling between gate and chanel because this tunneling represents a leakage current which contributes to the static dissipation of CMOS circuits. Therefore, usually the thickness of these gate oxides are larger than in MTJ where we try to favor easy tunneling through the barrier for high current density applications such as in STTRAM.
-However, in applications such as FLASH memories, tunneling of electrons is used to charge or discharge the floating gate. In this case, the tunneling barriers are much thickner than in MTJ (several nanometers) and the bias voltage used to write are also much higher (10-20V). This corresponds to Fowler Nordheim tunneling with injection of electrons in the conduction band of the oxide. This mode of charge injection is known to generate defects in the oxide which turn out to form electron traps. In contrast in MTJ, much thinner oxide barriers are used (~1nm) and bias voltage of the order of 0.5V lower than the barrier height are applied; As a result, direct tunneling from one metallic electrode to the other takes place. A priori, this should be much more favorable in terms of reliability since the hot tunneling electrons loose their energy in the receiving electrodes rather than in the barrier

In chapter 3 we will propose a new mechanism for electrical breakdown in MTJ which contrasts with those described above and may be also present in FLASH memories. It will be based on the mechanical stress induced by the electrostatic interaction between trapped charges in the oxide barrier and the image opposite screening charges which appear in the metallic electrodes.

II.3 CMOS reliability characterization techniques

II.3.1 Time Dependent Dielectric Breakdown

Time Dependent Dielectric Breakdown, or TDDB, is one of the most important failure mechanisms for semiconductor reliability. Since the 1960s, researchers have struggled to understand the nature of how an oxide degrades over time. Over the past 40 years scientists have been able to piece together enough information concerning TDDB to develop basic models that describe the breakdown as a function of variables like time and electric field. For a number of years the debate was whether TDDB followed an E or a 1/E model. Recent data indicates that this discussion may be irrelevant. The Weibull distribution best models the statistics associated with breakdown, since TDDB appears to be a “weakest link” type of failure mechanisms.

II.3.2 Accelerated Stress Testing

Reliability engineers use two major oxide breakdown test configurations. These include: the voltage ramp and the current ramp. The Joint Electron Devices Engineering Council (JEDEC) standardized these two accelerated test methods. Engineers from time to time use other stress tests as well. These include the stepped voltage, the stepped current, the constant voltage, and the constant current stress tests.

II.3.2.a The Voltage Ramp

JEDEC defines a standard voltage ramp stress test for oxide reliability called the V_{Ramp} test (see Figure II-19). This test is one of the most common accelerated tests performed on oxides today. Many reliability test systems can be programmed to do this test.

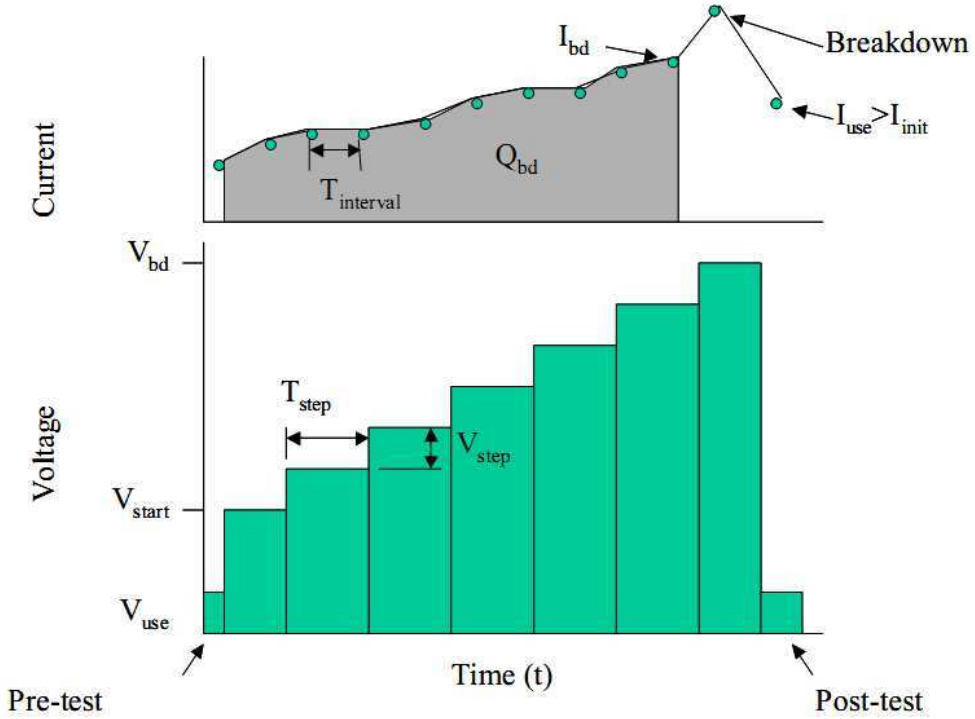


Figure II-19: Diagram showing the operation of the JEDEC V_{Ramp} test.

Basically, there is an initial measurement at a given voltage to verify the integrity of the oxide. Next, the voltage is raised to a predetermined start voltage (depending on the technology) and the current is measured. At equal time intervals, the voltage is stepped up in equal voltage increments and again the current is monitored. This process continues until there is a sharp increase in the current. The previous data point is defined as the breakdown voltage. A final measurement is then made at the use voltage.

II.3.2.b The Current Ramp Test

JEDEC also defines a standard current ramp test called the J_{Ramp} test (see Figure II-20). The test procedure is quite similar to the V_{Ramp} test. First, an initial voltage measurement is done at a predefined current level. Next, the current is raised to the starting stress current. The current is increased in equal increments while making voltage measurements. At a certain current level, the oxide breaks down, causing the voltage to drop sharply. The measurement before is defined as the breakdown voltage. One final measurement is made at the initial current value.

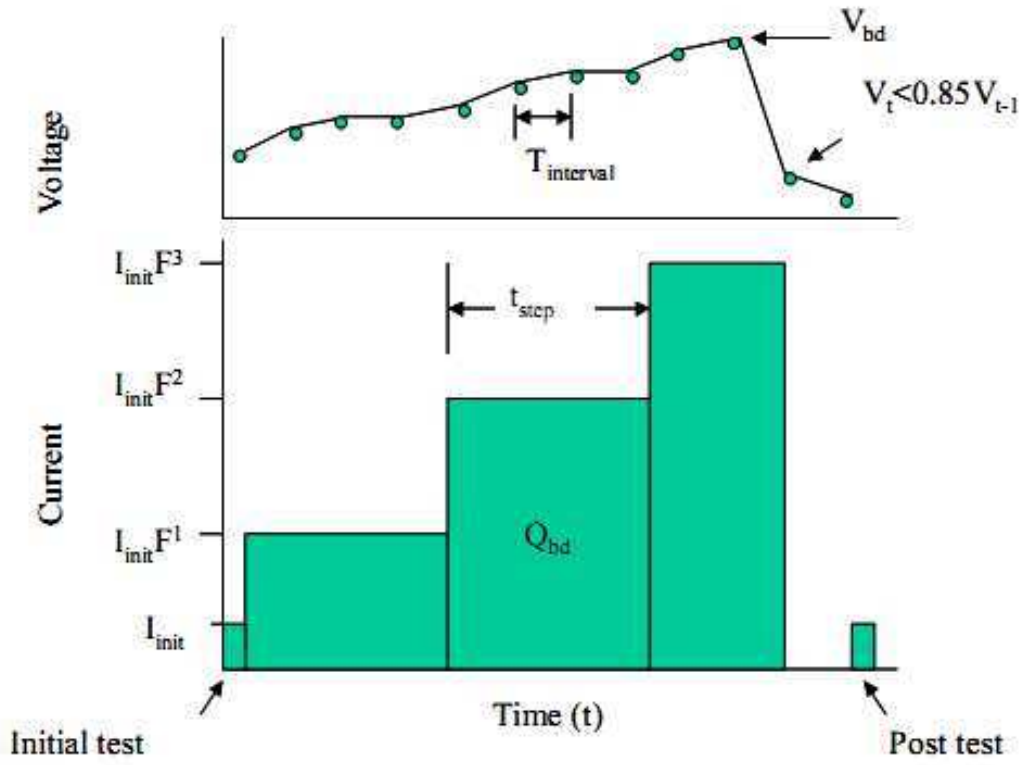


Figure II-20: Diagram showing the operation of the JEDEC J_{Ramp} test.

II.3.2.c Other Stress Test Issues

In addition to hard breakdown, soft breakdowns and quasi breakdown events can occur. Soft or quasi breakdown events occur when the thermal damage is limited by power dissipation. The occurrence of soft breakdown increases as the oxide thickness decreases, the area of the oxide increases, the voltage stress increases, and the stored energy decays with time. Researchers have postulated several mechanisms over the past two decades that explain soft or quasi breakdown: trap-to-trap transport, tunneling via electron traps, dynamic trapping/de-trapping, and insufficient energy transfer of tunneling electrons to anode holes.

II.3.3 AC Effects

In general, the oxide lifetimes are longer under AC stress than DC stress. While this makes sense from a qualitative standpoint, researchers have struggled to understand why this is so. The following graph shows the increase in lifetime as the stress frequency increases.
High frequency TDDB testing is quite difficult to perform, since proper cabling and fixtures are necessary to reduce ringing and voltage overshoots. It has been noticed that lifetime observed under pulsed stress can be attributed to de-trapping of holes. Liang speculated that positive charges at cathode are de-trapped [II.18].

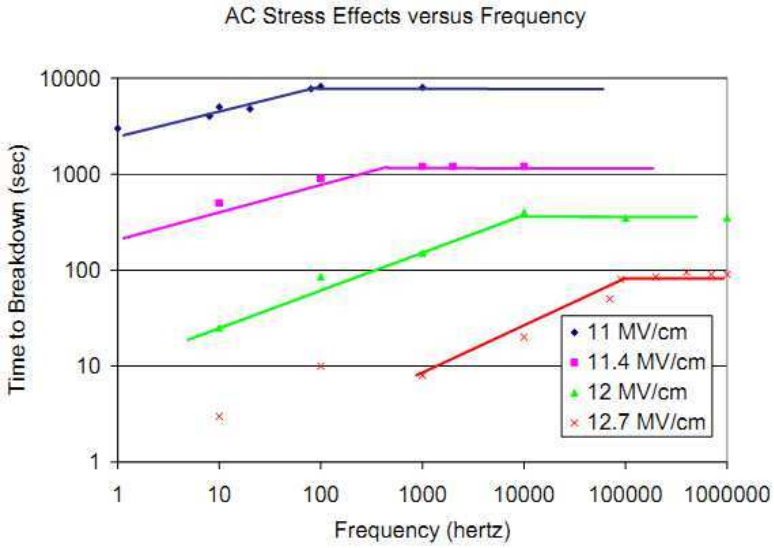


Figure II-21: Graph showing TDDB lifetimes versus frequency.

Fong speculated that reduced transient hole generation occurred under AC stress, while Rosenbaum [II.19] observed detrapping of holes under AC stress [II.19]. Other researchers have observed that lifetime enhancement diminishes as E field and oxide thickness is decreased. Hwang determined that TDDB was worse under bipolar stress in very thin oxides (< 6nm) [II.20]. Researchers believe that this is caused by decreased charge generation and trapping. Further work needs to be done to understand these effects for very thin oxides and especially in MgO to understand MTJs breakdown mechanism. This will be our main objective in chapter 3. We have carried out such AC time dependent dielectric breakdown experiments under pulsed conditions to be closer to the operating conditions of memories applications.

II.3.4 Low-frequency Noise test:

In practically all electronic and optical devices, the excess noise obeys the inverse frequency power law. It exists in addition to intrinsic thermal noise and quantum noise. Many experimental data has been accumulated on 1/f noise in various materials and systems. In very small electronic devices the alternate capture and emission of carriers at an individual defect site generates discrete switching in the device resistance referred to as a low frequency noise. The study of low frequency noise has demonstrated the possible microscopic origin of low-frequency (1/f) noise in these devices, and has provided new insight into the nature of defects at an interface. As will be shown in chapter 4, low frequency noise tests can be used to probe magnetic tunnel junction quality and to highlight the differences in terms of present defects.

II.4 MTJs reliability studies

Oxide barrier breakdown represents one of the main reliability issues for advanced semiconductor memory technology. Despite numerous studies on the tunnel magnetoresistance (TMR) of either aluminum oxide or magnesium oxide MTJs, the breakdown mechanism of ultrathin barrier of MTJs has not been well understood. A more detailed understanding of MTJ reliability issues is still essential for the success of STT-MRAMs or of other devices based on hybrid CMOS/MTJ technology. In both Thermally

Assisted MRAM (TA-MRAM) and Spin-Transfer-Torque RAM (STTRAM), the tunnel barrier is exposed to a voltage stress in the range of 0.4-0.7V at each write event. Considering that the tunnel barrier thickness is of the order of 1nm and that common oxides experience electrical breakdown when exposed to electrical field larger than 10^9V/m, the MTJ barrier electrical reliability has to be thoroughly investigated [II.21]. The write endurance in MTJs has already been studied by several groups [II.22]-[II.26] by time to dielectric breakdown experiments (TTDB). Different breakdown phenomena have been observed depending on oxide layer thickness [II.27], junction resistance area product (RA) [II.25], and junction area [II.22],[II.23]. However, the mechanism and main cause of barrier breakdown in MTJ systems is not yet fully understood, especially when the thickness of the oxide tunnel barrier gets in the range of 1nm-1.4nm.

II.4.1 Aluminum oxide based MTJ:

For thin tunnel barriers with low RA value (7–22Ωμm^2 naturally oxidized Al based MTJ) and large junction area (>1μm^2), the oxide layers experience a gradual breakdown as a function of bias stress time. Correlatively, a progressive decrease of the tunnel magnetoresistance (TMR) is observed before the major breakdown occurs.

For example, J. Das et al had observed a gradual breakdown [II.24] in their stress measurements. Pre-breakdown current jumps occur and, finally, breakdown is observed (Figure II-22). It was shown, by using statistics, that both the current jumps and the final breakdown can be attributed to single trap generation. Moreover, the current jump height can be related to the trap location.

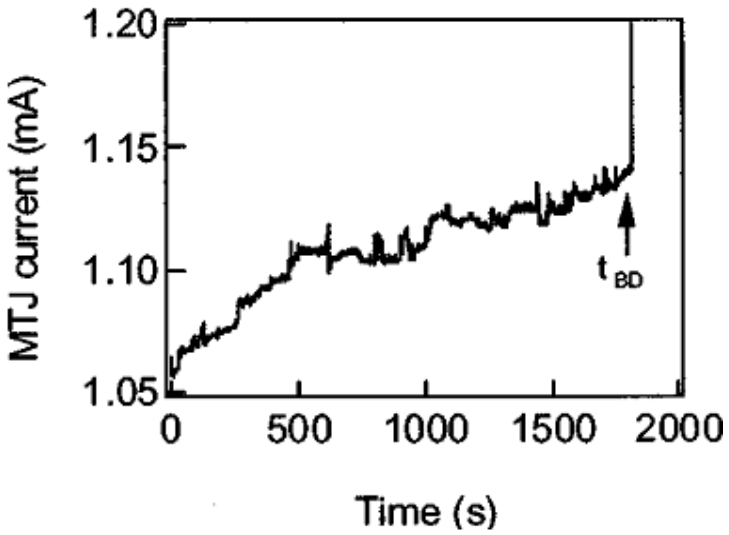


Figure II-22: Typical stress curve (V=1.1 V) of a 12.5 μm² MTJ. Several pre-breakdown current jumps are observed before the MTJ finally breaks down at t=t_{BD} [II.24].

D. Rao et al [II.27] also had observed the effect of a dc stress voltage on the junction resistance and magnetoresistance (MR) of spin-dependent tunneling junctions with naturally oxidized barriers. There was noted that one can define a threshold voltage at which irreversible resistance change begins Figure II-23. Beyond this threshold, device resistance decreases gradually over a transition period prior to breakdown of the tunneling barrier.
The onset voltage of irreversible resistance change is much higher than the optimum operating

voltage of MTJ device (whether STTRAM cell or magnetoresistive heads for hard disk drive, ~0.5V). Correlatively, it was observed that the MR ratio decreases with increasing stress voltage in a pattern similar to that of the junction resistance. [II.27]

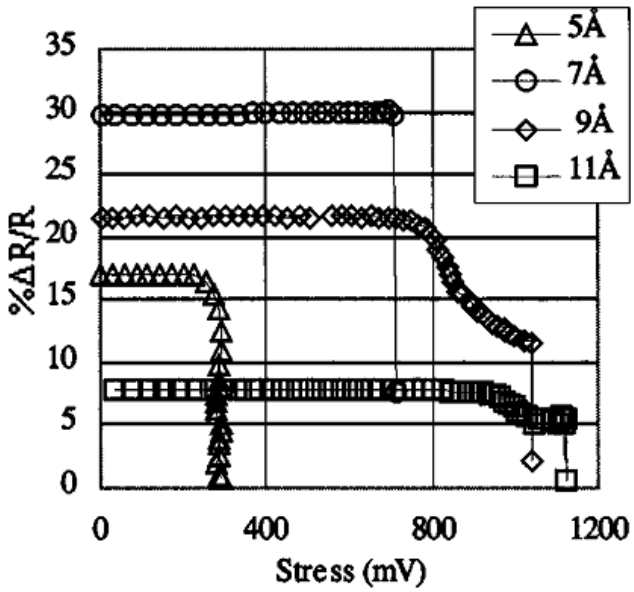


Figure II-23: [II.27] Variation of MR ratio with stress voltage in Alumina based MTJ.

The time-dependent dielectric breakdown of Co/Al_2O_3 /Co (-Fe) magnetic tunnel junctions was investigated in several works, such as the publication of W. Oepts et al [II.28]. It was observed that for applied voltages larger than 1.2 V, almost immediate breakdown of the junction was observed, leading to a decreased (magneto) resistance. Most junctions showed only one hot spot after Breakdown. The shorts, which are local hot spots, were visualized by making use of a liquid crystal film on top of the junction see Figure II-24. These studies were conducted on relatively large junctions (several microns in width).

According to the previous bibliography study of MTJ reliability, the most common failure mechanism for MTJs is the formation of a nanometer-sized conductive short, or ‘‘pinhole,’’ between the two ferromagnetic electrodes. Several groups have investigated the properties of insulating barriers and pinholes using a number of different methods, including analysis of current–voltage characteristics, imaging of pinholes via decoration or liquid crystal-based methods, and scanning tunnelling methods.
In this work for example [II.29], they have presented a powerful method of studying current flow and failure in MTJ elements. Current density mapping and pinhole imaging in magnetic tunnel junctions via scanning conductive atomic force microscopy were carried before and after pinhole formation in several different junctions, it was found that many junctions exhibit an unexpectedly complicated current distribution after high-voltage-induced breakdown. Further, they have seen that pinhole locations can be correlated with current inhomogeneities observed before junction breakdown. Therefore, this breakdown on relatively large junction is essentially extrinsic, related to pre-existing defects such as hot spot due to interfacial roughness.

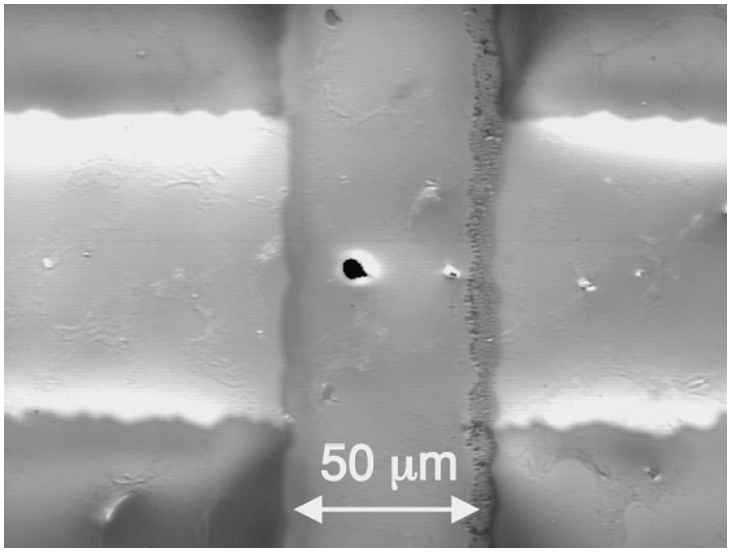


Figure II-24: [II.28] Polarized light picture of liquid crystal on top of a Co/Al2O3 / $Co_{50}Fe_{50}$ junction, the black spot in the middle of the junction surface is the location of a breakdown.

In contrast, according to literature, tunnel barriers with small junction area (≤1µm²) and less extrinsic defects show an abrupt dielectric breakdown without resistance variation or TMR reduction preceding the major dielectric breakdown. A fundamental breakdown mechanism of ultrathin oxide barrier was proposed in terms of percolation model [II.30],[II.31]. According to this model, a complete path of defects see Figure II-25 is formed through the oxide barrier after a certain amount of stress similarly to the conducting filament which forms during the forming phase in Redox RAM (RRAM) [II.32]. However, the nature and role of the defects in the percolation model are not clearly defined and specified in the context of MTJ.

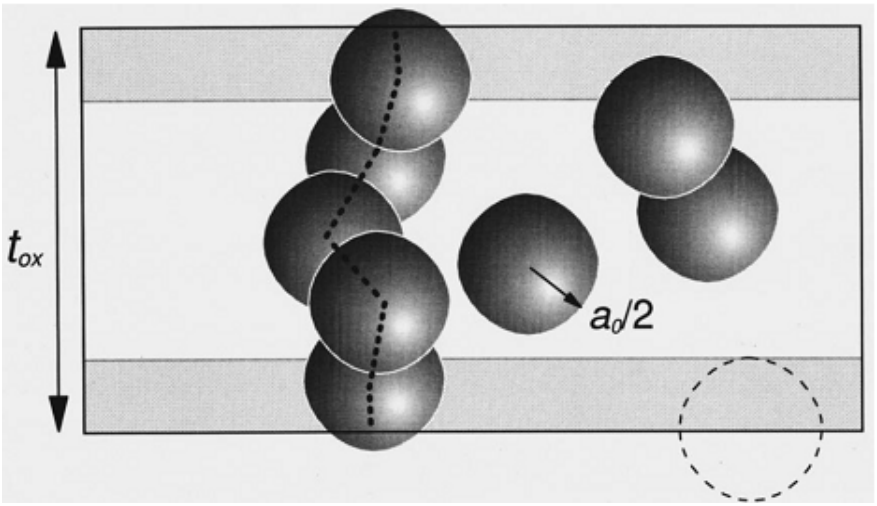


Figure II-25: [II.31] Illustration of the random sphere model (after Degraeve, [II.33]).A cluster of overlapping spheres connecting the top and bottom interfaces defines the breakdown event.

From reliability studies on SiO2 gate dielectrics previously presented, it is known that Weibull statistics have to be used to fit the t_{BD} data. This Weibull function was typically used in all previous studies of MTJ breakdown (see examples Figure II-26 (a) and (b)) and had shown a good fit of MTJ breakdown data.

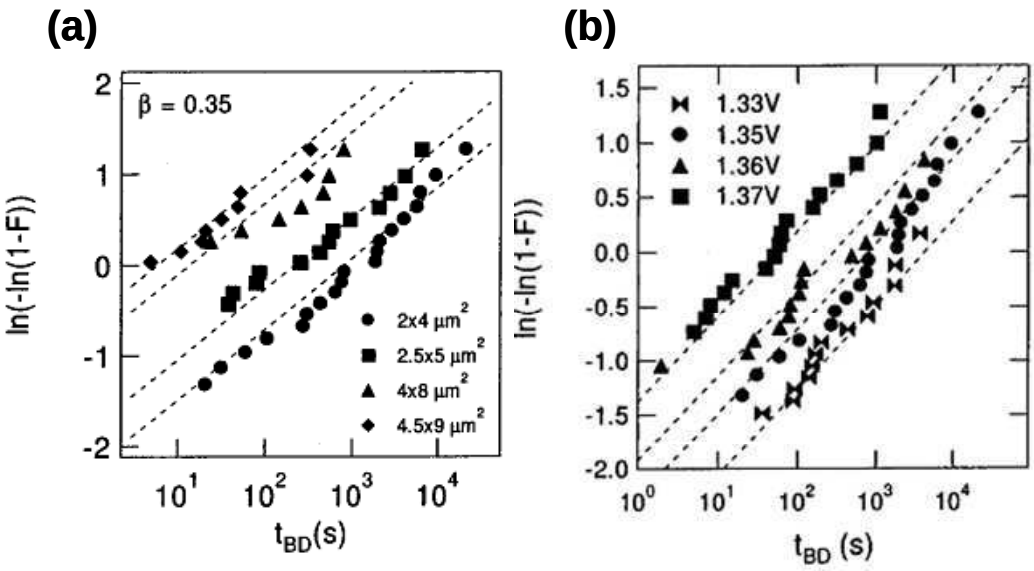


Figure II-26. [II.33] (a) MTJ Weibull plots (V_{MTJ}=1.35 V) for different areas (2*4, 2.5*5, 4*8, and 4.5*9 μm²). (b) MTJ Weibull plots, rescaled to 8 μm², for different stress voltages: 1.33, 1.35, 1.36, and 1.37 V applied to alumina based MTJ.

It was demonstrated that the two breakdown mechanisms observed in an ultrathin alumina barrier MTJ reveal themselves in contrasting ways by studying the parameters of barrier thickness (see Figure II-27), junction area, voltage ramp speed, and substrate temperature. It was found that the observed breakdown mechanism is related directly to the presence of pinholes in ultrathin alumina barrier. MTJs showing an abrupt decrease in resistance at the breaking point are observed to fail due to the intrinsic dielectric breakdown of a well-formed oxide that can be described using the E model. The amplitude of the electric field and temperature were found to accelerate the breakdown of the junctions. Scaling the junction area and the barrier thickness can affect the physical properties of the oxide and its variation of structure and composition. These variations can possibly be attributed to incomplete barrier oxidation, deposition nonuniformity, interfacial roughness, redeposition at the MTJ pillar edges occurring during the etching process…

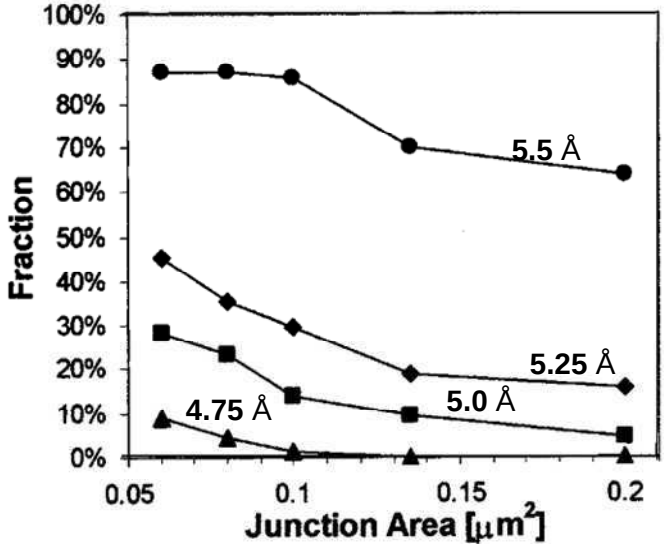


Figure II-27: [II.25] Dependence on barrier thickness (5.5 Å , 5.25 Å , 5.0 Å , and 4.75 Å)and area on the fraction of devices that break down abruptly. Each point represents a fraction in a set of 64 nominally identical AlOx based MTJs.

MTJs showing a gradual decrease in the resistance at the breaking point (see Figure II-28) were determined to fail due to an extrinsic breakdown mechanism caused by pinhole presence. It was possible even to estimate the pinhole area [II.34] and the pinhole growth [II.34] during the breakdown event using two resistor models of MTJs and extrapolating existing data to two extreme situations: When the MTJ has no pinhole and when the MTJ is completely covered by a gigantic pinhole. Extrinsic breakdown weakly depends on the stress factors that effect intrinsic breakdown: Voltage ramp speed and external temperature.

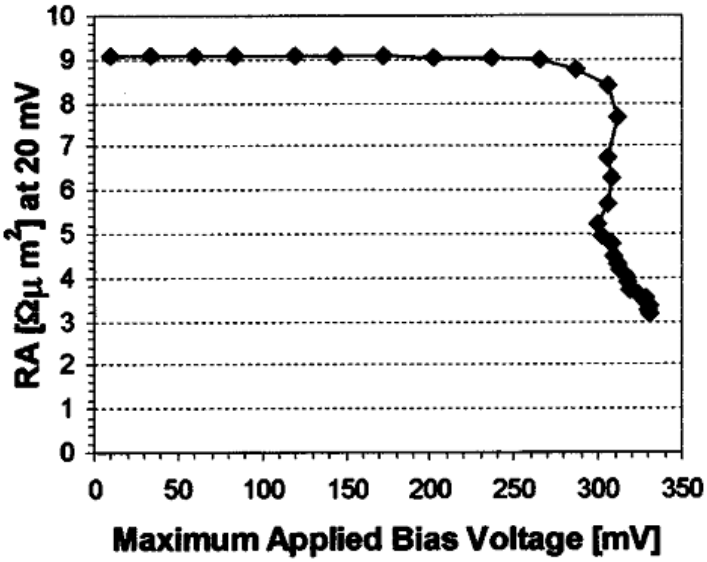


Figure II-28: [II.25] Multiple ramp test of the device that breaks down extrinsically beginning at 270 mV. the RA product is nearly constant until surpassing a threshold voltage of about 270 mV, where further increase of the voltage across the barrier results in the resistance gradually decreasing.

Instead, it was found that the power density at the pinhole and/or the electric field across the barrier are the main stress factors causing the pinhole to grow. To make projections of device lifetime, detailed knowledge about pinhole growth kinetics is needed. At voltages much lower than the extrinsic breakdown voltage, the pinholes are stable, which demonstrates the potential use of ultrathin barriers in tunneling hard drive sensors. From a microscopic point of view, ultrathin barriers will always have pinholes (or at least atomic defects) and we should consider them as a ‘‘composite’’ material in which the structure needs to be very precisely known and controlled.

II.4.2 MgO-based MTJ:

Abrupt breakdown and gradual breakdown were also observed in magnetic tunnel junctions having an ultrathin MgO barrier. The two breakdown mechanisms manifest themselves differently when considering large ensembles of nominally identical devices under different stress conditions. The results suggest that one type of breakdown (abrupt) occurs because of the *intrinsic* breakdown of a well-formed oxide barrier that can be described by the *E* model (see Figure II-29) of *dielectric breakdown*. The other is an *extrinsic* breakdown (gradual degradation then breakdown) related to *defects* in the barrier rather than the failure of the oxide integrity.

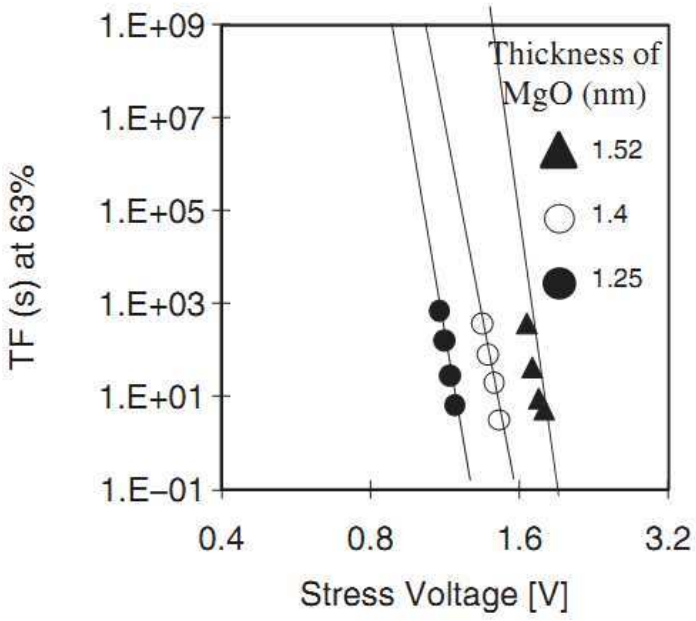


Figure II-29: Time to Failure of 63 % of tested MTJs versus Stress Voltage. Data fitted by E-field model.

In ref [II.35], an abrupt breakdown was observed. Before the breakdown, the resistances in both high and low state were stable during the test, although high state resistance exhibited a slight 4% drop towards the end of the test as shown in Figure II-30. We show in our experimental results in chapter 3 section III.4.1 that very stable resistance values till breakdown were observed in our MTJs.

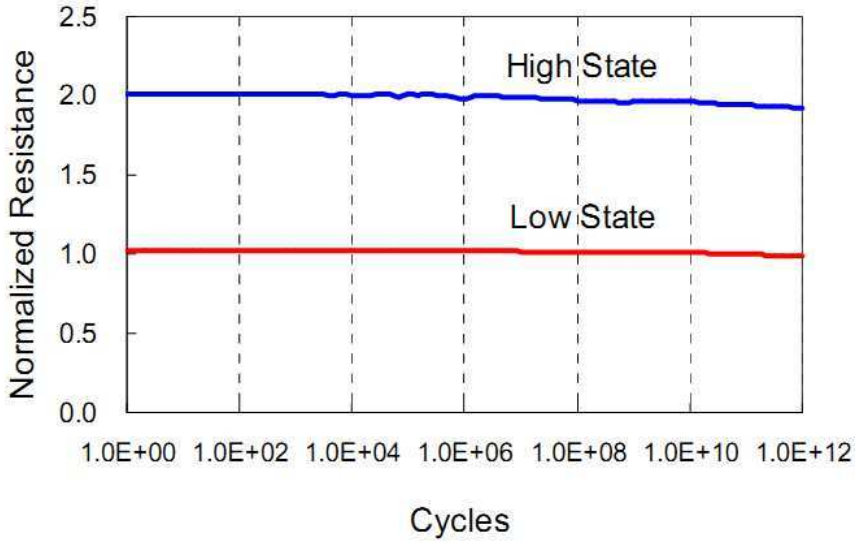


Figure II-30: [II.35] Resistance change during 10^{12} cycle test using 100 ns pulse width. Resistance was normalized by a low state resistance in the first cycle. RA=20 Ωμm².

MgO has been found to be an excellent film with little resistance drift. To make highly reliable tunneling barriers, precise control of CoFeB/MgO/CoFeB interface, related to charge trapping and de-trapping phenomena, was found to be important.
Time-dependent dielectric breakdown (TDDB) measurements under constant voltage stress with positive and negative bias polarities were carried out for magnetic tunnel junctions

(MTJs) with different oxidation status (under-, optimal, and over oxidation). Many groups have found that there is significant polarity dependence in the TDDB and speculated that the polarity dependence is due to both intrinsic and extrinsic origins. Optimally oxidized MTJs with positive bias on the top electrode show shorter times to breakdown (t_{BD}'s) and lower barrier height than with negative bias, indicating that asymmetric band structure, in part, causes the polarity dependence [II.36]. On the other hand, under- and over oxidized MTJs show much shorter t_{BD}'s than optimally oxidized one (see Figure II-31) and show a higher 1/f noise power density [II.36] for positive bias than for negative bias (see Figure II-32), indicating that the polarity dependence is also, in part, due to the interface states, which acts like precursors for the dielectric breakdown. In conclusion, the deteriorated reliability for MTJs with under- or overoxidized tunnel barriers is found to be due to interfacial traps [II.36].

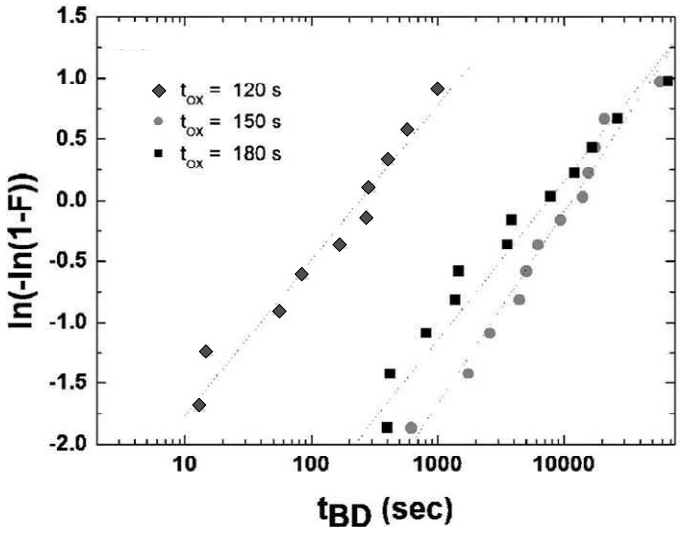


Figure II-31: [II.36] Weibull plots of time to breakdown (t_{BD}) under a bias voltage for the junctions with various oxidation times (t_{ox}).

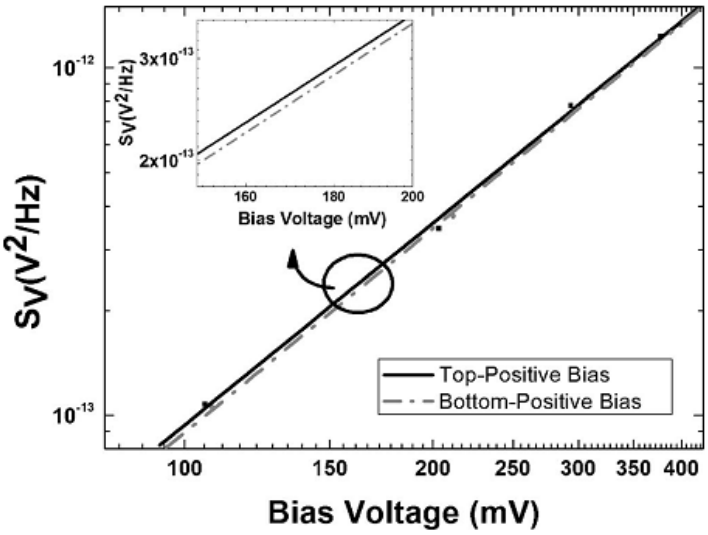


Figure II-32: [II.36] Bias voltage dependence of low frequency 1 / f noise power at 207 Hz for the tunneling barriers in MTJs measured at both positive and negative bias polarity directions.

In conclusion, the deteriorated reliability for MTJs with under- or overoxidized tunnel barriers is found to be due to the interface traps as an extrinsic origin for the polarity dependence of tunnel barrier breakdown.

Finally, we show the results published in [II.37] showing the influence of diffused Boron into MgO barrier (see Figure II-33) on pinhole creation in CoFeB/MgO/CoFeB Magnetic Tunnel Junctions [II.37]. A relationship between boron (B) diffusion into the MgO barrier and pinhole creation in CoFeB/MgO/CoFeB magnetic tunnel junctions (MTJs) was investigated. The diffused B in the MgO layer was identified by secondary ion mass spectrometry for the MTJs annealed at 350 C, which provide the giant magnetoresistance (TMR) ratio. The pinhole density, estimated from the statistic distribution of breakdown voltage of the TMR properties, increased as either the thickness or the B content of the CoFeB layer became thicker or higher.

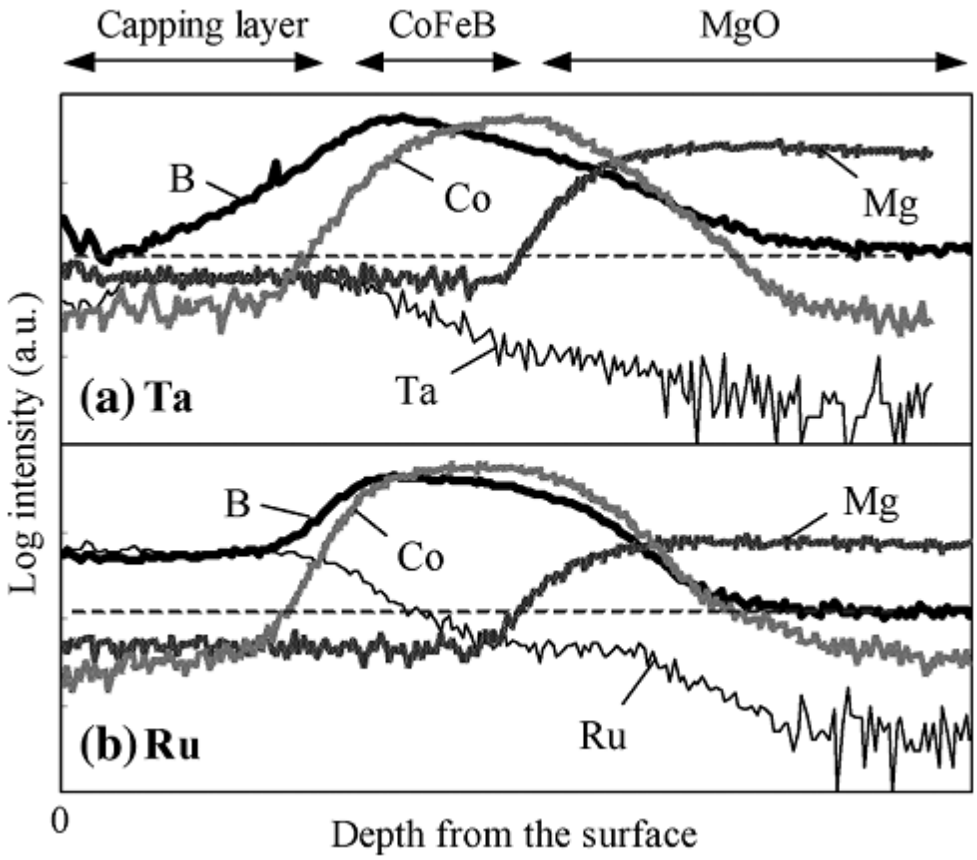


Figure II-33: [II.37] Secondary ion mass spectroscopy (SIMS) profiles measured for the films with SiO_2 (sub) /MgO / $(CoFe)_{20}B_{80}$ / capping layer structure, after annealed at 350 C . The capping layer is (a) Ta and (b) Ru, respectively. The dashed line indicates a baseline of the B intensity.

These experimental findings imply that the diffused B towards the MgO barrier favors the formation of pinholes that short-circuit the tunnel conduction.. This can be due to the formation of a rough BO layer next to the MgO barrier which creates hot spots through the barrier. Three different techniques were found to be useful for the reduction of diffused B towards the MgO barrier layer: the use of materials having boron affinity on the back side of the magnetic electrodes (Ta, Ti, Ru…), decrease of the total amount of B-content in CoFeB layer, and reduction of grain boundaries in the MgO barrier layer.

II.4.3 Conclusion:

One can underline three important points:
First of all, time-dependent dielectric breakdown (TDDB) measurements under constant voltage stress with positive and negative bias polarities were carried out for aluminum oxide and magnesium oxide magnetic tunnel junctions (MTJs) with different oxidation status (under-, optimal, and over oxidation). Different breakdown phenomena have been observed depending on oxide layer thickness, junction resistance area product (RA), junction area, stress polarity, ect. Two breakdown mechanisms were observed: either abrupt or gradual breakdown for aluminum oxide and magnesium oxide based MTJs.
Secondly, the weibull distribution and the E-field model seemed to fit well different data. Finally, the most common failure mechanism for MTJs is the formation of a nanometer-sized conductive short, or ‘‘pinhole,’’ between the two ferromagnetic electrodes.
In chapter 3, we will study the barrier breakdown of MTJs under pulsed conditions, varying the voltage stress. We will try to derive a better understanding of MTJ reliability from these measurements and propose solutions to improve the MTJs reliability.

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Chapter III. Experimental and modelling study of MTJ reliability

Content

III.1 Introduction

Spin transfer torque magnetoresistive random access memory (STT-M RAM) are promising memory technologies because of their non-volatility, high speed operation, low power consumption, very large endurance, high density, and compatibility with standard complementary metal oxide semi-conductor (CMOS) process.
As the magnetic tunnel junction (MTJ) size shrinks, the MTJ resistance must remain comparable to the resistance of the selection transistor in a one transistor-one MTJ (1T-1MTJ) design. Hence, a thinner tunnel barrier that does not compromise on reliability is required. This is even more important for STT-MRAM technologies as compared to magnetic field switching MRAMs since a large current flow through the barrier is necessary for writing.
Oxide barrier breakdown represents one of the main ***reliability issues*** for advanced semiconductor memory technology. Despite numerous studies on the tunnel magnetoresistance (TMR) of MgO-based MTJs, the breakdown mechanism of ultrathin MgO-based MTJ ***has not been thoroughly investigated***. A more detailed understanding of MTJ reliability issues is still essential for the success of STT-MRAMs or of other devices based on hybrid CMOS/MTJ technology.
Lifetime of MTJs is usually measured using a time dependent dielectric breakdown technique carried out by applying a DC voltage while recording the time to breakdown. However, the normal operation conditions of an MTJ in a MRAM device require applying a large number of read/write voltage pulses a few nanoseconds long.
This work reports on the breakdown behaviour of MgO-based MTJs submitted to ***successive voltage pulses***. We studied their ***endurance*** as a function of ***the time interval between pulses*** as well as pulses amplitude and polarity. An earlier study has shown that MgO dielectric breakdown measurements carried under DC voltage and under cumulative pulsed voltage yield equivalent results for pulse-widths longer than 100 ns. In our study, we chose to work with shorter ***constant pulse-width of δ=30 ns*** which is close to the normal operating conditions and is thus of strong interest for MRAM chips reliability. For MRAM application and their 10 years reliability, MTJs have to withstand 10^{16} writing cycles. Testing MTJs in the operating conditions would thus take too long. In our case, we thus have used accelerated conditions (higher pulse voltage than the 0.5-0.8V operating voltage) to obtain reasonable measuring times.

The aim of this third Chapter is to study MgO based MTJ breakdown under pulsed conditions. Firstly, we will start by presenting the studied samples and their preparation methods.
Then we will outline the ***experimental study*** of the effect of delay between pulses for different resistance area values, different pulse voltage amplitudes and different pulse polarities.
Third, we expound our physical ***interpretation*** of experimental results. A charge trapping–detrapping ***model*** was developed to explain our observations. Finally, we show the good ***consistency*** of our developed ***model*** with ***experimental results***.

III.2 Studied samples: composition and preparation

III.2.1 Introduction:

To realize high TMR in MTJs, it is important to obtain a good crystallinity of both the magnetic electrodes and MgO tunnel barrier, with (001) crystallographic orientation.
The excellent crystallinity of (001)MgO layer and (200) CoFeB layer is the primary factor for the higher TMR in CoFeB/MgO/CoFeB structure, confirmed by X-ray diffraction [III.1],[III.2].

In the literature, the (001) oriented MgO layer has been obtained with different methods, such as molecular beam epitaxy [III.3], magnetic sputtering deposition [III.4], [III.1] and ion beam deposition [III.5], *etc*. The deposition parameters - such as, in the case of magnetic sputtering deposition, Ar pressure [III.6], sputtering power, deposition rate and the distance between target and substrate - usually affect the crystal structure of MgO layer. Therefore, the careful research work of the influence of deposition parameters on the crystal structure of MgO layer and the TMR ratio of MgO based MTJs is important for successfully fabricating (001)-oriented MgO and obtaining higher TMR ratio in MgO based MTJs [III.7].

In this study, we investigated MTJs based on MgO tunnel barriers that were prepared by sputtering deposition of a thin Mg layer, followed by a subsequent oxidation, performed either by plasma or natural oxidation. The deposition was performed with a growth rate of less than 0.5 Å/s. For the plasma oxidation case, oxygen plasma of 100W power was used while for the natural oxidation we have used an oxygen flow of 500sccm and a pressure of 1Torr. The oxidation time was adjusted in both cases in order to maximize the TMR ratio. This optimization ensures that the Mg metallic layer is fully oxidized - not underoxidized, which would reduce both the RA and the TMR, - neither overoxidized, which would increase the RA and reduce again the TMR ratio. In order to avoid pinhole formation within the barrier the deposition was performed in 2-3 alternating steps of deposition of Mg/oxidation.

III.2.2 Layer deposition by Magnetron Sputtering:

Sputtering process is a physical vapour deposition process widely used in magnetic recording industry, mainly to deposit films onto a substrate for a wide variety of commercial and scientific purposes.

In 1852, Grove founded the sputtering deposition method. This method has been developed and applied to industry for 200 years. The main principle is to use a vacuum chamber and fill with it with Argon. By applying a high voltage to the material target to be sputtered, the argon gets ionized, forming a plasma. This plasma is confined nearby the targets thanks to magnets placed behind the target (magnetron configuration). The argon ions (Ar^+) are then accelerated towards the target cathode with high speed. When impinging on the target, the Ar+ ions eject atoms from the target material. These sputtered species are directed towards a facing substrate (anode) where they condense as a film. The sputtering process is schematically presented in (Figure III-1)

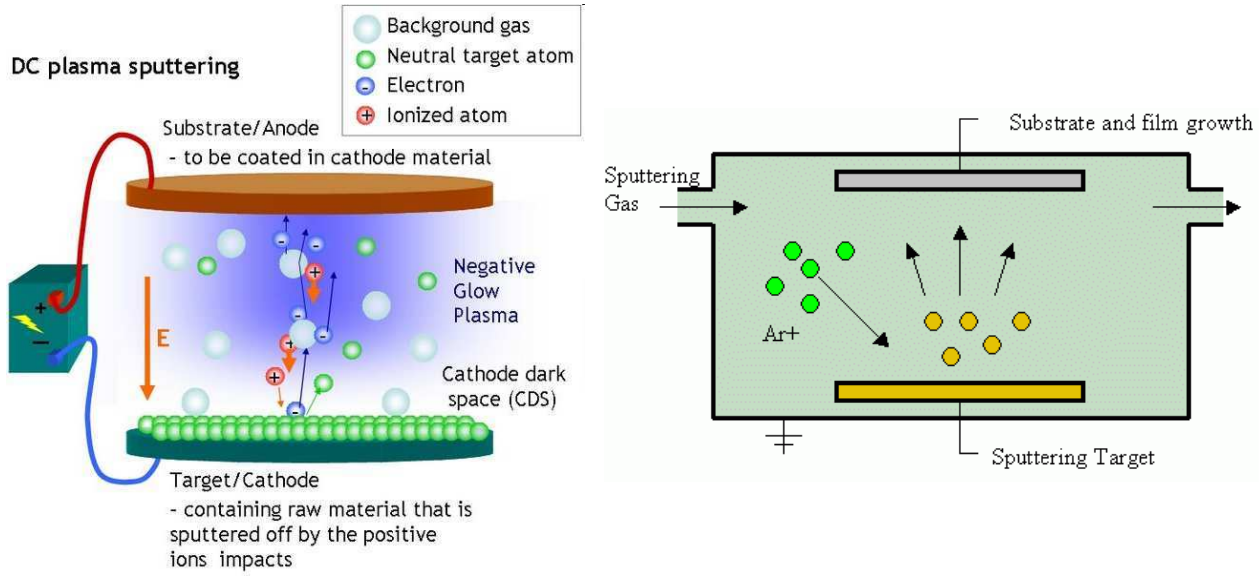

Figure III-1 - Schematic representation of sputtering process.

In brief, we can summarize the advantages of sputter deposition, which make it interesting for industrial purposes, as follows:
* Multi component films, insulators as well as refractory materials can be deposited.
* Good adhesion on the substrate with proper buffer layers.
* Thickness uniformity over large areas can be obtained.
* Thickness control is easy since the thickness is proportional to the deposition time.
* *In situ* substrate cleaning is possible by argon ion bombardment.

Figure III-2 – Photography of Plassys Sputtering machine.

Usually the equipment is composed of several chambers, each being dedicated to a particular class of materials (for instance a chamber for metallic deposits, another one for oxides (see Figure III-1).

III.2.3 Studied samples:

This study was carried out on MTJs comprising an MgO barrier and CoFeB electrodes. The MgO barrier was formed by a plasma oxidation of metallic Mg layer. The used stack is thus buffer/PtMn 20/CoFe 2/Ru 0.8/CoFeB 2/CoFe 0.5/Mg 1.0 oxidation/Mg 0.4 oxidation/CoFe 0.5/CoFeB 2/Ta 0.2/NiFe 3/cap (thicknesses in nm). The top CoFe 0.5/CoFeB 2/Ta 0.2/NiFe 3 is the free (storage) electrode and the bottom PtMn 20/CoFe 2/Ru 0.8/CoFeB 2/CoFe 0.5 is the pinned (reference) electrode. This latter is composed of a synthetic antiferromagnet (SAF), *ie.* antiferromagnetically coupled CoFeB and CoFe layers separated by Ru, that are magnetically pinned by exchange bias to the PtMn antiferromagnet. The use of SAFs and thus the local compensation of magnetic moment, is important to reduce stray fields in the future pillars and improve the pinning of the reference layer. After depositing the MTJ stack, the samples were annealed in a magnetic field of 1 T at 300 ◦C for 1 h to recrystallize the barrier and CoFeB electrodes as well as to set the exchange bias in the bottom pinned electrode.

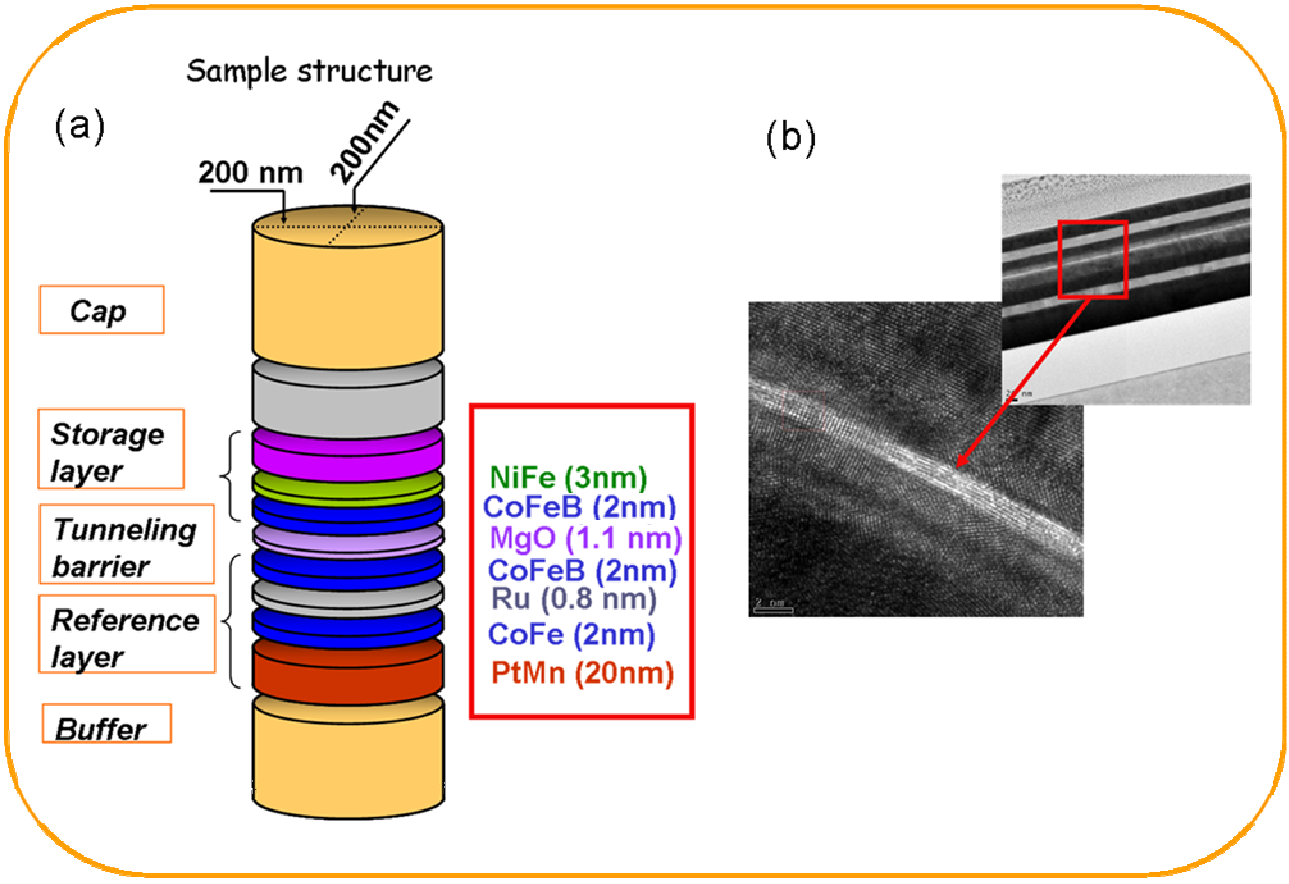

Figure III-3 - (a) Schematic representation of the layers in the studied MTJs.
(b) Cross section TEM image of such a MTJ. The lower part is a zoom of the upper part in the red rectangle. The white region in the lower image corresponds to the MgO barrier.

The junctions were defined by advanced photolithography and patterned in circular pillars of 0.2μm diameter. More details of processing steps will be presented in the next section.
Quasi-static electrical measurements show a maximum TMR signal of 140% and a resistance x area product (RA) of 25 $\Omega.\mu m^2$.
In fact, many samples with different resistance area (RA) product (different barrier oxidation and thickness) were tested.

An example of TEM cross section of a MTJ with MgO barrier is shown in Figure III-3-b). This example of studied junctions had the following composition: buffer/PtMn 20/CoFe 2/Ru 0.8/CoFeB 2/Mg 1.1 plasma ox/CoFeB 2/NiFe 3/cap (thicknesses in nm). The MgO barrier was also prepared by plasma oxidation of an Mg layer. The measured devices were patterned into 250 nm circular pillars showing 100%– 130% TMR ratio and a resistance area (RA) product of 30 $\Omega.\mu m^2$ except otherwise mentioned. The white layer in the lower image of Figure III-3-b corresponds to the MgO barrier 1.1nm. Its continuity and crystallinity is visible.

III.2.4 Patterning of MTJs:

After deposition and preparation of the different layers on a full sheet wafer, the MTJs have to be patterned in the form of submicronic pillars contacted at top and bottom by conductive electrodes..
The patterning process was done in the PTA clean room (Plateforme de Technologie Amont). For the nanoprocessing, the studied MTJs are deposited on a thick TaN buffer layer (40nm thickness), which is used as the bottom electrode to flow the current for the electrical measurements. On the top of the MTJ a thick Al/Ta mask is deposited before the process, which is used as a protection hard mask during the pillar definition (see Figure III-4 left).

In the first level, we define the pillar sizes by E-beam insolation of PMMA resist, and after that we deposit Pt. After the lift-off (removal of the resist), the Pt pillars serve as a protection for the subsequent Ta selective etching by Reactive Ion Etching (RIE). The MTJ active layers are then non-selectively etched by Ion Beam Etching (IBE), the Ta pillars previously defined used as protecting mask. A Scanning Electron Microscopy SEM image at this step is presented in Figure III-5.

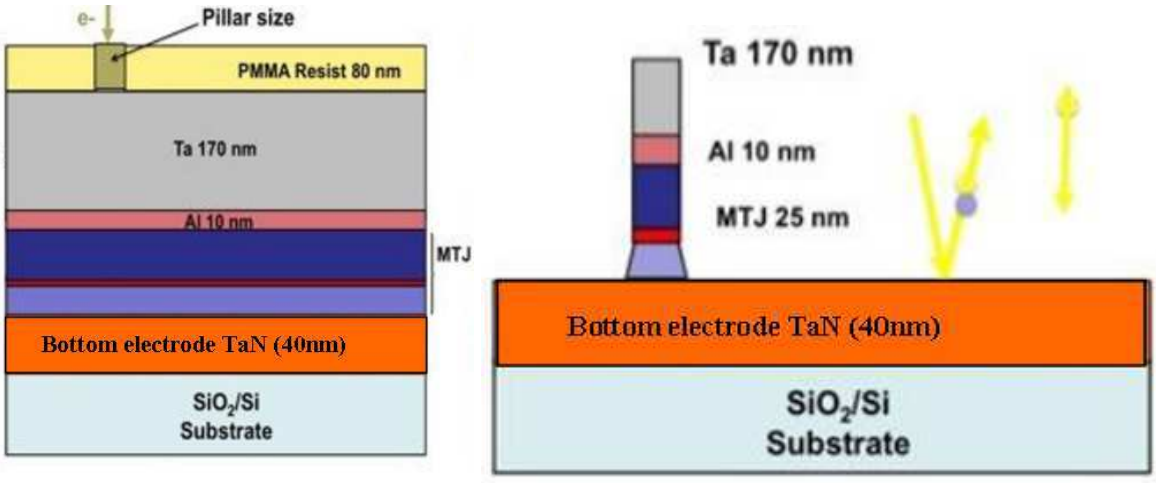

Figure III-4 - (left) E-beam insolation for pillar sizes definition and (right).Ion Beam Etching (IBE) for MTJ pillar definition.

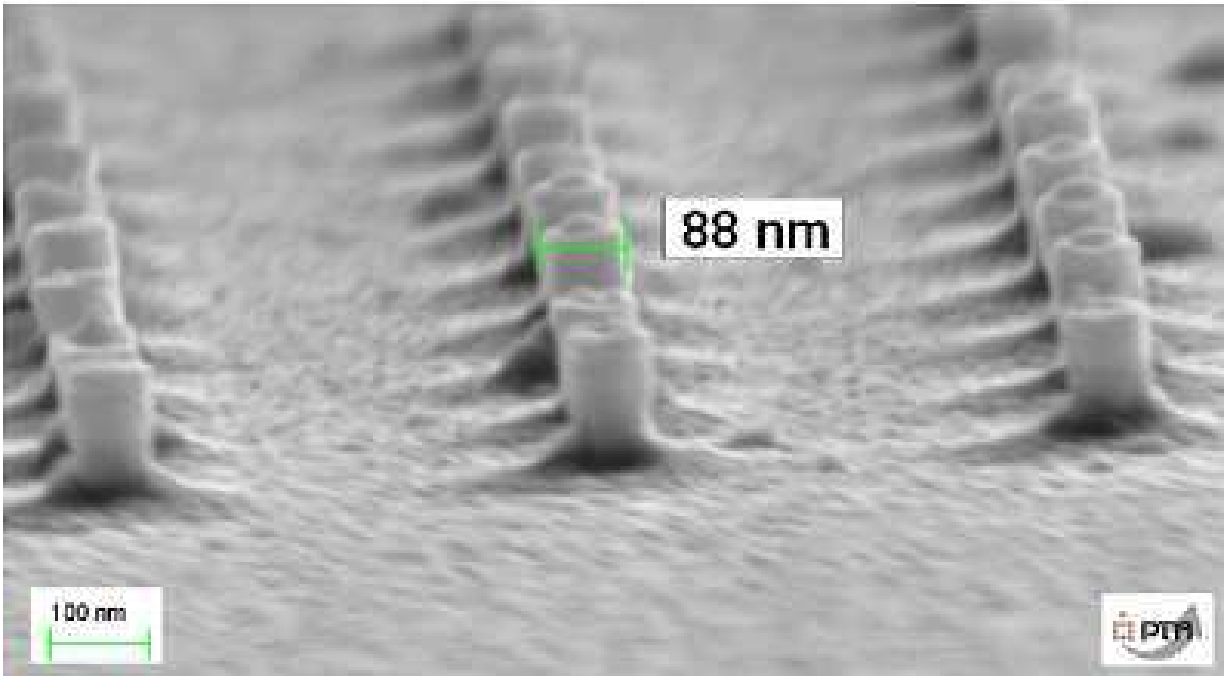

Figure III-5 - Scanning Electron Microscopy (SEM) image of a range of pillars after IBE etching.

Next, the patterning of the bottom electrode is done by UV lithography.
The resist AZ1512 is exposed to UV light and the electrodes are defined using an optical mask. In the next step, the exposed resist is removed using a chemical developer. After an IBE etching of TaN, the top resist, unexposed to UV and damaged by the IBE (strong heating during the process) is removed by RIE, using oxygen plasma. The obtained structure is illustrated in Figure III-6.

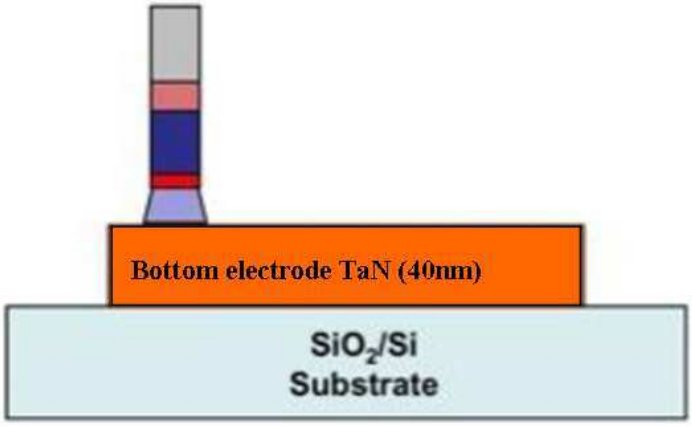

Figure III-6 - Fabrication of the bottom electrode by UV lithography.

The third level consists of the planarization and opening of the dots. We deposit an insulating planarizing resist (called accuflo). After the appropriate annealing process, accuflo provides a very flat surface, independent of the underlying topography and in particular of the pillars. AZ1512 resist is then deposited and exposed to UV lithography.
Using O_2 plasma, the accuflo not protected by the resist is then etched so that it remains around the pillars to subsequently insulate the top and bottom electrodes (see Figure III-7).

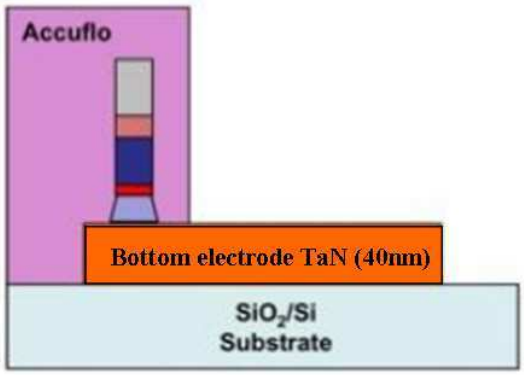

Figure III-7 - Planarization and opening of the dots.

After the lift-off of the resist, a thinning of the accuflo is performed by O_2 plasma RIE allowing the pillars to emerge from the accuflo. The last step is the fabrication of the top electrode. We deposit AZ1512 resist and we expose it to UV radiation using level mask.
After the lift-off we deposit a 30nm Al layer by evaporation to get a good electrical contact during measurement (see Figure III-8). This Al also allows taking the contacts of the bottom electrode.

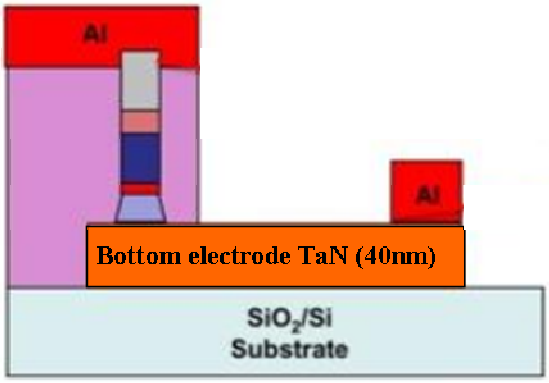

Figure III-8 - Fabrication of the top Al electrode.

III.3 Experimental procedure

In this section, we will present the endurance measurements performed on the MTJs. It consists in applying a sequence of pulses until barrier breakdown occurs, the latter being detected by RA and TMR measurements. The statistical treatment of the data allows the extraction of generic behaviour and avoids the influence of cell-to-cell variations due to possible inhomogeneities in film composition, thickness, quality or in patterning.

III.3.1 Experimental setup:

The experimental setup consisted of an Agilent 81103A pulse generator and a Phasemetrics MRW magnetoresistance probe system. A 2 GHz bandwidth switch matrix was used to connect both systems to the MTJ using a 50Ω adapted probe card as shown schematically in (Figure III-9). This setup was used to alternatively measure the magnetoresistance loop and to apply the stress voltage pulses. In order to ensure consistency in the reported endurance

results, only junctions with similar electric and magnetic properties were selected. To do so, a first MR loop measurement was performed to check TMR and resistance levels.
The endurance test procedure consisted in applying a sequence of pulses of constant width and voltage amplitude until barrier breakdown occurs. After each pulse sequence, a MR loop was performed to check the junction TMR and resistance levels.

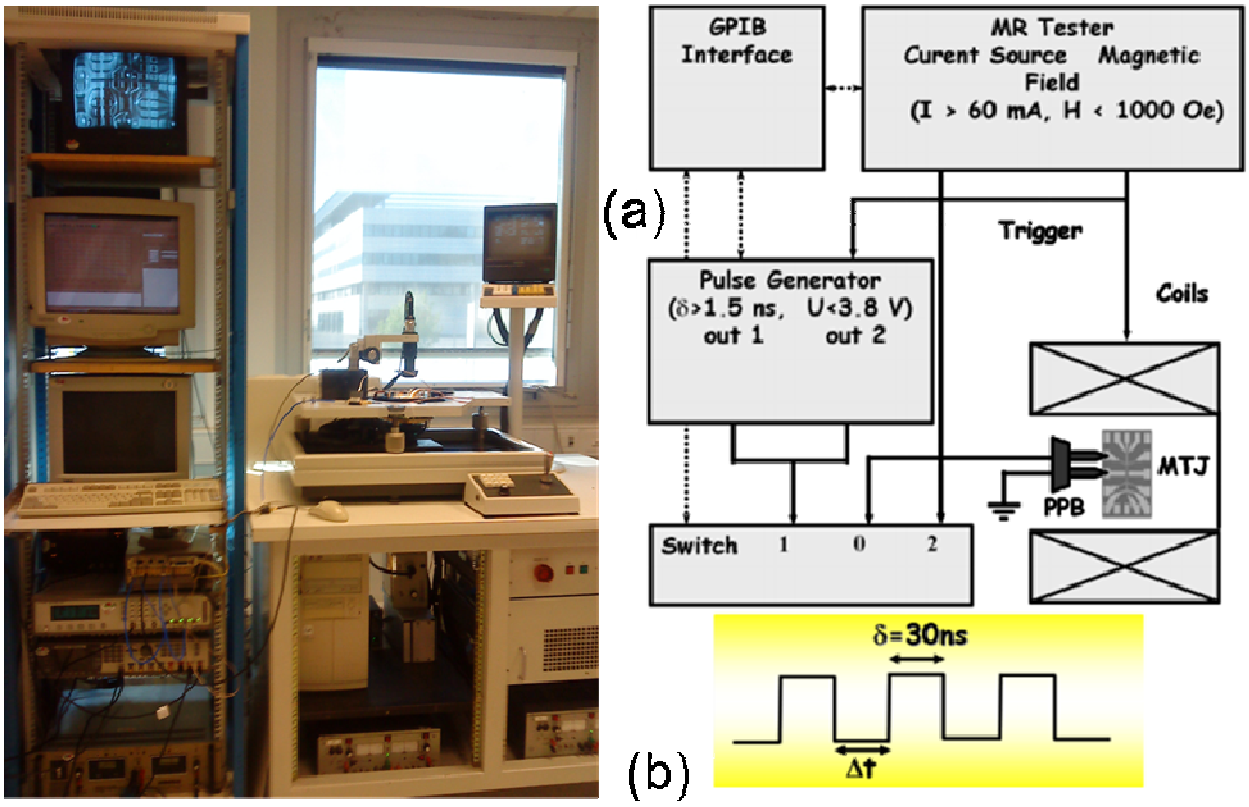

Figure III-9 – Left: picture of the used bench. (a) Schematic experimental setup used to study MTJ breakdown. (b) Train of pulses applied with the pulse duration δ=30ns and delay between pulses Δt.

For each wafer, we did a first speed test which gives us an idea of the adequate pulse amplitude we have to apply.
As we are limited in time, we decided to apply a maximum of 10^{12} pulses (cycles) representing about 28hours of continuous measurements(1 cycle=δ+Δt=30ns+70ns=100ns).
If the junction is not broken after 10^{12} applied pulses, we choose another junction neighbour to the last tested one and we increase the pulse amplitude. We repeat this primary test till we find the range of pulse amplitude that satisfies the condition of time to failure inferior or equal to 10^{12} pulses.

III.3.2 Adopted experimental procedure:

After performing a first MR loop to select the MTJs of interest (ie. same resistance around 2kΩ and similar MR loops), the experimental procedure consisted in applying successive pulses of 30 ns with constant amplitude (ranging from 1.00 to 1.80V) at zero magnetic field until barrier breakdown occurs, ie. until a drop in both MTJ resistance and TMR (see Figure III-11(b). Figure III-9 (b) represents a schematic train of pulses applied with the pulse

duration δ=30ns and delay between pulses Δt as a constant parameter for the whole sequence of pulses. The pulse amplitude was corrected taking into account the voltage drop in the electrical leads. The latter was determined for every junction from the resistance value after breakdown, around 250 Ω (see Figure III-11), 10 times lower than the initial resistance. This value is mainly due to electrical leads.
For each set of pulse parameters, this time dependent dielectric breakdown test is performed for a group of (30–40) MTJs.
In order to reach reasonable measuring times, the experiments were performed in accelerated breakdown conditions, i.e., with a corrected pulse amplitude ranging between 1.0 V and 1.8 V, corresponding to an electric field of ~ 9–18 MV/cm. This pulse amplitude is two to three times higher than that required for STT-RAM writing under normal operation conditions.

Two different measurements were adopted in our study:

1) For a constant pulse duration δ=30ns and a constant delay between pulses Δt =70ns, we determine N_{pulse}, the number of pulses after which 63% of (30–40) MTJs are broken (see statistical treatment in paragraph III.4.2). This test was repeated for ***different pulse amplitudes*** (1.00 V–1.80V).
2) For a constant pulse duration δ=30ns and a constant pulse amplitude, we determine N_{pulse} the number of pulses after which 63% of (30–40) MTJs are broken. This test was repeated for ***different delay between pulses Δt*** (1 ns – 10 µs).
3) For constant pulse amplitude, we study the effect of pulse duration δ variation.

III.4 Experimental results

III.4.1 Types of Breakdown

III.4.1.a For high RA= 25-30 $\Omega.\mu m^2$.

As explained before, for a given pulse duration of 30 ns and constant delay between pulses Δt =70ns, we studied the resistance and TMR evolution after pulse application.
After each pulse sequence, a MR loop was plotted to check the junction TMR and resistance levels. In Figure III-10, we represent an example of MR loops of a studied MTJ plotted respectively before applying pulses, after 10^6 applied pulses, after 10^{10} applied pulses and after breakdown (6.10^{10} applied pulses).

Let's first discuss the evolution of the junction resistance under this train of successive voltage pulses. For that, we represent the R_{max} corresponding to antiparallel configuration and R_{min} corresponding to parallel configuration as a function of the number of already applied pulses (see Figure III-11(b)).
For all of studied samples which represent a high RA of 25-30 $\Omega.\mu m^2$, no gradual degradation of the barrier resistance was observed. The breakdown occurs abruptly as shown in Figure III-11 (b) and corresponds to a sharp drop of the junction resistance accompanied by a degradation of the TMR response (see Figure III-11 (a)).

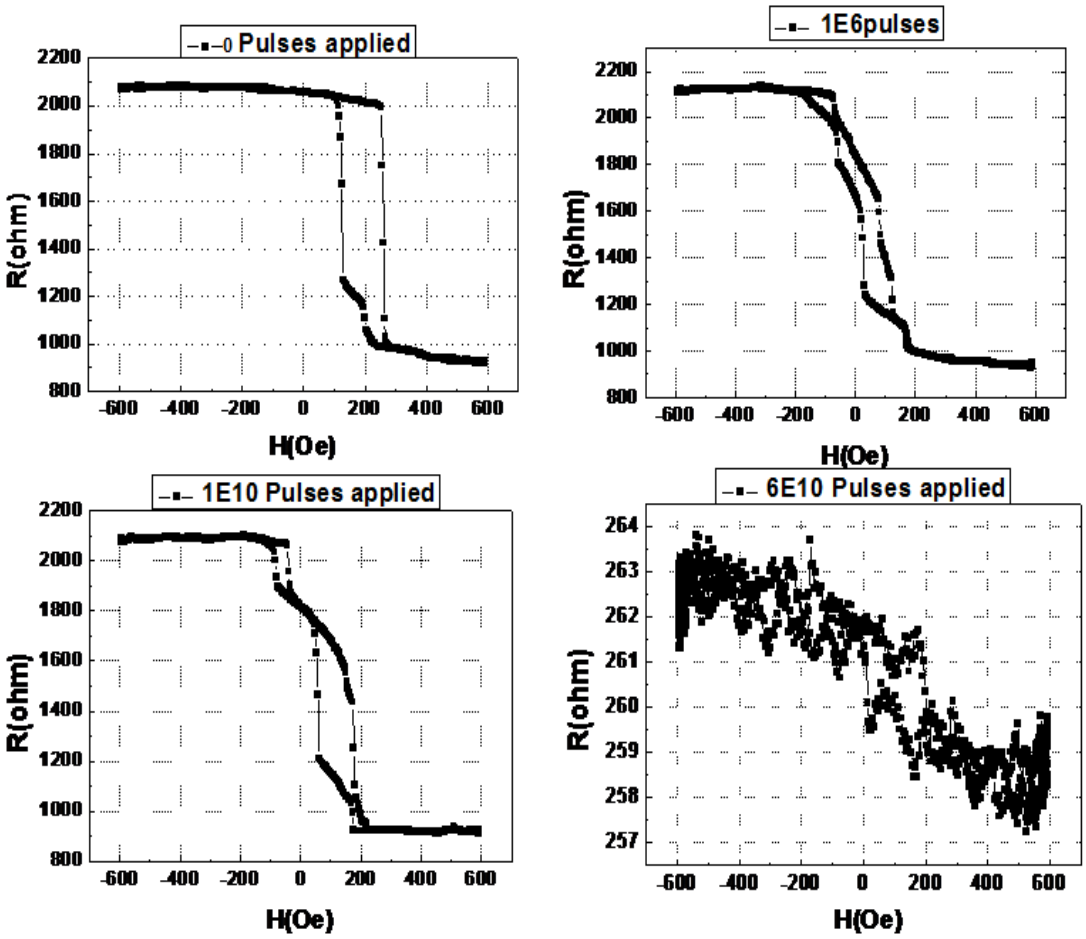

Figure III-10 - MR loops after a certain applied pulse sequence with pulse duration δ=30ns, delay between pulses Δt=70 ns and pulse amplitude V= +1.4V. Breakdown was reached after 6.10^{10} applied pulses.

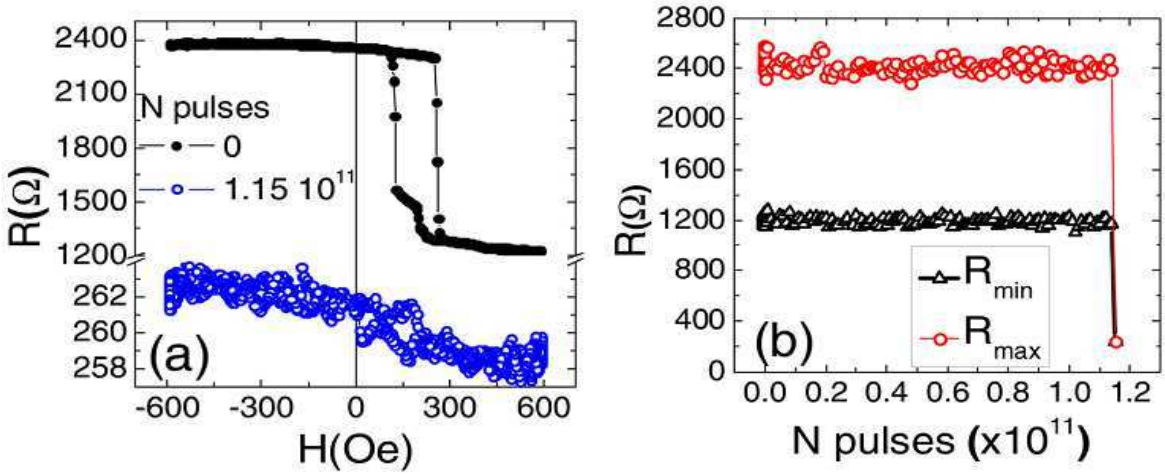

Figure III-11 - (a) TMR curves before (top loop) and after breakdown (bottom loop). For this junction, breakdown occurred after $1.15*10^{11}$ pulses of +1.3 V amplitude separated by a delay of 70 ns. (b) Evolution of R_{min} and R_{max} vs number of pulses. An abrupt drop of R_{min} and R_{max} is observed after $1.15*10^{11}$ pulses when the breakdown has occurred. The time interval and voltage used here were 70 ns and +1.3 V. RA=30 $\Omega.\mu m^2$.

The breakdown seems to be an avalanche effect occurring abruptly. Our understanding is that there are pre-existing defects in the barrier (vacancies, dislocations, traps at possible BO/MgO interface…) which trap tunnelling electrons, as we will further develop in section III.5.1.
The electrostatic interaction between the trapped electrons and the screening image charges which appear in the metallic electrodes create a stress on the barrier. This stress favors the atomic mobility through the barrier and thereby the formation of a percolation path thorugh the barrier (pinhole). This pinhole formation seems to be an avalanche effect yielding to abrupt electrical breakdown.

III.4.1.b For low RA= 2-5 $\Omega.\mu m^2$.

We performed these measurements for different wafer with different RA, different resources of deposition, oxidation and patterning. The used stack is buffer/PtMn 20 /CoFe2.5/Ru 0.85/CoFeB1.5/CoFe1.5/MgO 0.9/Mg 0.4/CoFe1.5/CoFeB 1.5/Ru 6/Ta 170 /cap (thicknesses in nm). For these wafers representing low resistance area product RA, we represent the variation of R_{max} and R_{min} after sequences of pulses.
In the stress measurements, many pre-breakdown resistance jumps and, finally, breakdown are observed. The TMR evolution describes a gradual degradation before the abrupt breakdown occurrs as shown in Figure III-12.

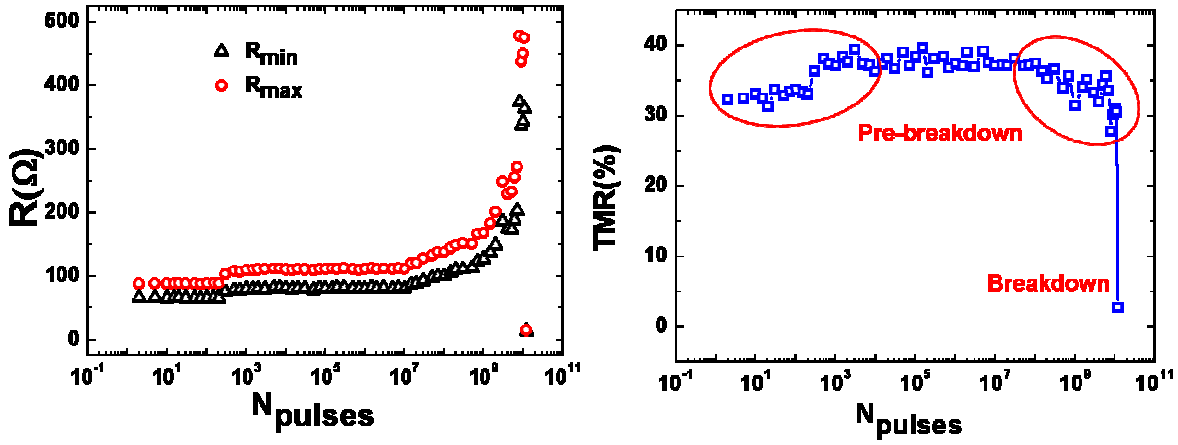

Figure III-12 – (left) Evolution of R_{min} and R_{max} vs number of pulses. Gradual degradation of R_{min} and R_{max} is observed between $1*10^7$ pulses till $1.20*10^{10}$ when the breakdown abruptly occurs. The time interval and voltage used here were 70 ns and +1.7 V. Several pre-breakdown resistance jumps are observed before the MTJ finally breaks down at $N=N_{BD}=1.20*10^{10}$ applied pulses. (right) TMR evolution vs N_{pulses}. RA=5 $\Omega.\mu m^2$.

We can also observe a stable state of R_{min} and R_{max} for a certain number of applied pulses which is followed by a gradual increase of resistance as shown in Figure III-12. On other MTJs of the same sample, we can also observe a gradual increase of resistance but also an abrupt increase of TMR (Figure III-13).
Thus, in these low RA samples, we observe two different TMR responses just before breakdown: a gradual degradation followed at the end by a TMR increase or a TMR drop.

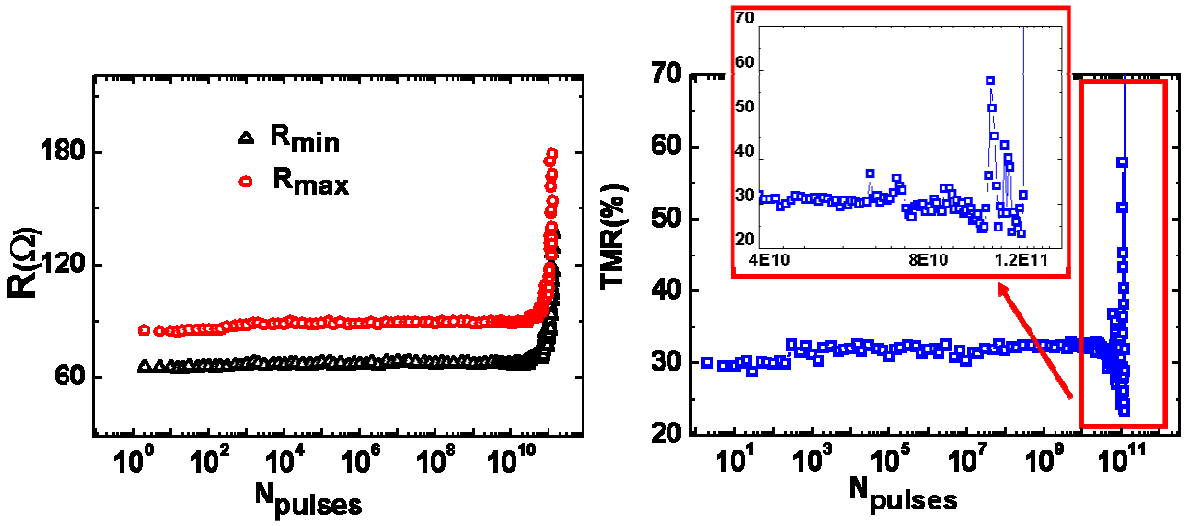

Figure III-13 - (left) R_{min} and R_{max} evolution during applying pulses. Gradual degradation of R_{min} and R_{max} is observed along the range [10^{10}-210^{11}] applied pulses. The pulse width δ=30ns, delay between pulses Δt=70ns and voltage used here +1.7 V. Gradual degradation of resistance is observed just before the breakdown occurred at $1.2*10^{11}$ pulses. (right) TMR evolution versus N_{pulses}. RA=5$\Omega.\mu m^2$.

To explain this observation, we adopt the following interpretation. These studied MTJs have an ultrathin MgO barrier (9Å) formed by natural oxidation of a Mg layer. It is very likely that these barriers present pinholes during the fabrication process. These pinholes are electrical shorts through the barrier so that the current density at their location is very high. They therefore constitute hot spots in the barrier. When the current density reaches a critical value, these hot spots can burnout and correlatively the corresponding short disappears like a fuse. Thus, the resistance increase suddenly and reach higher values as observed in Figure III-12 and Figure III-13.

It is similar to the operating principle of Conductive Bridge memory cells (CBRAM). CBRAM are composed of a thin solid state electrolyte layer (often made of mobile Ag atoms dispersed in a chalcogenide matrix) sandwiched between electrodes. At a first voltage threshold, Ag atoms diffuse in the matrix and form percolating conductive bridges between the electrodes. At a higher second voltage, these bridges can burn out and the resistance increases back to high values.

Another possible explanation of the increase of MgO barrier resistance may be related to oxygen diffusion yielding a better uniformity of oxygen in the barrier and therefore a more insulating barrier.

III.4.2 Statistical analysis and Weibull distribution

As described previously, for each value of pulse amplitude and delay between pulses Δt, the distribution of number of applied pulses leading to breakdown was determined from measurements performed on a set of 30–40 junctions.
It is well described by a Weibull distribution with a cumulative distribution F as function of time (see Figure III-16) given by :

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\eta}\right)^{\beta}\right] \qquad \text{(III-1)}$$

In our case, we will use N_{pulses} instead of time as we use pulsed conditions.

$$F(N_{pulses}) = 1 - \exp\left[-\left(\frac{N_{pulses}}{\eta}\right)^{\beta}\right] \qquad \text{(III-2)}$$

To obtain an equivalent time, we can just multiply by 30ns (pulse duration). Let's remind here that this function F(N) - measured in pulsed conditions - will not be equivalent to F(t) obtained for measurements performed with continuous application of voltage [III.8].
This distribution is characterized by two parameters:

(1) the shape parameter β , associated with the breakdown mechanism, and

(2) the scale parameter η, representing the number of pulses after which a fraction 63.2% of MTJs has failed.

At the beginning of my thesis, I started this study on samples fabricated within the laboratory with a not so good yield. Typical Weibull plots for these samples are given in Figure III-14. We see on these plots that a large amount (20%) of MTJs are broken after only 10 pulses. These "bad" MTJs are said to present an infant mortality because they have a very low endurance compared to the rest of the sample. In Figure III-15, we see the two distributions of infant mortality and good MTJs in blue ellipses.

Indeed, we first aimed at validating our experimental proceedure and our program that controlled our pulsed conditions breakdown test. For these samples with a lot of infant mortality, the Weibull distribution shows a majority of "bad" MTJs (50% are broken after only 10^7 pulses).

For MRAM application, a first step to improve reliability would be to identify and extract from the process these "bad" MTJs. The real MRAM would work only with the "good" ones.
We should precise that all following presented examples of Weibull distribution are plotted by taking in consideration only "good" MTJs, ie. removing MTJs that present an infant mortality. But, in general and for optimized samples, this infant mortality is a negligible minority in our statistical study.

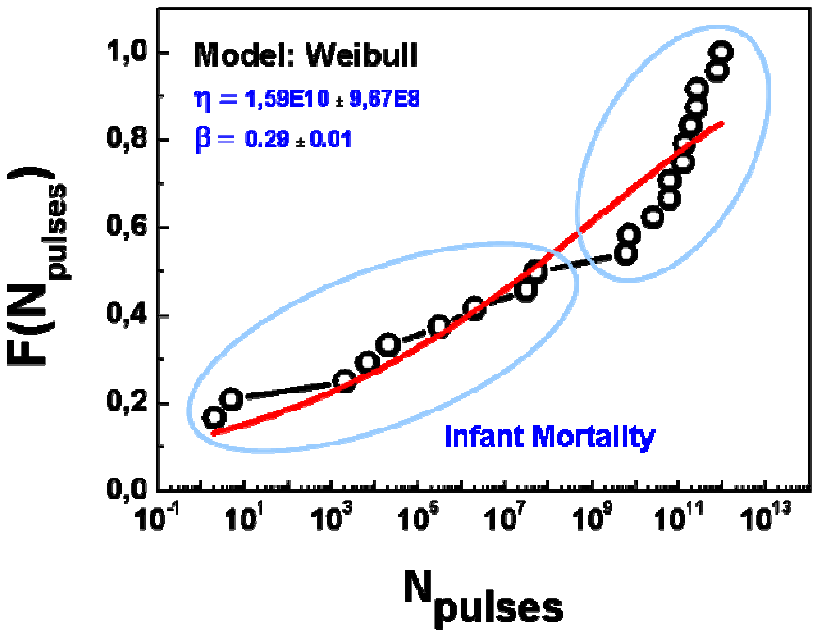

Figure III-14 - Weibull plot of the number of pulses to dielectric breakdown for V =1.60 V, δ=30ns and Δt =70 ns. The red solid line is the Weibull fit. The fitted η and β parameters are given. The studied MTJ is one of the tested set of the wafer representing RA=30 $\Omega.\mu m^2$. The blue ellipses represent the two distributions (infant mortality (lower-left ellipse) and good MTJs (upper-right ellipse)).

If we consider this example of Weibull distribution shown in Figure III-14, we can obviously see that one Weibull distribution (solid red line) doesn't describe well the distribution of studied MTJs, which justifies that the shape parameter β has a very low value $\beta << 1$ (see following section for the typical values of β). That proves that this set of 40-50 studied MTJs contains a large amount of "bad" MTJs and that two behaviors have to be taken into account. In our case, we will not further study infant mortality MTJs.

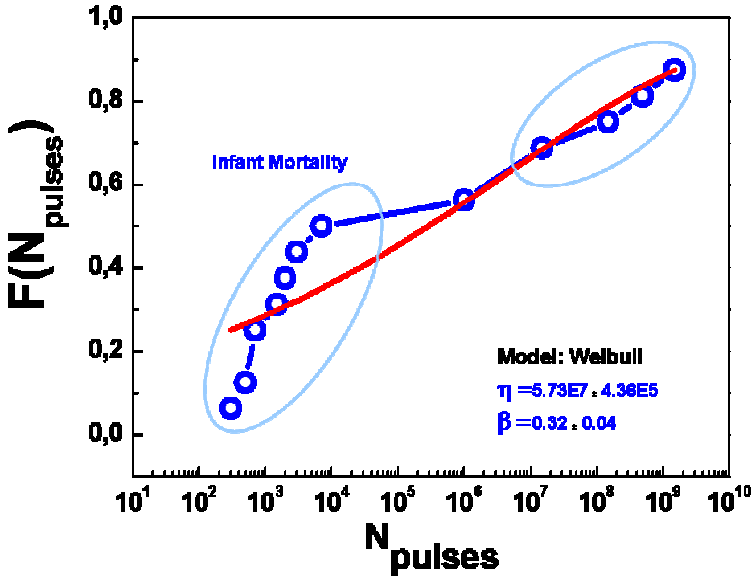

Figure III-15 – Second example of Weibull distribution presenting MTJs with infant mortality. Weibull plot of the number of pulses to dielectric breakdown for V =1.70 V, δ=30ns and Δt =70 ns. The red solid line is the Weibull fit. The fitted η and β parameters are given. The studied MTJ is one of the tested set of the wafer representing RA=25 $\Omega.\mu m^2$.

After underlying this infant mortality, that we remove from our statistical study, we have paid attention to choosing our studied samples. Before starting breakdown test, we get a mapping of the wafer to see its yield in terms of TMR response. We consider for test only good wafers presenting a maximum of operating MTJs with a TMR superior to 40%. Let us mention that the quality of the wafers that we could investigate kept on increasing during my thesis by improving the deposition conditions and patterning process.

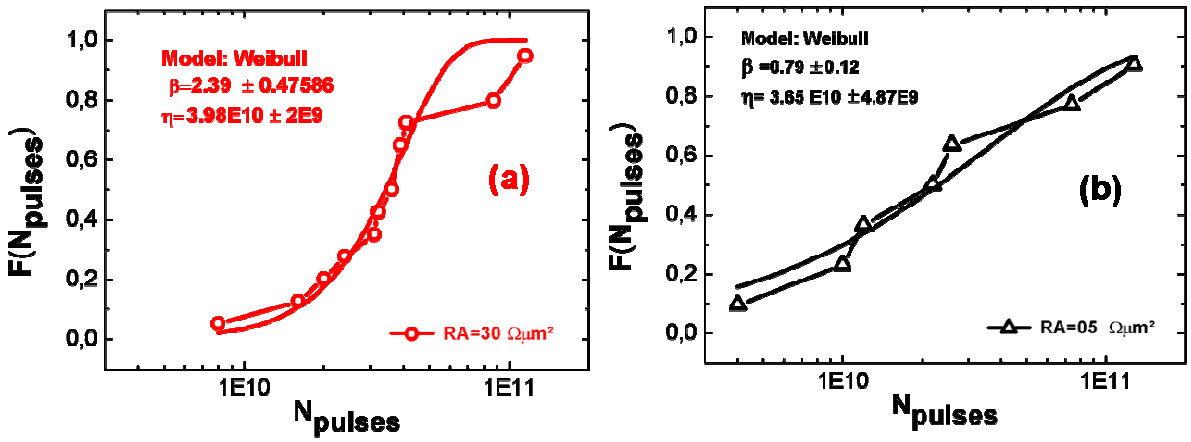

Figure III-16 - (a) Weibull plot of the number of pulses to dielectric breakdown for V =1.30 V, δ=30ns and Δt =70 ns. The red solid line is the Weibull fit. The fitted η and β parameters are given. The studied MTJ is one of the tested set of the wafer presenting RA=30 $\Omega.\mu m^2$.
(b) Weibull plot of the number of pulses to dielectric breakdown for V =1.70 V, δ=30ns and Δt =70 ns. The red solid line is the Weibull fit. The fitted η and β parameters are given. The studied MTJ is one of the tested set of the wafer presenting RA=5 $\Omega.\mu m^2$.

After selecting samples with good TMR ratio and removing infant mortality, we obtain the distribution shown in Figure III-16 (a) for high RA and Figure III-16 (b) for low RA. For a set of good MTJs (30–40 samples), the number of pulses before breakdown follows a Weibull distribution from which we can extract η the number of pulses after which 63% of the MTJs are broken in the set [III.10]. This statistical treatment gives a good representation of the behaviour of a whole MRAM chip instead of a single MTJ behaviour that would include cell to cell variability. [III.11]

For the two RA range, the Weibull distribution fits well the measured data. We have applied in these measurements pulses of positive polarity only. In both cases, η reaches a few 10^{10}, but β is much lower in the low RA case, indicating a larger amount of defective MTJs in that latter case.
If we combine the two Weibull plots we can observe the shape parameter β effect. In section II.1.1.c we have discussed the shape parameter variation and Figure II-5 shows cumulative distribution function for different β values. One can note that the Weibull plot is more flat (case of RA=5 $\Omega.\mu m^2$) see Figure III-17 than the other example of Weibull distribution showing a higher shape parameter value. We will see in fact in section III.4.3.a and Figure III.22 that this shape parameter strongly depends on the pulse voltage amplitude for each RA value. Therefore the observed difference here does not reflect an important difference between the two samples but rather the difference in voltage amplitude at which these measurements were performed.

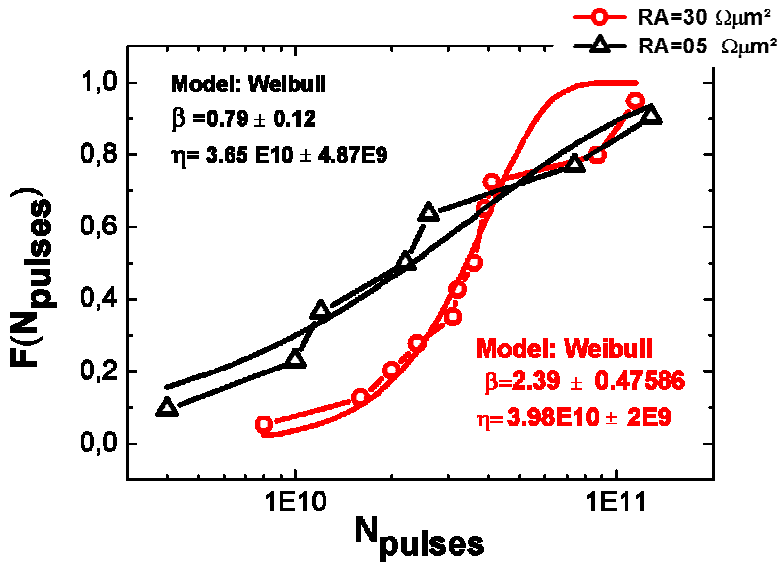

Figure III-17 - Weibull plot of the number of pulses to dielectric breakdown for two wafers representing RA=30 and 5 $\Omega.\mu m^2$.

As mentioned before in the introduction chapter, Weibull distribution can be plotted in linear form to get easily the two Weibull parameters, the shape parameter β and the scale parameter η, representing the number of pulses after which a fraction 63.2% of MTJs has failed.
In log (log) scale, the linear form of Weibull expression is given by the following expression:

$$\ln(-\ln(1-F(N))) = \beta \ln(N) - \beta \ln(\eta) \qquad \text{(III-3)}$$

β is thus the slope and η the number of pulses at which $\ln(-\ln(1-F(N)))$ is equal to zero (see Figure III-18).

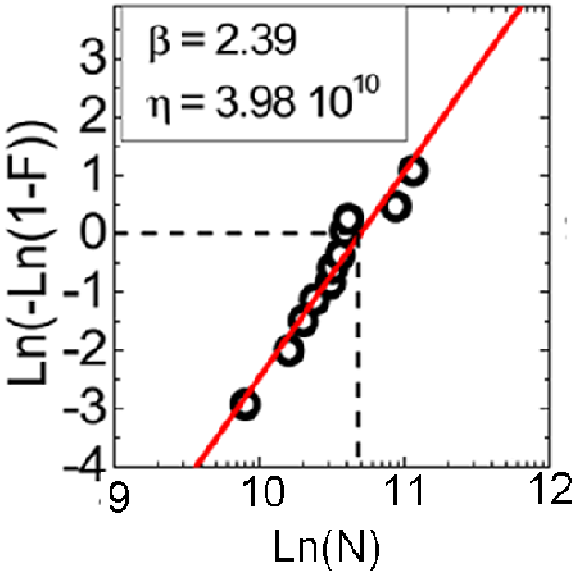

Figure III-18 - Weibull plot in linear form of the number of pulses to dielectric breakdown for V =1.30 V, δ=30ns and Δt =70 ns. The red solid line is the Weibull fit. The fitted η and β parameters are given. The studied MTJ is one of the tested set of the wafer representing RA=30 $\Omega.\mu m^2$.

Let's now see if this Weibull analysis applies to negative pulses. Similarly, we used a set of 30–40 MTJs and we applied successive negative pulses until breakdown.

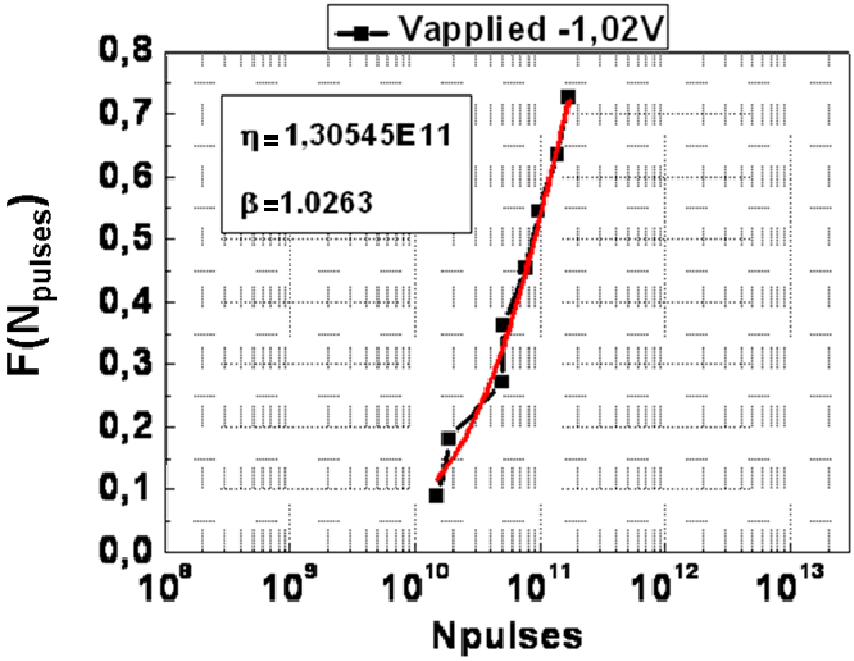

Figure III-19 - Weibull plot of the number of pulses to dielectric breakdown for V = -1.02 V, δ=30ns and Δt =70 ns. The red solid line is the Weibull fit. The fitted η and β parameters are given. The studied MTJ is one of the tested set of the wafer presenting RA=25 $\Omega.\mu m^2$.

Figure III-19 shows the distribution in that case. Similarly to the case of positive pulses, this distribution can also be fitted by a Weibull distribution..
This experimental procedure of barrier breakdown test was therefore validated for the two polarities and we will benefit from this procedure for the extrapolation to operating conditions (paragraph III-4-2) and the study of the effect of delay between pulses (paragraph III.4.3).

III.4.3 Extrapolation of endurance to operating V

In this section, we will present the evolution of the Weibull parameters with applied voltage. This will in particular allow the extrapolation of the MTJs lifetime to operating conditions, which is of interest for MRAM applications.

III.4.3.a Evolution of the shape parameter β (V)

We can clearly note that the shape parameter β of Weibull distributions can be equal, inferior or superior to unity (see Figure III-20).
The shape parameter β can be interpreted directly as follows:
A value of β <1 indicates that the failure rate decreases over time. This happens if there is significant "infant mortality", or defective items failing early and the failure rate decreasing over time as the defective items are weeded out of the population.
A value of β =1 indicates that the failure rate is constant over time. This might suggest random external events are causing mortality, or failure.
A value of β >1 indicates that the failure rate increases with time. This happens if there is an "aging" process, or parts that are more likely to fail as time goes on.

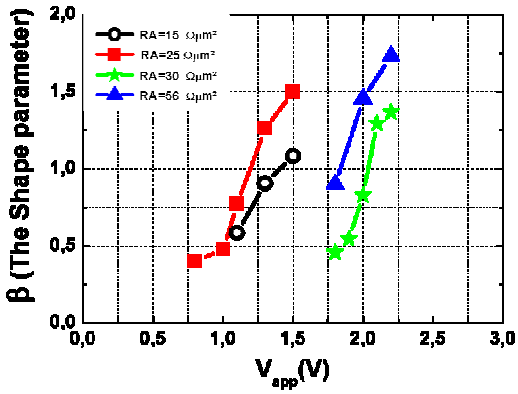

Figure III-20 - The shape parameter β as a function of applied pulses amplitudes for different value of RA.

We note that when the bias voltage increases the shape parameter β increases and exceeds unity. Indeed, for high applied voltage the "good" and "bad" (defective) MTJs behave approximately in a similar way and the difference in terms of endurance is not remarkable. Hence, the shape parameter β increases. However, when we apply low pulses amplitude, MTJs behave differently. "Good" MTJs resist well to applied pulses and have an important endurance, but defective MTJs are broken early even if we apply low amplitude because of their pre-existing defects. The difference in endurance between "bad" and "good" junctions is large at low voltage. Consequently Weibull distribution gives a lower β, lower than 1.

III.4.3.b Evolution of the scale parameter η (V) and E-model

We then studied the voltage dependence of η by stressing the MTJs with various pulse amplitudes of positive polarity (from 1.20 to 1.35 V) in the magnetic antiparallel state, for a fixed Δt of 100 ns.

The dependencies obtained are plotted in Figure III-21. The η variation was fitted to the E-model where log (η) is proportional to the electric field (E) [III.12] thus to the voltage.

This model fitted well our experimental data, and the extrapolation indicates that for these pulse conditions with an operating voltage of 0.4 V to 0.7 V typically used in STT-MRAM, the MTJs endurance can reach values over 10^{16} cycles required for use as core level memories with 10 years lifetime (see Figure III-21).

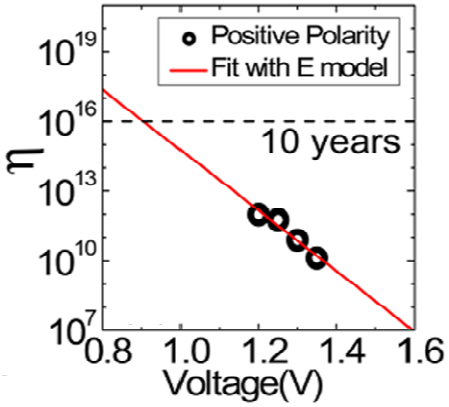

Figure III-21 -Variation of η versus applied pulses voltage for Δt=100 ns. Data were extrapolated with E-field model (red solid line) to determine the MTJs lifetime for 0.8 V pulses corresponding to an upper limit of write conditions in STT-MRAM applications. The corresponding wafer presents a RA=30 $\Omega.\mu m^2$.

III.4.3.c Influence of RA

We have tested many wafers corresponding to different RA values, obtained by changing the type of Mg oxidation and the deposition setup but for approximately the same nominal MgO thickness. It is not easy to garantee that the MgO thickness was the same especially if the samples come from different sputtering units. There is always some uncertainty on the deposition rates.

Such test helps us to qualify our samples and wafers and have an idea of the time to failure of the MTJs in operating conditions of MRAMs. We repeated the same test with the same condition of pulse width δ=30ns, the same delay between pulses Δt=100ns. The pulse amplitude range depends on the RA value.

If we summarize all these η variation of different RA, we get the result shown in Figure III-22. Surprinsingly, we note that the time to failure of 63% of studied junctions increases for junctions presenting lower RA (see Figure III-22), which is counter- intuitive. However, this can be explained by considering the different oxidation processes used to obtain these various RA and the related amount of defects which can be generated in the barrier:

-For RA= 47 $\Omega.\mu m^2$ the MgO barrier was prepared by plasma oxidation. This yields the worst MTJ reliability compared to all other samples in which the barrier was formed by natural oxidation. This lower endurance can be interpreted by the fact that plasma oxidation is aggressive and corresponds to an accelerated oxidation regime. In fact, it can yield the production of more defects within the barrier compared the natural oxidation.

-The second worst wafer with RA= 35 $\Omega.\mu m^2$ was prepared by a double natural oxidation of the MgO barrier which multiplies the risk of defects formations because the oxidation was done in two steps. For the best two wafers with natural oxidation (RA= 5 $\Omega.\mu m^2$, RA= 25 $\Omega.\mu m^2$), they were prepared also by sputtering but in a different sputtering unit (SINGULUS) ie. with different deposition conditions and different patterning process. Thus, it is difficult to compare these two last samples with the two first ones but the trend within each pair of samples is the same.

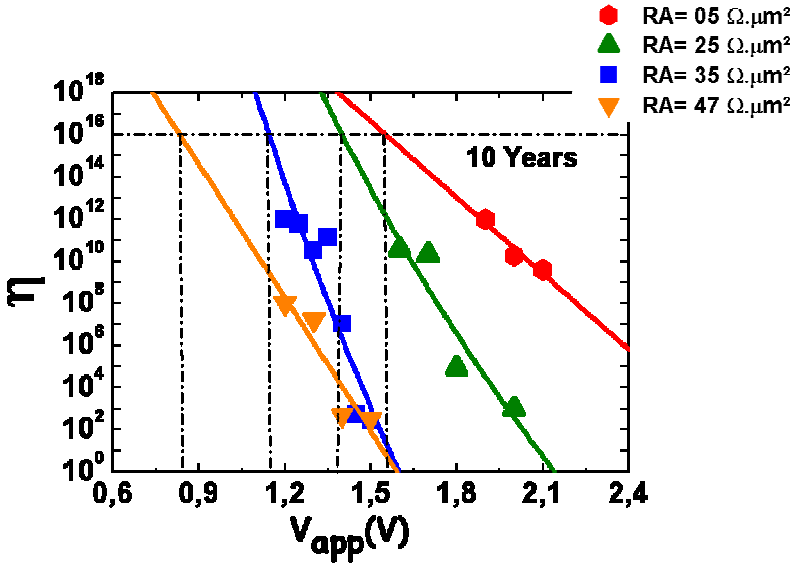

Figure III-22 -Variation of η versus applied pulses voltage for Δt=100 ns for different wafers with different resistance area product RA= 5 $\Omega.\mu m^2$, RA= 25 $\Omega.\mu m^2$, RA= 35 $\Omega.\mu m^2$ and RA= 47 $\Omega.\mu m^2$. Data were extrapolated to determine the corresponding applied voltage limit to reach the 10^{16}pulses equivalent to 10 years limit.

One point that we should precise is that the wafer with lower RA and presenting the best endurance has the following composition: buffer/PtMn 20 /CoFe2.5/Ru 0.85/CoFeB1.5/CoFe1.5/MgO 0.9/Mg 0.4/CoFe1.5/CoFeB 1.5/Ru 6/Ta 170 /cap. We note that there is an insert of Mg 0.4 nm thick and CoFe1.5nm on both sides of the barrier. Such inserts can limit the Boron migration from the electrodes to the barrier during crystallization annealing. Thus we get less interfacial defects and as a result better MTJ with better reliability.

III.4.3.d Influence of pillar dimension

For all previously presented results, the tested MTJs had the same dimension: After patterning, the final dimension of the circular pillars was 0.2μm in diameter.
As we have different dimensions in the same wafer, we studied the life time i.e. the endurance of MTJs with two different dimensions (200nm and 400nm diameter). The dependencies obtained are plotted in Figure III-23. The η variation was fitted to the E-model where log (η) is proportional to the electric field (E).
This extrapolation indicates that the endurance of smaller (0.2μm diameter) MTJs is better than for MTJs having larger 0.4μm diameter.

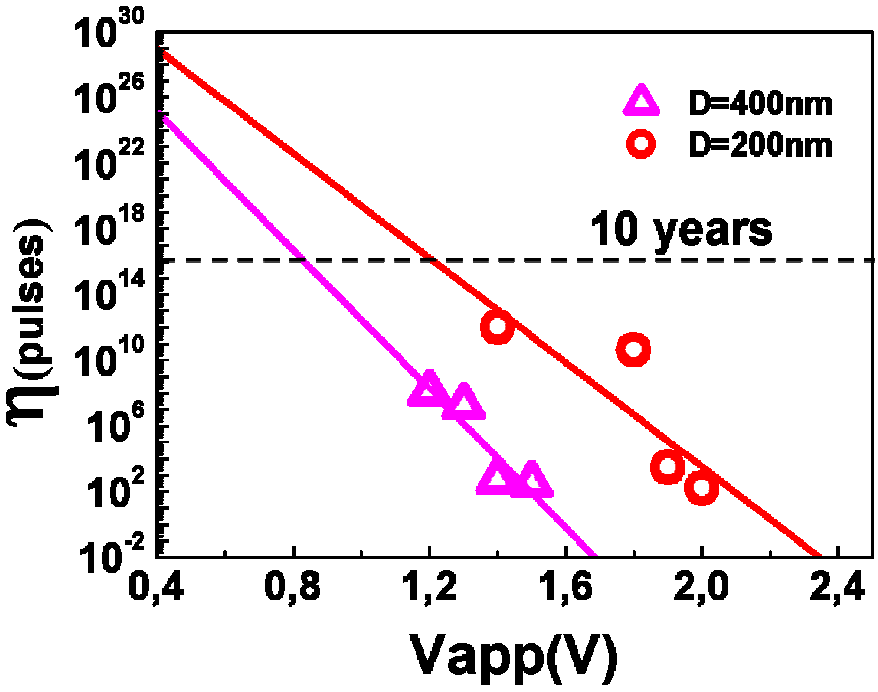

Figure III-23 -Variation of η versus applied pulses voltage for Δt=100 ns. Data represent two different MTJs dimensions. The corresponding wafer represents RA= 5 $\Omega.\mu m^2$.

This difference can be explained by the probability of presence of defects in the barrier. For larger surface, more defects are likely to be present within the barrier yielding lower endurance.
Furthermore, larger MTJ surface corresponds also to longer perimeter. As a consequence, it is more probable to have edge defects which can also yield breakdown.
All of these risks of defects are translated into lower endurance of MTJs.

III.4.4 Influence of delay between pulses:

In this part, we will discuss the effect of delay between pulses Δt for a pulse duration δ=30 ns. This time interval (Δt) was chosen as a variable parameter. Experiments were repeated for time delays between pulses from 1 ns up to 10 µs. Furthermore, as explained previously, the experiments were performed in accelerated breakdown conditions, i.e., with a corrected pulse amplitude ranging between 1.0 V and 2.0 V, corresponding to an electric field of ~ 9–18 MV/cm. This pulse amplitude is two to three times higher than that required for STT-MRAM or Thermally Assisted MRAM writing under normal operation conditions. In normal operation conditions, the Δt would be large as every MTJ would be "randomly" written.
We then studied the evolution of η as a function of the delay Δt between successive pulses. As explained above, each point is derived from endurance measurements on a set of 20–40 junctions.

III.4.4.a Unipolar versus alternative pulses:

In Figure III-24, we plot the evolution of the scale parameter η as a function of Δt. This experiment shows that the η variation exhibits two different regimes separated by a pronounced maximum for unipolar pulses.
For short delays between pulses (1 ns <Δt <100 ns), the barrier lifetime increases dramatically with Δt from rather short values for Δt<30 ns to values 4 to 10 orders of magnitude larger when Δt approaches ~ 50-100 ns.
When the delay Δt is longer than 100 ns, the opposite evolution is observed: the barrier lifetime decreases as the time between consecutive pulses increases and asymptotically reaches a value of the same order of magnitude as for short Δt in the range of investigated voltage.

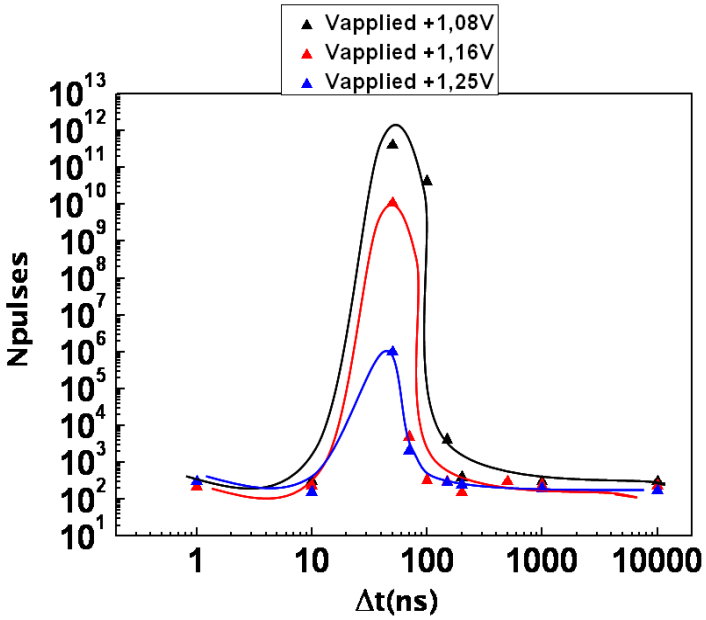

Figure III-24 - Evolution of η as a function of delay between pulses with unipolar positive pulses of various amplitudes. The corresponding wafer represents RA= 35 $\Omega.\mu m^2$. The lines are guides to eyes.

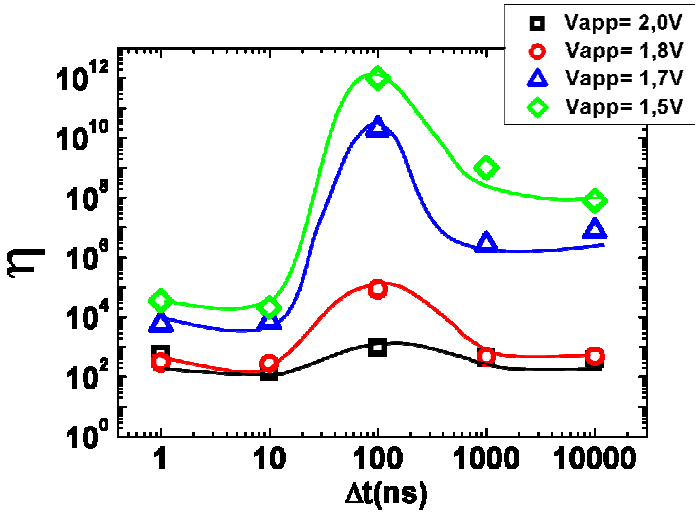

Figure III-25 - Evolution of η as a function of delay between pulses with unipolar positive pulses of various amplitudes. The corresponding wafer represents RA= 5 $\Omega.\mu m^2$. The lines are guides to eyes.

This test was performed for different wafers from different deposition conditions, different sputtering and different RA values. This increased endurance around Δt~50-100 ns was observed for all studied samples, for example RA= 5 $\Omega.\mu m^2$ (see Figure III-25), RA= 35 $\Omega.\mu m^2$ (see Figure III-24).
Moreover, such peak is observed for both pulse polarities (either positive or negative pulses) and for different pulse amplitudes with the η maximum strongly depending on the amplitude of the voltage pulses (Figure III-25 for positive pulses and Figure III-26 for negative pulses).

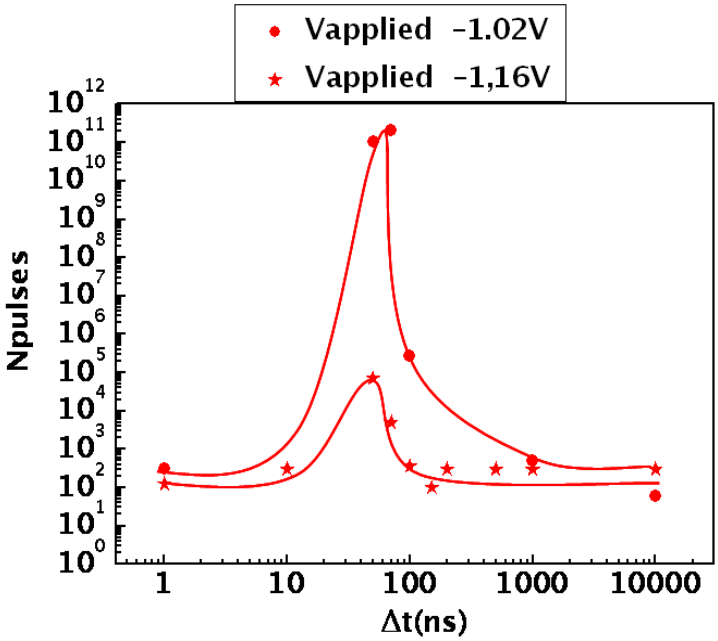

Figure III-26 - Evolution of η as a function of delay between pulses with unipolar negative pulses of various amplitudes. The corresponding wafer represents RA= 35 $\Omega.\mu m^2$. The lines are guides to eyes.

However, remarkably, the peak completely disappears when pulses of alternating polarity are used, as shown in Figure III-27 where we compared unipolar positive pulses and alternative pulses of same amplitude.

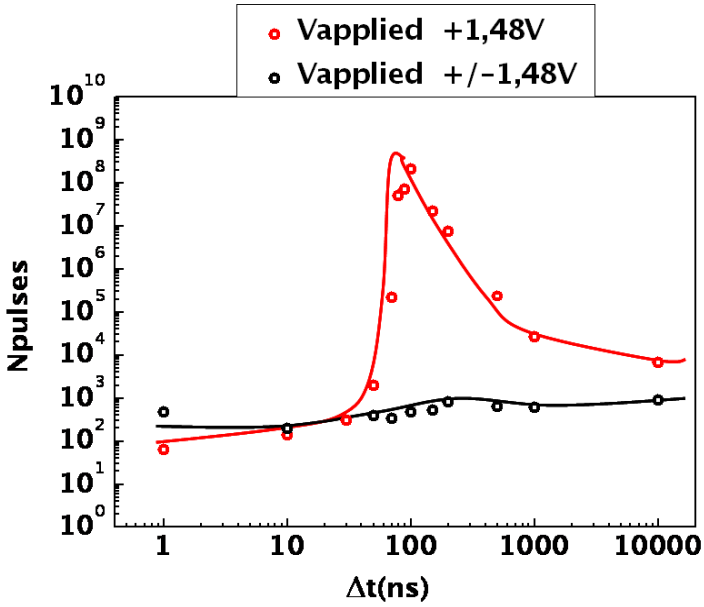

Figure III-27 - Evolution of η as a function of delay between pulses with unipolar positive and alternative pulses. The corresponding wafer represents RA= 35 $\Omega.\mu m^2$. The lines are guides to eyes.

Because of the marked difference between pulses of the same and opposite polarity, these observations cannot be explained only by a heating effect in the tunnel barrier.
That would be similar for unipolar and alternative as Joule heating does not depend on voltage sign [III.13].

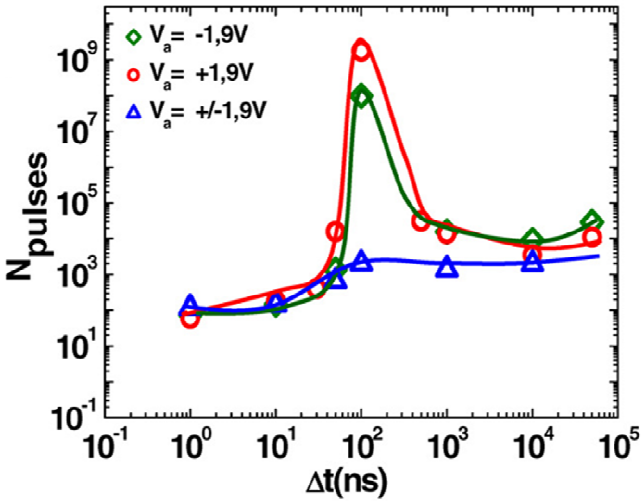

Figure III-28 - Evolution of η as a function of delay between pulses with unipolar positive or negative and alternative pulses. The corresponding wafer presents a RA= 5 $\Omega.\mu m^2$. The lines are guides to eyes.

Other wafers with different RA values were also tested. We repeated the same measurements for unipolar and bipolar pulses. Experiments (see Figure III-28) show that for both polarities, the behaviour is the same, i.e. no strong vertical or horizontal shift of the peak was observed, indicating a uniform or symmetric distribution of traps within the barrier. However for alternative pulses, the pronounced peak disappears. The vanishing of the peak for alternative pulses confirm that breakdown mechanism could not be explained with self heating effect only.

III.4.4.b Influence of pulse width:

In our previous study, we kept the pulse width constant δ=30ns. Let's now repeat the same study of endurance evolution versus delay between pulses Δt but for pulse width δ=60ns. Figure III-29 shows that the peak behaviour is still present but the peak gets broader and possibly slightly shifted towards higher Δt close to 200ns. However, more measurement points in the range Δt=80ns-200ns would be required to assess this last point.

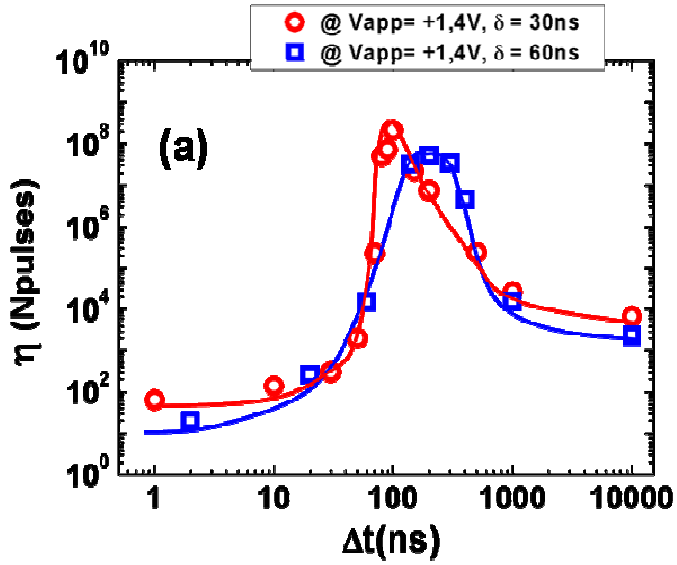

Figure III-29–Endurance of a set of MTJs as a function of the delay between pulses. Plots for positive pulses are presented for pulse width δ=30ns and δ=60ns. The lines are guides to eyes.

III.5 Interpretation of experimental results

We have shown that an optimum endurance is obtained for an intermediate *Δt* value around 100 ns. For shorter or longer *Δt*, the endurance becomes very low. We propose an interpretation of this phenomenon in terms of trapping/detrapping of electrons on defects in the barrier. We will develop in more details our charge trapping–detrapping interpretation in section III-5-2 but the main idea is as follows: For low *Δt*, we ascribe this behaviour to a heating of the MTJ and also a high level of charging of the traps within the barrier thus rendering it fragile and thus lowering its endurance. In contrast, for large *Δt*, the decrease in barrier lifetime is attributed to a large modulation of these charges within the barrier, due charge trapping during the current pulses followed by charge detrapping during the long delay between pulses. This modulation induces a strong alternating mechanical stress in the barrier, thus rendering it also fragile.
In our interpretation, the defects in the MgO barrier or at the CoFeB/MgO interface can trap electrons, thus charging the barrier. The following paragraph discusses the possible defects responsible for this trapping of electrons.

III.5.1 Traps in MgO barrier:

The presence of traps within the MTJ barrier is not good not only for reliability but also for TMR response. Discrepancies between the theoretically predicted [III.14] and experimentally

verified giant tunnel magnetoresistance (TMR) effect [[III.15],[III.16]] and the reliability issues have been generally attributed to the presence of vacancies and other structural defects within the barrier [[III.15],[III.16],[III.17]–[III.26]]. These traps can be pre-existing dislocations resulting from the lattice mismatch between CoFe and MgO (of the order of 4.3%), interstitial defects, vacancies (O or Mg) or local inhomogeneities in the oxide polariability for instance if some boron oxide has formed next to the MgO barrier during the annealing of the MTJ. Many techniques were adopted to characterize the presence of such different defects within the MgO barrier [[III.27], [III.28].]

The drop of TMR with bias voltage (V) [[III.15], [III.29], [III.30]] is also a matter of great importance, not only because of the need to understand its fundamental physical origin but also because of its impact on applications and its possible relation with reliability issues. To explain such a decrease, several mechanisms have been proposed. Some are intrinsic; they include excitation of magnons at the FM-barrier interface [III.29], the energy dependence of the spin-polarized density of states [[III.31], [III.32]]. Another is extrinsic and related to reliability: incoherent tunneling due to scattering at impurities or defects in the barrier [[III.33]-[III.35]]. A control of these defects is thus very important.
One can cite some adopted techniques to observe such different defects. For examples density of states (DOS) measurements were used to characterize the presence of oxygen vacancies (see Figure III-30). High-resolution transmission electron microscopy (HRTEM) was also used to observe and localize defects present in the barrier (see Figure III-31).

In [III.36], DOS measurements performed with a conductive AFM allow to localize oxygen vacancies and an example is shown in Figure III-30.

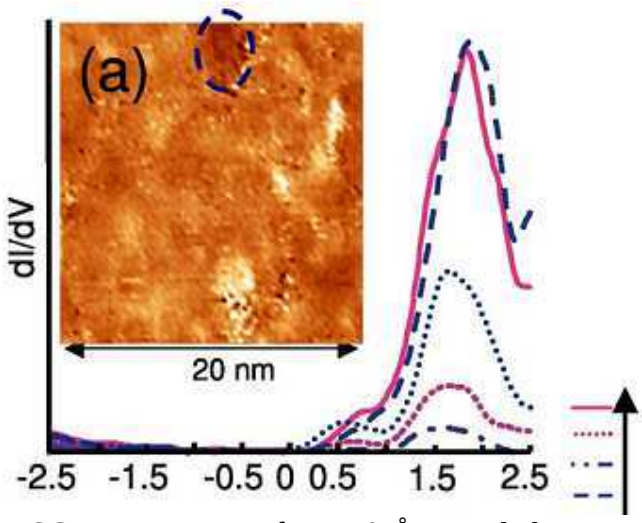

Figure III-30-[III.36] DOS measurements for a 20 Å annealed, sputter deposited MgO film, taken at the lowest points in the DOS map (inset, circled) show peaks characteristic of oxygen vacancy sites 1.75 and 0.5 V above the Fermi level.

In [III.37], the trap locations and energy levels were estimated, revealing that most traps are located in the middle of the MgO for all the studied MTJs. Based on a simple model [III.38], one can estimate both the average physical location (t_{trap}) and energy level (V_{trap}) of the traps given by:

$$V_{trap} = \frac{V_{pos}V_{neg}}{V_{pos} + V_{neg}} \qquad \text{and} \qquad t_{trap} = \frac{t_b V_{pos}}{V_{pos} + V_{neg}}$$

where V_{pos} and V_{neg} are the voltages at which the trap feature occurs in positive and negative biased Inelastic Electron Tunneling Spectroscopy IETS spectra. The t_{trap}/ $t_{barrier}$ ratios of the studied MTJs are between 0.47 and 0.53, indicating that the centroid of the probed traps is located approximately in the middle of the barrier. This is experimentally confirmed by HRTEM images (see Figure III-31), showing the presence of defect regions distributed roughly in the middle of the MgO barrier.

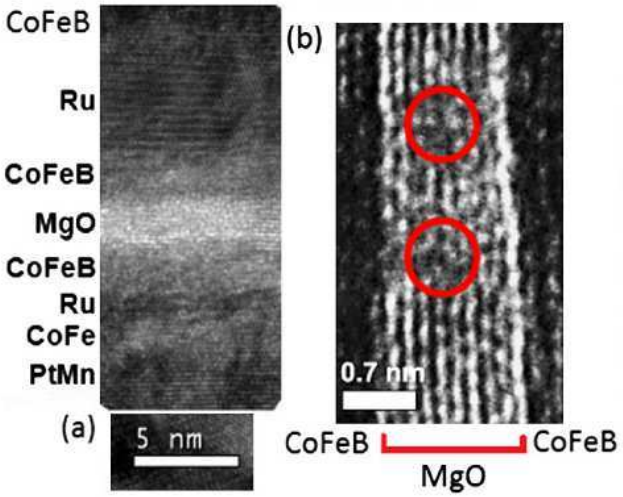

Figure III-31- (a) HRTEM picture of the MTJ stacks after annealing. (b) Enlarged image from the CoFeB/ MgO / CoFeB layers only. Circles indicate defects or disorder in the MgO barrier [III.37].

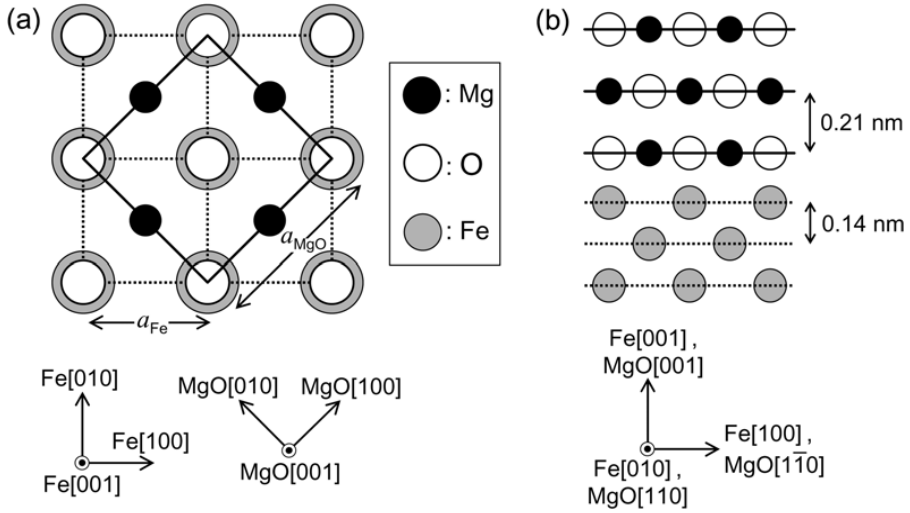

Figure III-32- Crystallographic relationship and interface structure of epitaxial bcc Fe(001)/NaCl-type MgO(001): (*a*) top view and (*b*) cross-sectional view. a_{Fe} and a_{MgO} denote the lattice constants of bcc Fe and NaCl-type MgO unit cells. [III.39]

We said before that these traps can be also pre-existing dislocations resulting from the lattice mismatch between CoFe and MgO. If we calculate the lattice constants a_{Fe} and a_{MgO} of bcc Fe

and NaCl-type MgO unit cells (see Figure III-32), we estimate this lattice mismatch of the order of 4.3%. An example of dislocations could be seen in Figure III-33 localized by circles.

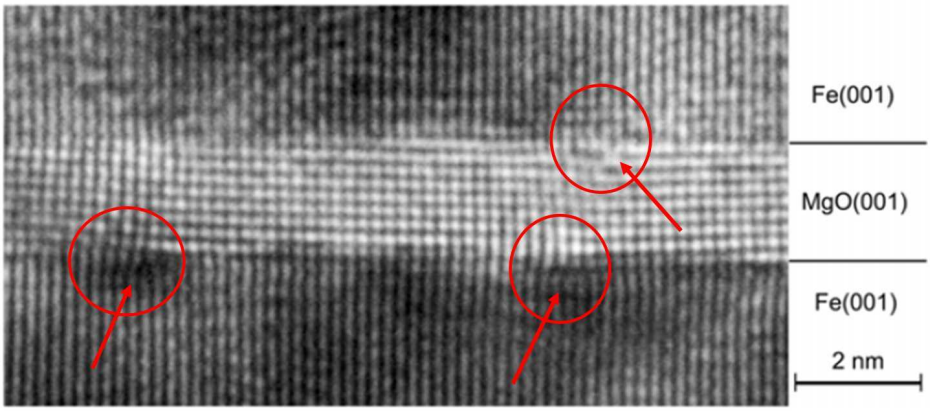

Figure III-33 - Cross-sectional transmission electron microscope (TEM) images of an epitaxial Fe(001)/MgO(001)(1.8nm)/Fe(001) MTJ. The vertical and horizontal directions respectively correspond to the MgO[001] (Fe[001]) axis and MgO [100] (Fe[110]) axis. [III.39] Red circles localize and illustrate examples of dislocations at interfaces MgO barrier/electrodes.

We have seen in our experimental results that breakdown behaviour remains the same for both polarities. This indicates that the defects that trap electrons are symmetrically distributed around the barrier (either in the middle or the same amount on each side). It would thus probably be a combination of oxide defects within the barrier and of dislocation on both sides of the barrier.

A third possible origin to the presence of traps in the MgO barrier can be related to the formation of BO next to the MgO barrier. Indeed, it is known that during the initial annealing which follows the growth of the MTJ stack, the crystallinity of the MgO barrier increases and the CoFeB electrodes which were initially amorphous, start crystallizing first at the MgO interface and gradually in the bulk of the CoFeB layer. During this CoFeB crystallization, the B has to get out-of the CoFeB layer. The B diffusion can take place either towards the MgO interface or towards the opposite interface (Ru or Ta most often). In most cases, a B getter material (Ta, Ru, Ti…) is used on the CoFeB interface opposite to the MgO layer to attract the B away from the MgO interface since the presence of B next to the MgO barrier is detrimental for the TMR amplitude and may create hot spots through the barrier. However, in some cases, some B may still diffuse towards the MgO layer. The B then tends to get oxidized in BO thus forming a BO/MgO interface. These two oxides have different dielelectric polarisabilities (α_{MgO}=3.32Å^3) [III.40] whereas (α_{B2O3}=2.43Å^3) [III.41]. This spatial variation in polarisability along the BO/MgO interface creates a local potential well for the tunnelling electrons (Ref: G.Blaise, Journ.Appl.Phys. 69 (1991) 6334) and therefore the BO/MgO interface, if any, can provide trapping sites for the electrons tunnelling through the MgO barrier.

In the presence of a lot of defects, when electrons are trapped, the oxide barrier gets more and more charged and thus fragile. Moreover, on the different types of defects, when an electron gets trapped in the barrier, a screening positive charge appears in the metallic electrodes to force the electrical field in the metallic electrode to be zero (see Figure III-34). The interaction between each trapped electron and its corresponding screening charge yields a

large electrostatic force between these two opposite charges considering the very small distance which separates them.

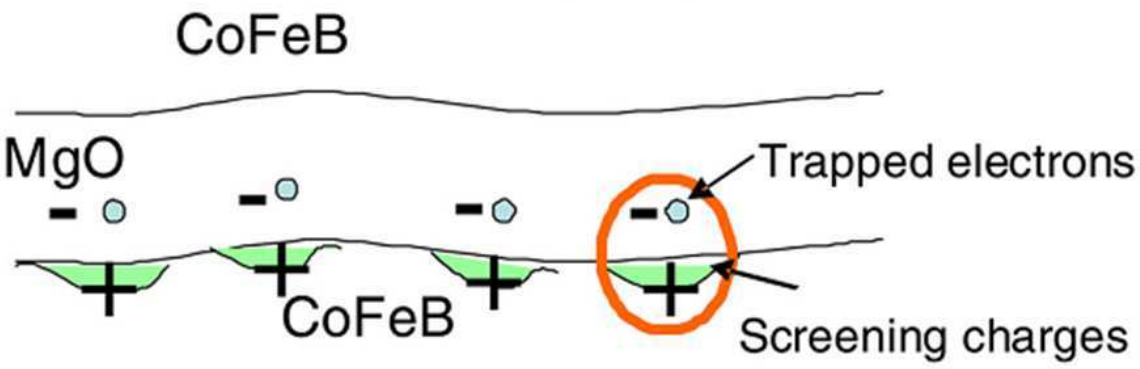

Figure III-34-Schematic representation of trapped electrons in the barrier screened by positive image charges in electrodes. The circle indicates the charges in strong electrostatic interaction generating a large local compressive stress on the barrier.

From $F = \frac{e^2}{4\pi\varepsilon_0\varepsilon_r d^2}$, this force is estimated to be ~10 nN assuming that the distance between charges (d) is half the barrier thickness.
This attractive force translates into a local compressive stress exerted on the barrier. In order to estimate the corresponding MgO lattice distortion, we first derive an order of magnitude of the MgO lattice stiffness constant k from typical phonon frequency in MgO: f=10THz [III.42] and by considering the reduced mass of MgO (m = 4.05 * 10^{26} kg).
The calculated value is then

$$k = (2\,\pi\,f)^2 * m = 160\ kg/s^2 \qquad \text{(III-4)}$$

The 10 nN force then yields a lattice distortion of the order of $\Delta x = 0.056$ A˚. This value is the same order of magnitude as the typical amplitude of vibration of atoms at room temperature in a crystal such as MgO (0.1 A˚).

Within this picture, if the traps are successively charged and discharged, a large alternative mechanical stress is generated in the barrier as a result of the electrostatic interaction between the trapped electrons and the corresponding screening charges. This alternating stress favors the atomic mobility through the barrier and therefore pinhole formation. The endurance of the barrier is thus strongly reduced when the density of trapped electrons in the barrier is high or when the time-modulation of this density is large.

III.5.2 Charge trapping/detrapping qualitative model:

We have seen previously that the charging of traps may induce strong mechanical forces on the barrier and the strong charge may break the oxide when the electric field becomes too large (dielectric breakdown). In this section, we will further develop this interpretation in

terms of charge trapping / detrapping effect based on qualitative representations of the population of trapped electrons in the barrier as represented in Figure III-35(d)–(f) .
At each pulse, some of the tunneling electrons get trapped in the barrier at trapping sites. Then between two pulses, the trapped electrons may escape from their traps with a characteristic time τ (which is ~100 ns in our experiments, see section III.4.3).

The three regimes are then interpreted as follows for unipolar pulses:

(1) The first observed regime corresponds to $\Delta t << \tau$. At each pulse, the barrier gets more and more charged up to an asymptotic regime characterized by a high density of trapped electrons. The delay between pulses does not allow the electron to escape. The barrier is then submitted to a large electrical stress which renders it more fragile. As a result, its lifetime is decreased yielding the low η value observed for short Δt.

(2) In the opposite limit $\Delta t >> \tau$, some of the tunneling electrons get trapped at each pulse but have enough time to escape from their trap between consecutive pulses (Figure III-35 (f)).
As a result, the amount of trapped charges in the barrier remains weak in average but exhibits a strong time-dependent modulation. This generates an alternating stress on the oxide barrier which also leads to a shorter lifetime. This alternating stress favours atomic mobility through the barrier, i.e., percolation path which also yields rapid breakdown.

(3) The intermediate situation with $\Delta t \sim \tau$ is the most favorable in terms of lifetime. The average amount of trapped electrons in the barrier is moderate as is the time-dependent modulation of this amount (Figure III-35 (e)), resulting in the large observed lifetime. Since the amplitude of the charge and charge modulation is proportional to the applied voltage, the peak around 100 ns is thus expected to decrease in magnitude for larger voltages, which is indeed observed (Figure III-35 (b) and Figure III-35 (c)).
For intermediate Δt (100 ns) of unipolar pulses, an optimum trade-off regime is thus obtained where the barrier is neither submitted to a large density of trapped charges nor to a strong time-modulation of these charges thus yielding an optimum endurance.
This overall picture is also consistent with the absence of peak when pulses of alternating polarity are used (Figure III-35 (a)). Indeed, in this case, electrons are trapped and detrapped at each alternating pulses whatever the delay Δt between pulses. In particular, if the electrons are trapped in dislocations close to one interface between barrier and electrode, they will be very easily detrapped when the voltage is reversed as their tunnelling thickness will be very small. This yields for any Δt to a strong time-dependent modulation of the trapped electrons density leading therefore to a behavior similar to the one observed for pulses of same polarity when $\Delta t >> \tau$.

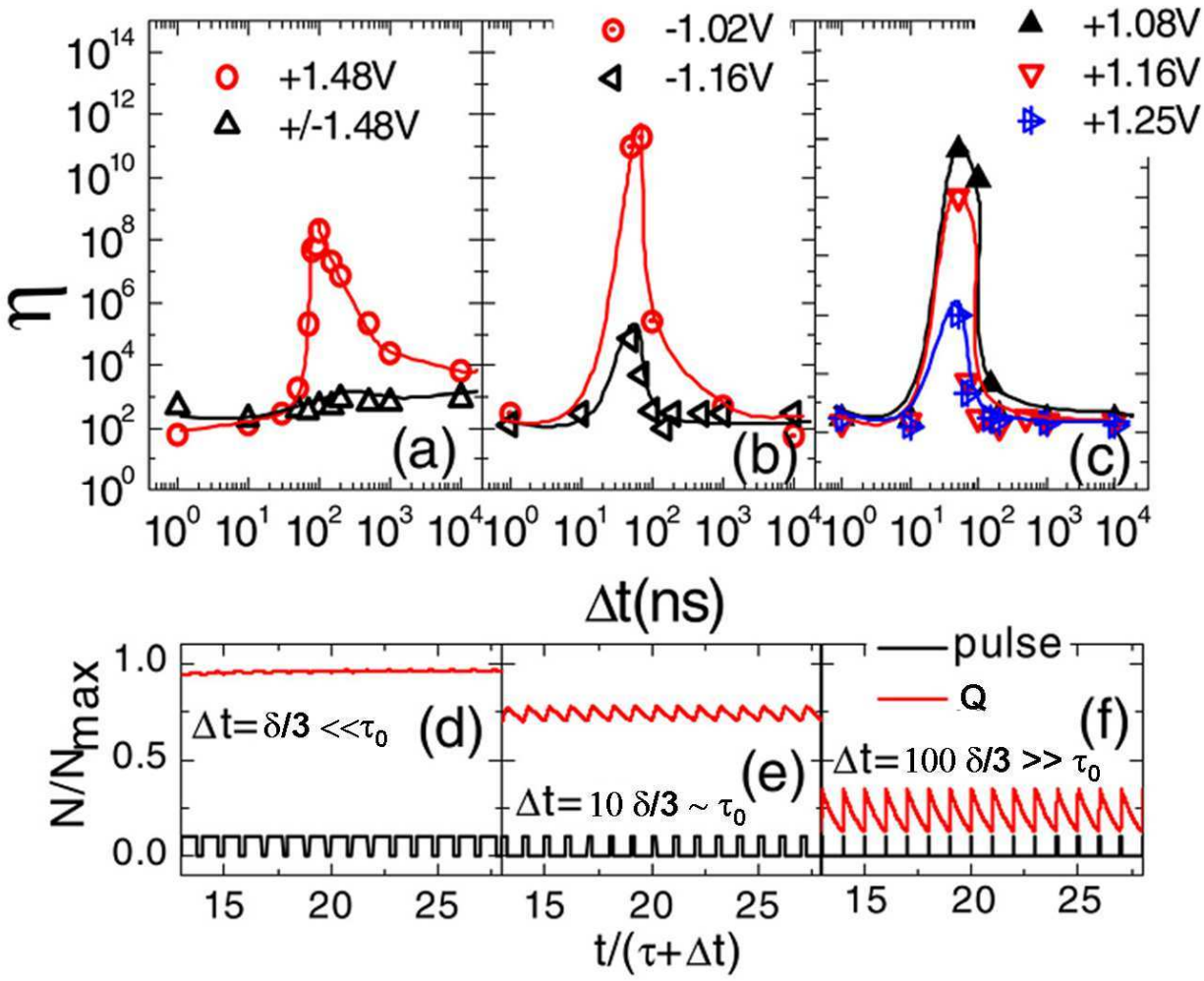

Figure III-35-Evolution of η as a function of delay between pulses, with unipolar positive or bipolar pulses (a), with negative (b) and positive (c) pulses of various amplitudes. The lines are guides to the eye. Studied samples have different RA product of 47 (a) and 30 Ωμm² (b-c). (d)-(f) Qualitative representation of the time variation of the normalized population of trapped electrons in steady state. On the horizontal axis, the time is normalized by the signal period, i.e., δt+Δt (pulse duration + delay). (d), (e), and (f) cases correspond, respectively, to short/intermediate/long delays between pulses.

This interpretation thus explains the presence of this pronounced peak for unipolarity case.
For negative voltages, the electrons flow in the other direction and the charging/discharging mechanisms remain similar. If the traps in the barrier are uniformly or symmetrically distributed in the barrier thickness, the breakdown behaviour should thus remain the same for both polarities. This would no longer be true if the traps lie only very close to one side of the barrier due to the preparation method. In our case, the symmetry between positive and negative pulses indicates uniformity and symmetrically distributed traps.

For alternating polarities, we have noted that this peak disappears. This overall picture also explains that with pulses of alternating polarities. Indeed in this case, the charge modulation is always large, and the optimum of endurance versus *Δt* is not observed. Only a low endurance is obtained, whatever the delay between pulses.

In the next modeling section, we develop in more details the calculations used in this charge trapping–detrapping model to better understand the breakdown mechanisms in MgO-based MTJs and help optimizing the endurance of these devices.
In conclusion, charge trapping/detrapping phenomena seem to play a very important role in the aging and breakdown of MgO-based MTJs. The extremely long endurance obtained for intermediate delay times indicates that MTJ lifetime can be increased for any delay between pulses in MgO barriers by reducing the amount of trapping sites. This could be achieved by avoiding the formation of boron oxide at MgO interface, avoiding the presence of oxygen vacancies in the barrier, and obtaining a better lattice matching between magnetic electrodes and MgO in order to eliminate dislocations.

III.5.3 Modelling:

In this trapping–detrapping model, we calculate the charge associated with the trapped electrons in the barrier Q as a function of time when applying the sequence of voltage pulses. We assume that there are Q_0 trapping sites in the barrier where the electrons can get trapped during tunneling.
The probability for an electron to get trapped during a tunneling event is proportional to Q_0-Q, i.e. to the number of available sites, and to the number of tunneling electrons. During one pulse, the variation of trapped charge is thus given by

$$\frac{dQ}{dt} = A\frac{I_0}{e}(Q_0 - Q) \qquad \text{(III-5)}$$

where e is the electron charge and A is a dimensionless constant representing an effective normalized cross section of electron trapping and I_0 *(=V/R* = voltage/resistance) is the current flowing through the barrier. By integrating this equation over time, one obtains

$$Log(Q_0 - Q) = -A\frac{I_0}{e}t + cte \qquad \text{(III-6)}$$

If we call Q_1 the value of Q at the beginning of the pulse (i.e. $t = t_1$), we thus have:

$$Q(t) = Q_0 - (Q_0 - Q_1)e^{-A\frac{I_0}{e}(t-t_1)} \qquad \text{(III-7)}$$

Then at the end of the pulse, the electrons may escape the traps with a certain time constant τ, thus leading to an exponential decrease in Q following:

$$Q = Q_2 e^{-\frac{(t-t_2)}{\tau}} \qquad \text{(III-8)}$$

where Q_2 and t_2 are, respectively, the charge and time at the end of the pulse, thus at the beginning of the trap discharge.

Now we can calculate the charge versus time for several pulses with a given pulse duration δ and variable delay between pulses Δt. This is shown in next section for unipolar pulses and alternative pulses with δ = 30 ns, I_0 = 1.5 mA (=V/R_{MTJ} = 1.5 V/1 kΩ), e = 1.6 × 10^{-19} C, Q_0 = 10, A = 9.78 × 10^{-18} and τ = 100 ns.

δ, I_0 are determined from experiments. Q_0 is arbitrary value. τ and A are determined so that the simulations fit the experimental results, as will be explained in the following sections.
In the next sections, we will change Δt and I_0 (via changing applied voltage).

III.5.3.a Time charge evolution:

III.5.3.a.i. For unipolar pulses:

For unipolar pulses of 1V (I_0 =1mA), we represent the charge level variation from the first applied pulse to a certain number of applied pulses for different values of delay between pulses. The Figure III-36 represents the cases of Δt = 1, 10, 100 and 1000 ns. For all of these value of Δt we calculate the charge with the same value of parameters ie. we consider that δ = 30 ns, I_0 = 1.5 mA (=V/R = 1.5 V/1 kΩ), e = 1.6×10^{-19} C, Q0 = 10, A = 9.78×10^{-18} and τ = 100 ns.
For the short delay between pulses Δt = 1 ns, we see in Figure III-36 that, after a short transient regime, Q reaches a steady state regime for which the maximum and minimum charges reach a constant value. After a short transient regime during which more and more electrons get trapped in the barrier, the trapped charge level gets close to its maximum value corresponding to the situation where all traps are full with rapped electrons. The barrier becomes quickly over charged after a few applied pulses and the oxide thus undergoes a early dielectric breakdown.
We can note for short delay the high average of trapped charge but the temporal charge modulation is weak.

For the long delay between pulses Δt = 1000 ns, we see in Figure III-36 that, the steady state regime is reached at the first pulse. Indeed, after one pulse, the delay between pulses is long enough to allow nearly total discharge of the traps. The temporal charge modulation is thus large.
If we compare the regimes of short delay and long delay between pulses, we can easily associate the large trapped charge to short delay and the large temporal charge modulation to long delay between pulses. So we can speak about to different phenomena that characterize each of these two regimes. These regimes are separated by an intermediate case characterized by both a moderate trapped charge level and a moderate temporal charge modulation as shown in Figure III-37. This is the basis or our interpretation for the presence of this pronounced peak in endurance versus delay that we observe.

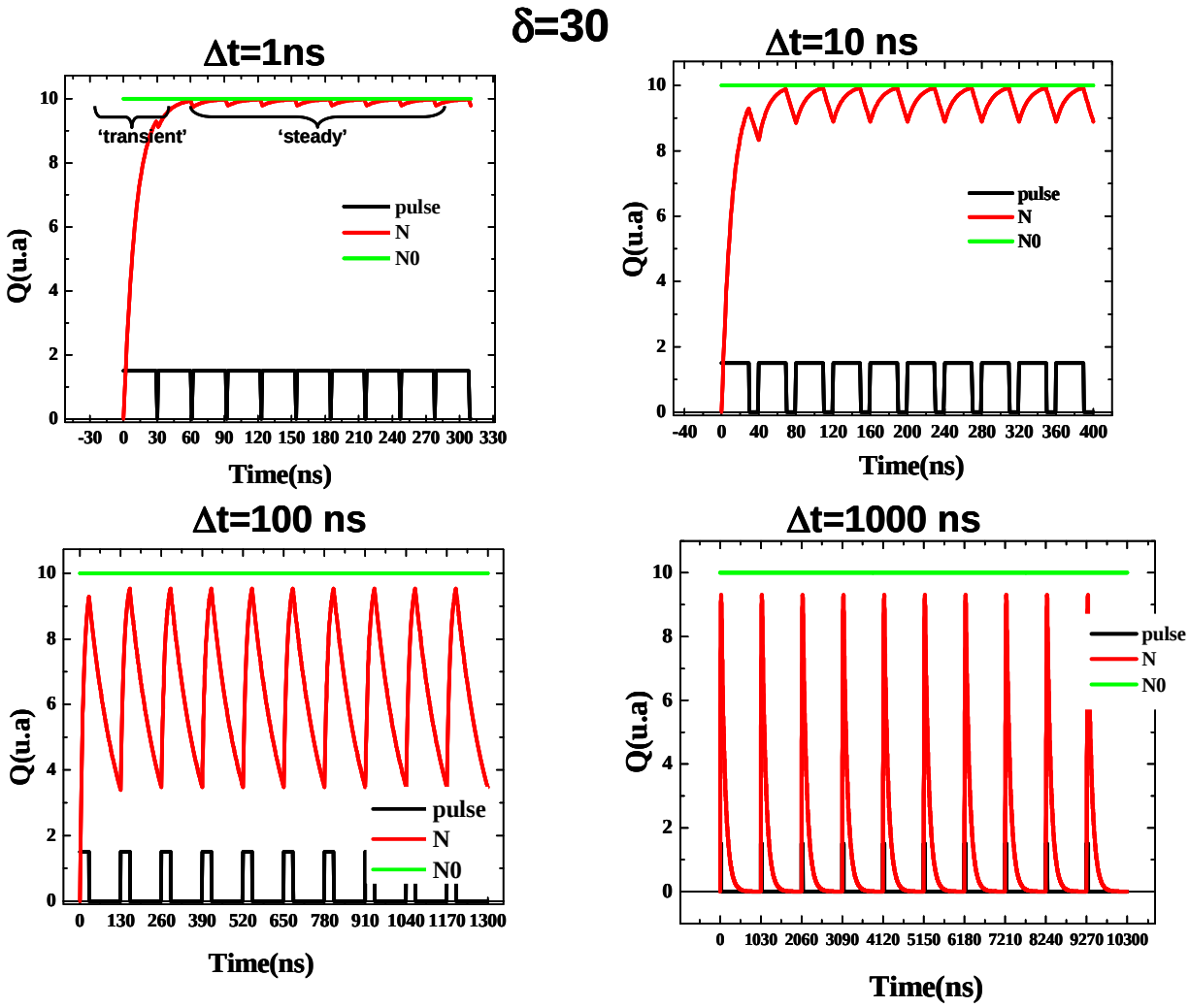

Figure III-36- Variation of charge versus applied pulses voltage for δ = 30 ns, I_0 = 1.5 mA (=V/R = 1.5 V/1 kΩ), e = 1.6 × 10^{-19} C, Q0 = 10, A = 9.78 × 10^{-18} and τ = 100 ns. The delay between pulses Δt varied from 1 ns, 10 ns, 100 ns to 1000 ns.

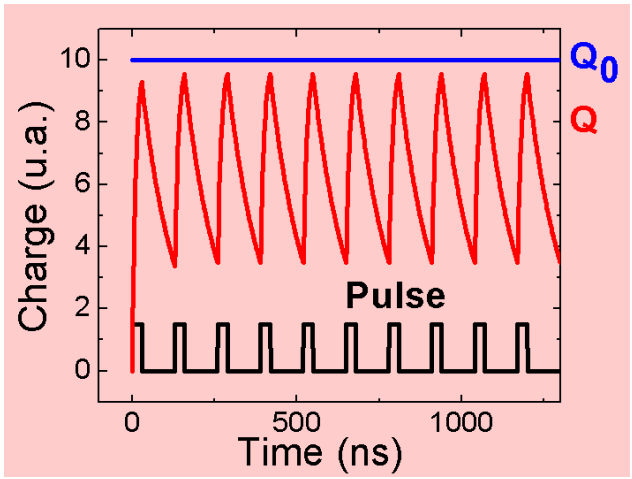

Figure III-37- Variation of charge versus applied positive pulses voltage for δ = 30 ns, I_0 = 1.5 mA (=V/R = 1.5 V/1 kΩ), e = 1.6 × 10^{-19} C, Q0 = 10, A = 9.78 × 10^{-18} and τ = 100 ns. The delay between

pulses Δt = 100 ns corresponding to moderate trapped charge level and moderate temporal charge modulation.

For negative voltages, the electrons flow in the other direction and the charging/discharging mechanisms remain similar. If the traps in the barrier are uniformly or symmetrically distributed in the barrier thickness, the breakdown behaviour should thus remain the same for both polarities, which is consistent with our experimental result showing symmetry in breakdown behaviour for both polarities (see Figure III-28).

III.5.3.a.ii. For alternative pulses:

Let's now study the alternative pulses effect. We have previously discussed the fact that the endurance peak around 100ns observed for pulses of same polarity disappears when pulses of alternating polaritites are used (see Figure III-27). As explained previously, this indicates that the breakdown mechanisms are not only linked to heating effects of the barrier, which would give similar results for positive, negative and alternative pulses. With our model, we have calculated the charge within the barrier versus time for these alternative pulses. For the first pulse, this is similar to the case of unipolar pulses.
Then after the delay, the traps are partially discharged. After that a pulse with an opposite polarity is applied. It accelerates the discharge of the already charged traps, in particular those close to one electrode that were the first to be charged and eventually charges other traps from the opposite electrode. We have modeled that by setting the voltage and number of traps to

$$(-1)^{i+1}V \quad \text{and} \quad (-1)^{i+1}Q_0$$

respectively, where *i* is the number of the pulse. The charge within the barrier is not really changing sign as we still trap electrons, but the side from which electrons are coming is. To obtain charge within the barrier, we thus take the absolute value of the calculated charge, as represented in Figure III-38 for the same parameters as in Figure III-37. We see that in that case, the minimum value of charge is zero whereas for unipolar pulses it was a non-zero value.

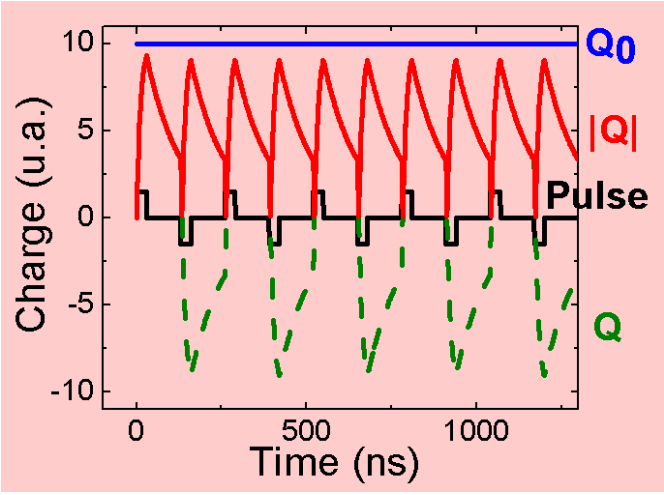

Figure III-38- Variation of charge versus applied alternative pulses voltage for δ = 30 ns, I_0 = 1.5 mA (=V/R = ±1.5 V/1 kΩ), e = 1.6 × 10^{-19} C, Q_0 = 10, A = 9.78 × 10^{-18} and τ = 100 ns. The delay between pulses Δt = 100 ns.

For the alternative polarity, the large temporal charge modulation is present whatever the delay between pulses. The endurance is thus lowered due to this charge modulation for all ranges of Δt.

III.5.3.b Breakdown probabilities:

Then in order to correlate the time evolution of charge within the MTJs with its endurance, we have calculated the breakdown probability of the MTJ from *Q(t)* using three breakdown mechanisms. First, as discussed previously, we have observed that for short delays, the charge within the MTJ is large, thus leading to poor endurance, i.e. early breakdown. In contrast, for large delays, the modulation of charge during time is large, also leading to poor endurance. We can thus define two first breakdown probabilities: breakdown due to the average charge within the device, named P_c (section III-5-3-b-i) and breakdown due to the modulation of trapped charges named P_m (section III-5-3-b-ii). Moreover, as an electric field is applied to the oxide barrier, we will take into account a direct dielectric breakdown probability named P_d (section III-5-3-b-iii). We will also discuss the influence of temperature in breakdown (section III-5-3-b-iv).

To calculate the first two probabilities directly linked to the charges present in the barrier, we assume that in steady state, the density of trapped charges remaining at the end of the discharge following a given voltage pulse corresponds to the initial density of trapped charges at the beginning of the voltage pulse. A simple calculation then yields the average density of trapped charges in the barrier Q_{av} as well as the amplitude of the time-modulation of this density ΔQ.
Considering the extreme values of the density of trapped charges Q_{max} and Q_{min}, the average charge sustained by the barrier is given by:

$$Q_{av} = \frac{(Q_{max} + Q_{min})}{2} \qquad \text{(III-9)}$$

and the modulation of charge by:

$$\Delta Q = (Q_{max} - Q_{min}) \qquad \text{(III-10)}$$

To calculate these probabilities, we use the extreme values of charge Q_{max} and Q_{min} for the last pulse, ie. in the steady regime, we use equation (III-6) and (III-7) where $Q_1 = Q_{min}$ and $Q_2 = Q_{max}$, we thus obtain:

$$Q_{max} = Q_0 \frac{1 - e^{-A\frac{I_0}{e}\delta}}{1 - e^{-(A\frac{I_0}{e}\delta + \frac{\Delta t}{\tau})}} \qquad \text{(III-11)}$$

and

$$Q_{\min} = Q_0 \frac{1-e^{-A\frac{I_0}{e}\delta}}{e^{\frac{\Delta t}{\tau}} - e^{-A\frac{I_0}{e}\delta}} \qquad \text{(III-12)}$$

From equations (III-13) and (III-14) in steady state, one derives:

$$Q_{av} = \frac{Q_0}{2} \frac{1+\exp\left(\frac{\Delta t}{\tau}\right)}{1+\frac{\left[\exp\left(\frac{\Delta t}{\tau}\right)-1\right]}{\left[1-\exp\left(-\frac{AI_0\delta}{e}\right)\right]}} \approx \frac{Q_0}{2} \frac{1+\exp\left(\frac{\Delta t}{\tau}\right)}{1+\frac{e}{AI_0\delta}\left[\exp\left(\frac{\Delta t}{\tau}\right)-1\right]} \qquad \text{(III-15)}$$

And

$$\Delta Q = Q_0 \frac{\exp\left(\frac{\Delta t}{\tau}\right)-1}{1+\frac{\left[\exp\left(\frac{\Delta t}{\tau}\right)-1\right]}{\left[1-\exp\left(-\frac{AI_0\delta}{e}\right)\right]}} \approx Q_0 \frac{\exp\left(\frac{\Delta t}{\tau}\right)-1}{1+\frac{e}{AI_0\delta}\left[\exp\left(\frac{\Delta t}{\tau}\right)-1\right]} \qquad \text{(III-16)}$$

For the alternative pulses,

$$Q_{\max} = Q_0 \frac{1-e^{-A\frac{I_0}{e}\delta}}{1+e^{-(A\frac{I_0}{e}\delta+\frac{\Delta t}{\tau})}} \quad \text{and} \quad Q_{\min} = Q_0 \frac{1-e^{-A\frac{I_0}{e}\delta}}{e^{\frac{\Delta t}{\tau}}+e^{-A\frac{I_0}{e}\delta}}$$

$$Q_{av} = \frac{Q_0}{2} \frac{1-e^{-A\frac{I_0}{e}\delta}}{1+e^{-(A\frac{I_0}{e}\delta+\frac{\Delta t}{\tau})}} \left(1+e^{\frac{-\Delta t}{\tau}}\right) \text{ and } \Delta Q = Q_0 \frac{1-e^{-A\frac{I_0}{e}\delta}}{1+e^{-(A\frac{I_0}{e}\delta+\frac{\Delta t}{\tau})}} \left(1-e^{\frac{-\Delta t}{\tau}}\right)$$

All is ready now to calculate the different breakdown probabilities for unipolar and bipolar applied pulses and see their dependences of delay between pulses.

III.5.3.b.i. Breakdown probability due to trapped charges:

From these values, we can thus calculate the breakdown probabilities. The breakdown due to the average trapped charge within the barrier is given as following:

For unipolar:
$$P_c = \frac{Q_{av}}{Q_0} \approx \frac{1}{2}\left[\frac{1+\exp\left(\frac{\Delta t}{\tau}\right)}{1+\frac{e}{AI_0\delta}\left[\exp\left(\frac{\Delta t}{\tau}\right)-1\right]}\right] \quad \text{(III-17)}$$

.

If we represent P_c as a function of delay between pulses for the two cases of unipolar and alternative pulses, we can get these two figures (see Figure III-39).

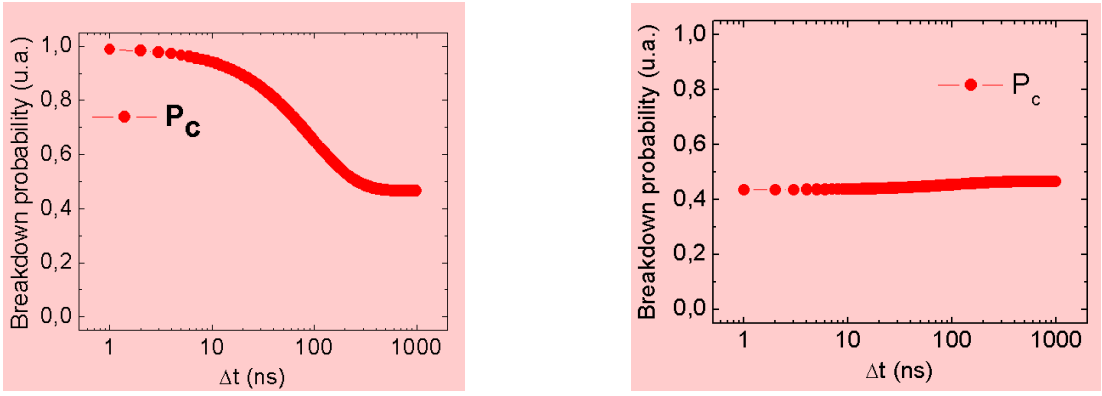

Figure III-39–Breakdown probability due to the average of trapped charge as a function of delay between pulses for positive pulse polarity (left) and alternative pulse polarity (right).

For unipolarity, the breakdown probability due to the average of trapped charge within the barrier is large for short delay. This probability decreases when the delay between pulses becomes larger and larger. The charge probability reaches his maximum for shorter delay (Δt=1ns) and decrease to a minimum constant value for Δt > 1000ns.
For bipolarity, the breakdown due to trapped charge is nearly independent of delay between pulses and represents a moderate level close to P_c=0.5.

III.5.3.b.ii. Breakdown probability due to charge modulation:

The breakdown due to the temporal charge modulation within the barrier is given as following:

For unipolar:
$$P_m = \frac{\Delta Q}{Q_0} \approx \left[\frac{\exp\left(\frac{\Delta t}{\tau}\right)-1}{1+\frac{e}{AI_0\delta}\left[\exp\left(\frac{\Delta t}{\tau}\right)-1\right]}\right] \quad \text{(III-18)}$$

If we represent P_m as a function of delay between pulses for the two cases of unipolarity and bipolarity we can get these two figures (see Figure III-40).

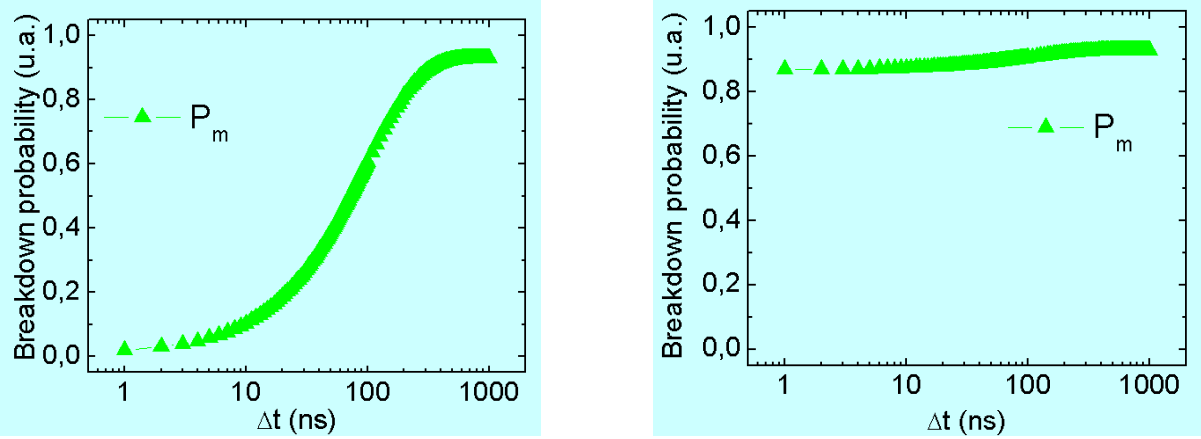

Figure III-40- Breakdown probability due to the temporal charge modulation as a function of delay between pulses for unipolar pulse (left) and alternative pulse polarity (right).

For unipolarity, the breakdown probability due to temporal charge modulation within the barrier is large for long delay. This probability increases when the delay between pulses becomes larger and larger. The charge probability reaches its maximum for longer delay (Δt=1000ns) and represent minimum value for Δt <100ns.
For alternative pulses, the breakdown due to temporal charge modulation is nearly independent of delay between pulses and represents a high level close to the unity. This important and interesting value of P_m is well justified as the alternative pulses represent a large modulation between two extremes values of trapped charges within the barrier.

III.5.3.b.iii. Direct breakdown probability:

It has also been observed in SiO_2-based capacitors [III.43] that independently of the defects within the barrier, i.e. in an ideally perfect oxide, breakdown can occur, depending on the value of the applied voltage. In SiO_2-based systems, this breakdown is attributed to a field-induced distortion of atomic bond in the oxide barrier and results in the so-called *E*-field model. This model is also used in the case of MgO-based MTJs [III.35]. In this model, the average time to breakdown is given by

$$t(E) = Ce^{-\frac{E}{B}} \qquad \text{(III-19)}$$

Where *E* is the electric field in the oxide, *C* and *B* are constants.
Here, we rewrite this equation as

$$t(V) = t_0 e^{\frac{(V_c - V)}{\Delta V}} \qquad \text{(III-20)}$$

where V is the voltage on the oxide, V_c is a critical voltage above which breakdown occurs at a very short time scale compared with the time scale used in the experiment, ΔV corresponds to the width of this transition and t_0 is a typical breakdown time.
The associated breakdown probability $P_d(t)$ linked to this direct breakdown mechanism may thus be expressed as

$$P_d(t) = (1 - e^{-\frac{t}{t(V)}}) \quad \text{(III-21)}$$

For pulsed conditions, this direct breakdown probability will be calculated for the pulse length $P_d(\delta)$. Indeed, the probability will increase while the voltage is applied whereas it will not change between two pulses. Direct breakdown is thus completely independent of delay between pulses as its expression depends only on the applied voltage amplitude and duration.
We plot the direct breakdown probability versus the delay between pulses and we can observe in Figure III-41 that this probability have a constant value for the two types of polarities unipolar and alternative as we apply the same pulse amplitude of V=1.5V on the barrier. The sign of the voltage will not change the resulting bond distortion, just their direction.
V_c and ΔV have been adjusted to fit experimental results as explained in section II-5-3-b.

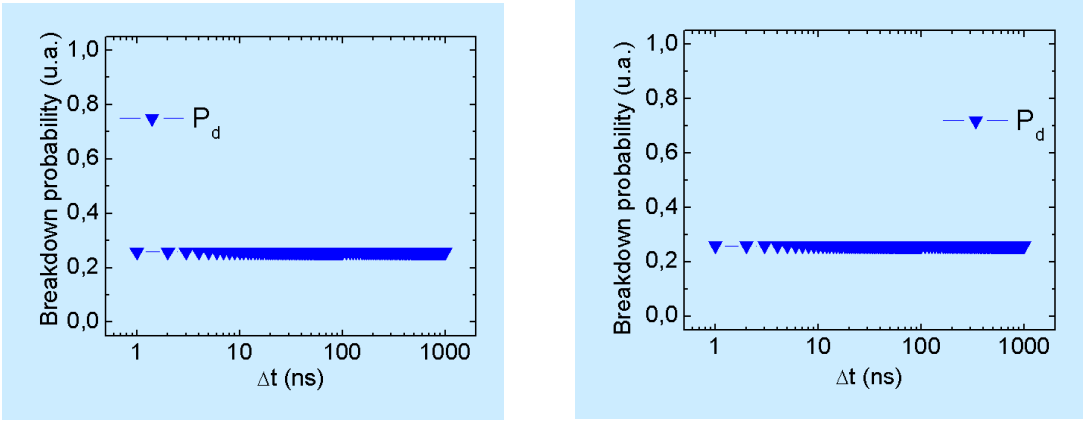

Figure III-41– Direct Breakdown probability as a function of delay between pulses for positive pulse polarity (left) and alternative pulse polarity (right).

III.5.3.b.iv. Total Breakdown probability:

To summarize, we consider in our model these three breakdown mechanisms, one due to the average density of charges trapped in the barrier, one due to the time-modulation of this trapped charge and one due to electric field-induced distortion of bonds in the barrier.
The total breakdown probability P will be high if at least one of the three aforementioned mechanisms has a large contribution. Hence P is given by:

$$1 - P = (1 - P_c) \times (1 - P_m) \times (1 - P_d) \quad \text{(III-22)}$$

This equation represents the fact that if one of the breakdown probabilities is large, then the overall breakdown probability will also be large.

For pulses of duration δ=30ns, we have calculated all these breakdown probabilities as a function of Δt and plotted them in Figure III-42 for unipolar pulses and Figure III-45 for alternative pulses for V=1.5V. The used parameters are R=1kΩ, A=9.78 10^{-18}, τ=100ns, δ=30ns, V_c=1.5V and ΔV=0.25V. These values are either given by the system (R, δ) or have been optimized to fit the experimental data (V_c, ΔV, τ, A).

If we combine these three breakdown probabilities P_c, P_m and P_d, as shown in Figure III-43 for unipolar pulses, we can see that for each range of delay between pulses one of these breakdown probabilities dominates. For the short delays, the breakdown probability P_c due to the average density of charges trapped in the barrier is large and the breakdown probability due to the time-modulation of this trapped charge is weak. In contrary, for long delay between pulses the breakdown probability due to the time-modulation P_m is really large while the one due to the average density of trapped charges is low.

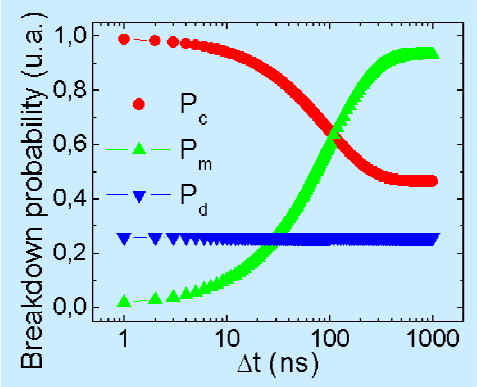

Figure III-42- Calculated breakdown probabilities separated in breakdown due to charge Pc, due to charge modulation Pm and due to direct breakdown Pd .

To calculate the total breakdown probability, we combine the three breakdown probabilities and we plot the total breakdown probability as a function of delay between pulses. In Figure III-43 , P is presented in black. It exhibits a minimum close to Δt=100ns.

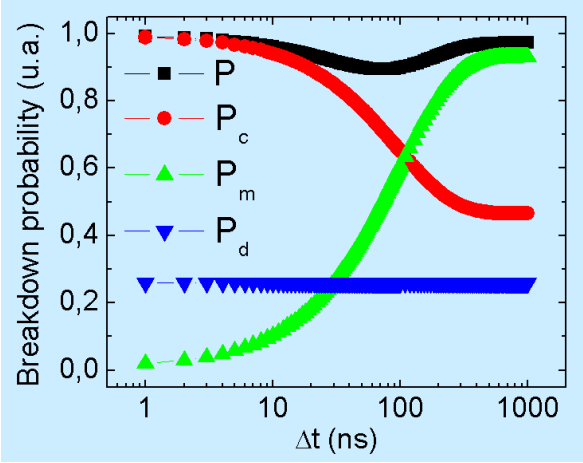

Figure III-43- Calculated breakdown probabilities separated in breakdown due to charge P_c, due to charge modulation P_m and due to direct breakdown P_d for unipolar pulses. The overall breakdown probability P presented in black is the total breakdown probability.

To calculate the endurance and plot its dependence on delay between pulses, we calculate the non breakdown probability or the endurance (1-P) by the formula (III-25) mentioned before. We obtain the peak observed experimentally for $\Delta t \approx 100ns$ shown in Figure III-44. We will see in the next section that the escape time τ is the parameter determining the position of this peak.

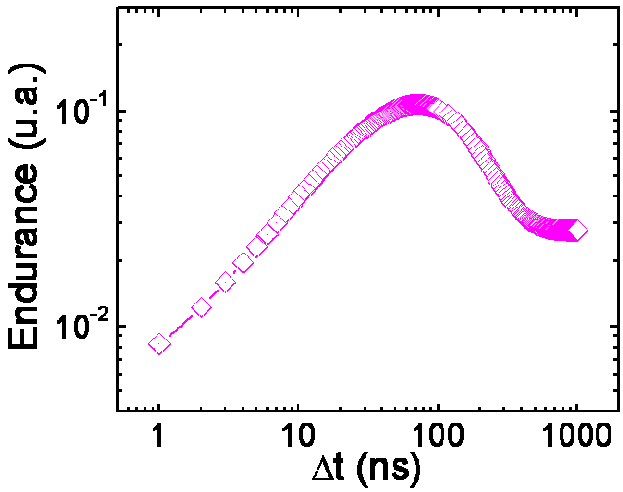

Figure III-44– Plot of (1 − P), the non-breakdown probability, also representing the endurance of the barrier, for unipolar pulses. The parameters are the same as in Figure III-43.

We did the same calculation for pulses of alternating polarity with the same parameters as previously. We calculate the three breakdown probabilities and the total breakdown probability P and we present them in the Figure III-45.

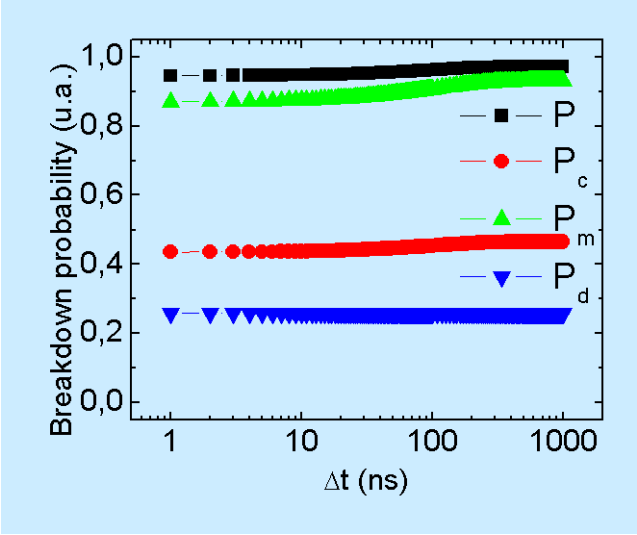

Figure III-45- Calculated breakdown probabilities separated in breakdown due to charge P_c, due to charge modulation P_m and due to direct breakdown P_d for alternative pulses. The total breakdown probability P presented in black is the total breakdown probability.

We represent the endurance (1-P) in Figure III-46. We observe that the peak around 100ns is no more present, consistently with experiments.

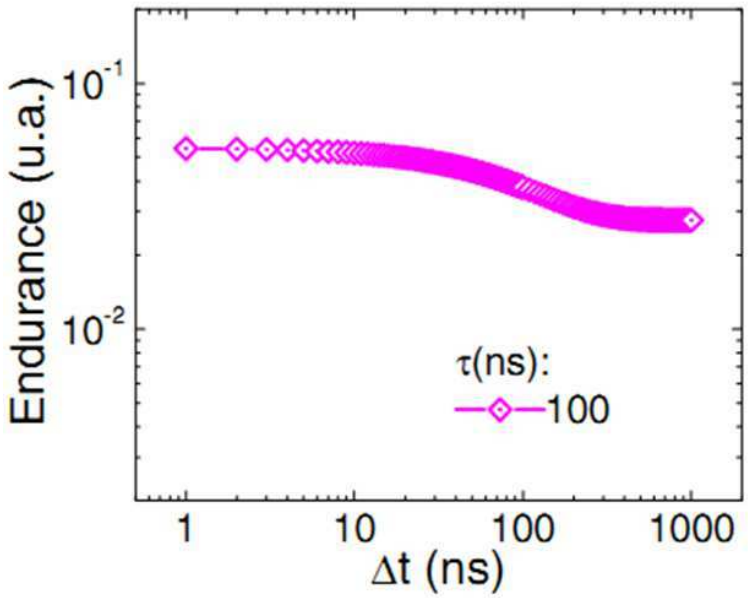

Figure III-46– Plot of (1 − P), the non-breakdown probability, also representing the endurance of the barrier for alternative pulses. The parameters are the same as in Figure III-45.

For pulses of alternating polarities (Figure III-27,Figure III-28, Figure III-46), the average charge does not depend much on Δt, thus giving a nearly constant breakdown probability due to average density of trapped charge P_c. On the other hand, the modulation is always large giving a large breakdown probability due to P_m.

We see, however, that in the alternative case, the calculated endurance is slightly lower for long Δt as compared with short Δt. This contrasts with what is experimentally observed for which the tendency is opposite [III.10]. This discrepancy may be explained by the heating of the MTJ when applying a voltage pulse [III.44]which is not taken into account in the model.

Indeed for short Δt, the injected power increases the MTJ temperature.
The temperature does not have time to decrease significantly between pulses. The steady-state increase in temperature is thus much higher for short Δt. This then results in a weaker endurance of the MTJ barrier for short Δt. In contrast, for long Δt, the temperature can cool off between pulses so that the average temperature is lower yielding an enhanced endurance.
This effect occurs for both unipolar and alternative pulses but does not impact the peak behaviour that we have modelled for unipolar pulses.

III.5.3.c Adjustment of the peak position:

As previously observed, in the unipolar case, a clear optimum in endurance is obtained by our model around 100 ns in agreement with the experimental data. In fact, the 100 ns position of the peak is mainly determined by the value of τ, the typical time that electrons take to escape from their traps.
Indeed, in our simulations, when we calculate the endurance versus Δt for different value of the escape time τ=*1ns, 10ns, 100ns and 1000ns* as shown in Figure III-47, we note that the peak position shifts when τ changes and the peak maximum appears exactly at the value of τ.

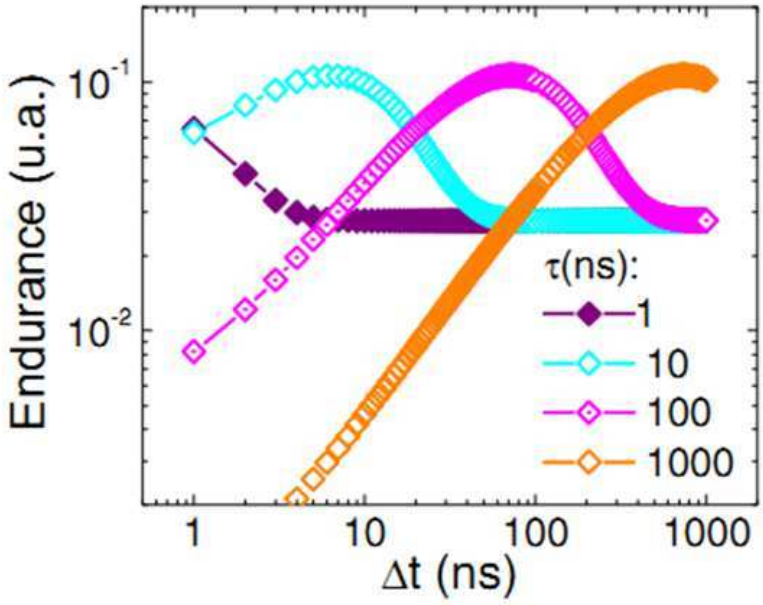

Figure III-47- Endurance versus Δt for different values of the time to escape *τ=1ns, 10ns, 100ns and 1000ns* in the unipolar case. Peak position depends on escape time *τ*. The parameters are the same as in Figure III-43.

III.5.3.d Pulses amplitude effect:

We have then performed similar simulations with different applied voltages in order to compare the model with experimental data.

The variation of different breakdown probabilities versus delay between pulses for different applied pulses amplitudes are shown in Figure III-48. The three breakdown probabilities due to trapped charge average, to charge modulation and direct breakdown strongly depend on voltage amplitudes.

As expected, for unipolar pulses, the endurance increases when the voltage is decreased (Figure III-49). However, the amplitude of this increase significantly depends on the delay *Δt*. In particular, the peak around 100 ns increases a lot with decreasing voltage (10 orders of magnitude in endurance by reducing the voltage from 2 to 1.5 V in the case of the measurement of Figure III-49 (a)). The endurance plateaus at long *Δt* also increase quite significantly (6 orders of magnitude from 2 to 1.5 V for the sample presented in Figure III-49). This is a consequence of a decrease in the amplitude of the time modulation in the density of trapped charges as the voltage is lowered. This is interesting since this low voltage/long *Δt* regime corresponds to the most common working conditions in MRAMs.

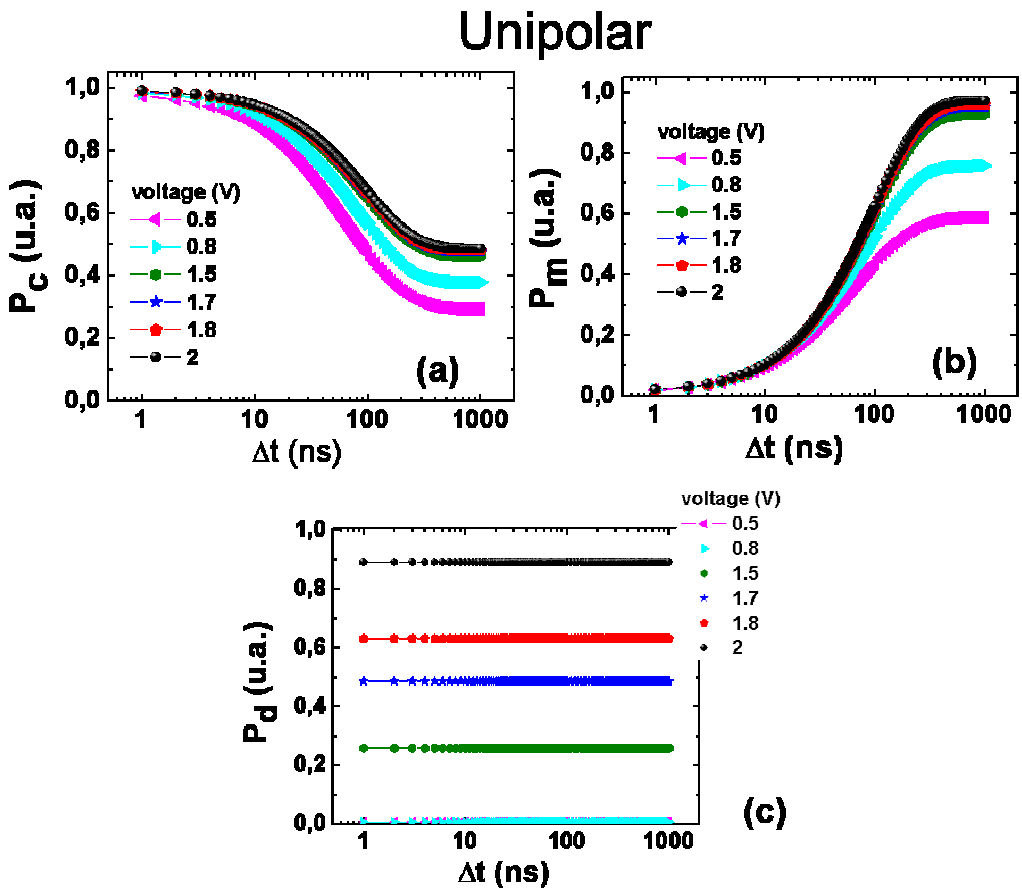

Figure III-48– Modelled breakdown probabilities as a function of Δt for different amplitudes of unipolar pulses with δ = 30 ns. For the model, the parameters used are A = 9 .78 × 10^{-18}, τ = 100 ns, Q_0 = 10 , V_c = 1 .5 V and ΔV = 0 .25 V. Calculated breakdown probabilities breakdown due to charge P_c (a), due to charge modulation P_m (b) and due to direct breakdown P_d (d) for unipolar pulses.

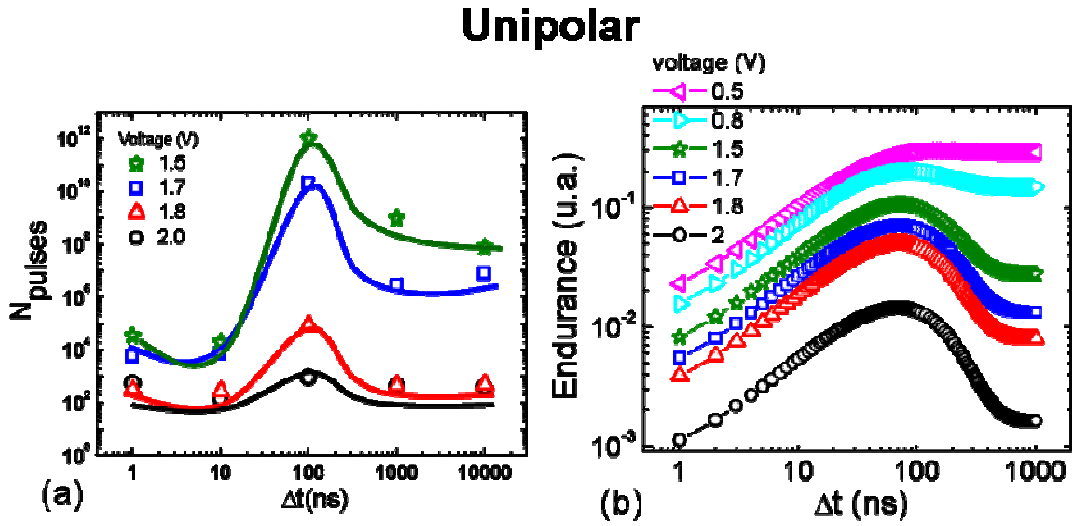

Figure III-49- Experimental (a), and modelled (b) endurances as a function of Δt for unipolar pulses with δ = 30 ns. For the model, the parameters used are A = 9 .78 × 10^{-18}, τ = 100 ns, Q_0 = 10 , V_c = 1 .5 V and ΔV = 0 .25 V.

In contrast, the increase in endurance is weaker for short Δt (2 orders of magnitude increase only from 2 to 1.5 V). Indeed in this later case, whatever the voltage, after a sufficient number of pulses, the density of trapped charge reaches a high level since the electrons do not have enough time to escape from their traps between pulses. Also the temperature rise may impact this low Δt regime as explained previously.

For alternative pulses (Figure III-50) the whole endurance increases uniformly over the whole Δt range when the voltage is reduced.

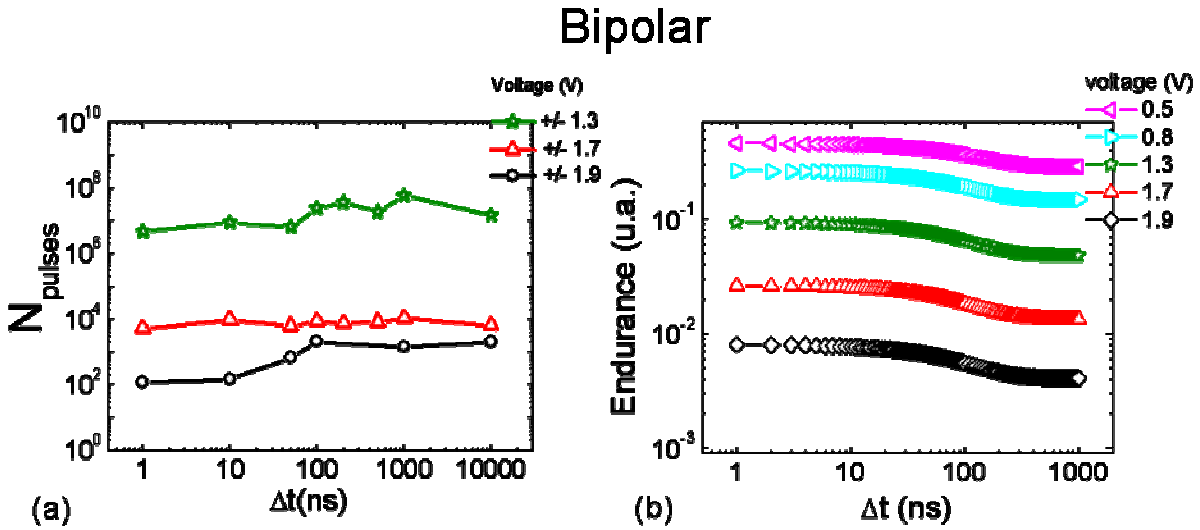

Figure III-50- Experimental (a), and modelled (b) endurances as a function of Δt for bipolar pulses with δ = 30 ns. For the model, the parameters used are A = 9 .78 × 10^{-18} , τ = 100 ns, Q_0 = 10 , V_c = 1 .5 V and ΔV = 0 .25 V.

The corresponding simulations are presented in Figure III-49 (b) for unipolar pulses and Figure III-50 (b) for alternative pulses. A good coherence is obtained between simulations and experiments for the set of adjusted parameters. Indeed, as explained previously, several parameters have been adjusted to fit the experimental data such as A, V_c, ΔV. The value of A has been determined so that when the voltage is increased the simulation for unipolar pulses of Figure III-49 (b) reproduces the general evolution experimentally observed in Figure III-49 (a), in particular the plateau increase for high Δt. The values used to calculate the direct breakdown probability P_d, i.e. V_c and ΔV, have been adjusted to fit the experimental variation of the peak amplitude around 100 ns versus voltage.

III.6 Conclusion

We have studied the barrier breakdown in MgO based MTJs under pulsed conditions that are closer to working conditions than the classical time dependent dielectric breakdown method carried out under static DC voltage stress. We have measured the effect of delay between pulses, of unipolar versus alternative pulses and of the voltage amplitude of these pulses.
Two regimes were observed as a function of delay between voltage pulses: (i) a regime at short delays (<100 ns) where the barrier contains a high density of trapped charges, (ii) a regime at long delays (>100 ns) where the time-modulation of the density of trapped charges is large. Both regimes are characterized by a reduced endurance. In between these two regimes, a dramatic increase in the endurance is observed for pulses of unipolar polarity. This peak behaviour disappears for alternative pulses.
We have interpreted these results in terms of charge trapping–detrapping of electrons in the defects of the barrier [III.10]. We have also discussed the influence of field-induced distortion of atomic bonds in MgO on breakdown.
We have developed a charge trapping–detrapping model [III.45] to explain the endurance in MgO-based MTJs. Our model allows estimating the endurance variations in the MTJs for different pulsed conditions. It reproduces fairly well the experimental trends. Under normal working conditions, i.e. relatively long delay between pulses and low voltage, the endurance is predicted to be high. However, if short delays between pulses or high voltages are needed for other applications, e.g. to increase the working frequency of the device, the low endurance may become problematic. It would then be necessary to decrease the number of defects within the barrier that act as trapping sites for electrons during tunnelling.
This study clearly demonstrates the key role played by electron trapping sites in the tunnel barrier. These traps can be dislocations, vacancies (O or Mg) or local variation of polarizability for instance if some BO has formed next to the MgO barrier.
If the density of these trapping sites can be reduced, then the endurance could reach the extremely high values that we observed in the optimum delay conditions over the whole delay range.

III.7 References

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Chapter IV. Characterization of electrical 1/f noise and correlation with write endurance

Content

IV.1 Introduction

In the precedent chapter, we have presented an experimental study of the barrier endurance in CoFeB/MgO/CoFeB based MTJ with RA product of the order of 5 Ω.µm² to 35 Ω.µm². These MTJs with thin oxide barrier and small junction area, exhibit sharp breakdown.
Our samples were tested under pulsed electrical stress. By studying the influence of delay between successive pulses, a dramatic increase by 8 to 10 orders of magnitude in the MTJ endurance was observed for an intermediate delay between pulses of the order of 80 to 100ns. This striking result has been interpreted by an electron trapping/detrapping mechanism in which the optimal delay of 80 to 100ns corresponds to the characteristic time for a trapped electron in the oxide tunnel barrier to escape from the trap.
A charge trapping-detrapping model was developed based on this physical picture which showed good coherence with experimental results. This study clearly demonstrated the key role played by electron trapping sites in the tunnel barrier. These traps can be pre-existing dislocations resulting from the lattice mismatch between CoFe and MgO (of the order of 4.3%), interstitial defects, vacancies (O or Mg) or local inhomogeneities in the oxide polarisability for instance if some BO has formed next to the MgO barrier during the annealing of the MTJ.
In oxides used in CMOS microelectronics, 1/f noise measurements are often used to characterize the presence of traps [IV.1], [IV.2]. Each trap generates a telegraph noise with its own duty cycle. The averaging over a large number of telegraph fluctuators having a random distribution of duty cycles yields a 1/f electrical noise. Since our earlier study demonstrated the key role played by electrical traps on the MTJ endurance, we decided to characterize the low frequency 1/f noise of electrical origin in these MTJs.
In this chapter, we show a correlation between the amplitude of 1/f noise of *unexercised* MTJs (*before* any electrical stress is applied) and the MTJ endurance (breakdown *after* applying a large number of electrical pulses). This confirms the expectation that a larger number of defects, inducing earlier breakdown, should correspond to a larger amount of fluctuators contributing to a larger 1/f noise amplitude.
The studied MTJs were developed for TA-MRAM and have the following composition: buffer/ PtMn 20 / CoFe 2 / Ru 0.8 / CoFeB 2 / Mg1.4/ CoFeB 2 / NiFe 1.5 / FeMn 9 / cap (thickness in nm). The MgO barrier was deposited in two steps: first a 1nm layer of Mg was subjected to natural oxidation, then a second layer of 0.4 nm was similarly deposited and oxidized. The measured devices were patterned into pillars of 200nm nominal diameter showing typically 130% TMR and RA product of about 35Ω.µm².

IV.2 Motivation for studying 1/f electrical noise

IV.2.1 Motivation:

The dielectric breakdown mechanism has always been an important question. There has been a growing interest to precisely characterize the process of oxide breakdown to have an accurate estimation for the reliability of ultrathin gate oxides of MOS transistors. When a voltage is applied across an ultrathin capacitor, the conduction through it can be categorized in two types. One is the direct tunneling of carriers through the oxide barrier and the other is the tunneling through the defects (traps) present in the oxide, which is called trap-assisted tunneling (TAT). As lots of studies have been conducted on the reliability of CMOS oxides, we will benefit from the know-how acquired in this field to study the MTJ reliability. With increasing stress, the density of traps increases and new conduction paths are formed inside the oxide, giving rise to breakdown events. In thinner oxides, the characterization becomes difficult because the breakdown events are often very soft and are not easily detected in the (commonly measured) average leakage current density. On the contrary, it was earlier reported that the ***low frequency 1/f*** noise can be very sensitive to the damage associated with the trap assisted processes [IV.3],[IV.4] and it was observed that the emergence of transient current spikes in TAT made the noise highly non-Gaussian. Our idea is to benefit from previous knowledge on low frequency noise to study the noise characteristics in MgO based Magnetic Tunnel Junction by applying a ramp of voltage.
Electrical noise in MTJs has different origins, either electronic thermal fluctuations responsible for *Johnson-Nyquist noise*, defects fluctuations responsible for *1/f noise* or statistical noise at nonzero current called *shot noise* [IV.5]. The Johnson noise and shot noise are both frequency-independent, and together they define the ultimate noise floor. 1/f noise is dominant in the low frequency range and is a performance-limiting factor for magnetic field sensors [IV.6], [IV.7].
At room temperature, two sources of noise dominate: Johnson-Nyquist noise and 1/f noise. Johnson noise is due to thermal fluctuations of electrons and it is related to the resistance *R* of the system by the Nyquist formula.
This noise has no magnetic origin and cannot be suppressed or modified but it is independent of the sensitivity of the sensor and depends only of its total resistance.
In addition to this white noise, a 1/f frequency-dependent noise is universally observed in all systems; it is due to uniform distribution of two-level fluctuators. In our MTJs, 1/f Noise is mostly related to defect fluctuations inside the barrier.
In addition to this electrical noise, MTJ can exhibit magnetic noise associated with magnetic excitations in the magnetic electrode translating into voltage fluctuations when a current flows through the device. This noise adds up to the purely electrical noise. However, the magnetic noise can be reduced by saturating the magnetization under large magnetic field thus allowing to concentrate on the purely electrical noise which is the focus of this chapter.

IV.2.2 Types of electrical noise sources

The current flowing in a device under DC conditions can be written as $I(t) = I_{DC} + i_n(t)$, where I_{DC} is the mean current due to the chosen bias point, while $i_n(t)$ is a random fluctuating current related to the noise. This latter current can be caused by external noise sources and by fundamental physical processes. External sources are for example cross-talk between adjacent

circuits, electrostatic and electromagnetic coupling from AC power lines, vibration etc. These disturbances can often be eliminated by shielding, filtering, and change of layout.
Fundamental physical sources cannot be eliminated, but it is however possible to reduce them by proper design of the devices and circuits. In this work we are interested only in these latter sources. A brief introduction on fundamental noise sources is reported below.

IV.2.2.a Thermal noise

Thermal noise, also called Nyquist or Johnson noise, appears in all resistors, resulting from a random thermally-activated motion of charge carriers in equilibrium with a thermal bath. The phenomenological description of its origins is based on the thermal activation of a large number of independent and random events. One event is related to a departure from the equilibrium state followed by a relaxation of the system to compensate the local perturbation of the charge distribution. The direct current has no influence on the thermal noise since the electron drift velocity is much less than the electron thermal velocity. Considering a piece of material with a resistance R at a temperature T, thermal noise can be represented by a current generator ($\overline{i^2}$) parallel to R or a voltage generator ($\overline{v^2}$) in series to R:

$$\overline{i^2} = 4k_B T \frac{1}{R}\Delta f \quad ; \quad \overline{v^2} = 4k_B TR\Delta f \qquad \text{(IV-1)}$$

where k_B is the Boltzmann constant and Δf is the bandwidth in Hertz.
Equation (IV-1) shows that thermal noise is proportional to the absolute temperature and it approaches zero when the temperature approaches zero. The power spectral density PSD of thermal noise is also independent of frequency. All noise sources which are independent of frequency are called *white noise* sources. This is because all different frequencies are present with the same weight.

IV.2.2.b Shot noise

Shot noise is a statistical noise associated to the direct current flowing across a potential barrier; it is a non-equilibrium form of noise. Shot noise is caused by the random barrier crossings by electrons and is related to the discrete nature of the electronic charge: electrons which are randomly emitted from the cathode and flow to the anode under the influence of the electric field generate a current which fluctuates around a mean level. The fluctuations are caused by the random and discrete nature of the electronic emission. The noise increases proportionally to the current flowing through the potential barrier. The mean square value of the current associated to the shot noise is:

$$\overline{i^2} = 2qI\Delta f \qquad \text{(IV-2)}$$

where q is the electronic charge. Shot noise is independent of frequency (white noise) and of temperature. It should be distinguished from the thermal fluctuations at equilibrium, which are present even when no voltage (or current) is applied to the device.

IV.2.2.c 1/f noise

The commonly called "1/*f* noise" refers to fluctuations of a physical variable with a PSD following a $1/f^{\alpha}$ law, where the exponent α is equal or close to 1.
This noise is also called "flicker" or "excess" noise: "excess" actually means in excess compared with the thermal noise level. Its first characterization goes back to Johnson's experiments on current fluctuations of the electronic emission in the thermionic tube (1925) [IV.9]. In addition to the shot noise, Johnson measured current noise whose spectral density increases with decreasing frequency *f*. The striking aspect of the 1/*f* noise which motivates a vast amount of research activity is its universal character. It is observed in a tremendous variety of systems, far beyond the borders of solid state physics.
Restricting the description of the 1/*f* noise to electrical noise measurements in condensed matter, we point out that 1/*f* fluctuations have been observed on the voltage probes in a vast number of different materials, like semiconductors, metallic and magnetic films, spin glasses, heterogeneous conductors, superconductors in the normal state, tunnel junctions, electronic devices, magnetic sensors ([IV.10]- [IV.18]) (based on AMR, CMR or TMR) and also in half metallic ferromagnets [IV.19].
In all materials and devices mentioned above, the 1/*f* fluctuations are related to resistance fluctuations $\delta R(t)$. These are measured by applying a current I and deducing the resistance fluctuations from the voltage fluctuations $\delta V(t) = I\,\delta R(t)$ at the terminal probes. The applied current does not create the fluctuations but just reveals them, above the white noise. This intrinsic nature of 1/*f* noise was clearly demonstrated in a major experiment performed by Voss and Clarke in 1976 [IV.20]: in zero current, fluctuations of the variance of the Johnson noise exhibit a 1/*f* power spectrum. This rules out any contribution of the driving current to the resistance fluctuations.
In the case of our MTJ, the fluctuators at the origin of the 1/f electrical noise can be predominantly the trapping sites in the barrier which can be charged or discharged. Depending on the traps electrical state, the electron tunneling probability locally varies thereby creating current fluctuations. Some recent results [IV.21],[IV.22] show a correlation between the low frequency noise characterizing the MgO based MTJs and the presence of defects and dislocations within the barrier. D. Herranz et al had presented a comparative study of low frequency noise [IV.21] in $Fe_{1-x}V_x$ / MgO / Fe and Fe / MgO / $Fe_{1-x}V_x$ magnetic tunnel junctions revealing that V doping of the bottom electrode reduces in nearly two orders of magnitude (see Figure IV-1) the normalized nonmagnetic and magnetic 1/f noise. As alloying Fe electrodes with V, through reduced FeV/MgO interface mismatch in epitaxial magnetic tunnel junctions with MgO barriers, the suppression of 1/f noise was attributed to strongly reduced misfit and dislocation density [IV.21]. Indeed, when used as the supporting bottom electrode, Fe–V alloys reduce the dislocations density and therefore the strain of the barrier and its roughness.
Furthermore, Kwang-Seok Kim et al [IV.22], had measured voltage fluctuations of the junctions with the constant voltage stress. It was found that low frequency 1/f noise power spectral density S_v follows 1/f noise characteristics. Figure 2 shows that the 1/f noise power spectrum changes with the stress time. The 1/f noise power increases with the stress time and the noise looses its 1/f character after breakdown.
Low frequency 1/f noise in studied MTJs is believed to come from fluctuations in the barrier associated with charge trapping/detrapping process in the barrier or near the interface. Its power spectral density increases with the density of defects in the barrier and interface quality between ferromagnet electrode and insulating layer. [IV.22]

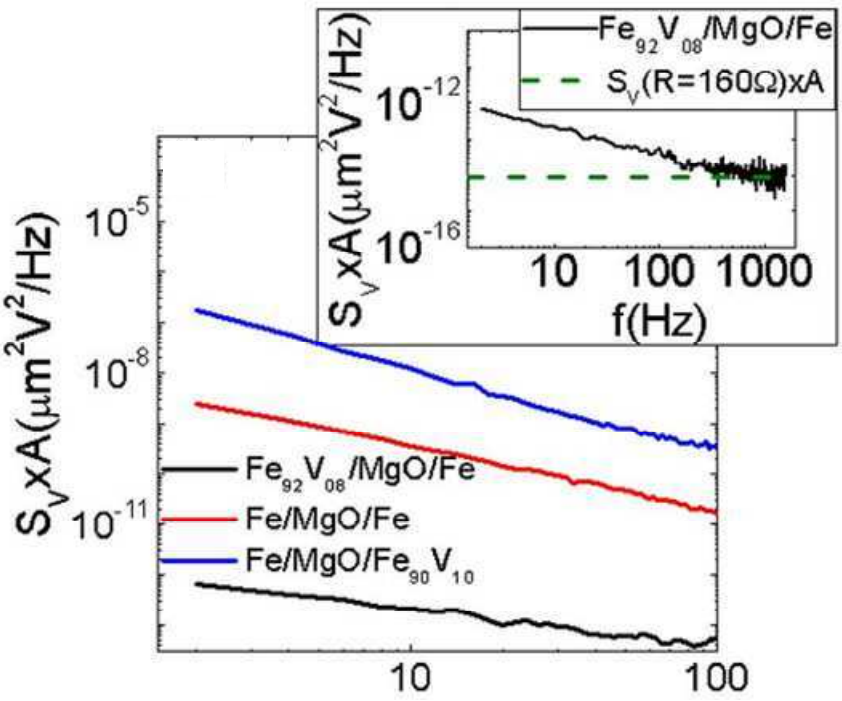

Figure IV-2 - [IV.21] Voltage noise power spectral density times area measured on the junctions with undoped, bottom doped or top doped elec-trodes with bias of 200 mV in the P state. The inset expands up to 2000 Hz the power spectral density for the junction with bottom doped electrode. The green horizontal line marks the noise power times area expected level of Fe92V08 / MgO / Fe with resistance of 160 Ω and direct electron tunneling processes.

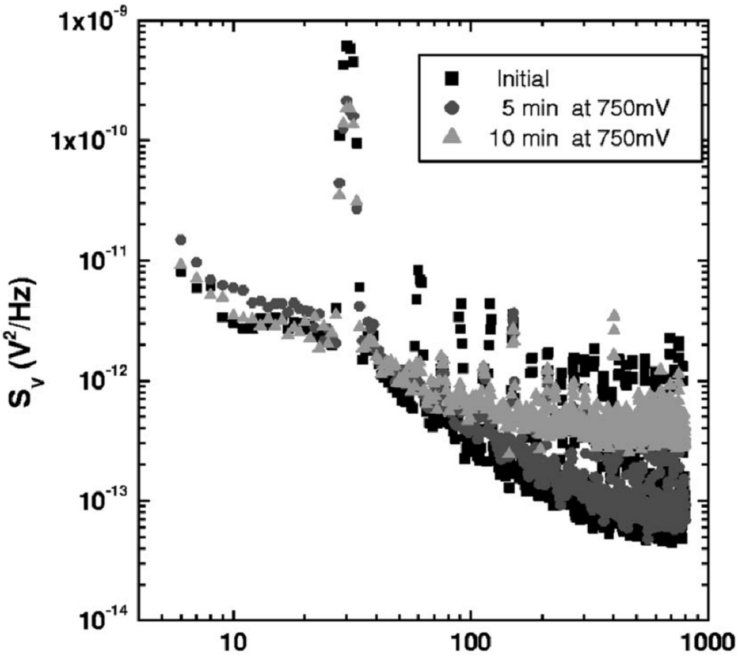

Figure IV-3- [IV.22] The variation of low frequency 1/f noise power spectral density S_v with constant voltage stress at 0.75 V for the denoted stress times.

A General Formula to Quantify the 1/*f* Noise

The 1/*f* resistance fluctuations are customarily quantified by a phenomenological equation given by Hooge in 1969 ([IV.23], [IV.24]) which can be expressed as follows:

$$S_V(f) = \alpha_H \frac{V^2}{N_C f^\gamma} \quad \text{(IV-3)}$$

Here, V is the applied voltage between the probes, N_c is the number of charge carriers in the noisy volume and α_H is a dimensionless constant for $\gamma = 1$, which is called Hooge's constant and refers to the noise level once the PSD is normalized by the volume and the applied voltage. Over the years, Hooge's constant was found to be equal to 2×10^{-3} in very different materials [IV.25], which was quite exciting in the search for a universal theory. Hooge's expression also implies that the noise level is independent of the temperature. However, since the eighties, strong experimental evidence has been found that Hooge's constant actually ranges from 10^{-6} to 10^{7} and is temperature dependent. The 2×10^{-3} value seems to be more a contact noise characteristic related to the sample geometry than a real estimate of fluctuations in bulk materials [IV.26]. Besides, the normalization by the number of charge carriers is strongly questionable because it would imply that each mobile carrier individually carries the noise. This property is inconsistent with the 1/*f* law: we cannot assume fluctuations due to individual charge carriers which last longer than the duration of the mobile charges within the sample[IV.27]. Despite the above arguments against a physical meaning of Hooge's equation, it remains a very convenient way to normalize the noise level between different systems and to provide an estimate of how noisy a device is at room temperature. The lowest α_H values have been obtained for bismuth and semiconductors with very clean surfaces. 10^{-3}-10^{-2} are the "standard" Hooge's constants for well crystallized metallic films and semiconductors. And the noise level is usually between 4 and 6 orders of magnitude higher in magnetic materials, oxides and nanocomposites. This noise is due to fluctuations of energy around equilibrium. It can be seen as a weighted sum of two-level fluctuators.

A general empirical Hooge formula [IV.28] describes its power density:

$$S_V(V^2/Hz) = \alpha \frac{R^2 I^2}{A f^\gamma} \quad \text{(IV-4)}$$

where α is the Hooge-like parameter, γ is the exponent of the 1/f noise, R and A are the junction resistance and area, respectively, and I is the bias current.

1/*f* Electrical Noise in Magnetic Materials:

As mentioned in the introduction of this chapter, noise in MTJ can have a magnetic origin in addition to a purely electrical origin. This magnetic noise comes from the magnetization fluctuations which are thermally activated and convert into electrical noise due to the TMR effect if a current flow through the MTJ. Since in this study, we wanted to focus on electrical noise, we performed the noise measurements on junctions exhibiting a large shift of the soft layer hysteresis loop so that during the noise measurement in zero field (well defined antiparallel configuration, see Figure IV-5, we could assume that the magnetic noise was much smaller than the noise of electrical origin.

The 1/f noise in Magnetic Tunnel Junctions is usually described using the empirical Hooge formula [IV.30] (Equation (IV-4)) where the Hooge-like parameter α is expressed in μm².
In the following, all our measurements are analyzed with this last formula (IV-4).

IV.3 Experimental procedure

IV.3.1 Experimental setup:

Noise measurements were performed with a SR780 spectrum analyzer at low frequency (0–102.4 kHz) on MTJs *before* applying any electrical pulse to test the MTJ endurance. The sample bias current was delivered by a battery and the sample signal was amplified by a low noise preamplifier (LI-75A). The experimental setup is shown schematically in (Figure IV-4 a,b). Noise measurements were performed at bias current I=30‧μA in the antiparallel state of the junction.

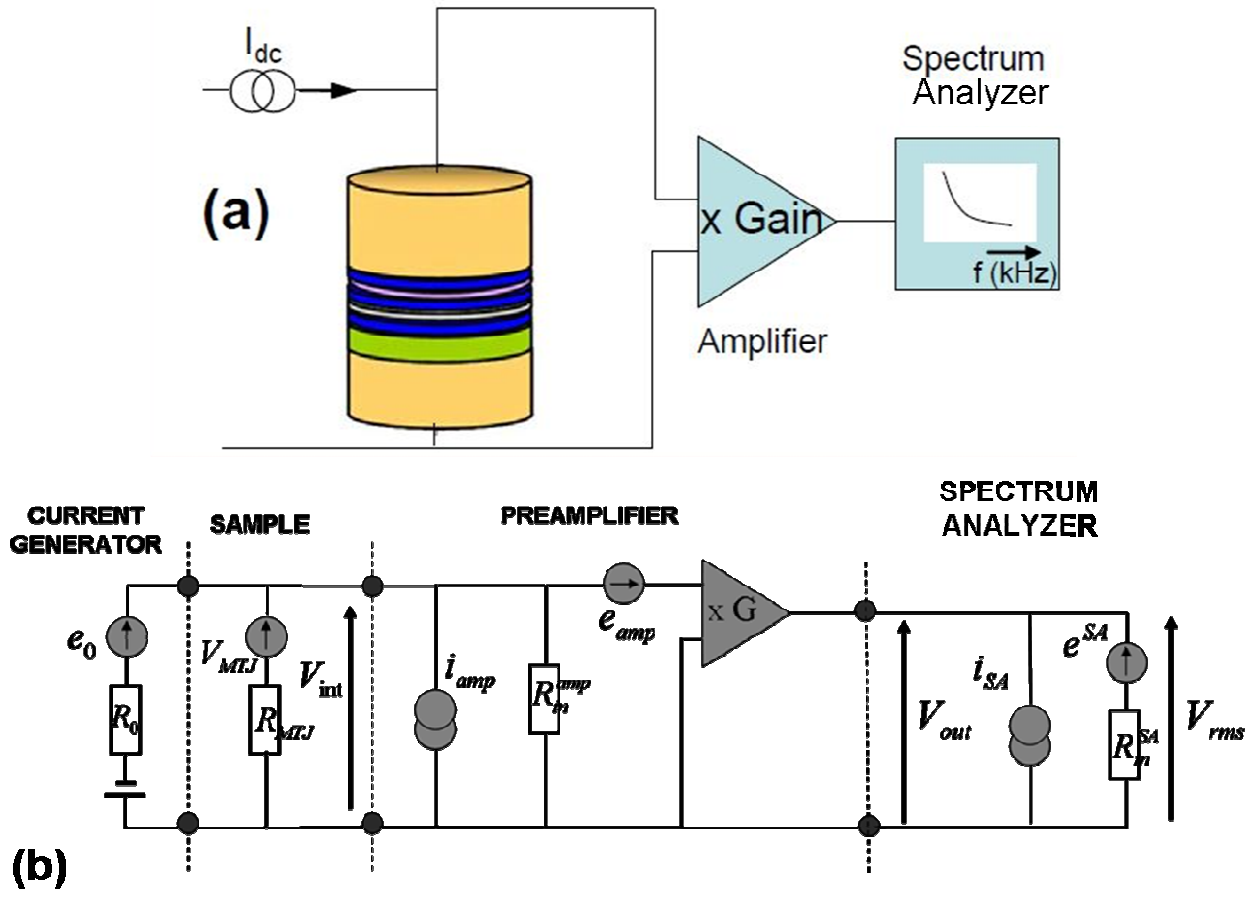

Figure IV-4 - (a) Schematics of the noise measurement setup. The sample is placed within a pair of rectangular coils fed by an external power source. (b)The sample is biased with a dc current source (battery-plus a variable resistor), and its ac-signal is amplified by a low noise preamplifier (LI-75A) and then measured with a real time spectrum analyzer (SR780).

IV.3.2 Adopted experimental procedure:

IV.3.2.a Suppression of magnetic noise:

As mentioned previously, to get rid of the magnetic noise, we performed the measurements on junctions exhibiting a large shift of the soft layer hysteresis loop so that during the noise measurement in zero field (see Figure IV-5) we could assume that the magnetic noise was much smaller than the noise of purely electrical origin. The experimental procedure consisted in repeating the noise measurement for a set of 50–60 junctions on the same wafer at room temperature. In order to ensure consistency in the reported noise and breakdown tests, only junctions with similar resistance (1200 Ω ± 5%) and similar magnetic properties were selected.

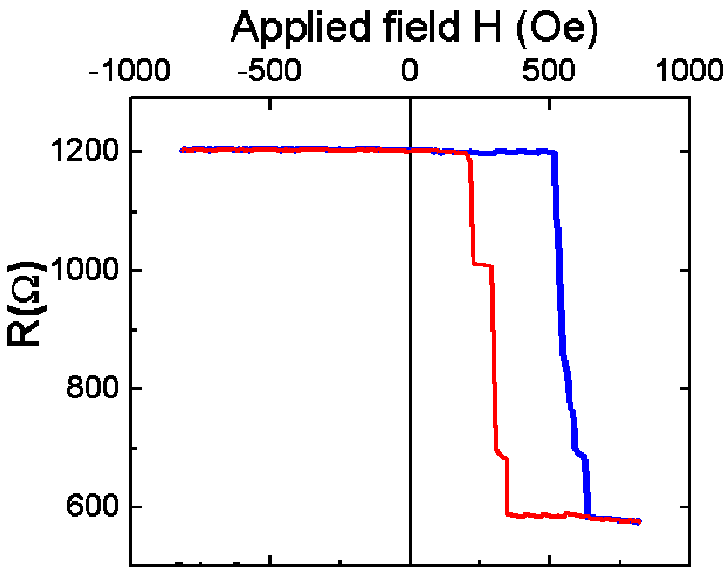

Figure IV-5 - Example of studied MTJ magnetoresistance loop. At zero magnetic field, the MTJ is in antiparallel state, far from magnetic reversal.

IV.3.2.b Set-up Noise and background distribution

The junction noise was corrected from the background distribution measured at zero bias current that contains the sample Johnson noise and the set-up noise.
The set-up noise is related to the noise of the Network analyzer and of the preamplifier. Figure IV-6 shows the different noise sources in the set-up. Both apparatus have their own noise (see Figure IV-6). All noises of different sources are presented as measured ie. amplified. The preamplifier multiplies the voltage value by ~ 100. V^2/Hz is then amplified by 10^4. The measured noise at zero current corresponds to background distribution plus the set-up noise.

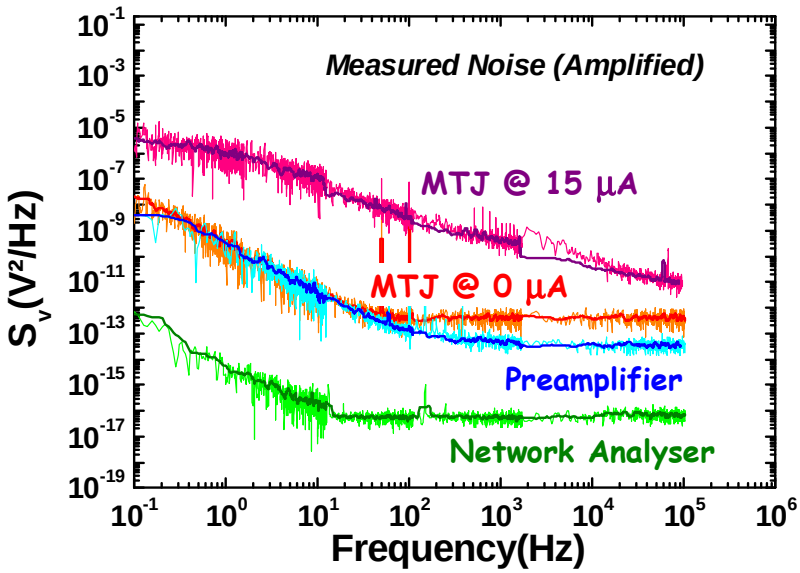

Figure IV-6 - Low-frequency (0–102.4 kHz) noise spectra for an MgO based MTJs of 200nm nominal diameter at antiparallel state either @ 15µA or @ 0 µA bias current. Measured Network analyser and Preamplifier noise spectra.

If we calculate the difference between the MTJ noise (measured at antiparallel state and 15µA bias current) and the background distribution , we get the corrected noise value.

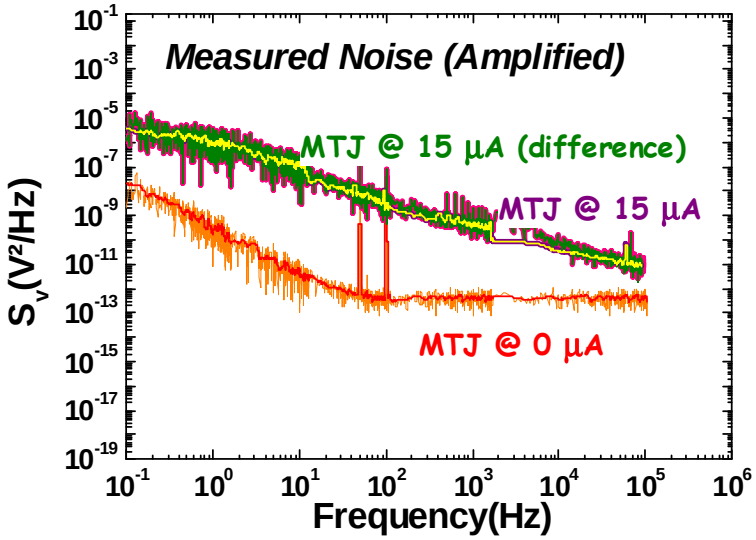

Figure IV-7 - Low-frequency (0–102.4 kHz) amplified noise spectrum of an MgO based MTJ of 200nm nominal diameter at antiparallel state corrected by substracting noise measured at zero bias.

We performed these different measurements to estimate the background distribution and subtract this value to get the net MTJ low frequency noise spectrum. We noted that the background distribution represents a negligible value compared to the MTJ noise, so we conclude that it is not necessary to subtract this correction each time. The junction noise shown in Figure IV-7 was corrected from the background distribution measured at zero bias current that contains the sample Johnson noise and the set-up noise. The measured noise spectrum is then devided by the amplifier gain(10^4) to obtain the proper noise value (see Figure IV-8).

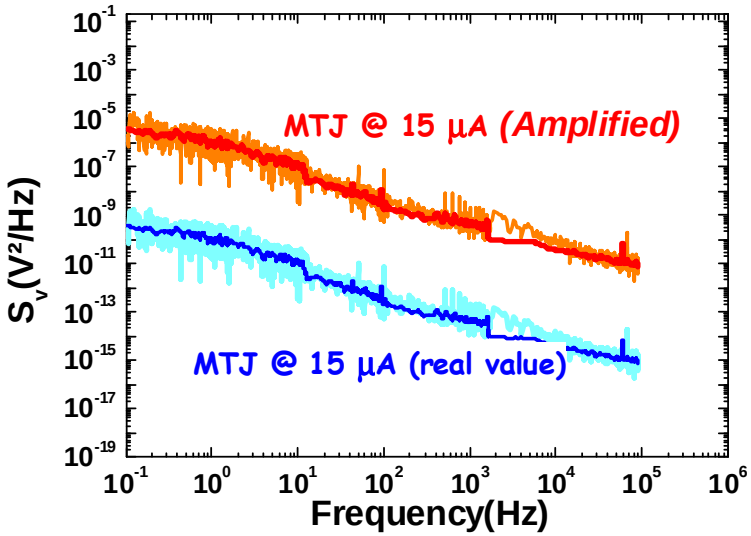

Figure IV-8 –Net low-frequency (0–102.4 kHz) noise spectrum of an MgO based MTJs of 200nm nominal diameter after eliminating the set-up noise and background distribution and corrected from amplification.

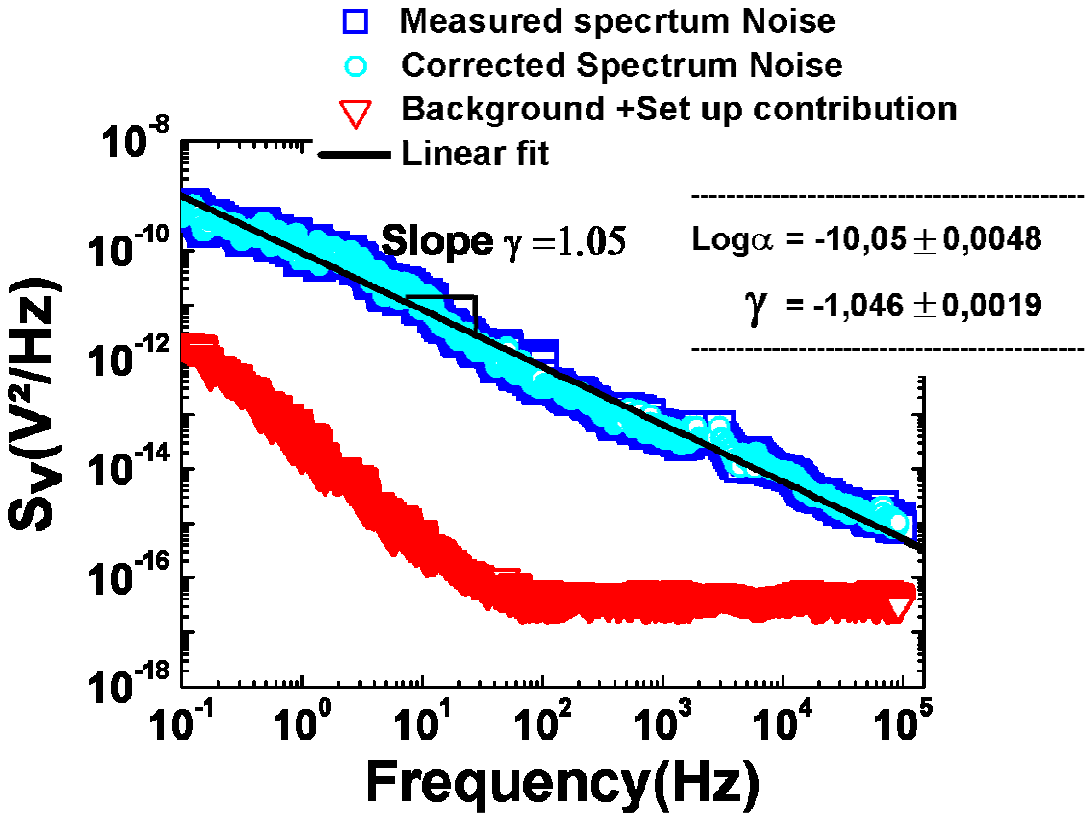

Figure IV-9 - Low-frequency (0.1Hz–102 kHz) noise spectrum of a MgO barrier MTJ with 200nm nominal diameter at 30µA dc bias current. The bottom curve corresponds to the noise measured at zero bias.

To summarize, we have controlled the background + set-up contribution and we corrected the measured noise by this value. As shown in Figure IV-9, the two noise spectra measured and corrected are superposed because the correction is negligible.

In all the rest, the noise spectrum are presented as measured and only corrected from the amplifier gain.

IV.3.2.c The bias current effect

Noise measurements from dc to 102 kHz and for biasing currents ranging from 0 µA to 30 µA are shown in Figure IV-10.
At the higher measured frequencies (102 kHz) and for zero bias current, the noise approaches the thermal background. The evolution of noise fluctuations with bias current is given in Figure IV-10. The measurements clearly indicate a 1 / f dominated regime that increases with current. This is due to the increased number of fluctuators excited by the current and thus taking part in the measured noise. The spectrum noise normalized by the square of the sense current exhibit comparable values (See inset of FigureIV-9). This noise is therefore a resistance noise.

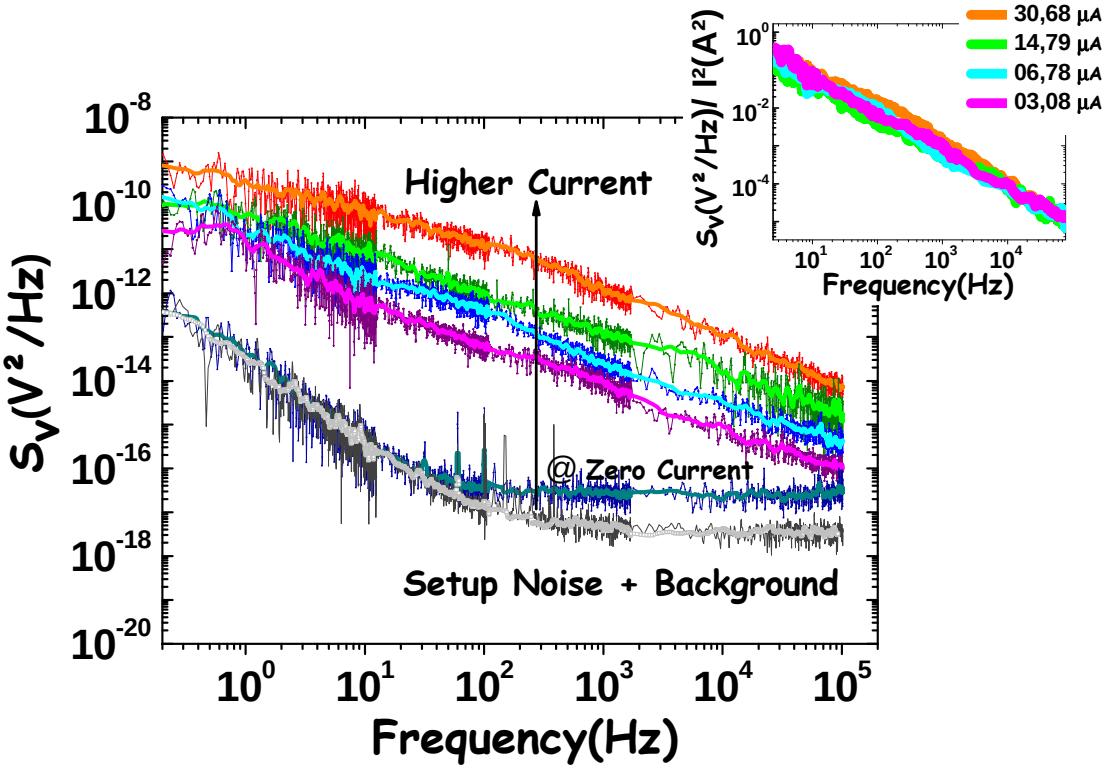

Figure IV-10 – Noise fluctuations at room temperature and at zero field expressed in V²/Hz as a function of frequency for bias currents ranging from 0 to 30µA. The higher the bias current, the more important is the 1/f noise.

IV.3.2.d Size Effect

In a rough approach, it is normally assumed that the noise level is inversely proportional to the volume of the sample between the probes [IV.7], [IV.31]. This dependence originates from the fact that if one assumes that the fluctuators are uniformely distributed in the volume

of the system, then the number of fluctuators N in the considered volume varies proportionally to the volume. As in a random walk, the amplitude fluctuations of the overall signal are then expected to vary as $N^{-1/2}$. The power of fluctuations is then expected to scale as 1/N i.e. as the inverse of the volume.
Noise measurements from dc to 102 kHz were performed on junctions of different sizes ranging from 1µm in diameter down to 0.2µm diameter (see Figure IV-11). The measurements were performed on MTJs from the same wafer i.e. having the same R.A. They were carried out for the same current of 30 µA.
The measurements clearly indicate a 1 / f dominated regime.
At the higher measured frequencies (102 kHz) and for zero bias current, the noise approaches the thermal background.
It is clear from Figure IV-11 that for junctions of reduced lateral sizes the noise behaves similarly but its level increases by 4 orders of magnitudes when the diameter was reduced by a factor 5. There are two contributions to this 10^4 increase in noise.
-A first contribution is the increased bias voltage used during the measurements. Indeed, by reducing the MTJ diameter by a factor 5, their resistance was increased by a factor 25. Since the measurements were performed with the same sense current of 30 µA, this means that the bias voltage was increased by a factor 25 so that its square was increased by a factor 625.The second contribution is the 1/volume dependence previously mentioned. A reduction by a factor 5 of the MTJ diameter means an increase by a factor 25 of the intrinsic noise level.
If we combine these two contributions, we expect an increase of the noise by a factor 625*25=15625~1.5 10^4 between the 1µm diameter and 0.2µm diameter MTJs. This is good agreement with the observation of Figure IV-11.

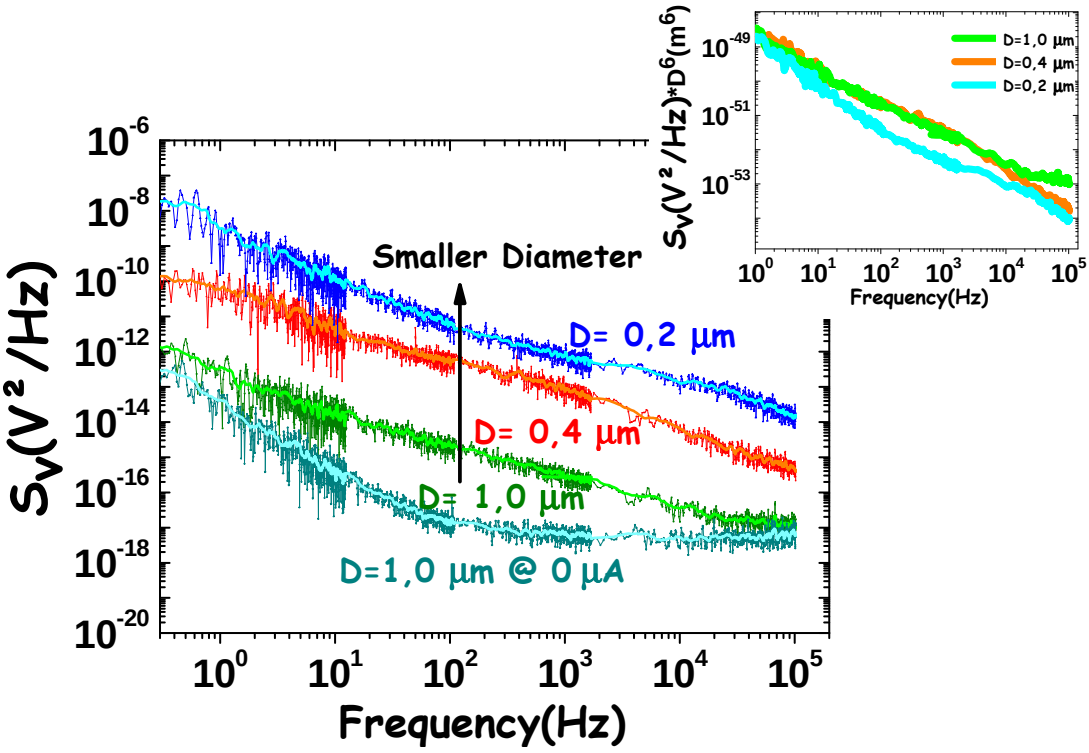

Figure IV-11 – Noise fluctuations expressed in V²/Hz as a function of frequency at room temperature at zero magnetic field different sizes. The bias current is 30 µA, except for the lower curve for which it is 0 A.

Expression (IV-4) $S_V(V^2/Hz) = \alpha \frac{R^2 I^2}{A f^\gamma}$ shows that at constant bias current and for different junction dimensions of the same wafer (RA=constant) the spectrum noise is proportional to R^2/A.ie, $S_v \propto (RA)^2/A^2*A$, as RA is constant so $S_v \propto 1/A^2*A \equiv S_v \propto 1/A^3$.
This means that we can expect that S_v be proportional to $1/D^6$ where D is the MTJ diameter. Therefore we have to plot $S_{v*} D^6$ to normalize the spectrum noise by MTJs diameters. The spectrum noise times D^6 shows a constant value (see inset of Figure IV-11). The small remaining differences between the various curves in the inset of Fig IV-10 can be ascribed to the unaccuracy in dimension of the patterned pillars.

IV.3.2.e MTJs Noise spectra:

We have tested a whole set of junctions which all belong to the same wafer. As shown in Figure IV-12, nominally identical junctions may have significantly different noise spectra. The noise amplitude strongly varies from junction to junction. This first result outlines that noise test could be a good tool to differentiate between them. Thus, we plot noise spectra of a certain set of MTJs and perform breakdown test and try to see if we can find a correlation between the two experiments. Our motivation to try finding a correlation between 1/f noise and endurance was based on the combination of two ideas: i) In microelectronics, the quality of CMOS oxides is often characterized by 1/f electrical noise measurements because these measurements are known to reflect the density of carrier trapping sites in the oxide. ii) Since our model of endurance was explaining the endurance in terms of trapping/detrapping of electrons, we could expect some correlation between 1/f noise and endurance. Furthermore, an earlier study [IV.21] has correlated the density of dislocations in the MgO barrier (which can act as electron trapping sites) with the 1/f electrical noise in MgO based MTJ with FeV electrodes. All these combined elements motivated us to carry out this investigation of possible correlation between 1/f noise and endurance.

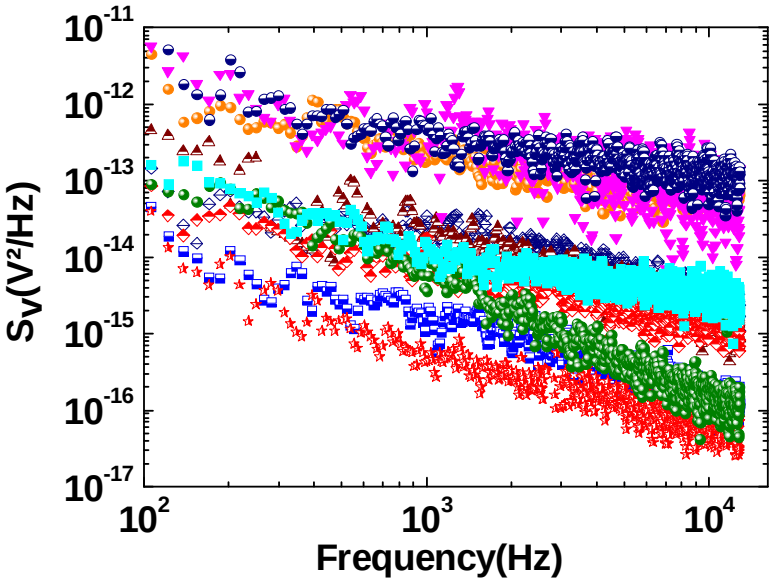

Figure IV-12 – Low-frequency (0.1 kHz –12.8 kHz) noise spectra for a set of 10 different MgO based MTJs of 200nm nominal diameter dimension. All of the tested junctions are from the same wafer and therefore have the same nominal characteristics (ie. same RA, same dimensions). They are tested under the same conditions (AP states and 30µA bias current).

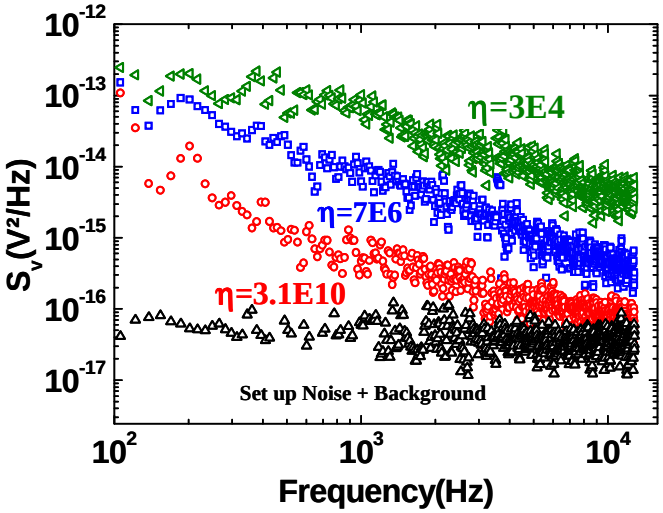

Figure IV-13 – Low-frequency (0.1 kHz –12.8 kHz) noise spectrum for a MgO barrier MTJ sensor with 10^{-2} nm² at 30µA dc bias currents. Notice the different low frequency Noise for different MTJs. The noise level is linked to the endurance (η) of the MTJ reported on the graph.

A first brief test of some jonctions shown in Figure IV-15 had encouraged us to further investigate in this direction since this test seemed to indicate that the expected correlation between 1/f noise amplitude and endurance (measured by η parameter in Weibull distribution) does exist . This investigation will be presented in details in section IV.4.2 but we now present the low frequency noise evolution of a MTJ while applying pulses till breakdown.

IV.3.3 Low frequency noise of MTJ during breakdown test

The experimental procedure of breakdown test, explained in more details in chapter III, consisted in applying successive pulses of 30 ns with constant amplitude (1.73 V) at zero magnetic field (corresponding to well-defined antiparallel alignment) until barrier breakdown occurs. As shown in previous chapter III, no gradual degradation of the barrier resistance was observed. The breakdown occurs abruptly as shown in Figure IV-14 and corresponds to a sharp drop of the junction resistance accompanied by a degradation of the TMR response.

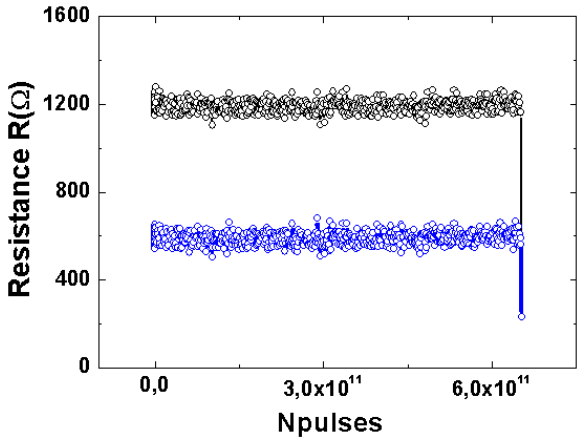

Figure IV-14 – Evolution of R_{min} and R_{max} vs number of pulses. An abrupt drop of R_{min} and R_{max} is observed after $6.53*10^{11}$ pulses when the breakdown occurred. The time interval and voltage used here were 70 ns and +1.73 V. RA=30 $\Omega.\mu m^2$.

We start by measuring the low-frequency noise spectrum for our junctions *before* applying pulses. After that we alternate between breakdown test and noise measurement. We repeat the low-frequency noise measurements *after each series* of applied pulses (see Figure IV-15).
We observe that the 1/f noise is stable as long as the MTJ is not broken. After breakdown, an abrupt change in noise spectrum is observed as shown in Figure IV-15.
The noise level versus the number of applied pulses is better represented in Figure IV-16. After breakdown, the sharp drop of the junction resistance and degradation of the TMR response is associated with a drop in junction noise level.

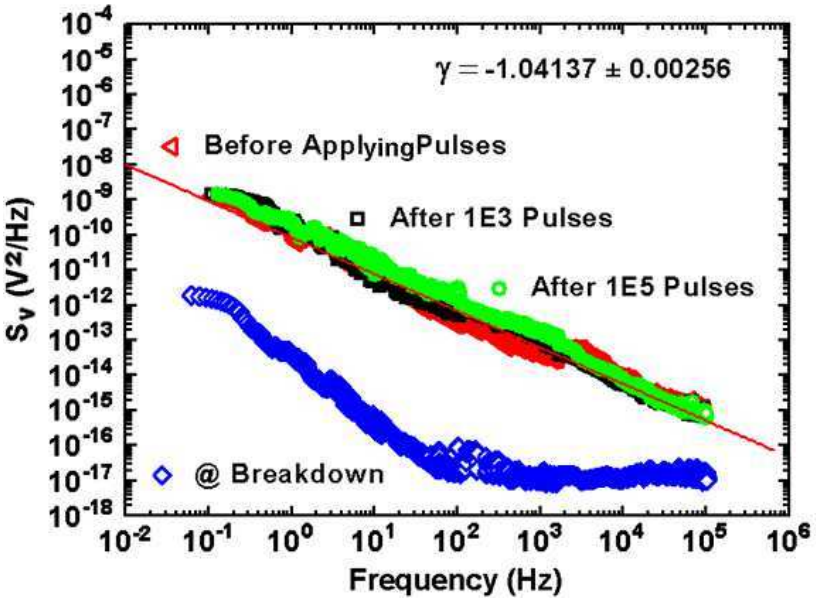

Figure IV-15. Noise spectrum plot after some series of applied pulses (The pulse duration, the time interval and the pulse amplitude used here were respectively: 30 ns, 70 ns and 1.6V). The upper plot is the noise after breakdown (degradation of the TMR response, Resistance drop down to R=184Ω).

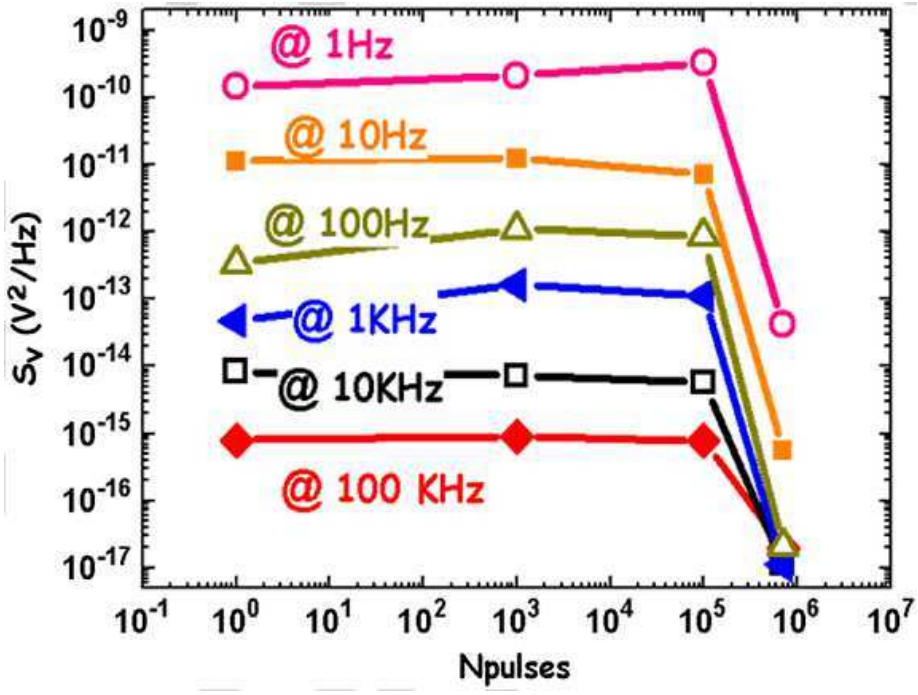

Figure IV-16- 1/f noise evolution during applying pulses to the junction until breakdown.

This observation is consistent with our previous study of Magnetic Tunnel Junction endurance presented in chapter 3.
We can confirm that there are no structural phenomena happening during applying this series of pulses. If pinholes or structural defects were created inside of the barrier, electric noise could increase. But in our case, electric Noise stays stable until breakdown occurs. Our interpretation is that there are pre-existing defects (dislocations, vacancies, traps at BO/MgO interfaces) that trap charges. The trapped charges induce mechanical stress in the barrier due to electrostatic forces favoring atomic mobility and pinhole formation until breakdown occurs.
To conclude, in chapter 3 we have developed a charge trapping-detrapping model to explain breakdown in MgO based MTJs. In this section, we have shown that the 1/f noise level does not vary during applying pulses. This result is consistent with an assumption of an abrupt junction degradation at breakdown.

IV.4 Correlation between Write Endurance and Electrical 1/f noise

In this section we will discuss the correlation between the noise level and the junction endurance of each MTJ. As shown in Figure IV-17, we can note that nominally identical junctions may have significantly different noise spectra: the noise amplitude varies by three orders of magnitude from junction to junction, but the γ parameter remains similar. The Hooge parameter α, representing the noise level, is systematically extracted from the data and varies between 10^{-10} µm² and 10^{-7} µm².
In a second step, we performed the breakdown test for these measured junctions under the same breakdown conditions ($\approx$1.73V, zero magnetic field, δ=30ns and Δt=70 ns).

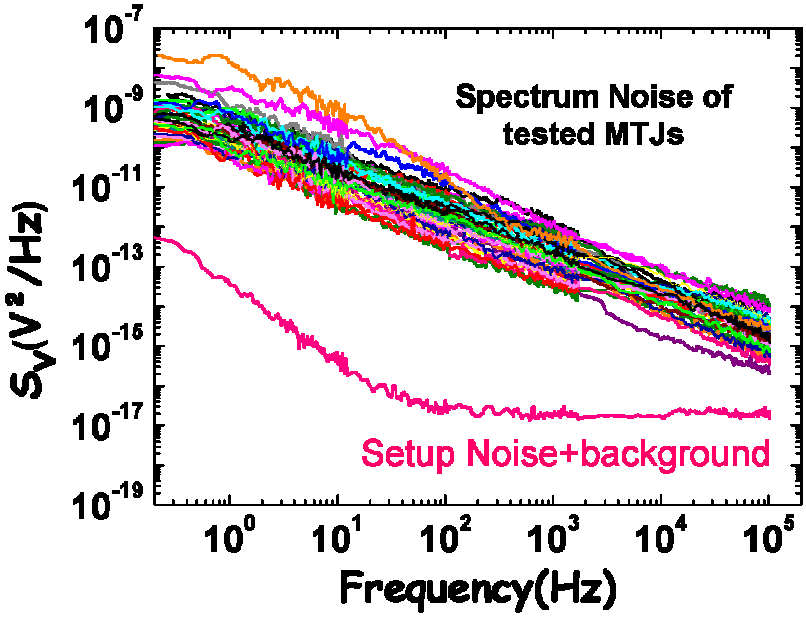

Figure IV-17- Low-frequency (0–102.4 kHz) noise spectra for a set of 60 different MgO based MTJs of 200nm nominal diameter dimension. All tested junctions are from the the same wafer and therefore have the same nominal characteristics (ie. same RA, same dimensions). They are tested under the same conditions (AP states and 30µA bias current).

Let us stress that the low-frequency noise measurements were performed before any pulse was applied to the MTJ. The breakdown tests were carried out afterwards. In Figure IV-18, the junctions endurance is plotted as a function of the corresponding Hooge parameter α.
We observe a rough correlation between MTJ endurance and 1/ f noise amplitude ie. Hooge parameter in MgO tunnel junctions: We notice that the junctions showing the largest 1/f noise power before starting the write endurance test have the lowest endurance. Reciprocally, the junctions exhibiting a low 1/f noise before being exercized tend to be those having the largest endurance. This observation suggests that endurance, and 1/f noise, are both sensitive to the amount of electron trapping sites present in the barrier[IV.7]. However, we note that the dispersion in lifetime between the 60 tested junctions (approximately 9 orders of magnitude) is much broader than the dispersion in Hooge parameter (4 orders of magnitude). This can be explained by the fact that the different defects present in each junction contribute differently to the noise and to the electrical breakdown. In fact, the voltage applied during endurance tests (≈1.73V) is much larger than the voltage applied for noise measurements (≈0.036V). Therefore a much larger number of trapping sites are charged during endurance tests by contrast to noise measurements. Supposing that a few defects play a dominant role in oxide breakdown and that their activation energy is large, they may not be detected by a noise experiment at low voltage. Indeed, from the noise perspective, each defect acts like a telegraphic fluctuator with a certain characteristic dwell time. The random distribution of these dwell times yields the observed 1/f noise. In contrast, from an endurance perspective, one of these fluctuators may dominate because atomic mobility may be more enhanced around this fluctuator than around others. Pinhole formation is likely to take place first at this dominant fluctuator location. Therefore all fluctuators contribute to the 1/f noise whereas a dominant fluctuator may be responsible for electrical breakdown. This difference may explain why the correlation shown in Figure IV-18 is only a rough one.

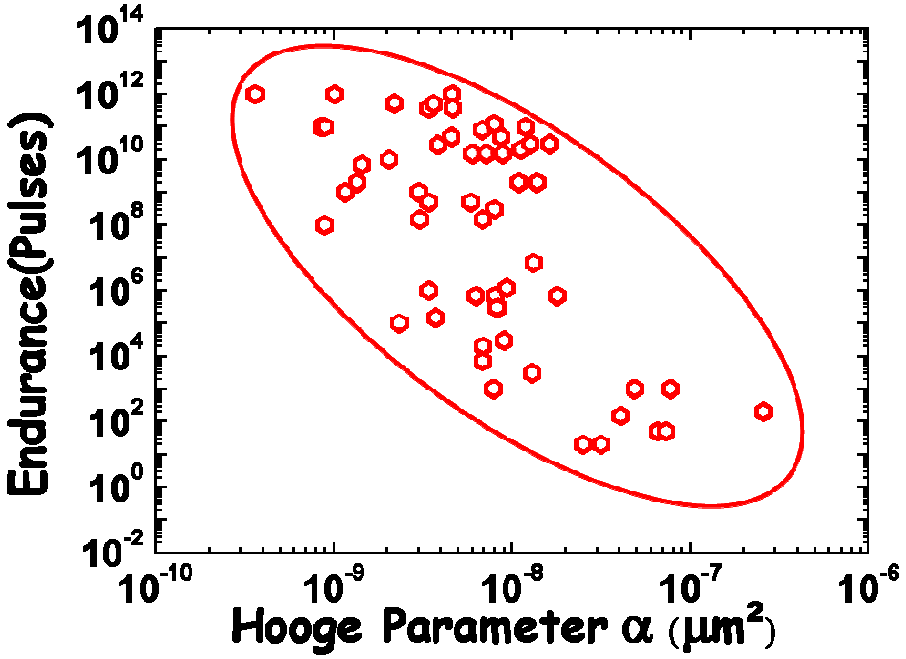

Figure IV-18- MTJs' endurance (defined as the number of voltage pulses of 1.73V after which the MTJ has experienced breakdown) versus Hooge Parameter α for the same set of 60 nominally identical junctions as used in Figure IV-17. The ellipse is a guide for the eye to underline the correlation between endurance and 1/f noise amplitude.

In our earlier study ([IV.34], [IV.35]) we clearly demonstrated the key role played by electron trapping sites in the tunnel barrier on the endurance of MTJs. These traps can be dislocations resulting from the crystallographic mismatch between CoFe and MgO (about 4.3%), or vacancies (O or Mg), or local changes in dielectric polarisability at BO/MgO interface if such interface forms during annealing of the MTJ.

The observed correlation between endurance and 1/f noise reported in the present study suggests that measurements of 1/f noise in unexercised MTJs could be used as a predictive approach to estimate the endurance of MTJs, unlike endurance tests which are destructive. At chip level, this could be a very interesting way to identify weak bits susceptible of early failure and discard these bits to reduce the need for redundancy.

One could think that this dependence of endurance on Hooge parameter is simply related to the resistance variation and is a simple correlation between Hooge parameter and the corresponding MTJ resistance.

About this point, let us notice that the range of resistances for the used samples is 1200 Ohm +-4%. Moreover the plot of the Hooge parameter versus resistance shows that no correlation is observed (see following Figure IV-19) contrary to endurance versus Hooge parameter. Thus the correlation between endurance and Hooge parameter cannot be ascribed to resistance variations between the studied MTJs.

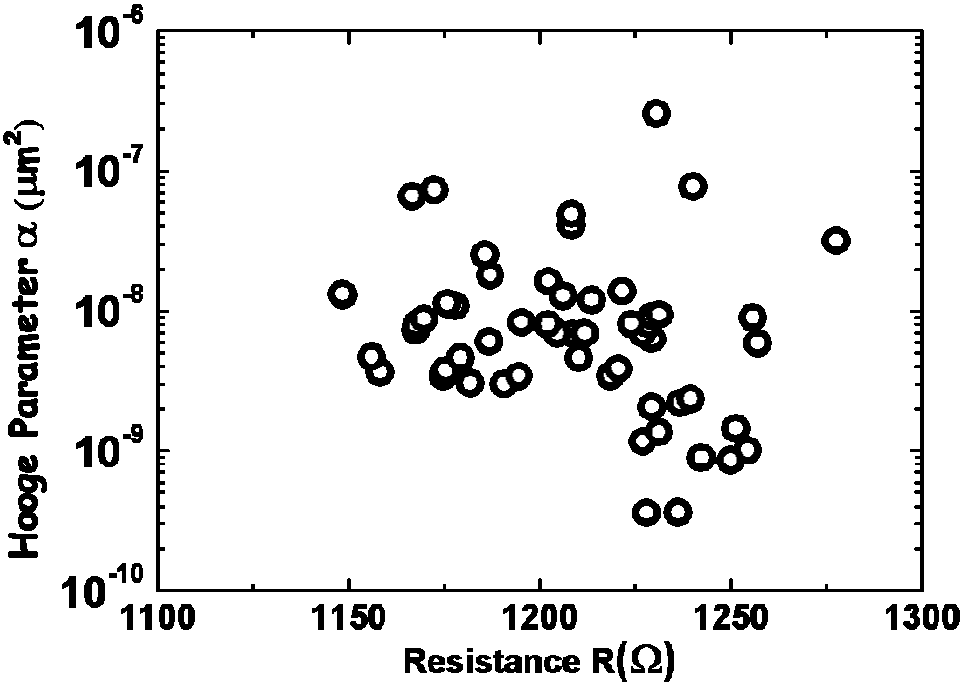

Figure IV-19- Hooge Parameter (α) variation versus correspondant resistance of the same tested jonctions plotted in Figure IV-17.

Besides, in our noise experiments, we have used a constant voltage battery. So for the small resistance variations (± 50Ohm), the current is in fact varying from one MTJ to the other, representing ± 1.5 µA. This current variation is very small and cannot account for the variations observed in Figure IV-18 as can also be seen in Figure IV-20. Indeed, we have measured the variation of α with current. A 3µA current variation gives a change of alpha of 10^{-14} µm^2, which is negligible and cannot account for the α variation of Figure IV-18.

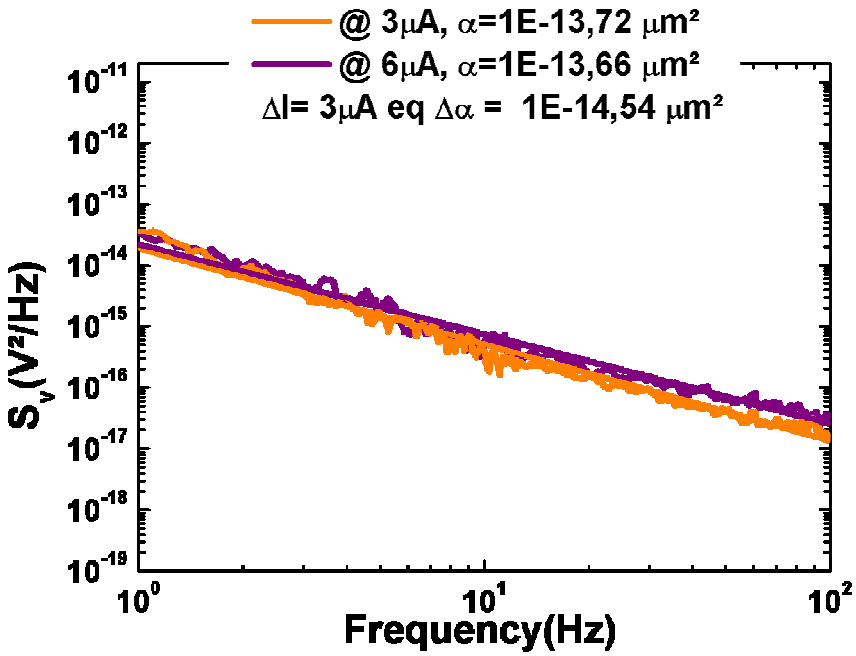

Figure IV-20. Two low frequency noise spectra of a MTJ under two bias currents of 3 μA and 6 μA to determine the Hooge parameter variation.

The main experimental finding of this noise study is this correlation between MTJ endurance and the 1/ f noise amplitude. Such result allows us considering the low frequency noise test of MTJs as a predective tool of MTJ quality and reliability.

To extend this study, it will be interesting to characterize the 1/f noise amplitude as well as the endurance in MTJs in which the number of electron trapping sites has been reduced. This requires optimization of the condition of deposition of the MgO barrier, minimization of the lattice mismatch between magnetic electrodes and MgO barrier, and good control of the B diffusion away from the MgO barrier during the MTJ initial annealing. In such junctions, extremely large endurance whatever the delay between voltage pulses associated with very low 1/f noise should be observed.

IV.5 Conclusion

Our study shows a correlation between endurance and 1/f noise level in magnetic tunnel junctions. This observation is explained by the fact that both phenomena are related to the presence of trapping sites in the barrier. As expected, the highest endurance is observed in low noise junction. This property could lead to a non-destructive test of junction endurance by choosing a maximum acceptable value for the Hooge parameter of the MTJs. However the observed data variability is more important for endurance than for noise. In order to perform a more sensitive noise test, it may be useful to measure the 1/f noise closer to the operating voltage of the tunnel junction. Finally this observation suggests that 1/f noise characterization could be used as a predictive tool for determining the barrier electrical reliability and therefore the write endurance of STT-RAM or TA-MRAM cells.

IV.6 References

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Conclusions and perspectives

This thesis aimed at studying the Magnetic Tunnel Junction reliability and cyclability to better understand the barrier breakdown mechanisms. The write endurance in MTJs has already been studied by several groups by time-to-dielectric-breakdown experiments. Different breakdown phenomena have been observed depending on oxide layer thickness, junction resistance area product (RA), and junction area. However, the mechanism and main cause of barrier breakdown in MTJ systems was not yet well understood, especially when the thickness of the oxide tunnel barrier gets in the range of 1nm-1.4nm. During my thesis, we focused on studying MgO based MTJ breakdown mechanism under pulsed conditions to better understand the phenomena of barrier breakdown in MTJs. We have chosen to work under pulsed conditions with shorter constant pulse-width of δ=30 ns which is close to working conditions in contrast to the classical time dependent dielectric breakdown method carried out under static DC voltage stress.

An investigation of barrier endurance till electrical breakdown in MgO-based magnetic tunnel junctions (MTJs) was presented. Samples were tested under pulsed electrical stress. By studying the effect of delay between successive pulses, an optimum endurance of MTJs was observed for an intermediate value of delay between pulses corresponding to an optimum trade-off between the average density of charge trapped in the barrier and the amplitude of its time-modulation at each voltage pulse.
We have measured the effect of delay between pulses, of unipolar versus alternative pulses and of the voltage amplitude of these pulses. Two regimes were observed as a function of delay between voltage pulses:

(i) a regime at short delays (<100 ns) where the barrier contains a high density of trapped charges,

(ii) a regime at long delays (>100 ns) where the time-modulation of the density of trapped charges is large. Both regimes are characterized by a reduced endurance. In between these two regimes, a dramatic increase in the endurance is observed for pulses of unipolar polarity. This peak behavior disappears for alternative pulses.

We have interpreted these results in terms of charge trapping–detrapping of electrons in the defects of the barrier. We have developed a charge trapping–detrapping model to explain the endurance in MgO-based MTJs. Our model allows estimating the endurance variations in the MTJs for different pulsed conditions. It reproduces fairly well the experimental trends. Under normal working conditions, i.e. relatively long delay between pulses and low voltage, the endurance is predicted to be high. However, if short delays between pulses or high voltage are needed for other applications, e.g. to increase the working frequency of the device, the low endurance may become problematic. It would then be necessary to decrease the number of defects within the barrier that act as trapping sites for electrons during tunneling.

The study emphasizes the role of electron trapping/detrapping mechanisms on the tunnel barrier reliability. It also shows that extremely long endurance could be obtained in MTJs by reducing the density of electron trapping sites in the tunnel barrier.
In oxides used in CMOS microelectronics, 1/f noise measurements are often used to characterize the presence of traps. Each trap generates a telegraph noise with its own duty

cycle. The averaging over a large number of telegraph fluctuators having a random distribution of duty cycles yields a 1/f electrical noise. Since our earlier study demonstrated the key role played by electrical traps on the MTJ endurance, we decided to characterize the low frequency 1/f noise of electrical origin in these MTJs.
Our study had shown a correlation between endurance and 1/f noise level in magnetic tunnel junctions. This observation was explained by the fact that both phenomena are related to the presence of trapping sites in the barrier. As expected, the highest endurance is observed in low noise junction. This property could lead to a non-destructive test of junction endurance by choosing a maximum acceptable value for the Hooge parameter of the MTJs. However the observed data variability is more important for endurance than for noise. In order to perform a more sensitive noise test, it would be useful to measure the 1/f noise closer to the operating voltage of the tunnel junction. Finally this observation suggests that 1/f noise characterization could be used as a predictive tool for determining the barrier electrical reliability and therefore the write endurance of STT-RAM or TA-MRAM cells.

This study clearly demonstrates the key role played by electron trapping sites in the tunnel barrier. These traps can be dislocations, vacancies (O or Mg) or local variation of polarizability for instance if some BO as formed next to the MgO barrier.
If the density of these trapping sites can be reduced, then the endurance could reach the extremely high values that we observed in the optimum delay conditions over the whole delay range.

Finally, the main perspectives of this thesis work concern the improvement of the MTJ structure to try reducing the amount of trapping sites in the barrier. This could allow dramatically increasing the endurance of MTJ. This implies reducing the mismatch between electrodes and barrier (for instance by V addition [IV.21]), optimizing the oxidation conditions during the barrier formation to avoid the formation of vacancies , control the B diffusion away from the barrier to avoid the formation of a BO/MgO interface. Additional measurements could be completed of three samples (CoFeB/MgO/CoFeB, CoFeB/Mg /MgO/Mg/CoFeB and CoFeB/CoFe /MgO /CoFe/CoFeB) without and with insert of a thin layer of Mg or CoFe between barrier and the two electrodes to see if it affects the reliability of these three samples. A comparative study of these MTJs endurance could be carried out using the same breakdown test under pulsed conditions we have used during this thesis. Results could be interpreted as the inserted layer could limit the B diffusion away from the barrier to avoid the formation of a BO/MgO interface. It would be of course useful to investigate the reliability in MTJs of smaller dimensions to evaluate the impact of edge defects due to the etching process on the reliability. The quantitative charge trapping/detrapping model adopted in chapter 3 could be extended by taking in account the self heating effect within the barrier for the shortest delays between pulses ie, by adding the breakdown probability P_T due to intrinsic thermal effect. An investigation of duty cycle effect on MTJ endurance could also be carried out by studying the delay between pulses effect for different pulse widths such as δ=0.1 ns, 1ns and 10ns. For low frequency noise test, it would be beneficial to repeat the same study but by applying larger voltage for noise measurements (> 0.036V applied in our presented test in chapter 4). Thus, we could improve the dispersion in Hooge parameter.

APPENDIX1

SCIENTIFIC COMMUNICATIONS

JOURNAL ARTICLES

1. Strelkov, N., A. Vedyaev, D. Gusakova, L.D. Buda-Prejbeanu, **S. Amara**, M. Chshiev and B. Dieny. *Finite element modelling of charge and spin currents in magnetoresistive pillars with current crowding effects.* IEEE Magnetics Letters **1** (2010) 3500204.

2. Strelkov, N., A. Vedyaev, N. Ryzhanova, D. Gusakova, L.D. Buda-Prejbeanu, M. Chshiev, **S. Amara**, N. de Mestier, C. Baraduc and B. Dieny, *Spin current vortices in current-perpendicular to-plane nanoconstricted spin valves.* Physical Review B **84** (2011) 024416.

3. S. Amara-Dababi, R.C. Sousa, M. Chshiev, H. Béa, J. Alvarez-Hérault, I.L. Prejbeanu, K. Mackay and B. Dieny , *Charge trapping-detrapping mechanism of barrier breakdown in MgO magnetic tunnel junctions***,** Applied Physics Letters **99** (2011) 083501.

4. S. Amara-Dababi, H.Béa, R.C.Sousa and B.Dieny, *Modelling of time-dependent dielectric barrier breakdown mechanisms in MgO-based magnetic tunnel junctions.* J. Phys. D: Appl. Phys. **45** 295002 (2012).

5. S. Amara-Dababi, H.Béa, R.C. Sousa, C.Baraduc and B.Dieny, *Correlation between write endurance and electrical 1/f noise in MgO based magnetic tunnel junctions for MRAM cells.* Applied Physics Letters L12-07710 (Accepted).

6. S. Amara-Dababi, H.Béa, R.C. Sousa, C.Baraduc and B.Dieny, *Barrier Breakdown mechanisms in MgO-based Magnetic Tunnel Junctions under pulsed conditions and correlation with low-frequency Noise.* Journal of Nanophotonics JNP 12076SSP (submitted).

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1. S. Amara, R. C. Sousa, H. Bea, C. Baraduc, and B. Dieny, *Barrier Breakdown Mechanisms in MgO-Based Magnetic Tunnel Junctions and Correlation with Low-Frequency Noise.* IEEE Trans. Magn. **48** (2012).

2. S. Amara-Dababi, H Bea, R.C.Sousa, C.Baraduc, K. Mackay, B.Dieny, *Barrier breakdown mechanisms in MgO-based magnetic tunnel junctions under pulsed conditions and correlation with low-frequency noise.* SPIE NanoScience+ ingineering.**8461-14** (2012).

3. S. Amara-Dababi, H.Béa, R.C.Sousa and B.Dieny. *Barrier Breakdown mechanisms in MgO-based Magnetic Tunnel Junctions under pulsed conditions.* Memory Workshop (IMW), 2012 4th IEEE International.**10**-1109 (2012).

PERSONAL COMMUNICATIONS

1. S.Amara, C. Baraduc, N. Strelkov, A. Vedyaev, L.D. Buda-Prejbeanu, M. Chshiev, Y. Liu, M. Li, K. Zhang and B. Dieny. *Modelling and measurement of transport properties in Current-Confined Path GMR structures.* 11th Joint MMM-Intermag Conference, Washington (USA), Jan. 18-22 2010 **(Oral).**

2. S. Amara, R.C. Sousa, J. Alvarez-Hérault, H. Béa, I.L. Prejbeanu, K. Mackay and B. Dieny. *Duty cycle effect on barrier breakdown in MgO magnetic tunnel junctions*, ImagineNano Conference, Bilbao (Spain), Apr. 11-14 2011 **(Poster).**

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7. S. Amara, R.C. Sousa, J. Alvarez-Hérault, H. Béa, I.L. Prejbeanu, K. Mackay and B.Dieny. *Etude du claquage de barrière MgO de jonctions tunnel magnétiques dû au piégeage/dépiégeage de charges dans la barrière*. Colloque Louis Néel, Brest (France), Sep. 20-23 2011 **(Poster).**

8. S. Amara-Dababi, H.Béa, R.C. Sousa, C.Baraduc and B.Dieny. *Barrier Breakdown mechanism in MgO-based Magnetic Tunnel Junctions and correlation with low-frequency Noise*, Intermag Conference, Vancouver (Canada), May. 7th-11th 2012 **(Oral).**

9. S. Amara-Dababi, H.Béa, R.C.Sousa and B.Dieny. *Barrier Breakdown mechanisms in MgO-based Magnetic Tunnel Junctions under pulsed conditions*. Memory Workshop (IMW), Milano (Italy), May 20th – 23rd, 2012 **(Oral).**

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11. S. Amara-Dababi, H Bea, R.C.Sousa, C.Baraduc, B.Dieny. *Giant Thermoelectric Effect in MgO Magnetic Tunnel Junctions asymmetrically heated by hot electron tunneling current.* 12th Joint MMM-Intermag Conference, Chicago (USA), Jan. 14-18 2012 **(Poster).**

French Introduction

Fiabilité et Cyclabilité des jonctions Tunnel magnétiques

Ce sujet de thèse s'inscrit dans le projet ERC obtenu par Bernard DIENY. Il se rattache directement au workpackage 1 de ce projet qui concerne l'amélioration des performances des matériaux spintroniques et en particulier la fiabilité et la cyclabilité des jonctions tunnels magnétiques. Les jonctions tunnels magnétiques constituent un élément de base des dispositifs d'électronique de spin. Ces jonctions sont constituées d'une barrière extrêmement fine (~1 à 2nm) de MgO ou d'Alumine insérée entre deux électrodes magnétiques. Elles sont au centre de différents dispositifs, comme les mémoires magnétiques MRAM et les oscillateurs à fréquence accordable. Dans ces dispositifs, on utilise l'action du courant polarisé en spin sur l'aimantation d'une des couches magnétiques pour changer la configuration magnétique des électrodes magnétiques, permettant soit de générer des mouvements de précession entretenue d'aimantation (oscillateur RF) ou sa commutation (cellule mémoire). Ces phénomènes se produisent typiquement à des densités de courant de l'ordre de $1\text{-}9\times10^{6}$A/cm² correspondant à des tensions à travers la barrière tunnel proches des limites de claquage électrique de cette dernière. Le claquage se produit typiquement lorsque le champ électrique dans l'oxyde devient de l'ordre de 10MV/cm (1V/nm). Les mécanismes de claquage et vieillissement des oxydes sont bien connus en électronique traditionnelle (CMOS, SiO2) mais pas du tout avec les oxydes et les épaisseurs utilisées dans ces jonctions tunnels. L'objectif de cette thèse est de caractériser et ensuite augmenter la fiabilité électrique des barrières tunnel utilisées dans des cellules MRAM et oscillateurs. Ces applications correspondent à des régimes de courant continu dans le cas des oscillateurs et impulsionel pour les cellules mémoire. Des cellules avec barrière tunnel MgO ont été évaluées pour déterminer leur tension de claquage et les paramètres des distributions de Weibull caractéristiques du temps de vie. L'étude a porté sur l'influence de temps de repos entre deux impulsions successives, l'influence de la durée, amplitude et polarité des impulsions appliquées, et aussi la température induite au sein de la barrière suite à l'application des impulsions. Les différents types de défauts seront identifiés et corrélés aux différents modes de préparation des jonctions tunnels (points chauds, inhomogénéité d'oxyde, diffusion interfaciale…). On a cherché également à comprendre le rôle des défauts intrinsèques (existants dans le matériau de départ) et ceux générés par le procédé de lithographie/gravure mis en oeuvre dans la nanostructuration de la jonction tunnel.

Le but sera ensuite de réduire ces défauts pour augmenter la résistance des jonctions au stress électrique et donc leur longévité dans les dispositifs spintroniques.
Une étude de l'effet de délais entre impulsions a été étudié. On a eu un nouveau résultat qui présente un pic de maximum de durée de vie correspondant à un délai entre pulses optimum de 100ns. On a expliqué un tel phénomène par le processus de charge et décharge des électrons piégés dans la barrière tunnel. Ça nous a donné une idée sur la possibilité de présence des défauts intrinsèques et extrinsèques au sein de la barrière qui représentent des pièges pour les électrons injectés dans la barrière.

Pour bien dominer le résultat et son explication, on a développé un modèle qui modélise l'effet de délais entre les pulses sur la durée de vie des jonctions tunnel magnétiques.
A ce stade, on a eu l'idée de mesurer le bruit télégraphique à faible fréquence et voir si ça peut être lié à la durée de vie des jonctions Tunnel magnétiques et si on peut prévoir par cette méthode si une telle jonction est « bonne ou mauvaise » sans passer par le test de claquage.
Les plaques étudiées viennent de la start up CROCUS ainsi que des plaques que je prépare à la salle blanche PTA à notre laboratoire SPINTEC.
Pour finir, après l'étude de tout ce phénomène de claquages des jonctions Tunnel magnétique on propose en perspectives de thèse d'optimiser la barrière en ajoutant du Vanadium à sa composition pour diminuer le mismatch et éliminer partiellement les défauts dans la barrière et par la suite avoir une durée de vie meilleure.

French Summary

L'endurance de barrière tunnel à base de MgO a été étudiée par la méthode d'étude du claquage du diélectrique dépendant du temps (CDDT) [1].On applique une série de pulses électriques successifs à durée constante de 30 ns, tout en variant l'amplitude et l'écart (Δt) entre deux pulses successifs. Cette série de pulses est bien appliquée jusqu'au claquage de la jonction Tunnel magnétique.

Les jonctions étudiées sont de la composition suivante : PtMn 20 / CoFe 2 / Ru 0.8 / CoFeB 2 / Mg 1.1 plasma ox/ CoFeB 2/ NiFe 3 (épaisseur en nm) présentant un produit RA= 30 Ω.µm² et une TMR=130%**.** On applique jusqu'à claquage des séries d'impulsions électriques de durée constante de 30 ns mais tout en variant à chaque fois l'écart Δt entre deux impulsions successives. On répète le même mode d'application d'impulsions pour différentes Δt de 1ns à 10 µs et pour différentes amplitudes V=1.0V à V=2.0V. Les données obtenues sont bien décrites par la distribution de Weibull [2] F(t) où η est le nombre des impulsions au bout duquel 63% des jonctions ont claqué et β le paramètre de forme (taux de panne) qui décrit le régime de claquage.

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\eta}\right)^{\beta}\right]$$

En premier lieu, on a suivi l'évolution des cycles de R(H) après chaque paquet d'impulsions appliqué. Cette étude de claquage dépendant de temps nous a montré qu'on a un régime de claquage plutôt brusque que graduel. On a tracé l'évolution de R_{min} et de R_{max} au cours d'application d'impulsion. On a observé un comportement de R_{min} et R_{max} stable au cours de temps sans aucune dégradation graduelle mais le claquage se fait brusquement par une chute de niveau de résistance. Comme notre étude d'endurance est sensée être statistique, ces mesures ont été faites à chaque fois pour une statistique de 30-40 jonctions claquées. Ce que nous a permis de tracer les distributions de Weibull pour chaque tension appliquée.

Par la suite, on a tracé la durée de vie η de 63% des jonctions Tunnel Magnétiques en fonction de l'amplitude des impulsions appliquées. On a extrapolé après les données expérimentales par le modèle en E [3] pour déduire la durée de vie des JTMs dans les conditions normales d'applications de 0.8V. Ça nous a donné une endurance supérieure à 10 ans, ça nous permet de dire qu'on dispose de JTMs de bonne fiabilité.

Dans une deuxième direction d'étude, on a décidé de voir l'effet de variation de délais entre les impulsions successives sur l'endurance des JTMs mais tout en gardant une durée d'impulsion constante. On a joué sur le paramètre Δt qui représente l'écart (le temps de pause) entre deux impulsions successives .On détermine à chaque amplitude la durée de vie de 63% des jonctions claquées pour Δt variant de 1ns à 10 µs. On a observé deux régimes d'endurance : Pour Δt de 1ns à 100ns, le paramètre η augmente alors que pour Δt =100ns à 10 µs la durée de vie des jonctions diminue. Ce pic aux alentours de 100ns a été observé que ce soit pour des impulsions positives ou négatives mais il disparaît si on applique une polarité alternative.
Pour interpréter ce résultat, on a associé ce comportement à un mécanisme de charge/décharge au niveau de la barrière MgO. Pour les impulsions assez serrées Δt<100ns,

on vient d'injecter des charges dans la barrière d'une manière continue.Les charges viennent se piéger dans des défauts, des pièges, des impuretés,des dislocations qui existent déjà dans la barrière,sans avoir le temps de se décharger. A force d'insérrer des charges dans la barrière ça augmante le niveau de charge dans la barrière et ça finit vite par faire claquer la jonction. Dans le deuxième régime des impulsions bien espacées $\Delta t>100ns$, on donne à la barrière le temps pour se décharger et faire sortir toutes les charges piégées, mais cette fois-ci on a appliqué un stress puissant sur la barrière à travers la modulation temporelle de charge assez importante soulignée par un passage sec d'un niveau haut de charge à un niveau bas. Ça se traduit par une diminution de temps de vie des jonctions Tunnel magnétiques. Cette interprétation est bien cohérente avec le résultat qu'on a eu pour les impulsions alternatives qui exercent elles aussi une modulation de charge en d'autres termes un stress sur la barrière. On n'oublie pas que les charges piégées dans la barrière MgO seront écrantées par des charges images positives dans l'électrode ce qui résulte une très forte interaction électrostatique qui fragilise la barrière de plus en plus jusqu'au claquage brusque.

Pour mieux comprendre le mécanisme de claquage liée à l'apparition de ce pic, nous avons développé un modèle en terme de piégeage / dépiégeage de charge basé sur des représentations qualitatives de la population des électrons piégés dans la barrière en cours du temps. A chaque impulsion, une partie des électrons tunnel se retrouvent piégés dans la barrière sur les sites de piégeage. Puis, entre deux impulsions, les électrons piégés peuvent échapper de leurs pièges avec un temps caractéristique τ_0 (~ 100 ns dans nos expériences).

Les trois régimes sont alors interprétés comme suit pour les impulsions unipolaires:

(1) Le premier régime observé correspond à $\Delta t << \tau_0$. À chaque impulsion, la barrière est de plus en plus chargée jusqu'à atteindre un régime asymptotique caractérisé par une forte densité d'électrons piégés. Le retard entre les impulsions ne permet pas à l'électron d'échapper. La barrière est par conséquent soumise à un grand stress qui la rend de plus en plus fragile. Par conséquent, sa durée de vie est réduite produisant la valeur basse de η observée à court Δt.

(2) Dans la limite opposée $\Delta t >> \tau_0$, une partie des électrons tunnel se retrouvent piégés à chaque impulsion, mais ils ont assez de temps pour échapper de leur pièges entre deux impulsions consécutives. En conséquence, la quantité de charges piégées dans la barrière reste faible en moyenne, mais présente une forte modulation en fonction du temps. Ceci génère une contrainte alternée sur la barrière d'oxyde qui conduit également à une courte durée de vie. Cette contrainte alternée favorise la mobilité atomique à travers la barrière, donc la formation d'un chemin de percolation qui peut causer le claquage.

(3) La situation intermédiaire de $\Delta t \sim \tau_0$ est la plus favorable en termes de durée de vie. La montée moyenne des électrons piégés dans la barrière est modérée ainsi que la modulation en fonction du temps de cette montée, ce qui entraîne une durée de vie importante. Puisque l'amplitude de la modulation de charge est proportionnelle à la tension appliquée, le pic d'environ 100 ns est donc prévu de diminuer en grandeur pour les grandes tensions, ce qui est effectivement observé. Cette vue d'ensemble est cohérente avec l'absence de pic lorsque on applique des impulsions de polarité alternée sont utilisés.

En effet, dans ce cas, les électrons sont piégés et dépiégés à chaque impulsion alternative quel que soit le retard Δt entre les impulsions. On obtient ainsi une forte modulation en fonction du

temps de la densité des électrons piégés conduisant donc à un comportement similaire à celui observé pour des impulsions de même polarité lorsque $\Delta t >> \tau_0$.
Pour l'intermédiaire Δt (100 ns), un compromis optimal régime est ainsi obtenue lorsque la barrière est ni soumis à une grande densité de charges piégées, ni à une forte modulation du temps de ces charges donnant ainsi lieu à une durée de vie optimale.

Cette interprétation semble expliquer la présence de ce pic prononcé d'endurance pour le cas d'application des impulsions unipolaires. Pour des tensions négatives, les électrons circulent dans le sens opposé et les mécanismes de charge / décharge des électrons piégés restent similaires. Si les pièges de la barrière sont uniformément répartis symétriquement ou dans l'épaisseur de la barrière, la variation d'endurance en fonction de délais entre les impulsions devrait donc rester la même pour les deux polarités. Ce ne serait plus le cas si les pièges se trouvent d'un seul côté de la barrière en raison de la méthode de préparation. Dans notre cas, la symétrie entre les impulsions positives et négatives indique soit une uniformité de répartition des pièges au sein de la barrière soit les pièges sont symétriquement répartis dans la barrière. Pour la polarité alternative, nous avons constaté que ce pic disparaît.
Cette vue d'ensemble explique également le cas des impulsions de polarités alternées, la modulation de charge est toujours grande, et l'optimum de l'endurance par rapport Δt n'est pas observée. Seule une faible endurance est obtenue, quel que soit le délai entre les impulsions. Dans la partie suivante de modélisation, nous développons plus en détail cette interprétation de piégeage-dépiégeage de charge pour mieux comprendre les mécanismes de dégradation dans JTM à base de MgO et aider à l'optimisation de la barrière et par conséquent sa fiabilité.
Dans le cadre de ce modèle, on définit trois probabilités de claquage en fonction de l'écart entre les impulsions. Aux faibles écarts Δt entre les impulsions $\Delta t << \tau_0$ ie. les impulsions assez serrées, on associe la probabilité de claquage due à la valeur moyenne de charge piégée au sein de la barrière Pc qu'on calcule et on trace la variation de cette probabilité Pc en fonction de Δt. Aux larges écarts entre les impulsions $\Delta t >> \tau_0$, on associe la probabilité de claquage due à la modulation de charge Pm au cours de temps. Pareil, on a calculé et tracé cette probabilité en fonction de Δt. Et la troisième probabilité de claquage est due au claquage direct qui a été également observé en SiO2. Ce claquage direct peut se produire indépendamment des défauts à l'intérieur de la barrière en fonction de la valeur de la tension appliquée ie le champ électrique induit. On a calculé cette probabilité et on a tracé sa dépendance en Δt. Par la suite, on a combiné ces trois probabilités pour déterminer et tracer la variation de la probabilité de claquage totale en fonction de Δt. On retrouve le pic d'endurance à $\Delta t \sim \tau_0$ (~ 100 ns dans nos expériences).

En dernière partie, on a étudié le bruit 1 / f de basses fréquences. En oxydes utilisés en microélectronique CMOS, les mesures de bruit 1 / f sont souvent utilisés pour caractériser la présence de pièges et de défauts dans l'oxyde. Chaque piège génère un bruit télégraphique avec son cycle propre. Le calcul de la moyenne sur un grand nombre de défauts et leurs attributions télégraphiques ayant une distribution aléatoire de cycles de fonctionnement produit un bruit 1 / f électrique. D'après notre étude précédente, on a montré le rôle clé joué par les pièges électriques sur l'endurance MTJ. C'est pourquoi nous avons décidé de caractériser les bruits 1/f basses fréquences d'origine électrique dans ces MTJ.
Dans ce chapitre, nous avons montré une corrélation entre l'amplitude du bruit 1 / f de MTJ non exercées (avant toute contrainte électrique appliquée) et l'endurance MTJ (claquage après application d'un grand nombre d'impulsions électriques). Cela confirme l'espoir qu'un plus

grand nombre de défauts, induisant plus tôt claquage, doit correspondre à une plus grande quantité de défauts contribuant à une plus grande amplitude de bruit 1 / f.

En conclusion, le phénomène de piégeage / dépiégeage de charges semble jouer un rôle très important dans le vieillissement et la dégradation des JTM à base de MgO. L'endurance maximale assez pertinente observée pour les temps de retard intermédiaire indique que la durée de vie des MTJ peut être augmentée indépendamment des délais entre les impulsions en réduisant la quantité de sites de piégeage. Ceci pourrait être réalisé en évitant la formation de l'oxyde de bore à l'interface de la barrière MgO, en évitant la présence de lacunes d'oxygène dans la barrière, et l'obtention d'un meilleur accord de maille entre les électrodes magnétiques et la barrière MgO pour éliminer les dislocations qui risquent de se former. Enfin, cette dernière observation de corrélation entre le bruit de faibles fréquences et l’endurance des JTMs propose que la caractérisation bruit 1 / f peut être utilisé comme un outil prédictif pour déterminer la fiabilité de la barrière électrique et donc l'endurance d'écriture des cellules STT-RAM ou TA-MRAM.

French Conclusion

Cette thèse vise à étudier la fiabilité des Junctions tunnel magnétiques et leur cyclabilité pour mieux comprendre les mécanismes de dégradation de la barrière. L'endurance d'écriture dans les JTM a déjà été étudiée par plusieurs groupes. Différents phénomènes de claquage ont été observés en fonction d'épaisseur de la couche d'oxyde, en fonction du produit résistance surface (RA) des JTMs et la surface de jonction. Cependant, le mécanisme et la cause principale de claquage de la barrière des JTMs n'était pas encore bien comprise, en particulier lorsque l'épaisseur de la barrière d'oxyde tunnel est de l'ordre de 1 nm-1.4nm. Au cours de ma thèse, nous nous sommes concentrés sur l'étude de mécanisme de claquage des JTMs avec la barrière MgO, en régime impulsionnel afin de mieux comprendre les phénomènes de rupture de barrière. Nous avons choisi de travailler dans des conditions pulsées avec une largeur d'impulsion de δ= 30ns qui est proche des conditions de fonctionalisation des JTMs, contrairement à la méthode classique réalisée sous contrainte de tension statique DC.
Une étude de l'endurance de la barrière à base de MgO dans les jonctions tunnel magnétiques (JTM) jusqu'au claquage électrique a été présentée. Les échantillons ont été testés sous contrainte électrique pulsé. Par l'étude de l'effet de retard entre des impulsions successives, une durée de vie optimale de MTJ a été observée pour une valeur intermédiaire de délai (repos) entre les impulsions correspondant à un compromis optimal entre la densité moyenne de charge piégée dans la barrière et l'amplitude de sa modulation au cours du temps à chaque impulsion de tension. Nous avons mesuré l'effet de retard entre les impulsions, l'effet des polaritées des impulsions unipolaire et bipolaire ainsi que l'amplitude de ces impulsions de tension. Deux régimes ont été observées en fonction du retard entre les impulsions de tension:

(i) à un régime de retards courts (<100 ns), la barrière contient une forte densité de charges piégées,

(ii) à un régime de longs retards (> 100 ns), où le temps de modulation de la densité de charges piégées est grand.

Les deux régimes se caractérisent par une endurance réduite. Entre ces deux régimes, une augmentation spectaculaire de la résistance est observée pour des impulsions de polarité unipolaire. Ce comportement de pointe disparaît pour des impulsions alternatives.

Nous avons interprété ces résultats en termes de piégeage-dépiégeage de charge (des électrons) dans les défauts de la barrière. Nous avons développé un modèle quantitatif de piégeage-dépiégeage de charge pour expliquer l'endurance des JTMs à base de MgO. Notre modèle permet d'estimer les variations d'endurance dans les JTM pour différentes conditions pulsées. Il reproduit assez bien les tendances expérimentales. Dans des conditions normales de travail, à savoir délai relativement long entre les impulsions et basse tension, l'endurance est prévu pour être élevé. Toutefois, si des courts délais entre impulsions ou haute tension sont nécessaires pour d'autres applications, par exemple à augmenter la fréquence de travail du dispositif, la faible endurance peut devenir problématique. Il serait alors nécessaire de réduire le nombre de défauts dans la barrière qui agissent comme sites de piégeage pour les électrons.
L'étude met l'accent sur le rôle des défauts présents au sein de la barrière dans le mécanisme piégeage / dépiégeage de charge et par par conséquent sur la fiabilité barrière tunnel. Elle montre aussi que l'endurance extrêmement longue pourrait être obtenue dans les JTMs en réduisant la densité des sites de piégeage d'électrons dans la barrière tunnel.

Dans un second temps, nous avons étudié le bruit basses fréquences dans les jonctions Tunnel Magnétiques.
En oxydes utilisés en microélectronique CMOS, les mesures de bruit 1 / f sont souvent utilisés pour caractériser la présence de pièges. Chaque piège génère un bruit télégraphique avec son cycle propre. Le calcul de la moyenne sur un grand nombre de fluctuators télégraphiques ayant une distribution aléatoire de cycles de fonctionnement produit un bruit 1/f électrique. Depuis notre étude antérieure on a montré le rôle clé joué par les pièges électriques sur l'endurance MTJ, nous avons décidé par la suite de caractériser le bruit 1 / f les basses fréquences d'origine électrique dans ces JTMs. Notre étude a montré une corrélation entre l'endurance et le niveau de bruit 1/f dans les jonctions tunnel magnétiques. Ce constat s'explique par le fait que les deux phénomènes sont liés à la présence de sites de piégeage dans la barrière. Comme prévu, la plus haute endurance est observée dans la jonction à faible bruit. Cependant, la variabilité des données observées est plus importante pour l'endurance que pour le bruit. Pour effectuer un test de bruit plus sensible, il serait utile de mesurer le bruit en 1/f proche de la tension de fonctionnement de la jonction tunnel. Enfin, cette observation suggère que la caractérisation bruit 1/f peut être utilisé comme un outil prédictif pour déterminer la fiabilité de la barrière et donc l'endurance d'écriture de STT-RAM ou TA-MRAM cellules.
Cette étude montre clairement le rôle clé joué par les sites de piégeage d'électrons dans la barrière tunnel. Ces pièges peuvent être dislocations, lacunes (O ou Mg) ou une variation locale de la polarisabilité par exemple si certains BO ainsi formé près de la barrière de MgO. Si la densité de ces sites de piégeage peut être réduite, alors la résistance peut atteindre des valeurs très élevées que l'on observe dans les conditions optimales de retard.
Enfin, les principales perspectives de ce travail de thèse sont concernent l'amélioration de la structure des JTMs : essayer de réduire la quantité de sites de piégeage dans la barrière. Cela pourrait permettre d’augmente considérablement l'endurance de MTJs. Cela implique la réduction de l'écart atomique entre les électrodes et la barrière (par exemple par addition du Vanadium), l'optimisation des conditions d'oxydation au cours de la formation de la barrière pour éviter la formation de lacunes, de contrôler la diffusion du Bore de la barrière pour éviter la formation d’oxyde de Bore à linterface avec le MgO. Il serait bien sûr utile aussi d'étudier la fiabilité des JTMs de plus petites dimensions pour évaluer l'impact des défauts de bord en raison du processus de gravure sur la fiabilité.

ABSTRACT

The thesis objective is to study the Magnetic Tunnel Junction reliability and cyclability to more understand the barrier breakdown mechanisms. An investigation of barrier endurance till electrical breakdown in MgO-based magnetic tunnel junctions (MTJs) is presented. Samples were tested under pulsed electrical stress. By studying the effect of delay between successive pulses, an optimum endurance of MTJs is observed for an intermediate value of delay between pulses corresponding to an optimum trade-off between the average density of charge trapped in the barrier and the amplitude of its time-modulation at each voltage pulse. Furthermore, a charge trapping/detrapping model was developed which support this interpretation. The study emphasizes the role of electron trapping/detrapping mechanisms on the tunnel barrier reliability. It also shows that extremely long endurance could be obtained in MTJs by reducing the density of electron trapping sites in the tunnel barrier. Then the write endurance and the 1/f noise of electrical origin were characterized in CoFeB/MgO/CoFeB MTJ for STT-MRAM or TA-MRAM. A correlation was observed and explained by the presence of electron trapping sites in the MgO barrier and the role of electron trapping/detrapping phenomena in both the MTJ reliability and its 1/f electrical noise power. These results suggest that 1/f noise could be used as a predictive characterization of the MTJ endurance. Finally, as thesis perspectives, some complement measurements were proposed to further investigate this model and an optimization of MgO barrier which could be carried out to reduce the density of these trapping sites was presented to ameliorate the MTJs reliability.

Keywords: **Time Dependent Dielectric Breakdown; Magnetic Tunnel Jonctions; Endurance; Charge Trapping-Detrapping; low frequency noise.**

RESUME

L'objectif de cette thèse est d'étudier la fiabilité et la cyclabilité des jonctions Tunnel magnétique pour mieux comprendre les mécanismes de dégradation et de claquage de la barrière. Une étude de l'endurance de la barrière MgO jusqu'au claquage électrique est présentée. Les échantillons ont été testés sous un mode impulsionnel. Par l'étude de l'effet de retard entre des impulsions successives, une durée de vie optimale des JTM est observée pour une valeur intermédiaire de retard entre les impulsions correspondant à un compromis optimal entre la densité moyenne de charge piégée dans la barrière et la modulation temporelle de charge. En outre, un modèle de piégeage / dépiégeage de charge a été développé qui appuie cette interprétation. L'étude souligne le rôle des pièges de charges dans le mécanisme de claquage de la barrière tunnel. Elle montre aussi que l'endurance extrêmement longue pourrait être obtenue en réduisant la densité des sites de piégeage d'électrons dans la barrière tunnel.
Puis, une étude de l'endurance et du bruit basse fréquence a été établie dans les jonctions CoFeB/MgO/CoFeB pour STT-MRAM ou TA-MRAM. Une corrélation a été observée et expliquée par la présence de sites de piégeage d'électrons dans la barrière de MgO et le rôle des phénomènes de charge/ décharge à la fois dans la fiabilité et la puissance du bruit électrique en 1 / f. Ces résultats prouvent que le test du bruit basse fréquence peut être utilisé comme une caractérisation prédictive de l'endurance.
Enfin, en perspectives, des mesures complémentaires ont été proposées pour développer plus le modèle de charge/décharge, une optimisation de la barrière pourrait ainsi être réalisée pour réduire le nombre des pièges de charge au sein de la barrière et par conséquent améliorer la fiabilité des jonctions Tunnel.

Mots-clés: **Claquage du diélectrique dépendant du temps; Jonction Tunnel Magnétique; Endurance ; Piégeage-Dépiégeage de charge ; Bruit basse fréquence.**