CMOS Integration of field effect plasmonic modulators

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Intégration en technologie CMOS d'un modulateur plasmonique à effet de champ

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Abstract

Compact and low energy consumption integrated optical modulator is urgently required for encoding information into optical signals. To that respect, the use of plasmon modes to modulate light is of particular interest when compared to the numerous references describing silicon based optical modulators. Indeed, the high field confinement properties of those modes and the increased sensitivity to small refractive index changes of the dielectric close to the metal can help decrease the characteristic length scales of the devices, towards to that of microelectronics. This thesis investigates the realization of Si field-effect plasmonic modulator integrated with a silicon-on insulator waveguide (SOI-WG) using the standard CMOS technology.

The material aspects and also the technological steps required in order to realize an integrated plasmonic modulator compatible with requirements of CMOS technology were investigated. First, we demonstrate a Metal-Nitride-Oxide-Semiconductor (MNOS) stack for applications in electro-optical plasmonic devices, so that a very low optical losses and reliable operation is achieved. This objective is met thanks to a careful choice of materials : (i) copper as a metal for supporting the plasmonic mode and (ii) stoechiometric silicon nitride as an ultrathin low optical loss diffusion barrier to the copper. Final electrical reliability is above 95% for a 3 nm thick Si_3N_4 layer, leakage current density below 10^{-8} A.cm^{-2} and optical losses as low as 0.4 dB.μm^{-1} for a 13 nm thick insulator barrier, in agreement with the losses of the fundamental plasmonic mode estimated by 3D FDTD calculations, using the optical constant of Cu measured from ellipsometry. After demonstrating the MNOS as an appropriate structure for electro-optical CMOS plasmonics, we fabricate a vertical Metal-Insulator-Si-Metal (MISM) waveguide integrated with an SOI-WG, where the back metal was fabricated by flipping and molecular bonding of the original SOI wafer on a Si carrier wafer. The active device area varies from 0.5 to 3 μm^2, 0.5 μm width and length varying from 1 to 6 μm.

An efficient and simple way to couple light from Si-WG to vertical MISM PWG was experimentally realized by inserting a Metal-Insulator-Si-Insulator (MISI) coupling section between the two waveguides. We demonstrate that such couplers operates at 1.55 μm with the highest efficiency geometry corresponds to a compact length of 0.5 μm with coupling loss of just 2.5 dB (50 %) per facets. This value is 3 times smaller compared to the case of direct coupling (without any MISI section).

High-k dielectrics are demonstrated as promising solution to reduce both the MISM absorption loss and the operation voltage. Given that interest, we experimental demonstrate an electrical reliable high-k stack for future applications to the MOS plasmonic modulators.

A few μm long plasmonic modulator is experimentally investigated. Devices show leakage current below 10 fA through the copper electrodes based MOS capacitance. The accumulation capacitance (few fF) was found to scale with the surface of the device, in consistent with the expected equivalent oxide thickness of the MOS stack of our modulator. A low electro-absorption (EA) modulation showing capacitive behaviour was experimentally demonstrated in agreement with simulations. Finally, low energy consumption devices 6 fJ per bit was demonstrated.

Table des matières

Table des figures

Liste des tableaux

Chapitre 1

Introduction

Silicon (Si) technology is considered as the ideal platform to merge photonics with electronics owning to its promise of low cost, high yield and device integration. In this platform the realization of photonic-electronics circuits is strongly dependent of the availability of Si based optical modulator that enable the interaction of electrical and optical signal. In this chapter we will give a general introduction about the state of the art of Si technology and Si photonics. Then we will focus on optical modulators and in particular plasmonic modulators based on MOS technology. Finally the outline of this manuscript is presented.

1.1 Silicon Technology

It is globally accepted that the Silicon technology is the driving force of the continuous technological progress. The tremendous success of this technology is attributed to the fact that by scaling the length of the metal oxide semiconductor (MOS) transistor we can achieve improvement of performance and reduction of the price per transistor. This success was predicted by the famous Moores law [1] which defines that it is possible to pack more and more transistors in the same area as a consequence of scaling down the size of each transistor. At the same time better performance can be achieved (Fig. 1.1). Since 1960, it is seen as a trend that for every three years the Si industry has been

producing new generation technology by scaling down the feature size to 0.7 times its initial dimension. This thus results in a MOS transistor with smaller, faster and more energy efficient characteristics [14].

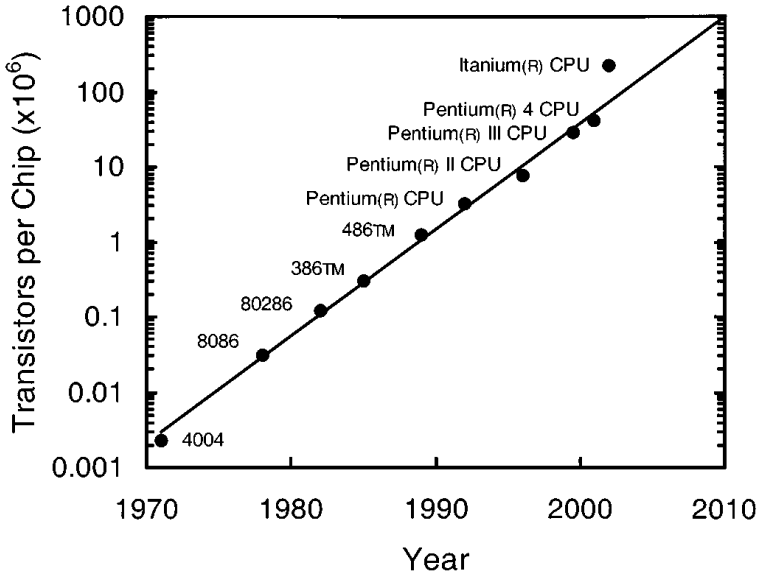

FIGURE 1.1 – *Transistor per chip for Intel central processing unit (CPU)*

Fig. 1.2 shows the evolution of the transistor, starting from the first Metal Oxide Semiconductor Field Effect Transistor (MOSFET) with a length of 100 μm, to the present technology of the 22 nm length tri-gate transistor, originally invented by Intel. Finally, it is seen that more transistors can be packaged in a given area. For mass production this can be translated into huge economies of scale.

The imminent drawback of scaling is often referred to as the "Interconnect bottleneck". As the dimensions of MOS a transistor are scaled down, more interconnecting lines are required in order to connect each transistor, resulting in less space between the interconnects. This increases the capacitance between the interconnect lines. Additionally, information transfer through interconnects results in an increase of heat dissipation due to resistivity. These trends are responsible for the increased interconnect Resistive-Capacitive (RC) delay leading to lower operation bandwidth of the device. The solution to the problem of high resistivity is addressed through the use of copper as compared

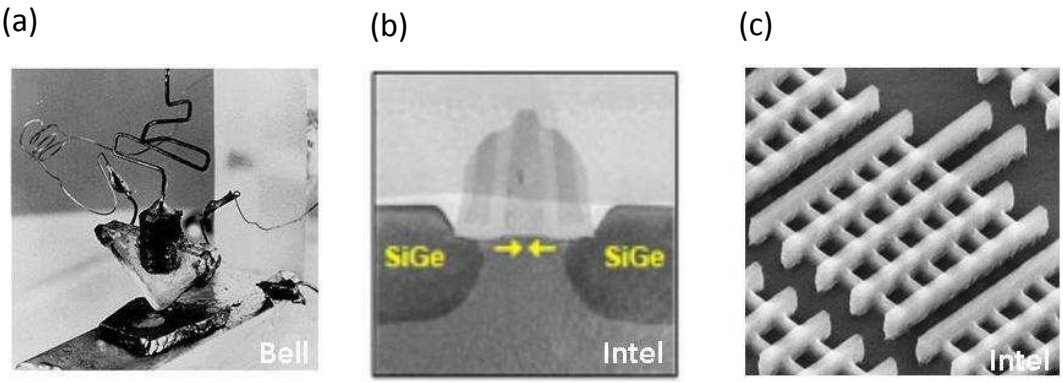

FIGURE 1.2 – *The history of the transistor : (a) First experimental demonstration of a transistor ; (b) MOSFET with gate length of 35 nm ; (c) Tri-gate transistor with 22 nm gate length*

to conventional used aluminium interconnects due to the fact that the former has a low resistivity than the latter by a factor of two. The issue of increased capacitance is solved through the use of a low dielectric constant material (low "k").

Choosing copper as the new material of the electrical interconnects creates several issues to the manufacturing process. In the inexistence etching method of copper, new techniques for deposition are implemented namely "Damascene" technique. This technique is based on chemical-mechanical-planarization (CMP) [15]. Furthermore, Copper is a fast diffusion material in the Silicon and insulators and creates short circuits in the transistors. Hence, several diffusion barriers for copper are proposed [16]. The deposition and patterning of copper is therefore well mastered in a CMOS environment, and thanks to that, scaling is allowed to continue.

Using copper with very low k insulators as an interconnect structure may extend the continued use of electrical intereconnects for a while (Fig. 1.3). As Moore said "No exponential is forever : but "Forever" can be delayed" [17]. However, as the speed of the travelling information becomes higher and higher, these solutions will be inappropriate because they will create too much heat. To that respect new long term solutions are needed to overcome these phenomena.

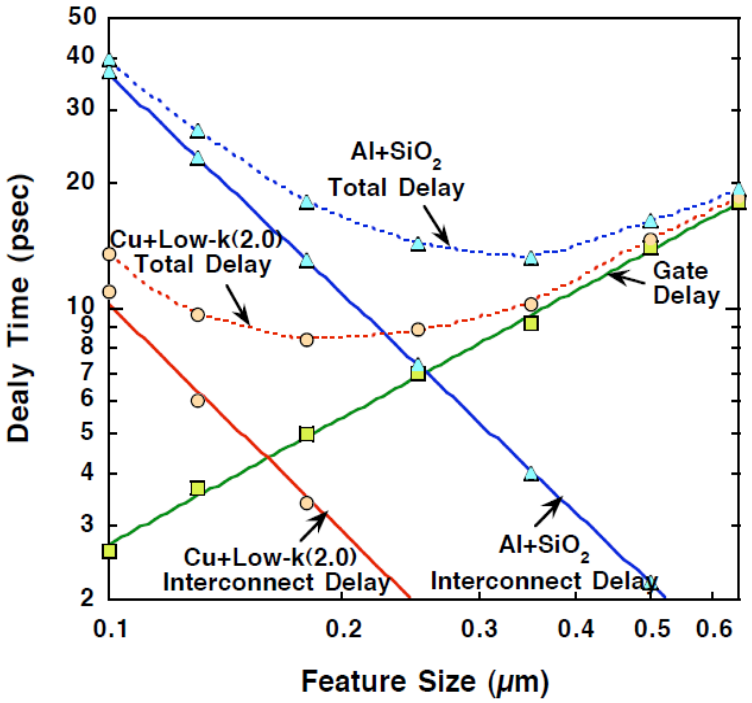

FIGURE 1.3 – *Delay time for using different interconnects technology for different technology nodes [1]*

Optical interconnects suggested as the most promising innovative path for replacing the electronic data bus thereby solving the issue of "interconnect bottleneck". In this prototype interconnect scheme, the information transmitted from one point to another uses photons rather than electrons and copper wires, with expected data transfer to be in the range of 50 gigabits per second and also with much less power dissipation [18]. The breakthrough of a light-based technology requires a number of building blocks such as lasers, optical waveguide, modulators and photodetectors. Si photonics has come to face up to this challenge by inventing high performance optical components.

1.2 CMOS Silicon Photonics

Silicon photonics refers to the technology that creates high performance Si based optical components taking advantage of CMOS compatible material and techniques used in electronic technology. For example, the long-standing (more than 40 years) use of Silicon for device fabrication in electronic industry, enables not only sound understanding of the physics of Silicon but also manufacturing tools to be well mastered. Thanks to that, small electrical components (few nanometers) which are available today. By taking advantage of that and also with the development of the silicon-on-insulator technology we are able now to transfer the knowledge and the technology of Si based electronics in order to fabricate small and low cost optical components thus making feasible the development of silicon-based photonic integrated circuits.

As it is already observed in long-distance data propagation (exceeding 10 meters), electrical "buses" are successfully replaced by optical ones offering more than 100,000 times higher data transfer. Therefore the limitations of electrical interconnects are overcome. The same trend now applies to on-chip data communication with the copper wires to be replaced with the so called optical interconnect system. The construction of this system requires elementary optical components such as lasers, modulator, optical waveguides and photo-detectors to be integrated on a Silicon wafer (Fig. 9.1). An Si based photonic integrated circuit [2] transfers optical signal from one point to another one using (a) an optical source to produce continuous light, (b) a modulator to encode the optical data, (c) multiplexer to couple different wavelengths to the waveguide,(d) an optical waveguide as the data optical 'bus' and (e) a photodetector in order to transform the optical signal to electrical. Several paradigms of Si based passive devices such as waveguide and multiplexer are already proposed in the literature. During the last few years most of the efforts have been directed towards active photonic devices such as lasers, photodetectors and modulators. The critical issues involving these elements for intra-chip applications are power consumption and device footprint. Some of these devices are already demonstrated in the literature and are briefly reviewed below.

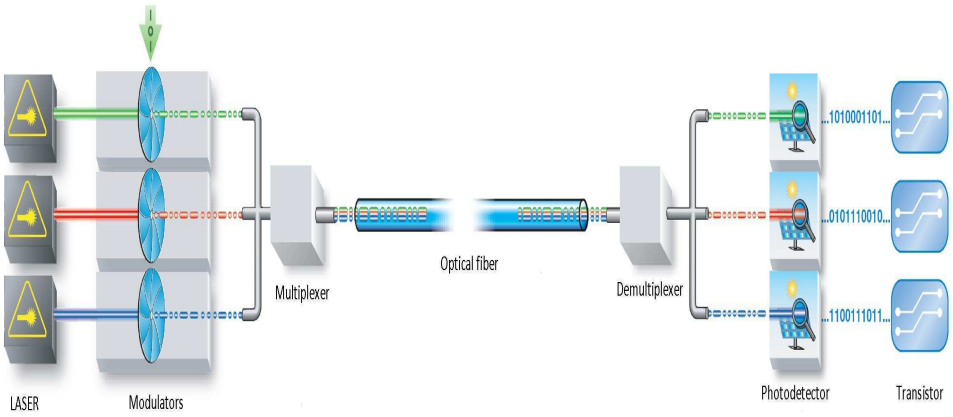

FIGURE 1.4 – *The basic optical components of integrated circuit [2]*

As an optical source, semiconductor diode laser is an excellent candidate because it emits monochromatic and directional light. The principle of operation is based on enhancement of radiation by stimulating emission. The careful choice of material is again critical in this case. Using silicon as the active material for laser is not a good choice because it has an indirect band gap. This means that when the conduction band electrons are excited, the recombination process of electrons will give light only if there is momentum (absorption or emission of phonon) and energy conservation, making it less efficient for radiative emission. A silicon based laser operated by Raman scattering instead of photon emission is reported [19]. However, it is hard to implement for practical application as the excitation comes from another pump laser. Better materials for emitting light are those of direct band-gap, like the III-V elements but are not CMOS compatible as there is a crystal lattice mismatch compared to the silicon. Although, the integration remains a non-trivial problem it can be solved by the new technological achievements such as wafer bonding technology. Given that, several types of lasers were reported such as microdisks [20, 21, 22], Fabry-Perot lasers [23, 24], racetrack resonators lasers [25, 26], Distributed feedback lasers [27] and Distributed Bragg reflector (DBR) lasers [28]. Microdisk lasers are of particular importance for intra-chip optical interconnects, thanks to their low-power consumption and small footprint. As have been demostraded by J. Van

Campenhout et al. [20], threshold currents as low as 0.5 mA for small footprint (few μm) microdisks can be achieved.

A photo-detector is a device that converts incident light into an electric current and is usually accomplished by using a photodiode in photovoltaic mode. When a photon of energy higher than the band gap of the active material is strike the diode, it is absorbed and an electron-hole pair is generated in the junction. The internal potential of the diode causes the charge carriers towards the electrodes and a photocurrent is produced. Using silicon for photodetection in the wavelength range of telecommunication (1.4-1.55 μm) is not a good choise since it is transparent in the infrared (below 1.1 μm). Therefore materials with lower band gap such as germanium [29, 30] or InGaAs [31, 32] grown on a Si substrate have demonstrated as more promising solutions. Both technologies have approximately the same sensitivity (1 A/W) but the speed of operation of the InGaAs detectors remains relatively low (smaller than 10 GHz [31] compared to that of germanium photo-detectors (higher than 40 GHz [33]). The latter have also a micrometer scale footprint and operate at 1.5V which makes it ideal for intrachip applications.

Modulators are devices that transform continuous optical signal coming from the laser source to discrete piece of light. Two main mechanisms are used to achieve light modulation, namely electro-absorption and electro-refraction. The former modulate the amplitude of the transmitted power and the latter changes the phase of the wave. Silicon-based modulators have gained much attention, with several devices reported with high performances (briefly described to the section 1.3). These devices rely on the free carrier plasma dispersion effect [34]. As the underlying physical effect is not strong, these efforts have led to large structures (compared to that of laser and photodetector) with high driving powers for obtaining a significant modulation depth.

Modulators are the largest (regarding the size) and the most demanding in terms of energy among the optical components of the photonic intgrated circuit. To that respect a particular attention is given to those devices. The goal of this thesis is to investigate an optical modulator using the Si photonics platform existing in CEA LETI. The following section is a brief review of different kinds of optical modulators investigated so far.

1.3 Optical Modulators

In the realization of chip-based hybrid electronic-photonic networks, integrated optical modulators are urgently required for any optical building block. The easiest way to perform light modulation is to switch on and off the optical source very fast (10GHz) by modulating the injecting current (direct modulation). However, this approach involves constant changes in the temperature leading to perturbation of the operation wavelength (âĂIJchirpâĂİ) and, in turn, distorts the optical data. In contrast an external modulation offers the advantage of high data transfer (10-40GHz) and also wavelength stabilization. In this scheme the optical source is switch to the continuous mode and the external modulator work such as shutter on-off for the continuous light. Therefore external optical modulators expected to be the key component to push towards higher bandwidths and low energy consumption of data transfer.

1.3.1 Photonic modulators

Today, commercially available optical modulators at 10 Gbps are based on lithium niobate and III-V compound semiconductors. While the former requires the use non-CMOS electro-optical materials, the latter works on the principle of electro absorption. However both materials are contaminants within the CMOS integrated photonic-electronics circuit. Using active materials that are compatible with the current micro-electronics processes, we are able to circumvent the inherent limitations of the proposed approaches listed above. Silicon itself is a CMOS compatible material and therefore modulating light through silicon will be the essential solution for the future photonic technology. Several demonstrations of integrated Si based modulators have been published/patented since 2000 and are briefly described below.

Efficient light modulators using silicon as active material are already proposed. Using strain we can break the crystal symmetry of Silicon, leading to a linear electro-optic effect useful for light modulation [35]. SiGe/Ge quantum wells is also proposed for low power dissipation optical modulators, taking in advantage the quantum-confined Stark

effect which leads to strong changes of optical absorption [36]. Finally by bonding III-V materials to silicon may enable to use their strong electro-optical properties such as thermo-optic plasma dispersion effects as well as plasma dispersion effect.

Although silicon does not in normal circumstances exhibit an electro-optic effect, other mechanisms are available for modulation and in particular the plasma dispersion effect has been proven as a promising approach of achieving high speed modulation in silicon devices. In this effect the real and imaginary parts of the refractive index are changed due to the concentration of free charges in silicon. Soref et all [34] have experimentally demonstrated that induced real refractive index and absorption coefficient variation (due to the free charges) at a wavelength of 1.55 μm is given by the following formula :

$$\Delta n = \Delta n_e + \Delta n_h = -[8.8 \times 10^{-22} \Delta N_e + 8.5 \times 10^{-18} (\Delta N_h)^{0.8}] \tag{1.1}$$

$$\Delta a = \Delta a_e + \Delta a_h = -[8.5 \times 10^{-18} \Delta N_e + 6 \times 10^{-18} (\Delta N_h] \tag{1.2}$$

where Δn_e and Δn_h are changes in refractive index resulting from changes in the free-electron (ΔN_e) and free-hole carrier concentrations (ΔN_h), respectively, and Δa_e and Δa_h are the changes in absorption resulting from changes in the free-electron and free-hole carrier concentrations, respectively.

The required change in the free carrier concentration is achievable through a variety of different mechanism such as carrier injection, depletion or accumulation. Carrier depletion and accumulation, unlike carrier injection, are not limited by the relatively long carrier lifetime in silicon and consequently the faster reported devices have utilised these mechanisms. However, the free carrier dispersion effect in silicon is insufficient, leading to long devices [3] (L is of the order of millimetres for the modulator shown in Fig. 1.5) with high energy demands and therefore inappropriate for intra-chip optical interconnect.

Two main effects, namely Electro-Absorption (EA) and Electro-Refraction (ER) are used to achieve light modulation. EA induce absorption (by changing the optical absorption of the material) and directly modulates the intensity of the propagating light.

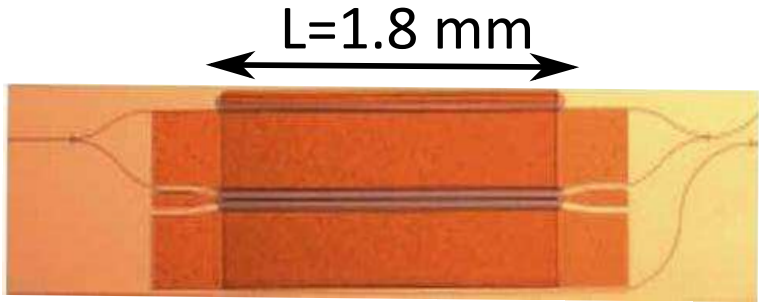

FIGURE 1.5 – *Optical microscope view of the silicon-based optical modulator demonstrated experimentally using standard CMOS processing techniques [3].*

ER induce phase shift of the propagating waves (by changing the refractive index of the material) and can be exploit for modulation in two typical geometrical configuration, namely MachâĂŞZehnder interferometer (MZI) and ring resonator. In the case of ring resonators [37, 38], the induce phase shift, changes the resonant condition allowing to switch between on- and off-resonant states. Using MZI, we convert the induced changes of the relative phase of the two propagating modes, to intensity modulation. Although more compact devices are achievable using resonant based structures, the MZI configuration remains more attractive. This is because the resonator optical bandwidth is limited to 1 nm and thus makes it ultra sensitive to external parameters such as the temperature.

The ideal Silicon optical modulators will be characterized by CMOS compatibility, ultralow power consumption, small device size, high modulation speed as well as large modulation depth and optical bandwidths. Given the fact that these requirements contradict each other, innovation is needed in order to combine all these requirements with an optimal trade off. Recently, researchers proposed that by using the properties of surface plasmons [39], such as high field confinement it is possible to create a modulator which fulfill several of the mentioned requirements. Such kind of modulators is reviewed to the following section.

TABLE 1.1 – Performances of optical modulators recently demonstrated expirementaly

Modulation Principle	Speed Achieved (Gbit/s)	Footprint (μm)	Modulation Voltage(V)	Energy **(fJ/bit)**	Working Spectrum (nm)
Intel MZ Depletion pn junction	20 /s Gbit/s	6000	6.5	28000	30
IBM-Si injection pin	10 Gbit/s	200	7.6	5000	-
Cornell injection microring	12.5 Gbit/s	33	8	300	1
MIT BAE GeSi EA	1.2 Gbit/s	30	3	50	14
Kotura Ge EA pin	12.5 Gbit/s	45	4	100	30

1.3.2 Plasmonic modulators

Surface plasmons polaritons (SPP) are electromagnetic waves strongly coupled to the free electrons of the metal. They are propagating along the metal-dielectric interface (direction x) and decays exponentially as one moves away from the interface (Fig. 1.6). The field penetration (D) into the dielectric can be subwavelength and it depends on the excitation wavelength and the materials. For example in a copper/SiO_2 interface the typical transverse decay lengths at the telecom wavelength is 20 nm inside the copper

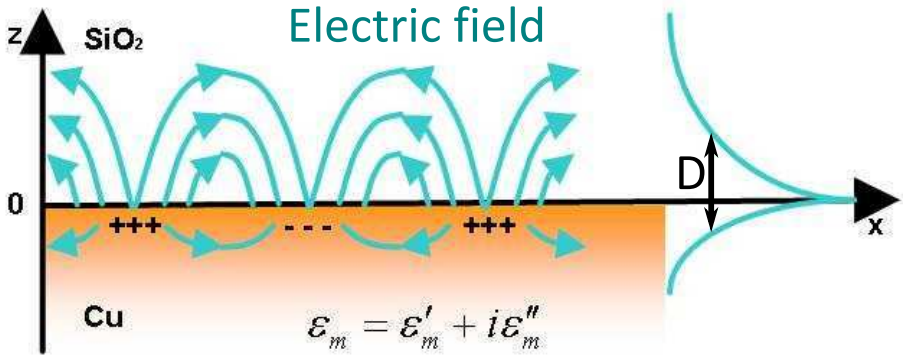

FIGURE 1.6 – *Transverse dependence of the E field of SPPs on a Cu/SiO_2 interface.*

and 1000 nm inside the SiO_2. For such interfaces, the typical propagation length is of the order of several hundreds μm. Combining the propagation properties of optical waves with the high localization of electronic waves, plasmons can achieve extremely large field confinement. This confinement property can be exploited to develop novel optoelectronic devices such as sensing [40], light emission [41, 42], photodetectors [43] and modulators [44].

Surface Plasmon field confinement is expected to be very helpful in the context of modulators. The environment sensitivity of metal/dielectric interface SPP modes is well known and it is already used for different applications such as bio-sensing and optical active components. The physical origin of this sensitivity is basically related with the field confinement of the SPP mode at the metal surface. However, when considering structures more sophisticated than just a metal/dielectric interface, such metal/semiconductor/metal systems, this confinement can be increased to a level that can be only hardly reached with standard index-guided modes (Fig. 1.7). Thus, the field confinement properties of SP modes and the increased sensitivity to small refractive index changes of the dielectric in contact with the metal make these modes rather unique for applications targeting high-frequency modulation of an optical signal. Fig. 1.8 shows the performances of different technologies in terms of speed and size. Based on this reference, plasmonics can offer the size of electronics because can highly confine modes

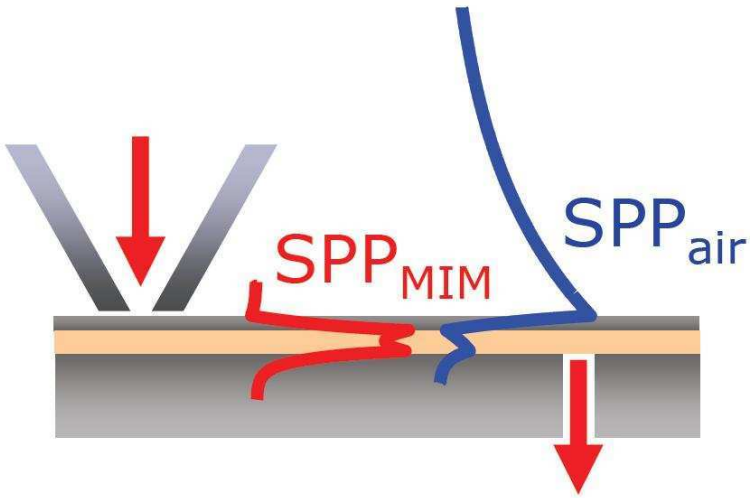

FIGURE 1.7 – *H field mode profiles of the two waveguided SPP modes : The highly confine mode inside the Metal-Insulator-Metal (MIM) stack(red) and the less confine metal/air mode(blue). Figure taken from [4].*

and also to travel data with the speed of photonics. The drawback here is that the high confinement is associated with propagation losses. Therefore by designing our device we have to be careful to have high modulation depth for compact devices (resulting from high confinement) while keeping the optical losses in acceptable values.

Taking in advantage of the key assets of use of metals for both electronics (electrodes) and photonics purposes (electromagnetic concentration) plasmonics can fuel the prospects of scale down the dimension of optical modulators.

Different schemes of SPP-based modulators were proposed and reported so far. Basically, one can identify three types of SPP modulators ; (i) all-optical SPP modulators (ii) thermo-optics modulators, and finally (iii) electro-optics modulators.

Different configurations of all-optical SPP modulator were described and reported recently. First, a rather specific configuration using the properties of gallium was suggested and demonstrated by Krasavin et al. [45] This system relies of the phase change of gallium (due to its very low melting point) when illuminated by a pump signal at 1064nm. The last all-optical modulator described in the literature exploits a two slits

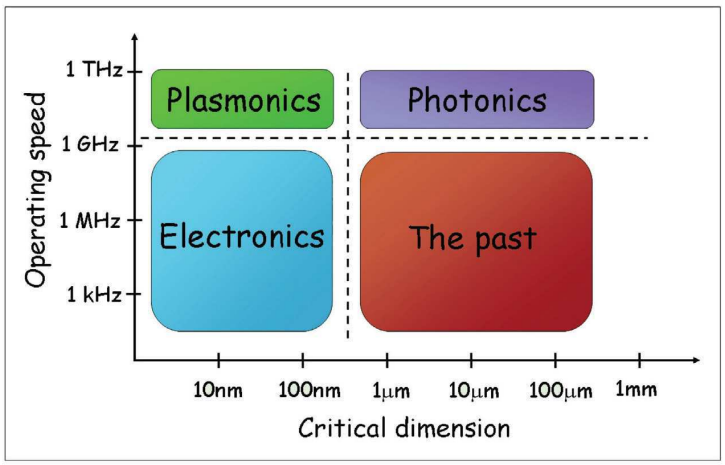

FIGURE 1.8 – *According to [5], plasmonics offers the size of electronics and the speed of photonics.*

interferometer configuration . In this configuration, the modulation of a SPP mode is performed by changing the optical properties of CdSe quantum dots. When pumped at a frequency within their maximum absorption band (around 515 nm), the Q-dots are placed in an excited state promoting the absorption of the probe beam (1415 nm). This light-induced absorption modifies the interaction between the incident probe beam and the probe SPP leading to the modulation of the signal at the probe frequency. While these results are impressive, it is clear that all optical SPP modulators do not have a practical future because they require materials that are not CMOS compatible.

Thermo-plasmonic modulators [46, 47] are already proposed based on metal waveguide supporting SPP modes and heat dissipation within the metal to induce index modulation. The justification for the use of metal waveguide is that the heat source can be localized at the place where it is the most efficient. Given that, Gosciniak et al [46] demonstrate thermo-optics plasmon modulators relying on Mach-Zehnder interferometers comprised of gold long-range surface plasmon polariton (LR-SPP) waveguides. This type of modulators exhibits strong output modulation, low power consumption (1.4 mW), but only moderate response time (1 ms).

Electro-optic plasmonic modulator are already proposed in the bibliography as a solution for achieving higher bandwidth modulation. A proposition was made by Jannson et al. [48] and is based on mode coupling between light propagating in a dielectric waveguide to a nearby metal film placed a certain distance away : the coupling coefficient between the optical mode in the waveguide and the plasmon polariton mode is made variable through a e.g. voltage-dependant property (for example the refractive index) of an electro-optical material in contact with the metal. Such a material is often taken as $LiNbO_3$ for example. However the electro-optical constants of those materials are weak and applied voltage remains high and system dimensions large. Moreover, the latter aspect precludes the use of plasmon modes in configuration where electromagnetic fields are very confined but lossy. The configuration proposed by Breukelaar et al. [49], relying on the electrically induced long range plasmon polariton mode cut off, could not circumvent this drawback.

More recently, Liu and Xiao [50] suggested in a theoretical work an electro-optical switch (modulator) relying on the use of a metal film supporting surface plasmon modes embedded within a ferroelectric medium. By adjusting a bias voltage at the surface of the electro-optical material (such as Ba0.5Sr0.5TiO3), they show numerically that for a given propagation distance, interference between the symmetric and the anti-symmetric surface plasmon modes could be switched from constructive to destructive leading to the localization of the SPP field at one or the other metal thin film interface. Following a very similar strategy, this concept was extended to the case of LR-SPP and demonstrated experimentally by Berini et al. [51]. In this system, a very thin film supporting a long-range plasmon mode is embedded within two layers of lithium niobate with Z-axis orientation pointing in opposite directions. By applying a voltage, a refractive index contrast between the two sides of the gold film is created leading to an increase of the LR-SPP propagation losses. A much more compact modulator relying also on the use of BaTiO3 was proposed and investigated by Dicken et al. [52]. This modulator is actually a double-slits interferometer exploiting the interaction between a directly transmitted field and two SPP counter-propagating along an interface in contact with the lithium niobate.

However, the underlying materials are contaminants and therefore hard to be used in the CMOS platform.

Amongst the numerous patents and publications describing optical plasmonics modulators, very few have the potential to integrate in CMOS integrated photonics. In a recent article of Melikyan et all [53] they demonstrate an EA modulator operates at 1.55 μm. In this device, the absorption change is a result of voltage-induced carriers in ITO, providing thus a modulation speed which is free from any slow carrier-related phenomena. Furthermore, Zhu et al. [54] they demonstrate a Si nanoplasmonic electro-absorption modulator using copper as a metal electrode. This novel device is fabricated within a CMOS environment. They suggest that this modulator relies on accumulation of charge carriers inside a MOS, induced by an applied voltage. However, such device dissipate an unacceptable power due to the high leakage current that is observed (0.1 mA for 2 μm^2 surface). Furthermore, we speculate that the thermal effect plays an important role to the measured modulation depth due to the high current passing from the insulator. Finally, the so-called PlasMOStor device proposed by Dionne et al. [6], use Si as active material in order to modulate light in a vertical $Ag/SiO_2/Si/Ag$ configuration. In the following section we present a detailed description of this device, since it is the subject of this work.

1.4 Integrated PlasMOStor

PlasMOStor it is an interferometric configuration used for performing modulation. The device employs a four-layer of Ag-oxide-silicon-Ag (Fig. 1.9) that supports both photonic and plasmonic modes (Fig. 1.10a). In this electro-optical device, the modulation is achieved by changing the index of an n-doped Silicon layer by means of charges accumulation in a MOS structure. Such an index change is at the origin of the disappearance of a hybrid photonic mode excited at a frequency close to its cut-off. The perturbation of the beating created by the interference of the photonic mode and a plasmonic mode creates a modulation of the transmitted optical signal with a depth in the range of 3

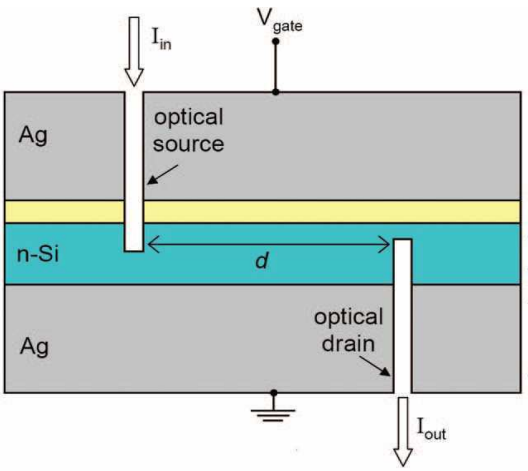

FIGURE 1.9 – *Cross section (schematic) of the plasMOStor modulator [6]*

to 4 dB in a device 2.6 μm long (Fig. 1.10b). The operating voltage of plasMOStor was estimated to be 1V which is compatible with the low energy consumption demands of integrated photonics technology. It is also suggested that the bandwidth of the device, is fundamental limited by the speed of the formation of the MOS accumulation layer (as it is in a conventional small-geometry MOS field-effect transistor) and therefore gigahertz operation is expected. However, this structure is not completely compatible with the CMOS environment because they use contaminants metals such as silver. This issue can be solved by switching to CMOS metals such as copper or aluminum.

The outstanding device performances provided by the innovative modulation concept of the plasMOStor, originates the interest to integrate this concept in a CMOS environment available on LETI platform in colaboration also with CALTECH. To do that we take advantage of the key assets of microelectronics and Si photonics technology, namely maturity and the low-loss long-range optical circuitry (developed for CMOS photonics) and the well known fabrication technology of the metals (developed for microelectronics) for both electronics (electrodes) and photonics purposes (electromagnetic concentration). The experimental proof of such approach would bring a new paradigm in the design of electro-optical modulators. Fig. 9.2 show schematically the integrated plasMOStor consisting of an Silicon On Insulator (SOI) waveguide integrated with a MOS plasmon

(a)

λ=1.55µm	|E| mode profile	Mode Index	Loss (dB/µm)
Off state (V=0) *depletion*	Ag SiO_2 Si Ag	3.641	0.207
		0.375	2.37
On state (V>0.7V) *accumulation*	Ag SiO_2 Si Ag	3.649	0.228
		0.033	28.14

(b)

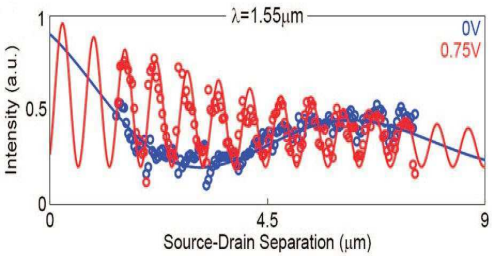

FIGURE 1.10 – *Mode profiles, refractive indices and losses supported by the plasMOStor stack (a) ; Optical intensity as function of the source-drain separation for the on state and off-state(a)*

waveguide (plasMOStor).

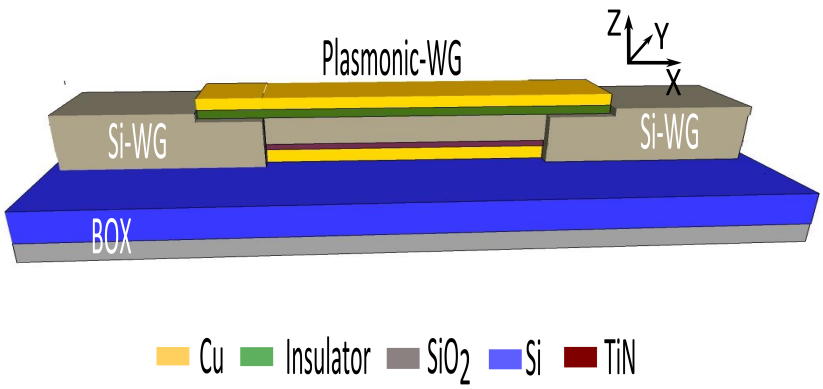

FIGURE 1.11 – *SOI based integrated plasMOStor*

1.5 Outline of this thesis

This thesis presents experimental and theoretical work, investigating the potential of CMOS integration of plasmonic modulator. The chapters are organized as follows :

Chapter 2 describes the experimental and numerical methods used to investigate the physical mechanisms underlying the operation of our copper based plasmon MOS

modulators. These methods are adapted to the specifications of our device which are the use of a metal instead of highly doped polycrystalline silicon contact and the single micron-scale dimensions of our devices. Finally an automated and reliable method is described for large-scale electro-optical characterization system.

Chapter 3 investigates the material aspects and also the technological steps required in order to realize an integrated plasMOStor [10] within the CMOS environment. The main constraints related with material aspects come from the need for electrical contacts with metals with high electrical conductivity in order to ensure low optical losses. To that respect we choose Cu as the most promising metal for the integration of plasmon devices. After that choice, we show that the insertion of an ultrathin stoichiometric Si_3N_4 layer in a MOS stack acts as an efficient diffusion barrier of Cu, while preserving the low optical losses operation of the device. Finally, we describe the main technological steps in order to fabricate the plasMOStor stack integrated with a mono-mode Si waveguide. Fabrication of our modulator require the use of both front-end and Cu back-end technologies, which are properly combined only a few nanometers one from each other thanks to the use of a diffusion barrier layer.

Chapter 4 presents the experimental realization of an efficient light coupling scheme between the SiWG and the integrated plasmostor on the SOI platform. Three dimensional FDTD is also exploited in order to simulate our plasmonic coupler structure. The experimental and simulation results are in agreement illustrating that the highest-efficiency geometry corresponds to a compact coupler of 0.5 μm length having coupling loss of only 2.5 dB per coupler (experimental value).

Chapter 5 discusses the electro-optical behaviour of the integrated plasmostor. We demonstrate first that by using high dielectric constant (high-k) materials such as Al_2O_3 and HfO_2 we can achieve an optimized MOS structure with low operation voltage and low optical losses. Given that interest, we decided to experimental validate the Cu/high-k as an electrical reliable stack for future applications to the MOS plasmostor stack. After that, we present a detailed electro-optical investigation of the integrated plasmostor. The theoretical study shows that the Electro-Absorption (EA) is the dominant effect for light

modulation with the accumulation conditions as the most efficient operation mode. This was followed by the electrical as well as electro-optical (EO) experimental investigation. Devices show accumulation capacitance of few fF and leakage current below 10fA. Finally, an optical modulation having a capacitive signature it was demonstrated, in agreement with simulations.

Finally, we give the final conclusions of this thesis and we discuss future research directions for CMOS plasmonic modulators.

Chapitre 2

Experimental and numerical methods

In this chapter we discuss the electrical and optical characterization methods which are used to investigate the physical mechanisms underlying the operation of our copper based plasmon MOS modulators. The use of copper for the contact electrodes is an important feature of this study. From a plasmonic point of view, the low DC electrical resistivity of copper can lead to a low propagation loss [55]. However, without the use of a metal-dielectric interface layer, during annealing, copper may rapidly diffuse into the dielectric layers [56], degrading significantly the device performance.

In order to electrically characterise the MOS stack and in particular the copper diffusion effect and the performance of an interlayer diffusion barrier, a wide range of electrical techniques were employed. The understanding of the electrical behaviour of our MOS devices was enhanced through the use of numerical simulations obtained using either SILVACO, a commercial software package, or an in-house package, 'Le simulateur' [57] (section 2.1).

Following electrical characterisation, optical investigations were performed. Results of experimental transmission measurements were interpreted in conjunction with 3D Finite difference Time Domain (FDTD) simulations and analytical methods specifically

developed for this study (see 7.1), in order to understand the optical behaviour of the devices (section 2.2).

Finally, we describe a reliable automated large-scale electro-optical characterisation system which was developed to test the optical transmission, current-voltage characteristics and electrically induced modulation depth for a large number of devices. This system was specifically adapted for the single micron-scale dimensions of our devices (section 2.3).

2.1 Electrical characterization methods

In this section, we detail the electrical characterization methods that were used to investigate the electrical performance of different dielectric layers and also to study the integrity of a diffusion barrier designed to mitigate the penetration of copper into the underlying dielectric layers. To that respect, Capacitance-Voltage (C-V), Conductance-Voltage (G-V) and Linear Ramp Voltage Stress (LRVS) was performed and are briefly described below.

The capacitive response C-V, can give insight about keys parameters such as the equivalent SiO_2 thickness of the dielectric (EOT) and the flat band voltage V_{fb}. The extraction of these parameters is crucial in this thesis in order to estimate the break down field across the insulator. Moreover by estimating the V_{fb} we can extract information about the defects inside the insulator. Finally, C-V measurements can give the charge concentration in a wide range of voltages. The extraction of this quantity can be used for accurate electro-optical simulations.

The standard conductance method G-V developed by Nicollian et al. [7] was used to study the electrically active interface states at the SiO_2/Si interface. Furthermore, when the conductance and the capacitance is estimated, the resistance of our device can be calculated. This parameter will finally define the RC delay of our device which is critical parameter defining the speed of our modulator.

Finally, the maximum break down field of the insulator was estimated using linear

ramp voltage stress (LRVS). This technique is extensively used to investigate the quality of the insulator. The interest of LRVS experiment is to be very fast and to provide information on intrinsic as well as extrinsic breakdown behavior of our device [58].

2.1.1 C-V and G-V measurement

The measurement of the capacitance and the conductance is carried out by grounding the substrate while applying a combination of voltages on the gate metal : a DC component V_g that determines the voltage at which the measurement is taken, and an AC component v_g (40 mV) with frequency varying from 10 to 100 kHz. V_g allows polarizing the capacitor in different MOS modes (accumulation, depletion, inversion). The analysis of the response of the device to the excitation voltage v_g gives us its capacitance ($C = \frac{dQ}{dv_g}$) for a bias V_g. The measurement were performed with HP4284 impedance analyzer meter (Fig. 2.1). By connecting the two electrodes (gate and substrate) the LCR meter measure the current (I) flowing through a device, the voltage (V_g) across the device, and the phase angle between the measured V and I. From these three measurements, all impedance parameters can then be calculated. Since the impedance is calculated, then the capacitance is estimated from its imaginary part.

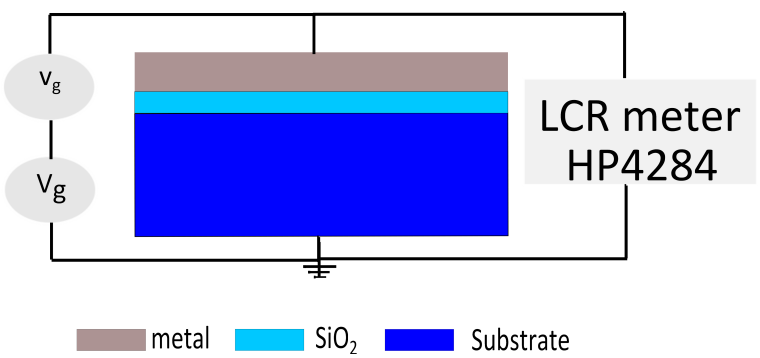

FIGURE 2.1 – *Experimental configuration for measuring the capacitance of a MOS structure.*

Fig. 3.4 presents a measure C(V_g) of a MOS capacitor. Two operating modes can be distinguished, the accumulation and the depletion regime. The boundary between the two

systems is the flat band condition. The inversion is not visible because the measurement frequency is too high to allow diffusion of minority carrier. In this figure, we also present a simulation of the characteristic $C(V_g)$ extracted by the model described in the section 2.1.4.

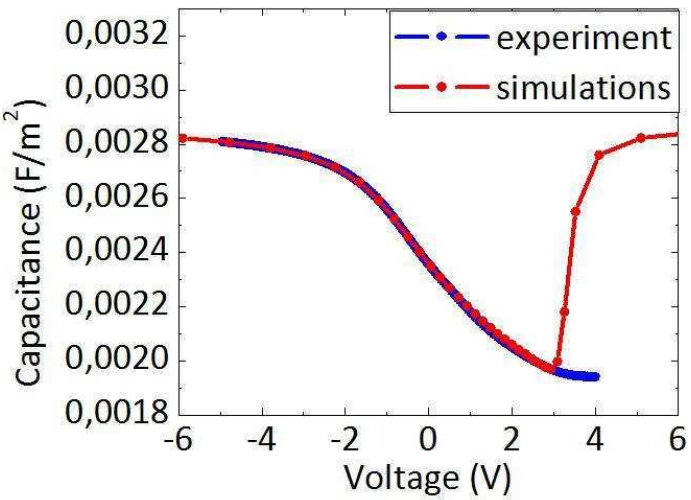

FIGURE 2.2 – *C-V characteristic of MOS capacitor consists of Cu/Si_3N_4 (3nm)/SiO_2 (10nm)/p-doped Si (10^{18}) at 100 kHz voltage sweep frequency. Blue line : experimental results, red line : simulations (see section 2.1.4.1). The accumulation and depletion mode are also presented.*

We also use the same experimental set up to measure very low capacitance, in the range of fF. Due to the fact that the target capacitance is ultra low, we made some calibration before the measurement. First we measure the capacitance of a reference structures consisting of two open-circuit probe pads. A second reference structure consisting of interconnects but not target device is also measured. De-embedding the parasitic capacitance and using the open circuit connections we are able to measure the capacitance of the target device which is of the order of few fF. An example of such measurement is shown in the Fig. 2.3.

The interface defect density D_{it} between silicon substrate and gate insulator is an important parameters that directly influence the MOS device performances such as the

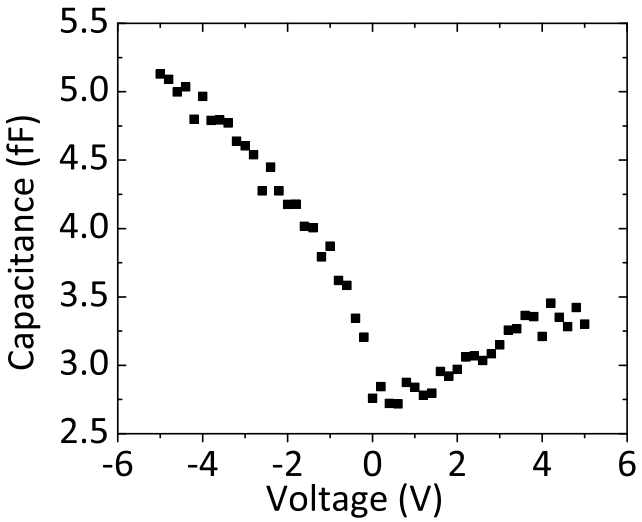

FIGURE 2.3 – *Experimental results of ultra low capacitance measuring using the impedance analyser meter, HP 4284. The measurement was performed to the plasmostor device of active length = 1 μm*

leakage current through the dielectric (i.e an increase of defect density can be translated as an increase of the electrons trapped state in the oxide or an increase of the weak spot in the dielectric, resulting in a subsequent increase of leakage current) and the gate dielectric reliability. In this thesis, we use this parameter in order to investigate the copper induce ionic defects at the interface of insulator/Silicon.

Several methods were proposed in order to measure the interface defects. Here, we use the standard parallel conductance method developed by Nicollian et al. [7]. To that aim, capacitance and conductance (CâĂŞGâĂŞV) characteristics are performed using the HP4284 impedance analyzer at frequencies ranging from 1 kHz to 1 MHz with an applying modulating signal of 40 mV and V_g varying from -5 V to +5 V with a step of 0.01 V (Fig. 2.4). Subsequently, the equivalent parallel conductance G_p/ω is estimated by :

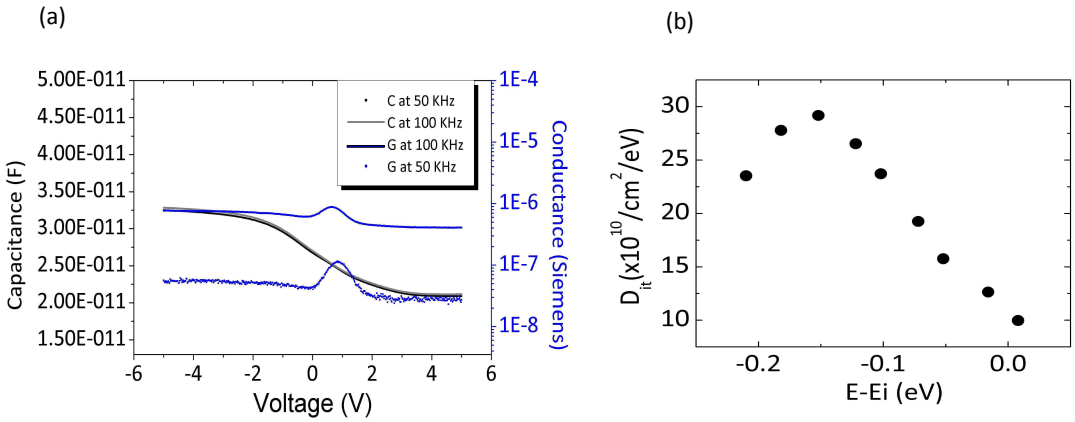

FIGURE 2.4 – *(a) An example of C-V_g and G-V_g measurement at 50 kHz and 100 kHz.(b) Extraction of interface defect density using the conductance method developed by Nicollian et al. [7].*

$$G_p/\omega = \frac{\omega C_{ox}^2 G_m}{C_m^2 \omega^2 (C_{ox} - C_m)^2} \tag{2.1}$$

The interface trap density D_{it} is then extracted from the equivalent parallel conductance through the relation :

$$D_{it} \simeq \frac{2.5}{q} (\frac{G_p}{\omega})_{max} \tag{2.2}$$

where C_{ox} is the oxide capacitance, G_m is the measured conductance, C_m is the measured capacitance and ω is the angular frequency (ω=2πf). We note that for the extraction of Eq. 2.2 we assume that a surface potential fluctuation is neglected. Fig. 2.4 shows an example of the measured capacitance (C_m) and conductance (G_m) at 50 KHz and 100 KHz (2.4a) and also the extracted interface defects density at different energy levels (E) with respect to the the intrinsic Fermi level (Ei) for Cu/Si_3N_4 (3nm)/SiO_2 (10nm)/Si MOS capacitor.

2.1.2 Non ideal C-V characteristics

Several phenomena are responsible for the deterioration of the C-V characteristics such as high leakage current, high series resistance (R_s) and the creation of an undesired loss interface layer between the oxide/silicon or metal/silicon interface. These phenomena usually cause to an additional parasitic capacitance and also to an increase of the resistance of the device. The latter is of particular importance for this thesis, since will define the RC time constant of the device and thus its operation speed. Therefore the phenomena described hereafter are playing a key role in the performance of our devices.

The first is related to leakage current. When the insulator thickness becomes smaller than 3 nm, the leakage current through the insulator becomes important (around 1 $A.cm^{-2}$ [59]) and may affect the C-V characteristics especially in accumulation and inversion region [60]. As a result the estimation of oxide capacitance is inaccurate and consequently leads to unreliable extraction of oxide thickness, defect density and break down field of the insulator. However, in our case the oxide thickness is larger than 3 nm which leads to low leakage current. Therefore, it can be assumed that tunnelling is not a significant issue in our devices.

The series resistance is also identified one of the reason causes deterioration of C-V [61]. The series resistance (R_s) can come from either the substrate or the backside of the semiconductor/metal interface. For the latter it is possible to create a Schottky contact instead of ohmic and to cause in a significant increase of the resistance ($> 1k\Omega$ [62]) which in turn affects the capacitance. The effect of series resistance can be limited via the simplified three-element model [63] by measuring the conductance and capacitance at accumulation conditions using the simple two-element (parallel) model.

Finally, it is well known that during fabrication process, if the surface cleaning is not ideal, it is possible to create an undesired loss dielectric layer between the oxide/silicon [64, 65] or metal/silicon interface. This layer may induce additional resistance and parasitic capacitance in our system. These effects can alter the MOS capacitance (especially in accumulation regime) and also can significantly increase the RC time constant of our device. Since in some of our devices we deposit a TiN direct to silicon it is possible to

suffer from this unwanted loss layer.

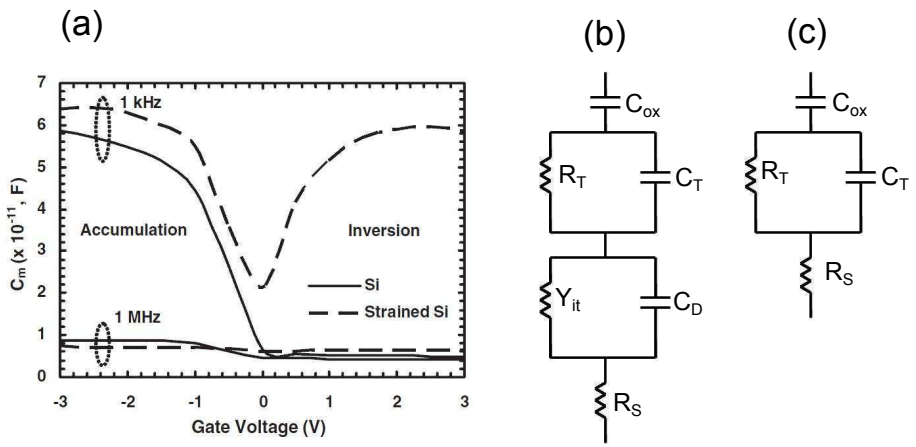

FIGURE 2.5 – *(a) Measured capacitance at different frequencies illustrating the tremendous effect of the unwanted loss dielectric layer taken from [8]; (b) The equivalent circuit model of the real MOS capacitor including the effect of lossy dielectric layer;(c) The equivalent circuit model of (b) but in strong accumulation.*

The phenomena described above can be summarized in an electrical equivalent model (Fig. 2.5b and c). Fig. 2.5b shows the electrical model describing a real MOS capacitor including the effect of the loss dielectric layer and also the series resistance, where C_{ox} is the oxide capacitance, C_D the depletion layer capacitance, Y_{it} is the admittance due to the interface trap charge, C_T and R_T is the capacitance and resistance of the unwanted loss layer, respectively. By biasing the capacitor in strong accumulation, the effect of the depletion capacitance and admittance (2.5c) are limited and therefore we can estimate the parasitic effect of the loss layer (see [8] for more details).

2.1.3 Linear ramp voltage stress measurement

When qualifying the reliability of a device, the extrinsic break down mode due to process induced defects is one of the most important parameter to be investigated [58]. In this thesis we use the extrinsic mode of Linear Ramp Voltage Stress (LRVS) measurement (with the measurement set-up described in 2.1.1) as a method for investigating process

induced defects in the insulator which, in our case, are related to the copper diffusion inside the insulator.

Break down reliability measurement such as LRSV consists in applying a linearly increasing voltage with typical speed of 0.5 V/s and detecting the break down at a critical gate current of 100 mA/cm^2. The interest of LRVS experiment is to be very fast and to provide information on intrinsic as well as extrinsic breakdown events. The usual way of describing the statistical analysis of the break down parameters is the Weibull approach [66]. This approach is widely used in CMOS foundry. Fig. 2.6 shows a Weibul scale plot of the cumulative distribution function (F), $ln(-ln(1-F))$, of the break down field for a large number of capacitors. One can distinguish two types of statistical population as suggested by the presence of two linear regions. The region of high break down fields which is associated with intrinsic quality of the insulator (e.g., bonding energy, lattice strength) and the region with low field to break down which is related to the extrinsic behavior such process induced defects.

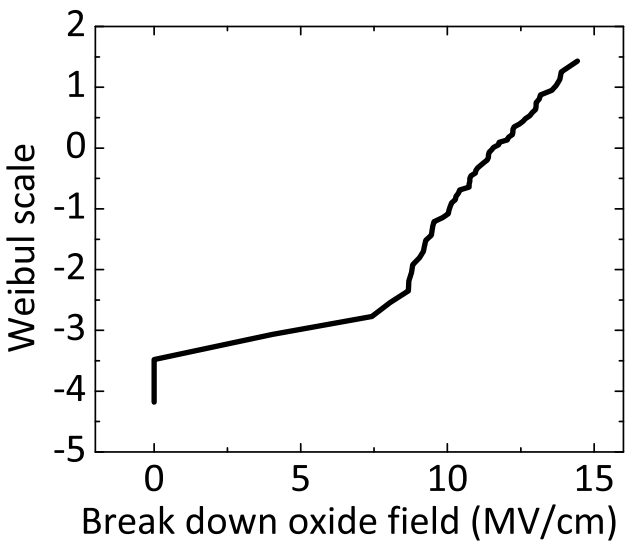

FIGURE 2.6 – *Typical Weibul scale plot of the maximum voltage to breakdown as obtained on a population of 70 MOS capacitors using LSRV*

2.1.4 Modelling and Extraction of MOS parameters

In this section, I will describe the electrical simulation tools, such as Silvaco and an in-house simulator,named "Le simulateur" (developed by Ch. Leroux [67]), that were used for the understanding of the experimental electrical behavior of MOS devices.

With regards to the electrical behavior, the MOS capacitor can be considered as a two plate capacitors connected in series (Fig. 2.7) : the oxide capacitance C_{ox} and the substrate capacitance C_{sub}. The oxide capacitance per unit area is given by $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$, where ϵ_{ox} and t_{ox} is the dielectric constant and physical thickness of the oxide. The substrate capacitance is given by $C_{sub} = \frac{dQ_{sub}}{d\psi_s}$, where Q_{sub} is the substrate charge at a given voltage V_g and ψ_s is the surface potential. The total measured capacitance can be written as [68] :

$$\frac{1}{C_m} = \frac{1}{C_{sub}} + \frac{1}{C_{ox}} \tag{2.3}$$

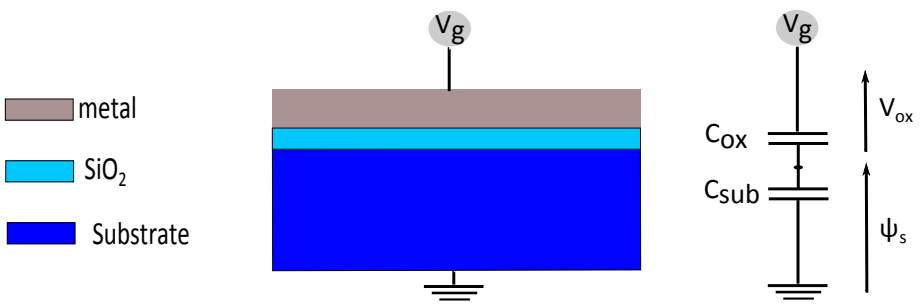

FIGURE 2.7 – *(a) Schematic picture of a MOS structure ; (b) Electrical equivalent model for the capacitance.*

2.1.4.1 "Le simulateur"

A simulation programme, "Le simulateur", is developed in LETI [67] to model the distribution of charge inside the silicon taking into account quantum mechanical effects. In this model by giving the substrate doping (as an input parameter) we can extract both the charge in the semiconductor (Q_{sub}) and the substrate capacitance (C_{sub}) as

a function of the surface potential ψ_s. Before starting our simulations we calculate the C_{sub} and Q_{sub} for different doping concentration varying from 10^{15} to $10^{21}cm^{-3}$ (10 values by decades) and the results have been stored in a database. Therefore by choosing the value of the doping that we are interesting we can have quickly the C_{sub} and Q_{sub} of the device being analysed without having to perform each time the simulation. We note that, using the same programme, more accurate simulations can also consider the influence of interface states at high and low frequencies. Fig. 3.4 shows a simulation curve (red line) of the characteristics $C(V_g)$ with a nice fit accordingly to the model described above. This allows the extraction of the equivalent oxide thickness (EOT) and flat band voltage V_{fb}. In this work, we used that method to extract the V_{fb} and the Equivalent Oxide Thickness (EOT) of the experimental C-V.

2.1.4.2 Extraction of V_{fb} based on Maserjian function

In this study, the V_{fb} is extracted using the Maserjian function. This specific function, usually denoted as Y, is given by the following equation :

$$Y = \frac{1}{C^3}\frac{dC}{dV_g} \tag{2.4}$$

This function has the characteristic property to be independent from the C_{ox} of the device and therefore can give the most reliable values for the V_{fb}, especially when the maximum accumulated measurable capacitance is reduced (for example due to high leakage current through the insulator or/and high substrate resistance, R_s). Indeed, one can show that in the expression of Y, only the C_{sub} and ψ_s are involved :

$$Y = \frac{1}{C_{sub}^3}\frac{dC_{sub}}{d\psi_s} \tag{2.5}$$

It can be demonstrated that for $\psi_s = 0$, which is the case that the V_g corresponds to V_{fb} , the function Y is equal to Ymin /D. The parameter D depends on the majority carrier concentration profile and varies from 3 to 9 according to the substrate characteristics (intrinsic, doped or degenerate) [69].

2.1.4.3 Extraction of EOT

In this section we show an accurate extraction of EOT by taking into account the quantum effects. The extraction process of EOT is summarized in the following steps : (a) Assuming a reliable extraction of V_{fb} from Maserjian methods, it is possible to determine the substrate charge (Q_{sub})versus V_g using the following equation :

$$Q_{sub}(V_g) = \int_{V_{fb}}^{V_g} C_m(V_g)\,\mathrm{d}V_g. \tag{2.6}$$

(b) Knowing the substrate charge we can use the data base of the simulator (see 2.1.4.1) to estimate the substrate capcitance $C_{sub}(V_g)$. Finaly, the oxide capacitance can be estimated using the following equation :

$$\frac{1}{C_{ox}} = \frac{1}{C_{mes}(V_g)} + \frac{1}{C_{sub}(Q_{sub}(V_g))} \tag{2.7}$$

Since the C_{ox} is extracted then the EOT is simply found by :

$$EOT = \frac{\epsilon_{ox}}{C_{ox}} \tag{2.8}$$

where ϵ_{ox} is the dielectric constant of the oxide.

2.1.4.4 Silvaco

The electrical behavior of a MOS capacitor is modelled also by using a two dimensional device simulation package ATLAS from SILVACO. The purpose of using this software is to extract the profile distribution and the density of carriers inside the Si. It is noted that the accurate extraction of these parameters is critical because it will finally define the strength of the electro-optical interaction which is related with the electro-optical performance of the device (i.e modulation depth).

The carrier extraction was performed using both the classical and quantum approach. For the former we use the Maxwell-Boltzmann and Fermi-Dirac statics. For the later, a self consistent solution of the Schrodinger and Poisson equation was implemented. In this thesis, we used Silvaco as a tool to extract the charge concentration profile as an input for optical simulations.

2.2 Optical methods

This section deals with the optical tools that were developed in order to enhance the understanding of the optical behaviour of our device. First, the optical index of the materials used for the simulations are reported. This is followed by a short introduction to a home made mode solver. Finally, 3D FDTD simulations procedure used in this work are described.

2.2.1 Optical index of the materials used for the simulations

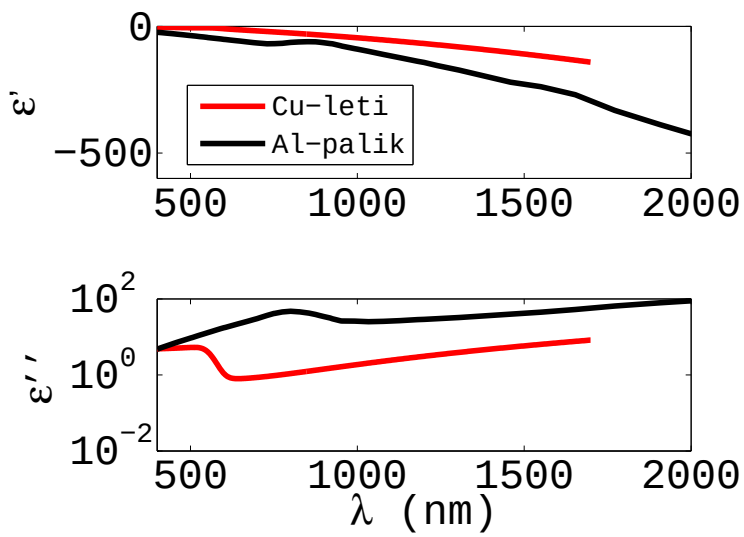

FIGURE 2.8 – *Dielectric function* ($\epsilon = \epsilon^{'} + i\epsilon^{''}$) *for different wavelenghts* (λ) *for the fabricated Cu metal measured by ellipsometry, with dielectric functions of Al taken from [9]*

Accurate simulations will require the estimation of optical index of the materials. Especially for plasmonic devices the accurate determination of the optical index of the metal is critical since it is the main parameter defining the total optical loss of the device. In our devices, since we are using Cu as a metal electrode, we experimentally measure its optical dielectric constant by using ellipsometry technique. The details of the of Cu

fabrication are presented in chapter 3. Fig. 2.8 shows the dielectric functions, $\epsilon = \epsilon^{'} + i\epsilon^{''}$, for the fabricated Cu, together with dielectric functions of aluminum from Palik [9]. It is noted also that for Si, SiO_2 and Si_3N_4, TiN (main materials used in this thesis) we use the optical index data base of Palik [9].

2.2.2 Mode solver for planar MOS plasmon waveguides

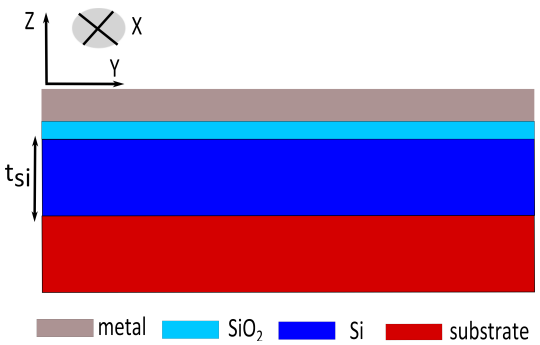

FIGURE 2.9 – *Generalized schematic of the semi-infnite metal-oxide-silicon-substrate waveguide.*

Having reliable and fast tools to extract the optical modes supported by a multilayer structure is crucial for the understanding of the optical behavior of our device. Furthermore, since we are interested to calculate optical modes at the cut-off regime, an analytical solution will be more accurate compared to the numerical ones. Therefore, an analytical optical mode solver is developed and is reported below.

The configuration of the investigated structure is shown in the figure 7.1 consists of copper-oxide-Si-substrate. The substrate can be either a metal or an insulator. We first look for solutions to the Maxwell equations for the geometry shown in figure 7.1. The type of solution that we are interesting in corresponds to wave propagation along a direction parallel to the boundary surfaces separating the different materials, which is define as the x direction. With z axis normal to these surfaces, we further assume that there is no y dependence of any of the fields. In our analysis we assume that the propagation constant is the same in all layers and also all the materials are non magnetic and so that the

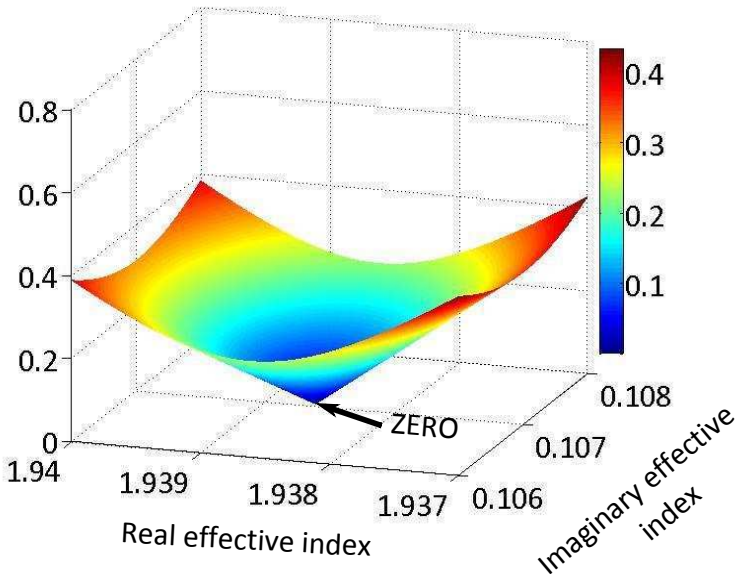

FIGURE 2.10 – *Numerical zero of the determinant estimated by MATLAB.*

magnetic permeability Îij has been taken equal to 1. Applying the appropriate boundary conditions of the fields, namely, the continuity of the tangential fields, the mode equation in the form of matrix is extracted (more details are reported in Appendix A).

To get non-trivial solutions, the determinant (G) needs to be zero, which leads to the mode equation. The complex root of the determinant was estimated numerically using matlab software (figure 2.10). The zero value of the determinant G corresponds to a certain value of the real and imaginary part of the effective index which corresponds to the solution of the eigenmode equation.

In order to validate our method we estimate the effective index of the photonic mode supported by the Ag-SiO_2(10 nm)-Si-Ag (plasMOStor [10]) structure and we compare our results (analytical calculation using MATLAB software) with that of other numerical methods such as FDTD, Finite Elements method (FEM from COMSOL) and RCWA. Fig. 2.11 presents the results of different silicon thickness. By comparing the semi-analytical method and FDTD simulations we observe maximum disagreement smaller than 10% in the whole range of Si thickness. Furthermore comparing the results extracted by our

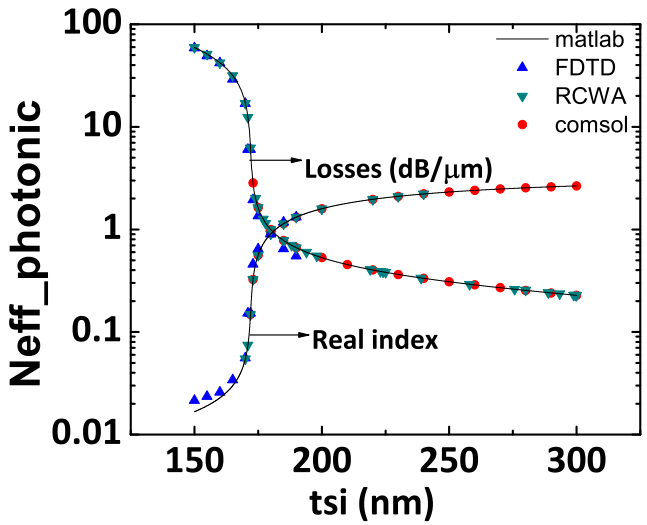

FIGURE 2.11 – *Mode effective index estimated using different methods*

method with that of the plasMOStor structure [10] we observe consistency (for example at t_{si}=170 nm). Finally, the semi analytical method showed considerable variation from the COMSOL simulations regarding the effective index of the mode in the region below the cut-off (weekly bound modes). We note that in this regime FEM method can not converge. This drawback was observed also by other researchers [70].

2.2.3 Finite Difference Time Domain (FDTD)

Finite-difference time-domain (FDTD) is a powerful method to model light-matter interactions in complex systems by solving the full set of MaxwellâĂŹs equations. In this thesis we use FDTD simulations, in order to investigate the optical behaviour plasmonic waveguides. In order to accurate model the optical behavior of plasmon devices (an example of a layout is presented in the inset figure) we set a non-uniform mesh with 2 nm in the region of low thickness and in the vicinity of metal/dielectric interfaces for x, y, z directions. Excluding the aforementioned regions, we use 50 nm mesh size for the rest of the device. Perfectly matched layer (PML) boundaries are used to attenuate

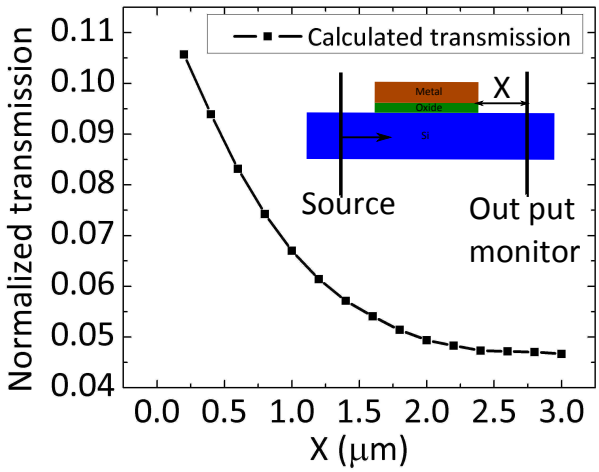

FIGURE 2.12 – *Transmission measurement for different position of the output monitor away from the metal interface of the plasmonic waveguide.*

the field without the back reflection at the simulation box boundary. The transverse distance between the PML and the device was chosen to be 2 μm. Finally, in order to measure the guided output power in a dielectric loaded plasmonic waveguide we position the transmission monitor at 2.4 μm away from the plasmonic device etch in order to avoid the scattered and radiated power of the device metal interface and consequently to measure only the guided power in the Si waveguide (Fig. 2.12).

2.3 Electrical and optical characterization methods

In the frame of this PhD, we develop in CEA/LETI an electro-optical characterization bench of copper based MOS modulator using a 200 mm wafer proper station (Fig. 9.3).

2.3.1 Coupling light from fiber to an SOI waveguide

Grating couplers are used in order to facilitate coupling between free-space radiation (propagate in the fibers) and guided modes. The fiber-grating coupling is placed at the

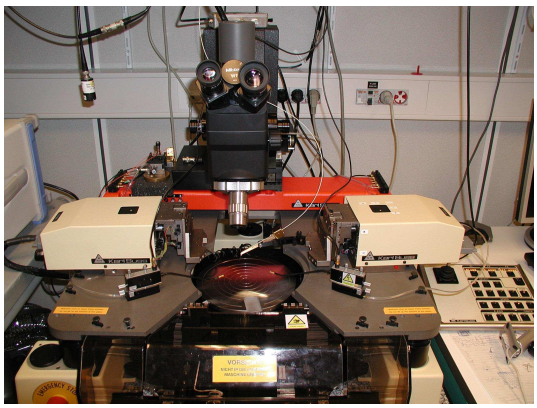

FIGURE 2.13 – *Picture of the developed EO experimental set-up.*

beginning and at the end of the device. The main advantage of using this coupling configuration is the possibility to excite a mode which may have the same dimension as a single SOI waveguide. Therefore the butt-coupling between the fiber and the grating is feasible and thus the wafer-scale testing of nanophotonic circuits is possible. In this thesis we used this property and we developed a wafer scale platform for investigating the EO behavior of our ultra-small (1 μm) devices.

2.3.2 Transmission measurement

Experimental transmission measurements are performed and these results are compared to the simulations to provide in depth understanding of the optical behavior of our device. Transmission measurement through our devices was performed using Light Emitting Device (LED) or LASER as an optical source of center wavelength of 1550 nm. The output power was coupled to the TM-polarized mode of the photonic waveguides through grating couplers using monomode fiber. The optical axis of the monomode fiber was fixed at an angle, 10°, with respect to the surface of the sample, optimized with respect to the period (950 nm), etch depth (70 nm) and duty cycle (50) of the gratings. This grating geometry allows to couple the fundamental TM mode. The TE mode is rejected by the couplers with a ratio more than 20 dB per one grating coupler. A multimode fiber is positioned at the output grating and the optical transmission measured through

the whole sample using an ANDO AQ2140 optical multimeter. Using multimode fibers ensures better collection efficiency of power from the device.

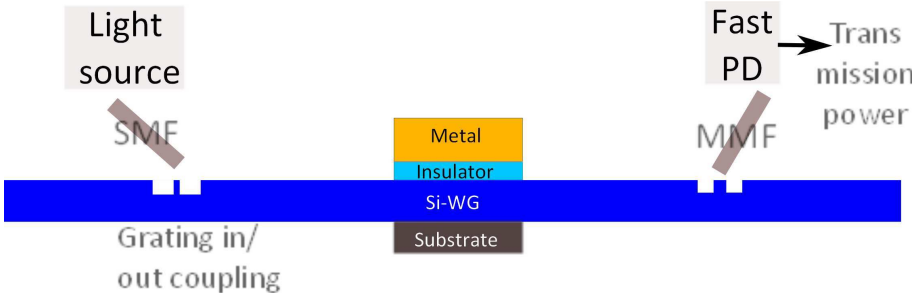

FIGURE 2.14 – *Experimental set up for measuring the transmission of the device.*

A KARL SUSS automatic wafer probe station was used to measure the samples on the wafer. The data was normalized with the optical transmission of a reference 220 nm × 500 nm silicon waveguide (SiWG) placed close to every group of 34 PWG samples. The output transmission is maximizing by performing automatic alignment at the reference waveguide. When the automatic alignment is completed we move automatic to the second, third, until the last device. After that we move again to a reference waveguide of other group of devices, starting first with the automatic alignment. This optimization technique is fast (more than 700 devices in 12 hours), and therefore is ideal for investigating devices which are fabricated by ultra large scale CMOS foundries. It is worth noting that the overall measured transmission through the investigated devices was very low, varying from 50 nW for the larger devices (7.4 μm length) to 1 μW for the shortest devices (1 μm length).

2.3.3 Electro-optical characterization

2.3.3.1 Low frequency measurements

A methodology for automated and reliable extraction of the low frequency modulation depth (1 kHz), optical transmission and leakage current under applied bias was implemented for wafer level testing.

The experimental setup is depicted in Fig. 2.15. A tunable laser and a light emitting device (LED) are both used to couple continuous wave (CW) optical signal inside the optical modulator. The optical sources are all interfaced with monomode fibers. The output power is collected with multimode fibers and transformed to electrical power through a low speed photodiode (below 10 kHz). Pre fiber alignment was used on a reference waveguides to maximize optical transmission. Finally the output signal is then measured using either a power meter when optical transmission measurement is performed or a lock in amplifier when the modulation depth is estimated.

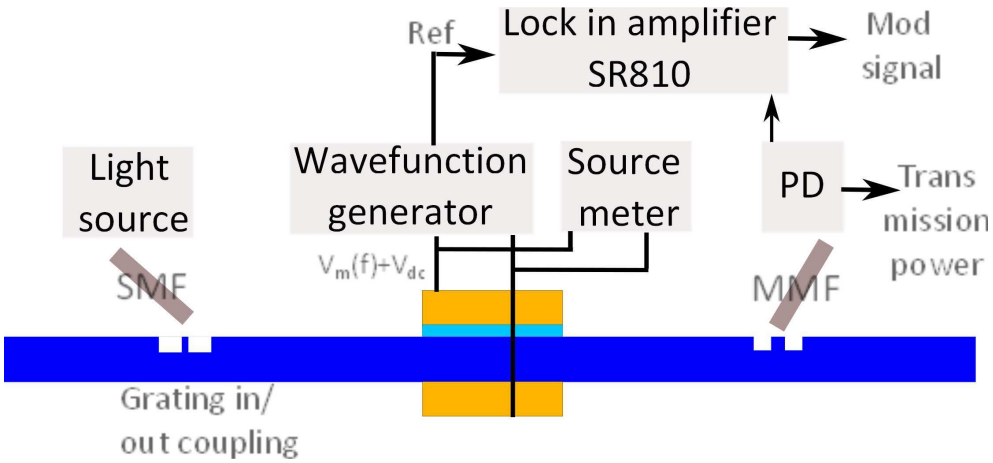

FIGURE 2.15 – *Experimental set up used for the wafer scale EO measurements at low frequency (below 10 kHz)*

A wave function signal generator is used to generate the modulating electrical signal. Its output is define by an ac signal $V_m(f)$ added with a constant dc value V_{dc}, such that the signal at the electrical input of the MOS plasmonic modulator is $V(f) = V_m(f) + V_{dc}$. The magnitude and frequency of the ac voltage are fixed for each measurement ; the magnitude of the dc voltage is swept in time. The purpose of the dc voltage bias is to allow sampling at different modes of operation of the MOS capacitor, namely accumulation, depletion and inversion. The ac voltage bias provides the modulated signal. Therefore the modulated intensity is extracted at different operation regions of the capacitor. The modulated signal is then measured by a lock in amplifier SR840 for frequencies up to

200 MHz. At that point, note that the use of a lock-in amplifier than a Telecom Network Analyser (TNA) was preferred in our case due to the following reasons : (a) The dc optical sensitivity of the internal photodetector of the TNA is -35 dBm (10^{-6}W) which is smaller than the dc output optical power of our device (see section 2.3.2) and (b) the TNA starts to measure the modulation for frequencies larger than 70 MHz much higher than the speed of our device.

It is worth noting that before of E.O testing, the dc leakage current for each device was measured through the source-meter, in order to make a fast scanning of the devices. Based on this measurements we exclude devices with leakage current larger than 10^{-9} A.μm^{-2} or equivalent 100 mA.cm^{-2} (Fig. 2.16(b)). This current density represent also the breakdown criterion used in section 2.1.3

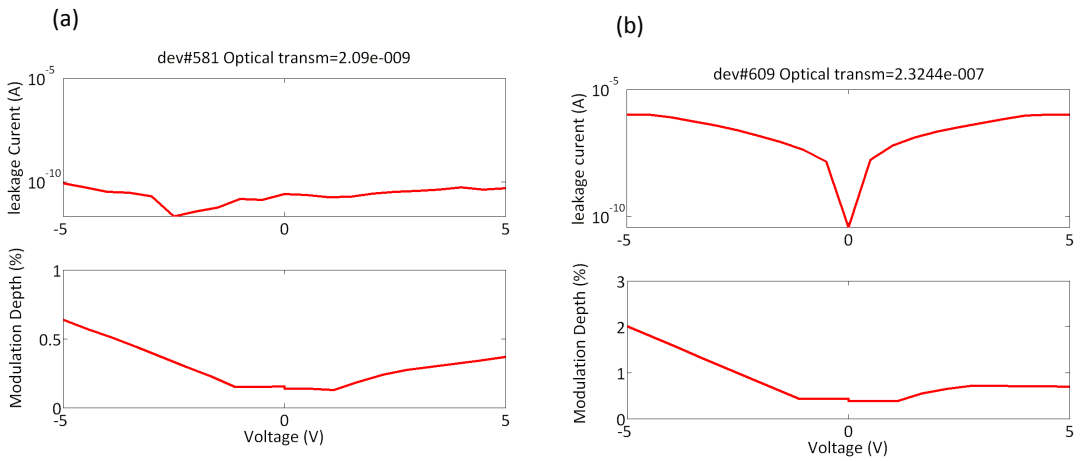

FIGURE 2.16 – *(a) A non leaky device of 1 μm^2 surface is measured with its modulation depth and transmission; (b) A leaky device of 5 μm^2 surface is measured with its modulation depth and transmission. This device will excluded from the analysis of the data.*

The modulated signal of the device (measured by lock-in amplifier in volts) was translated to modulation depth with the help of the internal modulator of the laser source which acts as reference. By switching the laser in modulated mode we perform 100% light modulation. The latter was transformed to voltage modulation through a

photodiode and finally measured by the lock in amplifier. By doing that we know the modulation intensity (measured by lock in amplifier) corresponds to 100% modulation for the reference structure (MI_{ref}). Therefore the modulation intensity of the device (MI_{dev}) can be calibrated to that of the reference and finally to extract its modulation depth (MD_{dev}) through the following relation :

$$MD_{dev} = \frac{MI_{dev}}{MI_{ref}} \tag{2.9}$$

2.3.3.2 High frequency measurements

The experimental set-up drawn in the Fig. 9.4 was used for measuring the dynamic response of our device in the frequency range from 50 kHz to 200 MHz (thanks to the use of lock in amplifier which operates up to 200 MHz in a frequency). A tunable laser is used to generate the CW optical signal. The light propagates via monomode fibers and couple to the on-chip device through optical gratings. The output power is collected with multimode fibers and transformed to electrical power through a high speed photodiode. Finally the output signal is measured using a lock in amplifier (SR 844) which is able to operates in a frequency range from 25 kHz to 200 MHz. A wave function signal generator (the same as for low frequency measurement), was used to generate the modulating electrical signal. This electrical signal is then propagated along the 50 Ω coax until it reaches the 50 Ω probe. The latter is finally contact the device. We use The reason of using the 50 Ω coax and 50 Ω probe is to avoid any impedance mismatch (which means additional electrical loss) between the wavefunction generator and the device.

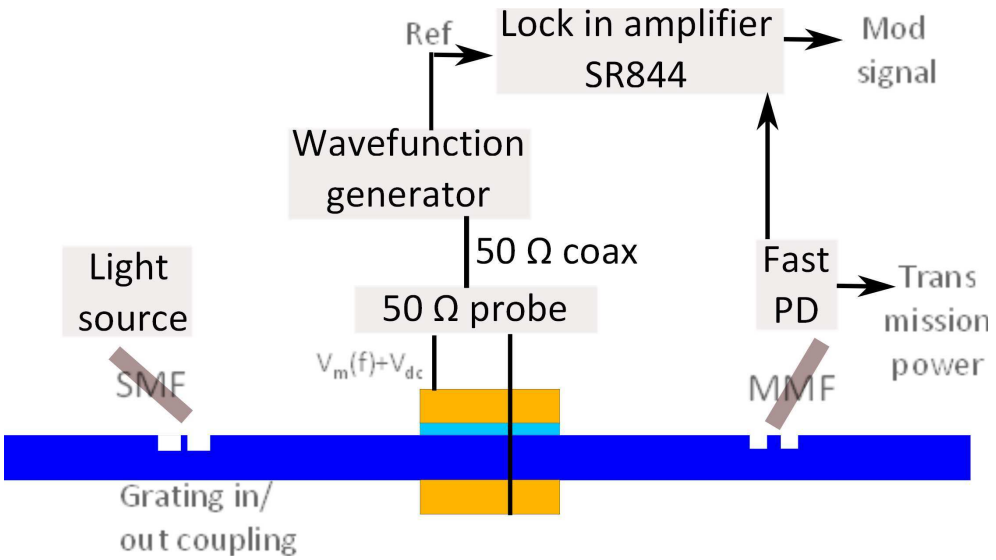

FIGURE 2.17 – *Experimental set up used for measuring the bandwidth of the device (up to 200 MHz)*

Chapitre 3

CMOS Integration of MOS Plasmonic Modulator

As discussed in the introduction, the aim of this thesis is to integrate the plasMOStor [10] design within the CMOS environment. However, this design does not fulfil the requirements of CMOS compatibility because they use silver as a metal electrode, which is contaminant within the CMOS environment, and also no considerations have been done regarding the interfacial layer between the metal and the insulator or semiconductor. Therefore, the risk of using such design (see Fig. 3.1) within the CMOS foundries, is to fabricate devices with detrimental effects on the fabrication yield, a high leakage current through the MOS insulating barrier and electrostatic breakdown during operation [71]. In this chapter we investigate the material aspects and also the technological steps required in order to realize an integrated plasMOStor compatible with requirements of CMOS technology. In particular we investigate both the choice of metal and the interfacial layer in terms of CMOS compatibility, low optical loss and high electrical reliable devices. Finally, in order to realize the vertical design of plasmostor with metallization on both sides of the device, we implement the direct bonding technique.

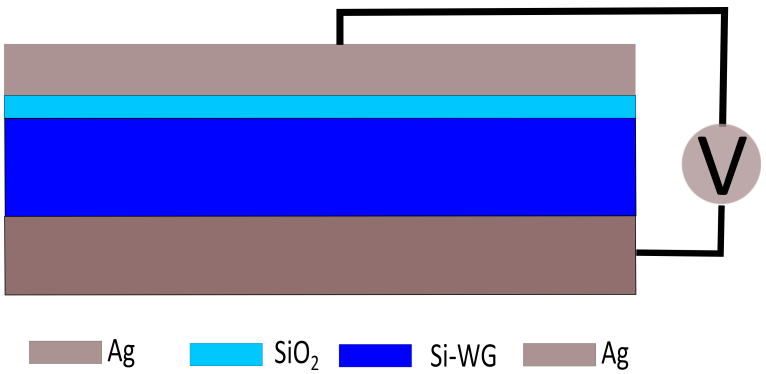

FIGURE 3.1 – *Plasmostor design [10] with silver as a metal electrode and without any consideration about interfacial layer between the metal and insulator or semiconductor.*

3.1 Choice of materials

The main constraints related with material aspects comes from the need for electrical contacts and interfacial layers in order to ensure high electrical reliability devices with low plasmonic losses. These properties were investigated in a plasmonic MOS waveguide, in the perspective of the integrated fabrication within a CMOS foundry. A careful choice of materials for the plasmonic metal and the interfacial layers was done and will be discussed in this chapter.

As regards to the metal choice we decide to use Cu as a metal electrode and the reasons of this choice are analysed in section 3.1.1. Electrical reliability issue raised by this metal choice is solved thanks to the insertion of an ultrathin nitride diffusion barrier layer between the gate metal and the oxide (section 3.1.2). Experimental investigation of this MNOS (Metal-Nitride-Oxide-Silicon) stack is performed by monitoring electrical breakdown under voltage stress of capacitances, and optical transmission experiments through a CMOS integrated MNOS Plasmonic Waveguide.

3.1.1 Choice of Cu for CMOS plasmonics

Plasmonic losses are highly dependent on the electric field penetration in the metal, therefore the nature and crystalline quality of the latter are critical technological issues.

For this reason, several proposed active and passive plasmonic devices [10, 72, 73, 74] use metals such as Ag and Au. However, these materials are not a good choice for a fabrication on a silicon CMOS platform, as they are well known contaminants of MOS devices. Conversely, metals such as Al and Cu are widely used in CMOS foundries, but have been much less studied for plasmon devices [54, 55]. Fig. 3.2 shows the propagation losses of a plasmon propagating at a metal-air interface, as a function of free space wavelength, for both Al and Cu. It was calculated by using the formula $\alpha_{SP} = \frac{1}{4.3 \times L_{SP}} = \frac{2\pi}{4.3 \times \lambda_0} \sqrt{\frac{\epsilon}{1+\epsilon}}$, where α_{SP} is the propagation loss (in dB/μm), L_{SP} the propagation length of the plasmon mode, ϵ the dielectric constant of the metal, and λ_0 the free space wavelength. For the calculation, we used the dielectric constant of copper which we measured by ellipsometry [55], or the dielectric constant of aluminium given by Palik [9]. It has recently been demonstrated [55] that the optical losses of plasmon propagating at the surface of Cu layers prepared in CMOS foundries was low and in agreement with the ellispometry results. From this simple comparison, we conclude that copper is the best choice for plasmonic devices in terms of optical losses. It is also technologically relevant, as Al has been progressively replaced by Cu in nowadays electrical interconnects [75]. Cu is therefore the most promising metal for the integration of plasmon devices in a CMOS environment, and will be considered below as a metallization of the MOS waveguide. However, choosing Cu as a metal electrode we have to be careful about the choice of the interfacial layer between the copper and insulator or semiconductor. In the following section, we demonstrate the use of thin Si_3N_4 as an efficient and low optical loss diffusion barrier of copper.

3.1.2 Choice of diffusion barrier

The most widespread Cu diffusion barrier used for electrical interconnects are currently chosen between the following materials : Ti, TiN, Ta, TaN, W, Pd [76, 56, 77]. As being conductive and low thickness diffusion barriers, they can fullfill the needs of electronics applications. However they are optically very lossy, so that they are not suited for CMOS plasmonics devices (Table 3.1) : we calculate that the plasmonic mode losses

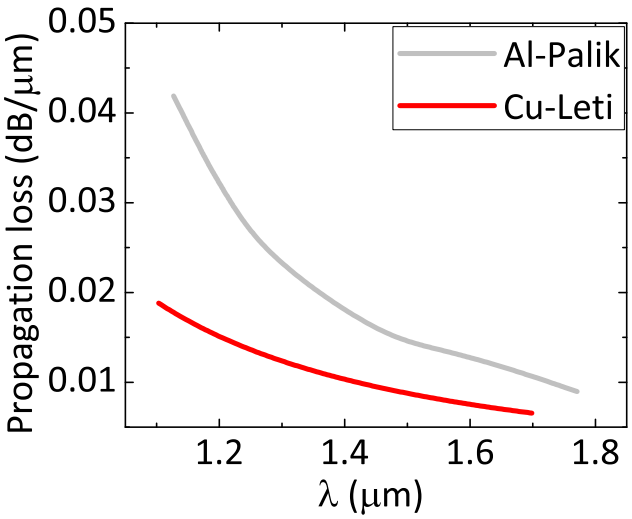

FIGURE 3.2 – *Plasmon propagation losses induced by Cu and Al along a metal/dielectric interface for different wavelengths.*

increase up to 15 times compared to the barrierless case. Ta having a better performances than the others, the plasmonic mode losses are increased by a factor of only 5, but its barrier effect is lower than for the other, eg requiring more thickness than considered in Table 3.1 to reach the same level of reliability.

TABLE 3.1 – Plasmonic MOS mode losses for different diffusion barriers at a wavelength of 1.55 μm. The operation voltage for constant electrical performance is also presented.

Diffusion Barriers	without barrier	Ta	TaN	Ti	TiN	Si_3N_4 (25 nm)	Si_3N_4 (3 nm)
Plasmonic losses ($dB/\mu m$)	0.29	1	3.3	3	3.61	0.2	0.31
Operation voltage (V)	3.5	4	4	4	4	33	4

The electrical interconnect literature also considered alternative insulating materials, including silicon nitrides, as a diffusion barrier. For example, T.C. Wang et al [78] investi-

gated 50 nm thick SiN, SiCN, SiCO layers deposited by PECVD as a Cu diffusion barrier. Both SiCN and SiCO demonstrated a poor adhesion on copper, leading to integration problems. On the contrary, SiN showed a good diffusion-barrier performance as well as good adhesion with copper. However, only non stoechiometric nitride are considered in the previous works (see also [79, 80]), because of limited thermal budget used for back end processes. Our motivation is different, as we need the thinnest possible dielectric diffusion barrier in a front end MOS device, for which the operating voltage and the energy consumption scale with the thickness of the insulating barrier. For example, a MIS electro-optical device [81] is a capacitance-operated device, where its performance depends on the charge density of the accumulated layer :

$$\Delta N_e = \frac{C_{ox}}{t}[V_g - V_{fb}] \tag{3.1}$$

where C_{ox} is the oxide capacitance, V_g is the applied voltage, V_{fb} is the flat band voltage and t the effective charge layer thickness. For a given level of performance (density of accumulated charges and so magnitude of modulation depth for a modulator) a thinner oxide thickness is needed in order to achieve low operation voltage and hence lower energy consumption. In Table 3.1, we see that despite lower optical losses can be reached, typical operating voltage of the MNOS stack using 25 nm SiN is much higher than in the barrier less case. To improve that figure, we propose to use thin stoichiometric Si_3N_4, which is available in front end CMOS processes. Note that Si_3N_4 should not be used alone as a gate dielectric as its interface with Si remains worse than the Si/SiO2 interface in terms of density of interface traps [82].

We are therefore promoting an hybrid Metal Nitride-Oxide-Silicon (MNOS) stack for active CMOS plasmonics. That stack with highly doped silicon as a metal has already been extensively studied in microelectronics for highly reliable and aggressively scaled transistors [83]. However, reliability of such stack was never investigated when Cu is the gate metal, as required for CMOS plasmonics devices. We experimentally demonstrate below that an ultrathin (3 nm) stoichiometric Si_3N_4 can fulfill the above requirements for diffusion barrier in MOS based optoelectronics devices using plasmons and provide

high reliability performances.

3.2 Improved electrical reliability of Cu based MNOS stack

Electrical investigation is the most sensitive technique to identify the effect of copper diffusion to the insulator or semiconductor [16]. Hence the detailed electrical investigation of a Cu gate MOS capacitor is presented below. In order to validate the use of very thin Si_3N_4 as a diffusion barrier for copper, we fabricated copper gate MNOS and MOS capacitors on 200 mm silicon wafers on the Leti fabrication line. The silicon wafers are p-doped with $4x10^{18}$ boron cm^{-3} (Fig. 3.3(a)). A damascene patterning technique [84] was used in order to fabricate the metal gate electrode of the capacitors. An 800 nm thick thermal oxide is first deposited on the silicon wafers (Fig. 3.3(b)). A cavity is subsequently drilled into the oxide layer by a lithography step followed by dry and wet etching steps (Fig. 3.3(c)). Wet etching allows cleaning of the Si interface before the fabrication of the gate dielectric stack. After etching, a 10nm thermal oxide (t-SiO_2) layer is formed by thermal annealing (Fig. 3.3(d)). Except for reference purposes, wafers were then submitted to a deposition via LPCVD of a stoichiometric silicon nitride Si_3N_4 layer on top of the oxide (Fig. 3.3(e)). A copper layer is then deposited by a combination of the PVD and Electro Chemical Deposition (ECD) and polished by Chemical Mechanical Polishing (CMP) [15]. Finally, an Al contact is fabricated on top of copper electrode, followed by thermal stress at 400 °C (Fig. 3.3(f)) to simulate the typical thermal budget of a backend process.

C-V measurement were automatically conducted using the experimental set-up detailed in chapter 2. The Fig. 3.4 shows a typical example of C-V characteristics of a MOS and a MNOS stack. Both the accumulation and the depletion regimes can be distinguished. The inversion regime is not observed at positive voltages because the voltage sweep frequency is too high to allow the diffusion of minority carriers. These C-V experimental curves were nicely fitted accordingly to the model described in section 2. This allows the extraction of the equivalent oxide thickness (EOT) and flat band voltage V_{fb} (Table

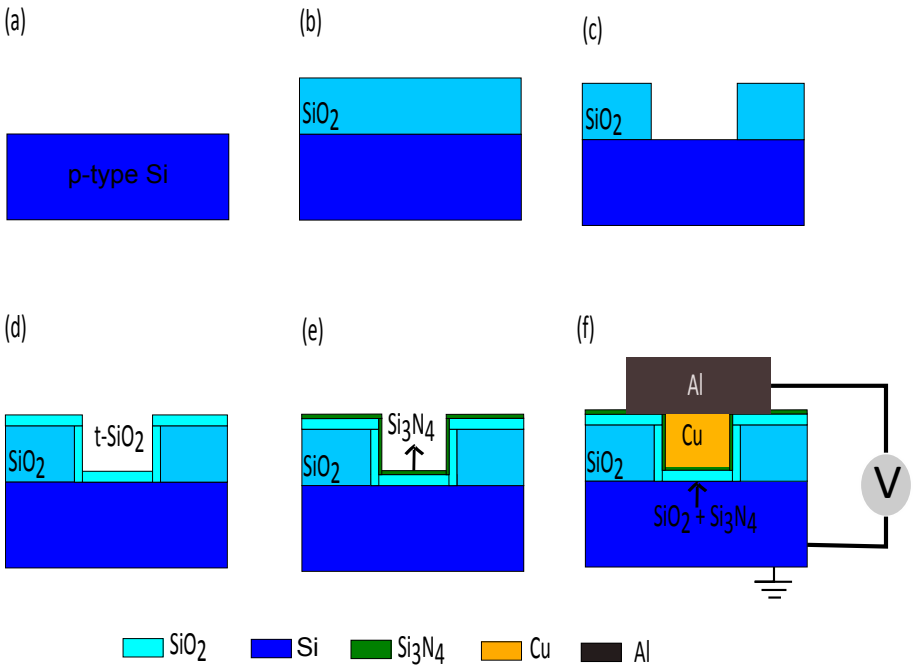

FIGURE 3.3 – *Fabrication process of MOS capacitors using standard CMOS technology.*

3.2). Note that the inversion regime is observed in the simulation due to the equilibrium assumption. The EOT for both gate stacks are fully in agreement with the dielectric constant of the insulators used [85], thanks to the quantum corrections of the C-V model. No hysteresis of the C-V curve is observed, indicating that no slow trapping of charge occurs in the silicon nitride and/or in the oxide barrier. However a negative voltage shift of the flat band voltage is observed after the introduction of the nitride in the stack, that is commonly attributed to the increased negative fixed charge contained in the silicon nitride layer [86].

TABLE 3.2 – EOT and V_{fb} of given MOS stack layer, extracted by fitting to C-V measurements. Values are averaged out of 10 different devices, for each gate stack.

MOS description	EOT (nm)	V_{fb} (V)
Cu/SiO_2 (10 nm)/Si	10	-1.32
Cu/Si_3N_4 (3 nm)/SiO_2 (10 nm)/Si	11.7	-1.7

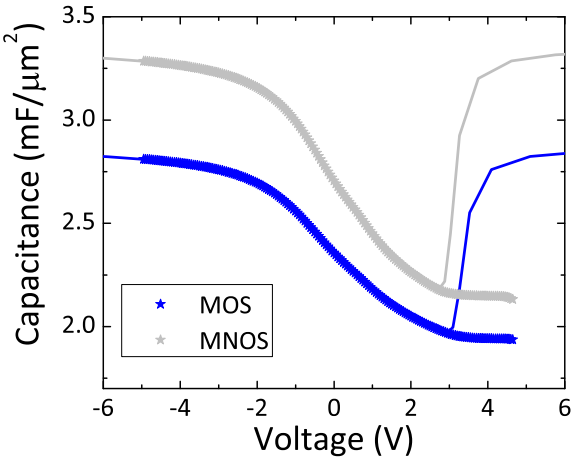

FIGURE 3.4 – *C-V characteristic of MOS capacitor at 100 kHz voltage sweep frequency, for a singe oxide (MOS, black symbol) and an oxide/nitride barrier (MNOS, blue symbol). The corresponding quantum simulation of the curve is also shown (Black and blue line), following the model presented in the section 2.*

Copper mainly impacts the reliability of the MOS capacitance. The latter is conveniently assessed by the measurement of the electric field at breakdown, using a conventional Linear Ramp Voltage Stress (LRVS) technique with a speed of voltage ramp of 0.5 $V.s^{-1}$, the criterion of break down being chosen at a critical gate current of 0.1 $A.cm^{-2}$. Fig. 9.5(a) shows the Weibull plot of the fabricated capacitors (surface of 10000 μm^2) versus the equivalent oxide field to break down ($(V_g - V_{fb})/EOT$), where we used the EOT and V_{fb} extracted from the C-V fit. MOS Capacitors exhibit extrinsic break down characteristics, with early failure behaviour (E < 1 MV.cm-1) occurring for 40% of the devices. Conversely, 95% of MNOS capacitors using an additionnal thin stoichiometric Si_3N_4 have a breakdown field higher than 10 $MV.cm^{-1}$, with no sign of extrinsic behavior. Extrinsic break down failure is commonly associated with point defects inside the insulator [58], which in our case can originate from the diffusion of Cu within the oxide [16, 87]. We therefore checked that assumption by performing Secondary Ion Mass Spec-

troscopy (SIMS) on both the oxide and the oxide/nitride barriers (Fig. 9.5(b)). SIMS measurements were performed on same capacitance structures, used for electrical test. Measurement was performed from the rear side, by locally removing the silicon of the wafer thanks to a TMAH solution. Analysis was performed by a 45 keV O-ion-beam bombardment at an angle of 45°, down to the underlying Cu layer. The analysis of the copper concentration in the MNOS and MOS structures puts in evidence a one order of magnitude lower Cu concentration in the oxide of the MNOS compared to the MOS case. This observation is consistent with previous observations from the literature about stoechiometric Si_3N_4 [79]. The Si_3N_4 layer hence allows lowering the concentration of Cu in the barrier, therefore strengthening the resistance of the MOS stack to the electric field.

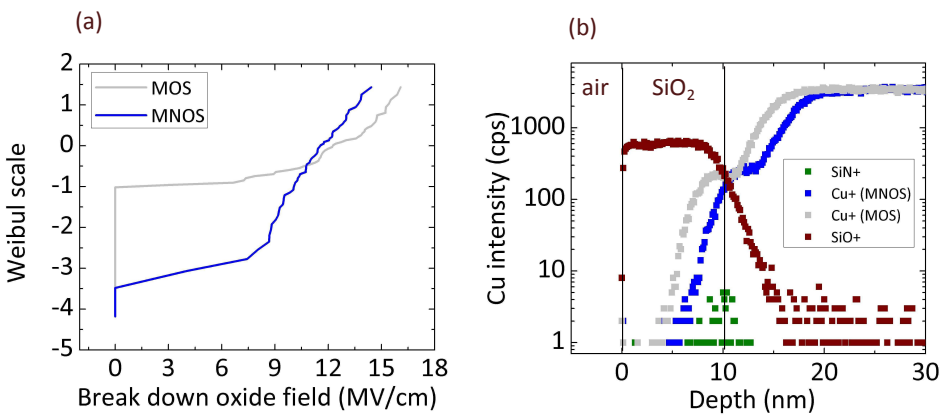

FIGURE 3.5 – *(a) Experimental reliability plot (in Weibul scale) of the break down field ;(b) SIMS measurement of depth profile of Copper intensity for MOS and MNOS multilayer insulator*

In order to further corroborate the quality of the insulating stack of the investigated structures, we estimate the interface defect density D_{it} using the standard conductance method developed by Nicollian and Goetzberger [88]. This technique is already described in section 2. The extraction of the D_{it} at different energies, requires to know the capacitance (C-V) and the conductance (G-V) of the devices at different frequencies (in

this study ranging from 1 kHz to 1 MHz). Fig. 3.6(a) shows an example of the measured conductance as a function of the voltage at 100 kHz for the MOS and MNOS devices. This measurement shows a peak at the depletion voltage region which is correlated with interface defects with a specific energy inside the Si band gap [89]. The extracted interface defect density (D_{it}) for different energies is shown in the Fig. 3.6b. First, both structures display a D_{it} peak around 0.35 eV above the valence band edge. This feature is already mentioned in the literature and it has been attributed to the copper-induced mid-gap interface states [90, 16]. Second, we can observe that, for the MNOS devices the defect density reduced up to 30% compared to the MOS structure suggesting that the Si_3N_4 plays a key role to limit the copper diffusion. Indeed these results are consistent with the reliability measurements.

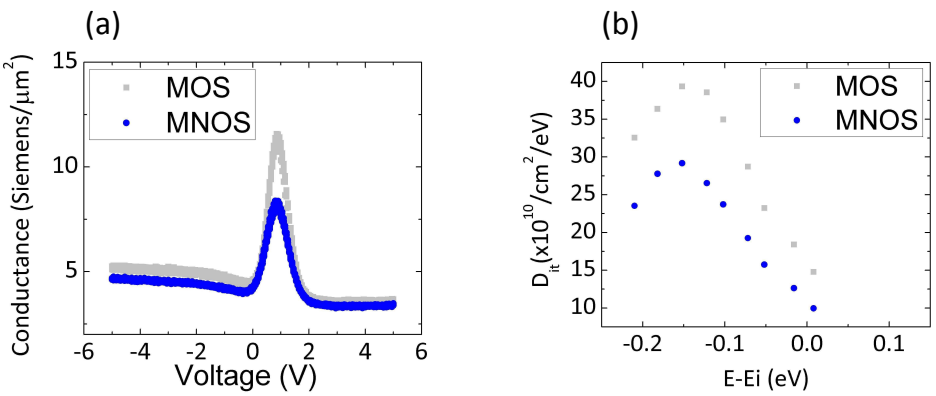

FIGURE 3.6 – *(a) G-V characteristic of studied capacitor at 100 kHz voltage sweep frequency, for a single oxide (MOS, black symbol) and an oxide/nitride stack (MNOS, blue symbol) ;(b) Defect density, D_{it} at different energies in the Si bandgap for a singe oxide (black symbol) and an oxide/nitride stack (blue symbol).*

The conduction mechanism of our devices was also investigated by measuring the DC leakage current for low voltages up to -5 V (Fig. 3.7). For the investigated structures (MOS and MNOS) we observe two populations of devices with different I-V : (a) the devices showing an ohmic like conduction ; (b) the devices showing an enhanced conduction starting from -3.5 V. The latter is observed for 40% and 10% of the MOS and MNOS de-

vices respectively. These values are consistent with the population of the devices showing extrinsic voltage break down failure characteristics (Fig. 9.5(a)), suggesting that devices with higher defect densities (and so enhanced conduction) are more prone to break down.

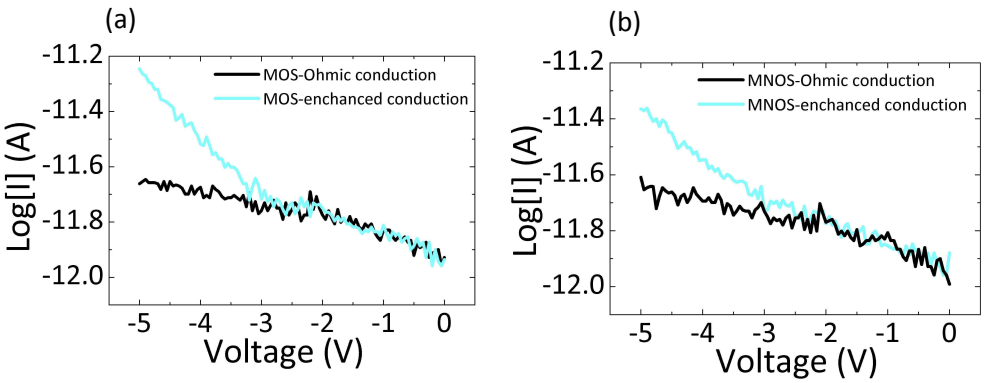

FIGURE 3.7 – *Example of leakage currents as a function of the applied voltage for (a) MOS and (b) MNOS multilayer insulator, showing the two different population with just ohmic conduction and the enhanced conduction starting from -3.5 V*

The leakage current at low fields can be attributed to ohmic conduction mechanism [68]. To identify the conduction mechanism for the higher slope regime, we check the dependence of current (I) on electric field (E) for two main transport tunnelling mechanism, namely Fowler Nordheim (FN) tunneling and Poole-Frenkel (PF) emission. Using

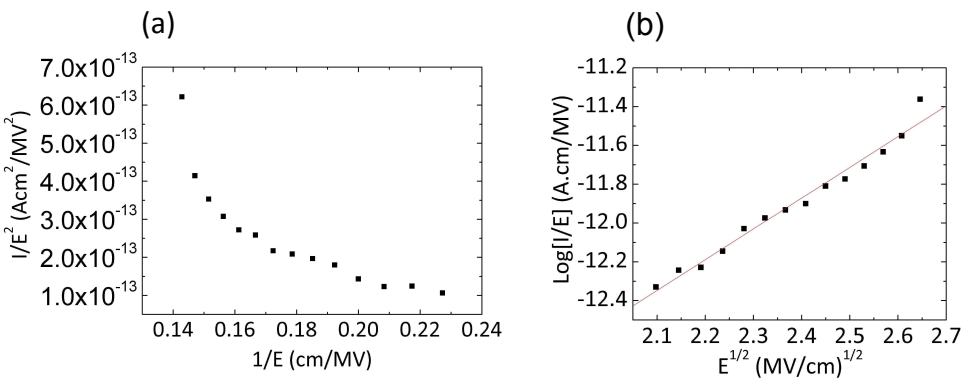

FIGURE 3.8 – *Leakage current in a (a) FN plot and (b) FP plot.*

the F-N plot (I/E^2 as a function of $1/E$) [68] was observed a non linear fit (Fig. 3.8(a)) which implies that it is not the right conduction mechanism for our investigated devices. The conduction mechanism of the dominant leakage is closer to Poole-Frenkel (PF) emission since the I-V curve shows linear dependence as a function of the $V^{0.5}$ (Fig. 3.8(b)). This behavior is already observed by other researchers showing that Cu-induced leakage current was better fit to a Poole-Frenkel type mechanism [91, 92]. Further measurements, i.e. I-V at different temperature, would be nevertheless needed in order to definitely prove this hypothesis.

In conclusion, a MNOS stack can fulfill the requirement for highly electrically reliable structures, owing to efficient copper diffusion barrier induced by the thin Si_3N_4. This result is consistent with the demands of CMOS technology.

This aforementioned results was implemented to the fabrication of the integrated plasmonic modulator investigated in this thesis (see section 3.4 below).

3.3 Low optical loss Cu based MNOS stack

Transmission measurements of the coming out device from the gate metal fabrication phase (section 3.4.3), were performed using a fiber based 1.55 μm laser optical source. The used experimental set-up was described in the chapter 2. The data were normalized with the optical transmission of a reference 220 nm $\times$ 500 nm Si-WG placed close to every group of 34 PWG samples. Fig.9.6 displays the normalized transmission of about 1200 PWGs whose silicon thickness is 170 nm and the length L_{PWG} is varied between 2 and 7 μm. For each device length L_{PWG}, the transmitted power is measured for 18 identical PWGs taken at various positions on the wafer.

One indeed observes a decay of the transmission as L_{PWG} is increased. An exponential fit to the experimental data gives propagation losses of 0.39$\pm$0.02 dB.μm^{-1} and an insertion loss of 2.2 dB. The latter is extracted from the interception of the Normalized transmission at $L_{PWG} = 0mum$. These results are close to that of numerical calculations based on the picture of a direct butt coupling of the incoming fundamental

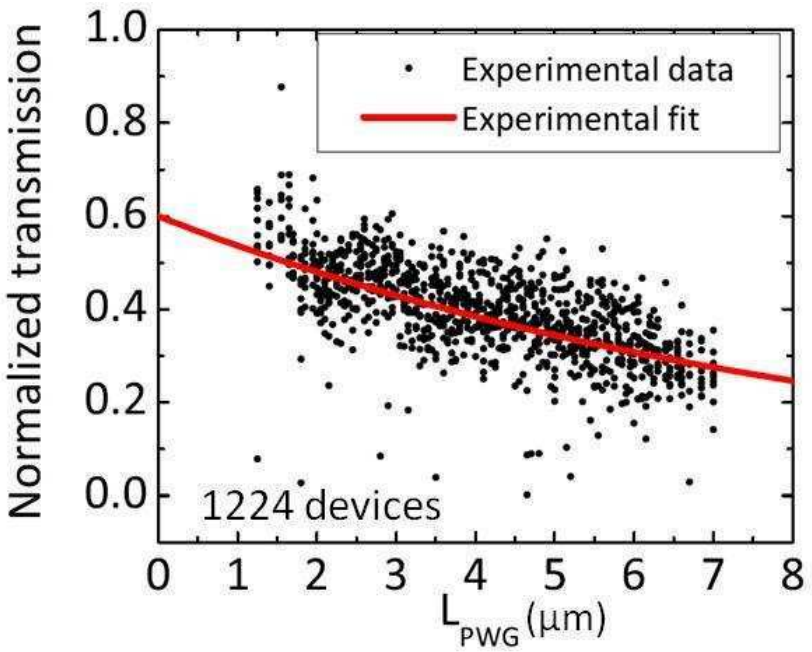

FIGURE 3.9 – *Normalized experimental transmission data as a function of the* L_{GATE}.

mode of the SiWG to the fundamental mode of the PWG. Using the optical constants of copper given in [55] (0.3+10.8i at 1.55 μm), and Si, SiO_2 and Si_3N_4 from palik, we found, using a modal analysis (Lumerical FDTD) that the fundamental plasmonic mode of the MNOS stack considered here has an effective index of n_{PWG}= 2.51 and propagation losses of 0.31 dB.μm^{-1}. Following direct coupling theory [93], the expected power transmission between the fundamental SiWG mode of effective index n_{SiWG}= 1.9 and the fundamental mode of the PWG is the product of Fresnel transmission coefficient $T_{fresnel} = \frac{4n_{PWG}n_{SiWG}}{(n_{PWG}+n_{SiWG})^2} = 0.98$ multiplied by the overlap integral of the corresponding mode fields (Fig 3.10(b)) which is calculated as 0.61. According to this simple calculation, we then expect an insertion loss of 4.3 dB. For comparison purpose, a 3D Lumerical Finite difference time domain (FDTD) simulation of the experiment was performed (Fig. 3.10(c)) using nominal geometry parameters for both PWG and SiWG, as well as the same optical data used for the modal analysis. An exponential fit of the calculated optical transmission data shows a propagation loss of 0.3 dB.μm^{-1} which is consistent with

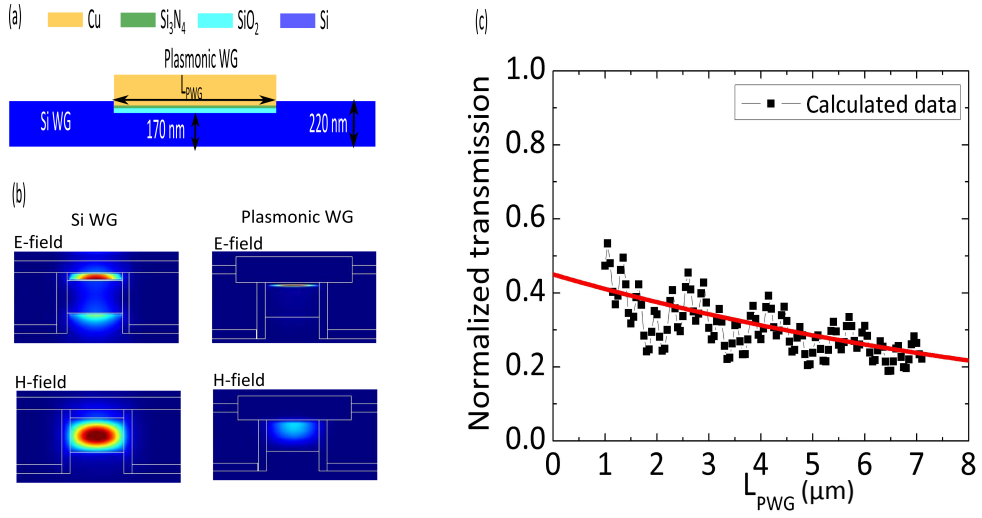

FIGURE 3.10 – *(a) Cross section in the propagation direction indicating the main components of the hybrid plasmonic WG ;(b) The E and H field intensity of the fundamental plasmonic mode is depicted for Cu-Si3N4 (barrier)-SiO_2-Si-SiO_2 structure taken from 3D mode analysis using FDTD ;(c) Calculated transission through the device by using 3D FDTD.*

the loss of the fundamental mode estimated by mode analysis. Furthermore an insertion loss of 4 dB was extracted which it is in agreement by the aforementioned picture of direct coupling. Finally, two oscillating features are observed. The short period (300 nm) feature is consistent with Fabry Perot oscillation of the fundamental plasmonic mode ($\lambda/(2 * 2.5) \approx 310nm$) within the PWG. Such FP oscillations could not be evidenced in the experimental data, because of the fabrication noise level. The long period feature is the result of two modes with different effective index. The beating period of 1.55 μm corresponds to an effective index difference of 1 for *lambda*=1.55 μm. This is very close to the difference of the effective index of the fundamental plasmonic mode, n_1=2.51, and the index of the mode supported by the side of the metal, propagating in the same direction, n_2=1.55 (Fig. 3.11).

The discrepancies between the experimental and the theoretical results may be at-

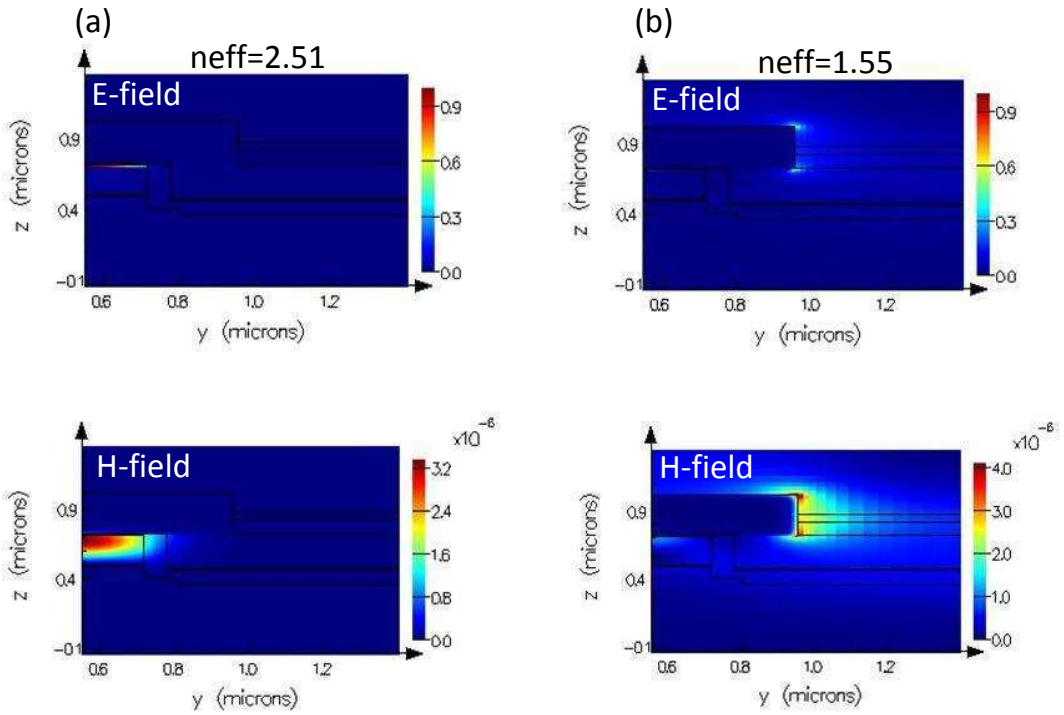

FIGURE 3.11 – *(a) E and H field of the fundamental plasmonic mode ; (b) E and H field of the mode supported in the side of the metal*

tributed to structural imperfections like slightly taperized PWG entrance due to some imperfectly etched edges, or metal surface roughness at the interface with oxide, and finally a possible difference in the optical indexes of the materials with respect to the values used in simulations.

3.4 Fabrication of an integrated plasMOStor

In this section we describe the main technological steps in order to fabricate the plasMOStor stack [10] integrated with a mono-mode Si waveguide using standard CMOS technology available on LETI platform. The key milestones of this fabrication are the following :

1. Fabrication of vertical Cu based MISM stack which satisfy the electrical, optical and material constraints of CMOS technology (i.e Cu as a metal electrode, Si_3N_4

as low optical loss diffusion barrier, limitation of the thickness of TiN in order to minimize the induced loss).

2. In-plane waveguide coupling in order to put light inside the plasMOStor. This gives the advantage of CMOS ultra large scale fabrication.
3. Direct bonding in order to fabricate the back contact.

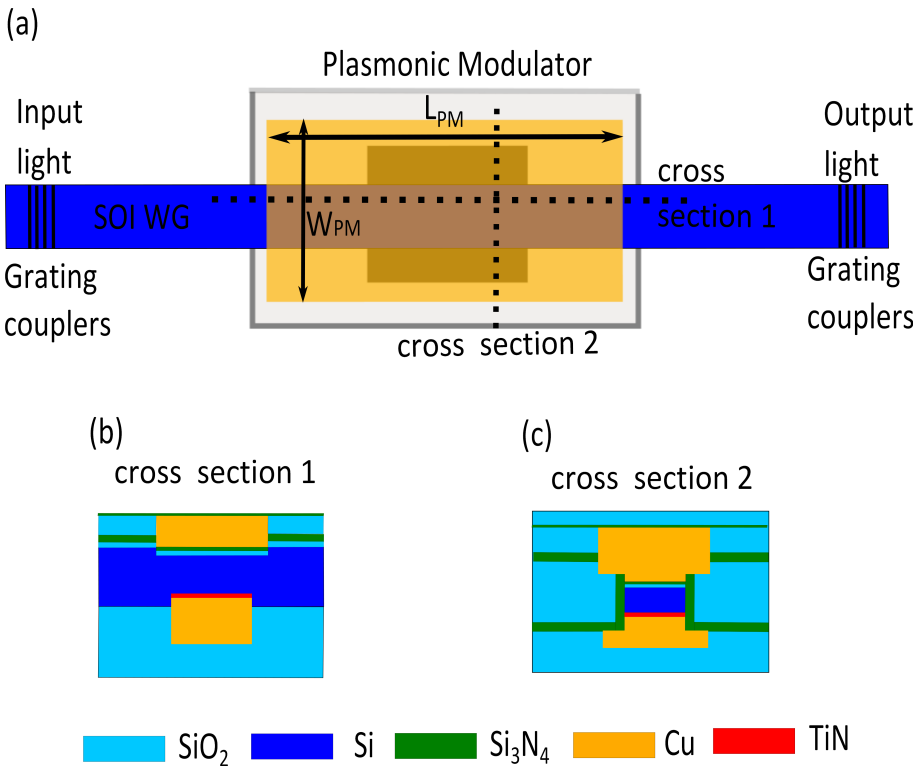

FIGURE 3.12 – *Schematic top view of the integrated plasmonic modulator (a) with different cross accordingly to different planes ; cross section in the direction of propagation (b) cross section in perpendicular direction (c).*

The structure of the integrated plasmonic modulator is shown schematically in Fig. 9.7. The device is fabricated on a silicon-on insulator (SOI) wafers, with SOI waveguide serving as the medium of propagating light. The light is coupled to the TM-polarized mode of the photonic waveguides through grating couplers. As the light propagates through the active region (plasMOStor), it couples into a plasmonic mode. Fig. 9.7(a)

shows a schematic top view of the integrated plasMOStor, with all the major components indicated. The plasMOStor consists of a metal-insulator-Si-metal waveguide where the back metal was fabricated by flipping and molecular bonding of the original SOI wafer on a Si carrier wafer. The active device area varies from 1 to 6 μm^2, 1 μm width and length varying from 1 μm to 6 μm.

The fabrication of these structures can be synthesized in five main phases (Fig. 3.13) :

1. The first phase ("Grating couplers") is used to design the grating couplers to couple light to SOI waveguide.
2. The second phase is ("Si-WG") to create the SOI Si waveguide which is required to couple light to the active region.
3. After that a metallization window is opened and the first electrical contact is made ("Gate metal")
4. After the formation of the first metal layer, the wafer is flipped and molecular bonded ("Back metal")
5. Finally we fabricate the electrical pad.

We will describe hereafter in details each single fabrication phase.

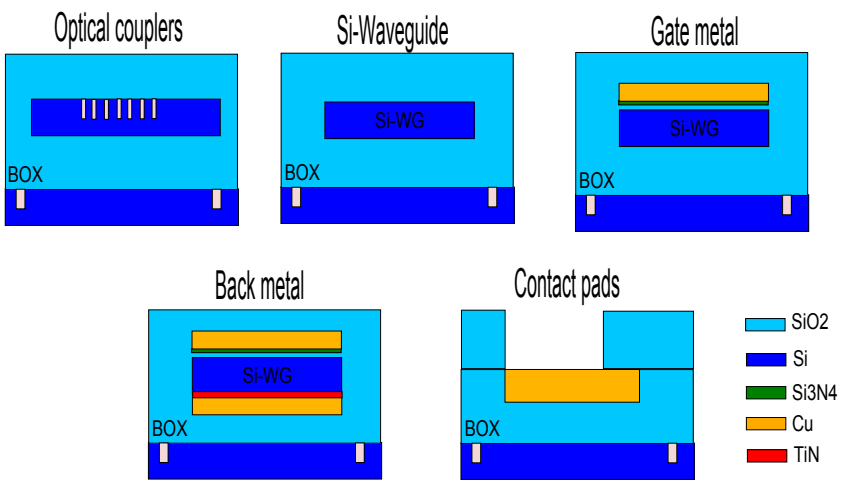

FIGURE 3.13 – *Schematic representation of the electro-optical plasmonic modulator after the 5 main fabrication phases.*

3.4.1 Grating optical couplers

In order to couple light between the fiber and the SOI WG we use grating couplers Fig. 3.14. The grating couplers are placed on the initial SOI wafer of a 220 nm Si layer on a 145 nm buried oxide (BOX) (Fig. 3.14(a)). At the level of grating, a DUV 193 nm optical lithography is followed by partial etching of the Si layer using the reactive ion etching step. In order to maximize the optical power inside the SOI waveguide we carefully design the optical couplers [94]. For a given wavelength λ and a coupling angle θ, the optimal grating period is given by the phase matching conditions :

$$k.\sin(\theta) + p\frac{2\pi}{\Lambda} = B \tag{3.2}$$

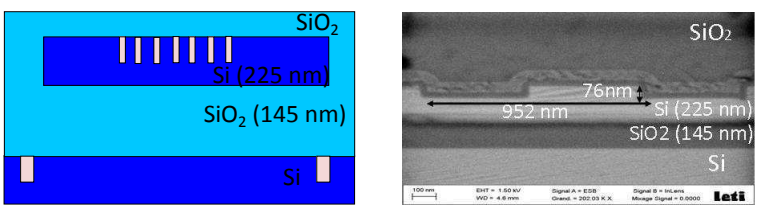

FIGURE 3.14 – *(a) Schematic diagram of the optical couplers ; (b) SEM cross section Fpicture of the couplers indicating the main dimensions of the critical components*

where k is the wave vector of the out coupled mode (k=$2\pi/\lambda$), p is the diffraction order, Λ is the grating period, B=$(2\pi/\lambda)n_{eff}$ is the real part of the propagation constant of the mode and n_{eff} is the real effective index of this mode. Based on our calculation, for a coupling angle of 10° the maximum coupling is given by the following set of parameters : lines of 12 μm in length, 0.475 μm in width with repetition of 0.950 μm Fig. 3.14 and etched in silicon with a depth of about 70 nm. This grating couplers was designed such as it is working efficiently in an upside down excitation configuration.

3.4.2 Si waveguide

In order to fabricate the Si-WG we use a mask whose layout it is comprised of three parts (Fig.3.15). The central part (Fig.3.15) consists of the Si PWG with varying lengths, L_{si}, from 1 to 6 μm with a step of 0.15 μm. The input and output side (Fig. 3.15) of

Si plasmonic wave guide, is coupled with a standard channel Si-WG of 220 nm × 500 nm. The silicon waveguide was created by photo-lithography and etching trough a 40 nm

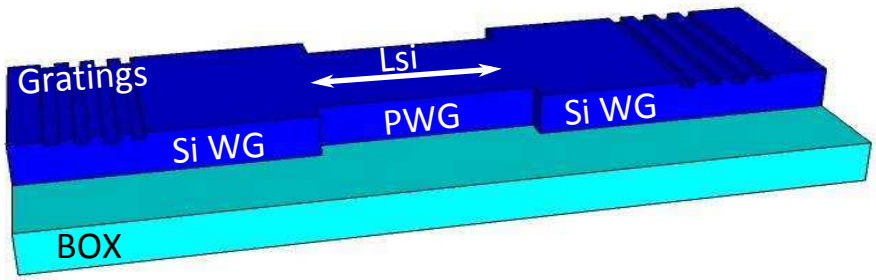

FIGURE 3.15 – *Si-WG coupled with the Si-PWG.*

thick thermal oxide hard mask (Fig. 3.16(b)). After that it was subsequently encapsulate by a conformal 60 nm thick Si_3N_4(by Low Pressure Chemical Vapor Deposition at 720 °C) followed by 800 nm SiO2 (TEOS LPCVD at 700 °C), Fig. 3.16(c)). Si_3N_4 plays two roles ; it was used as a diffusion barrier for the Cu in order to eliminate the short circuit and also as an etch stop when we etch through the encapsulation in the following steps.

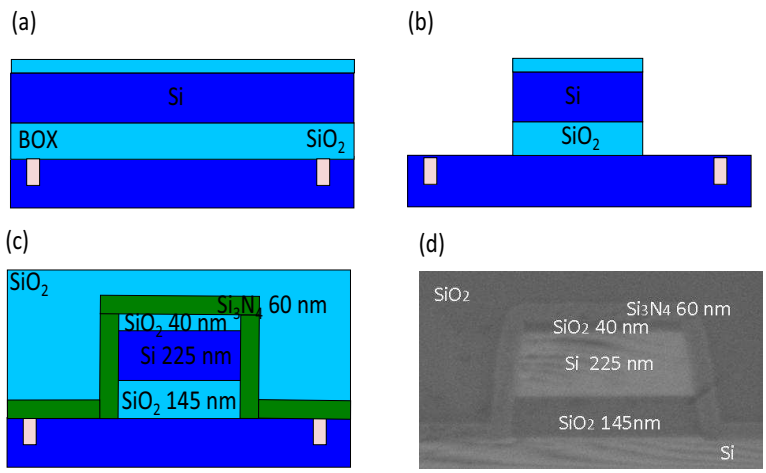

FIGURE 3.16 – *(a-c) Fabrication progress of silicon WG, using fully CMOS compatible technology ; (d) SEM image of the final Si-WG*

3.4.3 Gate metal

An other mask is used to create the metal gate of the MOS capacitor as well as the external electrical pad. Fig. 3.17 presents a top view of the whole structure. The gate metal is located at the level of the plasmonic modulator and it is a rectangular with length, L_{GATE}, and width of W_{GATE}= 0.8 μm. The electrical contact are square-shaped of 50 μm $\times$ 50 μm with voids inside in order to prevent the total etching of copper during the CMP process. The two areas are linked with an electrical contact of a width of W1=5μm, which is reduced up to W2=0.5 μm at the side of plasmostor to minimize the optical perturbation of the modulator. It is worth noting that since this device is a first proof of concept we decide to do not use the RF specific design (which is expensive and requires specific knowledge) for the electrodes.

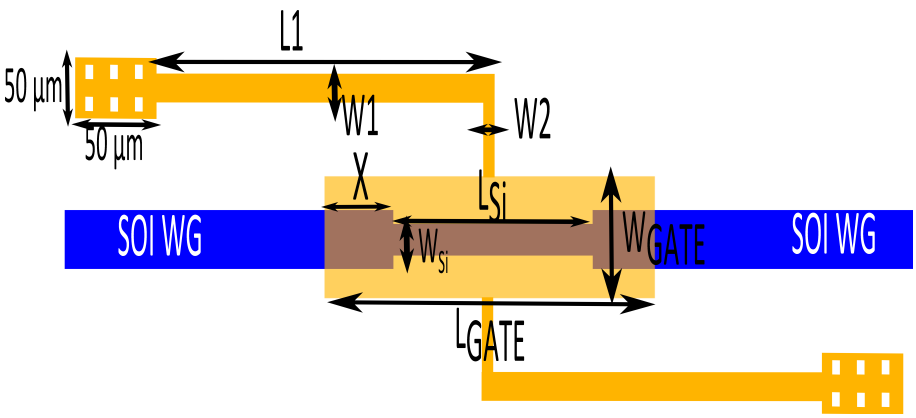

FIGURE 3.17 – *The gate metal phase comprise from the contact pad, the electrical links and the gate metal.*

Furthermore, the gate metal is center in the middle of the Si plasmonic waveguide (Fig. 3.17) and its length is given by the following equation : $L_{GATE} = L_{Si} + X$, where X = 0.2, 0.6, 1, 1.4 μm. We note also that the contact pad extends 34.6 μm from the Si waveguide in order to have enough space for the electro-optical characterization.

A detailed description of the fabrication of the metal gate is shown in the Fig. 3.18. After the fabrication of the Si-WG (Fig. 3.18(a)), the gate contact is patterned by damascene technique followed by dry and wet etching until Si waveguide. Wet etching is

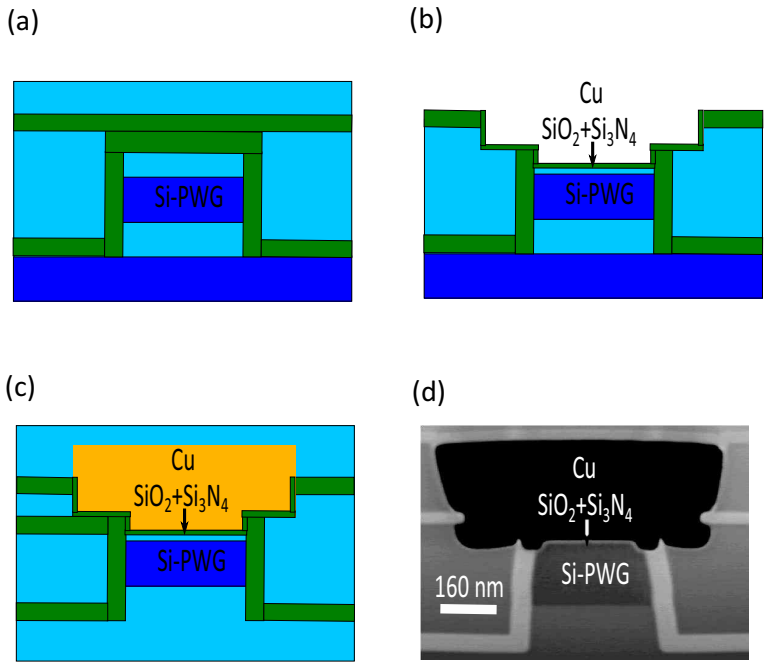

FIGURE 3.18 – *(a-c) Different fabrication phase of MNOS plasmonic WG ;(d) SEM image of the final PWG.*

performed in order to to avoid any dry etching of Si, and thus control the thickness of Si. Wet etching also allows achieving a clean and smooth Si interface before the fabrication of the gate stack. After etching of a cavity in the encapsulation down to the Si waveguide, the insulator gate stack is formed by 10 nm thermal oxidation and 3 nm Si_3N_4 deposition as a diffusion barrier (Fig. 3.18(b)) to Cu ; a very thick (1.5 μm) Cu layer is then deposited and polished by CMP after annealing. Annealing improves the Cu crystalline quality, and therefore leads to state of the art low optical SPP propagation losses. After that step the gate metal is encapsulated by Si_3N_4 and SiO_2. Finally, the wafer was transferred on a 2 μm oxidized carrier Si wafer by molecular bonding, and the Si substrate of the initial SOI wafer was removed by mechanical grinding and chemical etching down to the BOX. (Fig. 3.18(c)). A SEM cross section picture at that phase is presented in the Fig. 3.18(d).

Note, at that point, some of the wafers are extracted from the clean room and an optical validation of the MNOS stack was performed (see Fig. 9.6). This was an intermediate

stage before the full fabrication of the integrated plasmonic modulator. Measurements and results related to this optical validation are already reported in the section 3.3(see Fig. 9.6)

3.4.4 Back metal

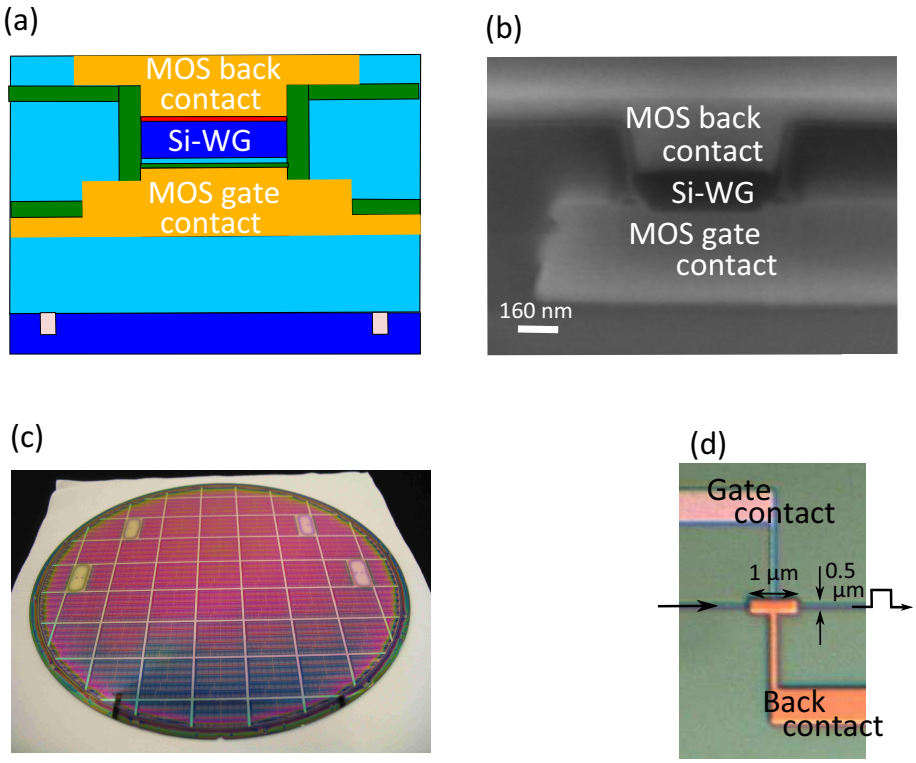

FIGURE 3.19 – *(a) Schematic and (b) SEM cross section of the final structure ; (c) Top view of 200 mm wafer including more than 30000 devices ;(d) binocular top view of single device indicating the important components ;*

After the validation of MNOS stack as a reliable and low optical loss plasmonic waveguide we continue to the fabrication of our plasmonic modulator [10] in vertically integrated channel configuration. At that point, the wafer-to-wafer direct bonding was performed at atmospheric pressure and room temperature, with μm-range control of wafer alignment and after chemical mechanical polishing (CMP) of SiO_2 surfaces. The bonded

wafer pair was subsequently annealed at 200 °C for 2 hours to convert hydrogen bonds into covalent bonds and increase the bonding energy. Finally, the back metal contact was fabricated on the flipped structure, using a Cu/TiN barrier scheme. The final structure is shown schematic in the Fig. 9.8(a), (b). Fig. 9.8(c) and Fig. 9.8(d) shows the top view of the 200 mm wafer and the single device respectively.

3.4.5 Electrical contact pads

We finalize the fabrication of the plasmonic modulator, with the fabrication of Al contact pads on the Cu lines. To do that, two lithography steps are used in order to create the cavity for the electrical pads which are square of $50\mu m \times 50\mu m$.

3.5 Conclusion

In this chapter we discuss the integration issues which face up with the fabrication of our plasmonic modulator. We proposed a MNOS stack for applications in electro-optical plasmonic devices, so that a very low optical losses and reliable operation is achieved. This objective is met thanks to a careful choice of materials, copper as a plasmon supporting metal and stoechiometric silicon nitride as a ultrathin diffusion barrier to the latter, and the use of fully CMOS compatible processes to integrate the MNOS plasmonic waveguide within silicon photonics circuitry. Final reliability is above 95% for a 3 nm thick Si_3N_4 layer, leakage current density below 10^{-8} A.cm^{-2} and optical losses as low as 0.4 dB.μm^{-1} for a 13 nm thick insulator barrier, in agreement with the Cu ellispometric data. Furthermore, we note that the MNOS stack was fabricated using the same fabrication process of the MNOS capacitance described in subsection 3.2. The damascene technique appears particularly well suited for a high quality PWG fabrication as (i) the patterning of the metal is achieved thanks to well mastered and standard oxide/nitride etching steps, (ii) it prevents the absorbing copper oxide formation [55] at the interface where plasmon mode are propagating, and (iii) it uses a high temperature annealing of the metal which favors high material quality and extremely low optical loss SPP propagation.

After demonstrating the MNOS as an appropriate structure for electo-optical CMOS plasmonics, we fabricate a vertical metal-insulator-Si-metal waveguide where the back metal was fabricated by flipping and molecular bonding of the original SOI wafer on a Si carrier wafer. The active device area varies from 0.5 to 3 μm^2, 0.5 μm wide and length varying from 1 to 6 μm. These results open the way towards the high performance and low cost fabrication of plasmonic active devices within CMOS foundries. The aforementioned development was applied in order to realize efficient plasmonic coupler (Chapter 4) as well as active electro-optical modulator (Chapter 5).

Chapitre 4

Efficient light coupling from Si-WG to integrated plasMOStor

In the previous chapter a hybrid plasmonic waveguide (PWG) is demonstrated by integrating the vertical Metal-Insulator-Si-Metal (MISM) PWG (refered as plasMOStor) with a conventional Si waveguide. Now the question that arises is : "How can we put light inside the integrated plasMOStor efficiently ?". This chapter seeks to answer this problem by proposing and experimentally demonstrating an efficient plasmonic coupler between the Si waveguide and the MISM plasmonic PWG. The whole structure is fabricated using the CMOS compatible process available at CEA-LETI. Three dimensional FDTD is also exploited in order to simulate our plasmonic couplers. The experimental and simulation results are in agreement illustrating that the highest-efficiency geometry corresponds to a compact coupler of 0.5 μm length having coupling loss of only 2.5 dB per coupler (experimental value).

4.1 Introduction

The MISM hybrid plasmonic waveguide (PWG) is of particular interest for CMOS active plasmonics because it allows the propagation of highly confined modes in the region of the insulator [10] and can potentially be integrated within Si-based electronics

foundries (chapter 3). However, such plasmonic structures suffers from both high material absorption loss (due to the high field confinement) and high coupling loss. The former can be addressed by material choices as it is already discussed in chapter 3. Considering the latter, we note that the sharp junction and the size mismatch between the standard Si-photonics WG and the MISM WG leads to detrimental losses [13]. Fig. 4.1(a) shows an example of such junction where the SOI-WG is butt coupled with the MISM PWG. When the incident mode (I) in the SOI-WG reaches the Si-WG/MISM junction some of the power is coupled to the MISM mode although it is observed that a part of it, is lost to reflection and scattering.

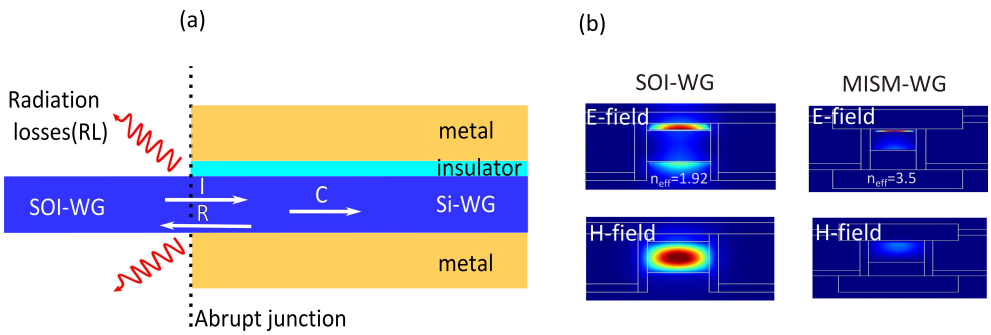

FIGURE 4.1 – *(a) Abrupt junction between the Si WG and a metal based waveguide ; (b) The E and H field intensity of the fundamental plasmonic mode supported in Si WG and MISM plasmonic WG taken from 3D mode analysis using FDTD*

Hereafter, the case of abrupt junction is investigated in detail. In particular, by using 3D FDTD simulation tools, we model a device where the SOI-WG is butt coupled with MISM plasmonic WG (Fig. 9.9 with an L_c=0). The detail description of such device is reported at the beginning of the section 4.3. We found that 14% of the initial power is reflected back into the SOI-WG mode propagating in the opposite direction (Fig. 4.6), while 55% of the initial power is scattered into unguided modes.

The results obtained by FDTD are compared with those extracted by considering the butt coupling approach in which the fundamental SiWG mode is direct coupled to the fundamental mode of the MISM plasmonic waveguide. In this case, the power coupling

efficiency (c_t) between two waveguides with different mode effective index and fields amplitudes is the product of the overlap integrals between the fields of the input and the coupled mode, multiply by the Fresnel transmission coefficient [95, 93] :

$$c_t = [\frac{4\beta_I\beta_C}{(\beta_I+\beta_C)^2}] \times Re[\frac{\iint\limits_{\Omega} E_I \times H_C^* \,\mathrm{d}\Omega \iint\limits_{\Omega} E_C \times H_I^* \,\mathrm{d}\Omega}{\iint\limits_{\Omega} E_C \times H_C^* \,\mathrm{d}\Omega)}] \times \frac{1}{Re(\iint\limits_{\Omega} E_I \times H_I^* \,\mathrm{d}\Omega)} \quad (4.1)$$

where β_I and β_C are the propagation constant of the incident and coupled mode respectively, E_C and H_C are the electric and magnetic field of the coupled mode respectively and E_I and H_I are the electric and magnetic field of the incident mode (Fig. 4.1(b)). Based on this model, the expected reflected power between the fundamental SiWG mode and the fundamental mode of the MISM PWG is given by the Fresnell coefficient $R_{fresnel} = [(n_I - n_C)/(n_I + n_C)]^2 = [(\Delta n/(n_I + n_C))]^2 = 0.09$. Moreover the overlap integral (Eq. 4.1) of the corresponding mode fields (4.1(b)) was found as $\Omega = 0.49$. Then the coupling loss per coupler (k_c) is given by $k_c = -10log \times [(1 - R_{fresnel}) \times \Omega] = 3.49dB/coupler$ which is close to that found from 3D FDTD transmission calculation (see Fig. 4.14).

Therefore the direct coupling of SOI-WG to MISM PW leads to high coupling loss. The solutions to that problem are reported in the following section.

4.2 Review of plasmonic coupler structure

In order to enhance the coupling of light from a Si-WG to a PWG, we have to maximize the mode overlap of incident mode with that of coupled mode and also to minimize the momentum mismatch between these modes. To that respect, several coupling configurations have been used in the literature, including butt couplers, taper couplers and directional couplers and are briefly described below.

Directional coupling has been proved to be an efficient way to couple light from a Si waveguide to a PWG [11, 96, 97, 98, 99]. The theory and the operation principle of directional coupling between two waveguides are well known [100]. One of the issue when designing an efficient directional coupling system is to achieve the same phase conditions with the waveguides involved. For example in the publication of Delacour et al [11] (Fig.

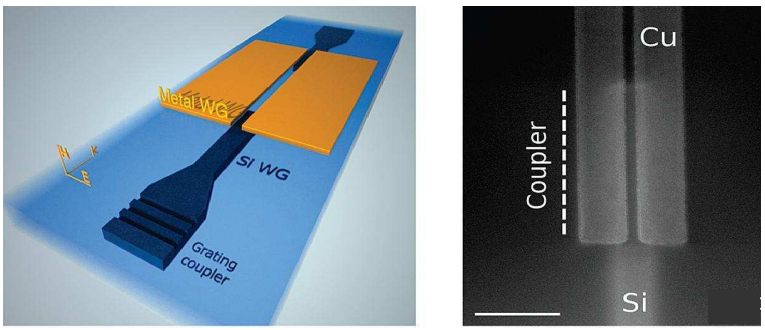

FIGURE 4.2 – *Hybrid optical chip showing directional coupling between the Si-WG and the metal slot waveguide [11].*

4.2) the slot plasmonic WG and the ridge Si-WG were design in a way in order to satisfy the mode phase matching condition of the two waveguides. This could be a great benefit for reducing reflection (see Eq. 4.1). However, this coupling scheme will not be appropriate for coupling light from Si-WG to MISM plasmonic WG due to the immanent momentum mismatch between the modes involved in the two waveguides. The latter is illustrated in the Fig. 4.3 which shows a parametric mode analysis of the fundamental mode supported in the planar MISM stack. It is seen that by varying parameters such as the silicon and insulator thickness (in order to change the momentum of the mode) the effective index of the mode remains very high (> 3.5) and much larger to that supported by the conventional CMOS Si-WG (n_{eff} is approximately 2)

An alternative solution to enhance the coupling between Si WG and plasmonic WG is the taper coupler. By using tapers we can eliminate the abrupt geometrical changes, which is responsible for some scattering and reflection loss, and thus we can achieve higher mode overlap between the incident (I) and the coupled mode (C). As a consequence the radiation loss can be significantly reduced. Different design of couplers are already proposed in the literature including mainly lateral [12, 101, 102, 103, 46, 74] and vertical [104, 13] scheme (Fig. 4.4). The latter is of particular interest because could potentially fit with our problem which is the coupling light into a vertical MISM stack. In this particular scheme, the insertion loss is very sensitive to the thickness of the tapered WG.

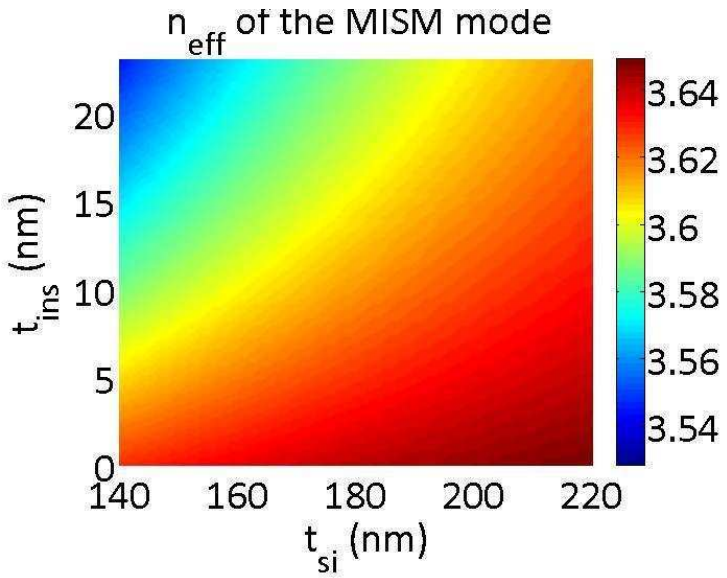

FIGURE 4.3 – *Effective index of the the fundamental mode supported by the MISM stack for different silicon and insulator thickness*

Therefore, an accurate control of the thickness along the taper is needed. However, this will be associated with the development of special etching techniques [105] which induce complexity to the fabrication and therefore is not preferable.

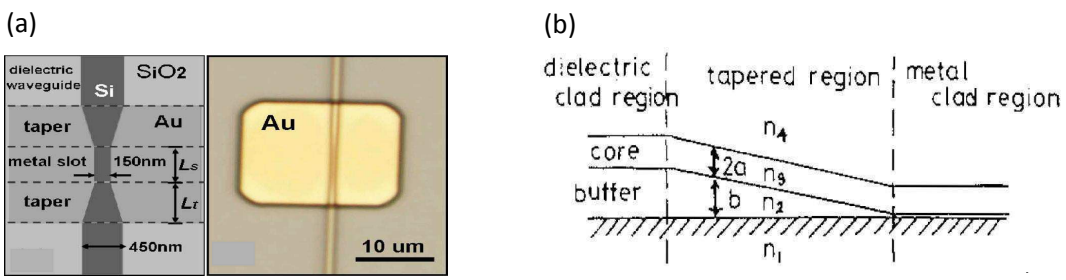

FIGURE 4.4 – *(a) Lateral taper [12]; (b) vertical taper [13] connecting dielectric WG with metal WG.*

Finally, direct or butt coupling is proposed as a simple way to connect Si-WG with PWG. This coupling scheme represents the most straightforward, practical and simple way to link PWG with Si-WG. Butt coupling has already been demonstrated [106], in

2D numerical simulations (infinity width), as an efficient way of putting light inside the PWG. However, for more realistic cases 3D calculations are required. As it is already showed in the introduction, the direct coupling leads to high coupling loss (see Fig. 4.14).

4.3 Novel coupling structure

In this section we describe an efficient coupler scheme by inserting a MISI short waveguide section between the Si-WG and the MISM plasmonic waveguide. Furthermore we have also, using the CMOS technology, fabricated and experimentally characterized this design. Finally it is worth noting that the MISM structures presented here are designed for operation as active switching elements (chapter 5) ; however, this section focuses specifically on minimizing optical coupling loss, which is essential for demonstrating the viability of plasmonic components in practical photonics architectures.

The asymmetric plasmonic-photonic hybrid structure investigated in this section is schematically depicted in the Fig. 9.9. It consists of a vertical MISM structure composed of two symmetric copper metals. The MISM structure is butt-coupled with a monomode Si waveguide of 220 nm $\times$ 500 nm cross section through a compact coupling regime composed of a vertical Copper-Insulator-Silicon-Insulator (MISI) waveguide. Fig. 9.9(b) shows a cross section SEM picture at the level of plasMOStor in the direction perpendicular to the propagation of the light.

The design presented above was investigated with the help of 3D FDTD simulations using the optical constants of copper given in [55], and the optical constants for Si, SiO_2 and Si_3N_4 given by Palik [9] at the wavelength of 1.55 μm. The coupling efficiency is enhanced by inserting an intermediate MISI section between the Si-WG and the MISM-PWG. The principle of this enhancement is governed by multimode interference effect within the MISI section. Furthermore, the MISI section gradually decreases the mode index, which reduces the phase mismatch between the Si-WG and the MISM- PWG and therefore leads to less reflection loss(compared to the case without any MISI section). Hereafter, we present simulations and experiments demonstrating the aforementioned

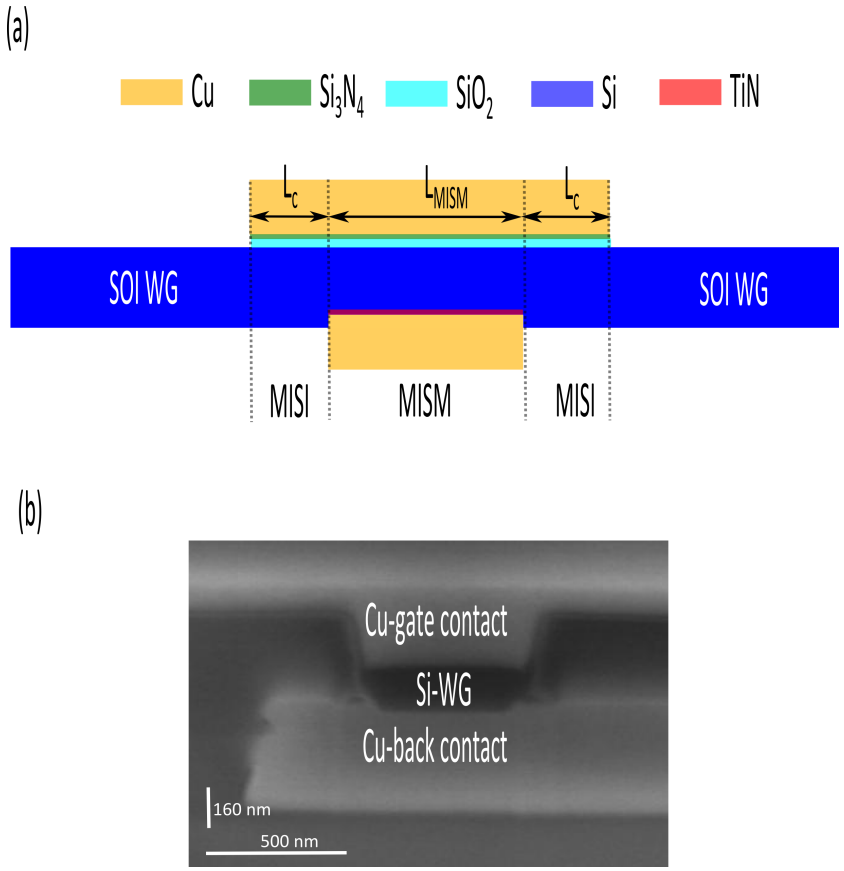

FIGURE 4.5 – *(a) Hybrid plasmonic waveguide showing the coupling structure (MISI) connecting the SOI-waveguide and MISM; (b) SEM image of the cross section of the MISM structure*

physical effects which leads to improved coupling.

Fig. 4.6 shows the back reflected power of the SOI-WG mode as function of the MISM length for L_c= 0 μm (symmetric coupling) and the L_c= 0.7 μm (asymmetric coupling) estimated using FDTD. The simulations were performed at the telecommunication wavelength for a MISM device length (L_{MISM}) varying from 2 μm to 4 μm with a step of 0.15 μm. In the case of L_c=0.7 μm, it was observed that the reflected power is 7% which is 50% less compared to the symmetric case.

The multimode interference effect is also demonstrated with simulations. Fig. 9.10 shows the calculated transmitted power at a wavelength of λ = 1550 nm through a 2.4

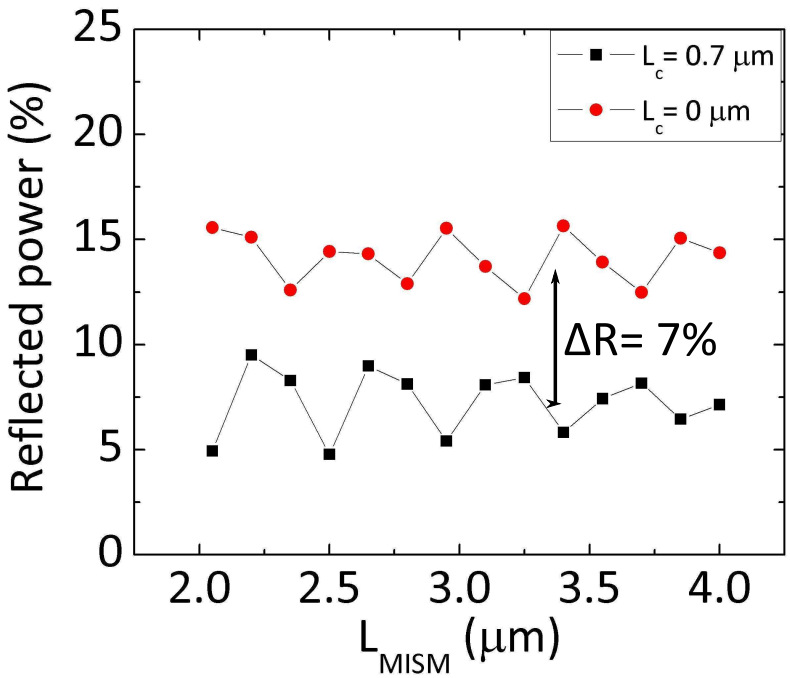

FIGURE 4.6 – *Calculated reflection for different MISM length for two cases : L_c= 0 μm and L_c= 0.7 μm.*

μm long MISM waveguide with identical input and output MISI couplers of length L_c. The coupler length are varying from 0 to 5 μm with an increments of 50 nm. We observe oscillating behavior with a periodicity equal to 1.5 μm with a maximum transmission efficiency (first peak in the Fig. 9.10) at L_c=0.5 μm. Independent of the oscillation, the transmission data (Fig. 9.10(a)) is characterized by an exponentially decaying envelope, which was used to determine the propagation loss of the MISI couplers. In particular, we find that the propagation loss is 0.3 dB.μm^{-1}, in agreement with the imaginary part of the effective index calculated for the fundamental plasmonic mode of the MISI structure (Fig. 4.6a).

Three different MISI lengths, L_{MISI})=0.3 μm, 0.5 μm, 0.7 μm, have been fabricated

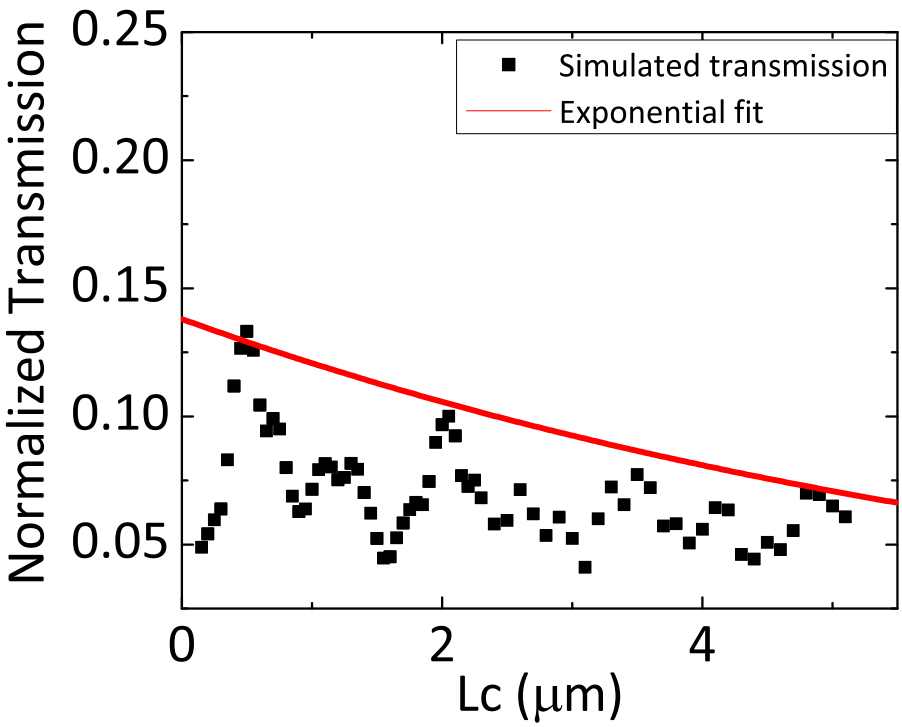

FIGURE 4.7 – *Simulated transmission for different coupling lengths* L_c *and* L_{MISM}*=1* μm*.*

in order to identify the optimum MISI length. We note that the width of the plasmonic section is W_{PL}=330 nm for all the investigated structures. The detailed fabrication procedure is reported to the chapter 3. Automated extraction of optical transmission of the MISM device was implemented at a wafer level scale (for details see the chapter 2). All the transmission measurement was performed at 1550nm using laser as an optical source and the data was normalized with the optical transmission of a reference 220 nm × 500 nm silicon waveguide (SiWG) placed close to every group of 34 PWG samples. We note that, thanks to the ultra large scale fabrication, provided by CMOS technology, a large number of devices are allowed to be tested. In particular, for each MISM section (L_{MISM}), we measure the transmitted power of three identical PWGs at different posi-

tions on the wafer. Figure 9.11 shown the normalized attenuated power of the PWG as a function of the MISM length L_{MISM}, varying between 1 and 6.5 μm, in increments of 150 nm, for three different coupling lengths (L_c=0.7 μm, L_c=0.5 μm, L_c=0.3 μm). The transmitted data is linear fitted and therefore the propagation and insertion losses can be extracted accurately. The fitted value for propagation loss per length is comparable for all contact geometries studied, with an average value of 2.58±0.2 dB/μm (Fig. 4.14a).

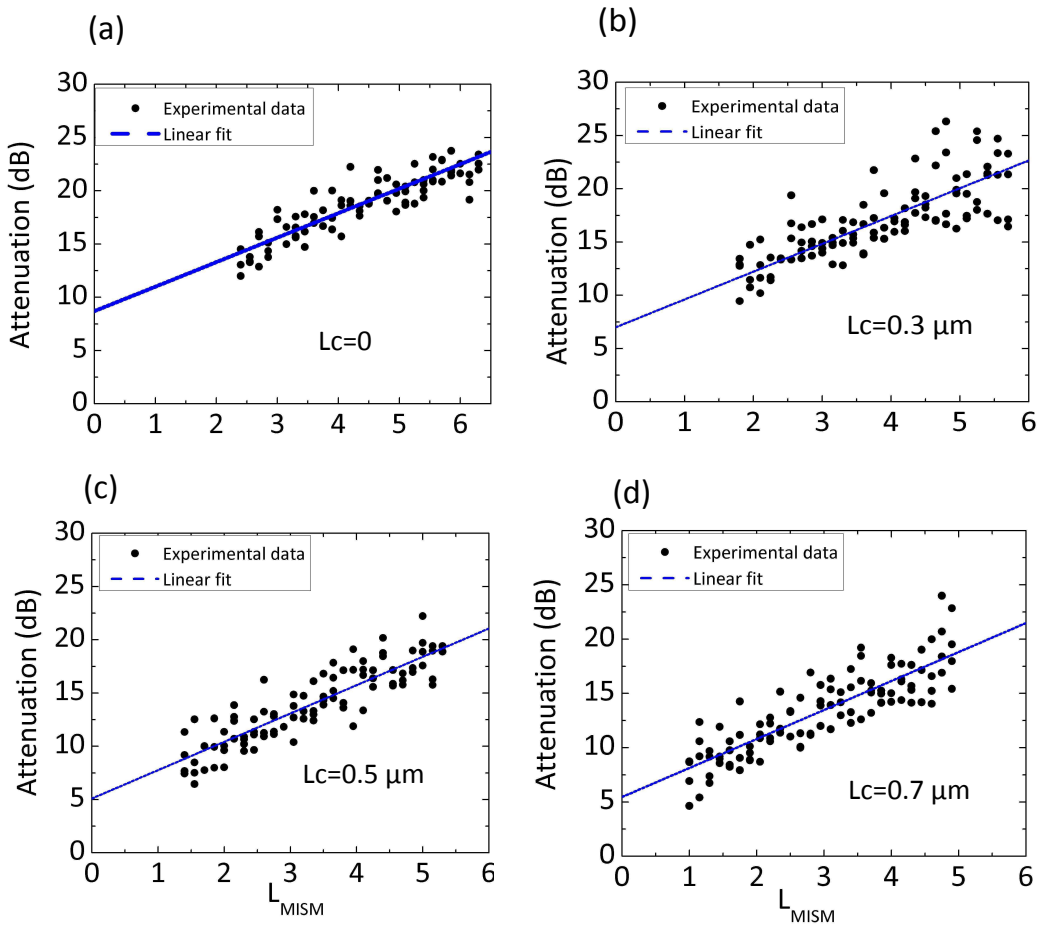

FIGURE 4.8 – *Experimental attenuation measurement as a function of the MISM length (L_{MISM}) for different coupling lengths : (a) symmetric (L_c= 0 μm), (b) L_c=0.3 μm ; (c) L_c=0.5 μm ; (d) L_c=0.7 μm.*

For comparison purpose, a 3D FDTD simulation of the experiment was performed

using nominal geometry parameters for both PWG and SiWG. Fig. 4.9 shows an example of the recording power transmission with fixed L_c=0.7 μm but MISM sections of varing length. The calculation were performed at 1.55 μm single-wavelength. It was observed that the transmission data reveals linear fit from which both the propagation and insertion loss is extracted. The calculated transmission for the other geometries (L_c=0 μm, L_c=0.3 μm, L_c=0.5μm) was also measured and the results from the exponential fit are summarized in the Table 4.1. It is worth noting that the error in the fitted values is reflected in the oscillation in transmission vs. MISM length, apparently due to interference between multiple plasmonic modes. For longer gate contacts the oscillations are diminished suggesting stronger coupling into a single mode.

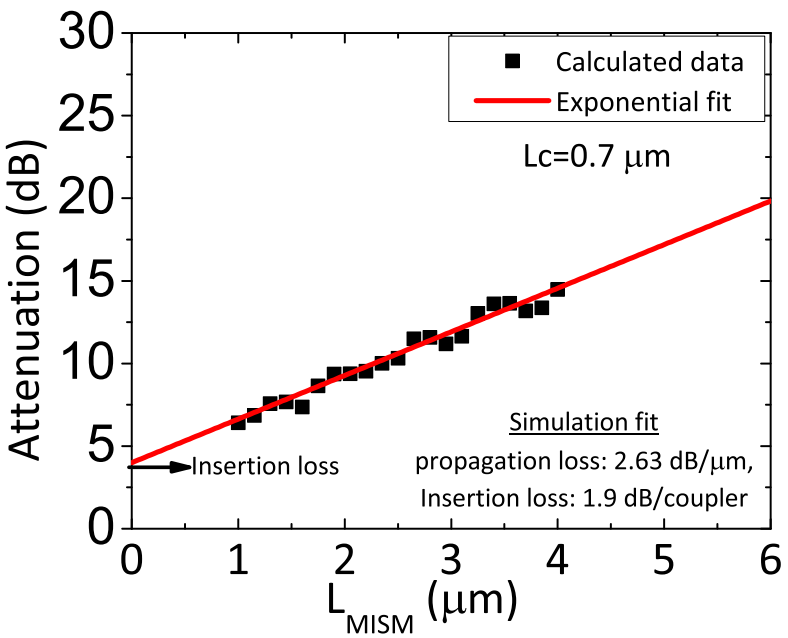

FIGURE 4.9 – *Calculated transmission as a function of the MISM length (L_{MISM}) coupling lengths equal to for L_c=0.7 μm. By an exponential fit (red line) we extract the propagation and the insertion loss*

4.4 Discussion

We start our discussion with the investigation of the numerical results presented in the Fig. 4.6. We recall that in this graph we observe that the power reflection is reduced by 50% in the case of using an additional MISI coupler. In order to understand this behaviour, we estimate the expected Fresnel reflection coefficient between firstly the fundamental SiWG mode (n_{SiWG}= 1.9) and the fundamental MISI mode (n_{MISI}= 2.6) and secondly the MISI mode and the foundamentamental MISM mode (n_{MISM}= 3.5). We found that for the asymmetric case the $R_{fresnel}$=4% which is approximately 50% lower compared to the Fresnel reflection coefficient of the symmetric case ($R_{fresnel}$=9%). Indeed, the MISI section gradually decreases the mode index, which reduces the phase mismatch between the Si-WG and the MISM-PWG and leads to less reflection loss.

In addition to the Fresnel reflection coefficient we estimate the overlap integral (Eq. 4.1) between, firstly, the mode fields of the fundamental TM mode supported in a SiWG section and the mode fields of the fundamental mode supported in a MISI section and, secondly, the fundamental mode supported in a MISI section and the fundamental mode supported in the MISM section. The E and H field of the fundamental plasmonic mode supported in each section (SiWG, MISI and MISM) are presented in the Fig 4.10. According to this calculation, we estimate the total overlap integral value as 0.48 which is very closed to the one calculated for the symmetric case (see introduction).

Finally we estimate the expected power transmission, which is the product of the Fresnel transmission coefficient multiplied by the overlap integral of the corresponding mode fields (calculated above) for the assymetric case. Based on that calculation, we then expect a coupling loss of 3.46 dB per coupler. This value is very close to the one estimated for the symmetric case (3.49 dB, see introduction) but much higher than the expected value from the 3D FDTD transmission calculation (see Fig. 4.14). The reason of discrepancy maybe attributed to the Fabry-Perot effect as well as multimode interference (MMI) effect in the MISI section. The latter is discussed in detail in the following section.

The multimode interference effect thanks to the use of the MISI section was suggested

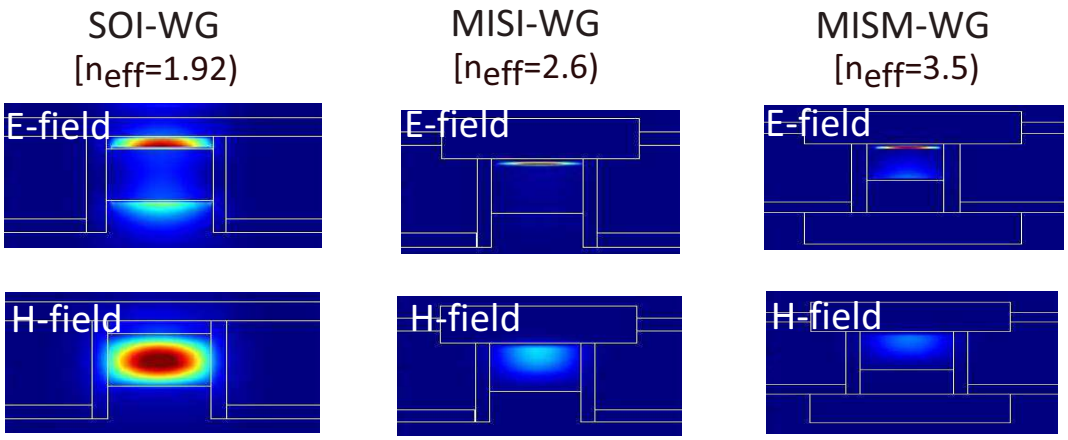

FIGURE 4.10 – *E and H field intensity of the fundamental modes supported in the different sections (SOI-WG, MISI-WG and MISM-WG).*

as another physical phenomenon which improves the coupling efficiency of our device. The first objective of this discussion is to justify that the oscillations observed in the Fig. 9.10 comes from the MISI section (and not from the MISM section). To that respect we plot the field intensity in the side view (slice through the gate insulator) corresponds to a plane bisecting the waveguide in the x-direction. We observe a periodicity of the field, L_b=1.5 μm, in the MISI coupling region (Fig. 9.12(b),(c)). It is therefore plausible that the observed oscillation is a result of the MISI section. The latter is enhanced by an additional simulation experiments that we perform named "one sided calculation". During this calculation, the metal was extended through the PML absorbing layer (inset of Fig. 4.12(b)). By doing that we exclude the effect of out coupling and any phase effect occurring in the MISM section and we focused only to the investigation of the input coupling (i.e from SOI WG to MISI PWG and then to MISM PWG). Optical calculations of the transmitted power as a function of the one sided L_c was recorded and presented in the Fig. 4.12. We found a beating feature of 1.5 μm which is consistent with that observed in the Fig. 9.10(a). These numerical experiment provides evidence that the MISI coupling structure originates the oscillating features observed in the transmission measurement.

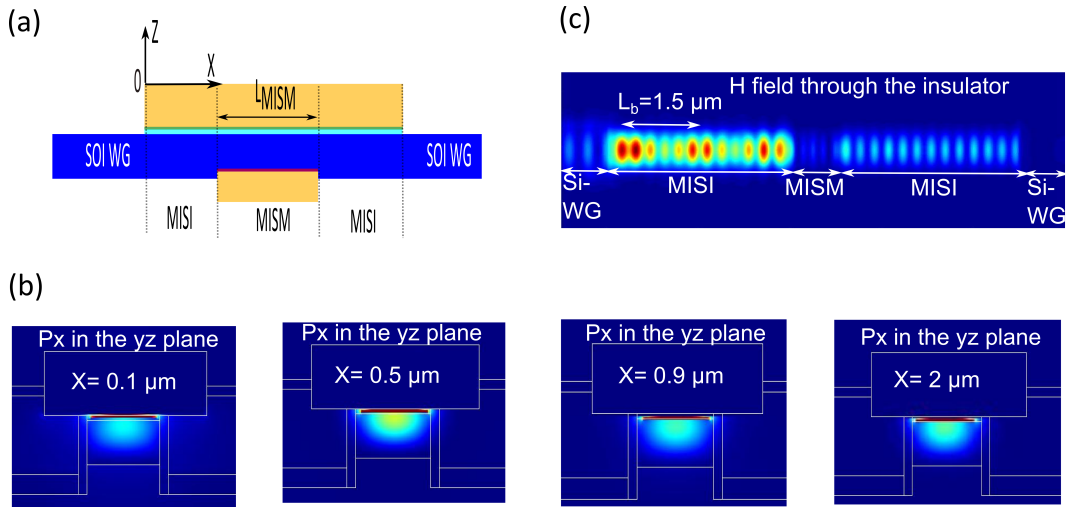

FIGURE 4.11 – *(a) Cross section of the investigated structure in the propagation direction ; (b) Field intensity through the hole device (direction x) from a monitor positioned in the insulator of the gate stack; (c) Power intensity in the propagation direction (Px) at different cross section of the MISI stack (X= 0.1 µm, X= 0.5 µm, X= 0.9 µm, X= 2 µm).*

In order to understand the origin of these oscillations we try to fit the intensity profile of the Fig. 9.10(a) to a model for a Fabry-Perot cavity with loss. We found the non-physical result that the oscillation period corresponds to an intracavity mode index significantly less than 1. The physical interpretation of those oscillating futures is well explained by the multi mode interference phenomena which is detailed reported in the chapter 3.

Finally as the coupler length, L_c, is increased the power transmission efficiency reaches a maximum at L_c=0.5 μm. Even though the optimized MISI coupler regions contribute an additional 1 μm to the overall length of the plasmonic waveguide section, we note that the end-to-end transmission is increased by nearly a factor of three. The optimal value of L_c was found to be approximately 0.5 μm, regardless of the length of the MISM section, indicating that the couplers operate independent of any interference effects within the MISM waveguide region. The latter is demonstrated by performing numerical calculations

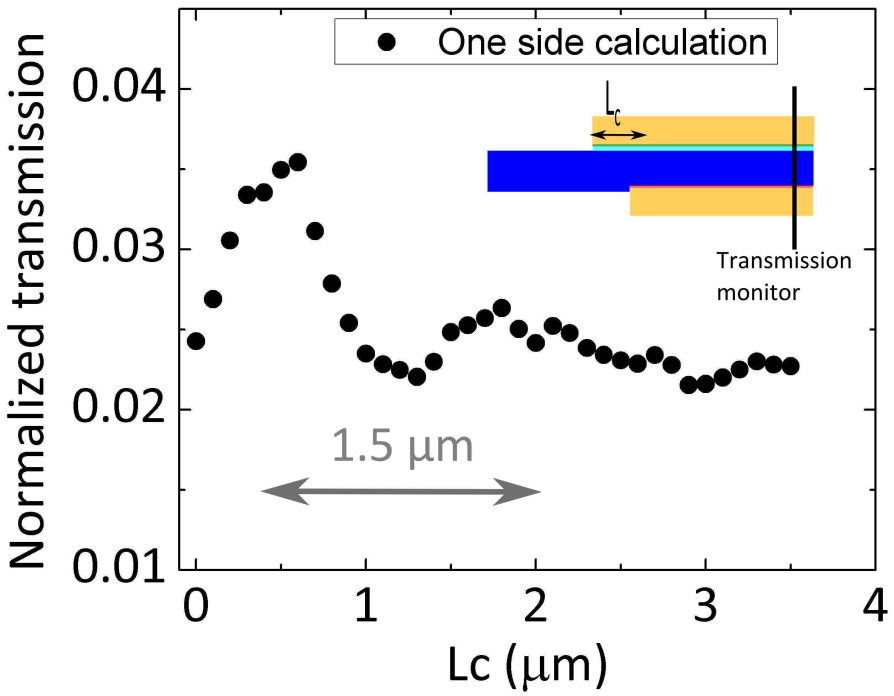

FIGURE 4.12 – *Calculated transmission for different L_c lengths in one side configuration (inset).*

and monitor the transmission power as a function of the coupling length (L_c) for two different MISM length (Fig. 4.13). For both L_{MISM} we observe an oscillating behaviour with a beating period of 1.5 μm which it was independent from the MISM length. An additional decrease of the transmission is observed, which agrees well with the additional induced losses from the increased MISM length.

Table 4.1 summarize the propagation loss extracted from experimental data and 3D FDTD calculations for different coupling lengths (L_c). The fitted value for loss per length is comparable for all contact geometries studied, with an average experimental value of 2.56 dB.μm^{-1}. This value is close to that of the fundamental plasmonic mode loss

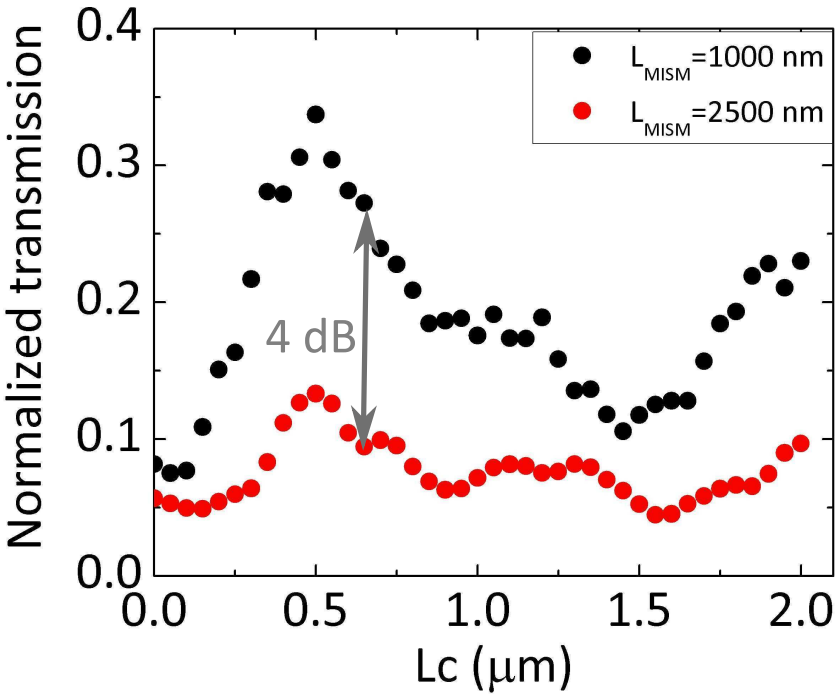

FIGURE 4.13 – *Calculated transmission as a function of the coupler length, L_c, for two different MISM length.*

(supported by MISM stack) estimated from mode analysis.

Fig. 4.14 shows the experimental and theoretical insertion loss for different coupling lengths, L_c, as well as the value obtained from direct coupling theory. Similar to the experimental measurements, the theoretical insertion loss was determined from FDTD simulations with the way explained in Fig. 4.9. From the fabricated devices, we find that an optimal coupling length of 0.5 μm results in an insertion loss of 2.5 dB. As a function of L_c, the measured insertion loss follows the same trend as the calculated values (from FDTD), with an offset of approximately 1 dB for the fabricated devices that we attribute to additional propagation loss caused predominantly by imperfect metal-

TABLE 4.1 – Experimental and theoretical propagation loss for the investigated geometries.

Propagation loss	L_c=0 μm	L_c=0.3 μm	L_c=0.5 μm	L_c=0.7 μm
Experimental (dB.μm^{-1})	2.3±0.2	2.62±0.15	2.66±0.15	2.67±0.15
Theoretical (dB.μm^{-1})	2.6±0.49	2.64±0.35	2.81±0.2	2.64±0.11
Mode analysis (dB.μm^{-1})	2.61	2.61	2.61	2.61

dielectric interfaces in the MISI coupling regions. Finally we compare the insertion loss extracted from both the FDTD and experimental data with that obtained from the direct coupling expression. In the case of an extended MISI section, we observe that the values obtained from FDTD and experiments follows different trend compared to those predicted from the direct coupling method (which are approximately constant for all the investigated geometries). This may be attributed to the MMI phenomena occurs inside the MISI section, which are not taken in acount for the direct coupling calculation. This suggests that the multimode interference effect, plays the dominant role for improving the coupling of our device.

4.5 Comment on the planar structure and the CMOS integrated device

In this section we compare the optical behaviour of the original plasMOStor, invented from CALTECH, with that of integrated plasMOStor, fabricated in the CMOS foundries process available in CEA-LETI.

The original plasmostor is modelled as a four-layer waveguide consisting of semi-infinite Ag cladding layers in contact with the Si core, on the back side, and the SiO_2 on the front side. We recall that this structure, with a Si thickness around 180 nm supports a plasmonic mode and a hybrid "photonic" mode. The electric field distribution of the plasmonic mode (blue) is mainly confined in the insulator and a mode index of n=3.641,

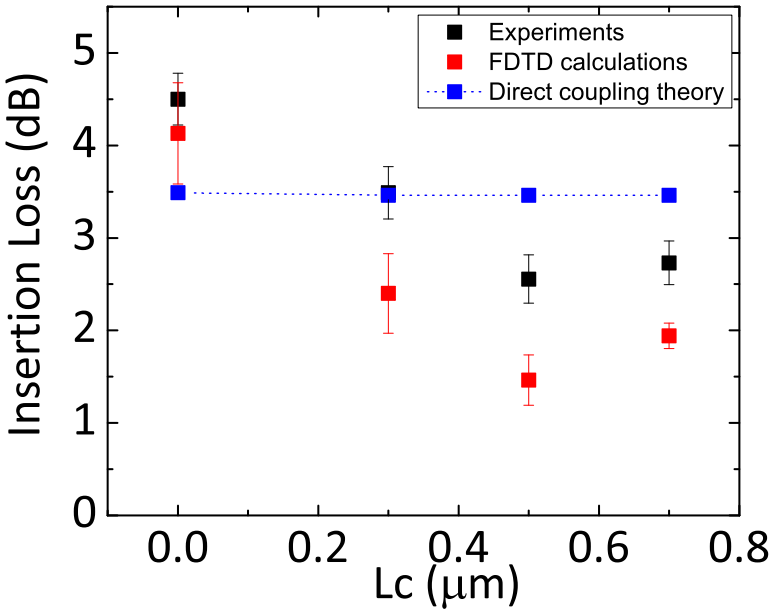

FIGURE 4.14 – *Experimental (black symbols) and simulation (red symbols) insertion loss for different coupling lengths (L_c=0.3 μm, L_c=0.3 μm, L_c=0.5 μm, L_c=0.7 μm). The results obtained from the direct coupling theory (blue symbols) are also presented.*

λ = 1550 nm (t_{Si}~170 nm)	|E| mode profile	Mode Index	Loss (dB/μm)
Off state ($V_{applied}$=0) *depletion*	Ag / SiO_2 / Si / Ag	3.641	0.207
		0.375	2.37
On state ($V_{applied}$>V_{FB}) *accumulation*	Ag / SiO_2 / Si / Ag	3.649	0.228
		0.033	28.14

FIGURE 4.15 – *Mode properties of the plasmostor [10]*

while the electric field of the photonic mode is mainly placed at the center of the Si-WG and a mode index of n=0.375 (Fig. 4.15). Although, the loss of the plasmonic mode were reasonably low (0.207 dB/μm), the loss of the photonic mode is relatively large (10 times larger compared to the plasmonic mode).

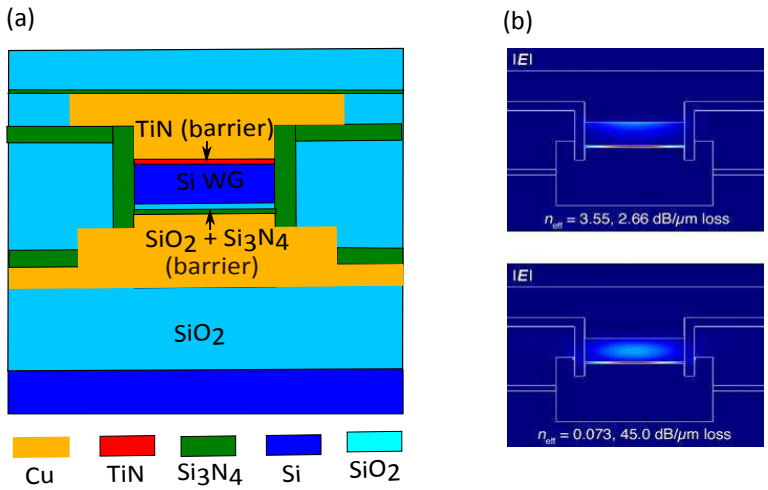

FIGURE 4.16 – *(a) Device schematic of the integrated plasmostor ; (b) Mode properties of the integrated plasmostor*

We already discussed (chapter 3) that the proposed structure of plasmostor can not be integrated as it is within the CMOS environment. Presented below are some simulations of the CMOS stack (Court. CALTECH) The main constraints comes from the need of CMOS compatible material which also prevents both the optical and electrical behaviour of our device. We remind that regarding the material aspects, instead of Ag we use Cu (CMOS compatible) and also we use inter-facial layers between the metal/insulator and the metal/Si. Fig. 4.16a shows the new geometry which fulfils the above mentioned requirements. Fig. 4.16b shows the modes supported by the device with the as-fabricated integrated geometry. A plasmonic modes with loss of 2.6 dB/μm, and a very lossy âĂIJphotonicâĂİ (45 dB/μm) mode are supported. By comparing those losses with the slab design we observe that the plasmonic loss increases by a factor of 10 and the photonic mode loss by a factor of 20. This is due either to materials choice (TiN is very loss material for plasmons) either to the geometry (the lateral confinement induce

higher optical loss). As a conclusion, the CMOS restrictions induce higher optical losses and may prevent the device from functioning as well as the slab design.

4.6 Conclusion

We have provided an efficient and simple way to couple light from Si-WG to vertical MISM PWG by inserting a MISI coupling section between the two waveguides. This coupling scheme allowing insertion losses as low as 2.5 dB/coupler. This value is 3 times smaller compared to the case of direct coupling (without any MISI section). The significant improvement of coupling loss is attributed to the following reasons : (a) thanks to the use of the MISI section we gradually decreases the mode index, which reduces the phase mismatch between the Si-WG and the MISM-PWG and leads to less reflection loss(compared to the case without any MISI section) ; (b) the proposed coupler acts as a multimode interference region and therefore, working at the first peak of the oscillating behaviour we can benefit of an enhanced coupling. We demonstrate also that the dominant effect of the improved coupling is the MMI effect. Finally a comparison between the slab and the integrated plasMOStor was performed, assuming that the lateral confinement and the materials restriction demanded by CMOS environment preventing the device from functioning as well as in the slab design.

Chapitre 5

Electro-Optical Investigation of Integrated MOS plasmonic Modulator

This chapter presents the electro-optical investigation of MOS plasmonic modulator. At the beginning we check the interest of using high dielectric constant (high-k) materials such as Al_2O_3 and HfO_2 in order to achieve an optimized MOS structure with low operation voltage and low insertion loss. After that, we present a detailed electro-optical investigation of the integrated plasmostor. The theoretical study shows that the Electro-Absorption (EA) is the dominant effect for light modulation with the accumulation conditions as the most efficient operation mode given the optical loss of the plasmonic mode. Electrical measurements are also performed showing devices with accumulation capacitance of few fF and leakage current below 10fA. Finally, electro-optical (EO) measurements show an optical modulation having a capacitive signature, in agreement with simulations.

5.1 Insertion loss of a MISM stack

The performance of our device may be defined in terms of both the modulation depth and the insertion loss. The latter investigated in detail in this section.

Insertion loss refers to the loss due to the incoupling ($k_{coupling}$) and outcoupling ($k_{coupling}$) losses as well as the material absorption loss, ($k_{absorption}$), within the MISM region :

$$k_{total}(dB) = k_{incoupling} + k_{outcoupling} + k_{absorption} \tag{5.1}$$

In the chapter 4 the incoupling and outcoupling processes were discussed (relating to the first two components of the right side of Eq. 5.1) without dealing with the MISM absorption loss. These optical losses are related to the modal absorption coefficient that is a function of the constituent dimensions, the absorption coefficient materials, as well as the spatial distribution of the electric field component. The absorption loss (in dB/μm) of the MISM stack is given by the relation :

$$k_{absorption} = -10log[exp(-\alpha_{mode} \times L_{MISM})] \tag{5.2}$$

where L_{MISM} is the MISM length and α_{mode} is the mode loss. In the following we will investigate the MISM absorption loss with respect to the nature (i.e. high-k dielectric material) and thickness of the insulator as well as the thickness of the Si layer in the MISM stack (see Fig. 5.1).

5.2 Interest of high-k dielectrics to optimize the insertion loss of a MISM stack

The impact of the thickness and different optical index insulating layers on optical losses was investigated for the MISM plasmonic waveguide shown in the Fig. 5.3 with the help of the mode solver described in the chapter 2.

This waveguide consists of a five layer of Cu-SiO_2-Si(160 nm)-TiN(5 nm)-Cu waveguide. The thickness of the insulator (t_{ins}) vary from 3 nm to 40 nm. The thickness of

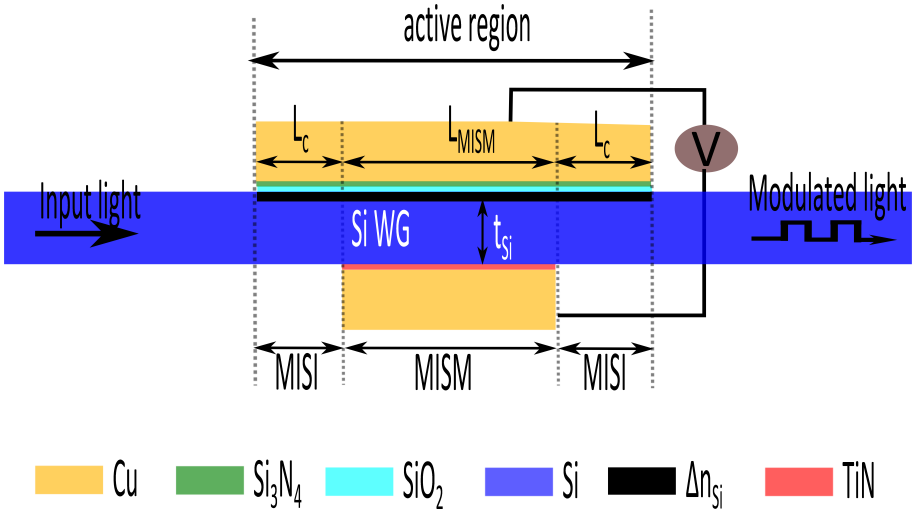

FIGURE 5.1 – *Schematic cross section of the active integrated plasmostor*

the Cu film is 400 nm in order to avoid effects of the Cu film thickness on the plasmonic mode inside the insulator as the plasmonic skin depth in Cu remains approximately constant at 22 nm at near-infrared wavelengths. We investigate this structure for ope-

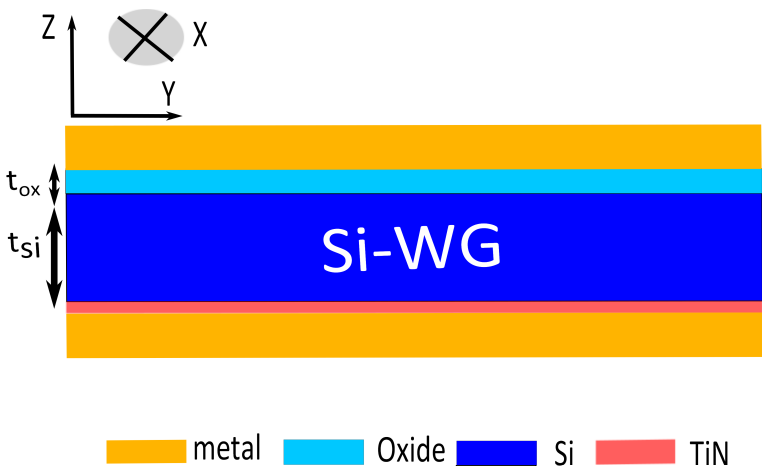

FIGURE 5.2 – *Schematic of the 2D MISM plasmonic waveguide with infinite width*

ration wavelength at 1.55 μm. We note that the optical index of the materials used is given in [9] except the Cu [55]. Fig. 5.3 shows the propagation losses of the fundamental plasmonic mode with varying the insulator thickness using SiO_2 or Al_2O_3 as insulators.

For both cases, we found that the losses of the fundamental plasmonic mode decreases with decreasing the insulator thickness.

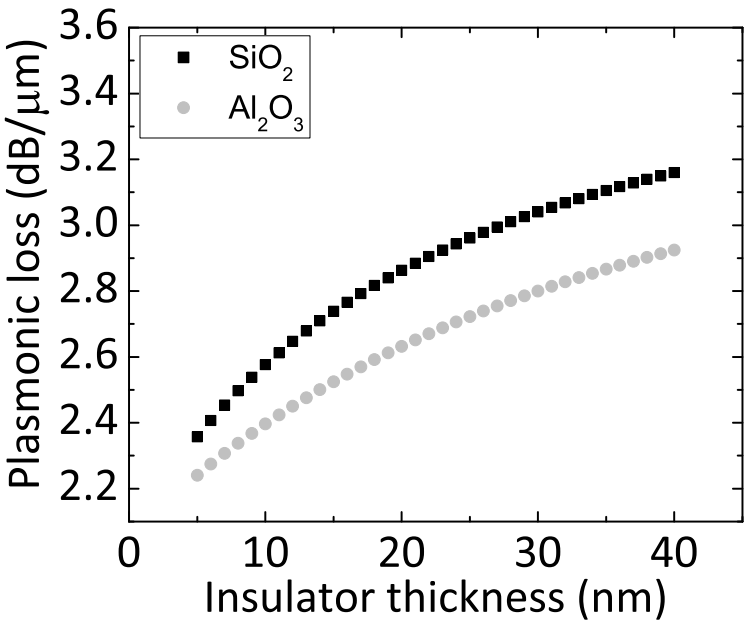

FIGURE 5.3 – *Plasmonic losses as a function of the gate oxide physical thickness with SiO_2 and Al_2O_3*

In order to understand the origin of this behaviour we plot the Electric field intensity for five different insulator thickness (Fig. 5.4(a)). We observe that by increasing the thickness of the oxide, the magnitude of the field inside the very lossy back metal (TiN/Cu) is increasing leading therefore to higher optical losses.

The oxide optical index related losses is also a key challenge of plasmon assisted electro-optical devices. In our specific design we observe that by switching from SiO_2 (optical index : 1.44 at 1.55 μm) to Al_2O_3 (optical index : 1.75 at 1.55 μm) we decrease the optical losses of the MISM stack. This decrease of the loss is, again, attributed to the lower field inside the back metal (Cu/TiN) which in turn leads to lower optical loss.

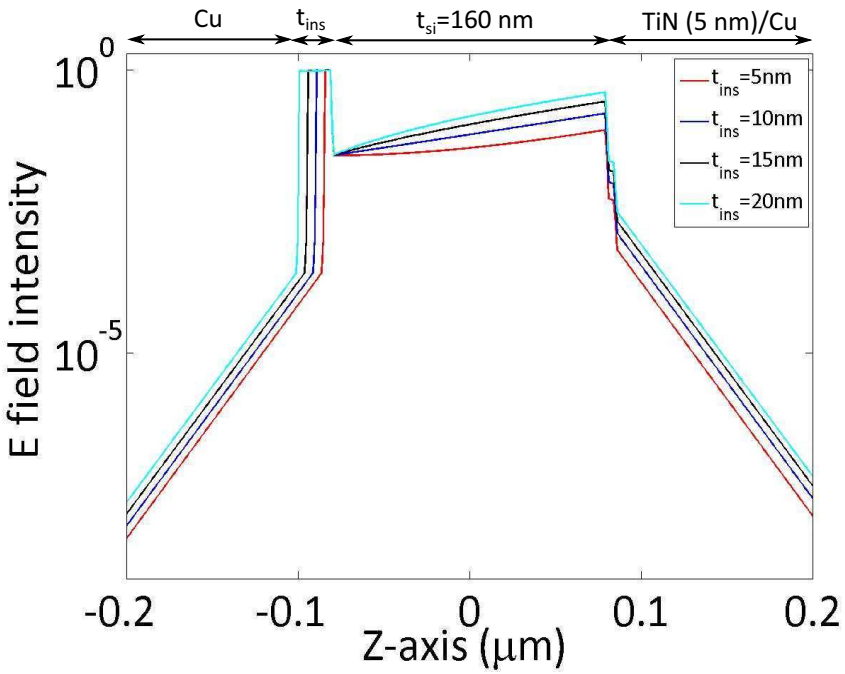

FIGURE 5.4 – *Plot of the electric field intensity, E, for t_{si}=160 nm and t_{ins}=5,10,15 and 20 nm*

At that point, it must be considered that optimizing the insulator parameters (i.e. thickness and nature) from the optical point of view, we affect also the electrical performance of the device, such as operation voltage. For example a MOS plasmonic modulator is a capacitance-operated device in which the operation voltage depends both on the thickness (t_{ins}) and the dielectric constant (k_{ins}) of the insulator :

$$V_g - V_{fb} = \frac{Q}{C_{ox}} = \frac{Qt_{ox}}{\varepsilon_0 k_{ox} A} \tag{5.3}$$

where the parameters V_g, V_{fb}, Q, C_{ox}, ϵ_0 and A are already defined in the chapter 2. We note that, by using the definition of the EOT ($EOT = \frac{k_{ox}}{k_{high-k}} t_{ox}$ see chapter 2) we can write the Eq. 5.3 in more convenient way for the purpose of the electrical design of the device :

$$V_g - V_{fb} = \frac{QEOT}{k_{SiO_2} A} \tag{5.4}$$

Therefore the thickness as well as the nature of the insulator, or alternative the EOT,

within a plasmonic MOS modulator will affect its performance in terms of the optical losses and operation voltage.

After this small introduction, Fig. 5.3 can be replotted in more beneficiary way for the purpose of the electro-optical design of the devices. In Fig. 5.5, the plasmonic losses is now plotted as a function of the EOT and not the physical thickness of the insulator. In this case, we observe that for constant EOT (constant operation voltage) the loss induced by the Al_2O_3 is higher than the one of SiO_2. This results from the increased thickness of the insulator, thanks to the use of high-k dielectrics, thereby increasing the optical losses.

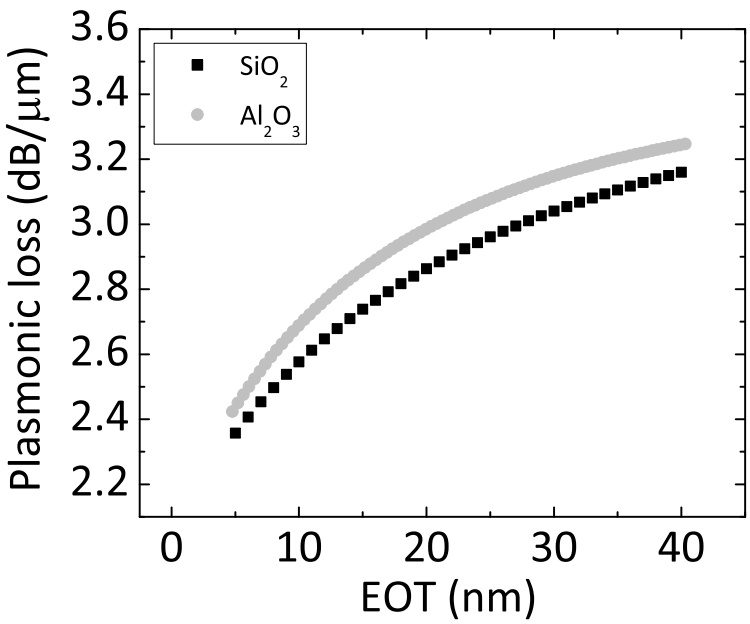

FIGURE 5.5 – *Plasmonic losses as a function of the gate oxide thickness for t_{si}=160 nm*

Moreover the Si-WG thickness also affects the optical losses of the MISM region. It was found that by increasing the SiWG thickness the optical losses are reduced. This is due to the fact that by increasing the Si-WG we deconfine the mode and therefore the

intensity of the field inside the metal becomes lower which can be translated to lower optical loss. Therefore the higher the SiWG thickness the lower the optical losses. In this study, since the objective it was to work with single mode operation, we choose the Si thickness as 160 nm which is the limit of single mode operation (after this thickness the device behave as a multimode).

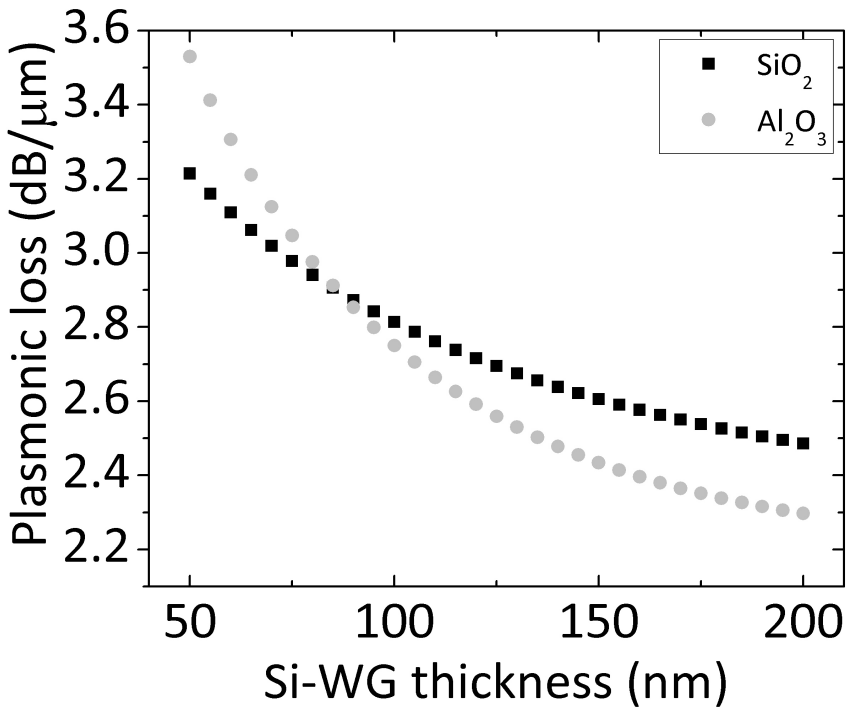

FIGURE 5.6 – *Plasmonic losses as a function of the SiWG thickness*

Based on the analysis made above, the propagation loss of the fundamental plasmonic mode is calculated for different Si thickness and EOT in order to identify the set of parameters (EOT,t_{si}) for achieving an optimize structure operates at low voltage (or lower EOT) and low optical loss compared to the case of SiO_2. Fig. 9.13 shows the interesting range of EOT and thickness of Si (tsi) for having higher propagation length

by using high-k dielectrics such as Al_2O_3 and HFO_2. In the following graphs we plot the percentage changes in propagation length compared to SiO_2 (A) as function of EOT and t_{si}. The quantity A is define using the following equation : A = (propagation length (Al_2O_3 or HFO_2)- propagation length (SiO_2))/ propagation length (SiO_2). This equation shows that when the quantity A is positive it means that the propagation length induced by high-k dielectrics is higher compared to the case of using SiO_2 (see equation 2). Therefore for A>0 it is interesting to use high-k dielectrics for lower optical losses.

For low operation voltage it is interesting to work with EOT thickness varying from 1 nm<EOT<10 nm. At this range, and for t_{Si}= 160 nm, using Al_2O_3 and HfO_2 as a high-k insulator provides no gain in propagation loss of the fundamental plasmonic mode compared to the case of using SiO_2 of the same EOT. The same study was performed for a MISI stack and the results are presented in the Appendix 8.

In conclusion, by using high-k dielectrics and for constant operation voltage (or EOT) there is no gain in the absorption loss of targeted MISM stack compared to the case that we use SiO_2 as an insulator. However, when the physical thickness is fixed (and not the EOT), by using high-k dielectrics (Al_2O_3 and HfO_2) we significantly reduce both the optical absorption loss (Fig. 5.3) and the operation voltage (see Eq. 5.3).

5.3 Electrical reliable high-k gate stacks

As high-k dielectrics can be interesting to lower the optical propagation loss as well as the operation voltage of our device, we decided to experimental validate the use of high-k dielectrics for application to MOS plasmonics modulator. To this aim, we fabricate MOS capacitor with Al_2O_3 and HfO_2 high-k dielectrics (available with industrial process in our clean room) with Cu gate electrodes (previously demonstrated as highly promising for plasmonic applications). Indeed, these structures allow us to make a first evaluation of the Cu/high-k electrical reliability for future applications to the MOS plasmostor. Hereafter, we present the experimental electrical studies that were performed at the mentioned structures.

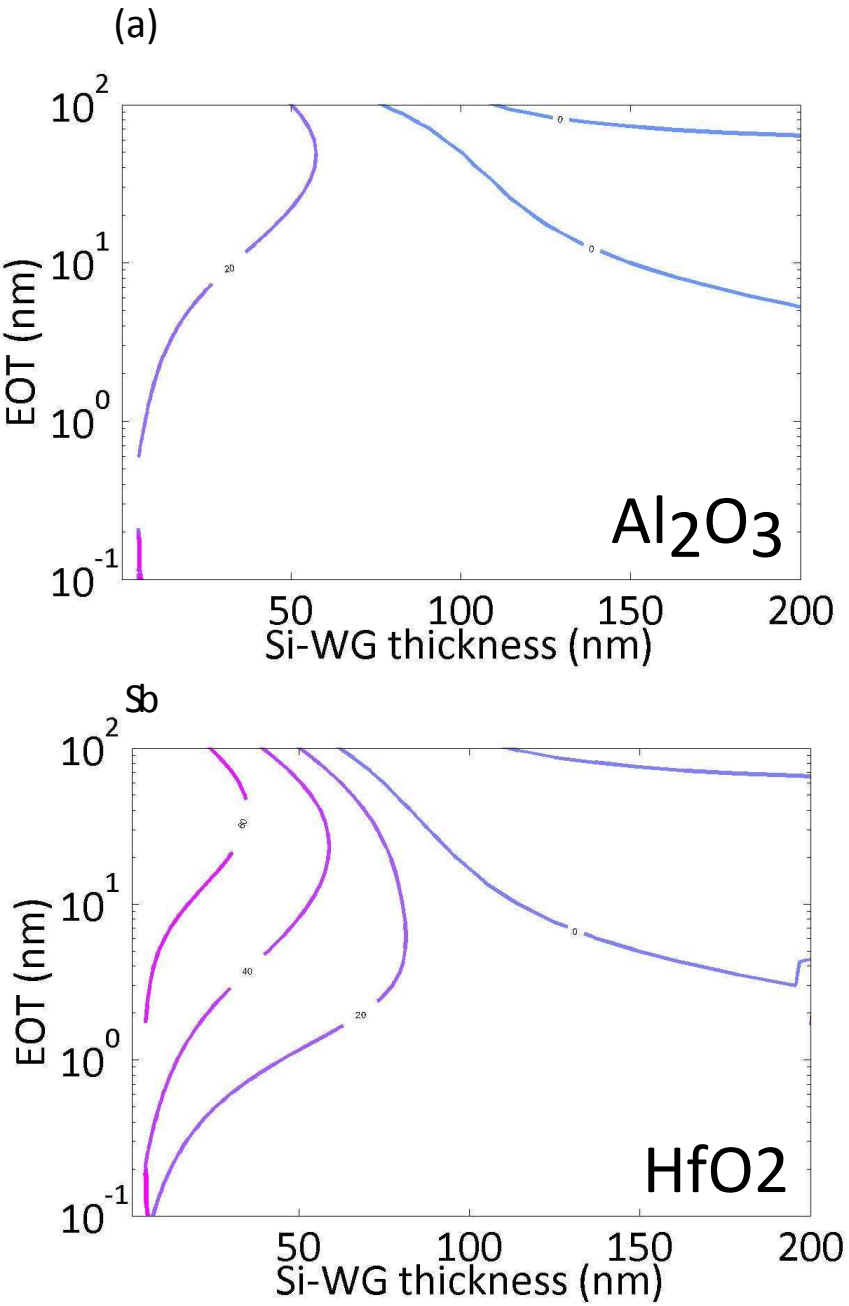

FIGURE 5.7 – *Percentage gain in propagation loss (%) compared to the SiO_2 as a function of EOT and Si thickness when (a) Al_2O_3 or (b) HFO_2 are used.*

In order to validate the electrical reliability of the high-k stacks, we fabricated copper gate MOS capacitors on p-type silicon wafers on 200 mm silicon wafers on the Leti fabrication line. MOS capacitance was designed and fabricated by a damascene patterning technique of the gate metal electrode with the same way described in chapter 3 (Fig. 5.8(a), (b), (c)). After that steps, atomic layer deposition (ALD) was used in order to

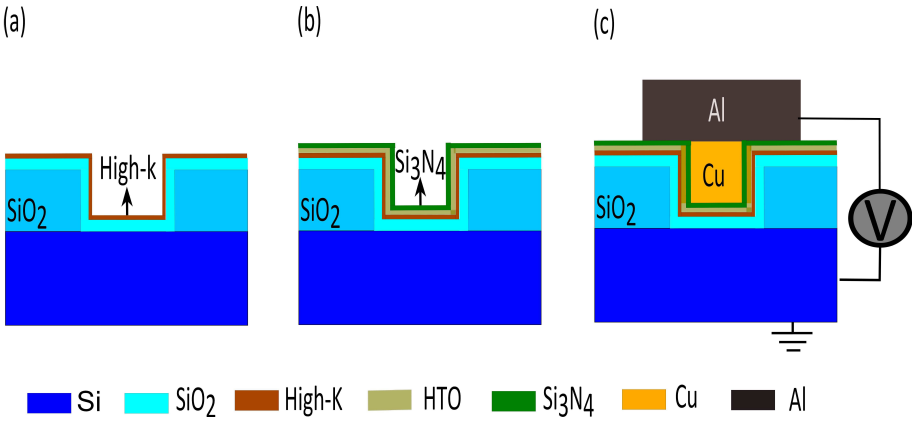

FIGURE 5.8 – *Fabrication process of high-k MOS capacitors using standard CMOS technology.*

fabricate 6 nm of Al_2O_3 and HFO_2 in two different samples (Fig. 5.8(a)). A thermal oxide of 2 nm is then deposited on the silicon wafers by heating at 720 °C (5.8(b)). The stoichiometric Si_3 N_4 layer (3 nm) is then deposited over the oxide via low pressure chemical vapour deposition (LPCVD) at a temperature of 625 °C. The latter is used as a diffusion barrier of copper (chapter 3). The role of the 2 nm HTO is to protect the high-k dielectrics from the chemical interaction of the deposition atmosphere used during CVD Si_3N_4. A copper layer is then deposited with the same way as in chapter 3. The final structure is depicted in the Fig. 5.8(c). We recall that all the capacitors are temperature stressed at 450 °C.

Capacitance-voltage measurements were performed (details for experimental set up in chapter 2), for different stacks (described in Table 5.1) on a surface of 10000 μm^2. The C-V experimental curves were nicely fitted accordingly to the simulation tool used in this thesis, namely "Le simulateur" (described in section 2). Therefore an accurate

Gate stack	Si_3N_4(3nm)/ HTO(2nm)/ Al_2O_3(6nm)	Si_3N_4(3nm)/ HTO(2nm)/ HfO_2(6nm)	Si_3N_4(4nm)/ SiO_2(10nm) (ref 1)	SiO_2(10nm) (ref 2)
EOT(nm)	6.5	5.5	11.7	10
$C_{(-3.5MV/cm)}$ (mF/m^2)	5	5.9	2.8	3.3

TABLE 5.1 – EOT of different gate stacks investigated in this thesis extracted from C-V measurements with the corresponding accumulation capacitance at -3MV/cm.

extraction of the EOT was achieved. The results are summarized in Table 5.1. It is found, as expected, that by introducing high-k materials in the gate stack we can achieve higher accumulation capacitance compared to the SiO_2 (thickness of 10 nm) gate stack. We note that the comparison were done at the same oxide field. These results showing the interest of high-k dielectrics for low operation voltage for devices design for plasmonic application (e.g. by using Cu as electrode).

As it is already discussed in chapter 3, using copper as a metal electrode may impact the reliability of the investigated MOS capacitance due to the diffusion of Cu ions inside the active region of MOS capacitor. We consequently showed that the Si_3N_4 layer used to improve the reliability of SiO_2 insulator MOS stack in chapter 3 can be used in a similar way for high-k. Fig. 5.9 shows Weibul scale plot of the high-k stacks with and without Si_3N_4 as a barrier. We observe that devices without any Si_3N_4 as a barrier shows extrinsic break down behaviour with early failure observed for more than the 70% of barrierless devices for an applied oxide field smaller than 1MV/cm. On the other hand by using high-k with Si_3N_4 as a barrier we observe that more than 95% of the devices have a break down voltage of -12 V without any extrinsic behaviour. As in chapter 3, we attribute this behaviour to the less Cu concentration inside the active region of the MOS capacitor which is a consequence of diffusion barrier effect introduced by thin Si_3N_4.

Our results showing that high-k dielectrics without any diffusion barrier can not be an electrical reliable MOS structure, in contrast to earlier findings. For example, Majumder et al. [107] demonstrates that ALD deposited ultrathin 1 and 2 nm-thicknesses of

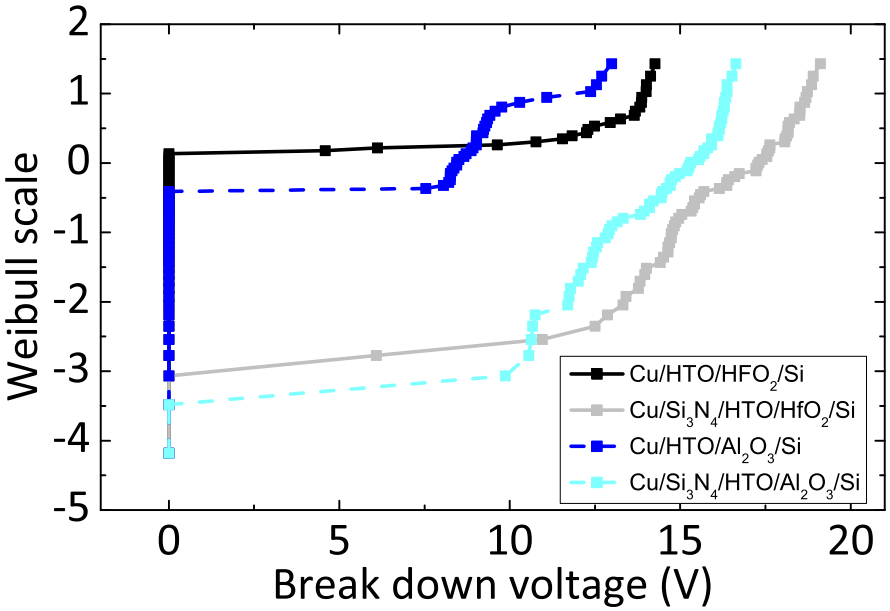

FIGURE 5.9 – *Break down field characteristics for high-k insulator stacks with and without the insertion of thin Si_3N_4 as abarrier*

HFO_2 and Al_2O_3, are capable of limiting the copper diffusion. In this research study, the effect of HFO_2 and Al_2O_3 based diffusion barrier has been studied using two characterization techniques. The first technique was a classical four-point probe for sheet resistance measurements. This probe was used to measure sheet resistance of stacks containing a diffusion barrier layer as a function of annealing temperature. The second technique was an X-ray diffraction (XRD) analysis which was carried out to identify phase formations of compounds containing Cu and Si atoms in annealed stacks containing a diffusion barrier layer. The use of XRD analysis allowed the detection of Cu_3Si compound formation. This compound requires the presence of a significant Cu atom concentration in a silicon layer. According to this study, XRD analysis can qualitatively detect the annealing temperature of the mechanical failure of the barrier film. Likewise, the four-point probe measurements

are appreciable only in the presence of significant Cu atom diffusion in a silicon layer. Generally, these two characterization techniques detect Cu atoms penetration in the silicon layer with typically a ratio greater than 0.1%. Therefore, these results could be available to realize diffusion barriers for interconnections in ultra-large scale integrated circuits, but probably would not be a valid criterion to test and perform effective diffusion barriers in a MOS capacitor stack. Indeed, the constraint in terms of impurity concentration is more drastic for stacks used in a MOS capacitor structure (electrical failure mode) than for an interconnection (metallurgical failure mode).

In conclusion, at the beginning we demonstrate the interest of high-k dielectrics for reducing the insertion loss and the operation voltage of the integrated plasmostor. This result was the driving force in order to fabricate and experimental demonstrate an electrical reliable high-k MOS stack, consistent with the demands of CMOS technology. The aforementioned results is promising for the next generation of the integrated plasmostor.

5.4 Theoretical investigation of the electro-optical response

This section deals with the theoretical study of the electro-optical behaviour of the integrated plasMOStor described in chapter 3. Fig 5.1 shows the schematic cross section of the investigated modulator through the direction of light propagation. As the input light reaches the active region, it couples to the plasmonic mode supported by the structure which is modulated by the voltage-induced optical index change of Si (Δn_{Si} in black in Fig. 5.1) through the accumulated charge carriers.

We first begin with the optical investigation of our device in the active operation mode (voltage on). The problem here, is to accurately estimate the voltage-induced optical index change of Si which, in turn, affect the optical properties of the supported mode (effective index and mode loss). Based on a detailed literature survey of previous works, it is noted that these index changes either were predicted using the Soref [108] or Drude [109] model. On close comparison of the foresaid models, a difference in scaling of refractive index and absorption coefficient is observed. Fig. 5.10 presents the refrac-

tive index and absorption coefficient changes varied as a function of induced electron and hole concentration (estimated with the electrical model described below) for the aforementioned models.

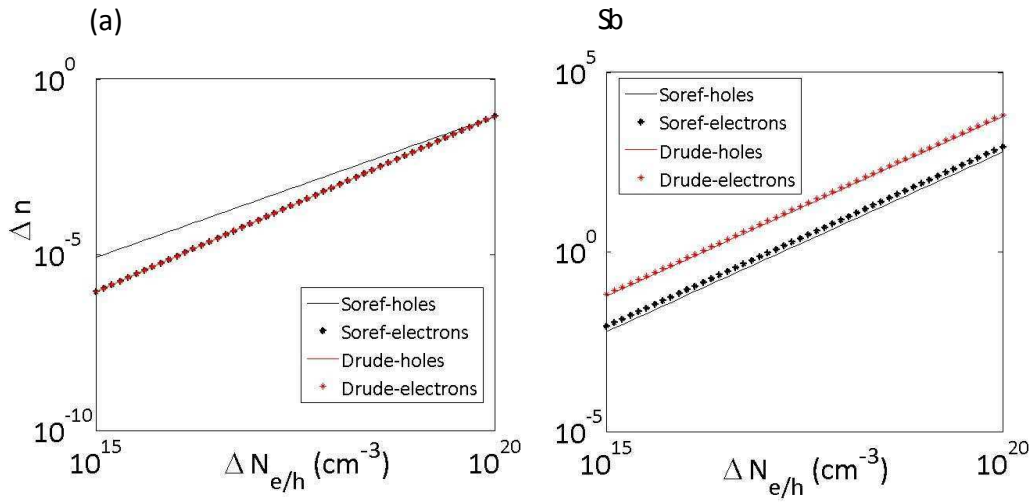

FIGURE 5.10 – *(a) Refractive index change extracted from Soref and Drude model; (b) Absorption coefficient change extracted from Soref and Drude model at 1.55 μm*

The Drude model parameters are chosen as m_h=0.39m_0, m_e=0.26m_0 μ_e= 1000 cm^2V/s and μ_h= 500 cm^2V/s (the values are taken from [68]). As far as the change in refractive index is concerned, there exists a match between the two models with regard to variation in electron concentration. In the case of low free hole concentration however, there is an order of difference in magnitude for the refractive indices predicted by the two models. Furthermore, it is seen that while the Drude model predicts same refractive index changes due to free electrons and holes, the Soref model likewise predicts more changes in index due to free holes. Also with regard to the optical absorption coefficients, the Drude model predicts higher changes compared to the Soref model. In the following, the Soref model is used as it is a valid formula which is widely used and demonstrated in the standard Si photonics [110].

With regard to the electrical operation, the parameters that we are interesting for a MOS modulator are the amount of carriers concentration in accumulation regime as

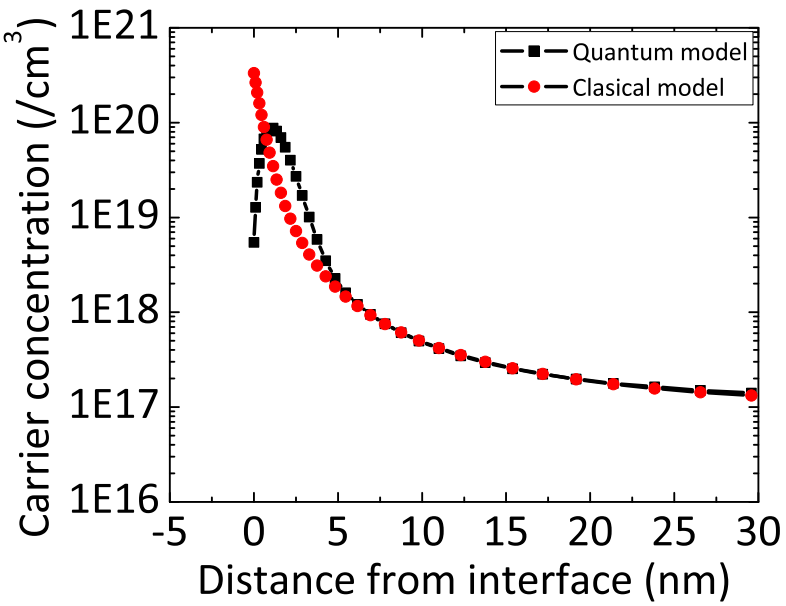

FIGURE 5.11 – *Carrier concentration in accumulation conditions using semi classical and Shrodinger-Poisson model*

well as the spatial distribution of these carriers inside the Si. These parameters are determined using two simulation programmes : the 2D device simulation package ATLAS from SILVACO and the "Simulateur" (see chapter 2 for details). For the calculations, the classical and the quantum approach are considered since both of them are used in the literature. For example Dionne et al. [6] model the electron carrier density in accumulation conditions using a classical model with a maximum of charge density at the interface of Si/SiO_2 and a Debye decay length of 14 nm. On the other hand Zhu [54] they use quantum mechanical approach. Fig. 5.11 shows the simulated electron density at accumulation conditions as a function of the distance from the interface using both approach. It can be seen that when the quantum mechanical approach (Schrodinger and poisson equation) is used, the maximum carrier concentration is located few Angstroms below the interface Si/SiO_2. This position is directly linked to the wavefunction associated with the carriers

which is near zero at the insulator-silicon interface because of the high energy barrier of the insulator. On the other hand, the classical method (analysis based on PoissonâĂŹs equation and Fermi-Dirac function) predicts maximum charge density at the interface of Si/Insulator. Finally, the quantum model shows 1.5 times less maximum carrier intensity compared to that of classical model. Considering the electro-optical behaviour of the integrated plasMOStor (our work), we note that the accurate estimation of index change close to the Si/insulator interface is critical. This is because at this interface the overlap between the optical power and the voltage-induced optical index changes is maximum and therefore sensitive to small index changes. Therefore, in this thesis the quantum mechanical model was used as it is the most accurate approach especially for the region close to the interface.

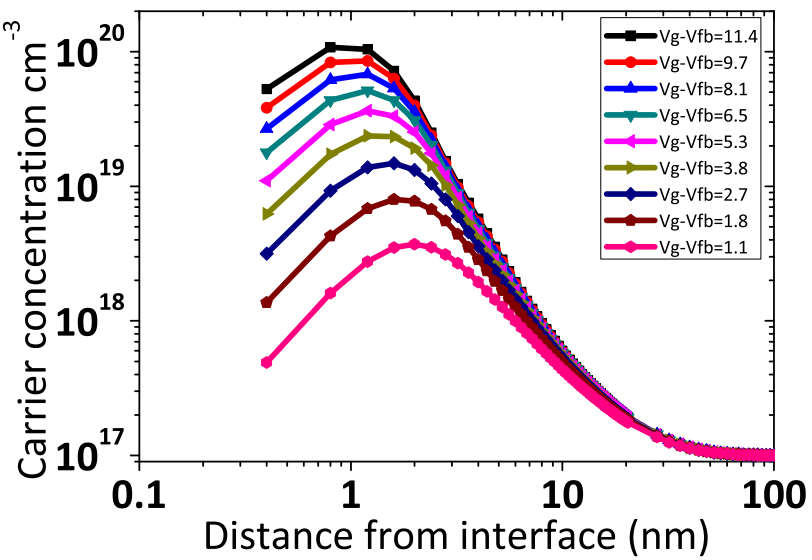

FIGURE 5.12 – *Carrier concentration in accumulation conditions for different applied voltages*

Fig. 5.12 shows the simulated electron density as a function of the distance from the interface for various applied voltages using the quantum approach, after fitting with the

experimental C-V measurements which are shown in the next section (Fig. 5.16(a)). It can be seen that the free carriers in the accumulation layer are localized in a thin region that is about 4 nm. This spread is slightly depends on the applied voltage ; higher bias forces the carrier to be closer to the interface [68].

Based on the previous analysis and with the help of the electro-optical simulation tools (described in chapter 2), we investigate the properties of our modulator. The objective at that point, is to classify our modulator as either electro-refractive (the principle of operation is based on the changes of the real part of the refractive index) or electro-absorptive (the principle of operation is based on the changes of the imaginary part of the of the refractive index).

Considering the experimental results presented in the chapter 4, we will consider a situation of single mode operation ; only the fundamental plasmonic mode is supported by the integrated plasmostor MISM stack. Based on that, the only way to consider electro-refraction (ER) is to assume that we have a lossy Fabry-Perot cavity. We check this assumption with the help of 3D FDTD simulation, by performing two different numerical experiments in an asymmetric device (Fig. 5.1) with extended gate metal of L_c= 0.7 μm. In the first one, we calculate the induced modulation depth (MD) at different L_{MISM} lengths by considering both electro-refraction and electro-absorption effect. The MD, in this case, is defined as (P_{off}-P_{on})/P_{off} where P_{off} and P_{on} are the transmission power in the "off" and "on" state respectively at 1.55 μm. The accumulated layer in the "on state" (V_g= 3 V) was modelled as a 3 different layers with the first layer adjacent to the SiO_2-Si interface and the others stick below to each other. The thickness t, the carrier concentration N and the optical index for each layer were taken as : (t1, N1, n1)= (0.5 nm, 2.1×10^{18}/cm^3, 3.477+0.0013i) ; (t2, N2, n2)= (2 nm, 1.36×10^{19}/cm^3, 3.468+0.0059i) ; (t3, N3, n3)= (0.5 nm, 7.1×10^{18}/cm^3, 3.473+0.0031i). The length of this layers was chosen to cover all the active region L_{acc}= 2L_c+L_{MISM} (see Fig. 5.1), assuming that the Si(p-type)/TiN junction is ohmic contact and the electrical loss in the Si (p-type) substrate are negligible. We check this assumption by performing 1D calculations using SILVACO. The investigated structure is presented in the onset of Fig. 5.13. We note

that the calculation are done for an ideal MOS stack, means that the stack is free from interface, mobile and oxide charge. The Si thickness was fixed at 160 nm. Furthermore, the work function of Cu and TiN is taken as W_{Cu}=4.55 eV [111] and W_{TiN}=4.6 eV (mid-gap metal [112]). Fig 5.13 shows the calculated capacitance at different dc bias for an Ohmic and Schottky back contact. We found that the maximum variation between the measured capacitances is less than 6% (observed at the inversion regime). It is therefore reasonable to use the back contact as an Ohmic.

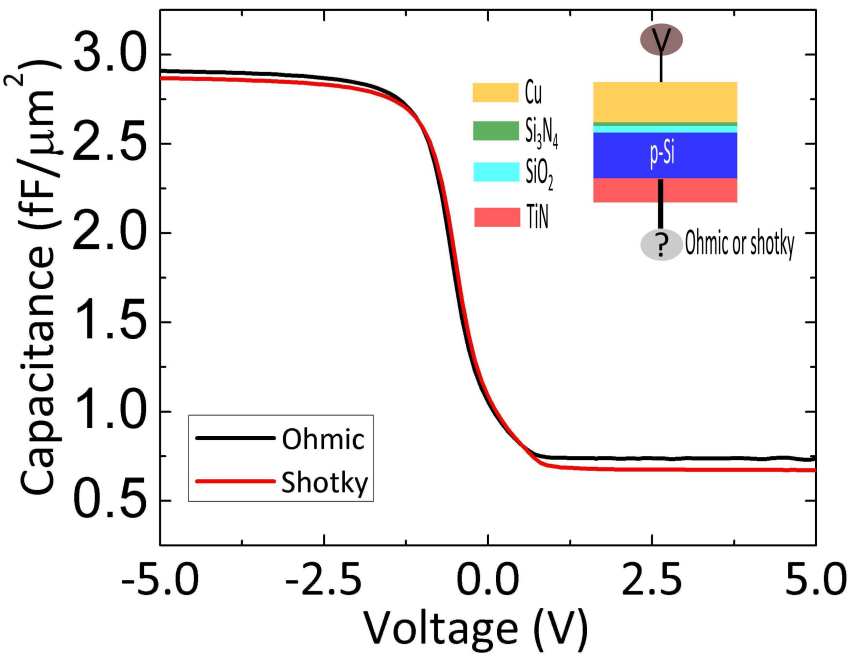

FIGURE 5.13 – *Capacitance voltage characteristics for an Ohmic and Schottky back contact*

In another numerical experiment we consider the EA as the only effect which defines the modulation depth of our device. In this case, the MD is defined with the following

simple mathematical relation [113] :

$$MD = 1 - exp(-\Delta a \times L) \tag{5.5}$$

where Δa=a_{on}-a_{off}, and a_{on} and a_{off} refers to the optical absorption coefficient in the "on" and "off" state respectively and L is the length of the device. It is worth mentioning that, since $\Delta a << 1$ (of the order of 3.48 $\times 10^{-4}$ dB), the Eq. 5.5 can be aproximate as $MD = \Delta a \times L$.

Fig. 9.14(a) shows the results of the MD as a function of the L_{MISM} length for the numerical experiments described above. This data was plotted with a linear fit and the slope of this fit gives the modulation depth per μm which was calculated to be 0.03487 $\pm$ 0.005 %/μm. We found that the modulation depth estimated by Eq. 5.5 follows the same trend as the FDTD data suggesting that the dominant mechanism which leads our device to an increased modulation as a function of its length, is the electro-absorption effect. Furthermore an additional offset of 0.0161% was observed between the FDTD data and the Eq. 5.5. This is may be attributed to the additional modulation induced by the extended length of the metal (L_c). We check that by using the Eq. 5.5 with optical absorption coefficients (at "on" and "off" state) of the MISI section (see Fig. 5.1) estimated by mode analysis. For a device length of $2L_c$= 1.4 μm we found a modulation depth value of 0.0166 which is consistent with observed offset.

Fig. 5.15 shows the theoretical results of the DC modulation depth at different operation modes of the MOS capacitor (accumulation, depletion, inversion) for a voltage range from -5V to 5V. The results are obtained by considering only EA effect (Eq. 5.5). The absorption coefficient of the modes was calculated by the mode solver described in chapter 2. The investigated structure consist of five layer Cu/Si_3N_4(3 nm)/SiO_2 (10 nm)/TiN (5 nm)/Cu (like the fabricated MISM stack). The analysis were perform at 1.55 μm.

It is observed that the depletion mode induce less modulation (10 times lower) compared to the inversion and the accumulation operation mode. This is due to the higher overlap of the accumulated or inverted charge layer with the optical power. Further-

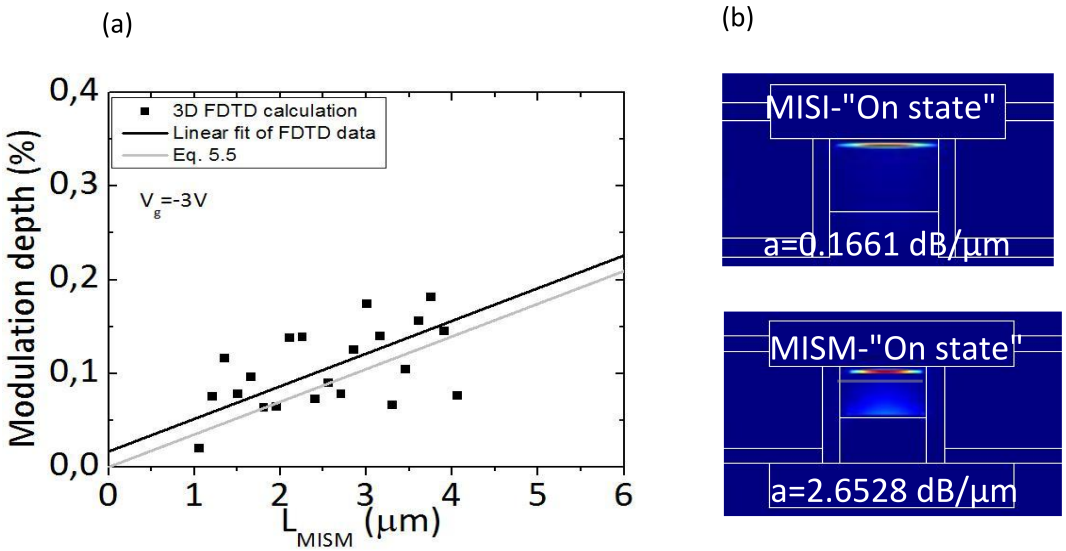

FIGURE 5.14 – *(a) Modulation depth estimated by 3D FDTD simulations; (b) Mode analysis of the on state for the fundamental modes supported by MISI and MISM section*

more, the amount of charge in these two modes is much larger than that of the depletion mode which means higher electro-optical changes which finally leads to higher modulation depth. Hence, both accumulation and inversion are the most efficient operation modes for modulating light in the plasmonic MOS stack. However, for high bandwidth applications the inversion operation mode it is not well suited due to the inability of the minority charge to follow the electrical signal [68].

Considering the EA effect as the only mechanism of light modulation, we found a maximum modulations depth as low as 0.6% which corresponds to maximum applied voltage (i.e. at -5V) and for the longer device (7 μm). The reason of this poor electro-optical behaviour is attributed to both single mode operation and the low electro-optical interaction of light with charge carriers in silicon. The extracted value of the MD (in dB/μm) for our MOS plasmonic modulator was compared with the one of waveguide-based MOS modulator [114, 115]. We found that in our device the MD is 1.5×10^{-3} dB/μm which 10 times larger than the one observed in [114, 115]. This is due to the fact that a higher fraction of the power is overlapped with the accumulated layer which leads

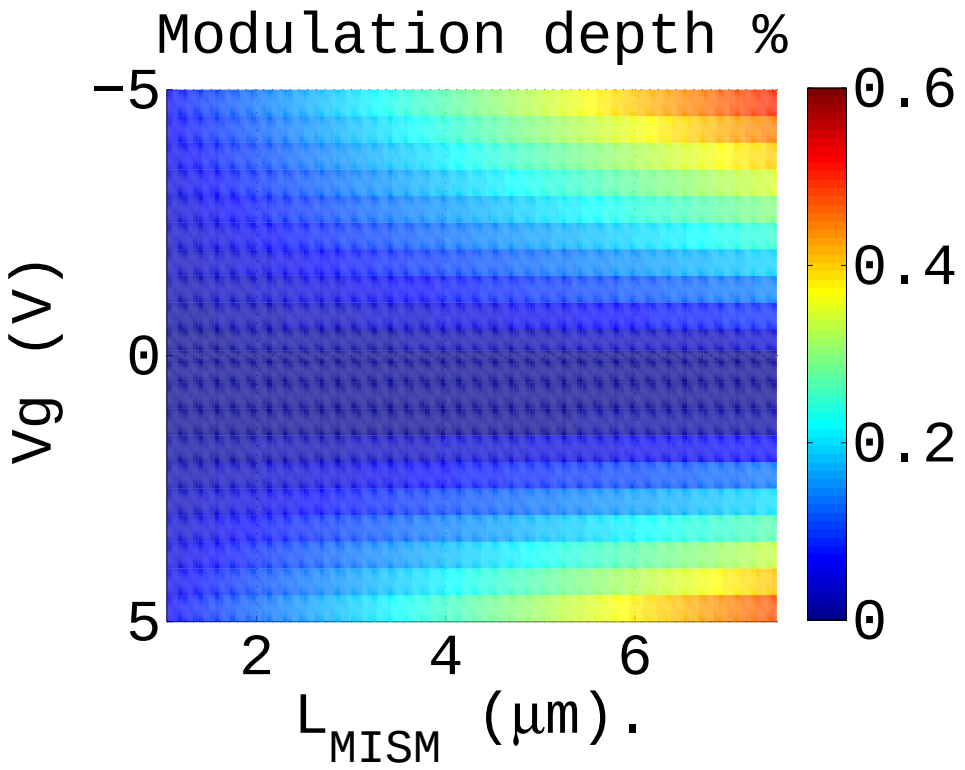

FIGURE 5.15 – *Theoretical investigation of the DC modulation depth for different operation modes of the MOS capacitor (accumulation, depletion, inversion).*

to higher electro-optic effect. While this result is promising for further reducing the size of the device, it is clear that, the plasmonic modulator (which investigated in this thesis) do not have a practical future because they induce high optical loss, 2.6 dB/μm, which is 1000 times larger than the one investigated in [114, 115]. For example in order to achieve a modulation depth of 3 dB we have to use a 2000 μm device length which in turn leads to an optical loss of 5200 dB. These results illustrate the difficult trade off to be made between optical loss and modulation depth in plasmonic modulators.

5.5 Electrical characterization

The electrical behaviour of the fabricated plasmonic modulator (see chapter 3) has been investigated by means of capacitance-voltage (C-V), conductance-Voltage (G-V) and dc leakage current-voltage (I-V) measurements.

We start the experimental investigation of the integrated plasMOStor by performing capacitance-voltage measurement at 100 kHz. The experimental set-up used for measuring such small capacitance is already discussed in chapter 2. Fig.5.16(a) shows a typical C-V measurement of our device. As the figure disclose, three MOS operation mode are observed, namely accumulation ($V_g < -1.7V$), depletion ($-1.7V < V_g < 1.5V$), and deep depletion ($V_g > 1.5V$). The inversion layer is not observe due to the incapacity of charge to follow the applied ac signal. The latter is a an experimental demonstration which reveals that the inversion operation mode is not relevant for high speed operation. Moreover, a numerical fit of the experiments was performed, accordingly to the model described in section 2, in order to determine the fundamental parameters which characterise the gate oxide layer in an MOS capacitors such as equivalent oxide thickness (EOT) and flat band voltage (V_{fb}). Table 5.2 summarize the extracted values. The accumulated capacitance is also estimated to be as 2,7 fF/μm.

Another parameter which can estimated from the C-V measurements is the electrical power consumption per transferred information (bit). This can be calculated using the relation $\frac{1}{2}CV^2$, where C is the device capacitance of the MOS capacitor and V is the applied voltage. Assuming an applied voltage of -3V and an accumulated capacitance of 2.7 fF.μm^{-2} the electrical energy consumption was found 24 fJ.μm^{-2}.bit. Considering that the surface of the fabricated plasmostor is varying between 0.25 μm^2 to 5 μm^2, the energy consumption will varying also from 6 fJ (for the lower surface) to 120 fJ. These values are much lower compared to that of the existing optical modulators (see table chapter 1), fulfilling the energy consumption criteria of CMOS technology which is smaller than 100 fJ/bit [116]. Finally, Fig. 5.16(b) shows the dc leakage current measurement for the integrated plasmostor for voltages varying from -11V to 11V. For the

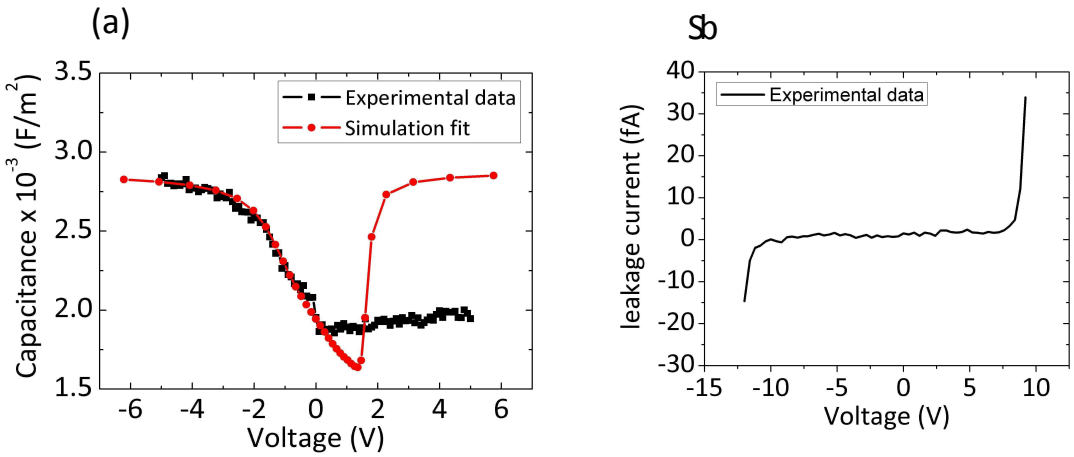

FIGURE 5.16 – *(a) Capacitance-voltage characteristic for the integrated plasmostor; (b)DC leakage current at different voltages*

Gate stack	Integrated plasMOStor
EOT (nm)	11.8
V_{fb} (V)	-1.7

TABLE 5.2 – EOT and V_{fb} of the integrated plasMOStor

voltage range -10V to 10V the leakage current is as low as few fF for 2 μm^2 (or equivalent less than $10^{-8}A/cm^2$) which is a typical value for a non leaky capacitors [117]. Furthermore, by comparing the leakage current density of our device with the one of the MOS plasmonic modulator recently published by Zhu et. al [54] ($10^4A/cm^2$) we observe more than 12 order of magnitude lower value in our device for the same applied oxide field (approximately -10 MV/cm).

Fig. 5.17 shows a plot of the oxide capacitance (at -5V) as a function of the the device surface area. Along with the experimental data, a theoretical line with a slope corresponding to EOT= 11.7 nm is also presented. This value of the EOT corresponds to the measured one from the C-V measurements. For device surfaces larger than 2.5 μm^2, it is observed that the experimental oxide capacitance is directly proportional to the surface area of the device (Eg. 5.3) and follows the expected theoretical line. For very

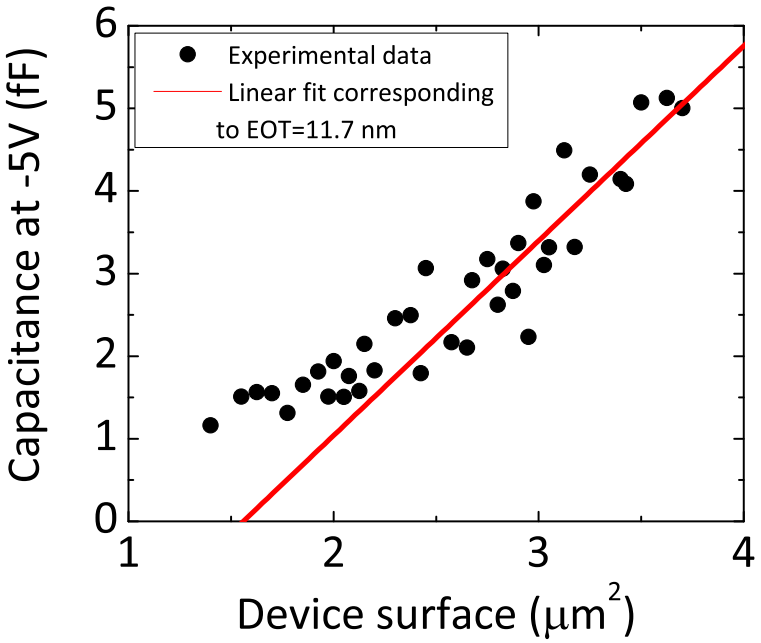

FIGURE 5.17 – *Oxide capacitance at -5V as a function of the surface*

small devices (smaller than 2.5 μm^2), it is found that the expected behaviour deviate with respect to the experimental one. This is may be attributed to inaccuracies between the real fabricated surface area value of the device and that of the design (which is used for the plot in Fig. 5.17)or the calibration procedure.

Fig. 5.18 shows the conductance of our device as a function of the dc voltage. The absence of a peak in the measurement curve means that the device resistance produced the dominant loss, completely masking the interface trap loss [88]. From the capacitance and conductance measurements in strong accumulation conditions, the series resistance can be measured considering the equivalent circuit of the MOS capacitor [88]. Based on our experimental results, we measure a series resistance $R_s = \frac{G_m}{G_m^2+\omega^2 C_m^2} = 10^8 \Omega$, where G_m and C_m are the measured conductance and capacitance respectevely. The origin of this high resistance is still under investigation.

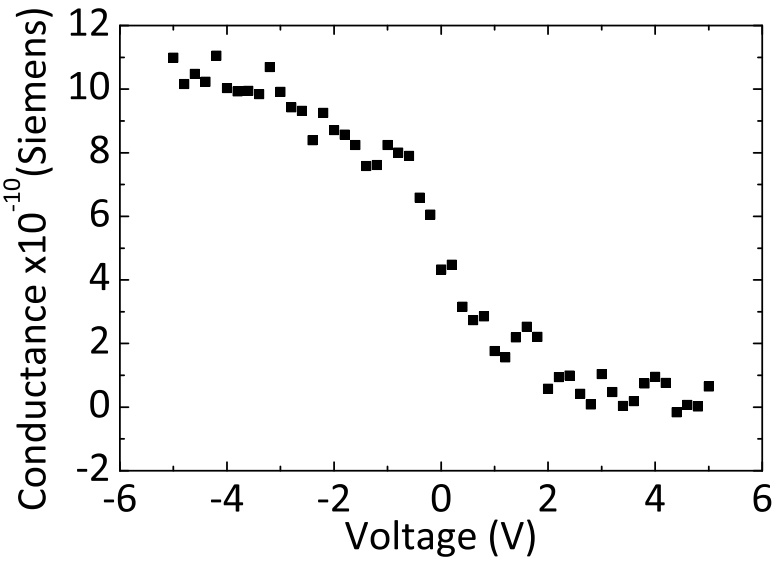

FIGURE 5.18 – *Conductance-voltage characteristic for the integrated plasmostor*

5.6 Electro-optical characterization

In this section the electro-optical experimental results are presented and a discussion of the results have been done including a comparison with simulations.

We start with the investigation of the experimental electro-optical behaviour of our device by measuring its modulation depth as a function of the applied voltage and device length (Fig. 5.19). The measurements were done with the experimental set-up already described in chapter 2. At 1.55 μm the modulation depth increases as a function of the voltage. This is something which expected since applying a higher voltage will lead to higher optical index changes which in turn leads to a higher modulation depth. When plotted as a function of the device length, it is seen that the modulation depth is also increasing with an additional oscillating behaviour. This oscillating feature of the modulation depth may be attributed to the Fabry Perot effect inside the MISI and MISM stack as a result of reflection from the corresponding metal end facets.

In order to draw a comparison between the simulations and experiments we replot the Fig. 9.14 along with the experimental data (Fig. 5.19(b)). The experiments were performed for different device lengths and for constant voltage of V_g=-3 V. By linear fit the experimental data we extract the slope which corresponds to the modulation depth per μm and was estimated to be 0.038 $\pm$ 0.008 %/μm. This value is 10% higher with respect to the simulated one (extracted above). The observed discrepancy could be due to the difference in both charge density and charge profile of accumulated carrier used in simulations and the experiments.

Finally, in order to check the ability of our device to modulate light at high frequency we perform small signal transient measurement. In this experiment, by applying a dc voltage (varying from -5V to 5V) we polarize the MOS capacitor in order to have different operating modes (accumulation, depletion, inversion). Along with this dc voltage a small signal voltage is also applied (V_m= 40 mV with its frequency varying from 100 kHz to 2 MHz). The measured quantity was the modulated light intensity at different dc voltage and different frequency. Below we will describe this small signal characteristics for the accumulation operation mode.

In the accumulation conditions the total measured capacitance (C_{total}) is equal to the oxide capacitance C_{ox} of the MOS capacitor. The latter is expected to be independent from the operation frequency [68]. For example if we use the estimated oxide capacitance C_{ox}= 2.4 fF/μm^2 (Fig. 5.16) with a load resistance of R=50 Ω we expect a time constant (RC) of 100 fs/μm demonstrating the ability of this device to operate at high frequency. However, on analysing experimental results (Fig. 9.15) we observe a frequency dependence behaviour at accumulation condition. The latter is attributed to the high resistance of our device (calcutated as shown above, R_s= $10^8\Omega$). For example, if we consider device capacitance of few fF, the operation speed of our device was estimated to be few MHz.

A few μm plasmonic modulator is experimentally investigated. Devices show leakage current below 10 fA through the copper electrodes based MOS capacitance. The accumulation capacitance was found to scale with the surface of the device with a slope which is consistent with the equivalent oxide thickness (EOT= 11.2 nm) of our modulator.

Based on the capacitance and conductances at accumulation conditions we estimate a series resistance of 10 $10^8\Omega$ limiting our device to operate at low frequency (few MHz). A low modulation (MD=0.038 $\pm$ 0.008 $\%/\mu$m) showing capacitive behaviour is experimentally demonstrated. This results are in agreement with simulations considering the Soref formula for predicting the voltage-induced optical index changes in silicon. Furthermore it was proved with experiments that the modulation in our device is mainly due to electro-absorption effect. Finally, low energy consumption such as 6 fJ was demonstrated.

5.7 Conclusion

At the beginning of this chapter, we demonstrate (theoretically) that by using high-k dielectrics we are able to reduce the optical loss of the device while keeping the operation voltage constant. After that, we experimental demonstrate an electrical reliable high-k stack thanks to the use of thin Si_3N_4 as a diffusion barrier of copper.

Finally, the theoretical and experimental electro-optical behaviour of our device was investigated. Electro-optical tools for the understanding plasmonic field effect modulators were developed. Our modulators having capacitive signature and operates based on the electro-absorption effect. The single plasmon mode operation with combination of the low Si electro-optical effect results to low modulation depth devices. This results are in agreement with simulations when considering the Soref formula for predicting the voltage-induced optical index changes in silicon.

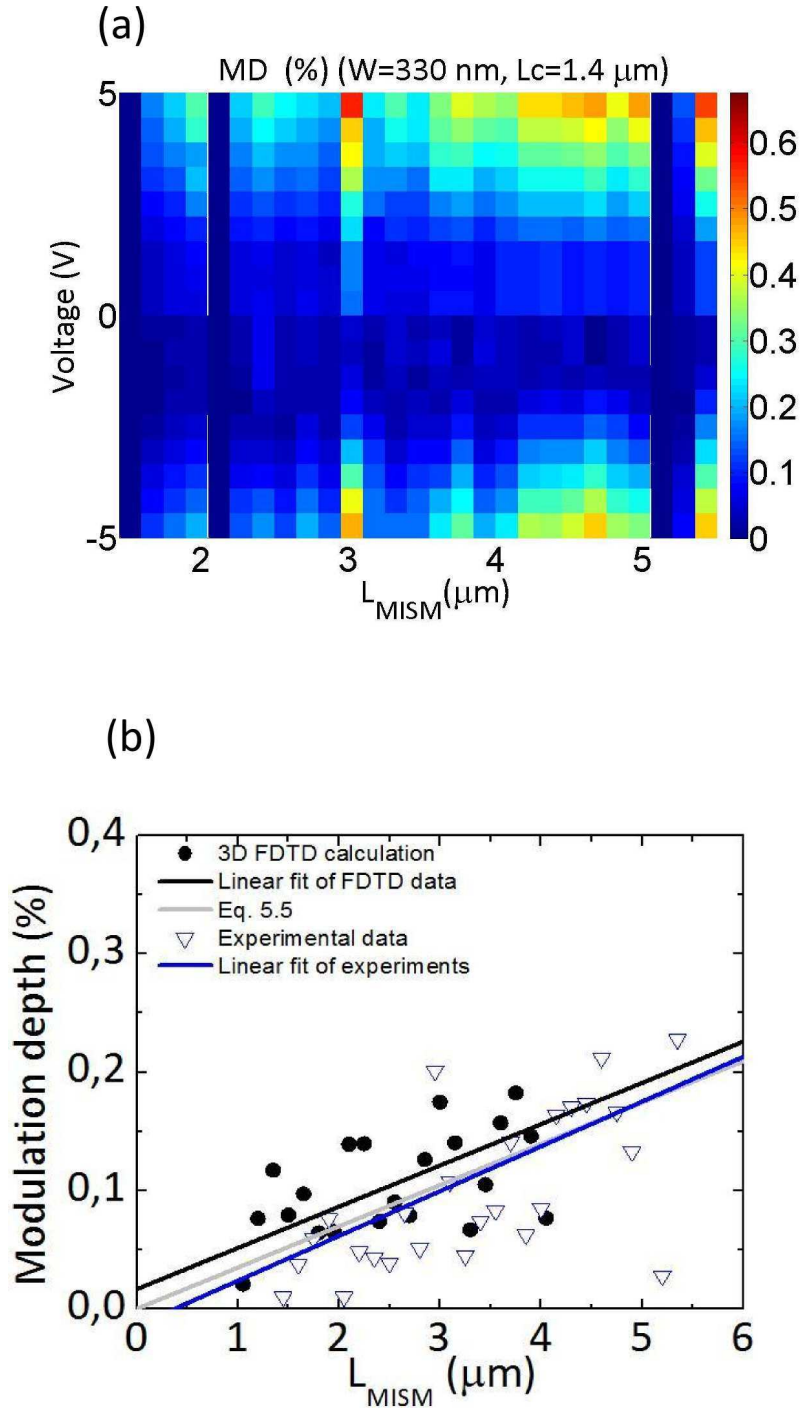

FIGURE 5.19 – *(a) Experimental modulation depth measured at 1 KHz; (b) Theoretical and experimental data of modulation depth at voltage of -3 V.*

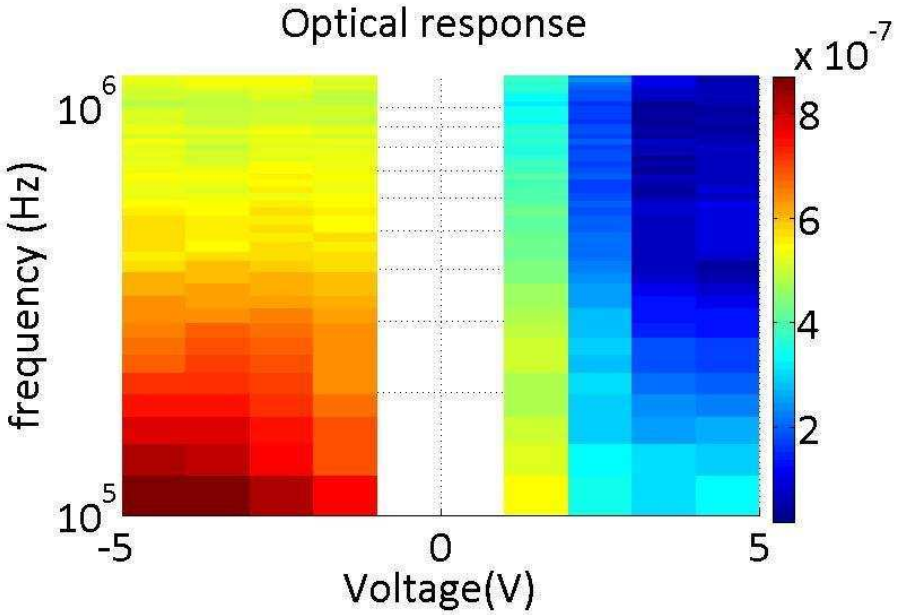

FIGURE 5.20 – *(a) Small signal optical response (data taken from the lock in amplifier) as a function of the voltage and the frequency*

Chapitre 6

General conclusion and perspectives

The thesis presents experimental and theoretical work, investigating the potential of CMOS integration of plasmonic modulator.

Chapter 1 is a general introduction to the work, where state of the art of Si technology and Si photonics is reviewed. Optical modulators and in particular plasmonic modulators based on MOS technology are presented.

Chapter 2 describes the experimental and numerical methods used to investigate the physical mechanisms underlying the operation of our copper based plasmon MOS modulators. These methods are adapted to the specifications of our device which is the use of copper as a metal contact and the single micron-scale dimensions of our devices. Finally an automated and reliable method is described for large scale electro-optical characterization system.

Chapter 3 describes the design and fabrication of a CMOS compatible MOS plasmonic modulator. Materials aspects are also extensively investigated.

Entering in more details, we first discuss the integration issues which face up with the fabrication of our plasmonic modulator. We proposed a MNOS stack for applications in electro-optical plasmonic devices, so that a very low optical losses and reliable operation is achieved. This objective is met thanks to a careful choice of materials, copper as a plasmon supporting metal and stoechiometric silicon nitride as a ultrathin diffusion barrier to the latter, and the use of fully CMOS compatible processes to integrate the

MNOS plasmonic waveguide within silicon photonics circuitry. Final reliability is above 95% for a 3 nm thick Si_3N_4 layer, leakage current density below 10^{-8} A.cm^{-2} and optical losses as low as 0.4 dB.μm^{-1} for a 13 nm thick insulator barrier, in agreement with the Cu ellispometric data. Furthermore, we note that the MNOS stack was fabricated using the same fabrication process of the MNOS capacitance described in subsection 3.2. The damascene technique appears particularly well suited for a high quality PWG fabrication as (i) the patterning of the metal is achieved thanks to well mastered and standard oxide/nitride etching steps, (ii) it prevents the absorbing copper oxide formation [55] at the interface where plasmon mode are propagating, and (iii) it uses a high temperature annealing of the metal which favors high material quality and extremely low optical loss SPP propagation. After demonstrating the MNOS as an appropriate structure for electo-optical CMOS plasmonics, we fabricate a vertical metal-insulator-Si-metal waveguide where the back metal was fabricated by flipping and molecular bonding of the original SOI wafer on a Si carrier wafer. The active device area varies from 1 to 6 μm^2, 1 μm wide and length varying from 1 to 6 μm. The aforementioned development was applied in order to realize efficient plasmonic coupler (Chapter 4) as well as active electro-optical modulator (Chapter 5).

Chapter 4 presents the experimental realization of an efficient and compact coupler between the Si waveguide (WG) and a vertical metal-insulator-silicon-metal (MISM) plasmonic WG fabricated using CMOS technology. This coupling scheme allowing insertion losses as low as 2.5 dB per coupler. This value is 3 times smaller compared to the case of direct coupling (without any MISI section). The significant improvement of coupling loss is attributed to the following reasons : (a) thanks to the use of the MISI section we gradually decreases the mode index, which reduces the phase mismatch between the Si-WG and the MISM-PWG and leads to less reflection loss(compared to the case without any MISI section) ; (b) the proposed coupler acts as a multimode interference region and therefore, working at the first peak of the oscillating behaviour we can benefit of an enhanced coupling. We demonstrate also that the dominant effect of the improved coupling is the MMI effect. Finally a comparison between the slab and the integrated

plasMOStor was performed, assuming that the lateral confinement and the materials restriction demanded by CMOS environment preventing the device from functioning as well as in the slab design.

Chapter 5 presents the electro-optical investigation of MOS plasmonic modulator. The interest of using high dielectric constant (high-k) materials, such as Al_2O_3 and HfO_2, in order to achieve an optimized MOS structure with low operation voltage and low optical losses, is demonstrated. After that, we experimental demonstrate an electrical reliable high-k stack thanks to the use of thin Si_3N_4 as a diffusion barrier of copper. Finally, the theoretical and experimental electro-optical behaviour of our device was investigated. Electro-optical tools for the understanding plasmonic field effect modulators were developed. Our modulators having capacitive signature and operates based on the electro-absorption effect. The single plasmon mode operation with combination of the weak electro-optical effect of Si, leads to low modulation depth devices.

Finally, an integrated electro-optical plasmonic modulator was demonstrated using standard CMOS technology on LETI platform. Fabrication of our modulator requires the use of both front-end and Cu back-end technologies, which are properly combined only a few nanometres one from each other. A careful choice of materials was done, copper as a plasmon supporting metal and stoechiometric silicon nitride as a diffusion barrier to the copper, in order to achieve low optical losses and electrical reliable operation. Furthermore, efficient and easy fabricated plasmonic couplers are demonstrated. Such couplers operates at 1.55 μm with a compact length of 0.5 μm and coupling loss of just 2.5 dB per facets. The electro-optical behaviour of the device was also investigated in detail. Devices show leakage current below 10 fA through the copper electrodes based MOS capacitors. The accumulation capacitance (few fF) was found to scale with the surface of the device, in consistent with the expected equivalent oxide thickness of the MOS stack of our modulator. We demonstrate low energy consumption devices, 6 fJ per bit, thanks to the low capacitance and the low operation voltage of our device. Finally, an electro-absorption (EA) modulation showing capacitive behaviour was experimentally demonstrated in agreement with simulations.

There are several questions remaining to be answered regarding the CMOS integration of Si based plasmonic modulators. In the following, we propose some experiments that could give new insights and better understanding with regards to the operation of CMOS plasmonic modulator. We also propose a new concepts for plasmon based modulators.

1. **Metal/Si ohmic junction**

   The back contact of the integrated plasmostor was fabricated using the Cu/TiN barrier scheme in order to protect the Cu diffusion inside the Si. However no consideration has been given to ensure the ohmic nature of TiN/Si junction. We note that by having ohmic contact, we eliminate the resistance of the TiN/Si junction and therefore allow devices to operate at high speed. We propose to fabricate Cu/TiN/Si junctions and by varying the doping concentrations of Si (p or n type) to tune the ohmic behaviour of this junction. This can be also experimental validated by performing resistance-voltage measurement.

2. **Experimental validation of the interest of using high "K" materials for low optical loss channel of plasmons**

   In chapter 5 we experimentally demonstrate the electrical reliability of a high-k insulator for Cu-based MOS capacitors. Furthermore, we prove by simulations that for a given level of electrical performance (i.e. EOT constant), high-k dielectrics could be interesting for low optical loss operation (Appendix 8). However, experimental validation is still required. We propose to use the recipe of the technology developed in chapter 3 in order to fabricate high-k MOS plasmonic waveguides. This would then be followed by optical transmission measurements in order to validate the results of simulations.

3. **Detail parametric study of the fabricated plasmostor**

   For this thesis, by using the CMOS technology we have fabricated several thousand devices of different geometries. By using the newly developed automatic experimental set up we can investigate trends that are related to the thickness of the silicon as well as the thickness of the insulator. Indeed as it is already demonstrated in

chapter 5 by reducing the oxide thickness (see Fig. 5.3) we are able to reduce the optical losses and at the same time to reduce the operation voltage.

Chapitre 7

Dispersion relation for Metal-Insulator-Silicon-Substrate waveguide

Dispersion relation for a Metal-Insulator-Silicon-substrate waveguide (M-I-S-Sub) is investigated and the results are reported in this chapter. The configuration of the investigated structure is shown in Fig 7.1.

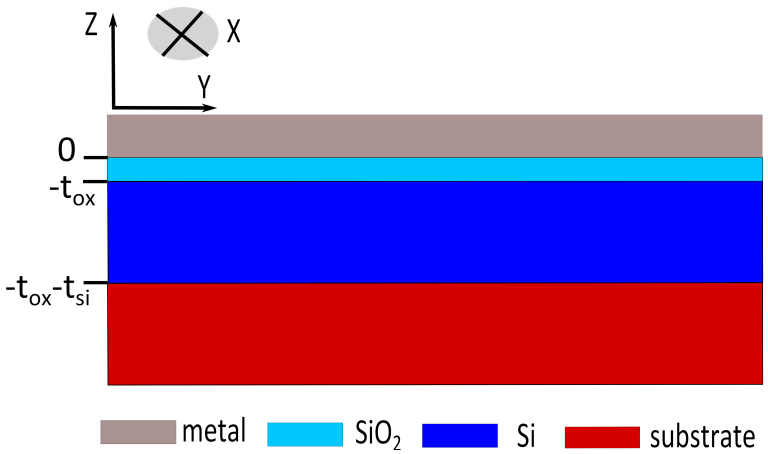

FIGURE 7.1 – *Generalized schematic of the semi-infnite metal-oxide-silicon-substrate waveguide.*

We wish to find solutions which satisfy Maxwell equations for a planar geometry. Assuming charge neutrality (ρ=0) and current density (J) to vanish we take the following form for the Maxwell equation :

$$\bigtriangledown \cdot E = 0 \tag{7.1}$$

$$\bigtriangledown \cdot H = 0 \tag{7.2}$$

$$\bigtriangledown \times E = -\partial B/\partial t \tag{7.3}$$

$$\bigtriangledown \times H = \partial D/\partial t \tag{7.4}$$

The type of solution that we are interesting correspond to plane wave propagates along a direction parallel to the boundary surfaces separating the different materials, which is define as the x direction. With z axis normal to these surfaces we further assume that there is no y dependence of any of the fields. In our analysis we assume that the propagation constant is the same in all layers and also all the materials are non magnetic and so that the magnetic permeability μ has been taken equal to 1. The Maxwell equations are supplemented under the constraint of tangential E, H fieldâĂŹs continuity at each boundary. Uniqueness of the results is guaranteed by Helmholtz theorem. For unpolarized waves in a four layer structure the electromagnetic fields take the form :

$$E(x,z,t) = (E_x\widehat{x} + E_y\widehat{y} + E_z\widehat{z})e^{i(k_x x - \omega t)} = ReF(z)e^{i(k_x x - \omega t)} \tag{7.5}$$

$$B(x,z,t) = (B_x\widehat{x} + B_y\widehat{y} + B_z\widehat{z})e^{i(k_x x - \omega t)} = ReF(z)e^{i(k_x x - \omega t)} \tag{7.6}$$

with E_y, B_x, B_z identically to zero for transverse magnetic (TM) polarization and E_x, E_y and B_y equals to zero for transverse electric (TE) polarization. The wave travels in the positive x direction so that Rek > 0 and Imk < 0. The Maxwell equation determines the fieldâĂŹs amplitude F(z) inside each material through ordinary differential equations as follows :

$$\frac{\partial^2 E}{\partial z^2} + (\epsilon_j \frac{\omega^2}{c^2} - k_x^2)E = 0, \qquad E_x(z) = -(\frac{i}{k})\frac{\partial E_z}{\partial z}, \qquad H_y(z) = (\frac{\omega\varepsilon_j}{ck_x})E_x \tag{7.7}$$

where

$$k_{z,j}^2 = (\epsilon_j \frac{\omega^2}{c^2} - k_x^2), \qquad j = m_1, ox, Si, sub \tag{7.8}$$

The different layers are composed of materials with complex dielectric constant ϵ_j and a wave vector k_{zj}. The field components in each layer may be written as :

$$E_z = A_1 e^{ik_{m1}z} \qquad for \;\; z > 0 \tag{7.9}$$

$$E_z = A_2 e^{ik_{ox}z} + A_3 e^{-ik_{ox}z} \qquad for \;\; z : [0, -t_{ox}] \tag{7.10}$$

$$E_z = A_4 e^{ik_{si}z} + A_5 e^{-ik_{si}z} \qquad for \;\; z : [0, -t_{ox}] \tag{7.11}$$

$$E_z = A_6 e^{ik_{sub}z} \qquad for \;\; z < 0 \tag{7.12}$$

Using the equation 1.7 we can estimate the tangential fields E_x and H_y. With these solutions in the various media, we have six arbitrary constants for the amplitude of the fields. There are also six boundary conditions that must be satisfied, namely, the continuity of the tangential fields E_x and H_y. Applying the boundary conditions we can write the resulting equation in the form :

$$G \cdot \psi = 0 \quad where \quad A = (A_1, A_2, A_3, A_4, A_5, A_6) \tag{7.13}$$

The matrix G is given by :

$$\begin{pmatrix}
\frac{k_{z,m1}}{k_x} & -\frac{k_{z,ox}}{k_x} & \frac{k_{z,ox}}{k_x} & 0 & 0 & 0 \\
0 & \frac{k_{z,ox}}{k_x} e^{-ik_{z,ox}t_{ox}} & -\frac{k_{z,ox}}{k_x} e^{ik_{z,ox}t_{ox}} & \frac{k_{z,Si}}{k_x} e^{ik_{z,Si}t_{ox}} & \frac{k_{z,Si}}{k_x} e^{ik_{z,Si}t_{ox}} & 0 \\
0 & 0 & 0 & \frac{k_{z,si}}{k_x} e^{-ik_{z,si}t_{sum}} & -\frac{k_{z,Si}}{k_x} e^{ik_{z,Si}t_{sum}} & \frac{k_{z,sub}}{k_x} e^{ik_{z,sub}t_{sum}} \\
\frac{\omega\varepsilon_{m1}}{ck_x} & -\frac{\omega\varepsilon_{ox}}{ck_x} & \frac{\omega\varepsilon_{m1}}{ck_x} & 0 & 0 & 0 \\
0 & \frac{\omega\varepsilon_{ox}}{ck_x} e^{-ik_{z,ox}t_{ox}} & \frac{\omega\varepsilon_{ox}}{ck_x} e^{ik_{z,ox}t_{ox}} & -\frac{\omega\varepsilon_{Si}}{ck_x} e^{-ik_{z,Si}t_{ox}} & \frac{\omega\varepsilon_{Si}}{ck_x} e^{ik_{z,Si}t_{ox}} & 0 \\
0 & 0 & 0 & \frac{\omega\varepsilon_{Si}}{ck_x} e^{-ik_{z,Si}t_{sum}} & \frac{\omega\varepsilon_{Si}}{ck_x} e^{ik_{z,Si}t_{sum}} & -\frac{\omega\varepsilon_{Sub}}{ck_x} e^{-ik_{z,Sub}t_{sum}}
\end{pmatrix}$$

where t_{sum}=t_{ox}+t_{Si}

In order to get non-trivial solutions for k_x, the determinant of the aforementioned matrix $G(k_x)$ needs to be zero ($\det(G(k_x))=0$ is the equation to be solved). G matrix is depending on the oxide thickness (t_{ox}) and the silicon thickness t_{Si}, the optical dielectric constant of the different materials ϵ_j and the excitation frequency ω. Hence the solution $k_x$will also depend on those parameters $k_x(t_{ox}, t_{Si}, k, \epsilon_j, \omega)$. In the 4 layers case considered here, the analytical solutions of this equation cannot be given.

Chapitre 8

Interest of high-k dielectris for Metal-Insulator-Silicon-Insulator active plasmonic devices

Hereafter, we demonstrate that by using high-k dielectric (Al_2O_3 and HfO_2) for a Metal-Insulator-Silicon-Insulator (MISI) plasmonic waveguide, we significantly reduce the optical losses without affecting the electrical performance of a MOS capacitor (i.e by keeping constant the EOT). This was achieved by carefully choosing the correct set of parameters such as EOT, t_{si} and nature of the high-k.

Following the procedure made on the chapter 5, the propagation length of the fundamental plasmonic mode is calculated for different Si thickness and EOT. The aim here it was to identify the set of parameters (EOT,tsi) in order to achieve an optimize structure operates at low voltage (or lower EOT) and low optical loss compared to the case of SiO_2. Fig. 9.13 shows the interesting range of EOT and thickness of Si (tsi) for having higher propagation length by using high-k dielectrics such as Al_2O_3 and HFO_2. In the following graphs we plot the "percentage changes in propagation length compared to SiO2" (A) as function of EOT and tsi. The quantity A is define using the following equation : $A = \frac{(propagationlength(Al_2O_3 or HFO_2) - propagationlength(SiO_2))}{propagationlength(SiO_2)}$. This equation shows

that when the quantity A is positive it means that the propagation length induced by high-k dielectrics is higher compared to the case of using SiO_2. Therefore for A>0 it is interesting to use high-k dielectrics for lower optical losses. For low operation voltage it is interesting to work with EOT thickness varying from 1 nm<EOT>10 nm. At this range, by using Al_2O_3 as a high-k insulator it is observed no significant gain (less than 10%) in propagation length of the fundamental plasmonic mode compared to the case of using SiO_2 of the same EOT. On the other hand, HfO_2 is identified as a promising insulator for active plasmonics since its use will increase the propagation length up to 60% for the aforementioned range of the EOT.

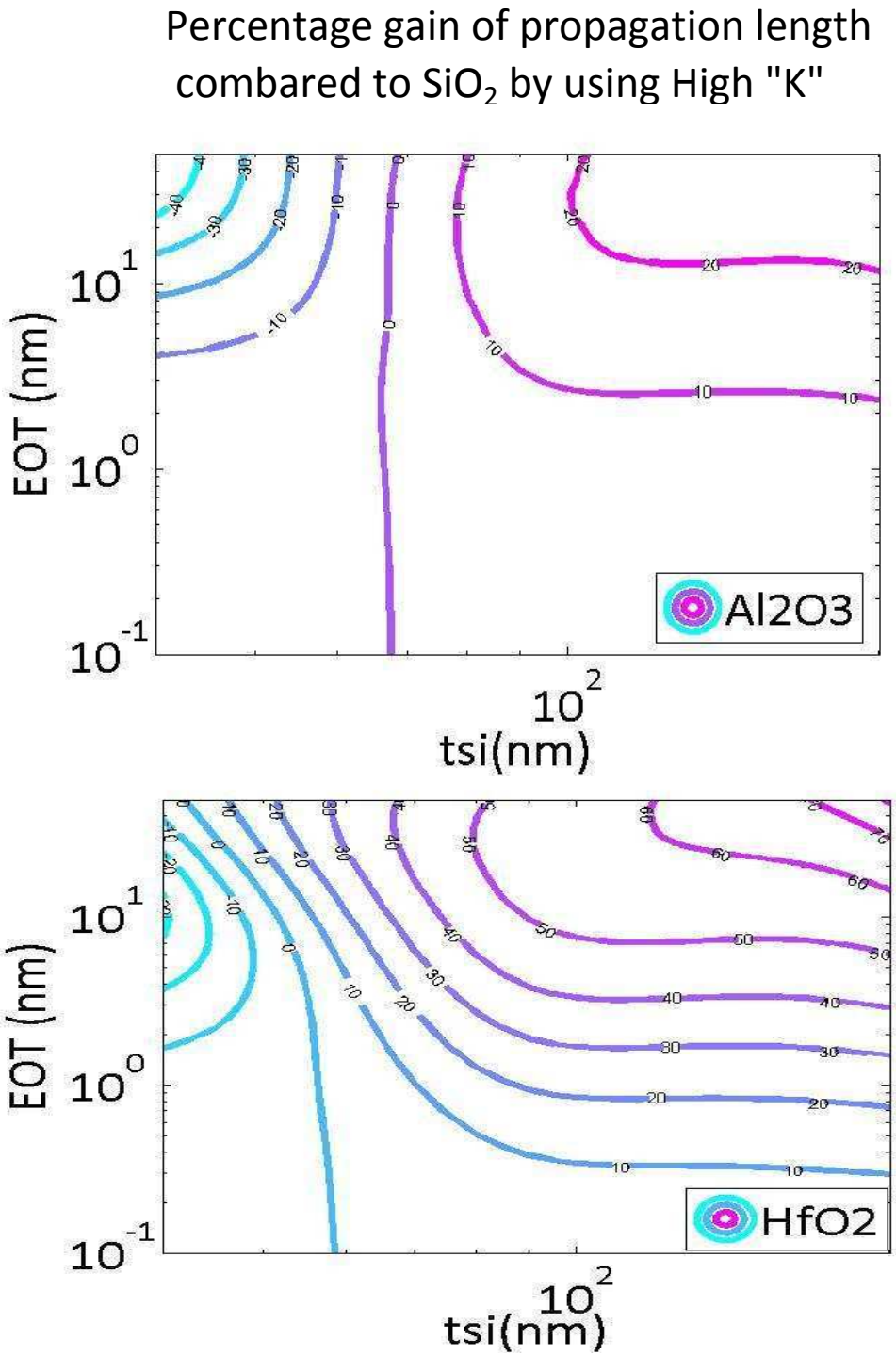

FIGURE 8.1 – *Percentage gain in propagation length (%) compared to the SiO_2 as a function of EOT and Si thickness when Al_2O_3 or HFO_2 are used.*

Chapitre 9

Résumé de THÈSE

9.1 abstract

Dans la réalisation de circuits intégrés hybrides électroniques - photoniques pour les réseaux télécom, les modulateurs intégrés plasmoniques pourront jouer un rôle essentiel de codage de l'information en signaux optiques. Cette thèse montre la réalisation d'une approche modulateur plasmonique à effet de champ, intégrée en silicium en utilisant les technologies CMOS standards. Ce modulateur MOS plasmonique présente diverses propriétés intéressantes, à savoir un confinement optique fort, permettant une augmentation de l'interaction lumière matière. Ces modulateurs plasmoniques permettent aussi de réduire l'inadéquation entre la taille des dispositifs en photonique Si et celle de l'électronique, ce qui permet d'envisager une convergence de leur fabrication en technologie VLSI sur une même puce. Le modulateur étudié dans ce mémoire repose sur l'accumulation de porteurs dans un condensateur MOS à grille cuivre intégré dans un guide d'onde en silicium, nécessitant aux technologies front end et back end Cu d'être combinés de quelques nanomètres l'une de l'autre. Nous présentons aussi de nouveaux designs pour injecter de la lumière à partir de guide d'onde SOI dans un guide à nanostructure plasmonique et les mesures d'une modulation électro-optique dans les structures MOS plasmoniques.

Mots-Clefs : technologie CMOS, plasmonique, photonique silicium

9.2 Introduction

Le chapitre 1 est une introduction générale au travail, où l'état de l'art de la technologie et de la photonique silicium est examiné. Les modulateurs optiques et en particulier des modulateurs plasmoniques basés sur la technologie MOS sont présentés. la technologie silicium est considérée comme la plate-forme idéale pour fusionner la photonique avec l'électronique à faible coût, à haut rendement. Dans cette plate-forme la réalisation de circuits photonique-électronique est fortement dépendante de la disponibilité de modulateurs optique à base Si qui utilisent l'interaction du signal électrique et optique. Les interconnexions optiques sont considérées comme la voie la plus prometteuse et innovante pour remplacer le bus de données électronique et résoudre ainsi le problème de consommation et de bande passante des interconnexions. Dans ce schéma prototype d'interconnexion, l'information transmise d'un point à un autre utilise des photons plutôt que des électrons et des fils de cuivre, avec un transfert de données qui devrait être de l'ordre de 50 gigabits par seconde et une consommation d'énergie largement inférieure à 1μJ/bit [18]. La percée d'une technologie basée sur la lumière nécessite un certain nombre de blocs de base tels que des lasers, des guides d'ondes optiques, des modulateurs et des photodétecteurs. La photonique sur silicium permet de faire face à ce défi en inventant des composants optiques de haute performance. La photonique sur silicium fait référence à la technologie qui développe des composants optiques haute performance à base de Si en prenant avantage des techniques et des matériaux compatibles CMOS utilisés dans le domaines de la micro-électronique. En tirant parti de cela ainsi que du développement de la technologie silicium sur isolant (SOI), nous sommes maintenant en mesure de transférer les connaissances et la technologie de l'électronique à base silicium afin de fabriquer des composants optiques compacts et à faibles coût rendant ainsi possible le développement des circuits photoniques intégrés à base de silicium.

La construction de ce système nécessite des composants élémentaires optiques tels que lasers, modulateurs, guides d'ondes optiques et photo-détecteurs pouvant être intégrés sur un wafer de silicium. Au cours des dernières années la plupart des efforts ont été

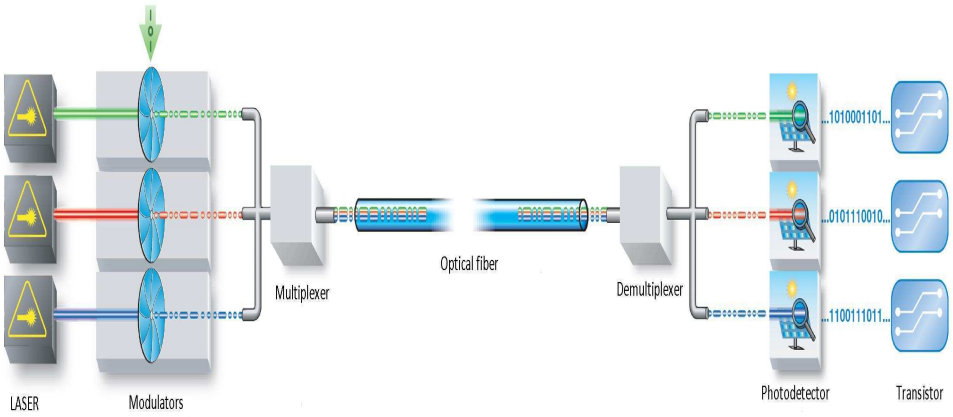

FIGURE 9.1 – *Les composants de base des circuits intégrés optiques [2]*

dirigés vers des dispositifs photoniques actifs tels que les lasers, les photodétecteurs et les modulateurs. Les questions cruciales portant sur ces éléments pour les applications intra-puces sont la consommation d'énergie et la surface du dispositif. Les modulateurs sont des dispositifs qui transforment un signal optique continu provenant de la source laser en un train d'impulsion discrète de lumière. La meilleure façon de réaliser une modulation de lumière est d'allumer et éteindre la source optique très rapidement (10 GHz) en modulant le courant d'injection (modulation directe). Cependant, cette approche implique des changements constants de la température ce qui conduit à une perturbation de la longueur d'onde de fonctionnement ce qui, à son tour, entraîne une distorsion des données optiques. En revanche une modulation externe offre l'avantage de transfert de données élevé (10 - 40 GHz) ainsi qu'une stabilisation de la longueur d'onde. Dans ce schéma, la source optique est de passer en mode continu et le travail modulateur externe tel que l'obturateur sur l'arrêt de la lumière continue. Par conséquent les modulateurs optiques externes devraient être l'élément clé pour pousser à la hausse des largeurs de bande et á la faible consommation d'énergie pour le transfert de données.

Deux principaux mécanismes sont utilisés pour atteindre la modulation de la lumière, à savoir l'électro-absorption et l'électro-réfraction. Le premier module l'amplitude de la puissance transmise et le dernier change la phase de l'onde. Les modulateurs à base

de silicium ont gagné beaucoup d'attention, avec plusieurs appareils rapportés avec des performances élevées. Ces dispositifs reposent sur l'effet de dispersion transporteur plasmatique libre [34] . Comme l'effet physique sous-jacent n'est pas fort, ces efforts ont conduit à de grandes structures (par rapport à celle du laser et un photodétecteur) avec une forte puissance d'entraînement pour obtenir une profondeur de modulation significative. Les modulateurs sont alors les plus grands (en ce qui concerne la taille) et les plus exigeants en termes d'énergie entre les composants optiques du circuit photonique intégrés. L'objectif de cette thèse est d'étudier un modulateur optique à l'aide de la plateforme photonique Si existant au CEA LETI, et diminuant sa taille et sa consommation d'énergie par l'utilisation de plasmons de surface.

En combinant les propriétés de propagation des ondes optiques avec la localisation des ondes électroniques haute, plasmons peuvent atteindre confinement du champ extrêmement large. Cette propriété de confinement peut être exploitée afin de développer de nouveaux dispositifs optoélectroniques tels que la détection [40], l'émission de lumière [41, 42], photodétecteurs [**?**] et modulateurs [44]. Le confinement du champ des plasmons de surface devrait être très utile dans le contexte de modulateurs. La sensibilité de l'environnement en métal / diélectrique d'interface modes PSP est bien connue et il est déjà utilisé pour différentes applications telles que la bio-détection et l'optiques des composants actifs. Différents schémas de base de SPP-modulateurs ont été proposées et signalé jusqu'ici. Fondamentalement, on peut identifier trois types de modulateurs du PSP ; (i) modulateurs tout-optique spp (ii)modulateurs thermo-optique , et enfin (iii) les modulateurs électro-optique. Parmi les nombreux brevets et publications décrivant les modulateurs optiques plasmonique, très peu ont la possibilité d'être compatible avec les procédés CMOS [53, 6]. Le dispositif PlasMOStor soi-disant proposé par Dionne et al. [6] utilise le Si comme matière active afin de moduler la lumière dans un plan vertical de la configuration Ag / SiO_2 / Si / Ag .

Le PlasMOStor est une configuration interférométrique utilisé pour effectuer une modulation. Le dispositif utilise une structure de quatre couche d'Ag-oxyde-silicium-Ag qui prend en charge les deux modes photoniques et plasmonique . Dans ce dispositif

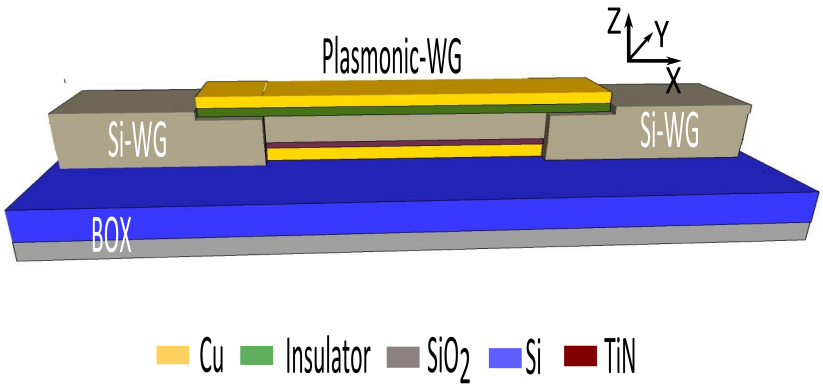

FIGURE 9.2 – *plasMOStor intégré sur plateforme SOI*

électro-optique, la modulation est réalisée par le changement de l'indice d'une couche dopée n de silicium au moyen d'accumulation de charges dans une structure MOS. Une telle variation de l'indice est à l'origine de la disparition d'un mode hybride photonique excité à une fréquence proche de sa coupure. La perturbation du battement créée par l'interférence du mode photonique et un mode plasmonique crée une modulation du signal optique transmis à une profondeur dans la plage de 3 à 4 dB dans un dispositif de 2,6 μm de long. Pour intégrer ce modulateur sur la plate-forme CMOS du Leti, nous profitons des atouts majeurs de la technologie de la microélectronique et de la photonique Si , à savoir la maturité et la faible perte à long terme de circuits optiques (développé pour la photonique CMOS) et la technologie de fabrication bien connu des métaux (développé pour la microélectronique) pour les deux appareils électroniques (électrodes) et les buts de la photonique (concentration électromagnétique). La preuve expérimentale d'une telle approche apporterait un nouveau paradigme dans la conception de modulateurs électro-optiques. La Fig. 9.2 montre schématiquement le plasMOStor intégré constitué de silicium sur isolant (SOI) guide d'ondes intégré avec un guide d'onde plasmon MOS (plasMOStor).

9.3 Méthodes expérimentales et numériques

Dans ce chapitre, nous aborderons les méthodes de caractérisation électrique et optique qui sont utilisées pour étudier les mécanismes physiques sous-jacents au fonctionnement de notre modulateur MOS á base de plasmons sur cuivre . L'utilisation du cuivre pour les électrodes de contact est un élément important de cette étude. D'un point de vue plasmonique, la faible résistivité électrique DC de cuivre peut conduire à une perte de propagation faible. Cependant, sans l'utilisation d'une couche d'interface métal-diélectrique, pendant le recuit, le cuivre peut rapidement se diffuser dans les couches diélectriques [56], dégradant sensiblement les performances du dispositif.

Afin de caractériser électriquement l'empilement MOS et en particulier l'effet de diffusion du cuivre et de la performance d'une barrière de diffusion entre les couches, un large éventail de techniques électriques ont été utilisés (capacité-tension (CV), conductance-tension (GV) et réponse á une fonction rampe linéaire (Linear Ramp Voltage Stress, LRVS)). La réponse capacitive CV peux donner un aperçu sur les paramètres clés tels que l'épaisseur équivalente de SiO_2 du diélectrique (EOT) et la tension de bande plate V_{fb} . L'extraction de ces paramètres est essentiel dans cette thèse afin d'estimer le champ de claquage à travers l'isolant. De plus, par l'estimation de la V_{fb} nous pouvons extraire des informations sur les défauts à l'intérieur de l'isolateur. Enfin, les mesures CV peut donner à la concentration de porteurs pour une large plage de tensions. L'extraction de cette quantité peut être utilisé pour la précision électro-optiques des simulations. La méthode standard de la conductance GV développé par Nicollian et al. [7] a été utilisé pour étudier les états d'interface électriquement actifs á l'interface SiO_2 / Si. Enfin, le champ de claquage maximal de l'isolant a été estimée en utilisant la contrainte de tension linéaire de rampe (LRVS). Cette technique est largement utilisée pour étudier la qualité de l'isolant. L'intérêt de l'expérience LRVS est d'être très rapide et de fournir des informations intrinsèque ainsi qu'extrinsèque sur le comportement de claquage de notre dispositif [58] .

La compréhension du comportement électrique de nos dispositifs MOS a été améliorée

grâce à l'utilisation de simulations numériques obtenus en utilisant soit SILVACO, un logiciel commercial, ou code interne ÂńLe simulateur" [57]. Un programme de simulation, "Le simulateur", est développé au LETI [67] pour modéliser la distribution de charge à l'intérieur du silicium en tenant compte des effets de la mécanique quantique. Le comportement électrique d'un condensateur MOS est modélisé aussi á l'aide d'un dispositif de simulation en deux dimensions à partir du package ATLAS de SILVACO. L'intérÃłt de l'utilisation du logiciel est d'extraire le profil de la distribution et la densité de porteurs à l'intérieur du silicium. Il est à noter que l'extraction précise de ces paramètres est essentielle parce qu'elle sert finalement á définir la force de l'interaction électro-optique qui est en relation avec l'exécution électro-optique du dispositif (profondeur de modulation).

Après la caractérisation électrique, des mesures optiques ont été effectués. Les résultats des mesures de transmission expérimentale ont été interprétés en conjonction avec la FDTD 3D, des simulations et des méthodes analytiques développées spécifiquement pour cette étude, afin de comprendre le comportement optique des dispositifs. Puisque nous nous intéressons à calculer les modes optiques au régime de coupure, une solution analytique sera plus précise par rapport à celles numériques. Par conséquent, un solveur de mode analytique optique est développé et est expliqué.

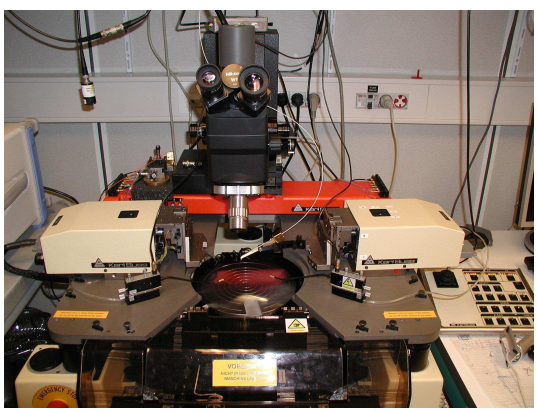

FIGURE 9.3 – *Image du montage de mesure de la modulation.*

Enfin, nous décrivons un système fiable automatisé à grande échelle du système de caractérisation électro-optique qui a été développé pour tester les propriétés optiques

de transmission, caractéristiques courant-tension et la profondeur de modulation induite électriquement pour un grand nombre de dispositifs. Ce système a été spécifiquement adapté pour les mesures de dispositifs à l'échelle du micromètre. Les mesures de transmission optique à travers nos dispositifs ont été réalisées en utilisant des diodes électroluminescentes (LED) ou un laser comme source optique de longueur d'onde centrée sur 1550 nm. La puissance de sortie a été couplée en polarisation TM dans les guides d'ondes photoniques à travers des coupleurs réseau en utilisant une fibre monomode. Une station automatique Karl Suss wafer level a été utilisé pour mesurer les échantillons sur le wafer. Une méthodologie pour l'extraction automatisée et fiable de la profondeur de modulation, de transmission optique et courant de fuite sous polarisation appliquée a été mis en oeuvre pour le test au niveau du wafer. Le dispositif expérimental a été conçu pour mesurer la modulation de largeur de bande de notre modulateur optique. Un laser accordable, et un dispositif d'émission de lumière (LED) sont tous deux utilisés pour exciter le dispositif par une source optique continue. Les sources optiques sont interfacés avec les fibres monomodes. La puissance de sortie est recueilli par des fibres multimodes et transformé en énergie électrique par une photodiode à grande vitesse. L'alignement des fibres a été réalisé sur un guide d'onde de référence pour maximiser la transmission optique. Enfin le signal de sortie est ensuite mesurée en utilisant soit un compteur de puissance quand la mesure de transmission optique est effectué ou une détection synchrone lorsque la profondeur de modulation est estimée.

9.4 Integration CMOS d'un modulateur plasmonique MOS

Le chapitre 3 du manuscrit décrit la conception et la fabrication d'un modulateur MOS compatible CMOS plasmonique. Les aspects des matériaux sont également largement étudiés.

Dans ce chapitre, nous étudions les aspects matériels et les étapes technologiques nécessaires pour réaliser un plasMOStor intégré [10] dans l'environnement CMOS. La conception actuelle du plasMOStor plan [10] s'appuie sur une configuration de couplage

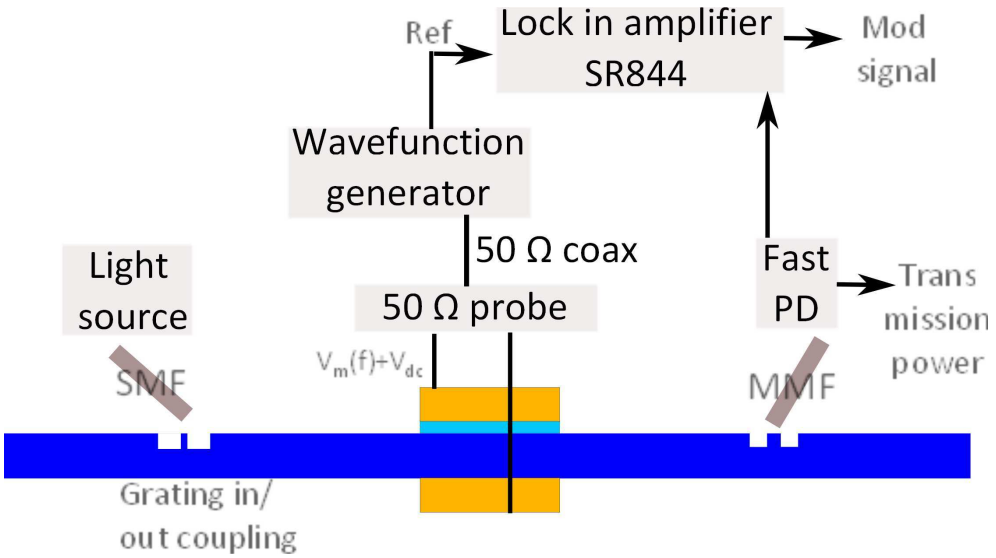

FIGURE 9.4 – *Experimental set up used for measuring the bandwidth of the device (up to 200 MHz)*

verticale, toutefois, des dispositifs avec un couplage dans le plan du guide d'ondes ont été réalisés, comme étant plus proche de l'intégration VLSI au LETI. En outre, dans le plasMOStor, de l'argent est utilisé comme une électrode métallique, qui est contaminant dans l'environnement CMOS. Il n'y a pas non plus de considérations relatives à la couche interfaciale qui est d'une importance particulière pour les appareils de haute fiabilité. Dans ce qui suit, nous étudions à la fois le choix du métal et la couche interfaciale en termes de compatibilité CMOS à faible perte optique et électriques pour un grand nombre de dispositifs.

Il a été démontré récemment [55] que les pertes optiques de plasmon se propageant à la surface des couches Cu préparés dans les fonderies CMOS sont faibles et en accord avec les résultats d'éllipsométrie. A partir de cette simple comparaison, nous concluons que le cuivre est le meilleur choix pour les appareils plasmoniques en termes de pertes optiques. Il est également technologiquement pertinent, tout comme Al a été progressivement remplacé par Cu dans nos jours dans les interconnexions électriques [75] . Cu est donc le métal le plus prometteur pour l'intégration de dispositifs de plasmon dans un

environnement CMOS, et sera considéré ci-dessous comme une métallisation du guide d'ondes MOS. Cependant, avec le choix de Cu comme électrode en métal, nous devons être prudents sur le choix de la couche interfaciale entre le cuivre et l'isolant ou semiconducteur. Dans la section suivante, nous montrons l'utilisation de couches minces Si_3N_4 comme une barrière efficace pour bloquer la diffusion du cuivre et à faible perte optique.

Nous faisons la promotion d'un métal hybride de l'empliment nitrure-oxyde-silicium (MNOS) pour dispositifs actifs CMOS plasmonique. Cet empilement de silicium fortement dopé comme un métal a déjà été largement étudié dans la microélectronique pour les transistors à haute fiabilité et à des échelles très agressives [83]. Toutefois, la fiabilité de cette empilement par exemple n'a jamais été étudiée lorsque Cu est le métal de grille, tel que requis pour les dispositifs CMOS plasmonique. Nous démontrons expérimentalement qu'une couche ultrafine de Si_3N_4 (3 nm) stoechiométrique peut satisfaire aux exigences ci-dessus comme barrière de diffusion dans les dispositifs MOS à base optoélectronique utilisant des plasmons et de fournir des performances de haute fiabilité. Le Cuivre agit essentiellement su la fiabilité de la capacité MOS. Les condensateurs MOS présentent les caractéristiques de claquage électrostatique extrinsèques , avec un comportement de court circuit précoce (E $<$ 1 MV.cm-1) se produisant pour 40% des dispositifs. A l'inverse, 95% de condensateurs MNOS incluant un mince nitrure stoechiométrique supplémentaire Si_3N_4 ont un champ de claquage supérieure à 10 $MV.cm^{-1}$, sans aucun signe de comportement extrinsèque. Le comportement extrinsèque du claquage est souvent associée à des défauts ponctuels à l'intérieur de l'isolateur [58] , qui dans notre cas peuvent provenir de la diffusion de Cu dans l'oxyde [16, 87].

Ces résultats ouvrent la voie vers la haute performance et faible coût de fabrication de dispositifs plasmoniques actifs au sein de fonderies CMOS. Le développement ci-dessus a été appliquée afin de réaliser efficacement un coupleur plasmonique (chapitre 4) ainsi que modulateur actif électro-optique (chapitre 5). La structure du modulateur intégré plasmonique est schématisé. Le dispositif est fabriqué sur des wafer de silicium-sur isolant (SOI) avec guide d'onde SOI siégeant en tant que moyen de propagation de la lumière. La lumière polarisée TM est couplée dans des guides d'ondes photoniques par

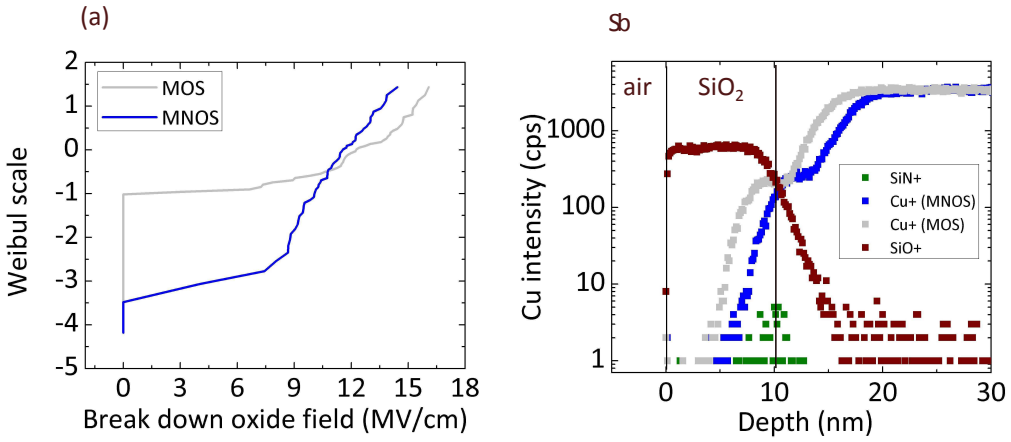

FIGURE 9.5 – *(a) la fiabilité partielle expérimentale (à l'échelle de Weibull) du claquage ; (b) la mesure SIMS de la profondeur de profil de l'intensité de cuivre pour des empilements MOS et MNOS*

coupleurs réseau. Quand la lumière se propage à travers la région active (plasMOStor), il couple dans un mode plasmonique. La figure ? ? montre une vue de dessus schématique du plasMOStor intégrée, avec toutes les composantes majeures indiqué. Le plasMOStor se compose d'un guide d'ondes métal-isolant-Si-métal où le métal de retour a été fabriqué par collage moléculaire flip-chip de la plaquette d'origine sur une tranche SOI support de Si. La zone de dispositif actif varie de 1 à 6 μm^2, 1 μm de large et de longueur variant de 1 μm à 6 μm.

9.5 Couplage efficace de la lumière d'un guide silicium vers le plasMOStor intégré

Le guide d'ondes MISM hybride plasmonique (PWG) est d'un intérêt particulier pour la plasmonique actifs CMOS, car il permet la propagation des modes très confinés dans la région de l'isolant [10] et peut potentiellement être intégrées dans les fonderies de l'électronique à base de Si (chapitre 3). Cependant, ces structures plasmoniques souffrent à la fois de perte en mode importante (en raison de la génération de fort champ électrique)

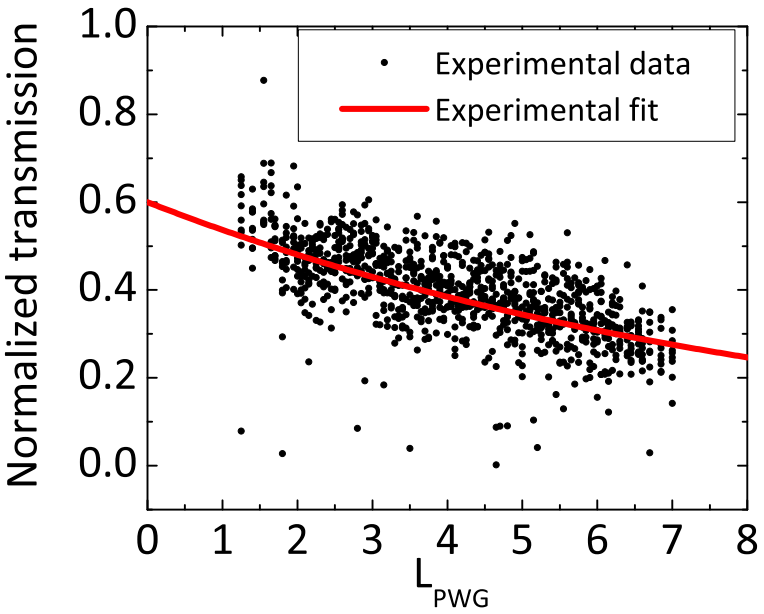

FIGURE 9.6 – *Transmission optique normalisée de données expérimentales en fonction de* L_{GATE}.

et de perte d'insertion élevé. Le premier peut être résolu par le choix des matériaux car il est déjà discuté dans le chapitre 3. Considérant ce dernier, nous notons que la fine ligne de jonction et la différence de taille entre la norme de Si-photonique GT et le GT MISM conduit à des pertes préjudiciables [13] pour le cas symétrique, $L_c = 0$. Lorsque le mode incident (I) dans la liaison Si-GT atteint la jonction Si-WG/MISM, une partie de la puissance est couplé au mode MISM bien qu'il est observé qu'une partie de celui-ci, est perdue à la réflexion et par diffusion. Ce dernier est attribuée à la fois à l'index et au recouvrement entre les profil de champ de modes supportés les deux guides d'ondes couplés. Afin d'améliorer le couplage de la lumière à partir d'un Si-GT à un PWG, nous devons maximiser le recouvrement du mode incident avec le mode couplé et aussi minimiser le décalage de mouvement entre ces modes. Les configurations de couplage sont nombreuses dans la littérature : coupleurs bout à bout, les coupleurs coniques et

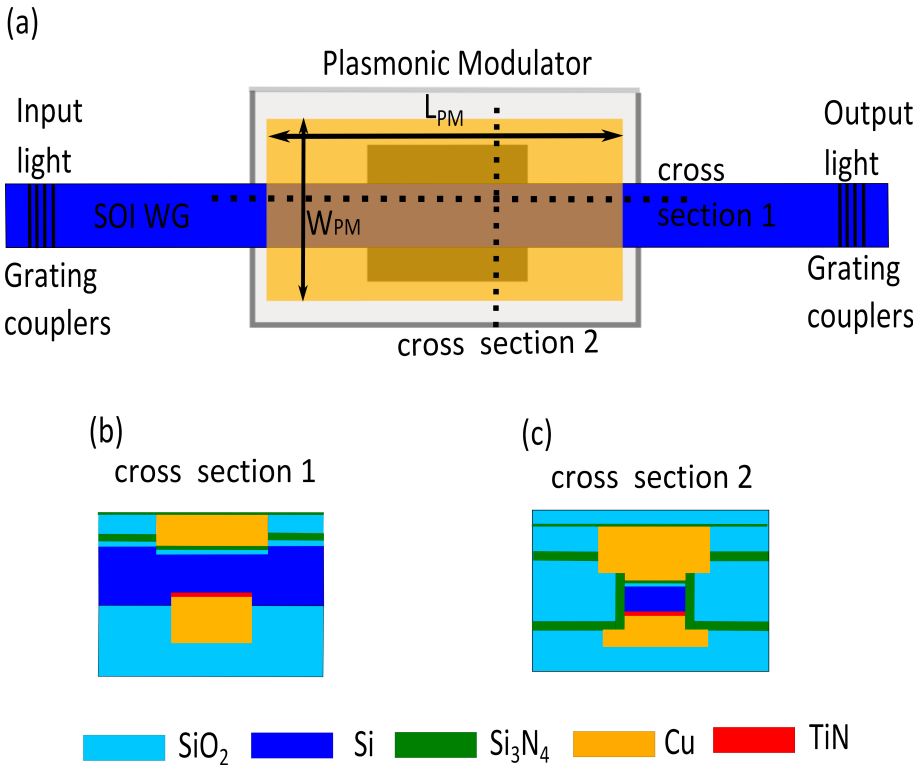

FIGURE 9.7 – *Schéma vue de dessus du modulateur intégré plasmonique (a) avec coupe transverse à des plans différents ; et (b) section transversale dans la direction de propagation (c)section transversale dans la direction perpendiculaire.*

coupleurs directionnels.

Le chapitre 4 présente la réalisation expérimentale d'un coupleur efficace et compact entre le guide Si (GT) et un empilement vertical métal-isolant-silicium-métal (MISM) plasmonique fabriqué en utilisant la technologie CMOS. Le coupleur est constitué de métal-isolant-silicium-isolant (MISI) la structure qui a été insérée entre les deux guides d'ondes mentionnés ci-dessus. Le principe de fonctionnement des coupleurs proposées est régi par les effets d'interférence multimode. En outre, la section MISI diminue progressivement l'indice de mode, ce qui réduit le décalage de phase entre le Si-GT et le MISM-PWG et conduit à moins de diffusion et de perte par réflexion (par rapport au cas sans modification de section MISI). Nous démontrons que ces coupleurs fonctionne

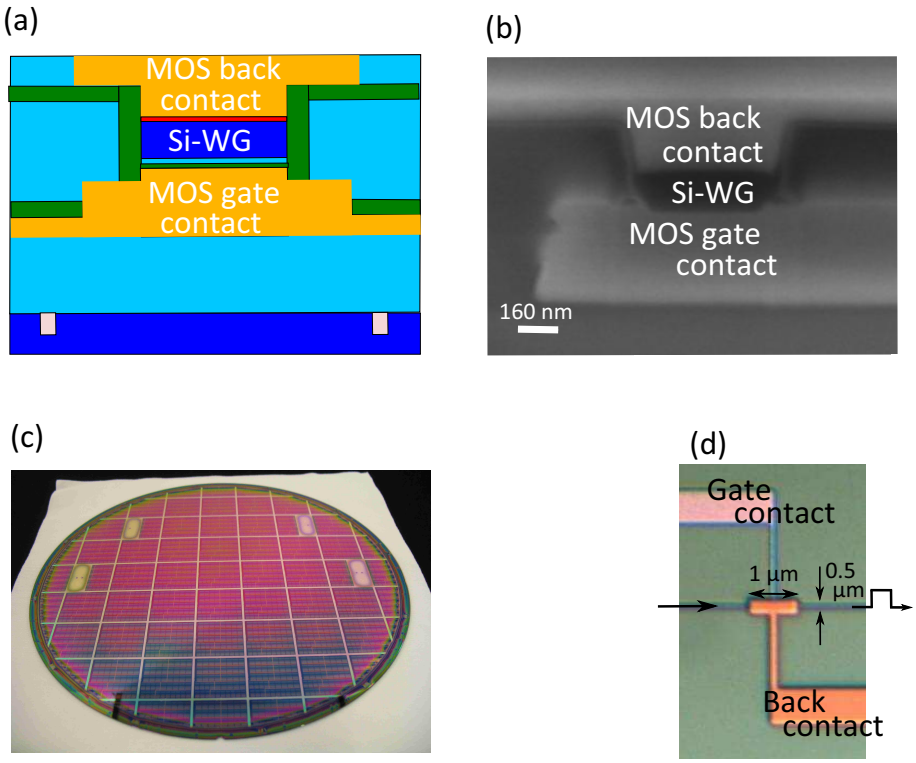

FIGURE 9.8 – *(a) Schéma et (b) section transversale MEB de la structure finale ; (c) Vue de dessus de wafer de 200 mm, incluant plus de 30000 dispositifs ; (d) vision binoculaire supérieure d'un dispositif en indiquant les éléments importants ;*

à 1,55 μm et la géométrie de plus grande efficacité correspond à une longueur compacte de 0,5 *mu* m avec des pertes de couplage de seulement 2,5 dB par facettes. Cette valeur est 3 fois plus petite par rapport au cas de couplage direct (sans la section MISI). La structure entière est fabriquée en utilisant un procédé CMOS compatible disponible au CEA-LETI. Des calculs FDTD-3D sont également exploités dans le but de simuler nos coupleurs plasmoniques. Les résultats expérimentaux et de simulation sont en accord, illustrant que la géométrie de plus haute efficacité correspond à un coupleur compact de 0,5 μ m de longueur ayant une perte de couplage de seulement 2,5 dB par coupleur (valeur expérimentale). Les pertes d'insertion expérimentale et théorique sont comparées pour des longueurs de couplage différents, L_c. A l'instar des mesures expérimentales, la perte d'insertion théorique a été déterminée à partir de simulations FDTD. A partir des

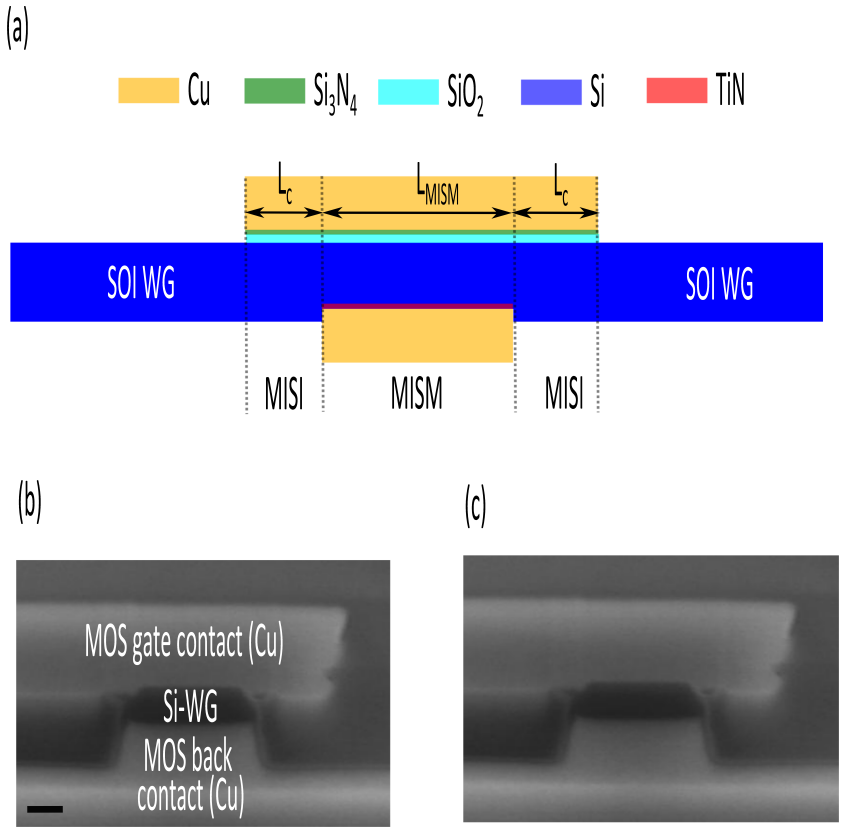

FIGURE 9.9 – *(a) Schéma de guide d'ondes hybride plasmonique montrant la structure de couplage (MISI) reliant le guide d'onde SOI et MISM. (b) l'image SEM de la section transversale de la structure MISM. (c) images MEB des coupleurs en vue de dessus*

dispositifs fabriqués, nous constatons qu'une longueur de couplage optimal de 0,5 μm en une perte d'insertion de 2,5 dB. En fonction de L_c, la perte d'insertion mesurée suit la même tendance que les valeurs calculées, avec un décalage d'environ 1 dB pour les dispositifs fabriqués que nous attribuons à la perte de propagation supplémentaire causée principalement par des interfaces métal-diélectriques imparfaites dans le régions de couplage MISI.

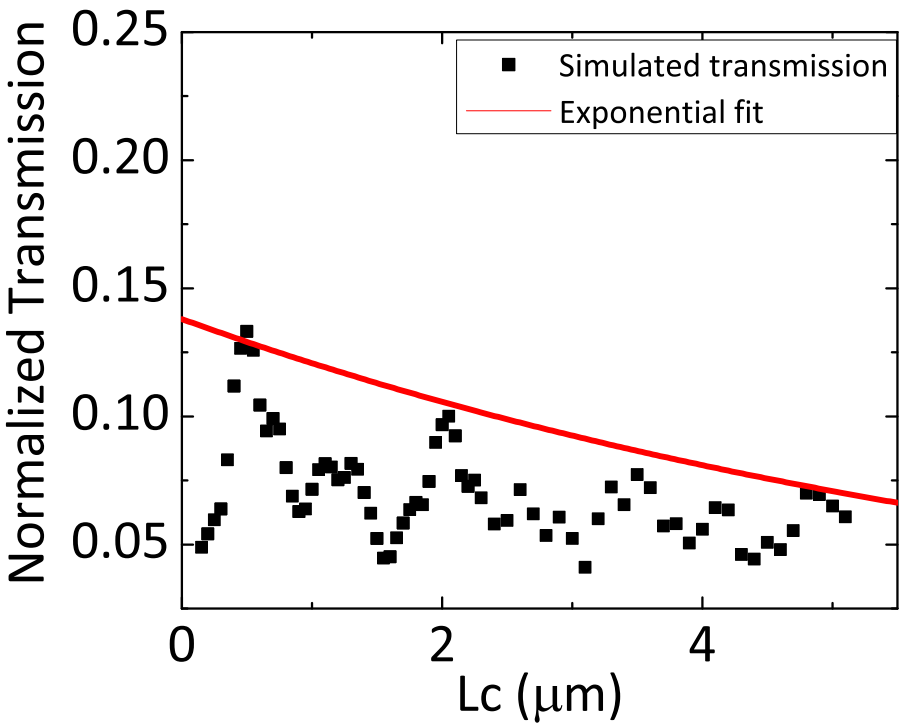

FIGURE 9.10 – *Transmission simulé pour le couplage des longueurs L_c différentes et $L_{MISM} = 1\ \mu m$.*

9.6 Etude électro-optique sur le Modulateur plasmonique MOS intégré

Le chapitre 5 présente l'étude électro-optique de modulateur MOS plasmonique. L'intérêt d'utiliser des matériaux à haute constante diélectrique (high "K") , tels que Al_2O_3 et HfO_2, est de parvenir à une optimisation de la structure MOS avec une tension de fonctionnement basse et de faibles pertes optiques, est démontrée. Les modulateurs plasmoniques, sur la base de la configuration du MOS, utilisent des diélectriques non seulement comme un isolant électrique, mais aussi comme un canal optique pour les plasmons de surface. Par exemple, comme indiqué dans l'empilement MOS du plasmostor [10] ,

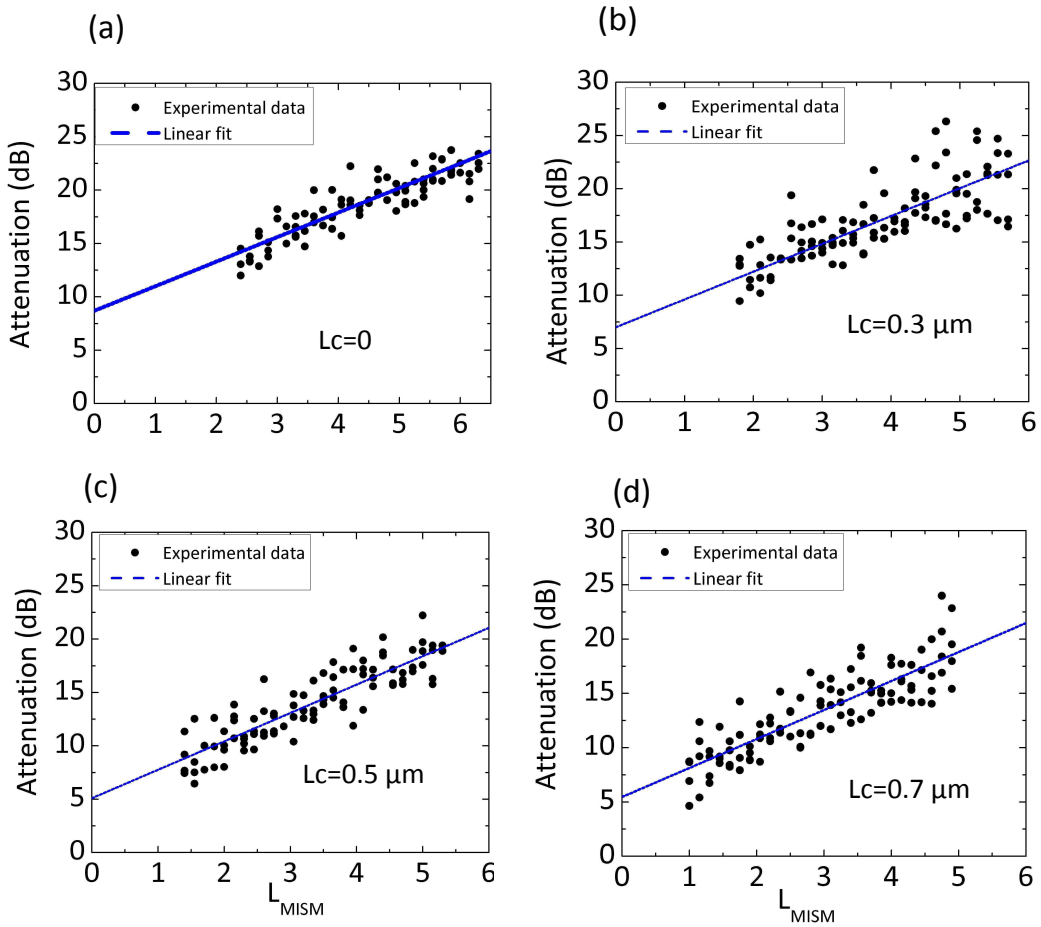

FIGURE 9.11 – *Mesure de l'atténuation expérimentale en fonction de la longueur MISM (L_{MISM}) pour les longueurs de couplage différents : (a) symmetric (L_c= 0 µm), (b) L_c=0.3 µm ; (c) L_c=0.5 µm ; (d) L_c=0.7 µm.*

l'isolateur de grille agit non seulement en tant que guide d'ondes plasmons mais aussi comme un isolant électrique de la grille de contact. De plus, par rapport à des propriétés électriques, un modulateur MOS plasmonique est un dispositif capacitif lorsque la tension de fonctionnement dépend à la fois l'épaisseur et la constante diélectrique de l'isolateur, et l'EOT de la MOS. L'impact de l'épaisseur et de l'indice optique différent des couches isolantes sur les pertes optiques a été étudié pour la plasmonique MOS guide d'ondes avec l'aide du mode solveur décrit dans le chapitre 2. Ce guide d'ondes est constitué d'une

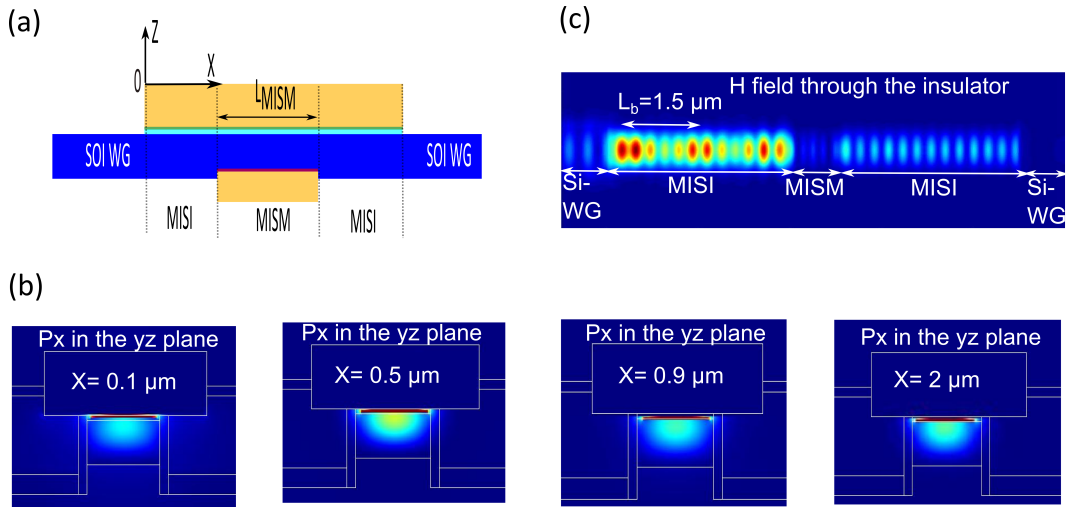

FIGURE 9.12 – *(a) vue en coupe de la structure recherchée dans la direction de propagation ; (b) l'intensité du champ (b) par l'intermédiaire du dispositif de trou (direction x) à partir d'un moniteur placé dans l'isolant de grille de l'empilement (c) intensité de puissance dans la direction de propagation (Px), dans des sections transversales différentes de l'empilement MISI (X= 0.1 µm, X= 0.5 µm, X= 0.9 µm, X= 2 µm).*

à quatre couches Cu-Isolant-Si-substrat de guide d'ondes. L'épaisseur de l'isolant (t_{ins}) varie de 3 nm à 40 nm. Un autre paramètre qui affecte les pertes optiques du dispositif est l'épaisseur de Si-GT. Il a été constaté que grâce à un réglage correct de l'épaisseur SiWG nous pouvons réduire encore plus la perte optique du mode fondamental plasmonique.

Enfin, le comportement théorique et expérimentale électro-optique de notre dispositif a été étudiée. Des outils électro-optiques pour la compréhension plasmoniques du modulateurs à effet de champ ont été développés. En ce qui concerne le fonctionnement électrique, les paramètres intéressants pour un modulateur MOS sont le taux de la concentration des porteurs dans le régime d'accumulation ainsi que la distribution spatiale de ces porteurs à l'intérieur du silicium. L'objectif à ce moment-là est de classer notre modulateur en électro-réfraction (le principe de fonctionnement est basé sur les changements de la partie réelle de l'indice de réfraction) ou en électro-absorption (le principe de fonctionnement est basé sur les changements de la la partie imaginaire de l'indice de réfraction de

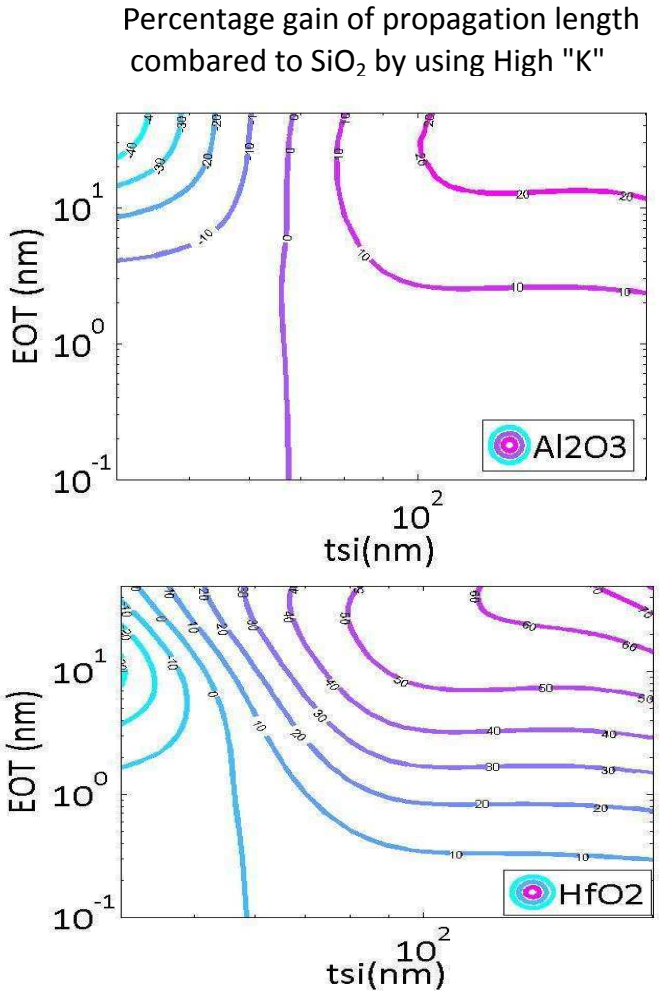

FIGURE 9.13 – *Pourcentage de gain en longueur de propagation (%) par rapport à la SiO_2 en fonction de l'EOT et l'épaisseur de Si lorsque Al_2O_3 ou HFO_2 sont utilisés. Pour une tension de fonctionnement faible, il est intéressant de travailler avec une épaisseur variant de 1 EOT nm < EOT < 10 nm. A cette distance, en utilisant Al_2O_3 comme une grande "K" isolant, il est observé aucun gain significatif (moins de 10 %) en longueur de propagation du mode fondamental plasmonique par rapport au cas de l'utilisation de SiO_2 de l'EOT même. D'autre part, HfO_2 est identifié comme un isolant prometteur pour la plasmonique actifs depuis son utilisation va augmenter la longueur de propagation jusqu'à 60 % pour la plage précitée de l'EOT.*

l'indice). Nous allons considérer une situation de fonctionnement en mode unique, seul le mode fondamental plasmonique est pris en charge par la empilement plasmostor intégré. Sur cette base, la seule façon d'envisager l'ER est de supposer que nous avons une perte de Fabry-Pérot. Nous vérifions cette hypothèse à l'aide de simulation FDTD-3D de la zone par deux différentes expériences numériques dans un dispositif asymétrique avec du métal de grille étendue de L $_c = 0{,}7$ mu m . nous avons montré que l'EE est le seul effet qui définit la profondeur de modulation de notre dispositif.

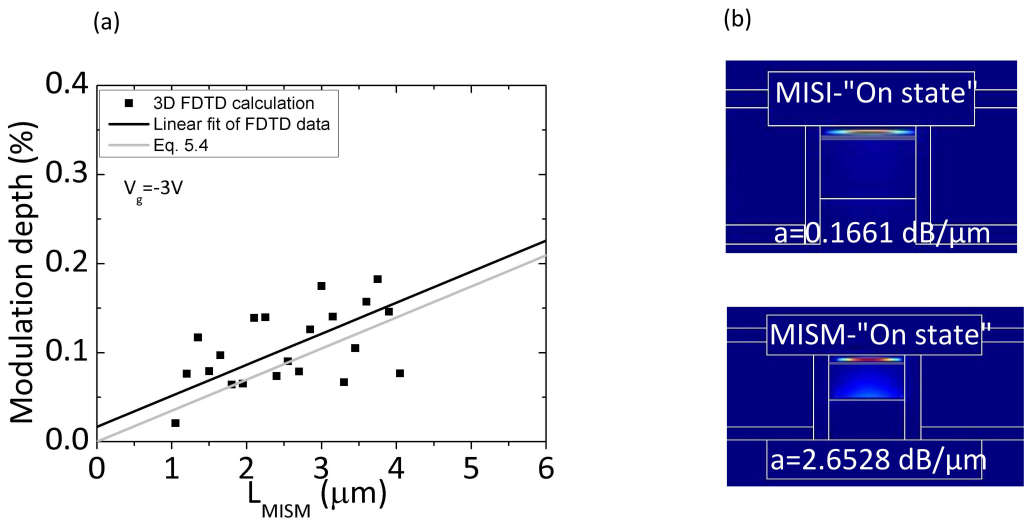

FIGURE 9.14 – *(a) Taux de modulation estimée par des simulations FDTD 3D, l'analyse du mode (b) de l'état sur les modes fondamentaux soutenus par l'article MISI et MISM*

Nos modulateurs ont une signature capacitive et fonctionnent sur la base de l'effet électro-absorption. La modulation de ce mode de plasmon unique sous l'effet des propriétés électro-optiques limités du Si conduisent à un dispositif à faible profondeur de modulation.

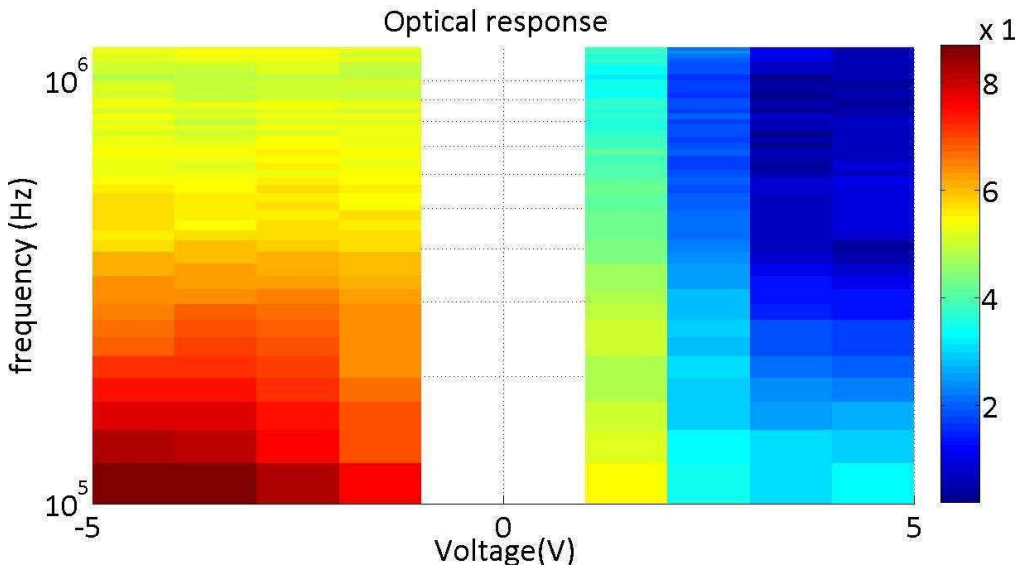

FIGURE 9.15 – *Réponse optique de petites signaux en fonction de la tension appliquée et de la fréquence*

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