Caractérisation et modélisation des fluctuations aléatoires des paramètres électriques des dispositifs en technologies CMOS avancées

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To my parents,

A mes parents,

A meus pais,

"A mind, once stretched by a new idea, never comes back to its original dimensions."

Oliver Wendell Holmes

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Abstract

This research characterizes and models the mismatch of electrical parameters in advanced MOS transistors. All characterizations are made through a test structure, which is experimentally validated using a structure based on Kelvin method. A model, valid in the linear region, is proposed. It is used for modeling the threshold voltage fluctuations of the transistors with pocket-implants, for any transistor length and gate voltage. It gives a deep understanding of the mismatch, especially for devices with non-uniform channel. Another study analyzes the mismatch of the drain current by characterizing and modeling in terms of the drain voltage. A second model is then proposed for transistors without pocket-implants. In order to apply this model, the correlation of threshold voltage fluctuations and mobility fluctuations must be considered. Characterizations are also performed on transistors with pocket-implants, showing a new drain current mismatch behavior for long transistors. Finally, characterizations are made to analyze the impact of gate roughness fluctuations on mismatch.

Key-words: matching, mismatch, fluctuations, variability, MOS transistor, pocket, halos.

Résumé

Ce travail porte sur la caractérisation et la modélisation des fluctuations aléatoires des paramètres électriques des transistors MOS avancées. La structure de test utilisée est validée expérimentalement au moyen de la méthode de mesure de Kelvin. Pour comprendre le comportement des fluctuations, un modèle est dŠabord proposé pour le régime linéaire. Il permet de modéliser les fluctuations de la tension de seuil des transistors avec implants de poche pour toutes les longueurs de transistor et aussi pour toute la gamme de tension de grille. Ensuite, l'appariement du courant de drain est caractérisé et modélisé en fonction de la tension de drain. Pour modéliser les caractéristiques réelles de transistors sans implants de poche, il est nécessaire de considérer la corrélation des fluctuations de la tension de seuil et celles de la mobilité. De plus, des caractérisations sur des transistors avec implants de poche montrent un nouveau comportement de l'appariement du courant de drain. Des caractérisations ont aussi été menés pour analyser l'impact des fluctuations de la rugosité de grille.

Mots-clés : appariement, désappariement, fluctuations, variabilité, transistor MOS, poches, halos.

Resumo

Este trabalho consiste na caracterização e na modelagem do descasamento dos parâmetros elétricos em transistores do tipo MOS avançado. Uma estrutura de teste é necessária para a caracterização, a qual foi validada experimentalmente usando uma estrutura de teste baseada no método de Kelvin. Um primeiro modelo foi proposto válido no regime linear. Este é usado para modelar as flutuações da tensão de limiar nos transistores com os implantes de bolso para todos os comprimentos de transistores e também para toda a gama de tensão da porta. Outro estudo analisa o descasamento da corrente de dreno, caracterizando-o em função da tensão de dreno. Um segundo modelo foi então proposto para transistores sem implantes de bolso. Para aplicar esse modelo, foi necessário considerar a correlação das flutuações de tensão de limiar e das flutuações da mobilidade. Caracterizações do descasamento da corrente de dreno também foram feitas em transistores com implantes de bolso, as quais permitiram identificar um novo comportamento do casamento da corrente de dreno. Finalmente, caracterizações também foram realizadas para analisar o impacto das flutuações da rugosidade da porta.

Palavras-chave: casamento, descasamento, flutuações, variabilidade, transistor MOS, pocket, halos.

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List of acronyms

ADC	Analog-to-digital converters
DAC	Digital-to-analog converters
DIBL	Drain Induced Barrier Lowering
DUT	Device Under Test
GAA	Gate-All-Around
L	Transistor Length
LER	Line Edge Roughness
LWR	Line Width Roughness
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NBTI	Negative-Bias Temperature Instability
PSG	Poly Silicon Granularity
RDD	Random Discrete Dopant
SCE	Short Channel Effect
SCZ	Space Charge Zone
SEM	Scanning Electron Microscopy
SMU	System/Monitor Unit
SNM	Static Noise Margin
SON	Silicon-On-Nothing
STI	Shallow Trend Isolation
FD-SOI	Fully depleted Silicon On Insulator
SRAM	Static Random Access Memory
TCAD	Technology Computer Aided Design
Vt	Threshold voltage
W	Transistor width

Chapter I

Introduction

Microelectronics has a central position in the global economy, being vital to many emerging industries in the 21st century. It offers strategic advantages to firms, institutions and nations through its capacity to develop products and services efficiently. Twenty years ago, a cell phone made calls and little else. As a result of microelectronics advancement, today a cell phone has many features: fast internet connection; integrated video camera; calendar; calculator; MP3 player; text messaging; GPS receiver; can be used to diagnose eye conditions such as nearsightedness and farsightedness (with a device called the Near Eye Tool for Refractive Assessment - Netra); and also make calls. The industries in many areas, such as telecommunications, medicine, entertainment or automotive cannot substantially advance without microelectronics technology.

Since the seventies, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. Moore's law describes a long-term trend, where the number of transistors in a chip doubles roughly every twenty-four months. The trend has continued for more than half a century and is expected to go beyond 2015. This improvement trend, called "scaling trend", was enabled by large research and development investments.

One of the major challenges to keep the scaling trend is the local transistor random variability, also called mismatch. The increase of the variability with the miniaturization of the integrated circuits is detrimental for analog as well as digital devices. The stochastic variability, which comes from process variations, makes equally designed transistors displaying different electrical behavior. The variations of the fabrication process are caused by random microscopic device architecture fluctuations, such as statistical variations in the number of dopant atoms, polysilicon granularity, gate-edge roughness, gate-oxide thickness, etc. These are the reasons why variability issues are paramount for nowadays and future metal-oxide semiconductor field-effect transistors (MOSFET) technologies.

For several technology generations, research has been conducted continuously to keep a good knowledge of the sources of fluctuations and to minimize the level of electrical fluctuations.

This research may be performed by simulation, modeling or characterization. Modeling is used to predict the sources and the level of fluctuations while characterization quantifies them. Simulations are useful to accelerate this prediction, such as 3D 'atomistic simulations'.

In this context, the purpose of this thesis is to understand, quantify and reduce the effect of the local fluctuations on the electrical characteristics of the CMOS transistors.

This thesis was made in collaboration with the Electrical Characterization and Reliability

(ECR) team of STMicroelectronics[1] company and with IMEP-LAHC[2] laboratory from Institut National Polytechnique de Grenoble (INPG)[3].

This research, as part of the ECR team, models and characterizes electrical fluctuations using 45nm and 28nm CMOS technology. While previous works identified that pocket-implants have a strong impact on transistor mismatch, especially for long transistors, this work goes further and proposes the modeling and characterization of this and other contributions.

This study focuses on two sources of fluctuations: random dopants and edge roughness, the first being the critical source for this technology node and the second announced as a major challenge for future technologies.

This thesis is divided in four chapters.

The first chapter is dedicated to explain the objective and the importance of the mismatch study. In addition, it presents the technology, the methodology and the tools that are necessary for this thesis. Moreover, a mismatch test structure based on Kelvin method is proposed to verify if the limitations of the basic test structure may induce characterization errors on mismatch.

The second chapter focuses on the influence of random dopants fluctuations in transistor mismatch. Here, only the linear region of operation is considered. It shows that pocket implants have a large influence in the transistor mismatch, especially for long transistors. Experiments to reduce the mismatch using co-implants in pocket regions were performed. In addition, a mismatch model valid from weak to strong inversion region is proposed to qualify and quantify the effects of pocket regions on mismatch.

In the third chapter, drain-current mismatch is analyzed as a function of drain bias conditions for any region of operation. First, transistors without pocket-implants are characterized. A drain-current mismatch model is proposed. With this model, the influence of the threshold voltage fluctuations and also mobility fluctuations on mismatch are analyzed. Finally, mismatch characterizations are performed for transistor with pocket-implants.

The fourth and last chapter is focused on the mismatch limiting factors for future technologies. One of these factors pointed out by the literature is the edge roughness. The edge roughness is then analyzed for the 45nm technology node. The objective is to quantify the line edge roughness impact on mismatch and to predict the maximum roughness that the gate can have to not influence the mismatch. In this chapter, it is also presented the first mismatch results obtained for 28nm technology node. In addition, the trends for the mismatch on future technologies are discussed.

[1]STMicroelectronics at Crolles, France

[2]Institut de Microelectronique Electromagnetisme et Photonique et le LAboratoire d'Hyperfrequences et de Caracterisation at Minatec, Grenoble, France

[3]INPG at Grenoble, France. INPG is now part of Grenoble Universities

Chapter II

Transistor mismatch: theory, modeling and characterization

In this chapter, a brief introduction of the MOS transistor is given for a better familiarization with the principal device analyzed in this thesis. Afterwards, the main concepts of the mismatch are defined, followed by the matching importance and the motivation for this study. The methodology used to model and to characterize the mismatch is then presented. Thus, the statistical treatment, the extraction methods and the measurement system are described, before concluding with the specific matching test structures. These test structures have some limitations. One of the limitations is the presence of parasitic series resistances. To verify if these parasitic resistances may induce erroneous results, a matching test structure based on Kelvin method is used and results are discussed.

II.1 Brief description of MOS transistor

This section gives a brief introduction of the principal device used in this work, the metal-oxide-semiconductor field-effect transistor (MOSFET). Its architecture, regions of operations and effects are presented. For a detailed description of the equations presented in this section, see references [Skotnicki 00] [Skotnicki 03] [Sze 81][Mathieu 04].

II.1.1 MOS transistor architecture

MOSFET are integrated into a silicon (Si) substrate, called also transistor body. This kind of transistor can be considered as a planar capacitor MOS (metal-oxide-semiconductor), with one of the electrodes replaced by a semiconductor (Si substrate). The other electrode is a poly-silicon (polycrystalline silicon) gate. The term "metal" in MOS is still used today although it has been replaced by a poly-silicon since the mid-1970s. For transistors beyond 32nm, current research points out for a return of metal gates. The poly-silicon and the Si substrate electrodes are insulated by a gate dielectric layer (oxide), as represented in figure II.1.

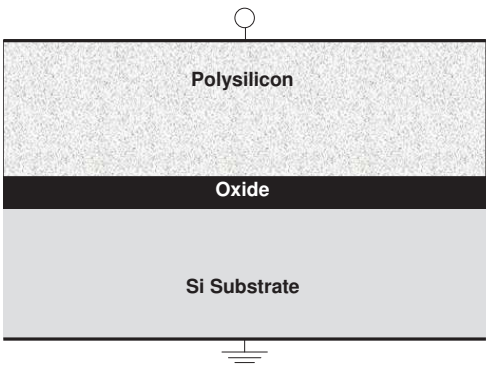
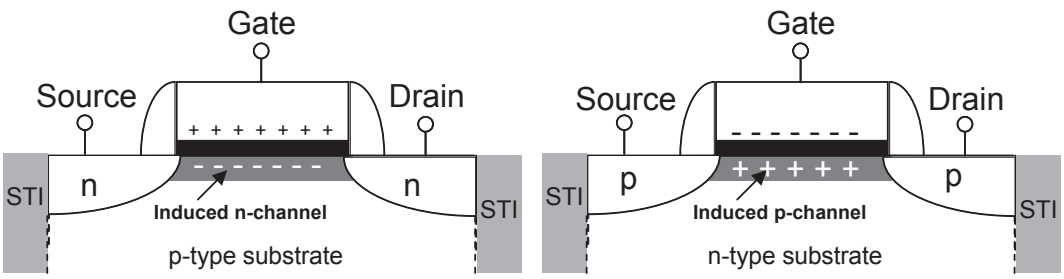


Figure II.1: *Planar capacitor MOS, where poly-silicon and Si substrate are the electrodes and oxide is the dielectric layer.*

Compared to the MOS capacitor, the MOSFET includes two additional terminals implanted in the Si substrate: source and drain. These implanted terminals can be either N-type (excess of electrons) or P-type (lack of electrons or holes). Source and drain implants must both be of the same type, and of opposite type to the body region (figure II.2).



(a) NMOS transistor (b) PMOS transistor

Figure II.2: *Cross section view of bulk MOSFET.*

The gate electrode produces an electric field creating a channel which allows the current to flow between the drain and source for $|V_{DS}|>0$. Thus, the gate creates a conductor channel and enables the current to flow in the channel. Depending on the type of carrier in the channel, the device may be n-channel (NMOS), for electrons, or p-channel (PMOS), for holes.

Previous figure II.2 shows a cross section view of MOS transistors. Both gate side walls are bounded by spacers. The spacers are used to mask high-energy ion-implantation. In the same figure it is represented the Shallow Trench Isolation (STI), which is used to isolate devices from each other. The silicon region where the transistor is manufactured is called active zone. The width (W) and the length (L) of the active zone correspond to the width and the length of the transistor.

II.1.2 Principle of operation

According to the gate voltage applied, three modes of operation are observed: accumulation, depletion and inversion (figure II.3). The voltage separating the accumulation and depletion regime is referred to as the flatband voltage, V_{FB}. The voltage separating depletion and inversion regimes is the threshold voltage Vt. Following, results are shown only for NMOS devices, as NMOS and PMOS have complementary characteristics.

- *Accumulation ($V_{GS} < V_{FB}$):*

  Under negative gate bias, the gate attracts holes from the substrate to the surface, yielding accumulation.

- *Depletion - weak inversion ($Vt > V_{GS} > V_{FB}$):*

  Surface depletion occurs when the holes in the substrate are pushed away by a positive gate voltage.

- *Strong inversion($V_{GS} > Vt$):*

  A more positive voltage attracts electrons (the minority carriers) to the surface, which form the so-called inversion layer or inversion channel.

The transition between the weak and the strong inversion does not happen abruptly. Thus, an inversion level is defined as the threshold between weak and strong inversion regimes. The threshold is defined when the surface potential is twice the Fermi potential $\phi_S = 2\phi_F$, as represented in figure II.4. This is the physical definition of threshold voltage Vt.

Fermi potential is expressed as (equation (II.1)),

$$\phi_F = \frac{kT}{q} ln\left(\frac{N_B}{n_i}\right) \tag{II.1}$$

where $\frac{kT}{q}$ is the thermal voltage, N_B is the channel doping concentration and n_i is the intrinsic concentration.

Therefore, the threshold voltage, which is the voltage applied to pass from weak to strong inversion regime, can be expressed as (equation (II.2)),

$$Vt = V_{FB} + 2\phi_F + \frac{Q_{dep}}{C_{ox}} \tag{II.2}$$

with

$$Q_{dep} = \sqrt{2q\varepsilon_{Si}N_B(\phi_S - V_{BS})} \tag{II.3}$$

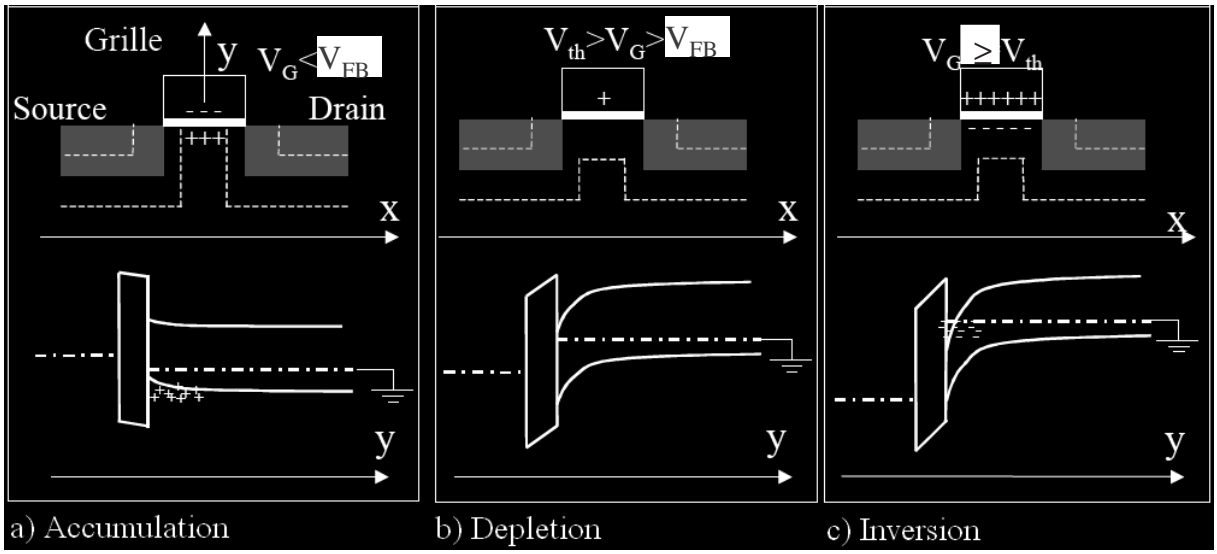


Figure II.3: *Different regimes in NMOS transistor. The first line represents a cross view of the transistor. The second line represents the energy levels belong a transversal section of the channel in the metal, oxide and semi-conducteur regions [Sze 81].*

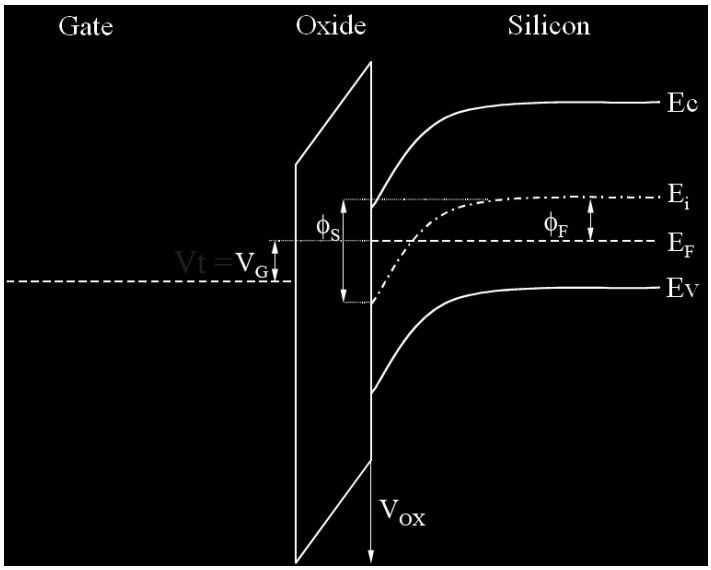


Figure II.4: *Energy band when* $\phi_S = 2\phi_F$.

where Q_{dep} is the depletion charge, q is the elementary electrical charge, ε_{Si} is the silicium permitivity and N_B is the substrate dopants.

Considering the influence of substrate biasing in the inversion layer and, consequently, in the threshold voltage, the Vt can be expressed as (equation (II.4)),

$$Vt = Vt_0 + \gamma\left(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F}\right) \tag{II.4}$$

with

$$\gamma = \frac{\sqrt{2q\varepsilon_{Si}N_B}}{C_{ox}} \tag{II.5}$$

where Vt_0 is the Vt defined in equation (II.2) for $V_{BS} = 0$. γ represents the substrate coefficient.

Once the transistor is in the strong inversion regime, a current flows between source and drain regions, for $V_{DS} > 0$. The drain region induces an additional electrical field, which plays an important role in transistor operation, where three different zones are then observed: linear, non-linear and saturation. These zones are represented in the $I_D - V_{DS}$ characteristics (figure II.5).

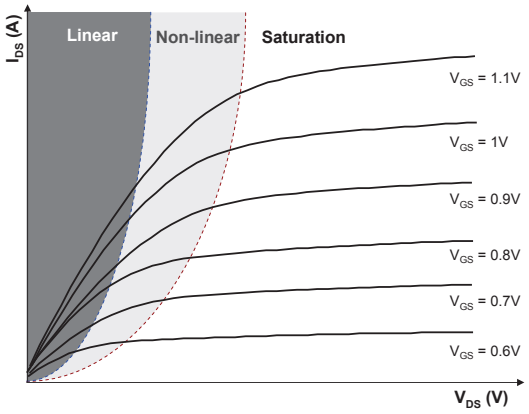


Figure II.5: *Experimental $I_D - V_{DS}$ characteristic for nMOS transistors.*

Linear regime: $V_{DS} < (V_{GS} - Vt)$. The MOS transistor operates like a resistor controlled by the gate bias relative to both drain and source voltages. In this case, the drain current increases linearly with drain voltage. The drain current is given by equation (II.6), where β is the gain factor.

$$I_D = \beta \left(V_{GS} - Vt - \frac{V_{DS}}{2} \right) V_{DS} \tag{II.6}$$

The transistor channel in linear regime is represented in figure II.6.

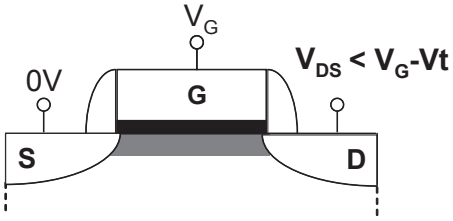


Figure II.6: *MOS transistor in linear regime.*

Non-linear regime: $V_{DS} = (V_{GS} - Vt)$. When the drain voltage is equal to $(V_{GS} - Vt)$, the inversion charge is not constant along the channel length. This regime is also called pinch-off (figure II.7).

Saturation regime: $V_{DS} \geq (V_{GS} - Vt)$. When $V_{DS} > (V_{GS} - Vt)$, electrons spread out and part of the channel is disconnected. There is no more strong inversion charge between the pinch-off point and the drain. The drain current is now quasi-independent of V_{DS} and is controlled by the gate-source voltage (figure II.8).

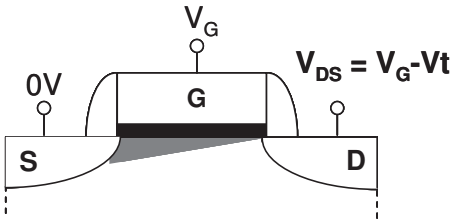


Figure II.7: *MOS transistor pinch-off.*

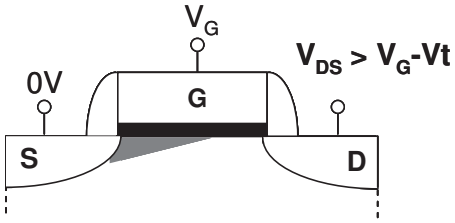


Figure II.8: *MOS transistor in saturation regime.*

To model the drain current for larger drain bias, the V_{DS} has to be replaced by the saturation voltage, which is given by equation (II.7).

$$V_{DS,sat} = V_{GS} - Vt \tag{II.7}$$

Applying equation (II.7) to equation (II.6), the drain current yields (II.8).

$$I_D = \frac{\beta}{2}\left(V_{GS} - Vt\right)^2 \tag{II.8}$$

II.1.3 Short Channel Effect

In this part, the effects caused by shrinking transistor dimensions are presented.

For long transistors, the surface potential along the channel is constant, except near the drain and source junctions. The expansion of the space charge zones (SCZ) are independent of the channel length. By decreasing the length of the transistors, as in figure II.9, the source-channel and channel-drain depletion zones get closer. Then, for short transistors, these zones (SCZ) can overcap.

When the source/drain depletion zones are overcapped, the potential barrier formed by the channel of the transistor decreases. Then, the flat behavior of the surface potential noticed for long transistors is no more observed. Consequently, the threshold voltage gets smaller. This effect is called Short Channel Effect (SCE), and can be seen in figure II.9.

In addition to SCE, the V_{DS} biasing has an effect on the potential barrier as the extension of the depletion zones depends on V_{DS}. If the drain biasing increases, the extension of drain depletion is also increased. As a consequence, the V_{DS} induces a supplementary decrease of the pontential barrier, and then, of the threshold voltage for short devices. This effect is called Drain Induced Barrier Lowering (DIBL). As a result, uncontrolled lowering of the potential barrier causes a drop in the threshold voltage and increases the leakage current, as can be seen in figure II.10.

The decreasing of the Vt for short lengths, as showed in figure II.10(a), is know as the Vt roll-off.

The depletion zones extend mainly within the channel, because of its low doping in comparison to the source and drain. Then, to eliminate the SCE, two regions, called pocket or halo, are

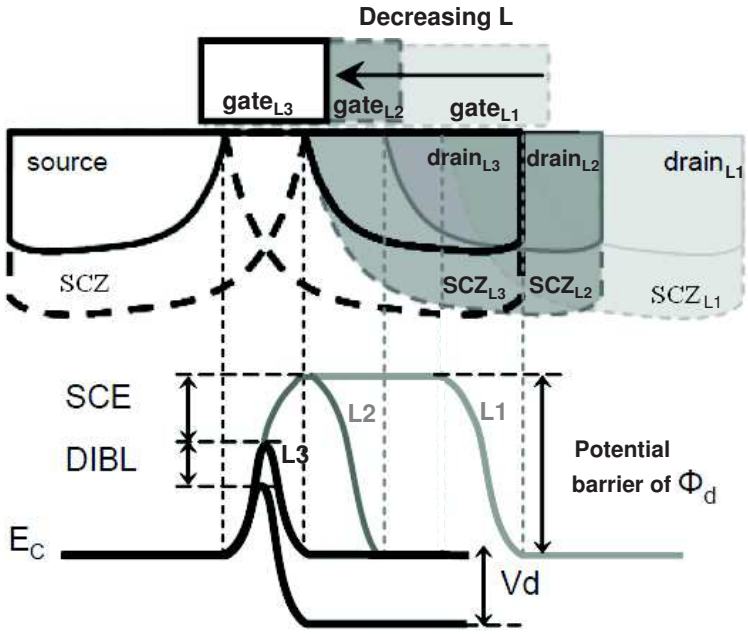
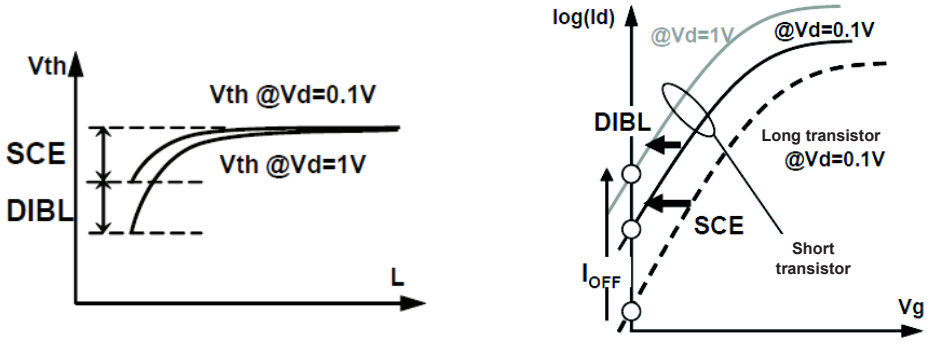


Figure II.9: *Illustration of length decreasing effect on the potential barrier [Chanemougame 05]. The space charge zones (SCZ) get overcapped for the shortest length. The corresponding energie (Ec) is shown, where Short Channel (SCE) and Drain Induced Barrier Lowering (DIBL) effects are represented.*



(a) (b)

Figure II.10: *Short Channel Effect and Drain Induced Barrier Lowering impact on the (a) threshold voltage and (b) leakage currents [Skotnicki 03].*

implanted, by an angle θ, near the drain and source, as seen in figure II.11. These implantations are of the same type of the transistor body, but with a higher dopping concentration, limiting the extension of the depletion regions.

Moreover, for small length, pocket regions are close to each other. As pocket regions are heavily-doped, the channel dopping is increased. Consequently, the Vt increases, eliminating Vt roll-off.

On the other hand, for relatively long devices, pocket regions become separated, creating a non-homogeneous channel. The presence of high-doped and weakly doped regions in the

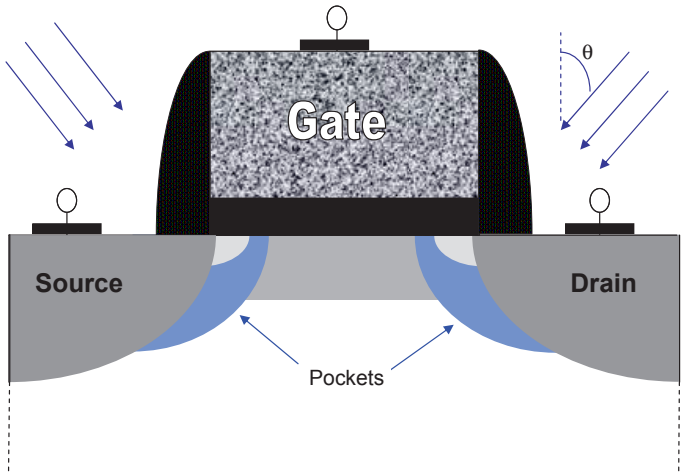


Figure II.11: *Transistor with pocket implants. θ is the angle used to make the implants, to better introduce the dopants under the gate.*

channel implies non-uniform surface potential. This non-uniformity may considerably increases transistor variability [Cathignol 08c] [Johnson 08] [Cathignol 09].

The effects of the pockets on transistor variability will be described with details in following chapters.

II.2 Theory of mismatch

The purpose of this thesis is to model and characterize the differences between two identical designed MOSFET, placed in the same environment, at a (quasi) minimal distance. This section is dedicated to the main concepts of mismatch and the motivation for this study.

II.2.1 Mismatch definition

To introduce the mismatch concept and to understand in which scale it is inserted, the figure II.12 illustrates the different scale of variations between two devices presented in the integrated circuit flow. The amplitude of the variations depends on the distance between these two devices.

When two products are manufactured in different factories, they are produced by different equipments. This results in slightly different circuits. This is also observed among wafers. In this case, the wafers are not at the same position in the equipments, resulting for example in a slight difference in temperature among wafers. This is enough to result in a slight difference between the devices.

At the bottom of the pyramid in figure II.12 are the inter-devices fluctuations. These fluctuations are the differences between two supposedly identical devices separated by a minimum (or quasi-minimum) design rule in an identical environment. They are produced at the same factory, in the same lot, on the same wafer and they are placed in the same die, close to each other. This local variation is commonly known under the terms of [Lakshmikumar 86]:

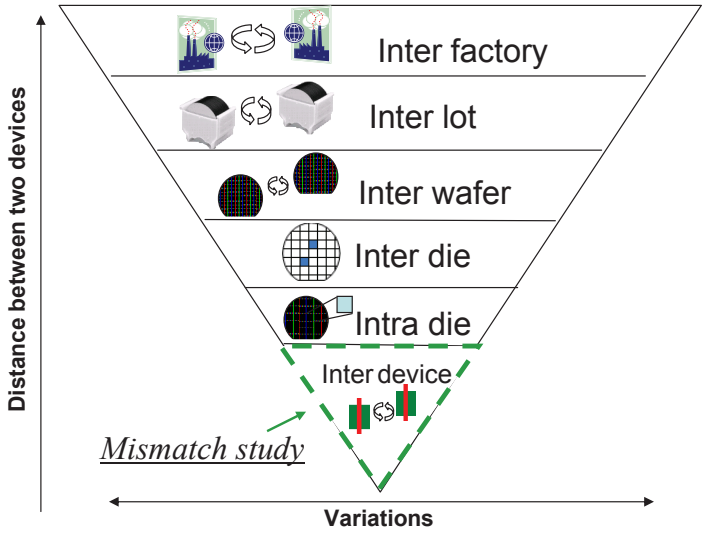


Figure II.12: *Variations at several levels of the fabrication process.*

- *mismatch*: represents the electrical differences between two paired transistors.
- *matching*: it is the opposite of mismatch, showing how alike the paired transistors are.
- *local variability or local fluctuations*: variability or fluctuations are generic terms, which may represent any variation (inter-die, inter-lot, etc). The term *local* is then used to indicate that the external conditions are the same and the variations come from the devices.

It is important to take in mind that variability and local variability are different. For example, if a physical parameter presents inter-die variability, it does not imply in local variability.

II.2.2 Importance and motivation

With the development of the technology and the scaling down of the transistors to deep-submicrometer feature size, the circuit can be composed by millions of transistors in the same die. By scaling down, the variability between two supposed identical transistors increases considerably and becomes a major difficulty for process development.

Since many blocks are based on the availability of two or more electrically identical devices, the quantification of fluctuations is important for both analog and digital circuits.

The impact of the transistor mismatch is more important in the case of analog circuits [Shyu 84], [Kinget 96], [Pelgrom 98], [Lakshmikumar 86]. In analog circuits block, small differences in electrical parameters can determine the performance and/or yield of a product. To illustrate the impact of fluctuations in MOS transistor applications, the current mirror is taken as an example (figure II.13). Its structure consists in two symmetrical transistors, with common-gate and common-source connections. Current mirrors are used to provide bias currents and active loads for a circuit. The function of a current mirror consists in providing an output current I_{out} identical to the input current I_{in}. As drain current depends of the threshold voltage and/or gain factor of the transistor, then, fluctuations in these parameters may implies errors in the reference current source.

As other examples, fluctuations reduce the accuracy of analog-to-digital converters (ADC - as illustrated in figure II.14) and digital-to-analog converters (DAC), degrading the stability of

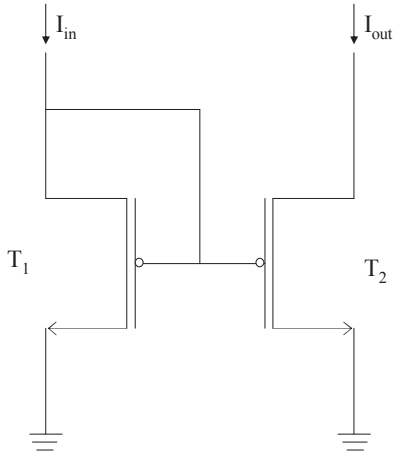


Figure II.13: *Schematic of a current mirror*

reference sources and increasing the off-set voltage of operational amplifiers. There is also the impact of the matching performance on the speed-accuracy power trade-off. For example, in a DAC, the output in the analog circuit is provided by currents, using current mirror circuits. If there is a digital signal of 8 bits, the analog circuit will need 256 current mirrors to make the conversion. Hence, the reproducibility of the current mismatch parameter is very important.

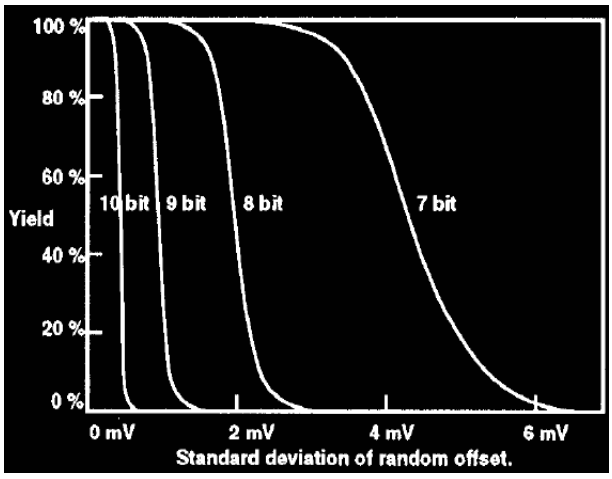
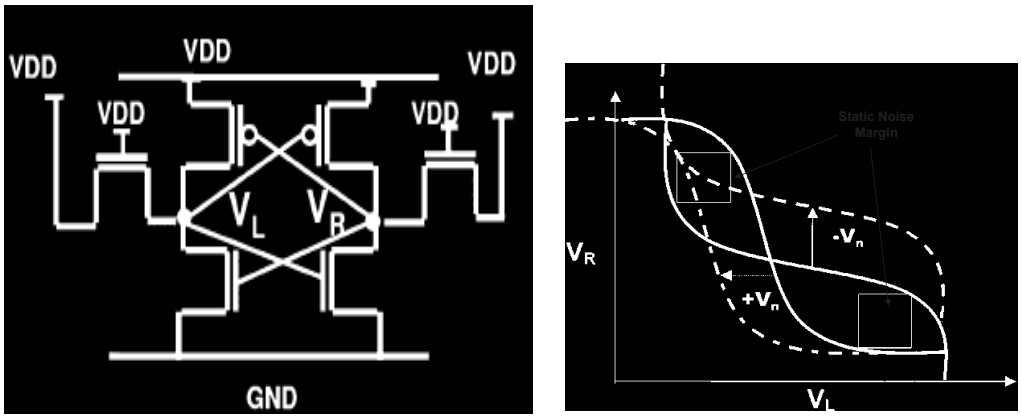


Figure II.14: *Yield of analog-to-digital converters as a function of the standard deviation of the input transistor pair mismatch [Pelgrom 98].*

In digital circuits, the transistor mismatch leads to fluctuations in the time delay between logic circuits, an increase of leakage currents and an increase in the number of errors in the processes of writing and reading memories, [Pineda de Gyvez 04], [Burnett 94], [Burnett 02], [Stolk 01]. Bhavnagarwala et al. [Bhavnagarwala 01] studied the effect of the fluctuations on a 6T-SRAM. The SRAM cell operates as a bistable circuit with two distinct stable states during Read and Retention periods. Figure II.15(a) shows a schematic of a 6T-SRAM and its static voltage characteristic during a Read operation. Fluctuations in the threshold voltage translates into a variation on the static noise margin (SNM). The SNM of some cells may be annulated if variations are too large, as observed in the dashed line in figure II.15(b), which implies in a fail as it is not possible to change the state of the cell.

With the miniaturization of the transistors, the fluctuations are becoming more important.



(a) (b)

Figure II.15: *(a) Schematic of a conventional 6T-SRAM cell during a Read operation. (b) Static voltage characteristics of a conventional cell during a Read operation [Bhavnagarwala 01].*

This fact can also be noticed by the increasing number of publications in the last few years, looking at the references of this thesis. The variations in the MOSFET performance are a major challenge for future process generations [Pitcher 10]. Thus, it is becoming important to understand, quantify and reduce the effect of these fluctuations on the electrical characteristics of the transistors.

II.2.3 State of the art

The mismatch in MOS transistors has been studied for more than three decades. One of the first investigation of the fluctuations effects was made in 1972 by Hoeneisen and Mead [Hoeneisen 72]. They noticed that a possible limitation for MOSFET technology are due the unpredictability in the threshold voltage because of substrate doping fluctuations. This problem is discussed in 1975 by Keyes [Keyes 75]. Using a discretization of the chanenl region, Keys formalized a model to predict the amplitude of Vt variations, but without considering the operation of the transistor.

McCreary showed the dimensional dependency of MOS capacitance, which was explained by Shyu et al. [Shyu 82]. At this point, the mismatch factors are already grouped as stochastic and systematic. The stochastic mismatch is given by the standard deviation of a population distribution while systematic mismatch is given by the mean. Stochastic and systematic concepts will be explained in following sections.

In a new work, Shyu et al. [Shyu 84] presented a more complete mismatch model for MOS capacitors and MOS transistors. It gives the dependence of each error source on the physical dimensions, the standard deviations of the fabrication parameters and the bias conditions. The dimensional dependency equations presented then, were consecrated afterwards. It is in 1986 that Lakshmikumar et al. [Lakshmikumar 86] presented a paper exclusively about mismatch on MOS transistors. They experimentally observed the dimensional dependence for the mismatch in MOS transistors.

In 1989, one of the most cited papers on the field was published by Pelgrom et al. [Pelgrom 89]. Differently of the previous works, which start the analysis from the causes of mismatch, this one

makes a generically mathematical treatment of the mismatch between two transistors, where a parameter P varies spatially. This paper explicitly demonstrates the dimensional dependence of electrical parameter fluctutaions in MOS transistors. It points out that the standard deviation of the δP is inversely proportional to the square root of the transistor area, as show in equation (II.9).

$$\sigma_{\delta P} = \frac{A_{\delta P}}{\sqrt{WL}} \tag{II.9}$$

From Pelgrom's law, many contributions have been made. The discrete model formalized by Keyes is rediscussed by Mizuno et al. [Mizuno 93] [Mizuno 94] [Mizuno 96], where they experimentally verified that the Vt mismatch is given by a Gaussian function and this distribution results from fluctuations of the number of discret dopants in the depletion region. The doping fluctuations became then very significant for the mismatch studies, especially due the decreasing feature sizes [Steyaert 94] [Elzinga 96] [Stolk 96] [Wong 97] [Bastos 97] [Tanaka 00b]. Other important contributions to from the mismatch 'atomistic' simulations, performed by A. Asenov and the Device Modelling Group at Glasgow University at the end of nineties. Some of their works are listed here, but are not exhaustive: [Asenov 98a] [Asenov 98b] [Asenov 00a] [Brown 02] [Roy 05] [Cheng 06].

Other effects related to doping are studied, as the halo implantation [Tanaka 00a], [Rios 02], [Mc Ginley 04], [Difrenza 00].

Another source of intrinsic parameter fluctuations is the line edge roughness (LER). Since 2000, the line and width gate roughness (LER and LWR) became a critical factor for the mismatch study [Oldiges 00], [Asenov 03], [Xiong 04], [Gunther 05], [Fukutome 06]. LER has caused little worry in the past since the critical dimensions of MOSFETs were orders of magnitude larger than the roughness. However, with the shrinking of transistors, LER does not scale accordingly, becoming a larger fraction of the gate [Asenov 03].

The impact of gate material has also been studied, especially the effect of polysilicon granularity fluctuations, [Difrenza 03b], [Cathignol 06b], [Brown 06].

Among this important list of fluctuations sources, Cathignol et al. [Cathignol 08b] identified the percentage of each contribution for 45nm technology. Cathignol et al. showed that the major physical sources of fluctuations are the random discrete dopants (RDD), the poly silicon grain (PSG) and the line edge roughness (LER), where more than 60% of the mismatch is due the RDD.

While some researchers focused on the identification of the fluctuctuations sources, some were interested in the fluctuation level of electrical parameters that are useful for design and modeling. The mismatch in drain current parameter was extensively studied. It can be represented by a study of the mismatch in threshold voltage and in gain factor. Bastos and Drennan [Bastos 98], [Drennan 99], [Drennan 03] focused on the modeling of the drain current. Croon [Croon 04] also gave his contribution to its model.

The measurement methodology, test structure and layout issues on mismatch have been extensively studied by Tuinhout since 1994 [Tuinhout 94] [Tuinhout 10].

In this thesis, the mismatch in 45nm technology node is analyzed. This study focous on RDD and LER sources of fluctuations, as RDD is the critical source for this technology node and LER is indicated to be a major challenge for future technologies.

II.3 Mismatch study

The general methodology flow of the mismatch study applied during this thesis is represented in diagram of figure II.16.

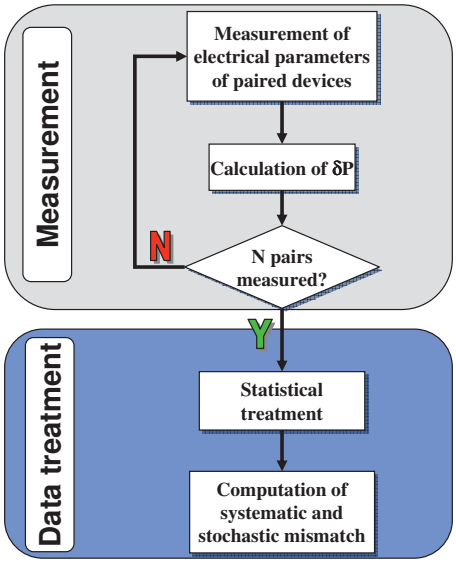


Figure II.16: *Methodology flow of the mismatch study.*

The methodology consists in measuring a pair of identically designed devices, separated by the minimum (or quasi-minimum) design rule spacing, placed in the same environment. For each device, an electrical parameter (P) is measured. Then, the absolute variation ΔP (equation (II.10)) or the relative variation $\Delta P/\bar{P}$ (equation (II.11)) of the electrical parameter of the pair is calculated. This procedure is performed for a large number of pairs of transistors to assure a significant statistical population (for a confidence level of 99 %).

$$\Delta P = P_2 - P_1 \tag{II.10}$$

$$\frac{\Delta P}{\bar{P}} = \frac{2(P_2 - P_1)}{P_2 + P_1} \tag{II.11}$$

The statistical distribution of these electrical differences represents the variations of the parameter in question. This distribution can be modeled by a Gaussian law, defined by its mean and standard deviation. This distribution is filtered by a $\pm 3\sigma$ filter to eliminate the erroneous values. Then, the mean and the standard deviation are calculated.

Following figure II.17 represents the requirements to perform the methodology flow.

To compute the mismatch parameter $A_{\delta P}$, there are basically two steps: measurement and data treatment. For the measurement of electrical parameters, a test structure, a measurement setup, a measurement system and a parameter extraction method are required. In the data treatment step, once the parameters P of interest is extracted from the measurements results for N pairs, the statistical treatment is performed. Finally, the stochastic and the systematic mismatch are characterized and the mismatch parameter is obtained. These required steps are detailed in following sections.

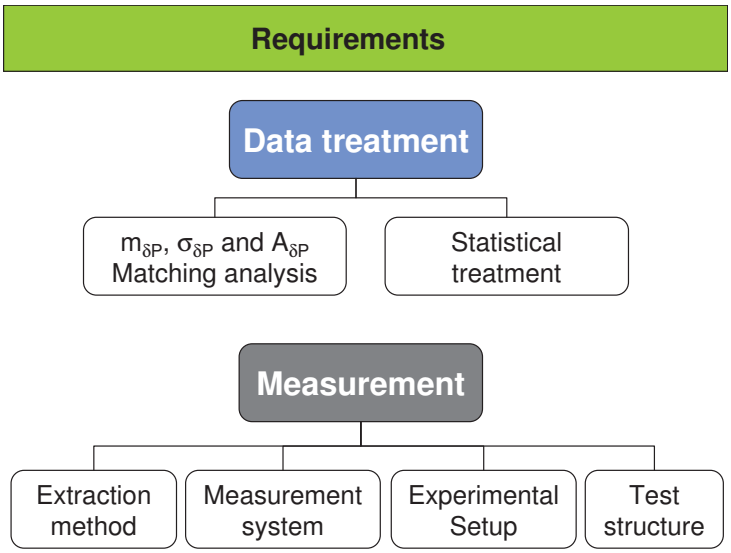


Figure II.17: *Schematic of the requirements for the mismatch study.*

II.4 Computation of systematic and stochastic mismatch

This section presents how systematic and stochastic mismatch are computed, explaining their concepts (figure II.19).

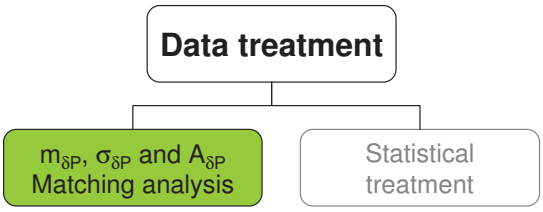


Figure II.18: *Schematic of the requirements for the mismatch study.*

Considering δP (equation (II.12)) the difference of parameter P measured between the two paired devices, matching characterization results in evaluating both the mean $<\delta P>$(II.13) and the standard deviation $\sigma(\delta P)$ (II.14) from Gaussian distribution δP.

$$\delta P = \Delta P \; or \; \Delta P/\bar{P} \tag{II.12}$$

$$m_\delta = \frac{1}{N}\sum_{i=1}^{N}\delta_i \tag{II.13}$$

$$\sigma_\delta = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(\delta_i - m_\delta)^2} \tag{II.14}$$

The mean is called the systematic mismatch and can be supressed by the design. The standard deviation represents the stochastic fluctuations, or the local process fluctuations. Finally, investigations result in the extraction of a mismatching parameter $A_{\delta P}$ (II.15), which is the

proportionality coefficient between standard deviation of δP and reverse square root of drawn gate area [Pelgrom 89].

$$\sigma_{\delta \mathbf{P}} = \frac{\mathbf{A}_{\delta \mathbf{P}}}{\sqrt{\mathbf{WL}}} \tag{II.15}$$

Systematic mismatch The distribution δP is usually centered in zero. There is a systematic mismatch if the average of the distribution is not zero. It is caused mainly by the differences in the environment where the devices are inserted. It can be, for example, different metallic covers between the pair device [Tuinhout 96] [Tuinhout 97] which induce local differences in terms of mechanical constraints, or another asymmetry in the conception of the mask used for manufacturing [Tuinhout 94]. Tuinhout et al. [Tuinhout 03] states that all phenomenon which can provoke a difference in the measurement conditions between the pair of devices induces a systematic mismatch.

In most cases, the systematic mismatch can be avoided during the design of the devices. One of the techniques is the use of dummies, devices which are not connected to the pair. In the case of transistors, the dummies are placed in both sides of the gate, assuring the same environment for both devices of the pair.

Stochastic mismatch The stochastic mismatch is given by the standard deviation of the distribution $\sigma_{\delta P}$. It is generally attributed to random variations in physical characteristics of the devices. This happens because the manufacturing process of the integrated circuits cannot be precisely controlled. Then, some physical parameters may randomly vary from one device to another. For example, it is not possible to control the number of dopants implanted in the device.

II.5 Statistical treatment

The mismatch is studied through the use of statistical tools. In order to understand such tools, some basic statistical concepts are presented [Soong 04].

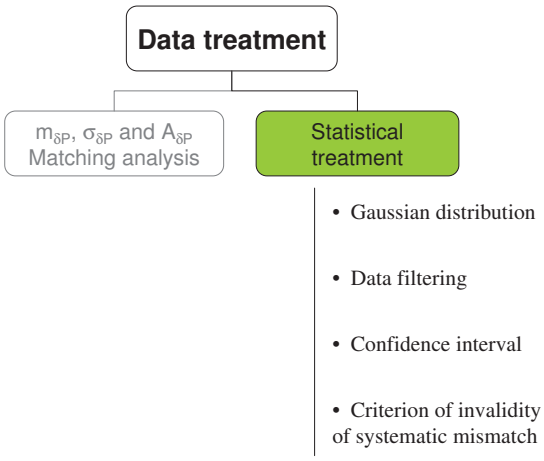


Figure II.19: *Schematic of the requirements for the mismatch study.*

II.5.1 Normal or Gaussian distribution

A random variable X is Gaussian or normal if its probability density function is of the form:

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} exp\left(-\frac{(x-m)^2}{2\sigma^2}\right), -\infty < x < \infty \tag{II.16}$$

where m is its mean and σ is its standard deviation.

If the experimental distribution of the local electrical variations (ΔP *or* $\Delta P/P$) follows a Gaussian law, then

$$\delta P(x) = \frac{1}{\sigma_{\delta P}\sqrt{2\pi}} exp\left(-\left(\frac{x-m_{\delta P}}{2\sigma_{\delta P}}\right)^2\right) \tag{II.17}$$

where $m_{\delta P}$ is the mean of the δP distribution and $\sigma_{\delta P}$ is its associated standard deviation.

Both parameters are extracted from experimental measures from N pairs devices. Then, it is important to verify if the population in question follows the normal distribution.

There are different statistical tests to verify if the distribution is Gaussian. Chi-square is a statistical test commonly used to compare the observed data with the data expected to be obtained according to a specific hypothesis, normal distribution in the case of matching study. The chi-squared test enables to validate or to reject the Gaussian feature of a distribution. After the verification of the distribution nature using the chi-squared test, the mean and the standard deviation are computed.

II.5.2 Data filtering

During the test, Cathignol et al. [Cathignol 07a] have observed that the resistance of the points used to measure the devices can increase considerably, as shown in figure II.20.

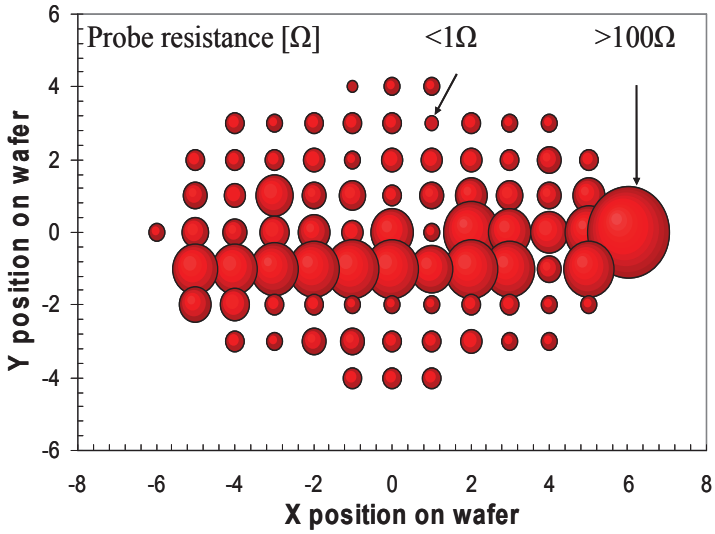


Figure II.20: *Mapping of one of the probe resistance used for a matching test, performed row by row, starting from the top row [Cathignol 07a].*

Cathignol et al. points out that, whatever the method used for extraction, a special care should be taken on probes resistance. If they are not low enough, they can distort mismatch estimation. This means that it is important to monitor the resistances during measurement test.

Afterwards, the experimental data are filtered before being analyzed. This step is very important because if an erroneous data is presented in the distribution, it can strongly impact the population's dispersion.

The filter consists in removing the experimental data which have abnormal fluctuation levels, as represented schematically in Figure II.21.

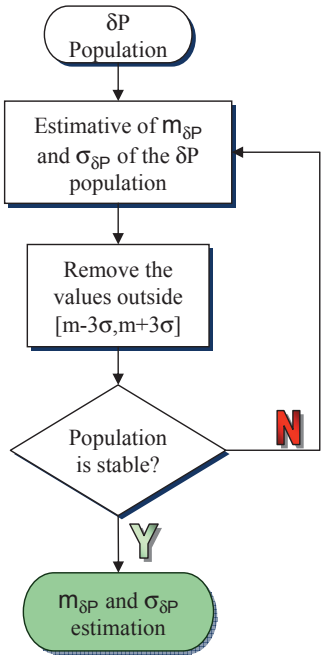


Figure II.21: *Schematic of data filtering.*

The three-sigma method is used to filter the data. This method consists in estimating the standard deviation and the mean of the population. Then, all values outside the interval $[m - 3\sigma, m + 3\sigma]$ are removed, using 99% of confidence level. This step is repeated until there are no more values to be removed, thus making the population stable. Then, the standard deviation and the mean are obtained.

II.5.3 Confidence interval

For each transistor geometry, the standard deviation of δP is estimated from the population by N pairs of transistors (σ_{exp}) and not by the total dice manufactured, where its correspondent standard deviation (σ) is unknown. The confidence interval can be calculated, with a confidence degree of (1-γ)[Pergoot 95].

$$\frac{\sigma_{exp}\sqrt{N-1}}{\chi_{1-\gamma/2}} < \sigma < \frac{\sigma_{exp}\sqrt{N-1}}{\chi_{\gamma/2}} \tag{II.18}$$

Then, the upper and lower relative error of the standard deviations can be obtained:

$$\sigma_{exp}(1-Y) \leq \sigma \leq \sigma_{exp}(1+X) \tag{II.19}$$

Where:

$$X = 1 + \sqrt{\frac{N-1}{\chi^2_{\gamma/2}}} \tag{II.20}$$

$$Y = 1 - \sqrt{\frac{N-1}{\chi^2_{1-\gamma/2}}} \tag{II.21}$$

The table II.1 gives some examples of the error as a function of the chosen sample and confidence interval. The errors are not symmetrical. This dissymmetry is reduced as the sample increases.

Table II.1: *Upper and lower confidence limits for three confidence levels.*

	Upper confidence limit (%) for a confidence level of:			Lower confidence limit (%) for a confidence level of:		
Number of elements	90%	99%	99.9%	90%	99%	99.9%
20	37.0	66.6	96.7	20.6	29.8	35.7
25	31.6	55.8	79.5	18.8	27.4	33.0
30	28.0	48.7	68.4	17.5	25.6	30.9
35	25.3	43.5	60.6	16.4	24.1	29.2
40	23.2	39.7	54.8	15.5	22.8	27.8
45	21.5	36.6	50.3	14.7	21.8	26.5
50	20.2	34.1	46.6	14.1	20.9	25.5
55	19.0	32.0	43.6	13.5	20.1	24.5
60	18.0	30.3	41.1	13.0	19.4	23.7
65	17.2	28.7	38.9	12.5	18.7	23.0
70	16.5	27.4	37.0	12.1	18.2	22.3
75	15.8	26.3	35.4	11.8	17.6	21.7
80	15.2	25.2	33.9	11.4	17.2	21.1
85	14.7	24.3	32.6	11.1	16.7	20.6
90	14.2	23.5	31.4	10.9	16.3	20.1
95	13.8	22.7	30.4	10.6	15.9	19.7
100	13.4	22.0	29.4	10.4	15.6	19.3
150	10.6	17.3	22.9	8.6	13.1	16.2
200	9.0	14.7	19.3	7.6	11.5	14.3

In this work, 99% of confidence level is used.

II.5.4 Criterion of invalidity of systematic mismatch

The systematic mismatch can be considered as null if it is negligible compared to the stochastic mismatch. For that, the mean of the distribution δP has to be equal to zero. To verify if the distribution δP follows a Gaussian one with a zero mean, the normal reduced variable Z is calculated:

$$Z = \frac{<\Delta P>}{\sqrt{\frac{2\sigma^2_{\delta P}}{N}}} \tag{II.22}$$

The systematic mismatch is not negligible with a confidence degree of (1-λ) if Z exceeds the critical value for $\lambda/2$ [Pergoot 95].

II.6 Extraction methods

One of the steps in the mismatch study is to estimate the mean and the standard deviation of δP parameter. This section presents the extracted parameters (P), and the procedure of extraction.

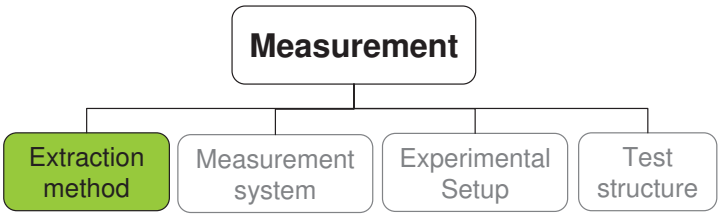


Figure II.22: *Schematic of the requirements for the mismatch study.*

Threshold voltage and gain factor are important parameters of the MOS transistors to be considered during design. Fluctuations in the drain current are also important aspects to be controlled. The mismatch in the drain current is assumed to be a result of a mismatch in threshold voltage (ΔVt) and in the current factor ($\Delta\beta/\beta$) [Pelgrom 98] [Lakshmikumar 86] [Bastos 96] [Serrano-Gotarredona 00] [Croon 04]. Thus, the parameters usually analyzed in the mismatch study are Vt, β and I_D.

The drain current parameter is obtained directly from transistor measurements. For the threshold voltage and the current factor several techniques are presented in the literature [Hamer 86] [Mourrain 00]. The commonly used methods are the maximum slope method, the three points method and the four points method. In addition to those, the constant current method is also used to extract the threshold voltage.

A comparison between the different extraction techniques is made by Croon et al. [Croon 02b]. Between the methods above, the three points method and the four points method show interesting results. These are relatively independent of the transistor geometries and the input parameters, yielding accurate results. However, these methods require long measurement time. The maximum slope method is purely intended for extracting parameters. It does not present a model for the drain current as a function of the bias conditions. Also, it strongly depends on source/drain resistances. Otherwise, this method is physical, the Vt and β parameters can be obtained and it is faster than the three points and the four points method. Other method commonly used is the constant current method. It is simple and fast, but it is not physical and it can be used only to Vt extraction. The major drawback of the constant current method is the arbitrary choice of the drain current, usually scaled by W/L, at which the value of Vt is measured.

In this work, the focus is to analyze electrical parameter differences and not the intrinsic value of the parameter. Moreover, a lot of data is necessary as a statistical study is performed. To this aim, a quick method with good repeatability [1] is required. In addition, comparisons between different processes are performed and the same method is used to avoid introducing a margin of error due to the extraction method. Thus, the maximum slope method is used in most of the studies. For some specific studies, the constant current criterion is used.

Following, the methods used in this work (maximum slope and constant current criterion) are described with details.

[1] A test of repeatability has been performed and is presented in Appendix A

II.6.1 Maximum slope method

Linear region The maximum slope method is illustrated in figure II.23. The drain current is measured as a function of the gate bias in the linear regime. The tangent is taken at the place where the transconductance g_m reaches its maximum value (II.23) [Sedra 07]. The g_m is defined as the partial derivative of the drain current with respect to the gate voltage. The gate bias where the tangent and $I_D = 0V$ intercept is equal to $Vt + V_{DS}/2$. The Vt and the current factor are expressed as equations (II.24) and (II.25) respectively [Skotnicki 00] [Skotnicki 03].

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{II.23}$$

$$Vt = V_{GS} - \frac{V_{DS}}{2} - \frac{I_D}{g_{m,max}} \tag{II.24}$$

$$\beta = \frac{g_{m,max}}{V_{DS}} \tag{II.25}$$

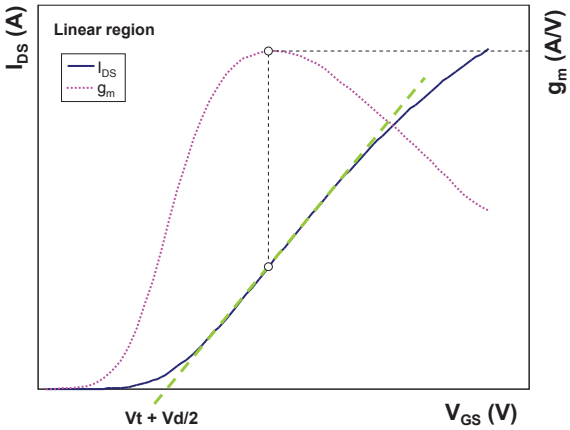


Figure II.23: *Maximum slope method for linear region.*

Saturation region The drain current in saturation region is expressed as equation (II.8). A square root of this expression is given by equation (II.26).

$$\sqrt{I_D} = \sqrt{\frac{\beta}{2}}\,(V_{GS} - Vt) \tag{II.26}$$

The Vt is defined as the intersection of $\sqrt{I_D} = 0$ line and the tangent line of $(V_{GS} - \sqrt{I_D})$ curve at the point where the slope of the $\frac{\delta\sqrt{I_D}}{\delta V_{GS}}$ curve is maximum [Shimizu 02]. It is expressed as equation (II.27) and its extraction is represented in figure II.24. The current factor is given by equation (II.28).

$$Vt = V_{GS} - \sqrt{\frac{2I_D}{\beta}} \tag{II.27}$$

$$\beta = 2\left(\frac{\delta\sqrt{I_D}}{\delta V_{GS}}\right)^2 \tag{II.28}$$

Therefore, using equations (II.26) and (II.28), g_m is given by equation (II.29).

$$g_m = \frac{\delta I_D}{\delta V_{GS}} = \beta\,(V_{GS} - Vt) = 2\sqrt{I_D}\frac{\delta\sqrt{I_D}}{\delta V_{GS}} \tag{II.29}$$

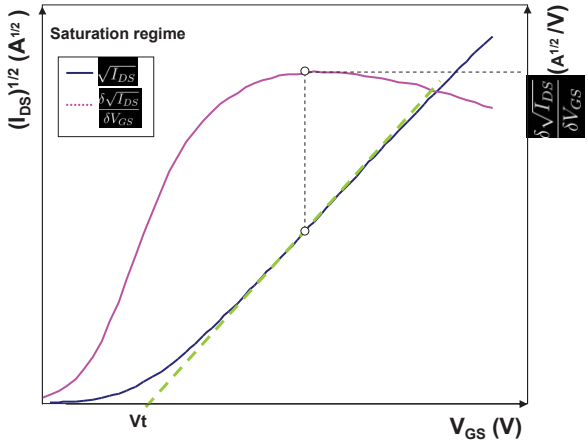


Figure II.24: *Maximum slope method for saturation region.*

II.6.2 Applying a current criterion or constant-current method

In this method, the threshold voltage is defined as the gate bias required to reach a fixed current criterion (figure II.25).

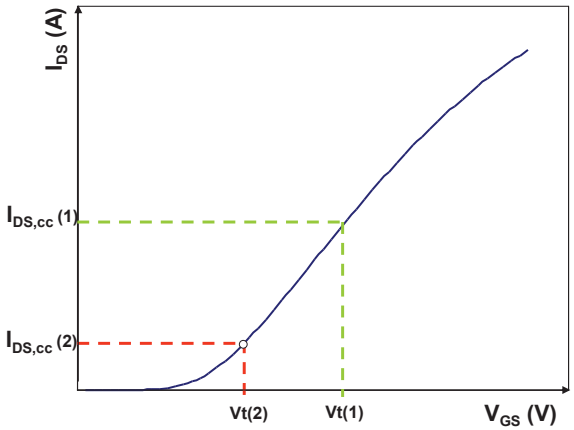
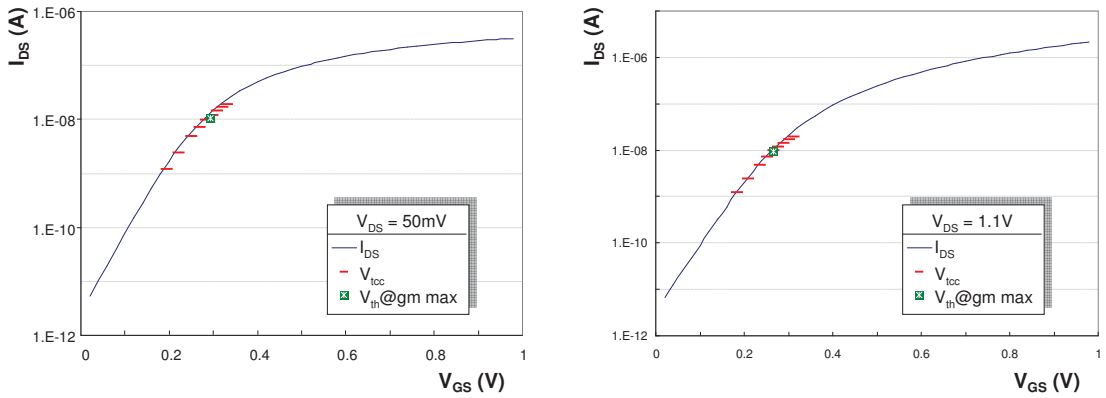


Figure II.25: *Constant current method, where the threshold voltages for two current levels ($I_{DS,cc}$) are represented.*

Although constant-current method is not physical, it is the simplest method to measure Vt. One of the limitations of this method is that no other parameter besides the Vt is obtained. But the major limitation is still the choice of the current level. To analyze the extraction using different current levels, the threshold voltage, called here as V_{tcc}, was extracted from the I_D - V_{GS} curves by current levels in the range [$50nA\frac{W}{L}$, $800nA\frac{W}{L}$]. They are represented in figure II.26, for linear and saturation region.

The V_{tcc} extracted for different current criterions form a cloud of points around the zone where the transistor passes from weak to strong region. The current level corresponding to the threshold voltage extracted by the maximum slope method, called here $Vt@g_{m,max}$ is situated in the V_{tcc} cloud of points. The $Vt@g_{m,max}$ and V_{tcc} values are represented in figure II.27. In this case, the V_{tcc} which corresponds to $Vt@g_{m,max}$ is the one extracted with $500nA\frac{W}{L}$ current level in linear region and $400nA\frac{W}{L}$ in saturation region.



(a) Linear regime (b) Saturation regime

Figure II.26: *Representing $Vt@g_{m,max}$ and V_{tcc} in the I_D - V_{GS} characteristics.*

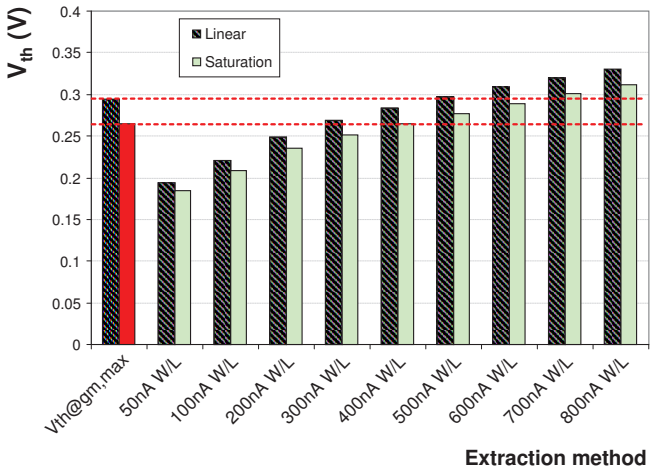


Figure II.27: *$Vt@g_{m,max}$ and V_{tcc} for NMOS transistors.*

For PMOS devices, V_{tcc} is extracted in the range $[50nA\frac{W}{L}, 400nA\frac{W}{L}]$. The $Vt@g_{m,max}$ is the one extracted with $150nA\frac{W}{L}$ current level in linear region and $100nA\frac{W}{L}$ in saturation region, as shown in figure II.28.

For the technology node used in this work, experimental current levels at which the V_{tcc} measured is close to $Vt@g_{m,max}$ correspond to $400\frac{W}{L}nA$ for NMOS and $100\frac{W}{L}nA$ for PMOS devices.

As it will be shown in next chapter, a special method is used to characterize long transistors with pocket implants. This method is then described.

II.6.2.a Gate-bias-dependent threshold voltage extraction method

The gate-bias-dependent threshold voltage extraction method is used to characterize long transistors with pocket implants. These transistors have non-uniform surface potential. To model long transistors, Cathignol [Cathignol 08a] introduced a gate-bias-dependent threshold voltage, Vtcc(V_{GS}). This function allows translating the non-uniform potential profile of long devices

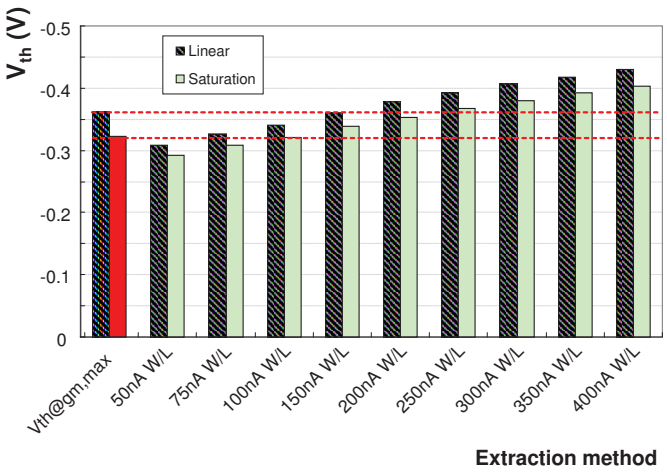


Figure II.28: *$Vt@g_{m,max}$ and V_{tcc} for PMOS transistors.*

with pocket implants.

Gate-bias-dependent threshold voltage method relies on a constant current-like method, as illustrated in figure II.29.

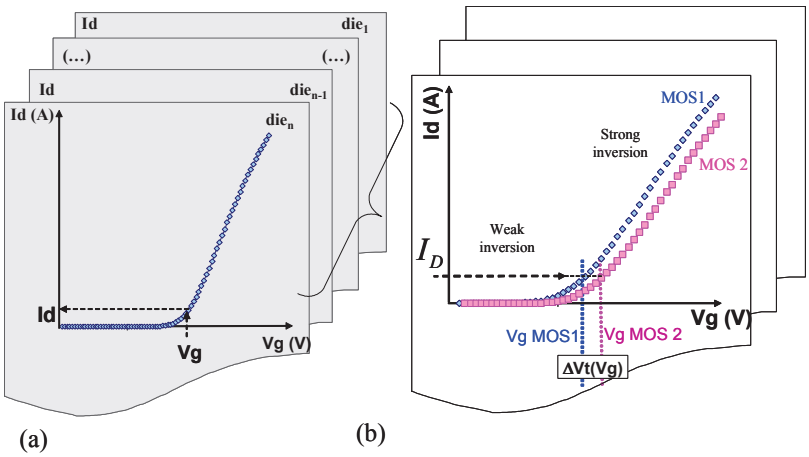


Figure II.29: *Gate-bias-dependent threshold voltage. (a) First step and (b) second step.*

The Vtcc(V_{GS}) is extracted from $I_D(V_{GS})$ curves, by two steps.

The first step consists in defining the constant-current criterion. To define it, the I_D at a given V_{GS} is extracted for n-transistors. The average I_D is then used as the constant-current criterion.

The second step consists in extracting the Vt via a constant-current method. The current criterion used is the average I_D extracted in the first step. For each $I_D(V_{GS})$ curves, the V_{GS} corresponding to the current criterion is obtained, here called Vtcc(V_{GS}).

The ΔVtcc(V_{GS}) is extracted from the Vtcc(V_{GS}) function. For this, the Vtcc(Vg) method is applied for both transistors and the ΔVtcc(V_{GS}) is obtained. Then, the mismatch dispersion $\sigma_{\Delta Vtcc(V_{GS})}$ can be estimated.

II.7 Measurement system

The measurement system is described in this section (figure II.30)

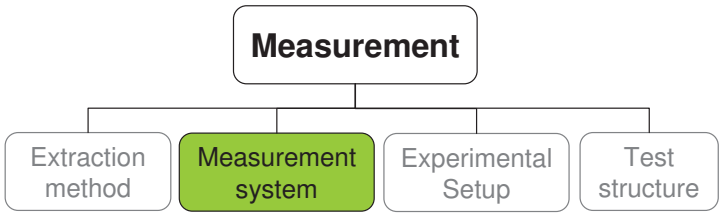


Figure II.30: *Schematic of the requirements for the mismatch study.*

The measurement system used is schematically represented in figure II.31.

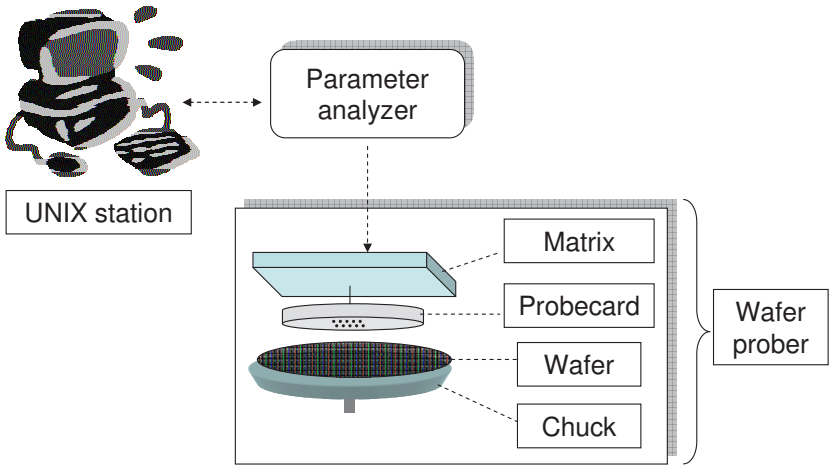
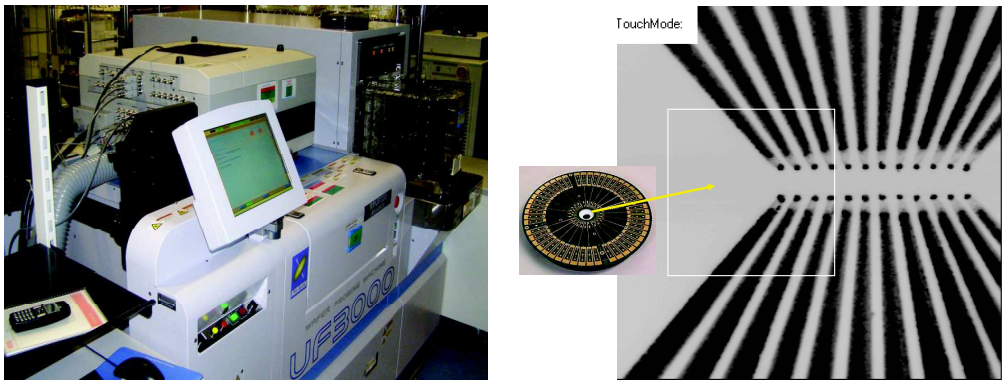


Figure II.31: *Measurement system.*

It consists in a probe station II.32(a), a chuck, a probe card II.32(b), a switching-matrix, a parameter analyzer and a UNIX station. The wafer to be measured is placed on the chuck. The wafer-probe automatically moves the chuck around. This enables the automatic measurement of N dice, which is a requirement for a statistical study. The used probe card consists of two lines with twelve pins each, connected to a switching matrix, which connects the correct pin to the correct SMU (Source/Monitor Unit). Through the SMUs, the parameter analyzer supplies the defined voltages/currents and measures the currents/voltages of the devices under test (DUT). Finally, the UNIX workstation is used to communicate with the measurement equipment and to collect the experimental data.



(a) (b)

Figure II.32: *Photo of a) a wafer prober and b) a probecard*

II.8 Experimental setup used along this work

In this section, the experimental setup used along this work is described (figure II.33).

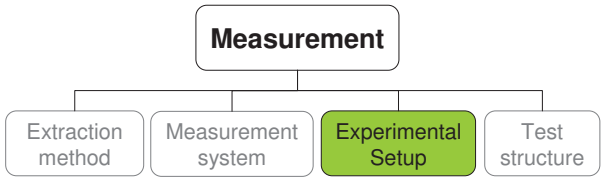


Figure II.33: *Schematic of the requirements for the mismatch study.*

In this work, both NMOS and PMOS devices are analyzed. For each study, around 70 pairs of transistors for each geometry are measured. The electrical parameters analyzed are the threshold voltage, the gain factor and the drain current.

The technology used is the 45nm STMicroelectronics MOSFET, except for the advanced technologies presented in the last chapter. This technology has a supply voltage of 1.1V for devices with oxide thickness equal to 2nm. The geometries for both NMOS and PMOS transistors are presented in table II.2. For other specific studies, the geometries are described in detail for each case, in the respective sections.

Table II.2: *Transistors geometries.*

W (μm)	L (μm)	W (μm)	L (μm)
0.12	0.04	0.12	0.1
0.15	0.04	1	0.1
0.2	0.04	0.12	0.2
0.5	0.04	0.12	0.5
1	0.04	1	0.5
5	0.04	0.12	1
0.12	0.05	0.15	1
1	0.05	0.2	1
0.12	0.06	5	1
0.15	0.06	0.12	5
0.12	0.08	1	5
0.2	0.08	5	5
1	0.08		

II.9 Test structure

The last point to be presented is the test structure used in the measurement (figure II.34).

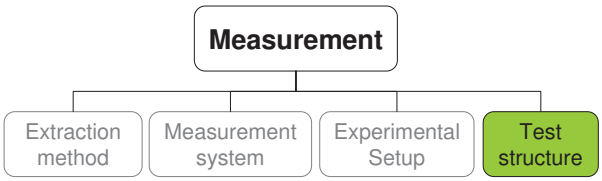


Figure II.34: *Schematic of the requirements for the mismatch study.*

The test structure used is presented in figure II.35.

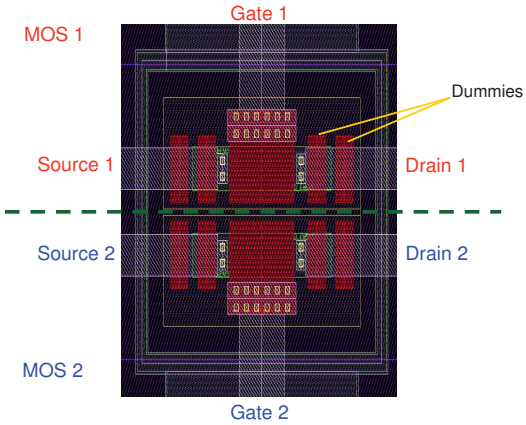


Figure II.35: *Usual test structure.*

This structure is composed of two identical MOSFET transistors (transistor pair), as symmetrical as possible, placed close to each other, at a (quasi-)minimum design rule spacing, in an identical environment. They have common bulk (B) and separate gate (G), drain (D) and source (S) and symmetrical connections. Their currents flux are also in the same direction. Gate

dummies are positioned on both sides of the gate of the transistors. These dummies improve the transistor lithography and etching process.

These structures are regrouped in scribes. Each one has five transistors pairs, totalizing two times twelve connection pads. A scribe is represented in figure II.36. The symmetry between the transistor pair can be noticed.

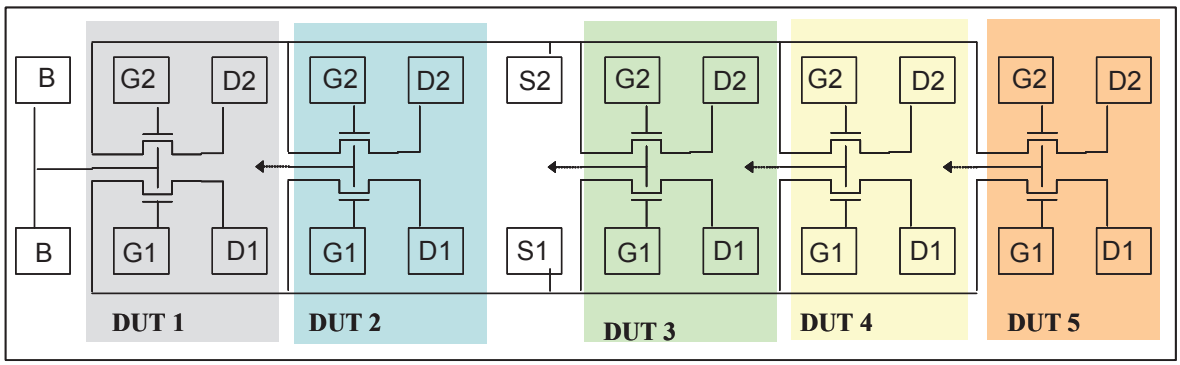
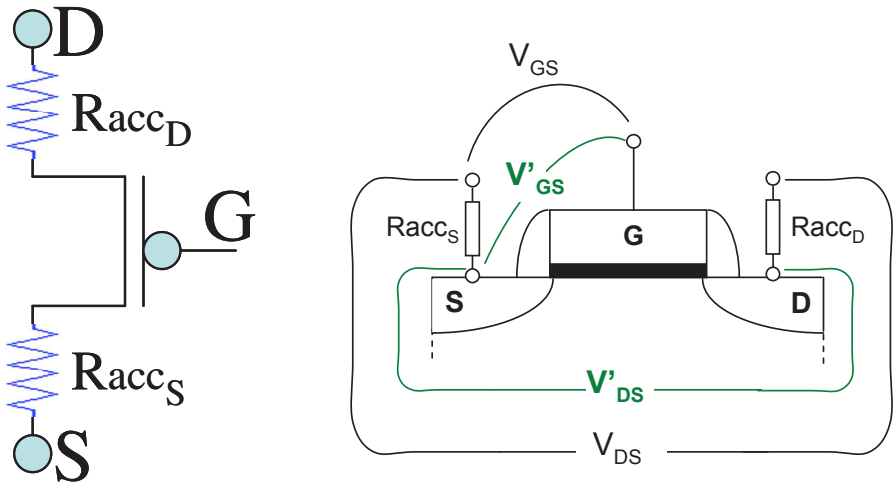


Figure II.36: *Schematic of a scribe composed with five transistors pairs.*

II.9.1 Limitations of test structure

One of the limitations of the presented test structure is the presence of parasitic series resistances (figure II.37). These resistances come from interconnection, contact, source and drain resistances.

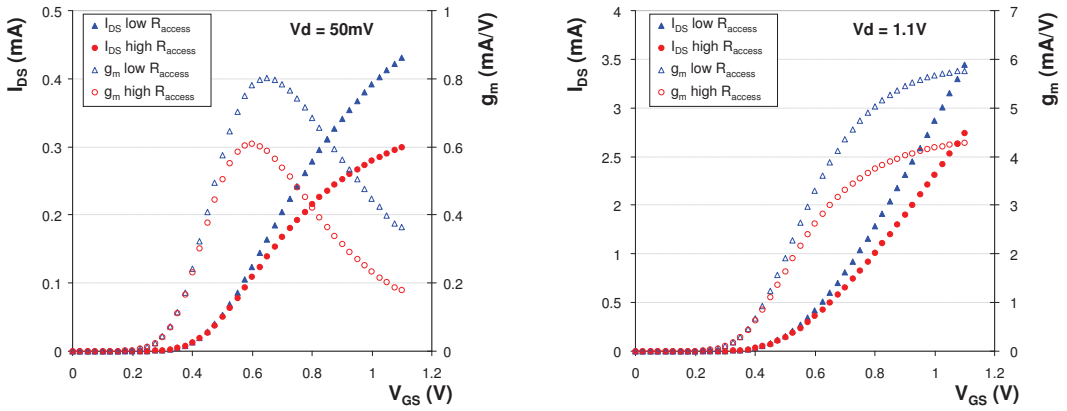


(a) Access resistances (b) Potential drops

Figure II.37: *Transistor with drain and source external access resistances ($Racc_D$ and $Racc_S$, respectively).*

The $Racc_D$ is the access resistance localized between the transistor channel and the drain terminal. The resistance situated between the other side of the transistor channel and the source contact is labeled $Racc_S$. They may be responsible for of an important error in the transistor I_D-V_{GS} characteristics.

The parasitic resistances cause voltage drops and the decreases of drain current. This can be noticed in figure II.38. This figure shows the I_D-V_{GS} characteristics for the same transistor, but with different access resistances (source connections have different metal lengths).



(a) (b)

Figure II.38: *$I_D(V_{GS})$ and $g_m(V_{GS})$ curves on usual test structure for different access resistances on (a) linear regime and (b) saturation regime of operation.*

The one with higher access resistance presents lower drain current for both linear and saturation regions. An effect on transconductance is also noticed, not only in g_m level, but also in the V_{GS} correspondent to $g_{m,max}$. Analyzing figure II.37(b), the effects in the gate and source potentials and in transistor transconducance can be expressed by equations (II.30), (II.31) and (II.32) [Sze 81] [Skotnicki 03].

$$V'_{GS} = V_{GS} - Racc_S I_D \tag{II.30}$$

$$V'_{DS} = V_{DS} - (Racc_S + Racc_D) I_D \tag{II.31}$$

$$g'_m = \frac{g_m}{1 + 2Racc_S\, g_m} \tag{II.32}$$

Substituting the ideal potentials and transconductance (equations (II.30), (II.31) and (II.32)) for the effective ones in equation (II.6), an additional term that depends on Racc_D and Racc_S appears in the Vt. Consequently, the effective Vt changes with a fluctuation in drain or source access resistances. The parasitic resistances have also an influence in the gain factor.

A pertinent question can be posed here: *Does the effect of the parasitic resistances on the electrical parameters has an impact on mismatch?*

To answer it, a mismatch test structure based on Kelvin structure is introduced and discussed in the next section.

II.9.2 Mismatch test structure using Kelvin method

The Kelvin method was invented by William Thomson, Lord Kelvin, in 1861 to measure very low resistances. This method is also known as four-terminal sensing (4T sensing), 4-wire sensing or 4-point probes method. It is a measuring technique that uses separate pairs of current-carrying and voltage-sensing to make more accurate measurements than traditional two-terminal sensing. That is, different terminals are used to apply and measure current/voltage. The accuracy of this technique comes from the fact that no current flows in the sense wires, so the voltage drop is extremely low.

Recently, Kuroda et al. [Kuroda 08] [Kuroda 09] studied the characterization of transistor performance using Kelvin test structures on fully-depleted silicon-on-insulator (FD-SOI) CMOSFETs. They analyzed the short channel transistors intrinsic current- voltage characteristics as well as the quantitative effects of the parasitic series resistance in the device performance. In parallel with this work, Terada et al. [Terada 09] used the Kelvin test structure on MOSFET devices to study the drain current variation under high gate voltage. Their analysis is made using MOSFET arrays circuits, which were also used in [Lefferts 03].

In transistor pair configuration, the structure is symmetrically designed, but the access to the interconnect lines or probe contact resistances of the device, defined here as *external access connections*, might be the source of non-negligible voltage drops when measuring large aspect ratio (width/length) transistors. Hence, Vt mismatch can be impacted by these parasitic resistances during Vt extraction. The Vt is not the only constraint: β and I_D are some examples of other parameters which are influenced by parasitic resistances [Kinget 05].

To verify if the parasitic resistances introduce characterization errors on mismatch, a mismatch test structure is proposed [Mezzomo 09b]. This test structure is based on the four-terminals Kelvin method on transistor pair configuration, represented in figure II.39.

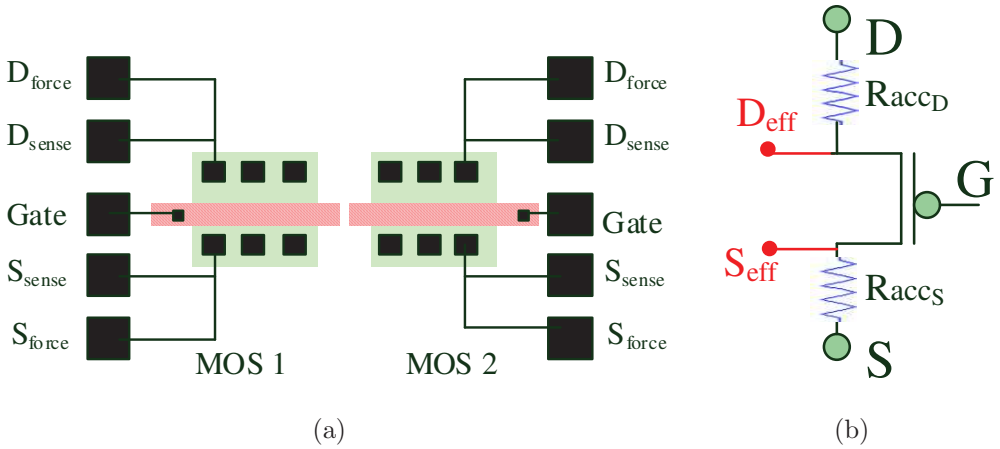


Figure II.39: *Mismatch test structure using Kelvin method. (a) Schematic layout showing the terminals and (b) schematic view of one transistor with force (D and S) and sense terminals (D_{eff} and S_{eff}).*

The difference between this Kelvin mismatch test structure II.39 and the conventional one II.35 is that drain and source have two connections called force and sense terminals. These two additional terminals allow the measurement of the effective biasing applied to the device. In addition, an algorithm is used to correct the transistor biasing, by compensating the potential drops caused by the parasitic resistances.

To observe the impact of external access resistances, the Kelvin mismatch test structure is used in three different ways:

1. **as the Kelvin mismatch structure:** it has force and sense terminals to the drain and to the source (figure II.39(a)). While force terminals are used to supply current or voltage, sense terminals are used to voltage or current measurement. To make it available, an algorithm of polarization is applied to compensate voltage drops due to parasitic resistances, which will be detailed later. Hence, the effective drain and source measures (D_{eff} and S_{eff}) do not include the parasitic resistances (figure II.39(b)).

2. **as conventional test structure with short access to source and drain terminals:** the Kelvin test structure is used as a conventional one, where only the closest connections to transistor channel are used (figure II.40). In this work, this test structure is labelled as "*short access*" test structure.

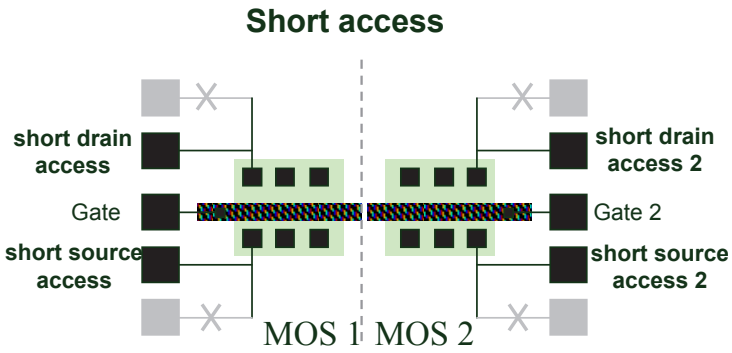


Figure II.40: *Schematic layout of Kelvin test structure used as conventional test structure with short access to source and drain terminals.*

3. **as conventional test structure with long access to source and drain terminals:** the Kelvin test structure is used as a conventional one, where only the longest paths are used. Consequently, it is more resistive than that with *short* access connextions (figure II.41). In this work, this test structure is labelled as "*long access*" test structure.

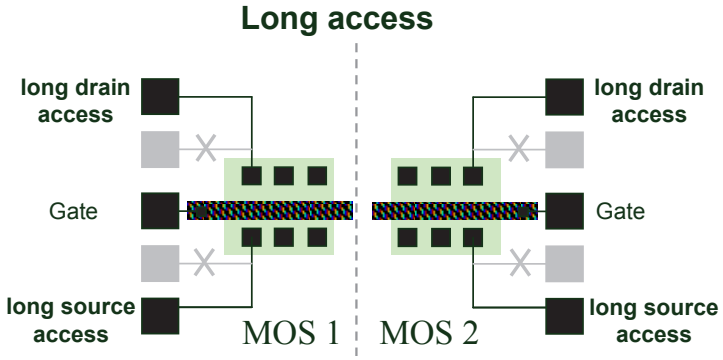


Figure II.41: *Schematic layout of Kelvin test structure used as conventional test structure with long access to source and drain terminals.*

II.9.2.a Algorithm of polarization

The following algorithm was developed in order to adjust the transistor biasing on the Kelvin test structure (figure II.42).

Nominal gate (V_{GS}) and drain (V_{DS}) voltages are forced, and the effective V_{GS}/V_{DS} voltages are measured by source/drain sense terminals. Then, forced terminals biases (first the gate and then the drain) are adjusted until electrical potential drops caused by external access resistances (probe contacts and interconnection lines) are compensated, by bringing the effective gate and drain voltage (V_{GSeff} and V_{DSeff}, respectively) to nominal values. Once these steps are over, V_{GS} and V_{DS} are able to supply the voltage drops. Then, mismatch parameters can be measured.

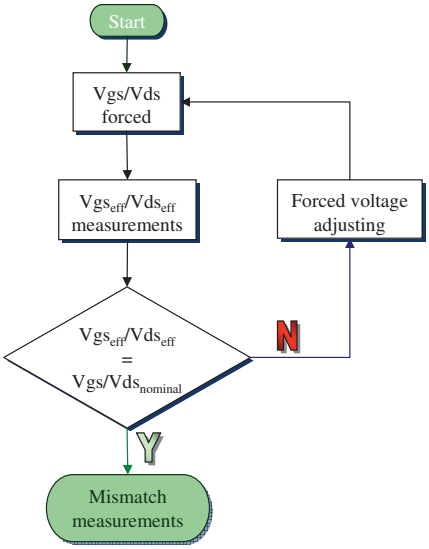


Figure II.42: *Algorithm flow to adjust forced terminals.*

The introduction of this algorithm in the characterization flow can increase the measurement time. However, a maximum of four iterations is needed to achieve the correct V_{GS} values, as shown on the example of figure II.43.

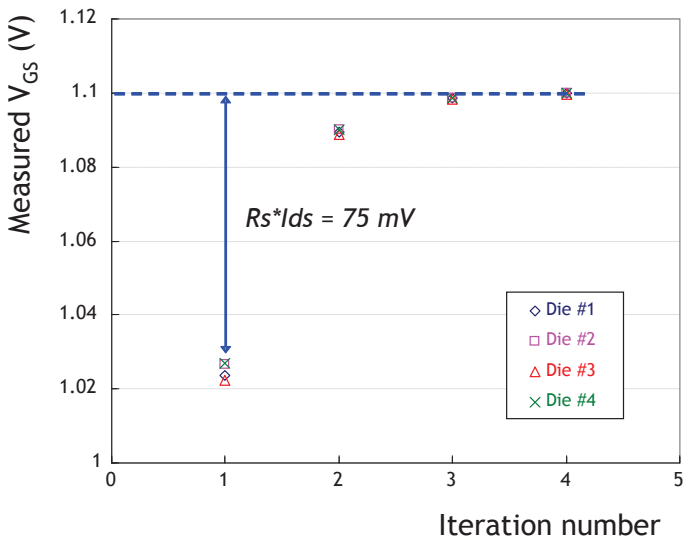


Figure II.43: *Number of iterations to adjust V_{GS} value on four different dice. Initial V_{GS} voltage differs of 75mV from the nominal one.*

In this example, the effective gate-to-source voltage as a function of the number of iterations for different dice is presented. The initial V_{GS} voltage differs of 75mV from the nominal one.

II.9.2.b Results and discussion

In this section, the threshold voltage, the gain factor and the drain current mismatch are characterized and discussed. Both NMOS and PMOS devices have been measured. Table II.3 shows the geometries and the corresponding drain voltage of the devices under test.

Table II.3: *Transistors geometries for N and PMOS devices.*

$W\ (\mu m)$	L (μm)	t_{ox} $(\AA)$	V_{DD} (V)
10	0.15	17	1.1
5	0.15	17	1.1
10	0.27	32	1.8

The geometries with higher W/L ratio have higher current and then, the impact of the external access resistance is easily noted. Thus, NMOS devices are expected to be more impacted by external access resistances than PMOS devices, as the current in PMOS devices is lower.

Threshold voltage mismatch Figure II.44 shows Vt experimental results of the transistor pair (MOS1 and MOS2) for the three studied test structures. It points out that Vt values are not the same for *long access*, *short access* and Kelvin mismatch structures. This demonstrates that Vt is impacted by external access resistances. The *long access* structure has the lowest Vt because it has the highest access resistance, thus the highest potential drop. Consequently, the Vt obtained using the standard structure may present a distortion due to access resistances. The correct value is given with the Kelvin structures, which is higher than the others. For devices where the W/L ratio are small, Kelvin and *short access* presents close results.

The Vt values of MOS1 are not exactly the same as values obtained on MOS2, indicating that Vt mismatch does exist. Although there is Vt shift between the different test structures, it is not sure that it impacts the mismatch.

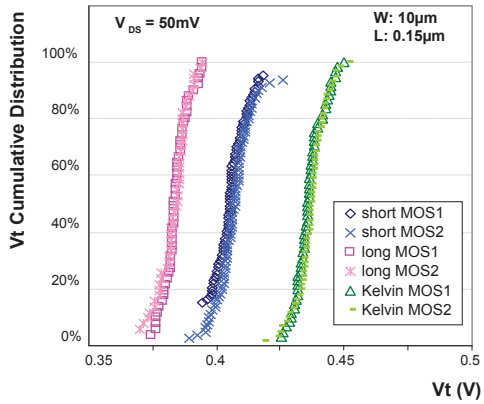
Therefore, the impact of external access connections on Vt mismatch is evaluated.

On figure II.45, the cumulative distribution of ΔVt variations is shown. Although there is a Vt shift between the test structures, the mismatch of Vt is not impacted. It is possible to notice the three ΔVt curves corresponding to *short access*, *long access* and Kelvin structures are superimposed. Also, the cumulative distribution is centered in zero. The $A_{\Delta Vt}$ mismatch parameter is shown in figure II.46 for each test structure. It shows that the Vt mismatch are the same, independently of the test structure. Thus, external access connections have no impact in Vt mismatch.

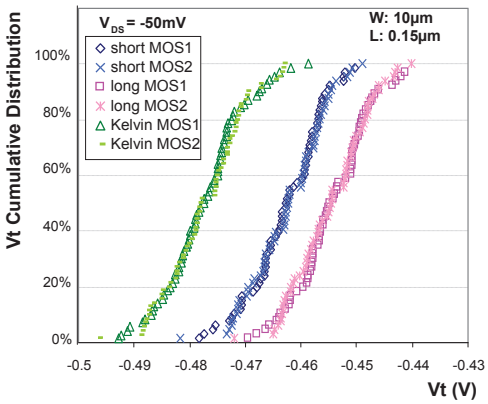
Consequently, conventional test structures, which have less a more simple design and take less time to measure compared to Kelvin strucutres, can be used to measure Vt mismatch for this low power 45nm technology node.

Gain factor mismatch The same method used for the threshold voltage can also be used for the β electrical parameter. The gain factor cumulative distribution has the same behavior as for the Vt for both N and PMOS devices, which means that the β cumulative distribution are not the same for *short access*, *long access* and Kelvin mismatch structures. The long structure has the lowest β because it has the highest access resistance and then the highest potential drop.

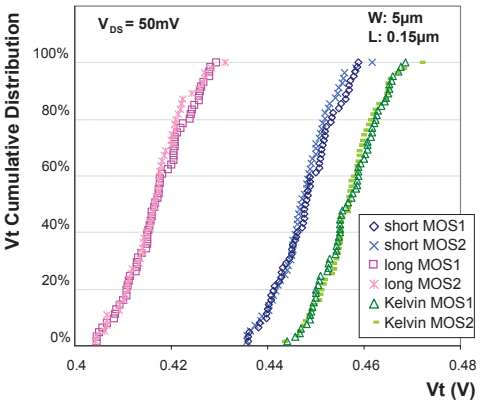
Analyzing $\Delta\beta/\beta$ mismatch, the same conclusion as Vt mismatch could not be made. The mismatch of $\Delta\beta/\beta$ is less obvious. Different results are obtained when using the *short access*, the *long access* or the Kelvin structure for NMOS devices (figure II.48).



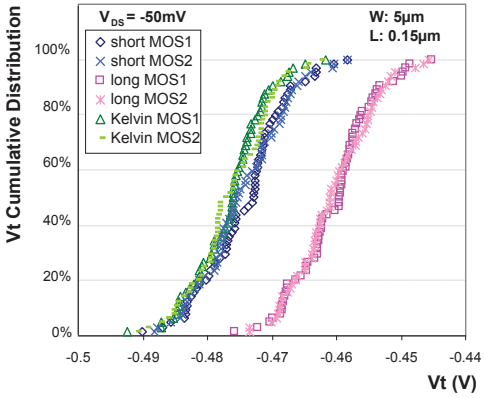
(a) NMOS W/L = 10/0.15



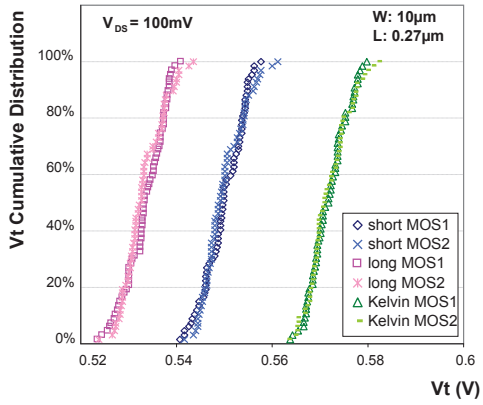
(b) PMOS W/L = 10/0.15



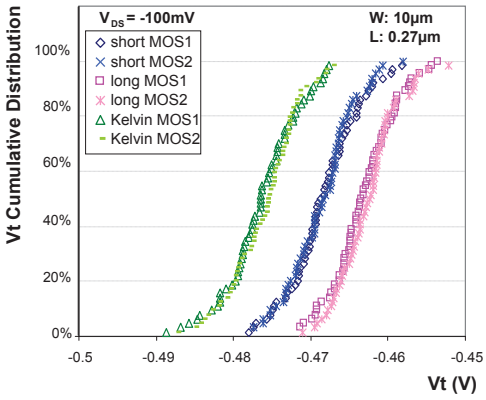
(c) NMOS W/L = 5/0.15



(d) PMOS W/L = 5/0.15



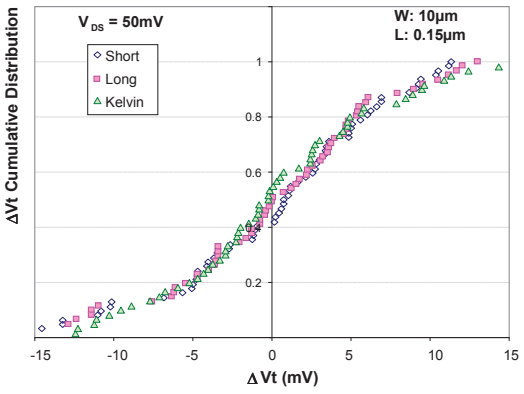
(e) NMOS W/L = 10/0.27



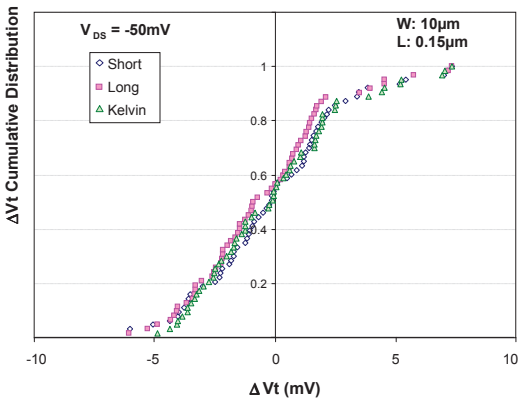
(f) PMOS W/L = 10/0.27

Figure II.44: *Cumulative distribution of Vt for transistor pair (MOS1 and MOS2) for short and long access and Kelvin structures.*

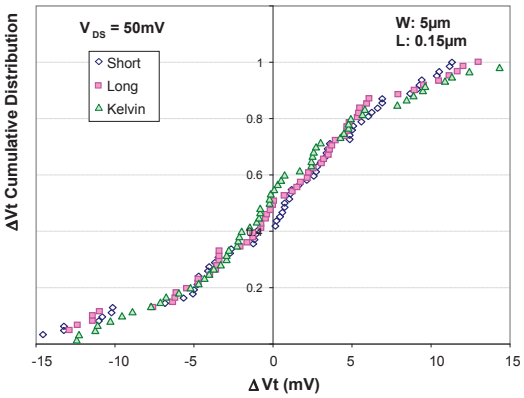
Figure II.48(a)(c) and (e) represent the $\Delta\beta/\beta$ cumulative distribution for NMOS devices. For the geometry with the highest W/L ratio (figure II.48(a)), the *short access* structure is not centered on zero. Results obtained on Kelvin test structures do not exhibit good performances either. The $\Delta\beta/\beta$ mismatch ($A_{\Delta\beta/\beta}$) is represented in figure II.47. It shows that the three structures present different level of mismatch for the geometry with the highest W/L ratio. For



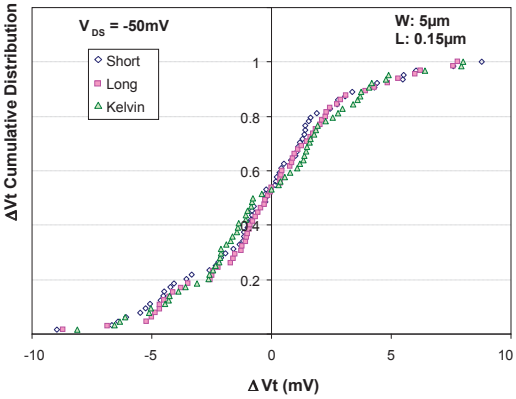
(a) NMOS W/L = 10/0.15



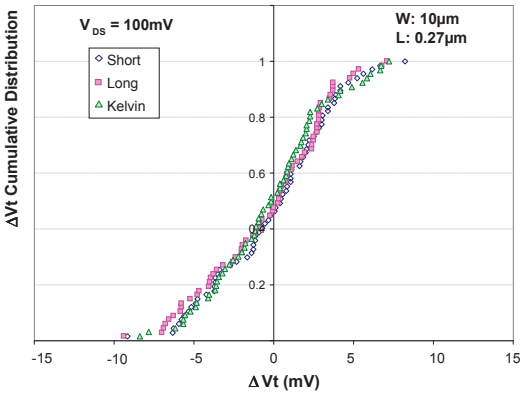
(b) PMOS W/L = 10/0.15



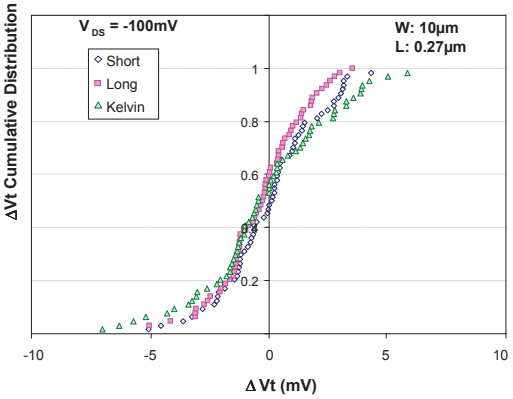
(c) NMOS W/L = 5/0.15



(d) PMOS W/L = 5/0.15



(e) NMOS W/L = 10/0.27



(f) PMOS W/L = 10/0.27

Figure II.45: *Cumulative distribution of ΔVt for short and long access and Kelvin structures.*

the other two geometries, there are no important differences.

For PMOS devices, the $\Delta\beta/\beta$ distributions are well centered on zero. Analyzing the values for $\Delta\beta/\beta$ mismatch ($A_{\Delta\beta/\beta}$) represented in figure II.47, no difference between *short access*, *long access* and Kelvin structures are observed. These results are not surprising, as PMOS devices have small drain current. As the weaker is the drain current, smaller is the importance of access

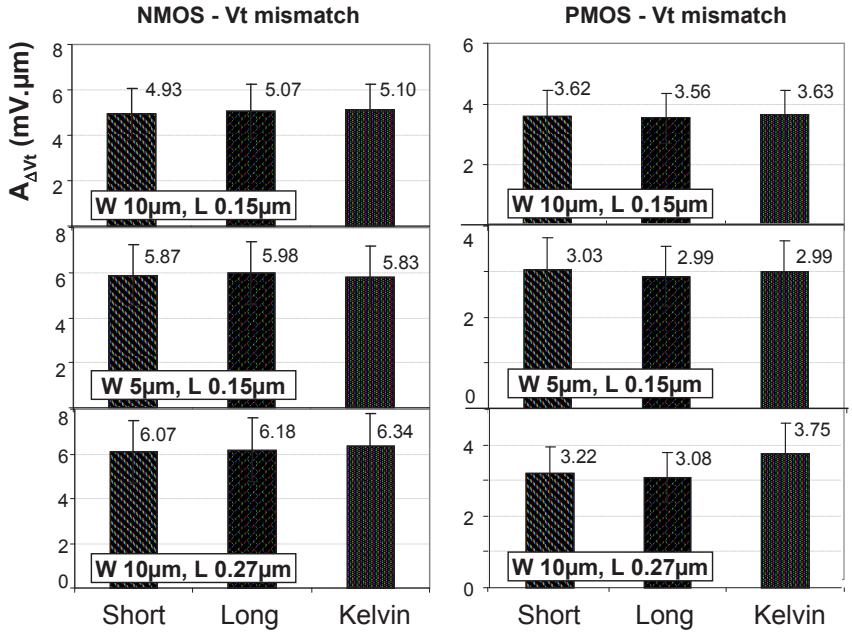


Figure II.46: *$A_{\Delta Vt}$ mismatch parameter for NMOS (left side) and PMOS (rigth side) transistors.*

resistances in the gain factor parameter.

As seen before, the access resistances have no impact in the Vt mismatch. However, no clear tendency could be pointed out for the $\Delta\beta/\beta$ mismatch. Then, as the drain current mismatch is represented by a mismatch in Vt and β parameters, the I_D mismatch is analyzed hereafter to check if it can clarify the results obtained here.

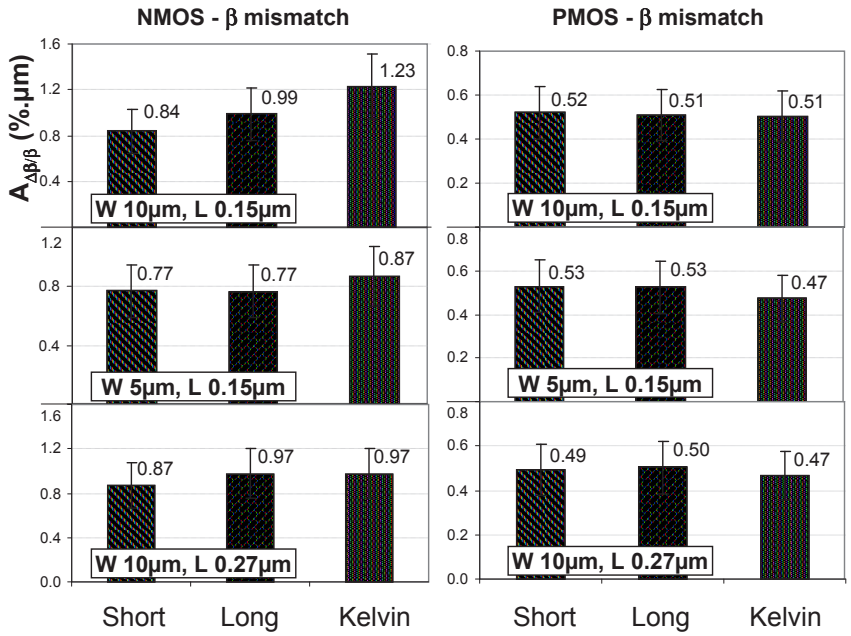
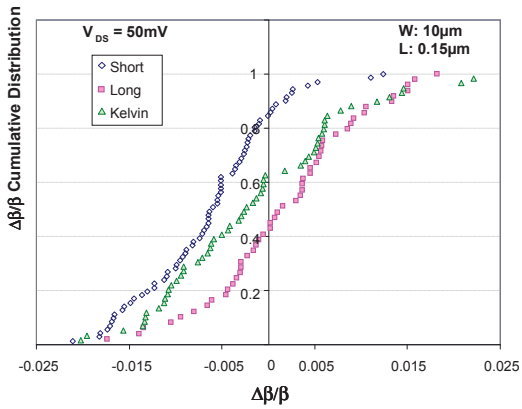
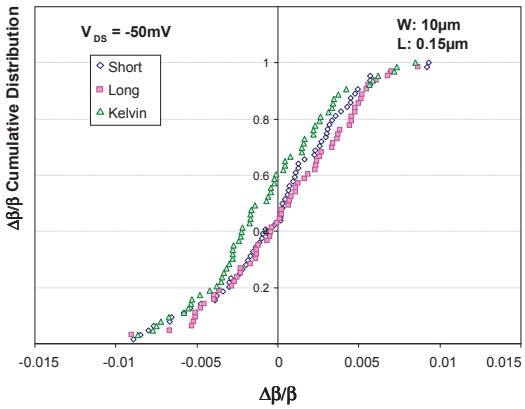


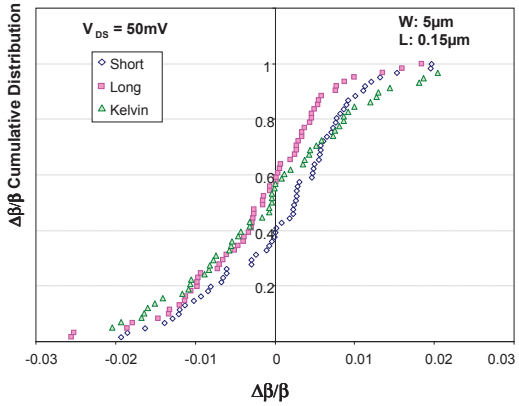
Figure II.47: *$A_{\Delta\beta/\beta}$ mismatch parameter for NMOS (left side) and PMOS (rigth side) transistors.*



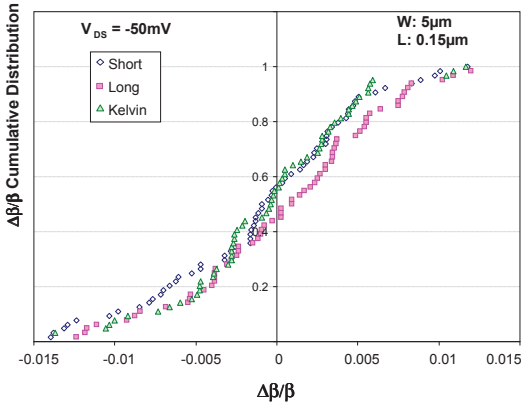
(a) NMOS W/L = 10/0.15



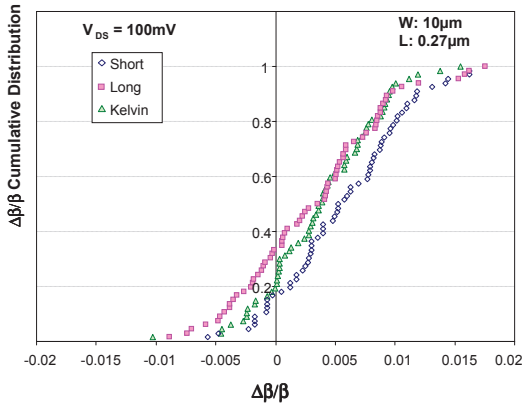
(b) PMOS W/L = 10/0.15



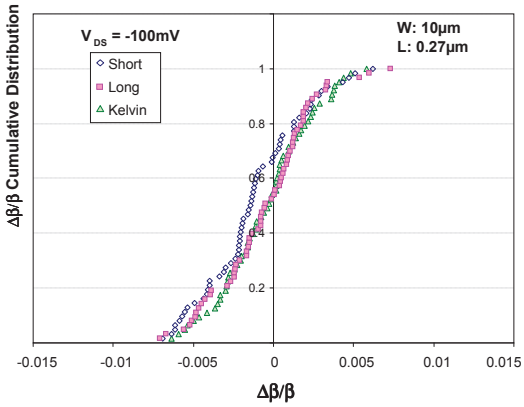
(c) NMOS W/L = 5/0.15



(d) PMOS W/L = 5/0.15



(e) NMOS W/L = 10/0.27



(f) PMOS W/L = 10/0.27

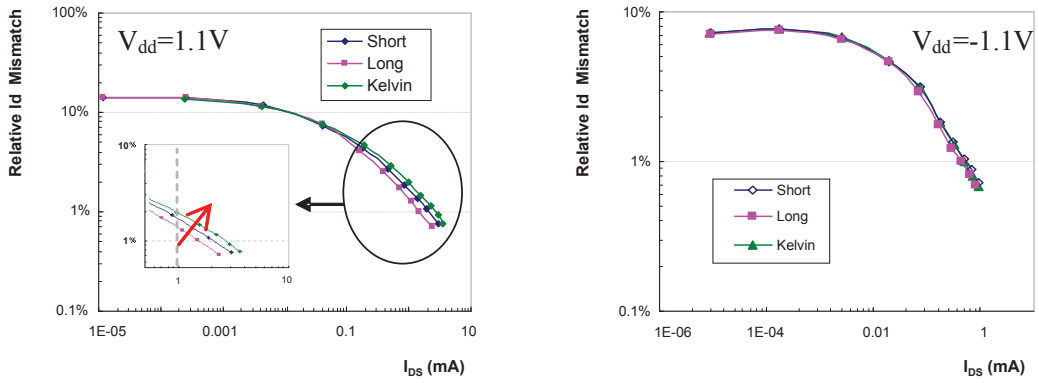
Figure II.48: *Cumulative distribution of $\Delta\beta/\beta$ for short and long access and Kelvin structures.*

Drain current mismatch The last parameter which is analyzed is the drain current I_D. Drain current mismatch is a significant technological indicator.

The drain current mismatch is then analysed for *short access*, *long access* and Kelvin mismatch test structures. Among the different geometries analyzed, the external access resistances have more effect on the one with higher W/L ratio ($10\mu m/0.15\mu m$). For these reason, only the

results obtained with this geometry are shown.

Figure II.49 shows the relative mismatch of $\Delta I_D/I_D$ at V_{DS}= 1.1 V. For NMOS transistors, the more resistive is the access connection to the device, the more drain current mismatch is underestimated when using the conventional test structure. No differences are observed for PMOS devices, as this type of transistor has weaker drain current. Hence, for this 45nm technology node, the difference among the three test strucutes are insignificant. Then, the conventional test structures is adapted for the mismatch study in this technology. However, for high-voltage purposes, the parasitic resistances can no longer be ignored and the Kelvin mismatch test structure is recommended.



(a) NMOS W/L = 10/0.15 (b) PMOS W/L = 10/0.15

Figure II.49: *The $\Delta I_D/I_D$ mismatch as a function of drain current for short and long access and Kelvin structures.*

II.9.3 Discussion of mismatch test strucure using Kelvin method

It has been shown that external access connections do not affect the Vt mismatch neither the relative drain current mismatch for this 45nm technology node, even if the intrinsic extracted Vt has different value with standard structures. Consequently, for the mismatch study, the conventional test structure can be used. The conventional test structure have less complexity and are faster than Kelvin test structure. In addition, it is convenient to use a faster test structure as a lot of data is required on mismatch studies.

The mismatch of β for PMOS transistors presented similar results for the conventional *short access*, *long access* and Kelvin test strucutes. On the other hand, the mismatch of β for NMOS transistors depends on the access layout, introducing uncertainty in its determination for this technology node.

It is important to keep in mind that devices with high current can be affected by the external access resistances. The Kelvin mismatch test structure is recommended to be used in these cases.

II.10 Conclusions Chapter I

In this chapter, the main concepts of the MOS transistor mismatch were presented. It was shown that mismatch is crucial for both analog and digital applications. In the state of the

art, it was shown that random dopants is the critical source of fluctuations for this technology node and line edge roughness is indicate to be a major challenge for future technologies. These two sources of fluctuations will be analyzed in next chapters, paying more attention for random dopants.

The measurement methodology was presented and the three steps concerning the methodology - measurement, data treatment and mismatch analysis - were described. Concerning electrical parameter extraction, the focus is to analyze electrical parameter differences and not the intrinsic value of the parameter. As a lot of data is necessary, a quick method with good repeatability is required. To this aim, in most part of this work the maximum slope method is used. Only for some specific studies the constant current method is used.

Afterwards, the mismatch parameter extraction using the conventional mismatch test structure for the 45nm STMicroelectronics technology was validated. In order to do so, a mismatch test structure based on the Kelvin method was introduced. For that technology, the conventional test strucutre is adapted for the mismatch study. It is important to keep in mind that devices with high current can be affected by the external access resistances. The Kelvin mismatch test structure is recommended to be used in these cases.

Chapter III

Random dopants impact on mismatch in linear regime for transistors with pocket implants

In this chapter, random dopants fluctuations are investigated in linear regime. Doping fluctuations have been shown to be the main physical origins of the mismatch. In particular, local random doping fluctuations due to pocket implants are analyzed. The influence of the pocket implants on mismatch is introduced, followed by a pocket engineering study focusing on the addition of co-implants near source and drain regions to reduce the mismatch. In the sequence, a mismatch model valid from weak to strong inversion regions is presented and discussed.

III.1 The evolution of mismatch with transistor miniaturization

In the previous chapter, pocket implants were shown to avoid short channel effects. But, these pocket implants degrade transistor mismatch, especially for long transistors. In order to underline these effects, experimental results comparing devices with and without pocket-implants are shown for threshold voltage parameter. Then, it will be shown what are the problems for transistor with pocket implants. After analyzing transistor mismatch for threshold voltage parameter, the mismatch for the gain factor parameter is then experimentally shown for the 45nm technology node.

To quantify the local fluctuations, Pelgrom et al. [Pelgrom 89] introduced a mismatch parameter $A_{\delta P}$. Its estimation is made by a model (equation (II.9)) that uses linear regression, experimentally represented in figure III.1. This model is now known as the Pelgrom scaling law for mismatch issues.

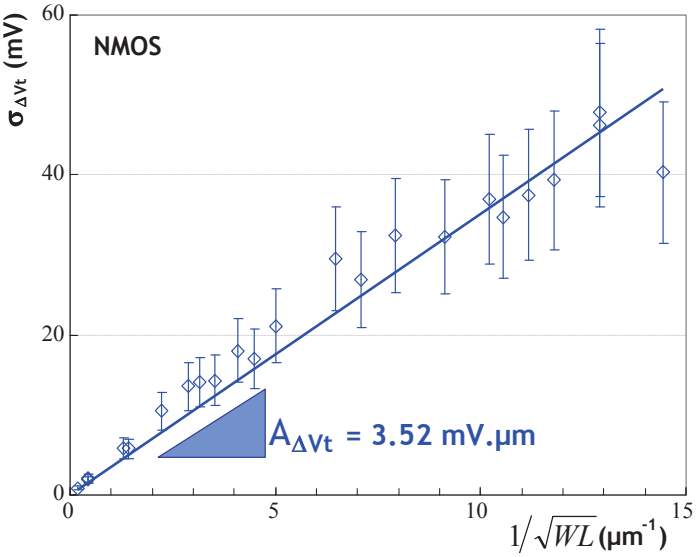


Figure III.1: *Experimental threshold voltage mismatch.*

This methodology was improved by Cathignol et al. [Cathignol 06a] for better accuracy on the characterization of transistor mismatch. They proposed the replacement of the conventional least squares regression by a weighted least squares regression (figure III.2). In this new methodology, the normalized standard deviation is estimated for each transistor geometry (equation (III.1)),

$$iA_{\delta_P} = \sigma_{\delta P_i}\sqrt{W_i L_i} \tag{III.1}$$

where iA_{δ_P} is the individually normalized mismatch.

Then, the A_{δ_P} consists in averaging the iA_{δ_P}, yielding equation (III.2),

$$A_{\delta_P} = \frac{1}{n_{geo}} \sum_{i=1}^{n_{geo}} iA_{\delta_P} \tag{III.2}$$

where n_{geo} is the number of geometries.

The dispersion of A_{δ_P} can be reduced due to this weighted methodology. Consequently, better detection of physical effects responsible for mismatch is achievable [Cathignol 06a]. For these reasons, this methodology is used in this work.

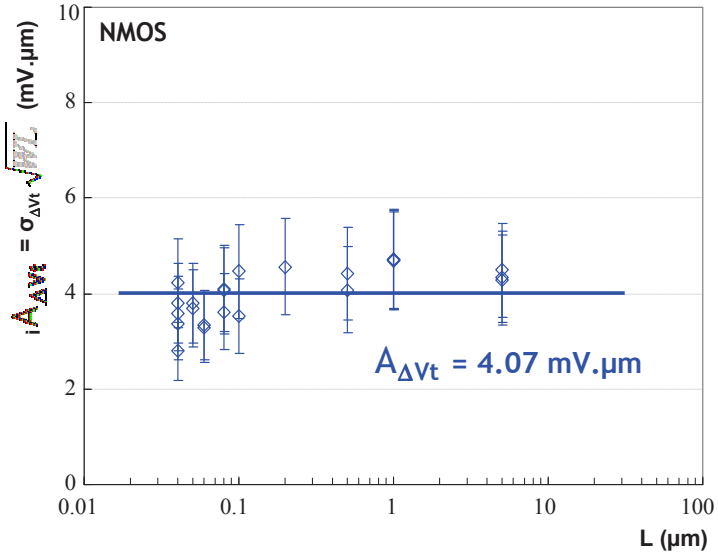


Figure III.2: *Experimental scaling law-normalized mismatch.*

For the threshold voltage, another approach can also be derived from equation (II.9). It is obtained considering the random numbers of channel impurities controlling the depletion charge under the gate, yielding [Lakshmikumar 86] [Mizuno 94] [Stolk 98]:

$$\sigma_{Vt} = \frac{1}{C_{ox}}\sqrt{\frac{qQ_{dep}}{4WL}} \tag{III.3}$$

This equation allows to obtain the Vt mismatch parameter for the channel as (equation (III.4)):

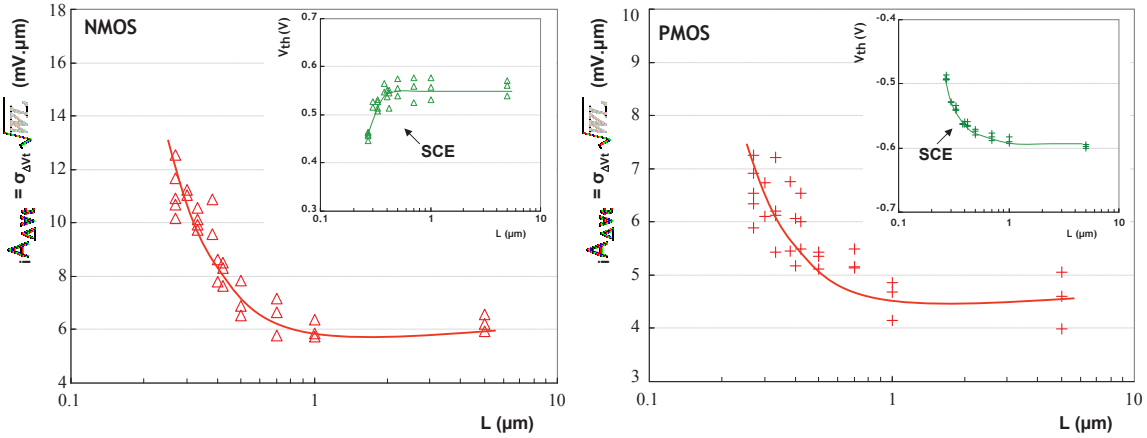
$$A_{Vt,ch} = \frac{t_{ox}}{\varepsilon_{ox}}\frac{\sqrt[4]{2q\varepsilon_{Si}N_a(2\phi_F - V_{BS})}}{2} \tag{III.4}$$

where $\varepsilon_{ox,Si}$ is the oxide/silicon permittivity and Na is the channel doping concentration. These equation shows that $A_{Vt,ch} \propto Na^{0.25}$.

Equations (II.9) and (III.4) have physical bases and provides satisfactory accuracy in many cases. However, these models are not valid for the whole device geometry range [Croon 00] [Difrenza 03a] [Stolk 98], because one or several hypotheses that these laws relied on [Pelgrom 89] are no longer valid.

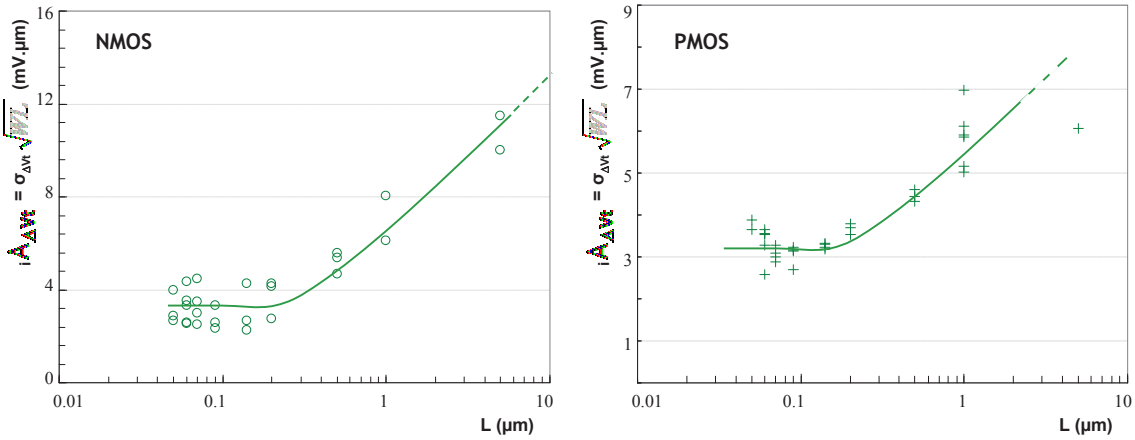
One reason why scaling law is not followed is due to short channel effects. Figure III.3 shows an example of threshold voltage roll-off due to SCE and the respective effect on threshold voltage mismatch. As it can be noticed for both NMOS and PMOS transistors, fluctuations are higher for short transistors. Mismatch issues for short device has been widely observed and was explained by the global increase of impurities concentration in the channel [Difrenza 00] [Mc Ginley 04].

To avoid SCE, pocket regions are implanted near drain and source regions. These implants should lead to an increase of the mismatch, as shown in figure III.4. In this figure, the experimental $iA_{\Delta_{Vt}}$ for low power (LP) 65nm MOSFET technology is shown. It should be noticed that small gate lengths can be modeled by equation (II.9), indeed the level of fluctuations is higher than in devices without pocket-implants. For gate lengths higher than 0.1μm, the normalized mismatch increases and Pelgrom's model is no longer valid. Thus, the increase of fluctuations is attributed to the pockets implants [Croon 02a] [Mc Ginley 04] [Johnson 08].



(a) NMOS (b) PMOS

Figure III.3: *Impact of short channel effect on threshold voltage mismatch.*



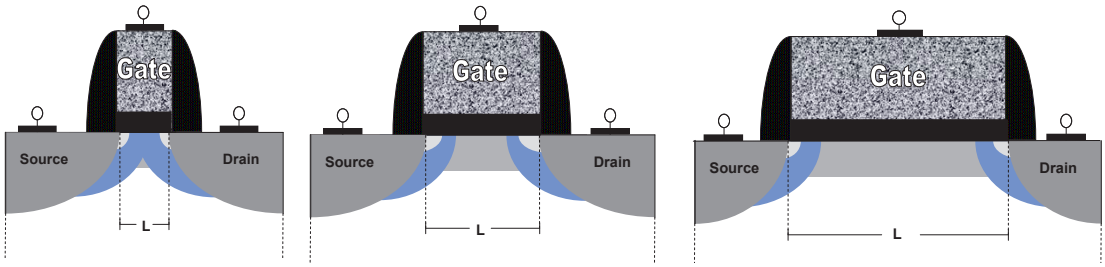
(a) NMOS (b) PMOS

Figure III.4: *Experimental mismatch behavior as a function of gate length in 65 nm pocket architecture on bulk MOSFET technology.*

The modeling of mismatch in devices with pocket implants has first been conceived based on the weighted summation of the variances associated to the channel and pocket regions [Difrenza 00] [Rios 02]. That model allows understanding the increase of fluctuations for short gate lengths. This model have shown strong limitations in sub 65nm CMOS technologies, where very high doping level contrast exists between the low doped channel and the heavily doped pocket regions. It cannot explain the abnormal increase of Vt mismatch observed for relatively long gate lengths.

In previous figure (figure III.4), it should be noted that $\sigma_{\Delta Vt}$ for short transistors is inversely proportional to $\sqrt{WL}$. Short transistors with pocket implants also have a uniform channel, as pocket regions are superimposed (figure III.5(a)). As pocket regions are heavily-doped, short devices with pocket implants present heavily-doped channel. Equation (III.4) shows a proportional dependence of the mismatch parameter and the channel doping ($A_{Vt,ch} \propto Na^{0.25}$). Asenov [Asenov 99] showed that, for short transistors, this proportionality is stronger, where $A_{Vt,ch} \propto Na^{0.401}$. Thus, for uniform devices, transistor with pocket-implants presents more fluctuations than devices without pocket implants.

Moreover, only long transistors do not follow the normalized mismatch. For long transistors (figure III.5(b)), pocket regions become separated. As pocket regions are heavily-doped compared to the channel, a non-homogeneous channel is formed.



(a) Short transistor (b) Long transistor (c) Very long transistor

Figure III.5: *Schematic of a transistor cross section view for different gate lengths.*

Cathignol et al. [Cathignol 08a] [Cathignol 09] explain that the rather long devices present strong potential barriers at both source and drain regions, giving these barriers a major role in the control of Vt. These potential barriers are represented experimentally in figure III.6.

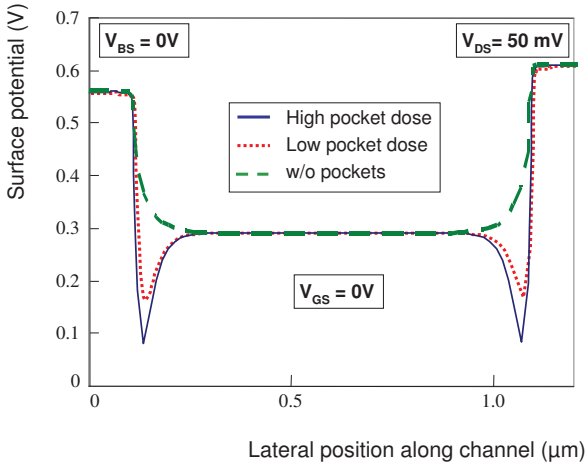


Figure III.6: *Surface potential in the lateral position along the channel. Stronger potential barriers are observed for the transistor with pocket implants [Cathignol 09].*

These barriers are responsible for Vt fluctuations, independently of the gate length. As the potential barriers control Vt independently from the L, the Vt mismatch is also independent of the length and the $\sigma_{\Delta Vt}$ remains constant with increasing length. Thus, as can be noticed in figure III.4, if the mismatch is normalized by the square root of the transistor area ($\sigma_{\Delta Vt}\sqrt{WL}$), the $iA_{\Delta Vt}$ increases with increasing length.

As shown in previous figure (III.6), the higher is the contrast between pocket and channel doping, the stronger is the potential barriers near source and drain. The $\sigma_{\Delta Vt}$ depends on doping concentration ($\sigma_{\Delta Vt} \propto Na^{0.25}$ [Takeuchi 97]). Following figure (figure III.7) schematically shows the effect of different pocket and channel doses in the mismatch. For short transistors, more $\sigma_{\Delta Vt}$ fluctuations are observed as higher is the level of pocket doping. For long transistors, in addition to the level of pocket doping, more $\sigma_{\Delta Vt}$ fluctuations are observed as higher is the pocket and channel doping contrast.

Pocket implants have also an effect on gate bias for long devices. Figure III.8 shows that local fluctuations increase as V_{GS} decreases for long transistors.

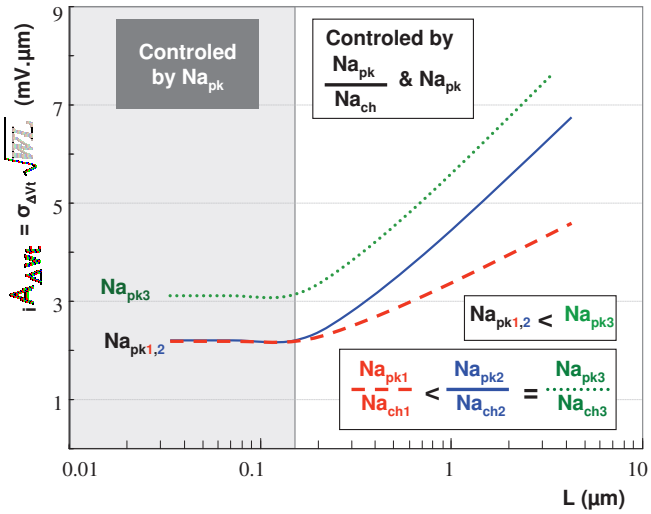


Figure III.7: *Schematic of the influence of pocket and channel doping levels on the treshold voltage mismatch.*

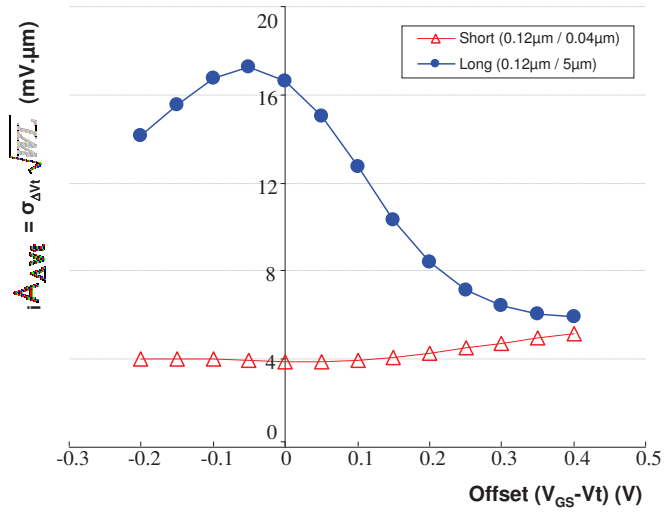


Figure III.8: *Experimental mismatch behavior as a function of gate bias for short (homogeneous channel) and long (non-homogeneous channel) transistors.*

The increase of fluctuations as a function of gate bias is also explained by the presence of a non-homogeneous channel [Cathignol 09]. As gate biasing grows, the barrier height decreases along with the ability to control current flow. This makes a device with pocket implants similar to a device without pockets (figure III.9). Thus, these barriers are responsible for local fluctuations. These effects were also observed by [Hook 10] for a 32nm technology node with high-k metal gate, which confirms that the effects are related to doping only.

Figure III.10 shows threshold voltage mismatch for a 45nm technology node. For NMOS transistors, the mismatch increases for gate lengths higher than 0.1μm. However, the mismatch decreases for very long transistors, getting closer to the fluctuations level obtained if the scaling law is followed. For very long transistors, the drain and source pocket regions are outspread, making the channel area much bigger than the pocket area. The channel in this case is quasi-homogeneous (figure III.5(c)). Thus, very long transistors are expected to present the same behavior as a transistor without pocket.

The NMOS transistors present high fluctuations level compared with PMOS devices. In

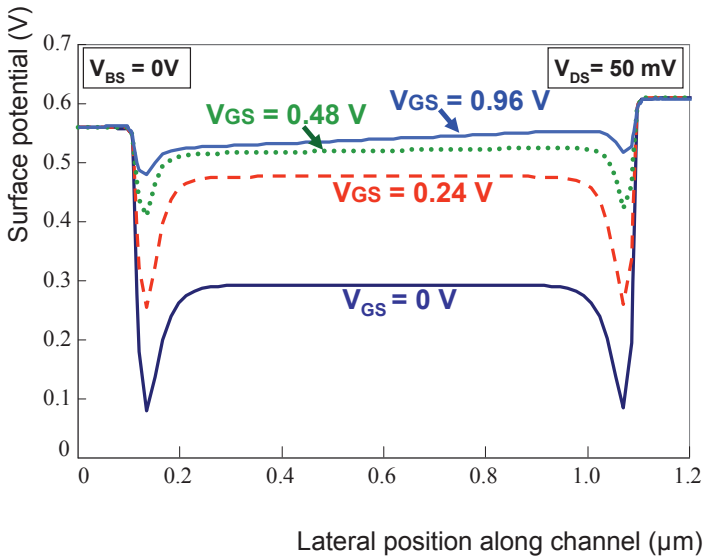
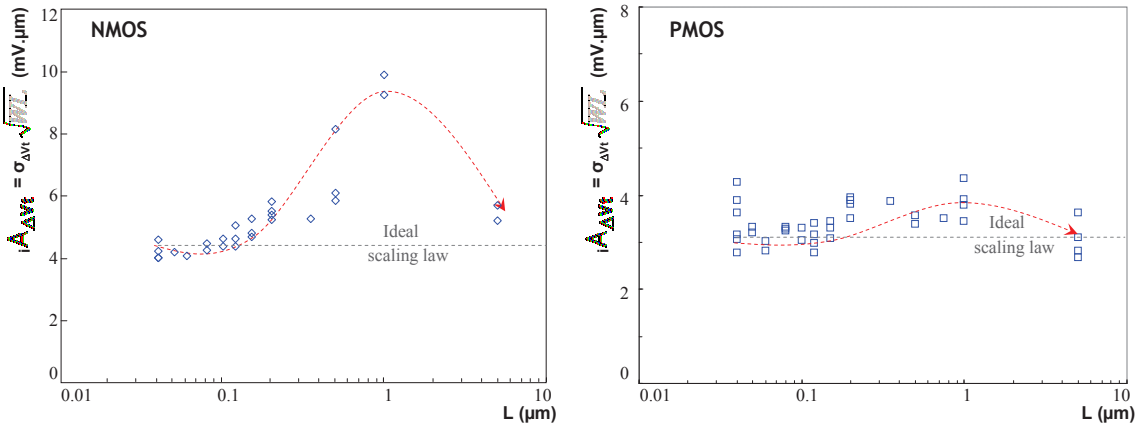


Figure III.9: *Surface potential in the lateral position along channel for various gate bias conditions [Cathignol 09].*



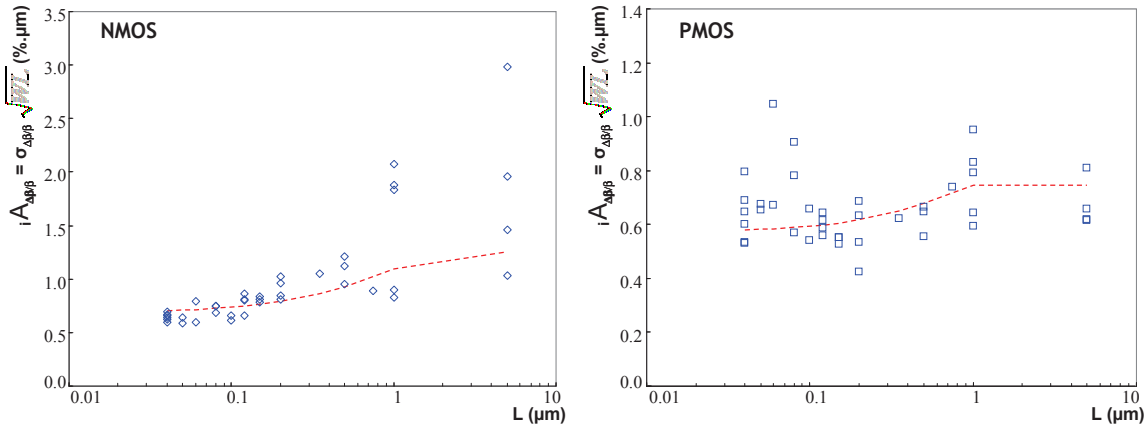
(a) NMOS (b) PMOS

Figure III.10: *Experimental mismatch behavior in 45nm pocket architecture on bulk MOSFET technology. The linear dashed line represents the scaling law.*

addition, the hump observed on PMOS devices are attenuated. That difference will be studied in following sections (§III.3.4).

Figure III.11 shows the relative gain factor mismatch ($A_{\Delta\beta/\beta}$) for the 45nm technology. As it can be noticed, $A_{\Delta\beta/\beta}$ also increases for long lengths.

It has been shown that pocket implants have strong influence on transistor mismatch. A pocket engineering study is then performed for NMOS transistors with the aim to reduce the level of fluctuations on NMOS transistors, especially for the long ones.



(a) NMOS (b) PMOS

Figure III.11: *Experimental gain factor mismatch behavior in 45 nm pocket architecture on bulk MOSFET technology.*

III.2 Pocket engineering impact on mismatch

The previous section has analyzed the influence of pocket-implants on transistor mismatch. The aim of this section is to investigate ways for reducing the mismatch on NMOS transistors, especially for long devices. For that, STMicroelectronics engineers have modified the architecture of the transistor, implanting an additional pocket and making use of co-implants. These are combined with various materials.

The transistor architecture used is presented, followed by an explanation about the properties of co-implants. Finally, the mismatch is analyzed and discussed [Mezzomo 09a].

III.2.1 Architecture of transistor with pocket co-implants

The architecture of transistors with pocket co-implants has double pocket regions. These regions are denominated as "*Pocket 1*" for the deeper pocket and "*Pocket 2*" for the shallower (figure III.12).

Pocket 2 is closer to the transistor channel than *Pocket 1*. Thus, it has more influence on the channel, and on the electrical parameters that rely on it, as threshold voltage, gain factor and drain current.

To reduce the impact of pockets on mismatch performances, five different recipes are used (table III.1).

The first one is doped with BF_2 and is taken as the reference. In the others splits, in addition to BF_2, Indium (In) is used as dopant. Other trials are also done adding Carbon (C) and Nitrogen (N).

In order to understand why these materials have been chosen, co-implant properties are now introduced.

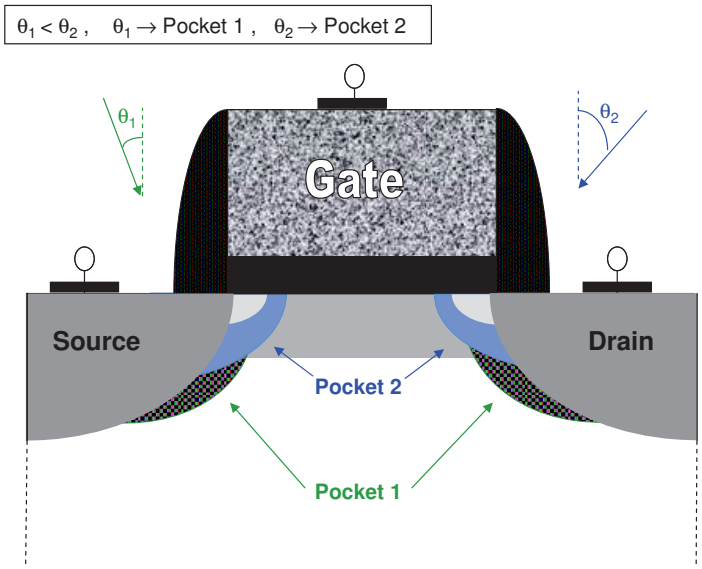


Figure III.12: *Schematic of transistor cross-view with double pocket regions: Pocket 1 and Pocket 2. The smaller is the applied tilt, the deeper is the pocket region.*

Table III.1: *Split presentation for study of the impact on NMOS mismatches using Indium.*

Implant type
BF_2 (reference)
BF_2 + In
BF_2 + In + C
BF_2 + In + N
BF_2 + In + C + N

III.2.1.a Co-implants properties

BF_2 implantation: In the case of BF_2 implantation, the large amount of Boron diffuses in the region close to the silicon channel surface. This results in the decrease of the drive current due to the higher channel resistance with a strong reverse short channel effect [Mineji 06]. To solve these problems, trials have been performed to reduce transistor mismatch. For that, Indium, Carbon and Nitrogen are (co-)implanted. The element uppon which the current literature has devoted most of its attention is the Carbon. This is not the case for Indium, as its use is less commonly documented in current literature.

Indium: The study of Indium as dopant in silicon gained increasing interest due to the shallow and steep doping profiles which can be obtained by implantation because of its heavy mass of Indium ions [Scalese 03]. Indium has been introduced as a Vt adjust implant on NMOS transistors in order to better control short channel effects. Its diffusion coefficient and activation rate are lower than Boron, as Indium is a heavier element. Its lower diffusion can lead to retrograde channels type, where the active doping is lower at the surface than in the Silicon. When implanted, it turns the Silicon amorphous, even at low concentrations ($10^{-13}cm^{-2}$), as it is implanted with a tilt of 30°. Current research points out that Indium might play a role in the transistor mid-gap and band-gap, but it is difficult to measure. The use of Indium is, however, problematic because of the very low achievable electrical activation [Jones 98]. The

poor electrical activation can be improved by Carbon co-implantation [Baron 79] [Jones 81], as was observed by sheet resistivity and Hall effect measurement by [Boudinov 99] [Gennaro 02] [Scalese 03].

Carbon: Carbon is also used as co-implant to reduce the diffusion of Boron and Phosporus. Zechner et al. [Zechner 07] developed a model to simulate Boron-Carbon and Phosphorus-Carbon co-diffusion. Carbon atoms act as efficient interstitial traps that delay Phosporus and Boron diffusion. A similar effect is also observed in the case of Si preamorphizing implantation. When Carbon is present, the diffusion of Boron is strongly reduced and no further Boron clustering is observed [Marino 06]. The diffusion of Boron is delayed even for the lowest $10^{15} cm^{-2}$ implant dose. It is caused by additional Boron deactivation described by [Pawlak 06]. Transistor variability is also expected to be improved by reducing the diffusion of Boron and Phosporus, and then, reducing random dopants in the channel.

Nitrogen: Nitrogen implant has been used to obtain thinner and more uniform oxides [Dokumaci 01]. Nitrogen co-implants also help to reduce Boron penetration in gate oxides [Liu 97]. This might be due to the suppression of Boron diffusion in poly in the presence of Nitrogen [Nakayama 97]. High amount of Nitrogen in Silicon can adversely affect the carrier mobility in the channel [Dokumaci 01]. Villanueva et al. [Villanueva 06] have shown that a 15% gain can be achived on the I_{on}/I_{off} performance trade-off by adding Nitrogen as co-implant species to standard BF_2 pockets. In the boron-implanted samples, the structural order of the silicon lattice remains damaged by the high-dose implantation. The high dose of N+C co-implantation in Silicon helps considerably in this damage recovery [Barbadillo 03].

III.2.2 Experimental results

The mismatch of different electrical parameters (threshold voltage, gain factor and drain current) will be experimentally analyzed for the various splits with co-implants.

III.2.2.a Effect on threshold voltage mismatch

Before analyzing the effect of co-implants on threshold voltage mismatch, the intrinsic Vt is observed. Figure III.13 shows Vt as a function of the gate length. Comparing with the reference, there are no difference for long lengths. However, at short lengths, there is an important difference of ∼100mV. In this case, the Vt behavior of the splits with Indium are almost flat, while the reference presents reverse short channel effect (RSCE)[1]. These results show that pockets with co-implants are more efficient, with a better control of short channel effects.

Considering all the transistor lengths, an improvement of matching using Indium is clearly observed, as shown in figure III.14.

When Indium is included, $A_{\Delta Vt}$ is reduced to $4.0 mV.\mu m$. If Indium is combined with another material, "$BF_2 + In + C''$, "$BF_2 + In + N''$ or "$BF_2 + In + C + N''$, similar $A_{\Delta Vt}$ is found and $A_{\Delta Vt}$ value is reduced considerably ($\sim 3.5 mV.\mu m$). These splits differ almost $1.0 mV.\mu m$ ($\sim 22\%$) from the reference ($A_{\Delta Vt,ref} \simeq 4.4 mV.\mu m$).

The $A_{\Delta Vt}$ mismatch is analyzed for different length ranges: for devices shorter than $0.1\mu m$ and for those longer than $0.1\mu m$. Considering only the short transistors, an important difference

[1]RSCE: at short channel lengths the halo doping of the source overlaps that of the drain, increasing the average channel doping concentration, and thus increasing the threshold voltage.

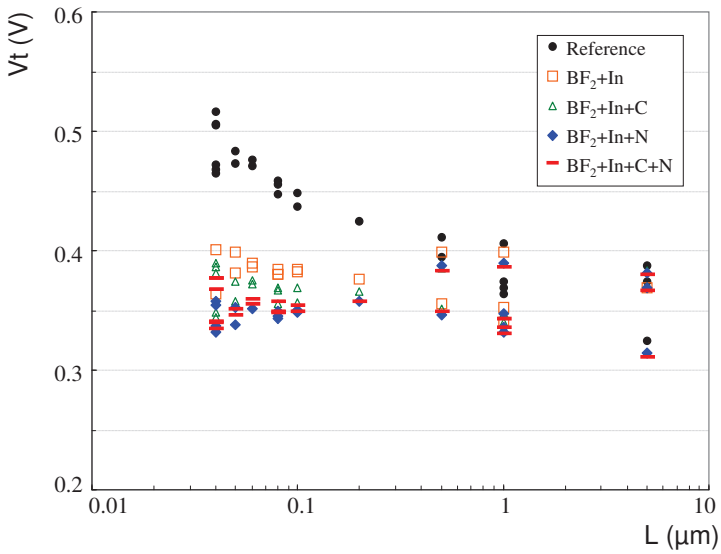
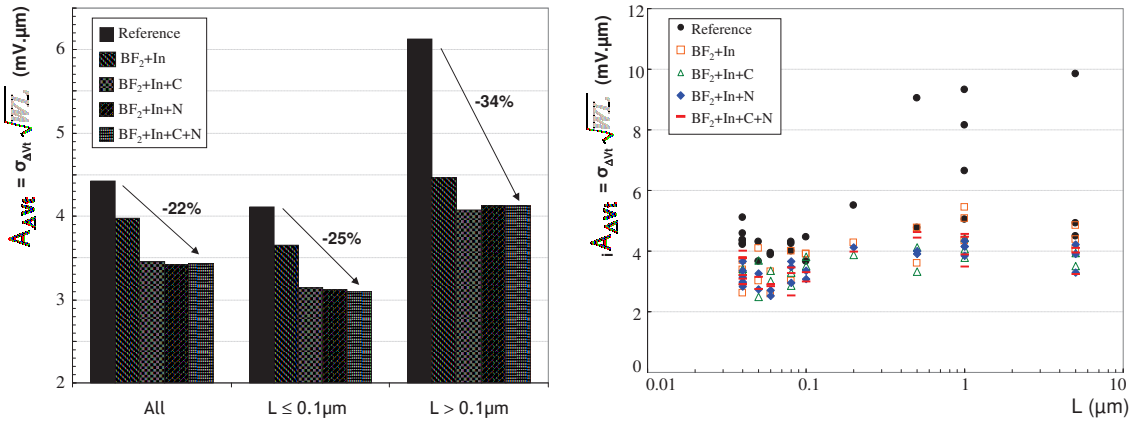


Figure III.13: *Theshold voltage as a function of the gate length for splits with co-implants.*



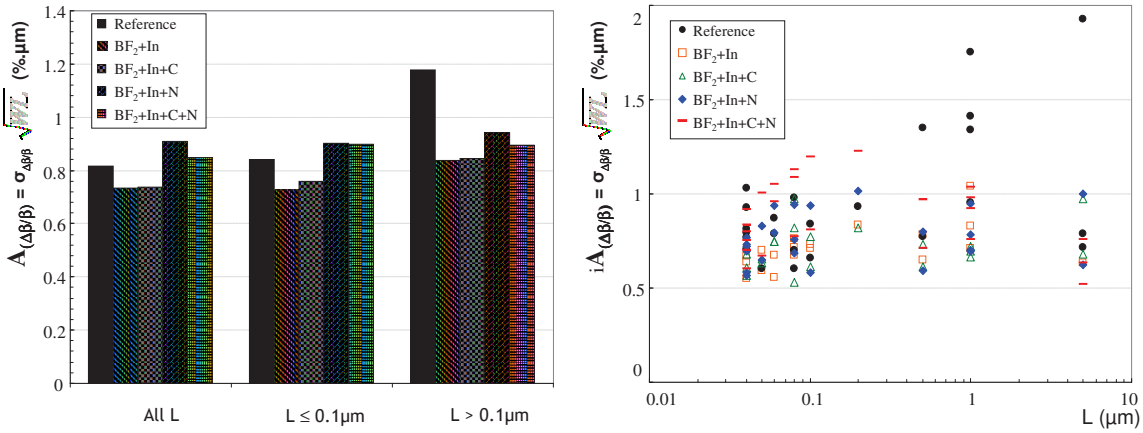
(a) (b)

Figure III.14: *Theshold voltage mismatch as a function of the gate length for the splits under discussion. (a) $A_{\Delta Vt}$ values considering all geometries (left), short transistors (middle) and long transistors (right) and (b) the individual $A_{\Delta Vt}$.*

in the mismatch is observed. By simply doping only with Indium, $A_{\Delta Vt}$ falls to $3.5mV.\mu m$. If other materials are included, this value falls down to $3.0mV.\mu m$ while reference has $A_{\Delta Vt}$ value equal to $4.0mV.\mu m$. Surprisingly, for big lengths, $A_{\Delta Vt}$ is extremely reduced on the split with Indium. The difference between the reference and the splits is more than $2.0mV.\mu m$ ($\sim 34\%$). "$BF_2 + In$" has the highest value in comparison with the other co-implants. It is also important to remark that $A_{\Delta Vt}$ of the reference increases by $2.0mV.\mu m$ from short to long transistors. For splits with Indium, this difference is reduced to $1.0mV.\mu m$. Figure III.14(b) shows that with the introduction of co-implants, $iA_{\Delta Vt}$ presents a flat behavior. This means that the $\sigma_{\Delta Vt}$ of these architectures are proportional to $1/\sqrt{WL}$. The impact of pocket on threshold voltage mismatch is thus strongly reduced.

III.2.2.b Effect on gain factor mismatch

Considering all geometries, gain factor mismatch has no significant difference among the splits (figure III.15).



(a) (b)

Figure III.15: *Relative gain factor mismatch as a function of the gate length for the co-implant splits. (a) $A_{\Delta\beta/\beta}$ values considering all geometries (left), short transistors (middle) and long transistors (right) and (b) the individual $A_{\Delta\beta/\beta}$.*

The splits "$BF_2 + In$" and "$BF_2 + In + C$" have $A_{\Delta\beta/\beta}$ slightly smaller than the reference. However, when Nitrogen is added, the $\Delta\beta/\beta$ mismatch is slightly increased. The same behavior is observed for short transistors. However, for long transistors, there is a considerable difference. Reference goes from 0.8 to 1.2%.μm, while in devices with Indium it goes from 0.7 to 0.8%.μm.

III.2.2.c Effect on drain current mismatch

Fluctuations in drain current have been analyzed for the reference and "$BF_2 + In + C$" (figure III.16). For short transistors, there are almost 0.3%.μm of $A_{\Delta I_D/I_D}$ difference between the splits. These differences may be due to threshold voltage differences. If Vt decreases, drain current also decreases, as shown in equation (II.6).

To verify if $\Delta I_D/I_D$ mismatch differences come from Vt differences, the model proposed by Croon [Croon 02a] has been applied. It is given by equation (III.5),

$$\sigma^2_{\Delta I_D/I_D} = \left(\frac{g_m}{I_D}\right)^2 \sigma^2_{\Delta Vt} + \sigma^2_{\Delta\beta/\beta} + 2\left(-\frac{g_m}{I_D}\right)\rho(\Delta Vt, \Delta\beta/\beta)\sigma_{\Delta Vt}\sigma_{\Delta\beta/\beta} \tag{III.5}$$

where $\rho(\Delta Vt, \Delta\beta/\beta)$ is the Vt and β correlation term. The parameters were all experimentally obtained.

First, only the term $(g_m/I_D)^2\sigma^2_{\Delta Vt}$ in previous equation has been considered, hence, the drain-current mismatch depends only on Vt fluctuations (figure III.17(a)). Then, the complete model is used, including the gain factor and the correlation term (figure III.17(b)).

The reference and "$BF_2 + In + C$" differences are larger when considering only Vt fluctuations. These discrepancies are reduced when β mismatch is considered, but differences still

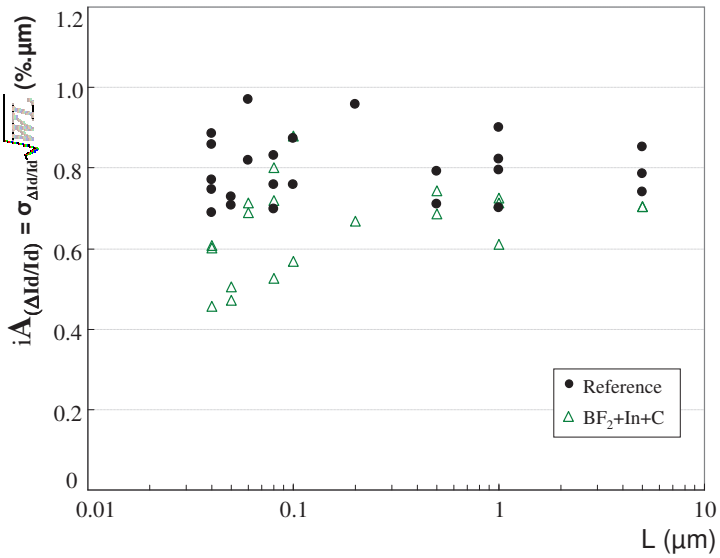
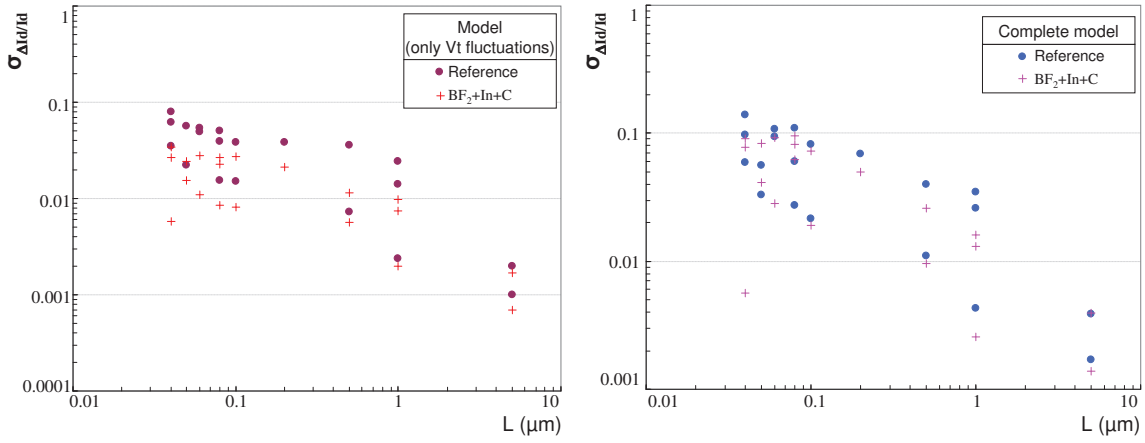


Figure III.16: *Relative drain current mismatch.*



(a) (b)

Figure III.17: *Modeled drain current mismatch for the reference and "$BF_2 + In + C$" split considering (a) only Vt fluctuations and (b) Vt + β fluctuations.*

remain between the splits. These leads to the conclusion that the differences observed in the experimental drain-current fluctuations are explained by threshold voltage and gain factor fluctuations.

To investigate if the differences between the splits on drain-current mismatch is really due to the co-implanted materials' properties or to the Vt differences, the $A_{\Delta I_D/I_D}$ is experimentally investigated at $V_{GS} - Vt$ (figure III.18).

Comparing the drain-current mismatch at $V_{GS} = Vt$, differences are still observed between reference and co-implanted splits. These validate that an improvement of mismatch is obtained with co-implants introduction. A possible explanation for that is the presence of random dopants in the channel, which is analyzed in following section.

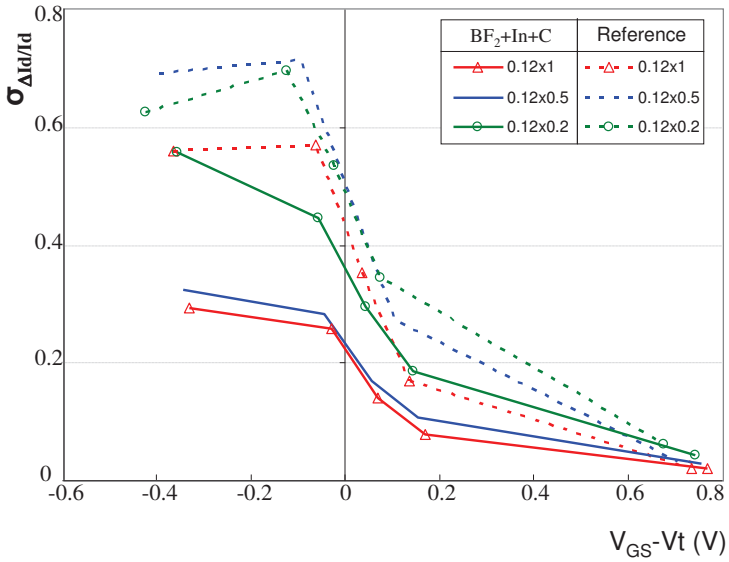


Figure III.18: *Drain-current fluctuations as a function of $V_{GS} - Vt$ for the reference and $BF_2 + In + C$ split.*

III.2.3 Discussion of random dopant fluctuations on splits with co-implants

To verify and understand why devices with Indium have less mismatch, a comparison of random dopant effects between experimental results and the theory are performed. Indeed, random dopants are known as the major source of fluctuations for 45nm technology node [Cathignol 08c]. This technology present pocket-implanted regions. As pocket regions are in the active area, an hypothesis is made: during pocket doping process some impurities diffuse into the channel. These random dopant fluctuations due to pocket implants could have strong impact in transistor mismatch. With the introduction of co-implants, the diffusion of the dopants in the channel may be reduced.

As fluctuations are well-controlled for short transistors, and these have uniform channels, only short transistors have been analyzed to observe the impact of random dopant fluctuations on mismatch for the different splits.

To compare the experimental results with the theory, dopants profiles are extracted by Synopsys TCAD for the devices presented in table III.2. Since at small geometries the channel is considered uniform, a cut on the first dimension is done (figure III.19).

Table III.2: *Split sheet.*

Implant type	Dose/Energy variation
BF_2 (reference)	-
BF_2 + In	High Medium Low
BF_2 + In + C	-

Once net doping concentration is extracted (figure III.20(a)), the $A_{\Delta Vt}$ has been modeled

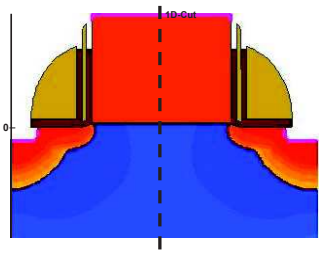
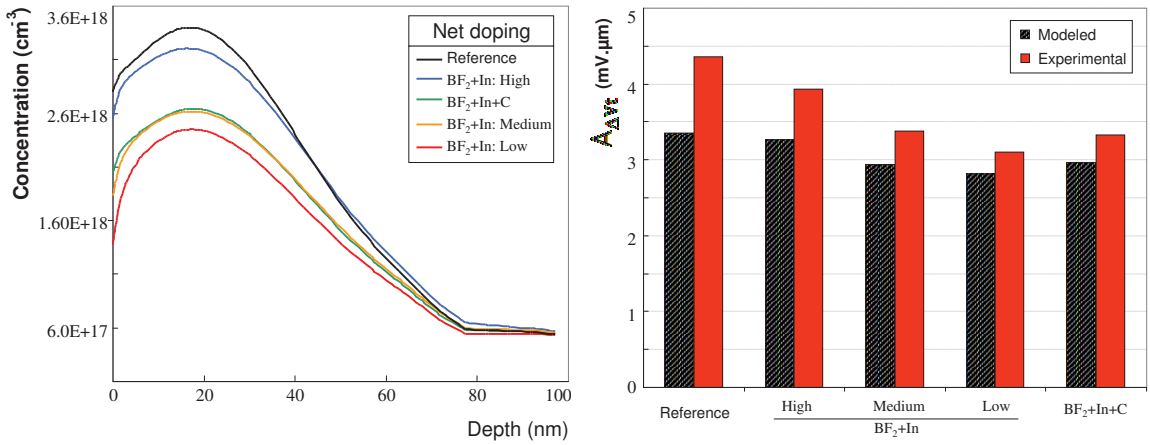


Figure III.19: *Cross section view of a transistor provided by TCAD showing a cut in the first dimension (1D-cut).*

using equation (III.6) [Takeuchi 97].

$$\sigma^2_{\Delta Vt} = \frac{2q^2 t^2_{ox}}{WL\epsilon^2_{ox}} \int_0^{W_m} \left(1 - \frac{y}{W_m}\right)^2 Na(y)dy \tag{III.6}$$



(a) (b)

Figure III.20: *(a)Net doping concentration for L=40nm obtained from TCAD and (b) the $A_{\Delta Vt}$ comparison between modeled and experimental results.*

The comparison of modeled and experimental results is represented in figure III.20(b). Differences can be observed between modeled and experimental results. The $A_{\Delta Vt}$ is calculated considering only random dopant fluctuations. The remaining differences should be due to other sources of fluctuations, such as polysilicon granularity, LER, etc. Thus, it is not surprising that modeled results underestimate the experimental ones. However, the reference split has the greatest difference between modeled and experimental results, which may be induced by the applied model or other unknown properties of the co-implants.

In figure III.20(a) can be noticed that the reference has the highest doping concentration, differing 33% from implants with Indium and medium dose/energy variation. The $A_{\Delta Vt}$ of the reference is also higher, which is consistent with the doping level. The reduction of the doping level can be explained by co-implant properties. Therefore, the mismatch performances

improvement for splits with Indium are in part explained by the lower doping level in the channel.

It has been shown that pocket implants have strong influence on transistor mismatch. Indeed, the 45nm technology node present a different behavior compared to previous technologies. A new physical model is thus necessary to understand this mismatch behavior.

III.3 Pocket model for 45nm technology node

In order to understand and model the Vt mismatch behavior, it is necessary to first review the existing models for the devices with pocket implants.

Some of the models currently available in the literature are empirical [Zhou 00] [Miura-Mattausch 01]. In addition to those, Ueno et al. [Ueno 02] developed a complex Vt model, where the basic idea is to introduce an average carrier concentration to determine Vt. This model has five additional parameters: the maximum doping concentration of the pocket profile, the penetration length into the channel, and three enhanced short-channel parameters. The sheet carrier concentration is calculated for any Vg, but high accuracy is restricted to the region around threshold condition, which is a drawback for this work, aiming at having a valid model for all gate bias conditions.

Cao et al. [Cao 99] reported that pocket implants bring abnormally large drain-induced threshold voltage shifts and low output resistances to long channel devices. They proposed the first physical model of these effects. The additional barrier near the drain creates more DIBL and less output resistances, which are a serious concern for analog design along with matching performance.

A three-transistor model has been proposed by Rios et al. [Rios 02]. Being a physically compact model, it allows accurate Vt fits for any channel length. It can be approximated by considering a device composed of three transistors in series, with a low threshold voltage center device bounded by two higher threshold voltage devices, corresponding, respectively, to the channel and pocket regions. The pocket-implant has an impact in the weak inversion since the device turn-on characteristics are limited by the available carriers in the higher Vt halo region. With strong halo processes, the proposed model is assumed to be in strong-inversion regime.

A compact model form was developed by [Johnson 08] for improved representation of random dopant fluctuation transitor mismatch. This model considers two sources of variations: one due to well doping and the other one due to halo doping. But this model introduce three parameters wich are found by optimization.

A physical approach was proposed by [Cathignol 08a] [Cathignol 09], which provides an adapted model describing the drain current mismatch as Vt fluctuations through any Vg bias and for long devices. One of the limitations of this model is that it leads to an indefinitely increase of $iA_{\Delta Vt}$ with L. This does not correspond to the behavior observed today, as discussed previously on figure III.10. Another limitation is that it gives only a qualitative representation of the mismatch.

In this context, a new physical mismatch model is proposed here, aiming at solving these issues [Mezzomo 10]. A qualitative representation is obtained and the mismatch behavior is analyzed for different transistor gate lengths and also for different gate biasing conditions. An accurate characterization of the parameters used in the model is also performed. The validation of the new mismatch model is done by comparing it with the experimental results, for NMOS and PMOS devices.

III.3.1 Mismatch Model

The proposed physical mismatch model provides both qualitative and quantitative mismatch representation for all the gate lengths. It is also valid for any gate biasing. It is based on the three-transistor series approach to include local Vt fluctuations. One transistor emulates the channel region (ch), whereas the two others account for the source and drain pockets (pk) (figure III.21). The parameters related to the channel will be noted as P_{ch} and those related to the pocket as P_{pk}.

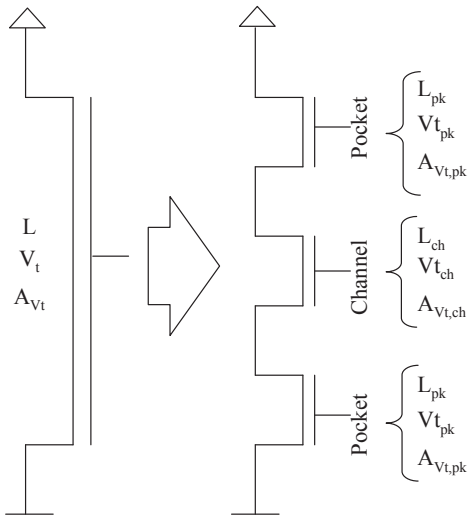


Figure III.21: *Three-transistor model.*

For the sake of analytical derivation, the inversion charge (Qi) is an approximate version of the one in [Ghibaudo 97] valid from weak to strong inversion. Qi is given by equations (III.7) and (III.8) for each transistor,

$$Qi_{pk}(V_{GS}) = C_{ox} n \frac{kT}{q} ln\left(1 + e^{\frac{V_{GS}-Vt_{pk}}{nkT/q}}\right) \tag{III.7}$$

$$Qi_{ch}(V_{GS}) = C_{ox} n \frac{kT}{q} ln\left(1 + e^{\frac{V_{GS}-Vt_{ch}}{nkT/q}}\right) \tag{III.8}$$

where:

- C_{ox} is the oxide capacitance,
- n is the sub-threshold slope parameter,
- kT/q is the thermal voltage at 300K,
- V_{GS} is the gate voltage,
- Vt_{pk} corresponds to the threshold voltage for a transistor whose channel is homogeneous and highly doped (Na_{pk}) and
- Vt_{ch} is the threshold voltage considering only the channel doping (Na_{ch}).

The channel and pocket resistances (R_{ch} and R_{pk}) are calculated by equations (III.9) and (III.10),

$$R_{pk}(V_{GS}) = \left(\frac{W}{L_{pk}} \mu Qi_{pk}(V_{GS})\right)^{-1} \tag{III.9}$$

$$R_{ch}(V_{GS}) = \left(\frac{W}{L_{ch}}\mu Qi_{ch}(V_{GS})\right)^{-1} \tag{III.10}$$

where W is the gate width, L_{ch} is the channel length, L_{pk} is the pocket length and μ is the mobility. Thus, the total resistance (R_{tot}) is obtained, which consists in the sum of the channel and the pocket resistances (equation (III.11)).

$$R_{tot}(V_{GS}) = R_{ch}(V_{GS}) + 2R_{pk}(V_{GS}) \tag{III.11}$$

The drain current (I_D) can be obtained from equation (III.12), where V_{DS} is the drain voltage.

$$I_D = \frac{V_{DS}}{R_{tot}(V_{GS})} \tag{III.12}$$

The variation in the total resistance due to the Vt fluctuations in each region can be obtained from equation (III.13).

$$\delta R_{tot} = \delta R_{ch} + 2\delta R_{pk} = \frac{\partial R_{ch}}{\partial V_t} dVt_{ch} + 2\frac{\partial R_{pk}}{\partial V_t} dVt_{pk} = -\frac{\partial R_{ch}}{\partial V_{GS}} dVt_{ch} - 2\frac{\partial R_{pk}}{\partial V_{GS}} dVt_{pk} \tag{III.13}$$

Since the fluctuations of each transistor are statistically independent, the variance of the total resistance is, therefore, the sum of the variance of each region,

$$\sigma^2_{R_{tot}} = \left(\frac{\partial R_{ch}}{\partial V_{GS}}\right)^2 \sigma^2_{Vt_{ch}} + 2\left(\frac{\partial R_{pk}}{\partial V_{GS}}\right)^2 \sigma^2_{Vt_{pk}} \tag{III.14}$$

The standard deviation of the total resistance can finally be expressed as,

$$\sigma^2_{R_{tot}} = \sqrt{\left(\frac{\partial R_{ch}}{\partial V_{GS}}\right)^2 \frac{A^2_{ch}}{WL_{ch}} + 2\left(\frac{\partial R_{pk}}{\partial V_{GS}}\right)^2 \frac{A^2_{pk}}{WL_{pk}}} \tag{III.15}$$

As a result, the normalized drain current standard deviation is,

$$\frac{\sigma_{I_D}}{I_D}(V_{GS}) = \frac{\sigma R_{tot}}{R_{tot}}(V_{GS}) \tag{III.16}$$

The constant current threshold voltage[2] standard deviation [Cathignol 09] can be defined as,

$$\sigma_{\Delta Vtcc}(V_{GS}) = \frac{\frac{\sigma_{I_D}}{I_D}(V_{GS})}{g_m/I_D} \tag{III.17}$$

The associated Pelgrom′s parameter for the whole transistor can then be deduced from equation (III.17) by multiplying by the square root of the total transistor surface,

$$A_{\Delta Vtcc}(V_{GS}) = \sigma_{\Delta Vtcc}(V_{GS})\sqrt{W(L_{ch} + 2L_{pk})} \tag{III.18}$$

yielding:

$$A_{\Delta Vtcc}(V_{GS}) = \sqrt{\left(\frac{\partial R_{ch}}{\partial V_{GS}} / \frac{\partial R_{tot}}{\partial V_{GS}}\right)^2 \frac{A^2_{ch}L}{L - 2L_{pk}} + 2\left(\frac{\partial R_{pk}}{\partial V_{GS}} / \frac{\partial R_{tot}}{\partial V_{GS}}\right)^2 \frac{A^2_{pk}L}{L_{pk}}} \tag{III.19}$$

The proposed model will be qualitatively analyzed, followed by a comparison with the experimental results. Finally, the influence of the physical parameters of the model on the Vt mismatch is explored.

[2]This method is described in §II.6.2.a

III.3.2 Qualitative results

In this section, the qualitative mismatch behavior resulting from the proposed model will be studied for NMOS transistors. The mismatch behavior is first analyzed in terms of gate length, then of gate bias conditions, followed by a study of their simultaneous variations.

The parameter values are represented in table III.3 and are explained in depth in the section §III.3.3.

Table III.3: *Parameters characterized with the corresponding method applied and the respective values.*

Parameter	Method	Value	Unit
μ_0	C-V	370	cm^2/Vs
T_{ox}	C-V	1.7	nm
n	Empiric	1.45	
L_{pk}	TCAD	20	nm
Na_{ch}	TCAD	7.2E+17	cm^{-3}
Na_{pk}	TCAD	3.0E+18	cm^{-3}
Vt_{ch}	Extrapolation	0.35	V
Vt_{pk}	Extrapolation	0.51	V
$A_{\Delta Vt_{ch}}$	[Takeuchi 97]	1.01	mV.μm
$A_{\Delta Vt_{pk}}$	[Asenov 99]	2.02	mV.μm

III.3.2.a Gate length analysis

The proposed model is first analyzed for the case of a transistor without pocket implants. For that, the pocket regions have the same doping concentration as the channel region. Hence, $Na_{pk} = Na_{ch}$, $Vt_{pk} = Vt_{ch}$ and $A_{pk} = A_{ch}$. The three transistors used in the model are then similar. The modeled normalized mismatch as a function of the gate length follows the scaling law, which confirms the results shown in the introduction of this chapter.

Considering a device with pocket implants, figure III.22 presents the $iA_{\Delta Vtcc}(Vg)$ (left axis) and the $2R_{pk}/R_{tot}$ resistance relation (right axis) evolution with the gate length for a fixed $V_{GS} = 0.4V$.

It is possible to remark that for L<0.1μm, $2R_{pk}/R_{tot} = 1$, i. e., the R_{tot} tends to $2R_{pk}$. Indeed, for L<0.1μm, the pockets are superimposed meaning that they control the total resistance of the transistor. Consequently, the $iA_{\Delta Vtcc}(Vg)$ is equal to pocket stochastic mismatch value A_{pk} for L=L_{min}=2L_{pk}=40nm.

As the gate length increases, the $iA_{\Delta Vtcc}(Vg)$ parameter has a similar pattern at first, but then decreases, tending to the channel stochastic mismatch value A_{ch}. As L increases, R_{pk} remains constant, while the relation $2R_{pk}/R_{tot}$ decreases. Indeed, for relatively long transistors, L>0.1μm, the pockets separate themselves from each other, creating a non-homogeneous channel (pockets doping area + channel doping area), but the weight of pocket resistances are still dominant and the $\sigma_{\Delta Vtcc}$ keeps constant, making the $iA_{\Delta Vtcc}(Vg)$ increases. The $iA_{\Delta Vtcc}(Vg)$ decreases when the weight of channel resistance becomes more significant. The length corresponding to $iA_{\Delta Vtcc}(Vg)$ when it reaches the highest value is called the critical length ($L_{critical}$). It will be modeled further in this manuscript (section §III.3.2.c).

Finally, $2R_{pk}/R_{tot}$ ratio tends to zero for a big L, i.e., the R_{tot} is much bigger than $2R_{pk}$, then, the R_{ch} becomes dominant and the R_{tot} tends to the R_{ch} value. In this case, the source

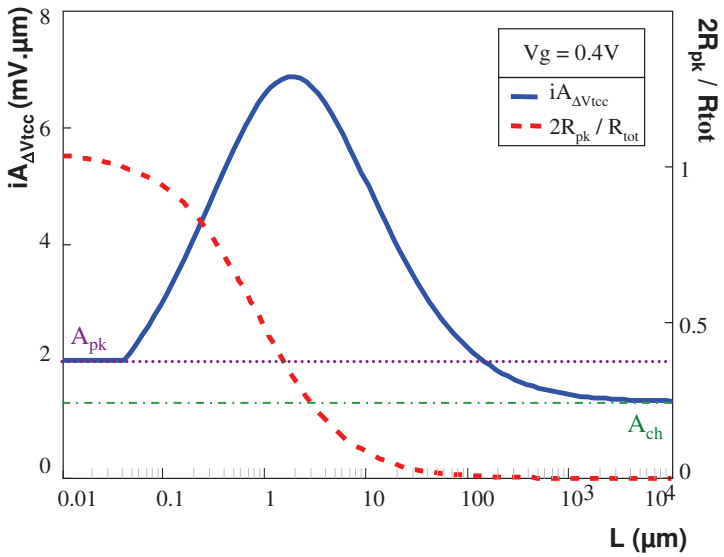


Figure III.22: *The $iA_{\Delta Vtcc}(V_{GS})$ mismatch model and the $2R_{pk}/R_{tot}$ resistance relation for different gate lengths with a $V_{GS} = 0.4V$.*

and drain pockets are outspread, making the channel area much bigger than the pocket area. Here, as the channel area has weak doping, the $iA_{\Delta Vtcc}(Vg)$ decreases, tending to the channel mismatch plateau A_{ch}. It is important to note that the mismatch parameter reaches the A_{ch} plateau for transistor gate lengths which are too long for being observed in 45nm technology test structures (L<100μm).

The A_{pk} and the A_{ch} plateau limits can be recovered with equations (III.15) - (III.18), as shown in equation (III.20) and equation (III.21).

$$\lim_{L_{ch}\to 0}\left(\sigma_{\Delta Vtcc}|_{V_{GS}}\sqrt{W(L_{ch}+2L_{pk})}\right) = A_{pk} \tag{III.20}$$

$$\lim_{L_{ch}\to \infty}\left(\sigma_{\Delta Vtcc}|_{V_{GS}}\sqrt{W(L_{ch}+2L_{pk})}\right) = A_{ch} \tag{III.21}$$

III.3.2.b Gate bias analysis

The next analysis mode for the proposed model is the threshold voltage fluctuations as a function of the gate bias.

The model is applied for a device without pocket implants (figure III.23(dotted line)). For that, pocket and channel regions are considered to have the same doping concentration. In this case, the $iA_{\Delta Vtcc}$ mismatch model is constant along gate bias.

The mismatch is also plotted for devices with pocket implants, considering different gate lengths. Although the shortest transistor (L=0.05μm) has pocket-implants, it is V_{GS}-independent, as a device without pockets, due its homogeneous channel. The fluctuations for medium lengths are strongly increased for weak V_{GS} values. For very long transistors, the V_{GS} dependence is atenuated. To explain these behaviors, the fluctuations in a non-homogeneous device are analyzed.

Considering a device with pocket implants, figure III.24 shows the modeled $iA_{\Delta Vtcc}$ for different V_{GS} values and for a fixed gate length L=1μm.

In this figure is also represented the trend of the relation between the pocket resistance R_{pk} (equation (III.9)) and the total resistance R_{tot} (equation (III.11)). The $iA_{\Delta Vtcc}$ decreases

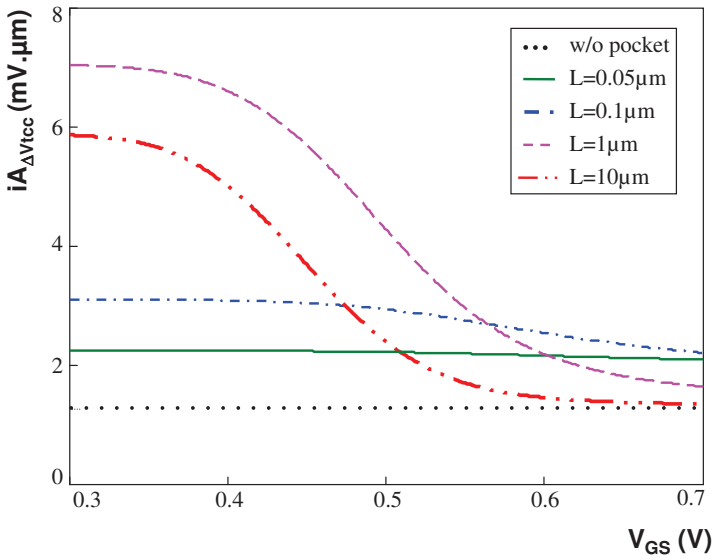


Figure III.23: *The $iA_{\Delta Vtcc}$ mismatch model for different gate bias on NMOS transistor for a device without pocket implants and various devices with pocket-implants, representing short, long and very long transistors.*

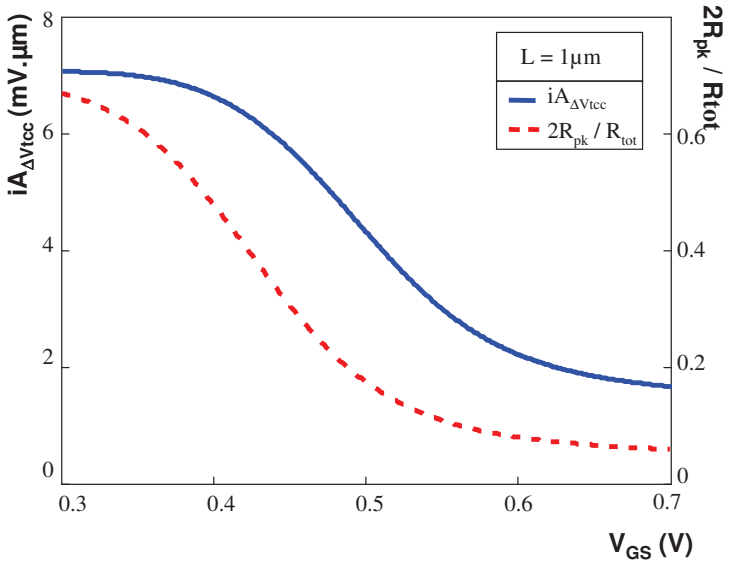


Figure III.24: *The $iA_{\Delta Vtcc}$ mismatch model and the $2R_{pk}/R_{tot}$ resistance relation for different gate bias ($L = 1\ \mu m$).*

when V_{GS} increases in agreement with the results previously obtained by [Cathignol 09]. The $iA_{\Delta Vtcc}(V_{GS})$ behavior can be explained by the $2R_{pk}/R_{tot}$ ratio. For small V_{GS} conditions, the $2R_{pk}/R_{tot}$ ratio tends to 1, because the pocket resistance R_{pk} becomes predominant. For high V_{GS} bias, the channel resistance R_{ch} increases, decreasing the value of $2R_{pk}/R_{tot}$. Thus, the mismatch behavior becomes similar to that of a device without pocket implants.

III.3.2.c Analysis of gate bias and length simultaneous variation

The stochastic mismatch for different gate lengths and for different V_{GS} bias conditions can be seen in figure III.25.

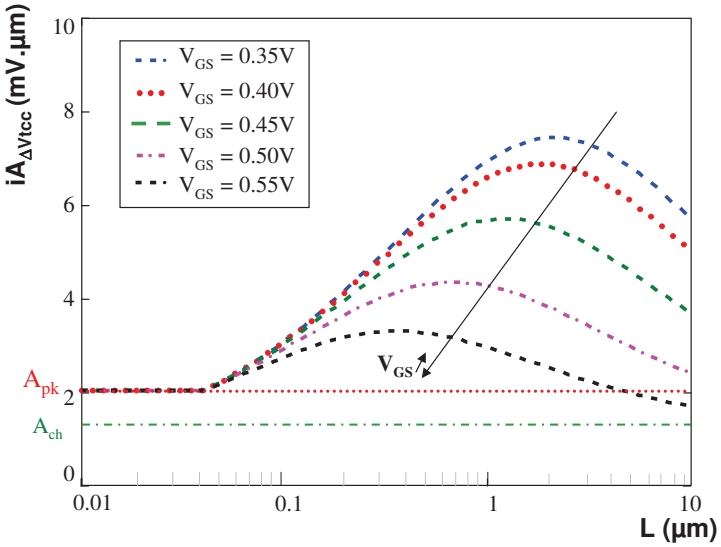


Figure III.25: *The $iA_{\Delta Vtcc}$ mismatch for different gate lengths and different gate bias conditions. A_{pk} and A_{ch} were obtained for $V_{GS} = Vt$.*

The model starts at A_{pk} plateau and tends to A_{ch} plateau, as explained before. As L increases, the $iA_{\Delta Vtcc}$ curves spread according to V_{GS}. This happens when the $2R_{pk}/R_{tot}$ ratio is around 0.5, thus, the $iA_{\Delta Vtcc}$ is V_{GS} dependent. For very long transistors, the $iA_{\Delta Vtcc}$ curves converge to the same value. The convergence is not represented as it is reached for transistors which are too long for being observed in 45nm technology. In this case, the total resistance is related only to R_{ch}, which leads to an $iA_{\Delta Vtcc}(Vg)$ that tends to be equal to A_{ch} (equation III.21), and not V_{GS} dependent. For L<0.1μm, the total resistance is related only to $2R_{pk}$. The $iA_{\Delta Vtcc}$ tends to be equal to A_{pk} (equation III.20), which is also V_{GS} independent.

The critical gate length ($L_{critical}$) is different for each V_{GS} bias condition (figure III.26), i. e., the mismatch worst case corresponds to different gate lengths.

$L_{critical}$ is an important parameter for designers and it can be expressed as the gate length corresponding to the maximum of $A_{\Delta Vtcc}(Vg)$ (equation (III.22)).

$$L_{critical} = L|_{A_{\Delta Vtcc}(Vg)=max} = L|_{\frac{dA_{\Delta Vtcc}(Vg)}{dL}=0} \tag{III.22}$$

Solving equation III.22, yields:

$$L_{critical} = \frac{2L_{pk}\left(A_{pk}^2 d_{pk}^2 - A_{ch}^2 d_{ch}^2\right)(d_{pk} - d_{ch})}{A_{pk}^2 d_{pk}^2 d_{ch} - 2A_{ch}^2 d_{ch}^2 d_{pk} + A_{ch}^2 d_{ch}^3} \tag{III.23}$$

where

$$d_{pk} = \frac{d(1/Qi_{pk})}{dV_{GS}} \tag{III.24}$$

$$d_{ch} = \frac{d(1/Qi_{ch})}{dV_{GS}} \tag{III.25}$$

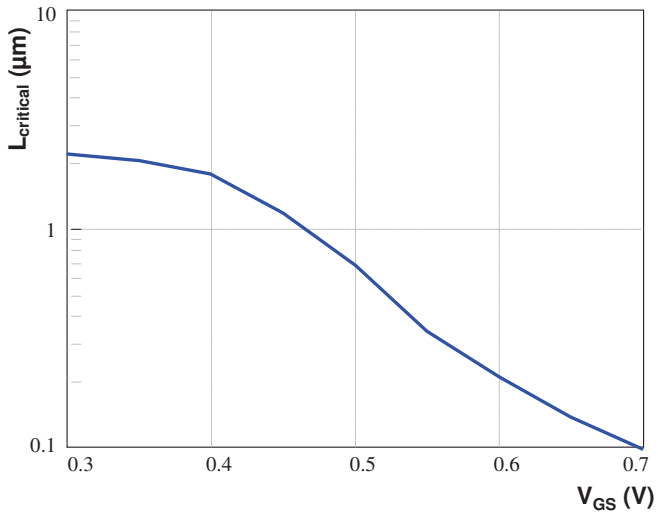


Figure III.26: *$L_{critical}$ for different gate bias extracted numerically.*

Simplifying, $L_{critical}$ can be expressed as equation (III.26).

$$L_{critical} \approx 2L_{pk} \frac{Qi_{ch}^2}{Qi_{pk}^2} \frac{\frac{dQi_{pk}}{dVg}}{\frac{dQi_{ch}}{dVg}} \tag{III.26}$$

yielding:

$$L_{critical} \approx 2L_{pk} \frac{Qi_{ch}^2}{Qi_{pk}^2} \frac{\left(1 + e^{-\frac{V_{GS} - Vt_{pk}}{nkT/q}}\right)}{\left(1 + e^{-\frac{V_{GS} - Vt_{ch}}{nkT/q}}\right)} \tag{III.27}$$

These equations demonstrate that if L_{pk} increases, the critical length also increases (equation III.26). Moreover, $L_{critical}$ depends on the doping concentration of the channel and the pockets zones (equation III.27) through the respective threshold voltages.

Figure III.27 shows $L_{critical}$ as a function of the gate bias for three cases: numerically result (obtained directly from figure III.25), analytical model (equation (III.23)), and the simplified analytical model (equation (III.27)).

The analytical model and the numerical $L_{critical}$ are superimposed. The simplified and analytical model differ only for very high gate bias. Thus, for gate bias around threshold voltages, the simplified analytical model is adapted to represent the $L_{critical}$.

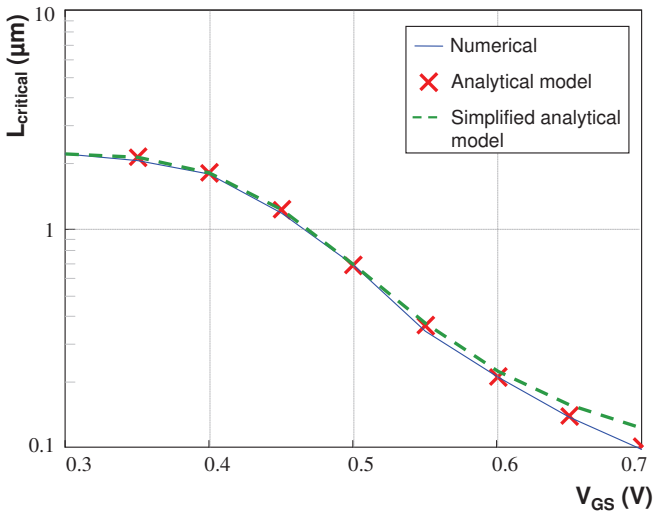


Figure III.27: *$L_{critical}$ for different gate bias.*

III.3.3 Quantitative results

In order to validate the proposed model it will be compared to experimental data. The parameters used in the model are characterized in section §III.3.3.a. Its results will be compared to the data of NMOS in section §III.3.3.b and PMOS in section §III.3.3.c.

III.3.3.a Parameter characterization

To compare the mismatch model with the experimental results, the following parameters are necessary to calibrate the model (figure III.28): pocket gate length (L_{pk}), oxide capacitance (C_{ox}), mobility (μ_0), pocket doping concentration (Na_{pk}), channel doping concentration (Na_{ch}), pocket threshold voltage (Vt_{pk}), channel threshold voltage (Vt_{ch}), pocket stochastic mismatch ($\sigma_{Vt_{pk}}$), channel stochastic mismatch ($\sigma_{Vt_{ch}}$), pocket mismatch parameter ($A_{\Delta Vt_{pk}}$) and channel mismatch parameter ($A_{\Delta Vt_{ch}}$). These last four parameters depend on Vt, which depends on Na.

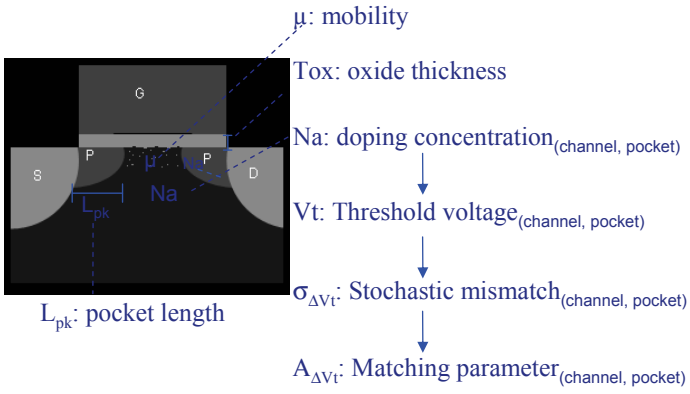


Figure III.28: *Physical parameters used for the mismatch model calibration.*

The method used for extracting each parameter and its value are given in table III.4.

Table III.4: *Parameters characterized with the corresponding method applied and the respective values.*

Parameter	Method	Value	Unit
μ_0	C-V	370	cm^2/Vs
T_{ox}	C-V	1.7	nm
L_{pk}	TCAD	20	nm
n	Empiric	1.45	
	TCAD		
Vt_{ch}	Extrapolation	0.35	V
Vt_{pk}	Extrapolation	0.51	V
Na_{ch}	TCAD	7.2E+17	cm^{-3}
Na_{pk}	TCAD	3.0E+18	cm^{-3}
$A_{\Delta Vt_{ch}}$	[Takeuchi 97]	1.01	mV.μm
$A_{\Delta Vt_{pk[T]}}$	[Takeuchi 97]	1.57	mV.μm
$A_{\Delta Vt_{pk[A]}}$	[Asenov 99]	2.02	mV.μm
	Body factor (γ)		
Vt_{ch}	Body factor (γ)	0.38	V
Vt_{pk}	Body factor (γ)	0.54	V
Na_{ch}	Body factor (γ)	1.5E+18	cm^{-3}
Na_{pk}	Body factor (γ)	2.8E+18	cm^{-3}
$A_{\Delta Vt_{ch}}$	[Takeuchi 97]	1.35	mV.μm
$A_{\Delta Vt_{pk[T]}}$	[Takeuchi 97]	1.58	mV.μm
$A_{\Delta Vt_{pk[A]}}$	[Asenov 99]	1.91	mV.μm

The oxide thickness (T_{ox}) is give by equation (III.28), where ε_{ox} is the permittivity of silicon dioxide, equals to $4 \times 8.84 \times 10^{-14} F/cm$, and C_{ox} the oxide capacitance. The oxide capacitance is obtained from C-V method, where, C_{ox} is taken at the maximum of gate-bulk capacitance C_{GB}.

$$T_{ox} = \frac{\varepsilon_{ox}}{C_{ox}} \tag{III.28}$$

To obtain the length of pocket regions, Technology Computer Aided Design (TCAD) has been used. It has been calibrated for the same split used for the electrical measurements. A lateral profile of the dopant concentration along the transistor length is obtained (figure III.29). In this figure, it is possible to notice the difference of the doping concentration of channel, pockets, drain and source regions.

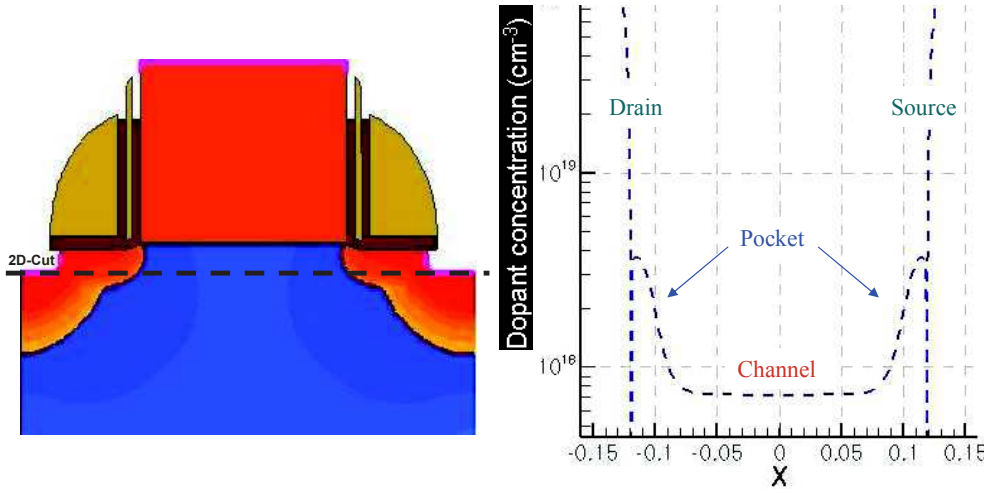
One of the major difficulties during the characterization step is the extraction of the doping concentration. In order to do so, two different methods have been applied: TCAD doping profiles and body factor (γ) .

The doping profile is obtained for a very long and a short transistor using TCAD, as both have quite-homogeneous channel. For that, a 1-D cut has been made and the Na_{ch} and the Na_{pk} are obtained (figure III.30).

The channel depth W_m is calculated by equation (III.29) [Sze 81].

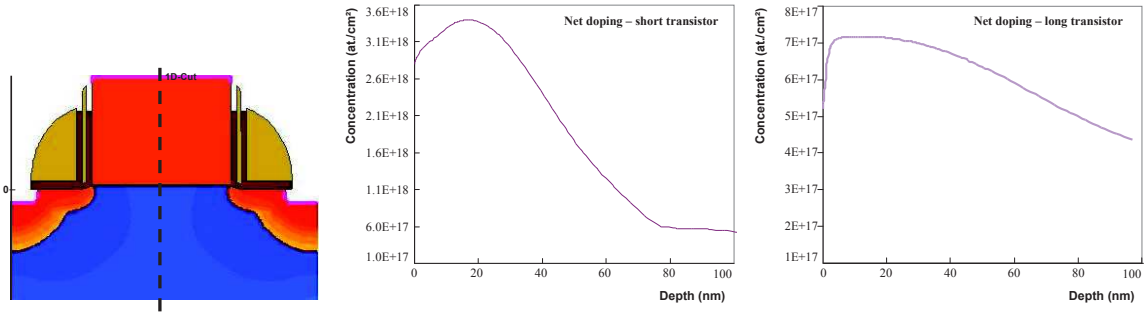
$$W_m \simeq \sqrt{\frac{4\epsilon_{Si} kT ln(Na/n_i)}{q^2 Na}} \tag{III.29}$$

Doping concentration is then obtained by the weighted average of Na, integrating the dopant



(a) Profile cut (b) Dopant profiles

Figure III.29: *Dopant profiles along the channel provided by TCAD making a cut in the second dimension.*



(a) Profile cut (b) Short transistor (c) Long transistor

Figure III.30: *Dopant profiles provided by TCAD using (a)1D-cut for (b) short and (c)long transistors.*

profile along the channel (equation (III.30)).

$$N_{eff} = 3\int_0^{W_m}\left(1-\frac{y}{W_m}\right)^2 Na(y)\frac{dy}{W_m} \tag{III.30}$$

Channel and pocket doping concentration are also obtained by the body factor method, using equation (II.5).

Channel and pocket threshold voltage are extracted by extrapolation (showed in first chapter § II.6.1) and body factor (γ), using equation (II.4), with similar results. Threshold voltage extracted by the extrapolation method is used to calibrate the proposed mismatch pocket model.

In order to calculate the mismatch parameter ($A_{\Delta Vt_{ch}}$ and $A_{\Delta Vt_{pk}}$), two models have been used: the one proposed by [Takeuchi 97], where the mismatch is $Na^{0.25}$ dependent (equation

(III.31) [3]) and the one proposed by [Asenov 99], where, for small geometries (smaller than 0.1μm) the mismatch is $Na^{0.40}$ dependent (equation (III.32)).

$$\sigma^2_{\Delta Vt} = \frac{2q^2 t^2_{ox}}{WL\epsilon^2_{ox}} \int_0^{W_m} \left(1 - \frac{y}{W_m}\right)^2 Na(y)dy \tag{III.31}$$

$$\sigma_{\Delta Vt} = \sqrt{2}\ 3.19\ 10^{-18} \frac{t_{ox} Na^{0.40}}{\sqrt{WL}} \tag{III.32}$$

The value obtained by body factor method is more significant for the channel doping concentration (Na_{ch}). Consequently, the $A_{\Delta Vt_{ch}}$ has higher value. Thus, it has been ruled out and the comparison is done only using the results provided by TCAD method.

The $A_{\Delta Vtcc}(Vg)$ calculated before is associated with the random doping as a source of fluctuations. Even if this is a major contribution in modern technological nodes, other sources of fluctuations, mainly polysilicon granularity and line edge roughness, are present as well. Therefore, it is necessary to calculate the total mismatch fluctuations A_{total} (equation (III.33)).

$$A_{total} = \sqrt{A^2_{other\_contributions} + A^2_{doping}} \tag{III.33}$$

For this, the mismatch due to other contributions ($A^2_{other\_contributions}$) is obtained through the difference between the square mismatch of the experimental results and the square mismatch related to the doping. In addition to the known sources of fluctuations (line edge roughness, poly gate granularity) there may be additional unknown sources. Then, in order to avoid making any hypothesis about the scaling, the general case is used, where the mismatch follows the scaling law.

The $A_{\Delta Vtcc}(Vg)$ was calculated for L<0.1μm as the mismatch extraction is well-controlled for these lengths. Thus, the modeled $A_{\Delta Vtcc}(Vg)$ now includes all sources of fluctuations and is ready to be compared to the experimental results. The A_{total} , the A_{doping} and the $A_{other\_contributions}$ are represented in figure III.31. It can be noticed that for the minimal gate length, the contribution of the doping fluctuations is lower than the contribution of other fluctuation sources.

This result is slightly surprising since random discrete dopants are the major contribution for this 45nm MOSFET, as shown by the atomistic simulations, calibrated on this 45nm technology, performed by [Cathignol 08b]. Despite its high value, the effect of these contributions is still far lower than the long devices pocket induced effect that is discussed in this chapter. Therefore, it does not affect the validity of this study.

III.3.3.b Experimental results for NMOS transistors

Before comparing the model and the experimental mismatch results, the $I_D - V_{GS}$ characteristic must be checked. Figure III.32 shows the modeled and the experimental $I_D - V_{GS}$ after model parameter adjustment.

Figure III.33 shows the mismatch results for several gate lengths and several V_{GS} bias conditions.

It shows the onset of the hump and the A_{pk} and the A_{ch} plateau tendencies for both model and experimental results. The experimental $L_{critical}$ seems to be smaller than that in the model. This slight difference can be explained by some of the hypothesis made in this work. The

[3] This equation was presented in previous section §III.2, equation (III.6). For a better clearance of the text, that same equation has been copied here.

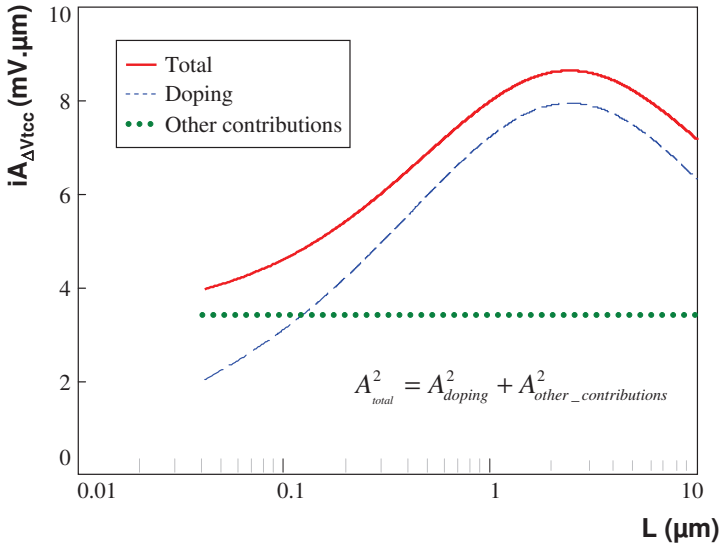


Figure III.31: *Matching for different sources of fluctuation: the dashed line represents the dopant fluctuations, the dotted line represents other sources of fluctuations and the entire line is the total mismatch.*

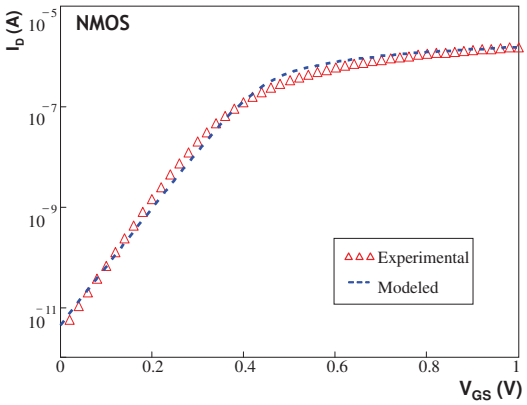


Figure III.32: *$I_D - V_{GS}$ comparison between the model and the experimental results for L=1μm.*

proposed model is based on the three-transistor series approach. Therefore, the transition from heavily-doped (pocket) to weakly-doped (channel) region is abrupt, while in the reality it is smooth. Thus, some of the parameters used to estimate the $L_{critical}$, as the L_{pk}, can have a non-exact value. Nevertheless, to experimentally determine which is the critical length, more measurements with different transistor geometries would be needed.

Figure III.33 also shows some disagreement between the model and the theory, where the model underestimates the experimental results for long transistors. One of the reasons for these differences is because the methods used to characterize the physical parameters, such as mobility, are quite complex for this technology node. Then, since a simplified model is used, the results can be slightly different from reality. Also, the $A_{other\_contributions}$ is considered scaled in surface, to avoid making hypothesis about the scaling of these sources of fluctuations. Although the mismatch for long transistors is not perfect, the model follows the mismatch experimental behavior for different V_{GS}: the curves are superimposed for small gate lengths and as gate length

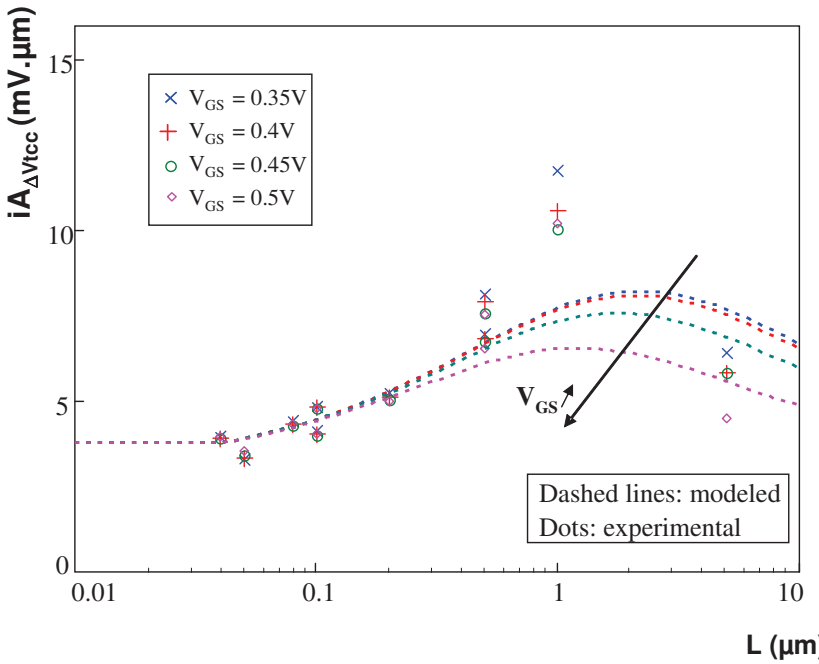


Figure III.33: *Matching comparison between the new physical mismatch model and the experimental results.*

increases, they spread away from each other.

NMOS transistors have been the focus of this study as they have strong mismatch, especially for long transistors. But PMOS transistors have also been modelled. In the next section, the pocket model is then applied for PMOS transistors. Following, the influence of the physical parameters on the mismatch for NMOS and PMOS devices are discussed.

III.3.3.c Pocket model for PMOS transistors

The proposed model is now applied for PMOS transistors. The value of each parameter and its associated method are summarized in table III.5.

Table III.5: *Parameters characterized with the corresponding method applied and the respective values for PMOS transistors.*

Parameter	Method	Value	Unit
μ_0	C-V	70	cm^2/Vs
T_{ox}	C-V	1.7	nm
L_{pk}	TCAD	20	nm
n	Empiric	-1.45	
Vt_{ch}	Extrapolation	-0.43	V
Vt_{pk}	Extrapolation	-0.50	V
Na_{ch}	TCAD	2.8E+17	cm^{-3}
Na_{pk}	TCAD	1.5E+18	cm^{-3}
$A_{\Delta Vt_{ch}}$	[Takeuchi 97]	0.7	mV.μm
$A_{\Delta Vt_{pk}}$	[Takeuchi 97]	1.68	mV.μm
$A_{\Delta Vt_{pk}}$	[Asenov 99]	1.47	mV.μm

The $I_D - V_{GS}$ characteristics for a PMOS transistor with gate lenght equals to $1\mu m$ is shown in figure III.34, where experimental and modeled results are represented. As can be seen, the model fits experimental results.

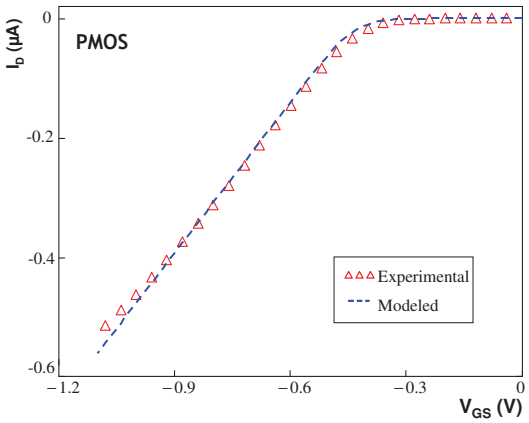


Figure III.34: *$I_D - V_{GS}$ comparison between modeled and experimental results for L=1μm.*

A comparison between the new physical mismatch model and experimental results for $V_{GS} = Vt$ is shown in figure III.35. It can be noticed that the proposed model is also adapted for PMOS transistors. It should be highlighted that N and PMOS devices present different level of mismatch. The level of mismatch is smaller for PMOS transistors. Moreover, the hump observed for long pMOSFET is also attenuated.

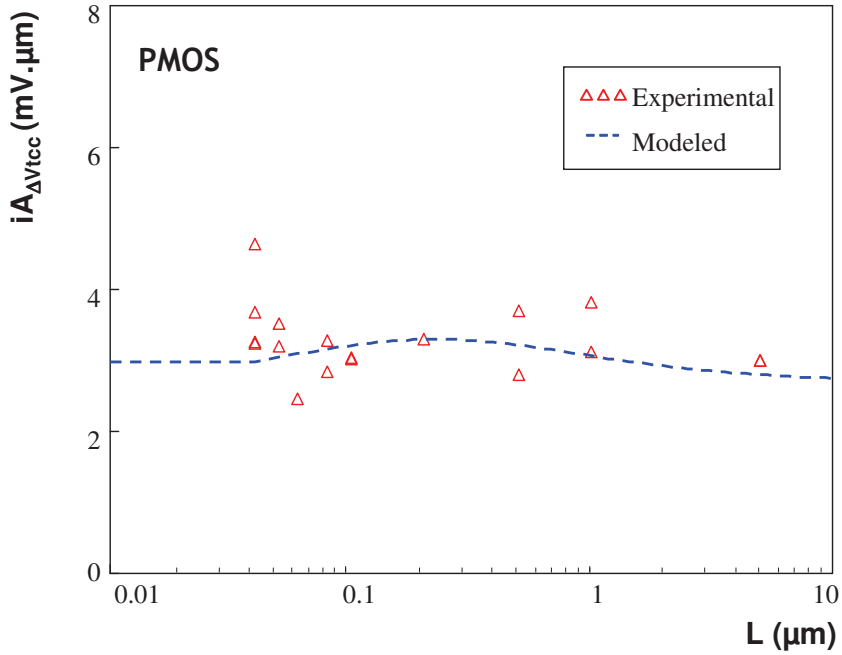


Figure III.35: *Matching comparison between the new physical mismatch model and the experimental results for $V_{GS} = Vt$ on PMOS transistor.*

To understand why NMOS and PMOS have different levels of fluctuations, a discussion about the influence of physical parameters on mismatch will be performed in the next section.

III.3.4 The influence of physical parameters on mismatch for NMOS and PMOS devices

A mismatch model have been proposed in previous section. It is valid from weak to strong inversion region, for both N and PMOS devices. Another application of this model is the possibility to analyze the influence of each physical parameter on the mismatch.

A physical parameter of interest is the dopant concentration (Na). In the case of transistors with pockets, where pocket and channel regions present different dopant concentration, the presence of a non-homogeneous channel has a direct impact on the mismatch. Indeed, both mismatch parameter A_{Vt} and threshold voltage Vt are a function of Na. In addition, Na is not the only factor which can influence the Vt and the A_{Vt}.

The objective of this section is to decorrelate the impact of Vt and A_{Vt} parameters on mismatch. In this 45nm technology, both Vt and A_{Vt} depends on Na. However, the Vt and A_{Vt} correlation may not happen in other technologies. For example, for technologies with high-k metal gates, the edge roughness fluctuations may impact the Vt but not the A_{Vt}. For these reasons Vt and A_{Vt} are analyzed independently of the Na variations.

The proposed model is then used to analyze the influence on the mismatch of each one of these physical parameters: Na, Vt and A_{Vt}. Different conditions for Na, Vt and A_{Vt} parameters are applied III.6. First the impact of the Vt and the A_{Vt} are analyzed separately. This provides the analysis of each parameter independently from the variation in the dopant concentration. Then, Na will be subject to different conditions, which imply in Vt and A_{Vt} variations.

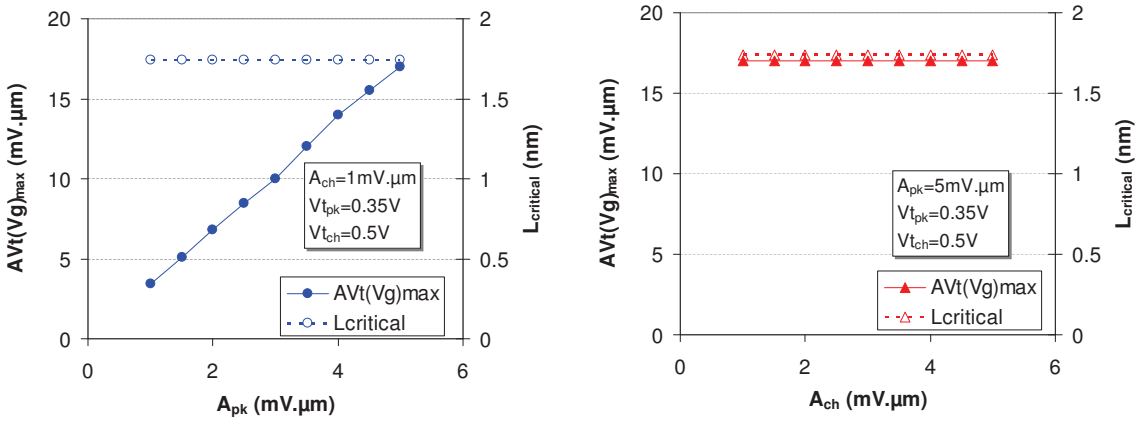
Table III.6: *Conditions to analyze the impact of different parameters on mismatch. In first and second case, Vt and A_{Vt} are varied independently of the Na, even this does not correspond to the real case in 45nm technology. In third case, the real characteristic of the transistors are considered, where a variation in Na implies in Vt and A_{Vt} variations.*

Case	Na	Vt	A_{Vt}
First case	(-)	Fixed	Varied
Second case	(-)	Varied	Fixed
Third case	Varied	$Vt(Na)$	$A_{Vt}(Na)$

Thus, it will be possible to verify if the dopants have the major influence on the mismatch.

***First case:* the A_{Vt} varies for fixed Vt values.** Threshold voltages is fixed for channel and pocket regions considering $Vt_{pk} = 0.5V$ and $Vt_{ch} = 0.35V$. First, A_{pk} is varied for a fixed $A_{ch} = 1\ mV.\mu m$ (figure III.36 (a)). Then, A_{ch} is varied for a fixed $A_{pk} = 5\ mV.\mu m$ (figure III.36 (b)).

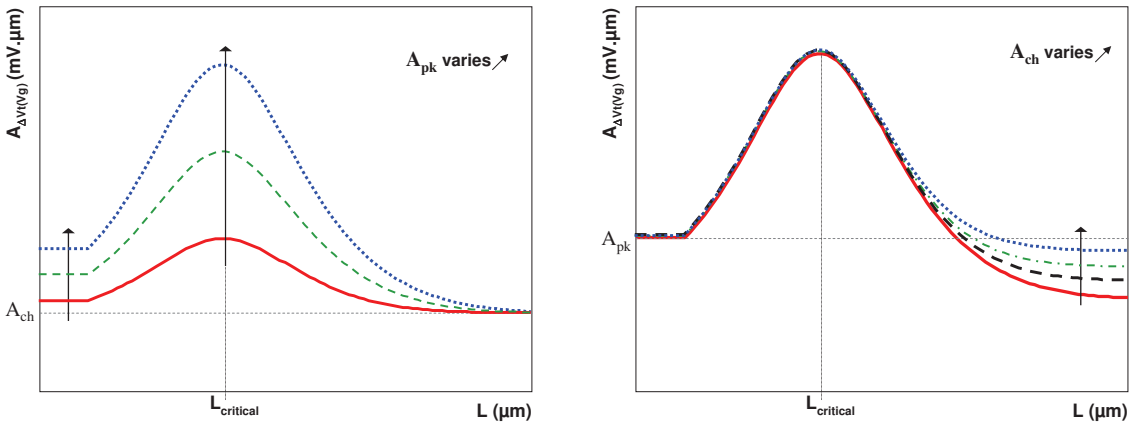
In both cases the $L_{critical}$ does not change. These results agree with equation (III.26), which shows that this parameter does not depend on A_{ch} or A_{pk} for V_{GS} around Vt value. For a fixed A_{ch}, the maximum value of the total mismatch ($A_{\Delta Vt(Vg)max}$) increases linearly with A_{pk}. It is interesting to notice the case when $A_{pk} = A_{ch} = 1\ mV.\mu m$. In that case, the $A_{\Delta Vt(Vg)max}$ is higher than $1\ mV.\mu m$. This happens because Vt_{pk} and Vt_{ch} have different values. For a fixed A_{pk}, the $A_{\Delta Vt(Vg)max}$ remains constant with the increase of A_{ch}, as A_{pk} is predominant. Thus,



(a) (b)

Figure III.36: *The maximum value of the total mismatch ($A_{\Delta Vt(Vg)max}$) and the critical length ($L_{critical}$) numerically obtained for (a) variations in A_{pk} and (b) variations in A_{ch}.*

a variation in the mismatch parameters will change only the fluctuations level, as illustrated in figure (III.37).

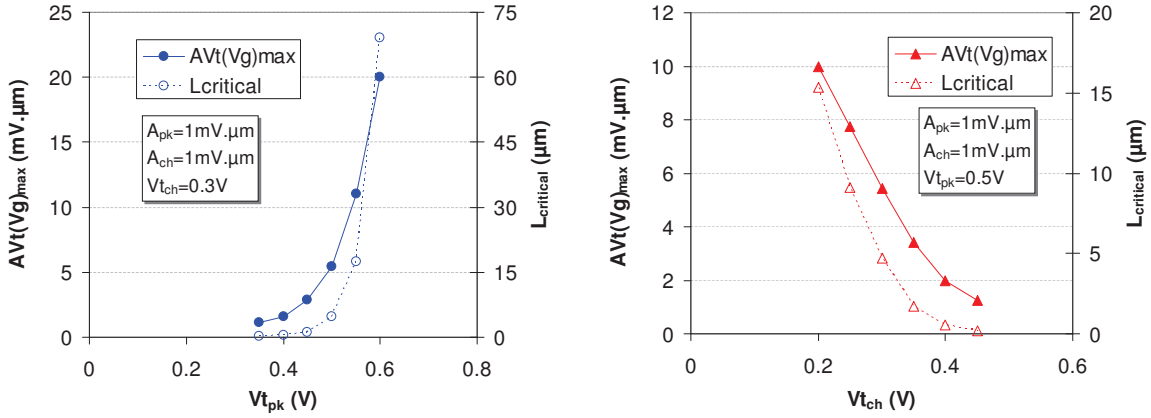


(a) (b)

Figure III.37: *Variations of the fluctuations level for (a) variations in A_{pk} and (b) variations in A_{ch}.*

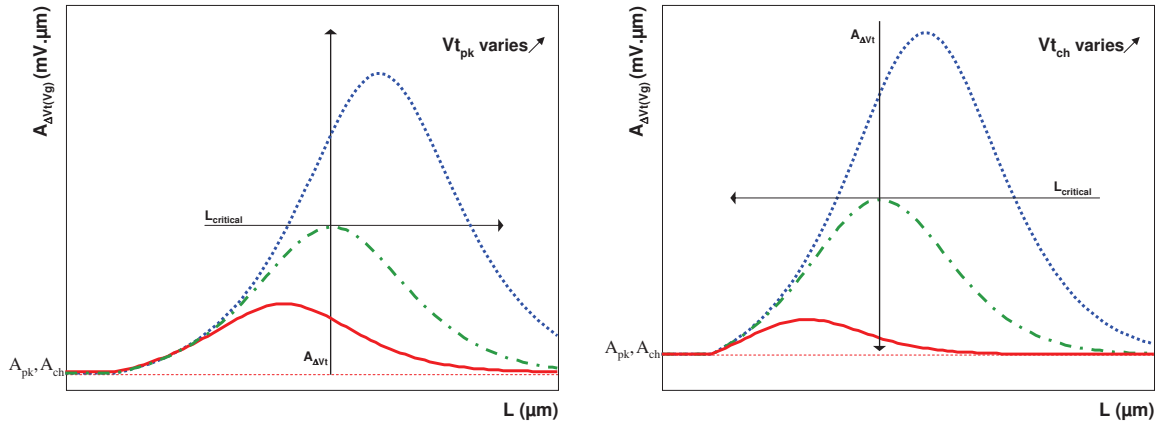
Second case: **the Vt is varied for fixed A_{Vt} values.** Mismatch parameter values are fixed for channel and pocket regions considering $A_{pk} = 1\ mV.\mu m$ and $A_{ch} = 1\ mV.\mu m$. First, Vt_{pk} is varied from 0.35V to 0.6V for a fixed $Vt_{ch} = 0.3V$ (figure III.38(a)). Then, Vt_{ch} is varied from 0.2V to 0.45V for a fixed $Vt_{pk} = 0.5V$ (figure III.38(b)).

As the difference between Vt_{ch} and Vt_{pk} increases, $A_{\Delta Vt(Vg)max}$ and $L_{critical}$ increase exponentially. This leads to the conclusion that a variation in the threshold voltage changes the fluctuations level and the critical length, as ilustrated in figure (III.39).



(a) (b)

Figure III.38: *The maximum value of the total mismatch ($A_{\Delta Vt(Vg)max}$) and the critical length ($L_{critical}$) for (a) variations in Vt_{pk} and (b) variations in Vt_{ch}.*



(a) (b)

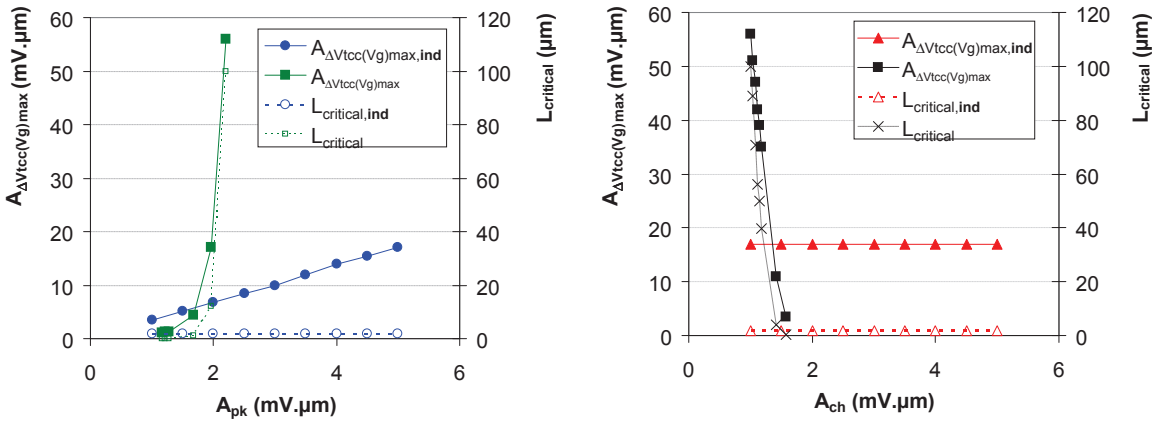
Figure III.39: *Schematic of the critical length and the variations in the fluctuations level for (a) variations in Vt_{pk} and (b) variations in Vt_{ch}.*

***Third case:* the Na varies.** In this case, Vt and A_{Vt} depends on Na accordingly to the usual dependence in 45nm technology. First, Na_{ch} is fixed ($Na_{ch} = 5E + 17cm^{-3}$) and Na_{pk} varies from $8E + 17cm^{-3}$ to $4E + 18cm^{-3}$. Then, the Na_{pk} is fixed ($Na_{pk} = 4E + 18cm^{-3}$) and the Na_{ch} varies from $5E + 17cm^{-3}$ to $3E + 18cm^{-3}$. In both cases, the $A_{\Delta Vt(Vg)max}$ and the $L_{critical}$ change with an increase in Na.

In figure III.40 and III.41 a comparison is made between the previous results, where the parameters vary independently (called here P_{ind}), and the new results, where the parameter Na varies (Vt and A_{Vt} are a function of Na).

Figure III.40(a) and (b) show important disagreements between the $A_{pk,ch,ind}$ and the $A_{pk,ch}(Na)$. An important increase of $A_{\Delta Vt(Vg)max}$ and also of $L_{critical}$ is observed. These disagreements lead to the conclusion that, in addition to the $A_{pk,ch}$, other parameters are strongly varied when there

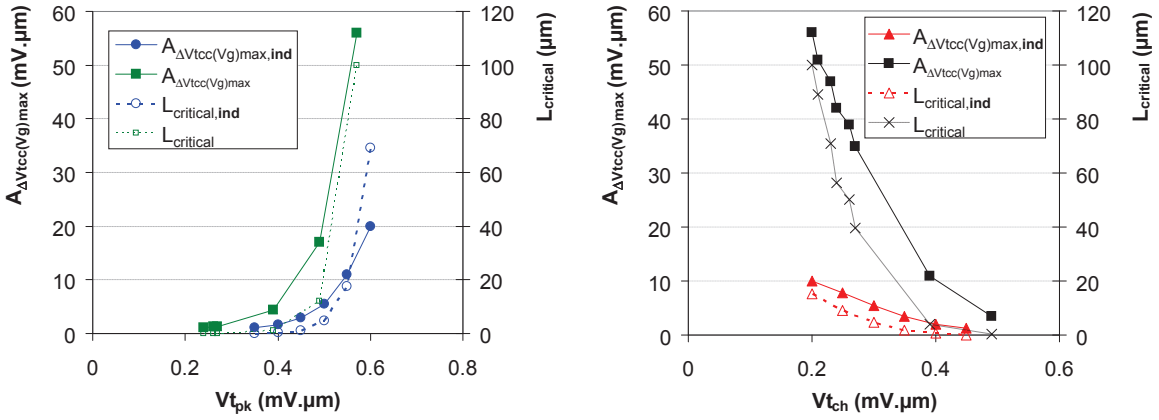
is a variation in Na, which have more influence in the transistor mismatch.



(a) (b)

Figure III.40: *The maximum value of the total mismatch ($A_{\Delta Vt(Vg)max}$) and the critical length ($L_{critical}$) comparison between previous results (P_{ind}) and the case where Na is varied as a function of (a) A_{pk} and (b)A_{ch}.*

Figure III.41(c) and (d) shows $A_{\Delta Vt(Vg)max}$ and the $L_{critical}$ variations in function of Vt_{pk} and Vt_{ch}. Comparing the influences of $Vt_{pk,ch}(Na)$ and $Vt_{pk,ch,ind}$ in $A_{\Delta Vt(Vg)max}$ and in $L_{critical}$ variations, the discrepancies observed are smaller than that shown in previous figure (figure III.40).



(a) (b)

Figure III.41: *The maximum value of the total mismatch ($A_{\Delta Vt(Vg)max}$) and the critical length ($L_{critical}$) comparison between previous results (P_{ind}) and the case where Na is varied as a function of (a)Vt_{pk} and (b) Vt_{ch}*

Thus, a variation in the Na provokes variations in the Vt and A_{Vt} parameters. But Vt and A_{Vt} parameters are not limited to the Na variations. Also, it was shown, as summarized in table

III.7, that a difference between Vt_{pk} and Vt_{ch} has an important influence in $A_{\Delta Vt(Vg)max}$ and $L_{critical}$. This influence can be explained by the exponentially dependent Vt on $A_{\Delta Vt(Vg)}$, as observed in equation (III.7) and (III.27). $A_{\Delta Vt(Vg)max}$ and $L_{critical}$ change exponentially with a variation with Vt_{pk} and Vt_{ch} (equation (III.34)), while A_{Vt} changes linearly (equations (III.35) and (III.36)). Thus, a difference in Vt has more impact in mismatch than a difference in the A_{Vt}. Hence, a difference between Vt_{pk} and Vt_{ch} has more influence in the $A_{\Delta Vt(Vg)max}$ than a difference in other parameters, as A_{pk} and A_{ch}.

$$A \sim e^{Vg-Vt(Na)} \tag{III.34}$$

$$A \sim A_{ch}(Na^{0.25}) \tag{III.35}$$

$$A \sim A_{pk}(Na^{0.4}) \tag{III.36}$$

Table III.7: *Summary of the analysis for the three studied cases (Abbreviations: constant (=), increase (↗), decrease (↘), linearly (lin), exponentially(exp)).*

Case	Na_{pk}	Na_{ch}	Vt_{pk}	Vt_{ch}	A_{pk}	A_{ch}	$L_{critical}$	$A_{\Delta Vt(Vg)_{max}}$
First	(-)	(-)	0.5V	0.35V	**Varied (↗)**	$1mV.\mu m$	=	lin↗
	(-)	(-)	0.5V	0.35V	$5mV.\mu m$	**Varied (↗)**	=	=
Second	(-)	(-)	**Varied (↗)**	0.3V	$1mV.\mu m$	$1mV.\mu m$	exp↗	exp↗
	(-)	(-)	0.5V	**Varied (↗)**	$1mV.\mu m$	$1mV.\mu m$	exp↘	exp↘
Third	**Varied (↗)**	$5 \times 10^{17}cm^{-3}$	$Vt_{pk}(Na_{pk})$	$Vt_{ch}(Na_{ch})$	$A_{pk}(Na_{pk})$	$A_{ch}(Na_{ch})$	exp↗	exp↗
	$4 \times 10^{18}cm^{-3}$	**Varied (↗)**	$Vt_{pk}(Na_{pk})$	$Vt_{ch}(Na_{ch})$	$A_{pk}(Na_{pk})$	$A_{ch}(Na_{ch})$	exp↘	exp↘

Difference on mismatch for N and PMOS transistors NMOS and PMOS devices present different fluctuations level. The level of fluctuations on PMOS transistors is smaller than that on NMOS devices for this 45nm technology, as showed previously in figure III.10. Moreover, the hump observed for long NMOS transistors is also attenuated on PMOS devices. A pertinent question is why NMOS and PMOS transistors have different mismatch behavior? To understand why this happens, two hypotheses have been made:

- ***1st hypothesis:*** The Na_{pk}/Na_{ch} ratio on NMOS transistor is more significant in comparison with PMOS transistors.
- ***2nd hypothesis:*** The difference between pocket and channel threshold voltage is higher for NMOS than in PMOS transistors.

These two hypotheses are analyzed with the model proposed on section III.3. For this matter, the following conditions have been applied, using the calibrated PMOS model:

- ***1st condition:*** The PMOS A_{pk} and A_{ch} parameters are replaced by those corresponding to the NMOS transistors. In this case, the PMOS threshold voltages, Vt_{pk} and Vt_{ch}, are conserved. This explains the 1^{st} hypothesis.
- ***2nd condition:*** The PMOS threshold voltages, Vt_{pk} and Vt_{ch}, are replaced by the threshold voltages corresponding to the NMOS transistors. In this case, the PMOS A_{pk} and A_{ch} are conserved. This explains the 2^{nd} hypothesis.

Table III.8: *Threshold voltage and mismatch parameters for NMOS and PMOS devices.*

Parameter	NMOS	PMOS
Vt_{ch}	0.35 V	-0.43 V
Vt_{pk}	0.51 V	-0.50 V
$A_{\Delta Vt_{ch}}$	1.01 mV.μm	0.7 mV.μm
$A_{\Delta Vt_{pk}}$	2.02 mV.μm	1.47 mV.μm

The values of the parameters used are presented for NMOS and PMOS devices are given in Table III.4 and Table III.5 respectively, and are reminded in following table III.8.

Figure III.42 shows the $A_{\Delta Vtcc(Vg)}$ as a function of the transistor length for the above conditions and the PMOS model.

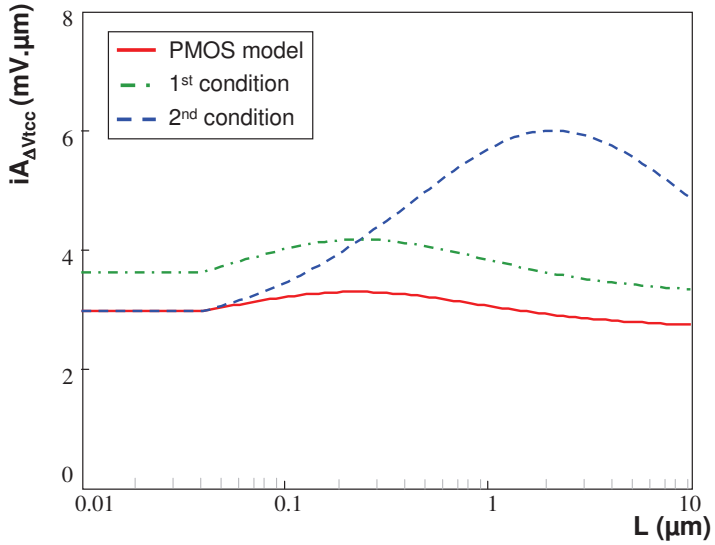


Figure III.42: *$A_{\Delta Vtcc(Vg)}$ as a function of the transistor length for the 1^{st} and 2^{nd} conditions and the modeled PMOS transistor.*

The second condition presents the highest mismatch level for long transistors. In this case, $Vt_{pk} = -0.5V$ and $Vt_{ch} = -0.35V$ while the values obtained for the PMOS transistors are $Vt_{pk} = -0.5V$ and $Vt_{ch} = -0.43V$. This supports the second hypothesis. As discussed before, a difference between Vt_{pk} and Vt_{ch} has more influence in the $A_{\Delta Vtcc(Vg)max}$ than a difference in the A_{pk} and A_{ch}. Indeed, the $A_{\Delta Vtcc(Vg)max}$ depends of the Vt_s exponentially.

Thus, for this 45nm technology, as the difference between pocket and channel threshold voltages are more significants for NMOS transistors, the level of fluctuations is also higher than in PMOS devices.

III.4 Conclusions Chapter II

It was shown that pocket regions have strong impact on transistor mismatch. A pocket engineering study was performed on NMOS transistors, to improve mismatch performances reducing random dopant fluctuations. The use of Indium during pocket-implant process clearly improve mismatch performance, not only for short transistors, but also for the long ones. Moreover,

adding other materials such as Carbon and Nitrogen help to get better matching performance than using only Indium implant. The co-implants properties should help to reduce the doping level in the channel. These mismatch performances improvement were explained by the lower doping level in the channel.

In the second part, the threshold voltage mismatch was modeled from weak to strong inversion, in linear regime. The proposed physical model based on three-transistors in series is useful for NMOS and PMOS transistors. In addition, thanks to this model it is possible to investigate the impact of each physical parameter. Moreover, the critical length can be obtained, which is an interesting parameter for designers.

Chapter IV

Current mismatch for all regions of operation on N-MOSFET

Up to now, mismatch analyses have been performed only for the linear regime. In this chapter, the drain-current mismatch is characterized from linear to the saturation regime. These characterizations are performed for transistors without pockets and for heavily pocket-implanted transistors. A general drain-current mismatch model, valid for any operation region, is also presented. It has been shown that correlated mobility and Vt fluctuations must be considered to qualitatively model the experimental results. A comparison between transistors with and without pocket is performed and an important drain-current mismatch enhancement in the latter case is reported and discussed.

IV.1 State of the art for drain-current mismatch

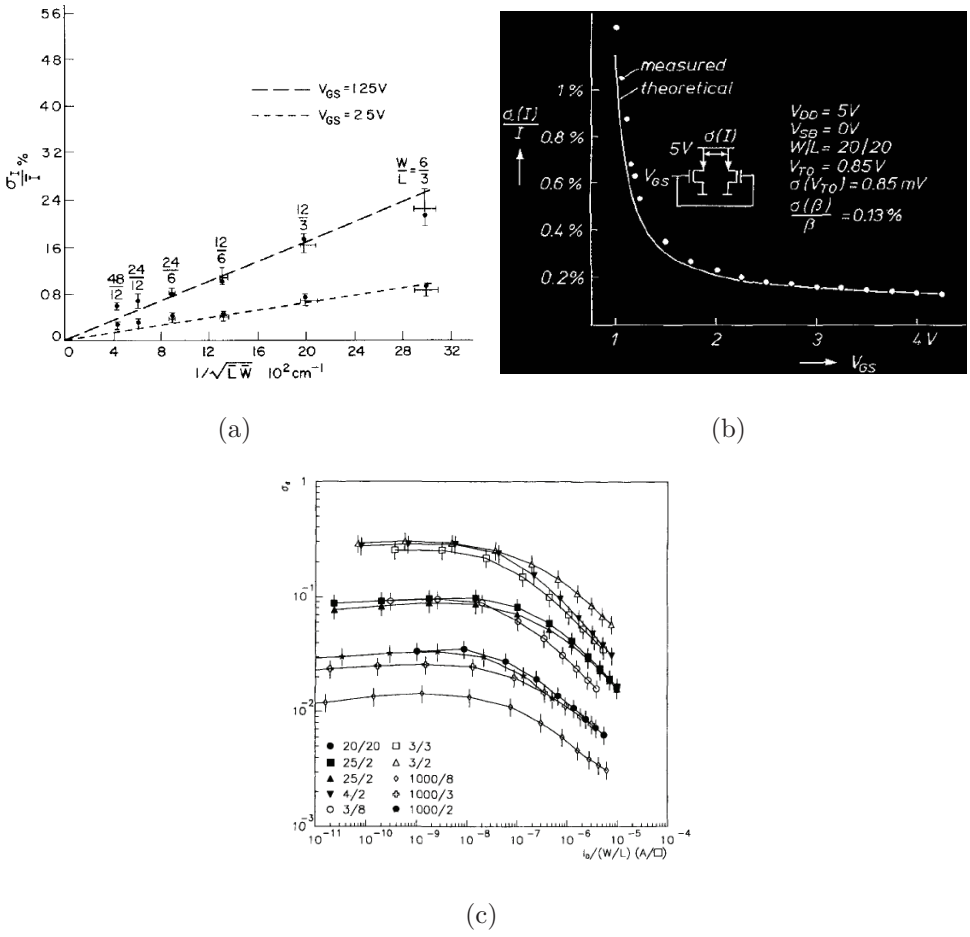
Drain current variations may imply serious consequences in circuit performance. For example, a current mirror provides the same current in different points of the circuit. If there is a drain-current variation, it should have an impact in the functionality of the circuit. Consequently, drain-current mismatch is also an important technological indicator and this chapter is dedicated to analyze drain-current mismatch.

The drain current fluctuations have been analyzed since the beginning of matching studies [Lakshmikumar 86]. Usually, drain current fluctuations are described by equation (IV.1).

$$\sigma^2_{\frac{\Delta I_D}{I_D}} = \left(\frac{g_m}{I_D}\right)^2 \sigma^2_{\Delta Vt} + \sigma^2_{\frac{\Delta\beta}{\beta}} \tag{IV.1}$$

This equation shows that drain current fluctuations can be induced by threshold voltage and gain factor fluctuations. These two parameters have been extensively analyzed to understand transistors mismatch.

Many studies can be found in the literature about drain current mismatch as a function of transistor geometries, gate bias and drain current density. Some of these results are shown in figure IV.1, for NMOS transistors.



(a) (b)

(c)

Figure IV.1: *Drain-current mismatch as a function of (a) transistor geometries [Lakshmikumar 86], (b) gate bias [Pelgrom 89] and current density [Forti 94].*

Drain current mismatch was experimentally studied in the weak inversion region by [Forti 94]. Previous works were all performed in the strong inversion region. In that work, the current mismatch as a function of the current density, represented in figure IV.1(c), shows a plateau at low currents that they have further analyzed in terms of device area and substrate voltage. These results clearly show differences in weak region compared with strong inversion, pointing out to the need of an analytical model from weak to strong inversion.

The model proposed by [Bastos 98] yields good results if either saturation or ohmic region operation (for small size transistors) is considered, but not both. If mismatch modeling is optimized for saturation, poor mismatch prediction is obtained for ohmic and vice-versa [Serrano-Gotarredona 99].

A mismatch model valid for all regions of operation, continuous from weak to strong inversion regions, has been published by [Croon 02a]. The drain-current mismatch model is based on the Pelgrom's model. It describes mismatch in the drain current as a function of mismatch in the threshold voltage, the current factor, the roughness scattering and the saturation velocity. It also makes qualitative predictions for the bulk bias dependence. It analyzes the mismatch as a function of gate bias and transistor geometries. This model gives a good estimation of mismatch in the saturation region. However, it has the same inconsistency observed in the Pelgrom's model and requires a larger number of fitting parameters. Despite it works continuously from weak to strong inversion, the model gives mismatch prediction relative errors in the weak inversion region of the order of 100%.

Yang et al. [Yang 03] developed a microscopic multitransistor model to analyze the impact of local fluctuation on current mismatch of the MOSFET. They pointed out that the two-transistors approach [Gray 01] considering one for the linear region and the other one for the saturation region is not self-consistent. Then, they used the approach which divides the transistor of length L into small sections of length ΔL, where the local fluctuation in each section can be calculated. It is a similar approach used to model the high frequency noise in non quasi static MOS [Goo 01]. That model proposed by Yang et al. presents accurate results, but it is limited to the strong inversion, as it diverges for overdrive voltages close to zero.

Drennan et al. [Drennan 03] proposed a drain current mismatch model. In that model, the drain current mismatch was analyzed through the contribution of each physical process parameters, resulting in a matrix of mismatch parameters. The total current variation yields the multiplication of the matrix by a vector composed of the standard deviation from each physical parameter. Although the procedure results in good approximations of the mismatch, there are many disadvantages due to its complexity. Characterization is also complicated as a large number of parameters are needed.

Serrano-Gotarredona et al. [Serrano-Gotarredona 03] proposed a five parameter mismatch model valid for all regions of operation, continuous from weak to strong inversion. The drain-current mismatch has been analyzed as a function of the gate bias and the transistor geometry. However, many parameters are necessary as, for each transistor type (NMOS or PMOS), the standard deviation of each parameter and the ten corresponding correlation terms are needed. This model was used by [Velarde-Ramirez 05] to compare with experimental results. Some disagreements are observed for small gate bias, especially for short transistors.

Recently, new approaches were presented based on an accurate physics-based model, which allows the assessment of mismatch from process parameter and is valid for any operating region [Klimach 04] [Galup-Montoro 05] [Klimach 06] [Klimach 08]. They analyzed the drain-current mismatch for drain-to-source voltage. The model does not include mobility effects. Moreover, only devices without pocket implants have been analyzed.

The models described before are sometimes too complex, valid for a specific regime or do not consider mobility effects. They are usually analyzed as a function of the transistor geometries,

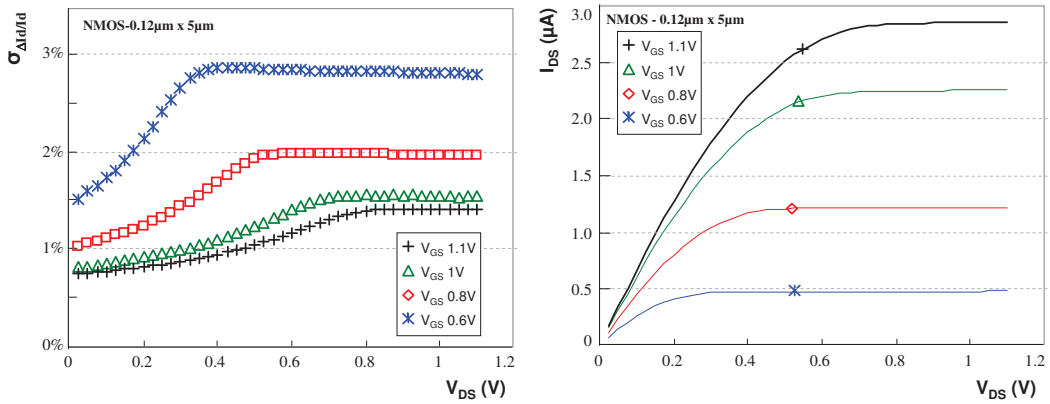
the gate bias or the drain current density. Concerning mismatch characterization as a function of drain-to-source bias, it has been performed on transistors without pocket-implants.

In this context, this chapter presents a quasi-analytical mismatch model valid for any operation regime as a function of the drain-to-source bias, including correlated mobility effects. The drain current mismatch is characterized for devices with and without pocket implants, which are presented and discussed in the following sections.

IV.2 Experimental drain-current mismatch on transistors without pocket-implants

The drain-current fluctuations $\sigma_{\Delta I_D/I_D}$ have been characterized for 45nm bulk transistors without pocket implants.

Figure IV.2(a) shows the experimental $\sigma_{\Delta I_D/I_D}$ as a function of the drain-to-source voltage for transistors without pocket-implants. The V_{DS} ranges from 25mV (linear region) to 1.1V (saturation region), for different gate bias (V_{GS} from 0.6V to 1.1V). The corresponding $I_D - V_{DS}$ is also plotted (figure IV.2(b)).



(a) (b)

Figure IV.2: *(a) Drain-current mismatch as a function of drain bias conditions at V_{GS}=[0.6, 0.8, 1 and 1.1]V and (b) corresponding $I_D - V_{DS}$.*

In figure IV.2(a), the current standard deviation increases until the transistor get into the saturation region. After this point, the standard deviation is constant. This mismatch behavior is in agreement with the one presented by [Klimach 08]. Only one transistor geometry was shown as the transistors without pocket-implants presents the same behavior.

The threshold voltage parameter is often interesting for circuit design,. The standard deviation of the equivalent input gate voltage mismatch can be easily obtained by normalizing $\sigma_{\Delta I_D/I_D}$ by the g_m/I_D, corresponding to the desired current density (equation (IV.2)).

$$\sigma_{\Delta Vg} = \frac{\sigma\left(\frac{\Delta I_D}{I_D}\right)}{g_m/I_D} \tag{IV.2}$$

The experimental normalized Vt mismatch parameter is shown in figure IV.3.

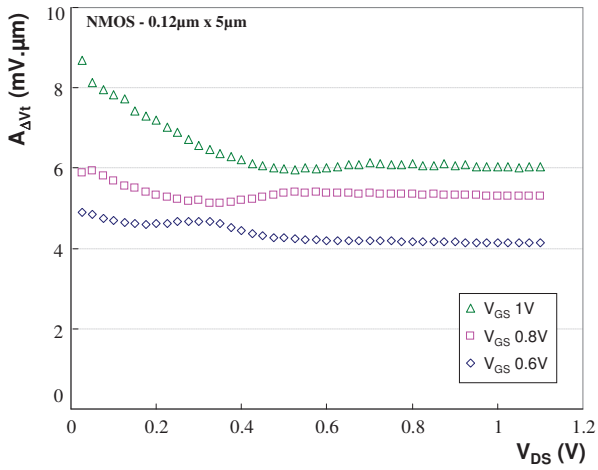


Figure IV.3: *Drain-current mismatch normalized into Vt mismatch parameter as a function of drain bias conditions at V_{GS} = [0.6, 0.8 and 1]V.*

A significant dependence for small drain bias conditions is observed, especially for high gate bias. A model for transistors without pocket-implants is then proposed to cover this case and it is discussed in the following section.

IV.3 Proposed drain-current mismatch model for transistors without pocket-implants

Two identical transistors, when submitted to identical potential bias, may show slightly different drain currents, due possibly to random local conductivity fluctuations along the channel. These local fluctuations are integrated along the channel, taking into account the main non-linear characteristics of the MOS. The integration of the local conductivity fluctuations have already been done by the $1/f$ noise approach [Christensson 68]. The mismatch and the noise have been shown as similar phenomena [Kinget 96], which depends on the process, bias and dimensions of the transistors.

A general drain current mismatch model has been developed by considering the impact of a local threshold voltage shift, δVt, in a portion of the channel, of area δa, as in the RTS noise approach [dit Buisson 92] (figure IV.4).

In the RTS noise approach, the relative drain current change due to a weak local conductivity variations, $\delta\sigma_{ch}$, reads (equation (A.3)),

$$\frac{\Delta I_D}{I_D} = \frac{\delta\sigma_{ch}}{\sigma_{ch}}\frac{\delta a}{a} = \frac{1}{\sigma_{ch}}\frac{\partial\sigma_{ch}}{\partial Vt}\frac{\delta a}{a}\delta Vt \tag{IV.3}$$

where a is the area of the transistor channel.

Calculating the local variance of the drain current fluctuations yields (equation (IV.4))

$$\sigma^2_{\frac{\Delta I_D}{I_D}<L>} = \left(\frac{1}{\sigma_{ch}}\frac{\partial\sigma_{ch}}{\partial Vt}\frac{\delta a}{a}\sigma_{\delta Vt}\right)^2 \tag{IV.4}$$

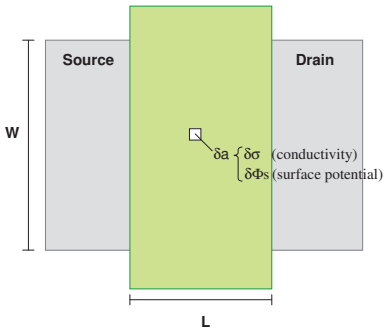


Figure IV.4: *Transistor schematic representing the elementary δa and the fluctuations in the conductivity $\delta\sigma$ and the surface potential $\delta\phi_s$.*

Replacing $\sigma_{\delta Vt}$ by using Pelgrom's model (equation (IV.5)),

$$\sigma_{\delta Vt} = \frac{A_{\delta Vt}}{\sqrt{\delta a}} \tag{IV.5}$$

the local variance can be expressed as (equation (A.4)).

$$\sigma^2_{\frac{\Delta I_D}{I_D}<L>} = \left(\frac{1}{\sigma_{ch}}\frac{\partial\sigma_{ch}}{\partial Vt}\right)^2 A^2_{\delta Vt}\frac{\delta a}{a^2} \tag{IV.6}$$

By integrating these fluctuations over the channel surface yields (equation (A.5)):

$$\sigma^2_{\frac{\Delta I_D}{I_D}} = \iint_0^{WL}\left(\frac{1}{\sigma_{ch}}\frac{\partial\sigma_{ch}}{\partial Vt}\right)^2 \frac{A^2_{\delta Vt}}{a^2}\,dx\,dy \tag{IV.7}$$

The gradual channel approximation enables the drain current to be expressed by (equation (IV.8)) [Sah 66]:

$$I_D = W\sigma_{ch}\frac{dUc}{dx} \tag{IV.8}$$

where Uc is the quasi Fermi level shift along the channel.

Making a change of variables $x \rightarrow Uc$, where,

$dx = \frac{W\sigma_{ch}dUc}{I_D}$

$x : 0 \rightarrow L$

$Uc : 0 \rightarrow V_{DS}$

the drain current variance can be expressed as (equation (IV.9)),

$$\sigma^2_{\frac{\Delta I_D}{I_D}} = \frac{1}{W}\int_0^{V_{DS}}\left(\frac{\partial ln(\sigma_{ch})}{\partial Vt}\right)^2 \frac{A^2_{\delta Vt}}{L^2}\frac{\sigma}{I_D}\,dUc \tag{IV.9}$$

Accounting for current conservation along the channel, drain current is derived from equation (IV.8) as [Sah 66]:

$$I_D = \frac{W}{L}\int_0^{V_{DS}}\sigma\,dUc \tag{IV.10}$$

The relation between the channel conductivity and the inversion charge[1] is given by (equation (IV.11)):

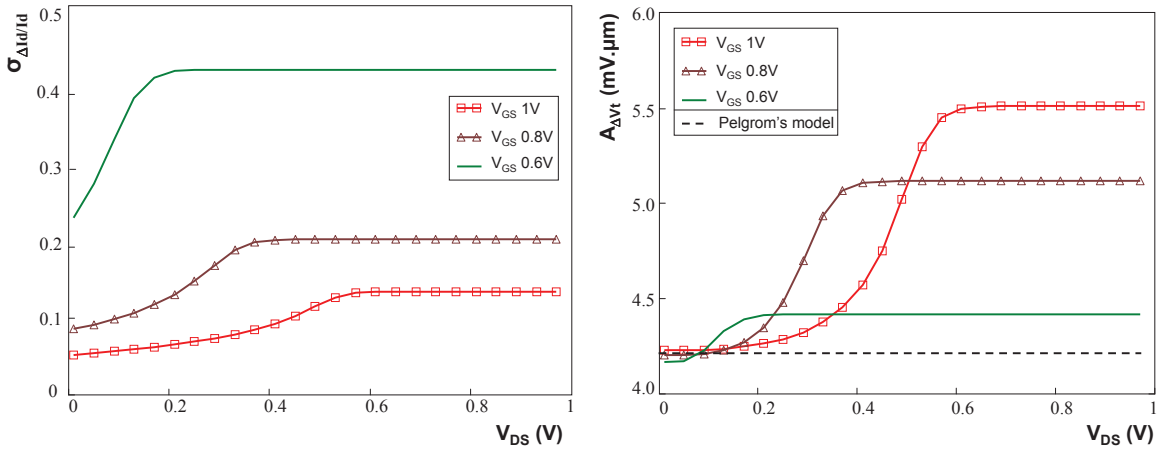
$$\sigma_{ch} = \mu_{eff}Q_{inv} \tag{IV.11}$$

[1]This equation is described in *Chapter II*, equation (III.8).

Finally, with $\sigma = \mu_{eff} Q_{inv}$, the drain current variance yield (equation (IV.12)),

$$\sigma^2_{\frac{\Delta I_D}{I_D}} = \frac{\int_0^{V_{DS}} \left(\frac{\partial ln(\mu_{eff} Q_{inv})}{\partial Vt} \right)^2 \frac{A^2_{\delta Vt}}{WL} \mu_{eff} Q_{inv} \, dUc}{\int_0^{V_{DS}} \mu_{eff} Q_{inv} \, dUc} \tag{IV.12}$$

The drain-current mismatch model and the converted gate voltage mismatch model as a function of drain bias are plotted in figure IV.5 for $Na = 10^{17} cm^{-3}$, $t_{ox} = 1.5nm$, $V_{GS} = 1.2V$, $L = 0.2\mu m$ and constant mobility $\mu = 350 cm^2/Vs$.



(a) (b)

Figure IV.5: *(a)Drain-current mismatch model as a function of the drain bias at Vg=[0.6, 0.8 and 1]V and (b) drain-current mismatch converted in a constant threshold voltage mismatch.*

The drain-current mismatch model (figure IV.5(a)) seems to qualitatively model the experimental results (figure IV.2(a)). A difference can be seen when comparing modeled (figure IV.5(b)) and experimental results (figure IV.3) for the converted gate voltage mismatch. This difference can be due to the transistor mobility, and will be studied in the next section.

IV.3.1 Influence of mobility and threshold voltage fluctuations in drain-current mismatch

The proposed drain-current mismatch model is analyzed considering three different conditions. The threshold voltage fluctuations (δVt) induced by random dopants fluctuations are taken into account for the three cases. In term of mobility, one case considers a constant effective mobility. For both remaining cases, the electrical field-dependent mobility is considered. In the last case, since both mobility and Vt fluctuations are generated by the same source (random doping fluctuations), they are naturally correlated. Then, correlated doping-mobility fluctuations are also taken into account. A description of these three adopted conditions is presented.

IV.3.1.a Threshold voltage fluctuations and constant mobility ($\delta Vt + \mu_{eff}$)

In this case, in addition to the Vt fluctuations, the effective mobility is considered constant along the channel. The mobility depends on the impurities concentration. The expression of the electrons mobility in the volume zone, according to the Na impurity concentration and temperature yields [Caughey 67].

$$\mu_b = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{Na}{N_{ref}}\right)^{\alpha}} \tag{IV.13}$$

where μ_{min}, μ_{max}, N_{ref} and α are coefficients which vary slightly according to [Caughey 67] [Jacoboni 77] [Masetti 83]. In this work, the values adopted for these parameters are: $\mu_{min} = 70cm^2/Vs$, $\mu_{max} = 1270cm^2/Vs$, $N_{ref} = 1.2 \times 10^{17}cm^{-3}$ and $\alpha = 0.8$.

IV.3.1.b Threshold voltage fluctuations and electric-field-dependent mobility ($\delta Vt + \mu_{eff}(E_{eff})$)

In this case, in addition to the Vt fluctuations, the electric-field-dependent mobility is considered. The effective mobility depends on the transverse field, $\mu_{eff}(E_{eff})$, seen by the carriers. As a consequence, it is not constant along the depth of the transistor channel.

The effective field is defined as the average transverse electric field taken on the distribution of the inversion layer (equation (IV.14)) [Ando 82] [Sabnis 79],

$$E_{eff} = \frac{|Q_{dep}| + \eta |Q_{inv}|}{\varepsilon_{Si}} \tag{IV.14}$$

where η is a parameter that reflects the spreading of the inversion layer in the silicon, Q_{inv} and Q_{dep} are the inversion and depletion layer charge per unit surface area respectively. In this study, where Si substrate is $< 001 >$-oriented with transport $< 110 >$-oriented, $\eta = 1/2$ in the case of electrons [Sabnis 79] [Sun 80] [Takagi 94] and $\eta = 1/3$ for holes [Watt 87] [Takagi 94] [Arora 87] at 300K.

The universal law of mobility can be decomposed into several components representing scattering mechanisms. These components depend on the effective field. Sun and Plummer [Sun 80] have summarized the three main types of dispersal mechanisms that account for the evolution of mobility in the inversion layer when the gate voltage exceeds the threshold voltage. These mechanisms, represented in figure IV.6, are described in following paragraphs.

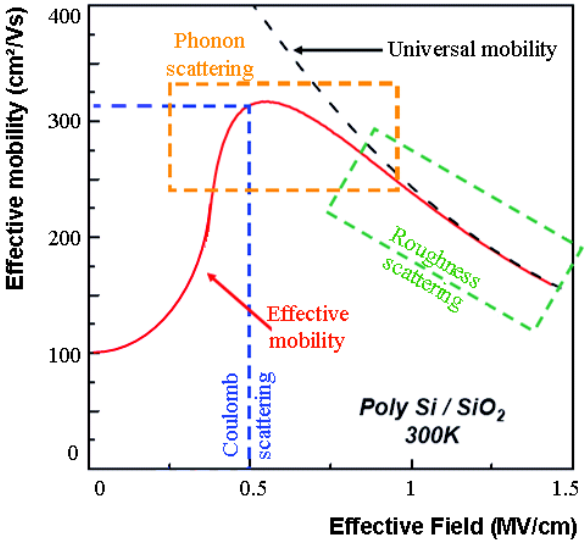


Figure IV.6: *Effective mobility in function of the effective field. The different scattering characteristic at ambient temperature (300K) and the universal mobility are also represented [Takagi 94].*

Mobility due to surface roughness scattering μ_{sr}, predominant at high effective field. The presence of the Si/SiO_2 interface is perceived by the carriers of the inversion layer as a set of potential perturbations. Surface roughness is defined as [Walker 87]:

for electrons:

$$\mu_{sr} = 1450 \cdot E_{eff}^{-2.9} \quad \left[\frac{cm^2}{V.s}\right] \; at \; 300K \tag{IV.15}$$

and for holes:

$$\mu_{sr} = 140 \cdot E_{eff}^{-1} \quad \left[\frac{cm^2}{V.s}\right] \; at \; 300K \tag{IV.16}$$

Mobility due to phonon scattering μ_{ph}, predominant at medium effective field. These interactions are related not only to phonons of the solid material of the channel, but also to surface phonons that occur at the Si/SiO_2 interface. For temperatures below 100K, the interactions with acoustic phonons dominate. Beyond this temperature, the interactions with optical phonons dominate. The mobility due to phonon scattering is defined as [Walker 87]:

for electrons:

$$\mu_{ph} = 330 \cdot E_{eff}^{-0.3} \quad \left[\frac{cm^2}{V.s}\right] \; at \; 300K \tag{IV.17}$$

for holes:

$$\mu_{ph} = 90 \cdot E_{eff}^{-0.3} \quad \left[\frac{cm^2}{V.s}\right] \; at \; 300K \tag{IV.18}$$

Mobility due to Coulomb scattering or impurety scattering μ_c, predominant at weak effective field. It results from the scattering between the carriers of the inversion layer,

localized charges within the oxide, interface charges and ionized impurities in the volume. The Coulomb scattering is generally considered, although its contribution is not universal. In highly doped channel, Coulomb-scattering is responsible for a high degradation of linear and saturation current, and can lead to a deformed I_D-V_{DS} curves. A practical model of the Coulomb-limited mobility has been proposed by Masetti et al. [Masetti 83].

Boeuf et al. [Boeuf 09] take into account that the inversion charge created in the transistors channel screens the ionised impurity charge responsible for Coulomb limited mobility. As a result, a corrected value of μ_c, for electrons and holes, has been defined as:

$$\mu_c = \mu_b \left(\frac{\alpha Q_{dep}(Na)}{Q_{inv}(Na, E_{eff}) + \alpha Q_{dep}(Na)} \right)^{-1} \left[\frac{cm^2}{V.s} \right] \tag{IV.19}$$

where α is a fitting parameter (in this work, α=0.1).

When the inversion charge Q_{inv} is smaller than the depletion charge Q_{dep}, which separates the weak and the strong inversion regimes, the corrected mobility is equal to the mobility term calculated with the Masetti model (IV.13). This is typically the case in the sub-threshold regime. When Q_{inv} starts to dominate at strong inversion, the corrected mobility term increases, reflecting the average screening effect of the inversion charge on carriers.

The effective mobility takes into account the average mobility seen by the inversion layer (equation (IV.20)) [Fischetti 02].

$$\frac{1}{\mu_{eff}} = \sum_s \frac{1}{\mu_s} \tag{IV.20}$$

Then, the total mobility in inversion layer can be extrapolated using Matthiessen's law [Lombardi 88]:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_c} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}} \tag{IV.21}$$

For NMOS transistors, the effective mobility can then be expressed as:

$$\mu_{eff}(E_{eff}) = \left(\left(\frac{1200}{1 + \left(\frac{Na}{1.2\times10^{17}} \right)^{0.8}} + 70 \right) \left(\frac{0.1 Q_{dep}(Na)}{Q_{inv}(Na, E_{eff}) + 0.1 Q_{dep}(Na)} \right) + \frac{E_{eff}^{2.9}}{1450} + \frac{E_{eff}^{0.3}}{330} \right)^{-1} \tag{IV.22}$$

IV.3.1.c Correlated threshold voltage fluctuations and mobility fluctuations ($\delta Vt + \delta\mu_{eff}(E_{eff})$)

Difrenza et al. [Difrenza 02] have showed that doping fluctuations due to random dopants induces mobility fluctuations. These effects are then considered and analyzed in this section.

Fluctuations in channel doping generate fluctuations in the threshold voltage and also fluctuations in mobility. Thus, equation (A.3) should be rewritten as equation (IV.23)

$$\frac{\Delta I_D}{I_D} = \frac{1}{\sigma_{ch}} \left(\frac{\partial \sigma_{ch}}{\partial Vt} \delta Vt + \frac{\partial \sigma_{ch}}{\partial Na} \delta Na \right) \frac{\delta a}{a} \tag{IV.23}$$

Resulting in,

$$\frac{\Delta I_D}{I_D} = \frac{1}{\sigma_{ch}} \left(\frac{\partial \sigma_{ch}}{\partial Vt} \delta Vt + \frac{\partial \sigma_{ch}}{\partial Na} \frac{\delta Na}{\delta Vt} \delta Vt \right) \frac{\delta a}{a} \tag{IV.24}$$

Which can be rewritten as equation (IV.25)

$$\frac{\Delta I_D}{I_D} = \frac{1}{\sigma_{ch}} \left(\frac{\partial \sigma_{ch}}{\partial Vt} + \frac{\partial \sigma_{ch}/\partial Na}{\delta Vt/\delta Na} \right) \delta Vt \frac{\delta a}{a} \tag{IV.25}$$

Considering $\sigma = \mu_{eff} Q_{inv}$:

$$\frac{\Delta I_D}{I_D} = \frac{1}{\mu_{eff} Q_{inv}} \left(\frac{\partial \mu_{eff} Q_{inv}}{\partial Vt} + Q_{inv} \frac{\partial \mu_{eff}/\partial Na}{\delta Vt/\delta Na} \right) \delta Vt \frac{\delta a}{a} \tag{IV.26}$$

leading to:

$$\frac{\Delta I_D}{I_D} = \left(\frac{\partial ln(\mu_{eff} Q_{inv})}{\partial Vt} + \frac{\partial ln(\mu_{eff})/\partial Na}{\delta Vt/\delta Na} \right) \delta Vt \frac{\delta a}{a} \tag{IV.27}$$

Thus, the term $\frac{\partial ln(\mu_{eff} Q_{inv})}{\partial Vt}$ in equation (IV.12) is added to the term (IV.28)

$$\frac{\partial ln(\mu_{eff})/\partial Na}{\delta Vt/\delta Na} \tag{IV.28}$$

resulting:

$$\sigma^2_{\frac{\Delta I_D}{I_D}} = \frac{\int_0^{V_{DS}} \left(\frac{\partial ln(\mu_{eff} Q_{inv})}{\partial Vt} + \frac{\partial ln(\mu_{eff})/\partial Na}{\delta Vt/\delta Na} \right)^2 \frac{A^2_{\delta Vt}}{WL} \mu_{eff} Q_{inv} \, dUc}{\int_0^{V_{DS}} \mu_{eff} Q_{inv} \, dUc} \tag{IV.29}$$

In this case, the electric-field-dependent mobility is considered.

IV.3.1.d Drain-current mismatch with the various mobility and threshold voltage fluctuations conditions

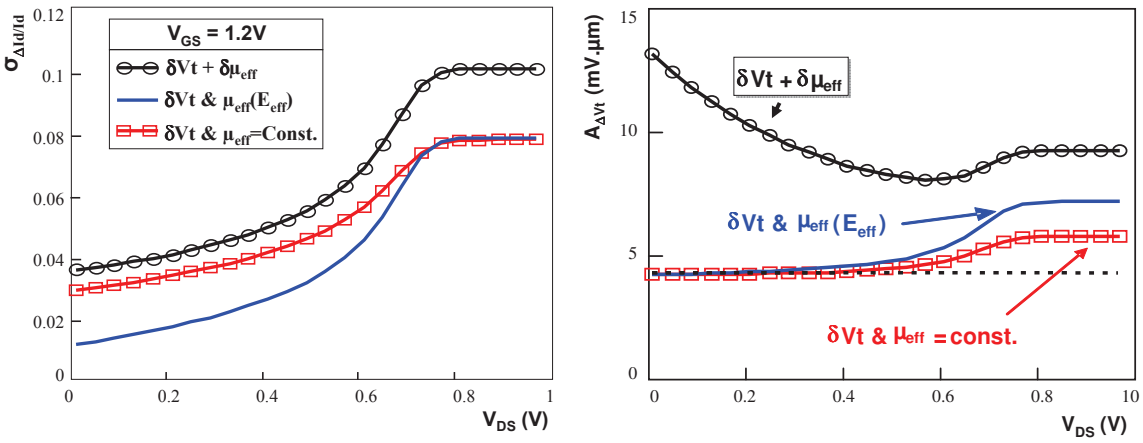
The proposed drain-current model as a function of drain bias is analyzed considering the discussed conditions of mobility and fluctuations, summarized in table IV.1.

Table IV.1: *Various conditions applied in the drain-current mismatch model.*

Case	Fluctuations	Mobility	Fermi Level
$\delta Vt + \mu_{eff} = const$	$\delta Vt(Na)$	μ_{eff}	Variable
$\delta Vt + \mu_{eff}(E_{eff})$	$\delta Vt(Na)$	$\mu_{eff}(E_{eff})$	Variable
$\delta Vt + \delta\mu_{eff}(E_{eff})$	correlated $\delta Vt(Na)$ and $\delta\mu(Na)$	$\mu_{eff}(E_{eff})$	Variable

Figure IV.7 shows $\sigma_{\Delta I_D/I_D}$ and the $A_{\Delta_{Vg}}$ as a function of the drain-to-source bias.

A significant $\sigma_{\Delta I_D/I_D}$ shift is observed in figure IV.7(a), for the three cases. Observing the drain-current mismatch converted into gate voltage fluctuations (figure IV.7(b)), when the first case is considered ($\delta Vt + \mu_{eff} = const$), the $A_{\Delta_{Vg}}$ increases at high V_{DS} biasing, as the vertical eletrical field varies. For the second case ($\delta Vt + \mu_{eff}(E_{eff})$), a shift is observed at high V_{DS} due the effective field dependence. Finally, considering doping-mobility correlation ($\delta Vt + \delta\mu_{eff}(E_{eff})$), a strong dependence for small V_{DS} conditions is observed. Only that case



(a) (b)

Figure IV.7: *Modeled (a) drain-current mismatch as a function of drain bias applying different mobility conditions at $V_{GS} = 1.2V$ and (b) converted drain-current mismatch into gate voltage fluctuations.*

where doping-mobility correlation is considered as capable to represent the experimental results, showed previously on figure IV.2.

The impact of pocket-implants on mismatch as a function of drain bias has not been observed yet. That is the subject of following section.

IV.4 Experimental drain-current mismatch on transistors with pocket-implants

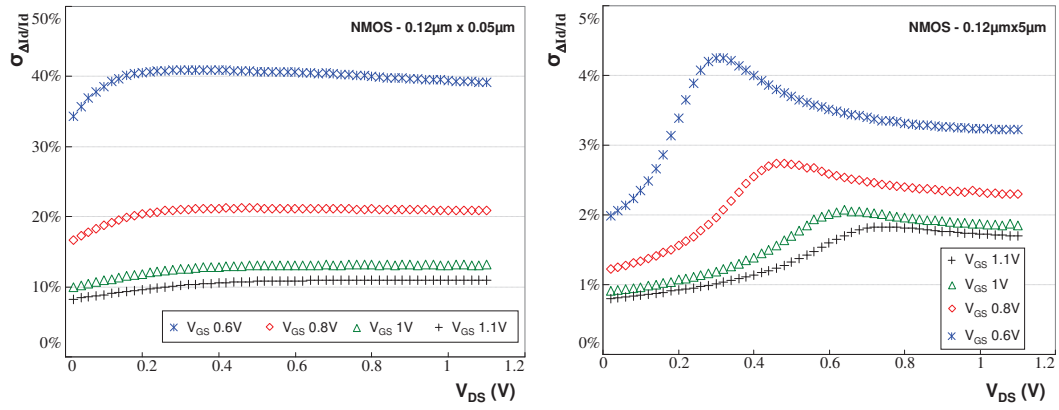
The drain-current fluctuations ($\sigma_{\Delta I_D/I_D}$) as a function of V_{DS} is now analyzed for transistors with pocket-implants. Figure IV.8 shows these fluctuations for a short and a long transistor (L = $0.05\mu m$ and $5\mu m$ respectively).

Short transistors have the same behavior as a transistor without-pocket implant. This is consistent with the fact that the channel is uniform.

For long transistors, the standard deviation increases with drain bias and it starts to decrease when the transistor gets into the saturation region. After this point, the standard deviation tends to a constant value. A strong increase of the mismatch is observed in the non-linear region. This may be attributed due to the non-uniform channels of the heavily doped pocket-implants.

As for transistors without pocket, current fluctuations have been converted into a Vt mismatch parameter (equation (IV.2)) and are represented in figure IV.9.

Here, the mismatch increases in the non-linear region. The difference between devices with and without pocket-implants will be analyzed in details in next section.



(a) Short transistor (b) Long transistor

Figure IV.8: *Drain-current fluctuation as a function of drain bias at V_{GS} = [0.6, 0.8, 1 and 1.1] V for (a) short and (b) long transistors with pocket-implants.*

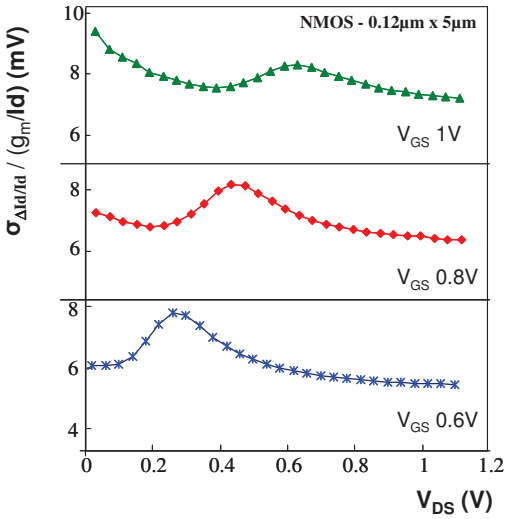


Figure IV.9: *Converted drain-current mismatch into a threshold voltage mismatch as a function of the drain bias for a long NMOSFET with pocket-implants at V_{GS} = [0.6, 0.8 and 1]V.*

IV.5 Drain-current mismatch comparison between transistors with and without pocket-implants

A comparison of the drain-current mismatch as a function of the drain bias between transistors with and without pocket-implants has been performed. Only long transistors have been compared, since these are the only transistors available without pocket-implants.

Current mismatch has been extensively analyzed in the linear region. The results obtained in this work should be in accordance with the results from the literature. The $\sigma_{\Delta I_D/I_D}$ is then analyzed in the linear region (figure IV.10). In this figure, two points can be highligthed:

– transistors with pocket implant presents more fluctuations than transistor without pocket-

implants

– fluctuations increases as gate bias decreases.

These results follow those obtained by [Cathignol 09] [Hook 10].

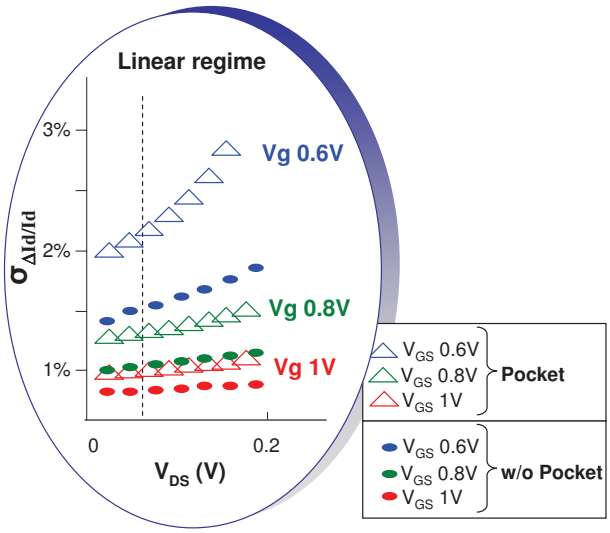


Figure IV.10: *Drain-current fluctuations in linear regime at V_{GS}=[0.6, 0.8, 1]V for transistor with and without pocket-implants.*

Comparing $\sigma_{\Delta I_D/I_D}$ from linear to saturation region, the mismatch for transistors with pocket-implants increases for any drain bias conditions (figure IV.11). These transistors clearly show increased mismatch in the non-linear regime.

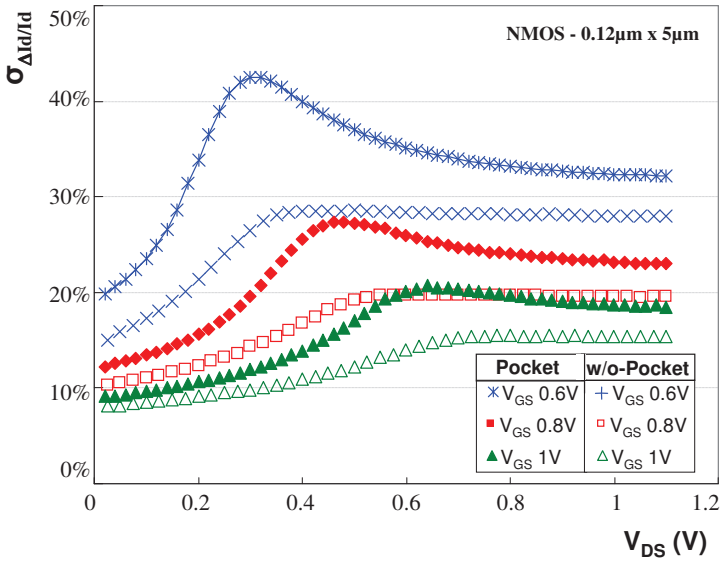


Figure IV.11: *Drain-current fluctuations as a function of drain bias at V_{GS}=[0.6, 0.8, 1]V for transistor with and without pocket-implants.*

After converting to a Vt mismatch (figure IV.12), the abnormal behavior in non-linear region is still observed. This is not explained by the model of equation (IV.12), valid only for uniformly doped channel devices [Mezzomo 10].

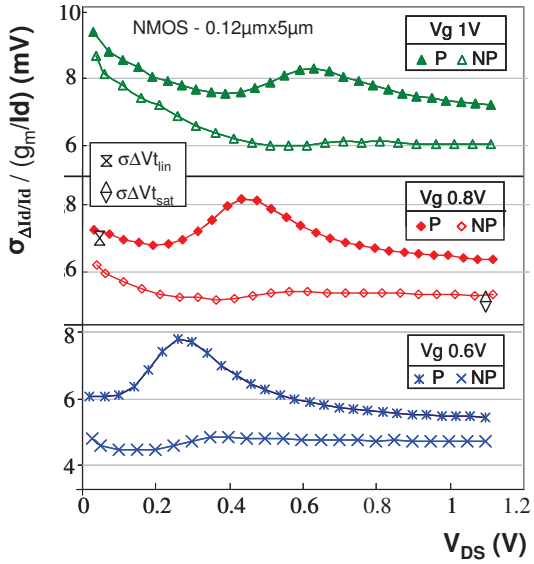


Figure IV.12: *Converted drain-current fluctuations into threshold voltage mismatch as a function of drain bias at V_{GS}=[0.6, 0.8, 1]V for transistor with and without pocket-implants.*

To model the mismatch for any operation regimes in non-uniform channels, a three-transistors model can be considered, as shown in schematic IV.13. However, a numerical analysis will be necessary to solve it, as the potentials in A and B are unknown.

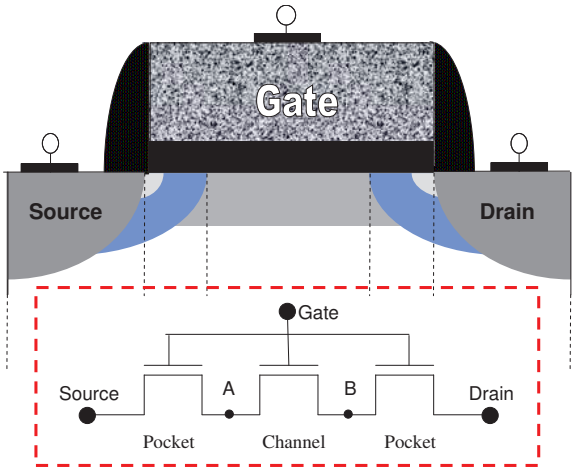


Figure IV.13: *A three-transistors in series to model transistors with pocket-implants.*

IV.6 Conclusions Chapter III

This chapter analyzed the drain-current mismatch as a function of drain-to-source bias.

A general drain current mismatch model has been proposed. It is valid for any operation regime - from linear to saturation regime and from weak to strong inversions. It has been

developed by considering the impact of a local threshold voltage shift, in a portion of the channel, as in the RTS noise approach.

Three different cases have been analyzed. In all cases, random dopant fluctuations are used to calculate the Vt fluctuations. In addition to the Vt fluctuations, one case considers constant mobility along the channel, the second one uses electric-field-dependent mobility, and the last one adds the correlated doping-mobility fluctuations. Only the case considering correlated threshold voltage and mobility fluctuations due to random doping is found to be appropriate for interpreting the experimental data.

The drain-current mismatch as a function of the drain-to-source voltage has also been characterized for devices with and without pocket-implants, in 45nm bulk MOSFET technology. An abnormal behavior has been observed for long transistors with pocket. The drain current fluctuations rise when the transistor varies from linear to saturation regime. The increase of the fluctuations is already known for transistor dimensions and gate bias, and is now also observed for drain bias conditions.

Chapter V

Perspectives for the transistor mismatch

Matching studies have been performed in previous chapters for 45nm Bulk MOSFET technology, focusing on random dopant fluctuations. Beyond 45nm technology node, the line edge roughness is pointed out in the literature as one of the main limiting factor, which is discussed in this chapter. It is proposed to evaluate the maximum roughness a gate can have so that the device remains not impacted. Moreover, to shrink the dimensions of the transistor beyond 45nm, literature shows that new transistor architectures are required. The trends on innovative technologies are then discussed and some characterizations obtained for 28nm are shown.

V.1 Impact of gate roughness on mismatch in 45nm technology and beyond

The line edge and line width roughness (LER and LWR respectively) are considered to be the main limiting factors in future technology [ITR 09]. They have caused little worry in the past since the critical dimensions of the transistor were far greater than its roughness. Miniaturization of the components allowed device dimensions to be into the nanometer scale [Harriott 01]. However, LER has not scaled accordingly, becoming an increasingly larger fraction of the gate length [Asenov 03]. In this section, the transistor gate roughness mismatch is experimentally analyzed on N and PMOS devices, in 45nm technology node.

V.1.1 Line-edge roughness and line-width roughness

The gate line of the transistors may present some roughness. Line edge roughness (LER) consists of 3σ deviation of the edge from the line fit and line width roughness (LWR) is defined as the 3σ deviation of width (critical dimension), as illustrated in figure V.1.

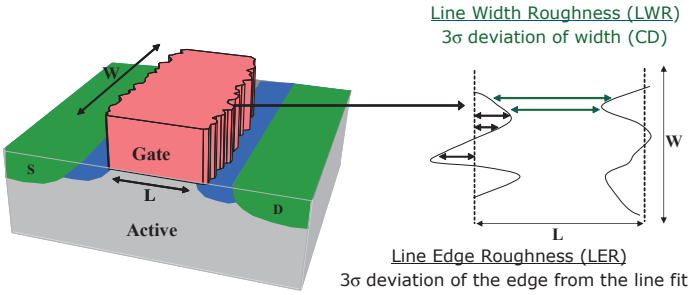


Figure V.1: *Illustration of line-edge roughness (LER) and line-width roughness (LWR).*

Gate roughness can be produced in lithography and etching processes. There are many factors contributing to it. Some examples are [Xiong 02]:

- photo-resist line roughness: depends on photo-resist type, thickness, substrate reflectivity, image contrast as well as process conditions;
- gate polysilicon etching condition;
- polysilicon grain size and doping.

In the end of the nineties, literature pointed out that the roughness on the gate edge does not scale down according to the scale of polysilicon line widths below 100nm [Linton 98] [Oldiges 00]. Random variations of MOS dimensions due to lithography and etching processes are a source of electrical parameter variability (figure V.2) [Kaya 01], introducing transistor mismatch [Asenov 03].

First investigations of the effects of LER were made by 2D [Oldiges 00, Linton 02] or 3D [Kaya 01, Asenov 03] device simulations. In the case of 2D simulations, the polysilicon gate is divided in small segments and for each segment the current is found from the simulation. An analytical model was proposed by Diaz et al. [Diaz 01] using the 2D approach, describing the drain current of a segment. In [Linton 02, Croon 02a] simulations were calibrated on 0.13μm technology on which the LER was exaggerated. From SEM top-view, Croon et al. found that the roughness of both polysilicon edges can be considered uncorrelated. This mean that the variance of the LWR is two times the variance in LER ($\sigma^2_{LWR} = 2\sigma^2_{LER}$).

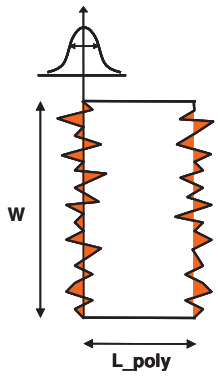


Figure V.2: *Illustration of line edge roughness (LER) as a source of variability.*

The variance of a electrical parameter P is defined as equation V.1 [Croon 02a]

$$\sigma^2_{\Delta P} \cong \left(\frac{\partial \Delta P}{\partial L}\right)^2 \sigma^2_{<L>} \tag{V.1}$$

where $\sigma_{<L>}$ is the standard deviation of the average length and it is inversely proportional to transistor width [Croon 04]. Hence, LER should specially degrade the mismatch for narrow devices.

Some research about LER impact on mismatch have been made for advanced technologies, such as FinFET and FD-SOI transistors [Dixit 06, Gustin 06, Li 09, Baravelli 08, Patel 08, Yu 09]. These technologies have slightly doped channels, reducing the random dopants fluctuations. Indeed, the LER is difficult to be reduced due to patterning processes, becoming a critical challenge to shrink transistors [Gogolides 06].

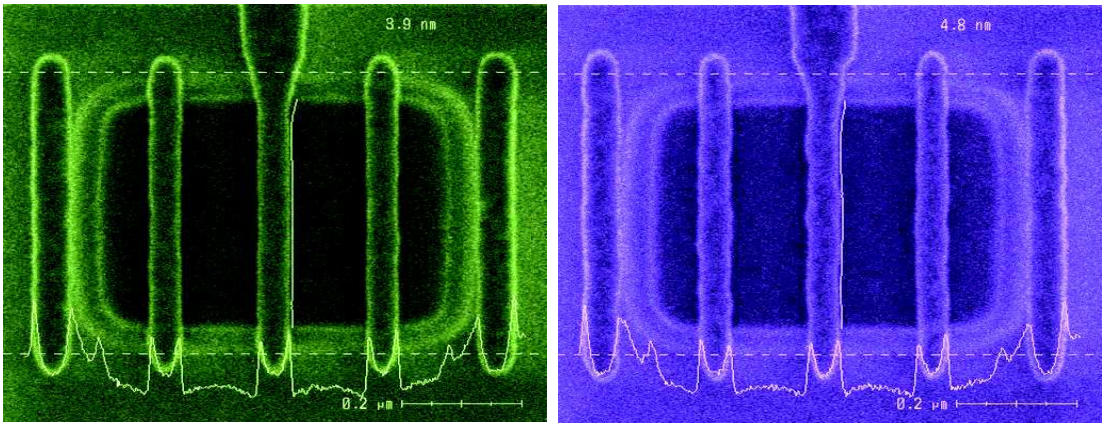
Experimental data to quantify the impact of line-edge roughness on mismatch are sparse. Some of the works used SEM top-views to validate a line-edge roughness model [Diaz 01, Linton 02, Xiong 04, Kim 04, Gustin 08]. An experimental mismatch investigation was done by [Croon 04], but on 130nm technology.

In this context, an experimental study has been performed to investigate the impact of line edge roughness on mismatch for a 45nm technology node. It consists of an intentional degradation of the gate roughness on a mismatch test structure, followed by an electrical characterization. That degradation and the corresponding experimental results are discussed in following sections.

V.1.2 Degradation methodology comparative study and morphological results

One of the procedures used to provide straight polysilicon gate is the hardening of the resin used to form the gate by a plasma HBr during gate etching process [Martin 08] [Pargon 09]. To provide the degradation of the gate roughness, the resist was not hardened. The resist should have some deformations, thus a higher gate roughness.

For this study, three wafers have been processed [Babaud 10]. One followed the reference process, including the resist hardening step. For the other two, the polysilicon gate of the transistors has been degraded. The same step has been applied to make the degradation: the resist has not been hardened, degrading the gate roughness. The results of this degradation are shown in figure V.3.



(a) Reference (b) Degraded sample

Figure V.3: *SEM top-view of a mismatch test structure with the polysilicon-gate rounded by four poly-dummies.*

Scanning Electron Microscopy (SEM) has been used to measure the gate roughness, using a dedicated recipe. However, this recipe on mismatch test structure was not efficient to measure its roughness, as the mismatch test structures have too small dimensions. The gate roughness was then measured in a test structure dedicated to control the transistor dimensions. The LER measured for the reference is 3.6nm while for the degraded wafers is 4.6nm, showing a variation around 28% (1nm). Although it was not possible to measure directly in the mismatch test structures, SEM top views show that removing the resist hardening induces visible gate roughness degradations on these structures.

The experimental results are shown and discussed in following section.

V.1.3 Experimental results for the impact of gate roughness on mismatch

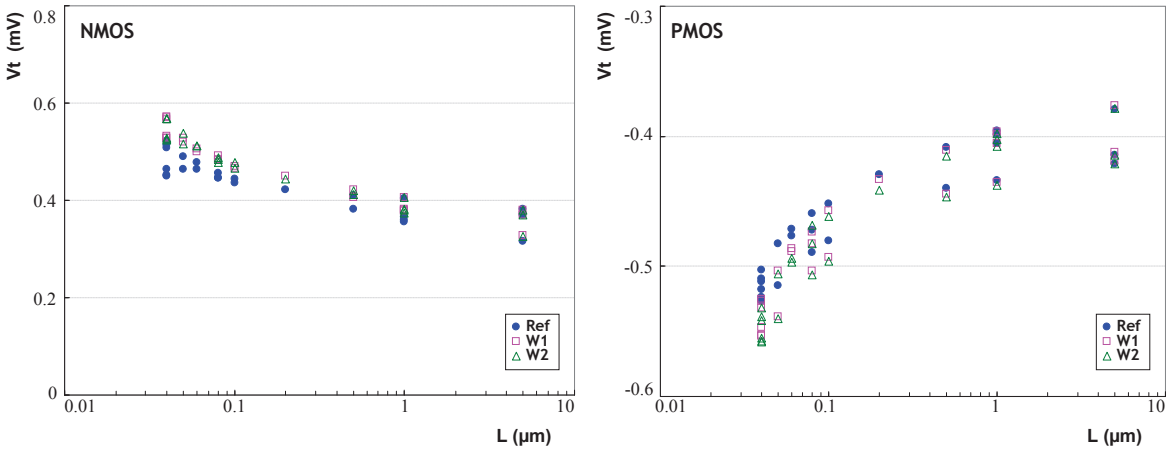
Threshold voltage is showed on figure V.4, for NMOS and PMOS devices. The two degraded wafers present the same behavior. A slight difference between the reference and the degraded wafers can be noticed in NMOS devices, for small gate lengths (∼50mV). On PMOS devices, no differences are observed.

Figure V.5 shows the $iA_{\Delta Vt}$ as a function of gate length. The two degraded wafers are compared to the reference. The threshold voltage mismatch $iA_{\Delta Vt}$ is reported for both N and PMOS transistors. However, no difference is observed between reference and degraded wafers.

Since the mismatch due to LER has more impact on narrow transistors, figure V.6 shows narrow transistors $A_{\Delta Vt}$ for both reference and degraded wafers. On the left of each graph, all gate widths are represented. On the right side, only geometries with gate width smaller than 0.2μm are considered. No important difference is noticed among the three splits, even for the narrow ones.

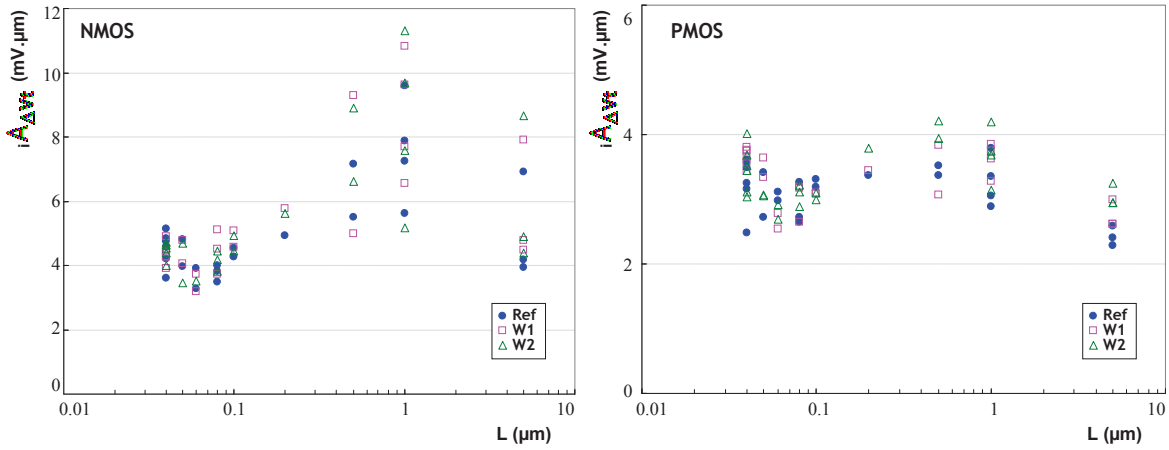
The gain factor mismatch is also reported for both N and PMOS transistors (figure V.7). The two degraded wafers are compared to the reference. As for the Vt mismatch, no significant difference are remarked between the three splits.

As it could be observed, no significant impact of the gate roughness for both Vt and β mismatch are pointed out. Two hypotheses have been made to explain these results:



(a) NMOS (b) PMOS

Figure V.4: *Experimental threshold voltage for the reference and the degraded splits.*



(a) NMOS (b) PMOS

Figure V.5: *Experimental $iA_{\Delta Vt}$ on N and PMOS for the reference and the degraded splits.*

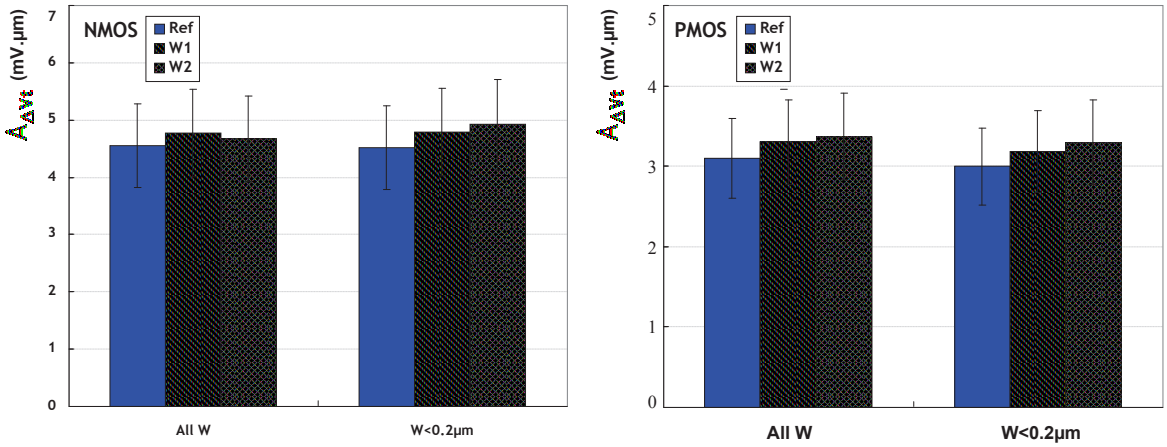
1. Random dopant fluctuations represent more than 70% of the sources of fluctuations for this technology node, while LER represents 9% [Cathignol 08b]. Thus, the impact of LER should be masked by random dopant fluctuations.

2. The gate roughness is not important enough to have significant impact on mismatch.

Reference [Roy 06] is in accordance with the first hypothesis. In that study, Roy et al. analyzed the individual and combined sources of intrinsic parameter fluctuations for technologies beyond 45nm. For the LER, it considers two scenarios:

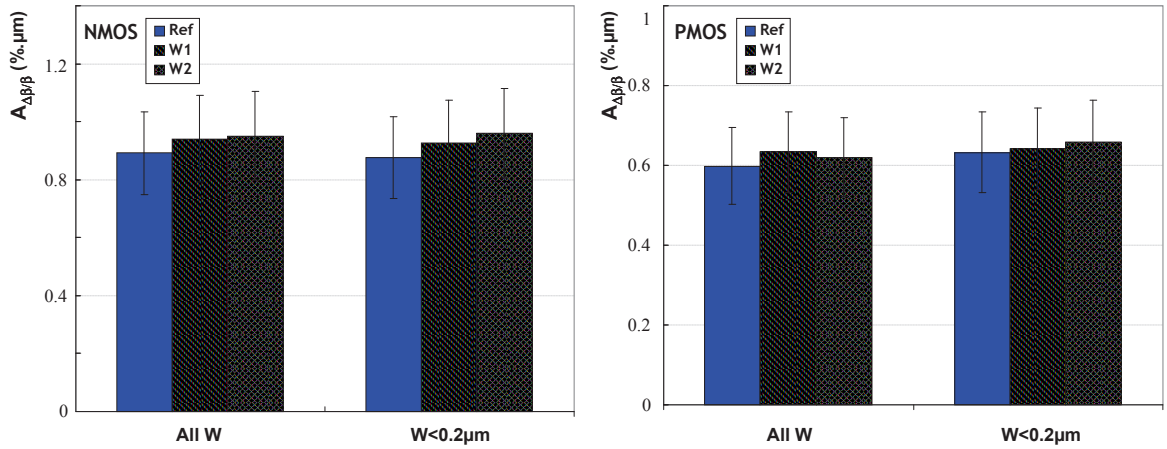
– $LER = 1.2,\ 1,\ 0.75\ and\ 0.5nm$ for the 65-, 45-, 32-, and 22-nm technology nodes, respectively, following the values prescribed by the ITRS 2003.

– LER=4nm, representing the current status of lithography and following the assumption that the scaling of LER will be a very difficult task due to the molecular structure of the photoresist.



(a) NMOS (b) PMOS

Figure V.6: *Experimental $A_{\Delta Vt}$ on N and PMOS transistors for the reference and the degraded splits.*



(a) (b)

Figure V.7: *Experimental gain factor mismatch for the reference and the degraded splits.*

In the first scenario, the LER remains lower than random dopants. In the second one, the LER takes over than random dopants only beyond 22nm channel length. Moreover, in the second chapter it was shown that random dopants is the main source of fluctuations in this 45nm technology and that pocket implants have strong contribution to the mismatch. These effects should mask the impact of LER on mismatch and may explain the results obtained until now. Thus, considering transistors without pocket implants, these are expected to be more sensitive to line edge roughness.

Then, it is proposed to evaluate the level of LER impact in MOS mismatch on current 45nm technology, for transistors with and without pocket implants. In case of a minor impact compared with other fluctuations sources, it will be interesting to evaluate the maximum gate roughness for a minimum impact on the mismatch.

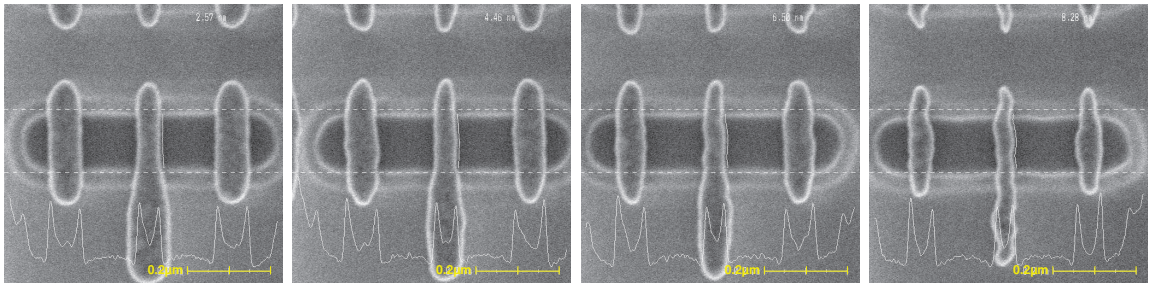
To perform this evaluation, an intentional degradation of the gate roughness is proposed. In previous LER study (section § V.1.2), the gate roughness degradation has been made modifying the resist hardening. Now, to provide different levels of degradations and to have strong line edge roughness another technique is used. In this case, different focus of the photo mask are

used during lithography process.

The degradation will be followed by a monitoring of the LER in the mismatch test structures and measuring the electrical mismatch.

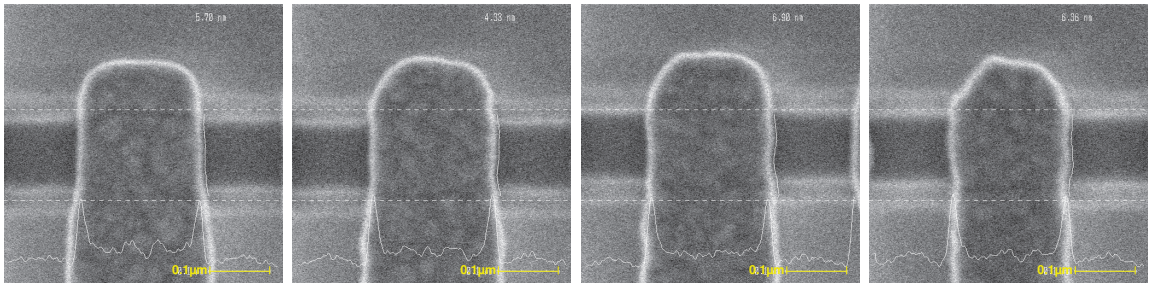
Three electrical wafers are used with four degradation levels of gate roughness. The first level of degradation corresponds to the default process, which is used as reference. For the other three degradations, different focus of the photo mask have been used during lithography process.

The following figures show SEM top views of these degradations for four different geometries: short and narrow (figure V.8), long and narrow (figure V.9), short and wide (figure V.11) and long and wide (figure V.10).



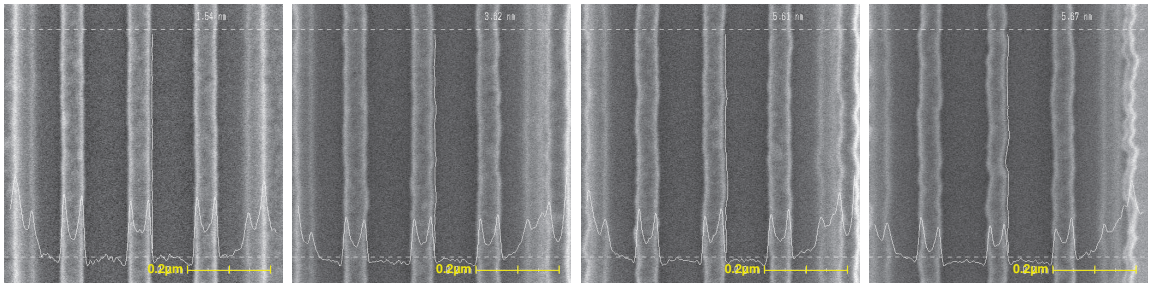
(a) Reference (b) Degradation 1 (c) Degradation 2 (d) Degradation 3

Figure V.8: *SEM top-view for W=0.12µm and L=0.05µm*



(a) Reference (b) Degradation 1 (c) Degradation 2 (d) Degradation 3

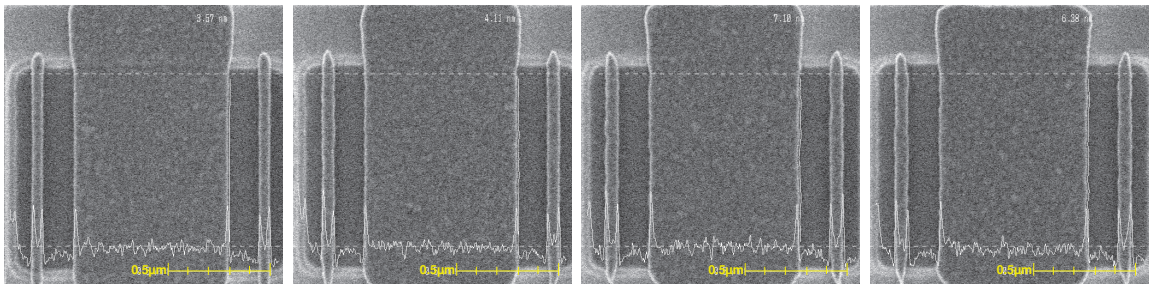
Figure V.9: *SEM top-view for W=0.12µm and L=0.2µm*



(a) Reference (b) Degradation 1 (c) Degradation 2 (d) Degradation 3

Figure V.10: *SEM top-view for W=1µm and L=0.05µm*

These SEM top-views clearly show different levels of gate roughness. Unfortunately, it was not possible to complete this study before the conclusion of this thesis. The next step is the



(a) Reference (b) Degradation 1 (c) Degradation 2 (d) Degradation 3

Figure V.11: *SEM top-view for W=1µm and L=0.75µm*

mismatch electrical characterization and the LER evaluation. Another interesting study to be performed would be to analyze the roughness correlation between the right and the left side of the polysilicon gate.

An experimental investigation of line-edge roughness impact on mismatch has been performed in 45nm technology. No significant impact was observed in this technology, as random dopants fluctuations are predominant and the gate process is well-controlled. The LER is pointed out as a major challenge for technologies beyond 45nm. In addition to LER, there are other sources of fluctuations that are becoming important for mismatch, which are discussed in following sections.

V.2 Evolution of mismatch parameter with miniaturization

The mismatch has been characterized for many years in successive CMOS technologies starting from 0.5μm generation down to a recent 32nm prototype.

The recapitulation of all these experimental results for threshold voltage mismatch as a function of gate oxide thickness t_{ox} is shown in figure A.15 [Mezzomo].

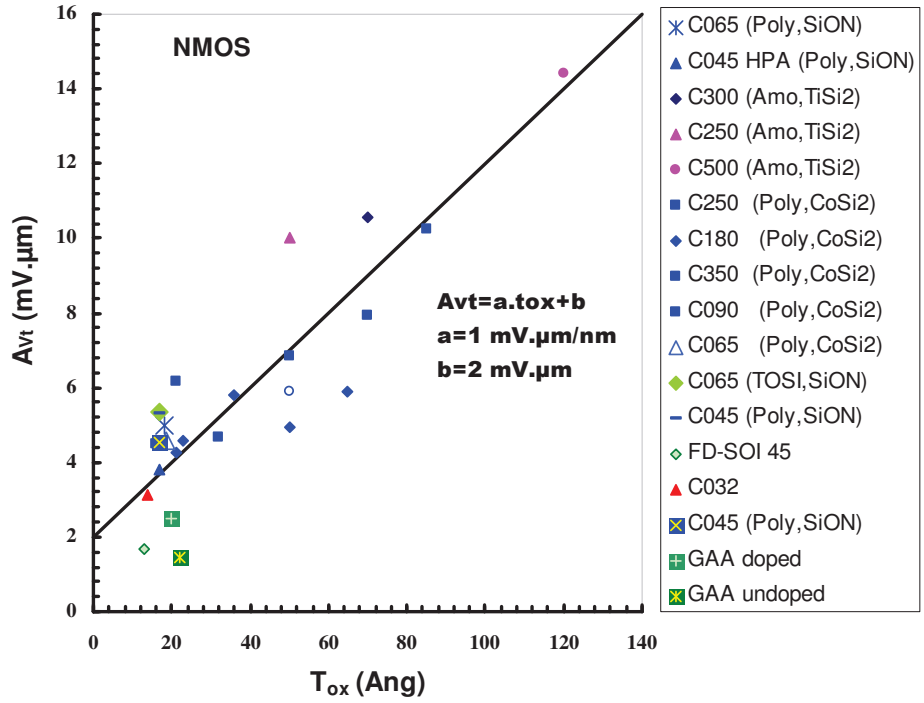
Most of the data presented in figure A.15 comes from bulk devices. Some data are from gate-all-around (GAA) and fully depleted silicon on insulator (FD-SOI) technologies. The data points follows a straight line, described as $A_{Vt} = a.t_{ox} + b$. This result is in agreement with the modeling results and, in particular with equation (A.7) obtained from atomistic simulations [Asenov 00b]:

$$A_{Vt} = 3.2 \times 10^{-3} Na^{0.4} \left(t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{Si}} t_{pol} \right) \tag{V.2}$$

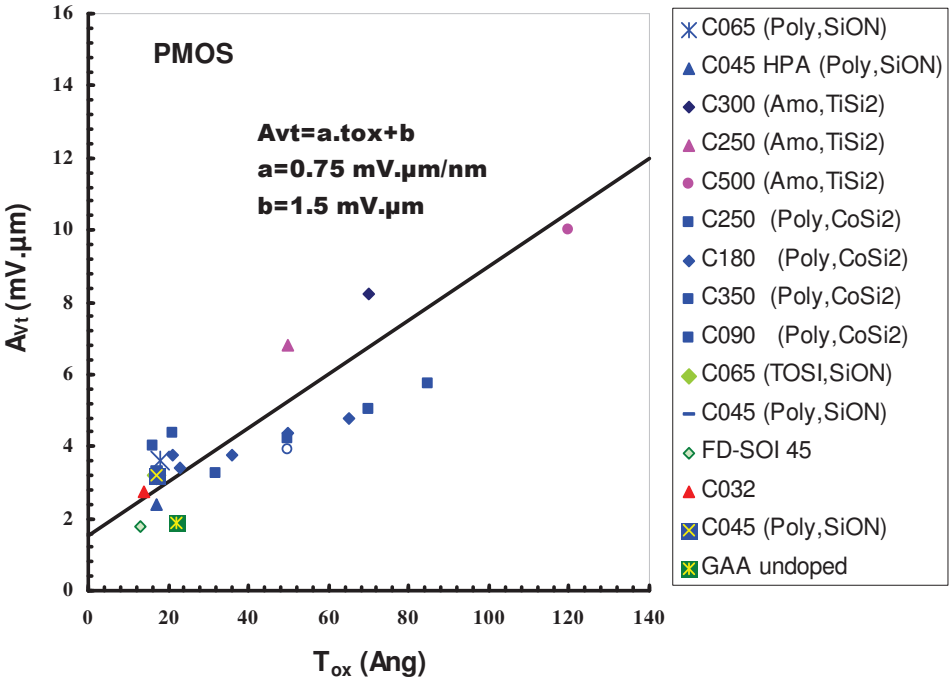
where t_{pol} is the depletion layer width in the polysilicon gate and Na, t_{ox} and t_{pol} being in centimeters, grams and seconds units.

It is found that the slope "a" is about 1mV.μm/nm and 0.75 mV.μm/nm, whereas the intercept "b" is around 2 mV.μm and 1.5 mV.μm, respectively, for NMOS and PMOS. It should also be noticed that the mismatch parameter for GAA and FD-SOI devices is significantly reduced compared to bulk ones [Cathignol 07b]. Note as well the matching improvement for 32nm generation, probably due to the introduction of high-k metal gate. Some experimental mismatch results are presented in the following section.

This feature clearly demonstrates and reinforces that the channel and gate dopant fluctua-



(a) NMOS



(b) PMOS

Figure V.12: *Evolution of threshold voltage mismatch with gate oxide thickness for various technologies nodes, from 0.5µm down to 32nm.*

tions bring an important contribution to mismatch, which allows to foresee strong benefits from undoped channel and metal gate thin film technologies like FD-SOI, double gate (DG) MOS, GAA and FinFETs.

V.3 Trends on innovative technologies

Process variations is among to the most critical challenges for the further scaling of nanoelectronic devices, as highlighted at [ITR 09]. In the tutorial "Nanoelectronics: a tool to face the future" [ESS 10] it is highlighted that "in order to meet the process variations challenges, sources of variability must be identified, their size must be quantified, and their impact on devices, circuits and systems assessed and compared to the specifications of the products in terms of variations or performance".

The proposed solution to continue scaling down is to use materials which have a far higher dielectric constant so that the isolating layer can be much thicker. Thus, foundries are opting to use high-k metal gates. In this case, polysilicon gate is replaced by metal and silicon dioxide gate insulation is replaced by material with higher dielectric constant (figure V.13). The term metal-oxide-silicon (MOS), which was no more adapted when polysilicon was introduced, is now coming back to its right signification.

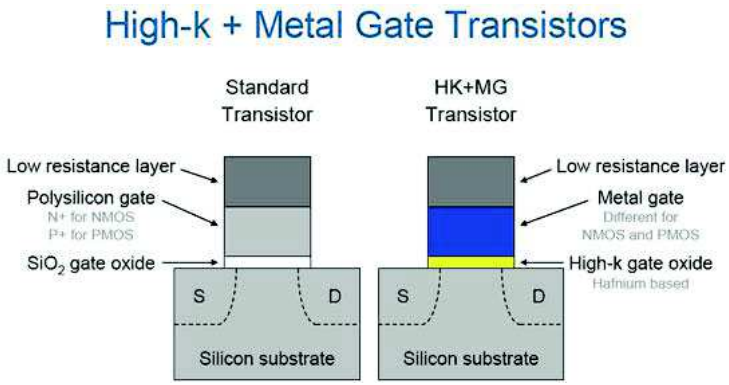
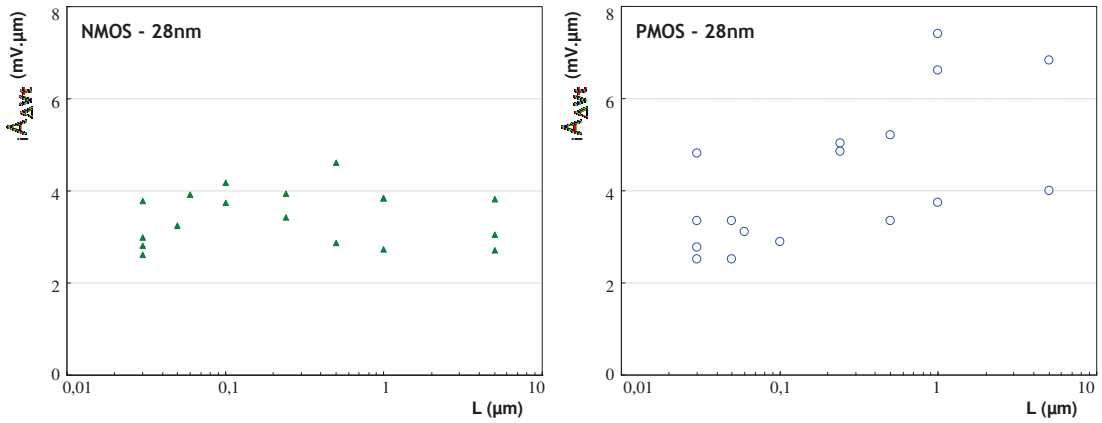


Figure V.13: *Difference between standard polysilicon transistor and high-k/metal gate transistor [Int b].*

Metal gates and high-k dielectric increase the gate field effect and allows use of thicker dielectric layer to reduce gate leakage. Then, using high-k/metal gates combined allows to increase drive current or reduce source-drain leakage; reduce gate oxide leakage; and reduce switching power consumption [Int a]. High-k materials that show promise for replacing the silicon dioxide gate dielectric such as hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2) and titanium dioxide (TiO_2) inherently have a dielectric constant or "k" above 3.9, the "k" of silicon dioxide.

Foundries are starting to process integrated circuits in 32nm and 28nm technologies node. In these technologies, transistors are still produced using Bulk CMOS architectures. An innovation is the introduction of high-k metal gates [Chen 08] [Yang 08] [Diaz 08] [Hook 10]. Their channel are doped and pocket regions near source and drain are still presented. Despite the transistors being doped, the doping level is lower than in 45nm technology node.

Following figure (figure V.14) shows experimental threshold voltage mismatch characterization for 28nm technology, for both N and PMOS transistors.



(a) NMOS (b) PMOS

Figure V.14: *Experimental $iA_{\Delta Vt}$ for 28nm technology on N and PMOS transistors.*

For NMOS transistors, the 28nm technology shows smaller threshold voltage mismatch levels than those of 45nm technology. The $A_{\Delta Vt}$ is around $3.5mV.\mu m$ while in 45nm technology $A_{\Delta Vt}$ is around $4.5mV.\mu m$. The decreases of the mismatch level can be explained by the lower doping of the transistor channel in 32nm technology. In addition, the ratio between pocket and channel doping is also smaller. Consequently, the hump observed in 45nm technology is attenuated for 28nm technology [1], which is in accordance with the model presented in second chapter.

PMOS devices presented the same level of $A_{\Delta Vt}$ of short 28nm NMOS transistors and of 45nm PMOS technology. For long transistors, the $iA_{\Delta Vt}$ is significantly increased, differing from 45nm results, where the mismatch is well-controlled for PMOS transistors. But the 28nm technology is not mature enough to make conclusions and to experimentally identify the physical sources of fluctuations.

Predictions shows that new architectures are needed to continue the transistor miniaturization. Some examples of these architectures are fully depleted silicon-on-insulator (FD-SOI), fin field-effect transistor (FinFET), silicon-on-nothing (SON), double-gate and gate-all-around (GAA). While random dopants are the major source of fluctuations for 45nm technology, other sources of local fluctuations become dominant for these new technologies. Some of these sources of mismatch are: line edge roughness (discussed in previous section), mobility fluctuations and work function fluctuations induced by metal grain orientation differences [Zhang 09] [Dadgour 08] [Brown 10a].

Another trend in the transistor mismatch area is its impact on the transistor reliability [Pae 07] [Rauch 07] [Rauch 02]. The reliability mechanism of negative-bias temperature instability has recently gained a lot of attention due to its increasingly adverse impact on nanometer CMOS technology [Schroder 03]. NBTI is a significant issue in analog circuits since many analog operations require matched device pairs and mismatches induced by NBTI could cause severe circuit failure [Chang 10] [Gielen 08]. Moreover, NBTI degradation introduces threshold voltage drifts in correlation with increased intra-die variability, becoming an important barrier to Static Random Access Memory (SRAM) bitcell scaling [Brown 10b] [Huard 08] [La Rosa 06].

[1] Section §III.3.4 explains why the "hump" is attenuated with a smaller ratio between pocket and channel doping.

V.4 Conclusions Chapter IV

This chapter discussed the perspectives of the mismatch for future technologies. Literature points out that line edge roughness has been shown as one of its major challenges. The impact of edge roughness on mismatch was analyzed for 45nm technology node. The gate roughness was exaggerated by not hardening the gate resist during etching process. Experiments showed no impact of the line edge roughness on the mismatch. The influence of gate roughness on mismatch is masked by random dopant fluctuations, as this source of fluctuations is the major one in the STMicroelectronics 45nm technology. Moreover, the obtained roughness may be not enough to influence the mismatch.

Another analysis of gate roughness in 45nm technology node was proposed. In this case, the gate roughness is induced by different focus of the photo mask, providing various levels of roughness. This will experimentally provide the maximum roughness for a minimum impact on mismatch.

First mismatch characterizations in 28nm technology node was shown. These first results showed better result for the mismatch for NMOS transistors. However, the threshold voltage mismatch is worse for PMOS devices, especially for long lengths.

Finally, literature shows that shrinking transistors require new architectures. This can be observed in the evolution of mismatch parameter with miniaturization. The results demonstrate and reinforce that the channel and gate dopant fluctuations bring an important contribution to mismatch, which allows to foresee strong benefits from undoped channel and metal gate thin film technologies. Along with these, several new sources of fluctuations such as line edge roughness, mobility, work function fluctuations and NBTI are also becoming crucial for the transistor scaling.

Chapter VI

Conclusion

This thesis focused on modeling and characterization of the mismatch on metal-oxide-semiconductor technology field-effect transistors. The research was mostly made in 45nm CMOS STMicroelectronics technology.

The purpose of this thesis was to understand, quantify and reduce the mismatch on CMOS transistors. But to understand the sources of fluctuations, a mature technology is needed. And, if the technology node is mature enough to be manufactured in very large scale, it is difficult to reduce its fluctuations sources. Thus, mismatch should be reduced during the development of a new technology node.

During this thesis, the 45nm technology node was in the end of its development. The 32nm and 28nm technology nodes were starting to be developed by the end of this thesis. Their late appearance proved to be an obstacle to the proposed reduction of the mismatch. In these conditions, this work focused on understanding and quantifying the mismatch for the next node development.

In this thesis, two models were proposed. The characteristics of each model and its main contributions are summarized in the following table.

Modeling		
Pocket mismatch model (Chapter II)	**Characteristics**	
	Source of fluctuations:	Random dopants
	Parameters analyzed:	Vt
	Operation regime:	From weak to strong (linear regime)
	Development:	Based on three-transistors in series
	Main contributions	
	- qualitative and quantitative results, especially for long transistors with pocket-implants - the critical length of a transistor can be obtained - valid for NMOS and PMOS transistors	
Drain-current mismatch model (Chapter III)	**Characteristics**	
	Source of fluctuations:	Generic model. Used here considering random dopants
	Parameters analyzed:	I_D
	Operation regime:	From weak to strong inversion and from linear to saturation regions
	Development:	by considering the impact of a local threshold voltage shift, in a portion of the channel, as in the RTS noise approach
	Main contributions	
	- analyzed as a function of drain-to-source bias - correlated threshold voltage fluctuations and mobility fluctuations due to random doping must be considered to model the experimental results	

An extensive work in characterization was also carried out. The main contributions and topics are listed in the table below.

Characterization	
Effects of pocket co-implants on mismatch (Chapter II)	**Characteristics**
	Source of fluctuations: Random dopants
	Parameters analyzed: Vt, β, I_D
	Main contributions
	- the use of Indium as a co-implant clearly improves matching performance, not only for short transistors, but also for long ones - better results were obtained adding other co-implants such as Carbon and Nitrogen together with Indium - co-implant properties help to reduce the doping level in the channel, improving the transistor matching
Drain-current mismatch as a function of the drain-to-source voltage (Chapter III)	**Characteristics**
	Source of fluctuations: Random dopants
	Parameters analyzed: I_D
	Main contributions
	- characterized for devices with and without pocket-implants - abnormal behavior was observed for long transistors with pocket-implants - the increase of the fluctuations for long transistors is already known for transistor dimensions and gate bias, and is now also observed for drain bias conditions
Effects of line-edge roughness on mismatch (Chapter IV)	**Characteristics**
	Source of fluctuations: Line-edge roughness
	Parameters analyzed: Vt, β
	Roughness degradation: gate roughness was induced by not hardening the gate resin
	Main contributions
	- no impact of the line edge roughness on the mismatch for STMicroelectronics 45nm technology

Another work is related to the improvement of the test structure (Chapter I). In this work, the mismatch parameter extraction using the conventional mismatch test structure was validated. In order to do so, a mismatch test structure based on the Kelvin method was introduced. As a result for the 45nm STMicroelectronics technology, the conventional test structure is found to be adapted for the mismatch study.

Based on the main contributions listed before, it is important to keep in mind that devices with high current can be affected by the external access resistances. The Kelvin mismatch test structure is recommended to be used in these cases.

The use of paired transistors as test structure limits the number of samples for characterization. As mismatch is a statistical study, the results would be more accurate with more samples. An array of transistors should be developed, thus, thousands of transistors could be measured.

For future technologies, factories are still manufacturing transistors with pocket-implants. The first model proposed in this thesis would be useful to predict the mismatch for these technologies. Before applying this model, it is necessary to calibrate some physical parameters. In addition, the transition from heavily-doped (pocket) to weakly-doped (channel) region is abrupt, while in the reality it is smooth. These two points may add errors in this prediction. This model could be used in coming technology nodes since 32nm and also 22nm devices are expected to be built with pocket-implants. This model could also be adapted to include the body bias effects. It will also be interesting to include mobility fluctuation effects.

The proposed drain-current mismatch model was qualitatively analyzed. It would be interesting to analyze it quantitatively. Other important topic which was pointed out is the characterization of drain-current mismatch as a function of drain-to-source bias for long transistors with pocket implants. To treat that case, a new model or an improvement of the existent model is suitable.

It was shown that the mismatch is length-dependent, especially for relatively long transistors

(L>0.1μm). Thus, the proposed models should be integrated in the entire microelectronics chain, helping designers and process engineers to improve circuit performances.

Another research of gate roughness in 45nm technology node was proposed in the last chapter. In this case, the gate roughness is induced by different focus of the photo mask, providing various levels of roughness. This will experimentally provide the maximum roughness for a minimum impact on mismatch. Characterizations should be performed in devices with and without pocket-implants to not mask the results by pocket-implants mismatch effects. Other interesting study to be performed would be to experimentally analyze the roughness correlation between the right and the left side of the polysilicon gate. If the gate-edge lines are proved to be correlated, models should be adapted to include this correlation, rising their complexity. Dedicated test structures with different designed roughness may be an even better solution to observe that correlation.

Literature points out that new transistor architectures are required for further shrinking of the transistors. However, new architectures never come free. Hard work awaits everyone involved in the creation of new transistor generations. As several sources of fluctuations such as line edge roughness, film thickness variation, mobility and work function of metal gates become more and more important, mismatch will become a central topic in microelectronics.

Appendix A

Test of repeatability

This thesis has been based in electrical characterizations. A test of repeatability has been performed to ensure good precision of the measurements.

Repeatability is the variation in measurements taken by a single person or instrument on the same item and under the same conditions. The mismatch characterization may be said repeatable if the repeatability of the standard devition is much smaller than the measured mimatch standard deviation ($\sigma_{\Delta P,rep} \ll \sigma_{\Delta P}$).

Following table A shows that $\sigma_{\Delta Vt,rep}$ represents less than 5% of the $\sigma_{\Delta Vt}$, for various geometries. This table shows the repeatability made in two different dice.

Table A.1: *Test of repeatability*

$W\ (\mu m)$	L (μm)	$\sigma_{\Delta Vt,rep_A}/\sigma_{\Delta Vt}(\%)$	$\sigma_{\Delta Vt,rep_B}/\sigma_{\Delta Vt}(\%)$
0.12	0.04	1.6	3.2
0.12	1	3.2	2.1
0.12	5	3.6	1.5
1	0.04	1.7	4.3
1	5	4.1	4.7
5	5	5.0	4.4

Author publications

Journal

- ⋆ C.M. Mezzomo, A. Bajolet, A. Cathignol, R. DiFrenza, and G. Ghibaudo. “Characterization and modeling of transistor variability in advanced CMOS technologies”. IEEE Transactions on Electron Devices (TED), accepted.

- ⋆ C.M. Mezzomo, A. Bajolet, A. Cathignol, and G. Ghibaudo. “Drain-current variability in 45nm bulk n-MOSFET with and without pocket implants”. Solid-State Electronics (SSE), accepted.

- ⋆ C.M. Mezzomo, A. Bajolet, A.Cathignol, E.Josse, and G. Ghibaudo. “Modeling local electrical fluctuations in 45nm heavily pocket-implanted bulk MOSFET”. Solid-State Electronics (SSE), vol. 54, pp. 1359-1366, 2010.

Conferences

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- ⋆ G. Bidal et al. “Pushing Bulk Transistor with Conventional SiON Gate Oxide for Low Power Applications”. International Conference on Solid State Devices and Materials (SSDM), 2008.

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Résumé en Français

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(Resume in French)

Caractérisation et modélisation des fluctuations aléatoires des paramètres électriques des dispositifs en technologies CMOS avancées

Cette thèse porte sur la modélisation et la caractérisation des différences entre les paramètres électriques de deux ou plusieurs MOSFET dit appariés.

Le manuscrit comporte quatre chapitres:

Le premier chapitre a pour objectif d'expliquer l'importance des fluctuations des paramètres électriques des transistors. Les technologies étudiées, les méthodologies utilisées ainsi que les outils nécessaires à cette étude sont présentés et discutés.

Le deuxième chapitre est dédié à l'influence des fluctuations aléatoires liés au dopage dans les composants MOS. Dans ce chapitre, seul le régime linéaire de fonctionnement est étudié. Cette étude montre que les dopages des poches ont un impact très important notamment pour les transistors longs. Des expériences pour réduire le désappariement en utilisant la co-implantation dans les poches ont été réalisées. Un modèle de désappariement du courant de drain, de la faible à la forte inversion, a été développé permettant d'expliquer qualitativement et quantitativement l'effet des implants de poche sur le désappariement.

Dans le troisième chapitre, le désappariement du courant de drain est analysé en fonction de la tension de drain pour tous les régimes de fonctionnement. D'abord, des transistors sans dopage de poche sont caractérisés et un modèle de désappariement du courant est proposé. Avec ce modèle, l'influence des fluctuations de tension de seuil et de la mobilité des porteurs sur le désappariement a été analysé. Finalement, des caractérisations de désappariement ont aussi été effectuées pour des transistors avec des implants de poche.

Le quatrième et dernier chapitre est focalisé sur le désappariement des facteurs limitants pour les futures technologies. La rugosité de la grille du transistor est analysé pour le noeud technologique 45 nm. Il est également présenté les premiers résultats obtenus du désappariement pour le noeud 28 nm. En outre, les tendances du désappariement sur les technologies futures sont discutées.

Chapitre I : Désappariement du transistor: théorie, modélisation et caractérisation

A chaque développement d'un nouveau noeud technologique, la taille des transistors diminue considérablement. En conséquence, les fluctuations électriques qui apparaissent lors des différentes étapes de fabrication ne sont plus négligeables et influencent de plus en plus les performances électriques des transistors. De ce fait, deux dispositifs supposés strictement identiques ne présentent pas exactement les mêmes performances électriques. Cette fluctuation locale est généralement connue sous le terme de [Lakshmikumar 86] [Pelgrom 89]:

- *Désappariement* : il représente la différence électrique entre deux ou plusieurs transistors.
- *Appariement* : au contraire du désappariement, il montre combien les transistors sont égales.
- *variabilité ou fluctuations locales* : la variabilité ou les fluctuations sont des termes génériques, qui peuvent représenter toute sorte de variation (inter-die, inter-lots, etc.). Le terme *local* est alors utilisé pour indiquer que les conditions extérieures sont les mêmes et aue les variations proviennent des dispositifs.

Le désappariement est en train de devenir un obstacle majeur pour le développement des procédés de fabrication. En effet, ce paramètre est critique pour les performances des circuits intégrés soit du type numérique, comme la SRAM, soit du type analogique (convertisseurs analogique/numérique, miroirs de courants, amplificateurs, etc.), qui consistent en plusieurs paires de transistors [Lakshmikumar 86].

Méthodologie de la caractérisation des fluctuations locales La méthode consiste à mesurer des paires de transistors de différentes géométries, puce à puce. Pour chaque paire de transistors sont mesurés des paramètres électriques "P". Le désappariement est défini comme la différence δP entre les deux dispositifs. Comme le désappariement est une étude statistique, il est nécessaire de caractériser un grand nombre de paires de transistors de différentes géométries. La distribution des résultats obtenus est gaussienne. Un filtre récursif est utilisé pour éliminer les résultats aberrants, c'est-à-dire, les résultats qui proviennent d'erreurs de mesures ou de transistors non fonctionnels. Le filtre utilisé élimine tous les résultats au-dessus et en dessous de trois fois l'écart-type caractérisé ($\pm 3\sigma$). Après filtrage, deux paramètres de désappariement sont estimés : la moyenne m_δ et l'écart type σ_δ [Croon 02a]. Le premier représente des fluctuations, dites systématiques, qui résulte en général d'une incertitude de design. Le deuxième représente des fluctuations locales du procédé de fabrication, dites fluctuations stochastiques. Dans ce contexte, ce travail est focalisé sur les fluctuations stochastiques. Usuellement, le paramètre $A_{\delta P}$ est extrait pour analyser le désappariement. Ce paramètre correspond au coefficient de proportionnalité entre l'écart-type du δP et l'inverse de la racine carré de la surface du canal [Pelgrom 89].

Les paramètres P analysés sont la tension de seuil (Vt), le facteur de courant (β) et le courant de drain (I_D). Vt et β sont extraits par la méthode d'extrapolation de $I_D - V_{GS}$, au maximum de la transconductance. $|V_{GS}|$ varie de 0V jusqu'à 1.1V avec un intervalle de 25mV et $|V_{DS}|$ est constante et égale à 50mV pour la région linéaire ou 1.1V pour la région saturée.

Structure de test Pour la caractérisation des fluctuations locales, une structure de test dédiée est utilisée. Elle est composée de deux transistors identiques du type MOSFET (une paire de transistors), séparés par une distance quasi-minimale fixée par les règles de dessin et placés dans un environnement identique. Les transistors ont le même substrat et différentes interconnexions pour la source, le drain et la grille.

Une des limites de la structure de test présenté est la présence de résistances parasites en série. Ces résistances proviennent des résistances des interconnexions, des contacts, de la source et du drain, dites résistances parasites.

Les résistances parasites provoquent une chute de la tension et la diminution du courant de drain. Pour vérifier si les résistances parasites introduisent des erreurs de caractérisation sur le désappariement, une structure de test est proposée [Mezzomo 09b]. Cette structure de test est basée sur la méthode Kelvin pour la configuration de paire de transistors, représentée sur la figure A.1.

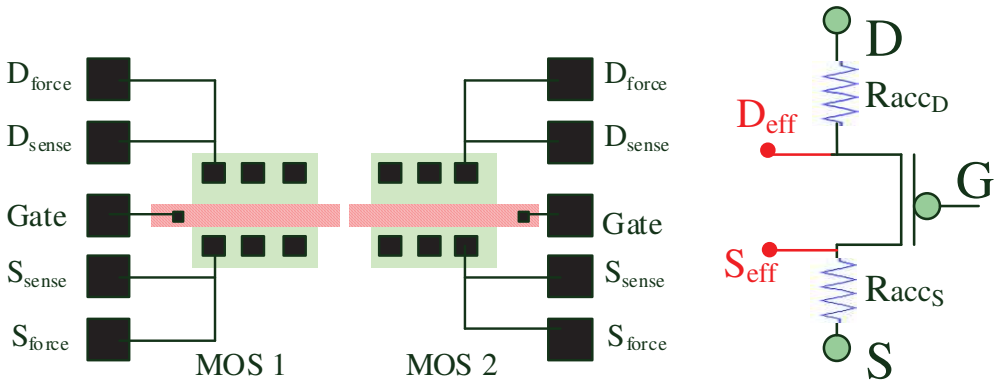


Figure A.1: *Structure de test pour le désappariement en utilisant la méthode Kelvin. (a) Schéma d'un layout montrant les terminals et (b) schéma d'un transistor avec des terminals "force" (D et S) et des terminal de détection (D_{eff} and S_{eff}).*

La différence entre la structure de test pour le désappariement en utilisant Kelvin et la structure conventionnelle est que le drain et la source ont deux connexions appelées de force et de détection. Ces deux terminaux supplémentaires permettent de mesurer la polarisation effective appliquée au dispositif. En outre, un algorithme est utilisé pour corriger la polarisation du transistor, en compensant les baisses de potentiel causées par les résistances parasites.

Pour observer l'impact des résistances d'accès, la structure de test pour le désappariement en utilisant Kelvin est utilisée de trois façons différentes :

- **comme structure de test Kelvin lui-même**

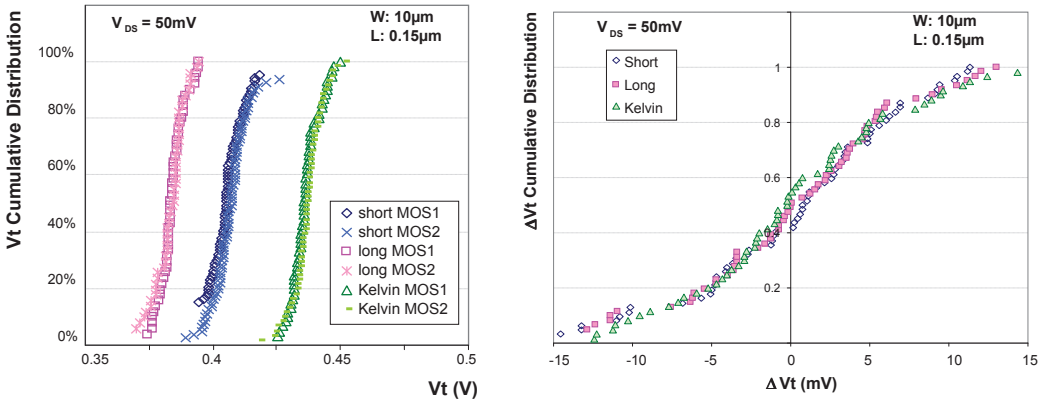
- **comme structure de test classique avec un accès court entre les terminaux source et drain :** la structure de test Kelvin est utilisée comme une structure classique, où seulement les liens les plus courts sont utilisés. Dans ce travail, cette structure de teste s'appelle "*structure de test à accès court*".

- **comme structure de test classique avec un accès long entre les terminaux source et drain :** la structure de test Kelvin est utilisée comme une structure classique, où seulement les liens les plus longs sont utilisés. Dans ce travail, cette structure de teste s'appelle "*structure de test à accès long*".

Pour la suite, l'impact des résistances parasites sur désappariment est évaluée expérimentalement.

Résultats expérimentaux Figure A.2(a) montre les résultats expérimentaux du Vt de la paire de transistors (MOS1 et MOS2) pour les trois structures de test étudiées. Ce graphe montre que les valeurs du Vt ne sont pas les mêmes pour les *accès long*, *accès court* et la structure de désappariement Kelvin. Cela démontre que le Vt est affecté par les résistances d'accès. Bien qu'il y ait des différences de Vt entre les structures de test, il n'est pas sûr que cela aura des effets sur le désappariement.

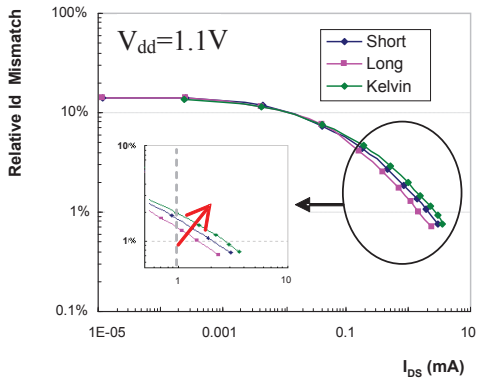
Sur la figure A.2(b), la distribution cumulée du ΔVt est représentée. Bien qu'il y ait un décalage du Vt entre les structures de tests, le désappariement du Vt n'est pas impacté. Il est possible d'observer que les trois courbes du ΔVt correspondant à l'*accès court*, l'*accès long* et la structure Kelvin se superposent. En outre, la distribution cumulée est centrée sur zéro.



(a) NMOS W/L = 10/0.15 (b) NMOS W/L = 10/0.15

Figure A.2: *Distribution cumulée du (a) Vt et du (b) ΔVt de la paire des transistors (MOS1 et MOS2) correspondant à l'accès court, l'accès long et la structure Kelvin.*

Le désappariement du courant de drain $\Delta I_D/I_D$ à V_{DS}= 1.1 V est représenté sur la figure A.3. Plus l'accès au dispositif est résistif, plus le désappariement du courant de drain est sous-estimé lors de l'utilisation de la structure de test classique. Par contre, pour ce noeud technologique 45 nm, les différences entre les trois structures de test ne sont pas significatives.



(a) NMOS W/L = 10/0.15

Figure A.3: *Désappariement du $\Delta I_D/I_D$ en fonction du courant de drain pour l'accès court, l'accès long et la structure Kelvin.*

En conséquence, la structure de test classique est adaptée pour l'étude du désappariement

dans cette technologie. Cependant, pour des applications à haute tension, les résistances parasites ne peuvent plus être ignorées et la structure de test Kelvin est fortement recommandée.

Chapitre II : L'impact des dopants aléatoires sur le désappariement en régime linéaire des transistors avec des implants de poche

Les implants de poches ont une forte influence sur le désappariement des transistors. Une étude d'ingénierie de poche est effectué pour les transistors NMOS dans le but de réduire le niveau des fluctuations, surtout pour les transistors longs. Pour cela, les ingénieurs de STMicroelectronics ont modifié l'architecture du transistor, en faisant l'implantation d'une poche supplémentaire avec l'utilisation de co-implants. Ces implants sont combinés avec différents matériaux, cinq différentes recettes sont utilisées (table A.2).

Table A.2: *Différents implants de poche avec Indium pour l'étude de leurs influences sur le désappariement des transistors NMOS.*

Type d'implant
BF_2 (référence)
BF_2 + In
BF_2 + In + C
BF_2 + In + N
BF_2 + In + C + N

Le désappariement de la tension de seuil est analysée expérimentalement. Considérant toutes les longueurs de transistor, une amélioration de l'appariement à l'aide d'Indium est clairement observée, comme le montre la figure A.4.

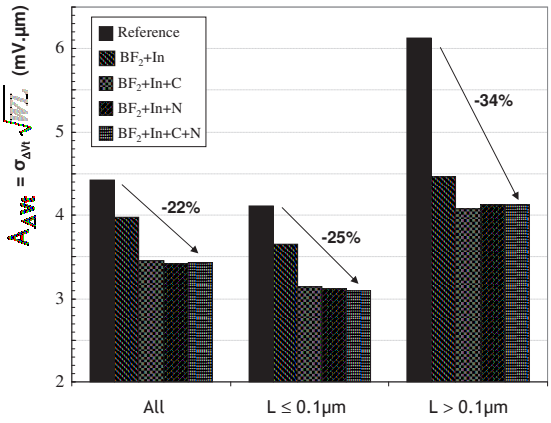


Figure A.4: *$A_{\Delta Vt}$ en considerant toutes les géometries (à gauche), les transistors courts (au centre) et les transistors longs (à droite).*

Quand l'Indium est utilisé, le $A_{\Delta Vt}$ est reduit à $4.0mV.\mu m$. Si l'Indium est combiné avec d'autres matériaux, "$BF_2 + In + C$", "$BF_2 + In + N$" or "$BF_2 + In + C + N$", le niveau du $A_{\Delta Vt}$

est réduit considérablement ($\sim 3.5mV.\mu m$). Ces splits diffèrent d'environ $1.0mV.\mu m$ ($\sim 22\%$) de la référence ($A_{\Delta Vt,ref} \simeq 4.4mV.\mu m$).

Une différence encore plus importante est observée si on considère seulement les transistors longs.

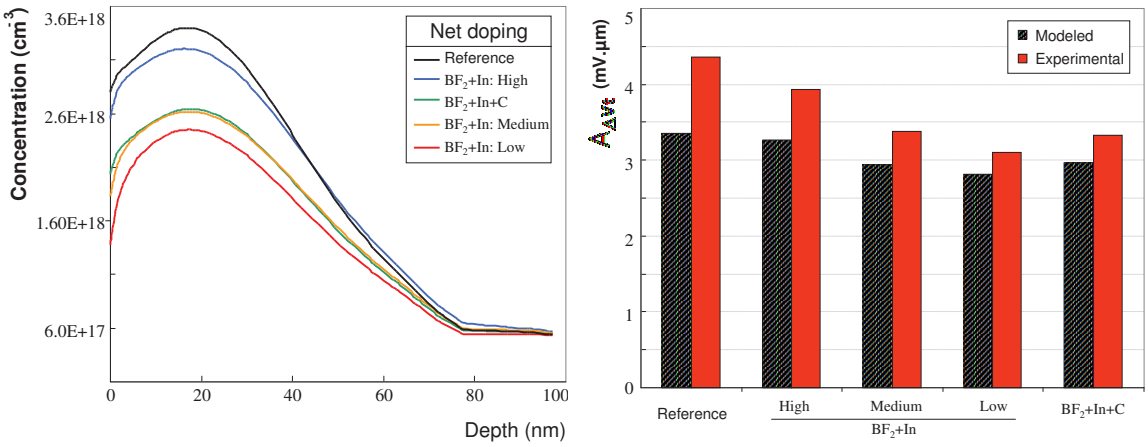
Comme hypothèse, il est suspecté que les co-implants réduisent les dopants aléatoires sur le canal et ainsi, améliorant l'appariement. Pour vérifier si l'amélioration de l'appariement provienne des fluctuations aléatoires des dopants sur le canal, les résultats expérimentaux ont été comparés avec la théorie.

Pour comparer les résultats expérimentaux avec la théorie, les profils de dopants sont extraits par TCAD pour les dispositifs présentés dans le tableau A.3. De plus, comme l'appariement est mieux contrôlé pour les transistors courts, seulement ceux-ci sont analysés.

Table A.3: *Split sheet.*

Type d'implant	Dose/Variation d'énergie
BF_2 (référence)	-
BF_2 + In	Haute Médium Baisse
BF_2 + In + C	-

Les profils de dopants obtenus sont représentés sur la figure A.5(a)



(a) (b)

Figure A.5: *(a)Concentration des dopants pour L=40nm obtenus à partir de simulations TCAD et (b) comparaison $A_{\Delta Vt}$ entre les résultats modélisés et expérimentaux.*

La comparaison des résultats de la modélisation et des résultats expérimentaux est représentée sur la figure A.5(b). Des différences peuvent être observées entre les résultats de la modélisation et expérimentaux. Le $A_{\Delta}Vt$ est calculé en ne considérant que les fluctuations aléatoires des dopants. Les différences qui subsistent devraient être dues à d'autres sources de fluctuations, telles que la granularité du silicium polycristallin, la rugosité de la grille, etc. Ainsi, il n'est pas surprenant que les résultats de la modélisation sous-estiment les valeurs expérimentales.

Cependant, la référence a la plus grande différence entre les résultats de la modélisation

et l'expérimentation. Ces différences peuvent être induites par le modèle appliqué ou d'autres propriétés inconnues des co-implants.

Sur la figure A.5(a), on peut remarquer que la référence a la plus forte concentration de dopage, soit une différence de 33% des splits avec des implants d'Indium et avec une variation moyenne de dose/énergie. L'$A_{\Delta}Vt$ de la référence est également plus élevé, ce qui est cohérent avec le niveau de dopage. La réduction du niveau de dopage peut être expliquée par les propriétés de co-implantation. Par conséquent, l'amélioration des performances pour l'appariement des splits avec d'indium est en partie expliqué par le faible niveau de dopage dans le canal.

Le modèle du désappariement pour des transistors avec des implants de poche

Un nouveau modèle physique pour le désappariement est proposé ici [Mezzomo 10]. Une représentation qualitative est obtenue et le comportement du désappariement est analysé pour différentes longueurs de grille du transistor et aussi pour plusieurs conditions de la tension de la grille. Une caractérisation des paramètres utilisés dans le modèle est également effectuée. La validation du nouveau modèle physique pour le désappariement se fait en comparaison avec les résultats expérimentaux pour les transistors NMOS et PMOS.

Le modèle est basé sur l'approche par séries de trois transistors. Un transistor émule la région de canal (ch), tandis que les deux autres tiennent compte des poches du côté de la source et du drain (pk). Les paramètres liés au canal sont notés P_{ch} et ceux liés à la poche P_{pk}.

Le modèle est défini par l'équation suivante:

$$A_{\Delta Vtcc}(V_{GS}) = \sqrt{\left(\frac{\partial R_{ch}}{\partial V_{GS}} / \frac{\partial R_{tot}}{\partial V_{GS}}\right)^2 \frac{A_{ch}^2 L}{L - 2L_{pk}} + 2\left(\frac{\partial R_{pk}}{\partial V_{GS}} / \frac{\partial R_{tot}}{\partial V_{GS}}\right)^2 \frac{A_{pk}^2 L}{L_{pk}}} \qquad \text{(A.1)}$$

Considérant un transistor avec des implants de poche, la figure A.6 présente les $iA_{\Delta Vtcc}(Vg)$ (axe de gauche) et le ratio des résistances $2R_{pk}/R_{tot}$ (axe de droite) modélisés en fonction de la longueur de grille pour le $V_{GS} = 0.4V$.

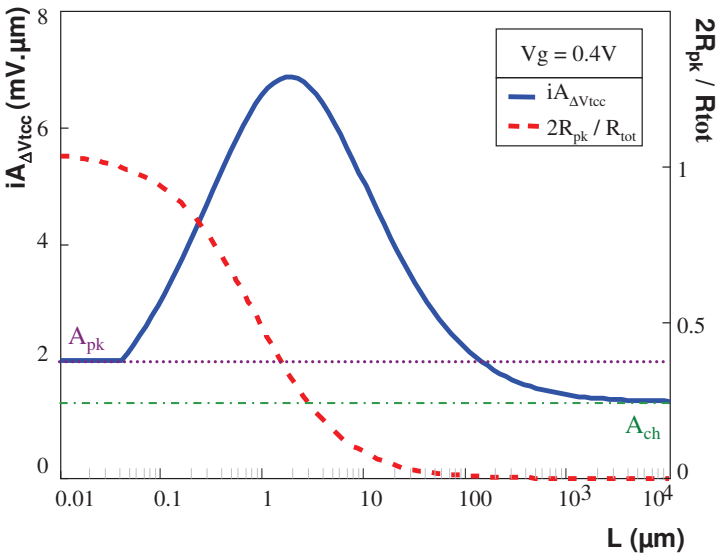


Figure A.6: *Courbe du modèle de désappariement du $iA_{\Delta Vtcc}(V_{GS})$ et ratio des résistances $2R_{pk}/R_{tot}$ pour différentes longueurs de grille avec $V_{GS} = 0.4V$.*

On remarque que pour L<0.1μm, $2R_{pk}/R_{tot} = 1$, i.e., la R_{tot} tend vers $2R_{pk}$. En effet, pour L<0.1μm, les poches sont superposées, et contrôlent ainsi la résistance totale du transistor. Par

conséquent, le $iA_{\Delta Vtcc}(Vg)$ est égal à la valeur du désappariement pour le poche (A_{pk}) pour L=L_{min}=2L_{pk}=40nm.

Avec l'augmentation de L, R_{pk} est constante, tandis que le rapport $2R_{pk}/R_{tot}$ diminue. En effet, pour les transistors relativement longs, L>0.1μm, les poches sont séparées les unes des autres, formant un canal non-homogène (zones des poches + zone canal). Dans ce cas, le poids des résistances de poche est encore dominant et le $\sigma_{\Delta Vtcc}$ se maintient constant, faisant augmenter le $iA_{\Delta Vtcc}(Vg)$.

Le $iA_{\Delta Vtcc}(Vg)$ diminue lorsque le poids de la résistance du canal devient plus important. La longueur correspondant au maximum de $iA_{\Delta Vtcc}(Vg)$ est appelée la longueur critique (L$_{critique}$).

Enfin, le rapport $2R_{pk}/R_{tot}$ tend vers zéro pour un grand L, autrement dit, la R_{tot} est beaucoup plus grande que $2R_{pk}$, puis la R_{ch} devient dominante et la R_{tot} tend vers R_{ch}. Dans ce cas, les zones des poches de la source et du drain sont éloignées, ce qui rend la zone de canal beaucoup plus grande que la zone de poche. Dans ce cas, comme la zone de canal a un dopage faible, le $iA_{\Delta Vtcc}(Vg)$ diminue et tend vers le plateau du désappariement du canal A_{ch}. Il est important de noter que le paramètre de désappariement atteint le plateau A_{ch} pour des longueurs de grille de transistor qui sont trop longues pour être observées dans les structures de la technologie 45nm (L<100μm).

Le modèle est aussi analysé en fonction de la tension de la grille. Considérant un transistor avec des implants de poche, la figure A.7 montre le modèle $iA_{\Delta Vtcc}$ en fonction de V_{GS} pour une longueur de grille fixe L=1μm.

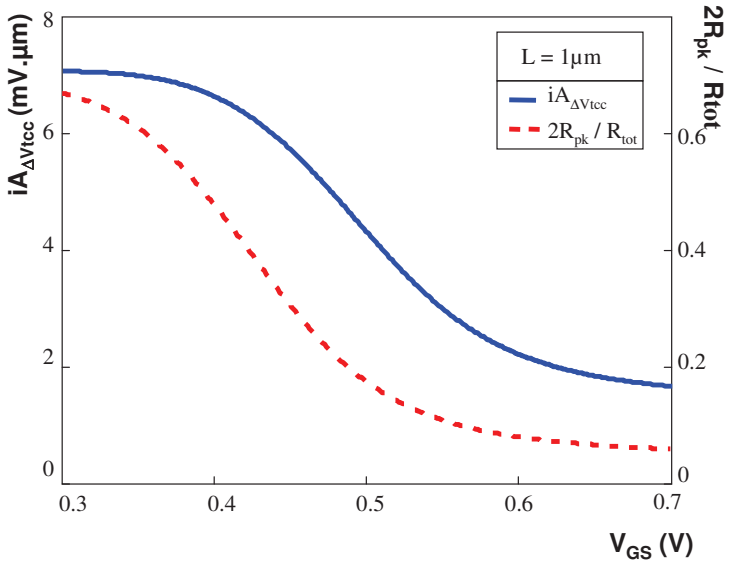


Figure A.7: *Modèle de désappariement du $iA_{\Delta Vtcc}$ et ratio des résistances $2R_{pk}/R_{tot}$ pour divers tensions de grille (L = 1 μm).*

Sur cette figure est également représentée l'évolution du rapport entre la résistance des poches R_{pk} et la résistance totale R_{tot}. Le $iA_{\Delta Vtcc}$ diminue lorsque V_{GS} augmente en accord avec les résultats précédemment obtenus par [Cathignol 09] [Hook 10]. Le comportement du $iA_{\Delta Vtcc}$ peut être expliqué par la relation $2R_{pk}/R_{tot}$. Pour les faibles V_{GS}, le ratio $2R_{pk}/R_{tot}$ tend vers 1, parce que la résistance de poche R_{pk} devient prédominante. A fort V_{GS}, la résistance du canal R_{ch} augmente, réduisant la valeur de $2R_{pk}/R_{tot}$. Ainsi, le désappariement devient similaire à celui d'un transistor sans implants de poche.

Afin de valider le modèle proposé, il est comparé aux données expérimentales.

Pour comparer le modèle avec les résultats expérimentaux, les paramètres suivants sont

nécessaires pour calibrer le modèle : longueur de poche (L_{pk}), capacité de l'oxyde (C_{ox}), mobilité (μ_0), concentration des dopants de la zone des poches (Na_{pk}), concentration des dopants du canal (Na_{ch}), tension de seuil de la zone des poches (Vt_{pk}), tension de seuil du canal (Vt_{ch}), variation de la zone de poche ($\sigma_{Vt_{pk}}$) et variation du canal ($\sigma_{Vt_{ch}}$). Ces deux derniers paramètres dépendent de Vt, qui dépend de Na.

La figure A.8 montre les résultats du désappariement en fonction de la longueur de grille et de plusieurs conditions de polarisation de la grille.

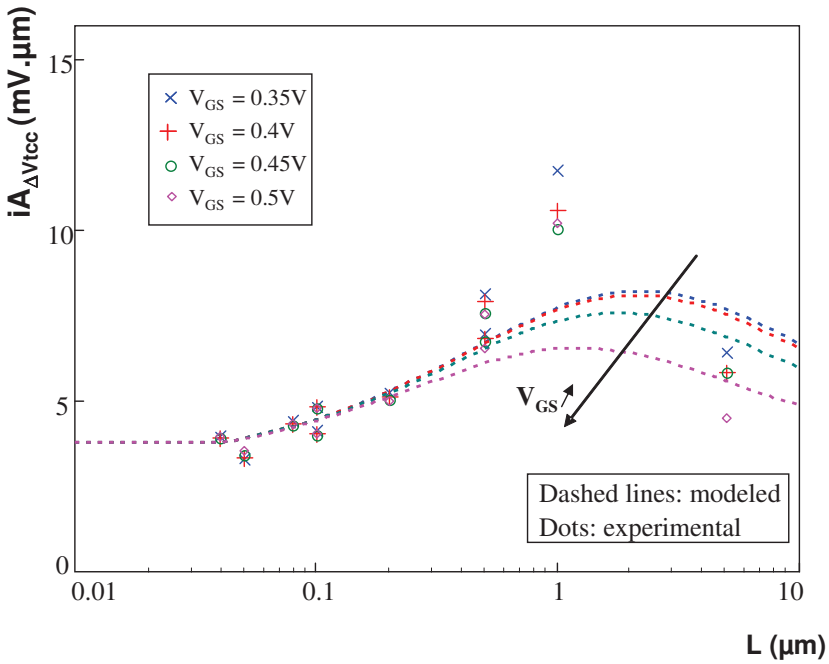


Figure A.8: *Comparaison du désappariement entre le nouveau modèle et les résultats expérimentaux.*

Cette figure montre la bosse et les tendances vers le plateau du A_{pk} pour les petits transistors et vers le plateau du A_{ch} pour les transistors longs et les résultats expérimentaux. La valeur expérimentale du $L_{critique}$ semble être plus faible que dans le modèle. Cette légère différence peut s'expliquer par certaines des hypothèses faites dans ce travail. Le modèle proposé est basé sur l'approche par séries de trois transistors. Par conséquent, le passage de la zone fortement dopée (poche) à la zone faiblement dopée (canal) est brusque, tandis que, dans la réalité, le changement est graduel. Ainsi, certains des paramètres utilisés pour estimer le $L_{critique}$, comme le L_{pk}, peuvent avoir une valeur non exacte. Néanmoins, afin de déterminer expérimentalement la longueur critique, plus de mesures avec des différentes géométries de transistors seraient nécessaires.

La figure A.8 montre également un certain désaccord entre le modèle et la théorie, car le modèle sous-estime les résultats expérimentaux pour des transistors longs. Une des raisons de ces différences est que les méthodes utilisées pour caractériser les paramètres physiques, tel la mobilité, sont assez complexes pour ce noeud technologique. Puis, comme un modèle simplifié est utilisé, les résultats peuvent être légèrement différents de la réalité. En outre, l'$A_{autres\_contributions}$ est considéré comme indépendant de la surface du transistor, pour éviter de faire des hypothèses sur la dépendance a ces sources de fluctuations. Bien que le désappariement des transistors longs ne soit pas parfait, le modèle suit le comportement expérimental du désappariement pour différentes V_{GS} : les courbes se superposent pour de petites longueurs et s'éloignent les unes des autres avec l'augmentation de la longueur de grille.

Les transistors du type NMOS ont fait l'objet de cette étude, car ils ont un fort niveau de désappariement, en particulier pour les transistors longs. Les transistors du type PMOS ont également été modélisés et le modèle est aussi adapté pour ces dispositifs.

Chapitre III: Le désappariement du courant de drain pour tous les régimes de fonctionnement du transistor NMOS

Jusqu'à présent, les analyses sur le désappariement ont été effectuées seulement pour le régime linéaire. Dans ce chapitre, le désappariement du courant de drain est caractérisé du régime linéaire au régime de saturation. Ces caractérisations sont effectuées pour des transistors sans implants de poche et pour des transistors avec des implants de poche. Un modèle général du désappariement du courant de drain, valable pour tous les régimes de fonctionnement, est également présenté. On montre que la corrélation des fluctuations de la mobilité avec les fluctuations de la tension de seuil doit être considérés pour modéliser les résultats expérimentaux qualitativement. Une comparaison entre les transistors avec ou sans implants de poche est effectuée et une amélioration importante de l'appariement du courant de drain dans ce dernier cas est rapportée et discutée.

Pour la conception de circuits, la tension de seuil est souvent un paramètre intéressant. L'écart-type du désappariement de la tension de la grille peut facilement être obtenu en normalisant $\sigma_{\Delta I_D/I_D}$ par g_m/I_D, qui correspond à la densité de courant souhaitée (équation (A.2)).

$$\sigma_{\Delta Vg} = \frac{\sigma\left(\frac{\Delta I_D}{I_D}\right)}{g_m/I_D} \tag{A.2}$$

Le paramètre du désappariement du Vt normalisé obtenu expérimentalement est alors indiqué sur la figure IV.3.

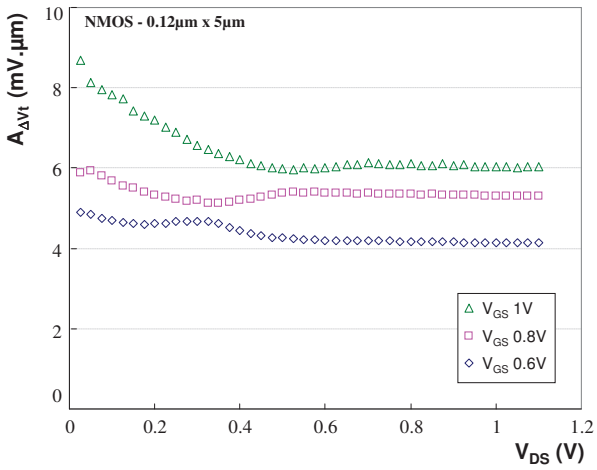


Figure A.9: *Désappariement du courant de drain normalisé en fonction de la tension du drain avec V_{GS} = [0.6, 0.8 and 1]V.*

Une dépendance importante à faible V_D est observée, en particulier pour une forte tension de grille. Un modèle est alors proposé pour couvrir ce cas et est discuté dans la section suivante.

Un modéle général du désappariement du courant de drain a été développé en considérant l'impact d'une variation locale de la tension de seuil δVt en une portion du canal de surface δa, comme sur l'approche RTS pour le bruit [dit Buisson 92].

Dans cette approche, le courant de drain relatif varie en raison d'une faible variation locale de la conductivité $\delta\sigma$ (equation (A.3)):

$$\frac{\Delta I_D}{I_D} = \frac{\delta\sigma}{\sigma}\frac{\delta a}{a} = \frac{1}{\sigma}\frac{\partial\sigma}{\partial Vt}\frac{\delta a}{a}\delta Vt \tag{A.3}$$

où "a" est la surface du canal du transistor.

L'écart-type peut être exprimé par l'équation (A.4):

$$\sigma^2_{\frac{\Delta I_D}{I_D}} = \left(\frac{1}{\sigma}\frac{\partial\sigma}{\partial Vt}\right)^2 A^2_{\delta Vt}\frac{\delta a}{a^2} \tag{A.4}$$

En intégrant ces fluctuations sur la surface du canal, on a (equation (A.5)):

$$\sigma^2_{\frac{\Delta I_D}{I_D}} = \iint_0^{WL}\left(\frac{1}{\sigma}\frac{\partial\sigma}{\partial Vt}\right)^2 \frac{A^2_{\delta Vt}}{a^2}\,dx\,dy \tag{A.5}$$

Considérant la conservation du courant au long du canal, avec $\sigma = \mu_{eff}Q_{inv}$, l'écart-type du courant de drain est égal à (equation (A.6)),

$$\sigma^2_{\frac{\Delta I_D}{I_D}} = \frac{\int_0^{V_{DS}}\left(\frac{\partial ln(\mu_{eff}Q_{inv})}{\partial Vt}\right)^2 \frac{A^2_{\delta Vt}}{WL}\mu_{eff}Q_{inv}\,dUc}{\int_0^{V_{DS}}\mu_{eff}Q_{inv}\,dUc} \tag{A.6}$$

Ce modèle du désappariement du courant de drain est analysé en considérant trois conditions différentes. Les fluctuations de la tension de seuil (δVt) induites par les fluctuations aléatoires des dopants sont prises en compte pour les trois cas. En terme de mobilité, le premier cas considère une mobilité effective constante. Pour les deux autres cas, la mobilité dépendant du champ électrique est considérée. Dans le dernier cas, étant donné que les fluctuations de la mobilité et du Vt sont générées par la même source (les fluctuations aléatoires du dopage), elles sont naturellement corrélées. Ainsi, cette corrélation est également prise en compte dans le dernier cas. Ces trois cas sont résumés dans le tableau suivant (tableau A.4):

Table A.4: *Plusieurs conditions utilisées dans le modèle du désappariement du courant de drain.*

Cas	Fluctuations	Mobilité	Niveau de Fermi
$\delta Vt + \mu_{eff} = const$	$\delta Vt(Na)$	μ_{eff}	Variable
$\delta Vt + \mu_{eff}(E_{eff})$	$\delta Vt(Na)$	$\mu_{eff}(E_{eff})$	Variable
$\delta Vt + \delta\mu_{eff}(E_{eff})$	corrélé $\delta Vt(Na)$ et $\delta\mu(Na)$	$\mu_{eff}(E_{eff})$	Variable

La figure (fig. A.10) suivante montre le $A_{\Delta_{Vg}}$ en fonction de la tension du drain.

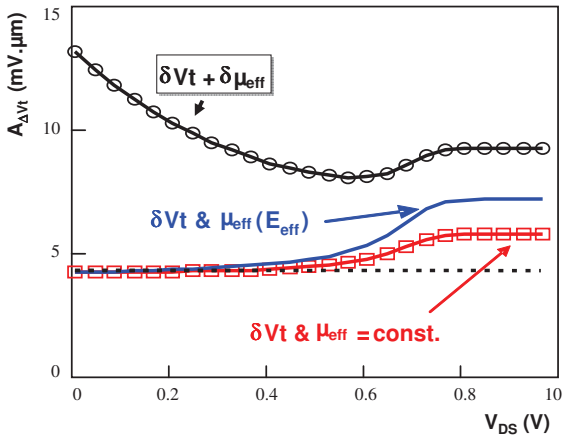


Figure A.10: *Modèle du désappariement du courant de drain (a) en fonction de la tension du drain pour différentes conditions de la mobilité à* $V_{GS} = 1.2V$

Si le premier cas est considéré ($\delta Vt + \mu_{eff} = const$), l'$A_{\Delta_{Vg}}$ augmente à fort V_{DS}, parce que le champ électrique vertical varie. Pour le second cas ($\delta Vt + \mu_{eff}(E_{eff})$), un décalage est observé à fort V_{DS} en raison de la dépendance du champ électrique effectif. Enfin, considérant la corrélation des fluctuations de la mobilité et du Vt, une forte dépendance à faible V_{DS} est observée. Seuls les cas où cette corrélation est considérée permettent de représenter les résultats expérimentaux, montrés précédemment sur la figure A.9.

L'impact du désappariement du courant de drain en fonction de la tension de drain pour les transistors avec des implants de poche n'a pas encore été observé.

Une comparaison des résultats expérimentaux obtenus pour les transistors avec et sans implants de poche est illustrée sur la figure A.11.

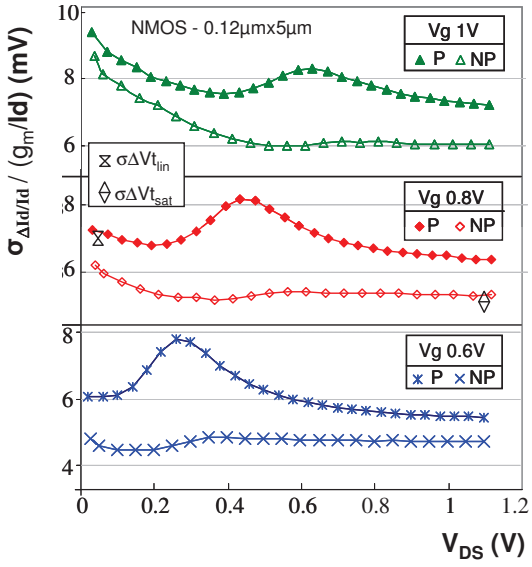


Figure A.11: *Le désappariement du courant de drain convertis en fluctuations de la tension de la grille en fonction du* V_D *à* V_{GS}*=[0.6, 0.8, 1]V pour les transistors avec et sans implants de poche.*

Un comportement anormal a été observé pour les transistors longs avec implants de poche

et n'est pas expliqué par le modèle proposé précédemment, valable seulement pour un canal uniforme [Mezzomo 10]. Les fluctuations de courant de drain augmentent lorsque le transistor varie du régime linéaire au régime de saturation. L'augmentation des fluctuations est déjà connue en fonction des dimensions du transistor et de la polarisation de la grille et elle est maintenant aussi observée en fonction de la polarisation du drain.

Chapitre IV: Perspectives pour le désappariement des transistors

Des études sur le désappariement ont été effectuées dans les chapitres précédents pour la technologie 45nm bulk MOSFET, en se focalisant sur les fluctuations aléatoires des dopants. Au-delà du noeud technologique 45 nm, la rugosité de bord de ligne de la grille est soulignée dans la littérature comme l'un des principaux facteurs limitants. On propose d'évaluer la rugosité maximale que la grille peut avoir pour que le dispositif reste non affecté par le désappariement de cette rugosité. En outre, pour réduire les dimensions du transistor au-delà de 45 nm, la littérature montre que des nouvelles architectures de transistors sont nécessaires. Les tendances sur les technologies innovantes sont ensuite discutées et des caractérisations obtenues pour 28 nm sont présentées.

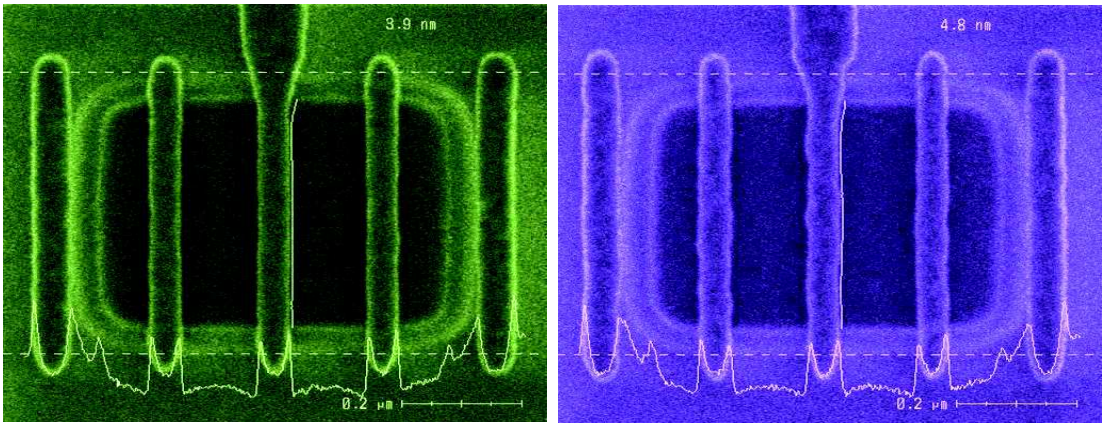
L'impact de la rugosité de la grille sur le désappariement pour la technologie 45 nm et au-delà

La rugosité du bord de ligne et de la largeur de ligne (LER et LWR respectivement) sont considérées comme les principaux facteurs limitants de la technologie future [ITR 09]. Ils ont causé peu de soucis dans le passé puisque les dimensions critiques du transistor étaient beaucoup plus grandes que sa rugosité. La miniaturisation des composants a permis la fabrication des dispositifs avec des dimensions à l'échelle nanométrique [Harriott 01]. Par contre, LER n'a pas été réduite dans les mêmes proportions, et représentent une grande proportion de la longueur de grille [Asenov 03]. Dans cette section, le désappariement de la rugosité de grille du transistor est analysé expérimentalement sur des transistors N- et P-MOS, sur la technologie 45 nm.

Une des procédures utilisées pour faire des bords de grille en polysilicium bien droit est le durcissement de la résine utilisée pour former la grille par un plasma HBr pendant le procédé de gravure [Martin 08] [Pargon 09]. Pour faire la dégradation de la rugosité de la grille, la résine n'a pas été durcie. Ainsi, la résine doit présenter des déformations et donc une rugosité plus forte de la grille.

Pour cette étude, trois plaques ont été traitées [Babaud 10]. Une plaque a reçu le procédé de référence, y compris l'étape de durcissement de la résine. Pour les deux autres, la grille des transistors en silicium polycristallin a été dégradée. Sur ces deux plaques, la résine n'a pas été durcie, dégradant la rugosité de grille. Les résultats de cette dégradation sont présentés sur la figure A.12.

Scanning Electron Microscopy (SEM) a été utilisé pour mesurer la rugosité de la grille, en utilisant une recette spécifique. Par contre, cette recette sur la structure de test dédié pour le désappariement n'a pas été efficace pour mesurer la rugosité, vu que ces structures ont des



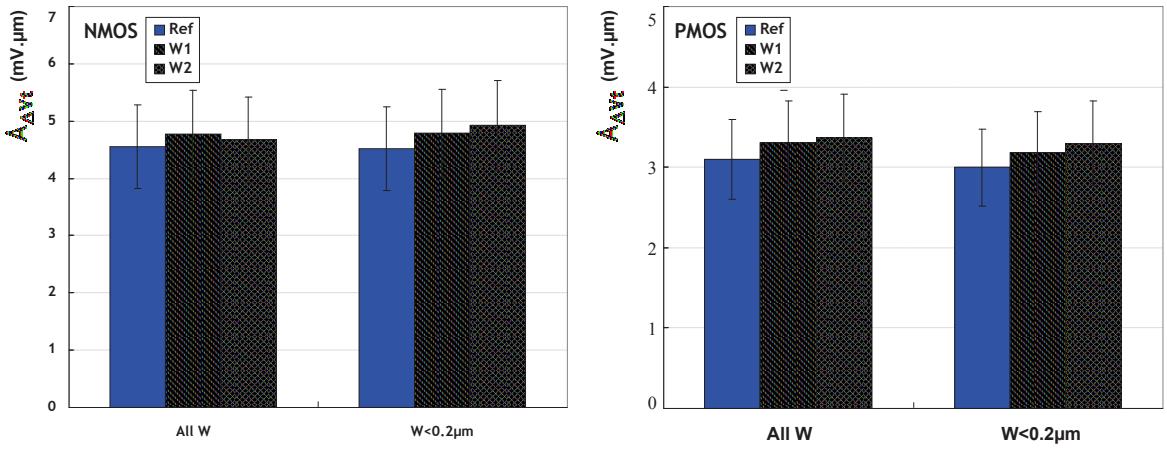
(a) Reference (b) Degraded sample

Figure A.12: *Vue de dessus d'une structure de test du désappariement avec la grille en silicium polycristallin entourée par de poly-dummies.*

dimensions trop petites. La rugosité de la grille a ensuite été mesurée dans une structure de test dédiée pour contrôler les dimensions du transistor. La LER mesurée pour la référence est de 3.6nm tandis que, pour les plaquettes dégradées, elle est de 4.6nm, montrant une variation autour de 28% (1nm). Bien qu'il n'ait pas été possible de mesurer directement sur les structures de test dédiées pour le désappariement, les photos SEM montrent que l'élimination du durcissement de la résine induit des dégradations visibles de la rugosité de la grille sur ces structures.

Les résultats expérimentaux sont présentés et discutés dans la section suivante.

Puisque le désappariement dû à la LER a plus d'impact sur les transistors étroits, la figure A.13 montre le $A_{\Delta Vt}$ pour des transistors étroits de la plaque de référence et celles dégradées. Sur la gauche de chaque graphe, toutes les largeurs de grille sont représentées. A droite, uniquement les géométries avec des largeurs de grille inférieure à 0.2μm sont considérées. Aucune différence importante n'est constatée entre les trois plaques, même pour les transistors les plus étroits.

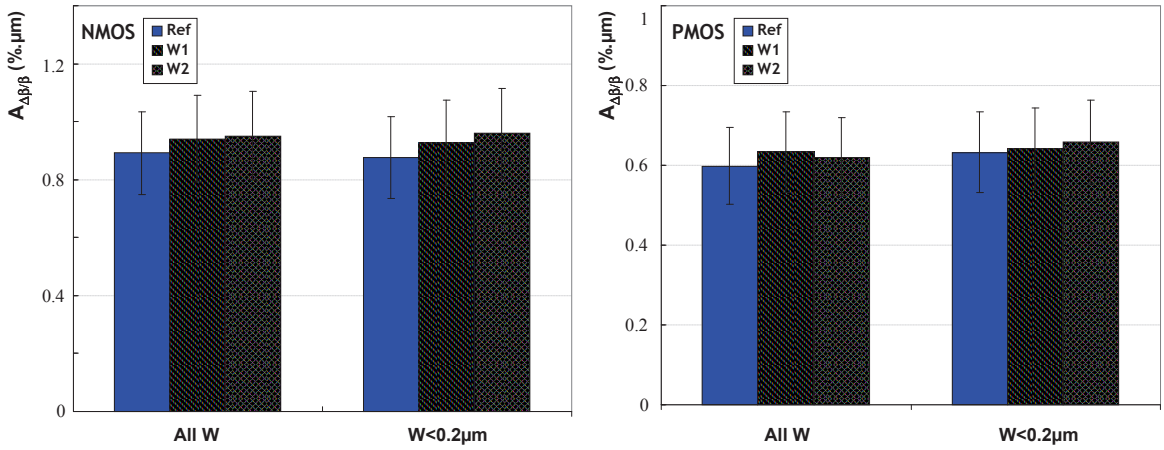


(a) NMOS (b) PMOS

Figure A.13: *L'$A_{\Delta Vt}$ expérimental sur des transistors du type N- et P-MOS pour la plaque de référence et les plaques dégradées.*

Le désappariement du facteur de gain est également indiqué pour les transistors du type N et PMOS (figure A.14). Les deux plaques dégradées sont comparées à celle de référence. Par

rapport au désappariement du Vt, aucune différence significative entre les trois plaques n'est observée.



(a) (b)

Figure A.14: *Le désappariement du facteur de courant pour la plaque de référence et celles dégradées.*

Comme on a pu l'observer, aucun impact significatif de la rugosité de grille pour le désappariement du Vt et du β n'est observé. Deux hypothèses ont été faites pour expliquer ces résultats:

1. Les fluctuations aléatoires des dopant représentent plus de 70% des sources de fluctuations pour ce noeud technologique, alors que les fluctuations de la rugosité de la grille représente 9% [Cathignol 08b]. Ainsi, l'impact du LER devrait être masqué par des fluctuations aléatoires des dopant.

2. La rugosité de la grille n'est pas assez importante pour avoir un impact significatif sur le désappariement.

La référence [Roy 06] est en accord avec la première hyphothèse.

En outre, dans le deuxième chapitre, on a montré que les dopants aléatoires sont la principale source des fluctuations de cette technologie 45nm et que les implants de poche ont une forte contribution sur le désappariement. Ces effets peuvent masquer l'impact de la rugosité de la grille sur le désappariement et peuvent expliquer les résultats obtenus jusqu'à présent. Ainsi, si on prend en compte des transistors sans implants de poche, on s'attend à être plus sensible à la rugosité de la grille.

Ensuite, il est proposé d'évaluer le niveau de l'impact du LER sur le désappariement, sur la technologie 45nm, pour des transistors avec et sans implants de poche. Dans le cas d'un impact mineur par rapport à d'autres sources de fluctuations, il sera intéressant d'évaluer la rugosité grille maximale pour un impact minimal sur le désappariement.

Pour effectuer cette évaluation, une dégradation intentionnelle de la rugosité de grille est proposée. Dans l'étude précédente (section § V.1.2), la dégradation de la rugosité de grille a été faite en modifiant le durcissement de la résine. Maintenant, pour fournir différents niveaux de dégradations et d'avoir une forte rugosité de la grille, une autre technique est utilisée. Dans ce cas, différent focus sur le masque sont utilisés pendant le procédé de la photolithographie.

La dégradation sera suivie par un monitoration de la rugosité de la grille sur les structures de test dédiées et des mesures du désappariement.

Trois plaques électriques sont utilisées avec quatre niveaux de dégradation de la rugosité de grille. Le premier niveau de dégradation correspond au processus par défaut, qui est utilisé comme référence. Pour les trois autres dégradations, différente focus ont été utilisés pendant le procedé de photolithographie.

Ces photos SEM montrent clairement les différents niveaux de la rugosité de la grille. Malheureusement, il n'a pas été possible de terminer cette étude avant la conclusion de cette thèse. La prochaine étape sera la caractérisation électrique du désappariement et l'évaluation du LER. Une autre étude intéressante à réaliser serait d'analyser la corrélation entre la rugosité de la ligne droite et de la ligne gauche de la grille en polysilicium.

Dans cette partie, une étude expérimentale de l'impact de la rugosité de la grille sur le désappariement a été réalisée sur la technologie 45nm. Aucun impact significatif n'a été observé dans cette technologie, car les fluctuations aléatoires des dopants sont prédominantes et le procédé de la grille est bien contrôlée. Le LER est souligné comme un défi majeur pour les technologies au-delà de 45 nm. En plus de la rugosité de la grille, il existe d'autres sources de fluctuations qui sont de plus en plus importantes pour le désappariement. L'évolution du désappariement avec la technolgie est discuté dans la section suivante.

L'évolution du désappariement avec la technologie

Le désappariement a été caractérisé pendant plusieurs années pour les technologies CMOS successives à partir de la génération 0.5μm jusqu'à un récent prototype 32nm.

La récapitulation de tous ces résultats expérimentaux du désappariement de la tension de seuil en fonction de l'épaisseur d'oxyde de grille est représentée sur la figure A.15 [Mezzomo].

La plupart des données présentées dans la figure A.15 vient de Bulk CMOS. Certaines données proviennent des technologies *gate-all-around* (GAA) et *fully depleted silicon on insulator* (FD-SOI).

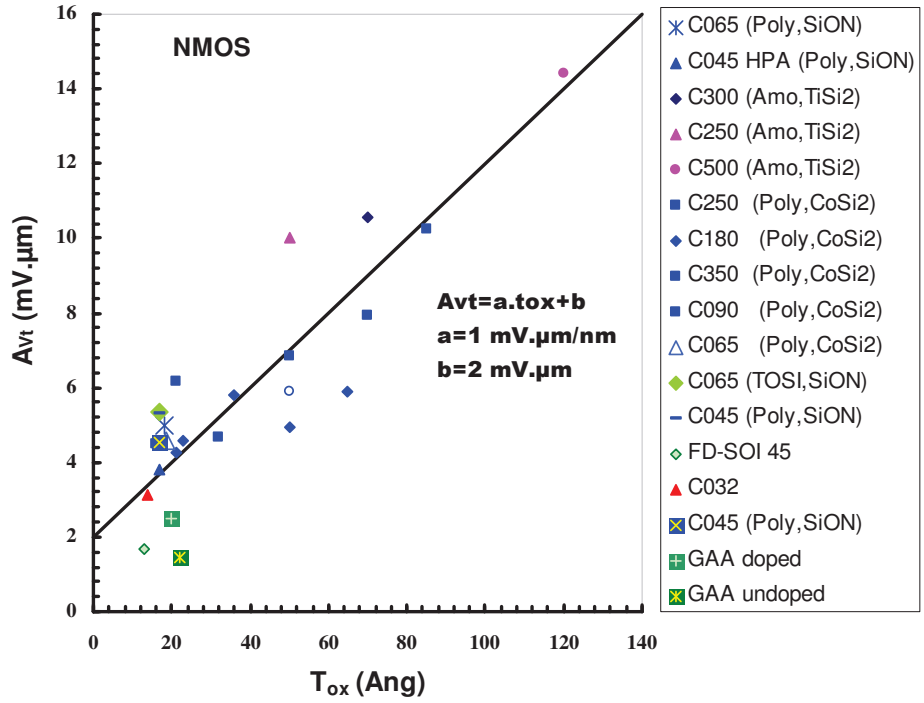
Les données suivent une ligne droite, décrit comme $A_{Vt} = a.t_{ox} + b$. Ce résultat est en accord avec les résultats de la modélisation et, en particulier avec l'équation (A.7) obtenus à partir de simulations atomistiques [Asenov 00b]:

$$A_{Vt} = 3.2 \times 10^{-3} Na^{0.4} \left(t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{Si}} t_{pol} \right) \tag{A.7}$$

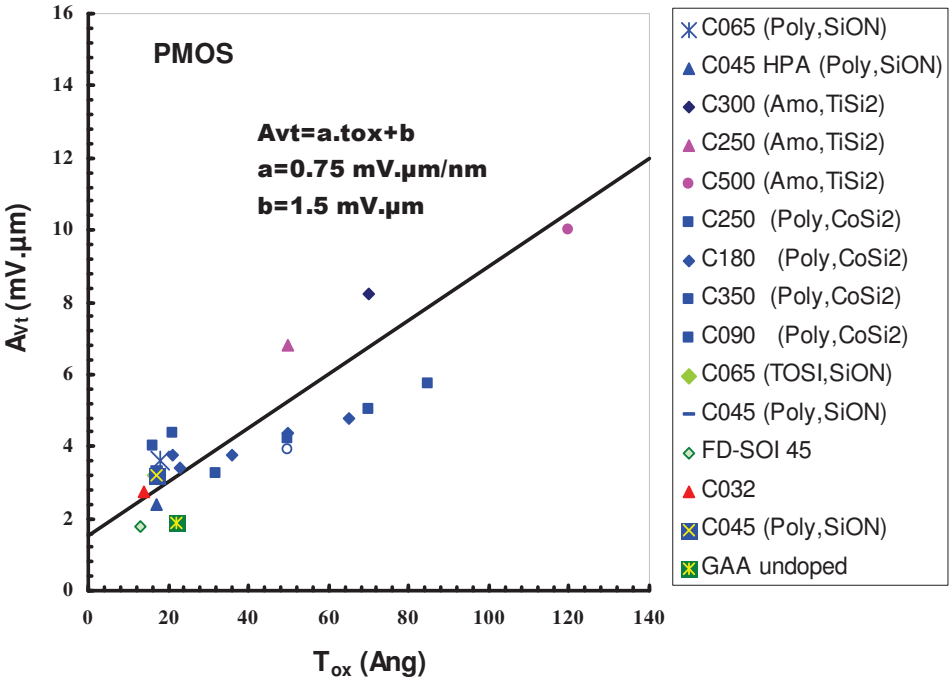
où t_{pol} est la largeur de dépletion de la grille de polysilicium et Na, t_{ox} et t_{pol} étant respectivement en centimètres, grammes et secondes.

On trouve que la pente "a" est d'environ 1mV.μm/nm et de 0.75 mV.μm/nm, alors que l'interception "b" est d'environ 2 mV.μm et de 1.5 mV.μm, respectivement pour les NMOS et PMOS. Il est également intéressant de noter que le paramètre de désappariement des dispositifs GAA et FD-SOI est nettement réduit par rapport à ceux en bulk [Cathignol 07b]. Il faut aussi noter l'amélioration de l'appariement pour la génération 32nm, probablement due à l'introduction de grille métallique high-k.

Cette fonction démontre clairement et renforce l'idée que le canal et les fluctuations des dopants apportent une contribution importante au désapariemment, ce qui permet de prévoir des avantages importants du canal non dopé et de grille métalique à film mince comme FD-SOI, double grille (DG) MOS, GAA et FinFET .



(a) NMOS



(b) PMOS

Figure A.15: *Evolution du désappariement de la tension de seuil en fonction de l'épaisseur d'oxide de grille pour plusieurs noeuds technologiques, de 0.5µm jusqu'à 32nm.*

Conclusion

Cette thèse porte sur la modélisation et la caractérisation du désappariement des transistors métal-oxyde-semiconducteur à effet de champ (MOSFET). La recherche a été réalisée principalement sur la technologie CMOS 45nm de STMicroelectronics.

L'utilisation des paires des transistors comme structure de teste limite le nombre d'échantillons pour la caractérisation. Comme le désappariement est une étude statistique, les résultats sont plus précis avec plus d'échantillons. Un réseau de transistors doit être développé, des milliers de transistors peuvent ainsi être mesurés.

Pour les prochaines technologies, les entreprises continuent à devélopper des transistors avec des implants de poche. Le premier modèle proposé dans cette thèse est utile pour pouvoir prédire le désappariement des transistors. Avant d'appliquer ce modèle, il est nécessaire de calibrer certains paramètres physiques. Le modèle considère la transition de la zone fortement dopée (poches) à la zone faiblement dopée (canal) comme étant abrupte, tandis que dans la réalité, cette transistion se fait de manière graduelle. Ces deux points peuvent ajouter des erreurs dans la prédiction du désappariement. Ce modèle peut être utilisé dans les noeuds technologiques à venir, comme le 32nm et le 22nm, mais aussi pour étudier des effets sur des technologies déjà matures, vu que toutes ces technologies sont/seront développés avec des implants des poches.

Le modèle proposé sur le désappariement du courant de drain a été analysé de manière qualitative. Il serait intéressant de l'analyser quantitativement. Un autre sujet important qui a été souligné est la caractérisation du désappariement du courant de drain en fonction de la tension Vds pour les transistor longs avec des implants de poche. Pour traiter ce cas, il est possible de faire une adaptation du modèle proposé.

Il a été montré que le désappariement est dépendant de la longueur, en particulier pour les transistors relativement longs (L>0.1μm). Ainsi, les modèles proposés devraient être intégrés dans toute la chaîne de la microélectronique, pour aider les concepteurs et les ingénieurs des procédés a améliorer les performances des circuits.

Le dernier chapitre propose une étude de la rugosité de la grille dans le noeud technologique 45 nm. La rugosité de la grille a été dégradé par différents focus du masque pendant l'étape de photolithographie, en ayant comme résultat différents niveaux de rugosité. Le résultat expérimental permet de connaitre la rugosité maximale que les transistors peuvent avoir pour qu'ils aient un minimum de désappariement. Les caractérisations doivent être faites sur des dispositifs avec et sans implants de poche pour ne pas masquer les résultats par des effets de désappariement des implants de poche. Une autre étude intéressante à effectuer serait d'analyser expérimentalement la corrélation entre la rugosité du côté droite et du côté gauche de la grille de polysilicium. Si les rugosités des lignes de la grille sont corrélées, les modèles doivent être adaptés pour inclure cette corrélation. Des structures de test dédiées, en faisant la rugosité de grille en design, peuvent être une solution encore meilleure pour observer cette corrélation.

La littérature souligne que de nouvelles architectures seront nécessaires pour réduire la taille des transistors. Cependant, des nouvelles architectures ne sont jamais gratuites. Comme

plusieurs sources de fluctuations telles que la rugosité, l'épaisseur du film, la mobilité et la fonction de travail de sortie des grilles métalliques deviennent de plus en plus importantes, le désappariement sera un point critique pour le développement des nouvelles technologies.