



# Physical modelling of impurity diffusion and clustering phenomena in CMOS based image sensors

Zahi Essa

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# THÈSE

En vue de l'obtention du

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Délivré par :

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**Présentée et soutenue par :**

**Zahi ESSA**

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## **Abstract**

Over the last years, microelectronics growth was made possible thanks to the innovations occurring in CMOS (Complementary Metal Oxide Semiconductor) technology, leading to a constant improvement of device performances. These innovations have to answer the technological challenges related to devices miniaturization, as well as to their continuous diversification. In response to these challenges, modelling approaches such as TCAD (Technology Computer Aided Design) drastically reduce the technologies development time and cost. In this context, the thesis deals with TCAD models development of several physical mechanisms taking place within advanced process steps. In the first part, diffusion and activation mechanisms following high-dose dopant implantation were studied, mainly in the case of plasma implantation, a promising technique for conformal doping in image sensors and Tri-Gates transistors. In high doping conditions, the observation and modelling of large boron interstitial clusters (BICs) were carried out. In the second part, the evaluation of chemical species diffusion and transfer between materials was considered. In particular, Boron dose loss from silicon in spacer stacks and corresponding diffusion in oxide were studied. In addition, lanthanum diffusion evaluation during thermal annealing in gate stacks with high-k oxides was investigated. In the last part, the impact of the different investigated mechanisms on CMOS devices electrical behaviour was finally evaluated, resulting in the improvement of TCAD models predictability on MOS transistors performances, as well as FSI (Front Side Illumination) and BSI (Back Side Illumination) CMOS-based image sensors.



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# List of abbreviations

<b>AA</b>	Anti Aliasing
<b>A/C</b>	Amorphous/Crystalline
<b>APS</b>	Active Pixel Sensor
<b>APT</b>	Atom Probe Tomography
<b>AR</b>	Anti Reflective
<b>BBT</b>	Band to Band Tunnelling
<b>BEOL</b>	Back End Of Line
<b>BIC</b>	Boron Interstitial Cluster
<b>BJT</b>	Bipolar Junction Transistor
<b>BOX</b>	Buried Oxide
<b>BSI</b>	Back Side Illumination
<b>CCD</b>	Charged Coupled Devices
<b>CDF</b>	Cumulative Distribution Function
<b>CMOS</b>	Complementary Metal Oxide Semiconductor
<b>CPU</b>	Central Processing Unit
<b>CVD</b>	Chemical Vapour Deposition
<b>DIBL</b>	Drain Induced Barrier Lowering
<b>DL</b>	Dislocation Loop
<b>DPN</b>	Decoupled Plasma Nitridation
<b>DRAM</b>	Dynamic Random Access Memory
<b>DTI</b>	Deep Trench Isolation
<b>EOR</b>	End Of Range
<b>EOT</b>	Equivalent Oxide Thickness
<b>ETSOI</b>	Extremely Thin Silicon On Insulator
<b>EWf</b>	Effective Work Function
<b>FDL</b>	Frank (or Faulted) Dislocation Loop
<b>FDSOI</b>	Fully Depleted Silicon On Insulator
<b>FDTD</b>	Finite Difference Time Domain
<b>FEM</b>	Finite Elements Method
<b>FEOL</b>	Front End Of Line
<b>FinFET</b>	Fin Field Effect Transistor
<b>FSI</b>	Front Side Illumination
<b>FTIR</b>	Fourier Transform Infrared
<b>GAA</b>	Gate All Around

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<b>GIDL</b>	Gate Induced Drain Leakage
<b>GR</b>	Generation Recombination
<b>HP</b>	High Performance
<b>HRD</b>	Hydrogen Related Defect
<b>IC</b>	Integrated Circuit or Interstitial Cluster
<b>IL</b>	Interfacial Layer
<b>IR</b>	Infra Red
<b>ITRS</b>	International Technology Roadmap for Semiconductors
<b>KMC</b>	Kinetic Monte Carlo
<b>LBIC</b>	Large Boron Interstitial Cluster
<b>LDD</b>	Lightly Doped Drain
<b>LKMC</b>	Lattice Kinetic Monte Carlo
<b>LP</b>	Low Power
<b>LPCVD</b>	Low Pressure Chemical Vapour Deposition
<b>LTA</b>	Laser Thermal Anneal
<b>LPE</b>	Liquid Phase Epitaxy
<b>MC</b>	Monte Carlo
<b>MEMS</b>	Micro Electro Mechanical System
<b>MG</b>	Metal Gate
<b>MIS</b>	Metal Insulator Silicon
<b>MLA</b>	Melting Laser Anneal
<b>MOCVD</b>	Metal Organic Chemical Vapour Deposition
<b>MOS</b>	Metal Oxide Semiconductor
<b>nMOS</b>	negative (type) Metal Oxide Semiconductor
<b>ONO</b>	Oxide Nitride Oxide
<b>PDE</b>	Partial Differential Equation
<b>PDL</b>	Perfect Dislocation Loop
<b>PECVD</b>	Plasma Enhanced Chemical Vapour Deposition
<b>PIII</b>	Plasma Immersion Ion Implantation
<b>PLD</b>	Peroxy Linkage Defect
<b>pMOS</b>	positive (type) Metal Oxide Semiconductor
<b>PVD</b>	Physical Vapour Deposition
<b>QE</b>	Quantum Efficiency
<b>R&amp;D</b>	Research and Development
<b>RS</b>	Row Select
<b>RST</b>	Reset Transistor
<b>RTA</b>	Rapid Thermal Anneal
<b>RTA</b>	Rapid Thermal Processing
<b>SCE</b>	Short Channel Effect

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<b>SF</b>	Source Follower
<b>SCR</b>	Space Charge Region
<b>SIMS</b>	Secondary Ion Mass Spectrometry
<b>SN</b>	Sense Node
<b>SOI</b>	Silicon On Insulator
<b>SPER</b>	Solid Phase Epitaxial Regrowth
<b>SRAM</b>	Static Random Access Memory
<b>SRH</b>	Shockley Read Hall
<b>STI</b>	Shallow Trench Isolation
<b>TAT</b>	Trap Assisted Tunnelling
<b>TCAD</b>	Technology Computer Aided Design
<b>TDS</b>	Thermal Desorption Spectroscopy
<b>TED</b>	Transient Enhanced Diffusion
<b>TEM</b>	Transmission Electron Microscopy
<b>TG</b>	Transfer Gate
<b>ToF-SIMS</b>	Time of Flight Secondary Ion Mass Spectrometry
<b>TTL</b>	Transistor Transistor Logic
<b>USJ</b>	Ultra Shallow Junction
<b>WBDF</b>	Weak Beam Dark Field



# Introduction

Transistors play a key role in modern electronics, and clearly modified our society thanks to innovative applications with a direct impact on our everyday's life. Metal oxide semiconductor (MOS) transistors and related electronic components shrinking size led to the birth of modern microelectronics and the definition of the famous Moore's law by Gordon E. Moore in 1965, according to which the number of transistors on integrated circuits (ICs) doubles approximately every two years [1]. Moore's prediction was more or less satisfied during the last fifty years following the miniaturization of MOS transistors thanks to continually increasing research and development efforts of the semiconductor industry. Miniaturization allowed increasing the number of components in ICs, extending their functionalities. Nowadays, complementary MOS (CMOS) technology is used in several ICs such as microprocessors, microcontrollers, memories, image sensors and others. The semiconductor industry markets are therefore constantly expanding and diversifying. ICs are currently used in several applications [2]: data processing (personal computers, laptops, servers and tablets), communications (mobile phones, smartphones ...), consumer electronics (television sets, music players, gaming consoles ...), automotive, industrial (transport...), military in addition to spatial and medical applications.

According to the International Technology Roadmap for Semiconductors (ITRS) 2011 [3], two main improvement trends are followed by the different actors of the semiconductor industry:

- Miniaturization, or integration level expressed by Moore's law related to shrinking CMOS devices with a direct consequence on cost-per-function decrease. The miniaturization in microelectronics concerns "More Moore" devices and their corresponding scaling from a technology node to another <sup>1</sup>. "More Moore" elements evolution is related to technology node reduction. Currently, the most advanced CMOS commercially available products use 22 nm technology node and R&D efforts for 14 nm node are made by the leading semiconductor companies. "More Moore" elements correspond historically to core CMOS devices such as MOS transistors used in logic circuits and other memory devices.
- Diversification, corresponding to "More than Moore" elements according to ITRS 2011 [3], which are an emerging category of devices integrating additional functionalities that do not necessarily scale according to Moore's law, but provide additional values and functions in CMOS products.

Therefore, semiconductor industry is facing both miniaturization and diversification challenges and the latter's weight is expected to expand over the next years leading to the "pure microelectronics" interaction with other scientific fields in order to maintain progress and innovation. The example of modern mobile phones known as smartphones as a final product addressed by semiconductor companies is quite interesting. Indeed in a smartphone, one can find on one side "More Moore" elements such as MOS transistors in the processors and other memory devices such as Flash and DRAM. On another side, "More than Moore" elements can be found, as the image sensors used in up to two

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<sup>1</sup>The term "technology node" used here is defined as the smallest half-pitch of contacted metal-lines on a given CMOS product [3]. Historically, dynamic random access memory (DRAM) device had the highest integration level among CMOS devices, and was used for "technology node" definition.

camera modules in the phone. Microelectromechanical systems (MEMS) can also be found such as the accelerometer used for screen rotation. Therefore, from the particular example of smartphones, one can see that semiconductor companies have to solve both miniaturization and diversification challenges in order to stay competitive.

Among “More than Moore” elements concerned with both miniaturization and diversification issues, image sensors are also a very good example. In fact, image sensors followed the miniaturization trend which enhanced their electrical performances. In addition, their extra-functionalities would not have been possible without answering the diversification challenges.

Image sensors market is continually growing and the same trend is expected for the next years [4, 5]. Image sensors cover applications in consumer electronics such as mobile phones, cameras, in addition to security, surveillance, automotive, medical and spatial applications. Their market includes two main categories: charge coupled devices (CCD) sensors discovered in 1970 by W. S. Boyle and G. E. Smith [6], 2009 Nobel’s prize [7] and CMOS image sensors based on CMOS technology, invented in 1960 by S. R. Morrison [8]. The cost-effectiveness of CMOS image sensors in comparison to CCD sensors and their easy integration in a CMOS technology scheme gave them a leading role in image sensors market. As a consequence, semiconductor companies quickly became the main actors in this field.

As for core CMOS devices, CMOS image sensors miniaturization is targeted by semiconductor companies in order to increase their electrical performances. Indeed, a CMOS image sensor is an array of pixels, each pixel containing a photo-detector and several MOS transistors in order to convert an optical image into an electrical signal. Thus, increasing the number of pixels is expected to improve the image resolution obtained by a CMOS image sensor. However, as for MOS transistors reducing pixels dimensions leads to several challenges to be solved in order to keep the required CMOS sensor performances.

In order to answer miniaturization and diversification challenges, CMOS devices processes had to continually evolve in order to meet technical requirements in terms of high performance, low operating power and low standby power [9]. Therefore, new materials, new implantation and annealing techniques were developed to answer these challenges and improve overall CMOS devices performances. The impact of such novel techniques on CMOS devices of both “More Moore” and “More Than Moore” categories has to be estimated and optimized. In addition to the direct physical effects observed during the devices fabrication, remaining undesired chemical species configurations may have a direct impact on the performances of the final CMOS devices. Therefore, in addition to the development of such new techniques, their constant evaluation has to be made to avoid devices deterioration. Several conditions have to be tested before a given process step is chosen following the design and fabrication of a great number of samples. This approach is unavoidably time and money consuming in the highly competitive semiconductor industry. In addition, multiplying experimental investigations does not necessarily lead to a better physical understanding of the benefit or drawback introduced by a new process technique. To this regard, technology modelling and simulation can be used to study the physical mechanisms involved by such techniques, therefore making this strategy the best solution to reduce advanced CMOS development cycle, both in terms of time and cost [10]. Such modelling methodologies are called Technology Computer Aided Design (TCAD) and cover: process modelling of the different manufacturing steps and device modelling of the final active devices in their operational regime (electrical, optical ...).

Over the last two decades, thanks to important European but also worldwide R&D efforts, TCAD process and device simulations were able to predict with a sufficient accuracy most of the physical mechanisms occurring in advanced CMOS technologies. With the previously calibrated TCAD models

for technology nodes above 45 nm, core CMOS devices behaviour can be correctly predicted without additional model calibration or development efforts. However, the implementation of new process techniques to improve high performance and low power requirements introduced new physical mechanisms to be accounted for in TCAD simulations. These new concepts referred to both “More Moore” and “More Than Moore” applications (such as CMOS image sensors) are not sufficiently covered by TCAD. Therefore, research collaborations between industrial and academic actors have to be established for a better understanding of physical mechanisms involved in advanced CMOS processes. The PhD thesis described in this report was proposed in this context and carried out in collaboration between STMicroelectronics Crolles and LAAS CNRS Toulouse in the frame of the European project ATEMOX [11] gathering several European industrial and academic partners. The project deals with the development of new TCAD models and improvement of existing ones in order to predict the physical mechanisms involved in advanced process techniques.

In particular, the objectives of my work concern modelling of advanced CMOS devices, answering both miniaturization and diversification challenges in CMOS technologies with a main focus on derivative applications of CMOS image sensors. Therefore, TCAD models should be able to reproduce all these different aspects by improving existing models and developing new models if needed.

The main challenges to be answered by the PhD work are:

- Improving dopants implantation and diffusion modelling in high implant-dose conditions such as those achieved by the plasma immersion ion implantation technique. In such case, diffusion and electrical activation mechanisms may be strongly influenced by the concurrent dopant precipitation phenomena, which are not yet well reproduced by existing TCAD physical models.
- Improving diffusion models of chemical species in multi-materials stacks, due to their expected impact on CMOS devices electrical behaviour. Boron dose loss in nitride/oxide/silicon stacks for instance, is not well understood on both experimental and modelling parts. The dose loss effect modifies electrical characteristics of CMOS based devices and its evaluation in TCAD models becomes mandatory. A second example is lanthanum diffusion in high-k stacks during thermal annealing leading to a negative threshold voltage shift in n-type MOS transistors.

These challenges were investigated during the PhD and the outline of the research activities presented in this report, is the following:

- Chapter 1 summarizes advanced CMOS technologies modelling challenges as well as the main physical concepts that represent the background of the PhD work.
- Chapter 2 deals with implantation-induced defects and their impact on dopant diffusion and activation mechanisms. In this chapter, plasma immersion ion implantation technique will be presented and investigated experimentally and using TCAD modelling, focusing on boron precipitation models for high implantation dose conditions, and corresponding boron diffusion and electrical activation.
- Chapter 3 considers chemical species diffusion in multi-materials stacks. Two main subjects are investigated: (i) boron dose loss in nitride/oxide/silicon stacks modifying electrical characteristics of advanced CMOS devices and (ii) lanthanum diffusion in advanced high-k stacks leading to a negative threshold voltage shift in advanced n-type MOS transistors.
- Chapter 4 deals with TCAD modelling of advanced CMOS devices. The different process models developed in previous chapters will be evaluated in terms of their impact on the electrical characteristics of several advanced MOS transistors, including Bulk, FDSOI and TriGate MOS, but also on FSI and BSI advanced CMOS image sensors.



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- [11] ICT Project 258547 ATEMox Advanced Technology Modeling for Extra-Functionality Devices, Website: <http://www.atemox.eu>.

# Chapter 1

## Advanced CMOS technologies modelling challenges

### 1.1 Introduction

In this chapter, we will summarize the main concepts of the work activities of the thesis. In section 1.2, a brief introduction to MOS transistor and CMOS technology will be given. In section 1.3, image sensors based on CMOS technology will be presented. Considering miniaturization and diversification challenges of CMOS technology, silicon level TCAD modelling will be presented in section 1.5 with an identification of possible improvements of existing models and missing ones.

### 1.2 A brief introduction to MOS transistor

The first pnp point-contact germanium transistor [1] was invented in 1947 by John Bardeen, Walter Brattain and William Shockley, Nobel laureates in Physics 1956 “for their researches on semiconductors and their discovery of the transistor effect” [2]. The following discoveries in semiconductor physics and mainly the development of the first silicon npn bipolar junction transistor (BJT) by Morris Tanenbaum et al. [3] at Bell Laboratories in 1954, clearly reshaped our modern society and the role played by electronics in everyday’s life. Following the silicon bipolar transistor invention, Dawon Kahng and Martin M. (John) Atalla also from Bell Laboratories used an older concept of field effect transistor developed by Julius Edgar Lilienfeld in the 1920s [4] and achieved the first field effect metal oxide semiconductor (MOS) transistor in 1959 [5]. The ease of fabrication of MOS transistors and the advances made in fabrication process techniques quickly allowed the inventors to point out the transistor’s role as a key component in integrated circuits (ICs). Indeed, combining n-type (electrons conduction) and p-type (holes conduction) MOS transistors, logic functions can be developed in the frame of CMOS technology, invested by Frank Wanlass at Fairchild Semiconductor in 1963 [6]. CMOS technology quickly invaded the ICs market replacing the existing transistor-transistor logic (TTL) based on BJTs. In addition to its high noise immunity and low static power consumption, the main advantage of CMOS technology is its high density of integration.

MOS transistor is a key element in modern electronics with main applications in digital technologies. In the frame of CMOS technology [6], a combination of negative type and positive type MOS (respectively nMOS and pMOS) transistors are implemented in order to preform the different logic gates in ICs. nMOS and pMOS transistors are based respectively on the transport of negative charges (or electrons) and positive charges (or holes). In both nMOS and pMOS cases, the MOS transistor is a three-terminal device where the channel conduction between two of the contacts called source and drain is controlled by a third terminal called gate [7]. Therefore, MOS transistor can be used as a switching device, very useful for logic operations in digital circuits. Fig. 1.1 shows the structure

of both nMOS (left) and pMOS (right) transistors obtained by 2D TCAD simulations. The source and drain regions have an excess of negative and positive charges respectively for nMOS and pMOS transistors. For the sake of simplicity and in order to explain MOS operation regimes, we will concentrate on the nMOS transistor, the same explanations being valid for pMOS transistor by reverting the charges sign and applied voltages. In the case of nMOS transistor the n-type source and drain regions have an excess of electron carriers (obtained by external n doping using specific technological processes such as ion implantation to be explained in 1.2.3). Source and drain regions are formed on a p-doped silicon substrate. Therefore, substrate/source and substrate/drain interfaces form two p-n junctions or diodes. Before going further in MOS transistor understanding, p-n junctions basics are reminded in sub-section 1.2.1.

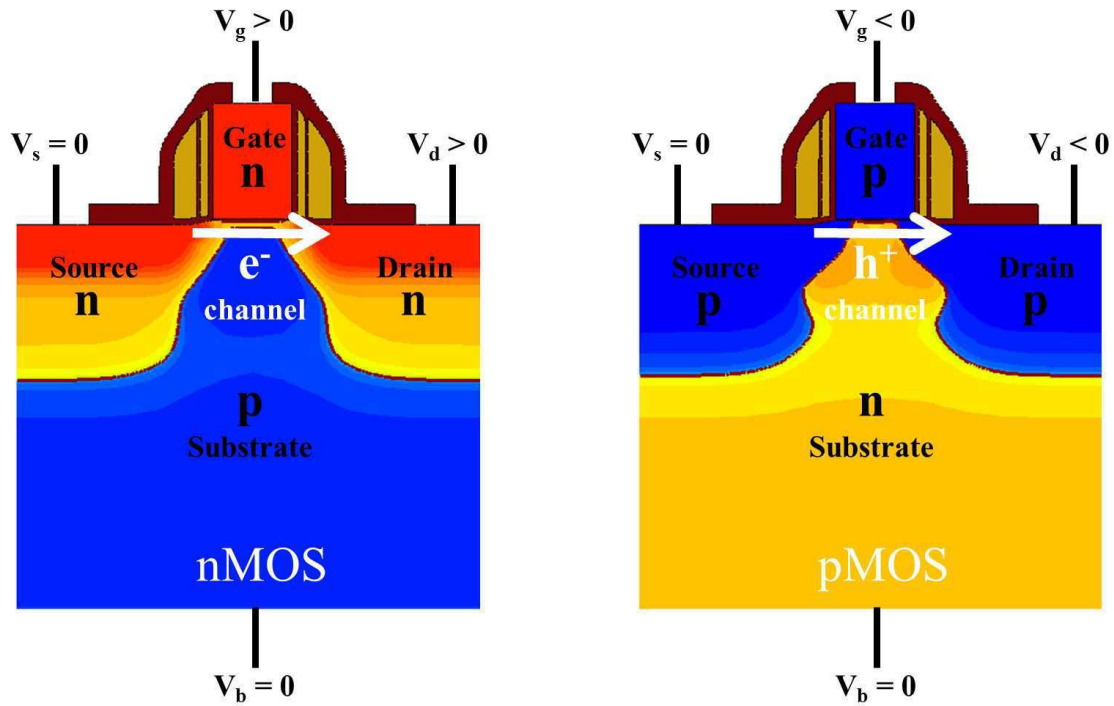


Figure 1.1: nMOS and pMOS transistors two dimensional (2D) structures from TCAD simulations with silicon net doping (red: n-doping, blue: p-doping). Are also given the different terminals voltage conditions leading to a strong inversion regime (sub-section 1.2.3) with electrons and holes transfer between source and drain respectively for nMOS and pMOS.

### 1.2.1 The p-n junction

A p-n junction is a two terminal device, considered as the fundamental element of semiconductor physics, whose mechanisms are extensively explained in reference manuals such as [7, 8]. In the periodic diamond cubic silicon crystal, energy bands of allowed energy states for electrons form in the reciprocal space, separated by energy gaps called band gaps [9]. Electrons in silicon are fermions and therefore, considering Pauli exclusion principle, follow Fermi-Dirac statistics with an energy distribution  $f(E)$  defined by:

$$f(E) = \frac{1}{1 + e^{\frac{E-\mu}{k_B T}}} \quad (1.1)$$

where  $k_B$  is Boltzmann's constant ( $\sim 1.38 \times 10^{-23} \text{ J.K}^{-1}$ ),  $T$  is the temperature in Kelvin (K), and  $\mu$  is the total chemical potential also known as the Fermi level  $E_F$ . In a semiconductor such as silicon,

$E_F$  is located in a band gap and the energy band just below  $E_F$  is called the valence band with an energy maximum  $E_V$ , and the one just above is called the conduction band with an energy minimum  $E_C$ . The two valence and conduction bands are separated by an energy band gap  $E_g$  of approximately 1.12 eV at room temperature [10].  $E_F$  depends on temperature and external (or extrinsic) doping. At finite temperature  $T$ , and due to the Fermi-Dirac distribution 1.1, the valence band is almost full with electrons and some free energy states are available, which leads to the concept of holes (or hole carriers), corresponding to a missing electron and therefore a positive charge in the valence band. It should be noticed that a hole is not an actual particle and is only the mathematical opposite of an electron, introduced for its usefulness in semiconductor physics calculations. From the other side, the conduction band is almost empty with electrons or full with holes. In the pure crystal at finite temperature  $T$ , thanks to the thermal energy some electrons will leave the valence band to the conduction one, contributing in an electron current when an electric field is applied to the material. In an opposite manner, some holes can leave the conduction band to the valence one, leading to a hole current in the presence of an electric field.

Electrons or holes conduction in an undoped silicon (also called intrinsic silicon), is related respectively to available free electrons in the conduction band or holes in the valence band. However, in an intrinsic semiconductor, conductivity control is quite limited and can only be modified by changing the temperature or using an external energy source such as light.

Doping process in semiconductors was first introduced for germanium in 1944 [11], according to which an impurity is intentionally introduced in a pure semiconductor in order to modulate its conducting properties. Doping silicon crystal consists of replacing some crystal sites by dopant atoms, therefore called substitutional atoms. When dopants are introduced in silicon crystal, its periodicity is altered leading to the formation of allowed energy states within the band gap that are close to the valence or conduction energy band, therefore called shallow levels whose exact position depends on the used dopant atoms.

Silicon can be either p or n-doped. In p-doping, periodic table's group III atoms such as boron or indium are commonly introduced in silicon. In n-doping, periodic table's group V atoms such as arsenic, phosphorus or antimony are commonly introduced in silicon and introduce shallow energy levels below the conduction band [7]. p and n dopant are called respectively acceptors and donors. Indeed, when introduced in silicon, thermal energy at room temperature is sufficient to ionize them. If we concentrate on n doping, group V atoms are used and have an additional electron in comparison to group IV silicon atoms. In order to recover the four silicon covalent bonds, they can be considered as positively charged ions in silicon with a free orbiting negative charge or electron in the frame of the hydrogenic model [12], with the binding energy  $E_B$  of the free electron equal to the difference of the conduction band minimum and the dopant's shallow energy level. n dopants are therefore called donors and labelled  $N_d^+$  because they "donate" a free electron to silicon when positively ionized.

In the same manner, p dopant are called acceptors and labelled  $N_a^-$  because they "accept" an additional electron when negatively ionized leading to free hole carriers in silicon.

A p-n junction is simply the association of two oppositely doped silicon regions. In thermal equilibrium conditions and without external applied voltage on the p-n junction and/or electrical current, electrons will diffuse from highly n doped region to the p doped region due to the electron density gradient with a corresponding electron diffusion current. The same mechanism will take place for holes from the p region to the n region with a corresponding holes diffusion current. In addition, a conduction current exists for both electrons and holes due to the electric field between n and p region.

At thermal equilibrium, respective diffusion and conduction currents for electrons and holes cancel out and corresponding total currents equal respectively zero. The main consequences of the electrons and holes respective zero currents are a flat Fermi level value across the p-n junction and the formation of a built-in potential across the p-n junction depending on doping levels in p and n regions. Following diffusion of electrons and holes respectively from n and p regions, n and p sides of the p-n junction are respectively depleted of electrons and holes leaving only fixed charged dopant behind, with  $N_a^-$  concentration in the p region and  $N_d^+$  concentration in the n region. The depletion region is called space charge region (SCR) and the potential drop across the depletion region at zero voltage is the built-in potential. In order to evaluate the extension of the SCR in p and n regions, we will consider the abrupt junction approximation where dopant concentration changes abruptly from  $N_a^-$  in p region to  $N_d^+$  in n region. Poisson equation for the electrostatic potential  $\psi$  in one dimension (1D) is:

$$\frac{\partial^2 \psi}{\partial x^2} = \frac{\rho}{\kappa_{Si} \epsilon_0} \quad (1.2)$$

where  $\rho$  is the charge density including the contribution of electrons  $e^-$ , holes  $h^+$ , ionized acceptors  $N_a^-$  and donors  $N_d^+$ .  $\kappa_{Si}$  is the silicon relative permittivity of approximately 11.7 and  $\epsilon_0 \simeq 8.85 \times 10^{-12} F.m^{-1}$  is the vacuum permittivity. Associating Poisson equation 1.2 with electrical neutrality condition at thermal equilibrium in the SCR:

$$N_a^- W_{D,p} = N_d^+ W_{D,n} \quad (1.3)$$

where  $W_{D,p}$  and  $W_{D,n}$  are respectively SCR extension in p and n regions, one gets from [7]:

$$W_{D,p} = \sqrt{\frac{2\kappa_{Si}\epsilon_0\psi_{bi}}{q} \frac{N_d^+}{N_a^-(N_a^- + N_d^+)}} \quad (1.4)$$

$$W_{D,n} = \sqrt{\frac{2\kappa_{Si}\epsilon_0\psi_{bi}}{q} \frac{N_a^-}{N_d^+(N_a^- + N_d^+)}} \quad (1.5)$$

where  $q$  is the electron charge of  $1.6 \times 10^{-19} C$  and  $\psi_{bi}$  is the built-in potential in the depletion region. From equations 1.4 and 1.5, simple calculations show that the higher the doping in a given region, the lower the SCR extension is in the corresponding region. These conclusions in abrupt junction approximation are still valid for p-n junctions with arbitrary doping profiles.

When a voltage  $V$  is applied to a p-n diode, one can obtain the diode's current-voltage characteristic (or the famous Shockley equation for an ideal diode) where the following approximations are made:

- The applied potential on the diodes boundaries, is the same as the one on the depletion region boundaries. It is equivalent to consider that silicon is neutral outside the p-n junction SCR.
- Maxwell-Boltzmann statistics approximation is considered valid for non-degenerate semiconductors, where Fermi level  $E_F$  (equation 1.1) distance from an energy band extremum is much higher than the thermal energy  $k_B T$ .
- Low injection hypothesis is considered, where injected minority carriers concentration in a given region (due to diffusion currents) is much lower than the majority carriers one.
- Generation-recombination currents (to be considered later) are neglected.

With the previous assumptions, it can be demonstrated [7] that the current-voltage I-V characteristic of the p-n diode follow the Shockley relation [13]:

$$I = I_0 \left( \exp \left( \frac{qV}{k_B T} \right) - 1 \right) \quad (1.6)$$

$V$  is the voltage applied on the p side of the diode (0 V is applied on the n side) and  $I_0$  is the saturation current in reverse regime for a negative voltage  $V$ , depending on doping levels in p and n regions and minority carriers diffusion current characteristics [7]. From equation 1.6, we can notice that in forward regime for a positive voltage  $V$ , p-n diode current  $I_F$  increases exponentially with the voltage with a  $q/k_B T$  slope in logarithmic scale. In the ideal diode approximation,  $I_0$  is temperature dependent and is proportional to  $\exp(-E_g/k_B T)$ . Equation 1.6 is a good starting point to understand p-n diode I-V characteristic. However in real diodes, in addition to dopant atoms, several crystal defects may exist in the p-n junction SCR, introducing deep energy levels located close to silicon mid-gap and leading to an additional generation-recombination (GR) current in reverse regime. According to Shockley-Read-Hall (SRH) statistics [14], for a single energy level  $E_t$  introduced by a given defect (also called a trap for free carriers), the carriers net transition rate is:

$$U = \frac{\sigma_n \sigma_p v_{th} N_t (pn - n_i^2)}{\sigma_n \left[ n + n_i \exp \left( \frac{E_t - E_i}{k_B T} \right) \right] + \sigma_p \left[ p + n_i \exp \left( \frac{E_i - E_t}{k_B T} \right) \right]} \quad (1.7)$$

$\sigma_n$  and  $\sigma_p$  are respectively the electron and hole capture cross sections,  $v_{th}$  is the carriers thermal velocity,  $N_t$  is the traps density,  $p$  and  $n$  are respectively holes and electrons densities,  $n_i$  is the intrinsic carriers density and  $E_i$  is the Fermi level in intrinsic conditions which is close to mid-gap. With the additional GR mechanism of equation 1.7, the reverse current is modified and does not saturate at  $I_0$  as in equation 1.6 but varies with the negative applied voltage. In the presence of the SRH mechanism, the reverse current for a given voltage temperature dependence varies as  $\exp(-E_g/2k_B T)$  for mid-gap levels in the abrupt junction approximation. Therefore, the reverse current integrates both diffusion and GR currents. In addition, in the forward regime, diode current exponential variation with applied positive voltage is modified and verifies the following relation [7]:

$$I_F \propto \exp \left( \frac{qV}{nk_B T} \right) \quad (1.8)$$

where  $n$  is called the ideality factor, equals 1 in the ideal case when the diffusion current dominates and 2 when the GR current dominates. When diffusion and GR currents values are comparable,  $n$  value is between 1 and 2.

As it will be seen in sub-section 1.2.3, in advanced CMOS technologies, SRH mechanism is due to undesired silicon defects introduced during the different process steps. SRH GR current leads to an uncontrolled current in reverse regime called leakage current that can be detrimental for low power applications. In addition to the SRH GR current, a tunnelling GR current discovered by L. Esaki in 1958 [15], appears in highly doped p-n junctions such as the ones used in source/drain of advanced MOS transistors (Fig. 1.1). Indeed, when doping levels difference between p and n region is very high ( $p^+/n$ ,  $p/n^+$  or  $p^+/n^+$  cases) and mainly for abrupt junctions, the electrical field across the p-n junction is very high ( $> 7 \times 10^5 \text{ V.cm}^{-1}$  [16]) and leads to an important valence and conduction bands bending. The potential barrier becomes sufficiently thin and carriers can tunnel across the Fowler-Nordheim triangular barrier [17] with a transfer of an electron from valence band in p region to conduction band in n region, leaving a free hole in the p region. Such mechanism is called band to band tunnelling (BBT) leads to an additional contribution for reverse current, and modifies current-voltage characteristics in the forward regime. It should be noticed that contrarily to diffusion and SRH currents and as discussed in [18], BBT current in reverse regime depends mainly on the applied voltage on the p-n junction and corresponding electric field, and shows very small variations with the temperature.

In real diodes, a GR current using trap assisted tunnelling mechanism (TAT) may also take place. TAT current can be considered as a combination of SRH and BBT in the respective presence of a deep energy level introduced by a given defect and a high electric field. According to the TAT mechanism in the p-n junction, an electron is transferred from the valence band in p region to a trap level located in the SCR, and then crosses a Fowler-Nordheim barrier to reach the conduction band in n region as for the BBT mechanism. Therefore, TAT mechanism in reverse regime has an important temperature and voltage dependence.

Leakage current  $I_{\text{leak}}$  then includes diffusion, SRH, BBT and TAT contributions:

$$I_{\text{leak}} = I_{\text{diffusion}} + I_{\text{SRH}} + I_{\text{TAT}} + I_{\text{BBT}} \quad (1.9)$$

The different contributions activation energies  $E_a$  and thus temperature dependence [18] are summarized in table 1.1.

Table 1.1: Summary of the different leakage current contributions in a p-n junction and corresponding activation energy [18].

Leakage current mechanism	Activation energy
Diffusion	$E_a \sim E_g$
SRH	$E_a \sim E_g/2$
TAT	$E_a \sim E_g/2$
BBT	$E_a \sim 0$

The SRH, BBT and TAT mechanisms simplified presentation described above can be explained microscopically in more details using quantum mechanics methods, which is largely above the scope of this work. Interested readers can look at [19] for more details and references therein.

After introducing p-n junction main concepts, a first step is established in understanding n and p-type MOS transistors operation of Fig. 1.1 with n-p junction for nMOS and p-n junction for pMOS in source/substrate and drain/substrate junctions. However as explained in the beginning of section 1.2, the switching behaviour of a MOS transistor is due to a transfer of carriers between source and drain electrodes with electrons for nMOS (Fig. 1.1 left) , holes for pMOS (Fig. 1.1 right), the transfer and corresponding current being controlled by the applied voltage  $V_g$  on the gate electrode formed by a metal/oxide/silicon capacitance. In order to understand how the gate controls the carriers transfer in MOS transistor, MOS capacitor basics will be reminded in next sub-section 1.2.2.

### 1.2.2 The metal/oxide/silicon capacitance

The gate electrode controls carriers transfer between source and drain in MOS transistors. It consists of a metal-oxide-silicon (MOS) capacitor. MOS structure physics and electrical characteristics are extensively described in [7, 8]. In a MOS structure, the silicon semiconductor can be n or p doped. In the following, we will consider that a voltage  $V_g$  is applied on the metal side of the MOS capacitance, the semiconductor being connected to a zero voltage. Depending on the applied voltage  $V_g$ , both energy band diagram of the MOS structure and the electrostatic potential  $\psi_s$  at the silicon surface near oxide/silicon interface are modified with a corresponding charge distribution at the surface.  $\psi_s = (E_{i,s} - E_{i,bulk})/q$  is classically defined as the difference in Fermi intrinsic level at the surface (modified with  $V_g$  voltage) and in bulk silicon far from the surface (un-modified due to zero voltage). In order to estimate such charges in an ideal MOS capacitance, the following assumptions are made [7]:



- The only charges in the MOS structure are those located in silicon semiconductor, and those with equal quantity and opposite sign located in the metal side of the capacitance. No charges such as interface traps or fixed charges in the oxide are considered.
- No carrier transport is considered in the oxide layer, whose resistivity is assumed to be infinite.
- A zero work function difference  $\phi_{ms} = \phi_m - \phi_s$  is considered between the metal and the semiconductor, where  $\phi_m$  and  $\phi_s$  are respectively the metal and semiconductor work functions. We remind that in a metal (or semiconductor), the work function is the energy difference between the Fermi level  $E_F$  and the vacuum level.

If we consider a p-type semiconductor with constant doping, Fermi level is constant in the semiconductor. With an applied  $V_g$  voltage, valence band maximum  $E_{v,s}$ , conduction band minimum  $E_{c,s}$  and intrinsic Fermi level  $E_{i,s}$  near the surface are modified. An important quantity in MOS capacitance is the Fermi level relatively to the intrinsic level (approximately mid-gap) in the bulk semiconductor defined as  $\varphi_F = E_{i,bulk} - E_F$ , which is positive for p-type silicon. Therefore, if we take the example of a p-type silicon, the following regimes are observed for different applied voltage  $V_g$  and corresponding surface potential values<sup>1</sup> [7, 8] leading to different charge populations near the surface:

- $\psi_s < 0$  or accumulation regime:  $E_{c,s}$ ,  $E_{v,s}$  and  $E_{i,s}$  bend upward. The proximity of the valence band to the Fermi level at the surface leads to an accumulation of holes.
- $\psi_s = 0$  or flat-band condition: in this case no valence or conduction band bending is observed. Charges populations are the same as the ones observed in bulk silicon far from the surface. It should be noticed that in a real MOS capacitance,  $\phi_{ms} \neq 0$  and existing charges at the interfaces and in oxide lead to a non-zero flat-band voltage. In such case, a new potential reference can be defined according to this flat band voltage and the different MOS capacitance regimes described here are still valid.
- $0 < \psi_s < \varphi_F$  or depletion regime:  $E_{c,s}$ ,  $E_{v,s}$  and  $E_{i,s}$  bend downward with  $E_{i,s}$  still above Fermi level leading to a depletion of holes for the surface region leaving behind negatively charged acceptors  $N_{a,s}^-$  forming a depletion layer or SCR near the interface.
- $\varphi_F < \psi_s < 2\varphi_F$  or weak inversion regime:  $E_{c,s}$ ,  $E_{v,s}$  and  $E_{i,s}$  downward bending is more important in this case.  $E_{i,s}$  crosses the Fermi level leading to the formation of an electron minority carriers inversion layer near the surface with a density higher than the hole majority carriers density at the surface  $n_s > p_s$ .
- $\psi_s > 2\varphi_F$  or strong inversion regime:  $E_{c,s}$ ,  $E_{v,s}$  and  $E_{i,s}$  downward bending is even more important than in the weak inversion regime with  $E_{i,s}$  and  $E_{c,s}$  both crossing the Fermi level, leading this time to the formation of an electron minority carriers inversion layer near the surface with a density higher than the hole majority carriers density in the bulk  $n_s > p_b$  where  $p_{bulk} = N_a^-$ .

The previous regimes are valid for an ideal MOS capacitor. Even though the main operation regimes are still valid for a real MOS capacitor, some additional significant physical mechanisms may occur. First of all, as explained previously due to non zero work function difference  $\phi_{ms}$  in addition to interface charge states and fixed charges in the oxide, flat band voltage is not necessarily zero leading to changes in the MOS capacitance different regimes and their voltage ranges. Due to interface charge states and fixed charges in oxide and to the very small thickness of the oxide layer in advanced MOS structures, the oxide with infinite resistivity assumption is no more verified. For instance SRH GR mechanisms with interface charge states may take place, in addition to other tunnelling mechanisms

<sup>1</sup>With a zero work function difference  $\phi_{ms}$  between the metal and the semiconductor,  $V_g = V_{ox} + \psi_s$  where  $V_{ox}$  is the voltage drop across the oxide.



and quantum effects modifying the ideal capacitance.

Similarly to GR mechanisms in p-n junctions in 1.2.1, microscopic understanding of the fundamental mechanisms behind the different carriers transfer mechanisms across the oxide is largely above the scope of this report. Again, interested readers can find the needed information in [19] and references therein.

After introducing the basics of p-n junction in sub-section 1.2.1 and of MOS capacitance in this sub-section, we can now have an understanding of MOS transistors shown in Fig. 1.1 to be presented in next sub-section 1.2.3

### 1.2.3 MOS transistor and CMOS technology

#### 1.2.3.1 MOS transistor operation regimes

As mentioned in the beginning of section 1.1, MOS transistor is a three terminal device (four terminal device if the bulk, or substrate, voltage is taken into account)<sup>2</sup>. The carriers flux between source and drain electrodes is controlled by the gate electrode and its corresponding MOS capacitance. Before detailing MOS transistor fabrication process in advanced CMOS technologies, different MOS transistor operation regimes will be given.

In equilibrium condition all MOS transistors terminals are set to zero:  $V_s = V_d = V_g = V_b = 0$ . In all our discussion  $V_b = 0$  and therefore source, drain and gate voltages will be considered in reference to the bulk potential. We will also consider the nMOS case (Fig. 1.1 left) with n-type source and drain regions and p-type substrate. The same mechanisms can be explained for pMOS transistor by reverting the adequate physical quantities. In order to guarantee a carrier transfer between source and drain, a positive voltage  $V_d > 0$  is applied at the drain electrode. In these conditions, nMOS transistor has the following operation regimes:

- For zero gate voltage  $V_g = 0$ , no current flow is observed between source and drain which corresponds to two n-p junctions (source/bulk and drain/bulk) connected back to back. In this case, the nMOS transistor is said to be in Off state.
- When a negative voltage is applied at the gate electrode  $V_g < 0$ , from 1.2.2 the MOS capacitance is in accumulation regime and hole carriers accumulate in the region near the surface between source and drain called the channel. As in equilibrium condition, no current flow is possible between source and drain regions and the nMOS transistor is in Off state
- When a positive voltage is applied at the gate electrode  $V_g > 0$ , from 1.2.2, the MOS capacitance will reach successively depletion, weak inversion and strong inversion regimes. For a sufficient positive gate voltage in strong inversion regime, a thin electron inversion layer will form in the channel region and carriers flow from source to drain thanks to the applied positive drain voltage. Therefore, in nMOS transistor strong inversion regime, the n-channel conductance is modulated by the gate voltage. Within the charge-sheet model [20], and assuming a constant electrons mobility  $\mu_n$  in the nMOS channel, drain current  $I_d$  as a function of gate and drain voltages can be calculated [7]:

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<sup>2</sup>In Fig. 1.1, a zero voltage is applied at the bulk electrode  $V_b=0$ . However in some advanced CMOS technologies, bulk electrode can be as important as gate electrode for MOS operation as in fully depleted silicon on insulator (FDSOI) transistors.

$$I_d = \frac{W}{L_g} \mu_n C_{ox} \left\{ \left( V_g - V_{fb} - 2\varphi_F - \frac{V_d}{2} \right) V_d - \frac{2}{3} \frac{\sqrt{2\kappa_{Si}\epsilon_0 q N_a^-}}{C_{ox}} \left[ (V_d + 2\varphi_F)^{3/2} - (2\varphi_F)^{3/2} \right] \right\} \quad (1.10)$$

where  $W$  is the transistor width in the horizontal direction perpendicular to the channel direction,  $L_g$  is the gate length related to the metal gate dimension in the channel direction,  $C_{ox}$  is the oxide capacitance and  $V_{fb}$  is the flat-band voltage (needed gate voltage  $V_g$  in order to get flat valence and conduction bands). In strong inversion condition, the nMOS transistor is said to be in On state. In On state, depending on the drain voltage positive value, the following regimes can be distinguished:

- Linear regime: for small  $V_d$  values,  $I_d$  increases linearly with  $V_d$  and the nMOS channel region behaves like a simple resistor. This regime is also called the ohmic regime and can be verified using equation 1.10.
- Saturation regime: when increasing  $V_d$  voltage, the difference between source ( $V_s = 0$ ) and drain voltages will lead to a non uniform inversion layer distribution along the channel region with a thicker channel near the source region in comparison to the drain one. Therefore, when increasing  $V_d$ , the  $I_d$  current linear increasing with  $V_d$  is no more verified. At a given  $V_d$  voltage, the inversion layer thickness on the drain side equals zero. In this condition, the transistor is in the saturation regime with a corresponding drain voltage  $V_{d,sat}$ . This regime can also be verified using equation 1.10.

The MOS transistor regimes presented above and summarized by equation 1.10 are valid for an ideal long channel MOS transistor with ideal p-n junctions and MOS capacitance as discussed respectively in 1.2.1 and 1.2.2. In a real transistor even with a high gate length value  $L_g$ , some non ideal effects are observed, even though the main transistor regimes are preserved. Analysing all the non ideal mechanisms is above the report's scope, and we will discuss some of them when needed all along the report.

For instance in Fig. 1.2, we show  $I_d(V_g)$  current-voltage characteristics for nMOS and pMOS transistors based on the same CMOS technology node of MOS transistors presented in Fig. 1.1 with a gate length  $L_g = 3\mu m$  in both linear for  $V_d = 25mV$  and saturation regime for  $V_d = V_{dd} = 1.2V$  using 2D TCAD device simulations [21].  $V_{dd}$  is the power-supply voltage, corresponding to the maximum voltage that can be applied on gate and/or drain electrodes.  $V_{dd}$  has different values depending on the technology node (decreasing with advanced technology node for power consumption reduction) and on the type of application such as high performance (HP) or low power (LP) ICs. From Fig. 1.2, one can see that as expected,  $I_d(V_g)$  current is higher in saturation regime in comparison to linear one for both nMOS and pMOS transistors. In addition, contrarily to nMOS transistor, gate voltage is negative for pMOS transistor operation.

MOS transistors exhibit many electrical features that can be optimized in a given CMOS technology, the main ones being:

- The threshold voltage  $V_t$ : defined as the gate voltage necessary for electrons conduction in the MOS channel to take place or more specifically to reach strong inversion regime.  $V_t$  voltage is quite difficult to estimate both theoretically and experimentally. From the theoretical side,  $V_t$  expression depends on the approximation made for  $I_d(V_g)$  calculation, with different extracted values depending on the chosen technique. From the experimental side, several techniques can be used for  $V_t$ , also leading to different values depending on the experimental approach. Therefore, one has to use the same reference experimental approach when comparing  $V_t$  values from different

transistors. When dealing with extracting  $V_t$  from modelling as in TCAD, the model used has to be as close as possible to the experimental approach. In this report, our reference for  $V_t$  calculation is a simple and fast method used in parametric testing of MOS transistors, according to which  $V_t$  is the voltage needed to reach a given threshold current in  $I_d(V_g)$  characteristics depending on the technology node and type of device (core MOS, Flash, SRAM ...). It should be noticed that  $V_t$  can be defined both in linear and saturation regimes, labelled respectively  $V_{t,lin}$  and  $V_{t,sat}$ .

- The On current  $I_{on}$ : defined as the drain current when MOS transistor is On when  $V_d = V_{dd}$ . As in the case of  $V_t$ ,  $I_{on}$  can be estimated in linear and saturation regimes, labelled respectively  $I_{on,lin}$  and  $I_{on,sat}$ .
- The Off current  $I_{off}$ : from Fig. 1.2, it can be seen that  $I_d(V_g = 0) \neq 0$ . Indeed in the real transistor, even for a zero gate voltage, a small current can be observed in the drain called the Off current and is due to different leakage currents [18, 22], the main ones being:
  - p-n junctions leakage current and mainly the drain/bulk junction leakage current due to the different GR mechanisms discussed in 1.2.1.
  - Subthreshold leakage detailed in [22] observed in weak inversion regime for  $V_g < V_t$  and due to a small diffusion current of minority carriers between source and drain near the surface. In subthreshold regime, the subthreshold slope parameter can be defined from  $I_d(V_g)$  characteristics:

$$S_t = \left( \frac{d \log_{10} I_d}{d V_g} \right)^{-1} \quad (1.11)$$

$S_t$  is generally measured in mV/decade and typical values for silicon based planar MOS transistors are in the 70-120 mV/decade range [22].  $S_t$  indicates the effectiveness of turning off the MOS transistor and thus, it is desirable to have low  $S_t$  values.

- Gate leakage current across the oxide layer with the different possible mechanisms discussed in 1.2.2. Gate induced drain leakage (GIDL) may also be observed when  $V_g = 0$  and  $V_d = V_{dd}$ . The high electric field in the drain/bulk junction near the surface, leads to enhanced GR mechanisms in the junction's SCR, such as BBT, TAT but also TAT with the help of interface states due to the proximity of the oxide/silicon interface.

$I_{off}$  can also be defined in linear and saturation regime, labelled respectively  $I_{off,lin}$  and  $I_{off,sat}$ .

### 1.2.3.2 MOS transistor miniaturization

MOS transistor down scaling has always been the main objective of the semiconductors industry. The fundamental shrinking dimension is the gate length  $L_g$  of MOS transistors continually reduced and leading to the total transistor surface divided by two for a new technology node as expected by Moore's law [23]. The goal of miniaturization is reobtain a higher number of transistors on the same silicon surface leading to a better performance and lower cost of ICs. Therefore, transistors with small gate length have to be designed in order to keep the same behaviour of transistors from older technology nodes with higher gate length. However, size reduction leads to several additional and correlated physical mechanisms modifying MOS transistors behaviour. In the frame of this work, we will discuss mainly the following scaled parameters: gate oxide thickness  $t_{ox}$ , junction depth  $X_j$  and junction electrical activation level.

When decreasing  $L_g$ , source/bulk and drain/bulk junctions SCR regions dimensions become comparable to the channel dimension, and several effects, labelled short channel effects (SCEs) may occur.

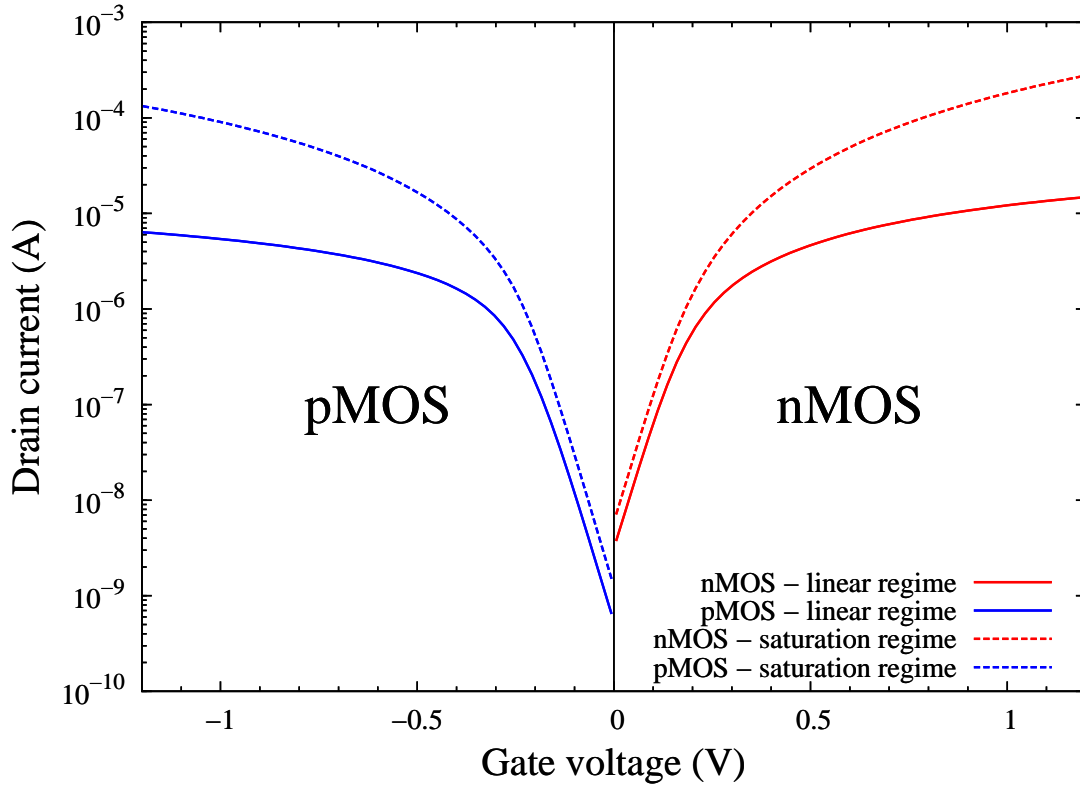


Figure 1.2: nMOS and pMOS  $I_d(V_g)$  characteristics in linear and saturation regimes from TCAD device simulations [21] for the transistors presented in Fig. 1.1 with a gate length  $L_g = 3\mu\text{m}$ .

First of all, for a short channel, a direct contact between the two SCR regions of source and drain can be reached. This effect is called punch-through and leads to an undesired leakage current between source and drain when a high drain voltage is applied. The origin of this effect is the lowering of the energetic barrier for the carriers near the source region referred to as the drain-induced barrier lowering (DIBL). The DIBL can be extracted from  $I_d(V_g)$  characteristics in linear and saturation regimes (Fig. 1.2) and is defined by:

$$\text{DIBL} = V_{t,\text{lin}} - V_{t,\text{sat}} \quad (1.12)$$

One way to avoid punch-through effect is to increase channel doping in order to limit source and drain junctions SCR extension in the channel region according to equations 1.4 and 1.5. However, increasing channel doping will require a higher gate voltage to obtain strong inversion regime, and therefore a higher threshold voltage  $V_t$ .  $V_t$  cannot be increased indefinitely due to power consumption issues and to fixed supply voltage  $V_{dd}$ . Knowing that  $V_t$  varies inversely with oxide capacitance  $C_{ox}$ , reducing oxide thickness  $t_{ox}$  allows to control  $V_t$  value. However, as discussed in 1.2.2 and 1.2.3.1, reducing gate oxide thickness leads unavoidably to gate leakage currents harming transistor performance and increasing  $I_{off}$  and power consumption. One solution is the use of a gate insulator with a dielectric constant higher than silicon dioxide, called high-k dielectric resulting in a higher equivalent  $\text{SiO}_2$  thickness, which will be discussed in detail in chapter 3. It should be noticed that increasing  $C_{ox}$  allows also to increase On current from equation 1.10.

In addition to DIBL, other SCEs may take place regardless of drain voltage, and leading to a decrease in threshold voltage  $V_t$  for short channels, known as roll-off (or roll-down) effect observable on  $V_t(L_g)$  characteristics. The main explanation is that the increased extension of source and drain SCR for a short channel leads to a smaller channel region to be controlled by gate electrode and to

be inverted to reach the On regime of MOS transistor. Therefore, a smaller gate voltage is needed in order to reach strong inversion, and consequently a smaller  $V_t$ . A useful first order estimation of SCEs in both linear and saturation regimes for a short channel length  $L_g$  is:

$$\Delta V_t(L_g) = V_t(L_g) - V_t(L_g = \infty) \quad (1.13)$$

where  $L_g = \infty$  corresponds to a given long channel transistor. It can be demonstrated that  $\Delta V_t$  increases with  $X_j$  [7], the junction depth of source/bulk or drain/bulk junctions. Therefore one way to avoid SCEs is to reduce  $X_j$ . However, let us remind the sheet resistance formula for a thin semiconductor doped layer:

$$R_s = \frac{1}{\int_0^{X_j} q\mu(x)N(x)dx} \quad (1.14)$$

where  $\mu(x)$  is the depth dependent majority carrier mobility and  $N(x)$  is the depth dependent doping concentration. From equation 1.14, a simple approximation of constant mobility  $\mu$  and doping concentration  $N_{dop}$  shows that in the case of source and drain junctions:

$$R_{source}, R_{drain} \propto \frac{1}{N_{dop}X_j} \quad (1.15)$$

Therefore, the drawback of  $X_j$  decrease for SCEs reduction is a higher parasitic source and drain sheet resistance, reducing On current of MOS transistor and its overall performance. In order to limit this effect, from relation 1.15, the junction doping is increased in order to reduce sheet resistance. Therefore, following miniaturization, highly doped and very shallow junctions are used in advanced CMOS technologies and labelled as ultra shallow junctions (USJs) in literature. Advanced doping and USJs fabrication techniques will be presented in 1.4.

### 1.2.3.3 CMOS technology process

The fabrication process solutions found on the fundamental devices level in silicon CMOS technologies to be integrated in the different ICs addressed by the microelectronics industry, include two main parts in the following order:

1. Front-end-of-line (FEOL) processing refers to the formation of transistors and other elemental active devices (diodes, capacitors ...) directly in the initial crystalline silicon substrate in a wafer form.
2. Back-end-of-line (BEOL) processing refers to the formation of the physical interconnections between the active devices manufactured during FEOL process. Interconnections use several levels of metal lines depending on the technology node and integration density. BEOL also include the formation of bonding sites for subsequent packaging operations.

Both FEOL and BEOL processes benefit from photolithography advances, used in microelectronics in order to pattern some parts of silicon substrate and other overlying layers and form the different active devices. The geometric patterns are formed thanks to a combination of a mask and a light-sensitive photoresist. Therefore, improving photolithography resolution is mandatory for technology node evolution.

CMOS technology FEOL part includes several process fabrication steps in order to design the different MOS transistors regions including source and drain junctions in addition to the gate stack. Different process schemes can be used to achieve MOS structures depending on the semiconductor company and on the technology node, with an increasing complexity for the latest technology nodes

for both FEOL and BEOL parts. In the following, we will give a short summary of main process steps of a CMOS technology using heavily doped polycrystalline silicon as a metal for the gate MOS capacitance, close to what can be found in technology nodes above 45 nm. The major CMOS process steps for both nMOS and pMOS fabrication are the following:

1. **Starting Wafer:** the initial silicon substrate generally used in CMOS technologies is crystalline silicon substrate with (100) orientation lightly p-doped with boron. It should be noticed that in advanced CMOS technologies, the substrate's orientation may be changed in order to increase the carriers mobility in transistors channel and improve On current.
2. **Trenches isolation:** trenches can be made in some silicon regions thanks to a specific lithography/etch process. The etched regions are then filled with oxide to isolate electrically adjacent devices such as nMOS and pMOS transistors. Shallow trench isolation (STI) with approximately 300 nm depth, and deep trench isolation (DTI) with few microns depth can be made depending on the device application.
3. **Wells doping:** in order to integrate both nMOS and pMOS transistors on the same silicon wafer the substrate doping type has to be opposite to that of the source and drain regions. However, the initial substrate doping is p-type and some additional steps are needed for both nMOS and pMOS integration. Therefore, well doping by ion implantation is used in order to place dopant atoms at a sufficient depth in silicon. Several doping strategies can be used depending on the type of applications and needed devices protection. The most common way is to start with a deep n-type well doping on the whole substrate, followed by subsequent shallow well doping of two different regions using two separate masks: n-type well doping for pMOS transistors and p-type well doping for nMOS transistors. Implanted ions for well doping are electrically activated using a high temperature anneal.
4. **Gate Stack:** following well doping, a very pure thermal oxide is grown on the silicon substrate as part of the gate oxide of MOS transistor. Using adequate masking, polycrystalline silicon is deposited on the gate oxide to act as the metal contact of the gate. Polysilicon is then etched in well-defined regions forming the gate electrodes and leaving remaining silicon regions in order to define source and drain junctions.
5. **Extensions, pockets and source/drain doping:** Prior to source and drain doping, extension and pocket (or halo) implants are made. Extensions doping, commonly labelled lightly doped drain (LDD) is a shallow doping with lower concentration in comparison to source and drain. Using the direct masking effect of the already manufactured gate electrode, LDDs of the same doping type of source/drain are introduced near the surface in order to get more gradual and less abrupt doping in the transition region between source or drain and the channel. The smaller gradient minimizes series resistance in the source or drain/channel region, but also reduces the electric field in this region decreasing field enhanced leakage mechanisms. Pockets doping is used in addition to LDDs. Pockets use a high concentration doping, of opposite type of the LDDs and source/drain, and are introduced deeper in comparison to LDDs, not closer to the channel region. According to equations 1.4 and 1.5, pockets are used in order to limit source and drain SCR extension in the channel, and reduce SCEs effects. After LDDs and pockets for SCEs improvement, a spacer material is added. The spacer material is generally formed by oxide and nitride isotropic deposition followed by anisotropic etching in order to form two walls on the sides of the gate electrodes. Such side walls called spacers are used in order to limit source and drain doping lateral extension in the channel region due to dopant diffusion during activation annealing (section 1.4). Source and drain doping is achieved by ion implantation, and thanks to the spacers, the dopant atoms are introduced away from the channel region. It should be noticed that in some technologies, several spacer levels can be used in addition to the source/drain ones.



For instance, before the LDD step, a spacer level can be used to limit specifically the LDDs lateral extension. Finally, it should be noticed that the metallic behaviour of the polysilicon used as gate material is due to the LDDs and source/drain high concentration doping. The polysilicon becomes degenerate and behaves like a metal. In addition, depending on the MOS type, polysilicon doping has the same type as the source/drain one (Fig. 1.1).

6. Activation anneal: the final step after LDDs, pockets and source/drain doping is the electrical activation of introduced atoms in order to get a functional device. A high temperature short time thermal anneal (to be detailed in 1.4) is used in order to achieve the highest activation level and the lowest diffusion in silicon for USJs requirements.

### 1.3 CMOS image sensors

Previous section 1.2 dealt with MOS transistors and miniaturization challenges as defined by the ITRS [24] within “More Moore” domain. In this section, we will focus on the example of CMOS image sensors, considered as derivative elements from the “More than Moore” category [24] facing both miniaturization and diversification challenges as discussed in the introduction chapter .

CMOS image sensors cover a large range of applications where the sensors required performances are not the same. This strategy called diversification for CMOS image sensors [24] leads to new challenges depending on the type of application and its corresponding targeted features. Therefore, after introducing CMOS image sensors and their main operation regimes in 1.3.1, their features will be presented in 1.3.2. CMOS image sensors FEOL process is the same as the general CMOS process, however includes some additional steps which will be presented in 1.3.3. Some remarks on BEOL part of CMOS image sensors will also be given in 1.3.3.

#### 1.3.1 CMOS image sensors operation regimes

A CMOS image sensor is an electro-optical module consisting of an IC containing an array of active pixel sensors (APS) converting photons from a given scenery into an electrical digital signal. The different operation steps of a CMOS image sensor are the following:

1. Emitted photons from a light source are partially reflected by a given scenery.
2. Reflected photons reach the CMOS sensor and are focused on the silicon matrix thanks to an optical system. After crossing the optical system, photons reach an infra-red (IR) filter, due to silicon sensitivity to near IR electromagnetic waves ( $\sim 1.1 \mu\text{m}$ ) and in order to capture only visible light photons. Photons will then cross an anti-aliasing (AA) filter in order to avoid high spatial frequency signals and obtain an image resolution achievable by the image sensor. A diagram showing these different parts is given in Fig. 1.3.
3. Due to optical crosstalk (detailed below), photons are focused towards the APS array thanks to a micro-lenses array (Fig. 1.3). Adding a micro-lenses system allows to reduce optical crosstalk effect. After crossing the micro-lenses, photons reach an array of colour filters based on a Bayer filter mosaic [25] (Fig. 1.3). In order to mimic human’s eye response to light and its high sensitivity to green colour, a Bayer system uses a red filter, a blue filter and two green filters periodically disposed above the pixels array. Corresponding pixels are therefore called blue (B), red (R), green blue (GB) for the green pixel next to a blue one and green red (GR) for the green pixel next to a red one.
4. Chromatically filtered photons can now reach the active silicon surface of the pixels. Depending on the illumination strategy (to be described in 1.3.3), the photon may have to cross (or may not)

the different BEOL metal lines before reaching the active silicon surface of the pixel (Fig. 1.3). The pixel consists of a photo-detector, generally a photodiode transforming light to an electrical signal treated and amplified by additional transistors in the pixel.

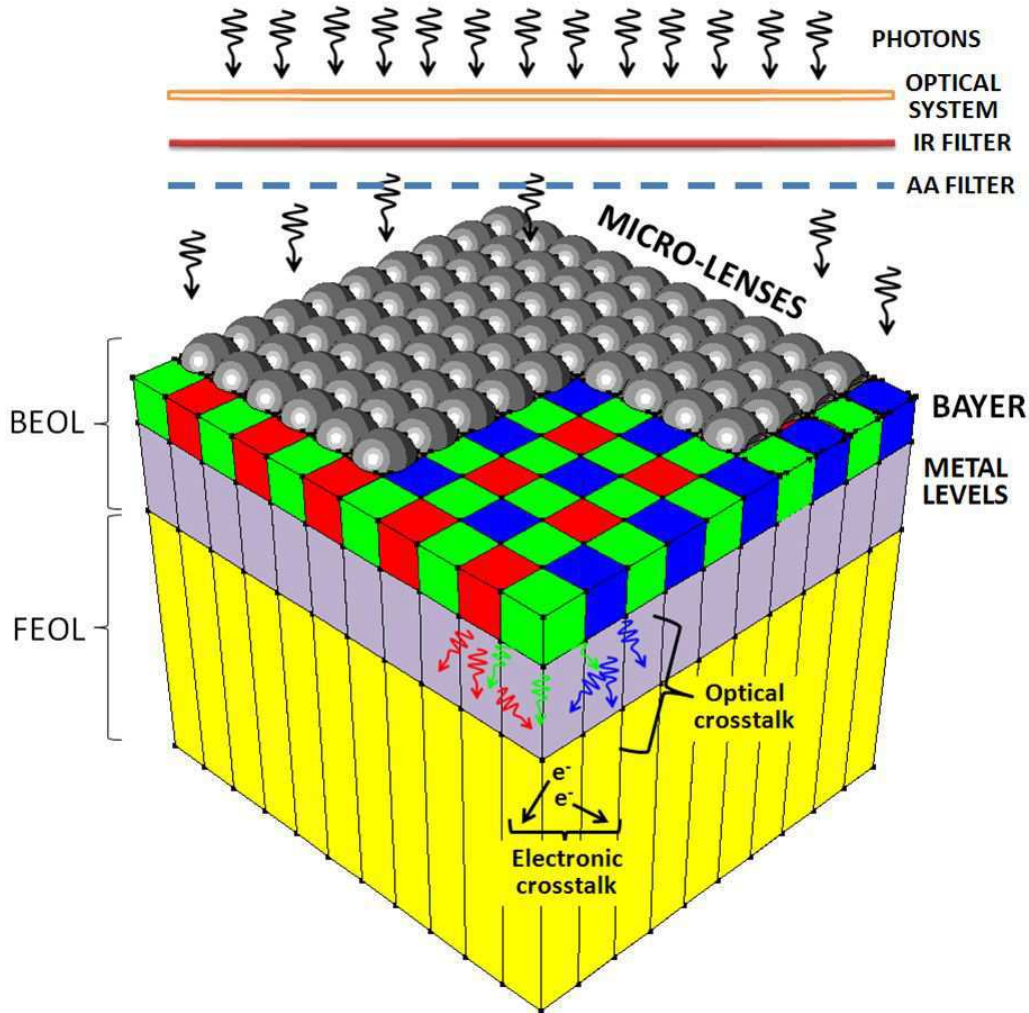


Figure 1.3: Diagram of a FSI CMOS image sensor different parts, crossed by photons including successively the optical system, the IR and AA filters, the array of pixels BEOL part (micro-lenses, Bayer filters and metal levels) and FEOL part. Are also highlighted in this diagram, optical crosstalk in the BEOL part and electronic crosstalk in the FEOL part.

Depending on the required features of CMOS image sensors, the following elements shown in Fig. 1.4 can be found in each pixel [26]:

- A photodiode that converts photons into an electrical signal. Generally, in n-type CMOS image sensors, the photodiode is a n-p junction consisting of an n-doped region surrounded by a p-doping also called pinned photodiode. The SN is first reset and the photodiode is fully depleted. Then during light detection, the photons reach the fully depleted photodiode and generate electron-hole pairs that are stored inside the photodiode. As shown in Fig. 1.4 right, in order to avoid the n-type photodiode electrical contact with top oxide/silicon interface and corresponding leakage currents, a p-type implant, called pinning implant is made. In addition, high  $p^+$  pinning doping is preferred in order to avoid the photodiode SCR extension in the  $p^+$  region near the surface interface. It should be noticed that CMOS image sensors photodiodes



are also investigated on the industrial level with very promising performances in high radiation environments [27].

- A sense node (SN) n-doped in n-type photodiode pixels consists of an n-p diode in association with the photodiode. During an integration time, the SN receives the charges stored in the photodiode, through a transfer gate (TG). By inverting the channel below the TG, the electrons in the photodiode are transferred to the SN whose potential is modified.
- A reset transistor (RST) allows to empty the SN from electrons and initializes its potential after an integration time.
- A source follower (SF) transistor whose role is to amplify and convert the electrons of the SN into a voltage that is the output to the column bus of the pixels array.
- A row select (RS) transistor that allows to connect the pixel's output to the column bus in order to be read.

All the pixels elements are detailed in Fig. 1.4, where we present on the left two Bayer patterns with eight pixels of  $1.4\ \mu\text{m}$  pitch manufactured at STMicroelectronics with their main elements (photodiode, SN, TG, RST, SF and RS transistor). Electrical isolation between the pixels is established thanks to DTIs (1.2.3.3) which will be more detailed in 1.3.3. On Fig. 1.4 right, one pixel's doping is highlighted with the corresponding doping of the photodiode and the SN [28].

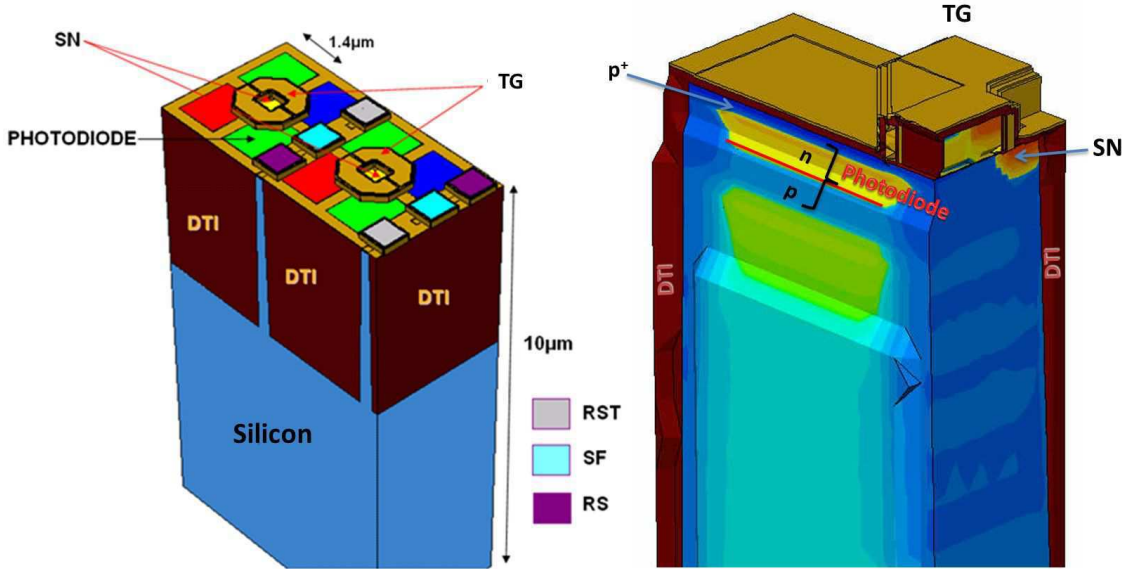


Figure 1.4: Left: two Bayer patterns with eight pixels of  $1.4\ \mu\text{m}$  pitch manufactured at STMicroelectronics with their main elements including the photodiode, the sense node (SN), the transfer gate (TG) in addition to the Reset (RST), Source Follower (SF) and Read Select (RS) transistors, the different pixels being isolated thanks to DTIs (more details in 1.3.3). Right: one pixel's doping is highlighted thanks to 3D TCAD simulations where the photodiode n-doped region can be evidenced in addition to the substrate p and surface  $p^+$  pinning doping [28].

### 1.3.2 CMOS image sensors features

CMOS image sensors have to meet some requirements in terms of geometric, electrical and electro-optical features depending on the type of application. In practice, trade-off among the different requirements is necessary to minimize the undesired effects. The main features are detailed below:

- Geometric features:
  - Resolution: this is the total number of horizontal and vertical pixels in a CMOS image sensor. By increasing this value for a given pixel size (or pitch defined below), the image resolution is improved.
  - Pixels array size: depending on the type of application, the pixels array size may be modified. While the array's size is expected to be small in mobile phone applications, it can be much more higher in medical and spatial applications.
  - Pitch: is a fundamental parameter in image sensors corresponding to the dimension of a square pixel. For a same CMOS imager size, reducing the pixel's pitch allows to increase the number of pixels and therefore the resolution.
  - Filling factor: is the ratio between the photosensitive area and the total area of a pixel. Some strategies where neighbouring pixels share several transistors allow to improve the filling factor as in Fig. 1.4 left where 7 transistors ( $= 4 \times \text{TG} + \text{RST} + \text{SF} + \text{RS}$ ) are shared by 4 pixels of a Bayer pattern.
- Electrical features:
  - Saturation charge  $Q_{\text{sat}}$ : defined as the maximum charges number that can be collected by the pixel's photodiode.  $Q_{\text{sat}}$  is an important feature whose increase improves the image sensor dynamic range, and mainly depends on the photodiode doping and spatial extension:

$$Q_{\text{sat}} = \int_{\text{photodiode}} n(\vec{r}) d\vec{r} \quad (1.16)$$

where  $n$  is the electron density in  $\text{cm}^{-3}$  and the integration is carried out on  $\vec{r}$  3D space vector.

- Photodiode potential: the doping inside the photodiode induces a potential well allowing the storage of the photo-generated electrons. For three dimensional photodiodes structures as the one shown in Fig. 1.4 right, the photodiode potential estimation can be quite complicated and 3D simulations are needed.
- Lag: after the electrons transfer from the photodiode to the SN during an integration step, some of them may remain in the photodiode and are not integrated in the pixel's signal, which is called the lag. The remaining electrons may lead to some additional noise in the image. Therefore, several complex engineering strategies can be used to reduce the lag on the design level but also on the 3D doping extension and corresponding electrostatic potential level in order to improve the electrons transfer
- Dark current  $I_{\text{dark}}$ : represents the charges collected by the pixel's output during an integration cycle, when the pixel is not exposed to light, thus in "the dark".  $I_{\text{dark}}$  is one of the main features to be minimized in CMOS image sensors and depends on several factors:
  - \* Oxide/silicon interfaces surrounding the photodiode (pixel surface, DTIs, or box oxide to be detailed in 1.3.3). The different interface states lead to leakage mechanisms such as the ones described in 1.2.2 on MOS capacitance and contribute to the dark current.
  - \* Process induced defects, that introduce deep energy levels in the SCR of the photodiode as described in 1.2.1. The defects can be formed during implantation and annealing process steps but can also consist of metal contaminants randomly distributed in the pixel and in the sensor's matrix [29].
  - \* Tunnelling mechanisms in the photodiode SCR region (cf. section 1.2.1).
  - \* Transfer gate leakage mechanisms such as GIDL (cf. section 1.2.3.1).

- Electro-optical features:

- Quantum efficiency  $QE(\lambda)$ : a major wavelength dependent feature of CMOS image sensors, defined as the ratio of collected charges by a given pixel on the number of incident photons reaching the pixel.  $QE(\lambda)$  is a dimensionless parameter allowing to account for the different signal losses for a given wavelength in both the FEOL and BEOL parts of the CMOS image sensor. Quantum efficiency versus wavelength is defined by:

$$QE(\lambda) = \frac{N_e - hc}{\phi_0 t_{int} \lambda} \quad (1.17)$$

where  $N_e$  is the number of photo-generated electrons,  $h$  is the Planck constant ( $\sim 6.63 \times 10^{-34}$  J.s),  $c$  is the light's velocity in vacuum ( $\sim 3 \times 10^8$  m.s $^{-1}$ ),  $\phi_0$  is the incident optical power in W and  $\lambda$  is the wavelength in nm.  $QE(\lambda)$  characteristics are measured for each pixel of a Bayer pattern and the mean quantum efficiency can be defined as:

$$QE_{mean} = \frac{QE_B + QE_{GR} + QE_{GB} + QE_R}{4} \quad (1.18)$$

- Crosstalk: for a given pixel, it represents the parasitic signal from neighbouring pixels. Due to pixels miniaturization, crosstalk is an important feature in image sensors with two main components. Optical crosstalk is due to photons crossing the different BEOL parts including micro-lenses, colour filters and metal lines, and landing in a wrong pixel as highlighted in Fig. 1.3. Electronic crosstalk is due to photo-generated charges transfer between neighbouring pixels. Electronic crosstalk can be reduced thanks to DTIs as shown in Fig. 1.4.

### 1.3.3 CMOS image sensors process

CMOS image sensors fabrication process is based on CMOS technology already detailed in 1.2.3.3 for MOS transistors. However, in comparison to a “classical” core CMOS process some additional steps are introduced in the FEOL and BEOL parts of CMOS image sensors as it will be detailed in the following sections.

#### 1.3.3.1 CMOS image sensors FEOL process

In addition to the different process parts detailed in 1.2.3.3, CMOS image sensors FEOL process includes the following additional steps:

- DTIs: similarly to STIs used to isolate MOS transistors in core CMOS, several microns deep trenches are etched in silicon. After silicon etching, several implantations are made throughout the DTIs with a doping opposite to the photodiode's one, followed by trenches filling with silicon oxide. The additional DTIs doping avoids the photodiode SCR extension on the DTIs oxide/silicon interfaces, which can be a source of additional dark current. DTIs are used as physical boundaries between the different pixels of the CMOS image sensor as already shown in Fig. 1.4. The main advantage of DTIs is an electrical isolation between the pixels which reduces electronic crosstalk.
- Photodiode doping: this is achieved using an additional mask and implants before spacer and source/drain steps. The photodiode is called planar when its doped region is close to the flat horizontal surface as shown in Fig. 1.4 right. With pixels miniaturization, the photosensitive region of the pixel is reduced, thus the number of photo-generated charges, directly influencing  $Q_{sat}$  and the image sensor dynamics. In order to increase the collection region, photodiodes with vertical and deep doping extension are designed [30, 31] as the one shown in Fig. 1.5

modelled in [28]. In addition, as expected by Beer-Lambert's law [32], a vertical and deep doping distribution allows a better collection of photo-generated charges through the visible light spectrum.

- Pinning implant: for a photodiode with a given doping and in order to avoid the extension of the SCR outside the photodiode, additional doping opposite to the photodiode's one is used. For instance, for a planar photodiode as in Fig. 1.4, a  $p^+$  surface doping is added for the n-doped photodiode. Pinning  $p^+$  implants are also made in the DTIs to vertically pin the photodiode's potential, as in Fig 1.5.

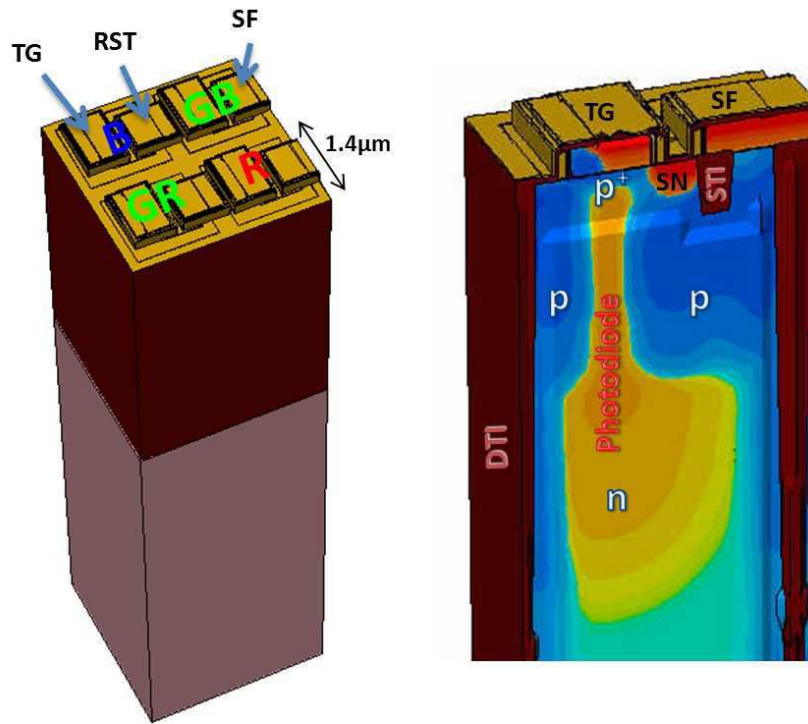


Figure 1.5: Left: Bayer pattern with four pixels of  $1.4 \mu\text{m}$  pitch with a vertical photodiode manufactured at STMicroelectronics, and their main transistors including the TG, the RST and the SF, the different pixels being isolated thanks to DTIs. Right: one pixel's doping is highlighted thanks to 3D TCAD simulations [28] where the vertical photodiode n-doped region can be evidenced in addition to the vertical and surface  $p^+$  pinning doping [31].

### 1.3.3.2 CMOS image sensors BEOL process

Following FEOL process steps of the image sensor presented in 1.3.3.1, BEOL steps are performed including metal levels for the different pixels elements connections, colour filters and micro-lenses array fabrication already mentioned in 1.3.1. In the BEOL process, depending on the different image sensors parts crossed by the light before reaching the photosensitive area of the pixel, two approaches can be distinguished:

- Front Side Illumination (FSI): in this approach, colour filters and micro-lenses are directly implemented on the silicon active region and overlying metal levels. In this case after micro-lenses and colour filters, the light has to cross the different metal levels before reaching the silicon photosensitive region. Therefore, light reflections on the different metal levels before reaching silicon can both decrease QE and increase optical crosstalk presented in 1.3.2, deteriorating pixels

performances. It should be noticed that these effects are increased with pixels size reduction due to an increasing metal lines density.

- **Back Side Illumination (BSI):** for small pixels, due to QE reduction and optical crosstalk increase, FSI approach becomes limited. In back side illumination approach, a silicon on insulator (SOI) substrate obtained by the Smart Cut<sup>TM</sup> technique [33, 34] is used. The FEOL part of the image sensor is carried out on the SOI active silicon on top of the SOI oxide and followed by the metal levels of the BEOL part. The wafer is then flipped, and a silicon substrate thinning is made until reaching the SOI oxide, above which the colour filters and micro-lenses array are manufactured. Therefore, the light only needs to cross micro-lenses and colour filters before reaching silicon active region, and the reflections on metal lines are avoided, improving QE and reducing optical crosstalk. In order to increase the pixels performances, the SOI oxide is replaced by a nitride/oxide/nitride (ONO) stack acting as an anti-reflective layer and improving light collection [31, 35].

## 1.4 Advanced process techniques

In CMOS based devices, such as MOS transistors and CMOS image sensors, doping is a fundamental step in FEOL processes for the formation of the electrically active silicon regions.

Doping consists of two main steps:

1. Dopant introduction in silicon using an implantation technique.
2. Electrical activation of the dopant using a thermal anneal.

The need for highly doped and/or ultra-shallow junctions with low leakage currents leads to several R&D efforts on the process techniques for both implantation and thermal annealing. In addition, several physical mechanisms may take place during these process steps and their control is necessary for functional devices development. Therefore, physical mechanisms occurring during implantation and annealing process steps will be presented in 1.4.1. Considering these physical mechanisms, we will present in sections 1.4.2 and 1.4.3 the different available techniques to meet the advanced junctions requirements in terms of high doping and/or shallowness and low leakage that can be used during implantation step.

### 1.4.1 Physical mechanisms during implantation and thermal annealing

Ion implantation has been used since the 1960s, following the need for a better control of dopant profiles spatial extension in silicon based devices. During ion implantation, the dopant atoms in an ion form are introduced in silicon following an electrical field induced acceleration. A summary of modern ion implantation techniques with a focus on USJs can be found in [36]. The main ion implantation techniques currently used in semiconductor industry are:

- “Conventional” beam-line implantation where dopant atoms are ionized in a plasma source and introduced in silicon following an electrical field acceleration and a magnetic field mass selection. In the ion implantation process, several parameters can be fixed such as the ion energy determining the implanted depth of dopant atoms and the mean value of their spatial distribution also known as the projected range  $R_p$ . Dopant total quantity can also be defined by the implantation dose (in  $\text{cm}^{-2}$ ) and finally the tilt angle with respect to silicon surface can also be fixed.

- Plasma immersion ion implantation (PIII) is a very promising alternative to traditional beam-line for applications where highly-doped or shallow or conformal junctions are needed. PIII will be presented in detail in chapter 2 on both experimental and modelling level, where we will see that the dopant is located at the surface with a peculiar shape of the dopant distribution defined by the plasma acceleration voltage.

When a dopant atom is introduced in silicon either by beam-line implantation or PIII, its initial energy when entering the silicon crystal will unavoidably lead to the creation of additional interstitial and vacancies called point defects. Thus during implantation, the silicon crystal can be severely damaged and even amorphized for high energy (or acceleration voltage for PIII) and dose conditions.

After implantation, silicon is far from equilibrium and the crystal is highly super-saturated with silicon interstitial and vacancy point defects. In such non-equilibrium conditions, a point defect super-saturation is defined as:

$$S_X = \frac{X}{X^*} \quad (1.19)$$

where  $X$  and  $X^*$  are respectively the point defect  $X$  concentration in implanted silicon and in silicon at thermal equilibrium.

Point defects play a major role on dopant dynamics during thermal annealing, where several complex physical mechanisms summarized in [37], may take place.

During thermal annealing, dopants diffuse in silicon by forming pairs with point defects [37, 38]. Considering a dopant  $A$  and point defect  $X$ , the diffusing species can be  $AI$  (dopant-interstitial) or  $AV$  (dopant-vacancy) for respectively interstitial and vacancy mediated diffusion. Consequently, dopant  $A$  diffusion mediated by  $AX$  pair increases with the point defect  $X$  supersaturation  $S_X$ . It should be noticed that  $AX$  diffusing pairs may exist in different charge states leading to a diffusion dependent with the Fermi level and therefore silicon background doping. Diffusion in  $AX$  form also depends on the stress field in the silicon material.

In addition to pairs formation, dopant atoms  $A$  and point defects  $X$  can aggregate forming  $A_nX_m$  clusters with  $n$  dopant atoms  $A$  and  $m$  point defects  $X$ . Such clusters are generally immobile and do not diffuse, even though some small clusters can be mobile at high doping concentration [39]. Dopant defect clusters are electrically inactive and explain the different deactivation mechanisms taking place in highly doped silicon.

Point defects resulting from implantation may also aggregate to form pure point defect clusters or other extended defects. For instance vacancy point defects may form clusters  $V_n$  that have been investigated experimentally and theoretically in literature [40–42]. However, main literature studies on point defects aggregates concern interstitial clusters and extended defects. Indeed, during the first steps of thermal annealing, in addition to  $AX$  pairs diffusion and  $A_nX_m$  clusters formation, interstitial  $I$  and vacancy  $V$  atoms will recombine. The  $I$ - $V$  recombination will leave an excess of silicon interstitial atoms in crystalline implanted regions (in amorphous region  $I = V = 0$ ), with a concentration corresponding to the implanted dopants concentration. Thus, an interstitial supersaturation  $S_I$  is mainly obtained after the implant leading to the formation of interstitial extended defects  $I_n$ . Interstitial extended defects grow following an Ostwald ripening mechanism detailed in [43]. Indeed, the interstitials super-saturation in equilibrium with a defect of size  $n$  is given by:

$$S_I(n) = \exp \left[ \frac{E_f(n)}{k_B T} \right] \quad (1.20)$$



where  $E_f(n)$  is the formation energy of a defect of size  $n$ . Given that the formation energy decreases with the defect size  $n$  [43], interstitials super-saturation is higher around small defects in comparison to big ones, leading to an interstitials flux from small to big defects, in agreement with Ostwald ripening mechanism. With increasing defects size and decreasing formation energy the following defects can be formed: small interstitial clusters (ICs) for small  $n$  values,  $\{113\}$  rod-like defects, (111) faulted circular Frank dislocation loops (FDLs) and (111) perfect elongated loops (PDLs). For a non amorphizing implant, interstitials extended defects form at the implanted dopant projected range  $R_p$ . For an amorphizing implant, excess interstitials are located below the amorphous/crystalline (A/C) interface, and therefore extended defects will form in this region and are labelled end of range (EOR) defects.

After an implantation step, excess interstitials are in small ICs form leading to a high interstitial super-saturation according to equation 1.20 and [43] for formation energy versus size dependence. For dopant diffusion mediated by interstitials, an important and transient diffusion takes place at the beginning of annealing following an implantation step. Such mechanism is known as transient enhanced diffusion (TED) in literature, and was one of the major challenges in USJs realisation. TED can be reduced by using high temperature and short time thermal anneals, in order to quickly reduce  $S_I$  forming big size extended defects. Advanced annealing techniques presented in 1.4.3 allow to answer TED challenges.

Extended defects presented above introduce deep energy levels in the silicon bandgap and are responsible for junction leakage currents when located in the SCR of advanced junctions. Several literature studies showed the direct correlation between EOR defects following amorphizing implants and junction leakage currents [18, 44–46]. It should be noticed that deep energy levels introduced by extended defects can be either discrete, or correspond to a continuum energy band in the silicon band gap, depending on the local environment of the extended defect as defined by Schröter et al. [47].

We mainly described physical mechanisms taking place in silicon material during thermal annealing. However, dopant but also other chemical species present in CMOS based devices can diffuse from one material to overlying (or underlying) ones and segregate at the different materials interfaces. In such case, the chemical species diffusion has a multi-materials aspect, requiring dedicated experimental investigation. Chemical species transfer from a material to neighbouring ones may have an impact on electrical performances of CMOS based devices.

### 1.4.2 Implantation advanced solutions

In order to answer the different challenges of advanced junctions in terms of high electrical activation, shallowness and low leakage currents for low power applications, several solutions already exist at the implantation process [36]. The solutions considered here concern mainly conventional beam-line implantation while PIII advantages will be detailed in 2. The following approaches are currently used in advanced CMOS technologies:

- Amorphization pre-implant: an amorphizing pre-implant, generally germanium ions, can be used in order to improve dopant diffusion and activation, following a thermal anneal. Indeed, during thermal annealing, amorphous silicon phase will recrystallize thanks to solid phase epitaxial regrowth (SPER) mechanism [48]. A better dopant electrical activation is generally obtained during SPER [49]. However after SPER, activated dopant atoms are in a metastable state, and subsequent thermal annealing may lead to dopant deactivation as observed in [50, 51] for boron. However, due to the high doses used in pre-amorphization implants, EOR defects will unavoidably form, and their location has to be carefully adjusted in order to avoid leakage currents. In addition, the free interstitials gradient between EOR defects and surface oxide/silicon

interface with a corresponding diffusion from EOR defects to the surface is responsible of dopant deactivation for thermal anneals subsequent to SPER [51].

- **Molecular implants:** for USJs applications in the sub-keV implantation energy regime, using traditional beamline implantation becomes very limited and mainly for light ions such as boron. Therefore, molecular implants are used in advanced technologies where an ionized molecule containing the dopant atom is implanted in silicon, in order to benefit from the molar mass ratio scaling factor  $M_{\text{ion}}/M_{\text{molecule}}$  leading to a lower ion implantation energy. For instance,  $\text{BF}_2$ ,  $\text{B}_{18}\text{H}_{22}$  or  $\text{C}_2\text{B}_{10}\text{H}_{12}$  (carborane) molecules can be used for boron implantation in silicon.
- **Cold implantation:** traditionally ion implantation is carried at room temperature. As mentioned in 1.4.1, I-V recombinations take place during the implantation step which is known in literature as dynamic annealing. Therefore, interstitials and vacancies initial concentrations after the implant depend on the dynamic annealing mechanisms. Recently, several results showed that ion implantation performed at low temperature below  $0^\circ\text{C}$  is quite interesting in order to reduce post-implants excess interstitials concentration. At low temperature, I-V recombinations that are thermally activated are highly reduced leading to a higher damage accumulation in comparison to room temperature implants and consequently a deeper A/C interface. Therefore, excess interstitials concentration below the A/C interface is lowered, EOR defects density is lowered leading to lower deactivation for thermal anneals subsequent to SPER and reduced junction leakage currents [52–54].
- **Impurities co-implants:** in order to reduce interstitials super-saturation introduced by dopant implants, additional non doping impurities can be implanted or co-implanted. Such impurities form stable clusters with both interstitials and vacancies and act as traps for these point defects. Therefore by capturing free interstitials (or vacancies), the co-implanted impurities allow to reduce dopant diffusion and improve their activation by avoiding the formation of stable dopant-defect clusters. For instance, carbon [55, 56], fluorine [57, 58] and nitrogen [59, 60] can be used in order to reduce interstitials super-saturation and therefore boron diffusion in silicon.

### 1.4.3 Thermal annealing advanced solutions

Both dopant diffusion and electrical activation mechanisms are thermally activated, with a higher activation energy for the latter [61]. Therefore, high temperatures are used in advanced process techniques ( $1000^\circ\text{C}$ ) due to their much higher beneficial effect on dopants electrical activation, in comparison to their diffusion. Short times are used in USJs applications in order to reduce dopant diffusion and mainly TED for USJs applications. A summary of advanced annealing techniques can be found in [62, 63]. Here, we will present the different annealing approaches found on the industrial level in terms of temperature and time characteristics:

- **Rapid thermal processing (RTP) anneals:** also called rapid thermal anneals (RTA) are the most common in semiconductors industry. In RTPs, a thermal anneal includes a temperature ramp-up, plateau and ramp-down performed thanks to high intensity lamps such as halogen or infra-red lamps providing fast and uniform heating. Ramp-ups can vary from  $20^\circ\text{C/s}$  to  $400^\circ\text{C/s}$  which is interesting to reduce TED [64]. Ramp-downs are however more limited on the order of  $80^\circ\text{C/s}$ . The plateau part temperature can reach  $1300^\circ\text{C}$  and last several seconds or minutes, leading to what is commonly called “soak” anneals. RTAs with very short plateau time of several fractions of a second to few seconds are called “spike” anneals and are generally used for source/drain USJs activation in advanced CMOS technologies.
- **Flash anneals:** in flash lamp anneals (duration in millisecond range [65, 66]), a xenon lamp electrical discharge is generally used allowing thermal anneals up to  $1300^\circ\text{C}$  with ramp-up



reaching  $10^6$ °C/s and ramp-downs from 50 to 400°C/s leading to interesting junctions characteristics in terms of shallowness (due to ms times) and electrical activation (due to high temperature) [67, 68]. However, it was also observed [68] that EOR dissolution following their interaction with oxide/silicon surface is slower for flash anneals in comparison to RTP ones. Indeed, despite the high temperature used, flash anneals are not long enough to remove or decrease the residual EOR defects.

- Laser thermal anneals (LTA) can currently be considered as the most advanced industrial annealing approach in terms of short times (nanosecond range) and high temperatures exceeding sometimes silicon melting temperature (1412°C). Excimer laser annealing is generally used with UV wavelength and pulses in the nanosecond range, where a pulsed laser beam scans a silicon wafer surface leading to a local nanosecond annealing of silicon surface. However, contrarily to RTP and flash anneals, LTA is highly non-uniform leading to a temperature field in silicon depending on the scanned surface nature [69]. In addition, depending on the laser fluence (in J/cm<sup>2</sup>), but also on the number of laser pulses, local temperature at the silicon surface may exceed the melting one [62]. Therefore in LTA, two main regimes can be distinguished:
  - Sub-melt regime: where local temperature in silicon is high ( $\sim 1300$ °C) but below melting point. In this regime, due to very short times of annealing, no profile diffusion is observed and diffused profile is almost identical to the as-implanted one. In addition, due to the high temperatures used in this regime, dopant can be electrically activated with an activation rate depending on the laser characteristics such as pulse duration, fluence or number of pulses.
  - Melt regime: where local temperature exceeds melting point leading to a corresponding silicon melting during the anneal also depending on melting characteristics. However, physical mechanisms are more complex in melting regime. During the anneal, silicon melt is localized near the surface, while silicon substrate is at room temperature and followed by a regrowth through a liquid phase epitaxy (LPE). During LPE, and similarly to what is observed in SPER, higher dopant activation can be achieved in comparison to the sub-melt regime due to faster interface regrowth velocity (4-5 m/s) [70]. In liquid silicon, dopant diffusivity is almost  $10^8$  times greater than in solid silicon. The combination of high dopant diffusivity and LPE regrowth velocity leads to highly activated uniform, abrupt and box-shaped dopant profiles, the box dimension being determined by the molten silicon depth.

Both sub-melt and melt regimes are useful for localized anneals where very low dopant diffusion is needed. High activation levels can be obtained in the melt regime and when increasing the pulses number in the sub-melt regime [62]. For BSI CMOS image sensors applications, LTA is an interesting technique for localized dopant activation in the pixel backside region at the SOI oxide/silicon interface without frontside dopants diffusion. Backside doping is used in order to avoid vertical photodiode (Fig. 1.5) SCR extension near the interface, leading to a dark current reduction. However as for flash annealing, one of LTAs drawbacks is the short time used, insufficient for extended defects dissolution. Thus, LTA conditions can be chosen in order to avoid extended defects formation in the SCR region of p-n junctions.

## 1.5 Silicon level TCAD modelling

As we have seen in previous section, several complex doping techniques in terms of implantation and thermal activation can be used for advanced CMOS devices manufacturing. Therefore, modelling methodologies such as TCAD can drastically reduce CMOS technologies development cycle time and cost. In the frame of this PhD thesis, the industrial software Synopsys Sentaurus TCAD was used, including two main parts:

- Sentaurus process (SProcess) [71]: where the FEOL part processes for CMOS based devices can be carried out including mainly implantation and thermal annealing steps in addition to topographic operations such as deposition and etching. Simulations can be performed in 1D, 2D and 3D.
- Sentaurus device (SDevice) [21]: following the process simulations of SProcess, CMOS based devices electrical simulations can be carried out thanks to SDevice, also in 1D, 2D and 3D.

Thanks to several literature results to be detailed below and within previous European projects [72, 73], TCAD models are able to predict complex doping profiles in advanced CMOS technologies and corresponding electrical characteristics ( $I_d(V_g)$ ,  $V_t(L_g)$ ,  $QE(\lambda)$  ...) of core CMOS devices. State-of-the-art TCAD models already available at the beginning of the PhD thesis will be presented in 1.5.1. TCAD models considered here will deal mainly with dopant implantation and diffusion for process modelling part in 1.5.1.1 and junction leakage currents for device modelling part in 1.5.1.2. Missing models will be identified and discussed in 1.5.2 and will allow us to define the goals of this work.

### 1.5.1 State-of-the-art TCAD models

#### 1.5.1.1 Advanced process models

For silicon TCAD process modelling, two main modelling approaches are available:

- Continuum: this approach is based on partial differential equations (PDE) for the different diffusion and reaction mechanisms taking place during an annealing step. PDEs based equations for point defects, dopant, and other dopant defect complexes are discussed in details in [37, 38] and references therein. The PDEs numerical resolution is based on finite element methods (FEM). Therefore, CPU (Central Processing Unit) time depends on the meshing characteristics, and generally increases with the number of PDEs but mainly when several PDEs are coupled due to non-linear effects. It should be noticed that continuum models concern the thermal annealing part. The implantation step previous to the annealing one can be simulated with two methods:
  - Analytical: where dopant analytical tables are simply loaded during an implantation step depending on the implantation characteristics (energy, dose, tilt, ...). In this approach, crystal damage (= Interstitials + Vacancies) is calculated thanks to the Hobler model [74]. Due to its low CPU time, this approach is very attractive for large 3D structures including several transistors as in CMOS image sensors.
  - Monte Carlo (MC): this statistical approach allows the calculation of dopant ion penetration in silicon and corresponding damage generation using the binary collision approximation [75–77]. MC approach is more physical than the analytical one and indeed, analytical tables are generally calibrated using Monte Carlo implants simulations [74]. The MC method can be highly CPU consuming, however can easily benefit from parallelization techniques due to its statistical character.
- Kinetic Monte Carlo (KMC): this approach is both atomistic and probabilistic and uses Monte Carlo methods. Details on the KMC technique applied to silicon material can be found in [71, 78, 79]. In this approach all silicon defects can be modelled (point defects, dopant, clusters, EOR defects ...). Every physical effect such a diffusion or reaction mechanism, corresponds to a random event with a well-defined frequency. KMC can also be used in association with the implantation simulation where dynamic annealing can be taken into account, which can be suitable for cold implants and other dose rate (in  $\text{cm}^2.\text{s}^{-1}$ ) dependent implants simulations. KMC simulations are generally CPU consuming. However, CPU time becomes equivalent to continuum approaches for nanometric devices, while similarly to MC implants, KMC can also

benefit from parallelization. Finally, a KMC version with silicon lattice atoms can be considered and is called lattice KMC (LKMC). LKMC technique is generally used in some particular process steps such as SPER.

The PhD work mainly focused on continuum approach discussed above, and therefore only state-of-the-art process models using this approach [71] will be presented below.

First of all, the majority of advanced diffusion models in silicon use the five-stream model [80, 81] where dopants diffuse by forming a pair with point defects. Five equations are therefore needed to model diffusion mechanisms: one for dopant atoms, two for point defects (interstitials and vacancies), one for dopant-interstitial pairs and one for dopant-vacancy pairs. It should be noticed that point defects and dopant-point defects charge states are also taken into account in advanced five-stream models.

Considering point defects interstitial complexes, several small interstitial clusters (ICs) can be considered ( $I_2$ ,  $I_3$  and  $I_4$  in SProcess) among the different small ICs  $I_n$  with  $n < 10$  studied in literature [82].  $\{311\}$  and FDLs extended defects are modelled using moments approach [83–85] with two moments generally considered: the concentration of interstitials (in  $\text{cm}^{-3}$ ) in the defects and the density of defects (in  $\text{cm}^{-3}$ ).

Dopant activation and deactivation mechanisms during thermal annealing are modelled using small dopant-point defect clusters [86], as for example in SProcess: boron clusters ( $B_2$ ,  $B_2I$ ,  $B_2I_2$ ,  $B_3I$ ,  $B_3I_2$  and  $B_3I_3$ ) and arsenic clusters ( $As_2$ ,  $As_2V$ ,  $As_3$ ,  $As_3V$ ,  $As_4$  and  $As_4V$ ). Another possible cause of dopant deactivation is their interaction with interstitial EOR defects as already observed for boron trapping at the boundaries or EOR defects ( $\{311\}$ s and FDLs) [87, 88].

As already discussed in 1.4.2, in association with dopant implantation, non-doping impurities co-implantation can be carried out in order to reduce point defect super-saturation and limit their diffusion. For instance carbon interstitial clusters reduce interstitials super-saturation and corresponding dopant TED [55, 56, 89]. Fluorine-vacancy and fluorine-interstitial clusters [58, 90] have also the same effect on interstitials super-saturation reduction.

#### 1.5.1.2 Junction leakage current models

Considering leakage currents modelling, the different GR mechanisms are included in advanced device simulators [21]. Details on advanced GR models can be found in [19] and references therein.

First of all, SRH GR mechanisms can be modelled, where minority carriers lifetimes can be both dopant concentration [91, 92] and temperature dependent [93]. Within the SRH mechanism, traps deep energy level(s), nature (donor, acceptor, trap or GR center) and cross section capture rates can be defined. In addition, the exact spatial localization of traps can be defined using for instance a process simulation field such as EOR defects concentration.

BBT GR mechanisms are modelled in highly doped and abrupt p-n junctions. In order to include the field assisted BBT GR mechanism, a simple field dependent GR term can be added [94], and phonon assisted tunnelling can also be included for more complex models [19, 95]. For highly doped 2D and 3D junctions, with direction dependent tunnelling mechanisms, non local tunnelling models [96] can also be used.

Similarly, TAT can be modelled taking into account the field effect [94] but also the phonons in more advanced models [19, 97]. Non local tunnelling can also be included in the TAT models.

### 1.5.2 Beyond state-of-the-art

Following the short summary of state-of-the-art process and junction leakage current TCAD models presented respectively in 1.5.1.1 and 1.5.1.2, several missing models were identified. The development of the new models is the goal of the PhD thesis. The main objective to extend the capabilities of TCAD models to the prediction of alternative doping processes and corresponding leakage currents. Our results are expected to increase TCAD predictability for core CMOS devices such as short channel MOS transistors and mainly for CMOS derivatives such as advanced CMOS image sensors with both FSI and BSI schemes.

The different modelling challenges can be summarized in two main research activities:

1. Alternative USJs formation techniques: advanced CMOS technologies and mainly BSI CMOS image sensors require the use of alternative doping techniques on both implantation and annealing parts in order to improve their electrical features such as reducing dark current sources. The first challenge concerns doping at the different oxide/silicon interfaces of CMOS image sensors in order to reduce  $I_{\text{dark}}$ . Concerning oxide/silicon interfaces, a 3D conformal doping is needed for DTIs. PIH is the main industrial technique that is currently available for conformal doping. In addition to modelling the conformal aspect of PIH, the resulting dopant profile leads to high dopant concentrations near the surface region, largely above dopant solubility limits. Therefore, new high dopant and point defects concentrations mechanisms may occur and lead to additional modelling efforts presented in chapter 2. The second challenge is modelling LTA processes (1.4.3) used in BSI image sensors, where a dopant activation is required at the backside of the image sensors, while preserving the integrity of frontside active regions already present in the structure. Several physical mechanisms have to be taken into account during the LTA, such as the temporal and spatial temperature field evolution, LPE, but also dopant diffusion in liquid and its segregation at the liquid/solid interface.
2. Chemical species diffusion in multi-materials stacks: in addition to classical dopant diffusion taking place in silicon, additional dopant but also other chemical species diffusion and transfer between neighbouring materials may take place during annealing. These diffusion and transfer mechanisms have an impact on devices electrical behaviour and therefore cannot be neglected for predictive TCAD simulations. In chapter 3, two different PhD results on such mechanisms will be presented. The first example concerns a dopant species boron and its diffusion in nitride/oxide/silicon stacks used for instance in spacer materials (1.2.3.3) or in ONO SOI of BSI CMOS image sensors (1.3.3.2). The second example concerns a non doping species lanthanum and its diffusion in advanced high-k stacks following thermal annealing, which has an impact on  $V_t$  shifts in n-MOS transistors.

The different challenges identified above resulted in several new models developed in the frame of ATEMox project [98]. The PhD thesis carried out in association with STMicroelectronics Crolles and LAAS CNRS Toulouse France mainly focused on these challenges. The resulting set of models was tested on device structures of MOS transistors, FSI and BSI CMOS image sensors used in advanced CMOS technologies, and corresponding process and device simulation results will be presented in chapter 4.

## 1.6 Conclusion

The aim of this chapter was to introduce the needed background for the PhD results. The MOS transistor was introduced, including its main components: p-n source/drain junctions and MOS capacitance. Different MOS transistor operation regimes were presented followed by its main miniaturization

challenges in the frame of advanced CMOS technology processes. In addition to MOS transistors considered as core CMOS “More Moore” elements, CMOS image sensors belonging to derivative elements from “More than Morre” category were presented. After reminding CMOS image sensors main operation regimes and features, both FEOL and BEOL process parts of CMOS image sensors were detailed. Following MOS transistors and CMOS image sensors description, the need for advanced process techniques was identified for both miniaturization and diversification requirements for CMOS based devices. Considering doping techniques, after a summary of main physical mechanisms occurring during ion implantation and thermal annealing, process solutions existing on the industrial level were given for the implantation part and thermal annealing part. In the frame of advanced CMOS technologies challenges and corresponding fabrication process solutions, TCAD modelling becomes mandatory for technologies development cost and time reduction. Silicon level TCAD modelling was presented, with a reminder of state-of-the-art TCAD models available at the beginning of the PhD thesis, including process models and leakage current models. This TCAD models listing allowed us to evidence the main missing models for predictive CMOS based devices modelling including MOS transistors, but also FSI and BSI CMOS image sensors. In the frame of the PhD thesis and ATE-MOX European project, two main modelling challenges were identified: alternative USJs formation techniques and chemical species diffusion in multi-materials stacks. Therefore, PIII alternative doping technique and its resulting physical mechanisms due to high doping concentrations will be presented in chapter 2. Two examples of chemical species diffusion in multi-layer materials stacks such as MOS transistors gate stacks or ONO SOI stack in BSI CMOS image sensors, will be presented in chapter 3. Finally the different new models developed in the frame of the PhD will be evaluated in chapter 4 on CMOS based devices, including MOS transistors, FSI and BSI CMOS image sensors.

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## Chapter 2

# Implantation-induced defects and their impact on dopant diffusion and activation

### 2.1 Introduction

The race for highly doped ultra-shallow junctions (USJs) in advanced CMOS technologies and the need for both ultra low energy (sub-keV) and high implantation doses ( $\geq 10^{14} \text{ cm}^{-2}$ ) quickly showed the limits of traditional beam-line implantation. In the frame of ATEMox project [1], several alternative doping techniques like plasma immersion ion implantation (PIII), cocktail implants, laser annealing and low-temperature implantation were studied, including experimental investigation and modelling. These doping techniques have very interesting applications in both core CMOS more Moore applications and diversified CMOS derivatives "more than Moore" applications [2], as defined by the International Technology Roadmap for Semiconductors (ITRS) 2011.

In the first part of this chapter, we will emphasize the work on plasma implantation during the PhD thesis. After reminding the PIII technique in section 2.2, we will describe the investigation of  $\text{BF}_3$  plasma implanted  $p^+/n$  USJs dedicated experiments and the corresponding simulations using default advanced process models [3] in section 2.3. These experiments will result in the observation of large boron interstitial clusters (BICs) lying in (001) crystalline plane for the different annealed samples whose description is mandatory for a correct modelling of diffusion and activation in high dose implanted samples. Thus, section 2.4 will be dedicated to the development of a large BICs (LBICs) continuum model based on moments approach. The model will be calibrated thanks to dedicated traditional beam-line implants and then tested on other beam-line implanted samples and on the  $\text{BF}_3$  PIII annealed samples.

### 2.2 Plasma Immersion Ion Implantation (PIII)

PIII technique is a promising alternative for highly doped USJs where contrarily to beam-line implantation, the ions plasma source is directly in contact with the implanted sample [4]. Different plasmas are used for implantation in industrial applications such as  $\text{AsH}_3$  (arsenic) or  $\text{PH}_3$  (phosphorus) for n doping and  $\text{B}_2\text{H}_6$  (boron) or  $\text{BF}_3$  (boron) for p doping [5].  $\text{BF}_3$  is currently used in  $p^+/n$  USJs and will be investigated in this chapter using the PULSION<sup>®</sup> plasma doping tool [6, 7] from Ion Beam Services (IBS) in Rousset France. The doping tool is a classical PIII one described in details in [6–8] and will be presented in this section.

Let us remind that plasma is the fourth state of matter in addition to solid, liquid and gas and is by far the most commonly observed state in the universe. Plasmas are typically composed of ionized atoms or molecules and electrons, but may also include neutral species or non-matter particles such as photons. Plasmas can be found in a huge variety of natural and artificial physical systems with variations in electronic density  $n_{e-}$  and temperature  $T_{e-}$  of several orders of magnitude. Microelectronics industry is mainly interested in non-equilibrium plasma discharges for materials processing generally used for etching, deposition or PIII operations. A complete review of the physics of these plasma discharges is given in [9] and they are characterized by low pressure ( $p \approx 1$  mTorr to 1 Torr) and electronic density ( $n_{e-} \approx 10^8$ - $10^{13}$  cm $^{-3}$ ). In addition, the electronic temperature is in the 1-10 eV ( $10^4$ - $10^5$  K) range, much higher than the ions temperature  $T_i$  ( $T_{e-} \gg T_i$ ).

In Fig. 2.1, a very simplified version of the plasma doping tool is presented. The plasma tool has a 4 m $^2$  surface [8] with a chamber under vacuum where the ions are to be implanted. Depending on the desired species to be implanted, different gases are introduced in the top of the chamber as we can see for the BF $_3$  plasma in our case (Fig. 2.1a). The sample or wafer to be implanted is localized in the center of the chamber, positioned on a sample holder and completely immersed in the plasma environment of the chamber. The BF $_3$  precursor gas is ionized and the BF $_3$  plasma is formed thanks to a radio frequency (RF) generator at the top gas entry of the chamber (not shown here) which allows forming high electronic density  $n_{e-}$  plasmas ( $\geq 10^{11}$  cm $^{-3}$ ). Once the plasma is created, different ions are formed in the chamber. In order to implant the ions in the sample, negative bias pulses  $V_0$  are applied on the sample holder or cathode as shown in Fig. 2.1b. Positive ions in the plasma are thus attracted to the sample holder. In the meantime, electrons resulting from the different species ionization are attracted to the top walls of the plasma chamber or anode. Given the lower mass of electrons in comparison to positive ions, electrons velocity is higher than the positive ions one in the vicinity of the sample surface. While ions are localized in the region near the sample surface, this same region will be depleted from electrons and a plasma sheath with a given thickness containing a uniform distribution of positive ions is formed around the sample. The electrical field in the plasma sheath accelerates the ions, which are then implanted in the sample. Following this implantation step, positive ions density within the sheath is reduced and thus the plasma sheath thickness increases in the direction of the anode. Other ions from the top of the chamber are then attracted to the sample and the cycle with the negative bias pulse can be repeated as much as needed depending on the desired dopant dose.

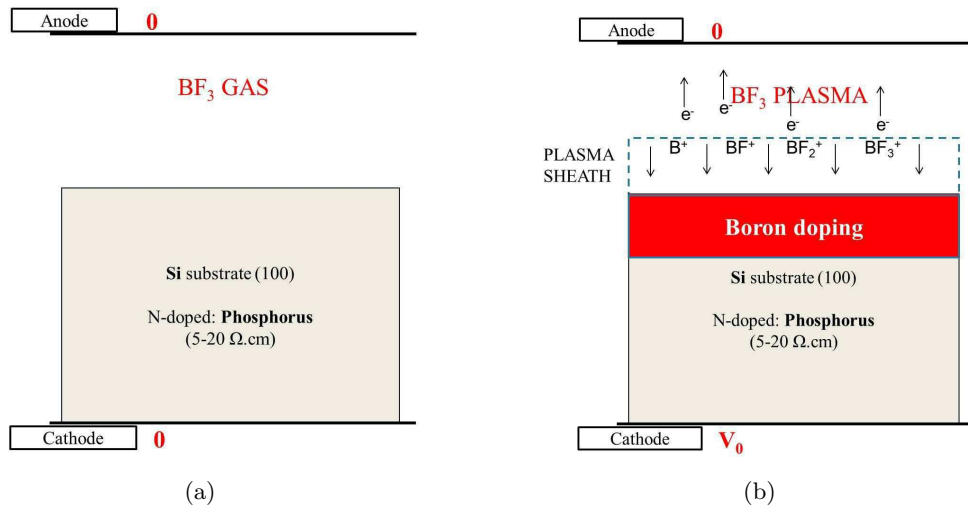


Figure 2.1: PULSION $^{\text{®}}$  plasma doping tool characteristics: (a) at zero voltage and (b) with applied negative voltage  $V_0$  at the cathode connected to the sample holder.

In comparison to beam-line implantation, PIII has specific characteristics to be kept in mind as we will see in next section 2.3:

- Multi-species implant: while in traditional beam-line implantation, the mass selection leads to a unique ion implantation in the sample, when ionizing a  $\text{BF}_3$  gas, several ionized species present in the plasma ( $\text{B}^+$ ,  $\text{BF}^+$ ,  $\text{BF}_2^+$  and  $\text{BF}_3^+$ ) will be implanted in silicon [10]. This multi-species aspect of plasma implants makes their modelling quite difficult and some assumptions have to be made in order to reproduce  $\text{BF}_3$  as implanted SIMS profiles as we will see in sub-section 2.3.1.
- Multi-energetic implant: when the plasma ions are accelerated within the sheath (Fig. 2.1b), they will undergo several collisions and thus an important fraction of the ions will be implanted at an energy lower than the one applied between the anode and the cathode. In addition, sheath dynamics during the implant leads to an energy distribution of implanted species. This is valid in collision-less sheath [11] where ions mean free path is higher than the sheath thickness, but also in highly collisional plasma sheath [12]. This multi-energetic aspect of plasma implants can also be due to the neutrals formed following the different ions collisions within the sheath [13].
- Multi-angle implant: increasing the pressure in the plasma chamber ( $10^{-2}$  to 1 Torr) leads to more ions collisions within the plasma sheath. Thus, the different ions collisions and the corresponding ions direction modification and energy exchange lead to an angular distribution of the ions. This aspect can be used for three dimensional conformal doping as we will see in chapter 4.

Following the short description of PIII in this section, we will present our experimental and modelling investigation of  $\text{BF}_3$  plasma implanted p+/n USJs in the frame of the PhD work and the ATEMOX project [1] in next section 2.3.

## 2.3 Experimental investigation and modelling of $\text{BF}_3$ plasma implanted p+/n USJs

In this section, we present our experimental and modelling investigation of dedicated  $\text{BF}_3$  plasma implanted p+/n USJs. In 2.3.1, details of the different experiments will be given. Sub-section 2.3.2 will deal with the investigation of implantation and amorphization when using  $\text{BF}_3$  PIII followed by the investigation of dopant diffusion and electrical activation during subsequent thermal anneals (sub-section 2.3.3).

### 2.3.1 $\text{BF}_3$ PIII dedicated samples

Dedicated  $\text{BF}_3$  plasma implanted samples were designed in order to investigate the specific characteristics of PIII and their TCAD modelling including implantation, amorphization, dopant diffusion and electrical activation. The starting samples are several 300 mm silicon wafers with an n-type phosphorus doping ( $5\text{-}20\ \Omega\cdot\text{cm}$ ) and (100) crystalline orientation. The samples were implanted by a  $\text{BF}_3$  plasma using PULSION<sup>®</sup> plasma doping tool [7] shown in Fig. 2.1. Two negative voltages  $V_0$  (Fig. 2.1b) of 0.5 kV (low energy) and 10 kV (high energy) were used, each one with two doses of  $5.10^{14}$  (medium dose) and  $5.10^{15}\ \text{cm}^{-2}$  (high dose). We should notice that in these experiments and as for traditional beam-line implantation, the dose was calculated by integrating the total implantation current.

The different implanted samples are summarized in table 2.1. After the plasma implants and in order to investigate diffusion and electrical activation related physical phenomena when using a PIII, samples from high energy/high dose category ( $\text{BF}_3$  10 kV,  $5.10^{15}\ \text{cm}^{-2}$ ) were cut and annealed at different temperatures and times. A high energy was chosen in these studies in order to localize the

junction far from the surface silicon/oxide interface and therefore minimize its impact on the junction electrical activation. The high dose was chosen in order to be closer to high boron doping required in advanced USJs. The thermal anneals used a rapid thermal anneal (RTA) system from Fraunhofer IISB<sup>1</sup>. The temperature/gas flow process of these anneals is the following:

1. Cleaning step during 5 min at room temperature in a N<sub>2</sub> ambient with a 15 l(Liters)/min gas flow.
2. Pre-heat step with a ramp-up from room temperature to 400°C in a N<sub>2</sub> ambient with a 5 l/min gas flow.
3. Heat-up step using a temperature ramp-up in a N<sub>2</sub> ambient with a 4 l/min gas flow with the following characteristics for the different annealed samples summarized in table 2.1:
  - 400 to 800°C ramp-up during 18 s for the 800°C 10 s , 1 and 10 min samples.
  - 400 to 900°C ramp-up during 24 s for the 900°C 10 s , 1 and 10 min samples.
  - 400 to 1065°C ramp-up during 32 s for the 1065°C 1s sample
4. Plateau step with a constant temperature and a given duration in a N<sub>2</sub> ambient with a 3 l/min gas flow, depending on the considered sample.
5. Cooling down steps with a ramp-down that is the exact opposite of the heat-up step in N<sub>2</sub> ambient with a 3 l/min gas flow, followed by a second ramp-down from 400 to 350°C in a N<sub>2</sub> ambient with a 15 l/min gas flow.

All as-implanted and annealed samples of table 2.1 were characterized by SIMS at Probion Analysis<sup>2</sup> using a 1 keV O<sub>2</sub><sup>+</sup> tilted beam on 200 x 200 μm samples in order to extract boron and fluorine total concentrations versus depth in silicon by measuring the intensities of <sup>10</sup>B<sup>+</sup> and <sup>11</sup>B<sup>+</sup> positively charged isotopes for boron and the <sup>19</sup>F<sup>+</sup> positively charged isotope for fluorine. Transmission electron microscopy in cross section view were made on the different as-implanted samples of table 2.1 in order to extract amorphization depths generated by the different BF<sub>3</sub> plasma implants. Considering the annealed samples, cross section and plan view images were carried out in order to evaluate the EOR defects survival following the different thermal budgets (excluding 800°C 10 s and 1 min). Finally, in order to investigate the electrical activation in BF<sub>3</sub> PIII following the different thermal budgets, Hall effect measurements described in [14, 15] were made and sheet resistance values in addition to Hall mobility and active boron dose were extracted on the p+/n BF<sub>3</sub> USJs. The different experiments on the PIII samples are summarized in table 2.1.

The results relative to these experiments were studied and published in [16, 17], as we will see in next sub-sections 2.3.2 and 2.3.3 where we will present respectively our results on implantation-induced amorphization and dopant diffusion-electrical activation in BF<sub>3</sub> PIII.

### 2.3.2 Implantation and amorphization in BF<sub>3</sub> PIII

SIMS implanted profiles of table 2.1 for boron and fluorine following the BF<sub>3</sub> PIII at 0.5 and 10 kV negative voltage V<sub>0</sub> acceleration are shown respectively in Fig. 2.2a and 2.2b. Typical triangular profiles (in log scale) of plasma implants are observed for both boron and fluorine leading to very high concentrations ( $\geq 10^{20}$  cm<sup>-3</sup>) near the silicon/oxide interface. Triangular shapes are due to the ions energy distribution and depend on the plasma sheath dynamics during the negative voltage V<sub>0</sub>

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<sup>2</sup>Probion Analysis 37 rue de Fontenay 92220 Bagneux, France

Table 2.1: Summary of the different  $\text{BF}_3$  PIII samples and corresponding experimental measurements presented in this chapter.

Sample	SIMS	Hall effect measurements	TEM
$\text{BF}_3$ 0.5 kV $5.10^{14} \text{ cm}^{-2}$	x		x
$\text{BF}_3$ 0.5 kV $5.10^{15} \text{ cm}^{-2}$	x		x
$\text{BF}_3$ 10 kV $5.10^{14} \text{ cm}^{-2}$	x		x
$\text{BF}_3$ 10 kV $5.10^{15} \text{ cm}^{-2}$	x		x
$\text{BF}_3$ 10 kV $5.10^{15} \text{ cm}^{-2}$ - $800^\circ\text{C}$ 10 s	x	x	
$\text{BF}_3$ 10 kV $5.10^{15} \text{ cm}^{-2}$ - $800^\circ\text{C}$ 1 min	x	x	
$\text{BF}_3$ 10 kV $5.10^{15} \text{ cm}^{-2}$ - $800^\circ\text{C}$ 10 min	x	x	x
$\text{BF}_3$ 10 kV $5.10^{15} \text{ cm}^{-2}$ - $900^\circ\text{C}$ 10 s	x	x	
$\text{BF}_3$ 10 kV $5.10^{15} \text{ cm}^{-2}$ - $900^\circ\text{C}$ 1 min	x	x	x
$\text{BF}_3$ 10 kV $5.10^{15} \text{ cm}^{-2}$ - $900^\circ\text{C}$ 10 min	x	x	x
$\text{BF}_3$ 10 kV $5.10^{15} \text{ cm}^{-2}$ - $1065^\circ\text{C}$ 1 s	x	x	x

pulse (Fig. 2.1b). The majority of ions are implanted at low energies [18]. Depending on the plasma conditions, deposition and sputtering may also occur leading to high concentrations at the surface. In addition to the multi-energetic aspect of  $\text{BF}_3$  plasma implants already presented in section 2.2, the multi-species aspect was already observed by Godet et al. [10] where in their plasma implantation conditions, several species are implanted during  $\text{BF}_3$  PIII, with a main  $\text{BF}_2^+$  component. In our case, the different species distributions during the  $\text{BF}_3$  PIII were not measured. Thus for simplification, we will assume the implantation of a single  $\text{BF}_3^+$  positive ion. The multi-angular aspect of plasma implants cannot be evaluated on these one dimensional (1D) structures. In chapter 4 we will give some examples of devices where plasma conformal doping is used.

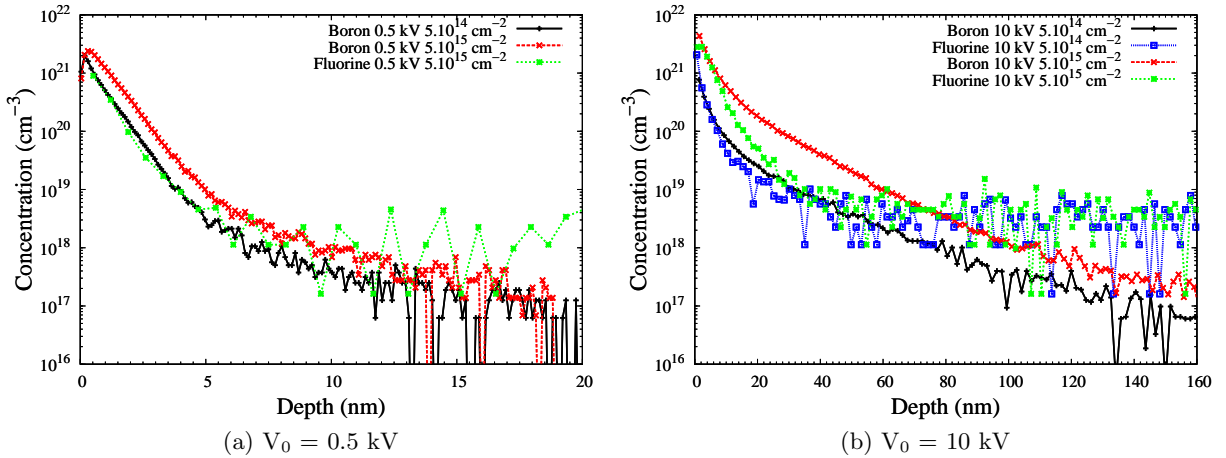


Figure 2.2: SIMS as implanted profiles for (a) 0.5 kV  $\text{BF}_3$  plasma acceleration voltage for boron at  $5.10^{14} \text{ cm}^{-2}$  and boron and fluorine at  $5.10^{15} \text{ cm}^{-2}$  and (b) for 10 kV  $\text{BF}_3$  plasma acceleration voltage for boron and fluorine at  $5.10^{14}$  and  $5.10^{15} \text{ cm}^{-2}$ .

Modelling  $\text{BF}_3$  PIII on these 1D SIMS structures has to include both the multi-energetic aspect and multi-species aspect. We used the commercial TCAD tool SProcess [3] for our simulations. The implanted profiles were simulated using the implantation Monte Carlo code Sentaurus Monte Carlo



(MC) [3, 19].  $\text{BF}_3^+$  ionized molecule implantation is not included in the simulator and thus simple boron  $\text{B}^+$  and fluorine  $\text{F}^+$  ions were implanted separately in our simulations in order to reproduce the  $\text{BF}_3$  PIII profiles. Mass correcting factors in front of the plasma implant acceleration voltage were added with the respective values of  $M(\text{B})/M(\text{BF}_3^+)$  and  $M(\text{F})/M(\text{BF}_3^+)$  where  $M$  is the molar mass of the corresponding species.

When we started our work on plasma implantation modelling, the only available energy distribution in SProcess within Sentaurus MC code was a simple Gaussian energy distribution [3] given by:

$$f(E) = \frac{1}{\sigma_E \sqrt{2\pi}} e^{-\frac{1}{2} \left( \frac{E-E_0}{\sigma_E} \right)^2} \quad (2.1)$$

where  $E_0 = V_0$  is the mean energy of the plasma implant considering the acceleration voltage  $V_0$ ,  $\sigma_E$  the standard deviation of the Gaussian distribution and  $f$  the probability distribution verifies the normalisation condition  $\int_0^\infty f(E) dE = 1$ . However, the Gaussian energy distribution of equation 2.1 is a simplistic approximation to model plasma implants and is in contradiction with main literature experimental and theoretical results [10–13]. In the frame of the ATEMox project, Burenkov et al. [20] considered a more realistic double exponential (2-exp) energy distribution developed in the Monte Carlo code MCSIM [21]:

$$f(E) = A e^{-aE} + B e^{-bE} \quad (2.2)$$

where  $A$ ,  $B$ ,  $a$  and  $b$  are the four calibration parameters of the 2-exp energy distribution with  $A/a + B/b = 1$  in order to verify the normalization condition. The energy distribution of equation 2.2 allows to modulate the low and high energy parts of the plasma implanted ions and successfully reproduces  $\text{BF}_3$  plasma implants with 6.5 kV applied voltage and doses ranging from  $1.10^{15}$  to  $1.10^{17} \text{ cm}^{-2}$  [20]. Indeed, boron and fluorine as-implanted profiles can be easily reproduced when using the 2-exp distribution whether considering a single species implant ( $\text{BF}_3^+$  in our case) or multi-species implants. It can be argued that the 2-exp energy distribution is non-physical due to the extension of exponential functions to infinite energies. However, the exponential functions quickly vanish in the high energy part following adequate choice of calibration parameters. Burenkov et al. also considered a more physical energy distribution [22] where implanted ions energy is lower than  $E_0 = q_{\text{ion}} V_0$  where  $q_{\text{ion}}$  is the ion electrical charge. The corresponding energy distribution extracted from [23] is the following:

$$f(E) = \frac{5}{6E_0} \left( \frac{E}{E_0} \right)^{-1/6}, E \in [0, E_0] \quad (2.3)$$

Energy distribution in equation 2.3 is defined for  $E \in [0, E_0]$  and also verifies normalization condition. In our simulations, we will use the 2-exp energy distribution of equation 2.2 with a simple  $\text{BF}_3^+$  ion implantation.

In order to integrate the 2-exp energy distribution in SProcess, we used the inverse cumulative distribution function (CDF) method [24]. Inverse CDF uses the following procedure in order to generate random energies following a given probability distribution  $f$ :

- Consider an energy probability distribution  $f(E)$
- Calculate the primitive  $F(E)$  of  $f(E)$  known as the CDF and given by:  $F(E) = \int_0^E f(E) dE$ . In the case of the 2-exp energy distribution of equation 2.2,  $F(E) = \frac{A}{a} (1 - e^{-aE}) + \frac{B}{b} (1 - e^{-bE})$ .
- $F(E)$  is a continuous and monotonous (increasing) function of  $E$  and thus has an inverse function  $F^{-1}(E)$  called inverse CDF. In addition the CDF has the following property:  $F(E) \xrightarrow{E \rightarrow \infty} 1$  (probability distribution normalization).

- It can be mathematically demonstrated [24] that the CDF  $F$  follows a uniform probability distribution  $U(0,1)$  between 0 and 1:  $F(E) = U \Rightarrow E = F^{-1}(U)$  where  $U$  is a random number generated with the uniform law  $U(0,1)$ . Thus in order to generate energy values with a given distribution  $f(E)$  (2-exp distribution in our case), the following two steps have to be carried out:

1. Generate a random number  $u$  using a uniform distribution  $U(0,1)$
2. Calculate a random energy of the  $f(E)$  distribution using the inverse CDF:  $E = F^{-1}(u)$ . In the case of the 2-exp energy distribution considered in our case, inverse CDF cannot be calculated analytically, and thus 1<sup>st</sup> order Newton method was used in order to calculate the random energy using the following iterative procedure for steps  $n$  and  $n + 1$  ( $n$  integer):

$$E_{n+1} = E_n - \frac{F(E_n)}{F'(E_n)} = E_n - \frac{F(E_n)}{f(E_n)} \quad (2.4)$$

where the derivative of the CDF is  $F' = f$ . Iterative equation 2.4 is to be repeated in the code until a given integer rank  $N$  where  $|F(E_N) - y| < \epsilon$  where  $\epsilon$  is a fixed error.

3. The calculated energy  $E_N$  follows the 2-exp energy distribution  $f$ .
- The previous steps are repeated for each particle in Sentaurus MC code with energies randomly distributed using the 2-exp distribution  $f$ . By increasing the number of particles  $N_{\text{part}}$  and the corresponding randomly generated energies, the statistical accuracy of the simulated plasma implanted profiles is enhanced.

In our case, inverse CDF method described above has an interesting simulation accuracy/time trade-off and was applied to the 2-exp energy distribution that was calibrated for boron and fluorine implants data of table 2.1. The parameters values are given in table 2.2 for boron and fluorine and resulted in a good agreement for the different samples as shown in Fig. 2.3. For instance, in Fig. 2.4, we give energy distributions for the  $\text{BF}_3$  10 kV  $5.10^{15} \text{ cm}^{-2}$  PIII for  $N_{\text{part}} = 100000$  particles for both boron and fluorine, using inverse CDF method described above with the set of parameters of table 2.2.

Table 2.2: Boron and fluorine calibrated parameters of the 2-exp energy distribution of equation 2.2 with  $E_0$  the ion energy corresponding to the acceleration voltage  $V_0$ .

Parameter	a	b	A/a	B/b
Boron	$1.8/(M(\text{B})E_0/M(\text{BF}_3^+))$	$0.95/(M(\text{B})E_0/M(\text{BF}_3^+))$	0.88	0.12
Fluorine	$2.7/(M(\text{F})E_0/M(\text{BF}_3^+))$	$0.15/(M(\text{F})E_0/M(\text{BF}_3^+))$	0.88	0.12

Sentaurus MC plasma implantation simulations used cascades mode [3] in order to model damage generation by both boron and fluorine implanted atoms. The  $\text{BF}_3^+$  implanted species considered in our simulations is however not implemented in the simulator we use. Thus, in order to reproduce the damage generated by the  $\text{BF}_3^+$  ionized molecule, the boron damage multiplication factor  $d(\text{B})$  has been increased using the following formula:

$$d'(\text{B}) = \alpha(\phi_{\text{B}}) \frac{M(\text{BF}_3)}{M(\text{B})} d(\text{B}) \quad (2.5)$$

where  $d'(\text{B})$  is the modified damage multiplication factor and  $\alpha(\phi_{\text{B}}) = (\phi_{\text{B}} + 5.10^{14})/5.10^{14}$  is a fitting formula depending on the implant dose  $\phi_{\text{B}}$  for boron. A good agreement was found between TEM measured amorphous depths shown in Fig. 2.5 and TCAD simulations.

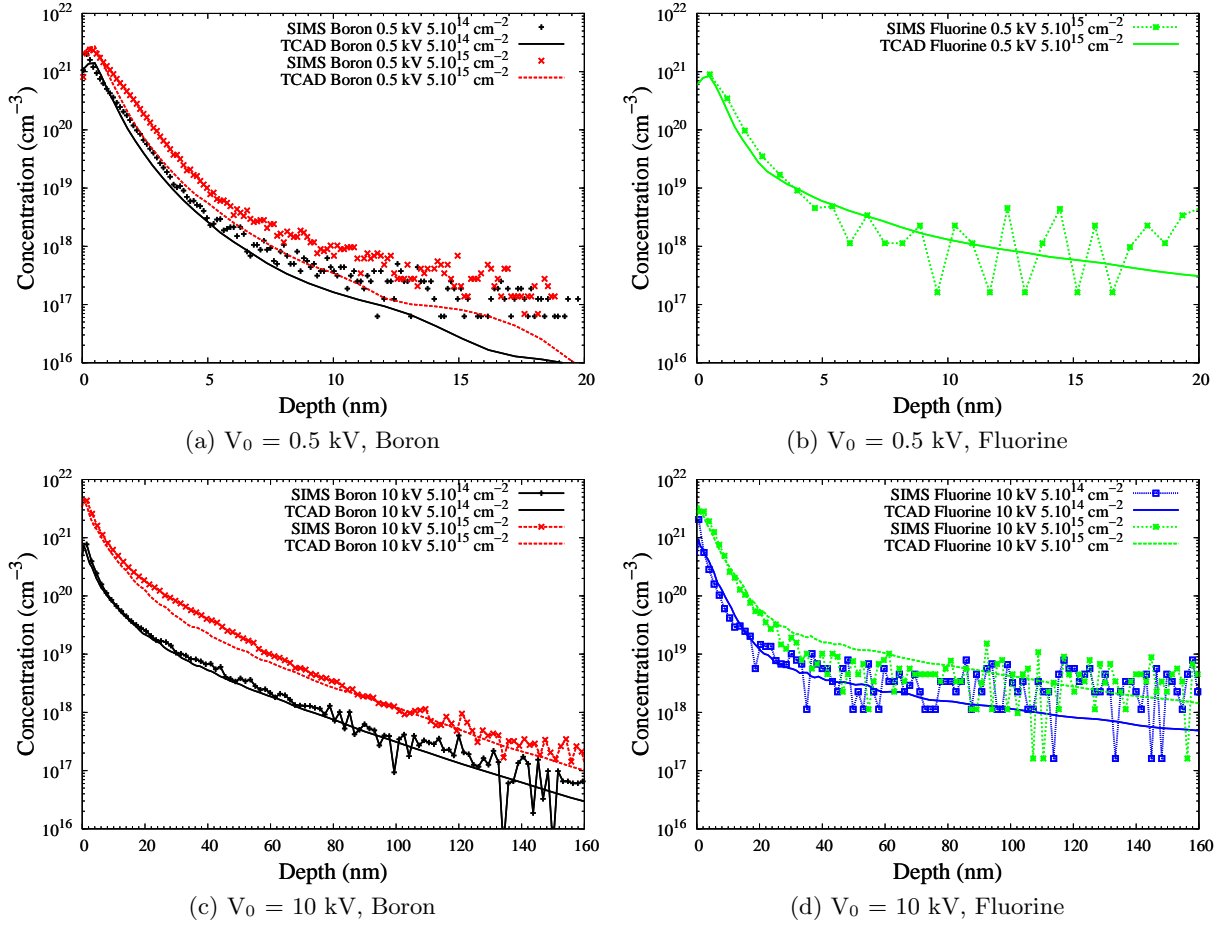


Figure 2.3: SIMS versus TCAD as implanted profiles using 2-exp energy distribution of equation 2.2 with the set of parameters of table 2.2 for 0.5 kV  $\text{BF}_3$  plasma acceleration voltage for (a) boron, (b) fluorine and for 10 kV  $\text{BF}_3$  plasma acceleration voltage for (c) boron and (d) fluorine.

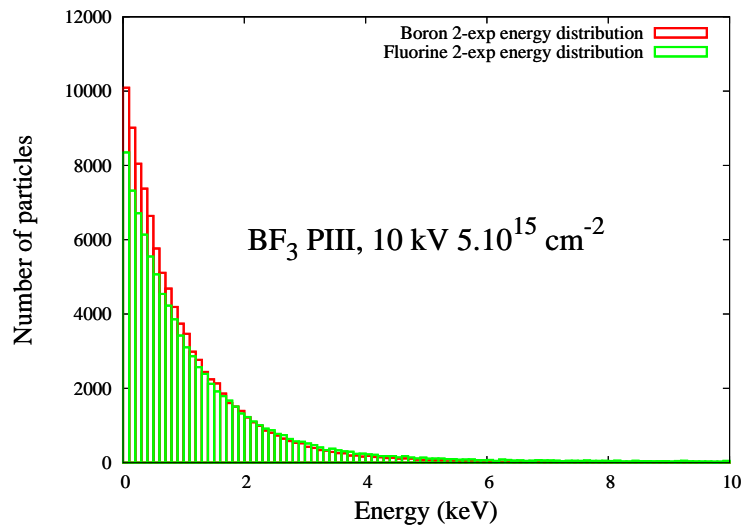


Figure 2.4: 2-exp energy distributions for the  $\text{BF}_3$  10 kV  $5.10^{15} \text{ cm}^{-2}$  PIII for  $N_{\text{part}} = 100000$  particles for both boron and fluorine using inverse CDF method and the set of parameters of table 2.2.

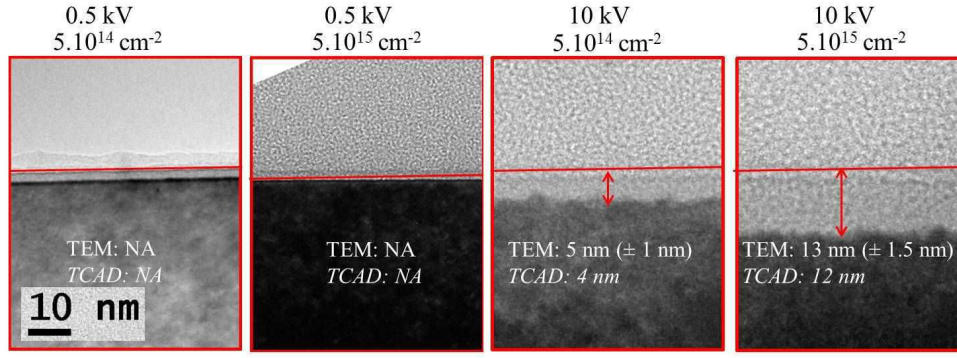


Figure 2.5: Amorphous depth from TEM measurements and TCAD simulations for the different PIII samples of table 2.1.

Once we successfully modelled implantation and amorphization in  $\text{BF}_3$  PIII samples, thermally annealed samples of table 2.1 were investigated in order to study dopant diffusion and electrical activation mechanisms. Corresponding results are given in next sub-section 2.3.3.

### 2.3.3 Dopants diffusion and electrical activation in $\text{BF}_3$ PIII

Following implantation and amorphization simulations,  $\text{BF}_3$  PIII diffused profiles were investigated. Boron SIMS profiles of the  $\text{BF}_3$  annealed samples at  $800^\circ\text{C}$  10 min,  $900^\circ\text{C}$  10 min and  $1065^\circ\text{C}$  1 s of table 2.1 are given in Fig. 2.6. Two main phenomena occur during anneal in all observed samples: boron tail diffusion and the formation of a boron peak below the post-implant A/C interface at 12 nm. The boron peak concentration is higher than boron equilibrium solubility in silicon at the given temperature [25] and is in an inactive precipitated form. In addition, a slight decrease of the peak concentration is observed when increasing the thermal budget at  $1065^\circ\text{C}$  1 s with a corresponding boron diffusion tail.

In order to investigate boron diffusion profiles in  $\text{BF}_3$  PIII including boron peak below the A/C interface, we modelled SIMS profiles of Fig. 2.6 using state-of-the-art TCAD diffusion and activation models in SProcess [3]. Diffusion models included boron and fluorine five-stream diffusion models [26]. Activation and precipitation models included small boron interstitial clusters [27], fluorine-interstitial and fluorine-vacancy clusters [28] and EOR defects models for small interstitial clusters [29],  $\{311\}$  and  $(111)$  [30] dislocation loops (DLs). Suspecting that boron peak below the A/C interface is due to a decoration of EOR  $\{311\}$  and  $(111)$  DLs by boron atoms, we also used boron trapping by EOR defects model [31]. Corresponding TCAD simulated results are given in Fig. 2.7. From Fig. 2.7a, a good agreement is found between SIMS and TCAD for the low thermal budget at  $800^\circ\text{C}$  10 min. However, simulations at high thermal budgets do not reproduce neither boron peak below the A/C interface, nor diffusion tail. Boron detailed profile is given in Fig. 2.7b, where boron diffusion tail is correctly reproduced, while boron peak below the A/C interface is not captured. With the process models used above, boron inactive peak below the A/C interface has three possible sources investigated in Fig. 2.7b for the  $900^\circ\text{C}$  10 min anneal:

- Boron trapping by  $\{311\}$  rod-like defects: no  $\{311\}$  defects were observed in our simulations for the  $900^\circ\text{C}$  10 min anneal, which is in agreement with literature results on interstitial EOR defects [32].
- Boron trapping by  $(111)$  DLs: boron decorating DLs concentration is shown in Fig. 2.7b and is very low to explain the boron peak below the A/C interface. This low boron concentration

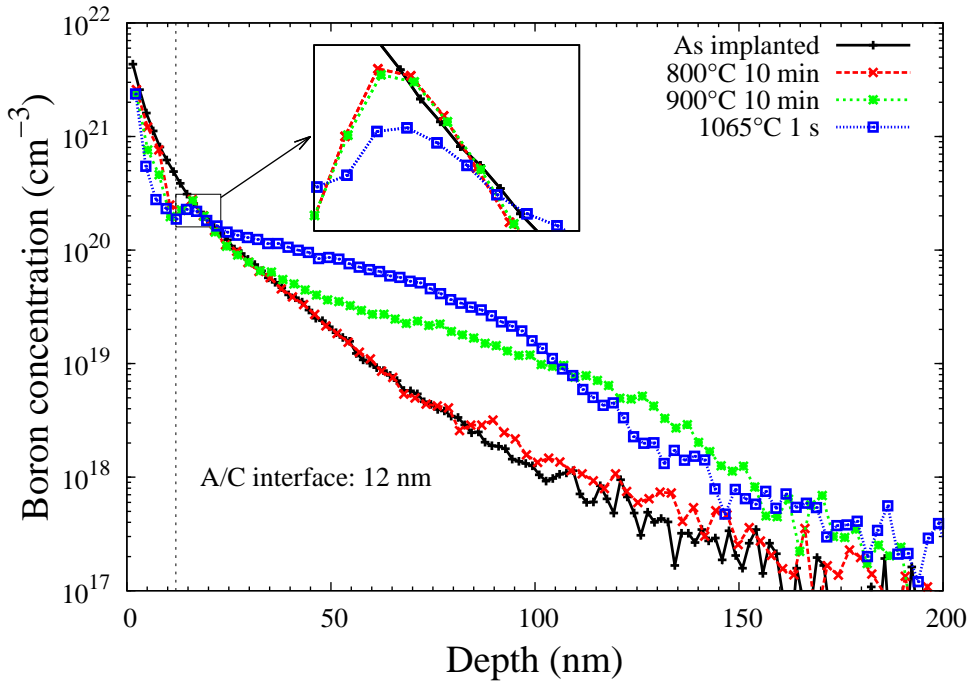


Figure 2.6: Boron SIMS profiles following a  $\text{BF}_3$  PIII at  $10 \text{ kV } 5 \cdot 10^{15} \text{ cm}^{-2}$  annealed at  $800^\circ\text{C}$  10 min,  $900^\circ\text{C}$  10 min and  $1065^\circ\text{C}$  1 s. A boron peak below the A/C interface is observed for the different thermal anneals.

decorating (111) DLs is expected given the low perimeter to surface ratio of dislocation loops [31], and its corresponding low capturing efficiency.

- Boron in small BICs: from our simulations in Fig. 2.7b, small BICs are localized near the oxide/silicon interface at the  $\text{BF}_3$  plasma as-implanted surface peak (Fig. 2.2b) and thus cannot explain boron peak below the A/C interface.

From simulation results shown in Fig. 2.7, default advanced TCAD models cannot explain boron peak below the A/C interface. Therefore, the annealed samples at  $800^\circ\text{C}$  and  $900^\circ\text{C}$  10 min of table 2.1 were investigated by cross-section and plan-view TEM analysis [17, 33] shown in Fig. 2.8. From cross section TEM images of Fig. 2.8a, no  $\{311\}$  defects were observed which is in agreement with our TCAD simulations of Fig. 2.7b. In addition to (111) DLs, several (001) DLs were observed below the A/C interface at the position of the B peak of SIMS results in Fig. 2.6. From literature results [34–36], such (001) DLs have been observed in experimental conditions where silicon is highly super-saturated ( $> 10^{20} \text{ cm}^{-3}$ ) with both boron and silicon interstitial atoms. These defects are called large boron interstitial clusters (LBICs) consisting of precipitates with hundreds to thousands of both boron and silicon interstitial atoms. The defects were also observed in plan view TEM with a  $[400]$  diffracting vector  $\mathbf{g}$  as shown in Fig. 2.8b.

In order to investigate the details of defects populations in the  $800^\circ\text{C}$  and  $900^\circ\text{C}$  10 min annealed samples, additional plan-view weak beam dark field (WBDF) TEM analysis were carried out for different diffracting vectors  $\mathbf{g}$  and both positive and negative deviation parameters. Three EOR defects categories investigated in [37] and summarized in table 2.3 could thus be extracted: D001 category with  $[001]$  Burgers vector corresponding to (001) crystalline plane LBICs, D101 category with four different Burgers vectors combinations corresponding to LBICs with a habit plane close to (001) but also to  $\{111\}$  interstitial perfect dislocation loops (PDLs) and D111 category corresponding to classical  $\{111\}$  interstitial dislocation loops. Even though the D001 defects were clearly identified as LBICs,



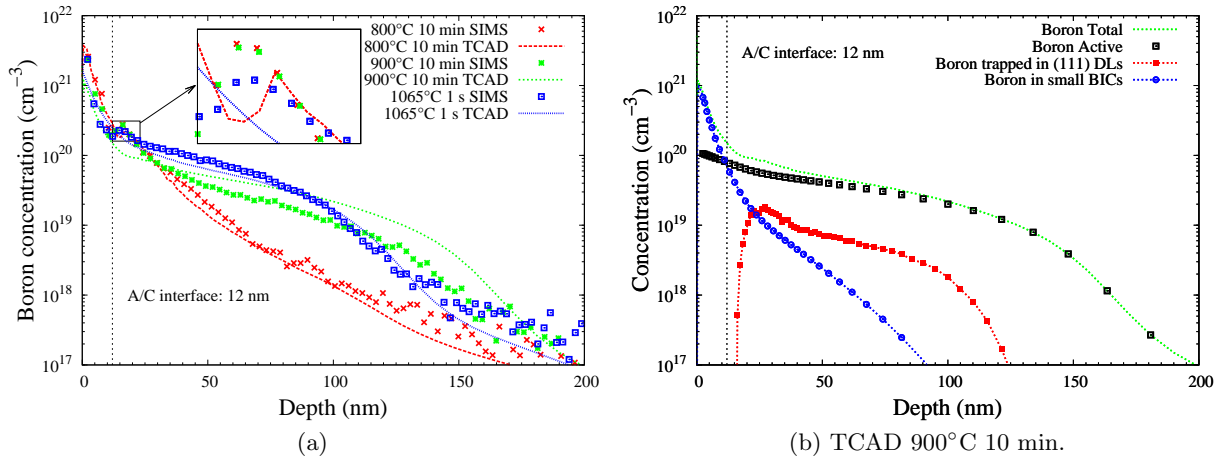


Figure 2.7: (a) Boron SIMS versus TCAD profiles using state-of-the-art SProcess models [3] following a  $\text{BF}_3$  PIII at  $10 \text{ kV } 5.10^{15} \text{ cm}^{-2}$  annealed at  $800^\circ\text{C}$  10 min,  $900^\circ\text{C}$  10 min and  $1065^\circ\text{C}$  1 s, and (b) details of boron concentration including total boron, active boron, boron in (111) DLs and small BICs for the  $900^\circ\text{C}$  10 min anneal.

the TEM investigation carried out here cannot distinguish LBICs from  $\{111\}$  interstitial PDLs within the D101 family. However, despite the ambiguity within the D101 family, LBICs presence is clearly confirmed with not less than 20% of LBICs for the  $900^\circ\text{C}$  10 min annealed sample. The different defects categories densities are given in Fig. 2.9 and a total defect density decrease is observed in agreement with Ostwald ripening mechanism. In the meantime and as expected the defect size projected on (001) plane increases from approximately 14 to 15 nm for D101 defects and from 12 to 19 nm for D111 defects for the respective 800 and  $900^\circ\text{C}$  10 min anneals.

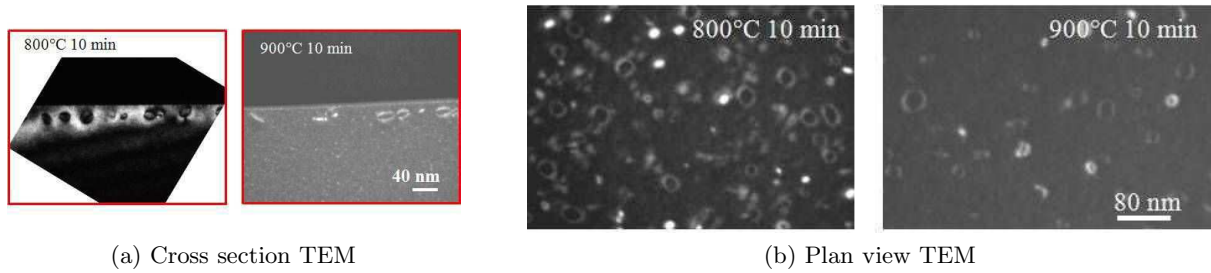


Figure 2.8: TEM (a) cross-section where (001) DLs corresponding to LBICs are observed below the A/C interface and (b) plan-view images with a  $[400]$  diffracting vector  $\mathbf{g}$  of the  $\text{BF}_3$  PIII samples at  $10 \text{ kV } 5.10^{15} \text{ cm}^{-2}$  and annealed at  $900^\circ\text{C}$  and  $900^\circ\text{C}$  10 min.

Current TCAD process models do not integrate LBICs forming during thermal anneals in high boron and silicon interstitials super-saturated silicon. Therefore, a clear disagreement between SIMS and TCAD results is observed for high thermal budgets, where TCAD misses both boron peak below the A/C interface and the diffusion tail. In addition, sheet resistance values extracted from Hall effect measurements were compared to simulations using boron's dependent mobility formula of Masetti et al. [38]. Boron active concentration included in the mobility formulas were obtained from TCAD simulations shown in Fig. 2.7. Corresponding results are shown in Fig. 2.10 where a disagreement is observed between Hall effect measurements and TCAD. Therefore, LBICs have to be included in TCAD models in order to reproduce both SIMS diffused profiles (Fig. 2.7) and electrical activation

Table 2.3: Observed EOR defects using TEM in the PIII  $\text{BF}_3$  at 10 kV  $5.10^{15} \text{ cm}^{-2}$  annealed at 800°C and 900°C during 10 min, including defect category, Burgers vectors and defect nature.

Category	Burgers vector <b>b</b>	Nature
D001	[001]	(001) LBICs
D101	[101] $[\bar{1}01]$ [011] $[0\bar{1}1]$ [110] $[\bar{1}10]$	close to (001) LBICs or {111} interstitial PDLs
D111	[111] $[\bar{1}\bar{1}\bar{1}]$ $[\bar{1}11]$ $[1\bar{1}1]$	{111} interstitial dislocation loops

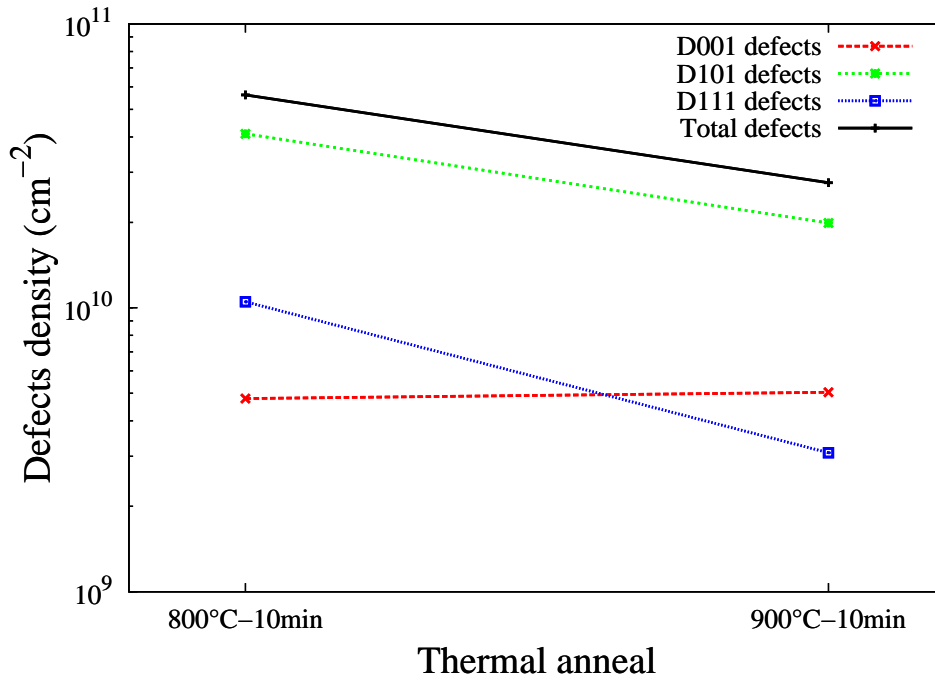


Figure 2.9: Defects density measured from TEM WBDF images for  $\text{BF}_3$  PIII at 10 kV  $5.10^{15} \text{ cm}^{-2}$  annealed at 800°C and 900°C 10 min including D001, D101, D111 defects(table 2.3) and total EOR defects.

extracted from Hall effect measurements (Fig. 2.10). Next section 2.4 will deal with the investigation of LBICs and the strategy built in order to develop a LBICs continuum TCAD model.

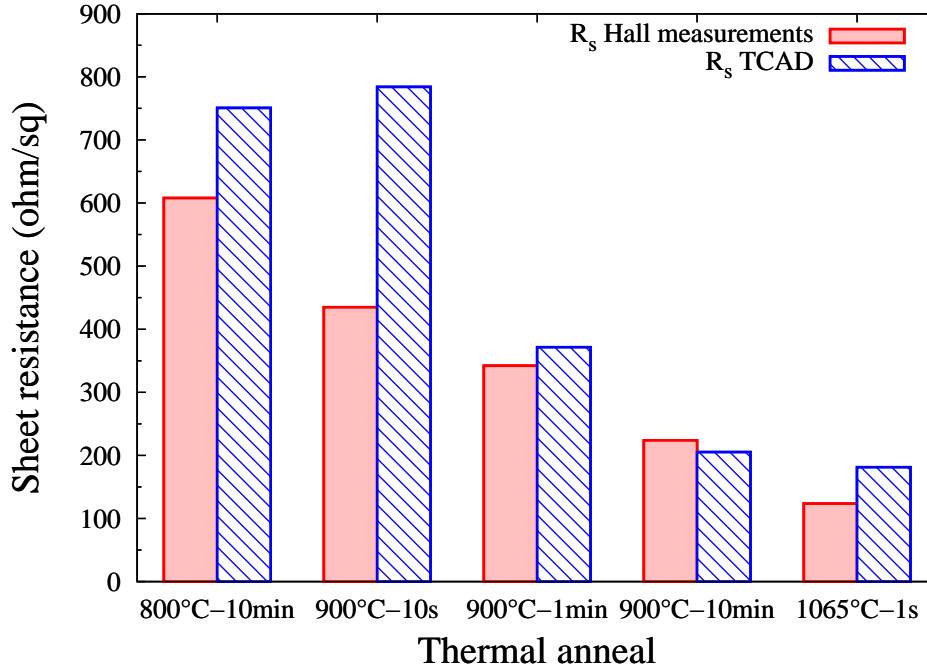


Figure 2.10: p+/n PIII  $\text{BF}_3$  junctions sheet resistance extracted from Hall effect measurements for different thermal anneals of table 2.1 compared to TCAD state-of-the-art process models.

## 2.4 High boron and interstitials super-saturation and large boron-interstitial clusters

In sub-section 2.3.3, LBICs were evidenced both from SIMS measurements with the boron peak below the A/C interface (Fig 2.6) and TEM cross section and plan view images showing (001) DLs (Fig 2.8). In sub-section 2.4.1, we will give the different literature data on LBICs in addition to current TCAD models for boron and silicon interstitials interactions, showing the need to develop a new LBICs TCAD model. LBICs continuum modelling will be presented in sub-section 2.4.2, where the model was evaluated thanks to simple high dose boron beam-line implants. Finally, the new model will be evaluated on the  $\text{BF}_3$  PIII data of section 2.3.

### 2.4.1 Introduction to large BICs

The use of high doses in boron implanted silicon raises several fundamental questions on the boron precipitation mechanisms in silicon. In such conditions observed using beam-line or plasma implantation, followed by thermal annealing, silicon is highly super-saturated with both boron and silicon interstitials concentrations exceeding  $10^{20} \text{ cm}^{-3}$ . The development of new characterization techniques such as APT and field ion microscopy [39, 40] led to new ways to observe boron in silicon at the atomic scale, improving the understanding of boron-silicon interactions. In addition, according to the ITRS, highly doped systems are among the modelling challenges for CMOS technology nodes beyond 14 nm [41].



In these conditions, largely above boron solid solubility limit in silicon [25], large boron precipitates containing boron and silicon interstitial atoms will form [34–36] following thermal annealing used for dopants activation. In several cases, these large boron precipitates also called in literature large BICs (LBICs) are (001) dislocation loops with hundreds to thousands of both boron and silicon interstitial atoms as observed by TEM [35, 37, 42], where it was seen that LBICs growth is similar to an Ostwald ripening mechanism. In addition to the density and size of LBICs investigated by TEM and thanks to recent advances in the APT technique [39], it is now possible to measure the chemical composition of the large BICs [43, 44]. Recent experimental results [45, 46] also showed that for sufficiently high thermal budgets, boron precipitates close to the stoichiometric stable boride phases such as  $\text{SiB}_3$  and  $\text{SiB}_4$  [47] seen in APT measurements may also form, corresponding to the (001) large BICs observed by TEM. The stability of these LBICs is in agreement with a previous study [48] showing that two BICs dissolution mechanisms take place during a thermal anneal: a fast mechanism associated to small boron clusters and a slow one associated to more complex clusters believed to be more stable.

Historically, the formation of small BICs with few boron and interstitial atoms already observed below boron solubility limit were the first clusters to be evidenced in literature from boron immobile peak on SIMS profiles [49]. Modeling the thermal evolution of such BICs and their corresponding boron deactivation was already carried out using a continuum approach [27, 50] with small BICs sizes and more recently [42] using a KMC approach. However, current models including small BICs models and EOR defects decoration by boron atoms [31] are not able to reproduce the formation of LBICs in conditions of high boron and silicon interstitials super-saturation as observed in our results on high dose  $\text{BF}_3$  plasma implantation [17]. Modeling all LBICs sizes in process TCAD simulators is quite expensive in terms of calculation time. Thus, in this work a large BICs continuum model [51] based on a moments approach already used for silicon end of range extended defects [30, 52], and more recently for voids modeling in helium implanted silicon [53] will be used in order to evaluate (001) large BICs evolution following thermal anneals. The model is integrated as add-on for a TCAD commercial simulator [3] in association with previous small BICs, small interstitial clusters (ICs) and EOR defects models.

### 2.4.2 Large BICs continuum modelling in silicon

When dealing with precipitates of different sizes ranging from two to thousands atoms, modeling all precipitates sizes can be very expensive from a computational aspect. Thus, moments approach based on low order moments can be an interesting and computationally efficient alternative. In previous applications of this method, precipitates exchange only one species: interstitials in the case of {311} defects and (111) dislocation loops [30, 52] and vacancies in the case of voids [53]. Precipitates interact with the mean super-saturation field surrounding them. The diffusion of the given species between the precipitates and the super-saturation field leads to the growth of large precipitates at the expense of smaller ones following an Ostwald ripening mechanism. In the case of (001) LBICs, a behavior close to an Ostwald ripening mechanism has also been verified [35, 54]. However, contrarily to previous examples, two different species, boron and silicon interstitial atoms, contribute to the precipitation mechanism in this case. The following three moments (in  $\text{cm}^{-3}$ ) will be considered in our model:

- Boron content in the LBICs:

$$C_{\text{B,LBICs}} = \sum n B_n I_m \quad (2.6)$$

- Silicon interstitials content in the LBICs:

$$C_{\text{I,LBICs}} = \sum m B_n I_m \quad (2.7)$$

- LBICs density:

$$D_{\text{LBICs}} = \sum B_n I_m \quad (2.8)$$

Following a high dose implantation step, silicon is highly super-saturated with boron and silicon interstitial atoms. At the end of the implantation and beginning of anneal step, several small ICs [55] and BICs are formed. In the same way as small ICs are the precursors for the formation of interstitial EOR defects [29, 30], small ICs and BICs are the precursors for the formation of LBICs. In this model, we chose  $I_2$  for small ICs and  $B_3I$  for small BICs. LBICs of different sizes and composition are then formed from the reaction of the precursors with diffusing free interstitials,  $I$ , and boron interstitial pairs,  $BI$ , as follows:



It should be noticed that the choice of the small clusters precursors is arbitrary and changing the precursors (such as  $I_3$  or  $B_2I$ ) would lead to the same simulation results after adequately calibrating the model's parameters. Also, we limit ourselves to two precursors in order to simplify the model's equations.

Fig. 2.11 is an atomistic view diagram describing boron and silicon interstitials interactions. In Fig. 2.11a, the diagram presents default TCAD SProcess models including small BICs formation and boron trapping by a (111) DL, where boron decorates only the boundaries of the defect. In Fig. 2.11b, the LBICs formation is represented with the different corresponding moments  $C_{B,LBICs}$ ,  $C_{I,LBICs}$  and  $D_{LBICs}$ .

LBICs are assumed to be disk-shaped dislocation loops, with a circular section and a fixed thickness (corresponding to an additional (001) Si plane inserted in the lattice, in agreement with previous experimental observations [35, 45, 54]). The (001) LBICs grow and increase in radius  $R_{LBICs}$  following the diffusion and reaction of  $I$  and  $BI$  at the loop periphery as shown in Fig. 2.11b. Contrarily to boron trapping at the boundaries of EOR defects (Fig. 2.11a), LBICs have equivalent content of boron and silicon interstitial atoms as observed experimentally [45] and as shown in Fig. 2.11b.

Following the same formalism used for (111) interstitial DLs [30], the different fields of the moment's model verify the following equations:

$$\begin{aligned} \frac{dC_{I,LBICs}}{dt} = & 2D(BI) \frac{A}{R_{eff}} \Big|_{BI,B_3I} BI.B_3I + 2D(I) \frac{A}{R_{eff}} \Big|_{I,B_3I} I.B_3I + 3D(BI) \frac{A}{R_{eff}} \Big|_{BI,I_2} BI.I_2 \\ & + k_{BI,LBICs} \cdot 2\pi^2 R_{LBICs} D(BI) (BI - C_{BI,LBICs}^*) D_{LBICs} \\ & + k_{I,LBICs} \cdot 2\pi^2 R_{LBICs} D(I) (I - f_{prec} C_{I,LBICs}^*) D_{LBICs} \quad (2.12) \end{aligned}$$

$$\begin{aligned} \frac{dC_{B,LBICs}}{dt} = & 4D(BI) \frac{A}{R_{eff}} \Big|_{BI,B_3I} BI.B_3I + 3D(I) \frac{A}{R_{eff}} \Big|_{I,B_3I} I.B_3I + D(BI) \frac{A}{R_{eff}} \Big|_{BI,I_2} BI.I_2 \\ & + k_{BI,LBICs} \cdot 2\pi^2 R_{LBICs} D(BI) (BI - C_{BI,LBICs}^*) D_{LBICs} \quad (2.13) \end{aligned}$$

$$\begin{aligned} \frac{dD_{LBICs}}{dt} = & D(BI) \frac{A}{R_{eff}} \Big|_{BI,B_3I} BI.B_3I + D(I) \frac{A}{R_{eff}} \Big|_{I,B_3I} I.B_3I + D(BI) \frac{A}{R_{eff}} \Big|_{BI,I_2} BI.I_2 \\ & - k_{I,LBICs} \cdot 2\pi^2 R_{LBICs} D(I) C_{I,LBICs}^* \frac{D_{LBICs}}{C_{I,LBICs}} D_{LBICs} \\ & - k_{BI,LBICs} \cdot 2\pi^2 R_{LBICs} D(BI) C_{BI,LBICs}^* \frac{D_{LBICs}}{C_{B,LBICs}} D_{LBICs} \quad (2.14) \end{aligned}$$

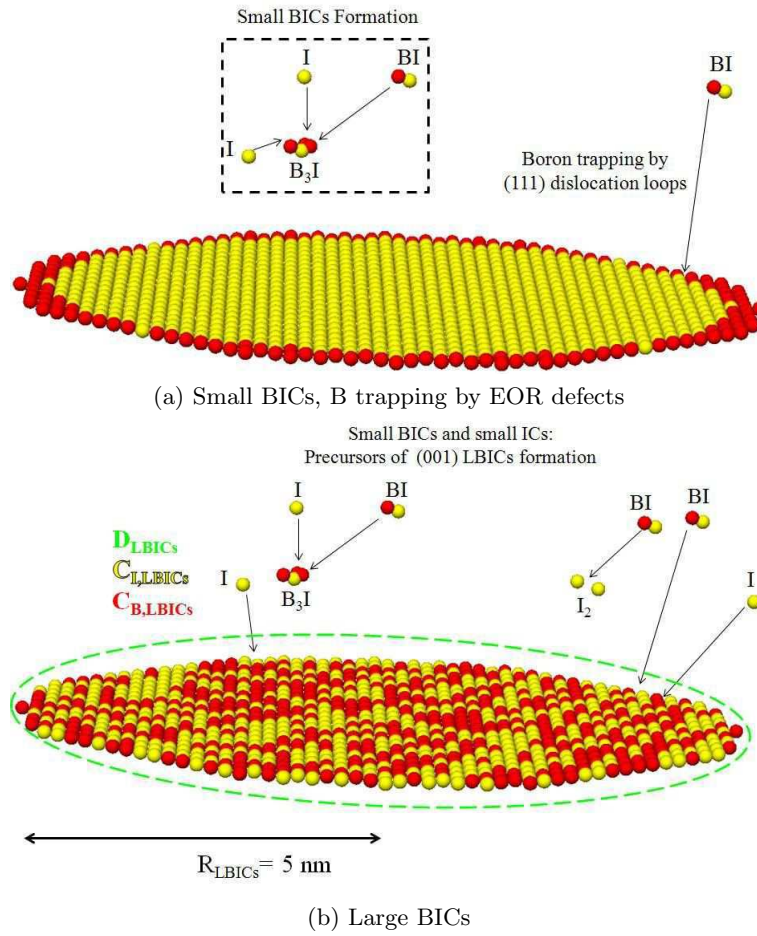


Figure 2.11: Diagram showing boron interaction with silicon interstitial atoms in (a) default advanced continuum TCAD models and (b) using the LBICs model based on moments approach [51]. The atomistic view shown here is explanatory and only continuum simulations were carried out in our work.

Equation 2.12 is the temporal evolution of the silicon interstitial atoms in the LBICs  $C_{I,LBICs}$ .  $D(BI)$  and  $D(I)$  are respectively the fixed diffusion coefficients of boron interstitial pairs  $B^-I^+$  and neutral interstitials  $I^0$ . However, it should be noticed that diffusing species charge state will be neglected in our model. LBICs form following reactions 2.9, 2.10 and 2.11 leading to an increase in the number of interstitials in the LBICs as given in the three first right hand side (rhs) terms of equation 2.12. In these terms,  $\frac{A}{R_{eff}} \Big|_{X,Y}$  is a free parameter and corresponds to the capturing efficiency of a mobile species  $X$  ( $I$  or  $BI$ ) by a given cluster ( $I_2$  for  $BI$  and  $B_3I$  for  $I$  and  $BI$ ) representing the ratio between the cross section of cluster  $Y$  on its effective radius as already used in literature for small ICs [56, 57]. The evolution of larger LBICs is governed by the balance between their capture and emission of free  $I$  and  $BI$  rhs terms 4 and 5 of equation 2.12. For  $I$  species, the capture is defined by the reaction constant  $k_{I,LBICs}$  a free parameter in our model, the LBICs mean radius  $R_{LBICs}$  and the respective difference between the free interstitial concentration and the equilibrium concentration in the vicinity of the LBIC defect  $C_{I,LBICs}^*$ . In the same manner for  $BI$  species, the capture is defined by the reaction constant  $k_{BI,LBICs}$  (also a free parameter in the model), the mean radius  $R_{LBICs}$ , and the respective difference between the free boron interstitial pairs  $BI$  concentration and equilibrium concentration in the vicinity of the LBIC defect  $C_{BI,LBICs}^*$ . The free parameter  $f_{prec}$  in front of  $C_{I,LBICs}^*$  of rhs term 4 of equation 2.12 is introduced in order to reproduce the formation of stable boride phases such as  $SiB_3$  and  $SiB_4$  at very high concentration by enhancing the emission of interstitials from the LBICs:

$$f_{prec} = \begin{cases} 1 & \text{if } C_{B,LBICs} < 7.10^{20} \text{ cm}^{-3} \\ C_{B,LBICs}/7.10^{20} & \text{if } C_{B,LBICs} \geq 7.10^{20} \text{ cm}^{-3} \end{cases} \quad (2.15)$$

As for equation 2.12 for  $C_{I,LBICs}$  field, a similar behaviour is verified by  $C_{B,LBICs}$  field in equation 2.13. Equation 2.14 gives the temporal evolution of the LBICs density whose first three rhs terms are similar to those of the respective equation 1 and 2 for  $C_{I,LBICs}$  and  $C_{B,LBICs}$ . The last two terms of equation 2.14 model the LBICs density reduction following their content increase with interstitials and boron thanks to the respective factors  $\frac{D_{LBICs}}{C_{I,LBICs}}$  for  $I$  and  $\frac{D_{LBICs}}{C_{B,LBICs}}$  for  $BI$  emission.

As described above, in order to determine the volume growth and density decrease of the LBICs, the mean radius  $R_{LBICs}$  evolution should be evaluated. The theoretical formula used for disk-shaped DLs mean radius extracted from [58] is:

$$\frac{dR_{LBICs}}{dt} = k_{BI,LBICs} \left( \frac{\pi}{n_{001}} \right) D(BI)(BI - C_{BI,LBICs}^*) + k_{I,LBICs} \left( \frac{\pi}{n_{001}} \right) D(I)(I - C_{I,LBICs}^*) \quad (2.16)$$

where  $n_{001}$  is the surface density of two (001) crystalline planes equal to  $1.36 \times 10^{15} \text{ cm}^{-2}$ . However convergence issues were encountered when implementing  $R_{LBICs}$  formula of equation 2.16 in the LBICs model. Therefore, a more simplified formula was used for the mean radius calculation:

$$C_{I,LBICs} + C_{B,LBICs} = n_a \pi R_{LBICs}^2 D_{LBICs} \Rightarrow R_{LBICs} = \sqrt{\frac{C_{I,LBICs} + C_{B,LBICs}}{n_a \pi D_{LBICs}}} \quad (2.17)$$

The term under the square root of equation 2.17 is inspired from an identical formula used in TEM statistical analysis of interstitials (111) DLs [59]. The respective equilibrium concentrations  $C_{I,LBICs}^*$  and  $C_{BI,LBICs}^*$  of  $I$  and  $BI$  in the vicinity of the LBICs of mean radius  $R_{LBICs}$  will be calculated using the minimization of the LBICs. The total energy of a (111) DL of silicon interstitials [60] is generalized to (001) DLs of radius  $R_{LBICs}$  containing both silicon and boron atoms:

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$${}^3D(I^0) = 1.746 \times e^{-\frac{3.57(\text{eV})}{k_B T}} \text{ and } D(B^-I^+) = 51 \times e^{-\frac{1.77(\text{eV})}{k_B T}} \text{ in SProcess database [3].}$$


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$$E(R_{\text{LBICs}}) = \pi R_{\text{LBICs}}^2 \gamma + \frac{\mu b^2 R_{\text{LBICs}}}{2(1-\nu)} \left( \ln \left( \frac{8R_{\text{LBICs}}}{b} \right) - 1 \right) - \frac{\pi R_{\text{LBICs}}^2 b}{\Omega_I} k_B T \ln \left( \gamma_I \frac{C_{\text{I, LBICs}}^*}{C_I^*} \right) - \frac{\pi R_{\text{LBICs}}^2 b}{\Omega_{\text{BI}}} k_B T \ln \left( \gamma_{\text{BI}} \frac{C_{\text{BI, LBICs}}^*}{C_{\text{BI}}^*} \right) \quad (2.18)$$

First rhs term of equation 2.18 is the DL interface energy where  $\gamma$  is the internal energy associated with the stacking fault which we fixed to the one already used for the (111) DLs of 70 mJ/m<sup>2</sup> [61]. Second rhs term is the strain energy of the circular dislocation loop where  $b \simeq \frac{1}{3}(001)$  is the Burgers vector [37],  $\mu$  is the shear modulus of  $63.28 \times 10^{10}$  dyne/cm<sup>2</sup> and  $\nu$  is the silicon Poisson ratio set to 0.28. Third and fourth rhs terms of equation 2.18 are the chemical potentials associated respectively with I and BI pairs with  $k_B$  the Boltzmann constant and  $T$  the temperature.  $\Omega_I$  and  $\Omega_{\text{BI}}$  are respectively the volume per silicon interstitial atom I and BI pair and it will be assumed:  $\Omega_I = \Omega_{\text{BI}} = \Omega$ , where  $\Omega$  is the volume per silicon atom of  $2 \times 10^{-23}$  cm<sup>3</sup>.  $\gamma_I$  and  $\gamma_{\text{BI}}$  are respectively the activity coefficients for non-ideal solutions [62] of I and BI and will be set to unity in our simulations.  $C_I^*$  and  $C_{\text{BI}}^*$  are respectively I and BI bulk silicon equilibrium concentrations. Available interstitials at thermal equilibrium are the limiting factor for BI pair equilibrium concentration and therefore BI equilibrium concentration cannot exceed the interstitials one in boron free silicon. Consequently, we will consider  $C_{\text{BI}}^* = C_I^*$ , where  $C_I^*$  is the intrinsic interstitial equilibrium concentration in silicon used in the process simulator [3].

$C_{\text{I, LBICs}}^*$  and  $C_{\text{BI, LBICs}}^*$  are calculated following the minimization of the total energy of equation 2.18 with correspondence to  $R_{\text{LBICs}}$ :

$$\frac{dE}{dR_{\text{LBICs}}} = 0 \quad (2.19)$$

which leads after simplifications to:

$$\left( \frac{C_{\text{I, LBICs}}^*}{C_I^*} \right) \cdot \left( \frac{C_{\text{BI, LBICs}}^*}{C_{\text{BI}}^*} \right) = \exp \left( \frac{\gamma \Omega}{b k_B T} \right) \exp \left( \frac{\sigma \Omega}{b k_B T R_{\text{LBICs}}} \right) \quad (2.20)$$

with  $\sigma = \frac{\mu b^2}{4\pi(1-\nu)} \ln \left( \frac{8R_{\text{LBICs}}}{b} \right)$ . From equation 2.20, it can be noticed that no unique equation can be extracted for both  $C_{\text{I, LBICs}}^*$  and  $C_{\text{BI, LBICs}}^*$ . Knowing that after an implantation step and at the beginning of an anneal, silicon super-saturation with interstitials is much higher than the super-saturation with BI pairs, we will therefore consider that in its vicinity, the LBIC defect behaves like a pure interstitials defect. From literature results for pure interstitial DLs [58] and using equation 2.20, the following relations are verified:

$$C_{\text{I, LBICs}}^* = C_I^* \exp \left( \frac{\gamma \Omega}{b k_B T} \right) \exp \left( \frac{\sigma \Omega}{b k_B T R_{\text{LBICs}}} \right) \quad (2.21)$$

$$C_{\text{BI, LBICs}}^* = C_{\text{BI}}^* \quad (2.22)$$

The set of equations 2.12, 2.13, 2.14, 2.21 and 2.22 summarize the LBICs model with the four following calibration parameters described previously:  $\frac{A}{R_{\text{eff}}} \Big|_{X,Y}$ ,  $k_{\text{I, LBICs}}$ ,  $k_{\text{BI, LBICs}}$  and  $f_{\text{prec}}$ .

Even though LBICs were observed in BF<sub>3</sub> PIII samples of sub-section 2.3.3, these samples cannot be used for the LBICs model calibration. First of all, BF<sub>3</sub> plasma implants are very shallow and therefore the LBICs thermal evolution is impacted by silicon/oxide surface interface. Moreover, in addition to boron and silicon interstitials high super-saturation after the implant, very high fluorine concentrations are also present ( $> 10^{20}$  cm<sup>-3</sup>) which may lead to inaccuracies in LBICs evolution due

to the fluorine effect. Consequently, simple boron implants with no additional fluorine, are needed in order to calibrate the LBICs model.

Three literature references using simple beam line implants were considered for LBICs model calibration. The results and their corresponding process conditions are summarized in table 2.4. The first reference is of Cristiano et al. [35, 54, 63], where LBICs were observed by TEM following a shallow boron implant at 0.5 keV  $1.10^{15} \text{ cm}^{-2}$ , annealed at 650°C for 2, 10, 40 and 160 s. The 650°C 10 s annealed sample, was also subsequently spike annealed in order to study possible dissolution mechanisms of the LBICs [63]. In this reference LBICs density and mean diameter were measured by TEM. In the second reference of Cojocaru-Mirédin et al. [45], a higher boron implantation energy at 10 keV  $5.10^{15} \text{ cm}^{-2}$  was used in order to localize the implant projected range  $R_p$  far from the silicon/oxide interface. Following the implant, several anneals were made including 600, 800 and 900 °C 1 h and 900 °C 5 h. In these experiments, boron and silicon content in the LBICs in addition to their mean size were investigated using APT measurements. The most recent reference of Blavette et al. [46] used even higher implantation energy and dose where boron implants at 27 keV  $1.10^{17} \text{ cm}^{-2}$  were used followed by thermal anneals at 500, 750 and 1000°C during one hour.

The LBICs model was first calibrated on the complete data set of [45] from table 2.4. The LBICs model free parameters were calibrated and corresponding values are given in table 2.5.  $\frac{A}{R_{\text{eff}}}\bigg|_{X,Y}$  was set to  $3.10^{-7} \text{ cm}$  which is in the range of literature values for interstitials capture efficiency by small ICs [57].  $k_{I,\text{LBICs}}$  and  $k_{BI,\text{LBICs}}$  are the respective dimensionless reaction constants of I and BI pairs with the LBICs and were calibrated using this set of experimental data.  $C_I^*$  (and  $C_{BI}^*$ ) bulk intrinsic equilibrium concentration in silicon was fixed to its default value already implemented in the process simulator [3].

Table 2.4: Summary of literature experimental results used for LBICs continuum model calibration.

Reference	Implantation	Anneal	Experiment
Cristiano et al., Hebras et al. [35, 54, 63]	0.5 keV, $1.10^{15} \text{ cm}^{-2}$	650°C - 2, 10, 40 and 160 s + Spike anneal 800 to 1050°C (step 50°C)	TEM
Cojocaru-Mirédin et al. [45]	10 keV, $5.10^{15} \text{ cm}^{-2}$	600, 800 and 900 °C 1 h and 900 °C 5 h	APT, SIMS
Blavette et al. [46]	27 keV, $1.10^{17} \text{ cm}^{-2}$	500, 750 and 1000 °C 1 h	APT, SIMS

Table 2.5: LBICs model parameters [51] calibrated using the experimental data of 2.4.

$\frac{A}{R_{\text{eff}}}\bigg _{X,Y} \text{ (cm)}$	$k_{I,\text{LBICs}}$ (no unit)	$k_{BI,\text{LBICs}}$ (no unit)	$f_{\text{prec}}$ (no unit)
$3.10^{-7}$	$6.44 \times 10^{-1} e^{\frac{0.14(\text{eV})}{k_B T}}$	1.0	Equation 2.15

In Cojocaru-Mirédin et al. experiments and thanks to APT technique, several LBICs were analysed and the number of boron and silicon atoms in each precipitate were extracted. In this manner, histograms of number of LBICs versus boron (or silicon) content in the LBICs can be built for the different thermal anneals. Corresponding results are given in Fig. 2.12 for the different thermal an-



neals with the following mean boron content from [45]: 9% for 600°C 1 h, 12% for 800°C 1 h, 21% for 900°C 1 h and 44% for 900°C 5 h. Every bin in the histogram corresponds to the number of LBICs with a given boron content. Are also shown in Fig. 2.12 the kernel density estimation (KDE) of the LBICs distribution which is more accurate for estimating the LBICs distribution than a histograms representation [64]. In every graph of Fig. 2.12, we added a small graph representing the number of B and Si atoms in the different LBICs analysed by the APT method. From the histograms and the number of atoms in the LBICs, we can see that both boron content and number of atoms (and therefore size) of the LBICs increase when increasing the thermal budget. For the highest thermal budget in Fig. 2.12d, some LBICs are in the SiB<sub>3</sub> and SiB<sub>4</sub> stable phases [47].

Boron content in the precipitation region is defined by:

$$\text{Frac(B)} = \frac{\int C_{\text{B,LBICs}}}{\int C_{\text{B,LBICs}} + C_{\text{I,LBICs}}} \quad (2.23)$$

and was first investigated in our simulations. Corresponding results compared to APT data are given in Fig. 2.13a. Our model reproduces correctly APT data and as expected, when increasing the thermal anneal of Fig. 2.13a, the LBICs are enriched with boron due to the formation of a stable boride phase SiB<sub>3</sub>.

With the set of calibrated parameters of the LBICs model obtained from Cojocaru-Mirédin et al. experimental data, our models predictability was evaluated on high boron dose implanted samples from Blavette et al. work [46]. In these experiments, an extremely high boron implantation dose at 27 keV  $1.10^{17} \text{ cm}^{-2}$  (table 2.5) was used. APT measurements were also carried out on these data and the following mean boron content was obtained: 30%, 37% and 75% for respectively 500, 750 and 1000°C 1 h of anneal. In the 1000°C 1 h case, the formation of SiB<sub>3</sub> and SiB<sub>4</sub> boride phases is clearly confirmed. The APT data were perfectly reproduced by our LBICs model and simulation results are given in Fig. 2.13b.

Our model was also evaluated on older literature results from Cristiano et al. [35, 63] and Hebras et al. [54] (Fig. 2.14) obtained from samples fabricated using typical p<sup>+</sup>/n USJs conditions. The first point in Fig. 2.14 (sample without spike post anneal) corresponds to the LBICs density calculated using the LBICs model after the initial 650°C 10 s thermal anneal. The simulated density of  $8.3 \times 10^{12} \text{ cm}^{-2}$  is in agreement with the experimentally observed one ( $\sim 10^{13} \text{ cm}^{-2}$  [35, 37, 54]). When adding a subsequent thermal anneal from 800 to 1050°C with a 50°C step, TEM analysis [63] indicated that the LBICs density progressively decreases, until their complete dissolution at temperatures of 1000°C and higher. This result is different from the others discussed above, where LBICs are found to become more stable at higher thermal budget and is due to the surface proximity to the silicon self-interstitial distribution in the USJ case (centered at  $\sim 3 \text{ nm}$  for a 0.5 keV B<sup>+</sup> implant). The simulation results shown in Fig. 2.14 clearly show that the decrease in LBICs density and the final dissolution above 1000°C (calculated density below the TEM detection limit) are perfectly captured by the LBICs model and confirm its predictability for highly boron doped USJs.

In addition to the APT data of the 10 keV  $5 \times 10^{15} \text{ cm}^{-2}$  boron implants, SIMS results were also investigated. As expected and due to a low boron diffusion, boron SIMS results at 600°C and 800°C during one hour were easily reproduced and are shown in Fig. 2.15a. For the 900°C for 1 and 5 h samples, an interesting effect is observed where a boron profile narrowing is clearly evidenced in the LBICs precipitation region ( $> 10^{20} \text{ cm}^{-3}$ ). In addition to profile narrowing, the boron peak value is slightly increased with respect to the as-implanted profile following the two 900°C anneals. This apparent uphill diffusion effect, not reproduced by our simulations, might be due to a real negative diffusion due to the spinodal decomposition during precipitation of the binary system composed of

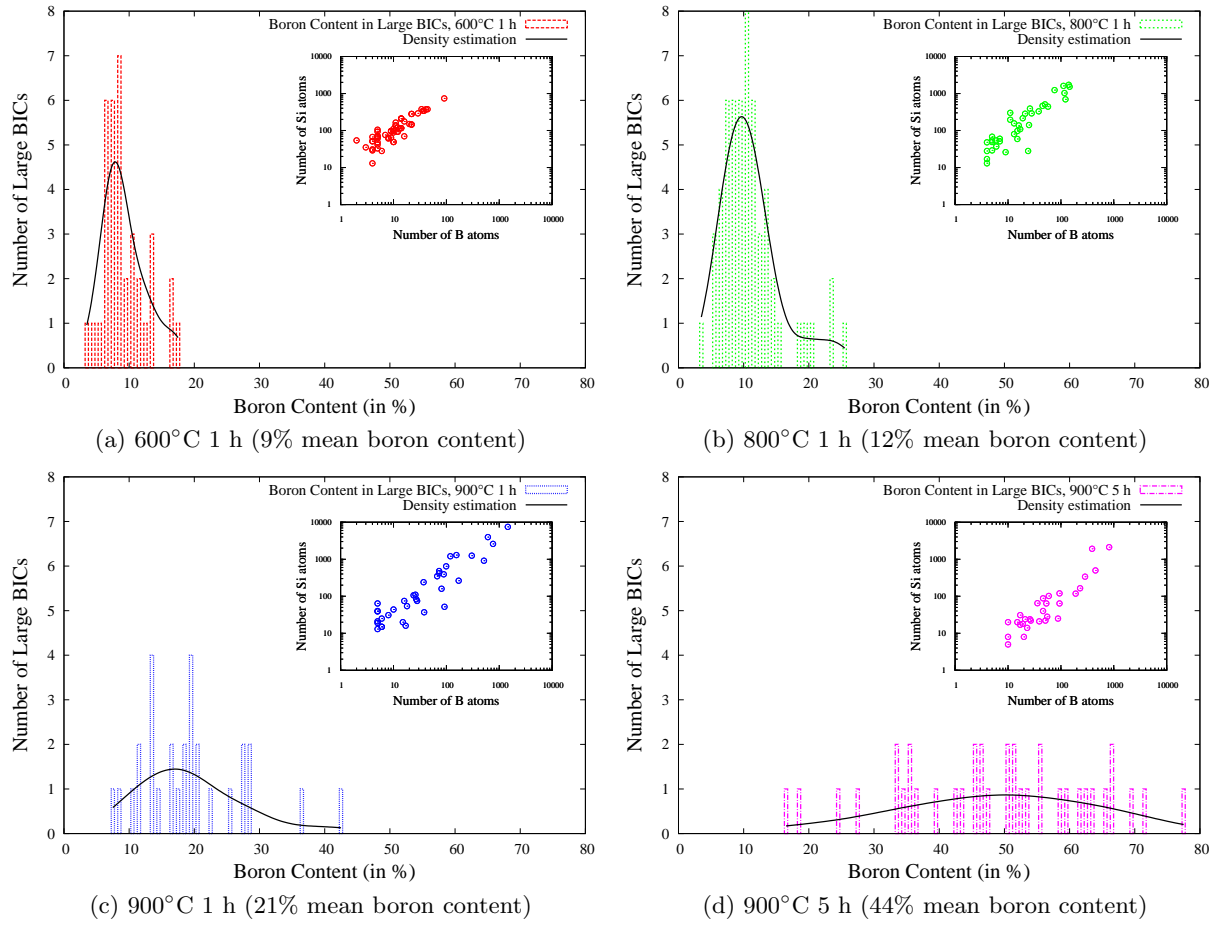


Figure 2.12: Histogram distribution of boron content in the LBICs from [45] following a boron implant at 10 keV  $5.10^{15} \text{ cm}^{-2}$  implant annealed at (a) 600°C 1 h, (b) 800°C 1 h, (c) 900°C 1 h and (d) 900°C 5 h.

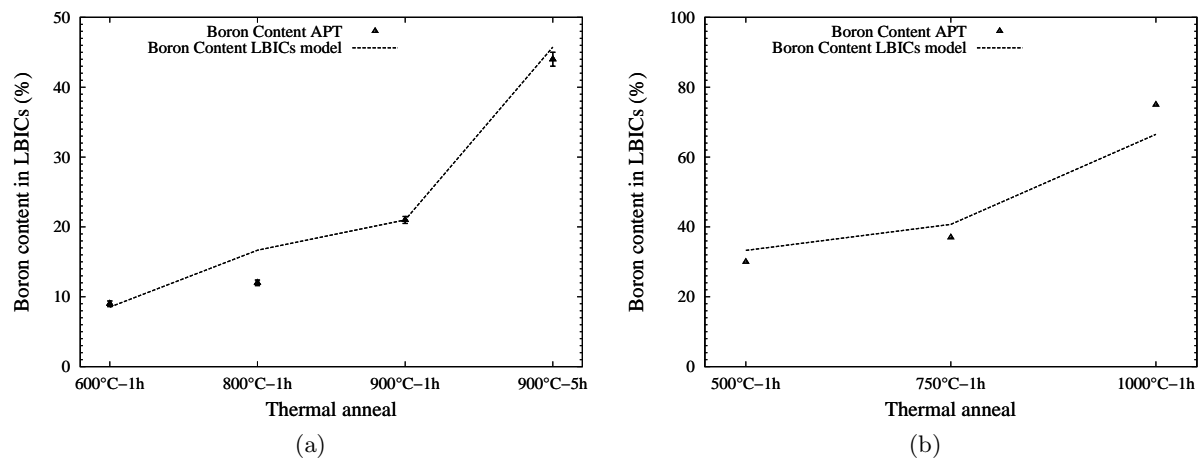


Figure 2.13: Boron content in the LBICs from APT measurements and LBICs model simulations following a boron implant at (a) 10 keV  $5.10^{15} \text{ cm}^{-2}$ , annealed at 600, 800 and 900°C 1 h and 900°C 5 h from Cojocaru-Mirédin et al. work [45] and (b) 27 keV  $1.10^{17} \text{ cm}^{-2}$  annealed at 500, 750 and 1000°C 1 h from Blavette et al. work [46].



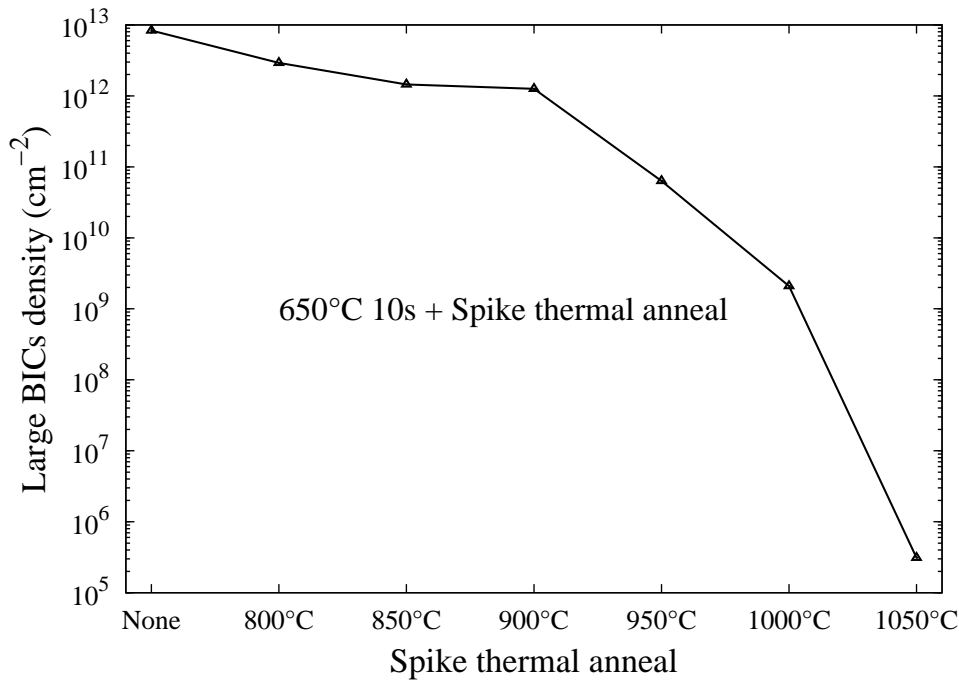


Figure 2.14: LBICs density evolution using the LBICs model for a shallow boron implant at 0.5 keV  $5.10^{15}\text{cm}^{-2}$  from Cristiano et al. work [35, 63] annealed at 650°C 10 s (None) and followed by subsequent spike anneals at 800, 850, 900, 950, 1000 and 1050°C.

the dilute boron in bulk silicon phase and boron in the precipitated LBICs phase [46]. Such mechanism would result in an overall boron negative diffusion coefficient. Alternatively, the boron profile narrowing might be due to a nucleation-growth mechanism and the corresponding increase in boron fraction in the precipitation region.

Given all these uncertainties on the origin of apparent uphill diffusion, our boron diffused profiles simulations at 900°C 1 and 5 h in Fig. 2.15b could not reproduce boron narrowing effect as well as the kink concentration separating the immobile region from the diffusing tail, although the slope of the latter is correctly reproduced. Moreover, using a negative diffusion coefficient quickly leads to convergence issues when using classical numerical resolution methods such as finite difference time domain (FDTD) or finite elements method (FEM) used in our simulations.

Negative diffusion effects have already been observed and extensively studied in binary systems in geology examples [65]. The particular case of boron negative diffusion evidenced in Fig. 2.15b by profile narrowing has already been seen in older literature results [66, 67], even though the authors did not comment the profile narrowing aspect. For instance boron profile narrowing is quite noticeable in Hofker et al. [66] work following boron implants at 70 keV  $1.10^{17}\text{cm}^{-2}$  annealed at 1000°C during 1×, 2× and 3×35 minutes. In the work of Cowern et al. [67], a profile narrowing was also observed following an implant of 25 keV  $5.10^{15}\text{cm}^{-2}$  annealed at 900°C during 10 h. The previous literature results show that boron profile narrowing in the precipitation region is enhanced when increasing boron implantation dose. Indeed, when using even higher implantation dose such as in the work of Blavette et al. [46] of table 2.4, the profile narrowing due to the LBICs precipitation is even more pronounced. In Fig. 2.16, we present SIMS profiles of the boron 27 keV  $1.10^{17}\text{cm}^{-2}$  as implanted and annealed at 500, 750 and 1000°C during one hour. In these results, boron profile narrowing in the precipitation region is very pronounced at 1000°C and is already visible for the lower temperature anneals at 500 and 750°C.

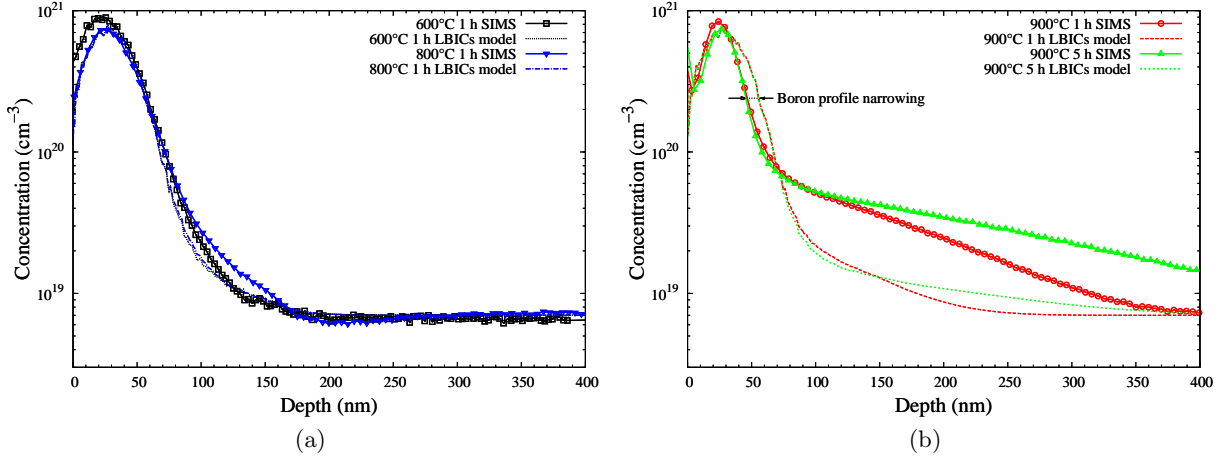


Figure 2.15: Boron 10 keV  $5.10^{15}\text{cm}^{-2}$  annealed at (a) 600°C and 800°C during 1 hour and (b) 900°C during 1 and 5 hours from SIMS results [45] and using our LBICs model. Boron profile narrowing is observed experimentally in the precipitation region for the two 900°C anneals.

In any case, this apparent boron diffusion against concentration gradient should not be confused with boron uphill diffusion effect near silicon/oxide interface in case of pre-amorphization, already observed in literature [68], due to existing interstitials flux from EOR defects band to the silicon/oxide interface during thermal anneals. Indeed, these point-defect diffusion related mechanisms are already included in our model but are not able to reproduce the observed results.

To conclude, a LBICs continuum model based on moments approach was developed in order to reproduce boron precipitation mechanisms in high boron dose implanted samples. Model parameters calibration presented in [51] was carried out thanks to recent literature results including boron content in the LBICs extracted from APT data. Using this set of calibrated parameters, predictive modelling of different literature experimental results could be obtained, including the evolution during thermal annealing of boron content in the LBICs from APT data and LBICs density evaluated by TEM. Possible dissolution or stabilization of LBICs depending on boron implantation conditions in terms of dose and energy are also captured by the model. Finally, an apparent uphill diffusion against the concentration gradient in very high dose boron implanted samples and annealed at high temperatures, was evidenced experimentally from boron peak narrowing in SIMS profiles.

The LBICs model shown here will be applied in next sub-section 2.4.3 on  $\text{BF}_3$  PIII samples of sub-section 2.3.3.

### 2.4.3 Large BICs model applied to $\text{BF}_3$ PIII

In previous sub-section 2.4.2, the LBICs model was applied to beam-line simple boron implantation with very high doses in order to better understand the evolution of LBICs during thermal anneals. Using the set of the LBICs model calibrated parameters shown in table 2.5 of sub-section 2.4.2, TCAD boron annealed profiles at 800°C 10 min, 900°C 10 min and 1065°C 1 s were compared to  $\text{BF}_3$  PIII SIMS data of Fig. 2.6. Corresponding results described in [69] are shown in Fig. 2.17a. A good agreement between SIMS and TCAD boron diffused profiles is observed, mainly for high thermal budgets, including boron peak below the A/C interface and its slow dissolution when increasing the thermal anneal. Fig. 2.17b shows boron detailed profile following thermal anneals at 900°C 10 min and 1065°C 1 s including active boron and boron in the LBICs extracted from the  $C_{\text{B,LBICs}}$  field within the

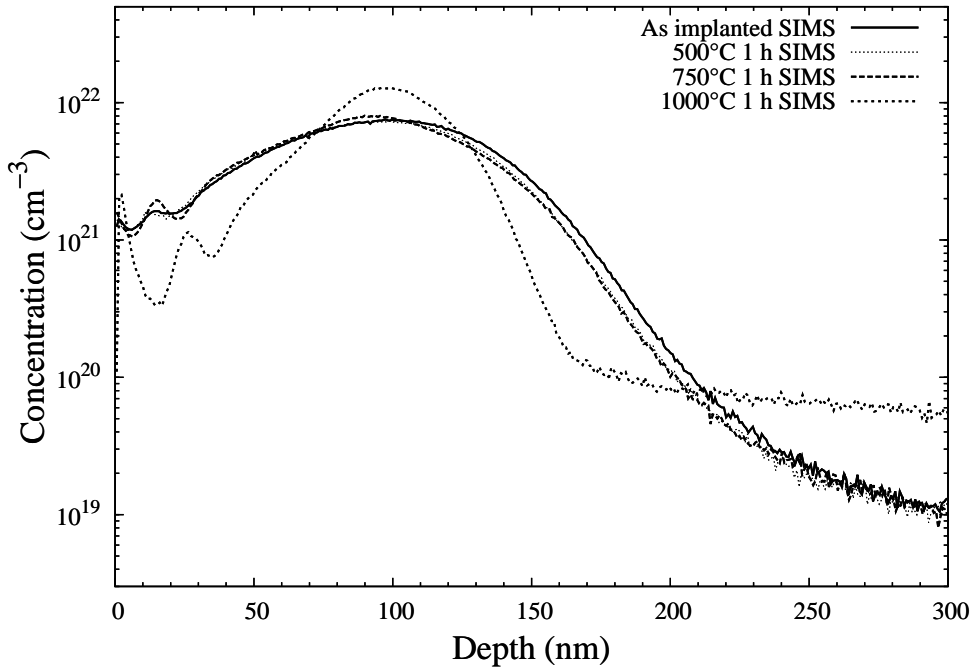


Figure 2.16: Boron 27 keV  $1.10^{17}\text{cm}^{-2}$  as implanted and annealed at 500, 750 and 1000°C during one hour SIMS profiles [46]. Boron profile narrowing in the precipitation region is observed for the different thermal anneals and is very pronounced for the 1000°C anneal.

LBICs model. As expected from recent results of Cojocaru-Mirédin et al. [45], LBICs slowly dissolve at high thermal budgets leading to a deeper diffusion tail for the 1065°C 1 s anneal.

In addition to SIMS results, junctions sheet resistance already presented in Fig. 2.10 using default process models, were simulated using the LBICs model. Corresponding sheet resistance values are given in Fig. 2.18 and show that contrarily to previous results shown in Fig. 2.10, the LBICs model is able to reproduce boron activation for the different  $\text{BF}_3$  plasma implanted and annealed samples, with an electrical activation improvement when increasing the thermal budget.

## 2.5 Conclusion

In this chapter on implantation related defects and their relative challenges, we gave a small introduction on plasma immersion ion implantation (PIII), a promising technique for advanced CMOS technologies. Its different characteristics in comparison to traditional beam-line implantation in CMOS technologies were also presented. Dedicated experiments using  $\text{BF}_3$  PIII with different implantation energies and doses were studied and modelled using a Monte Carlo implantation code and a double exponential (2-exp) energy distribution. A good agreement was obtained between SIMS and TCAD simulation results.

In order to investigate implantation defects evolution during thermal anneals, the  $\text{BF}_3$  PIII at 10 kV  $5.10^{15}\text{cm}^{-2}$  was intentionally chosen and annealed at different times and temperatures in order to localize the defects far from the oxide/silicon interface and reduce its impact. SIMS and TEM measurements on the annealed samples confirmed the presence of (001) dislocation loops behind the A/C interface of the implant corresponding to large BICs already observed in literature. As expected, state-of-the-art default TCAD process models were not able to reproduce boron diffused tail and peak behind the A/C interface due to the absence of a LBICs model.

A new continuum CPU efficient TCAD model based on moments approach was developed. The

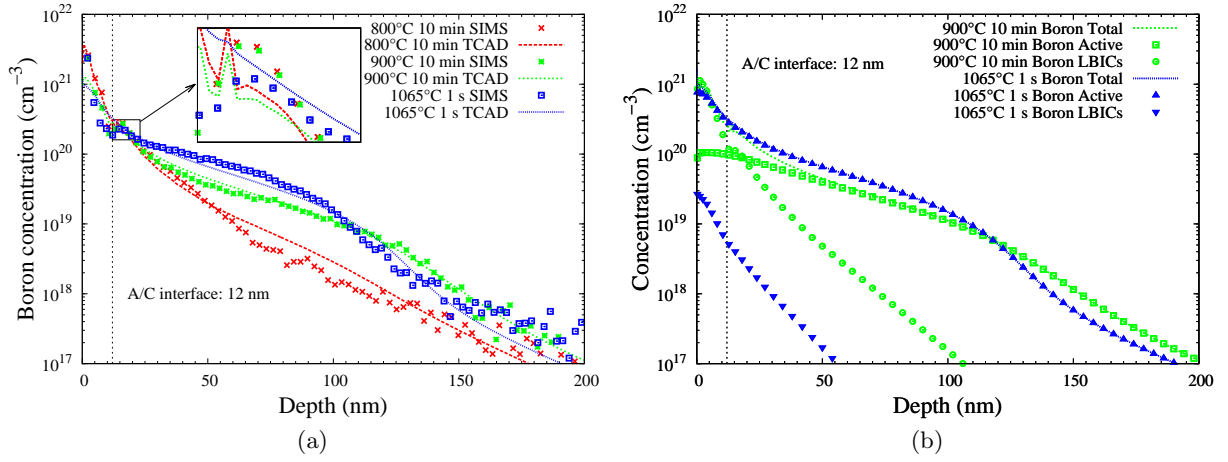


Figure 2.17: (a) Boron SIMS versus TCAD profiles using the LBICs model following a  $\text{BF}_3$  plasma implant at 10 kV  $5 \cdot 10^{15} \text{cm}^{-2}$  annealed at 800°C 10 min, 900°C 10 min and 1065°C 1 and (b) boron detailed TCAD profiles at 900°C 10 min and 1065°C 1 s, including concentrations of total boron, active boron and boron in the LBICs.

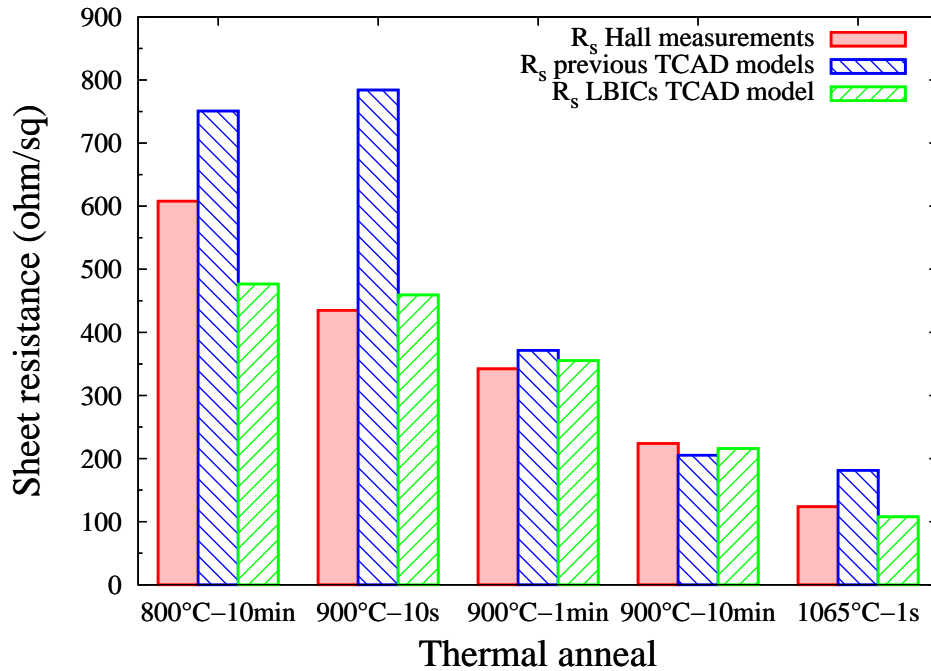


Figure 2.18: p+/n PIII  $\text{BF}_3$  junctions sheet resistance extracted from Hall effect measurements for different thermal anneals of table 2.1 and compared to TCAD simulations using previous TCAD models [17] in comparison to the LBICs model [69].

three moments within the model include LBICs density, concentration of boron in the LBICs and concentration of silicon interstitials in the LBICs. The model was tested on several literature data with traditional boron beam-line implants at very high doses where LBICs were observed by TEM and APT. The model parameters were successfully calibrated thanks to one particular data set. Following the calibration step, the model predictively reproduced other literature data with different experimental conditions. For the very high dose implanted samples, an interesting boron apparent uphill diffusion against the concentration gradient in the precipitation region was observed and still needs further theoretical and experimental investigation. However, for shallower implantation energies such as the one used in BF<sub>3</sub> PIII presented in this chapter, the model resulted in good agreement between SIMS and TCAD simulations. Contrarily to previous state-of-the-art TCAD process models, the LBICs model was able to reproduce both boron diffused tail and peak behind the A/C interface in BF<sub>3</sub> PIII. In addition, electrical activation in BF<sub>3</sub> PIII was correctly modelled thanks to the LBICs model, where boron activation improvement when increasing the thermal budget was correctly captured.

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## Chapter 3

# Chemical species diffusion in multi-materials stacks

### 3.1 Introduction

In previous chapter, implantation induced defects in silicon were studied. However, the use of USJs required by miniaturization shortens the distance between the USJs in silicon and overlying materials such as those used in advanced gate stacks of MOS transistors described in chapter 1. Consequently, taking into account the interactions between the different materials of CMOS devices in TCAD models becomes mandatory. The chemical species diffusion in such stacks including diffusion in the different materials and transfer from a material to neighbouring ones can no more be ignored because of their impact on advanced devices electrical performances. In the frame of ATEMOS project [1], two main chemical species diffusion mechanisms in multi-materials stacks were considered during the PhD:

- Boron out-diffusion in nitride/oxide/silicon stacks like pMOS spacer stacks leading to a boron dose loss in silicon modifying electrical characteristics, shown in Fig. 3.1 in the green framed region of the pMOS transistor.
- Lanthanum diffusion in advanced high-k stacks leading to negative threshold voltage  $V_t$  shifts in advanced nMOS transistors, white framed in Fig. 3.1 on the right.

The two diffusion mechanisms lead to two corresponding diffusion models for boron dose loss in nitride/oxide/silicon stacks and lanthanum diffusion in high-k stacks described respectively in sections 3.2 and 3.3.

### 3.2 Boron dose loss modelling in nitride/oxide/silicon stacks

In this section, boron dose loss in nitride/oxide/silicon stacks will be investigated. A small introduction to boron out-diffusion mechanisms and impact on electrical characteristics will be given in 3.2.1. Dedicated experiments using a  $\text{BF}_2$  1 keV  $5 \cdot 10^{14} \text{cm}^{-2}$  shallow implant, annealed at  $1000^\circ\text{C}$  during 2 min with different nitride/oxide combinations followed by SIMS measurements were designed in order to evaluate the stack's dependent dose loss. The experiments will be described in 3.2.2. Using this experimental investigation, a boron dose loss TCAD model, based on B. Pelletier PhD's previous work [2] was developed and will be presented in 3.2.3.

#### 3.2.1 Introduction to boron dose loss

CMOS transistors miniaturization must ensure the control of the electrical properties of USJs together with the short channel effects (SCE) induced by the USJs. For instance, an important region for SCE

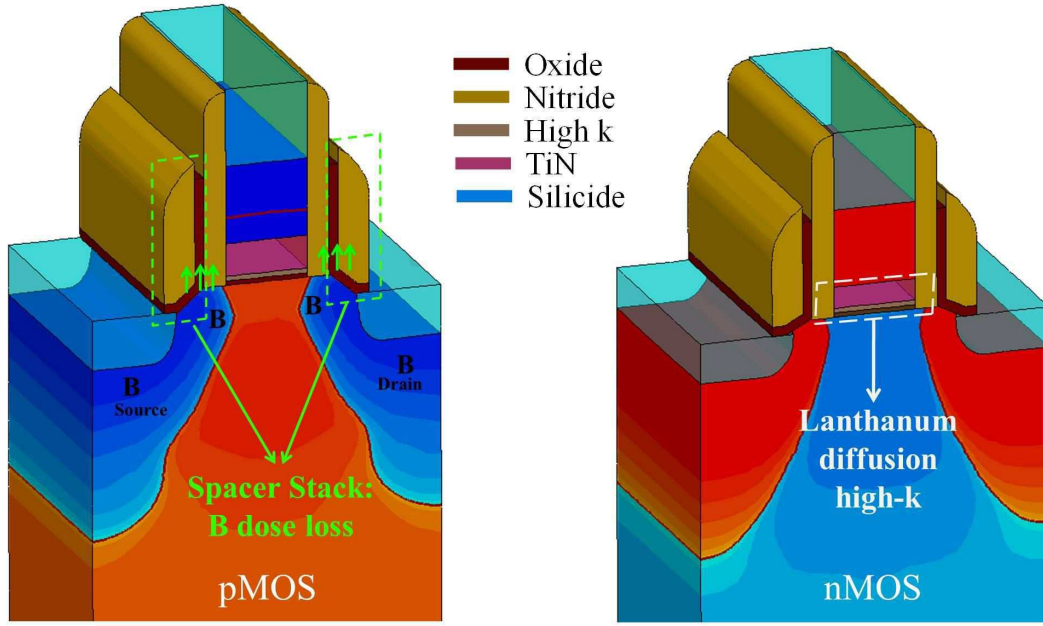


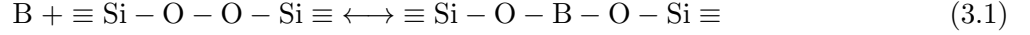
Figure 3.1: Diagram of the different materials (silicon, oxide, nitride, high-k, TiN metal gate and silicide) and interfaces between materials of a pMOS transistor (left) where we show the LDD and source/drain boron (B) doped regions (green square) in silicon relatively to the position of the spacer stack and corresponding boron dose loss from silicon to be presented in section 3.2 and a nMOS transistor (right) gate stack region (white square) with the interfacial oxide, the high-k and the TiN metal gate where lanthanum diffusion will take place as it will be presented in section 3.3.

control on CMOS devices is the LDD region where the use of new materials allows to keep the required electrical performances. However, this leads to different interactions between the materials such as segregation of chemical species at the interfaces and/or transfer of species from a material to neighbouring ones. This is the case of boron in nitride/oxide/silicon stacks such as spacer stacks and corresponding boron dose loss from silicon. According to the ITRS [3], predictive segregation and dose loss models are among modelling challenges for technology nodes above 14 nm. In microelectronics industry, nitride/oxide/silicon stacks are mainly found in spacer stacks of MOS transistors with nitride and oxide, used in order to separate LDD and source/drain from the channel and control effective electrical gate length  $L_{\text{eff}}$ . However, nitride/oxide/silicon stacks can also be found in other CMOS based devices such as CMOS image sensors with a back side illumination (BSI) scheme, as we will see in chapter 4.

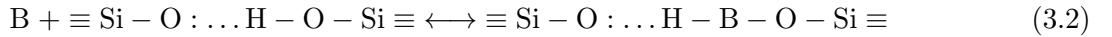
In the particular case of pMOS transistors, several literature results [4–7] demonstrated that the oxide and nitride layers used in spacer stacks modulate boron diffusion from silicon to oxide during the thermal anneals subsequent to the spacer process step. This out-diffusion effect can lead to an important boron dose loss from silicon to oxide affecting electrical characteristics of CMOS devices such as the LDD extension sheet resistance  $R_{\text{ext}}$  and the threshold voltage  $V_t$  of pMOS transistors. On the left of Fig. 3.1, we show a diagram of the different materials and interfaces between materials, present in advanced pMOS transistors and more particularly in the spacer stack region where boron out-diffusion will take place. In the out-diffusion mechanism, boron dose loss is controlled by the transfer of boron from silicon to oxide and by the diffusivity of boron in oxide. Therefore, for an identical oxide/silicon interface, the higher the diffusion in oxide, the more important is the dose loss.

Boron out-diffusion literature investigations were first carried out on thermally grown oxides. It was shown by Fair et al. [8] that boron diffusion in oxide is monitored by the SiO bonds called

Peroxy-Linkage-Defects (PLDs) following the reaction:



with an activation energy  $E_{a,\text{PLD}}$  for the diffusion mechanism by PLDs of 3.56 eV [8]. However, this activation energy led to low values of boron effective diffusivity that cannot explain the boron diffused profiles in gate oxides and therefore the role played by hydrogen in the oxide was suspected. Indeed, several results [8–10] showed that thermal anneals in a  $\text{H}_2$  ambient enhance boron diffusion in the oxide leading to a higher boron dose loss in silicon. With the presence of hydrogen in oxide, in addition to Si-O bonds, energetically favoured O-H bonds will also form and are called hydrogen related defects (HRDs) [8]. As for reaction 3.1, boron diffusion by HRDs used the following reaction:



with an activation energy  $E_{a,\text{HRD}}$  for the diffusion mechanism by the HRDs of 3.12 eV [8] lower than  $E_{a,\text{PLD}}$  and explaining the enhancement of boron diffusion in oxide in the presence of hydrogen.

Since the advent of the 65 nm technology node, spacer oxide and nitride layers are deposited at low temperatures using chemical vapor deposition (CVD) and are hydrogen rich [11–13]. Hydrogen and more specifically HRDs content in the oxide will depend on the specific oxide CVD process. In order to account for the dependence of boron diffusivity in oxide on OH bonds (or HRDs) concentration, Chakravarthi et al. [14] used a modified boron diffusivity:

$$D(\text{B})_{\text{SiO}_2} = D_0(\text{B}) \left( 1 + \frac{\text{OH}}{\text{OH}_{\text{ref}}} \right)^n \quad (3.3)$$

$D_0(\text{B})$  is the boron diffusivity in a OH bonds free oxide. OH and  $\text{OH}_{\text{ref}}$  are respectively the OH (HRDs) concentrations in the given oxide and in a reference oxide,  $n$  is a fitting parameter. It should be noticed that the diffusivity of equation 3.3 depends on the total hydrogen concentration, while in Fair et al. work [8], boron diffusion is favoured by OH bonds, and therefore the formulation of equation 3.3 is chosen here. In equation 3.3, boron diffusion in oxide depends on the initial OH concentration. However, the evolution of OH concentration during a thermal anneal is not considered. In the meantime, even though no boron diffusion was observed in nitride in literature [4–6], nitride layer can indirectly influence the out-diffusion mechanism by injecting hydrogen in the oxide during thermal anneals subsequent to the nitride deposit, modifying OH concentration in the oxide. Nitride can also act as a capping layer responsible for hydrogen retention in the oxide limiting thermal degassing during thermal anneals and consequently increasing boron out-diffusion [6].

In order to study rigorously boron out-diffusion in nitride/oxide/silicon spacer stacks during thermal annealing, hydrogen related species physical characteristics and evolution in both nitride and oxide should be monitored, in addition to the oxide boron diffusion dependence on the hydrogen related species concentrations. The correlation between hydrogen related species and boron dose loss will be carried out using full sheet boron implanted and annealed samples with different nitride/oxide/silicon stacks. These samples have been analysed by SIMS and are described in 3.2.2. Following the experimental part description, modelling boron dose loss will be shown in 3.2.3 including hydrogen reaction and diffusion dynamics in oxide and nitride, and corresponding boron out-diffusion modelling using SIMS data.

### 3.2.2 Dedicated boron dose loss experiments

The samples were prepared on (001)-oriented p-type silicon wafers according to the experimental plan presented in table 3.1 ( $\text{S}'_1$  to  $\text{S}'_4$ ). We first performed a 1 keV  $5.10^{14} \text{ cm}^{-3}$   $\text{BF}_2$  implantation step similar to the low doped drain (LDD) condition used in electrical lots. Four different material stacks

have been studied by combining two different oxides (OA and OB) and three different nitrides (NA, NB and NC) which present different hydrogen characteristics. OA oxide was deposited at 625°C by low pressure chemical vapour deposition (LPCVD) using a liquid tetraethyl orthosilicate (TEOS) liquid precursor. OB oxide is an un-doped silicon glass (USG) film deposited at 400°C by plasma enhanced chemical vapour deposition (PECVD) using the reaction between  $\text{SiH}_4$  and  $\text{N}_2\text{O}$  compounds. NA and NC nitride layer were deposited by PECVD using a  $\text{SiH}_4/\text{NH}_3/\text{N}_2$  chemistry at 480°C and 400°C, respectively. NB nitride was deposited at 590°C by LPCVD using a hexachlorodisilane (HCD), ammonia ( $\text{NH}_3$ ) and ethylene ( $\text{C}_2\text{H}_4$ ) as precursors. The samples were then subjected to an anneal process at 1000°C during 2 min by using a rapid thermal annealing (RTA) tool in a  $\text{N}_2$  ambience at the atmospheric pressure, under a controlled oxygen atmosphere (radiance chamber from Applied Materials). The four nitride/oxide combinations of stack considered in this study have been characterized by Secondary Ion Mass Spectrometry (SIMS) using a 1 keV 45° tilted  $\text{O}_2$  beam. A specific calibration was carried out in order to quantify the boron concentration as function of the depth in oxide and silicon.

Table 3.1: Summary of the samples used in this study.  $S'_1$  to  $S'_4$  are the nitride/oxide/silicon samples for boron SIMS measurements with the 1 keV  $5.10^{14} \text{ cm}^{-2}$   $\text{BF}_2$  LDD implant, annealed at 1000°C during 2 min. A reference  $S'_5$  similar to  $S'_4$  but not annealed has also been preferred for the sake of comparison.

Sample	$S'_1$	$S'_2$	$S'_3$	$S'_4$	$S'_5$
$\text{BF}_2$ implant	x	x	x	x	x
OA LPCVD	x	x			x
OB PECVD			x	x	
NA PECVD	x				
NB LPCVD		x	x		x
NC PECVD				x	
Anneal (1000°C, 2 min)	x	x	x	x	

The boron SIMS profiles for samples  $S'_1$  to  $S'_5$  are given in Fig. 3.2. First of all, in presence of a nitride cap during the anneal we observe a substantial boron diffusion in silicon after anneal as compared to  $S'_5$ . In addition, boron has diffused in the oxide whereas no dopant has been detected in the nitride cap. Qualitatively, the higher the boron dose is in oxide, the lower it is in silicon in agreement with the boron out-diffusion mechanism. Two different types of behavior are observed: sample  $S'_1$  and  $S'_2$ , with the same oxide layer OA (LPCVD TEOS) show a higher boron dose loss in the oxide and a shallower diffusion in silicon. Conversely samples  $S'_3$  and  $S'_4$  made with oxide OB (PECVD USG) result in a higher dose and diffusion depth in silicon and lower boron out diffusion in the oxide.

Some remarks can then be drawn concerning the impact of the nitride. For the same OA oxide, NA/OA spacer exhibits slightly higher out-diffusion than NB/OA spacer, which suggests in first order a higher  $\text{SiNH}_0$  initial concentration of NA in comparison to NB nitride. These results are in agreement with the out diffusion literature which have demonstrated the impact of the nitride cap on the loss of boron in the oxide during anneal [4-6]. They will be discussed in the next section.

Another interesting effect that can be seen in Fig. 3.2 concerns boron diffused profiles in oxide having a shape with an exponential tail (straight line in log scale). While the resolution of Ficks 2<sup>nd</sup> law diffusion equation [15] with a boron emission from the oxide/silicon interface to the oxide leads to



classical complementary error functions (erfc) shaped profiles, in our case exponential shaped boron diffused profiles are observed. The exponential diffusion behaviour suggests that boron diffusion in the oxides used in our experiments could be mediated by intermediate mobile species and will be discussed later in the paper. We can also see that boron diffusivity in oxide correlates with the exponential tails steepness corresponding to different hopping lengths.

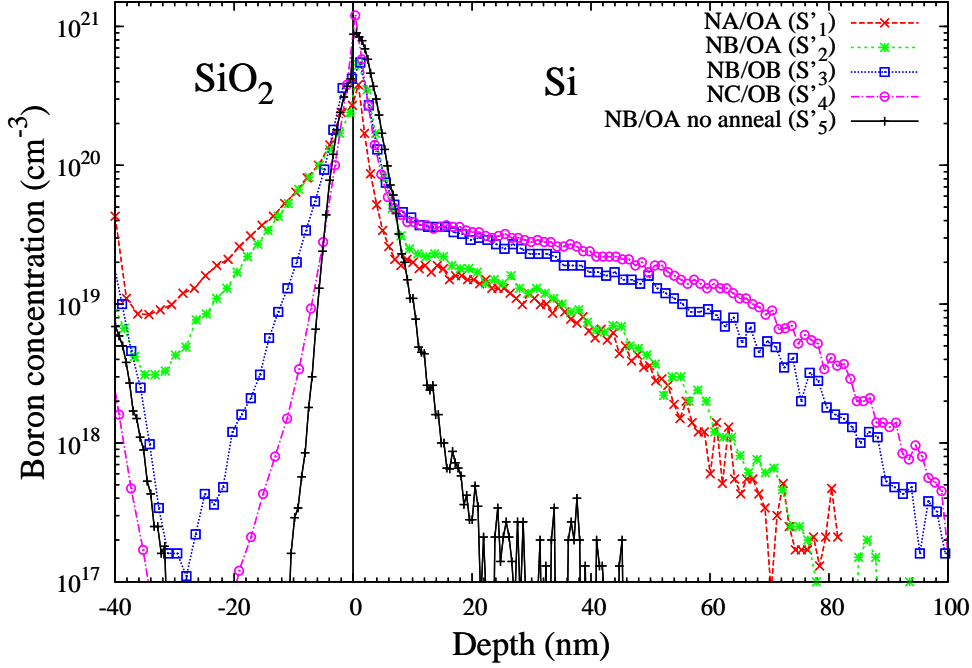


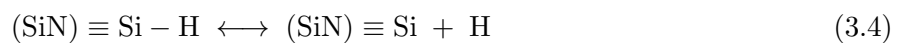
Figure 3.2: Boron SIMS results for samples  $S'_1$  to  $S'_4$  (table 3.1) with different nitride/oxide/silicon spacer stacks annealed at  $1000^\circ\text{C}$  2 min, in addition to NB/OA  $S'_5$  reference sample before annealing.

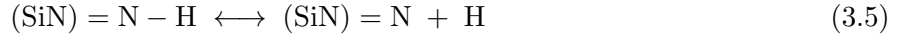
### 3.2.3 Boron dose loss modelling

SIMS results have emphasized in Fig. 3.2 the boron dose loss from silicon into the oxide as function of the spacer stack. Given the relation between boron diffusion in oxide and hydrogen related species content in both oxide and nitride, hydrogen related species dynamics in the spacer stack is first discussed in sub-section 3.2.3.1. Then we present models of boron diffusion modelling in sub-section 3.2.3.2 by using two different diffusion mechanisms through fixed and mobile chemical traps respectively.

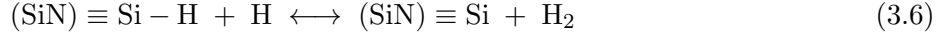
#### 3.2.3.1 Dynamics of hydrogen related species

Boron dose loss observed for the different spacer stacks of Fig. 3.2 can be understood following the investigation of hydrogen related species dynamics in both oxide and nitride. The three nitrides NA to NC used in the samples  $S'_1$  to  $S'_4$  of table 3.1 were analysed using coupled mechanical stress/thermal desorption spectroscopy (TDS) measurements described by Morin et al. in [16] and corresponding hydrogen related species chemical characteristics were extracted. In the nitrides deposition conditions used in our work, hydrogen can be incorporated in nitride by forming SiH or NH bonds [12] in the SiN lattice. The hydrogen species concentration in the nitride is strongly dependent on the process conditions and therefore some differences are expected for the nitrides under consideration. During a thermal anneal, hydrogen bonds can be broken thus releasing free diffusing hydrogen H atoms [17]:





The released hydrogen from reactions 3.4 and 3.5 can also react with other present SiH and NH bonds releasing a free diffusing dihydrogen  $\text{H}_2$  molecule:



The released hydrogen species (H in reactions 3.4 and 3.5,  $\text{H}_2$  in reactions 3.6 and 3.7) can freely diffuse in nitride, but also be transferred to adjacent materials such as oxide or air in the annealing chamber for samples  $\text{S}'_1$  to  $\text{S}'_4$ . As a consequence, reaction mechanisms 3.4 to 3.7 and the diffusion of released H and  $\text{H}_2$  species should be characterized in order to evaluate the hydrogen species evolution in the nitride during a thermal anneal. Chemical kinetics of the different hydrogen reactions are then analysed by TDS using a thermal anneal for each nitride under consideration. However, the TDS technique cannot distinguish between the atomic and molecular desorbed hydrogen species. Therefore, the following assumptions are made in our study:

- H and  $\text{H}_2$  can both diffuse in the nitride and will be considered as one group of species called H.
- The released H species cannot be re-absorbed by the nitride SiN lattice.
- Hydrogen bonds in SiN (NH and SiH) will be labelled SiNH and their initial concentration before annealing is  $\text{SiNH}_0$ .
- No free diffusing H species are present in nitride before annealing.

Following the previous assumptions, H and SiNH concentrations in nitride can be modelled using the following equations in a one dimensional (1D) system along x direction:

$$\frac{\partial \text{H}_{\text{nit}}}{\partial t} = D(\text{H})_{\text{nit}} \frac{\partial^2 \text{H}_{\text{nit}}}{\partial x^2} + K(\text{H})_{\text{nit}} \text{SiNH} \quad (3.8)$$

$$\frac{\partial \text{SiNH}}{\partial t} = -K(\text{H})_{\text{nit}} \text{SiNH} \quad (3.9)$$

$D(\text{H})_{\text{nit}}$  is the H diffusivity in nitride in  $\text{cm}^2.\text{s}^{-1}$  and  $K(\text{H})_{\text{nit}}$  is the H desorption constant in  $\text{s}^{-1}$ . Both  $D(\text{H})_{\text{nit}}$  and  $K(\text{H})_{\text{nit}}$  are extracted from coupled stress/TDS measurements [16] and follow Arrhenius laws that are temperature dependent with an exponential pre-factor and an activation energy. Stress and TDS measurements were fitted numerically using equations 3.8 and 3.9 and  $K(\text{H})_{\text{nit}}$  and  $D(\text{H})_{\text{nit}}$  were extracted for nitrides NA and NC. Corresponding results are given in table 3.2 with the corresponding pre-exponential factors, activation energies and values at  $1000^\circ\text{C}$  (in italic).

From table 3.2, we can observe that hydrogen effective diffusivity in NC nitride is much higher than the one in NA nitride, which can be explained by the difference in density of NA and NC nitrides respectively of 2.65 and 2.15  $\text{g.cm}^{-3}$  (table 3.2). These results are in agreement with literature data [18–20] where a hydrogen diffusivity increase with a nitride density decrease was observed.  $K(\text{H})_{\text{nit}}$  could not be deduced for NB nitride from stress/TDS measurements. However from table 3.2, we can see that NC density of 2.52  $\text{g.cm}^{-3}$  is close to NA density of 2.65  $\text{g.cm}^{-3}$  and therefore we assume that hydrogen effective diffusivity in NC nitride is  $1.05 \times 10^{-14} \times e^{-\frac{0.01(\text{eV})}{k_B T}} \text{cm}^2.\text{s}^{-1}$ , equal to the one in NA nitride and of the same order of magnitude as the one observed in literature at  $1000^\circ\text{C}$  for LPCVD nitride ( $5 \times 10^{-14} \text{cm}^2.\text{s}^{-1}$  in [21]). Considering this diffusivity value for NC nitride, the reaction constant  $K(\text{H})_{\text{nit}}$  at  $1000^\circ\text{C}$  was deduced from simulations using equations 3.8 and 3.9 and is given in table 3.2. Finally, NA, NB and NC nitrides density and their corresponding approximate

initial SiNH<sub>0</sub> bonds concentrations measured by Fourier transform infrared spectroscopy (FTIR) are given in table 3.2.

Table 3.2: Summary of physical parameters of the different materials used in this study:  $K(H)_{\text{nit}}$  and  $D(H)_{\text{nit}}$  (equations 3.8 and 3.9) extracted from coupled stress/TDS measurements [16] for nitrides NA to NC, initial SiNH bonds concentration SiNH<sub>0</sub> and OH bonds concentration OH<sub>0</sub> extracted from FTIR measurements for nitride NA to NC and oxide OA and OB. Nitrides density  $\rho$  was obtained by simple weighing. Values at 1000°C are in italic.

	$K(H)_{\text{nit}}(\text{s}^{-1})$	$D(H)_{\text{nit}}(\text{cm}^2.\text{s}^{-1})$	SiNH <sub>0</sub> (cm <sup>-3</sup> )	OH <sub>0</sub> (cm <sup>-3</sup> )	$\rho(\text{g.cm}^{-3})$
NA	$5.71e^{-\frac{0.82(\text{eV})}{k_B T}}$ <i><math>3.27 \times 10^{-3}</math></i>	$1.05 \times 10^{-14} \times e^{-\frac{0.01(\text{eV})}{k_B T}}$ <i><math>9.59 \times 10^{-15}</math></i>	$\sim 10^{23}$		2.65
NB	<i><math>9.0 \times 10^{-4}</math></i>	$1.05 \times 10^{-14} \times e^{-\frac{0.01(\text{eV})}{k_B T}}$ <i><math>9.59 \times 10^{-15}</math></i>	$\sim 10^{22}$		2.52
NC	$6.34 \times 10^4 e^{-\frac{1.22(\text{eV})}{k_B T}}$ <i><math>9.53 \times 10^{-1}</math></i>	$4.07 \times 10^{-10} \times e^{-\frac{0.23(\text{eV})}{k_B T}}$ <i><math>5.02 \times 10^{-11}</math></i>	$\sim 10^{23}$		2.15
OA				$\sim 10^{21}$	
OB				$\sim 10^{20}$	

In order to characterize hydrogen related species in oxides OA and OB, samples S'<sub>1</sub> to S'<sub>4</sub> will be used. In the deposited oxides of this study, hydrogen is mainly in the SiH and OH bonds form [11, 13], the latter corresponding to HRDs already seen in reaction 3.2 and enhancing boron diffusion in the oxide. However, coupled stress/TDS method cannot be used for oxides as for nitrides [16] in order to extract hydrogen related species characteristics, mainly because deposited oxides are rich with water H<sub>2</sub>O molecules [22], and many indistinguishable chemical reactions can lead to the formation of HRDs [23]. Thus, hydrogen related species characteristics in oxides OA and OB will be determined indirectly using boron SIMS profiles in silicon and oxide of Fig. 3.2, as it will be shown in 3.2.3.2. As for nitride and in order to model hydrogen related species in oxide, the following assumptions are made:

- All the hydrogen diffusing species in oxide will be considered as one group of species called H.
- OH bonds (or HRDs) are considered as the only hydrogen bonds in oxide and their initial concentration before annealing is OH<sub>0</sub>.
- No free diffusing H species are present in oxide before annealing.
- Contrarily to the SiNH bonds in nitride (equations 3.8 and 3.9), OH bonds can both absorb and desorb H species respectively from and into the oxide.

Given the previous assumptions, H and OH concentrations in the oxide can be modelled using the following equations in a one dimensional (1D) system along x direction:

$$\frac{\partial H_{\text{ox}}}{\partial t} = D(H)_{\text{ox}} \frac{\partial^2 H_{\text{ox}}}{\partial x^2} - K_a(H)_{\text{ox}} H_{\text{ox}} + K_d(H)_{\text{ox}} OH \quad (3.10)$$

$$\frac{\partial OH}{\partial t} = K_a(H)_{\text{ox}} H_{\text{ox}} - K_d(H)_{\text{ox}} OH \quad (3.11)$$

$D(H)_{\text{ox}}$  is the H effective diffusivity in oxide in  $\text{cm}^2.\text{s}^{-1}$ ,  $K_a(H)_{\text{ox}}$  and  $K_d(H)_{\text{ox}}$  are respectively the hydrogen absorption and desorption constants for OH bonds in  $\text{s}^{-1}$ .

In summary, equations 3.8, 3.9, 3.10 and 3.11 model diffusion and reaction mechanisms of hydrogen related species in nitride and oxide materials. Considering the transfer of free hydrogen from nitride to oxide at the nitride/oxide interface, it can be modelled by a simple segregation model, with the flux  $\vec{j}$  of hydrogen between the two materials and  $\vec{n}$  the vector normal to the interface. The corresponding boundary condition is:

$$\vec{j}(H) \cdot \vec{n} = k \left( H_{\text{nit}} - \frac{H_{\text{ox}}}{s} \right) \quad (3.12)$$

where  $k$  (in  $\text{s}^{-1}$ ) and  $s$  (no unit) are respectively the transfer and segregation parameters.  $H_{\text{nit}}$  and  $H_{\text{ox}}$  are respectively hydrogen concentration at nitride side and oxide side of the nitride/oxide interface. In order to model hydrogen degassing during the thermal anneal, a recombination boundary condition was defined for hydrogen at air/nitride interface:

$$\vec{j}(H) \cdot \vec{n} = k_{\text{rec}} H_{\text{nit}} \quad (3.13)$$

where  $k_{\text{rec}}$  (in  $\text{s}^{-1}$ ) is the recombination constant. It should be noticed that the same boundary condition is fixed at the air/oxide interface in order to allow hydrogen degassing in a simple oxide/silicon stack and reproduce nitride capping layer effect when comparing it to a full nitride/oxide/silicon stack [6].

Considering hydrogen related species, in addition to experimentally extracted parameters of table 3.2,  $K_a(H)_{\text{ox}}$  and  $K_d(H)_{\text{ox}}$  for free hydrogen absorption and desorption by SiO bonds, are extracted from boron SIMS results of Fig. 3.2 in samples S'1 to S'4 to be shown in 3.2.3.2. Finally as for SiNH bonds, OH bonds concentrations in oxides OA and OB are extracted from FTIR measurements and given in table 3.2.

Before modelling temporal evolution of boron and hydrogen related species densities, we will give a detailed analysis of equations 3.8, 3.9, 3.10 and 3.11. As a first approximation, if we consider an independent conservative (no recombination at interfaces) nitride system with an initial homogeneous SiNH bonds concentration  $\text{SiNH}_0$  to be extracted from table 3.2, a zero initial homogeneous (no diffusion) hydrogen concentration, solving analytically 1<sup>st</sup> order differential equations 3.8 and 3.9 leads to:

$$H_{\text{nit}}(t) = \text{SiNH}_0 \left( 1 - e^{-K(H)_{\text{nit}} t} \right) \quad (3.14)$$

$$\text{SiNH}(t) = \text{SiNH}_0 \cdot e^{-K(H)_{\text{nit}} t} \quad (3.15)$$

With parameters values from table 3.2, we show in Fig. 3.3 the corresponding SiNH and hydrogen dose (in  $\text{cm}^{-2}$ ) temporal evolution during the  $1000^\circ\text{C}$  anneal for NA, NB and NC nitrides 55 nm thick. As expected from the simple analytical temporal solutions 3.14 and 3.15, Fig. 3.3 shows that the higher the reaction constant  $K(H)_{\text{nit}}$ , the higher is the dissolution of SiNH bonds and formation of free hydrogen.

Now if we consider oxide, assuming an independent conservative (no recombination at interfaces) oxide system with an initial homogeneous OH bonds concentration  $\text{OH}_0$  to be extracted from table 3.2, a zero initial homogeneous (no diffusion) hydrogen concentration, solving the system of the two first order differential equations 3.10 and 3.11 leads to:

$$H_{\text{ox}}(t) = \frac{K_d(H)_{\text{ox}} \text{OH}_0}{K_a(H)_{\text{ox}} + K_d(H)_{\text{ox}}} - \frac{K_d(H)_{\text{ox}} \text{OH}_0}{K_a(H)_{\text{ox}} + K_d(H)_{\text{ox}}} e^{-(K_a(H)_{\text{ox}} + K_d(H)_{\text{ox}}) t} \quad (3.16)$$

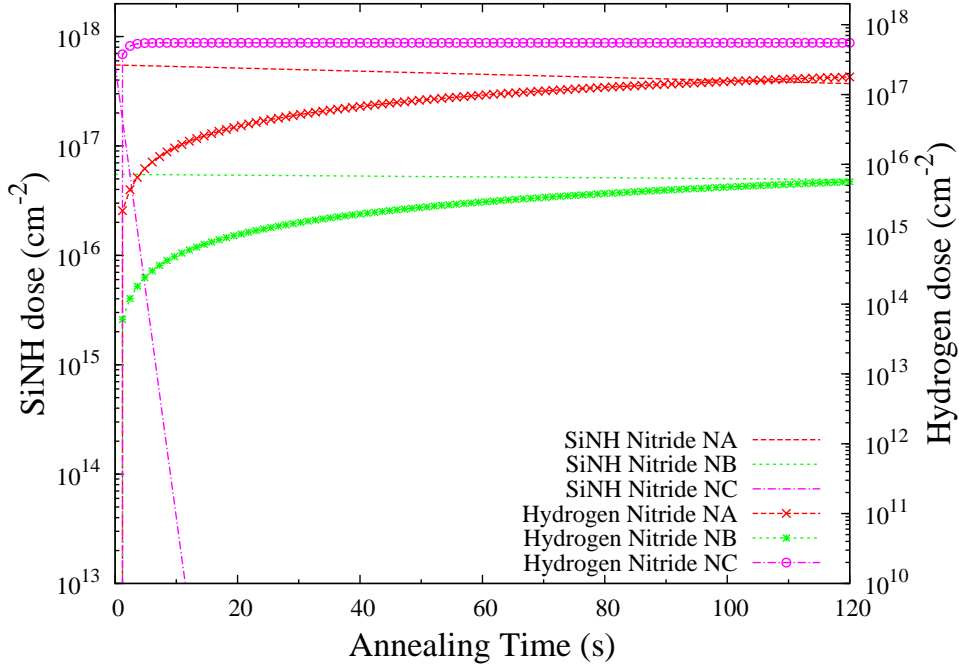


Figure 3.3: Temporal evolution of SiNH bonds (lines) and hydrogen (lines + symbols) density for homogeneous isolated nitrides NA, NB and NC during the 1000°C 2 min anneal using the analytical solutions 3.14 and 3.15.

$$OH(t) = \frac{K_a(H)_{ox} OH_0}{K_a(H)_{ox} + K_d(H)_{ox}} + \frac{K_d(H)_{ox} OH_0}{K_a(H)_{ox} + K_d(H)_{ox}} e^{-(K_a(H)_{ox} + K_d(H)_{ox})t} \quad (3.17)$$

From equations 3.16 and 3.17:  $H_{ox}(0) = 0$ ,  $OH(0) = OH_0$ ,  $H_{ox}(\infty) = \frac{K_d(H)_{ox} OH_0}{K_a(H)_{ox} + K_d(H)_{ox}}$  and  $OH(\infty) = \frac{K_a(H)_{ox} OH_0}{K_a(H)_{ox} + K_d(H)_{ox}}$ . With parameters values from table 3.2,  $K_a(H)_{ox}$  fixed at  $0.01 \text{ s}^{-1}$  for both oxides and  $K_d(H)_{ox}$  fixed respectively at 0.8 and  $0.6 \text{ s}^{-1}$  respectively for oxides OA and OB, we show in Fig. 3.4 the corresponding OH and hydrogen dose (in  $\text{cm}^{-2}$ ) temporal evolution during the 1000°C anneal for OA and OB 40 nm thick oxides. From Fig. 3.4, we can observe that oxides OA and OB have the same behaviour with slight differences due to different  $K_d(H)_{ox}$  values for the two oxides. We can also notice that constant equilibrium densities  $H_{ox}(\infty)$  and  $OH(\infty)$  are achieved respectively for hydrogen and OH bonds after approximately 10 s of anneal.

Fig. 3.3 and 3.4 showed temporal evolution of hydrogen related species during thermal annealing where oxide and nitride material were considered independently. However, in the real systems of nitride/oxide/silicon stacks, hydrogen is mobile, diffuses in both oxide and nitride and can be transferred to neighbouring materials as suggested by conditions 3.12 and 3.13. Therefore, hydrogen related species temporal evolution in the real system will be given in 3.2.3.2 in association with boron out-diffusion modelling.

### 3.2.3.2 Boron out-diffusion modelling

After the presentation of the model that drive the hydrogen dynamics in oxide and nitride stack, we address the boron diffusion here introducing first the diffusion through fixed traps and then through mobile traps.

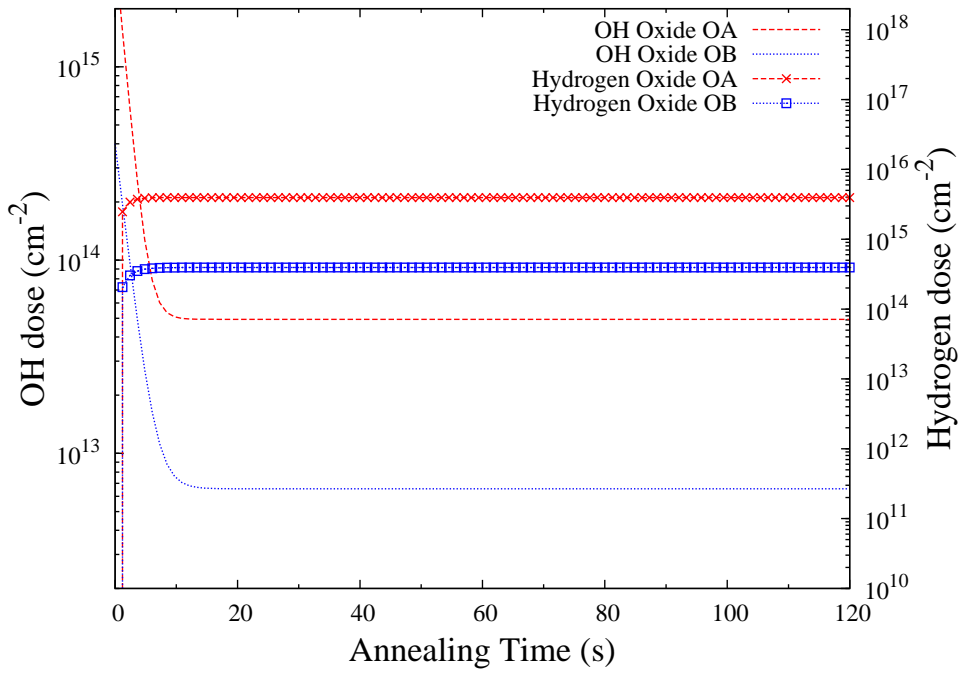


Figure 3.4: Temporal evolution of OH bonds (lines) and hydrogen (lines + symbols) density for homogeneous isolated oxides OA and OB during the 1000°C 2 min anneal using the analytical solutions 3.16 and 3.17.

Regarding previous remarks, we first considered boron diffusion in oxide as a function of OH bonds, modelled using diffusion constant in equation 3.3, where boron diffusivity depends on the OH bonds concentration. The following boron diffusion equation is considered in the oxide:

$$\frac{\partial B_{ox}}{\partial t} = D_0(B) \left( 1 + \frac{OH}{OH_{ref}} \right)^n \frac{\partial^2 B_{ox}}{\partial x^2} \quad (3.18)$$

The set of advanced models of SProcess simulator [24] was used and hydrogen related species equations were integrated using Alagator scripting language [24]. Boron transfer from oxide to silicon for out-diffusion modelling used a three phase segregation boundary condition at the oxide/silicon interface [25, 26], the three phases being oxide, silicon and oxide/silicon interface defined by the following system of equations in a 1D system:

$$\begin{aligned} \frac{\partial B_{ox/si}}{\partial t} &= D_{0,ox/si} \frac{\partial^2 B_{ox}}{\partial x^2} + F_{ox} + F_{si} \\ F_{ox} &= T_{ox} (C_{max} - B_{ox/si}) B_{ox} - E_{ox} (B_{ox}^s - B_{ox}) B_{ox/si} \\ F_{si} &= T_{si} (C_{max} - B_{ox/si}) B_{si} - E_{si} (B_{si}^s - B_{si}) B_{ox/si} \end{aligned} \quad (3.19)$$

First line equation of system 3.19 is boron diffusion in oxide/silicon interface  $B_{ox/si}$  where  $D_{0,ox/si}$  is the diffusion constant,  $F_{ox}$  and  $F_{si}$  are respectively boron fluxes to oxide and to silicon where the different parameters in 2<sup>nd</sup> and 3<sup>rd</sup> lines of equation 3.19 are:  $B_{ox}$  and  $B_{si}$  the respective boron concentration at oxide and silicon sides of the oxide/silicon interface,  $B_{ox}^s$  and  $B_{si}^s$  the respective boron solubility limit in oxide and silicon,  $T_{ox}$  and  $T_{si}$  the trapping rates from oxide and silicon,  $E_{ox}$  and  $E_{si}$  emission rates to oxide and silicon and  $C_{max}$  maximum density of traps for boron at the oxide/silicon interface.

From SIMS results of Fig. 3.2 showing different dose loss for samples S'₁ to S'₄, a set of model parameters for OH and boron was chosen in order to reproduce boron profiles in silicon. The different



parameters values at 1000°C are given in table 3.3, where we can see that all the OH and boron parameters from equations 3.10, 3.11 and 3.18 are identical for both OA and OB oxides, except for the hydrogen desorption constant  $K_d(H)_{ox}$  which is higher for OA oxide (0.8) in comparison to OB oxide (0.6).

TCAD process simulations of boron diffused profiles for the different stacks using tables 3.2 and 3.3 model parameters for OH bonds, hydrogen and boron in oxide, SiNH bonds and hydrogen in nitride, are given in Fig. 3.5 and compared to SIMS results. From Fig. 3.5, a good agreement between SIMS and simulation results is obtained for boron diffused profiles in silicon. However, even though the out-diffusion mechanism is qualitatively reproduced in oxide with an effective diffusion in oxide increasing with the dose loss in silicon, we can see that as discussed previously, boron diffused profiles in oxide have an erfc shape in agreement with Fick's second law of equation 3.18. In addition, it should be noticed that the general trend given in the legend of percentage dose loss defined by the ratio of the integrated dose in silicon after diffusion on the  $BF_2$  implanted dose ( $5.10^{14} \text{ cm}^{-2}$ ) is the same between SIMS and TCAD simulations. However, some differences are observed between the two values probably due to boron peak SIMS uncertainties at the oxide/silicon interface. Combining equation 3.18 for boron diffusion [14] with hydrogen related species temporal evolution of our set of equations 3.8, 3.9, 3.10 and 3.11, we are able to reproduce boron dose loss from silicon for the different stacks.

Table 3.3: Summary of model parameters for OH and boron species related to equations 3.10, 3.11 and 3.18 for OA and OB oxides in order to match boron SIMS profiles in silicon from Fig. 3.2. Different values between oxides OA and OB are in italic.

	$K_a(H)_{ox}(s^{-1})$	$K_d(H)_{ox}(s^{-1})$	$D_0(B)(cm^2.s^{-1})$	$OH_{ref}(cm^{-3})$	n
OA	0.01	<i>0.8</i>	$3.07 \times 10^{-18}$	$2.20 \times 10^{16}$	1.0
OA	0.01	<i>0.6</i>	$3.07 \times 10^{-18}$	$2.20 \times 10^{16}$	1.0

Boron diffusion equation 3.18 models correctly boron dose loss in silicon as a function of OH bonds concentration in oxide after simulating the different hydrogen related species temporal evolution in both nitride and oxide. Qualitatively, boron out-diffusion mechanism is captured with a correlation between boron dose loss and diffusivity in oxide. However, boron diffused profiles in oxide are not correctly reproduced as we can see in Fig. 3.5. Typical Fick's law based erfc diffused profiles are observed in our simulations, while exponential profiles are obtained experimentally, suggesting a boron diffusion using a migrating species form before recombining and forming immobile species. In this case, boron is suspected to diffuse using a long hop mechanism with a characteristic length  $\lambda$ , defined as the mean projected path length for mobile B between its formation and recombination [27]. From SIMS results and previous simulations of Fig. 3.5, it was observed that boron diffusion in oxide is a function of OH bonds concentration. However, from SIMS results of Fig. 3.2, it is also observed that the exponential tails in oxide have different slopes with a decreasing slope from sample S'<sub>1</sub> to S'<sub>4</sub>. Consequently, we have different hopping lengths for the different samples suggesting that not only boron diffusivity depends on OH concentration but also the hopping length  $\lambda$ .

Regarding previous remarks, let us remind that in silicon, long hop mechanism has already been studied by Cowern et al. [28] where boron diffusing species are boron interstitial pairs BI and the immobile one is substitutional boron B<sub>sub</sub>. Diffusion in silicon takes place with a kick-out mechanism [29]. As discussed in details previously, Fair et al. [8] showed that boron diffuses in oxide using HRDs (or OH bonds) as shown in reaction 3.2. Therefore, by adapting the boron diffusion mechanism of Cowern et al. [28], we consider in the case of oxide, that boron is in two forms: an immobile species



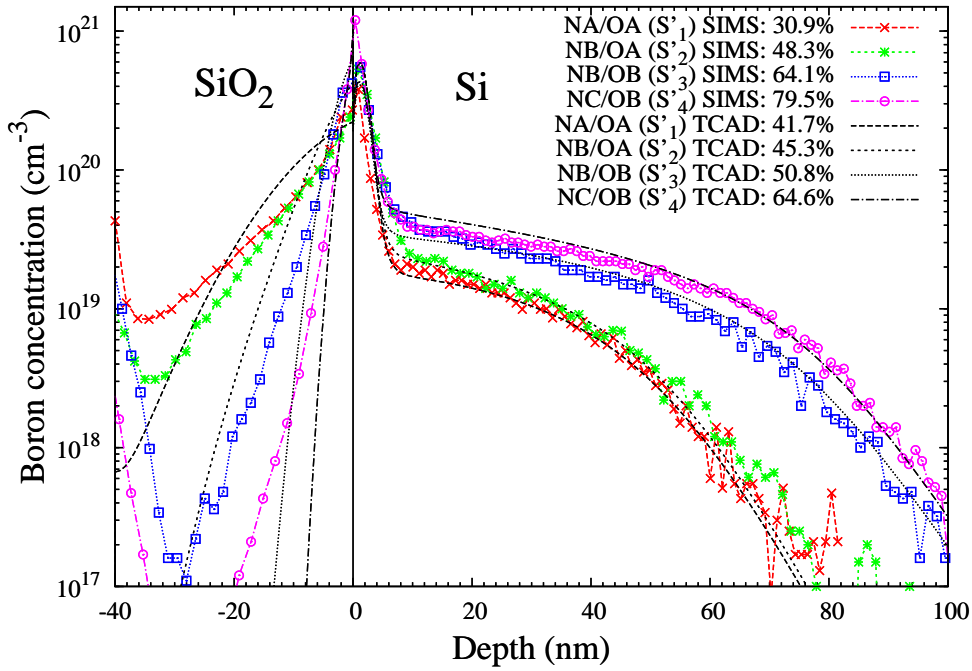


Figure 3.5: Boron SIMS versus TCAD results for samples S'₁ to S'₄ (table 3.1) using equation 3.18 for boron diffusion in oxide, in association with equations 3.8, 3.9, 3.10 and 3.11 for hydrogen related species temporal evolution. Final percentage of boron dose loss in silicon after anneal is also given in the legend.

B such as substitutional boron in silicon, and diffusing species BOH via OH HRDs such as BI pair in silicon formed following the reaction of immobile B and an OH bond (reaction 3.2). The following two equations are consequently set for B and BOH in oxide:

$$\frac{\partial B}{\partial t} = \left( r_0 \left( \frac{OH}{OH_0} \right)^2 \right) BOH - gB.OH \quad (3.20)$$

$$\frac{\partial BOH}{\partial t} = \left( D(B)_{ox} \frac{OH}{OH_{ref}} \right) \frac{\partial^2 BOH}{\partial x^2} - \left( r_0 \left( \frac{OH}{OH_0} \right)^2 \right) BOH + gB.OH \quad (3.21)$$

In equations 3.20 and 3.21, we can see that BOH is the diffusing species, and as in equation 3.18, BOH diffusivity  $D(B)_{ox} \frac{OH}{OH_{ref}}$  is enhanced with the OH concentration using the multiplying factor in front of the 1<sup>st</sup> right hand side (r.h.s.) of equation 3.21 with a reference OH concentration  $OH_{ref}$ . After a diffusion step with a characteristic length  $\lambda$ , BOH will recombine and form and immobile boron atom B. The recombining factor  $r_0 \left( \frac{OH}{OH_0} \right)^2$  in 1<sup>st</sup> and 2<sup>nd</sup> r.h.s terms of the respective equations 3.20 and 3.21 depends on OH concentration in oxide and the two fitting parameters  $r_0$  (in s<sup>-1</sup>) and  $OH_0$  (in cm<sup>-3</sup>). As for kick-out mechanism for BI pairs in silicon, BOH can also be generated following the reaction between B and OH (reaction 3.2) with a generation constant  $g$  (in cm<sup>-3</sup>.s<sup>-1</sup>) in 2<sup>nd</sup> and 3<sup>rd</sup> terms of equations 3.20 and 3.21.

It should be noticed that in addition to absorption and desorption constants  $K_a(H)_{ox}$  and  $K_d(H)_{ox}$ , boron diffusion model in oxide of equations 3.20 and 3.21 has five different calibration parameters:  $D(B)_{ox}$ ,  $OH_{ref}$ ,  $r_0$ ,  $OH_0$  and  $g$ . Therefore, given the number of experimental conditions with four spacer stacks S'₁ to S'₄, the set of parameters values found in our simulations of SIMS results, and even the formulation for the recombination constant dependence with the square of the OH concentration are

certainly not unique. However, the aim of this work is to show for the first time that boron diffusion in oxide can be modelled using a long hop mechanism in order to reproduce the boron exponential tails clearly observed experimentally. The different model parameters of equations 3.20 and 3.21 are given in table 3.4.  $K_a(H)_{ox}$  absorption constant from table 3.4 was modified from 0.01 to 0.008 for oxide OB.  $K_d(H)_{ox}$  desorption constant from table 3.4 was modified from 0.8 to 3.8 and 0.6 to 3.6 respectively for oxides OA and OB.

Table 3.4: Summary of diffusion model parameters at 1000°C for boron in both oxides OA and OB including the long hop mechanism from equations 3.20 and 3.21.

Oxide	$D(B)_{ox} (cm^2.s^{-1})$	$OH_{ref} (cm^{-3})$	$OH_0 (cm^{-3})$	$r_0 (s^{-1})$	$g (cm^{-3}.s^{-1})$
	$3.07 \times 10^{-17}$	$7.02 \times 10^{15}$	$9.02 \times 10^{15}$	$2.50 \times 10^{-8}$	$1.42 \times 10^{-30}$

With the set of parameters of table 3.2 and 3.4, boron diffused profiles for samples S'<sub>1</sub> to S'<sub>4</sub> are shown in Fig. 3.6. A good agreement between SIMS and TCAD simulated results is obtained for boron diffused profiles in the different samples, including boron profiles in silicon and exponential shaped profiles in oxide. Boron dose loss from silicon is qualitatively reproduced (legends Fig. 3.6) with slight differences again due to SIMS artefacts at the oxide/silicon interface.

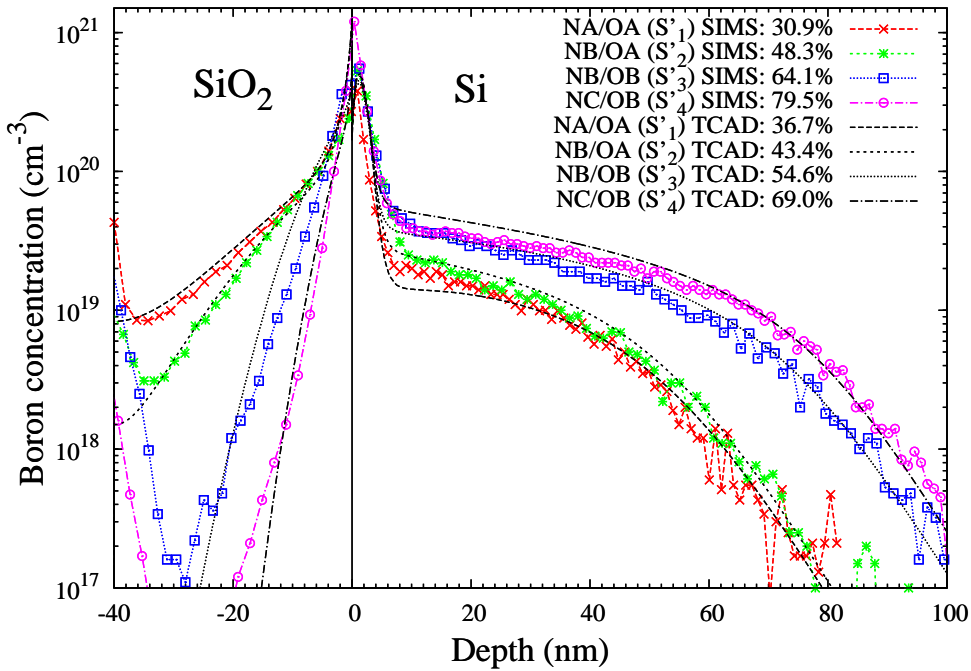


Figure 3.6: Boron SIMS versus TCAD results for samples S'<sub>1</sub> to S'<sub>4</sub> (table 3.1) using equations 3.20 and 3.21 for boron diffusion in oxide with the long hop mechanism, in association with equations 3.8, 3.9, 3.10 and 3.11 for hydrogen related species temporal evolution. Final percentage of boron dose loss in silicon after anneal is also given in the legend.

In association with boron dose loss models of equations 3.20 and 3.21, hydrogen related species temporal evolution can be evaluated thanks to equations 3.8, 3.9, 3.10 and 3.11. Samples S'<sub>1</sub> and S'<sub>4</sub> of Fig. 3.6 showing respectively the lowest and highest boron dose loss will be compared. Hydrogen related species temporal evolution in oxide and nitride during the thermal anneal is shown in Fig. 3.7. SiNH bonds temporal evolution in nitride is shown in Fig. 3.7a. Knowing that SiNH bonds simply dissolve by emitting free hydrogen and do not react with neighbouring materials it is not surprising

that the SiNH density temporal evolution of Fig. 3.7a is the same as the one shown in Fig. 3.3 using analytical equation 3.15. Hydrogen density versus time in both nitride and oxide is shown in Fig. 3.7b, which as expected is quite different from the results using the approximations of Fig. 3.3 and 3.4. Indeed, in addition to different OH bonds absorption and desorption constants  $K_a(H)_{ox}$  and  $K_d(H)_{ox}$  in oxide in comparison to results shown in Fig. 3.3 and 3.4, in these full simulations, hydrogen can diffuse in both oxide and nitride and can be transferred from nitride to oxide (and vice versa) and finally can be degassed by recombining at the air/nitride interface.

Sample S'<sub>4</sub> with NC nitride and OB oxide, is interesting in these simulations. From desorption reaction constant in nitride  $K(H)_{nit}$  ( $9.53 \times 10^{-1} \text{ s}^{-1}$  table 3.2), it is expected that hydrogen concentration in nitride quickly reaches its maximum concentration as seen for NC nitride using the simplified assumptions in Fig. 3.3. However, in the full simulations, hydrogen diffusivity in NC nitride  $D(H)_{nit}$  at 1000°C equals  $5.02 \times 10^{-11} \text{ cm}^2.\text{s}^{-1}$  (table 3.2) and is almost four orders of magnitude higher than the one for NA and NB nitrides of  $9.59 \times 10^{-15} \text{ cm}^2.\text{s}^{-1}$  (table 3.2). Consequently, given these high values of both  $K(H)_{nit}$  and  $D(H)_{nit}$ , hydrogen will quickly desorb from the SiNH bonds and recombine at the nitride/air interface. This will lead to a complete degassing of hydrogen from nitride, a transfer of hydrogen from oxide to nitride due to the resulting densities gradient between oxide and nitride. Hydrogen will then degas from oxide to nitride to air and OH bonds in oxide will completely desorb which can be seen from hydrogen and OH bonds fast density decrease respectively in Fig. 3.7c and 3.7d. In sample S'<sub>4</sub>, nitride does not have a capping effect for hydrogen and is almost transparent for hydrogen degassing. S'<sub>4</sub> stack behaves like a simple oxide/silicon stack where hydrogen degassing reduces significantly boron out-diffusion [6]. Finally, OH bonds density is correlated to boron dose loss from silicon. Indeed, from Fig. 3.7c, OH bonds density decreases from samples S'<sub>1</sub> to S'<sub>4</sub> leading to a boron dose loss decrease from S'<sub>1</sub> to S'<sub>4</sub> as observed on Fig. 3.7d of boron dose temporal evolution in oxide and silicon for the different samples.

Boron out-diffusion model developed here and also described in [30], is also able to reproduce nitride capping effect already observed in literature [6]. In the case of a simple oxide/silicon stack, we considered that the air/oxide interface boundary condition is the same as the air/nitride boundary condition of equation 3.13. Therefore, if the oxide is directly in contact with air, hydrogen will degas and OH bonds concentration will decrease in oxide leading to a lowering of boron dose loss. In Fig. 3.8, we compare boron diffused profiles simulation results for S'<sub>1</sub> (NA/OA), S'<sub>2</sub> (NB/OA) and a simple oxide/silicon stack with OA oxide and its corresponding OH bonds density temporal evolution. Thus from Fig. 3.8 for the simple oxide/silicon case OA, boron dose loss is lower than S'<sub>1</sub> and S'<sub>2</sub> nitride/oxide/silicon stacks due to a degassing of hydrogen and a decrease in OH bonds density.

Following boron out-diffusion modelling in Fig. 3.6, it should be noticed that induced dose loss in silicon for the different stacks S'<sub>1</sub> to S'<sub>4</sub> is expected to have an influence on electrical characteristics of CMOS based devices as it will be seen in chapter 4. A first investigation of this aspect will be given here by modelling boron layer sheet resistance  $R_s$  of samples S'<sub>1</sub> to S'<sub>4</sub> in addition to the simple oxide/silicon stack OA of Fig. 3.8. Corresponding  $R_s$  temporal evolution is given in Fig. 3.9. Sheet resistance calculations used Masetti et al. formulas [31] and from Fig. 3.9, we can see that the higher the dose loss the higher is  $R_s$ . This behaviour is expected because  $R_s$  decreases when dopant activated dose and junction depth increase. Therefore, from these sheet resistance results, boron dose loss is expected to impact electrical performances of CMOS based devices as it will be observed in chapter 4.

### 3.3 Lanthanum diffusion in high-k stacks

The results of previous section, but also chapter 2 concentrated on dopant atoms and mainly boron diffusion in silicon and oxide materials. Such diffusion mechanisms impact electrical behaviour of

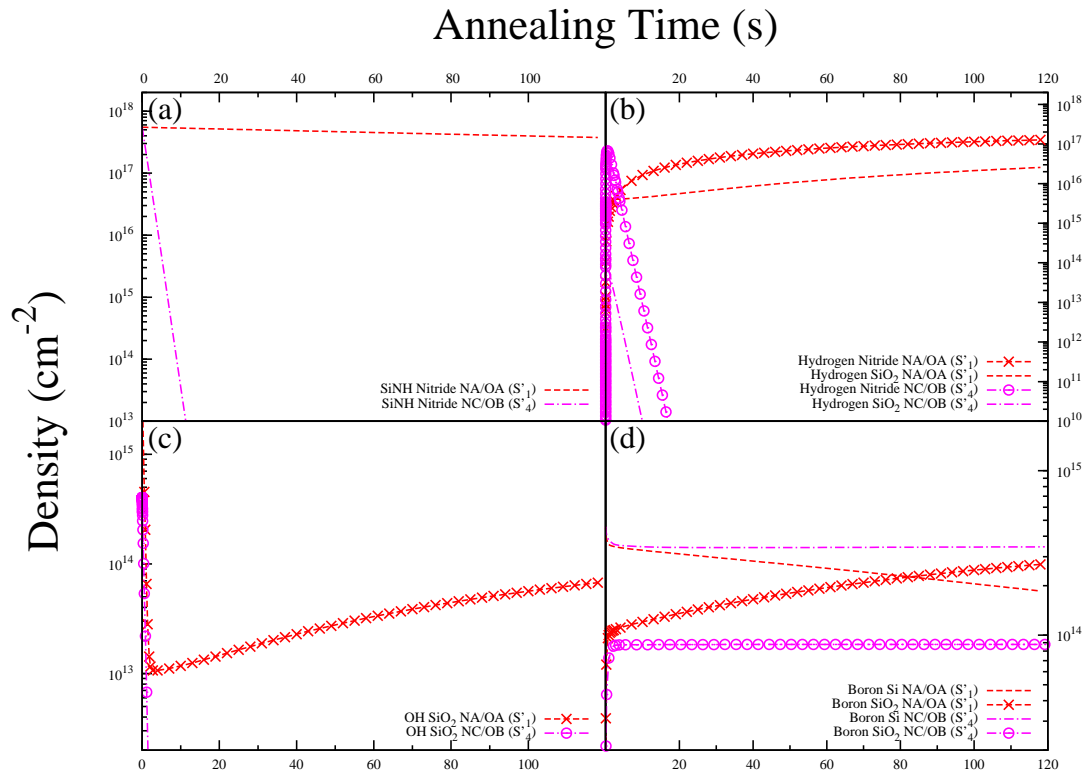


Figure 3.7: TCAD temporal evolution of (a) SiNH bonds density in nitride, (b) hydrogen density in nitride and oxide, (c) OH bonds density in oxide and (d) boron density in oxide and silicon for samples S'<sub>1</sub> and S'<sub>4</sub> during the 1000°C 2 min anneal using equations 3.8, 3.9, 3.10 and 3.11 for hydrogen related species and equations 3.20 and 3.21 for boron diffusion in oxide.

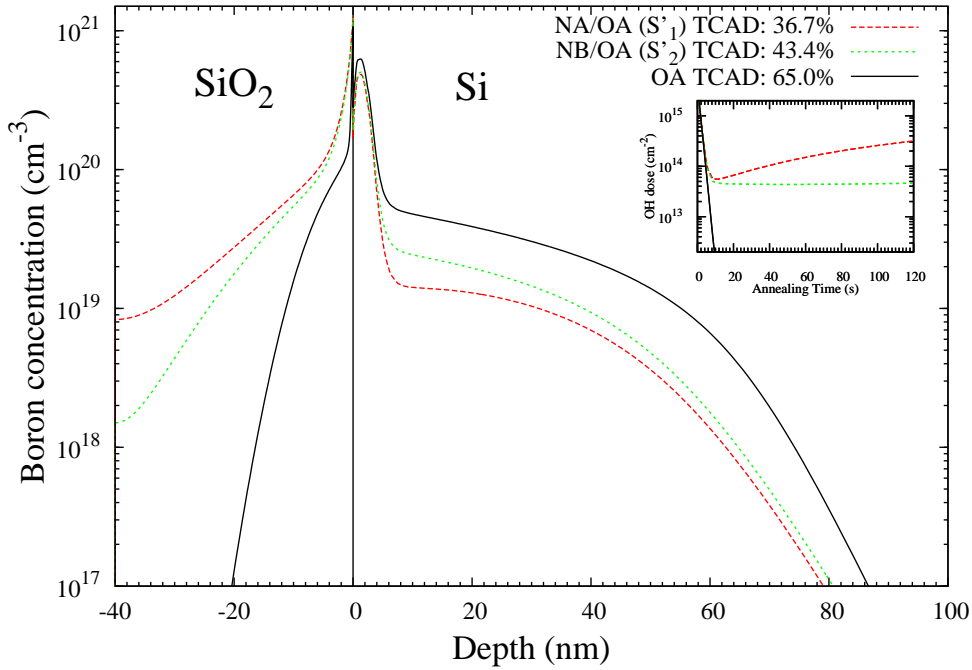


Figure 3.8: Boron TCAD results for the two nitride/oxide/silicon stacks  $S'_1$  and  $S'_2$ , in comparison to a simple oxide(OA)/silicon stack showing the capability of the model in reproducing the capping effect of nitride on hydrogen degassing during the  $1000^\circ\text{C}$  2 min thermal anneal. Final percentage of boron dose loss in silicon is also given in the legend.

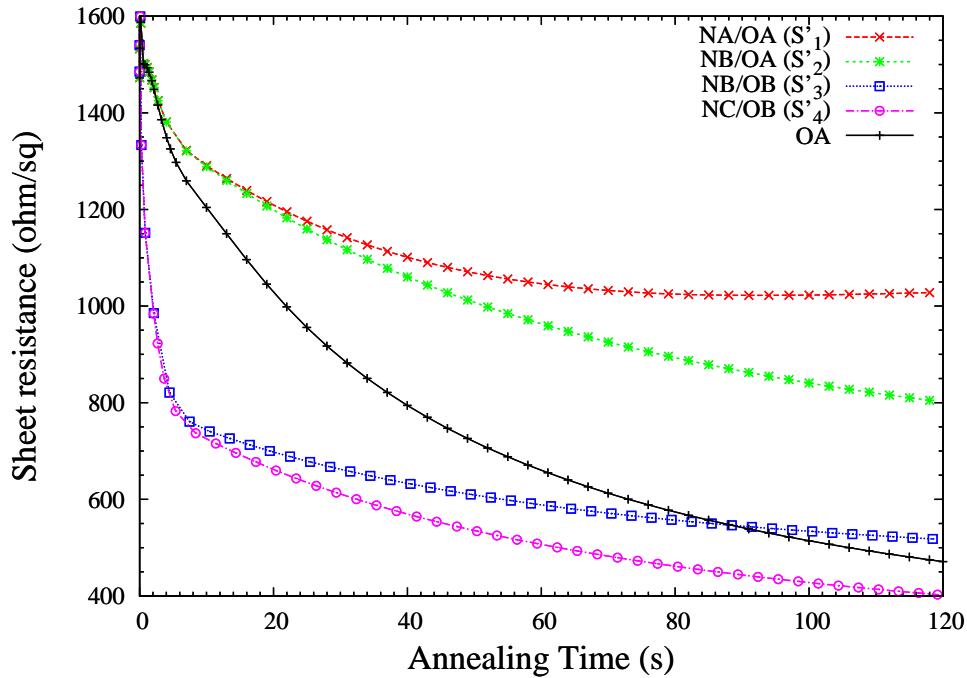


Figure 3.9: TCAD temporal evolution of sheet resistance  $R_s$  for samples  $S'_1$  to  $S'_4$  (table 3.1) and the simple oxide(OA)/silicon stack (Fig. 3.8) during the  $1000^\circ\text{C}$  2 min thermal anneal.

CMOS devices. However, it should be noticed that diffusion of other non conventional chemical species in multi-materials stacks following thermal annealing may also have an impact on electrical characteristics of CMOS based devices. In the frame of the PhD and ATEMOS project [1], one particular species used in advanced high-k stacks for nMOS transistors was investigated: lanthanum (La). After an introduction in 3.3.1 to high-k dielectrics and La use in advanced nMOS transistors, we will present in 3.3.2 our dedicated experimental structures consisting of TiN/La<sub>2</sub>O<sub>3</sub>/HfSiON/SiO<sub>2</sub>/Si high-k stacks in order to investigate La diffusion. These experiments will be used for the development of a La diffusion model in TiN/La<sub>2</sub>O<sub>3</sub>/HfSiON/SiO<sub>2</sub>/Si high-k stacks [32] to be presented in 3.3.3.

### 3.3.1 Introduction to high-k stacks and the use of lanthanum

In order to reduce power consumption in the sub-32 nm CMOS technologies, high-k dielectric materials are used in association with metal gate materials [33]. Indeed, the MOS or more generally a metal insulator silicon (MIS) capacitance is defined by:

$$C = \frac{\kappa \epsilon_0 A}{t} \quad (3.22)$$

where  $\kappa$  is the dielectric constant or relative permittivity of the dielectric material used in the MIS structure,  $\epsilon_0$  is the free space permittivity of  $8.85 \times 10^{-3}$  fF/ $\mu$ m, A the area of the capacitance and t the thickness of the dielectric. Following miniaturization, the classical oxide dielectric thickness t was reduced in order to increase the gate capacitance of MOS transistors and keep the required electrostatic control of the channel of MOS transistor [33]. However, the main drawback of oxide thickness reduction is an increase in gate leakage currents and consequently in overall power consumption.

The capacitance expression 3.22 can be rewritten in terms of equivalent oxide thickness (EOT)  $t_{eq}$  of dielectric constant  $\kappa_{ox} \simeq 3.9$ . Therefore, for a given dielectric with a dielectric constant  $\kappa$ , the EOT  $t_{eq}$  is the theoretical thickness of SiO<sub>2</sub> oxide required to have the same capacitance 3.22 as the dielectric. In order to increase the physical thickness of a given dielectric, its dielectric constant has to be as high as possible, and therefore such dielectrics are labelled high-k. The following relation is verified for the high-k [33]:

$$\frac{t_{eq}}{\kappa_{ox}} = \frac{t_{high-k}}{\kappa_{high-k}} \implies t_{high-k} = \frac{\kappa_{high-k}}{\kappa_{ox}} t_{eq} \quad (3.23)$$

where  $t_{high-k}$  and  $\kappa_{high-k}$  are respectively the high-k thickness and dielectric constant.

Over the last years, hafnium oxides such as HfO<sub>2</sub>, HfSiO<sub>2</sub> and HfSiON deposited on a thin pedestal SiO<sub>2</sub> (or SiON) interfacial layer (IL) were used in microelectronics industry and became a serious alternative to classical SiO<sub>2</sub> dielectrics [34, 35]. In association with the use of high-k dielectric as a MOS capacitance insulator, metal gate (MG) materials are used. MG materials eliminate the depletion effect increasing the EOT, observed for polycrystalline silicon (polysilicon) gates in classical gate schemes. However, while tuning the poly-silicon doping allows modifying the gate effective work function (EWF) and to provide adequate threshold voltages ( $V_t$ ) for both nMOS and pMOS transistors, the use of MGs does not allow a simple modification of the EWF. Therefore, a solution to this problem was to introduce a thin capping layer of a rare-earth oxide between the MG and the high-k dielectric [36, 37]. Several rare-earth oxides can be used in nMOS and pMOS transistors depending on the desired positive or negative  $V_t$  shift. In the case of a nMOS transistor, lanthanum oxide (La<sub>2</sub>O<sub>3</sub>) is used to provide a negative shift in the  $V_t$ . The physical mechanism behind the shift is that in a gate first approach, the high-k and MG are deposited before the fast high temperature spike anneal for source, drain and extensions dopant activation. During the anneal, lanthanum diffuses from the La<sub>2</sub>O<sub>3</sub> capping layer through the high-k material and forms lanthanum silicates that are typically La-SiO bonds at the high-k/IL interface [38–40]. The LaSiO bonds are believed to form electrical dipoles



at the high-k/IL interface, which from literature results are responsible of the  $V_t$  shift [37, 41, 42].

Therefore, in regards of these literature results, the  $V_t$  shift is expected to be related to the number of LaSiO dipoles resulting from La diffusion in the high-k and the LaSiO formation after reaching the high-k/IL interface. In the meantime, technology relevant nMOS MG-high-k stacks such as the TiN/La<sub>2</sub>O<sub>3</sub>/HfSiON/SiO<sub>2</sub>/Si stack to be studied here use ultra-thin high-k and IL with thicknesses not exceeding 3 nm. Such low thickness makes difficult a precise study of La diffusion and reaction mechanisms described above, even though some very interesting results already exist in literature on that subject combining electron loss spectroscopy, X-ray photoelectron spectroscopy and high resolution TEM [40]. In the work to be presented in 3.3.2 and 3.3.3, dedicated TiN/La<sub>2</sub>O<sub>3</sub>/high-k/IL/Si gate stack structures with thick high-k and IL were intentionally designed in order to have a reliable investigation of the physical mechanisms taking place during La diffusion in the high-k stack. The corresponding experiments will be first described in 3.3.2 before being used to build a La diffusion model [32] described in 3.3.3.

### 3.3.2 Experimental investigation of lanthanum diffusion in high-k stacks

The dedicated structures TiN/La<sub>2</sub>O<sub>3</sub>/HfSiON/SiO<sub>2</sub>/Si stacks were prepared using a gate-first approach on 300 mm Si (100) wafers. In order to study diffusion and reaction mechanisms of La in the high-k and IL, two series of samples summarized in table 3.5 were designed: (i) "thick" high-k (15 nm) on "thick" IL (10 nm) corresponding to samples 1 to 8 in table 3.5 and (ii) "thin" high-k (2.5 nm) on "thicker" IL (20 nm) corresponding to samples 9 to 16 in table 3.5. Series (i) and (ii) samples allow us to study the diffusion mechanisms, respectively in the HfSiON high-k and the SiO<sub>2</sub> IL. Initial silicon substrate was cleaned using a hydrofluoric acid solution. A rapid thermal oxidation of the silicon substrate at 1100°C and 1150°C was used to grow respectively a 10 nm for series (i) and 20 nm for series (ii) thick silicon oxide SiO<sub>2</sub> layer. The 2.5 nm HfSiON layer of series (ii) was deposited by metal organic chemical vapour deposition (MOCVD) of HfSiO followed by a decoupled plasma nitridation (DPN) for 90 s in order to inject nitrogen N in the high-k layer. For series (i) samples of 15 nm HfSiON high-k layer, the HfSiO MOCVD and DPN steps were repeated 6 times. In order to homogenize the N density in the HfSiON, a post nitridation anneal was carried for both thin and thick high-k samples. Following the high-k step, a thin La<sub>2</sub>O<sub>3</sub> 1 nm thick capping layer was formed by physical vapour deposition (PVD) followed by the titanium nitride TiN MG 6.5 nm thick deposition by PVD. Finally thermal anneals made in a RTA system at different times and temperatures including 1000°C/50 s and {1040 and 1080}°C/{10, 30 and 50}s were made in order to study the La diffusion and reaction mechanisms in the stack.

The different samples were analyzed by time-of-flight secondary ion mass spectrometry (ToF-SIMS) using a 0.5 keV 45°tilted O<sub>2</sub> beam and La<sup>+</sup>, HfO<sup>+</sup>, Si<sup>+</sup> and Ti<sup>+</sup> positively charged species signals versus depth were detected. La intensity quantification was carried using a reference sample analysed by APT as in [43]. Knowing that etch rates during ToF-SIMS measurements are different for the stack's different materials, a depth calibration based on the process thickness was made for the thick HfSiON 15 nm layer of series (i). Other materials thickness may have slight inaccuracies, however this does not impact La diffusion evaluation in HfSiON high-k. From another side, series (ii) samples with a thin high-k of 2.5 nm on a thicker IL of 20 nm, SIMS results interpretation is more difficult. In this case, LaSiO lanthanum silicates formation after anneal may be important due to the proximity of the high-k/IL interface from the La<sub>2</sub>O<sub>3</sub> capping layer forming a thin LaSiO layer and complicating La depth and concentration calibration. Moreover, following the HfSiON thin layer etch by the SIMS beam, it was observed that a part of the Hf atoms form a metallic aggregate at the HfSiON/SiO<sub>2</sub> interface, causing a lower etch rate of the SiO<sub>2</sub> material and consequently leading to a more difficult SIMS calibration and interpretation for series (ii) samples.



Table 3.5: Deposit and anneal details of the samples designed in order to study La diffusion in TiN/La<sub>2</sub>O<sub>3</sub>/HfSiON/SiO<sub>2</sub>/Si high-k stacks.

Samples	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SiO <sub>2</sub> layer (10 nm)	x	x	x	x	x	x	x	x								
SiO <sub>2</sub> layer (20 nm)									x	x	x	x	x	x	x	x
HfSiON layer (15 nm)	x	x	x	x	x	x	x	x								
HfSiON layer (2.5 nm)									x	x	x	x	x	x	x	x
La <sub>2</sub> O <sub>3</sub> layer (1 nm)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
TiN layer (6.5 nm)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
poly-Si layer (20 nm)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
No Anneal	x								x							
1000°C - 50 s		x								x						
1040°C - 10 s			x								x					
1040°C - 30 s				x								x				
1040°C - 50 s					x								x			
1080°C - 10 s						x								x		
1080°C - 30 s							x								x	
1080°C - 50 s								x								x

Series (i) thick high-k/thick IL samples were first analysed by SIMS. Corresponding results for La<sup>+</sup>, Ti<sup>+</sup> and HfO<sup>+</sup> clusters intensities versus depth for the as-deposited sample are given in Fig. 3.10. In the intensities versus depth profiles of Fig. 3.10, the 0 position on x-axis corresponds to the silicon surface on which the different layers are deposited. We can clearly distinguish the positions and thicknesses of the different layers of the high-k stack. The different species profiles are slightly spread in neighbouring layers, which is due to SIMS resolution artefacts at the different interfaces. The real intensity profiles are closer to rectangular ones with constant concentrations.

The annealed La SIMS profiles are shown in Fig. 3.11. Isochronal anneals (50 s) between 1000°C and 1080°C shown in Fig. 3.11a indicate that La diffusion increases in the temperature range under consideration, suggesting a thermally activated La diffusion mechanism. Previous literature results [39, 44] showed that La diffusion in the high-k is source limited depending on the concentration of La in the La<sub>2</sub>O<sub>3</sub> capping layer. Indeed, this effect was observed in our samples where we noticed a slight decrease (not shown here) in La concentration in the La<sub>2</sub>O<sub>3</sub> capping layer following the thermal anneals. However in addition to this La<sub>2</sub>O<sub>3</sub> source effect and according to La annealed profiles in our experiments, the thermally activated La transport in the high-k cannot be ignored. From another side, isothermal anneals at 1040°C and 1080°C are shown in Fig. 3.11b. For both temperatures, we observe in Fig. 3.11b that La diffusion exhibits a transient behaviour and stops after approximately 30 s. This La diffusion saturation with time in this case is due to a chemical reaction kinetic effect. Indeed, as mentioned above, La reacts with SiO bonds at the high-k/IL interface forming lanthanum silicates LaSiO in a stable phase, probably stopping La diffusion and explaining the overlapping of 30 and 50 s curves in Fig. 3.11b. Therefore, in the frame of SIMS results of Fig. 3.11a and 3.11b, two mechanisms both in agreement with literature results [38–40] are identified:

- A diffusion mechanism of La atoms that is thermally activated.
- A kinetic reaction mechanism explaining the diffusion saturation versus time due to LaSiO silicates formation at the high-k/IL interface.

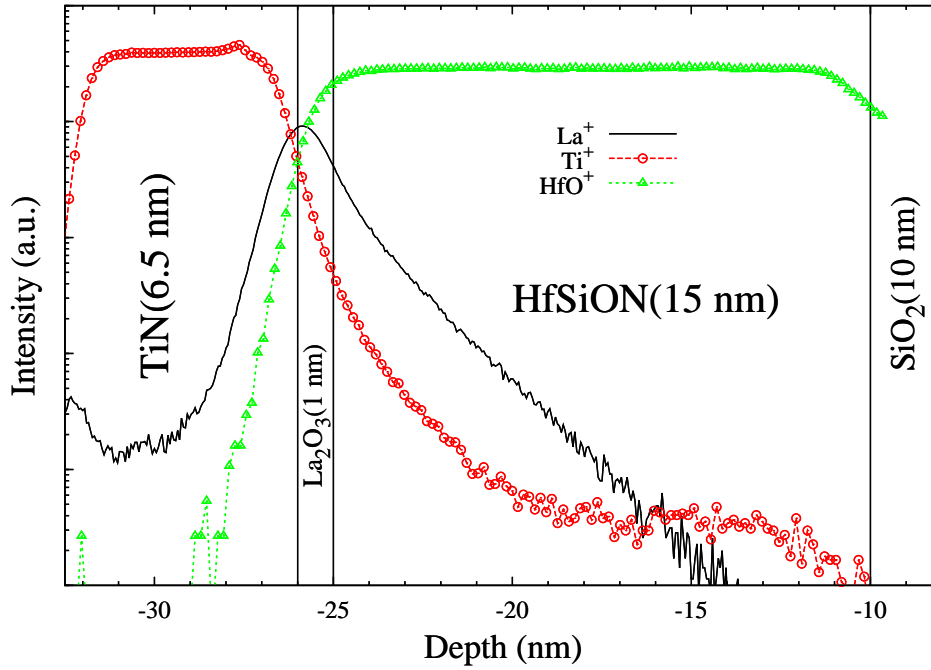


Figure 3.10: SIMS profiles for  $\text{La}^+$ ,  $\text{Ti}^+$  and  $\text{HfO}^+$  in the as-deposited (non annealed) sample of table 3.5 for the  $\text{HfSiON}(15 \text{ nm})/\text{SiO}_2(10 \text{ nm})$  stack.

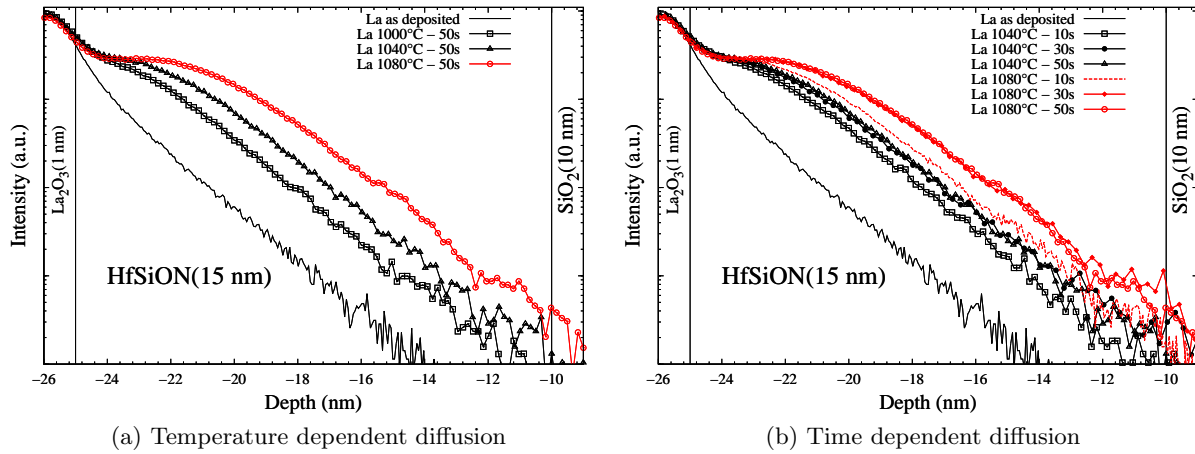


Figure 3.11: La SIMS profiles for thermal anneals at (a) 1000, 1040 and 1080°C during 50 s where we can see that the La diffusion in  $\text{HfSiON}$  is thermally activated and (b) 1040 and 1080°C during 10, 30 and 50 s for each temperature where La diffusion saturation versus time is observed.

Thin high-k/thicker IL samples of series (ii) (table 3.5) were also analysed. Figure 3.12 shows that La diffuses after thermal anneals in the HfSiON material compared to the as deposited sample. However as explained previously, SIMS resolution limits on these thin high-k/thick IL samples were not resolved. Given that uncertainties on the positions and depths of the different materials in the stack persisted, no further modelling of these data in sub-section 3.3.3 was possible. In addition, in series (ii) samples, given the thickness of the HfSiON (2.5 nm) and the proximity of the high-k/IL interface from the  $\text{La}_2\text{O}_3$  capping layer, the La diffusion saturation takes place probably faster forming a thin LaSiO layer between the high-k and the IL, even after 10 s of anneal.

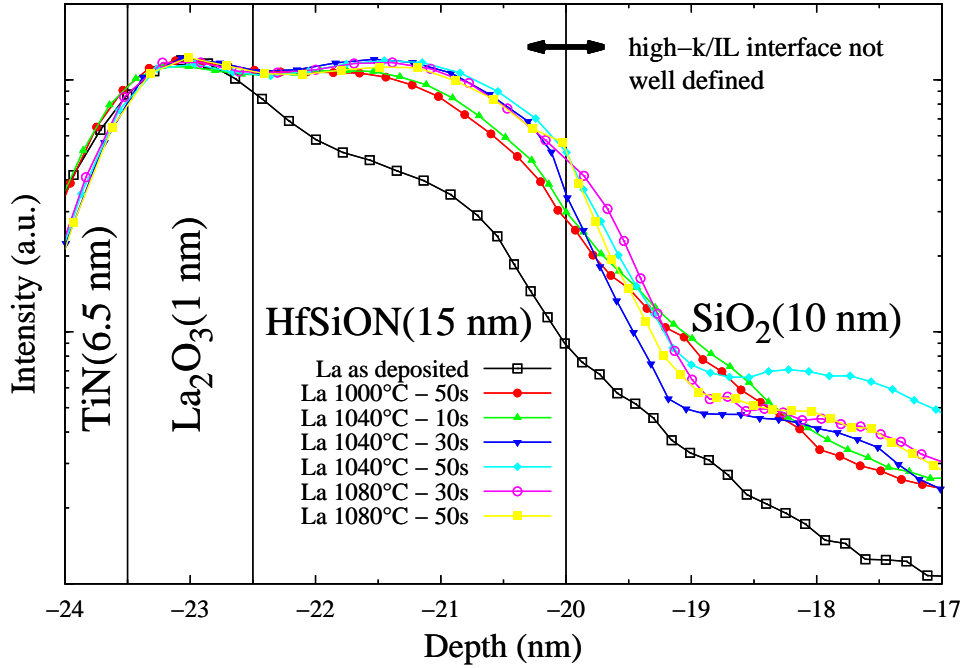


Figure 3.12: La SIMS profiles for series (ii) samples (table 3.5) with a thin HfSiON (2.5 nm) high-k and a thick  $\text{SiO}_2$  (20 nm) IL.

Given SIMS results of this section and profiles uncertainties for series (ii) samples (table 3.5), next sub-section 3.3.3 on lanthanum diffusion modelling in TiN/ $\text{La}_2\text{O}_3$ /HfSiON/ $\text{SiO}_2$ /Si high-k stacks will focus on series (i) samples with a 15 nm thick HfSiON high-k layer.

### 3.3.3 Lanthanum diffusion modelling in high-k stacks

In the following, we will concentrate on the evaluation and modelling of La diffusion in the thick high-k/ thick IL series (i) samples in order to get a better understanding of the La diffusion in the TiN/ $\text{La}_2\text{O}_3$ /HfSiON/ $\text{SiO}_2$ /Si stack. In sub-section 3.3.2, we assumed that the La diffused profiles can be explained by two mechanisms: a thermally activated diffusion mechanism allowing the La atoms to reach the high-k/IL interface and a kinetic reaction mechanism due to LaSiO dipoles formation at the high-k/IL interface that blocks the diffusion mechanism and explains diffusion saturation versus time of anneal observed in Fig. 3.11b. The simulations to be carried in this sub-section will allow us to check the validity of these assumptions. The TCAD diffusion model developed here was implemented in SProcess using the scripting language Alagator [24] used to define the species and their different related equations in the HfSiON material and at the  $\text{La}_2\text{O}_3$ /HfSiON interface. Fig. 3.13 is a synthetic diagram not to scale of the different materials and interfaces in the stack with their related equations.

Our model mainly deals with La diffusion in the HfSiON material and therefore the La diffusion

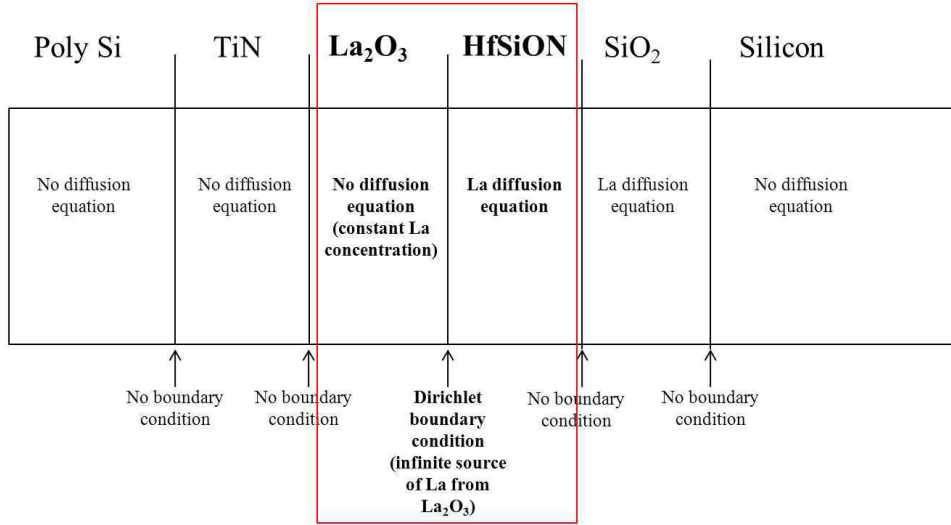


Figure 3.13: Diagram of the different materials and interfaces in the TiN/La<sub>2</sub>O<sub>3</sub>/HfSiON/SiO<sub>2</sub>/Si stack and their related equations.

equation is considered only in this material. We already noticed from SIMS results in 3.3.2 that La concentration in the 1 nm La<sub>2</sub>O<sub>3</sub> layer is almost unaltered after the different thermal anneals. Therefore, a Dirichlet boundary condition [45] is considered at the La<sub>2</sub>O<sub>3</sub>/HfSiON interface, according to which the La<sub>2</sub>O<sub>3</sub> layer is an infinite source emitting La in the HfSiON high-k. A constant La concentration is considered in the La<sub>2</sub>O<sub>3</sub> layer, adjusted to the one measured by SIMS at the La<sub>2</sub>O<sub>3</sub>/HfSiON for the as-deposited sample. Considering La diffusion in the high-k, the simplest diffusion equation that can be used is Fick's second law [15] described by:

$$\frac{\partial \text{La}}{\partial t} = D \frac{\partial^2 \text{La}}{\partial x^2} \quad (3.24)$$

where La is the concentration of lanthanum in cm<sup>-3</sup> and D is the La diffusivity in cm<sup>2</sup>.s<sup>-1</sup>. It should be noticed that equation 3.24 assumes an isotropic diffusion which is quite simplistic and implies that the high-k is amorphous. However, it has already been shown [46] that for thick high-k layers, some partial crystallisation may take place after the thermal anneal leading to the formation of crystalline regions within the amorphous high-k layer. In this case, La diffusion can be monitored by different complexes, clusters and grain boundaries formed during the thermal anneal and consequently leading to an anisotropic diffusivity. Therefore, if this partial crystallisation is confirmed, the diffusivity D in equation 3.24 has to be considered as an effective diffusivity in our one dimensional structures.

Fig. 3.14 shows the TCAD simulation results using equation 3.24 for samples annealed at 1040°C for 10, 30 and 50 s, with D fixed at  $6 \times 10^{-15}$  cm<sup>2</sup>.s<sup>-1</sup>. As expected when using Fick's second law of equation 3.24, the longer the anneal time, the more La diffuses. These simulations results are not in agreement with SIMS experimental results of Fig. 3.11b indicating La diffusion saturation versus time of anneal.

La reaction from the La<sub>2</sub>O<sub>3</sub> capping layer with SiO bonds from the HfSiON high-k and the SiO<sub>2</sub> IL discussed previously are quite complex and related to the La<sub>2</sub>O<sub>3</sub>.SiO<sub>2</sub> binary system [47]. Therefore, we simplify the different chemical reactions described in [47] and leading to the LaSiO formation at the high-k/IL interface using the following reaction:



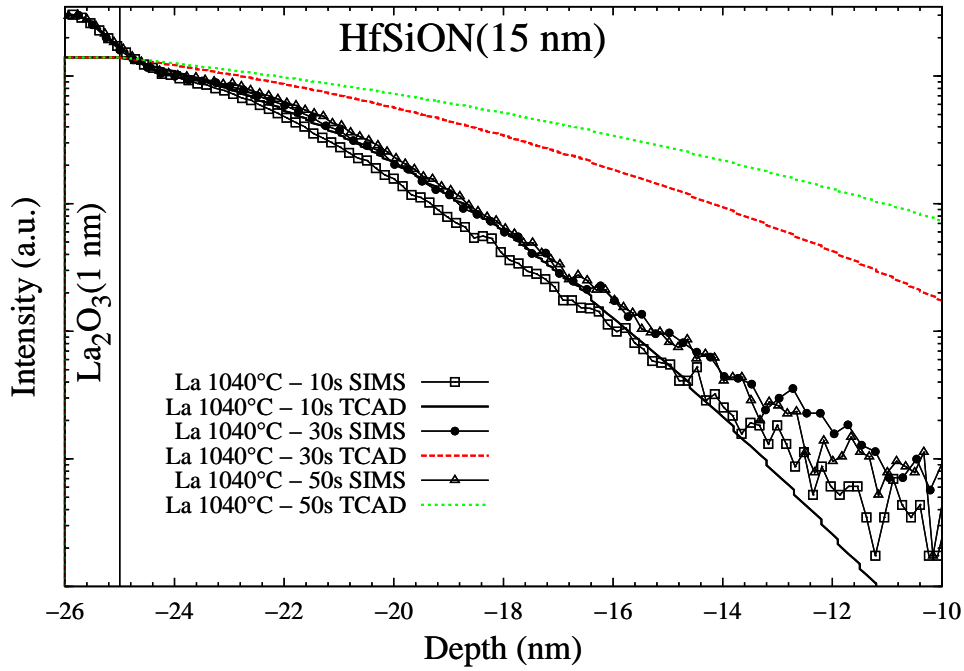


Figure 3.14: La SIMS versus TCAD profiles for thermal anneal at 1040°C during 10, 30 and 50 s, using equation 3.24 where La diffusion saturation versus time of anneal is not reproduced.

where  $k_f$  is the forward LaSiO formation reaction constant. Reaction 3.25 is used to limit the diffusion of La in the HfSiON and in order to further simplify our model, we consider that the reaction takes place in all the material and not only at the high-k/IL interface. Knowing that a Dirichlet boundary condition was considered at the  $\text{La}_2\text{O}_3/\text{HfSiON}$  interface, the  $\text{La}_2\text{O}_3$  is an infinite source of La and consequently La is not a limiting factor for reaction 3.25. Consequently, SiO bonds follow the first order differential equation:

$$\frac{d\text{SiO}}{dt} = k_f \text{SiO} \quad (3.26)$$

whose analytical solution is  $\text{SiO}(t) = \text{SiO}(t=0) \cdot e^{-k_f t}$ , where  $\text{SiO}(t=0)$  is the concentration of SiO bonds at the beginning of the anneal. Thus, defining  $S(t)$  as the unitless function:

$$S(t) = \frac{\text{SiO}(t)}{\text{SiO}(t=0)} = e^{-k_f t} \quad (3.27)$$

one can reproduce the diffusion saturation versus time taking into account reaction 3.25 by modifying La Fick's second law diffusion equation 3.24:

$$\frac{\partial \text{La}}{\partial t} = D S(t) \frac{\partial^2 \text{La}}{\partial x^2} \quad (3.28)$$

From equation 3.27, we should notice that  $S(t=0) = 1$  and  $S(t) \xrightarrow[t \rightarrow \infty]{} 0$  and thus the effective diffusivity  $D \cdot S(t)$  will tend towards 0 versus time, which will block the diffusion mechanism and will reproduce the diffusion saturation versus time. The La diffusion model represented by equations 3.26 to 3.28 was therefore calibrated thanks to the different SIMS data of Fig. 3.11 and the best agreement was obtained with  $D$  fixed at  $1.25 \times 10^{-10} e^{-\frac{1.04(\text{eV})}{k_B T}} \text{ cm}^2 \cdot \text{s}^{-1}$  and  $k_f$  at  $0.15 \text{ s}^{-1}$ . The results of the corresponding TCAD simulations are shown in Fig. 3.15. It can be seen from Fig. 3.15a that equation 3.28 allows a correct modelling of the diffusion saturation versus time at 1040°C. In addition, diffusion saturation versus time at 1080°C (not shown here) was also correctly modelled, validating

our assumption on the kinetic effect in La diffusion due to the formation of LaSiO bonds. On the other side, the diffusivity  $D$  follows an Arrhenius law versus temperature, and the thermally activated diffusion mechanism discussed earlier is also verified. The thermally activated diffusion mechanism in Fig. 3.15b is correctly captured by TCAD in comparison to SIMS measurements and mainly in the tails of the La diffused profiles. However, a less good agreement between SIMS and TCAD was observed near the  $\text{La}_2\text{O}_3/\text{HfSiON}$  interface.

Indeed, we can observe that near the  $\text{La}_2\text{O}_3/\text{HfSiON}$  interface, where the La concentration is high, La diffusion is stronger than far from the interface where La concentration is lower. In addition, we can observe that La diffusivity for high La concentration increases with temperature. Therefore, in order to reproduce this effect, the following improved La diffusion equation was used:

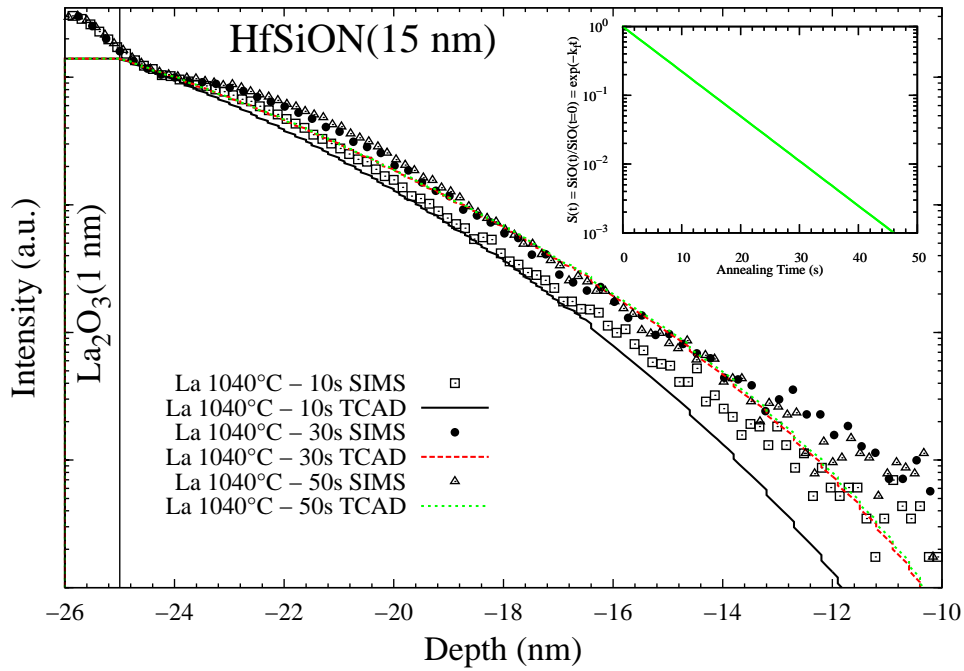
$$\frac{\partial \text{La}}{\partial t} = D \left( S(t) + \frac{\text{La}}{\text{La}_0} \right) \frac{\partial^2 \text{La}}{\partial x^2} \quad (3.29)$$

with  $S(t)$  already defined in equation 3.27 and  $\text{La}_0$  a fitting parameter. Equation 3.29 parameters have been also calibrated using the SIMS data:  $k_f$  kept the same value  $0.15 \text{ s}^{-1}$ ,  $D$  has been slightly changed to  $1.2 \times 10^{-10} \text{ e}^{-\frac{1.04(\text{eV})}{k_B T}} \text{ cm}^2 \cdot \text{s}^{-1}$  and the  $\text{La}_0$  fitting parameter has been fixed at  $1.91 \times 10^{12} \text{ e}^{-\frac{2.92(\text{eV})}{k_B T}} \text{ cm}^{-3}$ . Corresponding TCAD simulations results are shown in Fig. 3.16. Fig. 3.16a shows that the La diffusion saturation effect is again correctly modelled using equation 3.29 for  $1040^\circ\text{C}$  (not shown here) and  $1080^\circ\text{C}$  as we have already seen in Fig. 3.15a using equation 3.28. The La thermally activated diffusion mechanism is correctly modelled in the tail of the profiles, but also near the  $\text{La}_2\text{O}_3/\text{HfSiON}$  interface thanks to the  $\text{La}/\text{La}_0$  term enhancing the La diffusion in the high La concentration region and at high temperatures. Therefore, from Fig. 3.16b, a very good agreement between experimental and simulated results is observed. The three versions of our diffusion model presented respectively using equations 3.24, 3.28 and 3.29 with their related calibrated parameters are summarized in table 3.6.

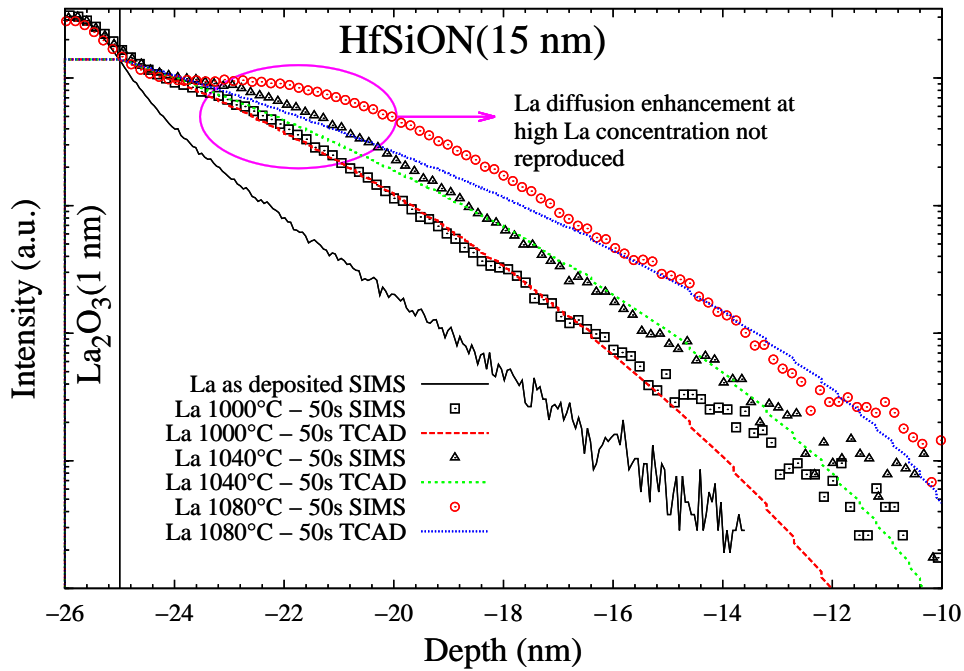
Table 3.6: Summary of the different models used in this work, and their related parameters and characteristics.

Model	Parameters	Characteristics
$\frac{\partial \text{La}}{\partial t} = D \frac{\partial^2 \text{La}}{\partial x^2}$ (equation 3.24)	$D = 6 \times 10^{-15} \text{ cm}^2 \cdot \text{s}^{-1}$ (at $1040^\circ\text{C}$ )	Fick's 2 <sup>nd</sup> law, no diffusion saturation.
$\frac{\partial \text{La}}{\partial t} = D \text{e}^{-k_f t} \frac{\partial^2 \text{La}}{\partial x^2}$ (equation 3.28)	$D = 1.25 \times 10^{-10} \text{ e}^{-\frac{1.04(\text{eV})}{k_B T}} \text{ cm}^2 \cdot \text{s}^{-1}$ $k_f = 0.15 \text{ s}^{-1}$	Improved Fick's 2 <sup>nd</sup> law, correct diffusion saturation vs. time and thermally activated diffusion.
$\frac{\partial \text{La}}{\partial t} = D \left( \text{e}^{-k_f t} + \frac{\text{La}}{\text{La}_0} \right) \frac{\partial^2 \text{La}}{\partial x^2}$ (equation 3.29)	$D = 1.2 \times 10^{-10} \text{ e}^{-\frac{1.04(\text{eV})}{k_B T}} \text{ cm}^2 \cdot \text{s}^{-1}$ $k_f = 0.15 \text{ s}^{-1}$ $\text{La}_0 = 1.91 \times 10^{12} \text{ e}^{-\frac{2.92(\text{eV})}{k_B T}} \text{ cm}^{-3}$	Improved Fick's 2 <sup>nd</sup> law, correct diffusion saturation vs. time, thermally activated diffusion and La diffusion enhancement at high La concentration.

The La diffusion model in HfSiON high-k described in [32] and summarized by equation 3.29 gives very good agreement with experimental SIMS data. Several comments given in [48] can be drawn considering these experimental and simulation results. First of all, it should be noticed that the La



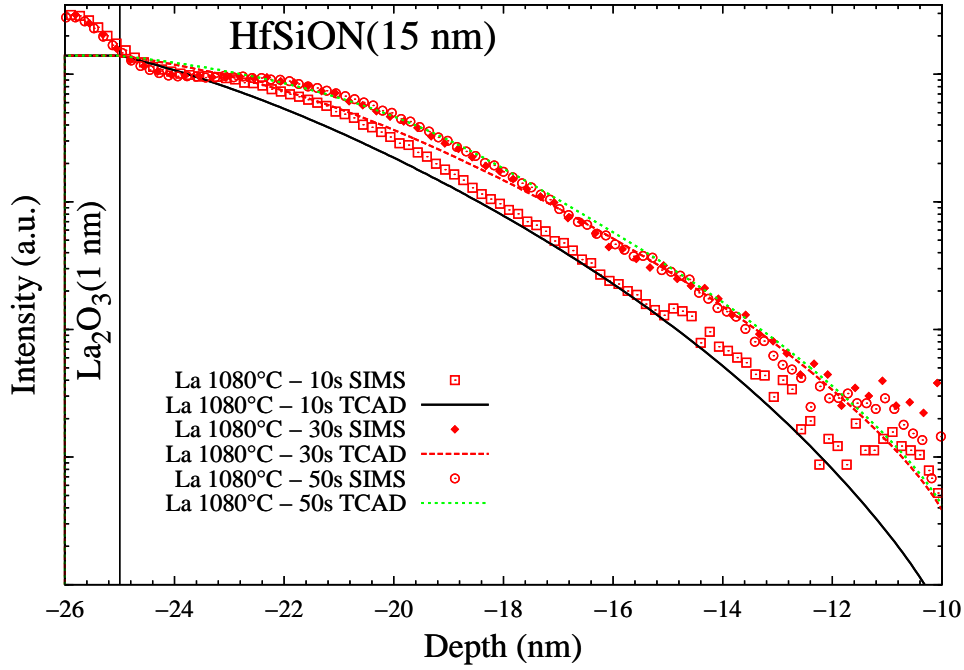
(a) Temperature dependent diffusion



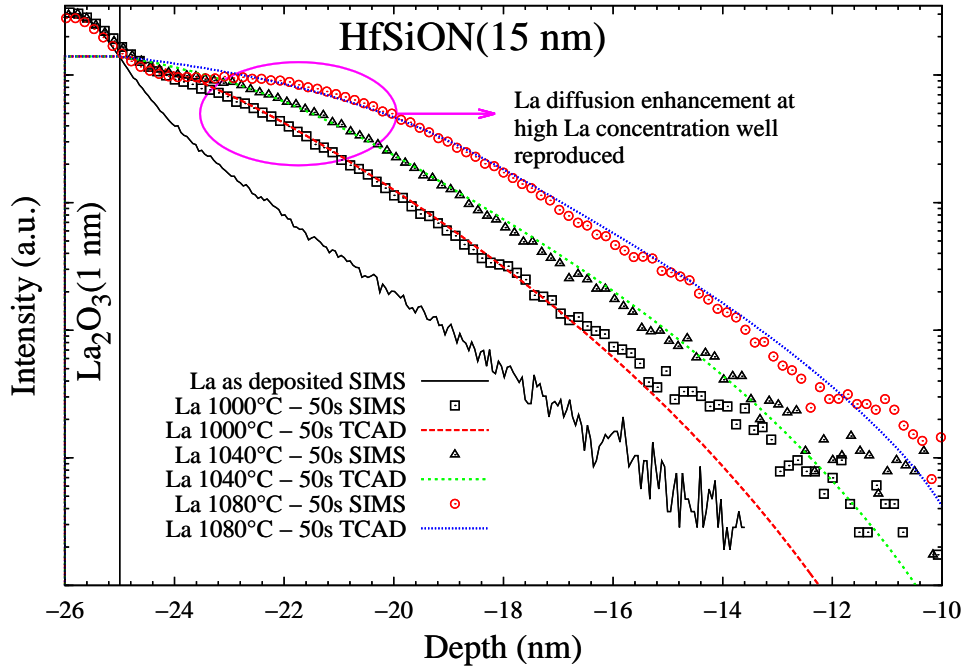
(b) Time dependent diffusion

Figure 3.15: La SIMS versus TCAD profiles for thermal anneals at (a) 1040°C during 10, 30 and 50 s using equation 3.28 where La diffusion saturation is correctly reproduced and (b) at 1000, 1040 and 1080°C during 50 s using equation 3.28 where La thermally activated diffusion is correctly reproduced, except near the La<sub>2</sub>O<sub>3</sub>/HfSiON interface with a high La concentration.





(a) Temperature dependent diffusion



(b) Time dependent diffusion

Figure 3.16: La SIMS versus TCAD profiles for thermal anneals at (a) 1040°C during 10, 30 and 50 s using equation 3.29 where La diffusion saturation is correctly reproduced and (b) at 1000, 1040 and 1080°C during 50 s using equation 3.29 where La thermally activated diffusion is correctly reproduced, including near the  $\text{La}_2\text{O}_3/\text{HfSiON}$  interface with a high La concentration.

diffusion model calibration is based on a limited set of data with a thick HfSiON layer. Indeed, different additional effects may intervene for other hafnium oxide based high-k layers :

- For thin high-k layers ( $\leq 2.5$  nm), such as the ones used in series (ii) samples of table 3.5, a predominance of the reaction mechanism and the formation of a lanthanum silicates LaSiO layer between the high-k and the IL may be observed. Therefore, the La diffusion model shown here for thick high-k should be supplemented by a growth reaction model as in [49] for the formation of LaSiO layer at the high-k/IL interface. Indeed, from SIMS profiles of series (ii) samples of table 3.5 with a thinner 2.5 nm HfSiON high-k, very small differences in La annealed profiles were observed probably due to the formation of a lanthanum silicates layer with constant La concentration.
- Thin high-k layers may have different crystallinity from the thick layers used in series (i) with a possible impact on La diffusion depending on the crystalline state of the high-k.
- For thin layers, the electrical potential difference between silicon and TiN metal gate may be very important causing a drift diffusion mechanism of La charged species, requiring a drift-diffusion equation for La.
- Different stoichiometry and chemistry in the high-k such as the presence of nitrogen in the hafnium oxide high-k may change diffusion mechanism.

The calibration performed here used a small temperature range between 1000 and 1080°C, and one could expect that the model covers only this limited temperature range. However, for low temperature anneals, La profiles at 700 and 800°C (not shown here) gave almost no diffusion and were below SIMS resolution limits. For higher temperature anneals, such as the ones used in flash or  $\mu$ s sub-melt laser anneals, an accuracy identical to the one shown in Fig. 3.16b is expected. Considering the parameter  $k_f$  for lanthanum silicates reaction 3.25, no temperature dependence was observed. However, for a larger temperature range, a temperature dependence would be expected in order to avoid that  $S(t)$  function vanishes quickly at room temperature or during a typical RTA ramp-up anneal including some hold times at low temperature.

As discussed in 3.3.1, lanthanum diffusion in the high-k is expected to impact  $V_t$  shifts in nMOS transistors. Within ATEMOS project [1, 48], Hackenberg et al. [50] investigated this correlation between La diffusion and  $V_t$  shifts in nMOS capacitance using the same gate stack as the one used in series (i) samples of table 3.5 with different thermal anneals. In these results, no linear correlation was observed between  $V_t$  values and La concentration at the high-k/IL interface. From literature results [37, 41, 42], a linear dependence between the  $V_t$  shift and the La atoms creating electrical dipoles at the high-k/IL interface is observed. Therefore, in these experiments, the  $V_t$  shift cannot be explained by La induced dipoles formation at the high-k/IL interface. However when drawing the  $V_t$  as a function of the total density of La in the high-k layer, a linear correlation was observed by Hackenberg et al. [50]. Therefore, the corresponding  $V_t$  shifts in these annealed high-k samples may have two origins discussed in [48, 50]:

- La atoms form simple fixed charges inside the HfSiON bulk material causing the observed  $V_t$  shifts after thermal anneals.
- La atoms form simple electrical dipoles inside the HfSiON bulk material with a non-random dipoles orientation possibly due to the La concentration gradient or to the electric field across the gate stack leading to the formation of electrical dipoles in a preferential direction.

In the frame of these explanations, additional material analysis such as the one carried out in [40] and additional  $V_t$  shifts measurements for different HfSiON and SiO<sub>2</sub> IL thicknesses are mandatory

for a more complete understanding of the  $V_t$  shift mechanism. Once this mechanism understood, the one dimensional La diffusion model of equation 3.29 can be easily extended to 2D and 3D and coupled with a device dipole model in order to predict  $V_t$  shifts in technology relevant nMOS transistors.

### 3.4 Conclusion

In the frame of ATEMox project, two main chemical species diffusion in multi-materials stacks were investigated experimentally and using TCAD modelling:

- Boron out-diffusion in nitride/oxide/silicon stacks and corresponding boron dose in silicon investigated in section 3.2.
- Lanthanum diffusion in advanced high-k stacks of nMOS transistors and corresponding threshold voltage  $V_t$  shifts presented in section 3.3

In the first section 3.2, boron dose loss modelling in nitride/oxide/silicon stacks following thermal anneals is due to a boron out-diffusion mechanism from silicon to oxide related to boron diffusivity increase in oxide depending on hydrogen related species content and mainly OH bonds. Using SIMS measurements of a 1 keV  $5.10^{14} \text{ cm}^{-2}$   $\text{BF}_2$  implant annealed at  $1000^\circ\text{C}$  during 2 min, in addition to coupled TDS/stress and FTIR measurements, hydrogen related species characteristics were extracted in both oxide and nitride for four different nitride/oxide/silicon stacks. Using these physical characteristics, a first version of a boron TCAD diffusion model in oxide was developed. The first version of this model uses a linear dependence with OH bonds of the boron diffusivity in oxide. Boron diffused profiles in silicon and corresponding dose loss were correctly reproduced using this model. However, in order to reproduce the exponential-shaped boron diffused profiles in oxide, the simple Fick's law based boron diffusion model in oxide was extended to a long hop mechanism with two mobile and immobile boron species. This improved model also allowed to reproduce nitride capping effect for hydrogen, already observed experimentally in literature. The impact of boron out-diffusion on the temporal evolution of the sheet resistance of the silicon boron doped layer in the different stacks was monitored, showing a clear impact of boron dose loss on this electrical characteristic. Therefore boron dose loss is expected to have an impact on electrical performances of MOS transistors and CMOS image sensors as it will be seen in chapter 4.

In the second section 3.3 of this chapter, dealing with lanthanum diffusion in advanced high-k stacks, dedicated  $\text{TiN}/\text{La}_2\text{O}_3/\text{HfSiON}/\text{SiO}_2/\text{Si}$  high-k structures used in nMOS transistors were designed and processed at high temperature anneals. La diffusion in the  $\text{HfSiON}$  high-k is followed by the formation of  $\text{LaSiO}$  dipoles at the  $\text{HfSiON}/\text{SiO}_2$  interface explaining negative  $V_t$  shifts in advanced nMOS transistors. In our study, SIMS profiles on high-k stacks with thick high-k and IL, annealed at different temperatures and times were made in order to evaluate La diffusion in the different materials of the stacks. Thanks to the thick high-k/thick IL SIMS data, we observed two mechanisms explaining the La diffused profiles: a thermally activated diffusion mechanism leading to the migration of La from the  $\text{La}_2\text{O}_3$  capping layer to  $\text{HfSiON}/\text{SiO}_2$  interface and a kinetic reaction mechanism due to the  $\text{LaSiO}$  dipoles formation at this interface and explaining the La diffusion saturation versus time. Using SIMS results, a La TCAD diffusion model was developed and allowed to confirm and reproduce successfully these two mechanisms. In the frame of ATEMox project, additional data [50] showed that  $V_t$  shifts in nMOS capacitors with the same high-k schemes, correlate with the total content of La in the high-k. Therefore, several assumptions [48, 50] may explain this effect and further experimental investigations are still needed in order to confirm or infirm these assumptions.

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## Chapter 4

# TCAD modelling of advanced CMOS devices

### 4.1 Introduction

In previous chapters 2 and 3, we presented the different TCAD process models developed during the PhD. Chapter 2 dealt with implantation induced defects and their impact on dopant diffusion and activation, focusing on PIII technique modelling for  $\text{BF}_3$  with its main characteristics (shallowness and conformality). High doping conditions used in PIII generate large BICs modifying boron diffusion and electrical activation. Large BICs evolution during thermal annealing was thus evaluated thanks to dedicated beam-line experiments correlated to TEM, APT and SIMS data, and led to the development of a continuum large BICs model. Chapter 3 was dedicated to chemical species diffusion in multi-materials stacks and in particular to the development of a boron dose loss model in nitride/oxide/silicon stacks and lanthanum diffusion in high-k stacks. In this chapter, these models will be tested on real advanced device structures used in CMOS technologies. The models consequences on advanced devices electrical features will also be evaluated.

In section 4.2, advanced MOS transistors with different miniaturization schemes will be evaluated using process and device simulations. pMOS transistors of 45 and 28 nm bulk technology nodes will be modelled in 4.2.1 mainly focusing on boron dose loss in spacer materials. Boron high doping and induced precipitation mechanisms will be evaluated in 4.2.2 on p-type fully depleted SOI (FDSOI) MOS transistors, using using different implantation conditions. PIII conformality effects will be tested for TriGate n-MOS transistors where  $\text{AsH}_3$  (n-type doping) is used for extensions implants and compared to classical arsenic multi-tilt beam-line implants.

Section 4.3 deals with the modelling of FSI CMOS image sensors with  $1.4\mu\text{m}$  pitch pixels, including the evaluation of boron dose loss close to the TG of CMOS image sensors in 4.3.1 and the use of PIII in the DTIs of FSI CMOS image sensors in 4.3.2.

In section 4.4, BSI CMOS image sensors with  $2\mu\text{m}$  pitch pixels will be modelled. In these simulations, we will focus on diffusion mechanisms occurring in the backside ONO stack of the sensors, and their corresponding effects on electrical characteristics. Simulations include boron dose loss modelling at the backside 4.4.1 and the evaluation of LTA also used for backside boron doping in 4.4.2.

Lanthanum diffusion effect on nMOS transistor electrical characteristics will not be investigated in this chapter due to a lack of a complete set of experimental data for thin high-k layers used in advanced MOS transistors technology.

## 4.2 MOS transistors modelling

### 4.2.1 Boron dose loss in advanced bulk pMOS transistors

As already discussed in 3.2, boron dose loss in nitride/oxide/silicon stacks was first observed in spacer materials of pMOS transistors. In order to evaluate boron dose loss effect on the electrical characteristics of pMOS transistors, the boron dose loss model presented in 3.2 was used for 2D process simulations of bulk pMOS transistor. Two different technology nodes manufactured at STMicroelectronics with two respective nominal gate lengths of 45 and 28 nm, were therefore investigated. The 2D process simulations [1] of 45 and 28 nm gate length pMOS transistors with their corresponding doping profiles after a 1000°C spike anneal are represented respectively in Fig. 4.1a and 4.1b. The LDD region where boron out-diffusion is expected to occur is white framed. Some differences exist between the two technology nodes. The main one is a higher distance and lower interaction between the boron-doped LDD region and the spacer for the 45 nm technology node transistor (Fig. 4.1a) when compared to the 28 nm transistor (Fig. 4.1b). We can also notice the integration of a metal gate and a high-k dielectric in the gate stack of the 28 nm transistor (Fig. 4.1b), whereas the 45 nm transistor exhibits a classical p-type doped polycrystalline silicon gate (Fig. 4.1a). However, the high-k/metal gate stack used here has no influence on the boron dose loss mechanisms.

Simulations with and without boron dose loss model were carried using an  $S'_1$  like spacer stack and its corresponding OA oxide and NA nitride (table 3.1). The results obtained with the boron dose loss model included, are shown in Fig. 4.1c (boron), 4.1d (free H) and 4.1e (OH bonds).

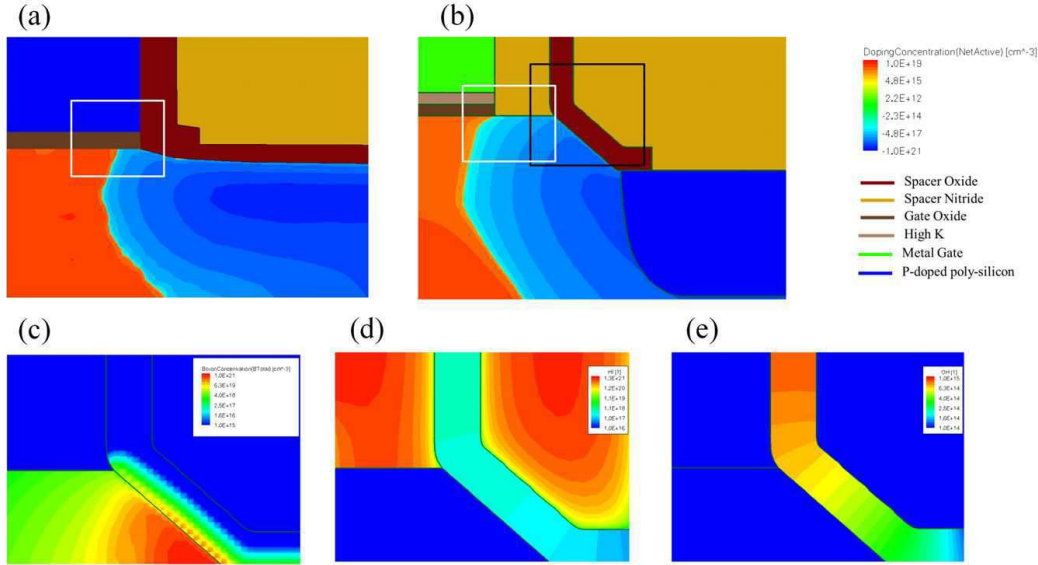


Figure 4.1: 2D process simulations after a 1000°C spike anneal with a  $S'_1$  (table 3.1) sample based spacer stack of (a) 45 nm and (b) 28 nm technology node pMOS transistor with the corresponding doping profiles in silicon. The boron doped LDD region is white framed. The 2D concentration profiles of boron, free hydrogen and OH bonds contained in the black framed region of the 28 nm transistor (b) are shown in (c), (d) and (e), respectively.

The 2D doping profiles were injected in the device simulator SDevice [2] in order to study the impact of boron out-diffusion on the electrical characteristics of the pMOS transistors with gate lengths  $L_g$  between the nominal length and 1  $\mu\text{m}$ . The following electrical parameters extracted from  $I_d(V_g)$  characteristics were investigated as a function of the transistor gate length [3]:  $\Delta V_{t,lin}$  and  $\Delta V_{t,sat}$  respectively in linear and saturation regimes (equation 1.13) with a reference long transistor with  $L_g = 1\mu\text{m}$ , DIBL ( $L_g$ ) (equation 1.12) and On current in saturation regime  $I_{on,sat}(L_g)$ . The results are

presented respectively in Fig. 4.2. From these characteristics, boron dose loss effect is quite noticeable mainly for short gate lengths in both 45 and 28 nm technology nodes. In the 45nm case, typical roll up-roll down effect is observed for  $\Delta V_{t,lin}(L_g)$  and  $\Delta V_{t,sat}(L_g)$  characteristics (Fig. 4.2a and 4.2b) due to  $n^+$  pocket implants used below the LDD region. For the 28 nm, dose loss effect is more important on  $\Delta V_{t,lin}(L_g)$  and  $\Delta V_{t,sat}(L_g)$  characteristics due to the higher interaction between boron in the LDD region and the spacer stack. From DIBL( $L_g$ ) characteristics in Fig. 4.2c, we can observe that boron dose loss reduces SCE due to shallower LDD junctions with a much more noticeable effect in the 28 nm case than in the 45 nm one. This can be explained by the higher spacer-LDD region interaction in the 28 nm case. However, when modelling boron dose loss, we can observe from Fig. 4.2d that lower on currents in the saturation regime  $I_{on,sat}$  are observed for short transistors lengths. In figure 3.9, it was observed that  $R_s$  increases with the dose loss due to a lower available active boron after the anneal and a shallower junction. Thus knowing that  $I_{on,sat}$  varies inversely with the LDD extension sheet resistance  $R_s$ , lower  $I_{on,sat}$  values are obtained when boron dose loss is included.

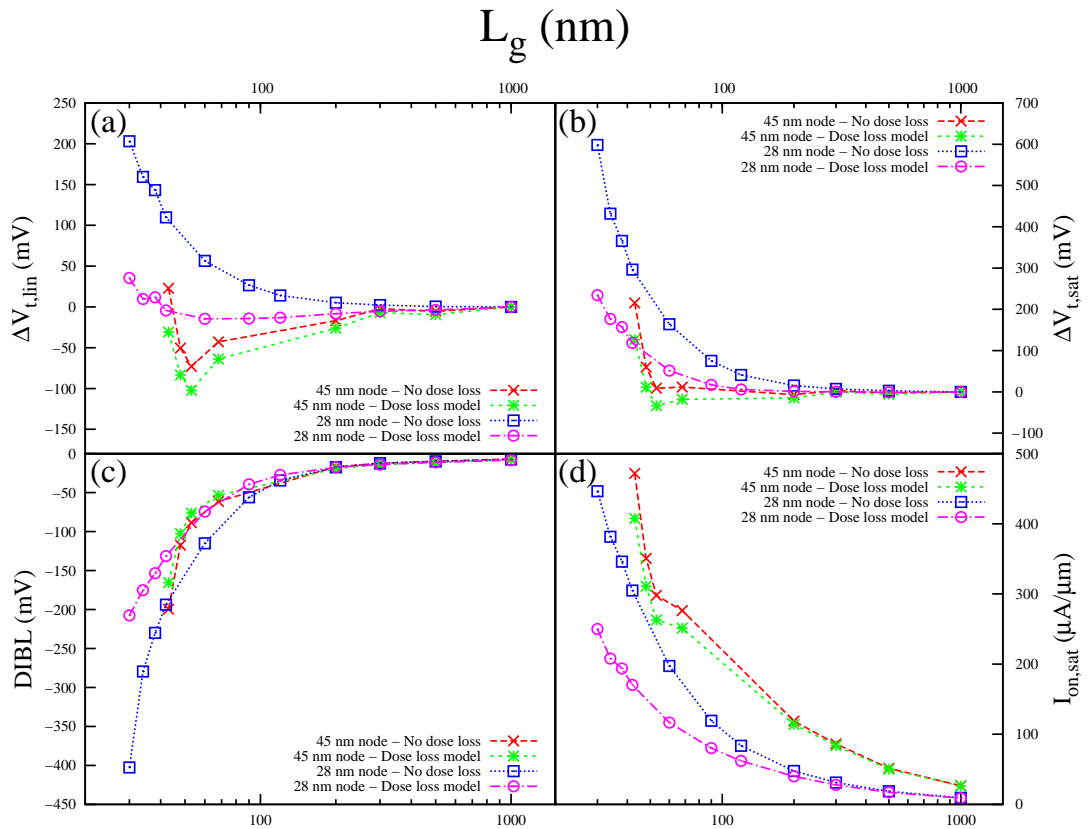


Figure 4.2: 45 nm and 28 nm technology node pMOS transistors electrical characteristics versus gate length including (a)  $\Delta V_{t,lin}(L_g)$ , (b)  $\Delta V_{t,sat}(L_g)$ , (c) DIBL( $L_g$ ) and (d)  $I_{on,sat}(L_g)$  following 2D device simulations with and without boron dose loss model.

#### 4.2.2 Boron precipitation in FDSOI pMOS transistors

Among the silicon based solutions to continue MOS transistors downscaling, fully depleted silicon on insulator (FDSOI) transistors can be used. In comparison to bulk transistors, FDSOI transistors are manufactured using SOI wafers with a thin silicon top layer ( $\leq 30$  nm) where source and drain junctions are made. In FDSOI, the junction depth is thus defined by the top silicon film thickness  $T_{Si}$ . In addition, the channel region is fully depleted with no need for channel doping leading to an improved electrostatic control, SCEs, mobility and devices variability [4, 5]. The feasibility of extremely thin

SOI (ETSOI) transistors was also demonstrated in [6], where silicon film was scaled down to 3.5 nm making SOI devices a promising solution for technology nodes below 16 nm.

In addition to electrical characteristics improvement, FDSOI transistors are quite interesting for dopant diffusion reduction and electrical activation enhancement. Indeed, the silicon active layer in FDSOI transistors is surrounded by two silicon oxides: the buried oxide (BOX) and the surface oxide. During thermal annealing, Si self interstitials generated by implants recombine at the available silicon/oxide interfaces [7]. Therefore, in FDSOI devices interstitials recombination is enhanced when compared to bulk Si, reducing boron TED and EOR defects formation [8, 9].

In this section, we will investigate boron precipitation mechanisms in 28 nm technology node pMOS FDSOI transistors manufactured at STMicroelectronics. Indeed as in bulk technologies, following extensions and source drain implantations, boron and silicon interstitials concentration exceed  $10^{20} \text{ cm}^{-3}$  and large BICs may form as already observed in 2.4. The effect of source/drain implantation conditions on FDSOI transistors with lengths between 28 nm and 1  $\mu\text{m}$  were therefore investigated. Experimental  $V_{t,\text{lin}}(L_g)$ ,  $V_{t,\text{sat}}(L_g)$  and  $I_{\text{on,sat}}(L_g)$  characteristics were extracted. For source and drain regions,  $\text{BF}_2$  implants are used and led to the investigation of three conditions summarized in table 4.1. A reference sample  $C_1$  was used with a given  $\text{BF}_2$  implantation energy and dose, spike annealed at 1040°C. Sample  $C_2$  has the same dose as  $C_1$  and was annealed at 1050°C and  $C_3$  has two times  $C_1$  dose also spike annealed at 1050°C (table 4.1).

Table 4.1: Summary of the different  $\text{BF}_2$  source/drain implantation conditions investigated experimentally on FDSOI pMOS transistors with gate lengths between 28 nm and 1  $\mu\text{m}$ .

Source/drain $\text{BF}_2$ implantation	$C_1$	$C_2$	$C_3$
Dose( $C_1$ )	x	x	
$2 \times \text{Dose}(C_1)$			x
Spike 1040°C	x		
Spike 1050°C		x	x

2D TCAD process simulations using the large BICs continuum model presented in 2.4.2 were carried out and corresponding electrical characteristics from device simulations were compared to experimental data.  $C_1$  condition 2D profiles for boron active concentration  $B_{\text{act}}$ , boron in the LBICs  $C_{B,\text{LBICs}}$  and LBICs density  $D_{\text{LBICs}}$  for 28 nm gate length FDSOI pMOS transistor are presented in Fig. 4.3. From Fig. 4.3, we can notice that following thermal annealing,  $C_{B,\text{LBICs}}$  (Fig. 4.3b) and  $D_{\text{LBICs}}$  (Fig. 4.3c) fields concentrations are low in comparison to active boron field concentration. Indeed, as already noticed in [8, 9] for classical interstitials EOR defects, the proximity of both surface and BOX oxide to high boron and silicon interstitials concentration region in FDSOI pMOS transistors leads to an interstitials recombination reducing boron content in the LBICs and LBICs density, already observed in [10]. In addition, the salicidation for electrical contact of source and drain regions consumes silicon material as observed in Fig. 4.3, also decreasing the LBICs population in source/drain highly doped regions.

The different process simulated transistors of table 4.1 using the LBICs continuum model, were injected in SDevice simulator in order to model electrical  $I_d(V_g)$  characteristics. Corresponding  $\Delta V_{t,\text{lin}}(L_g)$ ,  $\Delta V_{t,\text{sat}}(L_g)$ , DIBL( $L_g$ ) and  $I_{\text{on,sat}}(L_g)$  were extracted and compared to experimental data respectively in Fig. 4.4a, 4.4b, 4.4c and 4.4d. Using the LBICs model, the dose effect between  $C_1$  and  $C_3$  observed experimentally on the electrical characteristics is well reproduced. The LBICs model

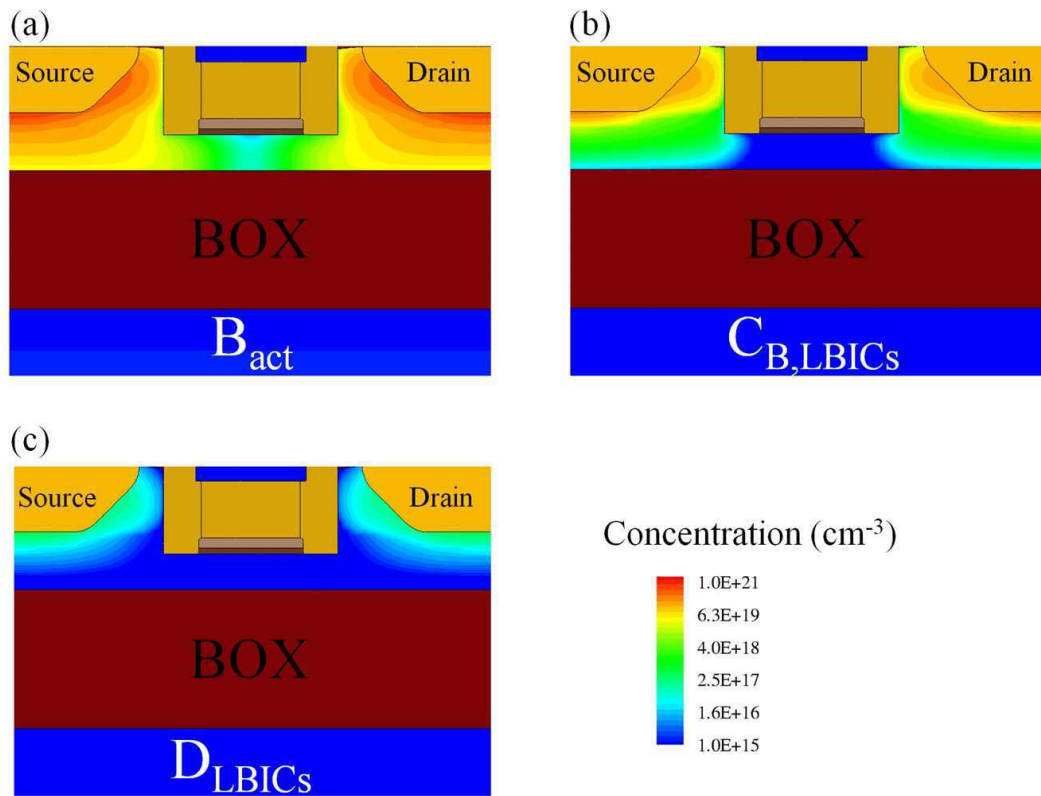


Figure 4.3: 2D process simulations using large BICs continuum model on FDSOI pMOS transistor of 28 nm gate length using  $\text{BF}_2$  implantation condition  $C_1$  of table 4.1 including (a) boron active concentration, (b) boron in the LBICs concentration  $C_{B,LBICs}$  and (c) LBICs density  $D_{LBICs}$ .

correctly predicts boron dose effect and corresponding activation mechanisms in advanced pMOS FD-SOI transistors.

The thermal anneal effect on electrical characteristics when comparing  $C_1$  and  $C_2$  is qualitatively reproduced. However, this effect is stronger in the experiments in comparison to our simulations. The spike anneals carried out for these simulations include ramp-up and ramp-down steps, leading to temperature range probably not covered by our LBICs model calibration of chapter 2 and explaining the differences between experiments and TCAD simulations.

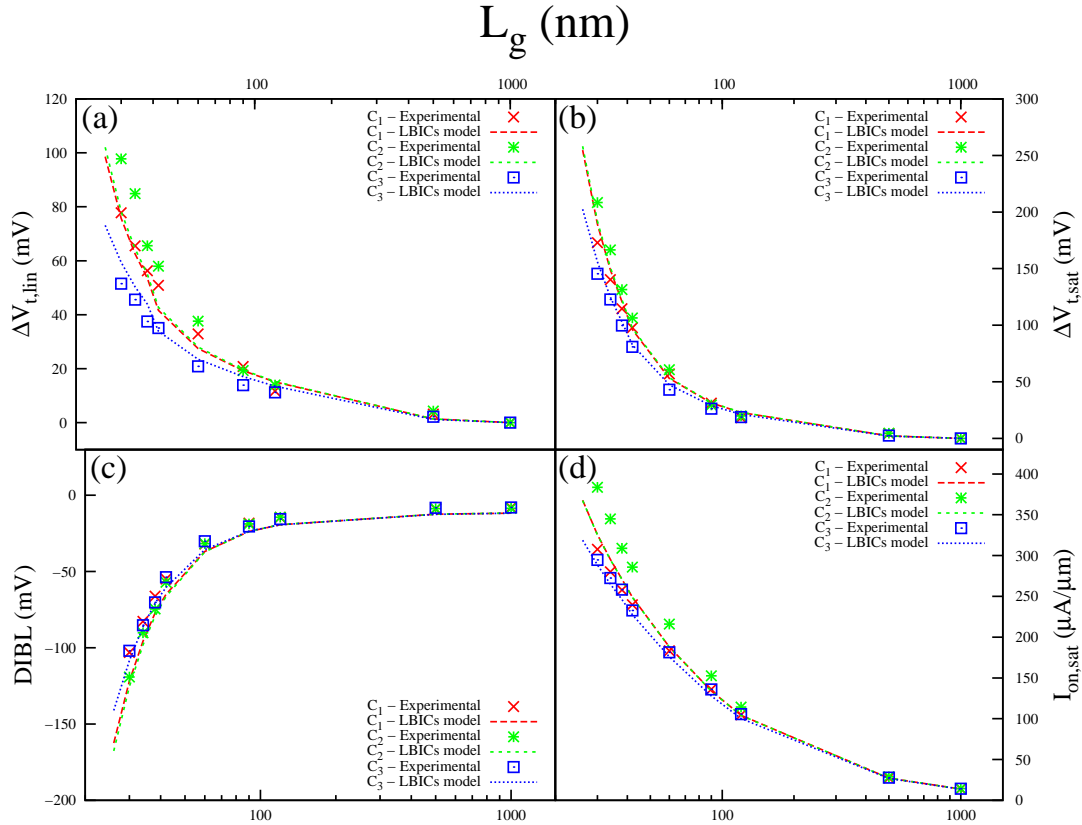


Figure 4.4: 28 nm technology node FDOSI pMOS transistors electrical characteristics versus gate length with different process conditions of table 4.1 including (a)  $\Delta V_{t,lin}(L_g)$ , (b)  $\Delta V_{t,sat}(L_g)$ , (c) DIBL ( $L_g$ ) and (d)  $I_{on,sat}(L_g)$  following 2D device simulations using LBICs continuum model developed in 2.4.2.

### 4.2.3 PIII in TriGate nMOS transistors

In 4.2.1 and 4.2.2, we evaluated our models on planar MOS transistors technologies: bulk with 45 and 28 nm nodes and FDSOI with 28 nm node. Planar FDSOI transistors technology is a promising alternative for 20 nm CMOS technology node and below [5, 6]. However, for more aggressive technology nodes below 16 nm, silicon based planar devices even with a SOI scheme show several limits in terms of electrostatics control, low power and SCEs.

To this aspect, three dimensional transistors (fabricated on bulk or SOI substrates) have already been proposed to replace planar devices for deep sub-micron transistors, solving several miniaturization challenges. Multi-gates are used in these 3D transistors including: fin field effect transistors (FinFET) with a channel control by two vertical and facing gates [11, 12], TriGate transistors with a



three sided gate [13],  $\Omega$ -gate and gate all around (GAA) nanowires [14, 15]. Among the different multi-gate transistors, main semiconductor industrial groups recent R&D efforts concentrated on TriGate devices [16, 17]. TriGate nMOS transistors are investigated in this sub-section using TCAD modelling.

Fig. 4.5a shows a 3D simulation of a nMOS TriGate FinFET transistor with its main dimensions: gate length  $L_g$ , lateral dimension  $W_{fin}$  and vertical dimension  $H_{fin}$  at the TriGate side-walls. Contrarily to planar MOS transistors, electrons current between source and drain regions in TriGates takes place in both horizontal and vertical planes. As a consequence, source/drain and extensions 3D doping has to be conformal in order to obtain the same electrons conduction in all directions and benefit from the TriGates 3D structure. Conformal 3D TriGates doping can be obtained by two implantation approaches:

- Multi-tilt beam line implants where several beam-line implantation steps with different tilts are carried out in order to obtain the desired 3D conformal doping. In this approach, shadowing effects have to be carefully taken into account, and the conformal aspect is improved by multiplying the number of tilts. In addition, the chosen implant energy and dose depend on the geometrical characteristics of the TriGates (dimensions, rounding ...). For these reasons, the beam-line approach for TriGate 3D conformal doping can be quite complex and costly.
- PIII, where the 3D conformal doping is achieved thanks to the “built-in” angular distribution of the implanted ions in the plasma sheath, as already detailed in 2.2. This approach is both faster and cheaper than the multi-tilt beam-line one and does not depend on the geometrical characteristics of the TriGates. Precise conformal doping has been demonstrated using PIII [18, 19]. In addition to cost/time advantages, careful choice of PIII conditions results in better devices characteristics for both p-type [20] and n-type [21] TriGate FinFETs.

In this work, n-type Tri-Gate MOS transistors with gate length  $L_g$  between 20 and 100 nm,  $W_{fin} = 100\text{nm}$  and  $H_{fin} = 40\text{nm}$  are simulated using beam-line implantation and PIII conditions. Extension doping using beam-line multi-tilt implants ( $0^\circ$ ,  $20^\circ$  and  $45^\circ$ ) and PIII and their corresponding effects on electrical characteristics of nMOS TriGate are investigated. The same source/drain implants, pocket implants and laser sub-melt activation anneals were used in both conditions. Extension beam-line and PIII conditions were adjusted in order to get highly doped USJs, when using the two techniques. Monte Carlo method was used in TriGate 3D simulations for extensions arsenic multi-tilt beam-line implants. Before PIII 3D simulation, a first 1D calibration was carried out. As for p-type  $\text{BF}_3$  PIII presented in 2.3.2, the 2-exp energy of equation 2.2 was used and calibrated on  $\text{AsH}_3$  PIII SIMS profiles. A simple approach using Monte Carlo method was then used here in order to reproduce the conformal doping of PIII [22]. In this simple approach, implanted ions can be launched along the simulated structure interface with the ambient. If this interface is not flat and has a 3D structure, a resulting 3D conformal doping will be obtained.

Beam-line implants and PIII results are respectively shown in 3D arsenic profile of Fig. 4.5b and 4.5c. From these process simulations conditions, the 3D conformal aspect of PIII in comparison to multi-tilt beam-line implants can be noticed. Of course, beam-line implantation can also be optimized in order to reach similar conformal doping as for the PIII case. Thus, the aim of this section is to investigate the effect of conformal doping, obtained in our simulations using PIII in comparison to a less conformal doping strategy using a particular set of multi-tilt beam-line implants.

The effect of the conformality of the doping will be monitored on the electrical characteristics of n-type TriGate transistors extracted from 3D device simulations. Electrical characteristics include: DIBL ( $L_g$ ) (Fig. 4.6a), sub-threshold slope in linear and saturation regimes  $S_{t,lin}(L_g)$  and  $S_{t,sat}(L_g)$  (Fig. 4.6b), On current in saturation regime  $I_{on,sat}(L_g)$  (Fig. 4.6c) and Off current in saturation regime



$I_{\text{off,sat}}(L_g)$  (Fig. 4.6d). Simulation results show that when using PIII, better DIBL (Fig. 4.6a), sub-threshold slope in saturation regime  $S_{t,\text{sat}}$  (Fig. 4.6b) and Off current in saturation regime  $I_{\text{off,sat}}$  (Fig. 4.6d) are obtained for short channels TriGate transistors, in comparison to beam-line implantation. In the meantime, similar sub-threshold slope in linear regime  $S_{t,\text{lin}}$  (Fig. 4.6b) and On current in saturation regime  $I_{\text{on,sat}}$  (Fig. 4.6c) are obtained in both beam-line implantation and PIII techniques. Given the cost/time advantages in comparison to beam-line implantation, PIII is a promising technique for sub-20 nm TriGate transistors. Our electrical simulations are in agreement with recent experimental results showing better electrical performances for TriGate FinFETs when using PIII [20, 21].

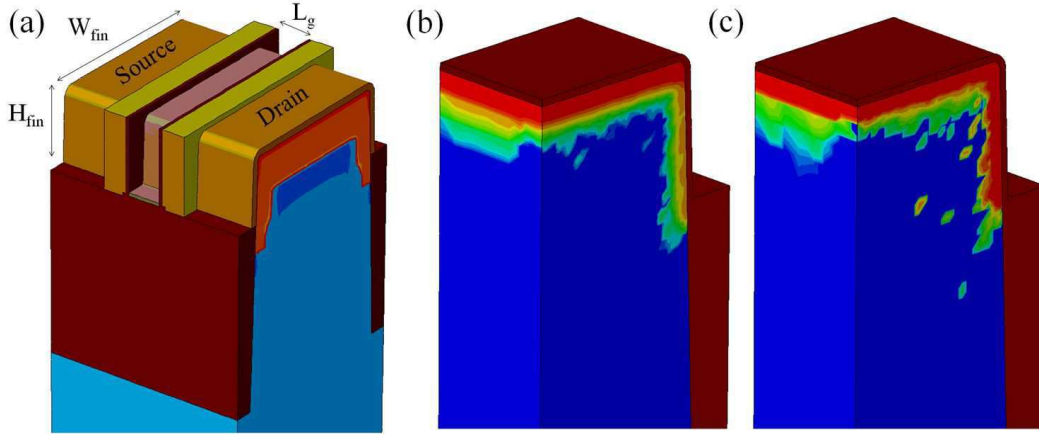


Figure 4.5: 3D process simulations of (a) n-type TriGate transistor with  $L_g = 20\text{nm}$ ,  $W_{\text{fin}} = 100\text{nm}$  and  $H_{\text{fin}} = 40\text{nm}$ . 3D arsenic profiles following extension implantation obtained using multi-tilt ( $0^\circ$ ,  $20^\circ$  and  $45^\circ$ ) beam-line arsenic implants (b) or  $\text{AsH}_3$  PIII (c) where the conformal aspect of the implant can be noticed.

## 4.3 FSI CMOS image sensors modelling

### 4.3.1 Boron dose loss in TG of FSI CMOS image sensors

As discussed in chapter 1 (Fig. 1.4 and 1.5), boron  $p^+$  pinning implants are used in n-type photodiodes of CMOS image sensors to avoid SCR extension to the surface oxide/silicon interface and corresponding dark current. In the particular case of frontside imagers, the boron  $p^+$  region is in contact with the spacer stack of the TG of the pixel. Therefore, similarly to the case of spacers in simple MOS transistors, boron dose loss is expected in the  $p^+$  pinning region of FSI pixels. In addition, boron dose loss may also take place above the photodiode region far from the TG, where boron from  $p^+$  implant is directly in contact with an oxide/nitride stack used for silicon protection during electrical contacts process, also called “Si protect stack”. Boron dose loss effects on electrical characteristics of the  $1.4\ \mu\text{m}$  pixels shown in Fig. 1.4 are investigated here. 3D coupled process and electro-optical device simulations (detailed in [23, 24]) were carried out in order to monitor the following electrical characteristics:

- $Q_{\text{sat}}$ : evaluated for a given pixel after completely depleting the photodiode and artificially enhancing electron-hole pairs generation in the photodiode until simulated integrated electrons density (in  $\text{cm}^{-3}$ ) in the photodiode reaches a saturation value.
- $QE(\lambda)$ : evaluated for the different pixels (R, GR, GB and B) of a four pixels Bayer pattern with periodic boundary conditions. QE for a given pixel and a given wavelength is defined by the ratio of the number of photogenerated electrons collected by the photodiode on the number

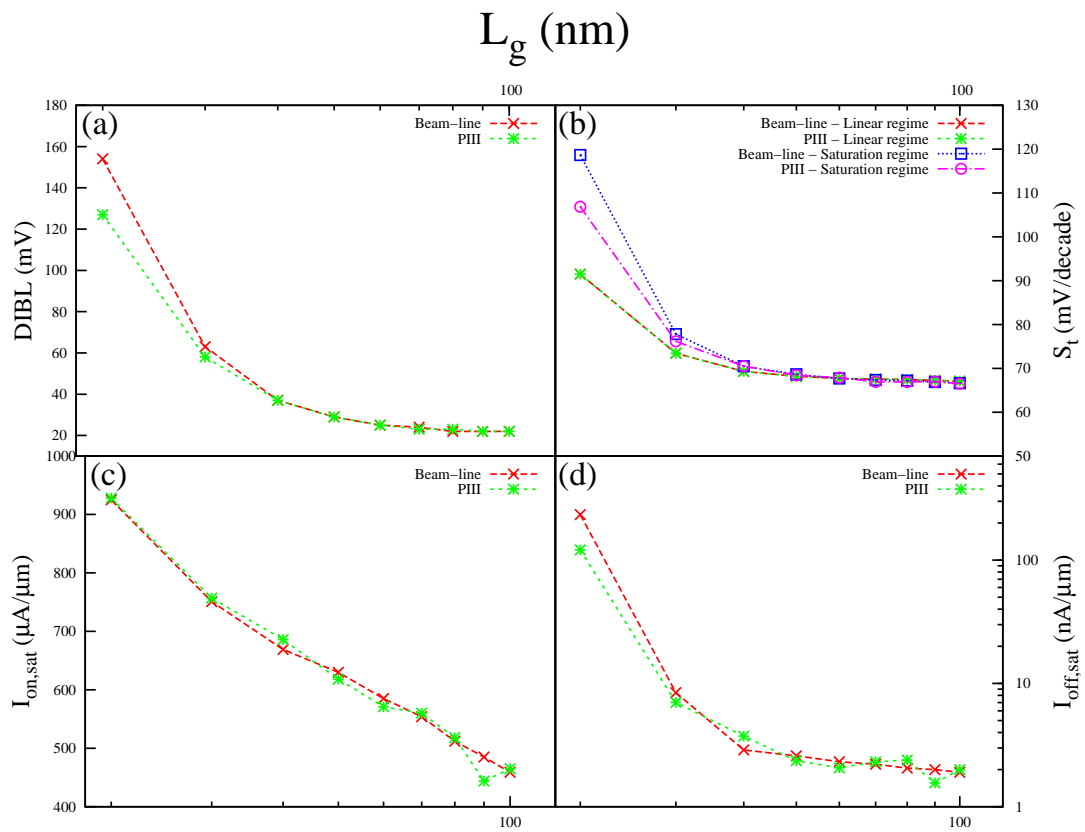


Figure 4.6: N-type TriGate transistors electrical characteristics versus gate length for extensions beam-line arsenic implantation and AsH<sub>3</sub> PIII including (a) DIBL ( $L_g$ ), (b)  $S_{t,lin}$  ( $L_g$ ) and  $S_{t,sat}$  ( $L_g$ ), (c)  $I_{on,sat}$  ( $L_g$ ) and (d)  $I_{off,sat}$  ( $L_g$ ) following 3D device simulations.

of incident photons extracted from optical simulations [23]. The number of photogenerated electrons is calculated by integrating the electron density in the photodiode during an integration time  $t_{\text{int}}=66.7$  ms corresponding to 15 captured images/second in a real image sensor.

- $I_{\text{dark}}$ : calculated from experimentally calibrated GR currents resulting from the traps at the different interfaces in the pixel: silicon/STIs oxide, silicon/DITs oxide, silicon/gate oxide, silicon/spacer oxide and silicon/Si protect stack. Given the process conditions of the pixel, no implantation-induced EOR defects are expected to form in the SCR region of the n-type photodiode. In addition, we assume that no metal contaminants can be found in the SCR region of the photodiode. Therefore, no silicon volume defects are responsible for GR mechanisms contributing to the dark current calculation. Due to the different trap energy levels at the various interfaces of the pixel, electrons are generated, then collected by the photodiode and their concentration increases linearly with time in the dark without any external source of light. In this linear regime, the electrons density volume integral, or number of electrons in the photodiode is plotted versus time and the slope of the curve corresponds to the dark current:

$$I_{\text{dark}} = \left. \frac{\Delta e^-}{\Delta t} \right|_{\text{lin}} \quad (4.1)$$

- Electrons transfer and lag in the photodiode: where electrons transfer from the photodiode to the SN is evaluated. In such simulations [25], the following transfer steps are modelled:
  1. Illumination: the pixel is illuminated using a monochromatic laser optical source. During the step of  $10 \mu\text{s}$ , the photodiode is filled with photo-generated electrons. All along the simulation, a positive voltage is applied on the SN while TG is in Off state
  2. TG ramp-up: in this step the TG voltage is ramped up from an Off value to an On value during  $0.3 \mu\text{s}$  in order to create an inversion layer between the photodiode and the SN allowing the electrons transfer from the photodiode to the SN.
  3. TG On plateau: a TG On value is kept during  $1 \mu\text{s}$  in order to allow electrons transfer from the photodiode to the SN for image integration. During this step, the photodiode is emptied of its electrons.
  4. TG ramp-down: as for the TG ramp-up step, TG voltage is ramped down from the On value to an Off value during  $0.3 \mu\text{s}$ . Following this step, no electrons are expected to be left in the photodiode. Actually, they are supposed to have been transferred during the TG ramp-up and On plateau steps. However, depending on the photodiode's 3D doping extension, some electrons may remain in the photodiode even after the ramp down. Such effect of remaining electrons corresponds to what is called lag discussed in 1.3.2.

The previous image sensors electrical features were evaluated with and without boron dose loss model developed in 3.2. Corresponding 3D process simulations are shown in Fig. 4.7 including net doping concentration in Fig. 4.7a and 4.7b, and boron concentration in Fig. 4.7c and 4.7d. From the simulations, we can notice that when boron dose loss is modelled in Fig. 4.7d, boron concentration level in the pinning implant region is lower than in Fig. 4.7c where no boron dose loss is included.

Following 3D process simulations with and without boron dose loss model, electro-optical simulations were carried out and are shown in Fig. 4.8.

In saturation regime very small differences are observed in  $Q_{\text{sat}}$  simulations from Fig. 4.8a leading to  $Q_{\text{sat}} = 3251$  electrons with the dose loss model, only 44 electrons higher than without dose loss where  $Q_{\text{sat}} = 3207$  electrons. Due to boron dose loss, boron concentration near the surface interface is lower leading to a higher extension of the photodiode SCR near the interface, slightly increasing the

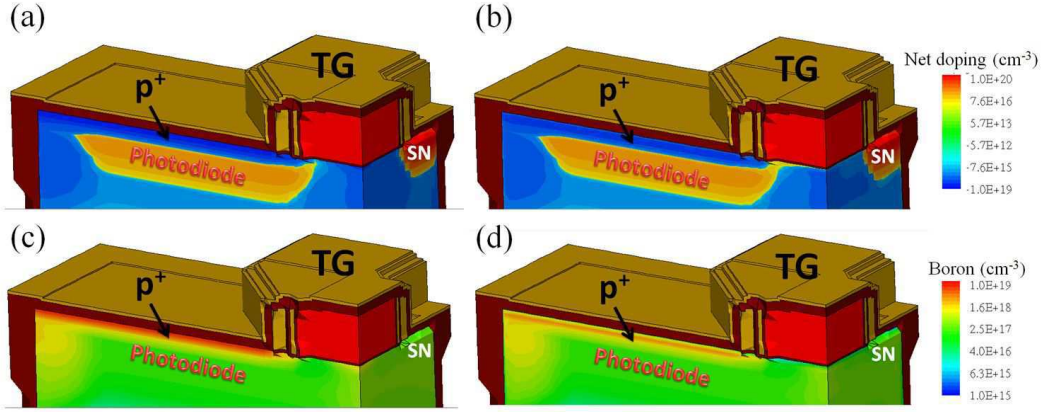


Figure 4.7: 3D process simulations of 1.4  $\mu\text{m}$  FSI pixels including (a) net doping concentration without and (b) with boron dose loss model. Is also shown boron concentration (c) without and (d) with boron dose loss model.

number of collected charges in saturation regime when the dose loss is included. The linear regime of photodiode filling with electrons is also presented in Fig. 4.8a. In this case, the number of electrons characteristic is the same with and without boron dose loss model.

Indeed, from Fig. 4.8b, no difference is observed on  $QE(\lambda)$  characteristics simulated in linear regime. This result can be expected because p<sup>+</sup> implant extension with and without boron dose loss shown in Fig. 4.7a and 4.7b does not modify significantly the n-type photodiode extension in the region where the photons are collected. The p<sup>+</sup> pinning implant/n photodiode junction is the same in both cases and differences in terms of SCR extension mainly occur close to the surface region below the Si protect stack/silicon interface, which has no impact on QE characteristics carried out in linear regime for different wavelengths.

SCR region is closer to the surface interface when dose loss is included, and mainly above the photodiode region at the Si protect stack/silicon interface. GR mechanisms in this region are expected to be more important when the dose loss is included. Indeed, from simulations of Fig. 4.8c, we can notice that dark current almost doubles when boron dose loss is included.

Finally, and as explained above, electrons lag following a transfer cycle can be modelled and corresponding results are presented in Fig. 4.8d, where almost no electrons lag is observed when boron dose loss is taken into account, while 137 electrons remain without the dose loss model. Due to a higher SCR extension near the interface when the dose loss is included, a better transfer is obtained. Electrons have to overcome an energy barrier due to p-doping below the spacer region of the TG in order to be transferred to the SN. When the boron dose loss model is included, the energy barrier is lowered leading to better transfer.

#### 4.3.2 PIII in DTIs of FSI CMOS image sensors

In previous section, the p<sup>+</sup> surface pinning implant is used in order to avoid the SCR extension at the surface interface. We observed that when boron dose loss is included, the SCR is closer to the surface interface due a lower boron concentration, which leads to a higher dark current from Fig. 4.8c. In the same manner, in order to avoid the n-type photodiode SCR lateral extension, and its contact with DTIs oxide/silicon interfaces (also source of dark current) additional p-type multi-tilt implants, generally using BF<sub>2</sub> are carried out in the DTIs region before filling them with oxide. It should be noticed that these BF<sub>2</sub> multi-tilt beam-line implants have already been used in the simulations of 4.3.1

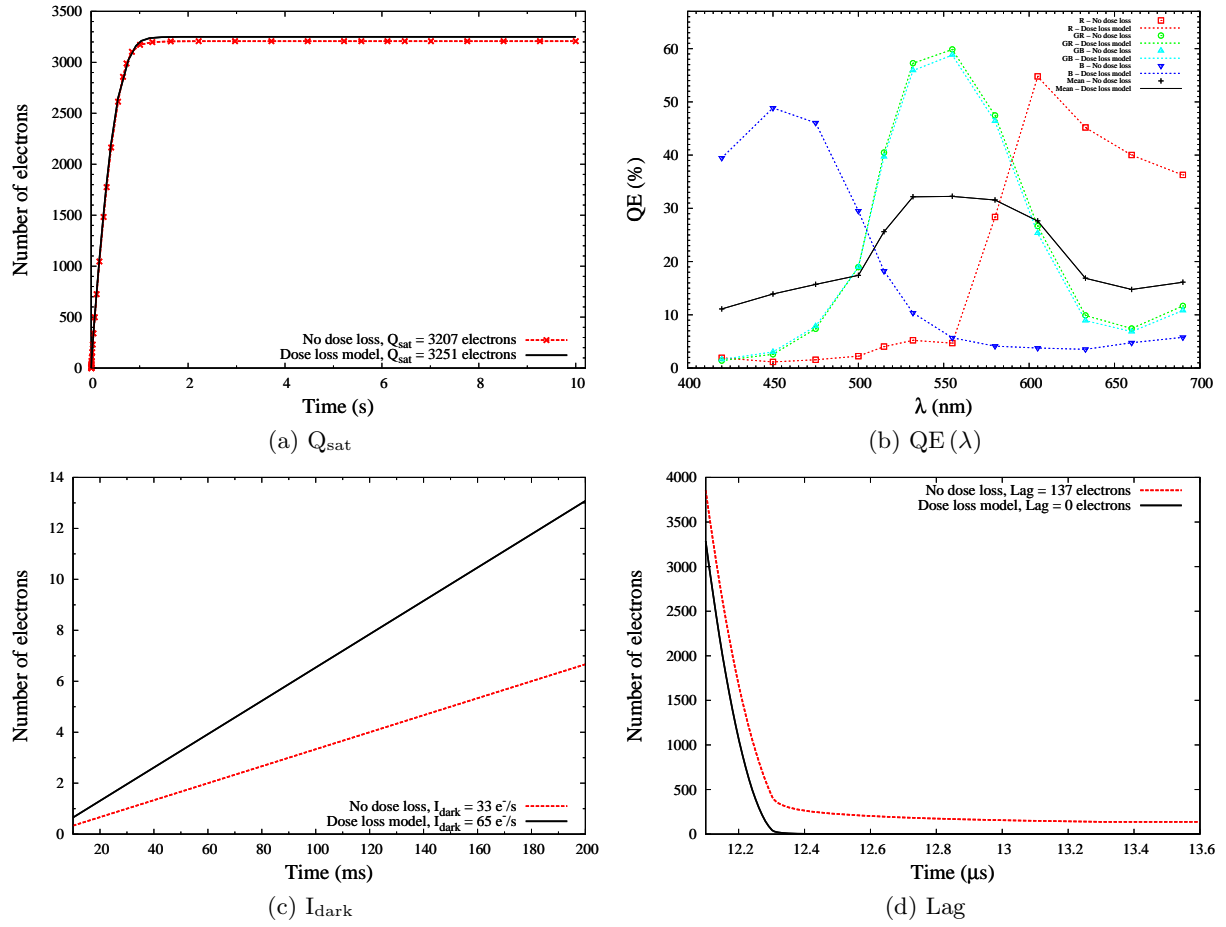


Figure 4.8: Electro-optical device simulation results for 1.4  $\mu\text{m}$  FSI pixels without and with boron dose loss model of 3.2 including (b)  $Q_{\text{sat}}$ , (a)  $QE(\lambda)$  characteristics, (c)  $I_{\text{dark}}$  and (d) electrons lag.

summarized in Fig. 4.7 and 4.8. For better dark current performances, conformal doping along the DTIs seems quite adequate. As already noticed in 4.2.3 on n-type TriGate transistors extension conformal doping, PIII can be used in this case for DTIs.

Two PIII conditions  $P_1$  ( $\text{BF}_3$  2 kV  $3.8 \times 10^{13} \text{ cm}^{-2}$ ) and  $P_2$  ( $\text{BF}_3$  3 kV  $9.2 \times 10^{13} \text{ cm}^{-2}$ ) for DTIs implants were therefore investigated and compared to a reference beam-line condition  $B_1$  using multi-tilt  $\text{BF}_2$  implants. Corresponding 3D doping boron profiles along the DTIs are shown in Fig. 4.9 in addition to 1D cuts (black dashed lines in Fig. 4.9) of boron profiles presented in Fig. 4.10. The 1D boron profiles show that a higher DTIs oxide/silicon interface concentration can be obtained when using PIII conditions in comparison to beam-line condition, which is beneficial in order to avoid the n-type photodiode SCR extension near the interface.

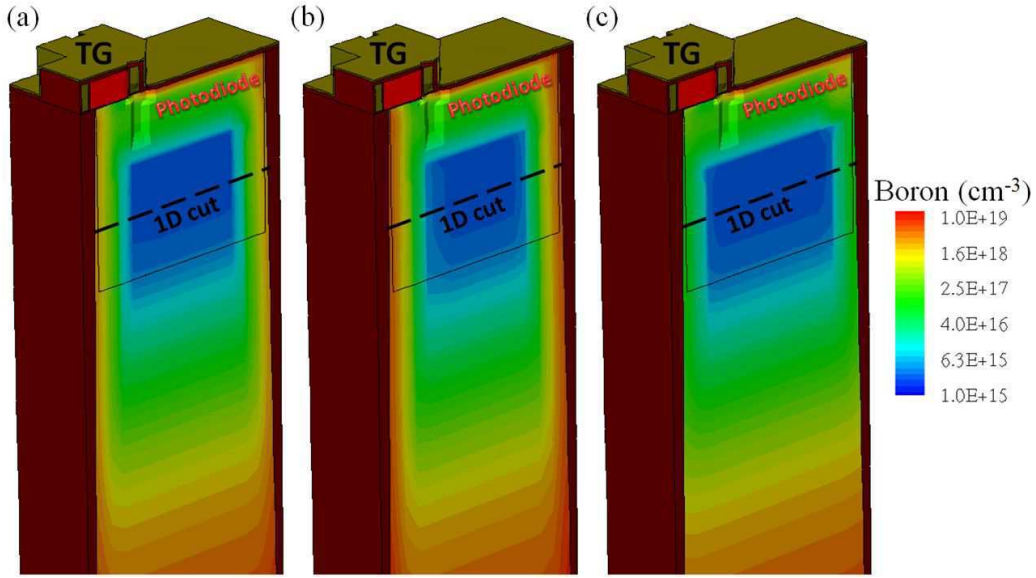


Figure 4.9: 3D boron profiles following simulations of  $1.4 \mu\text{m}$  FSI pixels including (a) PIII  $P_1$  condition ( $\text{BF}_3$  2 kV  $3.8 \times 10^{13} \text{ cm}^{-2}$ ) (b) PIII  $P_2$  condition ( $\text{BF}_3$  3 kV  $9.2 \times 10^{13} \text{ cm}^{-2}$ ) and (c) reference multi-tilt beam-line implantation  $B_1$  condition. A 1D cut (black dashed line) is made on the different 3D structures and corresponding boron profiles are shown in Fig. 4.10.

Electrical features  $Q_{\text{sat}}$  and  $I_{\text{dark}}$  of the different DTIs implantation conditions are given in table 4.2, where equivalent values are obtained for the three implantation conditions. As for TriGate transistors conformal doping in 4.2.3, PIII is an interesting alternative in terms of cost and time for DTIs implantation leading to electrical performances similar to the ones obtained using beam-line implantation.

However, considering dark current simulations of table 4.2, similar traps characteristics (energy levels, capture cross section, surface density) were assumed at the DTIs oxide/silicon interface for both PIII and beam-line implantation. In our simulations, the dark current small differences between the three conditions is only due to differences in terms of boron doping at the DTIs oxide/silicon interfaces. Due to the high sensitivity of dark current to interface traps, the two implantation techniques may lead to different dark current levels.

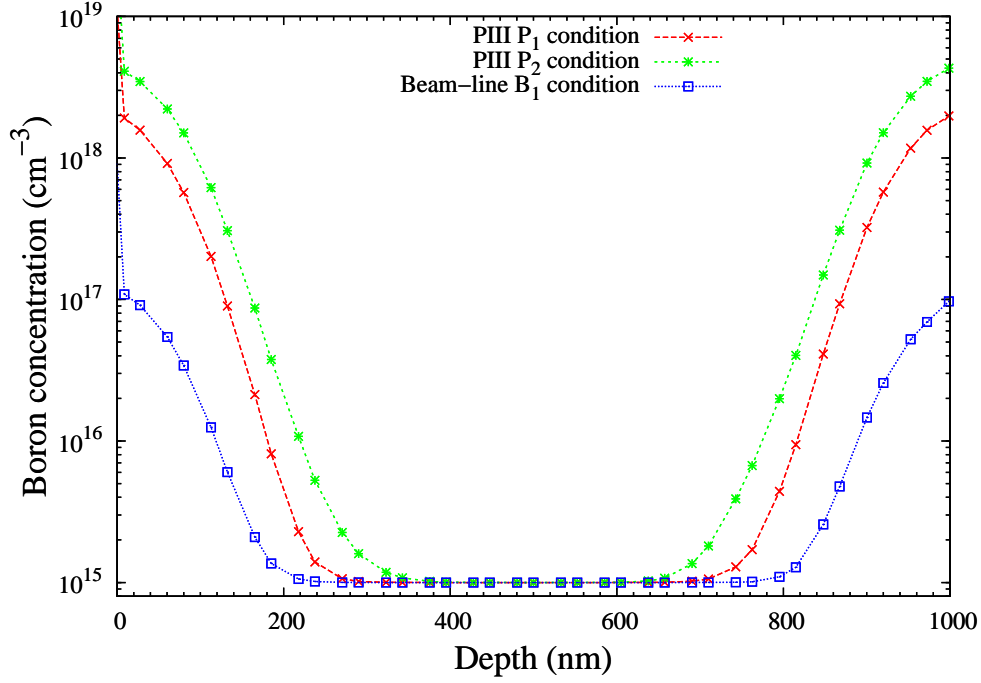


Figure 4.10: Boron 1D profiles following the 1D cut of 3D simulated structures shown in Fig. 4.9 for implantation conditions PIII P<sub>1</sub>, PIII P<sub>2</sub> and beam-line implantation B<sub>1</sub>.

Table 4.2: Electrical features including  $Q_{\text{sat}}$  and  $I_{\text{dark}}$  obtained from 3D simulations for the different DTIs implantation conditions of 1.4  $\mu\text{m}$  FSI pixels, assuming identical interface traps.

DTIs implantation	$Q_{\text{sat}}$ (electrons)	$I_{\text{dark}}$ ( $\text{e}^-/\text{s}$ )
PIII P <sub>1</sub>	3201	39
PIII P <sub>2</sub>	3091	38
Beam-line B <sub>1</sub>	3237	40



## 4.4 BSI CMOS image sensors modelling

As presented in chapter 1 (cf. section 1.3.3.2), BSI image sensors have been developed over the last years in order to improve QE and crosstalk features. In the BSI scheme, the pixels performances can be enhanced when replacing the backside SOI oxide by a nitride/oxide/nitride (ONO) stack acting as an anti-reflective layer for higher light collection [26, 27]. In addition, with pixel size reduction, the surface of a planar photodiode collection region is reduced, and consequently the number of photo-generated charges and  $Q_{\text{sat}}$  value decrease. To solve this problem, photodiodes with vertical and deep doping extensions (already presented in Fig. 1.5) have been recently designed [26, 28].

When a vertical photodiode is used in association with a SOI box oxide or ONO stack, the photodiode SCR extension may reach the box oxide/silicon backside interface, therefore increasing dark current if interface carriers are present. For n-type photodiodes, a boron backside implant is therefore required mainly to recombine electrons generated by interface traps, but also to avoid the n photodiode SCR contact with the backside oxide/silicon interface.

The boron back-side implant can be realized out using two main strategies:

1. Before the pixel active regions process: in this case, starting from a SOI wafer with an ONO stack and a thin silicon film, a boron (or  $\text{BF}_2$ ) beam-line implant is carried out in order to locate the boron profile  $R_p$  at the backside oxide/silicon interface in order and achieve a high boron concentration at this interface. Following this step, a silicon epitaxy on the thin silicon film is made, after which the different process steps of the pixel's active regions (STIs, DTIs, photodiode, TG) are performed. Within this strategy, boron implanted at the backside interface is electrically activated thanks to the different thermal anneals used in the pixel's active regions process steps. In this configuration, backside boron is in contact with an ONO stack and thus, boron dose loss in the ONO stack is expected. The effect of boron dose loss in the ONO stack following the pixel thermal anneals is investigated in section 4.4.1 on  $2\ \mu\text{m}$  BSI pixels.
2. After the pixel active regions process: in this case, the pixel active region process is initially carried out on a silicon substrate. The wafer is then flipped and the silicon substrate is thinned from the backside until reaching the DTIs region. Following this step, boron back-side implant is made. In order to electrically activate the backside implanted boron without modifying the pixel active regions doping due to undesired diffusion or deactivation, an LTA is used thanks to its ultra-fast and spatially localized characteristics. Following the LTA, the ONO stack is processed on the backside, and no dose loss takes place in this case due to the low thermal budget of the deposition steps of the ONO stack. The effect of the LTA energy on boron profile and corresponding electrical performances will be investigated in section 4.4.2 on  $1.1\ \mu\text{m}$  BSI pixels. It should be noticed that the ONO stack process steps used in this case are generally not the same as the one used in the first approach without LTA described above.

### 4.4.1 Back side boron dose loss in BSI CMOS image sensors

BSI pixels with  $2\ \mu\text{m}$  pitch and n-type photodiode, a boron backside implant and an ONO stack are investigated here using 3D TCAD process and electro-optical device simulations. In order to reduce process simulations CPU time of the Bayer structure simulations, boron backside profile diffusion and interaction with the backside ONO stack were simulated in 1D with all the process steps of the 3D simulations. The corresponding 1D diffused profile at the end of the fabrication process was injected in the 3D simulated structures for further device simulations. Fig. 4.11 is a diagram of backside boron dose loss in the ONO stack. It should be noted, that the oxide directly in contact with the boron backside implant, is thermally grown and therefore very low concentrations of hydrogen related species are expected in this oxide before the annealing steps. However, remaining nitride and oxide layers are

deposited using CVD techniques (similar to MOS transistors spacer materials). In our simulations, these nitride and oxide layers are respectively of NA and OA type with their corresponding hydrogen related species characteristics detailed in tables 3.2 and 3.4 of section 3.2. During thermal annealing, hydrogen can be transferred from NA nitride and OA oxide to thermally grown oxide, enhancing backside boron dose loss from silicon to the thermal oxide of the ONO stack.

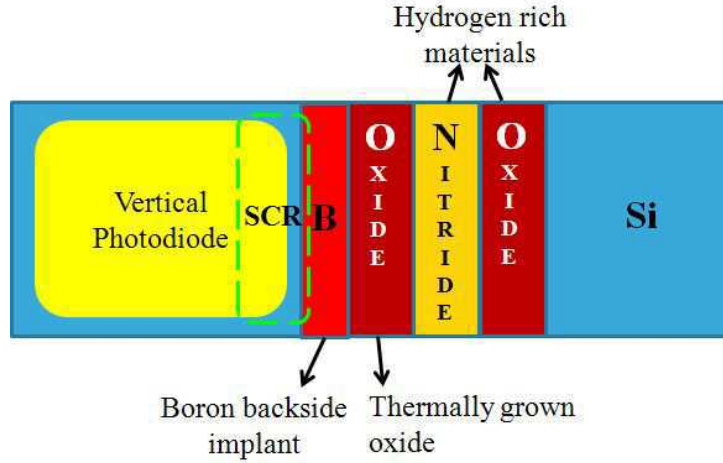


Figure 4.11: Diagram presenting the 1D system of backside boron dose loss in the ONO stack. The oxide directly in contact with boron is thermally grown. Remaining nitride and oxide layers are deposited using CVD techniques. SCR of n-type vertical photodiode is also presented.

Boron 1D profiles with and without boron dose loss are given in Fig. 4.12 where approximately one order of magnitude lower boron concentration at the backside silicon/oxide interface is observed when boron dose loss model is included. The 1D profiles of Fig. 4.12 were then injected in the 3D Bayer structure of  $2\ \mu\text{m}$  BSI pixels and QE ( $\lambda$ ) characteristics, shown in Fig. 4.13, were extracted from electro-optical device simulations. From QE ( $\lambda$ ) characteristics, we can observe that QE maxima for the different Bayer pixels are lower when boron dose loss is included. The boron profile collapse at the backside interface, observed in Fig. 4.12 probably induces a potential well for electrons preventing their collection by the n-photodiode and reducing QE; this effect is more pronounced for the blue pixel. Indeed, according to Beer-Lambert's law [29], blue photons are generated near the backside interface where boron dose loss occurred. Some of the generated electrons get trapped by the backside potential well and possible  $\text{SiO}_2/\text{Si}$  recombination centers.

#### 4.4.2 Back side LTA in BSI CMOS image sensors

Backside implant can also be performed out after the silicon active regions process steps as described above. Thermal activation of boron in this case is achieved using LTA in order to localize the anneal at the boron doped backside and avoid eventual modification of the pixels active regions doping. In this case, the anti-reflective (AR) backside stack, which can be different from the ONO stack described in 4.4.1, is fabricated after the LTA anneal.

The LTA anneal for backside dopant activation can be used in both sub-melt and melt regime. Melt regime is preferred due to higher activation levels and a better control of the backside junction depth defined by the liquid/solid interface depth  $X_{l/s}$ . Within the liquid region, high dopant diffusivity takes place, leading to box-shaped dopant profiles after the anneal.

BSI pixels with  $1.1\ \mu\text{m}$  pitch, a boron backside implant and different LTA anneals are investigated

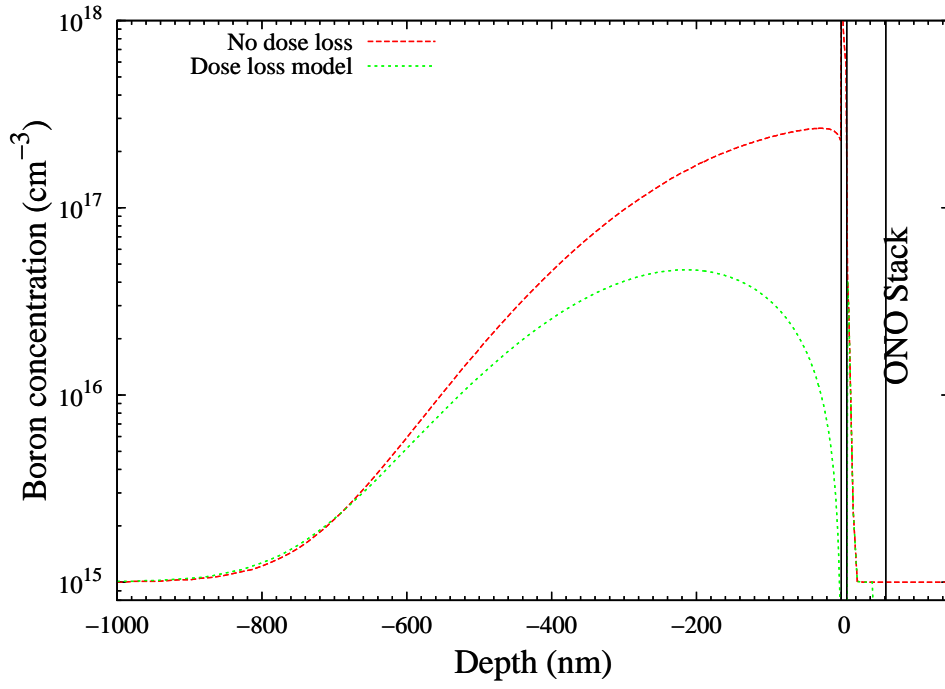


Figure 4.12: Boron 1D profiles at the backside interface with the ONO stack without and with boron dose loss model.

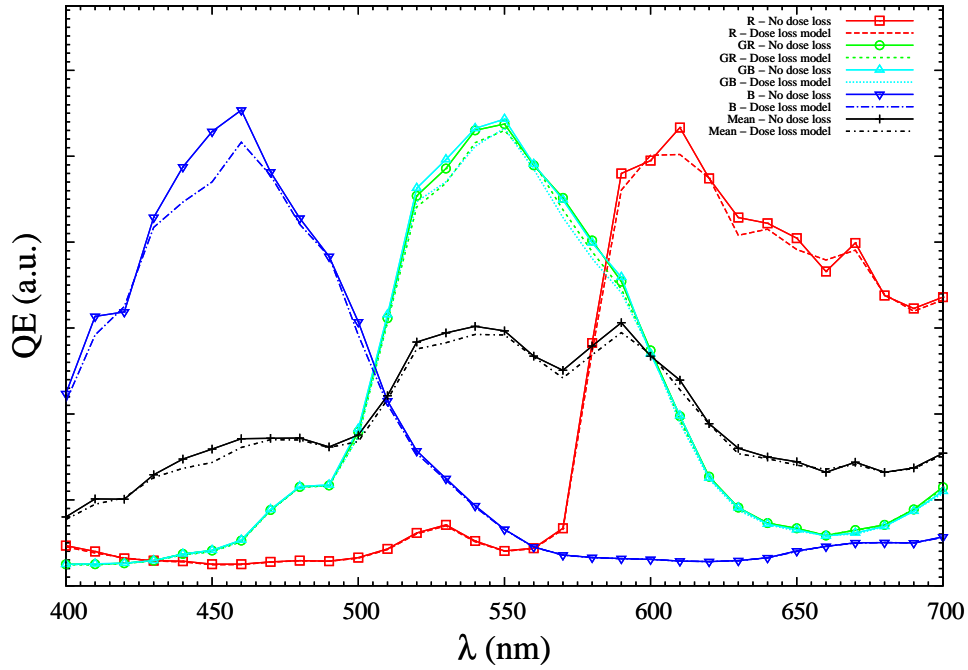


Figure 4.13:  $QE(\lambda)$  characteristics of a 3D Bayer structure of 2  $\mu\text{m}$  BSI pixels with and without backside boron dose loss in the ONO stack.

here using 3D TCAD process and electro-optical device simulations. The LTA for boron activation was modelled using the melting laser anneal (MLA) model developed by our partners within the ATE-MOX project and implemented in the latest versions of SProcess [22]. The model details are described in SProcess manual and references therein [22]. Using the calibrated parameters for the MLA model, and following a shallow boron backside implant, three LTA conditions were used with the following laser energy density:  $1.9 \text{ J.cm}^{-2}$  for  $L_1$  condition,  $2.1 \text{ J.cm}^{-2}$  for  $L_2$  condition and  $2.3 \text{ J.cm}^{-2}$  for  $L_3$  condition. Corresponding 1D boron dopant profiles and melting depths  $X_{l/s}$  are shown on Fig. 4.14. From the 1D simulations, the melting depth  $X_{l/s}$  increases with the laser energy density, determining boron profile extension. As expected, a boron plateau is observed for the different conditions due to the high diffusivity in liquid, in addition to a segregation peak at the liquid/solid interface, whose origin is investigated in [30].

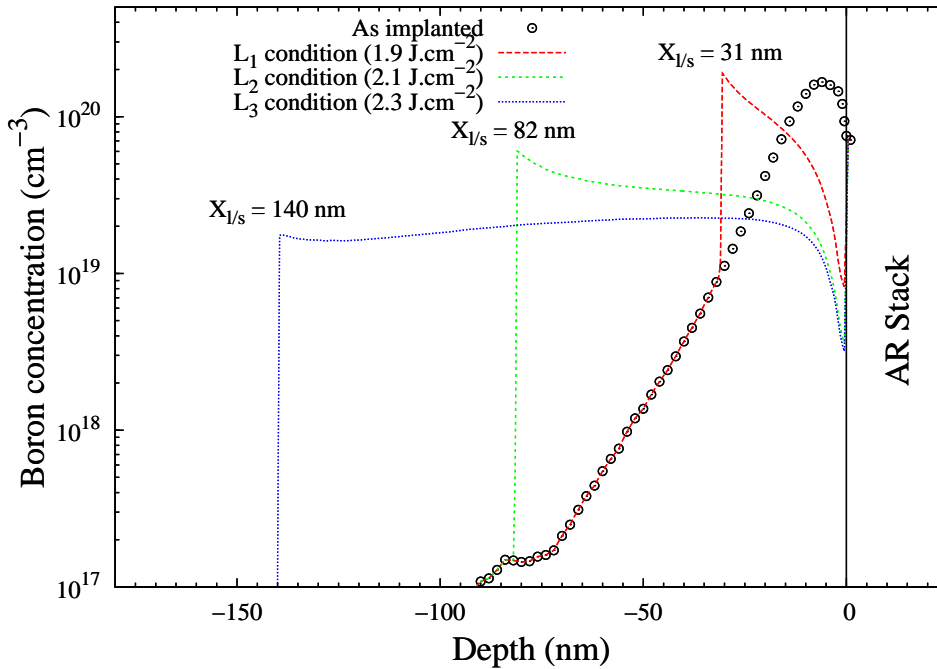


Figure 4.14: Boron 1D profiles at the backside interface with the AR stack following LTA anneales using  $1.9$  ( $L_1$ ),  $2.1$  ( $L_2$ ) and  $2.3$  ( $L_3$ )  $\text{J.cm}^{-2}$  laser energy density with corresponding melt depth  $X_{l/s}$ .

The 1D profiles for the three LTA condition of Fig. 4.12 were injected in 3D electro-optical simulations of  $1.1 \mu\text{m}$  BSI pixels with n-type vertical photodiode.  $I_{\text{dark}}$  values were extracted from these simulations and are summarized in table 4.3. Dark current simulations included backside interface traps and junction tunnelling GR mechanisms. From table 4.3, comparable dark current levels are observed for the three LTA conditions. A slightly lower  $I_{\text{dark}}$  value is obtained for  $L_1$  condition with  $1.9 \text{ J.cm}^{-2}$ , and can be explained by the higher boron doping concentration at the backside interface in comparison to  $L_2$  and  $L_3$  conditions.

Even though the MLA model developed in the frame of ATEMOX is able to simulate backside LTA, experimental data are still missing in order to confirm our simulations results for  $I_{\text{dark}}$  of  $1.1 \mu\text{m}$  BSI pixels using different LTA conditions.

Table 4.3: Electrical features including  $Q_{\text{sat}}$  and  $I_{\text{dark}}$  obtained from 3D simulations for the different backside boron LTA conditions of  $1.1 \mu\text{m}$  BSI pixels.

<b>LTA</b>	$I_{\text{dark}} \text{ (e}^-/\text{s)}$
$L_1 \text{ (1.9 J.cm}^{-2}\text{)}$	7.4
$L_2 \text{ (2.1 J.cm}^{-2}\text{)}$	8.5
$L_3 \text{ (2.3 J.cm}^{-2}\text{)}$	8.4

## 4.5 Conclusion

The process models developed during the PhD were evaluated in this chapter on real CMOS based devices manufactured at STMicroelectronics corresponding to the latest MOS transistors and CMOS image sensors technologies. The models allowed to improve TCAD predictability for new physical phenomena introduced by advanced process solutions, required by miniaturization and diversification challenges.

Boron dose loss modelling in spacer stacks has a clear impact on bulk 45 and 28 nm pMOS transistors electrical behaviour. High source/drain doping conditions in 28 nm FDSOI pMOS transistors unavoidably leads to the formation of large BICs, whose density can be reduced thanks to adequate high temperature spike annealing. This effect is correctly reproduced by our model and is in agreement with literature results. Corresponding TCAD electrical characteristics using the LBICs model match well experimental data. Conformal aspect of PIII in comparison with beam-line implantation was evaluated on 20 nm TriGate nMOS transistors where higher electrical performances were obtained, also in agreement with recent literature results.

After the first evaluation of our models on advanced MOS transistors, CMOS image sensors were investigated. Considering FSI  $1.4 \mu\text{m}$  pitch pixels, it was observed from 3D simulations, that  $p^+$  implant boron dose loss in the top surface region has a clear impact on dark current values. Therefore, boron dose loss can no longer be ignored in the surface pinning region of advanced pixels with n-type photodiodes. Thanks to our simulations mainly concentrating on the doping aspects, we also demonstrated that similar FSI  $1.4 \mu\text{m}$  pixels performances can be obtained when doping the DTIs with  $\text{BF}_3$  PIII or multi-tilt beam-line  $\text{BF}_2$  implants. However, the DTIs interface traps effect on dark current and eventual differences between the two implantation techniques was not investigated in our simulations due to a lack of experimental characterization.

Backside boron doping for n-type photodiode in  $2 \mu\text{m}$  BSI pixels, and boron dose loss in the ONO stack can also be reproduced thanks to our model, with a clear effect on  $\text{QE}(\lambda)$  characteristics, mainly for the blue pixels. Finally, LTA model developed by our partners in ATEMox project was evaluated on different laser conditions used in backside doping thermal activation of  $1.1 \mu\text{m}$  BSI pixels.

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# Conclusion

The aim of this PhD work was to improve TCAD process models of impurity diffusion and clustering phenomena in advanced CMOS based devices, with a particular focus on CMOS image sensors, where both miniaturization and diversification requirements are challenging.

The background of the PhD was first introduced where MOS transistor and CMOS image sensors in the frame of CMOS technology processes were presented. A summary of advanced process techniques and corresponding physical mechanisms allowed to identify strategies and improve existing TCAD models, as well as developing new ones in high-dose doping conditions and for chemical species diffusion in multi-materials stacks.

High dopant implantation doses used in advanced CMOS technologies lead to physical mechanisms not well understood or correctly modelled on the TCAD level. In this frame, the PIII technique was studied. Dedicated  $\text{BF}_3$  plasma implanted experiments were designed and led to a successful modelling of both implantation doping profiles and amorphization depth. Annealed samples brought out the formation of LBICs, which strongly influence dopant diffusion and activation. Due to the lack of LBICs TCAD models, a continuum model based on moments approach was developed which reproduced several literature experimental data on simple boron beam-line implants. When applied to  $\text{BF}_3$  PIII, the LBICs model clearly improved the prediction of boron diffusion and electrical activation.

Chemical species diffusion between materials in multi-materials stacks becomes of paramount importance in CMOS devices, due its consequence on the devices electrical characteristics. Among the modelling challenges covered during the PhD, boron dose loss in nitride/oxide/silicon stacks found in MOS transistors spacers or CMOS image sensors AR layer, was investigated. Our study led to a boron dose loss model with boron diffusion in oxide depending on hydrogen related species dynamics inn both oxide and nitride.

Non dopant species diffusion in multi-materials stack has also an impact on devices electrical behaviour. Thus, lanthanum diffusion in high-k stacks was investigated and a lanthanum diffusion model in  $\text{HfSiON}$  high-k was developed for the first time. Our results showed a thermally activated diffusion mechanism with a diffusion time saturation, that is assumed to be due to the formation of lanthanum silicates. These silicates are supposed to be responsible for electrical characteristics shifts through the formation of dipoles.

With the exception of lanthanum diffusion in high-k stacks, all the process models developed during the PhD were tested on real CMOS devices. Advanced MOS transistors were first investigated. Boron dose loss model effect on bulk pMOS transistors was evaluated with a noticeable effect of the model on the transistors electrical characteristics. LBICs model was then tested on FDSOI pMOS transistors and allowed to reproduce experimental data where boron dose and spike activation anneal were varied. TriGate n-type MOS transistors simulations showed that higher electrical performances can be obtained in such 3D devices when extension doping is high and conformal as in PIII.

The models were then evaluated on CMOS image sensors. Boron dose loss in the TG spacer region of frontside pixels with planar photodiode was studied showing a clear impact on dark current and lag characteristics. Assuming equal traps characteristics at the different interfaces, similar saturation charge and dark current were obtained for the frontside pixels when using PIII or beam-line implants. Boron dose loss simulations in the ONO stack of BSI pixels with vertical photodiode showed a modification of QE characteristics mainly for the blue pixel at low wavelengths. We also demonstrated that LTA simulations can also be carried out in BSI pixels thanks to a LTA model developed by our partners in the frame of the ATEMOM project.

The process models developed in the PhD allowed to improve TCAD predictability for advanced CMOS devices and mainly image sensors. Yet, several open questions remain:

- In heavy doped silicon, apparent uphill boron diffusion against concentration gradient was observed in several literature results. Modelling this uphill diffusion effect is a big challenge both from the physical side (ie. to understand the origin of the phenomenon), but also from the numerical side due to convergence issues.
- Concerning PIII, conformal doping is simulated using a simple geometric approach in TCAD. Such an approach is not predictive enough and additional experimental and theoretical investigations are needed in order to correctly model this effect.
- Only boron dose loss was investigated in this thesis. However, other dopant species such as phosphorus or arsenic may also exhibit out-diffusion in multi-material stacks, with an impact on nMOS transistors or pixels with p-type photodiode.
- Lanthanum diffusion was investigated in a thick high-k layer during the PhD. However, different diffusion mechanisms may occur for thin layers with an impact on the electrical behaviour of nMOS transistor.
- A difficult challenge in CMOS image sensors is dark current simulations where several volume and surface defects may contribute to this parasitic signal. In addition, with pixels size reduction, the photodiode distance to the different interfaces is reduced, therefore increasing the interfaces contribution to dark current. The main difficulty is the design of dedicated experiments to separately investigate the different contributions, and also understand the variation of a given contribution with process conditions.

From this conclusion and the different remaining challenges, it is clear that the time is long past when TCAD process and device modelling development could mainly focus on the physical mechanisms occurring in the “bulk” silicon only. Devices are smaller and the interfaces are closer to the active regions, increasing the interactions between silicon and neighbouring materials. For the next years, we therefore believe that TCAD modelling can no longer be predictive without taking into account this multi-materials aspect.