SiC Nanowires : from growth to related devices

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▶ To cite this version:

Jihoon Choi. SiC Nanowires : from growth to related devices. Other. Université de Grenoble, 2013. English. NNT : 2013GRENT028 . tel-01061784

HAL Id: tel-01061784

https://theses.hal.science/tel-01061784

Submitted on 8 Sep 2014

UNIVERSITÉ DE GRENOBLE

THÈSE

Pour obtenir le grade de

DOCTEUR DE L'UNIVERSITÉ DE GRENOBLE

Spécialité : **NANO ELECTRONIQUE ET NANO TECHNOLOGIES (NENT)**

Arrêté ministériel : 7 août 2006

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dans **l'École Doctorale EEATS**

Silicon carbide nanowires: from fabrication to related devices

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Silicon carbide nanowires:
from fabrication to related devices

by Jihoon Choi

Ph.D thesis prepared at IMEP-LAHC and LTM laboratories, Université de Grenoble, France
under supervision of Edwige Bano and Laurence Latu-Romain.

Acknowledgements

Firstly, I would like to thank my two advisors, Edwige Bano and Laurence Latu-Romain for accepting me as a Ph.D. student and for their efforts in building up the research activities at Grenoble University. Without their encouragement and wisdom, it would have been so much harder to conduct this work. I have greatly appreciated to Marco Pala and Alessandro Cresti in IMEP-LAHC for providing me the initial numerical code for the simulation of FET and supervising my simulation results. Also, I would like to thank Laurent Montes for valuable discussions.

During my Ph.D study, I have collaborated with several famous researchers, Giovanni Attolini (IMEM-CNR, Italy), Anne Henry (Linköping University, Sweden), Didier Chaussende (LMGP, France), Marc Portail (CHREA, France), Dominique Planson (Ampere, INSA Lyon, France), Won-Jae Lee (Dong-Eui University, Korea) and Sang-Mo Koo (Kwang-won University, Korea). They have supported me overwhelmingly such as providing expensive SiC nanowires and SiC wafers and/or epilayers.

It has also been a pleasure to interact with my colleagues at the LTM laboratory: Maelig Ollivier, Bassem Salem, Thierry Chevolleau, Thierry Luciani, Florian Dhalluin, Guillaume Rosaz, Martin Kogelschatz, Camille Petit-Etienne, and Thierry Baron. Specifically, I have worked closely and productively with Florian Dhalluin on the etching of SiC nanostructures. I know I could not have all achieved without him.

The whole process for fabricating the nanowire device was performed in the Plateforme Technologique Amont (PTA), Grenoble. I would like to thank the technical staffs: Thibault Haccart, Jean-Luc Thomassin, Delphine Constantin, Frederic Gustavo, Christophe Lemonias and Marlene Terrier. And I would like to thank my former and current office mate in IMEP-LAHC: Louis Gerrer, William Van Den Daele, Amer El Hajj Diab, Louis Fradetal and Sharon Hsu.

I have very much appreciated Konstantinos Zekentes for his detailed reading of my thesis. I have benefited a lot from his comments and discussions. I would also like to thank my committee members; Dr. Giovanni Attolini, Dr. Konstantinos Zekentes, Dr. Michel Pons and Dr. Mikhael Bechelany, for their time and knowledge.

Life at Grenoble is unforgettable. It was very enjoyable working with my bright fellow students. I really want to send my thanks and best wishes to them: Doyoung Jang, Jeawoo Lee, Daeyoung Jeon, Sojung Park, Sungjae Jang, Minkyu Joo, Jungkyu Chae, Hee-eun Kho and Misang Ryu. Finally, I owe more than words to thank my family. This work is dedicated to them.

Citations to published work

International Journals

- J. H. Choi, L. Latu-Romain, E. Bano, F. Dhalluin, T. Chevolleau and T. *Baron, "Fabrication of SiC* nanopillars by inductively coupled SF_6/O_2 *plasma etching", J. Phys. D: Appl. Phys.* Vol. 45 (2012) p. 235204.
- J. H. Choi, L. Latu-Romain, E. Bano, A. Henry, W. J. Lee, T. Chevolleau, T. *Baron,* "Comparative study on dry etching of α- and β-SiC nano-pillars*",* Materials Letters Vol. 87 (2012) pp. 9–12.

Publications in Refereed Conference Proceedings

- J. H. Choi, L. Latu-Romain, F. Dhalluin, T. Chevolleau, B. Salem, T. Baron, Didier Chaussende, and E. *Bano, "Fabrication of SiC* nanopillars by inductively coupled SF_6/O_2 *plasma", Materials Science Forum* Vol. 711 (2012) pp 66-69.
- J. H. Choi, L. Latu-*Romain, T. Baron, T. Chevolleau and E. Bano, "Hexagonal faceted SiC nanopillars* fabricated by inductively coupled SF_6/O_2 *plasma method"*, Materials Science Forum Vols. 717-720 (2012) pp 893-896.
- J. H. Choi, M. Pala, L. Latu-*Romain, and E. Bano, "Theoretical study of thermoelectric properties of SiC nanowires",* Materials Science Forum Vols. 717-720 (2012) pp 561-564.
- J. H. Choi, L. Latu-*Romain, E. Bano, A. Henry, W. J. Lee, T. Chevolleau, T. Baron, "Comparative study on dry etching of* α- and β-SiC nano-*pillars", will be published in Materials Science Forum, presented in* ICSCRM 2012 (International Conference on Silicon Carbide and Related Materials, held in St Petersburg, September 2012).

Abbreviations

AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
BTE	Boltzmann Transport Equation
CNT	Carbon NanoTubes
CVD	Chemical Vapor Deposition
CMOS	Complementary Metal-Oxide- Semiconductor
DI	De-Ionized
DOS	Density Of States
EBL	E-Beam Lithography
EDX	Energy-Dispersive X-ray spectroscopy,
EELS	Electron Energy Loss Spectroscopy
FET	Field Effect Transistor
GAA	Gate-All Around
HRTEM	High Resolution Transmission Electron Microscopy
ICP	Inductively Coupled Plasma
IPA	IsoPropyl Alcohol
MOSFET	Metal-Oxide- Semiconductor Field-Effect Transistor
MIBK	Methyl-IsoButyl-Ketone
NEMD	Non Equilibrium Molecular Dynamics
MC	Monte Carlo
MD	Molecular Dynamics
MEMS	MicroElectroMechanical Systems
NEMS	NanoElectroMechanical System
NP	NanoPillar
NW	NanoWire
NEGF	Non Equilibrium Green's Function
PF	Power Factor
PMMA	Poly-MethylMethAcrylate
PSD	Power Density Spectrum
PR	Photo Resist
PVT	Physical Vapor Transport
QD	Quantum Dot
RIE	Reactive-Ion Etching
rms	Root Mean Square
rpm	Revolutions Per Minute
SEM	Scanning Electron Microscopy
Si	Silicon
SiC	Silicon carbide
SOI	Silicon on Insulator
S/D	Source/Drain
SR	Surface Roughness
TC	Thermal conductance
TCR	Thermal Contact Resistance
TEM	Transmission Electron Microscopy

VLS	Vapor–Liquid–Solid
VPE	Vapor Phase Epitaxy
VS	Vapor–Solid
VS-FET	Vertical Surround-gate Field-Effect Transistor
XRD	X-Ray Diffraction
1D, 2D and 3D	One-, Two and Three-Dimension

Physical Constants

Symbol	Name	Value
q	Electronic charge	1.602×10^{-19} C
ε_o	Permittivity of vacuum	8.854×10^{-14} F/cm
k_B	Boltzmann's constant	1.381×10^{-23} J/K 8.617×10^{-5} eV/K
h	Planck's constant	6.625×10^{-34} J s 4.135×10^{-15} eV s
ε_r	Relative dielectric constant	$SiO_2 = 3.9$

Parameters in the equation (or in the text)

Symbol	Name	Unit
C_d	Depletion layer capacitance	[F]
C_{ox}	Gate coupling capacitance	[F]
D_{it}	Electrically active interface states	[cm^{-2}]
E	Electric field	[$V \cdot \mu m^{-1}$]
E_F	Fermi energy level	eV
E_{ON}	Electron emission turn-on field	[$V \cdot \mu m^{-1}$]
E_{Th}	Electron emission threshold field	[$V \cdot \mu m^{-1}$]
$f_{S/D}$	Fermi function at the Source/Drain	
G	Electrical conductance	[Ω^{-1}] or [S]
$G^<$, $G^>$	Lesser than or greater than Green's function	
G^A, G^R	advanced or retarded Green's function	
g	degeneration coefficient (4 for Si, 2 for SiC)	
g_m	Transconductance	[Ω^{-1}] or [S]
h	Thickness of oxide	[nm]
H	Hamiltonian	

I	Current	[A]
L	Channel length	[nm]
L_m	Correlation length of surface roughness	[nm]
m^* or m_o	Effective mass of a carrier	
m_l	Longitudinal effective mass	
m_t	Transverse effective mass	
N	Carrier concentration	[cm^{-3}]
N_{1D}, N_{3D}	Linear or volume charge density	[cm^{-1}] or [cm^{-3}]
R	Radius of nanowire	[nm]
r	Diameter of nanowire	[nm]
r=(x, y, z)	3D position vector	
S	Seekbeck coefficient	[V·K^{-1}]
T	Temperature	[K]
T(E)	Transmission coefficient	
Usc	Self-consistent potential energy	[eV]
V	Voltage	[V]
Z	Material's thermoelectric properties	[K^{-1}]
β	Field enhancement factor	
Δm	Root mean square of surface roughness	[nm]
$\eta+$	Infinitesimal positive value,	
κ	Thermal conductance	[W·K^{-1}]
κ_e, κ_{ph}	Electrical or phonon thermal conductance	[W·K^{-1}]
$\mu_{S/D}$	Chemical potential at the Source/Drain	
μ_e, μ_h	Electron or Hole mobility	[cm^2·V^{-1}s^{-1}]
ρ	Resistivity	[Ω·cm]
$\rho(r)$	Charge distribution	
$\Sigma_{S/D}$	Self-energy matrices at the Source/Drain	
φ	Electrostatic potential	[V]
ψ	Electron wave function	
v_d	Drift velocity	[cm·s^{-1}]
ω	Phonon frequency	[cm^{-1}]

Abstract

Low dimensional semiconductor nanostructures (such as nanowires (NWs), nanorods and nanotubes) have become the focus of intensive research for exploring new emergent phenomena at the nanoscale and probing their possible use in future electronics. Among these semiconductor NWs, Silicon Carbide (SiC) has very unique properties, such as wide bandgap, excellent thermal conductivity, high breakdown electric field, chemical and physical stability, high electron mobility and biocompatibility. These factors makes SiC a long standing candidate material to replace silicon in specific electronic device applications operating in extreme conditions or/and harsh environments.

SiC nanostructures have been studied extensively and intensively over the last decade not only for their fabrication and characterization, but also for their diverse applications. I have outlined the growth of SiC nanostructures based on different growth methods, a noteworthy feature of their characteristic properties and potential applications in the chapter one.

As-grown SiC NWs fabricated by bottom-up method present a high density of structural defects, such as stacking faults. This kind of defect is one of the factors which lead to poor electrical performance (such as weak gate effect and low mobility) of the related devices. Therefore, it is required to develop a high quality of SiC nanostructures with low density of the structural defects using an alternative method, such as top-down process.

Main objectives of this thesis are divided into three main parts.

The first part of the thesis (Chapter two), we present the simulation results of the electrical transport and thermoelectric properties of SiC and Si NWs. I have investigated the thermoelectric enhancement by studying the complex interplay of the size of NWs, temperature and surface roughness. Our simulation results show that the ZT of Si terminated SiC NW (2.05×2.05 nm^2) reaches a maximum value of 1.04 at 600K. In case of Si NW, the ZT of Si NW for the cross section (3×3 nm^2) with the SR (Δ_m= 0.2 nm) is 0.7, which is comparable to the highest experimental ZT value of Si NW (0.6).

The second part of the thesis (Chapter there) is devoted to the fabrication of high quality SiC nanostructures with controlled doping level. I have developed a top-down fabrication technique for high quality nanometer scale SiC nanopillars (NPs) using inductively coupled plasma etching. The etching behavior of SiC NPs has also been studied depending on polytypes and crystallographic orientations.

Under the optimal etching conditions using a large circular mask pattern with 370 nm diameter, the obtained 4H-SiC nanopillars exhibit high anisotropy features (6.4) with a large etch depth (>7μm). A hexagonal, rhombus and triangle based pillar structures have been obtained using α-SiC (0001), 3C-SiC (001) and 3C-SiC (111) substrates, respectively. The length of these pillars below 100 nm in diameter is around 1.0 μm, which is long enough to reveal the electrical property of SiC nano-FETs.

The last part of the thesis (Chapter four) is dedicated to the design and the electrical characterization of SiC nanodevices. To investigate the electrical properties of SiC nanostructures, two different kinds of SiC nanoFETs (SiC NWFET and SiC NPFET) have been fabricated by using SiC NWs and SiC NPs prepared via bottom-up method and top-down methods, respectively.

In case of SiC NWFET, low resistivity ohmic contacts (378 kΩ) have been obtained after the annealing at 650 °C. Ni silicide intrusion into the SiC NW channel has been observed the annealing at 700 °C. This temperature is compared to one of other group IV materials. In case of SiC NPFET, two different types of NPFET (3C-SiC (001) and 4H-SiC (0001)) have been fabricated using our SiC nanopillars, obtained by top-down approach. The estimated values of the field-effect carrier mobility are 411.6 $cm^2\cdot V^{-1}s^{-1}$ for 3C-SiC (001) NPFET (#2) and 95.2 $cm^2\cdot V^{-1}s^{-1}$ for 4H-SiC (0001) NPFET, which is higher than the best values reported in the literature (15.9 $cm^2\cdot V^{-1}s^{-1}$).

TABLE OF CONTENTS

Introduction

The main focus of this Ph.D. thesis is to develop new methodologies and design strategies for the fabrication of SiC nanostructures and SiC nanodevices.

This thesis is organized in the following manner.

- ✓ In the first chapter of this thesis, I briefly introduces the properties of bulk SiC (section 1.2), including the polytypism and defects, because the basic properties of NWs are originally based on their parent materials. And then, the current research activities is introduced to synthesize one dimensional semiconductor nanowires by covering different methods (either top-down or bottom-up techniques) in section 1.3. I summarize the current state of the research on the properties (section 1.4) and the related applications (section 1.5) of SiC nanostructure.

- ✓ Chapter two presents the device numerical simulations of SiC (and Si) nanowire based on the self-consistent solution of the Schrödinger and Poisson equations within the NEGF formalism. The electrical transport in SiC (and Si) NWFET has been investigated in SiC (and Si) NWFET (section 2.2), including the thermoelectric properties (section 2.3).

- ✓ Chapter three contains the details of process parameters and relevant results for the fabrication of one dimensional SiC nanostructures by top-down approach using ICP etching. In addition, the dependency of polytypes and crystallographic orientations are discussed, which are responsible to control the morphology of etched SiC nanostructures. It is demonstrated that SiC nanopillars can be successfully fabricated.

- ✓ In the Chapter four, two different kinds of SiC nanoFET (SiC NWFET and SiC NPFET) have been developed to reveal the electrical property of SiC nanostructures. SiC NWFET is fabricated by using SiC NWs prepared via bottom-up method. SiC NPFET is fabricated by using SiC nanopillar demonstrated in the chapter 3. The detail device fabrication process and the electrical characterization are presented in this chapter.

- ✓ Finally, the summary of our findings is given in the conclusion together with a discussion of possible future directions.

Chapter 1. Silicon carbide nanowires bibliography: growth, properties and applications

1.1 Introduction

Nanostructured materials are a new class of materials, having dimensions in the 1 - 100 nm range. Over the past decade, one-dimensional (1D) semiconductor nanomaterials have formed a promising category for their exclusive electrical, mechanical and optical properties, and potential applications in nanotechnology, such as nanoelectronics [1], nanooptics [2] and nanosensors [3]. The novel properties of 1D nanostructures are caused by their nanoscale dimension, morphology and crystal structure. In the literature, a lot of different names of 1D nanostructures can be found to refer the differences in shape and dimensions, like nanowires, nanotubes, nanowhiskers and nanorods, as summarized in Table 1.1.

Table 1.1 Nomenclature for various one-dimensional nanostructures.

	Diameter (nm)	Length (μm)	Cross section	Ref.
Nanowires	1 – 100	1-100	Cylinder	[4]
Nanotubes	1 – 100	1-100	Hollow	[5]
Nanorods	1 – 100	< 2	Cylinder	[6]
Nanowhiskers	≥ 1000	10 - 1000	Cylinder	[7]
Nanocables	1 – 100	1-100	Core-shell	[8]

Among the 1D nanostructures, nanowires (NWs) have two quantum confined directions with a diameter between 1 and 100 nm, while still leaving one unconfined direction with a length of several microns. Due to sufficiently small dimension of NWs, it has also been proposed as promising solution for the overcoming down-scaling limitations of CMOS devices. In addition, NWs are expected to exhibit significantly different electrical properties from their bulk counterparts, such as ballistic transport, owing to quantum confinement effects along the transverse direction. The quantum confinement effect exists when the diameter (d) is such that $d < 2R_{Bohr}$, where R_{Bohr} is the Bohr radius. Wu et al. [9] estimated the Bohr radius of 3C-SiC to be 2.7 nm, so SiC nanostructures with sizes less than 5.4 nm have an obvious quantum confinement effect and quasi-ballistic transport. The other prominent feature of NWs is their higher surface-to-volume ratio than bulk counterpart, which provides higher sensitivity to the surrounding environment. Therefore, NWs are excellent candidates for sensing applications due to more reaction area per volume. These properties of NWs have stimulated new device design concept for a variety of applications in electronics [1], photonics [2] and sensors [3].

NWs can be synthesized either by a top-down or by a bottom-up approach. Much effort has been devoted to fabricate high-quality semiconductor NWs based on different techniques. There has been significant progress made in the area of the fabrication of NWs, such as dimension and morphology control, chemical composition and alignments, etc.

First, I'll briefly introduce the properties of bulk SiC in section 1.2, including the polytypism and defects, because the basic properties of NWs are originally based on their parent materials. Then I'll describe recent progress and advances in the growth of NWs in section 1.3. In the section 1.4, I'll review the important properties of the SiC NWs, in particular, electrical, mechanical, and thermal properties. Finally, I'll explore and address possible applications based on SiC NWs in section 1.5, including the simulation and the experimental results of the literature.

1.2 Introduction about bulk SiC

SiC is a IV–IV compound semiconductor. The crystalline structure of SiC is composed of strong tetrahedral SP^{3*} bonds of carbon (C) and silicon (Si) atoms. SiC has been considered as a long standing candidate material to replace silicon in specific electronic device applications, which required high temperature, high power, high frequency and extreme environments.

The technology of single crystalline SiC growth has been developed over the past decades and has shown commercial availability of SiC substrates of ever-increasing diameter and quality. Most successful method for the growth of large SiC crystals of high quality is the physical vapor transport (PVT) method [10], also known as seeded sublimation growth.

Currently, commercial hexagonal 4H- and 6H-SiC polytypes substrate are now available at diameters up to 150 mm. It has opened the way for the fabrication of electronic devices with steadily improving performances, but the price of substrate is still relatively expensive. Increasing substrate diameter while reducing the defects is crucial for reducing the cost of SiC materials and SiC based devices. An optimistic point is that the progress in commercial growth of SiC has occurred much quicker than Si and GaAs. SiC substrates of high quality and cost-effective with ever-increasing diameter will be available within the near future.

1.2.1 Polytypism in SiC

SiC exists in hundreds of different polytypes, which have the same chemical composition but different crystalline structures. The polytypes of SiC is defined by the combination of the number of stacking layers and the type of crystal symmetry in an unit cell. The popular polytypes are 3C-, 4H- and 6H-SiC, as presented in Figure 1.1. Small crystal inclusions of 2H-, 15R-SiC can be found on 4H and 6H wafers. H, C, and R stand for hexagonal, cubic, and rhombohedral, respectively.

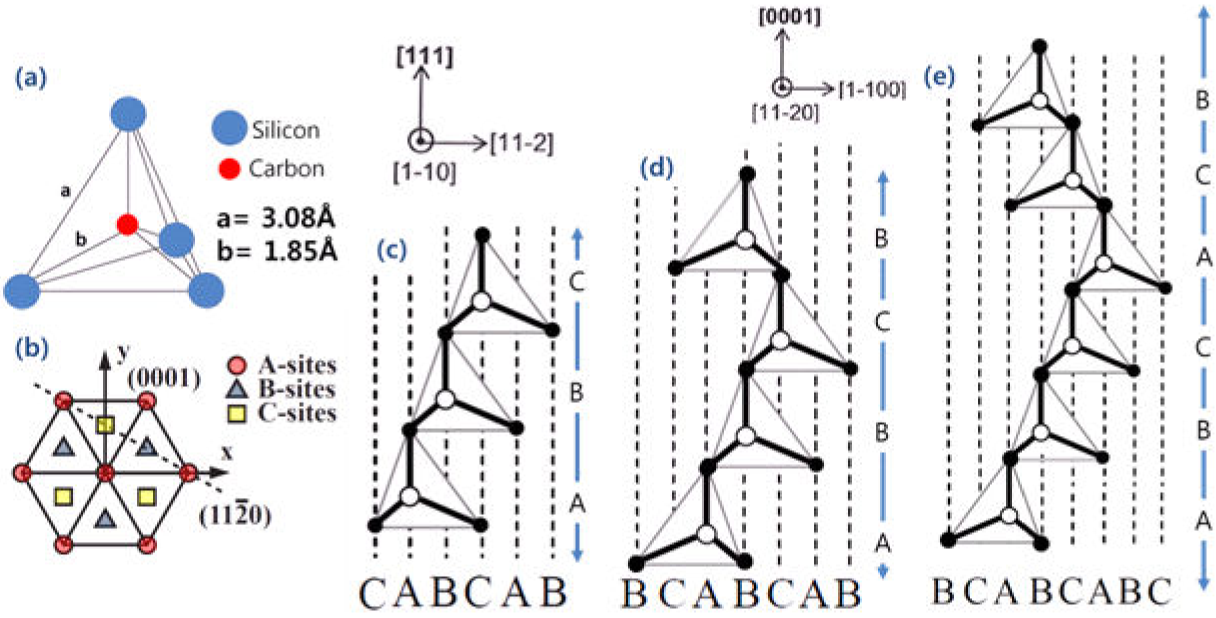

Figure 1.1 (a) Elementary Si-C tetrahedron, (b) projection of the different positions of the atoms, Stacking sequences for different SiC polytypes, (c) 3C-SiC, (d) 4H-SiC and (e) 6H-SiC, respectively [10].

The structure of SiC (the [0001] direction) is the tetrahedrally bonded carbon atoms linked to three Si atoms within the bilayer (see Figure 1.1(a)). Each SiC bilayer can be oriented into only three possible positions (A-, B- and C- cites), as shown in Figure 1.1(b), with respect to the lattice while the tetrahedral bonding is maintained. The stacking sequence of 3C-SiC is ABCABC in Figure 1.1(c) 4H-SiC is composed of an equal number of cubic and hexagonal structures with stacking sequences of ABCB (the hexagonality is 50%) in Figure 1.1(d). 6H-SiC consists of two-thirds of cubic bonds and one-third of hexagonal bonds with stacking sequences of ABCACB (the hexagonality is 33%) in Figure 1.1(e). Generally, 4H- and 6H-SiC are called α-SiC, 3C-SiC is referred to as β-SiC because it is the only cubic SiC crystalline structure, and corresponds to the zinc-blende structure. As is obvious from the definition, cubic structure of 3C-SiC shows zero hexagonality. The band energy gap of SiC polytypes tends to increase with increasing the degree of hexagonality.

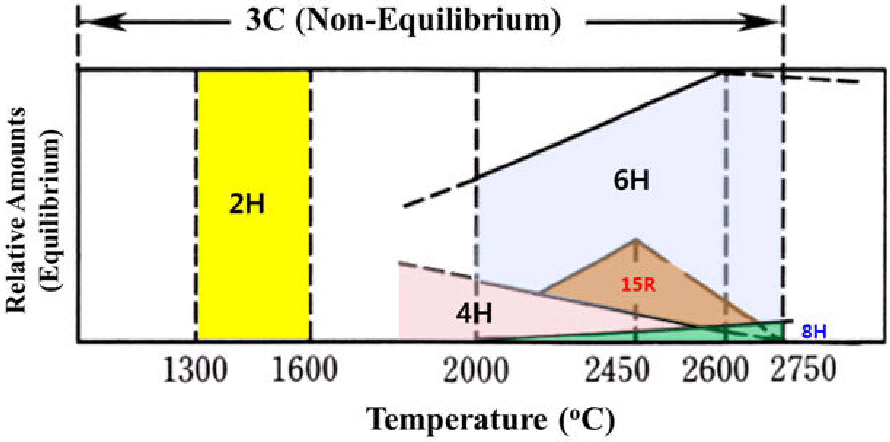

Figure 1.2 Stability diagrams of SiC polytypes [11].

The stability of the different polytypes is mainly a function of temperature and supersaturation as shown in Figure 1.2 according to Knippenberg (1963) [11]. The cubic form of SiC (3C-SiC) is believed to be more stable than the hexagonal structure (4H- and 6H-SiC) at low temperature (below 2000 °C).

▣ 4H- and 6H- SiC

Except for the cubic polytype of SiC (3C-SiC), other polytypes of SiC are anisotropic. In particular, hexagonal structure shows a clear distinction between the different directions in the lattice, as illustrated in Figure 1.3. Therefore, electrical properties can vary not only between the polytypes, but also with the crystal orientation of polytypes.

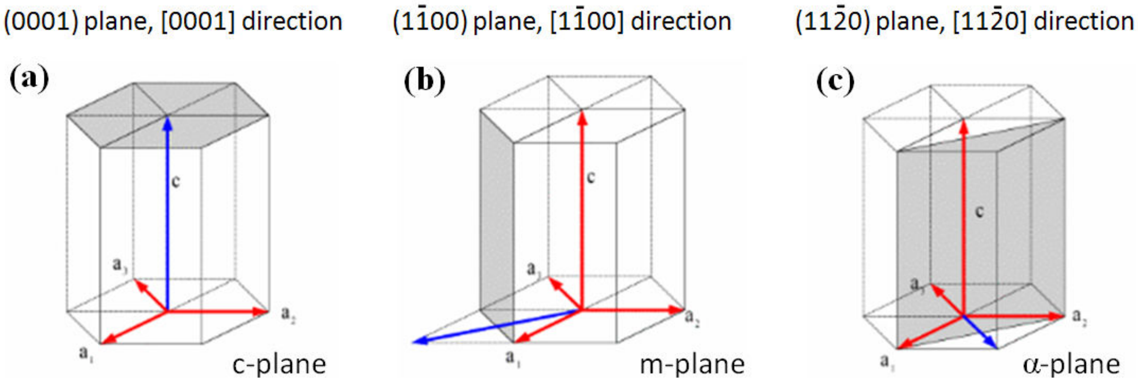

Figure 1.3 Hexagonal lattices of (a) c-, (b) m- and (c) α-planes on 4H- or 6H-SiC substrates.

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The direction parallel to the central axis in the hexagonal structure is called the crystal axis, or c-axis (blue arrow in Figure 1.3a). In commercially available wafer, the c-axis noted as the [0001] direction is either perpendicular the substrate which is a (0001) plane or slightly disoriented of about 3 to 8° to be able to favor, further and homo-epitaxy by the step controlled growth [12].

▣ 3C-SiC

3C-SiC is the only crystalline structure with isotropic morphology. Therefore, the electrical properties are same in different directions. The advantage of 3C-SiC is that it is able to be grown on Si substrates, therefore it can provide the large size, low price and the possibility in the future of integration of 3C-SiC devices with Si technology. However, it doesn't guarantee high quality of polytypes due to the large lattice constant (~20 %) and thermal coefficient (~ 8%) mismatch between Si and SiC interface. That is why the best crystalline quality of 3C-SiC is obtained on hexagonal SiC seeds [13, 14]. In comparison with 4H-SiC, the 3C-SiC shows lower hole mobility, smaller band-gap and larger electron mobility.

1.2.2 Properties of bulk SiC

SiC is a material of great interest because of its intrinsic physical and chemical properties in comparison with other semiconductors, as listed in Table 1.2.

Table 1.2 Comparison of SiC and other semiconductors [15].

	Si	**GaAs**	**3C-SiC**	**4H-SiC**	**6H-SiC**	**GaN**	**Diamond**
E_g (eV)	1.12	1.43	2.4	3.2	3.0	3.3	5.5
Band gap type (Direct [D] or indirect [I])	I	D	I	I	I	D	I
Electron mobility (μ_e) ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	1300	8500	1000	947 ⊥c 1141 ∥c	415 ⊥c 87 ∥c	400	2200
Saturation velocity(v_{sat}) ($10^7 cm \cdot s^{-1}$)	1.0	1.0	2.5	2.0	2.0	2.0	2.7
Hole mobility (μ_h) ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	480	400	40	120	80	30	1600
Thermal conductance ($W \cdot cm^{-1} K^{-1}$)	1.5	0.5	3.5–5.0	3.5-5.0	3.5-5.0	1.3	20.0
Critical field (E_c) ($MV \cdot cm^{-1}$)	0.25	0.3	2.0	2.2	2.5	3.0	5.0
Density ($g \cdot cm^{-3}$)	2.3	5.3	3.2	3.2	3.2	6.1	3.5

(⊥c: perpendicular to the c-plane, ∥c: parallel to c-plane)

▣ Wide bandgap

The wide band gap of SiC (2.3 - 3.3 eV) opens up for SiC devices to be used at very high temperatures (in excess of 600 °C), because the thermal generation of electron-hole pair is low. Thanks to its wide bandgap, SiC material shows a higher than 10^{12} cm^{-3} intrinsic carrier concentration at over 1000 °C.

▣ High breakdown field and high saturated electron drift velocity

Thanks to its wide band gap, SiC also possesses a very high breakdown field (3 - 5 $MV\cdot cm^{-1}$). The breakdown field of SiC is about ten times higher than the one of Si. The high electric breakdown field allows the fabrication of SiC devices with a theoretical power efficiency two orders of magnitude better than Si devices. High breakdown electric field of SiC enables to fabricate the device with small size, low-resistive and high-power.

The combination of high breakdown field and high saturated electron drift velocity values allowed also publication of high performance microwave PIN diodes [16].

▣ High thermal conductivity

SiC has nearly three times as high thermal conductivity (350 - 490 $W\cdot m^{-1}K^{-1}$) compared to Si and 7 times higher than GaAs, and is superior to Cu. Therefore, SiC based devices operate at extremely high power levels, since it can dissipate heat more efficiently. If this property is coupled with low thermal expansion, SiC devices could be used for specific applications, which require thermal shock resistant environment.

Due to these properties of SiC mentioned above, SiC is expected to operate with the most advantageous benefits over conventional Si and GaAs electronics in high-power applications.

▣ Chemical inertness

SiC has very high etch resistance in most acid and alkaline solutions due to its chemical inertness. Therefore, SiC has attracted much attention as a possible material for microelectromechanical systems (MEMS) operating in harsh environments (aggressive and corrosive media). In addition, the native oxide is silicon dioxide, which makes SiC directly compatible with the usual Si technology.

▣ Biocompatibility

SiC is one of the semiconducting materials that possess an excellent biocompatibility and great sensing potentiality compared to Si, which is widely used for fabrication of biological systems. According to our knowledge, several reports are found in the literature, which investigates crystalline SiC biocompatibility [17, 18]. Colett and Saddow et al. [17] have investigated the biocompatibility of SiC polytypes compare with Si by culturing mammalian cells directly on substrates. SiC in all its phases shows better proliferation than Si for all mammalian cell lines studied. There are no significant differences of the cell proliferation on different SiC polytypes. They suggest that two possible explanations could be the basis of the enhanced cell proliferation observed on SiC substrates. From the contact angle images, SiC surfaces are more hydrophilic than Si surfaces and mammalian cells preferentially adhere to hydrophilic surfaces.

It is known that surfaces with a normal electrochemical potential close to the one of the cells are more biocompatible [17]. Since the electrochemical potential of carbon is comparable to that of living tissue, the higher carbon concentration of the SiC surfaces most likely justifies SiC greater biocompatibility. The results of this biocompatibility study show that SiC is indeed a better promising material for bio-applications than Si, whose cytotoxicity has been reported by several studies [17]. These results open up exciting perspectives for in a variety of medical applications (e.g. implant coating material [18]) and bio-electronic devices.

1.2.3 Defects in SiC

As any real crystal, the SiC crystals and epilayer also suffer from defects. The defect density in SiC is still high compared with Si. Defects have been a major limiting factor for SiC based applications because they are often detrimental to the behavior of electrical devices. It is therefore critical to understand the impact of various kinds of defects. In this section, I'll briefly introduce the defects related with SiC materials.

▣ Structural defects in SiC bulk and epilayer

The most severe defect in the crystal and epilayer structure of hexagonal SiC is called micropipe, which looks like wormholes with micro-diameter-scale. The micropipes decreased the breakdown voltage and increased the leakage currents in high-field devices. The density of micropipes of commercial available SiC wafer was scaled down to around zero per cm^2. Closed-core axial screw dislocation defects are similar in structure and strain properties to micropipes, but the core is solid instead of a hollow void due to smaller Burgers vector [19]. Overall dislocation densities of commercial available SiC wafer have been reduced by up to low 10^4 cm^{-2} [20].

▣ Defects in SiC nanostructures

Most SiC NWs are the cubic zinc-blend structure (β-SiC) oriented along the thermodynamically preferred [111] direction because of the low growth temperature (1000 ^oC) [11]. The dominant defects in SiC nanostructures, are the staking faults. A very small energy is needed to create a stacking faults (SFs) in SiC [21]. Theoretically, it has even been calculated the SFs energy in cubic SiC should be negative [22].That is why SFs are easily created.

As-prepared SiC NWs by bottom-up methods show a high density of SFs perpendicular to the growth direction. SFs in low dimensional structures are generally thought to originate from release of thermal stress during the growth process. The imperfections of 1D SiC nanostructures strongly influence the performance of SiC NWs based devices, but it remains less explored.

In summary, I briefly presented certain kind of defects with SiC materials and studied root causes of each defect, because the defects have a strong influence on the performance of SiC devices. The removal of defects is still a main challenge for SiC material itself as well as related applications. We expect that the density of defects will be dramatically reduced in the near future with improved crystal growth processes.

1.3 SiC nanowires growth

1.3.1 Introduction: the fabrication methods of nanowires

There are two different approaches to the production of 1D nanostructures: top-down and bottom-up technologies. These terms were first introduced in the field of nanotechnology by the Foresight Institute in 1989.

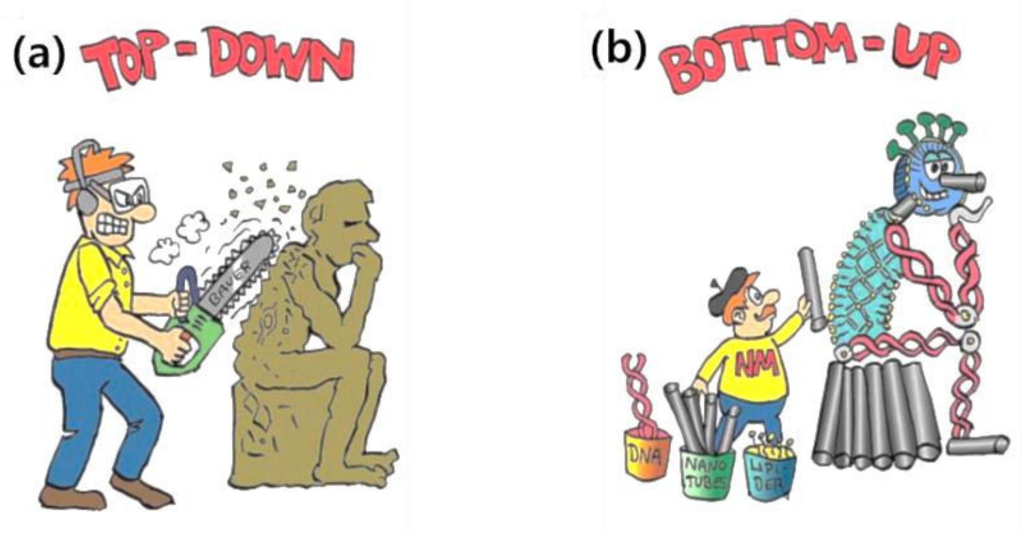

Figure 1.4 Illustrations of (a) top-down and (b) bottom-up approach [23].

Top-down approach literally means that it transforms a bulk material into several structures until reaching the desired sizes. Whereas, a bottom-up approach assemble small particles, such as constituent atoms, into a larger structure, as shown in Figure 1.4.

▣ Top-down methods

Usually, the top-down approach involves the lithography and etching processes to fabricate NWs with their integrated systems on the substrate. This method can obtain highly ordered NWs with precisely controlled dimensions and location. One of the big advantages is also compatible with well-developed complementary metal-oxide-semiconductor (CMOS) fabrication technology. Planarly and vertically etched NWs can be obtained using with line and dot patterns via top-down processing, respectively.

Figure 1.5 shows a planarly and a vertically etched high density of Si NWs arrays fabricated by top-down processing. Wang et al. [24] have fabricated high density of Si NWs array with top-down approach by pattering on silicon-on-insulator (SOI) substrates (34 nm Si <100> films on 250 nm oxide). The dimensions of Si NWs are 17 nm wide and 34 nm thickness with a pitch of 34 nm (Figure 1.5a). They also have modulated the doping levels of boron (p-type) and phosphorous (n-type) by optimizing the diffusion temperatures.

Henry et al. [25] have demonstrated vertically etched silicon nanopillars with the high-aspect-ratio using alumina dot mask patterns. Figure 1.5b shows the SEM images of alternating rows of 40 and 65 nm diameter Si naonopillars with a height of 780 nm.

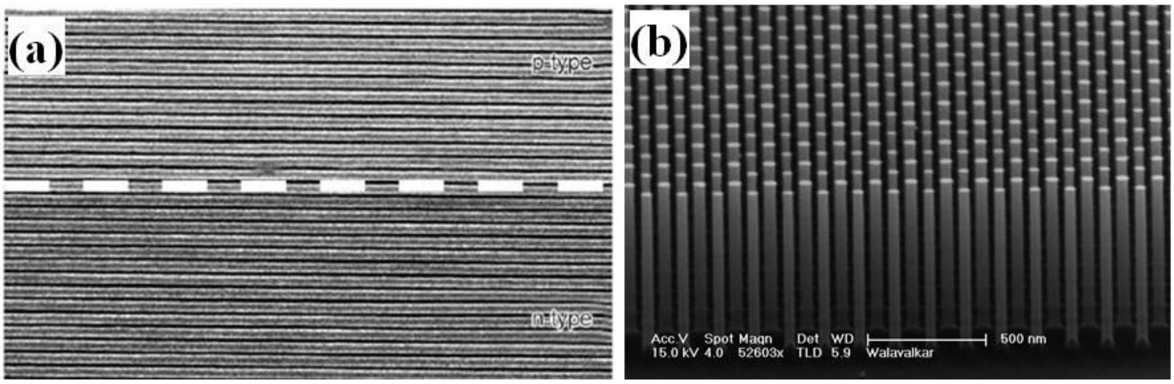

Figure 1.5 (a) Planarly *etched Si NW's array with the* controlled doping profile (diameter = 17 nm, pitch distance = 34 nm) [24], *(b) vertically etched Si NW's* (diameter = 40, 65 nm, height = 780 nm) [25].

Although the top-down approach has been successful carried out for the fabrication of nanostructures, this approach has some drawbacks. This approach is complicated, time-consuming, and expensive. And it usually leads to additional roughness on the NWs sidewalls. In addition, it cannot produce nanomaterials with high throughput and the dimension of nanostructures has strongly limited by the resolution of lithography for the patterns.

Bottom-up methods

The bottom-up approach for the growth of nanostructures is more of an assembly process, which is analogous to the way that nature works. The nanostructures are built by stacking the core materials to the growth directions.

As devices approach atomic size, the bottom-up method may prove to be a suitable solution to the technological challenges, which allows smaller geometries than the limitation of lithography resolution. It also provides a convenient way to fabricate a broad range of single-crystalline nano-materials with cost-effective way. In addition, it is providing more flexibility in growing complex heterostructures, such as super lattice [26] and coaxial [8] types.

In spite of several advantages mentioned above, there are still major challenges in the fabrication of nanostructures by the bottom-up methods. For example, as-grown NWs possess the growth induced defects, such as twinning and SFs. Moreover, it is difficult to tailor the exact doping level of NWs. On the other hand, the metallic catalyst that could be used for the growth may diffuse from the tip and get incorporated into the NW as a contaminant and affect the electronic and optical properties of the NWs. In addition, this method may not fully control over the position and orientation of NWs. So, the assembling of NWs into hierarchical architectures are still major challenges for the realization of nanoscale components.

1.3.2 Bottom-up growth mechanisms of nanowires

The growth is in general described by two mechanisms: vapor–liquid–solid (VLS) and vapor–solid (VS).

Vapor Liquid Solid method

The VLS mechanism discovered by Wagner and Ellis in 1964 [7] has proven to be extremely flexible and allows the controlled growth of complex nanostructures. A schematic of VLS mechanism is shown in Figure 1.6. VLS growth is promoted by the presence of a metallic particle droplet usually named as the catalyst to direct the 1D growth. So, VLS growth is often referred to as "catalyst assisted" growth. For Si NWs growth, gold is usually used as catalyst because Au and Si forms an eutectic at a very low temperature The eutectic temperature is at 363 ^{o}C in Figure 1.6(b). The catalyst forms a liquid alloy with the supplied vapor species of the materials to be synthesized. When the liquid alloy is supersaturated, nucleation occurs, and the axial growth proceeds by precipitation at the liquid alloy/solid interface.

The diameter of NWs could be successfully controlled by tailoring the catalyst particle size due to the lateral growth confinement. In addition, VLS growth is providing more flexibility in growing complex heterostructures by modulating the supplied vapor species of the materials.

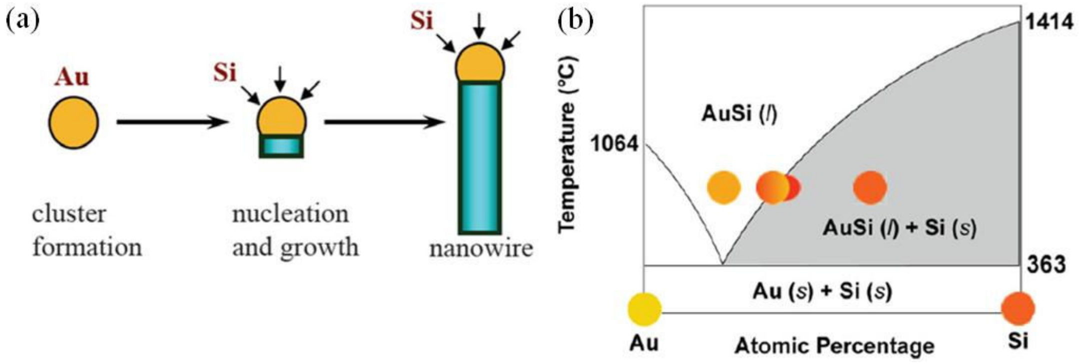

Figure 1.6 (a) Schematic of VLS growth of Si NWs,
(b) binary phase diagram for Au and Si illustrating the thermodynamics of VLS growth [27].

The presence of a metal particle at the tip of the NWs is generally considered as an evidence of the VLS growth. However, in some cases the metal particle may also be consumed during the growth or detached due to interfacial dewetting and thermal strain during the cooling process.

Many efforts have been done to fabricate the SiC NWs via VLS route using various catalysts; NiSi, Fe-Si, Co-Si, Fe and Ni [28, 29] . Typical SiC NWs synthesized by VLS methods show a high density of SFs along the NW (see for examples Figure 1.7a).

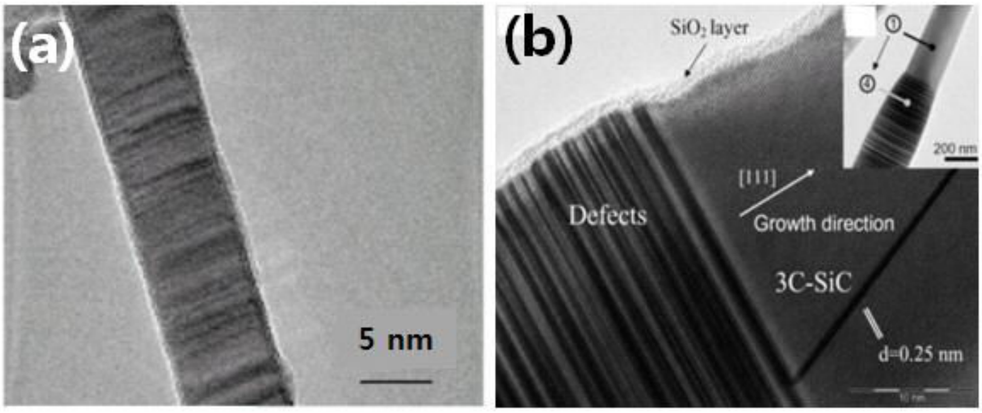

Figure 1.7 TEM images of SiC NWs synthesized by (a) VLS [29] and (b) VS [8], respectively.

▣ Vapor Solid method

VS growth is a spontaneous condensation process of vapor into solid material induced by the decrease in Gibbs free energy from crystallization or the decrease in supersaturation [8]. VS growth is often referred to as “catalyst free” growth. Specifically, the growth mechanism has been associated with the radial thickening and tapering of NWs, due to direct adsorption of gas to the crystallized NWs. Considerable efforts have been done to fabricate SiC NWs by VS methods [8], but SFs are again present (Figure 1.6b).

1.3.3 Fabrication of SiC nanowires

SiC nanostructures, in particular NWs, could be fabricated by the bottom-up and the top-down methods. Common technique for fabrication of SiC NWs is the bottom-up approach. Many efforts have been made to fabricate SiC NWs with controlled diameters and crystallinity by bottom-up approach. The big majority of SiC NWs studies deal with 3C-SiC NWs. This is due to the fact the cubic polytype is the most stable polytype at low temperature [11]. So, when SiC NWs are mentioned in this thesis, it'll mean 3C-SiC NWs. Otherwise, the specific polytypes of NWs will be mentioned. In this section, I'll review the literature on synthetic diversity techniques to fabricate the SiC NWs by the bottom-up methods. SiC NWs also can be prepared by conversion methods, which is exposing carbon and silicon precursor on Si NWs and CNTs, respectively. I'll also mention the recent progress of conversion methods for the fabrication of SiC NWs.

▣ Top-down approach

Feng et al. [30] have fabricated the SiC nanostructures with a diameter of 55 nm by etching heteroepitaxially grown 3C-SiC layers (thickness ~ 55 nm) on Si substrate. Fabricated SiC nanostructure is suitable to nanoelectromechanical system (NEMS) devices, but it is not suitable for the electrical device due to the low crystalline quality.

▣ Bottom-up approach

Considerable efforts have been made to fabricate SiC NWs by bottom-up approach. To date, many techniques have been developed to synthesize SiC NWs, as listed in Table 1.3

Table 1.3 Bottom up growth methods of SiC NWs.

Growth technique	Ref.	Growth technique	Ref.
Thermal evaporation (carbon thermal reduction)	[31, 32]	Laser ablation	[33]
Arc discharge	[34]	Polymer pyrolysis route	[35]
Chemical vapor deposition	[28]	Combustion process	[36]
Microwave heating-assisted methods	[37]	Template-directed synthesis	[38]

The vapor based techniques employed to synthesize SiC nanostructures could be categorized according to the route to generate the vapor species, such as thermal evaporation, laser ablation, polymer pyrolysis, arc discharge, combustion process, microwave methods and chemical vapor deposition.

- ❖ Thermal evaporation (Carbon thermal reduction)

The thermal evaporation (also called carbothermal reduction) is widely employed in nanofabrication processes due to its simplicity, high yield and low cost. The technique uses powder or condensed source materials that are vaporized at an elevated temperature. The vapor phase is transported onto a substrate, and consequently produces the SiC NWs by following the VLS or VS mechanism [31, 32].

- ❖ Laser ablation

Laser ablation is the process of vaporizing material from a solid target (such as SiC) containing the desired elements to fabricate 1D nanostructures by irradiating it with a laser beam. The clusters of vaporized material are collected by a cold finger inside a chamber with a controllable environment. The SiC nanostructures are formed on the cold finger [33].

- Arc discharge

Direct current arc discharge is an effective growth method for nanomaterials, which has been commonly used to synthesize carbon nanotubes (CNTs). High temperatures (3000 - 4000 K) instantaneously produced by arc plasma result in enhancement in the synthesis efficiency of nanomaterials. In a typical experiment for the growth of SiC nanostructures, the anode is a sintered graphite crucible with a hole, in which SiC powder was filled, and a pure graphite rod was used as the cathode [34]. When voltage is applied between the electrodes, an arc discharge occurs, which allows the SiC clusters in the anode to instantly evaporate. The clusters of vaporized material precipitate into SiC nanostructure on the cathode or wall of the chamber.

- Polymer pyrolysis route

For polymer pyrolysis method, a slurry solution is prepared by introducing the activated carbon powder and catalyst into polymer (such as, l-PS) [35]. The activated carbon acts as an absorbant to postpone the evaporation during the pyrolysis. A slurry solution or a ground fine powder is loaded in a conventional furnace and begin to pyrolyze at 1300 – 1450 ^{o}C. The silane fragments derived from decomposition of the polymer precursor provided both the Si and C sources for the growth of the SiC NWs.

- Chemical vapor deposition

Chemical vapor deposition (CVD) method directly introduces the gas-phase sources (for Si: SiH_4, $SiCl_4$, $Si(CH_3)Cl$ and for C: CH_3SiCl_3,CH_4, C_3H_8) into the reaction chamber [28]. Three different methods have been used by this group to synthesize SiC NWs using a thin Ni film deposited on Si substrate.

In the first one, 3C-SiC NW is grown on a Ni film (4 nm) deposited on the Si substrate in a Vapor Phase Epitaxy (VPE) reactor with silane (SiH_4) and propane (C_3H_8) as precursors. The synthesized NW are predominantly 3C polytype with <111> growth axis, and planar defects are characterized such as SFs lied on {111} planes, these SFs are oriented perpendicular to the growth axis.

In the second case, 3C-SiC NWs are also synthesized in a heated quartz tube using carbon tetrachloride (CCl_4) as precursor. The carbon tetrachloride (CCl_4) is decomposed at high temperature and formed silicon chlorides by reacting with Si substrate. Consequently, the reaction between silicon chlorides and carbon atoms produce 1D 3C-SiC NWs. As-grown SiC NWs are less than 80 nm in diameter and several tens of microns long.

Last, 3C-SiC/SiO_2 core/shell NWs can be obtained on the Ni-covered Si substrate (Si source) in an open-tube configuration by flowing carbon oxide (carbon source). Carbon oxide served as carbon source for the growth of SiC core structures by reacting with Si species, and it also reacts with SiC core and consequently forms thin SiO_2 sheath on SiC NWs.

- Combustion process

The initiation of the combustion (strong exothermic reaction) results in the fast temperature increase in the reactor, hence the pyrolysis of reactants (poly-tetrafluoroethylene - PTFE) are started. These gaseous species (Si-containing compounds and halocarbons (e. g. C_2F_4)) will be formed in the combustion zone [36]. When they move from the central reaction zone toward the colder area (low temperature zone), the freshly formed carbon atoms assemble either into hexagonal carbon clusters (which may grow into soot particles) and reacts with Si-containing compounds, and consequently it forms SiC compounds. During this rapid SiC nucleation phase, Si and C atoms pack along its close-packed plane. Finally, it leads to the nucleation and growth of 1D SiC structures, generally with abundant SFs and of a low crystalline quality.

- ❖ Microwave heating-assisted methods

Microwave heating is a relatively new technique for large-scale NW processing [37], which is different from existing conventional process. Microwave heating-assisted methods will only heat the target compounds (SiC) without heating the entire furnace. Therefore, this method provides a simple but effective synthesis of SiC NWs using inexpensive resources.

- ❖ Template-directed synthesis

Template-directed method provides a straightforward route to fabricate 1D nanostructures. Channels in porous membranes, such as anodic aluminum oxide (AAO), provide a class of templates for use in the synthesis of 1D nanostructure. Different materials can be generated in situ and shaped into a nanostructure with its morphology complementary to that of the template. Template-directed synthesis provides a high-throughput, simple and cost-effective procedure. Li et al. [38] have demonstrated a large-area highly oriented SiC NW arrays in the nanopores of an AAO template via a series of chemical reactions of Si, SiO_2, and C_3H_6.

In summary, we reviewed the literature on techniques to fabricate the SiC NWs by bottom-up methods. Among the various synthesis methods, CVD and thermal evaporation are widely used for the VLS and the VS mechanism of SiC NW, respectively, because those methods can easily control the amount of reaction species and the reaction temperature. Even though considerable efforts have been made to fabricate the SiC NWs by the bottom-up methods, as-grown SiC NWs still suffered from high density of SFs with unintentional doping.

▣ Conversion methods

As it has been mentioned in the previous section, conventional SiC NWs fabricated by bottom-up methods have shown very high structural defects density with a high level of n-type unintentional doping. To minimize these kinds of problems, some research groups have tried to synthesize the SiC nanostructures by exposing carbon or silicon precursor on Si NWs or CNTs, respectively. A number of works have been carried out in order to control the diameter, length and morphology of Si NWs and CNTs with various growth methods. Therefore, well defined SiC NWs might be obtained with conversion methods by using high quality and controlled 1D material (Si NWs and CNTs).

- ❖ Carbonization of Si nanowires

Zhang et al. [39] have first reported the exposing of carbon-containing precursor on Si NWs in 2000. After the carbonization process, they got a crystalline Si core with a sheath of MWCNT due to the fast carbon deposition. Tsakalakos et al. [40] have demonstrated in situ carburization process by flowing methane and hydrogen right after catalyst-assisted Si NWs growth. After carburization process, it shows partially carburized NWs contained distinct polycrystalline SiC nanosized grains on the Si NWs surface (Figure 1.8(a)). Even though thermodynamically the carbonization of Si wafers is favorable over a wide temperature range (from 500 up to 1360 °C), there exists a significant kinetic barrier to Si NWs carburization below ~1100 °C according to their experimental results.

Yang and coworkers [41] have achieved highly oriented SiC porous NW arrays on Si substrate via in situ carbonizing aligned Si NW porous NW arrays, which are fabricated by chemical etching methods. During the carbonization process, the porous Si NWs react with active carbon species decomposed from C_2H_5OH to form porous SiC, as shown in Figure 1.8(b). Thanks to the porous structure of Si NWs, carbon species can easily diffuse into the whole region of Si NWs without the limitation of carbon's diffusion length in Si. Consequently, the original Si NWs were completely converted into SiC porous NWs.

Xing et al. [42] and Zhou et al. [43] have demonstrated the incorporation of carbon element into Si NWs by the implantation and ion beam deposition, respectively. These small protrusions on Si NWs induced by ion implantation and deposition are confirmed to be β-SiC precipitates by TEM, shown Figure 1.8(c) and (d).

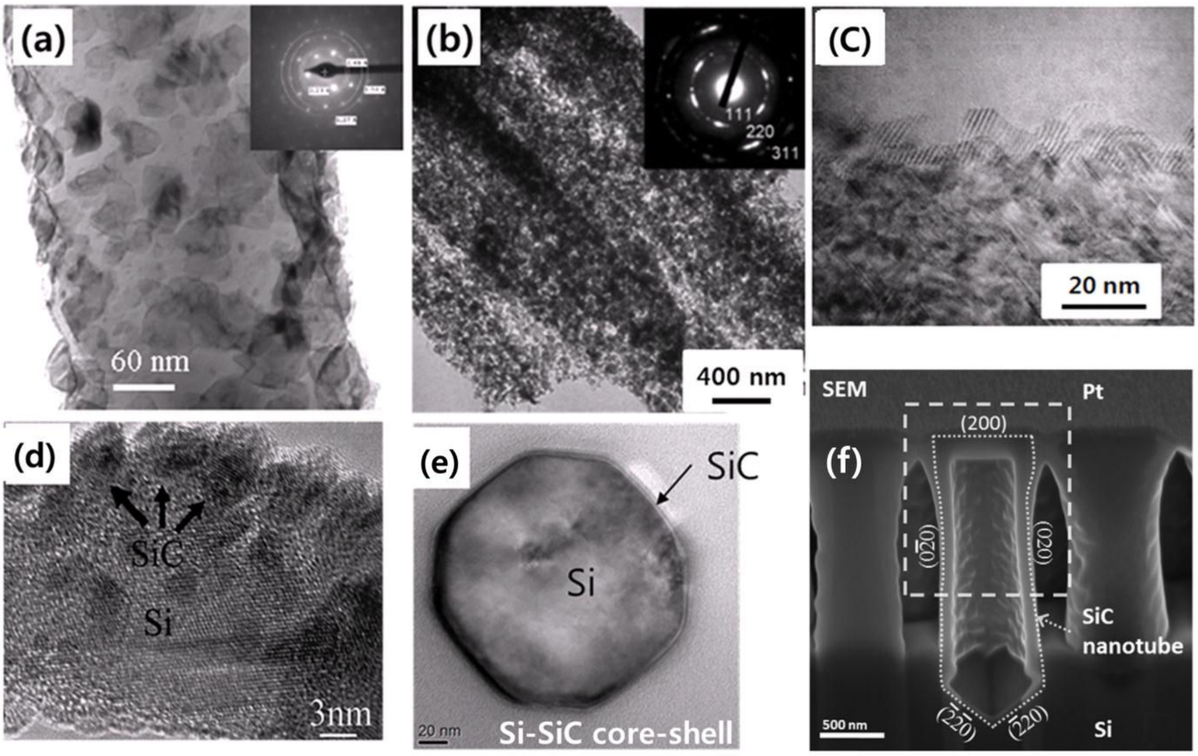

Figure 1.8 (a-b) TEM images and corresponding SAD patterns (inset) after the carbonization of Si NWs, (a) SiC nanosized grains on Si NW [40], (b) SiC porous NWs [41], SiC nanosized grains on Si NW fabricated by (c) carbon implantation [42] and (e) ion beam deposition [43], (e) TEM image of a Si-SiC core-shell NW [44] and (f) SiC NTs [45].

Latu-Romain et al. have reported the carbonization of Si NWs at 1100 °C under methane to form 1D SiC nanostructures [44, 45]. Experimental results have shown that Si NWs can be transformed either in Si-SiC core-shell NWs [44] or in SiC NTs [45]. In the first case, the SiC shell is continuous and single crystalline (as well as the Si core); the thickness of the SiC shell is about 2 to 4 nm (Figure 1.8(e)). In the second case, 3C-SiC-NTs with faceted {200} sidewall planes are obtained with an excellent crystalline quality (Figure 1.8(f)). The external diameter of the SiC-NT is about 300 nm (nearly the same than the etched Si-NWs used) and the thickness of the sidewalls is about 40 to 100 nm. By controlling the pressure during the carburization process, out-diffusion of Si through the SiC layer can be monitored and could lead either to Si-SiC core shell NWs or to SiC-NTs.

- Carbon nanotube-mediated growth

Since the discovery of CNTs in 1991 [5], this 1D nanostructure material becomes very attractive because of its unique mechanical, optical, electronic properties. CNT has also been used as a template (base material) for the fabrication of other 1D nanomaterials such as SiC, TiC, NbC, TaC, BN, and GaN, etc. CNTs are suitable starting materials as precursors for reactant and provide the frame for preparation of new type or heterostructures of 1D nanomaterials. Because, it can be easily converted into a 1D heterostructures nanomaterials by filling the inside of CNTs or coating the outside surfaces of CNTs with other elements. It also can be transformed into various metal carbide nanomaterials or new type of nanotubes by spatially confined reaction or substitution reaction, which replace the carbon element of CNTs with other atoms.

Dai et al. [46] first reported SiC nanorods through a reaction between CNTs and SiO or SiI_2 at high temperature (1100 – 1450 °C). Li et al. [47] have revealed the transition process from the CNTs into SiC NW via a systematic time-dependent TEM analysis. They have also investigated the chemical reaction on different morphology of CNTs (bamboo shape) [47]. The terminations of graphitic layers in the bamboo-like CNTs provide more active sites for the chemical reactions. The segmented bamboo-like structure of the CNTs causes the reaction to start on the external surface of the tubes and progressively transform the CNTs into solid NW segment by segment.

In conclusion, CNT-mediated growth for SiC NWs have successfully demonstrated via various reactions, such as filling, coating, confined reaction and substituted reaction. Even though the SiC NWs synthesized by CNT-mediated growth still possess high density of SFs along the growth direction, it is versatile way to produce a large quantity of SiC NWs with low-cost production.

▣ Several points for the growth of SiC nanowires

❖ Crystal orientation growth

SiC NWs have been grown on various substrates, such as Si, SiO_2, graphite, poly-SiC, 4H-SiC [48] and 6H-SiC [49]. NWs generally grow in the crystal direction with minimum the total free energy. Fabricated SiC NW are 3C-SiC NWs in the most cases grown along <111> direction with SFs {111} planes due to low growth temperature. The use of monocrystalline SiC substrates with a specific orientation may offer possible controllability of hexagonal polytypes SiC NWs during the growth [48] (see discussion below). The growth habits of SiC NWs are strongly affected by the SiC substrate orientations. It has been found that 6H-SiC NWs can grow along the [$\bar{1}$102] direction. The polytype-controlled SiC NWs have great potential to become building blocks for electronic nanodevices, optoelectronic nanodevices with tailored electrical and optical properties.

❖ Growth of 6H-SiC nanowires

The polytype control is a big issue for the growth of SiC NWs as well as SiC bulk substrate, because the various polytypes with different physical properties can provide more versatile applications of SiC NWs. Several methods have been proposed for the fabrication of 6H-SiC NWs, such as arc-discharge process [50], polymer pyrolysis route [35] and microwave methods [51].

Li et al. [50] have first reported the synthesis of cone-shaped 6H–SiC nanorods by an arc-discharge process. The 6H-SiC nanorods have the same preferential growth <10$\bar{1}$0> direction. They have proposed that the high enthalpy of the droplets and the Al doping in the NWs favor the formation of hexagonal 6H–SiC NWs rather than the stable cubic 3C–SiC phase. Gao et al. [35] have reported Al-doped single-crystalline 6H-SiC NWs by the catalyst-assisted pyrolysis of polymeric precursors with $FeCl_2$ as the catalyst. The 6H-SiC lattice constant decreases with increasing the Al content, which indicate that Al-doped SiC NWs formed by the substitutional solid solutions. Wei et al. [51] have synthesized by microwave method with the presence of nano-Al powders. It is interesting to find that they could not have obtained 6H–SiC NWs without the use of nano-Al powders. It seems that Al powders play a crucial role in forming 6H-SiC NWs. Wang et al. [49] have first demonstrated preferred orientation of 6H-SiC NWs on 6H-SiC substrate. 6H-SiC NWs grew in <10$\bar{1}$0> direction (or its equivalent ones). SiC NWs grown on (0001) plane show six growth directions with same orientation ($\bar{1}$102).

- Various morphologies of SiC nanowires

Synthesized 1D SiC structures show various morphologies in the literature. Its range includes core-shell, nanotubes, hollow, helical, flower, neck-lace, needle, bamboo and porous morphologies, as shown in Figure 1.9.

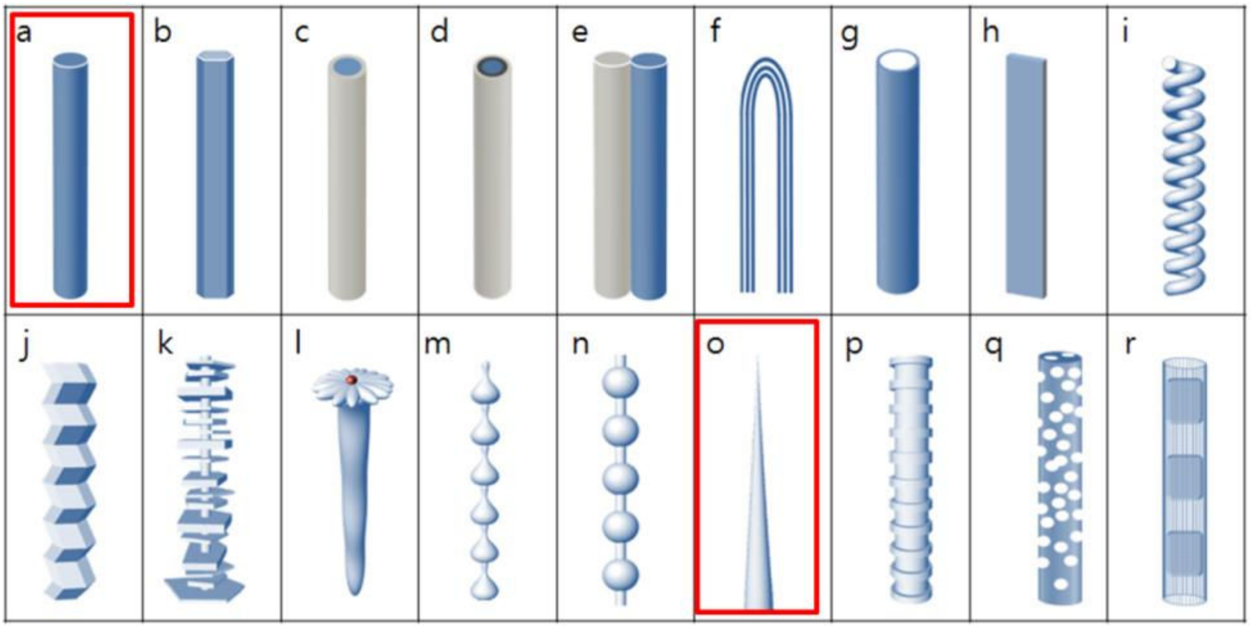

Figure 1.9 Schematic summary of various morphologies of SiC nanostructure reported in the bibliography. (a) cylinder [28], (b) hexagonal [52],(c) core-shell [8], (d) core/multi-shell [53], (e) bi-axial [54], (f) nanotubes [55], (g) hollow [45], (h) nanobelt [56], (i) helical [57], (j) twin [58], (k) hierarchical nanoarchitectures [59], (l) flower [60] , (m) beaded nanochains [61], (n) neck-lace [62], (o) needle [63], (p) bamboo [52], (q) porous [41], (r) CNT-encapsulated SiC nanocrystals [64].
In the present thesis, SiC NWs with the morphologies of (a) cylinder and (o) needle have been investigated.

The growth kinetics and thermodynamics of 1D SiC nanostructures are complex, the morphologies of as-synthesized SiC nanostructures will be significantly different even with a minor difference on the synthesis conditions. It is known that the properties of NWs, such as optical, electrical and mechanical properties, may sensitively depend on their geometrical shape. Therefore, full control of morphologies, composition and dimensions of SiC nanostructure has been a dominant theme in materials science

For example, core-shell structure might be suitable for building blocks of nanoelectronics device, since the electron density is confined to the core and the shell serves as a potential barrier. And the SiC nanotube has theoretically proven well suited to hydrogen storage. Unique morphology of SiC beaded nanochains has exhibited an excellent reinforcing property when used as filler in composite [61]. Needle, bamboo and porous SiC nanostructures have been proven to increase the field emission efficiency by enhancing the field enhancement factor.

In our study, two types of SiC NWs (cylinder and needle shapes - (Figure 1.9(a) and (o), respectively) are used for the fabrication of SiC nanodevices in chapter 4. In case of the needle-shaped SiC NW growth, the Ni catalyst is gradually evaporated or diffused into NW during the reaction, therefore the size of the nanosize metallic droplet as catalyst will decrease. Consequently, it results in a sharp end of the needle-shaped SiC NWs. The apex of a needle SiC NW could be down below 10 nm [63].

- Doping of SiC nanowires

Doping is obviously used to tailor the electronic properties of SiC, and is one of the main reasons for the usefulness of semiconductors in electronics. It is therefore necessary to investigate how impurities incorporate into NWs. For bulk SiC and SiC thin films, doping can be realized by vapor phase co-deposition [65] and ion-implantation [66]. Ion implantation method can control the lateral control of dopant incorporation. However, doping processes of nanostructures may show completely different behaviors from that obtained in the bulk phase. For instance, several nanocrystals exhibit a lower incorporation rate of impurities than their bulk counterpart. In this case, the impurity elements are ejected from the inner sites of the nanocrystal, lying at the nanocrystal surface, there is a "self-purification" process.

Generally, SiC NWs grown by many growth technique show unintentional n-type doping (~ 10^{19} - 10^{20} cm^{-3}) along the NWs [29]. Among the doping methods, diffusion methods are not suitable for SiC NWs, because the diffusivities of dopants in SiC are very low due to the chemical inertness and densely packed atomic structure of SiC, and high temperatures above 1800 °C are needed for the incorporation of dopants into the SiC. However, this process might promote the graphitization of SiC NWs by Si sublimation and probably induce the SiC/CNT heterostructures.

A feasible method for the doping of SiC NWs is in situ doping during the growth by exposing the doping precursor. In most cases, as-grown SiC NWs are unintentional n-type doped (10^{18} – 10^{19} cm^{-3}) during the growth. The best value of effective carrier mobility measured on n-type SiC NWFET is 15 $cm^2 \cdot V^{-1} s^{-1}$ [29]. P-type doping is also investigated for modulating the electrical property of SiC NWs [67, 68]. Al doped 3C-SiC NWs have demonstrated as an outstanding building blocks for the field emitter [67] and nano Field Effect Transistor (FET) [68]. Chen and Zhang et al. [68] have reported for the first time the fabrication of p-type 3C-SiC NW FET, it exhibits a hole carrier concentration of ~ 1.7×10^{17} cm^{-3} and a low mobility of 6.4 $cm^2 \cdot V^{-1} s^{-1}$. They also considerably improve the field emission properties of 3C-SiC NW by reducing the work function via in situ Al doping [67].

Besides the doping for modulating the electrical property, Seong et al. [69] have also demonstrated the doping of transition metal (V) in 3C-SiC NWs and characterized its magnetic semiconductor behavior at very low temperature.

1.4 Properties of SiC nanowires

In this section, I'll introduce the electrical, mechanical and thermal properties of SiC NWs. Our experimental results of the electrical properties of SiC NW FET will be discussed in chapter 4.

1.4.1 Mechanical properties of SiC nanowires

The mechanical properties of nanostructures have aroused considerable interest due to possible stronger property than their bulk counterparts. This might be attributed to a reduction in the number of defects per unit length (compared with larger structures), which leads to mechanical failure.

For the practical applications of SiC NWs, it is important not only to understand its mechanical properties, such as toughness and hardness, but also to investigate mechanical response, such as elastic-plastic response and brittle-ductile transition, in the nano-domain [70]. Researchers have investigated the mechanical properties of various nanowire systems with different approaches, such as nano-indentation [71], atomic force microscopy (AFM) [72] and mechanical resonance by in situ TEM [54].

▣ Mechanical properties of SiC nanowires

Two main approaches have been developed to characterize the mechanical properties of various NWs. The first one has measured the strength of SiC nanorods with AFM by physical bending of the SiC nanostructure, which was pinned at one end to molybdenum disulfide surfaces [72]. The bending force was measured versus displacement along free-end lengths. The measured bending strength and Young's modulus of SiC nanostructures were 53.4 and 660 GPa, respectively. Young's modulus of SiC nanostructure shows were substantially greater than those found previously for any type SiC structures (SiC whiskers and fibers), and they approaches theoretically predicted value (600 GPa) for [111] oriented bulk SiC [72].

The second method used electric-field-induced resonance for measuring the mechanical properties by the field emission microscopy (FEM) [73] and in situ TEM [54]. One end of the NW is pinned on the tip, and an oscillating voltage is applied across the ball and its counter electrode. Mechanical resonance occurs when the applied frequency matches the natural resonance frequency of NWs. Wang et al. [54] have measured the mechanical property of biaxial SiC-SiO_x NWs by in situ TEM. They have proved that the effective Young's modulus (E_{eff}) of biaxial structured SiC–SiO_x NWs is the combination from SiC and SiO_x. The Young's modulus determined by FEM yielded a high Young's modulus value (Y =750 GPa) [73], which is corresponding to the highest value reported in the literature for a bulk single crystal of 748 GPa.

▣ Mechanical behavior of SiC nanowires

Han et al. [74] have directly observed the mechanical behavior of SiC NWs in situ TEM measurement by bending individual NWs. Instead of a crystalline fracture (or any cracks) under deformation, the SiC NW has transformed from crystalline to amorphous at the mostly strained region. Large strain plasticity of SiC NWs at temperatures close to room temperature has been observed for the first time in this study. From their experimental results, the plastic deformation process of SiC NWs is typically regarded as three stages, dislocation initiation, dislocation propagation and amorphization. Zhang et al. [70] have investigated the plastic deformation and fracture behavior of individual SiC NWs by in situ stretching equipment in a SEM. The plastically deformed region shows identical size and morphology without any necking appearance, indicating a super-plastic deformation.

In conclusion, SiC NWs show excellent mechanical property, such as Young's modulus (660 GPa), comparable or better performance than similar size CNTs. The mechanical properties of SiC NWs have been measured by the bending of NWs with AFM tip and mechanical resonance by in situ (SEM and TEM).

Moreover, the mechanical behaviors SiC NWs have been investigated by the bending and stretching of SiC NWs. SiC NWs shows unique mechanical response like as large strain plasticity (or super plasticity) at low temperature (~ 300 K), which is rarely observed for ceramic materials. Their considerable studies on mechanical properties of SiC NWs will be very useful information when SiC NWs is applied into the composite matrix materials to enhance the mechanical property.

1.4.2 Electrical properties of SiC nanowires

The electrical properties of nano FET is generally evaluated by several figures-of-merit, such as mobility, transconductance, $I_{on\text{-}off}$ ratio and subthreshold slope. A higher value of these figures-of-merit show better electrical device performance [see Appendix.1].

- A high transconductance means that the gate voltage has a large effect on the channel conductance and thus the output current; a small change in V_G induces a large change in I_D. The transconductance determines the maximum operating frequency of devices, which is calculated by the following equation (Eq 1.1).

$$g_m = \frac{dI_D}{dV_G} = \mu\left(\frac{C_{\mathrm{ox}}}{L^2}\right)V_{DS}, \qquad \text{Eq 1.1}$$

,where μ is the effective carrier mobility, C_{ox} is the coupling capacitance and L is the channel length. To estimate the effective mobility of back-gated SiC NW FETs, the coupling capacitance (C_{ox}) between the SiC NW channel and the back gate was calculated by using the cylinder-on-plate model, which can be given by the following equation (Eq 1.2).

$$C_{ox} = \frac{2\pi\varepsilon\varepsilon_o L}{\ln(2h/r)}, \qquad \text{Eq 1.2}$$

,where ε ~ 3.9 is the SiO_2 dielectric constant, h is the thickness of the SiO_2 layer and r is the NW radius.

- High mobility means that the carrier in the channel of nanoFET can be easily controlled by the electric field. The effective electron mobility can be estimated from the following equation (Eq 1.3).

$$\mu = \frac{g_m \cdot L^2}{C_{ox} \cdot V_{DS}} \qquad \text{Eq 1.3}$$

- High subthreshold slope (S.S.) describes how the switch turns off (low current) and on (high current) in the subthreshold region. This S.S. is generally measured at the maximum slope of $\log(I_D)$ versus V_G, which is usually given as Eq 1.4 [75].

$$S.S. \equiv \frac{dV_G}{d(\log I_D)} = \ln(10)\frac{kT}{q}(1 + \frac{C_d}{C_{ox}}) \qquad \text{Eq 1.4}$$

, where C_d is depletion layer capacitance, C_{ox} is gate-oxide capacitance.

- The ON-to-OFF current ratio is also an important parameter. The ON-state current (I_{ON}) determines the FET switching speed, whereas an OFF-state current (I_{OFF}) determines the passive power consumed by a logic gate. Therefore, I_{OFF} level should be as low as possible in order to minimize power consumption of the devices at the OFF-state.

The study of electrical properties of SiC NW has not been investigated in much detail relative to that of Si NW. Up to now, only a few studies have been reported on the electrical properties of 3C-SiC NW. All reported results of SiC NWFET show similar device performance in terms of transconductance and carrier mobility (~ several $cm^2 \cdot V^{-1} s^{-1}$), as listed in Table 1.4. It might be due to very high structural defects density of SiC NW associated with a high level of n-type unintentional doping and weaker electrostatic gating effects of back gate configuration and poor-quality SiC NW-gate oxide interface..

Table 1.4 Reported SiC NWFET and their device performance.

Author	Transconductance	Majority carrier	Mobility	Ref.
Seong et al.	1.7E-10 [Ω^{-1}] at V_{DS}=0.05V	electron	15 $cm^2 \cdot V^{-1} s^{-1}$	[29]
Zhou et al.	5.0E-10 [Ω^{-1}] at V_{DS}=0.02V	electron	15.9 $cm^2 \cdot V^{-1} s^{-1}$	[76]
Jang et al.	N/A	electron	1.6 $cm^2 \cdot V^{-1} s^{-1}$	[77]
Rogdakis et al.	N/A	electron	0.5 $cm^2 \cdot V^{-1} s^{-1}$	[78]
Rogdakis et al.	7.0E-10 [Ω^{-1}] at V_{DS}=1V	electron	0.11 $cm^2 \cdot V^{-1} s^{-1}$	[79]
Chen et al.	12.0 E-9 [Ω^{-1}] at V_{DS}=0.5 V	hole	6.4 $cm^2 \cdot V^{-1} s^{-1}$	[68]

n-type SiC NW FET shows high electric conductivity (2.2×10^{-2} $\Omega \cdot cm$) for 0 V gate voltage due to highly n-type doping level [29]. The measured transconductance (g_m) that is obtained using (Eq 1.1) has value of several 10^{-10} Ω^{-1} [29, 78]. The estimated n-type doping concentration by fitting I-V curve with simulation program (Silvaco) was around 1×10^{19} cm^{-3} [78]. Best electron mobility value measured on SiC NWFET was around 15 $cm^2 \cdot V^{-1} s^{-1}$ [76].

Rogdakis et al. [78] have theoretically investigated the effect of doping concentration to explain poor performance of SiC NWs FETs. Their simulation results show that the device could have a good gating effect with high mobility (> 80 $cm^2 \cdot V^{-1} s^{-1}$) at a doping level of 10^{17} cm^{-3} with an ideal interface (that is to say, without interface scattering).

Chen et al. [68] have reported for the first time the fabrication of p-type SiC NWFET using a Al-doped 3C-SiC NW. But, one again p-type FETs based on an individual Al-doped 3C-SiC NW exhibits a low mobility 6.4 $cm^2 \cdot V^{-1} s^{-1}$. The estimated hole carrier density from I-V curve was determined to be 1.7×10^{17} cm^{-3}.

To exploit excellent electrical property of SiC NWs, many efforts need to be put forth, in particular, to minimize the structural defects (SFs) and unintentional doping. The devices with either ideal ohmic or Schottky barrier contacts are an important parameter to determine the device operating modes. And it is also strongly crucial to investigate about reliable and reproducible of complementary doping (p-type) of SiC NWs.

1.4.3 Thermal property of SiC nanowires

NWs are receiving much attention for applications in energy conversion devices as well as nanoelectronics. In particular, thermal properties of NWs have received significant research interest for designing thermoelectric devices. Experimentally understanding and theoretically prediction of thermal conductivity of NWs are important for related applications.

The thermal conductivity of NWs can be significantly reduced due to the size effect. In case of Si NWs, experimentally measured thermal conductivity of Si NWs show two orders of magnitude lower than the bulk value (150 W·m^{-1}K^{-1}) [80]. In the case of SiC, experimental and theoretical results show also that NW structure to be effective at reducing the lattice thermal conductivity of SiC. Let remind that bulk 3C–SiC presents high thermal conductivity in the order of 330 W·m^{-1}K^{-1} at room temperature [15]. Lee et al. [81] have experimentally measured the thermal conductivity with pre-patterned electrodes by using a focused ion beam and a nanomanipulator They have measured the thermal conductivity of single and double SiC NW, which consist of the same diameter (~ 60 nm). The thermal conductivity of the NWs was extracted by the four-point-probe method. The thermal conductivities were measured at 82± 6 W·m^{-1}K^{-1} and 73± 5 W·m^{-1}K^{-1} for the single and double SiC NW, respectively.

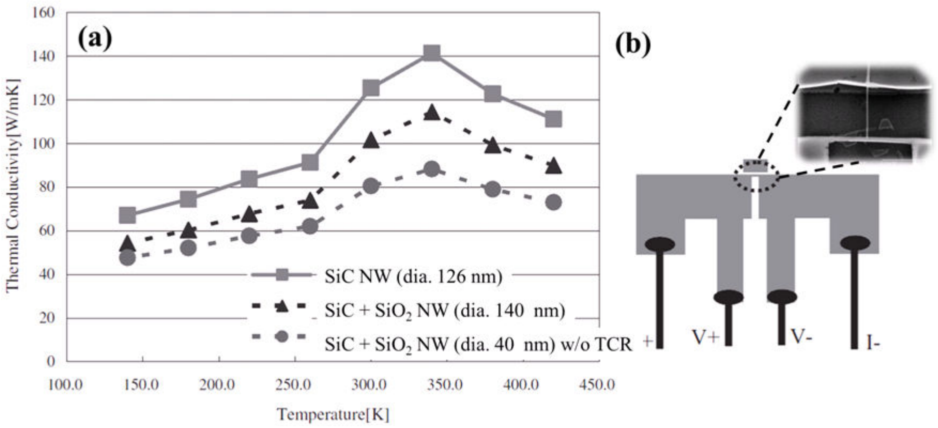

Figure 1.10 (a) Thermal conductivity of SiC NWs according to temperature, (b) T-type nanosensors used for the measurement of thermal conductivity. (TCR in (a) is thermal contact resistance) [82].

Takahashi et al. [82] have characterized the thermal conductivity of an individual SiC/SiO$_2$ NW of 140 nm diameter using T-type nanosensors (see Figure 1.10(b)). Figure 1.10(a) shows measured and estimated thermal conductivity of core-shell SiC/SiO$_2$ NW and intrinsic of SiC core, respectively. There is some variation of thermal conductivity due to the thermal contact resistance. Obtained thermal conductivity of SiC is over 100 W·m^{-1}K^{-1} at room temperature, which is less than the pure bulk data. From theoretical calculations, N. Papanikolaou [83] has estimated the lattice thermal conductivity of SiC NWs at high temperature (500 K) by using non-equilibrium classical molecular dynamics simulation. He has investigated the dependence of the thermal conductivity on the wire cross section and considers the influence of different wire surfaces (Si and C face) on the thermal transport. According to their simulation results, SiC NWs with diameter from 2 to 4 nm shows a thermal conductivity of 3 to 6 W·m^{-1}K^{-1} at 500 K. The lattice thermal conductivity depends sensitively not only on the cross section of nanowire but also on surface terminations (Si and C) of NW. Si terminated SiC NW has lower thermal conductance than C terminated SiC NW. This might be due to stronger scattering on a more disordered Si surface compared to the C one [83].

It has been found experimentally as well as theoretically that the lattice thermal conductivity of SiC NWs can be largely reduced by the size confinement effect. Reduced dimension of SiC NWs induce the change of band structure and phonon dispersion relation, it also leads to increase the interface scattering of phonons.

1.5 Potential applications of SiC nanowires

As we have mentioned in the previous section, SiC NWs have unique electrical, thermal and mechanical properties. Due to these excellent properties, SiC NWs may have some potential applications. In this section, I will attempt to summarize the progress made for practical applications based on SiC NWs. Furthermore, I will also discuss about the potential application of SiC NWs, including proof-of-concept and simulation results.

1.5.1 Field emission display

1D structures can greatly enhance the field emission property due to the high field enhancement factor (β), which is attributed to the high aspect ratio with small diameter and the small radii of curvature. Among 1D structures, CNTs are considered as promising cold-cathode electron emitters due to their low turn voltage (1.0 $V \cdot \mu m^{-1}$) and high brightness (current density of 2.0 $mA \cdot cm^{-2}$) [84]. However, there are some issues to improve for the commercialization of CNT-based field emission devices, such as emission stability and life time.

Nanostructures for field emission have to withstand high temperature near the tip due to Joule heating and the high tensile stress induced by applied high electric field to sustain the tip shape. In most cases, the CNT tip exhibits the degradation behavior during field emission. On other hand, chemical inertness and excellent mechanical property of SiC would result in long life expectancy with stable emission property [67] even under the severe environment, such as high electric field and high temperature.

In addition, SiC NWs are expected to show reliable emission property even at high temperature due to its inherent properties as excellent thermal stability. Even if the maximum temperature is located at the SiC NW's tip by current-induced heating, SiC NW is more likely to form SiC–CNT core–sheath structure due to the graphitization of SiC by the sublimation of Si element [85], rather than gradually shortening such in case of CNTs. Moreover, SiC NWs based field emitter can operate at relatively lower vacuum conditions, which is critical point for commercialization, because it is less venerable than CNT by degassed elements owing to the chemical inertness. Even if oxygen reacts with the emitter, the oxide layer formed on SiC NWs, rather than destroying the tip such in case of CNTs. In addition, the thin SiO_2 shell might enhance the field emission of SiC emitter due to its electron affinity (0.6 - 0.8 eV). Moreover, Perisanu et al. [73] have measured high Young's modulus of SiC NW during the field emission, which shows more mechanical robustness than CNTs.

The above mentioned excellent properties of SiC NWs make these materials particularly interesting candidates for robust field emitter with life expectancy and stable field emission. The research for field emission of 1D structure could be divided into mainly three categories to improve the field emission property, reducing the tip size, doping or coating of the tip, and increasing the emitter sites density [67].

Field emission ability of nanostructures have typically been characterized by two properties, electron emission turn-on field (E_{on}) and threshold field (E_{th}), which defined as the electric fields required to produce a current density of 10 $\mu A \cdot cm^{-2}$ (minimum current level for field emission) and 10 $mA \cdot cm^{-2}$, (current level for realistic application) respectively. Some applications of field emission need the additional information, such as maximum current density, emission stability and life time. Their best values measured on SiC NWs emitters with a needle shape show low turn-on field (0.55 - 1.54 $V \cdot \mu m^{-1}$) and threshold field (1.88 $V \cdot \mu m^{-1}$) [67]. It is believed that needle shape of SiC NW provides higher density of electron emitting sites than typical cylinder shape. In addition, Al doping also might be contributed to this field emission enhancement.

Extraordinary properties of SiC NWs, such as chemical inertness and excellent mechanical property, result in long life expectancy (100 h) with stable emission property even under a severe environment, such as high electric field and high temperature. Thus, SiC NWs are expected to have great potential applications in the areas of X-ray sources for medical imaging, UV light-emitting diodes and UV photodiodes.

1.5.2 SiC nanowires as fillers for composite matrix materials

1D structures have been proposed as an excellent reinforcement material for composites, because it shows extraordinary electronic, mechanical properties with good structural morphology, such as high aspect ratio, compare to bulk counterparts.

SiC NWs have reported a promising candidate for the reinforcing element materials of ceramic matrix, because it guarantees excellent mechanical properties with chemical stability even during the process at high temperature. In addition, SiC NWs is much easier to get a homogenous distribution in the composite matrix compared to other materials like CNTs, which have curl shape and entangled morphology.

Another important feature of SiC NWs is easy to moderate the nanowire/matrix interfacial bounding strength with a compliant coating, such as carbon [86] and silica [87]. These properties of SiC NWs not only lead to the production of low-cost nanocomposites with enhanced mechanical properties, but also permit taking benefits from the well-known surface chemistry of silica and carbon [87]. SiC NWs have also been used as fillers for other composite matrix materials to enhance the mechanical and electrical performance, such as polymer and metal hybrid composites.

In conclusion, SiC NWs have been confirmed to exhibit excellent reinforcement materials in SiC ceramic or polymer or metal hybrid composites. In particular, SiC NWs is the promising 1D material for the composite compare to other NWs, since it is easy to fabricate and control the interfacial layer (e.g. carbon and silica layer) by thermal decomposition of carbon contained gas and SiO, respectively. For the elaboration of SiC NWs based composite, it still need further systematic study about the interfacial layer thickness, filler concentration dependence and dispersion in the matrix, etc.

1.5.3 NEMS applications

SiC is widely used for MEMS applications, because it can operate at higher temperatures and in harsh environments compared to Si. In addition, SiC can also provide potential improvements in operating frequency, power handling capability and reliability compared to devices made in Si. The principles of MEMS can be scaled down to nanoscale dimensions of NEMS for increased sensitive to external perturbations.

SiC NWs could be also used as important building blocks in the development of NEMS and have been intensively investigated for high frequency NEMS application via top-down methods [30]. SiC based NEMS show substantially higher frequencies than other materials due to high values of parameters related to the nano-resonator itself, such as Young's modulus and quality factor, which describes the strength of the damping of its oscillations relative to its center frequency. Flexural mechanical resonance frequencies for beams directly depend upon the ratio its Young's modulus (E) to mass density (ρ) ($\sqrt{E/\rho}$). In addition, excellent chemical stability of SiC guarantees higher quality factors, which is governed by surface defects. Nanometer-scale SiC resonators are capable of yielding substantially higher frequencies than GaAs and Si resonators. Feng et al. [30] have realized NEMS switches based on SiC NWs. This specific device has dimensions L ~ 5 µm, w ~ 55 nm, t ~ 50 nm, and g ~ 60 nm. This device make interesting contact-mode nanomechanical switches that offer very low turn-on voltages down to the level of ~ 1V, and it also simultaneously offer very short switching times in the sub-microsecond range.

1.5.4 Energy conversion devices

NWs based energy conversion devices can be categorized into three different subtopics regarding photovoltaic, piezotronic and thermoelectric applications, generating the energy by harvesting light, mechanical and heat energy waste from the environment, respectively.

▣ Photovoltaic

SiC has been considered to be an inefficient material for photovoltaic applications due to wide band-gap of 2.3 - 3.3 eV. However, solar cells based on SiC materials could be chosen for special use, such as application in space due to the excellent radiation hardness. Richards et al. [88] have demonstrated that 3C-SiC based thin films could be possible choice for photovoltaic applications by employing the amorphous-SiC/amorphous-Si (a-SiC/a-Si) super lattice type or doping technique. NWs have been regarded to be superior for photovoltaic applications compare to bulk or film counterparts, since it has an increase of junction areas and a reduction of defect recombination of photogenerated carriers.

However, up to now, there are no reports about the study of SiC NWs for photovoltaic applications due to its wide and indirect bandgap properties. Nevertheless, in the case of boron doped 3C-SiC, the dopant band of B in the bandgap of 3C-SiC reduces the bandgap up to around 1.8 eV and leads to an efficient use of sun light so that an efficiency up to 48 - 60 % could be achieved depending on theoretical models [47]. If boron doped 3C-SiC substrate is successfully commercialized, SiC nanostructures based on boron doped 3C-SiC substrate could be an excellent candidate for photovoltaic applications in harsh environment.

▣ Piezotronic

The piezoresistive effect describes change in the electrical resistivity (ρ) of a semiconductor when mechanical stress is applied, since the giant piezoresistive effect of Si NWs with a gauge factor of B5000 was reported by He et al. [89]. The piezoresistance effects have been explored in many nanomaterial systems, such as CNT, GaSb, ZnO and InGaAs/GaAs, etc. Gao et al. [90] have characterized the piezoresistance behaviors of single p-type 6H-SiC NWs under different compressed stresses by using a conductive atomic force microscopy (C-AFM) based technique. The decrease of the resistances (ρ) with increasing compressed strains within 6H-SiC NWs has been observed, which is regarded as the piezoresistance effect. The transverse piezo-resistance coefficient $\pi_{[010]}$ of the nanowire is calculated to be in the range of 51.2 to 159.5×10^{-11} Pa^{-1} under the applied loading forces from 43.8 to 140.2 nN. Therefore, SiC NWs could be an excellent candidate for piezoresistivity-based stress sensors working in harsh environment.

▣ Thermoelectric device

Thermoelectric elements, converting heat into electrical energy, offer potential for refrigeration and conversion of heat waste into electricity. Bulk SiC is a poor thermoelectric material due to its high thermal conductivity (300 $W{\cdot}m^{-1}K^{-1}$) [15]. However, 1D structures, such as NWs and quantum dots, are theoretically predicted by Hicks and Dresselhaus to have larger figure of merit (ZT) compared with the bulk counterpart, due to their novel band structure [91].

In particular, SiC is expected to be promising at higher temperature region due to wide gap semiconductor characteristics. Therefore, these unique properties of SiC, if coupled with the advantages of NWs, will make it an outstanding candidate for thermoelectric devices, which operate at high temperature. The performance of a thermoelectric device is usually characterized by the figure of merit ZT (zero dimension value), which can be calculated by Eq 1.5.

$$ZT = \frac{TS^2G}{\kappa_e + \kappa_{ph}} \qquad \text{Eq 1.5}$$

where Z is a measure of a material's thermoelectric properties [K^{-1}], T is temperature [K], S is the Seebeck coefficient [$V{\cdot}K^{-1}$] , G is the electrical conductance [Ω^{-1}], and κ is the thermal conductance [$W{\cdot}K^{-1}$], which is the sum of the electron (κ_e) and phonon (lattice vibration) (κ_{ph}) contributions. To maximize ZT, one strategy is to minimize the thermal conductivity (the denominator of ZT), the other is to maximize the electronic contribution (the numerator of Z), that is, the power factor (S^2G). Si has long been considered to be an inefficient thermoelectric material with ZT ~ 0.01 because of its high thermal conductivity. Recent experiments demonstrated a dramatic increase in ZT (up to 0.6) for Si NWs at room temperature, which is attributed to a two orders of magnitude decrease in thermal conductivity due to the high surface roughness [80]. SiC NWs is considered an inefficient thermoelectric material at room temperature compared to Si NWs, due to lower electronic contribution and higher thermal conductivity than Si. But, SiC NWs could be promising materials for thermoelectric elements operating at high temperature due to its wide band gap and low intrinsic carrier concentration, while silicon cannot compete above 300 °C, due to the large intrinsic carrier concentration.

Xu et al. [92] have theoretically investigated the thermoelectric property of SiC NWs with nitride dopants and vacancies. The figure of merit ZT of SiC NWs can be significantly enhanced by doping N impurities together with making Si vacancies. For the SiC NW with a diameter of 1.1 nm and a length of 4.6 nm, the ZT value for the n-type is shown capable of reaching 1.78 at 900 K.

We have also theoretically explored the thermoelectric behavior of SiC NWs as a function of the temperature (300 – 600K) and the wire square cross sections (varying from 2.05×2.05 to 4.21×4.21 nm^2). The ZT of C terminated SiC NWs reaches a maximum value of 1.04 at 600K. The detail theoretical results will be discussed in chapter 2.

Theoretical studies have envisaged SiC NWs based thermoelectric application at high temperature. It needs to investigate structural effect of NWs, such as surface roughness and periodic twin structures, to further enhance the ZT of SiC NWs.

1.5.5 Catalytic nanomaterials

Recently, photocatalysts have gained a lot of attention to solve the environmental pollution at global scale. Photocatalysts can be used for the removal of contaminants from the environment (the air, wastewater, etc.). Photocatalysts accelerate the decomposition of water to give hydroxyl radicals, when it exposed to strong sunlight or ultraviolet (UV) light. These strongly oxidizing molecules can subsequently react with many different pollutants, decomposes into non-toxic organic materials. Zhou et al. [93] have evaluated the photocatalytic activity of the SiC NWs by measuring the photodegradation rates of CH_3CHO as a function of UV irradiation time. Zhou and coworkers have demonstrated excellent photocatalytic activity using β-SiC NWs coated with amorphous SiO_2.

1.5.6 Nanowires for self-cleaning coating films

Generally, it is also known that as-synthesized SiC-NWs are hydrophilic due to the existence of a native oxide. However, when the size of a material is reduced to the nanoscale, the property of SiC could be changed into hydrophobic due to the high-energy barrier between a solid and liquid interface. Niu et al. [47] have demonstrated high super hydrophobicity by laterally aligning SiC NWs during the growth. Aligned SiC NWs show excellent super hydrophobic property with a high water contact angle more than 156 ± 2°, compared to random oriented NWs (147 ± 2°) and pure Si wafers (101 ± 2°). Even after exposing the samples in air for one week, it shows little variation (less than 5°). Aligned SiC NWs show the better super hydrophobicity with surface fictionalization with CF_2/CF_3 groups. Wang et al. [94] have modulated the surface properties of SiC NWs by a coating of C. The measured water contact angles of SiC NWs and C-sheathed SiC NWs are 68° and 112°, respectively. The surface modifications of C coating tailored SiC surface property from hydrophilic to hydrophobic, which could maintain excellent electrical property of SiC NWs even in a humid atmosphere.

Niu et al. [47] have fabricated the coating material by dropping the SiC NWs into a mixture of tetraethyl orthosilicate (TEOS), ethanol and hydrochloric acid. The mixture could be coated on glass and a possible on any substrate other substrates. Smooth glass coated with the SiC NWs mixture shows a contact angle - the intrinsic angle formed between a liquid droplet and a solid surface - of up to 160°, much greater the 105.8° for pure glass. And the sliding angle (or roll-off angle) was low, down to ~ 5°. When water droplets rolled off from the SiC NWs coated glass, it also takes a dust with them. Based on the above mentioned experimental results, super hydrophobic property of SiC NWs may open new possibilities to apply it into various self-cleaning fields, such as in fields of various coatings, textiles, on windows in high-rise buildings and on car windscreens. But, it is still required to further improve the stability of the coating and against damage to use in practical applications.

1.5.7 Hydrogen storage

Since CNTs is a possible candidate for hydrogen storage application, a considerable amount of experimental and theoretical works has been carried in order to improve the hydrogen storage capacity. Two main strategies for increasing the H_2 storage capacity are based on the introduction of point charges to the host material either by doping with hetero-atoms or by incorporating light metal atoms. In this way, the binding energy of the hydrogen molecules would be enhanced due to charge induced dipole interactions. The focus of research has mostly been done by importing hetero-atoms, such as BN NTs. SiC NTs also could be considered another candidate for the heteroatom structure. SiC NTs were synthesized based on the substituted chemical reaction, which is transforming CNTs or Si NTs into SiC NTs [55]. However, to the best of our knowledge till date, there is no experimental report of the hydrogen storage by using SiC NTs.

Simulated results show an increase of 20% in the binding energy of H_2 in SiC NTs compared with pure CNTs. The main contribution to the improvement of storage capacity is owing to the alternative charges that exist in the SiC NTs walls. Classical Monte-Carlo simulations of nanotube bundles have also shown an increase of the storage capacity in SiC NTs (3.68 wt%) compared with pure CNTs (3.03%), especially in low-temperature (175K) and high-pressure conditions (10 Mpa) [95]. Wang et al. [96] have shown a further improvement in hydrogen absorption of SiC NT by incorporating light metal atoms (Li). Baierle et al. [97] have studied the hydrogen absorption at defects site, hydrogen interaction with boron acceptors and nitrogen donors in single-wall SiC NTs, respectively.

Based on the simulation results, SiC NTs seem to be more suitable materials for hydrogen storage than pure CNTs. However, if we want to apply the SiC NTs into real hydrogen storage applications, it still needs some improving on the control growth of SiC NTs and its chirality independence.

1.5.8 Nanodevices

Semiconductor NWs have been intensively studied in the last decade due to their novel physical properties and potential applications in high performance electron devices. In particular, Si NWs have shown as unique building blocks for fabrication of advanced electronic devices [1]. Among various NW-based electronic device, FET is the key component, which determine the device performance. However, compared with the study of electronic properties of Si NWs, there has been less work done for SiC NWFETs.

The experimental results of SiC NWFET show poor device performance in terms of transconductance and mobility (several $cm^2 \cdot V^{-1} s^{-1}$). It is well known that unintentionally doped SiC NWs show n-type characteristics because of a high density of donor states under the conduction band edge, resulting from SFs that cause intrinsic structural defects [77]. The poor-quality interface between SiC NW and gate oxide could also be another reason for poor device performance. The source/drain(S/D) contact properties become an important issue and determine the device performance. Jang et al. [77] have evaluated ohmic contact properties of SiC NW FET with different metal species (Ti/Au and Ni/Au). Their results indicate that Ni/Au ohmic contacts had ~ 40 times lower specific contact resistances of $5.9\times10^{-6} \pm 8.8\times10^{-6}$ $\Omega\cdot cm^2$ compared to the values of Ti/Au ohmic contacts ($2.6\times10^{-4} \pm 3.4\times10^{-4}$ $\Omega\cdot cm^2$). Rogdakis et al. [79] have demonstrated the Schottky contact barrier (SB) SiC NW FET. SB SiC NW FET shows improved device performance by suppressing the off current and indirectly modulating the drain current through the control of contact barrier at S/D regions. Chen et al. [68] have reported for the first time the fabrication of p-type SiC NW FETs using an individual Al-doped 3C-SiC NWs. The value of the field-effect hole mobility (~ 6.4 $cm^2 \cdot V^{-1}s^{-1}$) is found to be 2 - 3 times lower compared to that expected in the p-type 3C-SiC film (20 $cm^2 \cdot V^{-1}s^{-1}$ at same hole carrier density).

For computational study of SiC NW FET, it has been shown that SiC NWs FETs have similar electrical behavior compared with Si NWs FETs in the ballistic regime [98]. They have the same subthreshold slope (69.5 mV/dec for SiC and 69.8 mV/dec for Si devices for 3×3 nm^2 NW cross-sections). Rogdakis et al. [78] have estimated the density of electrically active interface states (D_{it}) and the doping concentration by fitting the experimentally measured I-V curve using simulation program (Silvaco). The value of D_{it} and the doping concentration are equal to ~1.5×10^{12} $cm^{-2} \cdot eV^{-1}$ and the n-type doping level of 1×10^{19} cm^{-3}, which are responsible for the poor device performance of SiC NWFET.

To exploit excellent electrical property of SiC nanostructure, we fabricate high quality of SiC nanostructure by etching single crystalline SiC substrate via top-down approach (see chapter 3) and realize the SiC nanodevices (see chapter 4).

1.5.9 Bio-related applications

SiC has been proposed as a suitable material for bio-related in vivo and in vitro applications due to its biocompatibility and chemical inertness [17]. For in vivo applications, SiC is expected to be a promising coating material of implantable parts, such as total hip replacement, because it possess biocompatibility, chemical inertness and superior tribological properties compare to common orthopedic metals [18]. Traditional orthopedic materials (such as titanium and stainless steel) are biocompatible for use in joint replacement. However, it is a relatively soft metal and wears easily, which leads to component loosening. Therefore, mechanically stable and biocompatible SiC material is expected to be an excellent coating material for in vivo applications [18]. But, there is no report for in vivo applications based on SiC NWs up to now. SiC NWs are potentially applicable as coating materials or fillers of traditional orthopedic materials to increase the biocompatibility and mechanical properties.

For in vitro application, 3C-SiC quantum dots (QDs) with no protective shells have been used for fluorescence imaging of biological living cells [99]. QDs can be useful tool for monitoring cancerous cells and for providing a mean to better understand its evolution for in vitro analysis due to its excellent luminescent property. SiC QDs do not need a protective shell to avoid the cytotoxicity owing to its biocompatibility.

Despite of excellent biocompatibility of SiC NWs, to the best of our knowledge, there has been no report of the bio-sensor based on SiC NWs. Generally, NWs FET regarded as a basic component and structure for sensing devices. Conventional SiC NWs FET shows poor performance in terms of low mobility and weak gate owing to high density of SFs associated with a high level of non-unintentional doping. Therefore, SiC NWs based sensor, which modified or functionalized the channel of SiC NWs FET with molecular receptors, could not guarantee a sensitive and selective operation due to poor electrical properties of SiC NWs FET. Thus, the growth of defect-free SiC NWs with controlled doping is strongly needed to realize the excellent performance of bio-sensor based on SiC NWs.

1.6 Conclusion

The objective of this chapter was to give an introduction on the growth, properties and potential applications of SiC NWs based on the reported results up to now.

Over the past decade, tremendous efforts have been made to fabricate various 1D structures with controlled crystallography and morphology by two different strategies; the bottom-up and the top-down approach. This chapter has reviewed the main growth mechanism of SiC 1D nanostructures, since this understanding is beneficial for their future application [100]. The fabrication of SiC NWs by bottom-up method has been intensively studied based on different growth methods. Even though they were basically successful, several issues also still need to be investigated to use SiC NWs as a building block for various applications:

(1) As-grown SiC NWs fabricated by bottom-up method present a high density of structural defects, such as SFs. This kind of defect is one of the factors which lead to poor electrical performance (such as weak gate effect and low mobility) of the related devices and it limits their practical applications. Therefore, it is required to develop a high quality of SiC nanostructures with low density of the structural defects using an alternative method, such as top-down process. It will be discussed in more detail in chapter 3.

(2) In addition, as-grown SiC NWs by bottom-up method are also suffered from high level of n-type non-unintentional doping. And it is also strongly needed to investigate about reliable and reproducible of complementary pairs of n-type and p-type of SiC NWs

(3) The polytypes control is a big issue for the growth of SiC NWs as well as SiC bulk substrate. Different polytypes (such as, 3C-, 4H-, and 6H-SiC) of SiC have different physical properties, that originate from the different stacking sequences of the Si–C layers. Therefore, the various polytypes with different physical properties can provide more versatile applications of SiC NWs. Conventionally grown SiC NWs are predominantly 3C polytype with <111> growth axis. Therefore, more intensive research studies about the control of SiC polytypes, potential should be developed.

(4) The orientation of NWs plays a key role in determining the applications of 1D nanostructures. It is desirable to fabricate oriented SiC NWs arrays for the application rather than the random oriented morphology. For example, aligned SiC NWs arrays exhibited excellent field emission property and high hydrophobicity compared to randomly oriented arrays.

(5) The fabrication methods of SiC nanostructure presented here generally involves a high-cost starting material, complicated catalyst fabrication process and low yield of products. Hence, alternative methods toward simpler and more economic directions have to be developed.

(6) The technology of single crystalline SiC substrate with different polytypes has been developed over the two past decades and has shown commercial availability of SiC substrates of ever-increasing diameter and quality. Therefore, top-down SiC nanostructures will combine the advantage of high quality commercially available SiC material and the ones of nanostructures.

Intensive research work have been attempted to investigate various properties of SiC NWs on the experimental and theoretical levels [101]. An understanding of their fundamental properties of SiC NWs leads to enrichment their applications from nanodevices to nanocomposites. In particular, potential applications of SiC NWs have been systematically summarized in this chapter including a proof-of-concept and simulation results.

Surprisingly, there is no any report of implementing SiC NWs for biosensor applications despite their interesting biocompatibility property. Generally, SiC is biosafety and biocompatible than Si, and it can be used for biomedical applications without any coating. Therefore, SiC NWs might be ideally suited as interfaces capable of bridging biomaterials and nanoelectronic devices because of their excellent biocompatibility [17]. We believe that it opens up exciting perspectives for in a variety of medical applications and bio-electronic devices.

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Chapter 2. Modeling of electrical transport in Si and SiC nanowire FET

2.1 Introduction

When the channel length (L) of MOSFET is sufficiently larger than the mean-free-path length (λ) of electrons, as illustrated in Figure 2.1, a first principle semi-classical based on the electronic transport modeling (such as Monte Carlo (MC) simulation [1] and a full Boltzmann equation (BTE) [2]) well describes the electrical behavior of devices. However, as the feature size of the MOSFETs enters into the nanoscale (or when L is close to the λ), these models are faced with difficulties arising from the quantum mechanical effects. Therefore, full quantum transport approaches, such as the nonequilibrium Green's function (NEGF) formalism, become necessary to describe the quantum confinement effects and the ballistic transport.

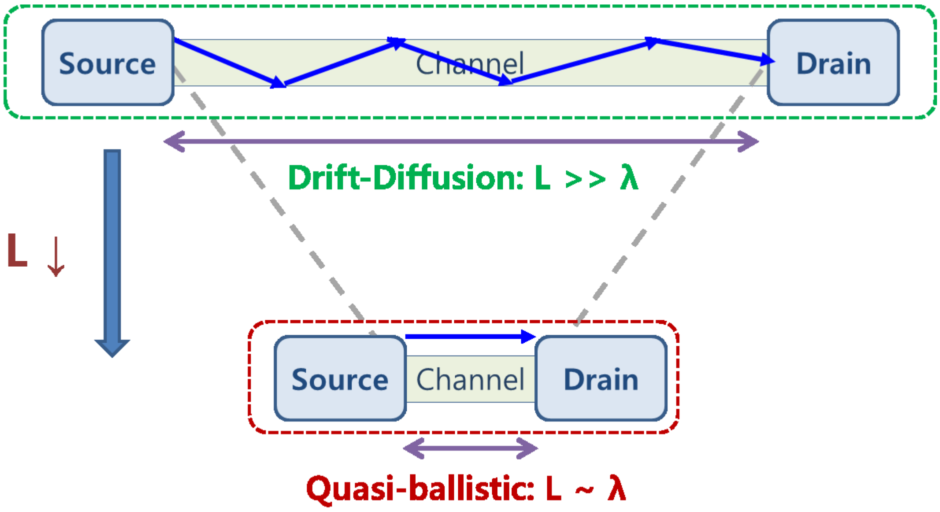

Figure 2.1 Illustration of carrier motion with decreasing the channel length. The arrows are carrier motion in the channel. If L>>λ carrier motion can be approximated as drift and diffusion while carrier transport becomes quasi-ballistic when L is close to λ.

In this chapter, the electronic transport in SiC (or Si) NWFET has been investigated based on the NEGF formalism in the ballistic regime with a diameter below 5 nm. Before delving into details simulation results, I'll briefly introduce the main features of the simulation models of SiC (or Si) NWFET using the NEGF formalism. And then I'll show the simulation results of electrical transport of SiC and Si NWs, including the thermoelectric properties.

2.1.1 Self-consistent solution

Our simulation of electrical devices involves a self-consistent simulation scheme between the charge distribution ρ (obtained from Schrödinger equation) and the electrostatic potential ϕ (obtained from Poisson equation). To fully realize the self-consistent simulation, we need to understand the two major equations in our simulations.

The calculation of the fundamental physical observables parameters (*i.e.* charge distribution $\rho(r)$ and current) for a given the self-consistent potential energy $U_{SC}(r)$, is obtained by the solution of the time-independent Schrödinger equation (Eq 2.1):

$$H\Psi(r) = \left(-\frac{\hbar^2}{2m^*}\nabla^2 + \mathrm{U_{SC}}\right)\Psi(r) = E\Psi(r), \qquad \text{Eq 2.1}$$

where *H* is the Hamiltonian (in parabolic effective mass approximation), $\psi(r)$ is the electron wave function, m^* is the position-dependent effective mass tensor, U the conduction band potential energy profile, E the injection energy of the carrier, and r=(x, y, z) is the 3D position vector.

The electrostatic potential ϕ is computed through the solution of the Poisson equation. Specially, in order to take into account the non-homogeneities in the simulated structure, we adopted a generalized form for Poisson equation (Eq 2.2):

$$\nabla \cdot (\varepsilon(r)\nabla U_{SC}(r)) = -\nabla \left(\varepsilon(r)\nabla \phi_{SC}(r)\right) = \rho(r) = q(N_D - n), \qquad \text{Eq 2.2}$$

where $\varepsilon(r)$ is the position-dependent dielectric constant of the medium, $\rho(r)$ is the charge density. It determines the self-consistent potential energy $U_{SC}(r)$ (ϕ is the electrostatic potential) for a given charge density $\rho(r)$.

The numerical calculation is starting from an initial guess coming from the solution of the Poisson equation, which determines the conduction band profile ($U \leftrightarrow -q\,\phi$, where q is the elementary charge). On the other hand, the electron density depends on the solution of the Schrödinger equation through the square modulus of the electron wave function. The two equations are iteratively solved until a convergence. Thus, a coupling between (Eq 2.1) and (Eq 2.2) is determined and an iterative self-consistent scheme has to be applied to find the solution, as shown in Figure 2.2.

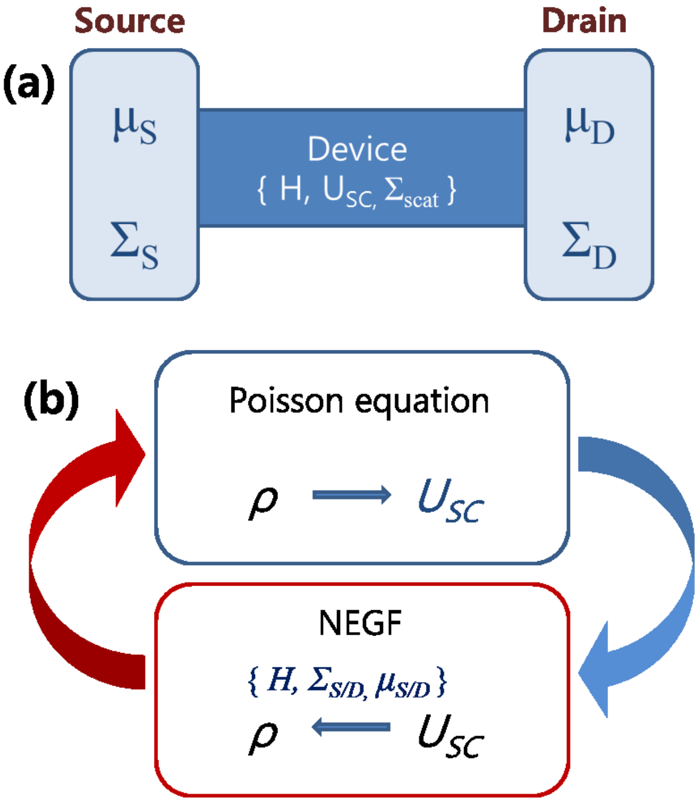

Figure 2.2 (a) Schematic structure of a device coupled to the source/drain contacts, (b) diagram representing the iterative self-consistent solution of NEGF and Poisson equations.

2.1.2 Non equilibrium Green's Function formalism

NEGF solves the Schrödinger equation under non-equilibrium conditions. NEGF provides an ideal approach for bottom-up device simulations due to the following reasons:

(1) The device can be coupled to contact,

(2) Open boundaries can be rigorously treated,

(3) Atomistic descriptions of devices can be readily implemented,

(4) Multi-phenomena (e.g. tunneling, inelastic scattering) can be included.

In the NEGF formalism, the two main quantities to be calculated are the retarded Green's function G^R, which describes the dynamics of electrons inside the conductor (Eq 2.3) and the lesser-than Green's function $G^<$, which correlates the electron wave functions (Eq 2.4).

$$G^R = [(E + i\eta^+)I - H_d - \Sigma^R]^{-1}, \qquad \text{Eq 2.3}$$

$$G^< = G^R \Sigma^< G^A, \qquad \text{Eq 2.4}$$

where a matrix notation has been adopted and η^+ is an infinitesimal positive value, H_d presents the device Hamiltonian, G^R is the retarded self-energy, G^A is the advanced Green's function (which is the Hermitian adjoint operator of G^R) and $\Sigma^<$ describes the in-scattering rates including the effect of scattering from both contacts and phonons.

The electrical current (at 300 K) within NEGF formalism is calculated using the following equation (Eq 2.5),

$$I = \mathrm{g}\frac{q}{h}\int T(E)[f_S(E) - f_D(E)]dE, \qquad \text{Eq 2.5}$$

where *g* denotes the degeneration coefficients (which is 4 (the valley and spin degeneration coefficients) for Si, 2 (the valley degeneration coefficients) for SiC), *h* is the flank constant $h = 2\pi\hbar$, *T(E)* is the transmission coefficient, $f_{S/D}$ (E) is the Fermi function at the Source/Drain (S/D).

The transmission coefficient is calculated from the Green's function of equation as follows (Eq 2.6).

$$T(E) = Trace(\Gamma_S G \Gamma_D G^+), \qquad \text{Eq 2.6}$$

where $\Gamma_{S/D} = i[\Sigma_{S/D} - \Sigma_{S/D}^+]$ is the S/D transmission coefficient, $\Sigma_{S/D}$ describe how the channel couples to the S/D contacts.

2.1.3 Presentation of the simulation scheme

The flowchart of the computation in modeling nanodevices with the nonequilibrium Green's function is shown in Figure 2.3 [3].

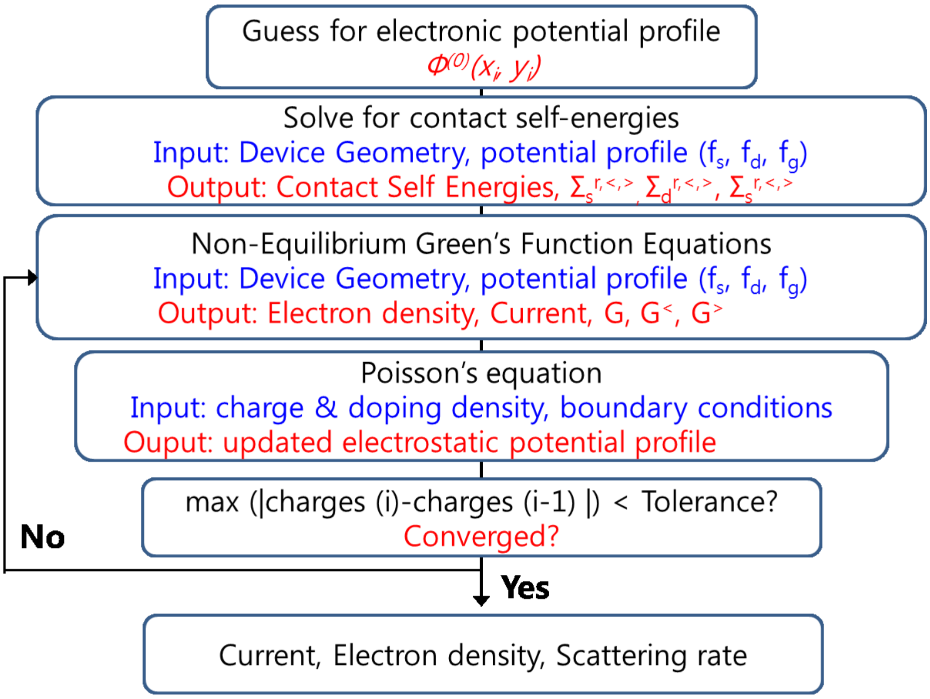

Figure 2.3 Flowchart of simulation involved in modeling of a nanodevice, adopted from [3].

The step-by-step procedure for the NEGF approach is described as follows:

- The simulation starts with the initial guess of the electrostatic potential profile ($\phi^{(0)}(x_i,y_i)$), which is constructed by analytical functions or from the electrostatic potential of a nearby bias point.

- The second step is to compute the contact self-energy matrices (Σ_S and Σ_D), which describes how the channel couples to the S/D contacts and the self-energy matrix (Σ_s), if Σ_s not zero. And then, the S/D contacts are described by a chemical potential μ (μ_s, μ_d), which controls the carrier injection from the contacts into the channel.

- The third step is to solve the nonequilibrium Green's function equations for the Green's function (G) and the electron correlation function ($G^<$). Following this, the self-energies due to electron–phonon scattering are calculated.

- Then, the electron density (diagonal elements of $G^<$) is plugged into Poisson's equation in order to obtain updated electrostatic potential profile. And obtained new electrostatic potential profile served as an input to solve for updated nonequilibrium Green's functions and iterate the above process (outer left loop of Figure 2.3 until convergence is achieved.

▣ Simulated device structure and physical parameter

The structure of the simulated SiC (or Si) NWFETs is depicted in Figure 2.4(a), The SiO_2 oxide layers surrounding the Si channel are not subject to the transport calculation, but are included to compute the 3D electrostatic potential. The dimensions of the NWFETs are chosen to be close to the physical and theoretical limit (ballistic region: the sub-10nm dimensions) of MOS structures.

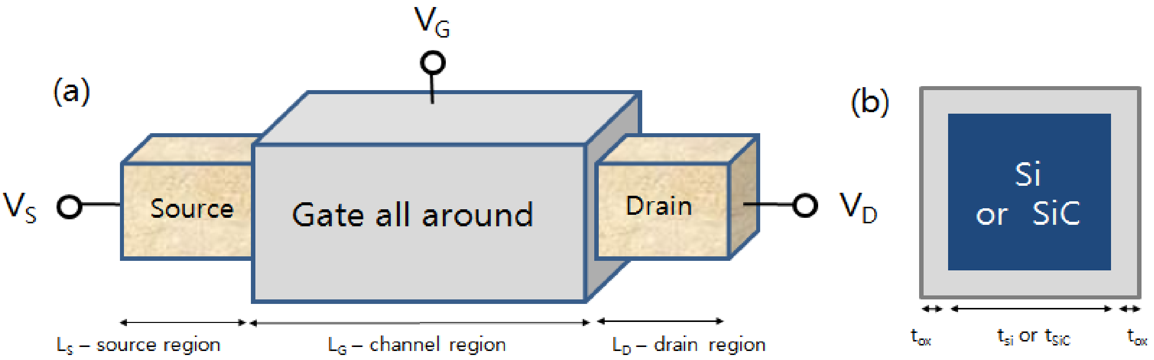

Figure 2.4 (a) Structure of the simulated NW transistor, (b) a cross-section view of NW channel.

Table 2.1 Parameters for the simulation of Si and 3C-SiC [4, 5].

Constant	Si	3C-SiC
x_mass	0.191 m_o	0.25 m_o
y_mass	0.191 m_o	0.25 m_o
z_mass	0.916 m_o	0.68 m_o
Mass density [g·cm^{-3}]	2.329	3.166
Lattice constant [Å]	5.43	4.3596
Electron acoustic deformation potential [eV]	14.6	24.6
Electron affinity [eV]	4.05	3.83
Conduction band energy difference with SiO_2 [eV]	3.0	3.6
Dielectric constant (ε_o)	11.7	9.72
Bandgap energy (eV)	1.12	2.3

The device feature is gate-all-around (GAA) FET using SiC (or Si) NWs as the conduction channel. The cross section of the silicon channel is 5×5 nm^2 and a gate oxide thickness (t_{ox}) of 1 nm is used as the dielectric materials (Figure 2.4(b)). We assume that there is no gate current through oxide tunneling. The source and drain extension regions are heavily n-doped (Si: $N_D = 10^{20}$ cm^{-3}, SiC: $N_D = 2\times10^{20}$ cm^{-3}) with abrupt doping profiles. Metallic gate with the mid-gap work function (Si: 4.6 eV and SiC: 3.9 eV) is assumed. If there is no mention, the length of the channel is 20 nm, which is long enough to prevent charge penetration from the doped regions so that the effective mobility can be exactly measured.

The SiC (or Si) NWs is along the [100] orientation, the effective-mass approximation is assumed for the six valleys of conduction band with m_t (Si: 0.191 m_o, SiC: 0.25 m_o) and m_l (Si: 0.916 m_o, SiC: 0.65 m_o), where m_t is the transverse effective masses, m_l is the longitudinal effective masses and m_o is the mass of the free electron. Other material parameters for simulation of Si and SiC are based on experimental values, as listed in Table 2.1.

2.2 Electrical transport of nanowire FET

2.2.1 Effective mobility

To evaluate the device performance of (simulated or fabricated) FET, it is important to analyze some key device parameters, such as effective mobility, on/off current ratio, current density and transconductance. Among those device parameters, the mobility is one of the most important parameters that determine the performance of FET and provide useful information on the transport phenomena.

The simulation results of Kotlyar *et al.* [6] and Jin *et al.* [7] showed that the electron mobility in Si NW decreases with decreasing channel diameter. They explained this phenomenon with electron phonon wave function overlap [6], because an increase of electron phonon wave function overlap with decreasing channel diameter results in increased electron phonon scattering rates and consequently lower electron mobility.
On the other hand, the experimental results and simulation results of Si NWFET [8, 9] showed higher mobility in Si NWs compared to planar MOSFETs. The reduced density of electron states (DOS) for scattering in 1-D wire transport devices gives an advantage over MOSFET and thereby an enhancement in the mobility.

In case of SiC NWs, experimental results of SiC FET show lower effective mobility (below 15 $cm^2 \cdot V^{-1}s^{-1}$) than that of its bulk counterpart (several hundred $cm^2 \cdot V^{-1}s^{-1}$), as we discussed in the section 1.4.2. Only a few studies have reported about the electron mobility of SiC NW in the ballistic regime [5]. In this subsection, it will be discussed the background theory of the effective mobility and simulated results of the Si and SiC NWFET.

The mobility can be extracted in the linear transport (V_{DS} = 10 mV) regime by using the expression (Eq 2.7).

$$\mu_{eff} = \frac{G\,L}{eN_{1D}} \qquad \text{Eq 2.7}$$

where L represents the channel length of device, G is conductance and N_{1D} is the one-dimensional charge density along the channel.

The conductance G is evaluated according to the Landauer–Büttiker formalism as (Eq 2.8).

$$\mathrm{G} = \mathrm{g}\frac{q^2}{h}\int dE\, T(E)\left[-\frac{df}{dE}(E-\mu_s)\right], \qquad \text{Eq 2.8}$$

where g denotes the degeneration coefficients (4 for Si, 2 for SiC), $T(E)$ is the transmission probability at a given energy (E), μ_s is the source chemical potential. From a theoretical point of view, a crucial point for calculation of mobility is how to correctly define the channel region to compute the charge density. The charge is not uniformly distributed over the whole channel region due to carrier penetration from the doped regions (source and drain). Therefore, a calculation of the charge density over the entire gated region gives rise to spurious results.

Figure 2.5(a) shows the effective mobility of SiC NWFET (cross sections of 5×5 nm^2 and L_G = 20 nm) with different gate voltage bias, which was extracted by using whole and reduced channel region integration. Here and in the following calculations, a low drain bias of V_{DS}= 10 mV is assumed, and the temperature is fixed at T= 300 K. In case of the whole channel region, the effective mobility was drastically reduced at the low gate bias region. This can be explained by taking into account the behavior of charge penetration from the (highly doped regions) contacts, as indicated in Figure 2.5(b).

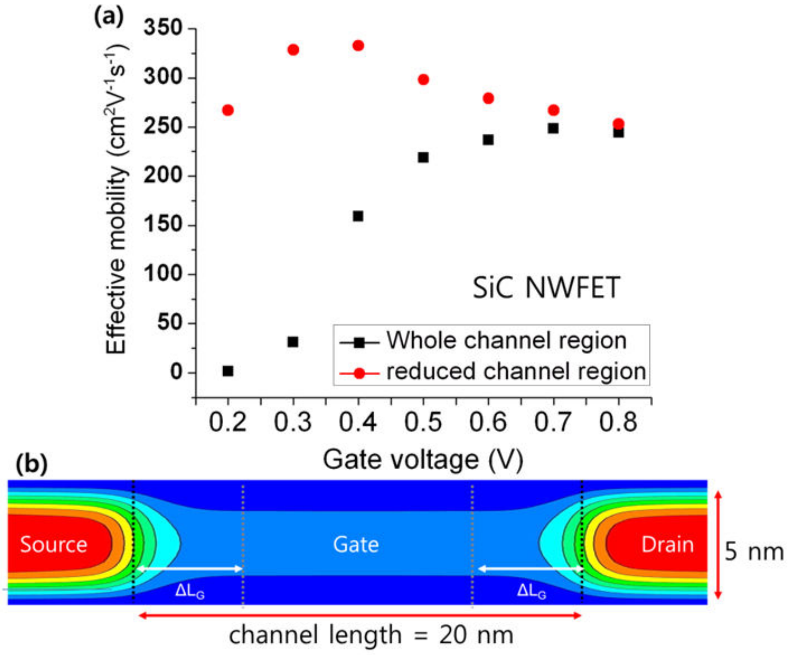

Figure 2.5 Extracted effective mobility of SiC NWFET with whole gated region extension integration (black symbol) and reduced channel region integration (red symbol), (b) reduced gate length for calculation of electron density, which prevents charge penetration from the contacts.

It is important to exclude the charge penetration from the doped regions for the estimation of the effective mobility in small devices. In experiments, the influence of doped drain and source regions can be hardly separated from the channel mobility. In case of simulation, we can simply eliminate this charge component by computing the linear charge density in a reduced region ($L_G - 2\Delta L_G$, L_G= 20 nm and ΔL_G= 5 nm) at the center of the channel. In this way, region for the calculation of charge density is restricted over a section of the gated region characterized by an almost uniform electron distribution (as shown in Figure 2.5(b)), which is not affected by the charge penetration from the contact.

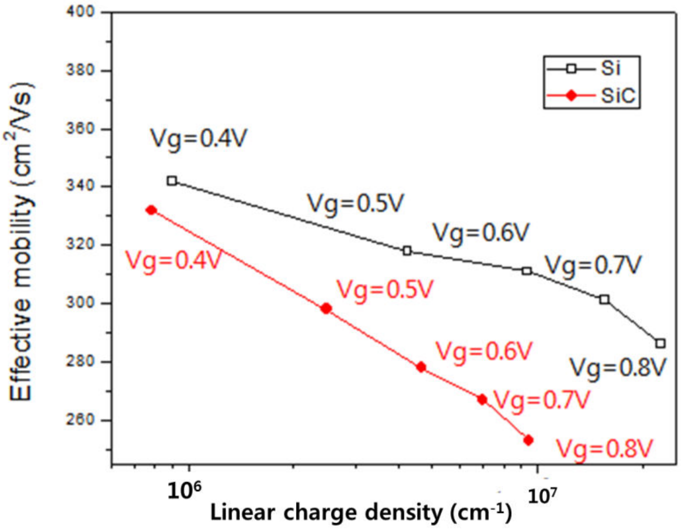

Figure 2.6 Effective mobility of electron of SiC and Si NWFET with different linear charge density.

Figure 2.6 shows the effective mobility of SiC and Si NWFETs with different linear charge density (N_{1D}). The effective mobility of SiC NWFET is smaller than that of Si NWFET. It is because the transverse effective mass of SiC NWFET is a little bit higher than that of Si NWFET (Si= 0.191 m_o, SiC= 0.25 m_o), which would lead to a faster decrease of the effective mobility. We observed a reduction of the effective mobility at large gate overdrive, above the threshold voltage (V_{th}= 0.4 V). The electron mobility decreases due to the effect of Fermi degeneracy in the ballistic case. The electron mobility of 3C-SiC and Si NWFET are 330 $cm^2 \cdot V^{-1}s^{-1}$ at N_{1D}= 9×10^6 cm^{-1} and 341 $cm^2 \cdot V^{-1}s^{-1}$ at N_{1D}= 8×10^6 cm^{-1}, respectively. The calculated electron mobility of 3C-SiC and Si NWFET exhibit higher value than the experimentally obtained electron mobility of their bulk counterpart with the corresponding carrier concentration (3C-SiC: 200 $cm^2 \cdot V^{-1}s^{-1}$ at N_{3D}= 3.2×10^{18} cm^{-3} [10] and Si: 230 $cm^2 \cdot V^{-1}s^{-1}$ at N_{3D}= 3.6×10^{18} cm^{-3} [11]). The mobility enhancement mainly comes from quantum confinement and the possibility of ballistic transport.

2.2.2 Surface roughness effect

Surface roughness (SR) scattering is main reason for mobility degradation in conventional MOSFETs at high transverse fields [12], because electrons are confined at the Si/SiO_2 interface by an electrostatic potential well. Under high gate voltage bias, the electrostatic potential well become thinner, more electrons are confined very near the interface. Therefore, If SR scattering increases, the effective mobility decreases.

Intuitively, SR scattering is even more deleterious effect in Si NWFET than in conventional planar MOSFETS structure because the influence of the interface Si/SiO_2 increases with the increase of the number of gates (multigate or gate-all-around structures). Moreover, as the device is scaled down, the ratio of the interface area to the channel volume increases. Therefore, larger fraction of carriers in the channel is significantly affected to the roughness of Si/SiO_2 interface, and it might reduce the performance of Si NWFET.

SR scattering in NWs is the key scattering mechanism [13] as it yields a reduction of the local density of states in the channel [14, 15], as well as an increase of threshold voltage [14]. Therefore, it seems worth critically examining SR scattering in the simulation of NWFET device.

▣ Surface roughness generation

The Si/SiO_2 interface roughness is implemented into the 3D simulator according to the following procedure [16]. We discretize the simulation domain with a 3D finite element mesh; each element is a rectangular with 0.2 nm height and width. And then, we produce the two-dimensional random distribution across the whole Si/SiO_2 interface according to an exponential auto-covariance function, which describe the statistics of the potential fluctuations $\Delta(\vec{r})$ in real space as (Eq 2.9):

$$C(x) = {\Delta_m}^2 e^{\frac{-\sqrt{2}x}{L_m}}, \qquad \text{Eq 2.9}$$

where L_m is the correlation length, Δ_m is the root mean square (RMS) fluctuation of the roughness, and x is the distance between two sampling points at the interface. Each particular realization of SR was generated by starting from the Power Density Spectrum (PSD) calculated by transforming the correlation function (Eq 2.10):

$$|\Delta(\vec{p})|^2 = \mathcal{F}(C(\vec{r})), \qquad \text{Eq 2.10}$$

where $|\Delta(\vec{p})|^2$ is the PSD and $\mathcal{F}$ is the Fourier transform.

Then, we generate a statistic of local fluctuations in the momentum space by adding a random odd phase

$\phi(\vec{q})$ to the square root of the PSD and finally anti-transformed into the real space (Eq 2.11):

$$\Delta(\vec{r}) = \mathcal{F}^{-1}\left(|\Delta(\vec{q})|e^{i\phi(\vec{q})}\right), \qquad \text{Eq 2.11}$$

▣ Simulation results

Figure 2.7 shows 3D structure of SiC NWFET (cross sections of 5×5 nm^2, L_G = 20nm) according to generated roughness with different RMS fluctuation (Δ_m).

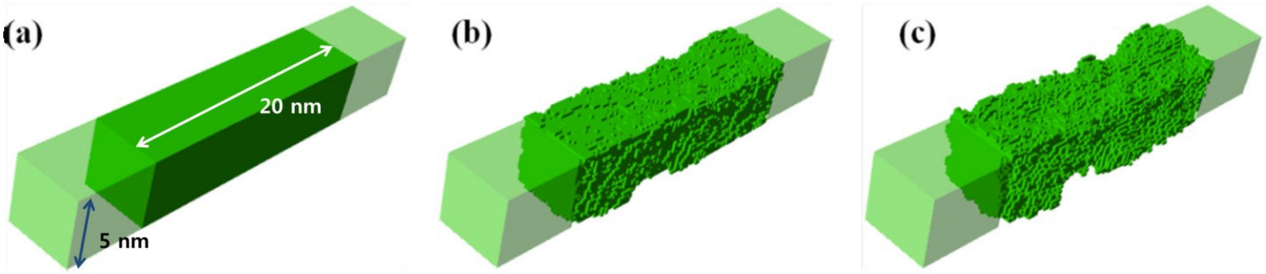

Figure 2.7 3D structures of SiC NWFET (a) without SR and with (b) SR (Δ_m=0.2 nm) and (c) SR (Δ_m=0.4 nm).

It has been observed a monotonic mobility reduction with increasing the roughness (Δ_m), as depicted in Figure 2.8(a). Such a large mobility reduction can be explained by sub-band fluctuation mechanism, because the conductance is physically limited by the smallest potential constriction generated by SR [16].

At low charge density, potential fluctuations are the main degradation mechanism. As expected, large SR (Δ_m) values resulted in lower conductance and effective mobility. Figure 2.8(b) shows the simulation results of the first sub-band profile according to SR. The sub-band fluctuation along the transport direction increases with increasing SR (Δ_m).

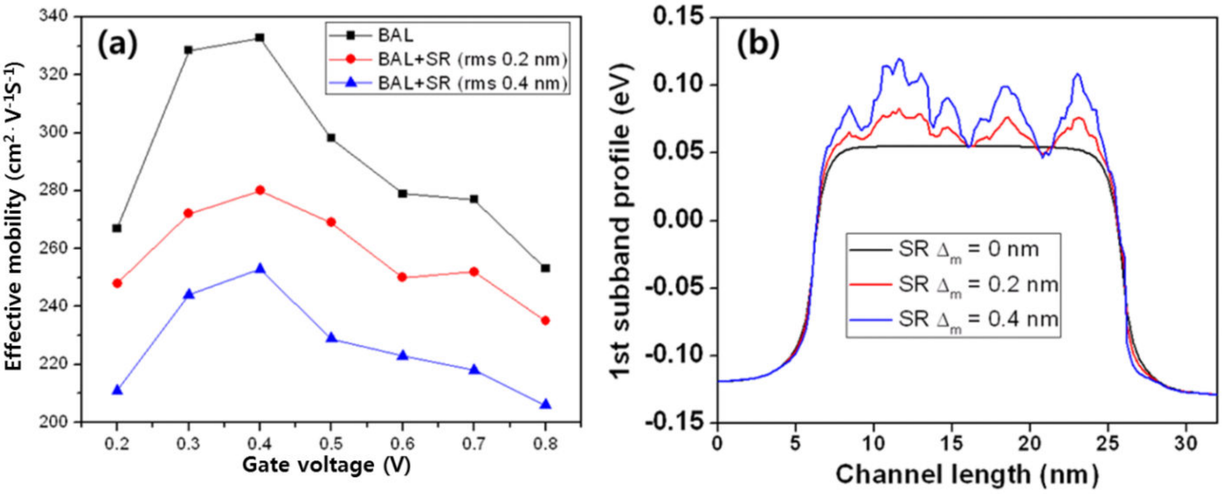

Figure 2.8 (a) Effective mobility of SiC NWFET as function of V_{GS} for different SR parameters. (b) First sub-band profile of SiC NWFET with different SR parameters.

Figure 2.9 shows the transverse cross section of the charge density in the SiC NW channel with/without SR (Δ_m=0.4 nm) at different V_{GS}. The white rectangular in Figure 2.9(a) indicates the Si/SiO$_2$ interface in ideal case. With increasing the gate voltage (Figure 2.9(a)-(c)), the contour plot of charge density for SR (Δ_m=0.4 nm) becomes denser, which means that the charge density is pushed towards the Si/SiO$_2$ interface by the high gate voltage. SR strongly modifies the shape of the charge densities and generates spatial irregularities compare to ballistic case (without SR scattering, Figure 2.9(d)) [16].

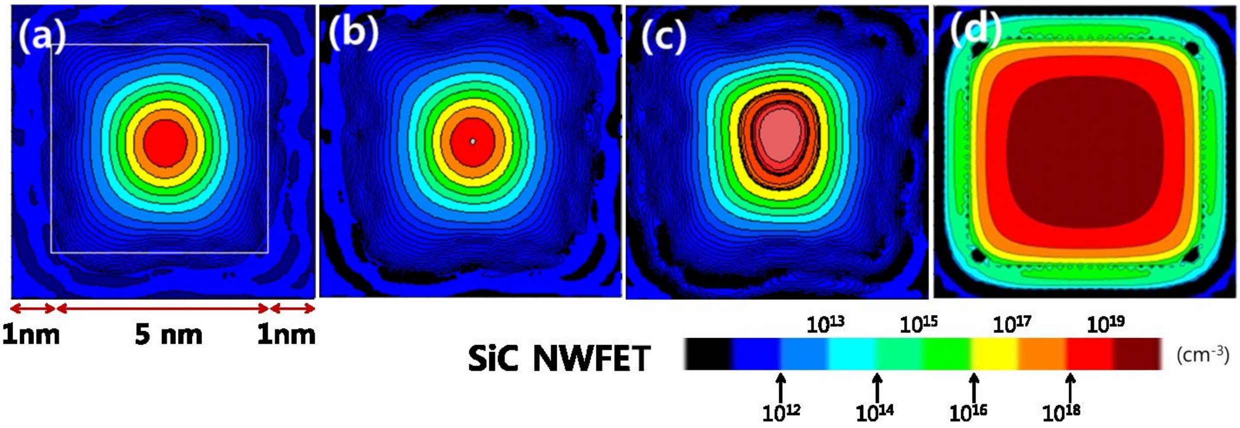

Figure 2.9 Transverse cross section of the charge density for slice in the channel region with SR (Δ_m=0.4 nm) at different V_{GS}, (a) V_{GS}=0.2V, (b) V_{GS}=0.5V, (c) V_{GS}=0.7 and without SR (Δ_m=0) at (d) V_{GS}=0.5V.

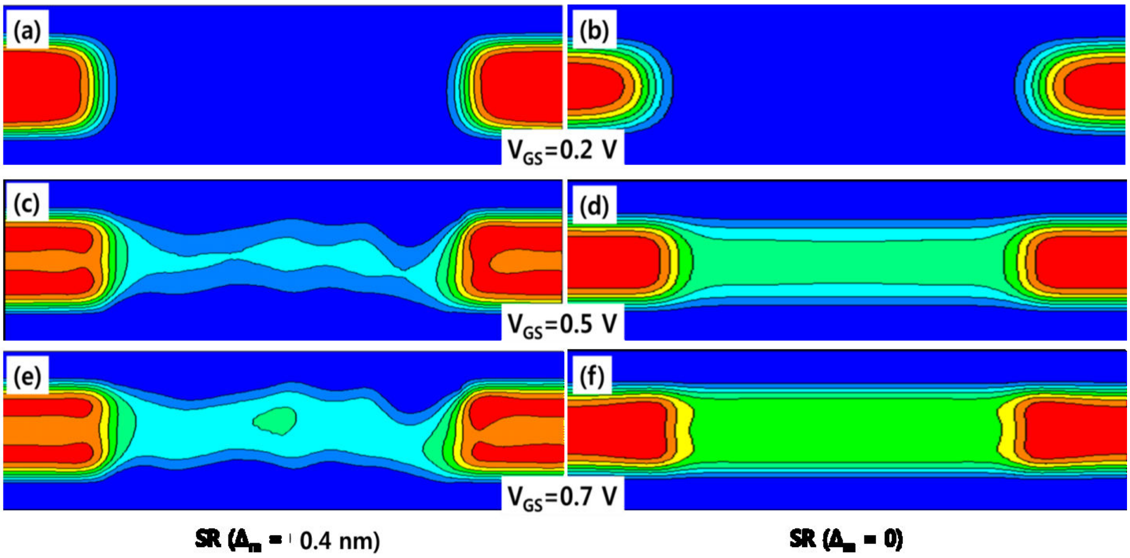

Figure 2.10 Charge density profiles of SiC NWFET along the transport direction according to different V_{GS} (a,c,e) with SR (Δ_m=0.4 nm) and (b,d,f) without SR (Δ_m=0).

Figure 2.10 shows the contour plot of charge density along the transport direction according to SR (Δ_m) for different V_{GS}. In case of ballistic transport, generated channel region with increasing the gate voltage is straight and wide, it shows uniform charge density profiles over the channel region. However, in case of including the SR scattering, potential energy fluctuation due to SR introduces strong spatial irregularities of the charge density. The effect of confinement variations on the electron concentration in the channel results in the meandering flux of the current. It is found that the SR-limited mobility is ruled by the two competing mechanisms of sub-band fluctuations and spatially disordered charge density fluctuations.

2.3 Simulation of thermoelectric properties of SiC and Si nanowires

A variety of electronic devices has been realized using NWs, ranging from FET and sensors to energy conversion devices. In particular, energy conversion devices with nanostructures have attracted significant interests in recent years to solve the global energy crisis. Energy conversion devices with NWs can be categorized into three different subtopics regarding photovoltaic, piezotronic and thermoelectric applications, generating the energy by harvesting light, mechanical and heat energy waste from the environment, respectively. Most of the world's energy resources are still generated by heat engines. If we assume that the efficiency of engine is around 30 – 40 %, roughly 15 terawatts of power are losing in the form of heat to the environment [17]. Therefore, if the electricity from "wasted heat" of heat engines is collected, amount of electricity would be saved.

In this section, the thermoelectric properties of SiC and Si NWs have been investigated. I will first explain and introduce the theoretical background of thermoelectric and thermal conductivity of SiC and Si NWs.

2.3.1 Theoretical background of thermoelectric properties

There are three effects involved in the thermoelectric phenomena, which are closely correlated with thermoelectricity, temperature and conductivity.

- ✓ Seebeck effect - converting temperature to current,
- ✓ Peltier effect - converting current to temperature,
- ✓ Thomson effect - conductor heating/cooling.

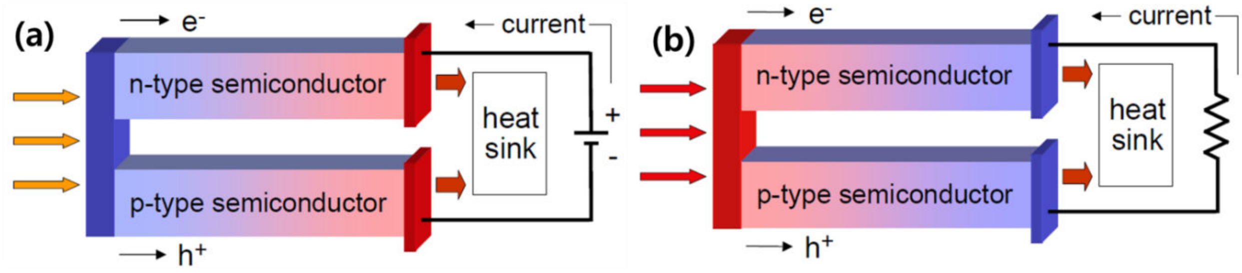

Figure 2.11 Schematic of thermoelectric: (a) power generator and (b) Peltier cooler [17].

▣ Seebeck, Peltier and Thomson effects

The Seebeck effect, which is named after the German physicist Thomas Johann Seebeck, is a phenomenon in which a temperature difference between two electrical conductors or semiconductors produces a voltage difference between the two materials. When heat is applied to one of the two conductors or semiconductors, heated electrons flow toward the cooler one. If the pair is connected through an electrical circuit, direct current flows through that circuit, as depicted in Figure 2.11(a).

When the temperature difference ΔT between the two ends of a material is small, then the Seebeck coefficient is defined by following equation (Eq 2.12):

$$S = -\left.\frac{\Delta V}{\Delta T}\right|_{I=0} \qquad \text{Eq 2.12}$$

The voltages produced by Seebeck effect are small, usually only a few microvolts per Kelvin.

Peltier effect is the reverse of Seebeck effect. Peltier effect shows that electricity can cause a heat difference at the junction of two different materials connected together (see Figure 2.11(b)). Seebeck and

Peltier effects can be related to a third, the Thomson effect, which describes the heating or cooling of a current-carrying conductor with a temperature gradient. These three effects are different components of the same scientific principle.

▣ Figure of merit (ZT)

The performance of a thermoelectric device is characterized by the figure of merit ZT (zero dimension value), which can be calculated by Eq 2.13.

$$\mathrm{ZT} = \frac{TS^2G}{\kappa_e + \kappa_{ph}} \qquad \text{Eq 2.13}$$

where Z is a measure of a material's thermoelectric properties [K^{-1}], T is temperature [K], S is the Seebeck coefficient [$\mathrm{V{\cdot}K}^{-1}$] , G is the electrical conductance [Ω^{-1}], and κ is the thermal conductance [$\mathrm{W{\cdot}K}^{-1}$], which is the sum of the electron (κ_e) and phonon (lattice vibration) (κ_{ph}) contributions. In particular, the numerator of Z (S^2G) is called power factor and defines the electrical performance of the thermoelectric material.

Good thermoelectric materials must have a high thermoelectric figure of merit ZT. In order to maximize ZT, S should be large so that a small temperature difference can induce a large voltage difference at both contacts. G should be large to maximize the available charge carriers contributing to the thermoelectric effect. Lastly, thermal conductance (κ) should be as small as possible to maintain the temperature gradient between both contacts. However, the quantities S, G and κ are not mutually exclusive, but inter-related (or coupled with each other). Therefore, it is very difficult to control these variables independently. Main attribution of nanostructures is the possibility to achieve high ZT by reducing the phonon thermal conductance (κ_{ph}) through the confinement and to enhance scattering of phonons, without significantly reducing electrical conductivity.

The electrical conductance, Seebeck coefficient and electron thermal conductance is computed within the framework of the quantum-transport theory of Landauer–Büttiker [18] (Eq 2.14 to Eq 2.16):

$$\mathbf{G} = \mathbf{g}\frac{\boldsymbol{q}^2}{\boldsymbol{h}}\int_{-\infty}^{\infty} \boldsymbol{T(E)}\left(-\frac{\partial \boldsymbol{f}}{\partial \boldsymbol{E}}\right)\boldsymbol{dE}, \qquad \text{Eq 2.14}$$

$$\mathbf{S} = -\frac{\mathbf{1}}{\boldsymbol{qT}}\int_{-\infty}^{\infty} (\boldsymbol{E}-\boldsymbol{E_f})\,\boldsymbol{T(E)}(\boldsymbol{f_1(E)}-\boldsymbol{f_2(E)}\boldsymbol{dE} \;\Big/\; \int_{-\infty}^{\infty} \boldsymbol{T(E)}(\boldsymbol{f_1(E)}-\boldsymbol{f_2(E)}\boldsymbol{dE}\,, \qquad \text{Eq 2.15}$$

$$\kappa_e = \frac{\mathrm{g}}{h\mathrm{T}}\int_{-\infty}^{\infty} T(E)(E-E_F)^2\left(-\frac{\partial f}{\partial E}\right)dE - TS^2G\,, \qquad \text{Eq 2.16}$$

where g denotes the degeneration coefficients (4 for Si, 2 for SiC), q is the electronic charge, h is the Planck constant, $T(E)$ is the transmission possibility at a given energy E, E_F is the Fermi level at the contact, f_1 and f_2 are equilibrium Fermi–Dirac distributions for the contacts.

The phonon thermal conductance for Si NW is computed by the following equation (Eq 2.17).

$$\kappa_{ph} = \int_0^{\infty} \frac{d\omega}{2\pi}\left(\frac{\hbar\omega}{kT}\right)\widetilde{\mathrm{T}}(\omega)\frac{e^{(\hbar\omega/kT)}}{(e^{(\hbar\omega/kT)}-1)^2}\;, \qquad \text{Eq 2.17}$$

where ω is phonon frequency, $\widetilde{\mathrm{T}}(\omega) = \mathrm{Tr}\left[\tilde{\Gamma}_S\widetilde{D}\tilde{\Gamma}_D\widetilde{D}\right]$ is the transmission probability of the phonon and $\tilde{\Gamma} = i\left(\tilde{\Sigma} - \tilde{\Sigma}^{+}\right)$. $\widetilde{\mathrm{D}} = [(\omega^2 + \mathrm{i}\eta^{+}) - \mathrm{D} - \tilde{\Sigma}(\omega)]^{-1}$. D is the dynamical matrix which can be computed by using a valence force model [19].

2.3.2 Simulation results of thermoelectric properties of SiC nanowires

▣ Comparison of power factor: SiC and Si nanowires

Our group has demonstrated that SiC NWFETs have shown similar electrical characteristic compared with Si NWFETs in the ballistic regime at room temperature [5]. In this study, the thermoelectric behavior of SiC and Si NWs has been investigated. Figure 2.12 shows *S*, *G*, and S^2G of SiC and Si NW with square cross section (5×5 nm^2) as a function of carrier concentration at 300 K.

S of SiC and Si NW linearly decreased with increasing the carrier concentration at a logarithmic scale because E_F moves close to E_c in Eq 2.15. *S* of Si NW is slightly larger (~ 20%) than that of SiC NW. *S* is closely related to the band structure, higher *S* of Si NW than that of SiC NW might be attributed to narrow DOS distribution [20]. *G* increases with increasing carrier concentration because more carriers are available to transport charge. *G* of SiC NW is also smaller than the one of Si devices. It might be due to the different transport masses of the unprimed valleys (transverse effective mass), $m_t = 0.19\ m_o$ for Si and $m_t = 0.25\ m_o$ for SiC [5]. Consequently, it leads to a faster decrease of the *G* and effective mobility than Si NWs.

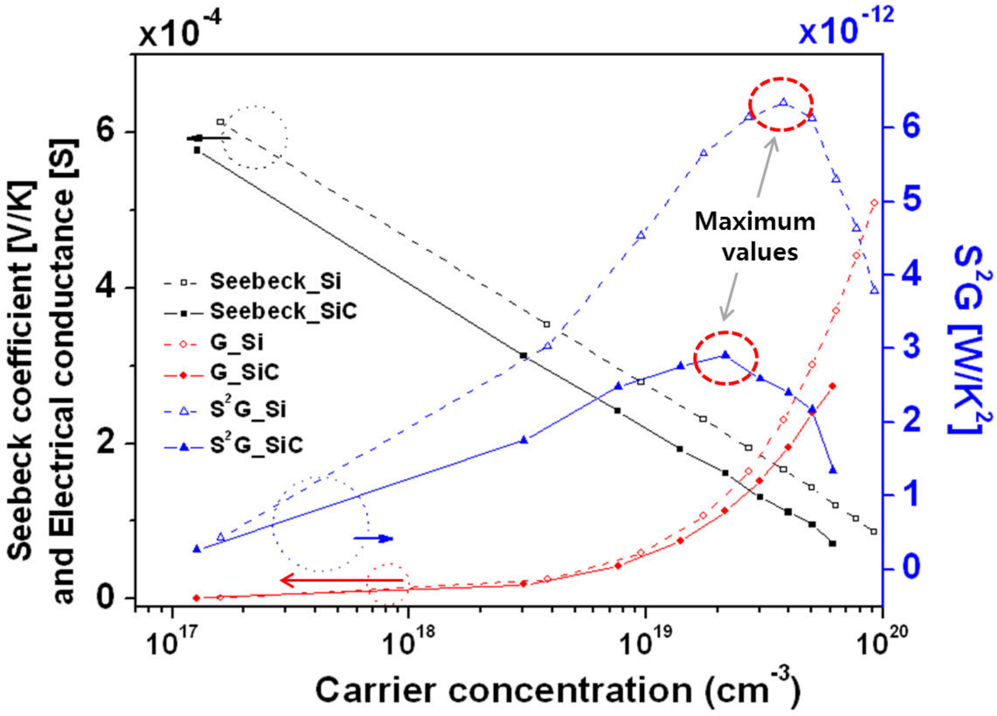

Figure 2.12 Seebeck coefficients, electrical conductance, and power factor for Si and SiC NW (5×5 nm^2) as a function of carrier concentration at 300 K.

S decreases with increasing carrier concentration, while *G* increases as the carrier concentration increases. Therefore, S^2G has the maximum value of power factor (PF_{max}) at a certain carrier concentration (N_{max}). PF_{max} of SiC NW is almost twice smaller than that of Si NW due to the combination of large band-gap and transverse effective mass. Generally, experimental measured thermal conductivity of SiC bulk (300 W·m^{-1}K^{-1}) and NW with similar diameters (80 W·m^{-1}K^{-1} for 60 nm [21]) are roughly two to three times higher than the one of Si bulk (150 W/mK) and NW (25 W·m^{-1}K^{-1} for 56 nm [22]). Therefore, the ZT of SiC NWs is roughly one-fourth to one-sixth of that of Si NWs at room temperature.

From numerical calculation, it is obvious that SiC NW is a poor thermoelectric device compare to Si NW at room temperature. This could be predicted because of the high thermal conductivity of SiC. However, SiC NWs might be promising materials for thermoelectric elements operating at high temperature due to its wide band gap and low intrinsic carrier concentration, while Si NW cannot operate above 500K and even less. Therefore, it is still worthwhile to investigate thermoelectric properties of SiC NW operating at high temperature.

▣ Dimension and temperature effect on power factor of SiC nanowires

Figure 2.13 shows S, G and S^2G of SiC NW with different cross sections (2.05×2.05, 2.92×2.92, 4.21×4.21 nm^2) versus a carrier concentration at 500 K. The increase in transverse dimension of NWs leads to the modification of its band structure: reduce the band gap; and widen the sharp DOS peaks [20]. These two effects have deleterious effect on S. As a result, S decreases with increasing a cross-sectional area, while G increases due to the increment of the numbers of modes, which are contributing to the carrier transport.

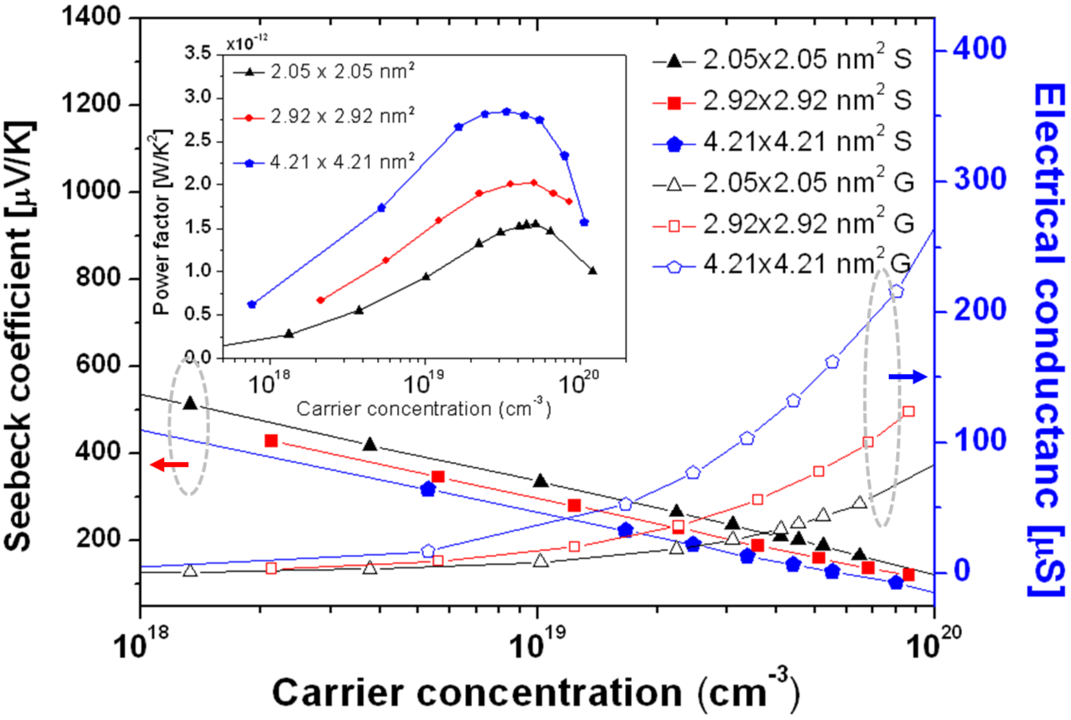

Figure 2.13 Seebeck coefficients and electrical conductance (inset: power factor) of SiC NW with difference cross sections as a function of carrier concentration at 500 K.

The power factor is determined by the two competitive factors: S and G. Increase rate of G with increasing the cross section is higher than decrease rate of S^2, therefore PF_{max} increases with transverse size increasing (the inset of Figure 2.13). Figure 2.14 shows thermoelectric coefficient (S, G and S^2G) of SiC NW (2.05×2.05 nm^2) with different temperature versus a carrier concentration at 500 K.

Theoretically, the Fermi level (E_F) decreases with increasing the temperature. So, S increases when the temperature is raised, because the term ($E - E_F$) in numerator of S (Eq 2.15) increases without dramatically changing other parameters. On the other hand, G decreases with increasing temperature due to the increase of optical and acoustic phonon scatterings. The S^2 increases larger than the decrease of G with increasing temperature. Hence, PF_{max} is gradually increasing with increasing the temperature (the inset of Figure 2.14). The graph of S^2G appears more spread in the *x*-axis (carrier concentration) as the temperature increases. N_{max} shifts to higher carrier concentration as temperature increases.

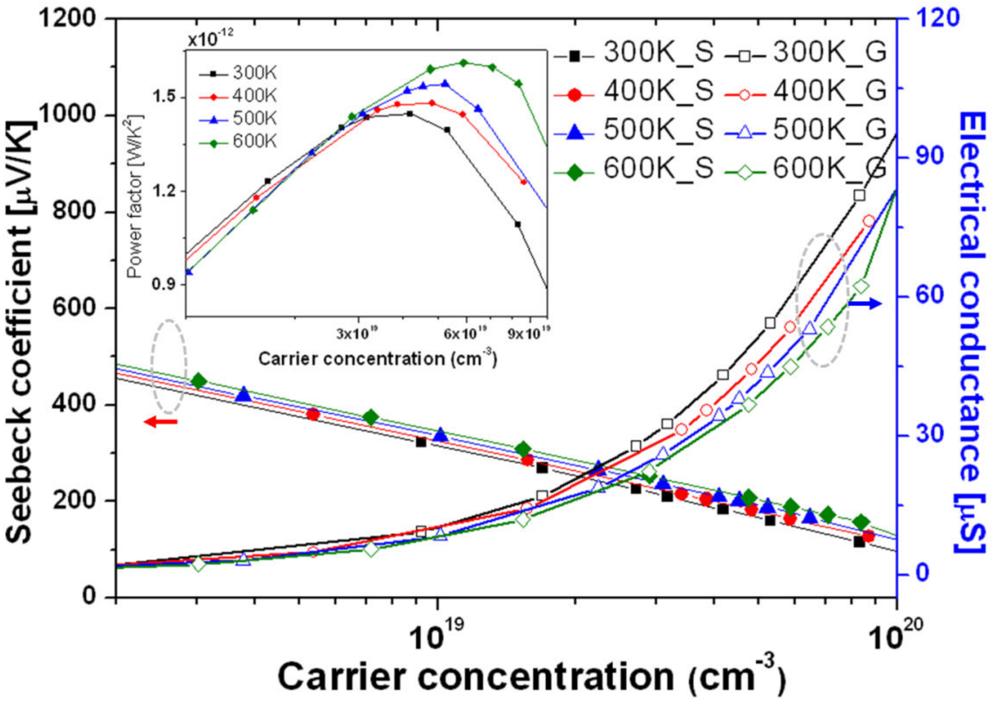

Figure 2.14 Seebeck coefficients and electrical conductance (inset: power factor) of SiC NW (2.05×2.05 nm^2) with difference temperature as a function of carrier concentration.

Thermal conductance of SiC nanowires

The total thermal conductance consists of the electron (κ_e) and phonon (lattice vibration) (κ_{ph}) thermal conductance. Electron contribution of the thermal conductance of SiC NW is easily calculated by Eq 2.16, but the calculation of phonon (lattice) thermal conductance for SiC NW by NEGF formalism (Eq 2.17) is not established yet.

Phonon (lattice) thermal conductance of nanostructures has been calculated by several methods, such as BTE [23], MC [24], Molecular dynamics (MD) [25], NEGF [26]. The BTE and MC are well-known and applicable to a wide range of nanostructures, but these methods are strongly depending on experimental results to assume the effective relaxation time [27]. Therefore, these methods are not suitable for the calculation of thermal conductance in ballistic region because there are no experimental results for sub 20 nm diameter NWs. Non-equilibrium MD (NEMD) and NEGF have been studied for the calculation of thermal conductance of SiC NWs. NEGF formalism is powerful method to describe the phonon transport as well as the electron transport in ballistic region. Xu *et al.* [28] have calculated the thermal conductance with various defects based on NEGF formalism for temperature from 0 to 1000 K. However, there is no schematic study of lattice thermal conductivity about quantitative expression of size dependence in SiC NWs, which limits the quantitative calculation of size dependent ZT. NEMD is another powerful model to predict the lattice thermal conductivity of NW in ballistic regions. NEMD approach can compute the thermal conductivity in the ballistic regions without any assumptions on the nature of the scattering mechanisms [29]. Papanikolaou [29] has calculated the lattice thermal conductivity of SiC NWs with different temperature, size and also has considered the effect of different wire surfaces (Si and C) terminations. This simulated lattice thermal conductivity [29] has been implemented in our calculation of thermoelectric properties of SiC NWs.

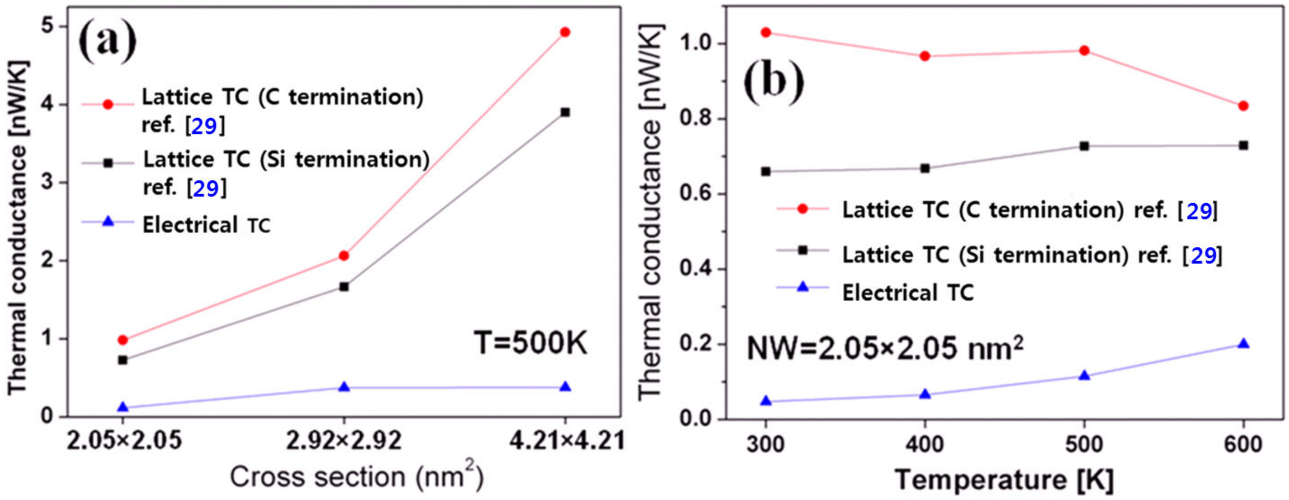

Figure 2.15 Thermal conductance of SiC NWs (a) with different cross sections at 500K and (b) with different temperatures at 2.05×2.05 nm^2.

The calculated lattice thermal conductivity from [29] is converted into thermal conductance. Figure 2.15(a) and (b) show the electric and lattice thermal conductance with different square cross sections at 500 K and different temperatures with 2.05×2.05 nm^2 cross sections, respectively. The electron thermal conductance is much lower than the lattice thermal conductivity. The electron thermal conductance increases with increasing the cross sections and temperature. An interesting observation is that thermal conductance is gradually reduced with decreasing the cross sectional areas. Decreasing the cross section of NWs increases the surface to volume ratio, so more phonons are diffusely reflected at the surface [26]. Consequently, it leads to the reduction of phonon mean free and lattice thermal conductivity of NWs.

The lattice thermal conductivity depends sensitively not only on the cross section of NWs but also on surface terminations (Si and C) of NWs. In all case, Si terminated SiC NW has lower thermal conductance than C terminated SiC NW. He proposed that it might be due to stronger scattering on a more disordered Si surface compared to the C one. Lattice thermal conductance shows small variation for temperatures range 300 - 600 K, except the C terminated wires at 600 K. The sudden decrease of thermal conductivity for C terminated NWs at T= 600 K might be attributed to temperature induced disorder, which explained by the Tersoff potential for SiC [30].

▣ Figure of merit ZT

The ZT has been evaluated according to a cross sections and temperature with consideration of both C and Si terminations (Figure 2.16). The ZT is determined by two competitive factors; power factor and thermal conductance. Hence, ZT increases monotony with decreasing the cross sections at 500 K. ZT of SiC NW with cross section 2.05×2.05 nm^2 increases with increasing temperature and reaches a value of 0.93 - 1.04 at 600 K.

This ZT enhancement mainly comes from a drastic reduction of thermal conductance through the enhanced scattering of phonons, without significant reduction of S and G. It indicates that quantum confinement effects play an important role on thermoelectric properties of SiC NW. Because the calculation of thermal conductance depends on surface terminations, the dependency of ZT on the surface termination on SiC NW could be calculated quantitatively. The ZT of Si terminated NW has a larger value than that of C terminated SiC NW due to the lower lattice thermal conductance.

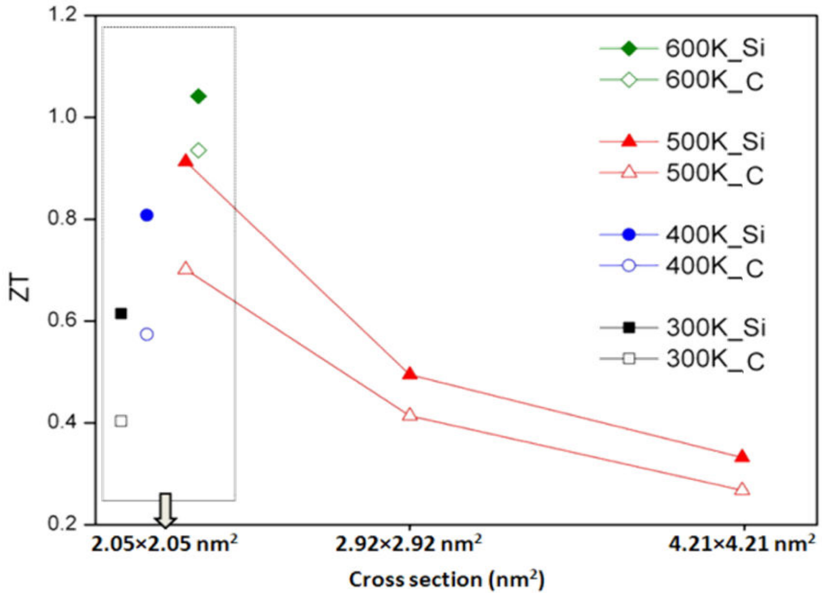

Figure 2.16 ZT of SiC NW according to cross section and temperature with both C and Si terminations.

ZT increases as the temperature increases at a cross section 2.05×2.05 nm^2, and it reaches ZT higher than 1 with Si termination at 600 K, which is 8 times larger than experimentally reported the highest ZT value of SiC thin film (0.125 at 973K) [31]. However, achieved maximum ZT value (1.04) is slightly smaller than previous reported value (1.78) [28].

2.3.2 Simulation results of thermoelectric properties of Si nanowires

Bulk Si is also not a very good candidate for thermoelectric conversion devices. Recently, efficient thermoelectric Si NWs have been reported: a ZT of about 0.6 has been measured at room temperature while the value for bulk Si is only 0.001. The reduction of thermal conductance by optimizing the roughness is responsible for this enhancement, which is two orders of magnitude from its bulk material value, and can be as low as k =1- 2W·m^{-1}K^{-1}[22].

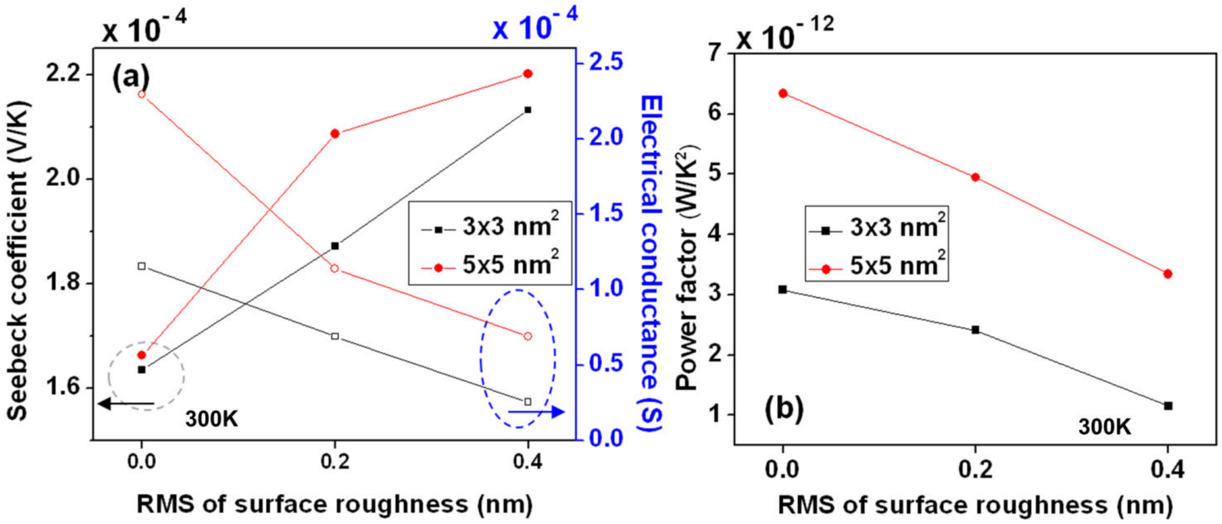

Figure 2.17 (a) Seebeck coefficient and electrical conductance,
(b) power factor of Si NW according to the SR with different cross sections.

In particular, SR is key issue to enhance the thermoelectric device performance by engineering phonons and electrons. However, the theoretical calculation of thermoelectric properties according to SR is less explored. In this work, it has been investigated that the theoretical calculation of thermoelectric properties of Si NWs according to the SR with different cross sections (3×3 and 5×5 nm^2) in the ballistic regime at room temperature.

Figure 2.17 shows S, G, and S^2G of Si NW with different square cross section (3×3 and 5×5 nm^2) as a function of the SR (Δ_m) at 300 K. G decreases with increasing the SR (Δ_m) in both cases (3×3 and 5×5 nm^2), because SR creates large fluctuations of the effective-potential profile seen by electrons [13], as shown in Figure 2.8(b). However, S increases when the SR (Δ_m) is raised, because the term (E - E_F) in numerator of S (Eq 2.15) increases without dramatically changing of other parameters.

The power factor (S^2G), which shows the electrical performance of the thermoelectric materials, monotonically decreases with increasing the SR (Figure 2.17(b)). SR strongly modifies the shape of the two spectral densities (the conductance and the carrier spectral densities) characterized by sharper peaks with respect to the ballistic case [13].

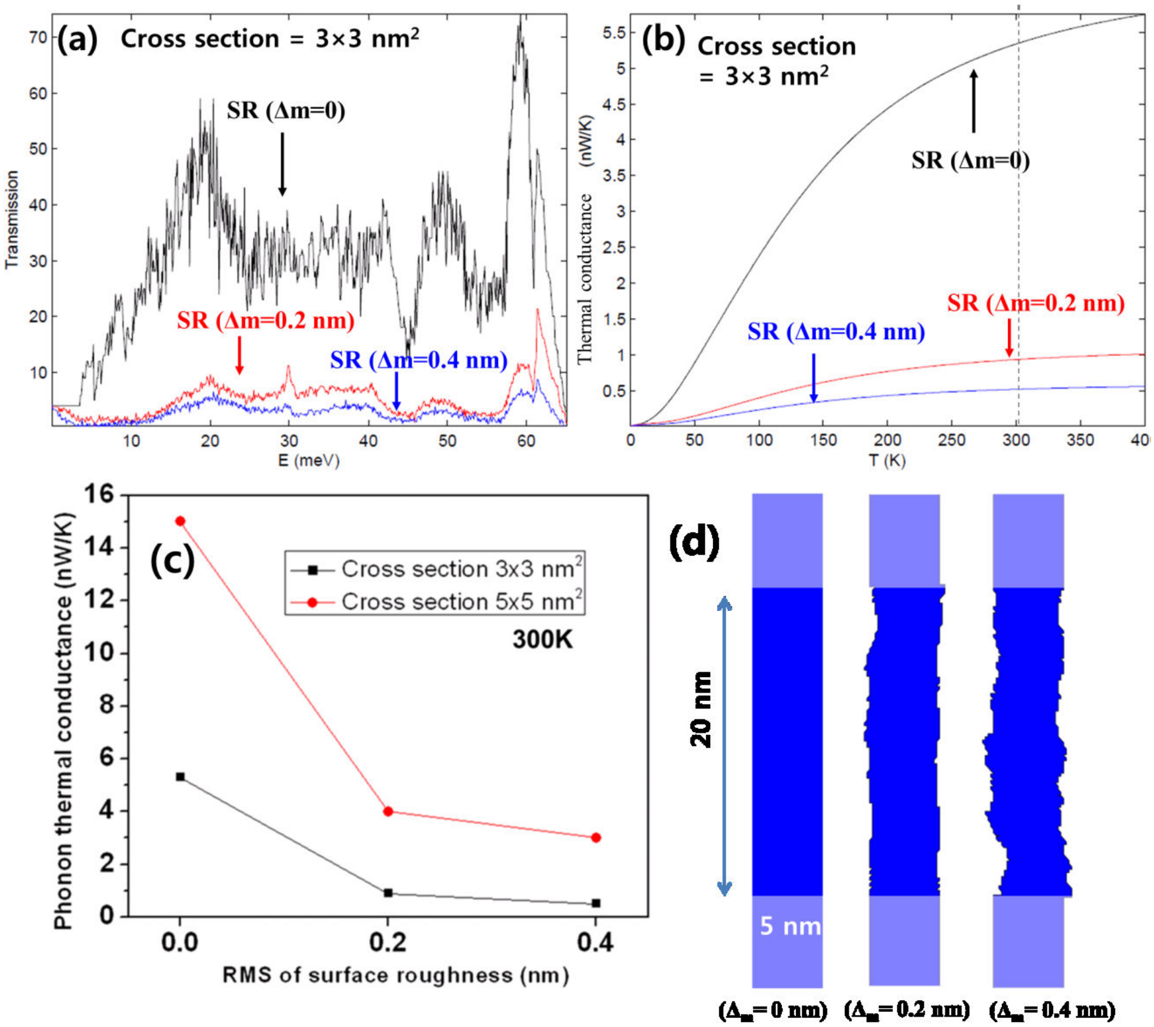

Figure 2.18 (a) Phonon transmission and (b) thermal conductance according to temperature through perfect and rough (Δ_m= 0.2 nm and 0.4 nm) Si NWs with cross section 3×3 nm^2. (black: without SR (Δ_m = 0 nm), red: SR (Δ_m = 0.2 nm), blue: SR (Δ_m = 0.4nm)), (c) phonon thermal conductance according to the SR with different cross sections, (d) morphology of Si NW's cross section along axial direction with different RMS of SR (Δ_m= 0, Δ_m= 0.2 nm, Δ_m= 0.4 nm).

Phonon thermal conductance of Si NW is computed within the framework of NEGF with a valence force model. The phonon transmission as a function of SR (Δ_m) with a cross section of 3×3 nm^2 at room temperature is shown in Figure 2.18(a). The phonon transmission through rough Si nanowires is strongly reduced around energies where the confined phonon subbands are almost flat [32]. Figure 2.18(b) shows the thermal conductance according to temperature through perfect and rough (Δ_m= 0.2 nm and 0.4 nm) Si NW with cross section 3×3 nm^2. The thermal conductance considerably decreases with increasing the SR (Δ_m) due to the degradation of thermal transport caused by SR.

Figure 2.18(c) shows the phonon thermal conductance according to the SR with different cross sections at room temperature. The results obtained Si NW for the cross section (3×3 nm^2) shows lower thermal conductance than that of cross section (5×5 nm^2) due to increased surface scattering. In addition, phonon thermal conductance considerably decreases with increasing the SR (Δ_m). Figure 2.18(d) shows the morphology of Si NW's cross section along axial direction with different RMS of SR (Δ_m) for the cross section (5×5 nm^2) and gate length (L_G) of 20 nm.

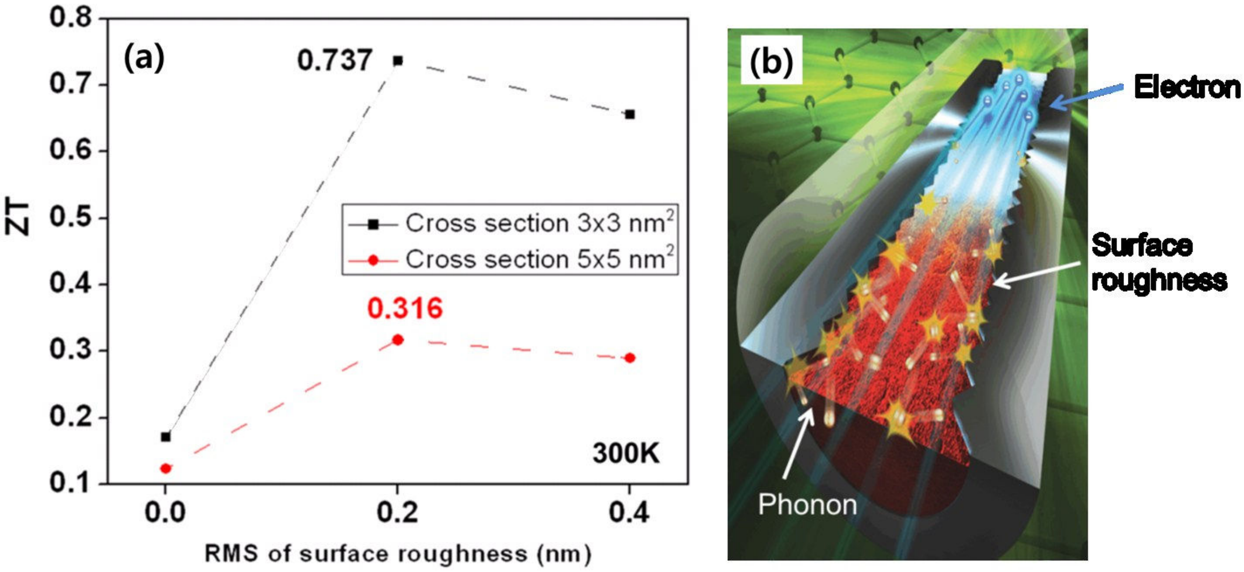

Figure 2.19 (a) ZT of Si NW according to the SR with different cross sections.
(b) Schematic illustration for the transport of electron and phonon in a rough NW [33].

Figure 2.19(a) shows ZT with two different square cross sections (3×3 and 5×5 nm^2) as a function of the SR (Δ_m). ZT has maximum value (0.737 for 3×3 nm^2 and 0.316 for 5×5 nm^2) at the SR of Δ_m= 0.2 nm. At a small SR (Δ_m =0.2 nm), ZT is increased because phonon thermal conductance decreases faster than the power factor with decreasing the wire cross sections. This enhancement is responsible for the modulation of electrons and phonons. It may be that thermal transport is impeded as phonons simply bounce off the rough surface of the NWs in Figure 2.19(b), however current flow is not impeded, as electrons maintain the stream toward the transport direction.

But, at a large SR (Δ_m= 0.4 nm), ZT is decreased because the decremented rate of electrical transport induced by the SR is higher than the one of phonon transport. The calculated ZT value (0.737) of Si NW for the cross section (3×3 nm^2) with the SR (Δ_m= 0.2 nm) is comparable to the highest experimental ZT value of Si NW (0.6) [22].

2.4 Conclusion

In this chapter, electrical transport and thermoelectric properties of 3C-SiC and Si NWs have been investigated. The calculated mobility of 3C-SiC NWFET operating in the ballistic regime (5 nm) is about 90% of Si ones, which is a direct result of the transverse effective mass difference of the two semiconductors. Large SR (Δ_m) values resulted in lower conductance and effective mobility of SiC NWFET. It is found that the SR-limited mobility is ruled by the two competing mechanisms of sub-band fluctuations and spatially disordered charge density fluctuations.

For the thermoelectric properties of 3C-SiC NW, it has been employed a combination of NEGF for the electrical transport and NEMD for the lattice thermal transport in the ballistic regime to predict the thermoelectric figure of merit. We have explored the thermoelectric behavior of 3C-SiC NWs as a function of temperature and wire square cross sections (varying from 2.05×2.05 to 4.21×4.21 nm^2). The expected ZT has been estimated using the calculated upper limit of the power factor. The ZT of Si terminated SiC NWs reaches a maximum value of 1.04 at 600K. SiC NWs doesn't show high thermoelectric efficiency compare to Si NW at room temperature, while SiC NWs is expected to be promising at higher temperature region due to wide gap characteristics.

NEGF formalism has been used for the electrical transport and the calculation of thermal conductivity to estimate thermoelectric properties of Si NW. ZT of Si NW is enhanced with an appropriate SR (Δ_m =0.2 nm), which is responsible for a drastic reduction of thermal conductance without significant reduction of electrical conductance. At high SR (Δ_m= 0.4 nm), ZT is decreased because electrical transport is impeded larger than phonon transport. The ZT of Si NW for the cross section (3×3 nm^2) with the SR (Δ_m= 0.2 nm) is comparable to the highest experimental ZT value of Si NW (0.6).

We have calculated the thermoelectric enhancement in SiC and Si NWs by studying the complex interplay of the size of NWs, temperature and SR. Main attribution of nanostructures is the possibility to achieve high ZT by reducing the phonon thermal conductance (κ_{ph}).

Enhancement of ZT value of NWs has the potential to be further improved by the following approaches: In case of SiC NW, the implement of polycrystalline, twin structures or SR could eventually lead to the targeted device performance by reducing the thermal conductance. In case of Si NW, ZT could be further improved by applying an appropriate doping, vacancy and defects. However, these effects also lead to the degradation on electrical properties.

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Chapter 3. Fabrication of SiC nanostructures by top-down method

3.1 Introduction

To realize SiC NW-based nanoelectric devices, such as field-effect transistors (FET), it is essential to start with a high quality single crystalline SiC material at the nanoscale. Currently, a common technique for the development of SiC NWs is the bottom-up approach, such as VLS [1] or VS [2] methods. Critical problem of these methods is that as-grown SiC NWs present a high density of structural defects, such as stacking faults.

In the contrary, a top-down approach by using SiC substrates can enable a precise control of the geometry of NWs, such as diameter, length and location of the NWs on the substrate. It also can minimize defects, such as stacking faults, which are formed during the growth of SiC NWs. The application of SiC for devices relies heavily on the quality of SiC epitaxies. The technology of SiC bulk and homo-epitaxial growth has been developed over the past few years and has shown commercial availability of SiC substrates of ever-increasing diameter and quality. Therefore, if the top-down approach is applied into a high quality SiC substrate, high crystalline SiC NWs with less defects density and with controlled doping level could be achieved.

Even though the price of SiC substrate is still relatively more expensive than Si substrate, if single crystalline SiC nanostructures are realized by top-down approach, it doesn't suffer from high density of stacking faults and unintentional doping (n-type, 10^{20} cm^{-3}). Therefore, it will allow the study of electrical properties of single crystalline SiC nanostructures. In addition, it opens new possibilities to apply it in widespread applications, such as bio-sensor based on SiC NWs, robust nanoneedles for AFM probes and field emitters.

The main interests of this section are in the realization of SiC nanostructures by top-down approach, in particular, using Inductively Coupled Plasma (ICP) etching technique. First, the fundamentals of plasma etching processes and influence of etching parameters are addressed in section 3.2. And then, experimental results of SiC nanostructures by using dry etching technique are presented in section 3.3.

3.2 Dry etching of SiC

In a top-down process, the etching plays an importance role to obtain defined patterns by removing or remaining certain area of target substrates. The etching methods are commonly classified into two types, wet and dry etching. There are several reports about the wet (or chemical) etching technique for Si NWs, but wet etching of SiC is not available in conventional acid or base solutions at normal temperature, due to chemical stability and inertness. Indeed, the high bond strength between Si and C makes SiC useful for high-temperature operation, but it becomes problematic in case of the technological processes of SiC. Wet etching of SiC can only be performed with high concentration of molten salts at high temperature, which is incompatible with conventional micro and nano electronic process. SiC dry etching is preferable than wet etching since it can be processed at lower temperature. It also provides high selectivity of etching with respect to the mask material. As a result, anisotropy of nanoscale SiC nanostructures could be achieved by dry etching [3].

For the dry etching of SiC, ICP is widely used than the Reactive-Ion Etching (RIE). ICP can generate much higher high-density plasma (>10^{11} cm^{-3}) than RIE (>10^{9} cm^{-3}) [4], which leads to higher etch rate of SiC. The operating pressure (1 - 2 mTorr) of ICP is much lower than in RIE systems (10 - 300 mTorr) [4]. High plasma density allows higher sputtering able to break Si-C bonds and the operation at low pressure improves the directionality of the ion flux, which enables the achievement of anisotropy profile with smooth surface without residue. The main problem of conventional RIE for SiC etching is residual surface damage due to the high dc self-bias, which leads to a rougher surface, but high density and low energy ions of ICP give better selectivity and less surface damage than RIE. In addition, a separate RF bias is applied to the substrate to create directional electric fields near the substrate to achieve more anisotropic etch profiles. Therefore, plasma density and sputtering energy can be independently controlled, thereby increasing flexibility in optimizing etch parameters.

In this section, top-down approach is addressed for SiC nanostructures via ICP etching in SF_6/O_2 based gas mixture. Before going into experimental results, the etching mechanism of SiC and the effect of etching parameters will be explained.

3.2.1 Etching mechanism of plasma-based process

When etching SiC using an SF_6/O_2 plasma, the dominant etch limiting factor is the breaking of the Si-C bonds [5]. Etching of SiC using inductively coupled SF_6/O_2 plasma is described as follows:

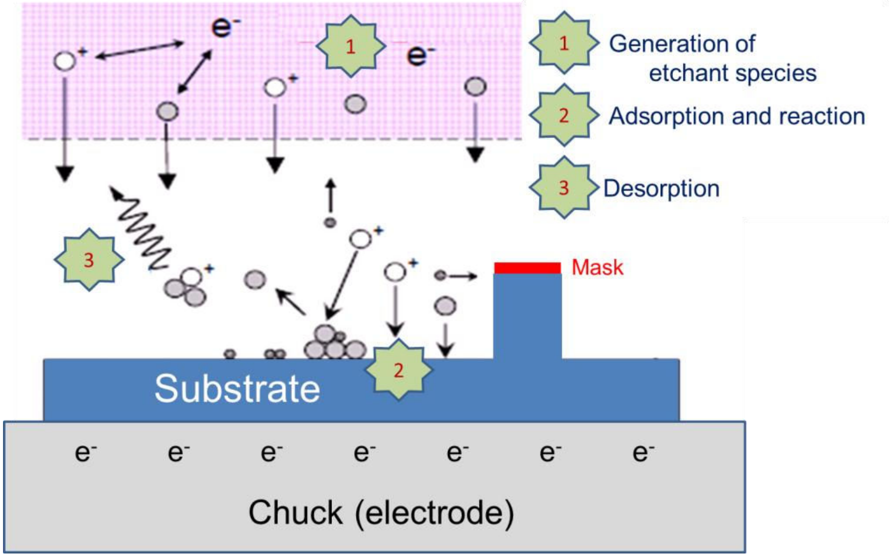

Figure 3.1 Schematic diagram of ICP etching mechanism.

First, reactive species formed by dissociation of gases in plasma (step: generation of etchant species).

$$SF_6\ (g) + e^- \rightarrow SF_5^+\ (g) + F\ (g) + 2e^- \qquad \text{Eq 3.1}$$

Fluorine radicals and sulfur fluoride ions (SF_x^+) generated in plasma are responsible for the breaking of the Si-C bond, then combine with Si and C to form volatile SiF_x and CF_x (step: adsorption and reaction).

$$\begin{gathered} SiC\ (s) + 8F\ (g) \rightarrow SiF_4\ (g) + CF_4\ (g) \text{ or} \\ SiC\ (s) + SF_x^+\ (g) \rightarrow SiF_x + CF_y + SF_z^+ \end{gathered} \qquad \text{Eq 3.2}$$

Then, the volatile species (SiF_x and CF_x) are pumped away (step: desorption).

In addition, the positive ions formed in the plasma will bombard the surface and help clear the surface of samples, due to an inherent electrical potential difference between the plasma and the substrate, thereby enhance the etch rate. The detail etching mechanism is illustrated in Figure 3.1.

3.2.2 Study of the effect of etching parameters

Etch behaviors strongly depend on the many process parameters, such as pressure, gas flows, coil power, etc. as illustrated in Figure 3.2. The effects of process parameters for micro-scale SiC etching have been intensively studied, but there are only few reports at the nanoscale. It is strongly recommended to understand the process parameters to be able to obtain high-anisotropy profile of nanostructures. Generally, optimum etching conditions is evaluated based on the combination of the etching rates, anisotropy, selectivity and etched surface morphology. In this section, the key etching process parameters will be studied, which influence on etching characteristics.

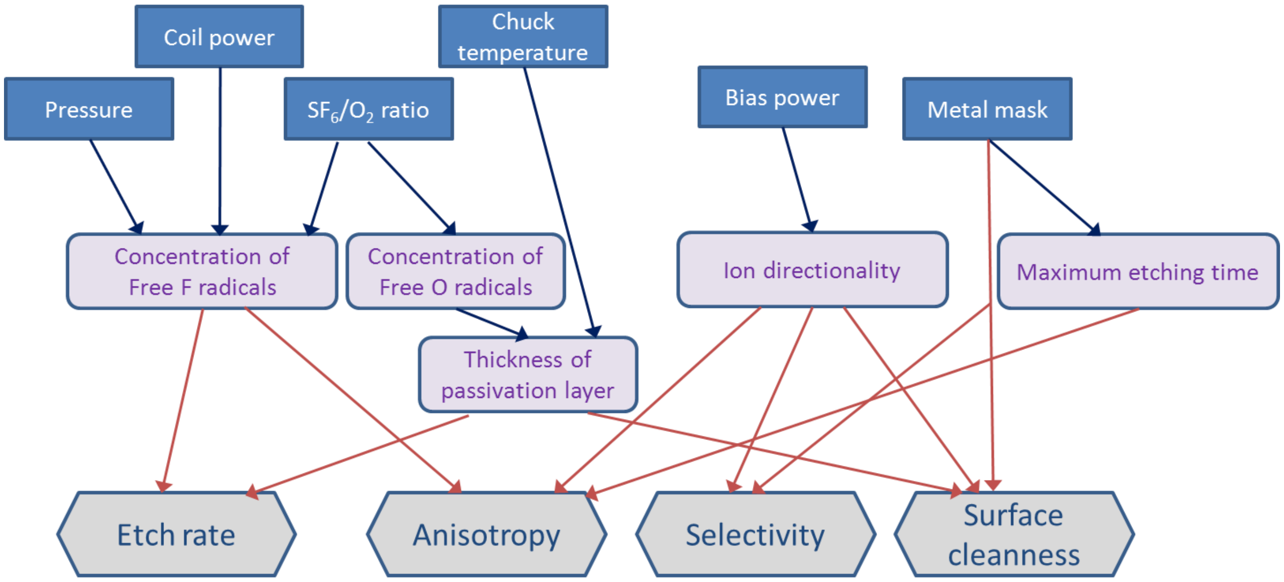

Figure 3.2 Effects of the key process parameters on the etch characteristics. Modified from [6].

▣ Etching gases

Many different fluorinated-based gases, such as SF_6 [7-10], NF_3 [4], and CHF_3 [11], with the addition of Ar or O_2 have been considered to achieve high rate ICP etching of SiC. Among these, SF_6 (sulfur hexafluoride) has been widely employed for SiC etching owing to high degree of F dissociation and nonhazardous nature. SF_6 has low F-atom binding energy (78.3 kcal/mol), which is second lowest among commonly available dry-etch gases (NF_3 at 66.4 kcal/mol) [12]. This low F atom binding energy would result in a high degree of F dissociation and relatively high etch rate.

❖ Effect of the gas flow rate

SiC etch rate increases with increasing the gas flow rates and starts to saturate at certain level. It might be attributed to the insufficient coil power to promote the dissociation of increased SF_6 gas or the insufficient number of broken Si-C bonds on the sample surface to enable formation of SiF_x and CF_x volatiles [13]. Even if there are enough coil power and number of broken Si-C bonds, the etch rate could be decreased due to recombination the fluorine radicals before reaching the sample surface.

▣ Main/Bias power and pressure

❖ Main power

Etch rate increases almost linearly with increasing the inductive coil power, because the increment of coil power promotes the dissociation of SF_6 in the chamber. It also enhances the ion directionality and induces the features with high-anisotropy.

❖ Bias power

The increment of RF power of the supply connected to the substrate electrode leads to high induced DC bias values and enhances thus the physic etching on the sample by the ion energy bombarding. It results in the increase of etch rate and aspect ratio, but it also leads to the increase of the surface roughness [4].

❖ Pressure

Etch rate has a maximum value at a certain level of operating pressure. If the operating pressure is too low, it results in low etch rate due to low density of fluorine. The etch rate also decreased with increasing operating pressure, because the number of colliding atoms increases. Consequently, the mean free path of the ions decreases [9].

3.2.3 Etching phenomena

▣ Micromasking

The micromasking (grass-like structure on the substrate in Figure 3.3(a)) are generated in two separate ways: (1) redeposition of nonvolatile species including etch products and material sputtered from the mask/reactor or (2) slow etching of defects in the SiC itself. Either of these sources of micromasking can cause via failure and should be eliminated or minimized [14].

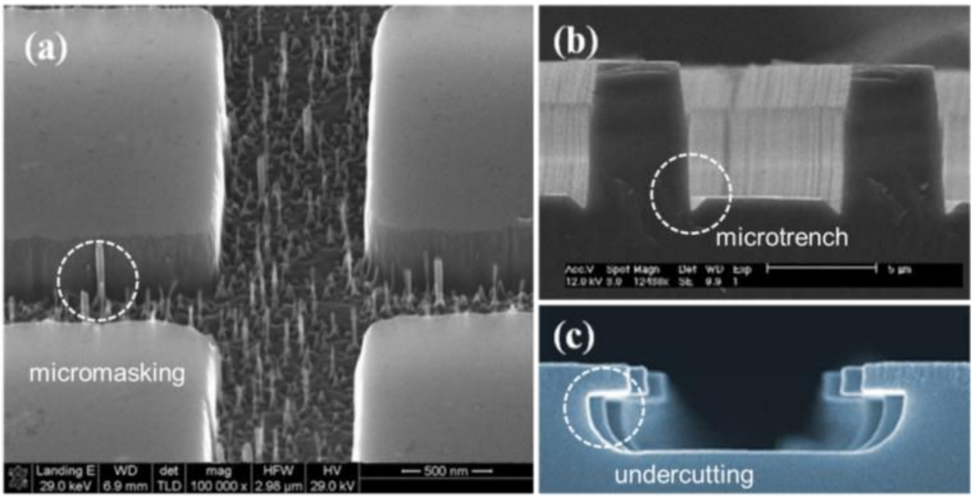

Figure 3.3 SEM images of (a) micromasking [15], (b) microtrench [7] and (c) undercutting [16].

▣ Microtrenching effect

ICP etching provides high etch rate and high anisotropy for the etching of SiC due to high density of ion flux and ion bombardment. However, it also results in undesirable phenomena, such as small trench (microtrenching) around the base of the profile (Figure 3.3(b)). Therefore, many group have investigated the effect of magnetic field [17], electron beam charge neutralization [18], substrate temperature [9] and plasma process parameter [11] to suppress the microtrenching effect.

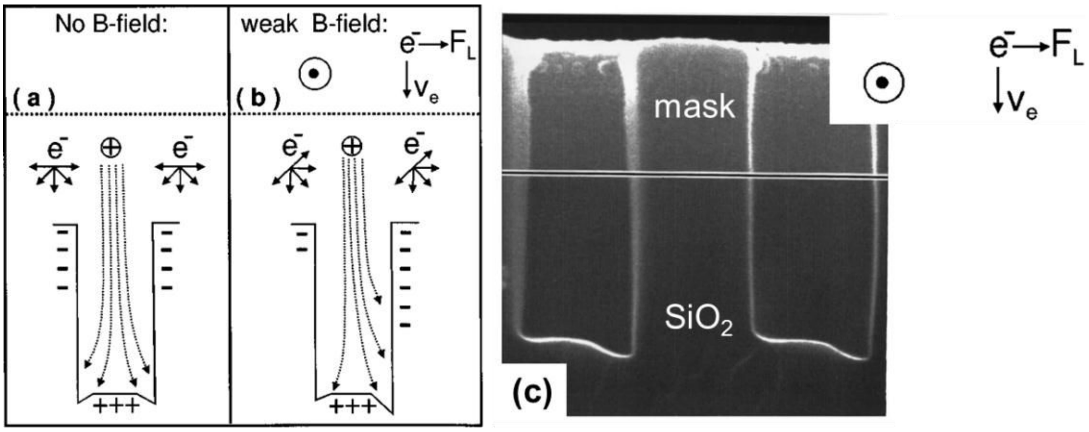

Figure 3.4 Schematic illustrations of microtrench formation (a) with and (b) without magnetic field, (c) the cross section of asymmetric microtrenching [19].

Microtrench formation mechanism has usually been explained by non-uniform charge distribution within etching features. The ion angular distribution is highly anisotropic, whereas the electron angular distribution is nearly isotropic. Therefore, plasma electrons are more likely to impinge on the top of feature. As a result, the top of the feature charges negatively and the bottom of the feature charge positively. This differential charging produces local electric fields inside the feature [19], ions tend to be deflected by negatively charged sidewalls and enhanced ion bombardment at the foot of the sidewall by increased ion flux [17, 18].

Schaepkens et al. [19] have demonstrated that a weak magnetic field produces a significant asymmetry in microtrenching in Figure 3.4(a-b). Their results demonstrate that electron-based sidewall charging is to a significant responsible for microtrenching (see Figure 3.4(c)), therefore differential charging along the structure is an important effect in micro or nanostructure fabrication using high-density plasmas.

▣ Undercut profile

Undercut profile from etching in Figure 3.3(c) is generally induced by over etching when the etchant is applied too long. Isotropic etching condition, which etches in all directions equally, also leads to the undercut morphology.

3.3 Experimental results for the fabrication of SiC nanopillars

The ICP etching experiments have been carried out on 8 inch diameter wafers in an industrial cluster tool, which consists of a load-lock chamber located in a class 10 clean room, a high density decoupled plasma source (CENTURA 5200B from Applied Materials Inc.), all these components connected together via a robotized transfer chamber [20], as shown in Figure 3.5

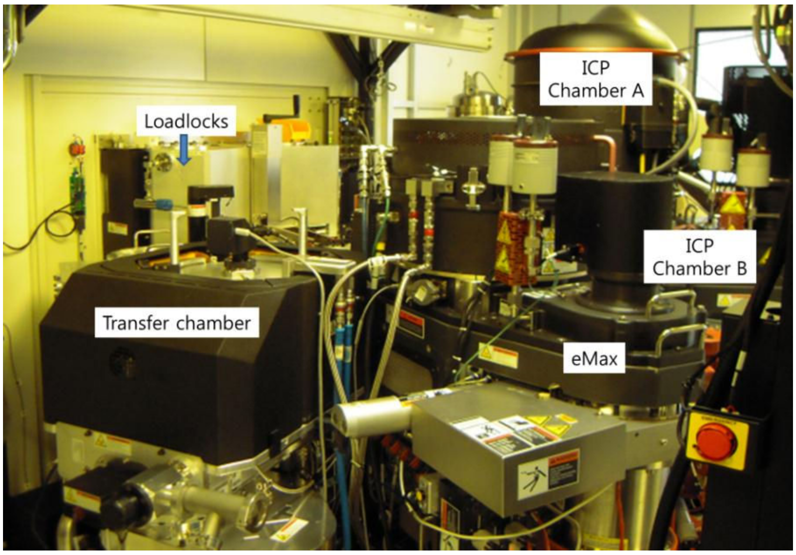

Figure 3.5 Photo image of ICP etching equipment (CENTURA 5200B).

▣ Etching procedure

For the etch masks, different sizes of circular patterns (115 and 370 nm diameters) were prepared with a same pitch distance (5 - 7 µm) using electron beam lithography (JEOL JSM-7401F). After developing the exposed resist, various metal (Ni, Al and Cu) masks with 110 nm thickness was deposited on different kinds of SiC substrates by e-beam evaporation. Then, the lift-off process is performed at 40 °C using the remover solution (AR 300-70).Afterwards, the SiC samples with mask pattern were attached on a supporting 8 inch Si wafers. The supporting Si wafer is covered by SiO_2 (10 µm) to protect the Si wafer. When the sample is ready, it is placed in the loadlock, and then evacuated. After mapping the wafer, it is transferred to the process chamber. Then, the wafer is clamped and moved to the process chamber (ICP chamber A in Figure 3.6). If the wafer is properly placed and clamped, the process is started. After finishing the etching process, the wafer is declamped and finally transferred to the loadlock.

Table 3.1 Overall etching conditions used in this study.

Etching parameter	Values
ICP power	1500 W
Total gas flow (SF_6+O_2)	50 sccm
Bias voltage	100 – 300 V
O_2 concentration	10 – 40 %
Chamber pressure	4 – 7 mTorr
Temperature of substrate	300 K

ICP source power which runs at the industrial frequency of 13.56 MHz was constant (1500 W) during the process. The substrate chuck, also powered at 13.56 MHz was varied between 100 and 300 V, independent of the ICP source power. The amount of gas mixture (SF_6 and O_2) was constant (50 sccm), but the gas pressure and oxygen content were also varied, the former between 4 and 7 mTorr, and the latter from 10% to 40%, respectively. The overall etching conditions used in this study are shown in Table 3.1. The temperature of the substrate was held constant at 300 K by means of a nitrogen cooled chuck.

▣ SiC substrates used in this study

The 4H-SiC (0001) substrates, which were fabricated by the conventional Physical Vapor Transport (PVT) method at LMGP laboratory [21], were used to study about the effect of etching parameters in the section from 3.3.1 to 3.3.5. Different kinds of SiC substrate were used to the study about the etching behavior according to SiC dependence in section 3.3.6, as listed in Table 3.2. The 4H and 6H-SiC (0001) on-axis substrates were purchased from Tankeblue Inc. [22]. The 6H-SiC (11-20) substrates were fabricated from different groups based on small rectangular seeds by using the conventional PVT [23].

For 3C-SiC (001) substrate, the 3C-SiC layers were grown in a hot-wall chemical vapor deposition reactor on 100 mm diameter p-type boron-doped (100) Si wafer without rotation of the wafer [24]. For SiC epitaxial growth, silane (SiH_4) and propane (C_3H_8) were used as the precursor gases. Hydrogen (H_2) mixed with 2 % of Ar was used as carrier gas. For 3C-SiC (111) substrate, the 3C-SiC layers were homo-epitaxially grown on quarters of 6H-SiC substrate with area larger than 1 cm^2 by sublimation method [25].

Table 3.2 SiC substrates used in this study.

Polytype	Orientation	Source	Single crystal / Hetero-epi	Doping level	Related sections
4H-SiC	(0001)	LMGP (France)	Single crystal	10^{17}	3.3.1 – 3.3.5
4H-SiC	(0001)	Tankeblue Inc.	Single crystal	10^{20}	3.3.6
6H-SiC	(0001)		Single crystal	10^{20}	
6H-SiC	(11-20)	Dong-Eui Uni. (Korea)	Single crystal	N/A	
3C-SiC	(001)	Linköping Uni. (Sweden)	3C-SiC epi (7μm) on Si	$2 - 8\cdot10^{16}$	
3C-SiC	(111)		3C-SiC epi (18μm) on 6H-SiC	$5\cdot10^{16}$	

3.3.1 Effect of metal mask species

A masking material with high selectivity with respect to SiC in the SF_6/O_2 etching process is needed to obtain the maximum height of SiC nanopillars. To find a suitable mask material for etching, ICP etching is carried out at an ICP coil power of 1500W and etching gas (SF_6: 40 and O_2: 10 sccm) with different metal mask species (Cu, Ni and Al) for an etching time of 3 min. SiC nanopillars with Cu mask show a roughness on the sidewalls (Figure 3.6(a)). This might be attributed to the irregularly formed products on the mask. These products are formed during the etching process by reacting with F or O radicals. These nonvolatile reaction products (Cu_2F or Cu_2O) formed on the mask exhibit high etch selectivity and sputter resistant properties, therefore Cu was evaluated as the best candidate for pattern mask materials of SiC MEMS devices [17]. However, a Cu metal mask is not suitable for etching at the nanoscale. In fact, the irregularly formed products on the mask act like a mask pattern, and they finally induce roughness on the sidewalls of the etched pillars

(Figure 3.6(a)). In addition, the nonvolatile reaction products (Cu_2F or Cu_2O) formed near the interface between Cu mask and SiC lead to low adhesion force of Cu mask on the SiC surface. Therefore, sometimes Cu mask is detached from the SiC surface during the etching process as indicated by the arrows in Figure 3.6(d).

SiC pillars with an Al mask present a higher roughness on the sidewalls than that with a Cu mask along the vertical direction (Figure 3.6(c)). It might be due to the damage of the mask by the energetic ion bombardment.

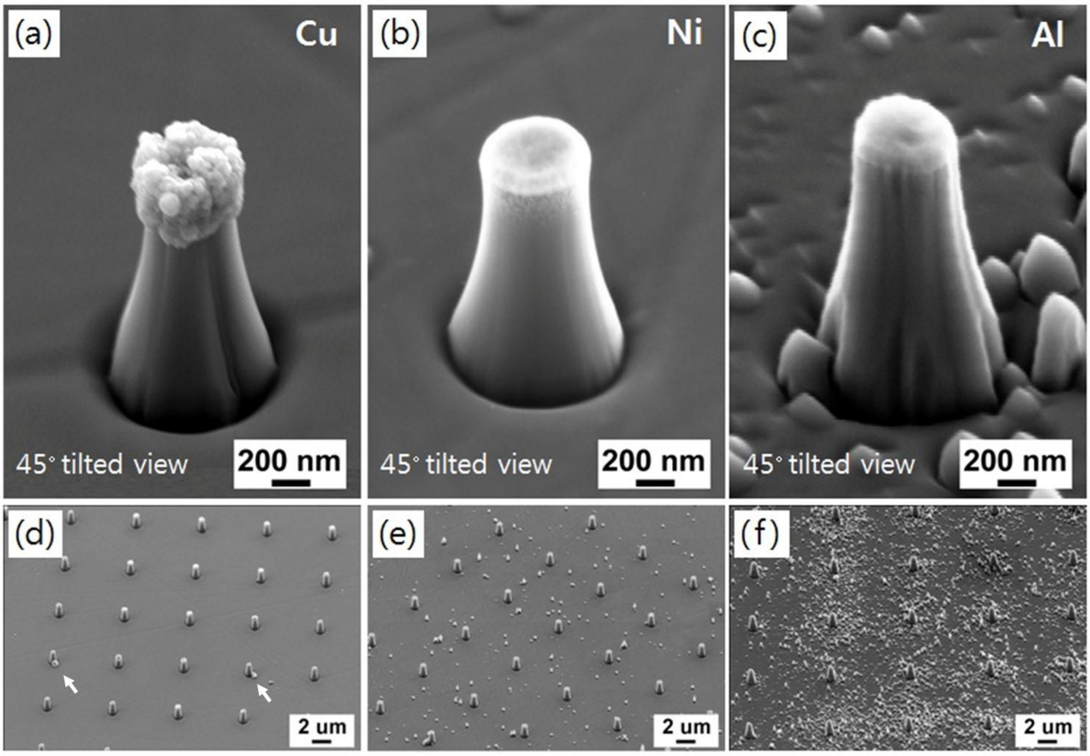

Figure 3.6 SEM images of nanopillars with (a) and (d) Cu, (b) and (e) Ni, and *(c) and (f) Al metal mask (45° tilted view)*, (initial mask size = 370 nm).

The Ni mask is sufficiently sputter-resistant to protect the SiC beneath the mask without an irregularly formed nonvolatile metal-fluoride layer. Consequently, the etching profile of SiC nanopillars with a Ni mask shows a clear surface on the sidewall of the nanopillar with a uniform mask shape (Figure 3.6(b)). Figure 3.6(f) shows a high density of residue (grass-like structure) on the substrate; it is believed to be due to the micromasking effect caused by the redeposition of sputtered material from the Al mask [26]. The mask material with a relatively low selectivity (such as Al) is more likely to be sputtered from the mask onto the SiC surface by the energetic ion bombardment than the other mask with a relatively high selectivity, such as Cu and Ni [27]. Consequently, the sputtered mask material on the surface leads to a micromasking effect that eventually results in rough and textured surfaces with grass-like features. The micromasking effect decreases in the following order: Al, Ni and Cu (see Figure 3.6(d)–(f)), which shows the reverse tendency of sputter-resistance (Cu > Ni > Al). As a result, the higher sputter-resistance of the mask results in a clearer SiC substrate surface than the lower sputter resistance of the mask. Even though the Cu mask shows the clearest surface, Cu is not a suitable mask material due to the induced roughness on the pillar. Based on these results, Ni is chosen as the mask material for the etching of nanopillars owing to the clear surface of sidewalls and the relatively low density of micromasking.

3.3.2 Effect of SF_6/O_2 flow rate ratio

The etching behavior depends strongly on the composition of etch gases. Specially, in the case of SF_6 plasma, oxygen concentration is known to influence the profile of SiC nanopillars, such as anisotropy, surface cleanness, metal mask selectivity and etch rate by controlling the neutral fluorine density [5]. To examine the oxygen effect, ICP etching is carried out with different oxygen concentrations from 10 to 40 vol%, while all other experimental conditions are kept constant.

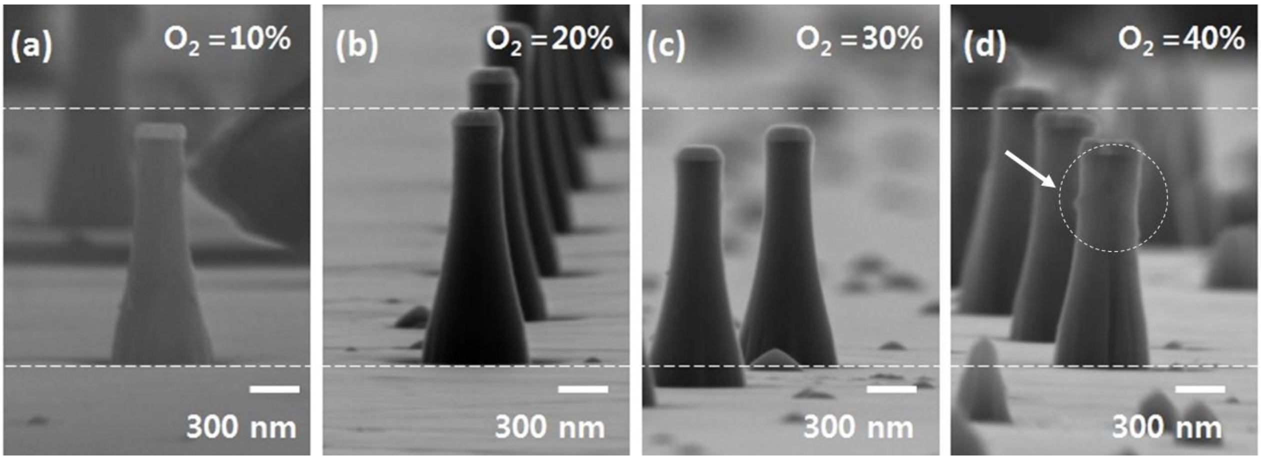

Figure 3.7 Side-view SEM images of nanopillars at different O_2 concentrations of (a) 10%, (b) 20%, (c) 30% and (d) 40%, respectively (initial mask size = 370 nm and etching time = 180 sec).

Figure 3.7 shows the SEM images of nanopillar arrays fabricated with different O_2 concentrations. The pillar height initially increases with O_2 concentration, and reaches a maximum value of 1.58 ± 0.02 μm at around 20% of O_2 concentration. Then, it decreases with increasing O_2 concentration, as shown in Figure 3.8.

The optimum O_2 was determined by measuring the position where the aspect ratio is the maximum. The aspect ratio is simply calculated by dividing the height by base width. The aspect ratio shows a maximum value of 2.4 ± 0.02 at 20% of O_2 concentration. The optimum O_2 concentration (20%) and the observed trend are comparable to the results reported elsewhere [28]. The addition of O_2 can keep fluorine (F) radical concentration high, which is responsible for the etching of SiC, by reacting with unsaturated CF_n and SF_n bonds so that F radicals do not combine with them. In addition, F radicals from the plasma preferentially etch Si rather than C [7]. As a result, a carbon-rich layer is formed on the SiC substrate, which is one of the limiting factors for SiC etching. The presence of appropriate O_2 level provides the driving force for removing the carbon by forming volatile etching products, such as CO, CO_2 and CF_2 [9]. Consequently, those two factors are believed to contribute to the increase in the etch rate. However, further addition of oxygen decreases the etch rate due to the dilution of F concentration. It is found that the O_2 concentration also affects the morphology (or vertical profile) of the etched nanopillars. We believe that higher density of F radicals induces higher aspect ratio. In addition, the base width slightly increases with increasing O_2 concentration due to the deposition of a passivation layer during the etching process, such as SiF_xO_y, as shown in Figure 3.8.

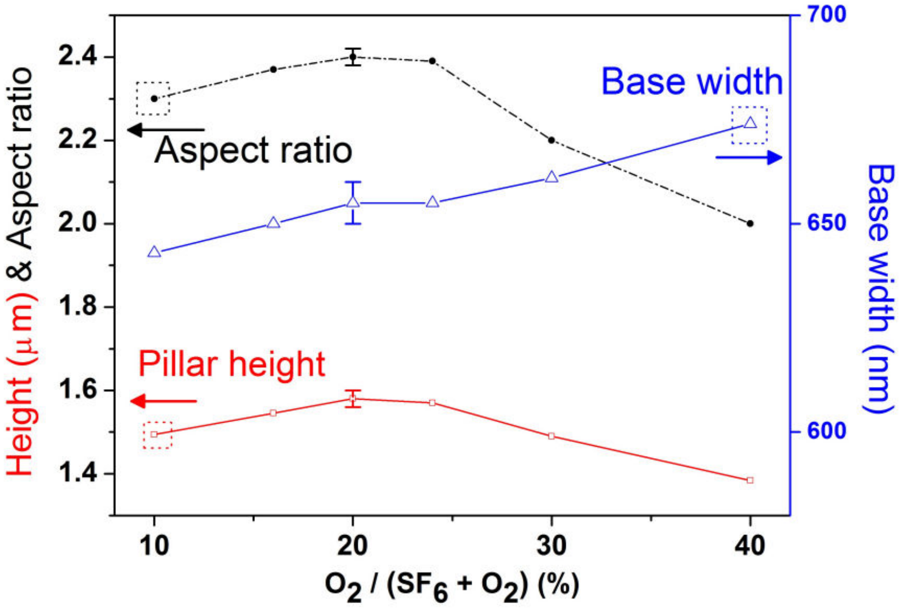

Figure 3.8 Height and base width of the pillars, and corresponding aspect ratio with different O_2 concentrations (initial mask size = 370 nm and etching time = 180 sec).

Broader base diameter of the nanopillars than the size of the mask could be explained by several factors, such as the shadowing effect of the mask [7, 29], deposition of passivation layer or mask erosion. In the ideal case, incident ions arrive at the substrate vertically during the etching process, but in the practical case, incident ions show a gauss angle dispersion due to scattering with other particles [29]. Therefore, incident ions are reduced in the vicinity of the base due to the shadowing effect of the pattern and pillar. Simultaneously, the deposition of passivation layer (SiF_xO_y) on the SiC nanopillars during the etching process also contributes to tapered nanopillars since the deposition rate decreases from the bottom to the top of the pillars.

Generally, these two effects are enough to describe the slope of structures with micro scale patterns. However, in the case of etching for nanoscale patterns and long etching time, mask erosion also needs to be considered. Moreover, if the pillar height is long enough to induce a non-uniform charge distribution within etching features, the deflected ion can also significantly influence the tapered profile of pillars. This will be discussed in more detail in sections 3.3.4 and 3.3.5, respectively.

Figure 3.7(d) pointed by an arrow shows a deposited layer on the sidewalls of the SiC nanopillars. It is believed to be due to the redeposition of nonvolatile species including etch products [26]. The inclusion of excess O_2 (above 20% of O_2 concentration) tends to react with the Si and form SiO_x or SiF_xO_y on the surface, which has lower etch rates than SiC (the SiO_2 etch rate is about 90% of the SiC etch rate for SF_6/O_2 [30]). Meanwhile, insufficient O_2 (below 20% of O_2 concentration) induces a carbon-rich layer and nonvolatile carbon-related products (CF_x) on the substrate. At optimum O_2 concentration (20%), clean wall surfaces are observed due to the balance between the etching by F radicals and the deposition by O radicals.

3.3.3 Effects of bias voltage and chamber pressure

The effects of bias voltage and work pressure were investigated using a small mask circular pattern (115 nm diameter) to fabricate SiC nanopillars. This size is the smallest circular pattern size with metal (Ni) deposition of 110 nm. The circular pattern below 100 nm disappears during the lift-off process due to low adhesion between Ni and SiC substrate.

Figure 3.9 shows the SEM images of etched SiC nanopillars as a function of bias voltages for 180 sec etching time. Higher bias voltage increases the directionality of ion and ion bombardment energy, so it provides more efficient bond breaking of SiC. As a result, the height and aspect ratio of the SiC nanopillars are gradually increased with the increase in bias voltage, as shown in Figure 3.10. The pillar height and aspect ratio reach the values of 2.2 µm and 7.4 at a bias voltage of 300V, respectively. Moreover, the size of microtrench increases with increasing bias voltage due to enhanced directionality of the energetic ions. On the other hand, the mask thickness and diameter considerably decrease with increasing bias voltage, which is induced by the enhanced physical sputtering. As a result, the initial mask size (115 nm) is considerably reduced to 60 nm at 300V bias voltage, as shown in Figure 3.9(d).

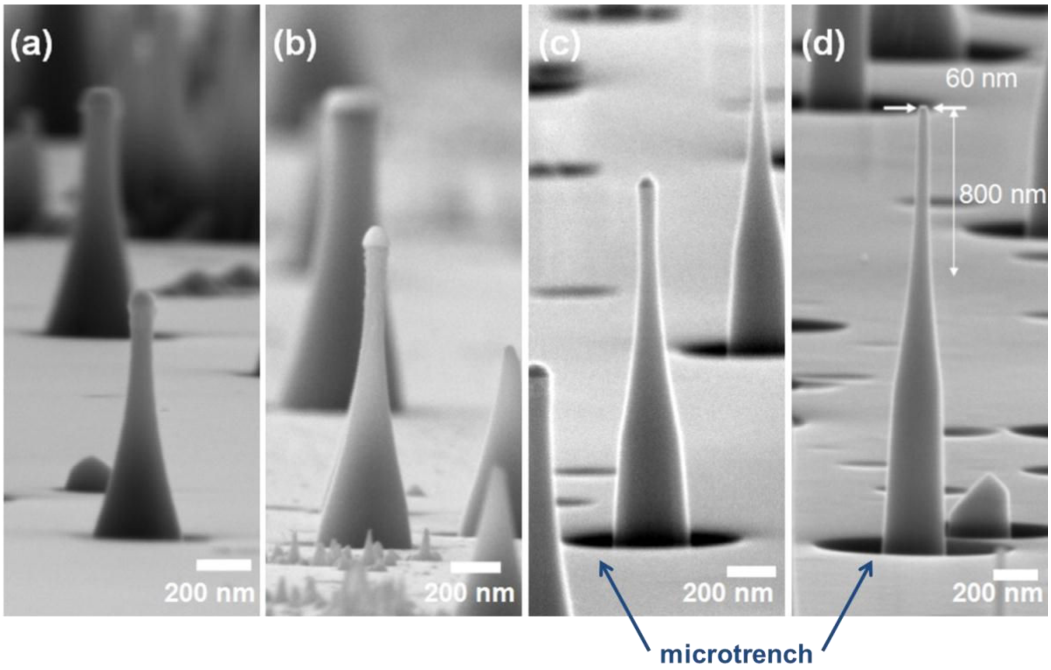

Figure 3.9 Side-view SEM images of SiC nanopillars at different bias voltages of (a) 100 V, (b) 150V, (c) 200V and (d) 300V, respectively (initial mask size = 115 nm , pressure = 6 mTorr and etching time = 180 sec).

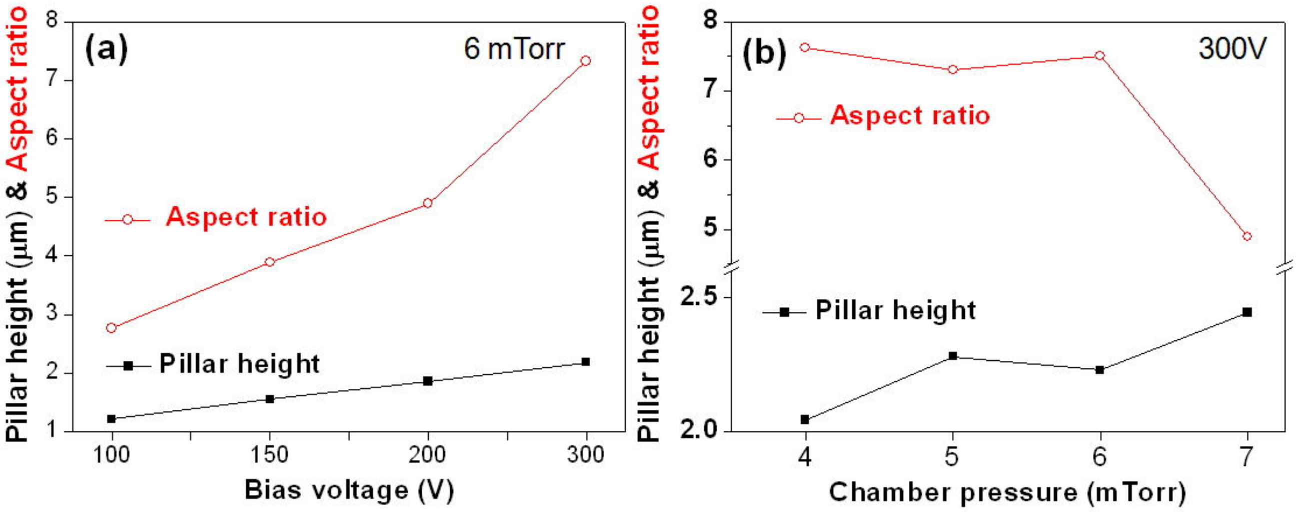

Figure 3.10 Height and aspect ratio of the pillars as a function of (a) bias voltage and (b) chamber pressure (initial mask size = 115 nm and etching time = 180 sec).

Figure 3.11 shows the SEM images of the etched SiC nanopillars with small mask circular pattern (115 nm) as a function of chamber pressure at 300 V bias voltage and 180 sec etching time. There is no big difference between 5 mTorr and 6 mTorr in terms of pillar height and aspect ratio, as depicted in Figure 3.10(b). The pillar height at 4 mTorr is slightly decreased due to the decrease in the ion density, but there is no obvious change in the aspect ratio.

At a pressure of 7 mTorr, the pillar height slightly increases due to the increase in the ion density, while the aspect ratio considerably decreases from 7.4 at 6 mTorr to 4.9 at 7 mTorr (Figure 3.10(b)). Increasing the pressure also increases the number of colliding atoms, so the mean free path of the ions decreases [9]. It reduces the directionality of the ions, and finally results in a tapered profile with a low aspect ratio.

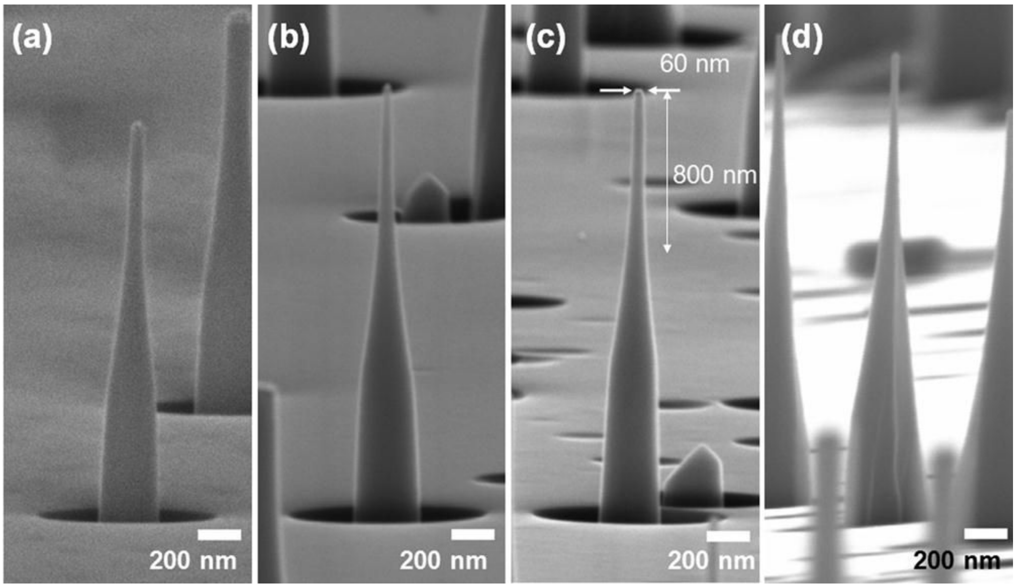

Figure 3.11 Side-view SEM images of nanopillars at different chamber pressures of (a) 4 mTorr, (b) 5 mTorr, (c) 6 mTorr and (d) 7 mTorr (initial mask size = 115 nm, bias voltage = 300V and etching time = 180 sec).

In conclusion, the effects of bias voltage and chamber pressure on the formation of SiC nanopillars were investigated using a 115 nm diameter circular mask pattern. The obtained SiC pillars at an optimum bias voltage (300 V) and chamber pressure (6 mTorr) show a height of 2.2 µm and aspect ratio of 7.4. The etched SiC nanopillars under these conditions have a minimum diameter (60 nm). The length of the pillars (below 100 nm in diameter) is around 800 nm, which is long enough to reveal the electrical property of SiC nano-FETs. Mask erosion and tapered profile are inevitable for the etching of hard-to-etch materials such as SiC using the ICP etching process.

3.3.4. Etching profile evolution over etching time

Due to mask erosion during the ICP process, the pillar height is strongly limited by the lateral mask size as well as the vertical mask thickness. Therefore, we have to take into account the mask erosion for the design of mask pattern size to get long SiC nanopillars. In this section, we have investigated the etching behavior using a sufficiently large circular pattern (370 nm diameter) as a function of etching time, not only to get longer SiC nanopillars, but also to monitor the etch characteristic parameters, such as mask size, mask thickness, pillar height and sidewall bowing.

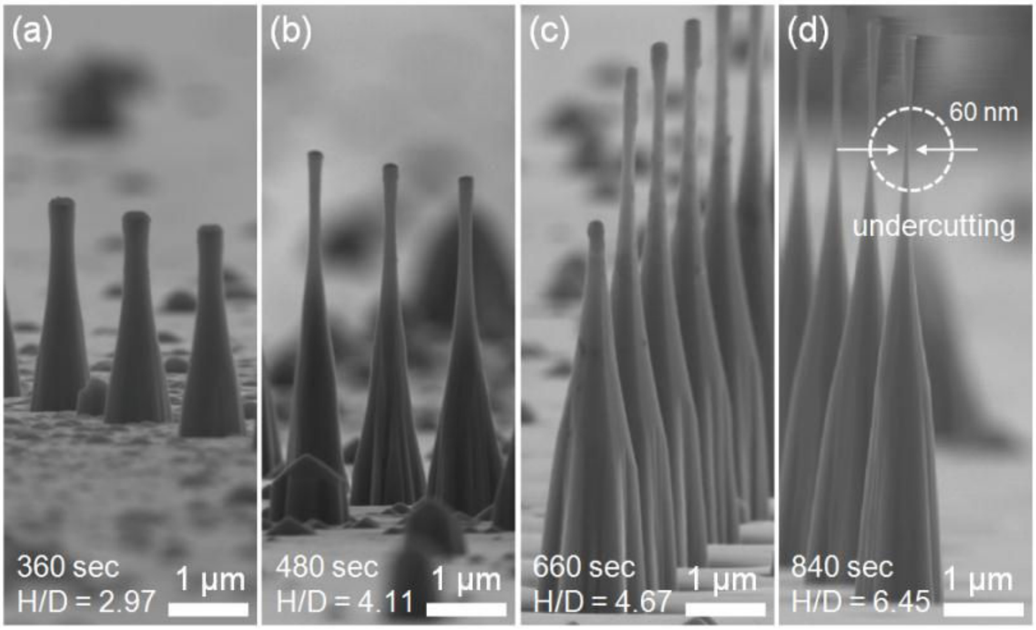

Figure 3.12 SEM images of SiC nanopillars with different etching time
(a) 360 sec, (b) 480 sec, (c) 660 sec, and (d) 840 sec, respectively (initial mask size = 370 nm).

Figure 3.12 shows the morphology of the etched SiC nanopillars according to etching time at the optimum O_2 concentration (20%) and 150 V bias voltage. The height of the SiC nanopillars is found to increase depending on the etching time. For a quantitative analysis, the mask size, mask thickness and pillar height are plotted as a function of etching time, as shown in Figure 3.13.

The aspect ratio (H/D) of the pillars increases with etching time (see Figure 3.12). The maximum obtained is 6.45 at 840 sec. Long etching time leads to large etching depth with high anisotropy, but it also gives an undercut etching profile at 840 sec (see Figure 3.12(d)), due to high chemical etching by direct exposure of F radicals from the plasma. The minimum diameter of the SiC nanopillars at 840 sec is around 60 nm at the undercutting. Therefore, it is obviously necessary to balance the physical (related to ion bombardment) and chemical (related to F radicals) contributions in order to get straight features of pillars.

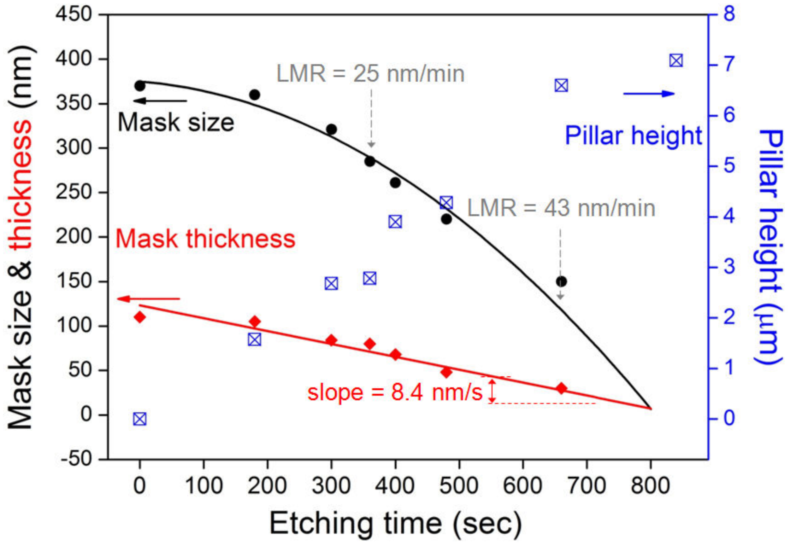

Figure 3.13 Mask size and thickness, and corresponding pillar height as a function of etching time.
(LMR is Lateral Mask erosion Rate from the fitted curve)

The etch rate is calculated by the pillar height over etching time. It remains almost constant (550 nm/min) during etching, and then slightly begins to decrease (165 nm/min) in the region between 660 and 840 sec when the metal mask is completely removed. The etch selectivity of mask materials (Ni) with respect to SiC is around 65. The mask thickness at the center is linearly reduced with time in Figure 3.13, so the vertical etch rate of the mask remained constant throughout the etching process (8.4 nm/min). In addition, the lateral etch rate of the mask increases evidently with increasing etching time. The vertical and lateral etch rates of the mask fitted a linear and a second-order polynomial for the experimental data, respectively. Mask erosion behavior seems to be quite well described by fitting the curve with R^2 values for mask size and thickness of 0.93 and 0.97, respectively.

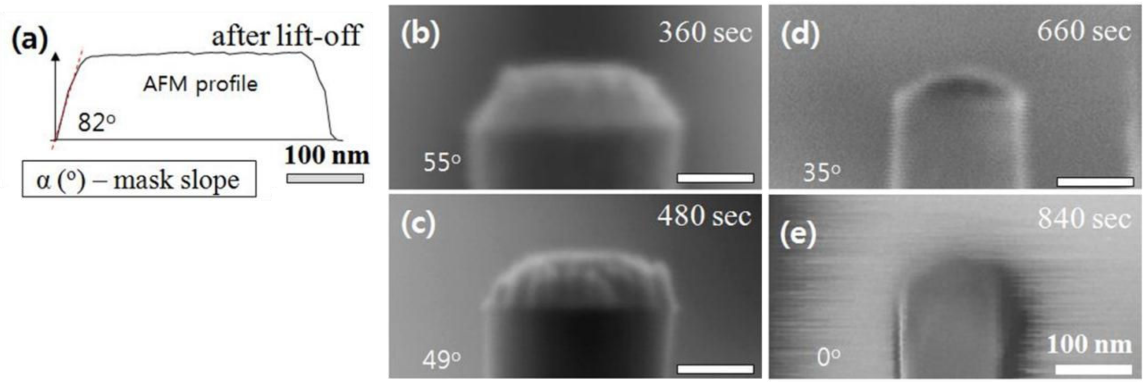

Figure 3.14 (a) AFM profile after lift-off, and (b-e) magnified SEM images of Ni mask after etching for (b) 360 sec, (c) 480 sec, (d) 660 sec and (e) 840 sec. Same scale from (a) to (e).

To analyze the mask profiles in more detail, the Ni mask part of each SiC nanopillar is magnified, as shown in Figure 3.14. Mask erosion is a little bit faster at the edges due to strong physical sputtering of energetic ions, which is enhanced by the local distortion of the electric field [27]. Therefore, mask faceting is observed due to the ion bombardment effect. Consequently, the mask slope angle is progressively decreased from 55^o at 36 s to 35^o at 660 sec, as shown in Figure 3.14.

As the etching proceeds, the edge of the mask pattern is etched away. SiC below the etched Ni mask is no longer protected and begins to be etched. Finally, when the metal mask is completely removed, SiC nanopillars begin to develop a slight convex shape at the top of the pillar, as shown in Figure 3.14e. As noted above, mask erosion can be one of the reasons for vertically tapered sidewalls of SiC nanopillars since reduced mask leads to more exposure of the energetic ion flux on the top part of the pillars than the bottom part. As the mask pattern size shrinks into the nanoscale, mask erosion and undercutting play a crucial role in determining the maximum height and etching profile of SiC nanopillars.

3.3.5. Hexagonal shape of SiC nanopillars

In this first part of the study, it was noted that the etched SiC nanopillars show a transition from circular to hexagonal shapes with increasing etching time, as shown in Figure 3.15. This phenomenon is explained by the in-plane anisotropy of growth rate. The hexagonal symmetry of SiC nanopillars revealed by the etching method is first presented in this study. It must be noted that the edges of the hexagon are parallel to the <11-20> direction of 4H-SiC in Figure 3.15(c-d), which corresponds to the densest crystallographic direction of the SiC phase. The anisotropy of the surface free energy of SiC along different crystallographic directions leads to the anisotropic chemical and physical properties of SiC, which determine the etching properties [31]. Therefore, the edge of the facet <11-20> is more robust than other directions due to close packed structure and low surface energy.

According to the Wulff theorem [32], hexagonal structure is formed as a result of SiC etching since it is energetically favored due to the minimum surface free energy of the facets [31]. Therefore, long time etching process leads to the appearance of the densest planes of the SiC phase, which have the lowest surface free energy. It is also noticeable that the hexagonal pyramid pillar shows two different contrast modes in Figure 3.15(d), unlike the circular pillar in Figure 3.15(a). It reflects the topology of SiC nanopillars, which corresponds to l–*l'*, *m−m'* and n–*n'* in Figure 3.15(e). The formation of this feature is typically attributed to the local electric field by non-uniform charge distribution within etching features.

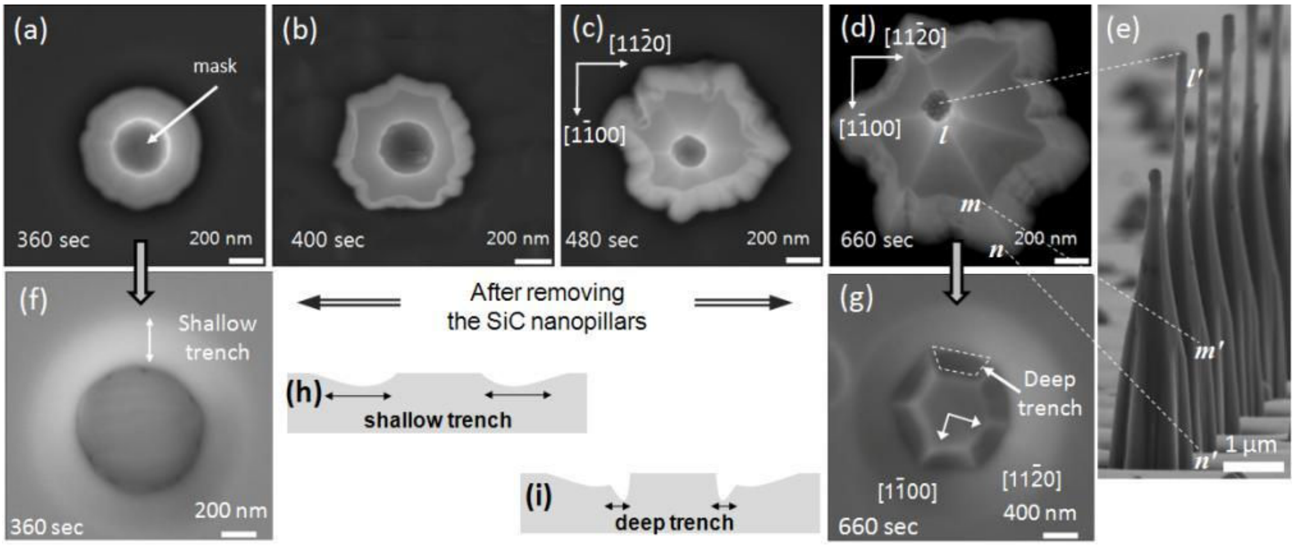

Figure 3.15 Top-view SEM images of 4H-SiC nanopillar after etching for (a) 360 sec, (b) 400 sec, (c) 480 sec, and (d) 660 sec, respectively. (e) side-view SEM image of SiC nanopillars after etching 660 sec. SEM images after removing the SiC nanopillar after (f) 360 sec, and (g) 660 sec etching, and the corresponding illustrations of cross section for (h) shallow trench and (i) deep trench.

The top of the feature is charged negatively and the bottom of the feature is relatively charged positively, since plasma electrons are more likely to impinge on the top of the feature due to isotropic electron angular distribution [19, 33]. Due to local distortion of the electric field, ions tend to be deflected by negatively charged sidewalls and enhanced ion bombardment at the foot of the sidewall by increased ion flux.

As a result, the slope is no longer inclined and is close to the vertical direction in the range of m' and n'. On the other hand, circular pillars show only one contrast mode (Figure 3.15(a)) and a single tapered profile (Figure 3.12(a)), because small height of the pillar at the initial stage of etching is not enough to induce the charge non-uniformity. However, the deflected incident ions can induce shallow trenches around the bottom of the pillar structure. This phenomenon is well known as the microtrenching effect [34]. Figure 3.15(f) clearly shows the shallow trench after removing the SiC nanopillars, and its corresponding cross-section is depicted in Figure 3.15(h). In the case of hexagonal pillars, ions arriving on the feature sidewalls are more easily reflected due to the grazing angle and accordingly ions are accumulated at the bottom of the pillar. Consequently, it leads to the enhancement of the etch rate and formation of deep trenches around the hexagonal six facets. Deep trenches at the six facets could be observed after removing the SiC pillar in Figure 3.15(g), and the corresponding illustration of cross-section is also shown in Figure 3.15. We can therefore conclude that shallow trenches around the bottom of the nanopillar and deep trenches near the six facets are attributed to deflected and reflected ions, respectively.

3.3.6 Dependence of polytypes and crystal orientations

In the previous section, the etching profile evolution of SiC pillars has been changed from a circular to a hexagonal pillar shape on 4H-SiC (0001) substrate with increasing of the etching time, which originated from the crystallographic structure of the α-SiC.

An interesting property of SiC is that different polytypes (such as, 4H-, 6H- and 3C-SiC) of SiC have different physical properties originating from the different stacking sequences of the Si-C layers. If a top-down approach is applied into these different polytypes of SiC layer, SiC nanostructures with different physical properties may be easily achieved, which can lead to further exploit the applications of SiC nanostructures. However, there is still a lack of understanding of the etch behavior, such a dependence of polytypes and crystal orientations.

In this section, the etching behavior of SiC nanopillars depending on the different polytypes and crystallographic orientations: 4H-SiC (0001), 6H-SiC (0001) c-plane, 6H-SiC (11-20) α-plane, 3C-SiC (111) and 3C-SiC (001), is presented.

▣ Etching characteristics depending on SiC polytypes

Figure 3.16 shows top-view SEM images of the etched SiC nanopillars with different polytypes and crystallographic orientations after etching during 360 sec, 700 sec and 840 sec, respectively. As shown in previous section 3.3.5, continuous etching in SF_6/O_2 plasma on α-SiC (0001) substrates causes that the pillar starts to transform into a hexagonal symmetry (Figure 3.16(a)-(c) and (d)-(f)). The 6H- and 4H-SiC (0001) on-axis substrates show exactly the same etching behavior. In both cases, one edge of the hexagon is parallel to the <11-20> direction of the α-SiC.

The mask size and thickness considerably decrease during the etching process due to strong physical sputtering of energetic ions, and it is completely removed after the etching during 840 sec. Therefore, the SiC nanopillars are no longer protected by the mask after long etching and begin to be etched. In this way, their transversal cross section, perpendicular to the z-axis of the SiC pillar, is clearly revealed (see top-view images in Figure 3.16(c), (f), (i), (l) and (n).

The morphology of etched SiC nanopillars on 6H-SiC (11-20) substrate shows an asymmetric pillar shape at the initial stage of etching (Figure 3.16(g)), and further etching makes the pillars appear with a distorted pentagon-based pyramid structure (Figure 3.16(h-i)). This unique morphology of SiC pillar is related to the unintentional misorientation crystal plane toward the [0001] directions.

For the growth of 6H-SiC (11-20) substrates used in this study, α-plane seeds were prepared by attaching four equivalent rectangular samples (15 mm × 50 mm) of the α-plane in parallel and the additional process (grinding) to make a circular shape [23]. The grooves near the connected regions induce the unintentional off-axis of the (11-20) plane. Hence, the α-plane after reactions is slightly misoriented toward the [0001] direction. As a result, the etched SiC pillars on 6H-SiC (11-20) substrate are tilted at an angle of misorientation, just like the leaning tower of Pisa, instead of standing upright. The apex of pillar moves from the center rhombus towards the [0001] direction (Figure 3.16(h) and (i)).

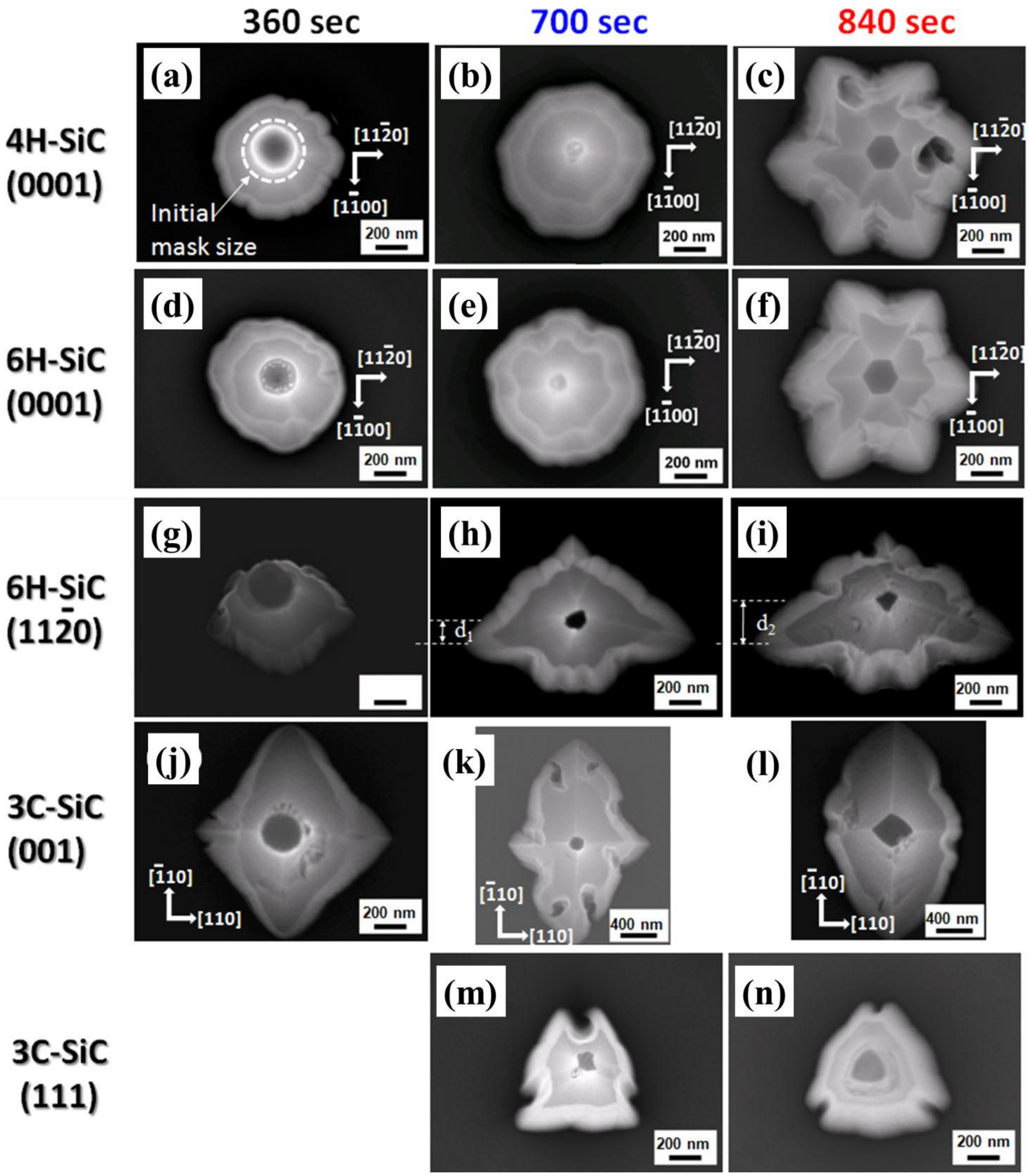

Figure 3.16 Top-view SEM images of SiC nanopillar after etching for (a, d, g, j) 360 sec, (b, e, h, k, m) 700 sec, and (c, f, i, l, n) 840 sec with different polytypes and crystallographic orientations. (a-c) 4H-SiC (0001) on-axis, (d-f) 6H-SiC (0001) on-axis, (g-i) 6H-SiC (11-20) misoriented toward [0001], (j-l) 3C-SiC (001) and (m,n) 3C-SiC (111), respectively.

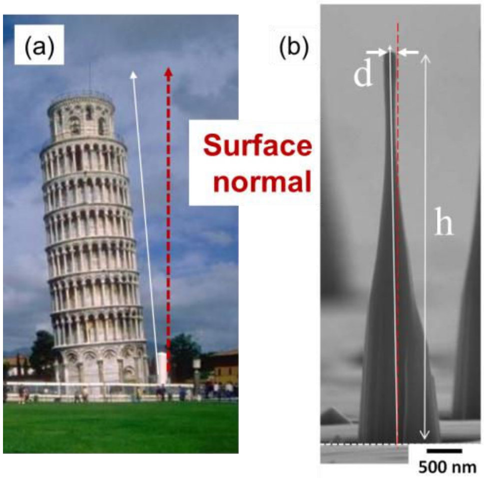

Figure 3.17 (a) Photo image of Leaning tower of Pisa and (b) SEM image of misoriented 6H-SiC (11-20) pillar (11-20).

The misorientation degree (θ) of α-plane as shown in Figure 3.17 can be roughly estimated from the following formula:

$$\theta = \tan^{-1}(d/h), \qquad \text{Eq 3.3}$$

where d is the apex-shift distance and h is the pillar height (see Figure 3.16(h) and (i)).

The estimated misorientation degrees (θ) are around 1.6° and 3.0° from Figure 3.16(h) (d_1= 160 nm, h_1= 5.8 μm) and Figure 3.16(i) (d_2= 300 nm, h_2= 5.6 μm), respectively. And it ranges between 1.0° and 3.0° over the entire sample area.

Several etching techniques are used for the evaluation of the crystal quality, the determination of defect types and SiC polytypes [35, 36]. ICP dry etching of the SiC nanopillars would be used to estimate the misorientation degree of the crystal planes. For future work, it is needed to investigate the correlation between the estimated misorientation angle by etching of SiC nanopillar and the measured misorientation angle by X-ray diffraction methods [37]. The top view of SiC pillar on 6H-SiC (11-20) substrate shows a distorted pentagonal shape due to the misorientation of α-plane, as shown in Figure 3.16(i).

It is interesting to note that the etched SiC nanopillars on the 3C-SiC (001) substrate gradually transform into a rhombic pyramid structure (Figure 3.16(j)-(l)). The two diagonals of a rhombus are corresponding to the direction of [-110] and [110], respectively. These directions have been indicated by the substrate supplied well before the ICP experiment. The facet appearing on the top of 3C-SiC (001) nanopillar clearly shows a rhombus shape (Figure 3.16(l)).

Generally, most as-grown SiC NWs fabricated by the bottom-up methods are cylinder shaped of 3C-SiC structure oriented towards the <111> direction [1, 2]. For heteroepitaxial growth of 3C-SiC on Si substrate, Si (001) plane is commonly used to minimize the density of planar defects, such as twin boundaries and anti-phase boundaries, with increasing thickness through mutual canceling [38, 39]. In addition, it is also possible to achieve thick SiC epitaxial layers on large area substrates using Si (001) substrate. In the present case, the etched pillars 3C-SiC exhibits a crystal orientation with [001] direction.

It seems that the etching behavior of SiC nanopillars is quite similar to the growth of SiC structure. The growth of 3C-SiC heteroepitaxial layer on mesa structure with different polytype substrates have gradually expanded into a hexagonal shape on 4H-SiC (0001) and a rhombus shape on Si (001) during reactions, respectively [40, 41]. These phenomena are well explained by in-plane anisotropy of the growth rate. In the same way, the sufficiently long etching process imposes developing of the planes with the lowest etch rates in all the different polytypes and crystal orientations.

The morphology of etched SiC nanopillars on 3C-SiC (111) substrate shows a triangle pillar shape after the etching (Figure 3.16(p) and (q)) that reveals the {111} equivalent planes, which is the densest planes of the SiC phase (or the lowest surface free energy).

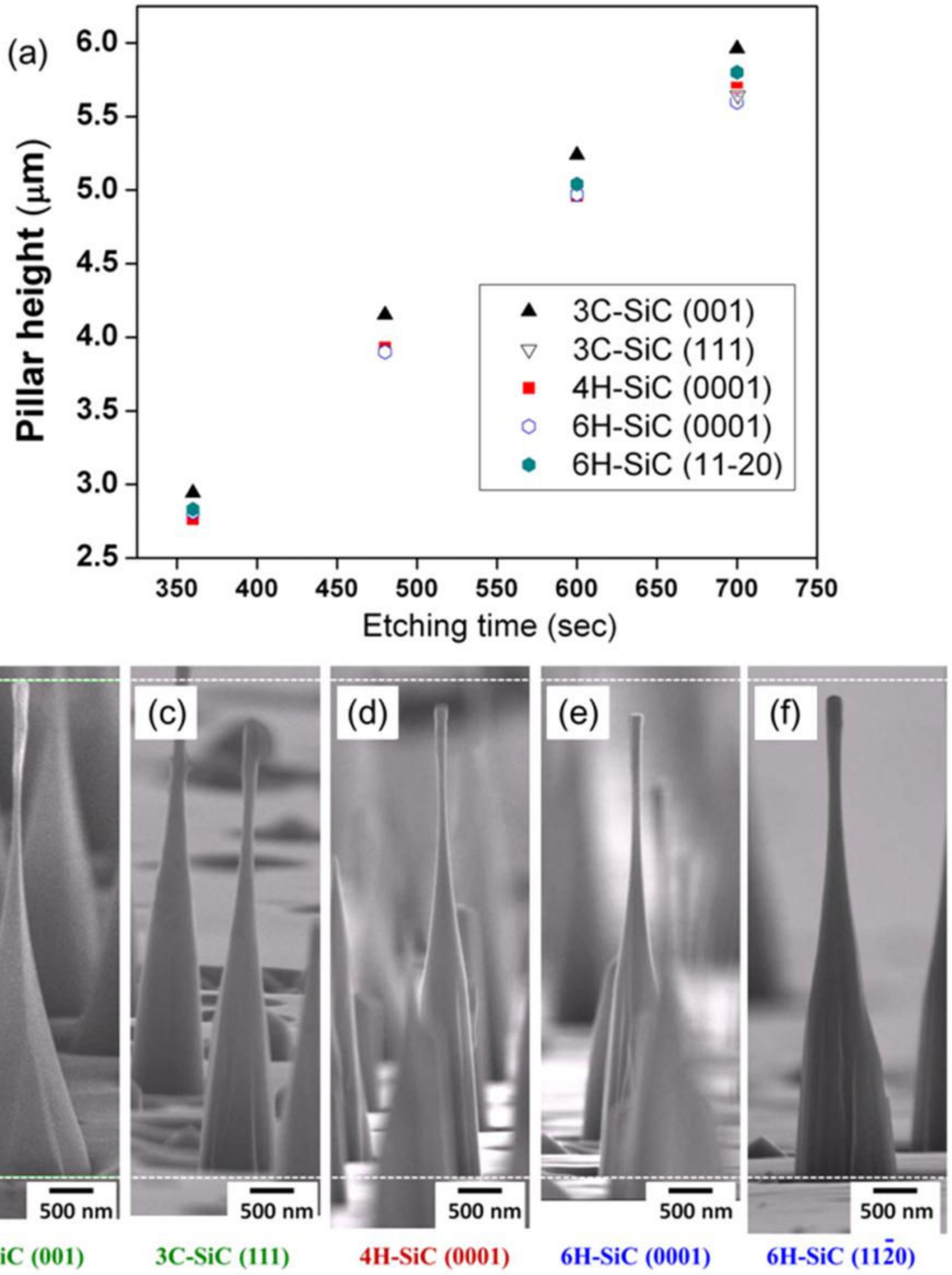

Figure 3.18 (a) Pillar height with different polytypes and orientations as a function of etching time, (b-f) the morphology of etched SiC pillars after 700 sec etching time, (b) 3C-SiC (001), (c) 3C-SiC (111), (d) 4H-SiC (0001), (e) 6H-SiC (0001) and (f) 6H-SiC (11-20), respectively.

Figure 3.18(a) shows the SiC nanopillars height with different polytypes and crystallographic orientations as a function of the etching time. The pillar height is proportional to the etching time. The time-averaged etch rate of 3C-SiC pillar (510 nm/min) is slightly larger than that of hexagonal SiC polytypes (490 - 500 nm/min). It is thought that the low crystalline quality of hetero-epitaxially grown 3C-SiC layer, which is induced by the large lattice mismatch (almost 20%) and the difference of thermal expansion coefficient (almost 8%) between the 3C-SiC layer and the Si substrate, could be one of the possible reasons of higher etch rates than in the case of the single crystal substrates of α-SiC [42]. The observed trend is comparable to the results reported elsewhere [43], which shows the etch-pit depth of 3C-SiC higher than that of other polytypes. In another study, the depth of etch pit decreased with increasing the hexagonality of SiC [43]. But, there is no obvious difference in etch rates of SiC pillars according to hexagonal polytypes and crystallographic orientations.

Figure 3.18(b-f) show the etching profile of SiC pillars with different polytypes and crystallographic orientations after 700 sec etching time. The minimum diameter of etched pillars can be shrunk into below 100 nm owing to the mask erosion. The length of these pillars (below 100 nm in diameter) is around 1.5 μm, which is long enough for the fabrication nano FET. It will be discussed in detail in chapter 4.

3.3.7 Fabrication of SiC FinFET like structures

A FinFET structure by etching the hetero-epilayer could be another possible to achieve SiC nanostructures. The 3C-SiC hetero-epilayer used for this study has been grown on Si substrate (see section 1.2.1, p 7) at CRHEA laboratory (Centre de Recherche sur l'Hétéro-Epitaxie et ses Applications, Valbonne France). The thickness and doping level of 3C-SiC hetero-epilayer are 1.0 μm thick and n-doped at 10^{16} cm^{-3}, as shown in Figure 3.19(a),

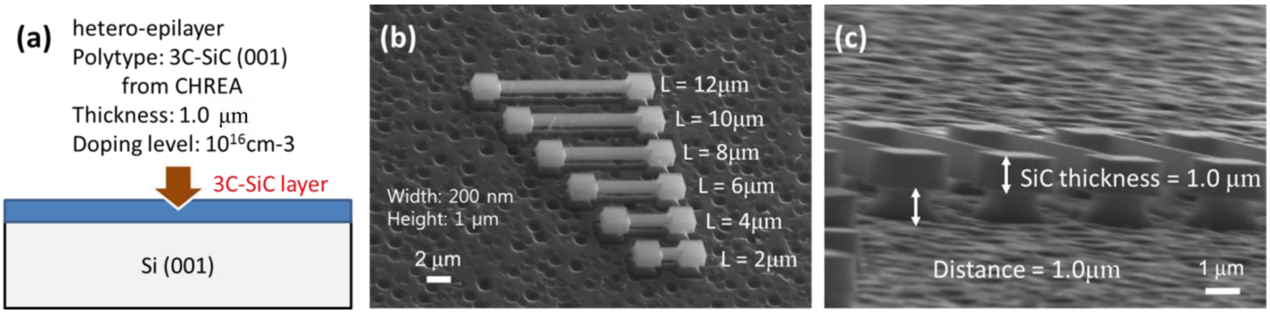

Figure 3.19 (a) Hetero SiC epilayer on Si substrate used for the fabrication of 3C-SiC FinFET structure, (b) tilted-view (45°) SEM image of 3C-SiC FinFET arrays with different (2 – 12 μm) gate length, (c) side-view SEM image of 3C-SiC FinFET.

Ni line mask patterns (thickness: 100 nm, width: 200 nm and different gate length (2 – 12 μm)) are fabricated by e-beam lithography on the 3C-SiC hetero-epilayer. The total gas flow rate, ICP coil power, substrate bias voltage, chamber pressure and etching time for etching conditions are 50 sccm ($SF_6/O_2 = 40/10$ sccm), 1500W, 150V, 6 mTorr and 150 sec, respectively. Figure 3.19(b) shows 3C-SiC FinFET arrays fabricated by ICP etching. SEM image (Figure 3.19(b)) puts in evidence holes coming from the Si substrate because 2 μm have been etched (Figure 3.19(c)). The dimensions of 3C-SiC FinFET after removing Ni mask are 200 nm width and 1 μm thickness with different gate length; and the 3C-SiC channel of FinFET is well separated from Si substrate (see Figure 3.19(c)).

To further reduce the height of 3C-SiC FinFET, another experiment has been carried out with two steps etching process. Ni line mask was removed after the ICP etching for 20 sec (step 1, Figure 3.20 (b)). After removing the Ni mask (HCl for 2 h), further ICP etching for 110 sec have been done to completely remove the remained 3C-SiC layer (step 2, Figure 3.20(b)). After whole etching process as illustrated in Figure 3.20 (a), the 3C-SiC FinFET array with reduced height (200 nm) has been achieved in Figure 3.20(c).

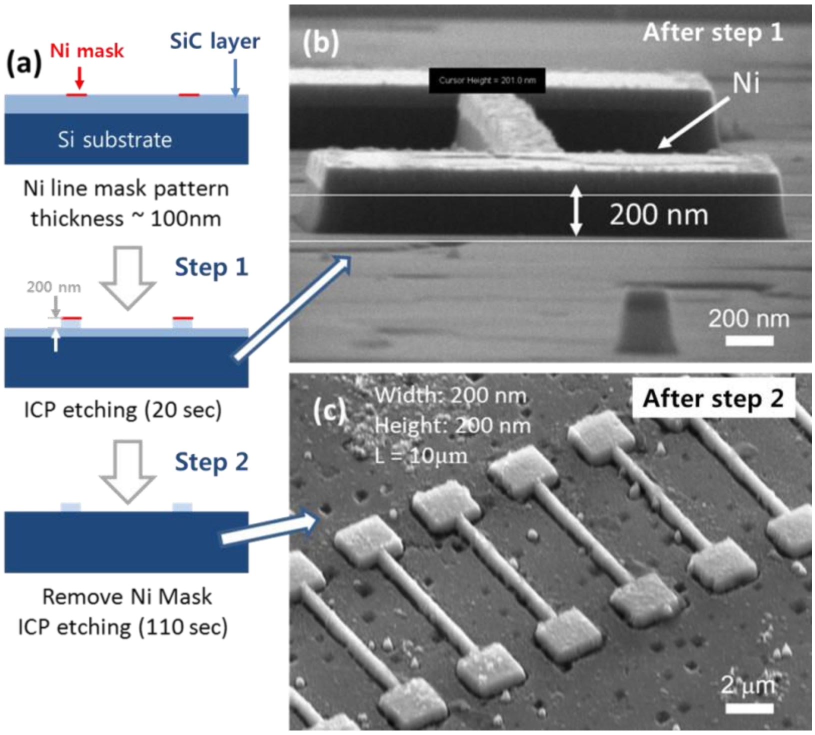

Figure 3.20 (a) Process flow chart of SiC FinFET with reduced height (200 nm), (b) side-view SEM images of 3C-SiC FinFET after short etching (20 sec), (c) tilted-view (45°) SEM images of 3C-SiC FinFET arrays with reduced height (200 nm).

The 3C-SiC FinFETs (width: 200 nm, height: 200 nm and 1 μm) with different gate length have been successfully demonstrated in this study. However, metal pads to contact the probe tip could not have been fabricated on these samples, (and electrical properties of 3C-SiC FinFET could not have been measured). Substrates used in this study were probably too thin and substrates were broken after optical process prior to metallization and finally E-beam lithography should have been used.

In our case, the height of 3C-SiC FinFET has been reduced by ICP etching process from 1 μm to 200 nm. If thin 3C-SiC hetero-epilayer (below 100 nm) are available, small dimensions (below <100 nm) of 3C-SiC FinFETs could be achieved. The 3C-SiC FinFET array of functionalized with specific receptors could be utilized for bio-sensors for the multiplexed detection of bio-hazardous agents.

3.3.8 Experiments with the Bosch process

The Bosh process could be a promising method to realize straight high-aspect-ratio SiC nanopillars [44]. The Bosch process, or also known as Time Domain Multiplexed (TDM), is named after the German company Robert Bosch GmbH, which patented the process [44]. Long etching time leads to undercut etching profile due to isotropic chemical etching by direct exposure of F radicals from the plasma.

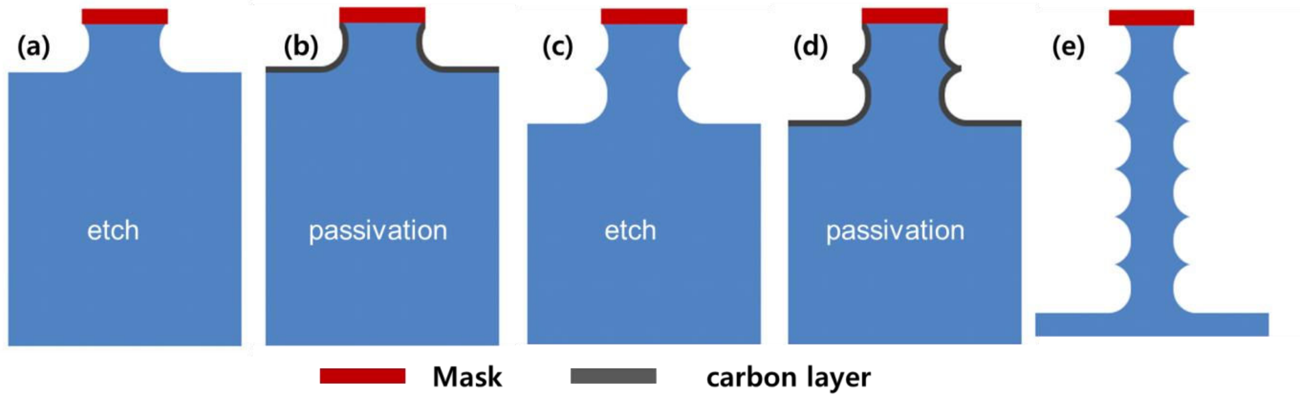

Figure 3.21 Schematic diagram of Bosch process (a) etch stage and (b) passivation in first cycle, (c) etch stage and (d) passivation in second cycle, (e) fabricated deep features after several cycles.

To prevent undercutting phenomena, Bosch process employs carbon passivation process during the etch process by exposing carbon fluorine based gas (such as C_4F_8). The deposition and etch steps are separated in time, the process switched continuously between an etching and a passivation process in cycles, as shown in Figure 3.21. In the passivation step, plasma breaks apart the strained cyclic hydrocarbon C_4F_8 into highly excited fragments (Eq 3.4).

$$C_4F_8 \xrightarrow{\text{gas phase}} 2C_2F_4 \xrightarrow{\text{gas phase}} C,\ F,\ CF,\ CF_2,\ CF_3 \qquad \text{Eq 3.4}$$

The individual fragments react one with another on the exposed surface and build up a more or less strongly cross-linked layer of polymer (Eq 3.**5**) [3], as show in Figure 3.21(b).

$$CF_2 \text{ or } C_2F_4 \rightarrow (CF)_x \qquad \text{Eq 3.5}$$

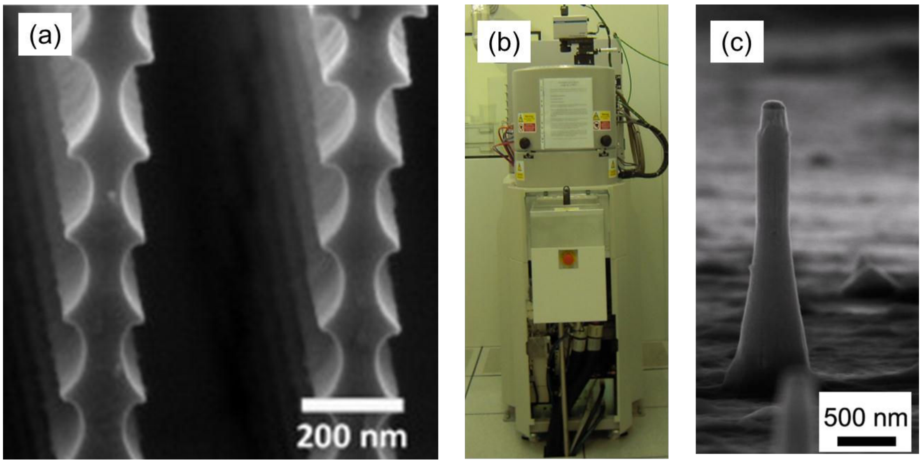

Figure 3.22 (a) Scalloped Si trenches after Bosch process [45], (b) STS multiplex equipment used for Bosch process and (c) preliminary experimental result of etched 3C-SiC nanopillar after Bosch process (initial mask size = 300 nm).

During the etching stage, the CF_x molecules are removed by combination of physical ion sputtering and chemical reactions. Meanwhile, the sidewalls thus remain protected during the etch stage due to the directional ion bombardment in Figure 3.21(c). These etch/passivation steps are repeated many times over resulting in a large number of very small isotropic etch steps taking place only at the bottom of the etched pits in Figure 3.21(e).

Figure 3.22(a) shows deep trench structures in Si after the etching of Bosch process, the etched structures using Bosch process generally show the "scalloped" morphology due to isotropic etching during the etch stage of Bosch process. The scalloping amplitude and pitch can be controlled by duration of etching and passivation steps of Bosch process. Short cycles (the combination of etching and passivation steps) yield smoother walls, and long cycles yield a higher etch rate.

A preliminary test of Bosch process is conducted on a 3C-SiC substrate using “STS multiplex etcher”[a] at CIME in Figure 3.22(b). The detailed experimental conditions of etching and passivation steps are listed in Table 3.3. Figure 3.22(c) shows a SEM image of etched 3C-SiC nanopillar after 20 cycles of Bosch process. The 3C-SiC nanopillar height and aspect ratio are 2.4 µm and 3.2 after Bosch process, respectively. Total etching time is 600 sec (etching duration (30 sec) with 20 cycles), so the corresponding etch rate in this etching condition is 240 nm/min. This etch rate is quite low compared to previously reported value (550 nm/min) in section 3.3.4. It might be attributed to the passivation step (15 sec) during each cycle of Bosch process.

Table 3.3 Experimental conditions of Bosch process for the etching of 3C-SiC nanopillar (Total = 20 cycles).

Etching conditions	
Coil/Bias power	800 / 75 W
Chamber pressure	5 mTorr
SF_6/O_2	40/10 sccm
Duration	30 sec

Passivation conditions	
Coil/Bias power	400 / 30 W
Chamber pressure	10 mTorr
C_4F_8	20 sccm
Duration	15 sec

It is noticeable that non-scalloped surface of SiC nanopillar is observed instead of "scalloped" morphology (see Figure 3.22(c)). It is believed that non-scalloped surface of SiC nanopillar originated from the anisotropic etching instead of the isotropic etching during the etch step of Bosch process. The etched 3C-SiC nanopillar in Figure 3.22(c) is just our first etching result of Bosch process.

The Bosch process might be promising method for the fabrication of deep features with high aspect ratio, but several parameters (such as etching condition (coil/bias power), the flow rate of C_4F_8 during the passivation steps, the duration of each cycles) should be further optimized to elaborate high aspect ratio SiC nanostructures with straight sidewalls.

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[a] An ICP system is fabricated by SPTS Inc. It provides the passivation step with carbon based gas (e.g. CF_4) and time domain multiplexed process (the repetition of the etching and passivation step).

3.4 Conclusion

In this chapter, etching characteristics of SiC have been investigated using ICP etching in SF_6/O_2 plasma to elaborate SiC nanopillars. In the previous study [46], the SiC nanostructures (dia. 55 nm) have been demonstrated by etching hetero-epitaxially grown 3C-SiC layers (thickness ~ 55 nm) on Si substrate with a line mask pattern. But, these SiC nanostructures still suffered from low crystalline quality due to large lattice mismatch (almost 20%) and the difference of thermal expansion coefficient (almost 8%) between the 3C-SiC layer and the Si substrate. We have realized high aspect ratio SiC nanopillars with high quality using single crystalline SiC substrates by optimizing a set of experiments (such as, mask materials, O_2 concentration, bias voltage, chamber pressure, and etching time) in SF_6-based plasma.

Ni has been evaluated as better mask material than other materials (Al and Cu). The etching profile of SiC nanopillars and etch rate are strongly controlled by O_2 concentration in the etching gas. The presence of appropriate O_2 level (20 %) provides the driving force for removing the carbon by forming volatile etching products, such as CO, CO_2 and CF_2. In addition, the addition of O_2 can keep fluorine (F) radical concentration high by reacting with unsaturated CF_n and SF_n bonds so that F radicals do not combine with them. The effects of bias voltage and chamber pressure are also investigated using a small circular mask pattern (115 nm). The obtained SiC nanopillars at an optimum bias voltage (300 V) and pressure (6 mTorr) exhibit a high aspect ratio (7.4) with an etching depth of 2.2 μm.

The etching profile and mask evolution have been monitored over the etching time using a large circular mask pattern (370 nm). As the etching progresses, the pillar height and aspect ratio increase until the mask removal point. The vertical etch rate of the mask remains constant throughout the etching process, but the lateral etch rate of the mask gradually increases with increasing etching time. Under the optimal etching conditions using a large circular mask pattern with 370 nm diameter, the obtained SiC nanopillars exhibit high anisotropy features (6.4) with a large etch depth (>7 μm).

Effect of different polytypes (4H-, 6H- and 3C-SiC) and crystallographic orientations ((0001) and (11-20) of 6H-SiC, (001) and (111) of 3C-SiC) have been investigated in order to realize SiC nanopillars. The morphology of etched SiC nanopillars has shown interesting features depending on the polytypes and crystal orientations. A hexagonal, rhombus and triangle based pillar structures have been obtained using α-SiC (0001), 3C-SiC (001) and 3C-SiC (111) substrates, respectively. The hexagonal, rhombus and triangle based SiC nanopillars revealed by the etching method is first presented in this study. These unique morphologies of SiC nanopillars are originated from a complex interplay between their polytypes and crystal orientations, which reflects the so-called Wulff's rule. The etched SiC nanopillars on 6H-SiC (11-20) show a distorted pentagon based pyramid structure due to the crystal misorientation during the growth.

Preliminary experimental results of SiC FinFET structures and Bosch process are also presented in this chapter. The 3C-SiC FinFETs (width: 200 nm, height: 200 nm and 1 μm) with different gate length have been successfully demonstrated by etching the 3C-SiC hetero-epilayer with Ni line patterns. If thin 3C-SiC hetero-epilayer (below 100 nm) are available, small dimensions (below <100 nm) of 3C-SiC FinFETs could be achieved. In addition, the Bosh process could also be another promising method to realize straight high aspect-ratio SiC nanopillars. The 3C-SiC nanopillar height and aspect ratio are 2.4 μm and 3.2 have been achieved after Bosch process, but it is still needed to optimize several parameters to elaborate high aspect ratio SiC nanostructures with straight morphology, (e. g. the duration of each cycles (passivation and etching step), coil/bias power during the etching step and the flow rate of carbon source during the passivation steps).

In this chapter, top-down approach with dry plasma etching has shown the capability to achieve single crystalline SiC nanopillars with a high aspect ratio (6 - 7). It will allow the study of electrical properties of single crystalline SiC nanostructures, and it opens new possibilities to apply it in widespread applications, such as robust nanoneedles for AFM probes or field emitters.

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Chapter 4. SiC nanoFETs

4.1 Introduction: the state-of-the-art of nanoFET

The development of NWFETs is opening promising perspectives for future high-performance electronic devices. Many efforts have been done to exploit excellent electrical properties of NWs. The device performance has been improved very significantly. In this section, I'll introduce the major advance and the state-of-the-art of nanoFETs and discuss several issues for the fabrication of nanoFETs. Then, devices fabrication process and the electrical characterization of SiC nanoFETs will be presented in section 4.2 and 4.3.

▣ The state-of-the-art of nanoFETs

Best reported results (in terms of carrier mobility) for different material and geometries NWFETs are listed in Table 4.1. All devices listed in Table 4.1 operated in depletion mode. Si NW based nanoFET have been most extensively studied owing to their well-developed recipes for the size and doping control during the growth mode. The Si nanoFET based on single-crystalline (n-type and p-type) Si NWs leads to high electron (560 $cm^2{\cdot}V^{-1}s^{-1}$) and hole (307 $cm^2{\cdot}V^{-1}s^{-1}$) mobility. It is difficult to directly compare these motilities with Si bulk because authors did not give the doping concentration in Si NW channels, but the mobility of Si nanoFET is quite smaller compare to the bulk material (1400 $cm^2{\cdot}V^{-1}s^{-1}$ for n-type, 470 $cm^2{\cdot}V^{-1}s^{-1}$ for p-type at a doping concentration of 1×10^{16} cm^{-3} [1]). It is believed that the access resistance even in the ON state does still contribute in the experimental device transconductance, consequently leading to an underestimate of its channel component, and thus to a lowered mobility [2].

Table 4.1 The state-of-the-art of different semiconductor NWFETs.

	n-type Si NW	*p-type Si NW*	*n-type InAs NW*	*p-type Ge/Si NW*	*GAA n-type Si nanoFET*	*GAA p-type Si nanoFET*
Diameter	~ 5 nm	~ 20 nm	50 - 70 nm	15 nm	≤ 5nm	≤ 5nm
Length	1 μm	1 - 2 μm	1 - 2 μm	~ 190 nm	180 nm	180 nm
g_m (μS)	0.8	1.25	1	26	N/A[a]	N/A
I_{on}/I_{off}	N/A	10^7	2–100	580	10^6	10^6
Subthreshold slope (mV/decade)	N/A	160	N/A	100	63	66
μ ($cm^2{\cdot}V^{-1}s^{-1}$)	560	307	3400	730	750	325
Reference	[3]	[4]	[5]	[6]	[7]	[7]

Thanks to InAs small effective electron mass (0.023 m_o), InAs-based NWFET shows a high electron-mobility (3400 $cm^2{\cdot}V^{-1}s^{-1}$), which shows the potential for high speed electronic applications [5]. Ge/Si core/shell NWs have shown a high-mobility hole carriers 730 $cm^2{\cdot}V^{-1}s^{-1}$ [6], which are three to four times higher than state-of- the-art Si p-MOSFETs [8], since the valence band offset of ~500 meV between Ge and Si confines the hole-gas in the core of Ge NW.

The surrounded-gate Si NWFETs (diameter ~ 5 nm) fabricated by top-down approach [7] show good performance (750 $cm^2{\cdot}V^{-1}s^{-1}$ for n-type, 325 $cm^2{\cdot}V^{-1}s^{-1}$ for p-type) due to excellent electrostatic control in

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[a] N/A: Not available

terms of ideal subthreshold slope (~ 63 mV/dec) for n-type and (~ 66 mV/dec) for p-type, low drain-induced barrier lowering (~ 10 mV/V) and high I_{ON}/I_{OFF} ratio (~ 10^6) . Our experimental results of SiC nanoFET and a comparison with the state-of-the-art of SiC NWFET will be presented in section 4.3.3.

4.1.1 Important issues for the nanowire FETs fabrication

To fulfill the potential of NWs as building blocks for future electronics, several issues still must be developed. These issues related to device fabrication, including doping, contact, gate structures, hetero-structures and vertical integration will be introduced in this section.

▣ Alignment of nanowires (or integration techniques)

Effective integration and assembly techniques must be developed to arrange large numbers of NWs into complex integrated circuits. Up to now, several integration techniques have been demonstrated, such as electric field directed assembly [9], fluid-assisted assembly [10] process and “grow-in-plane” [11]. Despite this encouraging achievement, a continued focus on assembly techniques are needed to further integrate NWs arrays with controlled orientation and spatial position.

▣ Doping or modulation of chemical composition

For practical applications of NWs based electronics, it is also strongly needed to develop reliable and reproducible (both p- and n-type) doping techniques. Many research works have been done to be able to control the doping types and concentration by in situ doping during the growth of NWs via the bottom-up methods. But, in situ doping method could not exactly control the doping concentration , and it also shows non-uniform dopants distribution within the NW channel [12]. A homogeneous dopant distribution is a critical issue in order to ensure a stable and reproducible device performance. Dopant incorporation during the device fabrication could be one possible approach to overcome these limitations. One possibility is by using ion implantation characterized by high doping-value controllability and selective area doping [13]. It could be applicable not only for NWFETs, but also for the formation of NW-based p-n junctions and bipolar junction transistors. In case of SiC nanoFET, the in situ doping method is more favorable to incorporate the dopant in the channel than the ion implantation methods [14]. Because it is required high voltage to inject the dopant due to densely packed atomic structure of SiC. Consequently, the implantation of high-energy ions creates lattice damage within the NW channel. Therefore, it needs additional process (high temperature annealing) to reduce the lattice damage induced by high dose ion implantation.

▣ Contact issues

In case of conventional MOSFETs, the source and drain (S/D) contacts are heavily n-type doped to obtain ohmic contacts. And then, metalized contacts are made to both S/D. However, in most cases of nanoFETs, metal contacts are directly formed on the NWs channel without any doping. Therefore, Schottky contacts are generally formed at the metal/semiconductor interface of nanoFETs [15, 16]. As a result, the performance of nanoFETs is strongly affected by the contact properties. In addition, the intrinsic NWs channel resistance becomes sufficiently small at the nanometer scale. The S/D resistance could be dominant factor, which limit the saturation current of nanoFETs. Many efforts have been done to tailor the interface between the metal and NWs, such as changing the metal species and optimizing the annealing conditions. In particular, the drive performance of nanoFETs can be significantly improved by appropriate silicidation of S/D for Si NWs. Silicidation modifies the metal–semiconductor interface and forms stable silicide–silicon interface. The silicidation process will be studied for our SiC NWFETs in section 4.3.2.

▣ Hetero structures

The unique theoretical transport characteristics of axial and radial NW heterostructures make them excellent building blocks for high performance NWFETs through energy band-edge engineering. Moreover, it provides an ideal model system to probe unique properties and physical phenomena. For example, radial Ge/Si NW heterostructures show high performance p-channel NWFETs due to the large valence band offset and Fermi level pinning between Ge and Si. As a result, 1D hole gas can be formed and confined inside the Ge core even with intrinsic core and shell materials [6].

Hetero NWFETs based on axial NW heterostructures fabricated by varying the composition show unique electrical transport compared to a single chemical composition NWs, since it can easily implement lateral heterostructures beyond the limitation of lithography. In that case, carriers are confined in the axial heterostructures. Songmuang et al. [17] have observed unique quantum transport (Coulomb blockade effect) in axial GaN/AIN NW heterostructures, because the incorporation of two AlN tunnel barriers causes confinement to occur within the channel of GaN NW.

Several SiC radial heterostructure have been reported up to now, such as SiC-SiO_2 or SiC-BN core-shell and Si-SiC core-shell structures. If SiC is served as core structure, SiC-SiO_2 or SiC-BN core-shell structure might be suitable for building blocks of nanoelectronics devices, since the electron density is confined to the core and the shell serves as a gate dielectric. In case of Si-SiC core-shell structure [18], the outer shell of SiC provides an ideal interface capable of bridging biomaterials and nanoelectronic devices because of their excellent biocompatibility, while the electrical transport is maintained Si core structure.

▣ Gate structures

To enhance gate controllability and field uniformity in channel, devices with different gate structure: double-gate, tri-gate, Π-gate, Ω-gate and gate-all-around (GAA), have been explored [19]. As the name suggests, the GAA FET features the gate fully surrounding the channel body and thus providing the best possible electrostatic control (nearly ideal subthreshold slopes). In addition, it also provides superior immunity against short-channel effects compared to the ultrathin body devices [19].

There is no report on the GAA SiC NWFETs up to date. It is believed [2] that even the implementation of a top-gated device with a high-k dielectric will result in improved carrier mobility and the reduction of the threshold voltage compared to back-gate geometry due to a much more efficient gate response.

▣ Vertically integrated nanoFETs

Vertically aligned NWs have attracted attention for their potential 3D integration in order to realize vertical surround-gate field-effect transistor (VS-FET) since they are geometrically suitable for achieving a surrounding gate structure. This geometry leads to excellent gate controllability and the suppression of short channel effects, it also offers an attractive alternative approach to construct 3D integrated circuits, as shown in Figure 4.1.

In case of the fabrication of common gate (or drain) VS-FET, vertically grown NWs on the substrate can be used for direct device fabrication without any complicate integration technique. In addition, it needs an ultimately small footprint for FETs. VS-FET with various materials, such as IV group NWs (Si, Ge, SiGe), III/V group (InAs), have been reported in the literature.

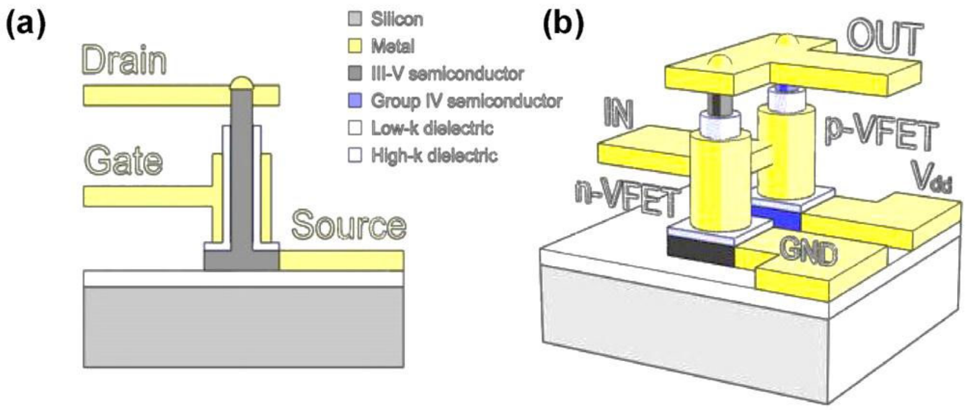
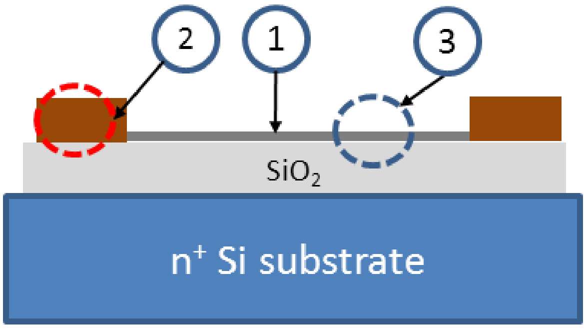


Figure 4.1 Illustration of (a) individual and (b) integrated vertical VS-FETs [20].

However, in spite of these geometrical advantages of VS-FET, VS-FET of Si demonstrated significantly higher subthreshold slope (120 mV/dec), and lower I_{on}/I_{off} ratio (~ 10^5) [21] than current state-of-the-art with top-down fabricated Si devices (subthreshold slope: 63 mV/dec and I_{on}/I_{off} ratio: 10^6) [7]. The reasons for their inferior performance of VS-FETs are connected with inherent to their geometry difficulties of processing. Thus, problems such as contact resistance at the S/D interfaces, nonuniform dopant distribution within the NW channel, charge trapping at the gate dielectric interface, are amplified in this case [22]. To further improve the VS-FET device performance, it should improve the semiconductor NWs surface passivation to remove surface state charge trapping sites [22], by the deposition of high *k* dielectric materials such as HfO_2 and Al_2O_3, or nitridation or sulfidation of the NW surface [23, 24]. The eventual presence of metal catalyst species (due to the growth) is also important. It can influence not only the morphology of as-grown NWs but also the majority charge carrier in the channel. If metal alloy still remains on the NW's sidewall after the reactions, it induces the surface state charge trapping sites on the channel. As a result, it leads to the degradation of device performance. Even though there is no report on the VS-FETs based on SiC NWs, vertical aligned SiC NW arrays have already been developed by both bottom-up [25] and top-down methods [26]. So, SiC NWs based VS-FETs would may be demonstrated within the near future.

4.1.2 Some challenges for high performance of SiC nanowire FETs

Even though the electron mobility of the three most important SiC polytypes (4H-, 6H- and 3C-SiC) in bulk show several hundreds of $cm^2 \cdot V^{-1}s^{-1}$ [27], all reported results of 3C-SiC NWFET show poor device performance in terms of transconductance and carrier mobility (several of $cm^2 \cdot V^{-1}s^{-1}$), as mentioned in Chapter 1.



1	Poor quality of SiC NW (high density of stacking faults and unintentional doping)
2	Metal contacts
3	NW-gate oxide interface

Figure 4.2 Three major issues for SiC NWFET.

There are three major issues for the fabrication of SiC NWFET, as depicted in Figure 4.2. First, one of most important problems of 3C-SiC NWFET is SiC NW quality itself. SiC NWs fabricated by bottom-up methods significantly suffer from a high density of stacking faults and unintentional n-type doping. This kind of structural defect could eventually lead to poor electrical performances although it has not been demonstrated up to now. Therefore, it may be developed another approach (such as top-down approach) to fabricate the SiC nanostructures, which significantly reduces the density of stacking faults.

Second, as devices size is scaled down into nanometer region, the channel resistance of NWs becomes sufficiently small. Therefore, the S/D contact properties become a dominant factor in determining the device performance. Jang et al. [28] have shown that Ni/Au ohmic contacts on SiC NWs had the lower specific contact resistances compared to the values of Ti/Au ohmic contacts. However, the contact property of SiC NWFET has not been investigated in much detail relative to that of Si NWFET. Moreover, the interface between the metal and NWs needs to be improved by optimizing the annealing conditions.

Last, poor device performance might also be due to weaker electrostatic gating effects, lower capacitances and weak gate coupling caused by back gate configuration and the poor-quality interface between SiC NW and gate oxide. To enhance gate controllability and field uniformity in channel, there is need to develop the integration process with top metal gate structure or the GAA FET features incorporating high-κ dielectric.

Our efforts to address these three major issues are described in the following sections (4.2 and 4.3).

4.2 Fabrication process of SiC nanowire FETs

In this study, two different kinds of SiC nanoFETs have been developed to reveal the electrical properties of SiC nanostructures, as shown in Figure 4.3.

- Type A (denoted as SiC NWFETs) was fabricated by using SiC NWs prepared via bottom-up method, with diameters ranging from 40 to 80 nm and with several lengths (1- 10 µm).
- Type B (denoted as SiC NPFETs) was fabricated by using top-down SiC nanopillars (NPs) with average diameter of 100 nm and a length of 1 µm.

Experimental details of each device will be discussed in this section.

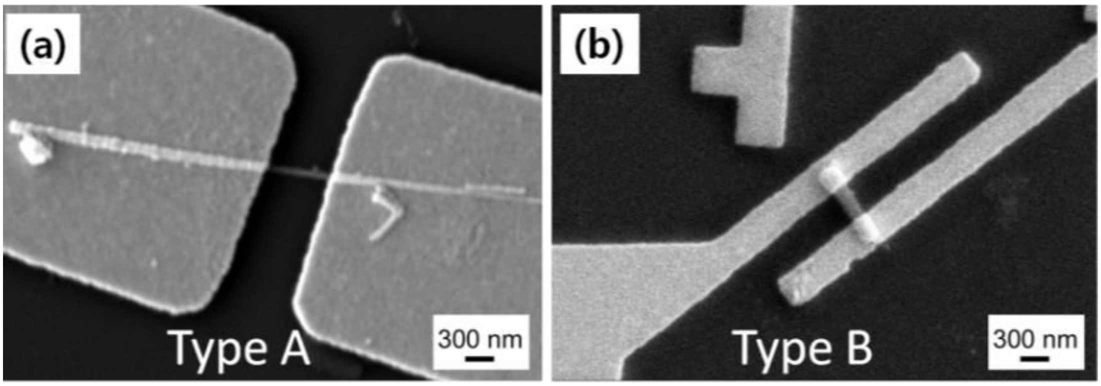


Figure 4.3 SEM images of two different kinds of SiC nanoFET;
(a) Type A: SiC NWFET and (b) Type B: SiC NPFET.

4.2.1 Fabrication steps of SiC NWFETs

In this section, the whole process of a back-gated SiC NWFETs fabrication will be described from chemical treatment of as-grown SiC NWs to e-beam lithography (EBL) for the S/D contact formation. Indeed, the simplest way to characterize the electrical properties of NWs is an implementation of a back gated configuration, which uses highly doped Si substrate as a back gate.

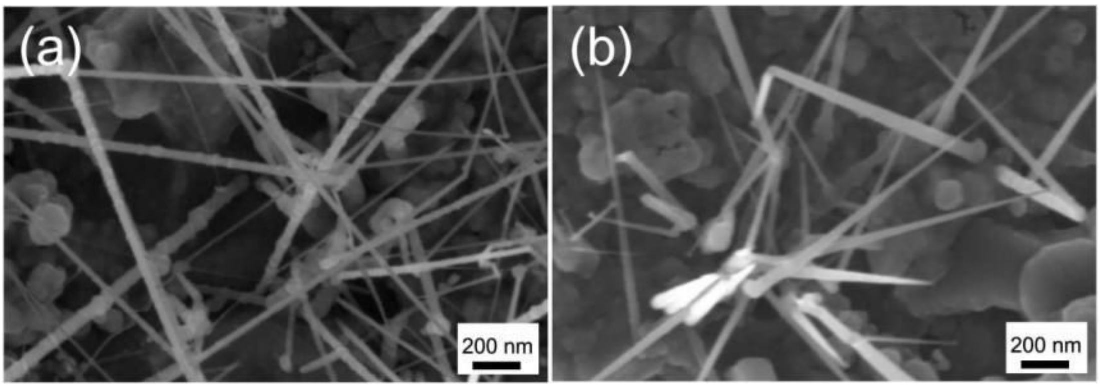


Figure 4.4 SEM images of (a) a cylinder shape [29] and (b) a needle shape of SiC NWs [30].

▣ Nanowire growth

Cylinder-shape of SiC NWs used in this study were prepared on a silicon wafer by the VLS method using Ni clusters as the catalyst [29], (see CVD method in the section 1.3.3.- p14). These samples have been grown by Dr. G. Attolini and his group from IMEM-CNR. As-grown SiC NWs are predominantly 3C polytype with <111> growth axis and high density of stacking faults. The diameter of SiC NWs is ranging from 40 to 80 nm with several lengths (1- 10 μm) (see Figure 4.4(a) and the section 1.3.3.- p18). The same group fabricated needle-shape SiC NWs, which also have been used in the present study [30]. The diameters of needle-like SiC NWs are found to decrease from the root (~ 80 nm) to the tip (~ several nm) (see Figure 4.4(b)).

▣ Nanowire solution preparation

The first step was to remove the amorphous silicon dioxide and the catalyst residues from the surface of the as-grown SiC NWs. The chemical treatment procedures for SiC NWs are described as follows:

a) SiC NWs are placed in HF treatment with 48 % for 1 min to remove the amorphous silicon dioxide which is formed on SiC NWs during their growth.
b) After that, SiC NWs are placed in *Aqua regia* for 3 min to remove a residue catalyst, such as Ni and Au nanoparticles.
c) SiC NWs are again treated by HF solution with 48 % for 1 min, and clean them by dipping in DI water.
d) Substrates containing NWs were mildly sonicated in isopropyl alcohol (IPA) solution for 1 minute to detach them from the substrate.
e) Finally, the SiC NWs in the solution are ready for use.

▣ Substrate preparation

A highly n-doped silicon substrate with a doping concentration of around 10^{20} cm^{-3} was purchased from Siltronix Inc. Back gated geometry is adopted for the fabrication of SiC NWFETs. Back-side of the Si substrate served as a back gate without metallization. Thanks to the high doping of the substrate (resistivity below 0.1 Ω·cm), there is no need for a metal ohmic contact for the back gate. In a subsequent process, a thermal oxidation process has been performed to fabricate an approximately 280 nm gate oxide (SiO_2).

▣ Definition of align markers and contact pads

After the oxidation process, the following step is to define the align markers and contact pads. This step is necessary since the NWs are too small to determine their coordinates and therefore to make metal contacts on them. These align markers provide a very high accuracy to determine coordinates and they can attenuate the probability of failure caused by alignment mismatch. Contact pads are used to probe with tips for electrical characterization of SiC nanoFET. Alignment markers were patterned by EBL due to their small dimensions (500 nm×500 nm), while contact pads were fabricated onto the substrates using the conventional photolithography.

Figure 4.5 shows the fabrication steps in order to define to contact pads and align markers. First, photoresist polymethyl methacrylate (PMMA) 4% is spin-coated at 4000 revolutions per minute (rpm) for 60 s on SiO_2/Si substrates. Then, spin coated substrate is heated up on a hotplate at 180 °C for 5 min. After that, the align markers design (red part in Figure 4.6) is exposed by the using e-beam writer shown in Figure 4.7(a).

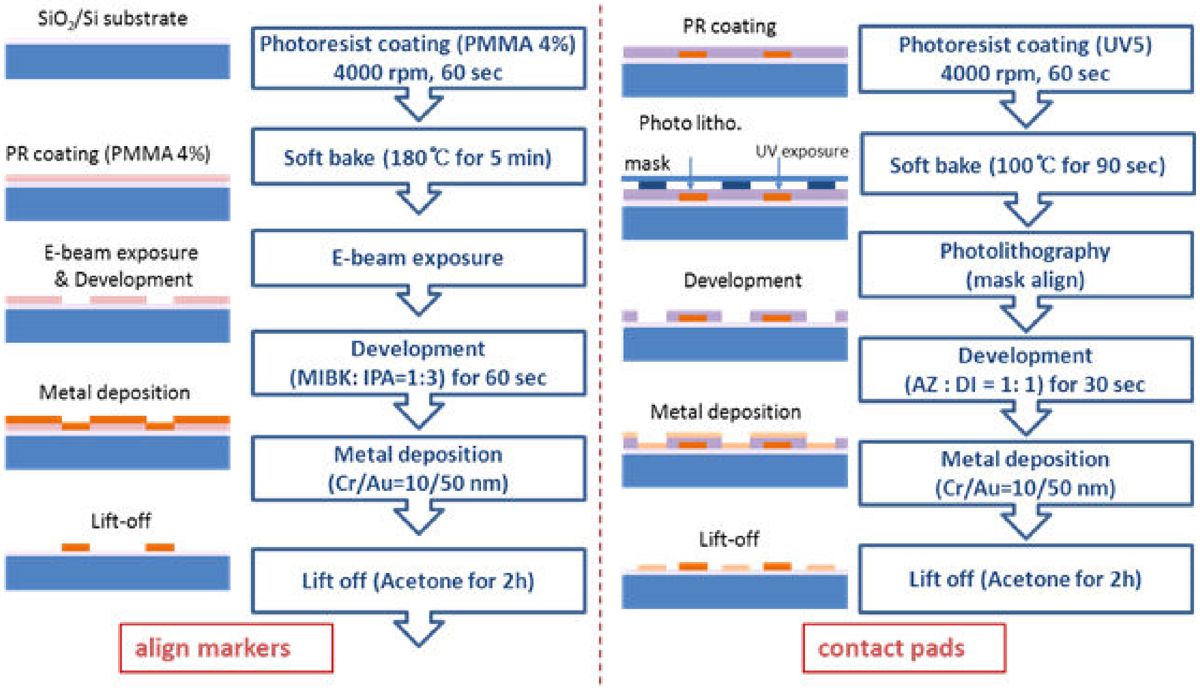


Figure 4.5 Align markers and contact pads fabrication process by using e-beam and photolithography, respectively.

The exposed sample is developed in methyl-isobutyl-ketone (MIBK) diluted in IPA (1:3) for 30 *s* and followed by a rinse in IPA solution and drying by nitrogen gas (N_2) blowing. And then, the metal deposition of the align marker is performed by e-beam evaporation with 10 nm thick Cr as an adhesion layer and 50 nm gold layer.

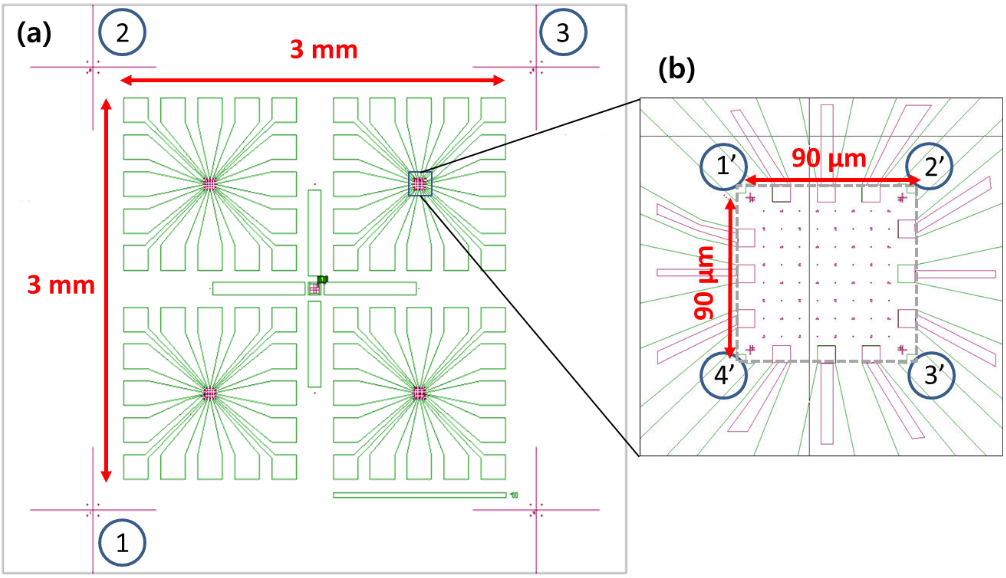


Figure 4.6 (a-b) Design for align markers and contact pads. (red: align markers with e-beam lithography, green: contact pads with photolithography).

Next step is the photolithography process in order to define contact pads. Positive photo resist (UV5 [b]) is spin-coated at 4000 rpm for 60 *s*. For the soft bake, spin coated substrate is heated up to 100 °C for 90 *s*. Then, contact pads area (green part in Figure 4.6(b)) is exposed by using a mask aligner shown in Figure 4.7(b).

After photolithography, chemical developers (AZ [c] developer: DI water= 1:1) are used to remove unhardened resist that was exposed to UV light, while IPA is mainly used for degreasing and dissolving remained developers. And then, the metal deposition for the contact pads is performed by e-beam evaporation with 10 nm thick Cr and 50 nm gold layer. Cr metal layer is good adhesion layer, which guarantee clear pattern after the lift-off process, gold is well known as good conducting material for electrical characterization. Next, the lift-off is done in acetone solution during 2 *h*, and finally, the wafer is cleaned by IPA solution.

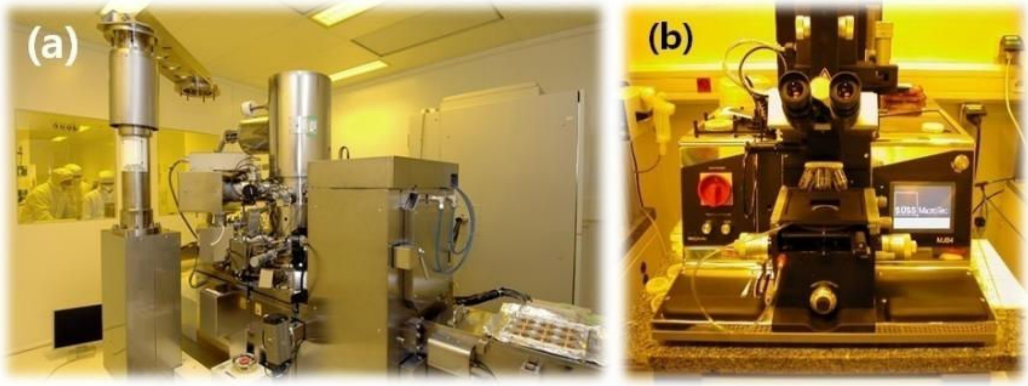


Figure 4.7 Photo image of (a) e-beam writer (JEOL 6300FS) and (b) mask aligner (Karl Süss MJB4 DUV).

▣ Definition of Source/Drain contact regions

The SiC NWs are deposited on the substrate by dropping one or two droplets of the solution with a micropipette from the top. The next step is to place the sample on a hot plate (60 - 90 °C) in order to evaporate the solvent. After that, a drop of the NWs suspension is dried on the wafer. AFM or SEM is used to locate the NWs deposited on the wafer and their position relative to the alignment markers, as shown in Figure 4.8(a).

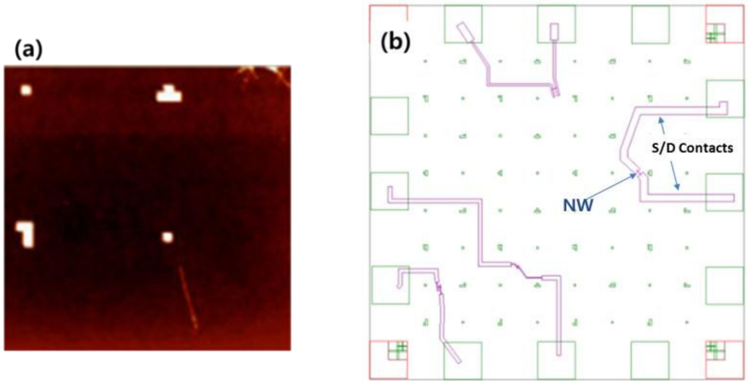


Figure 4.8 (a) AFM image of the deposited SiC NW on the substrate,
(b) Design for e-beam lithography to define the S/D.

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b) UV5: Produce name of positive DUV photoresist from Micro resist technology Inc.

c) AZ: Product name of developer from AZ Electronic Materials.

Based on the measured NW position, the e-beam lithography designs (GDS files) are created to connect the S/D for each NW, as shown in Figure 4.8(b). For the EBL process, PMMA 4% was spin-coated on substrates at 4000 rpm for 60 *s*. Consequently, spin coated substrate is heated up on a hot-plate at 180 °C for 5 min. After that, the design of S/D contacts is exposed by using e-beam lithography system (JEOL 7400S with Raith Quantum).

For performing the electron beam exposure with high accuracy, it is needed to do the conversion of stage (x, y) coordinates into (u, v) sample's coordinates and a subsequent adjustment of write field. First, the (x, y) coordinate should be changed into the (u, v) coordinate based on the three reference structures (three crosses - #1, #2, and #3 in the Figure 4.9). This process calculates the shift, rotation angles and scaling factors between the two coordinates systems. After this correction, the center of big green cross in Figure 4.9 set to (0, 0) in the (u, v) coordinate.

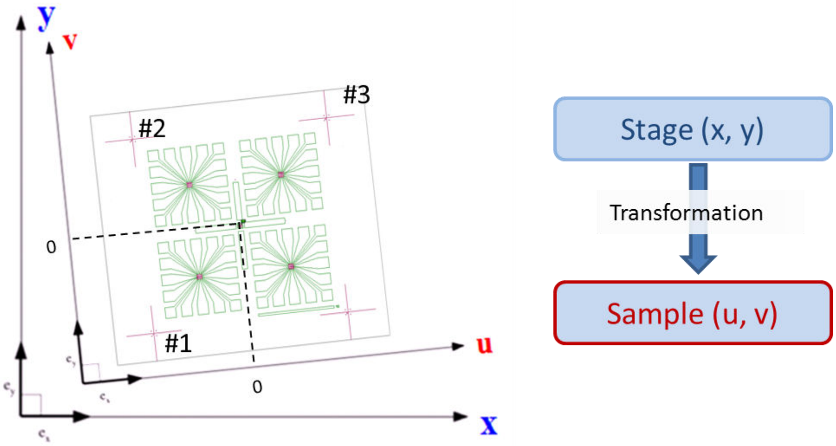


Figure 4.9 Conversion stage coordinate (x, y) into beam deflection coordinate (u, v).

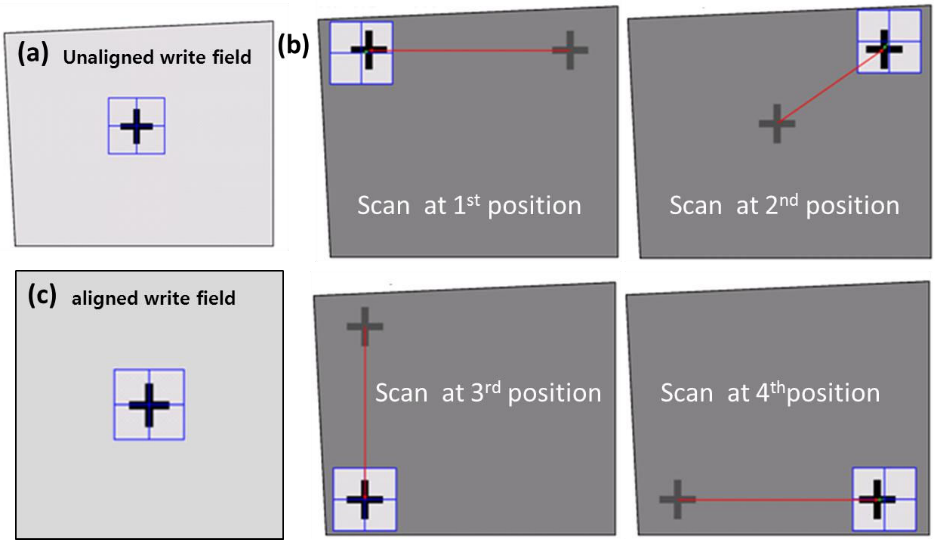
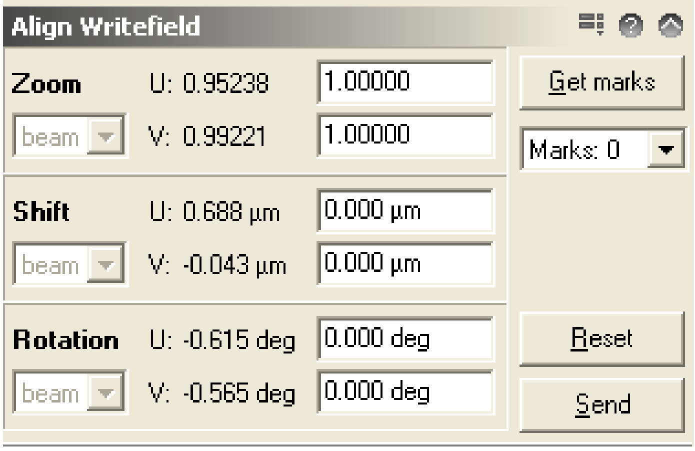


Figure 4.10 (a) Unaligned write field, (b) process of the write field alignment and (c) aligned write field.

Next step is the write-field alignment, which is the adjustment of the electromagnetic/electrostatic deflection system inside the e-beam column to the high precision X-Y-Z stage for a given combination of magnification and write field setting of the microscope [31].

Exposed write field on the sample could be distorted during the EBL (see Figure 4.10(a)), because the sample attached on the stage is not completely flat and the electromagnetic/electrostatic in EBL system is not perfectly aligned. After the write field alignment process (Figure 4.10(b)) based on four crosses in Figure 4.6(b) (#1' - #4'), Raith software calculates scaling, shift and rotation of write-field for the compensation, as shown in Figure 4.11.



Align Writefield

Zoom U: 0.95238 1.00000
beam V: 0.99221 1.00000

Shift U: 0.688 µm 0.000 µm
beam V: -0.043 µm 0.000 µm

Rotation U: -0.615 deg 0.000 deg
beam V: -0.565 deg 0.000 deg

Marks: 0

Figure 4.11 Modified align write field after the adjustment.

Based on the design, the sample is exposed to the e-beam. The acceleration voltage range is between 10 to 30 kV. A value of 20 kV is used. Indeed using high (30 kV) acceleration voltage would result in higher surface charging effect and important surface damage. On the other hand using low (10 kV) acceleration voltage would not warrant enough resolution for the nanopatterns.

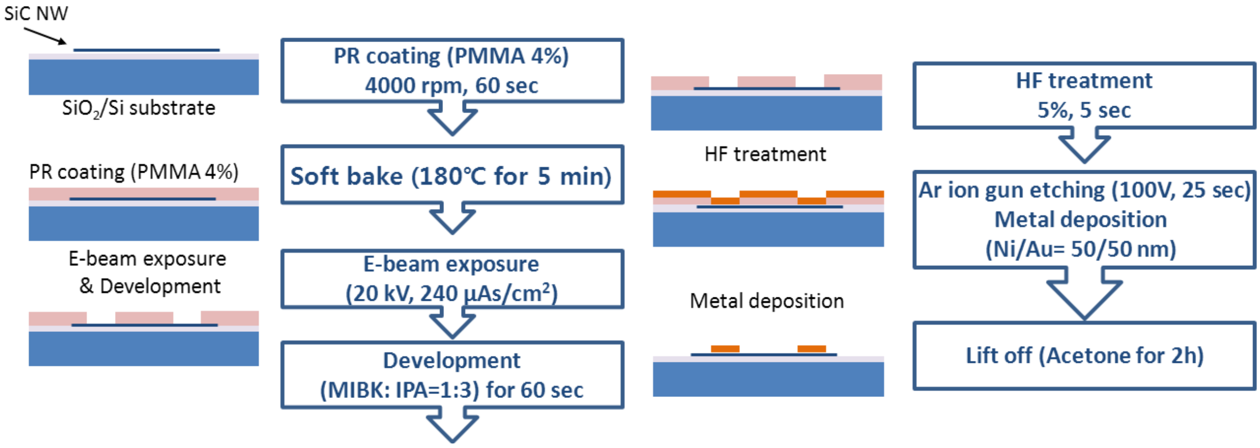


Figure 4.12 Fabrication process for S/D contacts by using e-beam lithography.

After e-beam exposure, the sample is held in air ambient even during the development process. At that time, a very thin silicon (native) oxide layer can be formed on SiC NWs. This thin oxide layer hinders charge injection between metal and SiC and acts as a contact barrier. For this reason, native oxide layer is removed with HF (5%) for 5 *s* and then metal contacts are immediately evaporated (Plassys MEB550S e-beam evaporator) with a thickness of Ni/Au=50/50 nm after development process. Finally, the lift-off is done in acetone solution during 2 *hr*, and cleaned by IPA solution.

Contact annealing

Even after lift-off process, the organics species (e.g. PMMA) might be remained on the substrate. Therefore, the sample is exposed to oxygen plasma at 350 W during 180 *s* for the removal of residue particles. After this cleaning step, the sample is annealed in the vacuum in the range of 500 and 700 °C to improve the electrical contact between the NW and the metal electrodes. The contact resistance is strongly depending on the annealing temperature, so it should be optimized according to metal species.

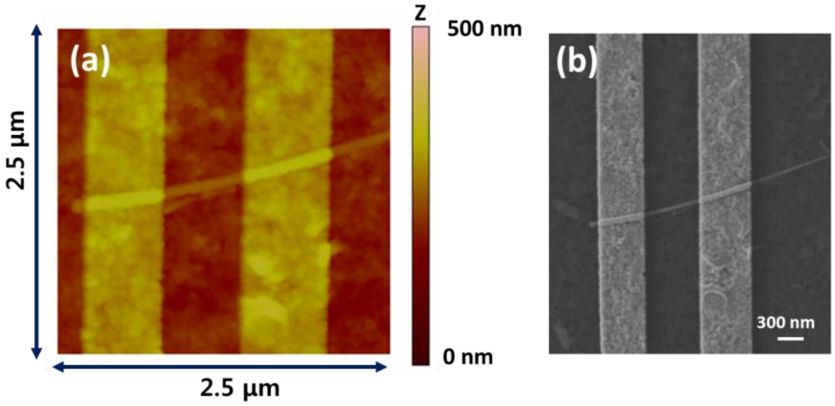


Figure 4.13 (a) AFM and (b) SEM image of SiC NWFET after finishing the whole process.

Generally, the Ni metal is widely used for ohmic contact formation to n-type SiC bulk material due to the resulting low contact resistance and the reproducibility after high temperature annealing. The origin of the low contact resistance in Ni-based ohmic contacts to SiC NWs after high-temperature annealing is assumed to originate from a new polycrystalline nickel silicide phase (Ni_2Si, $NiSi_2$, NiSi, etc.) at the interface between the Ni and 3C-SiC NWs [32], as seen in the bulk SiC materials. Figure 4.13 show the AFM (scanned image size is 1.5 µm×1.5 µm) and SEM image of SiC NWFET after finishing the whole process. The whole fabrication process of NWFET is summarized in Figure 4.14.

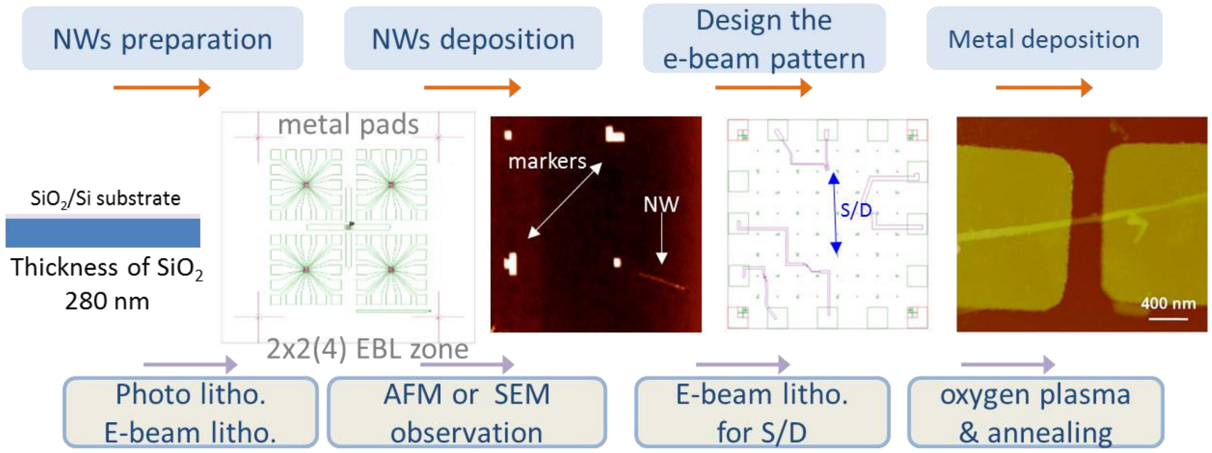


Figure 4.14 Whole fabrication process flow chart of SiC NWFET (type A).

4.2.2 Fabrication steps of SiC NPFETs

The fabrication process of SiC NPFETs is almost similar to that of SiC NWFET except the preparation of NP solution and contact pads. These two steps will be mainly discussed in this section.

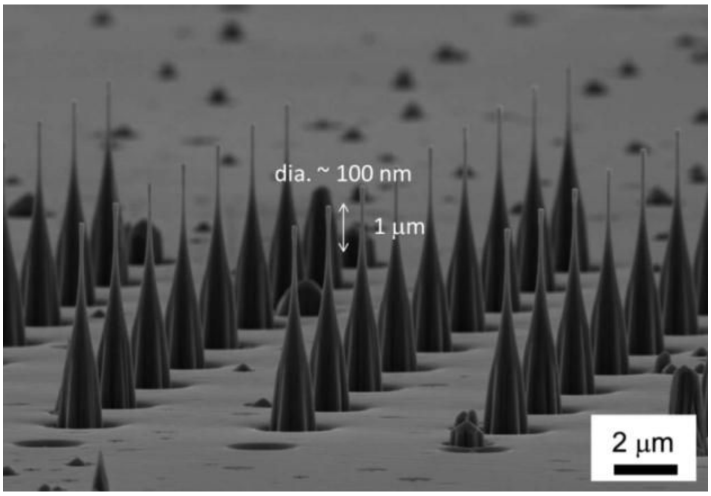


Figure 4.15 SEM image of etched 4H-SiC NP arrays.

▣ Nanopillar solution preparation

The first step is to remove the etching byproducts ($Si_xF_yO_z$) on the surface of SiC NPs and Ni mask, as described in the section 3.3.1 and 3.3.2. The chemical treatment procedure for etched SiC NPs is described as follows:

a) SiC NPs are placed in HF treatment with 48% for 1 min to remove the etching byproducts.
b) After that, SiC NPs are placed in HCl with 25 % for 1 *hr* to remove the Ni mask.
c) SiC NWs are again treated by HF solution with 48% for 1 min, and clean them by dipping in DI water.

▣ Cutting of SiC nanopillars

The second step is to cut the small diameter (below 100 nm) part of SiC NPs, which is a process step with inherent difficulties. We tried to cut the etched SiC NPs (for instance, the one shown in Figure 4.16(a)) with three different ways, as shown in Figure 4.16(b-g).

First, SiC NP arrays are loaded with upright position in IPA solution (Figure 4.16(e)) and then they are sonicated by means of sonicator for 30 min. In spite of long time sonication (30 min), only few NP is broken during the sonication (see the rectangular of Figure 4.16(b)).

Second, a small Si substrate is loaded on the top of SiC nanopillars during the sonication to impose the force in the vertical direction, as shown in Figure 4.16(f). It is clearly shown that the small diameter part of SiC NPs is broken after the sonication (2 min, Figure 4.16(c)). However after depositing the IPA solution with broken SiC NP on the metal pads, it was revealed that SiC NP is broken into small nanoparticles instead of nanorods (see Figure 4.16(c')).

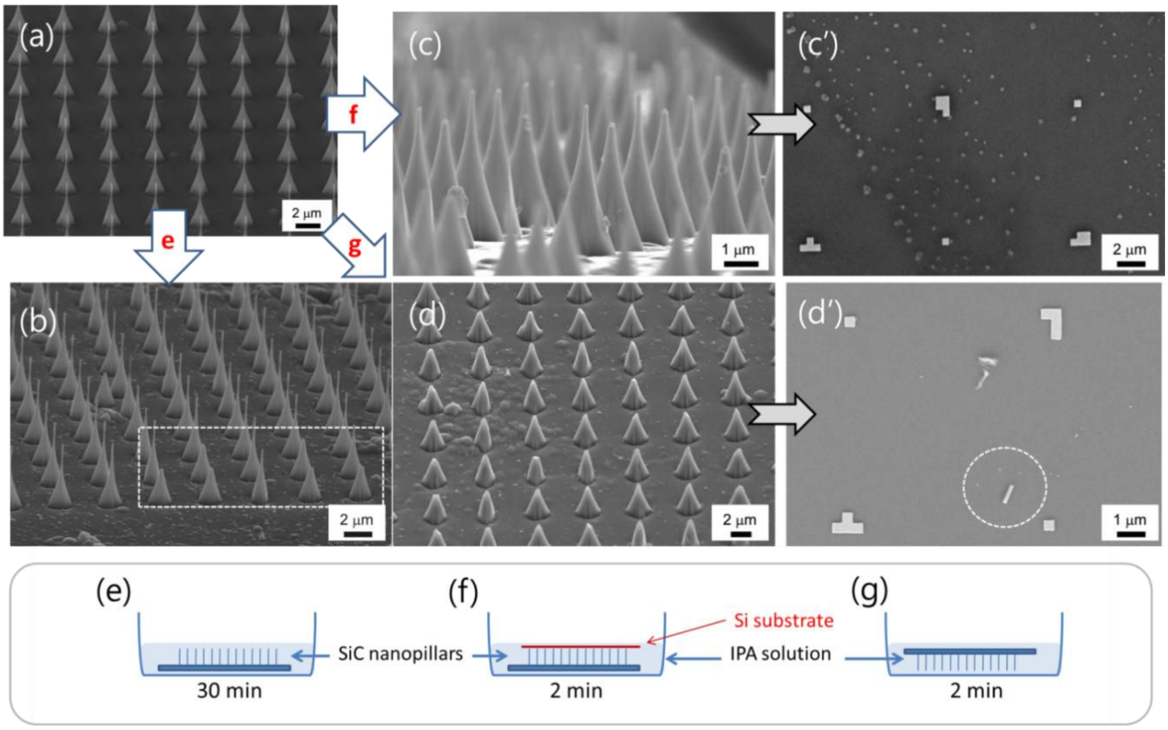


Figure 4.16 SEM images: (a) of–3C-SiC NP arrays prior to sonication; (b, c, d) the NP arrays after the sonication with three different methods; (c', d') after cut-NPs dispersion on the Si substrate with predefined pads. In (e-f) the schematic of each NP arrays sonication process is shown: (e) with loading in upright position corresponding to the above (b) image; (f) with loading Si substrate on the SiC NPs corresponding to the above (c) and (c') images, (g) with loading in downright position corresponding to the above (d) and (d') images.

Third, SiC NP arrays are loaded downright position during the sonication, as shown in (Figure 4.16(g)). Figure 4.16(d-d') shows that this sonication method can successfully cut small diameter part of SiC NPs in shape of nanorods with average length around 900 nm and diameter around 100 nm. The dimension of broken SiC NPs is long enough to fabricate the FET devices. In addition, this cutting was successful all over the surface of the sample. Note, that the whole process results in production of a substantially lower quantity of NPs in comparison to that of bottom-up fabricated NWs (device type A).

▣ Definition of align markers and contact pads

The low quantity of NPs in the solution resulted in a very low density of dispersed NPs on the prepatterned Si substrate. Consequently, NPs couldn't be found in the write field of EBL (Figure 4.6(b) and Figure 4.8(b)) after the deposition of solution containing the NPs. Therefore it was necessary to change the prepatterned array on Si substrates for that used in case of the device fabrication of SiC NWFET where, metal pads are fabricated by optical lithography (green in Figure 4.17(a)). Note that only four align maskers for EBL zone (size: 80×80 µm) are fabricated by e-beam writer (red in Figure 4.17(a)) in this case.

Since the probability to have a NP in the EBL zones is proportional to the ratio of the surface of the EBL zones over the whole surface, we increased the number of EBL zone from four (2×2) to twenty-five (5×5) as shown in Figure 4.17(b). On the other hand, the gate oxide (SiO_2) thickness is further reduced down to 80 nm to increase the gate controllability (see Appendix A2).

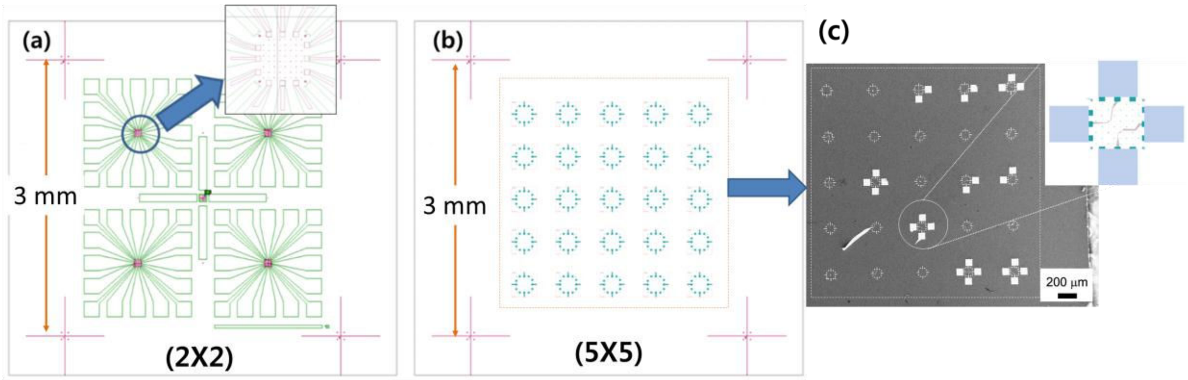


Figure 4.17 (a) Design of metal pads (green) and align markers (red) for the device fabrication of SiC NWFETs (2×2 windows), (b) Design of align markers for the device fabrication of SiC NPFETs (5×5 windows), (c) SEM images and design and of fabricated SiC NPFETs.

The metal pads for the contact with probe tips are fabricated by the EBL instead of optical lithography, as shown in Figure 4.17(c). The size of metal pad is 80×80 μm. Different conditions are used for the e-beam exposure of S/D connections and metal pads, as listed in Table 4.2. Small e-beam size (3.2 nm) is suitable for the pattering of S/D electrode with high resolution, while large e-beam size (i.e. 32 nm) is useful to expose large area in short time.

Table 4.2 Parameters for e-beam lithography of S/D and metal pads

(a) 1st e-beam litho. for S/D connection		(b) 2nd e-beam litho. for pads	
Probe current	50 pA	Probe current	200 pA
Area step size	3.2 nm	Area step size	32 nm
Area dose	240 μAs/cm^2	Area dose	200 μAs/cm^2

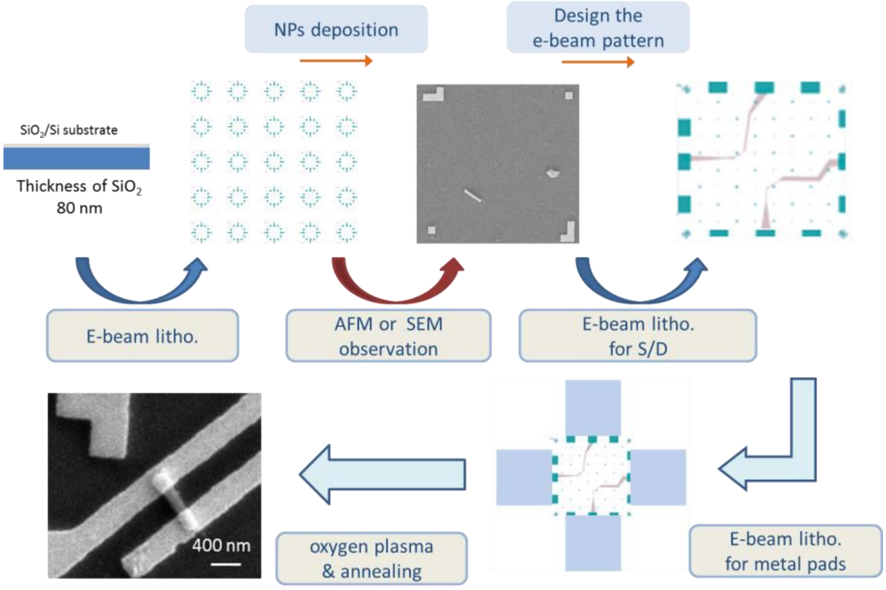


Figure 4.18 Whole fabrication process flow chart of SiC NPFETs (type B).

Other remaining steps for the device fabrication of SiC NPFETs (such as metal deposition, oxygen plasma and annealing) are same to the fabrication process of SiC NWFETs, as shown in Figure 4.18.

4.3 Electrical characterization of SiC nanoFETs

In this section, I'll introduce the electrical measurement results of two types SiC nanoFET (SiC NWFET and SiC NPFET). First, I will show our initial results on SiC NWFET fabrication and electrical characterization. And then, I'll introduce the improvement in contact resistance properties on SiC NWFET by optimizing the annealing conditions. These results showed the necessity for ohmic contact improvement and that Ni based silicidation is a key process to guarantee the stability and repeatability of ohmic contact by tailoring the metal-semiconductor interface. But, there is no a systematic study on Ni based silicidation on SiC NWs according to the annealing temperature. Finally, the electrical characterization of SiC NPFETs will be presented.

4.3.1 Electrical properties of SiC NWFET

Figure 4.19 shows AFM images of fabricated SiC NWFETs using a cylinder shape of SiC NWs [29]. The contact annealing of fabricated SiC NWFET was carried out at 700 °C for 30 *s* with ambient N_2 in a rapid thermal annealer (Jetfirst 100). Electrical properties of NPFET were measured at room temperature and in ambient air with HP 4155.

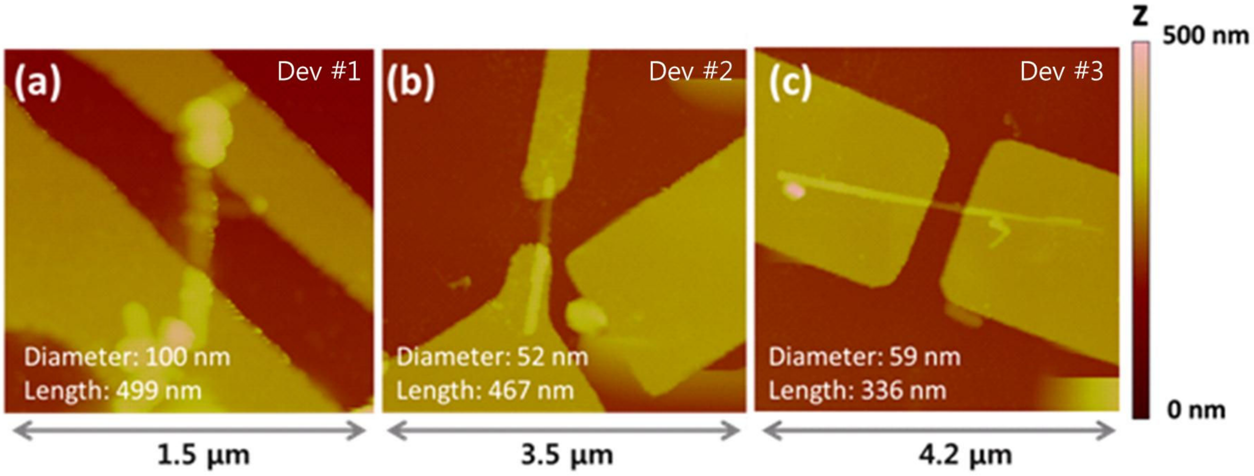


Figure 4.19 (a-c) AFM images of fabricated SiC NWFETs.

A typical I_{DS}–V_{DS} characteristic of SiC NWFET is shown in Figure 4.20(a-c). The gate voltages were applied from - 40 to 40 V and the drain voltages are from - 1 to 1 V at room temperature. The measured I_{DS}–V_{DS} curves of all devices show non-ohmic behavior. The current of dev #1 in Figure 4.20(a) increases with the increase of the gate voltage V_G, which attributes to n-type properties of the SiC NWs channel. But, the current of dev #2 and dev #3 is constant with the increase of the gate voltage (V_G). The estimated transconductance (g_m) from transfer characteristic curve (I_D-V_{GS}) in Figure 4.20(d) is 0.05 nS for dev #1 and below 0.01 nS for dev #2 and #3, as listed Table 4.3. The estimated field-effect carrier mobility for all SiC NWFETs is estimated to below 0.001 $cm^2 \cdot V^{-1}s^{-1}$, which is quite lower compared to the best values (15.9 $cm^2 \cdot V^{-1}s^{-1}$) reported in a previous study [33]. Weak gate effect and low mobility of SiC NWs could have been first explained by a high density of donor states that may result from an unintentional doping during the growth [28]. Unoptimized devices process could be another possible reason for these low motilities reported.

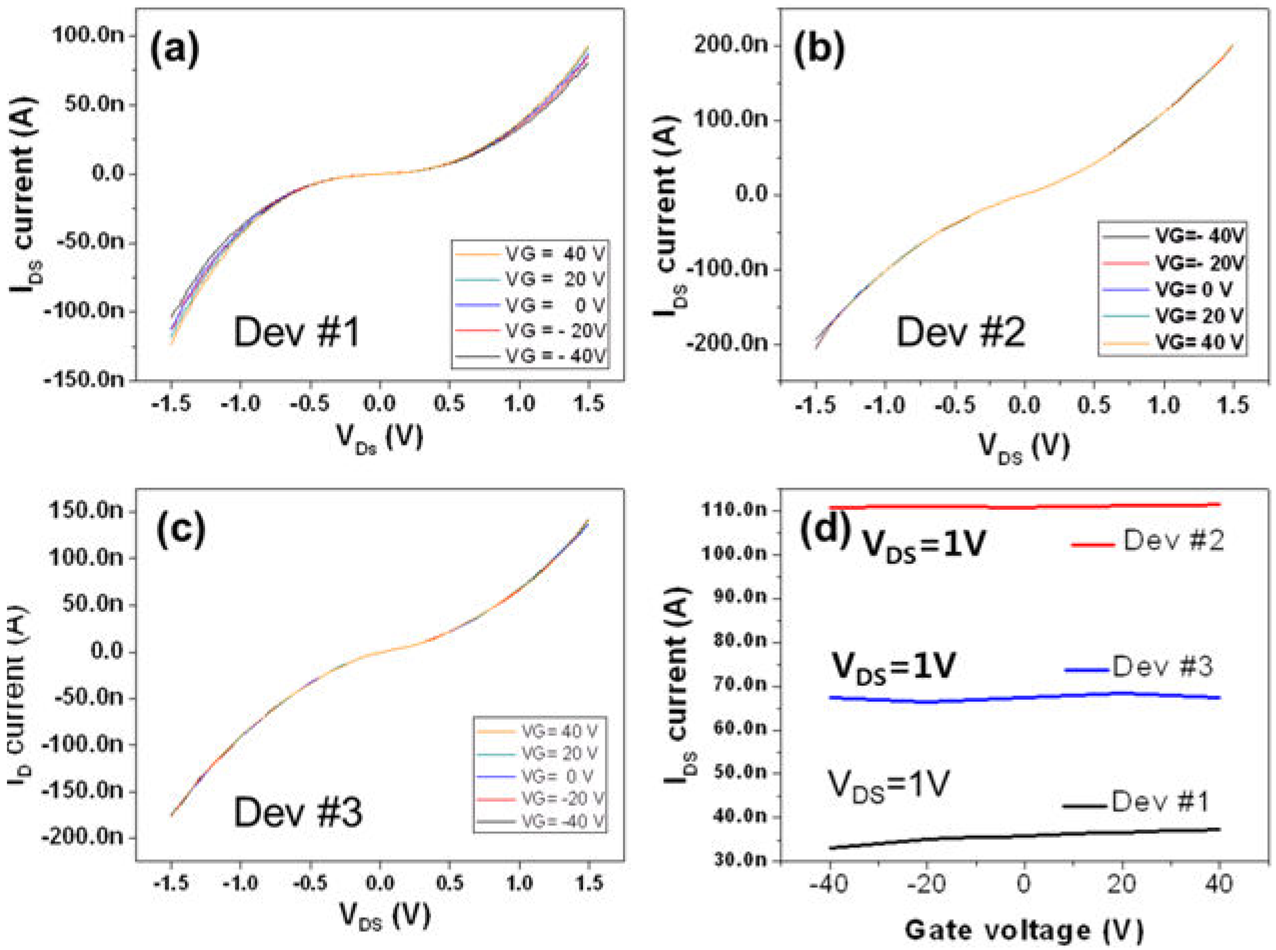


Figure 4.20 (a-c) Output (I_{DS}-V_{DS}) and (d) transfer characteristic curve (I_D-V_{GS}) of SiC NWFETs.

Table 4.3 Summary of 3C-SiC NWFET performance.

3C-SiC <111> NWFET	Dev #1	Dev #2	Dev #3
Diameter	100 nm	52 nm	59 nm
Length	449 nm	467 nm	336 nm
Oxide thickness	280 nm	280 nm	280 nm
C_{ox} (F)	0.04 fF	0.03 fF	0.02 fF
g_m (S)	0.05 nS at V_{DS}= 1V	below 0.01nS V_{DS}= 1V	below 0.01nS V_{DS}= 1V
μ ($cm^2 \cdot V^{-1} s^{-1}$)	below 0.002	below 0.001	below 0.001

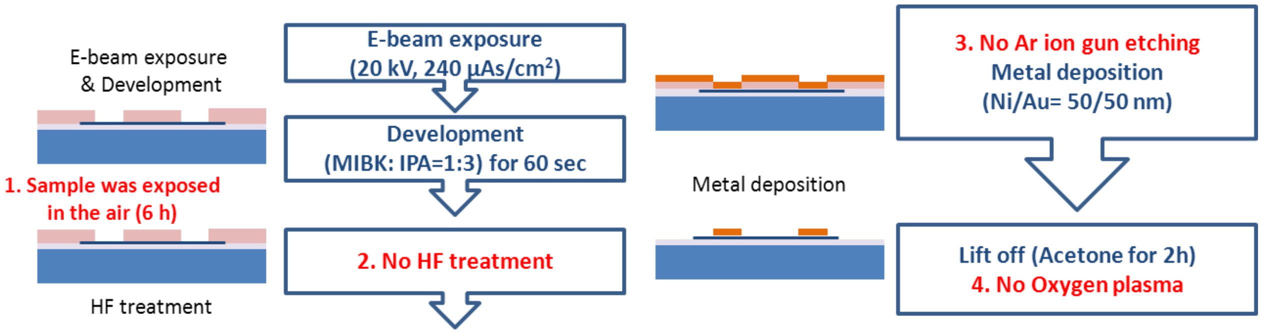


Figure 4.21 Fabrication process flow chart of our first SiC NWFET.

In the case of our first device fabrications, the opened S/D area of SiC NW after EBL and development is exposed at the air around 6 *hr*. Then, metal deposition (Ni/Au= 50/50 nm) is done without any treatment (such as HF treatment and Ar ion gun etching), as illustrated in Figure 4.21.

The native oxide formed on SiC NWs at the S/D region could be a possible reason for poor device performances. Moreover, the oxygen plasma of SiC NWFET has not been done after the lift-off process. The remaining organic material (such as photoresist) on the surfaces may hinder electrical transport in the channel of SiC NWFET.

So, we optimize our device fabrication process as depicted in Figure 4.12. HF treatment (5%, 5 *s*) right after the development and Ar ion gun etching (100V, 25 *s*) prior to metal deposition have been done to minimize the native oxide formation on SiC nanostructures. And then oxygen plasma (350 W during 180 *s*) also has been done to remove the remaining organic materials.

4.3.2 Improvement of SiC nanowire ohmic contact by Ni silicidation

It is well known that Ni-based ohmic contacts on SiC are improved with annealing optimization to form nickel-silicide phases [32]. Therefore, our purpose was to perform an annealing optimization study to form these low contact resistance phases. The annealing step was carried out in the range from 500 to 750 °C for 30 *s* with ambient N_2 in a rapid thermal annealer (Jetfirst 100). The temperature ramp rate was set to reach a desired temperature within 30 *s*. Then, electrical properties of devices were measured at room temperature and in ambient air with a Keithley 4200 semiconductor characterization system.

- ▣ Contact property according to annealing temperature

One SiC NWFET device with a four-point probe configuration (Figure 4.22(a)) has been performed to study the electrical resistivity and contact properties of a SiC NWFET. The distance between each electrode is 500 nm, the width of metal electrodes is 300 nm.

The total NWFET resistance (R_{tot}), which is defined as the zero-bias slope of the inverse of the two probe $I_{2\text{-}3}$-$V_{2\text{-}3}$ curve, consists of the channel resistance (R_{NW}) and two contact resistance (R_C) at S/D, as depicted in Figure 4.22(b). The channel resistance (R_{NW}) is evaluated using the four-probe measurement by sweeping a current $I_{1\text{-}4}$ across the outer leads and measuring the voltage $V_{2\text{-}3}$ across the inner leads. The contact resistance (R_C) is calculated by the following equation (Eq 4.1).

$$R_C = (R_{tot} - R_{NW}) / 2 \qquad \text{Eq 4.1}$$

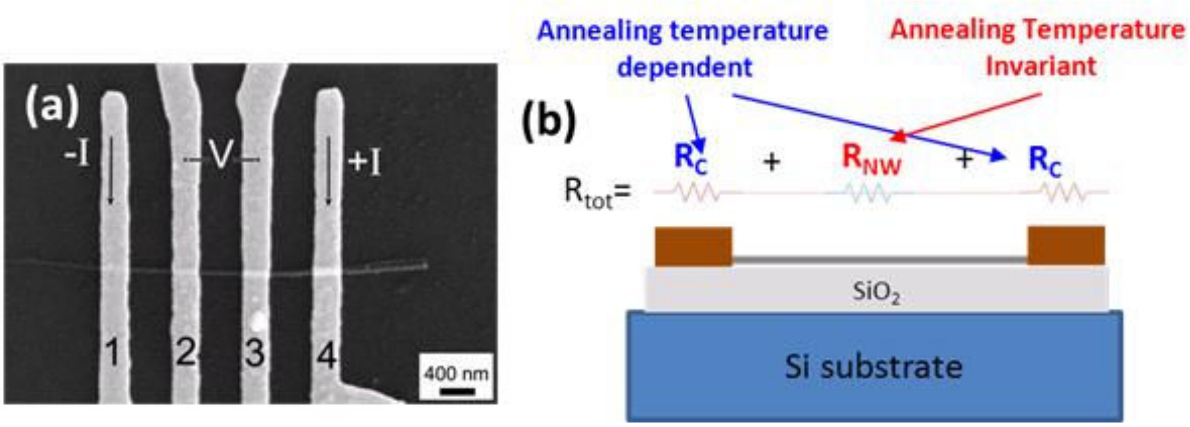


Figure 4.22 (a) SEM image of four-probe measurement,
(b) the contact and the channel resistance of a SiC NWFET.

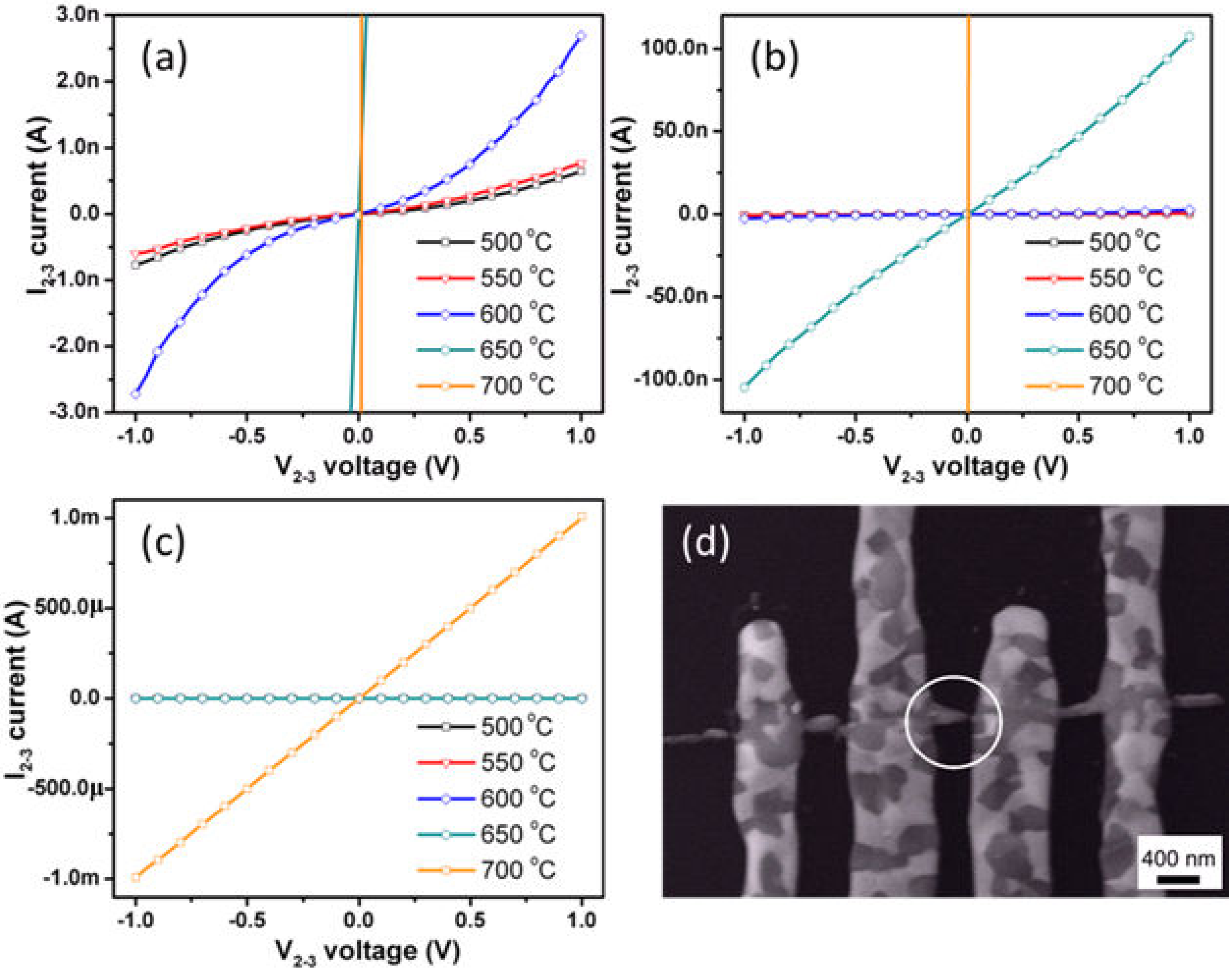


Figure 4.23 (a-c) The $I_{2\text{-}3}$-$V_{2\text{-}3}$ curves measured at the inner electrodes (2-3) as a function of the annealing temperature with different current ranges,(d) SEM images of a broken SiC NW after the annealing at 750 °C.

The current ($I_{2\text{-}3}$) increases with increasing annealing temperature (Figure 4.23(a-c)), which means the decrease of the total NW resistance (R_{tot}). The $I_{2\text{-}3}$-$V_{2\text{-}3}$ curves for annealing below 650 °C show a low current level and non-ohmic behavior (Figure 4.23(a)), but SiC NWFET for annealing at 650 °C presents an ohmic contact with the linear behavior of $I_{2\text{-}3}$-$V_{2\text{-}3}$ curve (Figure 4.23(b)). The current level of SiC NWFET after the annealing at 650 °C increases up to 100 nA.

When measuring the $I_{2\text{-}3}$-$V_{2\text{-}3}$ using two-probe measurement, the voltage is measured not only across the channel resistance, but also includes the resistance of contacts (see Appendix A3 – Figure A.5). Therefore, the total NW FET resistance (R_{tot}) can be extracted from the $I_{2\text{-}3}$-$V_{2\text{-}3}$ curve, which is defined as the zero-bias slope of the inverse of the I-V dependence. R_{tot} after the annealing at 650 °C is 11.56 MΩ from Figure 4.23(b).

When measuring the $I_{1\text{-}4}$-$V_{2\text{-}3}$ using four-probe measurement, a current ($I_{1\text{-}4}$) flows across the outer leads and voltage $V_{2\text{-}3}$ is measured across the inner leads (see Appendix A3 – Figure A.5). The detail configuration of four-point probe method is described in Appendix A3 (Figure A.6). The current (I_{VM}) flows in the inner probes connected to voltmeter is negligible due to high input impedance ($>10^{16}$ Ω) of voltmeter, only the voltage drop across the NW. Therefore, the slope of $I_{1\text{-}4}$-$V_{2\text{-}3}$ curve indicates only the channel resistance (R_{NW}). The channel resistance (R_{NW}) evaluated by the four-probe measurement is 10.80 MΩ at 650 °C, as shown in Figure 4.24(a). Therefore, contact resistance (R_C) of a device at 650 °C is calculated by the following equation (Eq 4.1) is 378 kΩ.

The resistivity (ρ) of SiC NW can be calculated by the following equation (Eq 4.2),

$$\rho \equiv \mathrm{R}\frac{\mathrm{S}}{\mathrm{L}} = \frac{\mathrm{V}_{\mathrm{DS}}\pi r^2}{I_{\mathrm{DS}}\,L}, \qquad \text{Eq 4.2}$$

where R is the NP resistance, S its section, L its channel length of the NP and r is the NW radius. The resistivity have been estimated to be 6.1 Ω·cm.

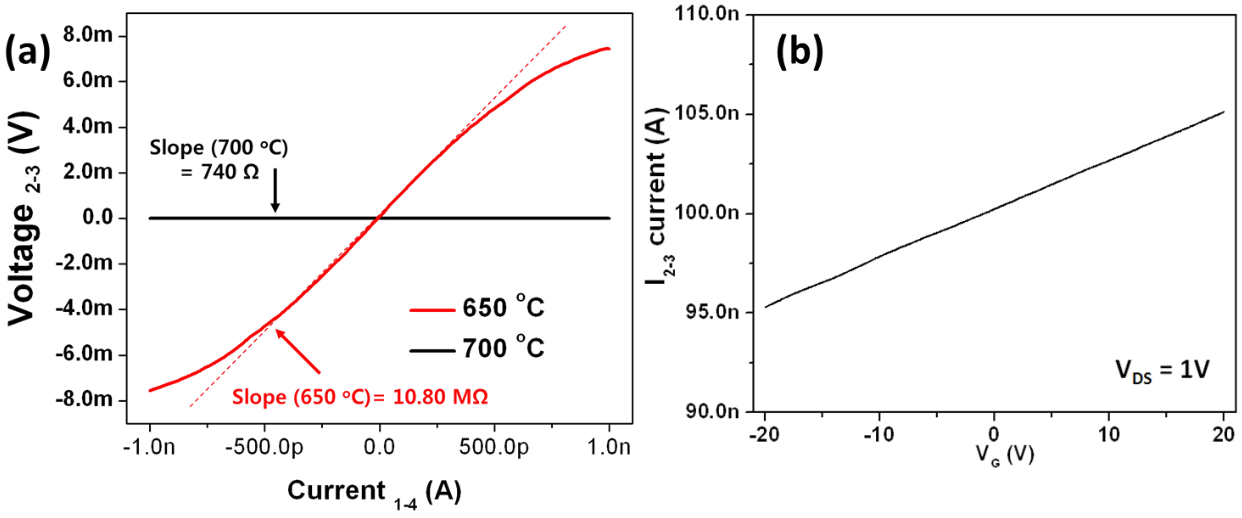


Figure 4.24 (a) The $V_{2\text{-}3}$ - $I_{1\text{-}4}$ curve after the annealing at 650 °C and 700 °C, (b) transfer ($I_{2\text{-}3}$-V_G) characteristic curve of SiC NWFETs.

The other important parameter in the study of ohmic contact is specific contact resistance (ρ_c), often referred to as the contact resistivity and can be calculated by

$$\rho_c = \mathrm{R}_c \cdot 2\pi \mathrm{r} \cdot \mathrm{L}_T, \qquad \text{Eq 4.3}$$

where r is the radius of the NW and L_T is the transfer length of the contact. It represents the length across the contact over which injection occurs. In the calculation of ρ_c, we assumed that current transport occurs uniformly in the contact length (L_T = the width of metal electrodes (300 nm)), and ~ 75% of the circumference of the SiC NWs was in contact with Ni/Au metal layer. The estimated ρ_c from Eq 4.3 is around 1.6 × 10^{-4} $\Omega\cdot cm^2$.

The SiC NWFET after the annealing at 700 °C shows the current level up to 1 mA in Figure 4.23(c). High current of SiC NWFET is originated from the fully converted Ni silicided SiC NW by the Ni intrusion, it will be discussed in detail later. The estimated R_{tot} and R_{NW} of SiC NWFET after annealing at 700 °C are around 1 kΩ and 740 Ω from Figure 4.23(c) and Figure 4.24(a), respectively. Note that, the current of SiC NWFET after annealing at 750 °C can't be measured, because SiC NW is broken due to the Ni intrusion, as shown in Figure 4.23(d).

Figure 4.24(b) shows the $I_{2\text{-}3}$–V_G curve with V_{DS}= 1V after the annealing at 650 °C. The transconductance (g_m) of SiC NWFET is 0.24 nS while the estimated gate oxide capacitance (C_{ox}) calculated from (Eq 1.2) is ~ 0.05 fF. The value of experimental electron mobility calculated from (Eq 1.3) is below 0.1 $cm^2\cdot V^{-1}s^{-1}$. Switching OFF was not achievable even for high negative gate voltages (- 20V) due to the high electron concentration along the NWs.

▣ Two-terminal SiC NWFET after annealing at 700 °C

The above study showed that the four-probe device annealed at 700 ℃ had high current level (1 mA at $V_{2\text{-}3}$= 1 V) and low channel resistance (740 Ω). A series of two-terminal devices directly annealed at 700 ℃ were fabricated for further investigation of their electrical behavior.

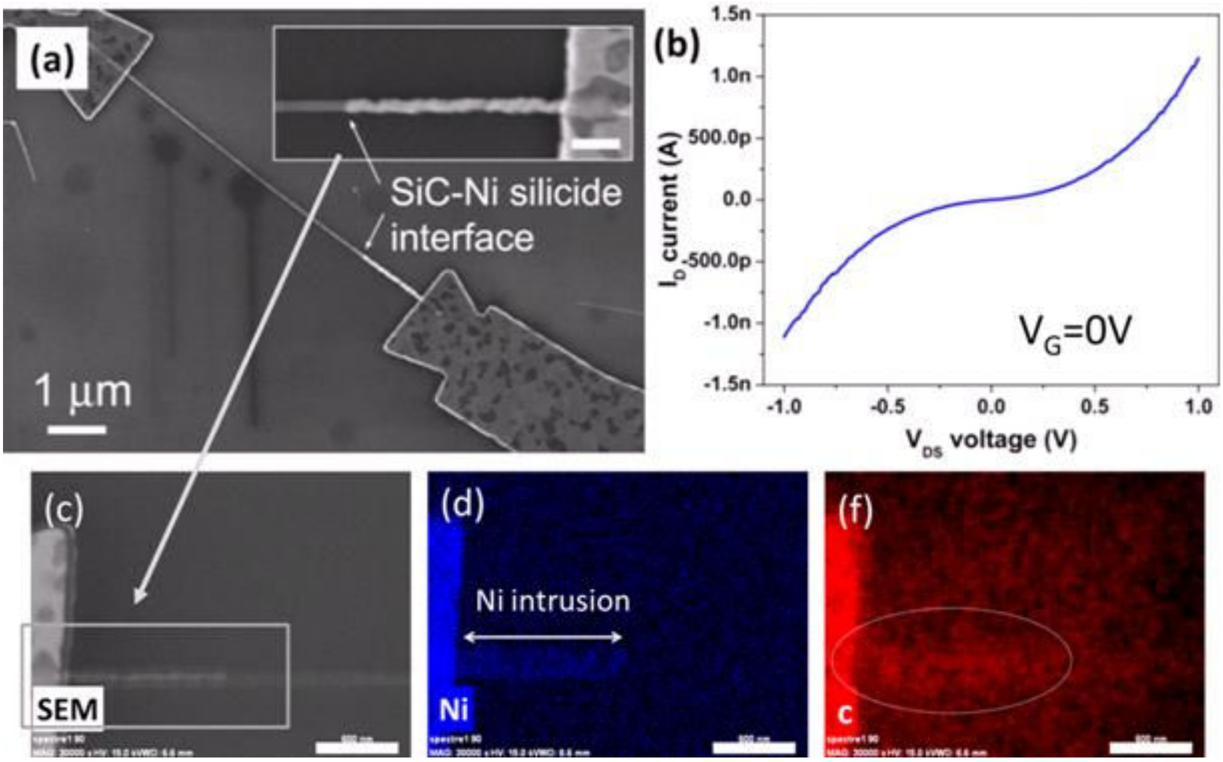


Figure 4.25 (a) SiC-Ni silicide heterostructures by silicidation after annealing at 700 °C during 30 s (inset: a magnified image of Ni silicide intrusion part, the scale bar is 300 nm). The length of Ni-silicide intrusion is around 1.6 µm. (b) I-V curve of SiC-Ni silicide heterostructures FET after the annealing at 700 °C, (c) SEM and (d) Ni and (f) carbon EDX mapping images of SiC-Ni silicide heterostructures (the scale bar is 600 nm).

Figure 4.25(a) shows SEM images of a Ni silicided SiC NWFET after annealing at 700 °C during 30 s. A clear contrast difference in Figure 4.25(a) inset is observed between the unreacted SiC NW (dark sections) and the formed metallic Ni silicided SiC NW (bright sections). Figure 4.25(c-f) shows the SEM and EDX mapping (Ni and carbon) images of the SiC-Ni silicide heterostructures. Ni EDX mapping image confirms a Ni silicide intrusion into the channel. The Ni silicide intrusion emerging from the metal electrode partially converts the SiC into Ni silicide phases by solid state reaction. The Ni silicide diffusion length in Figure 4.25(a) inset after annealing at 700 °C during 30 s is around 1.6 µm. A possible reason for the intrusion or not of Ni intrusion seems to be the existence or not of a surface oxide layer. Indeed a sample annealed at 700 ℃ without a previous HF clean didn't show any Ni silicide intrusion. However, further study is needed to clarify what factor would favor the Ni silicide intrusion. The existence of an insulating oxide layer on the surface of the SiC NW probably leads to low current level and non-ohmic behavior (see Figure 4.25(b)) and negligible gating effect.

In the optimum case Ni silicides begin to intrude from both contacts [2]. Consequently, the SiC NWFET channel is transformed into Ni silicide-SiC-Ni silicide heterostructures, as shown in Figure 4.26(a). The Ni silicide diffusion length measured from a magnified SEM images (Figure 4.26(b) and (c)) are 1.6 µm and 2.0 µm, respectively. However, the electrical properties of Ni silicide-SiC-Ni silicide heterostructures couldn't have been measured as no current was passing through. It might be attributed from the non-conformal interface between SiC NW and contacts (see Figure 4.26(d)). In this particular case, the SiC NW detached from the contacts due to the volume expansion induced by the Ni silicide intrusion. However, in the case of other NWs (as shown in Figure 4.25(a)) the contacts between SiC NW and metal electrode were still remained after the Ni silicide intrusion.

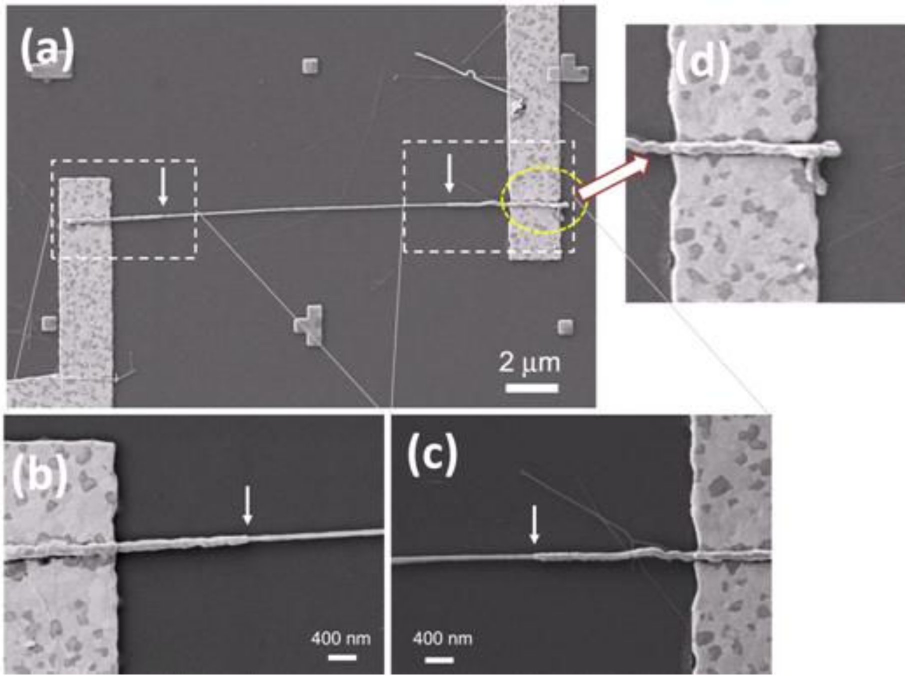


Figure 4.26 (a) Ni silicide-SiC-Ni silicide heterostructures by silicidation after annealing at 700 °C during 30 s, (b-c) a magnified images of Ni silicide intrusion part at the both contact. The length of Ni-silicide intrusion is 1.6 µm (left) and 2.0 µm (right), (d) a magnified images of the interface between Ni silicide SiC NW and Ni electrode.

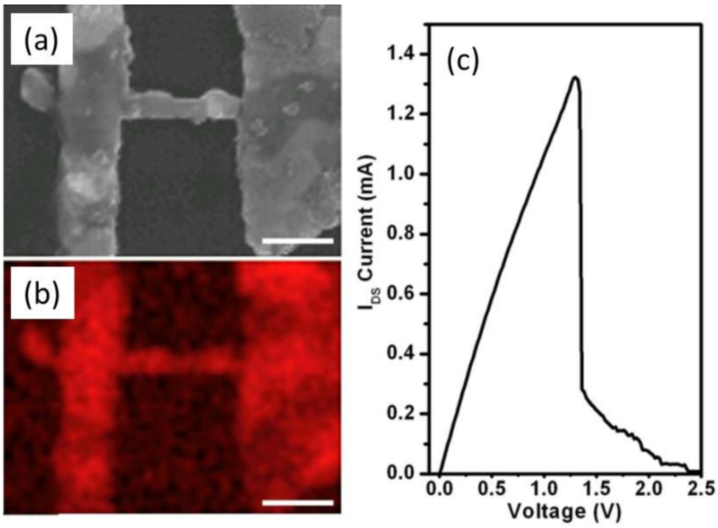


Figure 4.27 SEM images of a silicided SiC nanoFET after annealing at 700 °C during 30 s, (a) SEM and (b) the corresponding Ni EDX mapping image of completely transformed Ni silicided SiC NW. (the scale bars in (b, c) are 400 nm), (c) the I-V curve of fully Ni silicided SiC NW.

If the channel length of SiC NWFET is shorter than Ni silicide intrusion length, SiC NW is completely converted into Ni silicided SiC NW, as shown in Figure 4.27. EDX mapping in Figure 4.27(b) have indeed confirmed the presence of Ni in the channel. The formation of metallic Ni silicided SiC NW during the annealing is further confirmed by two-probe electrical transport study, as shown in Figure 4.27(c). The electrical property of high current, low resistance and perfect ohmic contact behavior before the breakdown point of device at 1.3 V obviously show the metallic behavior of Ni silicided SiC NWs. The fully Ni silicidized SiC NW (expanded diameter ~ 95 nm due to Ni silicide intrusion) can carry the current up to 1.32 mA, which gives a current density exceeding 1.5×10^7 A cm^{-2}.

Based on experimental results, high current level (1 mA) of SiC NWFET after the annealing (700 °C) in Figure 4.23 with the four-probe configuration is originated from the metallic property of fully Ni silicided SiC NW. The annealing temperature to obtain a low ohmic contact for SiC NWFET should be lower than the Ni silicide intrusion temperature (700 °C), because the channel of SiC NW is consumed by Ni silicidation. In this study, the optimum annealing temperature for SiC NWFET has been found to be 650 °C, which shows a low contact resistance (378 kΩ) with the linear behavior of I_{2-3}-V_{2-3} curve. The linear behavior of I-V curves at 650 °C demonstrates an ohmic contact between the single SiC NW and the Ni/Au electrodes.

▣ Ni silicide intrusion into SiC NWs

Ni silicide intrusion into the NW's channel was widely observed in other group IV semiconductors NWs, such as Ge [34], Si [2, 35-37], Ge-Si core-shell NWs [38]. The Ni silicide intrusion behavior in Si NWs had been systematically studied by in situ TEM [36]. Direct evidence from in situ TEM videos shows that Ni silicides are intruding along the Si NWs with the atomically flat epitaxial interfaces.

Ni silicide intrusion into SiC NWs is for the first time reported in the present study. Ni silicide intrusion temperature into SiC NW (700 °C) is significantly higher than that of other group IV semiconductors NWs (Si: 400 - 550 °C and Ge: 400 °C), as shown in Figure 4.28. It is believed that Ni diffusion rate into SiC is low due to the high binding energy between carbon and silicon and the dense packed atomic structure of SiC [39]. Ni silicide intrusion into the SiC NW channel had not been observed at high temperature annealing (700 °C) in ref. [28], even though they obtained low ohmic contact resistance (8.2 ± 0.2 kΩ). It was believed that amorphous SiO_2 formed on SiC NWs acts as a barrier for the Ni silicide intrusion. The removal processes of amorphous SiO_2 surrounding SiC NWs (the combination of HF treatment Ar ion gun etching) before metal deposition are indeed crucial to obtain the Ni silicide intrusion into SiC NWs.

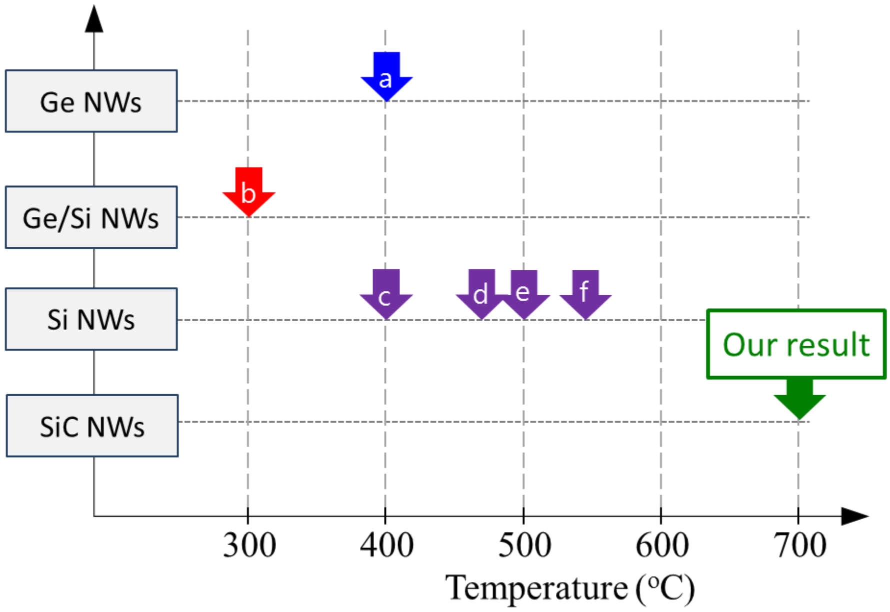


Figure 4.28 Temperature of Ni silicide intrusion into group IV semiconductors NWs. (a: ref. [34], b: ref. [38], c: ref. [35], d: ref. [2], e: ref [36] and f: ref. [37]).

The stoichiometric composition of Ni silicided formed on SiC NW has not been investigated in this study. For the analysis of our results, a bibliography study of the Ni-SiC reaction has been performed. The reaction of Ni with bulk SiC has been fully investigated as a function of annealing temperature [32, 40, 41]. In a previous study on Ni-based contacts on 3C-SiC substrate [32], Ni remained unreacted after annealing up to 600 °C. Further annealing at 750 and 850 °C, a coexistence of the Ni_5Si_2 and the Ni_2Si phase were observed by x-ray diffraction (XRD). After annealing at 950 °C, the most thermodynamically stable phase (Ni_2Si) was detected. It is normally required a high temperature annealing in the range of 900 - 1000 °C to get a stable Ni-based ohmic contact on SiC with high-reliability. In case of SiC nanostructures, all phases of Ni silicide formed during the annealing is easily diffused into a confined SiC NW channel. As a result, the maximum annealing temperature on SiC nano-devices is limited by the Ni silicide intrusion into the channel.

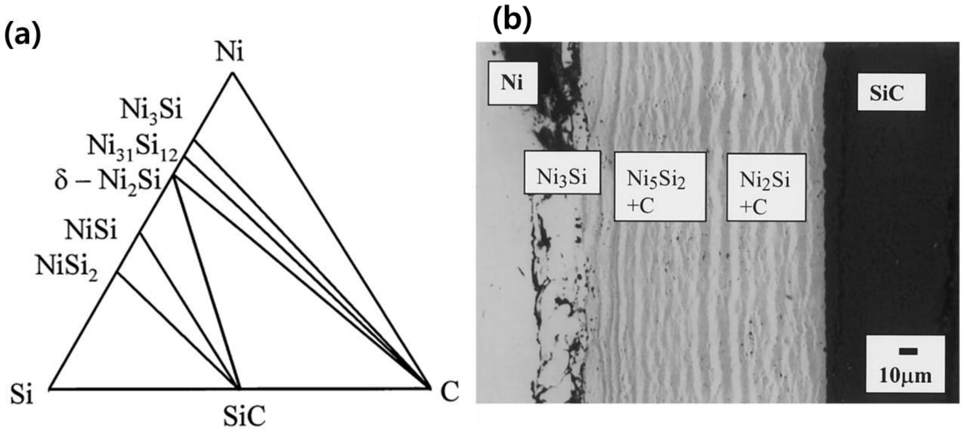


Figure 4.29 (a) Ni–Si–C ternary phase diagram [43] and (b) backscattered electron image of bulk SiC/Ni reaction after high temperature annealing [42].

According to the related bibliography [41, 42], when SiC is consumed by the solid state reaction with Ni metal, Ni predominantly reacts with Si and forms the Si-rich Ni silicide. The Ni–Si–C ternary phase is shown in Figure 4.29(a). It has also been reported that annealing at lower temperatures can result in the presence of various silicide phases (Ni_2Si, $Ni_{31}Si_{12}$ and Ni_3Si_2 silicides) [43].

Whereas unreacted carbon atoms tend to precipitate into (graphite-like) carbon clusters instead of forming carbides, as described by the following equation (Eq 4.4).

$$SiC + Ni \rightarrow Ni_xSi_y \text{ (Ni silicides)} + C \text{ (graphite)} \qquad \text{Eq 4.4}$$

The silicides with carbon clusters were developed as products after the reaction between bulk SiC and Ni [42], as depicted in Figure 4.29(b). It is also known that a segregated carbon clusters in bulk SiC introduce an electron trap below the conduction band edge, which leads to stable ohmic contact formation through the reduction of effective Schottky barrier height [44, 45]. Therefore, formed carbon clusters in SiC nanostructures will further reduce the barrier height.

▣ Ni silicide intrusion behavior with different shapes of SiC NWs

Many studies have been reported about the Ni silicidation on cylinder shape of group IV semiconductors NWs [2, 34-38]. However, to the best of our knowledge, there has been no study of the silicidation process on any other morphology of NWs. Among various shapes of SiC NWs, the needle shape of SiC NWs has proved to be well suited for field electron emission applications [46]. Needle shape of NWs could also be used as building block for fabrication of advanced electronic devices, because of their unique electrostatic characteristics due to the asymmetric diameter along the NWs [47]. Therefore, it is worthwhile to investigate the Ni silicidation on SiC NWs with a needle shape.

Figure 4.30 shows SEM images and schematic illustrations of cylinder and needle shapes of SiC NWs with Ni silicide intruded contacts after annealing at 700 °C for 30 s. As reported earlier, the Ni silicide progressively and uniformly diffuses into the SiC NW channel during the silicidation process in Figure 4.30(c) side-view.

A curved section is observed near the metal electrode in Figure 4.30(a), which is comparable to the results of other group IV semiconductors (Si, SiGe) NWs reported elsewhere [35, 48]. The intrusion of Ni silicide into SiC NWs roughly increases the volume around by 90% (3C-SiC: a= 4.3596 Å and $NiSi_2$: a= 5.406 Å). As a result, a straight SiC NWs is transformed into a curved SiC NWs due to the induced strain by the volume expansion as depicted in Figure 4.30(c) top-view.

The Ni silicidation on needle shape SiC NW shows different intrusion behavior because the diameter of NW is reduced toward the tip apex. In the case of cylinder SiC NW, the consumption rate of SiC by the solid state reaction and the Ni silicide intrusion rate is balanced along the channel. On another hand, the consumption rate of SiC in needle shape SiC NW is decreased toward the tip apex while the Ni silicide intrusion rate is constant. As a result, Ni silicide grows in a radial direction together with the axial direction, as depicted in a magnified picture in Figure 4.30(d) side-view. When the Ni silicide intrusion rate is much larger than the consumption rate of SiC, it reaches a very high degree of supersaturation. Consequently, the Ni silicide will precipitate in shape of the droplet. Therefore, periodic precipitation of Ni silicide leads to the formation of the bead necklace like morphology in Figure 4.30(b) and Figure 4.30(d) top-view.

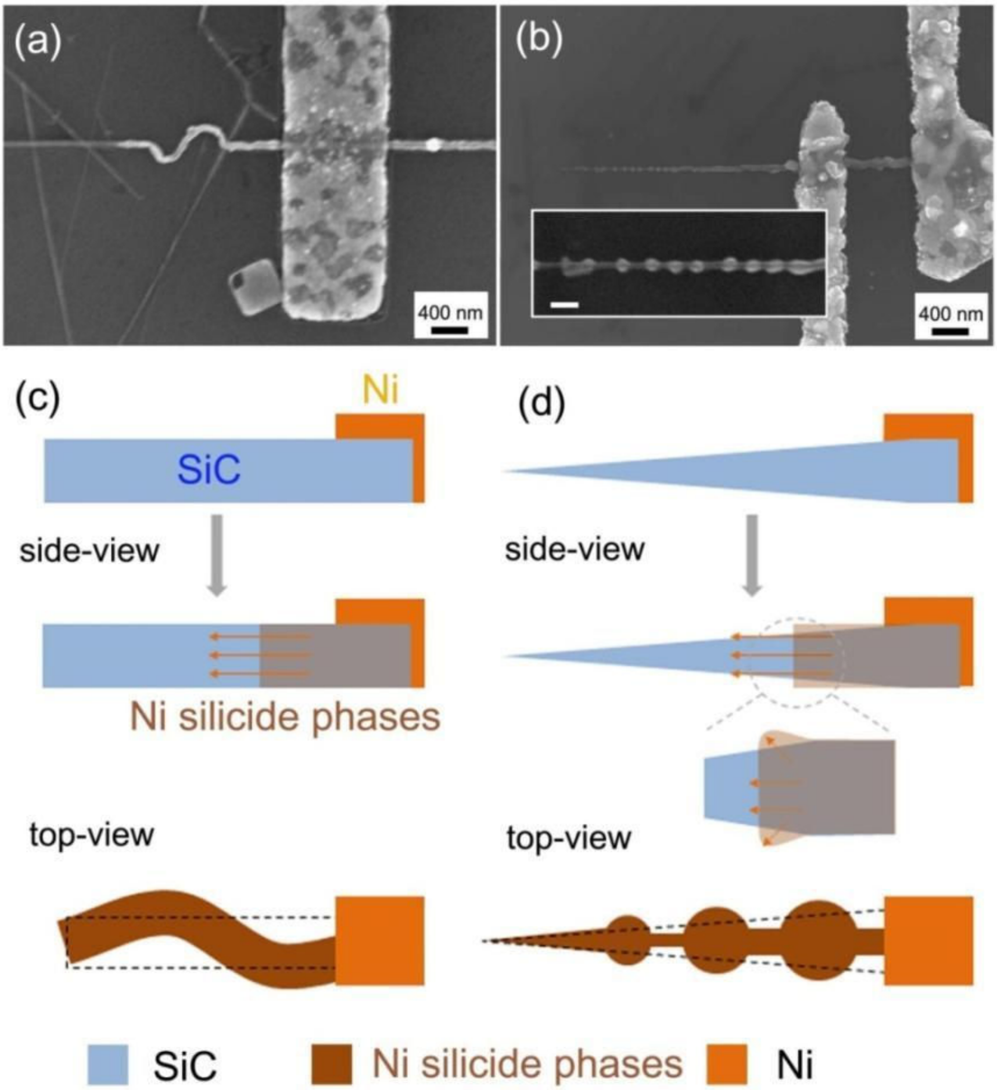


Figure 4.30 SEM images of Ni silicide intrusion into (a) the cylinder and (b) the needle shape of SiC NWs after annealing at 700 °C during 30 s (Inset: a magnified images of the apex of needle SiC NW, The scale bar in inset of b = 100 nm), schematic illustration of the diffusion process of Ni silicide into (c) the cylinder and (d) the needle shape of SiC NWs. (Top-view: dashed - before annealing and filled - after annealing)

However, our explanation of Ni silicide intrusion into needle shape SiC NW is only based on the SEM images. To prove our speculation, it needs more experimental evidences (such as TEM studies coupled with EDX and electron energy loss (EELS) spectroscopies).

- ▣ Summary and perspectives on SiC nanowire ohmic contact formation by Ni silicidation

Ni based silicidation is a key process to guarantee the stability and repeatability of ohmic contact by tailoring the metal-semiconductor interface. In addition, the longitudinal Ni-silicide formation at the both ends of a SiC NW (Ni silicide-SiC-Ni silicide heterostructure) can provide controlled injection geometry with carrier transfer coming atomically sharp epitaxial interfaces between Ni silicide and SiC [2, 48]. Hence, the silicidation process can reduce the Fermi level pinning effect due to the suppression of the surface state. Precisely controlled Ni silicide diffusion along the NW's channel can allow the fabrication of ultra-short channel transistors [49].

In our experimental results, we did not schematically study the stoichiometry of Ni contacts according to the annealing temperatures. However, from the I-V characteristic of SiC NWFT, the annealing temperature significantly influences on the current level and the total resistance (including the contact and the channel resistance). In case of our device process, the annealing temperature of 650 °C has been found as the optimum temperature for low ohmic contact of SiC NWFET, which shows the linear behavior of $I_{2\text{-}3}$-$V_{2\text{-}3}$ curve and a low contact resistance (378 kΩ). Ni silicidation process itself is favorable to get a low ohmic contact resistance by modifying the Ni-SiC interfaces. But Ni silicide intrusion into the channel by silicidation is another story.

In case of Si NW, ultra-short channel fabricated by precisely controlled Ni silicide intrusion with top gate structures have shown a better electrical properties compare to the conventional back-gate Si NWFET. However, our results of Ni silicide intrusion into SiC NWs are quite disappointing. When Ni silicides intrude into SiC NW, SiC NW is curved or detached from the contacts due to the induced strain by the volume expansion. Moreover, when the channel length of SiC NW is shorter than the Ni silicide diffusion length, the device does not operate as a FET due to the metallic property of fully Ni silicided SiC NW. It is more difficult to control the Ni silicide intrusion length in SiC NW compare with one in Si NWs due to relatively high annealing temperature.

To further exploit excellent electrical property of SiC NWs, other silicidation materials and their silicide-SiC heterostructures, which have been done in Si NWs (such as, Pt [48], Co [50] and Mn [51]), would be interesting to investigate.

4.3.3 Electrical properties of SiC nanopillar FETs

Two kinds of SiC substrates with controlled doping level (3C-SiC (001) hetero-epilayer substrates from Linköping Uni. and 4H-SiC (0001) mono-epilayer substrates from Ampère) have been used to fabricate SiC NP arrays, as depicted in Figure 4.31(a-b). Figure 4.31(c) and (d) show SiC NP arrays fabricated by top-down method as we have shown in section 3.

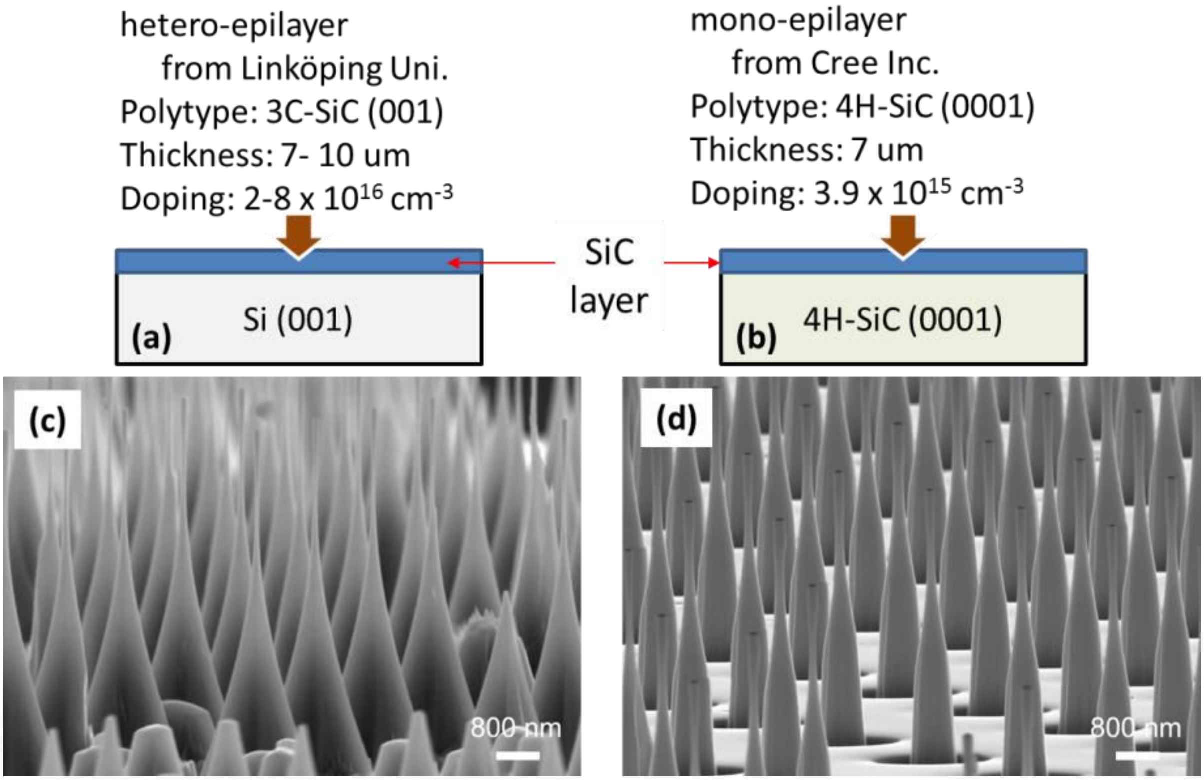


Figure 4.31 (a) hetero- and (b) mono- SiC epilayer substrates used for the fabrication of SiC NPs. (a) 3C-SiC layer grown on Si (001) substrate, (b) 4H-SiC layer grown on 4H-SiC (0001) substrate. SEM images of (c) 3C-SiC (001) and (d) 4H-SiC (0001) NP arrays.

Generally, most as-grown 3C-SiC NWs fabricated by the bottom-up methods are oriented towards the <111> dense growth direction. For heteroepitaxial growth of 3C-SiC on Si substrate, Si (001) plane is commonly used instead of Si (111), because it is possible to achieve thick SiC epitaxial layers on large area substrates using Si (001) substrate with low density of planar defects, such as twin boundaries and anti-phase boundaries, due to increasing thickness through mutual canceling [52]. Heteroepitaxial growth of 3C-SiC is done at Linköping university on Si (001) substrate [53]. Therefore, the fabricated 3C-SiC NPs in this study exhibits a crystalline orientation with [001] direction.

The contact annealing of fabricated SiC NPFETs on the above substrates was carried out at 650 °C for 30 *s* with ambient N_2 in a rapid thermal annealer (Jetfirst 100). Electrical properties of NPFETs were measured at room temperature and in ambient air with HP 4155.

▣ Electrical properties of 3C-SiC (001) NPFET

All previously reported results of SiC NWFET were oriented towards the <111> direction with 3C polytypes, but the channels of fabricated 3C-SiC NPFETs in Figure 4.32(a-b) are along <001> direction with doping level of 2-8 ×10^{16} cm^{-3}. The dimensions of two different 3C-SiC NPFET measured from SEM images are:

- ✓ 3C-SiC NPFET (#1): diameter: 110 nm and length: 340 nm (Figure 4.32 (a), (c) and (e))
- ✓ 3C-SiC NPFET (#2): diameter: 120 nm and length: 620 nm (Figure 4.32 (b), (d) and (f))

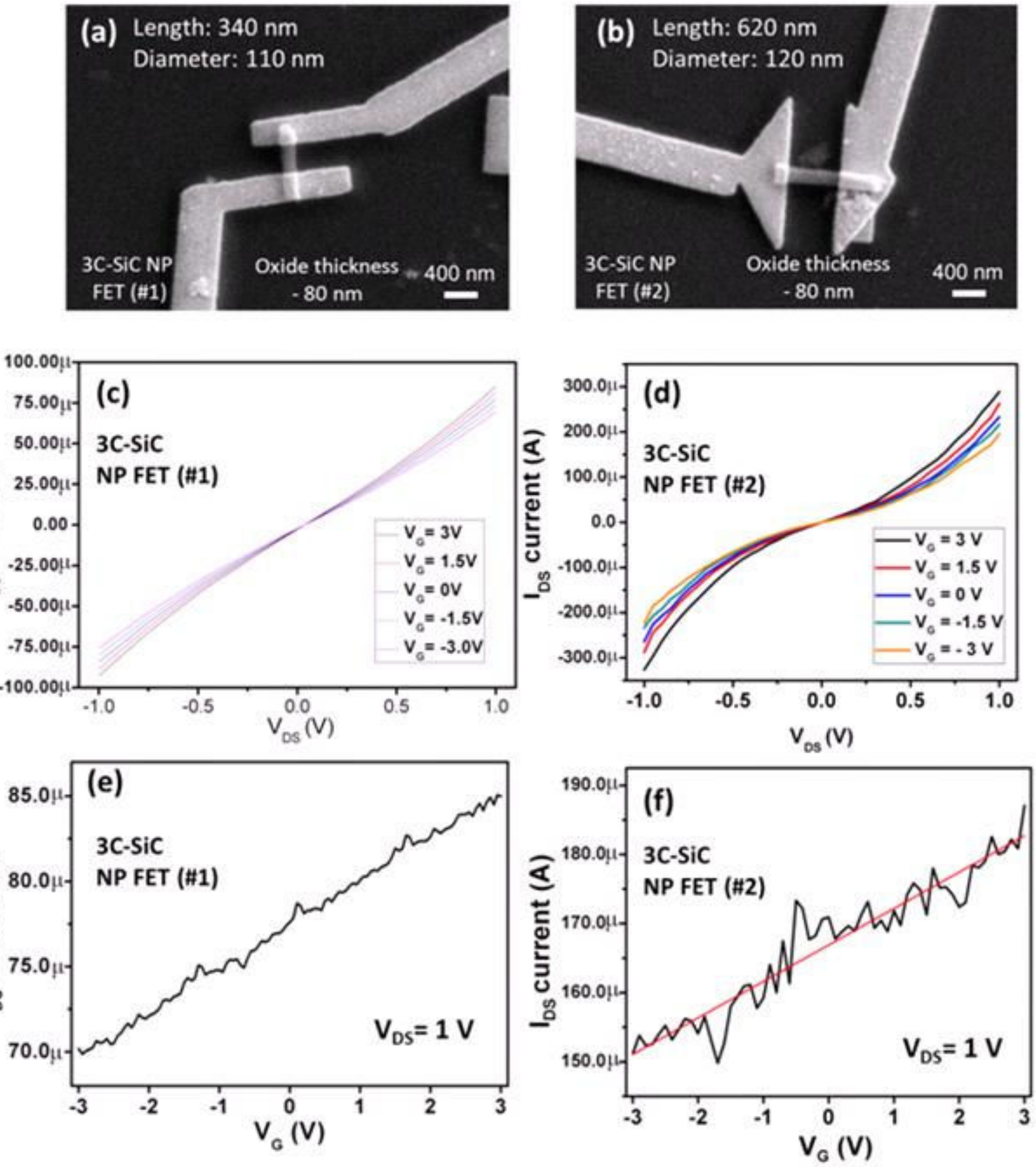


Figure 4.32 (a,b) SEM images of two fabricated 3C-SiC (001) NPFETs with different dimensions, (c,d) I_{DS}-V_{DS} curves of 3C-SiC (001) NPFET as a function of gate voltage (V_G), (e,f) I_{DS}-V_G curves of 3C-SiC (001) NPFET.

Figure 4.32(c)-(f) shows the corresponding I-V curves after the annealing at 650 °C. The level of current that has been measured is high, and will be further explained based on the simulation results. First, one can underline that no gate leakage current has been measured. Secondly, Ni silicide has not been intruded in the channel; SEM observations before and after annealing as well as EDX mapping have confirmed it.

A typical I_{DS}–V_{DS} curves of the device in Figure 4.32(c)-(d) show that the effective S/D current increases as V_G increases from -3 to 3 V. This result clearly indicates that the majority of carriers in the 3C-SiC (001) NP are n-type.

From the measured I-Vs, intrinsic properties like the carrier mobility can be extracted by applying Eq 1.1 – Eq 1.3. However, in our study, the resistance of the contacts is not separated from that of the channel (two-probe measurement). Therefore, the calculated g_m (or mobility) is also underestimated as followed [54] (Eq 4.5);

$$g_m = \frac{g_{in}}{1 + g_{in}R_s + \frac{(R_S + R_D)}{R_G}}, \qquad \text{Eq 4.5}$$

where g_{in} is the intrinsic transconductance, R_S is the source access resistance, R_D is the drain access resistance and R_G is the gated area's resistance. Nonetheless, other authors [33, 55] didn't account for Eq. 4.5 followed the same method to determine carrier mobility in order to determine a "rough" value. We have adopted the same approach and thus, one can compare our results with that of reported experimental studies.

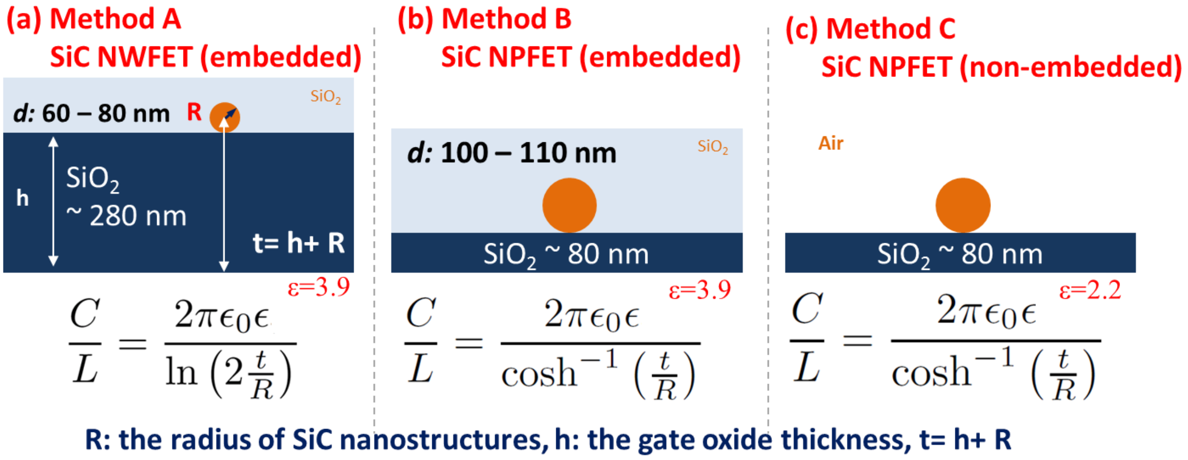


Figure 4.33 Estimation of the gate capacitance for (a) SiC NWFET with the approximation and for (b-c) SiC NPFET without the approximation at (b) ε=3.9 and (c) ε=2.2, respectively.

For the calculation of mobility, the gate capacitance (C_{ox}) of nano FET could be estimated by the metallic cylinder on an infinite metal plate model [56], as described the following equation (Eq 4.6);

$$C_{ox} = \frac{2\pi\varepsilon\varepsilon_o L}{\cosh^{-1}(\frac{t}{R})}, \qquad \text{Eq 4.6}$$

where R is the radius of NW, t is the distance between the metal plate and the center of the NW (see Figure 4.33). The $\cosh^{-1}(x) = \ln(x + \sqrt{x^2 - 1})$ can be approximated into ln(2x) when x = t/R >>1. Therefore, the equation of gate capacitance could be calculated by this approximation method as followed (Eq 4.7):

$$C'_{ox} = \frac{2\pi\varepsilon\varepsilon_0 L}{\ln(2t/R)},\qquad \text{Eq 4.7}$$

So, all previous reported studies of SiC nanoFET calculated the gate capacitance by using this approximation method. But, in case of SiC 3C-SiC NPFET (dev #1), t (130 = 80 nm (h: oxide thickness) + 50 nm (R: the radius of NP)) is slightly larger than the radius of NP (R=50 nm), which t/R is 2.6. Therefore, it would be more appropriate to use the non-approximated equation (Eq 4.6) for the device with thin gate oxide thickness although the low value of t/R will involve an error higher than 3% [56]. However, this capacitor model assumes that the oxide fills the entire space surrounding the nanoFET, as shown in Figure 4.33(a) and (b). In reality, the gate oxide exists only as a film, the NW fully exposed to air, as shown in Figure 4.33(c). As a result, this capacitor model overestimates the real value of the capacitance in the case of non-embedded in the gate dielectric NWs, an effective value of 2.2 has been used for the dielectric constant of SiO_2 to reduce this error [56]. In this study, the gate oxide capacitances calculated from three different methods, as listed in Table 4.4.

Table 4.4 Estimated gate capacitance of 3C-SiC NPFET by three different methods.

3C-SiC NPFET	Dev #1	Dev #2
C'_{ox} by approximation method (Eq 4.7)	0.069 fF	0.137 fF
C_{ox} by non-approximation method (Eq 4.6) with ε=3.9	0.047 fF	0.087 fF
C_{ox} by non-approximation method (Eq 4.6) with ε=2.2	0.027 fF	0.049 fF

The calculation based on the line at V_G = 0 V yields a two-terminal resistivity of 36 mΩ·cm (3C-SiC (001) NPFET dev #1) and 17 mΩ·cm (3C-SiC (001) NPFET dev #2), which is derived from Eq 4.2. From the above I_{DS}–V_G curve in Figure 4.32(e) and (f), a transconductance (g_m) of 2.58 µS (3C-SiC (001) NPFET dev #1) and 5.27 µS (3C-SiC (001) NPFET dev #2) at V_{DS} = 1.0 V for 3C-SiC NPFET (dev #1) and (dev #2) is obtained, respectively.

The gate oxide capacitances calculated from three different methods are 0.069 fF, 0.047 fF and 0.027 fF for 3C-SiC NPFET (dev #1), and 0.137 fF, 0.087 fF and 0.049 fF for 3C-SiC (001) NPFET (dev #2), respectively, as listed in Table 4.4. As I mentioned earlier, non-approximation method for the calculation of gate capacitance is more appropriate than approximation due to thin gate oxide thickness of SiC NPFET. However, all previous reported studies of SiC nanoFET calculated the gate capacitance by using this approximation method. In order to compare with previous reported studies of SiC nanoFET, gate capacitances calculated by both approximation and non-approximation methods have been used to estimate the mobility of SiC NPFET.

The estimated field-effect carrier motilities from (Eq 1.3) are 43.2 $cm^2 \cdot V^{-1} s^{-1}$ based on C'_{ox} by the approximation method, 62.5 $cm^2 \cdot V^{-1} s^{-1}$ (at ε=3.9) and 108.8 $cm^2 \cdot V^{-1} s^{-1}$ (at ε=2.2) based on C_{ox} by the non-approximation method for 3C-SiC NPFET (dev #1), and 147.8 $cm^2 \cdot V^{-1} s^{-1}$ based on C'_{ox} by the approximation method and 232.7 $cm^2 \cdot V^{-1} s^{-1}$ (at ε=3.9) and 411.6 $cm^2 \cdot V^{-1} s^{-1}$ (at ε=2.2) based on C_{ox} the non-approximation method for 3C-SiC NPFET (dev #2). These value of the field-effect carrier mobility of 3C-SiC NPFET are found to be higher than the best reported values (15.9 $cm^2 \cdot V^{-1} s^{-1}$) in a previous study [33], but it is still quite lower compared to that expected in the n-type 3C-SiC bulk (650 $cm^2 \cdot V^{-1} s^{-1}$ for $n = 8\times 10^{16}$ cm^{-3}) [27]. The simulation has been used to correlate the experimentally measured I-V curves at different mobility values.

Figure 4.34 shows the experiment and the simulation results of 3C-SiC NPFETs. The Simulations have been done in drift-diffusion region using two dimensional Silvaco program (Atlas, ver. 5.18.3.R), which has already been developed by Rogdakis et al. [55]. Same devices dimensions of fabricated 3C-SiC NPFETS have been used for the simulation at ideal interface (without fixed charges in the oxide and no structural defects) without consideration of gate effect (V_G=0V) at doping level of 8 × 10^{16} cm^{-3}. In particular, the current of 3C-SiC NPFETs has been estimated from the calculated carrier motilities using Silvaco program.

In case of 3C-SiC NPFET (dev #1) in Figure 4.34(a), the simulated I_{DS} current is smaller than the experimentally measured one. However, when we increase the carrier mobility up to 200 $cm^2 \cdot V^{-1}s^{-1}$, the simulated I-V curve shows similar electrical behavior compare to the experimentally measured curve.

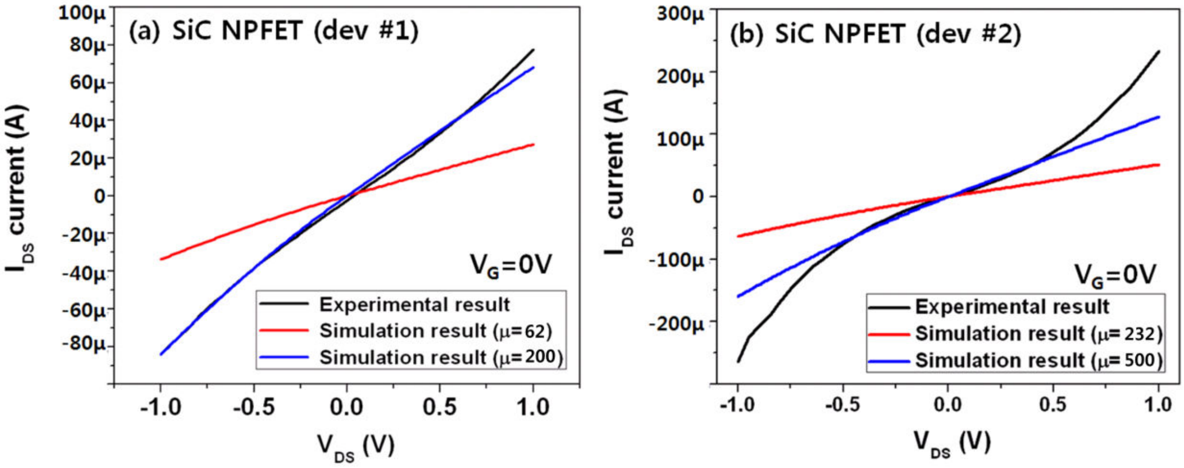


Figure 4.34 The experimental and the simulation results with different carrier mobility of 3C-SiC NPFETs; (a) dev #1 and (b) dev #2 (The unit of µ in the graph is $cm^2 \cdot V^{-1}s^{-1}$).

First of all, one has to keep in mind is that our simulated the structure in the Silvaco program is in two dimensions, so it is not enough accurate to describe the electrical behavior in the 3D structure. However, Rogdakis et al. [55] have already shown that 2D structure in Silvaco program roughly describe the electrical behavior of 3D structure.

Second, another possible reason might be due to the overestimation of gate capacitance. The calculated value of C_{ox} based on the metallic cylinder-plane model, even with the non-approximated equation (Eq 4.6), might overestimate the back-gate capacitance. This metallic cylinder-plane model assumes that the entire NW is electrostatically metallic, and the NW is assumed to be infinitely long [57]. In reality, the induced charges are more likely located on the bottom of NW surface. Moreover, the channel of NW is not infinitely long, which leads to distortion of the electric field near the metal electrodes. As a result, the overestimated capacitance (C_{ox}) leads to an underestimation of the field-effect carrier mobility from (Eq 1.3).

As we mentioned earlier, we cannot fully separate the channel resistance from the I-V curve using two-probe methods. Therefore, the calculated mobility also could be underestimated as described in Eq 4.5.

In case of 3C-SiC NPFET (dev #2), the simulated I_{DS} current is also smaller than the experimentally measured one, as shown in Figure 4.34(b). When we increase the carrier mobility up to 500 $cm^2 \cdot V^{-1}s^{-1}$, the simulated I-V curve is closely matched with the experimental measured curve in the linear region (from –0.5V to 0.5 V).

When we implement the maximum mobility (700 $cm^2 \cdot V^{-1}s^{-1}$ obtained in the bulk for n=8× 10^{16} cm^{-3}) into the 3C-SiC nanoFET structures, the simulated current could be increased (at V_{DS}= 1V) up to 318 µA for SiC NPFET (dev #1) and 179 µA for SiC NPFET (dev #2), respectively, as shown in Figure 4.35.

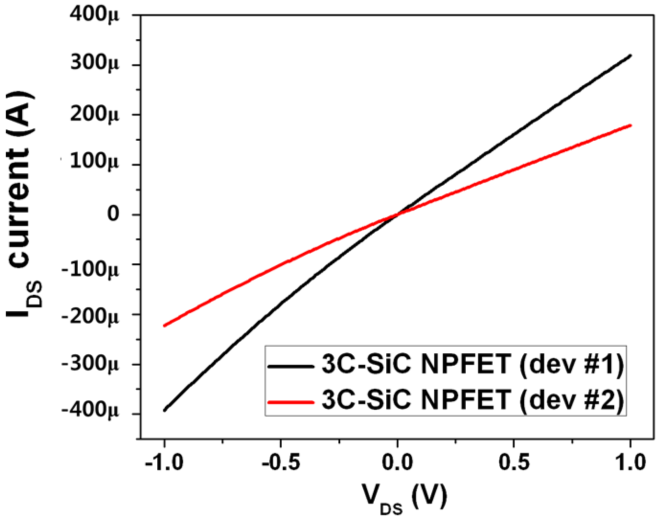


Figure 4.35 Simulated characteristics of 3C-SiC NPFETs at the maximum mobility (700 $cm^2 \cdot V^{-1}s^{-1}$) obtained in the bulk at the doping level of 8×10^{16} cm^{-3}.

The simulation of transfer characteristic (I_{DS}-V_G) of SiC NPFETs has not been investigated in this study. If the simulation of transfer characteristic of SiC NPFETs is demonstrated, we can further characterize the device performance of SiC NPFETs, such as the interface charge density (D_{it}) and the Schottky barrier height [55].

▣ Electrical properties of 4H-SiC (0001) NPFET

Figure 4.36 shows the image of fabricated 4H-SiC (0001) NPFET before the annealing and the I-V curves of NPFET (a diameter of ~ 110 nm and a channel length of ~ 570 nm) after the annealing at 650 °C. The 4H polytype SiC NPFET with <0001> direction is first presented in study.

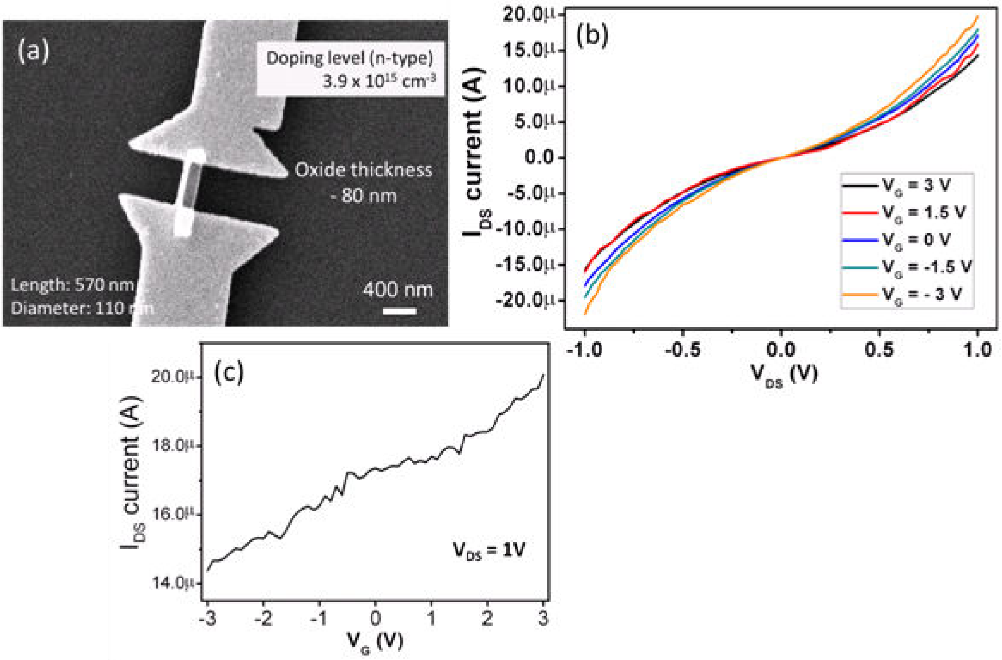


Figure 4.36 (a) SEM image of fabricated 4H-SiC (0001) NPFET, (b) I_{DS}-V_{DS} and (c) I_{DS}-V_G curves of 4H-SiC (0001) NPFET.

A typical I_{DS}–V_{DS} curve of the device in Figure 4.36(b) shows n-type behavior, which the effective I_{DS} current increases as V_G increases from -3 to 3 V. The two-terminal resistivity of 4H-SiC (0001) NPFET from Eq 4.2 is 0.19 Ω·cm. From the above I_{DS}–V_G curve in Figure 4.36(c), a transconductance (g_m) of 1.32 μS for 4H-SiC (0001) NPFET is obtained.

The gate oxide capacitances of 4H-SiC NPFET calculated from both approximation (Eq 4.7) and non-approximation methods (Eq 4.6) at ε=3.9 and ε=2.2 are 0.115 fF, 0.080 fF and 0.045 fF, respectively. The estimated field-effect carrier motilities from (Eq 1.3) are 37.1 based on C'_{ox} by the approximation method and 53.6 $cm^2·V^{-1}s^{-1}$ (at ε=3.9) and 95.2 $cm^2·V^{-1}s^{-1}$ (at ε=2.2) based on C_{ox} by the non-approximation method for 4H-SiC (0001), but it is still quite lower compared to that expected in the n-type 4H-SiC bulk (900 $cm^2·V^{-1}s^{-1}$ for n=1× 10^{15} cm^{-3}) [27].

The 4H-SiC (0001) NPFET could not be completely depleted up to - 3V in Figure 4.36(c), as similar to the electrical behavior of 3C-SiC (001) NPFET. Therefore, the I_{ON}/I_{OFF} current ratio and subthreshold slope could not be extracted from gate characteristics. Our results of SiC NPFET and comparison with best reported results of SiC NWFET are summarized in Table 4.5.

Table 4.5 Results of SiC NPFET performance and comparison with SiC NWFET.

	3C-SiC NPFET (dev #1)	3C-SiC NPFET (dev #2)	4HSiC NPFET	3C-SiC NWFET
Polytypes	3C	3C	4H	3C
Fabrication methods of SiC nanostructures	Top-down	Top-down	Top-down	Bottom-up [33]
Research Group	Our work	Our work	Our work	Zhou *et al.*
Crystal orientation	<001>	<001>	<0001>	<111>
Diameter	110 nm	120 nm	110 nm	20 nm
Length	340 nm	620 nm	570 nm	1.5 μm
Oxide thickness	80 nm	80 nm	80 nm	500 nm
Doping concentration (cm^{-3})	2 - 8 × 10^{16}	2 - 8 × 10^{16}	3.9 × 10^{15}	(estimated) 5.6 ×10^{18}
g_m (S)	2.58 μS at V_{DS}= 1V	5.27 μS at V_{DS}= 1V	1.32 μS at V_{DS}= 1V	0.5 nS at V_{DS}= 0.01V
C'_{ox} (F) with method A	0.069 fF	0.137 fF	0.115 fF	0.070 fF
C_{ox} (F) with method B (ε=3.9)	0.047 fF	0.087fF	0.080 fF	0.070 fF
C_{ox} (F) with method C (ε=2.2)	0.027 fF	0.050 fF	0.045 fF	0.039 fF
μ′ ($cm^2·V^{-1}s^{-1}$) with method A	43.2	147.8	37.1	15.9
μ ($cm^2·V^{-1}s^{-1}$) with method B (ε=3.9)	62.5	232.7	53.6	15.9
μ ($cm^2·V^{-1}s^{-1}$) with method C (ε=2.2)	108.8	411.6	95.2	28.5

In case of NPFET, there is a big difference of the estimated gate capacitance between approximation (method A) and non-approximation methods(method B) due to the thin oxide layer (80 nm). In case of our SiC NWFETs and the previously reported results of SiC NWFET [33], the gate capacitance and the mobility of SiC NWFETs calculated by both approximation (method A) and non-approximation methods (method B) show exactly same values since the gate oxide thickness is thick enough (280 – 500 nm).

▣ Discussion on results concerning the doping concentration of SiC NPFETs

Based on the calculated transconductance and carrier mobility, the carrier concentration also can be estimated by using the following formula [13];

$$I_{DS}=nq\mu V_{DS}A/L, \qquad \text{Eq 4.8}$$

where n the electron concentration, q the electron charge and A the area of NW cross section.

The estimated electron carrier density of SiC NWFET fabricated by bottom-up method were estimated to be ~ 1.7×10^{20} cm^{-3} due to high n-type unintentional doping incorporated during the growth [55]. Our SiC NPFET fabricated by top-down method can control the NW doping since it is the same as that of the initial bulk material. Table 4.6 shows the estimated doping concentration of SiC NPFET using Eq 4.8 based on the calculated carrier mobility with three different methods. The estimated doping concentrations are one or two order of magnitude higher than the doping level of SiC layer.

Table 4.6 Estimated doping concentration for the investigated SiC NPFETs.

	Estimated doping concentration (cm^{-3})			Measured doping concentration of SiC layer
	using μ′ calculated by method A	using μ calculated by method B	using μ calculated by method C	
3C-SiC NPFET (dev #1)	2.27×10^{18} cm^{-3}	1.57×10^{18} cm^{-3}	9.01×10^{17} cm^{-3}	2-8 $\times 10^{16}$ cm^{-3}
3C-SiC NPFET (dev #2)	2.57×10^{18} cm^{-3}	1.63×10^{18} cm^{-3}	9.23×10^{17} cm^{-3}	2-8 $\times 10^{16}$ cm^{-3}
4H-SiC NPFET	8.74×10^{17} cm^{-3}	6.05×10^{17} cm^{-3}	3.4×10^{17} cm^{-3}	3.9×10^{15} cm^{-3}

Note that the above method for extracting the mobility (Eq 1.3) and the carrier concentration of the SiC nanoFETs (Eq 4.8) assumes that the extrinsic transconductance is equal to the intrinsic one although the measured extrinsic transconductance is reduced from its intrinsic value, as described in Eq 4.5. In addition, the doping concentration calculated by Eq 4.8 is a rough approximation since it considers no depletion inside the channel, which would result in a reduction of the section through which the current passes.

Another difficulty with SiC nanoFETs is the experimental estimation of the interface trap density and fixed charges. The interface traps and parasitic effects are neglected in Eq 1.3 and Eq 4.8, which leads to underestimated experimental mobility values (at least a factor of two) [55].

We tried to estimate the doping concentration with three different methods, the method C seems quite a bit more appropriate than other methods because the estimated doping level of NPFET calculated by method C is far less than measured doping concentration of SiC epi-layer.

Discussion on results concerning the electrical properties of SiC NPFETs

Generally, the weak gating effects in 3C-SiC NWFET is partly explained by the high density of donor states (which close to the metallic limit). Rogdakis et al. [55] have shown that it is possible to have a good gating effect at a doping level of 10^{15} - 10^{16} cm^{-3} and below with ideal interfaces by the simulation study. However, even though a fabricated 3C-SiC (001) and 4H-SiC (0001) NPFETs present an appropriate doping level in the range of 3.9×10^{15} cm^{-3} and 2 - 8 $\times 10^{16}$ cm^{-3}, the device performance of NPFETs shows 2 - 5 times lower compared to that expected value from theoretical calculation (from *ref.* [55]). In addition, the NPFETs couldn't be completely switched-off.

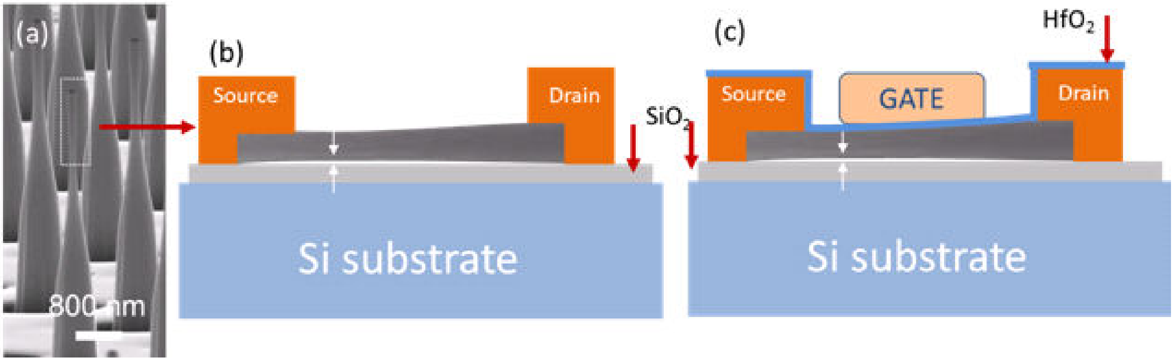


Figure 4.37 (a) SEM images of 4H-SiC (0001) NP arrays before the sonication, (b) the cross section of 4H-SiC (0001) NPFET, (c) the cross section of 4H-SiC (0001) NPFET with top-gate.

The observed gate characteristics (weak gate control on output characteristics and no possibility of switching-off) of the NPFETs might be due to weaker electrostatic gating effects due to weak gate coupling caused by the broken NPs having a concave shape. Fabricated SiC NPs by top-down methods are not completely straight, but of concave shape (Figure 4.37(a)). Therefore, there exists a gap between the broken NPs and SiO_2/Si substrate as indicated by the arrows in Figure 4.37(b). As a result, it can't guarantee excellent gate coupling of NPFET due to poor SiC NP-gate oxide interface. In case of the interface between Si and SiO_2 in planar devices, the density of electrically active interface states (D_{it}) could be possibly reduced in the range of 10^{10} cm$^{-2}\cdot$eV^{-1} with suitable processing. However, other IV-IV compound semiconductor, such as SiC and SiGe, is difficult to reduce D_{it} below (<10^{11} cm$^{-2}\cdot$eV^{-1}), whichever methods of developed process is used [58]. Therefore, the bad interface between SiC NP and SiO_2 gate oxide layer could be another reason, as proved in the numerical calculation [55].

High-*k* stack gate structures of SiC NPFETs

The gate coupling of NPFET would eventually be improved by implementing high-*k* gate stack on top gate, as illustrated in Figure 4.37(c). For this reason, the top-gate 3C-SiC (001) and 4H-SiC (0001) NP FETs have been fabricated by the deposition of HfO_2 layer (20 nm) using Atomic Layer Deposition (ALD) and the subsequent deposition of a metal layer (Au, 100 nm) (Figure 4.38). High-*k* gate stack on top gate structure of SiC nanoFET is realized, for the first time, in this study.

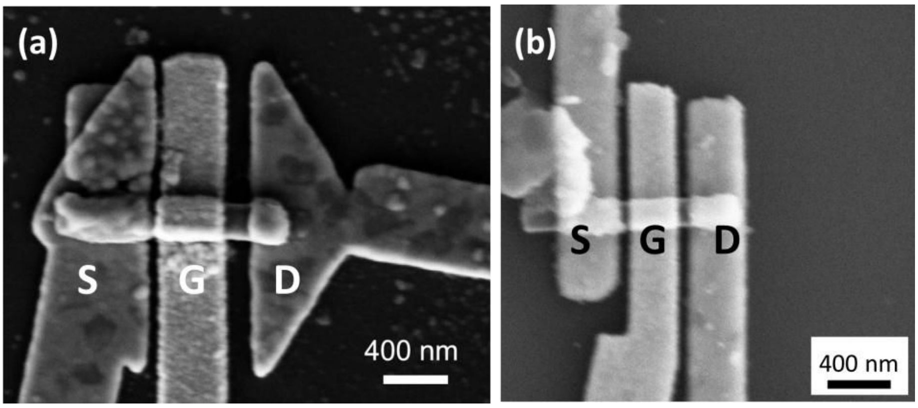


Figure 4.38 SEM images of top-gate (a) 3C-SiC (001) and (b) 4H-SiC (0001) NPFET with the deposition of HfO_2 (20 nm).

However, the top-gated 3C-SiC (001) and 4H-SiC (0001) NP FETs showed no electrical current after the fabrication of top gate structure. Since the ALD process was new and has not been fully optimized for the deposition of high-*k* materials (*e.g.* deposition temperature, source species and flow rate), it was our first result of the deposition of HfO_2 layer by this technique. It is believed that the imperfection of high-*k* (HfO_2) deposition, such as the deposition temperature (200 °C) of Hf precursor and oxidation step using Ar plasma with H_2O source, during ALD process leads to device failure. Therefore, it is needed to optimize the ALD process for the high-*k* materials to elaborate the reliable top-gate SiC NPFET.

4.4 Conclusion and perspectives of work

To achieve excellent performance of SiC nano-devices, it is needed to improve three main issues: (First: metal ohmic contact on nanoFET, second: poor quality of SiC NW with associated stacking fault and unintentional n-type doping, last: the NW (or NP)-gate oxide interface). To address these issues, two different kinds of SiC nanoFET (SiC NWFET and SiC NPFET) been fabricated and characterized.

To improve the metal ohmic contact on SiC nanoFET, Ni based contact property on SiC NW FET has been investigated as a function of the annealing temperature, since Ni based silicidation is a key process to guarantee the stability and repeatability of ohmic contact by tailoring the metal-semiconductor interface. Low resistivity ohmic contacts have been obtained after the annealing at 650 °C. Ni silicide begins to intrude into SiC NWs channel after annealing at 700 °C, a substantially higher temperature for the appearance of this phenomenon in comparison to other group IV materials. It has been demonstrated a SiC-Ni silicide (or Ni silicide-SiC-Ni silicide hetero-structures and a fully Ni silicided SiC NW by the intrusion of Ni silicide after annealing at 700 °C for 30 s depending on the channel length. It is interesting that Ni intrusion into needle shape of SiC NWs results in the bead necklace like morphology due to the reduction of diameter toward the tip apex.

In order to eliminate the effect of high residual doping and/or any effects resulting from the high density of stacking faults top-down SiC NPFET have been fabricated by using ICP etched NP arrays as demonstrated in chapter 3. Two different types of NPFET (3C-SiC (001) and 4H-SiC (0001) NPFET) are demonstrated. The estimated value of the field-effect electron mobility are 108.8 $cm^2 \cdot V^{-1}s^{-1}$ and 411.6 $cm^2 \cdot V^{-1}s^{-1}$ for 3C-SiC (001) NPFET (dev #1 and dev #2) and 95.2 $cm^2 \cdot V^{-1}s^{-1}$ for 4H-SiC (0001) NPFET, are higher compared to the previously reported (*ref.* [33]) best values (15.9 $cm^2 \cdot V^{-1}s^{-1}$), but it is still quite lower compared to that expected in the SiC bulk material (several hundred $cm^2 \cdot V^{-1}s^{-1}$).

Even though SiC NPFETs present an appropriate doping level in the range of 3.9×10^{15} cm^{-3} and 8×10^{16} cm^{-3}, the NPFETs couldn't be completely switched-off from I_{DS}-V_G curves. It might be attributed to weak gate coupling originated from poor interface between SiC NP and SiO_2. To further improve the device performance of NPFET, it is strongly needed to develop the top-gate SiC NPFET with the reliable high-*k* material deposition to enhance the gate coupling.

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Conclusion and Perspectives

Conclusions

In this three years Ph.D. thesis (November 2009 - October 2012), I focused on the fabrication of SiC nanostructures and SiC nanoFET technology. To realize high performance SiC nanoelectric devices, it is essential to start with a high quality single crystalline SiC material at the nanoscale. The common technique for the development of SiC NWs is the bottom-up approach. In the chapter one, I have reviewed the growth of SiC nanostructures based on different growth methods, their properties and potential applications.

In the chapter two, electrical transport and thermoelectric properties of Si and SiC NWs have been investigated. In case of SiC NW, it has been employed a combination of NEGF for the electrical transport and NEMD for the lattice thermal transport in the ballistic regime to predict the thermoelectric figure of merit SiC NWs. The ZT of Si terminated SiC NWs (2.05×2.05 nm^2) reaches a maximum value of 1.04 at 600K. SiC NWs doesn't show high thermoelectric efficiency compare to Si NW at room temperature, while SiC NWs is expected to be promising at higher temperature region due to wide gap characteristics. NEGF formalism has been used for the electrical transport and the calculation of thermal conductivity to estimate thermoelectric properties of Si NW. ZT of Si NW is enhanced with an appropriate SR (Δ_m =0.2 nm), which is responsible for a drastic reduction of thermal conductance without significant reduction of electrical conductance. The ZT of Si NW (0.7) for the cross section (3×3 nm^2) with the SR (Δ_m= 0.2 nm) is a little bit higher than the highest experimental ZT value of Si NW (0.6).

The chapter three is dedicated to fabricate SiC nanopillars by top down approach. Under the optimal etching conditions using a large circular mask pattern with 370 nm diameter, the obtained 4H-SiC nanopillars exhibit high anisotropy features (6.4) with a large etch depth (>7μm). I also demonstrated the SiC nanopillars with different polytypes and orientations; the length of these pillars below 100 nm in diameter is around 1.0 μm. Effect of different polytypes (4H-, 6H- and 3C-SiC) and crystallographic orientations - (0001) and (11-20) of 6H-SiC, (001) and (111) of 3C-SiC - have been investigated in order to realize SiC nanopillars.

The morphology of etched SiC nanopillars has shown interesting features depending on the polytypes and crystal orientations. Hexagonal, rhombus and triangle based pillar structures have been obtained using α-SiC (0001), 3C-SiC (001), and 3C-SiC (111) substrates, respectively. These unique morphologies of SiC nanopillars are originated from a complex interplay between their polytypes and crystal orientations.

In the chapter four, Ni based contact property on SiC NWFET has been investigated as a function of the annealing temperature to improve the metal ohmic contact on SiC nanoFET. Low resistivity ohmic contacts of SiC NWFET have been obtained after the annealing at 650 °C. Ni silicide begins to intrude into SiC NWs channel after annealing at 700 °C. This temperature is compared to one of other group IV materials. It has been demonstrated a SiC-Ni silicide (or Ni silicide-SiC-Ni silicide hetero-structures and a fully Ni silicided SiC NW) by the intrusion of Ni silicide after annealing at 700 °C.

After this study, two different types of NPFET (3C-SiC (001) and 4H-SiC (0001)) have been fabricated using our SiC nanopillars, obtained by top-down approach. The estimated values of the field-effect carrier mobility are 411.6 $cm^2 \cdot V^{-1}s^{-1}$ for 3C-SiC (001) NPFET #2 and 95.2 $cm^2 \cdot V^{-1}s^{-1}$ for 4H-SiC (0001) NPFET, which is higher than the best values (15.9 $cm^2 \cdot V^{-1}s^{-1}$) reported in the literature [i], but it is still quite lower compared to that expected in the SiC bulk material (several hundred $cm^2 \cdot V^{-1}s^{-1}$). Even though fabricated SiC NPFETs present an appropriate doping level in the range of 4×10^{15} cm^{-3} and 8×10^{16} cm^{-3}, the NPFETs couldn't be completely switched-off from I_{DS}-V_G curves.

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[i] W. M. Zhou, F. Fang, Z. Y. Hou, L. J. Yan, and Y. F. Zhang, "Field-effect transistor based on β-SiC nanowire," Electron Device Letters, IEEE, vol. 27, pp. 463-465, 2006.

▣ Prospective

Even though a lot of interesting results and considerable progresses have been made in this thesis, there are still several issues left which need more detailed and deeper exploration in future studies.

❖ Further experimental studies

In this study, the length of etched SiC pillars (below 100 nm in diameter) is around 1µm, which is long enough to reveal the electrical property of SiC nano-FETs. However, large circular patterns (300 nm diameter) instead of small patterns (below 100nm) have been used to elaborate SiC nanopillars with a diameter less than 100 nm because the Ni mask erosion was inevitable during the etching process. Therefore, the morphology of SiC nanopillars ends up with considerable tapering. However, if a robust mask material (such as Al_2O_3) with small pattern size is used, longer SiC nanopillars with small diameter might be achieved without any significant pillar narrowing caused by the mask erosion [ii]. In addition, the Bosh process could also be another promising method to realize straight high aspect-ratio SiC nanopillars. I demonstrated the preliminary experimental result of etched 3C-SiC nanopillar using Bosch process in section 3.3.7, but it is still needed to optimize several parameters to elaborate high aspect ratio SiC nanostructures with straight morphology, (such as, etching condition (coil/bias power), the flow rate of C_4F_8 during the passivation steps, the duration of each cycles (passivation and etching step).

Concerning SiC nanoFET development, there are three major issues for their fabrication as already mentioned in section 4.1.2. We significantly increase the carrier mobility of SiC nanoFET by implementing high quality of SiC NP with controlled doping. But, we still can't switch off the SiC NPFET. Therefore, the remaining issues (the quality of contact and poor interface between SiC nanostructures and SiO_2) are needed to be further investigated for the SiC nanoFET. In particular, Schottky contact is favorable for the switching OFF of device by tailoring Schottky barrier at S/D regions. And the electrostatic controllability of the gate can be further improved by implementing a top-gated configuration with high-k dielectric materials.

❖ Possible application of SiC nanopillars

As I summarized in chapter 1, SiC NWs have shown wide potential applications due to their excellent intrinsic properties. In particular, SiC nanopillars fabricated by top-down method in this study can open new possibilities to apply it in widespread applications as listed below.

- Photodetector based on SiC nanopillars
- Photovoltaics based on SiC nanopillars
- SiC nanopillars based hemocytometer for counting cells or related medical applications
- Biosensors based on SiC NPFET
- Stable field emitter based on SiC nanopillars
- Robust SiC nanopillars AFM probes

Kang et. al. [iii] have demonstrated an improved photocurrent of 4H-SiC photo-diodes using the nano-honeycomb structures. The increased photocurrent gain is attributed to the reduced surface reflectance and the

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[ii] M. D. Henry, S. Walavalkar, A. Homyk, and A. Scherer, "Alumina etch masks for fabrication of high-aspect-ratio silicon micropillars and nanopillars," Nanotechnology, vol. 20, p. 255305, 2009.

[iii] M.-S. Kang, S.-J. Joo, W. Bahng, J.-H. Lee, N.-K. Kim, and S.-M. Sang, "Anti-reflective nano- and micro-structures on 4H-SiC for photodiodes," Nanoscale Research Letters, vol. 6, p. 236, 2011.

increased light absorption thanks to nano-honeycomb structures. But, their SiC nano-honeycomb structures shows low aspect-ratio and small pillar height. If our high aspect ratio with small pitch distance of SiC nanopillars is applied on this SiC based photodetector, photocurrent gain could be further improved.

SiC has been considered to be an inefficient material for photovoltaic applications due to its wide band-gap of 2.3 - 3.3 eV. However, if boron doped 3C-SiC substrates (bandgap reduced into around 1.8 eV) are successfully commercialized, SiC nanopillars fabricated using boron doped 3C-SiC substrate leads to an efficient use of sun light and the reduction of surface reflectance. And it might be an excellent candidate for photovoltaic applications operating in harsh environment.

Kim et. al. [iv] have demonstrated a quartz nanopillar hemocytometer for counting of T lymphocytes. SiC nanostructures are well known as interfaces capable of bridging biomaterials and electronic devices because of their excellent biocompatibility. The performance of SiC nanopillar based hemocytometer could be improved due to the increased cell capture yield, which is originated from their biocompatibility. Based on its excellent biocompatibility, SiC NPFETs could be used as a promising tool in biosensor design because of their ultra-sensitivity, selectivity, and label-free and real-time detection capabilities

Because of the unique material properties of SiC including excellent mechanical strength and chemical inertness, SiC nanopillars could be used for specific applications, such as robust nanoneedles for AFM probes or field emitters.

I demonstrated 3C- and 4H-SiC NPFET with controlled doping level using nanostructures fabricated by top-down approach. The device performance of SiC NPFET could be further improved by implementing a high-k material with top gate: If p-type SiC substrates are implemented for the fabrication of SiC nanopillar, p-type behavior of SiC structure could be revealed.

[iv] D.-J. Kim, J.-K. Seol, G. H. Lee, G.-S. Kim, and S.-K. Lee, "Cell adhesion and migration on nanopatterned substrates and their effects on cell-capture yield," Nanotechnology, vol. 23, p. 395102, 2012.

Appendix A1

▣ Several figures-of-merit to evaluate the electrical properties of MOSFET

◈ Output (I_D-V_{DS}) characteristic of MOSFET

Figure A.1(a) show output (I_D-V_{DS}) characteristic of common MOSFET. For an enhancement-mode, n-channel MOSFET exists the three operational modes (subthreshold region, linear region (with including non-linear region) and saturation region) depending on the voltages at the source/drain and gate contacts. The gate voltage determines whether a current flows between the drain and source or not.

- The subthreshold region (V_{GS}<V_T)

In subthreshold region (cut off mode), there is no current flow throughout the drain since the threshold voltage (V_T) is lower than the drain and source voltage. If we apply a small voltage in the drain electrons will flow from the source to the drain. While the current between S/D should ideally be zero when the transistor is being used as a turned-off switch, there is a weak-inversion current, sometimes called subthreshold leakage.

- The linear region ((V_{GS}>V_T) and V_{DS} < (V_{GS}- V_T))

If we apply a small voltage in the drain ($V_{DS} < (V_{GS} – V_T)$), electrons will flow from the source to the drain. The drain current I_D in the linear regime can be expressed as (Eq A.1):

$$I_D = \frac{W}{L}\mu_{eff}C_{ox}\left(V_G - V_T - \frac{V_D}{2}\right)V_D, \qquad \text{Eq A.1}$$

where W is the channel width, L the channel length, μ_{eff} the effective mobility and C_{ox} the effective capacitance of gate oxide. At low drain voltages, the electric field applied along the longitudinal axis is low. Distribution of carriers remains uniform throughout the channel. It behaves as a resistor and the transistor operates as a gate controlled resistance.

- The saturation region ((V_{GS}>V_T) and V_{DS} ≥ (V_{GS}- V_T))

After pinch-off ($V_D > (V_G – V_T)$), the switch is turned on, and a channel has been created, which allows current to flow between the drain and source. Therefore, the drain current of MOSFET is saturated as (Eq A.2):

$$I_D = \frac{W}{2L}\mu_{sat}C_{ox}(V_G - V_T)^2, \qquad \text{Eq A.2}$$

where μ_{sat} is the carrier mobility in saturation region.

- The non-linear region

There exists the non-linear region between the linear and saturation region. In the non-linear region of MOSFET operation the drain current is defined by (Eq A.3)

$$I_D = \frac{W}{L}\mu_n C_{ox}\left(V_G - V_T - \frac{V_D}{2}(1 + \frac{\sqrt{\varepsilon_s q N_A}}{\sqrt{\Psi_B C_{ox}}}\right)V_D, \qquad \text{Eq A.3}$$

where ε_s is the relative permittivity of the semiconductor, N_A is carrier concentration and Ψ_B is the difference between the Fermi level and intrinsic Fermi level.

The I_D in the linear and saturation region increases with increasing (V_G – V_T) from Eq A.1 and Eq A.2, respectively, as shown in Figure A.1(a).

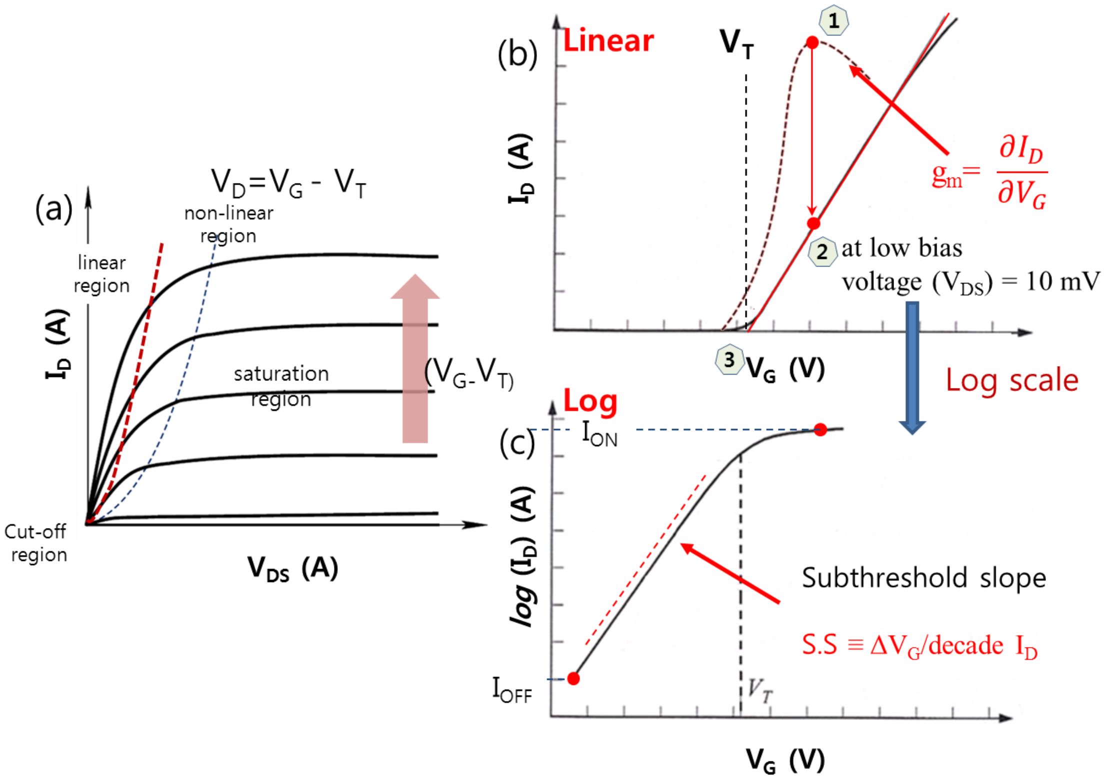

Figure A.1 (a) Output (I_D-V_{DS}) characteristic and (b) linear scale and (c) logarithmic scale representation of the I_{DS} versus V_G in common MOSFET.

The I_D-V_G curve in Figure A.1(b) called transfer characteristic is one of the most basic but important properties. From transfer characteristics, many important FET parameters such as threshold voltage, subthreshold swing, mobility, $I_{ON/OFF}$ ratio can be extracted.

◈ Transfer (I_D-V_G) characteristic of MOSFET

- Transconductance (g_m)

The transconductance (g_m) of the MOSFET, which is closely related to the gain of the transistor, is defined as Eq A.4:

$$g_m = \frac{dI_D}{dV_G} = \frac{W}{L}\mu_{eff}C_{ox}V_D, \qquad \text{Eq A.4}$$

,where μ_{eff} is the effective carrier mobility, C_{ox} is the coupling capacitance and L is the channel length. it is specified in unit of $[\Omega^{-1}]$ or [S]. g_m (which is the first derivatives of the I-V curves) is plotted as a red dot in Figure A.1(b). A high transconductance means that the gate voltage has a large effect on the channel conductance and thus the output current; a small change in V_G induces a large change in $I_{D.}$

- Threshold voltage (V_T)

Threshold voltage (V_T) is an important parameter for the device characteristic of FET. V_T is defined as the minimum gate voltage required to switch-on the transistor. Various extraction methods of V_T exist because transfer characteristic near V_T is nonlinear due to diode like drain current behavior below sub-threshold region. Among the various extraction methods, linear extrapolation is commonly used for the extraction of V_T. After finding the point of maximum slope on the I_D-V_G curve (which is the maximum value of transconductance (Figure A.1(b)-(1))), linear extrapolation to I_D=0 at (Figure A.1(b)-(3)) is carried out from linear fitting to I_D-V_G curve at that point (Figure A.1(b)-(2)).

- $I_{ON/OFF}$ ratio

The most simple and common used to determine the $I_{ON}/_{OFF}$ ration is simply take the maximum value of the current on a graph I_{DS}(or log(I_{DS}))-V_{GS} for I_{ON} and its value minimum for I_{OFF} (Figure A.1(c)). The ON-state current (I_{ON}) determines the FET switching speed, whereas an OFF-state current (I_{OFF}) determines the passive power consumed by a logic gate. Therefore, I_{OFF} level should be as low as possible in order to minimize power consumption of the devices at the OFF-state.

- Subthreshold slope (S. S.)

Another important parameter used to describe the behavior of transistors is the subthreshold slope. The drain current in the MOSFET rapidly approach to zero below the threshold voltage (V_T) on a linear scale, as shown in Figure A.1(b). However, the drain current remains non-negligible level even below the threshold voltage (which is called subthreshold region) on a logarithmic scale. Due to the exponential behavior of subthreshold drain current, it has linearity in the semi-log plot of transfer characteristics (log(I_D) – V_G)). Log I_{DS} increases linearly with gate bias (V_G) up to V_T (Figure A.1(c)). The subthreshold slope (S.S.), which gives the percent variation of the drain current as a function of the gate voltage in weak inversion, is defined as (Eq A.5) [i]:

$$S.S. \equiv \frac{dV_G}{d(\log I_D)} = \ln(10)\frac{kT}{q}(1+\frac{C_d}{C_{ox}}) \qquad \text{Eq A.5}$$

where k is a Boltzmann's constant, T is temperature, q is an electronic charge, C_d is depletion layer capacitance, C_{ox} is gate-oxide capacitance. Low S.S. (steep slope in log(I_D) – V_G curve) has better gate control. The lowest value of S.S. is 60 mV/decade at room temperature for planar MOSFET.

- Mobility of MOSFET

Carrier mobility (μ) represents how quickly carriers can move in the channel when an electric field (E) is

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[i] S. M. Sze, Physics of Semiconductor Devices (chapter 6.2.4): New York: Wiley, 3rd ed, 2007.

given. When an electric field E is applied across the conductor, electrons (or holes) begin to move with an average velocity which is named the drift velocity (v_d). So, the electron mobility μ is defined as (Eq A.6), and it is specified in unit of [$cm^2 \cdot V^{-1}s^{-1}$].

$$v_d = \mu \cdot E \qquad \text{Eq A.6}$$

The definition of field-effect mobility in MOSFET is given by (Eq A.7)

$$\mu_{FE} = \frac{Lg_m}{WC_{ox}V_{DS}}, \qquad \text{Eq A.7}$$

Appendix A2

▣ Electrical characterization of SiC nanoFET

◈ Mobility of nanoFET

In case of nanoFET, mobility (μ) can be expressed as (Eq A.8) from the relationship of Eq A.4,

$$\mu = \frac{g_m \cdot L^2}{C_{ox} \cdot V_{DS}} \qquad \text{Eq A.8}$$

In case of 1D structure, the gate capacitance (C_{ox}) is in the order of femto(10^{-15})-Farad (fF), therefore it is difficult to be experimentally measured. It can be estimated by an approximated “metallic cylinder on an infinite metal plate model” [ii]. The cross section geometry and the equipotential lines of this model are depicted in Figure A.2(a).

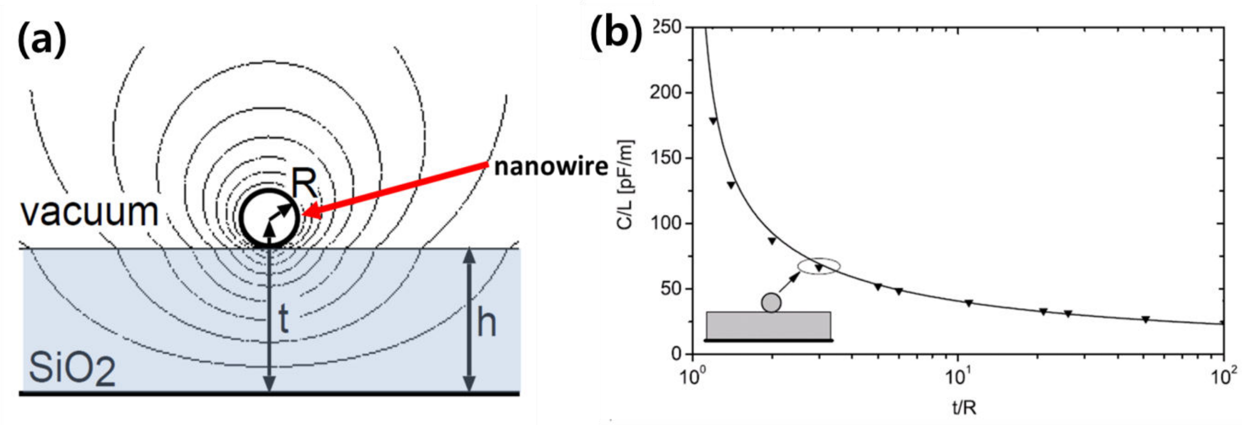

Figure A.2 (a) Cross section geometry of back-gated NWFET to calculate the capacitance of NW with equipotential lines, (b) gate capacitances with SiO_2 gate dielectric versus t/R. [ii].

The model yields an analytical equation for the gate capacitance per unit length (Eq A.9).

$$C_{ox} = \frac{2\pi\varepsilon\varepsilon_o L}{\cosh^{-1}(\frac{t}{R})}, \qquad \text{Eq A.9}$$

where ε_o is the dielectric constant, R is the radius of NW, t is the distance between the metal plate and the center of the NW. For x = t/R >>1, the approximation $\cosh^{-1}(x) = \ln(x + \sqrt{x^2 - 1}) \approx \ln(2x)$ can be used (Eq A.10).

$$C'_{ox} = \frac{2\pi\varepsilon\varepsilon_o L}{\ln(2t/R)}, \qquad \text{Eq A.10}$$

[ii] Olaf Wunnicke, Gate capacitance of back-gated nanowire field-effect transistors, Appl. Phys. Lett.89, 083102 (2006)

When the radius of NW (R) is constant, the gate capacitance per unit length (C/L) increases with decreasing the gate oxide thickness.

Figure A.3 shows our simulation results (by FlexPDE[iii] program) of an equipotential distribution with back-gated square NWFET (20×20 nm^2) at different gate oxide thickness. The denser the equipotential lines around the NW are, the easier it is to induce the gate electric field in the NW channel.

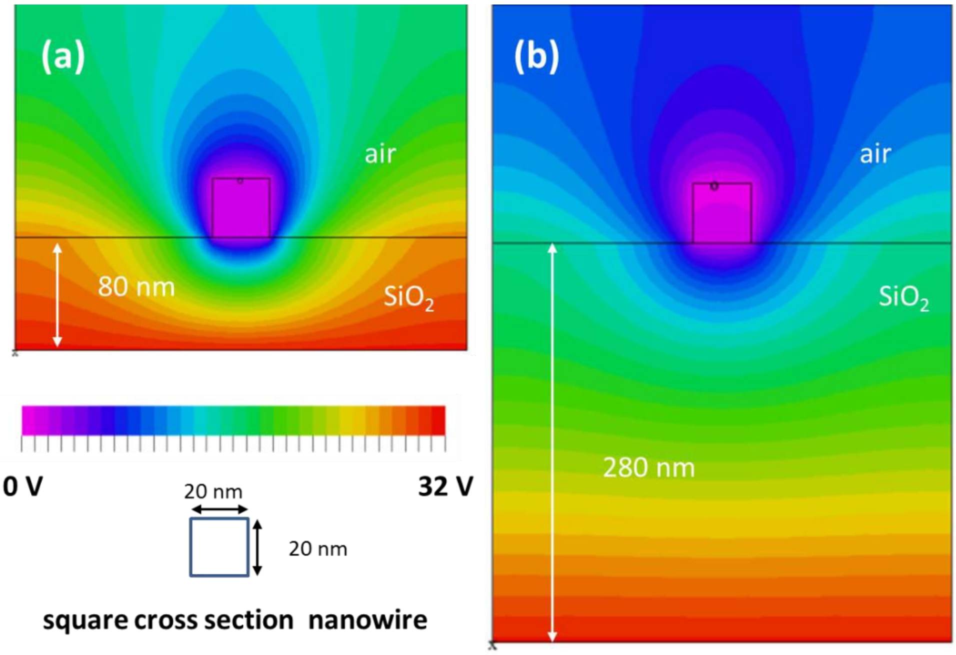

Figure A.3 Simulated equipotential distribution of back-gated NWFET with different gate oxide thickness: (a) 80 nm and (b) 280 nm

In our study of SiC NPFET, the gate oxide (SiO_2) thickness is further reduced down from 280 nm (in case of SiC NWFET) to 80 nm to increase the gate capacitance and gate controllability.

◈ Output characteristics (I_{DS}-V_{DS}) of SiC nanoFET

From the output characteristics of SiC nanoFET, the rectifying (Schottky-like) or ohmic contact can be identified, as shown in Figure A.4(a-b). The linear behavior of I_{DS}-V_{DS} curves in Figure A.4(a) demonstrates an ohmic contact between the SiC nanostructure and the metal electrodes. The resistivity (ρ) of SiC nanoFET can be calculated from the output characteristics (I_{DS}-V_{DS}) by the following equation (Eq A.11).

$$\rho \equiv \mathrm{R}\frac{\mathrm{S}}{\mathrm{L}} = \frac{\mathrm{V_{DS}}\pi r^2}{I_{\mathrm{DS}}\, L}, \qquad \text{Eq A.11}$$

where R is the resistance of SiC nanostructure, S its section, L its channel length of the NP and r is the NP radius.

[iii] FlexPDE; http://www.pdesolutions.com/

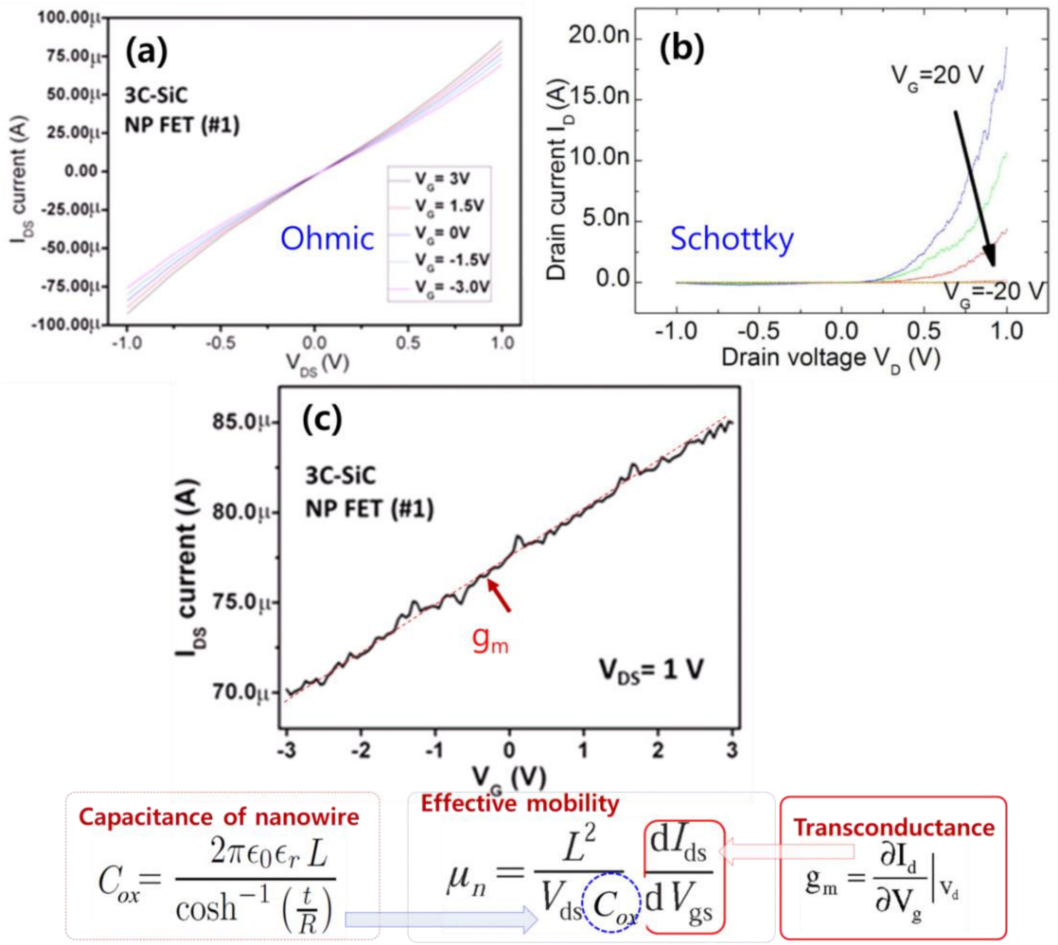

Figure A.4 Output characteristic (I_{DS}-V_{DS}) of SiC nanoFET with different contacts behavior; (a) ohmic and (b) Schottky contact [iv], (b) transfer characteristic (I_{DS}-V_G) of SiC nanoFET.

◈ Transfer characteristics (I_{DS}-V_G) of SiC nanoFET

From the transfer characteristics of SiC nanoFET, several parameters could be extracted, such as carrier mobility, transconductance, $I_{ON/OFF}$ ratio, threshold voltage and subthreshold slope etc. However, the device switching OFF is not achievable in our SiC nanoFET, as shown in Figure A.4(c). Therefore, several parameters ($I_{ON/OFF}$ ratio, threshold voltage and subthreshold) couldn't have been extracted. g_m of SiC nanoFET can be calculated from the I_{DS}-V_G curve of SiC nanoFET using Eq A.4: The capacitance (C_g) of SiC nanoFET can be estimated from Eq A.10. Based on the calculated g_m and estimated capacitance, the effective electron mobility of SiC nanoFET can be extracted from Eq A.8.

[iv] K. Rogdakis, E. Bano, L. Montes, M. Bechelany, D. Cornu, and K. Zekentes, "Rectifying Source and Drain Contacts for Effective Carrier Transport Modulation of Extremely Doped SiC Nanowire FETs", IEEE Transactions On Nanotechnology **10** (2011) 980.

Appendix A3

▣ Configuration of Four-point probe method

Ohm's law (V=IR) is used in order to determine a resistance, which is calculated by dividing the measured voltage by the sourced current. However, when the device is measured by using a two-probe setup, the voltage is measured not only across the devices (R_{NW}), but also includes the resistance of the contacts (R_{C2} and R_{C3}), as illustrated in Figure A.5(a). These added resistances are usually not a problem when using an ohmmeter to measure resistances above a few ohms [v]. However, if measuring low resistances (e. g. R_{NW}) or contact resistance (R_{C2} and R_{C3}) may be high, two-probe setup could be a problem.

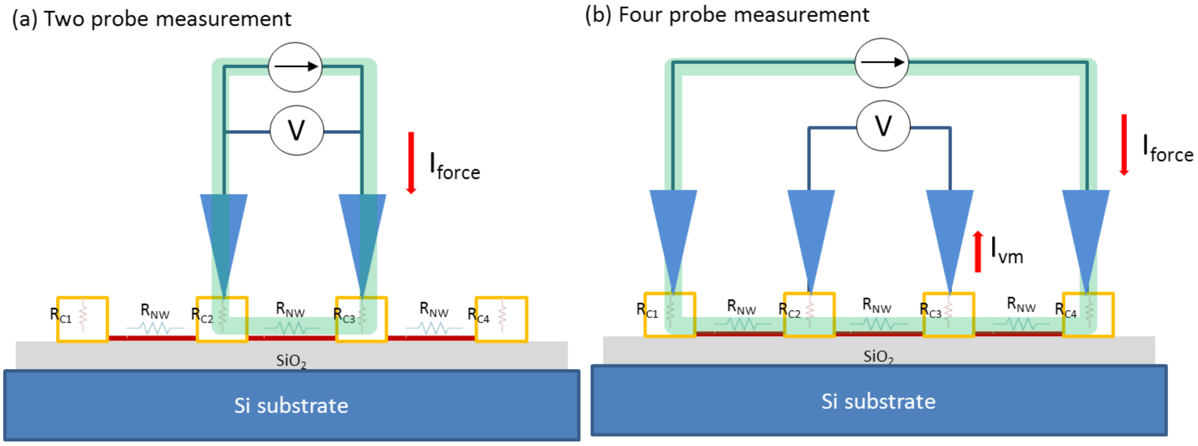

Figure A.5 Schematic illustrations of (a) two-probe and (b) four-probe measurement [v].

When measuring the $I_{1\text{-}4}$-$V_{2\text{-}3}$ using four-probe measurement, a current ($I_{1\text{-}4}$) flows across the outer leads and voltage $V_{2\text{-}3}$ is measured across the inner leads, as shown in Figure A.5(b). Second set of probes (probe 2 and 3) are used for sensing only the voltage drop across the device, because negligible current flows (I_{VM}=0) in these probes due to high input impedance ($>10^{16}$ Ω) of voltmeter. Therefore, four-probe configuration eliminates measurement errors due to the probe resistance or the contact resistance between each metal probe and the semiconductor material. As a result, exact channel resistance measurement can be achieved.

Figure A.6 shows the setup configuration of model 4200-SCS for the four-probe measurement. Second set of probes (probe 2 and 3) are defined as high impedance voltmeter with "zero" current on 1 nA range. The voltage difference between SMU2 and SMU3 are measured.

Figure A.7 shows total resistance (R_{tot}) of SiC NWFET, which consist of the contact (R_C) and the channel (R_{NW}) resistance. The total NW FET resistance (R_{tot}) can be extracted from the $I_{2\text{-}3}$-$V_{2\text{-}3}$ curve, which is defined as the zero-bias slope of the inverse of the I-V dependence. The channel resistance (R_{NW}) is evaluated from the slope of the $V_{2\text{-}3}$-$I_{2\text{-}3}$ curve.

The contact resistance (R_C) is calculated by the following equation; $R_C = (R_{tot} - R_{NW})/2$. Detail experimental results are presented in section 4.3.2.

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[v] Keithley, application note series, "Four-Probe Resistivity and Hall Voltage Measurements with the Model 4200-SCS"

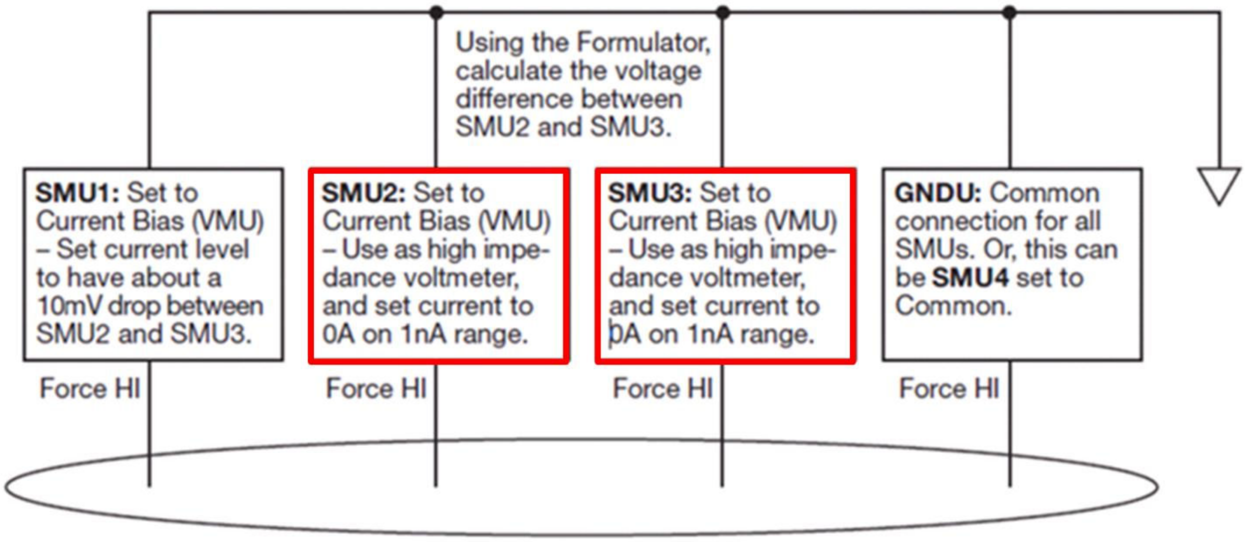

Figure A.6 SMU designation for four-point probe measurement.

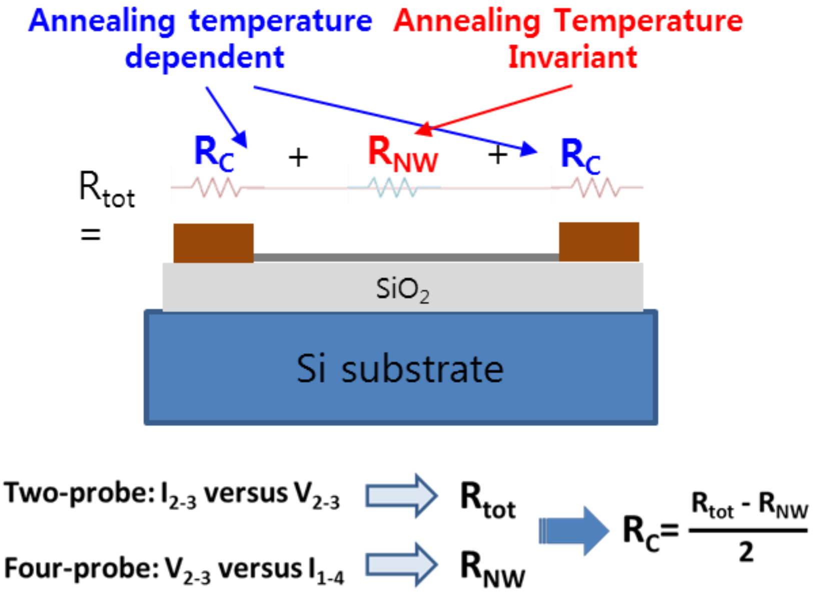

Figure A.7 The contact (R_C) and the channel (R_{NW}) resistance of a SiC NWFET.

French thesis summary

(Résumé de la thèse française)

Nanofils en carbure de silicium:
De la fabrication jusqu'aux dispositifs électroniques

Jihoon CHOI

Introduction générale

Les nanostructures semi-conductrices à une dimension (comme les nanofils, nanobâtonnets et nanotubes) sont devenus l'objet de recherches intensives pour explorer de nouveaux phénomènes émergents à l'échelle nanométrique et sonder leur possible utilisation dans l'électronique du futur.

Parmi ces nanofils (NFs) semi-conducteurs, le carbure de silicium (SiC) possède des propriétés très particulières, comme une large bande interdite, une excellente conductivité thermique, un champ électrique de claquage très élevé, une grande inertie chimique, une mobilité des électrons élevée et enfin le SiC est biocompatible. Ces facteurs font du SiC un candidat de choix pour remplacer le silicium dans des dispositifs électroniques spécifiques fonctionnant dans des conditions extrêmes (à haute température, haute puissances ou hautes fréquences) ou dans des environnements hostiles.

La synthèse des nanostructures en SiC par des voies ascendantes sont étudiées depuis la dernière décennie, toutefois les nanofils en SiC obtenus présentent une forte densité de défauts structuraux tels que des fautes d'empilement. Ce type de défauts accompagné d'un dopage non contrôlé dans ces nanofils conduisent à une mauvaise performance électrique des transistors à base de nanofils SiC (comme le faible effet de grille et une faible mobilité). Par conséquent, il est nécessaire de développer des nanostructures de SiC avec une faible densité de défauts structuraux en utilisant une autre méthode, comme la voie descendante (appellée « top-down »).

Les principaux objectifs de cette thèse sont divisés en trois parties principales.

Dans la première partie de cette thèse, nous présentons les résultats de simulation du transport électrique dans les NF-SiC. En particulier, nous avons étudié l'amélioration thermoélectrique du NF SiC par l'étude de l'interaction complexe de la taille de NF, la température et la rugosité de surface.

La deuxième partie de la thèse est consacrée à la fabrication de nanostructures de SiC de haute qualité avec un niveau de dopage contrôlé. Nous avons développé une technique de fabrication par gravure plasma afin d'obtenir des nanopiliers en SiC (NPs) à l'échelle nanométrique. Le comportement de gravure des NPs a été étudié en fonction de différentes polytypes (3C, 4H et 6H) et différentes orientations cristallographiques.

La dernière partie de la thèse est consacrée à la conception et à la caractérisation électrique de nano-dispositifs SiC. Pour étudier les propriétés électriques des nanostructures de SiC, deux types différents de transistors à effet de champ appelées nanoFETs (Field Effect Transistors) en SiC (NFFET et NPFET) ont été fabriqués en utilisant des NFs SiC et les NPs SiC préparés par les deux approches ascendante et descendante, respectivement.

Enfin, le résumé de nos différentes conclusions accompagné d'une discussion sur les futures orientations possibles clôturent le manuscrit.

Partie I: Modélisation du transport électrique dans les transistors à nanofil en SuC

En tant que matériau massif, le SiC est un mauvais matériau thermoélectrique en raison de sa forte conductivité thermique (330 $W \cdot m^{-1}K^{-1}$) [1]. Cependant, les structures quasi-unidimensionnels, tels que les nanofils sont théoriquement prédites par Hicks et Dresselhaus pour avoir un meilleur facteur de mérite [2].

Dans ce travail, nous allons modéliser les propriétés thermoélectriques des NFs SiC avec des sections transversales carrées dans le régime balistique à haute température (~ 600 K), basé sur le non-équilibre dynamique moléculaire classique et les fonctions de Green pour le transport thermique et le transport de courant.

a. Simulation des propriétés thermoélectriques de nanofils de SiC

L'efficacité d'un dispositif thermoélectrique est fortement dépendante du facteur thermoélectrique de mérite noté ZT :

$$\mathrm{ZT} = \frac{TS^2G}{\kappa_e + \kappa_{ph}} \qquad \text{Eq. 1}$$

où T est la température [K], S est le coefficient de Seebeck [V/K], G est la conductance électrique [Ω^{-1}], et κ est la conductance thermique [W/K] de l'électron (κ_e) et des phonons (κ_l). En particulier, le numérateur de Z (S^2G) est appelé facteur de puissance et définit les performances électriques des matériaux thermoélectriques. La conductance des NF-SiC, coefficient de Seebeck correspondant et la conductance thermique d'électrons ont été calculées dans le cadre de la théorie quantique transport de Landauer–Büttiker [3].

La Figure 1(a) montre S, G et S^2G de SiC NF avec des sections différentes (2,05×2,05, 2,92×2,92, 4,21×4,21 nm^2) par rapport à une concentration de porteurs à 500 K. L'augmentation des NFs dans la dimension transversale conduit à la modification de sa structure de bande. Ces deux effets ont un effet délétère sur S. En conséquence, S diminue avec l'augmentation de la section transversale, tandis que G augmente en raison de l'augmentation du nombre de modes, qui contribuent au déplacement des porteurs. Le facteur de puissance est déterminé par deux facteurs concurrentiels: S et G.

La Figure 1(b) montre les coefficients thermoélectriques (S, G et S^2G) du SiC NF (2,05 × 2,05 nm^2) avec différentes températures par rapport à une concentration de porteurs à 500 K.

En théorie, le niveau de Fermi (E_F) diminue avec l'augmentation de la température. Donc, S augmente lorsque la température est élevée en raison de la diminution de l'expression (E - E_F). D'autre part, G diminue

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[1] J. Li, L. Porter, S. Yip, Atomistic modeling of finite-temperature properties of crystalline β –SiC, J. Nucl. Mater. 246 (1997) 53.

[2] L. D. Hicks, M. S. Dresselhaus, Thermolectric figure of merit of a one-dimensional conductor, Phys. Rev. B 47 (1993) 16631

[3] R. Kim, S. Datta, M. S. Lundstrom, Influence of dimensionality on thermoelectric device performance, J. Appl. Phys. 105 (2009) 034506.

avec l'augmentation de la température due à l'augmentation des diffusions de phonons acoustiques et optiques. Le S^2 augmente plus que la diminution de G lorsque la température augmente. En conséquence, le facteur de puissance augmente progressivement avec l'augmentation de la température (encart de Figure 1(b)).

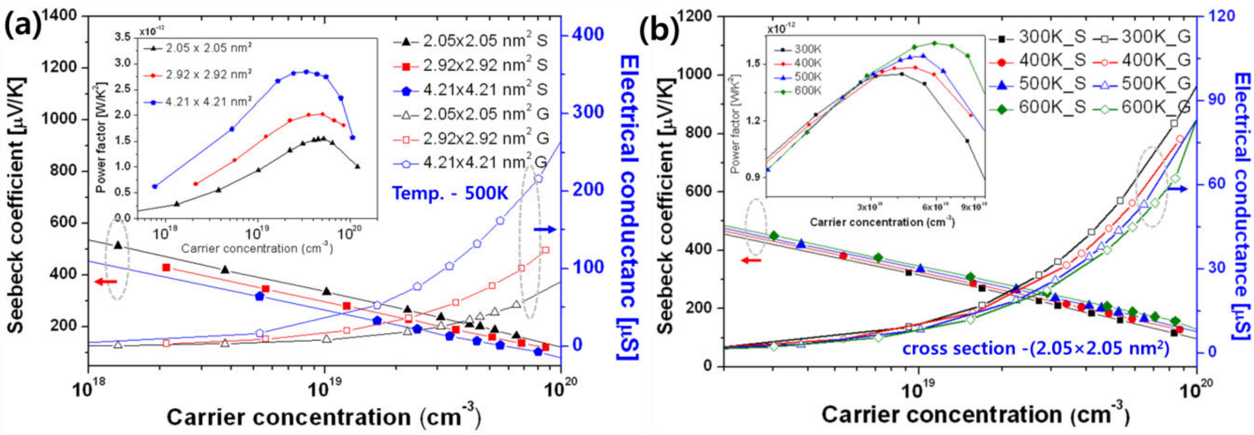

Figure 1. Coefficients de Seebeck et conductance électrique des NF SiC avec (a) des sections différentes à 500 K et (b) avec la température différente à 2,05×2,05 nm^2.

N. Papanikolaou [4] a calculé la conductivité thermique des NF-SiC à haute température (500 K) à l'aide de simulations dynamiques moléculaire hors-équilibre classiques. Les NF-SiC ayant un diamètre de 2 à 4 nm montre une conductivité thermique de 3 - 6 W·m^{-1}K^{-1} à 500K. Nous avons inclus ces résultats dans le calcul des propriétés thermoélectriques.

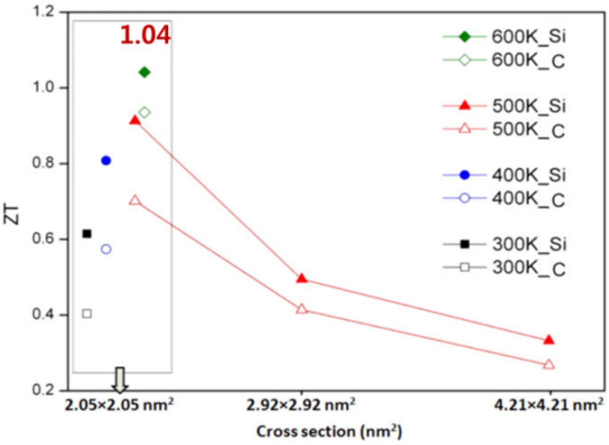

Figure 2. ZT de NF-SiC selon la section et la température avec les deux polarités possible : face Si et face C.

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[4] N Papanikolaou, Lattice thermal conductivity of SiC nanowires, J. Phys.: Condens. Matter 20 (2008) 135201

ZT augmente avec la diminution de la section transversale à 500 K. Le ZT de SiC NF pour une section de 2,05 × 2,05 nm^2 augmente avec l'augmentation de température pour atteindre une valeur de 0,93 à 1,04 à 600 K. Cette amélioration de ZT provient principalement d'une réduction drastique de la conductance thermique à travers la diffusion accrue des phonons, sans réduction significative de S et G. Parce que le calcul de la conductance thermique dépend de la surface des terminaisons, la dépendance de ZT à la surface des terminaisons de SiC NF peut être calculé quantitativement. Le ZT de NF de terminaison Si a une valeur plus grande que celle de C teminé SiC NF, en raison de la plus grande conductivité thermique [4].

ZT augmente alors que la température augmente pour une section 2,05 x 2,05 nm^2, et atteint 1 avec une terminaison Si à 600 K, ce qui est 8 fois plus grand que la plus grande valeur expérimentalement rapporté sur des films minces en SiC (0,125 à 973K) [5].

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[5] X. H. Wang, A. Yamamoto, K. Eguchi, H. Obara, and T. Yoshida, "Thermoelectric properties of SiC thick films deposited by thermal plasma physical vapor deposition," Science and Technology of Advanced Materials, vol. 4, p. 167, 2003.

Partie II: Fabrication de nanostructures en SiC par la méthode «top-down»

Pour parvenir à des performances excellentes avec des dispositifs nanoélectroniques à base de NF-SiC, tels que les transistors à effet de champ (FET), il est essentiel d'obtenir un matériau monocristallin au dopage contrôlé. Actuellement, une technique commune pour le développement de SiC NFs est l'approche «bottom-up». Le problème critique de ces méthodes est que les nanofils présentent une forte densité de défauts structuraux, tels que les fautes d'empilement, les macles et ces nanofils contiennent un dopage intrinsèque non-contrôlé (dû aux méthodes d'élaboration) très élevé.

Dans le cas contraire, une approche « top-down » peut permettre un contrôle précis de la géométrie des nanostructures, tels que le diamètre, la longueur et l'emplacement des NFs sur le substrat. Il peut surtout permettre de minimiser la densité des défauts en gravant un matériau de très bonne qualité cristalline et cela repose sur la qualité des épitaxies en SiC. La croissance massive et en couche mince ont été développées au cours des dernières années et ont montré une disponibilité commerciale des substrats de SiC de diamètre et de qualité sans cesse croissante. Par conséquent, si l'approche « top-down » est appliquée dans un substrat SiC de haute qualité, des SiC NFs hautement cristallins avec moins de densité de défauts et avec un niveau de dopage contrôlé pourraient être atteints. Les principaux intérêts de cette partie sont la réalisation de nanostructures de SiC par l'approche « top-down », en particulier, par l'utilisation de la technique de gravure du Plasma à Couplage Inductif (ICP).

Les expériences de gravure ICP ont été effectuées sur des wafers de 8 pouces de diamètre sur un équipement industriel, qui se compose d'une chambre sas situé dans une salle blanche de classe 10, une source plasma découplée à forte densité (CENTURA 5200B de chez Applied Materials Inc.). puissance de la source ICP qui fonctionne à la fréquence industrielle de 13,56 MHz est constante (1500 W) pendant le process . La polarisation du substrat variait entre 100 et 300 V, indépendamment de la puissance de la source ICP. La quantité de mélange gazeux (SF_6 et O_2) est constante (50 sccm), mais la pression du gaz et de la teneur en oxygène ont également varié, le premier entre 4 et 7 mTorr, et la seconde de 10% à 40%.

Tableau 1. Substrats de SiC utilisé dans cette étude de gravure ICP.

Polytype	Orientation	Source	Monocristallin / Hétéro-epi	Concentration de dopage	sections connexes
4H-SiC	(0001)	LMGP (France)	Monocristallin	10^{17}	II-a
4H-SiC	(0001)	Tankeblue Inc.	Monocristallin	10^{20}	II-b
6H-SiC	(0001)		Monocristallin	10^{20}	
6H-SiC	(11-20)	Dong-Eui Uni. (Korea)	Monocristallin	N/A	
3C-SiC	(001)	Linköping Uni. (Sweden)	3C-SiC epi (7µm) sur Si	$2 - 8\cdot10^{16}$	
3C-SiC	(111)		3C-SiC epi (18µm) sur 6H-SiC	$5\cdot10^{16}$	

Différents types de substrats SiC ont été utilisés pour l'étude sur le comportement en gravure en fonction de la dépendance du SiC, comme indiqué dans le Tableau 1. Les 4H-SiC et 6H-SiC orientés (0001) ont été achetés auprès Tankeblue Inc. Les substrats 6H-SiC (11-20) ont été fabriqués par la technique conventionnelle de sublimation «Physical Vapor Transport» (PVT) [6].Les couches 3C-SiC (001) et 3C-SiC (111) sont hétéro-épitaxiées sur substrat de Si (100) et homo-épitaxiées sur substrat de 6H-SiC (0001) [7].

a. Fabrication de nanostructures de SiC en optimisant les paramètres de gravure

Il est fortement conseillé de bien comprendre les paramètres du procédé afin d'obtenir un profil hautement anisotrope des nanostructures. Dans cette section, nous avons étudié plusieurs paramètres de gravure permettant d'élaborer des nanostructures de SiC par gravure ICP dans un mélange gazeux à base de SF_6/O_2.

❖ Effet des espèces de masques métalliques

Un matériau de masquage avec une haute sélectivité à l'égard du SiC lors du processus de gravure avec le SF_6/O_2 est nécessaire pour obtenir la hauteur maximale de nanopiliers SiC. Pour trouver un matériau masquant adapté pour la gravure, la gravure ICP est réalisée, pour une puissance de bobine ICP de 1500 W et un gaz de gravure (SF_6: 40 et O_2: 10 sccm), avec différentes espèces de masques métalliques (Cu, Ni et Al) pour un temps de gravure temps de 3 min.

Les nanopiliers SiC avec un masque Cu montrent une rugosité sur les flancs de la Figure 3(a). Cela peut être attribué aux produits irrégulièrements formés sur le masque. Ces produits sont formés au cours du processus de gravure par réaction avec des radicaux F ou O. Ces produits de réaction non volatils (Cu_2F ou Cu_2O) formés sur le masque présentent une grande sélectivité de la gravure et des propriétés de résistance à la pulvérisation, c'est pourquoi le Cu a été évalué comme étant le meilleur candidat en tant que matériau de masque de motif pour les appareils de SiC MEMS.

Toute fois, un masque de métal Cu n'est pas adapté pour la gravure à l'échelle nanométrique. En effet, les produits formés irrégulièrement sur le masque agissent comme un motif de masquant, et enfin, ils induisent une rugosité sur les parois latérales des piliers gravés. En outre, les produits de réaction non volatils formés à proximité de l'interface entre le masque et Cu SiC à entraine de faibles forces d'adhérence du masque Cu sur la surface de SiC. Par conséquent, le masque Cu est parfois détaché de la surface SiC pendant le processus de gravure, comme indiqué par les flèches dans la Figure 3(d).

De plus, nos résultats montrent que les piliers de SiC avec un masque Al présentent une rugosité plus élevée

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[6] I. G. Yeo, W. S. Yang, J. H. Park, H. B. Ryu, W. J. Lee, B. C. Shin, and S. Nishino, "Two-inch a-plane (11-20) 6H-SiC Crystal Grown by Using the PVT Method from a Small Rectangular Substrate," Journal of the Korean Physical Society, vol. 58, pp. 1541-1544, 2011.

[7] J. W. Sun, I. G. Ivanov, R. Liljedahl, R. Yakimova, and M. Syvajarvi, "Considerably long carrier lifetimes in high-quality 3C-SiC(111)," Applied Physics Letters, vol. 100, pp. 252101-5, 2012.

sur les flancs que celle avec un masque Cu suivant la direction verticale Figure 3(c). Cela pourrait être dû à la détérioration du masque par le bombardement ionique énergique.

Le masque de Ni est suffisamment résistant au « sputter » pour protéger le SiC sous le masque, sans la formation d'une couche irrégulière de métal de fluorure non volatile. Par conséquent, le profil de gravure des nanopiliers de SiC avec un masque Ni montre une surface de flanc nette du nanopilier avec une forme de masque uniforme Figure 3(b).

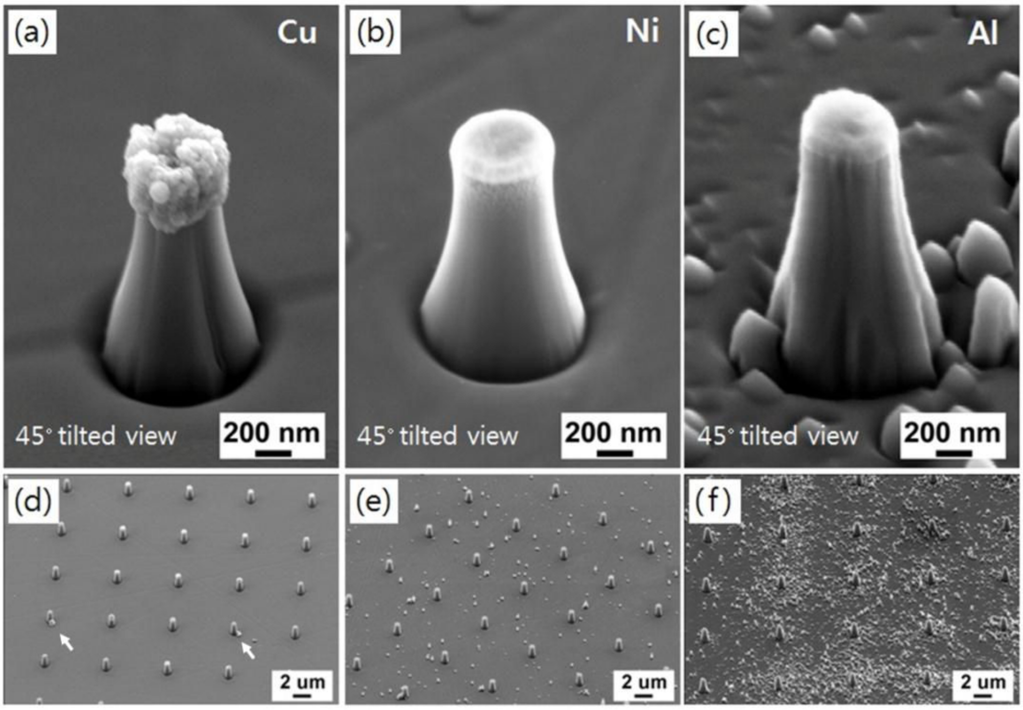

Figure 3. Images MEB de nanopiliers avec des masques métalliques;
(a, d) Cu, (b, e) Ni, and (c, f) Al metal mask (45˚ tilted view).

L'effet de micromasquage diminue suivant l'ordre: Al, Ni et Cu (voir la Figure 3(d)–(f)), cet ordre est l'inverse de celui de la résistance à la pulvérisation des matériaux (Cu> Ni> Al). Sur la base de ces résultats, Ni est choisi comme matériau de masque pour la gravure de nanopiliers en raison de la surface nette des parois latérales et de la densité relativement faible de micromasquagev.

❖ Effet du rapport de concentration SF_6/O_2

Le comportement de la gravure dépend fortement de la composition des gaz de gravure. Particulièrement, dans le cas du plasma SF_6, la concentration en O_2 est connu pour influencer le profil des nanopiliers de SiC, tels que l'anisotropie, la netteté de la surface, la sélectivité du masque métallique et le taux de gravure en contrôlant la densité des fluors.

La hauteur du pilier augmente initialement avec la concentration en O_2, et atteint une valeur maximale de 1,58 ± 0,02 um à environ 20% de la concentration en O_2. Puis, elle diminue avec l'augmentation de la concentration en O_2, comme représenté sur la Figure 4. Le rapport d'aspect présente une valeur maximale de 2,4 ± 0,02 à 20% de la concentration en O_2.

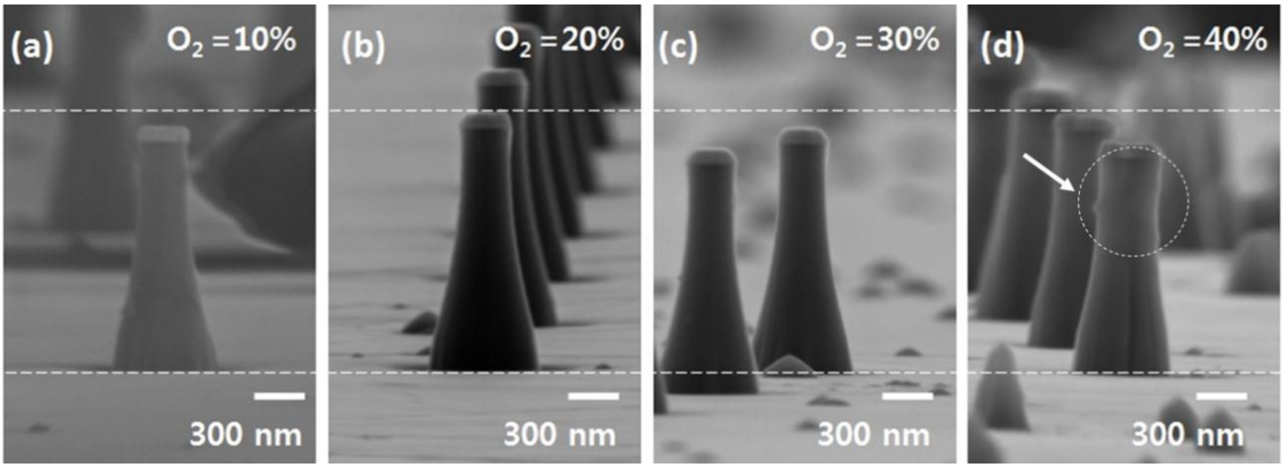

Figure 4. Images MEB vues latérales de nanopiliers à différentes concentrations d'O_2; (a) 10%, (b) 20%, (c) 30% and (d) 40%.

La présence d'un niveau approprié d'O_2 (20%) pemet de garder une forte concentration en radicaux de fluor (F), qui est responsable de la gravure du SiC par la réaction avec les liaisons CF_n et SF_n insaturées de ce fait les radicaux F ne se combinent pas avec eux. En outre, les radicaux F du plasma gravent préférentiellement le Si plutôt que C [8]. En conséquence, une couche riche en carbone est formée sur le substrat de SiC, ce qui est l'un des facteurs limitant pour la gravure de SiC. L'ajout d'O_2 fournit la force motrice pour enlever le carbone en formant des produits de gravure volatils, tels que CO, CO_2 et CF_2. Par conséquent, ces deux facteurs sont censés contribuer à l'augmentation de la vitesse de gravure. Toutefois, outre l'addition d'oxygène diminue la vitesse de gravure en raison de la dilution de la concentration de F. A une concentration optimale O_2 (20%), le ratio d'aspect élevé de SiC nanopilier ont été atteints grâce à l'équilibre entre l'attaque par F radicaux et le dépôt par les radicaux O.

❖ Evolution du profil de gravure en fonction du temps de gravure

Le comportement de la gravure de nanopilier de SiC a été étudiée en fonction du temps de gravure, non seulement pour obtenir des nanopiliers de SiC plu hauts, mais aussi pour surveiller les paramètres caractéristiques de gravure, comme la taille du masque, l'épaisseur du masque et de la hauteur du pilier.

Figure 5(a-d) montre la morphologie des nanopiliers de SiC gravés en fonction du temps de gravure à la concentration optimale O_2 (20%) et une tension de polarisation de 150 V. La hauteur des nanopiliers de SiC augmentent en fonction du temps de gravure. Pour l'analyse quantitative, la taille du masque, l'épaisseur du

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[8] N. O. V. Plank, M. A. Blauw, E. W. J. M. van der Drift, and R. Cheung, "The etching of silicon carbide in inductively coupled SF_6 /O_2 plasma," Journal of Physics D: Applied Physics, vol. 36, p. 482, 2003.

masque et de la hauteur du pilier sont tracés en fonction du temps de gravure, comme représenté sur la Figure 5(e).

Le ratio d'aspect (H/D) des piliers augmente avec le temps de gravure (voir Figure 5(e)). Le maximum obtenu est de 6,45 à 840 sec. Une longue durée de gravure conduit à une grande profondeur de gravure avec une anisotropie élevée, mais il donne aussi un profil de gravure amoindri à 840 sec (voir Figure 5(d)), en raison d'une attaque chimique élevée par exposition directe aux adicaux F du plasma. Le diamètre minimum des piliers gravés à 840 sec peut être réduit à moins de 100 nm à cuase de la combinaison des phénomènes d'érosion du masque et d'amoindrissement du diamètre. La longueur de ces piliers (de diamètre inférieur à 100nm) est d'environ 1,5 um, ce qui est assez long pour la fabrication de nanoFET.

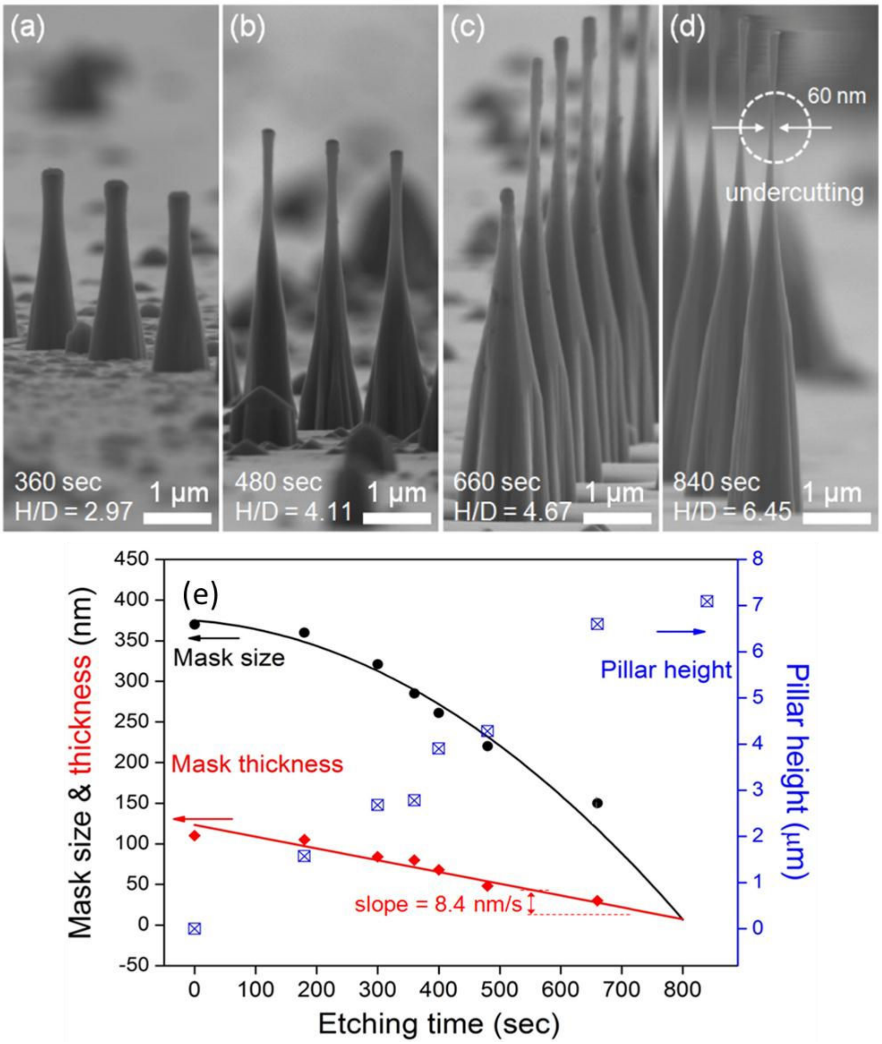

Figure 5. Images MEB de nanopiliers de SiC avec un temps de gravure différent; (a) 360 sec (b) 480 sec, (c) 660 sec, (d) 840 sec, (e) Courbes de la taille du masque, de l'épaisseur du masque, et de la hauteur pillier en fonction du temps de gravure.

Le taux de gravure est calculé par la hauteur de la colonne au cours du temps de gravure. Il reste à peu près constant (550 nm/min) lors de la gravure, et ensuite commence à décroître légèrement (165 nm/min) durant la période comprise entre 660 et 840 sec lorsque le masque de métal acomplètement disparu. La sélectivité de la gravure des matériaux de masque (Ni) par rapport au SiC est d'environ 65. L'épaisseur du masque au centre est réduit linéairement en fonction du temps voir Figure 5(e).

b. Étude morphologique des nanopiliers de SiC selon les polytypes et les orientations du cristal

Nous avons également étudié le comportement de la gravure de nanostructures de SiC selon les polytypes et les orientations cristallographiques.

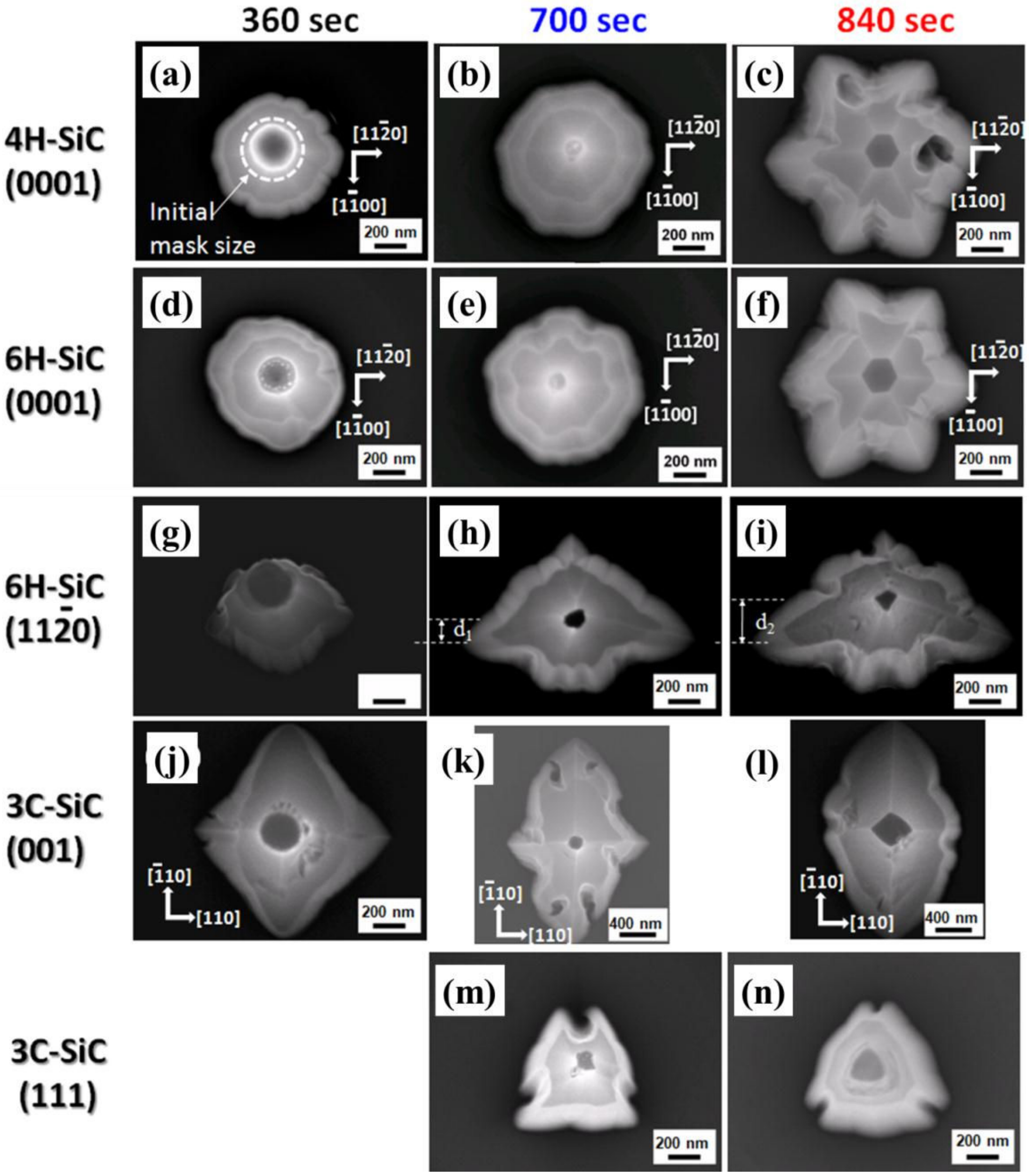

Figure 6. Vue du haut: images d'un nanopilier de SiC au MEB après la gravure durant (a, d, g, j) 360 sec, (b, e, h, k, m) 700 sec et (c, f, i, l, n) 840 sec avec différents polytypes et orientations cristallographiques. (a-c) 4H-

SiC (0001) sur l'axe, (d-f) 6H-SiC (0001) sur l'axe, (g-i) 6H-SiC (11-20) mal orienté vers [0001], (j-l) 3C-SiC (001) et (m, n) 3C-SiC (111).

La Figure 6 montre en vue de dessus les images prises au MEB des nanopiliers de SiC gravés avec différents polytypes et orientations cristallographiques, après l'attaque pendant 360 sec, 700 sec et 840 sec, respectivement. La taille et l'épaisseur du masque diminuent considérablement pendant le processus de gravure à cause d'une forte pulvérisation cathodique d'ions énergétiques, et il a complètement disparu après l'attaque pendant 840 sec. Par conséquent, les nanopiliers de SiC ne sont plus protégés par le masque après une longue gravure et commencent à être gravés à leur tour. De cette façon, leur section transversale, perpendiculaire à l'axe z du pilier de SiC, est clairement apparent (voir eles vues de dessus des Figure 6 (c), (f), (i), (l) et (n)).

La gravure continue dans un plasma de SF_6/O_2 sur les substrats 4H-SiC et 6H-SiC (0001) entraine un début de transformation du pilier en une symétrie hexagonale. Cette symétrie provient, de la structure cristallographique α-SiC. Les substrats « on-axis » (0001) 6H-SiC et 4H-SiC montrent exactement le même comportement lors de la gravure. Dans les deux cas, une arête de l'hexagone est parallèle à la direction <11-20> de l'α-SiC.

La morphologie des nanopiliers de SiC gravés sur substrat de 6H-SiC (11-20) présente une forme de pilier asymétrique au début de la gravure (Figure 6(g)), ensuite la gravure fait apparaitre des piliers avec une structure pyramidale avec une base pentagonale déformée (Figure 6(h,i)). Cette morphologie unique est liée à la légère désorientation du substrat initial suivant les directions [0001] [6].

Les nanopiliers de SiC gravés sur le substrat de 3C-SiC (001) se transforment peu à peu en une structure pyramidale en losange (Figure 6(j)-(l)). Les deux diagonales du losange correspondent aux directions [-110] et [110]. La facette apparaissant sur le haut du nanopilier de 3C-SiC (001) montre clairement une forme de losange (Figure 6(l)). Les faces polaires (Faces C et Si) du nanopilier 3C-SiC (001) pourraient être la raison de la structure en forme de losange.

La morphologie des nanopiliers de SiC gravés sur le substrat de 3C-SiC (111) présente une forme de pilier triangulaire après la gravure (Figure 6(m) and (n)) . Ce qui révèle le plan équivalent {111}, qui est le plan le plus dense du SiC phase (ou la furface de plus faible énergie libre).

Effet de différents polytypes (4H-, 6H et 3C-SiC) et orientations cristallographiques ((0001) et (11-20) de 6H-SiC, (001) et (111) de 3C-SiC) ont été étudiés dans le but de réaliser des nanopiliers SiC. Des structures de pilier à base hexagonale, losange et triangulaire ont été obtenues en utilisant les substrats α-SiC (0001), 3C-SiC (001) et 3C-SiC (111), respectivement. La morphologie des nanopiliers de SiC gravés a montré des caractéristiques intéressantes en fonction des polytypes et des orientations cristallines.

Partie III: SiC nanoFETs

Pour atteindre une excellente performance de nano-dispositifs électroniques en SiC, il est nécessaire d'améliorer trois problèmes principaux: En premier: le contact ohmique du métal sur le nanoFET, en deuxième: la mauvaise qualité du SiC NF associé aux défaut structuraux et au dopage involontaire de type n, en dernier: l'interface NF (ou NP) - grille d'oxyde. Pour répondre à ces questions, deux types de SiC nanoFETs (SiC NFFET et SiC NPFET) ont été fabriqués et caractérisés.

a. Propriétés de contact ohmique de SiC nanofil FET

Comme la taille des devices est réduite aux alentours du nanomètre, la résistance du canal de NFs devient suffisamment faible. Par conséquent, les propriétés du contact source/drain (S/D) deviennent un facteur dominant dans la détermination de la performance du device. Jang et al. [9]ont montré que les contacts ohmiques du Ni/Au sur SiC NFs ont des résistances de contact spécifiques inférieures aux valeurs de contacts ohmiques du Ti/Au. Toutefois, la propriété de contact du SiC NFFET n'a pas été étudié très en détail par rapport à celui de Si NFFET. Il est bien connu que les contacts ohmiques à base de Ni sur le SiC sont améliorés avec une optimisation du recuit pour former des phases de nickel-siliciure. Par conséquent, notre objectif était d'effectuer une étude d'optimisation du recuit pour former ces phases à faible résistance de contact.

Un SiC NFFET device, avec une configuration de sonde à quatre points, a été réalisé pour étudier la résistivité électrique et les propriétés du contact. L'étape de recuit est effectuée dans la plage de 500 à 750 °C pendant 30 sec dans une ambiance de N_2 dans de recuit thermique rapide (Jetfirst 100). Le rampe de température a été fixée pour atteindre la température souhaitée en 30 sec. Ensuite, les propriétés électriques des devices ont été mesurées à température ambiante et air ambiant avec un système de caractérisation de Keithley 4200 semi-conducteur.

Figure 7(a-b) montre les courbes de $I_{2\text{-}3}$-$V_{2\text{-}3}$ mesurés sur les électrodes internes en tant que fonction de la température de recuit pour différents courants. Lorsque l'on mesure $I_{2\text{-}3}$-$V_{2\text{-}3}$ en utilisant deux sondes de mesure, la tension ne se mesure pas seulement à travers la résistance du canal, mais comprend également la résistance des contacts (voir l'annexe A3 - Figure A.5). Par conséquent, la résistance totale de NFFET (R_{tot}) peut être extraite de la courbe $I_{2\text{-}3}$-$V_{2\text{-}3}$, qui est défini comme la pente nulle de la polarisation inverse de la dépendance I-V.

Le courant ($I_{2\text{-}3}$) augmente avec la température de recuit (Figure 7(a-b)), ce qui signifie la diminution de la résistance totale du NF (R_{tot}). Les courbes $I_{2\text{-}3}$-$V_{2\text{-}3}$ pour une temperature de recuit inférieure à 650 °C

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[9] C.-O. Jang, T.-H. Kim, S.-Y. Lee, D.-J. Kim, and S.-K Lee, "Low-resistance ohmic contacts to SiC nanowires and their applications to field-effect transistors," Nanotechnology, vol. 19, p. 345203, 2008.

montreent un faible niveau de courant et un comportement non-ohmique (Figure 7(a)), par contre le SiC NFFET pour une tmpérature de recuit de 650 °C présente un contact ohmique avec un comportement linéaire de I_{2-3}-V_{2-3} (Figure 7(b)). Le niveau du courant du SiC NFFET après le recuit à 650 °C augmente jusqu'à 100 nA. Le NFFET SiC après le recuit à 700 °C indique le niveau de courant maximum de 1 mA dans la Figure 7(c). Un courrant elevé de SiC NFFET est originaire de l'entièrement convertie Ni siliciurée SiC NF par l'intrusion de Ni.

La résistance totale (R_{tot}) évaluée par la mesure des deux sondes est respsectivement de 11,56 MΩ et 1 kΩ à 650 °C et 700 °C. Notez que, le courant de SiC NFFET après un recuit à 750 °C ne peut pas être mesurée, car SiC NF est rompu en raison de l'intrusion de Ni.

La résistance totale du NFFET (R_{tot}) se compose de la résistance de canal (R_{NF}) et de deux résistances de contact (R_C) à S/D. La résistance de canal (R_{NF}) est évaluée en utilisant quatre sondes de mesure par balayage d'un courant I_{1-4} travers les conducteurs extérieurs et par la mesure de la tension V_{2-3} travers les conducteurs intérieurs. Par conséquent, la pente de la courbe I_{1-4}-V_{2-3} indique que la résistance de canal (R_{NF}). La résistance de canal (R_{NF}) évaluée par la mesure de quatre sondes est respectivement de 10,80 MΩ et 740 Ω à 650 °C et 700 °C tel qu'indiqué sur la Figure 7(c).

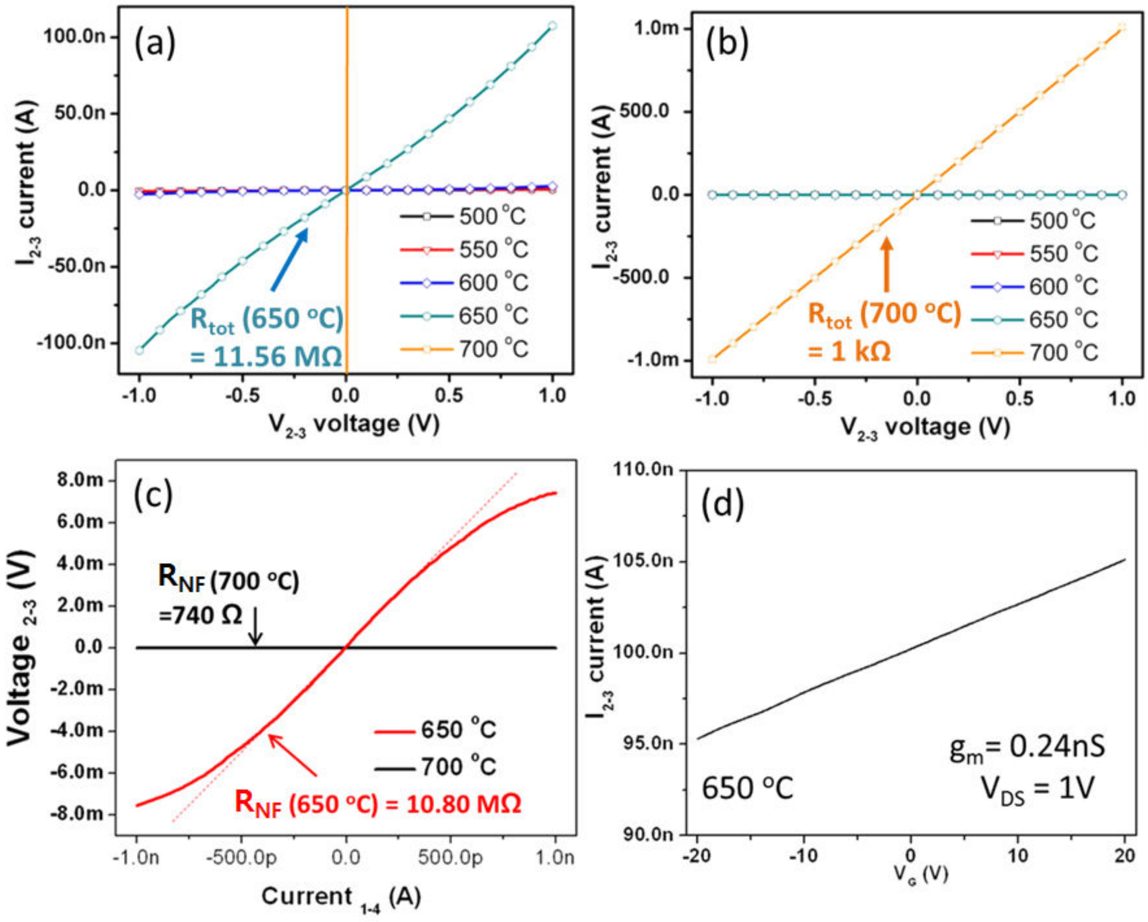

Figure 7. (a-b) Les courbes I_{2-3}-V_{2-3} mesurées sur les électrodes internes en fonction de la température de

recuit pour différentes gammes de courant, (c) La courbe $V_{2\text{-}3}$-$I_{1\text{-}4}$ après le recuit à 650 °C et 700 °C, (d) la courbe caractéristique de transfért ($I_{2\text{-}3}$-V_G) du NFFETs SiC après le recuit à 650 °C.

La résistance de contact (R_C) est calculée par l'équation suivante:

$$R_C = (R_{tot} - R_{NF}) / 2 \qquad \text{Eq. 2}$$

Par conséquent, la résistance de contact calculée (R_C) du device, respectivement à 650 °C et 700 °C est de 378 kΩ et 230 Ω. Le SiC NFFET présente un comportement quasiment métallique après le recuit à 700 °C, sans effet de grille en raison de l'intrusion de siliciure de Ni dans le canal.

La résistivité (ρ) du SiC NF peut être calculée par l'équation suivante:

$$\rho \equiv \mathrm{R}\frac{\mathrm{S}}{\mathrm{L}} = \frac{\mathrm{V_{DS}}\pi r^2}{I_{\mathrm{DS}}\,L}, \qquad \text{Eq. 3}$$

où R est la résistance de NP, S sa section, L la longueur du canal de NP et r est le rayon de NF. La résistivité est estimée à 6,1 Ω·cm.

La Figure 7(d) représente la caractéristique de transfert ($I_{2\text{-}3}$-V_G) à V_{DS} = 1V après le recuit à 650 °C. La transconductance (g_m) du SiC NFFET est calculée par l'équation suivante:

$$g_m = \frac{dI_D}{dV_G} = \mu\left(\frac{C_{\mathrm{ox}}}{L^2}\right)V_{DS}, \qquad \text{Eq. 4}$$

où µ est la « effective carrier mobility », C_{ox} est la capacité de couplage, et L est la longueur du canal. La transconductance calculée est de 0,24 ns. La capacité de la grille (C_{ox}) entre le canal NF SiC et la grille arrière est calculée en utilisant le modèle du « cylinder on plate », qui peut être donnée par l'équation suivante:

$$C_{ox} = \frac{2\pi\varepsilon\varepsilon_o L}{\ln(2h/r)}, \qquad \text{Eq. 5}$$

où ε ~ 3,9 est la constante diélectrique du SiO_2, h est l'épaisseur de la couche de SiO_2 et r est le rayon de NF. La capacité d'oxyde de grille estimée (C_{ox}) est calculée à partir de (Eq. 5) et vaut ~ 0.05 fF.

La « effective carrier mobility » peut être calculée sur la base de l'estimation de la transconductance (g_m) et la capacité de grille (C_{ox}) à l'aide de l'équation suivante;

$$\mu = \frac{g_m \cdot L^2}{C_{ox} \cdot V_{DS}} \qquad \text{Eq. 6}$$

La valeur de la « electron mobility » expérimentale, calculée à partir de (Eq. 6), est inférieure à 0,1 $cm^2 \cdot V^{-1} \cdot s^{-1}$. La mise à l'arrêt n'était pas réalisable, même pour des tensions de grille négatives élevées (- 20V) en raison de la forte concentration d'électrons le long des NFs.

b. Propriétés électriques de nanopilierde SiC FET

Un des problèmes les plus importants du SiC NFFET est la qualité du SiC NF lui-même. Les SiC NFs fabriqué par des méthodes « bottom-up » souffrent considérablement d'une forte densité de défauts d'empilement et dopage involontaire de type n. Ce type de défaut structurel et le l'important niveau de dopage de type n pourraient éventuellement conduire à de mauvaises performances électriques. Par conséquent, il peut être développé une autre approche (comme l'approche « top-down ») pour fabriquer des nanostructures de SiC, ce qui réduit considérablement la densité des défauts d'empilement et permet la maîtrise du dopage (car celui-ci est contrôlé dans les couches épitaxiées). Dans cette étude, nous avons démontré et caractérisé le 3C et le 4H- SiC NPFETs avec un niveau de dopage contrôlé en utilisant nos nanopiliers de SiC, qui est obtenu par l'approche top-down.

Dans le cas du SiC NPFET, l'épaisseur de l'oxyde de grille (SiO_2) a en outre été réduite jusqu'à 80 nm afin d'augmenter la possibilité de contrôler la grille. Le contact de recuit des SiC NPFETs fabriqués sur les substrats ci-dessus a été effectué à 650 °C pendant 30 sec dans une ambiance de N_2 dans un four à recuit thermique rapide (Jetfirst 100).

La Figure 8 montre les images MEB et les caractéristiques de transfert sortie des 3C (001) et 4H-SiC (0001) NPFET fabriqués. Le Tableau 2 contient toutes les informations concernant les dimensions et les paramètres physiques des SiC NPFETs fabriqués.

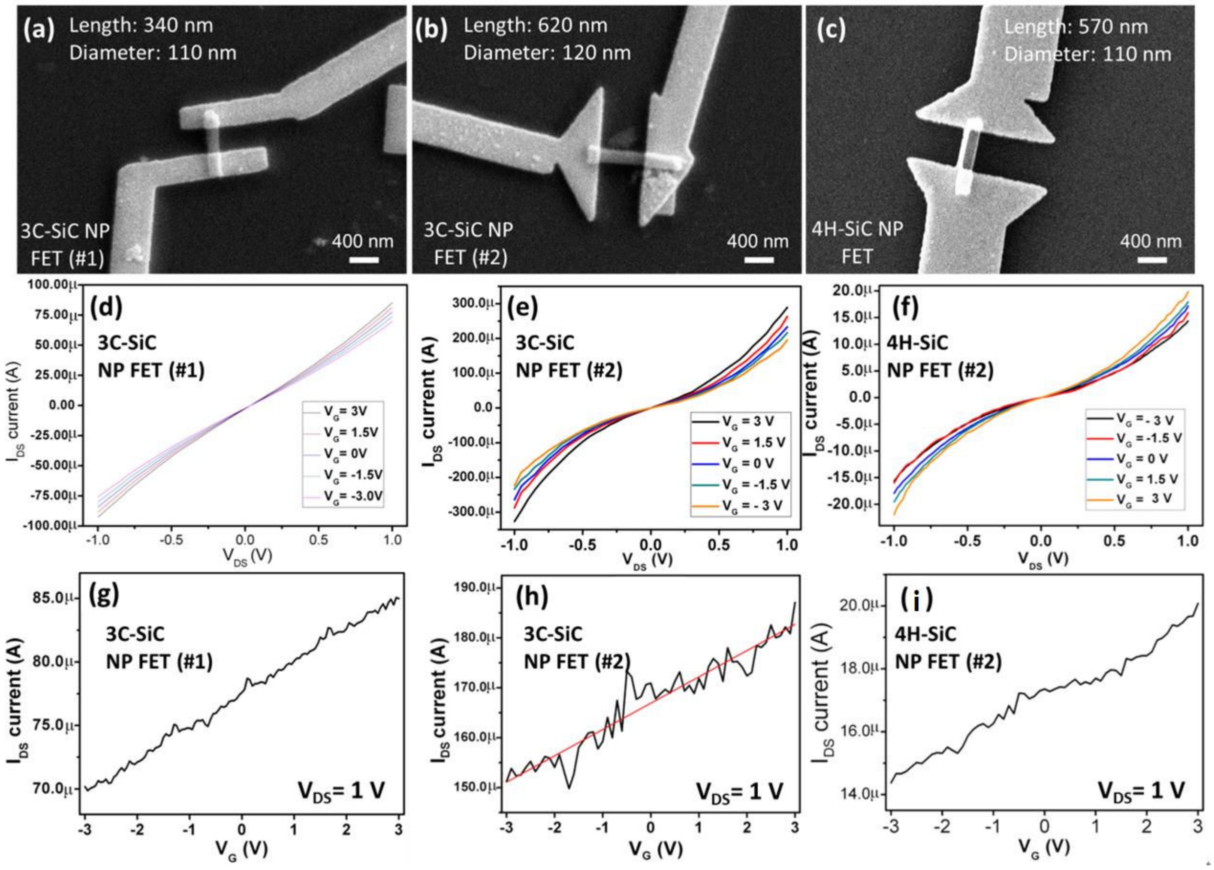

Figure 8. Images au MEB (a,b) du 3C-SiC (001) NPFETs produit et (c) du 4H-SiC (0001) NPFET produit, (d-f) la caractéristique de sortie (I_{DS}-V_{DS}) et (g-i) la caractéristique de transfert (I_{DS}-V_G) des 3C et 4H-SiC NPFET.

Le courant de sortie du NPFET est réduit lorsque la tension de grille devient plus négative, on en conclut que les électrons sont les porteurs de courant principaux. Les 3C- et 4H-SiC NPFETs présentent des valeurs de courant trois ordres de grandeur plus élevés qu'avec le SiC NFFET.

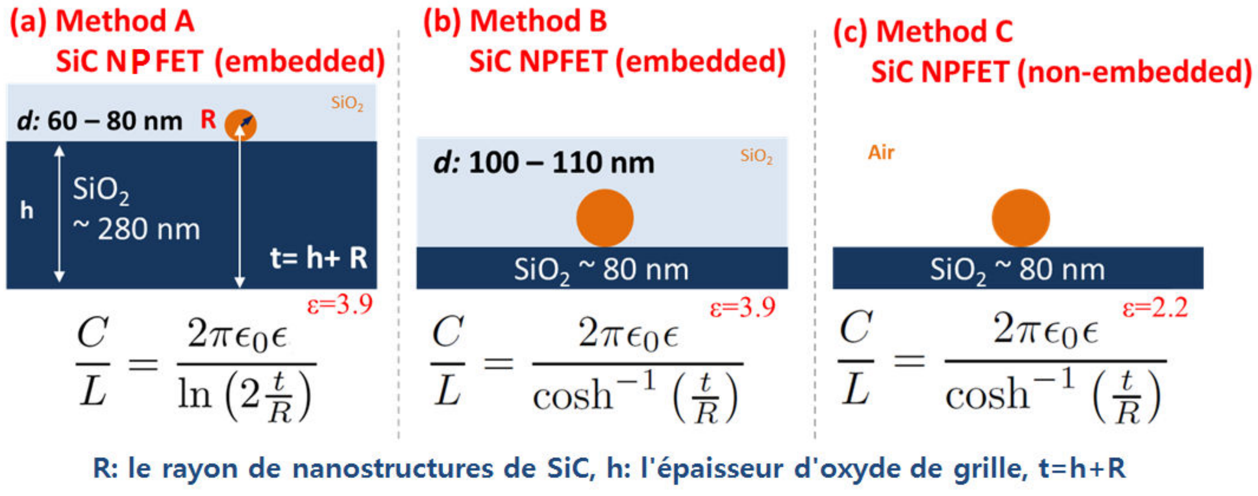

Figure 9. Estimation de la capacité de la grille (a) de SiC NFFET avec approximation et

pour (b-c) le SiC NPFET sans approximation. Respectivement, pour (b) $\varepsilon = 3.9$ et (c) $\varepsilon = 2.2$.

Pour le calcul de la mobilité, la capacité de grille (C_{ox}) du nano FET peut être estimée par le modèle « metallic cylinder on an infinite metal plate », comme décrit à l'équation suivante (Eq. 7);

$$C_{ox} = \frac{2\pi\varepsilon\varepsilon_o L}{\cosh^{-1}(\frac{t}{R})}, \qquad \text{Eq. 7}$$

où R est le rayon de NF, t est la distance entre la plaque métallique et le centre de NF (voir la Figure 9). $\mathrm{Cosh}^{-1}(x) = \ln(x + \sqrt{x^2 - 1})$ peut être approximée par ln(2x) lorsque x = t/R >> 1. Par conséquent, l'équation de la capacité de grille peut être calculée par l'équation approchée (Eq. 5). Ainsi, toutes les études rapportées précédemment sur le SiC nanoFET calculaient la capacité de grille à l'aide de cette méthode d'approximation , car l'épaisseur d'oxyde de grille était épais (500 nm). Toutefois, dans le cas de notre SiC NPFET, t (130 = 80 nm (h: épaisseur d'oxyde) + 50 nm (R: le rayon de NP)) est légèrement plus grand que le rayon de NP (R = 50 nm), soit qui t / R égal à 2,6. Par conséquent, il serait plus approprié d'utiliser l'équation non-approximative (Eq. 7 pour le device avec une épaisseur d'oxyde de grille mince. Toutefois, ce modèle de condensateur suppose que l'oxyde remplit tout l'espace entourant le nanoFET, comme représenté Figure 9(a) and (b). En réalité, l'oxyde de grille existe seulement comme un film, le NF est entièrement exposée à l'air, comme le montre la Figure 9(c).

En conséquence, ce modèle de condensateur surestime la valeur réelle de la capacité dans le cas d’un diélectrique de grille de NFs non-embedded, la valeur effective de 2,2 a été utilisée pour la constante diélectrique du SiO_2 afin de réduire cette erreur [10]. Dans cette étude, nous avons calculé les capacités d'oxyde de grille avec trois méthodes différentes, comme le montre la Figure 9. Nos résultats de SiC NPFET et la comparaison avec les meilleurs résultats rapportés de SiC NFFET sont résumés dans le Tableau 2.

Tableau 2. Résumé des résultats de nos NPFET SiC et comparatif avec le SiC NFFET indiqué précédemment.

	3C-SiC NPFET (dev n°1)	3C-SiC NPFET (dev n°2)	4H-SiC NPFET	3C-SiC NFFET
Polytypes	3C	3C	4H	3C
Les méthodes de fabrication de nanostructures de SiC	Approche descendante	Approche descendante	Approche descendante	Approche ascendante
Groupe de recherche	Notre travail	Notre travail	Notre travail	Zhou et al.
Orientation cristalline	<001>	<001>	<0001>	<111>

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[10] O. Wunnicke, "Gate capacitance of back-gated nanowire field-effect transistors," Applied Physics Letters, vol. 89, pp. 083102-3, 08/21/ 2006.

Diamètre	110 nm	120 nm	110 nm	20 nm
Longueur	340 nm	620 nm	570 nm	1.5 µm
Épaisseur d'oxyde	80 nm	80 nm	80 nm	500 nm
concentration de dopage (cm^{-3})	$2 - 8 \times 10^{16}$	$2 - 8 \times 10^{16}$	3.9×10^{15}	(estimé) 5.6×10^{18}
g_m (S)	2.58 µS à V_{DS}= 1V	5.27 µS à V_{DS}= 1V	1.32 µS à V_{DS}= 1V	0.5 nS à V_{DS}= 0.01V
C'_{ox} (F) à la méthode A	0.069 fF	0.137 fF	0.115 fF	0.070 fF
C_{ox} (F) à la méthode B (ε=3.9)	0.047 fF	0.087fF	0.080 fF	0.070 fF
C_{ox} (F) à la méthode C (ε=2.2)	0.027 fF	0.050 fF	0.045 fF	0.039 fF
μ' ($cm^2 \cdot V^{-1} s^{-1}$) à la méthode A	43.2	147.8	37.1	15.9
μ ($cm^2 \cdot V^{-1} s^{-1}$) à la méthode B	62.5	232.7	53.6	15.9
μ ($cm^2 \cdot V^{-1} s^{-1}$) à la méthode C	108.8	411.6	95.2	28.5

La mobilité des porteurs calculée par la méthode d'approximation est sensiblement inférieure à celle calculée de façon non approximative, du fait de surestimation de la capacité de grille.

Les valeurs estimées de la mobilité des porteurs par la méthode non-approximative sont 411.6 $cm^2 \cdot V^{-1} s_{-1}$ pour le 3C-SiC (001) NPFET (dev n°2) et de 95.2 $cm^2 \cdot V^{-1} s^{-1}$ pour le 4H-SiC (0001) NPFET, ce qui est plus élevé que les meilleures valeurs (15.9 $cm^2 \cdot V^{-1} s^{-1}$) rapportées dans la littérature [11], mais elles sont encore très faibles par rapport à celles attendues dans le SiC Bulk (plusieurs centaines $cm^2 \cdot V^{-1} s^{-1}$) [12].

Il est évident, que pour améliorer encore les performances du device de NFFET, il est fortement nécessaire de contrôler le diélectrique de grille avec l'interface du canal de NF. À cette fin, un NF embeded avec une géométrie grille haute et le dépôt de matériau high-k fiables sont nécessaires.

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[11] W. M. Zhou, F. Fang, Z. Y. Hou, L. J. Yan, and Y. F. Zhang, "Field-effect transistor based on β-SiC nanowire," Electron Device Letters, IEEE, vol. 27, pp. 463-465, 2006.

[12] M. Roschke and F. Schwierz, "Electron mobility models for 4H, 6H, and 3C SiC," IEEE Transactions on Electron Devices, vol. 48, pp. 1442-1447, Jul 2001.

Conclusion

Dans cette thèse, nous avons étudié les nanostructures de SiC au travers de la fabrication et de la simulation de dispositifs connexes. En outre, nous avons décrit la croissance de nanostructures de SiC sur la base de différentes méthodes de croissance, et présenté leurs propriétés caractéristiques et les applications potentielles.

Dans la partie I, les propriétés de transport et thermo-électrique du NFs SiC ont été étudiées. Il a été utilisé une combinaison de NEGF pour le transport électrique et NEMD pour le transport thermique dans le régime balistique pour prédire la figure de mérite du thermoélectrique (ZT) du NF-SiC. La ZT des NFs SiC (2,05×2,05 nm^2) atteint une valeur maximale de 1,04 à 600K pour la terminaison C. Le NF SiC ne montre pas une grande efficacité thermoélectrique par rapport au NF Si à température ambiante, bien que le NF SiC fût prometteur pour des zones de température plus élevées, en raison de ces caractéristiques de semi-conducteur à grand gap.

La partie II est consacrée à la fabrication de nanostructures de SiC par l'approche « top-down ». Dans les conditions de gravure optimales en utilisant un grand motif de masque circulaire avec un diamètre de 370 nm, les nanopiliers de 4H-SiC obtenus présentent des caractéristiques de hautement anisoptropes (6.4) avec une grande profondeur de gravure (> 7 µm). J'ai aussi démontré les nanopiliers de SiC avec différents polytypes et orientations; la longueur de ces piliers de diamètre inférieur à 100 nm est d'environ 1,0 µm. Les effets des différents polytypes (4H-, 6H et 3C-SiC) et des orientations cristallographiques ((0001) et (11-20) de 6H-SiC, (001) et (111) de 3C-SiC) ont été étudiées dans le but de réaliser des nanopiliers de SiC.

La morphologie des nanopiliers de SiC gravés a montré des caractéristiques intéressantes en fonction des polytypes et des orientations cristallines. Des structures de pilier à base hexagonale, losange et triangulaire ont été obtenues en utilisant respectivement des substrats de α-SiC (0001), 3C-SiC (001), et 3C-SiC (111). Ces morphologies uniques de nanopiliers de SiC sont issues d'une interaction complexe entre les polytypes et les orientations cristallines.

Dans la partie III, deux types différents de SiC nanoFETs (SiC NFFET et SiC NPFET) ont été fabriqués et caractérisés. La propriété de contact à base de Ni sur le SiC NFFET a été étudiée en fonction de la température de recuit pour améliorer le contact ohmique du métal sur le SiC nanoFET. Une faible résistivité ohmique de contact sur le SiC NFFET a été obtenue après le recuit à 650 °C. Le siliciure de nickel commence à diffuser dans le canal du nanofil en SiC après un recuit à 700 °C.

Nous avons démontré les caractéristiques du SiC NPFETs avec un niveau de dopage contrôlé et en utilisant nos nanopiliers de SiC, obtenus par l'approche top-down. Les valeurs estimées de la mobilité des porteurs sont 411,6 cm^2·V^{-1}s^{-1} pour le 3C-SiC (001) NPFET (dev n°2) et de 95,2 cm^2·V^{-1}s^{-1} pour les 4H-SiC (0001) NPFET, qui est plus élevée que les meilleures valeurs (15,9 cm^2·V^{-1}s^{-1}) rapportées dans la littérature [11], mais cette valeur est encore très faible par rapport à celle prévue dans le SiC Bulk (plusieurs centaines de cm^2·V^{-1}s^{-1}). Il est conseillé dans l'avenir de procéder au dépôt d'un matériau high-k fiable pour améliorer le couplage de grille et la performance du dispositif.

Résumé

Les nanostructures de semi-conducteurs de faibles dimensions (comme les nanofils(NFs)) sont devenues l'objet de recherches intensives pour explorer de nouveaux phénomènes émergents à l'échelle nanométrique et sonder leur possibilités d' utilisation dans l'électronique du futur. Parmi les différents nanofils semi-conducteurs, SiC a des propriétés très particulières, comme une large bande interdite, une excellente conductivité thermique, un haut champ électrique de claquage, une stabilité chimique et physique, une haute mobilité des électrons et une haute biocompatibilité.

Nous proposons dans cette étude ; d'examiner une nouvelle approche pour fabriquer des nanostructures de SiC par l'approche « top-down ». Cela permet l'élaboration de nanostructures cristallines de SiC de haute qualité monocristalline avec un niveau de dopage contrôlé. Le comportement de nanostructures de SiC gravées a également été étudié en fonction de polytypes et des orientations cristallographiques.

Nous avons également étudié les trois principaux sujets de SiC nano-devices pour atteindre une excellente performance. Pour répondre à ces questions, deux types de SiC nanoFET (SiC NFFET et SiC NPFET) ont été fabriqués et caractérisés par l'utilisation de nanofils de SiC et de nanopiliers de SiC préparés respectivement par les méthodes « bottom-up » et « top-down ».

Mots Clefs: Nanofil, transistor à effet de champ, SiC, de haut en bas , plasma à couplage inductif, propriété thermoélectrique

Abstract

Low dimensional semiconductor nanostructures (such as nanowires) have become the focus of intensive research for exploring new emergent phenomena at the nanoscale and probing their possible use in future electronics. Among various semiconductor nanowires, SiC has very unique properties, such as wide band-gap, excellent thermal conductivity, high breakdown electric field, chemical and physical stability, high electron mobility and biocompatibility.

We propose in this study to investigate a new approach to fabricate SiC nanostructures by top-down approach. This allows the elaboration of crystalline SiC nanostructures with high quality single crystalline with controlled doping level. The etching behavior of SiC nanostructures has also been studied depending on polytypes and crystallographic orientations.

We also investigate three main issues of SiC nano-devices to achieve excellent performance: (First: metal ohmic contact on nanoFET, second: poor quality of SiC NW with associated stacking fault and unintentional n-type doping, last: the nanowire (or nanopillar)-gate oxide interface). To address these issues, two different kinds of SiC nanoFET (SiC NWFET and SiC NPFET) been fabricated and characterized by using SiC nanowires and SiC nanopillars prepared via bottom-up method and top-down methods, respectively.

Keywords: Nanowire, Field-Effect Transistor, SiC, top-down, inductively coupled plasma, thermoelectric property