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Reliability analysis of embedded Phase-Change Memories based on innovative materials

Gabriele Navarro

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THÈSE

Pour obtenir le grade de

DOCTEUR DE L'UNIVERSITÉ DE GRENOBLE

Spécialité : **Nano Électroniques et Nano Technologies**

Arrêté ministériel : 7 août 2006

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co-encadrée par **Véronique SOUSA**

préparée au sein du **CEA-LETI**
dans **l'École Doctorale Electronique, Electrotechnique,
Automatique et Traitement du Signal**

Reliability Analysis of Embedded Phase-Change Memories Based on Innovative Materials

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Gabriele Navarro

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Abstract - Résumé

TITLE: Reliability Analysis of Embedded Phase-Change Memories Based on Innovative Materials

Abstract:

Memories are getting an exponential importance in our present era, and are fundamental in the definition of all the electronic systems with which we interact in our daily life. Non-volatile memory technology (NVM), represented by Flash technology, have been able to follow till now the miniaturization trend to fulfill the increasing memory density demanded by the market. However, the scaling is becoming increasingly difficult, rising their cost per byte due to the incoming technological complexity. In this context, innovative memory technologies are becoming not just an alternative, but the only possible solution to provide higher density at lower cost, better functionality and low power consumption. Phase-Change Memory (PCM) technology is considered the leading solution for the next NVM generation, combining non-volatility, scalability, bit-alterability, high write speed and read bandwidth and high cycle life endurance. However, some reliability issues remain to overcome, in order to be a valid Flash replacement in all the possible applications. In particular, retention of data at high temperature, is one of the main requirements of industrial and automotive embedded applications.

This work focuses on the study of embedded Phase-Change Memories, in order to optimize the memory device and finally propose some solutions to overcome the main bottlenecks of this technology, in particular addressing automotive applications. We designed, fabricated, and tested PCM devices based on recognized and innovative structures, analyzing their advantages and disadvantages, and evaluating the scaling impact. Our reliability analysis led to the development of a characterization setup dedicated to characterize our PCM cells with pulses in the order of nanoseconds, and to the implementation of a simulation tool based on a thermoelectrical solver and on the Level Set numerical approach, to understand the different mechanisms taking place in our cells during the programming operations.

In order to fulfill embedded NVM requirements, we engineered the phase-change material integrated in the PCM device with two main approaches: the stoichiometry variation and the dopants addition. We showed and explained how the data retention in GeTe based PCM devices can be enhanced increasing Te content, and how SiO₂ inclusions can reduce the read voltage disturbs at high operating temperatures. Moreover, we reported the advantages on the programming power reduction of carbon doping in Ge₂Sb₂Te₅ based devices. Finally, we studied the effects of Ge enrichment in Ge₂Sb₂Te₅, combined with N or C doping, integrated in state-of-the-art PCM cells. Through the introduction of a new programming technique, we demonstrated the possibility to improve the programming speed of these devices, characterized by data

retention performance among the best reported in the literature, and to reduce the drift phenomenon that affects the resistance state stability of PCM technology. We then proved, with these last results, the suitability of PCM for embedded applications.

Speciality: Nanoelectronics and Nanotechnology

Key Words: Phase-Change Memory, embedded applications, reliability, innovative materials, non-volatile memory.

Thesis work prepared at: Advanced Memory Laboratory, CEA, LETI, MINATEC Campus, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France.

TITRE : Analyse de la Fiabilité de Mémoires à Changement de Phase Embarquées Basées sur des Matériaux Innovants

Résumé :

Les Mémoires ont de plus en plus importance à l'époque actuelle, et sont fondamentales pour la définition de tous les systèmes électroniques avec lesquels nous entrons en contact dans notre vie quotidienne. Les mémoires non-volatiles (NVM), représentées par la technologie Flash, ont pu suivre jusqu'à présent l'effort à la miniaturisation pour satisfaire la demande croissante de densité de mémoire exigée par le marché. Cependant, la réduction de la taille du dispositif de mémoire est de plus en plus difficile et la complexité technologique demandé a augmenté le coût par octet. Dans ce contexte, les technologies de mémoire innovantes deviennent non seulement une alternative, mais la seule solution possible pour fournir une densité plus élevée à moindre coût, une meilleure fonctionnalité et une faible consommation d'énergie. Les Mémoires à Changement de Phase (PCM) sont considérées comme la solution de pointe pour la future génération de mémoires non-volatiles, grâce à leur non-volatilité, scalabilité, "bit-alterability", grande vitesse de lecture et d'écriture, et cyclabilité élevée. Néanmoins, certains problèmes de fiabilité restent à surmonter afin de rendre cette technologie un remplacement valable de la technologie Flash dans toutes les applications. Plus en détail, la conservation des données à haute température, est l'une des principales exigences des applications embarquées industrielles et automobiles.

Cette thèse se concentre sur l'étude des mémoires à changement de phase pour des applications embarquées, dans le but d'optimiser le dispositif de mémoire et enfin de proposer des solutions pour surmonter les principaux obstacles de cette technologie, en abordant notamment les applications automobiles. Nous avons conçu, fabriqué et testé des dispositifs PCM basés sur des structures reconnues et innovantes, en analysant leurs avantages et inconvénients, et en évaluant l'impact de la réduction de la taille. Notre analyse de fiabilité a conduit au développement d'un système de caractérisation dédié à caractériser nos cellules PCM avec des impulsions de l'ordre de la nanoseconde, et à la mise en œuvre d'un outil de simulation basé sur un solveur thermoélectrique et sur l'approche numérique "Level Set", pour comprendre les différents mécanismes qui ont lieu dans nos cellules pendant les opérations de programmation.

Afin de répondre aux spécifications du marché des mémoires non-volatiles embarquées, nous avons conçu le matériau à changement de phase intégré dans le dispositif PCM avec deux principales approches : la variation de la stœchiométrie et l'ajout de dopants. Nous avons démontré et expliqué comment la rétention des données dans les dispositifs PCM à base de GeTe peut être améliorée avec l'augmentation de la concentration de

Te, et comme les inclusions de SiO₂ peuvent réduire les défauts causés par la tension de lecture à températures de fonctionnement élevées. En outre, nous avons présenté les avantages sur la réduction de la puissance de programmation du dopage de carbone dans les dispositifs à base de Ge₂Sb₂Te₅. Enfin, nous avons étudié les effets de l'enrichissement en Ge dans le Ge₂Sb₂Te₅, combiné avec le dopage N et C, intégré dans des cellules PCM à l'état de l'art. Grâce à l'introduction d'une nouvelle technique de programmation, nous avons démontré la possibilité d'augmenter la vitesse de programmation de ces dispositifs, caractérisés par des performances de rétention des données parmi les meilleurs rapportés dans la littérature, et de réduire le phénomène de la dérive de la résistance qui affecte la stabilité de l'état programmé des cellules PCM. Nous avons donc prouvé, avec ces derniers résultats, la pertinence de la technologie PCM pour les applications embarquées.

Spécialité : Nano Électroniques et Nano Technologies

Mots Clés : mémoires à changement de phase, applications embarquées, fiabilité, matériaux innovants, mémoires non-volatiles.

Thèse préparée au sein du : Laboratoire de Mémoires Avancées,
CEA, LETI, MINATEC Campus, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France.

List of Symbols

Symbol	Measure Unit	Designation
a	$[m]$	Characteristic distance
A	$[A m^{-2}]$	Fitting parameter (current density) in the equation of the electrical conductivity of the amorphous phase (simulation tool)
A_{th}	$[m^2]$	Thermal effective area
A_{PLUG}	$[m^2]$	Surface area of the plug/phase-change material interface
B	$[m]$	Fitting parameter (distance) in the equation of the electrical conductivity of the amorphous phase (simulation tool)
B_W	$[Bytes s^{-1}]$	Memory bandwidth
C_{end}	$[cycles]$	Cycling endurance
C_p	$[J K g^{-1} K]$	Heat capacity of the material (simulation tool)
C_P	$[F]$	Parasitic capacitance
Δd	$[m]$	Average increase of the radius of the crystalline volume
d	$[m]$	Interatomic distance (simulation tool)
\vec{E}	$[V m^{-1}]$	Electric field vector
E	$[V m^{-1}]$	Electric field intensity
E_0	$[V m^{-1}]$	Characteristic field
E_{am}	$[eV]$	Activation energy of conduction in the amorphous phase (simulation tool)
E_{cr}	$[eV]$	Activation energy of the conduction in the crystalline phase (simulation tool)
E_g	$[eV]$	Energy band gap
E_A	$[eV]$	Activation energy of the failure process
E_B	$[eV]$	Energy barrier of the structural relaxation
E_C	$[eV]$	Activation energy of the conduction
E_{TH}	$[V m^{-1}]$	Threshold electric field
f_{BW}	$[Hz]$	Bandwidth
g	$[-]$	Shape factor
ΔG_{ac}	$[eV]$	Difference between the Gibbs free energy of the amorphous and crystalline phase
ΔG_v	$[eV m^{-3}]$	Difference between the Gibbs free energy per unit volume of the amorphous and crystalline phase
I_m	$[A]$	Melting current
I_{nucl}	$[m^{-3} s^{-1}]$	Nucleation rate
I_{peak}	$[A]$	Current peak
I_s	$[m^{-3} s^{-1}]$	Stationary nucleation rate
I_{CELL}	$[A]$	Current in the cell
I_{ON}	$[A]$	Current in the cell in the ON-state
I_R	$[A]$	RESET current
I_S	$[A]$	SET current
I_{TH}	$[A]$	Threshold current

\vec{J}	$[A m^{-2}]$	Current density vector
J	$[A m^{-2}]$	Current density intensity
J_R	$[A m^{-2}]$	RESET current density
J_S	$[A m^{-2}]$	SET current density
k_{th}	$[W m^{-1} s^{-1}]$	Thermal conductivity
k_{th}^e	$[W m^{-1} s^{-1}]$	Thermal conductivity due to electron diffusion
k_{th}^{pcm}	$[W m^{-1} s^{-1}]$	Thermal conductivity of the phase-change material
k_{th}^L	$[W m^{-1} s^{-1}]$	Lattice thermal conductivity
k_B	$[eV K^{-1}]$	Boltzmann constant
K	$[-]$	Crystallization rate of the Avrami equation
L_m	$[J m^{-3}]$	Latent heat of melting (simulation tool)
L_{PLUG}	$[m]$	Length of the plug element
M	$[Kg mol^{-1}]$	Molar mass (simulation tool)
M_C	$[Bytes]$	Memory capacity
n	$[-]$	Reaction order of the crystallization process in the Avrami equation
n_{ff}	$[-]$	Form factor
n_p	$[-]$	Polarization factor
N	$[m^{-3}]$	Density of the possible nucleation sites (simulation tool)
N_0	$[-]$	Number of growing crystals
O_n	$[-]$	Number of atoms at the surface of the critical size nucleus (simulation tool)
p	$[W m^{-3}]$	Power density
P	$[W]$	Electrical power
P_m	$[W]$	Power to melt the phase-change material
P_{CELL}	$[W]$	Programming power delivered in the PCM cell
q	$[C]$	Fundamental charge
r_0	$[m]$	Critical nucleus size
R	$[\Omega]$	Resistance value
R_0	$[\Omega]$	Resistance constant - fitting parameter
R_{th}	$[K W^{-1}]$	Thermal resistance
R_{CELL}	$[\Omega]$	Cell resistance
R_{LINES}	$[\Omega]$	Resistance of access lines
R_{LOAD}	$[\Omega]$	Pull-up load resistance
R_{ON}	$[\Omega]$	Resistance of the cell in the ON-state
R_{PCM}	$[\Omega]$	Resistive contribution of the phase-change material
R_{PLUG}	$[\Omega]$	Plug resistance
R_{SET}	$[\Omega]$	SET resistance of the device
R_{RESET}	$[\Omega]$	RESET resistance of the device
S_D	$[m^2]$	Amorphous dome external surface
\bar{t}	$[s]$	Observation time
\bar{t}_0	$[s]$	Characteristic time
t_0	$[s]$	Time constant - fitting parameter
t_{cr}	$[s]$	Crystallization time
t_{fail}	$[s]$	Failure time
T	$[K]$	Temperature
ΔT	$[K]$	Temperature variation

T_a	[K]	Ambient temperature
T_{life}	[s]	Life time of the cell
T_m	[K]	Melting temperature
T_C	[K]	Crystallization temperature
u_a	[m]	Amorphous material thickness
U_B	[eV]	Atomic energy barrier of the crystallization growth
v_g	[m s ⁻¹]	Growth speed
V_0	[V]	Characteristic voltage
V_{CELL}	[V]	Voltage drop on the PCM cell
V_H	[V]	Holding voltage
V_{MAX}	[V]	Maximum voltage of the pulse generator
V_{PULSE}	[V]	Voltage applied
V_{TH}	[V]	Threshold voltage
W	[eV]	Activation energy of the nucleation
W_0	[eV]	Zero-field energy barrier of nucleation
W_{cr}	[eV]	Activation energy of the crystallization
W_{ON}	[eV]	Activation energy of the ON-state (simulation tool)
Δz	[m]	Mean distance between two traps in the lattice
Z_e	[-]	Zeldovich factor (simulation tool)
α	[-]	Crystalline fraction in the amorphous volume
α_{nucl}	[-]	Geometrical constant dependent on the nucleus shape
α_{th}	[m ³ K W ⁻¹]	Thermal efficiency constant
α_{wle}	[%]	Wear leveling efficiency
γ_m	[-]	Material dependent constant
γ_c	[-]	Constant dependent on the critical conductivity at the switching point
γ_a	[Hz]	Characteristic atomic frequency (simulation tool)
ϵ	[F m ⁻¹]	Dielectric permittivity
λ	[m]	Percolation distance (simulation tool)
ν_c	[Hz]	Frequency of the atomic vibration in the crystalline phase
ν_a	[Hz]	Frequency of the atomic vibration in the amorphous phase
ν	[-]	Drift coefficient
ρ	[Ωm]	Resistivity
ρ_0	[Ωm]	Resistivity constant
ρ_{cr}	[Ωm]	Resistivity of the crystalline phase
ρ_m	[Ωm]	Material density (simulation tool)
ρ_{PLUG}	[Ωm]	Resistivity of the plug element
σ	[S m ⁻¹]	Electrical conductivity
σ_0	[S m ⁻¹]	Saturation conductivity
σ_{ac}	[J m ⁻²]	Crystal-amorphous interface energy
σ_t	[s]	Time variability
σ_{ON}	[S m ⁻¹]	Conductivity of the ON-state (simulation tool)
σ_{TH}	[S m ⁻¹]	Threshold conductivity
σ_V	[V]	Voltage measure resolution
σ_W	[eV]	Dispersion of the energy barrier of nucleation
σ_{W_0}	[eV]	Dispersion of the zero-field energy barrier of nucleation

τ_0	[s]	Defect relaxation time at high temperature
τ_i	[s]	Incubation time
τ_l	[s]	Carrier life time
τ_r	[s]	Relaxation time of the material
τ_v	[s]	Characteristic vibrational atomic time
τ_{SR}	[s]	Defect relaxation time
ϕ	[m]	Diameter of the plug in a lance-type structure
Ω	[m ³]	Nucleus volume

Introduction

Context

Memories are getting an exponential importance in our present era, and are fundamental in the definition of all the electronic systems with which we interact in our daily life. The number of digital data created and stored every day reached last year the surprising rate of 2.5 quintillion bytes per day (10^{18} bytes), with the 90% of the world's data created in the last two years alone [1]. Hence, the memory technologies have become more than a simple support technology, with the introduction of the “memory-centric” electronic concept [2]. The main example of this, is the changed measure unit along the years to describe a specific electronic application, moving from the computation power of the CPU to the memory capacity. Dynamic Random Access Memory (DRAM) but over all non-volatile memory technology (NVM), represented by Flash technology, have been able to follow till now the miniaturization trend to fulfill the increasing memory density demanded by the market. However, the scaling is becoming increasingly difficult, rising the cost per byte of Flash memories due to the incoming technological complexity. In this context, innovative memory technologies are becoming not just an alternative, but the only possible solution to provide higher density at lower cost, better functionality (bandwidth and latency) and low power consumption. Moreover, the great quest is to identify a technology able to guarantee the scaling for more consecutive technology nodes.

Different companies and research centers in recent years started the study of new possible solutions to replace standard memories. Instead of displacing and trapping electrons like in Flash memory, innovative approaches have been investigated, changing and simplifying also the philosophy of the device. A resistive NVM is based on a two-terminal device, in which an “active” material is sandwiched between two electrodes. The main idea of this structure, is to use a specific physical mechanism characteristic of the active material considered, to switch it reversibly, between two completely different resistive states. For example, in a Phase-Change Memory (PCM) a chalcogenide material (phase-change material) is used, taking advantage of the thermally induced transition from an amorphous phase to a crystalline phase. In a Resistive or Conductive Bridge RAM (RRAM or CBRAM), a metallic filament is grown and dissolved inside an insulating material. Another example is the Oxide RAM (OxRAM), in which the reversible soft-breakdown of some oxides is used. These memory devices, are among the most studied nowadays, and the possible candidates for the next NVM generation, replacing Flash and possibly also DRAM. The latter in fact, represents today the higher source of power consumption in the memory systems, requiring constant data refresh.

PCM technology is considered the leading solution for the next NVM generation, revealing unique capabilities with respect to the other competing memory technologies [3, 4]. In particular it offers:

- non-volatility: DRAM requires a constant power supply to retain information, resulting in higher power consumption. PCM, being non-volatile, offers the retention of the data after power removal;
- scalability: stability of the stored phase has been demonstrated to be at least as small as 5 nm [5];
- bit-alterability: Flash technology requires regular page refreshing. PCM, like random access memories (RAM), does not require pre-erasing operations to store the information;
- write speed: the PCM write speed (on the order of 100 MB/s) is approaching today the 1 GB/s of DRAM;
- read bandwidth: Flash has long random access times on the order of tens of microseconds. PCM shows read latency of tens of nanoseconds like DRAM, enabling in-place code execution (not possible with standard Flash);
- endurance: PCM has not reached already the high endurance of 10^{16} cycles of DRAM, but its demonstrated endurance of 10^{12} cycles [6] makes it suitable for some DRAM replacement in infrequent or managed write applications;
- rad-hardness: radiation hardness is another important feature of PCM technology [7], required in embedded space applications or high energy physical instruments.

Even if PCM is today a recognized mature industrial technology, some reliability issues remain to overcome, in order to be a valid Flash replacement in all the possible applications. In fact, the thermal stability at high temperatures of the phase-change material integrated in a PCM device, is an intrinsic challenge of this technology. The retention of data in high temperature environments is one of the main requirements of industrial and automotive embedded applications, like microcontrollers and other integrated circuits that embed NVM. The required operations from $-40\text{ }^{\circ}\text{C}$ up to more than $150\text{ }^{\circ}\text{C}$, the soldering reflow process at $260\text{ }^{\circ}\text{C}$ and the zero-defects requirement, are today the big challenges for PCM technology to finally fulfill all the requirements of the market. Moreover, the multi-level capability can open the door for higher data density.

Thesis presentation

This work focuses on the study of embedded Phase-Change Memory, in order to optimize the memory device and finally propose some solutions to overcome the main bottlenecks of this technology, in particular addressing automotive applications and multi-level capability.

In chapter 1 we present the PCM technology and the basics of the phase-change memory device. We introduce the $\text{Ge}_2\text{Sb}_2\text{Te}_5$ and the GeTe, as main phase-change materials that made possible the development of a PCM. We focus then on the three phases of a phase-change material: the crystalline phase, the amorphous phase and the liquid phase. The analysis of the electrical and thermal properties of the phases of a phase-change material, allows to understand the main characteristics of the final PCM cell, and the correlated reliability issues.

The chapter 2 presents the electrical parameters of a PCM device, and how the geometry and the scaling of the cell strongly impact the device performance. We present then some of the main PCM structures developed in the last decade, in order to scale the cell size, starting with the lance-type cell and ending with the state-of-the-art industrial “Wall” PCM. At the same time, we introduce the devices we designed, fabricated and tested, in order to perform our studies on this technology. We developed a specific characterization setup in order to perform the reliability analysis, and in the chapter we show the main issues of PCM, in particular correlated with the stability of the phase-change material at high operating temperatures. The specific case of the reliability of the PCM μ trench technology is addressed. To conclude, we present the simulation tool we implemented, in order to understand the different mechanisms taking place in the cell during the programming operations, and to understand the dependency of the device behavior, on the phase-change material physical parameters.

In chapter 3 we describe how we engineered our phase-change materials. We show how tuning the GeTe stoichiometry, we were able to improve the data retention of the PCM device. We demonstrate that SiO_2 doping in phase-change materials allows the reduction of the read-disturb problem at high temperature, and we propose the carbon doping, as possible solution for the cell power reduction. Finally, we show how we obtained data retention results among the best reported in the literature, in Ge-rich based state-of-the-art devices fabricated in the framework of the collaboration with STMicroelectronics. Through the introduction of a new programming technique, we demonstrate the possibility to improve the programming speed of these devices, and to reduce the drift phenomenon that affects the resistance state stability of PCM technology, in particular at high temperature. We then proved, with these last results, the suitability of PCM for embedded applications.

In the end, we present the general conclusions of this work, summarizing the main results obtained and proposing some perspectives for future research activities on this technology.

Chapter 1

The Phase-Change Memory Technology

Phase-Change Memory (PCM) bases its functionality on the physical phase change of a chalcogenide material, sandwiched between two electrodes. This simple definition, revealed in the last decade the potentiality of a new technology, which has become today the most promising candidate for the next generation of non-volatile memory. The phase-change materials belong to the class of chalcogenides. The outstanding property of these materials is the reversible switching from a high resistive amorphous phase to a low resistive crystalline phase, made possible in a memory device, by the current induced Joule heating of the phase-change material.

In this chapter we introduce the principles of the PCM technology, and the range of applications in which the PCM technology can be used. We present then the GeTe and the $\text{Ge}_2\text{Sb}_2\text{Te}_5$, considered as the two main phase-change materials, and studied in recent years before for optical applications, and nowadays for phase-change memory (PCM) applications. We address the phase-change theory and we analyze the three phases of a phase-change material: the crystalline phase, the amorphous phase, and the liquid phase. Their thermal and electrical properties are described, in order to understand how they impact the final behavior of the memory device.

United States Patent Office

3,241,009

Patented Mar. 15, 1966

3,241,009
**MULTIPLE RESISTANCE SEMICONDUCTOR
 ELEMENTS**
 Jacob F. Dewald, Mendham, William R. Northover,
 Westfield, and Arthur D. Pearson, Bernardsville, N.J.,
 assignors to Bell Telephone Laboratories, Incorporated,
 New York, N.Y., a corporation of New York
 Filed Nov. 6, 1961, Ser. No. 150,374
 14 Claims. (Cl. 317—234)

What is claimed is:

1. An electrical component capable of operating in two resistance states comprising a glass body having an electronic resistivity within the range 10^2 to 10^8 ohm-cm. and having electrical means for impressing an electric signal on said body, said glass comprising means responsive to voltage signals of a minimum value for changing the resistance state of said body from a first discrete high resistance state to a second discrete low resistance state and said means being further responsive to the rate of decrease of the value of the voltage signals to revert said body to the high resistance state when the rate of decrease of the voltage signal exceeds a given rate and to maintain said body in the low resistance state when the rate of decrease of the voltage signal is less than the given rate.

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BY

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ATTORNEY

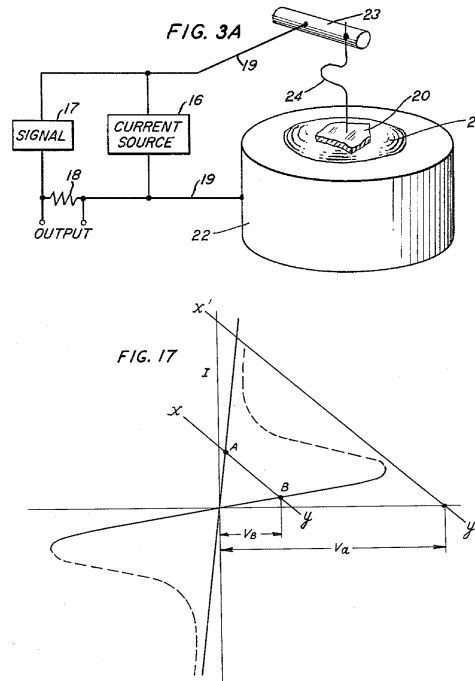


Fig. 1.1. First patent on a multiple resistance device, based on a reversible switching mechanism. On the right the idea for the characterization setup and the current/voltage characteristic of the device, showing the two different programmable state (A and B) [8].

1.1 Brief history of PCM technology

The concept of using the amorphous to crystalline phase transition of chalcogenide materials to store information has been proposed since the early 1960's by Stanford Robert Ovshinsky, considered the father of the phase-change memory devices. His main contribution is the demonstration of the existence of the switching phenomenon, that makes possible the transition of an amorphous phase-change material from a low to a high conductive state, in different chalcogenides integrated in analytical structures. The first patent concerning "multiple resistance semiconductor elements" was filled in 1961 by Dewald, Northover and Pearson, in which they advanced the description of the modern PCM technology and that we report partially in Fig. 1.1. In their idea they evidenced the main characteristics of a PCM device. First, two possible main stationary states: a low resistance state (called LRS or SET) and a high resistance state (HRS or RESET). Second, the presence of a so called "threshold voltage" (V_{TH}) that makes possible the electronic switching from a low to a high conductive state, in which the current-induced Joule heating of the phase-change material allows the recrystallization of the material, and then the transition from the HRS to the LRS [8].

Even if the industrial interest for PCM technology started to be concrete in 1970, when the first 256-bit memory array was developed by Neale and Nelson of Energy Conversion Devices along with Gordon Moore of Intel, a real first comprehension of

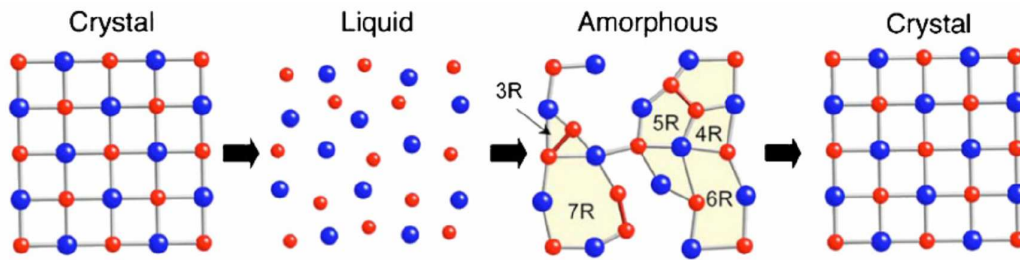


Fig. 1.2. The principle of the phase change transition. The phase-change material in the crystalline phase has to be melted to achieve the liquid phase. If the cooling rate is sufficiently high, then the material is quenched in the amorphous phase. To recover the crystalline phase, only a specific thermal profile can provide the energy necessary for the atomic reorganization [9].

the switching phenomenon has not been provided until the early 80's. Just after the first successful integrations of phase-change materials in silicon based electronics, the future of this technology started to be compromised by the limitation of the technology node: to guarantee a reliable and power-efficient device, the dimensions required a level of integration not available in that years. This explains the hibernation for about 20 years of PCM technology, just after the realization in 1978 of the first 1 kbit PCM prototype by Burroughs Corporation. Along this period, phase-change materials started their well known success in the optical applications, also thanks to the discovery of $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST) and its phase change properties. With the release of the first rewritable compact disc (CD-RW) in 1990, Panasonic declared the starting of the end of the magnetic tape supports for consumer applications: the first real revolution caused by the phase-change materials in the history of technology.

The principle of the phase transition in a PCM device, is based on the thermal-induced phase change of the material from a crystalline phase, ordered and lowly resistive, to an amorphous phase, disordered and highly resistive, passing from the liquid phase, as schematically described in Fig. 1.2 [9]. To achieve the amorphous phase, the phase-change material in the crystalline phase has to be melted (crossing the material melting temperature T_m), through Joule heating, at high current densities, and then rapidly quenched (RESET operation). Thanks to the switching phenomenon, once reached a specific electric field threshold (E_{TH}), the material in the amorphous phase changes abruptly its conductivity and starts to be highly conductive (what we call "ON-state" of the material). The phase-change material, once in the ON-state, is then crystallized through the Joule heating obtained thanks to the current flow (SET operation). There are many other properties of these materials that are involved in the device behavior, that we will analyze in the next sections introducing the properties of the crystalline phase, of the amorphous phase and of the liquid phase of a phase-change material.

1.2 The PCM cell

Like other resistive memories, the phase-change memory (PCM) cell is a two-terminal device. It bases its functionality on the strong difference in resistivity (up to more than 5 orders of magnitude), between the crystalline phase and the amorphous phase of the

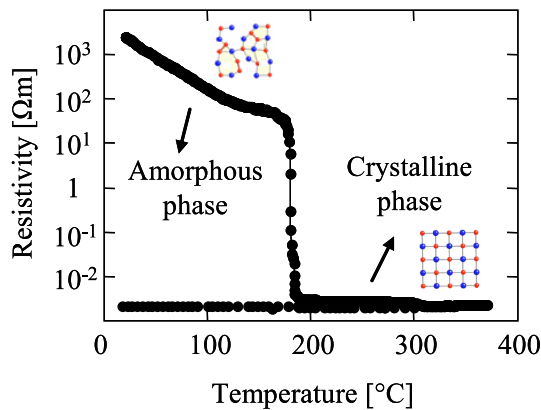


Fig. 1.3. Resistivity as a function of the temperature of a phase-change material. The transition from the amorphous to the crystalline phase, is highlighted by the sharp decrease of the resistivity of the material.

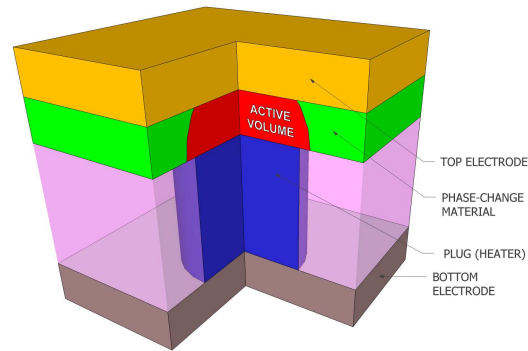


Fig. 1.4. General description of a PCM cell. The active volume involved in the phase transition is highlighted at the plug/phase-change material interface.

phase-change materials. In Fig. 1.3 we can see an example of this transition. The amorphous material is heated, and during the temperature increase, it experiences a decrease of the resistivity at a specific temperature, called crystallization temperature. The process of crystallization, activated and favorable at this temperature, drastically increases the conductivity of the material, finally crystallizing all the material volume. Once the material is cooled down to room temperature, the crystalline phase is preserved. The full process gives rise to the phase-change mechanism, in this case, induced by the external heating of the material.

The PCM cell, as reported in Fig. 1.4, can be basically described as consisting of:

- the bottom electrode;
- the plug conductive element (called also “heater”) with the function to provide the electrical access to the phase-change material, to enable the current limitation, and to contribute to the “heating” of the phase-change material in the different phases of the programming;
- the phase-change material;
- the insulator surrounding the plug;
- the top electrode.

In the standard memory array architecture, the memory cell consists of a transistor access device (1T) and the PCM cell in series (1R). This configuration is called “1T1R”. In an analytical structure in which only the PCM cell is realized in order to allow the study of the resistive element, the metal levels of the top and bottom electrodes are properly designed in order to provide the electrical access to the cell, and they are called “access lines”.

To program a PCM cell in the RESET state (or high resistance state, HRS), a RESET pulse is applied, consisting of a high current pulse able to raise the temperature above the melting point (T_m) in the active chalcogenide volume, followed by a sharp

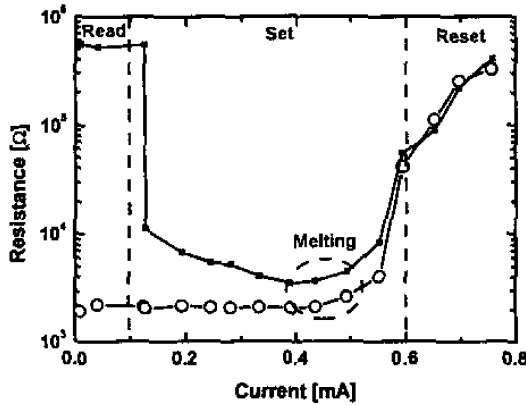


Fig. 1.5. Resistance as a function of the programming current (R-I), for a phase-change memory device starting from the SET state (open symbols), and starting from the RESET state (filled symbols). The READ, SET and RESET current ranges are highlighted [11].

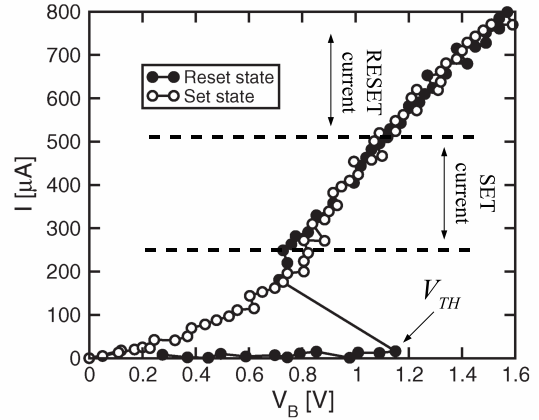


Fig. 1.6. Programming current as a function of cell voltage characteristic (I-V), typical of a PCM device. The two curves correspond respectively to a device starting from a RESET state (filled symbols), and to a device starting from a SET state (open symbols) [10].

trailing edge quenching the same volume into an amorphous state (RESET operation) [10]. The RESET operation can be successful, only if a considerable volume of phase-change material is amorphized over the plug surface, in order to increase considerably the resistance of the device. To program the cell in the SET state (or low resistance state, LRS), two main strategies can be adopted:

- the application of a pulse with the same amplitude of a RESET pulse, but with a trailing edge sufficiently long to guarantee the permanence of the phase-change material in the range of temperatures favorable to the recrystallization;
- a pulse with amplitude lower than the RESET pulse, but higher than the threshold voltage, able to provide already during the pulse width, the good crystallization temperature in the active area of the phase-change material, to achieve at the end of the pulse the final SET state. In this case, the trailing edge can be as fast as in the RESET pulse.

The pulse shape becomes fundamental for the programming of the cell, since the main parameter to play on the material phase-change is the temperature. The temperature in fact, is increased in the device by the current induced Joule heating, and specific pulse shapes, correspond to specific temperature profiles in the cell.

In Fig. 1.5 we report a typical resistance versus programming current characteristic of a PCM device. Each point in the graph corresponds to the final resistance of the memory, achieved after the application of a current pulse of specific intensity. Three main regions are highlighted: READ, SET and RESET. The READ operation enables the sensing of the device, and it has to avoid the disturbing or the change of the resistance state of the cell. Hence, it is performed at low current values. Increasing the programming current the temperature in the cell is risen enabling the recrystallization of the phase-change material, and lowering the final device resistance (SET). When the current intensity allows the partial melting of the phase-change material (melting

current), the rapid quenching allows the amorphisation of part of the material volume, resulting after the pulse application, in an increase of the resistance of the device (RESET). If we consider the characteristics of a device starting from a SET state, and of a device starting from a RESET state, we notice two main differences. The first, is the starting resistance, that is preserved in the READ region. The second is the different resistance achieved in the SET region. In fact, if the device starts already from a SET state, the material does not experience any phase transition till the reaching of the melting current. On the contrary, starting from an amorphous phase, the device, thanks to the crystallization mechanism, decreases its resistance, but this decrease depends as already observed, on the pulse shape (e.g. duration, fall time, etc.). As illustrated in the graph, in this case the pulses applied were not sufficiently long to recover the perfect crystallization of the phase-change material. Once reached the RESET region, the two characteristics overlap, because of the melting of the phase-change material in both cases.

The current as a function of the voltage plots of a phase-change memory (I-V), reported in Fig. 1.6, show the overlapping of the SET and of the RESET characteristics (that corresponds respectively to the device starting from the SET and the RESET state) in the SET and in the RESET range of currents. However, coming from the amorphous phase, only a long persistence in the SET current region, allows the recrystallization of the phase-change material. Moreover, the RESET I-V curve evidences the main electrical property of a PCM device: the switching phenomenon. The RESET device, once reached a critical threshold voltage V_{TH} , with a typical snap back in the I-V curve, switches to a high conductive state (ON-state), with conduction properties similar to the crystalline phase. Once in the ON-state, the heating induced by the increased current, can allow the recrystallization of the integrated phase-change material. The switching phenomenon, is the fundamental property that makes possible the phase transition in a PCM device.

1.3 PCM applications and challenges

Nowadays, an exponential growth of code and data is occurring in all electronic systems. The increasing memory density requirement in embedded applications of the non-volatile memory (NVM) market, made the scaling in the last years a great challenge for researchers and industries. The scaling of the Flash technology in fact, requires to overcome some major hurdles like economic limitations, increasing logic platform complexity, introduction and research of new materials (Hi-k) [12]. New memory technologies, to be competitive with Flash technology, must not only meet power needs but must demonstrate the ability to scale down for more technology nodes. In this context, PCM technology supports the promise of scalability beyond that of other memory technologies, with proven scalability down to the 5 nm node. And this is the reason why, with respect to other resistive memory technologies, it is already an industrial reality in the stand-alone market and first embedded prototypes have been presented. The range of applications in which the PCM technology can be used is wide [3]:

- ultra high-performance memory subsystems to achieve solid state drive (SSD) performance and reliability that is unachievable with Flash NAND and at power

- consumption levels (and nonvolatility) that cannot be achieved with RAM;
- execution memory in embedded systems, thanks to the bit-alterability;
- wireless systems (read latencies are on the same order of magnitude as the latencies of DRAM);
- computing platforms: PCM banks, with respect to DRAM can be turned off when they are not in use to provide reduced power in idle states. They also offer endurance and write latencies that are compelling for this type of application;

Two challenges remain for this technology, to be a valid Flash replacement: the multi-level capability, and the data retention in high temperature environments, like in automotive applications.

1.3.1 The multi-level PRAM cell

One possible direction to increase the effective memory density (number of bits per unit area) is the so called multi-level cell technology (MLC). It exploits the capability of a memory cell to store analog data in order to encode more than 1 bit of digital data per cell [13]. In PCM technology there are some intrinsic factors that limit this multi-level storing:

- the write noise, that increases with the lifetime and the number of cycles, and depends on fabrication variability, phase-change material stability, etc.;
- the recrystallization of the amorphous phase, seen at room temperature as a “long-term” phenomenon in standard phase-change material;
- the drift of the resistance towards higher values, even immediately after the programming (“short-term” phenomenon);

Among these factors, the drift represents the most important to be overcome to enable MLC. In recent years, because of the intrinsic nature of the phenomenon, different solutions have been proposed at system level [14], showing the capability for the PCM technology of multi level storing, at the expense of the reduced programming speed. The reduction of the resistance drift by the engineering of the phase-change material is another solution and the subject of current active research in the PCM research community.

1.3.2 Automotive applications

The problem of the preservation of data and code is not only a prerogative of the consumer market. The increasing number of microelectronic applications in the means of transport raised the demand for memory capability. Automotive applications have different requirements with respect to consumer and industrial applications in terms of reliability:

- from 15 years up to 30 years lifetime (for standard server the requirement is 10 years);

- effective working time $\sim 10\%$ of standard applications;
- working temperature range from $-55\text{ }^\circ\text{C}$ up to $150\text{ }^\circ\text{C}$;
- zero defect requirement.

The automotive environment represents a challenging target for PCM technology, first of all because of the high temperature at which programming operations and storage have to be guaranteed. The only possible way to overcome this limit, is the engineering of the integrated phase-change material and we will see in the next chapter, how our work contributed to the research of innovative phase-change materials, in order to make PCM a valid candidate for Flash replacement, even in this challenging market.

1.4 The phase-change materials

The chalcogen elements belong to the VI-A subgroup of the Periodic Table. These elements are: sulphur, selenium and tellurium. The chalcogens are the basic elements of the chalcogenides compounds. The chalcogenides are compounds of sulphur, selenium or tellurium with electropositive elements or with organic radicals. The name chalcogenide originates from Greek *φαλκοε* (copper) *γεννωω* (born) *ειδοε* (type) and being given initially to the chalcogenide minerals that contain copper in combination with sulphur, selenium and tellurium [15]. Phase-change materials belong to the family of chalcogenides. These materials at room temperature can present the amorphous or the crystalline phase, being the phase transition a reversible process. Hence, the crystallization mechanism becomes fundamental, and its speed impacts the final performance of the device in which the phase-change material is integrated. As we will see later, the crystallization is the result of the combination of two different mechanisms: the nucleation, and the growth. These mechanisms vary dependently on the phase-change material considered. We present here the $\text{Ge}_2\text{Sb}_2\text{Te}_5$ and GeTe , seen as the main phase-change materials used in PCM technology, and starting point of our work.

1.4.1 GeTe

Studied since 1968 [18] for its optical properties, the GeTe represents one of the first example of chalcogen compound that demonstrated a reproducible and controllable phase transition from a low resistive, crystalline and highly reflective state, to a high resistive, amorphous state. At room temperature the crystalline phase has been described as a rhombohedrally distorted Te sublattice phase with some of the Ge atoms misaligned, and a subsequent rupture of certain resonant bonds in the lattice (the bonding is supposed to be resonant with shorter, essentially covalent, bonds and longer resonance bonds formed through the back lobes of the same p orbitals that are used to form the shorter bonds [19]). When we increase the temperature, at around $400\text{ }^\circ\text{C}$, the rhombohedral angle approaches 90° , giving rise to a cubic structure. GeTe is a degenerated p-type semiconductor with the top of the valence band formed by p electrons. In the near-perfect cubic phase all atoms and consequently their p orbitals are aligned, and the resonant-bonding network extends throughout the crystal, while in

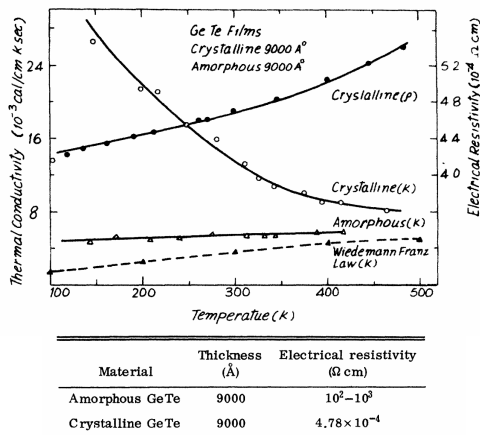


Fig. 1.7. Thermal conductivity vs temperature for amorphous and crystalline GeTe films. In the table are reported the values of the resistivity for both the phases [16].

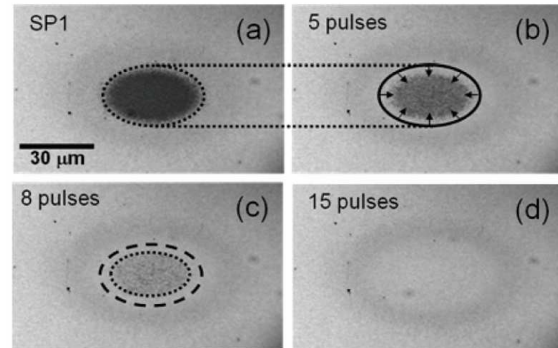


Fig. 1.8. A melt-quenched amorphous spot of GeTe (a), is recrystallized by multiple laser pulses procedure. First pulses (b) demonstrate the growth of the crystalline boundaries. Then, only after 8 laser pulses (c and d), the nucleation takes place in the central part of the spot [17].

the amorphous phase resonance bonding is localized to within fewer interatomic distances. Consequently, the two phases have very strong different electrical and thermal conductivity, as shown in Fig. 1.7.

As confirmed by recent works on GeTe [17, 20], this material is still largely investigated because of its high crystallization speed. Recrystallization provided with fs laser pulses has been demonstrated. Most of the pre-amorphized surface, has been observed recrystallizing starting from the interfaces between the amorphous region and the surrounding crystalline phase. Only in really long crystallization procedures, the nucleation has been observed coupled to the growth process, as observed in Fig. 1.8.

The melting temperature of this compound is around 725 °C [21] while its crystallization temperature is around 180 °C [22]. In the experimental results to evaluate the crystallization temperature, the transition from the amorphous to the crystalline phase is sharp: indeed, once a nucleus is generated during the heating process, it grows really fast. Both in optical and in resistivity measurements, it appears as an abrupt transition of the measured quantities.

1.4.2 $\text{Ge}_2\text{Sb}_2\text{Te}_5$

$\text{Ge}_2\text{Sb}_2\text{Te}_5$ or GST, thanks to its long-term stability at ambient temperatures and its relatively fast crystallization under laser irradiation (50 ns), has been considered, since the beginning of 1990s, as a great material for optical recording. Moreover, its properties made this material the first phase-change material considered candidate for PCM applications. Its crystallization temperature is around 150 °C, while its melting temperature is around 660 °C [23].

The resistivity measurement as a function of the temperature (Fig. 1.9), reveals 2-3 orders of magnitude drop in resistivity that coincides with the amorphous-fcc transformation which is near 150 °C (first transition). This metastable fcc phase transforms

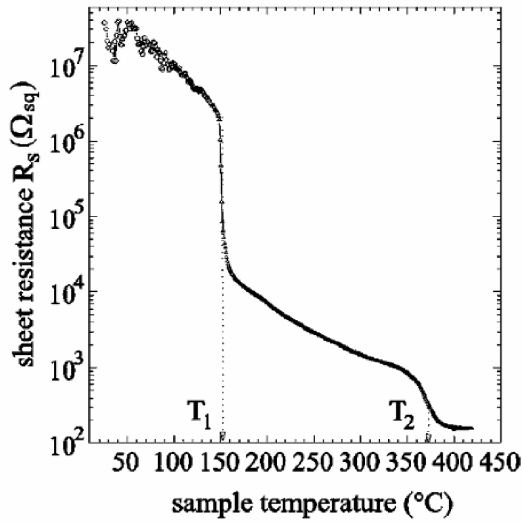


Fig. 1.9. Resistivity of full sheet material of GST, measured during increasing temperature [24]. The two transition amorphous-fcc (T_1) and fcc-hcp (T_2) are evidenced.

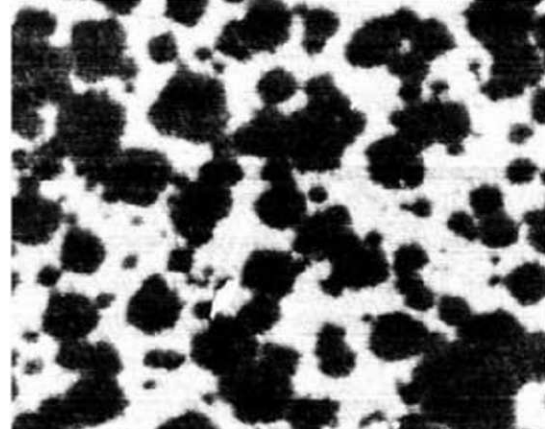


Fig. 1.10. AFM scans of a $\text{Ge}_2\text{Sb}_2\text{Te}_5$ sample surface, during isothermal annealing at $115\text{ }^\circ\text{C}$ for 15 hours [26]. The continuous nucleation observed is reflected in the nucleation-dominated recrystallization.

into the stable hexagonal phase at a higher temperature of $375\text{ }^\circ\text{C}$, which varies depending on the sample characteristics (second transition). The resistivity of amorphous $\text{Ge}_2\text{Sb}_2\text{Te}_5$ exponentially decreases as more carriers are excited at higher temperature, consistently with its semiconductive nature [24]. If it is cooled again, the resistivity essentially returns to its original value. However, the resistivity decrease of a crystalline phase is mainly due to the increase of mobility rather than carrier concentration. Crystal grains grow during heating and the scattering by grain boundaries decreases, increasing the mobility. This decrease in resistivity is irreversible, and the lower resistance persists once the sample is cooled back at room temperature.

The thermal conductivity of GST increases abruptly at $150\text{ }^\circ\text{C}$ (amorphous-fcc transition), while it increases more gradually near $\sim 340\text{ }^\circ\text{C}$ (fcc-hcp transition). The thermal conductivity, during the crystallization process, encompasses the entire range of values from $0.45\text{ WK}^{-1}\text{ m}^{-1}$ up to almost $1.53\text{ WK}^{-1}\text{ m}^{-1}$ [25]. This increase is likely due to the decreased defects density in the crystalline matrix.

Studies on the recrystallization mechanism of amorphous marks upon laser irradiation revealed that $\text{Ge}_2\text{Sb}_2\text{Te}_5$ recrystallizes by nucleation and subsequent growth of crystals inside the amorphous mark [23], being the heterogeneous crystal nucleation the fundamental mechanism that controls the crystallization [26] (Fig. 1.10). The nucleation rate can represent a limit for the amorphisation. In standard $\text{Ge}_2\text{Sb}_2\text{Te}_5$ the highest attainable experimental cooling rate is on the order of 10^{-10} Ks^{-1} (the highest cooling rate depends on the material parameters, and in particular on the thermal conductivity, on specific heat per volume, and on material dimensions). If now we suppose a range of temperatures of 100 K in which the nucleation is favorable, the range of time of the temperature decrease would be on the order of $\sim 10\text{ ns}$. For active volumes typical of a PCM device on the order of $\sim 10^{-23}\text{ m}^3$, the nucleation rate represents a problem if is higher than $10^{31}\text{ m}^{-3}\text{s}^{-1}$, that is the case of GST. What makes possible

the amorphisation of this material, is the existence of an incubation time of the nucleation, independent of the amorphous volume, required for the nucleation process to be stable.

1.5 Crystallization kinetics

The crystallization mechanism impacts many aspects of the life of a final PCM device. It affects in particular the programming speed, and the stability of the amorphous phase. To describe the crystallization process, we refer to the the Classical Nucleation Theory (CNT) developed by Gibbs in 1878. The main hypothesis of this theory are the unchanged composition of the material during the crystallization and the diffusion-limited nature of the process. The free energy of the system, consisting of a cluster of crystalline phase evolving in the surrounding amorphous phase, is expressed as the sum of the bulk contributions of the nucleus and the amorphous phase. These bulk terms are integrated by interfacial contributions, and the main one is given by the product of the interfacial area and specific surface energy. Applying the theory to cluster formation, these surface terms result initially in an increase of the characteristic thermodynamic potential and the existence of a critical cluster size (crystal nucleation). Only clusters with sizes larger than the critical size are capable to grow up in a deterministic way to macroscopic sizes (crystal growth). The change of the characteristic thermodynamic potential resulting from the formation of a cluster of critical size is commonly denoted as work of critical cluster formation. This quantity reflects basically the thermodynamic or energetic aspects of nucleation.

1.5.1 Crystal nucleation

We can calculate the free energy necessary to build a spherical nucleus with radius r , in an amorphous volume. The change of G due to the formation of a nucleus can be written as:

$$\Delta G = \sigma_{ac}A - \Delta G_v V \quad (1.1)$$

where ΔG_v is the difference between the free energies of amorphous and crystal per unit volume of the crystal (i.e., the thermodynamic driving force for crystallization), σ_{ac} is the specific interface free energy of the crystal-amorphous interface, while A and V are the external surface and the volume of the nucleus respectively. This equation has a minimum for a critical nucleus size r_0 , and allows the calculation of the so called thermodynamic barrier of nucleation (W) that leads the crystallization process. W can be defined as follow:

$$W = \Delta G \Big|_{\frac{\partial \Delta G}{\partial r} = 0} \quad (1.2)$$

where r is the spatial variable in a spherical coordinate system. According to the CNT, the steady-state homogeneous volume nucleation rate depends on W according to the equation

$$I_s \propto e^{-\frac{W}{k_B T}} \quad (1.3)$$

where k_B is the Boltzmann constant. Eq. 1.3 determines the number of supercritical clusters formed per unit time in a unit volume of the system in the steady-state condition, and shows how the nucleation is a statistical process with a given probability

distribution function dependent on the temperature. Some time period is needed for the reconstruction of a stable nuclei distribution toward the time independent distribution described in eq. 1.3 at a given temperature T . During this period, the nucleation rate varies and approaches a steady-state value. The time required to establish steady-state nucleation in the system is commonly denoted as the time-lag of the nucleation, or incubation time, that we will take into account later in our simulation tool.

The existence of foreign solid particles, phase boundaries, material interfaces, etc., may favor nucleation. This effect is mainly due to the diminished W , as compared to that of a homogeneous nucleation, owing to a decrease of the effective surface energy contributions to the work of critical cluster formation. This is the main distinguishing feature of heterogeneous nucleation. To estimate the energy barrier reduction, we can multiply W by a parameter Φ that takes into account the surface deformation and varies from zero to one ($W_{het} = W\Phi$) [27].

1.5.2 Crystal growth

Another important mechanism that takes part to the crystallization is the crystal growth and it is driven by the reorganization of the atoms along the crystal-amorphous interface. An atom has to overcome an energy barrier U_B to abandon its amorphous local order and to start to take part to the crystalline order of the neighboring atoms, lowering the energy of the entire system. To describe this phenomenon, we have to consider the contribution of the probability for the atom to rearrange itself in the crystalline matrix, and the probability to come back to the amorphous bond configuration. Subtracting the two probabilities we obtain the final growth speed, that can be written as [28]:

$$v_g = \frac{dr}{dt} \propto \Delta d \left(\nu_c e^{-\frac{U_B}{k_B T}} - \nu_a e^{-\frac{U_B + \Delta G_{ac}}{k_B T}} \right) \quad (1.4)$$

where r is the average radius of the crystalline volume, Δd is the average increase of the radius of the crystalline volume, ν_c is the frequency of the atomic vibration in the crystalline phase, ν_a is the frequency of the atomic vibration in the amorphous phase and ΔG_{ac} is the difference between the Gibbs energies of the two different phases. If we suppose that the atomic vibration at the interface is equal in both phases (γ_a), we can rewrite eq. 1.4 as follow:

$$v_g \propto \Delta d \gamma_a \left(1 - e^{-\frac{\Delta G_{ac}}{k_B T}} \right) \quad (1.5)$$

1.5.3 Overall Crystallization Kinetics

Crystal nucleation followed by subsequent growth results in overall crystallization. This process can be described by determining the volume fraction of the transformed phase, $\alpha(t)$. The formal theory of overall-crystallization kinetics under isothermal conditions was developed in the late 30's by Kolmogorov, Johnson and Mehl, and Avrami and is well known today as JMAK theory. According to this theory the volume fraction of the new phase (crystalline) is given by

$$\alpha(t) = 1 - e^{-g \int_0^t I_{nuc}(t') \left(\int_{t'}^t v_g(t'') dt'' \right)^3 dt'} \quad (1.6)$$

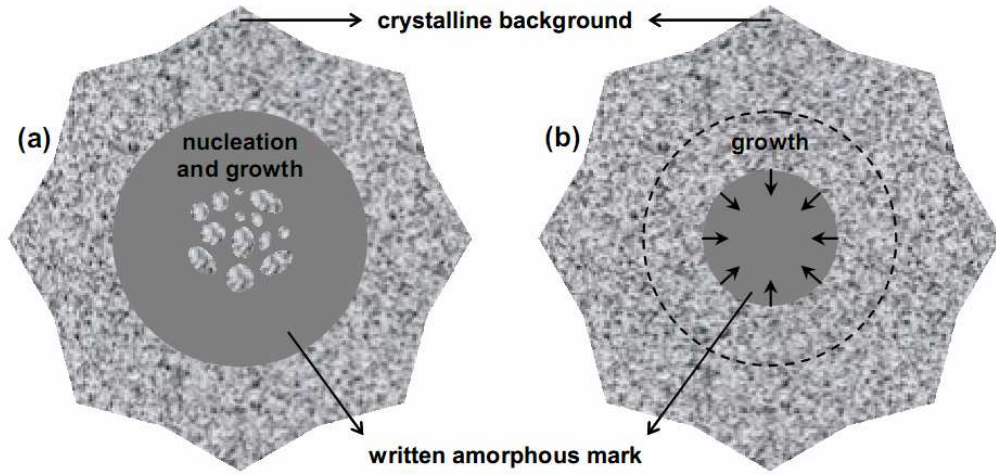


Fig. 1.11. Schematic drawing representing (a) nucleation-driven crystallization and (b) growth-driven crystallization during the laser erasure of a written amorphous mark in a crystalline background [29].

where g is the shape factor, which is equal to $4\pi/3$ for spherical crystals, I_{nucl} is the nucleation rate and v_g is the growth rate. If both I_{nucl} and v_g are constant throughout the transformation (steady-state nucleation) eq. 1.6 can be rewritten as

$$\alpha(t) = 1 - e^{-\frac{gI_{nucl}v_g^3t^4}{4}} \quad (1.7)$$

When the phase-change material presents a crystallization dominated by a really fast growth speed, we can suppose that the number of growing crystals (N_0) and the growing crystalline germs at the crystal-amorphous interface do not change with time and eq. 1.6 transforms to

$$\alpha(t) = 1 - e^{-gN_0v_g^3t^3} \quad (1.8)$$

Avrami proposed that generally the following relation should be used to describe the final crystallization kinetic

$$\alpha(t) = 1 - e^{-Kt^n} \quad (1.9)$$

where the parameters K and n can be estimated by fitting the experimental data of $\alpha(t)$, and are correlated respectively with the rate of nucleation and growth and with the “reaction order” of the crystallization process. The Avrami coefficient n , as observed in eq. 1.7 and eq. 1.8, can give an idea about the final contribution of the nucleation rate and of the growth rate, to the crystallization process. In particular, the transition to a diffusion controlled growth rate and the reduction of the nucleation rate can be concurrent and take to the lowering of n , discriminating between a nucleation-driven (higher n) and a growth-driven crystallization (lower n), situations schematically described in Fig. 1.11. Eq. 1.9 can be considered as the cumulative distribution function (CDF) relative to the probability to have a given percentage of crystalline volume α , after a given time t at a specific temperature [27].

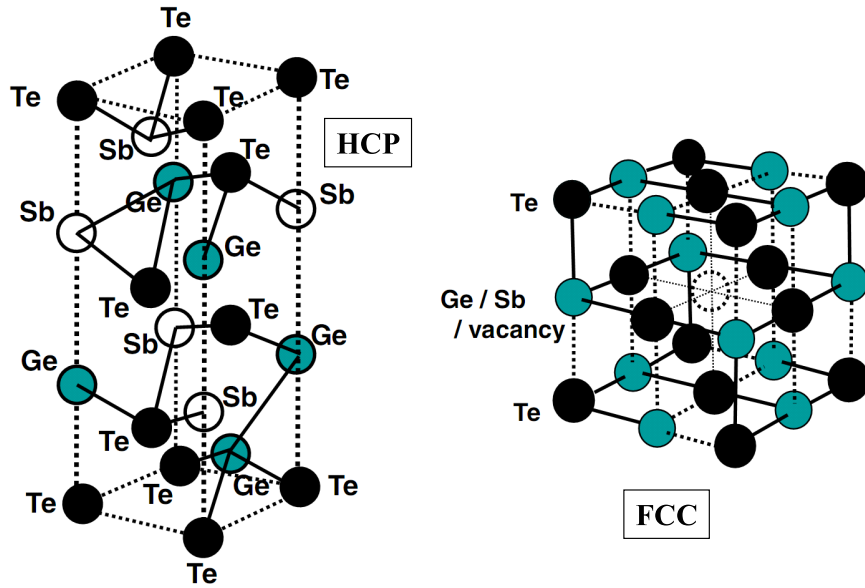


Fig. 1.12. Example of hexagonal crystal structure and fcc-type crystal structure, in crystalline $\text{Ge}_2\text{Sb}_2\text{Te}_5$ [9].

1.6 The crystalline phase

In thermodynamics, a transformation from an initial state to a final state is driven by the Gibbs free energy (G) defined as:

$$G = U + pV - TS = H - TS \quad (1.10)$$

with internal energy U , pressure p , volume V , temperature T , entropy S , and enthalpy H . The Gibbs free energy is the maximum amount of non-expansion work that can be extracted from a closed system; this maximum can be attained only in a completely reversible process. In a phase-change material the crystalline phase has a lower free energy G with respect to the other phases. And then the transition between different states of a phase-change material is like a gradual rearrangement of the atoms moving through metastable states (amorphous, intermediate crystalline phase), till the reaching of a minimum of Gibbs energy. This rearrangement can be achieved, overcoming an energetic activation barrier. The temperature, as we can see from eq. 1.10, plays an elemental role in this mechanism. In fact, the increase of the temperature of the material can boost the crystallization process, giving rise to a number of metastable phases that depends on the elemental composition of the phase-change material.

1.6.1 Structure of the crystalline phase

Speaking about the crystalline phase of a material, we have to refer first of all to the crystal structure. The stable crystal structure of the most common phase-change material, the $\text{Ge}_2\text{Sb}_2\text{Te}_5$, is hexagonal (hexagonal close-packed or hcp) but based on x-ray diffraction (XRD) measurements, it was argued that a layer of GST crystallized by laser beam, possessed the metastable rocksalt structure (face-centered cubic or fcc)

with Te atoms occupying sites on one fcc sublattice with Ge and Sb randomly forming the other fcc sublattice (20% of the sites being vacant), as described in Fig. 1.12 [30]. It was suggested that the cubic structure of GST (which is rather isotropic and hence more similar to the amorphous structure than any other crystal structure) was the reason for the high-speed switching and reproducible performance, since the hcp structure is more energetically expensive to obtain. The presence of vacancies in the lattice, means that covalent bond lengths are slightly different from each other and that the lattice is distorted. In the case of $\text{Ge}_2\text{Sb}_2\text{Te}_5$, there is a low volume difference between the amorphous and fcc-type crystalline state. A possible source of volume increase in the crystalline phase, is the presence of vacancies. A Ge-Te crystal has a rhombohedral structure, which changes into the fcc structure through slight changes in the covalent bonding angle, facilitated at high temperature. This is considered to be the basis of the fcc structure of the $\text{Ge}_2\text{Sb}_2\text{Te}_5$ metastable state [9].

1.6.2 The conduction in the crystalline phase

The electronic properties of the phase-change materials alloys have been studied since the early '70s. These studies showed that these materials present a p-type semiconductor behavior, with very high hole concentrations. The hexagonal structure of $\text{Ge}_2\text{Sb}_2\text{Te}_5$, has a hole concentration of $\sim 3 \times 10^{20} \text{ cm}^{-3}$ and a mobility of $\sim 30 \text{ cm}^2/\text{Vs}$ in thin film form [31]. The mobility is limited by scattering, and is therefore dependent on the microstructure and preparation conditions. The p-type behavior is consistent with the existence of numerous Ge and/or Sb vacancies in the lattice structure. Therefore, it is reasonable to conclude that hexagonal $\text{Ge}_2\text{Sb}_2\text{Te}_5$ is a narrow-gap degenerate semiconductor, where the Fermi level is within the valence band. In fact, because of the numerous vacancies in the crystal structure, there must be a defect band near the valence band, which may overlap and distort the valence band edge. The final conduction is really close to a metallic conduction, or the one of a highly p-doped semiconductor. At high temperature, close to the melting temperature, a high concentration of electrons are promoted to the conduction band (intrinsic conduction), taking part to the final conduction.

The difference in electrical properties between different crystal arrangements, is decided by the presence of excess vacancies [32]. In fcc GST crystal, we have a p-like electrical conductivity, with the Fermi level above the valence band ($\sim 0.15 \text{ eV}$) that gives rise to a semiconductor-like conduction. The higher is the temperature, the higher is the number of electrons promoted in the conduction band, reducing the final resistivity of the material, according to the law

$$\rho = \rho_0 e^{\frac{E_C}{k_B T}} \quad (1.11)$$

where ρ is the resistivity of the material, ρ_0 is a constant, E_C the activation energy of the conduction. There are still some conflicting results on the conduction nature of this phase, but what is well clear, is that it is highly defective. Due to the numerous vacancies, the existence of trap states near the valence band has been predicted, which at sufficient concentration might constitute a defect band [33].

If now a mixture of cubic-hexagonal structures and/or a mixture of crystal compositions exists, the Fermi level fluctuates up and down. This effect makes the resistance

high even in the crystalline phase, being mostly affected by the conduction in the cubic regions. In GeTe, in which the crystalline fcc structure is slightly deformed at room temperature in the rhombohedral configuration, the Ge vacancies generate a really high carrier density, that takes the Fermi level right above the valence band, giving to the material a typical metallic-like conduction [34]. In this case, the resistivity increases with the temperature, because the electronic scattering in the lattice becomes dominant.

The two distinct thermal conductivity mechanisms operative in a phase-change material are the conduction via electron diffusion, and conduction via longitudinal and transverse elastic waves. One can write the total thermal conductivity as

$$k_{th} = k_{th}^e + k_{th}^L \quad (1.12)$$

where k_{th}^L is the lattice thermal conductivity in the absence of electronic conduction and k_{th}^e is the thermal conductivity due to electrons and holes. The electronic contribution to thermal conductivity can be derived from the electrical conductivity using the Wiedemann-Franz law for degenerate crystalline systems

$$k_{th}^e = \frac{1}{3} \pi^2 \sigma \left(\frac{k_B}{q} \right)^2 T \quad (1.13)$$

where σ is the electrical conductivity and q is the electronic charge. In phase-change material where the conduction is assured by high carrier density (i.e. GeTe), the thermal conductivity is dominated by the electronic contribution. When the system is not homogeneous, and dominated by a large number of interfaces between different crystal grains, the main contribution to the final thermal conductivity is given by the lattice part.

Three main contributions are involved in the term k_{th}^L [16]. The first is the phonon-phonon scattering, almost inversely proportional to the temperature. The second term arises because of scattering by impurities and defects. Thin films are, in general, known to have a high concentration of defects and these are likely to produce a significant contribution towards the thermal resistivity. The smaller the ratio of the phonon wavelength to caused the size of defects, the greater is the scattering. Phonons of shorter wavelength (in the range of atomic distances) become dominant as the temperature rises and these are scattered more strongly. Therefore, the resistance caused by defects and impurities increases with temperature. The third term arises because of scattering of phonons at grain boundaries or film surfaces. This term plays the most important role in the case of not fully crystalline films, with amorphous inclusions (or in presence of dopants in the system, that do not take part to the crystallization process).

1.7 The amorphous phase

The word “amorphous” literally means without shape and express the macroscopic atomic disorder of a material. However, if an amorphous phase-change material lacks the long-range translational and orientational order characteristics of the crystalline state, its atomic local order is never truly random in a statistical sense. Amorphous materials are invariably thermodynamically metastable: they generally have a higher

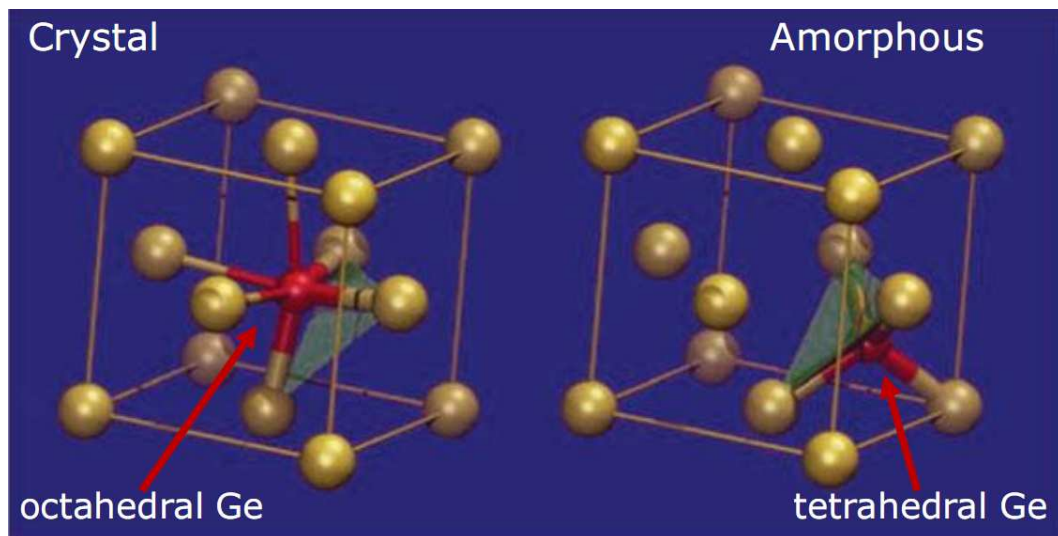


Fig. 1.13. Fragments of the local structure of GeTe/GST around Ge atoms in the crystalline (left) and amorphous (right) states. Upon heating the sample above the melting point, T_m , and subsequent quenching, the Ge atom flips from the octahedral to tetrahedral-symmetry position. Notice that the stronger covalent bonds remain intact upon the umbrella-flip structural transformation rendering the Ge sublattice random [36].

configurational entropy than the lowest free-energy state, the corresponding crystal, and their production is kinetically controlled [35]. We can find two kinds of amorphous phases in a phase-change material: the as-deposited (as-dep) material amorphous phase, and the glassy amorphous phase, obtained by a melt-quench process (melt-quenched). The first one comes from the deposition technique (like sputtering deposition), that doesn't allow for a regular atomic structure of the final phase-change material film deposited. The second one, is the most interesting from the final device point of view. In fact, once reached the liquid phase thanks to the current induced Joule heating of the material, a fast cooling of the material, will freeze the liquid phase preserving its long-range disorder.

1.7.1 Structural properties of the amorphous phase

Considering the GST, it has been demonstrated by EXAFS spectra, that in its amorphous phase both Te-Ge and Te-Sb bonds get shorter and stronger. Through atomistic simulations it has been also demonstrated that the best agreement with experiment was obtained when Ge was allowed to acquire its preferred tetrahedral surrounding in the amorphous phase. This structural transformation is illustrated in Fig. 1.13 where a Ge atom is shown within the fcc structure formed by Te atoms. The Ge atoms occupy octahedral and tetrahedral symmetry positions in the crystalline and amorphous states, respectively. The stronger covalent bonds are shown with thicker lines than the weaker bonds (left) [30].

Sb does not experience any significant changes upon amorphisation (except for the Sb-Te bond shortening) implying that the local arrangement of atoms around Sb remains essentially unchanged. It is believed that the Sb atoms mainly play the role of enhancing overall stability of the metastable crystal structure by participating in the



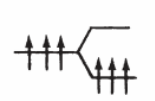



C_2^0	C_3^0	C_3^+	C_3^-	C_1^0	C_1^-
					
$-2E_b$	$-2E_b + \Delta$	$-3E_b$	$-2E_b + 2\Delta$ $+ U_{\sigma^*}$	$-E_b$	$-E_b + U_{LP}$

Fig. 1.14. Charge-defect model based on the fcc type structure and definitions of charge defects [9].

over-all electron balance. In the amorphisation of the material, after the rupture of the weaker Ge-Te bonds, the Ge atoms flip into the tetrahedral symmetry position forming the GeTe_4 tetrahedra. At the same time, the broken weaker Ge-Te bonds no longer counterbalance the Sb-Te bonds on the opposite site and, as a result, the Sb-Te bonds become structure-determining. The structure relaxes making the Sb-Te bonds shorter [36]. This can be interpreted as the local phase separation into GeTe and Sb_2Te_3 phases. Finally, the structure relaxation causes a distortion in the Te fcc sublattice. It is well known that lone-pair electrons (introduced in the next section) subtended at chalcogen Te atoms may play a role in the change of the bonding configuration discussed above.

The nature of the structural transformation discussed, namely the switching of Ge atoms between octahedral and tetrahedral symmetry positions is likely to be common for other phase-change material. In particular, very similar changes in the Ge-Te bond length in the binary GeTe have also been observed.

1.7.2 Band structure and conduction in the amorphous phase

One of the major features of amorphous chalcogenide films is their lack of a measurable density of unpaired spins. The first to explain this phenomenon was Anderson in 1975, who put forward the concept of negative-U (negative Hubbard or negative correlation) energy which implies that two identical charge carriers localized at the same center will attract, in spite of the Coulomb repulsion [37, 38]. Hence, the interactions between the lone-pair electrons generated by chalcogen atoms on different atoms and interactions with their local environment result in localized states in the gap of chalcogenide glasses. This specific interactions between non-bonding orbitals give rise to unusual bonding configurations called valence alternation pairs (VAPs) [39, 40]. To describe the charge defects for a typical amorphous chalcogenide material (C) the subscript number indicates the number of electrons at the bottom energy level [9]. The superscript sign +, - or 0 shows the charge depending on the total number of p electrons. If the total number is four, the charge is 0. C_2^0 for example describes a normal structural bonding (NSB) state having four electrons at the bottom level and one lone-pair. It makes two covalent bonds. C_3^+ describes a defect having three electrons at the bottom level and no other electrons in the upper energy levels. It makes three covalent bonds. All the defect types are described in Fig. 1.14. E_b is the energy cost for a dangling bond. The energy difference between the nonbonding orbital and antibonding orbital σ^* is $E_b - \Delta$

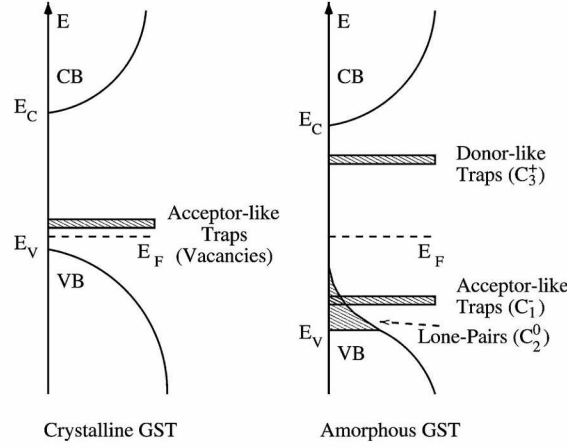
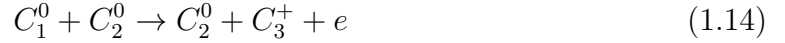


Fig. 1.15. Band diagrams for both the crystalline phase and the amorphous phase of $\text{Ge}_2\text{Sb}_2\text{Te}_5$ phase-change material [28].

where Δ is the antibonding repulsive energy. LP stands for lone-pair electrons.

The presence of Te-Te bonds in the material makes the lattice “flexible” and possible the decrease of the final free energy of the system, by the creation of charged defects (making possible then the conduction). This reaction is initiated by two Te atoms in C_1^0 state and C_2^0 state getting closer. Then the C_1^0 Te atom turns into C_2^0 state and the C_2^0 Te atom turns into C_3^+ state by making a covalent bond between them. This reaction is



One of the electrons moves away and is trapped by another C_1^0 Te atom close to the C_3^+ Te atom, overcoming the Coulomb repulsion force between the dangling bond electrons of the C_1^0 Te atom, which turns into a negative charge defect C_1^- . A pair of C_3^+ and C_1^- defects are then created in the process. In this case, the overall reaction is



The effective electron interaction energy U is $U_{LP} - w$, where w is the energy recovered by lattice relaxation and U_{LP} is the Coulomb repulsion energy. If the lattice relaxation is possible, like in our case, U has a negative value and the Fermi level is close to the center of the band gap, because the increased localized energy levels are lower than the Fermi level. The fact that the valence electrons are nonbonding, allows for the excitation of large free-carrier concentrations without any decrease in structural stability. Amorphous chalcogenide films are expected to have large densities VAPs, and charged centers should very likely be responsible for the observed trap-limited mobility in these materials.

At low applied electric fields, charges generation and recombination can be neglected, which explains the ohmic nature of the amorphous phase-change material at low fields. With increasing field strength, the generation mechanism increases the carriers number, but strong Shockley Hall Reed (SHR) recombination through trap levels inhibits their contribution to the conduction process. At high electric fields we start a saturation of the carrier trapping, due to the decreasing number of unoccupied trap

states. Hence, the generation process becomes dominant, and the number of free carriers increases exponentially, giving rise to an avalanche-like generation phenomenon [28].

In a high trap density environment such as an amorphous phase-change material, the electron transfer (hopping) between two trap states with spatial distance Δz may occur via thermal emission (TE) through the energy barrier (equivalent to the potential barrier) [41]. The exponential electric field dependence of the carrier increase observed experimentally can be described then by the Poole-Frenkel (PF) model. The final current density will obey to

$$J = J_{PF} e^{\beta_{PF} V} \quad (1.16)$$

where J_{PF} and β_{PF} are material parameters and V is the applied voltage. The linear dependence of barrier lowering on the applied voltage can be viewed as the result of the position of the potential maximum between the two trap, that can approximated as

$$\Delta U \simeq -qE \frac{\Delta z}{2} = -eV \frac{\Delta z}{2u_a} \quad (1.17)$$

where E is the electric field, u_a the amorphous phase-change material thickness, and q the elemental charge. To estimate the final current generated in the material due to the electric field application, we have to consider two main contributions. The first is due to the charges activated through the energy barrier between the energy of the trap and the conduction energy band. This current has the same direction as the electrostatic external force applied. The second contribution takes into account the charges that are recombined and jumped back in a trap against the electrostatic force. In this case, the barrier lowering is replaced by a barrier increase of the same amount of ΔU . The net current density generated by the distribution of electron traps above the Fermi level E_F is

$$J = J_0 e^{-\frac{E_g}{2k_B T}} \sinh\left(\frac{qV}{k_B T} \frac{\Delta z}{2u_a}\right) \quad (1.18)$$

where E_g is the energy gap of the material. From this relation we can also understand how the activation energy of the conduction in eq. 1.11 is strictly correlated with the energy gap of the amorphous phase-change material. At low fields in fact, the relation here described can be approximated as a linear dependency of the current on the voltage ($I \propto V$), and calculating the final resistivity through the derivative dV/dJ

$$\rho = \frac{1}{u_a} \frac{dV}{dJ} = \frac{2k_B T}{q \Delta z J_0} e^{\frac{E_g}{2k_B T}} = \rho_0 e^{\frac{E_C}{k_B T}} \quad (1.19)$$

we reobtain the relation valid for a semiconductor with gap energy $E_g = 2E_C$.

1.7.3 The threshold switching of the amorphous phase and the ON-state

As already presented before, at high electric fields, the conduction in the amorphous phase-change material increases really fast achieving current densities suitable for the melting of the material and/or the recrystallization. An intermediate highly-conductive state between the amorphous and the crystalline phase has been always taken into account since the first works on phase-change materials, and called generically “ON-state”

[40]. It is supposed to have the same structural properties of the amorphous phase (it is why it has been called also amorphous-ON phase [42]), but with a strongly increased conductivity. Experimental proofs of this phase have never been found, also because it can be eventually seen only during the dynamic transition of a PCM device, with all the complications related to an observation of a phenomenon that happens in the ns time scale.

In the standard theory, the ON-state is obtained after the crossing of a critical threshold electric field E_{TH} , at which all the traps are filled, and the recombination is strongly reduced (all defects filled) and can only partially balance the generation rate. The system thus reacts reducing the voltage drop to maintain the balance between recombination and generation, leading to the electronic switching. Generation in this regime is sustained by a large density of free carriers, with the electron quasi-Fermi level close to the conduction band edge. In this theory, the electronic switching electric field, can be found in the limit situation in which the density of donor traps (C_3^+) equals the density of minority charges n (electrons). This is considered as a limit situation, since only this charges configuration exists once reached the electric field E_{TH} . From this limit point, the system can evolve to two possible situations: if the current density is not sufficient to sustain the generation rate of majority charges (called holding current density J_H) n collapses and recombination takes place (electrons has not sufficient energy to neutralize C_3^+ traps). If the holding condition is reached, it means that a high density of holes is provided ($p \rightarrow \infty$) and electron and hole lifetimes become equal. Because of the high conductivity of the system, the holding condition can be sustained with a voltage that is lower than the threshold voltage ($V_H < V_{TH}$).

Another theory in recent years has been proposed to explain the threshold-switching mechanism, on the same basis of what already presented above, based on the balance between electron energy gain and relaxation in the hopping transport with the finding of a threshold switching that obeys to a critical electrical power-density condition (P_{TH}) instead to an electric field condition [43]. Different theories have been proposed to explain also the carrier generation mechanism in the amorphous phase-change materials at the reaching of the threshold condition. But the stochastic nature of the threshold mechanism, highlighted in recent years in experimental results [44], does not find a support in the standard theory presented in section 1.7.2.

A completely different theoretical approach has been published recently, and supported in the following years by experimental and numerical results [46, 47]. According to this model, the high electric field induces in the amorphous material a local nucleation, which leads to a gradual formation of a conductive filament made of crystalline nuclei, in perfect agreement with the percolation theory [48, 49]. The free energy of the system experiences a reduction due to the electrostatic energy according to

$$\Delta G_{total} = \Delta G - \frac{\Omega E^2 \epsilon}{8\pi n_p} \quad (1.20)$$

where ΔG is the free energy variation of the system according to the CNT, E is the electric field, ϵ is the dielectric permittivity, Ω is the nucleus volume, and n is the polarization factor that depends on the geometry of the nucleus. The theory takes advantage of the fact that the crystallization is a stochastic phenomenon with fluctuations (i.e. the variance of the nucleation energy barrier σ_W) that depends on

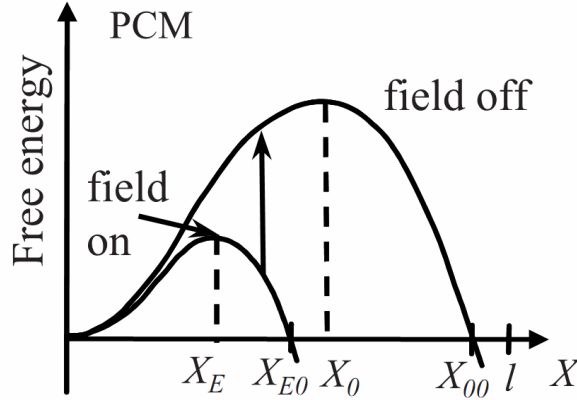


Fig. 1.16. Description of the free energy as function of the nucleus dimension X in the electric field assisted nucleation theory. The application of an electric field E on the amorphous material, decreases the free energy of the system, making possible the nucleation even at room temperature. The nucleus reaches the dimension X_{E0} and then the final stability at X_{00} , stability preserved after the field reduction (holding condition). If the electric field is removed before the reaching of X_0 , even if the filament is already formed, the nuclei formed are not stable and decay spontaneously [45].

temperature and material parameters. Since the activation energy of the nucleation is lower along the interfaces (as seen for the heterogeneous nucleation) is reasonable to think that the first nucleus could appear along these interfaces, increasing locally the electric field on the serial amorphous region. It results in the formation of an electric field assisted filamentary path along the amorphous matrix. The main result of this theory is that the switching is not a threshold phenomenon and can occur statistically with an expected time delay

$$t \propto \tau_v e^{\frac{W_0 E_0}{k_B T E}} \quad (1.21)$$

where W_0 is the nucleation energy barrier at zero electric field, E_0 is the critical electric field at which the formation of stable nuclei can have place, E is the electric field applied, and τ_v is the atomic vibrational characteristic time. This equation allows also to calculate the critical electric field (E_{TH}) (and its statistical distribution) for a given expected time t , that enables the formation of a conductive filament along the material. To maintain a negative difference between the free energies of the system with and without conductive filament an holding voltage is required (V_H). If during the filament persistence (ON-state), the crystallization of the system is not provided (that implies a specific temperature, hence a specific current density), after the voltage removal the filament rapidly decays [45]. It can generate an oscillatory behavior, observed in PCM devices at low programming current.

1.7.4 The stability of the amorphous phase

The stability of the amorphous phase has been deeply investigated in recent years, in particular because it affects the retention of the data stored in the PCM device. Two main mechanisms impact the stability of this phase:

- the thermally activated structural relaxation, that can be experimentally ob-

- served in the increasing in time of the resistivity of the material;
- the recrystallization process, that on the contrary reduces the resistivity of the material.

1.7.4.1 Structural relaxation of the amorphous phase

The phenomenon of the structural relaxation (SR) has been observed in the past in different amorphous semiconductors like Si and Ge [50]. The main macroscopical effect observed as consequence of this phenomenon is the temperature activated increase in time of the resistivity of the material. Even phase-change materials are affected by the drift of the resistivity towards higher values. If this phenomenon in standard PCM devices is not a problem, in highly scaled devices it can represent a problem in terms of reliability and shift of the programming resistance. The physics involved in the drift behavior is still debated. In the past years, several theoretical models have been proposed [51]:

- reduction of the conductivity due to the trap decay, in the trap-assisted conduction model;
- repositioning of the Fermi level by generation of the donor/acceptor defect pairs;
- widening of the energy gap between the Fermi level and the mobility edge, caused by mechanical stress release.

The phenomenon has been observed in as-dep [52] and in melt-quenched phase-change materials meaning that probably all the phenomena proposed have a contribution on the final mechanism and are correlated to each other. Once recovered the amorphous phase in a phase-change material coming from the liquid phase (i.e. through what in a final device is called a RESET operation), the number of dangling bonds varies in time and the structure tends to reach a local order of minimum free energy. The metastable state can relax to this equilibrium state by thermal excitation over an energy barrier (E_B). The average time τ_{SR} needed for the defect relaxation, overcoming the barrier, is assumed to depend on temperature T according to the Arrhenius law [53]

$$\tau_{SR} = \tau_0 e^{\frac{E_B}{k_B T}} \quad (1.22)$$

It is typical that such relaxations exhibit logarithmical slow temporal dependencies of the refraction index, sound velocity, etc., resembling that of the low temperature specific heat and related quantities. The latter are phenomenologically described in terms of random double-well potentials (DWP) [54]. All the models proposed in the literature takes to the same power law empirical dependency of the resistivity on time

$$\rho = \rho_0 \left(\frac{t}{t_0} \right)^\nu \quad (1.23)$$

If we don't assume any electronic phenomenon, in standard DWP theory the drift coefficient ν can be correlated with the intrinsic fluctuation in the material of the energy barrier E_B according to

$$\nu = \frac{u_0 D}{\sigma_{E_B}} \quad (1.24)$$

where u_0 is the dilatation coefficient of the volume of the phase-change material, supposed to vary linearly with respect to the cumulative probability distribution of the relaxation process, and D is the relative change of the Fermi energy level.

After the application of a RESET pulse, the threshold voltage necessary to switch the amorphized volume, increases in time. The evolution in time of the threshold voltage is correlated, like the resistivity, to the structural relaxation of the amorphous material. This phenomenon is called threshold recovery or drift of the threshold voltage. Considering always as hypothesis the DWP theory, we can calculate the equation that describes the drift in time of V_{TH}

$$V_{TH} = V_{TH0} \left(1 + \beta \ln \frac{t}{\tau_0} \right) \quad (1.25)$$

Here V_{TH0} is the value of the threshold voltage at the characteristic time τ_0 (considered the delay time for the activation of the drift phenomenon), β is the drift parameter. Instead, in the trap decay model [10] the threshold voltage as a function of time can be properly fitted with a power law similar to the resistance drift, based on a linear dependence between the threshold voltage and amorphous resistance

$$V_{TH} = V_{TH0} + \Delta V_{TH} \left(\frac{t}{t_0} \right)^\nu \quad (1.26)$$

A natural consequence of eq. 1.26 is that the coefficient of resistance drift and threshold drift necessarily must have the same value for the drift coefficient ν . Both the models have been supported with experimental results, with no real possibility to prefer one with respect to the other [55]. Recently, the trap decay model has been investigated with a more detailed description of the parameter ν [56]. Combining the equation of the conduction of a semiconductor (eq. 1.19) and the empirical equation of the drift of the resistivity in time (eq. 1.23), the drift coefficient has been put in correlation with the activation energy of the conduction, and then with the energy gap of the amorphous material, supposed to evolve in time, with a law that depends on the reading temperature (T_R), the baking temperature (T_B) and the baking time (t_B) of the experiment considered for the study

$$E_C(T_B, t_B) \propto k_B T_R \nu(T_B, T_R) \ln \left(\frac{t_B}{t_0} \right) \quad (1.27)$$

The main result of this study, was the finding that the parameter ν measured during the monitoring of the evolution of the resistivity in time, depends on the experimental conditions, demonstrating how the variation in time of the energy gap of the system can be accelerated increasing the baking temperature, and how this variation can appear different, dependently on the reading temperature [57] (temperature at which is performed the measure of the resistivity, that for reasons related to the experimental procedure, can be different from the baking temperature). In general, if the baking and the reading temperature are equal, we find that

$$\nu = \frac{\Delta E_C}{\Delta E_B} \quad (1.28)$$

that relates the drift coefficient linearly to the variation in time of the activation energy of the conduction ΔE_C . This relation has been deeply demonstrated also in experimental results, for different phase-change alloys, showing a general trend in which low

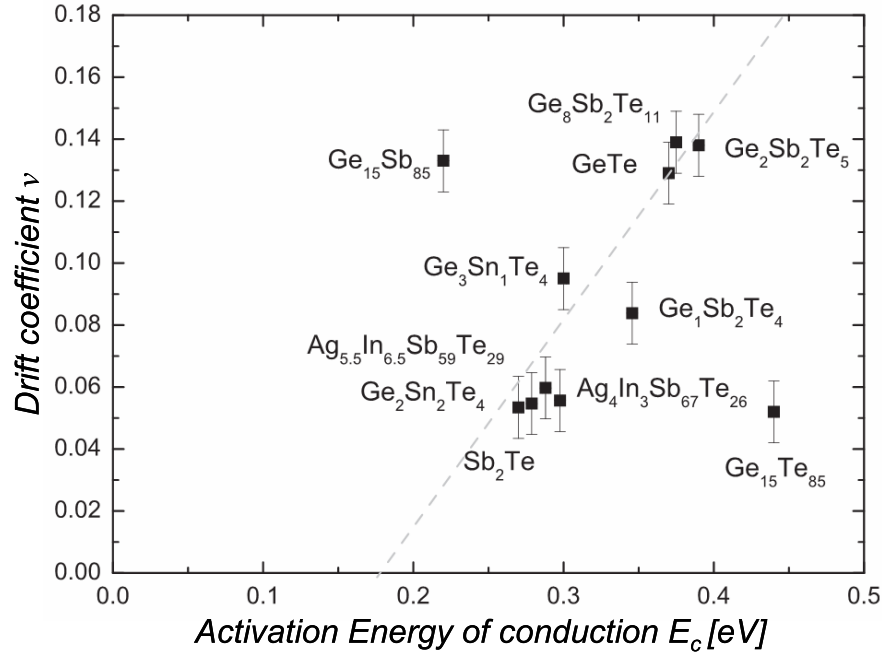


Fig. 1.17. Experimental demonstration of the correlation between the drift coefficient ν and the activation energy of the conduction, for different phase-change materials. The trend observed confirms that low drifting materials are characterized by low activation energy of electronic conduction [52].

drifting materials are characterized by low activation energy of electronic conduction (Fig. 1.17 [52]).

In the model proposed, the variation of the activation energy of the thermal relaxation ΔE_B , has been put equivalent to the activation energy of the crystallization ($\Delta E_B = W_{cr}$). The real correlation between these two parameters has been demonstrated by means of simulations but still no experimental results relates the SR phenomenon to the crystallization dynamics. The resistance dependence on E_C was explained by the disordered nature of the amorphous chalcogenide phase, where the energy barrier for thermally activated hopping is randomly distributed in the amorphous volume. As a result, the current is localized in percolation paths with minimum resistance, hence minimum E_C . For increasing thickness of the amorphous region, E_C increases due to the decreasing probability of finding a favorable percolation path with a low critical barrier. The model gives an explanation also to the reduction of ν when, thanks to the incoming crystallization, the resistivity of the material decreases [57]. In fact, as seen before, lower resistivity means lower amorphous volume and then a reduced E_C (Fig. 1.18).

Still some lacks remain in the comprehension of the drift mechanism, recently correlated with the change of the distribution of the bond angles in the phase-change material amorphous matrix. Atomistic calculation reported that both octahedral and tetrahedral coordinations are present for Ge atoms in $\text{Ge}_2\text{Sb}_2\text{Te}_5$, but the tetrahedral coordination is the majority. The coexistence of octahedral and tetrahedral coordinations of Ge atoms increases the uncertainty of SR and might play an important role in resistance drift of a PCM material [58, 59]. This led to the conclusion that reducing Ge concentration in Ge-Sb-Te ternary alloys leads to a less drift (as we will analyze

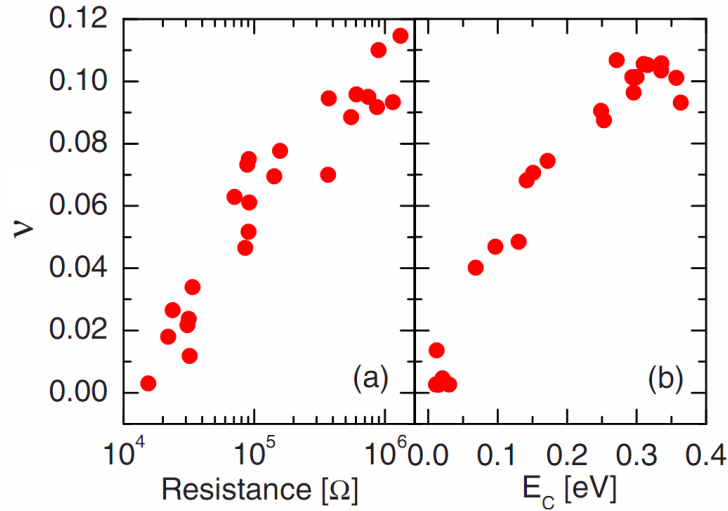


Fig. 1.18. Drift coefficient ν measured and annealed at 300 K (room temperature), as a function of the resistance of the material (a) and as a function of the activation energy of the conduction (b) [57].

later in our experimental results).

1.7.4.2 The Kissinger analysis of the crystallization dynamics

We already presented the amorphous phase as the phase, in which the minimum of the free energy is found recovering the structural long range order of the crystalline phase. The temperature is the fundamental parameter to define the stability of this phase and the characteristic time (recrystallization time) necessary to fully recrystallize the material. The direct study of the crystallization dynamics on full sheet wafers can give a first important sight on the material behavior in temperature. As already presented in the CNT, the nucleation rate and the growth speed depend on the temperature. Both mechanisms are involved when we increase the temperature of the phase-change material, and they contribute to reduce the resistivity of the material sheet. The convolution of the two phenomena, gives rise to a total crystallization dynamics as function of the temperature (presented in section 1.5.3). We can define then a specific temperature at which the complete recrystallization of the material occurs, under given thermal profile and conditions, and that represents for us the crystallization temperature of the material (T_C)

$$T_C = T|_{v_g \otimes I_{nucl} = fast} \quad (1.29)$$

The crystallization temperature of phase change materials tends to vary considerably as a function of material composition. This is not necessarily the temperature at which crystallization is most likely, but instead is the lowest temperature at which the crystallization process becomes “fast” [13]. While the crystallization temperature by itself does not reveal how “slowly” the programmed amorphous state would be lost for slightly lower or much lower temperatures, it sets a definitive and easily measured upper bound on the final data retention vs. temperature curve for a new phase-change material.

Thermodynamics can be used only to calculate the driving force for transformation but it cannot say how fast a transformation will proceed. The study of how fast process

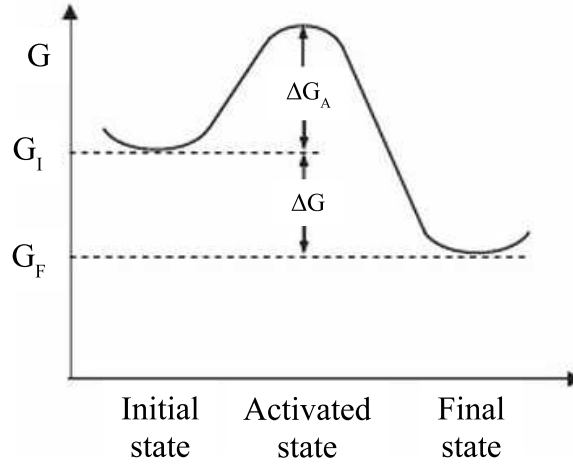


Fig. 1.19. Transformation from initial to final state through an activated state of higher free energy.

occurs belongs to kinetics. In Fig. 1.19 is shown the free energy curve of a single atom, which transforms from initially metastable state into a state of lower free energy. If G_I and G_F are the free energies of initial and final states, the driving force for the transformation will be $\Delta G = G_F - G_I$. However, before the free energy of the atom can decrease from G_I to G_F the atom must pass through a so-called activated state with a free energy ΔG_A above G_I . The energies shown in Fig. 1.19 are average energies associated with large number of atoms. As a result of random thermal motion of the atoms the energy of any particular atom will vary with time and occasionally it may be sufficient for the atom to reach the activated state. This process is known as thermal activation, and the energy barrier ΔG_A is called activation energy of the process [60].

To better qualify the crystallization dynamics of a phase-change material we can extract from the full sheet materials analysis, the activation energy of the crystallization (W_{cr}) through the Kissinger analysis [61, 62]. Applying to the material a ramp of temperature of known increasing rate (v_T), and knowing that the speed of the crystallization depends on the crystalline fraction itself ($\alpha'(t) = \beta(T)(1 - \alpha(t))$), when the crystallization process reaches its maximum reaction rate ($\alpha''(t) = 0$) at the crystallization temperature T_C as defined above, we have the relation

$$\ln\left(\frac{v_T}{T_C^2}\right) \propto -\frac{W_{cr}}{k_B T_C} \quad (1.30)$$

where we have supposed that the speed of the reaction β is temperature activated with the energy barrier W_{cr} , being the reaction under test, the crystallization process.

1.8 The liquid phase

The physics of liquid chalcogenides has not been further investigated in the last years, even if the liquid phase has a key role in the life of a PCM device. Every transition from the crystalline phase to the amorphous phase involves the reaching of the melting temperature T_m in part of the volume of the phase-change material. It has been found from XRD measurements on $\text{Ge}_2\text{Sb}_2\text{Te}_5$ samples [63] that liquid and amorphous phase

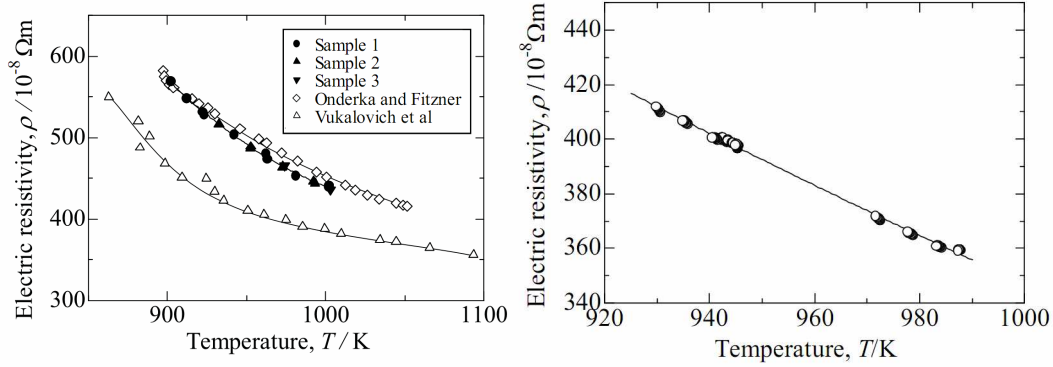


Fig. 1.20. Temperature dependence of electric resistivity of liquid Sb_2Te_3 (left) and GST (right) [66].

are similar in terms of structure, being the liquid phase considerably more structurally disordered. But this disorder observed in experimental results, can be explained by accounting for the diffraction intensity coming from the distribution of valence electrons among the ionic cores. What is supposed, is that in reality the liquid structure, reflects a remanence of bonds and that the crystalline and the amorphous states are the result of a sort of “freezing of this bonds”. Concerning the local structure a remarkable temperature-dependent behavior in the liquid phase of GeTe is found. At temperatures just above the melting point the structure is described to be driven by a reentrant Peierls distortion, exhibiting short and long bonds, similar to the trigonal crystalline ground state of GeTe. This distortion slowly disappears with higher temperatures accompanying a semiconductor to metal transition [64].

One consequence of the transition to the liquid phase is the change of the shear viscosity of the material [23, 65]. Viscosity is a measure of the response of the liquid to a suddenly applied shear stress and is related to the corresponding relaxation time by the Maxwell formula

$$\eta = M_{el}\tau_{stress} \quad (1.31)$$

where M_{el} is the high-frequency elastic shear modulus and τ_{stress} is the average response time of the system to the applied stress. The cooling of the melted volume provides an exponential increase of the viscosity, and the atomic rearrangement to provide a long range order typical of the crystalline phase becomes more and more difficult decreasing the temperature. It means that a critical cooling rate exists (R_c), that must be exceeded to permit the crystallization

$$R_c = \frac{\gamma k_B T_m^2}{V_m \eta} \quad (1.32)$$

where V_m is the molar volume and γ is a constant. This empirical relation embodies the fact that the measured R_c decreases as the viscosity of the melt increases and its specific form is roughly in accord with experiment. The notion of a critical cooling rate implies that it should be possible in principle to reach the recrystallization, from any liquid, but the speed would change dependently on the phase-change material used.

Only in recent years some resistivity measurements have been performed on liquid $\text{Ge}_2\text{Sb}_2\text{Te}_5$ and Sb_2Te_3 (used as phase-change material precursor for GST deposition) [66]. In these studies was found a negative temperature dependence in the electric resistivity of both materials, arguing that they are likely to be semiconductors in their

liquid state (Fig. 1.20). Unluckily, the data published are far from being exhaustive for a perfect understanding of the resistivity transition between the solid state and the liquid phase. What is clear, is that the electrical resistivity of a phase-change material, once reached the melting, decreases drastically with respect to the crystalline phase (e.g. GST has a resistivity of $\simeq 10^{-4} \Omega\text{m}$ in its fcc phase, while this value falls down to $\simeq 3.6 \times 10^{-6} \Omega\text{m}$ in the liquid phase).

The Young's modulus of a phase-change material is directly related to the interatomic energy, which can be determined alternatively in terms of melting temperature. Accordingly, Lindemann law states that the Young's modulus of a solid has a linear relationship with its melting temperature, as follows

$$T_m = \frac{E_Y a^3 \beta^2}{2k_B} \quad (1.33)$$

where a is the lattice constant, β is the critical fraction of the interatomic distance [67]. The melting temperature of a phase-change material affects directly the programming of a final PCM device. In fact, as we will see in detail in the next chapter, the reaching of T_m is provided by the current induced Joule heating of the material and the final programming current will be determined by this material parameter.

1.9 The impact of the phase-change material volume scaling

Nanomaterials have properties that are different from bulk materials of the same composition because surface and interface atoms play an increasing role. The same is true for phase change nanomaterials. It is important to know how phase change properties change with size in order to be able to evaluate the scalability of PCM technology. If PCM cells are scaled down to dimensions where the phase-change material is so small that the properties of the phase-change materials are size dependent these changing properties will modify the final device operation [68]. Scaling studies of phase-change materials have been done on thin films, nanowires, nanoparticles [5, 69], and PCM devices. It was found that many properties of the phase-change materials depend on size, in particular below the 10-nm range. These changing properties include crystallization temperatures and times, related activation energies for crystallization, melting temperatures, resistances, and optical and thermal properties.

It is known that for phase change materials the crystallization is likely heterogeneous, starting at defects which can be located in the bulk, but which tend to be prevalent at the interfaces. If we consider a sheet of phase-change material, as the film thickness d is reduced, the surface/volume fraction of phase-change material decreases, leading to changes in the externally observable crystallization temperature. As experimentally observed, the consequence is that the crystallization temperature can be increased for thinner films, dependently on the crystallization dynamics of the phase-change material used [70]. This increased T_C can be fitted by an exponential function

$$T_C = T_0 + (T_m - T_0)e^{-d/d_0} \quad (1.34)$$

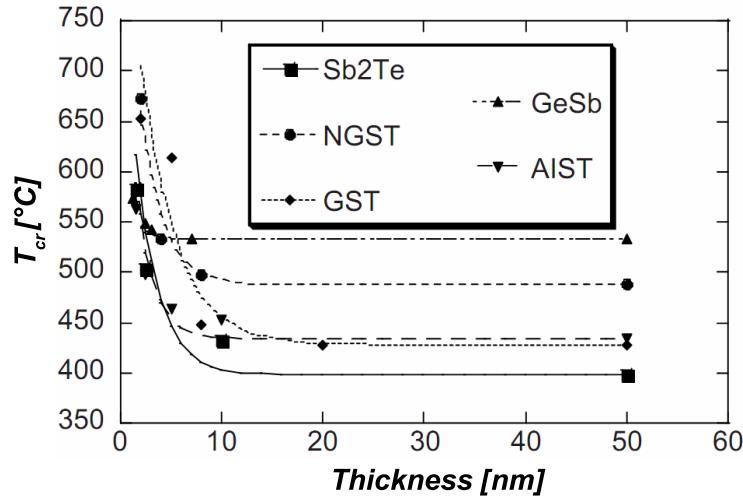


Fig. 1.21. Crystallization temperature T_{cr} as a function of film thickness for different phase-change materials [71].

where T_0 and d_0 are fitting parameters. In Fig. 1.21 we find this relation demonstrated for different phase-change materials. Also melting temperatures are reduced for thinner films which is advantageous because it will reduce the power to melt-quench the material. Moreover, crystallization temperatures can vary by up to 200 °C and can be increased or decreased for very thin phase change films depending only on the interface material, while crystallization times can also be changed (increased or decreased) by changing the interfaces.

In phase-change material nanoparticles, not just one dimension is reduced, but the full volume of the material. In general, large nanoparticles show properties similar to bulk, but the smallest nanoparticles below about 10 nm show size-dependent crystallization, in most cases increased crystallization temperatures, and reduced melting temperature. Both are beneficial for PCM applications and demonstrate the favorable scaling properties of phase-change materials. The ultimate limits of scaling will be reached when materials do not exist stably anymore in both phases. For the GeTe it has been demonstrated that nanoparticles can be synthesized in the amorphous phase and can be crystallized by heating them over their (remarkably increased compared to bulk) crystallization temperature for nanoparticle sizes as small as 1.8 nm (Fig. 1.22).

Down to these small sizes phase-change materials still do not lose their phase change properties. These nanoparticles are as small as about two to three times the lattice constant, so this will be close to the ultimate scaling limit of phase-change technology as far as the phase-change materials themselves are concerned. It demonstrates the great potentiality in terms of scalability of this technology, that makes it a suitable candidate for the new generation of non-volatile memory.

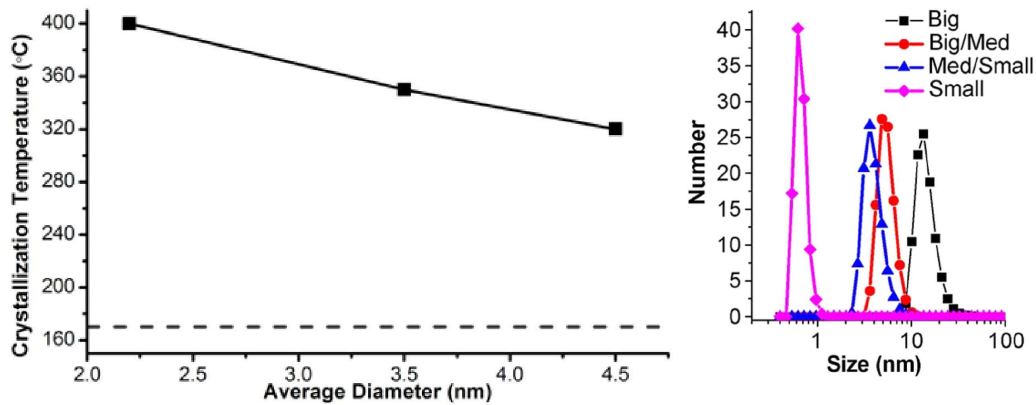


Fig. 1.22. Plot of nanoparticle diameter versus crystallization temperature (left). Crystallization temperature of bulk GeTe is indicated by the dotted line [72]. Size distribution till nm dimension (right) of the synthesized nanoparticles obtained successfully by dynamic light scattering technique [5].

1.10 Summary of the chapter

PCM technology owes its success to the reversible thermal induced transition of the phase-change materials from a low resistive crystalline phase to a high resistive amorphous phase. The basic idea of a phase-change based device, and its intrinsic possibility to store an information, has its origin in the 1960s, when the first patent about a multiple resistance device has been deposited. The PCM cell is a two-terminal device, in which the phase transition is obtained by the current induced Joule heating of the integrated phase-change material. The amplitude of the current in fact, determines the final temperature achieved in the cell, causing the crystallization of the phase-change material, if the temperature is favorable to the crystallization process, and the relative decreasing of the resistance of the device (SET state). If the melting temperature is reached in part of the phase-change material volume, the rapid quench allows the amorphisation of the melted material (RESET state). The key mechanism that makes possible the phase transition in a PCM device is the electronic switching. Once the RESET cell reaches the threshold voltage V_{TH} , the conduction increases leading to the so called ON-state. Only in this conduction regime, the heating of the material is allowed and the phase-change material can be recrystallized.

PCM is nowadays an already confirmed industrial reality. In particular, its scalability beyond that of other memory technologies, demonstrated its suitability for embedded applications. The range of applications in which it can replace the Flash technology is wide like execution memory in embedded systems, wireless systems, and computing platforms. However, the main bottlenecks of this technology remains the stability in time of the resistance state (affected by the drift phenomenon), and the thermal stability of the amorphous phase at high temperatures. These two reliability issues, still prevent PCM to address multi-level applications (to achieve the bit density of Flash technology) and automotive applications (where working temperature ranges up to 150 °C).

The crystalline phase represents the low resistance state of a phase-change material. The nucleation and the growth speed of a material, impact directly the performance of a PCM device, in particular in terms of speed of the SET programming operation. The highly defective structure of the crystalline phase, in some materials like GST, gives rise to a semiconductor-like conduction, demonstrated by the decreasing of the resistivity when the temperature is increased.

The amorphous phase of the phase-change materials has been largely studied, in order to understand the conduction mechanisms, and the origin of the electronic switching. Even if the Poole-Frenkel conduction has been confirmed by different experimental and simulation results, still some debates remain on the origin of the electronic switching. The standard theory attributes this phenomenon to the avalanche mechanism established in the material, when the density of donor traps equals the density of minority charges (electrons). The other theory is based on the electric field reduction of the activation energy of the nucleation.

The third phase of a phase-change material is the liquid phase, that despite its importance in the programming of the cell, has not been largely studied in the literature. We reported the existence of a critical cooling rate that has to be exceeded to allow the crystallization of the material coming from the liquid phase, and the strong increase of the conductivity of this phase with respect to the others, even at temperature higher than the melting temperature.

Chapter 2

The Phase-Change Memory cell: structures and reliability

As already presented in chapter 1, the concept of a resistive memory, is a two-terminal device that in the case of phase-change memory (PCM), consists mainly of a layer of a phase-change material sandwiched between two electrodes. However, despite the simplicity of the basic idea, there are many aspects that have to be considered to realize a final PCM embedded device. First of all, the cell has to allow a current density able to melt the integrated phase-change material. At the same time, the device design has to grant the fast cooling of the material, to enable the melt-quenching. Moreover, in order to embed PCM devices, the possibility to scale the cell (and the device pitch), and the reduction of the power consumption, are basic requirements. Hence, different PCM structures have been proposed to fulfill these specifications, allowing the progressive reduction of the integrated phase-change material volume, and of the final cell dimensions.

The higher is the maturity of a technology, the higher becomes the need to understand and overcome the reliability issues related to the final industrial product. PCM is considered nowadays as the most promising candidate to replace the Flash memory technology in a wide range of applications. However, some bottlenecks remain to make phase-change memory finally suitable for the automotive and multi-level applications. Among them, the most critical remains the thermal stability of the programmed state.

In this chapter, we analyze the phase-change memory cell and its main characteristics. We present the main electrical parameters of the device and we show how the scaling impacts these parameters and the behavior of the cell. Then, the main PCM structures developed in the last years are described, showing their main advantages, and introducing the structures of the devices we implemented to investigate the main reliability aspects of the PCM cell, in particular at high temperature. We describe the characterization system designed and developed to study our devices and finally the simulation tool implemented in order to understand the physical mechanisms that regulate the behavior of the phase-change memory.

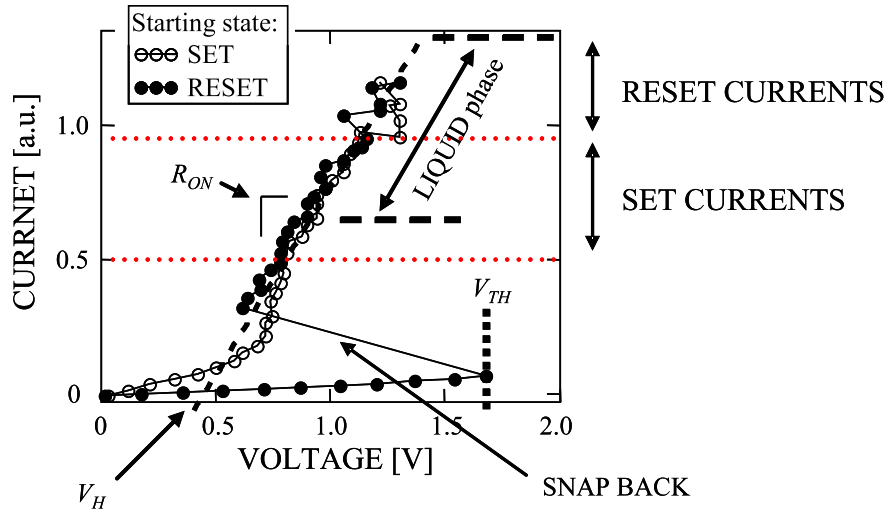


Fig. 2.1. Current-Voltage characteristic of a $\text{Ge}_2\text{Sb}_2\text{Te}_5$ -based PCM device. The starting from both the SET and the RESET state is reported, highlighting the typical electrical parameters.

2.1 The electro-thermal behavior of the cell and the main electrical parameters

As already mentioned, like other resistive memories, the phase-change memory (PCM) cell is a two-terminal device that bases its functionality on the strong difference in resistivity between the crystalline phase and the amorphous phase. Once integrated in a device, all the properties of each phase of the phase-change material have to be taken into account. In fact, these properties give rise to a specific current-voltage characteristic, that depends on the device structure and on the integrated phase-change material. Hence, the need to understand the electrical parameters that have to be considered during the programming of the PCM device.

In Fig. 2.1 is reported the current-voltage characteristic (I-V) typical of a PCM device. When we start with a cell in the RESET phase (filled dots), the increase of the voltage on the phase-change material produces an increase of the conductivity in the amorphous material according to eq. 1.18. It is evidenced in the change of the slope of the RESET curve, at voltages higher than 0.5 V. The reaching of the threshold voltage V_{TH} , produces the switching phenomenon, evidenced on the curve by a snap back. Once reached the ON-state, the device can experience a SET range of currents, in which it achieves a temperature favorable for the recrystallization giving rise after the pulse removal to a SET state. If the current provided is higher than this SET range (reaching the melting current I_m), the phase-change material is likely melted and, dependently on the speed of the pulse removal (trailing edge or fall time), the material can preserve the amorphous structure (short fall time) or recrystallize (long fall time).

Starting from the SET state, we observe again an increase of the conductivity of the phase-change material at voltages higher than 0.5 V, becoming exponential as expected from the intrinsic semiconductive nature of the fcc phase of the $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (section 1.6.2). Then, once highly conductive, the SET state experiences a strong change of the phase-change material structure only when the phase-change material reaches the

melting. We chose to well distinguish the current at which the material starts to melt, and the RESET current threshold. In fact, the liquid phase can be reached in the material even at currents lower than the ones that starts to increase the resistance of the cell. If the area of the plug/pcm interface is not fully covered by the amorphous phase of the material, the conductive paths through the remaining crystalline regions dominate with their low resistive contribution on the final conductance of the device (parallel effect).

To summarize the electrical behavior of the cell, the main parameters that we can extract from the IV characteristic are:

- the threshold voltage V_{TH} : it represents the voltage at which the RESET cell switches to its highly conductive ON-state;
- the RESET current;
- the SET current;
- the melting current I_m ;
- the holding voltage V_H , defined as the voltage drop on the phase-change material in the ON-state;
- the slope R_{ON} , that represents the resistance of the device, once the phase-change material is in its ON-state.

The last parameter R_{ON} , mainly equals the sum of the plug element resistance of the device, and the resistance of the phase-change material not involved in the transition to the ON-state (because of its distance from the plug/phase-change material interface). It means that the plug is the only way to make a PCM device self functional, limiting the current in the device, at the threshold switch event, in the range of the SET currents I_S ($V_{TH}/R_{ON} \simeq I_S$). In the example reported in Fig. 2.1, this is not the case. In fact, the direct application of the voltage on the RESET cell, once reached V_{TH} , would provide a current not sustainable by the device, taking to its degeneration. The memory access device in this case, capable of current limitation (like a MOSFET or a BJT) is mandatory.

From the I-V characteristic we can extract the dynamic equation that describe the drop of voltage on the cell (V_{CELL}) as a function of the current (I_{ON}) during the programming, once the cell is in the ON-state:

$$V_{CELL} = R_{ON}I_{ON} + V_H \quad (2.1)$$

The final power delivered into the device will be then

$$P_{CELL} = R_{ON}I_{ON}^2 + V_H I_{ON} \quad (2.2)$$

In the calculation of the power delivered to the cell, as we see in eq. 2.2, it is important to take into account both contributions from the resistance part (Joule heating), and from the holding voltage. In fact, the latter is the real voltage drop, during the programming, on the the phase-change material layer in the ON-state.

If now we consider the device from a thermal point of view, we can define somehow the thermal efficiency of the cell [73, 74]. When some power is provided to the device, a temperature increase (ΔT) is generated in the phase-change material, with respect to the external temperature, that depends on the structure, and on the thermal conductivity of the materials surrounding the phase-change material active volume. We can define then a general thermal resistance of the PCM cell R_{th} , according to

$$\Delta T = P_{CELL} R_{th} \quad (2.3)$$

The thermal resistance can be seen as the thermal efficiency of the device. In fact, since the power delivered to the cell is used to increment the temperature of the active phase-change material, the higher is R_{th} , the lower is the final power needed to achieve the target temperature increment. R_{th} depends on the thermal conductivity of the materials that surround the phase-change material active volume, and in particular of the plug and of the crystalline phase of the phase-change material, not involved in the phase transition [73].

2.1.1 The plug/phase-change material interface

The interface between the plug and the phase-change material, represents the heart of the phase-change memory. The functionality and the life-time of the device, depends on the quality of the deposition and on the subsequent adhesion of the phase-change material on the plug surface [75]. In fact, this is the region that experiences the highest thermal stress during the cell programming [67, 76]. Moreover, the higher is the scaling of the device, the higher is the quality of the interface required [68].

The temperature profile in the device (at dimensions still far from the atomic size, higher than 10 nm) does not vary with the cell size [74]. If we describe the variation of the temperature in the stationary case with the classical heat transfer equation we have

$$\nabla \cdot (k_{th} \nabla T) + p = 0 \quad (2.4)$$

where p is the power density and k_{th} the thermal conductivity of the materials. Since the power in the cell is generated by Joule heating we can rewrite the equation as

$$\nabla \cdot (k_{th} \nabla T) = -\vec{J} \cdot \vec{E} = -\frac{|\vec{J}|^2}{\sigma(|\vec{E}|, T)} \quad (2.5)$$

where we substituted the electric field \vec{E} with the Ohm equivalence $\vec{E} = \vec{J}/\sigma$, σ being the conductivity of the materials, that is temperature dependent, and in the case of a phase-change material, is also electric field dependent. A first estimation of the solution, considering the problem one dimensional, in the region of the the phase-change material right close to the plug/phase-change material interface [74], takes to

$$\Delta T \propto A_{th} \frac{|\vec{J}|^2}{k_{th}^{pcm}(T) \sigma(|\vec{E}|, T)} \quad (2.6)$$

where we suppose the thermal conductivity k_{th}^{pcm} of the phase-change material dependent on the local temperature reached in the material. The coefficient A_{th} takes into

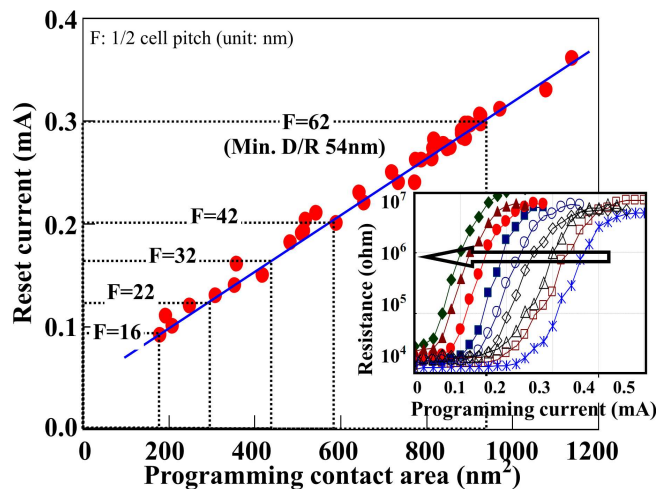


Fig. 2.2. RESET current as a function of the plug/phase-change material area interface [77]. The trend confirms eq. 2.7.

account the efficiency of the cell, that depends on the geometry and on the thermal conductivity of the materials surrounding the phase-change material active volume. As we see from eq. 2.6, to reach a specific temperature in the device, independently of the size, we require a specific J , that in first approximation, depends only on the materials parameters (k_{th} , σ) and on the geometry of the cell (A_{th}). The consequence of the last analysis, is that the surface area (A_{PLUG}) of the plug/phase-change material interface, impacts directly the final programming current (I) of the device. For a given cell structure, and for a given materials choice, known the current density J_R needed to RESET the device, the final RESET current, in first approximation, is fixed by the area scaling:

$$I_R \simeq J_R A_{PLUG} \quad (2.7)$$

This relation has been demonstrated in real PCM devices, to be valid till the 16 nm technology node [77], as reported in Fig. 2.2.

2.1.2 The plug element

The plug is the metallic element of the PCM device, that provides the electrical access to the phase-change material. Its geometry defines the area dimension and geometry of the interface between the plug itself and the active volume. The plug engineering is one of the first subjects to be addressed in the realization of a PCM device. The geometry and the material composition of the plug in fact, impact the functionality and the thermal efficiency of the memory cell. Its resistance has to be matched with the phase-change material resistivity, in order to optimize the position of the peak of the temperature at the plug/phase-change material interface. In Fig. 2.3 we see an example of optimization of the plug [73]. An increase of the plug height with respect to the phase-change material thickness produces a displacement of the peak of the temperature achieved in the device, inside the plug itself, far from the plug/phase-change material interface, decreasing the efficiency of the programming operation. The possibility to find an optimal value for the plug height to improve the cell efficiency, is

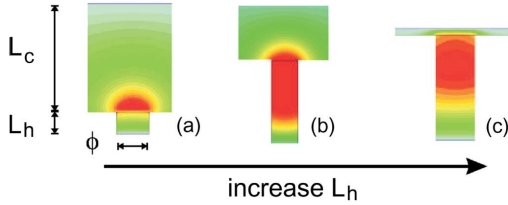


Fig. 2.3. Variation of the heater height and of the phase-change material thickness, in order to maintain a constant SET resistance. The effects on the location of the peak of the temperature reached in the device are evident [73].

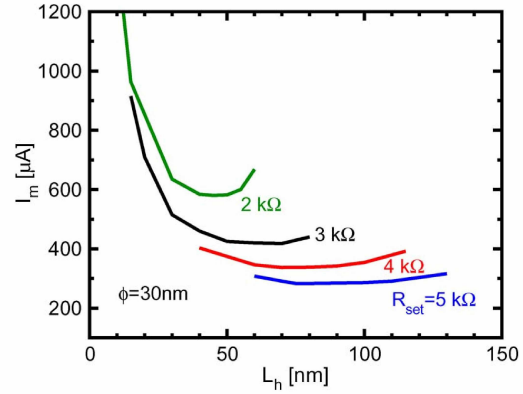


Fig. 2.4. Calculated melting current I_m as a function of the plug height, for a given plug diameter. The thickness of the phase-change material is calculated in order to preserve the SET resistance constant [73].

demonstrated in Fig. 2.4. Here, each curve represents the trend of the current I_m (able to achieve the melting temperature T_m in the phase-change material), as a function of the plug height, keeping the final SET resistance of the device constant. The latter, is obtained varying opportunely the thickness of the phase-change material. Increasing the resistance of the cell, we observe a decrease of the melting current, thanks to the better thermal confinement achieved in the device. The picture shows that for each SET resistance, exists a minimum for the melting current at a specific plug height.

Considering a different optimization approach, keeping the geometry unchanged, we can engineer the plug material. The plug resistance can simply be defined as

$$R_{PLUG} = \rho_{PLUG} \frac{L_{PLUG}}{A_{PLUG}} \quad (2.8)$$

where L_{PLUG} and A_{PLUG} are respectively the plug height and the plug area, and ρ_{PLUG} is the resistivity of the plug material. This resistivity can be engineered in order to make possible the self-limitation of the current in the device, in particular required in memory architectures where the access device does not provide a current limitation (like in cross-bar architectures where the access device is a diode). We suppose to have a defined device structure, with a given plug geometry (A_{PLUG} and L_{PLUG}). To guarantee the SET operation at voltages higher than the threshold voltage V_{TH} , supposing negligible the resistive contribution of the phase-change material volume that does not take part to the phase transition, the following relation has to be satisfied

$$I_S < \frac{V_{TH} - V_H}{R_{PLUG}} < I_R \quad (2.9)$$

In fact, once in the ON-state, the effective voltage drop on the plug is given by $V_{TH} - V_H$. We know from eq. 2.6 that the current densities to SET and to RESET the device, in first approximation, are defined by the geometry and do not depend on the size of the cell. Using eq. 2.8 we can then write

$$\frac{V_{TH} - V_H}{J_R L_{PLUG}} < \rho_{PLUG} < \frac{V_{TH} - V_H}{J_S L_{PLUG}} \quad (2.10)$$

that defines the range for ρ_{PLUG} to achieve the searched limitation. In this approximation, there are some aspects to take into account:

- since the increase of the resistivity of the plug, corresponds to a decrease of the thermal conductivity of the material (as predicted by the Wiedemann-Franz law), we expect a change also of the thermal efficiency of the cell α_{th} of eq. 2.6, reducing the effective J_S and J_R needed to respectively SET and RESET the cell;
- the increase of the resistivity of the plug element to make the device self-current-limiting, rises the final power dissipated in the cell, as showed in eq. 2.2, where in this case the main contribution to R_{ON} will be effectively the plug resistance.

As already anticipated, the plug thermal conductivity can be tuned by material engineering, in order to obtain a better thermal confinement of the cell. Recent works showed also, how is possible to increase the cell efficiency (decreasing the heat loss), by using multi-layer plug structures [78, 79], combining different metals to increase the thermal confinement along the plug direction, placing the peak of the temperature, as much as possible close to the plug/phase-change material interface.

To summarize, the plug element has four main functions:

- define the plug/phase-change material interface area;
- provide the electrical access to the memory cell;
- provide a resistance in series with the phase-change material volume, to limit the programming current;
- contribute to the thermal confinement of the active volume.

Except for this latter point, if the interface area is limited by the geometry structure and the current control is provided by an external MOS selector, the plug resistive contribution can be reduced (i.e. plug removal) reducing the final power dissipated in the PCM device.

2.2 The shrink of the cell

The exponential increase of the systems requirements in terms of memory size, made in the last decades the subject of the scaling more and more addressed. At the same time, if the number of devices per unit area increases, the parallel requirement is the decrease of the programming power of the single device. The maximum memory density achievable, is then one of the first topics that can make a new memory technology attractive for the market. While Flash technology is approaching its intrinsic scaling limit, many demonstrations of the feasibility of the phase-change material scaling have been provided [80, 81], and the scaling has been predicted industrially possible till the 16 nm technology node [77]. However, the decrease of the device size, increases the effects on the programming of the thermal boundaries of the cell. As shown in Fig. 2.5a, the reduction of the cell diameter (ϕ), makes the poor thermal boundary of

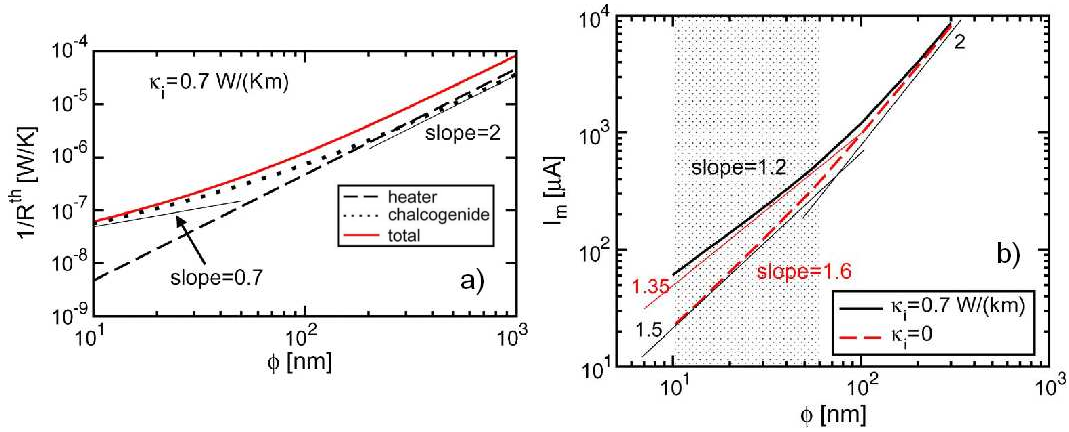


Fig. 2.5. a) Contribution of the thermal conductivity of the phase-change material and of the plug on the total thermal resistance of the cell. The total contribution $1/R_{th}$ is reported as a function of the diameter ϕ of the plug of a lance-type PCM. b) Melting current I_m as a function of the plug dimension [73].

the phase-change material surrounding the active volume, increasingly important on the final thermal resistance of the cell (R_{th}). Moreover, the thermal conductivity of the insulators becomes not negligible. In Fig. 2.5b in fact, the direct proportionality between the melting current (I_m) and the device area ($\propto \phi^2$), is preserved till the 30 nm plug radius dimension. At smaller dimensions, the impact of the low thermal confinement provided by the insulator surrounding the plug element, becomes important [73]. Furthermore, as the characteristic device dimensions approach the phonon and electron mean free paths, ballistic transport effects become increasingly important. The heat generation and thermal-resistance distributions will depend intimately on electron/phonon scattering physics at the interface regions [68]. This effect goes to increase the power density loss in the device. The main consequence of this analysis, is that the scaling to nm size of the PCM device, invalidates eq. 2.7, requiring an increasing current density to RESET the cell. Moreover, the increased current density is detrimental for the lifetime of the device, being higher the thermal stress at the interfaces and in the active volume.

If the melting of the cell can be achieved already in few ns [82], impacted only by the thermal time constant of the system, the crystallization requires a specific time that depends on the nucleation rate and on the growth speed of the phase-change material. A simple analysis, starting from eq. 1.9 gives

$$t_{cr} = \sqrt[n]{-\frac{\ln(1-\alpha)}{K}} \quad (2.11)$$

where t_{cr} is the crystallization time, not dependent on dimensions. What really impacts on the crystallization time, is the increased influence of the interfaces at reduced dimensions. Moreover, the surface/volume ratio becomes more important with the consequent increase of the heterogeneous component of the nucleation. If then the nucleation is boosted, and the growth speed is really high like in “growth-dominated” phase-change material, it leads to a decrease of the final crystallization time.

2.3 The main PCM structures

The scaling of a device is achieved by the improvement of the fabrication techniques, that not always can overcome limitations intrinsic of the lithographic technology available. The other solution is the engineering of the device structure, increasing the possibilities for the scaling, thanks to the changed fabrication procedures involved in the fabrication. Since the beginning of the PCM technology, one of its main bottlenecks has been the high programming current, and all the efforts have been put on the realization of a cell structure, featuring the plug area reduction. In the next sections, we show the evolution of the phase-change memory cell architecture, presenting the main structures proposed in the literature and their evolution in the actual PCM industrial products. In this context, we chose some of them for our implementations, in order to perform our analytical tests and the experimental research of this work.

2.3.1 The lance-type structure

The first PCM cell industrial concept was the one described in Fig. 1.4. The structure is vertical, and basically realized by the etching of a via in the dielectric deposited over the bottom electrode. Then, the via is filled with a metal to realize the plug. The chemical-mechanical polishing (CMP) is performed in order to guarantee the planarity of the surface, for the next phase-change material deposition. The vertical structure, in general, results suitable for the back end implementation in the final memory production. In this structure, the scaling depends on the via diameter ϕ , and then on the etching and lithography technology resolution available. The lance-type structure, from the first implementations based on GST, demonstrated capability of good resistance window (higher than 3 orders of magnitude), high speed (SET time = 40 ns and RESET time = 10 ns), and high cyclability up to 10^{12} cycles [6, 11].

We realized our lance-type structure, using two different lithography techniques, dependently on the via dimension:

- DUV (deep ultraviolet) lithography, for diameters > 250 nm;
- Electronic-beam lithography, for diameters < 250 nm.

In Fig. 2.6 we report the results of one of our lance-type implementation. In the example the plug material is tungsten, with height $\simeq 150$ nm. The dielectric material used is SiO_2 while the phase-change material integrated in the devices is GeTe. The trend of the RESET and the SET currents, as a function of the plug dimension, shows an initial linear dependency on the area of the plug (slope = 2) at plug diameters higher than 200 nm. When we decrease the size, the trend shifts toward a linear dependency on the plug diameter (slope = 1), as already shown in simulations reported in Fig. 2.5.

2.3.2 The edge structure

The edge structure redesigned the plug geometry, taking advantage of the good control offered by the deposition techniques (physical vapor deposition PVD, or chemical vapor deposition CVD) of the thickness of a metal layer. The structure of the cell becomes horizontal. In Fig. 2.7 we report the design proposed in [83], where the interface area, is

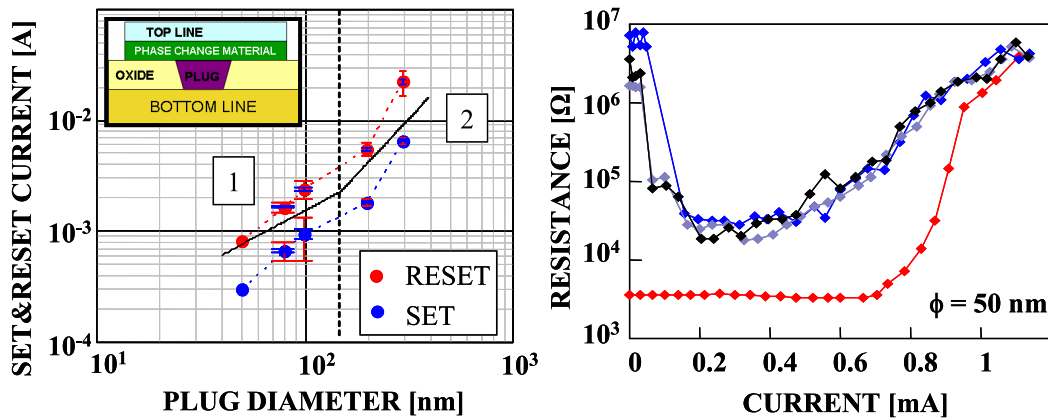


Fig. 2.6. The trend of programming current, in one of our lance-type PCM device implementation. The material integrated is GeTe. On the right, the programming characteristics of a 50 nm (plug diameter) device, showing the possibility to SET and RESET the cell.

defined by the thickness of the horizontal layer (BE), and its width. The phase-change material is deposited in order to have a lateral contact on the exposed surface of the plug. In the picture, we can see also the estimated capability of scaling of this design, with respect to the previous lance-type structure (in which the contact is at the bottom of the phase-change material). However, the main constraint of this architecture, is the difficulty to guarantee a perfect material lateral contact during the deposition.

2.3.3 The bridge structure

The bridge structure consists of a narrow line of ultrathin phase-change material bridging two underlying electrodes [84]. The TiN electrodes are formed very close together to obtain a reasonable threshold voltage, separated by a small insulating gap that defines the bridge length L (Fig. 2.8). Then, the phase-change material is deposited by magnetron sputtering, with thickness down to 3 nm (H), creating the “bridge” between the two electrodes. Electron-beam lithography finally defines the bridge width W down to 20 nm during the patterning step [85]. In this horizontal structure, the rise of the

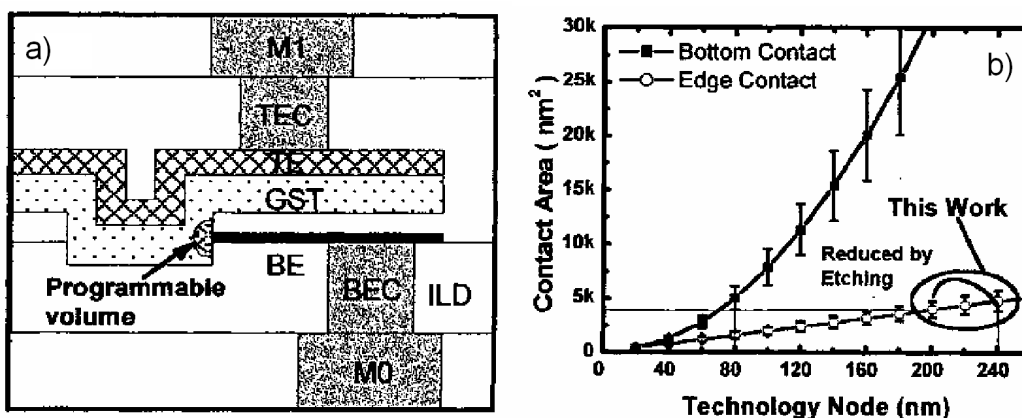


Fig. 2.7. a) Description of the edge PCM structure. b) Comparison in terms of scaling capabilities, between the lance-type structure and the edge structure [83].

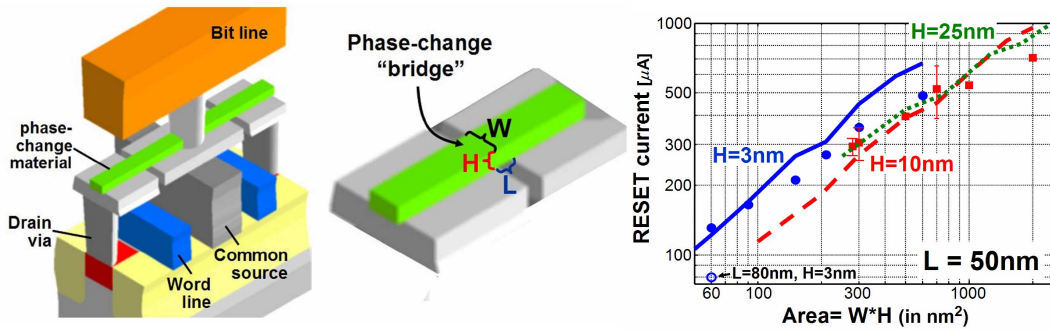


Fig. 2.8. Starting from the left: scheme of the bridge structure, integrated with the selector device; the main concept of the bridge structure, showing the phase-change material bridge, with its dimensions, and the two electrodes; the calculated (lines) and the experimental results (symbols) for the RESET current as a function of the cross-sectional area of the phase-change material bridge, for different thickness H of the phase-change material layer [84, 85].

temperature is inside the phase-change material (self-heating cell), losing the need of a plug element. It means, that the cross-sectional area of the bridge ($W \times H$), determines the final density of current. In Fig. 2.8, the trend of the RESET current of the bridge devices, as a function of the bridge area, still approximately confirms the relation in eq. 2.7. The bridge structure demonstrated great scalability, with RESET current lower than 150 μA , but limited endurance up to 30000 cycles [86].

2.3.4 The confined structure

As already introduced, scaling of vertical structures is limited by the increase of the current density required to program the cell, due to the increased contribution of the lateral thermal dissipation of the structure at low dimensions. The idea of the confined structure, is to “confine” the phase-change material in the same hole realized to implement the plug element, partially or totally replacing it. This enhances the thermal confinement of the active volume, since the power delivered to the phase-change material, is confined by the dielectric. Presented in the beginning as highly scalable architecture [87], it showed a big improvement on the final RESET current of the device, reducing up to more than two times the final programming current, and endurance performance of up to 10^8 cycles. Like for standard lance-type structure, the main limitation of this structure, is the minimum diameter of the via, achievable by the lithographic node. An evolution of this structure is the “pore” structure [88], where the combination of an accurate etch-back and conformal deposition creates a via with a sub-lithographic critical dimension that is essentially independent of the original via feature size. This technique allowed the reduction of the via (pore) diameter down to 20 nm. The main constraint of this technology is the perfect filling of the via (or of the pore), with the phase-change material, achievable only with more conformal deposition techniques like CVD (with respect to PVD), that depends also on the aspect ratio of the pore to fill (ratio between the pore/via height and its surface).

In recent years, Samsung demonstrated the high scalability of this structure down to sub-20 nm technology node, but abandoning the cylindrical shape of the via, and using a “dash” confined structure [89, 90]. Preserving the main idea of the confined structure, the plug is realized with a dash shape, filled with the metal. Then the recess of the plug,

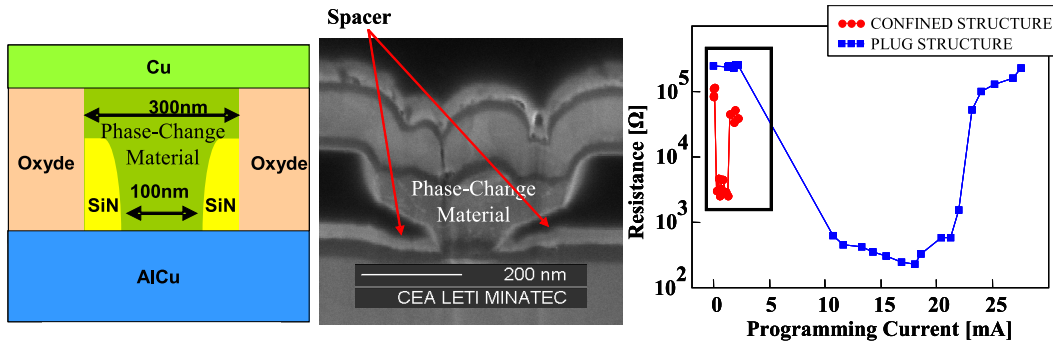


Fig. 2.9. Implementation of the confined structure. On the left the device basic structure. In the center, the SEM photo of our confined structure after the fabrication. On the right, the programming characteristics of a lance-type device with plug of 300 nm of diameter, and a confined structure realized with the same hole of 300 nm, but decreased by the SiN spacers to a 100 nm via.

allows the deposition by ALD (atomic layer deposition) of the phase-change material, in the “dashed hole” left. The result is a structure with a final plug/phase-change material interface area of 7.5×17 nm, RESET current below $80 \mu\text{A}$, and endurance up to 10^{11} cycles.

The confined structure is interesting for the better thermal confinement (increased power efficiency), and the fact that the current density determined by the plug surface is uniform in the phase-change material, even far from the plug/phase-change material interface, gaining again in power efficiency. But this latter consideration, leads also to the fact, that once reached the critical current density required to melt the phase-change material, all the volume of material is involved in the melting. The consequence, is the difficulty to achieve intermediate resistive states between the full SET and the full RESET of the device. In the structures described before in fact, the current density decreases in the phase-change material moving from the plug/phase-change material interface to the top electrode. It means that a proper control of the current density, can change the total volume of phase-change material involved in the melting (that crosses T_m). It results in the possibility to program the cell in different intermediate resistive states, by controlling just the amplitude of the electrical pulse applied on the cell. In the confined structure, this resistance control can be achieved only by partially recrystallizing the melted phase-change material at the end of the programming procedure, requiring a better control of the electrical pulse shape applied on the cell.

In our study, we implemented the confined structure, using a process flow similar to the one implemented for the lance-type, but using the spacer technique. Once created the 300 nm via by DUV, instead to fill it with the plug material, we deposited a uniform layer of silicon nitride (SiN) thick $\simeq 100$ nm, after etched vertically and anisotropically for a total thickness of 100 nm. The result, is a SiN spacer at the bottom of the via along the dielectric border, with the main function to create a pore of 100 nm of diameter. In Fig. 2.9 we report the scheme of the final confined cell, where we deposited GeTe as phase-change material and where the SiN spacers are evidenced. In the picture are reported also the programming curves of the device, compared with a standard lance-type structure with 300 nm plug. The RESET current results strongly decreased (down to 1.5 mA), and as previewed, the RESET and the SET state are achieved abruptly, without intermediate resistance states.

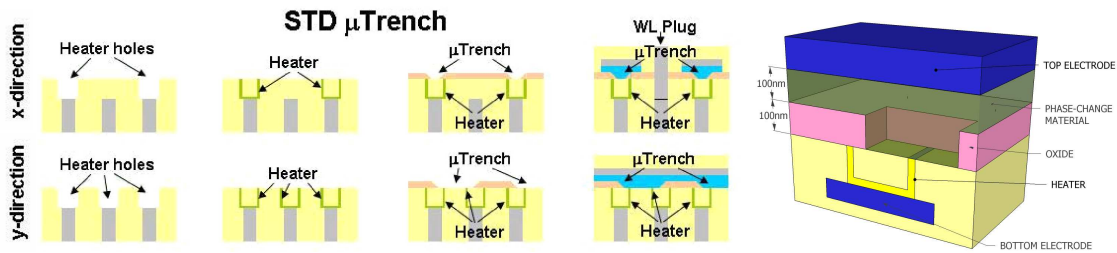


Fig. 2.10. PCM μ trench structure process flow as described in [91] (left). The scheme of the μ trench cell we implemented, showing the trench filled with the phase-change material, and the ring exposed surface (right).

2.3.5 The μ trench structure

The μ trench PCM cell architecture represents a well-tempered merging of all the appealing features of the PCM technology, having been demonstrated to simultaneously achieve low programming currents, small cell size, good dimensional control, and proven multi-megabit manufacturability [91]. Presented for the first time in 2004 by STMicroelectronics [92], it represents the first real industrial PCM product. This vertical structure combines the control of the thickness of a metal layer to define one plug dimension (like in the edge structure), and the critical dimension of the lithographic node used.

We implemented this structure in order to study the effects of the scaling and at the same time the reliability of this technology. The main process flow is described in Fig. 2.10 [91]:

- deposition of the bottom electrode and of the dielectric (SiO_2);
- opening of a squared via in the dielectric by DUV;
- deposition of the metal (WSi) layer by PVD, to create the so called “ring”;
- deposition of the dielectric to fill the via, and final CMP to leave the “ring” surface exposed;
- deposition of the dielectric (SiN);
- opening of the trench by etching of the dielectric;
- deposition of the phase-change material;
- deposition of the top electrode.

In this structure the interface area is defined by the ring thickness, and the trench width. In Fig. 2.11 this concept is well described in the SEM top view image of the cell, before the phase-change material deposition, where both the trench and the ring thickness are highlighted and describing the final surface area of the plug of the PCM device. In Fig. 2.12 we report the trend of the RESET and the SET current as a function of the trench width, for the same ring thickness (30 nm). The linear trend confirms again the linearity between the programming current and the effective area of the plug/phase-change material interface, predicted in eq. 2.7.

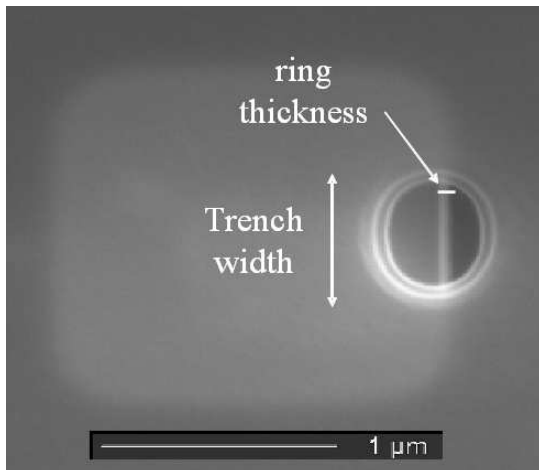


Fig. 2.11. SEM top view image of one of our μ trench devices, before the phase-change material deposition. The final plug surface is defined by the ring thickness, exposed by the trench, and by the trench width.

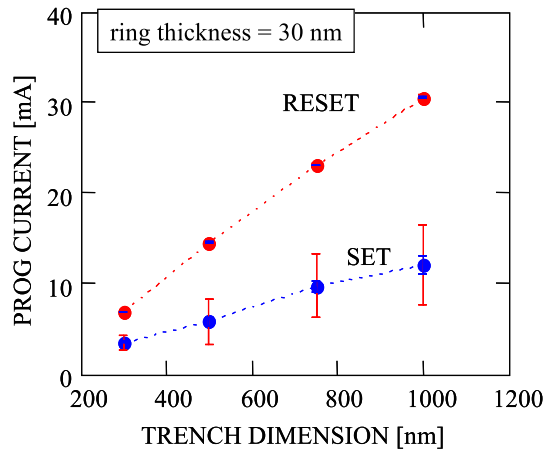


Fig. 2.12. Trend of the RESET and SET current in our μ trench devices, as a function of the trench dimension, for a fixed ring thickness (30 nm).

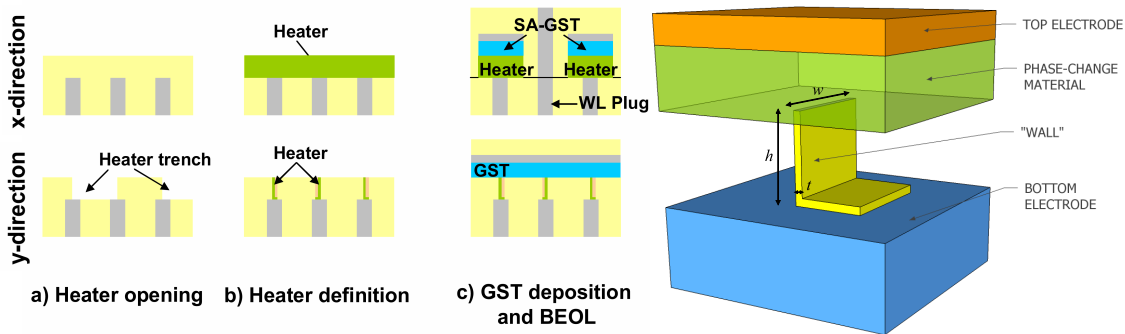


Fig. 2.13. PCM “Wall” structure process flow as described in [93] (left). The basic scheme of the “Wall” structure, evidences the structure of the plug (right).

The main resistive contribution of the plug to the programming of the cell (R_{ON}), in this structure, is in the regions really close to the plug/phase-change material surface. In fact, moving from this surface into the ring, the current density decreases rapidly, due to the larger effective area of the ring, below the trench. It means, that the engineering of the plug, to achieve the correct R_{ON} to allow SET and RESET operations (without the need of an external selector device to limit the current), becomes difficult. Nevertheless, a great advantage of the μ trench structure is the really fast programming operations, thanks to the fact that the peak of the current density is always at the plug/phase-change material interface during the programming, and the reduction of the power lost in the plug. However, the co-integration with a MOS selector becomes necessary.

2.3.6 The “Wall” structure

The “Wall” structure represents the direct evolution of the μ trench technology. With respect to the μ trench approach, the “Wall” structure has better lithographic alignment

tolerances, still preserving the good programming current controllability, and it allows to save one critical mask, simplifying the storage element process integration [93]. The basics of the process flow are reported in Fig. 2.13. From a functional point of view, this structure enables a better engineering of the cell with respect to the programming operations. In fact, the resistance of the plug (called also wall in this structure) can be simply calculated as

$$R_W = \rho_W \frac{h}{wt} \quad (2.12)$$

where ρ_W , h , w , and t are respectively the resistivity, the height, the width and the thickness of the wall. The analysis of the structure efficiency (reported in [94]), as already introduced in section 2.1.2, shows that the increase of the heater resistance (obtained by scaling down w and t and increasing h) to achieve a better control of the current in the cell, produces a displacement of the temperature peak inside the plug, with a consequent reduction of the power efficiency of the device. The scaling of cell then, has to be coupled to a proper selection of the properties (thermal and electrical) of the integrated phase-change material. As we will present in the next chapter, we performed our reliability studies on state-of-the-art “Wall” PCM devices fabricated in collaboration with STMicroelectronics.

2.3.7 The PCM structures: a comparison

In table 2.1 we report all the main advantages and disadvantages of the structures analyzed. The evolution of the cell architecture along the years, led to the progressive scaling of the plug/phase-change material interface area. It allowed to reduce the final programming power of the device, opening the road for PCM technology towards embedded applications. As we can see from the table, the vertical structures showed more advantages in terms of fabrication, being suitable for the back end of line production. In terms of thermal confinement of the phase-change material and reduction of programming current density, the confined structure represents the best solution. On the contrary it requires highly conformal deposition techniques. In order to improve the speed of the device, the current density increase provided strictly at the plug/phase-

Structure	Main features	Advantages	Disadvantages
Lance-type	vertical, plug based on a via	simple manufacturing, high endurance (10^{12})	scaling limited by lithography resolution, bad thermal confinement
Edge	horizontal, plug based on a metal layer	surface defined by plug thickness	difficulty to guarantee good lateral contact
Bridge	horizontal, self-heating cell	no need of a plug element, good thermal confinement	difficult implementation, poor endurance
Confined	vertical, active material deposited in the plug hole	good thermal confinement, high scalability	need of highly conformal deposition techniques
μ trench	vertical, active area defined by ring thickness & trench lithography	temperature peak at the plug/pcm interface, power reduction	no self-current limitation, need of external MOS selector
“Wall”	vertical, active area defined by “wall” surface	good current control, simple industrial process integration	X

Table 2.1. Comparison of the different PCM structures analyzed. The Wall structure results nowadays the best compromise in terms of fabrication process flow complexity and scaling capability.

change material interface in the μ trench structure represents a great solution, also in terms of programming power reduction. However, the absence of a real current limitation requires an external limitation provided by an access transistor, not suitable then for cross-bar applications. The best compromise in terms of fabrication process, scaling capability and device engineering opportunity, is the “Wall” structure, that represents nowadays the state-of-the-art of the industrial PCM products.

2.4 New PCM concepts to scale the dimensions: the μ ring structure

Some of the PCM structures presented before (i.e. “Wall”, confined), have already been integrated in final industrial products. But even if their scaling have been demonstrated almost down to the 10 nm technology node, to achieve higher device density and lower power consumption, new concepts and new design approaches for the cell structure are still one of the major topic of investigation. In this light, we proposed and studied an original different solution, that can be suitable also for the analytical study of new phase-change materials: the μ ring structure.

The μ ring structure is similar to the μ trench regarding the first steps of the process flow, till the CMP process to leave the “ring” surface exposed. Then after:

- lithographically masking of part of the ring (made in TiN) surface;
- recess of the exposed ring by TiN etching;
- stripping of the residual resist mask;
- deposition by CVD of a dielectric (SiN) layer, with the main goal to isolate the recessed cavity;
- CMP process to remove superficially the dielectric, with the goal to expose the ring surface not recessed (μ ring);
- phase-change material deposition;
- top electrode deposition.

In Fig. 2.14 we report the description of the process flow, and a SEM top view image of the μ ring device after the ring masking, where the final dimensions of the plug (called μ ring because it is obtained by the reduction of the ring surface) are highlighted. In particular we defined with w and t respectively the width, the thickness of the plug, and with h the height of the plug, equivalent to the effective length of the recessed region.

In order to understand the main features of this structure, we performed 3D simulations with FlexPDE tool, solving the heat diffusion equation and the continuity equation in the stationary case (the main equations and parameters are analyzed in section 2.7), but without the implementation of the crystallization mechanism. The main goal was to have a first idea of the impact of the scaling of this structure on the final programming performances. The phase-change material considered is the GST.

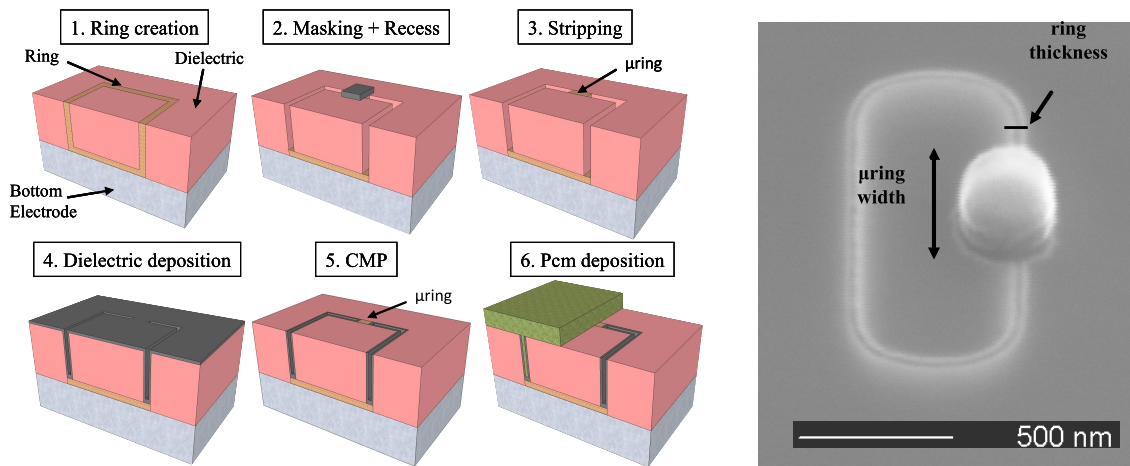


Fig. 2.14. Description of the process flow to fabricate the μ ring structure. On the right the SEM top view image of the μ ring cell, after the ring masking, where are highlighted the final dimensions of the plug (μ ring).

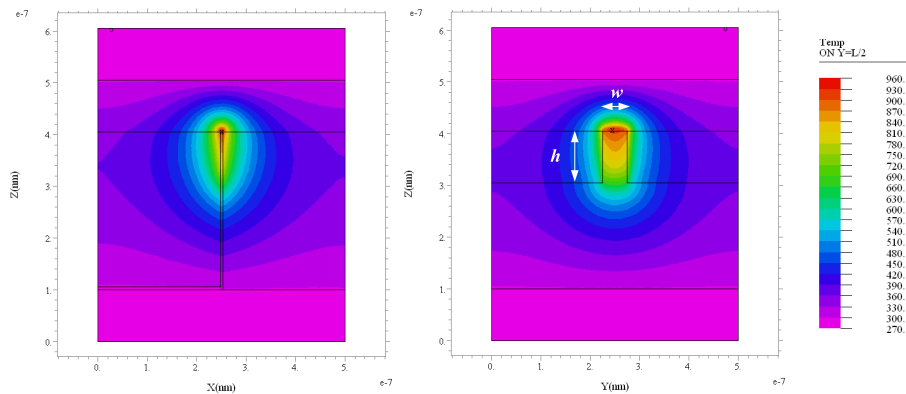


Fig. 2.15. The output of the 3D simulation of the temperature profile in the μ ring structure.

In Fig. 2.15 is reported an example of the simulations performed, showing the profile temperature achieved in the device during the RESET operation. As we can see we supposed a uniform recess of the ring.

The thermal isolation of the cell, as already observed before, is important to reduce the programming power. We simulated the device, considering two different dielectrics: SiO_2 ($k_{th} = 1.4 \text{ WK}^{-1}\text{m}^{-1}$) and SiN ($k_{th} = 22 \text{ WK}^{-1}\text{m}^{-1}$). The results on the current density to RESET the cell are reported in Fig. 2.16. Here the thickness and the height of the plug are kept constant, while the width of the plug is varied. First of all, we observe an increase of the current density, when the surface area scales down (as already observed before in other structures). At the same time, the use of a dielectric with higher thermal conductivity (i.e. the SiN), increases the final current density needed to achieve the same temperature variation in the phase-change material. Moreover, as the device area scales, the temperature peak reached in the phase-change material, approaches the plug/phase-change material interface (Fig. 2.17), allowing more efficient programming operations.

The optimization of the temperature control in the phase-change material, can be achieved increasing the μ ring height. In Fig. 2.18 we show that keeping constant the

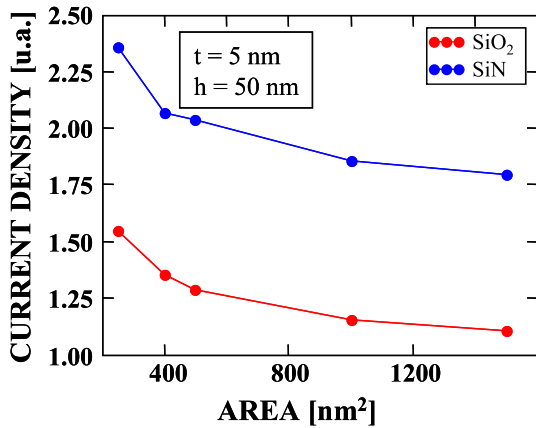


Fig. 2.16. Simulated current density as a function of the plug surface, for two different dielectrics used for the device fabrication.

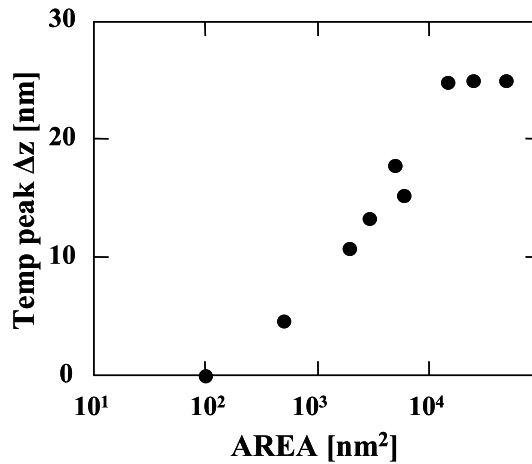


Fig. 2.17. Displacement of the peak of the temperature over the plug surface (inside the phase-change material) as a function of the plug surface resulted from the simulations.

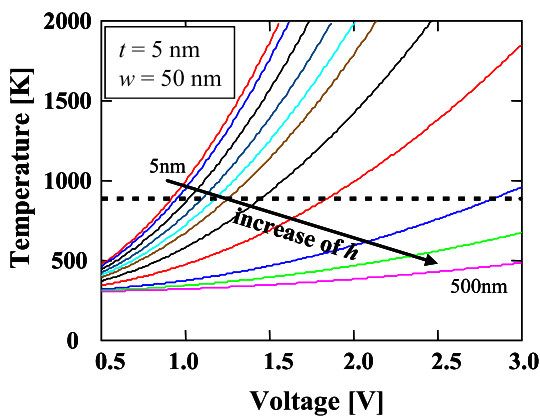


Fig. 2.18. Simulated maximum temperature generated at the plug/phase-change material interface, as a function of the voltage applied on the cell, for $w = 50 \text{ nm}$, $t = 5 \text{ nm}$, and for different values of the ring recessed height h (from 5 nm up to 500 nm). The melting temperature of the GST is evidenced (dashed line).

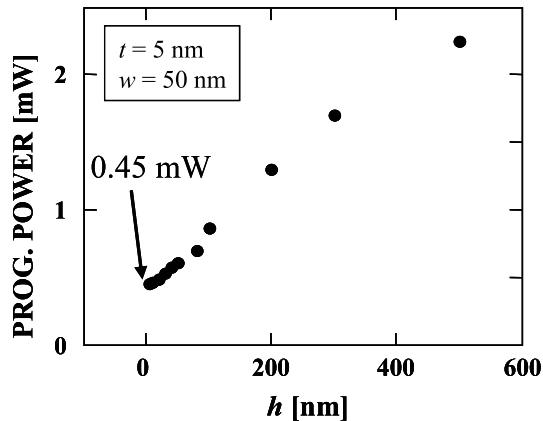


Fig. 2.19. Power to melt the phase-change material in the plug device, as a function of the plug height h . The plug thickness and the plug width are kept constant. The higher is the plug, the higher is the power dissipated in the device.

plug area (250 nm^2), the increase of h , enables a more gradual raise of the temperature in the device. In particular, thinking to a 3 V powered device, and considering as an example a threshold voltage of 1.2 V (like in GST based PCM), the choice of h should be of $\sim 200 \text{ nm}$ (in the graph reported with the blue curve). In fact, for this height of the plug, the temperature excursion from the ambient temperature (300 K) and the melting temperature of the considered phase-change material (dashed line), is perfectly covered from 0 V up to 3 V. If this solution can make the device “self-controlled”, without the use of an external current limitation, at the same time, the increase of the height of the plug, rises the final power dissipation in the cell. The latter, is confirmed in Fig. 2.19, where the plug height is varied, keeping constant the plug area,. The y-intercept calculated from the linear interpolation of the data (y-intercept = 0.45 mW), represents the real

power needed to melt the phase-change material. If now we consider the solution proposed before, with a plug height of 200 nm, we have an increase of 85% of the total power needed to melt the phase-change material, power lost in the plug element.

At the time of the writing of this work, the last steps for the device fabrication of this structure are still ongoing, preventing us to report the final electrical result on these devices. It represents then, the starting point for future works and analysis.

2.5 The electrical characterization of the PCM cell

The study of the electrical behavior of highly scaled PCM devices and the evaluation of their performance, implies the use of equipments that enable pulse width of few ns, with high output slew rate. The latter is fundamental to allow rise and fall times of few ns to quench the phase-change material, once melted, in the amorphous phase. At the same time, since a PCM device can have a resistance window wide up to 5 orders of magnitude, the sensing of the cell has to guarantee a high accuracy in all the possible resistance states in which the cell can be programmed. Many experiments need also a large number of tests on an equally large number of devices, in order to achieve a statistically relevant information on the phenomenon observed. This leads to the need of a fast and fully automatic characterization system. Moreover, all the characterizations performed at high temperature, have to guarantee the same order of reliability as the ones performed at room temperature. In the following sections we will introduce our devices and the setup used for our analysis. We will focus then on two main reliability issues typical of a memory device, and the procedures used during our tests to evaluate these aspects in our phase-change memory devices: the cycling endurance of the memory, and the retention of the information stored.

2.5.1 The device

The analytical devices under test have been designed to provide full access to the top and bottom electrode of the dual terminal cell. In order to perform a sufficiently accurate sensing of the device, excluding all the resistive contribution from the access lines, we enabled 4-probe measurement (Kelvin sensing) adding two access lines per electrode (Fig. 2.20). Standard bottom electrode is made in AlCu alloy, capped with Ti/TiN layer to improve the adhesion at the plug interface, while the the top electrode is made in copper. The devices under test are single cells, where no selector is co-integrated. The study of the single PCM cell enables the monitoring of the behavior of the integrated phase-change material. All the devices tested along the experiments have been fabricated on 200 mm wafers. The use of single cells devices as test vehicle, enabled the fabrication of a large number of devices on a single wafers, in order to increase the results statistics.

In order to limit and at the same time to acquire the current on the PCM device, a resistance (R_{LOAD}) is put externally, in series with the cell (pull-up configuration Fig. 2.21). The voltage drop on the load resistor during the pulse application, is acquired through an oscilloscope in order to calculate the final current provided to the

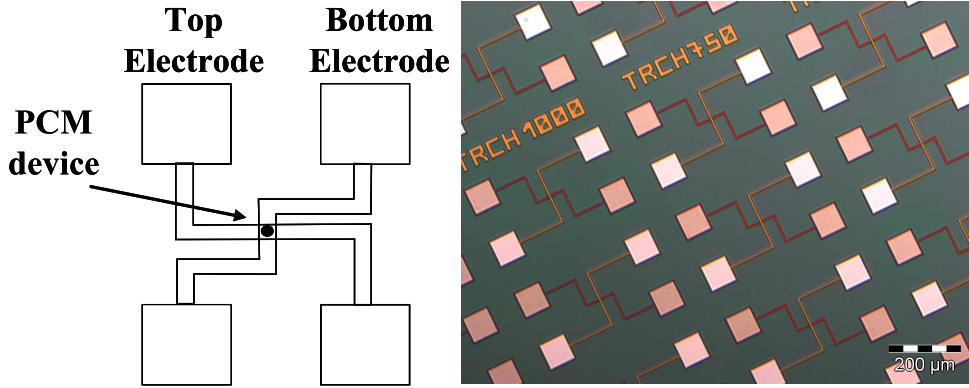


Fig. 2.20. Description of the 4-access lines analytical device, enabling Kelvin sensing. On the right the SEM image with the top view of our devices.

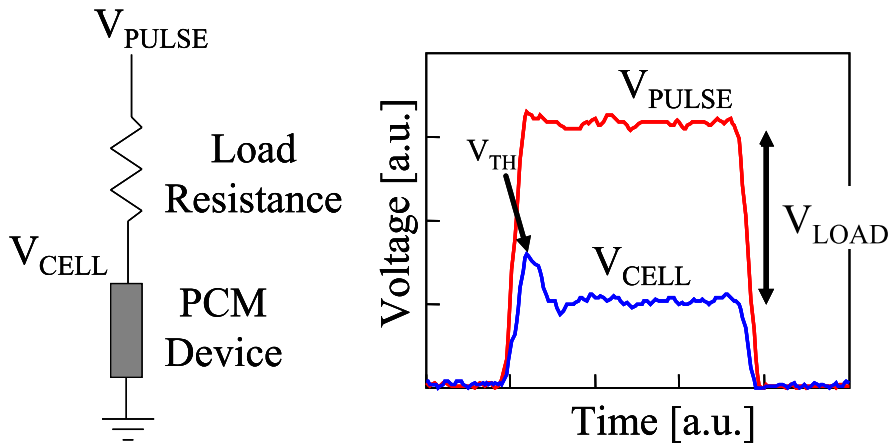


Fig. 2.21. Description of the general setup used to characterize the PCM cell. The cell current is monitored and limited by an external series resistance (R_{LOAD}). On the right, we see the final effect on the waveforms acquired. The voltage drop on R_{LOAD} enables the calculation of the current provided to the cell during the pulse application.

device, according to

$$I_{CELL} = \frac{V_{PULSE} - V_{CELL}}{R_{LOAD}} \quad (2.13)$$

where V_{PULSE} is the voltage applied on the series of cell and load resistor, and V_{CELL} is the voltage acquired on the PCM device. The dimensioning of R_{LOAD} is fundamental for the study of the cell, and depends on the device electrical parameters. The value of the load resistance has to fulfill the following requirements:

- The maximum voltage V_{PULSE} is limited by the equipment specifications (V_{MAX}), and since the RESET operation is the one that requires the highest current, the system has to guarantee to reach this current value:
 $V_H + (R_{ON} + R_{LOAD})I_R < V_{MAX}$;
- The minimum resolution (σ_V) of the measure of the voltage drop on the load resistance, has to allow the acquisition of the minimum current value (i.e. I_S):
 $\sigma_V/R_{LOAD} < I_S$;

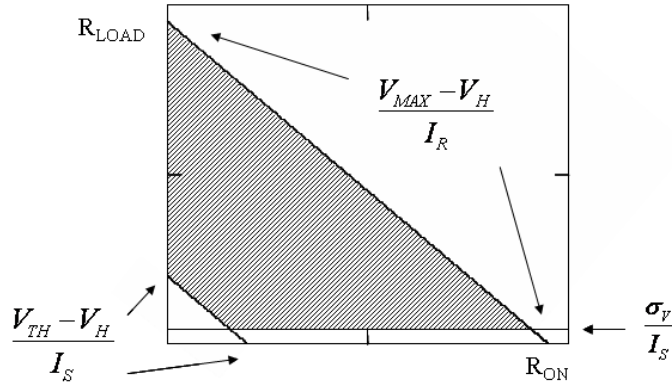


Fig. 2.22. Suitable values of R_{LOAD} for the characterization of our devices (filled area), as a function of the ON-state resistance of the PCM cell.

- At the threshold voltage V_{TH} , R_{LOAD} has to guarantee the possibility to screen currents able to crystallize the cell:

$$(V_{TH} - V_H - R_{ON}I_S)/R_{LOAD} < I_S.$$

These requirements are schematically reported in Fig. 2.22, where the range of suitable values of R_{LOAD} are reported as a function of the resistance R_{ON} of the cell (highlighted with the filled area of the graph).

In Fig. 2.21 we report an example of the waveforms acquired of the evolution of the voltage applied V_{PULSE} and of the voltage measured on the cell (V_{CELL}). The device in this case is starting from a RESET state. Initially the voltage applied drops completely on the cell, but once reached the threshold voltage, the cell reaches its ON-state and start to be highly conductive. The effect is the reduction of the voltage drop on the cell, and the increase of the drop on R_{LOAD} .

Since the current limitation is provided externally to the die, we expect a limitation on the bandwidth, due to the parasitic capacitance C_P of the system. C_P results from the sum of all the parasitic contribution of external cables, probe needles (used to contact the device electrodes), and the parasitic capacitance between top and bottom electrode of the device. The pole generated by C_P , depends on the variable resistance of the cell (R_{CELL}), and since this depends on the current (on the voltage), we will have a current dependent bandwidth

$$f_{BW}(I_{CELL}) = \frac{1}{2\pi C_P [R_{CELL}(I_{CELL}) || R_{LOAD}]} \quad (2.14)$$

It means that if the device is in the amorphous state (high R_{CELL}), the limitation to the voltage increase on the cell depends only on the load resistor, being also the worst case for the bandwidth limitation. The load resistor then, has to be the lowest possible, in the range of resistance values fulfilling the requirements listed above.

Considering now again the case of a cell in the HRS (high resistance state), during the application of the pulse we have the charging of C_P , till the reaching of the threshold voltage of the device (V_{TH}). The cell switches to its highly conductive ON-state, and the system experiences another transitory phenomenon before to recover the stability. C_P discharges on the parallel contribution of the cell and R_{LOAD} , giving rise to a peak

of current in the device approximatively equal to

$$I_{peak} \simeq \frac{V_{TH}}{R_{ON}} \quad (2.15)$$

R_{ON} includes the resistive contributions of all the elements of the device, in particular

$$R_{ON} = R_{PLUG} + R_{PCM} + R_{LINES} \quad (2.16)$$

where we find the resistance of the plug R_{PLUG} , the resistance contribution of the top and the bottom electrodes and the relative access lines in R_{LINES} , and the resistance of the phase-change material that after the switching event is taken to its ON-state (R_{PCM}). The recovering of the stability in the cell, is provided after a characteristic time proportional to $\sim C_P(R_{ON}||R_{LOAD})$. This transient can represent a source of thermal stress for the cell, with the consequent reduction of the endurance performance. Hence, a proper reduction of C_P can reduce the impact of this phenomenon. As we will see, in order to increase the bandwidth of the programming system and reduce the transients duration, and at the same time guarantee high disturb rejection, a specific electronic board has been developed to perform our tests.

2.5.2 The equipment

The characterization of a device is made of three main parts: the application of a voltage/current on the device, the sensing and the final exporting/elaboration of data. For the voltage generation we used an Agilent 81110A pulse/pattern generator capable of 2 ns transition time and 5 ns pulse width. The generator enables the application of train of pulses, combined pulses (e.g. sum of two different pulses), and also the tuning of the fall time independently from the rise time of the pulse. To acquire the pulses applied on the cell, we used a 2 GS/s oscilloscope Tektronix TDS 744A, combined with two active probes P6205 (750 MHz). To guarantee a high accuracy in the sensing of the cell, we used a parametric analyzer with verified current sensing resolution of 10 pA (in the final test configuration). We used different parametric analyzers, among which we quote the Agilent 4156C and the Keithley 4200-SCS. To automatically displace the probe needles, and then to contact the devices we employed the Cascade Microtech probe stations, equipped with hot-chuck with temperature remotely controlled (up to 300 °C).

In order to automatize all the electrical characterization process, we developed an electronic board (Fig. 2.23) with two main features:

- the possibility to change by remote control the load resistance during the characterization procedure;
- the switching between the pulse generation electronics, and the Kelvin sensing setup.

The change of the load resistance during the characterization procedure, was required in order to refine the current control in the range of currents favorable to the crystallization. The electronic board was designed to provide a stable ground to the PCM device and high disturb rejection.

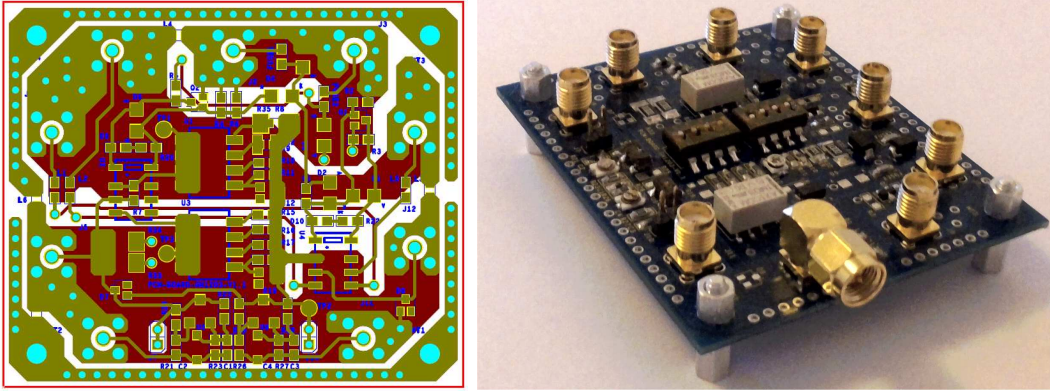


Fig. 2.23. The layout and a picture of the electronic board developed for our automatic characterization system.

The control of all the equipments was realized under Labview and C code programming environment. The final hardware/software system, enabled standard characterization procedures (low field measurements, data retention, cycling, programming characteristics, etc.) and the engineering of new procedures for the study of the behavior of new materials integrated in the PCM devices. In Fig. 2.24 we show an example of the output of the characterization system: a staircase-up (SCU) procedure is a train of pulses with increasing amplitude (Fig. 2.24a), and in this case it helps to verify the functionality of the cell. The cell starts in the RESET state (high resistance state or HRS), then, once reached the threshold voltage V_{TH} , the cell switches to the SET state (low resistance state or LRS). Increasing the current provided, the cell resistance gradually increases till the recovering of the original RESET state. From the acquisition of the current provided to the cell during each pulse, the voltage drop on the cell and the resistance of the device measured after each pulse applied, we can construct a full R-I-V programming characteristic for a given pulse width (Fig. 2.24b). From the latter, we can obtain the standard R-I and I-V standard plots, that identify the behavior of the cell, and from which we can extract all the electrical parameters of the PCM device under test (Fig. 2.24c-d):

- V_{TH} : the voltage at which the cell switches;
- V_H : x-intercept of the I-V characteristic of the cell in the ON-state;
- R_{ON} : slope of the I-V characteristic of the cell in the ON-state;
- R_{RESET} : maximum resistance of the cell (immediately after the RESET operation);
- R_{SET} : minimum resistance of the cell during the considered SET procedure;
- Resistance window: the maximum resistance window achievable by the device;
- I_R : current needed to take the cell to the 90% of the resistance window;
- I_S : current to program the cell to its minimum SET state (during the considered procedure).

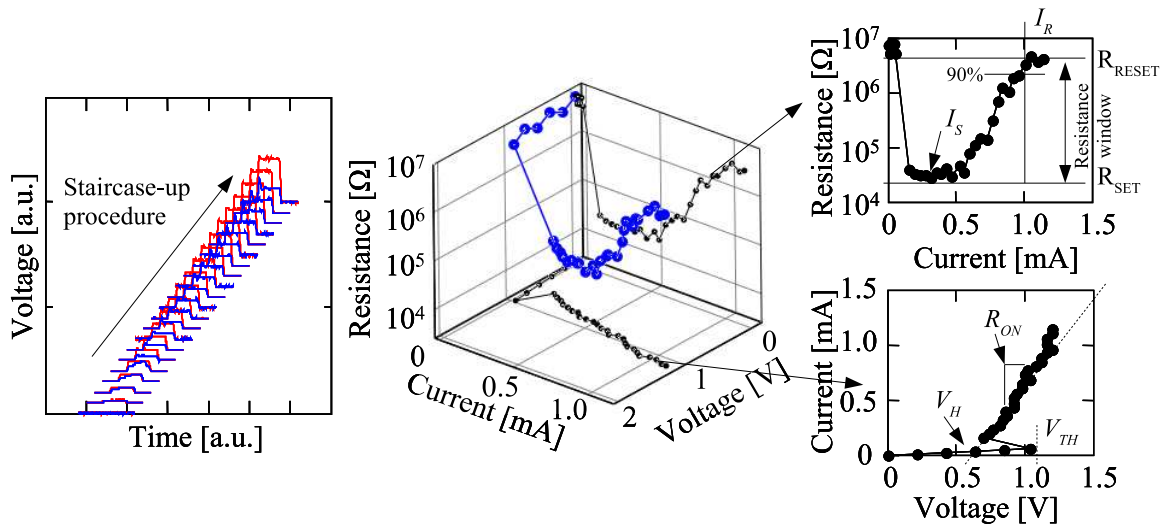


Fig. 2.24. A description of the output of the acquisition system designed for the PCM cells characterization. From the left, an example of a staircase-up procedure (SCU) (a), a full R-I-V characteristic of a PCM device for a given pulse width (b), and the relative R-I (c) and I-V (d) graphs that we can extract.

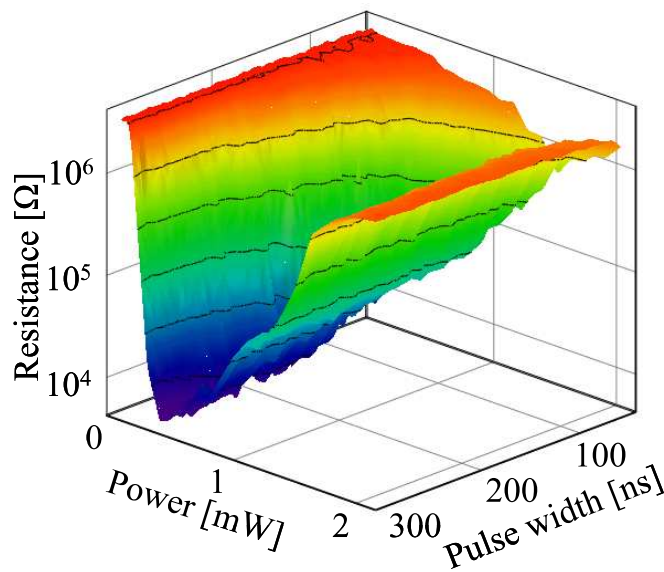


Fig. 2.25. An example of cartography of SET operation for a GST based lance-type cell.

Another important analysis enabled by the speed of the system developed, was the cartography of the SET operation. In Fig. 2.25 we report an example of this analysis. This test, similar in concept to the optical cartographies of recrystallization, is obtained by a sequence of RESET and SET pulses: the RESET is kept constant in order to pre-amorphize the cell, the SET pulse varies in amplitude and width (or fall time). Then the device resistance is measured after each RESET-SET sequence. The result is a detailed map of the cell programmed resistance, as a function of the power and pulse duration of the SET pulse. In the example reported in Fig. 2.25, the cartography is the result of 2000 different SET conditions, where each result is the mean value of 3 sequences with the same SET pulse parameters.

2.6 The study of the PCM reliability

There are some aspects of the PCM technology that are not common to other technologies and that can represent an issue for the final industrialization if not correctly considered and approached. The main reliability issues of the PCM technology are related to the working temperature of the device. However, some of them are not completely due to the temperature, but to a combination with other parameters like the reading disturb (called also subthreshold switching), that depends on the electric-field applied on the cell, the material segregation, that depends on the atomic composition.

The working temperature strongly affects the device performance, and first of all it can impact the retention of the information stored in a PCM device. However, the recrystallization mechanism, is not the only issue that can impact the thermal stability of a phase-change material. In particular, a phase-change material is affected by the temperature activated structural relaxation phenomenon, that in the device gives rise to the drift of the resistance toward higher resistance values. Moreover, the increase of the temperature produces a decrease of the threshold voltage. And even if the working temperature is lower than the critical crystallization temperature, the cell can experience an unwanted increase of the temperature due to the programming of neighboring devices (crosstalk phenomenon).

We describe in the following sections the main reliability issues of the PCM technology, presenting a specific analysis of these aspects in the case of the μ trench structure.

2.6.1 The cycling endurance

The scaling of the plug/phase-change material interface can impact the final lifetime of the PCM device, because of the thermal stress generated during the programming procedure. During the RESET pulse, the phase-change material reaches the melting temperature, and even if the pulse is applied for few ns, the cumulative effect can generate mechanical failures such as delamination [95], cracks, local material stoichiometry changes, materials interdiffusion, etc. [67]. PCM technology is well known for its capability of high cycling endurance up to more than 10^{12} cycles [6] demonstrated for the 180 nm technology node. In highly scaled devices with an indicative volume of $20 \times 3 \times 50 \text{ nm}^3$ of the active phase-change material, endurance of 10^4 cycles have been demonstrated [86]. The general trend observed in the literature, highlights the increasing importance of the engineering of the interfaces/materials and of the optimization of the deposition quality of the phase-change material, as the dimension of the active area of the PCM device decreases. To be competitive with other emerging technologies, the scaling of the PCM device must go hand in hand with the preserving of the cyclability performance. The requirement for the endurance of a memory technology can be estimated using the following empirical equation [13]:

$$C_{end} = T_{life} \frac{B_W}{\alpha_{wle} M_C} \quad (2.17)$$

where T_{life} is the lifetime expected for the memory device, B_W is the memory bandwidth, α_{wle} is the wear leveling efficiency, and M_C is the memory capacity. For a PCM device [96], we can assume 10 years of lifetime, 1 GB/s of bandwidth, 10% wear leveling

efficiency and 16 GB of capacity. The final endurance requirement calculated is $\sim 10^8$ cycles. This requirement has to be fulfilled, also when the device dimensions are scaled, meaning that the power reduction alone can not leave aside the cycling performance.

We performed the endurance test on our different devices, chaining repeated RE-SET and SET pulses, stopping the train of pulses at fixed time steps (logarithmically spaced), to verify the functionality of the cell and to evaluate the changing of the RESET-SET resistance window during the procedure.

One of the problems related to the long cycling of the cell, is the reaching of temperatures higher than the melting temperature of the material during each phase transition. It means that the atomic arrangement is modified at each programming pulse. In the case of phase-change material compositions stable (e.g. GeTe, GST), the phenomenon of the segregation and the lost of the phase-change mechanism can be attributed to:

- the high temperature gradient generated in the material during the RESET operation, that gives rise to strong volumetric variations. It causes a mechanical stress that in the long run can be detrimental, causing voids or local material stoichiometry changes;
- the interaction with materials of the interfaces, generating unwanted compounds;
- phase-change material imperfections (e.g. presence of contaminants like oxygen, that even in small atomic percentage in the long run can cause the cell failure);
- phase separation generating stable compounds, but with physical and chemical properties different from the starting material.

Another phenomenon recently described, is the phase elemental separation due to the different electronegativity of the atoms in the material [97]. It has been showed in these

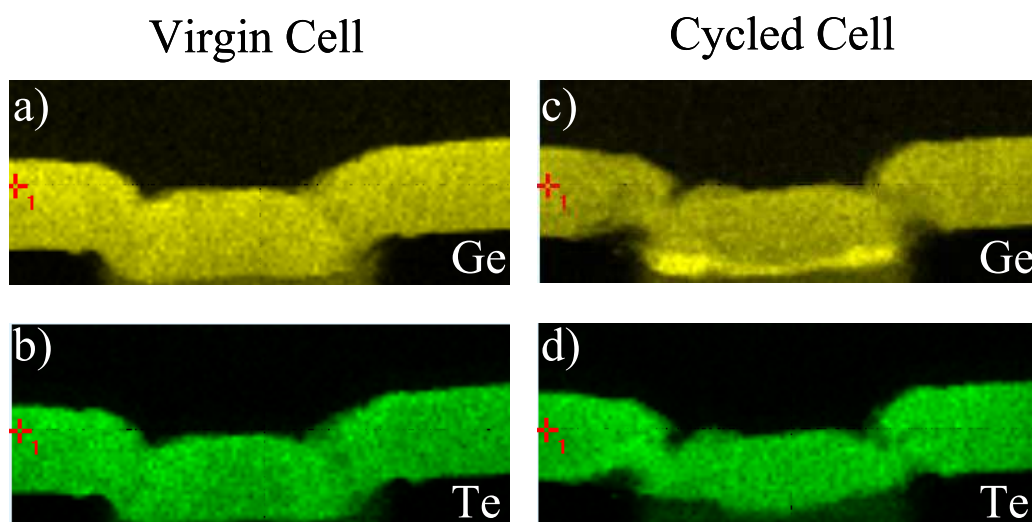


Fig. 2.26. EELS maps of the GeTe layer in our lance-type PCM cells. The plug at the bottom of the picture, while the top electrode is at the top. The intensity of the signal is correlated with the atomic specie concentration. We clearly observed an increase of the Ge at. % (c with respect to a) and a decrease of the Te at. % (d with respect to b) at the plug/phase-change material interface, after the cycling of the cell.

studies, that the pulse applied on the cell, can provide an atomic displacement along the material thickness. In Fig. 2.26 we show a similar effect in our GeTe based devices. We observe an increase of Ge concentration along the plug/phase-change material interface (at the bottom of the EELS pictures) and at the same time, a reduction of the Te at. %, the electronegativity of Ge (4.6 eV) being lower with respect to that of Te (5.49 eV).

2.6.2 The subthreshold switching: a statistical approach

The read disturb represents one of the main issues of the PCM technology correlated with the threshold voltage V_{TH} of the cell. In particular, when the reading voltage approaches V_{TH} , the device in the RESET state, can experience a switching event, modifying the programmed state. The subthreshold switching phenomenon has been explained by means of two different physical interpretations:

- the $1/f$ current noise fluctuation in the device [98, 99];
- the electric-field induced reduction of the energy barrier of the nucleation [44].

The first interpretation is based on the $1/f$ noise that affects the subthreshold current in the amorphous material. The author introduces the concept of switching current I_{TH} , and the fluctuations of the current in the material, can stochastically produce a switching event, according to the Weibull statistics. Even if the model fits the experimental results at room temperature, a real demonstration of its validity has not been provided at higher temperatures.

The second interpretation is based on the theory of the electric-field assisted nucleation [46], already introduced in chapter 1, and correlates the variability of the switching phenomenon with the effects of the electric field on the crystal nucleation energy barrier. In particular, it shows how switching is not a threshold phenomenon and can occur statistically with an expected time and a characteristic dispersion that depends on the temperature, and on the external electric field applied.

The decrease of the free energy of the amorphous system, due to the electrostatic energy of a particle with metallic electronic band characteristics, produces at high electric field an inversely proportional dependency of the nucleation barrier (W) on the field strength, according to

$$W \propto \frac{\alpha_{nucl} W_0 E_0}{E} \quad (2.18)$$

where W_0 is the zero-field energy barrier of nucleation, known from the classical theory of the nucleation, E_0 is the characteristic field (the equivalent electric field needed on a nucleus of critical radius r_0 to generate an energy barrier W_0) and α_{nucl} is a constant that depends on the shape of the formed nucleus. Since the distribution of the energy barrier, due to the non-uniformity distribution of atoms in an amorphous system, can be considered a gaussian distribution, it is reasonable thinking that also the characteristic dispersion of W depends on the electric field. Taking into account that the fluctuations of this parameter are more important along the interfacial discontinuities, the electric field dependency of the energy barrier dispersion can be presented in the form

$$\sigma_W \propto \sigma_{W_0} \sqrt{\frac{E_0}{E}} \quad (2.19)$$

This last equation shows how the electric field strength reduces the final fluctuation of the energy barrier, leading to a quasi-deterministic phenomenon. Roughly, it means that if we approach the threshold voltage (or critical electric field), the switching becomes highly probable.

To study the statistical nature of the switching phenomenon, and its dependency on the electric field and on the temperature, we chose to perform the tests on “Wall” industrial structures highly scaled, in which we integrated the standard phase-change material GST. This was also to provide a description of the impact of the phenomenon, on final industrial devices.

We chose two types of test approach. The first was to apply a constant bias on our RESET cells, at voltages considerably lower than the threshold voltage ($\simeq 0.5$ V), to be able to measure switching times on the order of ms. But as pointed out in eq. 2.19, the lower is the voltage, the higher is the fluctuation of the phenomenon, leading to highly spread distributions of the switching times. The test procedure becomes in this case really long and since we were searching for a large number of results in order to have a proper description of the statistics of the phenomenon, even if we observed a discrete probability of switching, we decided to move to another solution. The second approach was to apply a constant pulse on the cell pre-RESET, with pulse width lower than 500 μ s, and acquire through an oscilloscope, the total time needed to switch the cell. This solution is able to catch switching times on the order of tens of μ s, and thanks to the speed of our characterization system, the number of data acquired is highly sufficient to reconstruct the statistics of the phenomenon under test. The use of a thermal chuck, allowed also the performing of the test at different operational temperatures.

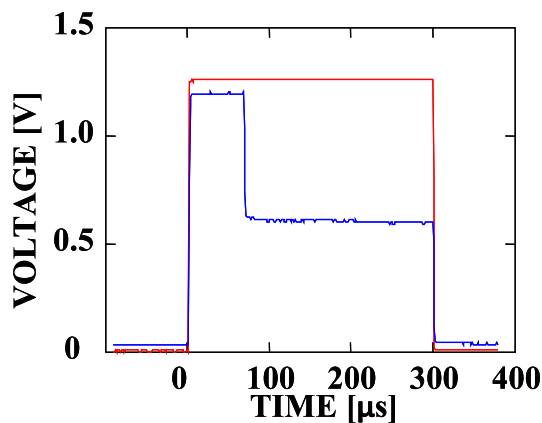


Fig. 2.27. Example of pulse applied on our device for the study of the switching time. The voltage of the stress is lower than the threshold voltage V_{TH} , but as we can observe, after some time, the cell switches. It is a sign of the stochastic nature of the switching phenomenon.

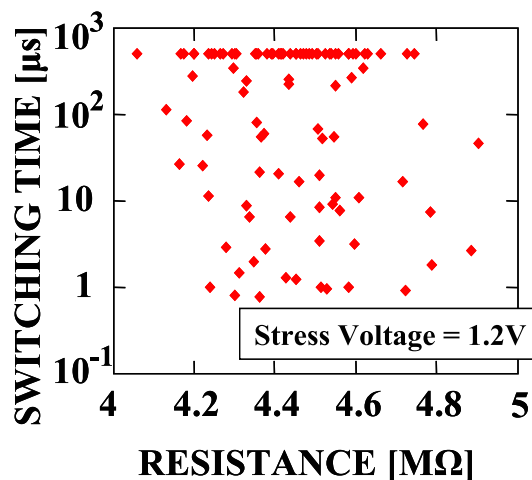


Fig. 2.28. Distribution of the switching time, as a function of the pre-programmed RESET resistance. In all the tests performed, no correlation has been observed between the programmed resistance (almost constant), and the switching time. The stress duration was fixed at 500 μ s, and the data relative to this time, are indicative of devices that didn't switch during the test.

In Fig. 2.27 we can see an example of the tests performed. The voltage is applied on the series of a load resistance (opportunistically dimensioned) and the cell, and is lower than the threshold voltage, but sufficiently close to V_{TH} to allow the switching after 80 μs . We have no visible sign before the switching, in the electrical parameters, of a change of the conduction mechanisms in the device. The phenomenon in all the tests performed appeared totally independent also of the initial RESET resistance of the devices. In Fig. 2.28, we show how the switching time calculated on a population of cells (at room temperature), doesn't show any dependency on the starting resistance, here reported in linear scale.

We think that, the variations of the amorphous volume in consecutive RESET procedures and in different cells, can impact our switching time distributions just with a fixed Variance variation, not dependent on the electric field, nor on the temperature. In fact, the stochastic nature of the phenomena that generate these variations (e.g. plug dimensions, phase-change material layer thickness, etc.), affect all our tests in the same way, without interfering with the main mechanism that produces the device switching. Moreover, the demonstrated absence of correlation between the device resistance and the switching time, allowed us to exclude the hypothesis that the switching time distributions observed, can depend on a difference in the amorphous phase-change material thickness.

In Fig. 2.29 we show an example of what we obtained in our tests. As expected, the higher is the voltage applied on the cells, the lower is the switching time, and the clear distributions obtained on a large population of devices and consecutive tests, evidence the statistics of the phenomenon. To model our results, we considered what is reported in [46], regarding the probability density distribution of the electric field assisted nucleation phenomenon in time. We calculated the final cumulative distribution

$$P(\bar{t}|T, E) = P_0(n_{ff}, \bar{t}_0(T, E)) \int_0^{\bar{t}} e^{-\left(n_{ff} \ln \frac{t}{\bar{t}_0(T, E)}\right)^2} dt \quad (2.20)$$

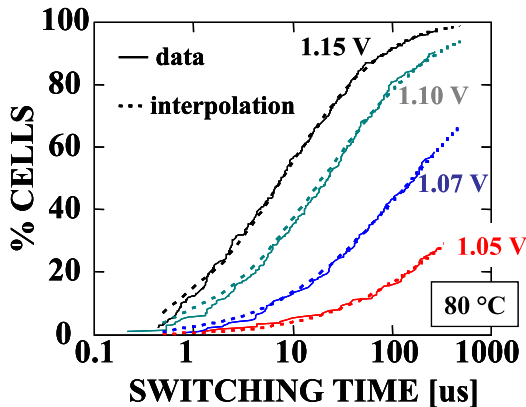


Fig. 2.29. Cumulative distributions of the switching time, for a population of 1000 devices, for different applied voltages and at 80 °C. The data acquired are perfectly fitted with eq. 2.20, showing the validity of the distribution equation considered.

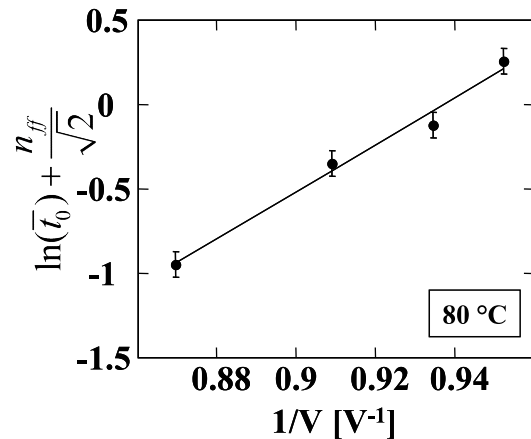


Fig. 2.30. Trend at 130 °C of the parameter \bar{t}_0 , indicative of the expected value of the switching time, as a function of the stress voltage. The graph confirms the relation expressed in eq. 2.21

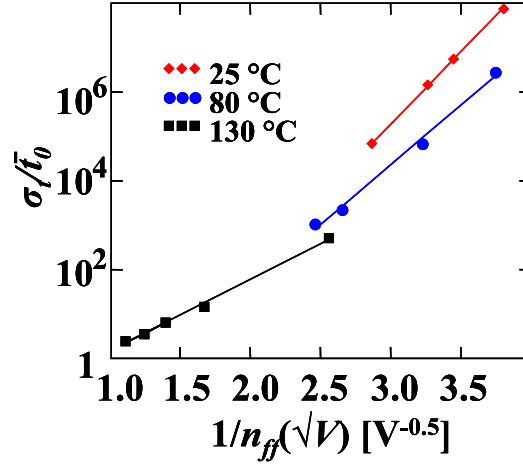


Fig. 2.31. Relative Variance σ_t of the probability distribution function considered in eq. 2.20. We reported the results obtained for three temperatures. We observe that the slope of the linear interpolation decreases when the temperature increases, as expected from eq. 2.22, and that the higher is the working temperature, the lower is the final Relative Variance of the distribution.

where n_{ff} is a form factor, that depends on the ratio S_D/r_0^2 where S_D is the amorphous dome external surface. The parameter n_{ff} represents in some way, the number of possible sites from where the filament can starts to grow. The parameter \bar{t}_0 is the characteristic time, at which the probability density reaches its maximum (and also correlated with the most likely switching time), and it is the parameter that incorporates the dependency on the electric field and on the temperature. P_0 is the normalization factor, that depends on n_{ff} and \bar{t}_0 , and \bar{t} is the observed time. We fitted our data using eq. 2.20, as reported in Fig. 2.29, finding a really high confidence level between data and the model. From the interpolation, we extracted the best fitting parameters n and t_0 for each voltage and temperature used. The characteristic time introduced in eq. 1.21 of chapter 1, is described in more details by the following equation

$$\bar{t}_0 = \tau_v e^{\frac{\gamma_m W_0 V_0}{k_B T V} - \frac{n_{ff}}{\sqrt{2}}} \quad (2.21)$$

where we can find its dependency on the temperature and in particular on the voltage applied on the cell. The parameter τ_v is the characteristic vibrational atomic time, and γ_m a material parameter. In Fig. 2.30, the plot and the relative linear interpolation, confirms the dependency on the voltage showed in eq. 2.21: the higher is the voltage, the lower is the expected switching time of the cell. From the intercept of the linear interpolation, we estimated also the value of τ_v to be 1.9 ps, on the order of magnitude of the values reported in the literature. The main result of this analysis, is the fact that when the time of the experiment is long enough and/or the temperature is high enough, switching can take place below the threshold voltage. Hence, we understand the strong importance to model this phenomenon, that can causes the failure of the cell at high operating temperature, during a simple reading procedure.

Moreover, we can calculate the dispersion of the switching time from eq. 2.20:

$$\frac{\sigma_t}{\bar{t}_0} \propto e^{\frac{\sigma_W}{k_B T n_{ff}}} \quad (2.22)$$

where substituting σ_W with eq. 2.19, we find that both the electric field and the temperature contribute to narrow the switching time dispersion. We find confirmation to

this equation in Fig. 2.31, where we reported the trend of the relative variance for all the distributions found at different temperature and different voltages. The slope of the linear interpolations plotted for each temperature, decreases when we increase the temperature of the test, as predicted in eq. 2.22.

To conclude, we found a strong compatibility between our data and what predicted in the theory of the electric field assisted nucleation.

2.6.3 The decrease of the threshold voltage rising the temperature

This phenomenon was already observed in fundamental material studies on first phase-change materials in 1970s [100]. The decrease of V_{TH} when the operating temperature of the device increases, can enhance the reading disturb problem. The latter, associated with the incoming crystallization of the amorphous phase, may reduce the effective allowed working temperature. The first explanation given, already took into account the lifetime of the carriers (τ_l) and the relaxation time of the material (τ_r). When τ_l is equal to τ_r , the system becomes instable, giving rise to the switching event (according to [100]). Like observed in eq. 1.17, the energy barrier (E_C) of the conduction is reduced by the electric field, and the final conductivity of the material, according to eq. 1.11, can be written as

$$\sigma = \sigma_0 e^{-\frac{E_C - qE \frac{\Delta z}{2}}{k_B T}} \quad (2.23)$$

where σ_0 is the saturation conductivity of the material at high temperature, E is the electric field, Δz is the mean distance between two traps in the lattice (originally called “characteristic distance”), q the fundamental charge, and T the temperature. The hypothesis was a total independency of τ_r on the temperature, that means the existence of a threshold conductivity σ_{TH} at which $\tau_r = \tau_l$. From eq. 2.23 we can then calculate

$$V_{TH} = \frac{2u_a}{q\Delta z} \left(-k_B T \ln \left(\frac{\sigma_0}{\sigma_{TH}} \right) + E_C \right) \quad (2.24)$$

where we substituted the electric field with the ratio between the threshold voltage and the amorphous material thickness (V_{TH}/u_a). This linear dependence of V_{TH} on the temperature was confirmed recently [101, 102], but taking into account the temperature dependence of the carrier escape time from a trap in the lattice. The integral on the escape time, on all the traps localized in the gap, led to same linear relation evidenced in eq. 2.24.

Even if not directly analyzed, in the electric-field assisted nucleation theory the threshold electric field depends directly on the temperature, but with an inversely proportional relation [103] ($E_{TH} \propto 1/T$). This relation has not been confirmed up to now, even if the rapid decrease of the threshold voltage with the increase of the temperature that it predicts, may be due to the fact that other temperature dependent parameters are not considered in the formulation.

2.6.4 The drift of the cell resistance

We already described in chapter 1 the drift phenomenon in a phase-change material. The increase of the resistivity of the amorphous phase in time, impacts the final sta-

bility of the programmed state in the cell, making the resistance window of the device time-dependent. Since the crystalline phase does not experience this problem, this phenomenon does not represent a problem in a final device: even if the RESET state drifts towards higher resistance values, the SET state is stable, and a threshold resistance to discriminate the two states can be found. This is true if we consider a crystalline phase with no vacancies and where the long-range order is shared by the full phase. Since we are providing the crystallization in the cell through really fast pulses, the material presents a polycrystalline nature and, in some materials like GST, it has a crystalline structure with a high concentration of vacancies (20% in fcc GST [32]). It means that the drift phenomenon can affect also the SET state of the device. Moreover, the higher is the resistance of the cell, the higher is the drift coefficient ν [104], calculated according to the equation derived from eq. 1.23:

$$R = R_0 \left(\frac{t}{t_0} \right)^\nu \quad (2.25)$$

Hence, the problem of the drift becomes detrimental in multilevel cell applications, where the cell is programmed in intermediate resistance states. This required programming and reading techniques at system level, to ensure storage reliability [105, 106]. At the same time, experimental results also show how the drift phenomenon, because of its stochastic nature, broadens the resistance dispersion of the devices, when the resistance value increases [107].

2.6.5 The data retention

One of the main bottlenecks of the PCM technology is the retention of RESET data at high temperatures. It is why this issue has been investigated widely in the last decade. The amorphized volume of phase-change material, since in a metastable phase, experiences a gradual recrystallization activated by temperature. Hence, the resistance of the device decreases till the final deterioration of the stored bit. The effect of the size reduction on the increase of the crystallization temperature for different phase-change materials has been already presented in section 1.9. But once integrated in the final device, the thermal stability of the phase-change material starts to be affected by surrounding interfaces, material impurities, amorphous/crystalline grains boundaries, etc.. Different models for the device data retention failure have been proposed in the last years. Considering the stochastic component of the crystallization process, the failure time of the cells under test can be approximated with the Weibull statistics [108], related to the combination of the nucleation and growth mechanisms on going during the recrystallization. According to this model, the failure time, considered as the time necessary for the 50% of the population of devices to fail, has an Arrhenius temperature dependency:

$$t_{fail} = t_0 e^{\frac{E_A}{k_B T}} \quad (2.26)$$

where t_0 is a fitting parameter, E_A is the activation energy of the failure process, k_B the Boltzmann constant and T the temperature used for the accelerated retention test. This equation allows to extrapolate the maximum temperature (fail temperature) to guarantee 10 years of retention for at least half of the population, and the maximum failure time expected at a given temperature (Fig. 2.32). Later works [109], showed how

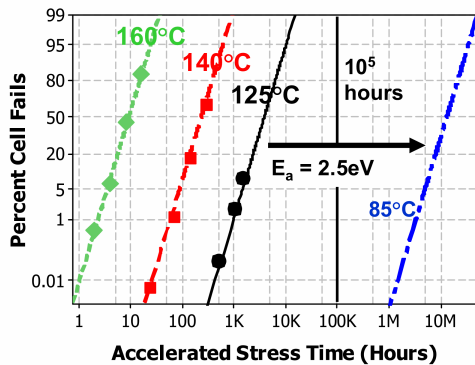


Fig. 2.32. Data retention failure rate (Weibull distribution) as a function of time at different temperatures, for GST-based PCM devices [110]. Data are fit according to eq. 6, revealing an activation energy of 2.5 eV and extrapolation is made at 85 °C (fail temperature requirement for industrial applications).

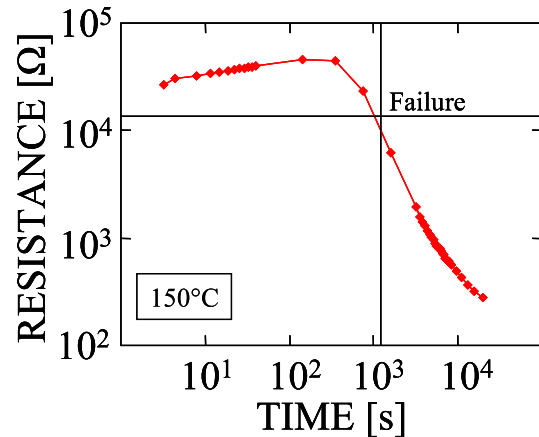


Fig. 2.33. Example of data retention test at 150 °C performed on one GST-based cell, through the chuck procedure. The failure criterium of the reaching of half of the starting resistance of the cell is highlighted.

this model underestimates the activation energy of the process, in particular because at high temperatures (used to activate the failure mechanism), the contribution to E_A of the activation energy of the nucleation is lower than at lower temperatures. But since a more accurate extrapolation depends on physical parameters that are not easy to characterize (like grain growth speed, and nucleation rate for a give temperature), in our studies we considered eq. 6 for the comparison between different PCM devices.

Early works demonstrated that isotropic scaling of the active volume of the integrated phase-change material, does not affect the retention performance of the device [111]: this is true, in materials where the growth-driven crystallization starting at the peripheral crystalline/amorphous interface, is negligible with respect to the nucleation rate. The growth becomes a problem, even in nucleation-dominated materials, at dimensions lower than 3 nm [109].

We performed our data retention tests with two main procedures, always after a pre-cycling of the cells (called “seasoning”) to validate the cells functionality:

1. Chuck procedure: increase of the chuck temperature till the target value, pre-programming of the cells in the RESET state, monitoring at logarithmically spaced time steps of the resistance of the cells till the full recrystallization (Fig. 2.33).
2. Oven procedure: preheating of the oven till the target temperature, pre-programming of the cells in the RESET state, annealing of the wafer in the oven and reading at room temperature at logarithmically spaced time steps.

We considered as failure criterium for each cell, the reaching of half of the starting RESET resistance.

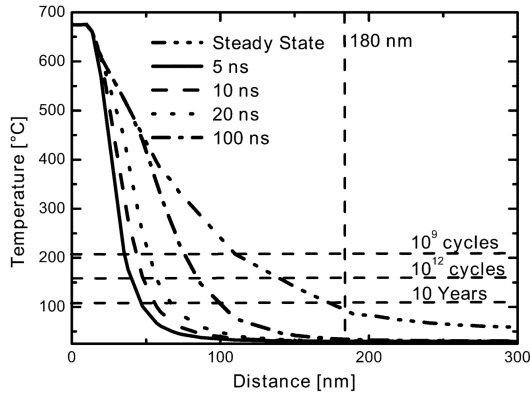


Fig. 2.34. Simulated thermal profiles in a programmed GST-based PCM cell in transient (programming pulse widths in the range 5-100 ns) and steady-state conditions [112] (RESET pulse). The estimated temperature for 10 years of retention is reported as reference, and also the equivalent temperatures limit for a full recrystallization of the neighbor cell if cycled 10^9 and 10^{12} times (estimated).

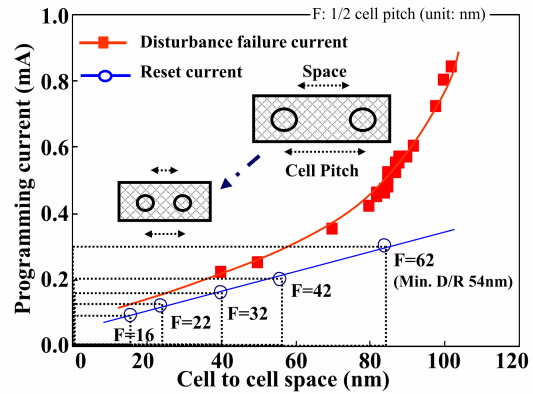


Fig. 2.35. Trend of the minimum allowed current to avoid cross-talk failure, and of the reset current of the PCM device, as a function of the cell to cell distance (reduced according to the technology node-shrink) [77].

2.6.6 The cell-to-cell cross-talk

Degradation of the PCM resistance may also result from unintentional heating of the active phase-change material layer induced by thermal cross-talk between adjacent bits [112]. As shown in Fig. 2.34, during the RESET of the cell, the temperature reached in the device reaches the melting temperature T_m of the phase-change material. The temperature profile, dependently on the pulse duration, extends far from the active region, with a gradient that depends inversely on the thermal conductivity k_{th} of the surrounding material. Since the temperature profile is not supposed to scale with the technology, is expected that decreasing the cell size and the cell-to-cell pitch, the impact of the cross-talk becomes detrimental. As reported in Fig. 2.35, where the minimum current to produce cross-talk is estimated as a function of the technology node, the only way to face this problem is to keep the maximum RESET current, lower than this limit [77].

2.6.7 Case study: the high temperature reliability of the μ trench PCM structure

The μ trench structure is considered as one of the most scalable technologies in the set of the phase-change memory structures, and the first real industrial PCM devices. In this light, we investigated the reliability of μ trench PCM devices at high operating temperatures. At the same time, we performed our analysis on different μ trench dimensions, confirming the low impact of the scaling on material dynamics in μ trench based PCM technology.

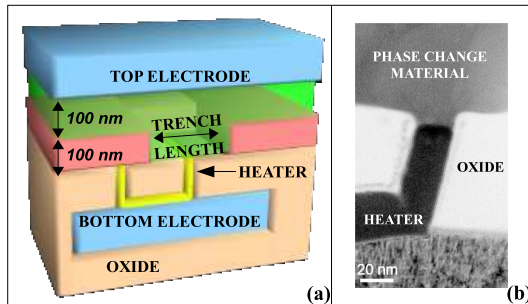


Fig. 2.36. (a) Simplified schematic of our analytical μ trench PCM structure. (b) TEM image showing the interface between the heater and the GST phase change material.

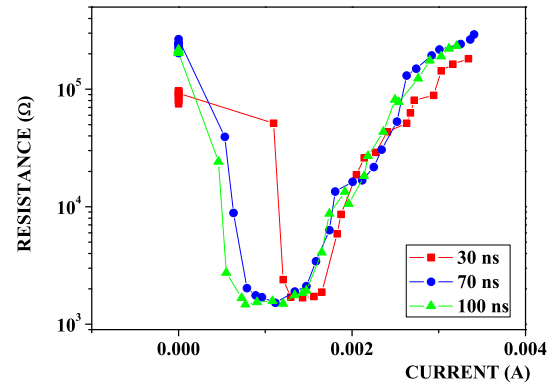


Fig. 2.37. Programming curves at room temperature for a 300 nm device. The device is able to cover more than three orders of magnitude.

2.6.7.1 Our μ trench memory cell structure

The schematic in Fig. 2.36 describes the μ trench structure considered. The heater thickness (30 nm) is controlled by film deposition, and the trench dimension by lithography: in our study, we analyzed PCM cells with four different trench width ranging from 300 nm to 1 μ m and we will refer to our samples by the trench width. In the inset of Fig. 2.36 is reported the cross-section TEM image of our μ trench cell showing the interface between the phase-change material and the heater element. The chalcogenide material integrated in our devices is 100 nm-thick $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST), deposited by PVD technique. The heater material is tungsten silicide.

2.6.7.2 The devices and the speed analysis

The electrical performances and reliability tests of analytical μ trench memory cells have been analyzed (on a minimum of six devices for each trench width) by means of our completely automatic setup equipped with hot-chuck system. During a general programming operation, a pulse is applied to the series of a load resistance and the PCM cell device. The programming current is acquired by monitoring the voltage drop on the load resistor.

The program speed is defined as the minimum time required to program the device in the SET state, starting from a RESET state. In Fig. 2.37, we report an example of characterization performed on the 300 nm devices. Each point in the graph corresponds to the resistance level reached by the cell after a SET pulse, applied on the cell pre-programmed with a 20 ns wide RESET pulse. A 30 ns SET pulse allows to recrystallize the phase change material with 1.5 mA, and we obtained the same order of programming speed for all the devices under test independently of the trench width. With the increase of the pulse width, the probability to have the electronic switch at lower voltages is increased, as already presented in section 2.6.2. This enables the appearing of a programming region (lower than 1 mA) in which we can program the cell in intermediate resistance states. Furthermore, in the region of currents where we start to amorphize the cell (higher than 1.5 mA), the curves are well superposed: this is an indication that the temperature profile reached during the programming pulse

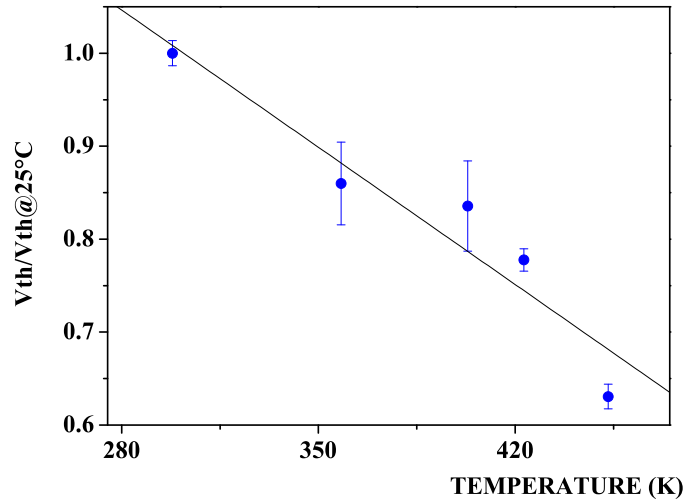


Fig. 2.38. Plot of the threshold voltage (normalized to the value of V_{TH} at 25 °C) as function of the operating temperature, for the 300 nm μ trench devices.

does not depend on the pulse width, and is achieved already in 30 ns.

2.6.7.3 Dependence of the threshold voltage on temperature

In order to evaluate the change of the threshold voltage V_{TH} at different operating temperatures, we programmed our devices in the RESET state and then we applied a staircase-up sequence of pulses till the reaching of the critical voltage. In order to decrease the dispersion in the measure, we chose a pulse width of 300 ns. In Fig. 2.38 are reported the results obtained in 300 nm devices. We notice a linear behavior of V_{TH} as function of the temperature, as introduced in section 2.6.3. In table 2.2, are reported the values resulting from the linear interpolation of the data for the four trench dimensions. As expected, we do not see any significant correlation between the reduction of the trench width and the V_{TH} slope and the y-intercept value. Since the programming conditions for the four trench widths are different (i.e. the programming current), we expect variable mean thickness for different trench dimensions. However, the higher is the V_{TH} slope, the higher is the y-intercept value. As reported in [113] we can correlate the y-intercept with Wu_a/aq where W is the thermal activation energy of the material, u_a the equivalent thickness of the amorphous region, a the characteristic distance and q is the electron charge. The slope can be correlated with $\gamma_c u_a k_B / aq$, where γ_c is a constant dependent on the critical conductivity at the switching point and k_B is the Boltzmann constant. These relations suggest that the slope and the y-intercept values are both correlated to the thickness of the amorphous region involved in the RESET-SET transition.

During a SET pulse, when the voltage drop on phase-change memory device reaches the threshold voltage V_{TH} , the conductivity of the cell increases abruptly (ON-state of the cell, with a resistance defined as R_{ON}). This changes the load seen from the access line to the memory, and as already introduced in section 2.5.1, it generates a transient peak of current in the cell ($\simeq V_{TH}/R_{ON}$): the lower the parasitic capacitance, the shorter this transient. This current peak can be higher than the current used to RESET the cell if R_{ON} is not providing a sufficient current limitation. All these considerations

Trench size	$\gamma_c u_a k_B / aq$	$W u_a / aq$
300 nm	-2.1 ± 0.4 mV/K	1.6 ± 0.2 V
500 nm	-2.5 ± 0.5 mV/K	1.7 ± 0.2 V
750 nm	-3.5 ± 0.8 mV/K	2.0 ± 0.3 V
1000 nm	-2.7 ± 0.5 mV/K	1.8 ± 0.2 V

Table 2.2. Parameters of the interpolation of V_{TH} (see Fig. 2.38) as function of temperature.

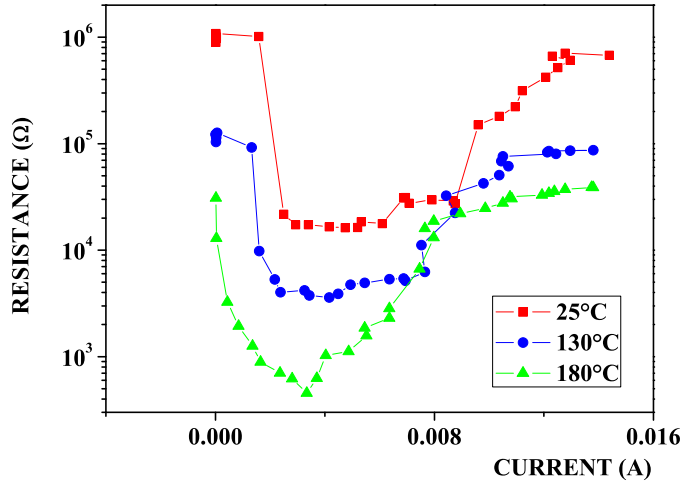


Fig. 2.39. Programming curves for the 750 nm μ trenchPCM device, at different operating temperatures.

lead us to the conclusion that the SET operation is a source of thermal stress for the cell, stronger as V_{TH} increases. V_{TH} decreases at high operating temperatures, thus increasing the sensitivity of the cell to low programming voltages. At the same time, the decrease of V_{TH} is expected to result in a decreased thermal peak stress in RESET-SET operations.

2.6.7.4 Programming curves

In Fig. 2.39, we report an example of the behavior of a 750 nm μ trench cell, when the operating temperature reaches 130 °C and 180 °C. The cell is pre-programmed in RESET state (with a pulse width of 300 ns); then a SET pulse (pulse width of 50 ns) of increasing voltage is applied, recording the resistance of the cell after each RESET-SET operation. By increasing the temperature, we observe the exponential decrease of the resistivity of the RESET state due to the semiconductive nature of the material. At the same time, the SET resistance also decreases. In fact, one has to note that the above described test procedure (each SET pulse being applied on RESET state) only leads to a partially crystalline SET state, as illustrated by the fact that for a given temperature the SET resistance is higher than that obtained with a staircase-up procedure in Fig. 2.37(one order of magnitude of difference can not be explained only through the trench width variation). Because of the lowering of the energy barrier of crystallization with temperature, a higher degree of crystallization is reached when the temperature increases, thus leading to a lower SET resistance. The increase of the conductivity with the temperature, according to the semiconductive

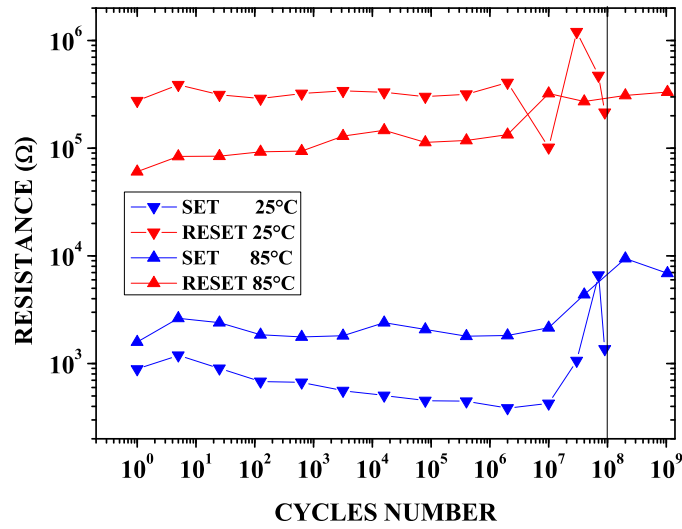


Fig. 2.40. Example of endurance test performed on a 500 nm μ trench PCM device. We observe the increase of the cyclability of the cells (up to more than 10^9 cycles) once the temperature is increased. The RESET pulse width is 30 ns; the SET pulse width is 100 ns.

nature of the material even in the SET state, can play a role in the reduction of the temperature, but it is not sufficient to explain the two orders of magnitude of decrease observed. As a consequence of the shift of both the RESET and SET resistances to lower values, we observe a preservation of the resistance window, for a given device under test. As previously observed, thanks to the decreased threshold voltage, we are able to SET the cell at lower programming currents, and obtain intermediate resistance states. Moreover, we observe a decreasing of the RESET current of 40% from 25 °C to 180 °C.

2.6.7.5 Endurance at high temperature

Endurance measurement is performed at room temperature on μ trench devices demonstrating the possibility to reach more than 10^8 cycles. After the endurance, we observe a degradation of the resistance programming window, in general affecting both the RESET and the SET states. When the operating temperature is increased (still using the same pulse conditions) we observe an increase of the cyclability of the cells. This is shown in Fig. 2.40, where an example of endurance test performed on a 500 nm device at 25 °C and at 85 °C is reported. The cells reach 2×10^8 cycles at room temperature; at 85 °C the cells are able to cycle up to more than 10^9 cycles. Indeed, this result confirms what already announced in section 2.6.7.3, that increasing the temperature, the decrease of the threshold voltage reduces the thermal stress in the cell during the SET operation.

2.6.7.6 Resistivity drift analysis

The drift study has been performed on our μ trench cells in order to understand the impact of the size of the trench dimensions on the stability of the amorphous phase. An initializing procedure (10 SET-RESET cycles) was applied to all the devices. Then a RESET pulse is applied in order to bring the device to the high resistivity state. In

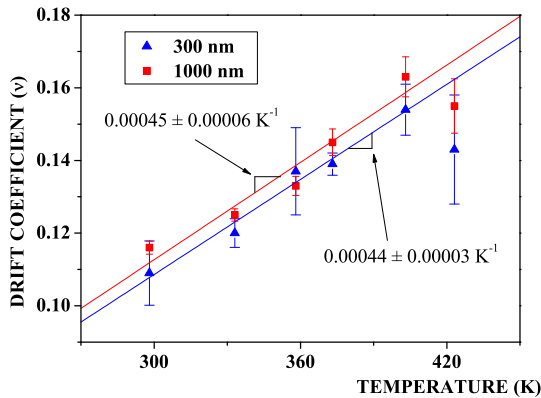


Fig. 2.41. Analysis of the drift coefficient at different operating temperatures for the 300 nm and for the 1000 nm devices.

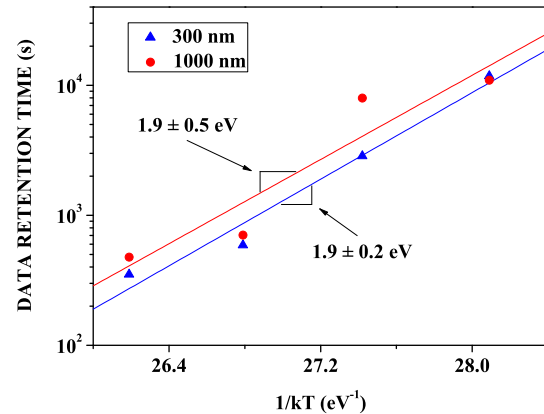


Fig. 2.42. Arrhenius plot for the data-retention analysis performed on 300 nm and on 1000 nm μ trench devices. The failure criterion considered is the reaching of a resistance equal to one order of magnitude less than the initial RESET state.

Fig. 2.41 we report for two trench dimensions the drift coefficient (ν) of the power law $R = R_0(t/t_0)^\nu$ (eq. 2.25) for each operating temperature. The drift coefficient linearly increases as the temperature increases [51, 53], starting to decrease at 150 °C probably due to the incoming crystallization process. There is no difference between the slope values calculated, with a confidence level of 88% (that quantifies the reliability of the result). This suggests that the traps distribution along the trench width is uniform and the structural relaxation can be considered as affecting locally the resistivity of the material.

2.6.7.7 Data retention measurements

In this experiment the temperature of the chuck was increased up to a specific temperature, then an initializing procedure (10 SET-RESET cycles) was applied to all the devices under test, finally a RESET pulse was applied before the data retention measurements. In Fig. 2.42 we report the Arrhenius plot for the 300 nm and 1000 nm μ trench devices. There is no difference between the extracted activation energies with a confidence level of 92%. It follows a data retention almost independent on the trench width. What we suppose is that the data retention depends on the generated amorphous region thickness, which indeed does not vary with the trench width.

2.6.7.8 Simulation results

The thermal stress of our μ trench cell during the RESET and the SET pulse have been analyzed in detail using simulations that make use of Level Set numerical approach to model crystallization kinetics [114] (the simulation tool will be described in detail in the next section). We simulated in particular the electro-thermal behavior of the μ trench cell during the application of a SET pulse to a cell pre-programmed in the RESET state. In Fig. 2.43, we report the thermal profile in the cell after 0.7 ns from the effective electronic switch, before the recovery of the thermal equilibrium in the

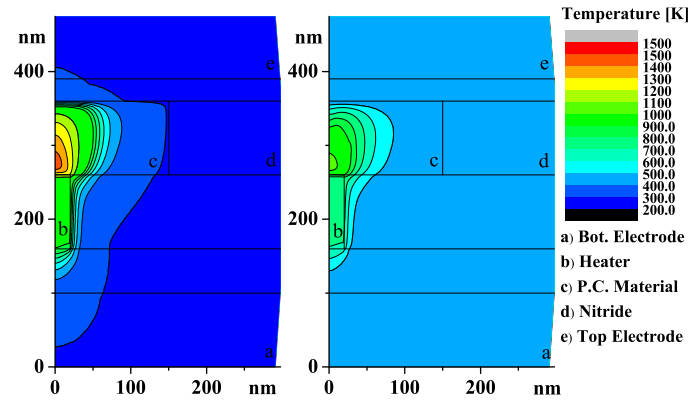


Fig. 2.43. Simulation of the temperature profile of the μ trench cell (cross-section view) during the RESET-SET transition after 0.7 ns from the effective electronic switch, at room temperature (left) and at 130 °C (right).

cell. Here we report the results obtained for a SET pulse at room temperature and at 130 °C. We can observe that a strong thermal stress happens in the cell at the interface between the heater and the phase change material during the switching event. Once reached the switching voltage, the peak of the temperature is localized at the edge of the heater element: then the peak of the temperature moves to the center above the plug (see Fig. 2.43). Since the threshold voltage is lower at higher temperatures, the peak of current (and of power) after the switch event is lower. This leads to a reduced thermal peak stress during the SET pulse at 130 °C (peak of 1000 K) compared to room temperature (peak of 1500 K) as shown in Fig. 2.43. This result is in agreement with the electrical tests and we demonstrated finally that, despite the shifted resistance window toward lower resistance values, high operating temperatures decrease the thermal stress in the cell during SET operations.

2.7 The simulation tool and the model

The simulation tool used to simulate the behavior of our Phase-Change Memory cells, has been developed in MATLAB and C code. The main goal of our simulations, was to understand the physical mechanisms on going during the programming of the device (RESET and SET operations), and correlate the electrical results obtained during the test of our cells (i.e. the variation of the resistance of the device dependently on the programming current) to the material phase evolution. The idea was to start with the implementation of the model for a given well known phase-change material ($\text{Ge}_2\text{Sb}_2\text{Te}_5$), in order to provide a tool for the analysis of new structures and new phase-change materials.

The realization of a tool to simulate the behavior of a phase-change memory device requires the coupling of the phase transitions of the phase-change material with the electro-thermal properties of the device. We took advantage for our simulations of the Level Set Method (LSM) combined to the electrothermal solver (presented in [114]). The Level Set Method is used to compute the evolution of the crystalline phase in the phase-change material, taking as input the growth speed. This method is used in applications involving the motion of complex interfaces, like in our case where the interface

is mainly between the crystalline phase (or liquid phase) and the amorphous phase. The evolution of the interface Γ in the n -dimensional space considered is calculated as:

$$\Gamma(t) = \left\{ \mathbf{x} \mid \varphi(\mathbf{x}, t) = 0 \right\} \quad (2.27)$$

where φ is the level set function, and the computation of its evolution in time is defined by

$$\frac{\partial \varphi}{\partial t} = -v_g |\nabla \varphi| \quad (2.28)$$

where v_g , as defined in chapter 1, is the growth speed of the crystallization. The main advantages of the LSM are:

- its intrinsic ability to deal with multiple connected interfaces and their topological changes;
- is n -dimensional;
- the interface presents no discontinuities, with the possibility to calculate always its curvature and its normal vector.

In our case, the sign of the function depends on the phase: positive in the crystalline domain, negative in the amorphous domain.

2.7.1 The crystallization model

The crystallization kinetics of a phase-change material is linked to the nucleation and growth of the crystal phase, as already mentioned in section 1.5. Due to the very fast increase (in the order of 10^{12} K/s) and decrease of temperature (in the order of 10^{10} K/s) associated to the current induced Joule heating of the cell, a transient nucleation rate is considered, that depends on the local temperature variation (dT/dt):

$$I_{nucl} = I_s e^{-\frac{\tau_i}{\delta t}} \quad (2.29)$$

where I_s is the stationary nucleation rate, τ_i is the incubation time and δt depends on dT/dt . I_s is defined by [115]:

$$I_s = N \gamma_a O_n Z_e e^{-\frac{W}{k_B T}} \quad (2.30)$$

N is the density of the possible nucleation sites, γ_a is the characteristic atomic frequency, O_n is the number of atoms at the surface of the critical size nucleus, Z_e is the Zeldovich factor, W is the free energy associated with the creation of a stable nucleus, and k_B is the Boltzmann constant. The regularity of the meshing implemented, made by ‘‘cubic’’ particles, requires the calculation of all the parameters involved in the crystallization equations, assuming that the fundamental nucleus is a cube. This approximation is valid for simulations where the size of the volume of phase-change material considered, is bigger than the critical nucleus volume ($\sim 1 \text{ nm}^3$).

The crystal growth speed, used to compute Γ , according to eq. 1.5, is given by:

$$v_g = \gamma_a d \left(1 - e^{-\frac{\Delta G_v d^3}{k_B T}} \right) \quad (2.31)$$

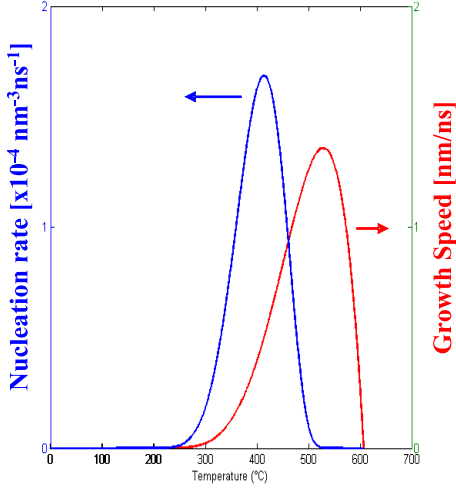


Fig. 2.44. Growth speed and nucleation rate for the $\text{Ge}_2\text{Sb}_2\text{Te}_5$ in the stationary case, as used in our simulations.

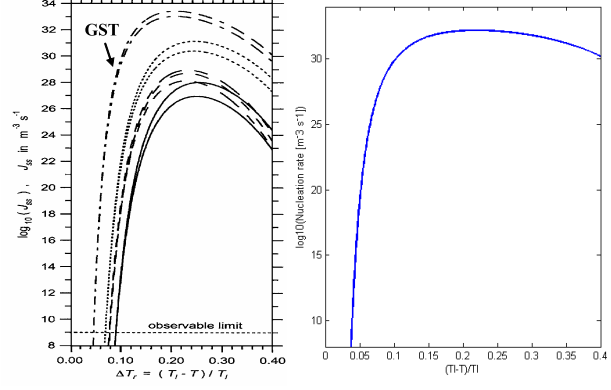


Fig. 2.45. Nucleation rate as a function of the relative undercooling $((T_m - T)/T_m)$ as calculated in [23] (left), and as calculated with eq. 2.30 (right).

where d is the interatomic distance, and ΔG_v is the difference between the Gibbs free energy per unit volume of the amorphous and crystalline phase.

For the implementation of the tool, we considered the $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST) as reference phase-change material, because it has been largely studied and most of its physical parameters are well known. Some of these parameters that we used in our simulations, are reported in table 2.3.

Parameter	Definition	Value
N	density of nucleation sites	10^{23} m^{-3}
d	interatomic distance	$3 \times 10^{-10} \text{ m}$
ρ_m	material density	6150 kg/m^3
M	molar mass	1.026 kg/mol
L_m	latent heat of melting	$11.2 \times 10^8 \text{ J/m}^3$
T_m	melting temperature	880 K
σ_{ac}	crystal-amorphous interface energy	0.1 J/m^2

Table 2.3. Main GST thermodynamical model parameters used in our simulations.

In Fig. 2.44 we report the trends of the nucleation rate and of the growth speed in the stationary case, as a function of the temperature. To validate the crystallization model, we compared the outputs with what already reported in the literature for the GST. In Fig. 2.45 for example, we compare the nucleation rate of our tool, with the graph reported in [23], finding a good agreement.

2.7.2 The electrothermal solver

The electrothermal solver, used to determine the distributions of electric potential V , the electric current density J and temperature T , relies on the coupled system of partial

differential equations formed by the current conservation equation (eq. 2.32) and the heat transfer equation (eq. 2.33)

$$\nabla \cdot \vec{J} = \nabla \cdot (-\sigma \nabla V) = 0 \quad (2.32)$$

$$\nabla \cdot (k_{th} \nabla T) + \sigma |\nabla V|^2 = \rho_m C_p \frac{\partial T}{\partial t} \quad (2.33)$$

where σ , k_{th} , ρ_m , and C_p are respectively the electrical conductivity, the thermal conductivity, the density and the heat capacity of the materials. J is calculated from the gradient of the electric potential ($J = (-\sigma \nabla V)$).

We performed 2D simulations of our PCM cell, considering the y-axis normal to the electrodes of the cell, and the x-axis having origin in the center of the plug of the device. The y-axis is the axis of symmetry of the structure simulated. The associated boundary conditions depend on the cell configuration: Dirichlet boundary conditions on the cell electrodes (north and south), with fixed electric potential and fixed room temperature, and Neumann boundary conditions on the lateral boundaries to guarantee the thermal and the electrical isolation (east and west).

The phase-change material, in our implementation, is treated as a material with four possible phases, and in the following we describe the key points of our model. The four phases are: the amorphous OFF phase, the amorphous ON phase, the crystalline phase, and the liquid phase. T , J and the electric field E , coupled with the level set function, define at each calculation step, in which of these phase is locally the phase-change material. This is the reason why, all the materials parameters in the electrothermal solver are considered constant (for the top electrode, for the dielectric, for the bottom electrode and for the plug), except for the thermal conductivity and the electrical conductivity of the phase-change material in which thermal conductivity depends on the phase and on the temperature while and electrical conductivity depends on the phase, on T , on J and on E .

2.7.3 The thermal conductivity

The thermal conductivity of the amorphous OFF phase is considered constant, equal to $0.2 \text{ W m}^{-1} \text{ s}^{-1}$, while the other phases have a common thermal conductivity temperature

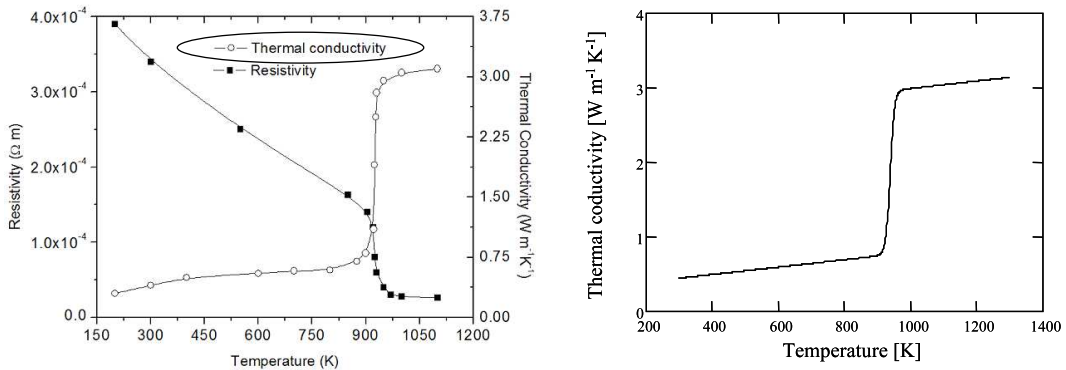


Fig. 2.46. Thermal conductivity of GST as a function of the temperature. On the left the trend reported in [116], and on the right the trend implemented in our tool.

dependent, that starts from $\sim 0.5 \text{ Wm}^{-1}\text{s}^{-1}$ at room temperature and rises abruptly at the melting temperature (T_m) up to more than $3 \text{ Wm}^{-1}\text{s}^{-1}$ [116] (an hyperbolic tangent function is used to preserve the continuity at T_m). In Fig. 2.46 we compare the graph reported in [116] with the thermal conductivity as a function of the temperature introduced in our tool.

2.7.4 The electrical conductivity

The amorphous OFF phase is equivalent in our model to the traditional amorphous phase of a phase-change material in the subthreshold regime, hence when the electric field is lower than the threshold field E_{TH} . In the amorphous phase the conduction is well described by eq. 1.18, derived from the Poole-Frenkel model. The approximation for the electrical conductivity is then:

$$\sigma_{am-OFF} = \frac{A}{|\vec{E}|} e^{-\frac{E_{am}}{k_B T}} \sinh\left(\frac{qB|\vec{E}|}{k_B T}\right) \quad (2.34)$$

that gives the possibility to extract the fitting parameters A and B directly from the experimental results. In our case we found $A = 3.6 \times 10^{13} \text{ A/m}^2$, $B = 3.6 \times 10^{-9} \text{ m}$, and $E_{am} = 0.39 \text{ eV}$.

Once reached the threshold electric field E_{TH} , we considered a model in which the type of conduction changes, and is activated by the electric field. We chose to call this phase “amorphous ON phase” as reported in [42]. Once in this phase, the phase-change material has not recovered the long-range order typical of the crystalline phase, but the electrical conductivity is similar, as illustrated by the perfect superposition of the two curves shown in Fig. 2.1. The main difference between the crystalline phase and the amorphous ON phase, is that the first, at low electric fields, preserves a conductivity higher than the amorphous phase ($\sim 4 \text{ S/m}$ for the amorphous phase and $\sim 700 \text{ S/m}$ for the crystalline phase of the GST), while the latter requires a minimum current density J_H to preserve the high conductivity as mentioned in chapter 1. If the $J > J_H$ condition is not satisfied, the material not crystallized during the persistency of the ON-state, preserves its amorphous structure coming back to the amorphous OFF phase, and recovering the low electrical conductivity. From now, if not differently specified, we will refer generically to the ON-state of the cell, considering equivalent in terms of electrical conductivity the amorphous ON phase and the crystalline phase at high current densities ($J > J_H$).

The other situation in which the material can reach the amorphous ON phase is when the temperature is risen above the melting temperature T_m , melting the material by Joule heating, and then the current density is lowered, remaining at current densities higher than J_H . This is necessary to take into account the recovering of a disordered system, once the material is melted.

The existence of a holding electric field E_H once the phase-change material is in the ON-state, was proposed in [45] where the idea of a saturated electric field was used to justify the changed free energy between the ON-state (in which a filament made of crystalline nuclei is formed in the amorphous region) and the amorphous phase. On the contrary, in [41], the holding voltage V_H is considered as the drop due to the energy gap between shallow and deep traps in the amorphous material, in a double trap energy

levels model. In both the models, once in ON-state (even if not directly specified in the literature) the phase-change material experiences a saturation of the local electric field.

To verify the existence of E_H , we studied the phenomenon in our μ trench structures (plug thickness = 30 nm, trench width = 300 nm), where we integrated the GeTe as phase-change material. From the electrical characterization of the devices we extracted the different electrical parameters, and in particular: the current I_R to RESET the devices (to achieve the 90% of the programming resistance window); the holding voltage V_H ; the resistance of the device once reached the ON-state (R_{ON}). In order to calculate the real contribution of the phase-change material to the ON-state resistance (R_{PCM}), we measured the resistive contributions of the plug (R_{PLUG}) and of the access lines (R_{LINES}) in devices in which we did not integrate the phase-change material. We calculated R_{PCM} from eq. 2.16:

$$R_{PCM} = R_{ON} - R_{PLUG} - R_{LINES} \quad (2.35)$$

Our hypothesis is that the main contribution to the value of R_{ON}^{pcm} is given by the volume of phase-change material, far from the plug and close to the top electrode, that is not involved in the phase-transition and that can be considered out of the active volume. It means that, from the fabrication, this volume of phase-change material not active, preserves its crystalline phase along the life of the memory cell. In a first approximation, we can write:

$$R_{PCM} \simeq \rho_{cr} \frac{h - L}{A} \quad (2.36)$$

where ρ_{cr} is the resistivity of the crystalline phase, h is the thickness of the deposited layer of phase-change material, L is the height of the active region in the ON-state, and A is the equivalent surface of the phase-change material over the plug. If the electric field saturates in the ON-state, we can rewrite eq. 2.36 as:

$$R_{ON}^{pcm} \simeq \rho_{cr} \frac{h - \frac{V_H}{E_H}}{A} = \rho_{cr} \frac{h}{A} - \frac{\rho_{cr}}{A E_H} V_H = c - m V_H \quad (2.37)$$

The dispersion of the values of R_{ON}^{pcm} , can be due to different factors, like the different crystallinity of the material in different wafer areas or the different shape of the amorphous dome. Following our assumption, is exactly this dispersion that can allow to appreciate the linear relation expressed by eq. 2.37 between R_{ON}^{pcm} and V_H . In Fig. 2.47a, we report the trend observed for our devices, where this linear relation is highlighted. From the parameters of the interpolation (m and c), we can also extract the value of the saturated electric field ($E_H = c/(m h)$), the thickness h of the deposited phase-change material being equal to 100 nm: $E_H = 5.7 \pm 0.2$ MV/m. The proposed approximation, does not take into account the fact that the resistivity of the material varies along the phase-change material layer because of the temperature gradient reached during the programming. Despite this, the result confirms the trend. Moreover, the approximated height L of the active region is 60 ± 10 nm ($L \simeq V_H/E_H$), and it did not show any correlation with the programming current I_R . We attributed the variation of the programming current calculated from our results, more to the fabrication variability, observed in particular between devices tested in the center of the

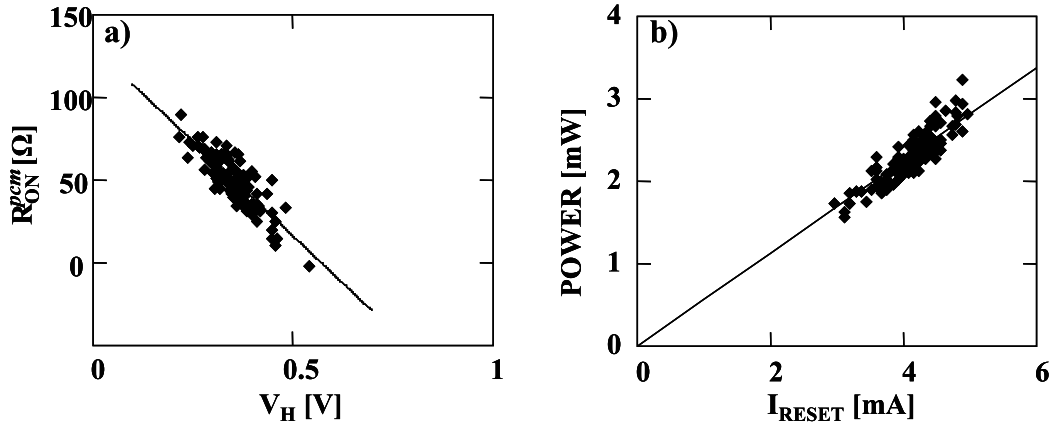


Fig. 2.47. a) Resistive contribution in the ON-state of the phase-change material layer (R_{ON}^{PCM}), as a function of the measured holding voltage (V_H), for all the devices under test. b) Trend of the power dissipated in the phase-change material layer as a function of the programming current, in the RESET operation.

wafer and devices on the edge (tests done on purpose, to increase the variability of I_R). If we suppose this variability due to the plug surface variation (correlated with A), effectively it does not impact the calculation of E_H as seen in eq. 2.37.

The variability of I_R helps us to further confirm the material-dependent nature and the existence of a saturated electric field in the ON-state. We calculated the total power provided to the phase-change material during the RESET operation, according to eq. 2.2:

$$P = V_H I_R + R_{PCM} I_R^2 \quad (2.38)$$

In Fig. 2.47b, we report the trend of the so calculated programming power, as a function of the RESET current. The linearity observed, means that there is a constant voltage drop on the cell during the RESET operation, independent on the programming current. In fact we can write:

$$P = E_H L J_R A + \rho_{cr} \frac{h-L}{A} J_R^2 A^2 = \left[E_H L + \rho_{cr} (h-L) J_R \right] I_R \quad (2.39)$$

where J_R is the current density to RESET the device, that is supposed to be constant, as explained in section 2.1.1. The other terms in the squared brackets, that represent the slope of the data in Fig. 2.47b, do not vary considerably from a device to the other, being affected from variabilities that appear in the plot, as a stochastic distribution of the data around the main linear trend. E_H appears again as a constant saturated electric field, independent of the current and of the voltage applied on the cell, but dependent on the material properties.

Since the ON-state is a state of the cell that is common to the crystalline phase (at high currents) and to the the amorphous ON phase, we decided to model the electrical conduction in both the phases, with the same equation. Moreover, the transition from the ON-state to the liquid phase, does not present discontinuities. Hence, the need to find an equation that describes the conductivity of the ON-state of the phase-change material and that at higher temperatures ($T > T_m$) becomes valid also for the conductivity of the liquid phase. The equation has to take into account the following aspects:

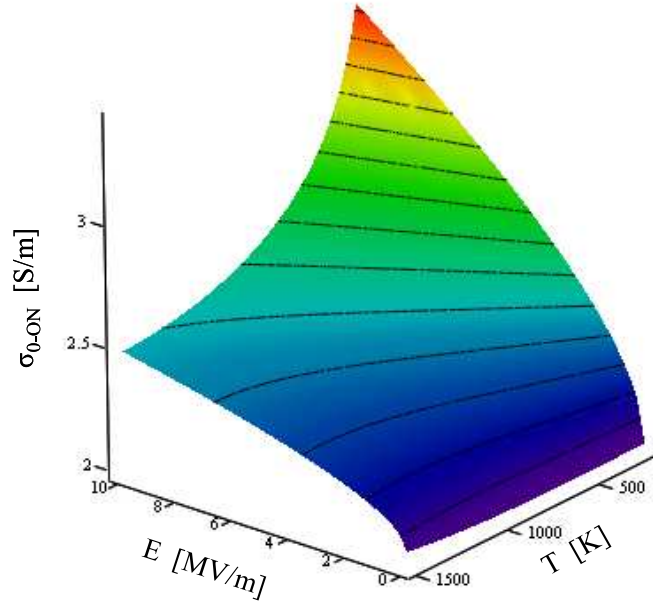


Fig. 2.48. Plot of the term σ_{0-ON} calculated in eq. 2.41, as a function of the electric field and of the temperature.

- the semiconductive nature of the crystalline phase at low electric fields (the electrical conductivity increases with the temperature increase);
- the saturation of the electric field, at high current densities;
- the continuity between the different phases, also to avoid non-convergence problems in the computation;
- the electric field activated conduction in the “sub-saturated” field regime.

The experimental results and the following analysis, led us to describe the electrical conductivity at low fields, with the classical temperature activated equation typical of semiconductor materials, according to eq. 1.11:

$$\sigma_{ON}(E, T) = \sigma_{0-ON}(E, T) e^{-\frac{E_{cr}}{k_B T}} \quad (2.40)$$

where E_{cr} is the activation energy of the conduction of the crystalline phase. The parameter σ_0 enables to describe the conductivity at higher electric fields and higher current densities:

$$\sigma_{0-ON}(E, T) = \sigma_c \frac{e^{\sqrt{\frac{q|E|\lambda}{k_B T}}}}{1 - e^{-\frac{W_{ON}}{k_B T}}} \quad (2.41)$$

where σ_c is a constant, q is the elemental charge, λ is the “percolation” distance, and W_{ON} is what we called “activation energy of the ON-state”. In Fig. 2.48 the term σ_{0-ON} is plotted as a function of the temperature and of the electric field.

We can distinguish in the final equation of σ_{ON} three main components:

- the semiconductive conduction in the low field region $\left(e^{-\frac{E_{cr}}{k_B T}} \right)$;

- the percolative nature of the crystalline phase, with a conduction activated by the electric field $\left(e\sqrt{\frac{q|\vec{E}|\lambda}{k_B T}}\right)$;
- the temperature activated nature of the conduction in the ON-state, characterized by a really high conductivity $\left(\frac{1}{1-e^{-\frac{W_{ON}}{k_B T}}}\right)$.

When the temperature increases by Joule heating in the material, as reported in eq. 2.5, we can estimate the temperature as:

$$T = \alpha_{th} \vec{J} \cdot \vec{E} + T_0 \quad (2.42)$$

where T_0 is the ambient temperature and α_{th} the efficiency term ($\propto 1/k_{th}$). As the temperature raises, σ_{ON} becomes:

$$\sigma_{ON} = \frac{\sigma_c k_B}{W_0} \left(\alpha_{th} \vec{J} \cdot \vec{E} + T_0 \right) \quad (2.43)$$

Then, the Ohm's law gives:

$$\vec{J} = \frac{\sigma_c k_B}{W_0} \left(\alpha_{th} \vec{J} \cdot \vec{E} + T_0 \right) \vec{E} \quad (2.44)$$

Considering the real system of the cell, in which the major component of the current is directed along the plug axis (we consider it to be the z-axis of the vertical structure), we can write the approximation:

$$J_z \simeq \frac{\alpha_{th} \sigma_c k_B}{W_0} J_z E_z^2 + \frac{\sigma_c k_B T_0}{W_0} E_z \quad (2.45)$$

that for high current densities takes to the local saturation of the electric field in the material:

$$E_z^{sat} \simeq \sqrt{\frac{W_0}{\alpha_{th} \sigma_c k_B}} \quad (2.46)$$

The equation of σ_{ON} helps to describe all the different conductivities that the phase-change material experiences passing from the crystalline phase to the liquid phase, or from the amorphous ON phase to the liquid phase. The parameters for the GST, have been extrapolated from the experimental results obtained for lance-type devices and reported in table 2.4.

Parameter	Definition	Value
σ_c	constant factor	2×10^5 S/m
λ	percolation distance	0.5 nm
W_0	activation energy of ON-state	0.5 eV
E_{cr}	activation energy of the conduction	0.15 eV

Table 2.4. Parameters of eq. 2.40 and eq. 2.41, extracted from experimental results, for the GST.

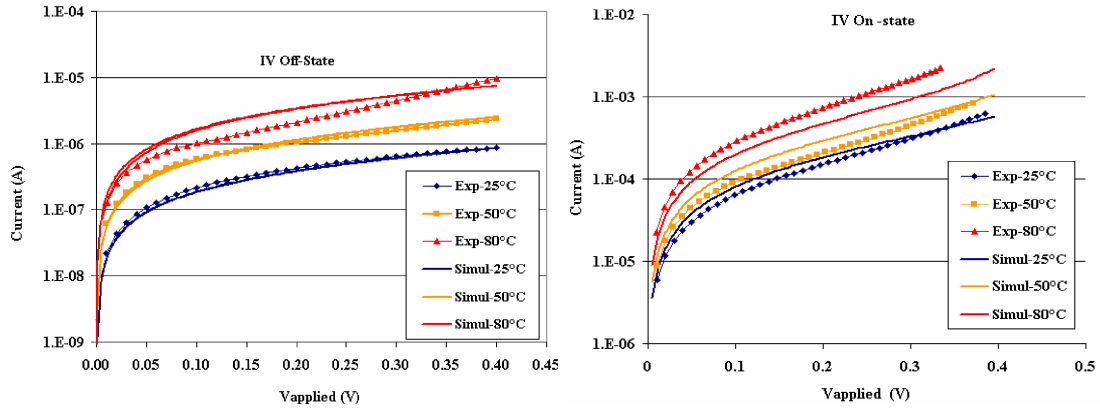


Fig. 2.49. Comparison between experimental and simulated current as a function of the voltage in the low field regime (< 0.4 V), for GST-based lance-type devices. Different working temperatures are considered. On the left we see the results for the amorphous OFF phase (OFF-state), and on the right for the crystalline phase (ON-state).

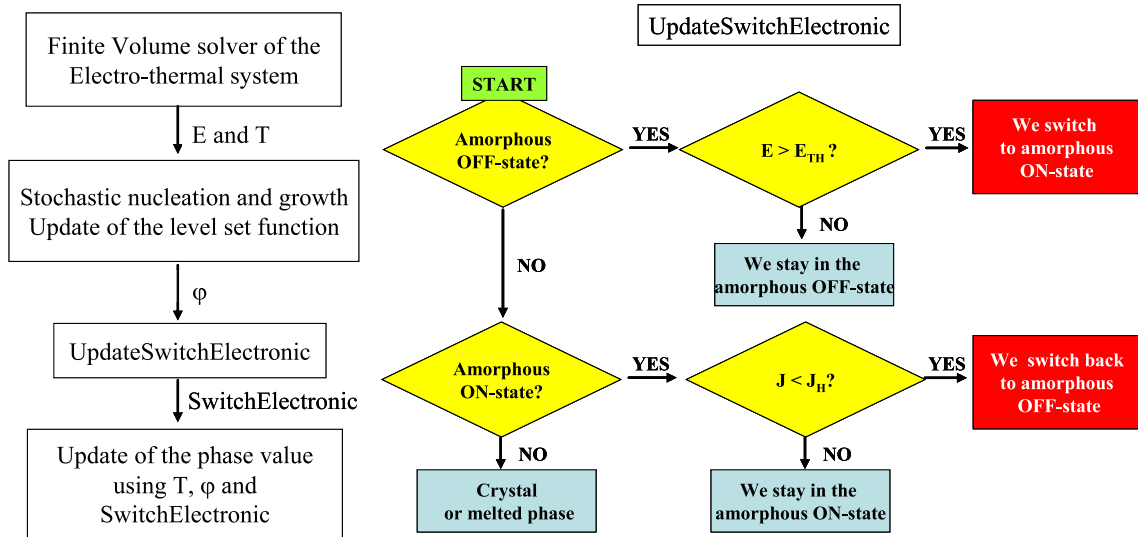


Fig. 2.50. Schematic description of the simulation tool, with its different calculation steps (left). On the right is described the “UpdateSwitchElectronic” sub-program, used to introduce the electronic switching.

Finally in Fig. 2.49, we report the comparison of experimental and simulation results, obtained on lance-type structures (plug diameter = 300 nm), in which we integrated our GST. The current as a function of the voltage (I-V curves) is reported for different temperatures, for the amorphous phase (OFF-state) and for the crystalline phase (ON-state). Even if we obtained a good fitting of the experimental results at low field, we faced a strong variability of the experimental results once the temperature is risen.

2.7.5 Implementation of the electronic switch

The final implementation of the simulation tool, is described schematically in Fig. 2.50 (left scheme). The solver, at a given simulation step of time, computes the solution of

the coupled thermal and electrical equations (eq. 2.32 and eq. 2.33) giving as output \vec{E} and T . The mesh size for the phase-change material is 4 nm. The nucleation rate is calculated and the level set equation is updated, defining if in the crystalline or in the amorphous ON regions, some nuclei are formed and/or grown. The phase-change material mesh is then screened by the “UpdateSwitchElectronic” sub-program described in the scheme on the right of Fig. 2.50. If the the material is in the amorphous OFF phase but the calculated electric field is higher then the threshold electric field E_{TH} (3×10^7 V/m), the material switches to the amorphous ON phase. On the contrary, if the material is in the amorphous ON phase, but the current density is lower then the holding current density J_H (10^9 A/m²) the material switches back to the amorphous OFF phase. The program also verifies if some regions crossed T_m , considering them amorphous ON sites once the temperature is decreased. The last step of the computation is the update of the “phase” variable in all the elements of the mesh of the phase-change material.

2.8 The simulation results

The description of the conductivity of the phase-change material in all its phases, can give an insight into the behavior of the PCM device during the different programming operations. In particular, we wanted to understand the real crystallization dynamics and the electrical behavior of the devices tested during the real experiments, taking into consideration also the characterization setup used. The simulations in fact, take into account the presence of load resistance (R_{LOAD} , that was chosen dependently on the device simulated, as in the our experiments) in series with the device, and of a parasitic capacitance ($C_P = 10$ pF) in parallel with the device as described in section 2.5.1. A pulse is applied to the series of R_{LOAD} and the cell, collecting at pre-selected time steps of the computation, all the values of the main variables (T , E , J , $phase$, etc.) in each element of the mesh.

2.8.1 The simulation of the RESET pulse

In Fig. 2.51 we report the simulation of a RESET pulse applied on a lance-type cell with a 300 nm plug diameter (the initial resistance is 1.5 k Ω). The thickness of the phase-change material layer is 100 nm. The y-axis is considered as the symmetry axis of the structure. The cell in the beginning is fully crystalline. The application of the RESET pulse (width = 50 ns, rise/fall time = 5 ns) rises the temperature in the cell above the melting temperature (880 K) and the material melts above the plug surface (located between 0 nm and 150 nm of the x-axis). At 60 ns the voltage drop on the cell has already started to decrease, like the temperature in the material. The phase-change material gradually passes to the amorphous ON state, maintained by the current in the cell that decreases with a time constant $\simeq R_{ON}C_P$. After the pulse, at 73 ns, the temperature definitely comes back to the room temperature, and the current density drops below J_H . The fast fall time does not give the possibility to the material to crystallize, leading to an amorphous dome that covers the plug surface. Nevertheless, some nuclei had the possibility to form during the falling edge of the pulse (represented

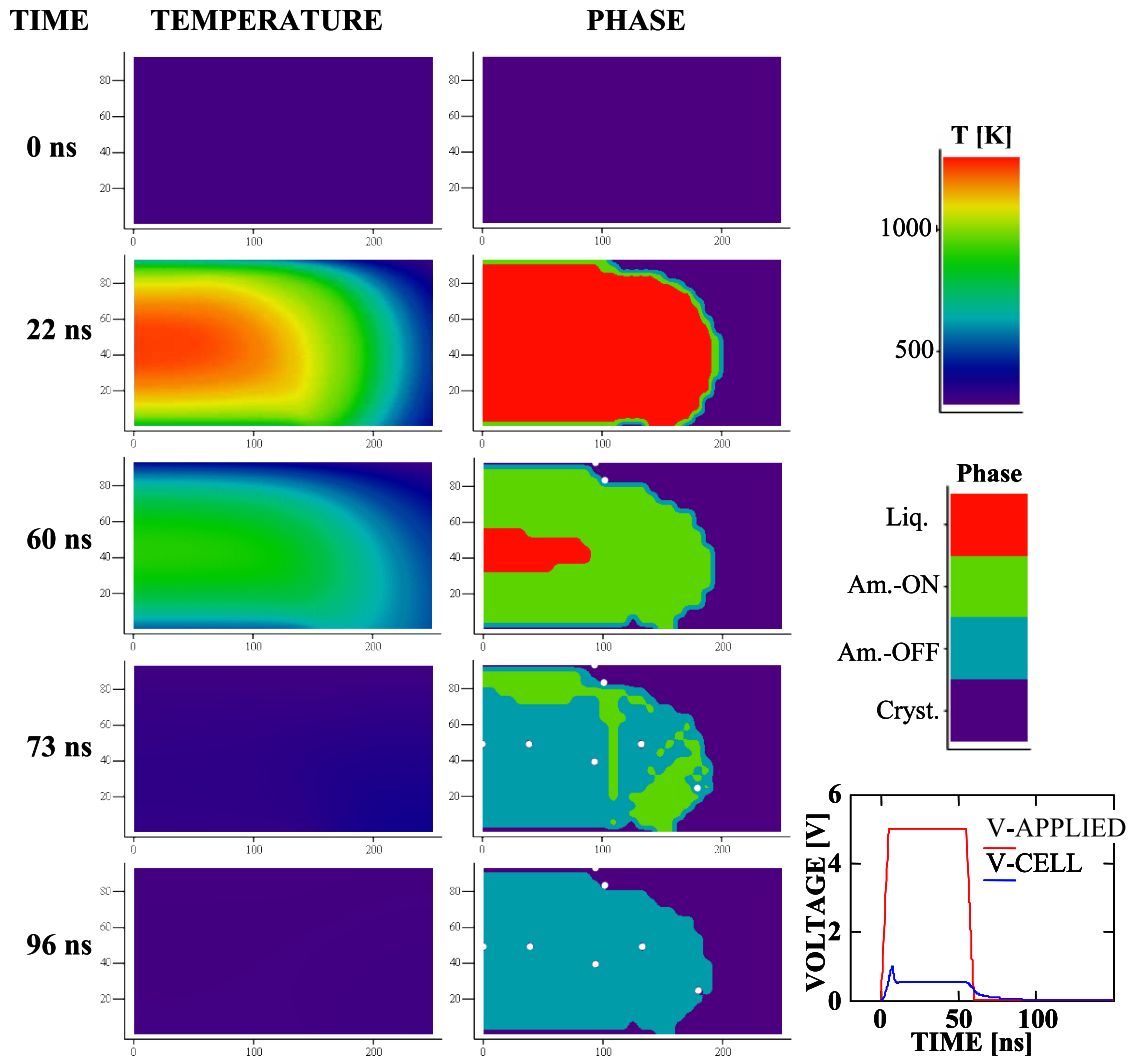


Fig. 2.51. Simulation of a RESET pulse, applied on a pre-SET lance-type cell (the starting resistance is 1.5 k Ω). The x-axis and the y-axis scales are in nm. The radius of the plug (not shown) is 150 nm. The plots show the evolution of the temperature and of the phase in the phase-change material region, at specific time steps. On the right is reported the time evolution of the voltage applied on the series of R_{LOAD} and the cell, and of the voltage drop on the PCM device. After the pulse application the cell reaches a resistance of 380 k Ω

in the picture with white dots), but without the possibility to grow. The final device resistance is 380 k Ω .

2.8.2 The simulation of the SET pulse

The simulation of the SET pulse, starts with a cell in the RESET state (390 k Ω), hence with an amorphous dome that covers the full plug surface (Fig. 2.52). A pulse shape similar to the RESET pulse is chosen, but with lower amplitude. The charging of the parasitic capacitor at the beginning of the pulse (< 20 ns), delays the reaching of the threshold voltage. At 20 ns, the amorphous OFF region at the edge of the plug, being the thinnest, reaches the critical electric field E_{TH} and switches to the amorphous ON

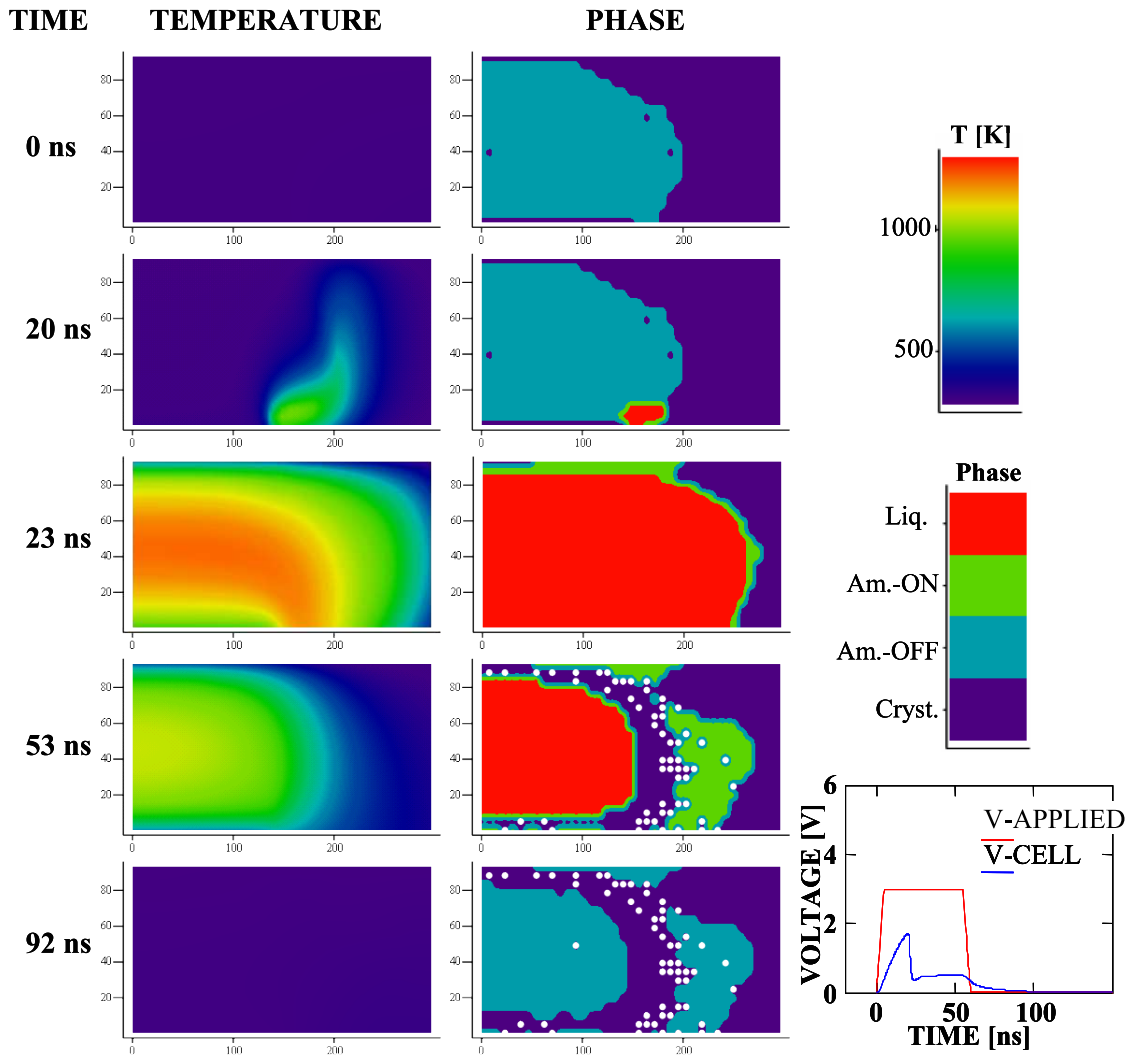


Fig. 2.52. Simulation of a SET pulse, applied on a pre-RESET lance-type cell (the starting resistance is 390 k Ω). The x-axis and the y-axis scales are in nm. The radius of the plug (not shown) is 150 nm. The plots show the evolution of the temperature and of the phase in the phase-change material region, at specific time steps. On the right is reported the time evolution of the voltage applied on the series of R_{LOAD} and the cell, and of the voltage drop on the PCM device. After the pulse application the cell reaches a resistance of 6.5 k Ω

phase. The conductivity of this region increases rapidly, and it experiences the discharging of the parasitic capacitor C_P . The fast rising of the current density, increases locally the temperature above the melting temperature, melting the material. At 23 ns, the current spike has already melted a big portion of the phase-change material area, that gradually decreases as the temperature in the system regains stability, after the transient phenomenon. Before the falling edge in fact (53 ns), the liquid area is reduced. The rest of the previously melted material had the possibility to recrystallize, passing through the amorphous ON phase, in which some stable nuclei formed and had the possibility to grow. At 92 ns the system is stable, with a considerable region recrystallized during the pulse application. The pulse was not able to recrystallize perfectly the cell, because of the sharp falling edge, but the final resistance of 6.5 k Ω is already

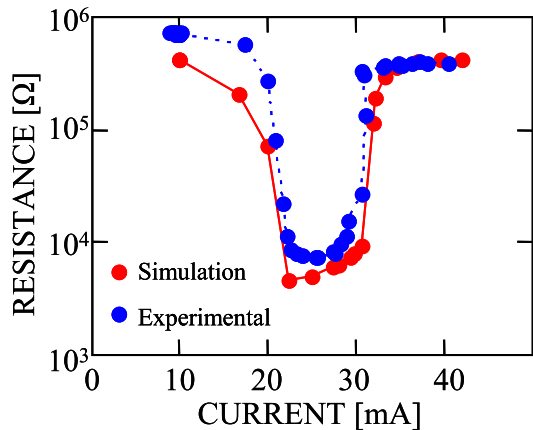


Fig. 2.53. Simulated and experimental results of the resistance as a function of the programming current, for a lance-type PCM device.

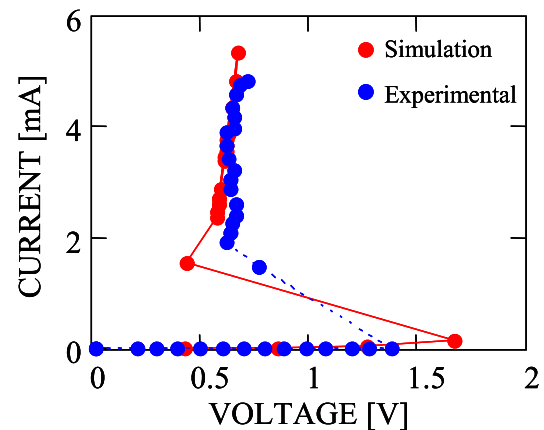


Fig. 2.54. Simulated and experimental results of the current as a function of the voltage drop on the cell, for a μ trench PCM device.

in the order of magnitude of the starting SET state of the previous section (1.5 k Ω).

2.8.3 A complete cell characteristic

We simulated the behavior of the devices that we fabricated, analyzed in the previous chapters, also to understand the impact of the temperature on the thermal stress of the PCM cell. As reported in Fig. 2.43, we demonstrated the reduced thermal stress in the μ trench structure, during the SET operation, at high working temperature. Moreover, we reproduced with the model proposed, the programming characteristics of the cell. In Fig. 2.53 we report the resistance of a lance-type cell (diameter = 300 nm) as a function of the programming current (R-I). The simulation reproduces what obtained during the real experiments, and in particular we find a correspondence in the SET current, the SET resistance, the RESET current and the RESET resistance. The points at low current values of the experimental results (blue), show a higher resistance value with respect to the final RESET resistance obtained at current values higher than 35 mA. On the contrary, the simulations show always the same RESET resistance. This is because in our simulations we did not take in consideration the drift phenomenon.

Fig. 2.54 shows the current as a function of the voltage drop on the cell (I-V), during the programming of a μ trench device (the thickness of the plug considered is 30 nm, while the trench width is 300 nm). The simulated and the experimental characteristics show a similar trend. We have almost the same threshold voltage ($\simeq 1.5$ V): the mismatch observed, is in the order of magnitude of the variability of the real threshold voltage, that depends on slight variations of the amorphous region thickness (a variation of 5 nm corresponds to a variation of ~ 0.15 V). Moreover, the characteristics show the same holding voltage V_H ($\simeq 0.5$ V), as theorized in our model.

2.9 Summary of the chapter

Phase-change memory demonstrated in the last decade the possibility to fulfill the increasing demand of scalability and power reduction, in particular to address the replacement of embedded Flash technology, experiencing more and more scaling limitations. Different PCM device structures have been proposed in last years in order to reduce the memory size. We presented, at first, the lance-type structure, based on a metallic via that provides the contact with the integrated phase-change material. This simple vertical structure experiences the scaling limitation due to the lithography technology resolution. This idea evolved into the confined structure, where the shrunk “hole” created to fabricate the memory, is filled with the phase-change material. The main constraint of this structure, is the need of a highly conformal deposition technique. Other structure designs, started to take advantage of the control of the thickness of a metal layer, in order to reduce the interface area between the plug element and the phase-change material. This is the case of the μ trench structure, that demonstrated the industrialization feasibility of the PCM technology. Its direct evolution, is the so called “Wall” structure that revealed to be the best compromise in terms of fabrication process, scaling capability and device engineering opportunity.

The growing technological maturity of PCM has to be supported by a growing research in the reliability issues faced when the device is highly scaled or subject to particular stress/working conditions (e.g. high operation temperature). In this context we implemented the plug structure, the confined structure and the μ trench structure in order to study their main aspects, firstly in term of scalability, and secondly in term of engineering of the performance to address embedded applications, as we will describe in the next chapter. We coupled this study, with the analysis of state-of-the-art “Wall” PCM devices fabricated in collaboration with STMicroelectronics. We introduced in the chapter, the main reliability aspects correlated with the PCM technology:

- the cycling endurance, impacted by the scaling. The lower is the interface area between the plug and the phase-change material, the higher is the probability of mechanical failures, due also the the thermal stress faced by the device during the programming;
- the subthreshold switching, that can cause the switching of the cell below the threshold voltage, when the pulse is sufficiently long and/or the temperature is high enough;
- the phase-change material elemental segregation, that can reduce the life time of the cell;
- the retention of the data, affected by the incoming crystallization of the phase-change material at high temperatures;
- the drift of the cell resistance towards higher resistance values;

- the decrease of the threshold voltage, when the temperature is risen;
- the cell-to-cell thermal cross-talk between adjacent cells.

We analyzed in detail some of these issues in the specific case of the μ trench structure. We revealed also the strong impact of the thermal stress generated in the cell by the SET operation, on the final life time of the device, showing how the endurance can be improved from 10^8 up to more than 10^9 , when at higher temperatures this effect is softened.

Finally, we presented the simulation tool implemented in MATLAB and C code, used to simulate the behavior of our PCM devices. The tool has been implemented taking in consideration the thermal and the electrical properties of a phase-change material, in particular introducing a new equation to model the conduction of the ON-state and the liquid phase. Our tool allowed us to fit the electrical behavior of different structures under test, understanding the different mechanisms taking place in the cell during the RESET and the SET operations.

Chapter 3

The reliability optimization of the embedded Phase-Change Memory

Different ideas to reduce the phase-change memory device size have been proposed in recent years, based on the engineering of the cell structure, and finally reducing the programming current. But the power consumption is not the only problem that we have to face. To overcome the problem of the retention of the information at high temperature, the engineering of the cell structure can be a possible key-road. However, once reached the nm scale as in state-of-the-art devices, the only possible solution is the engineering of the integrated phase-change material. Hence, our interest in the study of new phase-change materials to overcome most of the limitations correlated with the embedded PCM technology, in particular to address automotive and multi-level applications.

Nowadays, $\text{Ge}_2\text{Sb}_2\text{Te}_5$ is recognized as the reference chalcogenide material for standard PCM in consumer market applications [117, 118]. One of the most critical bottlenecks of $\text{Ge}_2\text{Sb}_2\text{Te}_5$, is the low crystallization temperature (~ 140 °C) [119] making intrinsically impossible to satisfy the standard 85 °C 10-years data retention requirements. In the last decades a lot of efforts have been put in the research of new materials and in the study of their properties to target automotive applications, for which the operating temperature is in the range of 150 °C. To address this requirement, different approaches at material level are possible. A first one is mainly based on changing the stoichiometry of $\text{Ge}_2\text{Sb}_2\text{Te}_5$ or adding dopants to increase the stability of the amorphous state [120, 121]. Another solution is to look for different materials with higher crystallization temperature.

In this chapter we describe how we engineered the GeTe stoichiometry to increase its crystallization temperature and then to improve the final thermal stability of the high resistance state of the cell. Then we show how the threshold voltage reduction experienced at high working temperature, can be overcome with SiO_2 doping. Moreover, we analyze the effects of C-doping on the speed and on the programming current in GST based memory devices. Finally, we present how the Ge enrichment can boost the data retention of the PCM cell, despite the reduction of the programming speed. We demonstrate the possibility to overcome this reduction, and the benefit of our innovative programming procedure on the drift of the cell, addressing for the first time the problem of the stability of the low resistance state of the cell.

3.1 $\text{Ge}_x\text{Te}_{100-x}$

Already in the '70s, some works started to focus on GeTe as suitable candidate for optical storage [122, 123]. In fact, GeTe is particularly interesting for device application because of its large resistivity window (4-5 orders of magnitude between the amorphous and the crystalline state) [124]. Furthermore, the high crystallization speed (in the order of nanoseconds [125]) and the high crystallization temperature (~ 180 °C) make GeTe a good candidate for integration in memory devices to address automotive applications. It has been also demonstrated by Wong et al. how the shrinking till the nm size, doesn't impact the final phase-change behavior of this material, showing how, single nanoparticles of GeTe, still are able to switch from a SET to a RESET state [5]. Chen et al. [123] showed that the GeTe 50:50 stoichiometric composition exhibits a very fast crystallization behavior, while, when the 50:50 composition is not respected, the alloys become very slow, this behavior being explained by a possible material segregation. In more recent years, Raoux et al. published a detailed analysis of the crystallization behavior of as-deposited amorphous and melt-quenched amorphous $\text{Ge}_x\text{Te}_{100-x}$ thin-films [20]. By means of optical characterization, the study confirmed the fast behavior of the GeTe compounds, and highlights the complexity of the crystallization process of this material, which appears to be strongly dependent on the Ge at. % content. Moreover Bruns et al. integrated GeTe in PCM devices, demonstrating high speed SET and RESET operations in the order of ns [126]. In the light of these works, we started to analyze $\text{Ge}_x\text{Te}_{100-x}$ compounds (where x varies from 36 up to 69) integrated in final phase-memory devices. Starting from the material analysis performed on thin films, including the results of temperature-dependent resistivity, x-ray diffraction (XRD) and optical cartographies, we moved to a detailed study of the influence of Ge as well of Te enrichment on the memory devices electrical performance, such as programming characteristics, endurance, and data retention properties.

3.1.1 RBS, resistivity and XRD measurements

Amorphous Germanium Telluride thin films of 100 nm thickness were deposited on $\text{SiO}_2(500 \text{ nm})/\text{Si}$ substrates by co-sputtering from Ge and Te elemental targets. Five different compositions were deposited. The Ge content was measured by means of Rutherford backscattering spectrometry (RBS) yielding fractions from 36 up to 69 at. % (the error being ± 1 at. %).

Resistivity measurements were performed as a function of the temperature by means of the 4-point measurement technique, while the samples were annealed up to 400 °C with different constant heating rates. The results for a 10 °C/min temperature ramp are shown in Fig. 3.1 and compared to the same measurements performed on $\text{Ge}_2\text{Sb}_2\text{Te}_5$ films used as reference. All the samples show a first transition with a sharp drop in resistivity corresponding to the GeTe crystallization, at temperatures between 160 °C and 250 °C.

For the stoichiometric 50:50 compound (i.e. for 44 and 53 at. % Ge), the temperature of the first crystallization remains under 190 °C, while it reaches more than 225 °C for 36 at. % Ge, in agreement with previous works [123]. As reported in [124], the formation of stronger Ge-Te bonding in Te-rich alloys, instead of the weaker Ge-Ge

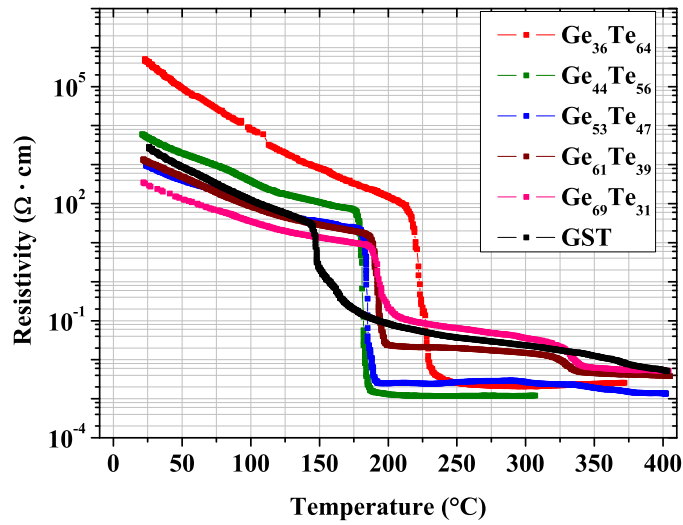


Fig. 3.1. Temperature-dependent resistivity measurements performed on 100 nm thin $\text{Ge}_x\text{Te}_{100-x}$ films. The results reported are for a heating rate of $10^\circ\text{C}/\text{min}$.

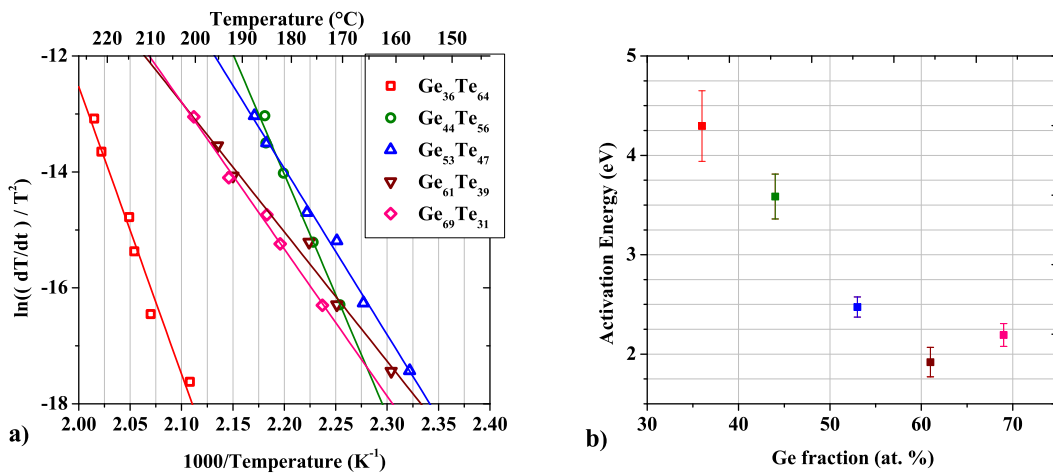


Fig. 3.2. a) Kissinger plots of crystallization temperature for the five compounds under test. $\text{Ge}_{36}\text{Te}_{64}$ shows the higher crystallization temperatures for all the heating rates applied. The Activation Energies are extracted from these plots and reported in b) as function of Ge at. % content.

bonds, delays the Te precipitation and the subsequent GeTe crystallization. The increase of the Te fraction improves the amorphous phase stability, as suggested by the higher crystallization temperature. Furthermore, the largest difference between the amorphous and the crystalline resistivity is shown by the tellurium-rich $\text{Ge}_{36}\text{Te}_{64}$ alloy. On the other hand, concerning the Ge-rich region, $\text{Ge}_{61}\text{Te}_{39}$ and $\text{Ge}_{69}\text{Te}_{31}$ show a first transition at temperatures lower than 200°C and then a second transition, likely due to the segregation of cubic-Ge, at temperatures higher than 325°C .

By the Kissinger method presented in section 1.7.4.2 (Fig. 3.2a), we calculated the activation energies of the crystallization process of the first transition for the GeTe materials, represented in Fig. 3.2b. The highest activation energy is found for $\text{Ge}_{36}\text{Te}_{64}$ ($W_{cr} = 4.3 \pm 0.4$ eV), while the lowest for $\text{Ge}_{61}\text{Te}_{39}$ ($W_{cr} = 1.9 \pm 0.1$ eV). The decrease of the activation energy of the first crystallization, as the Ge content increases is another confirmation of the hypothesis made before. The decrease of Ge-Te bonds in the

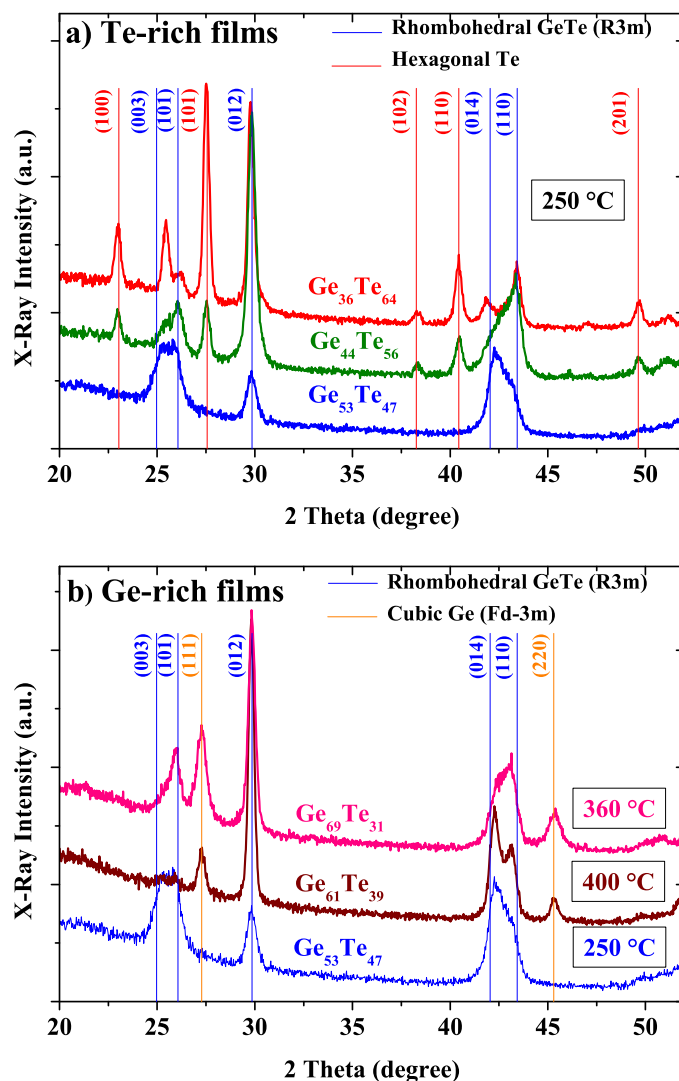


Fig. 3.3. Intensity of XRD peaks at different 2θ angles of diffraction, after annealing at specific temperatures (reported in the graphs). a) In Te-rich samples the (003), (101) and (012) peaks are characteristic of rhombohedral α -GeTe, that coexists with the formation of hexagonal-Te. b) In Ge-rich alloys, the (111) and (220) peaks (green lines) are characteristic of cubic-Ge. Note that GeTe exhibits rhombohedral structure after first crystallization at 185 °C, while it passes to the cubic structure (fcc) when annealed at temperature higher than 325 °C in agreement with [20].

material, reduces the stability of the amorphous phase, leading to a likely crystallization and precipitation of the GeTe compound. To achieve the full crystallization in Ge-rich samples, we have to increase the temperature to make possible the Ge diffusion and then the cubic-Ge precipitation.

In Fig. 3.3 are reported some of the x-ray diffractions (XRD) performed on the five compositions. For Te-rich samples ($\text{Ge}_{36}\text{Te}_{64}$ and $\text{Ge}_{44}\text{Te}_{56}$) we observe the evidence of the crystalline rhombohedral GeTe and hexagonal Te at 250 °C (a). As previously demonstrated in [20], the crystallization of GeTe and Te occurred simultaneously at the same temperature. Close to the 50:50 stoichiometric composition, the $\text{Ge}_{53}\text{Te}_{47}$ sample shows only the peaks characteristic of the presence of rhombohedral α -GeTe. For Ge-rich samples (b) the segregation of cubic Ge into a crystalline GeTe matrix is

confirmed for temperatures higher than 325 °C (as previously observed in resistivity measurements of Fig. 3.1). This is highlighted by the appearance of the (111) and (220) peaks typical of cubic-Ge in Ge₆₁Te₃₉ and in Ge₆₉Te₃₁. Raoux et al. [20] have demonstrated the successive crystallization of GeTe and Ge, the latter occurring at a higher temperature.

3.1.2 Optical characterization at the static tester

Characterization at the optical static tester by means of laser beam pulses allows having an insight on the dynamical behavior of the phase-change alloys under write/erase operating conditions. In Fig. 3.4 we see the recrystallization cartographies showing the relative change of the reflectivity of previously amorphized dots, as a function of the power and duration of the erasing laser pulses. Looking at the result for Ge₅₃Te₄₇, we observe a strong change of reflectivity even for pulse duration lower than 50 ns. Moving to the other compounds, the same pulse duration provides lower reflectivity variations. Ge₃₆Te₆₄ alloy does not show any sign of crystallization for power/time used in our test.

Ge₅₃Te₄₇ in the range of power where the crystallization takes place, shows a reflectivity that varies randomly. We attribute this to a low nucleation rate and to a high growth rate [127, 128]. In fact if the nucleation rate is low, for short laser pulses (< 50 ns) the final probability to have at least one nucleus is very low. But when the first nucleus appears, it grows really fast thanks to the high growth rate.

Moving to the Te-rich compounds, we observe a slower crystallization with respect to Ge₅₃Te₄₇, attributed to the delay produced by the Te separation on the formation of the GeTe compound. On the other hand, in Ge-rich samples the crystallization dynamics (incubation time and crystallization speed) are only slightly affected by Ge enrichment.

The material characterization analysis allowed us to conclude that a slight departure from the 50:50 stoichiometric composition, ranging from Ge₅₃Te₄₇ to Ge₄₄Te₅₆, does not provide any substantial difference in the amorphous-to-crystalline transition. The Te-rich Ge₃₆Te₆₄ shows a slow crystallization behavior confirmed in optical erase operation and it exhibits the largest resistance window between the amorphous and the crystalline state. Ge-rich alloys show cubic Ge-segregation.

3.1.3 Memory Device Characterization

All the wafers tested have been processed in the same batch, thus allowing the analysis of the dependence of the electrical performances on the materials properties. The devices under test were initially in the low resistance state (SET state). In order to perform the first SET-RESET program curve, we applied a staircase-up sequence of 100 ns wide pulses (10 ns fall time) to each cell. After each pulse, the cell resistance is read in order to follow the amorphisation process. The results are reported in Fig. 3.5. The transition to the amorphous state (RESET state) of the materials happens in a narrow range of currents, affected in the case of Ge₄₄Te₅₆, by the initial resistance state of the cell particularly low. The graph confirms results of the resistivity measurements: the Ge₃₆Te₆₄-based devices have the highest resistance window and the highest resis-

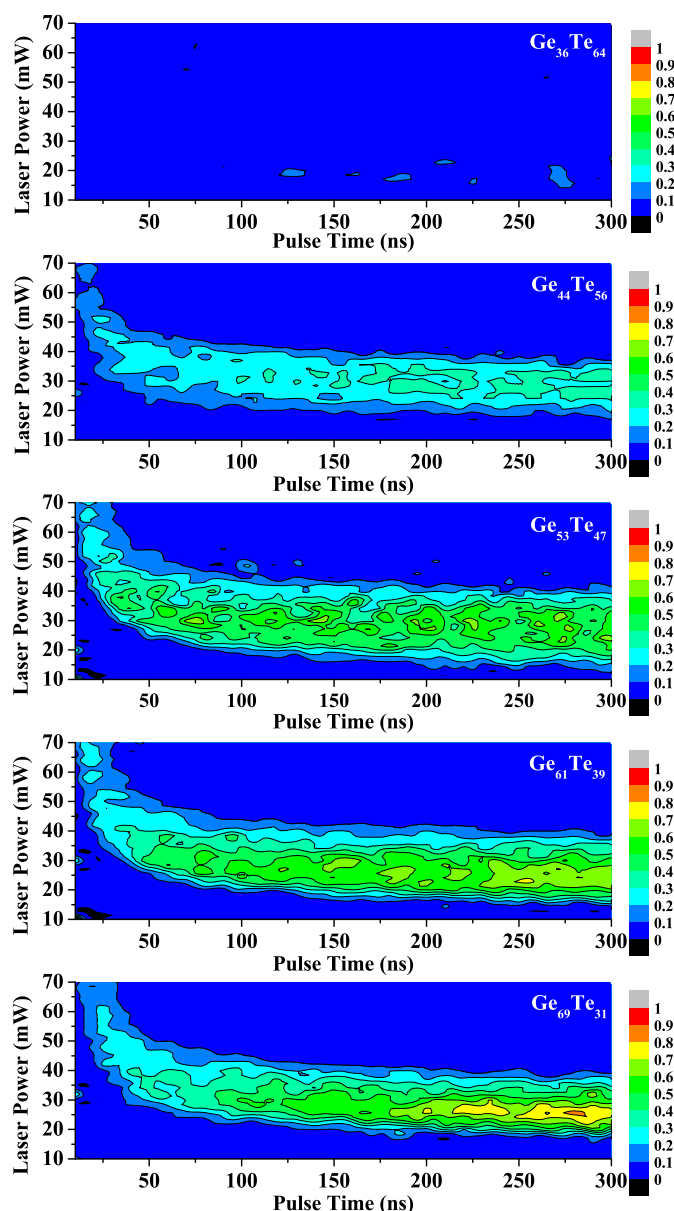


Fig. 3.4. Optical cartographies representing the relative change of reflectivity, after the application of the recrystallization pulse on a laser-amorphized dot. Colors vary from blue to red: respectively unchanged amorphous dot and maximum recrystallization.

tance value in the RESET state. Furthermore, the current needed to take the cells to the RESET state is the lowest in Te-rich $\text{Ge}_{36}\text{Te}_{64}$ devices (~ 30 mA).

The devices were then programmed with an iterative procedure at room temperature: in order to start from a high resistivity state, we applied a 100 ns wide RESET pulse, high enough to melt the phase-change material, with a 10 ns fall time to rapidly quench the device. Then we applied to the amorphized cell, a program pulse of increasing amplitude, at each iteration step. The final resistance of the device was read after each program pulse.

Five widths of the program pulse have been selected for each stoichiometry (Fig. 3.6), in order to bring out the main performances of the cells and their relation to the ma-

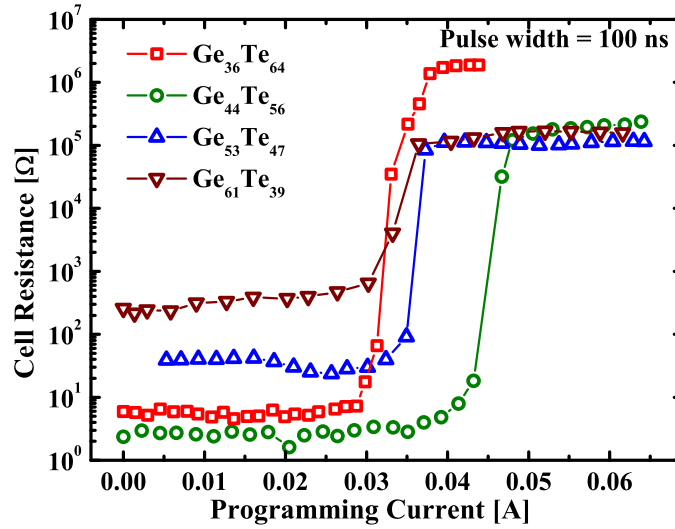


Fig. 3.5. First SET-RESET program curves for different Ge content. The resistance of the cells is plotted versus the programming current.

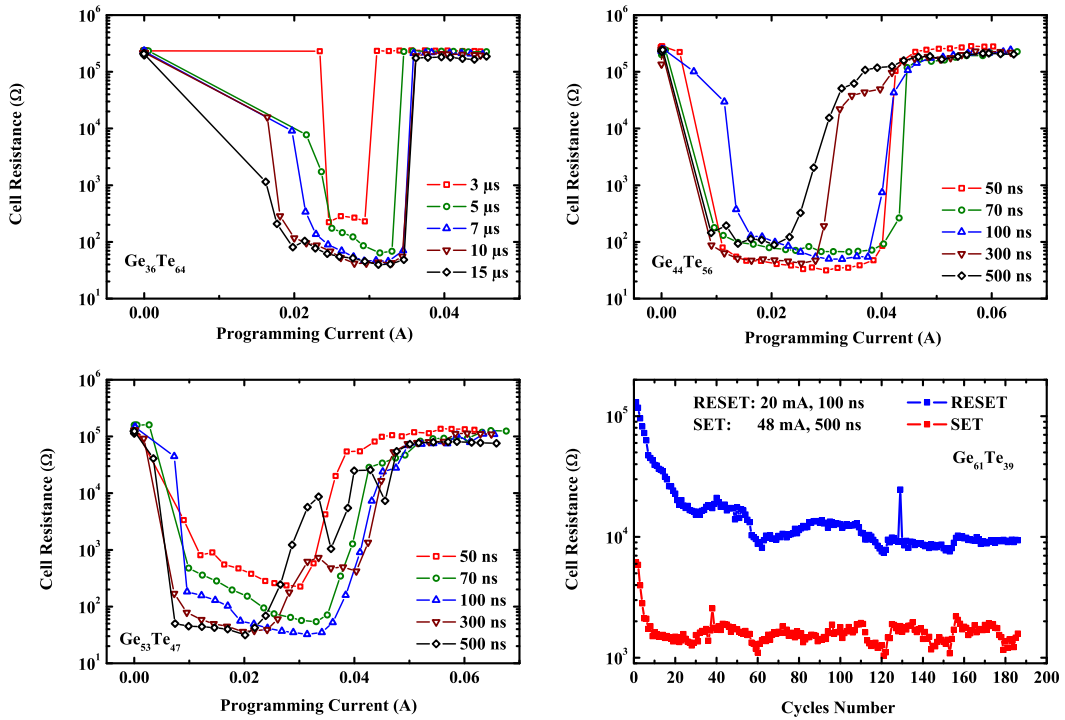


Fig. 3.6. Programming curves for the Te-rich $\text{Ge}_x\text{Te}_{100-x}$ compositions, showing the different performances in terms of speed and program current (average values on three cells). The RESET state instability is plotted for $\text{Ge}_{61}\text{Te}_{39}$.

materials features (i.e. crystallization speed and melting temperature). $\text{Ge}_{36}\text{Te}_{64}$ -based devices need long SET pulses (in the order of microseconds) to show a recrystallization of the active phase change area, in agreement with the results obtained by our optical tests (Fig. 3.4). The long crystallization time might be correlated with the expected phase separation between Te and the compound GeTe , requiring a slow diffusion process. On the other hand, we note the high speed in SET operation for $\text{Ge}_{44}\text{Te}_{56}$ and

Device	Min SET	SET	RESET
	Time Width	Power	Power
	[ns]	[MW/cm ²]	
Ge ₃₆ Te ₆₄	3000	7.1	65.1
Ge ₄₄ Te ₅₆	50	3.4	79.2
Ge ₅₃ Te ₄₇	50	3.3	87.7

Table 3.1. Programming pulse parameters for Te-rich compounds.

Ge₅₃Te₄₇, where the lowest SET resistances are achieved with the shorter SET pulse of 50 ns: this SET resistance is more than three orders of magnitude lower than the RESET resistance. The difference in the crystallization dynamics once we increase the Te content, pointed out in our optical tests and in the literature [20, 127, 128], is also evident in electrical tests on phase-change memories. In addition to the low speed, the Ge₃₆Te₆₄ composition shows the lowest RESET current.

RESET and SET power densities are indicated in Table 3.1 (the criterion used to calculate the SET current, is the reaching of a resistance lower than three orders of magnitude with respect to the RESET state). We observe that the power necessary to crystallize the cells increases with the Te content, and this result can be related to the crystallization temperature trend observed in resistivity measurements (Fig. 3.1). The power necessary to RESET the cells (correlated to the melting temperature) is in agreement with the phase diagram for the binary GeTe system [123]: increasing the Te fraction, the liquidus temperature decreases as reported in [125].

The Ge₆₁Te₃₉ does not show a stable RESET state during repeated program cycles (see Fig. 3.6): Ge-segregation plays a negative role in the repeatability of the electrical characteristics. This problem is even more serious in Ge₆₉Te₃₁ alloy (not shown here). In this case a first RESET pulse is able to take the material to the amorphous phase. Then the following recrystallization is possible, but because of the Ge-segregation (and its high stability in the cubic phase), the cell remains stuck in a permanent SET state.

3.1.4 Effects of the growth speed on the RESET-SET characteristics

Once we increase the width of the programming pulse in the fastest compounds (44 and 53 at. % of Ge content), we observe a decreasing of the current needed to amorphize the phase-change material. We highlight that this happens when we try to RESET again a cell, already in the RESET state (Fig. 3.7a). Taking into account that in the range of pulse durations explored in the experiment, we reach a stationary regime for the temperature, largely before the end program pulse, we would rather expect the RESET current not to depend on the pulse duration. Once reached the stationary regime in the cell in fact, the melted volume is stable, and the melt quenching and the final resistance state of the cell, are affected only by the fall time of the pulse. To explain why the result is not matching this hypothesis, we analyzed in detail what is happening during the pulse application in our cells.

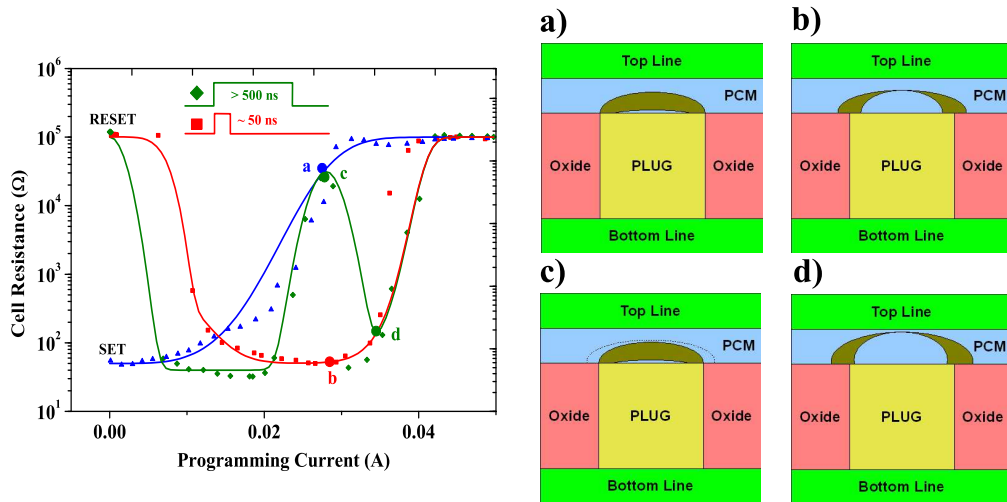


Fig. 3.7. In the left graph, experimental points are interpolated, to evidence the differences in the RESET-SET characteristics of $\text{Ge}_{53}\text{Te}_{47}$ samples, obtained with different pulse widths (in red 50 ns, in green 500 ns). In blue are reported the data relative to the SET-RESET characteristic (not affected by the pulse width). Applying more than 20 mA on a SET cell, the melted material is quenched in an amorphous dome that covers the plug interface (inset *a*). The same amount of current, applied on a RESET cell for 50 ns, takes the device to a SET state (inset *b*). Only increasing the duration of the programming pulse (inset *c*) the residual amorphous regions generated far from the plug interface (after the current spike caused by the electronic switch) are recrystallized, recovering the same thermal stationary conditions observed in inset *a*. If we increase the current in the case of the 500 ns pulse (inset *d*), the melted volume is even higher, and the longer will be the pulse width necessary to recover the stationary condition.

Our analytical device is not able to perform a self-limitation of the current during the electronic switch event (namely the change from RESET state to the high conductive state, called ON-state). The discharge of the parasitic capacitance during the SET operation, gives rise to a spike of current and a related increase of the temperature in the cell [129]. The temperature reached during this spike enables the melting of a large volume of phase-change material. Then the current decreases in time range in the order of the characteristic time constant of the discharge (~ 1 ns). The fast decrease of the temperature in the regions far from the plug interface provides residual amorphous domains that are preserved also once the stationary thermal conditions are restored during the pulse applied (after the spike transient). Since the thermal resistivity of amorphous GeTe is higher than the crystalline [16], the thermal barrier created by these amorphous domains, enhances the recrystallization of the volume of material closer to the plug interface, at the end of the pulse applied. This can be possible only if the growth speed of the material is sufficiently high (since the fall time of the pulse is 10 ns). This situation is described in Fig. 3.7b, and confirmed by the TEM image reported in Fig. 3.8.

If now we increase the duration of the pulse, we can achieve the recrystallization of these residual amorphous regions far from the plug center (in fact far from the plug, the temperature is lower and so the growth speed), and then restore a situation in which the melted region is not surrounded by any amorphous domains. In this case, at the

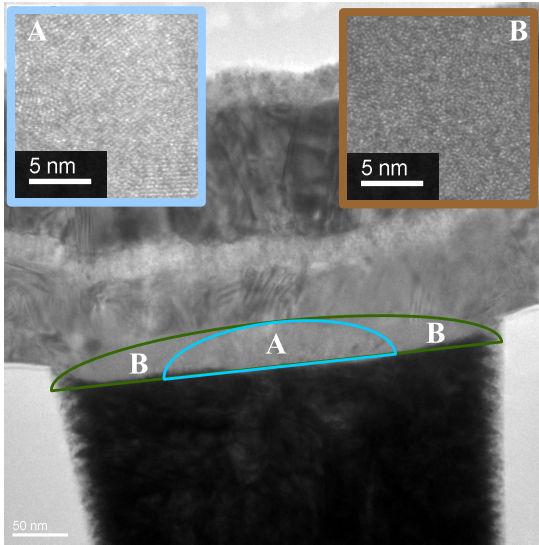


Fig. 3.8. TEM image representative of the inset *b* of Fig. 3.7. Is evident the presence of a polycrystalline region (A) and of the lateral residual amorphous regions (B).

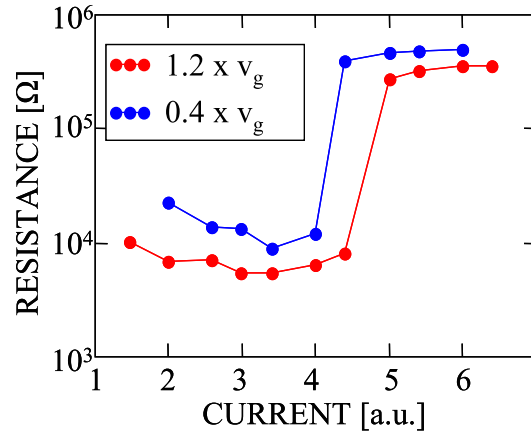


Fig. 3.9. Simulations of the R-I characteristics obtained for a lance-type device, increasing and decreasing the standard growth speed of the GST (multiplied by 1.2 and 0.4), in order to study the effects of the growth speed on the programming curves.

end of the pulse, the high thermal conductivity of the crystalline GeTe surrounding the melted volume, fast quenches the material in an amorphous phase (Fig. 3.7c). It is why we observe an apparent reduction of the RESET current for $\text{Ge}_{44}\text{Te}_{56}$ samples at higher pulse widths. This effect can be highlighted really well only if the crystallization speed of the material is fast enough to provide crystallization in ns range of time (as the fall time of the pulse applied).

Increasing now the voltage applied on the cell (Fig. 3.7d) we increase also the melted volume generated by the current spike. It provides residual amorphous domains that are even more distant from the plug interface, making necessary even longer pulses to recrystallize them. In Fig. 3.6 $\text{Ge}_{53}\text{Te}_{47}$ shows this effect, strongly dependent on the high growth speed of this material. This leads also to a higher randomness in the programming curve that is in agreement with the optical results reported in Fig. 3.4.

3.1.5 Simulation of the growth speed effects on the R-I characteristic

Thanks to the simulations performed, we were able to justify the changed electrical behavior of the cell, observed when the growth speed of the phase-change material is considerably high (like in the case of GeTe). In particular, we were interested in the effects of the crystallization speed, on the final programming characteristics. In Fig. 3.9 we show the results obtained for a lance-type device. The material parameters used, are the same of the GST, but we increased and decreased the growth speed, just multiplying eq. 2.31 by a constant parameter. The cell is programmed in the RESET state, before each pulse applied. We see that the minimum SET resistance achieved (we used the same pulse width of 50 ns for both the simulations), increases when we

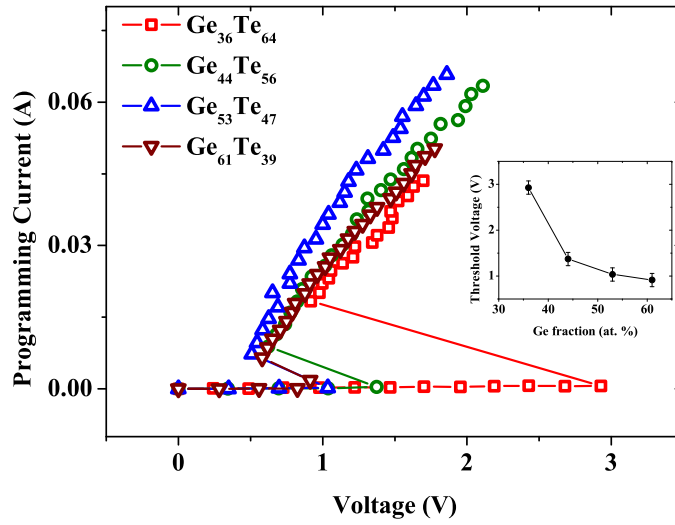


Fig. 3.10. I-V characteristics. Each point is the average value on 3 cells. In the inset is reported the trend of the threshold voltage (V_{TH}) as function of the Ge content.

decrease the growth speed, as expected. Furthermore, the RESET current is lowered by the decrease of the crystallization speed, showing that even if the current amplitude is already able to form an amorphous dome to cover the plug surface, if the growth speed is sufficiently high, during the falling edge of the pulse a partial growth of the surrounding crystalline phase can be activated, programming finally the device in a partial SET state.

3.1.6 Threshold voltage investigation

The investigation of the trend of the threshold voltage (V_{TH}) varying the Ge content was performed on the current-voltage curves (I-V) for the different stoichiometries programmed in the RESET state. The procedure applied to extract the I-V curves is the same than the one used in section 3.1.3. The SET pulse used for the I-V measurements had a width of 100 ns. In Fig. 3.10 we report the extracted cell current during the programming pulse versus the voltage drop on the cell for four stoichiometries. In the inset we report the value for V_{TH} obtained for each composition as function of the Ge at. %. If we compare the trend of V_{TH} with the trend of the activation energy reported in Fig. 3.2b, this two seem to support the relation reported in [100], in which the threshold voltage is correlated with the nucleation energy barrier ($V_{TH} \propto W_0$, as we can derive from eq. 2.18, where W_0 is the zero-field activation energy of the nucleation). At the same time in Fig. 3.1 we see a decrease of the activation energy of the conduction (E_C) of the amorphous phase, increasing the Ge content (0.50 eV in $\text{Ge}_{36}\text{Te}_{64}$ down to 0.28 eV in $\text{Ge}_{69}\text{Te}_{31}$) that is a sign of the reduction of the energy band gap. Probably both the reduction of the activation energy of the nucleation and the reduction of the energy gap of the material contribute to the decrease of the threshold voltage when we increase the Ge content in the compounds.

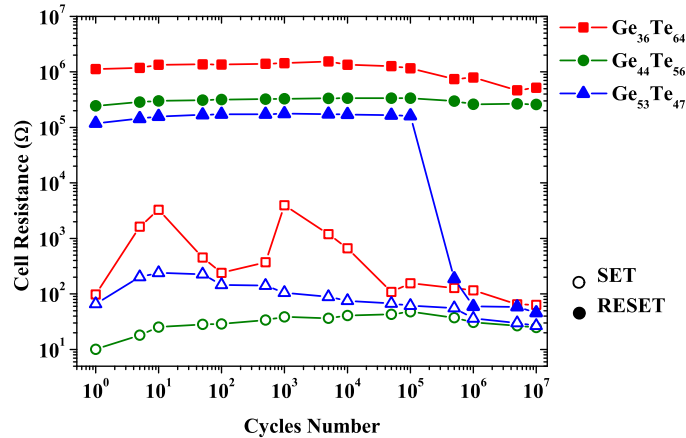


Fig. 3.11. Endurance test for $\text{Ge}_{36}\text{Te}_{64}$, $\text{Ge}_{44}\text{Te}_{56}$ and $\text{Ge}_{53}\text{Te}_{47}$ devices. The RESET pulse width is 50 ns; the SET pulse width is 500 ns.

3.1.7 Endurance

In Fig. 3.11, we report the endurance test for all Te-rich devices. We remark an excellent performance up to more than 10^7 cycles for $\text{Ge}_{44}\text{Te}_{56}$ and $\text{Ge}_{36}\text{Te}_{64}$, with no resistance window closure. On the contrary, $\text{Ge}_{53}\text{Te}_{47}$ does not reach more than 10^5 cycles. After the test, $\text{Ge}_{53}\text{Te}_{47}$ -based cells show a stuck SET state. It is comparable to the degradation due to Ge segregation similar to what showed in Fig. 3.6 for $\text{Ge}_{61}\text{Te}_{39}$. Note that the $\text{Ge}_{36}\text{Te}_{64}$ exhibits higher RESET value also after the repeated cycles, confirming its properties noticed from programming characteristics and resistivity measurements. Te enrichment in our analytical devices provides an improvement of the endurance performance. We attribute this result to the suppression of the Ge segregation. The higher is the content of germanium, the higher is the probability of the formation of stable cubic-Ge during cycling. The inclusions of cubic-Ge create conductive paths in the cell, providing a stuck SET state.

3.1.8 Resistivity drift in the RESET state

Low field resistance drift study of the RESET state was performed on 100 devices for each Te-rich stoichiometry at room temperature. An initializing procedure (10 SET-RESET cycles) was applied to the devices. Then a RESET pulse was applied in order to bring the device to the high resistance state. In Fig. 3.12 we report the value of the parameter calculated for each composition under test. We observe that in the time interval considered, the Te enrichment exhibits an increase of the drift effect on RESET state in our devices.

3.1.9 Data retention measurements

An initializing procedure (10 SET-RESET cycles) was applied to all the devices under test as described in section 2.6.5 (54 devices for each stoichiometry), and finally a RESET pulse was applied before the data-retention measurements. The stringent failure criterion considered, is the reaching of a resistance equal to half the resistance of the initial RESET state. The results are reported in Fig. 3.13. In table 3.2 we report

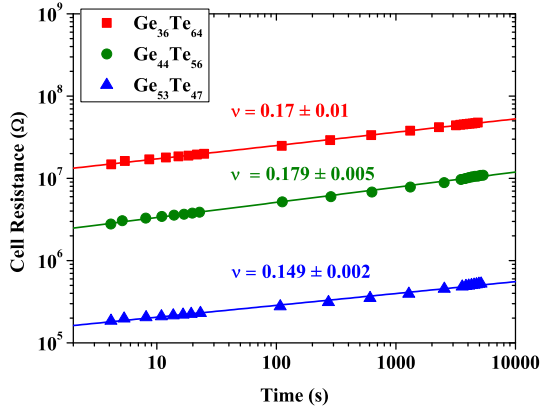


Fig. 3.12. Drift of the RESET state measured in Te-rich samples. The values are averaged on 100 cells.

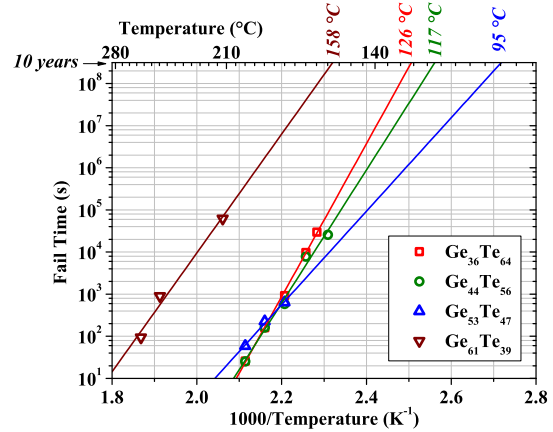


Fig. 3.13. Arrhenius extrapolation from data retention tests performed on Ge_xTe_{100-x} devices.

Device	Extracted Activation Energy	Extrapolated Fail Temperature for 10 years
Ge ₃₆ Te ₆₄	3.6 ± 0.1 eV	126 ± 1 °C
Ge ₄₄ Te ₅₆	3.1 ± 0.2 eV	117 ± 4 °C
Ge ₅₃ Te ₄₇	2.2 ± 0.2 eV	95 ± 7 °C
Ge ₆₁ Te ₃₉	2.8 ± 0.4 eV	158 ± 9 °C

Table 3.2. Results from data retention tests performed on Ge_xTe_{100-x} devices.

the results of the extracted activation energy and the extrapolated fail temperature. Ge₃₆Te₆₄ exhibits the highest activation energy, already remarked with the Kissinger analysis on blanket wafers (see Fig. 3.2b). The extrapolated temperature for reaching a ten years fail time shows the expected improvement by increasing the Te content in the chalcogenide material. Note that in this test the performances of the best performing devices, namely Ge₆₁Te₃₉, are based on devices cycled only 10 times. Indeed, as already pointed out, RESET state of Ge₆₁Te₃₉ is not stable after a higher number of cycles.

3.1.10 Conclusions

From XRD and temperature-dependent resistivity measurements on amorphous thin films we showed that Ge-rich alloys exhibit cubic-Ge elemental segregation if annealed at a temperature higher than 325 °C. Te-rich alloys on the contrary show a transition to the crystalline phase that is delayed by Te separation. This leads to an increased activation energy in Ge₃₆Te₆₄. Optical tests highlighted the strong difference in crystallization dynamics between the different stoichiometries. In particular, we pointed out the higher growth speed of Ge₅₃Te₄₇ alloy, but at the same time the higher randomness of the crystallization of this material, which is reduced both when we increase or reduce the Ge content. When integrated in memory devices, we demonstrated no substantial difference in the programming characteristics of the Ge₅₃Te₄₇ and Ge₄₄Te₅₆ devices,

while the RESET state of the latter devices appears more stable under data retention tests (a fail temperature after 10 years of 117 °C for Ge₄₄Te₅₆ while only 95 °C for the Ge₅₃Te₄₇ devices). Te enrichment provides also a gain in endurance performances, taking the devices up to 10⁷ SET/RESET cycles.

We showed that the increase of the Te at. % in GeTe-based phase-change memories can boost the thermal stability of the devices and reduce the programming power. At the same time, this increase gives rise to a strong decrease of the crystallization speed. Hence, dependently on the target application, the Te at. % can be engineered to find the needed compromise between data retention, power consuming and programming speed.

3.2 SiO₂-doped PCM

The effect of SiO₂ inclusions in Ge₂Sb₂Te₅-based PCM devices has been already reported [130], showing the possibility to reduce the thermal conductivity of the phase-change material increasing the SiO₂ content, with the consequent reduction of the programming power. We previously presented the better properties of GeTe (e.g. higher crystallization temperature and speed), with respect to standard GST, and in this light we started to analyze how the control of SiO₂ at. % in our GeTe based devices, can tune the final electrical performance (e.g. programming power reduction and threshold voltage increase). In the following, we will present also how the SiO₂ affects the final crystallization dynamics of the material, and how it can be a solution for the strong sensitivity of GeTe to low electric fields, in high temperature environments such as the automotive one (up to 150 °C).

3.2.1 Material characterization

SiO₂-doped Germanium Telluride amorphous thin films of 100 nm thickness were deposited on SiO₂(500 nm)/Si substrates by co-sputtering from stoichiometric GeTe and SiO₂ targets. The nominal SiO₂ content as referred to was varied from 0% to 10%. The 4-probes resistivity measurements shown in Fig. 3.14 and performed by annealing the samples up to 350 °C with a constant rate of 10 K/min reveal the increase of the amorphous resistivity with increasing the SiO₂ at. % as well as the increase of the crystallization temperature (187 °C for GeTe, up to 244 °C for GeTe-SiO₂10%). In table 3.3 we report also the activation energy of the conduction (E_C) for the amorphous state, that is slightly affected by SiO₂ inclusions.

The sharp drop in resistivity, once reached the crystallization temperature, suggests that all the materials, once nucleated, exhibit a very high growth speed typical of GeTe [127]. It also suggests that the activation energy, as calculated with the Kissinger method (Fig. 3.15), is in reality the activation energy of the nucleation process and it increases with the SiO₂ content, as already reported for SiO₂-doped Ge₂Sb₂Te₅ [131]. From our data, we suppose that chemical reactivity and degree of nucleation between SiO₂ inclusions and GeTe evidently bear an important role in boosting the activation energy of nucleation.

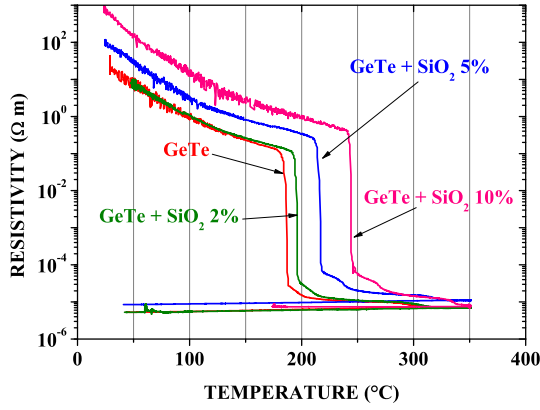


Fig. 3.14. Temperature-dependent resistivity measurements performed on 100 nm GeTe-SiO₂ thin films. The results reported are for a heating rate of 10 K/min.

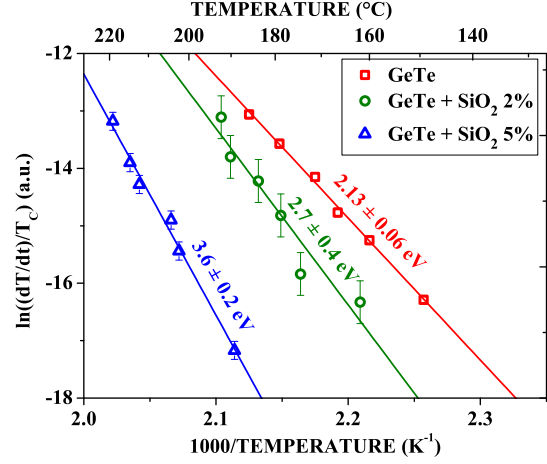


Fig. 3.15. Kissinger plots of crystallization temperature for the 100 nm thin sheet of GeTe doped with 0, 2 and 5 at. % of SiO₂. The activation energy of the crystallization, increases with the content of SiO₂.

SiO ₂	T_C	E_C
0%	186.5 ± 0.8 °C	0.417 ± 0.006 eV
2%	196.0 ± 0.9 °C	0.410 ± 0.004 eV
5%	216.6 ± 0.8 °C	0.436 ± 0.004 eV
10%	244.1 ± 0.9 °C	0.494 ± 0.003 eV

Table 3.3. Crystallization temperature (T_C) and activation energy of the conduction in the amorphous phase (E_C), extracted from the resistivity measurements of Fig. 3.14 for each at. % of SiO₂.

3.2.2 Device electrical characterization

We integrated 100 nm thick SiO₂-doped GeTe materials in lance-type PCM devices. To extract the electrical parameters at room temperature and after at high temperatures, we tested 54 devices for each composition.

From programming characteristics (Fig. 3.16) we can extract the main electrical parameters of the SiO₂-doped GeTe devices. Fig. 3.17 reveals the increase of the RESET resistance of the devices with increasing SiO₂ content, as was expected from the increase of the electrical resistivity of the amorphous phase already pointed out on full sheet films (Fig. 3.14). The programming characteristics also demonstrate the decrease of the RESET current (I_R), with a reduction reaching up to 44% for 10% SiO₂. We believe that the increase of the holding voltage V_H which we observed experimentally (table 3.4) contributes partially to the reduction of I_R needed to achieve the RESET power ($P = V_H I_R$), while the series resistive contribution (R_{ON}) has no impact. Besides this effect, our measurements also point out a reduction by 50% of the total RESET power. This reduction is more likely due to a better thermal efficiency of the cells, than to a decrease of the melting temperature of GeTe with SiO₂ inclusions. In fact, as reported in [132] we expect a decreased thermal conductivity of crystalline GeTe, as the amount of doping SiO₂ increases, that could explain the increased thermal efficiency of

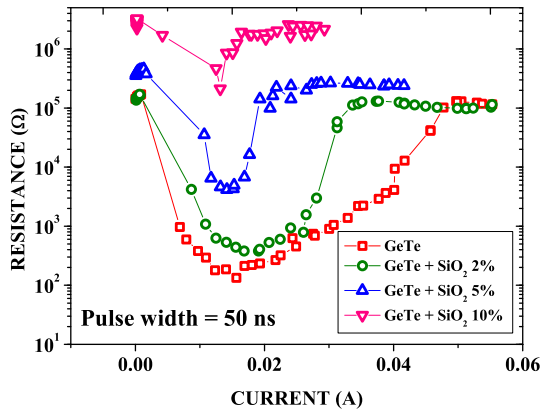


Fig. 3.16. Programming characteristics for the SiO₂ doped GeTe based devices. It is evident the increasing of the resistivity of the RESET state with the increasing of SiO₂ at. %, and the reduction of the speed of crystallization.

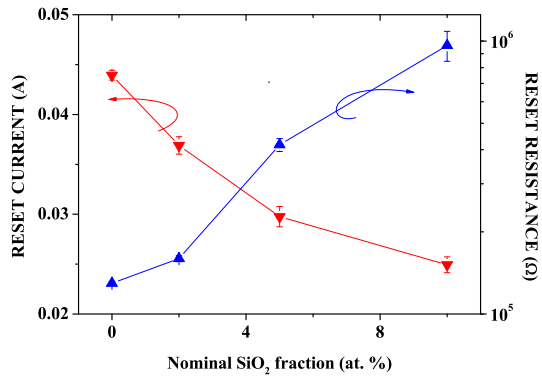


Fig. 3.17. Trend of RESET current and RESET resistance for all the at. % of SiO₂ under test.

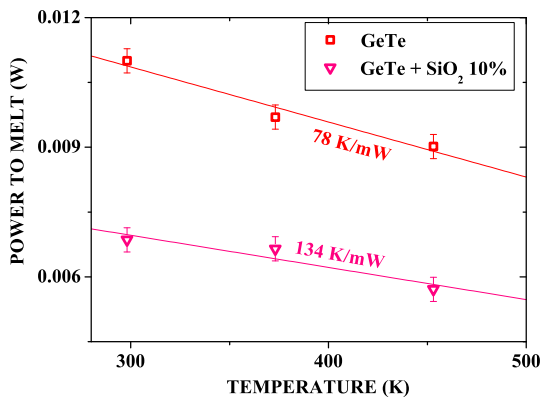


Fig. 3.18. Thermal resistance (R_{th}) extraction for GeTe and 10% SiO₂ doped GeTe devices. The SiO₂ doping increases the thermal resistance of the devices, providing a better thermal confinement.

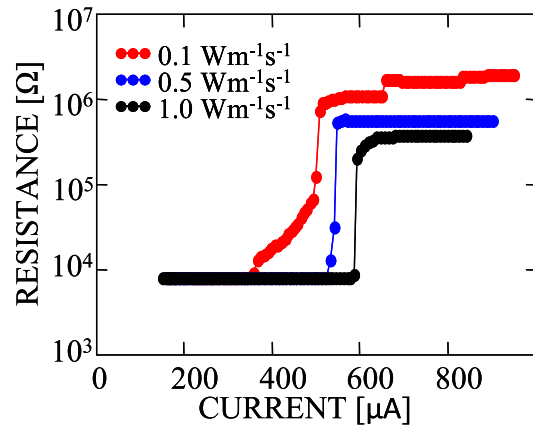


Fig. 3.19. Simulated resistance as a function of the programming current for a “Wall” structure, using different thermal conductivities for the crystalline phase of the phase-change material.

the cell environment [133]. To check this hypothesis we report in Fig. 3.18 the analysis [134] of the thermal resistance (R_{th}) of 0% and 10% doped devices, obtained from the electrical characterization of the cells at high temperatures (up to 180 °C). The power (P_m) needed to reach the melting temperature (T_m) of the phase-change material integrated in the cell, is correlated with the annealing temperature (T_a) according to eq. 2.3:

$$P_m = R_{th}^{-1}(T_m - T_a) \quad (3.1)$$

The interpolation of the data, clearly shows a 72% increase in the thermal resistance of the SiO₂10% doped cells with respect to the standard GeTe-based.

In order to demonstrate the effects of the better thermal confinement on the final RESET current of the cell we report the simulations performed considering a “Wall” structure in Fig. 3.19. Keeping constant all the simulation parameters used for standard

SiO ₂	V_H	MIN SET Time Width	MIN SET Resistance	RESET Power
0%	0.33 V	50 ns	134 Ω	22 mW
2%	0.34 V	60 ns	459 Ω	20 mW
5%	0.51 V	100 ns	795 Ω	16 mW
10%	0.65 V	500 ns	4.01 $k\Omega$	11 mW

Table 3.4. Electrical parameters: holding voltage (V_H), minimum SET pulse width (to reach the minimum SET resistance), lowest SET resistance and RESET power for the four composition under test.

GST, we rose and decreased the thermal conductivity of the crystalline phase (this value is assumed to be $0.5 \text{ Wm}^{-1}\text{s}^{-1}$ at room temperature, as reported in the literature). The better thermal confinement, reached in the cell decreasing the thermal conductivity, leads to a lower RESET current, and to the possibility to amorphize a bigger volume of phase-change material, as demonstrated by the increased RESET resistance of the device. This confirms the trend observed in Fig. 3.16 and the hypothesis of a better thermal confinement achieved in the device, once the SiO₂ at. % is increased.

In table 3.4 we show that the SET state is strongly affected by SiO₂ inclusions: the crystallization becomes slower, as already demonstrated for Ge₂Sb₂Te₅-based materials [135] (longer SET pulses are required), and the lowest SET resistance we can achieve, on average increases, probably due to the reduced crystal grain size [131]. However, since both the SET and RESET resistances increase, it allows to preserve a SET/RESET resistance window of about three orders of magnitude.

3.2.3 Drift of the RESET state characterization

To evaluate the impact of SiO₂ inclusions on the drift in time (t) of the resistance (R) of both the RESET and the SET state, we calculated the drift coefficient ν for each SiO₂ at. %, according to the empirical law (eq. 2.25):

$$R \propto t^\nu \quad (3.2)$$

The results of the interpolation are reported in Fig. 3.20.

The increased disorder produced in the material by SiO₂ inclusions, results in a slightly boosted drift of RESET state in 5% and 10% devices, while we observe an inversion of trend in the SET state of the 10% content. In Fig. 3.21 we report a TEM image of a GeTe-SiO₂5% cell in the SET state (obtained with a pulse of 100 ns) where residual amorphous regions are evidenced. These regions could explain the residual drift of the SET state. At the same time, from the EELS profile performed on the same sample, we don't have signs of SiO₂ aggregation or displacement along the material thickness (the cell was previously cycled 10^3 times).

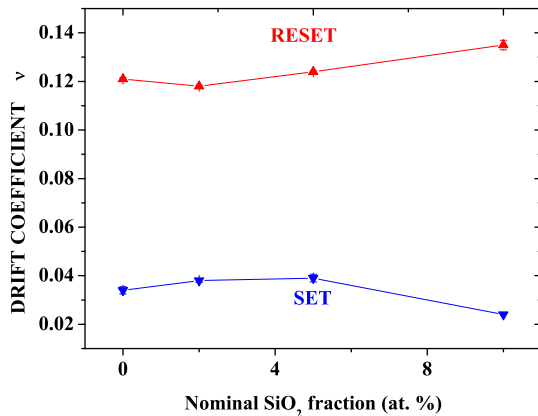


Fig. 3.20. Drift coefficient calculated for RE-SET and SET states, as function of the amount of SiO₂. Increasing the SiO₂ content, we observe a tendency towards an increase of the drift.

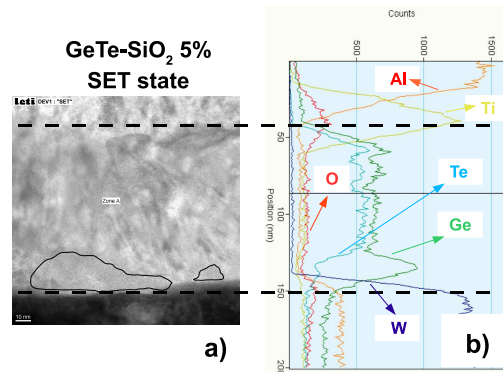


Fig. 3.21. a) TEM image of a 5% SiO₂ doped cell in the SET state. The residual amorphous regions affect the drift of the cell. b) EELS profile along the phase-change material thickness over the plug. We do not have signs of SiO₂ aggregation or displacement.

3.2.4 Retention properties

In Fig. 3.22 we report some indicative data retention measurements performed on our cells. Despite the increased activation energy observed in Kissinger analysis performed on SiO₂-doped GeTe full sheet materials, as expected, we do not see a strong improvement of the RESET state stability in temperature, being the extrapolated failure temperature for 10 years-retention in the same range of standard GeTe (95 °C [136]). In fact, the growth dominated nature of the materials under test, makes the crystalline phase surrounding the amorphized active region detrimental. Even if the activation energy of the nucleation is increased by the dielectric inclusions, as already showed, the growth speed is slightly affected, and then the crystalline phase, once reached the favorable temperature, grows in the same way both in SiO₂-doped and not doped cells.

3.2.5 Threshold voltage

The decrease of the threshold voltage V_{TH} with the temperature, as expected from eq. 2.24, results in an increased sensitivity to reading voltages at high operating temperatures [129]. This problem of PCM technology, could make useless all the efforts made to increase the thermal stability of the phase-change material chosen for the target application. We report in Fig. 3.23 the variation of V_{TH} as function of the SiO₂ doping content and temperature. As a result, GeTe appears not to be able to sustain a 1 V reading voltage above 60 °C while standard commercial operating temperatures range up to 70 °C. On the other hand, thanks to the increase of V_{TH} with the SiO₂ content, we show that GeTe-SiO₂10% RESET state is capable of a 1 V reading voltage up to 120 °C. The change in nucleation dynamics obtained by the inclusion of SiO₂ in the material, reveals in these results, its contribution in the increase of the threshold voltage [137]. This hypothesis seems more convincing than the possibility of a change of the conduction mechanism due to SiO₂ inclusions. In fact we found that, despite the increased resistivity, SiO₂ doesn't affect the conduction mechanism in the subthreshold

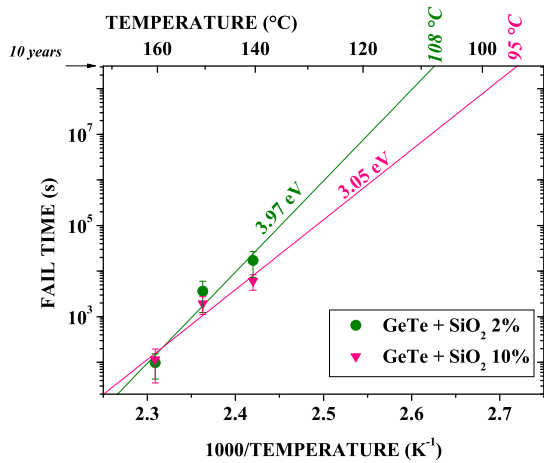


Fig. 3.22. Data retention test for 2% and 10% SiO₂ concentration. We do not see a strong improvement of the RESET state stability in temperature, being the extrapolated failure temperature for 10 years-retention in the same range of standard GeTe (95 °C [136]).

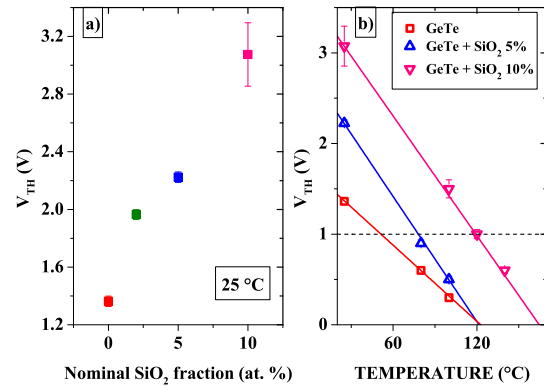


Fig. 3.23. a) Threshold voltage as function of the SiO₂ content at room temperature. b) Behavior of the threshold voltage in temperature, for different at. % of SiO₂. The doping increases the immunity of the RESET state to standard reading voltages at higher operating temperatures.

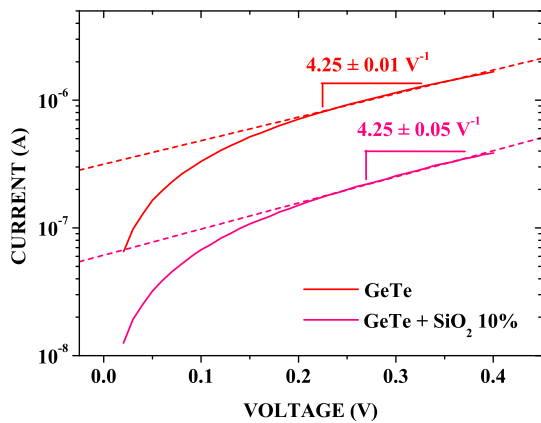


Fig. 3.24. I-V characteristics at room temperature for GeTe and GeTe-SiO₂ 10% devices. The two subthreshold slopes have a confidence level of 100%, calculated on a population of 100 cells for each composition.

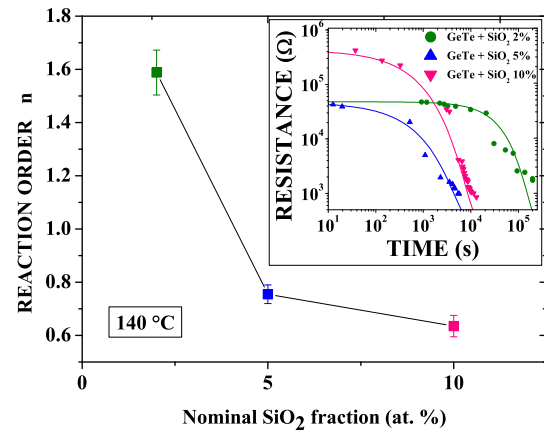


Fig. 3.25. Interpolation of the curves obtained from recrystallization of the devices at 140 °C (inset): it allows to calculate the reaction order n , here as function of the SiO₂ content. The decreasing of n as the SiO₂ content increases, is the evidence of a crystallization process affected by the dopant inclusions.

voltage region, the subthreshold slope being unchanged. In Fig. 3.24 we report the I-V characteristics at room temperature for GeTe and GeTe-SiO₂ 10% samples.

3.2.6 Avrami analysis

To confirm the hypothesis of the influence of a changed dynamics of the nucleation we show in Fig. 3.25 the result of the interpolation by an Avrami equation (eq. 1.9) of the recrystallization curves for three different at. % of SiO₂-doping at 140 °C. We suppose

in fact, a time dependency of the RESET resistance (R_{RESET}), dominated by the parameters K and n , correlated with the crystallization dynamics of the phase-change material, according to:

$$R_{RESET} \propto e^{-K t^n} \quad (3.3)$$

The increasing of SiO₂ in the material, lowers the parameter n that can be correlated with the reaction order of the crystallization process. The transition to a diffusion controlled growth rate and the reduction of the nucleation rate can be concurrent and provide the lowering of n , confirming the proposed hypothesis of a changed crystallization dynamics [138].

3.2.7 Summary of SiO₂ inclusions effects

We demonstrated how the increase of the threshold voltage with the SiO₂ content opens the possibility to engineer V_{TH} for high-operating-temperature applications. This property was correlated with the increase of the activation energy of the crystallization process and the changed crystallization dynamics. Moreover, we highlighted the significant reduction of programming power (by 50%), following the introduction of SiO₂ into GeTe, which enables addressing low-power applications.

3.3 Carbon-doping in Ge₂Sb₂Te₅-based PCM

As already pointed out before, one of the key bottlenecks of PCM technology is the power consumption during the programming operations. The C-doping, once introduced as dopant in GST based analytical devices, showed a strong decrease of the RESET current up to 30% of reduction ([139]). But the introduction of C, showed also a gradual detrimental effect on the resistance window of the cell. We analyzed then the behavior of GST-C based material, once integrated in state-of-the-art “Wall” structures, in particular focusing on the data retention and the speed of the devices.

We integrated our materials in our devices at room temperature by plasma-assisted co-sputtering from one target of pure GST and one target of pure carbon, to finally obtain three different compositions: GST, GST-C5% and GST-C10%. As already reported in the literature, C doping in phase-change materials strongly increases the crystallization temperature. Therefore, at the end of the fabrication, we applied an annealing process of 2 minutes at 450 °C on all the wafers under test, to achieve a full recrystallization of the devices, before to start the electrical characterization.

A first screening of the speed properties of our devices led us to the conclusion that C-doping is detrimental for the device speed. In Fig. 3.26 we show as an example, the RESET-SET characteristic for the GST-C10%. Standard 300 ns pulses normally sufficient to perfectly SET the GST based cells, are only slightly decreasing the resistance of the cell. We have to increase the SET time up to 10 μs to achieve a resistance window of one order of magnitude. The benefits of C-doping on the final programming current are reported in Fig. 3.27, confirming what already reported in the literature in analytical cell. We obtain an important programming RESET current reduction by almost 50%, achieving results comparable with more highly scaled PCM devices.

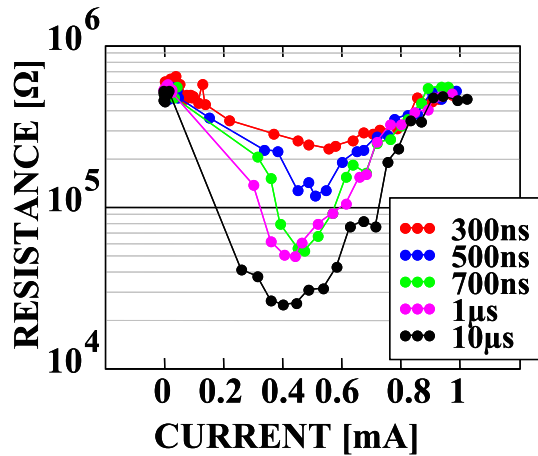


Fig. 3.26. RESET-SET characteristics for GST-C10% devices. Once integrated C-doped materials in shrunk devices, we don't observe a gain in speed during the SET operation, being the SET time in the order of tens of μ s to achieve a reasonable resistance window.

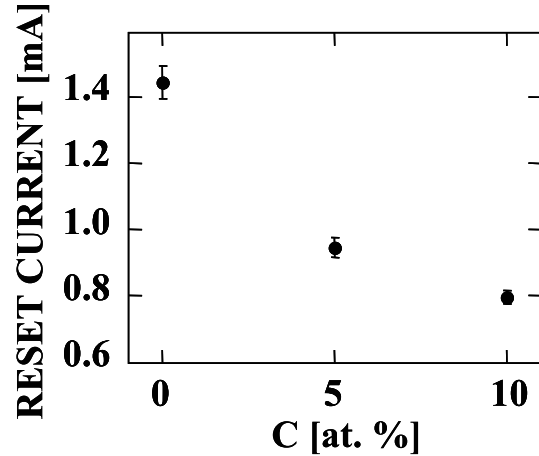


Fig. 3.27. Trend of the RESET current in GST-C devices. The higher is the C at. %, the lower is the programming current.

Concerning the data retention performances, C-doping seems to do not improve significantly the performance of the GST. The best result we obtained worthy of quotation, is the retention of 1 hour at 180 °C of GST-10%, that standard GST and GST-5% are not able to sustain.

As already showed in recent publications [140], carbon in the phase-change material layer has the tendency to form strong C-C chains, that have the effect to reduce the crystalline GST grain size, lowering at the same time the speed of the crystallization process, the expulsion of carbon from the material, being an energy expensive process.

3.4 Ge enriched phase-change materials

In recent years, IBM and Macronix showed the benefit of the engineering of the GST stoichiometry on the final data retention and RESET current of the devices [141]. In their study they showed how the increase of Ge in the final alloy, can boost the crystallization temperature of the material, at the expense of a reduction of the programming SET speed. The phenomenon of the drift of the RESET phase has been analyzed [59] in Ge-rich GST. One hypothesis is that the multiple coordination of Ge atoms in the matrix (tetrahedral bonds of 90°, and octahedral bonds of 110°), can create a new energy gap state, increasing the structural relaxation process. It is shown in fact, that mobile atoms lead to very small change in gap states while a finite atomic rearrangement of a local structure results in a bigger change and hence becomes the dominating factor for drift. This is the case of Ge-rich samples, where the higher is the number of possible gap states, the higher is the drift (structural relaxation).

We started to analyze the behavior of Ge-rich GST based materials, once integrated in shrunk “Wall” structures, being interested also in the effects of N and C doping on the final performances of the devices. We characterized the cells, but we started to observe a strong drift also of the SET state, even in samples programmed with really

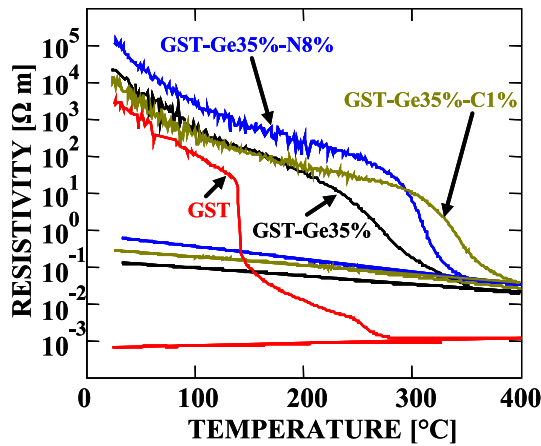


Fig. 3.28. Resistivity vs Temperature for materials under test.

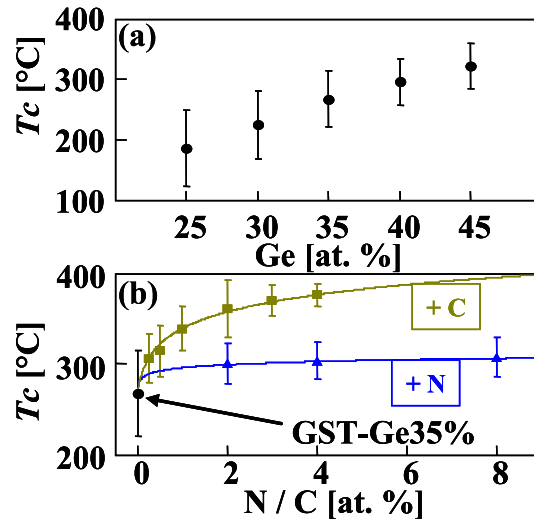


Fig. 3.29. Crystallization temperature (T_C) for different materials under test. T_C increases almost linearly with Ge content (a). It already saturates at 2 at. % of N content in N-doped samples, while C-doping boosts T_C up to roughly 400 °C (b).

long pulse-sequences (in the order of tens of μs). In an industrial memory device, the drift of the RESET state is not detrimental, since it enlarges the resistance window. On the contrary, a drift of the SET state towards higher resistance values, can be detrimental, decreasing the resistance window of the cell, and finally degenerating the information stored in the device. The drift of the SET state has never been analyzed and highlighted before in the literature. In this light, we report in the following sections a detailed characterization of N- or C-doped and undoped Ge-rich GST based materials, integrated in industrial state-of-the-art PCM devices, focusing on the phenomenon and on the effects of the drift of the SET state.

3.4.1 Material characterization

We investigated Ge-enriched GST alloys (with Ge at. % ranging from 25% up to 45%) undoped, C- or N-doped, deposited by co-sputtering and reactive sputtering. Resistivity measurements as a function of temperature (Fig. 3.28) show the benefits of Ge-enrichment on thermal stability of the as-deposited (as-dep) amorphous phase, demonstrating a gradual increase of the crystallization temperature of the samples (T_C) up to 322 °C in GST-Ge45% (Fig. 3.29a). N-doping in GST-Ge35% samples shows no increase of T_C at N at. % higher than 2%, whereas C-doping up to 4% raises T_C up to roughly 400 °C (Fig. 3.29b).

The increase of Ge content in the layer, delays the first phase transition (in the case of Ge35% till 250 °C), the cubic-Ge phase separation being fundamental for the starting of the contemporary formation of the cubic-GST phase. The higher the content of Ge, then, the higher the energy to provide to the system to initiate the crystallization process. To be noted, now, is the totally different dynamics of the transition to the crystalline phase between N- and C-doped samples. The C-doped sample preserves

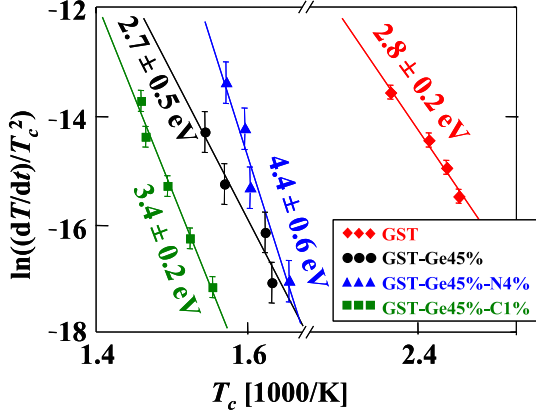


Fig. 3.30. Kissinger plots of crystallization temperature obtained with blanket layers. The N-doping reveals an increase by almost 60% of the crystallization activation energy.

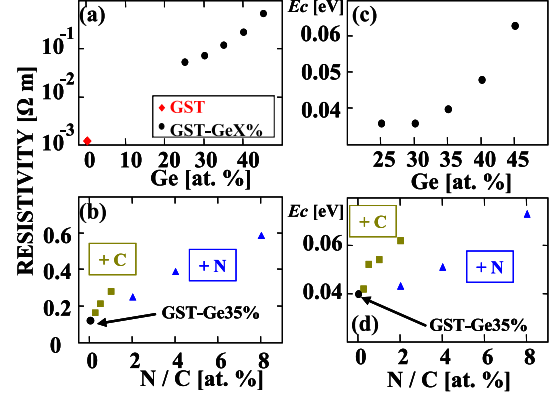


Fig. 3.31. Resistivity of the crystalline phase (at 25 °C) of all material samples crystallized by means of a temperature ramp up/down procedure (rate of 10 °C/min) and up to 400 °C (= max BEOL temperature) (a,b). On the right (c,d) the activation energy of the electrical conduction (E_C) of the crystalline phase.

at 330 °C the slope of the resistivity vs temperature observed for the undoped sample (GST-Ge35%), highlighting how the presence of C inclusions, just delays the formation of cubic-Ge. On the contrary, in N-samples, the formation of Ge-N bonds retards the Ge segregation, and once completed, the temperature is already sufficiently high to provide the steep appearing of cubic-GST thanks to the reduced Ge in the layer. Also Kissinger plot analysis (Fig. 3.30) reveals different crystallization dynamics between N- and C-doped alloys. N-doping results in the higher increase (by more than 60%) of the activation energy of crystallization with respect to the undoped sample.

The final resistivity of the full sheet samples evaluated at 25 °C (Fig. 3.31a-b) shows an exponential dependence on Ge at. %, which is dominant with respect to the slight linear increase due to N and C doping. It comes from the slight percentage of dopant with respect to the Ge amount. In Fig. 3.31c-d we report the activation energy of the conduction (E_C), calculated at room temperature according to the law $\rho = \rho_0 \exp(\frac{E_C}{k_B T})$ (eq. 1.11) for all the samples annealed up to 400 °C. E_C , calculated after the same kind of annealing performed on all the samples, is not representative of the conduction in the SET state of the final device. It gives an idea of how the conduction is affected by Ge content (and dopants) in an intermediate crystalline phase. We confirm that the higher is the Ge at. %, the higher is the disorder in the system and the higher is the energy needed to take the material to a stable crystalline phase (after all the phase separations that we have already described).

XRD measurements (Fig. 3.32) highlight the segregation of cubic-Ge at 400 °C in all the samples tested. The segregation is an energetically expensive process, hence we can explain the boost of the thermal stability of the amorphous samples observed when increasing Ge at. %. While the concentration of segregated cubic-Ge increases with Ge at. % (Fig. 3.33), it appears to be considerably reduced in GST-Ge45%-N4%, probably due to the formation of strong Ge-N bonds in the crystalline matrix [142] as already pointed out previously in the description of the crystallization dynamics.

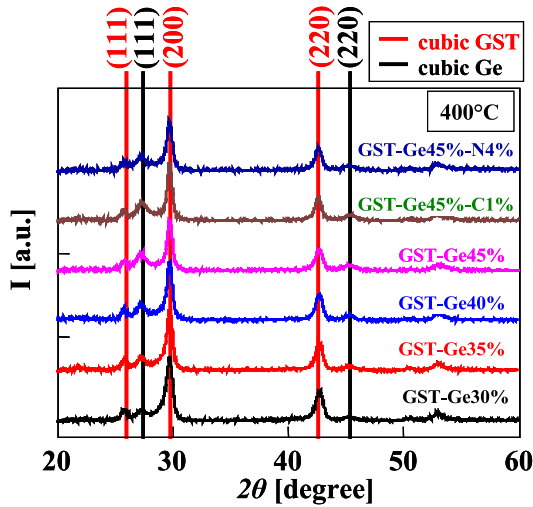


Fig. 3.32. XRD performed on samples after 400 °C annealing. There is evidence for the segregation of cubic-Ge.

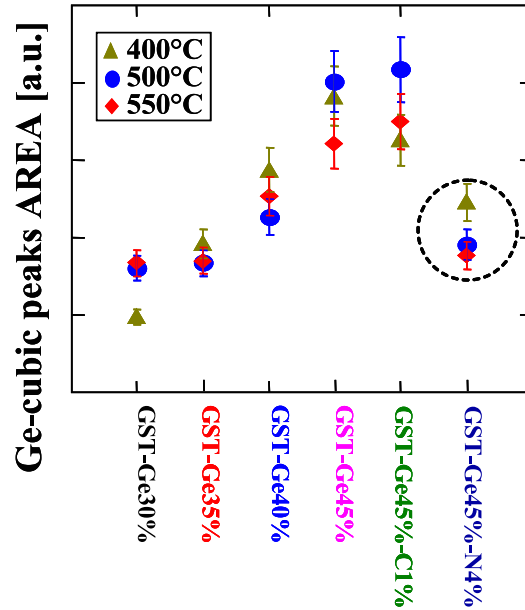


Fig. 3.33. Area of cubic-Ge XRD peaks, indicative of phase concentration. The significant reduction highlighted in GST-Ge45%-N4% is due to the formation of strong Ge-N bonds.

3.4.2 Device performance

We integrated the doped Ge-enriched GST materials in state-of-the-art PCM devices [93] to test the performance. The structure of our cells is the “Wall” structure, designed specifically to perform our analytical studies on the behavior of different materials. The wall thickness is 5 nm while the wall width varies (dependently on the device considered) from a minimum of 60 nm up to 240 nm. The plug is based on a particular titanium nitride alloy, designed to provide the maximum temperature peak at the plug-phase-change material interface. The BEOL temperature is 400 °C, at which temperature all the wafers are annealed at the end of the industrial process flow for 2 minutes. It means that the phase-change materials under test, as already pointed out in the material characterization, are not fully recrystallized at this temperature. In order to prepare the devices for the electrical characterization we performed a “pre-seasoning”. In this case it was made of 5 sequences of staircase-up (SCU) and staircase-down (SCD) pulses, each one (both the SCU and the SCD) composed by a series of 50 pulses of increasing (or decreasing) voltage. The pulse width used was 300 ns, with 5 ns rise and fall time.

The SET-RESET characteristics in Fig. 3.34 reveal that, by increasing the Ge at. %, we obtain a decrease in the RESET current (up to 33% of reduction) and an increase in the SET resistance (as already pointed out in Fig. 3.31a). We also observe a gradual softening of the slope of the SET-RESET curve. We think that this effect is probably correlated with two phenomena: the first is the changed thermal conductivity of Ge-rich materials with respect to GST. In fact, the presence of different phases in the material crystalline matrix, rises the number of boundaries in the system, inevitably increasing the final thermal conductivity of the material. It enables the starting of the amorphisation of the phase-change material at lower currents (lower temperatures), thanks to

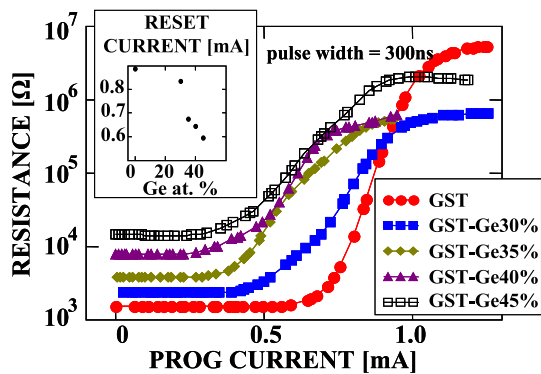


Fig. 3.34. SET-to-RESET device characteristics. The resistance of the SET state increases with Ge content. Ge-doping reduces the RESET current up to 33% (inset).

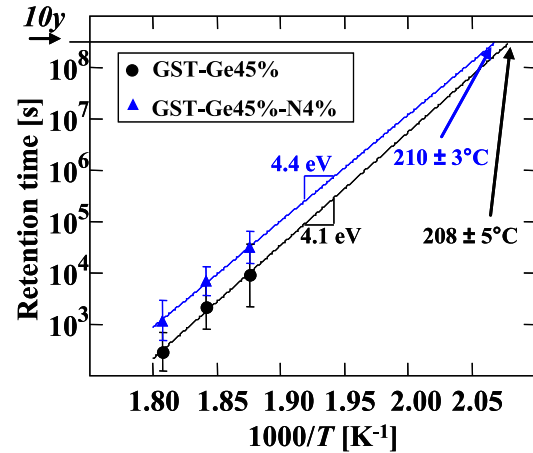


Fig. 3.35. Arrhenius plot of data retention time for GST-Ge45% with and without N-doping.

the increased thermal efficiency of the cell. The second phenomenon involved is the recrystallization speed (analyzed in detail later). Even if the pulse amplitude is already enough to provide the melting of a part of the phase-change material, if the material has a crystallization speed high enough (like the GST in this case), during the fall time of the pulse we can partially recrystallize the melted volume. If it happens, only when the melted volume is sufficiently extended, we can start to leave a fully amorphized area close to the plug interface at the end of the pulse, and then achieve a considerable increase of the resistance of the cell. The higher is the recrystallization speed, the sharper will be the transition SET-RESET in our test procedure.

The improvement of the data retention of the devices thanks to Ge-enrichment was tested through the monitoring of the failure of the RESET state in time on a population of 20 devices, during a constant temperature annealing provided with the thermal chuck. The criterion considered for the failure is the reaching of a resistance value equal to half the resistance of the initial RESET state. Fig. 3.35 shows that GST-Ge45% and GST-Ge45%-N4% allow for a retention time of 10 years at 210 °C and 208 °C respectively. These results are among the best reported in the literature [135].

Isochronal Annealing Steps Procedure (IASP) at successively higher temperatures (from 220 °C up to 280 °C) was applied through a specific baking oven, to evaluate the retention of both the HRS (high-resistance state) and LRS (low-resistance state) of the devices under test (DUTs) (Fig. 3.36). Ge enrichment increases the stability of the HRS, showing a drift of the resistance up to 220 °C and then, a gradual recrystallization in all the samples. As expected from resistivity measurements, the best stability is observed in high Ge content, even improved in N4% DUTs. The C-doping decreases the RESET resistance and then the final programming window. At the same time we observe its detrimental effect also on the LRS of the GST-Ge45%-C1% samples: the drift of the SET state in this devices continues up to 260 °C, reducing the total resistance window down to less of one order of magnitude. We can notice how IASP allows highlighting the LRS loss of stability at high temperature.

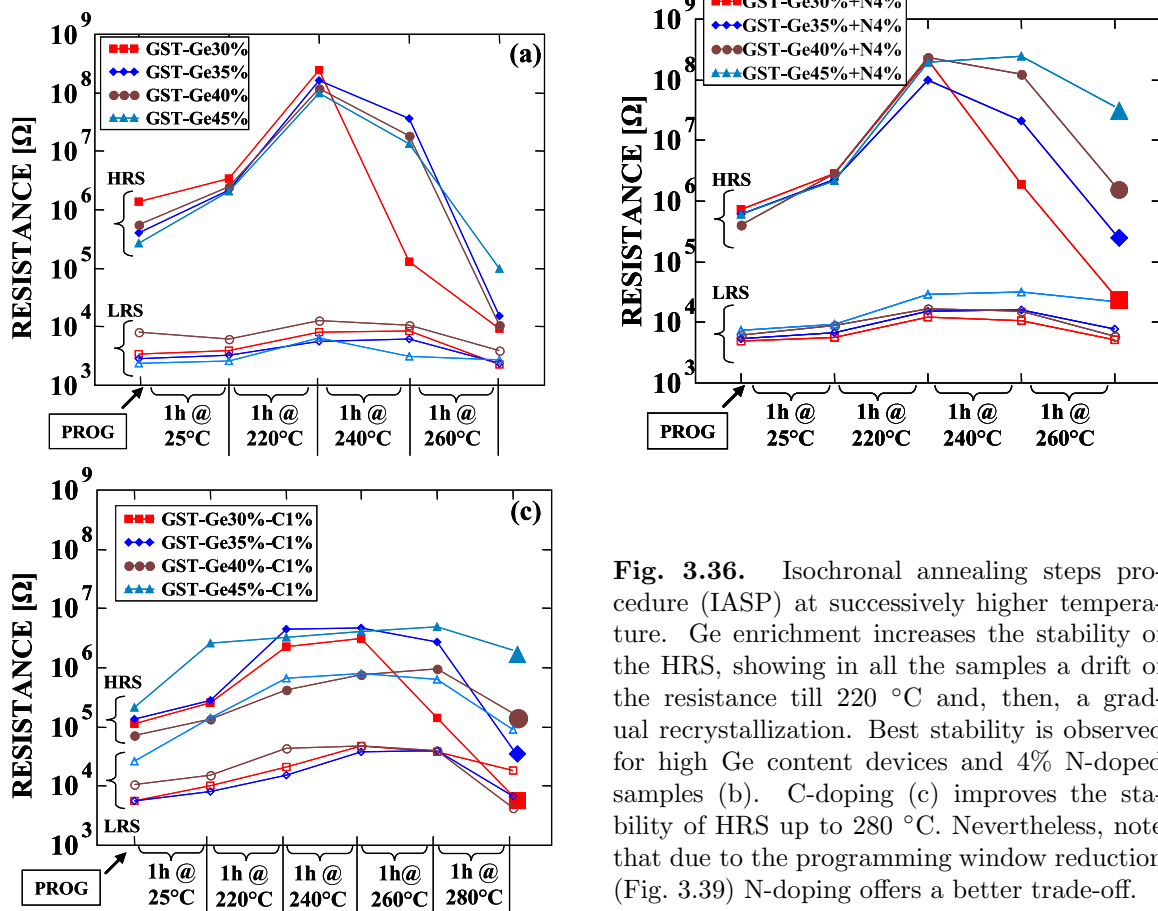


Fig. 3.36. Isochronal annealing steps procedure (IASP) at successively higher temperature. Ge enrichment increases the stability of the HRS, showing in all the samples a drift of the resistance till 220 °C and, then, a gradual recrystallization. Best stability is observed for high Ge content devices and 4% N-doped samples (b). C-doping (c) improves the stability of HRS up to 280 °C. Nevertheless, note that due to the programming window reduction (Fig. 3.39) N-doping offers a better trade-off.

3.4.3 SET performance

As already proved for GST [104], also in Ge-rich GST devices we observe a strong reduction of the drift coefficient ν (calculated according to eq. 2.25) when we decrease the resistance of the cell (Fig. 3.37). This leads us to correlate the drift of the SET state to the residual amorphous regions (in particular amorphous Ge) not involved in the recrystallization process during the application of the pulse sequence. What was unexpected, is the total independence of the drift of our Ge-rich samples on the electric field applied during the drift test (like in $\text{Ge}_2\text{Sb}_2\text{Te}_5$ [143]). In Fig. 3.37 in fact, are reported the results obtained at high and low stress voltage, that seem apparently in contradiction with what already published in [97]. It has been observed in GST-based devices, that during the pulse application, the polarity of the pulse can affect the final displacement of the atomic species present in the material layer. The effect starts to be evident after some cycling of the cells, and it is due to the different electronegativity of Ge and Sb atoms with respect to Te. The increase of Ge at. % in the material, doesn't impact the dependency of the structure relaxation on the electric field, probably because a considerable atomic diffusivity is possible only when the material is partially melted, not possible at still too low stress voltages used in our test. However, if the melting is reached, the programmed resistance state would be lost.

To study the drift of the SET state in our different materials under test, we programmed all the devices in the SET state with a time-consuming SCD procedure of 50

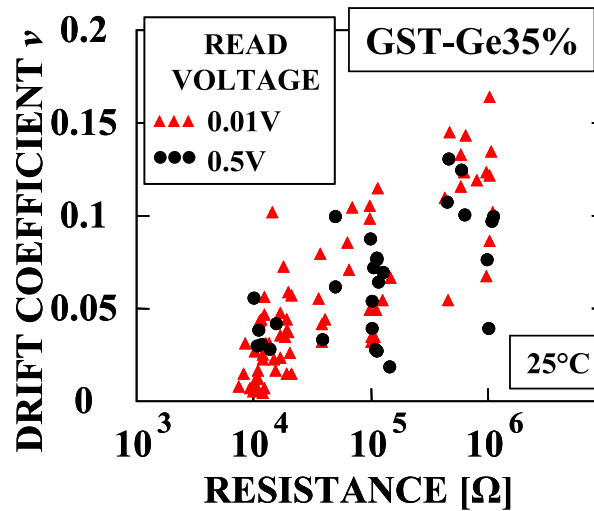


Fig. 3.37. Drift coefficient as a function of cell resistance (at 25 °C) in GST-Ge35%. The drift depends on the device resistance, but not on the reading voltage.

pulses ($> 15 \mu\text{s}$) to achieve the lowest SET resistance possible (also called “SET-MIN”). Then we started the annealing at 150 °C, with log-time-spaced intermediate readings at room temperature. Fig. 3.38 shows the value of ν at 150 °C for the LRS of doped and undoped devices. We observe the increase of ν with increasing Ge at. % (similarly as for the HRS [59]). On the contrary, even if C-doping produces a larger dispersion, the general effect of dopants is the softening of the drift. This is evident in particular in N-doped DUTs. We think it may be correlated with the decreased residual Ge amorphous phase, neutralized by the formation of stable Ge-N bonds, as shown in Fig. 3.33. However, to achieve this good result in terms of SET drift, programming time has to be

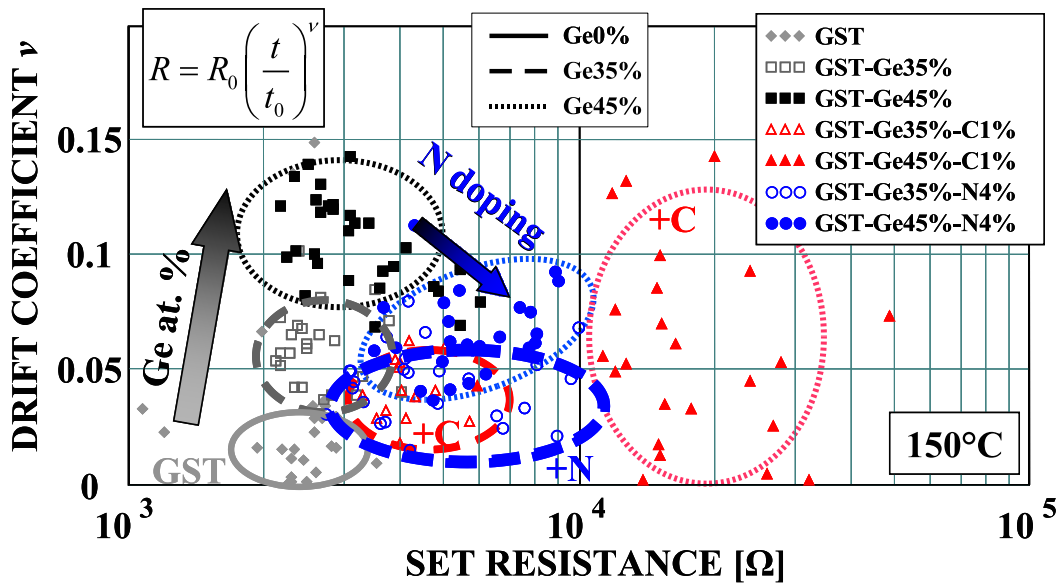


Fig. 3.38. Drift coefficient for the LRS at 150 °C measured for different materials under test (reading temperature = 25 °C). The cells were programmed with a staircase-down (SCD) time-consuming programming procedure of 50 pulses (pulse time width = 300 ns) to achieve the lowest possible resistance state.

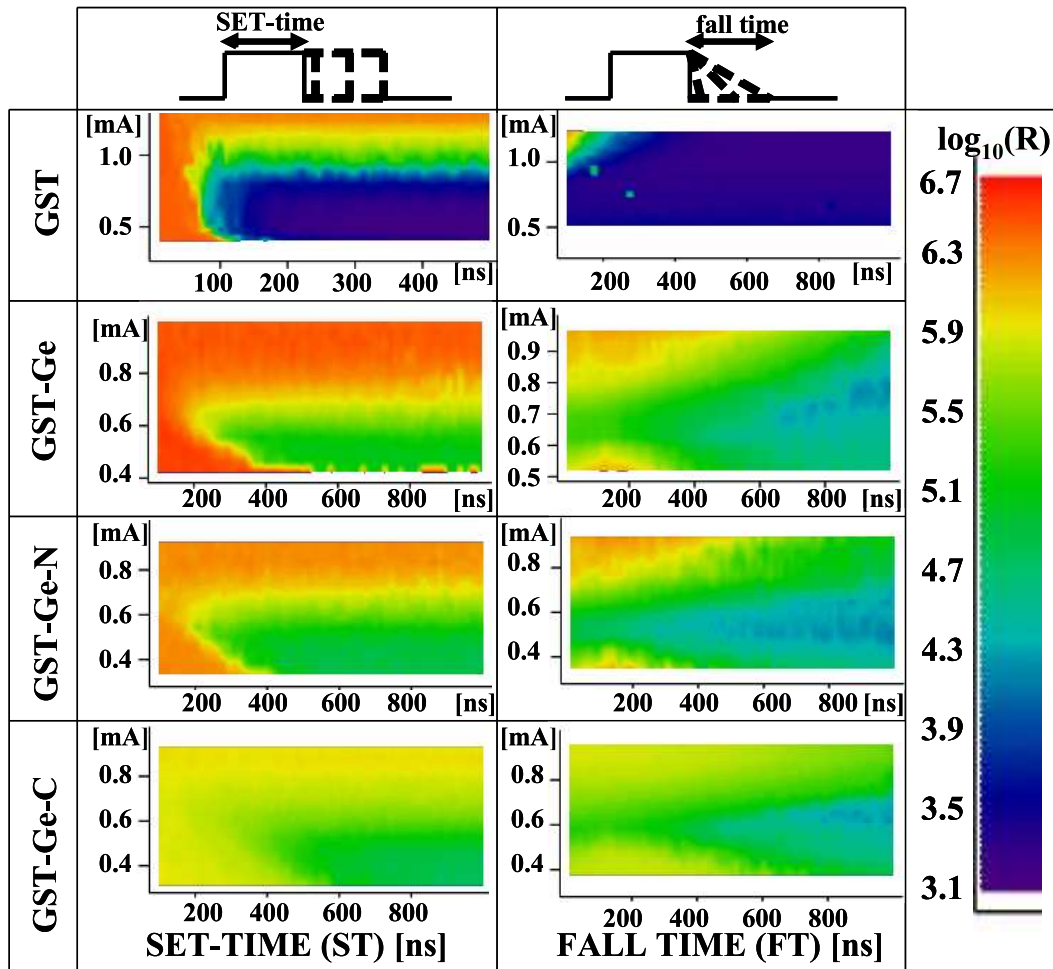


Fig. 3.39. Cartographies of SET operation for all the materials under test. The increase of both the ST and the FT of the programming pulse applied to the cell (pre-programmed in the HRS) is investigated. Long ST is not sufficient to achieve complete recrystallization: only the control of the FT enables the full SET. C-doping drastically reduces the crystallization speed, but it is also detrimental for the programming window.

reduced in order to address final applications. Our main goal was then to understand if it is possible to achieve such a low SET state, with a specific programming procedure, reducing the programming time.

We started to analyze in details the crystallization speed of our different materials. To achieve a very deep comprehension of this aspect, we used a new electric procedure similar to what done for optical cartographies (Fig. 3.4) on blanket layers. It consists in programming a device in the RESET state, and then applying a SET pulse with different current amplitude and different duration. After each sequence of RESET-&-SET, the final resistance of the device is acquired and stored. The result is a full cartography of the SET operation, the more detailed, the finer is the SET current and time step used. In our case, we considered 2000 different SET current/time steps, and for each point on the cartography we plotted the mean value of the results obtained on 3 devices.

Fig. 3.39 shows the cartographies of the SET operation for some of the different DUTs. The impact of both the SET-time (ST) and the fall time (FT) of the SET

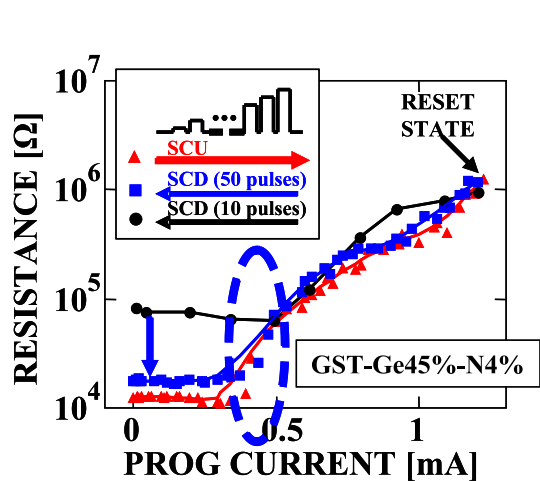


Fig. 3.40. SET resistance as a function of the programming current, for different SCD procedures.

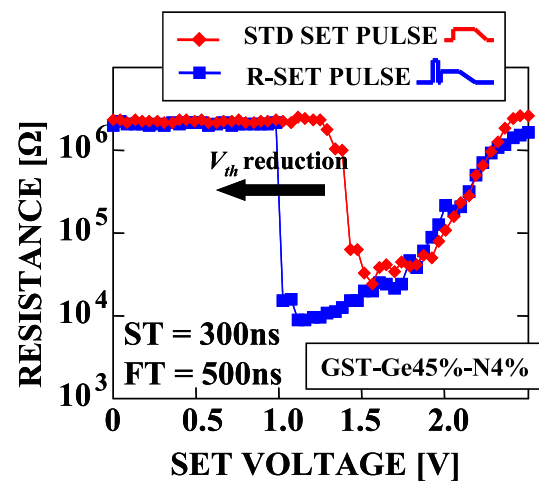


Fig. 3.41. Comparison of programming characteristics of Ge-rich samples, obtained with STD SET and R-SET pulses.

pulse on the final resistance state of the device was investigated. The reduction of the crystallization speed in Ge-rich samples (with respect to GST) and, at the same time, the inefficiency of the increasing of the time width to achieve lower resistance states are evident from the graphs. C, with respect to N doping, reduces even more the crystallization speed of the devices, being detrimental also for the programming window.

The “funnel-like” shape of the crystalline regions in the right column of Fig. 3.39 proves that LRS can be achieved with a one-pulse procedure at a specific programming current, a controlled ST, and a fall time on the order of 100 ns. The need of the combination of specific pulse conditions to achieve a “good” SET state, can be also demonstrated by means of a multi-pulse programming procedure in the case of GST-Ge45%-N4% (Fig. 3.40). Two different staircase-down (SCD) sequences (the first including 50 pulses and the second 10) bring the cell to two totally different final programmed states. The first SCD procedure leads to a current favorable for recrystallization and, then gradually lower current amplitudes are scanned with fine resolution. The second SCD leads to the same favorable current level, but the following pulses are at lower current levels, yielding a SET resistance higher (i.e. worse crystallization), than the one obtained with the previous procedure.

To obtain a good current control in our 1R PCM test structure, we engineered a combination of RESET and SET pulses (R-SET), by taking advantage of the threshold-voltage lowering achieved after the RESET operation as describe in section 1.7.4.1. In this way, the cell can switch at a lower voltage during the ST of the pulse, reaching a current value able to trigger the optimized crystallization process. Fig. 3.41 shows the effect of this procedure on the programming characteristics of the cell. A standard SET pulse, in which we tune just the ST and the FT, is not able to perfectly SET the cell. In fact once reached the threshold voltage, the programming current is already too high with respect to the one needed for an optimized crystallization. An R-SET pulse with the same ST (and FT), gives rise to a specific “programming-current-vs-time-profile” in the material, thus lowering the final programmed SET resistance. In order to integrate

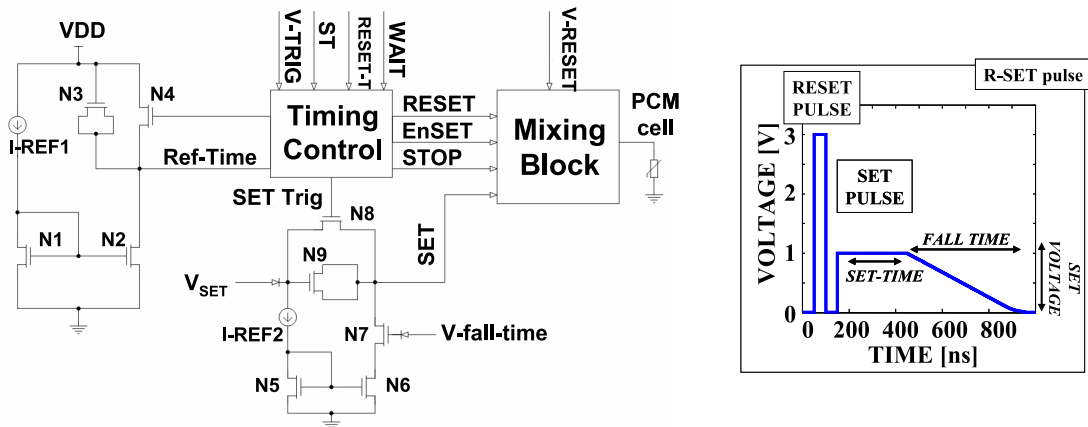


Fig. 3.42. Circuit implementation to provide the R-SET pulse to the PCM cell. The circuit output waveforms in the inset (right) show the possibility to externally tune all pulse parameters.

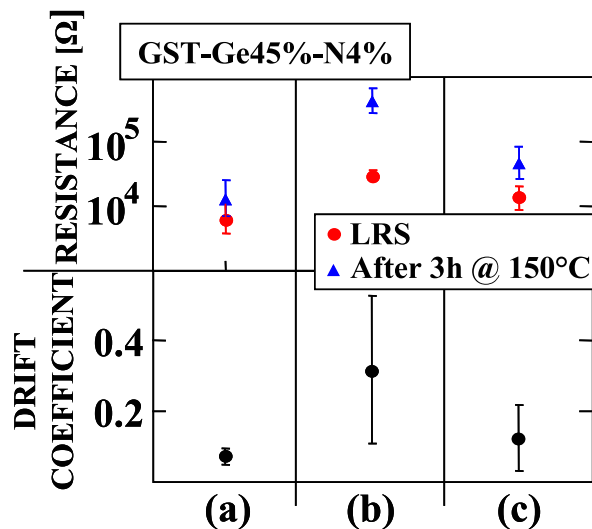


Fig. 3.43. Comparison of the drift of the LRS obtained with three different programming techniques. In (a), the cell is SET with a time-consuming SCD (SET-SCD) of 50 pulses ($> 15 \mu\text{s}$), which ensures a low drift. In (b), a standard SET pulse achieved with $\text{FT} = 1 \mu\text{s}$ ($\text{ST} = 300 \text{ ns}$), gives worse performance with respect to the results obtained with an R-SET pulse (c) with $\text{ST} + \text{FT} = 800 \text{ ns}$.

this idea in a final memory product we also proposed a possible implementation of the circuit needed to provide on the cell a proper R-SET pulse. The description of the R-SET pulse generator is shown in Fig. 3.42. We designed the generator with a full-control capability of pulse parameters, to be suitable for all the materials under test. Once verified our programming procedure in order to obtain a valid SET state of the cell, we started to compare different programming procedures in terms of final drift of the LRS. The benefits of the R-SET procedure are shown in Fig. 3.43 where different programming procedures are compared in terms of final ν measured at $150 \text{ }^\circ\text{C}$. The reduction of the drift obtained with the R-SET strategy (Fig. 3.43c) closely approaches the result obtained with time-consuming SCD (SET-SCD) procedure (Fig. 3.43a), while maintaining a programming time compatible with industrial applications. In order to evaluate the impact of RESET and SET pulses on the local composition of our best

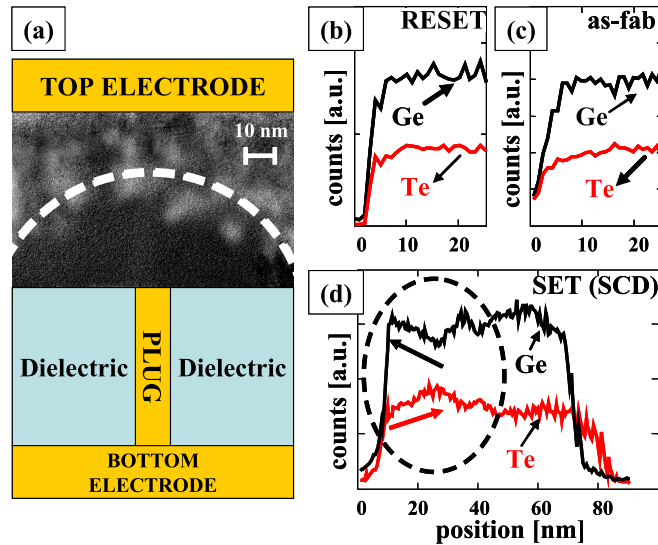


Fig. 3.44. (a) TEM picture of a RESET cell showing the dimensions of the cell active area. Evidence of post-seasoning composition stability is found by comparing EDX profiles (plug interface at 0 nm) of a RESET (pre-seasoned with 500 cycles) (b) and of an as-dep (c) GST-Ge45%-N4% cell. The EDX profile in (d), evidences the change of distribution of Ge and Te during the SET-SCD operation.

trade-off material GST-Ge45%-N4% (trade-off between SET drift and data retention performance), we analyzed through EDX profiles the atomic displacement of Ge and Te. Fig. 3.44 proves the stability of the HRS composition in GST-Ge45%-N4% cell after seasoning. Moreover, the EDX profile of Fig. 3.44d evidences the change of spatial distribution of Ge, and Te during the SET-SCD operation. This is a sign that during the SET procedure, also some atomic displacement is ongoing, correlated probably with the Ge segregation.

To be finally compliant with industrial standards, the final memory product has to preserve pre-coded information (generally the code for the standard functionalities of the memory), also after the soldering procedure on the PCB board. During the soldering provided with automatic temperature profile the die reaches the temperature peak of 260 °C. Standard phase-change materials, like GST, cannot sustain this temperature, losing all the information stored in the device. Hence, the need in standard PCMs, of a post-coding procedure (through a dedicated input port), once the memory is already soldered.

To overcome this problem, our materials represent a valid solution, thanks to their really high crystallization temperature. But at the same time, we showed that if not correctly programmed, the cells can lose their information because of the drift of the SET state at high temperatures. In Fig. 3.45 we provide the successful reflow soldering temperature profile (RSTP) tests for HRS and LRS (obtained with our R-SET pulse) of GST-Ge45%-N4%, which finally offers the best trade-off between data retention performance, resistance window, speed, and drift of LRS. It also confirms the high-temperature operations capability of our devices.

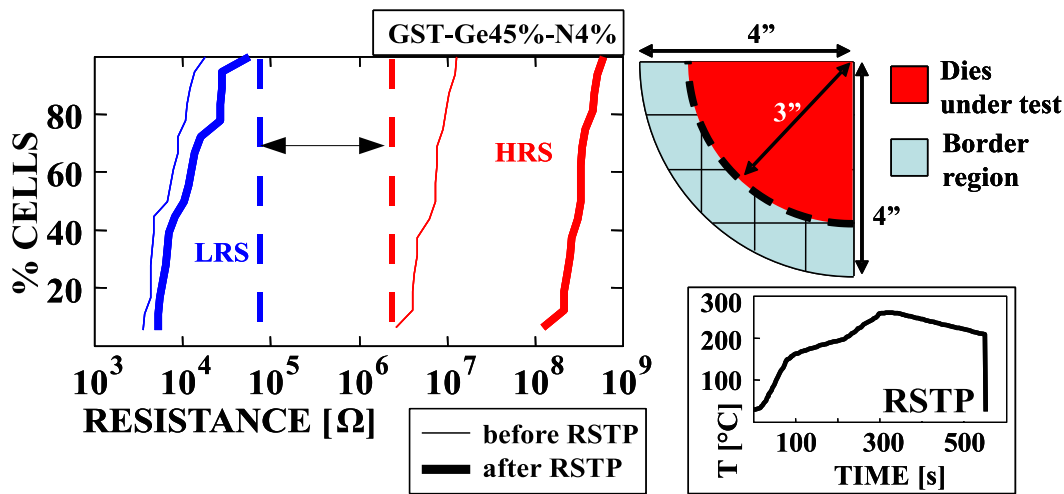


Fig. 3.45. RSTP applied to the HRS and the LRS (obtained with our R-SET procedure) of GST-Ge45%-N4%. In the worst case, a window of more than one order of magnitude is preserved after the RSTP procedure.

3.4.4 Conclusions

In this section we addressed for the first time, the optimization of SET performance and high thermal stability through innovative phase-change materials. We first demonstrated the high data retention capability of Ge-rich GST alloys (10 years data retention of 210 °C), at the expense of an increasing SET drift coefficient with the Ge at. %. The N- and the C-dopants act as softeners of the drift, offering also a better resistance window and higher stability of post-seasoning composition in N-doped devices. Based on cartographies of the SET operation in our devices, we introduced a “best-programming-current-vs-time-profile” which allows to achieve a valid LRS, with low drift coefficient, and industrially-compliant programming times (< 800 ns). Finally, RSTP tests demonstrated the good thermal stability of the HRS and of the LRS thanks to the GST-Ge45%-N4% alloy coupled with an optimized R-SET programming procedure.

3.5 Discussions

The engineering of the phase-change material led us to enhance the final performance of the PCM device, in terms of resistance stability (i.e. data retention improvement and lowering of the drift phenomenon), programming power, cycling endurance, programming speed and resistance window. On the other hand, we highlighted the difficulty to improve all these aspects at the same time due to their direct link with the same material properties. For example, the attempt to increase the crystallization temperature of the material, in order to boost the data retention at high temperatures, showed as drawback the reduced crystallization speed of the device. In fact, the changed crystallization dynamics induced by the introduction of dopants or by the changed stoichiometry, can enhance the thermal stability of the material, but at the same time decrease the nucleation rate and/or the growth speed of the phase-change material. Moreover, the impact on cyclability and on the resistance window of the device can be detrimental, like observed in section 3.4 for C-doped samples. Hence, as direct conse-

quence, a proper trade-off between the performances suited has to be found, identifying the right phase-change material that fulfills the main requirements of the target application. An example of this analysis, has been provided in the previous section where a specific phase-change material (GST-Ge45%-N4%) has been identified to fulfill the particular requirements in terms of data retention and resistance stability.

The use of GeTe in a PCM device, can assure high speed and a really large resistance window. This latter property is particularly interesting to achieve multi-level capability. Moreover this material presents a higher crystallization temperature with respect to standard GST (180 °C and 140 °C respectively). In our study, we demonstrated the possibility to further improve its thermal stability (through the stoichiometry engineering) and solve the problem of the high read voltage sensitivity at working temperature higher than 60 °C (through SiO₂ doping), although at the expense of the crystallization speed. The main problem of GeTe remains its composition stability during cycling, which manifests in particular in Ge segregation. Even if we demonstrated 10⁷ cycles capability in not stoichiometric samples, GST shows, already in analytical devices, capability of 10⁹ cycles as reported in section 2.6.7. GST has not the same speed performance of GeTe in the order of nanoseconds, but can still guarantee a programming speed in the order of tens of nanoseconds. Its composition stability along cycling, as reported in section 2.6.1, is likely a reason to consider GST as more suitable for automotive and industrial applications. This aspect, generated our interest in enhancing the thermal stability and speed of this material, as we successfully obtained in our work.

3.6 Summary of the chapter

Embedded PCM technology is competitive to rivals, such as embedded Flash, because of its much faster write operations, comparable or better read performance, lower manufacturing cost, and higher endurance. What makes it also a promising candidate for the next non-volatile memory generation is its compatibility with a standard CMOS process when using a MOSFET as the access device, requiring a modification of the process steps only in the back-end of the line (BEOL). If the already demonstrated highly scaling capability of this mature technology can reduce the final power consumption of the PCM device, its poor high temperature stability has been considered as an obstacle to address final automotive and multi-level applications. In this light, our work demonstrated the possibility to engineer the phase-change material to achieve a higher thermal stability of the memory cell, overcoming some of the main bottlenecks of the PCM technology.

Through the tuning of the stoichiometry, we demonstrated that the increase of the Te at. % in GeTe-based phase-change memories, can boost the thermal stability of the devices and reduce the programming power, at the expense of the final programming speed. For these materials, a compromise has to be found between data retention, power consuming and programming speed, dependently on the target application.

The decrease of the threshold voltage V_{TH} at high operating temperature, can

represent a limitation even for materials that demonstrated good data retention performance (e.g. GeTe). Thanks to the changed crystallization dynamics induced by SiO₂ inclusions in the material, we opened the possibility to engineer V_{TH} allowing high-operating-temperature applications.

The programming current reduction being extremely important for embedded applications, we proposed the carbon doping as solution to be coupled with the device scaling. At the same time, this method turned detrimental for the device speed and for the final resistance window.

Finally we studied the Ge enrichment in GST, combined with N or C doping integrated in state-of-the-art PCM devices. The results we obtained, in terms of data retention, are among the best reported in the literature (extrapolated 10 years data retention at 210 °C). We showed how both the high resistance state and the low resistance state of the cell are affected by the drift of the resistance towards higher resistance values, becoming a problem for the resistance window stability. Through the introduction of a new programming technique, we demonstrated the possibility to improve the programming speed, highly reduced by Ge enrichment, and to reduce the LRS drift phenomenon with respect to standard SET procedures. We then proved, with these last results, the suitability of PCM for embedded applications.

Conclusions and perspectives

Embedded non-volatile memories (NVM) have become a major component of many modern systems. In decentralized and mobile units, they enable autonomous software control and management of an increasing amounts of data [144]. One of the markets with the most stringent specifications is the automotive one, which requires operations from $-40\text{ }^{\circ}\text{C}$ up to more than $150\text{ }^{\circ}\text{C}$. Moreover, mobile applications continuously push memory requirements further, making power consumption optimizations for memory critical [145]. While Flash will extend probably further than what is expected, Phase-Change Memory (PCM) technology already showed the possibility to replace Flash in a wide range of applications thanks to its scalability, endurance, write performances and cost per bit [4, 146].

The PCM technology, owes its functionality to the reversible thermal activated transition of a phase-change material, from a high resistive amorphous phase, to a low resistive crystalline phase. This transition, in a PCM device, is obtained by the current induced Joule heating of the phase-change material, giving rise to the crystallization process of the material. The reverse phase-change, similarly, is obtained increasing the current in the device, and achieving the melting of the phase-change material. The fast quench of the liquid phase, restores the initial amorphous phase. The combination of the electrical and thermal properties of the phase-change material integrated in the phase-change memory cell defines the final behavior of the device.

Many efforts have been made in the last years to improve the thermal stability of the PCM cell. In fact, the main reliability issue of this technology is the strong impact of the temperature on the device performance. The work presented starts from this context, addressing the comprehension of the origins of the PCM device failure, with the main goal to optimize the memory cell and open the road for the fulfillment of the embedded market requirements.

Like other resistive NVM, a PCM is a two-terminal device. Despite the simplicity of the device concept, the cell scaling required in the last years the development of innovative structures. In our work, taking advantage of these designs, we fabricated three different PCM device structures: the lance-type structure, the confined structure and the μ trench structure. The lance-type PCM revealed its limit in the dependency on the lithography technology. The scaling of this structure, obtained by the scaling of the plug diameter down to 50 nm , allowed to verify the increasing impact of the thermal boundaries. In fact, while the density of programming current is supposed to be constant, at low dimensions this relation is invalidated by the increasing of the thermal loss at the boundaries, causing the rising of the current density required to program the cell. The confined structure has been implemented by means of the spacer technique. The deposition of the phase-change material in a via, showed the potentiality

of the better thermal confinement, on the reduction of the programming current of the cell (reduced by 20 times with respect to equivalent lance-type device), already in not highly scaled confined cells with diameter size of 100 nm.

The μ trench structure, was used as test vehicle to analyze the reliability of the PCM technology at high operating temperature, highlighting the main effects of the temperature increase on the device performance. We showed the fast programming operations in a μ trench cell, thanks to the fact that the peak of the current density is localized at the plug/phase-change material interface. The reduction of the threshold voltage at high operating temperatures and the shift of the programming resistance characteristic down to lower values have been investigated. Moreover, we demonstrated the strong impact of the thermal stress produced in the cell during the SET operation on the life time of the cell, by means of electrical measurements and simulations. The softening of this effect at high temperatures, revealed an improvement of the endurance from 10^8 (at room temperature) up to more than 10^9 (at 85 °C).

In the frame of the collaboration with STMicroelectronics, we integrated standard (like GST and GeTe) and innovative phase-change materials in state-of-the-art “Wall” PCM devices. The subthreshold switching phenomenon has been deeply analyzed in these devices, introducing a statistical approach based on the electric field activated nucleation theory, finding an experimental confirmation to the predictions of this model. In particular, we showed how switching can take place below the threshold voltage, when the time of the programming pulse is long enough and/or the temperature is high enough.

We presented our characterization setup, designed to perform our analytical tests, and some of the test procedures used to study the reliability issues of PCM. A specific electronic board has been developed in order: to minimize the parasitic capacitance of the system to reduce transient phenomena; to guarantee high disturb rejection; to provide a stable and protected ground to the device tested. Moreover, we developed all the control softwares used to perform our characterizations. The high speed of the final hardware/software developed, allowed to obtain good statistics of the parameters observed.

The simulation tool implemented in MATLAB and C code, used to simulate the behavior of our PCM devices, has been implemented taking in consideration the thermal and the electrical properties of a phase-change material. In particular, a new equation to model the conduction of the ON-state and the liquid phase was introduced. Our tool allowed us to fit the electrical behavior of different structures under test, understanding the different mechanisms taking place in the cell during the RESET and the SET operations. Overall, we were able to simulate the impact of the growth speed and of the thermal conductivity of the phase-change material, on the RESET current of the device.

The engineering of the phase-change material integrated in the PCM device, in order to fulfill embedded NVM requirements, was the main goal of this work. We started with the analysis of GeTe, material interesting because of its large resistivity window, its higher crystallization temperature with respect to standard GST (180 °C with respect to 150 °C), and its high crystallization speed (~ 1 ns). By means of physico-chemical analysis, and electrical characterization, we demonstrated the possibility to change the PCM performance, tuning the material stoichiometry. We showed that the increase of

the Te at. % in GeTe-based phase-change memories can boost the thermal stability of the devices (up to a fail temperature of 117 °C for 10 years of data retention) and reduce the programming power (by 26%). However, the decrease of the crystallization speed induced by Te at. % enrichment, obliges to find the compromise between data retention, power consuming and programming speed, dependently on the target application.

We showed the experimental results of the increase of the threshold voltage with the SiO₂ content in GeTe based cells. We correlated this phenomenon with the changed activation energy of the crystallization process and the changed crystallization dynamics due to the dielectric inclusions. It allows the threshold voltage engineering in high-operating-temperature applications. Moreover, we highlighted the significant reduction of programming power (by 50%), following the introduction of SiO₂ into GeTe, which enables addressing low-power applications. To reduce the programming power of the cell, we proposed also the carbon doping as solution to be coupled with the device scaling. We obtained a reduction by almost 50% of the RESET current with this method, turned detrimental for the device speed and for the final resistance window.

Finally we studied the Ge enrichment in GST, combined with N or C doping integrated in state-of-the-art “Wall” PCM devices. An extrapolated 10 years data retention at 210 °C was obtained in GST-Ge45%-N4% devices, among the best reported in the literature. We addressed for the first time the problem of the stability of the SET state in these innovative materials, revealing the drift of the resistance state towards higher values, even in devices programmed in the LRS. It represents a problem, in particular at high temperatures, at which this phenomenon is activated. With the engineering of a new programming technique and the relative design of the programming generator circuit, we demonstrated the possibility to improve the programming speed, highly reduced by Ge enrichment, and to reduce the LRS drift phenomenon with respect to standard SET procedures. Moreover, we showed how this solution ensures the passing of the reflow soldering temperature profile test. Hence, it allows the preservation of the pre-coded information when the final chip is soldered on the electronic board.

We proposed and studied an original PCM architecture, that can be suitable also for the analytical study of new phase-change materials: the μ ring structure. At the time of the writing of this work, the last steps for the device fabrication of this structure are still on going, preventing us to report the final electrical result on these devices. We report also that we started the investigations on the physical origins of the reduction of the LRS drift in Ge-rich GST materials, obtained by means of the new electrical programming technique proposed. Moreover, a first 12 Mb demonstrator produced by STMicroelectronics based on our engineered Ge-enriched phase-change material composition is in production. A detailed study of the final product, will permit to confirm our findings. All these, represent the future perspectives of our work.

PCM technology, after 10 years of development, started to enter the market as Flash replacement, in Smart Grids technology (Micron), and as stand-alone memory for mobile applications (Samsung). First embedded demonstrators for the 90 nm technology node, have been presented in 2011 by STMicroelectronics (4 MB) and this year by IBM (256 MB) showing the increasing interest in this technology of different competitors, and the compatibility with the standard CMOS industrial process. During the advancement of our work, PCM has crossed the status of “innovative” device, starting to be considered a real competitor in the NVM market, and a reference of comparison

for other memory technologies. We believe, that in the next future, thanks also to our work, its unique capabilities will be exploited in embedded applications in different electronic systems. This will represent the second real revolution for the phase-change materials after their use in optical applications, in the history of the technology applications.

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Résumé en français

Introduction

Les mémoires ont gagné une importance exponentielle dans notre époque actuelle, et sont fondamentales dans la définition de tous les systèmes électroniques avec lesquels nous interagissons dans la vie quotidienne. Ainsi, les technologies de mémoire sont devenues plus qu'une technologie de simple support, avec l'introduction de la notion de «électronique mémoire-centrée». Les mémoire non-volatiles, représentés par la technologie Flash, ont pu suivre jusqu'à présent la tendance à la miniaturisation pour satisfaire la densité de mémoire de plus en plus grande exigée par le marché. Toutefois, la mise à l'échelle est de plus en plus difficile, avec la hausse conséquente du coût par octet des mémoires Flash en raison de la complexité technologique. Dans ce contexte, les technologies de mémoire innovantes deviennent pas seulement une alternative, mais la seule solution possible pour fournir une densité plus élevée à moindre coût, une meilleure fonctionnalité et une faible consommation d'énergie. La grande quête est d'identifier une technologie en mesure de garantir la mise à l'échelle pour plus de nœuds technologiques consécutifs.

Différents études au cours des dernières années ont amené des nouvelles solutions pour remplacer les mémoires traditionnelles. Au lieu de déplacer et de piéger des électrons comme dans la mémoire Flash, des approches innovants ont été étudiés, en changeant et en simplifiant également la conception du dispositif. Une mémoire résistive est basée sur un dispositif à deux contacts, dans lequel un matériau «actif» est introduit entre deux électrodes. L'idée principale de cette structure, est d'utiliser un mécanisme physique spécifique du matériau actif considéré, pour le basculer de façon réversible, entre deux états résistifs complètement différents. Dans une mémoire à changement de phase (PCM) un matériau chalcogénure (matériau à changement de phase) est utilisé, en profitant de la transition induite par la chaleur entre une phase amorphe et une phase cristalline.

La technologie PCM est considérée comme la solution plus avantageuse pour la prochaine génération de NVM, grâce à des capacités uniques par rapport aux autres technologies de mémoire concurrentes. En particulier, cette technologie propose non-volatilité, scalabilité, «bit-alterability», grande vitesse de lecture et d'écriture, cyclabilité élevée et aussi dureté au rayonnement (nécessaire dans les applications spatiales ou des instruments physiques de haute énergie).

Même si la technologie PCM est aujourd'hui une technologie industrielle de maturité reconnue, certains problèmes de fiabilité restent à surmonter, afin d'être un remplaçant valable de la technologie Flash dans toutes les applications possibles. En fait, la stabilité thermique à des températures élevées des matériaux à changement de phase intégrés

dans un dispositif PCM, est un défi intrinsèque de cette technologie. La conservation des données dans des environnements à haute température est l'une des principales exigences des applications industrielles et automobiles embarquées, comme les micro-contrôleurs et autres circuits intégrés qui intègrent des mémoires non-volatiles. Les opérations nécessaires entre $-40\text{ }^{\circ}\text{C}$ à plus de $150\text{ }^{\circ}\text{C}$, le processus de soudage par re-fusion à $260\text{ }^{\circ}\text{C}$ et l'exigence de «zéro-défauts», sont aujourd'hui les grands défis de la technologie PCM pour finalement satisfaire toutes les exigences du marché. En outre, la capacité multi-niveau peut ouvrir la porte à une densité de données plus élevée.

Chapitre 1 : La technologie de la mémoire à changement de phase

Le concept de l'utilisation de la transition de phase entre l'état amorphe et l'état cristallin des matériaux chalcogénures pour stocker des informations a été proposé depuis le début des années 1960 par Stanford Robert Ovshinsky, qui est considéré le père de dispositifs de mémoire à changement de phase. Le principe de la transition de phase dans un dispositif de PCM est basé sur le changement de phase du matériau, induit thermiquement, à partir d'une phase cristalline, ordonné et faiblement résistive, pour arriver à une phase amorphe, désordonnée et très résistive, en passant par la phase liquide. Pour parvenir à la phase amorphe, le matériau à changement de phase, initialement dans la phase cristalline, doit être fondu (en atteignant la température de fusion T_m), par Effet Joule à des densités de courant élevées, et puis rapidement refroidi (opération de «RESET»). Grâce au phénomène de «switch électronique», une fois atteint un seuil de champ électrique spécifique (E_{TH}), le matériau amorphe change brusquement sa conductivité et commence à être très conducteur (ce que nous appelons «état-ON»). Le matériau à changement de phase, une fois dans l'état-ON, est ensuite cristallisé par chauffage par effet Joule, obtenu avec la circulation de courant (opération de «SET»).

La cellule PCM

Une cellule PCM est un dispositif basé sur deux électrodes. Elle fonde sa fonctionnalité sur la forte différence de résistivité (jusqu'à plus de 5 ordres de grandeur) entre la phase cristalline et la phase amorphe des matériaux à changement de phase. Dans la Figure 1, nous pouvons voir un exemple de cette transition. Le matériau amorphe est chauffé, et au cours de l'augmentation de la température, il présente une diminution de la résistivité à une température donnée, appelée température de cristallisation. Le processus de cristallisation, activé et favorable à cette température, contribue à la cristallisation de la totalité du volume amorphe, et augmente considérablement la conductivité du matériau. Une fois que le matériau est refroidi à température ambiante, la phase cristalline est préservée. Le processus complet donne lieu au mécanisme de changement de phase induit, dans ce cas, par le chauffage externe. La cellule PCM, comme indiqué dans la Figure 2, se compose des parties suivantes :

- l'électrode inférieure ;

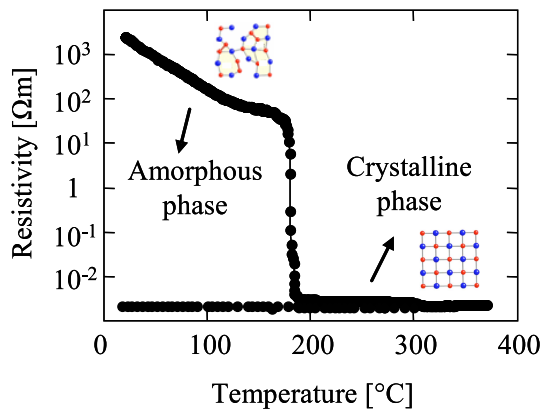


Fig. 1. Résistivité en fonction de la température d'un matériau à changement de phase. La transition de la phase amorphe à la phase cristalline, est mise en évidence par la forte diminution de la résistivité du matériau.

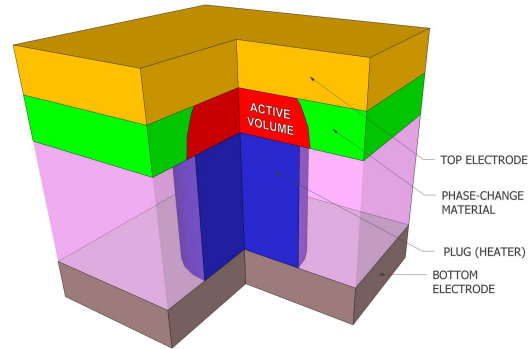


Fig. 2. Description générale d'une cellule PCM. Le volume actif impliqué dans la transition de phase est mise en évidence à l'interface entre le matériau à changement de phase et le plug.

- l'élément conducteur «plug», avec la fonction de fournir l'accès électrique à la cellule, de permettre la limitation de courant, et de contribuer au chauffage du matériau à changement de phase dans les différentes phases de la programmation ;
- le matériau à changement de phase ;
- le matériau diélectrique qui entoure le plug ;
- l'électrode supérieur.

Pour programmer une cellule PCM dans l'état RESET, une impulsion de RESET est appliquée, consistant en une impulsion de haut courant en mesure d'élever la température au-dessus de T_m dans le volume de chalcogénure actif, suivie d'une descente très rapide, en mesure de refroidir le même volume dans un état amorphe. L'opération de RESET peut être efficace que si un volume considérable de matériau est amorphisé sur la surface du plug, afin d'augmenter considérablement la résistance de la mémoire. Pour programmer la cellule dans l'état SET deux stratégies principales peuvent être adoptées :

- L'application d'une impulsion avec la même amplitude d'une impulsion de RESET, mais avec une descente suffisamment longue pour garantir la permanence du matériau à changement de phase dans la plage de températures favorables à la recristallisation ;
- Une impulsion de plus faible amplitude par rapport à l'impulsion de RESET, mais plus élevée que la tension de seuil, capable de fournir déjà au cours de l'impulsion la bonne température de cristallisation dans la zone active du matériau à changement de phase.

La forme de l'impulsion devient fondamentale pour la programmation de la cellule, étant donné que le paramètre principal à jouer sur le changement de phase est la température. Effectivement, la température est augmentée dans le dispositif par le chauffage par effet Joule induit par courant, et par des formes d'impulsion différentes, correspondent à des profils de température spécifiques dans la cellule.

Les matériaux à changement de phase

Les matériaux à changement de phase appartiennent à la famille des chalcogénures. Ces matériaux à température ambiante peuvent présenter soit la phase amorphe, soit la phase cristalline, étant donné que la transition de phase est un processus réversible. Ainsi, le mécanisme de cristallisation devient fondamentale, et sa vitesse influe sur la performance de la cellule de mémoire dans lequel le matériau à changement de phase est intégré. La cristallisation est le résultat de la combinaison de deux mécanismes différents : la nucléation et la croissance. Ces mécanismes varient dépendamment du matériau à changement de phase considéré. Le $\text{Ge}_2\text{Sb}_2\text{Te}_5$ et le GeTe , sont les principaux matériaux à changement de phase utilisés dans la technologie PCM, et le point de départ de notre travail.

Le GeTe est largement étudié en raison de sa grande rapidité de cristallisation. Sa recristallisation sous l'effet de impulsions laser de la durée d'un fs a été démontrée pendant les test sur les couches minces. Sur la plupart de la surface pré-amorphisée il a été observée une recristallisation à partir de l'interface entre la région amorphe et la phase cristalline. Seulement dans les procédures de cristallisation très longs, la nucléation a été observée couplé au processus de croissance. La température de fusion de ce composé est d'environ $725\text{ }^\circ\text{C}$ alors que la température de cristallisation est de l'ordre de $180\text{ }^\circ\text{C}$. Dans les résultats expérimentaux pour évaluer la température de cristallisation, la transition de l'état amorphe à la phase cristalline est nette : une fois que le noyau est généré au cours du processus de chauffage, il se développe très rapidement.

Le $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST), grâce à sa stabilité thermique à température ambiante et sa cristallisation relativement rapide sous irradiation laser (50 ns), a été considéré, depuis le début des années 1990, comme un matériau idéal pour l'enregistrement optique. De plus, ses propriétés ont fait de ce matériau, le premier matériau à changement de phase considéré un valable candidat pour les applications PCM. Sa température de cristallisation est de l'ordre de $150\text{ }^\circ\text{C}$, tandis que sa température de fusion est d'environ $660\text{ }^\circ\text{C}$. Les études sur le mécanisme de recristallisation des marques amorphes lors d'une irradiation au laser ont révélé que le GST recristallise par nucléation et qu'il y a une croissance ultérieure des cristaux à l'intérieur de la marque amorphe, la nucléation hétérogène étant le mécanisme fondamental qui contrôle la cristallisation dans le GST.

La cinétique de cristallisation

Le mécanisme de cristallisation affecte des nombreux aspects de la vie d'un dispositif PCM. En particulier il affecte la vitesse de programmation, et la stabilité de la phase amorphe. Pour décrire le processus de cristallisation, nous nous référons à la théorie classique de la nucléation (CNT). Les hypothèses principales de cette théorie sont la composition inchangée du matériau au cours de la cristallisation et la nature «diffusion-limited» du processus. L'énergie libre du système, constitué par un amas de phase cristalline en évolution dans la phase amorphe environnante, est exprimé comme la somme des contributions du noyau et de la phase amorphe. Ces termes sont intégrés par des contributions interfaciales, et dont la principale est donnée par le produit de l'aire interfaciale et l'énergie de surface spécifique. En appliquant la théorie de la formation de clusters, ces termes de surface se traduisent d'abord par une augmentation du potentiel

thermodynamique caractéristique et l'existence d'une taille critique (nucléation). Seuls les clusters avec des tailles plus grandes que la taille critique sont capables de grandir de façon déterministe jusqu'à des tailles macroscopiques (croissance). La nucléation des cristaux et la consécutive croissance contribuent au phénomène de cristallisation. Ce processus peut être décrit par la détermination de la fraction volumique de la phase transformée ($\alpha(t)$). La théorie formelle de la cinétique de cristallisation dans des conditions isothermes est bien connu aujourd'hui comme la théorie JMAK. Avrami a proposé l'équation suivante pour décrire la cinétique de cristallisation :

$$\alpha(t) = 1 - e^{-Kt^n} \quad (1)$$

où les paramètres K et n peuvent être estimés par l'interpolation des données expérimentales, et sont mises en corrélation respectivement avec le taux de nucléation et la vitesse de croissance (K), et avec l'«ordre de réaction» du processus de cristallisation (n).

La phase cristalline

Dans un matériau à changement de phase, la phase cristalline a une plus faible énergie libre par rapport aux autres phases. La transition entre les différents états d'un matériau à changement de phase est semblable à un réarrangement progressive des atomes, en passant par des états métastables (état amorphe et phases cristallines intermédiaires), jusqu'à l'atteinte d'un minimum de l'énergie libre de Gibbs. Ce réarrangement peut être réalisée en surmontant une barrière d'activation énergétique, en particulier grâce à la contribution de la température.

La structure cristalline stable du GST est hexagonale (hcp), mais sur la base des mesures XRD, une couche de GST cristallisée par un faisceau laser possède la structure du sel gemme métastable (cubique face centrée ou fcc) avec des atomes Te qui occupent les sites sur un sous-réseau fcc avec Ge et Sb qui forment l'autre sous-réseau fcc (étant vacant le 20% des sites). Il a été suggéré que la structure cubique du GST (qui est plutôt isotrope et donc plus similaire à la structure amorphe que à toutes les autres structures cristallines) est à la base de la rapidité de la cristallisation et de la stabilité de ce matériau, puisque la structure hcp est énergiquement plus cher à obtenir.

La différence dans les propriétés électriques entre les différents arrangements de cristal est décidé par la présence de lacunes en excès. Le GST fcc a une conductivité électrique de type p, avec le niveau de Fermi dessus de la bande de valence (~ 0.15 eV) qui donne lieu à une conduction de type semi-conducteur. Plus la température est élevée, plus le nombre d'électrons promus dans la bande de conduction est élevé, ce qui réduit la résistivité finale du matériau, conformément à la loi

$$\rho = \rho_0 e^{\frac{E_C}{k_B T}} \quad (2)$$

où ρ est la résistivité du matériau, ρ_0 est une constante, E_C l'énergie d'activation de la conduction.

La phase amorphe

Nous trouvons deux types de phases amorphes : la phase amorphe du matériau tel que déposé, et la phase amorphe vitreuse. La première provient de la technique de dépôt,

qui ne permet pas à une structure atomique régulière du film déposé de matériau à changement de phase. La seconde, est la plus intéressante du point de vue de dispositif final. En effet, une fois atteint la phase liquide par effet Joule, un refroidissement rapide du matériau va geler la phase liquide en préservant sa structure désordonnée. Grâce à des simulations atomistiques il a été démontré que le meilleur accord avec les résultats expérimentaux a été obtenu quand le Ge acquiert sa configuration tétraédrique dans la phase amorphe. Cette transformation structurale peut être expliquée quand les atomes de Ge, au sein de la structure fcc formé par des atomes de Te, forment une symétrie octaédrique dans l'état cristalline et une symétrie tétraédrique dans l'état amorphe («flip» atomique). Il est bien connu que les «lone-électrons» sous-tendus aux atomes de Te peuvent jouer un rôle dans ce changement de la configuration de la liaison atomique.

Dans la théorie classique, l'état-ON est obtenu dans le matériau amorphe, après le franchissement d'un seuil critique E_{TH} , à où tous les pièges sont remplis et la recombinaison est fortement réduite (tous les défauts remplis) et ne peut que partiellement équilibrer le taux de génération. Selon une approche théorique complètement différent, le champ électrique élevé induit dans le matériau amorphe une nucléation localisée, ce qui conduit à une formation progressive d'un filament conducteur composé de noyaux cristallins, en parfait accord avec la théorie de la percolation.

La stabilité de la phase amorphe a été profondément étudiés ces dernières années, en particulier parce qu'elle affecte la rétention des informations stockées dans le dispositif PCM. Deux mécanismes principaux influent sur la stabilité de cette phase :

- La relaxation structurale activé thermiquement, qui peut être observée expérimentalement dans l'augmentation dans le temps de la résistivité du matériau (drift) ;
- Le processus de recristallisation, qui au contraire réduit la résistivité du matériau.

L'impact de la mise à l'échelle du volume de matériau à changement de phase

Dans des nanoparticules de matériau à changement de phase, il n'y a pas une seule dimension qui est réduite, mais la totalité du volume. En général, grandes nanoparticules présentent des propriétés semblables aux propriétés macroscopiques, mais les plus petites nanoparticules inférieures à environ 10 nm montrent une cristallisation dépendant de la taille, dans la plupart des cas une augmentation de la température de cristallisation et une réduction de la température de fusion. Les deux sont bénéfiques pour les applications PCM et démontrent les propriétés d'échelle favorables des matériaux à changement de phase. Les limites ultimes de l'échelle seront atteintes lorsque les matériaux ne sont plus stable dans les deux phases. Pour le GeTe il a été démontré que les nanoparticules (1.8 nm) peuvent être synthétisés dans la phase amorphe et peuvent être cristallisés en les chauffant au-dessus de leur température de cristallisation. Même à cette taille, les matériaux à changement de phase ne perdent pas encore leurs propriétés de changement de phase : c'est une démonstration du grand potentiel en termes d'évolutivité de cette technologie, qui en fait un candidat idéal pour la nouvelle génération de mémoires non-volatiles.

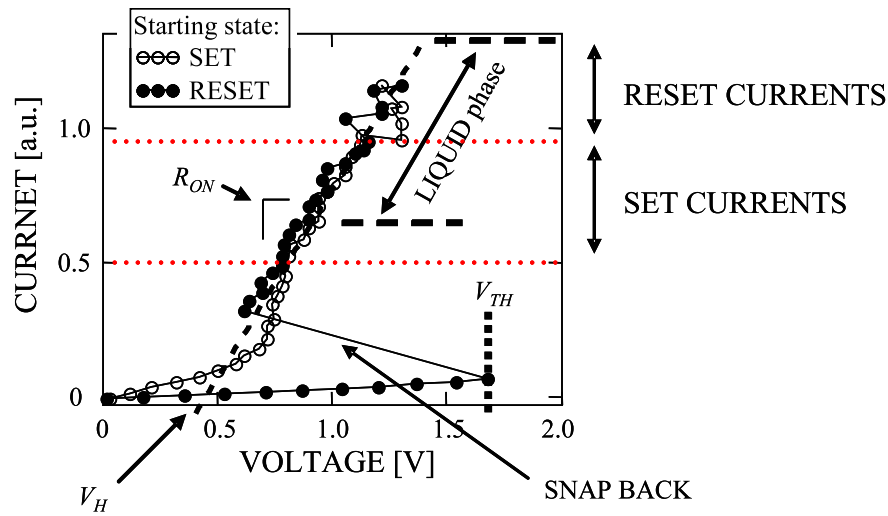


Fig. 3. Caractéristique courant-tension d'un dispositif PCM basée sur GST. Le départ à la fois de l'état SET et de l'état RESET est comparé, en mettant en évidence les paramètres électriques typiques de chaque état de la cellule.

Chapitre 2 : La cellule de mémoire à changement de phase : structures et fiabilité

Les propriétés du matériau à changement de phase intégré dans un dispositif de mémoire affectent fortement les performances électriques de la cellule.

Figure 3 décrit la caractéristique courant-tension (IV) typique d'un dispositif PCM. Quand on commence avec une cellule dans la phase amorphe, l'augmentation de la tension sur le matériau à changement de phase provoque une augmentation de la conductivité. L'atteinte de la tension de seuil V_{TH} produit le phénomène de «switch électronique». Une fois atteint l'état ON, le dispositif peut éprouver une gamme de courants, dans lequel le matériau à changement de phase arrive à une température favorable pour la recristallisation, qui permet le «SET» de la cellule. Si le courant fourni est supérieur à cette gamme de courants, le matériau à changement de phase fond, et dépendamment de la vitesse de l'enlèvement d'impulsion, le matériau peut conserver la structure amorphe (temps de chute courte de l'impulsion) ou recristalliser (temps de chute plus long).

Pour résumer le comportement électrique de la cellule, les principaux paramètres que nous pouvons extraire de la caractéristique IV sont :

- la tension de seuil V_{TH} : il représente la tension à laquelle la cellule à l'état RESET, commue à l'état ON ;
- le courant de RESET ;
- le courant de SET ;
- le courant de fusion I_m ;
- le voltage de «holding» V_H , défini comme la chute de tension sur le matériau à changement de phase à l'état ON ;

- R_{ON} , qui représente la résistance de la cellule à l'état ON. Cette résistance est principalement due à la contribution du plug et de la partie du matériau à changement de phase qui n'est pas impliquée dans la transition à l'état ON. Le plug est donc la seule façon pour rendre la cellule PCM auto-fonctionnelle, en limitant le courant pendant le «switch électronique».

À partir de la caractéristique IV on peut extraire l'équation dynamique qui décrit la chute de tension sur la cellule (V_{CELL}) en fonction du courant pendant la programmation (I_{ON}), une fois que la cellule est à l'état ON :

$$V_{CELL} = R_{ON}I_{ON} + V_H \quad (3)$$

On peut donc comprendre comme la puissance délivrée à la cellule pendant l'impulsion, est due à une contribution résistive (effet Joule)) et une contribution qui dépend de V_H .

L'interface entre le plug et le matériau à changement de phase, constitue le cœur de la mémoire à changement de phase. La fonctionnalité et la durée de vie du dispositif, dépendent de la qualité du dépôt et de l'adhérence consécutive du matériau à changement de phase sur la surface du plug. En effet, il s'agit de la région qui subit la contrainte thermique la plus élevée au cours de la programmation de la cellule. En outre, plus la mise à l'échelle du dispositif est élevée, plus la qualité de l'interface requise est élevée.

Pour atteindre une température donnée dans le dispositif, indépendamment de la taille, nous avons besoin d'une densité de courant spécifique, qui en première approximation ne dépend que des paramètres du matériau et de la géométrie de la cellule. En conséquence, la surface plug/matériaux à changement de phase (A_{PLUG}) influe directement le courant de programmation de la mémoire. Pour une structure de la cellule donnée et pour un matériau donné, une fois que la densité de courant J_R nécessaires pour l'opération de RESET est connue, le courant final de RESET, en première approximation, est fixé par la dimension de la surface A_{PLUG} :

$$I_R \simeq J_R A_{PLUG} \quad (4)$$

Cette relation a été démontrée être valable jusqu'au nœud technologique de 16 nm.

Au plus petites dimensions, l'effet du confinement thermique faible fourni par l'isolant entourant le plug devient important. En outre, comme les dimensions caractéristiques du dispositif se rapprochent du libre parcours moyen du phonon et de l'électron, les effets du transport balistique deviennent de plus en plus importantes. La génération de chaleur et la résistance thermique à ces dimensions dépendent de la diffusion électronique et des phonons dans les régions d'interface. Cet effet va augmenter la perte de densité de puissance dans le dispositif. La principale conséquence de cette analyse est que la mise à l'échelle du dispositif de PCM invalide l'éq. 4, et rende nécessaire une densité de courant de plus en plus élevée pour l'opération de RESET. En outre, la densité de courant accrue est préjudiciable pour la durée de vie du dispositif, car la contrainte thermique au niveau des interfaces et dans le volume actif est plus élevée.

Les principales structures de mémoire PCM

La mise à l'échelle d'un dispositif est obtenue par l'amélioration des techniques de fabrication, qui ne peuvent pas toujours surmonter les limitations intrinsèques de la

Structure	Principales Caractéristiques	Avantages	Désavantages
type «lance»	vertical, plug basé sur un via	fabrication simple, grande cyclabilité (10^{12})	mise à l'échelle limitée par la litho., mauvais conf. thermique
type «Edge»	horizontal, plug basé sur une couche métallique	surface définie par l'épaisseur du plug	difficulté de garantir un bon contact latéral
type «Bridge»	horizontal, cellule auto-échauffant	pas besoin d'un plug, bon confinement thermique	fabrication difficile, faible cyclabilité
Confinée	vertical, matériau actif déposé dans le via	bon confinement thermique, bonne scalabilité	besoin de techniques de dépôt très conformes
« μ trench»	vertical, surface active définie par l'épaisseur du plug et la litho. du trench	pic de température localisé, réduction de la puissance	pas de auto-limit. du courant, besoin du transistor d'accès
«Wall»	vertical, surface active définie par la surface du «wall»	bon contrôle du courant, simple intégration	X

Tabl. 1. Comparaison des différentes structures PCM qu'on été analysés. La structure «Wall» est aujourd'hui le meilleur compromis en termes de complexité de fabrication et de capacité de mise à l'échelle.

technologie lithographique disponible. L'autre solution est l'ingénierie de la structure du dispositif, ce qui augmente les possibilités de mise à l'échelle, grâce à des procédés de fabrication innovantes qui intervient dans la fabrication. Depuis le début de la technologie PCM, une de ses principales limites a été le courant de RESET, et beaucoup d'efforts ont été faits pour la réalisation de différentes structures de mémoire, avec l'objectif de réduire la surface du plug. Dans le tableau 1, nous présentons tous les principaux avantages et inconvénients des structures analysées. Nous avons choisi certaines de ces structures pour nos implémentations, afin d'effectuer nos tests analytiques et la recherche expérimentale de ce travail.

La structure de type «lance»

Le premier concept industriel de cellules PCM était celui décrit dans la Figure 2. La structure est verticale, et essentiellement réalisée par la gravure d'un via dans un diélectrique déposé sur l'électrode inférieure. Ensuite, le via est rempli d'un métal pour réaliser le plug. La structure verticale, en général, est favorable pour le «back-end» de la production de la mémoire. Dans cette structure, la mise à l'échelle dépend du diamètre du plug, et donc de la résolution de gravure et de la technologie de lithographie disponible. La structure de type «lance» démontre une bonne fenêtre de résistance (plus de 3 ordres de grandeur), grande vitesse (temps de SET de 40 ns et temps de RESET de 10 ns), et une grande cyclabilité jusqu'à 10^{12} cycles.

Nous avons réalisé notre structure de type «lance» en utilisant deux techniques de lithographie différentes :

- Lithographie DUV, pour des diamètres > 250 nm ;
- Lithographie à faisceau d'électrons, pour diamètres < 250 nm.

La Figure 4 présente les résultats d'une de nos cellules de type «lance». Dans l'exemple le plug est fait en tungstène. Le matériau diélectrique utilisé est SiO_2 , tandis que le matériau à changement de phase intégré dans les dispositifs est GeTe.

La structure confinée

La mise à l'échelle des structures verticales est limité par l'augmentation de la densité

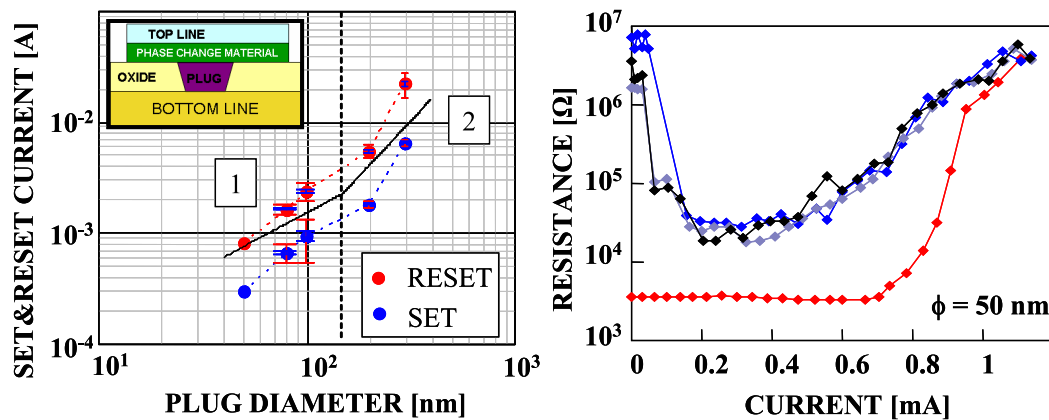


Fig. 4. Tendance de la courant de programmation, dans nos dispositifs PCM de type «lance». Le matériau intégré est GeTe. Sur la droite, les caractéristiques «résistance en fonction du courant programmation» d'un dispositif 50 nm (diamètre du plug), qui montrent la possibilité d'écrire et d'effacer la cellule.

de courant nécessaire à la programmation de la cellule, à cause de l'augmentation de la contribution de la dissipation thermique latérale de la structure à faibles dimensions. L'idée de la structure confinée est de «confiner» le matériau à changement de phase dans le via du plug de la structure de type «lance», et le remplacer partialement ou totalement. Cela améliore le confinement électrique et thermique du volume actif, étant donné que la puissance fournie au matériau à changement de phase est confinée par le diélectrique. La contrainte principale de cette technologie est le parfait remplissage du via (ou «pore») avec le matériau à changement de phase, réalisable uniquement avec les techniques de dépôt plus conformes telles que la CVD, qui dépend également du rapport d'aspect des pores à remplir. Dans notre étude, nous avons réalisé la structure confinée, mais associée à la technologie «spacer». Une fois créé le via de 300 nm, nous avons déposé une couche uniforme de nitrure de silicium (SiN) de 100 nm d'épaisseur, après gravé verticalement et anisotropiquement pour une épaisseur totale de 100 nm. Le résultat est un «spacer» de SiN au fond du via, avec la fonction principale de créer un pore de 100 nm de diamètre. La Figure 5 montre la cellule confinée finale, où nous avons

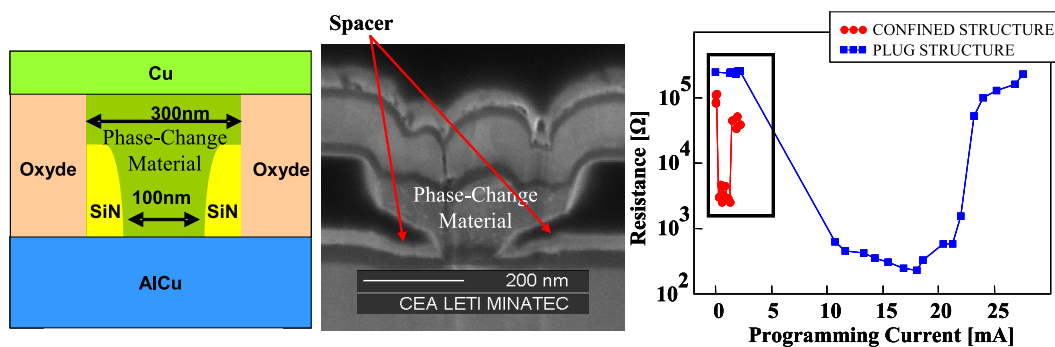


Fig. 5. La mémoire PCM avec structure confinée. Sur la gauche, la structure de base du dispositif de mémoire. Au centre, la photo MEB de notre structure confinée après la fabrication. À droite, les caractéristiques de programmation d'un dispositif de type «lance» de 300 nm, et d'un dispositif confinée réalisé avec le même via de 300 nm, mais avec technologie «spacer».

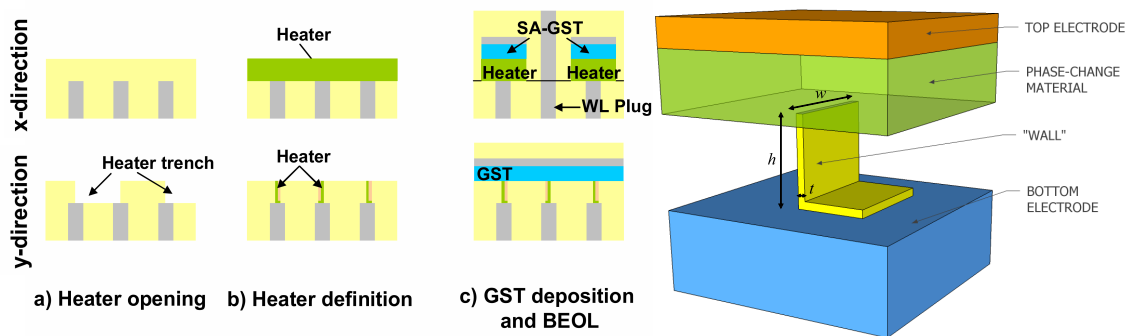


Fig. 6. Flow des procédés de fabrication de la structure «Wall» (à gauche). Schéma de la structure (à droite).

déposé le GeTe et où les «spacers» sont mis en évidence. Dans l'image sont présentées également les courbes de programmation du dispositif, comparé à un dispositif PCM de type «lance» : le courant de RESET est fortement réduit.

La structure « μ trench»

L'architecture « μ trench» représente la fusion de toutes les fonctionnalités intéressantes de la technologie PCM, car elle a attendu simultanément des courants faibles de programmation, potentialité de mise à l'échelle, un bon contrôle dimensionnel, et la capacité à être intégrée dans un processus industriel. Nous avons réalisé cette structure afin d'étudier les effets de la mise à l'échelle et en même temps la fiabilité de cette technologie. La structure « μ trench» a l'avantage que les opérations de programmation sont très rapides, grâce au fait que le pic de la densité de courant est toujours à l'interface entre le plug et le matériau à changement de phase, et que la puissance perdue dans le plug est réduite.

La structure «Wall»

La structure «Wall» représente l'évolution directe de la technologie « μ trench». Cette structure dispose de meilleures tolérances d'alignement lithographiques, en préservant le bon contrôle de courant de programmation, et présente un flow des procédés de fabrication plus simple (Figure 6). D'un point de vue fonctionnel, cette structure permet un meilleur contrôle des opérations de programmation. La mise à l'échelle de cette cellule PCM, doit être couplée à une sélection appropriée des propriétés thermiques et électriques du matériau à changement de phase intégré. Nous avons effectué nos études de fiabilité sur des dispositifs PCM «Wall» fabriqués en collaboration avec STMicroelectronics.

La caractérisation électrique de la cellule PCM

Les dispositifs d'analyse ont été conçus pour fournir un accès complet à l'électrode supérieure et inférieure de la cellule. Afin d'effectuer une détection suffisamment précise du dispositif, avec l'exclusion de toute la contribution résistive des lignes d'accès, nous avons utilisé une technique de type «Kelvin» (4 pointes) avec l'ajout de deux lignes d'accès par électrode. L'électrode inférieure est faite en alliage AlCu, protégé avec une couche de Ti/TiN pour améliorer l'adhérence à l'interface avec le plug, tandis que l'électrode supérieure est réalisée en cuivre. Les dispositifs sont de type «1R», sans sélecteur co-intégré. L'étude de la cellule PCM «1R» permet l'analyse plus directe du

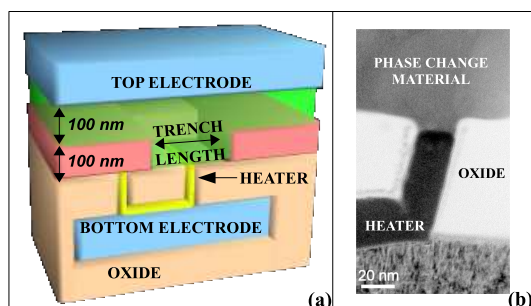


Fig. 7. (a) Schéma simplifié de notre structure «μtrench». (b) Image TEM qui montre l'interface entre le plug et le matériau à changement de phase.

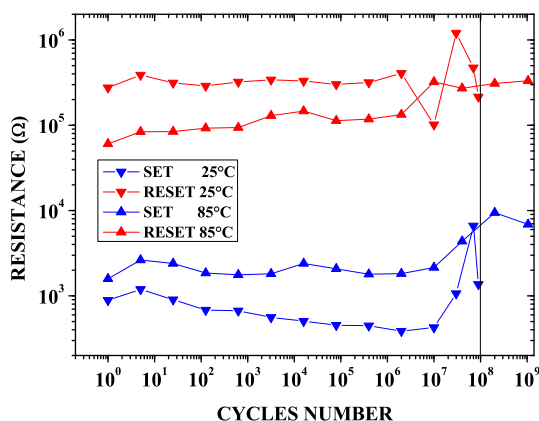


Fig. 8. Test d'endurance effectué sur un dispositif «μtrench». Nous observons l'augmentation de la cyclabilité des cellules (jusqu'à plus de 10⁹ cycles) une fois que la température augmente.

comportement du matériau à changement de phase intégré.

La caractérisation d'un dispositif est composée de trois parties principales : l'application d'une tension/courant, la détection et l'exportation/élaboration finale des données. Afin d'automatiser tout le processus de caractérisation électrique, nous avons développé une carte électronique avec deux caractéristiques principales :

- la possibilité de changer avec un contrôle automatique, la résistance extérieure mise en série avec le dispositif PCM pour limiter le courant pendant la programmation, au cours de la procédure de caractérisation ;
- la commutation entre l'électronique de génération d'impulsions, et le système de lecture de type «Kelvin».

La variation de la résistance série au cours de la procédure de caractérisation était nécessaire afin d'affiner le réglage du courant dans la plage de courants favorables à la cristallisation. La carte électronique a été conçue pour fournir une masse stable pour le dispositif PCM et une protection élevée contre les perturbations électriques.

L'étude de la fiabilité de la mémoire PCM

Nous avons étudié les principaux problèmes de fiabilité de la technologie PCM, et présenté une analyse spécifique de ces aspects dans le cas de la structure «μtrench».

Notre cellule de mémoire «μtrench»

Le schéma de la Figure 7 décrit la structure «μtrench» considérée. L'épaisseur du plug est contrôlée par le dépôt du film (30 nm), et la dimension de la tranchée par lithographie. Le matériau chalcogénure intégré dans nos dispositifs est le GST, en couches épaisses 100 nm, déposées par technique PVD. Le matériau du plug est le siliciure de tungstène.

La dépendance de la tension de seuil de la température «μtrench»

La diminution de V_{TH} lorsque la température de fonctionnement du dispositif augmente, peut augmenter le problème de perturbation due à la lecture. Celui-ci, associé à la

recristallisation de la phase amorphe, peut réduire la température de fonctionnement effective. La réduction linéaire de V_{TH} en température peut être attribuée à l'existence d'une conductivité électrique «critique» à laquelle la durée de vie des porteurs et le temps de relaxation du matériau sont égales. Le champ électrique de seuil (corrélé avec V_{TH}), pour atteindre cette conductivité, est donc réduit quand la température est augmentée, car la conductivité du matériau est plus élevée à haute température, comme l'éq. 2 met en évidence.

Au cours de l'impulsion de SET, quand la chute de tension sur la mémoire atteint le seuil V_{TH} , la conductivité de la cellule augmente brusquement (état ON), avec une résistance définie par R_{ON} . Cela, change la charge vue de la ligne d'accès à la mémoire, et elle génère un pic transitoire de courant dans la cellule ($\simeq V_{TH}/R_{ON}$). Ce pic de courant peut être plus élevé que le courant utilisé pour le RESET de la cellule si R_{ON} ne fournit pas une limitation de courant suffisante. Toutes ces considérations nous amènent à la conclusion que l'opération SET est une source de stress thermique pour la cellule, qui dépende de V_{TH} .

V_{TH} diminue à des températures de fonctionnement élevées, augmentant ainsi la sensibilité de la cellule à de faibles tensions de programmation. En le même temps, la diminution de V_{TH} se traduit par une diminution de la contrainte thermique pendant les opérations de RESET-SET.

Cyclabilité à basse et haute température

Les mesures de cyclabilité ont été réalisées à température ambiante sur des dispositifs « μ trench» pour démontrer la possibilité d'atteindre 10^8 cycles. Après le test, nous observons une dégradation de la fenêtre de programmation, dégradation qui touche à la fois l'état RESET et l'états SET. Lorsque la température de fonctionnement est augmentée (toujours selon les mêmes conditions d'impulsions) on observe une augmentation de la cyclabilité des cellules. La Figure 8 montre un exemple des tests d'endurance effectués à 25 °C et à 85 °C . Les cellules atteignent 2×10^8 cycles à température ambiante, et 10^9 cycles à 85 °C. En effet, ce résultat confirme que avec l'augmentation de la température, la diminution de la tension de seuil réduit le stress thermique dans la cellule lors de l'opération SET. Ces résultats ont été démontrés aussi à l'aide de simulations en utilisant l'approche numérique «Level Set» pour modéliser la cinétique de cristallisation.

Analyse de la dérive de la résistivité

L'augmentation de la résistivité de la phase amorphe dans le temps («drift»), a une incidence sur la stabilité finale de l'état programmé de la cellule, ce qui rend la fenêtre de la résistance du dispositif dépendent du temps. Si la phase cristalline ne connaît pas ce problème, ce phénomène ne représente pas un problème pour un dispositif : même si l'état RESET dérive vers des valeurs de résistance plus élevés, l'état SET est stable, et un seuil de résistance pour distinguer les deux états peut être trouvé. Cela est vrai si on considère une phase cristalline uniforme, sans défauts dans la matrice. Puisque nous cristallisons la cellule par des impulsions très rapides, le matériau présente une matrice polycristalline et, dans certains matériaux comme le GST, la structure cristalline a une forte concentration de défauts (20%). Cela signifie que le phénomène du «drift» peut également affecter l'état SET. En outre, plus la résistance de la cellule est élevé, plus

le coefficient de dérive ν est élevé, où ν est calculé selon l'équation :

$$R = R_0 \left(\frac{t}{t_0} \right)^\nu \quad (5)$$

Par conséquent, le problème de la dérive de résistance devient préjudiciable dans des applications multiniveaux, où la cellule est programmée dans des états de résistance intermédiaires.

L'étude du phénomène du «drift» a été effectuée sur nos cellules « μ trench» afin de comprendre l'impact de la taille des dimensions de la tranchée sur la stabilité de la phase amorphe. Le paramètre de dérive ν a été extrait à partir des données, pour chaque température de fonctionnement (entre 25 °C et 150 °C), en utilisant la loi empirique de puissance (eq. 5). Le coefficient de dérive augmente linéairement lorsque la température augmente, en commençant à diminuer à 150 °C probablement à cause du processus de cristallisation. Nous avons pas observé une différence dans le comportement du «drift», entre les dispositifs avec des largeurs différentes de la tranchée. Ceci suggère que la distribution des pièges sur la largeur de la tranchée est uniforme et la relaxation structurale du matériaux amorphe affecte localement la résistivité du matériau.

Mesures de rétention des données

Un des principaux problèmes de la technologie PCM est la rétention de l'état RESET à des températures élevées. C'est la raison pour laquelle ce problème a été étudiée largement dans les dernières années. Le volume du matériau à changement de phase amorphisé, puisque dans une phase métastable, connaît une recristallisation progressive activé par la température. Par conséquent, la résistance du dispositif diminue jusqu'à la dégradation finale du bit stocké. Une fois intégré dans le dispositif final, la stabilité thermique du matériau à changement de phase commence à être affecté par les interfaces environnantes, les impuretés, les joints de grains entre la phase amorphe et cristalline, etc. Le temps de défaillance, considéré comme le temps nécessaire à l'échec pour le 50% de la population des dispositifs, a une dépendance de type «Arrhenius» de la température :

$$t_{fail} = t_0 e^{\frac{E_A}{k_B T}} \quad (6)$$

où t_0 est un paramètre d'ajustement, E_A est l'énergie d'activation du processus de défaillance, k_B est la constante de Boltzmann et T la température utilisée pour le test de rétention. Cette équation permet d'extrapoler la température maximale («température de fail») pour garantir 10 ans de rétention pour au moins la moitié de la population, et le temps de «fail» attendu à une température donnée.

Pendant l'étude de nos dispositifs PCM « μ trench», les tests de rétention on démontré que l'énergie d'activation E_A pour le GST est d'environ 2 eV. L'effet de n'avoir pas observé une corrélation avec les dimensions de la tranchée, confirme que la rétention des données dépend seulement de l'épaisseur de la région amorphe générée à l'échelle considérée.

L'outil de simulation

L'objectif principal de nos simulations, était de comprendre les mécanismes physiques à la base de la programmation du dispositif PCM, et corréler les résultats obtenus pendant la caractérisation électrique à l'évolution de la phase du matériau. La réalisation

d'un outil pour simuler le comportement d'un dispositif PCM nécessite le couplage des transitions de phase du matériau à changement de phase avec les propriétés électrothermiques de la mémoire. Nous avons donc réalisé les simulations en utilisant l'approche numérique «Level Set» pour calculer l'évolution de la phase cristalline dans le matériau à changement de phase, combiné à un solveur électrothermique pour calculer le potentiel électrique V et la température T dans la cellule.

Afin de prendre en compte le changement de conductivité observé expérimentalement quand le matériau dépasse la température de fusion, une nouvelle équation a été introduit afin de simuler l'état ON de la cellule. Cette équation permet de prendre en compte les aspects suivants :

- la nature semiconductrice de la phase cristalline à des champs électriques faibles (la conductivité électrique augmente avec l'augmentation de la température) ;
- la saturation du champ électrique, à des densités de courant élevées ;
- la continuité entre les différentes phases, également pour éviter des problèmes de convergence pendant le calcul ;
- une conduction activé par le champ électrique avant la saturation du champ électrique à des densités de courant élevées.

Les simulations effectuées nous ont permis de comprendre l'évolution de la phase du matériau à changement de phase pendant la programmation dans la cellule de mémoire avec des résultats en parfait accord avec les résultats expérimentaux.

Chapitre 3 : L'optimisation de la fiabilité de la mémoire à changement de phase embarquée

Au cours des dernières années, différentes idées ont été proposées pour réduire la taille du dispositif PCM, basées sur nouvelles structures de la cellule de mémoire, pour réduire le courant de programmation. Mais la consommation d'énergie n'est pas le seul problème. Pour surmonter le problème de la rétention de l'information à haute température, une possible solution est l'ingénierie du matériau à changement de phase. D'ici vient notre intérêt pour l'étude de nouveaux matériaux à changement de phase pour surmonter la plupart des limitations en corrélation avec la technologie PCM embarquée, en particulier en adressant les marchés automobile et multiniveaux.

Aujourd'hui, le GST est reconnu comme le matériau chalcogénure de référence. L'un des problèmes les plus pressants du GST, est la température de cristallisation faible (~ 140 °C) qui rend intrinsèquement impossible atteindre une température de «fail» de 85 °C. Dans les dernières décennies, beaucoup d'efforts ont été dédiés à la recherche de nouveaux matériaux et dans l'étude de leurs propriétés. Différentes approches au niveau du matériel sont possibles. Une première approche est basé sur le changement de la stœchiométrie du GST et l'ajout des dopants pour augmenter la stabilité de l'état amorphe. Une autre solution est de changer le matériau à changement de phase, pour des matériaux avec une température de cristallisation plus élevée. Dans notre étude, nous avons considéré les deux approches.

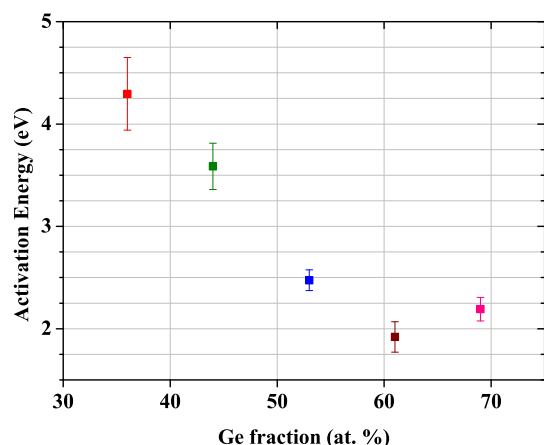


Fig. 9. Les énergies d'activation du processus de cristallisation en fonction de la concentration de Ge.

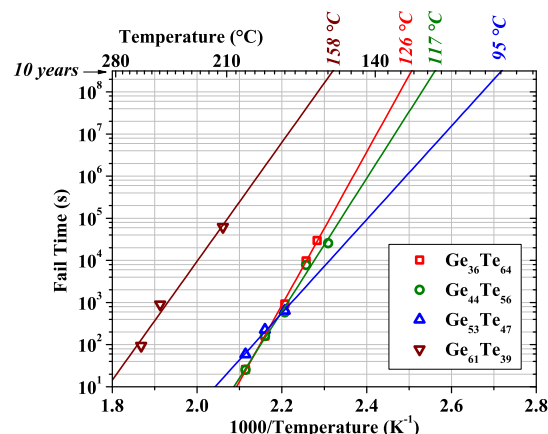


Fig. 10. Extrapolation de type «Arrhenius» à partir de tests de rétention de données effectués sur les dispositifs $\text{Ge}_x\text{Te}_{100-x}$.

$\text{Ge}_x\text{Te}_{100-x}$

Le GeTe est particulièrement intéressant en raison de sa fenêtre de résistivité très élevée (4-5 ordres de grandeur entre l'état amorphe et l'état cristallin). En outre, la vitesse de cristallisation élevée (de l'ordre de la nanoseconde) et la température de cristallisation élevée (~ 180 °C) font du GeTe un bon candidat pour l'intégration dans des dispositifs de mémoire pour répondre aux applications automobiles.

Nous avons commencé à analyser le $\text{Ge}_x\text{Te}_{100-x}$ (où x varie de 36 à 69) intégré dans des dispositifs de mémoire PCM. Nous avons effectué notre analyse sur ces matériaux déposés en couches minces, grâce aux mesures de résistivité en température, les mesures XRD and les cartographies optiques. Ensuite, nous sommes passés à l'évaluation de l'influence de l'enrichissement en Ge et en Te sur les performances des dispositifs (caractéristiques de programmation, cyclabilité et rétention des données).

Par la méthode Kissinger, nous avons calculé les énergies d'activation du processus de cristallisation pour les différentes stœchiométries analysées, représentés dans la Figure 9. Le $\text{Ge}_{36}\text{Te}_{64}$ présente l'énergie d'activation plus élevée. La diminution de l'énergie d'activation de la première cristallisation, lorsque la concentration de Ge diminue, a permis de confirmer que la diminution de liaisons Ge-Te dans le matériau, réduit la stabilité de la phase amorphe. Si l'augmentation de la concentration du Te représente un avantage pour la stabilité thermique de la phase amorphe, en même temps est préjudiciable pour la vitesse de cristallisation. Ce problème, déjà analysé au cours des tests optique qui utilisent un laser pour recristalliser le matériau, a été mis en évidence encore plus une fois que les matériaux à base de $\text{Ge}_x\text{Te}_{100-x}$ ont été intégrés dans nos dispositifs de mémoire. En fait, le GeTe nécessite d'une impulsion électrique de seulement 50 ns pour atteindre la valeur de résistance la plus faible (SET minimum), tandis que le $\text{Ge}_{36}\text{Te}_{64}$ nécessite d'une impulsion de plus de 15 μs .

La Figure 10 montre les résultats des tests de rétention effectués sur le dispositif à base de $\text{Ge}_x\text{Te}_{100-x}$. La température de «fail» extrapolée pour atteindre un temps de rétention de dix années montre l'amélioration attendue en augmentant la concentration du Te. Même si le $\text{Ge}_{61}\text{Te}_{39}$ montre une très bonne rétention à haute température, ce matériau est affecté par la ségrégation du Ge pendant le cyclage de la cellule.

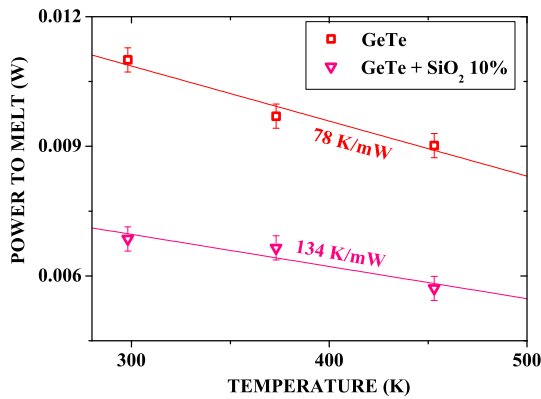


Fig. 11. Résistance thermique (R_{th}) calculée pour les dispositifs à base de GeTe et GeTe dopé avec 10% de SiO₂. L'introduction de SiO₂ augmente la résistance thermique des dispositifs et fournit un meilleur confinement thermique.

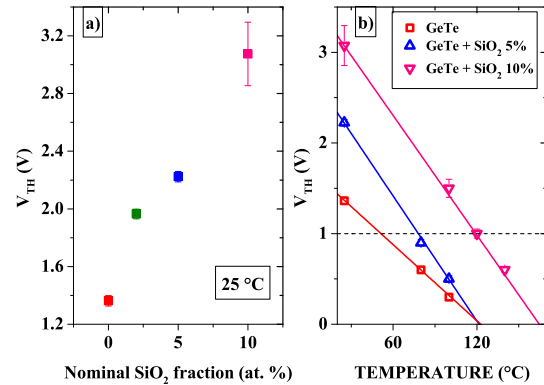


Fig. 12. a) Voltage de seuil V_{TH} en fonction du pourcentage de SiO₂ à température ambiante. b) Tendence de V_{TH} en température, pour différents pourcentage de SiO₂. Le dopage augmente l'immunité de l'état RESET à des tensions de lecture classiques à températures de fonctionnement plus élevées.

Une conclusion très important de cet étude est que la stabilité thermique et la vitesse de programmation (dans l'état SET), sont fortement corrélés. Pour cette raison, il est essentiel de trouver un compromis entre les deux performances, en fonction du type d'application adressé.

Cellules PCM dopées avec SiO₂

L'effet des inclusions de SiO₂ dans le GST, reporté dans la littérature, a montré la possibilité de réduire la conductivité thermique du matériau à changement de phase, avec la réduction conséquente de la puissance de programmation. Nous avons commencé à analyser les effets du dopage SiO₂ dans nos dispositifs basés sur GeTe, pour améliorer les performances électriques de nos dispositifs.

Nos mesures ont démontré une réduction de 50% de la puissance pendant le RESET de la cellule. Cette réduction a été attribuée à une meilleure efficacité thermique des cellules, plutôt qu'à une diminution de la température de fusion du GeTe avec des inclusions de SiO₂. Dans la Figure 11 on observe le calcul de la résistance thermique (R_{th}) pour les dispositifs dopés avec 0% et 10% de SiO₂, obtenu à partir de la caractérisation électrique des cellules à des températures élevées (jusqu'à 180 °C). L'interpolation des données montre clairement une augmentation de 72% de la résistance thermique des cellules avec 10% de SiO₂ par rapport au GeTe.

La Figure 12 montre la variation de V_{TH} en fonction du pourcentage de SiO₂ et de la température. Le GeTe n'est pas en mesure de supporter un voltage de lecture de 1 V à plus de 60 °C alors que les températures de fonctionnement commerciaux vont jusqu'à 70 °C. D'autre part, grâce à l'augmentation de V_{TH} avec le dopage SiO₂ nous montrons que le GeTe-SiO₂ est capable de supporter un voltage de lecture de 1 V jusqu'à 120 °C. Le changement dans la dynamique de nucléation obtenus par l'inclusion de SiO₂ dans le matériau, révèle avec ces résultats sa contribution à l'augmentation de la tension de seuil. Ces résultats ouvrent la possibilité pour le GeTe, d'être intégré

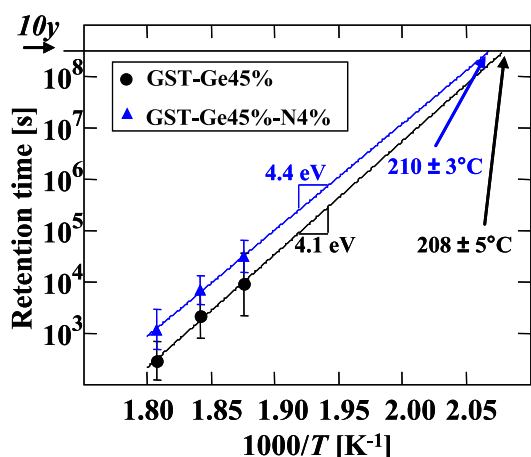


Fig. 13. Extrapolation de type «Arrhenius» du temps de rétention des données pour le GST-Ge45% sans et avec dopage à l'azote.

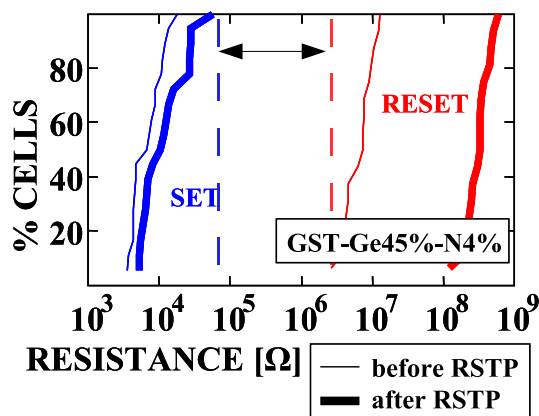


Fig. 14. Test de soudage par refusion appliqué à l'état RESET et SET (obtenus avec notre méthode R-SET) de dispositifs à base de GST-Ge45%-N4%. Dans le pire des cas, une fenêtre de plus d'un ordre de grandeur est conservée après le test.

dans des dispositifs de mémoire pour application à haute température.

Matériaux à changement de phase enrichis en Ge

Au cours des dernières années, l'objectif de rendre la technologie PCM valable pour les marchés automobile et industriel embarqués a poussé la recherche pour explorer des matériaux innovants à changement de phase afin de remédier à l'instabilité de la phase amorphe à haute température. Dans ce contexte, nous avons étudié l'impact du enrichissement en Ge couplé au dopage à l'azote ou au carbone dans le GST. Nous avons intégré le GST enrichi en Ge dans des dispositifs PCM à l'état de l'art pour tester la rétention des données à haute température. L'enrichissement en Ge augmente la stabilité de l'état RESET, même améliorée dans les dispositifs dopés N. En fait, nous avons constaté que le GST-Ge45%-N4% permet un temps de rétention de 10 ans à $210^\circ C$ (Figure 13). Ce résultat est parmi les meilleurs décrits dans la littérature. Nous avons souligné, comment le dopage au carbone améliore la stabilité de l'état RESET jusqu'à $280^\circ C$, mais il réduit considérablement la vitesse de cristallisation et la fenêtre de programmation des cellules. Si ces matériaux innovants sont capables d'excellentes performances de stabilité à haute température, ils ont révélé une dérive accentuée («drift») de la résistance dans le temps de l'état SET, vers des valeurs de résistance plus élevés. Nous avons analysé pour la première fois ce phénomène qui peut représenter un problème pour l'intégrité des données quand il est activé en température pendant le procédé de soudage par refusion de la mémoire (pendant lequel, la mémoire est soumise à un pic de température de $260^\circ C$). Nous avons conçu alors une procédure de programmation optimisée appelée «R-SET», qui permet d'obtenir une valeur de SET valide, avec un faible coefficient de «drift», et avec des temps de programmation conformes aux standards industriels (< 800 ns). Nous avons démontré la possibilité pour nos matériaux de passer avec succès les tests de soudage par refusion, où l'état SET a

été obtenu avec notre méthode «R-SET» (Figure 14). En outre, nous avons proposé le GST-Ge45%-N4%, comme la composition qui représente le meilleur compromis entre les performances de stabilité thermique, fenêtre de résistance, vitesse et dérive de l'état SET. Avec ce résultat, nous avons prouvé la pertinence de la technologie PCM pour les applications embarquées.

Conclusions et perspectives

Les mémoires non-volatiles embarquées sont devenues une composante majeure de beaucoup de systèmes modernes. Dans les unités décentralisées et mobiles, ils permettent un contrôle autonome et la gestion d'une quantité croissante de données. L'un des marchés avec les spécifications les plus strictes est le marché automobile, qui exige la fonctionnalité à températures de -40 °C jusqu'à plus de 150 °C. En outre, les applications mobiles demandent de plus en plus la réduction de la consommation. Même si les mémoires Flash continueront à être développées, les mémoires PCM ont déjà démontré la possibilité de les remplacer dans plusieurs domaines, grâce à leur non-volatilité, scalabilité, "bit-alterability", grande vitesse de lecture et d'écriture, et cyclabilité élevée.

De nombreux efforts ont été faits dans les dernières années pour améliorer la stabilité thermique de la cellule de PCM. En effet, le principal problème de la fiabilité de cette technologie est la forte incidence de la température sur les performances du dispositif. Le travail présenté, commencé à partir de ce contexte, a abordé la compréhension des origines de la défaillance du dispositif PCM, avec l'objectif principal d'optimiser la cellule de mémoire et ouvrir la voie à l'accomplissement des exigences du marché embarqués.

Nous avons commencé avec l'analyse du GeTe, et nous avons montré comme l'augmentation du Te peut augmenter la stabilité thermique des dispositifs. Cependant, la diminution de la vitesse de cristallisation induite l'enrichissement en Te, oblige à trouver un compromis entre la rétention des données à haute température, et la vitesse de programmation. En outre, nous avons présenté les avantages des inclusions de SiO₂ dans le GeTe, en démontrant comme les inclusions de SiO₂ peuvent réduire les défauts causés par la tension de lecture à températures de fonctionnement élevées et peuvent aussi augmenter l'efficacité thermique de la cellule, avec une réduction significative de la puissance de programmation de 50%.

Enfin, nous avons étudié l'enrichissement en Ge du GST, combiné avec le dopage à l'azote et au carbone. La température obtenue de 210 °C pour 10 ans de rétention, est parmi les meilleurs résultats dans la littérature. En outre, nous avons abordé pour la première fois le problème de la stabilité de l'état SET dans ces matériaux innovants, en révélant un phénomène significatif de dérive de la résistance de l'état SET. Avec la mise à point d'une nouvelle technique de programmation, nous avons démontré la possibilité d'améliorer la vitesse de programmation, très réduite par l'enrichissement en Ge, et de réduire le phénomène de dérive. De plus, nous avons montré comment cette solution assure le passage du test de soudage par refusion.

Nous avons proposé une nouvelle structure PCM, qui au moment de la rédaction de cet ouvrage, n'a pas encore terminé son parcours de fabrication. Les investigations sur les origines physiques de la réduction de la dérive de la résistance dans l'état SET par effet de notre technique de programmation, ont été commencées. En outre, un

démonstrateur de 12 Mb basé sur notre GST enrichi en Ge est en cours de fabrication. Une étude détaillée du produit final, permettra de confirmer nos résultats. Celles-ci, représentent les perspectives de notre travail.

La technologie PCM, après 10 ans de développement, a commencé à entrer sur le marché comme remplacement de la mémoire Flash. Des premiers démonstrateurs embarqués ont été présentés par STMicroelectronics et IBM, en montrant l'intérêt croissant de différents concurrents pour cette technologie de différents concurrents, et la compatibilité avec les procédés industriels de la technologie CMOS standard. Au cours de l'avancement de nos travaux, la technologie PCM a traversé l'état de dispositif innovant, et a commencé à être considéré comme un véritable concurrent sur le marché des mémoires non-volatiles, et une référence de comparaison pour les autres technologies de mémoire. Nous croyons que, dans un avenir proche, aussi grâce à notre travail, ses capacités uniques seront exploitées dans différentes applications dans les systèmes électroniques embarqués.