Addition of Ge to the H-Si-C chemical system during SiC epitaxy

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To my dear father

"الى أبي "

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Abstract

In this work, addition of GeH_4 gas to the classical SiH_4+C_3H_8 precursor system is reported for the epitaxial growth of SiC by chemical vapor deposition. The main objective of this fundamental study is to explore the influence of Ge presence within SiC lattice or at its surface on the overall growth mechanism and the grown layer quality and properties.

Epitaxial growth was performed either on high off axis (8 and 4°) or low off-axis (1° and on-axis) 4H-SiC substrate in the temperature range 1450-1600°C. On high off-axis seeds, we discussed the impact of Ge atoms on the homoepitaxial layer quality from surface morphological and structural point of view. Ge incorporation mechanism in these layers as a function of growth parameters was also investigated. The Ge incorporation can be controlled from $1x10^{16}$ - $7x10^{18}$ at.cm^{-3}. Moreover, a clear link between n-type doping and Ge incorporation was found. Electrical characterizations of these layers show an improvement of electron mobility and conductivity of 4H-SiC material while the performances of Schottky contacts were not negatively impacted.

On low off-axis seeds, GeH_4 was added to the gas phase only during the surface preparation step, i.e. before starting the SiC growth. It was found that there is a conditions window (temperature and GeH_4 flux) for which heteroepitaxial 3C-SiC twin free layers can be grown. Interpretation of the results allowed proposing a mechanism leading to twin boundary elimination. It involves a transient homoepitaxial growth step, favored by the presence of liquid Ge at the surface, followed by 3C nucleation when large terraces are formed by step faceting. Electrical characteristics of the twin free 3C-SiC layers were studied using conductive atomic force microscopy (c-AFM).

Keywords. 4H-SiC**,** homoepiataxy, GeH_4, Ge incorporation, growth mechanism, doping, 3C-SiC heteroepitaxy

Résumé

Ce travail concerne l'ajout de GeH_4 au système de précurseurs gazeux classique SiH_4+C_3H_8 pour la croissance épitaxiale de SiC par dépôt chimique en phase vapeur. L'objectif principal était d'explorer l'influence de la présence de l'élément Ge (impureté isoélectronique à SiC), dans la matrice SiC ou à sa surface, sur les mécanismes de croissance et sur la qualité et les propriétés des couches minces déposées.

La croissance épitaxiale a été réalisée dans la gamme de température 1450-1600°C sur des substrats 4H-SiC(0001) désorientés fortement (4° et 8°) ou faiblement (0° et 1°). Sur les germes désorientés, nous avons exploré l'impact des atomes de Ge sur la qualité des couches homoépitaxiales, d'un point de vue morphologique et structural. Les mécanismes d'incorporation de cette impureté ont été étudiés en fonctions des paramètres de croissance. Il a été montré que l'incorporation de cet élément peut être contrôlée dans la gamme $1x10^{16}$ - $7x10^{18}$ $at.cm^{-3}$. De plus, cette incorporation de Ge s'accompagne d'une augmentation du dopage de type n. Les caractérisations électriques de ces couches montrent une amélioration de la mobilité et de la conductivité électrique du matériau 4H-SiC sans aucun impact négatif sur les caractéristiques de contact Schottky.

Sur les substrats faiblement désorientés, GeH_4 a été ajouté à la phase gazeuse uniquement pendant l'étape de préparation de la surface, c'est-à-dire avant d'initier la croissance de SiC. Il a été montré que des couches hétéroépitaxiales de 3C-SiC exemptes de macles peuvent être déposées dans une fenêtre de conditions expérimentales (température et flux de GeH_4). Un mécanisme permettant l'élimination des macles a été proposé. Il implique une étape transitoire de croissance homoépitaxiale, favorisée par la présence de Ge liquide à la surface, suivie de la nucléation de 3C-SiC sur les larges terrasses résultant du facettage des marches. Ces couches de 3C-SiC ont été caractérisées électriquement par microscopie à force atomique en mode conduction.

Mots clés. 4H-SiC, 3C-SiC, Homoépitaxie, Hétéroépitaxie, GeH_4, Incorporation de Ge, Mécanisme de croissance

General Introduction

Electronics as we know would not exist without semiconductor devices. Semiconductors are an integral component of many products in our daily life. Since 1950's, the semiconductor technology has grown tremendously. As perceivable from the word "semiconductors" these are the materials having intermediate electrical conductivity between metals and insulators.

Ever since the beginning of microelectronic era, Silicon (Si) has been the primary semiconductor material. The main advantage of Si is that its growth process and material characteristics are known in-depth. Nonetheless, in the last decade, the demands on electronic devices are rapidly changing from low-power to high-power and low-speed to high-speed with their compatibility in very harsh environments like high temperature, high pressure and corrosive ambient. This is not accessible with the physical properties of Si. The physical properties of wide bandgap semiconductor materials like Silicon Carbide (SiC), Gallium Nitride (GaN) and diamond can certainly afford the current and near future demands in electronic applications.

SiC possesses many superior electrical properties that make it very attractive for power devices especially at high voltages and high temperature. In the recent years, significant material advances such as the availability of large diameter (up to 6'' at R&D level) SiC substrates from different suppliers or the growth of epitaxial layers with high purity and low defect density have opened the way for the fabrication of electronic devices with steadily improving performances. As a matter of fact, SiC market is growing year after year while these devices are entering little by little our daily life.

But SiC technology is now victim of its success and industry is now asking more and more from the fabricated devices. The demand is thus pushing towards the actual limit of device performances which are restrained by several factors. Among these limiting factors are the electronic properties of the actual devices, such as electron mobility, carrier lifetime or SiO_2/SiC interface traps. At the present time, post-

epitaxial growth processes are used for improving these properties but one would prefer an in-situ process during epitaxy for obvious time and cost saving.

Intentionally incorporating impurities into 4H-SiC epitaxial layers is a possible way of modifying the properties of the grown material. But unless the effect of this impurity is known from previous experimental works, each element requires a fundamental study. This is usually performed using ion implantation because much easier to implement and thus to make a rapid screening of impurities. But it is always accompanied by the formation of crystalline defects due to the implantation process itself and the impurity incorporation is limited to several hundreds of nm in depth. Incorporation of the studied impurity during epitaxial growth would be preferable but the experimental work is much heavier. That is why the targeted impurity must be well chosen.

In this work, we have selected Ge element as an isolectronic impurity to be incorporated into SiC material during epitaxy. Previous work on ion implantation is suggesting improvement of the electronic properties of 4H-SiC after implantation and annealing [i]. But, to the best of our knowledge, no experimental work was done before on in-situ incorporation of Ge into 4H-SiC during epitaxy. This is the main goal of the present study which will target several fundamental aspects, from growth mechanism to impurity incorporation and properties of the grown material. Especially, effect of this impurity on 3C-SiC polytype nucleation and growth will be also studied.

This work was done within European RTN network called NetFISiC (Network on Functional Interfaces for Silicon Carbide). It is composed of 12 partners (3 of them from industry) originating from 7 different countries in Europe. The main scientific objective of this Network is to provide Silicon carbide material (of various polytypes) with improved and adequate functional interfaces for getting a step forward in electronic devices performance. In the framework of NetFISiC, the Ge incorporated layers from the present work were analyzed using various techniques. It allowed having an efficient and accurate feedback to the growth from characterization and device specialists and thus contributed positively to the harvesting and interpretation of the results presented in this work.

The present thesis is organized in four chapters. It starts in Chapter I with an overview of SiC material, its properties and the main mechanism and challenges in 4H-SiC and 3C-SiC epitaxy.

In Chapter II, the main characterization tools used to analyze the grown layers will be briefly described. Additionally, a detailed description of the chemical vapor deposition (CVD) apparatus is presented.

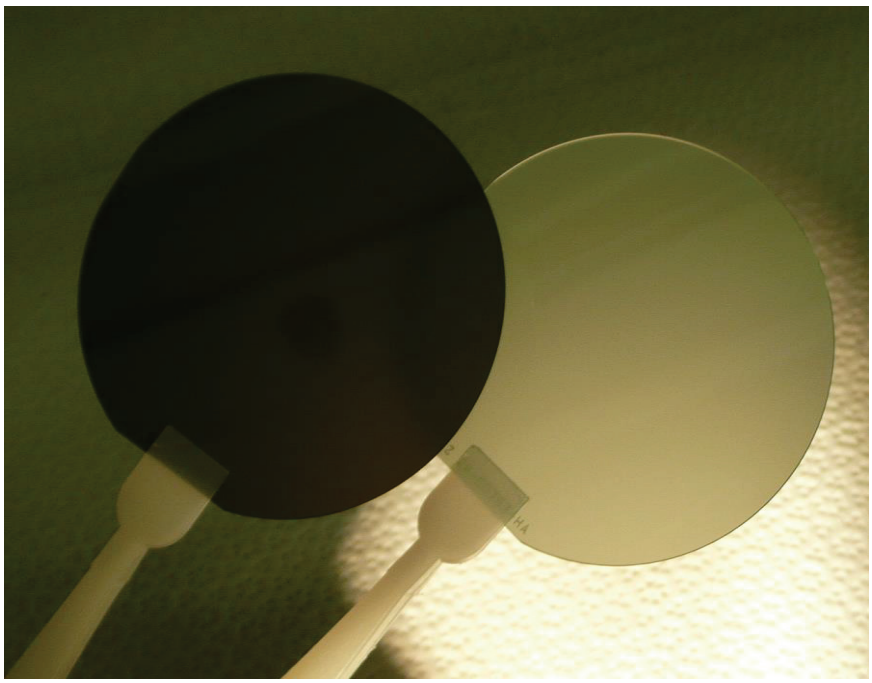
In Chapter III, the growth procedure for Ge incorporation during 4H-SiC epitaxial layers by CVD is presented. Its main impact on layers morphology and its incorporation mechanisms are described and discussed. At last, the influence of Ge incorporation on layers' optical and electronic properties is studied.

In chapter IV, the effect of a Ge-based surface treatment before growth is shown to lead to twin boundary elimination during 3C-SiC heteroepitaxy on α-SiC substrates. The mechanism leading to such results is described and discussed. Finally, the grown twin free layers are characterized by electrical means to access their quality.

[i] G. Katulka, C. Guedj, J. Kolodzey, R.G. Wilson, C. Swann, M. W. Tsao, J. Rabolt, Applied physics letters, **74-4** (1999) 540-542.

Chapter I

Silicon Carbide is await for something new



Chapter I: Contents

Chapter I: Silicon Carbide in await for something new

In this chapter, firstly, the historical background, material properties and applications of Silicon Carbide (SiC) are given. Then, the growth mechanisms and techniques commonly realized for the epitaxy of SiC are specified. After that, the challenges in the 4H homoepitaxial growth and 3C heteroepitaxy on different substrates are reviewed. Finally, the motivation of our work is set after a literature recall of the work related to Ge in SiC or Ge with SiC growth system.

I.1 Need for new electronic materials

The growth of semiconductors has always been one of the most important steps towards the development of any electronic device. Si, GaAs and Ge are well known semiconductors for electronic applications. They established the modern day electronic devices after over 50 years of research and development. However, they still cannot be implemented in certain extreme applications; like military (equipment and vehicles), space equipment and automobiles, due to their limited properties such as thermal conductivity, breakdown voltage and saturated electron drift velocity. For example, the maximum switching speed of silicon devices is 3 GHz, which is being used in modern computers. Another reason overdue searching for a new semiconductor is the aim to reduce system size and complexity and thus limit the amount of required cooling. Simply, what is needed is a semiconductor that can be easily incorporated into systems and circuits giving enhanced electrical and physical properties. SiC's wide band gap, coupled with the high break down field, high thermal conductivity, and high electron mobility has made it an excellent candidate that can be applied in various applications (high temperature and high power electronic device applications). The usefulness of SiC has grown beyond power electronics applications and is being developed for use in gas sensing and other novel applications directly related to the development of supporting technologies. While there are many challenges to overcome, epitaxy of SiC is no longer in the infancy stage.

The progress of SiC technology is, however, slowed down by various aspects, some of them related to the material itself such as the defect density of the substrate or other concerning material processing steps necessary for full-scale production. Although mankind has known about SiC for over 100 years, its recent expansion into the market place has made it an increasingly interesting research material within the past 20-25 years. Despite the defect density problems, commercial substrates are commonly available in 2″, 3″, 4″ and soon 6″ diameter. The status of SiC is still generally considered to be an emerging material with great potential. It is also used as a substrate to grow GaN for high efficiency, high brightness LEDs. A lot of work and effort is to be spent in SiC field to make it the leading material for the upcoming years.

I.2 Overview on SiC

I.2.1 History

The observation of silicon carbide started in 1824 by the Swedish scientist J. J. Berzelius who observed it during his attempts to synthesize diamond [I.1]. He speculated that there was a chemical bond between Si and C in one of his samples. Likewise, SiC can sometimes occur in nature. A Nobel Prize winning chemist Dr. H Moissan discovered it as hexagonal platelets at the Arizona meteorite [I.2]. At the beginning he falsely defined these crystals as diamond before characterizing and confirming them as silicon carbide. So, the mineral form of silicon carbide was named Moissanite in his honor. Nowadays, Moissanite is the name of commercial gemstone made from SiC. In 1891, E. G. Acheson carried out the first synthesis of crystalline SiC inside an electric melting furnace, which was primarily invented to produce suitable minerals that could substitute diamond as abrasive and cutting material. He heated a mixture of coal, sandstone (with a very high SiO_2 content) and NaCl. The crystalline products Acheson found after the process were characterized by a great hardness, refractability and infusibility [I.3]. The discovery had a considerable impact and much material was produced using this process.

Since the discovery of SiC, the polycrystalline form has been used in high temperature, harsh environment, and high-strength and abrasion resistant applications. But the crystal quality was not sufficient to focus on its semiconducting properties till

1950s. In 1955, J. A. Lely developed a process for producing the pure SiC single crystals with high quality [I.4]. This method, commonly referred as the "Lely method", was further improved by Hamilton [I.5] and Novikov [I.6] since the yield of the process was low, the sizes of the platelets irregular and no real control of the polytypism existed. In 1959 the first SiC conference was held in Boston. Apart from the lead of Si technology during 1960s and 1970s, the work on SiC was mainly focused on basic solid-state physics and material growth. In 1978, Tairov presented the seeded sublimation growth technique to grow SiC bulk crystals [I.7], This was the milestone of current SiC technology. And in the early 1980s, Nishino et al [I.8] made it possible to grow cubic single crystalline SiC on silicon substrates. Cree Research, Inc., produced the first commercial SiC wafers in 1991 [I.9 - I.11]. The availability of SiC wafers in recent years has spurred extensive research on epitaxial growth. Matsunami group's [I.12, I.13] mastery of step-controlled epitaxy is a notable development in optimizing SiC epitaxial growth morphology.

The main purpose of all new technologies is to reduce the cost that remained as the limiting factor on marketing the devices. Silicon carbide has been employed as a semiconductor material for more than 25 years in the production of blue and green LEDs by several companies especially Cree. In the last few years, the defect density has been reduced to a level low enough to allow the fabrication of large area power devices with an acceptable yield. Simultaneously, material costs are reducing and a realistic competition with silicon power devices is growing [I.14]. As a result, several companies in the U.S., Japan, Europe, and Russia have started producing SiC wafers commercially which results in a huge progress in their diameter (Figure I.1).

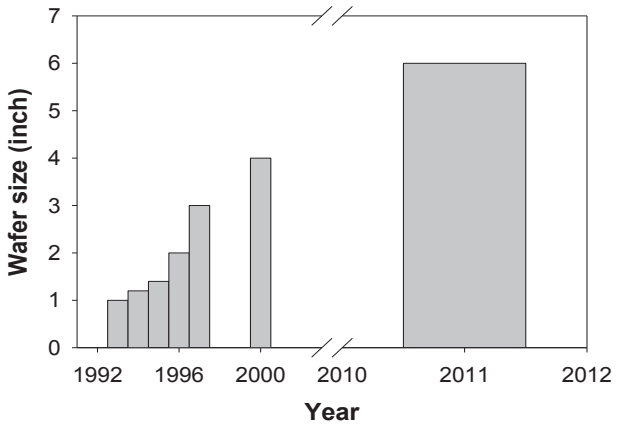


Figure I.1: Progress of SiC wafer diameter demonstrators. These diameters were commercially available few years after

I.2.2 Crystalline structure

SiC has equal parts silicon and carbon, both of which are group IV elements. It is the only stable compound composed of only carbon and silicon and each element is tetrahedrally bonded as shown in Figure I.2. The distance between neighboring silicon or carbon atoms is approximately 3.08 Å. The Si-C bond is nearly covalent (88 %), with an ionic contribution of 12 % having sp^3 hybridization. SiC exhibits short (1.89 Å) and very strong (289 $kJ.mol^{-1}$) bonding which marks it as a very hard material. Therefore, carbon atom is located at the center of mass of the tetragonal structure outlined by the four neighboring Si atoms and vice versa.

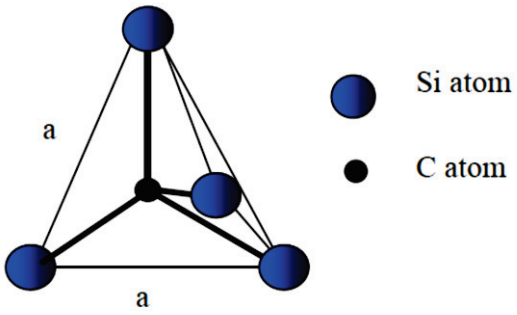


Figure I.2: The tetragonal bonding of a carbon with the four nearest silicon atoms

Single crystalline silicon carbide occurs in many different crystal structures, called polytypes. More than 200 polytypes of SiC have been identified. They are classified into three basic crystallographic structures, cubic (C), hexagonal (H) and rhombohedral (R) [I.15]. Only few of them, are stable enough and thus of technological interest [I.16]. Their stacking sequences are presented in Figure I.3 using Ramsdell notations [I.17].

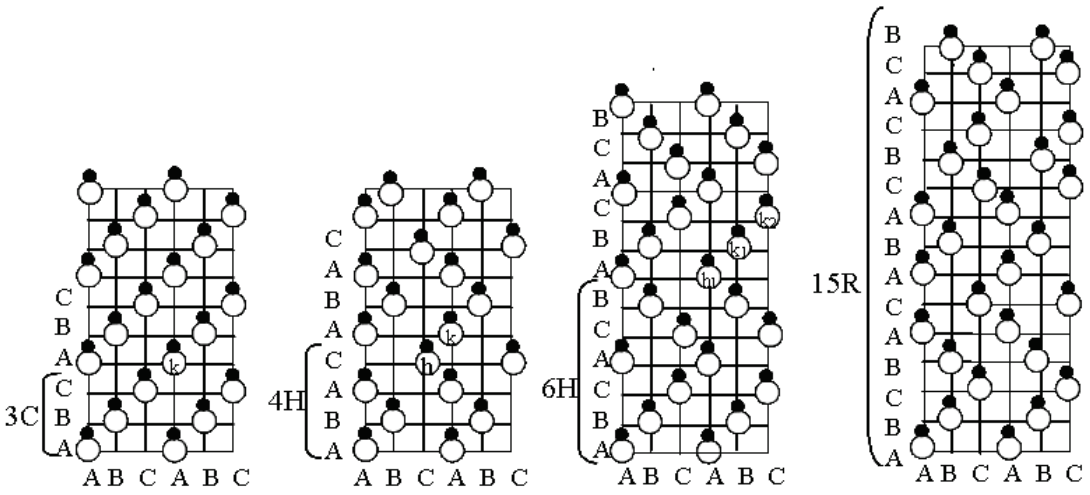


Figure I.3: The crystalline structure of the most common SiC polytypes

The most common polytypes in this notation are called 3C-, 4H-, 6H- and 15R-SiC where the digits represent the number of Si-C bilayers in the unit cell and the letters represent the crystal structure. 3C-SiC is the only cubic structure, also referred as β-SiC, while the others are referred as α-SiC. Each polytype can be considered as a repeated stacking sequence of Si-C bilayers along the c-axis. The bilayer is composed of a Si and a C atom lying exactly on the top of each other. If we consider the first closed packed layer as at position "A", the next bilayer can be placed either at position "B" or "C" and so on … The freedom of every next layer to choose between the two positions gives rise to several polytypes in SiC. The conventional ABC notations of the stacking sequences of 3C, 4H, 6H and 15R along with other physical parameters are given in the Table I.1.

It is also possible to determine the "hexagonality" of a SiC polytype, which is the percentage of the hexagonal sites of a whole crystal. Since 3C-SiC has only cubic sites, the hexagonality is obviously zero, whereas for 2H is 100%. In mixed-structure polytypes, the hexagonality varies between these two extremes, see Table I.1.

Table I.1: Stacking sequance and hexagonality with other physical properties of some SiC polytypes [I.18, I.19]

Polytype (Ramsdell)	Stacking sequence	Lattice parameters		Hexagonality [%]	Atom / unit cell
		a [A]	c[A]		
3C	ABC	4.359	4.3590	0	6
2H	ABAB	3.076	5.048	100	4
4H	ABCB	3.073	10.053	50	8
6H	ABCACB	3.080	15.117	33	12
15R	ABCACBCABACABCB	3.079	37.780	44	30

The SiC crystals are also characterized by their surface termination (or polarity) which is C-rich on one side and Si-rich on the other side (see Figure I.4). These two faces are commonly called C-face and Si-face, respectively. In fact, the two faces have different surface energies; 1.76 x 10^{-4} J.cm^{-2} for Si-face and 0.71 x 10^{-4} J.cm^{-2} for C-face [I.20]. Thus their properties are not the same. For instance, rates of both oxidation [I.21, I.22] and vapor phase epitaxial growth [I.23] are faster on the C-face than on the Si-face.

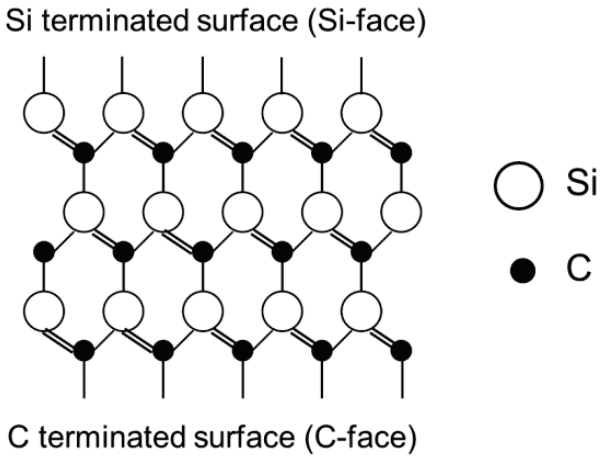


Figure I.4: Representation of the two different faces in the SiC crystal

I.2.3 Electrical and physical properties

SiC is a wide bandgap semiconductor with excellent combination of physical properties which makes it good candidate for high-temperature, high frequencies and high-power switching device applications. It is also among the strongest materials, ranking at least a 9.25 on Mohs scale of hardness (diamond = 10) [I.24]. In addition it is highly resistant to chemical reactions; it is not chemically etched by any acids or bases near room temperature.

The properties of the common SiC polytypes, compared with conventional and other wide bandgap semiconductors are given in Table I.2. Silicon carbide bandgap ranges from 2.3 eV (for 3C) to 3.3 eV (for 2H). It increases almost linearly with hexagonality [I.25]. For instance, 4H-SiC has 3.26 eV bandgap, that is approximately 3X that of silicon, 1.16 eV. The larger bandgap allows an operating temperature that is approximately 3 times that of Si, and over 2 times that of GaAs.

Moreover, SiC has a high saturated electron drift velocity that is over 2 times that of Si and GaAs. The electron drift velocity is defined as the speed at which electrons travel at a given applied potential. Better conductivity, more efficient operation under constant bias, faster frequency switching, and less power loss when switching are constantly associated with this physical property. The more efficient operation and less power loss in switching reduce the power requirements for running these devices and decrease the amount of waste heat created during operation.

Table I.2: Properties of the most stable SiC polytypes compared with other semiconducting materials. E_g is the bandgap at 300 K, vsat saturated electron drift velocity, μe electron mobility, μ h hole mobility, EB break down electric field and α_{therm} thermal conductivity [I.18, I.19, I.26 – I.29]

Semiconductor	E_g [eV]	í$_{sat}$ [10^7 cm.s^{-1}]	μ [cm^2(vs)$^{-1}$]		E_B [10^6 V.cm^{-1}]	á$_{therm}$ [W.(cmK)$^{-1}$]
			μ_e	μ_h		
Si	1.12	1.0	1400	600	0.3	1.45
GaAs	1.43	2.0	8500	400	0.4	0.46
3C-SiC	**2.39**	**2.7**	**1000**	**40**	**1.2**	**3-5**
6H-SiC	3.08	2.0	600	50	2.4	3-5
4H-SiC	**3.26**	**2.7**	**460**	**115**	**4.0**	**3-5**
GaN	3.39	1.5	900	150	5.0	1.30
Diamond	5.45	2.7	2200	1600	10	1.50
AlN	6.20	1.4	1100	-	1.2-1.8	3.50

Another important physical property of SiC is its high thermal conductivity which is almost independent on the polytype, while more dependent on doping type and concentration; the typical value is about 5 times higher than that of Si. High thermal conductivity leads to reduced requirements of cooling systems which lower the overall system volume and cost. The electric field at which SiC breaks down is over 10 times greater than that of both Si and GaAs. In order to increase the resistivity of conventional semiconductors to reach a high blocking voltage, a thick layer with low doping level is required which ultimately increases the power consumption and also enlarges the device size. The use of SiC material should result in small device size and low power consumption with thin and comparatively higher doped layer.

Compared with other wideband gap materials GaN and diamond, 4H-SiC material technology is by far the most mature. Currently, 6-inch 4H-SiC wafers are available from Cree, Inc with zero micropipe density and with crystalline defect densities in the $10^4 – 10^5$ cm^2 range.

I.2.4 Applications

Initial interest in SiC for semiconductor applications resulted from requirements for high temperature, and corrosion resistant materials. Advances in micro device processing in addition to a need for higher operating frequencies, greater power handling capabilities, and increased device packaging densities have spurred the

present developments in SiC material and device technologies. 4H-SiC and 6H-SiC are commercially available semiconductors with great potential for high temperature, high power and high frequency electronic devices. Between 4H- and 6H-SiC, 4H-SiC has substantially higher carrier mobility, shallower dopant ionization energies, and low intrinsic carrier concentration [I.30]. Therefore, the SiC device fabrication efforts have shifted towards 4H-SiC when it has become more readily available.

SiC opens the ability to place uncooled high-temperature semiconductor electronics directly into hot atmospheres (harsh environment). This would be greatly benificial to automotive, aerospace, or the drilling industries [I.31, I.32]. In the case of automotive and aerospace engines, improved electronic telemetry and control from high-temperature engine regions are necessary to more precisely control the combustion process to improve fuel efficiency though reducing polluting emissions. High-temperature capability eliminates performance, reliability, and weight penalties associated with liquid cooling, fans, thermal shielding, and longer wire runs needed to realize similar functionality in engines using conventional silicon semiconductor electronics.

In particular, the high breakdown voltage and high thermal conductivity coupled with high carrier saturation velocity allow SiC microwave devices to handle much higher power densities than their silicon or GaAs RF counterparts, despite SiC's disadvantage in low-field carrier mobility [I.33 – I.35]. So, silicon carbide can be used for fabricating high frequency devices (cellular phones, digital TV, telecommunication systems, and radars). SiC-based microwave transistors are predicted to produce more efficient microwave systems and further expand their existing applications [I.36]. Silicon carbide static induction transistor (SIT) and metal semiconductor field effect transistor (MESFET) have already been developed for these applications. Indeed, silicon carbide SITs are challenging devices for high power applications up to 900 MHz.

The development of GaN materials has replaced in the market the SiC bright blue and green light emitting diodes (LEDs). However, the combination between the two materials (by the use of SiC as a substrate) technologies allows the fabrication of high brightness GaN based LEDs.

I.3 Epitaxial growth of SiC

1.3.1 Epitaxial growth generalities

Bulk silicon carbide substrates grown with seeded sublimation techniques cannot be used directly for the fabrication of power electronic devices. Epitaxial thin film growth is a key process in SiC technology because accurate controlled thickness, conductivity and dopant concentration are required for specific electronic devices.

It is worth noting that epitaxial layer doping and thickness are characteristics depending on the electronic device that will be fabricated. For example, in the case of a power electronic device, a layer with a thickness up to 100 μm and with n-type doping concentrations in the range from 10^{13} to 10^{15} cm^{-3} can be required, while a high frequency device can be fabricated on a layer with few micrometers of thickness and a high doping concentration (up to 10^{19} cm^{-3}) [I.37].

The word epi-taxy come from the Greek words meaning “above” and “order”, which indicate the process of growing a structure above a substrate keeping the same (crystallographic) order of the substrate itself. If the substrate and the epitaxial layer (epilayer) are exactly the same, both in terms of chemical and physical characteristics, the process can be also called homoepitaxial growth. In other words, in homoepitaxy the chemical composition and the lattice parameters of the deposited material match that of the substrate, and the film/substrate interface should vanish into the bulk material so that the interface energy (γ_i) is approximately zero [I.38, I.39]. If substrate and epilayer have a different chemical identity or a different crystallographic structure (i.e. 3C-SiC on 4H-SiC), then the process is called heteroepitaxial growth. The epitaxial film orients itself to minimize γ_i and maximize bonding at the interface [I.39]. If the difference in lattice parameters is too high, epitaxy is very difficult [I.38]. The epitaxial growth modes (or mechanism) on a monocrystalline substrate are presented below.

I.3.1.1 Epitaxial growth mechanisms

The SiC surfaces of the commercially available substrates are composed of steps and terraces, which means that the degree of misorientation is never equal to zero (Figure I.5)

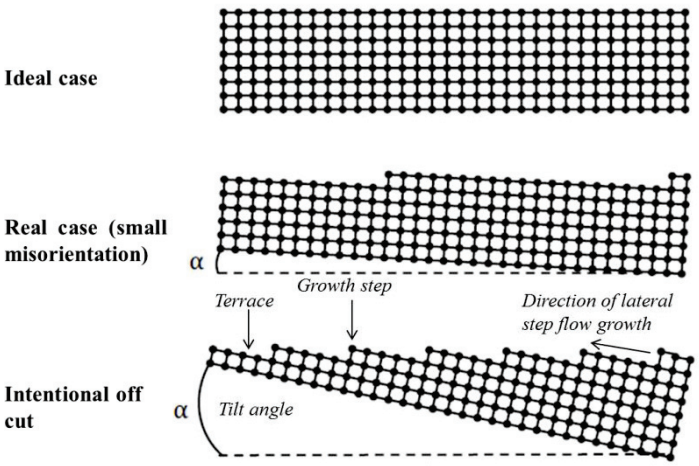


Figure I.5: Illustration of a cross section of perfect on-axis (ideal case), small misorientation (real case) and intentional off-axis crystalline substrate [I.40]

The occurrence of different epitaxial growth modes depends on various parameters of which most important are the thermodynamic driving force and the misfit between substrate and layer. The growth mode characterizes the nucleation and growth process. There is a direct correspondence between the growth mode and the film morphology, which gives the structural properties such as crystalline perfection, flatness and interface abruptness of the layers when appropriate conditions are used. It is determined by the kinetics of the transport and diffusion processes on the surface. The main growth modes during a SiC epitaxy are listed below and illustrated in Figure I.6:

Step-flow: When growth conditions are well controlled and if there is a sufficiently short distance between the steps, Si and C atoms impinging onto the growth surface find their way to steps where they bond and incorporate into the crystal. Thus, ordered lateral "step flow" growth takes place which enables the polytypic stacking sequence of the substrate to be exactly mirrored in the growing epilayer. The main advantage of this growth mechanism is that it hardly generates new defects, though it may propagate the ones present inside the substrate. Also, it implies to have some significant off axis misorientation for sufficient step density at the surface.

2D nucleation: If the adsorbed atom on the surface does not have enough mobility to arrive at the step edges, then 2D nucleation growth takes place by means of atoms aggregation on the terraces forming islands. These islands will act as nuclei for the subsequent growth. When growing on hexagonal low off axis seeds, growth adatoms

will nucleate and bond in the middle of the terraces instead of at the steps, leading to uncontrolled heteroepitaxial growth of poor-quality

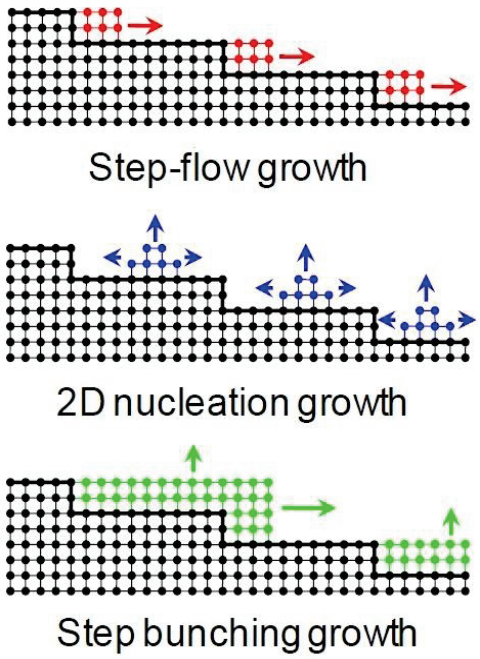


Figure I.6: Systematic representation of the different epitaxial growth mechanism: in red growth by step flow, in green growth by step bunching and in blue the 2D nucleation growth

Step bunching: Step bunching is observed when coalescence of multiple SiC growth steps occurs during epitaxy forming large macro-steps that can exceed thickness of thousands of mono steps. This is generally the case during the epitaxial growth from a liquid phase. Homoepitaxial growth is obtained by this mechanism in the case of SiC.

I.3.1.2 Epitaxial growth techniques

Different techniques have been used for the epitaxial growth of SiC, the main ones to be discussed in the following section are: A) Chemical Vapor Deposition (CVD), B) Liquid Phase Epitaxy (LPE) and C) Vapor-Liquid-Solid mechanism (VLS).

A) CVD

CVD is the current research and industrial standard for SiC epitaxial growth. Epitaxial layers must be uniform with respect to thickness and impurities (dopants) in order to be useful in microelectronic devices. CVD is the only technique that can afford these specifications.

CVD is a process where one or more gaseous species react on a solid surface to give a solid phase material. The several steps that must occur in every CVD process

(Figure I.7) can be simplified as: (1) reactant gases are transported into the reactor in a carrier gas, (2) reactant species diffuse through a boundary layer above the growth surface, (3) the species are transported to the surface via diffusion, (4) a reaction takes place on the surface where one of the products is a deposited solid, (5) gaseous by-products are transported away from the surface, and (6) finally they are diffused away via the boundary layer [I.41]. The rate at which the process proceeds from the initial to the final state will depend on chemical kinetics and fluid dynamic transport. Since the gas flows are continuous, the film thickness will increase over time.

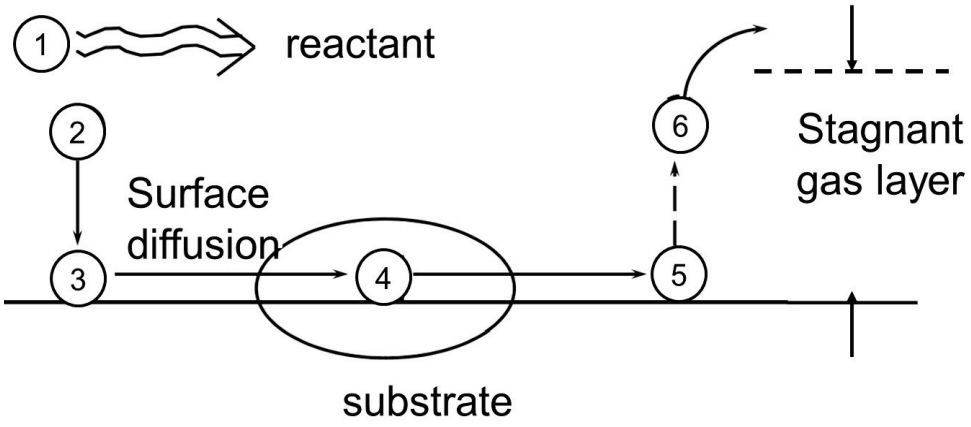


Figure I.7: Schematic illustration of the fundamental steps involved during chemical vapour deposition [I.38]

Several types of CVD systems exist [I.42] including horizontal and vertical reactor orientations, hot-wall and cold-wall, and numerous other variations. The CVD reactor could be operated at atmospheric pressure (AP), or low pressure (LP) and are commonly referred to as APCVD and LPCVD, respectively. SiC LPCVD is typically carried out in the pressure range of 10 – 150 Torr. The reactor geometry is an important parameter in the growth of epitaxial films. Hot-wall and cold-wall refers to the temperature of the walls adjacent to where the reacting gas stream flow. RF heating, is the source that is commonly used in SiC CVD.

Compared to the cold wall reactor, the hot wall type has demonstrated superior results. The grown material is of considerably better morphology and lower background doping. For instance, in hot wall reactor, the background doping can be easily obtained in the low 10^{13} cm^{-3} range and thicknesses greater than 50 µm could be grown fast due to high growth rates. The low thermal gradient [I.43, I.44] and the

backside deposition are not as severe as in the cold-wall reactors thus the lifetime of the susceptors could be noticeably extended.

During CVD, a carrier gas transports the reactants to the surface of the substrate. The carrier gas may also aids the reactions to take place. Typical carrier gases are argon (Ar), helium (He), and hydrogen (H_2); however, H_2 is the most commonly used, especially for SiC CVD [I.45]. Numerous precursors have been used to grow SiC epitaxial films [I.46]. Some of the silicon based precursors include silane (SiH_4) [I.47], disilane (Si_2H_6) [I.48], and silicon tetrachloride ($SiCl_4$) [I.49]. Some of the carbon source precursors that have been reported are acetylene (C_2H_2) [I.47, I.48], propane (C_3H_8), methyl chloride (CH_3Cl), methane (CH_4) [I.50], and carbon tetrachloride (CCl_4). Precursors containing both Si and C have also been investigated such as hexamethyldisilane ($C_6H_{18}Si_2$ or HMDS) methyltrichlorosilane (CH_3SiCl_3 or MTS) [I.51, I.52] and dimethyldichlorosilane ($(CH_3)_2SiCl_2$) [I.53]. In spite of all these options, propane and silane, C_3H_8 and SiH_4, are the most commonly utilized precursors for SiC epitaxial growth.

The history of CVD and SiC started since 1960's when Jennings et al. [I.54] and Campbell and Chu [I.55] reported the CVD growth of SiC. The $SiCl_4$ and CCl_4 were used as precursors. Jennings et al. used a vertical cold wall reactor with the gas inlet at the top and the substrate facing the gas flow. However, Campbell and Chu used a horizontal cold-wall reactor.

In the 1980's, the successful demonstration of 3C-SiC heteroepitaxy on silicon substrate by Nishino et al [I.8] promoted a renewed interest in the field of SiC by CVD. In this pioneer work, a GaAs CVD reactor was redesigned to meet the requirements for the growth of SiC. The cold-wall configuration is achieved by using a double-walled quartz tube with water circulated between the walls. The wafer is placed on an inductively heated graphite susceptor. To ensure the cold-wall conditions, the susceptor is placed on thermal insulation. The capabilities of this reactor configuration were limited in terms of substrate size, temperature uniformity, and growth rate, yet it can be valuable tool for understanding aspects of epitaxial growth. Since then a lot of efforts have been made to improve the reactor design, growth processes and reactor capacity to fulfill the requirements on the quality of the grown layers and to lower the overall cost of the process.

The hot-wall reactor concept was first introduced by Kordina et al. in 1994 [I.56]. This was a horizontal geometry reactor module. Later, the reactor was further improved for highly uniform epitaxial layer growth [I.47]. The susceptor is encircled by thermal insulator which is placed inside an air cooled quartz tube. The thermal insulator reduces the heat loss due to radiation and consequently, hotwall reactors consume less power (20-40 kW) than cold-wall reactors. The thermal insulator also helps maintain thermal uniformity. To date, this reactor geometry is one of the most widely used hot-wall reactor configurations.

Due to these persuasive advantages, the hot-wall reactor has become increasingly popular and is today used by most groups working on SiC. The hot-wall reactor was commercialized by Epigress (now Aixtron) and has gone through significant development. The planetary warm-wall reactor is from the same family of hot wall reactors which has a non-actively heated ceiling (the ceiling is heated through radiation from the susceptor). It is by far the most mutual production tool for thin layers. It is also a multi-wafer type reactor, which gives outstanding uniformity and reproducibility. On account of the success of the hot-wall reactor, a multi-wafer planetary style hot wall reactor was established with an actively heated ceiling. The first results introduced by Wischmeyer et al in 2001 who demonstrated it on a 7 x 2" configuration which gives extremely good thickness and doping uniformity with a thickness and doping uniformity of 0.4% and 6% (sigma/mean), respectively with a wafer to wafer thickness and doping uniformity of 0.6% and 3.6%, respectively [I.57]. A schematic of multi-wafer hot wall CVD reactor is depicted in Figure 1.8.

Though showing outstanding performances, hot wall reactors have also few drawbacks which we must not ignore:

1) Fall of SiC particles from the graphite ceiling are commonly reported and difficult to avoid after several or long growth runs. Hence, the graphite parts have to be cleaned frequently.
2) The graphite heated walls reacts with H_2 and thus brings extra C atoms under the form of CH_x species to the growing surfaces. This extra supply of C is not controlled and it affects the optimal growth conditions (mainly C/Si ratio). That is why hot wall reactors usually work at lower C/Si ratios than cold wall ones. Purity and lifetime of these graphite parts are therefore important issues.

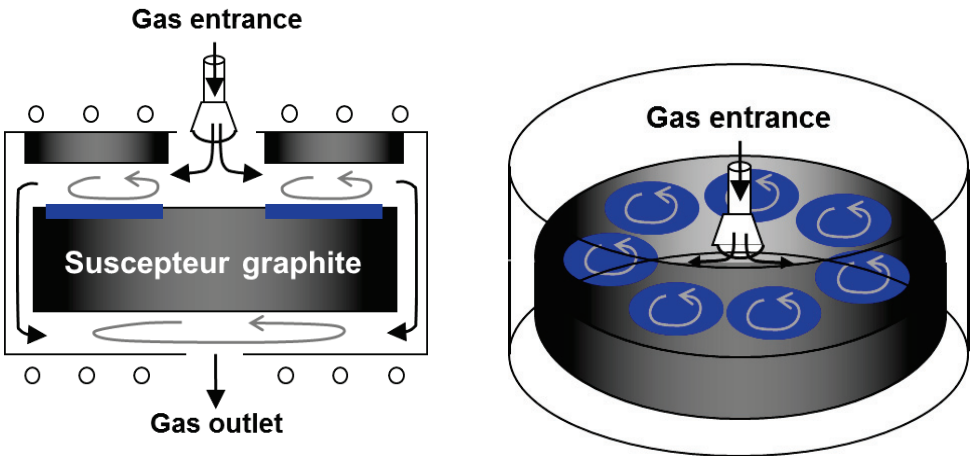


Figure 1.8: 2D (left) and 3D (right) illustration of the multi-wafer CVD geometry

B) LPE

While CVD is currently the preferred method for SiC epitaxial layer growth, the LPE was the first method allowing homoepitaxy of SiC and led to the first fabrication of devices [I.58]. Lately, the ability of LPE to heal the micropipe defect attracted the attention of the crystal growers [I.59]. Usually this growth method uses low temperatures and lower supersaturating conditions at which the micropipes are not energetically favored. Actually, this defect is no more an issue because the new generation of SiC substrates contains only few or even no micropipes.

The epitaxial growth by LPE is mainly carried out using the traveling solvent method (TSM) [I.60, I.61], in contrast to liquid phase bulk growth that primarily utilizes the top seed solution growth (TSSG) method (Figure I.9). In both methods, a temperature gradient is maintained between the source and substrate to facilitate the growth process. While the TSSG system involves only Si-based melt/graphite as the source, the TSM consists of a maintained solvent between a polycrystalline SiC source platelet (often SiC rod) and a substrate.

Growing SiC by LPE using silicon solutions saturated with carbon was studied since several decades and reproducible growth of 100 µm thick layers was shown already at that time [I.64]. Even if the solubility of carbon in liquid silicon ranges from 0.01 % to 19 % in the temperature interval from 1412 °C to 2830 °C, at high

temperatures the significant evaporation of silicon makes the growth process unstable, unless high working pressures are used like 200 bars of Ar for a growth temperature of 2000 °C [I.65].

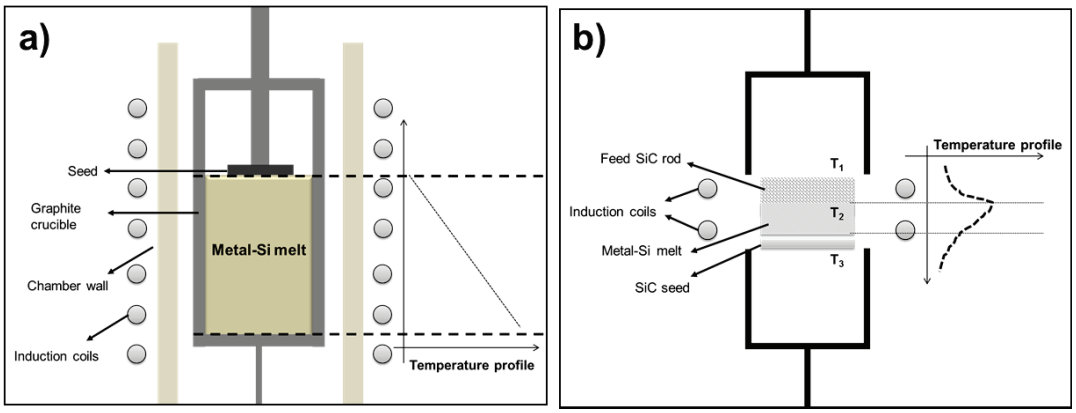


Figure I.9: a) Schematic representation of the TSSG growth reactor [I.62], b) Schematic representation of the traveling solvent method TSM [I.63]

The growth rate of LPE can be as high as 300 µm/h using a special sandwich configuration in LPE [I.60]. Both n and p-type doping can be achieved by selecting proper liquid phase. A key limitation to this method is the inability to switch doping level and conductivity type during the growth [I.66]. Also, it is difficult to achieve low n type doping (always $\geq 10^{18}$ at.cm^{-3}).

C) VLS

The VLS mechanism is well known for 1D crystal growth mechanism that is assisted by a metal catalyst. It results in the creation of whiskers, rods, and wires. 1D crystal growth was initially developed nearly 50 years ago in the Si industry and the mechanism was suggested for wider use by Wagner in 1964 [I.67]. Since the 1970s, the mechanism has been used to grow various types of whiskers from the micrometer to the mm scale. A typical example is SiC whiskers, which are excellent reinforcements for high-strength, high-toughness ceramic or metal composites [I.68]. The 1D growth can be decomposed in four basic steps: (1) transport of the gaseous precursors to the surface of the liquid; (2) cracking of the precursors and dissolution of carbon and silicon in the liquid at the vapor-liquid (VL) interface; (3) transport of Si and C from the VL interface to the liquid-solid (LS) interface; (4) and finally, crystallization of SiC at the LS interface. Some attempts for using such VLS mechanism to achieve epitaxial growth (3D growth) of SiC layers were performed

using silicon containing melt in a crucible. In this specific case, the growth starts with transporting of the only carbon precursor (commonly C_3H_8) to the surface of the liquid (where silicon exists) where precursor dissociation and dissolution of carbon in the silicon melt take place. Then, carbon transport from the vapor-liquid interface to the liquid-solid interface occurs and crystallization of SiC happens. Schematic illustration of the standard VLS used for whiskers and VLS system for the growth of SiC epilayers is shown in Figure I.10.

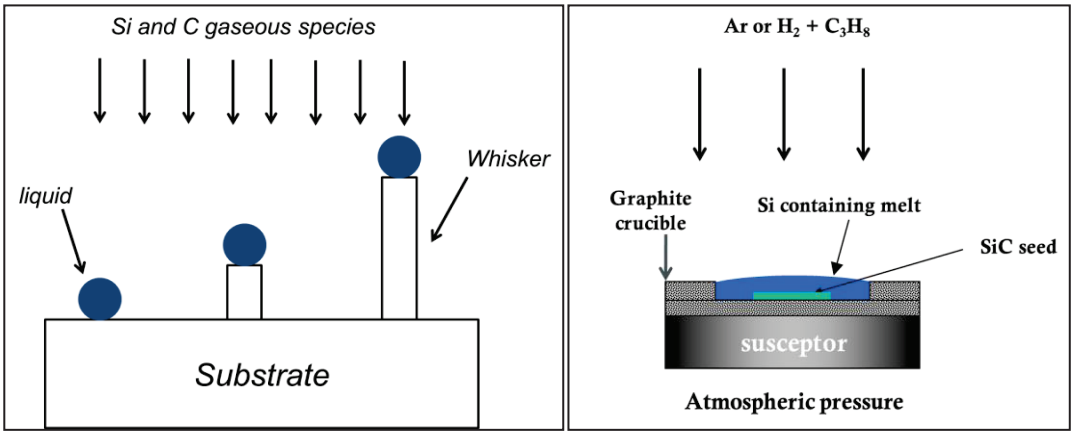


Figure I.10: illustration of the whiskers growth using VLS (left), b) Drawing of the VLS system used by LMI to grow SiC epitaxial layers (right)

There are only very few people who have tried to grow epitaxial layers of SiC using VLS technique [I.69, I.70]. This is probably due to the difficulty of implementation of the process which requires a complete covering of the seed. In addition, the wetting properties of the substrate surface by Si melt and the liquid height on the substrate are crucial for uniform growth rate. The fruitful work was done by our team at the LMI and main results on the 3C growth will be presented later on.

The transition from growth of whiskers to epitaxial thin layers is not obvious since it generates several major difficulties. First of all, due to higher amount of liquid necessary to cover the whole surface of the sample, it is not possible anymore to use pure metal catalyst like for whiskers. Indeed, most of the pure metals have certain reactivity when in contact with SiC substrate. Using metal-Si alloys is then highly recommended to reduce this reactivity, so that there is no need to add Si precursor in the gas phase. In addition, the important height of the liquid in VLS limits greatly the diffusion of the active species so that growth rates are expected to be lower.

Contrarily to LPE conditions, VLS growth (see Figure I.11) can be performed under an inverse temperature gradient, i.e. the temperature is higher at the substrate surface than in the liquid (or the top of the solution), and the requirements on the temperature gradient are not as strict during VLS growth.

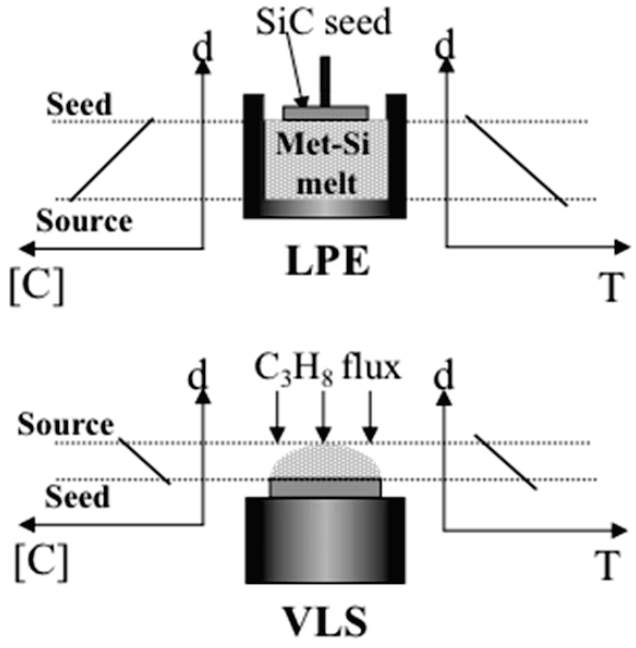


Figure I.11: Comparison between LPE (upper) and VLS (lower) configurations for SiC epitaxy. Left and right graphs represent respectively C activity gradient and temperature gradient along the vertical axis d

I.3.2 4H-SiC homoepitaxial growth

Generally, in order to obtain 4H homoepitaxial growth, one needs 4H seeds which availability came in the mid 1990's. But, this condition is not sufficient because of 3C polytypes stability when nucleation takes place on the terraces (see section I.3.1.1). That is why one needs to use off-oriented substrates in order to promote homoepitaxy by the so-called "step controlled epitaxy" technique proposed by Matsunami et al [I.12, I.13, I.71]. Usually the SiC substrate is tilted typically from 2 – 8° with respect to the basal plane (0001) depending on the polytype (6H or 4H). The substrate shows a surface constituted by steps of atomic height separated by "terraces" (Figure I.5). The steps act as preferred sites for the nucleation, and in order to favor this process, the terrace must be very narrow when compared to the surface diffusion length of the chemical reactants used in the growth. When the nucleation takes place only at the steps, the stacking sequence of the substrate is followed, and the polytype of the substrate grows epitaxially. 3C polytypes nucleation can occur if the terrace is large in comparison to the diffusion length of the reactants.

The step controlled epitaxy was a pioneer work which allowed fabrication for the first time of 4H-SiC epilayers of device quality while keeping the growth temperature in a reasonable range (1500 – 1600 °C). Ever since, CVD has evolved and improved, with the main challenges being maintaining high growth rate and keeping the density of defect as low as possible.

The homoepitaxial growth of 4H-SiC has been demonstrated using multiple techniques. But, in this section we will focus only on CVD which is the core of the present thesis. Different CVD configurations, C and Si precursors and conditions have been studied. This will be briefly reviewed below.

I.3.2.1 Standard 4H-SiC CVD Epitaxy

The typical SiC homo-epitaxial growth is usually performed using silane (SiH_4) as silicon precursor and propane (C_3H_8) as carbon precursor. Hydrogen is selected as carrier gas. The growth temperature is usually between 1500 and 1650 °C. Certainly, the main limitation of this process is the low growth rate (6-7 µm/h) that is correlated to the slow silicon diffusion through the stagnant layer. Also, increasing the Si/H_2 ratio above certain range would cause homogeneous nucleation of silicon droplets in the gas phase. It depletes the precursors in the gas phase available for the deposition and worsens the layer quality. The standard chemistry for the CVD growth of SiC has been extensively studied [I.12, I.28, I.72, I.73]. As mentioned in section I.3.1, to be able to fabricate high power and high voltage devices one need to grow thick (several tens of µm) layers with relatively low doping (10^{13} – 10^{15}). Achieving this thickness using the standard growth rate requires a process time of more than ten hours with a consequently high processing cost (problem of homogenous doping within the layer will rise with time).

Different growth configurations have been tested to increase the growth rates and obtain thick epitaxial layers. The use of a vertical chimney reactor resulted in a growth rate of 10-25 µm/h with a good surface morphology and epilayer quality [I.74]. Also low pressure CVD (in the 50 Torr range) with the usual silane – propane precursors results in growth rate up to 50 µm/h [I.75]. Though, this growth rate could be satisfying, the search for different systems and chemistry continued in order to go beyond.

I.3.2.2 HTCVD (high temperature CVD)

Extremely high temperature SiC CVD growth processes, is also being pioneered to obtain higher SiC epilayer growth rates in the order of hundreds of micrometers per hour [I.47, I.76]. The growth in HTCVD greatly differs from the conventional CVD process; it occurs through sublimation of gas phase nucleated Si_xC_y clusters. The process temperature is extremely high (1800 - 2300 °C) and helium is used as the carrier gas to prevent etching of the susceptor by hydrogen. Growth rates as high as 800 μm/h have been reported, and it is comparable to that of boule growth by the standard PVT method. Along with HTCVD crystal growth, this method for producing epilayer has been up scaled to the industrial level [I.77].

I.3.2.3 Chlorinated CVD

One of the main potential of chloride-based CVD is to prevent silicon nucleation in the gas phase which can occur at high precursor concentration. The Cl precursors were the first used in the 1960's and 1970's but they got replaced by SiH_4 and C_3H_8 in order to avoid problems associated with both the highly reactive and corrosive Cl species and the lower purity of these chlorinated compounds.

The demonstration of very high growth rate in a hot wall horizontal epitaxial reactor [I.78, I.79] using chlorinated precursors renewed their interest in the mid 2000's. At that moment, it represented a huge advance in SiC epitaxy. Using the standard chemistry, e.g. Si-H-C system and adding HCl dramatically reduces the amount of Si clusters in the gas phase. The growth rate increases and the morphology improves. The HCl and Si form $SiCl_2$ or SiHCl species which both are stable species at the growth temperatures that are used and both are presumed active in the growth. There is no need to reduce the pressure, increase the hydrogen flow rate, or temperature.

Regardless of the very high deposition rate (> 100 μm/h) with Cl, a nice surface morphology (RMS ≈ 0.3 nm), high minority carrier lifetime (≈ 1 s) [I.80] and good doping uniformity is obtained. Generally, the purity of the material is not affected by Cl, thus chloride-based material can be highly pure with background doping levels in the mid 10^{13} cm^{-3} ranges. Thus the introduction of chloride precursors in the epitaxy process has several positive potentialities and is considered as a very useful process

that gives the opportunity of improving the quality of the epitaxial layer and the growth yields so that it decreases simultaneously the overall cost of the process.

I.3.2.4 Epilayer crystal defects

Enhancements in epilayer quality are desired as there are presently many obvious defects existing in state of the art of SiC homoepitaxy. Though high-quality 4H-SiC epitaxial growth has been recognized by 'step-controlled epitaxy' in the CVD process [I.12], various extended defects in the epilayers are still considered as a key issue in the fabrication of large-area 4H-SiC devices. In general, many of these defects are present in the substrate and do replicate or propagate through the epitaxial layer. The main defects in typical off-angled 4H-SiC epilayers are threading screw dislocations (TSDs), threading edge dislocation (TEDs), basal plane dislocations (BPD), carrot defects, 3C inclusions named as triangular defects and other types [I.81 - I.86]. In addition, the impact of extended defects on the electrical characteristics of devices varies depending on the defect structure [I.81, I.87, I.88].

Figure I.12 give an example of the triangular and carrots like defects. They are most probably caused by substrate imperfection or improper surface preparation and the majority of these defects have been formed near the epilayer/substrate interface and continues propagating to the surface with the step flow [I.89]. In other words, most of these features arise from substrate defects which act as indices of non-optimal step flow, non-ideal substrate surface finish, contamination, and/or un-optimized epitaxial growth conditions. So improvement of the epitaxial growth procedure is very crucial to avoid the device killing defects.

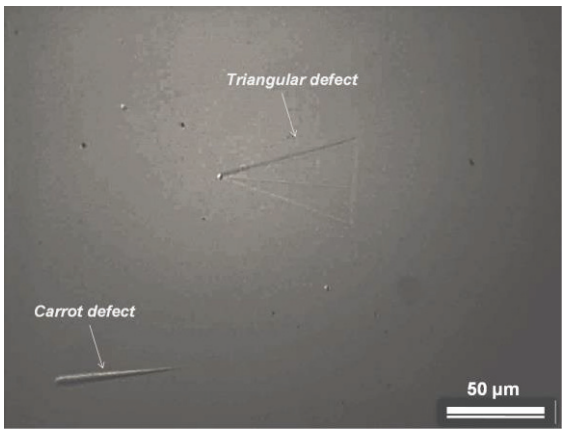


Figure I.12**:** Nomarski optical image of 4H-SiC epilayer grown on 4 ° off axis seed, the layer is characterized by the presence of triangular and carrots like defect

It has been reported that the use of lower off-angle substrates (4° instead of 8°) leads to reduction of basal plane dislocations (BPD) in the epitaxial layers due to the fact that such defects are propagating through the epilayers at the angle of the step flow [I.90, I.91]. It was revealed that the presence and propagation of the BPDs in the epitaxial layers are known to cause a drift of the forward voltage in bipolar devices during operation [I.92, I.93]. Furthermore, a large off angle reduces the number of wafers that can be sliced from a single crystal boule, thus producing an extensive amount of loss material, especially in the big size wafers. Reducing the off-cut angle decreases the wasted material, in this manner the total cost for the final device drops. So, researchers' effort nowadays is directed towards dropping the wafer off angle substrate. However, the main drawbacks of using 4° off angle substrate are typically the formation of step bunching [I.94 - I.96] or TDs of different shapes [I.94] on the epitaxial layers. Though, these formations on the surface can be avoided by carefully controlling the surface chemistry in the growth process. Things get more difficult when growing below 4° off angle substrates [I.97].

I.3.3 3C-SiC heteroepitaxial growth

Up to now, 3C-SiC bulk crystals are not commercially available. This is mainly due to the fact that 3C stabilization requires conditions far from equilibrium and/or low temperatures. In details, above 2000 °C, the 3C polytype is thermally unstable and transformation into hexagonal polytypes can occur. Hence, reduced temperature should be used. As a consequence, it is difficult to achieve high growth rates at growth temperatures below 2000 °C, because the mass transport from the source to the seed is strongly reduced. This implies particular adaption of the conventional growth techniques or development of new approaches. In other words, the lack of commercial 3C-SiC seeds for epitaxy has forced the researchers to prospect for different host materials in order to grow heteroepitaxial thin layers.

The stability of 3C-SiC below the Si melting point (1414 °C) open the possibility of using such substrate for the heteroepitaxy of such polytypes. Commercial α-SiC wafers are other candidate for this purpose. The issues related to the heteroepitaxial growth of 3C-SiC on both kinds of substrates are discussed in the following sections.

I.3.3.1 3C-SiC on Si

The search for the best host substrate started in the late sixties with a rather regular rate of publications until now. This abundance of research could be seen as a demonstration of 3C polytype attractiveness but it hides in fact other key reasons: i) for long (up to early 90's) heteroepitaxy was almost the only way of growing SiC layers on commercial wafers and ii) it was (and it is still) a cheap way (when using silicon substrate) for SiC deposition in regards to the price of hexagonal SiC wafers. Not surprisingly, the most studied substrate for growing 3C-SiC layers is silicon. Indeed, more than 90% of the thin 3C-SiC heteroepitaxial films are grown on such substrate because of the obvious economical and technical advantages and despite the mismatches in the lattice constant and in the thermal expansion coefficients (CTE), see Table I.3. In general, the presence of either a lattice mismatch or thermal mismatch between the materials will result in the occurrence of residual strain in the epitaxial system, strain that will exert an influence on the properties of the epilayers and its processability (wafer bowing).

Table I.3: Physical constants and mismatches between Si and 3C-SiC at room temperature

	Silicon	3C-SiC	Mismatch
Structure	Diamond	Zinc-blend	
Lattice mismatch	0.543	0.436	19.7 %
Thermal expansion coefficient	2.3×10^{-6} K^{-1}	2.5×10^{-6} K^{-1}	8.0%

Despite continuing progress in the crystal growth, 3C-SiC films still contain many lattice defects. In particular, twins, stacking faults and anti-phase boundaries (APBs) have been reported [I.98, I.99]. APBs occur as a common defect when a polar film, SiC in this case, is heteroepitaxially grown on a non-planar substrate. To eliminate this particular defect in 3C-SiC films, Si(100) misoriented with few degrees (2-4° off-angle) has proven to be beneficial [I.100]. Although APBs can be eliminated by growing 3C-SiC on Si (001) with an off-angle, SFs cannot be reduced.

The pioneer work of Nishino et al [I.8] in the mid-eighties, using a two-step deposition process, was a true milestone which accelerated the interest to the subject. The so-called “buffer layer method” (called also carbonization) is based on forming a

SiC buffer layer by carbonization of the Si surface using a hydrogen-hydrocarbon gas mixture. This carbonization step converts the surface of the Si substrate into SiC which serves as a quasi-substrate for the epitaxial growth. In the second stage, a Si source precursor is added to the gas mixture and the basic SiC growth takes place.

But, whatever the recipes or tricks used for thickening and improving the crystalline quality of the grown 3C-SiC material on Si substrate, one has always to struggle with a very large amount of defects initially formed during the nucleation step. In addition, thermal expansion mismatch is also critical because it provokes important bowing after growth. This can be mitigated using specific approaches on (100) wafer [I.101, I.102] but not on (111) orientation which easily leads to crack generation after few μm. Last but not least, the Si substrate itself brings another drawback by limiting the growth temperature to its melting point (1414°C) which is rather low for good SiC epitaxy.

By the early 2002, a technique for reducing planar defects, such as anti-phase boundaries (APBs) and stacking faults (SFs), was developed by growing quasi-bulk 3C-SiC on undulant-Si [I.103]. This technique enabled to fabricate several kinds of power device with low-defect 3C-SiC substrates. Briefly, the undulant Si is a Si (001) substrate whose surface is covered with continuous undulations in which the ridges are aligned in the [1-10] direction, as shown schematically in Figure I.13.

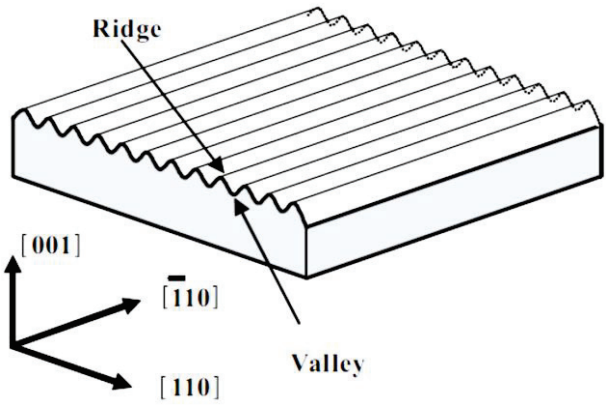


Figure I.13: Schematic view of undulant Si; the Si(001) surface is covered with continuous undulations in which the ridges are aligned in the [1-10] direction

An improvement of this approach was proposed later and called switch-back epitaxy (SBE) [I.103]. In the SBE, the 3C-SiC (001) face grown on undulant Si is turned over after removing of the Si substrate to convert the surface polarity of the residual SFs from the Si-face to the C-face. Then, an additional 3C-SiC homoepitaxial layer is grown on the newly exposed 3C-SiC surface, which is the plane (00-1). Using

SBE, the residual SF shrinks with increasing 3C-SiC thickness, and the SF density decreases drastically to one-seventh [I.104] that of 3C-SiC grown on undulant Si. This is currently the best 3C-SiC material ever grown on Si substrate.

I.3.3.2 3C-SiC on α-SiC substrates (twinning)

Besides the use of silicon as a substrate for the growth of cubic SiC, hexagonal SiC substrate can be used. The lattice mismatch between 3C-SiC (111) and hexagonal (0001) is below 0.1% and problems with thermal mismatch are greatly reduced compared to the growth of 3C-SiC on silicon substrates [I.104]. Considering the general requirements for heteroepitaxy, hexagonal SiC displays almost perfect match as a substrate for growth of cubic SiC. However, 3C-SiC can nucleate on hexagonal SiC in two orientations (Figure I.14), forming twin boundaries (TBs) which significantly deteriorate crystal quality [I.103, I.105]. Unfortunately, it is very problematic to grow twin free layers because both 3C orientations are equiprobable. There are mainly two approaches for achieving such purpose; 1) avoid twining from the nucleation step or 2) promoting the expansion of one orientation among the two possible ones [I.106].

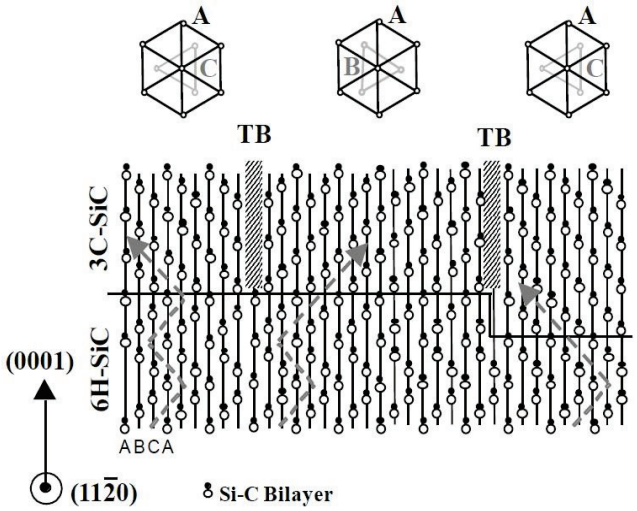


Figure I.14: Schematic representation of TBs formation during 3C-SiC heteroepitaxial layers grown on a hexagonal SiC (0001) substrate either on a terrace or at a step edge

The first approach is probably the most difficult to achieve due to the fact that the two possible 3C orientations are equiprobable as said above. Selecting one orientation among the two on a large area substrate and in a reproducible manner is thus a real challenge. The best 3C-SiC grown to date by Neudeck et al., who proposed a specific method in which 0.2 mm× 0.2 mm mesas were used to produce step-free surfaces and

to grow 3C-SiC material locally without TB [I.107]. However, the local presence of screw dislocations reduced the yield of fabrication of these step-free mesas so the difficulty lies not only in the control of the nucleation step but also in the control of the seed surface reconstruction which is not easy to achieve over large areas.

The second approach requires the tuning of growth conditions after nucleation in order to bend the TBs propagation so that these defects remains buried within the layer. The problem is then transferred to the growth parameters following the nucleation stage. In order to control the 3C nucleation step on α-SiC substrate, one can play both on the growth conditions (temperature, supersaturation, chemistry…) and on substrate preparation. On-axis seeds are preferred over the off oriented ones because it exhibits large terraces where nucleation should occur to promote cubic polytype formation.

Since perfectly on-axis crystals do not exist, they always display steps at the surface, separated by terraces of few to several hundreds of nanometers width depending on step height and/or the exact off orientation of the seed. As received commercial SiC wafers usually do not display any surface reconstruction so that in situ thermal etching under pure H_2 (or H_2 + HCl or C_3H_8) is necessary to reveal the steps [I.108, I.109]. However, the uniformity and reproducibility of the surface reconstruction is strongly dependent on various parameters among which are temperature, time, gas phase composition, substrate real off-orientation and substrate polytype. A TB-free 3C growth seems to be possible with optimized in situ surface preparation of the commercial substrate [I.110, I.111]. It was also mentioned in [I.110] that TB-free growth is independent on the surface step heights, although varying step heights complicate the step flow growth. Though, the interaction with step edges was proposed to be very important for selecting one of the two possible 3C orientations.

Whatever the more effective mechanism to avoid TB formation at the nucleation stage, it should imply the steps. Unfortunately, the situation is rendered even more complicated by the presence of screw dislocations inside the seeds which locally generate a high density of steps. It thus not only breaks the surface reconstruction periodicity but also provokes homoepitaxial spiral growth at its vicinity [I.12, I.112]. This is one of the main restrictions of the nucleation control approach since the

commercial substrates always contain screw dislocations (density in the 10^4 cm^{-2} ranges). It was shown recently that, using optimal carbon-rich surface preparation treatment, almost TB free layers could be grown by CVD on 4H on axis substrate [I.111, I.113]. However, the surface reconstruction after this thermal etching was not shown so that it is difficult to correlate this result with the previous discussion on nucleation.

More details about the nature, propagation and annihilation of the twin, results mainly from 3C-SiC epilayers grown by VLS, will be discussed in Chapter 4 (Ge assisted 3C-SiC nucleation).

I.4 Impurities in SiC

A perfect SiC crystal should not contain anything else except carbon and silicon atoms. However, to grow a completely undoped SiC crystal is almost impossible. But undoped SiC crystal is highly resistive and of limited use except as a substrate for specific devices. By adding a controlled amount of impurities, usually called dopant, the electrical characteristics of the crystal can be changed. A dopant can substitute a host atom in the SiC lattice and the dopant atom is then called substitutional. Or, it can be incorporated into the lattice but not at a substitutional site, then the dopant will be called interstitial. Finally, the most un-wanted possibility is that it forms a complex together with an intrinsic crystal defect, such as a vacancy.

The growth system and precursors would always contribute with impurities. Nitrogen, aluminum, boron and titanium are well known and studied impurities in SiC. Other impurities used for obtaining semi-insulating material have been investigated also for SiC (Fe and V) [I.114, I.115]

I.4.1 n- and p-type doping

The most typical dopants for SiC are nitrogen (N) for n-type and aluminum (Al) for p-type conductivity. Molecular nitrogen (N_2) and liquid trimethylaluminum (TMA) are the common precursors for these dopants. Some alternative dopants such as phosphorus for n-type and boron for p-type have also been investigated [I.116, I.117], but they are not as convenient as N and Al. N is the preferred n-type dopant over P because it has a higher probability to be incorporated into the lattice [I.45].

Boron is avoided as p-type dopant because of the it's rather high diffusion rate in SiC [I.118, I.119]. Moreover, boron can form complexes with H and can incorporate either on C or Si site so that it make it less predictable and reproducible as a dopant [I.120].

N is an impurity difficult to remove so that most of the non-intentionally doped layers are n-type. While some variation in epilayer doping can be carried out strictly by varying the flow of dopant gases, the site-competition doping methodology has enabled a much broader range of SiC doping to be accomplished [I.116, I.121]. The site-competition doping idea relies on the point that many dopants of SiC preferentially incorporate into either Si or C lattice sites. Generally, the atomic radii of any dopant play the major role in selecting its site within the SiC lattice. This means that N and Al preferentially incorporate on C and Si respectively. So, by epitaxially growing SiC on Si face 4H-SiC substrate under carbon-rich conditions, most of the nitrogen present in the CVD system can be excluded from incorporation into the growing SiC crystal. Thus a highly pure layer can be achieved. On the other hand, by growing in a carbon-deficient environment or on C face substrate, the incorporation of nitrogen can be enhanced to form very heavily doped epilayers for Ohmic contacts. Aluminum is opposite to nitrogen and prefers the Si site of SiC. Other dopants have also been controlled through site competition by properly varying the Si/C ratio during crystal growth. In addition, site competition has also made moderate epilayer doping more reliable and repeatable. N and p-type SiC epilayer doping ranging from mid 10^{14} to 1×10^{19} cm^{-3} are commercially available, and researchers have reported obtaining doping over a factor of 10 larger and smaller than this range [I.122].

I.4.2 Metallic impurities

As just mentioned, some of the impurities are un-avoidable since they either come from the precursors or from the system (susceptor mainly). Among them, the transition metals, Ti and V have been studied in detail as impurities in SiC. Studies of the behavior of vanadium in SiC became especially relevant after it was found that doping with V leads to the formation of semi-insulating (SI) layers of silicon carbide [I.114, I.123, I.124]. Introducing vanadium during CVD growth yielded epitaxial layers of 6H-SiC with a resistivity of 3000V.cm. Recent reports show that iron (Fe)

also may be a possible candidate to obtain SI SiC [I.125]. Manganese (Mn) and iron (Fe), may also be used to obtain diluted magnetic semiconductors [I.126 - I.129]. Deep levels inside intentionally doped SiC with various elements (Fe, W and Nb) were considered [I.130 - I.132]. Detailed review on the effect of other elements mainly on properties and deep levels of SiC can be found in the reference [I.133].

I.4.3 The specific case of Ge

The group IV element germanium (Ge) is an isoelectronic impurity in silicon carbide (SiC). This means that Ge does not induce any electronic doping to SiC (neither donors nor acceptors). Despite this we will abusively use the term "doping" to refer to Ge incorporation into SiC in all the manuscript.

Ge is a low bandgap (0.66 eV) semiconductor that allows the operation at lower voltage. It is characterized by high carrier mobility (1900 cm^2/Vs and 3600 cm^2/Vs for holes and electrons respectively), with a hole mobility value that is one of the highest of all the commonly used semiconductors, see Table I.2. It is worth noting that the first transistor, father of all the modern devices, was created in 1947 using Ge bulk crystal [I.134].

The link between Ge and SiC has been always rather weak but constant in the last decades. One can divide the work on Ge together with SiC into three main categories:

1) The SiGeC alloys study
2) Ge addition in the SiC growth techniques
3) Ge/SiC heterojunction or contacting

Before detailing all the aforementioned points the Si-Ge-C chemical system has to be presented.

I.4.3.1 Si-Ge-C chemical system

There are very limited data on the ternary phase diagram of Ge-Si-C. Extremely low carbon solubility in bulk germanium (Ge) and thermodynamically unfavorable Ge-C bond has hindered the production of crystalline $Ge_{1-x}C_x$ alloy materials in a close to equilibrium growth system. Note a recent work suggesting the VLS growth of $Ge_{1-x}C_x$ nanowires (NWs) [I.135].

Carbon has also a low solubility in bulk Si (3 x 10^{17} cm^{-3}) and Ge (1x 10^{8} cm^{-3}) near the melting point of both elements [I.136 – I.138]. It is 934 and 1414 °C for Ge and Si, respectively. Any alloy with a substitutional concentration above the bulk solubility is thermodynamically metastable. As a result, a mono-crystalline film of SiCGe has not been obtained yet. The experimental limit of solubility of Ge in SiC at very high temperature close to 2300 ˚C was found to be $3x10^{20}$ $at.cm^{-3}$ [I.139].

I.4.3.2 $Si_xGe_yC_{1-x}$

Owing to a very low solid solubility of C in either Si or Ge and the large size-differences among Si, C and Ge atoms, synthesis of the ternary alloy SiCGe with stable composition and structure is very difficult. So, special non-equilibrium epitaxial growth conditions are required to grow metastable films with substitutional carbon concentrations greater than few atomic percent. It was shown that the incorporation of substitutional carbon increases with reduced growth temperature and higher growth rates [I.140, I.141]. Moreover, Chen et al [I.142] revealed that at a growth temperature of 1100 °C, the content of Ge is < 0.1 % even if the flow of GeH_4 was higher than that of C_3H_8. So, there is no stable ternary alloy at high growth temperatures.

I.4.3.3 Ge addition during SiC growth

Ge-modified silicon substrates is one of the methods to improve the quality of the SiC/Si system [I.143]. The use of Ge in this approach is beneficial in terms of the improvement in crystalline quality of the grown 3C-SiC layers [I.144] even with a thickness of 120–300 nm. This could be related to the fact that the presence of Ge in the reactor during Si substrate carbonization partially relieves residual misfit strain due to the large Si–SiC lattice mismatch [I.145, I.146]. Beside all these enhancements the surface roughness increases greatly with the introduction of Ge, which will slow down the use of such layers in the application domain [I.147]. Ge is added to the MOCVD growth of SiC on Si (111) and SIMS results show that Ge has incorporated into the SiC film ([Ge] was not quantified due to the lack of reference sample). In the same manner, Pezoldt et al [I.148] revealed that Ge remains near the SiC/Si interface independently of the pre-deposited amount of Ge. It was also found in the same study that the presence of Ge during the carbonization process resulted in a reduced growth rate and a repetitive lower film thickness [I.149].

SiC epitaxy on SiC substrate in the presence of Ge was mostly studied in the case of liquid phase growth. For instance, homoepitaxial 4H-SiC epilayers were grown using Si-Ge melt with the dipping technique [I.59, I.150]. The surface morphology was characterized by hillocks when growing on on-axis substrates. However, high quality, macroscopically flat layers were deposited on substrates with off-orientation of about 5°. Micropipe healing during epitaxial growth was demonstrated. However, the growth rates were low due to low C solubilities in the melts and high Ge evaporation at high temperature. Unfortunately for this study, no determination of Ge concentration in the grown crystals was done.

In a different manner, Ge based melts was employed in the VLS growth of SiC epilayers [I.151]. It was shown that 3C-SiC is favored due to the formation of 3C-SiC islands on the seed surface, during the heating ramp, by a dissolution/precipitation mechanism [I.152]. In the grown 3C-SiC heteroepitaxial layers, Ge incorporation level can reach up to $1x10^{20}$ at.cm^{-3} [I.153] but in interstitial site rather than lattice site [I.154]. Transmission electron microscopy (TEM) revealed that Ge is incorporating in these layers through nanoscale interstitial clusters [I.155].

I.4.3.4 Ge/SiC heterojunction or contacting

Some studies are suggesting that the incorporation of Ge atoms in SiC lattice can give benefits to its electronic properties. For instance, after Ge implantation and annealing, the conductivity and resistivity of Ohmic contacts of 4H-SiC were found to improve [I.156, I.157]. This implantation was shown not to produce any precipitation or nano-clustering in the lattice [I.158]. This improvement of Ohmic contact was also seen when growing a Ge doped SiC layer by VLS mechanism, beneath a NiSi metallic contact [I.159].

For completing this part, note also the study of Gammon et al [I.160] on Ge/SiC hetero-junction diodes or the works on the growth mode and desorption of Ge nanocrystals on SiC (0001) giving information on the epitaxial relationship between these two materials [I.161 - I.164].

I.5 Conclusion and Motivation of the dissertation

In this Chapter, we have shown that the recent development in the field of silicon carbide (SiC) turned it to be highly promising material in the semiconductor

technology with extraordinary properties. The α-SiC and β-SiC epitaxial growth mechanisms and techniques were reviewed.

Nowadays, the technology of SiC epitaxy is rather advanced and very well controlled. For instance, the SiC doping with dopants of different conductivities (n and p type) has reached great level of maturity. Apart from this, the case of non-dopants (metallic impurities) did not attract enough attention from developers, and was not greatly implemented in the growth systems. There are very few reports on the investigation of the addition of another foreign element to the classical CVD system. A few papers on V, Fe, Ti, W and Nb incorporation exist; though in most cases the elemental incorporation was either non-intentional or occurred in a non-controlled manner.

Taking the specific case of Ge, owing to the similarities of the physical-chemical properties between SiC and Ge, its incorporation can have benefits. Presence during the growth of 3C-SiC/Si substrates reduced the stress in the grown layer. On the other hand, its incorporation by implantation showed that although Ge is not a dopant species for SiC (being a IV-group element as Si and C) its presence in the lattice improved the conductivity and resistivity of Ohmic contacts.

The case of Ge is rather unstudied using standard CVD epitaxy and since it can be easily implemented via GeH_4 gas. We found it an interesting and original subject to look at. Thus, our motivations are: 1) Considering the fundamental science part since we are adding an isovalent foreign element (Ge) into the classical CVD system (Si-H-C) and therefore into SiC matrix at the first place, 2) Studying the Ge interaction with SiC epitaxy during the CVD process and checking the possibility of any influence of such addition on the layer quality, 3) Investigating the Ge incorporation mechanisms and levels under different growth, 4) Exploring the possible interaction with other standard impurities mainly N by structural, optical and electrical means, 4) Finally, looking at the connection between Ge and polytype stability or growth.

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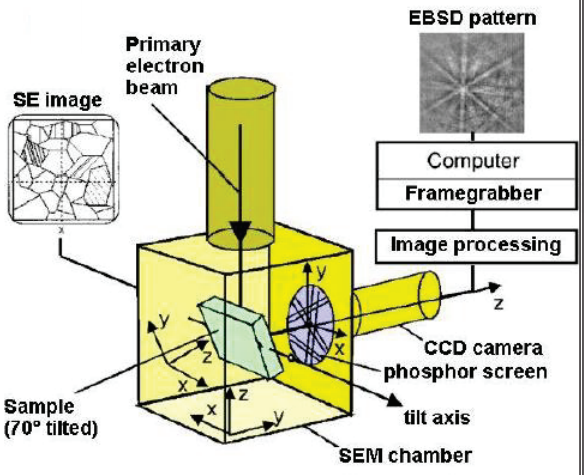
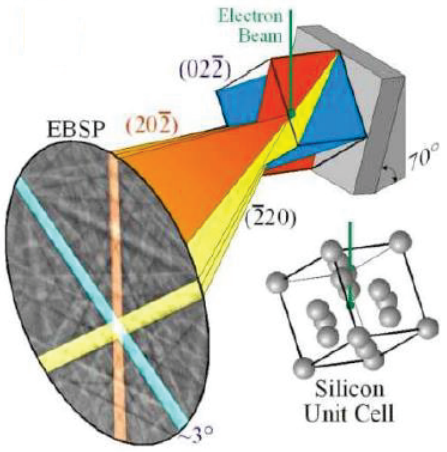
Chapter II

Experimental Techniques

Principle of EBSD pattern formation	Scheme of EBSD measurement
	

LABORATOIRE DES MULTIMATÉRIAUX ET INTERFACES - UMR 5615
ERI : EPITAXIE ET RÉACTIVITÉ D'INTERFACES

Chapter II: Contents

Chapter II: Experimental Techniques

This Chapter is dedicated to the employed characterization techniques to determine the different properties and the quality of the grown epitaxial layers. The most and frequent used methods are highlighted. At last, the epitaxial growth apparatus (chemical vapor deposition) is described.

II.1 Introduction

Characterization of the epilayers is crucial for two main reasons; first it gives feedback on the growth parameters and related processes to improve the quality of the layers. Second, impurities and defects in the epilayers influence the characteristics of these layers. Therefore, investigations of the structural, optical and electrical properties of the epilayer together with the new formations associated with any modifications to the system (like adding Ge in our case) are very important in the advancement of semiconductor technology.

In this study the epitaxial grown layer morphology and structure along with its optical and electrical properties is deeply investigated. Nomarski optical microscopes, scanning electron microscope (SEM) and atomic force microscopy (AFM) are used to get information on the top surface morphology. The quality and optical properties were seen by Raman spectroscopy and low temperature photoluminescence.

While CV mercury microprobe helped in determining the doping level, Hall measurements were conducted on specific samples to evaluate the carrier concentration and thus carrier mobility and conductivity. Deep and shallow levels are also investigated by means of admittance spectroscopy and deep level transmittance spectroscopy (DLTS).

Special techniques like conductive (CAFM), scanning capacitance microscopy (SCM) and electron backscattered diffraction (EBSD) are utilized for very specific issues which will be mentioned later. In the following section, we will make a brief description of the main tools used.

In fact, most of the routine characterizations were made in our institute while specific ones were performed within the NetfiSiC framework at partners' institutes. I had the opportunity to participate to most of these characterizations through short visits and secondments to the concerned institutions, whose are listed in Table II.1.

Table II.1: Detailed list of all the measurements done outside our institute and within the Framework

Index	Laboratory	Measurements	Period
Secondment 1	Institute for Microelectronics and Microsystems (CNR-IMM) Catania, Italy	DLTS, admittance and Hall effect	2 weeks
Secondment 2	applied physics laboratory in Friedrich-Alexander University - Erlangen	C-AFM, SCM and characteristics of Schottky contacts on 4H-SiC epilayes with Ge incorporation	2 weeks
Short visit 1	Laboratoire Charles Coulomb (L2C) in Université Montpellier 2, France	LTPL spectroscopy	2 days
Short visit 2	Laboratoire Charles Coulomb (L2C) in Université Montpellier 2, France	SIMS	2 days
Short visit 3	Laboratoire des Matériaux et du Génie Physique (LMGP) – Grenoble, France	EBSD	2 days

II.2 Raman spectroscopy

Raman scattering was discovered in 1928 by V. C. Raman who won the Nobel Prize for his work. Briefly, Raman spectroscopy is a spectroscopic technique based on inelastic scattering of monochromatic light, usually from a laser source. Inelastic scattering means that the frequency of photons in monochromatic light alters upon interaction with a specimen. Photons of the laser light are absorbed by the sample and then reemitted. Frequency of the reemitted photons is shifted up or down in comparison with original monochromatic frequency, which is called the Raman Effect. This shift provides information about vibrational, rotational and other low frequency transitions in molecules. Raman spectroscopy is considered as a very effective and practical tool for quick chemical identification, characterization of molecular structures, environment and stress on a sample.

II.2.1 The specific case of SiC

For the specific case of SiC, from the position, height, full width at half maximum (FWHM) and the shift of the SiC Raman peaks, one can get information on the crystal structure, strain, lattice related defects and doping. The frequencies of the main polytypes and their peaks positions are listed in Table II.2 and shown in Figure II.1

Table II.2: Raman frequency of the main SiC polytypes

Phonon modes – Frequencies (cm^{-1})				
Polytype	**TA**	**TO**	**LA**	**LO**
3C-SiC	-	796	-	972
4H-SiC	196, 204, 266	776, 796	610	838, 964
6H-SiC	145, 150, 236, 241, 266	767, 789, 797	504, 514	889, 965

TA and TO are Transversal Acoustic and Transversal Optic modes, respectively,
LA and LO are Longitudinal Acoustic and Longitudinal Optic modes, respectively.

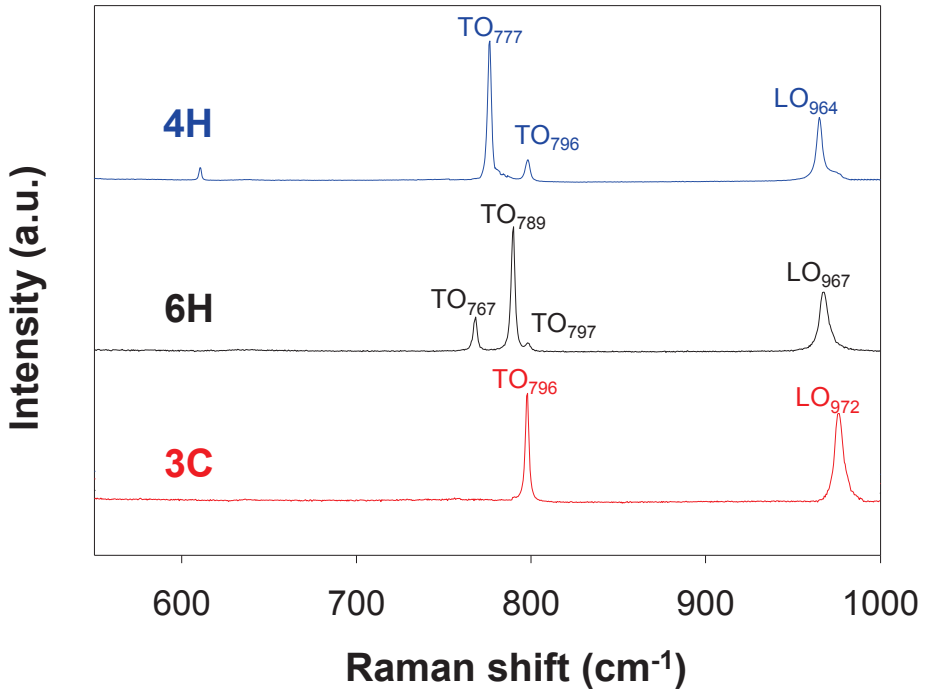


Figure II.1: Raman spectra of the main SiC polytypes

4H-SiC shows two main characteristic Raman lines: a transversal optical (TO) mode at 777 and 796 cm^{-1} and a longitudinal optical (LO) mode at 964 cm^{-1}. Though, 3C-SiC shares the same peak in the transversal mode with 4H-SiC, it can be differentiated from its characteristic peak in the optical mode which lies at 972 cm^{-1}. Both modes can be used for polytypic identification though this is rendered difficult when a thin layer (<0.5 µm thick) is deposited on α-SiC substrate, due to the strong signal coming from it. In addition, from the FWHM and the position of the LO peak, the n type doping concentration can be estimated. In this case, the detection limit is roughly from 5 x 10^{16} – 1 x 10^{18} $at.cm^{-3}$ [II.1, II.2]. Finally, qualitative information on p-type doping can also be obtained if the doping level is high enough (> 10^{18} cm^{-3}) [II.3].

II.2.2 The specific case of Ge

We shall start with a description of the Raman spectrum of pure Ge and SiGe alloys. The reported position of the Ge–Ge peak in pure Ge is located at about 300 cm^{-1} [II.4]. The μ-raman spectrum of Si_xGe_{1-x} alloys are characterized by three modes in the range of 250 to 650 cm^{-1}; in addition to the Ge-Ge peak that is shifted to the left depending on Si content, there exist a Ge–Si peak at about 400 cm^{-1} and a peak can be from 475-500 cm^{-1} (depending on Si content) attributed to the local Si–Si vibrations, see Figure II.2. The percentage of Ge in SiGe alloy can be easily deduced from the position of the Ge-Ge vibrational peak [II.5].

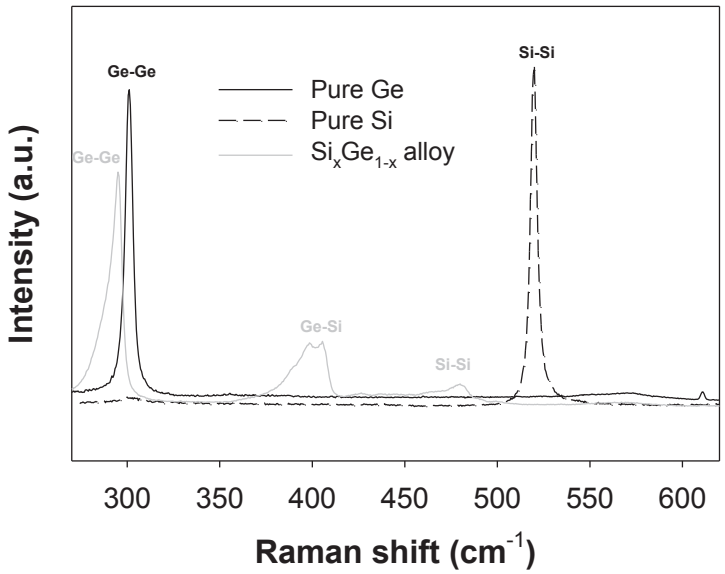


Figure II.2: Raman spectra of pure Ge, pure Si and Si_xGe_{1-x} alloy (x=0.35)

Renucci et al [II.6] and Rath et al [II.5] studied the evolution in the position and FWHM of the peaks related to Si_xGe_{1-x} alloy as a function of the alloy composition. They have shown that when the Si content of these alloys increases then the Ge-Ge peak position is shifted to lower wavenumber.

The only work in the literature on the assessment of Ge within the lattice of SiC by Raman spectroscopy was conducted by Nada Habka during her thesis at LMI [II.2]. It has been shown that Ge-Ge vibrational peak can be easily seen when the studied epilayer is of 3C-SiC polytype and grown on α-SiC substrates by VLS technique using Si_xGe_{1-x} melt. However, there is no such peak when the same melt is implemented in growing 6H homoepitaxy rather than 3C-SiC. A Raman spectrum

collected from SiC layer grown by VLS and containing Ge is depicted in Figure II.3. One can easily notice the peaks attributed to both Ge-Ge and Si-Ge vibrations.

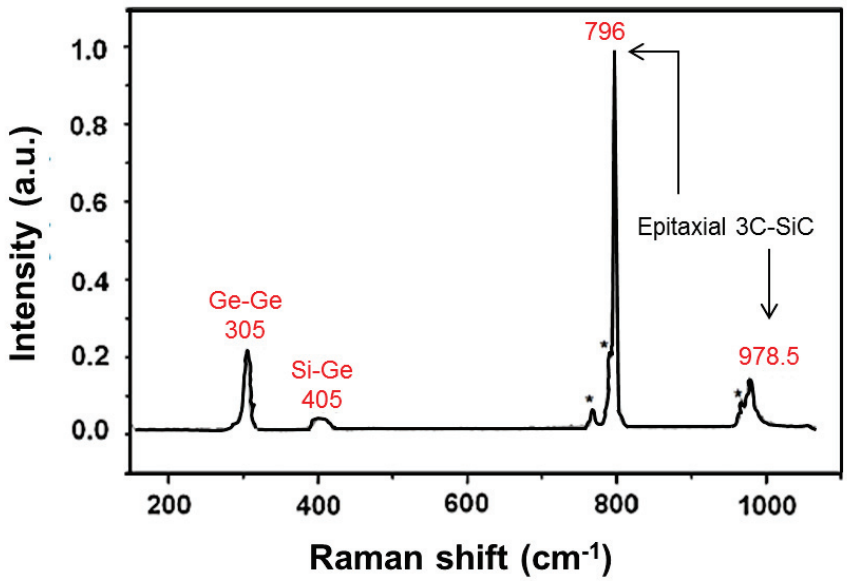


Figure II.3: Raman spectrum of VLS sample grown with $Si_{0.25}Ge_{0.75}$ alloy at T=1350°C. The peaks marked by * are from the 6H-SiC substrate. The evaluated Ge concentration of this layer is $6x10^{19}$ at.cm^{-3}

Finally, Habka et al [II.2] have shown that the amount of Ge incorporated inside 3C heteroepitaxial layers grown on α-SiC substrates using SiGe melts by VLS can be deduced from the Ge-Ge peak position as presented in Figure II.4.

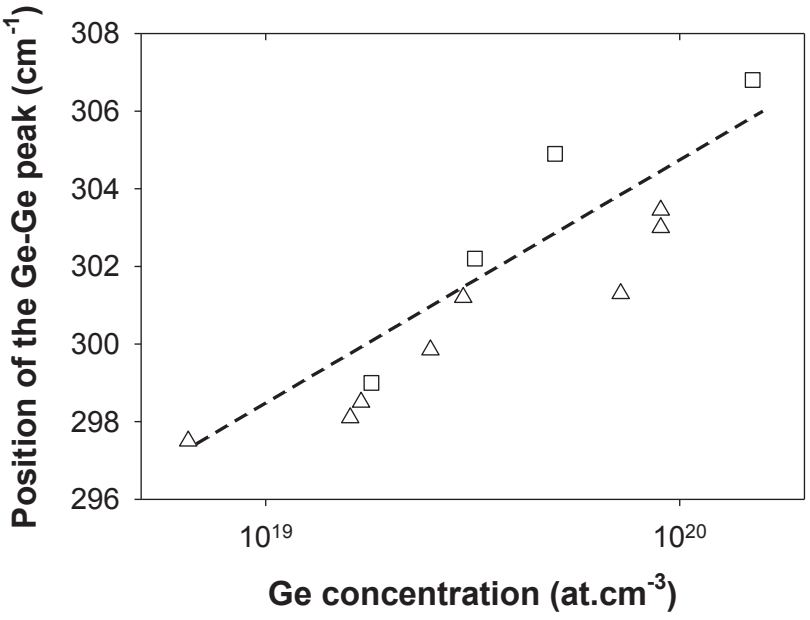


Figure II.4: Evolution of the position of Ge-Ge peak as a function of Ge concentration in the 3C-SiC epilayer measured by particle induced x-ray emission-PIXE (squares) and SIMS (triangles), [II.2].

In summary, Raman spectroscopy was shown to be an option to study the composition of Si_xGe_{1-x} alloys and it may be useful for assessing Ge incorporation inside SiC lattice.

II.2.3 Specifications of the employed Raman spectrometer in this work

A μ-Raman spectrometer (LabRAM ARAMIS HORIDA) equipped with a 20 mW HeNe laser beam (λ = 633 nm) with a spot of few μm^2 in a co-focal configuration for polytypes identification. However, for Ge detection, the use of co-focal configuration is not the best, an improved sensitivity can be obtained by using the objective 10X instead of that with 100X [II.7]. This configuration enhances the surface area analyzed by the laser with a factor of 2.6. In other words, the spot size is 5x3 μm^2 and 13x7.8 μm^2 for the objectives 100X and 10X, respectively. Note the used of 30 seconds acquisition time for two cycles. Thus, Raman measurements are rather quick. This apparatus is available at the Centre Commun de Microspectrométrie Optique (CECOMO) of Lyon.

II.3 Secondary Ion Mass Spectrometry (SIMS)

The Secondary ion mass spectrometry (SIMS) technique has gained wide spread acceptance as a tool for thin film and surface analysis owing to its high sensitivity and capability to provide information on the chemical composition of the surface.

In a SIMS analysis, the sample is bombarded with a beam of charged particles with energies in the 1-30 keV range. These incoming particles are called primary ions. This leads to the ejection (or sputtering) of both neutral and charged (+/-) species from the surface. The sputtered material is mostly neutral, but ~1% is ejected in the form of charged particles. The ejected species may include atoms, clusters of atoms and molecular fragments, see Figure II.5. The ejected ions are then analyzed by a mass spectrometer. They are subjected to a mass filtration prior to the detection and the mass spectrum is then obtained. The SIMS data can be recorded as mass spectra, depth profiles or ion images. The depth profiling is obtained by continuously analyzing while sputtering. The selection of the incident ions used for bombarding the

sample largely depends on the application and the targeted elements. The most used ones are Ar^+,Cs^+, Ga^+ and $O2^+$. It is worth noting that the resolution of the SIMS measurement is dependent on the surface morphology. A rough surface will result in accuracy loss in the SIMS profile.

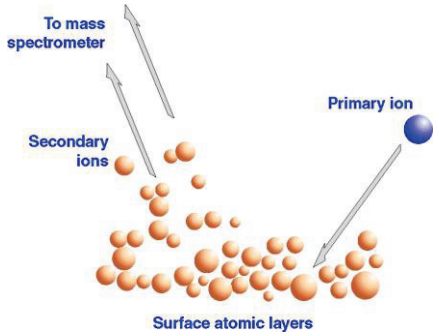


Figure II.5: Principle of SIMS

Additionally, SIMS allows thickness measurement if the analyzed elements are in different concentrations in the layer and in the substrate.

The main limitations of this technique are:

1) It is destructive
2) No quantitative model currently exists that can accurately predict the secondary ionization process. So, one needs a suitable reference samples for quantification purposes with experimental corrections
3) Care should be taken about isotopic abundance of each element specifically that with various stable isotopes
4) The material sputtered from the sample surface consists not only of mono-atomic ions but molecular species that in places can dominate the mass spectrum. Therefore possible mass confusion is always expected.

II.3.1 The specific case of Ge in SiC

Ge concentration in SiC may well be quantified by Secondary Ion Mass Spectrometry (SIMS). It is important to take into account the natural abundance of each isotope: For ^{27}Al and ^{14}N, they are close to 100% but for ^{74}Ge it's 36.54%. The stable isotopes of Ge are ^{70}Ge, ^{72}Ge, ^{73}Ge, ^{74}Ge and ^{76}Ge. Then it is necessary to adjust the intensities of ^{74}Ge to obtain the Ge overall concentrations. Ge concentration and depth profile in SiC has been broadly considered in the study of 3C-SiC epitaxial growth using SiGe melts by VLS technique [II.2, II.8 – II.10].

II.3.2 Description of both equipment and the measurement

Modified Cameca IMS 4f equipment with an O^{2+} ion source is used. This is the usual configuration of this SIMS equipment. The primary beam voltage was 15 kV and the primary current from 600 – 1200 nA. This resulted in an average etching rate of 30 – 60 Å/s. To calibrate the concentration, Relative Sensitive Factors (RSF) was defined from reference samples where the concentration profiles are well known ($74Ge^+$ / $13C^+$= 2.8 x 10^{18}). The determined detection limit of ^{74}Ge was around few 10^{15} at.cm^{-3}. The Nitrogen concentration should be high enough to be detected using this configuration, its limit of detection ~10^{17} cm^{-3}.

The used crater size is ~150 µm x 150 µm. Thus, zone of analysis is rather small and could be avoided if later some other characterizations are required or devices are fabricated.

All the measurements were done at Laboratoire Charles Coulomb (L2C) in Université Montpellier 2.

II.4 Scanning probe microscopy (SPM)

Scanning probe microscopy was developed to enable scientists to investigate surfaces with atomic resolution. It is a division of microscopy that used to make images of nanoscale surfaces and structures, including atoms using a physical probe that scans the specimen. In addition to picturing nanoscale structures, certain types of SPMs can be used to control individual atoms and move them to make specific patterns. SPMs are different from optical microscopes because the operator never sees the surface directly. Instead, the tool textures the surface and creates an image to represent it. The first member of SPM family, scanning tunneling microscopy (STM), was developed in 1980s. In 1982, Gerd Binnig and Heinrich Rohrer at IBM in Zurich created the ideas of STM [II.11]. Both of the two people won 1986 Nobel Prize in physics for their brilliant invention. Together with Dr. C. F. Quate from Stanford University, they developed the atomic force microscope (AFM) on 1985 [II.12]. In this part we will detail the AFM technique, CAFM briefly and describe the uses and benefits of SCM and SSRM.

II.4.1 Atomic force microscopy (AFM)

Three years after its invention, AFM becomes available commercially. The atomic force microscope (AFM) grew out of the STM and nowadays it is by far the more predominant of the two. Unlike STMs, in AFM no flow of current is needed between the probe and the sample therefore, surface topography from insulators as well as semiconductors and conductors can also be attained. This marks it superior to other SPMs based instruments.

An AFM has a probe tip mounted on the end of a cantilever that is usually 100–500µm long, see Figure II.6. The tip is moved across the sample many times. It can be moved precisely and accurately back and forth across the surface through a scanner made of a piezoelectric material. The accuracy of the scanner movements in the vertical and horizontal directions is vital to collect information from the atomic-scale interactions.

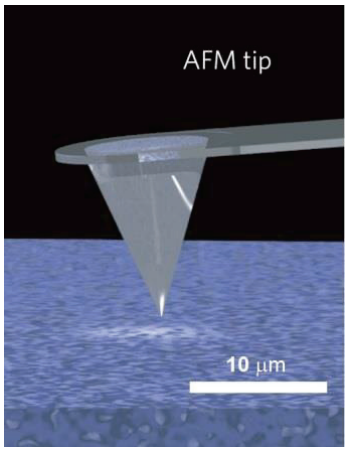


Figure II.6: AFM tip

Forces between the tip and the sample surface cause the cantilever to bend, or deflect. These deflections are measured by a detector as the tip is scanned over the specimen. This allows producing a map of surface topography. The tip-sample spacing determines the type of force that will contribute to the deflection of an AFM cantilever. The two principle primary AFM modes are tapping and contact mode. Many secondary modes can be derived from these primary modes. Some of these modes will be mentioned later in this chapter. The force-distance curve is a basic

AFM operation to explain its modes, Figure II.7. When the probe is far-away from the specimen, the cantilever is in its rest position and no force is identified. By getting the tip to the surface, the cantilever bends towards the sample under the effect of Van der Waals' attractive forces. The tip plunges to the sample surface (jump to contact) when the attractive gradient overcomes the cantilever elastic response. After that, the tip is in contact with the sample and the cantilever is deflected by a repulsive regime of interactions. So, in contact mode, also known as static or repulsive, the tip is in continuous contact with the specimen. The cantilever is usually not vibrating, but deflected due to friction or other forces. As the scanner traces the probe tip across the surface, the contact force causes the cantilever to bend according to the surface altitude and the resulting image is a topographical map of the surface of the sample. This provides accurate results, at the expense of touching and potentially damaging both the probe and the sample. Typically, the forces applied to samples in the contact mode are in the range from tens to hundreds of nano-Newtons. Indeed, among the first AFM applications, the contact mode studies were aimed on getting high-resolution results and, particularly, achieving molecular and atomic resolution on crystalline surfaces.

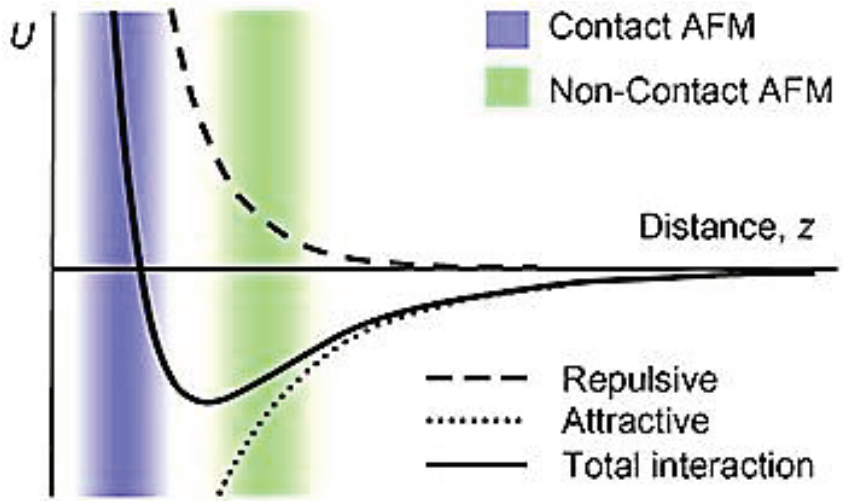


Figure II.7: The force distance curve

Tapping mode is also referred to dynamic contact mode, as the cantilever is oscillated between the repulsive and attractive regimes in tapping mode. It is then a compromise between non-contact modes sample-friendliness and contact modes accuracy. In this mode, the amplitude of oscillations is fixed and the frequency of oscillations is measured, or vice versa.

II.4.2 Conductive atomic force microscopy (CAFM)

CAFM is considered as a secondary mode derived from the contact mode (primary). Conductive AFM is able to image both the topography and the conductivity of the surface at the same time. It characterizes conductivity variations through medium- to low-conducting and semiconducting materials. CAFM has a current range of pA to µA by employing a conductive probe tip. Typically, a DC bias is applied to the tip and the sample is held at ground potential and the current flow between the two is measured. An example of CAFM measurement on 3C-SiC epitaxial layer grown on 4H-SiC on axis seed from this study is depicted in Figure II.8.

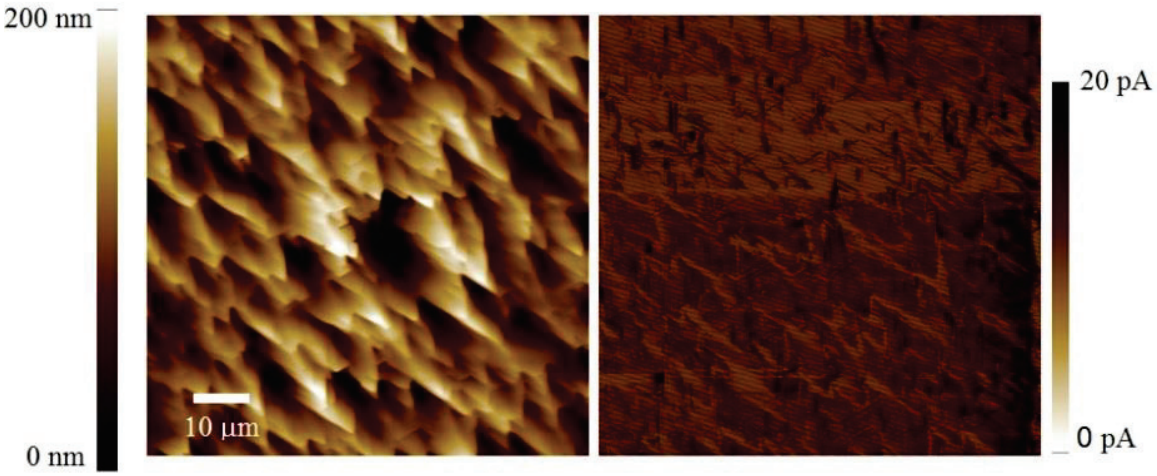


Figure II.8: Topography (left) and Conductive AFM (right) of 3C-SiC epilayer

As an example, C-AFM has been used to obtain the I-V characteristics of small contacts and to investigate the 3C-SiC epilayer morphology along with its current distribution [II.13]. Also one can find in the literature that CAFM can also be used to check the lateral homogeneity of metal/SiC interfaces [II.14].

II.4.3 Scanning capacitance microscopy (SCM)

Scanning capacitance microscopy (SCM) is a secondary imaging mode derived from contact AFM. Typically doped semiconductors are investigated by this technique since it records changes in majority electrical carrier concentration (electrons or holes) through the studied surface. The concept of SCM is very simple, once a high frequency (90 kHz) AC bias is applied to the sample; an ultra-high frequency (1 GHz) detector measures the local tip-sample capacitance variations as

the tip scans across the sample surface. These capacitance changes are a function of the majority carrier concentration in semiconductors. Hereafter, relative carrier concentration can be mapped in the range of 10^{16}–10^{21} cm^{-3}. This method was mainly employed for quantitative carrier profiling in SiC samples [II.15], for dopant profile measurements in ion implanted 6H–SiC by scanning capacitance [II.16] as well as for investigation of SiC interfaces and devices [II.14].

II.4.4 Instrumentations used in this study

All the AFM measurements on the homoepitaxial growth of 4H-SiC (results shown in Chapter III) are done in our Lab using Scien-tech (picoscan 5) apparatus in contact mode.

Regarding the CAFM and SCM measurements, they were all performed within the facilities of our partner in Institute for Microelectronics and Microsystems (CNR-IMM) Catania. I have accompanied some of the experiments during the 2 weeks stay over there. This was performed using a Veeco DI dimension 3100 atomic force microscope (AFM), equipped with the nanoscope V electronics and the conductive module (C-AFM) was used to acquire I-V curves on the small diodes. A detailed description about these diodes and its fabrication procedure can be found in the results section. SCM measurements were carried out by using a Digital Dimension 3100 microscope**.**

II.5 Capacitance voltage measurements (C-V)

II.5.1 Specific case of mercury microprobe station

Monitoring the doping type and concentration is critical issue for calibrating the growth parameters for epitaxial growth of the device structure. In the present study, this was achieved by the mercury probe measurement, which is considered as a rapid, convenient and non-destructive characterization technique.

C-V measurements are operational on rectifying metal semiconductor Schottky contacts. The mercury probe applies mercury over the epilayer surface as temporary contacts in the form of two disks, one with very small diameter which would act like Schottky contact and other with large known diameters acting like Ohmic contact. Once a low leakage current is determined, a reverse voltage is applied between the

two contacts and the capacitance is measured. A few volts are applied depending on the expected doping concentration and depth to be probed. The relationship between the capacitance and net doping concentration (n-type in this case) is given by [II.17]:

$$C = A\sqrt{\frac{\varepsilon.\varepsilon_o.Nd}{2\left(V-\frac{KT}{e}\right)}} \quad (1)$$

where A is the diode area, ε the semiconductor dielectric constant ε_0 is the permittivity in vacuum, V is the applied reverse bias, k is the Boltzmann constant, T the temperature and e is the elementary charge.

Similarly, the doping depth profile can be extracted using this method. Also, the maximum probed depth depends on both subjected reverse voltage and net doping concentration. Now, the depletion width is inversely proportional to the capacitance and the relationship between them is given by:

$$W = A\frac{\varepsilon.\varepsilon_o}{C} \quad (2)$$

Finally, mercury is liquid and can easily be withdrawn from the epilayers.

II.5.2 Our instrument and measurement limitations

During the whole study, a MDC mercury probe connected to C-V plotters, computerized semiconductor measurement systems is used. As a matter of fact, this technique measures the net donor (N_d - N_a) or acceptor (N_a – N_d) concentrations, so care has to be taken to a possible compensation within our layers. In addition, the depletion width is inversely proportional to the doping level (see equations 1 and 2). This means that if the layer is highly pure ($\leq 10^{14}$ cm^{-3}) then thick layer has to be grown in order to be able to measure the doping level and overcome the depletion layer. It is worth mentioning that our growth conditions give very pure layers and doping levels in the few 10^{13} cm^{-3} were sometimes measured, see Figure II.9.

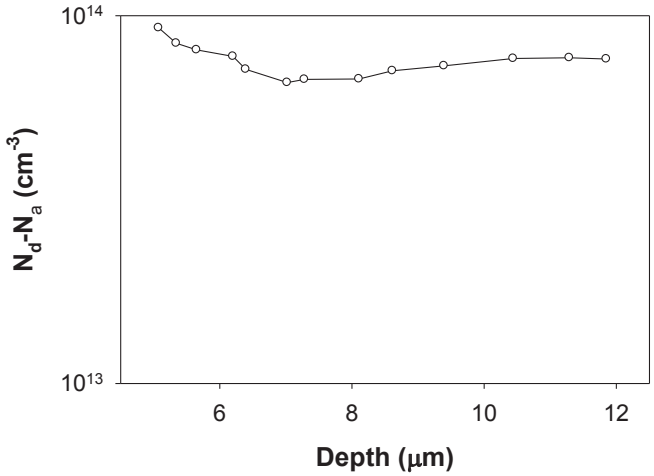


Figure II.9: Doping depth profile of a very pure epitaxial 4H-SiC layer grown at 1500 C for 2 hours measured by C-V mercury microprobe station. The capacitance at zero voltage was rather low in the order of 10 pF

From Figure II.9, one can easily see that the depletion width is around 6 µm. So, layers thicknesses higher than this value have to be grown in order to go beyond the depletion layer. This is very problematic in our reactor for several reasons. Long growth time is to be avoided due to the high dirtying caused by the use of GeH_4 and to the limited life time of susceptor coverage (graphite susceptor is covered by thick pure SiC deposit to insure purity for the reactor). In addition, high growth rates should not be used because it promotes defect formation; see Figure II.10. So a trade of has to be found.

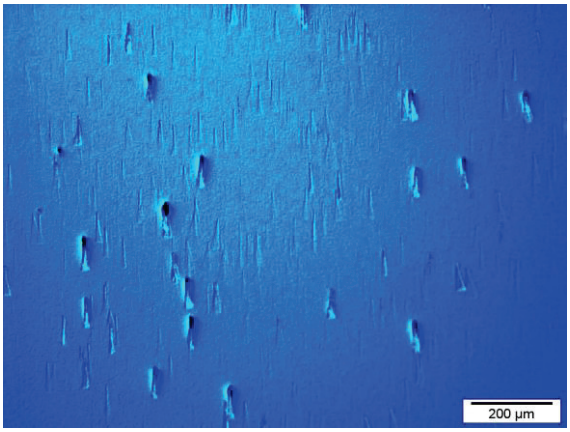


Figure II.10: 4H-SiC homoepitaxial layer grown on 8 °off-axis substrate using 6 µm/h growth rate at 1500 °C

The only remedy for this issue was to intentionally control the n-type doping by adding Nitrogen to the system. So, a flow of less than 0.5 sccm of N_2 was enough to achieve layers having doping levels in the range of few 10^{16} cm^{-3}. The depleted layer

in these samples was one order of magnitude less than that non-intentionally doped (0.6 μm).

II.6 More electrical measurements

In addition to the C-V mercury probe electrical characterization, we have performed admittance spectroscopy (AS), deep level transient spectroscopy (DLTS) and Hall Effect on specific samples. This was done during my 2 weeks stay at the applied physics laboratory in Friedrich-Alexander University - Erlangen. In this section, principles of these three techniques are presented.

II.6.1 Shallow levels and admittance spectroscopy

Semiconductor properties are strongly influenced by defects which produce levels in the bandgap. So, a complete understanding of levels is important technologically. Even now, little is known about the origin of many of them. They are often divided into two groups: shallow and deep levels. Depending on the size of the band gap, a level may be considered by its energetic location as deep in Ge or Si but may be shallow in a wide-band gap semiconductor.

The binding energies E of these donor & acceptor impurities are typically way less than the host bandgap. Thus, these impurities are often labeled “Shallow Impurities” or “Shallow Levels”. Shallow levels are intentionally introduced into the semiconductor to define the donor- and acceptor concentrations, N_D and N_A, respectively, i.e. the available charge carriers needed for conductivity. The shallow-level density can be measured from Hall or capacitance-voltage investigations, whereas the energetic location is determined by admittance spectroscopy- or photoluminescence measurements.

Admittance spectroscopy is a technique of electrical characterization, which provides the information about the shallow states in a semiconductor material. During the measurement the capacitance and conductance pair values are collected as a function of frequency and temperature. The peaks and plateaus in conductance and capacitance spectra, respectively, correspond to the shallow acceptors or donors. Using Shockley-Read-Hall statistic, activation energy of states is found from the slope of Arrhenius plot (constructed for maximal conductance-temperature pairs) and

electrical capture cross-section is calculated from its intersection with temperature axis (Figure II.11).

The energies corresponding to the nitrogen donor on hexagonal and cubic lattice site in 4H-SiC are at 53 meV and 100 meV respectively [II.18]. Admittance spectroscopy has been used to study shallow levels in n-type 4H-SiC epitaxial layer doped with Ge. Details about sample preparation can be found in the results part (Chapter III).

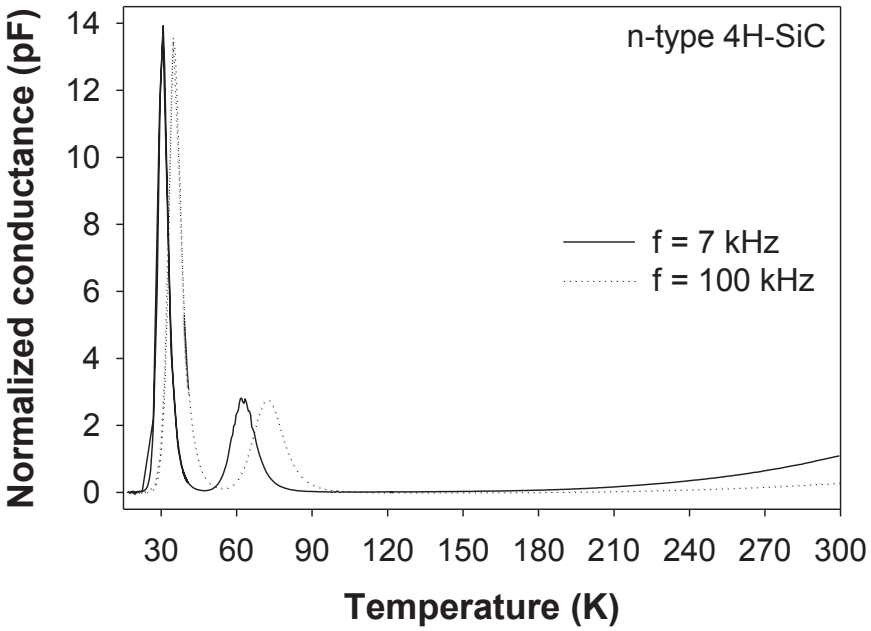


Figure II.11: G/w-T measured by admittance spectroscopy taken on Schottky contacts on with Ge at two different frequencies (7KHz and 100 KHz).

II.6.2 Deep levels and DLTS

For an ideal doped semiconductor, there is no allowed energy level inside the bandgap except the ones of the dopants. But a real semiconductor presents always other energy levels deeper in the bandgap which may come from various sources, for instance extended or points defects, or non-dopant impurities. Deep Level Transient Spectroscopy (DLTS) is a powerful tool for the study of electrically deep active defects (traps) in semiconductors, present either due to contamination (non-intentional) or intentionally incorporated (like Ge in our case). DLTS was first proposed by D. V. Lang in 1974 [II.19]. The properties of the deep level defects, such as the energy levels and concentrations, are extracted by analyzing the capacitance

transient decay of a Schottky diode after applying a reverse bias on the diode [II.17, II.19]. This is illustrated in Figure II.12. The technique of constant-voltage DLTS (CV-DLTS) makes use of the temperature dependence of the transient capacitance due to the filling and subsequent thermal detrapment of defect centers located inside an induced space charge region (SCR) while holding the applied voltage at a constant level. By measuring the transient pulse height, it becomes possible to determine the effective defect density. By measuring the transient capacitance behavior over a range of temperatures, it becomes possible to determine the associated trap activation energy and capture cross-section.

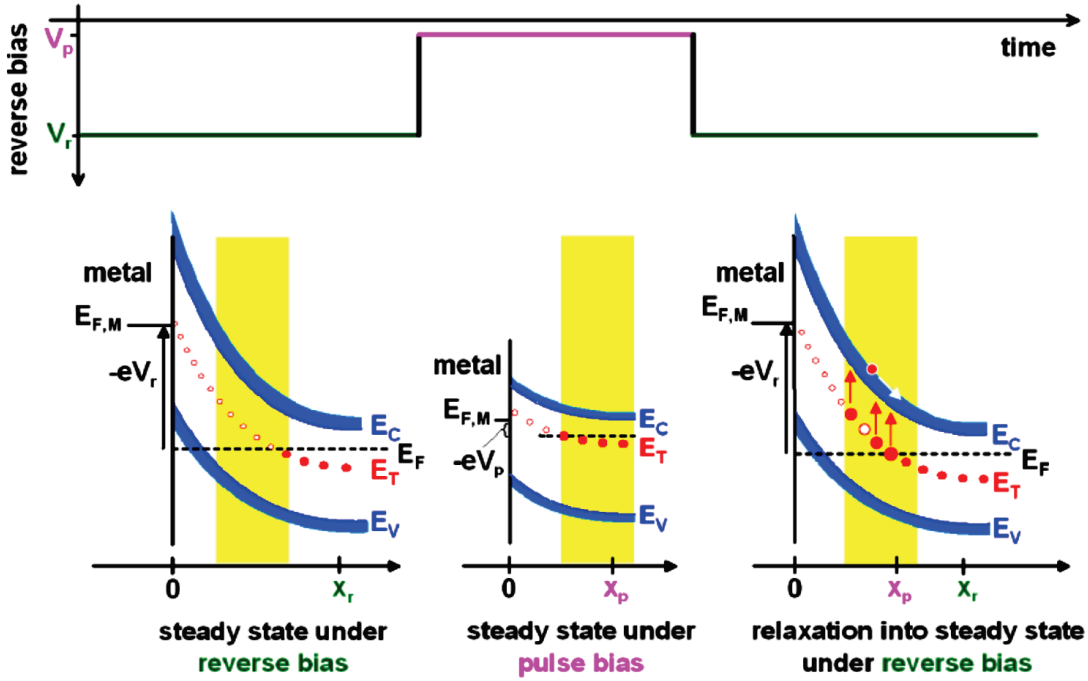


Figure II.12: Basic concept of the DLTS technique: By applying a voltage pulse, the Schottky barrier height is reduced, allowing the filling of some deep traps with electrons which are then liberated in the valence band at the end of the pulse.

In case of a wide bandgap semiconductor like SiC, the energy range in the bandgap measured from the conduction/valence band edge, which can be investigated with DLTS, is limited in most cases to 1.3 eV. The limitation is due to the fact that charge carriers have to be thermally emitted from the trap level into the respective band. As a consequence, a certain energy range in the middle of the SiC bandgap is not accessible for standard DLTS. Note also that one needs not too high a doping level in order to have reliable signal, i.e. $n < 1x10^{17}$ cm^{-3}.

For n-type 4H-SiC, deep levels located above the middle of the band gap, can be detected by a temperature scan from 85 to 700 K.

II.6.3 Hall measurements

A Hall Effect measurement system can actually be used to determine several material parameters, such as carrier mobility, carrier concentration (n), Hall coefficient (R_H), resistivity, and the conductivity type (N or P) where all are derived from the Hall voltage (V_H). Four ohmic contacts (van der Pauw configuration) are deposited on the edge of the sample to perform the hall measurements, see Figure II.13.

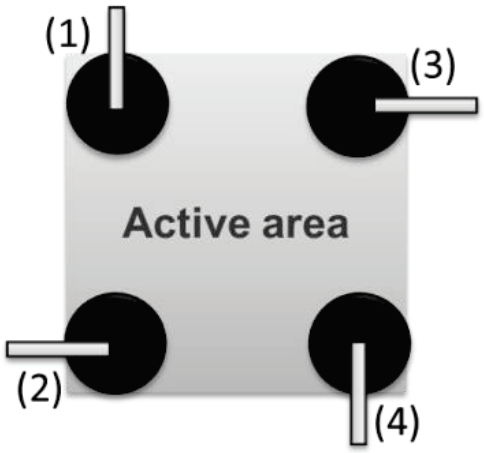


Figure II.13: Schematic illustration of the van der Pauw configuration used to perform Hall measurement.

To insure good and accurate measurements, one has to be very careful during the sample preparation. First, the Ohmic contacts need to have a good quality, with high symmetry, and equivalent size. Secondly, temperature uniformity during the measurements is another essential fact. Thirdly, accurate knowledge of thickness is highly required (resistivity and thus mobility are function of layer thickness). Finally, the sample should be uniform. Note that the layer to be analyzed has to be insulated from the substrate (if conductive substrate) or to be grown on a substrate with opposite doping type in order to avoid parasitic conduction.

In this work, Hall Effect measurements were carried out in a temperature range between 30 and 700 K under a magnetic field of 0.66 T. More details on the sample preparation will be presented in Chapter III.

II.7 Thickness calculation

Measuring the epitaxial layer thickness is vital not only for understanding and control of the process but also for better accuracy of other characterizations. For instance, accurate value of the layer thickness is needed for having reliable and precise hall measurements. In the specific case of homoepitaxial growth, direct cross sectional observation by SEM or TEM is impossible because the layer and the substrate are virtually identical. If the layer and the substrate are of opposite doping type, some contrast can be obtained by SEM [II.20]. Several in direct methods were used during this study to evaluate the as grown layer thickness. Some gives rough estimation in a routine characterization chain while others provide us with more precise values punctually.

II.7.1 Routine thickness measurement

When observing a homoepitaxial 4H-SiC layer by Nomarski microscopy, it always displays some triangular defects or carrot defects on the surface. These defects are known to generate at the epi substrate interface and propagates in the epilayer with the step flow direction reaching the top surface, see Figure II.14.

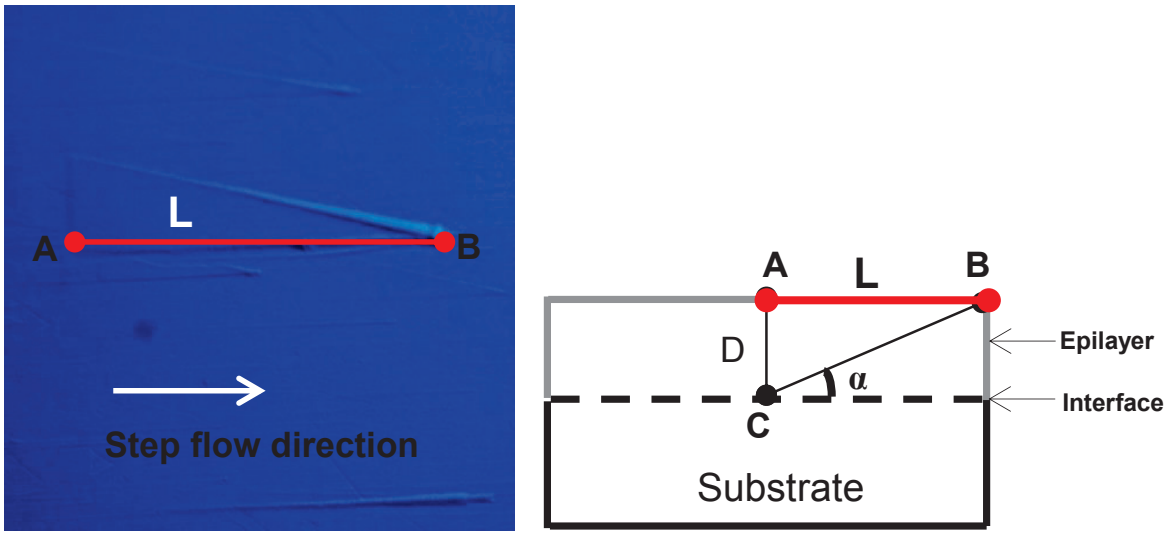


Figure II.14: Triangular defect observed in a top view by Nomarski microscopy (left) and a cross sectional drawing of this defect (right)

From Figure II.14, the layer thickness (D) is calculated according to the following equation:

$$D = L \times tan\alpha$$

Where α is the missorientation off angle of the substrate and L as illustrated in Figure II.14 is the length of the triangular defect. This thickness evaluation has the advantage to be fast that can be performed during standard layer quality inspection process using optical microscopy. The calculated values are however estimation but they give relevant information in case of unexpected growth rate variation.

Another routine technique used in this study for the layer thickness measurement is the FTIR spectroscopy. When an IR beam is focused on a sample consisting of two materials of different indexes, the beam is reflected at the various interfaces creating thus interferences. This interference spectrum is then collected and analyzed to determine the thickness "D" of the layer using the following equation:

$$D = \frac{1}{2n\Delta v}\ cm^{-1}$$

Where: n is the ordinary refractive index of the layer (2.55 for 4H-SiC) and Δv is the oscillation period (in cm^{-1}). An example of such interference spectrum is given in Figure II.15. When focusing the beam down to few tens of µm (µ-IR), it allows local measurement and thus determination of the uniformity of the deposited film. A FTIR MAGNA-IR Nicolet 560 spectrometers with a 1mW HeNe (λ = 633 nm) laser in a reflectance mode was used for routine thickness checking. The measurements were taken at atmospheric pressure in the 400–4000 cm^{-1} spectral range.

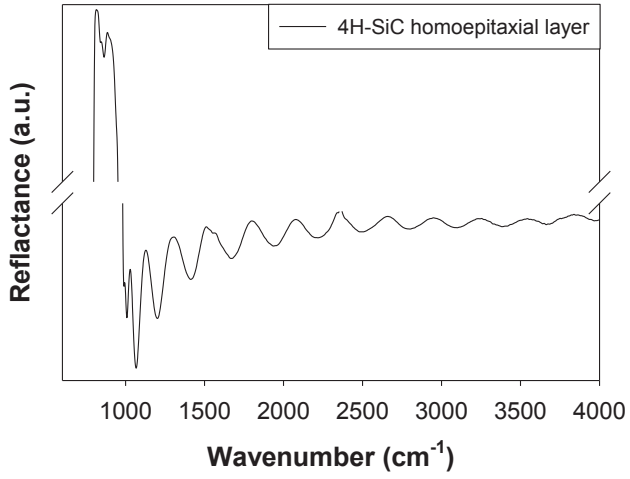


Figure II.15 µ-IR spectrum of a 4H-SiC layer grown homoepitaxially by CVD; Calculated thickness: 6.1 µm

Note that both FTIR and defect measurement approaches are fast and nondestructive. And a high correlation with $R^2 = 0.95$ was found between them, see Figure II.16.

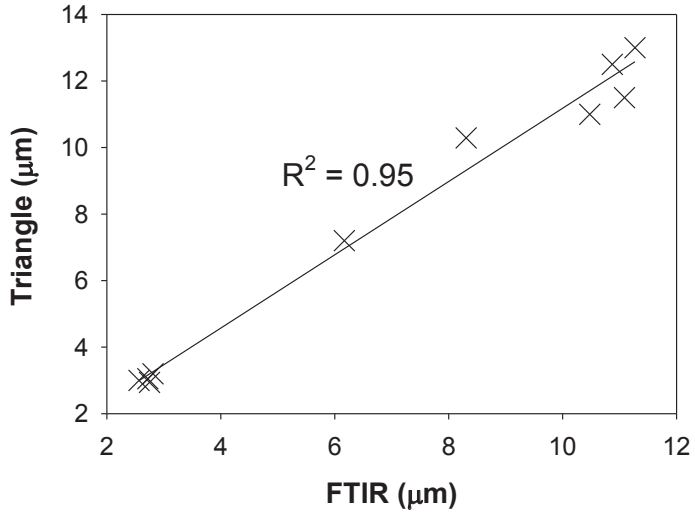


Figure II.16: Correlation between the thicknesses measured from the triangular defect and by FTIR

II.7.2 Punctual thickness measurement

As mentioned in section II.3, SIMS can give very accurate evaluation of a layer thickness if the layer is smooth and if one of the detected elements is in different concentration in the layer compared to the substrate. This is the case for Ge since it is not present in commercial SiC wafers. N impurity can also be followed if the doping level is significantly lower than the substrate doping level (typically > 10^{18} cm^{-3}). This is illustrated in the Figure II.17. The accuracy is within the tens of nm only.

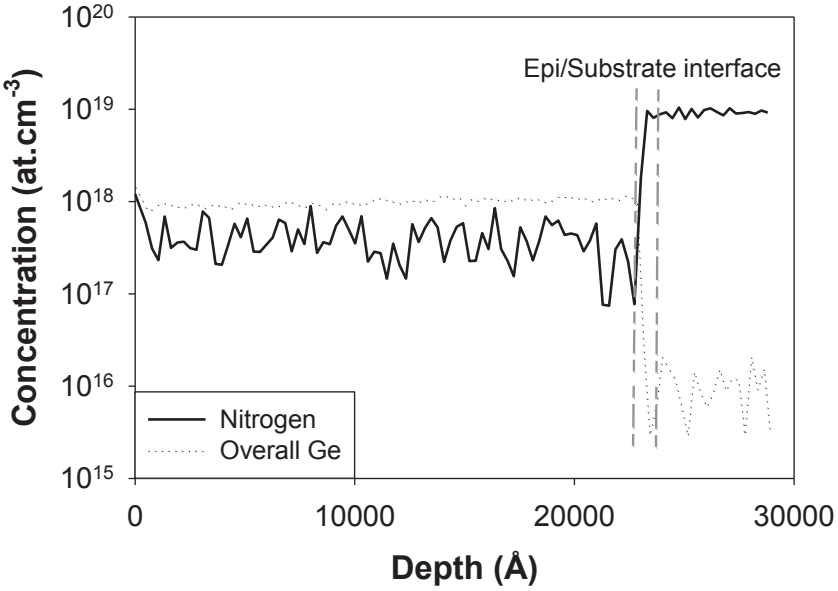


Figure II.17: SIMS depth profile taken on Ge doped sample with top layer depth of 2.3 μm

SCM measurements can be performed in cross sections to measure the variation of the capacitance along the layer thickness. If the doping type or level of the layer is enough different compared to the substrate, then the capacitance will sharply change allowing thus to locate the substrate/layer interface (see Chapter III for more detailed illustration).

In this work, SIMS was used more frequently than SCM because "less" destructive (only few craters, no sample cutting) and allowing the quantitative determination of Ge concentration. Thickness data for Hall measurement were obtained by SIMS.

II.8 Other relevant characterizations

Other techniques have also been applied to characterize the structure and optical properties of the as grown layers. They are not detailed in this chapter but briefly mentioned here under:

1) Nomarski optical microscopy (OM) and Scanning electron microscopy (SEM) for the observation of the surface morphology.

2) Transmission electron microscopy both in cross sectional and top view observations for structural evaluation of the layers and/or Ge droplets accumulating at the surface during growth. This was done at the Electron Microscopy laboratory of the Department of Physics in the Aristotle University of Thessaloniki (AUTH).

3) Electron backscattered diffraction (EBSD) for surface mapping of the grown polytype, with the possibility of separating areas with different orientation, such as on each side of a twin boundary [II.21]. The imaging was performed using a TSL (TexSEM Lab.) system installed on a Jeol 840A SEM with the Orientation Imaging Microscopy TM software was used. EBSD mappings were made on a large area up to (250x250 μm^2) with a less than 1.5 μm lateral resolution. The measurements was performed at Laboratoire des Matériaux et du Génie Physique (LMGP) – Grenoble.

4) Low temperature photoluminescence (LTPL) technique for the quality and purity of the grown homoepitaxial layer with and without Ge incorporation. Spectra were collected using 30 mW of the 244 nm wavelength of a FreD (Frequency Doubled) Ar+-ion laser as an excitation source. A Triax spectrometer from Jobin-Yvon Horiba fitted with a 600 gr/mm and 2400gr/mm gratings and a cooled CCD camera completed the set-up. The measurements were done at 5K temperature in the wavelength range between 380-700nm. This measurement was conducted at Laboratoire Charles Coulomb (L2C) in Université Montpellier 2.

II.9 Epitaxial growth apparatus - CVD

II.9.1 Description of the apparatus

For the epitaxial growth of all the SiC layers, home-made CVD epitaxy equipment working at atmospheric pressure was used. The CVD apparatus is shown in Figure II.18.

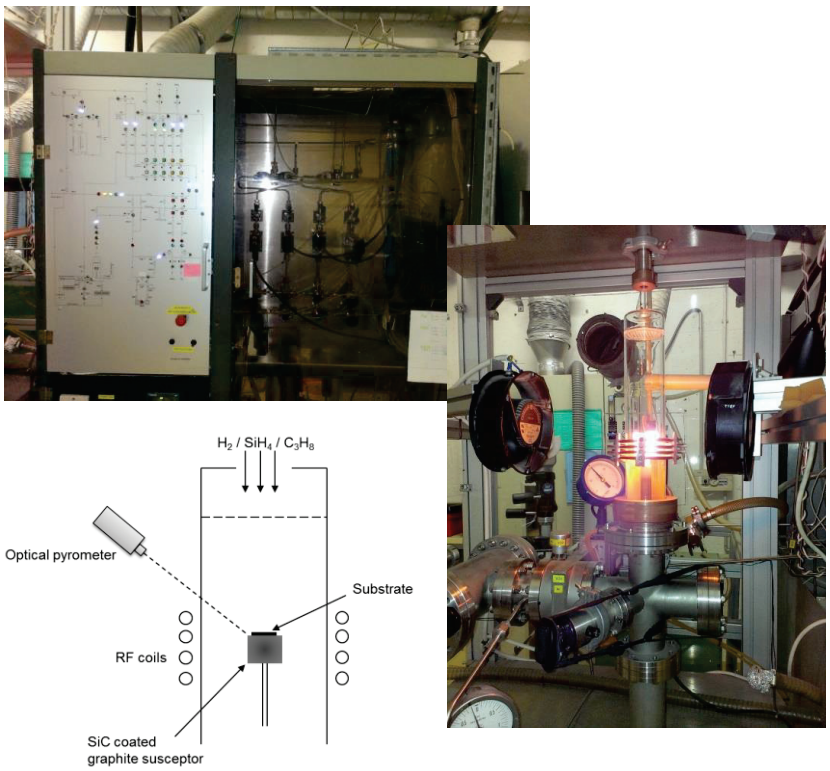


Figure II.18: Schematic representation of the CVD reactor and pictures of the CVD apparatus

It consists of two chambers; the reaction chamber where the deposition takes place and a transfer chamber denoted by “SAS” used for sample introduction. This

equipment respects all the safety rules for growing semiconducting thin films. That is why after apparatus disassembly and assembly, the reactor and the gas lines are checked using a helium leak detector. This also insures the semiconductor grade of the gases.. It can be divided into five main parts, which are: 1) the heating system; 2) the gas distribution; 3) the pumping system; 4) the SAS and reaction chamber 5) the cooling system and 6) the graphite components. All these parts will be described and/or discussed below.

The heating source is a 50 kW RF induction generator (Celes - 50 kW) which heats by radiofrequency the graphite parts inside the reactor. The temperature is read by an optical pyrometer (IRCON Infrared Mirage) working in the range of 750-2400 °C and the temperature is controlled and monitored by a PID interface (Eurotherm 2404) controller.

The main advantage of using such remote heating is that the coils are located outside the reaction chamber, so that one can work with a controlled atmosphere without risk. Furthermore, it allows the use of inexpensive and easily machined graphite parts to be heated.

The gas distribution is composed of five different gas lines: silane (SiH_4 - 1 % diluted in H_2), propane (C_3H_8 – 5 % diluted in H_2), Germane (GeH_4 – 1 % diluted in H_2), Nitrogen (N_2 – 5 % diluted in H_2) and Hydrogen (H_2) and Trimethylaluminium (TMA). In all lines, pneumatic and manual valves are strategically located to insure the right distribution of the gases (see Figure II.19).

The flows of all gases are controlled by different mass flow controllers (Brooks 5850E and 5850TR) which are calibrated for each gas. Table II.13 summarize the technical parameters for each gas.

Table II.3: Flux ranges and purity of each gas used in this work

Gas	Dilution	Mass flow	Effective precursor flux	Purity
H_2	-	30 slm 2 slm	30 slm 2 slm	Purified to electronic grade
Ar	-	10 slm	10 slm	electronic grade
C_3H_8	5 % in H_2	500 sccm 50 sccm	25 2.5	N35
SiH_4	1 % in H_2	500 sccm 50 sccm	5.0 0.5	Electronic grade
GeH_4	1 % in H_2	20 sccm	0.2	-
N_2	5 % in H_2	50 sccm	2.5	-

For H_2 gas, a set of bottles is located outside the building, with a quality/purity of Alphagaz 1 (5 ppm of oxygen). The gas passes through a NUPURE III Omini TM purificator which removes oxygen and also nitrogen down to the ppb level. Argon gas is used in the transfer chamber.

The pumping system is composed of a 63 m^3/h rotary pump (rough pump) with a base pressure limit in the 10^{-3} mbar range. It is directly connected to the transfer chamber (SAS) and isolated by manual valve.

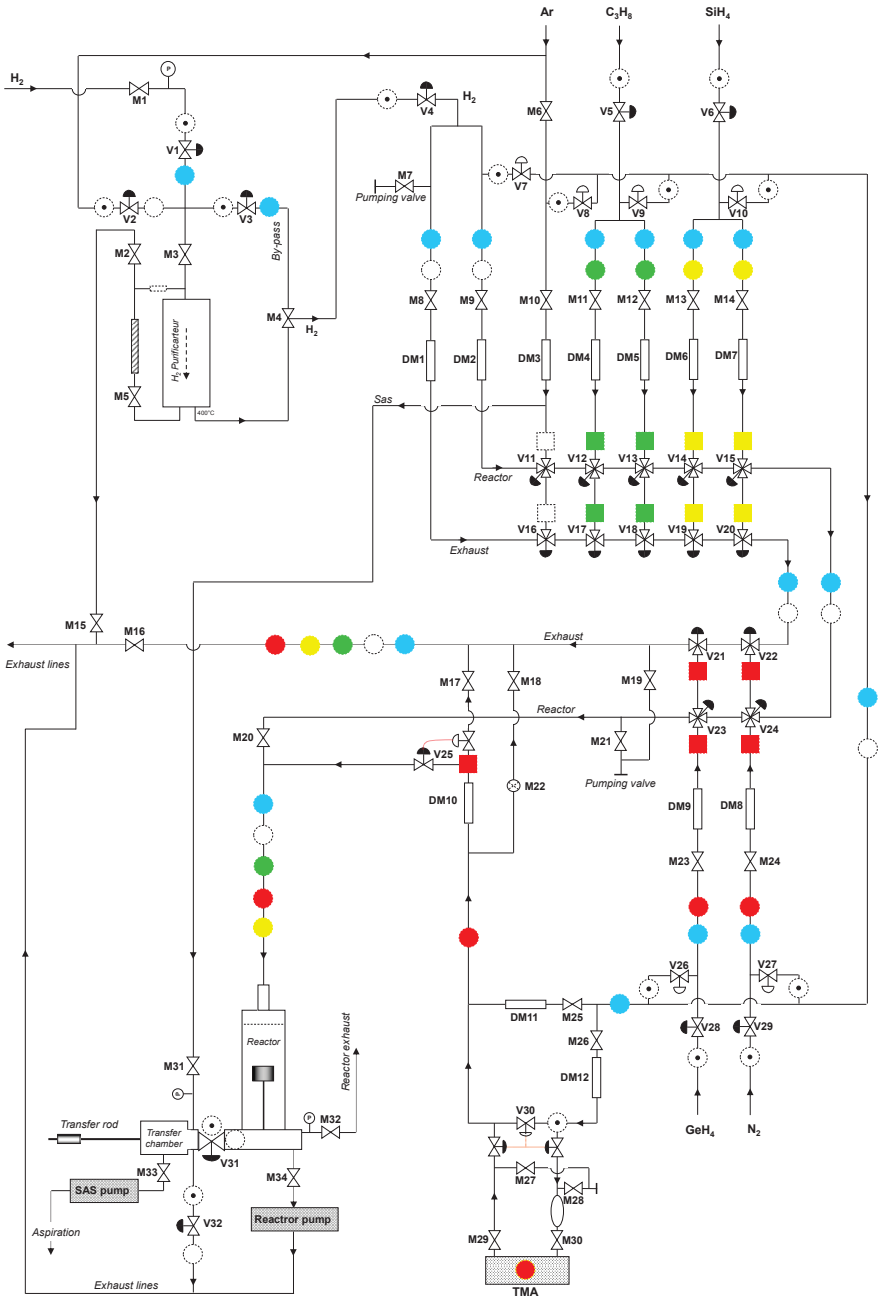


Figure II.19: Schematic detailed sketch of the CVD equipment

The CVD machine is constituted of a 70 mm diameter vertical cold wall reactor made of quartz equipped with a homogenization grid on the upper part of the reactor. The samples were placed on the top of the cylindrical SiC covered graphite susceptor (40 mm diameter). The reaction chamber is never opened to air in order to insure high purity. Thus, the graphite susceptor is transferred to the reactor by a transfer rod via a lock chamber (sas). Before opening the lock sas to the reaction chamber, 3 l/min flow rate of H_2 is maintained in the reaction chamber and equivalent amount of Ar is placed in the sas. And since both chambers are in a horizontal configuration, then no gas exchange would occur. The typical sample size was 1x1 cm^2 and a maximum of 35 mm diameter wafer of Si was used. Note also that before introduction into the reactor, the substrates are degreased in methanol ultrasonic bath.

Since a relatively high growth temperature (≥1450˚C) is used in this reactor, therefore the use of robust cooling system is a must. The cooling system is of two parts; water and air cooling. The water circulates in the base part of the reactor. And, two small fans are mounted opposite to each other and on one axis. They are supported by a huge fan on the other axis; this fan is only turned on if the growth temperature went beyond 1200˚C.

The graphite parts (susceptor holder, graphite rod) are machined at LMI using high purity graphite cylinders (CX 2123 - Carbone Lorraine). The 40 mm graphite susceptor is covered by 250 µm SiC thick layer. Both the graphite susceptor and the SiC layer are of high purity. Table II.4 depicts the impurity content of the SiC coating. It was bought from TOYO TRANSO CO., LTD.

Table II.4: Impurity analysis of SiC coating

Element	Content (ppm)
B	0.15
Na	0.02
Al	0.01
Cr	0.01
Fe	0.02
Ni	<0.01

Considering GeH_4 and SiH_4 as hazardous and flammable gases, a NaOH containing bubbler is connected after the exhaust lines for the purpose of treating the unreacted and unwanted species in the ambient. The NaOH is changed from time to time.

II.9.2 Precursors and substrates

While high purity hydrogen (H_2) with 16 slm was used as a carrier gas. A SiH_4 (1 – 5 sccm), C_3H_8 (2.1 – 8.33 sccm), N_2 (0.15 – 0.5 sccm) and GeH_4 (0.01 – 0.20 sccm) were used as precursors for the SiC growth.

For all experiments, commercial α-SiC wafers brought from SiCrystal Inc, were used as substrates. After reception, the 2 or 3 inches diameter wafers were sent directly to NOVASiC Company (NetFiSiC partner), where a well mastered polishing process called StepSiC® was performed. Briefly, StepSiC consists in chemical/mechanical polishing steps which allows the elimination of the surface scratches left by suppliers' basic polishing. The calculated average roughness (RMA) is always below 1 Å. Wafer cutting was performed after the StepSiC polishing.

The 4H-SiC (0001) and 6H-SiC (0001) wafers, were of different off orientations (nominally on axis, 1˚, 2˚, 4˚ and 8˚) mainly Si and in rare cases C face only for the 8˚ miscut 4H-SiC. The missorientation is always toward [11-20].

The carbon to silicon ratio (C/Si) was varied by changing only the propane flux and keeping the same silane flux.

II.9.3 Quality control of the reactor

The deposition of SiC at growth temperatures up to 1650 °C using SiH_4 and C_3H_8 as precursors causes parasitic deposition on the side walls (Figure II.20). This deposit restricts significantly both the pyrometric temperature measurement and reactor lifetime. Upon every change, an outgassing of all lines and reactor itself is conducted. And, the system goes for a very effective leak test using He detector. Likewise, to insure reactor cleanliness, a blank SiC growth at 1500 °C is performed after each changing. Then a 3C-SiC heteroepitaxial growth on Si is performed to check the working conditions. Indeed, such growth is very sensitive to parameter change such as precursors flux, temperature variation, impurities (leak), growth rate …etc. The growth conditions involve a two-step proceducre described elsewhere [II.22].

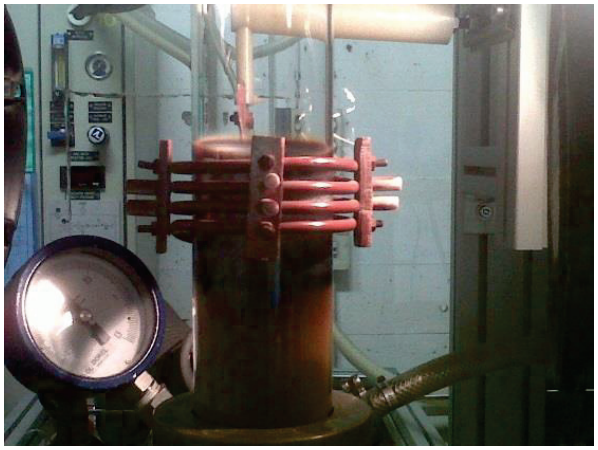


Figure II.20: State of the reactor after several growths with Ge (deposit on the side walls)

A simple look to the surface morphology after growth (Figure II.21) and to the thickness is enough to validate (or not) the use of the mounted reactor (and validity of other parameters). The final step involves growing a homoepitaxial layer of 4H-SiC at the typical growth conditions (T = 1500 °C and C/Si = 5) to check the background doping of the reactor, which should be n type and in the order of few 10^{15} cm^{-3} or below.

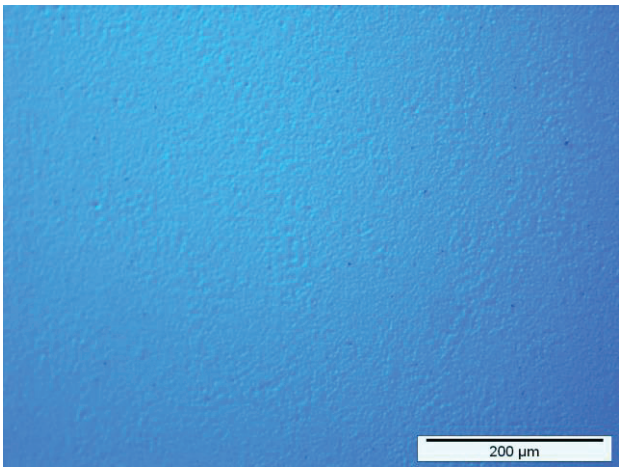


Figure II.21: Surface morphology of 1 µm thick 3C-SiC layer grown on Si (100) wafer at 1350 °C in 1 hour

II.10 Conclusion

This chapter was dedicated to the technical description of the various apparatus used in this study. The most employed characterization techniques are exhaustively described. Some of the used characterization tools are available at the vicinity of the laboratory and few within NetFiSiC network. A literature recall on the uses of these

techniques in SiC field was also mentioned. The chapter ends with a brief description of the epitaxial system. More details on the epitaxial growth procedure and parameters will be described in the results chapters (Chapter III and Chapter IV).

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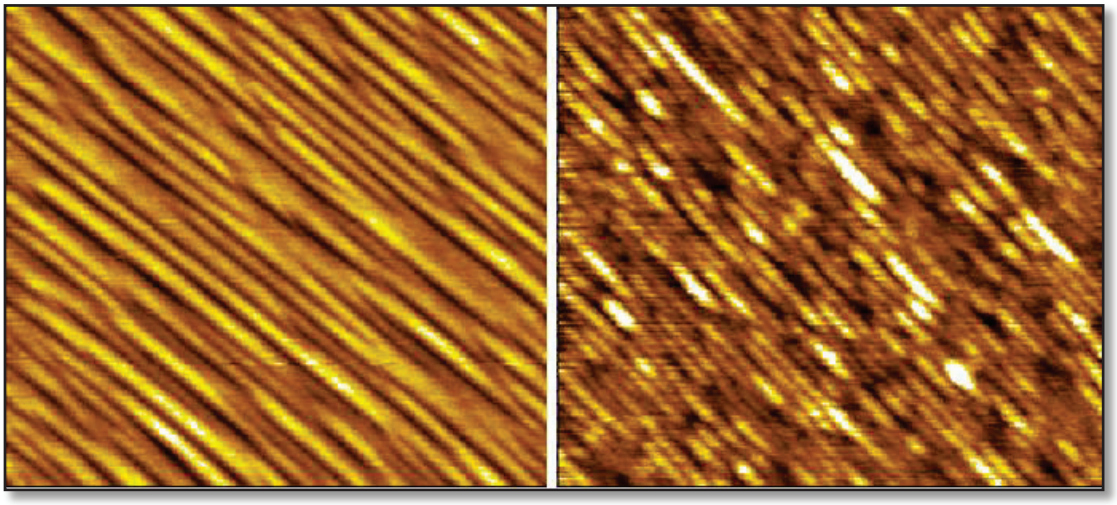
Chapter III

Ge incorporation during 4H-SiC homoepitaxial growth by CVD



Chapter III: Contents

Chapter III: Ge incorporation during homoepitaxial 4H-SiC growth by CVD

This chapter deals with the experimental study of in situ Ge incorporation into 4H-SiC during homoepitaxial growth by CVD. This is a rather unexplored topic addressing mostly fundamental aspects but with some results which might be of great interest to the SiC community. This Ge doping was implemented by adding GeH_4 to the standard SiH_4-C_3H_8-H_2 chemistry. Comparison of layers properties, with and without GeH_4 addition, will be studied. The level of Ge incorporation into 4H-SiC will be followed as a function of growth parameters. Electrical and optical characterizations performed on such Ge doped layers will be presented at the end of this chapter. I have participated to most of these characterizations through secondments inside NetFiSiC network.

III.1 Growth procedure

All the samples are cleaned in methanol bath and rinsed in ethanol just before being introduced to the reactor. The standard procedure for homoepitaxial growth of 4H-SiC procedure is represented in Figure III.1.

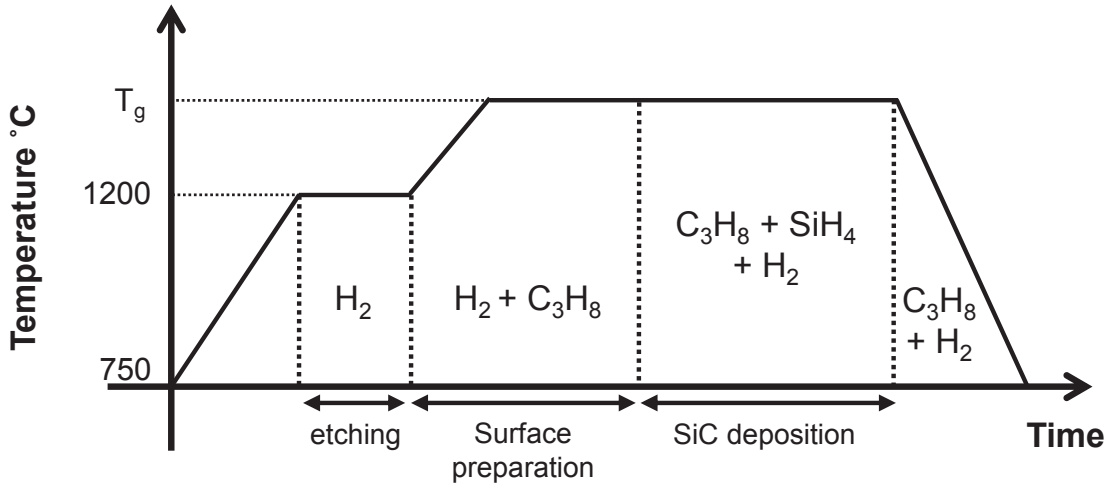


Figure III.1: CVD Epitaxial growth procedure

At first, the heating rate is fixed at 6 °C/sec under pure H_2 flow (16 slm). One of the most important process parameter, though rarely detailed, is the preparation of the

surface prior to the start of the epitaxial growth. The used CVD growth procedure consists of two main stages. It first initiates with in-situ desoxydation/cleaning of the substrates at 1200 °C under H_2 for 5 min. Subsequently, the temperature ramps at 6 °C/sec under H_2+C_3H_8 up to the growth temperature. Then, H_2+C_3H_8 atmosphere is kept for 10 minutes always using the 16 slm H_2 and the desired flux of propane during the deposition. These steps are called the in situ surface preparation (S.P) because its main task is to prepare a clean and smooth surface for commencing the epitaxial growth. The annealing of the substrate under H_2+C_3H_8 using the same growth temperature as for the growth was selected because [III.1]:

1) It helps in reducing the epilayers surface roughness,
2) It limits the substrate imperfections before the deposit and thus improve the layer quality
3) It restricts the etching of SiC coverage of the susceptors and thus increases their life time.

In the literature, there exists several mixture of gases used for the in situ surface preparation. Some procedures involve the use of only H_2 [III.2] or H_2 + HCl [III.3] and others utilize H_2 + C_3H_8 [III.4].

Finally, the SiH_4 is then added to the reactor and the epitaxial growth of SiC takes place. At the end of the deposition the reactor is cooled down under H_2+C_3H_8 down to 750 °C in order to avoid any surface degradation (possible Si droplets formation) of the surface.

III.2 Standard homoepitaxial growth (without Ge)

This section is devoted to the study of homoepitaxial growth of 4H-SiC on off-axis seeds without Ge addition. These results are rather standard but their recalling is essential because they will be used later on as a “reference” to rule on any influence of Ge. The effect of growth conditions and substrates crystallographic parameters (substrate off orientation and polarity) on the growth rate, surface defects and n-type doping of the homoepitaxial growth of 4H-SiC is checked. Growth conditions includes: growth temperature, growth rate, C/Si ratio and N_2 flux.

III.2.1 Epitaxial layer characteristics (non-intentionally doped)

Most of the samples were grown on 8° off axis (toward [11-20]) Si face 4H-SiC seed. Growth parameters of the discussed grown samples are presented in Table III.1. All the layers shown in Table III.1 are non-intentionally doped (n-type).

Table III.1: Growth conditions and parameters

Name	Off orientation	Polarity	T (°C)	C/Si ratio	Time (min)	SiH_4 (sccm)	t (µm)	Gr (µm/h)
Ref 1	8°	Si face	**1500**	3.5	120	5.00	12.5	6.25
Ref 2	8°	Si face	**1550**	3.5	60	5.00	6.20	6.20
Ref 3	8°	Si face	**1600**	3.5	60	5.00	6.10	6.10
Ref 4	8°	Si face	1500	3.5	180	***1.67***	***6.50***	***2.16***
Ref 5	8°	Si face	1500	3.5	100	***3.33***	***6.60***	***3.96***
Ref 6	8°	Si face	1500	*2*	120	5.00	12.5	6.25
Ref 7	8°	Si face	1500	*5*	120	5.00	12.5	6.25
Ref 8	4°	Si face	1500	5	60	5.00	6.00	6.00
Ref 9	8°	C face	1500	5	60	2.50	3.00	3.00

*t: layer thickness measured by µ-IR spectroscopy, **Gr: Growth rate

The surface morphology of all the grown layers is rather standard and characterized by the presence of triangular shape defects (TD) which were judged as 3C inclusions. Influence of growth temperature and growth rate on density of surface defects measured by Nomarski microscope was investigated. The surface morphology of two layers grown at a growth temperature of 1500 °C and C/Si ratio of 5 but with relatively low growth rate (2.5 µm/h) and high growth rate (6 µm/h) is shown in Figure III.2.

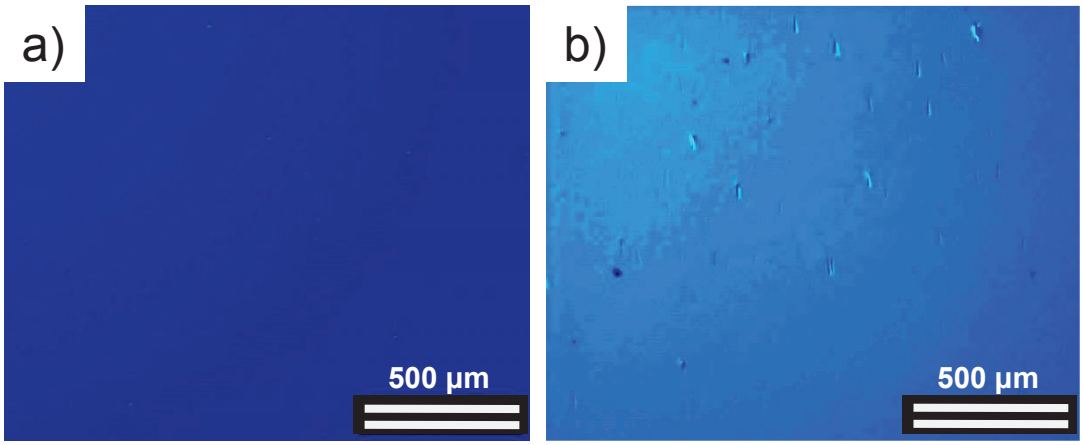


Figure III.2: Optical image of two layers grown at 1500 °C and C/Si ratio of 5 but with a) Growth rate = 2.5 µm/h, b) growth rate = 6 µm/h

We have found that density of TD diminishes with both the increase of growth temperature and the decrease in growth rate (Figure III.3 and Figure III.4). This is not surprising because both changes result in higher adatoms mobility and therefore the 3C inclusions are less favored. Moreover, no significant impact of growth temperature on the growth rate is seen since in this temperature region the process is under mass transport regime [III.5]. It is also worth mentioning that the growth rate linearly increases with SiH_4 flux (Table III.1), which is logical when considering the C rich growth conditions.

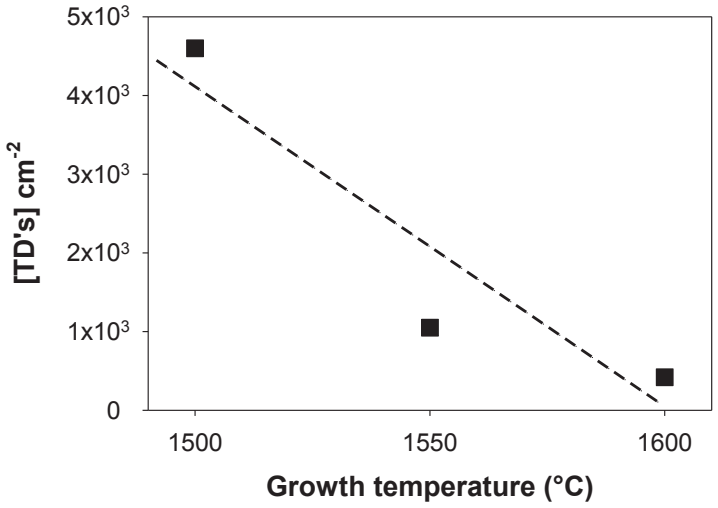


Figure III.3: Density of triangular defect as a function of growth temperature for C/Si ratio = 3.5 and growth rate of 6.25 µm/h

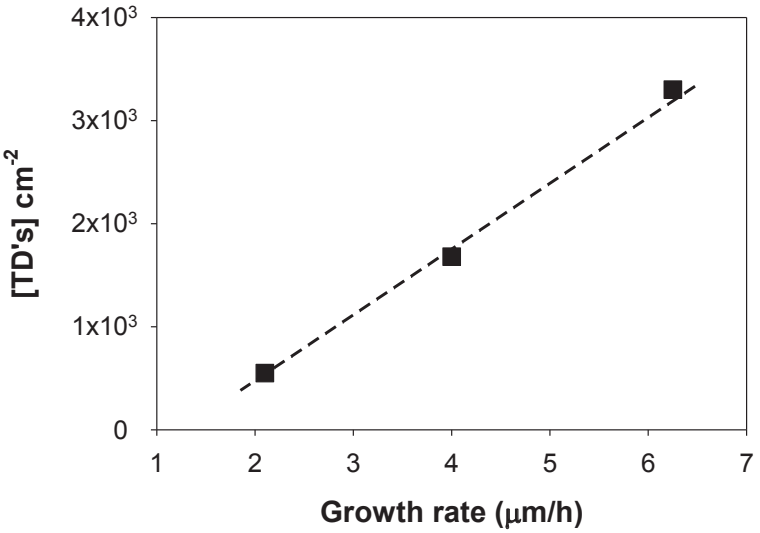


Figure III.4: Density of triangular defect as a function of growth rate for C/Si ratio = 3.5 and growth temperature of 1500 °C

As mentioned in chapter II, when the layers are not intentionally n-type doped, they can be extremely pure and sometimes too pure to be probed by C-V measurements. However, measuring the doping level is essential for knowing the base purity of the reactor. That is why layers as thick as 12 µm were grown at rather "high" growth rate of about 6 µm/h (this is high for our reactor using the standard chemistry and working at atmospheric pressure). This is the case of samples Ref 1, 6 and 7.

Figure III.5 show the C-V measurement of one of the purest layer (Ref 7) grown in this study and displaying N_d-N_a value as low as $5x10^{13}$ cm^{-3}. One may say that such measurement might hide a high compensation level of the layer since one measure only N_d-N_a. So, the nitrogen concentration in "Ref 7" sample was investigated using Low temperature photoluminescence (LTPL).

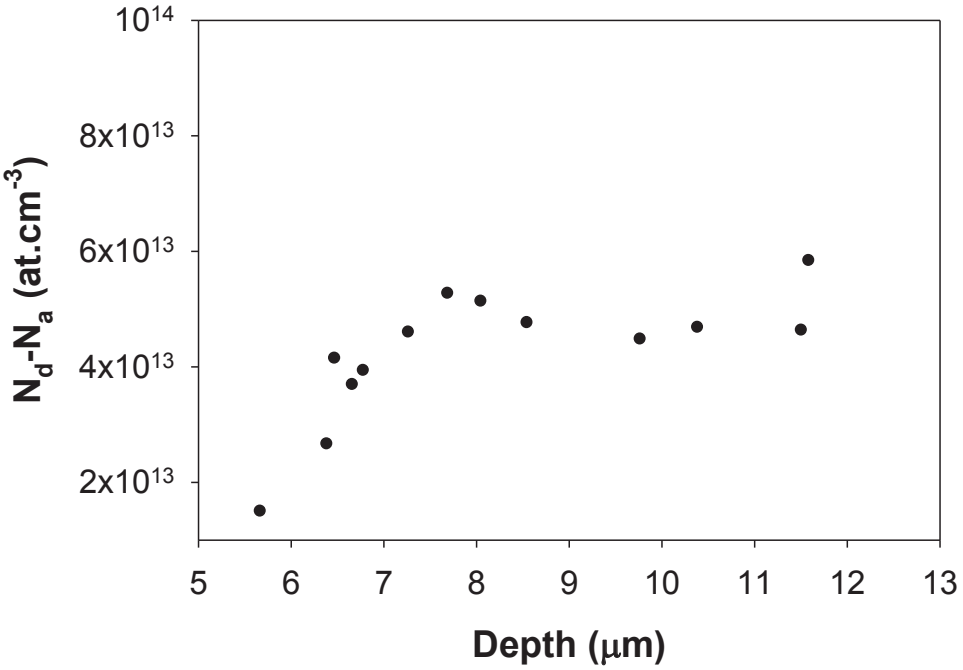


Figure III.5: C-V measurements on sample "Ref 7"

Figure III.6 show the PL spectrum obtained on such sample which displays sharp near bound edge exciton (NBE). Using the peak that is situated at 388.9 nm and which corresponds to I_{77}, the calculated nitrogen concentration was estimated to be 2.6×10^{14} cm^{-3} [III.6]. No significant donor-acceptor pair (DAP) was detected meaning that the level of compensation is low.

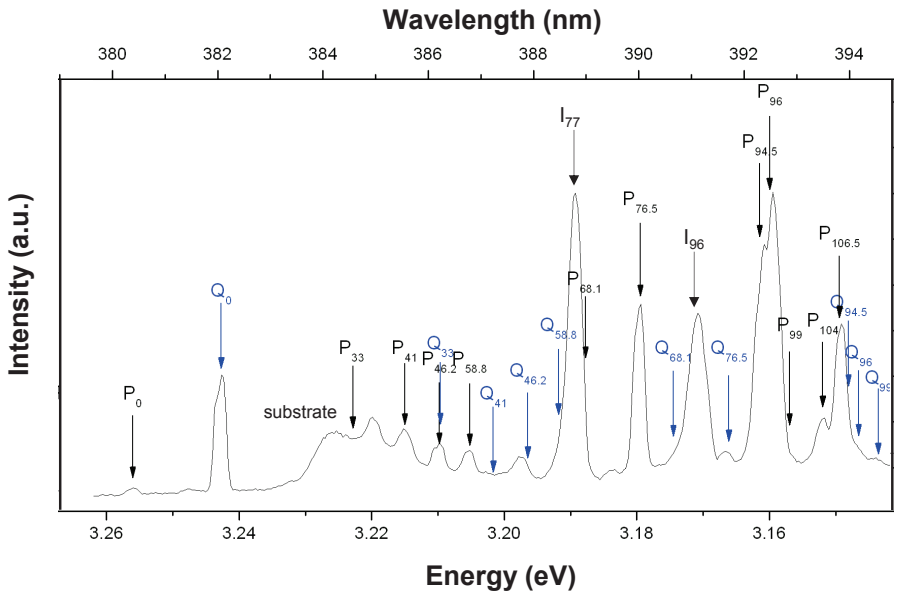


Figure III.6: LTPL spectra collected at 4 K on "Ref 7" sample in range 387-395 nm

Though the actual substrate standard misorientaion is 4° off, we mainly used 8° off axis substrates because the parameters window for obtaining good layers with smooth surfaces is wider. This is illustrated by Figure III.7 where the use of 4° off substrate led to a very rough surface while using identical growth conditions as in Figure III.2b (sample Ref 7). Such layer contains a very high density of defects leading to 3C inclusions.

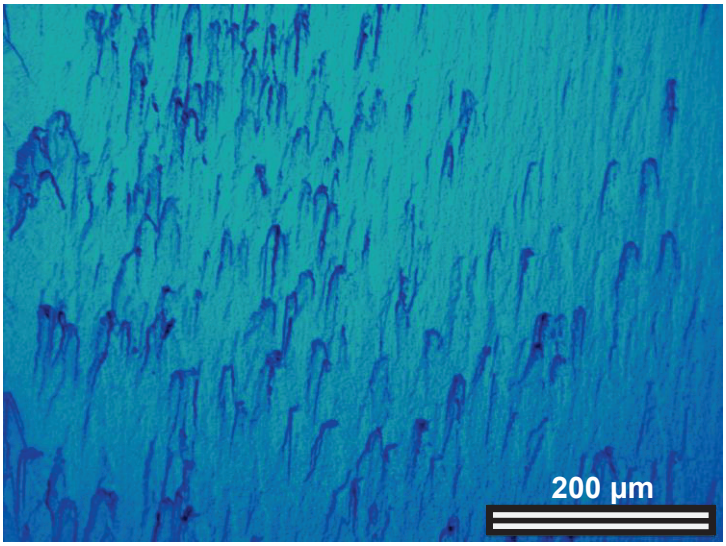


Figure III.7: Surface morphology after CVD growth on 4°off axis seed "Ref 8" with identical conditions as in Figure II.2b (sample ref 7)

While the low off orientation seed suffers from serious surface morphological issues, the C face has a doping level of about 2 orders of magnitude higher than that

of Si face. The doping level of this layer is determined by Raman spectroscopy applying the same method presented in reference [III.7]. Moreover, it has a high density of surface defects (Figure III.8). The origin of these defects which are 3C inclusions is not yet known and we speculate that either the quality of the substrate or of the polishing stands behind it.

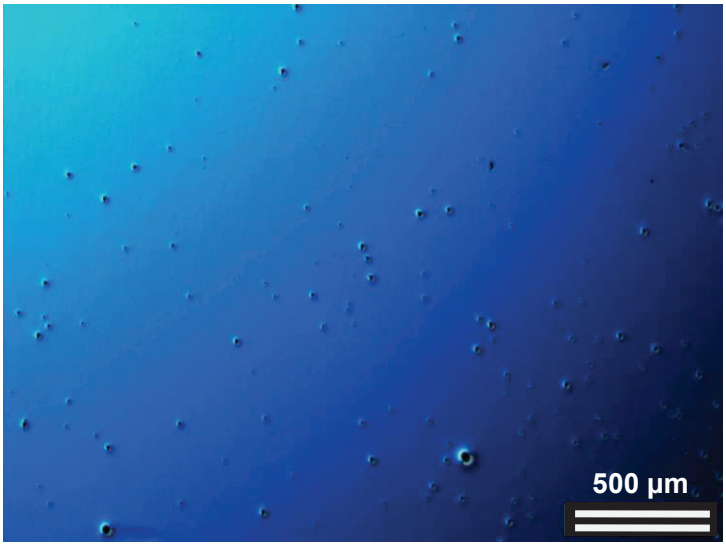


Figure III.8: Surface morphology after CVD growth on C-Face 4H-SiC 8° off-axis substrate, "Ref 9"

III.2.2 Intentional nitrogen doped layers

Demonstrating high purity layer growth is indeed essential for validating the reactor use. But for most of the electrical characterizations performed in this work, such high purity layers are of no use:

1) Too deep depletion when using C-V measurement or when making Schottky contact
2) Impossibility to make any Ohmic contact

That is why intentional n-type doping using N_2 gas was almost systematically performed during epitaxial growth, unless specified differently. N_2 flux was varied from 0.1 – 2.5 sccm. The target of n-type doping being in the $\approx 10^{16}$ cm^{-3} range, the evolution of this doping was studied for low N_2 flux (Figure III.9). One can see that N concentration increases with N_2 flux; this is of course a classical trend for the dopants [III.8 - III.10]. When changing the reactor, this curve remains more or less similar with some small changes from time to time. Note that N_2 addition does not deteriorate the layers morphology within the studied N_2 flux range.

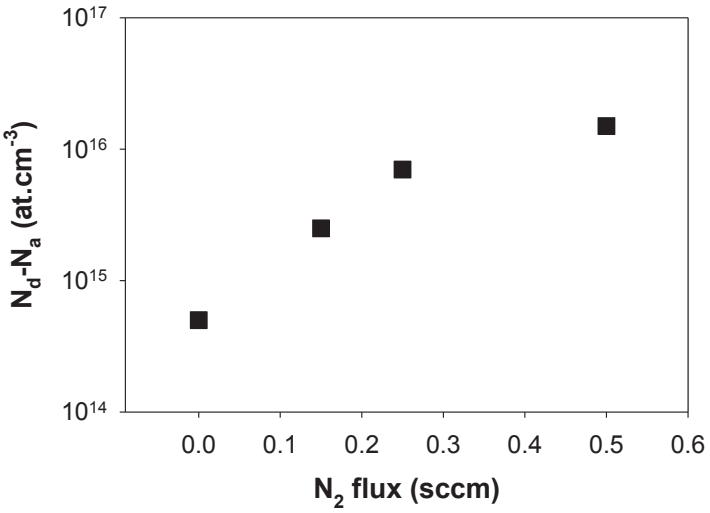


Figure III.9: donor concentration vs. N_2 flow rate in epitaxial growth of 4H-SiC for C/Si = 5, T = 1500 °C and 2.5 sccm SiH_4.

III.3 Homoepitaxial growth with Ge

After summarizing the data from the standard homoepitaxial growth of 4H-SiC in our reactor, the results collected on the growth of Ge doped 4H-SiC homoepitaxial layers will be presented. An important part of this section will be dedicated to the Ge incorporation evaluation and discussion on the mechanisms.

III.3.1 Influence of Ge addition on the layer

Let us first start by comparing Ge and non-Ge doped layers without any other addition (N_2 flux = 0) in order to avoid any unexpected interaction. The surface morphology of a Ge-doped layer is shown in Figure III.10.

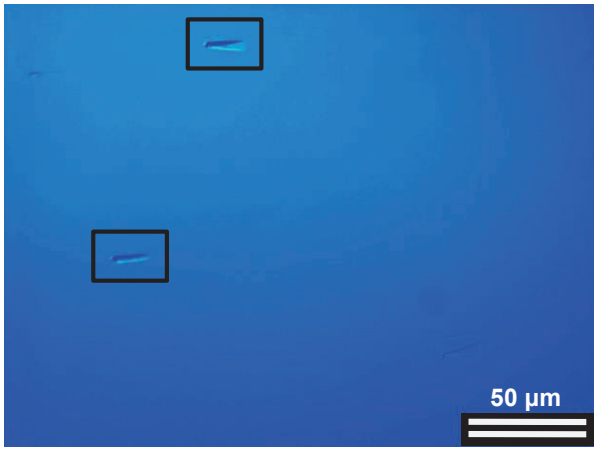


Figure III.10: Nomarski optical images after homoepitaxial growth at 1500°C using C/Si ratio of 5, growth rate of 2.5 µm/h and GeH_4 = 0.02 sccm. Squares ares marking the triangular defect place.

On a low magnification scale, the surface morphology is rather standard with no significant evolution even at the maximum GeH_4 flux value (0.10 sccm). Typically, at a temperature of 1500 °C and 2.5 µm/h growth rate, the density of triangular and carrot defects on the Ge and non-Ge containing epilayers is found to be similar, in the 400 – 600 cm^{-2} range depending on the C/Si ratio.

µ-Raman analyses were performed in order to obtain local information about the grown Ge doped layer and to check the possibility of Ge detection in the same manner as in the case of 3C-SiC grown from VLS transport using SiGe melt [III.7]. The recorded Raman spectrum (Figure III.11) is rather standard showing only the peaks related to 4H polytype.

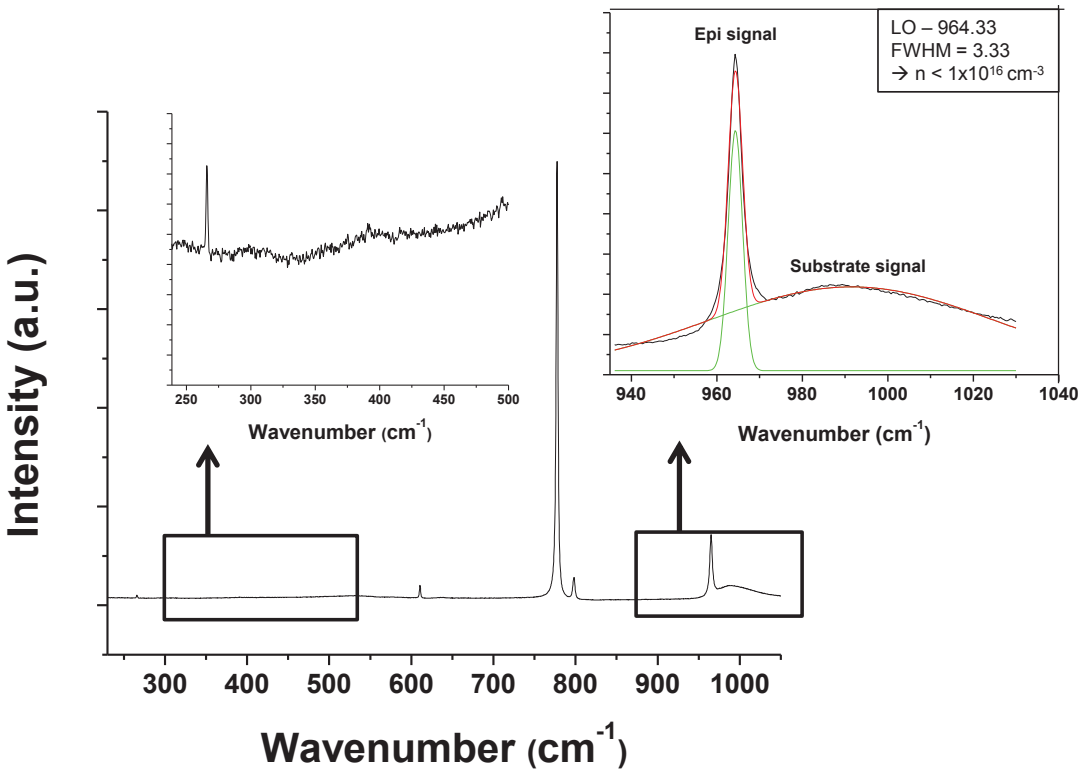


Figure III.11: µ-Raman spectrum collected on n-type Ge doped sample

Figure III.11 shows highly intense TO_{777} and narrow LO_{964} peak located exactly at 964.33 cm^{-1} having full with half maximum (FWHM) about 3.3 cm^{-1}. With these values, the residual n-type doping was estimated to be at the detection limit, i.e. around or below mid 10^{16} cm^{-3}. This is consistent with the non-intentional doping of these layers during growth. Moreover, in the range between 250 – 500 cm^{-1}, in which Ge or SiGe signature must appear, no peak is recorded except the TA peak of 4H-SiC

presented at 266 cm^{-1} (Figure III.11). The spectrum is not distorted in contrary to what was seen after Ge implantation of 4H-SiC [III.11].

Figure III.12 shows IR spectra taken on two samples grown under identical conditions with one Ge doped and the other not. The measured thickness was 2.5 µm for both samples. This implies no impact of GeH_4 addition on the growth rate. For both spectra estimation of the doping level (as proposed in Reference [III.12]) did not give any difference because they are below the limit of detection of this approach (low 10^{16} cm^{-3}).

Also, both spectra reveal identical axial folded-transverse-optic (FTO) mode which corresponds to 4H-SiC at 838 cm^{-1} [III.13]. This does not match with the observed reduction or broadening in this peak for the Ge doped sample grown by Dashiell et al [III.14] using ion implantation.

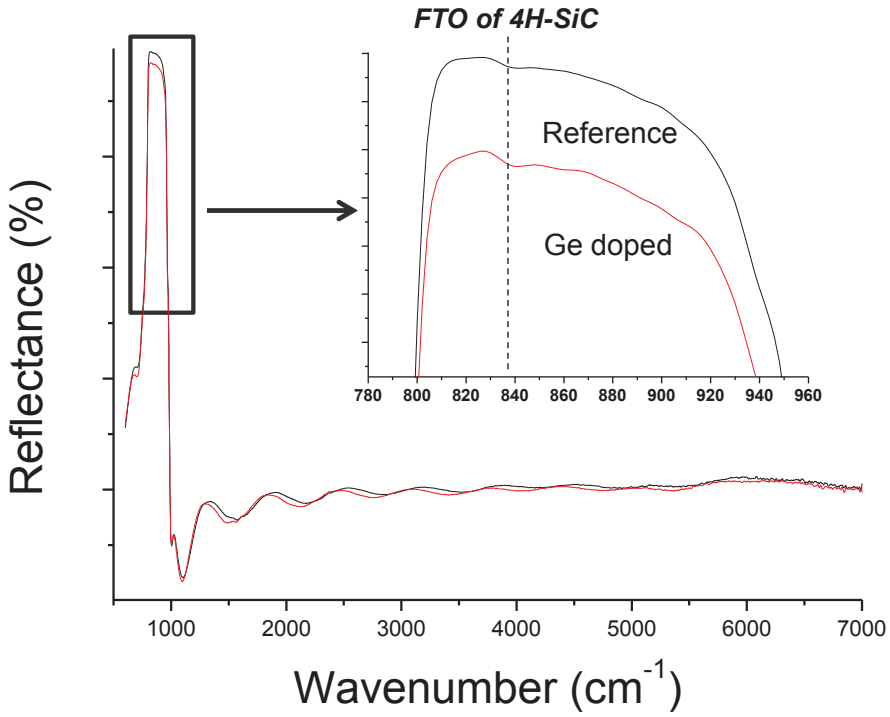


Figure III.12: µ-IR spectra collected on reference and Ge doped samples, the zoomed area shows the reflectance in the Reststrahlen band

Since these layers are rather pure (No N_2 addition), C-V measurement is of no help for accurate estimation of the type and level of residual doping. LTPL can be used for such evaluation in addition to the fact that it can also allow detecting new features (if any) which could be attributed to Ge incorporation.

The LTPL spectrum were collected at 5K temperature on a typical Ge containing sample in the wavelength range between 380-700nm. It showed that the layer is of high purity ($n < 10^{15}$ cm^{-3}), with rather low compensation (Figure III.13). The estimation of Al level was not possible because it was found to be very low. This is seen at low energy, where no signal can be associated with the presence of N-Al donor-acceptor pairs (DAP), which exclude any idea about layer purity degradation due to Ge presence inside the lattice. Besides, no unknown peak that could be related to the presence of Ge atoms was identified within the energy range. In summary, Ge doped layer can be of high quality and low doping level, alike the non Ge-doped ones.

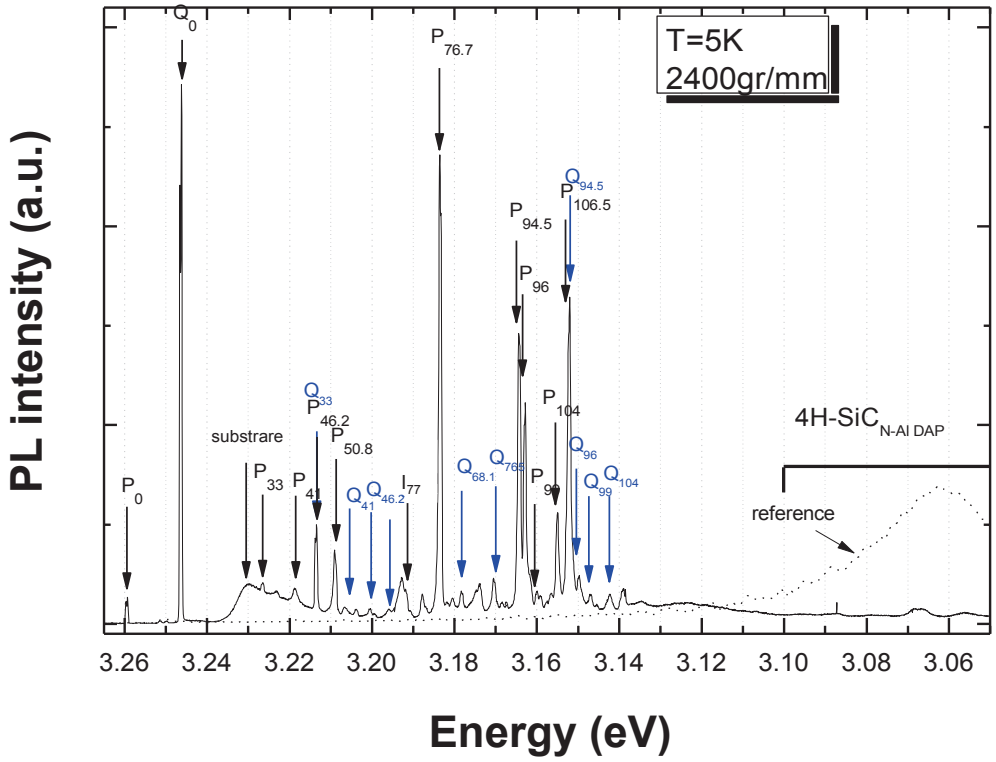


Figure III.13: PL spectrum collected on typical Ge containing sample, grown at 1500 °C using 0.02 sccm of GeH_4 and C/Si ratio of 3.5 with 6 µm/h growth rate in the energy range 3.26 - 3.05 eV with marked characteristic phonon position.

Coming back to the top surface morphology of Ge containing layer, the only detectable difference when using GeH_4 during growth could be seen on the surface when looking closely by SEM. One can see the presence of spherical shape droplets, which size and density depend on growth temperature (Figure III.14). Typically, at 1500 °C, the average diameter is 100 nm (Figure III.14a), while it goes up to ~1.5 µm at 1600°C (Figure III.14b).

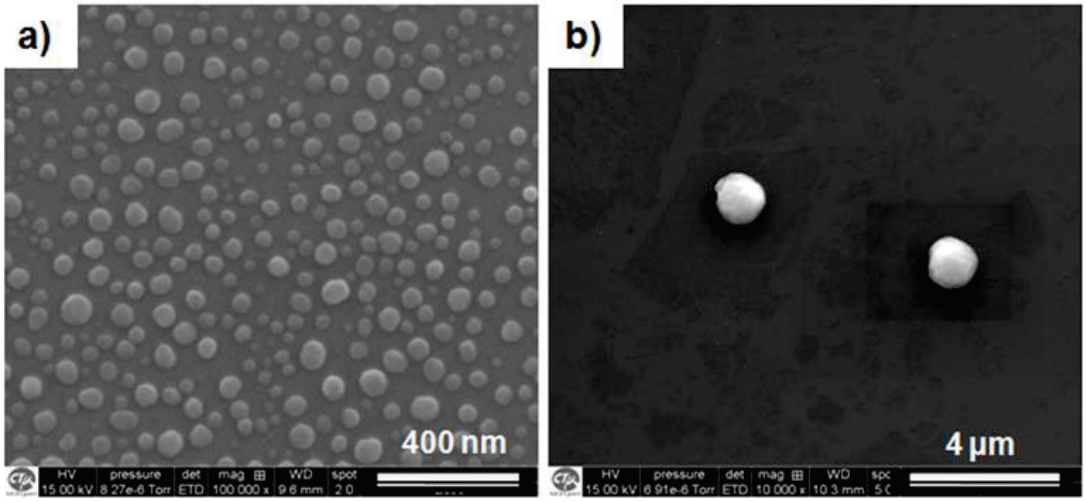


Figure III.14: SEM images of the spherical droplets formed at the surface when introducing GeH_4 gas for growth temperature of a) 1500 °C, b) 1600 °C

Energy-dispersive X-ray spectroscopy (EDX) analysis on the biggest droplets presented strong peaks related to Si and Ge (figure not shown). Si signals may come from the substrate. Consequently, EDX gives us only information on the presence of Ge inside the droplets.

µ-Raman analyses were also performed on a single droplet from sample of Figure III.14b in order to obtain more information on its nature (Figure III.15).

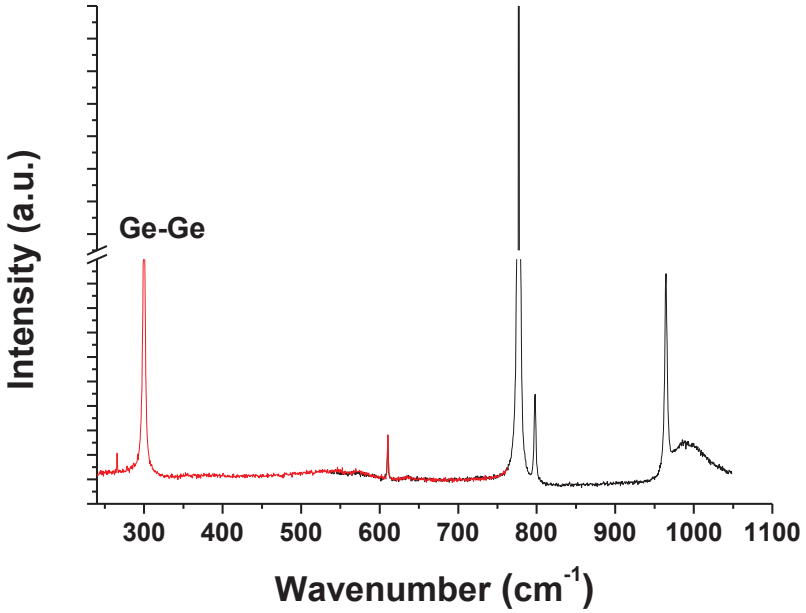


Figure III.15: µ-Raman spectra collected on a droplet shown in Figure III.14b

One can clearly see one additional peak to that of SiC located at ~300 cm^{-1} related to Ge-Ge bond and which confirm the presence of pure germanium [III.15].

Now, High Resolution Transmission electron microscopy (HRTEM) has been also used to investigate the Ge droplets formed on surface (Figure III.16). Scanning transmission electron microscopy (STEM) - High-Angle Annular Dark-Field (HAADF) Imaging and EDX Map and spectrum were carried out on the same sample to trace any possible Ge inclusion in SiC (figures not shown).

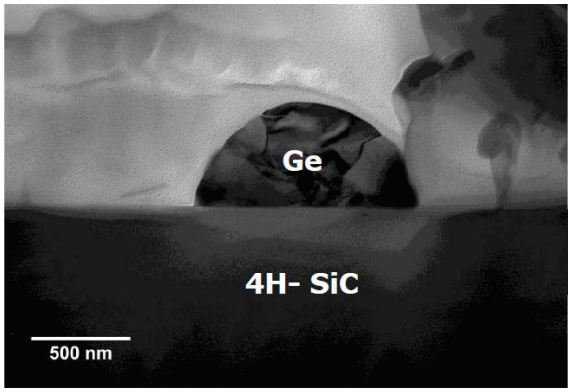


Figure III.16: Ge Polycrystalline droplet on the 4H-SiC surface

Ge was not detected in the Ge doped epilayer and the diffraction patterns confirm that the droplets are pure Ge (figure not shown). They are polycrystalline and an extensive study was performed to check possible epitaxial relationship between them and the substrate underneath [III.16]. Specific samples were grown for this purpose.

Energy filtered transmission electron microscopy (EFTEM) map (Figure III.17) was taken in 200kV Microscope to have better qualitative results on Ge incorporation in SiC. A thin region (~70nm) was chosen for the EFTEM map. This result shows higher Ge concentration at the epi-surface interface. But no significant signal was observed deep in the epilayer. The EFTEM map also confirmed that there was no Ge in the 3C SiC inclusion region (triangular/carrot defect).

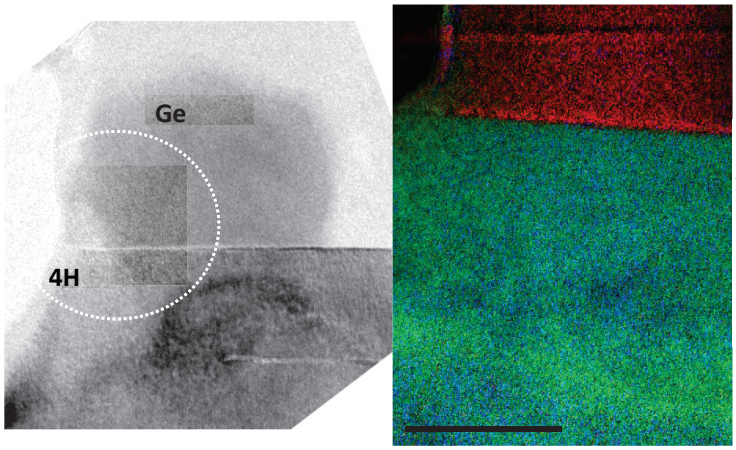


Figure III.17: EFTEM Chemical map was taken at the marked region of the TEM images. Ge (Red) and Si (Green) and C (Blue) energy filtered map show in the right

To now, we have shown that the accumulated droplets on the surface are pure Ge distributed on the surface and having diameters which can be as low as 40 nm. AFM conducted on a sample grown at 1450 °C allowed detecting particles with minimum size reaching 25 nm and the maximum was 100 nm (Figure III.18).

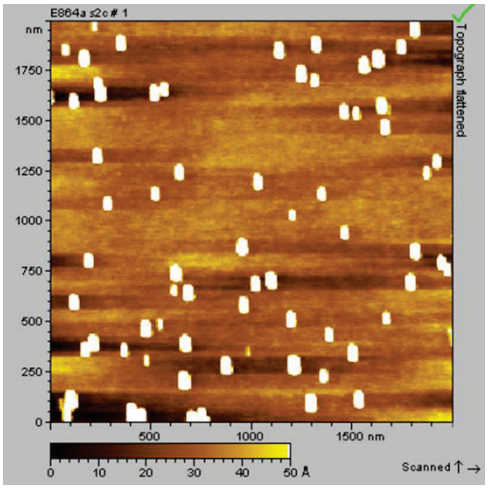


Figure III.18: AFM imaging showing the accumulated droplets on an epitaxial layer grown with Ge at 1450 °C

The droplets were easily removed chemically by HF-HNO_3 and NH_3-$H2O_2$ wet etching. AFM was then used to study the surface microstructure of the epilayers without the droplets.

A very strange and special feature has been recognized on a sample's surface when performing long time experiments (3 hours in this case). As can be seen in Figure III.19, the sample surface shows a unique morphology, characterized by the presence of a high density of depressions of few nanometers deep and few µm wide. Due to the presence of these features, the surface roughness (RMS) is about 6 nm, higher than in the state-of-art of 4H-SiC epitaxial layer that is 0.16 nm [III.17].

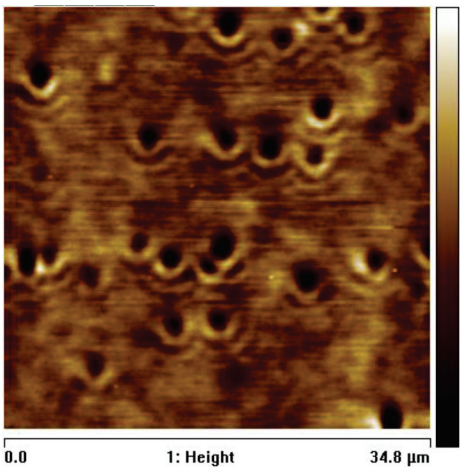


Figure III.19: AFM Morphological characterization of the surface of the Ge-doped 4H-SiC epitaxial layer after acid etching showing the surface "depressions". z-axis ranges from 0-5nm

As preliminary conclusion, long growth runs with Ge addition is affecting negatively the surface morphology. In order to avoid such droplet prints and to be able to observe the real step microstructure by AFM, the growth time is lowered to 1 hour. Before AFM measurement, the samples were etched chemically for removing the excess of Ge on the surface.

At first, on the Ge doped sample, the nano-metric depressions discussed in the previous paragraph are not observed (not shown). In addition, an irregular step and terrace structure is seen (Figure III.20a) whereas the steps are more elongated without GeH_4 addition (Figure III.20b). The average step height is calculated to be 7.9 and 9.5 nm respectively for growth with and without GeH_4. Despite this difference, the RMS roughness is similar in both case and equal to ~0.4 nm for a 2x2 μm^2 scan.

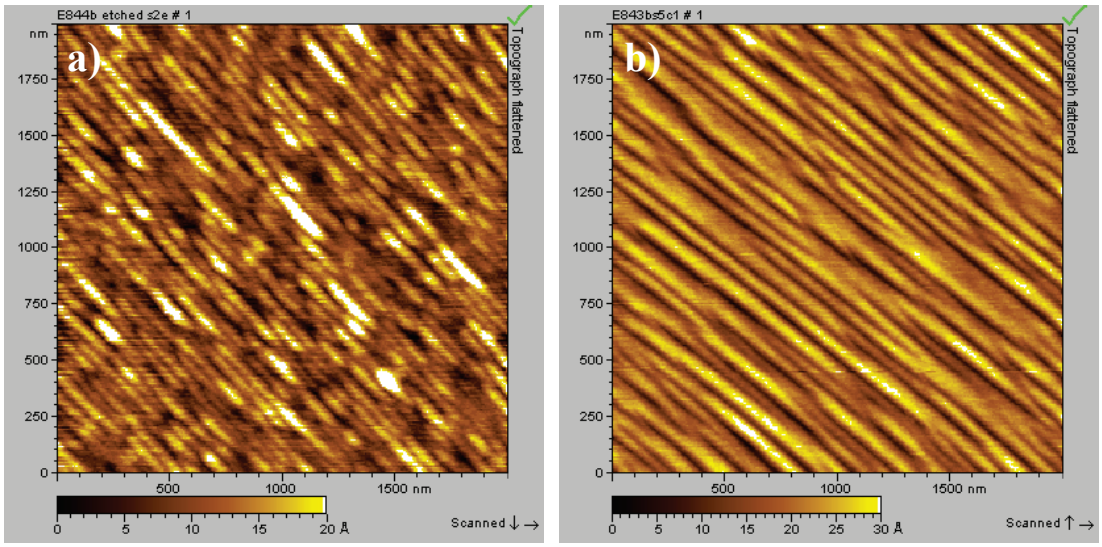


Figure III.20: a) AFM surface morphology after wet etching of sample; zoom (2x2 μm^2) between the droplets showing the irregular step structure. In b) is shown a sample grown in similar conditions as in a) but without GeH_4 addition. Scan size is 2x2 μm^2 in both cases.

Last but important remark to be made from the Ge doping experiments is the effect of GeH_4 addition on reactor cleanliness. Indeed from the very first experiments performed with this precursor, it was obvious that the reactor walls were dirtying more rapidly than usual. This is due to the fact that GeH_4 is much less thermally stable than SiH_4 and C_3H_8 so that its cracking efficiency is probably 100 %, even on the "colder" parts which are the reactor's walls. The deposit is then more important on the walls. This does not seem to have any impact on the layer quality or repeatability. But its major drawback is the increased deposit just above the susceptor which little

by little hinders the optical pyrometer measurements. This parameter defining the reactor "lifetime", using GeH_4 reduces significantly this life time and one needs to change it more often.

III.3.2 Ge quantification by SIMS

SIMS technique was extensively employed during this work to extract Ge incorporation depth profile and layers thicknesses. The layers were always chemically etched before any measurement to eliminate the droplets. These measurements were employed to check the influence of growth parameters on Ge incorporation level. Also, possible memory effect of the reactor that may be caused by the deposit on the side walls is tested.

On the first Ge-doped samples, the Ge depth profile was found to be non-flat. Ge incorporation showed an increasing trend from the substrate to the surface and it was saturating after approximately 20 minutes of deposition (Figure III.21).

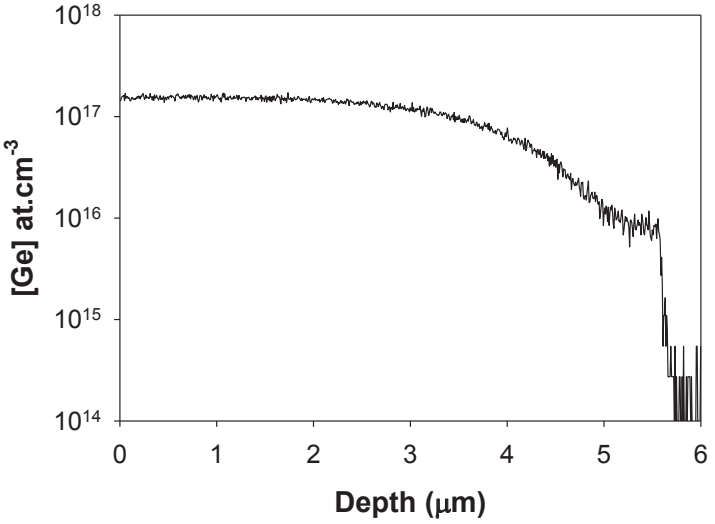


Figure III.21: SIMS depth profile collected on sample grown at 1600 °C for 1 hour using 5,7 um/h growth rate and at C/Si ratio of 3.5

This behavior being very uncommon for impurity incorporation, it was difficult to be directly connected to Ge element. The explanation is strictly technical and it has nothing to do with science. Indeed, the used GeH_4 flux was 0.02 sccm, which is relatively very low, compared to that implemented for other dopants like Al and N_2. After measuring the total volume of Ge line from the mass flow to the reactor, we have calculated that using such low flux (0.02 sccm), about 40 minutes would be in

principle required to fill entire line with the original GeH_4/H_2 composition. Since the precursors fluxes are always stabilized several minutes in the vent before sending to the reactor, this calculation roughly fits with the experimental observation. So, after optimizing all the conditions (i.e. increasing the time of flux stabilization in the vent), the SIMS depth profile on a typical sample grown with GeH_4 addition reveals a homogeneous incorporation level in the entire layer (Figure III.22). The estimated growth rate was 2.5 μm/h which is very similar to the one expected without GeH_4 using similar conditions.

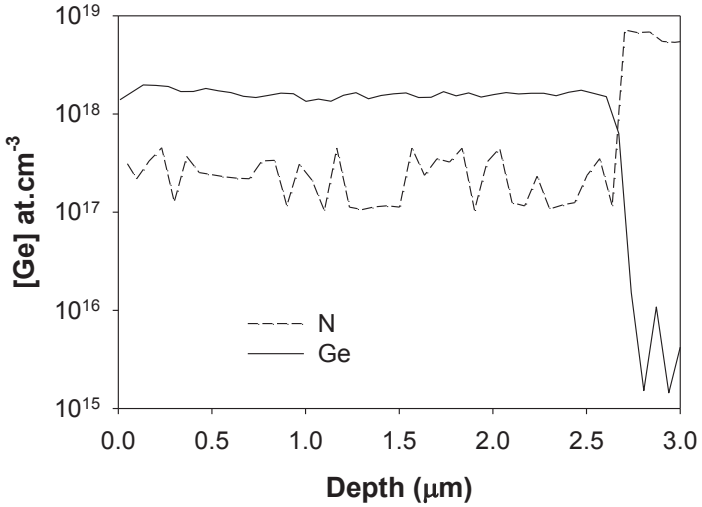


Figure III.22: SIMS depth profile of sample grown at 1500 °C with 0.02 sccm GeH_4 flux for 1h. N concentration profile is shown for localizing the epilayer/substrate interface (note that the N doping level of the layer is below the detection limit of the SIMS apparatus)

Ge concentration as a function of GeH_4 flow rate is shown in Figure III.23.

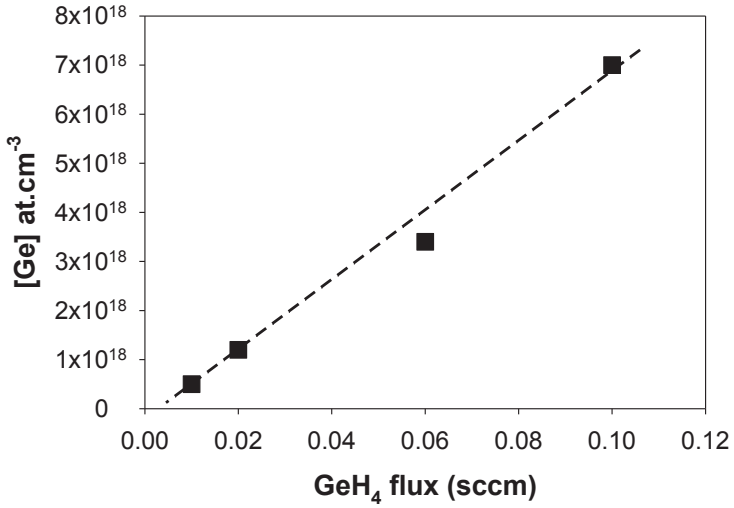


Figure III.23: Ge incorporation levels as function of GeH_4 flow rate. The growth was performed at 1500 ˚C using a C/Si ratio of 5 with a growth rate of 6 μm/h

One can notice that the Ge incorporation increases linearly with the precursor flow within the studied range ($0.01 \leq GeH_4 \leq 0.1$ sccm). The maximum achieved level is $7.0x10^{18}$ cm^{-3}.

Since the growth rate and C/Si ratio are two essential parameters in SiC epitaxial growth, Ge incorporation dependence as a function of these parameters was studied as shown in Figure III.24 and Figure III.25.

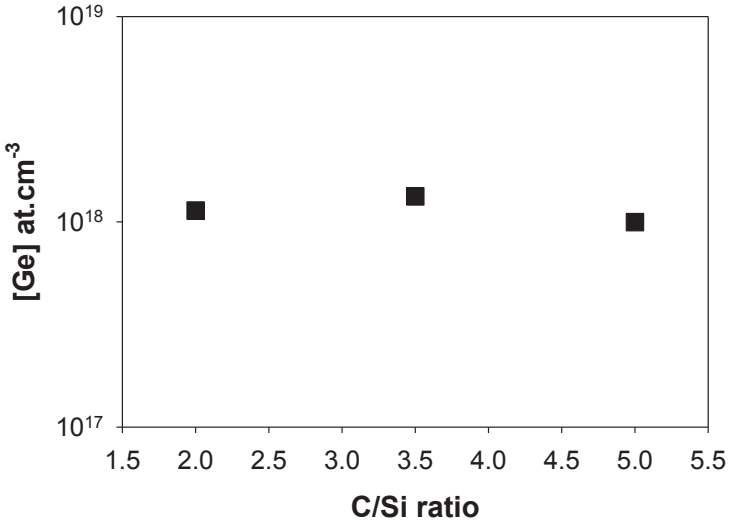


Figure III.24: Ge incorporation level as a function of C/Si ratio. Samples were grown at 1500 ˚C using 0.02 sccm of GeH_4 and fixing the silane flux to 5 sccm (growth rate is 6 µm/h)

In the case of C/Si ratio, no clear trend could be detected within the studied range (2-8). However, a moderate increase as a function of growth rate was observed. The Ge incorporation level remains close to $1x10^{18}$ cm^{-3}.

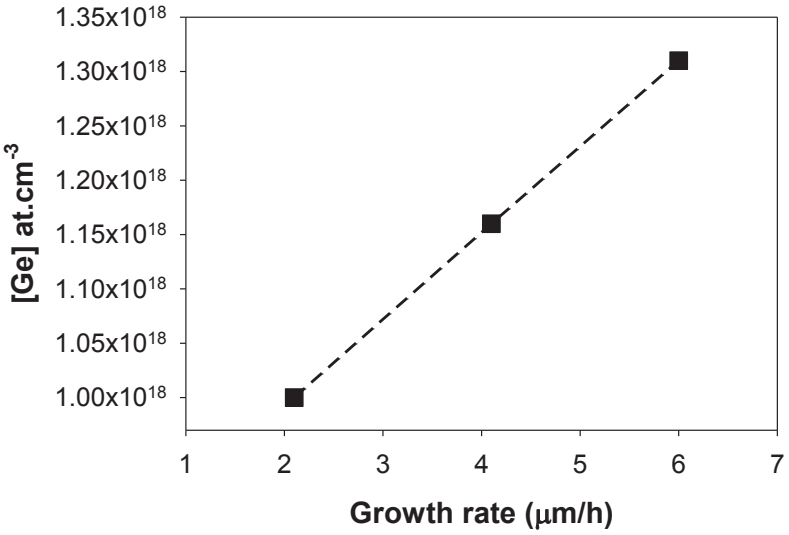


Figure III.25: Ge incorporation level as a function of growth rate. Samples were grown at 1500 ˚C using 0.02 sccm of GeH_4 with a fixed C/Si ratio of 5

On the other hand, temperature has a more pronounced effect than the two previous parameters as can be seen in Figure III.26. [Ge] decreases of one order of magnitude when growth temperature increases from 1450 to 1600 °C.

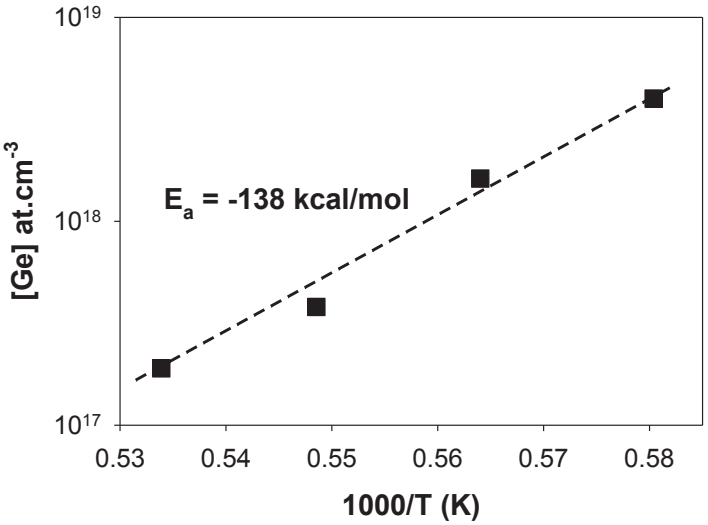


Figure III.26: Ge incorporation as a function of temperature. Samples were grown using fixed GeH_4 flux of 0.02 sccm and C/Si ratio of 3.5

Crystallographic dependence of Ge incorporation was studied using different types of substrates (off-orientation, polarity, polytype). The results are summarized in Table III.2. One can see that Ge incorporation does not seem to be significantly dependent on the crystallographic aspects.

Table III.2: Ge concentration inside samples grown using the same conditions but on various seeds (T= 1500 °C)

Sample	Substrate polytype	Off orientation from (0001)	Polarity	[Ge] at.cm^{-3}
E813a	4H-SiC	8 °	Si face	9.7 x 10^{17}
E813b	4H-SiC	8 °	C face	1.0 x 10^{18}
E813c	4H-SiC	4 °	Si face	9.8 x 10^{17}
E796b	3C-SiC	On-axis (111)	Si face	9.9 x 10^{17}

* The 3C-SiC seed was grown by VLS transport from Sn-Si melt, i.e. without Ge

Finally, when introducing a foreign element in a high purity CVD reactor, an important question is the possible memory effect, i.e. how much unintentional impurity incorporation one can get after a growth using this impurity. This investigation was performed in two ways: 1) a typical "witness" 4H-SiC epilayer was grown after several GeH_4 containing growth runs; 2) GeH_4 was only added during 10 min in the reactor at 1500°C (to form a network of Ge droplets on the seed surface)

before starting a typical CVD growth without GeH_4. The conditions for the typical CVD growths are 1500°C with 3 µm/h and C/Si = 5 for 1 hour. In the first case, SIMS analysis pointed out that the amount of Ge in the witness layer is less than or equal to the apparatus detection limit which is ~$1x10^{15}$ at/cm^3 (figure not shown). In the second case, SIMS analysis showed the presence of Ge in the layer but only located near the epilayer/substrate interface and restricted to several tens of nm only (Figure III.27). In conclusion, there is no significant memory effect due to the use of Ge impurity in our cold wall reactor.

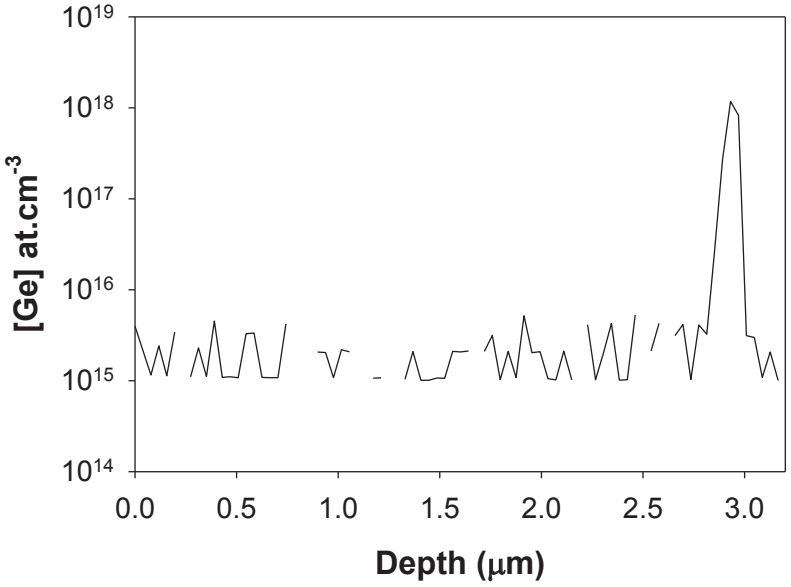


Figure III.27: SIMS profile collected from a sample grown without GeH_4 during the deposition time but with 0.1 sccm GeH_4 addition for 10 minutes prior to the growth at 1500 °C

III.3.3 Discussion

III.3.3.1 Ge impact on layer quality

The density of surface defects was shown not to be affected by GeH_4 addition. The large majority of these defects have similar length. Taking into account the crystal off-orientation, we postulate that they have been formed at the epilayer/substrate interface [III.18]. They are most probably caused by substrate imperfection or improper surface preparation, but not by the presence of Ge atoms. The absence of layer quality degradation was confirmed by LTPL characterization. And, the un-detected shift in the FTO mode of IR-spectrum can be explained by the low Ge content in the epilayers.

Since no other work has been ever performed on Ge element addition during 4H-SiC homoepitaxy by CVD, we shall compare with studies using other impurities. For instance, it was shown that Al incorporation degrades SiC crystalline quality when incorporated above 10^{20} at.cm^{-3} [III.19], while in the case of N the degradation starts a bit earlier in the 10^{19}– 10^{20} at.cm^{-3} range [III.20, III.21]. In the case of "non-dopant" impurities, VCl_4 addition to the CVD system leads to surface defect generation for [V] incorporated levels from $1x10^{17}$ at.cm^{-3} and above [III.22].

In our case, even in the highest Ge containing layer ($7x10^{18}$ at.cm^{-3}), we did not observe any detectable change in surface defect density. Thus, Ge impurity is more like Al or N and does not generate easily crystal defects during growth of 4H-SiC. One can still expect some strain because of Ge presence and its replacement of Si atom [III.14]. However, high resolution XRD is needed to confirm this hypothesis. On the other hand, Ge accumulates easily on the surface by forming pure Ge droplets, which tend to get bigger when increasing either deposition temperature and/or time. In fact, the main negative impact detected so far for GeH_4 addition is on the modification of the surface morphology, either for the step and terrace structure as seen in Figure III.20 or the droplet fingerprints in Figure III.19. However, the "depression" fingerprints are rarely detected and restricted to long growth runs.

III.3.3.2 Ge incorporation mechanism

It was shown in a previous study that, when growing 3C-SiC layers using VLS mechanism from a Si-Ge melt, Ge is incorporating in the layer through nanoscale interstitial clusters, which are detectable, by μ-Raman spectrometry [III.7, III.23]. This is not the case in the present study since no Ge-related signal was detected by μ-Raman analyses, even for the case of 3C-SiC polytype (sample E796b of Table III.2). In addition, cross sectional TEM analysis performed on one of the epitaxial layers grown with Ge confirms the absence of either Ge inclusions and or Si-Ge-(C) nanoclusters inside the layer [III.24]. Nevertheless Ge may incorporate as isolated interstitial (this will not be detected by Raman spectroscopy or TEM). That is why ALCHEMI (atomic location by channelling enhanced microanalysis) was used for determining the site occupancy of Ge inside 4H-SiC matrix. More description of this technique can be found in reference [III.25]. In short, the samples are irradiated by accelerated electrons under channeling conditions. EDX spectra are then recorded

while varying the angle of incidence of the electron close to these channeling angles. From the angle dependence of EDX spectra, one can estimate the atomic position of impurities inside a matrix if there is enough impurity to be detected by EDX. For this task two samples were grown, a 4H-SiC homoepitaxial layer on 8° off axis substrate and a highly twinned 3C-SiC layer grown on nominally on axis 4H-SiC. Before discussing our results, it is worth mentioning here that, according to its covalent radius of 0.122 nm, Ge should rather incorporate on Si site (covalent radius of 0.111 nm) than on C site (covalent radius of 0.077 nm). This was experimentally confirmed in the case of MBE growth of Si-rich cubic SiGeC alloys [III.26]. By comparing the ALCHEMI simulation and experimental results, one comes to the conclusion that Ge atoms are located on Si site, and not on C or interstitial sites (Figure III.28).

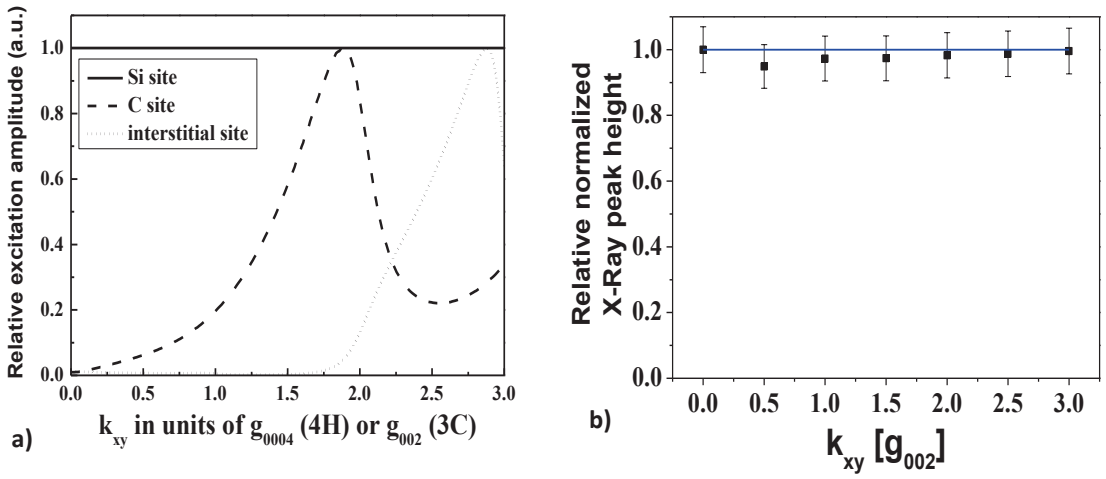


Figure III.28: a) ALCHEMI simulation showing Bloch state excitation (normalized to Si-signal) for different atomic sites in SiC material and b) Ge signal evolution on a Ge doped sample grown in this study. Both results are given as a function the reciprocal lattice vector in units of ghkl.

This finding supports the theoretical prediction obtained using an anharmonic Keating model showing that substitutional Ge is preferable incorporated in silicon side [III.27]. As a result, for the rest of the discussion, we will assume that Ge incorporates on Si site during our growth experiments. The presence of Ge droplets on the samples after growth is clear evidence that Ge is not massively incorporating inside the lattice, and the excess of Ge brought by the gas phase accumulates on the surface. While this accumulation is time dependent (droplets get bigger with time), when using the GeH_4 flux stabilization procedure none of the SIMS profiles displays any depth evolution of the Ge incorporation level (Figure III.22). This is surprising

since these droplets could act as an in-situ extra source of Ge so that one could reasonably expect an increase of Ge incorporation with time. This is not the case and it suggests that, within the studied conditions, Ge is mainly incorporating from the initial GeH_4 vapor phase. This is also confirmed by the increase of Ge incorporation with GeH_4 flux (Figure III.23). Taking the assumption that Ge droplet formation does not affect significantly Ge incorporation, we can now try to compare Ge incorporation behavior to the ones of some better known impurities (dopants) like Al, N or B (which are not known to accumulate on the surface), with more parallel focus on Al element which is supposed to incorporate on Si site like Ge.

Concerning Ge concentration increase with GeH_4 flux, this is of course a classical trend for the dopants [III.8, III.9]. The general trend with temperature (Ge incorporation decrease with temperature increase) is also found for the dopants [III.10, III.19]. This is explained by an increase of adatoms desorption from the growing surface at higher temperature. From the slope of Figure III.26, one can calculate the activation energy of Ge desorption using Arrhenius law. It is found to be ~ -137 kcal/mol. In the case of Al impurities, the activation energy of desorption which can be found in the literature are of the same order of magnitude though it is systematically higher, ranging from -160 kcal/mol (calculated from the results in ref [III.19]) to -204 kcal/mol [III.28]. This is to be correlated with the higher vapor pressure of this element compared to Ge. Another similarity with Al impurity is the effect of growth rate. Indeed, Ge incorporation was found to increase with growth rate, like Al does [III.29]. This can be attributed to the reduced residence time on the surface (and thus reduced desorption) of the adatoms at higher growth rates.

Except the previous cited parameters (temperature, Ge flux and growth rate), the other parameters investigated in this study (C/Si ratio and seed crystallography) do not show any significant influence on Ge incorporation level. This is rather uncommon since, for the cases of Al, B or N impurities, these parameters have visible and known influence. For instance, Al atoms, which incorporate on Si site as should Ge, incorporate less at low C/Si ratio (due to site competition effect [III.19]). These differences are difficult to explain though one can suggest that it may be linked to our particular Ge incorporation conditions from a Ge-saturated vapor phase and surface. Indeed, in other works, the formation of dopant aggregates or droplets on the growing SiC surface was never reported, even for high concentration of impurity precursors

[III.19, III.30]. Note that in both cases of B and Al, higher incorporation levels than in the present study can be reached without any surface accumulation.

Concerning the crystallographic aspect, Ge incorporation is found independent on off-orientation, polarity and polytype. In terms of off-orientation, this trend is more or less similar to the ones reported for Al and N incorporation [III.31] while the polarity has a much higher impact. In the present case of Ge impurity, these trends may be attenuated due to the Ge-saturated vapor phase and surface conditions, as previously mentioned.

III.4 Influence of Ge addition on layer properties

In the first part of this chapter we have discussed the epitaxial growth of Ge containing SiC layers from the surface and structural point of view. Ge was found to be incorporating without inducing surface and/ or optical degradation to the layer quality and purity. But, one could expect some changes in the layer properties due to the replacement of Si atoms by Ge ones inside the SiC lattice. Sometimes positive surprises are encountered when searching in different direction. In this section, the results from electrical characterization of various Ge doped layers are detailed and discussed.

III.4.1 Interaction between N and Ge

Since nitrogen doping is a very common step in SiC technology and since our Ge doped layers were almost systematically also N doped, the possible effect of GeH_4 addition on N incorporation was studied.

III.4.1.1 Experimental details

Three sets of samples were grown at different C/Si ratio and varied Ge flux but fixed time and growth rate, see Table III.3. Set A is the witness set to set B (Ge doped). Both were grown at different C/Si ratio and constant GeH_4 flux for set B. While, the third set was grown using constant C/Si ratio and varied GeH_4 flux.

All samples were grown on 8° off axis Si face seeds. N doping was performed using 0.25 sccm of N_2 at growth temperature of 1500 °C. The mercury microprobe was used to evaluate the doping type and level inside the layers.

Table III.3: Growth parameters of the sets grown to study the influence of GeH_4 adding on n-type doping

	Sample name	C/Si ratio	T (°C)	Time (min)	Gr (µm/h)	GeH_4 (sccm)
Set A	E1	2	1500	60	2.5	0.00
	E2	3.5				
	E3	5				
	E4	8				
Set B	E5	2	1500	60	2.5	0.02
	E6	3.5				
	E7	5				
	E8	8				
Set C	E3	5	1500	60	2.5	0.00
	E7					0.02
	E9					0.06
	E10					0.10

III.4.1.2 Results and discussion

The results obtained as function of C/Si ratio and constant GeH_4 flux is depicted in Figure III.29. All the C-V measurements were performed at the center of the sample. The error bars represent the fluctuation in doping concentration within every single C-V profile. One can see that the net n type doping follows the N site competition rule on Si face (N incorporates on C site so that [N] decreases for increasing C/Si ratio) with or without the presence of Ge atoms. But less expected is the fact that the presence of GeH_4 increases n doping level by a factor from 2 to 5 depending on the C/Si ratio.

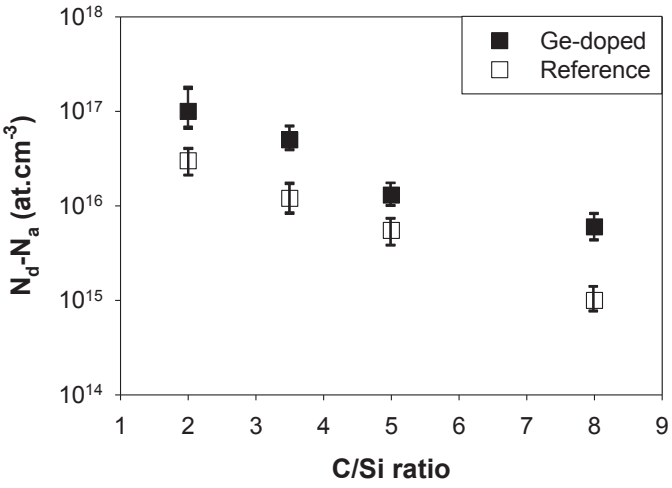


Figure III.29: N type doping level as a function of C/Si ratio for layers grown with or without GeH_4

To discuss this point, we will assume that the compensation level is low (as seen from LTPL) and that the N atoms incorporated are 100 % activated, so that

[N] = n type doping level. It is shown in Figure III.29 that the presence of GeH_4 during N_2 in situ doping increases N incorporation. Since Ge incorporation is supposed to occur on Si site and N one on C site, one may not expect any direct interaction between Ge and N impurities. Furthermore, gas phase interactions are very unlikely when considering the high dilution of GeH_4 and N_2 precursors. So, interaction at the surface is more probable. One may propose that the presence of Ge atoms on the surface decreases N desorption rate. And if this mechanism is true, it shall be effective at the step edges where the atoms are incorporated.

On the other hand, increasing GeH_4 flux does not seem to significantly affect n doping level Figure III.30. We have seen previously that Ge increases with GeH_4 flux which means here that [Ge] increase does not affect the n type doping level. This is probably due to the fact that [Ge] is about two order of magnitudes higher than [N] in these samples so that the observed Ge effect could be already saturating. If this assumption is right, the best chance to detect any dependence of n-type doping on [Ge] is to study the low [Ge] regime, i.e. in the $\approx 10^{16}$ at.cm^{-3} range.

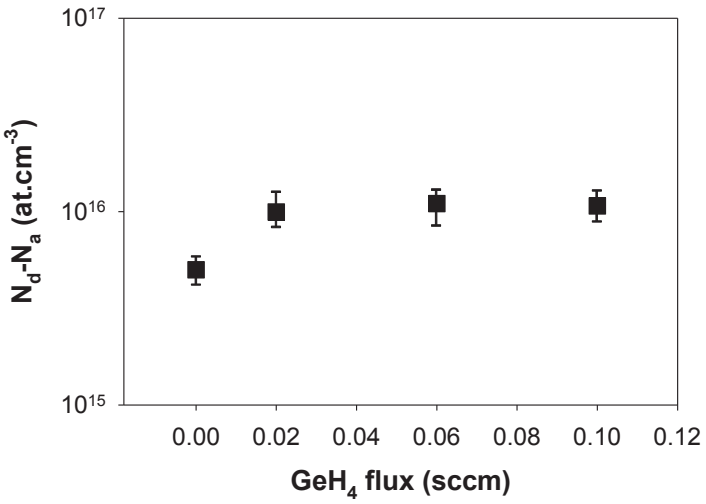


Figure III.30: N type doping level as a function of injected GeH_4 flux. Samples were grown at 1500 ˚C using fixed growth rate and C/Si ratio of 5

In fact, we have grown non-intentionally such a sample at the beginning of this study (see Figure III.21). For non-stabilized GeH_4 flux, [Ge] was shown to be $<10^{17}$ at.cm^{-3} close to the epilayer/substrate interface. Using a similar sample, SCM measurement in cross sectional observation was conducted. The result is displayed in Figure III.31 and compared with SIMS depth profile. One can see the direct correlation between [Ge] and SCM signal (directly related to n-type doping level).

Such result confirms our hypothesis concerning a link between Ge and effective n-type doping. The reason for such effect is difficult to find.

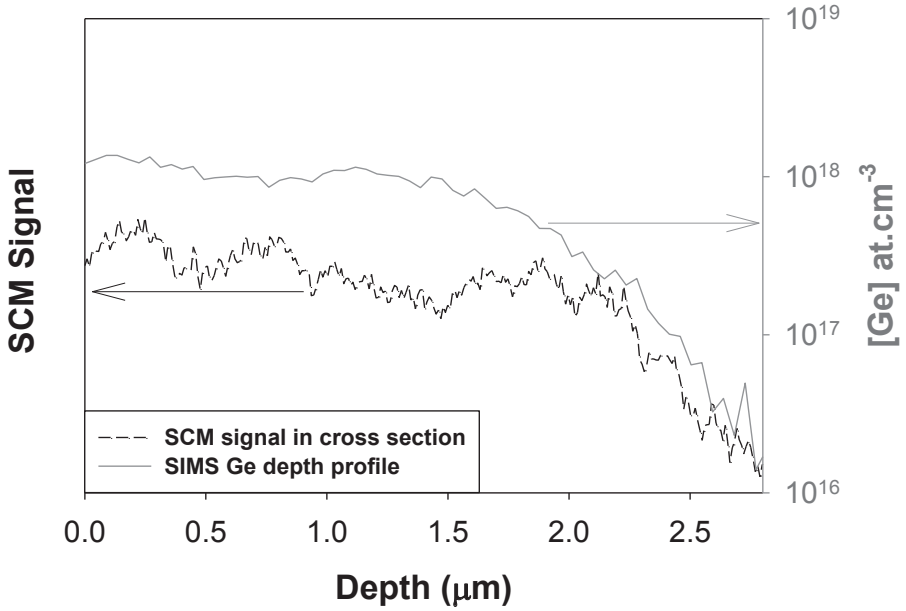


Figure III.31: Scanning capacitance microscope measurement (image to the left) and its relevant SIMS depth profile (image to the right). Both figures have to be merged.

The doping Level derived from CV-curves analysis collected from E3 and E7 samples shown in Table III.3 are depicted in Figure III.32. An average behavior was determined considering the best diodes. This result is consistent with the previous investigation done by mercury microprobe. Where a higher n-type doping level is found for Ge doped sample.

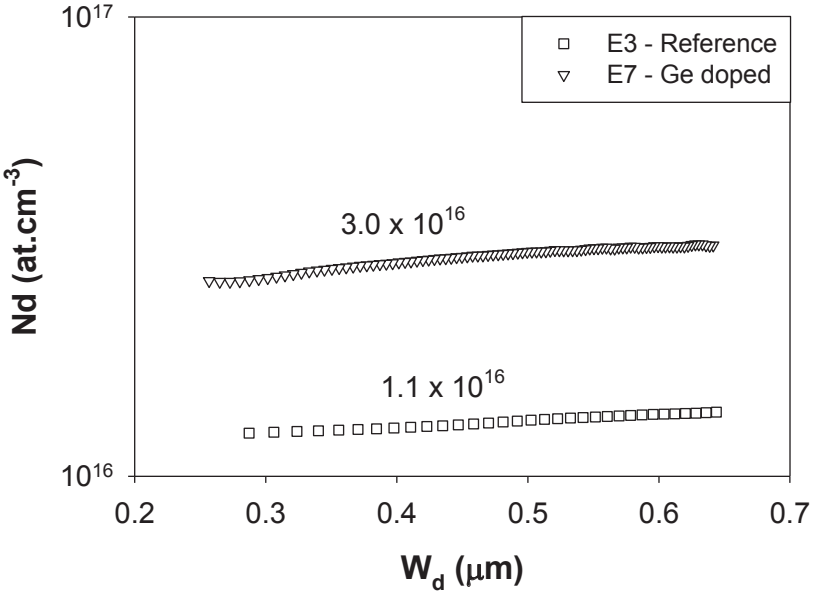


Figure III.32: N_d obtained from the CV analysis of several diodes fabricated on E3 and E7 samples

III.4.2 Schottky contact

As mentioned in Chapter I, the number of works related to electrical characterization of Ge doped 4H-SiC is very limited. It was mostly for Ohmic contact improvement [III.32]. But for Schottky contact, we could not find any study. This is thus the purpose of this section.

We will first perform a morphological and electrical nanoscale characterization of the surface, that is, the region where the Schottky junction will be formed. Secondly, the evaluation of the electrical properties of the Schottky contacts fabricated on this Ge-doped epitaxial material will be carried out, in order to determine any effects of the Ge doping on the metal/semiconductor interfaces behavior.

III.4.2.1 Sample preparation

The principle sample "E11"used in these measurements consists in a Ge-doped 4H-SiC epilayers, 6 µm thick, grown at 1500 °C for 3 hours using 0.02 sccm GeH_4 and 1.67 sccm SiH_4 with C/Si ratio of 3.5. The substrate was as usual a commercial n+ doped 8° off axis 4H-SiC material. The layer was n-type doping in the few 10^{15} cm^{-3} and [Ge] = 1 x 10^{18} cm^{-3}, as measured by C-V mercury microprobe and SIMS respectively.

The epilayer surface morphology was rather standard but covered by µm scale Ge droplets which were acid etched before further study. In addition, the morphological observation by AFM, showed that the layer is characterized by nano metric dips which causes the increase in the surface roughness (Figure III.19). The nanoscale electrical behavior of the epilayer surface was also visualized using the conductive AFM (C-AFM) technique**.**

Then, Schottky diodes were fabricated using the following procedure. First a back-side Ohmic contact was formed by nickel deposition and a rapid thermal annealing (RTA) process at 950°C in N_2 Ambient (100 nm thick). On the sample front, Ni circular diodes of different radii (varying from 50 to 250 µm) were defined by optical photolithography (Figure III.33). Electrical characterization of the devices was carried out by current-voltage (I-V) and capacitance-voltage (C-V) measurements. I-V characteristics were acquired also as a function of the temperature in order to get information on the temperature dependence of ideality factor (n) and Schottky barrier

height (φB). The electrical properties of the Schottky contacts were studied both before and after an additional RTA treatment at 700°C under Ar for 30 min.

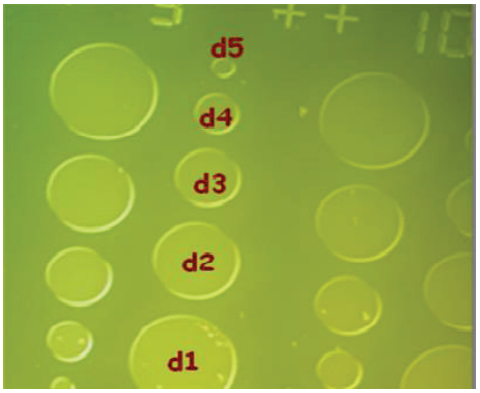


Figure III.33: Diodes of different sizes (radius from 50 to 250 µm), fabricated at CNR-IMM on "E11" sample

The results shown in the following section were obtained during two weeks stay at the facilities of CNR-IMM Catania, Italy. The work was supervised by Dr. Roccaforte.

III.4.2.2 Results and discussion

Before the fabrication of the devices, and after acid etching of the Ge droplets, the surface was studied by means of AFM and C-AFM analysis. Figure III.34a and Figure III.34b show the surface morphology and the corresponding two dimensional current map, respectively. The morphological behavior is previously discussed in the beginning of this chapter (Figure III.19) but we are showing it again here for explaining the nano-scale electrical behavior of the surface.

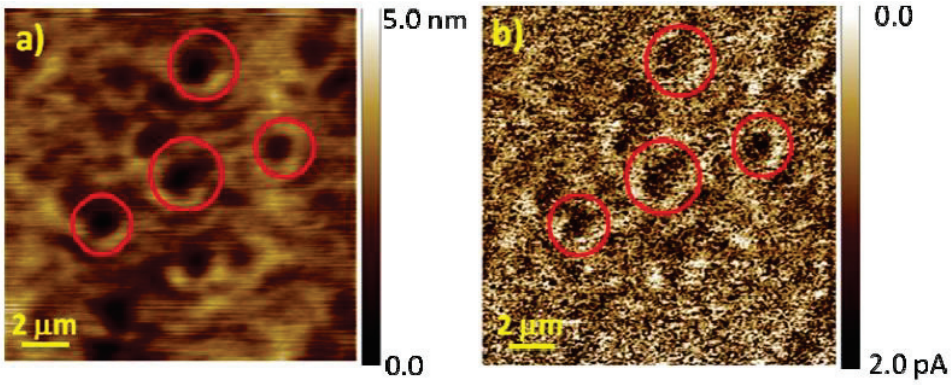


Figure III.34: AFM scans of the Ge-doped 4H-SiC epitaxial layer after acid etching: part a) shows the surface morphology, while the associated two dimensional current map (C-AFM) is reported in part b). The red circles indicate the presence of depressions, where an enhanced conduction is observed

The sample surface shows the presence of μm size "depressions" few nanometers deep (Figure III.34a). Interestingly, the C-AFM analysis carried out in the same area (Figure III.34b) shows a non-uniform current distribution, which is strictly correlated with the surface morphology. In particular, it can be seen that an enhanced current conduction is locally measured in these depressions (marked with red circles in the Figure III.34)

After Schottky metal deposition, the forward I-V characteristics of the devices mostly exhibited a poor ideal behavior, manifesting itself with a high ideality factor (n~1.6) and, in the worse cases of the largest diodes, with the presence of a double-Schottky barrier characteristic, typical of a non-ideal trend [III.33].The leakage current density measured in the devices was quite low, in the order of some tens of nA/cm^2 at a reverse bias of -100V. C-V measurements gave a doping concentration in the order of N_D=5x10^{15} cm^{-3}, which was consistent with the one measured using C-V mercury microprobe. Basing only on forward I-V characteristics, the observed inhomogeneous behavior could not be unambiguously attributed to the material surface quality or to the metal/SiC interface preparation.

An optimized RTA process at 700°C has been performed in order to induce a thermal reaction between Ni and SiC, consuming a thin SiC layer at the surface [III.34]. Under these conditions, the results should be almost independent of any nanoscale morphological or electrical feature of the epilayer surface (as those observed in Figure III.34). As a matter of fact, after RTA an overall improvement of the Schottky characteristics was observed, with the ideality factor decreasing down to 1.1 and the barrier height increasing up to about 1.57 eV. At the same time, no significant changes of the leakage current at 100V were observed. The electrical results of the C-V and I-V curves, averaged on a set of 20 diodes with radius of 50 and 100 μm, both before and after RTA, are summarized in Table III.4.

Table III.4: Electrical parameters of Ge-doped 4H-SiC Schottky diodes both before and after RTA. The Schottky Barrier Height is extracted from the I-V curves

	n	**$q\varphi_B$ (eV)**	**I_{REV} at 100 V**
Before RTA	1.60 ± 0.20	1.41 ± 0.13	2 x 10^{-10} A
Post RTA	1.10 ± 0.05	1.57 ± 0.09	2 x 10^{-10} A

n: ideality factor

In order to get further insights on the homogeneity of the Schottky barrier, the temperature behavior of the forward I-V characteristics has been monitored between 300 and 425K. The corresponding I-V curves, both diodes before (as deposited) and after RTA are shown in Figure III.35.

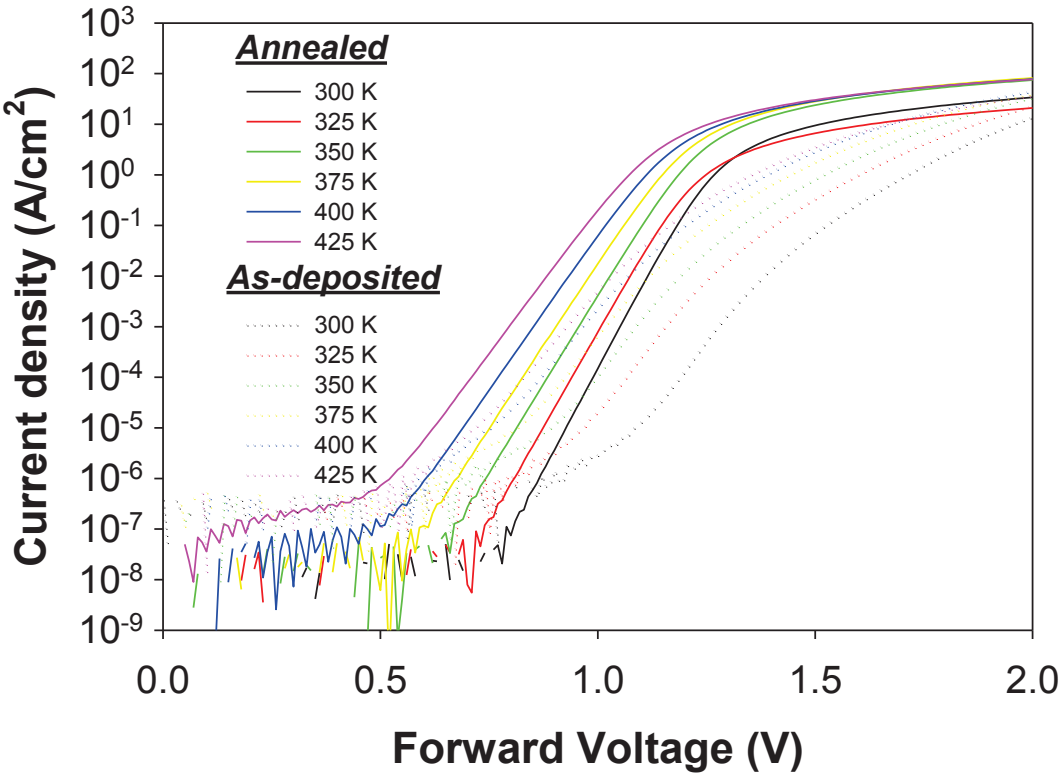


Figure III.35: Forward I-V curves of Ni/Ge-doped 4H-SiC Schottky contacts as a function of temperature both for the as-deposited and for the annealed diode

As can be seen, in both cases the forward current in the linear region increases with increasing annealing temperature. From a fit of the experimental data in the linear region, it was possible to determine the ideality factor n and the Schottky barrier height φ_B, as a function of temperature. These parameters are reported in Figure III.36, for the sample before and after the RTA treatment.

In both cases the Schottky barrier increases and the ideality factor decreases as the temperature increases from 300 to 425 K. Notably, with respect to the as-deposited, for the annealed diode smaller variations of n and φ_B are observed as function of the temperature in this range, with an increase of the barrier height up to 1.60 eV and a reduction of the ideality factor down to 1.05. The temperature dependence of these parameters is an indication of the inhomogeneity of the Schottky barrier [III.34].

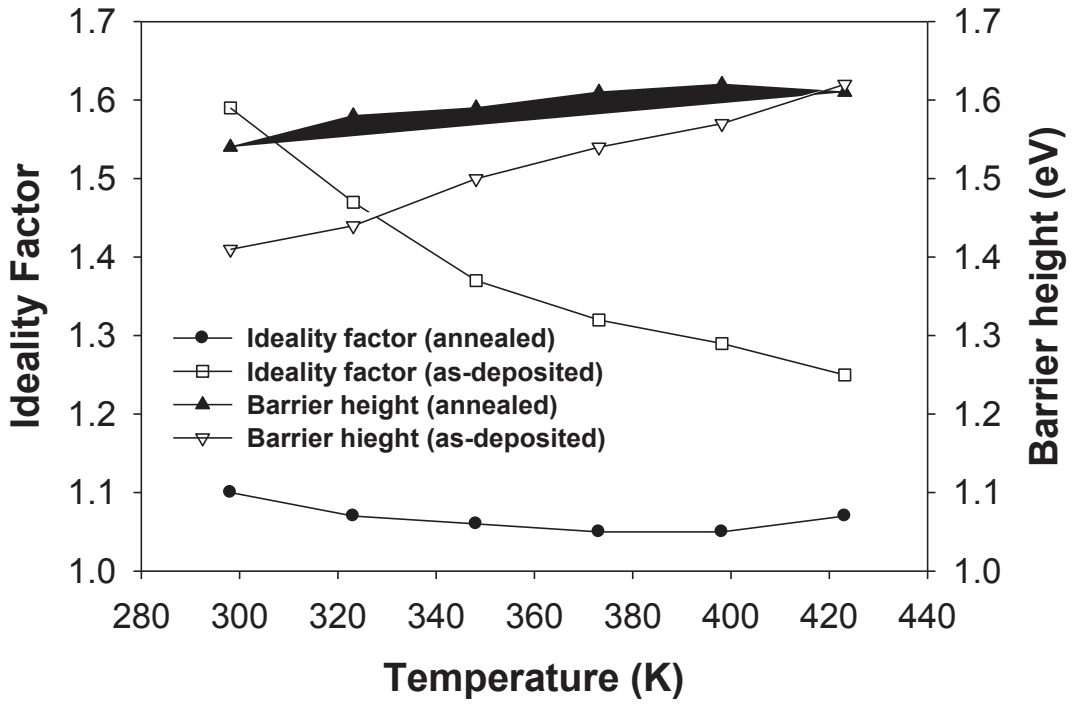


Figure III.36: Ideality factor n and Schottky barrier height φ_B as function of the temperature for the Ni/Ge-doped 4H-SiC diodes, both before and after RTA

In particular, in order to get additional information on the degree of barrier inhomogeneity in the two cases, and to establish a comparison with a standard (non containing Ge) 4H-SiC epitaxy, it is useful to report the plot nkT as a function of kT, where k is the Boltzmann constant and T is the absolute temperature. This plot of the experimental data is shown in Figure III.37, in which the straight line represents the ideal behavior of a Schottky barrier (n=1). In addition, the experimental data taken from Reference [III.35] are reported in the same graph as a reference. The as-deposited diodes, a significant deviation from the ideal behavior is observed: As discussed in Ref. [III.36 – III.38], this is probably linked to a high degree of inhomogeneity of the Schottky barrier, originated from a non-uniform local structure of the metal/semiconductor interface in the real contacts. On the other hand, after RTA, the experimental trend of Ge-doped 4H-SiC diodes approaches the ideal behavior, showing a similar behavior like Ni/4H-SiC Schottky diodes processed under the same conditions on commercial material [III.35]. Using the Tung's model [III.36 – III.38], we can calculate the T_0 anomaly, that gives a measure of the deviation from the ideal case by the relation $n=1+T_0/T$. A good agreement between

the experimental data and the theoretical model is obtained with a T_0 value of 40K, slightly higher than the value reported in Ref. [III.35] for the commercial material.

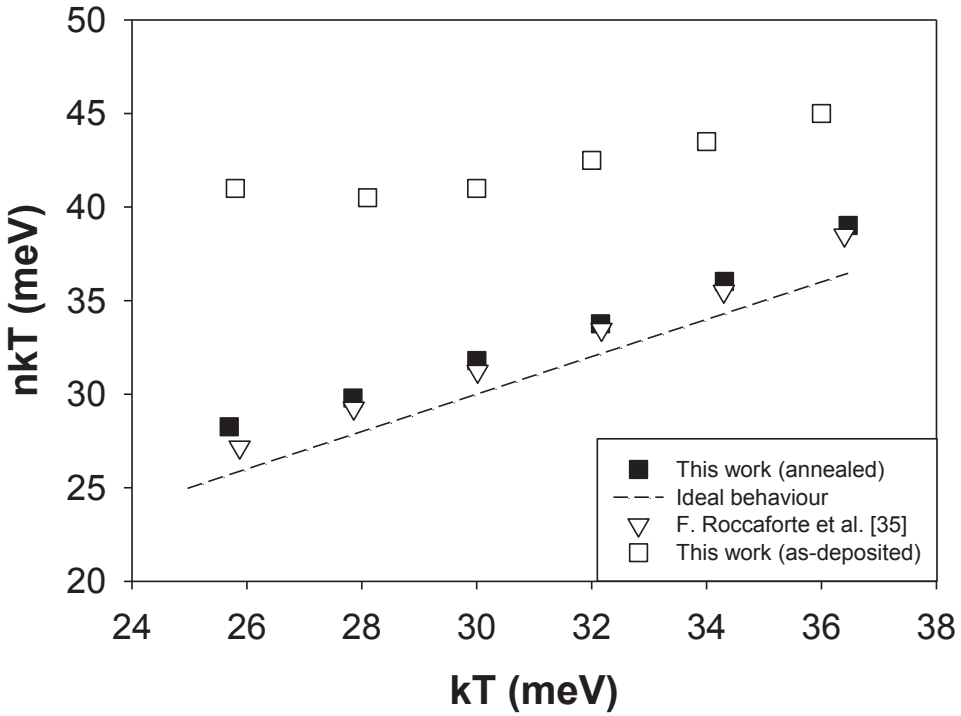


Figure III.37: Correlation plot nkT vs kT for the as deposited and annealed Ni/Ge-doped 4H-SiC Schottky contacts. For comparison, the literature data acquired on commercial material are also reported (taken from Reference [III.35]). The ideal behavior is reported as a straight line.

To conclude, in the as-deposited diodes, a significant deviation from the ideal behavior is observed. On the other hand, after RTA, the experimental trend of Ge-doped 4H-SiC diodes approaches the ideal behavior, showing a similar behavior like Ni/4H-SiC Schottky diodes processed under the same conditions on commercial material [III.35].

III.4.3 Hall, admittance and DLTS measurements

Although Ge does not contribute to the doping of SiC, it was shown previously that its incorporation leads to some increase in the doping level. Also from literature, Ge improves the conductivity and the resistivity of Ohmic contacts after Ge ion implantation and subsequent annealing [III.36]. Thus hall measurement is very essential to complete this study, since it can give both the carrier concentration and conductivity of the epilayers. Moreover, by introducing big element like Ge in the lattice of SiC, a possible effect on point or extended defects can be anticipated.

III.4.3.1 Experimental details

Two samples "E12" and "E13" were grown using identical growth conditions except the addition of 0.02 sccm of GeH_4 in the case of Ge doped one (E13). Growths were performed at 1550 °C using C/Si ration of 5 and growth rate of around 2.5 µm/h for 60 minutes. The layers were intentionally doped by N using N_2 flux of 0.25 sccm. They were deposited on top of a 3.3 µm thick Al-doped p-type epitaxial layer (grown by R. Arvinte in NovaSiC) allowing for Hall characterization of the Ge-doped top layer, only. The sample preparation consists of RCA cleaning followed by the definition of the mesa structure using reactive ion etching. This allows suppressing edge currents and to gives electrical access to the p-layer for verification of the blocking behavior of the p-n junction. Again RCA cleaning is performed before depositing 250 nm Ohmic nickel contacts in van der Pauw configuration. Finally, the contacts are annealed at 1000°C for 5 min.

Hall Effect measurements were carried out at temperatures between 30 K and 700 K and at a magnetic field of 0.66 T. Note that SIMS on sample E13 confirmed that the Ge is not homogenously incorporated inside the layer because of the technical problem mentioned before.

Admittance spectroscopy and deep level transient spectroscopy (DLTS) were employed to study point defects in the samples "E3" and "E7" using circular Ni Schottky contacts (d = 0.4 mm) and a large area ohmic Ni backside contact.

Admittance measurements were performed between 20 and 300 K. However, DLTS measurements were carried out in temperature range 100-600 K (tempscan). Deep levels were monitored by a Pchys Tech© computer controlled and fully automated DLTS system.

All the following electrical measurements were done during my secondment in Dr. Kreiger's group at the University of Erlangen in Germany. The secondment lasted for 2 weeks.

III.4.3.2 Results and discussion

Figure III.38 show admittance spectra taken on samples "E3" and "E7" from 20 K to room temperature (300 K). From these spectra, two capacitance steps and two

corresponding conductance peaks are observed in the C-T and G/w-T curves, respectively. Ionization energies of 52 meV and 99 meV are determined from the Arrhenius plot of the conductance peak maxima observed at various measurement frequencies from 10 kHz to 1 MHz. These energies correspond to the nitrogen donor on hexagonal and cubic lattice site in 4H-SiC and will be used later on for the Hall Effect evaluation. Thus, only point defects related to the hexagonal and cubic nitrogen donors have been detected by admittance spectroscopy.

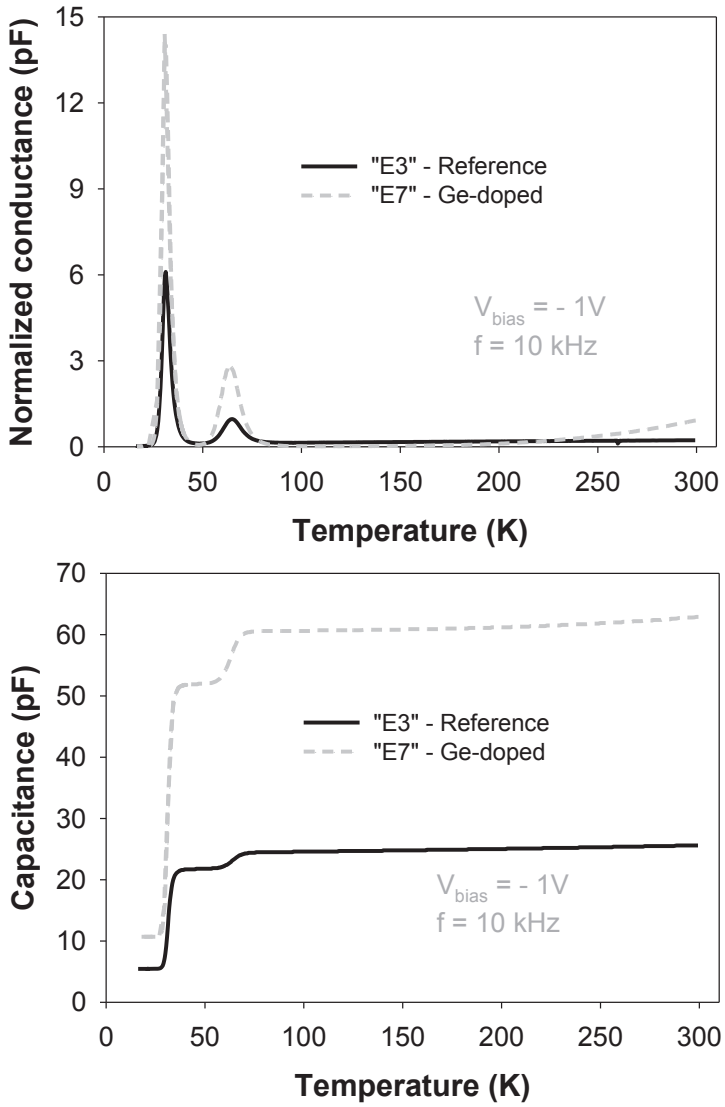


Figure III.38: G/w-T (top image) and C-T (down image) measured by admittance spectroscopy taken on Schottky contacts on samples "E3" (without Ge) and "E7" (with Ge)

The DLTS analyses conducted on the same samples (Figure III.39) gave a weak signal related to Ti impurity at 90 K in the reference sample "E3" only. However, the DLTS spectrum taken on the Ge-doped sample "E7" reveals negative DLTS signals

between 70 K - 140 K and 210 K - 230 K. They can be attributed to extended defects [III.37]. These defects could be generated due to local strain in the lattice generated by the large Ge atoms.

Moreover, one can notice that no signature of the $Z_{1/2}$ and $EH_{6/7}$ point defects (giving peaks at ≈ 300 K and 640 K respectively) is found in both layers. This is most likely due to the high C/Si ratio used during growth [III.38]. This point is very interesting since these defects (attributed to C vacancies) are very common in state of the art of 4H-SiC epilayers grown by hot wall CVD. We believe that the absence of these point defects in our layers is due to the rather C rich growth conditions (C/Si > 2) inherent to the use of cold wall reactors. As a matter of fact, cold wall reactors have some advantages compared to hot wall ones.

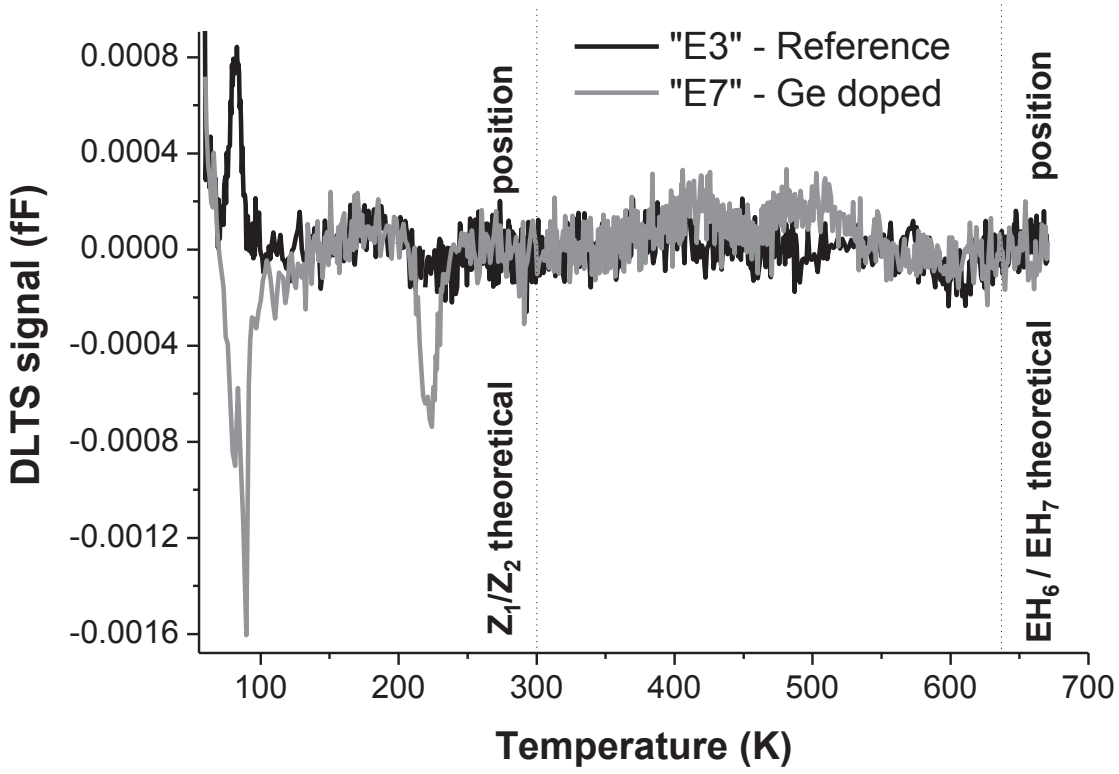


Figure III.39: DLTS spectra collected from "E3" and "E7" between 70 and 670 K. The measurement parameters are T_w = 512 us, T_p = 10 us, V_r = -5.0 V and V_p = -0.5 V

From the Hall Effect measurements that has been collected from the two samples, "E12" (reference) and "E13" (Ge-doped), we were able to extract the carrier concentration along with the amount of compensation, the mobility and the resistivity. Being very crucial parameter for the calculations, the thickness of both layers was determined by SIMS. It gave 2.2 and 2.7 µm thickness for "E12" and "E13" respectively.

Figure III.40 displays the free carrier concentration as a function of temperature. From the fit of the neutrality equation to the experimental data, the concentration N_N of the nitrogen donor as well as the concentration of the compensation N_C was obtained (see Table III.5). The ionization energies $E_{N(h)}$ and $E_{N(c)}$, used for the fit, were taken from admittance spectroscopy measurements (see Figure III.38) in order to reduce the number of fit parameters and, thus, gain accuracy in the evaluation.

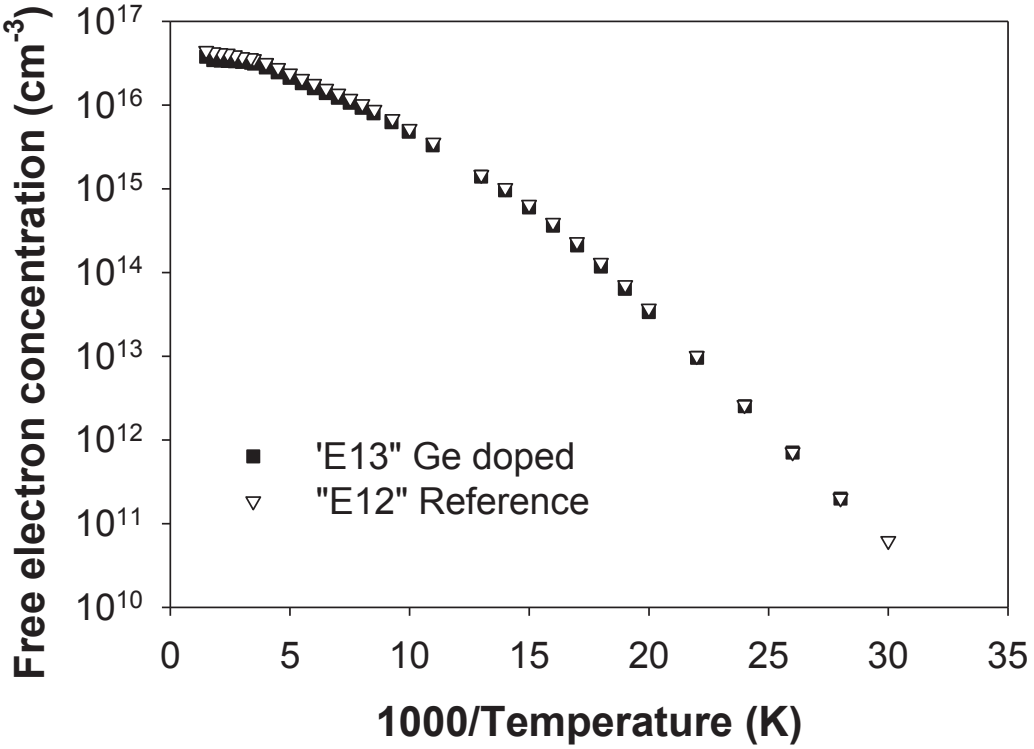


Figure III.40: Free electron concentration as a function of the temperature taken on sample "E12" (without Ge) and "E13" (with Ge).

Table III.5: Ionization energies obtained from admittance spectroscopy and concentration of the nitrogen donors and the concentration of the compensation obtained from the fit of the neutrality equation to the experimental Hall effect data and by *C-V* measurements ($N_{N,C\text{-}V}$)

	$E_{N(h)}$ [meV]	$E_{N(c)}$ [meV]	N_N [cm^{-3}]	N_C [cm^{-3}]	$N_{N,C\text{-}V}$ [cm^{-3}]
"E12" - Reference	52	99	4.2×10^{16}	6.0×10^{14}	4.5×10^{16}
"E13" - Ge doped	52	99	4.8×10^{16}	6.0×10^{14}	6.5×10^{16}

The investigated epitaxial layers reveal almost equal concentrations of nitrogen and equal compensation. Complementary capacitance-voltage (C-V) measurements, conducted on lateral Schottky diodes prepared on the very same samples, confirm the results obtained for sample "E12", but indicate a slightly higher nitrogen concentration N_N,C-V for the Ge-doped sample "E13" (see last column in Table III.5). The reason for this discrepancy is the different volume investigated by both

measurement techniques and an inhomogeneous nitrogen distribution in the epilayer. Whereas Hall effect takes into account the whole n-type epilayer with 2.5 μm thickness, C-V analysis is sensitive only in the 400 nm deep space charge region (at reverse bias of -10 V in this case).

In spite of almost equal or even higher concentrations of nitrogen in the Ge-doped sample "E13" compared to "E12", a higher Hall mobility in the whole temperature range is observed (see Figure III.41). The peak mobility for "E13" exceeds the peak mobility of "E12" by a factor of 2 at around 55 K. The same positive effect of Ge on the Hall mobility is also observed for another set of samples with higher concentration of nitrogen (not shown here). In the latter case, the mobility enhancement in the Ge-doped sample even overcompensates the increased Coulomb scattering originating from higher doping concentration. As a result of the mobility enhancement, a lower resistivity is obtained for the Ge-doped sample "E13" (Figure III.42). This observation is in agreement with conductive atomic force microscopy (C-AFM), which also confirmed the increased conductivity of Ge-enriched regions of Ge-doped layers (E11), see Figure III.34.

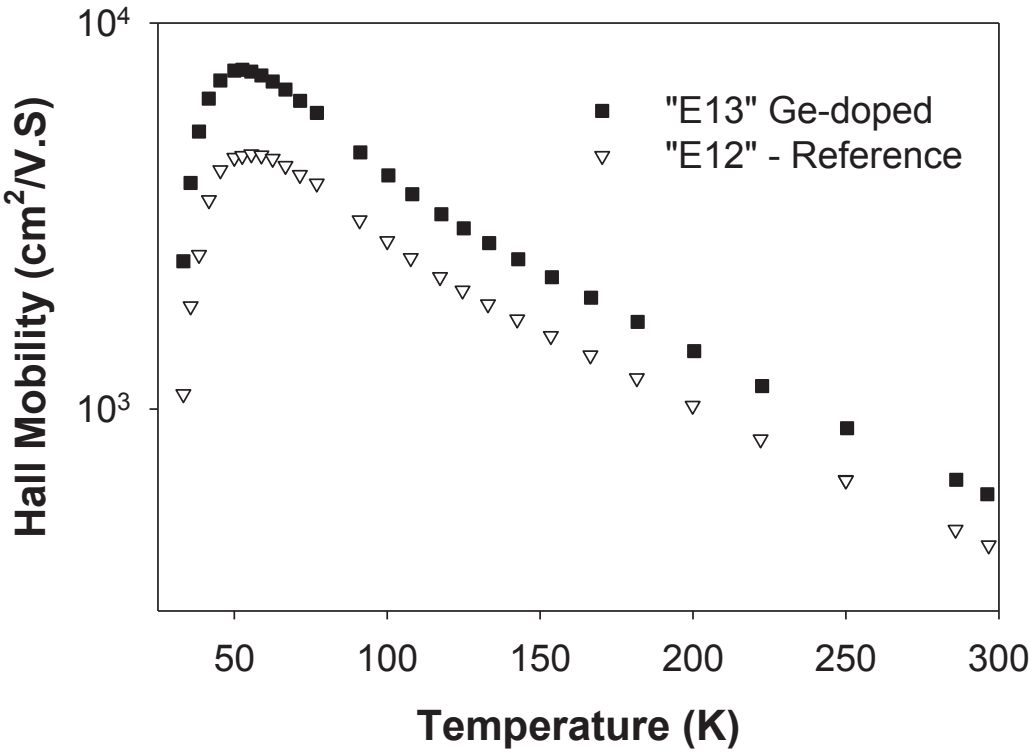


Figure III.41: Hall mobility as a function of the temperature taken on sample "E12" (reference) and "E13" (Ge-doped)

The physical origin of the positive effect of Ge on the mobility is not yet understood. However, it can be seen that the strongest effect of mobility enhancement is observed for the low-temperature mobility at T < 100 K (see Figure III.41). In this regime, the mobility is limited by scattering at ionized or neutral impurities. It is therefore speculated that Ge could getter defects. For example vacancies could be attracted by the strain field of large Ge atoms.

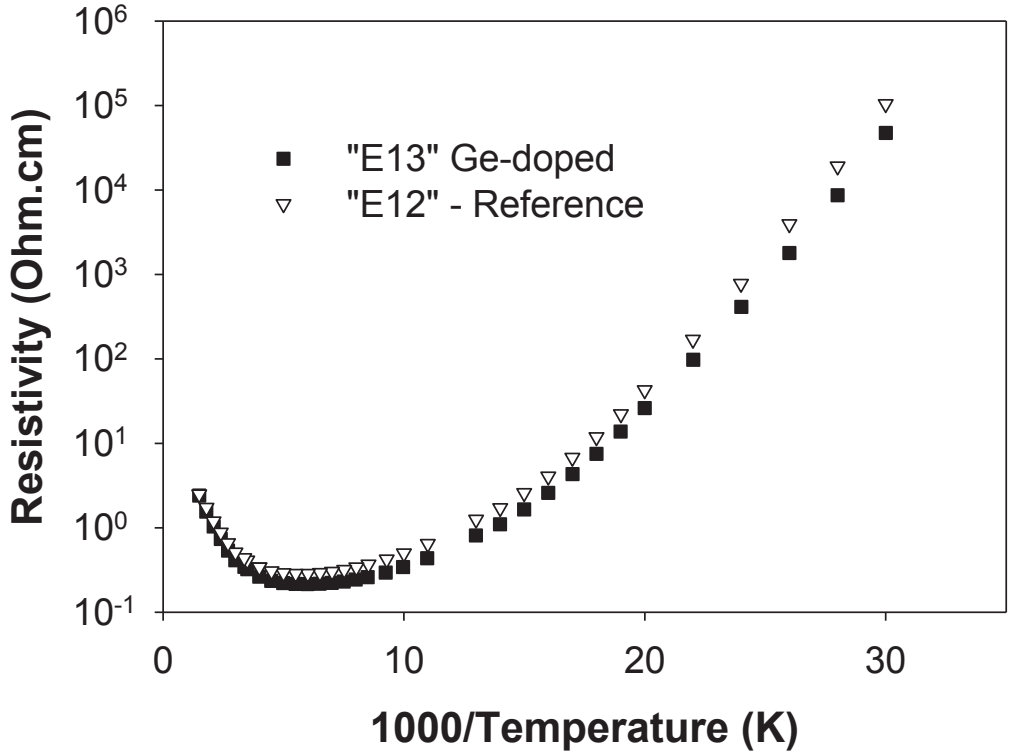


Figure III.42: Resistivity as a function of the temperature taken on sample "E12" (without Ge) and "E13" (with Ge).

III.5 Conclusion

In conclusion, adding Ge element to the Si-C-H chemical system during SiC epitaxial growth allowed exploring some fundamental aspects such as the Ge incorporation level in the lattice or its interaction with N impurity. Ge accumulation on the surface, in the form of droplets, does not affect significantly the layer quality or its level of incorporation into SiC, which is constant inside the layer. More surprising are the observed deviation from the well-known site competition rule and the interaction with N impurities. CAFM analysis confirmed the presence of an enhanced current conduction at the Ge rich areas on the surface. The Schottky performance of Ge doped sample well approaches the standard Ni_2Si/4H-SiC interface characteristics.

Incorporation of Ge during chemical vapor deposition growth leads to an increase of the Hall mobility and, as a result, to higher conductivity of 4H-SiC epitaxial layers. The influence of Ge on point defects could not experimentally be verified, but negative DLTS peaks observed in Ge-doped samples indicate the presence of charged extended defects. More work still needs to be done to understanding these findings.

III.6 References

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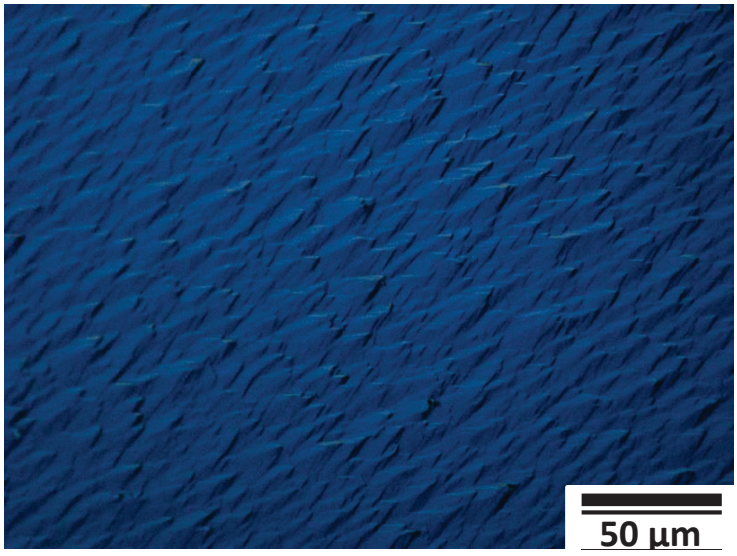
Chapter IV

Ge mediated 3C-SiC growth on low off-axis 4H-SiC substrates



Chapter IV: Contents

Chapter IV: Ge mediated 3C-SiC growth on low off-axis 4H-SiC substrates

We have shown in the previous chapter that GeH_4 addition during the growth did not significantly change the general surface morphology when growing epitaxially on 8° off axis 4H-SiC substrates. This may be different if this foreign element is introduced prior to the growth. For instance, it may affect the initial stage of SiC growth. Beneficial effect were already reported in the case of 3C-SiC heteroepitaxial nucleation and growth on Si substrate [IV.1]. While in the case of SiC growth on SiC substrates, no similar study was performed yet. As will be shown later, on 4° and 8° off 4H-SiC substrates, adding GeH_4 prior homoepitaxial growth does not induce significant changes on the morphological point of view. But when low off-axis or nominally on-axis seeds are used (i.e. when 3C-SiC growth is promoted), the morphology is very different and suggests some improvement of the 3C-SiC layer quality. These preliminary experiments are at the origin of the present chapter which will be dedicated to the heteroepitaxial growth of 3C-SiC on low off-axis (hexagonal) α-SiC substrates with the assistance of Ge. Mechanism for the 3C-SiC twin free nucleation and growth will be proposed. Last but not least, the best grown layers (i.e. from surface morphological point of view) will be characterized by electrical means for quality identification. I have participated to this characterization through a Secondment at CNR-IMM of catania.

IV.1 Bibliography of twin boundaries reduction or elimination in 3C-SiC growth on α–SiC substrates

As previously mentioned in Chapter I, despite obvious advantages in terms of chemical, lattice and thermal compatibilities compared to the use of Si substrate, the main difficulty in growing high quality 3C-SiC epilayers on α-SiC substrates lies in the quasi systematic formation of twin boundaries TB (also called double positioning boundary or DPB) within the layers. The elimination or reduction of TB has been studied by many groups. In this part will be review the main attempts performed in this direction. The more frequent attempts were using liquid-based techniques which

seem to be more adapted. For instance, vapor-liquid-solid (VLS) mechanism established the ability to produce DPB-free 3C-SiC layers [IV.2]. According to the authors, the polytypes selection occurs at the very beginning of the experiment, even before starting the growth upon propane introduction to the reactor. The simple contact of the seed with a Si–Ge melt causes the formation of 3C–SiC islands on the seed surface. This result was explained by a mechanism of dissolution-precipitation in which the seed delivers the C atoms at the origin of the 3C islands. This polytype is obtained due to the very fast growth generally associated with this kind of mechanism. Then, upon propane injection, these islands are preferentially enlarged at the expense of substrate polytypes replication, and coalesce so that a continuous 3C–SiC layer is attained. Despite the successful growth of twin free layers by VLS mechanism, issues like homogeneity, sample size and impurity level are still pending.

More recently, Ujihara et al uses top seeded solution growth (TSSG) to demonstrate high quality 3C-SiC on 6H-SiC substrate although a few DPBs and 6H– inclusions remained. The main approach of this growth method was the intentional inducement of a stacking error (i.e. 3C nucleation) just at the surface of the seed crystal and then the 3C would expand laterally and fuse with other 3C island [IV.3]. Apart from the liquid growth, using high temperature vapor phase process (CFPVT), it was demonstrated the possibility to grow large area DPB free, thick 3C-SiC layers. However, the growth parameter window for 3C-SiC is rather narrow. Thus control of the process is very difficult since small deviation from it can result in 6H-SiC growth in spiral or 2D-nucleation mode [IV.4]. There have been other few studies on the heteroepitaxial growth of 3C-SiC on 6H-SiC substrates by other techniques [IV.5, IV.6]. They pointed out the possibility of reducing the twins' density by varying different growth conditions.

The use of CVD based approach should be the best solution due its high scalability, reproducibility and the good performances of the SiC-CVD reactors. But, very few attempts were successful for DPB elimination using this technique, most probably due to the lack of a full understanding of the fundamental reasons which can help selecting one of the two possible 3C orientations.

Probably the best quality 3C-SiC material ever grown has been based on the mesa approach proposed by Neudeck et al. [IV.7, IV.8]. An ideally oriented (0001) surface,

i.e. not presenting any atomic step, should help limiting the formation of twins in heteroepixial layers of 3C-SiC by offering the same stacking (ABC or ACB) at the surface. Based on this observation, Powell et al proposed the local fabrication of such surface via 0.2x0.2 mm mesa structure obtained by plasma etching on on-axis seeds [IV.9]. Using growth condition with strong lateral growth (high temperature 1600-1700 °C), device-sized 4H/6H-SiC mesa regions with top surfaces completely free of atomic-scale steps can be grown [IV.7, IV.9], see Figure IV.1.

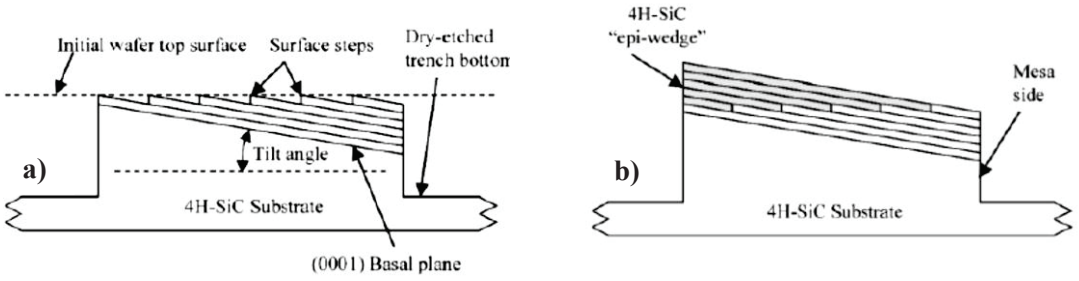


Figure IV.1: Cross sectional image of a mesa a) before epitaxy and b) step flow homoepitaxial growth without steps (end up by flat surface)

Subsequently, by lowering the temperature from 50 to 200 °C with a relatively slow ramp, a 3C-SiC layer without twins is obtained, but for some of these mesas only. Though, this process led to the elaboration of probably the best quality of 3C-SiC material ever grown, it is hampered by several limitations such as reproducibility and yield.

From the literature, it is obvious that the in-situ surface preparation of the substrate before 3C growth plays a major role in twin density reduction [IV.9 - IV.14]. Pure hydrogen or carbon-rich conditions were studied as surface preparation steps. Addition of chlorine during the growth seems to improve the process. The growth temperature could be as low as 1350°C [IV.13, IV.15] while other studies suggest better results at higher temperature [IV.16]. From all these works, some growth models were proposed to explain the twin elimination [IV.17, IV.18]. But these models need to be completed in order to take into account various growth specifications such as the presence of foreign atoms or even of a liquid phase on the surface.

It is important to note that the best results regarding 3C nucleation control on α-SiC seeds were obtained using Si-face orientation of these seeds. This is due to the

fact that the lower surface energy of the C-face reduces the energetic barrier for nucleation. It leads to the formation of a high density of nuclei and thus to uncontrolled nucleation.

As a result, more work is needed to understand and master the nucleation and growth in this difficult heteroepitaxial system. In the present study, we report the effect of adding GeH_4 to the standard chemistry H_2-SiH_4-C_3H_8 CVD system on the nucleation and growth of 3C-SiC on α-SiC substrate. We will show that such approach may help finding the appropriate conditions for TB elimination.

IV.2 Experimental section

The growth procedure is similar to that previously presented and discussed in Chapter III except the use of specific gas mixtures (H_2 + one or two precursors) during the in situ surface pre-treatment of the substrates, i.e. before adding SiH_4 and C_3H_8 to start the CVD growth., see Figure IV.2. These pre-treatments typically involved introducing the precursors in the reactor at 1500 °C for 10 min.

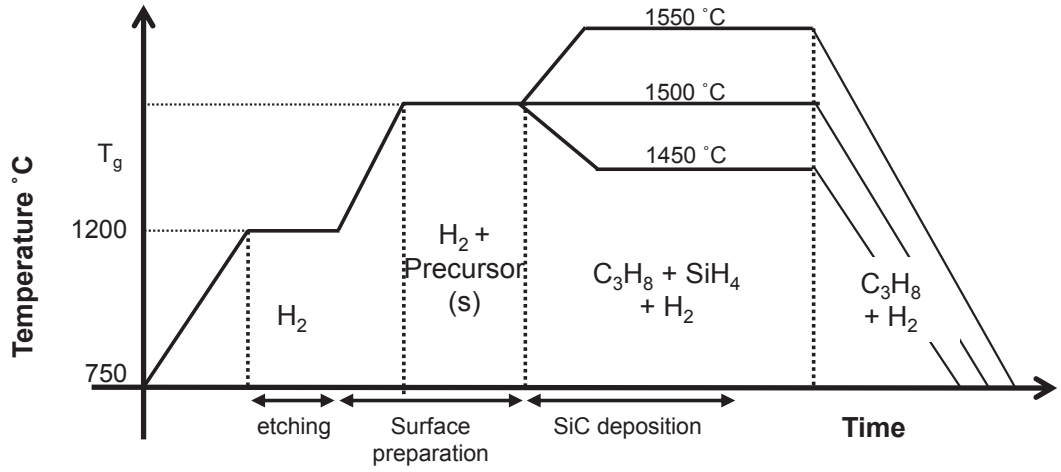


Figure IV.2: CVD epitaxial growth procedure used for mediating the 3C-SiC growth on α-SiC substrates

This study involved mainly the use of H_2+GeH_4 gas mixture while other mixtures were also tested for either complementary or comparison issues (Table IV.1). Addition of GeH_4 gas (0.02 to 0.2 sccm) was sometimes done also during the deposition time.

Table IV.1: The different gas mixtures studied for the surface preparation step before 3C-SiC growth

Gas mixture
$H_2 + GeH_4$
$H_2 + C_3H_8$
$H_2 + SiH_4$
$H_2 + C_3H_8 + GeH_4$

High purity hydrogen (16 slm), silane (1.25 to 5 sccm) and propane (2.1 to 8.33 sccm) are used, respectively, as vector gas and precursors for the SiC growth. C/Si ratio was set to 5 except when mentioned differently. The growth rate was changed from 1.25 to 5 µm/h depending on the used SiH_4 flux. The growth time was fixed at 1 hour.

The deposition occurred on 1x1 cm^2 pieces sawed from complete commercial 4H-SiC or 6H-SiC wafers (see Table IV.2 for more details). Results that will be presented hereafter are mostly obtained on on-axis (0001) Si face seeds unless mentioned differently.

Table IV.2: Main characteristics of the SiC substrates used in this chapter

Polytype	Face	Misorientation	Thickness(µm)	doping
4H-SiC (0001)	Si	on axis	250	$>10^{18}$ at.cm^{-3}
4H-SiC (0001)	Si	1 °	250	$>10^{18}$ at.cm^{-3}
6H-SiC (0001)	Si	on axis	250	$<10^{18}$ at.cm^{-3}
6H-SiC (0001)	Si	1 °	250	$<10^{18}$ at.cm^{-3}

IV.3 Growth Results

IV.3.1 Effect of GeH_4 addition

Our usual in situ surface preparation step before homoepitaxial 4H-SiC growth involves an etching under C_3H_8 for 10 min. When using such simple procedure, the 3C-SiC layer grown at 1500°C is highly twinned as can be seen in Figure IV.3 which displays a dense and random network of DPBs. These lines are in fact shallow grooves, which are probably due to a slightly smaller growth rate above the DPBs than far from them. Similar result is obtained when keeping the same surface preparation and adding 0.1 sccm GeH_4 during the growth (Figure IV.3b). The average density, size and shape of the DPBs are not much affected by the addition of

GeH_4. Note in this case that some Ge accumulates on the surface and forms micrometric to nanometric droplets decorating the DPBs.

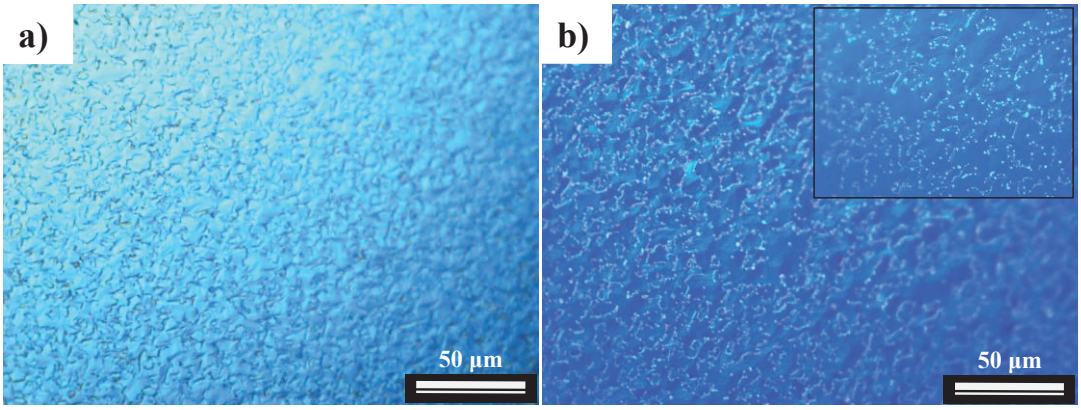


Figure IV. 3: Surface morphology of 3C-SiC grown layers using pretreatment of 10 min at 1500°C under 2.5 sccm C_3H_8: a) without GeH_4 addition and b) with 0.1 sccm GeH_4 addition during the deposition time.

If 0.02 sccm of GeH_4 is now added together with propane during the in situ surface preparation, no change in the surface morphology can be noticed. But if the GeH_4 flux increases to 0.06 sccm or higher (while keeping propane constant), the morphology significantly evolves (Figure IV.4). µ-Raman analyses were performed in order to obtain more information on the local nature of the deposit. One can see on Figure IV.4b the LO peak for both 4H-SiC and 3C-SiC located at 965 at 972 respectively. Thus, the layer is still composed mostly of 3C polytype (i.e. mixing polytypes of 3C and 4H exists) but exhibits elongated features, oriented toward the same directions. This is first evidence that Ge element can modify the 3C nucleation on low off axis SiC substrate.

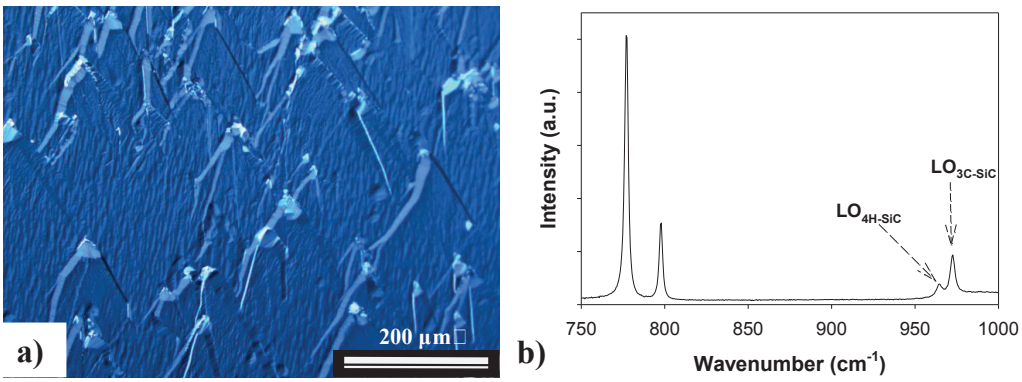


Figure IV. 4: Surface morphology of a layer grown at 1500°C using a surface preparation under 0.06 sccm of GeH_4 together with 2.5 sccm of C_3H_8.

Now, using GeH_4 alone (without C_3H_8) during the 10 minutes surface preparation leads to considerable morphological changes. The best result was obtained for the case of 0.06 sccm GeH_4 flux (Figure IV.5). The layer is globally much smoother and is composed of triangular hillocks (all oriented toward the same direction) surrounded by large step bunched areas (Figure IV.5a). µ-Raman spectroscopy evidenced that the layer is of 100 % 3C polytypes (no fingerprint of 4H from epi is seen, i.e. LO_{965}), even on the triangular hillocks (Figure IV.5b). The most surprising and positive result came from EBSD phase mapping which shows that the layer is not only 100% 3C-SiC, but also it is almost twin free (Figure IV.5d). In particular, no twining could be detected at the places where the triangles are located.

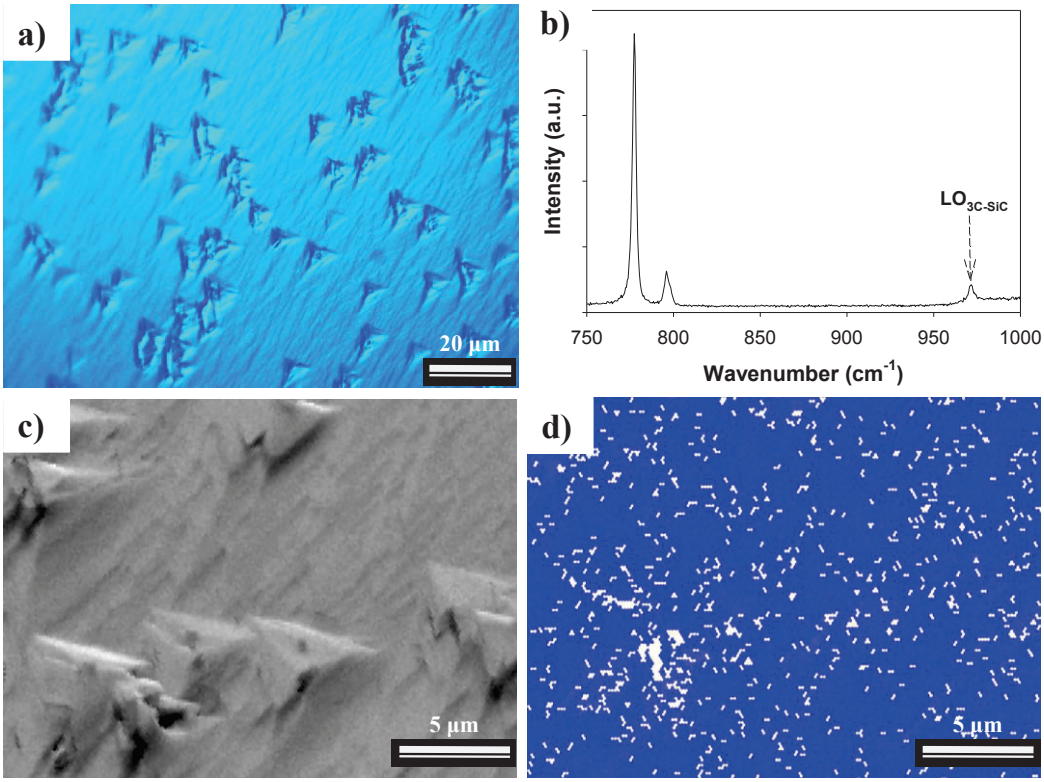


Figure IV.5: Characterization of a 3C-SiC layer grown after surface preparation of 10 min under 0.06 sccm GeH_4 : a) Surface morphology as observed by optical microscopy, b) µ-Raman spectrum recorded on a triangular hillock, c) and d) respectively SEM image and EBSD phase mapping of the same area; In d), with blue code meaning that the area has only one 3C orientation denoted as 3C(II) and the white spots corresponds to areas which could not be indexed by the software due to local surface roughness.

When using the minimum GeH_4 flux (0.02 sccm) for surface preparation (Figure IV.6a), the layer appears similar to that grown when adding both GeH_4 and C_3H_8

(Figure IV.4). EBSD phase mapping showed that the layer is mostly composed of twinned 3C with few hexagonal inclusions (Figure IV.6b).

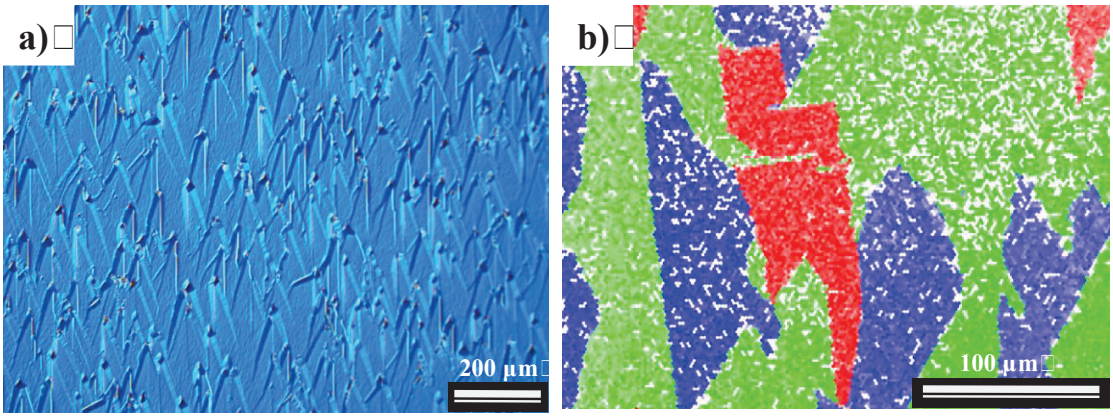


Figure IV.6: Characterization of a SiC layer grown after surface preparation of 10 min under 0.02 sccm GeH4 : a) Surface morphology as observed by optical microscopy, b) EBSD phase mapping; In b), the color code is green = 3C(I), blue = 3C(II), red = 4H, white = areas which could not be indexed by the software due to local surface roughness.

When increasing GeH_4 flux to 0.10 sccm, the layer was mainly homoepitaxial with high amount of carrot like 3C inclusions (Figure IV.7).

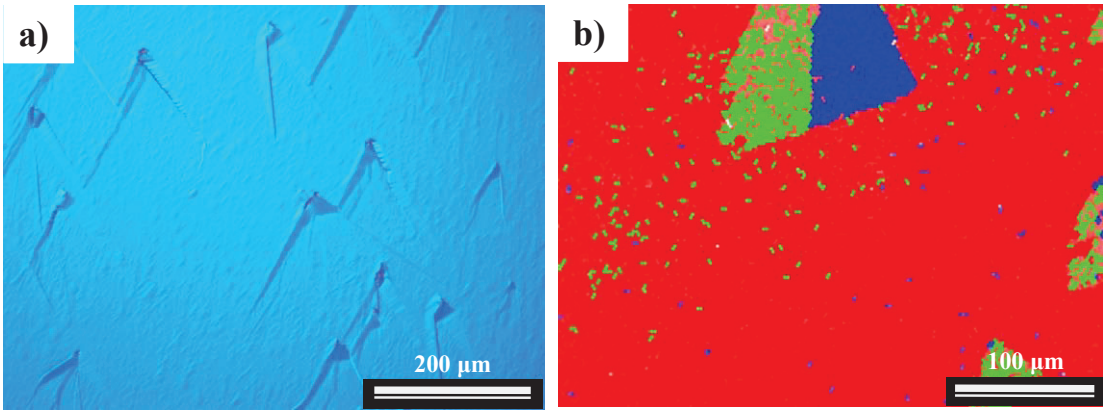


Figure IV.7: Characterization of a SiC layer grown after surface preparation of 10 min under 0.1 sccm GeH4 : a) Surface morphology as observed by optical microscopy, b) EBSD phase mapping; In b), the color code is green = 3C(I), blue = 3C(II), red = 4H, white = areas which could not be indexed by the software due to local surface roughness.

By further increase of GeH_4 flux to 0.20 sccm during surface preparation, the morphology after CVD growth was rather similar as with 0.10 sccm of GeH_4, i.e. mainly 4H homoepitaxial layers with triangular 3C inclusions Figure IV.8a.

For comparison purpose, an experiment was performed using SiH_4 instead of GeH_4 during the surface preparation, at a flux of 0.06 sccm (identical as for sample shown in Figure IV.5). In this case, the layer morphology (Figure IV.8b) is rather similar to the one obtained using higher GeH_4 flux during the surface preparation. Raman spectroscopy (Figure IV.8c) confirmed that the layer is mostly of 4H polytypes since the LO_{972} that is connected to 3C-SiC is not visible.

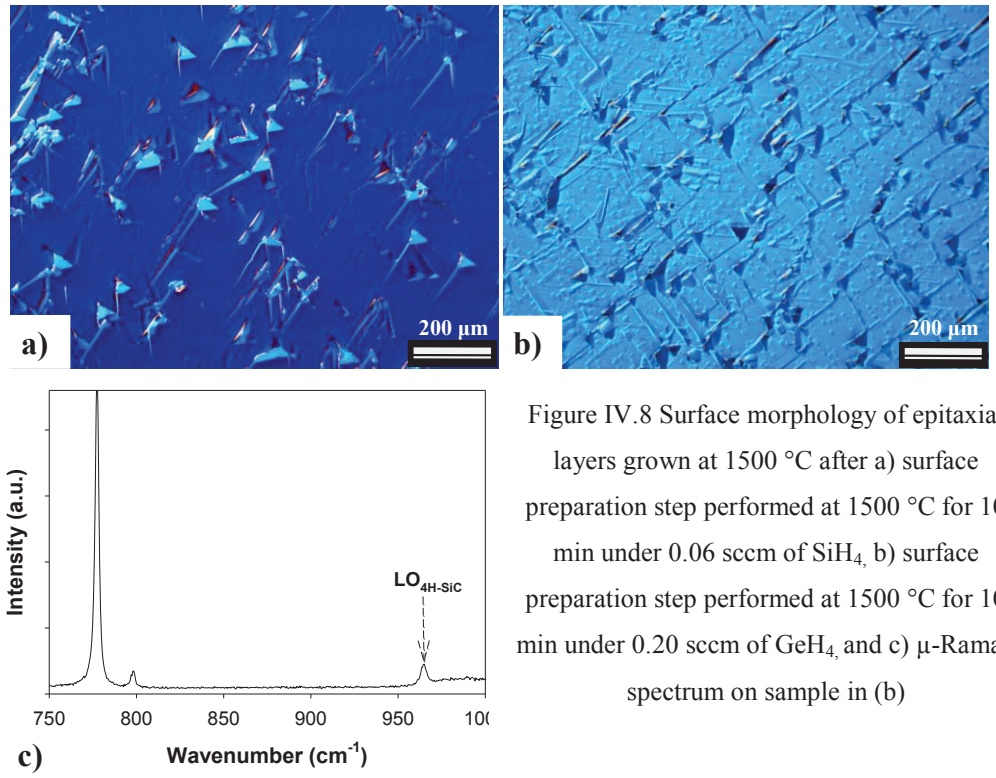


Figure IV.8 Surface morphology of epitaxial layers grown at 1500 °C after a) surface preparation step performed at 1500 °C for 10 min under 0.06 sccm of SiH_4, b) surface preparation step performed at 1500 °C for 10 min under 0.20 sccm of GeH_4, and c) µ-Raman spectrum on sample in (b)

IV.3.2 Effect of growth conditions

C/Si ratio, growth temperature and growth rate are the major parameters either for stabilizing one polytype over the other or determining the quality of the grown layer. Hence, the influence of these parameters has been studied by keeping the same preparation step as for the best grown 3C-SiC sample shown in Figure IV.5 (GeH_4 = 0.06 sccm at 1500°C for 10 min). For growth temperatures different than 1500°C, the temperature transition step was very short (< 30 sec) and performed under H_2 only.

After growth at 1450°C, the layer looks very similar to the one grown at 1500°C (Figure IV.9). The surface is again decorated by triangular features, which have apparent smaller mean size and higher density compared to those seen on sample grown at 1500°C. The size is smaller by 40 % and the density is almost twice.

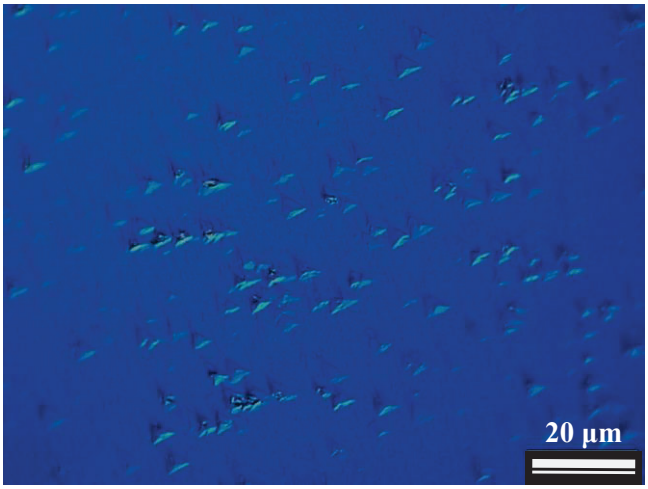


Figure IV.9: Surface morphology of epitaxial layers grown after the optimal surface preparation step (1500°C for 10 min under 0.06 sccm of GeH_4) and growth temperature of 1450°C and C/Si ratio of 5

On the other hand when the growth temperature is increased to 1550°C, the layer is mostly 4H-SiC homoepitaxy (as detected by Raman spectroscopy) with a high density of triangular defects (Figure IV.10). This is more or less a similar morphology as in Figure IV.8a but with higher density of defects.

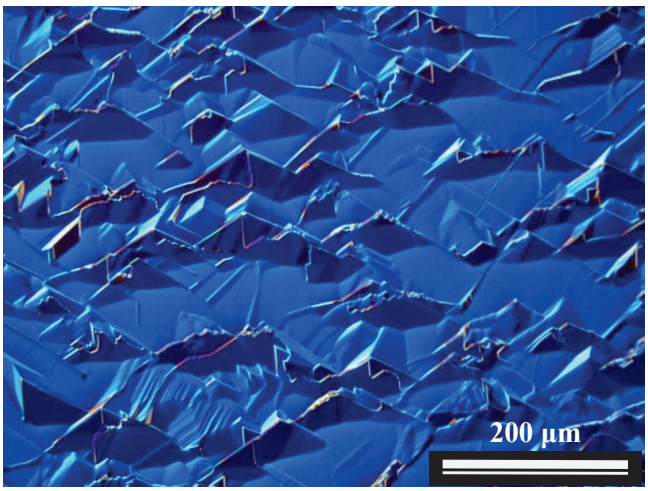


Figure IV.10: Surface morphology of epitaxial layers grown after the optimal surface preparation step (1500°C for 10 min under 0.06 sccm of GeH_4) and growth temperature of 1550°C and C/Si ratio of 5

Concerning the effect of the C/Si ratio, an increase of this ratio to 8 (for a growth at 1500 °C) did not induce any morphological difference compared to C/Si of 5 (Figure IV.5), i.e. with the formation of small triangular hillocks, suggesting a twin-free 3C-SiC layer. But when the C/Si ratio was decreased to 3, the morphology changed significantly (Figure IV.11) and the layer is found to be a mixing of polytypes, as detected by µ-Raman analyses performed at various areas.

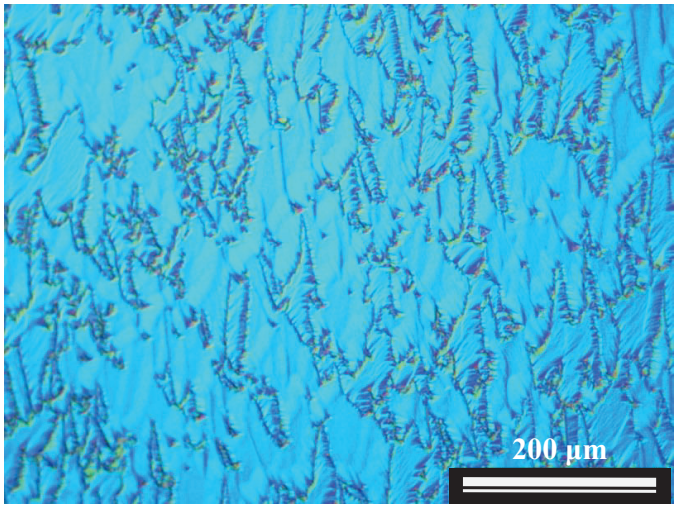


Figure IV.11: Surface morphology of epitaxial layers grown after the optimal surface preparation step (1500°C for 10 min under 0.06 sccm of GeH_4) at growth temperature of 1500°C and C/Si of 3

The effect of the growth rate was investigated within the range 1.25 – 5 µm/h. The growth time is kept constant at 1 hour. At high growth rate of 5 µm/h (Figure IV.13), the layer is clearly single domain 3C-SiC like for sample in Figure IV.5 (grown at 2.5 µm/h). The main difference is an overall rougher surface with higher density of triangular hillocks.

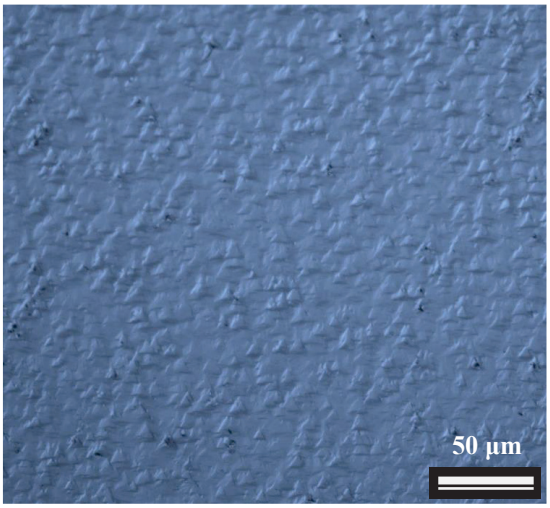


Figure IV.12: Surface morphology of epitaxial layers grown after the optimal surface preparation step (1500°C for 10 min under 0.06 sccm of GeH_4) ar growth rate of 5 µm/h and C/Si ratio of 5

On the other hand, the use of low growth rate (1.25 µm/h) resulted in very smooth morphology without observable triangular hillocks or step bunching by Nomarski optical microscopy (Figure IV.13). Confirmation of the 3C-SiC polytype was obtained from EBSD investigation which also revealed that the layer is single domain, Figure IV.13b.

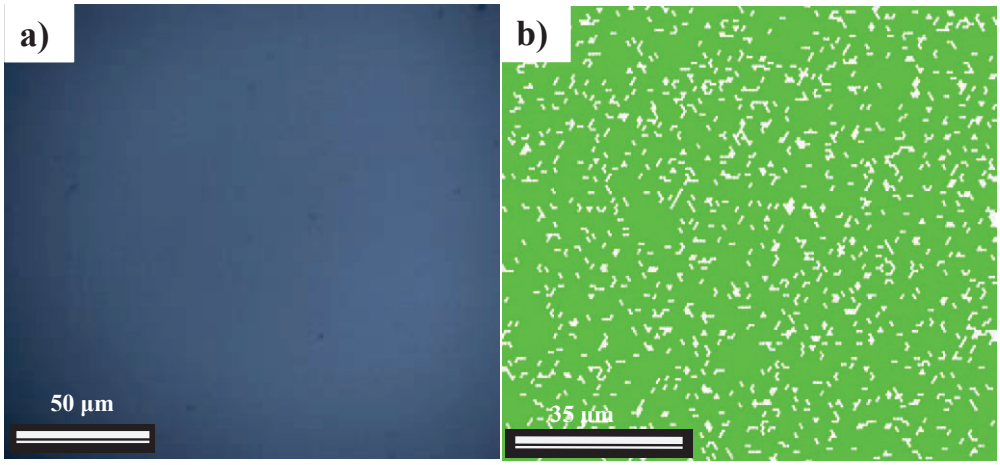


Figure IV.13: Surface morphology of epitaxial layers grown after the optimal surface preparation step (1500°C for 10 min under 0.06 sccm of GeH_4) : a) growth rate of 1.25 µm/h, C/Si ratio of 5; in b) is shown the EBSD phase mapping of sample displayed in b), with green code meaning that the area has only one 3C orientation denoted as 3C(I) and the white spots corresponds to areas which could not be indexed by the image software

IV.3.3 Thickening

It was previously shown that high temperature regrowth on top of 3C-SiC VLS seed could lead to surface smoothening [IV.19]. That is why the twin-free 3C-SiC layer shown in Figure IV.5 was subjected to a CVD regrowth at 1600 °C to try eliminating the triangular features. Figure IV.14 shows the resulting morphology after 8.5 µm thick regrowth at 1600 °C and C/Si of 5. One can notice that this thickening led to complete elimination of the triangular features. Instead, the regular 60° jagged step bunching was enhanced and homogeneously distributed on the entire sample.

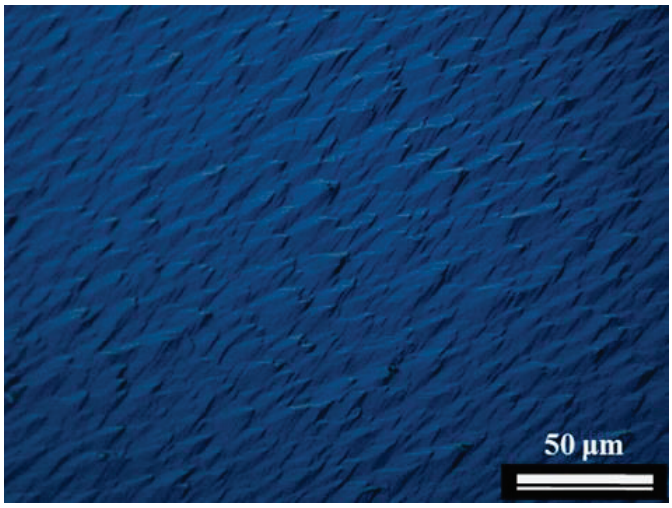


Figure IV. 14: Optical image of layer shown in Figure IV.5 after 8.5 µm thickening at 1600 °C with a C/Si ratio of 5.

The resulting 11 µm thick "re-grown" layer looks obviously rougher than before thickening. This is better seen from the AFM images recorded before and after thickening. The morphological analyses obtained by AFM on a scan area of 50×50 μm^2 of the two 3C-SiC epilayers are reported in Figure IV.15a and Figure IV.15b. For the first growth, the RMS (acquired excluding the triangular hillocks) was 5.5 nm while it reaches 17.4 nm after the 8.5 µm further thickening. It is also worth noting that, in the "regrown" sample, the size and height of the steps increased significantly. Besides these morphological features, the first grown sample shows several surface defects (i.e., the triangular hillocks visible with a bright contrast in Figure IV.15a which are some hundreds nanometers high and some micrometers in width.

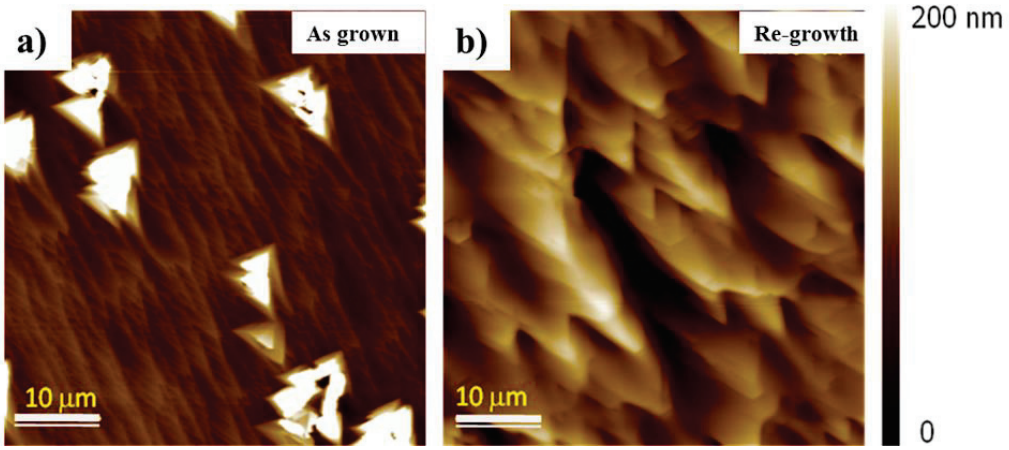


Figure IV.15: 50×50 μm^2 AFM images of a) the as-grown layer shown in fig. 3a and b) the regrowth sample in Figure IV.14.

IV.3.4 6H-SiC attemps

Based on the literature, the most frequent used substrate in the 3C-SiC/α-SiC system is 6H-SiC. This is more or less historical since the first commercially available SiC substrates were of 6H polytypes and their crystalline quality and size remained for long higher than 4H ones. In addition, some studies were mentioning that it is easier to prepare a nicely reconstructed step and terrace structure with 6H-SiC seeds compared to 4H-SiC [IV.20]. This is believed to be primary importance for controlling the 3C-SiC nucleation and thus eliminating the DPBs. For this reason and for comparison purpose we performed some attempts on 6H-SiC (0001) Si face on-axis, 1° and 2° off-axis substrates. Using the same optimal growth procedure as for 4H-SiC (i.e. 1500 °C, C/Si=5, 0.06 sccm of GeH_4 during surface preparation) the layers grown on off-axis seeds were rather smooth with few triangular defects (see

Figure IV.16). µ-Raman spectroscopy revealed that the layers are of 6H polytypes, not 3C-SiC, even for 1° off-axis. This result goes in the same trend as in the literature which suggests that 6H-SiC homoepitaxy is easier to obtain than 4H ones even on low off-axis [IV.21], though 1° off is unusually low off-axis for homoepitaxy.

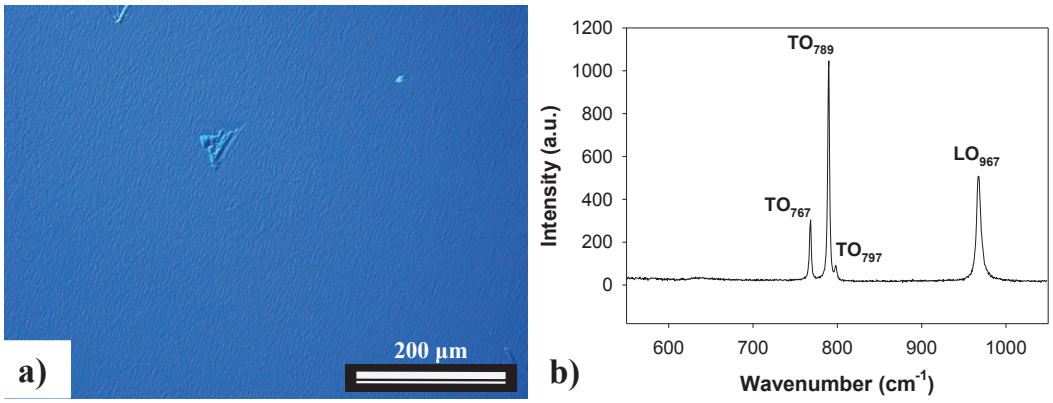


Figure IV.16: Surface morphology of epitaxial layers grown on 1 ° off-axis 6H-SiC seed after a) surface preparation step performed at 1500 °C for 10 min under 0.06 sccm of GeH_4, and growth at 1500 °C, b) µ-Raman spectrum on this sample showing the characteristic peaks of 6H-SiC.

Contrary to the misoriented seeds, the on-axis 6H-SiC always led to 3C-SiC growth (within the studied parameters). Indeed, a twin free 3C-SiC epilayer has been obtained on 6H-SiC seeds with optimum GeH_4 flux (during surface preparation) higher than that normally required in case of 4H-SiC seeds (Figure IV.17a). In this case, the surface displays high density of triangular hillocks and it gets slightly rougher upon further thickening at 1600 °C (Figure IV.17b).

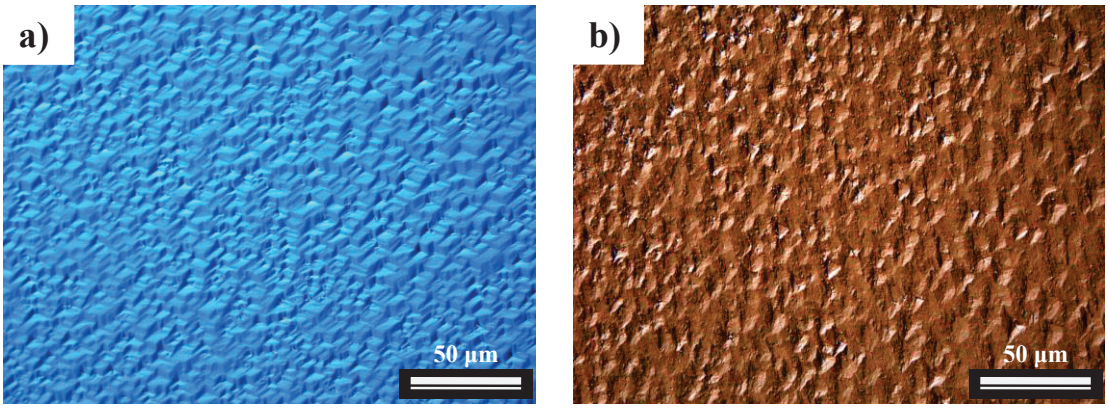


Figure IV.17 a) Surface morphology of epitaxial layers grown on on-axis 6H-SiC substrate after surface preparation step (1500°C for 10 min under 0.10 sccm of GeH_4) at growth temperature of 1500°C and C/Si of 5,in b) Optical image of layer shown in (a) after 6 µm thickening at 1600 °C with a C/Si ratio of 5

IV.3.5 Nucleation study

To better understand the role of Ge in the nucleation stage of 3C-SiC, a series of experiments targeting the early stage of growth was performed. Such study was rather difficult so that 1° off oriented substrates were used for reducing the scattering of the results thanks to off orientation control. The first parameter to be checked was the effect of Ge droplets on the surface morphology/reconstruction of the 4H-SiC seeds. After performing a 10 min surface preparation under 0.06 sccm GeH_4, the sample was cooled down and analyzed. Not surprisingly, spherical droplets were seen on the surface and identified as pure Ge by µ-Raman spectroscopy (Figure IV.18). Away from the spherical droplets, no growth features are seen. Particle's size ranges from 2 – 3 µm.

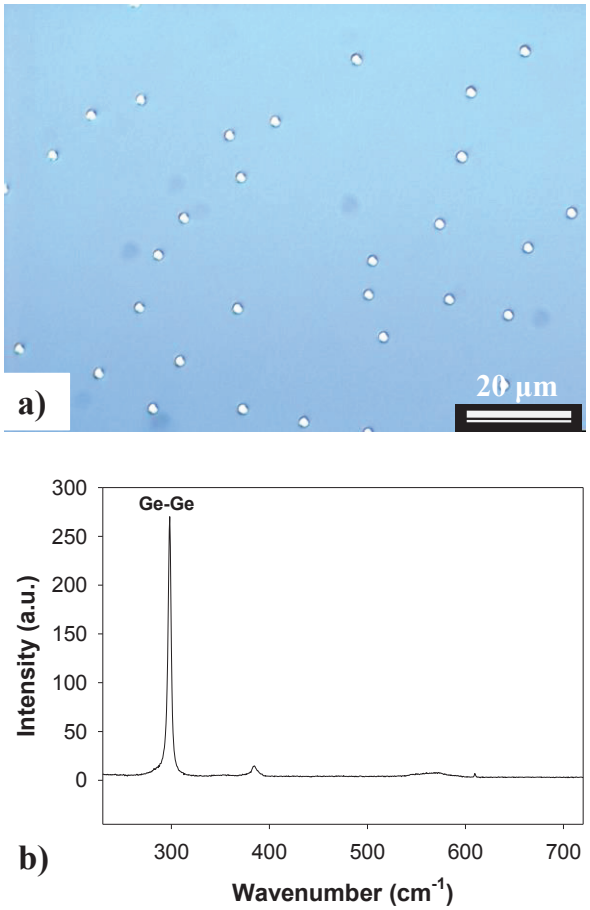


Figure IV.18: a) Nomarski optical image of 4H-SiC substrate after surface pretreatment performed at 1500 °C for 10 minutes under 0.06 sccm of GeH_4, b) µ-Raman spectrum obtained on a single droplet of the same sample

After chemical etching of these droplets, AFM revealed that the surface does not exhibit any specific surface morphology feature like macro-step (Figure IV.19). As a first conclusion, GeH_4 gas is not modifying significantly the surface of the seed before starting the growth.

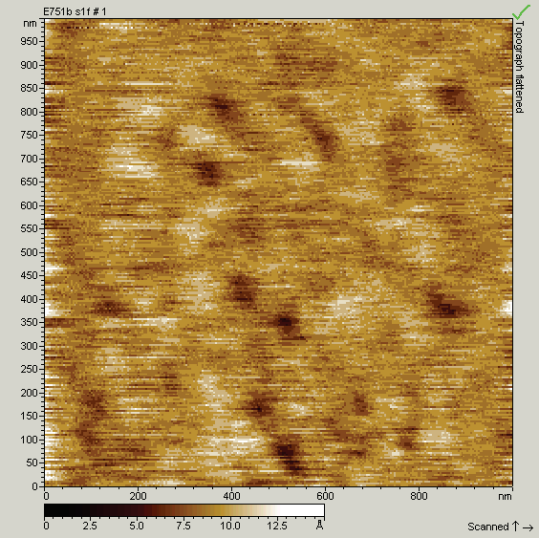


Figure IV.19: AFM image (1x1 µm^2 scan) showing the surface morphology of a sample treated 10 min at 1500°C under 0,06 sccm GeH_4, after wet etching of the accumulated Ge droplets on the surface. Z-scale varies from 0-15 Å.

The next step is to see what is happening to this surface at the early stage of SiC growth. Towards this end, three samples were fabricated with similar surface preparations (i.e. the optimized surface preparation that giving fully twin free 3C-SiC epilayer) followed by 30, 60 and 90 s growth respectively, see Table IV.3.

Table IV. 3: Growth conditions of the nucleation study

Name	Substrate	Tg (°C)	Gr (µm/h)	C/Si ratio	Time (sec)
Sample 1	1°off-axis 4H-SiC	1500	2.5	5	**30**
Sample 2	1°off-axis 4H-SiC	1500	2.5	5	**60**
Sample 3	1°off-axis 4H-SiC	1500	2.5	5	**90**

* Tg: growth temperature, ** Gr: Growth rate

On the sample grown with the shortest time, the presence of Ge droplets was still seen on the surface. AFM characterization on this sample showed that the surface is now composed of regular parallel steps with some local triangular protrusions (Figure IV.20a). The measured step height is around 22 nm. EBSD phase mapping of this sample suggests that the protrusions are made of 3C-SiC (Green) while the surrounding is 4H-SiC (Red) (Figure IV.20b). Note that this 3C-SiC is predominantly of one orientation. The surface coverage of 3C-SiC increases after 60 seconds growth while Ge is no more detected on the surface (Figure IV.20c). Again, the 3C-SiC is predominantly of one orientation. Finally, an almost complete 3C layer with nearly

one orientation is then observed after 90 seconds of growth (Figure IV.20d). The twinned areas are very small and isolated one to each other.

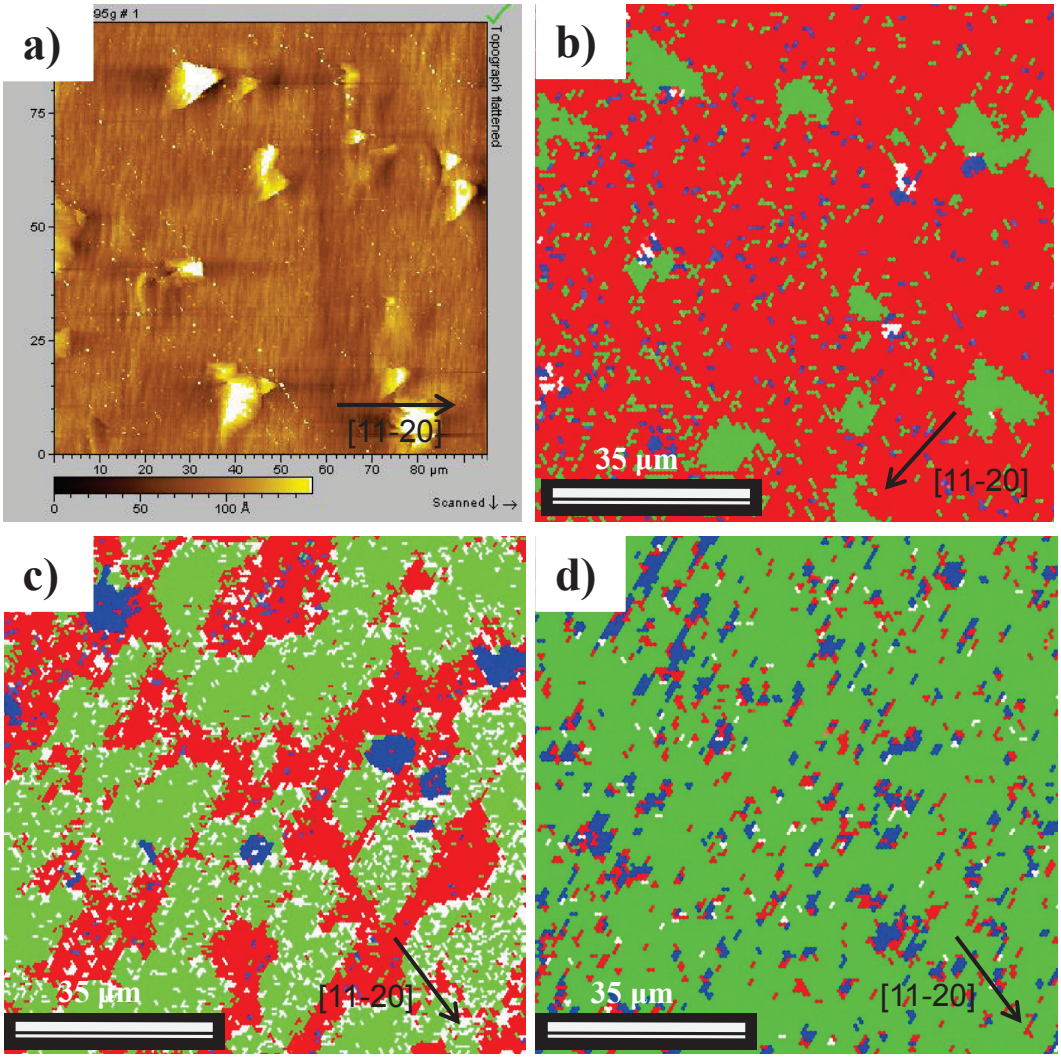


Figure IV.20: AFM and EBSD characterization of the 3C-SiC nucleation experiments performed for 30, 60 and 90 seconds at 1500°C after optimal GeH_4 surface preparation for obtaining 3C twin free layer. a) 95×95 µm^2 AFM image of the 30 seconds growth experiment and b) is its equivalent EBSD imaging. c) and d) are the EBSD mapping of the 60 and 90 seconds experiment respectively. The color code is green = 3C(I), blue = 3C(II), red = 4H, white = areas which could not be indexed by the software due to local surface roughness.

IV. 4 Discussion

IV.4.1 The role of Ge in twin boundary elimination

From these results, it is obvious that Ge element can help improving the quality of the 3C-SiC grown on low off-axis 4H-SiC (0001) substrate. However, its effective

role needs to be clarified. When GeH_4 is simply added during the growth, DPB density in the grown layer is the same as without GeH_4 addition. This later means at least that Ge element does not favor the elimination of the DPBs, for instance by changing their propagation direction like mentioned in ref [IV.22]. Ge atoms basically accumulate on the surface and incorporate to a certain extent inside the matrix (see Chapter III), but apparently do not affect significantly the growth itself. When considering the positive results obtained when adding GeH_4 during surface preparation, one can say that, in order to affect SiC nucleation, Ge needs to be present on the surface in a certain amount before starting the growth. Namely, it is not enough to introduce GeH_4 at the same time as starting SiC growth.

When GeH_4 is introduced during the surface preparation, the most obvious consequence is its accumulation on the surface under the form of separated droplets whose size depends on the GeH_4 flux. The simple presence of Ge droplets on the surface directly affects the 3C-SiC nucleation. However, in order to eliminate the DPBs from the 3C-SiC grown layer, having Ge droplets on the surface before growth is not enough. For instance, if propane is added to GeH_4 or if the GeH_4 flow itself is not adequate during surface preparation, then DPBs are formed or 4H polytype inclusions can be obtained.

Clearly, according to the literature works, the exact mechanism allowing DPB elimination inside vapor phase grown 3C-SiC on α-SiC substrate is still under debate [IV.10, IV.16, IV.17, IV.23]. In all the works, the surface preparation is reported to be a crucial phase and interaction of the nuclei with step edges is also mentioned. Indeed, our present investigation confirms the importance of this surface preparation step. The best proof is that the parameter window for surface preparation is very narrow (only 0.06 sccm GeH_4, without other gases) while it is much less narrow for the growth itself (temperature from 1450 and 1500 °C, C/Si ratio from 5 to 8 and growth rate between 1.25 to 5 µm/h).

From the results of the nucleation study, we propose the following mechanism which is summarized in Figure IV.21. From the nucleation study, the first conclusion which can be made is that growth does not start directly with 3C-SiC but with a transient 4H-SiC homoepitaxial period (Figure IV.20b). This delay in 3C-SiC growth is attributed to the presence of Ge atoms on the surface. Indeed, as seen from Figure IV.8, a high flux of GeH_4 during surface preparation promotes the stabilization

of 4H homoepitaxy against 3C nucleation despite the low off-axis of the seeds. In order to interpret this result different scenarios can be proposed. Ge atoms can induce an enhancement of the surface mobility of Si and C adatoms so that they can more easily reach the step edges. Another possibility is that Ge can reduce (or even remove) the 3C nucleation sites or can lower the probability of 2D nucleation on terraces. Note that these two proposed effects of Ge atoms do not take into account the fact that these Ge atoms are agglomerated under the form of droplets. We believe that the main effect of these droplets is to act as many local sources of gaseous Ge by their progressive evaporation.

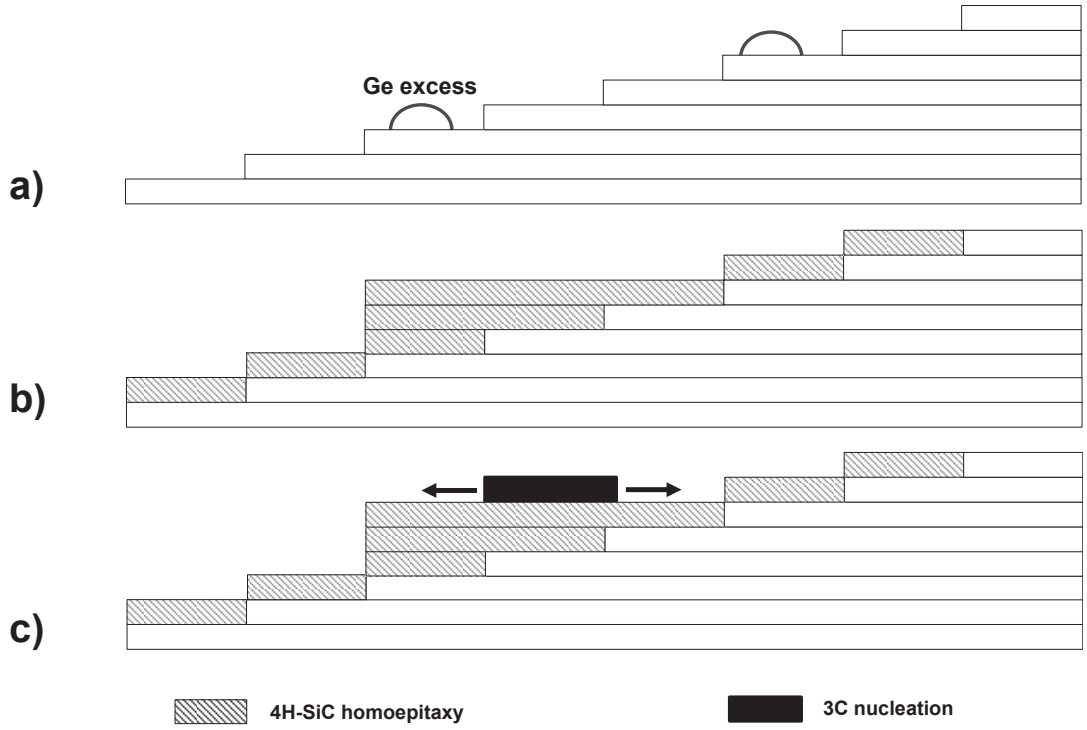


Figure IV.21: Mechanism of Ge assisted 3C nucleation on 4H-SiC low off axis seed. (a), 4H-SiC substrate with GeH_4 surface preparation, (b), starting the growth by 4H-homoepitaxy along with the formation of on-axis facets, and (c), nucleation of a 3C-SiC island on the facet and expansion toward all directions.

After the initial homoepitaxial growth, the step front should start to become irregular with the local formation of on-axis facets (Figure IV.20b). These facets should be preferential sites for 3C nucleation (Figure IV.20b). Then the 3C coverage increases either by lateral expansion of the initial nuclei or by the formation of new on-axis facets and 3C nucleation on them, until an almost complete 3C coverage is reached (Figure IV.20d). Note that the preferential selection of one orientation of the

deposited 3C (which should lead to DPB free layer) seems to occur from the beginning. The lateral expansion of the 3C nuclei favors selecting at the end one among the two possible orientations. Such mechanism is very similar to the one proposed by Latu-Romain et al [IV.17]. It is important to emphasize that within this scenario Ge atoms are just directly affecting the homoepitaxial growth and the faceting. The 3C-SiC nucleation is only the consequence of the faceting.

Another important conclusion from this nucleation study is that, to avoid twin formation, one has to finely control the 3C nucleation. In the present work, this is a self-controlled process mediated by the presence of Ge on the surface. Ge should play the role of transient 4H homoepitaxy promoter so that SiC growth does not start with 3C-SiC. The transition from 4H to 3C occurs smoothly, at separated places where on-axis facets form, which should leave the time for the early nucleated 3C islands to expand laterally. Though the exact reason for orientation selection is still to be found, we believe that the key parameter is to be able to move progressively from homo to heteroepitaxy, in the same way as in reference [IV.17].

In the proposed model, the collision between the 3C islands and the growth steps should not be ignored. Since such interaction is unavoidable and the lateral expansion of 3C-SiC islands can produce either double-positioning boundary (DPB) and/or stacking fault (SF) defects (Figure IV.22) [IV.24]. This model is also known as “selection rule” which has to be considered in the proposed mechanism of Figure IV.21. It can be simplified as follows : a seed surface displaying only steps of one unit cell height (1c step) would lead to equivalent 3C stacking on each side of the step while steps of half unit cell height (c/2 step) would generate TBs (Figure IV.22a). According to this model, stacking faults (SFs) should be generated above 1c steps of a 4H-SiC seed while perfect coherence should be obtained above such steps for a 6H-SiC seed.

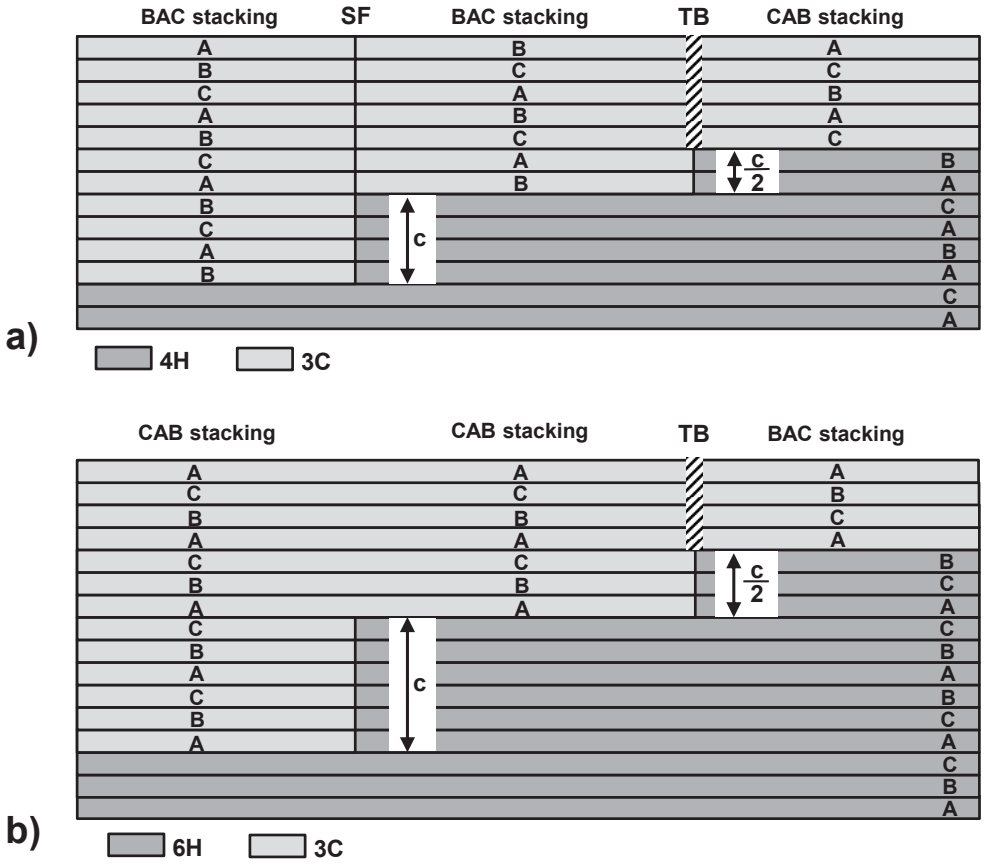


Figure IV.22: Schematic illustration of the " selection rule" applied to a) 4H-SiC and b) 6H-SiC seeds. c/2 steps lead systematically to T formation while 1c steps only generates SF in the case of 4H.

Some of the samples grown in this study display both 4H and 3C areas which suggest a competition between homo and heteroepitaxy all along the growth runs. This corresponds to layers grown with high GeH_4 fluxes, low C/Si ratios or high temperatures. High temperatures and low C/Si ratios are known parameter promoting homoepitaxy [IV.16]. And as discussed earlier, excess of Ge atoms on the surface seems to promote homoepitaxy. As a consequence, using conditions promoting too much 4H homoepitaxy is not good for twin boundary elimination. It probably delays too much the transition from 4H to 3C so that the 3C nucleation is too scarce. It then remains as isolated islands and leads to the formation of 3C inclusions in a hexagonal layer.

IV.4.2 Other growth features

All the twin free layers obtained in this study display triangular hillocks on the surface, which do not correspond to inclusions of polytype or to twinned 3C areas. We believe that this could be the result of some overgrowth of these early formed

inclusions. After thickening of a twin free layer, we have shown that all the triangular hillocks have vanished (Figure IV.14), which means that they are just transient morphological features. This result goes well with the hypothesis of early inclusion overgrowth which should happen only once and at the beginning. But the negative point brought to light by the regrowth experiment is that increasing 3C thickness also leads to surface roughening by enhanced step bunching. This may be the consequence of the growth on low off-angle which is known to favor step bunching [IV.25].

The last point to be discussed is the effect of substrate polytype on 3C nucleation and DPB formation. We demonstrated the ability to grow homoepitaxial 6H-SiC on rather low off-axis (1°) without real optimization of the growth conditions except the use of GeH_4 based surface preparation. This means that 3C nucleation is less favored on 6H compared to 4H substrate. As mentioned earlier 6H substrates lead easily to parallel step terrace structure which means that such structure is stable. One needs to destabilize this step front and form facets in order to smoothly pass from homoepitaxy to 3C nucleation and lateral expansion, and thus to possibly eliminate the DPBs. This requires more Ge amount on the surface than for the case of 4H seeds, as seen in Figure IV.17. But under these conditions, one can remain on homoepitaxy conditions with only scarce 3C nucleation. Experimentally, 6H-SiC seeds were found much less reproducible than 4H ones for DPB elimination. This is most probably due to narrower window of surface preparation under GeH_4 for achieving the optimal homo to heteroepitaxial transition as discussed previously.

IV.4.3 Toward non-Ge induced twin boundary elimination

According to the proposed mechanism, liquid Ge has the crucial role of promoting some transient 4H-SiC homoepitaxial growth. Let us take now the hypothesis that Ge itself has no effect except to be present on liquid state at the surface. Then any other "non-reacting" liquid phase could lead to similar result. For instance, let us replace liquid Ge by liquid Si for the surface pretreatment, with a SiH_4 flux comparable to that of GeH_4. After SiC growth using this procedure, the 3C-SiC layer is almost single domain with very small isolated twins (Figure IV.23) that could be probably overgrown using a 1600 °C regrowth step.

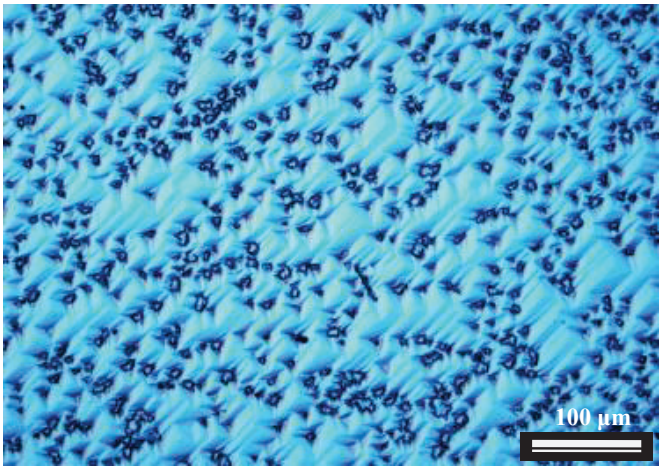


Figure IV.23: Surface morphology as observed by optical microscopy for a 3C-SiC layer grown at 1500 °C for 1 h with 0.06 sccm SiH_4 surface preparation.

Of course, this is a first trial-result which needs further work and optimization (by tuning SiH_4 flux for instance) to demonstrate the potential of such approach. But, it gives essential information on the mechanism viewpoint: this is not Ge element which seems to be important but rather the presence of a liquid on the surface prior growth. This promotes early 4H homoepitaxial growth which smoothly switches to 3C heteroepitaxy.

Note that this could be also the explanation of the DPB elimination observed by Li et al [IV.15] who are suggesting that their 3C growth is probably starting under very rich Si conditions. To be complete on this comparison, it is important to mention that these authors are mentioning a growth temperature below Si melting point (1350 °C). Though, when looking to the rounded shape of the Si islands they obtained under Si rich conditions, one can think that the given temperature could have been wrong and probably higher (above Si melting point, i.e. 1414 °C). In addition, using Si rich conditions below Si melting point should lead to solid Si deposition together with SiC and thus considerably degrade the SiC deposit. This is indeed what they observed but at 1325 °C which suggests that their temperature error may have been in the 70° range.

IV.5 Electrical characterization

A preliminary electrical characterization was carried out to get insight on the quality of the obtained twin free 3C layer and monitor the presence of electrically active defects on the surface.

IV.5.1 Sample preparation

In order to study the electrical behavior of the 3C-SiC samples, firstly a RCA cleaning composed of wet etching is performed. Then an Ohmic back-contact based on nickel silicide was fabricated by Ni-deposition followed by a rapid thermal annealing (RTA) treatment at 950°C. Then, circular Schottky contacts of different radii were defined by Au-sputtering, optical lithography and wet etching. An illustration of the device fabrication along with the used mask is depicted in Figure IV.24.

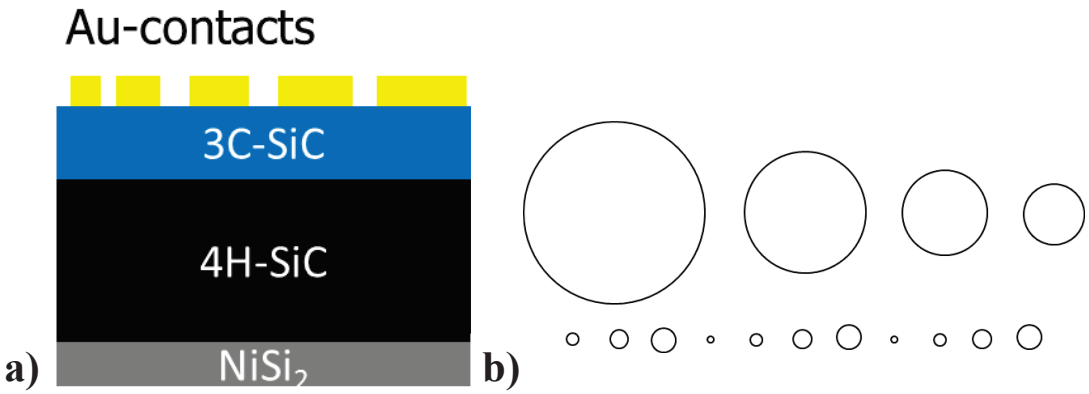


Figure IV. 24: a) Cross sectional illustration of backside Ohmic contact and Au contacts fabricated on the 3C-SiC epilayer grown on 4H-SiC substrate, b) the used mask to demonstrate the Au contacts on the front side.

The Au contact radii are: 150, 100, 75, 50, 25, 20, 15, 10 and 5 µm. Figure y shows optical image of sample in Figure IV.5a with the fabricated gold contacts.

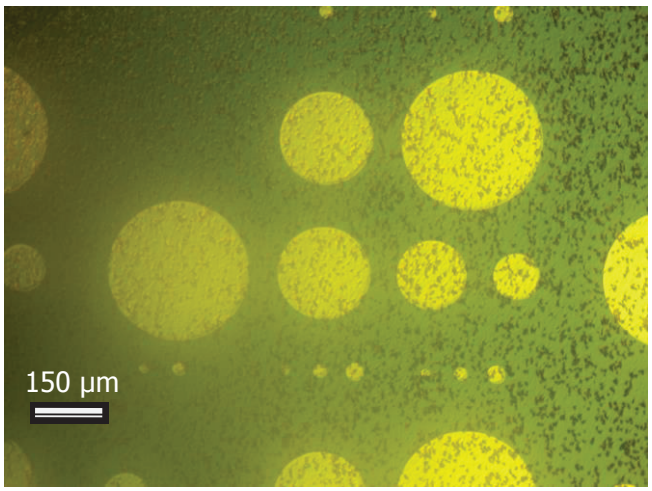


Figure IV.25: Optical image of sample in Figure IV.5a after the fabrication of Schottky contacts on the front side

The biased conductive tip of the AFM has been used in order to acquire the current-voltage (I-V) characteristics of these small Au-contacts, as reported elsewhere in more detail ref [IV.26].

IV.5.2 Results and discussion

The measurements were conducted on the "as-grown" layer shown of Figure IV.5a and after CVD "regrowth" as presented in Figure IV.14. The electrical behavior of the epilayer surface was investigated at nano-metric scale by means of C-AFM and correlated with the surface morphology. The AFM surface morphology images are reported in Figure IV.26a and b, while the corresponding C-AFM current maps are reported in Figure IV.26c and d.

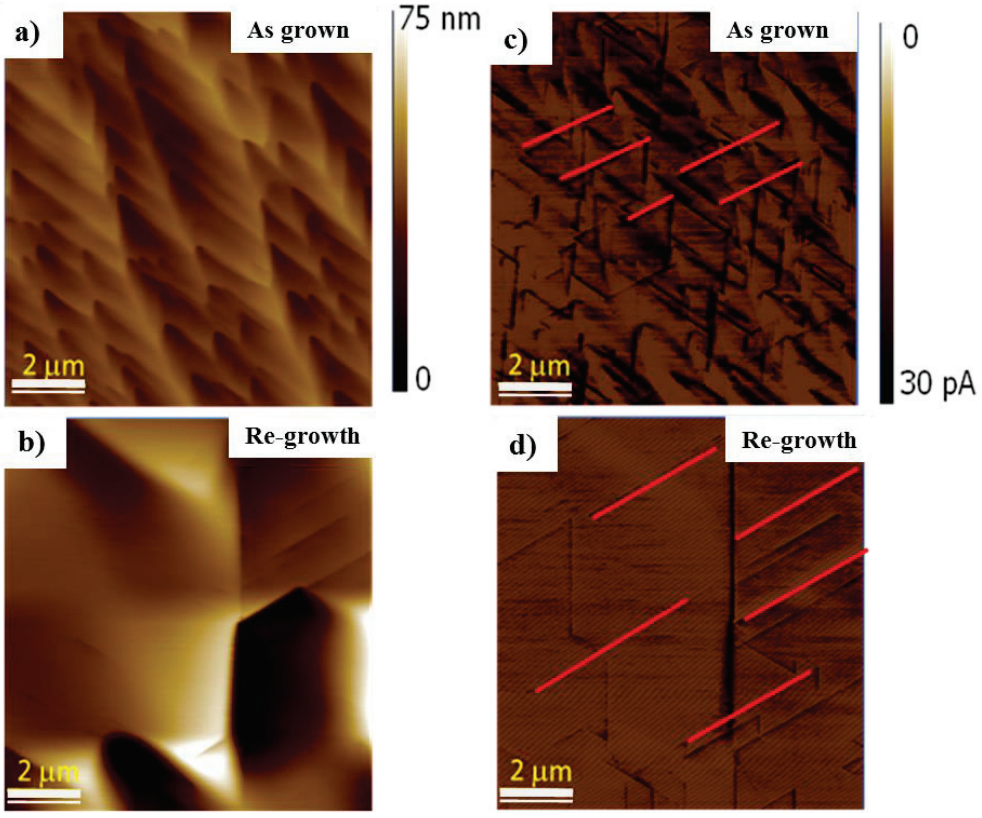


Figure IV. 26: Surface morphologies (a and b) and current maps (c and d) measured by C-AFM on the "as grown" 3C-SiC sample and "re-growth" one. Electrically conductive defects, most probably associated to the presence of SFs, are visible in the current map (highlighted by transversal red lines).

As can be seen, the nanoscale electrical behaviour of the two samples was rather similar. In particular, in the two dimensional current maps of the "as-grown" (Figure IV.26c) and the "re-growth" (Figure IV.26d), two types of electrically active

features are observed. Firstly, some conductive structures resembling to the surface steps and observed in the morphological analysis are clearly visible also in the C-AFM, especially for the "as grown" sample. This observation can be attributed to an enhanced conduction in the sidewalls of the surface steps, due to the increased contact area of the probe tip encountering such morphological features. In addition, most interesting is the presence of some isolated electrically active defects lines, forming an angle of ~55° with respect to the morphological surface steps, which are visible in the two samples. Some of these defects were marked by red lines in Figure IV. 26c and d. These electrically active defects can be ascribed to electrical signatures of stacking faults (SFs) like in reference [IV.26]. From the two dimensional current maps, it was possible to estimate a density of the electrically active defects in the order of the mid 10^2 cm^{-1} range, in both cases. So the thickening of the 3C-layers does not seem to significantly improve the crystalline quality in terms of SF density.

On the other hand, after exposure of the surface of the as-grown layer (shown in Figure IV. 26a and b) to UV treatment, these conductive lines are not visible any more in the current map (see Figure IV.27b). This latter confirms that this surface preparation electrically passivate SFs, limiting their potential detrimental effect on the metal/3C-SiC interface behavior [IV.27].

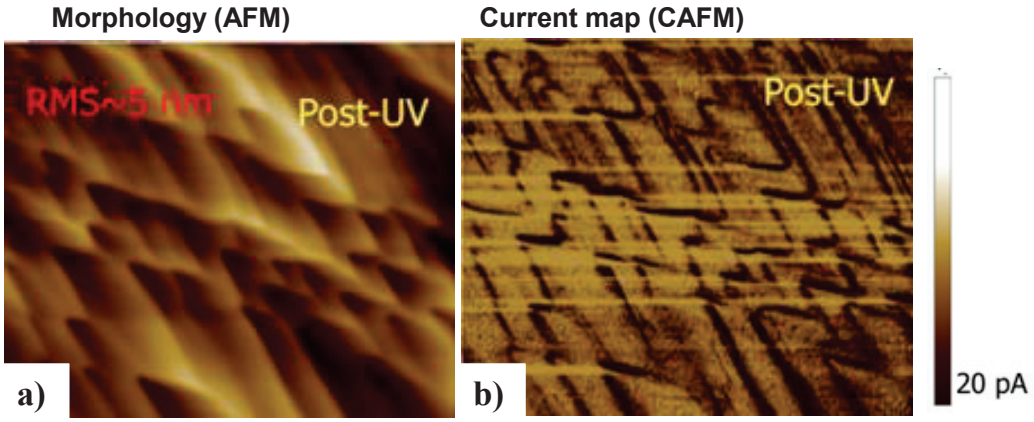


Figure IV.27: a) Surface morphology and (b) and current map as in Figure IV. 26 but after UV treatment, showing the passivation of stacking faults.

It is worth mentioning that the overall SF density measured by structural investigations techniques, such as by X-ray diffraction reciprocal space mapping for 3C-SiC grown on 4H-SiC [IV.28] or by TEM [IV.29] for 3C-SiC grown on Si, can be typically higher than the electrically active fraction observed by C-AFM.

To be more complete on this aspect, the question of such high density of SFs in the layers grown on 4H-SiC substrate has to be tackled. Indeed the lattice mismatch being small, it is most probably not at the origin of these defects. It may come from the "selection rule" model, as discussed earlier in section IV.4.1, which foresees the generation of SFs above steps of 1 unit cell height. Also, the 3C nucleation itself may generate these defects so as the coalescence of the nuclei can do also. Finally, the use of low off-axis seeds for favoring 3C nucleation means also that the step-flow growth is difficult to achieve when a complete layer is formed. 2D nucleation on terraces may be frequently encountered and thus lead to the generation of defects within the layers. For instance, such 2D nucleation may be at the origin of the fourfold twin complex already reported earlier [IV.30]. Such defect was also seen by TEM in our layers, as shown in Figure IV.28.

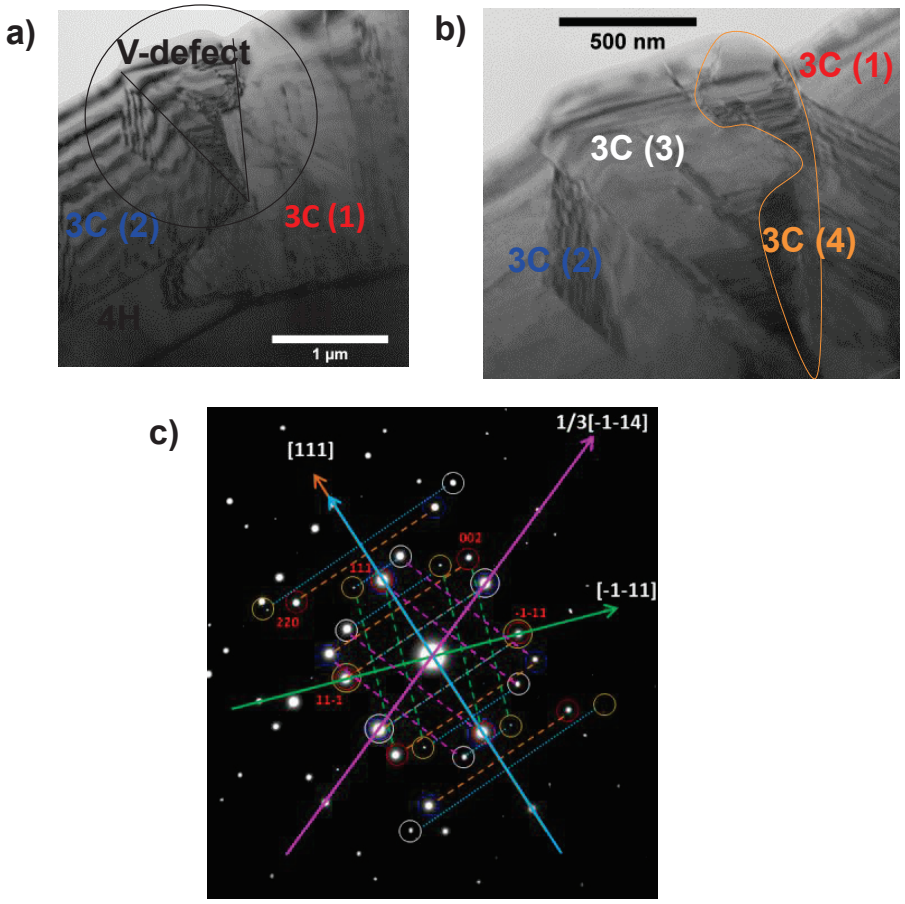


Figure IV.28: a) Bright-field and (b) Observations of the different layer orientations, b) is an on-axis magnification of the encircled area in (a). c) DP of the encircled area in (a): 4-fold twin around (-1-11), (111) (x2) and (-1-14) planes

Two I-V characteristics measured on circular Schottky diodes with 20 µm and 5 µm radii, representative of the behavior observed on several devices fabricated on the sample surface of the as-grown layer, are reported in Figure IV.29.

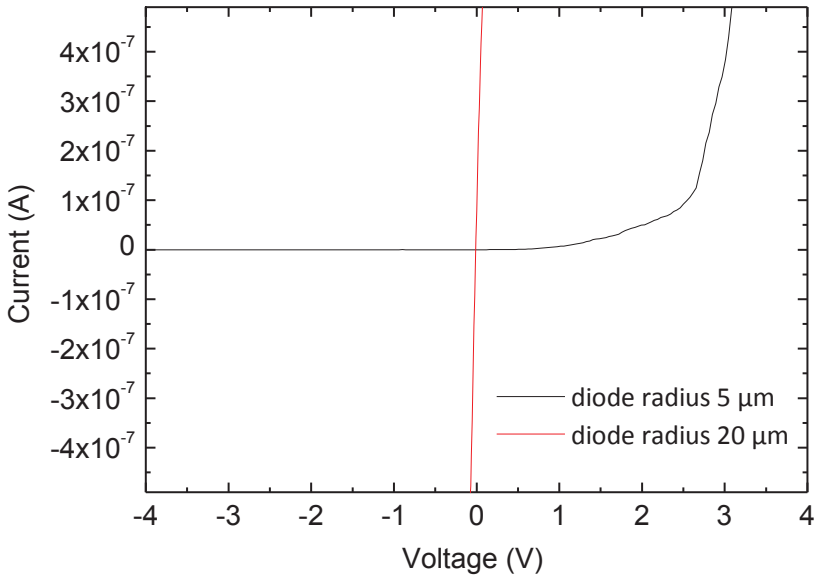


Figure IV.29: Current-voltage characteristics measured using C-AFM on circular Au contacts on 3C-SiC with 5 µm and 20 µm radius.

As can be seen, a Schottky-like behavior is observed only for the smallest device. On the other hand, the diodes with radius ≥20 µm exhibited linear I-V characteristics. This result assesses that the defect density of the material has still a significant impact on the metal/3C-SiC Schottky contact. The electrical investigation of the Au-contacts on both epilayers was carried out by C-AFM on the small devices, i.e. those showing a rectifying behavior.

Figure IV.30 reports the J-V characteristics for the as-grown and re-grown samples. Both contacts behave as Schottky diodes with low barrier height. Quantitatively, comparable values of the barrier height were found in the as-grown sample (0.76 eV) and in the re-grown case (0.73 eV). The derived Schottky barrier heights are lower than the ideal value of ~1.3 eV, predicted by the Schottky-Mott theory and given from the difference between the metal work function and the semiconductor electron affinity. The deviation of the Schottky barrier height from the ideal behavior can be ascribed to the presence of electrically active defects in the 3C material, which provide preferential current paths through the epilayer, as already reported in reference [IV.26].

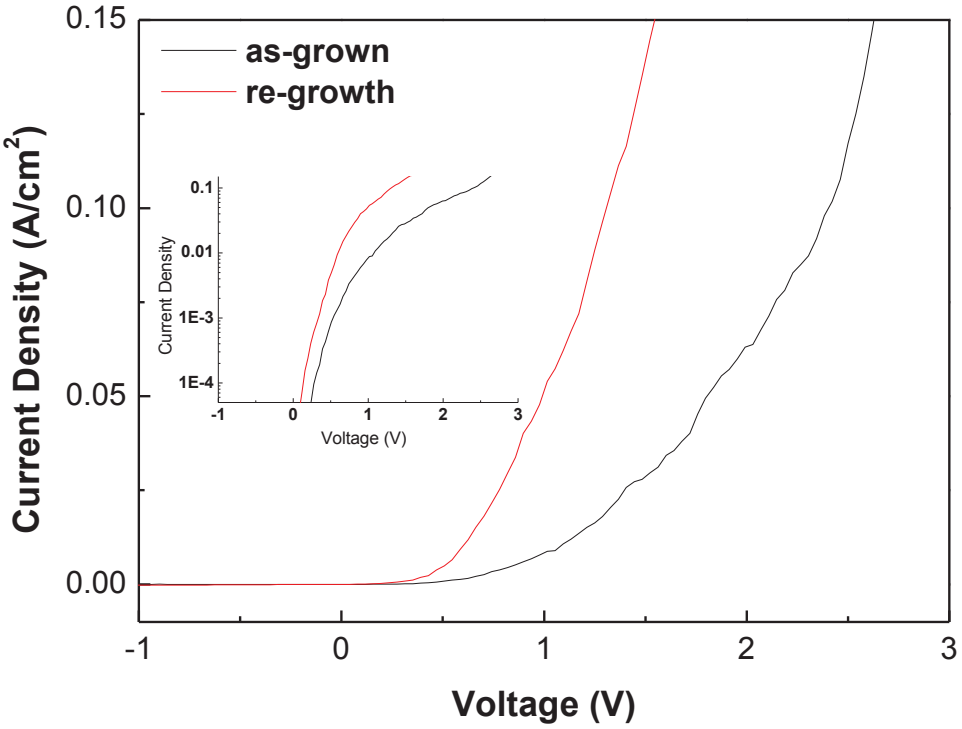


Figure IV.30: Semi-log plot of the forward J-V characteristics, acquired by C-AFM, related to the as-grown and re-grown layers. The inset reports the reverse curves for the two samples.

The two diodes exhibit high ideality factor values (3.3 and 1.8 for the as-grown and regrown layers, respectively), consistently with a non-perfect Schottky behavior and a strong recombination of the direct current. Regarding the reverse behavior with the characteristics reported in the inset of Figure IV.30, the two samples show leakage currents of the same order of magnitude (1×10^{-7} A/cm^2), with a slight lower value in the case of the as-grown layer, in agreement with the higher value of Schottky barrier height.

IV.6 Conclusion

In this Chapter, we have presented and discussed our understanding of the growth mechanism leading to twin boundary elimination during 3C-SiC heteroepitaxy on α-SiC substrate by CVD. It involves surface pre-treatment under GeH_4 or SiH_4 of low off-axis α-SiC seeds under optimal conditions. The growth conditions following the surface preparation step also affect less the twins elimination. The proposed mechanism involved a smooth transition between 4H homo and 3C heteroepitaxy thanks to the presence of Ge on the surface which transiently promotes 4H

homoepitaxy. Electrical characterizations revealed that the layer quality has an important impact on the metal/3C-SiC schottky contact.

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General Conclusion and perspectives

When starting this thesis work, none of the results obtained here could have be anticipated despite few articles suggesting some electronic improvement of the Ge implanted 4H-SiC material. This element has never been implemented before in a CVD machine dedicated to high purity SiC epitaxy. It was thus a bit risky in terms of possible positive results but the frame of NetFISiC project could allow and support such fundamental investigation.

The first experimental part of this work was devoted to exploring the effect of GeH_4 addition to the well-known H-Si-C chemical system used for 4H-SiC homoepitaxial growth. The main goal was to estimate the influence of this impurity on surface morphology and layer properties, while understanding its incorporation behavior inside SiC matrix.

We have found that GeH_4 addition during growth leads to droplets accumulation on the surface without significant effect on the homoepitaxial 4H-SiC layer quality. The density of epi-induced defects was similar in both Ge containing and reference samples. LTPL characterization confirmed the absence of any degradation of the layers quality. In fact, the sole negative effect detected so far related to GeH_4 addition is on the modification of the step and terrace structure and/or on the formation of droplet fingerprints (which is avoidable). The accumulated droplets on the surface were characterized as pure Ge by both μ-Raman spectroscopy and high resolution TEM. This accumulation is temperature and time dependent. Using SIMS analyses, Ge incorporation was found to be homogeneous all along the 4H-SiC layer thickness. Its level of incorporation, which ranges from few 10^{16} to few 10^{18} at.cm^{-3}, was mainly dependent on GeH_4 flux, growth rate and temperature. This suggests that Ge is mainly incorporated from vapor phase and increasing of the desorption rate with temperature reduces the incorporation level. The activation energy for this incorporation was found to be -137 kcal/mol.

On the other hand, C/Si ratio and crystallographic parameters (polytype, polarity and off-orientation) did not display any significant influence. This may be linked to

our particular Ge incorporation conditions from a Ge-saturated vapor phase and surface. Note that the memory effect of Ge from run to run was found to be negligible. Finally, ALCHEMI technique allowed us identifying that Ge is incorporating on Si site inside SiC matrix and not on C or interstitial sites.

Apart from growth related aspects, interesting results came also from the electrical characterization of the Ge-doped layers. Despite being isoelectronic to SiC, Ge incorporation surprisingly causes an increase in the n-type doping level by a factor from 2 to 5 depending on the C/Si ratio. The exact mechanism leading to this result is still unclear and needs further work for full understanding. Even more surprising is the increase of conductivity and Hall mobility of these Ge doped layers, despite the higher n type doping level. From DLTS measurement, no Ge related point defect was detected while a negative peak attributed to charge extended defects was found. According to the Schottky contact study, Ge doping did not improve or deteriorate the Schottky characteristics of Ni-based metallisation. The physical reasons behind all these results are not yet clarified and more experiments together with theoretical approach have to be done.

The second experimental part of this thesis focused on Ge mediated heteropolytypic growth of 3C-SiC on low off-axis α-SiC substrates. It was shown that optimal pre-treatment under GeH_4 of these low off-axis α-SiC seeds can lead to the complete elimination of the twin boundaries. This is usually very difficult to achieve reproducibly. These optimal pre-treatment conditions are temperature, C/Si ratio, growth rate and GeH_4 flux dependent. The proposed mechanism involves a smooth transition from 4H homoepitaxy to 3C heteroepitaxy mediated by the presence of Ge on the surface which is suggested to transiently promote 4H homoepitaxy. We have shown that this mechanism is not exclusive for Ge since another liquid phase like Si excess can also lead to some extent to twin boundaries elimination. When comparing the use of 4H-SiC and 6H-SiC seeds, the latter were found less reproducible than the former because less subjected to step faceting. Electrical characterization of the twin free layers confirms the rather good quality of the grown layers even if the density of SFs is still high. Though further optimization of the growth process (both for the nucleation and the regrowth steps) is still required for getting a step forward on this direction, the results of this chapter could pave the way of a future development of large area and twin-free 3C-SiC epilayers.

This thesis being the first one exploring the addition of Ge element in the epitaxial H-Si-C system, it has obviously opened more questions than it has answered. As a matter of fact, there is still a lot of science to be done (both experimentally and theoretically) for complete understanding of the results generated. And due to the positive effect of Ge incorporation on conductivity and hall mobility, the motivation is no more only fundamental but with clear applied targets for improving 4H-SiC electronic devices.

It is worth mentioning here some preliminary works performed by NetFISiC partners on our Ge doped samples and which were not discussed in the manuscript. Indeed, it was shown by INFINEON partner that Ge doped 4H-SiC layers can lead to reduced density of interface states after dry oxidation. Moreover, Oxidation rate is enhanced and oxide reliability is not negatively influenced. These results are additional tracks to follow for this Ge doping which is obviously suitable for MOSFET applications.

Ge accumulation at the surface is usually seen as a drawback of Ge doping because requiring chemical etching before further processing of the layers. But CNR-IMM partner is trying to turn this drawback into an advantage by studying the effect of micrometric Ge-droplets on the characteristic of Ni/4H-SiC Schottky contacts. Preliminary results showed a higher current conduction on the Ge-droplet with respect to the surrounding 4H-SiC surface, thus suggesting a barrier lowering. By optimizing the Ge droplet size and density, one can try to tailor the Schottky characteristics of the Ni contacts and, depending on the results, innovating ideas could be proposed for using such layers and materials into real devices or new concepts.

On the growth aspects, the next step would be to investigate the interaction of Ge with the usual dopants (N and Al). The observed increase of n type doping with Ge incorporation is still not understood and requires deeper research, while for the p type doping, all remains to be done. Obviously, it is of clear device interest to check if, like for the n type doping, one can increase conductivity and Hall mobility in the case of p type doping just by adding GeH_4 to the gas phase. Beside this, it would be interesting to study the lower Ge doping range, i.e. $< 10^{16}$ at.cm^{-3}, and to check if the electronic improvements are kept.

Finally, for the 3C-SiC heteropolytypic growth, improvement of the layer quality may not come only from finely tuning of the Ge pre-treatment step but also from the replacement of Ge by Si during this pre-treatment. Obviously, one cannot just transpose the conditions (fluxes, time, and temperature) from Ge to Si and experimental optimization is required. The regrowth (or thickening) step has also to be optimized in order to avoid surface roughening. Finally, attempts on large area wafers needs to be done to check growth homogeneity and yield of twin boundary elimination.

Résumé étendu

Le carbure de silicium (SiC) est une céramique semi-conductrice qui possède des propriétés électroniques et physiques bien supérieures à celles du silicium. C'est un matériau de choix pour des applications en électronique de puissance, fonctionnant notamment à haute tension et haute température. Les avancées technologiques sur le polytype 4H-SiC se sont accélérées ces dernières années pour atteindre un certain stade de maturité permettant d'utiliser des composants en SiC dans des dispositifs industriels. Mais la "technologie SiC" est maintenant victime de son succès et les utilisateurs demandent des performances toujours plus élevées, au-delà des limites actuellement atteintes. Parmi les facteurs limitant, on citera la faible mobilité électronique des composants, la durée de vie des porteurs ou encore la densité de pièges à l'interface SiO_2/SiC. Des étapes technologiques post-croissance épitaxiales sont actuellement utilisées pour essayer d'améliorer ces propriétés mais il serait clairement préférable d'employer un procédé in-situ pendant l'épitaxie pour des raisons évidentes de durée de fabrication et donc de coût.

L'incorporation intentionnelle d'impuretés dans le 4H-SiC est une voie possible pour modifier les propriétés du matériau. Mais, à moins que cette impureté ne soit déjà connue à partir de travaux expérimentaux précédents, chaque élément nécessite une étude fondamentale à lui seul. Ceci est généralement réalisé par implantation ionique car facile à mettre en œuvre et permettant de faire un tri rapide de différentes impuretés. Mais cette technique génère toujours des défauts cristallins dans le matériau, défauts très difficiles à guérir dans le cas du SiC. De plus, l'incorporation d'impureté par implantation ionique est limitée à quelques centaines de nm seulement, ce qui peut ne pas être suffisant. L'incorporation d'impureté pendant l'épitaxie serait une voie préférable mais elle nécessite une étude expérimentale plus longue et plus lourde. Ainsi, l'impureté visée doit être soigneusement choisie.

Dans ce travail de thèse, financé par le réseau Européen (RTN) intitulé NetFISiC (Network on Functionnal Interface for Silicon Carbide), nous avons sélectionné l'élément germanium (Ge) qui est une impureté isoélectronique à SiC pour étudier son incorporation pendant l'homoépitaxie du 4H-SiC. Des travaux précédents, utilisant l'implantation ionique de Ge, suggèrent une amélioration des propriétés électroniques

du 4H-SiC après recuit post-implantation. Mais, nous n'avons pas trouvé de travaux expérimentaux relatifs à l'incorporation de cette impureté durant l'épitaxie du 4H-SiC. C'est l'objectif principal de cette thèse qui vise à étudier les différents aspects fondamentaux liés à ce système : des mécanismes de croissance à l'incorporation de l'impureté Ge, en passant par la détermination des propriétés du matériau ainsi épitaxié.

La croissance épitaxiale par dépôt chimique en phase vapeur a été réalisée dans un réacteur vertical à mur froid travaillant à pression atmosphérique. Les dépôts ont été réalisés dans la gamme de température 1450-1600°C sur des substrats 4H-SiC(0001) désorientés fortement (4° et 8°) ou faiblement (0° et 1°). Le précurseur gazeux GeH_4 a été ajouté au système de précurseurs classique SiH_4+C_3H_8 dilué dans H_2.

Dans le cas de l'homoépitaxie de 4H-SiC sur substrats désorientés, excepté l'accumulation de gouttelettes de Ge en surface, l'ajout de cet élément lors de la croissance ne semble pas avoir d'effet négatif notable en termes de morphologie de surface et de qualité cristalline. Les analyses SIMS ont montré que le Ge s'incorporait de manière homogène tout au long de la croissance. Cette incorporation peut être contrôlée dans la gamme $1x10^{16}$ - $7x10^{18}$ $at.cm^{-3}$ en fonction des paramètres de croissance (flux de GeH_4, température et vitesse de croissance). Les résultats suggèrent que cette incorporation de Ge s'effectue à partir de la phase gazeuse et est indépendante de l'excès de Ge liquide en surface. L'énergie d'activation du phénomène a été déterminée à -137 kcal/mol. L'effet mémoire du Ge (incorporation résiduelle sans ajout de GeH_4) est négligeable.

Plus surprenant est l'absence de dépendance de l'incorporation de Ge dans SiC en fonction des paramètres cristallographiques (polytype du SiC, polarité, désorientation) et du rapport C/Si dans la phase gazeuse. Nous expliquons ces résultats en considérant les conditions particulières existantes en surface de croissance et plus particulièrement la forte saturation en espèces contenant du Ge. La technique ALCHEMI nous a permis de déterminer que les atomes de Ge s'incorporent exclusivement en site Si dans la matrice SiC (et non pas en site C ou en interstitiel), probablement pour des raisons de rayon atomique.

En parallèle des aspects relatifs à la croissance, des résultats singuliers ont été obtenus en réalisant des caractérisations électriques sur ces couches contenant du Ge.

Bien que cette impureté soit isoélectronique, son incorporation entraine une augmentation significative du dopage de type n d'un facteur allant de 2 à 5 en fonction du rapport C/Si en phase gazeuse. Les mécanismes à l'origine de cet effet restent encore à identifier. Encore plus surprenants sont les valeurs de conductivité électrique et de mobilité du 4H-SiC qui s'améliorent sensiblement avec l'ajout de Ge. Des caractérisations de contact Schottky à base de Ni n'ont montré aucune dégradation significative de ce type de contact électrique sur les couches contenant du Ge. Une étude expérimentale plus poussée en liaison avec une approche théorique serait nécessaire afin d'identifier les raisons physiques de ces améliorations.

En utilisant des germes faiblement désorientés, le polytype cubique 3C-SiC se forme spontanément mais contient habituellement une forte densité de macles. Nous avons montré que l'ajout d'une étape de préparation de surface sous flux de GeH_4 avant la croissance de 3C-SiC permet de réduire cette densité de macles jusqu'à leur complète élimination dans les conditions optimales (dépendant du flux de GeH_4, de la température, de la vitesse de croissance et du rapport C/Si). Ceci est habituellement très difficile à réaliser de manière reproductible. En se basant sur les résultats expérimentaux, nous avons proposé un modèle de croissance impliquant une transition progressive d'homoépitaxie du 4H-SiC à hétéroépitaxie de 3C-SiC, modulée par la présence de Ge en surface qui promeut une homoepitaxie transitoire. La formation de larges terrasses par le facettage des marches homoepitaxiales provoque la nucléation du 3C-SiC. L'interaction avec les bords de marche entraine la sélection d'une seule des deux possibles orientations. Nous avons montré que ce mécanisme n'est pas l'apanage du seul Ge mais peut fonctionner aussi avec une autre phase liquide, comme par exemple le Si. Enfin, la comparaison entre l'utilisation de substrats 4H et 6H-SiC a montré que la reproductibilité était supérieure sur les germes 4H probablement en raison d'une tendance au facettage des marches plus grande que sur germes 6H.

Les caractérisations par microscopie à force atomique en mode conduction de ces couches de 3C-SiC sans macle ont montré la présence d'une densité importante de fautes d'empilement. Cela montre qu'il reste encore tout un travail d'optimisation de la croissance (de la nucléation à l'épaississement) pour améliorer la qualité du 3C-SiC déposé et se rapprocher d'une qualité cristalline compatible avec les exigences de composants électroniques.

En conclusion, ce travail de thèse étant le premier explorant l'ajout de l'élément Ge dans le système épitaxial H-Si-C, il a nécessairement ouvert plus de questions qu'il n'en a répondues. De ce fait, il reste encore beaucoup de travaux scientifiques à réaliser (que ce soit théorique ou expérimental) pour la compréhension fine des résultats générés. Et en raison de l'effet positif de l'incorporation du Ge sur les propriétés électroniques du 4H-SiC, les motivations ne sont plus seulement d'ordre fondamental mais elles penchent logiquement vers les applications industrielles afin d'améliorer les performances des composants électroniques à base de 4H-SiC.

Behavior and chemical reactions of liquid Si and Ge on SiC surface

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Keywords. CVD, liquid Germanium, chemical reaction, Silicon.

Abstract. The interaction of liquid Ge and Si droplets, deposited by CVD, on the surface of 4H-SiC single-crystals is studied. It was found that at 1500 °C Ge forms micrometric droplets while Si forms nanometric dots. While the Si dots do not seem to interact significantly with SiC, the Ge droplets have the tendency to dissolve the Si from the seed. This mechanism not only happens during deposition but also during the cooling. If the cooling rate is too slow, Ge evaporates from the droplets while dissolving Si so that, at the end, the droplets look like to have been fully converted from Ge to Si.

Introduction

In the last years the formation of liquid phase on top of 4H-SiC during epitaxial growth has been very little studied, though Si droplets are often observed when Si rich conditions are used during chemical vapour deposition (CVD) [1]. Recently, while studying Ge incorporation into SiC during CVD, accumulation of Ge droplets at the surface was observed [2]. These droplets were even used for studying their impact on the electrical properties of Ni/4H-SiC Schottky contacts [3]. Also, it was shown that Ge droplets deposited prior to the growth on low off-axis α-SiC substrates can lead to 3C-SiC layers free from twin boundary [4]. However, some basic knowledge on Ge droplets behavior and reactivity with SiC are still missing.

The present study is a complementary investigation related to the addition of Ge element in SiC CVD system. Comparison between pure liquid Ge and Si droplets will be performed. Evolution of the Ge droplets will be followed as a function of cooling rate.

Experimental section

The experiments were carried out in home-made epitaxy equipment working at atmospheric pressure (see [5] for more details). High purity hydrogen (16 slm) is used as vector gas. Si and Ge droplets were deposited at 1500°C on top of Si face 4H-SiC 8° off axis commercial wafers using high purity GeH_4 and SiH_4 precursors. Constant flux of 0.06 sccm during 5 minutes has been used for the deposition. The cooling step under H_2 was studied using : 1) the natural cooling (which corresponds roughly to a cooling rate of ~10 °C/sec in the 1500 °C to 850 °C range) or 2) a two-step cooling involving a natural cooling from 1500 to 1100°C (to limit elemental evaporation) followed by a controlled one of 0.5 °C/sec from 1100 to 850 °C. For comparison purpose, a typical sample with GeH_4 addition during 4H-SiC homoepitaxial growth (1500°C, ~2 µm/h, 0.1 sccm GeH_4) and displaying Ge accumulation at the surface is also discussed.

The layers were routinely characterized by Normarski optical microscopy and µ-Raman spectrometry. Additional observations were made using scanning electron microscopy and Atomic force microscopy (AFM).

Results

For Ge and Si depositions followed by natural cooling, spherical shape droplets were observed for both elements. In the case of Ge, they were easily seen by optical microscopy and an average diameter of 2.75 µm was measured (Figure 1a). However, in case of Si, the droplets were in higher density but significantly smaller (< 1 µm) and only seen by AFM (Figure 1b). This difference is probably connected to the smaller wetting angle of liquid Si compared to liquid Ge on SiC surfaces [6]. High wetting angle leads to bigger droplets in order to counterbalance surface tension.

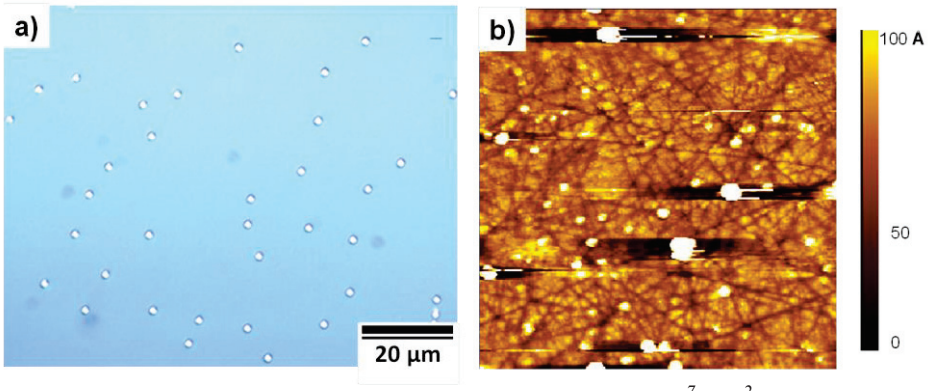

***Figure 1**: a) Nomarski optical image after Ge deposition ($0.8x10^{-7}$ cm^{-2}) and b) AFM scan (10 x 10 µm) after Si deposition (scratch lines are due to substrate polishing and elongated black areas besides the biggest dots are measurement artefacts) ($1.6x10^{-7}$ cm^{-2})*

Using µ-Raman spectroscopy analyses, no Si signal was detected on SiH_4 treated sample while a clear Ge related peak was seen at 298 cm^{-1} on GeH_4 treated sample (Figure 2). This is probably due to the fact that the Si dots were too small to focus one while Ge droplets are big enough for ensuring a direct focus on a single droplet. Surprisingly, the Ge droplet seems also to contain some amount of Si (peak at 384 cm^{-1}). From the positions of Ge-Ge and Si-Ge vibrational peaks, one can deduce that the Si content in the droplet can be up to 10 % [7]. So these droplets are not pure Ge but their composition is close to $Si_{0.1}Ge_{0.9}$. Since no SiH_4 was added during this experiment, the Si contains in the droplets is probably coming from slight dissolution of the substrate, during either the deposition or the cooling.

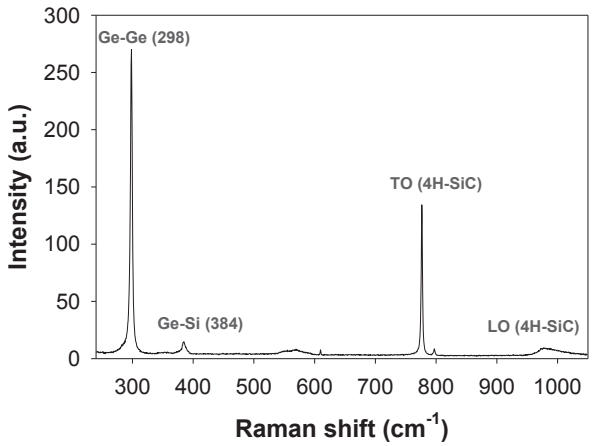

***Figure 2:** Typical µ-Raman spectrum collected on a droplet shown in Figure 1a.*

A two-step cooling was performed after Ge deposition in order to see better what is happening during the cooling. In the center of this sample (Figure 3a and 3b), no droplets are seen but there are instead step bunching-like circular features of roughly the same size as the original droplets of Figure 1a, very similarly to what was seen when liquid Si is in contact with a 8°off SiC seed [8]. At the edges of the sample, droplets are still seen but smaller than initially. Using µ-Raman spectroscopy, only Si related signal was detected on these droplets (figure 3c) so that can say they are now only composed of Si. After wet etching of these Si droplets, the same step-bunched circular prints as in the center of the sample are seen (not shown).

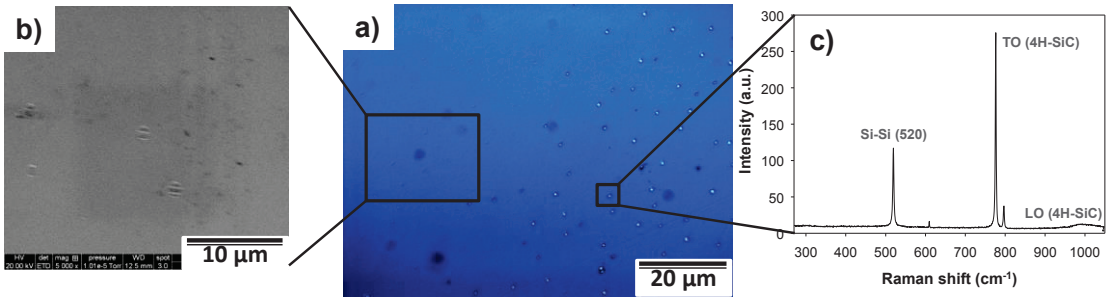

Figure 3: *Characterization of a sample after Ge droplets deposition and slow cooling : a) optical microscopy image showing on the left and on the right parts respectively the center and the edge of the sample; b) zoom using SEM of the sample center and c) µ-Raman spectrum collected on a single droplet remaining on the sample edge.*

As a matter of fact, liquid Ge droplets tend to convert into Si when in prolonged contact with SiC. Here is the proposed mechanism explaining such feature, which is illustrated in figure 4. Initially, pure Ge droplets are formed but pure liquid Ge is not in thermodynamic equilibrium with SiC while Ge-Si alloys are, as already discussed in details in [7]. So, the droplets start dissolving the silicon of the substrate. Since such alloys have a very low C solubility and since we did not detect any graphite like phase forming (for instance by µ-Raman spectroscopy), excess of C is probably etched away by H_2 under the form of volatile CH_x species. In the meantime, when GeH_4 flux is stopped, Ge starts to evaporate from the droplets due to its higher vapor pressure than Si. As long as the droplets remain in liquid state, such mechanism should continue occurring. Such dissolution of the substrate, even in small amount, should lead to step-bunched like structuration of the surface at the liquid-solid interface as is seen in figure 3b. If the cooling is too long, then enough time is given to Ge atoms to evaporate all, leaving on the surface just Si droplets (liquid or solid depending on the temperature).

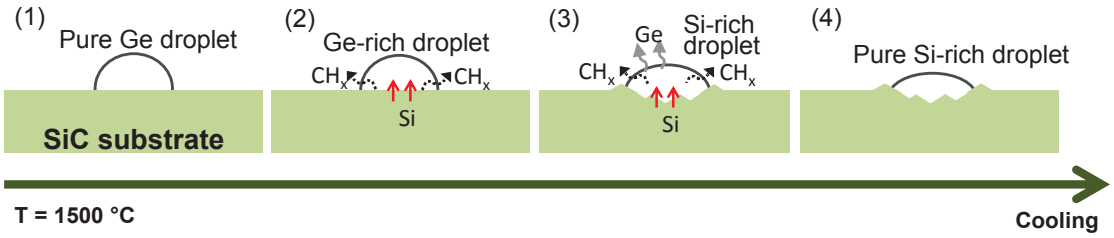

Figure 4: *Proposed mechanism explaining the conversion of Ge droplets into Si ones during deposition and cooling.*

In order to complete this discussion, it is worth comparing with the case of Ge

accumulation at the surface during 4H-SiC homoepitaxial growth, and natural cooling (Figure 5a). µ-Raman analysis on a single droplet shows that it is composed of pure Ge, with no detectable Si content (figure 5b). It means that, despite the fact that SiH_4 was present during the experiment, Si was not dissolved into the droplets. One can propose that the driving force for growing SiC is higher than for dissolving Si into liquid Ge. As a result, even if some Si atoms are dissolved in Ge droplets from the gas phase, at the end they are consumed and participate to the SiC growth. Also, this result indicates that the natural cooling under H_2 does not give sufficient time for the Ge-SiC reaction to occur.

So, an important outcome of this study is that now one can answer to the question: how to proceed to eliminate this excess of Ge at the surface after homoepitaxial growth? Wet chemical etching after growth is obviously an easy solution since Ge does not react with SiC during cooling and thus does not degrade the surface morphology. But this solution adds a process step. In situ elimination of the droplets is also possible, for instance by letting them evaporate using a high temperature annealing just after growth. In this case, as it was shown above, some SiC dissolution can occur and leave some unwanted circular prints. Another possibility would be to remove GeH_4 from the reactor few minutes before the end of SiC growth in order to evaporate the Ge droplets without substrate dissolution.

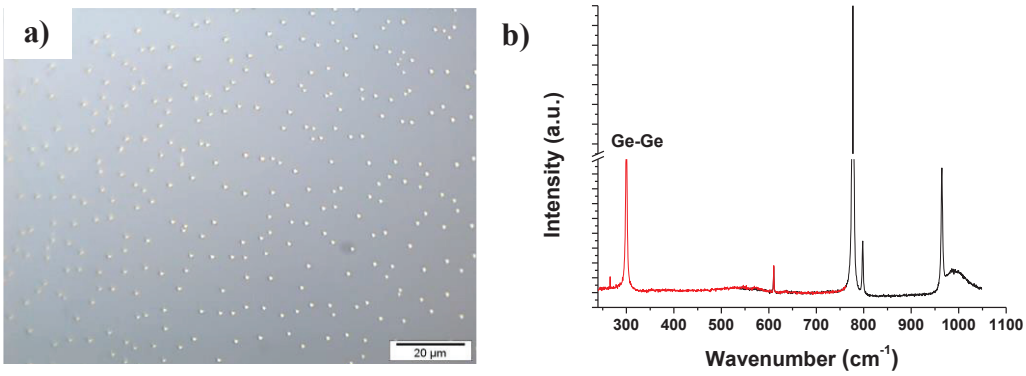

Figure 5: *a) surface morphology of a 4H-SiC homoepitaxial sample with Ge accumulation at the surface during growth; b) µ-Raman spectrum recorded on a single droplet in a)*

Conclusion

In this work, the behavior of Ge and Si deposits on 4H-SiC was studied. Si has the tendency to form small and non-reactive droplets while Ge forms bigger and reactive ones. Si dissolution into the Ge droplets happens both during Ge deposition and cooling causing step bunching like surface beneath the droplet. Such reaction does not occur during SiC epitaxial growth in the presence of Ge droplets.

Acknowledgment

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Exploring SiC growth limitation of vapor-liquid-solid mechanism when using two different carbon precursors

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Abstract. In this paper, conditions for obtaining high growth rate during epitaxial growth of SiC by vapor-liquid-solid mechanism are investigated. The alloys studied were Ge-Si, Al-Si and Al-Ge-Si with various compositions. Temperature was varied between 1100 and 1300°C and the carbon precursor was either propane or methane. The variation of layers thickness was studied at low and high precursor partial pressure. It was found that growth rates obtained with both methane and propane are rather similar at low precursor partial pressures. However, when using Ge based melts, the use of high propane flux leads to the formation of a SiC crust on top of the liquid, which limits the growth by VLS. But when methane is used, even at extremely high flux (up to 100 sccm), no crust could be detected on top of the liquid while the deposit thickness was still rather small (between 1.12 μm and 1.30 μm). When using Al-Si alloys, no crust was also observed under 100 sccm methane but the thickness was as high as 11.5 μm after 30 min growth. It is proposed that the upper limitation of VLS growth rate depends mainly on C solubility of the liquid phase.

Introduction

Growing SiC boules or epitaxial layers form a liquid phase is an old topic which has gained renewed interest recently [1-4]. For bulk growth, top seeded solution technique (TSSG) is preferred while for epilayers Vapor-Liquid-Solid (VLS) mechanism is more suited due to lower growth rate. The fact that the growth is regulated by a gas flux (mostly propane) promotes very stable, flexible and reproducible growth conditions, which are much easier to control than the thermal gradient in the case of TSSG. But VLS mechanism is mostly limited to thin layer growth due to rather low growth rates, in the few μm/h range. Parameters like melt composition, growth temperature and growth configuration were changed in order to increase the growth rates but the main parameter was found to be the propane flux. Unfortunately, attempts to increase the propane flux led to the formation of a SiC crust on top of the liquid, which stops the VLS growth [5]. The only study demonstrating bulk-like growth rates values using VLS concerns the use of methane and Si-Li melts which leads to the formation of 2H polytype [6]. However, it seems that one cannot use this chemical system for growing the more common 4H or 3C polytypes. Though the reasons for achieving high growth rates with Si-Li melts are not known, one cannot exclude methane to be a key parameter since its reactivity is very different compared to propane.

The goal of this study is to compare the use of methane and propane in order to find conditions for achieving high growth rate using VLS mechanism.

Experimental section

The experimental setup is composed of a water-cooled, vertical cold-wall reactor made of quartz. The temperature of the RF-heated graphite susceptor is controlled by an optical pyrometer. The carrier gas was high purity Ar. The carbon precursors were high purity methane and propane, both 5% diluted in H_2. The substrates were pieces of <0001> 1° or 4°off-axis 4H or 6H-SiC wafers. They were glued at the bottom of a graphite crucible and covered by pieces of elements which melting formed the targeted liquid phase. Upon reaching the targeted temperature, the carbon precursor was added in the reactor to start VLS growth. More details about the growth technique and procedure can be found elsewhere [7]. Briefly, the growth conditions used in this study are presented in table 1. Note that the addition of Al in the liquid phase implies to reduce growth temperature in order to limit Al loss by evaporation.

The layers were routinely characterized by Normarski optical microscopy and μ-Raman spectrometry. The deposit thickness was deduced either from interference fringes of Fourier Transform infrared (FTIR) reflectance spectra or by cross-sectional observations using scanning electron microscopy image.

Table 1. Growth conditions used within the study

Name	Carbon partial pressure	Carbon precursor	Melts composition (%)			Temperature (°C)	Time (min)	Layer thickness (μm)
			Si	Ge	Al			
SiGe10	0.0196	CH_4	25	75	-	1300	50	1.20
SiGe11	0.0099	CH_4	25	75	-	1300	30	0.95
SiGe12	0.0020	CH_4	25	75	-	1300	60	0.70
SiGe13	0.0196	CH_4	25	75	-	1300	30	1.20
AlSiGe01	0.0196	CH_4	30	35	35	1100	120	1.12
AlSiGe02	0.0196	CH_4	30	20	50	1100	120	1.30
AlSi01	0.0196	CH_4	30	-	70	1100	30	11.5
SiGe14	0.0020	C_3H_8	25	75	-	1300	60	0.7[5]
AlSi02	0.0042	C_3H_8	30	-	70	1100	30	5.5[3]

Results and discussion

Before detailing the results, it is worth mentioning that all the samples grown using Si-Ge melts gave 3C polytype while Al-based ones led to homoepitaxy. This is illustrated in figure 1. Also, according to our experience, the growth rate is not polytype dependent.

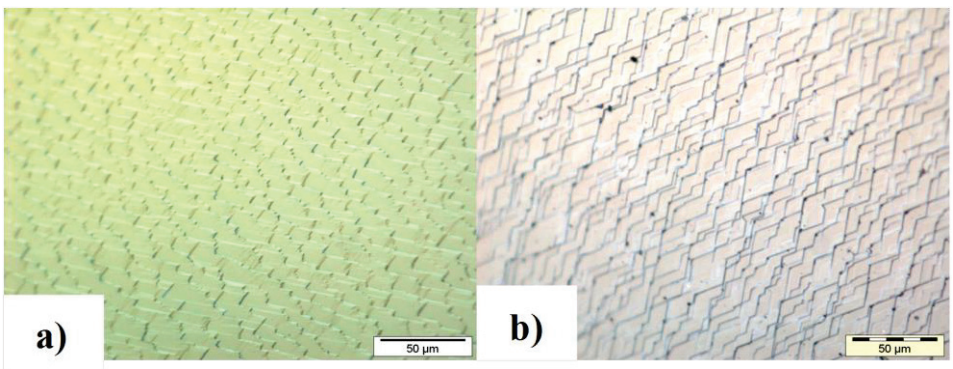

Figure 1. *Typical surface morphology of epitaxial layers grown within the study. (a) 3C layer using Si-Ge melt, (b) α-SiC layer using Al-based melt.*

The use of Si-Ge melts. As seen in figure 2, non-linear increase of layer thickness with methane partial pressure is obtained using $Si_{25}Ge_{75}$ melt at 1300°C. The growth rates of both methane and propane precursors are rather similar (~0.7 µm/h) at identically low carbon partial pressure. So the different reactivity of these gases does not seem to play a role at low partial pressure. However, they do not behave similarly at high partial pressure. Indeed, when using high carbon partial pressure (0.006) with propane, no measurable growth is obtained on the seed. This was already shown elsewhere [5] and was explained by the formation of a continuous SiC/graphite crust, which is visible by naked eye and covering the liquid surface immediately after the introduction of propane. In contrast, the use of even higher methane partial pressure (up to 0.0196) leads to some detectable growth of 1.2 µm with no obvious formation of any crust on the liquid (either by naked eye or using µ-Raman analyses on the solidified liquid. Furthermore, this deposit thickness does not change when increasing growth duration from 30 to 50 min. This difference with propane can be attributed to the well-known lower reactivity of methane. One can speculate that with methane some crust forms also on the liquid but its formation may not be instantaneous (as with propane) so that some deposit can form. Also, this crust with methane may be too thin to be detected, but sufficient for blocking the growth. This crust should not thicken with time (by forming a graphite deposit for instance) due to the low reactivity of methane, while the graphite deposit is observed using propane.

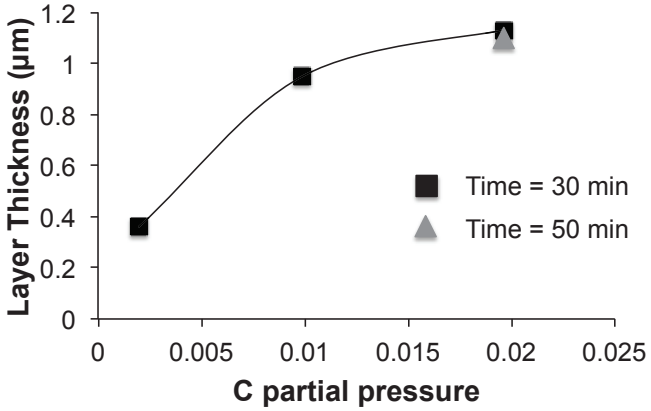

Figure 2. *Evolution of the thickness of 3C-SiC layers, grown by VLS on 6H-SiC 1° off axis seed using $Si_{25}Ge_{75}$ at 1300 °C, as a function of carbon partial pressure, for different precursors and for different growth time.*

The use of Al-based melts. Using ternary Al-Si-Ge alloys (samples AlSiGe01 and AlSiGe02) and high methane flux, the deposit thickness remains small and independent on growth time. However, one can notice in Table 1 a slight but noticeable increase in thickness with increasing Al content of the liquid (or decreasing Ge content). When no Ge is present in the liquid phase, the deposit thickness drastically increases up to 11.5 µm using the highest C flux studied here (with methane) and for only 30 min. This leads to growth rate as high as 23 µm/h for a temperature as low as 1100°C. This is illustrated in Figure 3. In all these samples, no visible crust could be detected on the liquid during or after growth.

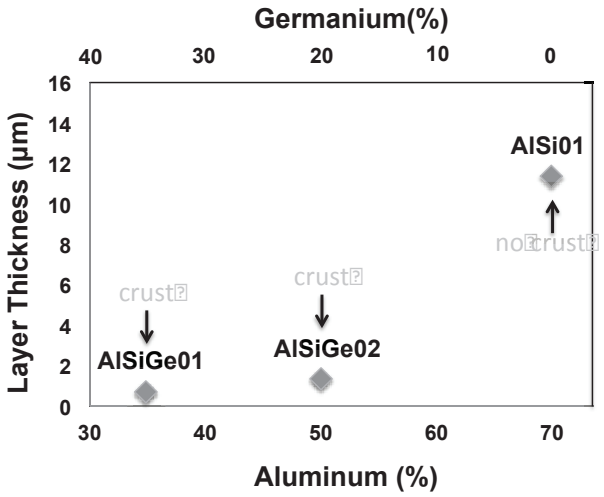

Figure 3. *Evolution of layer thickness as a function of Al-Si-Ge melts composition; all the melts contain 30% silicon. Temperature and carbon partial pressure (using methane) were fixed to 1100°C and 0.0196 respectively*

It seems that the same thin crust limiting effect as discussed above is occurring with the Ge containing ternary alloys, while it does not obviously occur without Ge in the liquid phase. Crust formation limit should be reached when C dissolution rate from the gas phase into the liquid becomes smaller than the precursor-feeding rate. Of course this limit should depend on the following parameters: temperature, C precursor and/or C solubility in the liquid. By fixing the temperature and the precursor (which is the case in experiments shown in figure 3), the only parameter that may change between the ternary and binary Al-based melts is the carbon solubility. It is known that pure liquid Ge has a lower C solubility compared to Al [4]. So, we believe that crust formation with Ge-based melts may be related to a reduction of C-solubility of the liquid.

So, if we come back now to the original goal of trying to increase the growth rate when using VLS mechanism, the present results shows that high C solubility melts should be used in order to shift away the limit of crust formation. Al-Si melts are good candidates but they have two serious limitations: Al element significantly evaporates above 1100°C and it may react severely with the graphite crucible (up to breaking it) after only few tens of min. That is why the VLS experiments in Table 1 using Al-Si melts are only conducted for 30 min. Adding some Ge in the liquid phase reduces this reactivity toward graphite but it is detrimental to reach high growth rate. Work is under progress in order to find either a better liquid phase than Al-Si or an appropriate configuration of growth allowing long time experiments. Concerning the choice between methane and propane, methane could be better since it provides a slower kinetics of crust formation. It may provide a wider range of C partial pressures before being limited by the crust formation.
Finally, note that the layers grown using Al-Si melts are heavily p type, which may be of great interest when considering that it is not easy to achieve thick p+-type layers with other techniques.

Summary

It is shown that the main limiting factor for achieving high growth rates using VLS mechanism is the formation of a crust on top of the liquid at high C partial pressure.

Using high C solubility liquid phase allows shifting the limit of formation of this crust and thus achieving higher growth rates. Methane may help also reaching higher growth rates by slowing the crust formation kinetics. Values as high as 23 µm/h were demonstrated with Al-Si melt but long time growth is still difficult to operate in this chemical system.

Acknowledgment

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