Study of electrical characteristics of tri-gate NMOS transistor in bulk technology

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Thèse de doctorat

Présentée devant

L'UNIVERSITÉ CLAUDE BERNARD - LYON 1

pour obtenir le grade de Docteur

École Doctorale : Électronique, Électrotechnique, Automatique

Par

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TITRE

Study of electrical characteristics of tri-gate NMOS transistor in bulk technology

Soutenue publiquement le 11 décembre 2014 devant la Commission d'Examen

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List of the symbols

Symbol	Description	Unit
A_{eff}	effective channel area	μm^2
B_{dop}	substrate doping	cm^{-3}
C_{ox}	oxide capacitance	F/m^2
C_p	parasitic capacitance	F/m^2
D_{it}	interface state density	$eV^{-1}cm^{-2}$
E_c	conduction band level	eV
E_F	Fermi level	eV
E_i	intrinsic Fermi level	eV
E_v	valance band level	eV
$\mathcal{E}_o$	vacuum permittivity	F/m
$\mathcal{E}_{si}$	semiconductor relative permittivity	-
Φ_F	Fermi potential	V
F_p	signal frequency	Hz
I_D	drain current	A
I_{cp}	charge pumping current	A
L	channel length	µm
q	electron charge	C
Q_G	gate charge	C
Q_{SC}	semiconductor charge	C
S	subthreshold slope	mV/dec
T_{ox}	oxide thickness	µm
t_r	raising time	s
t_f	falling time	s
μ_n	electrons mobility	$cm^2/V*s$
μ_{eff}	effective mobility	$cm^2/V*s$
Ψ_S	surface potential	F/m^2
V_{DS}	drain source voltage	V
V_{FB}	flatband voltage	V
V_{GS}	gate source voltage	V
V_G	gate voltage	V
V_{GB}	voltage between gate and bulk	V
V_{GBl}	low voltage between gate and bulk	V
V_{GBh}	high voltage between gate and bulk	V
V_{LTG}	lateral gate voltage	V
V_{TH}	threshold voltage	V
W	channel width	µm

Abstract

One of the recent solutions to overcome the scaling limit issue are multi-gate structures. One cost-effective approach is a three-independent-gate NMOSFET fabricated in a standard bulk CMOS process. Apart from their shape, which takes advantage of the three-dimensional space, multi-gate transistors are similar to the conventional one. A multi-gate NMOSFET in bulk CMOS process can be fabricated by integration of polysilicon-filled trenches. This trenches are variety of the applications for instance in DRAM memories, power electronics and in image sensors. The image sensors suffer from the parasitic charges between the pixels, called crosstalk. The polysilicon – filled trenches are one of the solution to reduce this phenomenon. These trenches ensure the electrical insulation on the whole matrix pixels. We have investigated its characteristics using *I-V* measurements, *C-V* split method and both two- and three-level charge pumping techniques. Its tunable-threshold and multi-threshold features were verified. Its surface-channel low-field electron mobility and the Si/SiO_2 interface traps were also evaluated. We observed no significant degradation of these characteristics due to integration of polysilicon-filled trenches in the CMOS process. The structure has been simulated by using 3D TCAD tool. Its electrical characteristics has been evaluated and compared with results obtained from electrical measurements. The threshold voltage and the effective channel length were extracted. Its surface-channel low-field electron mobility and the Si/SiO_2 interface traps were also evaluated. Owing to the good electrical performances and cost-effective production, we noticed that this device is a good aspirant for analog applications thanks to the multi-threshold voltages.

ACKNOWLEDGEMENTS

First and foremost, I would like to thank my supervisors, Guo–Neng Lu and Liviu Militaru for their support during these last three years. Your guidance let me to improve my research skills and well prepared me for future challenges. I am also very grateful to Francis Calmon. The advices and suggestions concerning the TCAD simulations, which you share with me, are priceless. I would like also to thank Sylvain Feruglio for his encouragement and patience while answering for all my questions. I want to thank the committee members Professor Dionyz Pogany, Professor Pascal Masson, Professor Olivier Romain and Francois Roy for the questions and engagement during the defense. Thank you once again; because of all of you, my defense has been an enjoyable moment.

Secondly, I would like to express my huge gratitude to the Annie Suslec, Rebecca Regis, and Martin Verdenelli who were all the time supporting me and helping me with the “complicated” bureaucracy. For the non-scientific side of my thesis, I would like to thank you all of my friends who reminded me that the life is not only a PhD. I thank as well Mateusz for his endless encouragement and forbearance.

Finally, I send my sincere gratitude to my parents Jolanta and Andrzej Zbierscy for their faith and for being around me.

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General Introduction

Nowadays one of the most important issues in microelectronics is connected with the scaling limits. Hence, the constantly researches are conducted in order to obtain better and better results. The well – known Moore's Law is a computing term which originated around 1970; the simplified version of this law states that processor speeds, or overall processing power for computers will double every two years. It turns out that the observed trends in terms of growth (doubling the density of the circuit and increasing performance of about 40% for each new generation of technology [1]) can be maintained by the reduction of conventional transistor channel. To forecast the future of the semiconductor industry, the International Technology Roadmap for Semiconductors (ITRS) [2] recognizes that there are physical limits to this growth: silicon CMOS transistor channel cannot be reduced beyond a certain size that is defined by physical boundaries [3]. However, as CMOS technology scaling begins to reach its theoretical limits, the ITRS predicts a new era known as "More Moore". Novel materials and devices show an ability to complement or even replace the conventional CMOS transistor. Actually, one of the most promising solutions is the multi-gates transistors. The well – known structures are the FinFET. For instance, Intel, in May 2011, has fabricated the first 3D FinFET in 22 nm technology (Fig. 0.1). It was the milestone in semiconductor industry.

Fig. 0.1 Intel's new 3-D transistor features vertical fins [4].

The multi-gates architecture can be applied for both analog and digital circuits. This structure can be also useful in controlled voltage oscillator or logical function with a reduced number of transistors compared to classical structure. One of the most common applications is in the image sensors domain, where, to overcome the crosstalk degradation, alike the increase of the dark current, deep trench isolation is introduced, which is one of the best solutions to suppress both optical and electrical crosstalk. It is due to its perfect barrier property compared to junction isolation [5].

There is a strong competition between the Silicon-On-Insulator (SOI) and the bulk technology. Additionally, this technology is less costly than the SOI technology.

A multi-gate NMOS transistor has been fabricated in 120 nm bulk CMOS technology by STMicroelectronics. In contrary to the conventional NMOSFET characteristics, few additional steps have been added during fabrication process, namely, the polysilicon – filled trenches have been integrated. The work aims to study this multi-gate NMOS transistor by electrical characterization and TCAD simulations. This structure can be studied as the conventional CMOS transistor for the surface top gate and particularities come from the lateral vertical gates, which can be considered as extra channels between source and drain. Therefore, the main objective of these researches is to investigate the influence of the trenches on the transistor performances.

In the subsequent of this manuscript, in the first chapter, the state of art is presented. The physics of MOS- transistor, as well as the different sort of multi-gate structures are introduced. What is more, the applications of these structures are introduced with special emphasis on the image sensors. The last section is dedicated to the explanation of analyzed structures.

In chapter two, the characterization techniques and the results are presented. To start, the *I-V* measurement is introduced to study the drain current level, the subthreshold slope, threshold voltage and low field mobility. Then, the *C-V* split method is used, mainly to establish the effective mobility calculation. To evaluate the quality of the interface, two- and three- level charge pumping is exploited. The results have been carried out for multi-gate structure (top gate and lateral gate transistor) and its conventional counterpart. Firstly, the top gate transistor behavior is examined and compared to its conventional counterpart. Then the lateral gates behavior is explained.

Chapter three is divided into two sections. The first one concerns 2D&3D TCAD simulations. The threshold voltages as well as the effective length are studied. The surface channel – low field

electron mobility and the Si/SiO_2 interface traps are also investigated. All of the simulation results are compared to the experimental results. The second part of this chapter concerns the SPICE modeling of the multi-gate transistor. Based on the results obtained by electrical measurements, a preliminary model is introduced. This part allows for better understanding the electrical behavior of examined structure. At last, the conclusions are presented in chapter four.

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1. Introduction

The first announces about the transistors are dated to mid-20thcentury. In 1953, H. Johnson from Radio Corporation of America (RCA) registered the first patent with integrated circuit [1]. He proposed to put all of the oscillator components on one silicon wafer. Nevertheless, the accurate explanation how to create all of the components, at that time, this conception was so innovative and there was no technology in which the inventor could realize this concept. In 1957, the transistors spread out and the ranges of its applications increased rapidly. It was obvious that transistor application may bring great improvement of device performance and shrink rapidly its dimensions. Therefore, Texas Instrument created the first silicon transistor which was one of the first bipolar transistors. One year later, a young engineer J. Kilby, created the oscillator on silicon wafer [2] and after several tests, the circuit was able to work properly. Then, in 1959, R. Noyce from Fairchild got to know that it is more efficient to produce a huge amount of transistors on one silicon wafer. Hence, his group elaborated the planar technology [3]. This technology is well – known, as in one silicon crystal it is possible to fabricate a huge amount of transistors, which are connected by aluminum paths situated on silicon – dioxide.

Firstly, the bipolar transistors have been used in all integrated circuits technologies. However, these structures had drawbacks, namely, the main factor which limited the size of the integrated circuits is the great amount of heat dissipation. The first research studies to improve these problems were oriented on seeking for the method which would release the heat in more effective way. The solution appeared in 1960 with the invention of the Metal Oxide Semiconductor (MOS) transistor which is characterized with smaller power consumption and size in comparison with the bipolar structure [4]. The invention has been castigated by the "scientific world" as in this device existed the overcoming of surface states which blocked electric fields from penetrating into the semiconductor material. Scrutinizing this problem it has been found that it can be easily reduced by applying the "sandwich" like configuration of metal (M – gate), oxide (O – insulation) and silicon (S – semiconductor). For this reason, the structure was designated MOSFET (Metal – Oxide – Semiconductor – Field – Effect – Transistor) commonly named MOS. Figure 1.1 shows the first MOSFET structure.

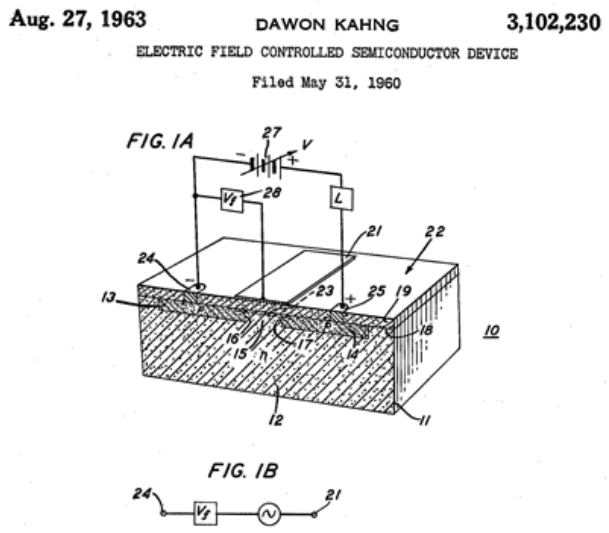

Fig. 1.1 The first MOSFET structure [4].

Despite this milestone invention, the device found its application in 1961, when Kahng indicated its potential. He valued its "ease of fabrication and the positivity of application in integrated circuit". Figure 1.2 presents the first integrated circuit consisting of four MOS transistors [5].

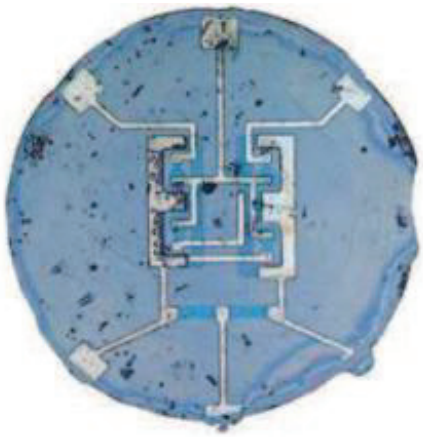

Fig. 1.2 First integrated circuit [5].

Due to its scaling capability as well as the low power dissipation, the MOS- transistor is applied in, nearly, 99 % of contemporary integrated circuits. Because of its ubiquity, it is worth to know how it operates. The next section will show the fundamental principles of the MOSFET structure.

1.1. MOSFET

The principal structure of the MOSFET is based on the MOS capacitor. The two regions, called source and drain were added. These regions are heavily doped with opposite doping to the substrate. In this case, when substrate is p doped, source and drain are n+ doped. With these doping configurations, this transistor is called NMOSFET. Before providing the explanation of this structure's principles a short description of the MOS capacitor will be presented.

1.1.1. MOS capacitor

MOS capacitor is based on MIS (Metal Insulator Semiconductor) structure. Thus, it consists of three material layers, namely, metal or polysilicon for gate, then isolator (oxide) and semiconductor doped p or n. Figure 1.3 presents structure of MOS capacitor (MIS structure).

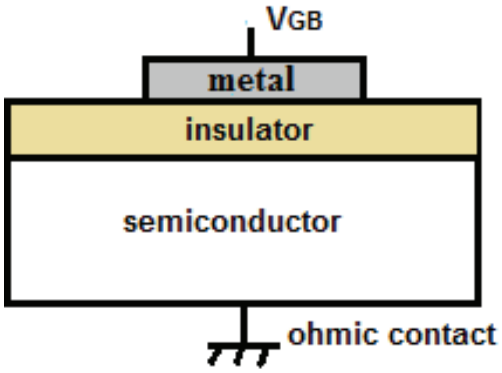

Fig. 1.3 Structure of MOS capacitor (MIS structure).

Voltage V_{GB} (between Gate and Bulk) creates the gate charge Q_G and its opposite charge Q_{SC} in semiconductor. Voltage variations provoke modification of charging state and different operating regimes appear. Capacitor can be either p – type or n-type. Figures 1.4A and 1.4B show five capacitor modes depending on V_{GB} voltage.

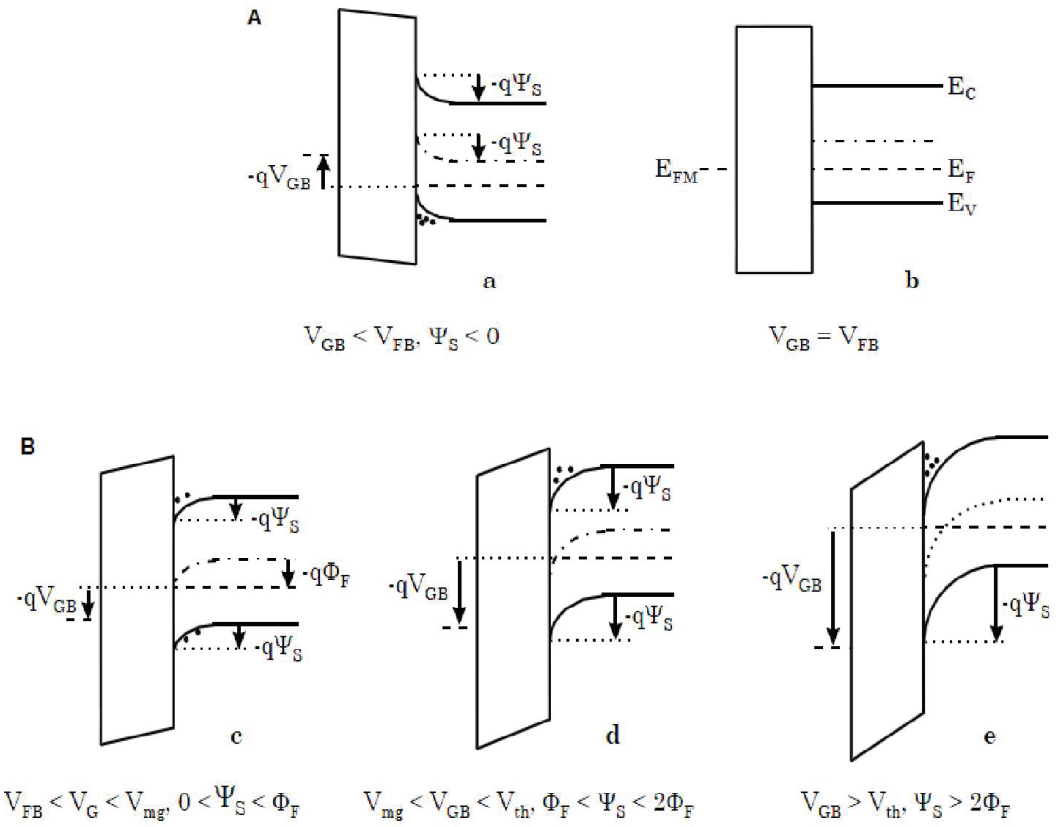

Fig. 1.4 Ideal MOS capacitor and region flatband (A). Regions of depletion, weak and strong inversion (B) [35].

Where Ψ_s is defined as the surface potential, q is the electron charge, Φ_F is a Fermi potential, E_F Fermi level, than E_c and E_v is conduction band and valance band energy. Below there are the definitions of the V_{FB}, V_{mg} and V_{TH}:

- V_{FB} (flatband voltage) - V_{GS} voltage applied when Ψ_s = 0V. It corresponds to transition from accumulation to depletion mode.
- V_{mg} - V_{GS} voltage is applied when $\Psi_s = \Phi_F$. It corresponds to transition from depletion to weak inversion.
- V_{TH} (threshold voltage) - V_{GS} voltage is applied when $\Psi_s = 2\Phi_F$. It corresponds to transition from weak inversion to strong inversion.

To understand properly the main three bias modes of MOS capacitor, the three different bias voltages will be discussed. In these studies, the main focus is on the bulk type p. The similar procedures are for type n with polarity inversion.

- when $V_{GB} < V_{FB}$

In this case, the gate voltage is smaller than the flatband voltage. Thus, the negative charge on the gate attracts holes from the substrate to the oxide-semiconductor interface. The accumulation charge is build up with a small amount of band bending. The majority of the potential variation is within the oxide. This mode is called **accumulation mode**.

- when $V_{FB} < V_{GB} < V_{TH}$

A greater value than flatband voltage is applied to the gate, hence, the negative charge occurs in the semiconductor. This phenomenon is due to the depletion of the semiconductor which begins from the oxide-semiconductor interface. What is more, with increasing gate voltage, the depletion layer width increases too. This mode is called **depletion mode**.

- when $V_{TH} < V_{GB}$

When the potential across the semiconductor increases twice, the bulk potential, another type of negative charge, emerges at the oxide-semiconductor interface: this charge is due to minority carriers, which form a so-called inversion layer. As one further increase the gate voltage, the depletion layer width barely increases further since the charge in the inversion layer increases exponentially with the surface potential. This mode is called **inversion mode**.

1.1.2. General principles

The basic NMOSFET structure is presented on Fig. 1.5. It consists of the bulk, generally in p-type wherein there are two n+ doped electrodes: source and drain. The MOS capacitor is set in bulk between source and drain. The control electrode of the MOS capacitor is the gate of transistor. Two types of MOSFET are distinguished:

- NMOSFET – the inversion channel consists of electrons. Hence, the channel is p-doped, whereas the source and drain are n-doped.
- PMOSFET – in the channel the major carriers are holes, thus the channel is n-doped but source and drain are p-doped.

These two transistors work symmetrically. The NMOSFET will be explained (Fig.1.5).

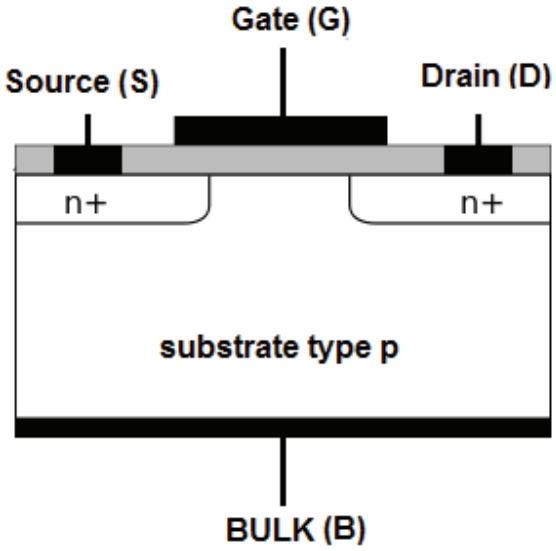

Fig. 1.5 Structure of NMOSFET.

A MOS transistor has two more terminals with respect to the MOS capacitor: the source (*S*) and drain (*D*) located on either side of the gate. If a voltage is applied between these two terminals *S* and *D*, a current may flow through the structure (Fig. 1.5). This current depends on the gate and drain biases, respectively, V_G and V_D, compared to V_S and V_B. Four operating modes are possible for the MOS transistor: the blocked mode, the linear mode, the weak inversion and the saturation mode. When the gate voltage V_G is lower than the threshold voltage, the free electrons are not sufficient to form the MOSFET channel. No current can circulate in the structure: the blocked mode. In reality, it is the ideal case because there is still a current below the threshold. When V_G is higher than the threshold voltage, the channel for current flow is created. Three operating regions are possible: the linear for weak V_{DS}, the saturation for high V_{DS} and the weak-inversion for V_{GS} smaller than threshold voltage. In linear mode, the drain current increases linearly with V_{DS}. On the other hand, in saturation mode, the increase of V_D is not reflected by an increase in current, hence the current saturates. In weak inversion region there is theoretically no current flow between drain and source (in practice, the subthreshold slope introduces leakage current).

1.1.2.1. Linear region

In the linear mode, current is proportional to the drain bias V_{DS}. Because of the bias to the drain there is a longitudinal channel in the E_L field. E_L field is given by:

$$E_L = \frac{V_{DS}}{L} \tag{I.1}$$

where L is the channel length. E_L causes electrons' flow from the source to the drain. There will be a current proportional to E_L.

$$I_D = q\mu_n n(V_{GS})E_L \tag{I.2}$$

where q is the elementary charge, the mobility of electrons μ_n and $n(V_{GS})$ is the concentration of free electrons. A simple model of the current in this regime is given by the expression [35]:

$$I_D = \frac{W}{L}\mu_n C_{ox}(V_{GS} - V_{TH} - \frac{V_{DS}}{2})V_{DS} \tag{I.3}$$

where W is the width of the channel device, L the channel length, μ_n the mobility of electrons in the channel.

1.1.2.2. Saturation region

If the V_{DS} value is very large, new effects appear. When the difference between the gate and the drain bias are situated below the threshold voltage, the channel on the drain side disappears. This is the pinch channel. The value of the drain voltage which cancels the drain side channel is then called V_{DSsat}, saturation voltage. Fig. 1.6 shows the NMOS transistor in saturation mode.

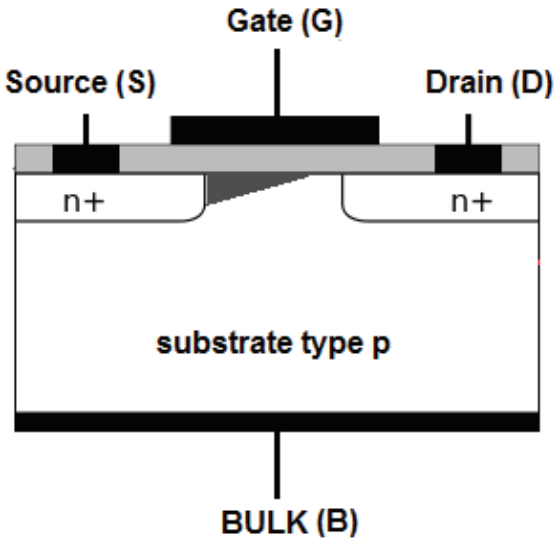

Fig. 1.6 MOSFET transistor in saturation region.

The drain current in the simplest model is presented as:

$$I_D = \frac{W}{2L}\mu_n C_{ox}(V_{GS} - V_{TH})^2 \tag{I.4}$$

and for the transconductance:

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{W}{L}\mu_n C_{ox}(V_{GS} - V_{TH}) \tag{I.5}$$

The simple equation for the drain current in saturation (I.4) indicates a quadratic dependence between I_D and V_{GS}. This dependence is true when the channel is long enough and gate biasing sufficiently low. The relation (I.5) assumes a mobility difference between gate voltage and threshold voltage. The longitudinal electric field which accelerates the electrons in the channel can be very high. This can lead to a saturation of the carrier velocity. In this case [35]:

$$I_D = C_{ox} W v_{sat}(V_{GS} - V_{TH}) \tag{I.6}$$

where v_{sat} is the limit velocity for electrons in the channel.

This law provides a linear relationship between I_D and V_{GS}. The transconductance is:

$$g_m = \frac{dI_D}{dV_{GS}} = C_{ox} W v_{sat} \tag{I.7}$$

Hence, this transconductance is constant and independent of the channel length and V_{GS}.

1.1.2.3. Weak inversion mode

When $V_{GS} < V_{TH}$ the transistor is turned off and there is no conduction between drain and source. Thus, the channel has not been formed and the current between drain and source should be theoretically zero. Nevertheless, the transistor is applied as a turned-off switch so the weak-inversion current exists, sometimes called as subthreshold leakage. In weak inversion mode the drain current is defined as:

$$I_D = I_{spec} \cdot \exp\left(\frac{V_{GS} - V_{TH}}{n V_T}\right) \cdot \left(1 - \exp\left(\frac{-V_{DS}}{V_T}\right)\right) \tag{I.8}$$

where, I_{spec} is a current at $V_{GS}=V_{TH}$, V_T the thermal voltage $V_T = \frac{kT}{q}$ and slope factor n is given by $n = 1 + \frac{C_D}{C_{OX}}$ with C_D is the depletion layer capacitance and C_{OX} oxide capacitance. The transconductance in weak inversion regime is easily derived:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{I_D}{n V_T} \tag{I.9}$$

The subthreshold slope is defined as $S = \left(\frac{\partial \left(\log \left(I_D \right) \right)}{\partial V_{GS}} \right)^{-1} = \frac{V_T}{n} \ln(10)$, the limit of S is then: $V_T \ln(10) \approx 60mV$.

The difference between the linear and saturation regimes is clear looking at a typical output characteristic of the MOS transistor (Fig. 1.7).

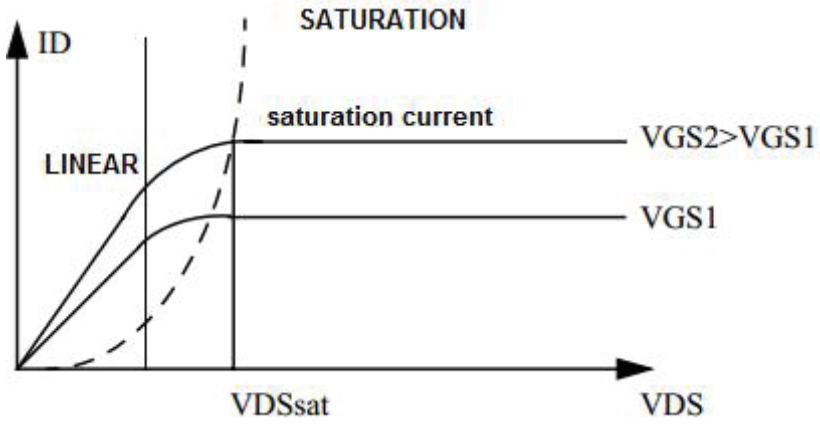

Fig. 1.7 Output characteristics of the MOS transistor.

1.2. Evolution of microelectronics

As it has been proved in section 1, the MOS transistor has been a major device for integrated circuits over the past two decades. The evolution of the emerging technologies, based on MOS transistor, is the topic under interest of different companies, institutions, as well as, governmental organizations specialized in technology and design of integrated circuits. Each year, the results and perspectives of these studies are published in ITRS. Nowadays, the predictions are till 2020 and concern the lithography, interconnections, memories and the emerging technologies. The first person who announced the scaling problem was Gordon Moore in 1965. He said that the complexity of ICs approximately doubles every two years [6]. He made a prediction of technological progress and explained comprehensibly the phenomenon of delivering, by the computer industry, the products which are smaller, more powerful and less expensive.

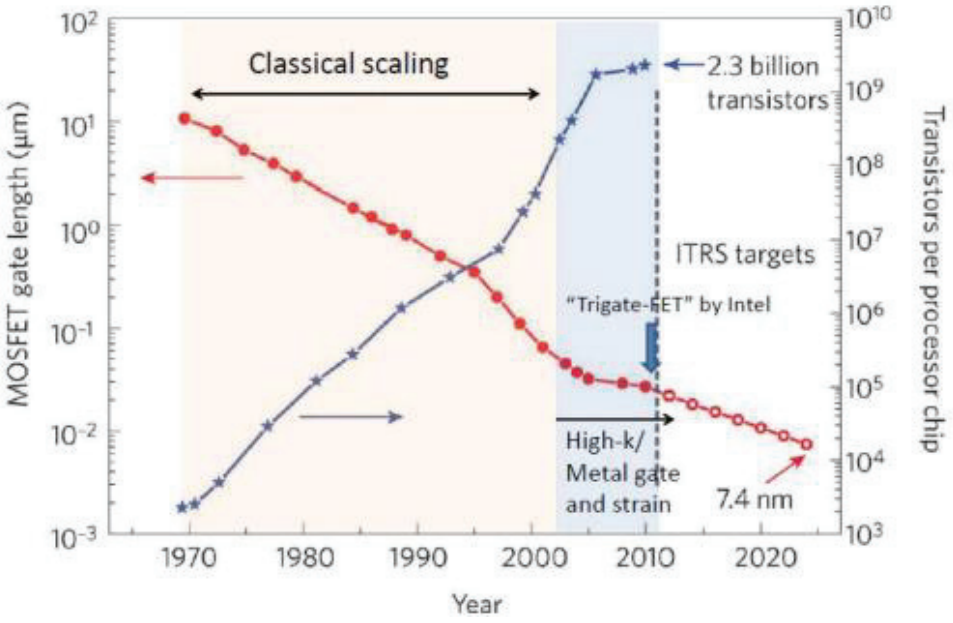

Fig. 1.8 The evolution of MOSFET gate length and number of transistors per processor chip [7].

The size reduction of the CMOS technology on silicon becomes more difficult and could stop when the channel length will decrease below 7.4 nm in 2024, according to forecasts by the ITRS. The International Roadmap for Semiconductors has highlighted the "miniaturization" and its associated benefits in terms of performances of the traditional parameters in Moore's Law. This trend will continue sustained by the devices of new materials and the application of new transistor concepts. This direction is called "*More Moore*" [6]. The second trend is characterized by functional diversification of semiconductor-based devices. These non-digital functionalities contribute to the miniaturization of electronic systems, although they do not necessarily scale at the same rate as the one that describes the development of digital functionality. Consequently, in view of added functionality, this trend may be designated "*More-than-Moore*" (MtM) [8]. Figure 1.9 shows the illustration of these two different domains by the ITRS.

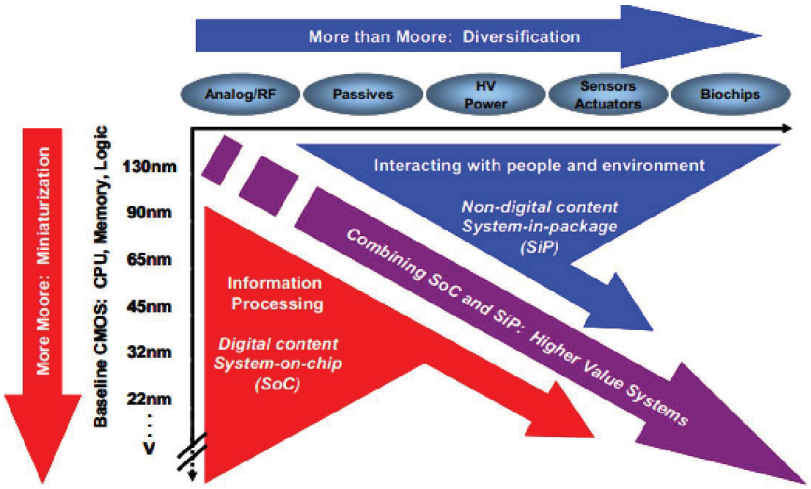

Fig. 1.9 The ITRS different domain [8].

From figure 1.9, it is noticeable that the "More Moore" law is more oriented on the miniaturization of the devices within the continuity in the approach to scaling. As device scaling continues into the 21st century, it turns out that past trends in growth, doubling circuit density and increasing performance by around 40% for each new technology generation [9] cannot be maintained by conventional scaling. Consequently, the channel length cannot be made much shorter. It leads to redundant short-channel effects and high off-state transistor leakage. New approaches are needed to allow the continued reduction of channel length in future technologies. Silicon-On-Insulator (SOI) technologies [10] and multi-gate structures appear at present to be the most promising approaches [11].

1.3. Multi-gate structures

One of the advanced MOSFET structures is multi-gate transistors. The first announcement about this device is dated on 1984, when T. Sekigawa [12] described the first double – gate MOSFET. This transistor might have improved the short channel effect, in contrary to the conventional structure. Five years later, in 1989, the first double gate MOSFET was fabricated [13]. From 90's, different structures of multi-gate MOSFETs have been invented and fabricated. Several examples are shown in figure 1.10 [14].

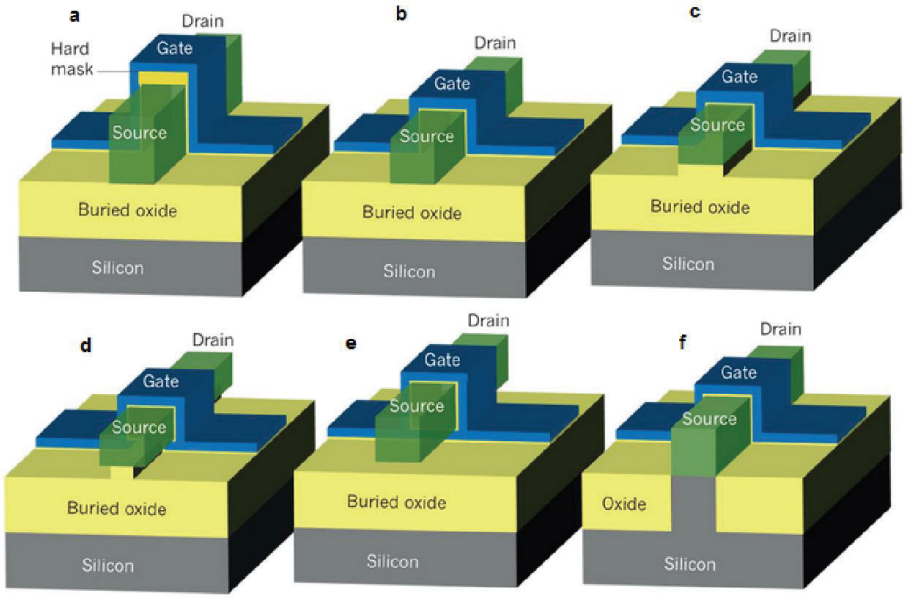

Fig. 1.10 Different types of multi-gate devices [14].

The second implementation of vertical channel was published by X. Huang [15]. Here, the "hard mask" is a thick dielectric that prevents the formation of an inversion channel at the top of the silicon. Next, the SOI triple gate or tri-gate MOSFET is presented (Fig. 1.10b). The device consists of a thin – film silicon island with a gate on the three sides. Based on similar architecture, the tri-gate MOSFET has been implemented [16]. Figures 1.10c and 1.10d show the structures with improved gate control. They are named as pseudo – fourth gate. Therefore, the first one is SOI Π-gate MOSFET [17] whereas the second one is called Ω-gate MOSFET [18]. The names Π - and Ω-gate simply reflect the shape of the gates. Another example of the multi-gate structures is gate – all – around device [19]. This device proposes the best control of the channel region and is usually fabricated using a pillar – like silicon island with a vertical channel. All of the presented devices were fabricated on SOI (Silicon on insulator substrate) [20]. This technology refers to the use of a layered silicon – insulator – silicon substrate in place of conventional silicon substrates, to reduce the device parasitic capacitance. In contrary to bulk CMOS technology, in the SOI devices, the silicon junction is above an electrical insulator. Nevertheless, the multi-gate MOSFET can also be fabricated with bulk silicon wafer. Figure 1.10f shows tri-gate structure, where source and drain are formed by ion implementation. The fabrication process of the bulk multi-gate transistors is less costly and less complicated compared to the SOI technology.

1.3.1. Applications of the multi-gate bulk structures

There are various applications of multi–gate structures like, in general, advanced logic applications [21]. In the static random access memory (SRAM) cells, since it is extremely important to shrink the size of memory cells, multi–gate structures allow to reduce the chip area [22]. The other application of multi–gate structures is the photodetection analog application, as in image sensors [23].

1.3.1.1. Image sensors

Image sensors are presented in wide range of human aspects, such as portable devices, security industrial vision, imaging phones, surveillance or guidance and navigation. There are two architectures of these devices: CCD and CMOS sensors (see Fig.1.11).

Charge couple device (CCD) is a simple silicon wafer which is created from photosensitive elements. It works as detector that catches and register the light, which is "bombarded" with photons flux. The wafer is divided into a lot of small, independent components, called "pixels". For each pixel an electrode is applied, which after being put on the voltage, creates a potential well. In this well the electrons are harvested. Although the CCD's image sensors have a lot of advantages like low Fixed – Pattern Noise (FPN), small pixel and high sensitivity to light, the researchers were looking for new opportunities to improve these devices and to reduce price. The alternative solution can be the CMOS image sensors technology. These devices offer many advantages in respect to the CCD such as lower power consumption, lower cost and higher level on integration [24]. In contrary to the CCD structures, in CMOS image sensors (CIS) every pixel consists of photodiode, transistor, as well as the analog-digital converter. CMOS imagers convert charge to voltage inside each pixel. CMOS image sensors are mainly divided into active pixels. In these structures each pixel consists of a photodetector and a transistor in order to connect it to a read out structure.

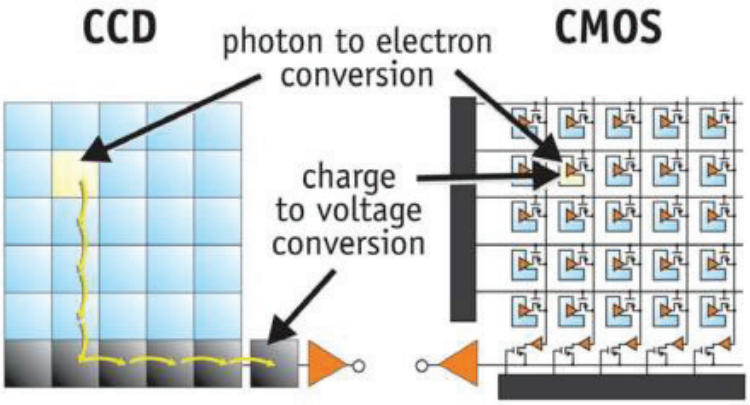

Fig. 1.11 Comparison between the CCD and CMOS image sensors.

CMOS sensors are sometimes referred as APS (Active Pixel Sensor), versus PPS Each pixel of a APS includes a photodiode and a transistor for line selection. However, the PPS were the first CMOS sensors introduced in the market (about 1970), the APS offered better performance, which is comparable to CCDs.

1.3.1.2. Crosstalk – challenge in image sensor miniaturization

In recent years, there is a tendency of the miniaturization of all the electrical devices. This trend did not skip the CMOS image sensors. The major challenge is to suppress all of the parasitic charge between the neighboring pixels, called the crosstalk [25]. This phenomenon might be the cause of the degradation of the image quality. There are three different origins of crosstalk, which are presented on figure 1.12.

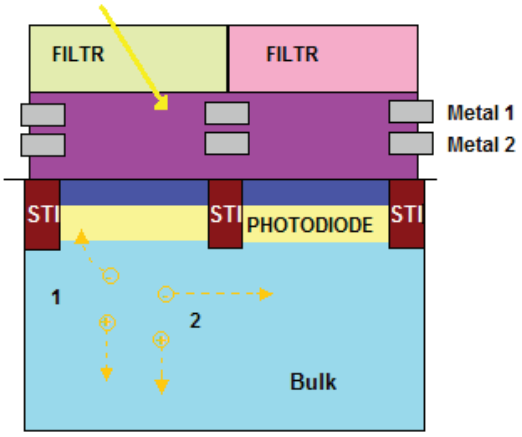

Fig. 1.12 Different origin of crosstalk in image sensors.

Firstly, the spectral crosstalk, which represents about 40% of the total contribution, is due to the imperfection of color filters. Then, optical crosstalk corresponds to a photon exchange between the neighboring pixels before electron/hole generations. Crosstalk can also occur in silicon substrate. Finally, the electrical crosstalk, that is responsible for 40 – 50% of the total crosstalk, consists of the parasitic exchange between the adjacent pixels. This exchange takes place in silicon material. What is more, the electrical crosstalk increases when the photodiode size decreases.

There are different techniques to reduce this effect, like µ-lenses optimization [26] or pixel isolation architectures. Two technological solutions to passivate the substrate interfaces are possible. The first is the implantation of the sidewall trenches, like the surface of the photodiode [27]. The second is to fill the trench with a conductive material, and use it as a MOS capacitor maintained in holes accumulation region. This specific integration (Capacitive Deep Trenches) was patented by Micron [28]. The trench isolations are one of the best structures to reduce the optical crosstalk due to its perfect barrier property compared to junction isolation [29]. The figure below presents the image sensor with deep trenches (Fig. 1.13).

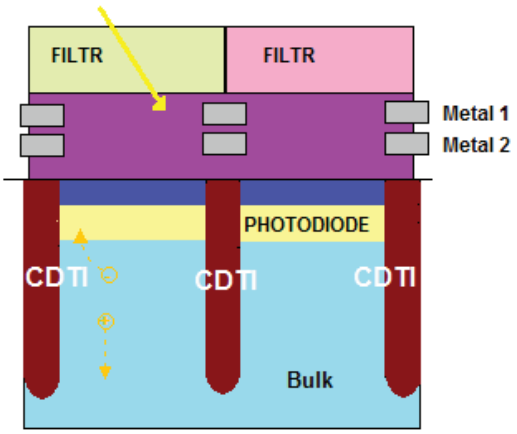

Fig. 1.13 Electric isolation between the pixels by the trenches.

The presence of trenches allows for creating the physical barrier (few micrometers). The electrical crosstalk decreases as the DTI become deeper [30]. This physical barrier significantly prevents the electron diffusion or drifts from pixel to another pixel. In the next part, the basic applications of the trenches will be presented.

1.3.1.3. The applications of deep capacitive trenches

The capacitive deep trenches are not only applied to image sensors. They are used for a long time for volatile memories (DRAM) and power electronic devices. Here, we will review some integration of these trenches, with a view to their incorporation in the image sensors technology. Firstly, the integration of the trenches in DRAM memory will be explained. Every memory – cell consists of the access transistor and the capacitor. These capacitive trenches allow for obtaining the value of the capacitance of several tens or hundreds of fF, maintaining an optimal density. The trenches, as well, are applied to the power electronic devices to create the vertical MOS transistor, like is shown on figure 1.14

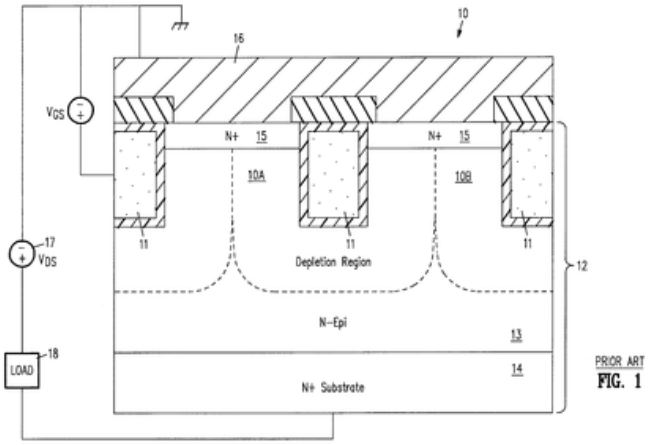

Fig. 1.14 Side cross-sectional view of a structure [31].

The gate insulator is a thick silicon oxide (50 nm for example [31]), the trench is then filled by doped polysilicon. A patented [32] integration has been retained to reduce current drilling volume for power MOSFETs. It consists in the conduction channel frame of two deep trenches polarized so it results in the abandonment of the deep substrate. This integration provides the basis for an additional possible use of these capacitive trenches. Vertical deep trenches surrounding the horizontal channel of the transistor can be biased (as lateral gates) to improve the transistor characteristics. In [30] it was proved that it is possible to set two deep biased trenches around the channel. This integration may be applied to the NMOS transistor, where the trenches might be biased in a way to improve the channel characteristics and to operate as additional gates.

1.4. Description of multi-gate NMOS transistors available for this study

The subject of this study is consequently a multi-gate NMOS transistor fabricated in 120 nm CMOS bulk technology. The structure has been fabricated and provided by STMicroelectronics (Crolles). In this structure, the transistor channel is framed by trenches. Thus, this device consists of three independent transistors.

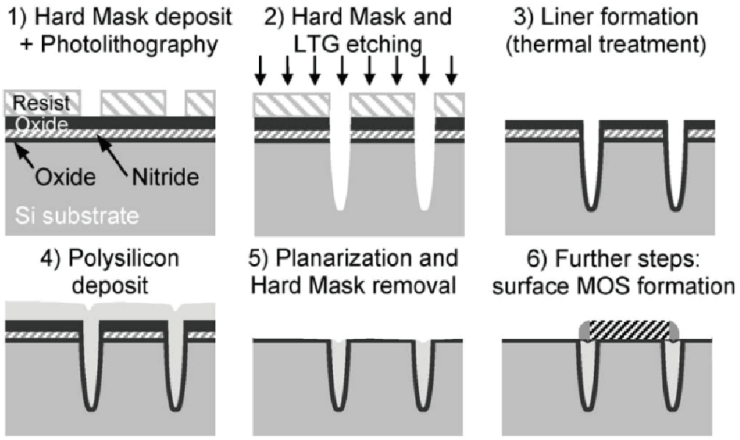

Fig. 1.15 Polysilicon – filled trench step [33].

The multi-gate MOSFET can be fabricated in standard CMOS process, as it is presented on figure 1.15: the multi-gate transistor manufacturing needs only a few additional process steps for integrating polysilicon-filled trenches. Firstly, trenches are etched in p-doped epitaxial layer (10^{15} cm^{-3}) and nitridation treatment was added to prevent doping diffusion through the oxide liner. Then, trenches are filled with boron – doped polysilicon deposition, before a planarization step to remove the remaining polysilicon. What is more, surface – gate and source – drain implants are realized following a standard CMOS process [33]. The device is manufactured on an epitaxial layer of thickness of about 1.5 μm, which is formed on the initial p+ doped substrate about $5x10^{18}$ cm^{-3}. The top gate insulator is formed of a thermal oxide with a nitrided thickness T_{ox} = 6.0 nm. The lateral insulation of gate trenches is made as well of a nitrided thermal oxide, but with a greater oxide thickness (T_{ox} = 10.5 nm). The polysilicon gate is doped standardly, thus, n-type (by implantation of phosphorus) with a very high concentration, about 10^{21} cm^{-3}. In

contrast, the polysilicon of CDTI (Capacitive Deep Trench Isolation) is p-doped, in situ, boron doping with a lower concentration of about 2×10^{18} cm $^{-3}$. The objective of p doping is to increase the flatband voltage of the trenches CDTI, and thus promote the accumulation regime of holes. The doping level was deliberately limited to limit the risk of boron diffusion. For device simulations, we have implemented the structure as shown in Fig. 1.16, where V_G signifies the top gate bias, V_{LTG} the lateral gate bias, h is the height of the lateral gate and W surface channel width

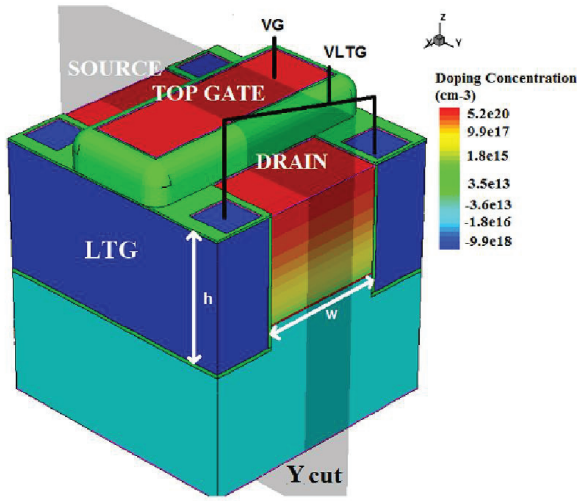

Fig. 1.16 Schema of the multi-gate structure.

A surface-gate MOSFET is situated between two trenches, whose distance determines the surface channel width W. In measurements, the two sidewalls channels are connected in parallel and controlled by the same voltage. The available device sizes for this study are summarized in table I-1.

Table I-1 Dimensions of the surface gate

W [µm]	L [µm]
0.2	**0.35**
0.3	**0.35**
0.4	**0.4**
1	**1**

The 2D schemas of the multi-gate structure are presented on figure 1.17.

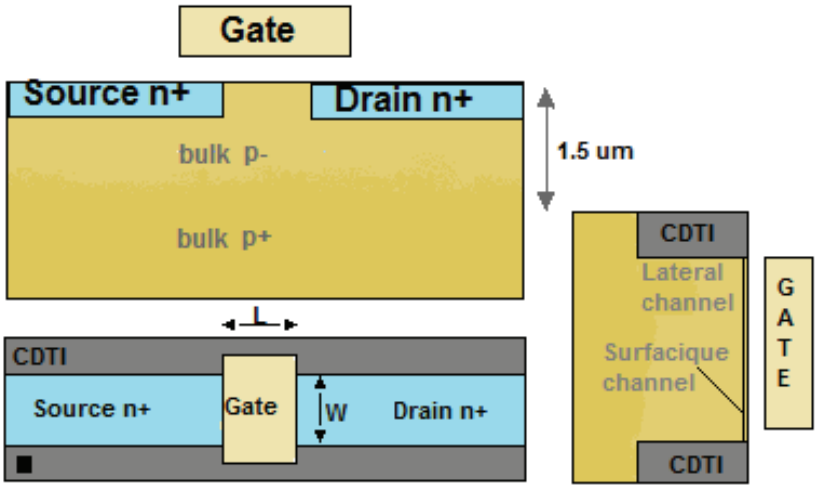

Fig. 1.17 Schematics views of the multi-gate transistor.

The schematics present the place where the lateral gate and surface gate channels are placed in structures. The *L* (the channel length) and *W* (the channel width) of the surface gate are indicated as well. The entire substrate is n+ doped and isolated laterally by CDTI trenches, while the deep substrate heavily doped p-type provides vertical isolation.

The first application of this structure is to use the surface transistor in the pixel array as a conventional NMOS transistor. The electrostatic effect of the biased trenches CDTI allows for determining the value of the threshold voltage close to that extracted from conventional transistor, even without the additional doping under the gate. This aspect will be developed at first.

However, it is also interesting to consider the lateral gates of multi – gate NMOS transistor structure like three independent transistors. Each of these transistors has different dimensions and parameters. This extremely interesting phenomenon called multi-threshold behavior has a wide range of the applications e. g. in logic circuits or analog electronics. The profound examination of the lateral gate will be done.

1.5. Conclusion

The aim of this section was to give an overview of current CMOS technology devices and their evolution. Due to drastic CMOS scaling, many issues have emerged mostly because of the Short Channel Effects (SCE), Narrow Channel Effects and downscaling problems. To improve SCE and allow future reduction of channel length, new approaches have already been implemented and proved their efficiency. Multi-gate structures are the most promising approaches. An alternative way is the use of Silicon-On-Insulator technology, as the SOI wafers are considered as the most important emerging wafer engineering technology in the next 3-5 years. Their improved switching speed and reduced power consumption over conventional provoke that the SOI wafers are over the Bulk-CMOS technology. Then this chapter has focused on multi-gate structure, the main advantage being a better electrostatically controlled channel (body) from multiple sides of the gate. Several examples were illustrated in this section. The structure of the multi–gate NMOS transistor with integrated polysilicon trenches has been presented. The top gate transistor can be applied in the pixel array as the conventional NMOSFET. However, the lateral gate might be considered as two different transistors in parallel.

Next chapter will present the experimental electrical characterizations of multi-gate and conventional transistors fabricated on the same wafer in order to evaluate the multi-gate performances and study the impact of the lateral trenches on the top gate.

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2. Electrical characterization

In this chapter, the characterization techniques and the experimental results are presented. Firstly, the *I-V* measurements will be introduced to extract and analyze the subthreshold slope, the threshold voltage, the low field mobility as well as the drain current level. Then, the *C-V* split method will allow us to calculate the effective mobility. To evaluate the quality of the interface, the two- and three- level charge pumping will be explained. The results have been carried out for multi-gate structure (surface gate and lateral gate transistor) and its conventional counterpart.

2.1. Overview of the different characterization techniques and associated experimental setup

The first type of the measurement is concerning the characterization of the $I_D(V_G)$ MOSFET characteristic with V_{LTG} constant or $I_D(V_{LTG})$ with V_G constant. For these measurements, the instrument HP 4156, which presents the capability to generate four voltages and to measure four currents simultaneously, was used. It is connected to the device under test by means of a probe station (Fig. 2.1), additionally an IEEE bus link to the computer allows acquiring the measured data for future treatment. The obtained data are analyzing with OriginPro software. Figure 2.1 presents a photo of the probe station with four micropositioners to place the tips onto the pads of the devices.

Fig. 2.1 Probe station used for electrical measurements

Another characterization technique was two- and three-level charge pumping technique. These measurements were conducted with the instruments presented on Fig.2.2.

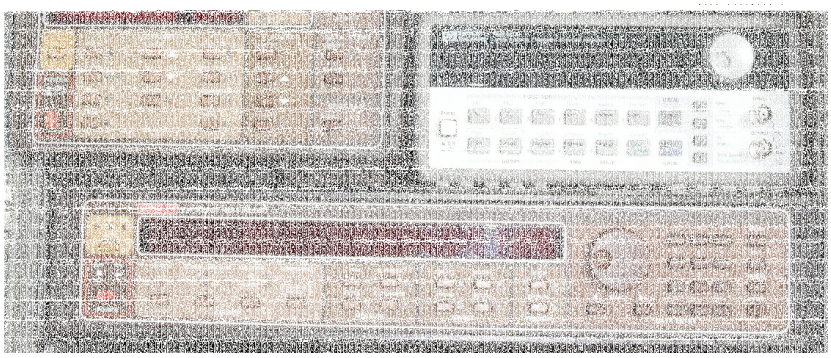


Fig. 2.2 Devices used to conduct the characterization by the charge pumping technique.

On figure 2.2, one can distinguish:

- Programmable electrometer Keithley 617 for charge pumping current measurements,
- Signal generator HP33120A which generate the gate signal,
- Source measure unit (SMU) Keithley 236 for $I_D(V_G)$ characteristic measurements.

All these devices are connected by IEEE protocol to the computer, on which the software CpWin is installed. This software allows for setup the following measurement configurations:

- $I_D(V_{GS})$ for surface potential determination (Ψ_S),
- $Icp(V_{GBl}, \Delta V_{GB}, F_P)$ with the signal sinusoidal and trapezoidal,
- $Icp(\Delta V_{GB}, V_3, t_3)$ for three level signal.

The *I–V* measurements have been conducted on the HP 4156 (Fig. 2.3), whereas the *C-V* measures on HP 4284 (Fig. 2.4).

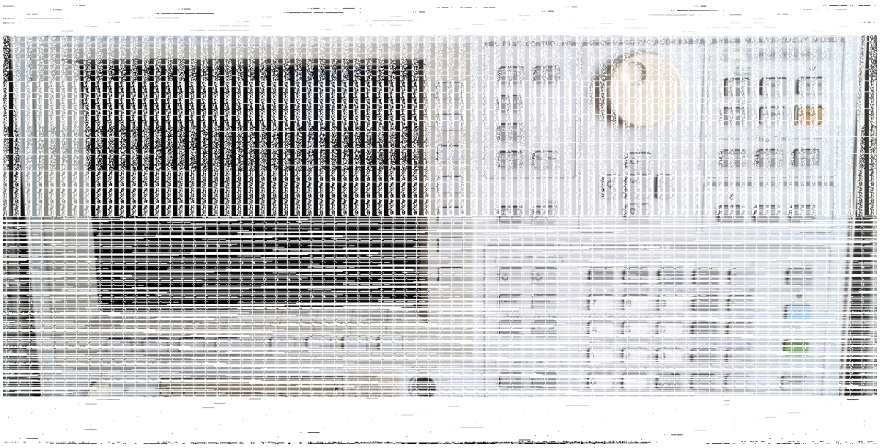


Fig. 2.3 HP 4156 used in *I-V* measurements.

Fig. 2.4 HP 4284 used for *C-V* measurements

2.1.1. Y function method

The Y function method [1] is an extraction method of the MOSFET parameters, based on the combined exploitation of the $I_D(V_G)$ and $g_m(V_G)$ characteristics. To eliminate the influence of mobility attenuation with gate voltage, the drain current expression is divided by the square root of the transconductance:

$$Y = \frac{I_D}{\sqrt{g_m}} = \left(\frac{W}{L} C_{OX} \mu_o V_{DS}\right)^{1/2} (V_G - V_{TH}) \qquad \text{(II.1)}$$

where C_{OX} signifies the oxide capacitance per surface unit, W is the channel width, L the channel length, μ_o the total channel mobility, V_{DS} the drain voltage, V_G the gate voltage and V_{TH} the threshold voltage. It should be remarked that this equation is valid only when the quadratic mobility reduction factor is equal to zero. From equation II.1 it is possible to notice that in strong inversion ($V_G >> V_{TH}$) the expression $I_D/g_m^{1/2}$ versus V_G should have a linear characteristic. Then, the intercept point and slope, which give respectively the threshold voltage (V_{TH}) and the low field mobility parameter (μ_o), have been extracted. Figure 2.5 presents the example of typical Y function characteristic with the illustration of the parameter extraction.

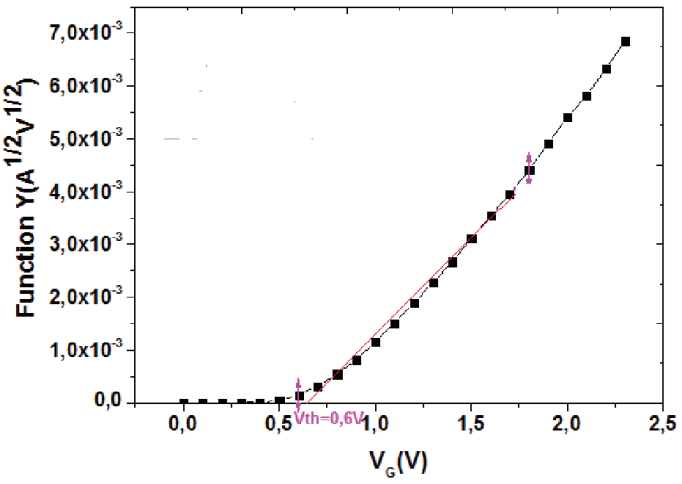


Fig. 2.5 Example of typical Y function characteristic with illustration of the parameter extraction (NMOSFET conventional W/L = 0.38 µm/0.28 µm, V_{DS} = 0.05V).

In this method, the threshold voltage and low field mobility parameter are independent, thus, we do not need one of them to detect the second one. The threshold voltage value can be determined directly from the $Y(V_G)$ characteristic, whereas the low field mobility is detected from equation II.1, which can be simplified:

$$Y = \frac{I_D}{\sqrt{g_m}} = V_G * \sqrt{\beta * V_D} \qquad \text{(II.2)}$$

Where β is defined as $\beta = \frac{S_x^{\,2}}{V_D} = \mu_o * C_{ox} * \frac{W}{L}$. S_x is the value of intercept extracted directly from Y function characteristic.

2.1.2. Hamer method

This method is an alternative for the threshold voltage extraction method [2] and is based on the drain current equation in linear region:

$$I_D = \frac{\beta V_D (V_{GS} - V_{TH} - V_D/2)}{1 + \theta V_e + \eta V_D} \qquad \text{(II.3)}$$

where β is the unsaturated gain factor, θ the gate field reduction parameter, η the lateral field velocity saturation parameter, V_D the drain voltage.

For the threshold voltage extraction θ is considered as zero. In this case a slope of βV_D and an intercept of $V_{TH} + V_D/2$ are obtained (Fig. 2.6) by plotting $I_D(V_{GS})$ curve.

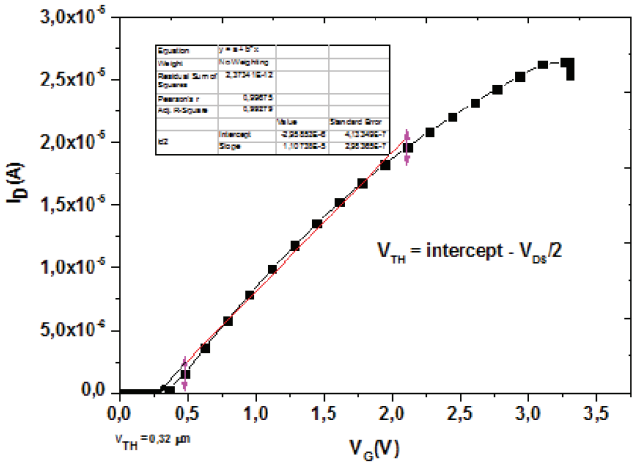


Fig. 2.6 Example of the extraction method of threshold voltage with the Hamer method [2].

The gain β and threshold voltage (V_{TH}) are derived, and then calculated by the following equations:

$$V_{TH} = intercept - V_{DS}/2 \tag{II.4}$$

$$\beta = slope/V_{DS} \tag{II.5}$$

For this extraction method, a lower value of V_{DS} is strongly recommended. The low value of V_{DS} would be advantageous in minimizing in extent of the saturation region and the effect of the drain bias dependence of η. In practice, too low value creates the difficulties in measuring the very small currents. The V_{DS} recommended value is between 20 mV and 100 mV. These values are also consistent with ensuring that the saturation region near the intercept is within the region of subthreshold currents.

2.1.3. C-V split method

The low-frequency *C-V* split method is the most common technique for mobility extraction, which was proposed first by Koomen [3]. It allows determining in a quantitative way the effective mobility in the NMOSFET interface as a function of the gate-bias-dependent channel charge density [4].

Theoretically, the effective mobility is obtained by relation II.6 which links the drain current in linear regime with gate biasing:

$$\mu_{eff} = \frac{I_D}{V_{DS}} \frac{L}{W} \frac{1}{Q_i} \qquad \text{(II.6)}$$

The extraction of the inversion charge is not direct; therefore, the channel-gate capacitance C_{GC} must be determined previously. Figure 2.7 presents the experimental setup.

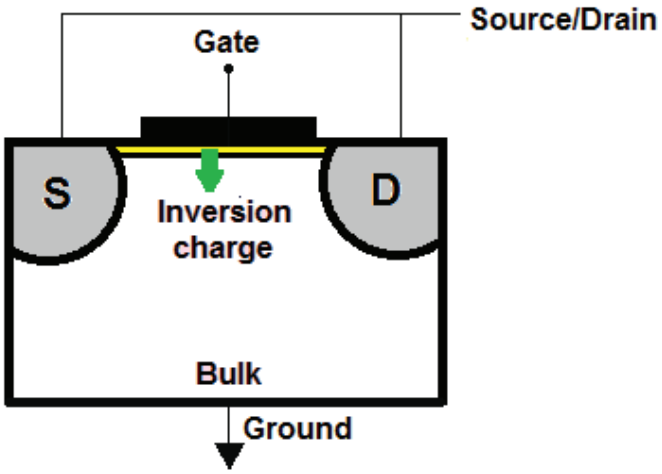


Fig. 2.7 Configuration of gate/channel capacitance (C_{GC}) measurements for split *C-V* technique.

Figure 2.7 illustrates how to measure the gate-channel capacitance (C_{GC}). It should be indicated that the measures have been performed on the HP 4284 device. The gate is connected to the high potential, whereas the source and drain are connected together and placed at the low potential, the substrate is grounded. In such biasing conditions, the inversion channel is formed, hence, capacitive response is measured. Knowing the value of the channel-gate capacitance, the inversion charge (Q_{INV}) can be obtained by the integration of the inversion capacitance C_{GC} as expressed:

$$Q_{INV} = \int_{-\infty}^{V_{GS}} C_{GC}(V_{GS})' dV_{GS} \qquad \text{(II.7)}$$

where V_{GS} is the gate voltage. Finally, based on the current-voltage measurements and result from equation II.6, the effective mobility can be calculated.

The *C-V* split method permits, as well, to extract the gate to bulk capacitance (C_{GB}) but in the examined structures, due to non-negligible parasitic capacitance, the C_{GB} could not be

determined.

2.1.4. Two- and three-level charge pumping.

The charge pumping technique is a characterization technique for determining the average density of electrically active states of the Si- insulator interface, the energy distribution and the capture cross section of these states [5]. It can be used for gate oxide thinner than 2 nm [6]. In 1969 Jesper and Brugler [7] reported a net DC substrate current generated by applying periodic pulse to the gate of a MOS transistor, keeping source and drain grounded. This current originates from recombination of minority and majority carriers at traps localized at the Si/SiO_2 interface. The observed current has been named the charge pumping current. The principles of two and three levels charge pumping are presented on Annex A.

2.2. I-V measurements

Static *I-V* measurements were performed on the multi-gate NMOSFET and on the conventional MOSFET fabricated on the same wafer. From the measured *I-V* characteristics, it is possible to extract some key parameters, such as the threshold voltage V_{TH}, the subthreshold slope *S* (see 2.2.1) and the low field mobility μ_o (see 2.3). The threshold voltage has been extracted with the Y function method (section 2.1.1) and Hamer method (section 2.1.2). For the multi-gate device, the surface-gate *I-V* characteristics were obtained with sidewall-gate biased below its threshold voltage, and vice versa for its sidewall-gate characteristics.

2.2.1. Threshold voltage and subthreshold slope

The threshold voltage (V_{TH}) is a crucial parameter for MOSFET modeling and characterization. It can be defined as the gate voltage from which the channel current becomes significant. Thereby, in simply words, it outlines the voltage when the transistor is blocked or active. The NMOS transistor is blocked when $V_G < V_{TH}$ (with $V_{TH} > 0$), whereas the transistor is active when $V_G > V_{TH}$. Second important parameter is subthreshold slope *S*. It is defined as the slope of the plot of logarithmic drain current versus gate voltage, extracted in weak-inversion region of MOS transistor. The equation II.8 presents the amount of V_{GS} which needs to decrease in order to reduce the drain current by one decade:

$$S = \frac{dV_{GS}}{dI_D} \tag{II.8}$$

For ambient temperature subthreshold slope is ~60mV/decade [8],[9]. However, the feasible slopes are around 70~80 mV/decade.

2.2.2. Results for the surface gate

Firstly, the studies concerning the top gate will be presented. Additionally, the results have been compared with the conventional NMOSFET. To measure the $I_D(V_{GS})$ characteristic, we varied the top gate voltage (V_G) from -2V till 3.3V with fixed lateral gate voltage V_{LTG} = -2V. In this situation, the lateral gate is blocked and the conduction is only through top gate channel. The source-drain voltage is fixed to 50 mV to stay predominantly in linear region. To conduct these analyzes, the multi-gate transistor with dimension *W/L* = 0.3 µm/0.35 µm and conventional NMOSFET with *W/L* = 0.38 µm/0.28 µm have been chosen.

Fig. 2.8 Characteristic I_D (V_G) (surface gate of multi-gate MOSFET, W/L=0.3 µm /0.35µm, NMOSFET conventional W/L=0.38 µm /0.28µm, V_{DS}=50mV, V_{LTG} = -2V).

Figure 2.8 presents the *I-V* characteristics for both multi-gate structure and its conventional counterpart. The subthreshold slope of the multi-gate NMOSFET is 93 mV/dec compared with 83 mV/dec for the conventional NMOSFET. The threshold voltage has been extracted by Hamer method with V_{LTG} = -2V: for multi-gate structure (W/L=0.3 µm /0.35µm) V_{TH} = 0.49 V and for classic NMOSFET (W/L=0.38 µm /0.28 µm) V_{TH} = 0.45V. As these values are nearly similar, we can state that the top gate multi-gate structure behaves as the conventional structure.

Fig. 2.9 Characteristic I_D (V_{GS}) (surface gate, W/L = 0.3 µm /0.35µm, V_{DS} = 50mV, V_{LTG} = -2V, -1V, 0V).

Analogous analyzes have been conducted for different lateral gate bias voltages V_{LTG} = -2V, -1V, 0V to detect the lateral gate impact on the top one. The threshold voltage shift has been observed. The top gate threshold voltage increases with the decrease of lateral bias. What is more, the threshold voltage is modulated by the lateral gate biasing. This effect can be observed notably for V_{LTG} higher than -2V, above this value the transistor performance is degraded. From the measured I_D-V_{GS} characteristic with variations of the sidewall gate bias (V_{LTG}), the extracted surface-gate threshold voltage related to V_{LTG} can be established. Fig. 2.10 plots the extracted value of V_{TH} with both Hamer and Y function methods.

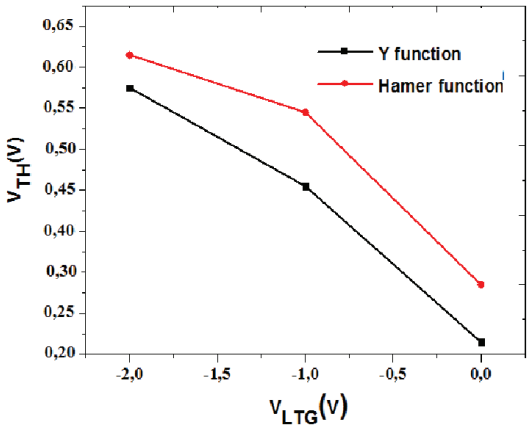


Fig. 2.10 Threshold voltage variation with V_{LTG} for multi-gate NMOS transistor (W/L = 0.3 µm/0.35 µm), using the Y function and the Hamer method, with V_{DS} = 50 mV and V_{BS} = 0 V.

Despite a small difference in the evaluated threshold voltage between the two methods, a clear tendency can be seen: the lowering of the sidewall-gate bias leads to an increase in the surface-gate threshold voltage. This dependence may be illustrated by the electrostatic modulation effect of the sidewall-gate bias on the effective surface channel width. This effect can be explained by the effective doping level, namely, it is possible to change the average V_{FB} voltage by adjusting the lateral gate voltage (V_{LTG}). By biasing the lateral gate trenches negatively, for instance in holes accumulation region, the threshold voltage is shifted by an amount corresponding to the increase of the holes concentration by electrostatic effect.

By using the Y function, the mobility has been extracted. The surface gate transistor of multi-gate structure has the mobility μ_0 = 174 $cm^2/V*s$, whereas the conventional structure μ_0 = 221$cm^2/V*s$. As we expected, the obtained mobility values are coherent and, generally, all of

the extracted parameters are nearly similar.

To complete static *I-V* studies, positive bias voltage was applied on the lateral gate. Surface gate characteristics are shown on figure 2.11.

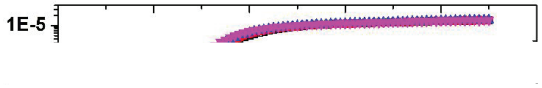


Fig. 2.11 Characteristic I_D (V_{GS}) (W/L = 0.3 µm/0.35µm, V_{DS} = 50mV, V_{LTG}= 3V, 4V, 5V, 6V, V_G=-2V).

We observe that positive voltage has an influence on threshold voltage as well (as it was for negative V_{LTG}). With the decrease of the positive lateral gate bias, the top gate threshold voltage increase as well. Figure 2.12 shows this phenomenon. The values have been extracted by Hamer method.

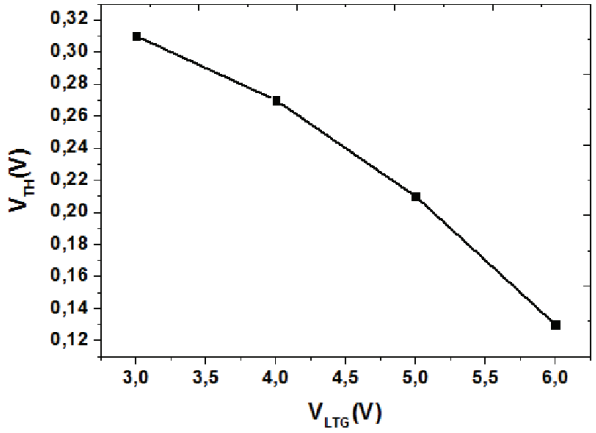


Fig. 2.12 Threshold voltage variation with V_{LTG} = 3V, 4V, 5V, 6V for multi-gate NMOS transistor extracted by Hamer method
(W/L = 0.3 µm/0.35 µm) with V_{DS} = 50 mV, V_G = -2V, V_{BS} = 0 V.

The evolutions of the threshold voltage function of the top gate length (L) for the multi-gate and conventional structure are presented on figures 2.13A and 2.13B. The V_{TH} is degraded due to the electrostatic modulation of the trenches.

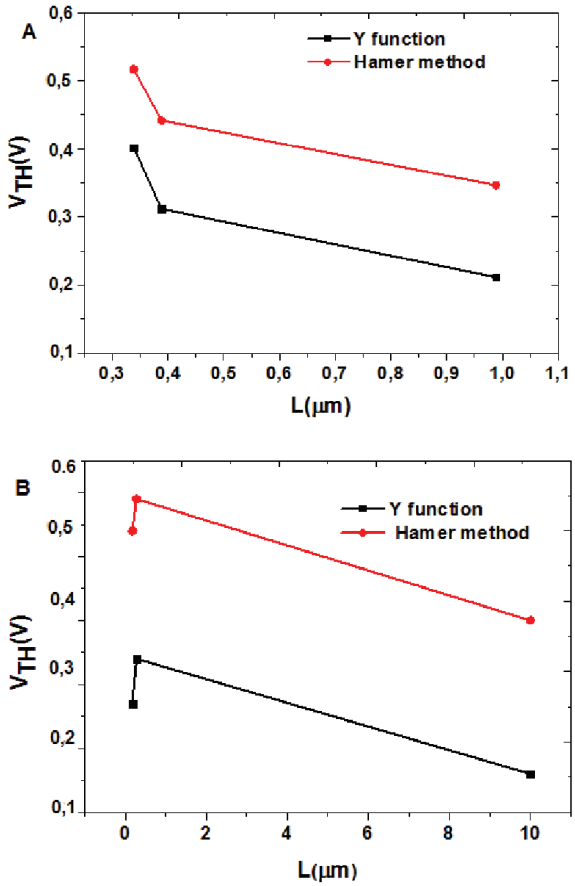


Fig. 2.13 Characteristics $V_{TH}(L)$ for (A) the multi-gate MOSFET, W = 0.2 µm , L=0.35; 0.4;1 µm (V_{LTG} = -2V) and (B) for conventional MOSFET, W = 0.2 µm L=0.28; 0.38; 10 µm.

The characteristics present for both methods and both structures, an increase in the threshold voltage while decreasing the transistor length. For the multi-gate transistor, this phenomenon is, probably, due to the electrostatic influence of the trenches. Moreover, it is clearly noticeable that extracted values are not coherent. It can be explained by the artifact in parameters determination. The second interpretation is a phenomenon of the short channel effect, from which the relation can be noticed: with the increase in threshold voltage the effective gate doping increases as well.

2.2.3. Results for the lateral gate

It is possible to characterize the conduction in the lateral gate channel. This channel is unusual since its extension is vertical. The results were compared with that from the surface channel studied previously.

Figure 2.14 presents the difference between the $I_D(V_{LTG})$ lateral gate characteristic and its top gate counterparts analyzed in section 2.2.2. The top gate characteristics have been extracted with positive lateral gate bias (V_{LTG} = 6V) and with negative lateral gate bias (V_{LTG} = -2V).

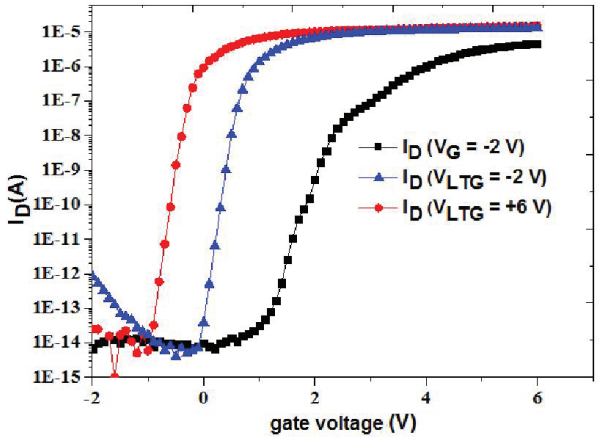


Fig. 2.14 I_D-V_G and I_D-V_{LTG} characteristics of multi-gate NMOSFET (W/L = 0.3 µm/0.35 µm), with V_{DS} = 50 mV and V_{BS} = 0 V.

We can observe that the multi-gate MOSFET has different *I-V* characteristics between the lateral gate and top gate. For the lateral gate, the threshold voltage is much higher compared to its counterpart, evaluated for the top gate transistor. As the lateral gate characteristic exhibits three bumps (peaks), thus the three threshold voltage can be distinguished. The first one is about V_{TH1} = 1.9 V, the second one (second peak) V_{TH2} = 2.3 V and the third one (third peak) V_{TH3} = 3.6 V (Fig. 2.14). The lateral gate threshold voltages have been determined by SPICE simulations (section 3.5.2). Thus, the lateral gate threshold voltage (V_{TH3} = 3.6 V) is about, nearly, nine times more important than the top gate one. This phenomenon can be explained by the different type of doping for each gate, where top gate is doped n+, the lateral is poly-silicon doped p+. The lateral

gate exhibits a multi-threshold behavior, which is indicated by the three peaks on its I_D-V_{GS} characteristic. These peaks represent three different channels with different threshold voltages. Figure 2.15 presents the *I-V* characteristic with the indication of three peaks indication.

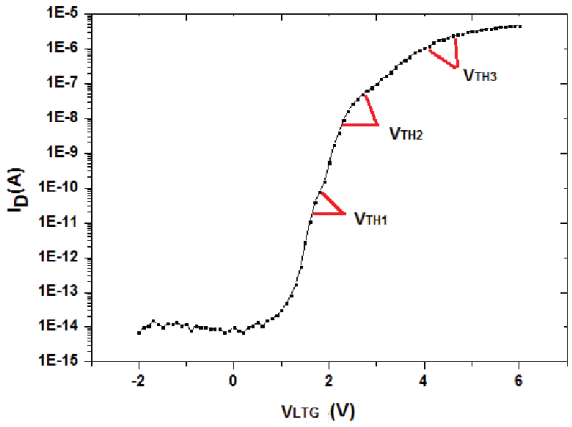


Fig. 2.15 I_D-V_G characteristic of multi-gate NMOSFET (W/L = 0.3 µm/0.35 µm), with V_{DS} = 50 mV, V_G = -2V and V_{BS} = 0 V.

Therefore, it behaves like three transistors in parallel with different dimensions and parameters. This phenomenon can be explained by the non-homogenous lateral gate doping. The important point is that the lowest lateral threshold voltage is about 1.9V, hence, for V_{LTG} > 1.9V the drain current of the device will include lateral channel contribution, which is significantly smaller compared to top gate current.

2.3. Mobility determination

Before the presentation of our results, a short description concerning the mobility will be presented. Mobility is an important parameter which defines transport of free charge carriers in semiconductor. It is described as the relation between the electrons or holes velocity (v_d) and the electric field (E). In other words, it characterizes how quickly the electrons or holes, triggered by the electric field, move through a metal or semiconductor.

The mobility is expressed as:

$$v_d = \mu * E \quad \text{(II.9)}$$

The mobility unit is $cm^2/(V*s)$. Mostly, in low-doped solid silicon at ambient temperature, the electrons mobility is about 1500 $cm^2/V*s$ and 500 $cm^2/V*s$ for holes [11]. For non-planar semiconductors, such as Si, the mobility is affected by the carrier and lattice interactions:

- **Phonon interactions [11]**

Phonons are created by the thermic vibrations in crystal-like lattice. Due to these particles, the modification of the electrical potential is observed. The movements of the free carriers are disturbed by the potential variations. Hence, the decrease of the carrier mobility is observed. There is a general tendency: with the increase in temperature, the mobility decreases. In this case, the structure has been characterized at ambient temperature with limited self-dissipation. Therefore, the mobility variation with temperature is negligible.

- **Coulomb interactions [12]**

The Coulomb interactions are known as the dopants ionized interactions with presence of traps, oxide charge. All of these interactions influence the free carrier mobility (mobility decreases). This influence depends also on the temperature. Indeed, at medium and high temperatures (>100K), it is less important that at low temperatures (< 100K). This phenomenon is due to the important thermic energy of the carriers at high temperatures.

- **Surface roughness diffusion [13]**

Due to the fabrication process, the device interface, usually oxide/semiconductor or oxide/metal (poly-silicon in our case), is not smooth. This roughness provokes the mobility decrease. This interaction strongly depends on the transversal electric field. Indeed, with increasing of the electric field, there is an increase of the charge carrier density near the interface and the interactions with roughness surface are more significant.
The mobility decrease is calculated as:

$$\mu_{SR} = SE_{eff}^{-2}\Delta^{-2}L_C^{-2} \quad \text{(II.10)}$$

when Δ is an average depth of the fluctuations, L_c the average distance between the asperity, E_{eff}

signifies the effective electric field and *S* is a transistor surface.

To sum up, all the presented interactions responsible for the mobility decrease are presented on figure 2.16: the different zones indicate the nature of interaction.

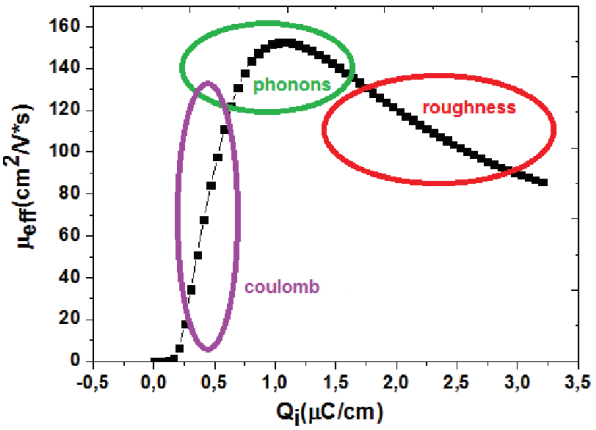


Fig. 2.16 Interactions types as well as its influence on the effective mobility characteristic in function of the inversion charge.

First of all, the mobility has been extracted by Y function method for lateral and top gate structure at low electric field (V_{DS} = 50mV).

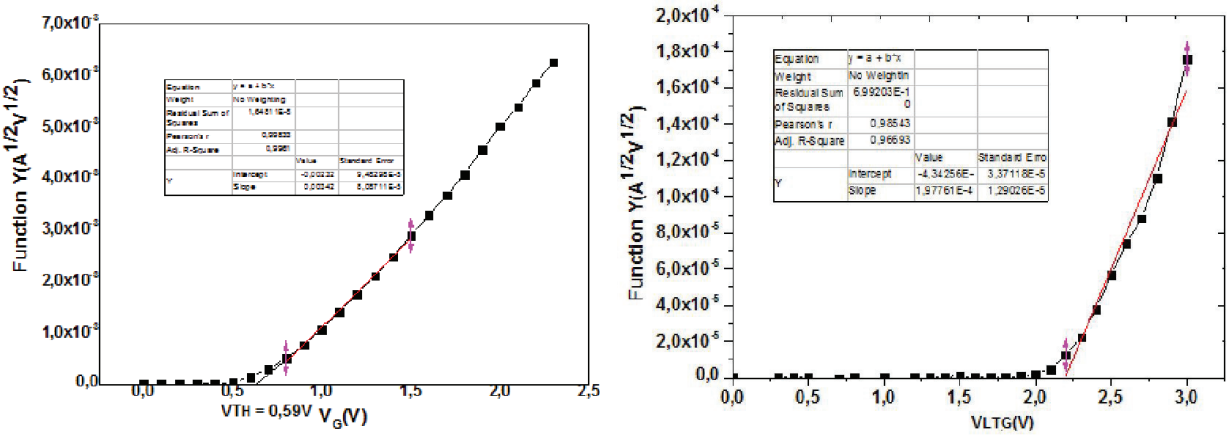


Fig. 2.17 $Y(V_G)$ function and $Y(V_{LTG})$ function for V_G = -2V and V_{LTG} = -2V (W/L = 0.3 µm/0.35 µm).

For the top gate transistor the value of the mobility has been evaluated and for top gate is $\mu_{o,surf.}$ = 200 cm^2/V*s whereas for lateral gate $\mu_{o,lat.}$ = 174 cm^2/V*s. This difference indicates that the density of the interface defects is higher for the top gate.

To summarize, the table II-1 presents the comparison of the extracted results for both lateral and the surface gate.

Table II-1 The comparison of the results for top and lateral gate.

	Top gate	Lateral gate
Oxide thickness (*Tox*)	6 [nm]	7.5 [nm]
Threshold voltage (V_{TH})	0.4 [V]	1.9 [V]; 2.3 [V]; 3.6 [V]
Mobility (μ_o)	200 [cm^2/V*s]	174[cm^2/V*s]

2.3.1. Effective mobility extraction

Among variety of techniques which allow obtaining the effective mobility, we can distinguish the Y function method which is explained in section 2.1.1, the high frequency *C-V* split method [14] or low-frequency *C-V* split method [15]. For our measurements, we decided to apply the latter since it is more reliable and precise (see section 2.1.3). Moreover, the high – frequency *C-V* split method requires specific test-structures which were not available for this study.

2.3.1.1. Results for the surface gate

Here, the results obtained by *C-V* measurements at the surface gate will be presented. First of all, the $C_{GC}(V_G)$ characteristics for several different transistors dimensions are presented.

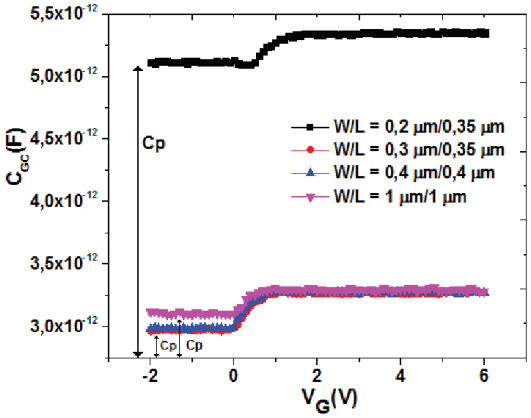


Fig. 2.18 $C_{GC}(V_G)$ characteristics for *W/L*= 0.2 µm /0.35 µm, *W/L*=0.3 µm /0.35 µm, *W/L*=0.4 µm /0.4 µm, *W/L*= 1 µm /1 µm with F_P= 1MHz.

The channel-gate capacitance for all transistors dimension is presented on figure 2.18. The smallest transistor has the highest parasitic capacitance (C_p), as for the rest there is nearly the same value. To obtain the "proper" value of the oxide capacitance (C_{ox}), we need the transistor surface determination, so the parasitic capacitance correction has been done [16]. What is more, in reality, there is a difference between the transistor surface determined by channel dimensions (S_t) and the real surface applied for measurements, here called as (S_r). Since a real surface corresponds to several transistors in parallel, it is impossible to directly measure the capacitance of a single transistor. Therefore, it is essential to determine S_r for calculating the proper value of inversion charge. The equation II.11 is transformed according to the surface determination (II.12).

$$C_{OX} = \frac{\varepsilon_o \varepsilon_{SiO_2} S_r}{T_{OX}} \qquad \text{(II.11)}$$

$$S_r = \frac{C_{OX} T_{OX}}{\varepsilon_o \varepsilon_{SiO_2}} \qquad \text{(II.12)}$$

where $\mathcal{E}_o$ is the vacuum permittivity, $\mathcal{E}_{SiO2}$ the semiconductor permittivity and T_{ox} signifies the oxide thickness.

Knowing the real value of the surface, the calculation of the real value of the inversion charge can be executed by the following expression:

$$Q_{ireal}(V_G) = Q_i(V_G) * \frac{S_t}{S_r} \qquad \text{(II.13)}$$

Figure 2.19 presents the characteristics after parasitic capacitance and surface correction.

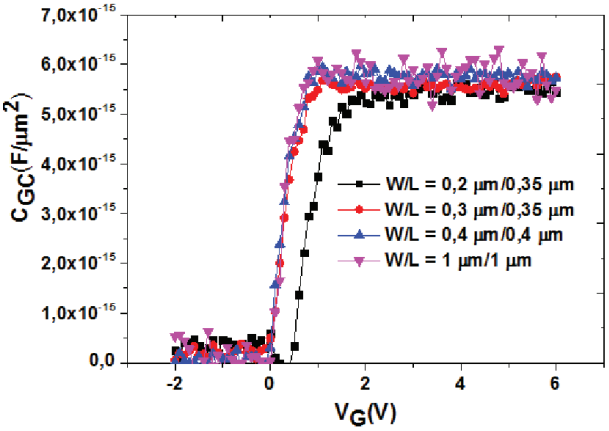
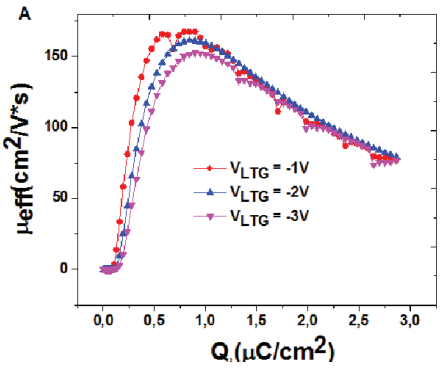
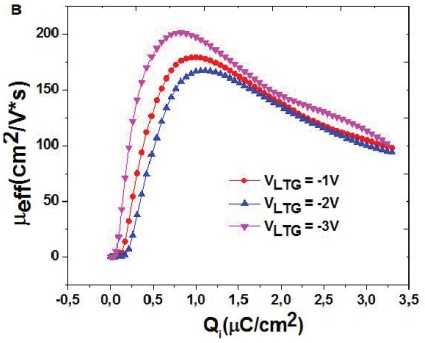


Fig. 2.19 $C_{GC}(V_G)$ characteristics for W/L=0.2 µm /0.35 µm, W/L=0.3 µm /0.35 µm, W/L=0.4 µm /0.4 µm, W/L=1 µm /1 µm after parasitic capacitance and surface correction.

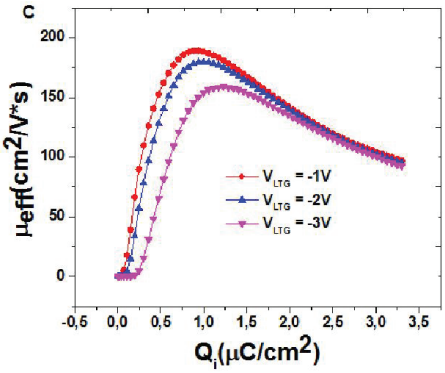
According to the expressions (II.6), (II.7) and based on the results from *C-V* split method and *I-V* characteristic, the effective channel mobility, for surface gate, was determined. Figures 2.20a, 2.20b, 2.20c, 2.20d present the effective mobility as a function of inversion charge for all transistor dimensions. The extractions have been done for V_{LTG} = -1V, -2V, -3V.



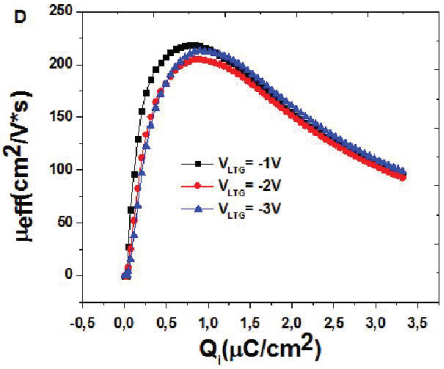
W/L = 0.2 μm/0.35 μm



W/L = 0.3 μm/0.35 μm



W/L = 0.4 μm/0.4 μm



W/L = 1 μm/1 μm

Fig. 2.20 Effective mobility in function of the inversion charge for V_{LTG} = -1V,-2V,-3V.

Analyzing the results from above characteristics, it is clearly visible that the transistors with channel dimension *W/L* = 0.2 μm/0.35 μm (Fig. 2.20A) and *W/L* = 0.4 μm/0.4 μm (Fig.2.20C) present similar tendency of effective mobility variation. What is more, with V_{LTG} decrease, the Coulomb and phonons effects decrease as well but surface – roughness diffusion is constant since it is not dependent on the lateral gate biasing but on the fabrication process. According to the expression (II.6), the effective mobility is directly related to I_D current. To obtain the value of I_D for surface gate, the sidewall gate is biased with a negative voltage. As it is known that lateral gates are doped inhomogeneously and this inhomogeneous doping might be the cause of the presented phenomenon. It is also under interest to observe the evolution of the top-gate effective mobility with the transistor's dimensions. Figure 2.21 presents the characteristics for all transistor dimensions with lateral gate biasing V_{LTG} = -2V.

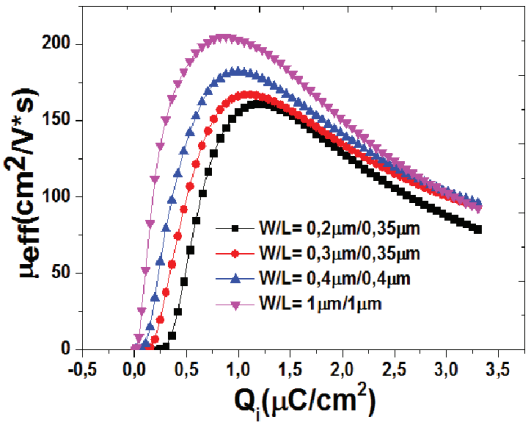


Fig. 2.21 Effective mobility function of the inversion charge for W/L = 0.2 µm/0.35 µm, W/L = 0.3 µm/0.35 µm, W/L = 0.4 µm/0.4 µm, W/L = 1 µm/1µm with V_{LTG} = -2V.

At first glance, it is clearly visible that the value of the mobility depends on the transistor dimensions. For the transistors with similar channel length L=0.35 µm, the value of the μ_{eff} is nearly the same. Moreover, it can be stated that the maximum effective mobility is increasing with the channel length. Figure 2.22 depicts the maximum effective mobility evolution with the channel length.

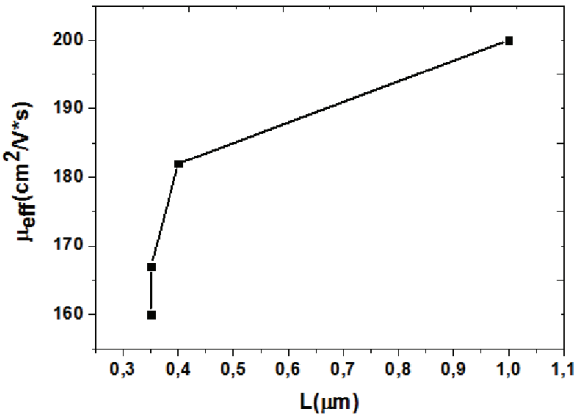


Fig. 2.22 Maximum effective mobility in function of the top gate channel length.

It is noted that the maximum mobility increases with the increase of the gate length L.

Finally, the analysis of the effective mobility curve behavior extracted with the geometrical length and effective length has been conducted. The effective channel length has been determined by TCAD simulation, as it was shown on figure 3.12A and 3.12B (Chapter 3). The transistor length influence on the effective channel mobility is verified. The extracted L_{eff} value, by TCAD simulations, has been applied with the equation II.6 for effective mobility evaluation. The extracted characteristics were compared to that, which was evaluated with geometrical transistor dimension. The extraction has been done for two values of the channel length: $L_{geom.}$, $L_{eff.}$, for V_{DS} = 0.05V. Fig. 2.23 plots the effective mobility as a function of the inversion charge Q_i.

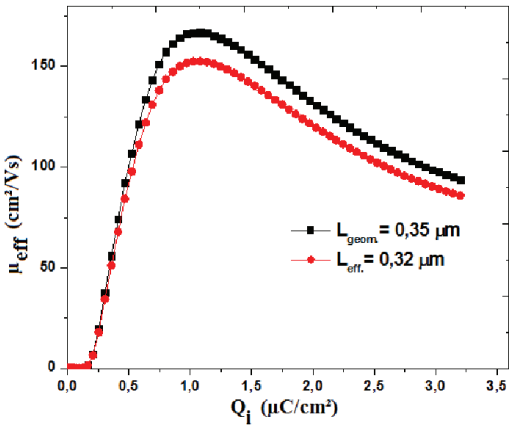


Fig. 2.23 Effective mobility extracted with L_{geom} and with L_{eff} versus inversion charge of a multi-gate device, obtained by electrical measurements (W/L = 0.3μm/0.35μm), for V_{LTG} = -2V.

The maximal value of the mobility, extracted with L_{eff}, decreases by 8.4%. Based on the equations (II.6) and (II.7), the effective mobility μ_{eff} depends on the channel dimensions, the channel-gate capacitance and the drain current. The short channel effect, discussed in 3.4.1.1, has a strong influence as well. Furthermore, the dependence of the effective mobility on the channel length might be due to the different device scattering, like surface roughness, phonon scattering and coulomb scattering. According to [18][19], the mobility degraded towards smaller dimensions of the MOSFET channel. The mobility extracted, with L_{eff} = 0.32μm at V_{DS} = 0.05 V, has a smaller value for low inversion layer (Q_i < 1.0μC/cm^2). This decrease is attributed to increase of the coulomb scattering. For Q_i > 1.0μC/cm^2, the degradation of the effective mobility is due to the surface roughness scattering [17] (linked to the collisions suffered by the electrons that are accelerated toward the interface).

2.3.1.2. Comparison between the surface gate transistor and conventional NMOSFET

Like in section 2.2, the measurements were performed on conventional MOSFET fabricated on the same wafer. Figure 2.24 depicts the capacitance – voltage characteristic comparison between the multi-gate MOSFET and conventional MOSFET, after surface and parasitic capacitance corrections.

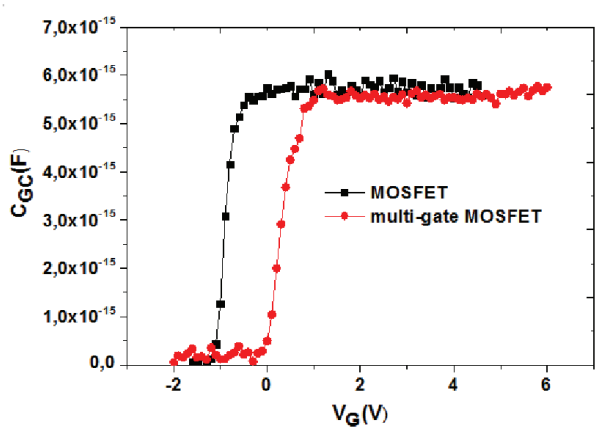


Fig. 2.24 Characteristics $C_{gc}(V_G)$ for conventional MOS (W/L = 0.38/0.28 µm) and multi-gate MOS (W/L = 0.3/0.35 µm).

To compare these two transistors, the capacitance characteristics, obtained from C-V split method, have been normalized with the effective surface of each transistor. Like the $I_D(V_G)$ characteristics (Fig. 2.7), the multi-gate transistor curve is shifted compared to the conventional MOSFET. It can be provoked by the influence of the lateral gate on the top one and the difference in doping level between these two examined transistors. The effective channel mobility, for surface gate, was determined. Figure 2.25 presents the effective electron mobility for conventional MOSFET and multi-gate MOSFET as a function of the inversion charge.

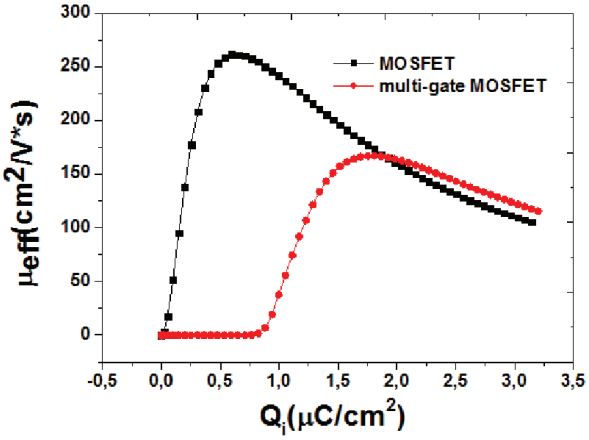


Fig. 2.25 Effective mobility versus inversion charge for conventional NMOSFET (W/L = 0.38 µm/0.28 µm), with V_G = -2V, and multi-gate device (W/L = 0.3 µm/0.35 µm), with V_{LTG} = -2V.

These curves can be considered for Q_i > 0.5 µC/cm^2 concerning the conventional NMOSFET and Q_i > 1.8 µC/cm^2 for the multi-gate NMOSFET, the multi-gate device has a slightly higher mobility compared to the conventional device. The inversion charge difference depends on their respective threshold voltage. Consequently, we can state that the multi-gate NMOSFET mobility is not degraded by the integration process of the sidewall gates. For the second part of the mobility curve (Q_i < 0.5 µC/cm^2 for the conventional transistor and Q_i < 1.8 µC/cm^2 for the multi-gate structure), the multi-gate device has a degraded mobility probably because it is more affected by defects in interface. This difference in mobility may have coordination with different values of their respective subthreshold slope.

2.3.1.3. Results for the lateral gate

To evaluate the lateral gate performances, we applied the same procedure as in the case of the top gate. First of all, the channel – gate capacitance was measured (Fig. 2.26). Comparing the extracted parasitic capacitance, we discover that lateral gate has much more important value of $C_{p,lat}$ = 2 pF, whereas the $C_{p,surf}$ = 0.35 pF, hence, its subthreshold slope is more degraded.

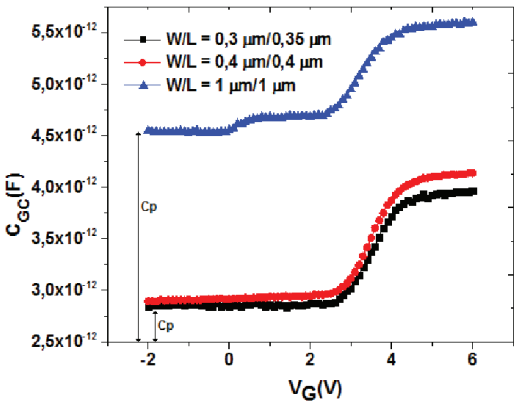


Fig. 2.26 $C_{GC}(V_G)$ characteristics for multi-gate structure W/L = 0.2 µm/0.35 µm, W/L = 0.3 µm /0.35 µm, W/L = 0.4 µm/0.4 µm, W/L = 1 µm /1 µm .

What is more, the $C_{GC}(V_G)$ curve for the multi-gate transistor with dimension W/L = 1 µm/1 µm is deformed due to, probably, the resistance in series with the source and drain region, which has a significant impact on the capacitance level. The four transistors are connected parallel. By applying the *C-V* split method, the study on effective lateral gate channel mobility was conducted. To obtain the real value of the inversion charge and effective mobility, the surface correction is mandatory. Like for the top gate, the equation II.14 is applied but the parameter S_t (transistor surface determined by channel dimension) here is defined as:

$$S_t = L * h * 2 \qquad \text{(II.14)}$$

where L signifies the channel length, h the trench height.

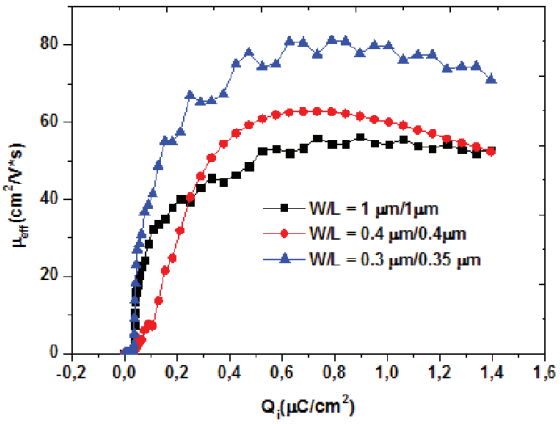


Fig. 2.27 $\mu_{eff}(Q_i)$ for V_G = -2V, W/L = 0.3 µm/0.35 µm, W/L = 0.4 µm/0.4 µm, W/L = 1 µm/1 µm.

Fig. 2.27 presents the effective mobility extracted for lateral gate transistor. The results revealed that the mobility of the lateral gate is much smaller than the top one. This phenomenon is due to the different value of the interface density, extracted by the charge pumping method in section 2.4, which is smaller for the surface gate. Additionally, the mobility decreases with increasing the transistor surface. This situation is provoked by the nonhomogeneous lateral gate doping. It is one of the differences between the lateral and surface gates.

2.4. Two- and three-level charge pumping.

The charge pumping technique is a characterization technique for determining the average density of electrically active states of the Si- insulator interface, the energy distribution and the capture cross section of these states [7].

2.4.1. Results for two – level charge pumping

The results from the two – level charge pumping method for surface and lateral gate will be presented.

2.4.1.1. Surface potential Ψ_s and flatband voltage V_{FB}

The flatband voltage V_{FB} as well as the V_{mg} voltage, which is defined as the value of the V_{GS} for $\Psi_s = \Phi_F$, have been calculated according to the method presented on figure A-5. The gate voltage for Ψ_s = 0V gives us the value of the flatband voltage V_{FB} = -0.68 V. However, from V_{GS} for $\Psi_S = \Phi_F$, we can indicate the value of V_{mg} = -0.97 V. The same analyze has been conducted for lateral gate with the results: V_{FB} = -1.78 V and V_{mg} = -0.41 V. The obtained results are crucial parameters to fix the appropriate value of the gate voltage magnitude to calculate the charge pumping current.

2.4.1.2. Charge pumping current

To calculate the charge pumping current, we have to set the parameters detected earlier (V_{FB} and V_{mg}). The signal must have the amplitude greater than V_{TH} - V_{FB} for obtaining the maximal charge pumping current. The sinusoidal signal is applied to the gate with frequency F_p = 1MHz. The measurements have been conducted on both top and lateral gates for two wafers.
First of all, the measurements have been carried out on top gate. Figure 2.28 shows the charge pumping current as a function of V_{GBI} for the surface gate

Fig. 2.28 Charge pumping current as a function of V_{GBI} (sinusoidal signal, F_p =1MHz, W/L = 0.3 µm/0.35 µm, Tox=6 nm), surface gate

The plateau of the presented characteristic represents the maximal level of charge pumping current. In fact, interface passes from accumulation state to strong inversion state; hence, defects recombination is maximal.

The studies have been done for the lateral gate as well (Fig. 2.29).

Fig. 2.29 Charge pumping current as a function of V_{GBI} (sinusoidal signal, F_p=1MHz, W/L = 0.3 µm/0.35 µm, Tox= 10.5 nm), lateral gate

Contrary to the top gate, the maximum pumping current is lower. This phenomenon could signify that the quantity of the interface defaults is more important for lateral gate. By varying V_{GB} we can probably observe the three peaks. Each of them can be consider as one of the transistor in lateral gate.

2.4.1.3. Charge pumping

The charge pumping measurement allows determining the interface density D_{it}, as well as, the average section of capture σ_{np}. The equation A.2 (Annex A) is only valid with the maximal value of the charge pumping. To carry out the measurements, it is necessary to fix V_{gl}. In order to obtain the optimal conditions, we choose the V_{gl} value corresponding to the center of the plateau: V_{gl} = -2V for top gate and 0.4V for lateral gate. Figure 2.30 presents the charge pumping as a function of the frequency in logarithmic scale.

Fig. 2.30 $Q_{cp}(log(F))$ for top gate (sinusoidal signal, F_p=1MHz, W/L = 0.3 µm/0.35 µm, Tox= 6 nm).

Equation A.7, which based on linear fitting, permits to extract the value of the D_{it}:

$$2qkTA_{eff}D_{it}\ln(10) = 3.24*10^{-16}$$

where kT = 26 meV, q = 1.6x10^{-19} C and A_{eff} = 33.21*10^{-8} cm^2 detected by C-V spit method.

The calculated value is:

$$D_{it} = 1.6*10^{9}\ \mathrm{eV^{-1}cm^{-2}}$$

The extracted value is low and it is in accordance with that observed on a good quality Si/SiO_2 interface structure.

Then based on the same equation, the average section of capture has been extracted based on the curve intercept point.

$$2qkTA_{eff}D_{it}\ln(\frac{\sigma_{np}V_t n_i Z}{2\ln(2)}) = 4.02*10^{-16}$$

The intercept equation allows detecting:

$$\frac{\sigma_{np}V_t n_i Z}{2\ln(2)} = \exp(\frac{4.02*10^{-16}}{3.24*10^{-16}}*\ln(10))$$

with n_i = 10^{10} cm^{-3}, V_t= $\sqrt[2]{\frac{3kT}{m*}}$ = 1,7 * 10^5 m/s (m* = 0,5 m$_e$)

From equation A.9 the parameter Z has been calculated:

$$Z = \arcsin\left(\frac{2\left|-0.68+0.5\right|}{0.86+2.7}\right) + \arcsin\left(\frac{2\left|-0.5-0.4\right|}{0.86+2.7}\right) = 102$$

Finally, the average capture cross section is:

$$\sigma_{np} = 8.3*10^{-17}\ \text{cm}^2$$

This value corresponds fairly well to the rough estimation, which is for cross capture section is between the 10^{-15} cm^2 and 10^{-17} cm^2.

The same analyzes have been conducted for the lateral gate.

Fig. 2.31 $Q_{cp}(log(F))$ for lateral gate for (F=1MHz, W/L = 0.3 µm/0.35 µm, Tox= 7.5 nm).

By the following steps, the exact value of the D_{it} will be evaluated.

$$2qkTA_{eff}D_{it}\ln(10) = 2.19\text{x}10^{-14}$$

where kT = 26 meV, q = 1.6x10^{-19} C and A_{eff} = 321.24x10^{-8} cm^2

The evaluated value is:

$$D_{it} = 3.6\text{x}10^{11}\ \text{eV}^{-1}\ \text{cm}^{-2}$$

The results revealed that the Si/SiO$_2$ interface structure is more degraded for lateral gate. The degradation is probably due to the fabrication process.

To calculate the effective capture section, similar procedure, like in case of top gate transistor, has been used.

$$2qkTA_{eff}D_{it}\ln\left(\frac{\sigma_{np}V_{TH}n_iZ}{2\ln(2)}\right) = 8.5x10^{-15}$$

The average capture cross section is:

$$\sigma_{np} = 2.9\text{x}10^{-17}\,\text{cm}^{-2}$$

To sum up, the effective capture sections for both gates are in similar order of magnitude, corresponding to the values obtained for dangling bond defects situated at the Si/SiO_2 interface. What is more, the increase of the charge pumping has not been observed with the frequency decrease. Therefore, all of the defects created by charge pumping were set at the Si/SiO_2 interface. There are no defects in the volume of the lateral and top gate oxide.

2.4.2. Results for three – level charge pumping

Then, three-level charge pumping method offers the possibility to determine the interface trap parameters emission times, interface trap density and energy distribution in the silicon bandgap.

2.4.2.1. Charge pumping

As it has been already explained, the principle is to probe, at first, the upper part of the band gap to observe the electron emission, then the lower for determining the hole emission. A 1 kHz pulse with third level duration, t_3, equals to 4650 ns is used to control emission of electrons and holes. The extraction of the V_{FB} and V_{mg} parameters allows determining $Q_{CP}(V_3)$ characteristic from which the emission of the electrons and holes were ascertained. Figure 2.32 shows the pumping charge function of V_3, determined by the application of the 3-level signal.

Fig. 2.32 Pumping charge as a function of the V_3 (F_p=1MHz, V_{GBl} = -2.7V, V_{GBh} = 0.86V, t_r = 5E-08, t_f = 5E-08, W/L = 0.3 μm/0.35 μm, Tox= 6 nm).

From figure 2.32, the two different measurements are distinguished, which separate the acceptors and donors. To obtain the acceptor energy distribution the variation of the electrons emission has been done. The gate was biased by the schema: $V_{GBI} \rightarrow V_{GBh} \rightarrow V_3 \rightarrow V_{GBI}$. Similar variations were executed for holes emission. Here, the gate voltage was varied as: $V_{GBh} \rightarrow V_{GBI} \rightarrow V_3 \rightarrow V_{GBh.}$ The later voltage variation gives us the donor energy distribution, which is presented as a black curve, whereas the acceptor distribution is marked in red.

Based on the equation A.13 and $\frac{dV_{GB}}{d\Psi_S}, \frac{dV_S}{d\Psi_S}$ for electron emission, the D_{it} distribution has been obtained. Figure 2.33 depicts the example of the spectra of the energy distribution of the interface states for top gate determined by the three-level charge pumping.

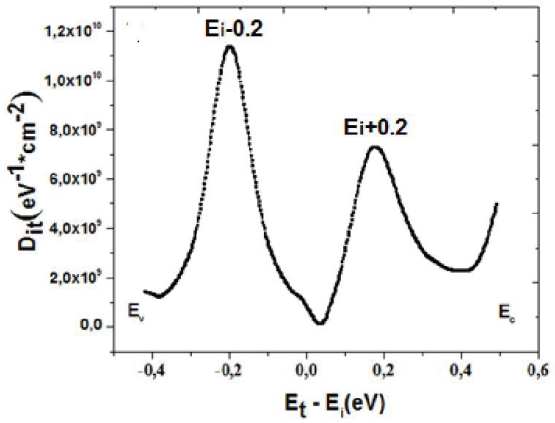


Fig. 2.33 Energy distribution of the interface traps for top gate (W/L = 0.3 µm/0.35 µm, Tox= 6 nm).

It should be mentioned that the measurements are limited to the range $[E_i - q\Phi_F; E_i + q\Phi_F]$. Hence, they are not variable close to the center of the forbidden band and close to conduction, and valence bands. As in the case of the conventional structure, there are distinctly two peaks, which exhibit the same asymmetry of distribution in the two halves on the bandgap. This characteristic distribution reveals two types of predominant traps localized at the Si/SiO_2 interface and due to the dangling bonds, with energy E_v + 0.2 eV and E_c - 0.3 eV, respectively, where E_c is the conduction-band energy and E_v the valence-band energy. What is more, the calculated value of the average density of the interface ($D_{it\_threelev.}$ = 3.6x10^9 eV^{-1} cm^{-2}) is in good accordance with the measured by two-level charge pumping since $D_{it\_twolev.}$ = 1.6x10^9 eV^{-1} cm^{-2}. The values are in the same range.

Figure 2.34 shows the energy distribution of the interface traps for lateral gate transistor.

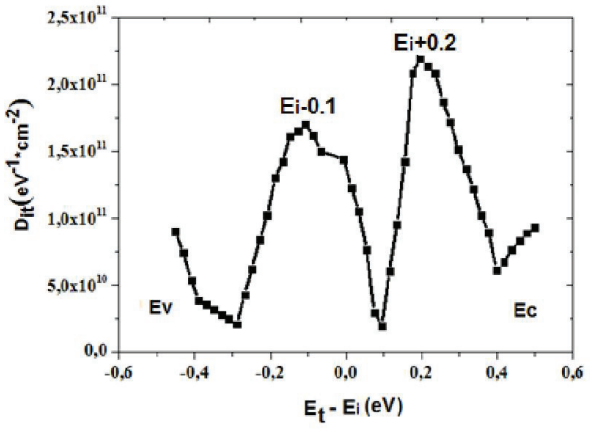


Fig. 2.34 Energy distribution of the interface traps for lateral gate (F_p=1MHz, V_{GBl} = -2.3V, V_{GBh} = 1.5V, t_r = 5E-08, t_f = 5E-08W/L = 0.3 µm/0.35 µm, Tox= 7.5 nm).

The lateral gate spectrum of the energy distribution of the interface states exhibits two peaks. As it has been already shown in section 2.4.1.3, the value of the interface density is two orders of magnitude higher in comparison to the top gate structure, due to the lateral gate trenches integration.

2.5. Conclusions

The multi-gate NMOSFET was investigated by three characterization methods: *I-V* measurements, *C-V* split methods and two- three-level charge pumping method. From current - voltage characteristics, its important parameters were verified: the threshold voltage and the subthreshold slope. The results from top gate transistor were compared with those from conventional NMOSFET fabricated on the same wafer. We observed that the top gate transistor exhibits similar electrical behavior to the conventional transistor, hence, it can be considered as a standard transistor. What is more, it was discovered that the surface gate threshold voltage is tunable with the lateral gate biasing. On the other hand, the sidewall gate transistor presents a multi-threshold behavior.

By *C-V* split method, the effective mobility was extracted. The results showed that the surface – channel electron mobility was comparable with those of the conventional n-MOSFET. With the

increase of the lateral gate biasing, the effective mobility increases. What is more, the mobility decreases with increasing the transistor surface. This situation is provoked by the nonhomogeneous lateral gate doping. It is one of the differences between the lateral and surface gates. Additionally, the maximal value of the effective mobility is much smaller for the lateral gate characteristic. This phenomenon is, probably, due to the different value of the interface density in both gates.

Finally, the average density of the Si/SiO_2 interface traps was estimated by 2-level charge pumping and then the energy distribution estimated by 3-level charge pumping. We noticed that the surface gate transistor has a higher quality channel interface than the lateral gate and its average density and energy distribution were comparable with those of the conventional NMOSFET.

To sum up, the table II-2 compares of main extracted parameters between multi-gate structure and conventional NMOSFET.

Table II-2 Comparison of all extracted results.

W/L [µm]	V_{TH} [V]	S [mV/dec]	μ_{eff} $cm^2/V*s$
Top gate of multi-gate transistor			
0.2/0.35	0.79	102	161
0.3/0.35	0.49	93	166
0.4/0.4	0.36	98	180
1/1	0.17	96	200
Lateral gate of multi-gate transistor			
0.3/0.35	1.9	180	79
0.4/0.4	2.2	120	63
1/1	2.3	155	54
conventional NMOS transistor			
0.38/0.18	0.22	80	98
0.38/0.28	0.45	83	90

To better understand the electrical behavior of multi-gate transistor and to investigate the impact of different geometrical or electrical parameters, the TCAD and SPICE simulations will be presented in chapter 3.

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3. TCAD simulations and SPICE modeling

This chapter presents studies of the multi-gate structure by both TCAD simulations and SPICE modeling. Through 2D and 3D TCAD modeling, the multi-gate transistor electrical behavior and especially its top gate characteristics were simulated and compared with results obtained by electrical measurements. The threshold voltages and the effective channel length of the multi-gate transistor have been studied. Its surface-channel low-field electron mobility and the quality of the Si/SiO_2 interface have also been investigated. The second part of this chapter concerns the SPICE analytical modeling of the multi-gate transistor. Based on the static electrical characteristics of the top and lateral gates, a preliminary SPICE model is proposed and simulation results were compared to the experimental data. This work on TCAD and SPICE modeling and simulations allows us firstly, to better understand the electrical behavior of multi-gate transistor and secondly, to investigate the impact of different geometrical (e.g. length) or electrical (e.g. interface defects) parameters on the transistor's characteristics.

3.1. Overview of the TCAD Sentaurus environment

Synopsys Sentaurus software is a suite of TCAD tools which allows basically simulating the fabrication (technological process) and/or the electrical operation of various semiconductor devices in 2 or 3 dimensions (diode, bipolar transistor, MOSFET etc.). The Sentaurus simulator uses numerous physical models to represent, for instance, different technological steps (e.g. doping atom implantation) and to determine electrical characteristics (including carrier mobility). The exploration and optimization of new semiconductor devices can be done by 2D and 3D simulation flows. What are the benefits of the TCAD simulations? Firstly, it reduces technological development time and costs. Secondly, by self-consistent multidimensional modeling capabilities, improving device design and reliability, it provides insight into advanced physical phenomena. Finally, it offers the 3D process and electrical simulation flow.
As it has been already mentioned, Sentaurus TCAD is consisting of a variety of tools. Figure 1 presents the Sentaurus TCAD suits divided according to its functionality.

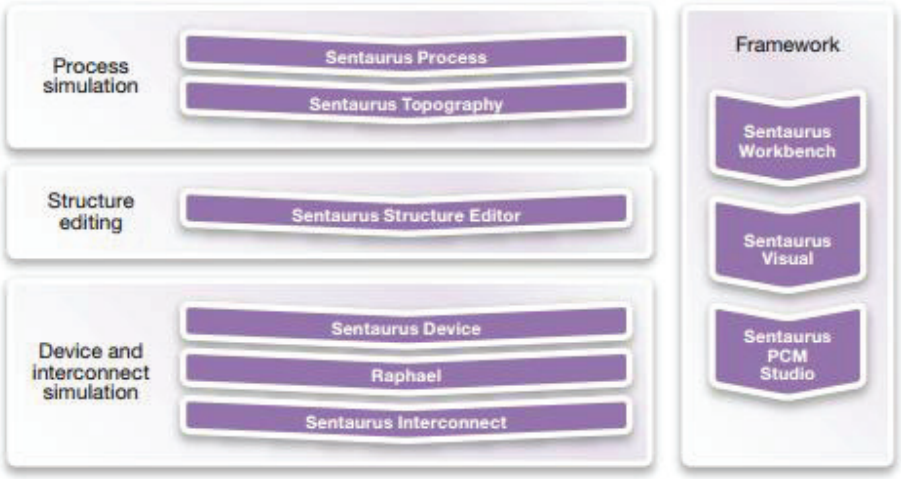


Fig. 3.1 Sentaurus TCAD suits [1].

From figure 3.1, it is possible to distinguish an overview of the different tools, thus, a short description of the most commonly used will be presented:

- Sentaurus Process allows simulating the technological fabrication steps such as implantation, diffusion, annealing, oxidation, material deposition etc. This tool was not used within in study because details of the fabrication process were not available.
- Sentaurus Structure Editor (SDE) [2] was applied to create the rendering of a multi-gate NMOS transistor structure (2 or 3D) through geometrical definitions. Then, thanks to this tool, it is possible to produce, as well, the finite-element meshes on the structure, i.e. a spatial discretization of the structure either through Delaunay grid generation or tensor-product mesh generation (suitable for axis-aligned structures and electromagnetic wave simulations). In the points of this mesh, the different physical properties can be evaluated [3] as for example the value of the junction. Sentaurus Structure Editor can be used in interactive mode (through a graphical user interface) or launched with an input text file containing script written in a specific language, describing the different geometrical forms of the structure. Due to the complexity of the multi-gate transistor, the scripted approach has been chosen for this study.
- Sentaurus Device (SDevice) [4] allows simulations of electrical, thermal and optical characteristics of silicon and compound semiconductors in 2 and 3 dimensions. Through the application of electrical potential (or current), thermal boundary at specific contacts

(electrodes), static or transient simulations can be executed. Basically for electrical simulations, the Poisson equation coupled with the drift-diffusion equations for electrons and holes will be solved for each mesh point as the voltage applied to an electrode is changing in gradual, defined steps. Solutions can be found by using the so-called Bank-Rose algorithm, which is a method of the Newton scheme used to control the latter and ensure convergence without the need to use very small steps [5].

- Sentaurus Visual [6] allows monitoring of the calculated results, such as I_D-V_{GS} characteristics in case of a MOSFET transistor. Moreover, this tools permits to know internal quantities saved at specific step such as electrical field, carrier concentrations etc. This tool enables post processing of output data to generate new curves and parameter extraction.
- Sentaurus Workbench [6] permits to manage, execute and analyze TCAD simulations. It is especially interesting for parametrical analysis.

3.2. Setup and procedure

A critical part of any simulation experiment is the creation of the structure-grid file containing the doping profiles with the associated mesh, on which the electrical simulation will be made. For this purpose, we use Sentaurus Structure Editor. Another important point is the choice and definition of the physical models to be used for the electrical simulation in SDevice. The simplest carrier transport solver has been used: Poisson and drift-diffusion equations. In this mode, the constant temperature is fixed by the user (not an electrothermal simulation) and is taken into account in various models such as carrier mobility or concentrations [4]. Among the different models associated with the chosen solver, the carrier mobility model is of utmost importance for MOSFET devices.

The mobility can be defined as the value which relates the electrons velocity with the applied electric field. This parameter depends on many quantities: electrical field (longitudinal and transversal), silicon doping concentration, the temperature (phonon scattering), interface roughness (case of MOSFET) through different sub-models that can be joined.

The total (effective) mobility is typically combined using the Mathiessen's rule:

$$\frac{1}{\mu_{total}} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \ldots \qquad \text{(III.1)}$$

where μ_1 and μ_2 are individual mobilities calculated by each model specified to be used by the simulation tool (SDevice). The mobility models set for each simulation are the Masetti [8] and Lombardi [9] models. The Masetti empirical model is for simulation of the doped silicon bulk mobility and is expressed as:

$$\mu_{dop} = \mu_{\min 1} \exp\left(-\frac{P_C}{N_{A,0} + N_{D,0}}\right) + \frac{\mu_{const} - \mu_{\min 2}}{1 + ((N_{A,0} + N_{D,0})/C_r)^{\alpha}} - \frac{\mu_1}{1 + (C_S / N_{A,0} + N_{D,0}))^{\beta}} \qquad \text{(III.2)}$$

where μ_{min1}, μ_{min2} and μ_1 are the reference mobilities. The reference doping concentration P_C, C_r, C_S and the exponents a, β are accessible in the parameter set called *DopingDependence*. The corresponding values for silicon are given in table III-1.

Table III - 1 Masetti model: Default coefficient for silicon [4].

Symbol	Parameter name	Electrons	Holes	Unit
μ_{min1}	mumin1	52.2	44.9	cm^2/Vs
μ_{min2}	mumin2	52.2	0	cm^2/Vs
μ_1	mu1	43.4	29.0	cm^2/Vs
P_c	Pc	0	9.23×10^{16}	cm^{-3}
C_r	Cr	9.68×10^{16}	2.23×10^{17}	cm^{-3}
C_s	Cs	3.43×10^{20}	6.10×10^{20}	cm^{-3}
α	alpha	0.680	0.719	1
β	beta	2.0	2.0	1

The μ_{const} signifies mobility due to phonon scattering, named constant mobility model. The constant mobility model is activated by default. It accounts only for phonon scattering and, therefore, it depends on the lattice temperature:

$$\mu_{const} = \mu_L \left(\frac{T}{300K}\right)^{-\zeta} \qquad \text{(III.3)}$$

where μ_L is the mobility due to bulk phonon scattering. The default values of μ_L and the exponent

ζ are listed in table III - 2. The constant mobility model parameters are accessible in the *ConstantMobilityparameter* set.

Table III - 2 Constant mobility model: Default coefficients for silicon [4].

Symbol	Parameter name	Electrons	Holes	Unit
μ_L	mumax	1417	470.5	cm^2/Vs
ζ	exponent	2.5	2.2	1

The Lombardi model is responsible for mobility degradation near the material interface. Mobility is degraded by carrier interaction with the semiconductor/insulator interface. Carriers are subjected to scattering by acoustic surface phonons and surface roughness. Hence, it requires a very fine mesh close to the interfaces. As a consequence, a gradual meshing strategy has been always defined in the appropriate regions like beneath the surface gate, between the lateral gates and between the source and drain. The recommended maximal meshing distance near the interface is 0.1 nm.

3.3. 2D simulations

In the chapter 2 – Electrical characterizations, it has been proved that the values of electrical properties like subthreshold slope (S), threshold voltage (V_{TH}) of the top gate transistor of multi-gate structure are not degraded compared to the conventional structure. For the classical structure the S = 83 mV/dec and V_{TH} = 0.4 V whereas the values for multi-gate structure are S = 90 mV/dec and V_{TH} = 0.45 V. To sum up the multi-gate structure behaves like its conventional counterpart. Therefore, the first simulations have been carried out on the 2D structure, which was defined for the L/W of the top gate of the multi-gate structure and its conventional counterpart. The aim of these simulations was to define and verify all of the 2D parameters to create the proper 3D multi-gate NMOSFET structure in a second step. In this way, the goal was to match the threshold voltage and the *I-V* curves with varying the doping level under the gate and the mobility model and parameters. Other transistor technological parameters have been taken from previous work [10].

The 2D structure of the NMOSFET transistor was created in order to fit the simulated results with the measurements for the top gate of the multi-gate transistor and conventional NMOS transistor. To start with, the definition of the tools utilized on Sentaurus Workbench was created in the right order. For instance, the Sentaurus Structure Editor (SDE) is before the Sentaurus Device (SDevice), firstly to draw the structure, define the doping profiles, electrodes and the grid ("meshing") before performing electrical simulations of the structure. Figure 3.2 presents the screenshot of Sentaurus workbench with a parametrical approach to investigating the impact of technological parameters (e.g. doping level).

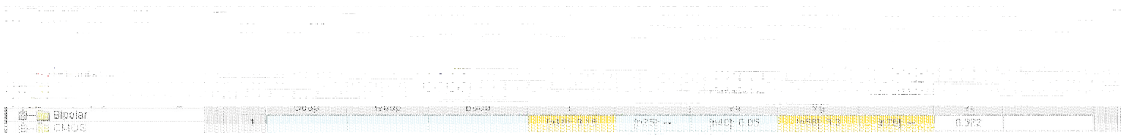


Fig. 3.2 Screenshot of the Sentaurus workbench for NMOS transistor simulation with used tools.

It is possible, as shown, in figure 3.2, that the bulk doping concentration can vary, in order to find a similar value of the threshold voltage to the measured one. This basic extraction will then allow us to simulate different parameters, using a more complex and comprehensive model like 3D, on these structures. What is more, the yellows nodes indicate the successful steps.

In Sentaurus Structure Editor, a NMOSFET conventional structure has been designed. The

objective of these studies was to create a model, similar possible to that presented in section 1.5. The doped polysilicon gate was defined. The substrate was made of p – type silicon and there was an oxide layer thickness (T_{ox}) of 6 nm between the gate and the bulk. The spacers were fabricated by Si_3N_4 deposition. The parameters declared, herein, are G_{dop}, W_{dop}, B_{dop} and L, representing, respectively, the depth of the Gaussian N-well doping profile in μm, the donor concentration (p doping) of the gate and wells, the acceptor (p doping) concentration of the bulk. Finally, L signifies the gate length. Figures 3.3A and 3.3B depict the 2-D simulated structure.

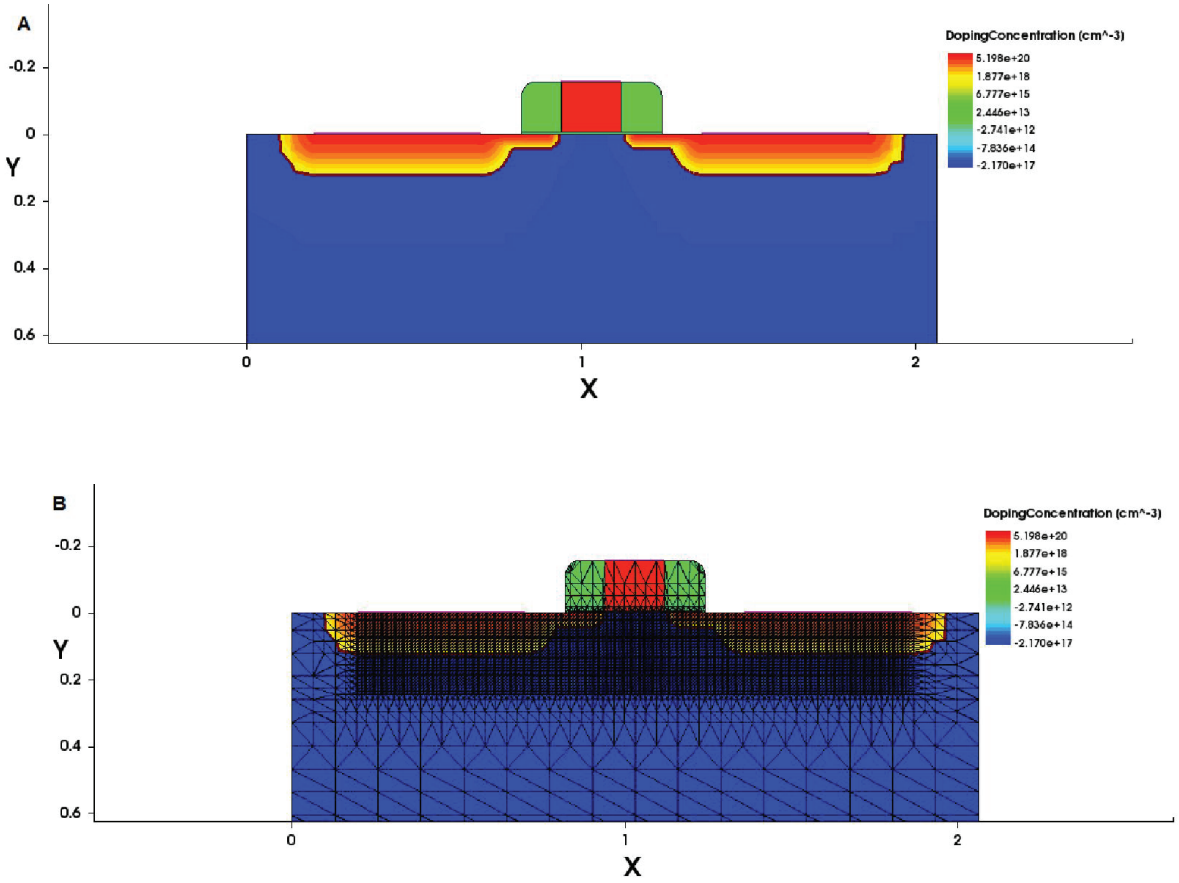


Fig. 3.3 Simulated conventional NMOS transistor with (A) doping profiles and (B) visible mesh.

From figure 3.3B, it is noticeable that the mesh is extremely fine in the channel region and in the source and drain, so as to obtain the most accurate simulation. The length of the channel is varying between 0.35 μm and 1.05 μm. The source and drain are simulated with active arsenic Gaussian doping profiles with a peak concentration of $2.6x10^{-20}$ cm^{-3} at the surface and a concentration of $2.6x10^{17}$ cm^{-3} at a depth of 0.12 μm and 0.4 μm for main wells and the

extensions under the spacers, respectively. The bulk has a constant active boron concentration of $3.05x10^{17}$ cm^{-3}, and the polycrystalline Silicon gate has a constant active arsenic concentration of $2.6x10^{20}$ cm^{-3}. The drain voltage is increased in a ramp from 0V to 0.05V before the gate voltage ramp from 0V to 3.3V is applied. The steps of the simulations increase from 0.001V to 0.05V by a factor of 1.3 at each increment.

3.3.1. Results

As already mentioned, the 2D simulation has been launched for the conventional NMOS transistor to validate the model and find the appropriate value of the substrate doping in the channel region. The objective of this analysis is to obtain a good coherence between measurements and simulations to determine parameters for 3D simulations.

The first step was to find the same threshold voltage as that obtained by measurements. For each transistor dimension, the changes of the value of substrate doping were done. The initial value of the substrate doping was 10^{15} cm^{-3}. The figure 3.4 presents the threshold value V_{TH} as a function of substrate doping (supposed to be uniform), obtained by TCAD simulation.

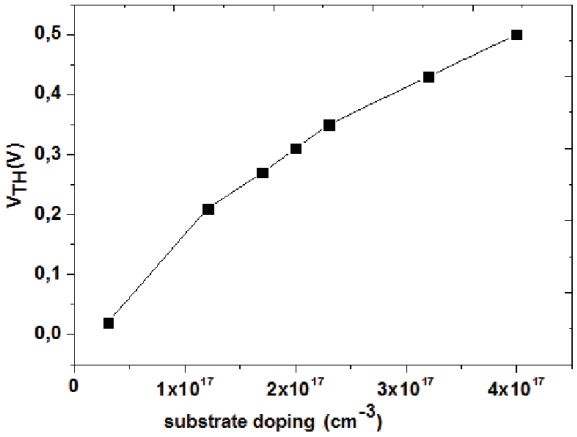


Fig. 3.4 Threshold voltage in function of the substrate doping for conventional transistor with dimension L=0.18 µm.

From the simulations, the value of the V_{TH} = 0.40V for conventional transistor with dimension L=0.35 µm has been simulated. The substrate doping level value has been found on characteristic presented on figure 3.4 and corresponds to B_{dop} = $3x10^{17}$ cm^{-3}. Thus, our studies revealed that, for B_{dop} = $3x10^{17}$ cm^{-3}, the best coherence between the measurements and simulations can be obtained. Fig. 3.5 shows the simulated surface-gate I_D-V_{GS} characteristics (at low V_{DS}=50mV, in

linear scale) of a multi-gate NMOSFET transistor (only top gate) for different gate lengths with V_{LTG} = -2V. The I_D-V_{GS} curves of the results from measurements are also plotted in Fig. 3.5 for comparison.

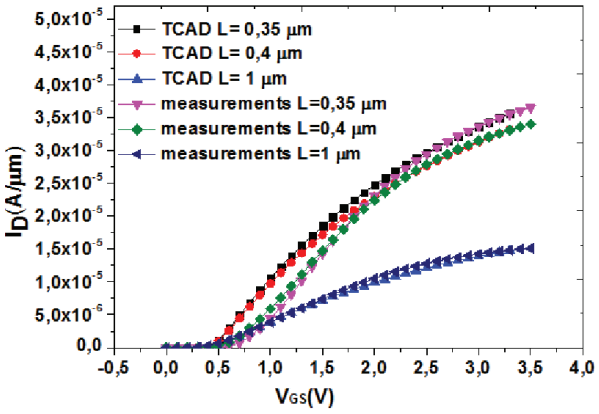


Fig. 3.5 I_D-V_{GS} 2D simulation TCAD characteristics (in linear scale) of multi-gate NMOS transistor (L= 0.35, 0.4, 1 µm) and its measured counterparts for V_{LTG} = -2V, with V_{DS} = 50 mV and V_{BS} = 0 V.

There is as well a small discrepancy in threshold voltage between simulated and calculated varying the transistor gate length. The more important difference in threshold voltage value is obtained for L=0.4 µm. From simulation, V_{TH}=0.53V was evaluated compared to V_{TH}=0.63V obtained by measurements. Figure 3.6 shows the observed trend of the variation for the threshold voltage as a function of the gate length.

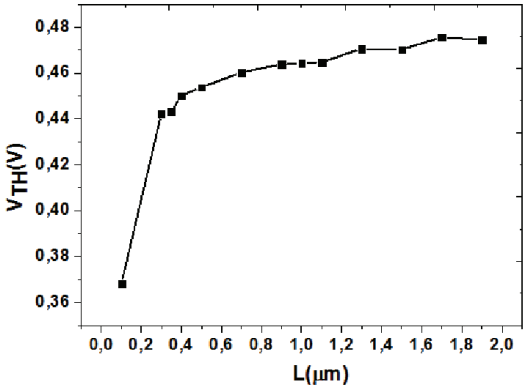


Fig. 3.6 Threshold voltage versus length of the top gate, for L varies between 0.18 µm up to 2.0 µm (2D simulations).

It is worth noticed that for all simulation runs, the threshold voltage calibration has been done for the first result (for 0.18 µm) on the conventional structure, before increasing the gate length by steps of 0.05 µm. Figure 3.6 shows that the threshold voltage decreases with the decrease of the channel length. Here, it exhibits one of the limitations of the scaled MOSFET, called the Short Channel Effect (SCE) that is linked to the lowering of the barrier while decreasing the channel length, furthermore this phenomena is exacerbated with the Drain Induced Barrier Lowering (DIBL) for high V_{DS} values. These effects are particularly pronounced in lightly doped substrates. In very short channel devices, part of the depletion is accomplished by the drain and source bias. Since less gate voltage is required to deplete Q_D, the barrier for electron injection from source to drain decreases. SCE results in increasing drain current at a given V_{GS} and decreasing V_{TH} with decrease of L. Figure 3.7 presents the $I_D(V_{GS})$ characteristics in logarithmic scale, from which the subthreshold slopes have been extracted.

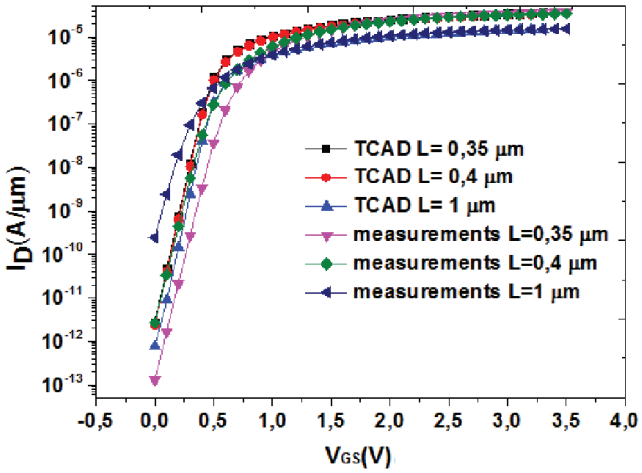


Fig. 3.7 I_D-V_G 2D simulation TCAD characteristics (in logarithmic scale) of multi-gate NMOS transistor (L= 0.35, 0.4, 1 µm) and its measured counterparts for V_{LTG} = -2V, with V_{DS} = 50 mV and V_{BS} = 0 V.

The presented characteristics exhibit very good accordance in current level. Nevertheless, there are clearly visible disproportions in the subthreshold slopes. Table III - 3 presents extracted values of the subthreshold slopes for various transistor sizes.

Table III - 3 Subthreshold slope values extracted from 2D simulations and comparisons to measurements.

	Measured value	Simulated result
L [µm]	S [mV/dec]	S[mV/dec]
0.35	90	80
0.4	90	88
1	80	90

From table III-3, it is possible to notice that there is not a significant discrepancy between measured and simulated subthreshold slopes. Nevertheless, this visible disproportion can be easily explained. The simulations were conducted without donors and acceptors traps in the gate oxide or Si/SiO_2 interface. The value of the subthreshold slope depends on the interface traps density [11].

Finally, the influence of the constant mobility, which is integrated in Sentaurus model, on the drain current was evaluated. These studies have been conducted only for one dimension of the transistor with length: L= 0.4 µm.

The initial value (value defined in Sentaurus model) of the μ_L is 1417 $cm^2/V*s$ (Table III - 2). The best mobility value for current adjustment was achieved for L = 0.4 µm and we obtained μ_L = 1500 $cm^2/V*s$. Table III - 4 presents the results of these studies.

Table III - 4 Mobility correction.

	Measured value	Without mobility correction	After mobility correction
L [µm]	Id_{max} [A/µm]	Id_{max} [A/µm]	Id_{max} [A/µm]
0.4	$3.38x10^{-5}$	$3.27\ x10^{-5}$	$3.36x10^{-5}$

The relative error between the electrical measurements and simulations without mobility correction is 4% whereas with the mobility corrections are 2%. Thanks to this mobility correction analysis, we noticed that the mobility parameter μ_L does not require a significant correction, thus, for further analyzes, the initial value of the maximal mobility has been kept.

3.4. 3D simulations

Based on the 2D model and 2D simulations results, the full 3D multi-gate NMOS transistor structure has been created. The main aim was to generate the 3D multi-gate structure to simulate and analyze the influence of the lateral gate on the creation of the surface channel. Fig. 3.8 presents the 3D simulated structure.

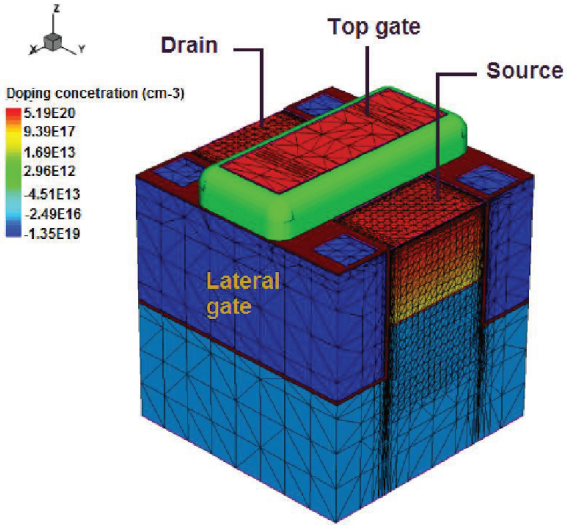


Fig. 3.8 The sketch of 3D structure with doping profiles and visible mesh.

The following points indicate the simulation setup:

- Source and Drain: Active Arsenic Gaussian doping profiles with a peak concentration of $2.6x10^{20}$ cm^{-3} at the surface and a concentration of $2.6x10^{17}$ cm^{-3} in the volume (n-doping),
- Lateral gates polysilicon: Active Boron constant profiles with a concentration of $9.8x10^{18}$ cm^{-3} (p-doping),
- Surface gate polysilicon: Active Arsenic constant profile with a concentration of $2.6x10^{20}$ cm^{-3} (n-doping),
- Bulk/substrate: Active Boron Gaussian profile with a concentration from 3.05 x 10^{17} cm^{-3} at the surface to 10^{15} cm^{-3} in the volume, under the top gate oxide (p-doping).

Picture 3.9 shows the cross-section along Y axis which presents the substrate gradual doping, whereas, the figure 3.10 has been directly extracted from TCAD and presents substrate doping concentration function of the substrate depth (vertical cut-line along Z axis).

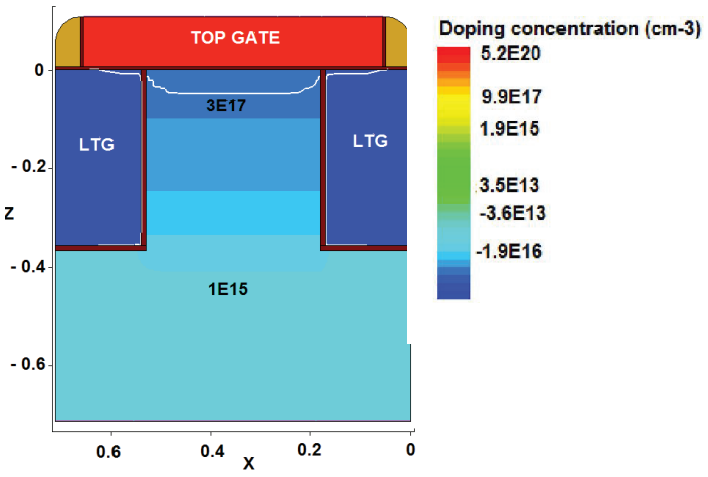


Fig. 3.9 Cross-section through Z axis (see Fig.3.8) which presents the substrate gradual doping (red = n doping, blue = p doping)

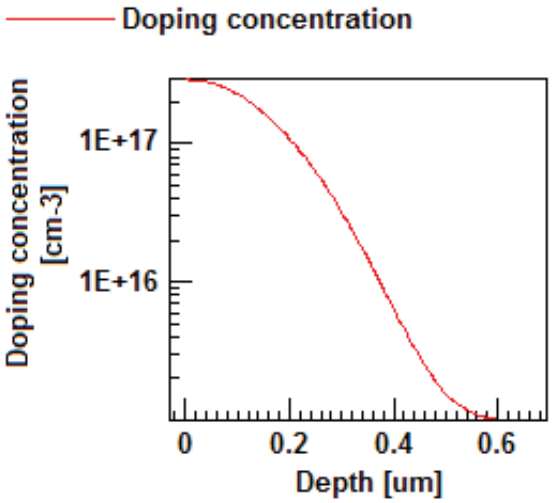


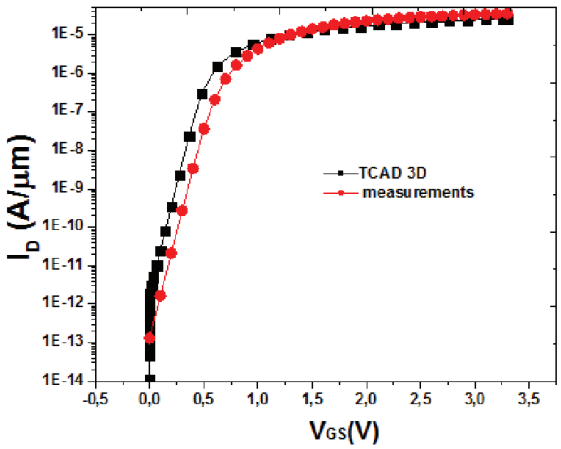
Fig. 3.10 Substrate p-doping concentration function of the substrate depth.

3.4.1. Results

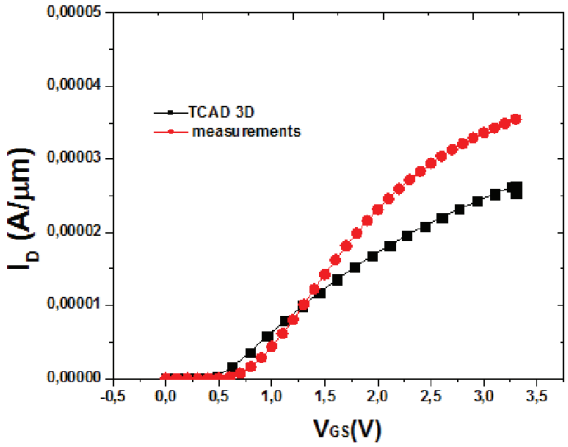
In this section, the simulated results for the top gate and lateral gate transistor are presented. Firstly, the current – voltage characteristics will be considered. Then, the effective mobility as well as the SiO_2/Si interface quality will be analyzed. The obtained simulated results are compared to its measurements counterpart.

3.4.1.1. *$I_D(V_{GS})$ static characteristics*

The current – voltage characteristics have been extracted from 3D simulations for top gate transistor. Both simulations have been done with substrate doping (under the top gate) B_{dop} = $3x10^{17}$ cm^{-3} (this specific value was estimated from the 2D simulations in previous section). Figures 3.11A and 3.11B compare the *I-V* characteristics between 3D simulations and measurements. To compare these characteristics, drain current density is plotted in A/µm (i.e. drain current divided by the transistor width).



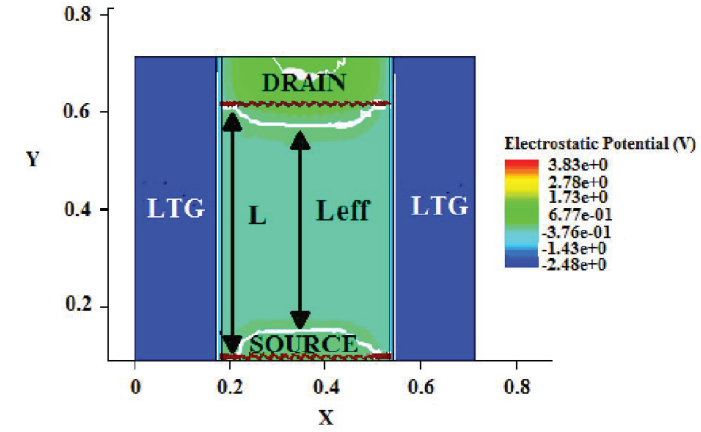
(A)



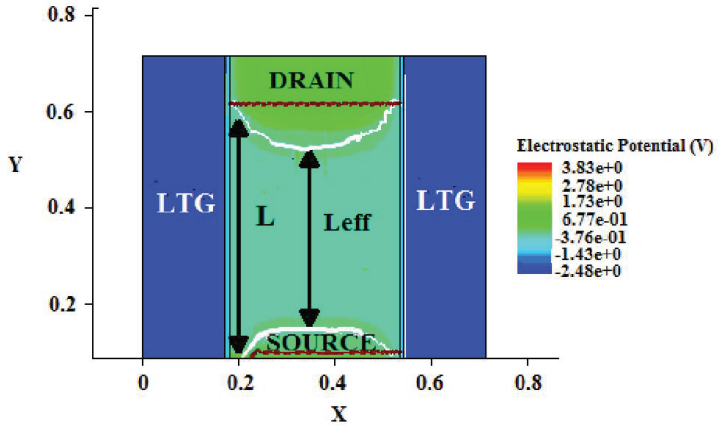
(B)

Fig. 3.11 I_D-V_{GS} 3D TCAD simulated characteristics, in logarithmic scale (A) and linear scale (B), of the top gate transistor (W/L = 0.3µm/0.35µm) and its measured counterparts for V_{LTG} = -2V, with V_{DS} = 50mV and V_{BS} = 0V.

The threshold voltage extracted from measurements, by using Hamer method (see section 2.1.2), is slightly higher (V_{TH} = 0.59V) compared to the 3D simulated one (V_{TH} = 0.5V). This discrepancy might be caused by lack of interface traps in the model used in TCAD simulation. The subthreshold slope extracted from the measurements is 89 mV/dec compared with 90mV/dec obtained by the simulations. Considering Fig. 3.11b in linear scale, it is noticeable that the difference in the value of the measured and simulated threshold voltage is slightly visible. For the 3D simulations, the three gates (top gate and two lateral gates) have been taken into account. The channel dimensions have a strong influence on the device performances. By executing the TCAD simulations, the effective length of the device has been extracted. It is influenced by the Gaussian doping profile in the lateral direction. Usually, it is calculated as the difference between the source/bulk and drain/bulk depleted junction distance. Figures 3.11A and 3.11B show the electrostatic potential below the top gate for a small drain-source voltage (V_{DS} = 50mV) and an important value (V_{DS} = 1V), which is $V_{DS} > V_{DSsat}$, where V_{DSsat} signifies the drain – source voltage bias at saturation.



(A)



(B)

Fig. 3.12 Electrostatic potential below the top gate for V_{DS}=50mV (A), and for V_{DS}=1V (B). Both simulations have been conducted under following conditions: V_{LTG}=-2V, V_{BS}=0V.

The obtained effective gate length value for MOS W/L = 0.3µm/0.35µm is equal to L_{eff} = 0.32µm at V_{DS} = 50mV. However, for V_{DS} = 1V, the effective length is smaller, with L_{eff} = 0.26µm. When the source - drain voltage increases beyond the saturation, the neighboring area of the drain is no longer in inversion regime. The pinch point moves towards to the source. The voltage that exceeded V_{DSsat} has spread across depletion area. Hence, the relative variation of the channel length is important and the channel length is decreasing while increasing V_{DS}. This study provides us with the information how much the effective channel length differs from the designed values. The V_{DS} increase leads to decrease of the effective channel length as it has been proved by

experiments. Considering the 2D and 3D simulated $I_D - V_{GS}$ characteristics, it was noticed that the threshold voltage slightly deviates between them, which is due to the corner effect [12]. In the upper corners of the region (Fig. 3.12), the electric field is much more important. Thus, the electron charge density will be high. However, in the lower corners the value of the charge density is small.

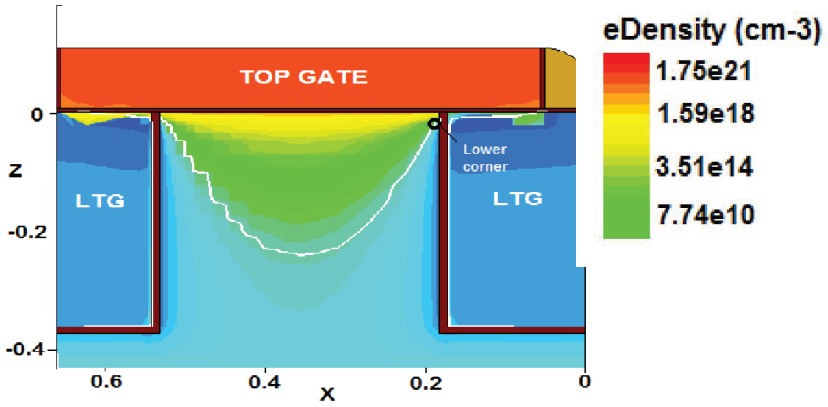


Fig. 3.13 Electron density (and corner effect) in cross section of the multi-gate structure.

The current voltage characteristics have been as well extracted for lateral gate transistor. The simulations have been conducted for negative surface gate biasing V_G = -2V and positive lateral gate biasing V_{LTG} = 4V. Figure 3.14 shows the results of these studies.

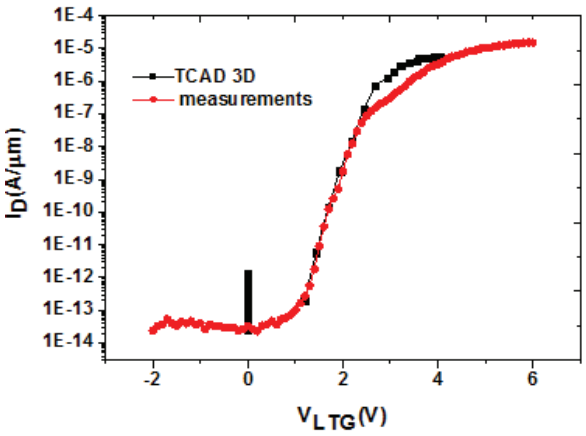


Fig. 3.14 I_D-V_{GS} 3D TCAD simulated characteristics, in logarithmic scale of the lateral gate transistor (W/L = 0.3µm/0.35µm) and its measured counterparts for V_G= -2V,with V_{DS} = 50mV and V_{BS} = 0V.

Although, the "bumps" have not been obtained, the simulated *I-V* characteristic coincides to measured one. The significant error between the measured current level and simulated is about 8%.

3.4.1.2. *SiO_2/Si interface quality*

The trap formation at the Si-SiO_2 interface in MOSFET devices is considered to be an important mechanism of device degradation [13]. The impact of trap's presence has become an issue for CMOS circuitry, shifting the drive current and the threshold voltage of the devices [14]. The current – voltage characteristics were simulated by introducing the interface traps with Gaussian distribution. These studies led us to investigate the degradation mechanism of the drain current in multi-gate NMOSFET transistor. By two and three-level charge pumping techniques explained in Annex A, the interface state density has already been studied. From two-level charge pumping measurements on the surface gate, the average interface state density $D_{it} = 3.9\text{x}10^{9}$ $eV^{-1}cm^{-2}$ and the capture cross section $\sigma = 9.45\text{x}10^{-17}cm^{2}$ have been obtained. Then, three-level charge pumping measurements allowed us to obtain the interface traps energy distribution in the silicon bandgap.

This characteristic distribution reveals two types of predominant traps localized at the Si/SiO_2 interface (Fig. 2.33, section 2.4.2.1). The donor-like traps has $D_{it} = 1.13\text{x}10^{10}eV^{-1}cm^{-2}$ whereas acceptor-like traps has $D_{it} = 7.27\text{x}10^{9}eV^{-1}cm^{-2}$. Initially, current – voltage curve is calculated at a low drain bias V_{DS} = 0.05V. To conduct the degradation simulation, the value of the average density of the interface states, which have been extracted by measurements, are applied.

The simulated I_D-V_G characteristics are plotted on Fig. 3.15, where the impact of donor-like and acceptor-like interface traps distribution is compared with measurements and TCAD $I_D(V_G)$ characteristic without traps injection.

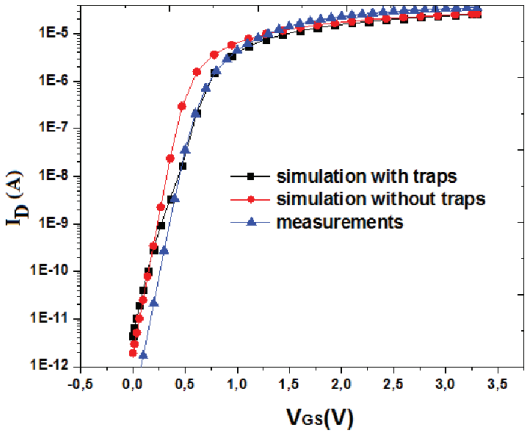


Fig. 3.15 I_D-V_G transfer characteristic 3D TCAD simulation of multi-gate NMOS transistor (L=0.35µm) with traps injection, without and it measured counterpart for V_{LTG} = -2V with V_{DS} = 50mV and V_{BS} = 0V.

Figure 3.15 presents the impact of the interface traps distribution on threshold voltage. The deviation is observed on the subthreshold slope, for a small value of gate voltage, which is degraded about 11% to its measured counterpart. What is more, the threshold voltage shift, between the characteristics with and without traps, is discerned due to the positively charged donor traps and negatively charged acceptor traps. To understand the influence of the observed phenomenon, the donor- and acceptor-like traps concentrations have been separately simulated.

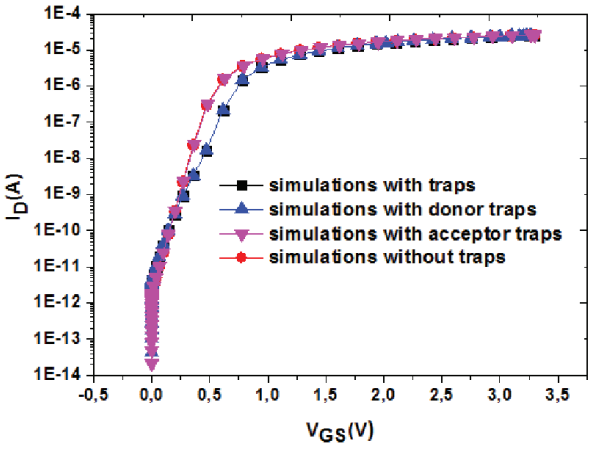


Fig. 3.16 I_D-V_G transfer characteristic 3D TCAD simulation of multi-gate NMOS transistor (L = 0.35µm) with traps injection, without and the only donor- and acceptor-like simulations for V_{LTG} = -2V with V_{DS} = 50mV and V_{BS} = 0V.

From figure 3.16, it is noticed that the injected donor traps have a more important influence on the current-voltage characteristics than acceptor-like one. A little degradation is observed when the I_D current reaches the value of 0.016mA. As the drain current increases, the Fermi level sweeps the highest part of the interface traps distribution within the bandgap. The meaningful amount of the donor traps stay positively charged which may occur in subthreshold slope degradation, observed on Fig. 3.15.

3.4.1.3. *Electron channel mobility*

The extraction of the electron channel mobility has been executed, based on simulation results. The electron channel mobility is defined as the sum of all mobility models (according to the Mathiessen rule) applied to the modeled structure (see section1.4). The studies were carried out from the smallest transistor length L=0.35 µm to the largest one with L=1 µm, for comparison. Figure 3.17 presents the cross-section through Y axis presenting the electron mobility distribution. The lines C1, C2, C3 represent the section where the electron mobility has been extracted.

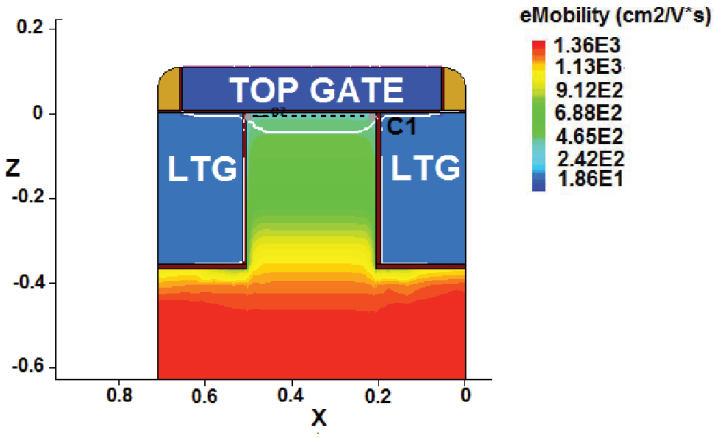


Fig. 3.17 Electron mobility distribution in top gate channel for L = 0.35 µm.

The simulated effective electron mobility through the channel is presented in figure 3.18.

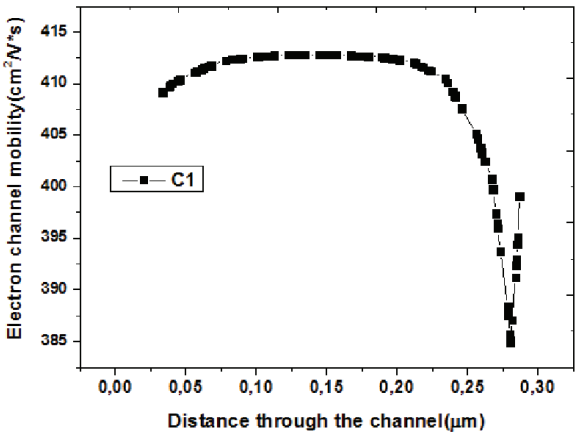


Fig. 3.18 Electron channel mobility through the top gate channel dimension for L= 0.35 μm.

Below the top gate, the mobility value is μ_e = 417 cm^2/V*s. Similar evaluation has been conducted for a transistor with channel length L = 1 μm (Figures 3.19 and 3.20).

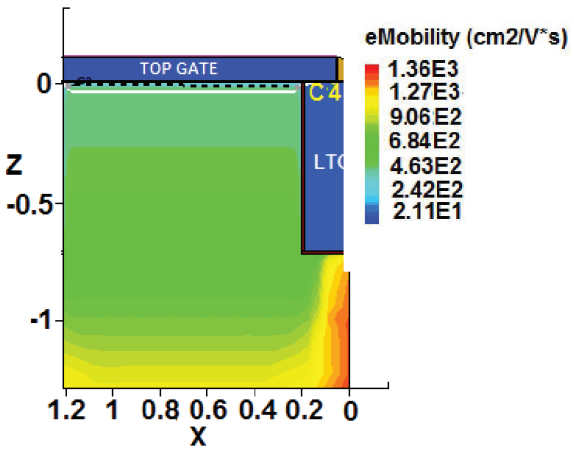


Fig. 3.19 Electron mobility distribution in top gate channel for L= 1 μm.

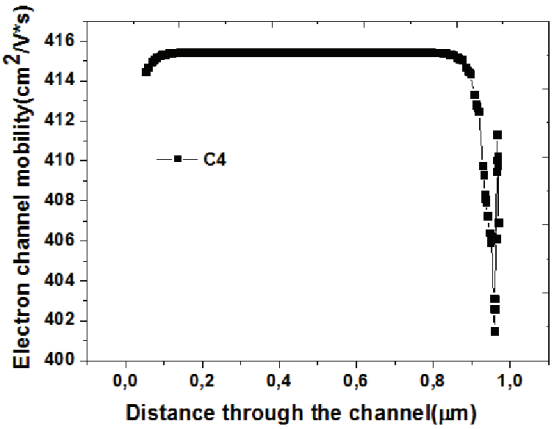


Fig. 3.20 Electron channel mobility through the top gate channel dimension for L= 1 µm.

For the structure with channel L = 1µm, the mobility level through the channel is more uniform with the maximal value equals μ_e = 415 cm^2/V*s. The obtained value is in the same range as those evaluated from the transistor with dimension L = 0.35 µm (Figs. 3.17 & 3.18). Therefore, based on these analyzes, the electron channel mobility in the structure of the multi-gate NMOS transistor is about 430 cm^2/V*s, which is slightly two times greater to the effective mobility extracted in section 2.3.1.1. This phenomenon can be explained by equation III.5 [15]:

$$\mu_{eff} = \frac{\mu_e}{1 + \Theta * V_p} \qquad \text{(III.5)}$$

where parameter Θ typically ranges between 0.1 and 0.5, and V_p is pinch off voltage, defined as: $V_p = V_{GS} - V_{DS}$. The pinch off voltage is almost a linear function of gate voltage. The electron channel mobility is proportional to the effective mobility, hence, with increase of the electron mobility the effective mobility increases as well.

To complete the studies, the electron channel mobility extracted by TCAD simulations has been compared with the effective channel mobility, obtained from electrical measurements, for each transistor width. To obtain the similar measurements conditions, the interface traps density has been injected to the surface gate: we use $D_{it} = 3.9 \times 10^9 eV^{-1}cm^{-2}$ for interface trap density and $\sigma = 9.45 \times 10^{-17}$ cm^2 for the capture cross section. To proceed analyze, the effective channel mobility and electron channel mobility in function of the transistor width was traced for comparison (Fig. 3.21).

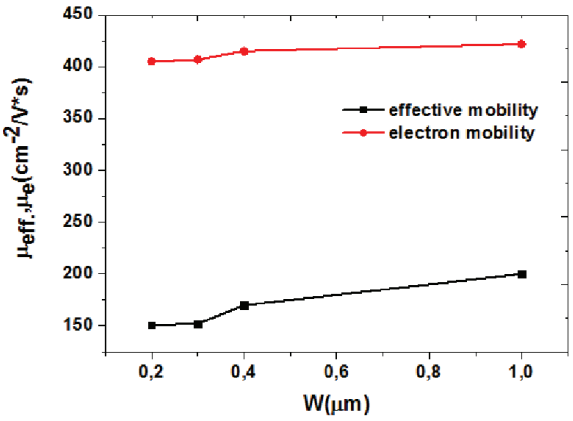


Fig. 3.21 Effective (extracted by *C-V* split method) and electron channel mobility versus transistor width.

The figure shows that both effective and electron channel mobility exhibits the same tendency. The mobility value increases with the increase of the channel width.

For the lateral gate the analogous tendency has been observed, the electron channel mobility is much more important than the effective mobility. What is more, the value of the electron mobility is not constant. The value of the mobility increase linear in function of the lateral gate channel length (see Fig. 3.23). This phenomenon is due to gradual substrate doping.

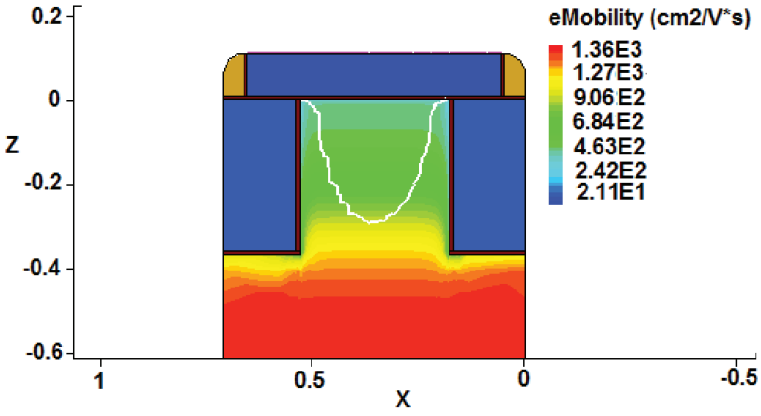


Fig. 3.22 Electron mobility distribution in lateral gate channel for L = 0.35 μm.

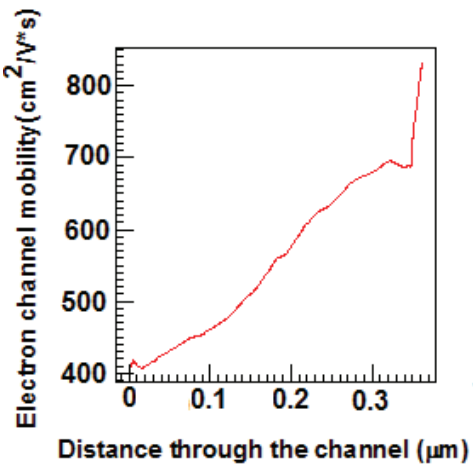


Fig. 3.23 Electron mobility distribution through the lateral gate channel for L = 0.35 μm.

3.5. SPICE drain current modeling

The objective of these studies was to obtain similar drain current level to its measured counterpart. The SPICE simulations have been applied to continuation of parameter extraction. SPICE became popular because it contained the analyses and models needed to design integrated circuits of the time, and was robust enough and fast enough to be practical to apply [16]. This simulator combined operating point solutions, transient analysis, and various small-signal analyses with the circuit elements and device models needed to successfully simulate many circuits. Due to the lower simulations time comparing to the TCAD simulations and variety of the different available analyzes the validations of already obtained results and applications perform much more quickly. Based on the superposition principle, the SPICE simulations have been firstly conducted on top gate, then on the lateral gate. Finally, the basic application (logic gate OR) has been carried out. To do these analyzes the proper model on each structure had to be created. The modeling parameters for semiconductor devices such as MOSFET, bipolar transistor or diode are contained in the part of the netlist called a MODEL statement. All of the simulations have been done in Level 3 [17] spice model. In comparison to BSIM models [18], this one characterizes the simplicity in its application. Although, the models created at the Berkley University are more precise, at the same time they are more time-consuming in understanding its concept. The main aim was to validate rapidly the obtained results and potential application. Thus, the Level 3 model fulfilled these requirements on the best way. Moreover, regarding the accuracy of the model, it is possible to specify if the additional devices with other dimensions are needed to better fit the model. The lateral gate of this device presents multiple (three) threshold-voltage behavior of the current-voltage characteristic (chapter 2, section 2.2.4 – 2.2.5). The lateral gate can be modeled by considering, in parallel, three source-drain-connected equivalent transistors with different threshold voltages and sizes. In contrast to lateral gate, the top gate performs as a conventional one. Finally, the proposed equivalent SPICE model for the multi-gate transistor is composed of four transistors in parallel (one for the top gate and three for the laterals gate featuring multiple threshold-voltages). By adjusting the different parameters of the SPICE model on the various transistor components, the multi-gate MOSFET characteristic can be correctly reproduced.

3.5.1. Surface gate model

As it has been already mentioned, the objective of these studies was to obtain the similar drain current level to its measured counterpart. Firstly, the Level 3 MOSFET model [17] of a transistor was applied for surface gate transistor modeling. In the SPICE model of NMOS transistor, to model I_D, we kept the following parameters of the SPICE model : *NSUB*, *TOX*, *VTO*, where *NSUB* is substrate doping corresponds to value $3x10^{17}$ cm^{-3}, *TOX* signifies oxide thickness (*TOX* = 6 nm) and *VTO* is zero – bias threshold voltage. The adjustment has been processed on transconductance parameter KP expressed as [A/V^2]. This parameter can be defined, basically, as the ratio between *Cox* and μ_o and it was determined step by step.

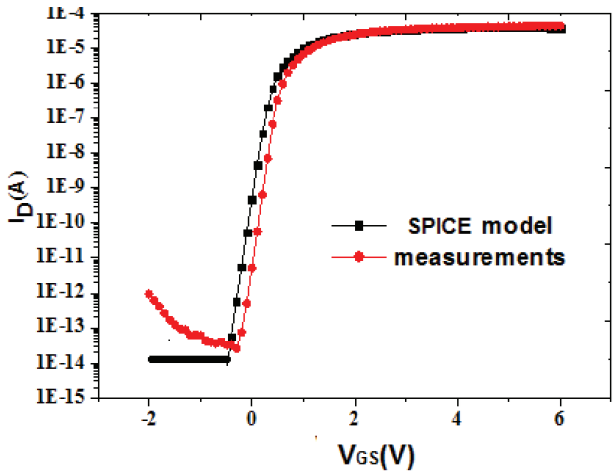


Fig. 3.24 $I_D(V_{LTG})$ SPICE model and measurements characteristics for W/L = 0.3 µm/0.35 µm, V_{DS}=50mV, V_G=-2V, V_{BS} = 0V.

Figure 3.24 shows the comparison of the current – voltage characteristics between measurements and SPICE simulation. The current level extracted by SPICE simulation is in the same level to that obtained from measurements. Hence, the created model reflects the reality. The code of the SPICE top gate model is attached in the Annex B.

3.5.2. Lateral gate model

For the lateral gate, there are three channels connected in parallel, between the source drain, featuring the multiple threshold-voltages. To reproduce this effect, three parallel NMOS transistors, controlled by the same gate and drain voltages, have been modeled. The presented model in Fig. 3.25 is representing the transistors associated to the lateral gate, which is modeled with three different transistors. The lateral gate model is based on the same model than for the surface gate. The width and threshold voltage of these three transistors, with KP, are the parameters to adjust to fit with measurement.

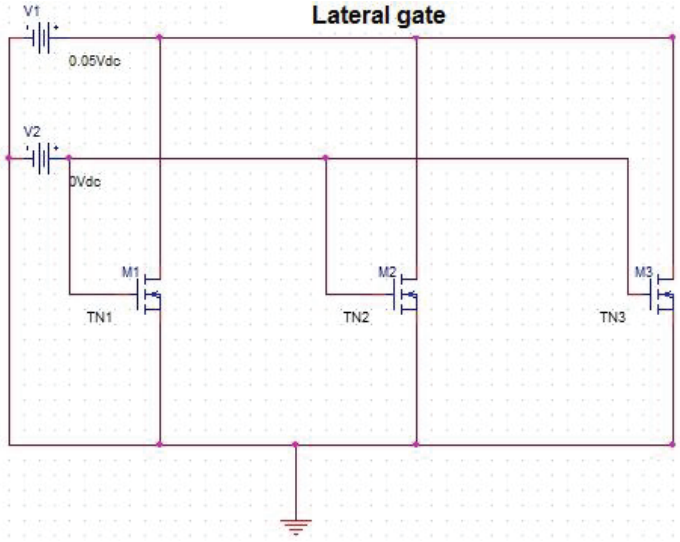


Fig. 3.25 Schematic of the lateral gate structure equivalent model.

Like in the cases of measurements and TCAD simulation, the lateral gate has been activated by varying positive bias V_{LTG} up to 6V (Fig. 3.26) on lateral gate and negative V_G= - 2V on top gate. What is more, all lateral gate transistors share the same oxide thickness (TOX = 7.5x10^{-9} µm), substrate doping ($NSUB$ = 3x10^{17} cm^{-3}), channel length L=0.35 µm. The channel width (W), process parameter (KP) and transistors threshold voltage (V_{TH}) are the adjusted parameters. The parameter KP can be adjusted to find the similar current level as that extracted from measurements. According to the equation (III.6), for the lateral gate, it is possible to distinguish

three transistors with different threshold voltages and width dimensions. Hence, the total drain current is a sum of these three transistors' drain currents, and is expressed as:

$$I_D = I_{D1} + I_{D2} + I_{D3} \qquad \text{(III.6)}$$

The figure 3.26 compares SPICE simulated results with measured ones, W/L = 0.32 µm/0.35 µm.

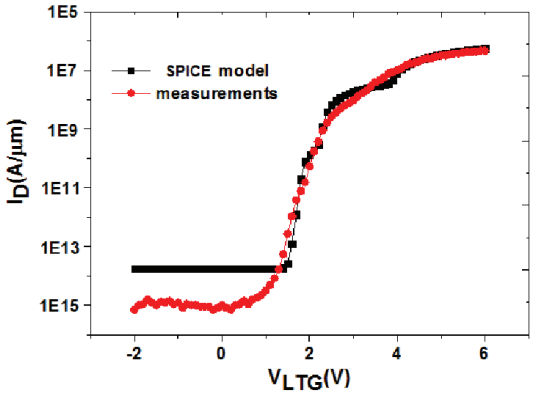


Fig. 3.26 $I_D(V_{LTG})$ SPICE model and measurements characteristics for W_L/L = 0.32 µm/0.35 µm, V_{DS}=50mV, V_G = -2V.

The characteristic simulated by SPICE exhibits three different "bumps" as what was observed in measurements. These "bumps" correspond to threshold voltages and transistor widths. By adjusting the threshold voltage to obtain the similar curve to the measured one and applying the length of the lateral gate the width of the each transistor have been determined. For lateral gate transistor the total width (W_L) depends on the each transistor width, thus the equation (III.7) can be formulated:

$$W_L = W_1 + W_2 + W_3 = 2*h = 0.32\ \mu m \qquad \text{(III.7)}$$

Table III - 5 presents the results of the extraction.

Table III - 5 Results of the extraction for W_L/L = 0.32 µm/0.35 µm.

Transistor*	$W_{1,2,3}$ [m]	V_{TH} [V]
TN1	$3.31x10^{-7}$	3.5V
TN2	$1.82x10^{-8}$	2.2V
TN3	$9.9x10^{-11}$	1.8V

* the terms TN1, TN2, TN3 signify the transistors in lateral gate presented on figure 3.20.

Based on the extracted result and equation (III.8) the lateral gate transistor width has been calculated W_L = 0.3 µm, compared to the standard value (W_L = 0.32 µm). Thus, the relative error is only 6,25 %. Summing up the table III - 5, it can be seen that the channel width extracted for TN3 model is very small, even unrealistic. The discrepancy of the threshold voltage value can be caused by the local redistribution of boron doping, in the bulk/oxide gate interface and lateral gate isolation respectively. This phenomenon is due to the segregation coefficient of boron which is smaller for Si/SiO_2 interface. The code of the simulated model is presented in Annex C.

3.6. Conclusion

In a first part, the top gate of the multi-gate NMOSFET transistor was investigated by 2D & 3D TCAD electrical simulations (Sentaurus platform). At first, the 2D model was built adjusting the doping under the gate to fit the experimental threshold voltage. Afterwards, the 3D model was constructed for advanced analysis of the multi-gate transistor. Its important electrical features were verified: the top-gate threshold voltage of 0.59V, the subthreshold slope around 90mV/dec and the effective length of the multi-gate NMOS channel. Its effective mobility was extracted for the geometrical and the effective channel length. The electron channel mobility has been extracted, as well, for transistors with length L = 0.35 µm and L= 1 µm. The results revealed that, for both transistors, the obtained mobility is in the same range, μ_{tot} = 430 $cm^2/V*s$. The extraction of the average density of the Si/SiO_2 interface traps and its impact on current-voltage characteristics were executed. The injected donor traps have a larger influence on the current-voltage characteristics than acceptor-like one. Results were compared with the measurements

pointing out a good Si/SiO_2 interface quality at the top gate.

In a second part of this chapter, an equivalent SPICE model of the multi-gate transistor was proposed. This model is based on different transistors in parallel representing the conducting paths along the top gate and the lateral gates with multiple threshold voltages. Firstly, the top gate model has been developed. Afterwards, the lateral gate transistor has been modeled with three transistors in parallel with different internal parameters. By fitting the Spice simulations to experimental data, the lateral gate threshold voltage and lateral gate transistor width have been adjusted. These parameters permitted to reconstruct the lateral gate characteristic with three humps associated to three threshold voltages.

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4. Conclusion

The aim of this thesis was to study a multi-gate NMOS transistor realized by the integration of polysilicon-filled trenches in a conventional 120 nm bulk CMOS process. To perform it, the electrical characterizations and TCAD simulations are realized and results are analyzed and compared to the state of the art. Presented in chapters two (measurements) and three (simulations), the main results can be summarized as follows.

First of all, static *I-V* measurements were performed on the multi-gate NMOSFET and conventional MOSFET. From measured *I–V* characteristics, it is possible to extract some key parameters, such as the threshold voltage (V_{TH}), the subthreshold slope (S). To determine threshold voltage both Hamer method (section 2.1.2) and Y function method (section 2.1.1) were employed. The studies of the subthreshold slope showed that the obtained value for the top gate of the multi-gate NMOS transistor is S = 93 mV/dec and it is relatively higher that which was determined for the conventional MOSFET (S = 83 mV/dec). The extraction of the surface gate threshold voltage has been preceded as well. Despite of the small difference in the evaluated results between the Hamer method (V_{TH} = 0.68V) and Y function method (V_{TH} = 0.64V), the clear tendency has been observed. Thus, the lowering of the sidewall gate bias leads to an increase in the surface gate threshold. This threshold – tunable feature can be particularly useful for applications involving design of novel circuits and system. Finally, it has been noticed that the multi-gate device has a slightly higher mobility compared to the conventional device. The relative estimation has been carried out between the surface gate and lateral gate transistor too. The measurements revealed that the lateral gate *I-V* characteristic exhibits a multi – threshold behavior that can be modeled from three channels in parallel. Additionally, the effective mobility of lateral gate is significantly higher compared to the surface gate transistor. This phenomenon is due to the different value of the interface density

By *C–V* split method, the effective channel mobility of the top gate transistor has been calculated and compared to the value extracted from conventional one. The studies revealed that the multi-gate NMOSFET mobility is not degraded by the integration of polysilicon trenches. Nevertheless, at the same time, the top gate transistor is affected by the defects at the interface. Comparing the lateral gate with top gate one, the effective mobility value of the sidewall gate transistor is much

smaller to its top gate counterpart.

The two – and three – level charge pumping technique allows extracting the density of interface traps (D_{it}) the Si/SiO_2 interface. The evaluated value from 3-level charge pumping measurements was in good accordance with measured value using 2-level charge pumping measurements ($D_{itcal.}$ = $1.6x10^9$ $eV^{-1}cm^{-2}$ and $D_{itmeas.}$ = $3.6x10^9$ $eV^{-1}cm^{-2}$). What is more, the studies revealed that the top gate transistor interface has a higher quality interface that the lateral gate transistor.

Chapter three showed the studies of the multi-gate structure by both TCAD and SPICE modeling and simulations. The results from simulations were compared with results obtained from electrical measurements. Moreover, by 2D &3D TCAD simulations, the important electrical features were verified. At first, the 2D model was built adjusting the doping under the gate to fit the experimental threshold voltage. Afterwards, the 3D model was constructed for advanced analysis of the multi-gate transistor. Its important electrical features were verified: the top-gate threshold voltage of 0.59V, the subthreshold slope around 90mV/dec and the effective length of the multi-gate NMOS channel. The results revealed that, for both transistors, the obtained electron mobility is in the same range, μ_{tot} = 430 $cm^2/V*s$. The analyze of the average density of interface traps at the Si/SiO_2 interface and its impact on current-voltage characteristics were executed. Results were compared with the measurements pointing out a good Si/SiO_2 interface quality at the top gate.

In the second part of chapter three, an equivalent SPICE model of the multi-gate transistor was proposed. This model is based on different transistors in parallel representing the conducting paths along the top gate and the lateral gates with multiple threshold voltages. Firstly, the top gate model has been developed. Afterwards, the lateral gate transistor has been modeled with three transistors in parallel with different internal parameters. By fitting the PSpice simulations to experimental data, the lateral gate threshold voltage and lateral gate transistor width have been adjusted. These parameters permitted to reconstruct the lateral gate characteristic with three bumps associated to three threshold voltages. Having both proper models, the whole structure has been reconstructed. The PSpice simulations have been launched and match correctly the measured electrical characteristics of the multi-gate transistor.

Last but not least, there is still space left for further investigations. Having the additional samples of the investigated structure the noise and temperature analyzes could be conducted. With our proposed compact model of multi-gate MOSFET, the next step will be enhancing the lateral gate

transistor model in order to obtain the proper *I-V* characteristic. The ameliorated model can be applied in the logic circuit.

Based on the results evaluated from electrical characterizations and TCAD simulations, it is possible to conduct the dynamic analyze of MOSFET transistor in order to propose a complete VHDL-AMS model. Then, DC analyze will allow for get to know the power consumption and its limits, while the transient analyze will show the instability of the circuit as well as the overloads and short-circuits. By developing all of the mentioned points, it is possible to create, with the multi-gate NMOSFET structure, analog circuits, such as amplifiers or voltage controlled oscillator.

Annex A

Principle of the two-level charge pumping.

The charge pumping method is used to characterize interface traps densities in MOS transistors for the evaluation of MOSFET degradation. It can be used for gate oxide thinner than 2 nm [1] In 1969 Jesper and Brugler [2] reported a net DC substrate current generated by applying periodic pulse to the gate of a MOS transistor, keeping source and drain grounded. This current originates from recombination of minority and majority carriers at traps localized at the Si/SiO_2 interface. The observed current has been named the charge pumping current. The section below will explain the principle of the charge pumping technique.

Basic principle of the charge pumping.

The basic experimental setup for the charge pumping method can be seen in figure A-1 for a conventional n-channel MOSFET. The source and drain to substrate diodes are reverse biased.

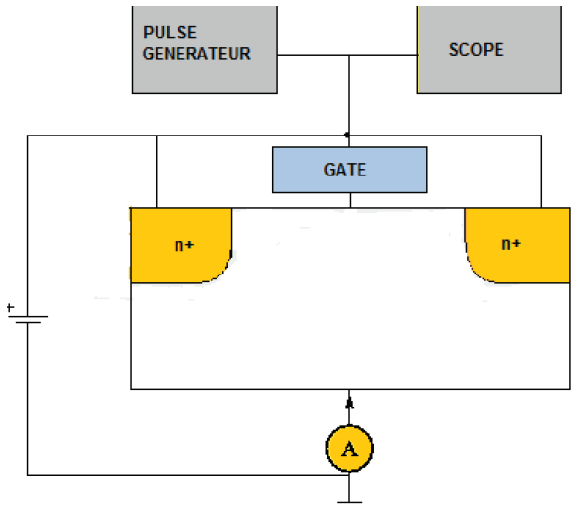

Fig.A-1 Experimental setup for the charge pumping measurement.

The source to substrate and drain to substrate diodes are typically slightly reverse biased, while the gate is pulsed between inversion and accumulation modes. The substrate current is measured as the charge pumping current I_{CP}. The gate is pulsed between an accumulation and an inversion condition while the charge pumping current is measured at the substrate electrode. This current flows in the opposite direction of the source and drain to substrate diode leakage currents. The majority carriers in accumulation phase, holes in case of an n-channel MOSFET, flow through the channel area and some of them become trapped in interface traps. When the gate pulse drives the transistor into inversion mode, the majority of the carriers leaves the channel and gets back to the substrate. Some trapped carriers, with energies close to the valence band, can be de-trapped through thermal emission before the channel becomes filling by electrons and also move back to the substrate. The rest of the trapped holes recombines with channel electrons and leads to a net current. The same process occurs when the transistor is driven from inversion back to accumulation mode, with opposite carrier types as depicted on figures A-2 and A-3.

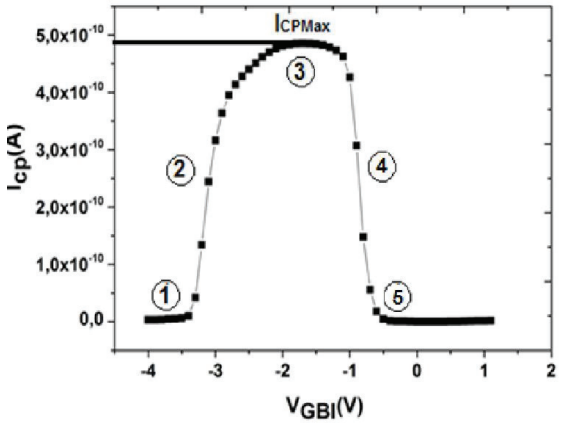

Fig.A-2 Representation of characteristic $Icp(V_{GBl})$ with V_{GB} const.

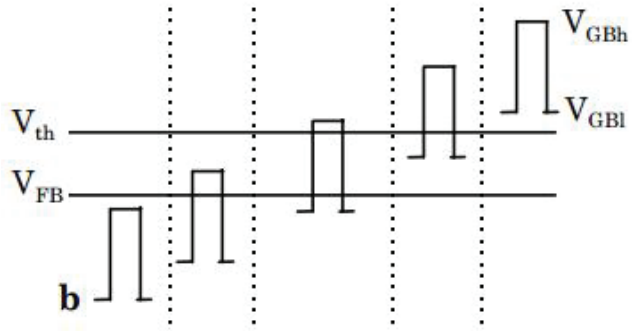

Fig.A-3 presents the position of the surface gate channel relative to V_{FB} and V_{TH}.

The base level sweep charge pumping method was first proposed by Elliot [3] and the different regimes are governed by the following mechanisms:

Phase 1

The whole pulse is below the flatband voltage and the substrate is in permanent accumulation state. The interface traps are permanently filled with holes and therefore semiconductor is always in accumulation mode, because of lack of the recombination between electrons, holes and traps there is no charge pumping current.

Phase 2

The top of the pulse reaches the region between the flatband and the threshold voltages. In this phase, the interface is moved from accumulation into strong depletion up to weak inversion. Here, the charge pumping current increases and the base voltage is around the threshold voltage minus the pulse height. It could be assumed that the shape of the rising in this regime is determined by the recombination process in weak inversion. It has been shown, though, that other mechanisms may have an important influence. These can be the surface potential fluctuations because of spatially non-uniformly distributed oxide charges [3], acceptor and donor traps [4], or variations in the proximity of the source and drain regions. Also the modulation of the effective gate area by the gate voltage might influence the rising charge pumping current.

Phase 3

The base level voltage is below the flatband voltage, and the top level of the pulse is above the threshold voltage. In this regime, the charge pumping pulse sweeps the substrate in the channel area from accumulation to complete inversion mode. At each time, the transistor is pulsed from accumulation to inversion or back. The fast interface traps are filled with holes, or electrons, respectively, which then recombine with the opposite carrier type leading to a net current measurable. In this regime the current has the highest magnitude, as it is shown in equation A.1:

$$I_{cp} = F_p A_{eff} q D_{it} \Delta\Psi_s \qquad \text{(A.1)}$$

where F_p is the signal frequency (1MHz in our case), A_{eff} the effective channel area, q the elementary charge, D_{it} the interface density and $\Delta\Psi s$ signifies bandgap probe.

Phase 4

The base level is between the flatband and threshold voltages. The transistor only reaches weak accumulation, the interface traps are mainly negatively charged and are no longer flooded with holes, thus recombination are reduced and the charge pumping current goes down.

Phase 5

The transistor is completely in inversion during the whole pulse. The traps are filled with electrons and no holes reach the channel at any time. The measured substrate current only consists of the source and drain leakage currents.

Three-level charge pumping

The three - level charge pumping method was first announced by Tseng [5] in 1987. In contrary to the two-level charge pumping method, this allows to determine the parameters like energy distribution and average density of the interface in more precise and quantitative way. What is more, Autran [6] discovered that based on this method it is possible to extract effective capture in the forbidden band of the semiconductor structure. Figure A-4 shows the signal waveform applied in three-level charge pumping.

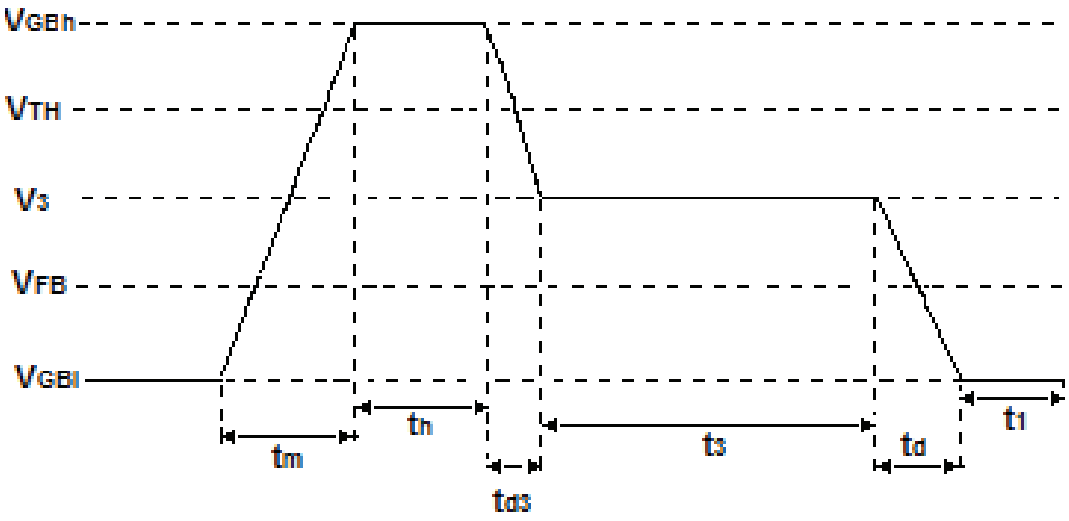

Fig.A-4 Waveform used in three-level charge pumping with step voltage on trailing edge.

To illustrate all of the phenomena occurring in this method, the showed waveform in Fig. A-4 will be explained. In addition to the voltage above the threshold voltage and the flatband voltage, a third voltage, called V_3, is introduced, according to the following expression:

$$V_{FB} < V_3 < V_{TH} \tag{A.2}$$

The new voltage level takes part in the sweep between the strong inversion and accumulation. Firstly, the pulsed V_{GB} voltage will be applied, where $V_{GB} = V_{GBI}$. Therefore, the structure is in accumulation regime. The energy level is smaller to the Fermi level, hence, all of the interface states are occupied. Then, the V_{GB} voltage is applied according to $V_{GBI}<V_{GB}<V_{GBem,h}$. In this situation, traps are filled by emission of holes in equilibrium and non-equilibrium regimes. The pulsed voltage is increased and $V_{GBem,h}<V_{GB}<V_{GBh}$ in the conduction band are presented the electrons captures which fill the traps. The next level is when $V_{GB}=V_{GBH}$, the structure is in the strong inversion and all of the traps whose energy level is below the Fermi level are filled. The state V_3 is activate for $V_3<V_{GB}<V_{GBh}$. During times t_{d3} and t_3, the interface states are emptied by electron mission. If the duration of the t_3 is sufficiently long, the charging function E_m catches the Fermi level E_F or energy level E_3. The traps located above the level of energy E_3 are empty. The electron flux passes between the interface and drain junction, and source junction. The current intensity is shown as:

$$I_{cp_1} = F_p A_{eff} q \int_{E_s}^{E_{Fh}} D_{it}(E) dE \tag{A.3}$$

For $V_{GBI}<V_{GB}<V_3$, the structure changes in accumulation regime. The capture of the empty holes is visible in the interface. The holes current which flows between the bulk and interface is calculated by equation (A.4):

$$I_{cp_2} = -F_p A_{eff} q \int_{E_{Fi}}^{E_S} D_{it}(E) dE \tag{A.4}$$

The charge pumping current is the sum of the equations (A.3) and (A.4):

$$I_{cp} = F_p A_{eff} q \int_{E_s}^{E_{em,h}} D_{it}(E) dE \tag{A.5}$$

whereas the V_3 variations, as well as the interval $[E_{em,h}, E_3]$, allow to determine the energy distribution of the interface states.

Extraction methods

The aim of this paragraph is to explain the methods used to determine the interface density (D_{it}), as well as, its effective section capture. To start with, we will present the methods and results from two - level charge pumping. Then, the same analyze will be conduct for three-level charge pumping.

Two-level charge pumping (interface density and effective capture section)

The average capture section σ_{np}, is defined by:

$$\sigma_{np} = \sqrt{\sigma_n * \sigma_p} \tag{A.6}$$

where σ_n and σ_p are respectively the effective section for electrons and holes .

Based on the charge pumping current (equation A.5), the pump charge is expressed as:

$$Q_{cp} = \frac{I_{cp}}{F_p} = 2qkTA_{eff}D_{it}\ \ln\left(\frac{\sigma_{np}V_{TH}n_i Z}{2\ln(2)\pi F_p}\right) \tag{A.7}$$

with σ_{np} signifies the geometric average capture section for electrons and holes captures.

Equation A.7 can be written, as well, in another form:

$$-Q_{cp} = \frac{I_{cp}}{F_p} = 2qkTA_{eff}D_{it}\left[\ln(10)\log(F_p) - \ln\left(\frac{\sigma_{np}V_{TH}n_i Z}{2\ln(2)\pi}\right)\right] \tag{A.8}$$

where the parameter Z is defined as:

$$Z = \arcsin\left(\frac{2|V_{FB} - V_o|}{V_{GBh} - V_{GBl}}\right) + \arcsin\left(\frac{2|V_o - V_{TH}|}{V_{GBh} - V_{GBl}}\right) \tag{A.9}$$

The characteristic -*Qcp* function of the log(*Fp*) allows obtaining the linear characteristic. From its slope the extraction of the average density can be done. Moreover, the effective capture section of electrons and holes can be determined by the curve extrapolation.

Three-level charge pumping (energy distribution of the interface states)

For determining the energy distribution of the interface traps, we need to link the density of the interface states with the energy E_3, introduced by the 3-level charge pumping. Firstly, we related the E_3 with surface potential Ψ_3 by the following equation:

$$E_3 = E_i + q(\Psi_3 - \Phi_F) \tag{A.10}$$

where E_i is intrinsic energy, Φ_F signifies the Fermi potential, q is simply the electron charge. Now, the expression of the pumping current is presented as:

$$I_{cp} = F_p A_{eff} q \int_{E_i + q(\Psi_S - \Phi_F)}^{E_{em,h}} D_{it}(E) dE \tag{A.11}$$

Based on the equation II.24 and deriving equation II.25, the D_{it} is calculated:

$$D_{it}(\Psi_3) = \frac{1}{q^2 A_{eff} F_p} \left| \frac{dI_{CP}}{d\Psi_S} \right| \tag{A.12}$$

To calculate the density of the interface states, we need to know the value of the relation $\frac{dI_{CP}}{d\Psi_S}$.

This relation can be directly determined from surface potential function of the gate voltage characteristic.

The variation of the surface potential function of the gate voltage is shown on figure A-5.

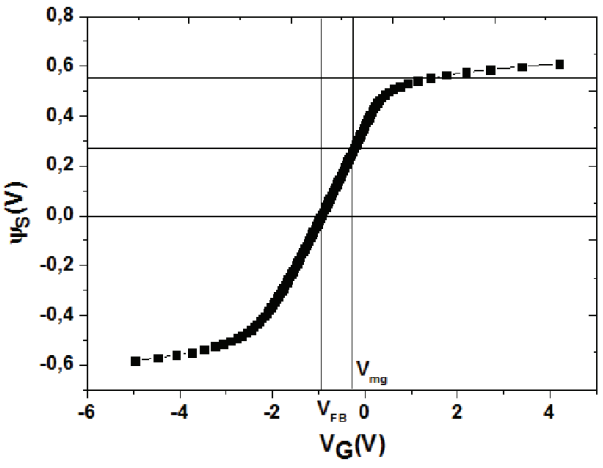

Fig.A-5 $\Psi_s(V_{GB})$ characteristics determined from I_D-V_G measurements (W/L = 0.3 µm/0.35 µm).

The characteristic from Fig. A-5 will be derived and the relation $\frac{dV_{GB}}{d\Psi_S}$ will be obtained.

It is considered as equal to $\frac{dV_S}{d\Psi_S}$. Therefore, equation A.12 is transformed as:

$$D_{it}(\Psi_3) = \frac{1}{qA_{eff}F_p}\left|\frac{dI_{CP}}{dV_G}\right|\frac{dVs}{d\Psi_S} \qquad \text{(A.13)}$$

From figure A-5, the flatband voltage V_{FB} as well as the V_{mg} voltage (V_{GS} for $\Psi_S = \Phi_F$) can be determined.

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Annex B

Size (W/L= 0.3 µm/ 0.35 µm)

.MODEL Mbreakn NMOS LEVEL = 3
+ TOX = 60E-10 NSUB = 3E17 GAMMA = 0.5
+ PHI = 0.7 VTO = 0.49 DELTA = 3.0
+ UO = 650 ETA = 3.0E-6 THETA = 0.1
+ KP = 67E-6 VMAX = 1E5
KAPPA = 0.3
+ RSH = 0 NFS = 1E12 TPG = 1
+ XJ = 500E-9 LD = 100E-9
+ CGDO = 1.44E-10 CGSO = 1.44E-10 CGBO = 1.73E-9
+ CJ = 1.175E-3 PB = 1 MJ = 0.5
+ CJSW = 0 MJSW = 0.5 CBD=1E-14

Size (W/L= 0.4 µm/0.4 µm)

.MODEL Mbreakn NMOS LEVEL = 3
+ TOX = 60E-10 NSUB = 3E17 GAMMA = 0.5
+ PHI = 0.7 VTO = 0.36 DELTA = 3.0
+ UO = 650 ETA = 3.0E-6 THETA = 0.1
+ KP = 68E-6 VMAX = 1E5 KAPPA = 0.3
+ RSH = 0 NFS = 1E12 TPG = 1
+ XJ = 500E-9 LD = 100E-9
+ CGDO = 200E-12 CGSO = 200E-12 CGBO = 1E-10
+ CJ = 400E-6 PB = 1 MJ = 0.5
+ CJSW = 300E-12 MJSW = 0.5

Size (W/L= 1 µm/1 µm)

.MODEL Mbreakn NMOS LEVEL = 3
+ TOX = 60E-10 NSUB = 3E17 GAMMA = 0.5
+ PHI = 0.7 VTO = 0.2 DELTA = 3.0
+ UO = 650 ETA = 3.0E-6 THETA = 0.1
+ KP = 102E-6 VMAX = 1E5 KAPPA = 0.3
+ RSH = 0 NFS = 1E12 TPG = 1
+ XJ = 500E-9 LD = 100E-9
+ CGDO = 200E-12 CGSO = 200E-12 CGBO = 1E-10
+ CJ = 400E-6 PB = 1 MJ = 0.5
+ CJSW = 300E-12 MJSW = 0.5

Annex C

Size (W/L = 0.3 µm/0.35 µm)

```
.model TN1 NMOS LEVEL=3
+TOX=7.5E-9 NSUB=1E17
GAMMA=0.5827871
+PHI=0.9  VTO=3.4  DELTA=0
+UO=205  ETA=0  THETA=0.1749684
+KP=4.264274331E-5
VMAX=8.309444E4  KAPPA=0.2574081
+RSH=0.0559398  NFS=1E12  TPG=1
+XJ=3E-7  LD=3.162278E-11  WD=0
+CGDO=0  CGSO=0  CGBO=0
+CJ=0  PB=0.9758533  MJ=0.3448504
+CJSW=0 MJSW=0.3508721


.model TN2 NMOS LEVEL=3
+TOX=7.5E-9 NSUB=1E17
GAMMA=0.5827871
+PHI=0.9  VTO=2.26  DELTA=0
+UO=205  ETA=0  THETA=0.1749684
+KP=4.264274331E-5
VMAX=8.309444E4  KAPPA=0.2574081
+RSH=0.0559398  NFS=1E12  TPG=1
+XJ=3E-7  LD=3.162278E-11  WD=0
+CGDO=0.22E-15  CGSO=0.22E-15
CGBO=0
+CJ=0  PB=0.9758533  MJ=0.3448504
+CJSW=0  MJSW=0.3508721


.model TN3 NMOS LEVEL=3
+TOX=7.5E-9  NSUB=1E17
GAMMA=0.5827871
+PHI=0.9  VTO=1.7  DELTA=0
+UO=205  ETA=0  THETA=0.1749684
+KP=4.264274331E-5
VMAX=8.309444E4  KAPPA=0.2574081
+RSH=0.0559398 NFS=1E12  TPG=1
+XJ=3E-7 LD=3.162278E-11  WD=0
+CGDO=0.22E-15 CGSO=0.22E-15
CGBO=0
+CJ=0  PB=0.9758533 MJ=0.3448504
+CJSW=0  MJSW=0.3508721
```

L=0.35 µm

W(TN1)= 3.3166E-7m

W(TN2)= 1.8241E-8m

W(TN3)= 9.9E-11m

Size (W/L = 0.4 µm/0.4 µm)

```
.model TN1 NMOS LEVEL=3
+TOX=7.5E-9  NSUB=1E17
GAMMA=0.5827871
+PHI=0.9  VTO=3.5  DELTA=0
+UO=205  ETA=0  THETA=0.1749684
+KP=5.738E-5  VMAX=8.309444E4
KAPPA=0.2574081
+RSH=0.0559398  NFS=1E12  TPG=1
+XJ=3E-7  LD=3.162278E-11  WD=0
+CGDO=0  CGSO=0  CGBO=0
+CJ=0  PB=0.9758533  MJ=0.3448504
+CJSW=0  MJSW=0.3508721


.model TN2 NMOS LEVEL=3
+TOX=7.5E-9  NSUB=1E17
GAMMA=0.5827871
+PHI=0.9  VTO=2.2  DELTA=0
+UO=205  ETA=0  THETA=0.1749684
+KP=5.738E-5  VMAX=8.309444E4
KAPPA=0.2574081
+RSH=0.0559398  NFS=1E12  TPG=1
+XJ=3E-7  LD=3.162278E-11  WD=0
+CGDO=0.22E-15  CGSO=0.22E-15
CGBO=0
+CJ=0  PB=0.9758533  MJ=0.3448504
+CJSW=0  MJSW=0.3508721


.model TN3 NMOS LEVEL=3
+TOX=7.5E-9  NSUB=1E17
GAMMA=0.5827871
+PHI=0.9  VTO=1.75  DELTA=0
```

+UO=205 ETA=0 THETA=0.1749684
+KP=5.738E-5 VMAX=8.309444E4
KAPPA=0.2574081
+RSH=0.0559398 NFS=1E12 TPG=1
+XJ=3E-7 LD=3.162278E-11 WD=0
+CGDO=0.22E-15 CGSO=0.22E-15
CGBO=0
+CJ=0 PB=0.9758533 MJ=0.3448504
+CJSW=0 MJSW=0.3508721

L=0.4 µm

W(TN1)= 3.789E-7 m

W(TN2)= 2.103E-8 m

W(TN3)= 7E-11 m

Size (W/L = 1 µm/1 µm)

.model TN1 NMOS LEVEL=3

+TOX=7.5E-9 NSUB=1E17
GAMMA=0.5827871
+PHI=0.9 VTO=3.9 DELTA=0
+UO=205 ETA=0 THETA=0.1749684
+KP=3.23854E-5 VMAX=8.309444E4
KAPPA=0.2574081
+RSH=0.0559398 NFS=1E12 TPG=1
+XJ=3E-7 LD=3.162278E-11 WD=0
+CGDO=0 CGSO=0 CGBO=0
+CJ=0 PB=0.9758533 MJ=0.3448504
+CJSW=0 MJSW=0.3508721

.model TN2 NMOS LEVEL=3

+TOX=7.5E-9 NSUB=1E17
GAMMA=0.5827871
+PHI=0.9 VTO=2.3 DELTA=0
+UO=205 ETA=0 THETA=0.1749684
+KP=3.23854E-5 VMAX=8.309444E4
KAPPA=0.2574081
+RSH=0.0559398 NFS=1E12 TPG=1
+XJ=3E-7 LD=3.162278E-11 WD=0
+CGDO=0.22E-15 CGSO=0.22E-15
CGBO=0
+CJ=0 PB=0.9758533 MJ=0.3448504
+CJSW=0 MJSW=0.3508721

.model TN3 NMOS LEVEL=3

+TOX=7.5E-9 NSUB=1E17
GAMMA=0.5827871
+PHI=0.9 VTO=2.0 DELTA=0
+UO=205 ETA=0 THETA=0.1749684
+KP=3.23854E-5 VMAX=8.309444E4
KAPPA=0.2574081
+RSH=0.0559398 NFS=1E12 TPG=1
+XJ=3E-7 LD=3.162278E-11 WD=0
+CGDO=0.22E-15 CGSO=0.22E-15
CGBO=0
+CJ=0 PB=0.9758533 MJ=0.3448504
+CJSW=0 MJSW=0.3508721

L=1µm

W(TN1)= 9.2388E-7 m

W(TN2)= 7.39E-8 m

W(TN3)= 2.22E-9 m

List of figures

List of publications

- I.Zbierska, L.Militaru, F.Calmon, G.N.Lu, ‘Electrical Characterization and TCAD simulations of multi-gate NMOSFET’, Microelectronics Journal, (under revision).

- I.Zbierska, L.Militaru, F.Calmon, S.Feruglio, G.N. Lu, ‘Investigation of Electrical Characteristics of Muli-Gate Bulk NMOSFET’, in Proc. of the 29thInternational Conference MIEL, mai 2014, Beograde, Serbie (Best paper award).

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Résumé en français

1. Introduction

Aujourd'hui la question la plus importante qui se pose dans le domaine de la microélectronique est de régler le problème des limites d'échelle, d'où des recherches menées en permanence à ce sujet. La loi bien connue dans le domaine informatique est celle de Moore, qui a pris naissance vers 1970; la version simplifiée de cette loi dit que la vitesse du processeur, ou la puissance de traitement global pour les ordinateurs, vont doubler tous les deux ans. Il s'avère que les dernières tendances en termes de croissance, à savoir en doublant la densité du circuit et en augmentant les performances d'environ 40% pour chaque nouvelle génération de la technologie [1], peuvent être maintenues par la réduction du canal de transistor classique. Pour l'avenir de l'industrie des semi-conducteurs, l'International Technology Roadmap for Semiconductors (ITRS) [2] reconnaît qu'il y a des limites physiques de cette croissance: la longueur de canal du transistor MOS ne peut pas être réduite au-delà d'une certaine taille qui est définie par des limites physiques [3]. Cependant, lorsque la technologie CMOS commence à atteindre ses limites théoriques, l'ITRS prévoit une nouvelle ère connue sous le nom «More Moore». Les nouveaux matériaux et dispositifs relèvent une capacité à compléter ou même remplacer le transistor MOS classique. Effectivement, la solution la plus prometteuse de nos jours, c'est celle des transistors multi-grilles. Les structures bien-connues sont les FinFET, par exemple le FinFET fabriqué en 3D en technologie 22 nm en mai 2011 par la société Intel (figure 1). C'était une vraie innovation dans l'industrie des semi-conducteurs.

Fig.1 Nouveau transistor 3D d'Intel avec d'ailettes verticales [4].

L'architecture multi-grilles peut être utilisée pour les circuits analogiques ainsi que pour les circuits numériques. Cette structure peut également être employée pour l'oscillateur contrôlé en tension ou comme une fonction logique avec un nombre réduit de transistors par rapport à une structure classique. Les applications les plus courantes sont les capteurs d'images, où, pour éviter la dégradation de la diaphonie, de même l'augmentation du courant d'obscurité, les structures d'isolation par tranchée profonde (DTI) ont été utilisées. Il est considéré que c'est une des meilleures structures pour supprimer la diaphonie optique et électrique, grâce à leur propriété de barrière parfaite par rapport à l'isolation d'impureté [4]. Les tranchées d'isolation profonde (DTI) peuvent être implémentées ainsi dans la structure multi-grilles de transistor NMOS.

Le transistor multi-grilles que nous avons étudié dans notre travail de thèse a été fabriqué dans une technologie CMOS bulk 120 nm. Contrairement aux transistors MOS classiques, dans le processus de fabrication, quelques étapes supplémentaires ont été ajoutées, comme l'intégration des tranchées de polysillicium.

L'objectif de notre travail a été de caractériser électriquement et de modéliser le transistor à multi-grilles. Cette structure peut être utilisée en tant que transistor conventionnel dans la matrice de pixels. Le transistor à grille latérale est considéré comme équivalent à trois transistors indépendants. Par conséquent, l'objectif principal de cette recherche est d'étudier l'influence des tranchées sur la performance du transistor. L'étude présentée sera divisées en trois parties. Tout d'abord, le fonctionnement du transistor à grille surfacique sera examiné et comparé au transistor NMOS conventionnel. Ensuite, les performances du transistor latéral seront analysées.

Les transistors multi-grilles sont caractérisés par les méthodes *I-V*, split *C-V* et pompage de charge à deux et à trois niveaux. Les résultats obtenus à partir des techniques de caractérisations

seront ainsi présentés. Dans un premier temps, les mesures *I-V* seront introduites afin de mesurer la pente de seuil, la tension de seuil, ainsi que, le niveau de courant de drain. Ensuite, la méthode split *C-V* sera appliquée pour calculer la mobilité effective des porteurs dans les deux canaux de conduction. Afin d'évaluer la qualité des interfaces oxyde/semi-conducteur, la méthode de pompage de charge à deux et à trois niveaux sera appliquée.

Par la suite, les résultats de simulations TCAD 3D seront exposés. La tension de seuil, la longueur effective du transistor seront étudiées ainsi que les pièges de l'interface Si/SiO_2. Tous les résultats obtenus par simulations seront comparés aux résultats obtenus expérimentalement. La deuxième partie de cette section se concentra sur la modélisation SPICE du transistor multi-grilles. Le modèle préliminaire sera introduit à la base des résultats de mesures. Cette partie permettra de mieux comprendre le fonctionnement électrique de la structure étudiée. Nous finirons par la présentation des conclusions.

2. Transistors MOS à grilles multiples

Les transistors étudiés ont la particularité de posséder des grilles multiples. Plus précisément, ils possèdent une grille supérieure ainsi que deux grilles latérales. L'architecture du transistor analysé dans notre étude est représentée sur le schéma suivant :

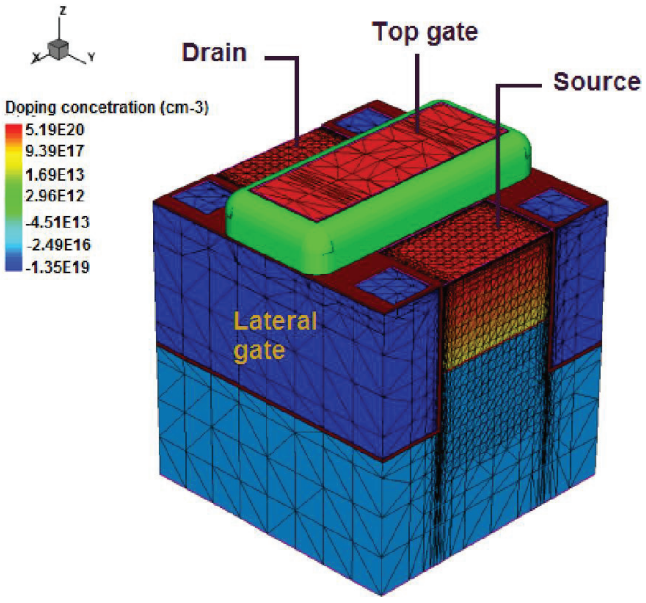

Fig.2 La structure 3D du transistor multi-grill avec des profils de dopage et de maillage visible.

Le substrat est de type p, les transistors sont donc des NMOS. La grille supérieure est en poly silicium dopé n+, isolée du substrat par un oxyde de SiO_2 nitruré d'épaisseur 6 nm. Les grilles latérales sont réalisées en polysilicium dopé p+, avec un oxyde épais de 7.5 nm. La grille supérieure du MOSFET est confinée entre deux tranchées, dont la distance détermine la largeur du canal W. La grille supérieure pouvant être réalisée par un process CMOS standard, la fabrication du dispositif complet ne nécessite que peu d'étapes supplémentaires pour l'intégration des grilles latérales. Des dispositifs de différentes dimensions sont réalisés, avec leurs propre ratio W/L = 1/1, 0.4/0.4, 0.3/0.35, 0.2/0.35 (en µm/µm).

La structure présente trois canaux de conduction, tous reliés à la source et au drain. Les deux canaux latéraux sont, par ailleurs, contrôlés par une seule et unique tension. On pourra ainsi considérer les canaux latéraux comme un canal unique, contrôlé par une tension de grille additionnelle. Plus généralement, on peut voir le dispositif comme deux transistors, avec la source et le drain communs.

3. Caractérisation électrique

Dans ce chapitre, les techniques de caractérisation et les résultats expérimentaux sont présentés. Tout d'abord, les mesures *I -V* seront introduites, pour extraire et analyser la pente sous le seuil (*S*), la tension de seuil (V_{TH}), la mobilité à faible champ ainsi que le courant de drain. Ensuite, la méthode « split *C–V*» nous permettra de déterminer la mobilité effective dans le canal. Grace à la technique de pompage de charge à deux et trois niveaux, la qualité de l'interface sera étudiée. Les études ont été menées pour la structure multi-grilles (transistor supérieur /transistor à grille latérale) et transistor MOS sans grille latérales fabriqués dans les même conditions que les transistors multi-grilles.

3.1. Caractéristiques statiques

Les mesures *I-V* statiques ont été effectuées sur le transistor MOS multi-grilles et le transistor MOS classique fabriqué sur la même plaquette. A partir des caractéristiques *I-V* mesurées, il est

possible d'extraire certains paramètres importants, tels que la tension de seuil V_{TH}, la pente sous le seuil S et la mobilité de faible champ μ_0. La tension de seuil a été extraite en utilisant la fonction Y [6] et la méthode Hamer [7]. Pour le dispositif multi-grilles, les caractéristiques *I-V* de la grille surfacique ont été obtenus avec une polarisation de la grille latérale inférieure à la valeur de la tension de seuil du transistor latéral.

3.1.1. Résultats *I-V* pour le transistor surfacique

Tout d'abord, les études concernant la grille supérieure seront présentées. En outre, les résultats ont été comparés avec le NMOSFET conventionnel. Pour mesurer la caractéristique $I_D(V_G)$, la tension de grille supérieure (V_G) varie de -2V jusqu'à 6V avec la tension de grille latérale constante $V_{LTG} = -2V$. Dans cette situation, le canal latéral n'est pas créé et la conduction n'a lieu que dans le canal supérieur. La tension source-drain est fixée à 50 mV afin de se placer dans la zone linéaire de fonctionnement. Pour réaliser ces analyses, le transistor multi-grilles avec la dimension W/L = 0,3 µm / 0,35 µm et NMOSFET classique avec W/L = 0,38 µm / 0,28 µm ont été utilisés.

Fig.3 Les caractéristiques I_D (V_{GS}) (grille surfacique du transistor multi-grilles MOSFET, W/L=0.3 µm /0.35µm, NMOSFET conventionnel W/L = 0.38 µm /0.28µm, V_{DS}= 50mV, V_{LTG} = -2V).

La figure 3 présente les caractéristiques *I-V* pour la structure multi-grilles et le transistor conventionnel. La pente sous le seuil du transistor supérieur est 93 mV/déc comparativement à 83 mV/déc pour le NMOSFET conventionnel. Le comportement électrique de la structure multi-

grilles est similaire avec le nMOS conventionnel. La tension de seuil a été extrait par la méthode Hamer avec V_{LTG} = - 2V: pour la structure multi-grilles (W/L = 0.3 µm /0.3µm) V_{TH} = 0.49V et pour NMOS classique (W/L = 0.38 µm /0.28 µm) V_{TH} = 0.45V. Comme ces valeurs sont presque similaires, nous pouvons affirmer que la grille supérieure de la structure multi-grilles se comporte comme la structure conventionnelle.

Des analyses similaires ont été menées pour les différentes polarisations de la grille latérale V_{LTG} = 2V, -1V, 0V pour détecter l'influence de la grille latérale sur la conduction dans le canal supérieur.

Fig.4 Les caractéristiques I_D (V_{GS}) (grille surfacique, W/L = 0.3 µm /0.35µm, V_{DS} = 50mV, V_{LTG} = -2V, -1V, 0V).

Le décalage de tension de seuil a été observé. La tension de seuil du transistor surfacique augmente avec la diminution de la polarisation latérale. La tension de seuil est modulée par le biais de la grille latérale. Cet effet peut être observé notamment pour une tension V_{LTG} supérieure à -2V, au-dessus de cette valeur la performance du transistor étant dégradée. De la caractéristique $I_D(V_{GS})$ mesurée avec des variations de la polarisation de la grille latérale, la tension de seuil, associées à V_{LTG}, peut être extraite. La tendance suivante a été observée : une diminution de la tension de grille latérale conduit à une augmentation de la tension de seuil du transistor surfacique. Cette dépendance peut être expliquée par l'effet de la modulation de la grille latérale sur la largeur efficace de canal de la grille surfacique. Cet effet peut être expliqué par le niveau de dopage effectif, il est possible de changer la tension de V_{FB} moyenne par réglage de la tension de grille latérale (V_{LTG}). En polarisant les tranchées LTG, par exemple dans des zones d'accumulation, la tension de seuil est décalée d'une quantité correspondant à l'augmentation de la

concentration de trous par effet électrostatique.

En utilisant la fonction Y, la mobilité à champ faible a été extraite. Le transistor surfacique de la structure multi-grilles a une mobilité μ_o = 200 cm^2/V*s, alors que la structure conventionnelle μ_o = 221 cm^2/V*s. Comme nous l'attendions, les valeurs de mobilités obtenues sont cohérentes, et, en général, tous les paramètres extraits étaient quasiment identiques.

Pour compléter les études *I-V* statiques, la tension de polarisation positive a été appliquée sur la grille latérale. Les caractéristiques de du transistor surfacique sont présentées sur la figure 5.

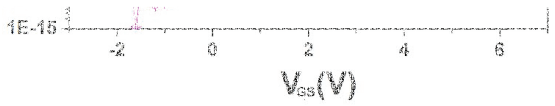

Fig.5 Les caractéristiques I_D (V_{GS}) (W/L = 0.3 µm/0.35µm, V_{DS} = 50mV, V_{LTG}= 3V, 4V, 5V, 6V).

La polarisation positive a aussi une influence sur la tension de seuil. Avec la diminution de la tension appliquée sur la grille latérale, la tension de seuil de la grille surfacique augmente.

3.1.2. Résultats pour le transistor latéral

Il est possible aussi de caractériser la conduction dans le canal latéral du transistor multi-grille. Ce canal est inhabituel puisque son extension est verticale. Les résultats ont été comparés avec les résultats obtenus pour le canal surfacique, présentées précédemment.

La figure 5 présente la caractéristique $I_D(V_{LTG})$ qui est comparée avec les caractéristiques $I_D(V_{GS})$, analysées dans la section 3.1.1. Les caractéristiques du transistor supérieur ont été extraites avec une polarisation de grille latérale positive (V_{LTG} = 6V) et une polarisation de grille latérale négative (V_{LTG} = - 2V).

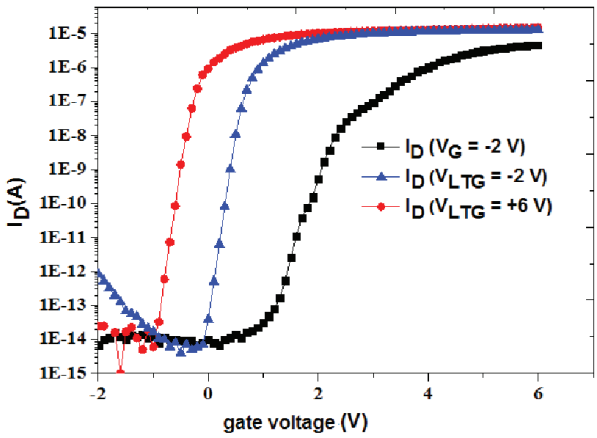

Fig.6 Les caractéristiques I_D-V_{GS} et I_D-V_{LTG} de multi-grilles NMOSFET (W/L = 0,3 µm / 0,35 µm), avec V_{DS} = 50 mV et V_{BS} = 0 V.

Nous pouvons observer que la structure multi-grilles a une caractéristique *I-V* différente entre la grille latérale et grille surfacique. Pour la grille latérale, la tension de seuil est beaucoup plus élevée par rapport à celle qui a été évaluée pour le transistor à grille surfacique. Comme la caractéristique de la grille latérale présente trois paliers (pics), ainsi trois tensions de seuil peuvent être distinguées. La première est V_{TH1} = 1,9 V, la deuxième V_{TH2} = 2,3 V et la troisième V_{TH3} = 3,6 V (Fig. 6). Ainsi, la tension de seuil de la grille latérale (V_{TH3} = 3,6 V) est près de neuf fois plus importante que celle du grille surfacique. Ce phénomène peut s'expliquer par les différents types de dopage pour chaque grille. Lorsque la grille supérieure est dopé n +, la latéral est dopé p +. La grille latérale présente un comportement multi-seuil, ce qui est indiqué par les trois pics sur sa caractéristique I_D-V_{GS}. Ces pics correspondent à trois canaux différents qui présentent des tensions de seuil différentes. La figure 7 présente les caractéristiques *I-V* avec l'indication de trois paliers.

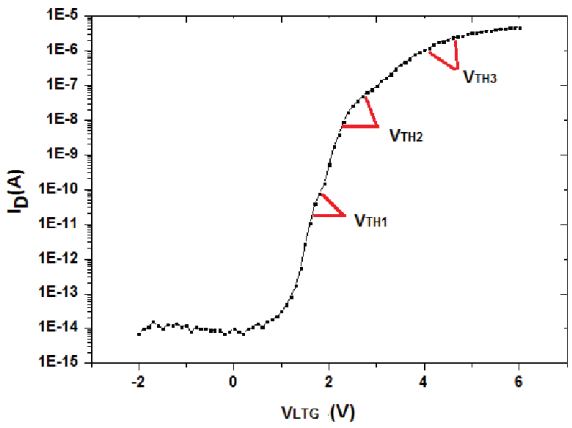

Fig.7 Les caractéristiques I_D-V_{LTG} du transistor latéral
(W/L = 0,3 µm / 0,35 µm), avec V_{DS} = 50 mV, V_G = -2V,V_{BS} = 0 V.

Par conséquent, la structure se comporte comme trois transistors en parallèle, chaque transistor ayant des dimensions et des paramètres différents. Ce phénomène pourrait être expliqué par le dopage non homogène de la grille latérale.

3.2. *La méthode split C-V : extraction de la mobilité effective*

Entre la variété des techniques qui permettent d'obtenir la mobilité effective, nous pouvons distinguer la méthode de la fonction Y [6], la méthode split *C–V* à haute fréquence [9] ou la méthode split *C-V* à basse fréquence [10]. Pour nos mesures, nous avons décidé d'appliquer la dernière car elle est la plus fiable et la plus précise par rapport aux deux autres méthodes. En outre, la méthode split *C-V* à haute fréquence nécessite des structures spécifiques qui n'étaient pas disponibles pour cette étude.

3.2.1. Résultats pour la grille surfacique

Les résultats obtenus par des mesures *C-V* de la grille surfacique seront présentées. Tout d'abord, les caractéristiques $C_{CG}(V_G)$ pour les transistors disponibles sont présentés.

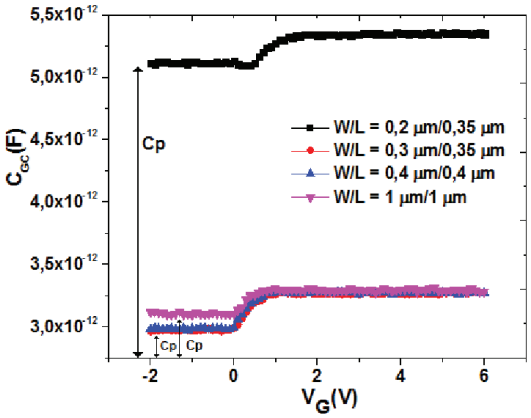

Fig.8 Les caractéristiques $C_{GC}(V_G)$ pour W/L= 0.2 µm /0.35 µm, W/L=0.3 µm /0.35 µm, W/L=0.4 µm /0.4 µm, W/L= 1 µm /1 µm et F_P=1 MHZ.

Le plus petit transistor a la plus grande capacité parasite (C_p). Pour obtenir la valeur exacte de la capacité d'oxyde (C_{ox}), nous avons besoin de la détermination de la surface du transistor, ainsi, la correction de la capacité parasite a été effectuée [10]. En réalité, il existe une différence entre la surface de transistor déterminée par les dimensions du canal (S_t) et la surface réelle appliquée pour la mesure, ici appelées aussi (S_r). Puisque une surface réelle correspond à plusieurs transistors en parallèle, il est impossible de mesurer directement la capacité du transistor unique. Par conséquent, il est essentiel de déterminer S_r pour le calcul juste de la valeur de la charge d'inversion. L'équation I est transformée en fonction de la détermination de la surface.

$$C_{OX} = \frac{\varepsilon_o \varepsilon_{SiO_2} S_r}{T_{OX}} \qquad \text{(I)}$$

$$S_r = \frac{C_{OX} T_{OX}}{\varepsilon_o \varepsilon_{SiO_2}} \qquad \text{(II)}$$

Lorsque $\mathcal{E}_o$ est la permittivité du vide, $\mathcal{E}_{SiO2}$ est la permittivité du semi-conducteur et T_{ox} signifie l'épaisseur d'oxyde.

Sachant la valeur réelle de la surface, le calcul de la valeur réelle de la charge d'inversion peut être réalisé en utilisant l'expression suivante:

$$Q_{ireal}(V_G) = Q_i(V_G) * \frac{S_t}{S_r} \qquad \text{(III)}$$

La figure 9 présente les capacités surfaciques après correction de la capacité parasite et de la surface.

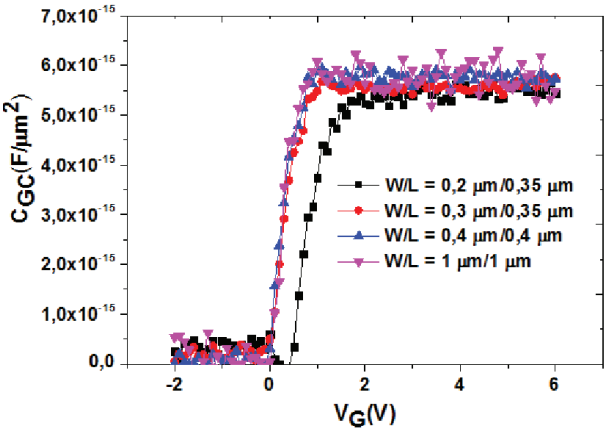

Fig.9 Les caractéristiques $C_{GC}(V_G)$ pour W/L=0.2 µm /0.35 µm, W/L=0.3 µm /0.35 µm, W/L=0.4 µm /0.4 µm, W/L=1 µm /1 µm après correction de la capacité parasite et de la surface.

Il est également intéressant d'observer l'évolution de la mobilité effective avec la dimension du transistor. La figure 10 présente les caractéristiques obtenus pour les quatre dimensions de transistor avec la polarisation V_{LTG} = - 2V.

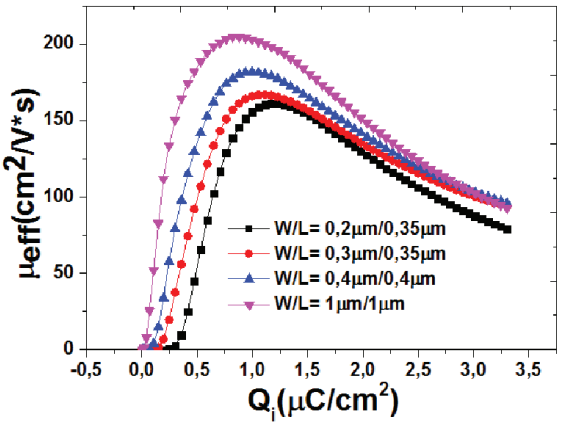

Fig.10 La mobilité effective en fonction de la longueur du canal pour W/L = 0.2 µm/0.35 µm, W/L = 0.3 µm/0.35 µm, W/L = 0.4 µm/0.4 µm, W/L = 1 µm/1µm avec V_{LTG} = -2V.

Il est clairement visible que la valeur de la mobilité dépend de la dimension du transistor. Pour les transistors à canal similaire de longueur L = 0,35 µm, la valeur de la μ_{eff} est à peu près la même. De plus, on peut affirmer que la mobilité maximale augmente avec la longueur du canal.

La mobilité effective μ_{eff} est un paramètre clé qui caractérise le transport dans les transistors MOSFETs. La mobilité des électrons dans le canal a été évaluée expérimentalement en utilisant la technique de séparation *C-V*. On a analysé le comportement de la courbe de la mobilité effective ainsi que l'influence de la longueur du transistor sur la mobilité de canal effective.

La valeur L_{eff}, extraite par des simulations TCAD, est intégrée dans l'équation V :

$$\mu_{eff} = \frac{I_{DS}}{V_{DS}} \frac{L}{W} \frac{1}{Q_i} \qquad \text{(V)}$$

Les caractéristiques extraites ont été comparées à celles qui ont été évaluées par les mesures. L'extraction a été faite pour deux valeurs de la longueur du canal: L_{geom} = 0.35 µm, L_{eff} = 0.32 µm pour V_{DS} = 0.05 V. Figure 11 présente la mobilité effective en fonction de la charge d'inversion Q_i.

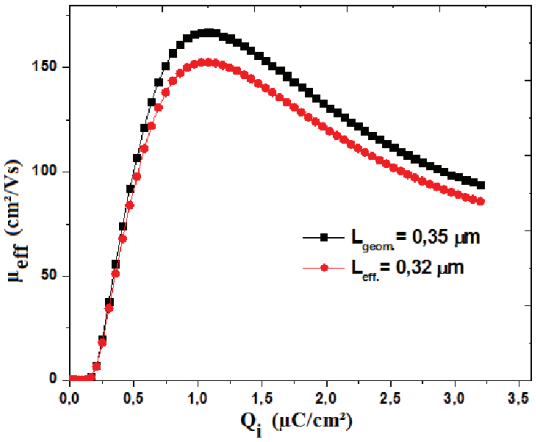

Fig.11 La mobilité effective extraite avec L_{geom} et avec L_{eff} versus l'inversion de charge de composant multi-grilles, extraite par les mesures électriques (W/L = 0.3µm/0.35µm), pour V_{LTG} = -2V.

La valeur maximale de la mobilité extraite avec L_{eff} diminue de 8,4%. En se basant sur l'équation (V), la mobilité effective dépend des dimensions du canal, de la capacité canal-grille et de courant de drain. Par conséquent, l'effet de canal court a une forte influence sur le comportement d'un transistor. En outre, la dépendance de la mobilité effective sur la longueur du canal peut être différente en raison de la diffusion, comme la rugosité de surface, la diffusion des phonons et de la diffusion de Coulomb. La mobilité est dégradée avec la miniaturisation de canal de MOSFET. La mobilité extraite, avec L_{eff} = 0.32 µm à V_{DS} = 0,05 V diminue lorsqu'on a une faible couche d'inversion (Q_i < 1.0 µC/cm^2). Cette diminution est due à l'augmentation de la diffusion de Coulomb. Pour Q_i > 1.0 µC/cm^2, la dégradation de la mobilité effective est due à la diffusion de la rugosité de surface [14].

3.2.2. Comparaison entre la grille surfacique du transistor multi-grilles et de la structure conventionnelle

Ces courbes (figure 12) peuvent être considérées en les divisant en deux parties. Tout d'abord, pour Q_i > 0.5 µC/cm^2 pour le NMOSFET classique et Q_i > 1.8 µC/cm^2 pour la structure multi-grilles, le dispositif multi-grilles possède une mobilité légèrement plus élevée par rapport au dispositif conventionnel. La différence de la charge d'inversion dépend de leur tension de seuil respective. Par conséquent, nous pouvons affirmer que la mobilité dans le canal supérieur du

transistor multi-grilles n'est pas dégradée par le processus d'intégration des grilles latérales. Pour la deuxième partie de la courbe de la mobilité (Q_i < 0.5 µC/cm^2 pour le transistor classique et Q_i < 1.8 µC/cm^2 pour la structure multi-grilles), le dispositif multi-grilles possède une mobilité dégradée, due probablement à une densité de défauts plus importante à l'interface. Cette différence peut correspondre aux valeurs différentes de leur pente sous le seuil respectif, pour la structure multi-grilles S = 93 mV/déc et pour NMOSFET conventionnel S = 83 mV/déc.

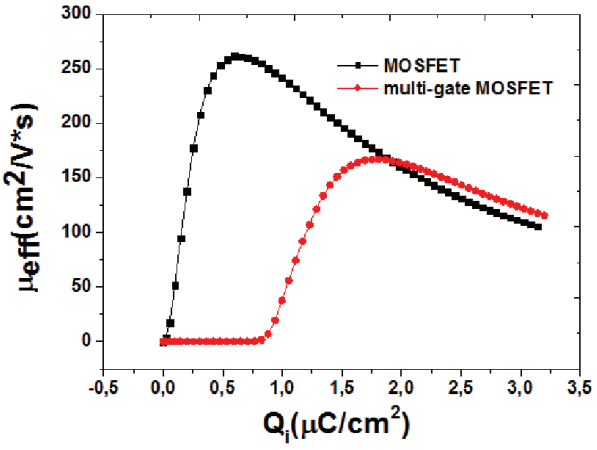

Fig.12 La mobilité effective versus charge d'inversion pour NMOSFET conventionnel (W/L = 0.38 µm/0.28 µm), avec V_G = -2V, et structure multi-grilles (W/L = 0.3 µm/0.35 µm), avec V_{LTG} = -2V.

3.2.3. Résultats pour le grille latérale

Pour évaluer les performances de transistors latéraux, nous avons appliqué la même procédure que dans le cas des transistors supérieurs. Tout d'abord, la capacité C_{GC} a été mesurée. En comparant les capacités parasites, nous avons observé que la grille latérale génère une valeur de capacité parasite beaucoup plus importantes $C_{p,lat}$ = 2 pF, alors que le $C_{p,surf}$ = 0.35 pF. Pour obtenir la valeur réelle de la charge d'inversion et de la mobilité effective, la correction de la surface est obligatoire. Comme pour la grille supérieure, l'équation II est appliquée mais le paramètre S_t (surface de transistor déterminé par la dimension du canal) est ici défini comme:

$$S_t = L * h * 2 \qquad \text{(IV)}$$

où L désigne la longueur de canal, h la hauteur de la tranchée.

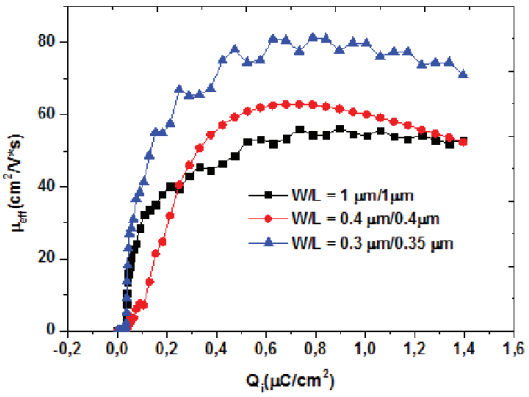

Fig.13 $\mu_{eff}(Q_i)$ pour V_G = -2V, W/L = 0.3 µm/0.35 µm, W/L = 0.4 µm/0.4 µm, W/L = 1 µm/1 µm.

La figure 13 présente la mobilité effective extraite pour le transistor à grille latérale. Les résultats ont montré que le comportement de la grille latérale est contraire à celui du transistor supérieur. Ce phénomène est dû à la différence de la valeur de la densité de l'interface, (voir section 3.3.1). Egalement, la mobilité diminue avec l'augmentation de la surface du transistor. Cette situation est provoquée par le non homogénéité du dopage des canaux latéraux. De plus, la valeur maximale de la mobilité effective est beaucoup plus faible par rapport à la valeur de la mobilité obtenue pour le canal supérieur.

3.3. Pompage de charge à deux et trois niveaux

La technique de pompage de charge est une technique de caractérisation pour déterminer la densité moyenne d'états de l'interface Si-isolant, ainsi que, la répartition de l'énergie et de la section efficace de capture [11].

3.3.1. Pompage de charge

Le principe de cette mesure consiste à sonder, dans un premier temps, la partie supérieure de la bande interdite pour observer l'émission d'électrons, puis la partie plus faible pour la détermination de l'émission de trous. Le signal à trois niveaux a été appliqué. Figure 14 montre la fonction de pompage de charge en fonction de V_3, déterminé par l'application du signal à trois niveaux à grille surfacique.

Fig.14 La fonction de pompage de charge en fonction de V_3 (F = 1MHz, V_{GBl} = -2.7V, V_{GBh} = 0.86V, t_r = 5E-08, t_f = 5E-08, W/L = 0.3 µm/0.35 µm, Tox= 6 nm).

Dans la figure 14, on distingue les deux mesures différentes qui séparent les accepteurs et les donneurs. Pour obtenir la distribution énergétique des défauts accepteurs, la variation de l'émission d'électrons a été effectuée. La grille a été polarisée selon de schéma: $V_{GBI} \rightarrow V_{GBh} \rightarrow V_3 \rightarrow V_{GBI}$ (courbe en noir). Les variations similaires ont été exécutées pour l'émission des trous, afin de déterminer la distribution énergétique des défauts donneurs (courbe en rouge). La tension de grille a été modifiée comme: $V_{GBh} \rightarrow V_{GBI} \rightarrow V_3 \rightarrow V_{GBh}$. La figure 15 illustre l'exemple de spectre de la distribution énergétique des états d'interface pour la grille supérieure, déterminée par le pompage de charge à trois niveaux.

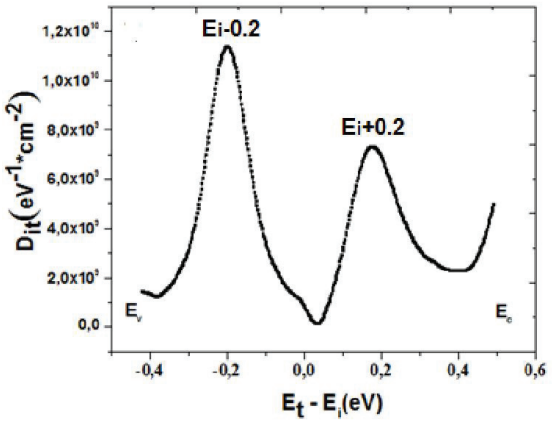

Fig.15 La distribution d'énergie des états d'interface pour la grille supérieure (F=1MHz, W/L = 0.3 µm/0.35 µm, Tox= 6 nm).

Il doit être mentionné que les mesures sont limitées à l'intervalle [E_i - $q\Phi F$; E_i + $q\Phi F$]. Par conséquent, ils ne sont pas valables à proximité du milieu de la bande interdite et à proximité de la bande de conduction et de la bande de valence. Comme dans un empilement SiO2/Si, il existe deux pics, qui présentent la même asymétrie de la distribution dans les deux moitiés de la bande interdite. Cette distribution révèle deux types de pièges prédominantes localisées à l'interface Si/SiO_2 et en raison des « dangling bonds », avec l'énergie E_v+0.2 eV et E_c-0,3 eV, respectivement, où E_c est l'énergie de la bande de conduction et E_v est l'énergie de bande de valence.

La figure 16 illustre la répartition énergétique des pièges d'interface pour le transistor à grille latérale.

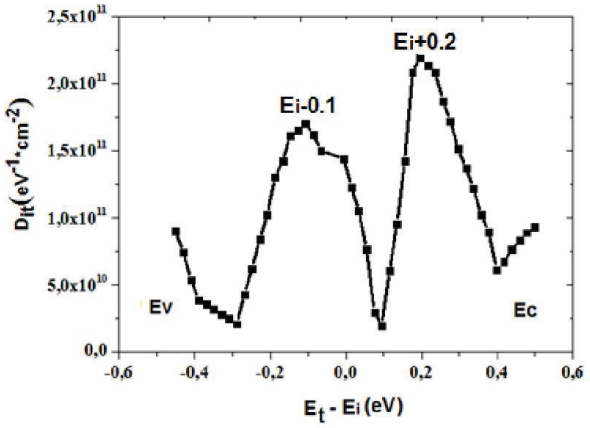

Fig.16 La distribution d'énergie des états d'interface pour la grille latérale
(*F*=1MHz, *W/L* = 0.3 µm/0.35 µm, *Tox*= 10.5 nm).

Le spectre de la distribution énergétique des états d'interface dans la grille latérale présente deux pics. Comme il a déjà été indiqué, la valeur de la densité d'interface est de deux ordres de grandeur plus élevée par rapport à la structure de grille supérieure, en raison de l'intégration de grille latérale des tranchées.

4. TCAD modélisations et SPICE simulations

Ce chapitre présente des études de la structure multi-grilles par modélisations TCAD et simulations SPICE. Grâce aux modélisations TCAD en 2D et 3D, le comportement électrique du transistor multi-grilles, en particulier les caractéristiques de la grille supérieure, ont été simulées et comparées avec les résultats obtenus par des mesures expérimentales. La tension de seuil et la longueur effective de canal du transistor multi-grilles ont été étudiées. La mobilité d'électrons à la surface de canal à faible champ ainsi que la qualité de l'interface Si/SiO_2 ont également été vérifiées.

4.1. *Etude statique de courant du drain en fonction de la tension de grille $I_D(V_G)$*

Les caractéristiques courant - tension ont été extraites à partir de simulations 3D. Les simulations ont été réalisées avec un dopage du substrat (sous la grille supérieure) de valeur B_{dop} = 3×10^{17} cm^{-3}. La figure 16 compare les caractéristiques *I-V* issues de simulation 3D aux mesures expérimentales. Afin de comparer l'ensemble des caractéristiques, le courant de drain a été divisé par la largeur du transistor, par conséquent, la densité du courant I_D est tracée en A /µm.

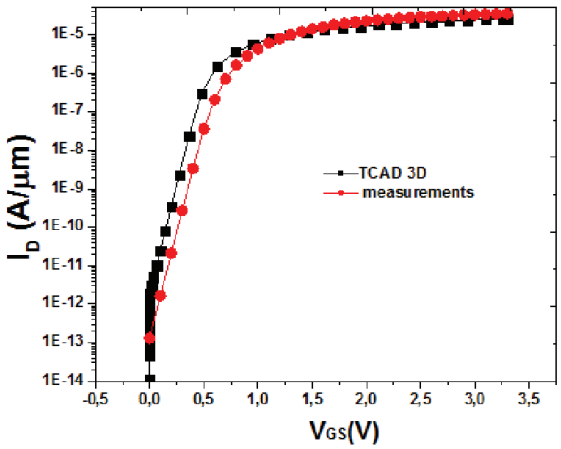

Fig.17 Comparaison de résultats de simulation (3D TCAD) avec les mesures expérimentales d'un transistor multi-grilles (*W/L* = 0.3µm/0.35µm) et NMOSFET conventionnel pour V_{LTG} = -2V, avec V_{DS} = 50mV et V_{BS} = 0V.

Pour les simulations 3D, les trois grilles (une supérieure et deux latérales) ont été prises en considération. Les courbes de la figure 15 montrent que la tension de seuil extraite à partir des mesures expérimentales est légèrement supérieure (V_{TH} = 0.59 V) à la tension de seuil simulée (V_{TH} = 0.5 V). Cette différence devrait être due au phénomène de piégeage à l'interface ou dans le volume de l'oxyde, qui n'est pas parfaitement pris en compte dans le modèle utilisé dans la simulation TCAD. La pente sous le seuil extraite des mesures est 89 mV/déc par rapport à 90mV/déc obtenu par les simulations. Cela reflète une bonne précision des résultats de simulations par rapport aux résultats expérimentaux. Les courbes présentées dans la figure 17 confirment la fiabilité du modèle TCAD avec des résultats de simulations qui correspondent bien aux mesures électriques réalisées.

4.2. La qualité de l'interface SiO_2 /Si

La formation des pièges à l'interface Si/SiO_2 dans les dispositifs MOSFET est considérée comme un mécanisme responsable de la dégradation des caractéristiques des transistors [11]. Le phénomène de piégeage à l'interface Si/SiO_2 est devenu un problème crucial pour les circuits CMOS, en impactant le courant à travers le canal de transistor et en modifiant la valeur de la tension de seuil [12]. Pour étudier la dégradation du courant de drain dans les transistors à multi-grilles, nous avons réalisé des simulations *I-V* en introduisant une distribution gaussienne des défauts à l'interface oxyde/canal. La densité d'états à l'interface a déjà été étudiée en se basant sur des techniques de pompage de charge à deux et trois niveaux [13]A l'aide de pompage de charge à deux niveaux, on a obtenu une densité d'états à l'interface moyenne D_{it} = $3.9x10^{9}eV^{-1}cm^{-2}$ et une efficacité de section de capture σ = $9.45x10^{-17}cm^{2}$. Ensuite, les mesures de pompage de charge à trois niveaux ont permis d'obtenir la distribution de l'énergie D_{it} de la bande interdite dans le silicium.

Cette distribution révèle deux types de pièges prédominants localisés à l'interface Si/SiO_2. La courbe de courant I_D en fonction de la tension de grille (V_{GS}) est obtenue à une faible tension de polarisation V_{DS} = 0.05V. Pour effectuer la simulation de la dégradation, nous avons utilisé la valeur de la densité moyenne des états d'interface extraite expérimentalement.

Les caractéristiques I_D-V_{GS} simulées sont tracées sur la figure 16. Trois courbes sont représentées:

i) I_D-V_{GS} obtenue à partir des résultats de simulations sous TCAD en tenant compte de l'impact de la distribution des pièges-donneurs et des pièges-accepteurs à l'interface.

ii) I_D-V_{GS} obtenue à partir des résultats de simulations sous TCAD sans tenir compte du phénomène de piégeage à l'interface.

iii) I_D-V_{GS} obtenue à partir des résultats des mesures électriques.

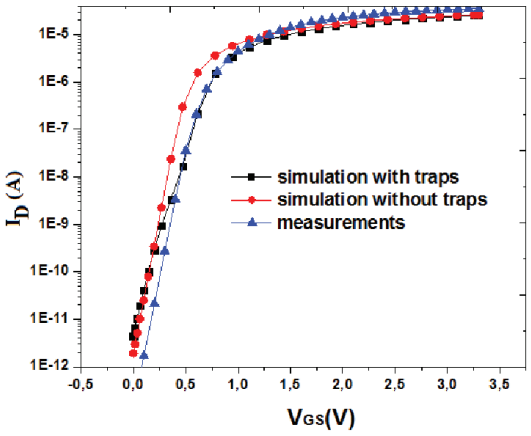

Fig. 18 Comparaison des résultats de simulations en 3D TCAD et des résultats expérimentales mesurées pour une structure multi-grilles (L=0.35µm) avec pièges injection, sans pièges et les mesures pour V_{LTG} = -2V avec V_{DS} = 50mV et V_{BS} = 0V.

La figure 18 montre bien l'impact de la distribution des défauts d'interface (D_{it}) sur la tension de seuil. L'écart est observé sur la pente de la tension de sous-seuil, pour une faible valeur de la tension de grille, qui est dégradé environ 11% par rapport aux valeurs mesurées. On observe aussi le décalage de la tension de seuil, entre les courbes avec et sans pièges, en raison des pièges donneurs et des pièges accepteurs.

Pour une meilleure compréhension du phénomène observé, les concentrations des pièges accepteurs et des pièges donneurs ont été simulées séparément.

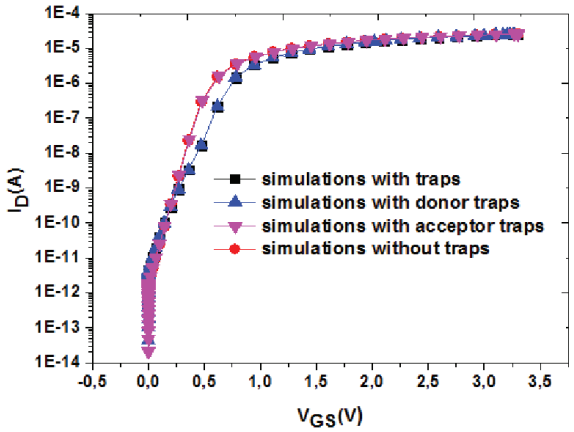

Fig. 19 Caractéristiques I_D-V_G obtenus par des simulations 3D TCAD d'une structure multi-grilles (L = 0.35µm) avec et sans pièges pour V_{LTG} = -2V avec V_{DS} = 50mV et V_{BS} = 0V.

On remarque sur la figure 19 que les pièges donneurs ont une influence plus importante sur les caractéristiques courant-tension que les pièges accepteurs. La dégradation est observée lorsque le courant I_D atteint la valeur de 0.016mA. Comme le courant de drain augmente, le niveau de Fermi atteint la partie haute de la distribution de Dit dans la bande interdite. La quantité significative des pièges donneurs peut être à l'origine de la dégradation de la pente de sous-seuil, observée sur la figure 18.

4.3.*Modélisation SPICE du courant de drain*

L'objectif de nos études est d'obtenir un model précis de transistor à multi-grilles. Un model SPICE prend en compte plusieurs paramètres technologiques obtenus ou calibrés à partir des mesures expérimentales. La grille latérale de ce dispositif présente trois comportements liés à la tension de seuil des courbes *I-V*. La grille latérale peut être modélisée en considérant, en parallèle, trois transistors équivalents connectés source-drain avec différentes tensions de seuil et dimensions. Quant à la grille supérieure, elle fonctionne comme un transistor conventionnel. Finalement, le modèle SPICE proposé est composé de quatre transistors en parallèle avec des multiples tensions de seuil (un pour la grille surfacique et trois pour la grille latérale). Par réglage des différents paramètres du modèle SPICE sur les transistors, les caractéristiques du MOSFET multi-grilles peuvent être reproduites correctement.

4.3.1. Modélisation de la grille surfacique

Comme il a été déjà mentionné, l'objectif de ces études est d'obtenir des courbes *I-V* similaires à celles obtenues par des mesures électriques. Tout d'abord, le modèle « niveau 3 » [15]d'un transistor a été appliquée pour la modélisation du transistor avec une grille surfacique. Dans le modèle SPICE du transistor NMOS, nous avons gardé les paramètres suivants: *NSUB*, *TOX*, *VTO*, où *NSUB* est le dopage du substrat avec une valeur de $3x10^{17}$ cm^{-3}, *TOX* désigne l'épaisseur d'oxyde (*TOX* = 6 nm) et *VTO* est la tension de polarisation. L'ajustement a été traité sur le paramètre de transconductance *KP* exprimée en [A/V^2]. Ce paramètre peut être défini essentiellement comme le rapport entre C_{ox} et μ_o.

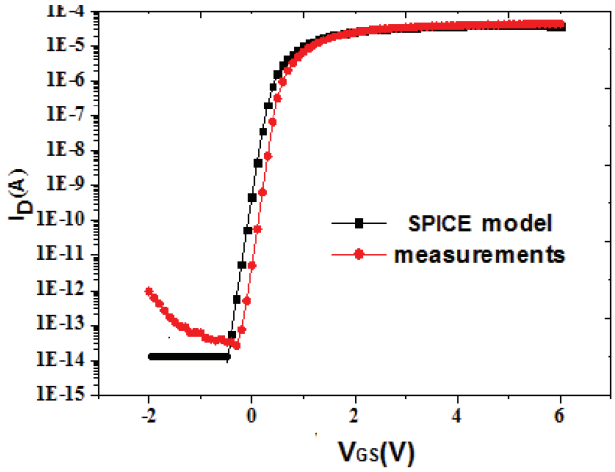

Fig.20 Comparaison des résultats de simulations SPICE de $I_D(V_G)$ avec les valeurs des mesures expérimentales pour W/L = 0.3 µm/0.35 µm, V_{DS}=50mV, V_G=-2V, V_{BS} = 0V.

La figure 20 montre une comparaison des caractéristiques I_D-V_{GS} extraites des mesures et des simulations SPICE. Une bonne précision est offerte par le model SPICE.

4.3.2. Modélisation de la grille latérale

Afin de modéliser la grille latérale, nous avons considéré trois transistors en parallèle, avec les drains communs et les sources communes, en fixant une tension de seuil spécifique pour chaque transistor. Les trois transistors NMOS parallèles sont contrôlés par la même tension de grille avec la même tension de polarisation V_{DS}. Figure 21 représente les transistors associés aux grilles latérales. Le modèle SPICE utilisé par les trois transistors qui présentent la grille latérale est le même modèle utilisé pour la grille surfacique.

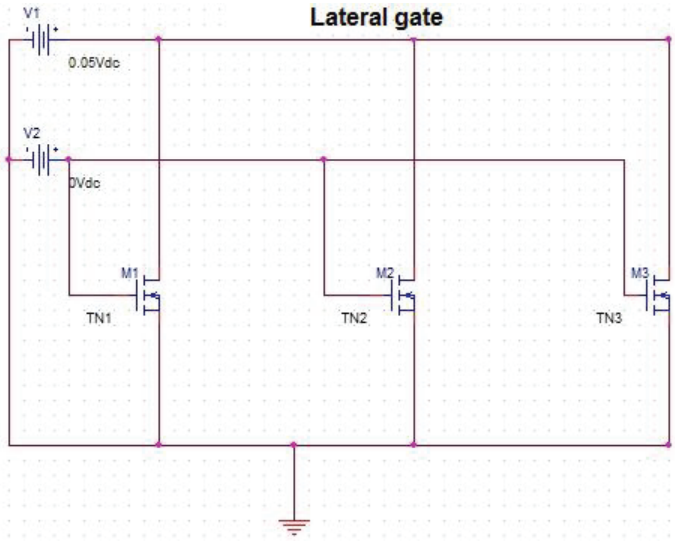

Fig. 21 Schéma du modèle de la grille latérale.

Pour les simulations TCAD et les mesures expérimentales, la grille latérale a été activée par variation d'une polarisation positive V_{LTG} jusqu'à 6V sur la grille latérale et une polarisation négative V_G = - 2V sur la grille surfacique. Tous les transistors à grille latérales partagent la même épaisseur d'oxyde (TOX = $7.5x10^{-9}$ µm), le même dopage du substrat ($NSUB$ = $3x10^{17}$ cm^{-3}) et la même longueur du canal L = 0,35 µm. La largeur de canal (W), le paramètre de procédé (KP) et de la tension de seuil des transistors (VTH), sont les paramètres ajustés dans le modèle SPICE pour obtenir les mêmes résultats expérimentaux. Par exemple, le paramètre KP est responsable de l'ajustement de courant. A partir de la figure 7 (section 3.1.2), il est clair que dans la grille latérale, il est possible de distinguer trois transistors avec une tension de seuil spécifique à chacun et une dimension de largeur différente. Par conséquent, le courant de

drain total est la somme de ces trois courants de drain des chaque transistor et il est exprimé par la formule:

$$I_D = I_{D1} + I_{D2} + I_{D3} \quad \text{(VI)}$$

La figure 22 montre l'approximation pour le transistor avec dimensions W_L/L = 0,32 µm/0,35 µm.

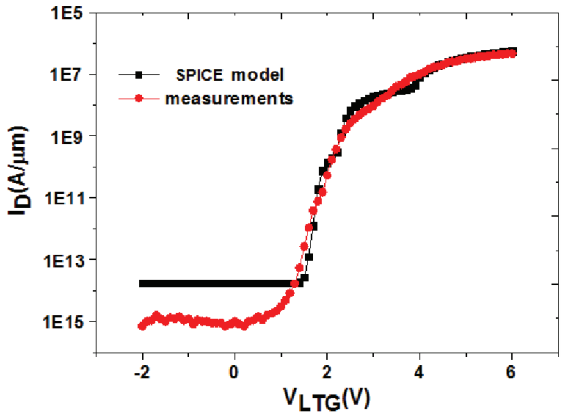

Fig. 22 Caractéristiques des courbes $I_D(V_{LTG})$ obtenues à partir des simulations SPICE et des mesures électriques pour W_L/L = 0.32 µm/0.35 µm, V_{DS}=50mV, V_G = -2V.

Nous pouvons observés trois pics qui sont présents pour les résultats de simulations ainsi que les résultats des mesures expérimentales. Ces pics correspondent à une tension de seuil et une largeur du transistor différentes. Pour obtenir les mêmes pics observés sur la courbe expérimentale, nous avons ajusté la tension de seuil pour chaque transistor à une longueur de grille latérale donnée. Ensuite, nous avons déterminé la largeur du chaque transistor. Pour un transistor à grille latérale, la largeur totale (W_L) dépend de la largeur de chaque transistor, donc l'équation (VII) peut être formulée comme suit:

$$W_L = W_1 + W_2 + W_3 = 2 * h = 0.32 \text{ µm} \quad \text{(VII)}$$

Tableau 1 présente les résultats de l'extraction.

Transistor*	$W_{1,2,3}$ [m]	V_{TH} [V]
TN1	$3.31x10^{-7}$	3.5V
TN2	$1.82x10^{-8}$	2.2V
TN3	$9.9x10^{-11}$	1.8V

* Les termes TN1, TN2, TN3 désignent les transistors à grille latérale présentés sur la figure 21.

En se basant sur les résultats extraits à partir des mesures et l'équation (VII), les calculs estiment une valeur de la largeur du transistor à grille latérale à W_L = 0,3 µm, ce qui correspond à la valeur standard (W = 0,32 µm). Ainsi, l'erreur relative est de seulement 6,25 %. A partir du tableau III - 5, nous observons que la largeur de canal extraite pour le transistor TN3 est significativement faible, même irréaliste.

5. Conclusion

En résumé, la structure multi-grilles a été examinée par les différentes méthodes de caractérisation ainsi que par la simulation TCAD et la modélisation SPICE. La mesure des caractéristiques *I-V* a permis de déterminer des paramètres importants tels que la tension de seuil (V_{TH}) et la pente sous le seuil (S). Les caractéristiques du transistor à grille surfacique ont été comparées avec ceux du NMOSFET conventionnel fabriqué sur la même plaquette. Nous avons observé que le transistor à grille supérieure présente un comportement électrique similaire au transistor conventionnel, par conséquent, il peut être considéré comme un transistor standard. En plus, il a été découvert que la tension de seuil du transistor surfacique est accordable avec la polarisation de la grille latérale. L'estimation comparative a également été effectuée entre le transistor à grille surfacique et le transistor à grille latérale. Les résultats ont révélé que la grille latérale présente un comportement multi-seuil, à l'encontre de la grille du transistor supérieur.
Par la méthode split *C-V*, la mobilité effective a été déterminée. Les résultats ont révélé que la mobilité du transistor à grille surfacique est comparable avec celle du NMOSFET conventionnel. La mobilité diminue avec une augmentation de la surface du transistor. Par le pompage de charge à deux et à trois niveaux, l'extraction de la densité moyenne des pièges de l'interface Si/SiO_2 a été effectuée. Nous avons remarqué que l'interface du canal de transistor à grille surfacique a une meilleure qualité que celle du transistor à grille latérale. En outre, sa distribution de densité moyenne et de l'énergie est comparable à celle du transistor NMOSFET conventionnel.
Le modèle 3D TCAD a été construit pour l'analyse du transistor multi-grilles. Les caractéristiques électriques telles que la tension de seuil de grille surfacique (0.59V), la pente sous le seuil (autour de 90 mV/déc), ont été vérifiées. L'ajout d'une densité moyenne de pièges à l'interface Si/SiO_2 a permis d'analyser l'impact de ces pièges sur les caractéristiques *I-V*. Les pièges de type donneur avaient une plus grande influence sur les caractéristiques *I-V* que les pièges de type accepteur. Les résultats de modélisation ont été comparés avec les résultats expérimentaux et ont montré une bonne qualité de l'interface Si/SiO_2 au niveau de la grille supérieure.

Un modèle SPICE équivalent du transistor à grilles multiples a été proposé. Tout d'abord, le modèle de grille supérieure a été développé. Ensuite, le transistor à grille latérale a été modélisé

par trois transistors en parallèle avec différents paramètres internes. En adaptant les simulations SPICE à des données expérimentales, la tension de seuil et la largeur de la grille latérale ont été ajustées. Ces paramètres ont permis de reconstruire les caractéristiques de la grille latérale avec trois bosses associées à trois tensions de seuil.

En ce qui concerne les perspectives de notre travail, nous pourrions proposer des analyses de bruit afin de quantifier le transport dans le canal et de compléter nos résultats expérimentaux concernant les défauts électriquement actifs. Avec notre modelé de transistor multi-grilles proposé, l'étape prochaine sera l'amélioration du modèle latérale pour obtenir les caractéristiques appropriées. Le modèle amélioré pourrait être applique aux circuits logiques. En se basant sur les résultats obtenus de caractérisations électriques et simulations TCAD, il serait possible de procéder à l'analyse dynamique du transistor MOS pour proposer un modelé complet en VHDL-AMS. Ensuite, des analyses DC permettraient de connaitre la consommation d'énergie et ses limites, tandis que l'analyse transitoire montrerait l'instabilité du circuit.

En développant tous les pointes mentionnées, il sera possible de créer avec la structure NMOSFET multi-grille des circuits analogiques tels que des amplificateurs ou oscillateurs contrôle en tension.

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