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Etude thermomécanique expérimentale et numérique d'un module d'électronique de puissance soumis à des cycles actifs de puissance

Camille Durand

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Camille Durand. Etude thermomécanique expérimentale et numérique d'un module d'électronique de puissance soumis à des cycles actifs de puissance. Génie mécanique [physics.class-ph]. Université de Valenciennes et du Hainaut-Cambresis, 2015. Français. NNT : 2015VALE0007 . tel-01153609

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Thèse de doctorat

**Pour obtenir le grade de Docteur de l'Université de
VALENCIENNES ET DU HAINAUT-CAMBRESIS**

En génie mécanique

Présentée et soutenue par Camille DURAND. Le 23/01/2015, à Valenciennes

N° d'ordre : 15/02

Ecole Doctorale :

Science pour l'Ingénieur (SPI)

Equipe de recherche, Laboratoire :

Laboratoire d'Automatique, de Mécanique et d'Informatique Industrielles et Humaines (LAMIH)

**Etude thermomécanique expérimentale et numérique d'un module
d'électronique de puissance soumis à des cycles actifs de puissance**

**Thermo-mechanical study of a power module under Active Power
Cycling by means of experiments and simulations**

JURY

Président du jury

- Ponthot, Jean-Philippe. Professeur, Université de Liège. Liège, Belgique.

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Acknowledgments

This work was realized in cooperation between the company Robert Bosch GmbH, Automotive Electronics, department for Engineering Technology Electronic Control Units in Reutlingen, Germany and the L.A.M.I.H (Laboratoire D'Automatique, de Mécanique et D'Informatique Industrielles et Humaines), UMR CNRS 8201, University of Valenciennes, France. Therefore I am grateful to all the colleagues and people who helped me during those three years.

I would especially like to thank Prof. Daniel Coutellier and Dr. Markus Klingler for the supervision of my work and their precious remarks.

Many thanks also to Prof. Hakim Naceur for his appreciated comments and suggestions.

I am also thankful to Dr. Peter Wolfangel head of the department Engineering Technology Electronic Control Unit and to Dr. Bernd Hohenberger, current group leader who gave me the possibility to carry out this work.

I would also like to express my gratitude to the whole AE/ETC group for their priceless support as well as the excellent working atmosphere. Among all my colleagues, I would like to especially thank the other PhD students, Mr. Thorsten Gross, Mr. Sebastian Jobst, Mrs. Alicja Palczynska, Mrs. Tanja Wolfer and Mr. Gaiser Patrick, for the numerous interesting discussions and for their help concerning the everyday German life. My gratitude goes also to my Ansys user's colleagues, Ms. Valiantsina Kramer-Sinzinger and Dr. Przemyslaw Gromala, for their precious simulation's advice.

I also want to thank Mr. Arian Grams and Dr. Olaf Wittler from the Fraunhofer IZM Berlin for their help concerning the fracture mechanics simulations.

Last but not least, I would like to thank my family and friends for their support along those three years and their permanent encouragement.

Reutlingen, December 2014

Camille Durand

Abstract

Today a point has been reached where safe operation areas and lifetimes of power modules are limited by the standard packaging technologies, such as wire bonding and soft soldering. As a result, further optimization of used technologies will no longer be sufficient to meet future reliability requirements. To surpass these limits, a new power module was designed using Cu clips as interconnects instead of Al wire bonds. This new design should improve the reliability of the module as it avoids wire bond fatigue failures, often the root cause of device failures. The counterpart for an improved reliability is a quite complicated internal structure. Indeed, the use of a Cu clip implies an additional solder layer in order to fix the clip to the die. The thermo-mechanical behavior and failure mechanisms of such a package under application have to be characterized. The present study takes advantage of numerical simulations to precisely analyze the behavior of each material layer under power cycling. Furthermore an experimental and numerical sensitivity study on tests parameters is conducted. Critical regions of the module are pointed out and critical combinations of tests parameters for different failure mechanisms are highlighted. Then a fracture mechanics analysis is performed and the crack growth at different locations is analyzed in function of different tests parameters. Results obtained enable the definition of lifetime prediction models.

Keywords: power module, MOSFET, Cu clip, solder, Al metallization, chip, intermetallics, thermo-mechanics, FEM simulations, passive temperature cycling, Active power cycling, failure mechanisms, sensitivity study, fracture mechanics, CTOD, VCCT, lifetime, reliability

Zusammenfassung

Die Zuverlässigkeit und Lebensdauer von Leistungsmodulen hängt heutzutage im Wesentlichen von der verwendeten Aufbau- und Verbindungstechnik wie Al-Drahtbondtechnik und Löten ab. Um zukünftige Zuverlässigkeitsanforderungen zu erfüllen reicht es nicht aus die bestehenden Technologien weiterzuentwickeln, vielmehr müssen ganz neue Konzepte der Aufbau- und Verbindungstechnik entwickelt werden. In dieser Arbeit wird ein Modul betrachtet, in dem die oberseitige Drahtbondtechnik durch einen aufgelöteten Cu-Clip ersetzt wurde. Dieses neue Design soll die Zuverlässigkeit verbessern, indem ein Versagen der Drahtbonds vermieden wird, welches oft die Hauptursache für den Ausfall des Moduls ist. Die neue Technologie erfordert den Einsatz eines Cu-Clips, einer zusätzlichen Lotschicht und einer lötbaren Chipmetallisierung. Das thermomechanische Verhalten und die Schadensmechanismen während des Betriebs eines solchen Moduls müssen charakterisiert werden. Diese Arbeit nutzt die Vorteile der numerischen Simulation, um das Verhalten jeder Materialschicht unter aktiven Temperaturwechseln genau zu analysieren. Außerdem wird eine experimentelle und numerische Sensitivitätsanalyse für die Testparameter durchgeführt. Kritische Bereiche des Moduls werden aufgezeigt und kritische Testparameterkombinationen für verschiedene Schadensmechanismen hervorgehoben. Danach wird eine mechanische Analyse mit bruchmechanischen Konzepten durchgeführt und die Beanspruchung an der Riss Spitze an verschiedenen Stellen im Bauteil in Abhängigkeit von verschiedenen Testparametern analysiert. Die gewonnenen Ergebnisse ermöglichen die Herleitung eines Lebensdauermodells für den aktiven Betrieb.

Stichwörter: Leistungsmodul, MOSFET, Cu-Clip, Lot, Al-Metallisierung, Chip, Intermetallische Phasen, thermomechanisch, FEM-Simulation, Passive Temperaturwechsel, Aktive Temperaturwechsel, Schadensmechanismus, Sensitivitätsanalyse, Bruchmechanik, CTOD, VCCT, Lebensdauer, Zuverlässigkeit

Resumen

Hoy en día la vida útil de un módulo electrónico de potencia está limitada por las técnicas estándar de envase, como el cableado y el soldadura. Así una optimización de las técnicas actualmente empleadas no será suficiente para satisfacer las futuras exigencias de fiabilidad. Para superar estos límites ha sido desarrollado un nuevo módulo de potencia sustituyendo los cables de conexión por clips de cobre. Este diseño innovador apunta a mejorar la fiabilidad del módulo, puesto que él impedía la degradación de los cables de conexión, la cual constituía a menudo la principal fuente de fallos. La contrapartida de esta ganancia de fiabilidad reside en la complicación de la estructura interna del módulo. Efectivamente el empleo de un clip de cobre necesita una soldadura suplementaria fijando el clip sobre el chip. Así, el comportamiento termomecánico y los diferentes modos de ruptura aquella el componente es sometido durante su utilización, deben ser caracterizados. Este estudio utiliza la simulación numérica para analizar con precisión el comportamiento de cada capa de material durante los ciclos activos de potencia. Además, un estudio de sensibilidad a la vez experimental y numérico relativo a los parámetros de test esta realizado. Las zonas críticas del módulo así que las combinaciones críticas de parámetros de test por diferentes modos de fallos son puestos en evidencia. Por otro lado, un análisis mecánico de la ruptura se lleva a cabo y la propagación de las fisuras a diferentes zonas claves están analizados en función de los diferentes parámetros de test. Los resultados obtenidos permiten la definición de modelos de predicción de la vida útil.

Palabras claves: Módulo electrónico de potencia, MOSFET, Cu clip, soldadura, Al metalización, chip, intermetálicos, termo-mecánica, FEM simulación, Ciclo Pasivo de Temperatura, Ciclo Activo de Potencia, mecanismo de ruptura, análisis de sensibilidad, mecánica de la ruptura, CTOD, VCCT, vida útil, fiabilidad

Résumé

De nos jours, la durée de vie des modules d'électronique de puissance est désormais limitée par les technologies standards de conditionnement, telles que le câblage par fils et le brasage. Ainsi une optimisation des technologies actuellement employées n'est pas suffisante pour satisfaire les futures exigences de fiabilité. Pour dépasser ces limites, un nouveau module de puissance remplaçant les fils de connexion par des clips en cuivre a été développé. Ce design innovant vise à améliorer la fiabilité du module puisqu'il empêche la dégradation des fils de connexion, constituant bien souvent la principale source de défaillance. La contrepartie de ce gain de fiabilité réside dans la complexification de la structure interne du module. En effet, l'emploi d'un clip en cuivre nécessite une brasure supplémentaire fixant le clip à la puce. Ainsi, le comportement thermomécanique et les différents modes de rupture auxquels le composant est soumis lors de son utilisation doivent être caractérisés. Cette étude utilise la simulation numérique pour analyser avec précision le comportement de chaque couche de matériaux lors des cycles actifs de puissance. De plus, une étude de sensibilité à la fois expérimentale et numérique concernant les paramètres de tests est réalisée. Les zones critiques du module ainsi que les combinaisons critiques des paramètres de tests pour les différents modes de rupture sont mis en évidence. Par ailleurs, une analyse en mécanique de la rupture est conduite et la propagation des fissures à différentes zones clés est analysée en fonction des différents paramètres de tests. Les résultats obtenus permettent la définition de modèles de prédiction de durée de vie.

Mot clés : module de puissance, MOSFET, Cu clip, brasure, Al métallisation, puce, intermétalliques, thermomécanique, FEM simulations, Cycle Passif de Température, Cycle Actif de Puissance, mécanismes de rupture, analyse de sensibilité, mécanique de la rupture, CTOD, VCCT, durée de vie, fiabilité

Notations and abbreviations

Notations

C_{th}	Thermal capacitance
$CTOD_I$	CTOD for mode I
$CTOD_{II}$	CTOD for mode II
d_{bond}	Bond thickness
ΔT_{amb}	Ambient temperature swing
ΔT_c	Case temperature swing
ΔT_j	Junction's temperature swing
$\epsilon_{acc\ creep}$	Accumulated creep strain in 1 cycle
G_I	Opening mode energy release rate
G_{II}	Shearing mode energy release rate
I_d	Exact drain current
I_{GES}	Gate emitter short
I_{load}	Loading current
I_{DS}	Drain to source current
I_{DSleak}	Drain to source leakage current
I_{GSleak}	Gate to source leakage current
I_{meas}	Measuring current
N_f	Number of cycles to failure
P_v	Power losses
R	Radius of curvature
R_{DSon}	Drain to source on state resistance
R_{th}	Thermal resistance
R_{th-jc}	Junction to case thermal resistance
T_c	Case temperature
T_g	Glass transition temperature
T_{HC}	Heat sink temperature
T_j	Junction temperature
T_{jmin}	Minimum junction temperature
T_{jmax}	Maximum junction temperature
T_m	Melting point in Kelvin
t_{on}	Power-on-time or pulse width or heating time
t_{off}	Power-off-time
V_{DS}	Drain to source voltage
V_{ce}	Collector emitter voltage
V_{cesat}	Collector emitter saturation voltage
V_{GS}	Gate to source voltage
V_f	Forward voltage of the body diode
Z_{th}	Thermal impedance

Abbreviations

AC	Alternating Current
Acc	Accumulated
APC	Active Power Cycling
BEM	Boundary Element Method
BJT	Bipolar Junction Transistor
BKIN	Bilinear Kinematic Hardening
CTE	Coefficient of Thermal Expansion
CTOD	Crack Tip Opening Displacement
CTS	Compact Tension Shear
CZE	Cohesive Zone Element
DBB	Danfoss Bond Buffer

DC	Direct Current
DCB	Direct Copper Bonding
DICM	Differential Interference Contrast Microscope
DMOS	Double-Diffused MOS
DoE	Design of Experiment
DUT	Device Under Test
EMC	Epoxy Molding Compound
EoL	End of Life
EoT	End of Test
ERR	Energy Release Rate
FCOB	Flip Chip On Board
FE	Finite Element
FEM	Finite Element Method
FIB	Focused Ion Beam
GTO	Gate Turn Off Thyristor
HDTMOS	High Density TMOS
IGBT	Isolated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
IMC	Intermetallic
JFET	Junction Gate Field-Effect Transistor
LTJT	Low Temperature Joining Technique
MCT	MOS Controlled Thyristor
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NP	Neutral Point
OM	Optical Microscope
PBGA	Plastic Ball Grid Array
PCB	Printed Circuit Board
PQFN	Power Quad Flat No Lead
PTC	Passive Temperature Cycling
PWM	Pulse Width Modulation
REM	Reflection Electron Microscope
RoHS	Reduction of Hazardous Substances
SAC	Sn Ag Cu solders material
SAM	Scanning Acoustic Microscope
SEM	Scanning Electron Microscope
SOA	Safe Operating Area
TEM	Transmission Electron Microscope
TIM	Thermal Interface Material
TRIAC	Triode for Alternating Current
TRS	ThermoRheologically Simple
TSP	Thermo-Sensitive Parameter
VCCT	Virtual Crack Closing Technique
WLF	Williams-Landel-Ferry

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Introduction

In the automotive industry, requirements for compactness and reliability are always increasing when it comes to power electronic modules. Today a point has been reached where the operation area and lifetime of power modules are limited by the standard packaging technologies, such as wire bonding and soft soldering. As a result, a further optimization of the used technologies will not be sufficient to meet the future reliability requirements. To surpass these limits new packaging technologies have to be developed. That is why a new designed module using wire bondless contacts and double sided soldering was developed. Indeed, a Cu clip soldered on the top of the chip is used as interconnect instead of wire bonds. This wire bondless contacts technology in combination with the mold package significantly increases the reliability of the chip connections. The solder joint also improves the heat transfer from the switches through the lead frame to the exposed area at the bottom of the module and through an insulating layer to the heat sink. Furthermore this module replaces 6 discrete MOSFETs switches and allows for tighter packing within a control unit. But, as this package has a completely different structure than standard modules, no knowledge are available concerning the behavior of this new module under working conditions. Thus the behaviors of the module and its failure mechanisms have to be characterized.

Electronic devices used in the automotive industry are mainly subjected to thermo-mechanical loads. These loads originate from both Passive Temperature Cycling (PTC) and Active Power Cycling (APC). Passive Temperature Cycling (PTC) is induced by the variations of the surrounding thermal environment in which the power module is placed. Active Power Cycling (APC) is obtained when thermal losses are generated inside power chips by conducting high currents or by switching the current on and off. Active Power Cycling (APC) can be distinguished from Passive Temperature Cycling (PTC) as the heating source differs: in APC the chip is the internal heating source (active) whereas in PTC the heating source comes from its environment (passive). Thus, the temperature distribution in the device is also different: the temperature is spatially not homogeneously distributed under APC whereas for PTC the temperature of the module is uniform. The effects of PTC were already extensively studied and the resulting failure mechanisms are quite well understood. The principal degradation induced by PTC is solder fatigue which led to the apparition of cracks, and delamination at solder joints. But the failure mechanisms occurring under APC are not characterized that well. Moreover the failure mechanisms are also strongly dependent on the tests parameters used for APC, like the minimum junction temperature T_{jmin} , the temperature swing ΔT_j , and the power-on-time t_{on} . Thus the module behavior under APC should be studied in detail and the influence of the test parameters should be taken into account.

Performing APC tests is necessary to be able to observe the different degradation phenomena occurring in the module and measure the resulting electrical and thermal consequences. But testing a high number of cycles requires long test times of the order of several months. This implies that testing of a wide range of application condition is not feasible. Moreover it is not possible to monitor the evolution of mechanical stresses and strains inside the package during APC. Thus it is not possible to study thoroughly the influence of tests parameters on the reliability of power modules solely with experiments. To overcome these experimental difficulties and analyze the behavior of power modules under varying test conditions, numerical simulation can be considered as an interesting tool. Indeed, with simulation, once a model is set up and validated, it is quite easy to modify some parameters and restart an analysis. This easy reproducibility of an analysis added to the rapidity of calculation allows an extensive numerical study on the influence of test parameter on reliability to be carried out. Furthermore, simulations provide information regarding the spatially and temporarily evolution of temperature and mechanical stresses and strains in the module. Thus it significantly helps to understand the failure mechanisms that are occurring in the module. That is why combining APC tests with numerical simulations, appears to be the best strategy in order to gain knowledge about the physics of failure in the module.

The main goal of this study is to understand the thermo-mechanical behavior of the new power package using a Cu clip as interconnect instead of Al wire bonds. Therefore, APC tests and more extensively simulations based on Finite Element Methods (FEM) are used to characterize the influence of three test parameters (T_{jmin} , ΔT_j and t_{on}) on the reliability of this new power module. A detailed model of the power package is developed and the behavior of all material layers is analyzed. In addition, fracture mechanics simulations are performed for regions of the module that were found to be subjected to cracking.

After this brief introduction, the first chapter details the different failure mechanisms occurring in standard power modules and reports the new technologies developed to restrain the apparition of failure mechanisms and thus increase the reliability of power modules. Then, a review of publications dealing with APC tests and simulations gives an overview regarding the types of modules tested, the test conditions and the analysis methods used as well as the goals reached in the APC studies published until now. Chapter 2 presents the module under study and the material properties used in the simulation models. A thermal pre-study of the module is carried out in chapter 3 and based on the results obtained, a Design of Experiment (DoE) is defined. The APC test stand is described in chapter 4 as well as the electrical and thermal measurements followed by the microscopic analysis, which allow for failure detection. Degradations observed for each layer are analyzed and eventually correlated to modifications in electrical or thermal parameters. Based on the information gathered it was possible to define an End of Life criterion and to predict the lifetime of the module in function with the test parameters. Chapter 5 presents the models used for the thermo-mechanical simulations. Results obtained under PTC for the 3D and the 2D models are compared in order to validate the 2D model. Attention is paid to detail the behavior of each important layer under PTC and APC. Then, the results of the sensitivity study on test parameters are analyzed. The sensitivity study is even extended and some special cases with longer power-on-time t_{on} , or different power-off-time t_{off} , or large ΔT_j , or thick Cu lead frame or with cracks and delamination in mold were studied. Fracture mechanics simulations were also performed to complete the sensitivity study on test parameters. Chapter 6 presents the models with the 3 cracks defined and describes the fracture criteria used to interpret cracks growth. Results obtained for the different cracks under PTC and APC are shown as well as the results of the sensitivity study. Results obtained with experiments are combined to the results obtained through simulations in chapter 7. The main failure mechanisms are highlighted and the most critical test parameters are detailed for each failure mechanism. Lifetime models were deduced by correlating the experimentally obtained lifetime with the corresponding calculated deformations, stresses, or strains. Finally, the conclusion reviews the most important findings, as well as their consequences. It closes the thesis by suggesting some further investigations.

1 State of the art in the reliability of power modules under Active Power Cycling (APC)

1.1 Power electronics

Power modules (Figure 1.1) aim at converting electrical energy from one form to another in an efficient, clean, compact, and robust manner for convenient utilization. In modern systems the conversion is performed with semiconductor switching devices such as diodes, thyristors and transistors. First transistors were created in 1950, and since then new types of modules have been developed: GTO (Gate Turn Off Thyristor), BJT (Bipolar Junction Transistor), IGBT (Isolated Gate Bipolar Transistor), IGCT (integrated Gate Commutated Thyristor), MCT (MOS Controlled Thyristor), MOSFET (Metal Oxide Semiconductor Field Effect Transistor)...

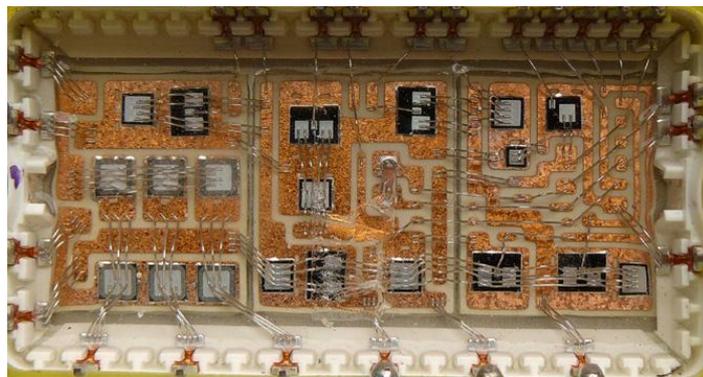


Figure 1.1 : Top view of a power module with IGBT chips [Tou10]

Converters are being used over a wide power range, with ratings from milliwatts up to gigawatts. Depending on required voltage and current ratings of the power semiconductors, different types of power semiconductors are being used, see Figure 1.2. Nowadays IGBT and MOSFET are preferred semiconductors for automotive applications.

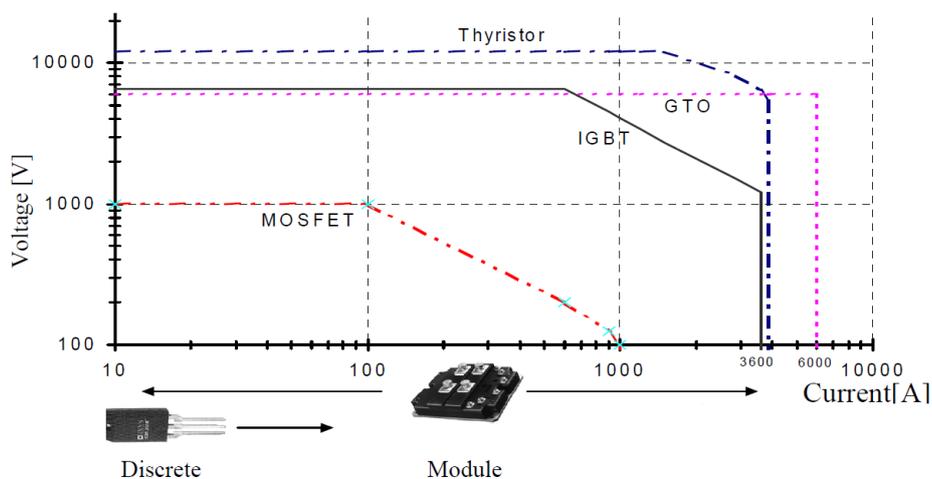


Figure 1.2 : Power levels of power electronic components [Lut11]

1.1.1 MOSFET and IGBT semiconductors

1.1.1.1 MOSFET

The Power MOSFET appears in 1976, and is a transistor used for amplifying or switching electronic signals. It is an electronic switch, which lock or ignition is controlled by a voltage: it behaves like a door that can be opened or closed at will. The power MOSFET is a unipolar component as it uses only one type of charge carrier. The basic principle is based on the effect of the electric field applied to the polycrystalline silicon semiconductor which is to say, the gate electrode, the insulator (silicon dioxide) and the semiconductor layer (called “substrate”). When the potential difference between the gate and the source is zero, nothing happens. With the increase of the potential difference the free charges in the semiconductor are pushed away from the junction semiconductor/oxide, first creating a zone known as “depletion” and when the difference potential is large enough it is an area of “inversion”. This inversion zone is an area where the type of charge carriers is opposite to the rest of the substrate, thereby creating a “channel” of conduction. The transistor is characterized by the burden of its majority carriers that determines whether it is a P or N type.

The power MOSFET technology has mostly reached maturity and is the most popular device for applications where high switching frequencies are desired but operating voltages are low. Its main drawback is that at the conductive state it behaves like a resistor ($R_{DS(on)}$) of tens of $m\Omega$, which generates conduction losses and therefore restricts its wider application.

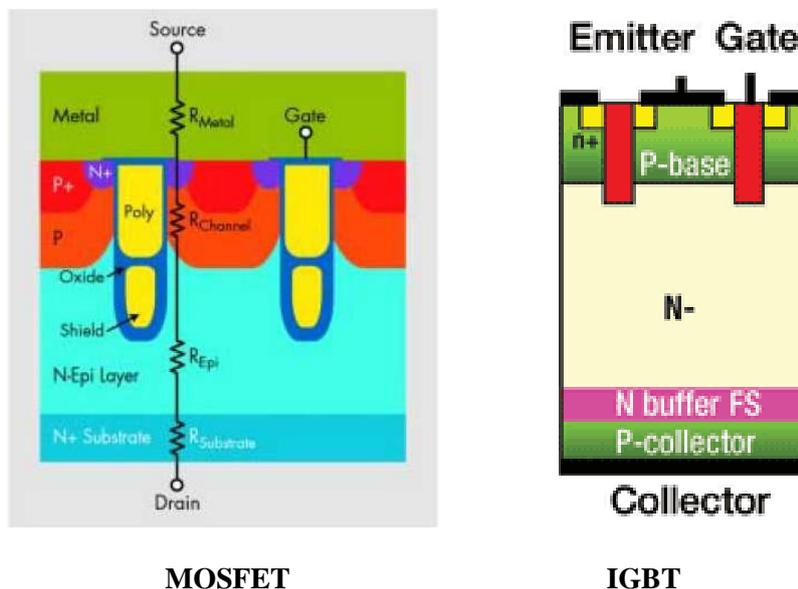


Figure 1.3: Schema of a trench MOSFET with added shield electrode on the left [Kang12] and a Field stop trench IGBT on the right [Sny10]

1.1.1.2 IGBT

The IGBT appears in 1982 and combines the simple gate drive characteristics of the MOSFET with the high current and low-saturation-voltage capability of bipolar transistors by combining an isolated gate FET for the control input, and a bipolar power transistor as a switch, in a single device. An IGBT cell is constructed similarly to a n-channel vertical construction power MOSFET (Figure 1.3) except the n+ drain is replaced with a p+ collector layer, thus forming a vertical PNP bipolar junction transistor. Since the 1990's, the IGBT is one of the most popular device for medium-to-high power applications such as switched mode power supplies traction motor control and induction heating [Lut11].

1.1.2 Power module design

Power modules are complex multilayered structures consisting of different materials. Since the emergence of IGBTs and MOSFETs, one can consider that there are two main standard module designs in power electronic for packages capable of housing multiple chips per electrical function in parallel: Direct Copper Bonding (DCB) based modules and lead frame based module.

1.1.2.1 DCB based modules

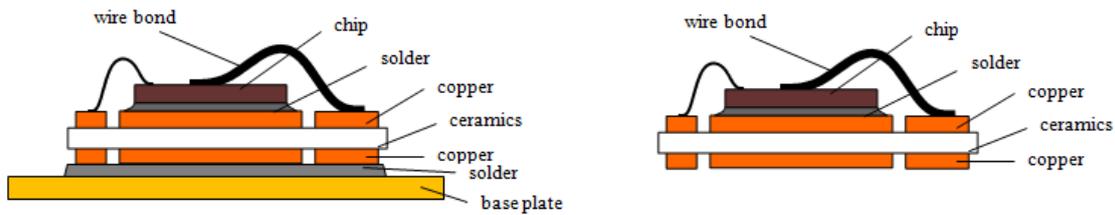


Figure 1.4: Internal structure of a DCB based module with a base plate on the left and without base plate on the right

First, there is the chip, made of silicon and which represents the active part of the module. The electrical connection of the chip is usually achieved by aluminum wire bond ultrasonically welded on the top side of the chip. The bottom side of the chip is soldered on the upper copper metallization of the DCB. The DCB allows a good adhesion of thin copper layers (200-300 μm) on ceramic surfaces. The ceramic is usually made of aluminum oxide Al_2O_3 or aluminum nitride AlN . The AlN is more advantageous: its thermal conductivity is 7 times higher than for Al_2O_3 , and its Coefficient of Thermal Expansion (CTE) is almost 2 times lower. Thus the AlN will have a better resistance to thermal shock and temperature gradient between the different layers of the modules will be consequently reduced (about 50%). Ceramic assure the electrical isolation and the dissipation of the heat flux generated by the chip. Then, there are 2 variants (Figure 1.4): one with a based plate and one more recent without base plate. In the first version, the DCB is mounted on a metallic base plate, usually made of copper, which maintains the module on the heat sink through thermal paste. This construction is found in 70-80% of all power modules produced by European manufacturers (Infineon, Semikron, IXYS, Danfoss, Dynex) and is also common in modules produced by Asian manufacturers. In the second version, there is no base plate, and the DCB is directly mounted on the heat sink through a thermal paste. This solution shows better thermal performances and avoids the stress inductance caused by the CTE mismatch between the ceramic and the base plate. Those packages with the chip soldered on a DCB are usually not encapsulated by a mold. The solder material used to join the chip on the DCB or the DCB on the base plate, were initially lead containing solder (like the $\text{Sn}_{63}\text{Pb}_{37}$ known for its low melt temperature 183°C), but are now replaced by lead free solder because of the Reduction of Hazardous Substances (RoHS) legislation. Lead free solders widely used are solder alloys called SAC and containing tin, silver and copper (for example SAC387, $\text{SnAg}_{3.8}\text{Cu}_{0.7}$).

1.1.2.2 Lead frame based modules

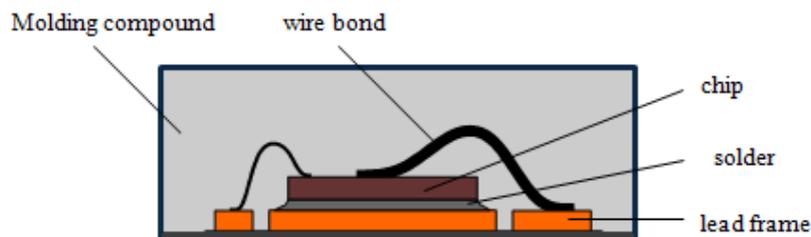


Figure 1.5: Internal structure of a lead frame based module

In these packages, the chip is soldered on a metal lead frame, mostly made of a copper alloy, which presents the electrical contact of the bottom side of the chip, where the top side connection is established by aluminum bond wires. As for DCB based packages, solder materials used to join the chip on the lead frame are lead free solders. To ensure the electrical isolation and the mechanical protection of chips, and dissipate the heat generated, the subassembly, excepting the lead frame, is transfer molded by a plastic molding compound [Liu12]. The package is then mounted on the heat sink through thermal paste. This internal structure (Figure 1.5) is used in the discrete power devices of the TO- family. Power devices of TO cases are widely used in low and middle power applications like DC/DC and AC/DC converters.

1.2 Working conditions

Traditionally, power modules are used for electrical traction but nowadays it is also widely used for household electrical appliances, laptop, cell phone, and in the automobile industry for hybrid and electrical cars. In this study the focus is set on power modules used for automobile applications.

Under working conditions, thermal stresses arise in power modules. These stresses are originating from Active Power Cycling (APC) and Passive Temperature Cycling (PTC). Active Power Cycling (APC) is obtained when thermal losses are generated inside power chips by conducting high currents or by switching the current on and off. Passive Temperature Cycling (PTC) is induced by the variations of the surrounding thermal environment in which the converters are placed. Power converters used in transport applications typically undergo both cycling modes (Figure 1.6), with different levels of temperature swings and frequency. Under APC, the temperature range on chips is typically situated between 20°C and 60°C. Simultaneously power modules can be submitted for a few cycles with ambient temperatures that can vary over a very broad range: around -40°C in cold ground zones to 120 °C near engines. Power modules used for transport applications are specified for maximum operating temperatures of 150-175°C. In terms of lifetime, automobile industry requires power devices capable to operate 8000 hours in a thermal nominal environment of 90°C which can increase up to 120°C and about 400 thousands of power cycles [Ber98].

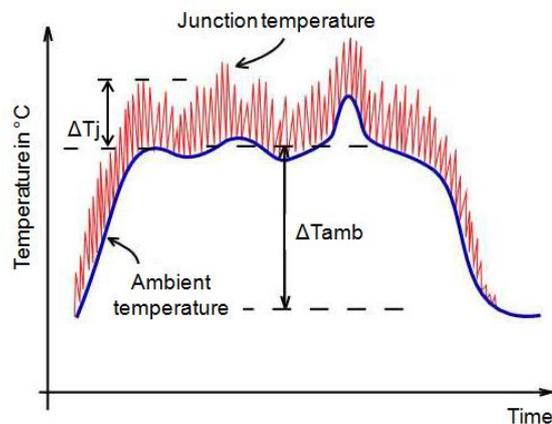


Figure 1.6: Schematic of temperature cyclic loading in service [Bou08]

1.3 Failure mechanisms

Abundant literature deals with failure mechanisms occurring in power modules made of MOSFETs or IGBTs and which are submitted to PTC or APC. About 65% of failures occurring in power modules are due to thermo-mechanical phenomena. The main failure mechanisms that are taking place are:

- Bond wire fatigue
- Aluminum reconstruction and ratcheting
- Solder voids and solder fatigue
- Delamination at the interface Mold/Copper
- Chip cracking

1.3.1 Bond wire fatigue

Bond wires are often reported as the weakest component of power modules, responsible of the device failure [Cia02, Coq03, Lef00]. Emitter bond wires have usually a diameter of 300-500 μm, and are bonded onto the active area of semiconductor devices. Therefore, they are exposed to almost the full temperature swing imposed by both the power dissipation in the silicon and the ohmic self heating of the wire itself.

The bond wire lift-off failure is caused by the CTE mismatch between the silicon of the chip (2,8 ppm/K) and the aluminum wire (23,5 ppm/K). The expansion and contraction of the Al is roughly 8 times higher than that of the Si. As both materials are joined together, strains occur in Si and in Al. But Al is a ductile material, so plastic strain accumulates and after a number of cycles, the interface is destroyed and the wire lifts off. The

crack leading to the failure is initiated from either end of the interconnected area and propagates within the wire material towards the center of the bond (Figure 1.7) [Goe10, Yam07].

The failure of a single or of multiple bond wires causes a change either in the contact resistance or in the internal distribution of the current, such that it can be traced by monitoring the collector-emitter saturation voltage V_{CEsat} in case of an IGBT [Cov97]. Indeed, the current load for the remaining wires will increase, leading to more self heating and a further increase in the temperature excursions and an acceleration of the degradation process. If all wires have lifted off, the current capability of the remaining wires is exceeded and the device will fail [Gla04, Goe10].

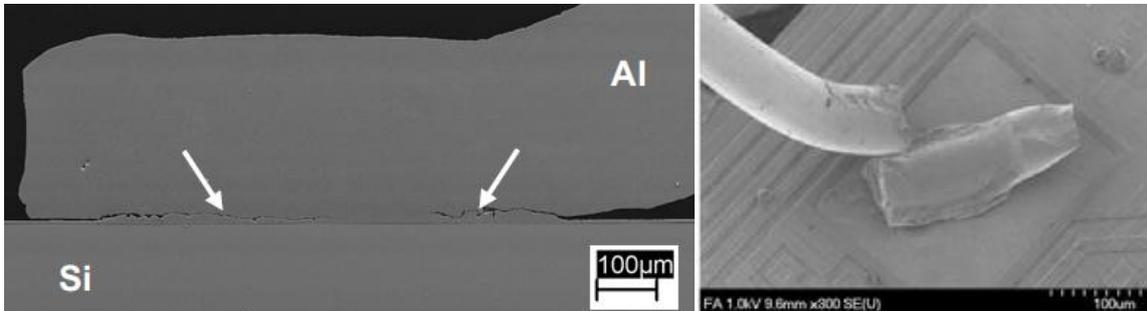


Figure 1.7: On the left, a cross-section of a bond showing cracks growing from either end of wire towards the center of the bond [Goe10]. On the right, wire bond lift-off on a chip pad [Scha06].

Bond wire heel cracking (Figure 1.8) are observed mainly after long endurance tests and can be promoted due to a non optimized ultrasonic bonding process [Cia02]. Indeed, during the bonding process, the heel region of wires already undergoes bending. Then, when the wire is subjected to temperature cycles it expands and it contracts, undergoing flexure fatigue. The displacement at the top of the loop can reach up to 25 μm per temperature cycle, thus producing a change in the bending angle at the heel. Repetitive heel bending generates cyclic plastic strain and thereby accumulated deformations leading to crack growth until the complete failure of the wire [Goe13].



Figure 1.8: Heel cracking [Cia02]

The reliability of wire bonds is affected by wire diameter, loop height, purity and manufacturing process. An increase in the wire diameter leads to an increase of plastic strain, thus it reduces the reliability. An increase in loop height increases the reliability. Wire diameter has a greater impact on reliability. A reduction in wire diameter will result in a reduction of its current carrying capability [Lu09].

There are two main technological countermeasures to face wire bond failures. On one hand, use molybdenum-aluminum strain buffers, mounted on top of the chip with the scope to eliminate thermo-mechanical fatigue by distributing the CTE mismatch of Al and Si across a thick layer. On the other hand, bond the wire with a coating layer.

1.3.2 Aluminum reconstruction and ratcheting

Aluminum metallization is a thin film of alloyed aluminum deposited onto the silicon substrate, forming bondable metal layer to establish electrical connections with the chip or with other chips via bond wires.

The reconstruction of the Al metallization was encountered in the early years of microelectronics [San69], but has begun to be studied only recently [Mal95, Cia96]. The Al reconstruction (Figure 1.9) is one of the most frequent failure mechanisms observed to affect mainly power modules, with bond wire lift-off and solder fatigue [Cia02].

The root cause for Al reconstruction is the same as for bond wire lift-off: the CTE mismatch between Si of chip and Al of metallization. This CTE mismatch is responsible for the generation of high compressive stress within the Al metallization during pulsed operation. This stress is likely to exceed by large the elastic limit. Under these circumstances, the stress relaxation can occur by grain boundary sliding, or by plastic deformation through dislocation glide, depending on temperature and stress conditions [Zha07]. Depending on the texture of the metallization, this leads either to the extrusion of the Al grains or to cavitation effects at the grain boundaries. A large amount of these plastic deformations leads to layer degradation with a subsequent open circuit. Reconstruction is more severe at the center of the chip, as the junction temperature reaches its maximum. At peripheral regions of the chip, where the maximum junction temperature does not exceed 110°C, the degradation is negligible [Cia96].

Surface reconstruction occurs sometimes as a secondary mechanism in conjunction with bond wire lift-off. Indeed, when one wire bond lifts off, the current has to be carried by the other bond wires, leading to an increase of the local temperature with consequent reconstruction of the metallization.

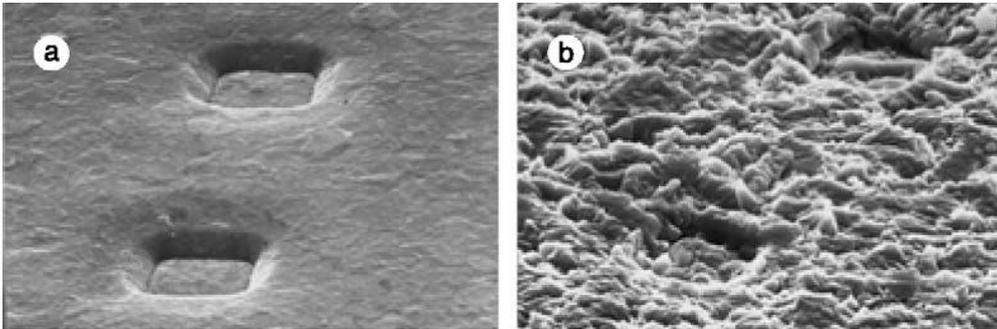


Figure 1.9: On the left, the emitter metallization of an IGBT chip before APC (a). On the right, the reconstructed emitter metallization after 3,2 millions of APC cycles between 85°C and 125°C (b). (SEM images) [Cia96]

Microscopically, the degradation of an Al layer sputtered on Si without any heat treatment, is characterized by 2 phenomena happening in parallel (Figure 1.10) [Mar10]:

- Intergranular cracking
- Grain size reduction

During heating phase, Al is under compression and its atoms emerge from the inner film through grain boundary and oxidize rapidly. They are forming hillocks. During cooling, the Al layer turns tensile and this causes grain boundary grooving, that is again stabilized by oxidation of bared Al surfaces. Repeating this grooving process leads to intergranular cracking with oxidized boundaries.

The division of initially large Al columnar grains may be attributed to regular dislocation processes. Dislocations move easily at relatively low temperature in the Al-metallization [Leg09]. Repeated cycles are then prone to accumulate dislocations in the Al grains and therefore create cells that will transform into grains when the added misorientations are sufficient. This classic recovery process is helped by mixed dislocation and diffusion processes such as dislocation climb. The degradation of the Al layer is thus a combined effect of accelerated diffusion at grain boundaries and division of initially large grains by dislocation-based plasticity. These Al degradations reduce the effective cross-section of the layer and result into an increase in the metallization resistance with time. This effect contributes to a linear increase of the on-state voltage V_{ce} (in case of an IGBT) as function of the number of power cycles [Gla04]. Although not easily measurable, the local drain-to-source on-state resistance R_{DSon} value of a transistor cell could also be considerably increased because of these cracks and ultimately create a hot spot responsible for a local melting of the Al layer and a failure of the chip [Mar09].

Polyimide passivation layer inhibits the Al extrusion, thus the use of a compressive over layers can be considered an effective countermeasure for controlling the increase of sheet resistance of metallization layer submitted to large temperature swings.

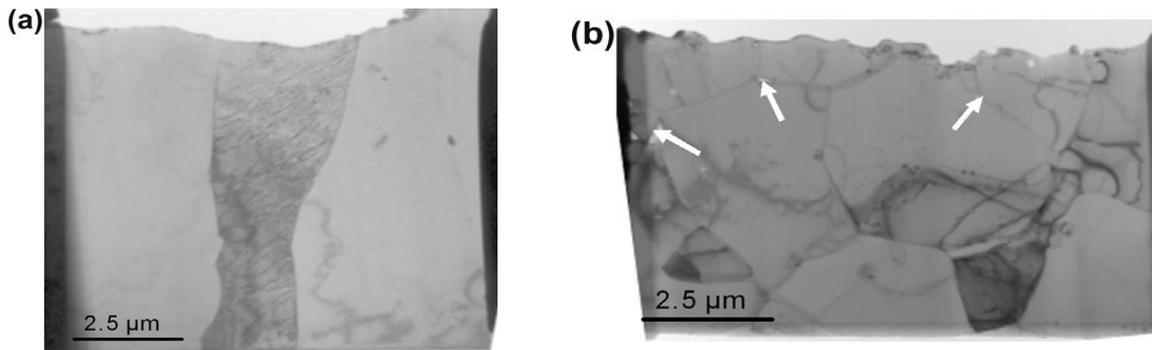


Figure 1.10: On the left, the Al metallization structure before APC test. Al grains have a columnar shape with a height equivalent to the layer thickness. (a) On the right, the Al metallization after 250 000 APC cycles at 85°C. Al grains are much smaller, with about 3-4 grains in the layer thickness. White arrows show some intergranular cracks. (b) (TEM images) [Mar10]

Another mechanism has been shown to induce Al extrusion: Al ratcheting [Kan09, Kan11, Smo08]. This ratcheting mechanism occurs because of the CTE mismatch between the Si (2,4 ppm/K) and the molding compound (~11 ppm/K). At high temperature, the CTE mismatch between mold and Si causes an in-plane compression in Al which goes beyond the elastic limit and therefore induces a plastic flow of the Al. Conversely, at low temperature, the CTE mismatch causes an in-plane tensile strain in Al followed by a plastic strain of the Al when the yield stress is reached. In addition, a constant shear stress, usually due to packaging, is acting on top of the Al, always into the same direction: from the edge to the middle of the chip [Hua00, Hua02]. Independently from the temperature excursion, it gives rise to a shear flow or tilting of the metal every time the yield stress is reached. Consequently, each temperature cycle gives rise to a tilting in the direction to the middle of the chip, which, for many cycles, sums up to considerable amounts. This phenomenon is called ratcheting [Suo03]. At the end, the Al film has totally yielded and is not able to transfer the shear stress to the adjacent layers anymore, similarly to a viscous fluid. If a silicon nitride film is overlaying the Al metallization, the stress will build up in this overlaying film, leading to cracks.

To avoid Al ratcheting in plastic encapsulated power devices, a series of papers [Alp09a, Alp09b, Alp09c] has evaluated the influence of the major components involved and consequently make suggestions to optimized power modules design (Figure 1.11). They found that the reliability of the Al metallization is affected by: the yield stress, the thickness and the Young's modulus of Al, the CTE and the thickness of the mold and the CTE of the passivation layer. So, first a new layered metallization material with a high yield stress was built up. Then, an appropriate molding compound is selected regarding its viscoelastic properties and its CTE. Finally, the geometry and the selection of passivation and die coating materials are optimized, taking into account their CTE properties. All these improvement steps have to be applied simultaneously, due to the interdependence of all components of the power module.

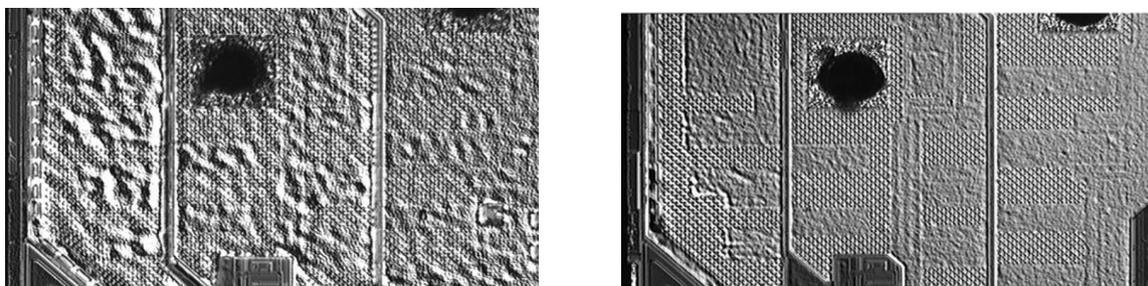


Figure 1.11: On the left, a 3,5 μm thick Al metallization observed after 1000 PTC cycles. On the right, a 6 multilayer Al metallization after 1000 PTC cycles.(Nomarski interference contrast microscopy) [Alp09a]

1.3.3 Solder voids and solder fatigue

Lead-free and lead-rich solder alloys used in power devices exhibit a CTE which is heavily mismatched with that of silicon and DCB or copper lead frame. Therefore, solder layers represents a critical interface in power assemblies, especially in the case of power modules with copper base plate. Degradation of solder joints can be categorized into: solder voids and solder fatigue.

A void is an empty volume in the solder layer and can be formed already during the joining process when e.g. the solder melts and releases oxides which float to the top of the drop and forms scum and bubbles. Voids can significantly increase the peak junction temperature of a power module and therefore accelerate the evolution of several failure mechanisms like bond wire lift-off and solder fatigue. Moreover, as the heat flow in a module is almost one dimensional, the presence of a large void in solder, forces the heat to flow around it. This creates a large local temperature gradient such that the heat dissipation performances of the assembly are degraded. Reversely, small voids have a small impact on the overall thermal resistance of the module, as they do not really perturb the heat flow. Power and Temperature Cycling increases the size of already existing voids like on Figure 1.12, where the void of a solder layer between DCB and base plate has doubled its size after 220 000 power cycles [Dup03, Wu95]. There are many countermeasures applied in advanced interconnection processes to obtain void-free solder joints like using of vacuum ovens and control of temperature profiles during soldering and successive annealing. Nevertheless the quality of large-area solder layers is still a critical issue in the reliability of power devices [Cia02].

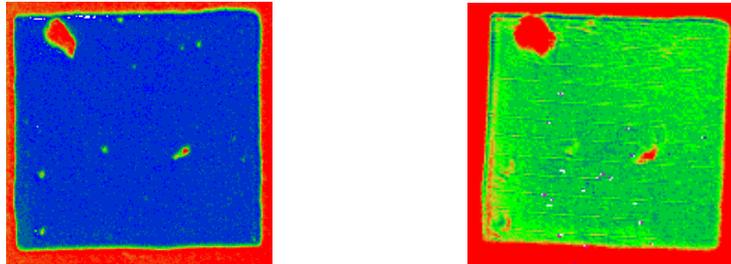


Figure 1.12: On the left, the solder layer between DCB and base plate before tests. On the right, the same solder layer after 220 000 APC cycles with $\Delta T=60K$. [Dup03]

Cyclic temperature shifts during operation produce cyclic shear strains in the die attach due to the CTE mismatch between layers and the spatial temperature gradients. This eventually produce cracking due to fatigue, which lower the critical capability of the solder to transfer heat generated in the die, and therefore increases the thermal resistance of the module [Eva98]. Due to the larger CTE mismatch and to the higher temperature, fatigue cracks are found preferably below the ceramic DCB substrate.

Solder alloys contain usually a combination of several materials like silver, tin or lead which enhance the electrical, thermal and flow characteristic of the final alloy. The bond between the soldered partners is mainly provided by the formation of one or more intermetallic phases. The size, the morphology, and the distribution of intermetallic are very important since they can be a determining factor for reliability of the interconnections.

Microstructural changes leading to macro-cracks in solder layers are markedly different depending on whether lead free or lead rich solders are used. As lead rich solders are tending to disappear due to the RoHS directive, only microstructural changes observed for lead free solders will be detailed here. Microstructural changes are initiated at region of strain concentration and gradually expand with thermal cycling, thus influencing the propagation of cracks. 4 different phases in the development of failure were distinguished [Mat10, Rat10]:

- Gradual formation of low-angle grain boundaries by recovery
- Discontinuous transformation of microstructures by recrystallization
- Intergranular cracking of solder interconnections along the high-angle grain boundaries
- Coalescence of micro-cracks leading to the formation of macro-cracks

The as-solder microstructure of a SAC solder is composed of a few but large grains and two copper rich intermetallics are formed: Cu_6Sn_5 and to a smaller extend Cu_3Sn . After a few thermal cycles, a recovery process takes place leading to the development of a sub-grain structure, through a gradual elimination of extraneous dislocations and the rearrangement of the remaining dislocations into low-angle grain boundaries. A coalescence of intermetallic particles and a gradual disappearance of the cell structure are observed. Then, sub-grains are coarsening until reaching a critical size to form a network of high-angle grain boundaries.

This process is called recrystallization and gives rise to a fine grains structure. In parallel, coarsen intermetallic particles are segregated in the boundaries. The supply in grain boundaries promotes the diffusion creep, so that grain boundary sliding is occurring. The rotation of individual grains causes the formation of voids at the triple points of grain boundaries or of micro-cracks at grain boundaries. This generates intergranular cracking of solder interconnections along the high-angle grain boundaries. At the end, the intergranular cracks coalesce until forming macro-cracks (Figure 1.13). These microstructural mechanisms were described for PTC, but it was proven that the same mechanisms occur in case of APC [Lau07]. Even though, some small differences between those tests were noticed, concerning the recrystallization kinetic and the thickness of intermetallic layers.

Another imperfection often encountered in solder joint, is the irregularity of the solder thickness. The die attach varies substantially between devices and may not be uniform under a single die. This non uniformity influences the device life by increasing strain concentration and influencing crack growth. This influence is highlighted in a simple Coffin–Manson-like power law, modeling the number of cycles to failure of large joints due to thermo-mechanical fatigue. The model can be expressed as follow [Cia02]:

$$N_f = 0,5 \cdot \left(\frac{L \cdot \Delta\alpha \cdot \Delta T}{\gamma x} \right)^{\frac{1}{c}} \quad \text{Eq. 1.1}$$

In Eq. 1.1, L represents the typical lateral size of the solder joint, $\Delta\alpha$ the CTE mismatch between the upper and lower plate, ΔT the temperature swing, c is the fatigue exponent, and x and γ are the thickness and the ductility factor of the solder, respectively.

It can be easily seen that the lifetime is improved by reducing the size of the solder joint, by matching the CTE of the materials, by reducing the edge voids, and by increasing the thickness of the solder (compatibly with the requirements imposed by the thermal resistance).

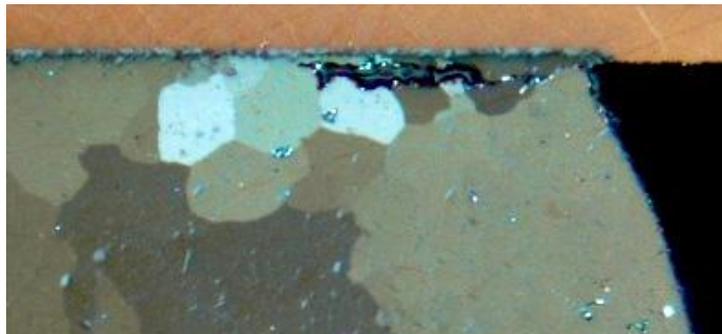


Figure 1.13: Cross-section of a solder interconnection with a crack in the recrystallized zone, taken with polarized light after thermal cycling (Optical micrograph) [Mat10]

1.3.4 Delamination at the interface Mold/Copper

Interfacial delamination is one of the major concerns in reliability issues of electronic packages encapsulated by a mold. The interface between Epoxy Molding Compound (EMC) and copper-based lead frame is often a weak link as a consequence of CTE mismatch [Yad13]. Indeed, under cyclic thermal variations, the CTE-mismatch leads to incompatible thermal strains along materials interfaces, and leads to interfacial cracks initiation, also called delamination. Delamination propagates until a boundary of the interface is reached. Interfacial cracks then kink in the encapsulant material (corner crack), leading to the complete failure of the encapsulation function. It allows then moisture intrusion and may cause component failure [Duri10]. The fracture can be reached by different ways. Either loading conditions are critical, fracture occurs within a short time, or the loading conditions leads to fatigue delamination growth along the interface, failure occurs after a given life time of the component.

A good interfacial adhesion between different materials is the basis of high package reliability. [Khan11, Puf12]. It was shown that, one way to improve the adhesion is to increase the substrate surface roughness [Guz97].

1.3.5 Chip cracking

For brittle materials like silicon, sharp stress concentration at pre-existing damages leads to the rupture under the influence of external mechanical stresses. Micro die cracks can occur during the manufacturing process through crystal growth, wafer scrubbing and slicing and die separation and during wire bonding or soldering [Lie89]. The most critical step is certainly the cutting of the silicon wafer, which could impact dice quality, for example by creating a notch in the chip, like in the Figure 1.14. These pre-existing defects may be not of critical size at moderate service thermal stress. However, during PTC and APC and due to the mismatch in CTE for silicon and substrate, tensile stresses in the central portion of the chip and shear stresses at the edges are developed and cracks grow by stable fatigue propagation and can reach critical size enough to cause brittle failure of the die [Cal12, Cia02]. This type of failure is usually observed immediately after mounting or powering the device.

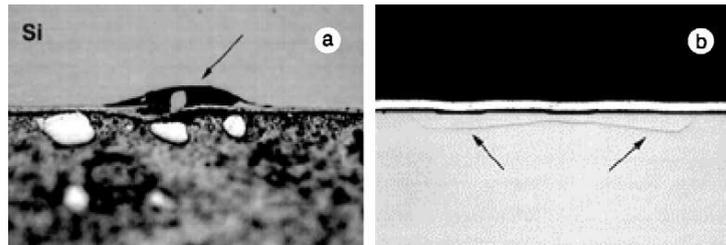


Figure 1.14: On the left, a notch, on the right a crack in a silicon chip (Optical microscopy) [Cia02]

1.4 Technological improvements

Today a point has been reached where the Safe Operation Area (SOA) and lifetime of power modules are limited by the standard packaging technologies, such as wire bonding and soft soldering. As a result, a further optimization of the used technologies will not be sufficient to meet the future reliability requirements. To surpass these limits new packaging technologies have to be developed.

1.4.1 Joining layers

In order to overcome the limits given by the low melting point of standard tin based soft solders, new materials or alloys have to be considered. The two main solutions that are currently developed are Low Temperature Joining Technique (LTJT) also called silver sintering and diffusion soldering.

1.4.1.1 Ag sintering

The Low Temperature Joining Technique was first introduced by Schwarzbauer in 1989 as an alternative for joining large area silicon devices with molybdenum plates. For this technique, a paste which consists of silver flakes embedded in a semi-fluid matrix is applied to the substrate. The chips are then placed into the paste, comparable to a solder paste process. Then the assembly is sintered under a relatively high pressure (e.g. 10 - 40 MPa) and moderate temperatures (e.g. 230°C) [Gut12]. Assisted by the pressure the particles are densified and diffuse together to form a porous interconnection layer. Noble metal surfaces on both partners are required for the formation of an interconnection. Silver diffusion presents numerous advantages. No transition to a fluid phase occurs in the interface layer which prevents a shifting of the chips. Additionally no voids can form in a silver sinter layer, only a homogeneous porosity is formed in the interface (Figure 1.15) [Sche09]. The thermal and electrical conductivity are enhanced in comparison to that of tin-silver solder interface. The mechanical characteristics as CTE and tensile strength are favorable for the implementation in power packages, and most important the high melting point of the silver (961°C) yields high stability and reliability of the joining layer [Amr06]. Today nearly all power electronics manufacturer are working on a solution to transfer silver sintering into IGBT power modules production [Amr05, Göb09]. Indeed, high material costs, non compatibility with today's soldering technologies and extreme process parameters (high pressures and long times) impede the rollout of this technology. The compatibility of a new joining technology with today's soft soldering methods for semiconductors will be a major advantage for the technology rollout into existing power module families [Gut10].

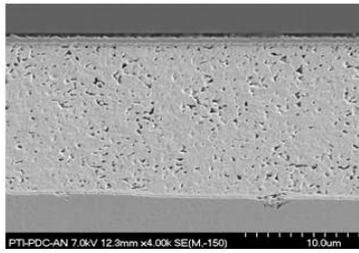


Figure 1.15: Cross-section of a silver sinter joint with optimized process parameters [Gut12]

1.4.1.2 Diffusion soldering

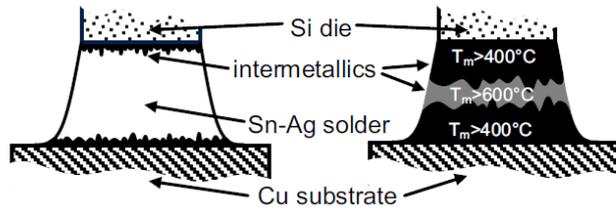


Figure 1.16: Schematic comparison of a standard solder joint on the left and a diffusion bonded joint on the right. The diffusion soldered joint consists of 2 different intermetallic phases. [Gut12]

In standard soldering processes the die attach system consists out of thin intermetallic interfacial layers and the unreacted solder material in between. Under PTC, standard soft solders are typically developing fatigue crack growth within the unreacted solder whereas the interfacial joint between the Sn-based intermetallics and the soldering partner (chip or copper substrate) does not show any ageing. Based on this finding, a diffusion soldering process creating a bond which is solely formed from intermetallics has been developed (Figure 1.16). This soldering technology is based on the inter-diffusion of a low melting point metal (Sn) in the other element (Cu), having a higher melting point. For the Cu-Sn system the joint can e.g. be realized by the formation of Cu_3Sn and Cu_6Sn_5 intermetallic phases (Figure 1.17) which have much higher melting points and higher mechanical strengths than the Sn-based soft solder base materials [Fer00]. Because of the total transformation into intermetallic phase, the bond formed is able to sustain temperatures which are several hundred degrees Celsius higher than the process temperature. Thus, in the system CuSn the process temperature is about 250°C at a pressure of some 2 MPa, while the melting temperature of the formed Cu_3Sn or Cu_6Sn_5 intermetallics was above 415°C and 460°C , respectively [Gon99]. At the same time there is only a moderate impact on the elastic moduli and the fracture toughness. As a result, an improved durability against thermo-mechanical loading can be expected for this interconnects. To create pure intermetallic joints with a remelting temperature $T_m > 400^\circ\text{C}$ a rapid solidification process using common Sn-Ag solder is utilized as a diffusion bonding process [Gut12]. The general formation of the intermetallic die attach system can be controlled by the solder thickness ($d \leq 10\mu\text{m}$), the pressure ($p \leq 6\text{MPa}$) as well as time and temperature. In the past, one major blocking point was the low phase formation rate for the development of a productive diffusion bonding process for IGBT modules. But now optimized process parameters lead to a controlled solidification of the joint within seconds [Gut10]. The complete conversion of the solder into high melting intermetallics can be ensured by the parallelization of process steps. Today the high degree of automation and the low process times are two major advantages of diffusion bonding compared to sintering.

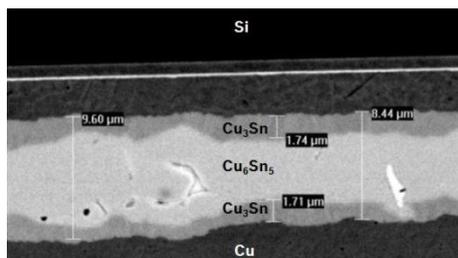


Figure 1.17: Cross-section image of diffusion bonded joint with optimized parameters[Gut12]

1.4.2 Interconnects

1.4.2.1 Cu wires

Nowadays, Al bond wire interconnect is not limited by the bond interface anymore but by the wire material itself. As previously seen, the CTE mismatch between the Si of the die and the Al bond wire induces thermo-mechanical stress resulting in the wire lift-off. The wire-to-die contact degradation does not happen at the die surface, but within the wire itself. Indeed, the initial bond crack is always formed near the semiconductor interface and propagates within the Al matrix along the Al-Al grain boundaries. In order to limit the degradation of the bond interface, Cu seems to be a good candidate as replacement material for an Al wedge bond. In addition to its superior mechanical properties, Cu also offers better electrical and thermal characteristics compared to Al. A comparison of thermo-mechanical properties of Al and Cu is shown in Table 1.1. A lower electrical resistivity and an increased thermal conductivity can directly be converted into higher current densities for IGBT modules [Gut10].

	Cu	Al
Electrical resistivity ($\mu\Omega\text{cm}$)	1,7	2,7
Thermal conductivity (W/mK)	400	220
CTE (ppm/K)	16,5	25
Yield Strength (MPa)	140	29
Elastic modulus (GPa)	110-140	50
Melting point ($^{\circ}\text{C}$)	1083	660

Table 1.1: Comparison of the material properties of copper and aluminum

Up to now, the main obstacle for ultrasonic Cu bonding of heavy wires was the mismatch in the mechanical properties of Cu and the semiconductor's topside metallization. For the standard Al topside metallization the Cu wire simply sinks into the soft Al matrix, leading to chip damage and weak bond interfaces. Consequently the implementation of pure Cu heavy wire bonds requires a new metallization stack with Cu, which is associated with severe problems. Cu contact on silicon devices are subjected to diffusion and corrosion. Diffusion of Cu into the semiconductor device can interfere with the electrical function of the device. Corrosion can also compromise the device functionality if conductive corrosion products interact with the high electrical fields at the passivation edges of high blocking devices. Both problems have to be solved by a suitable design of the contact metallization, like in Figure 1.18 [Sche12]. It was also related in [Nel11] that a copper-based power metallization on a robust power MOSFET is a very reliable concept as it can handle millions of electrical power pulses with a peak temperature in the silicon of 350°C without failure.

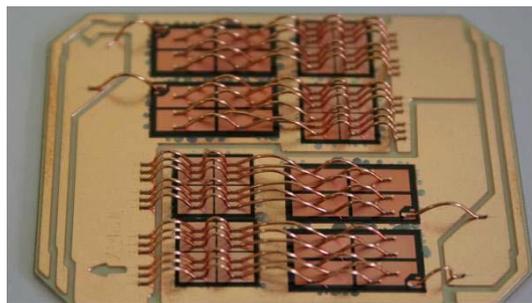


Figure 1.18: Ceramic substrate with $400\ \mu\text{m}$ Cu wire bonds on Cu metallized IGBTs [Gut10]

1.4.2.2 Al-clad Cu wire

An alternative to pure Cu wire bonds is Al-clad Cu wire bonds. The Al/Cu composite material combines the benefits of both constituent materials. The excellent mechanical, electrical, and thermal properties of Cu and the softness and good bonding characteristics of pure Al should result in a very reliable bonding joint without losing the versatility of the standard pure Al bonding process. An example of an Al-clad Cu wire is shown Figure 1.19, it consists of 60-70% Cu by volume, which is equivalent to an Al layer thickness of $25\text{-}35\ \mu\text{m}$ around a $230\text{-}250\ \mu\text{m}$ Cu core for a $300\ \mu\text{m}$ wire. Despite the much harder wire material, bonding on standard

semiconductor power chips with Al topside metallization can be applied with minor changes to the bond parameters and do not even require a special bond tool [Sche12].

The superior electrical performance becomes manifest in up to 45% higher ampacity and surge current capability. Together with the outstanding power cycling capability the Al-clad Cu wire becomes a real alternative to pure Cu wire bonds in the near future. Therefore, Al-clad Cu wire bonds are well suited to increase the wire bond lifetime without the drawback of a new chip top side metallization. Further material and process optimization has to be conducted to establish a safe and effective bonding process suitable for series production [Schm12].

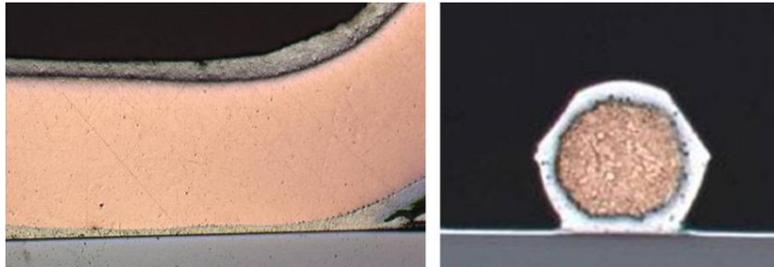


Figure 1.19: 2 cross-sections of an Al-clad Cu wire bond foot on a freewheeling diode [Schm12]

1.4.2.3 Ribbon

Large Al ribbon bonding may become a technique to address current and future interconnect requirements, as it eliminates some of the wire bonding limitations, like the need for bonding a significant number of parallel wires per device to fulfill the necessary resistance or current requirements (Figure 1.20) [Ong04]. Large Al ribbon is advantageous as it offers an improved electrical performance through lower on-state resistance (R_{DSon}), and higher current-carrying capability due to the scalable cross-section. Another benefit of the ribbon geometry is the ‘decoupling of thickness and width’ of the interconnect configuration, by choosing an aspect ratio which enables to fit a large interconnect cross-section with a minimum number of ribbons into the given space of a package. It therefore not only creates more design flexibility, but also enables thinner packages and a significant reduction in assembly cost. In addition, the ribbon’s lower stiffness better allows creating short loops with low but controlled loop height between bonds along the ribbon to cover the metallization area with multiple bonds efficiently.

But the change in cross-section from round to rectangular also reduces the possibility to twist wires under large forced angles. This flexibility is very important to interconnect configurations with a complex structure, like TO-packages, but it is not required to interconnect Power Quad Flat No-Lead (PQFN) packages, as those typically have a much more structured layout [Lue07]. Moreover, for a given loop geometry the heel damage in a ribbon is considerably lower than for an equivalent heavy wire, because of the larger cross-section at the heel of the ribbon bond. This allows ribbon to make connections across unusually high steps with short bonds and reduces stress from thermal cycling [Wei02]. A ribbon is also more immune against external vibrations, as its vibration resonances are very different in the vertical and lateral directions [Far07].

The process set-up for wire and ribbon bonding is exactly the same, only the bond force required to bond ribbon is much lower than that for round wire because the geometry of the ribbon contact area more closely matches that of the device surface [Wei02]. With Al ribbon bonding there is less risk of cratering than with Al wire bonding because the bond force and the ultrasonic energy are distributed over a larger area, thus lessening the stress on active substrate surfaces [Ong04].

To sum up, the major improvement of ribbon bonding, is due to the lower number of ribbons required to achieve the same interconnect resistance. This means the same electrical performance at lower cost, with a reliability which surpasses the one of packages with wire bonds. For all this reasons, the new ribbon bonding technology is an attractive alternative solution to standard large Al wire bonding [Ong04]. But ribbon bonding still a fairly new method and thus there exists ample improvement potential. But a systems approach should be taken, where die and lead frame design take into consideration the specifics of the ribbon bonding process and the respective equipment. PQFN as a standard package design and ribbon bonding as a standard interconnect technology are a good fit and together offer a standard that can fulfill present and future requirements regarding performance, reliability, package size and cost for all end-user market segments for discrete power semiconductors [Lue07].

A forward-looking concept for ribbons is based on Al-clad Cu ribbons. This could be a major advancement of the process. Al-clad Cu ribbons have shown the potential of a ten-fold lifecycle improvement in certain applications. Compared to large Al wire bonding, it's a jump by a factor of hundreds [Hau08]. Cu ribbons are also developed.

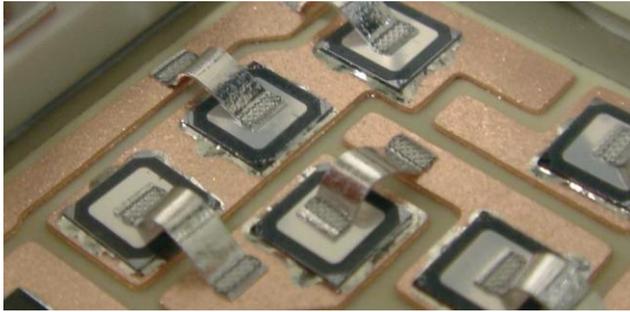


Figure 1.20: DCB substrate with Al ribbons on IGBTs [Far07]

1.4.2.4 Cu clip

Cu clip interconnects are a bond-less packaging technology whereby a small metal slab attached to the die surface replaces bonding wires (Figure 1.21). The process connects the active area of a die to the package lead frame using a specially designed copper conductor rather than making the connection with multiple ultrasonically bonded wires [Huang12].

The technology is typically used for MOSFET devices in various package types, for more than a decade. The advantage of bond-less technology is that it provides significantly improved electrical performance when compared with multiple wires or even with ribbons. The on-state resistance is reduced because the large cross-section of Cu clip makes use of the total top die metallization [Ken09]. The clip interconnect also reduces thermal resistance and package inductance and improves the current distribution into the device. The clip-bonded products have a higher current rating capability and efficiency by combining the reduction of thermal/electrical resistance and package source inductance.

The clip is reflow-soldered to the die pads and the substrate pads. However, soldering clips on a die that is itself soldered to the die pad is a challenging process. This requires a good control of the positioning of the die and clips during the molten phase of the solder reflow process. And it becomes more difficult with decreasing package size [Liu00]. The solder joint connecting the Cu clip to the device allows a much uniform current distribution and offers opportunities to reduce thermal stress by optimizing its geometry, using compliant substrate. But under APC, this solder joint exhibits plastic deformation and creep strain due to local heating and thus severe high temperature creep of solder.

The thick and large solder joint improves the heat dissipation with the added thermal path through the joint itself, whereas wire bond modules are limited to one directional heat dissipation. This design also allows mechanical and thermo-mechanical forces to be distributed over a larger area, thus reducing equivalent mechanical stresses at the device connections. [Liu00]

The clip-bonded package has an option of adding a heat sink on top of the clip or using a thick clip for two-sided cooling. The implementation of double sided cooling improves the thermal performance of the module, which the wire bond technique cannot achieve.

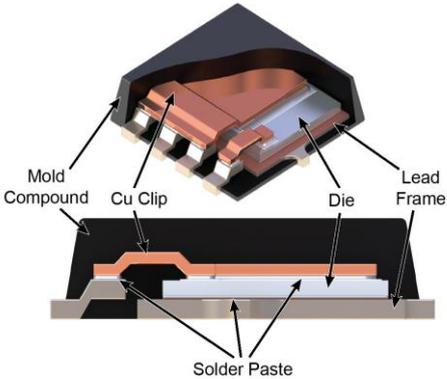


Figure 1.21: Cross-section of a Cu clip package SO8-FL from Amkor [Amk14]

1.4.3 Dual side cooling

Cooling methods have reached their limits. Thus, to further improve thermal performance, the area of thermal paths must be increased, for example by double sided cooling. With this packaging technique, the components are sandwiched between two DCB substrates. Thus, they can be cooled on bottom and top sides. The top DCB substrate serves as a heat conduction path so that the excessive heat generated by the chip can be directed to the top DCB then flow back to lower temperature diode devices. External fin heat sinks with air flow or microchannel heat sinks can be directly brazed onto both sides of the module, thus significantly improving the thermal performance and therefore the reliability of the module [Cha12, Gil99].

1.4.4 Combination of improved technologies

Applying simply one improvement step will not necessarily lead to a better reliability, due to the interdependence of all components. That is why manufacturers are developing technologies which are combining different improvement steps.

For example, the Danfoss Bond Buffer (DBB) technology combines the advantages of the sintering and the Cu bonding process, addressing the main weaknesses of the conventional power modules (soldering and Al-wire bonding). The key part of this technology is a thin Cu foil sintered onto the upper surface of the semiconductor, which absorbs the high mechanical load during Cu wire bonding and prevents the die from damage. At the same time, the sintering technology is also used to replace the soldering of the connection between the die and the DCB substrate. This technology can be applied as an upgrade for the state-of-the-art power module technology without dramatically affecting the set-up of the existing production lines and the design of the power modules [Rud14].

Infineon has developed a similar technology, called .XT. It consists of Cu bond wires, diffusion soldering and improved system soldering for the die to DCB interconnection [Ben11]. The result is a highly robust power module with optimized thermo-mechanical parameters.

A new packaging technology, called SKiN technology (Figure 1.22), which eliminates the need for solder layers and wire bonds, was developed by Semikron. The SKiN device contains power chips which are sintered on both sides. The chip top side is sintered to a special flexible circuit board, which is the key design element of the package. This flexible circuit board is made of polyimide with patterned metal tracks on both sides. The bottom metal, called “power side”, exhibits a thick metal layer which will be able to carry the load current. The bottom chip side is sintered to an insulating substrate, such as a conventional DCB substrate. The entire structure is sintered to an Al pin fin heat sink, thus eliminating the thermal grease and improving the power dissipation. The device exhibits a very low volume and weight, excellent thermal resistance and very good power cycling capability. The careful material selection makes the device usable for ambient temperatures beyond 150 °C. The flex board which replaces the wire bonds has the capability to integrate passive and active components for gate drive, current and temperature sensing, and filtering purposes on the logic side, thus proceeding towards true 3D integration [Sto11].

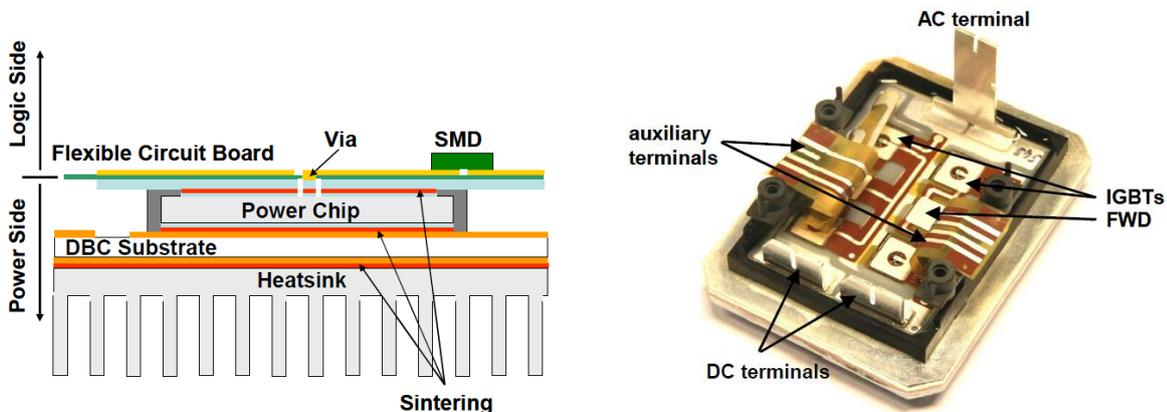


Figure 1.22: On the left a schematic cross-section of SKiN devices. On the right a dual SKiN device [Sto11]

1.4.5 SiC

Presently, almost all of the power electronic converter systems in automotive applications are using Si based power semiconductors. But the performance of these systems is approaching the theoretical limits of the Si fundamental material properties. The emergence of silicon carbide SiC based power semiconductor likely will result in substantial improvements in the performance of power electronic converter systems in transportation applications. Indeed, SiC exhibits many advantages compared with Si based devices. First of all, SiC is a wide-bandgap semiconductor which makes it support higher electric field than Si and is therefore able to operate at high temperatures. It has also a higher breakdown voltage. SiC devices are thinner, and they have lower on-resistance. With this lower R_{DSon} SiC unipolar power devices have lower conduction losses and therefore higher overall efficiency. SiC has also a higher thermal conductivity and thus a lower junction-to-case thermal resistance, R_{th-jc} . This means heat is more easily conducted away from the device junction, and thus the device temperature increase is slower. The reliability of SiC devices is also improved compared to Si devices. In spite of all these advantages, research pertaining to SiC power devices and their practical applications has been hampered by the lack of reproducible techniques to grow semiconductor-quality single crystals and epilayers. SiC technology remains new, for example the first commercial MOSFET was produced in 2011; therefore improvements still have to be made. Moreover, as SiC semiconductors handle high temperatures, new die attach technology as sintering are required to efficiently get the heat out of the devices and ensure a reliable connection. Therefore, once processing and fabrication issues with SiC are solved, a significant reduction in power electronic converters conduction and switching losses can be achieved by replacing Si devices with those made from SiC. This change means a much-reduced thermal management system is possible in the vehicle, with system benefits such as a reduction in the weight, volume, and cost of converter heat sink requirements [Bha93, Tol02].

1.5 State of the art in Active Power Cycling (APC) reliability

1.5.1 Active Power Cycling (APC)

Manufacturers seek to estimate lifetime of semiconductors and the conditions under which they fail. Such lifetime estimation and reliability testing is usually done through Active Power Cycling (APC) tests as it reproduces working conditions. The modules are mounted on a heat sink and a voltage is applied in forward direction to reach a defined current. This current through the Device Under Test (DUT) leads to power loss in the entire module and results in an increase of the semiconductor temperature. By switching periodically the current on and off, the temperature of the chip rises and falls due to alternating heating and cooling, inducing a junction temperature swing ΔT_j . One power cycle is defined as the period of heating up the junction from minimum temperature T_{jmin} to maximum T_{jmax} and cooling it down. In most set ups, the temperature and electrical data are monitored during each cycle. If these values increased more than a previously determined amount (e.g. 20%), the End of Life criteria is fulfilled, and the corresponding number of cycles to failure N_f is then used in models for lifetime estimation [Hut14].

Active Power Cycling (APC) can be distinguished from Passive Temperature Cycling (PTC) test as the heating source differs: in APC the chip is the internal heating source (active) whereas in PTC the heating source comes from its environment (passive). Thus, the temperature distribution in the DUT is also different: the temperature is spatially not homogeneously distributed in APC whereas for PTC the temperature of the module is uniform. Moreover, the commonly used cycle times are about ten to hundred times shorter at APC (from 0,2 seconds to 1 minute) than at PTC (from 15 minutes to 1 hour).

1.5.2 The LESIT and RAPSDRA project on APC reliability

The results of the Swiss LESIT project (1993-1995) [Hel97] are often used as a reference for the power cycling capability of standard power modules. In this project, IGBT modules with a base plate, coming from different manufacturers have been power cycled in 14 tests with different thermal conditions. The minimal junction temperature T_{jmin} ranges from 25°C to 85°C while the maximal junction temperature T_{jmax} ranges from 80°C to 130°C. The heating phase during these tests was adjusted to be shorter than 10 seconds to stress bond wires mainly, considering bond wire lift-off as the main failure mechanism in power devices. The results of the LESIT project are pictured in Figure 1.23, and in Eq. 1.2.

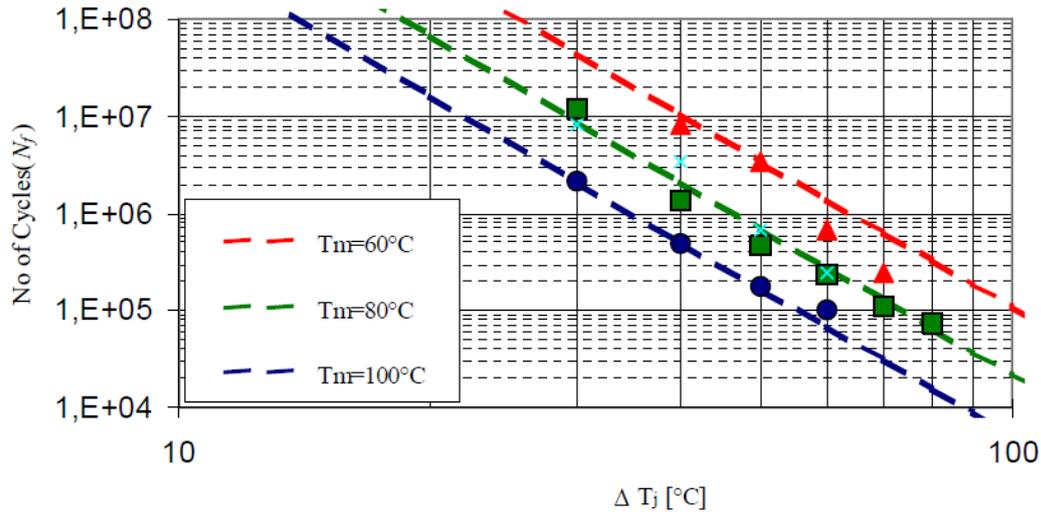


Figure 1.23: Number of cycles to failure versus ΔT_j and T_m from the LESIT project [Hel97]

$$N_f = A \cdot \Delta T_j^\alpha \cdot e^{\left(\frac{Q}{R \cdot T_m}\right)} \quad \text{Eq. 1.2}$$

With R being the gas constant (8,314 J/mol.K) and T_m in Kelvin make $A = 640$, $\alpha = -5$, and $Q = 7,8 \times 10^4 \text{ J} \cdot \text{mol}^{-1}$ (or about 0,8 eV).

LESIT curves show that for $\Delta T_j \geq 60\text{K}$ an increase of the temperature swing of 20K means a decrease of the power cycling reliability of factor 3 to 4 at constant T_m . Further important result of LESIT project is the prediction that beside ΔT_j , also the medium junction temperature T_m has considerable influence on the power cycling reliability. According to the really achieved results, if T_m increases of 20°C, also in the range of $\Delta T_j \geq 60\text{K}$, a decrease of the power cycling reliability of factor 2 can be expected (constant ΔT_j) [Amr06].

Another important research program devoted to power cycling reliability testing was the RAPSDRA (Reliability of Advanced Power Semiconductor Devices for Railway traction Applications, (1995-1998)) [Ber98] project. This project proposed 2 APC tests conditions. The first APC test focuses on the bond wire reliability and is based on the work of the LESIT project. It recommends to test devices with $T_{j\text{min}} = 55^\circ\text{C}$, $\Delta T = 50^\circ\text{C}$ to 70°C and with a short t_{on} so that the period of cycle does not exceed 3 seconds. The second APC condition aims at determining the solder reliability and recommends to test devices with the same temperature condition as for the first test but with a significantly longer period of cycle of 1 minute. This shows the influence of t_{on} on the failure mechanisms development and how this dependency can be used to study preferably one or another phenomenon.

1.5.3 A variety of test methods

Since the completion of LESIT project in 1997, standard modules have been improved and new technologies have been implemented. For examples, wire bonds techniques have been optimized, new solder materials have been used like lead free solders, base plates are not only made of Cu but can be made of AlSiC... Moreover new technologies are also under development like Ag-sintering or the replacement of Al wire bonds by stripes. All this contribute to push forward the established reliability limit of standard modules, known from the LESIT project. Nevertheless, it is not evident to compare all the power cycling reliability results obtained along the years, as it exist a variety of manners to perform APC tests.

1.5.3.1 The different type of APC tests

First of all, 3 different types of APC tests are in use: DC current, Pulse Width Modulation PWM, or superimposed tests. The DC current injection induces thermal stress by creating a thermal flux in the module. This kind of test is relatively simple but the excitation of devices is not realistic (no switching and no high voltage). PWM tests generate APC with realistic electrical stress in power devices. The DUT act as a single phase PWM inverter, its switching frequency is adjustable and provides a regulated sinusoidal current to an

inductive load. Here the operating conditions are similar to those existing in a drive inverter [Sme11]. In a superimposed test, devices are submitted to a combination of PTC and APC. During the dwell time of a PTC test, power injections are applied. This test also aimed at a better representation of real applications in which power modules undergo both PTC and APC at the same time. Obviously the number of cycles to failure obtained for the same device under those 3 different tests will be different as the loading conditions differ. But, even by assuming that all tests are performed under DC current, some differences can still be observed in the test set-ups.

1.5.3.2 Cooling conditions

The cooling function of the heat sink can be ensured with an air-cooled or a fluid-cooled system. Fluid-cooling presents the difficulty that one has to deal with pumps, pipes and to regulate the coolant flow. On the other hand with air-cooling the maximum cycle frequency is limited [Stu10].

1.5.3.3 Parameter monitoring and failure criteria

Besides the cooling system, the parameter monitoring is also an important issue in APC. Two main parameters are generally considered as good ageing indicators in power device ageing tests and are monitored: the thermal resistance between the junction and the base plate (R_{th}), the on-state voltage (Collector-Emitter voltage V_{ce} in case of an IGBT, Drain-Source voltage V_{DS} for a MOSFET and forward voltage V_F for a diode). Sometimes, the leakage current is also monitored as aging indicator. The on-state voltage measurement makes it possible to detect wire bonds damage by instantaneous stepwise increase. The relative variations due to this damage are very low because the low voltage across the connections constitutes a weak part of the total on-state voltage. Therefore this measurement must be made with a very high degree of accuracy. R_{th} is an indicator for characterizing the assembly integrity between the chip and the base plate. R_{th} increases if a fracture appears and significantly modifies the heat transfer. Its evaluation is the most delicate and requires measuring junction and base plate temperatures under a fixed thermal flux. By calculating the power dissipation P_d the thermal resistance R_{th} can be estimated (e.g. of an IGBT):

$$R_{th} = \frac{T_{j\ max} - T_c}{P_d} = \frac{T_{j\ max} - T_c}{V_{ce\ sat} \cdot (I_{load} + I_{meas})} \quad Eq. 1.3$$

With T_c the heat sink temperature (also called case temperature), $V_{ce\ sat}$ the collector-emitter saturation voltage, I_{load} the loading current and I_{meas} the measuring current.

The case temperature is usually measured via a thermal sensor i.e thermocouple glued to the base plate of the DUT. On the contrary there are several methods of measuring the junction temperature T_j . If a closed molded package is under test, the only way to measure T_j is via the measurement of Thermo-Sensitive Parameters (TSP), such as the on-state voltage. In the case of an open module with accessible die, T_j can be determined via the measurement of the chip surface temperature, for which there are 3 main methods: infra-red cameras, thermocouples and optical fibers with crystal senses on their ends. Infra-red method is a fast, accurate and non-contact temperature measurement. This method provides thermal imaging of the whole modules, which can be useful to have a first evaluation of the temperature distribution. Thermocouples method is a contact chip temperature measurement with a response time of about 10 ms but this response time and the measurement accuracy can be altered due to a bad thermal contact with the measurement area. Two sorts of contact optical fibers are used: fibers with GaAs sensors and whose response time is about 100 ms, and fibers with phosphor sensors with a response time at 63% of 25 ms (not depending on the environment of the sensor) and a measurement delivered every 250 ms. This last tool can provide reliable dynamic temperature measurements through the silicone gel recovering the chips. [Ham97]

So, depending on the method used to measure the junction temperature, the result obtained can be more or less precise, thus influencing the accuracy of the R_{th} ageing indicator. And ageing indicators are used to determine the number of cycles to failure via failure criteria. Indeed, when the on-state voltage or the R_{th} are increasing to a certain amount previously defined, the test is stopped and the DUT is considered to be failed (Figure 1.24). Moreover, some variations are to be observed in the definition of the failure criteria. For the on-state voltage based failure criteria, the amount of increase ranges from 5% to 20%. For the R_{th} based failure criteria, the amount of increase varies from 10% to 20%.

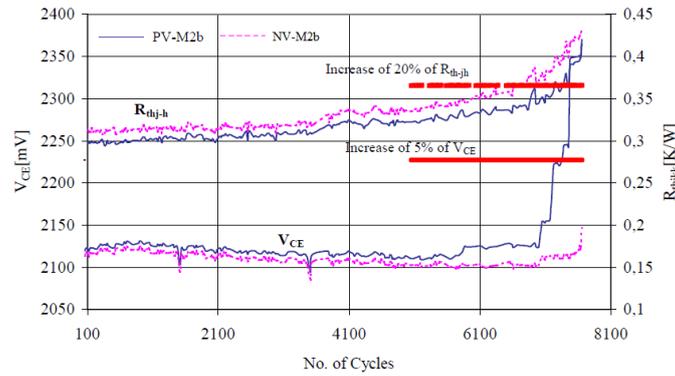


Figure 1.24: Evolution of V_{ce} and R_{th} during APC test of ECONOPACK power modules at $\Delta T_j=113K$ [Amr06]

More recently, other failure indicators were monitored, like the drain to source on state resistance R_{DSon} [Sow13] or the thermal impedance Z_{th} [Hen11]. To determine the R_{DSon} , APC has to be stopped, a small current is injected in the DUT and the exact drain current I_d that is injected through the device and the drain to source voltage V_{DS} are measured. R_{DSon} tends to increase in electrical tests when the component thermal performances are decreasing and a steep increase is observed when the percentage of failure is important. Monitoring the thermal impedance spectrum also require the test interruption. The Z_{th} is usually measured in the cooling phase, after that a load pulse is applied through a load current in the DUT. So, there is a wide range of variations concerning failure criteria.

1.5.3.4 Control strategy

The definition of the control strategy of an APC test, i.e the strategy of reacting to degradation effects in the DUT is also of prime importance. It was just seen that degradations effects can affect the device parameters and thus cause a change of the test condition during the test duration. Solder fatigue increases the thermal resistance of the DUT which increases the temperature swing under constant test conditions (load current, on-time, cooling conditions). As well as wire bonds degradations enhance the on-state losses in the device and increase the temperature swing. The positive temperature coefficient of modern devices will consequently lead to increased losses, which again will increase the device temperature. This positive feedback loop can significantly accelerate the failure process. Therefore, the control strategy is a very important feature of the APC test. There are 4 different control strategies which were described and compared in [Sche10]:

- 1) $t_{on} = \text{constant}$ and $t_{off} = \text{constant}$

This strategy of constant timing switches the load current on and off in fixed time intervals. ΔT_j is defined at test start via e.g the definition of a constant current and T_{jmax} , T_{jmin} and ΔT_j may increase during test duration due to aging effects with no compensation by a control strategy. This is the method closest to application and the most severe one.

- 2) $\Delta T_c = \text{constant}$

This strategy controls the heat sink temperature. On-time and off-time are not fixed, but are determined by the time needed to heat and cool the device to the specified temperatures. Here a change in the cooling liquid temperature would be compensated by adjusting the heating and cooling times. This maintains a constant temperature swing. Since a possible degradation of the thermal interface between module and heat sink would be compensated, this strategy is less severe than the strategy 1. Taking the strategy 1 has a reference, an increase of about 50% in the number of cycles to failure is observed by testing with strategy 2 in [Sche10].

- 3) $P_v = \text{constant}$

This control method is based on constant t_{on} and t_{off} times but with the additional requirement, that the power losses P_v are kept constant. This requirement is achieved by controlling the gate voltage or current to compensate an increase in the voltage drop V_{ce} . This strategy is much less severe for a module, as it reduces the acceleration effect of different failure modes, and results in a significant increased number of cycles to failure. In this case, the number of cycles to failure increases to 120% compared with strategy 1 [Sche10].

4) $\Delta T_j = \text{constant}$

This latest strategy supervises $T_{j\min}$ and $T_{j\max}$ and reduces t_{on} or the current load I_{load} to keep this parameter constant. This compensates all degradation effects and leads to the highest lifetime. Indeed, the number of cycles to failures increases to 220% in comparison with the reference [Sche10].

It is therefore essential to know the control strategy, if APC tests are to be compared.

The complexity in interpreting and comparing different APC studies comes also from the interdependence of all failure mechanisms and the influence of diverse test parameters. Recently, a pure statistical analysis [Bay08] of a significant number of APC tests suggested the impact of several parameters, in addition to ΔT_j and T_m known from the LESIT project. In this analysis, the power on-time t_{on} , the wire bond thickness d_{bond} , the current density and the chip's voltage class are shown as parameters influencing the lifetime.

1.5.4 Review of papers on APC tests

In order to have a clear overview about all the APC tests that were performed until now, 70 publications from 1993 to 2014 were reviewed [RefExp]. For all this papers, the quantity of modules tested, the type of modules, the test conditions as well as the analysis methods, the goal of studies and the lifetime estimations are reported and analyzed.

1.5.4.1 Quantity of samples tested

First of all, the number of samples tested per publication was reported and its distribution is plotted in Figure 1.25. For some papers the number of samples per test run was missing, so the quantity was assumed to be one. The statistical power is important to know in order to recognize significant effects between different APC tests. As there are minor deviations in the production parameters, the result for every sample can differ, therefore a minimum of 10-15 samples per test is generally required to obtain reliable results.

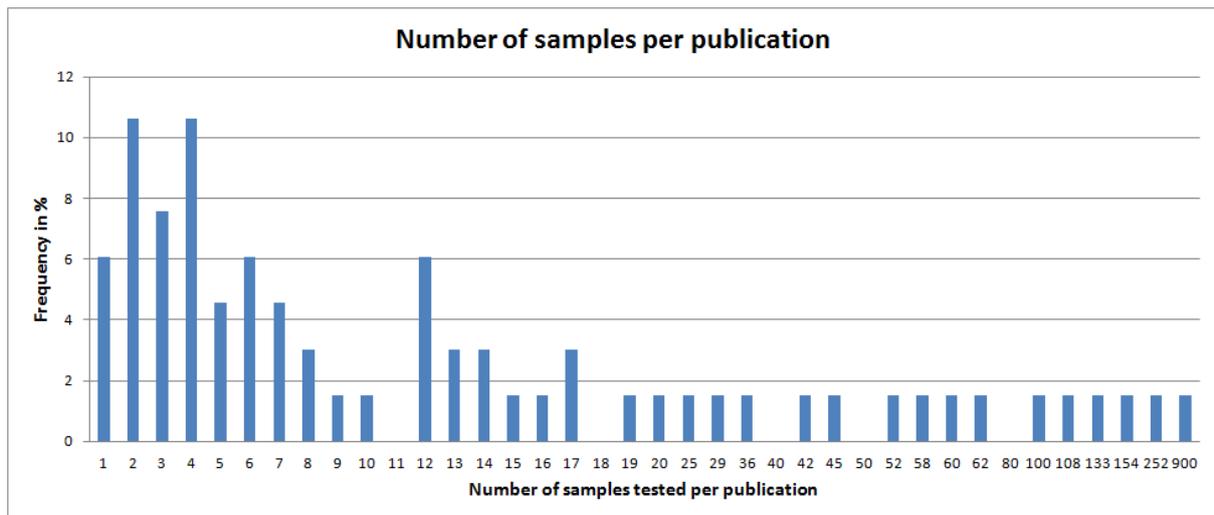


Figure 1.25: Distribution of the number of tested samples per publication

As can be seen from the Figure 1.25 most of papers are generally testing up to 10 samples or less. In a few cases, more than 100 devices were tested in total. But in 86% of cases there is only one sample per test run.

1.5.4.2 Type of device tested

The type of semiconductors that were submitted to APC was analyzed Figure 1.26. It reveals that with a frequency of 65% the big majority of tests are performed with IGBT. Then, come diode and MOSFET, both with about 10% of testing frequency. DMOS (Double-Diffused MOS), TRIAC (Triode for Alternating Current), HDTMOS (Third Generation of High Density TMOS), JFET (Junction Gate Field-Effect Transistor), and transistor were also tested but in small proportion. Here, the supremacy of IGBT on all other types of semiconductor appears clearly.

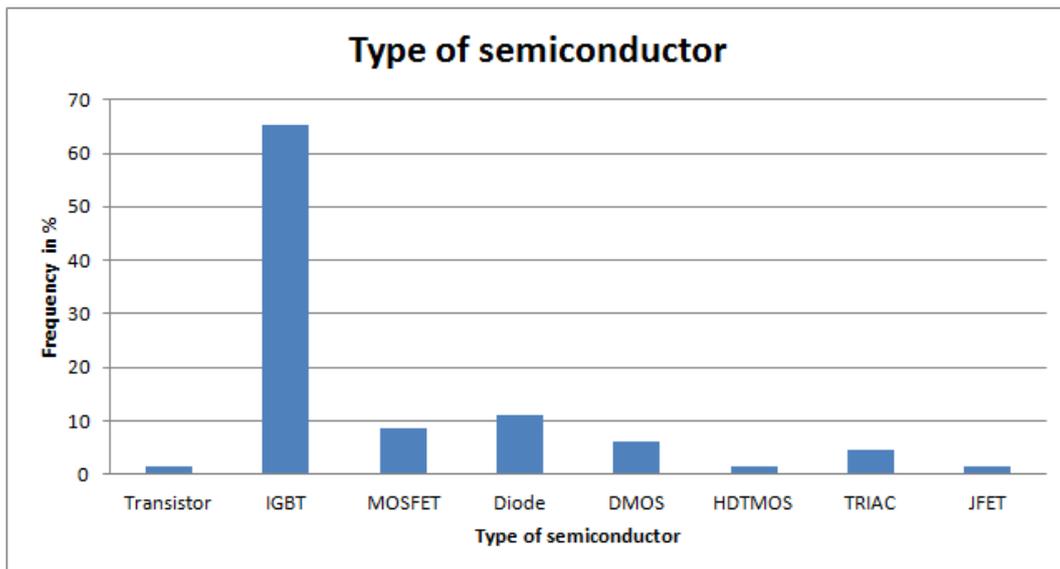


Figure 1.26: Histogram showing the type of semiconductors tested per publication

Details regarding the internal structure of modules under test were also investigated. The most widespread interconnect is Al wire, representing 85% of interconnects. 5% of the tested modules had either Cu wires or a Cu clip as interconnect and fewer had Ag stripes or Al-clad Cu wires (Figure 1.27).

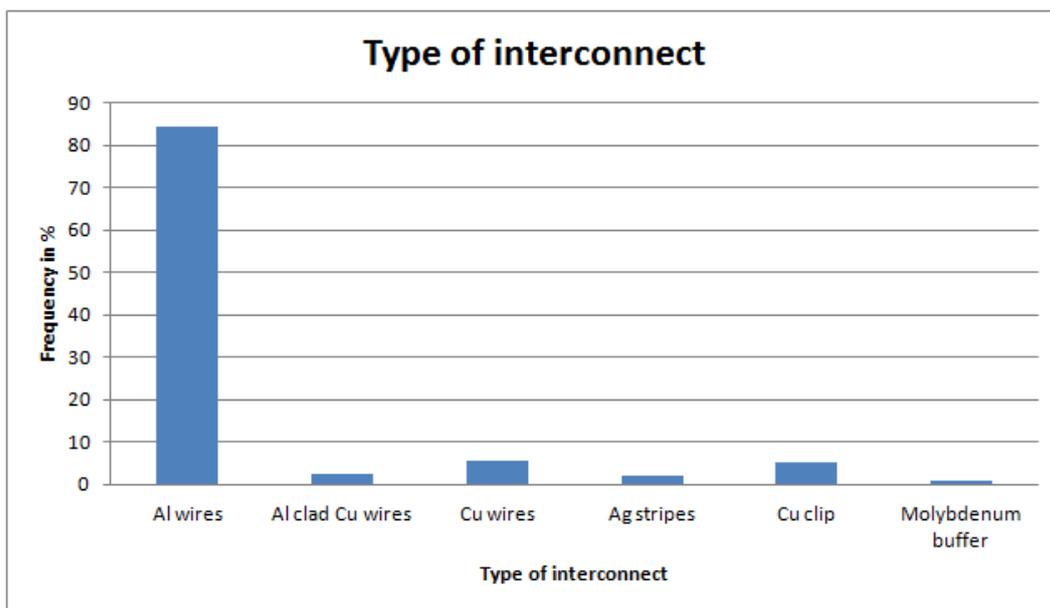


Figure 1.27: Histogram showing the type of interconnects in the tested modules

Concerning the metallization layer on top of the chip, 94% of the modules had a metallization made of an Al alloy (e.g. AlSiCu or AlCu...). Only 6% of them had a Cu metallization.

The die itself, was made of silicon, except for 4% of the modules which had a chip of silicon carbide SiC.

The die was attached to its substrate mostly via soldering. Only 12% of the dies were attached with Ag sintering. The solder alloy used for the die attach was quite often not mentioned. By analyzing the available data on solder alloys, one can see on Figure 1.28 that a short majority of modules are using lead-free solder rather than lead-rich solder. Diffusion soldering remains an exception.

The substrate is at 90% a DCB, at 6% a Cu Lead frame and at 4% a Printed Circuit Board (PCB). In almost half of the cases, the exact type of DCB was not mentioned, but concerning the available data, Figure 1.29 shows that DCB with Al₂O₃ is preferred to DCB with AlN.

60% of the modules are designed with a base plate. Among those modules, the majority had a Cu base plate, whereas the others had a new AlSiC or an Al base plate (Figure 1.30).

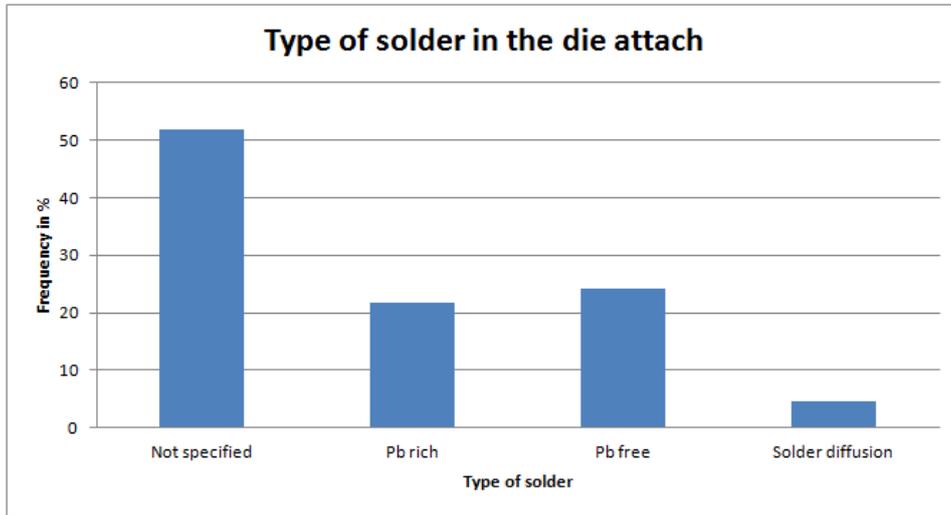


Figure 1.28: Histogram showing the type of solder for the die attach in the tested modules

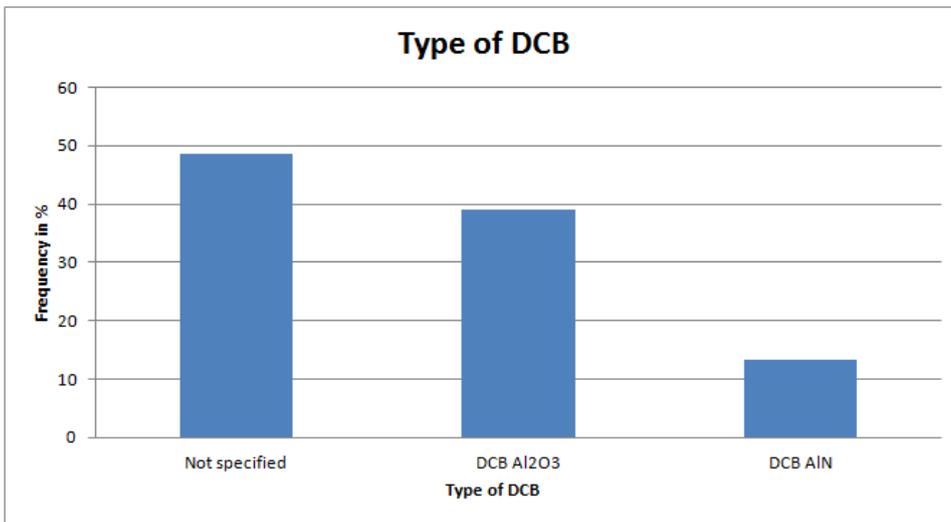


Figure 1.29: Histogram showing the type of DCB in the tested modules

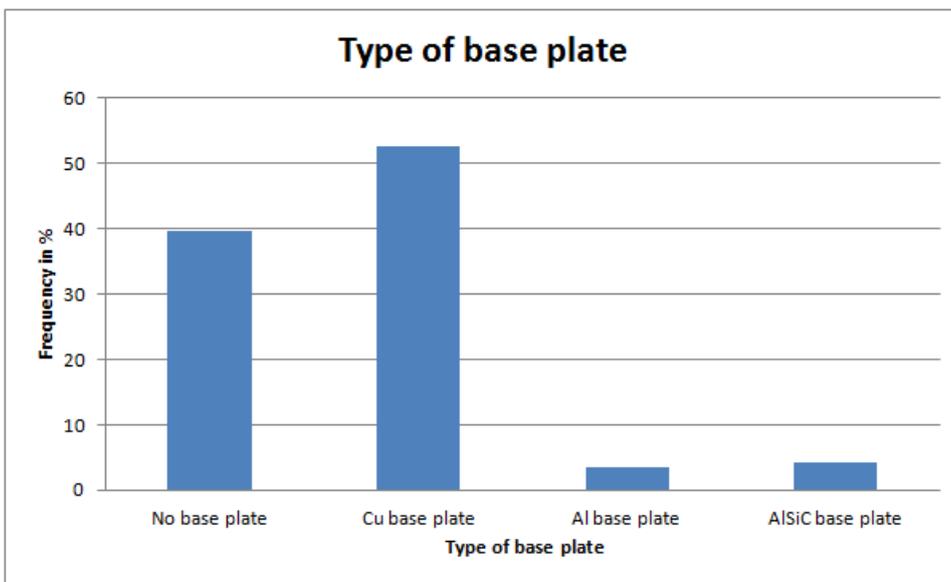


Figure 1.30: Histogram showing the type of base plate in the tested modules

The DCB attach, which corresponds to the joint between the lower Cu layer of the DCB and the base plate, is at 96% achieved via soldering. The rest of joints are Ag sintered. For more than 60% of the solder joints, the type of alloy used was not specified. But, by analyzing the collected data, it appears clearly that for this joint, lead-rich alloys are preferred by far (Figure 1.31). Indeed, in order to avoid the remelting of the alloy used for the die attach during soldering steps in production, high-lead alloys with melting point above 260°C are used. Due to a lack of cost-effective lead-free alternatives, those alloys are exempt from RoHS. Finally, only 18% of the tested modules are epoxy-molded.

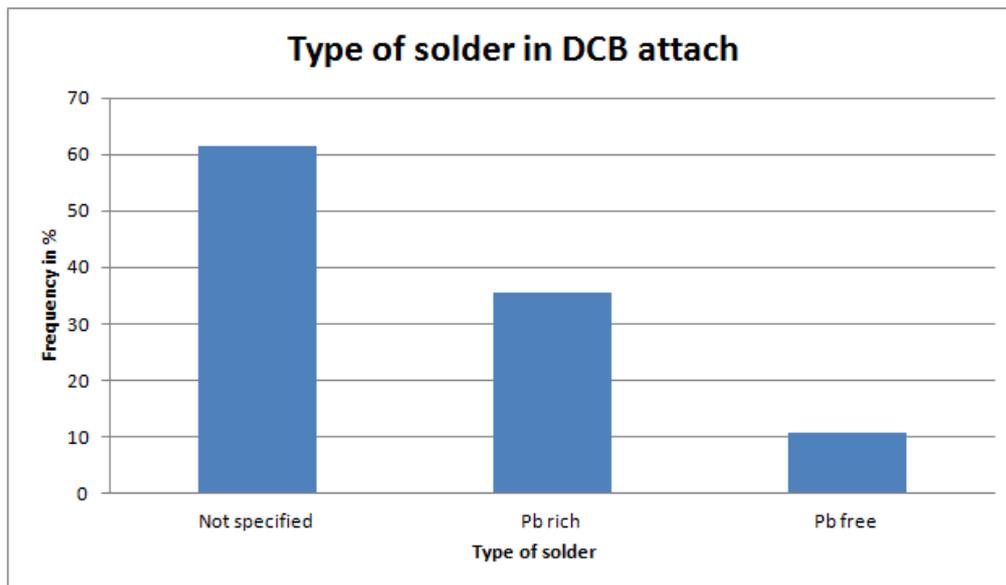


Figure 1.31: Histogram showing the type of solder for the DCB attach of the tested modules

To summarize, most of the DUT were standard IGBT modules, with Al wires, a lead free die attach, a DCB soldered with a lead-rich alloy on a Cu base plate, and without any encapsulant. But one should also notice that quite often a lot of information was missing, like the type of solder for both die attach and DCB attach and the type of DCB that was used.

1.5.4.3 Test methods

Now let's analyze the variety of testing conditions. First concerning the cooling method, fluid-cooled systems are used at 65%, whereas air-cooled systems are used at only 35%.

Moving on to the art of APC test performed, almost all tests are performed with DC current test bench. Only 5% of the tests are PWM tests and not any papers studied the behavior of modules under superimposed test. This comes from the fact that, setting up a test bench able to perform PWM or a combination of PTC and APC is far more complicated than setting up a conventional DC test bench.

The test strategy chosen in 65% is the strategy fixing constant time intervals for t_{on} and t_{off} (Figure 1.32). Almost 20% of tests are done with the " $\Delta T_c = \text{constant}$ " control method. This is the preferred test method, when a multitude of test equipments are connected to a single common cooling loop. Finally, 10% of the tests are using the " $\Delta T_j = \text{constant}$ " and 6% the " $P_v = \text{constant}$ " control methods. Their use remains for academic purposes, or to separate failure modes.

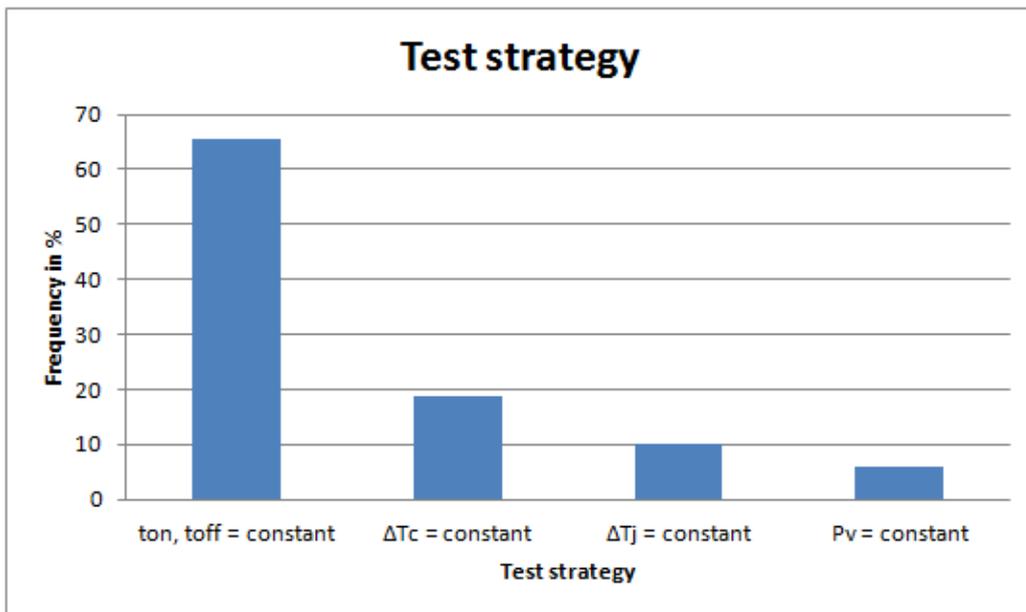


Figure 1.32: Histogram showing the test strategies used to test modules

Regarding the measurement of the junction temperature T_j (Figure 1.33), the preferred method is the Thermo-Sensitive Parameter (TSP). Optic fibers and thermocouples are used in about 10% of cases each. The Infra-red method, despite its accuracy is used only in 5% of cases due to its expensive cost. One can notice that the TSP method is sometimes coupled with a direct measurement method.

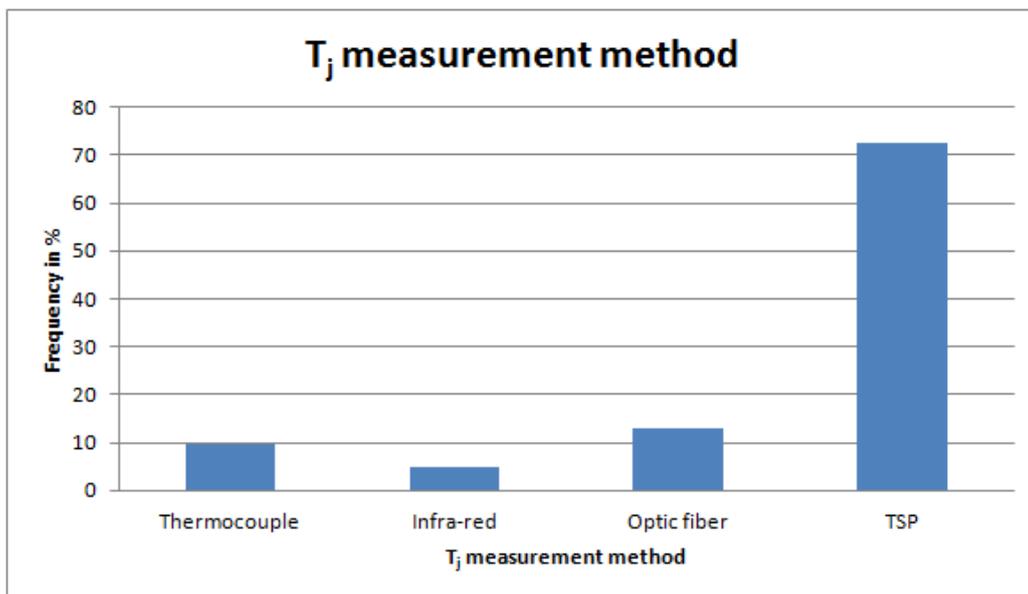


Figure 1.33: Histogram showing the junction temperature's measurement methods

There is quite a large variety of failure criteria (Figure 1.34). The criterion can be based on 6 different parameters: V_{ce} , R_{th} , Z_{th} , R_{DSon} , I_{GES} , or T_{jmax} . Then the amount of the parameter increase is also varying depending on the papers: 5%, 10% or 20% of parameter increase are often used. In some papers no failure criterion is defined and the test last until the complete failure of the device, which is referred as the End of Life of the device. Most of tests are taken an increase of 5% in V_{ce} and of 20% in R_{th} as failure criteria, often in combination. An increase of 20% in V_{ce} is also used as failure criterion in 13% of the tests. The use of R_{DSon} as failure criteria begins to expand.

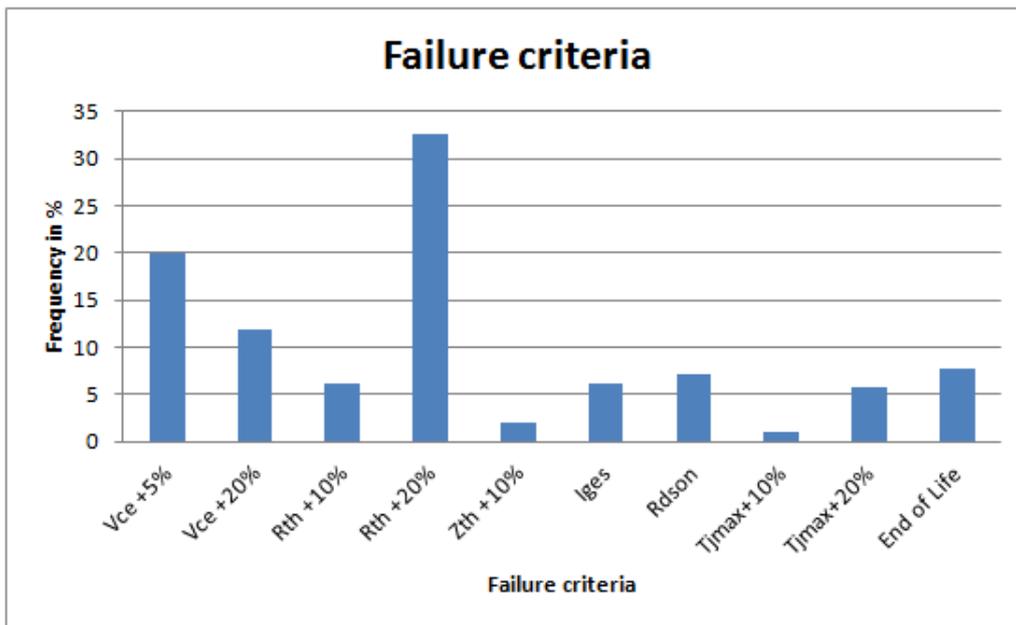


Figure 1.34: Histogram showing the failure criteria in use

Finally the variation of the different test parameters (T_c , ΔT_j , and t_{on}) was reported. Figure 1.35 shows that 39% of papers did not cycles under different test parameters. Those papers are in general more focused on the understanding of the failure mechanisms. For the other papers, the variation of the ΔT_j is often studied. This is done with the perspective to establish a lifetime curve in function of ΔT_j . Variation of T_c is also quite common. But it is remarkable that only about 6% of publications are interested in the influence of t_{on} on APC results. This is a very small amount.

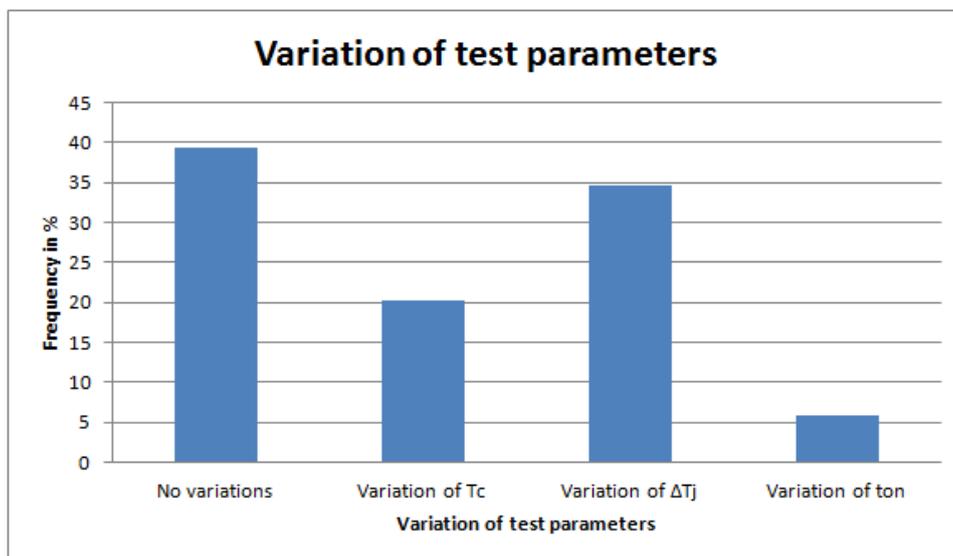


Figure 1.35: Histogram showing the test parameters variations studied

This review of the different test methods used by the 70 publications dealing with APC reveals a quite large variety in terms of control strategies used, as well as temperature measurement methods and failure criteria applied. This can generate a wide spread range of number of cycles to failure for the same kind of module under investigation.

1.5.4.4 Results analysis and interpretations

In most of cases, once APC tests are done, a failure analysis is performed. About 35% of the publications are scanning the modules with an Acoustic Microscope (SAM) in order to detect delamination. An Optical

Microscope (OM) and a Scanning Electron Microscope (SEM) are both used to analyze 17% of the samples. Cross-sections in the samples are often cut for a detailed observation of the internal structure (15%). More rarely specimens are investigated with techniques like X-ray, Focused Ion Beam (FIB), Differential Interference Contrast Microscope (DICM) or Transmission Electron Microscope (TEM). In papers focusing on wire bonds, shear or pull tests were performed on connected wires, to evaluate their degradation range (Figure 1.36).

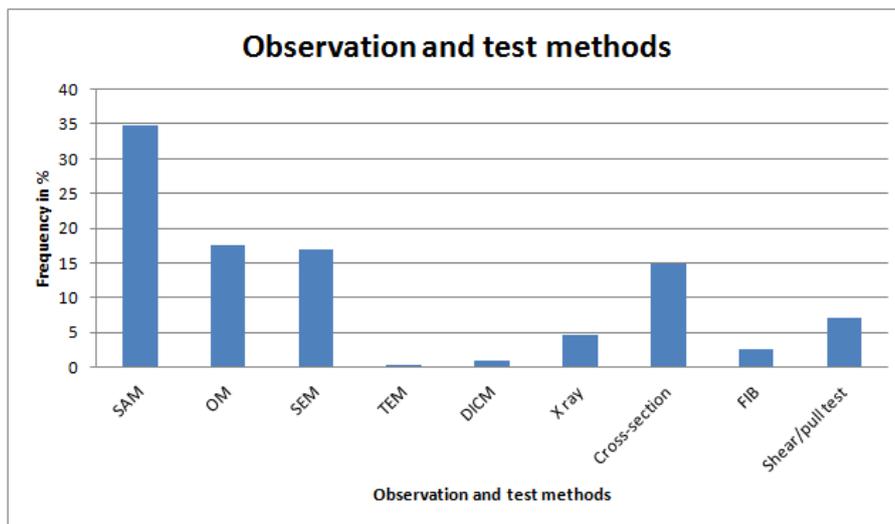


Figure 1.36: Histogram showing the observations and tests methods in use

Failure analyses are often dedicated to study one particular layer of the module (Figure 1.37). In more than 30% of cases, the die attach is the center of interest, followed by wire bonds studied in 28% of papers. The chip metallization on top of the chip is also frequently observed (18%), as well as the DCB attach (15%). These results are quite logical as the main failure mechanisms appearing in power modules are wire bond lift-off or cracking and delamination of solder layers. The Al reconstruction is also a failure mechanism known and discussed since the beginning of APC [Cia96]. The chip and the DCB are not really in focus as failures rarely occur there. The formation and growth of intermetallic at the solder layers is observed only in the few papers that are studying deeply the micro-structural changes. The molding compound is also rarely studied, probably because only 18% of the tested devices were encapsulated.

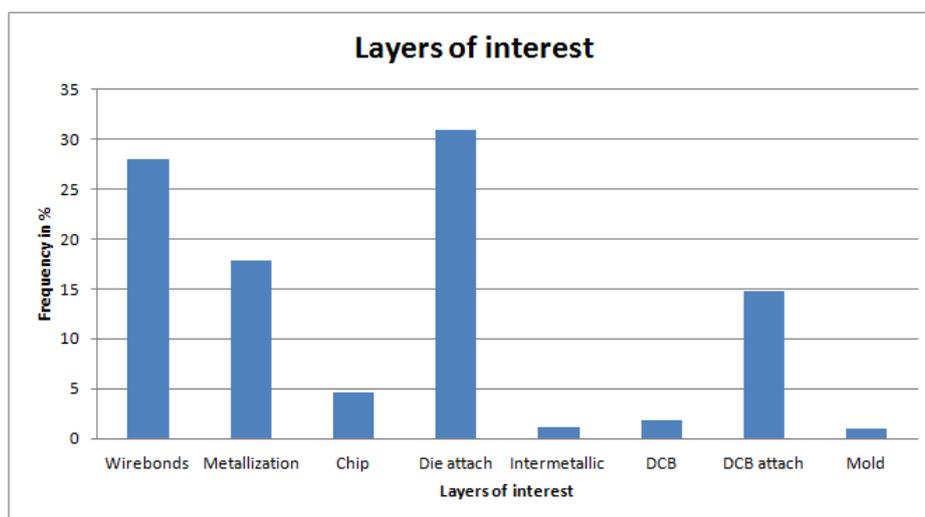


Figure 1.37: Histogram showing the layers of interest in failure analyses

The final goals of those studies were identified and classified in 10 categories (Figure 1.38). The influence of the design and the process is the most important goal with a frequency of 23%. In these studies, differences between the same type of semiconductor coming from different manufacturers, or modules with different geometries and/or dimensions, or even with different materials or joining processes are investigated and compared. It often results in a comparison of lifetime models. Lifetime prediction is frequently the ultimate

goal of APC publications (20%). Quite often the lifetime predictions are modeled in the form of a curve in function of ΔT_j , which necessitate studying the influence of the temperature (T_c and ΔT_j). Before to be able to develop a lifetime model, the failure mechanisms have first to be known and understood, that is why 14% of the papers are doing a failure analysis. To monitor and detect failure apparition a correlation between the evolution of one parameter and the corresponding failure status would be of great help. This was done in 9% of the studies, with for example a correlation determined between the R_{DSon} value and the delamination area in the die attach [Kho07]. Some other publications are proposing adequate test methods to investigate either solder degradations or wire bond failures, or some control strategies to reflect well working conditions. A comparison between failure mechanisms occurring in PTC and APC was made in a few papers [Bou08, Lau07]. For some others, the main goal was to have a precise idea of the temperature distribution in the whole module, or to investigate the effects of t_{on} on APC results, or to study in detail the micro-structural mechanisms that are taking place in different layers.

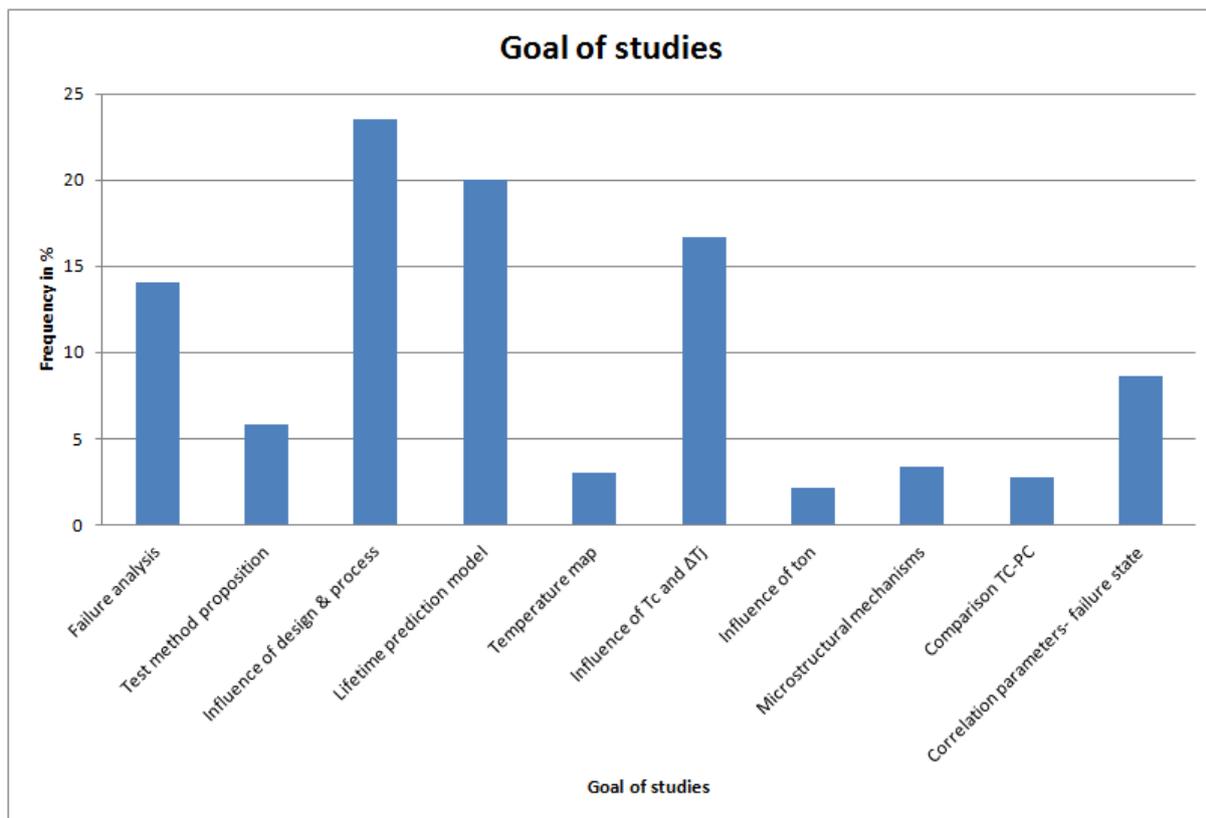


Figure 1.38: Histogram showing the goals of the studies

It comes out that, most of the studies are focusing on determining the lifetime of improved devices in function of the temperature swing, with wire bonds and solder degradation as the main failure mechanisms. Which makes sense as the semiconductor lifetime is a key factor for a sustainable use of devices and the optimization of its reliability.

1.5.4.5 Lifetime prediction

In order to have an overview of all the APC results obtained from 1993 until now, all the number of cycles to failure that were published versus the temperature swing were plotted Figure 1.39. The interpretation of the graphic is limited because as just seen, many different devices were tested, with different test conditions. Moreover, the lifetime is not only dependent on the temperature swing but also on other test parameters, influencing thus the results of the tests. However, the temperature swing is a parameter of such a big importance, that a trend line can emerge from the graphic.

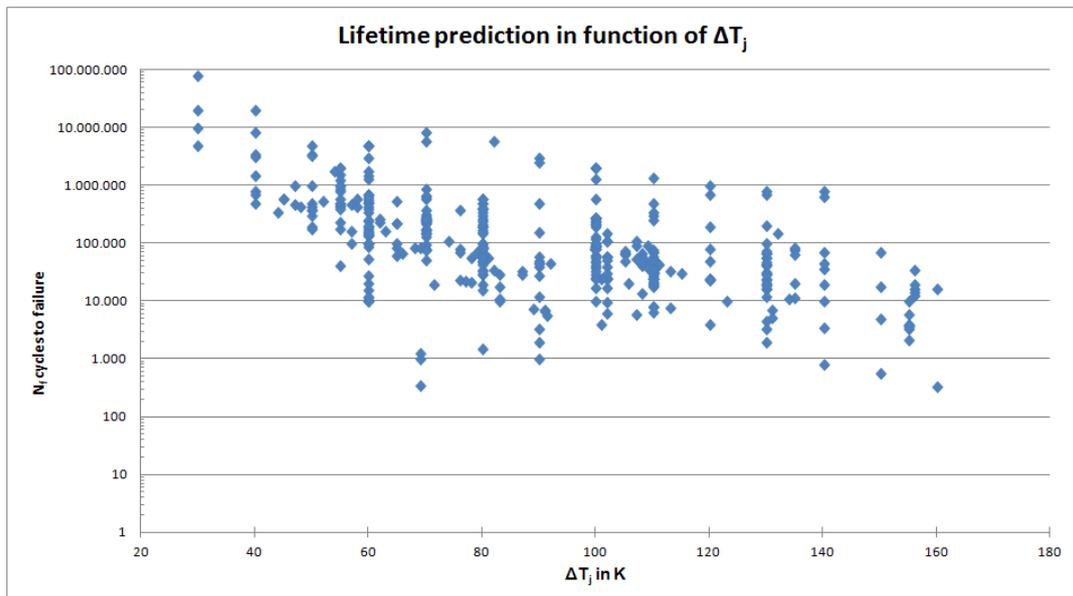


Figure 1.39: Number of cycles to failure versus the temperature swing ΔT_j

The number of cycles to failure versus T_{jmin} was plotted in Figure 1.40. T_{jmin} is also a test parameter of influence but, here it is difficult to make any interpretation of the results or to distinguish a trend line.

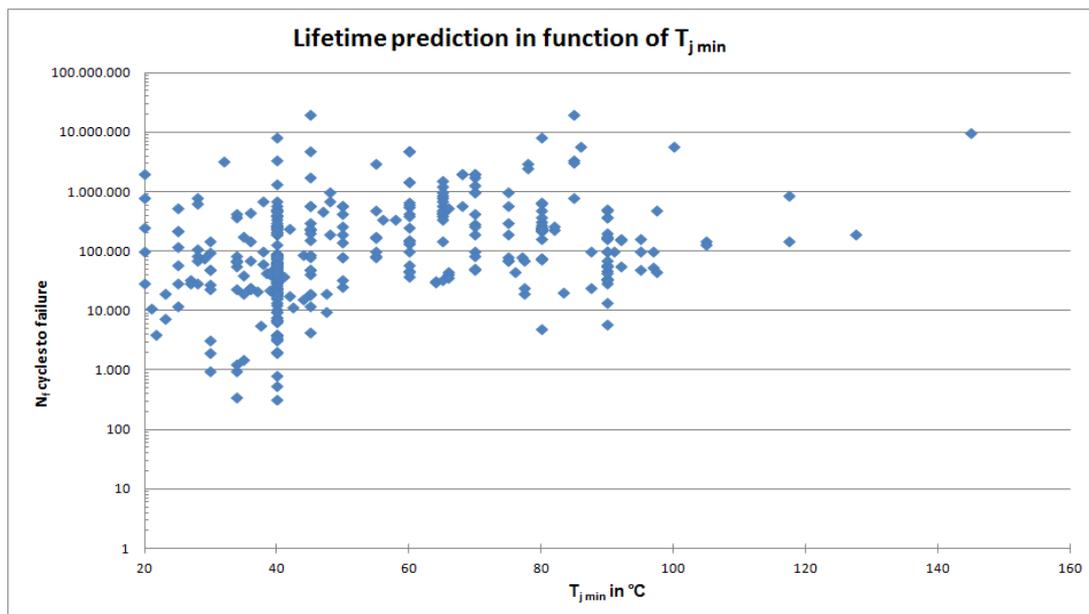


Figure 1.40: Number of cycles to failure versus the minimum junction temperature T_{jmin}

Finally the influence of the heating time t_{on} on the lifetime was studied Figure 1.41. Unfortunately this information was missing quite often, which results in a smaller data set than for the other diagrams. Some papers did state the cycle times but without mentioning the ratio of on and off time.

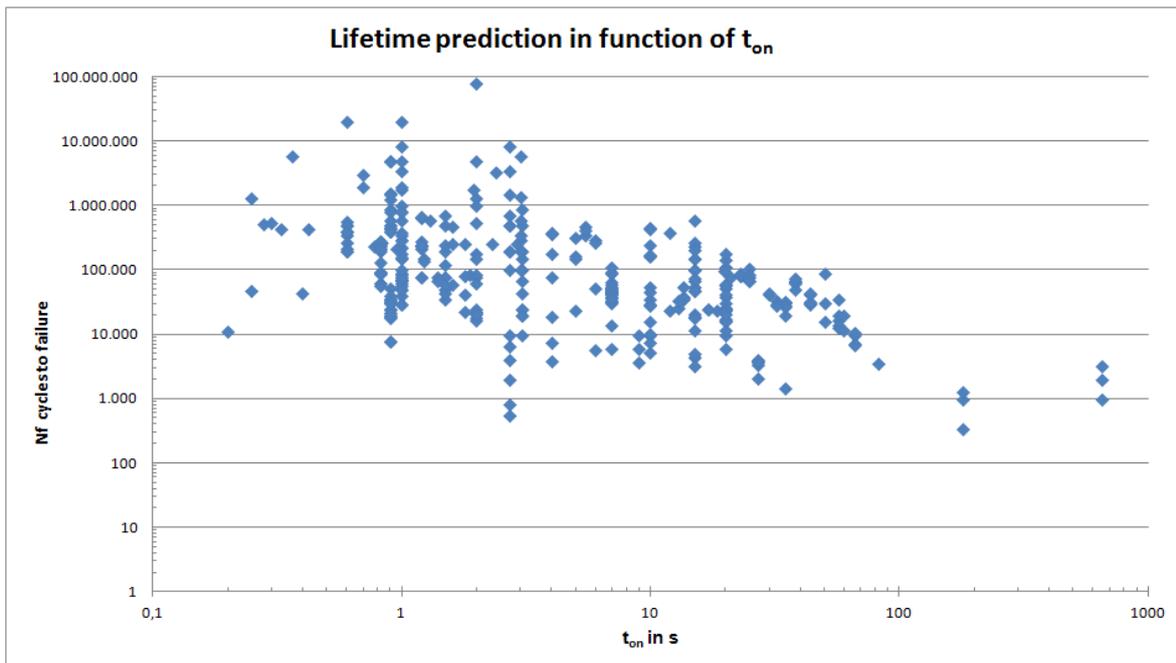


Figure 1.41: Number of cycles to failure versus the heating time t_{on}

This study shows that despite the fact that most of the publications are investigating standard modules with a focus on wire bonds and solder degradations, the variety of test set-up, measurement and monitoring methods as well as control strategies influenced significantly the APC results. This diversity of test methods was also highlighted by [Hut14]. For the authors, this variety of test methods might be due to the fact that an international standard for APC does not exist. In fact, there are several standards [DIN10, JESD07, MIL13] that differ in regards to the main focus of the test.

Moreover, the study reveals that the influence of test parameters on the lifetime was not extensively studied. Especially the influence of the heating time was neglected. This can be partially explained by the fact that testing a high number of cycles requires long test times of the order of several months. This implies that testing of a wide range of application condition is not feasible. To overcome all these difficulties, a solution could be to simulate APC. Indeed, the problem of test methods diversity would be reduced and it is not time consuming anymore to simulate APC with varying test parameters.

1.6 State of the art in Active Power Cycling (APC) simulation

1.6.1 Methods to simulate APC

First observation: there is less literature available on APC simulation than on APC test, and papers are more recent. Different methods to simulate APC exist. Some papers are simulating APC via an equivalent electronic RC circuit with a current source. The electric current corresponds to the power loss, the voltage of the resistor corresponds to the temperature difference ΔT_j , the electrical capacitance C to the thermal capacitance C_{th} and the electrical resistance to the thermal resistance R_{th} [Iko12]. Boundary Element Method (BEM) and Finite Element Method (FEM) are also often employed. Those methods will be the center of our interest. Simulating APC with FEM is more complex than simulating PTC. Indeed, for APC a coupling of analyses, like an electro-thermal analysis or a thermo-mechanical analysis, is required. For an electro-thermal simulation, first an electrical analysis is made: the electrical properties of the different materials should be registered (electrical conductivity, resistivity...) and a current pulse is simulated as the loading condition. At the end of this first analysis, the voltage mapping of the device in function of the time is known. This voltage mapping will then be the load in the second analysis, the thermal one. The thermal properties of the material (specific heat, heat conductivity) should also be implemented in the model as well as some thermal boundary conditions. For example, the environment temperature, and the heat sink temperature. After calculation, the temperature mapping of the device in function of the time is determined. In a thermo-mechanical analysis, the loading conditions for the first analysis are thermal. The environment and heat sink temperature, and/or convection factor of the air or of the cooling system should be known. Then, an internal heat generation is

simulated in the chip for a determined time. This corresponds to the current pulse of APC. Of course, the thermal material properties are also registered. After calculation the temperature distribution of the device in function of the time is available. This temperature distribution will then be the load in the second analysis, the mechanical one. The mechanical properties (Young's modulus, Poisson's coefficient, CTE) are implemented. A boundary condition like a fixation point is added. Then the mechanical analysis delivered a deformation map of the module from which stresses and strains are derived. In some few cases, electro-thermal simulations were followed by a thermo-mechanical simulation to accurately simulate APC. As this coupling of analysis required a long calculation time, some approximations should be made by modeling the device. For example, a 3D model with symmetries can be reduced to 2D, or the mesh can be refined in important areas but coarsen in others. Some models are also focusing only on the layers of interest, like wire bonds, or a bi-layer with the die and its metallization. In some other cases, the whole module is modeled, but without the thinnest layers. The accuracy of materials properties is also an issue, as implemented e.g. complex viscoplastic behavior will increase the calculation time, in the case of a mechanical analysis. Sometimes this problem was solved by considering all material layers to have a simple linear behavior, except the material of interest which was precisely modeled with temperature dependencies and a plasticity model.

1.6.2 Review of papers on FEM simulations of APC

In the same way as it was done for APC tests, 27 publications from 1997 to 2014 dealing with APC simulations were reviewed [RefSimu]. All simulations were using FEM except 2 of them which chosen BEM in order to simplify the problem to solve [Kha01, Car03].

1.6.2.1 Type of device simulated

First of all, the type of the component under study was analyzed, Figure 1.42. IGBTs are once again the preferred device as they are simulated in 65% of publications. Then, come MOSFETs and diodes which are both modeled in approximately 10% of the papers studied. TRIAC and DMOS are rarely modeled as these 2 kinds of device appear only in 7% of publications each. 75% of these devices were modeled in 3D, and only 25% in 2D.

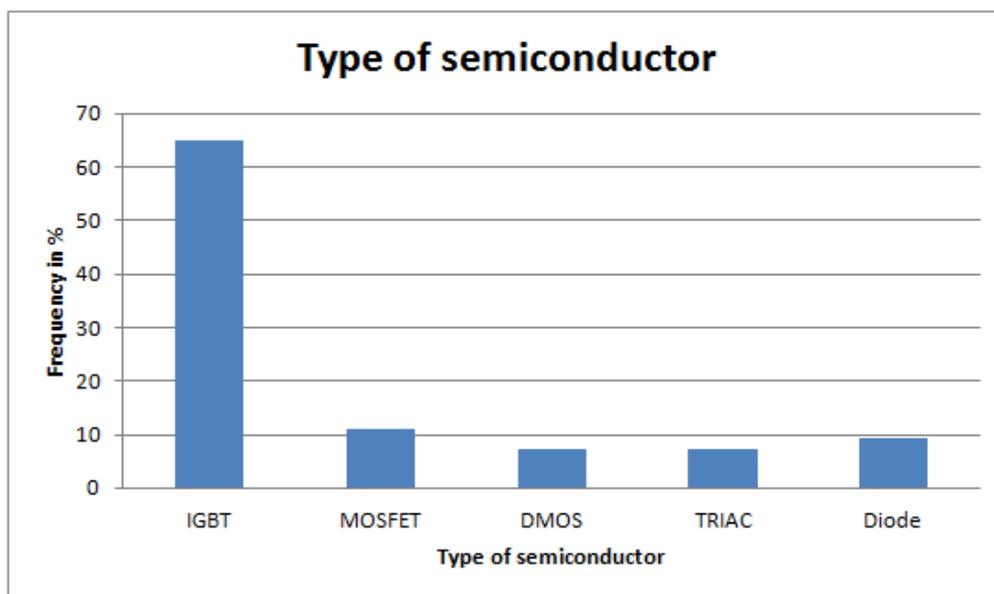


Figure 1.42: Histogram showing the type of semiconductors simulated

The internal architecture of the different models was also observed. For 56% of simulations, interconnects were not part of the model, when those were supposed to be Al wires. This can be explained by the fact that modeling a wire is complex, because of its geometry. So, if the study is not especially focused on wire bonds, those ones can be removed from the model for sake of simplicity. On the other hand, 32% of publications did pay attention to wires behavior by including them in the model. Cu clip, Al stripes and Cu wires were modeled as interconnects in respectively 7%, 4% and 1% of papers (Figure 1.43). When Al wires were modeled, they were considered to have linear elastic properties except in one a paper [Hun13] which included

temperature dependencies and plastic properties. Ag stripes were also modeled with an elasto-plastic behavior, whereas Cu clips and wires were described as linear elastic material.

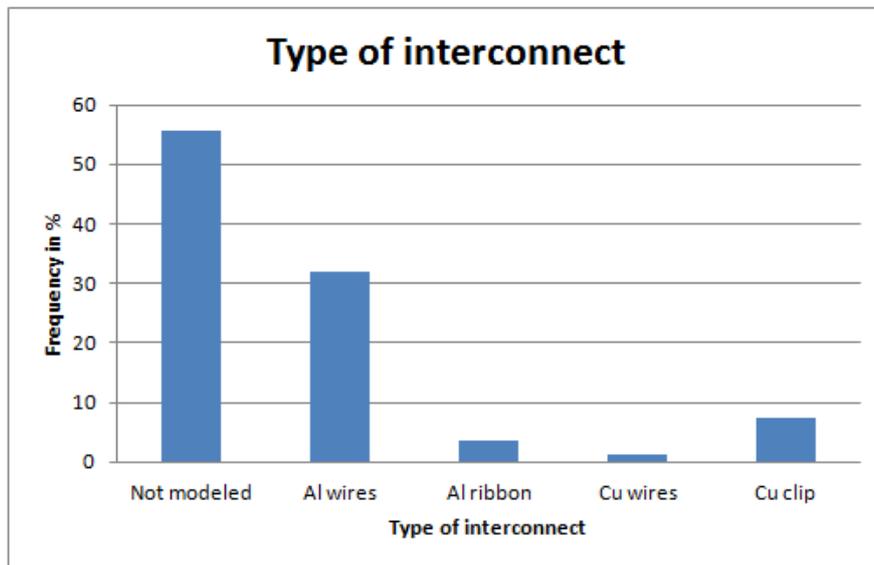


Figure 1.43: Histogram showing the type of interconnect of simulated modules

Almost all devices simulated were supposed to have a metallization of Al, but this layer was modeled in only 22% of simulations. On the other hand, every time that the metallization was included in a model, it was with precise material models that took into account the temperature dependencies and the elasto-plastic behavior of Al. The die itself was made of silicon except for 2% of cases which had SiC, and the die was always modeled with a linear elastic behavior.

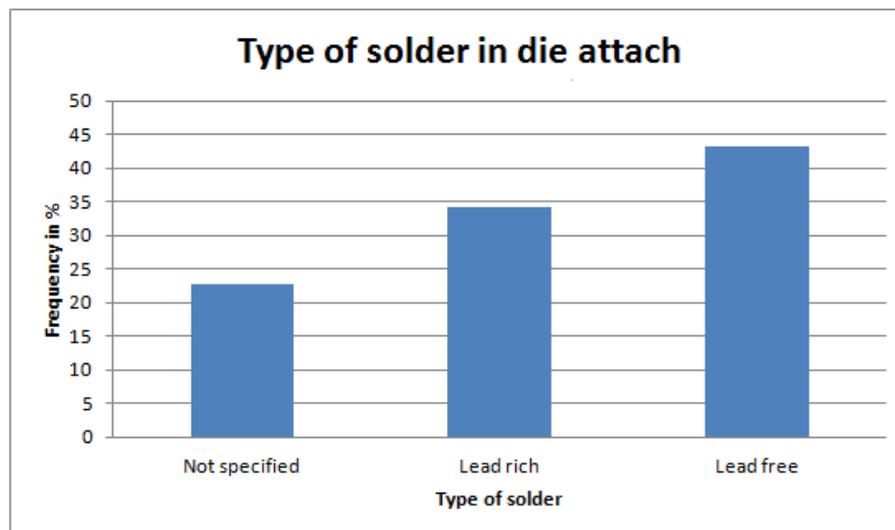


Figure 1.44: Histogram showing the type of solder alloy in the die attach of simulated modules

For the die attach, only 8% were Ag sinter joints, the rest was solder joints. Among these solder joints, lead free alloys were used in a majority of cases with 43% of occurrence while lead rich solders were used in 34% of solder layers (Figure 1.44). The solder alloy was not mentioned in 23% of papers. Concerning the mechanical behavior of these die attaches, almost 50% were described with a viscoplastic model. Plastic-creep and elastic-plastic models were both employed in about 12% of publications. In 10% of simulations, a simple elastic model was applied for the joint and the other papers did not mention anything on material properties (Figure 1.45).

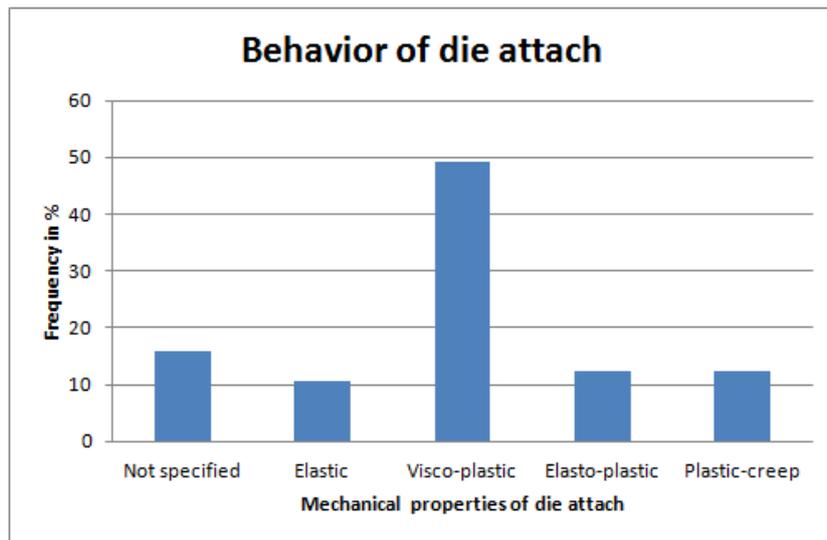


Figure 1.45: Histogram showing the die attach mechanical behaviors of simulation models

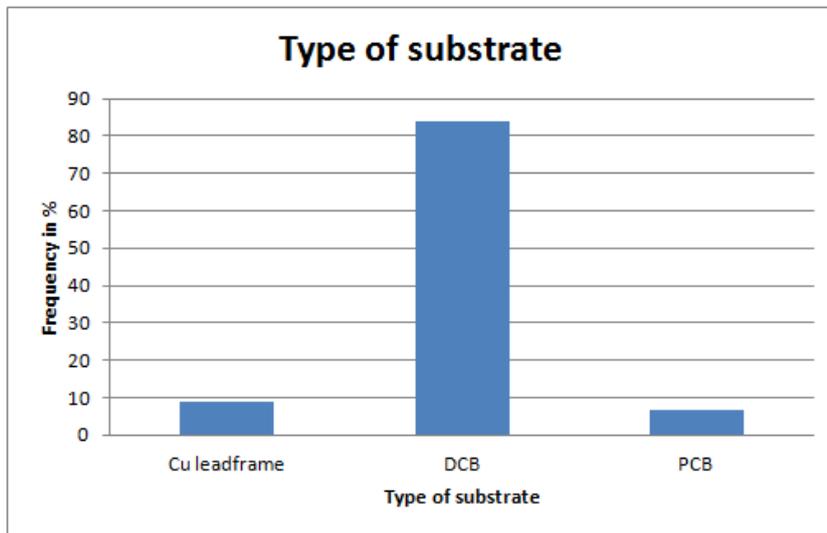


Figure 1.46: Histogram showing the type of substrate in simulated modules

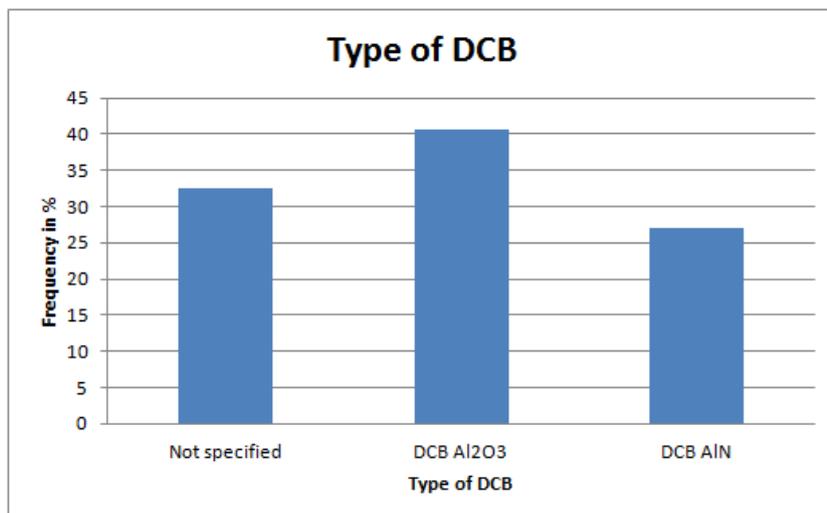


Figure 1.47: Histogram showing the type of DCB in modules simulated

Die was attached to a DCB in 84% of the simulated devices, 9% had a Cu lead frame and the 7% left a PCB (Figure 1.46). The type of DCB used was made with Al₂O₃ ceramic to 40% and with AlN to 27%.

The 32% left did not specify the type of DCB, which is already a high amount. Cu layers of DCB were considered elastic or elasto-plastic and the ceramic was always linear elastic (Figure 1.47).

33% of modules simulated did not have a base plate. The others were built with a Cu base plate, described with elastic or elasto-plastic material model. The DCB was always soldered to the base plate. In 40% of papers no information concerning the solder alloy was found. A lead rich alloy was employed in 32% and the 28% left were soldered with lead free alloy (Figure 1.48).

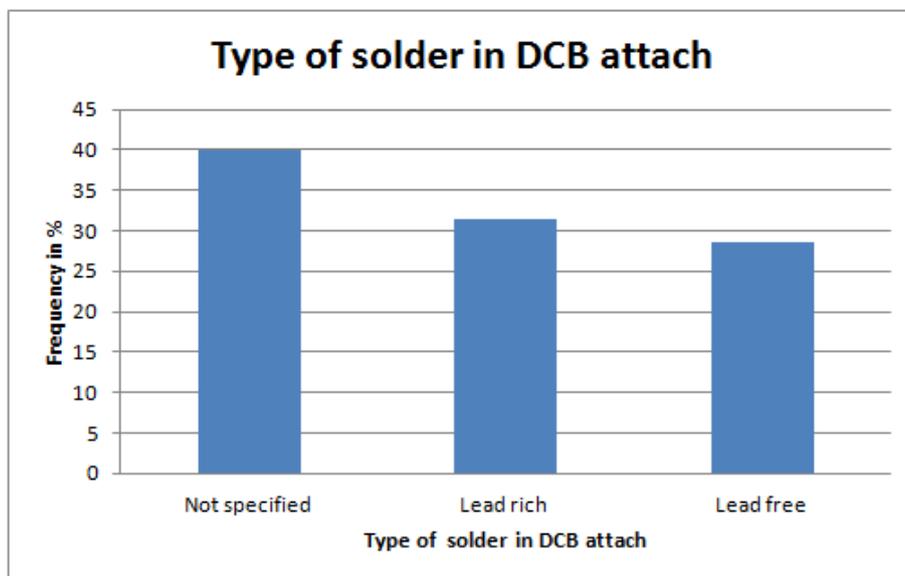


Figure 1.48: Histogram showing the type of solder in DCB attach of simulated modules

27% of papers did not precise what material model was used to describe the mechanical behavior of solder. More than 30% of simulations were performed assuming a viscoplastic behavior for solders, whereas plastic-creep, elasto-plastic and elastic behavior were used in 14% each. For the DCB attach less information was available about the material model than for the die attach. Nevertheless both distributions are following the same trend with a predominance of viscoplastic model compared to elastic, elasto-plastic or plastic-creep model (Figure 1.49).

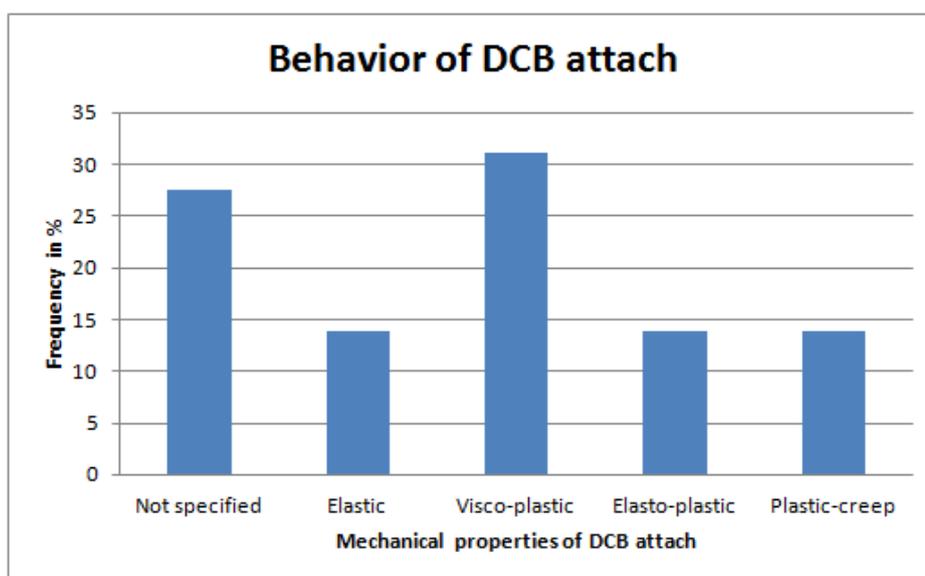


Figure 1.49: Histogram showing the type of DCB attach mechanical behaviors in simulated modules

Only 14% of modules were epoxy molded. For 25% of them, the mechanical behavior of the mold was not mentioned. Half of papers considered the molding compound to be elastic, whereas only 25% took into account the viscoplastic behavior of the encapsulant.

To summarize, the type of modules that were simulated in publications, corresponds to the ones which were submitted to APC tests. Indeed, IGBT is once again the device the most studied. The internal architecture corresponds most of the time to a standard one with Al wires, a chip soldered on a DCB, itself soldered onto a Cu base plate. But in simulations, one can simplify the model to be studied, and quite frequently the Al wire bonds were not included in the model because of their complex geometry. The same was also observed for the metallization which was often neglected due to its very small dimensions. Quite often information about materials and their assumed behavior were missing especially concerning DCB and DCB attach. Moreover, a relatively wide variety of material models were used in the different simulations.

1.6.2.2 Type of analysis and loading conditions

The type of APC test the most simulated is the DC current test in 90% of the papers studied. Tests with PWM and superimposed tests are simulated in about 5% of the cases. This distribution of simulated tests is similar to the one of experimental tests. This is due to the fact that simulation's models are often validated with the help of experiments and results of both experiments and simulations are compared. Moreover, just like for experiments, simulating DC current APC is easier than simulating PWM or superimposed tests. However, it is to notice that superimposed tests were simulated, whereas no experimental tests were performed. This showing that even though superimposed tests are complex to model, it is still easier to simulate such a test than to set up a complete test bench.

The type of analysis use to simulate APC was also taken into account. 26% of simulations are electro-thermal and 67% are thermo-mechanical analysis. Some papers did both kinds of simulations one after the other [Anz08, Cel11, Shi10, Hun13]. The 7% left were purely thermal simulations.

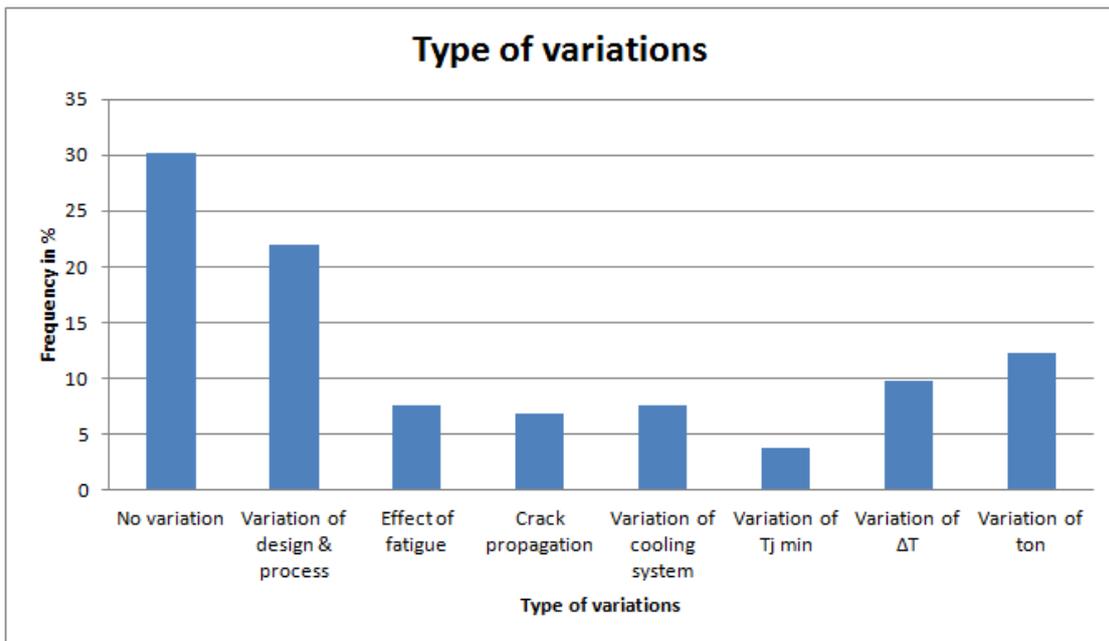


Figure 1.50: Histogram showing the type of variations studied with simulation

The different parameters variations and design effects studied were identified and plotted in Figure 1.50. 30% of papers did not manage to perform any variations neither of test parameters nor of design. 22% made variations in geometrical design, materials and process. ΔT_j and t_{on} variations were studied in respectively 9% and 12% of simulations. 7% of papers choose to study respectively variations of cooling system, the effect of fatigue by including delamination areas in the model, and crack propagation under APC. Other few studies focused on the variations of $T_{j\min}$. This shows that a wide range of test parameters variations were studied in a relatively small amount of publications.

1.6.2.3 Results analysis and interpretations

Layers on which papers are focusing were reported, and the corresponding distribution is shown Figure 1.51. The first layer of interest appears clearly: the die attach was in focus in 36% of papers. The chip comes at the second position with 26% of papers that concentrate on its behavior. Wire bonds are also of big interest for

10% of studies. The DCB and metallization have both 9% of publications focusing on them. Surprisingly the DCB attach was the object of study for only 8% of papers. The difference of interest between the die attach and DCB attach is quite important, although both solder joints are subjected to degradation under APC. This can be explained by the fact that not every module had a base plate and thus a DCB attach layer. But it might also come from the fact that solder degradations are more extensively studied under PTC, as this test is more critical for solder layer due to the long dwell time. The interconnect attach is also not frequently studied, as this layer is only present in modules with a Cu clip instead of wire bonds.

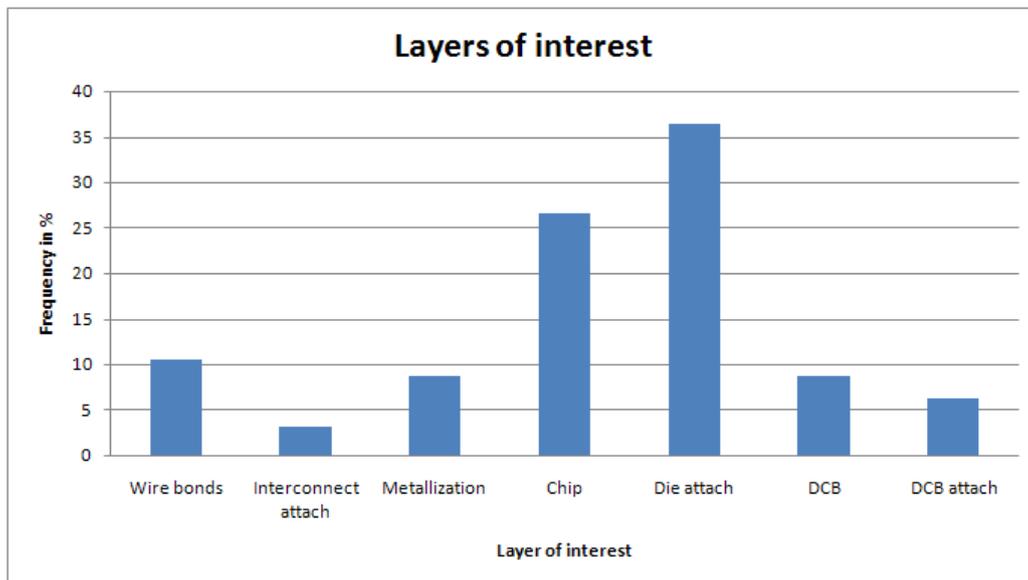


Figure 1.51: Histogram showing the layers of interest in simulations

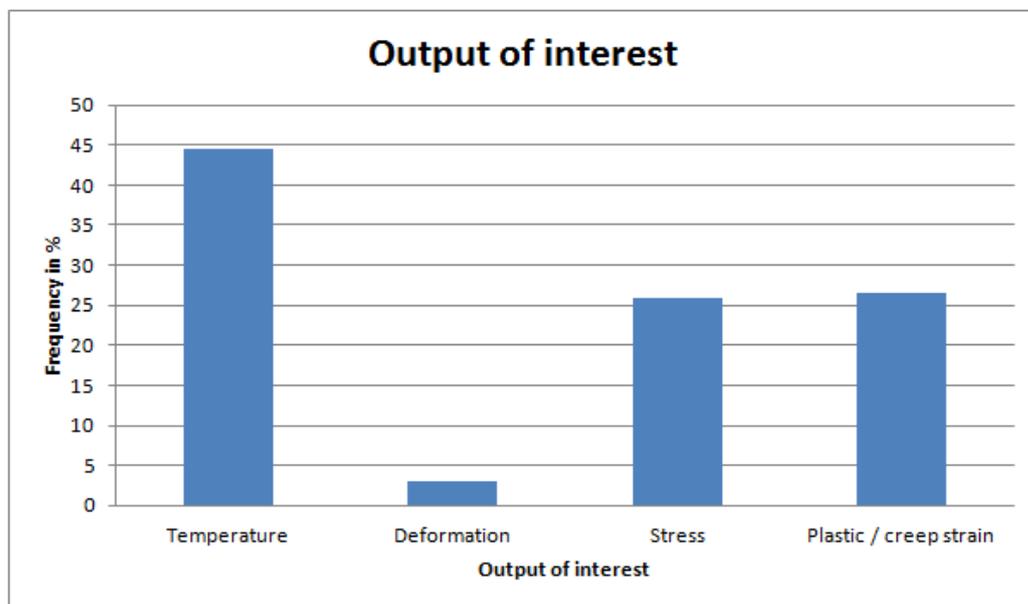


Figure 1.52: Histogram showing the outputs of interest in simulations

The results obtained via simulations were analyzed, and 4 main outputs of interest emerged out of them: temperature, deformation, stress and strain. These results were often shown as a map of the entire module. The voltage was also often observed, but it was not taken into account here, as the focus of this study is not about the electrical behavior of modules but on their thermal and mechanical behavior. Determined the temperature distribution through the module was the first interest of these studies. In about 45% of publications a temperature map was shown. Stresses and strains were also of importance as each of them is discussed in 25% of papers. The deformation was only observed in few papers which were looking more precisely at the phenomenon of metallization reconstruction [Kan11, Smo08] (Figure 1.52).

Finally the different goals of the studies were highlighted and plotted Figure 1.53. The main objective remains to understand the mechanisms that are taking place in modules to 24%. Then 20% of papers are studying design and process optimization. The lifetime prediction is the goal of more than 15% of simulations. 11% of papers wanted to characterize and understand the differences between PTC and APC. Determining the influence of the temperature on the number of cycles to failure was also an important point. Some papers look at the influence of fatigue on the APC results, for example by simulating a delamination area in solder layer. Others wanted to determine the temperature profile of the module during power pulses. Papers which have made PWM power cycling manage to compare the results obtained with both DC current and PWM tests. Few studies also investigated the influence of the cooling system on the APC results of a module. Finally, very few simulations had the objective to study the influence of the heating time t_{on} on the behavior of the module. This is quite surprising as simulation could be an appropriate tool to test different combinations of test parameters, once the model is set up. One can also notice that the goal was quite different depending on the study, a relatively large range of aspects influencing APC results was reviewed. But the main problematic remains to understand mechanisms, make some design optimization and determine the lifetime of modules.

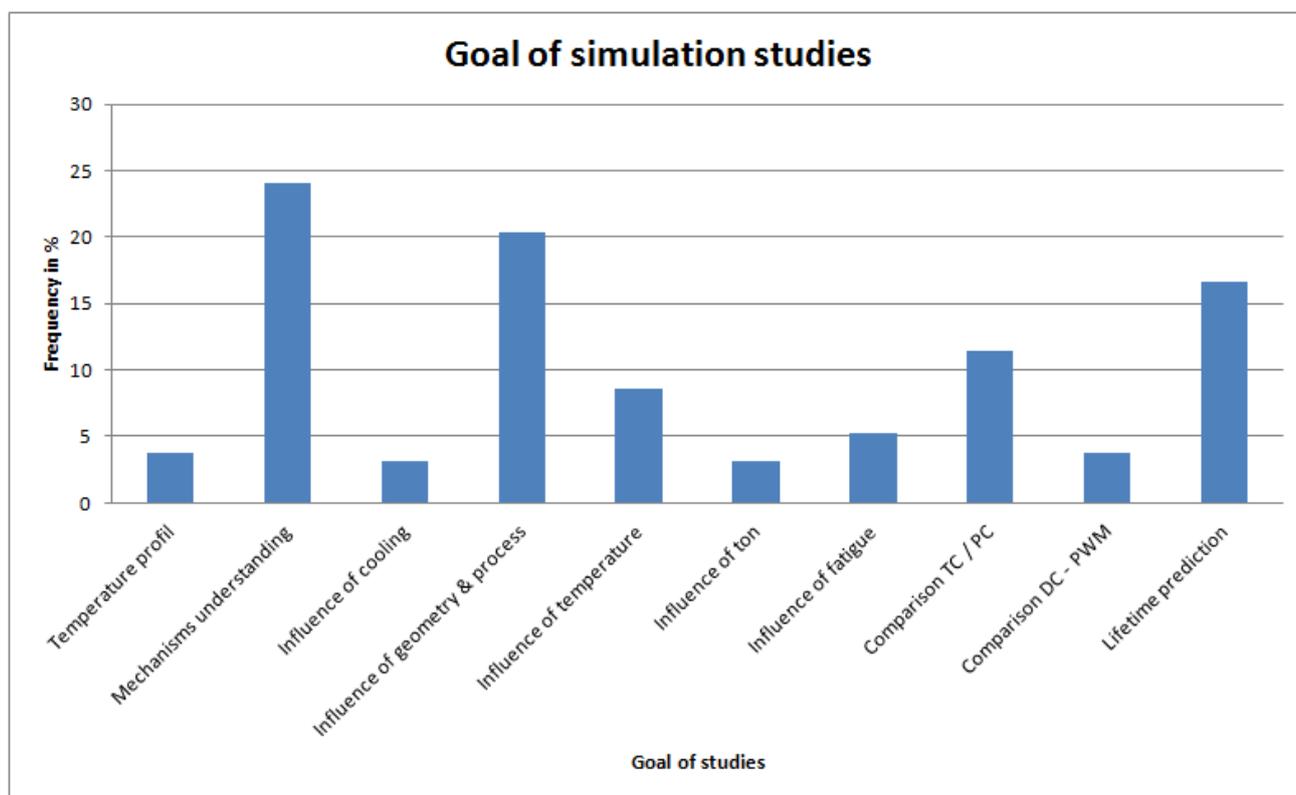


Figure 1.53: Histogram showing the goals of the simulations studies

1.6.2.4 Lifetime prediction based on simulations

Numbers of cycles to failure obtained with simulation were plotted in function of the temperature swing ΔT_j , Figure 1.54. The quantity of data available was quite limited. The difference with the number of data obtained with papers performing APC tests is really important. Plotting the lifetime prediction in function of the heating time or the T_{jmin} was not even possible because of missing data.

To conclude, FEM simulations are still not extensively used to study APC. Until now, studies using simulations are concentrated on standard modules with Al wires as interconnect, an IGBT chip soldered to a DCB, soldered itself to a Cu base plate and without encapsulation. Models are often simplified and are not taking into account all the layers actually present in a module. Too many times, the material model was not mentioned and for some materials the model used to describe the mechanical behavior was not precise enough. Studies are mainly focused on the die attach, the chip and wire bonds. The temperature distribution is still of prime interest, before stress and strain distribution. Main goals of these studies are: first understanding the mechanisms occurring then optimize the design of modules and predict the lifetime. The influence of

many different effects on different test parameters was studied but only superficially. Until now, no publication managing to test different combinations of parameters and report their influences on APC results was found. In simulations just like for experiments the study of the influence of heating time on modules under APC is neglected. But one should take advantage of simulation and study intensively the influence of different combination of parameters on the mechanical behavior of modules. Indeed, in simulation, once a model is set up and validated, it is quite easy to modify some parameters and restart an analysis.

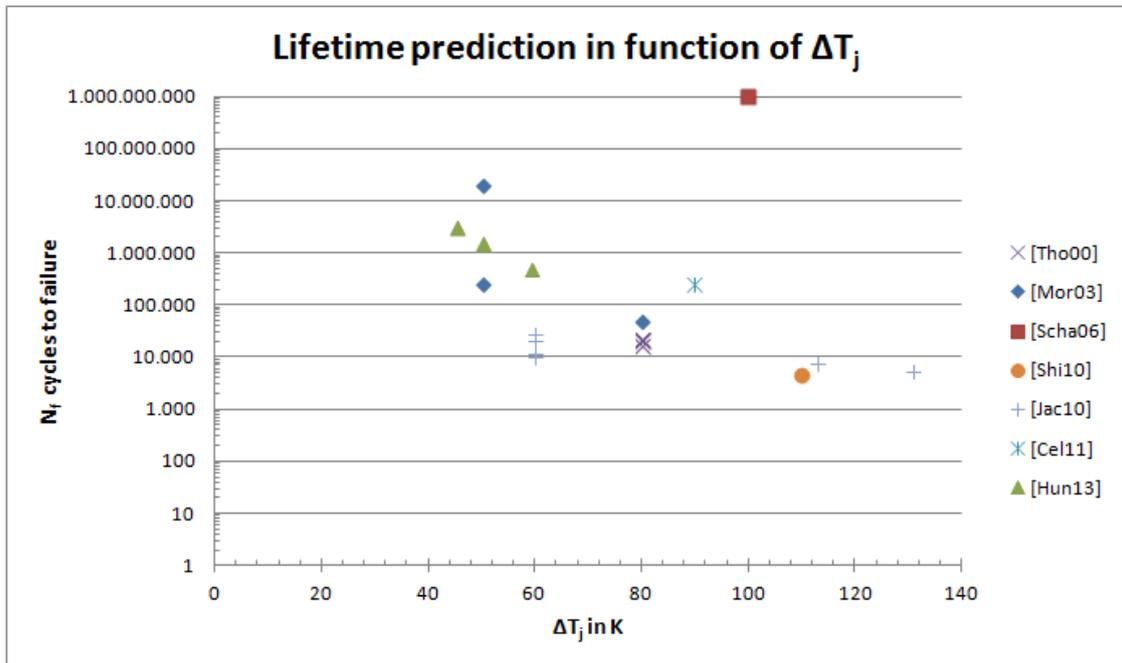


Figure 1.54: Number of cycles to failure predicted via simulation versus the temperature swing ΔT_j

1.7 Conclusion

These studies on the-state of the art in APC tests and simulations reveal that until now the power modules under study correspond to standard modules with Al wires bonded to a Si chip soldered on a DCB, itself soldered on a Cu base plate and without epoxy molding compound. It is only very recently that a few publications are managing to study modules with new technologies like SiC chip or Cu wires or clip or Ag sinter joint. Moreover, it was highlighted that a variety of test methods are available to perform APC tests, leading to quite different reliability results. Besides, performing APC test is time consuming and impedes to carry out a thorough study on the influence of tests parameters on the reliability of power modules. Thus numerical simulations can be considered as an interesting tool to overcome these experimental difficulties and analyze the behavior of power modules under varying test conditions. But actually, the use of simulations to determine the power cycling reliability is still quite recent and not very common. Less than half the number of papers dealing with APC tests was found regarding APC simulations. Furthermore, these studies dealing with APC simulations had quite different goals and were focusing mainly on one or two determined layers. This meaning that, despite the easy reproducibility of an analysis and the rapidity of calculation allowed by simulations, no extensive numerical study on the influence of test parameter on reliability was carried out.

That is why, in this study the thermo-mechanical behavior of a new power package with an epoxy molding compound and using a Cu clip as interconnect instead of Al wires bond is investigated by means of experiments and simulations. Indeed, APC tests and more extensively FEM simulations are used to characterize the influence of three test parameters (T_{jmin} , ΔT_j and t_{on}) on the reliability of this new power module. A detailed model of the power package is developed and the behavior of all material layers is analyzed. In addition fracture mechanics simulations are performed for regions of the module that were found to be subjected to cracking.

2 Presentation of the power module under study

2.1 Description of the module and its internal structure

The electronic component on which this study focuses, is a B6 Bridge power module used as frequency inverters in the steering of electrical cars (Figure 2.1). The module aims at converting the electrical energy of a battery (Direct Current) and distributing it to the motor (Alternating Current). The conversion is performed with 6 MOSFETs. Thus, the B6 Bridge module replaces 6 discrete MOSFETs switches and allows for tighter packing within a control unit.

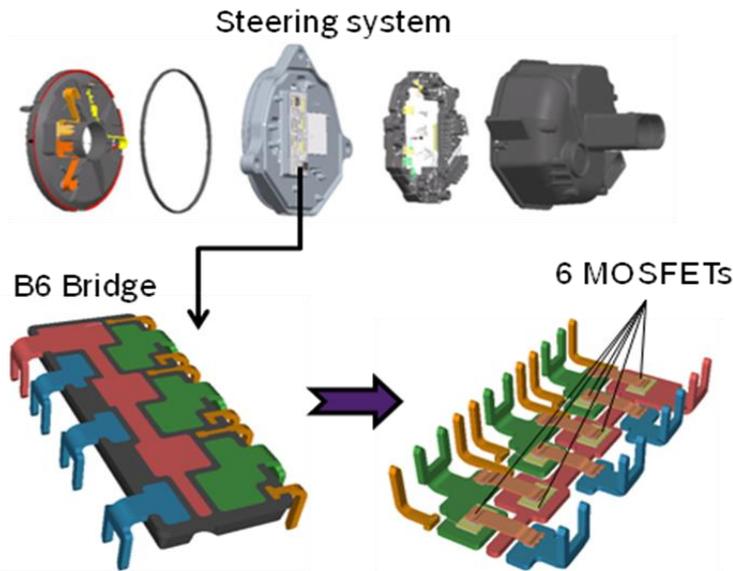


Figure 2.1: The steering system with the B6 Bridge power module

This power module has not a standard design with a chip mounted on a DCB and Al wire bonds as interconnects. Here the chip is mounted on a Cu lead frame with Cu clips as interconnects (Figure 2.2). Additionally the entire module is encapsulated in a robust molding compound. This design was developed in order to increase the reliability of the module. Indeed, like seen in the previous chapter, clips are more robust and allow a better distribution of the current than standard Al wires do. Moreover the encapsulation of the device provides a good protection against moisture and helps to evacuate the heat generated by the chip. The counterpart for an improved reliability is a quite complicated internal structure. Indeed, the use of a Cu clip implies an additional solder layer in order to fix the clip to the die.

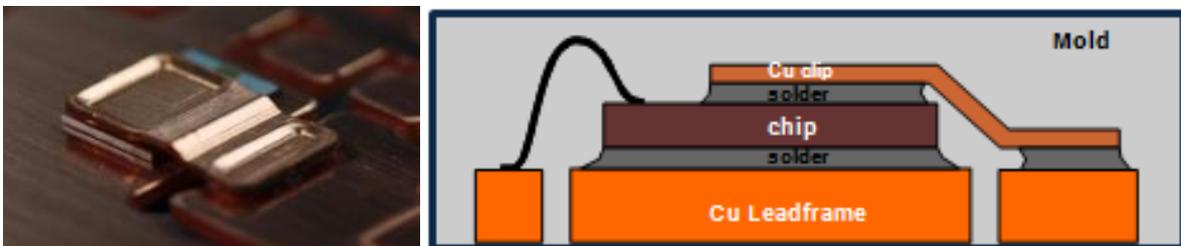


Figure 2.2: On the left a picture of the MOSFET with a copper clip. On the right a schematic cross-section of one MOSFET assembly.

Figure 2.3 details the layer structure between the chip and the Cu clip. The chip is at the bottom of the picture, and is constituted of 3 different layers: the substrate, the active zone and the Al metallization. First, there is the substrate, which is the thickest layer of the chip (about 180 μm). On the schematic, the substrate is not really represented, but would be under the zigzag line. Then, on top of the substrate, comes the active zone made of trenches in the silicon. This active zone of about 20 μm thick is the layer involved in the heat generation through the entire module. A very thin metal barrier separates the active zone from the Al metallization. This metallization is made with an Al alloy (here AlCu) and is quite thin (3-5 μm). To allow

the chip to be soldered on its top side, a thin Ni-based solderable metallization has to be deposited on its surface. Thanks to this layer, the Cu clip can then be soldered to the chip. The solder alloy used in the power module for connecting the clip to the chip but also the chip to the Cu lead frame, is a lead free solder, with tin, silver and copper and called SAC 305 for Sn96,5Ag3Cu0,5. By soldering, some intermetallics are formed at both interfaces of the solder layer: close to copper layers, Cu_6Sn_5 or Cu_3Sn intermetallics are created, while close to the chip there is the formation of $(\text{Cu},\text{Ni})_6\text{Sn}_5$ or Ni_3Sn_4 intermetallics. Those intermetallics remains thin layers of approximately $5\ \mu\text{m}$ but tend to grow with APC.

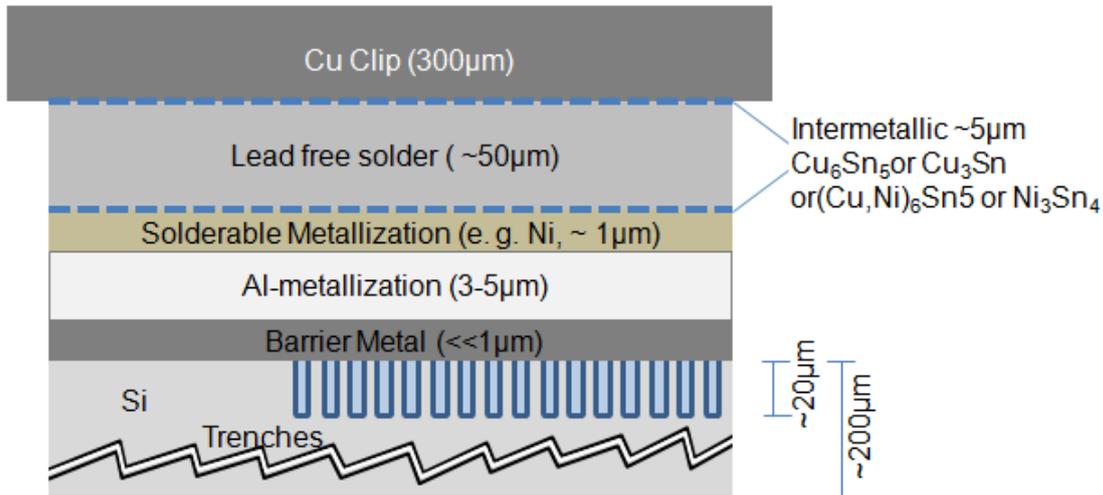


Figure 2.3: Detail of the layer structure between the chip and the Cu clip

2.2 The assembly process of the module

The assembly process is the second phase of the production cycle, after the chip fabrication. The different steps of the assembly process are shown on the Figure 2.4. First, zones of the Cu lead frame corresponding to chip locations are first covered with solder paste. The solder paste consists in a sticky mixture of powdered solder and flux and is applied using a stencil. The die is then precisely positioned and deposited on the solder paste. Another layer of solder paste is deposited on the chip surface, and the clip is mounted on it.

The assembly will then be reflow soldered in a reflow oven in order to create sound joints. The reflow process involves heating the assembly at successively higher temperatures in four stages: preheat, soak, reflow and cooling (Figure 2.5). The first step consists in a rapid rise in temperature ($<3^\circ\text{C}/\text{s}$), which evaporates the solvent from the paste and burns off the largest amount of contaminants. Soak ensures that the solder paste is fully dried before hitting reflow temperatures, and activates the fluxes. At the end of the soak zone a thermal equilibrium of the entire assembly is desired just before the reflow zone. Solder reflow starts happening when the paste is taken to a temperature above the melting point of the solder (also called liquidus), but this temperature must be exceeded by approximately 20°C to ensure quality reflow. The length of time the solder joint is above the liquidus is referred to as the ‘wetting time’. This is normally 60–150s, but if the wetting time is excessive, intermetallics may be too thick in the joint, which results in brittle solder joints. Finally, the assembly is gradually cooled down to solidify the solder joints. Proper cooling inhibits excess intermetallic formation or thermal shock to the components. A moderate cooling rate ($<6^\circ\text{C}/\text{s}$) is chosen to create a fine grain structure that is more mechanically sound.

Once the assembly is properly soldered, the module is ready to be encapsulated through transfer molding. In this process, the module is placed in the mold and the epoxy resin is preheated and loaded into a chamber called the pot. A plunger is then used to force the resin from the pot through channels known as a sprue and runner system into the mold cavities. The mold walls are heated to a temperature above the melting point of the epoxy resin, allowing a faster flow of material through the cavities. The mold remains closed as the resin is inserted and is opened to release the part.

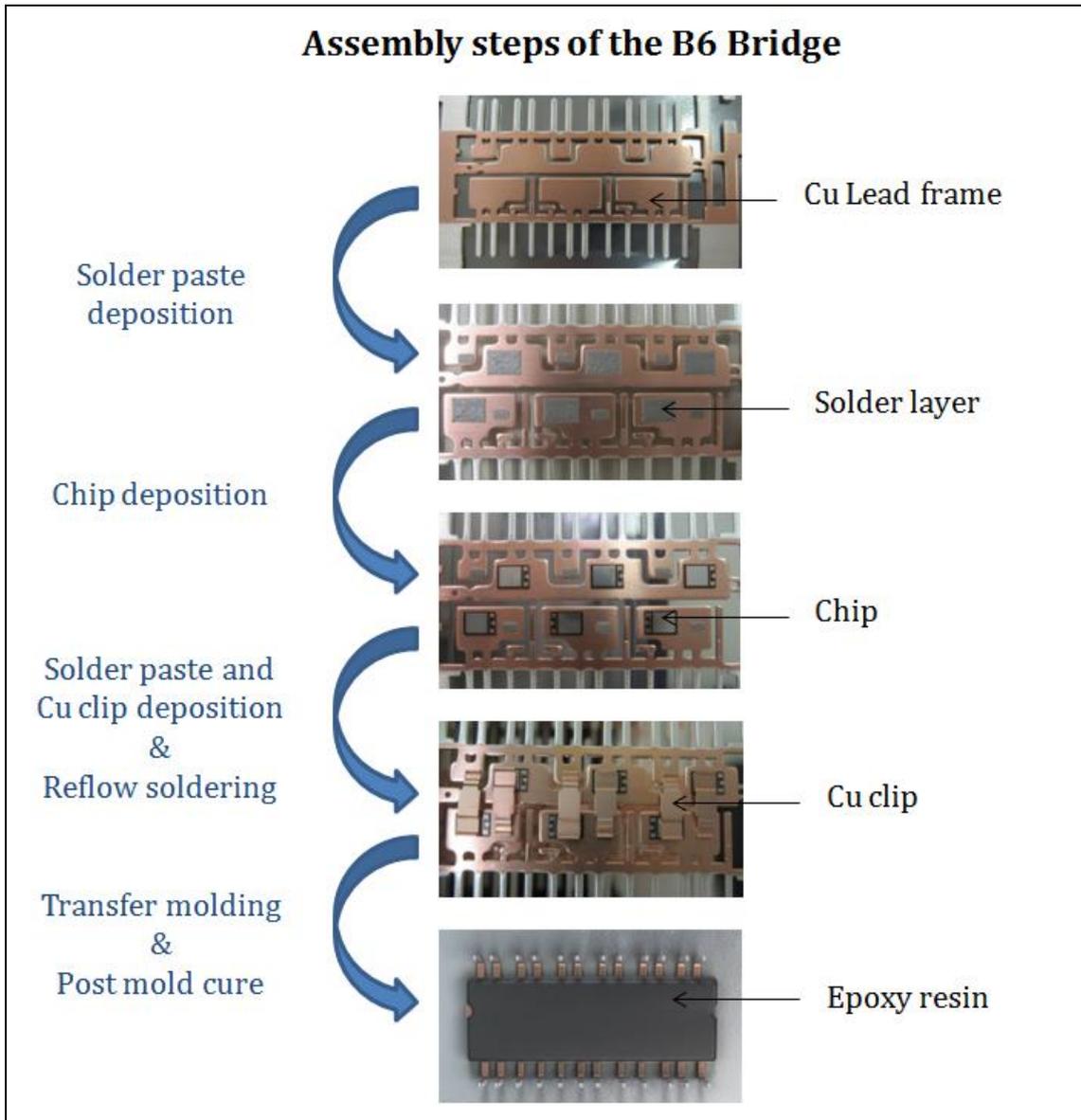


Figure 2.4: Assembly steps of the B6 Bridge

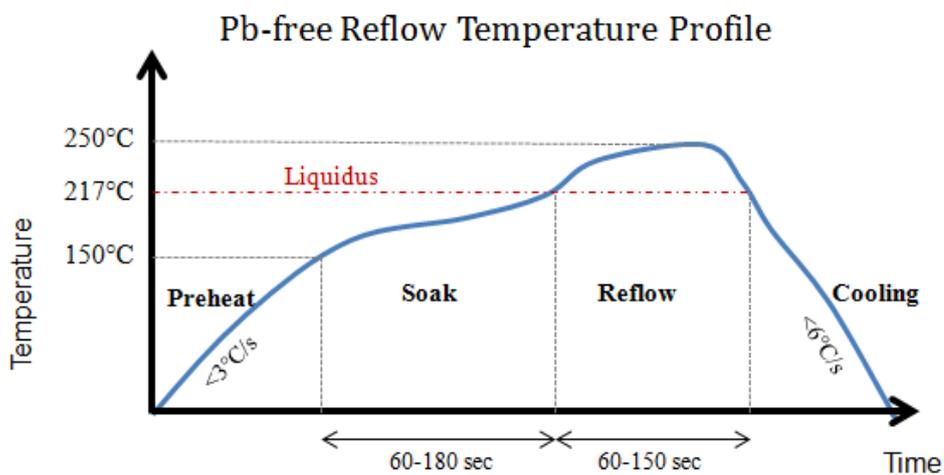


Figure 2.5: A typical reflow temperature profile for Pb-free solder alloys

Once the module is encapsulated, a first curing process at room temperature takes place for at least 12 hours, followed by a post mold cure process. This post curing process consists in exposing the module to elevated temperatures to speed up the curing process and maximize some of the material's physical properties.

Generally modules are post cured in an oven at 175°C for about 4 hours. Post curing expedites the cross-linking process of the polymer's molecules.

Due to this fabrication process, a stress free temperature of 175°C is assumed for the entire module, whereas a stress-free temperature of 195°C is assumed for the mold. A higher stress free temperature is defined for the mold in order to take into account residual stresses due to post mold cure.

2.3 Thermal and mechanical properties of materials

Material properties and material models used to describe the thermo-mechanical behavior of materials in simulations are presented in the following sections. In our simulations models, the Al metallization as well as intermetallics are taken into account in order to precisely simulate the mechanisms occurring inside the module. The solderable metallization and the metal barrier are not included in simulations as they are too thin (<1 μm) to be modeled with the other layers.

2.3.1 The copper lead frame and clip

Cu is a ductile metal with excellent electrical and thermal conductivity. His mechanical properties are quite good and it has a quite high CTE. The lead frame and clip were modeled with a bilinear kinematic hardening to simulate the elasto-plastic behavior of the Cu.

Density (kg/m ³)	Specific Heat (J/kgK)	Heat Conductivity (W/mK)	Young's Modulus (MPa)	Poisson's ratio	CTE (ppm/K)	Elasto-plastic model
8930	385	370	110000	0,34	16,5	Bilinear kinematic hardening

Table 2.1: Table of thermo-mechanical properties of the Cu

2.3.2 The solder

As solder degradation is an important failure mechanism in power module, it is therefore important to accurately model its thermo-mechanical behavior.

Density (kg/m ³)	Temperature (°C)	Specific Heat (J/kgK)	Heat Conductivity (W/mK)	Young's Modulus (MPa)	Poisson's ratio	CTE (ppm/K)
7300	from -73°C to 225°C	238	60	49551 - 32001	0,36	20

Table 2.2: Table of thermo-mechanical properties of the SAC solder alloy

Solder alloys are mainly subjected to creep deformation. The creep is typically a plasticity which occurs at high temperatures: when the temperature is greater than 0,4 T_m where T_m is the melting point in Kelvin. The creep curve at constant stress level describes this deformation as a time function until the fracture of the material (Figure 2.6). Three regions are to be distinguished: the first stage is the primary creep, where the creep rate is decreasing by increasing creep strain or time. The second stage is the secondary creep or steady state creep as the creep rate decreases to a constant value. Finally, in the tertiary creep, the creep rate increases continuously until the fracture, due to the increasing of cavities and cracks [Dép07]. Most of creep models are only describing the secondary creep stage, only a few of them are also including the primary creep.

Creep behavior

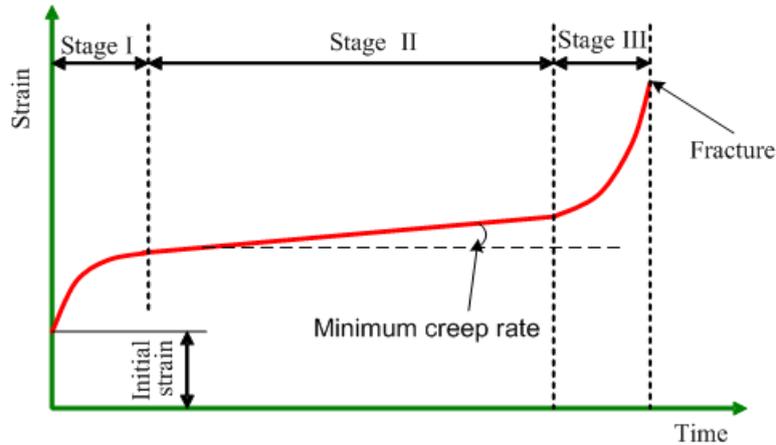


Figure 2.6: Creep curve at a constant stress level

To describe the solder behavior a Garofalo model which defines the secondary creep rate as a function of stress and temperature with a hyperbolic sine was chosen:

$$\dot{\epsilon}_{cr} = A[\sinh(B \cdot \sigma)]e^{-Q_c/RT} \quad \text{Eq. 2.1}$$

Where $\dot{\epsilon}_{cr}$ is the steady-state creep rate, Q_c is the activation energy for the creep in J/mol, R the universal gas constant (8,14 J/mol.K), T the temperature in K, σ the stress in MPa, and A and B are constants from experiment.

The SAC solder alloy was characterized by [Schu03], as follow:

$$\dot{\epsilon}_{cr} = C_1[\sinh(C_2 \cdot \sigma)]^{C_3}e^{C_4/T} \quad \text{Eq. 2.2}$$

Where C_1 through C_4 are constants defined as follow:

Constant C1 (1/s)	Constant C2 (1/MPa)	Constant C3 (-)	Constant C4 (K)
277984	0,02447	6,41	6500

Table 2.3: Table of values for the constants of the Garofalo creep law for the SAC solder alloy

2.3.3 The silicon chip

Si is a brittle material and has therefore a high elasticity modulus and is obviously modeled with a linear elastic model.

Density (kg/m ³)	Specific Heat (J/kgK)	Heat Conductivity (W/mK)	Young's Modulus (MPa)	Poisson's ratio	CTE (ppm/K)
2330	770	120	168000	0,278	2,8

Table 2.4: Table of thermo-mechanical properties of the Si

2.3.4 The aluminum metallization

The chip metallization is made of an AlCu alloys with an Cu weight percentage ranging from 0,1% to 1%. In a first approach, simulations were performed with a material model for Al with a plasticity model independent from temperature. But this model was not precise enough to be able to correctly simulate the plastic deformations of the metallization. So a literature study on material properties of Al alloys was conducted. 28 publications were reviewed [Alprop]. In those publications, the mechanical properties of different Al alloys with an Al weight percentage of about 99% (Al, AlSi, AlSiCu, AlCu) in the form of a thin film deposited on a Si substrate were investigated. The material properties were dependent on the film thickness. A thin film effect induces that thinner layers, are stronger. Our layer is 5 μm thick, but the data collected referred mainly to layers of about 1 μm . The yield stress in function of the layer's thickness was plotted Figure 2.7 for all the literature's data: yield stress values for an Al film of 1 μm thick are widespread, ranging from 20 MPa to 470 MPa. This diversity of results can be explained by the fact that the alloys studied did not always had the same composition, and the methods used to measure stress may also differ from one paper to another. For a layer thicker than 1 μm , the yield stress ranges between 50 MPa to 150 MPa. Stress-strain curves from literature were also analyzed and converted into a bilinear kinematic hardening model. Those models obtained for room temperature were compared with each other

Figure 2.8. Again, one can see that yield stresses range from 20 MPa to 470 MPa but also with different Young's modulus and tangent modulus. Finally the temperature dependence of yield stress was investigated (Figure 2.9). The dependence was mainly studied for temperature ranging from 20°C to 150°C. Only a few studies looked at the mechanical behavior at negative temperatures. Here, the yield stress ranges from 50 MPa to 230 MPa, but the slopes of the different curves are often comparable.

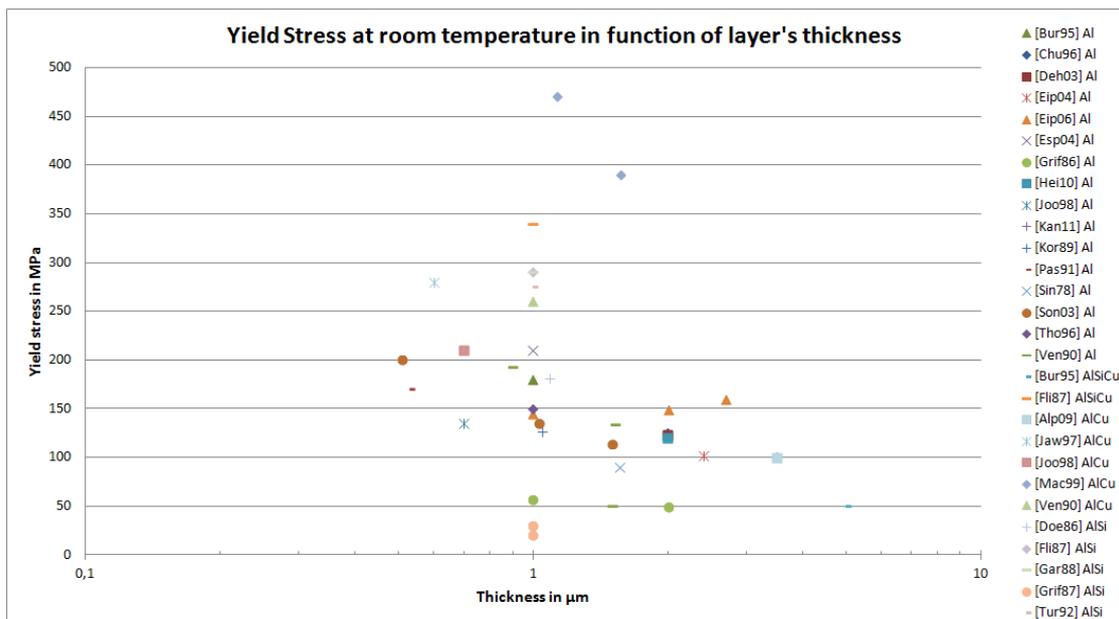


Figure 2.7: Yield stress versus layer's thickness at room temperature of literature's data

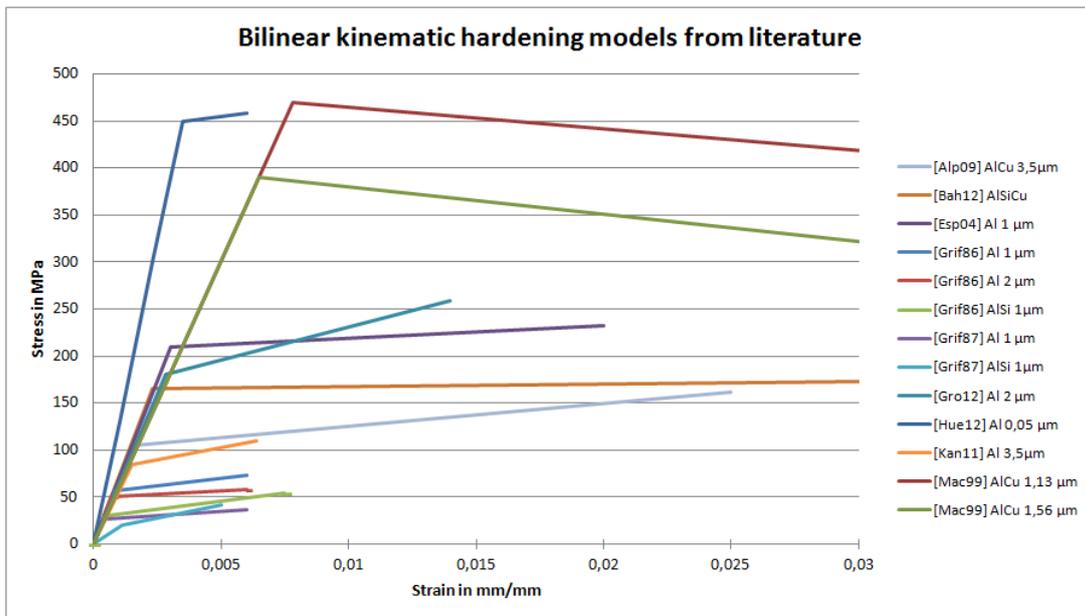


Figure 2.8: Bilinear kinematic models of literature's data

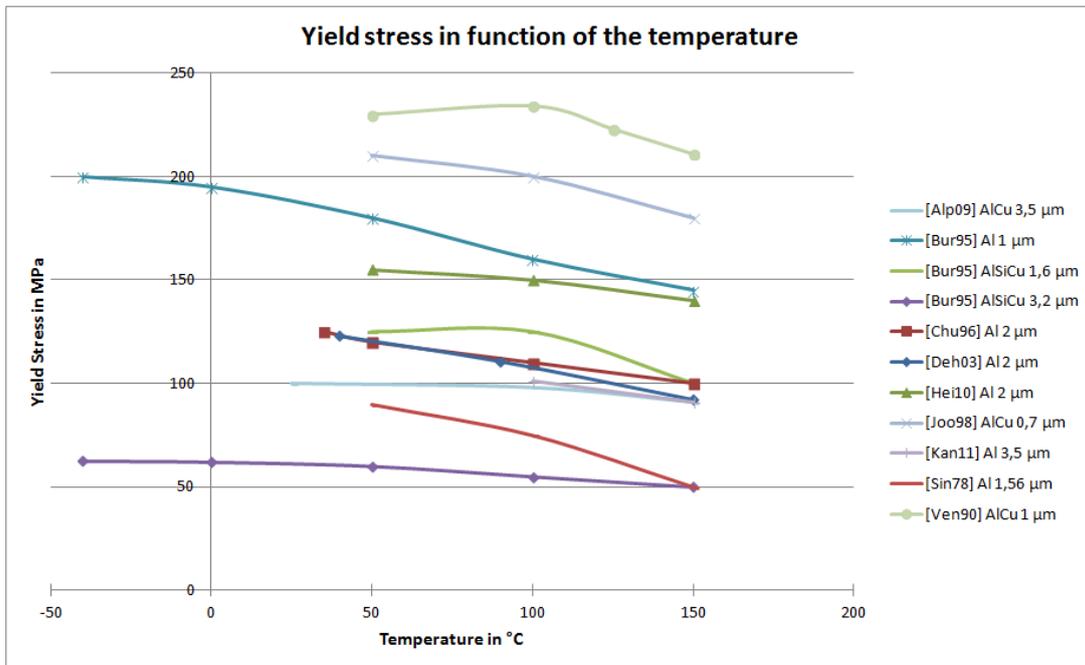


Figure 2.9: Yield stress versus temperature of literature's data

Finally, as a too high value of yield stress does not allow plastic deformations to occur, and because the yield stress of an Al layer thicker than 1 μm ranges between 50 MPa to 150 MPa, a yield stress in the vicinity of 100 MPa was chosen for room temperature. This corresponds to the model used by [Kan13]. This model also included the temperature dependence of the yield stress.

Density (kg/m ³)	Temperature (°C)	Specific Heat (J/kgK)	Heat Conductivity (W/mK)	Young's Modulus (MPa)	Poisson's ratio	CTE (ppm/K)
2700	from -63°C to 200°C	855 - 940	236	68600 - 61000	0,3	21,1 - 26,5

Table 2.5: Table of thermo-mechanical properties of the AlCu metallization

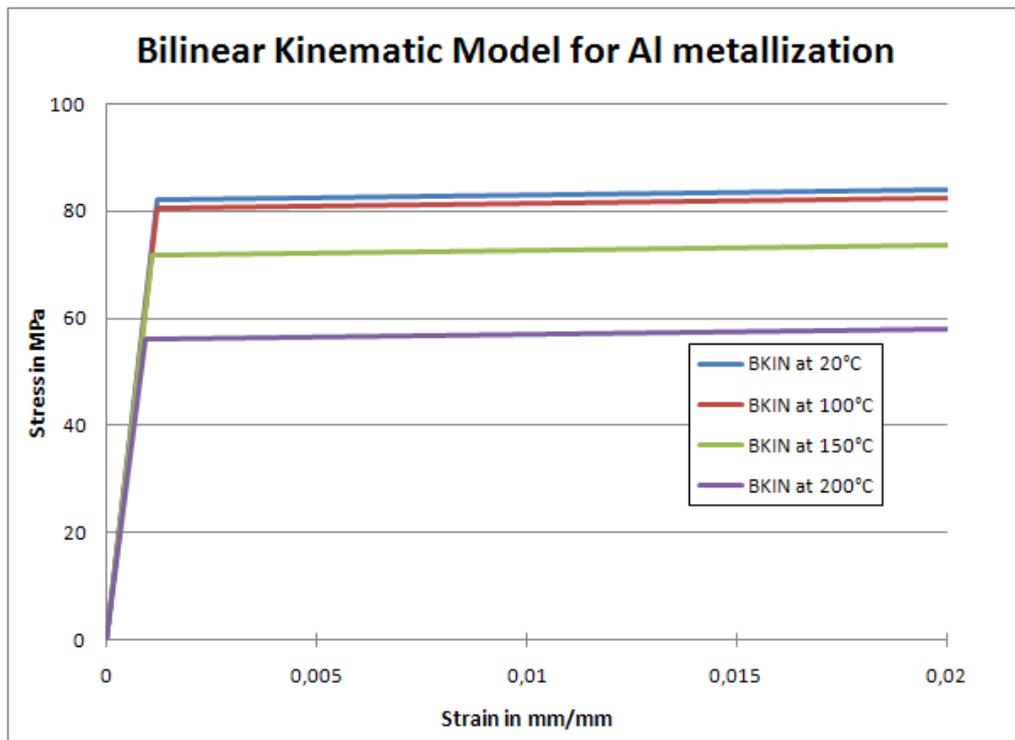


Figure 2.10: Bilinear kinematic hardening temperature dependent model for the AlCu metallization

2.3.5 The intermetallics (IMC)

To determine the material properties of intermetallics (IMC) a literature study was required [Fie91, Fre94, Gro12, Häs06, Jia97, Lee07, Tsa06]. Here the IMC were chosen to correspond to Cu_6Sn_5 . IMC are brittle materials; they have then a linear elastic model.

Density (kg/m ³)	Temperature (°C)	Specific Heat (J/kgK)	Heat Conductivity (W/mK)	Young's Modulus (MPa)	Poisson's ratio	CTE (ppm/K)
8280	from 25°C to 175°C	286	34,1	100000	0,309	18 - 20,2

Table 2.6: Table of thermo-mechanical properties of the intermetallics(IMC)

2.3.6 The molding compound

The commercially available epoxy-based molding compound is a polymer, and has thus a viscoelastic behavior, meaning that the mold exhibits both viscous and elastic characteristics when undergoing deformation. Upon application of a load, the elastic deformation is instantaneous while the viscous part occurs over time. Viscoelastic deformations are then depending on load, time and temperature.

Density (kg/m ³)	Temperature (°C)	Specific Heat (J/kgK)	Heat Conductivity (W/mK)	Young's Modulus (MPa)	Poisson's ratio	CTE (ppm/K)
1987	from -60°C to 260°C	987	1	14900	0,35 - 0,45	12 - 31

Table 2.7: Table of thermo-mechanical properties of the molding compound

The material is restricted to be ThermoRheologically Simple (TRS), which implies that the material response to a load at a high temperature over a short duration is identical to that at a lower temperature but over a longer duration. Thus, the time-temperature superposition principle can be used to determine the temperature-dependent mechanical properties of mold from known properties at a reference temperature. Indeed, the elastic moduli of typical amorphous polymers increase with loading rate but decrease when the temperature is

increased. Fortunately, curves of the instantaneous modulus as a function of time do not change shape as temperature is changed but appear only to shift left or right. This implies that a master curve at a given temperature can be used as the reference to predict curves at various temperatures by applying a shift operation [Ima08]. Here, the master curve was implemented through the use of Prony series (

Figure 2.11) and the shift operation was defined with the Williams-Landel-Ferry (WLF) shift function (Figure 2.12). In the Prony series, the shear modulus is defined as follow:

$$G(t) = G_{\infty} + \sum_{i=1}^N G_i e^{-t/\tau_i} \quad \text{Eq. 2.3}$$

Where $G(t)$ is the shear modulus at time t , G_{∞} is the long term modulus once the material is totally relaxed, and τ_i are the relaxation times.

The WLF shift function is an empirical equation:

$$\log(a_T) = \frac{-C_1(T - T_r)}{C_2 + (T - T_r)} \quad \text{Eq. 2.4}$$

Where T is the temperature, T_r is a reference temperature chosen to construct the master curve, and C_1 and C_2 are empirical constants adjusted to fit the values of the superposition parameter a_T .

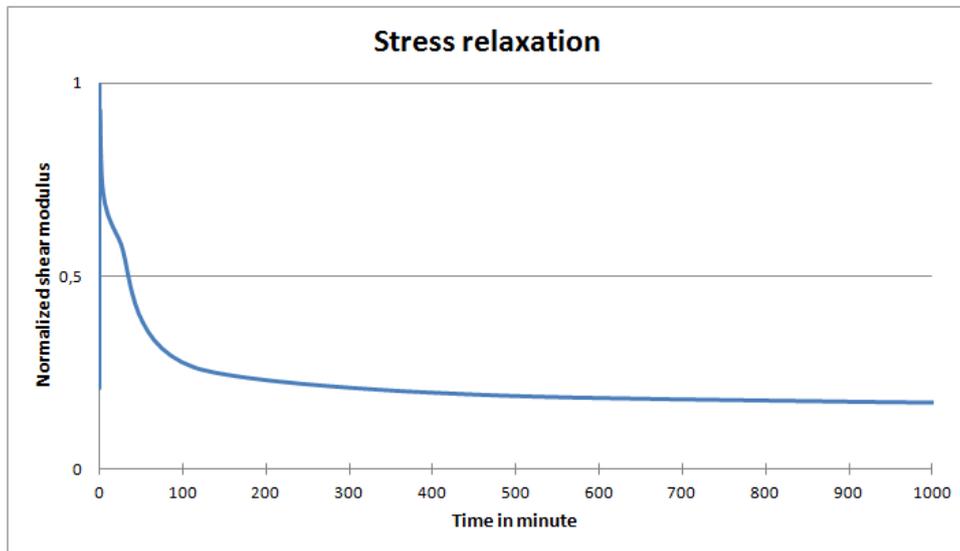


Figure 2.11: Master curve for stress relaxation of the molding compound

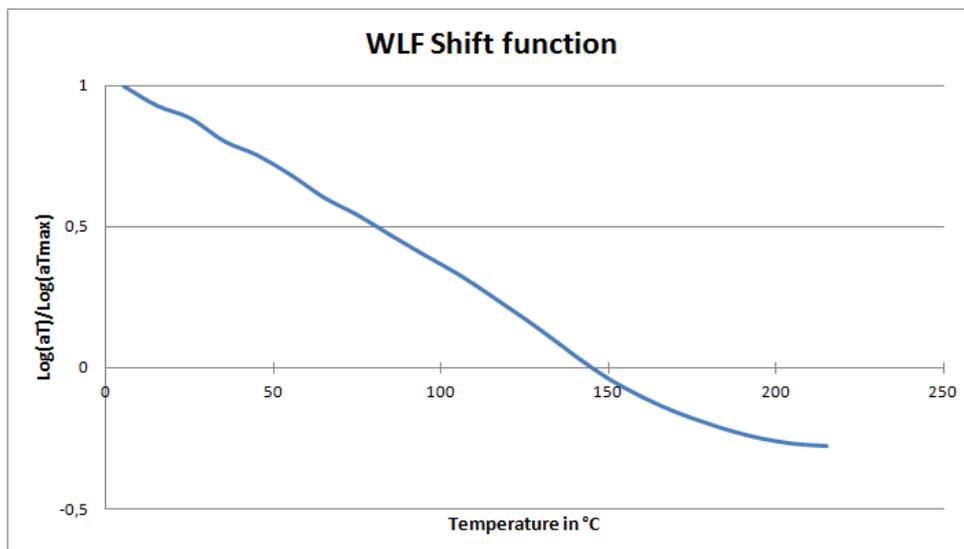


Figure 2.12: Shift function of the molding compound

3 Thermal pre-study

Before to be able to test the B6 Bridge under APC, the specific thermal behavior of the module has to be known and understood. That is why a thermal study was performed and the thermal impedance of the module was characterized. Based on this thermal study, the Design of Experiment for APC tests was defined.

3.1 Measurement and simulation of thermal impedance

3.1.1 Definition and application of the thermal impedance

The thermal impedance Z_{th} is the evolution of the temperature difference across a structure in function of the time for determined power dissipation P_v . The thermal impedance reflects then the transient thermal behavior of power modules. It is often given as a difference between the junction temperature and a reference temperature T_{ref} (case, or heat-sink temperature).

$$Z_{th} = \frac{T_j - T_{ref}}{P_v} \tag{Eq. 3.1}$$

This function is defined by means of a step response (Figure 3.1). The power device is exposed to an active power pulse P_v generated with load current. After the steady state is reached, the load current is switched off and the cooling behavior is measured until the junction temperature is equal to the reference temperature [Hen11]. The temperature rise is measured on the device by electrical means through the on-state voltage (V_{ce} for an IGBT, V_{DS} for a MOSFET) which is a Temperature Sensitive Parameter (TSP). The TSP is turned into temperature via a sensitivity factor K , which is a characteristic of the device.

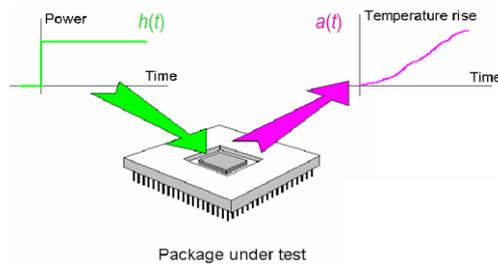


Figure 3.1: Schematic of a measurement setup of thermal transient behavior [Men00]

The heat flow can be modeled by analogy to an electrical circuit (Figure 3.2) where heat flow is represented by current, temperatures are represented by voltages, heat sources by constant current sources, thermal resistances by Resistors (R) and thermal capacitances by Capacitors (C) (Table 3.1). In most cases few RC elements are sufficient to describe the thermal system properly.

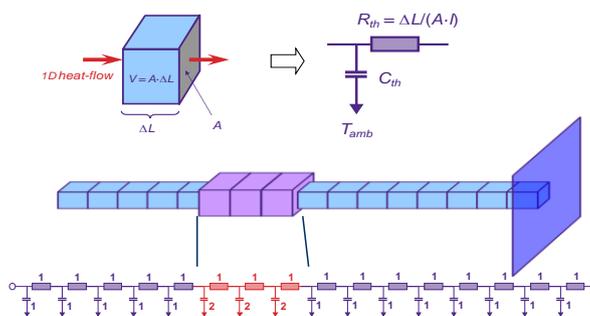


Figure 3.2: Example of a thermal RC model

Electric	Thermal
Electric current (SI unit Ampere)	Heat flow
$I = \text{Joule} \cdot \text{area}; [\text{m}^2]$	$\dot{Q} = \frac{dQ}{dt} = \text{Watt} = \frac{\text{Joule}}{\text{t}}; \left[\frac{\text{J}}{\text{s}}\right]$
Current density	Thermal flow
$J = \frac{\text{Current}}{\text{Area}}; \left[\frac{\text{A}}{\text{m}^2}\right]$	$\dot{q} = \frac{\text{Joule}}{\text{area} \cdot \text{time}} = \frac{\text{W}}{\text{A}}; \left[\frac{\text{J}}{\text{s} \cdot \text{m}^2}\right]$
Resistance	Thermal resistance
$R = \frac{U}{I} = \Omega = \frac{\text{Watt}}{\text{A}^2}; \left[\frac{\text{J}}{\text{s} \cdot \text{A}^2}\right]$	$R_{th} = \frac{\text{height}}{\lambda \cdot \text{area}}; \left[\frac{\text{W}}{\text{m} \cdot \text{K}}\right]$
Electrical capacity	Heat capacity
$C = \frac{Q}{U} = \frac{1C}{1V} = \frac{\text{Ampere} \cdot \text{Second}}{\text{Volt}}; [\text{F}]$	$c = \frac{\Delta Q}{m \cdot \Delta T}$ Specific heat capacity (energy needed to warm up 1kg of material to 1K)
	$C_{th} = c \cdot \rho \cdot V = \frac{\text{J}}{\text{kg} \cdot \text{K}} \cdot \frac{\text{kg}}{\text{m}^3} \cdot \text{m}^3; \left[\frac{\text{J}}{\text{K}}\right]$
Electrical tension	Temperature range
$U = \frac{dW}{dQ} \Rightarrow \int_1^2 \vec{E} \cdot d\vec{s}; [\text{V}]$	$\Delta T = T_2 - T_1$

Table 3.1: Table of electric-thermal analogies [Sci12]

The temperature rise function $a(t)$ is the unit-step response function of the thermal RC network of the measured system and it is a characteristic of the measured package.

The characteristic value for one single RC stage is the magnitude, which is represented by the resistance value, R and the time constant, which is τ . The value $\tau = RC$ is the time it takes the temperature across the component to either rise or diminish within $1/e$ of its final value. So the response function can be given in the form of:

$$a(t) = R \cdot \left[1 - e^{-\frac{t}{\tau}}\right] \quad \text{Eq. 3.2}$$

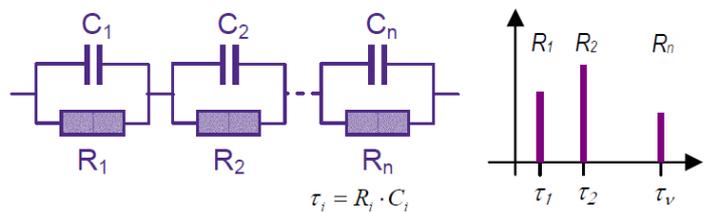


Figure 3.3: Serially linked RC stages and it responses [Men00]

Thus the $a(t)$ unit-step response of the lumped circuit shown in Figure 3.3 is easily calculated by the sum of a few exponential terms:

$$a(t) = \sum_{i=1}^n R_i \cdot \left[1 - e^{-\frac{t}{\tau_i}}\right] \quad \text{Eq. 3.3}$$

If the R_i is substituted by a continuous spectrum, then this summation should be replaced by the integration over all the possible τ range.

$$a(t) = \int_0^{\infty} R(\tau) \cdot \left[1 - e^{-\frac{t}{\tau}}\right] d\tau \quad \text{Eq. 3.4}$$

After switching to logarithmic time scale instead of $a(t)$, $a(z)$ will be used where z is the $\ln(t)$. The $a(z)$ function is either called heating curve or thermal impedance curve. Using the $z=\ln(t)$ transformation for Eq. 3.4 :

$$\frac{d}{d(z)} a(z) = \int_{-\infty}^{\infty} R(\xi) \cdot \left[e^{(z-\xi)-e^{(z-\xi)}}\right] d\xi \quad \text{Eq. 3.5}$$

Where $R(\xi)$ is the time-constant spectrum. It has the form of a convolution integral. Introducing the $w_z = e^{(z-e^z)}$ function:

$$\frac{d}{d(z)} a(z) = \int_{-\infty}^{\infty} R(\xi) \cdot w_z(z - \xi) d\xi \quad \text{Eq. 3.6}$$

$$\frac{d}{d(z)} a(z) = R(z) \otimes w_z(z) \quad \text{Eq. 3.7}$$

From the equation Eq. 3.6 and Eq. 3.7 $R(z)$ can be calculated applying the inverse convolution:

$$R(z) = \left[\frac{d}{d(z)} a(z) \right] \otimes^{-1} w_z(z) \quad \text{Eq. 3.8}$$

This inverse convolution, also called deconvolution can be calculated by numerical iterative approximation steps. Here, the commercial software called Tr3ster-Master is used. This software will be described more in detail in the chapter 4. T3ster-Master uses a Bayes iteration to perform the deconvolution [Rich72].

The $R(z)$ time-constant spectrum gives hints for the time-domain behavior of the system, and can be further processed and turned into a structure function. Indeed, the continuous time-constant can be cut into several discrete peaks, where each peak would refer to one important time constant in the system. From the τ time constant and R thermal resistance values, the corresponding thermal capacitance can be calculated. From the resulting RC pairs, a Foster type impedance model with RCs connected parallel and stages linked together serially can be deduced [Men00] (see Foster model in Figure 3.4). But this Foster model is just theoretical and does not reflect the physical structure of the thermal system. That is why the Foster model should be transformed into a Cauer model, which is a ladder-like model [Men00]. The discrete RC model network in the Cauer canonic form corresponds to the reality but is very difficult to interpret. Hence, the use of a comprehensive graphical representation of the RC network like the cumulative structure function which plot the sum of the thermal capacitances as a function of the sum of thermal resistances (Figure 3.4). This results in a map of the heat conduction path. The steep sections in this function represent the good conducting materials in the package, such as the silicon chip, the copper base, whereas flat section represent bad conduction material like the die attach or the thermal grease [Men00, Sze00].

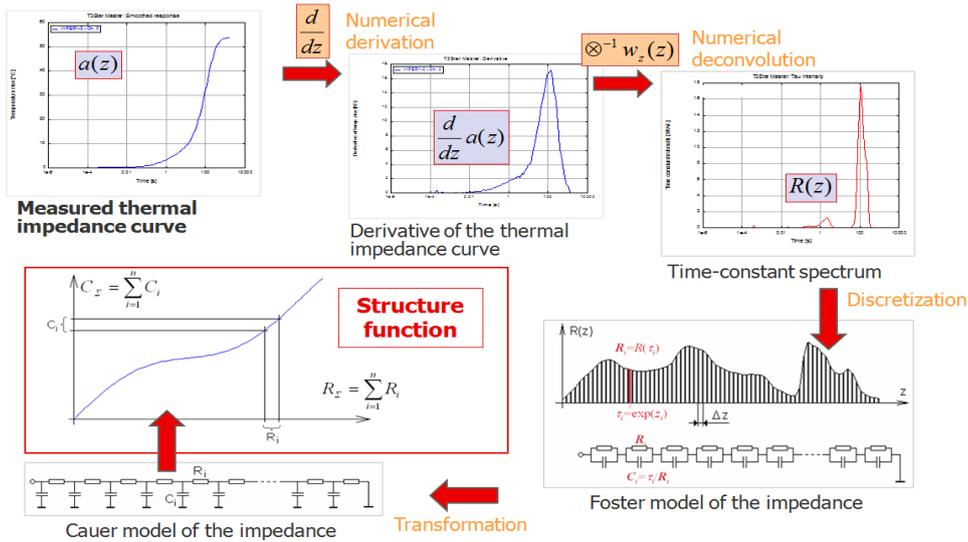


Figure 3.4: Successive steps to convert a measured thermal impedance curve into a cumulative structure function [Men00]

Thus it is possible to identify the layers inside the power module in the cumulative structure function. Moreover, it also allows detecting degradations in layers, for example after some thermal cycling (Figure 3.5). The structure function of a device is determined before to perform any tests. This curve will be the reference structure function. Then, the thermal impedance is measured again after some cycles in order to know the new structure function of the device. If the device has a degraded layer, then the flat section of the concerned layer will be longer reflecting a higher thermal resistance and the entire function will be shifted. The structure function can then be used as a non destructive method to detect failure in power modules. In principle this can also be done with the evaluation of the increase in Z_{th} , but as the Z_{th} is plotted in function of time, the shift between the original and the degraded Z_{th} is more difficult to see and interpret.

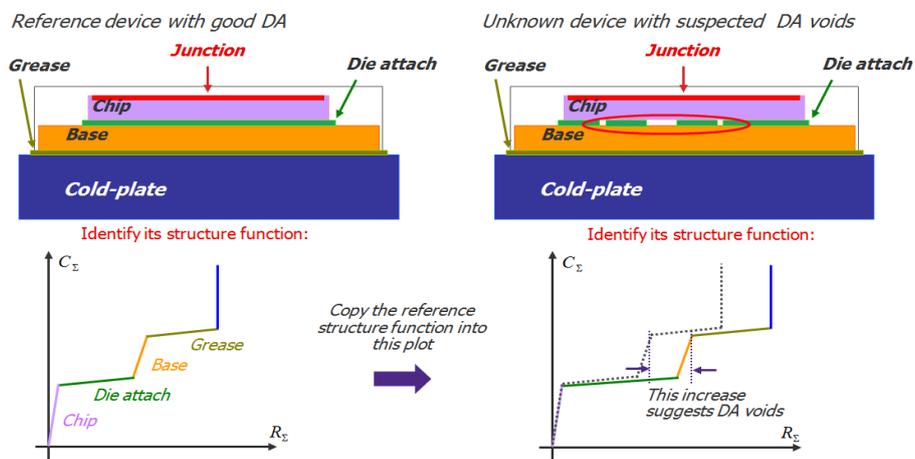


Figure 3.5: Shift in cumulative structure function due to a layer degradation in power module [Men00]

3.1.2 1D thermal simulation

First of all, the different thermal paths of the B6 Bridge were identified. There are three thermal paths. The first one is at the back of the device. The heat is transported from the silicon die to the heat sink through the solder layer, the Cu lead frame and a Thermal Interface Material (TIM), in our case a thermal film. The second one is on the top side of the device. The heat flows from the die to the air through a solder layer, the Cu clip and the mold. The third thermal path removes laterally the heat via the Cu clip to the heat sink.

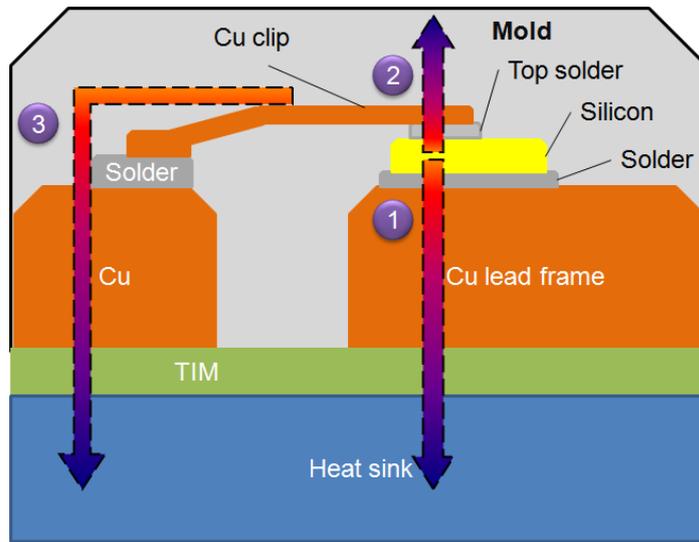


Figure 3.6: Schematic cross-section of the B6 Bridge with its 3 thermal paths [Sci12]

The 3 thermal paths of the module are modeled in a RC thermal circuit (Figure 3.7) where every layer is represented by a resistance R and a capacity C . Thermal circuits representing thermal paths are in parallel. In order to determine the importance of each path in the cooling behavior of the module evaluated via the Z_{th} measurement, the inverse R_{th} is calculated for every isolated path i ($1/R_{th\ path\ i}$). Indeed, the R_{th} of the entire module is defined as follow:

$$R_{th\ B6\ Bridge} = \frac{1}{\frac{1}{R_{th\ path\ 1}} + \frac{1}{R_{th\ path\ 2}} + \frac{1}{R_{th\ path\ 3}}} \quad Eq. 3.9$$

Thus, the thermal path with the highest inverse R_{th} value has the most impact on the cooling behavior of the module. Here, the main thermal path is the one at the back of the device: path 1, as its inverse R_{th} represents 95% of the sum of the inverse R_{th} of all 3 paths. Thus, performing a Z_{th} measurement on the B6 Bridge corresponds mainly to the characterization of its thermal path 1 at its back.

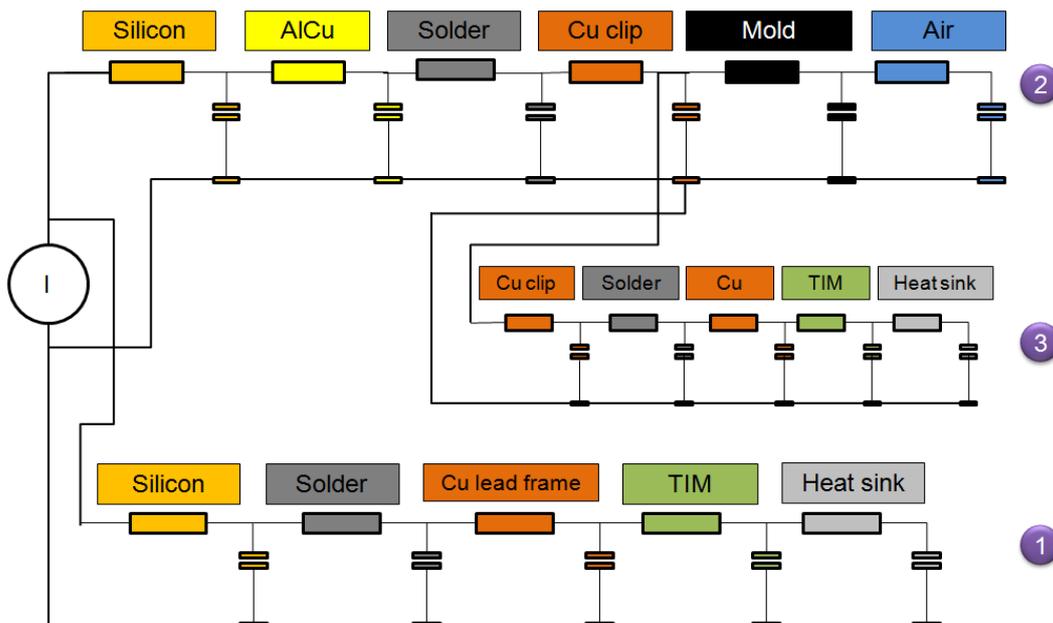


Figure 3.7: RC Cauer model of the 3 thermal paths of the B6 Bridge [Sci12]

The Z_{th} of the B6 was simulated in 1D with the thermal RC model shown Figure 3.7 and compared with a measurement. For the simulation a heat spreading with an angle of 45° was assumed, and only the thermal path at the back of the device was taken into account. The material data and geometry of each material layer were needed in order to determine R_{th} and C_{th} :

$$R_{th} = \frac{h}{A \cdot \lambda} \quad Eq. 3.10$$

Where h is the thickness of the material layer, A its surface, and λ its thermal conductivity.

$$C_{th} = C \cdot \rho \cdot V \quad Eq. 3.11$$

Where C is the specific heat capacity, ρ is its density and V the volume.

These material data were loaded and the thermal circuit modeled in the LT Spice software [Lin11], which calculates and plots the Z_{th} curve of the module. The Z_{th} obtained was then compared with a measurement Figure 3.8. One can see that both curves are overlapping in the first part of the graphic corresponding to the B6 Bridge area. In the second zone of the graphic corresponding to the TIM and heat sink area, curves are separated from each other. This is due to the fact that correctly simulating the heat sink is quite complicated because of the difficulty to model the water flow. Anyway, the matter of interest here is to simulate the B6 Bridge and the result is satisfying as the Z_{th} curve obtained reflects well the measurement.

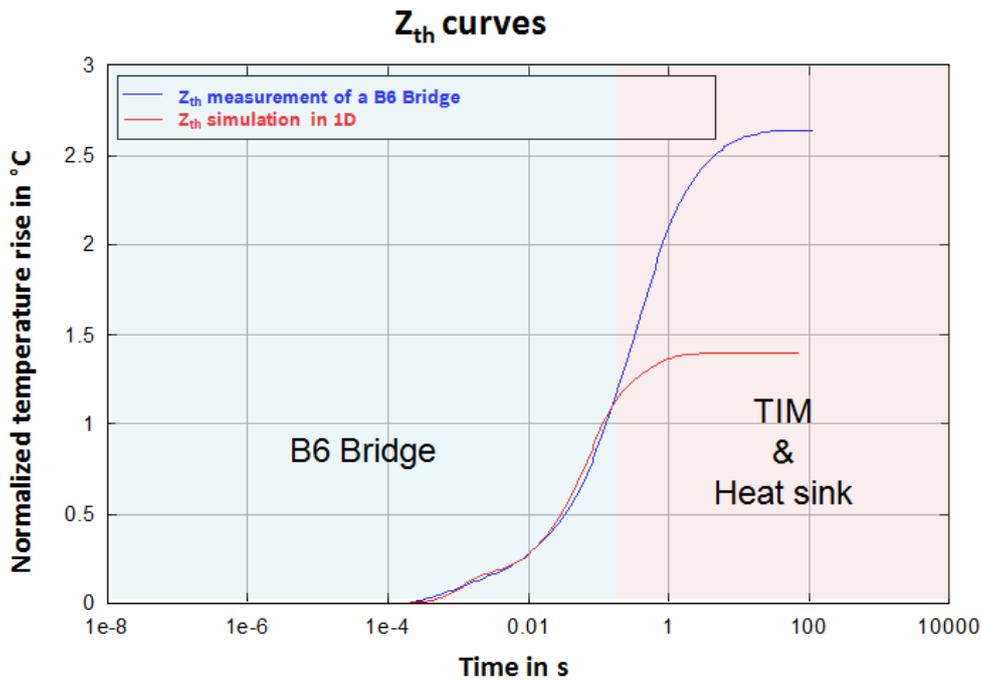


Figure 3.8: Z_{th} curves of the B6 Bridge from measurement and 1D simulation [Sci12]

Then, the simulated Z_{th} curve was turned into a cumulative structure function via the T3ster-Master software, and the different layers of the thermal path were identified. The identification of the layers was done with the help of an analytic cumulative structure function based on the R_{th} and C_{th} values calculated with geometry and material data. Both analytic and simulated structure function are plotted Figure 3.9 with the different layers highlighted.

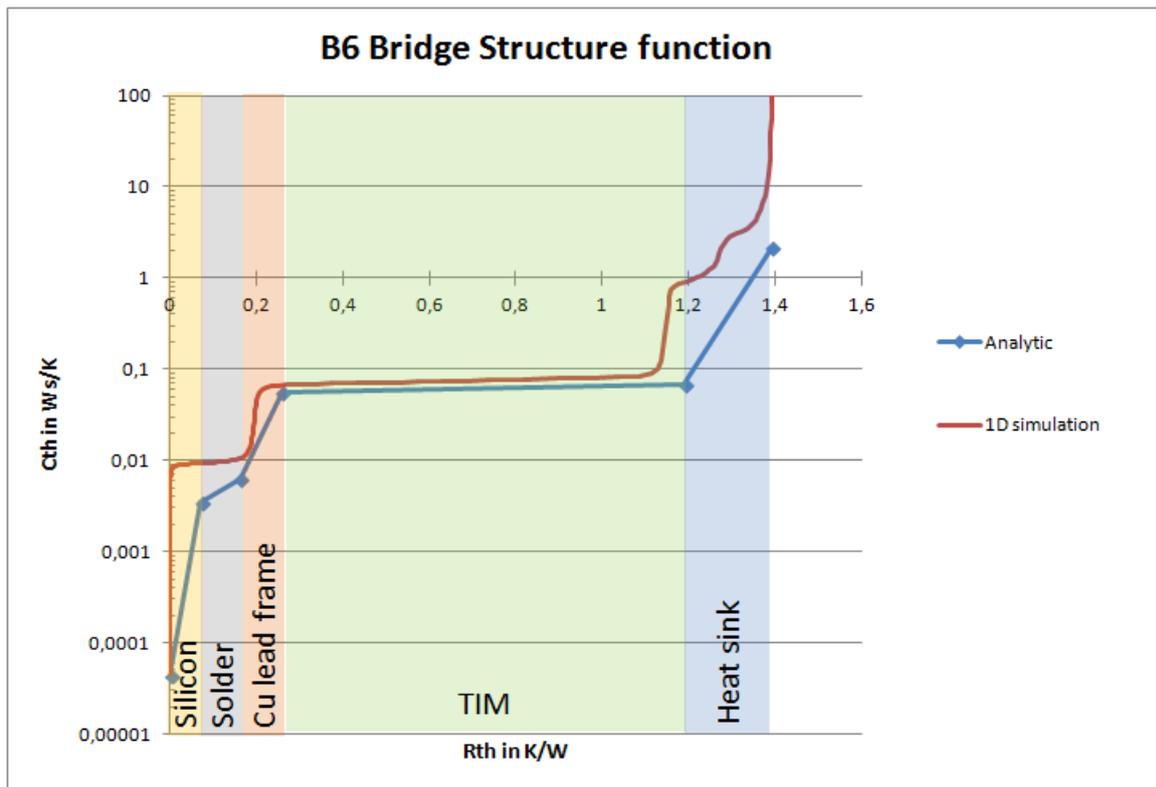


Figure 3.9: Analytic and 1D simulated structure functions of the B6 Bridge [Sci12]

3.1.3 2D FEM thermal simulation

A simulation of the Z_{th} curve of the B6 Bridge was also performed using the FEM software Ansys. A 2D axisymmetric model of only one MOSFET structure, including the TIM and the heat sink, was created. The model is composed of 44 775 thermal plane elements with 8 nodes (PLANE77). More details about the model and its mesh will be given in the chapter 5.

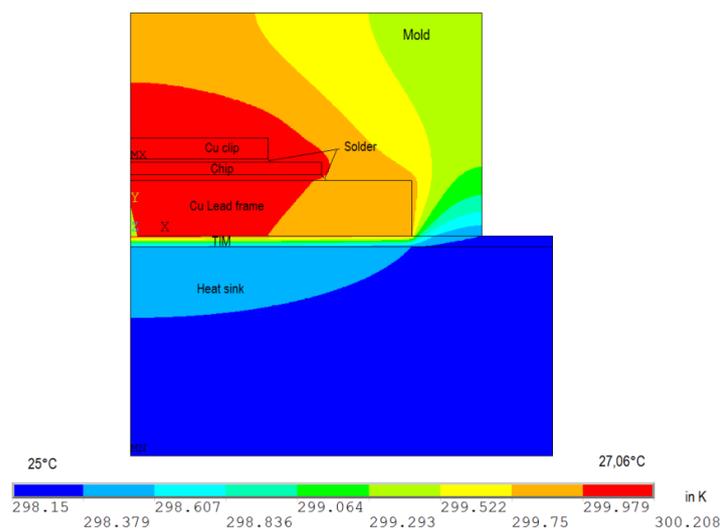


Figure 3.10: Temperature distribution in the MOSFET structure after 10s of heat generation

The loading conditions defined in the simulation are mimicking a Z_{th} measurement. First the thermal properties of materials were loaded. Then the boundary conditions were defined so that the mold was in the air, subjected to free convection and radiation ($10W/m^2K$), and the bottom line of the heat sink has a constant temperature of $25^{\circ}C$. Finally an internal heat generation of $1W$ was created in the active zone of the chip, for 100s. The resulting temperature distribution in the model after 10s of heat generation is shown Figure 3.10.

The Z_{th} is obtained by calculating the temperature rise at the p-n junction of the chip and compared to a measurement (Figure 3.11).

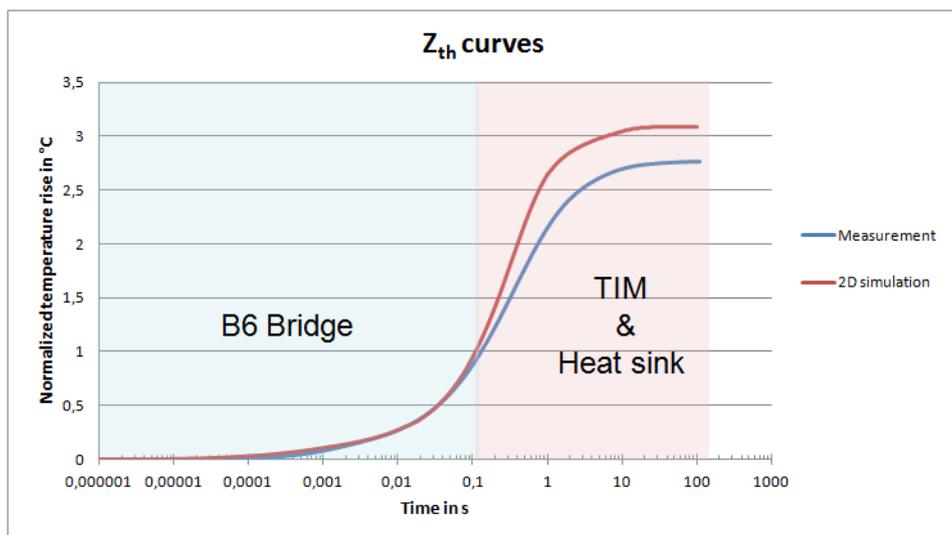


Figure 3.11: Z_{th} curve of a MOSFET structure from a measurement and 2D simulation

Once again, measurement's and simulation's curves are overlapping in the module area, but are diverging in the TIM and heat sink area due to the difficulty to model the heat sink and its water flow. But the measurement's and the 2D simulation's results are very similar concerning the module itself, thus the 2D thermal model is validated. The Z_{th} curve was converted into a cumulative structure function and was compared with structure functions from several measurements, and from the analytic and 1D simulation of the B6 Bridge (Figure 3.12). All structure functions are in the same range, except the one from the 1D simulation that take into account all the 3 thermal paths, which reached higher C_{th} values. So both the 2D and the 1D simulation with only one thermal path are in good agreement with measurements.

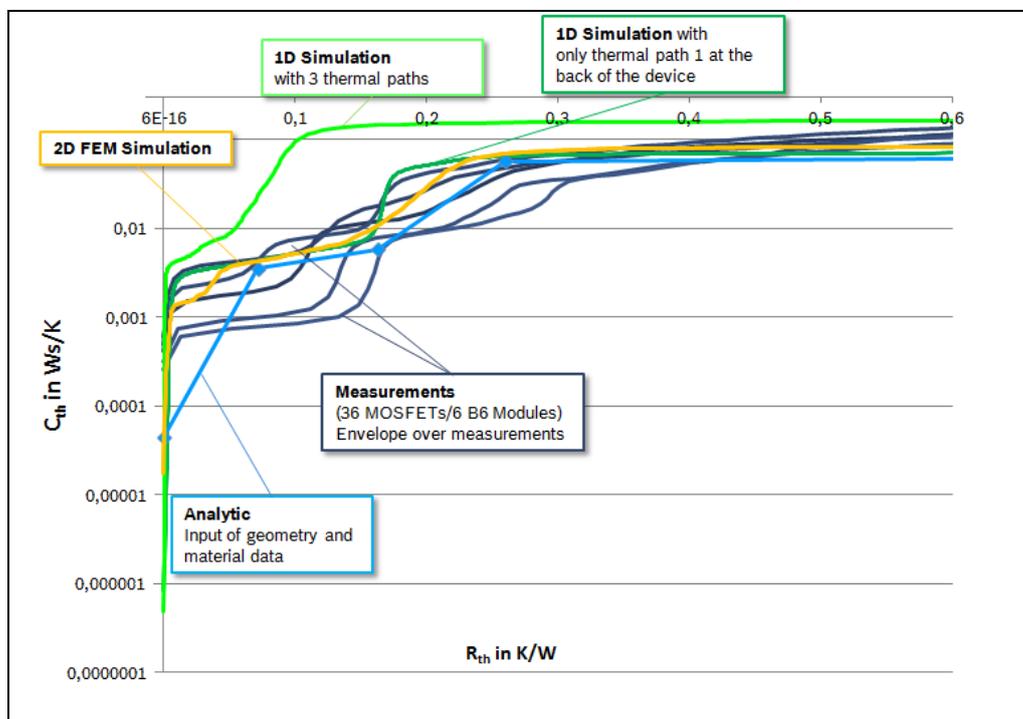


Figure 3.12: Comparison of different cumulative structure functions of the B6 Bridge

3.2 Detailed thermal study of the module

Once the 2D FEM model validated, a detailed thermal study was performed in order to gain insight about the thermal behavior of each layer of the module. The Z_{th} of each layer was simulated and is shown Figure 3.13. It is remarkable that the Z_{th} of the chip, the Al metallization, the IMC, the top solder and the Cu clip are coincident. This means that all these layers close to the chip, are following simultaneously the same temperature changes as the chip itself. The bottom solder layer has a temperature a bit lower than the chip one, but their Z_{th} curves are following the same trend. This is also the case for the Cu lead frame with a temperature even lower than the one of the bottom solder. The major difference is observed for the mold, which needs much more time than the other layers to be warmed up. Nevertheless the stationary stand is reached for all layers after 10s.

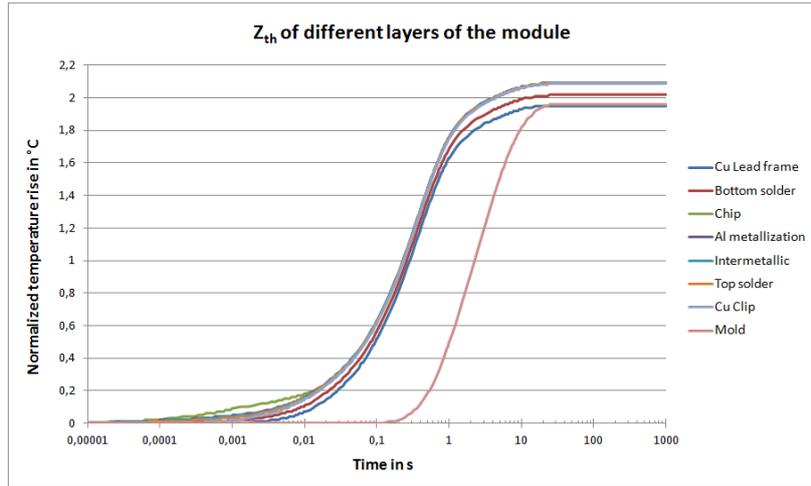


Figure 3.13: Z_{th} curves of the different layers of the module

Then a vertical path was defined at the center of the model, on the symmetry axis, and the evolution of the temperature was plotted for the time $t=10s$ (Figure 3.14). As already seen with the Z_{th} curves, the Cu clip, the top solder, the Al metallization and the IMCs have the same temperature. Inside the chip, there is a temperature gradient, as only a part of it generates heat. But the larger temperature gradient occurs in the mold, as it is making the connection between the Cu clip which has the highest temperature of the model and the cold air of the environment. One can also notice that the mold is a bit colder than the Cu lead frame even though this latter one is in contact with the heat sink. This shows again, that the mold needs more time to warm up than the other layers of the module.

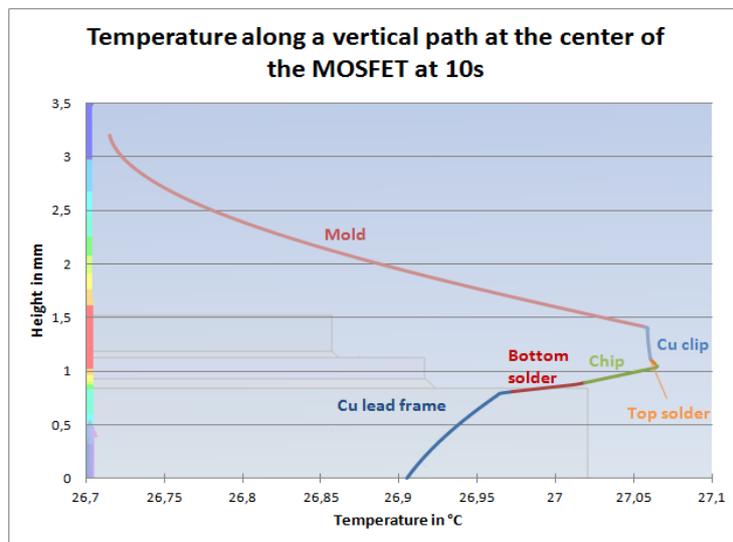


Figure 3.14: Evolution of the temperature along the vertical path at the center of the model at $t=10s$

Finally, the temperature rises of the different layers are compared at two different times on histograms representing the percentage of the chip temperature that is reached (Figure 3.15). At already $t=0,2s$, the Al metallization, the IMC and the top solder have the same temperature as the chip. The Cu clip and the bottom solder are respectively at 98% and 94% of the chip's temperature. The Cu lead frame in direct contact with the heat sink has reached only 88% of the chip's temperature. The mold can reach only 5% of the chip's temperature within 0,2s. After 100s, the Cu clip has also reached the same temperature as the chip. The temperature of the bottom solder and the Cu lead frame are now closer to the chip one. The biggest temperature rise occurs in the mold, as it has 94% of the chip's temperature. So the temperature of the mold increased of about 90% in 100s. This shows again the slower warm up process in the molding compound.

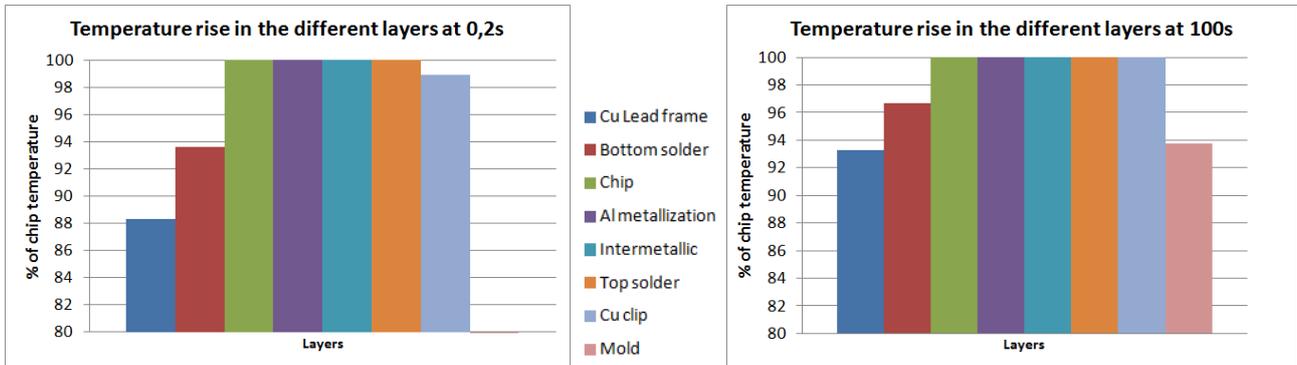


Figure 3.15: Temperature rise in the different layers at 0,2s and 100s

3.3 Definition of the Design of Experiment

Based on the application's requirements of the B6 Bridge and the information gathered on its thermal behavior, a full factorial Design of Experiment (DoE) can be defined for APC tests and simulations. The 3 parameters of APC that are going to vary are: the heat sink temperature T_c which is assumed to correspond to the minimum junction temperature T_{jmin} in our case, the temperature swing ΔT_j and the power-on-time t_{on} . In the literature, APC test parameters are typically ranging:

- Heat sink temperature: $T_c (= T_{jmin})$: from 20°C to 90°C
- Temperature swing: ΔT_j : from 60K to 130K
- Power-on-time: t_{on} : from 0,2s to 60s

Then concerning the application's requirements, the chip is limited to work with a maximum temperature T_{jmax} of 175°C. So this temperature should not be exceeded in our tests. Under application, the temperature swing ranges from 10K to 70K. The heat sink temperature represents the ambient temperature of the environment in which the module is located. As the module is used in a car, it can roughly be assumed that the ambient temperature can vary from -20°C corresponding to a cold outside temperature to 90°C the hottest temperature of the motor. Furthermore, it is known that important power-on-time for servo-steering applications are $t_{on} = 0,2s, 0,5s$ and 2s. Additionally it was learned via simulations that the stationary state of the module is reached after 10s of power-on-time. Based on all this information, the variations of the 3 parameters were defined. For the heat sink temperature, it was decided to have 3 equidistant temperature points, including one extreme negative temperature, one temperature close to the room temperature and one hot temperature. These 3 temperatures are thus chosen to determine if extreme negative or high temperatures are leading to the same failure mechanisms than the ones occurring at moderate temperatures, or if it is on the contrary accelerating degradations. So the 3 heat sink temperatures were chosen to be equal to: -40°C, 10°C and 60°C. Then, 3 different temperature swings were chosen. In the literature some tests were performed with $\Delta T_j = 30K$ or 40K, but devices did not fail even after several millions of cycles. Such temperature swings would not be appropriate for the DoE as performing such tests would be too much time consuming. Nevertheless, one value of temperature swing had to stay in the range of field load. Thus, the lowest value of temperature swing is chosen to be $\Delta T_j = 60K$. The 2 other values $\Delta T_j = 90K$ and 120K are not corresponding to field load anymore, and are then accelerating degradation processes. The highest value is limited to 120K, as with a heat sink temperature of 60°C and 120K temperature swing, the T_{jmax} limit of 175°C is already reached.

Finally, the 3 important values of power-on-time for servo-steering applications $t_{on} = 0,2s, 0,5s$ and $2s$, as well as the time needed to reach the stationary state $t_{on} = 10s$, were taken into account in the sensitivity study. The complete DoE is shown Table 1.1 and the power-off-time t_{off} is set to $10s$ to reach the stationary state.

case n°	T_{jmin}	ΔT_j	t_{on}
	°C	K	s
case 1	-40	60	0,2
case 2			0,5
case 3			2
case 4			10
case 5		90	0,2
case 6			0,5
case 7			2
case 8			10
case 9		120	0,2
case 10			0,5
case 11			2
case 12			10
case 13	10	60	0,2
case 14			0,5
case 15			2
case 16			10
case 17		90	0,2
case 18			0,5
case 19			2
case 20			10
case 21		120	0,2
case 22			0,5
case 23			2
case 24			10
case 25	60	60	0,2
case 26			0,5
case 27			2
case 28			10
case 29		90	0,2
case 30			0,5
case 31			2
case 32			10
case 33		120	0,2
case 34			0,5
case 35			2
case 36			10

Table 3.2: Table summarizing the Design of Experiment for APC tests and simulations

4 Active Power Cycling (APC) Tests

PTC tests are very often performed to characterize the reliability of electronic components. This type of test is quite simple to perform and the thermo-mechanical failure mechanisms induced were already extensively studied and are quite well understood. PTC consists usually in moving cyclically a device from a cold air chamber with a temperature that ranges from -55°C to -40°C to a hot air chamber with a temperature that ranges from 100°C to 250°C . The dwell times are quite long ranging from 15 min to 2 hours and with ramping time of $6^{\circ}\text{C}/\text{min}$ to $40^{\circ}\text{C}/\text{min}$. Thus in those tests, the temperature variation is coming from the environment and the temperature in the device is quasi-homogeneous. Power modules for automotive industry are expected to live 10 000 to 15 000 cycles under a field load that ranges from -10°C to 110°C . Thus a lifetime ranging from 1500 to 2000 cycles is required for modules under accelerated cycling tests with a temperature varying from -40°C to 150°C . The principal degradation induced by PTC is solder fatigue which lead to the apparition of cracks and delamination at solder joints and to the growth of IMC phases. As failure mechanisms induced during PTC are well understood, PTC test can be taken as a reference to which APC can be compared to.

4.1 Experimental method

4.1.1 Active Power Cycling (APC) tests

Our APC test bench is equipped with 5 current sources, 5 switching boxes and 3 heat sinks and the test parameters are controlled and monitored via a computer (Figure 4.1). Thus 5 devices can be cycled simultaneously. Devices Under Test (DUT) are mounted onto a liquid-cooled heat sink through the intermediary of a thermal film used as a Thermal Interface Material (TIM). Depending on the cooling temperature desired, the heat sink liquid consists either in glycol for temperature ranging from -30°C to 80°C or in silicon oil for temperature ranging from -50°C to 200°C . Two thermostats with glycol and one with silicon oil were available for tests, thus the thermostat with silicon oil was used only for tests requiring either negative or really high cooling temperature. Generally only one MOSFET of the 6 contained in the package was electrically loaded. The load current is conducted by the body diode of the power MOSFET and the power losses heat up the package. When the maximum target temperature within the diode is reached, the load current is switched off and the system cools down to a minimum temperature. The end of cycle is achieved when the minimal temperature is reached. The next cycle begins by starting the load current again. The current intensity as well as the duration of heating and cooling phase are determined at the beginning of the test and remain constant during the test. The test strategy used here consists in submitting the device to a loading current corresponding to a desired temperature swing ΔT_j and then to repeat the cycle with constant pulse width t_{on} and t_{off} . So the temperature swing is defined at the start, but may vary with ageing effects of the device. This strategy refers to the one called “ $t_{\text{on}}, t_{\text{off}} = \text{constant}$ ” and is the most severe method but the closest one to application (cf. chapter 1).



Figure 4.1: From the left to the right: a current source (200A), 2 devices under test mounted on the heat sink and connected to switching boxes, and both glycol and silicon oil thermostats.

During APC, the forward voltage V_f of the body diode and the junction's temperature swing ΔT_j are monitored as they are good indicators of modules health (Figure 4.3). Indeed, both parameters are likely to increase with ageing effects. T_j is measured via V_f which is a Thermo-Sensitive Parameter (TSP): a measuring current of 10 mA flows through the diode, the V_f is measured and converted into the corresponding T_j through the relation existing between both parameter $V_f = f(T_j)$ shown on Figure 4.2.

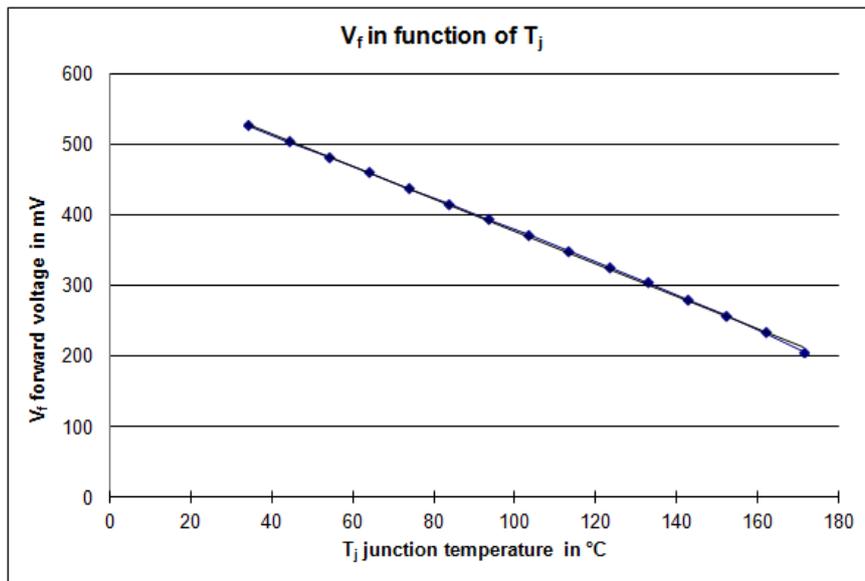


Figure 4.2: Relation between the forward voltage V_f and the junction temperature T_j

The thermal impedance Z_{th} was not measured during APC test, but was deduced from V_f and ΔT_j using the formula:

$$Z_{th} = \frac{\Delta T_j}{P_v} = \frac{\Delta T_j}{I \cdot V_f} \quad \text{Eq. 4.1}$$

Where P_v is the power and I is a constant current.

No fixed End-of-Life (EoL) criterion was defined, as more knowledge is required on the fatigue resistance of the new designed module. Determine an adequate EoL criterion for this kind of module is actually one of the goals of this study. Thus tests were stopped arbitrarily when the increase in forward voltage V_f or in temperature swing ΔT_j was judged high enough (Figure 4.3).

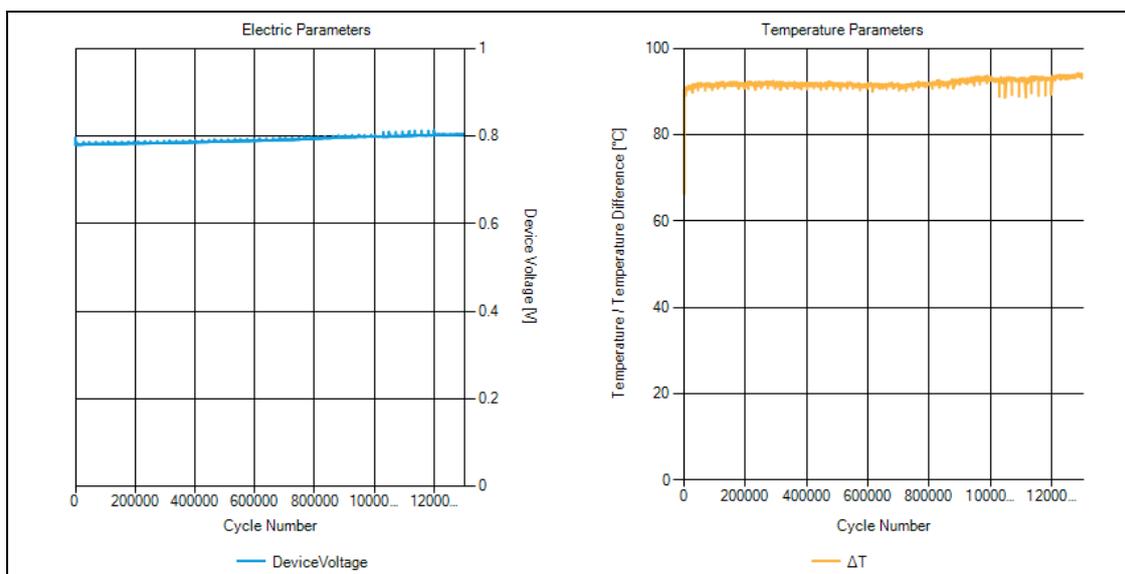


Figure 4.3: Online monitoring of the forward voltage V_f and the junction temperature swing ΔT_j

4.1.2 Failure detection methods

4.1.2.1 Electrical and thermal measurements

Before starting the test and at the end of it, power modules are electrically and thermally characterized by measuring the out and transfer characteristics, the leakage currents, the resistance R_{DSon} and the thermal impedance Z_{th} . The goal is to evaluate the healthiness of modules after cycling.

4.1.2.1.1 Electrical measurements

Out and transfer characteristics, leakage currents, as well as the R_{DSon} are measured by the Keysight Technologies, Inc. B1505A Power Device Analyzer and Curve Tracer (Figure 4.4). It is a single box apparatus which can accurately evaluate and characterize all types of power devices. It has a fast pulsing capacity (10 μ s) and a $\mu\Omega$ level R_{DSon} measurement resolution and sub-pA level current measurement capability [Key14].

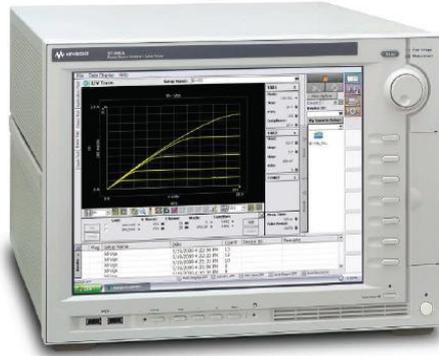


Figure 4.4: The Keysight Technology Inc. B1505A Power Device Analyzer and Curve Tracer[Key14]

The out characteristic of the MOSFET is recorded. It consists in measuring and plotting the drain to source current I_{DS} versus the drain to source voltage V_{DS} for different gate to source voltage V_{GS} . Curves obtained are characterizing the linear region also known as ohmic mode (Figure 4.5).

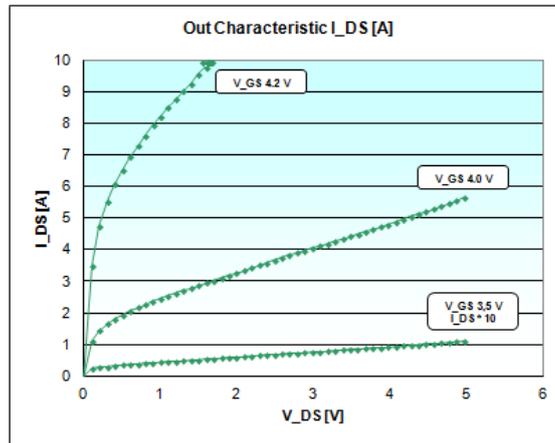


Figure 4.5: Out characteristic of one MOSFET for different values of V_{GS}

The transfer characteristics of the MOSFET at low and high current V_{DS} were recorded as well (Figure 4.6). Here, I_{DS} was measured and plotted versus V_{GS} at low and high I_{DS} . This allows verifying that the switching operation occurs correctly and thus that the MOSFET is still electrically functional. A damage of a single cell in the MOSFET would lead to an increase in I_{DS} at low V_{GS} . This leakage current would be in the range of $10e^{-6}$ A.

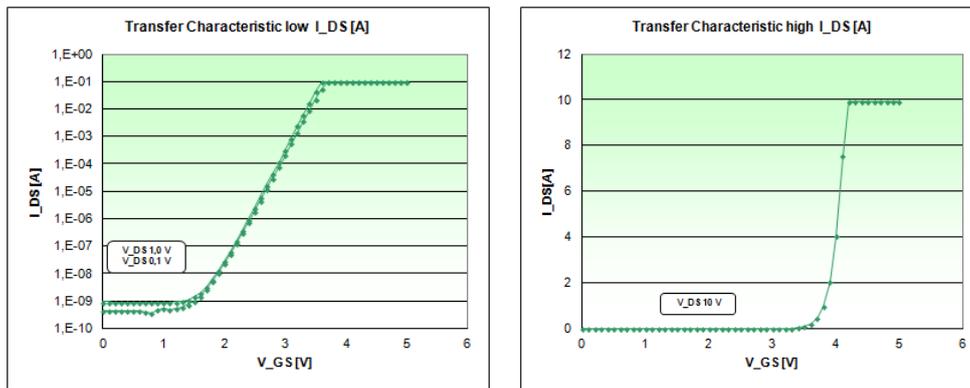


Figure 4.6: Low and high transfer characteristics of one MOSFET

Semiconductors conduct a small amount of current even when they are turned off, it is refer to as leakage current. This leakage is a quantum phenomenon where electrons tunnel through an insulating region. Other than tunneling via the gate insulator or junctions, carriers can also leak between source and drain terminals of a MOS device. This is called subthreshold conduction. Drain to source leakage current I_{DSleak} as well as the gate to source leakage current I_{GSleak} were measured at respectively $V_{GS}=0$ and $V_{DS}=0$. Increased leakage is a common failure mode resulting from non catastrophic overstress of a semiconductor device, when the junction or the gate oxide suffers permanent damage not sufficient to cause a catastrophic failure. On the Figure 4.7 the drain leakage curve I_{DSleak} has an exponential form due to its conduction properties, and the gate leakage curve I_{GSleak} can be explained by the tunnel effect for $V_{GS} \leq -20V$ and $V_{GS} \geq 20V$, whereas the rest is noise. The large variations in the gate leakage curve are due to measuring incertitude as values are really low, around $1e^{-11}$ A.

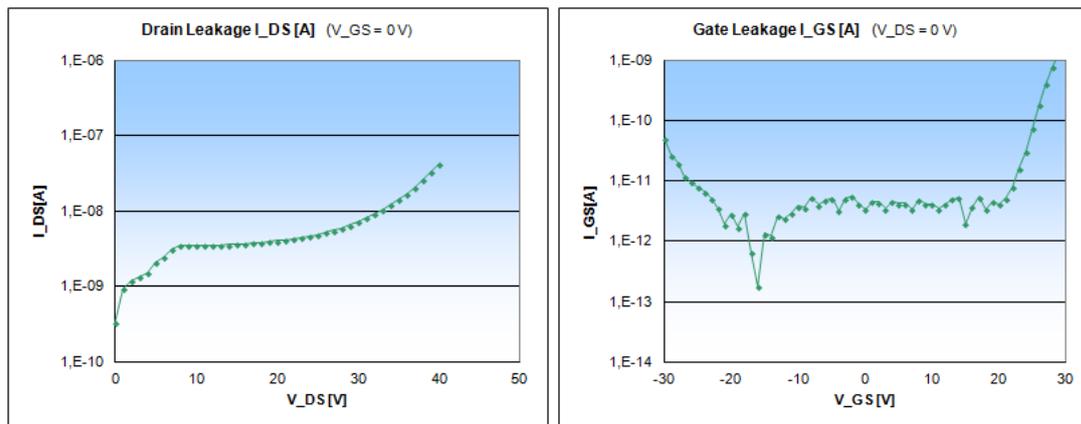


Figure 4.7: Drain and gate leakage of one MOSFET

The R_{DSon} is a characteristic of a power device. It corresponds to the drain to source resistance and is temperature dependent. Thus a pulse test is performed at room temperature to measure this parameter minimizing heating of the junction. During this test I_{DS} and V_{DS} are measured while applying the maximum V_{GS} . The R_{DSon} is then deduced with the ohmic law: $R_{DSon} = V_{DS}/I_{DS}$ (Figure 4.8). When the chip is degraded it leads to an increase in the R_{DSon} .

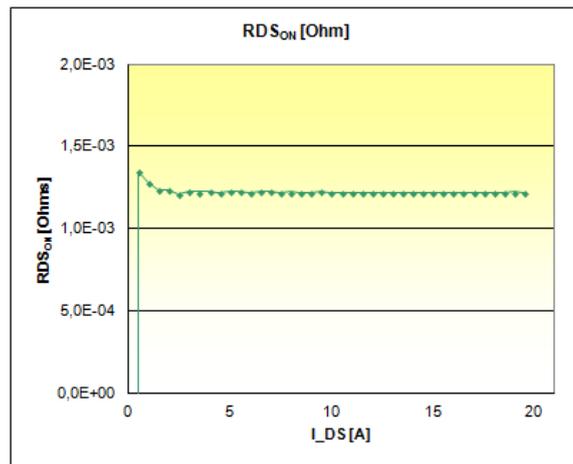


Figure 4.8: R_{DSon} of one MOSFET

4.1.2.1.2 Thermal measurement

The thermal impedance Z_{th} is measured respecting the norm JEDEC-JESD51-14 [JESD10] via an equipment from MentorGraphics and its T3ster-Master Software that enables the interpretation of measurements (Figure 4.9). This equipment has a $1\mu s$ time resolution, registers up to 64 000 data points and has a high resolution of 12 bit in $\Delta U=50mV$ [Men00]. The Z_{th} measurement is performed by loading the body diode of one power MOSFET of the package. The body diode conducts a loading current of approximately 5A for 10s, the time needed to reach the thermal steady state. Then the load current is switched off and the cooling behavior is measured during 10s until the junction temperature cools down to the environment temperature. The temperature rise is measured on the device by electrical means through the forward voltage V_f of the body diode which is a TSP. The TSP is turned into temperature via a sensitivity factor K , which is a characteristic of the device. For our module the factor K was determined to be approximately equal to 2,2 mV/K. Once the measurement performed, the T3ster-Master software enables us to visualize the Z_{th} curve and to interpret this curve as a cumulative or derivative structure function, already described in the chapter 3. Degradations in module's layers generate an increase in the Z_{th} curve.

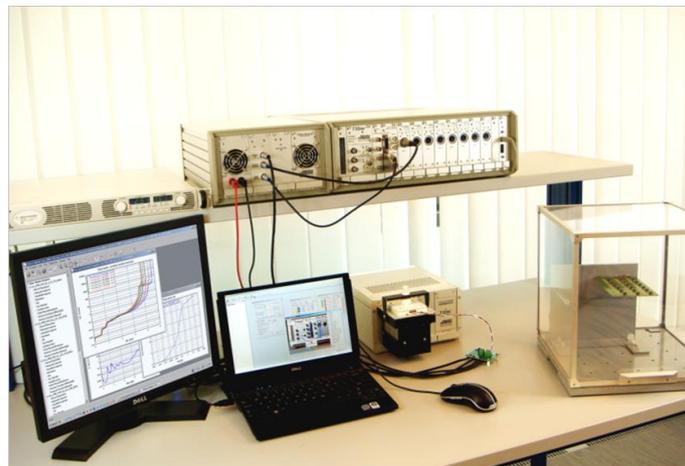


Figure 4.9: Test bench to measure the Z_{th} [Men00]

4.1.2.2 Optical analysis

Once the device tested and electrically and thermally characterized, some microscopic observations are carried out. First of all, the module was carefully examined at naked eyes to detect any big deformations, or visible cracks in the package. Then a Scanning Acoustic Microscope (SAM) is used to detect delamination at the interface mold/ Cu lead frame or degradation at solder joints area. A SAM analysis is a non destroying control technique that allows scanning the entire package. Thus it gives an overview of the module's degradations and help to decide if it is worthy to investigate the device more in details and with which

method. For example based on SAM observations one can define where a cross-section could be cut. Moreover, SAM allows an approximated measure of delaminated surface at solder joints (Figure 4.10). Sometimes, X-ray was also performed on modules, highlighting as well degradations in solder joints but also cracks in mold.

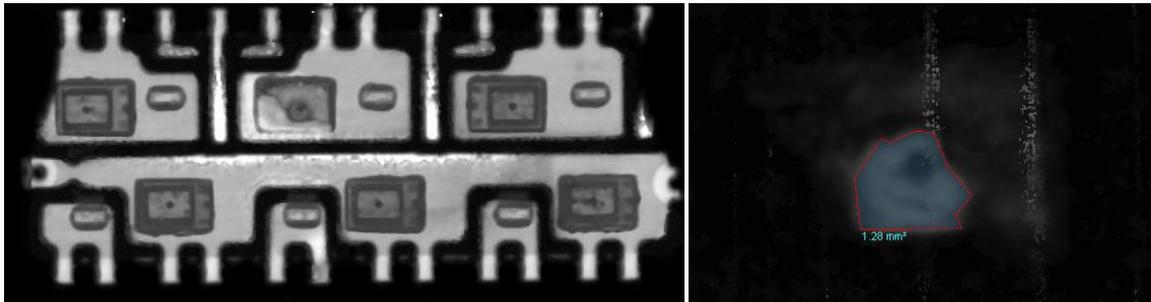


Figure 4.10: SAM picture of the entire B6 Bridge on the left, and measurement of the non degraded area in the top solder, on the right.

After that, one or two cross-sections were cut in the module at degraded area, and are observed under optical microscope and Reflection Electron Microscope (REM) (Figure 4.11). With the optical microscope one can see distinctly deformations and cracks of layers, while the REM allows a more detailed analysis of microcracks, voids and grains structure. In order to highlight delamination in package, the cross-section was observed with the dye and pry method. It consists in coloring the specimen with UV oil, which will penetrate in voids, cracks and delaminated zone. Thus by observing the metallographic specimen under UV light microscope, cracks are appearing in white color whereas the rest of the module is dark.

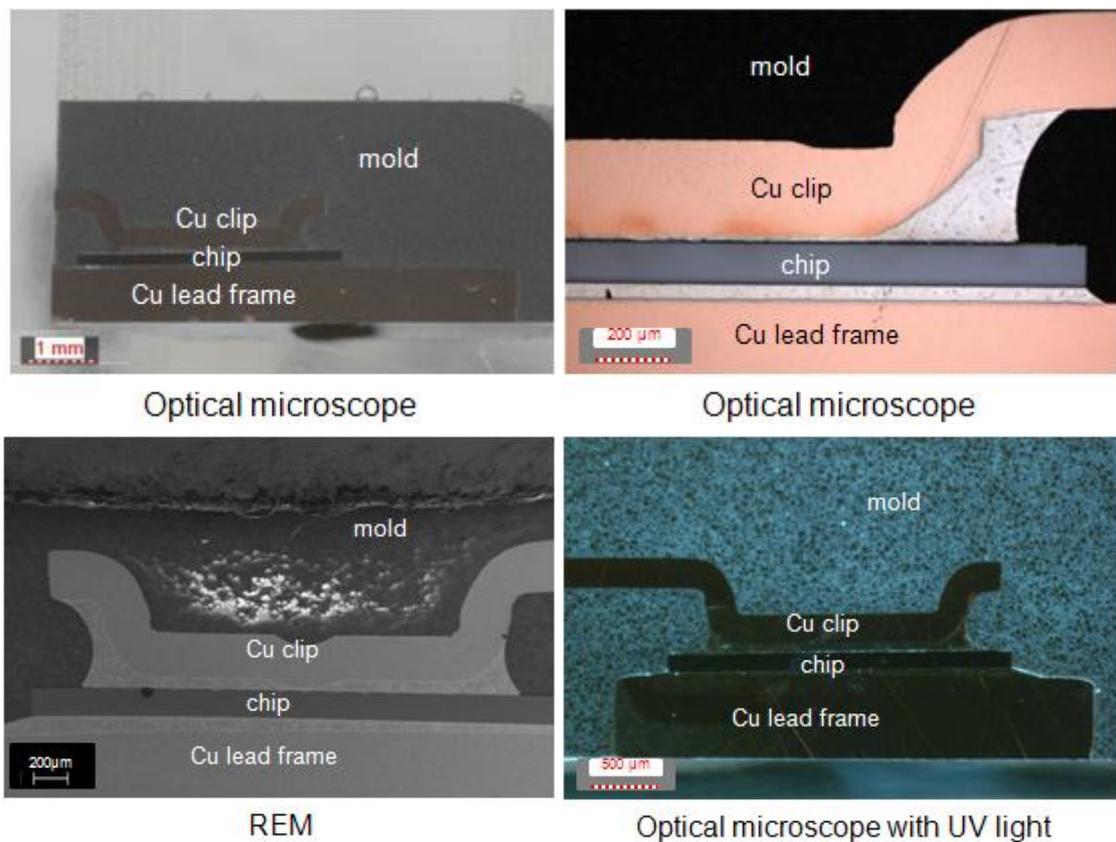


Figure 4.11: Cross-sections of metallographic specimens

4.2 Failure mechanisms observed after Active Power Cycling

4.2.1 Failure mechanisms in the entire module

About 30 samples were tested with varying sets of test parameters, covering the DoE:

- T_{jmin} ranges from -30°C to 100°C
- ΔT_j ranges from 60K to 130K
- t_{on} ranges from 0,2s to 10s

There was also 4 tests that were performed at negative T_{jmin} (-30°C) and with very large ΔT_j ($155\text{K} \leq \Delta T_j \leq 180\text{K}$), in order to highly accelerate the test and find out if the resulting failure mechanisms are comparable with the ones of PTC.

As no EoL criterion was defined, tests were stopped arbitrarily when the increase in the body diode forward voltage V_f or in the temperature swing ΔT_j was judged high enough. Tests with a $\Delta T_j \leq 130\text{K}$ were stopped after 60 000 to 2 million cycles, and modules were always electrically functional at the end of tests. This proves the high reliability of such power modules with double sided soldered chips. Despite this good endurance, modules are submitted to degradation phenomena. The different failure mechanisms occurring are:

- Cracks in chip
- Delamination at the interface mold/Cu lead frame or mold/Cu clip
- Degradations and cracks in solder layers
- Cracks in molding compound
- Delamination at interface Al metallization/top solder
- Cracks in Al metallization
- Delamination at interface IMC/solder or cracks in IMC

All these failure mechanisms are pictured on the Figure 4.13. Some of these failures are well known in microelectronics, like the brittle cracking of the chip which originates from microcracks in silicon induced by sawing. In our case, a crack in chip was observed only once, and it is not quite clear if the crack was induced by APC or by cutting the cross-section. So cracks in chip may occur in our module but it is not a systematical failure mechanism. Then, the delamination between mold and Cu lead frame is also well known as a lot of work has already been dedicated to study this phenomenon. Solder degradation is a critical failure already known and extensively studied under PTC. The solder degradation can also be influenced by the irregularity of the solder thickness. Indeed, due to the difficulty to accurately place and fix the chip or the clip on the solder paste, chip and clip may slightly move during the soldering process, thus leading to an inclination of solder layers (Figure 4.12). Cracks in mold hardly ever happen, but can cause other failures in the device, like solder degradations. Degradations in Al metallization and IMC as well as delaminations at interfaces solder/Al metallization and solder/IMCs are typical failures occurring under APC. Indeed, deformations in Al metallization were never observed in our module after performing PTC.

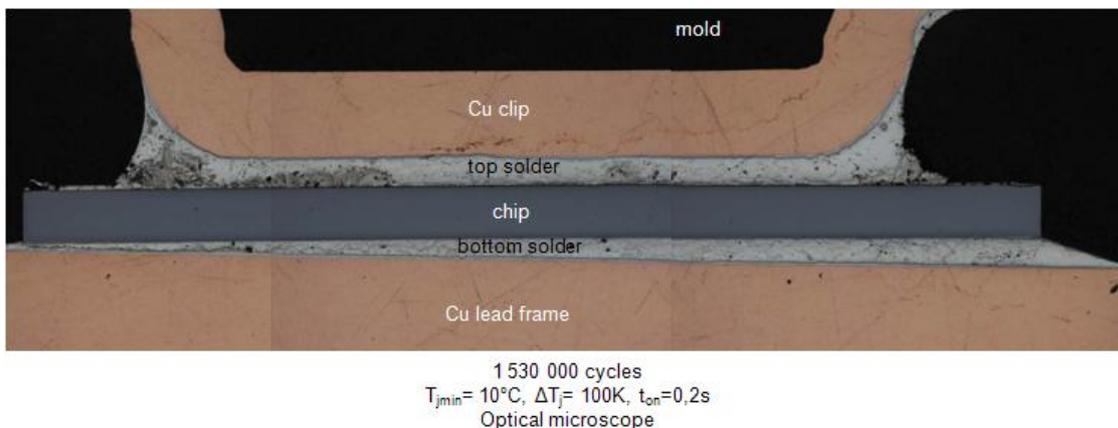


Figure 4.12: Significant inclination of the bottom solder layer

Failure mechanisms were often combined, thus several different failure mechanisms can occur simultaneously. For example, some samples presented cracks in solders, with deformations in the Al metallization and delamination at the interface mold/Cu lead frame. The few samples tested under high ΔT_j , were subjected to the same failure mechanisms as the other samples, but had a shorter lifetime as tests were

stopped quite rapidly due to a rapid increase in V_f . For all samples tested, no significant differences were observed concerning the out and transfer characteristics and the leakage currents. There were only changes in V_f , ΔT_j , R_{Dson} and Z_{th} . These changes as well as the degradations observed on metallographic specimens are analyzed more in details and layer per layer in the following paragraphs.

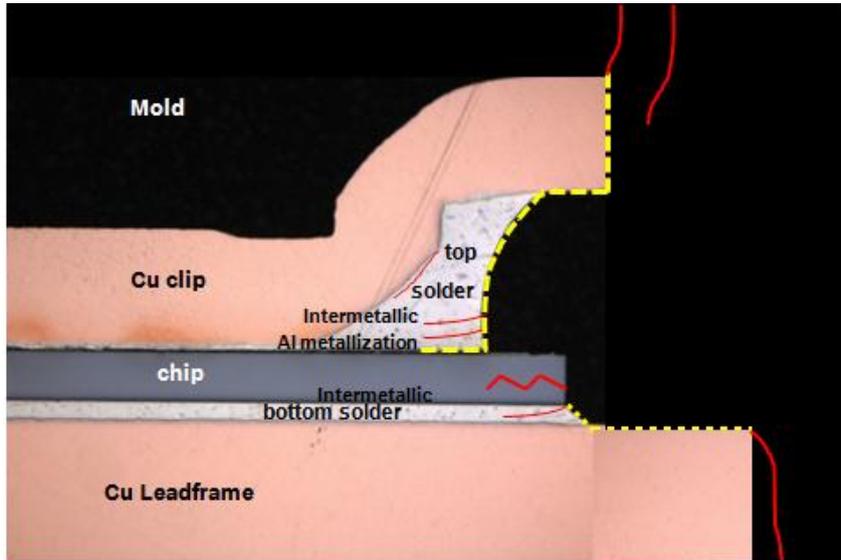


Figure 4.13: Schema showing all failure mechanisms occurring in the B6 Bridge: cracks are pictured in red and delaminations in yellow.

4.2.2 Failure mechanisms in the bottom solder

About 30 tests with different parameters were performed and analyzed, but only 13 of them were taken as representative examples for bottom solder degradations and are shown in the Table 4.1. This recap chart shows only 13 tests that were performed, in order to give a clear overview. When a – appears in the table, it means that there was no increase in parameter or no degradations observed.

T_{jmin}	-30°C				15°C					45°C ≤ T_{jmin} ≤ 70°C			
ΔT_j	60K	120 K			60 K	90 K	120K			60K	90 K		110K
t_{on}	0,2s	0,5s	2s	5s	0,2s	0,5s	0,5s	2s	7s	0,2s	0,2s	2s	0,35s
t_{off}	0,8s	2,5s	7s	10s	3s	4,5s	3,5s	6s	5s	1,2s	2,8s	5s	1,15s
Number of cycles	3.000.000	510.000	110.000	220.000	1.000.000	830.000	1.430.000	911.000	61.640	2.270.000	2.068.510	900.702	629.543
increase in V_f	-	+3,5%	+1%	+6%	-	+0,5%	+6,5%	problem	+1%	+1%	-	-	+6,6%
increase in ΔT	-	+17%	+3,5%	+12,5%	-	-	+8,3%	problem	0	-	-	-	+22%
increase in Z_{th} at 0,01s	+2,75%	-	+16%	+36,5%	-	-	+2%	-	-	-	-	-	yes
inclination bottom solder	-	-	yes	-	yes	yes	-	-	-	-	-	-	-
Degradations in bottom solder	-	cracks at chip edges	cracks at chip edges	long cracks and voids at chip edges	-	recrystallization and voids at chip edges	voids and cracks at interface with CuLF and big voids under the clip	strong recrystallization and cracks at chip edges and cracks at interface with CuLF	cracks at chip edges	-	cracks at chip edges	cracks at chip edges and at the interface with CuLF	cracks and thick IMC layer at chip edges
crack length max (µm)	-	411	400	-	-	-	704	552	-	-	-	242	-
% degraded surface	-	-	35	66,67	-	-	42,4	4	40	-	15,2	8,8	-

Table 4.1:Recap chart of 13 of the 30 APC tests performed with the resulting bottom solder degradations

The presence of damage in the bottom solder can be indicated by an increase in the Z_{th} measurement (Figure 4.14). It is known that the main thermal path is at the bottom of the package: the heat flows from the chip through the bottom solder and the Cu lead frame to the heat sink. So, when the bottom solder is degraded, it affects the thermal path, thus the thermal impedance Z_{th} increases at about 0,001s and until the end of the measurement. A maximum seems to be reached at 0,01s.

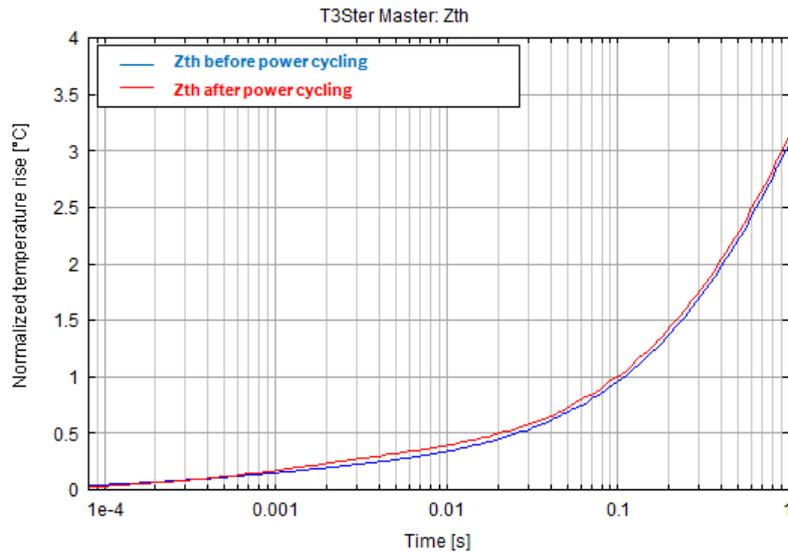


Figure 4.14: Example of an increase in Z_{th} after 110 000 APC cycles with $T_{jmin}=-30^{\circ}\text{C}$, $\Delta T_j=120\text{K}$, $t_{on}=2\text{s}$

With SAM and X ray, degradations in the bottom solder are visible (Figure 4.15). Typically the degradations were observed to start at the edges. When it was possible the degraded surface was measured. This gives us a quantitative idea on the importance of bottom solder's degradations.

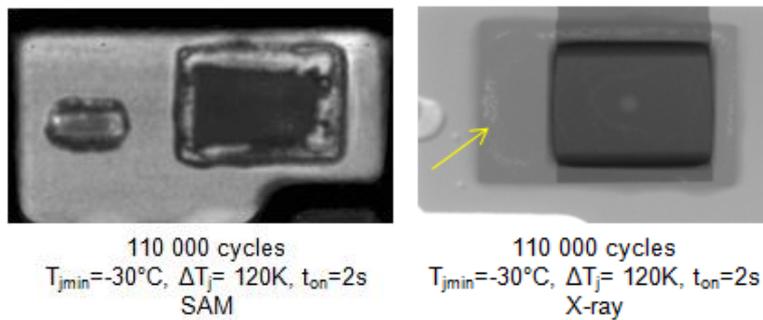


Figure 4.15: Pictures of a bottom solder with degraded edges

Then the observation of metallographic specimens has shown different types of solder degradations: recrystallization, voids and cracks at chip edges as well as an increase in the thickness of IMCs, and cracks at interface with Cu lead frame.

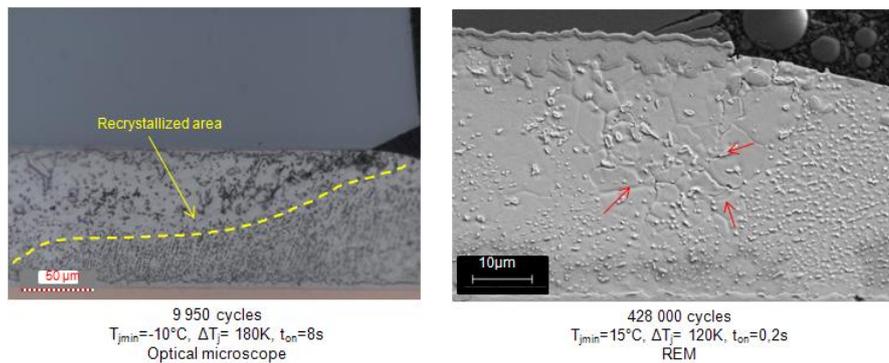


Figure 4.16: On the left, a recrystallized area in the bottom solder and on the right, a recrystallized area with cracks at grain boundaries (red arrows) at chip edges

The observation of recrystallization (Figure 4.16), voids (Figure 4.17) and cracks (Figure 4.18) at chip edges shows that chip edges solder's areas are regions of strain concentration where microstructural changes are initiated and propagate with APC. So chip edges are critical areas. Sometimes it was also noticed that cracks located at chip edges were propagating close to the interface with the IMC layer. Cracks propagating from chip edges toward chip center were also described in the literature for standard modules with Al wire bonds

and lead rich or lead free die attach [Amr06, Har10, Kra12, Sow13, Dug14, Her14]. But some other papers [Fel08, Lut08, Sche11, Hen12, Schm12, Schm13, Ste13] described a different crack propagation starting under the center of the chip as it is the hottest point in the module and expanding to the edges. In our case no hot points are to be seen in the chip, as no wire bonds are used as interconnect, but a Cu clip which homogeneously distributes the heat thanks to its large surface in contact with the chip.

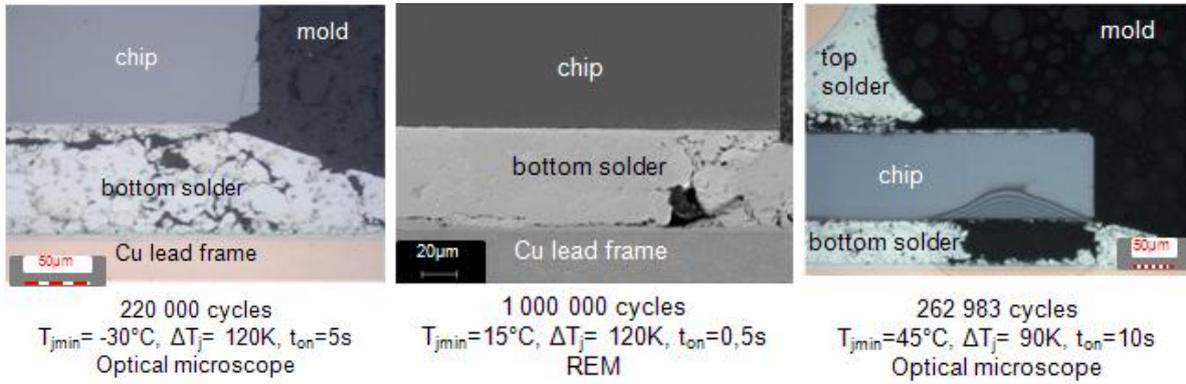


Figure 4.17: Voids in bottom solder

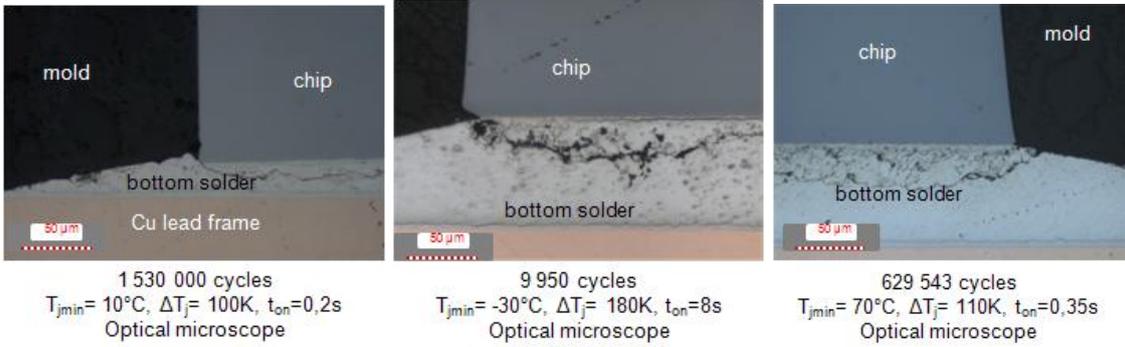


Figure 4.18: Cracks at chip edges

In our case, microstructural changes seem to occur in the 4 different phases of recovery, recrystallization, intergranular cracking and coalescence of cracks, described by [Mat10, Rat10]. The phenomenon of an increase in the thickness of the IMC layer due to APC (Figure 4.19) is also known and was already observed by [Lau07].

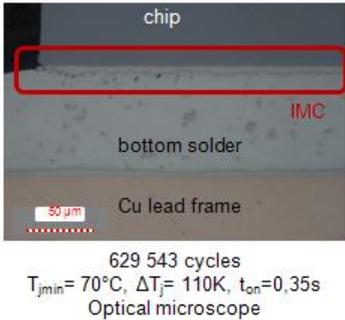


Figure 4.19: Thick IMC layer

Cracks at the interface with the Cu lead frame rarely occur (Figure 4.20). This was observed for only 4 cases. It is interesting to notice that here cracks are running at the interface between the IMC and the solder.

By comparing test results in function of test parameters, no clear assumptions can be made concerning the influence of tests parameters on solder degradation. Nevertheless one can notice that for tests performed with a field load of $\Delta T_j = 60K$, no significant increase in V_f or in ΔT_j were registered even after several millions of cycles. The metallographic analysis of these samples did not reveal any degradation in the bottom solder. Thus one can conclude that increasing the ΔT_j leads to more severe degradations in the bottom solder.

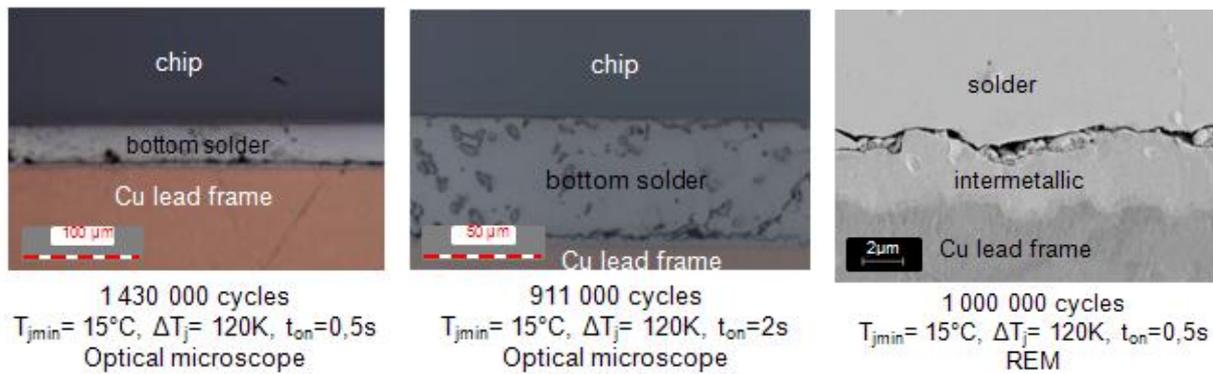


Figure 4.20: Cracks at the interface with Cu lead frame between the solder and the IMC

4.2.3 Failure mechanisms in the Al metallization

Just like for the bottom solder, some representative cases were taken out of the 30 tests performed and are presented in the Table 4.2 in order to have a general idea on tests and results in terms of Al degradations.

T_{jmin}	-30°C				15°C						45°C ≤ T_{jmin} ≤ 70°C		
	60K	120 K			60 K	90 K	120K				60K	90 K	110K
ΔT_j	60K	120 K			60 K	90 K	120K				60K	90 K	110K
t_{on}	0,2s	0,5s	2s	5s	0,2s	0,5s	0,2s	0,5s	2s	10s	0,2s	0,2s	0,35s
t_{off}	0,8s	2,5s	7s	10s	3s	4,5s	3,8s	3,5s	6s	5s	1,2s	2,8s	1,15s
Number of cycles	3.000.000	510.000	110.000	220.000	1.000.000	830.000	428.000	1.430.000	911.000	262.983	2.270.000	2.068.510	629.543
increase in Vf	-	+3,5%	+1%	+6%	-	+0,5%	+6,2%	+6,5%	+6%	+25%	+1%	-	+6,6%
increase in ΔT	-	+17%	+3,5%	+12,5%	-	-	+13,5%	+8,3%	+8%	+40%	-	-	+22%
increase in Z_{th} between 2e-4s and 0,02s	-	yes	yes	-	-	-	yes	-	yes	problem	-	yes	yes
increase in R_{DSon}	6,50%	+62%	+29%	+193%	-9%	+0%	+45%	+43%	+20%	problem	+15,5%	+23%	+54%
Degradation in Al	-	deformation, long cracks, and migration at top solder meniscus	delamination Al/top solder at top solder meniscus	deformation delamination Al/ top solder and migration at top solder meniscus	-	strong degradation and cracks at top solder meniscus	deformation, delamination Al/ top solder, cracks and migration at top solder meniscus	big deformation under the dimple area, delamination Al/top solder, cracks and migration at top solder meniscus	slight deformation and long cracks at top solder meniscus	deformation and cracks at top solder meniscus	-	delamination and cracks at top solder meniscus	strong deformation and migration at top solder meniscus
crack length max in Al (μm)	-	1279	-	-	-	-	-	904	929	-	-	1055	-
% delaminated surface top solder/AlCu	-	44,44	60	-	-	-	-	80	20	-	-	21,74	73,33

Table 4.2: Recap chart of 13 of the 30 APC tests performed with the resulting Al degradations

The presence of damage in Al after APC can be indicated by an increase in the resistance R_{DSon} . Indeed, the metallization layer is on top of the chip, and has to homogeneously distribute the current to the chip. When the metallization is degraded, the current is no longer perfectly distributed, thus generating an increase in the resistance R_{DSon} . A slight increase in thermal impedance Z_{th} at the beginning of the measurement can also be an indication of Al degradation. It was shown that the main thermal path is at the bottom of the package, and that bottom solder's degradations lead to a Z_{th} increase reaching a maximal value at about 0,01s. But for this module, there is also a top side cooling path which evacuates the heat from the chip, through the metallization, the top solder, the Cu clip and the mold to the air. This top side thermal path represents about 5% of the total cooling of the MOSFET. Thus Al degradations will affect the top side cooling path, and induce a slight increase in the thermal impedance Z_{th} at the beginning of the measurement between $2e^{-4}$ s and 0,02s as the Al metallization is close to the chip (Figure 4.21). But this slight increase in Z_{th} can only be used as an indication of possible Al degradation as this increase can also be due to top solder degradation. Moreover this increase is so slight that it is at the resolution limit of measurement equipment. So, in order to confirm the assumption of Al degradation, a failure analysis has to be carried out.

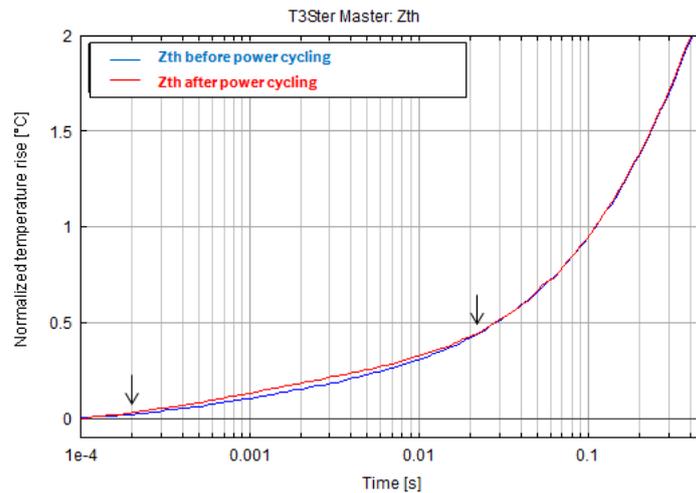


Figure 4.21: Example of a slight increase in Z_{th} after 428 000 APC cycles with $T_{jmin}=15^{\circ}C$, $\Delta T_j=120K$, $t_{on}=0,2s$

Different types of degradation in Al were highlighted: deformation of the layer (Figure 4.22) migration of Al in the top solder (Figure 4.23), delamination between Al and top solder (Figure 4.24), and cracks within the layer (Figure 4.25). Those degradations appear at the area of Al located under the top solder meniscus. Cracks and delamination between top solder and Al often start at this solder meniscus area, and then propagate to the center of the MOSFET. This differs from standard modules, where reconstruction occurs preferably at the center of the chip and wrinkles due to ratcheting develop from the edge to the middle of the chip. The degradation of the Al metallization seems to be more severe with an increase in temperature swing ΔT_j . Actually for small temperature swing, like $\Delta T_j=60K$, no significant increase in V_f or in ΔT_j were registered, thus tests were stopped after several millions of cycles. Metallographic specimens of these modules were investigated and no degradations at all were observed in Al. Even though, it should be specified that a deeper microstructural analysis should be performed to be able to observe dislocations, recrystallization and intercrystalline voids. Indeed, it may be possible that for $\Delta T_j=60K$, dislocations and recrystallizations occur, but do not reach a critical state leading to observable microcracks.

The influence of T_{jmin} and t_{on} on degradation's phenomena is more difficult to determine. This is also due to the fact that the number of experiments performed is still insufficient to make strong assumptions.

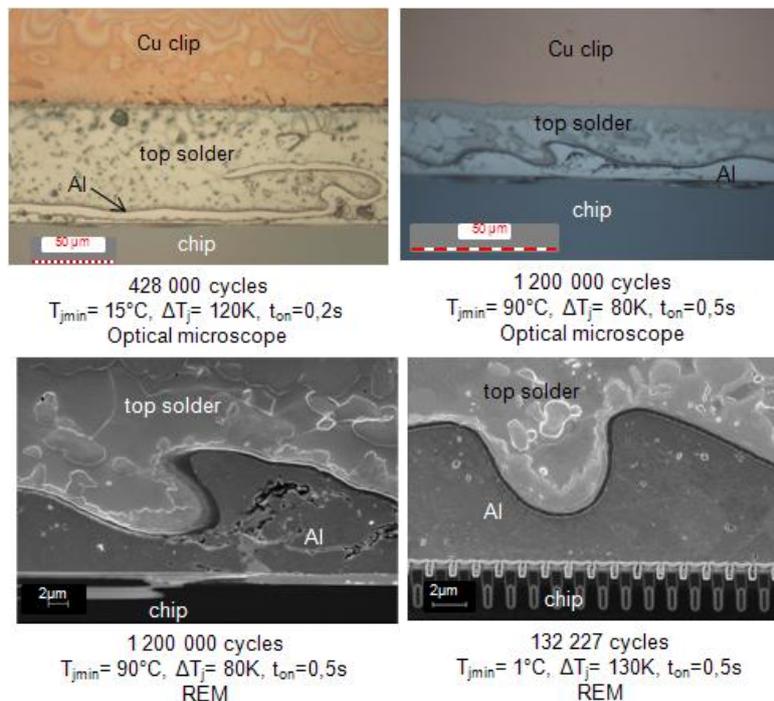


Figure 4.22: Strong Al deformations

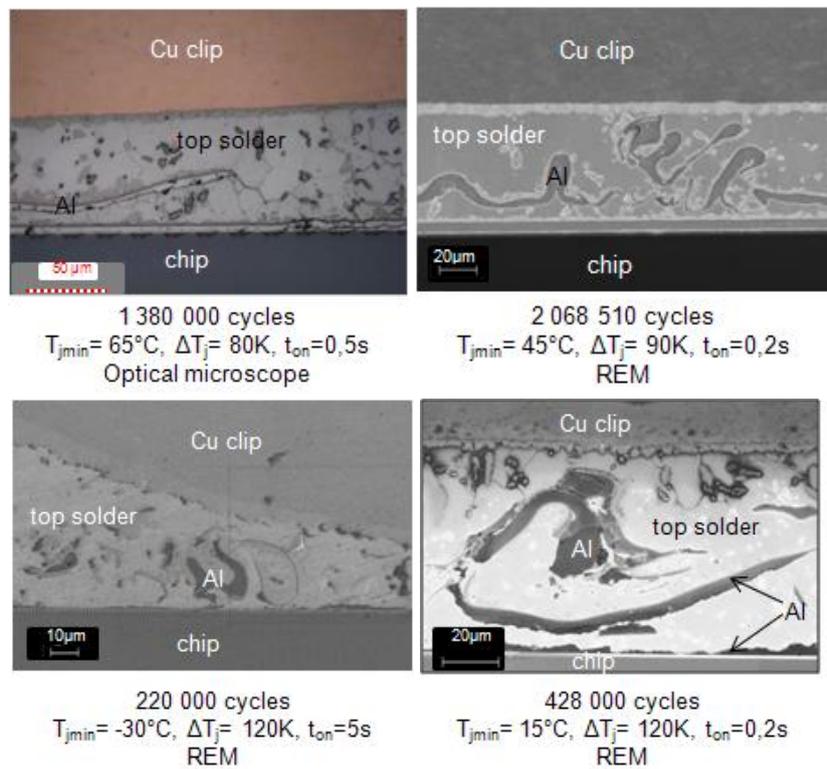


Figure 4.23: Migration of Al in top solder

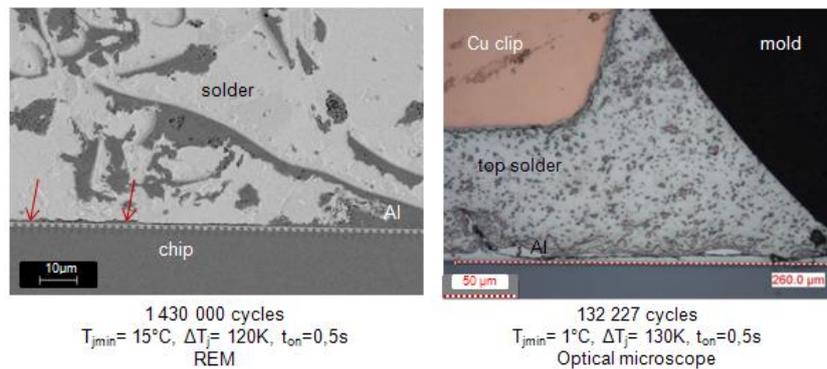


Figure 4.24: Delamination at interface Al/top solder

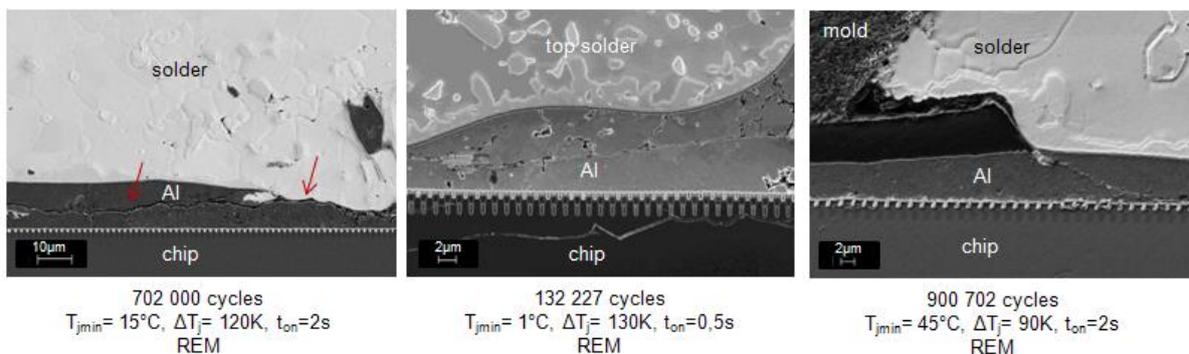


Figure 4.25: Cracks inside the Al metallization

As seen on cross-sections of metallographic specimens, delamination at the interface Al/top solder, and cracks in Al are occurring. These degradations are also visible on SAM and X ray pictures together with degradations occurring in the top solder (Figure 4.26). Indeed with SAM it is not possible to make a distinction between the Al metallization and the top solder, so degradations observed may concern both layers. The degraded area of

Al metallization and top solder can be estimated with SAM, giving us a quantitative idea on the importance of degradations in those layers.

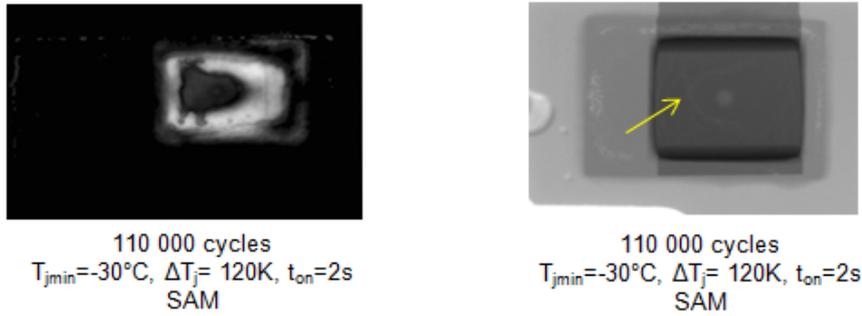


Figure 4.26: SAM and X ray pictures of degradations in the Al metallization and the top solder

4.2.4 Failure mechanisms in the top solder

Here again some representative cases in terms of top solder's degradations were taken out of the 30 tests performed and are presented in the Table 4.3.

T_{jmin}	-30°C				15°C					60°C ≤ T_{jmin} ≤ 70°C		
	60K	120 K			60 K	90 K	120 K			60K	80K	110K
ΔT_j	0,2s	0,5s	2s	5s	0,2s	0,5s	0,2s	0,5s	2s	0,2s	0,5s	0,35s
t_{on}	0,8s	2,5s	7s	10s	3s	4,5s	3,8s	3,5s	3s	1,2s	1s	1,15s
t_{off}												
Number of cycles	3.000.000	510.000	110.000	220.000	1.000.000	830.000	800.000	1.000.000	702.000	2.270.000	1.380.000	629.543
increase in Vf	-	+3,5%	+1%	+6%	-	+0,5%	+10,75%	+4%	+6%	+1%	-	+6,6%
increase in ΔT	-	+17%	+3,5%	+12,5%	-	-	+6%	+4%	+8%	-	-	+22%
increase in Z_{th} between 2e-4s and 0,02s	-	yes	yes	-	-	-	-	-	-	-	yes	yes
increase in R_{DSon}	6,50%	+62%	+29%	+193%	-9%	+0%	+114%	+50%	+32%	+15,5%	+26%	+54%
inclination top solder	-	-	yes	-	yes	yes	-	-	yes	-	-	-
Degradation in top solder	-	cracks and voids at meniscus above the chip	delamination at interface with Al and cracks at meniscus	cracks at interface with Al and presence of Al and IMC at meniscus above the chip	voids at grain boundaries at meniscus and along Cu clip and recrystallization above the chip	voids at grain boundaries and recrystallization at meniscus and along Cu clip	cracks at interface with IMC above the chip at meniscus and recrystallization at cracks	cracks at meniscus above the chip, voids and cracks along Cu clip and strong recrystallization at meniscus	voids at meniscus above the chip and along Cu clip	-	cracks and voids at interface with IMC above the chip, presence of Al and strong recrystallization at meniscus	strong degradation of almost the entire clip surface with voids and cracks above the chip, voids and presence Al at meniscus
% delaminated surface top solder/AlCu	-	44,44	60	-	-	-	81,75	85	-	-	33,33	73,33

Table 4.3: Recap chart of 12 of the 30 APC tests performed and the resulting top solder degradations

The presence of damage in the top solder is actually difficult to distinct from damage in the Al metallization due to the proximity of these layers. An increase in the R_{DSon} indicates degradations in the Al metallization but it can also be a sign of degradations in the top solder. However damages in the top solder may have less impact on the R_{DSon} than the Al metallization which purpose is to homogeneously distribute the current to the chip. Thus if the top solder is degraded, but the Al metallization remains intact, degradations in the top solder will be compensated by the Al metallization and no significant increase in R_{DSon} will occur.

A slight increase in thermal impedance Z_{th} at the beginning of the measurement was reported as an indication of degradation in the Al metallization but it can also be a top solder's degradation. The proximity of both layers and their thin thicknesses make impossible to clearly distinct each layer in a Z_{th} curve. To certify that degradations are located in the top solder, microscope analysis has to be carried out.

As explained for the Al metallization, degradations in the top solder are visible with SAM and X ray but are mixed up with degradations in the Al metallization. Thanks to the observation of metallographic specimens different types of degradations occurring in the top solder were highlighted: recrystallization (Figure 4.27), voids and cracks (Figure 4.28) as well as delamination at the interface with Al metallization or with IMC. These degradations are taking place most of the time at the top solder meniscus, above the chip, but also at the meniscus along the Cu clip. The degradations observed are similar to the ones occurring in the bottom solder, and both appear close to the chip. But damages in the top solder are also influenced by the specific geometry

of the Cu clip. Indeed, the top solder meniscus has to follow the round shape of the clip, and quite often voids and cracks were observed close to the Cu clip (Figure 4.29). The types of degradations and their locations occurring in the top solder cannot be compared to the literature, as only few papers studied module with clip, and when they did the clip attach was not the focus of the study.

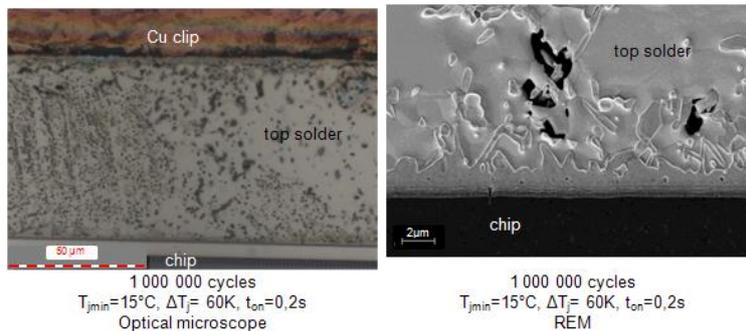


Figure 4.27: Recrystallization and voids at interface above the chip

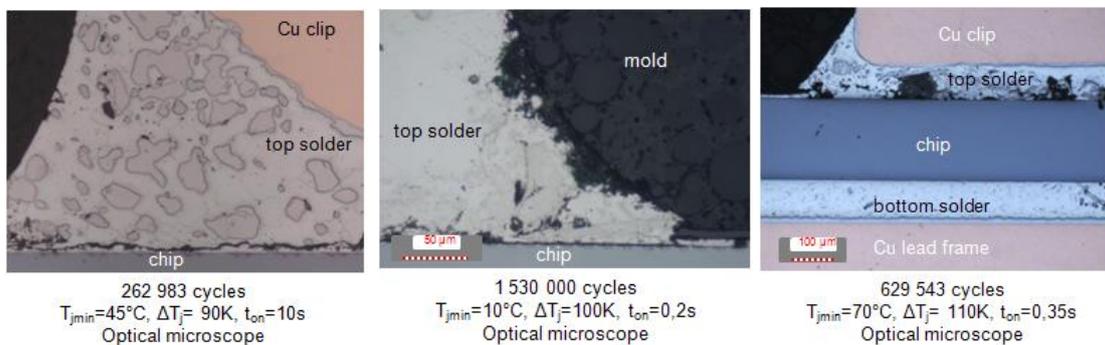


Figure 4.28: Voids and cracks at the meniscus above the chip

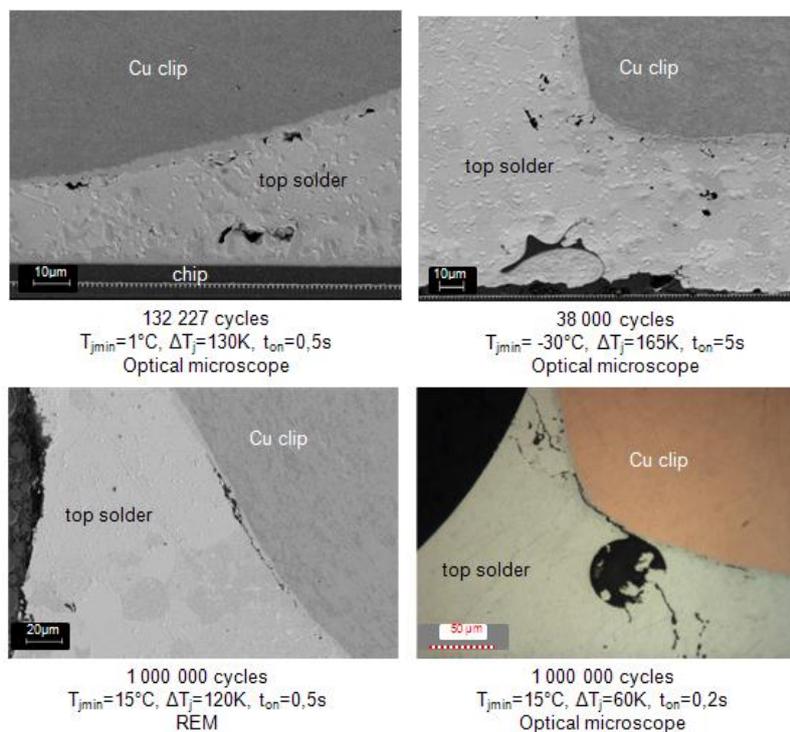


Figure 4.29: Voids and cracks at the meniscus along the Cu clip

Once again it is difficult to determine the influence of tests parameters on the top solder degradation. Nevertheless, it appears in the Table 4.3 that for the 3 tests performed with $\Delta T_j=60K$ no significant increase in V_f or in ΔT_j were registered even after 1 to 3 million of cycles. Then for 2 of those tests, no degradations were noticed in the top solder. For the third one with $T_{jmin}=15^\circ C$, degradations reported can be considered as minor as only recrystallization and voids are observed but no cracks. So this confirms that high ΔT_j are accelerating the occurrence of failure mechanisms in the top solder.

4.2.5 Failure mechanisms in the mold

Representative cases in terms of mold degradations are summarized in the Table 4.4.

T_{jmin}	-30°C			15°C					60°C ≤ T_{jmin} ≤ 70°C		
ΔT_j	60K	120K		60K	90K	120K			60K	80K	110K
t_{on}	0,2s	0,5s	5s	0,2s	0,5s	0,5s	2s	10s	0,2s	0,5s	0,35s
t_{off}	0,8s	2,5s	10s	3s	4,5s	3,5s	3s	5s	1,2s	1s	1,15s
Number of cycles	3.000.000	510.000	220.000	1.000.000	830.000	1.430.000	702.000	262.983	2.270.000	1.380.000	629.543
increase in V_f	-	+3,5%	+6%	-	+0,5%	+6,5%	+6%	+25%	+1%	-	+6,6%
increase in ΔT	-	+17%	+12,5%	-	-	+8,3%	+8%	+40%	-	-	+22%
Degradations in mold	delamination mold/CuLF	delamination mold/CuLF, mold/Cu clip and mold/top solder meniscus and cracks along Cu clip and Cu LF	delamination mold/Cu LF and mold/Cu clip and mold/solders meniscus and cracks close to Cu clip and Cu LF	delamination mold/CuLF	delamination mold/top solder meniscus and cracks along Cu clip	delamination mold/Cu clip and mold/solders meniscus and cracks along Cu clip	delamination mold/CuLF, mold/Cu clip and mold/solders meniscus and cracks close to Cu LF and Cu clip	delamination mold/CuLF, mold/Cu clip and mold/solders meniscus and cracks close to Cu LF	delamination mold/CuLF	delamination mold/Cu clip and mold/solders meniscus	delamination mold/Cu LF and mold/solder meniscus and cracks close to Cu clip

Table 4.4: Recap chart of 11 of the 30 APC tests performed with the resulting degradations in mold

The parameter monitoring does not provide information on mold degradations as it does not influence the electrical functionality of the device and has only a negligible impact on the thermal path of the device. Sometimes cracks in the package were visible at naked eyes, when the mold was strongly damaged (Figure 4.30). The SAM allows detecting delamination at the interface between the mold and the Cu lead frame (Figure 4.31). Then by observing metallographic specimens with UV light, all cracks of the cross-section are highlighted (Figure 4.32). Delamination between mold and Cu lead frame, mold and solders meniscus and mold and Cu clip are often observed. The first delamination to appear is the one at the interface solder meniscus/mold. Then the crack propagates either along the Cu clip or the Cu lead frame. And in the worst cases, delamination propagates even more leading to the creation of cracks close to the Cu clip and the Cu lead frame. If the loading time is long enough the crack can also propagate through the mold and reach the surface of the package.

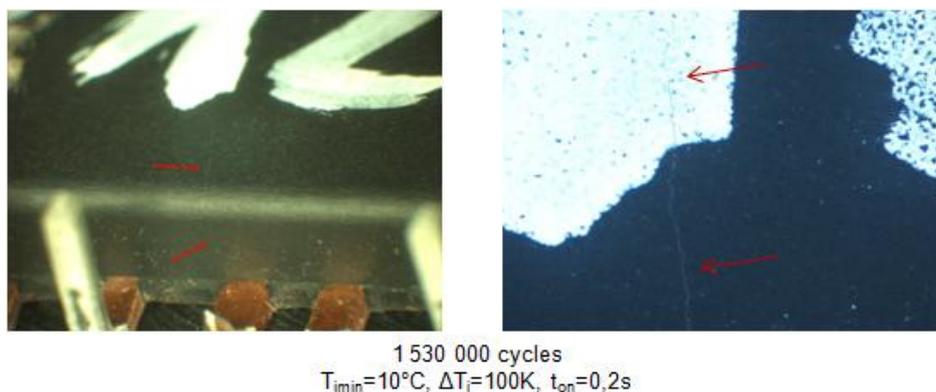
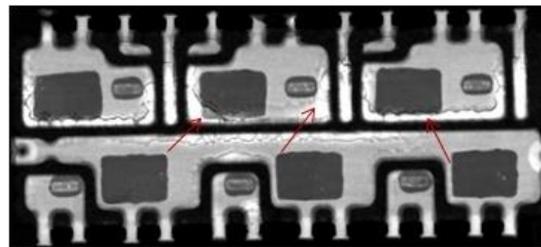


Figure 4.30: Crack in package visible at naked eyes

Delamination between mold and Cu lead frame is a typical issue in power electronic but cracks in the molding package induced by APC were reported in only one paper [Sow13]. One should also remark that only a few number of modules studied under APC are molded and quite often the degradation of the molding compound is not the main focus.

Here also it is difficult to make assumptions on the influence of test parameters on degradations of the mold. For the tests performed with $\Delta T_j=60K$, only delamination at the interface mold/Cu lead frame is reported. Even though only a SAM inspection was carried out for these samples. But still no evidence of cracks inside the package was found. So as expected large ΔT_j are leading to more important damage in the molding compound.



2 270 000 cycles
 $T_{jmin}=60^{\circ}C$, $\Delta T_j=60K$, $t_{on}=0,2s$
 SAM

Figure 4.31: Delamination at the interface mold/Cu lead frame

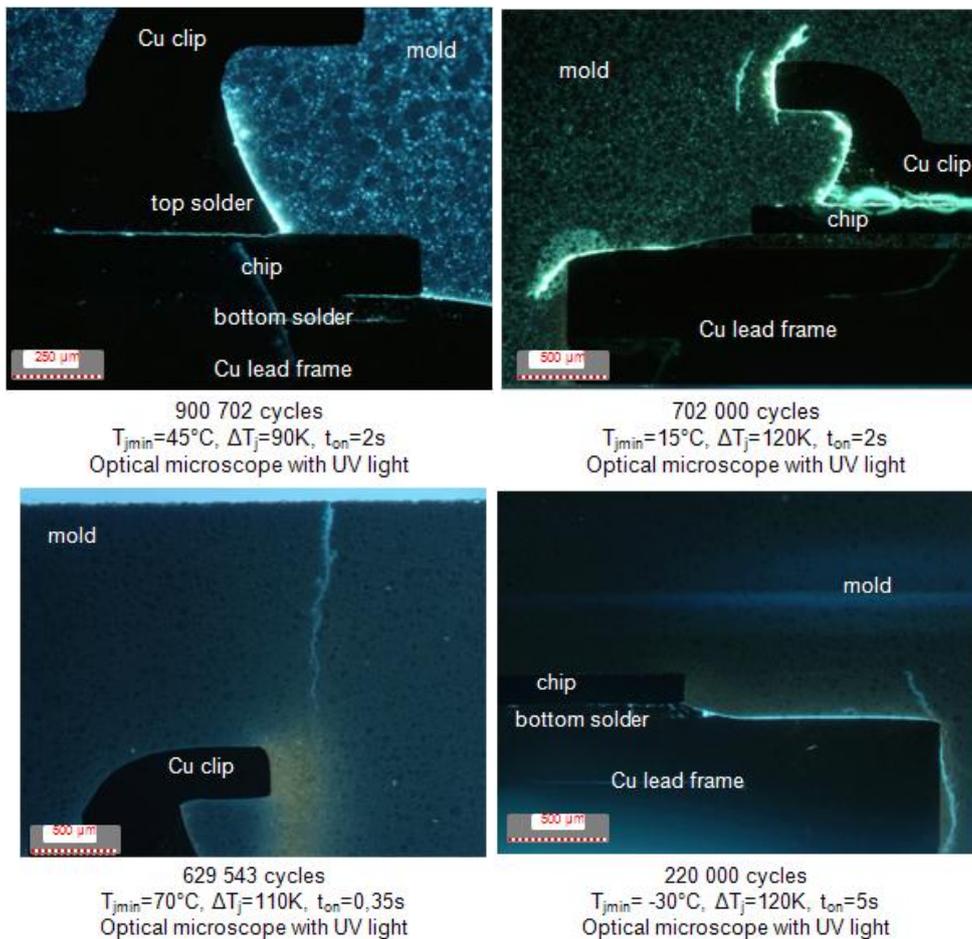


Figure 4.32: Degradations in the mold

4.3 Lifetime prediction

4.3.1 First evaluation of lifetime prediction

To be able to compare tests results in function of the different tests parameters, an End-of-Life (EoL) criterion has to be defined. In a first approach, an increase in V_f of 1% is taken as EoL criterion. This increase of 1% in V_f corresponds for our module to an increase in 5% in V_{ce} , which is a typical EoL criterion used for standard IGBT module. This criterion corresponds actually to a wire lift-off in a standard module. As our module does not have wire bonds but a Cu clip, this criterion does not correspond to a specific failure mechanism occurring in the module and thus may be too severe. But this criterion is here used as a basis to help us determining a suitable criterion for our module.

The number of cycles to failure with the EoL criterion $V_f + 1\%$ is determined for every tests and is plotted for different sets of test parameters (Figure 4.33). Sometimes, the quality of the test was not optimal as some problems occurred for example with the cooling system, thus leading to strong variations in the V_f monitoring. For these tests it was not possible to determine the number of cycles to failure. For some other samples, no increase in V_f is observed thus the number of cycles to failure was not reached before stopping the test. In this case, the number of cycles to failure is reported to be greater than the number of cycles reached until the end of the test. On the histogram these cases are marked with a red arrow on top of the bar.

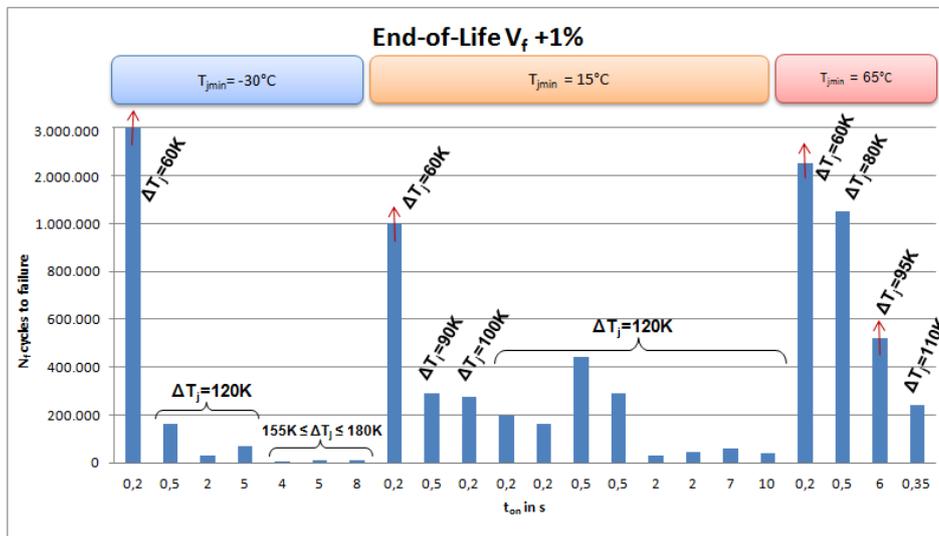


Figure 4.33: Histogram showing the number of cycles to failure N_f with the EoL criterion $V_f + 1\%$ for different sets of test parameters

It appears on the histogram that increasing the ΔT_j reduces the lifetime. So, it confirms what was already seen with the metallographic analysis. It is also important to remark that for all tests performed with $\Delta T_j = 60K$, the EoL criterion is not reached even though devices have already been submitted to several millions of cycles. For a higher ΔT_j of 120K the maximal number of cycles to failure reached is 445 000 cycles. Thus a huge difference of lifetime exist for tests performed with field loads $\Delta T_j = 60K$, and accelerated tests with $\Delta T_j = 120K$. Actually a device under field load can endure about 2,5 times more cycles than with $\Delta T_j = 120K$. This rise the question to know if the failure mechanisms are the same for field loads and high accelerated tests. Simulations will give us more information regarding this issue. Determine the influence of T_{jmin} and of t_{on} is more difficult: more tests have to be performed in order to have more data to compare. Thus it can only be deduced from the experiments that large ΔT_j can be critical for our module in terms of lifetime.

In order to better characterize the influence of test parameters, the number of cycles to failure is plotted in function of each parameter. Here also the tests which did not reached the EoL criterion are indicated by a red arrow. First we study the influence of the ΔT_j , with the Figure 4.34. Even though not enough tests were conducted to be able to make some statistics, a trend line appears quite clearly out of our few results. This shows that there is an exponential relation between the number of cycles to failure and ΔT_j .

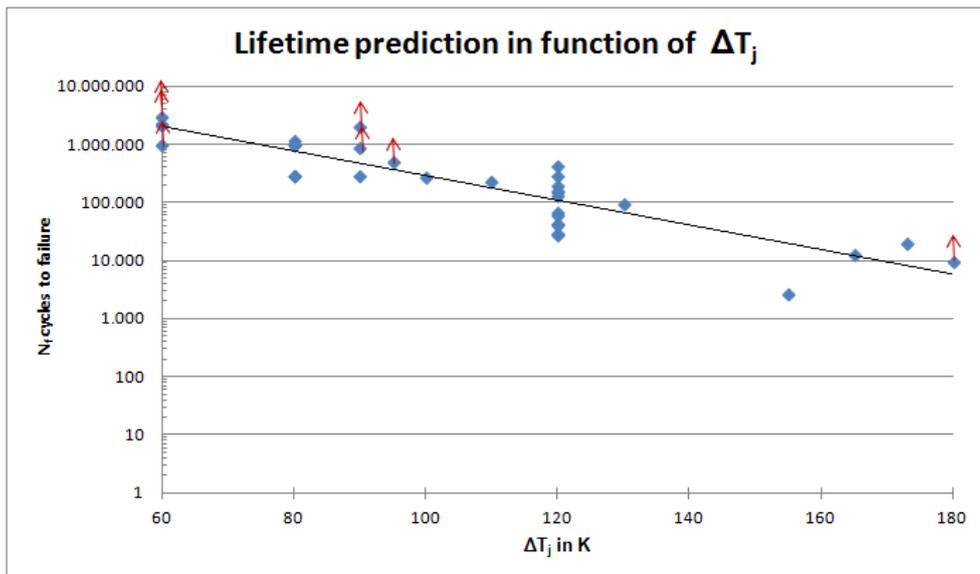


Figure 4.34: N_f cycles to failure with $EoL V_f + 1\%$ in function of ΔT_j

The Figure 4.35 shows the influence of T_{jmin} on the device lifetime. Here 4 exponential trend lines are plotted for 4 different orders of magnitude of ΔT_j . The 4 trend lines are not parallel to each other. The 2 trend lines obtained for $\Delta T_j = 60K$ and $\Delta T_j = 80K$ to $95K$ are indicating that the lifetime stays constant whatever T_{jmin} value. But for the 2 other trend lines obtained for $\Delta T_j = 100K$ to $130K$ and $\Delta T_j = 155K$ to $180K$, the lifetime increases with an increasing T_{jmin} . Thus, no clear trend line emerges out of the experimental results concerning the influence of T_{jmin} on the lifetime, as it also strongly depends on ΔT_j .

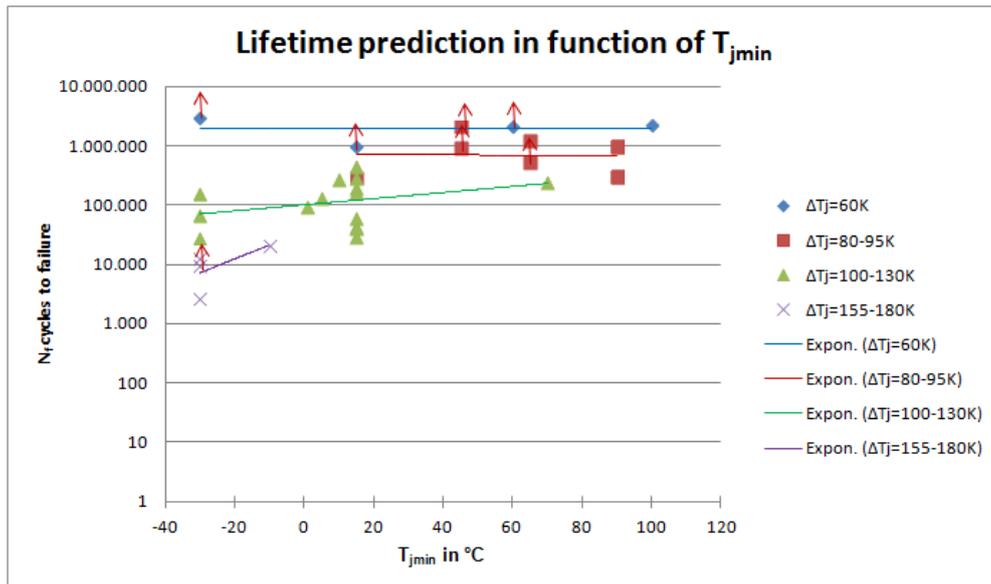


Figure 4.35: N_f cycles to failure with $EoL V_f + 1\%$ in function of T_{jmin}

Finally the influence of the pulse width t_{on} on the device lifetime is studied on the Figure 4.36. Here 4 trend lines emerge for 4 different orders of magnitude for ΔT_j . The 4 trend lines are not parallel to each other, but 3 of them are decreasing with a t_{on} increase. Thus trend lines indicate that the longer the pulse width the shorter the lifetime.

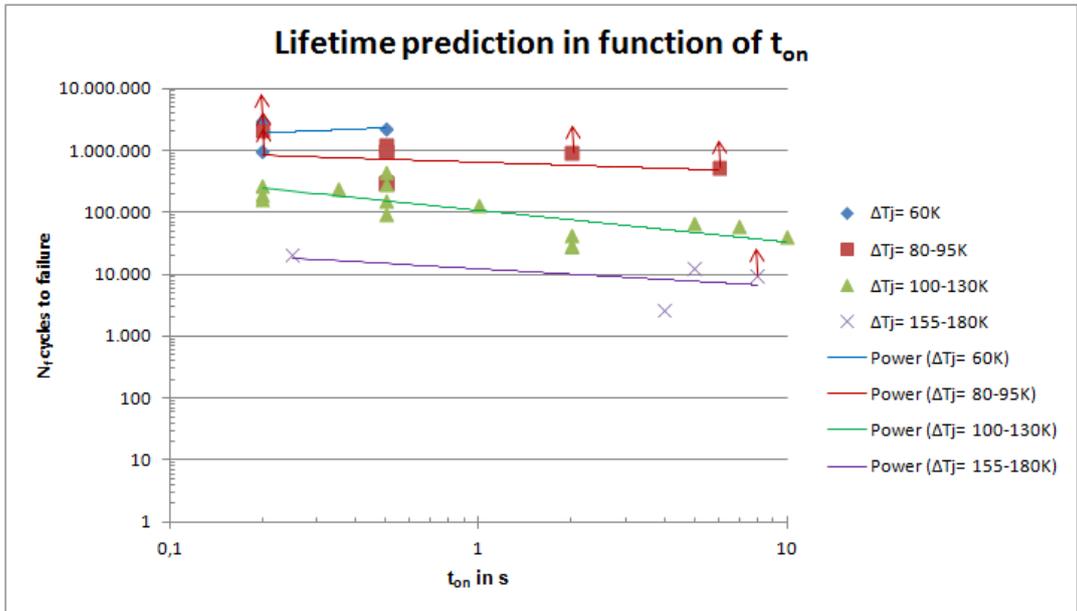


Figure 4.36: N_f cycles to failure with EoL $V_f + 1\%$ in function of t_{on}

Then, results obtained for our module were compared to the ones coming from the literature (cf. chapter 1). The same three graphics were plotted showing respectively the influence of ΔT_j , T_{jmin} and t_{on} on the device's lifetime. Data coming from the literature include all kind of devices (IGBT, MOSFET, diodes...), with all kind of internal structure (with solder or Ag sinter or with wire bonds or ribbons). On the Figure 4.37, one can see that our module is robust as our results are in the upper limit of the scatter chart. Moreover for some points on the chart, our module did not even reach the EoL criterion (points with a black arrow). This supposes a lifetime even higher than what is plotted.

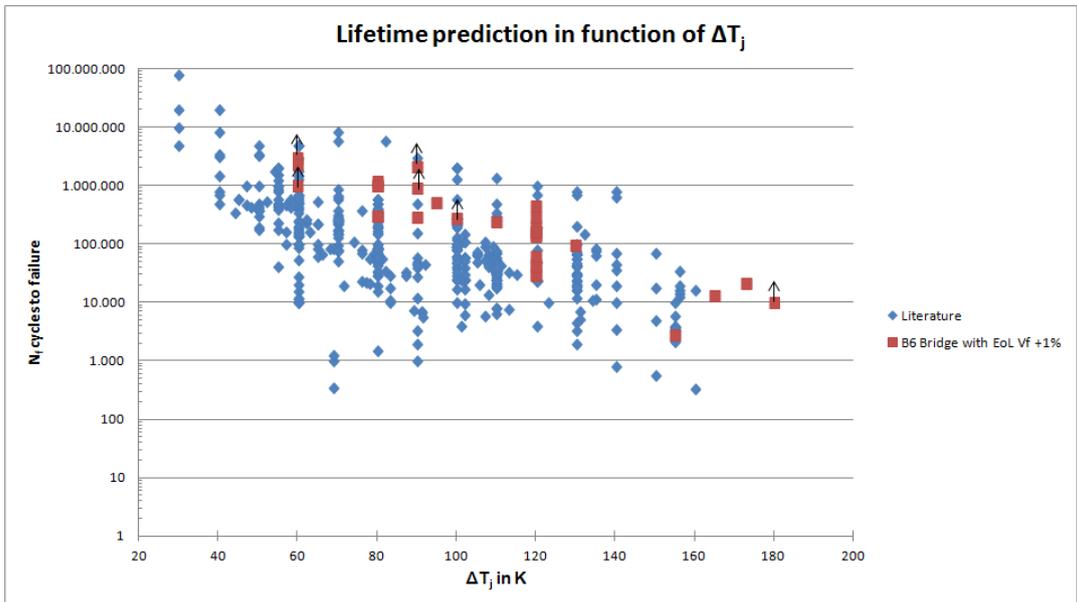


Figure 4.37: N_f cycles to failure in function of ΔT_j for the B6 Bridge with EoL $V_f + 1\%$ in comparison with data from the literature

For the Figure 4.38, results of our module are also in the upper limit of the scatter chart, once again with some points that did not reach the EoL criterion. It appears also that we were the first to perform some tests with a negative T_{jmin} of -30°C . Thus, for those points no comparison with existing results is possible.

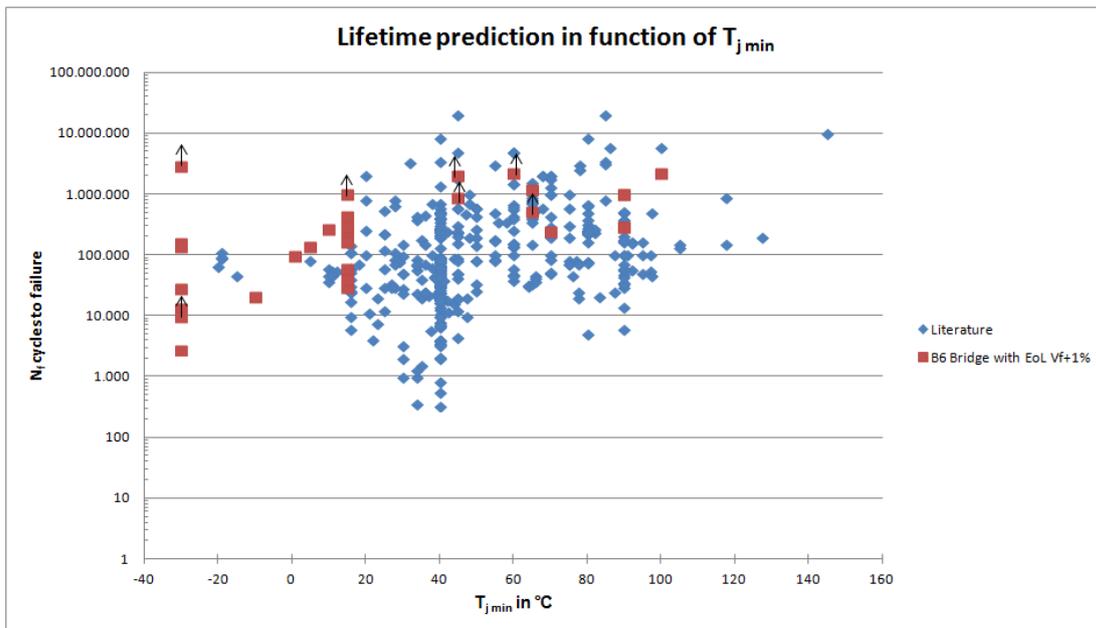


Figure 4.38: N_f cycles to failure in function of T_{jmin} for the B6 Bridge with EoL $V_f+1\%$ in comparison with data from the literature

Finally the Figure 4.39 shows that results of the B6 Bridge are following the same trend as the ones from the literature. Results of our module are more scattered than on the other charts, due to the strong influence of ΔT_j on the results. Thus here the results of the B6 Bridge are not in the upper limit but in the average of the results from the literature. We can notice also that we have done a few tests with short pulse width of 0,2s which was not made until now in the literature.

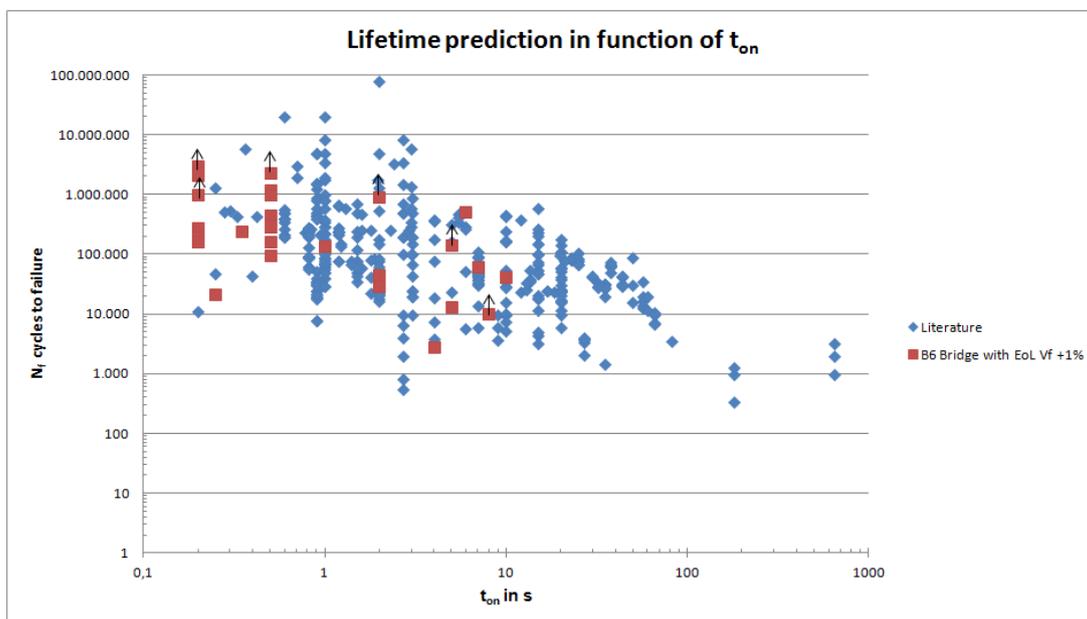


Figure 4.39: N_f cycles to failure in function of t_{on} for the B6 Bridge with EoL $V_f+1\%$ in comparison with data from the literature

4.3.2 Correlation between ageing indicators

In order to define an appropriate EoL criterion for our module, a relation has to be found between the physical degradations and the modifications in electrical or thermal parameters. As reported before, an increase in the Z_{th} at about 0,01s indicates degradations in the bottom solder. Based on that fact, an EoL criterion may be defined using the Z_{th} increase. Thus we try to see if this increase in Z_{th} can be correlated to the percentage of degraded area in the bottom solder, as both were measured. Tests with data on both indicators were selected and the degraded area in the bottom solder is plotted in function of the Z_{th} increase (Figure 4.40). As it can be seen, only 6 tests out of 30 had corresponding data, which is really far from being enough. Actually, an increase in Z_{th} was not often reported and the degraded area of the bottom solder was not systematically measured. Moreover the results are completely scattered, thus making impossible to establish a trend line. This impossibility to find a correlation between the Z_{th} and the degraded area of the bottom solder may also come from the difficulty to interpret a Z_{th} curve. It is also not certain that a Z_{th} measurement is able to take into account cracks which are closed due to the pressure applied by the mold on the rest of the module. So the EoL criterion cannot be defined using the increase in the Z_{th} curve, another parameter has to be found.

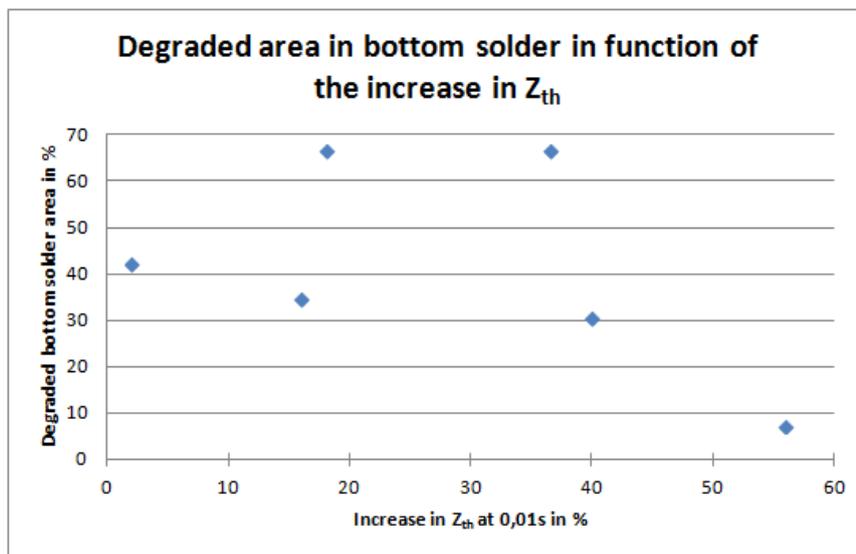


Figure 4.40: Degraded area of bottom solder versus the increase in Z_{th} at 0,01s

Then, it was explained that an increase in the R_{DSon} indicates Al metallization degradations. Thus we also try to see if the increase in R_{DSon} can be correlated to the percentage of degraded area in Al metallization. Tests with corresponding data were selected and the degraded area in the Al metallization is plotted in function of the increase in R_{DSon} (Figure 4.41). This time more data were available, and a trend line emerges out of the results. Thus a correlation exists between the percentage of area degraded in the Al metallization and the increase in R_{DSon} . This is really interesting as this relation can be used to define a better EoL criterion. Indeed, as explained before, the EoL criterion defined with an increase in V_f of 1% is not adapted to our module and seems to be too severe. For example, some devices which had reached an increase in V_f greater than 1% were still electrically functional and did not show critical degradations inside the package. So in order to be able to determine a more appropriate criterion, a correlation between a parameter continuously monitored during the test (V_f or ΔT_j) and a parameter indicating the amount of degradations in the module has to be found. As a correlation exists between the increase in R_{DSon} and the percentage of area degraded in the Al metallization, the increase in R_{DSon} can be taken as a parameter indicating the amount of degradations in the module. This is very interesting as the R_{DSon} was always measured at the end of tests thus a high amount of data is available, whereas the degraded surface in Al metallization was not always measured. And even more important, it means that we have now a non destructive method to determine the amount of degradations in the module, simply by measuring the R_{DSon} . This is quite advantageous.

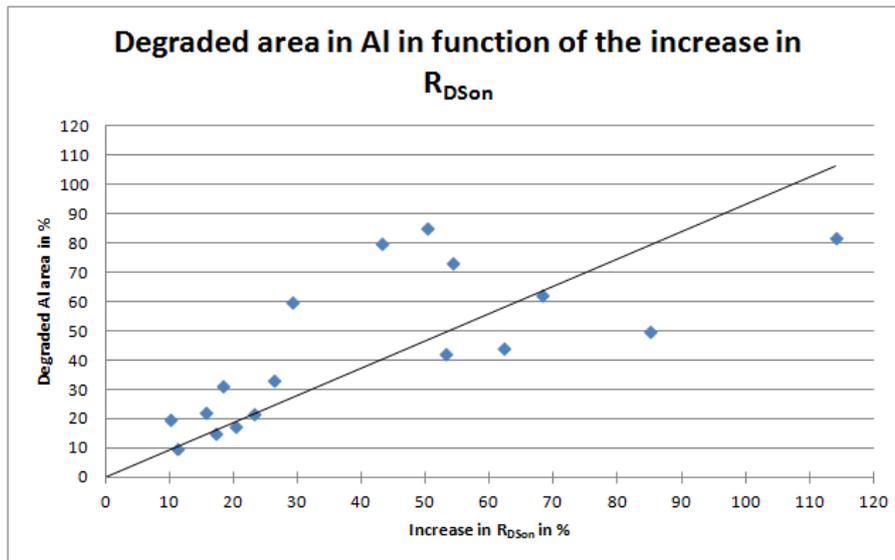


Figure 4.41: Percentage of degraded area in the Al metallization versus the increase in R_{DSon}

Then as the R_{DSon} was not continuously measured during our tests, a correlation has to be found between the increase in V_f and the increase in R_{DSon} . The increase in V_f in function of the increase in R_{DSon} is plotted Figure 4.42. Results are quite scattered, thus the correlation between the increase in V_f and R_{DSon} is not really good. The poor quality of this correlation suggests that an optimization of our test method could be to regularly measure the R_{DSon} in good thermal conditions during the tests. Thus the R_{DSon} could be directly used to define an EoL criterion. Despite the poor quality of the correlation between the increase in R_{DSon} and V_f , this one will still be used to define a new EoL criterion.

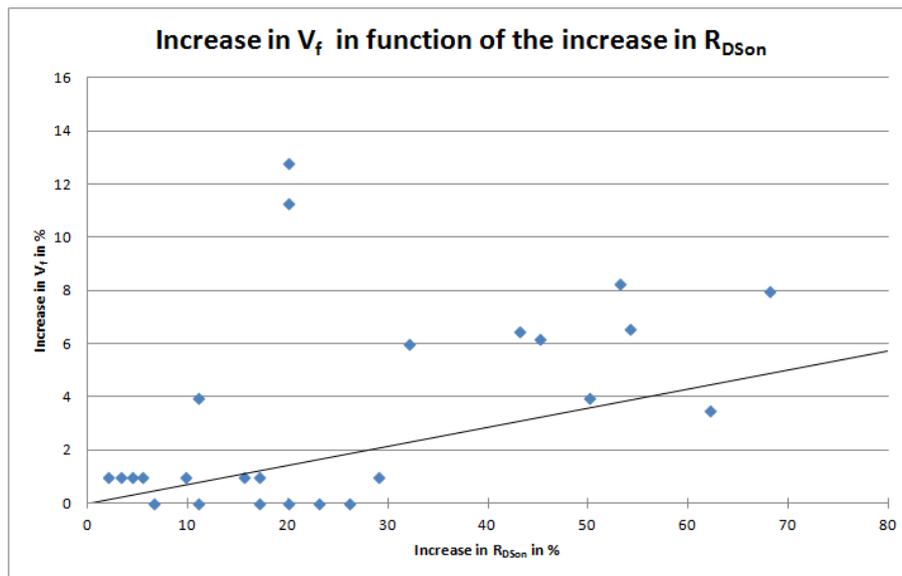


Figure 4.42: The increase in V_f versus the increase in R_{DSon}

4.3.3 Improved lifetime prediction

In a first approach an acceptable limit of degradation in our module is a degraded area of 40% in the Al metallization. Indeed, tested modules which had such a degraded area in the Al were still electrically functional. This 40% of degraded area is correlated to an increase in R_{DSon} of about 40% (Figure 4.41), itself correlated to an increase of 3% in V_f (Figure 4.42). So a first suggestion for a more appropriate EoL criterion could be an increase in V_f of 3%. A better adjusted EoL criterion can certainly be found by performing some more experiments and by regularly measuring the R_{DSon} . But this is already a first step in the determination of an appropriate EoL criterion for the B6 Bridge. The lifetime of modules tested was calculated based on the new EoL criterion and is plotted and compared to the lifetime based on the first EoL criterion in function of ΔT_j (Figure 4.43). Fewer results are obtained for the lifetime based on the new criterion as for some samples

the test was stopped before that an increase in V_f of 3% was observed. But this already gives an idea of the gain of lifetime with the new EoL criterion. And the gain of lifetime is non negligible as changing from an EoL criterion of an increase in V_f of 1% to an increase of 3% already double the lifetime prediction of the module. Finally the lifetime prediction based on the new EoL criterion is compared to the one based on the first criterion and to the literature data in function of ΔT_j (Figure 4.44). This shows again the gain of lifetime for the module with the new criterion and confirms the robustness of the module as its lifetime is competing with the best results from the literature.

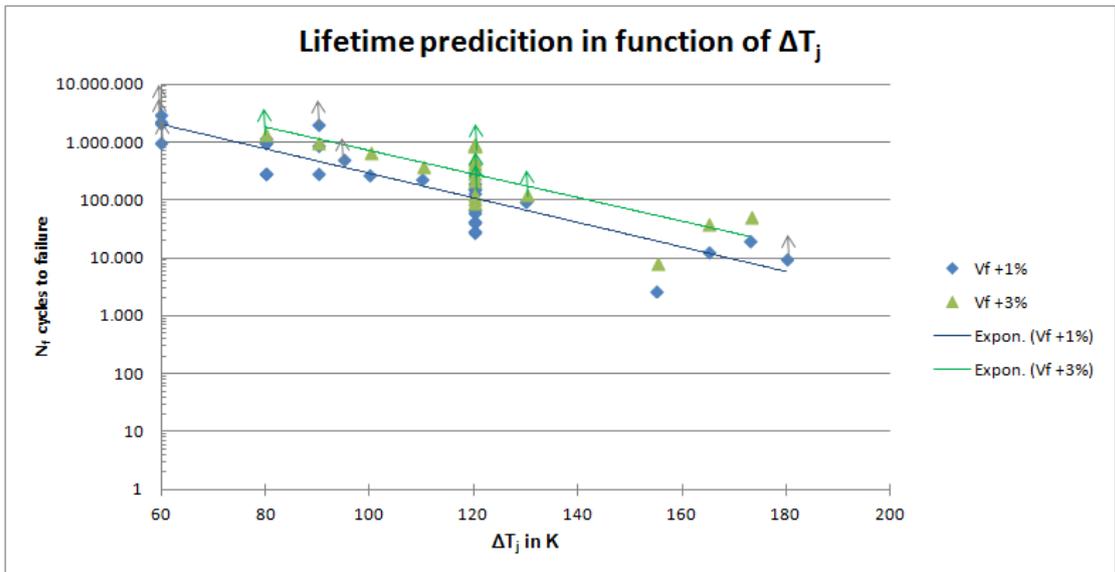


Figure 4.43: N_f cycles to failure in function of ΔT_j with EoL $V_f + 3\%$ and EoL $V_f + 1\%$

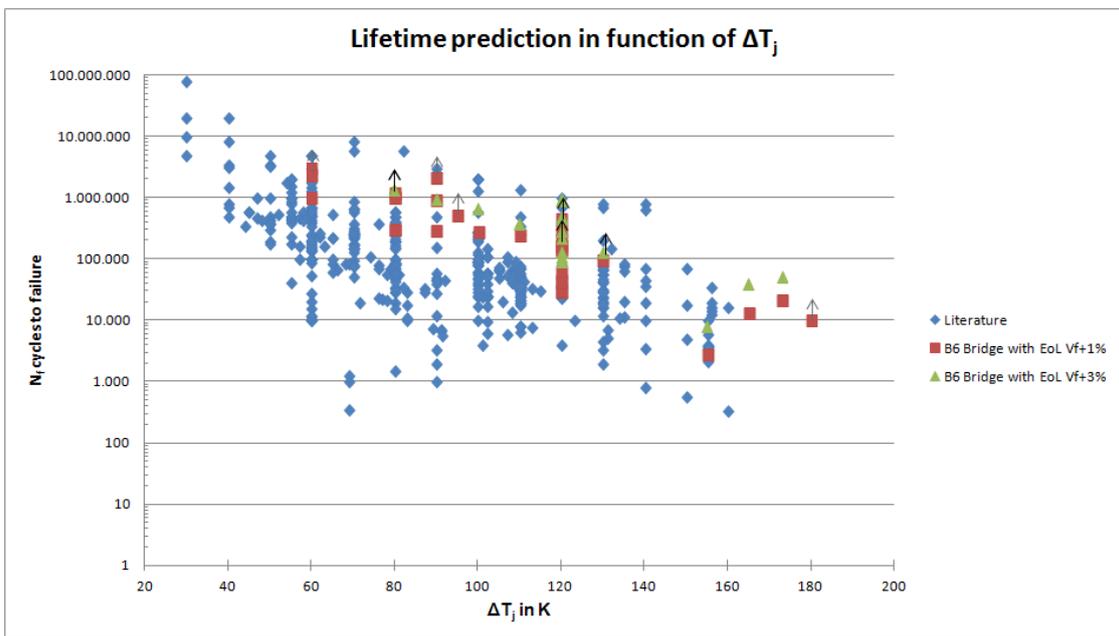


Figure 4.44: N_f cycles to failure in function of ΔT_j for the B6 Bridge with EoL $V_f + 3\%$ and $V_f + 1\%$ in comparison with number of cycles to failure from the literature

5 Thermo-mechanical simulations

As previously said, PTC is a test relatively easy to perform and also to simulate, and it can be taken as a reference to which APC can be compared to. Thus PTC was simulated to validate the 2D axisymmetrical model of one MOSFET structure in comparison to 3D models of the entire B6 Bridge, taken as references. The validation of the 2D model is done for PTC, as it is easier to simulate with large 3D models and required less calculation time than for APC.

Once the 2D model validated, the behavior of the module under PTC was analyzed in details based on the results of the 2D simulation. Then APC was simulated with the 2D model and results were analyzed in details and discussed in comparison with the results obtained for PTC. Finally a sensitivity study on test parameters is performed for APC.

5.1 Passive Temperature Cycling (PTC)

5.1.1 Loading conditions for PTC

PTC is simulated in Ansys by varying cyclically the temperature of the entire module. That for a static structural analysis is sufficient, no thermal-mechanical coupling are needed as the temperature is homogeneous in the entire module. A fixed point in the module as well as the temperature cycles have to be defined. Temperature cycles were defined to range from a cold temperature of -40°C to a hot temperature of 150°C , with dwell time and ramping time of 900s. For the comparison 2D/3D models, only a part of one temperature cycle is simulated after an initial cooling down from the reference temperature 175°C (defined in the chapter 2) to the room temperature 25°C . This was sufficient to validate the 2D model and it avoids long calculation times for 3D models (Figure 5.1). On the contrary 6 temperatures cycles were simulated after the initial cooling down to room temperature for the detailed analysis of the 2D model (Figure 5.2).

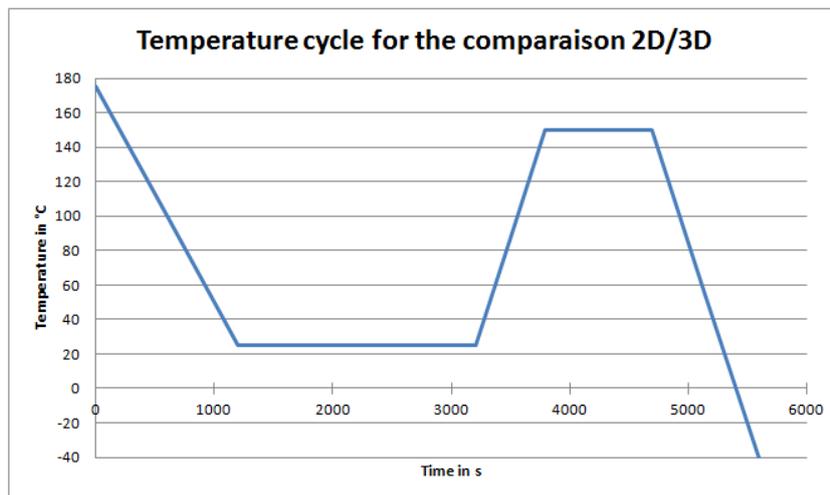


Figure 5.1: PTC for the comparison 2D/3D

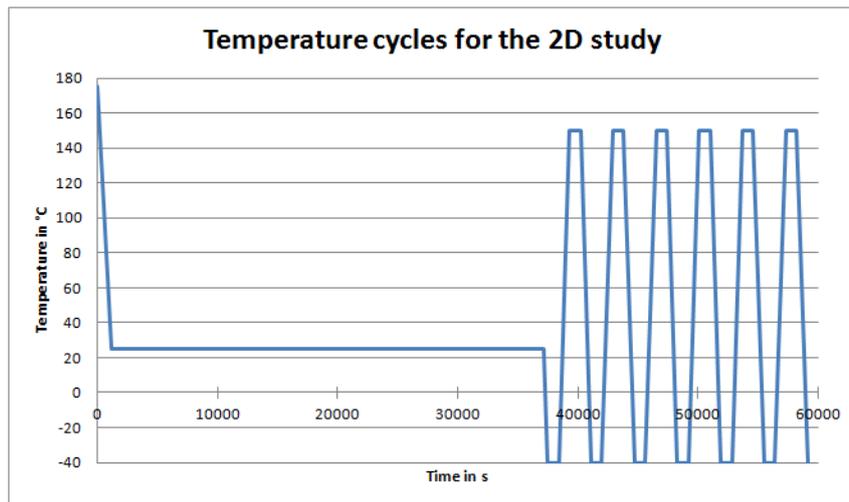


Figure 5.2: Temperature cycles for the 2D study

5.1.2 Comparison 2D/3D: validation of the 2D model

In this study, the goal is to precisely characterize the thermo-mechanical response of the stack of different materials that constitute the module. This includes also the study of the Al metallization and the IMCs, which are very thin layers. Conducting such a study on a large 3D model would be very difficult and time consuming. Indeed, modeling very thin layers in a large 3D model means difficulties for the meshing and results in a large and complex model that requires long calculation times for the simulation of several PTC or APC cycles. But when a sensitivity study has to be performed, simulations have to be relatively quick and easily reproducible. And this would not be the case with a large and complex 3D model. Thus a simplified model able to take into account thin layers and providing reliable results has to be developed. This corresponds in our case to a 2D axisymmetrical model of one MOSFET structure. As this model does not corresponds exactly to the real geometry of one MOSFET of the B6 Bridge, a validation was first done by comparing results obtained with the 2D model to the ones obtained for different cross-sections of a 3D model.

5.1.2.1 3D models

A 3D Finite Element (FE) model of the entire B6 Bridge is shown Figure 5.3. Only one MOSFET of the entire module is analyzed in details. A study has been previously done to determine which MOSFET of the module is the most damaged and thus representing the worst case. The study revealed that all MOSFETs have approximately the same behavior, but one had slightly more stress and strain than the others. This MOSFET is the one circled in red on the Figure 5.3 and was the one loaded in the experiments. Its mesh was then refined in comparison to the rest of the module. 3 different cross-sections of the 3D model were defined and compared to 2D, thus requiring 3 different 3D models with different meshes. All models had 3D tetrahedral structural solid elements with 10 nodes, called SOLID187 in Ansys. This type of element is well suited to mesh our model which was imported from a CAD program. These elements have 3 degrees of freedom at each node, which are the 3 translations in directions x, y, z, and are also compatible with plasticity, creep and large deflections which are required for our analysis.

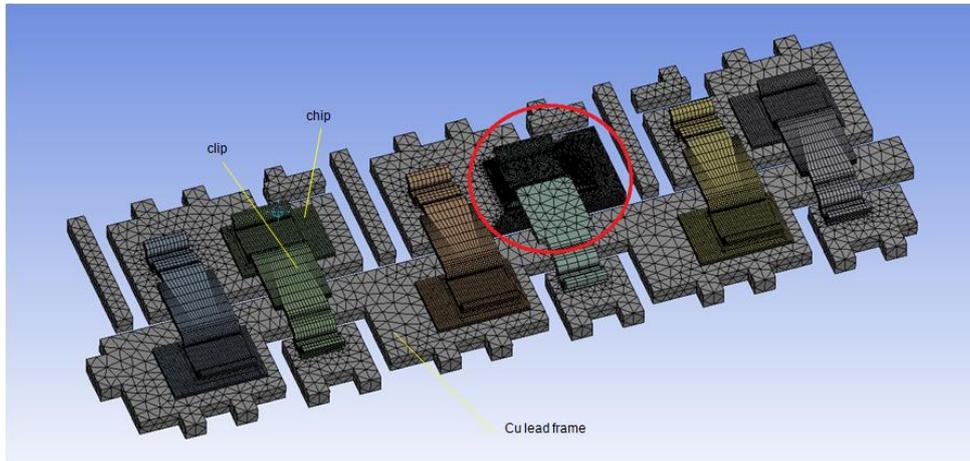


Figure 5.3: View of the mesh for a 3D model of the entire B6 Bridge with the hidden mold

The 3 cross-sections studied were:

- A cross-section along a straight line in the middle of the chip
- A cross-section along the chip diagonal
- A cross-section along the top solder diagonal

The mesh of these 3 cross-sections is shown on Figure 5.4 and the number of elements for each corresponding model is detailed [Yua13].

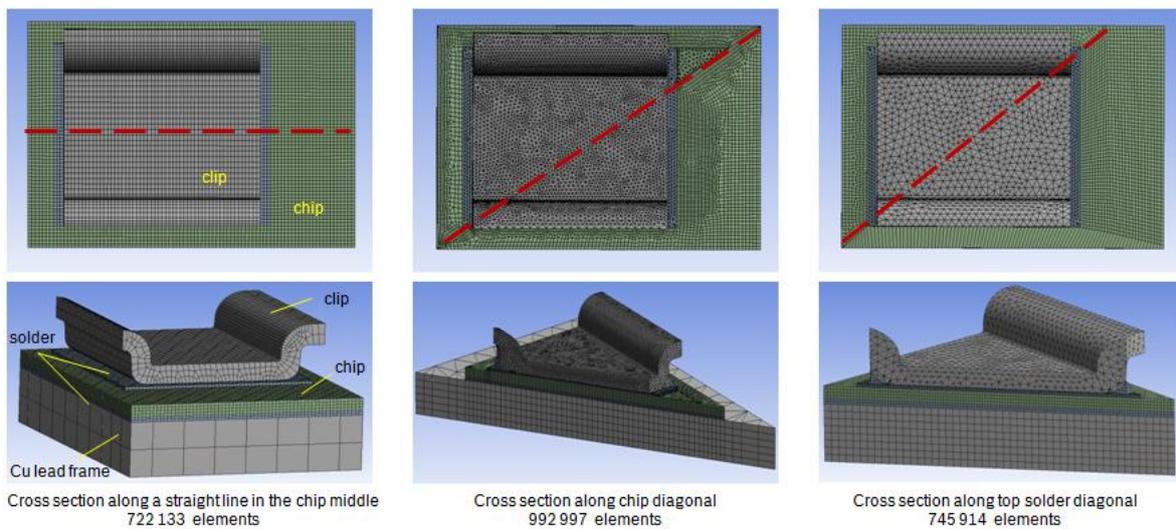


Figure 5.4: Views of the mesh of the 3 different cross-sections of one MOSFET

5.1.2.2 2D model

A 2D FE model has been created for a MOSFET structure with an axisymmetry condition. A MOSFET structure refers here to one chip and its close surrounding, which means its Cu lead frame, its solder layers, its Al metallization, its clip and the surrounding mold. Such a 2D axisymmetric model with chip-midpoint as symmetry axis is possible as the center of the chip is the neutral point (NP) in terms of thermal expansion. In this FE model, a fine mesh is defined using quadratic plane elements with 8 nodes, called PLANE183 in Ansys. These elements have 2 degrees of freedom at each node, which are the 2 translations in directions x and y, and are also compatible with plasticity, creep and large deflections which are required for our analysis.

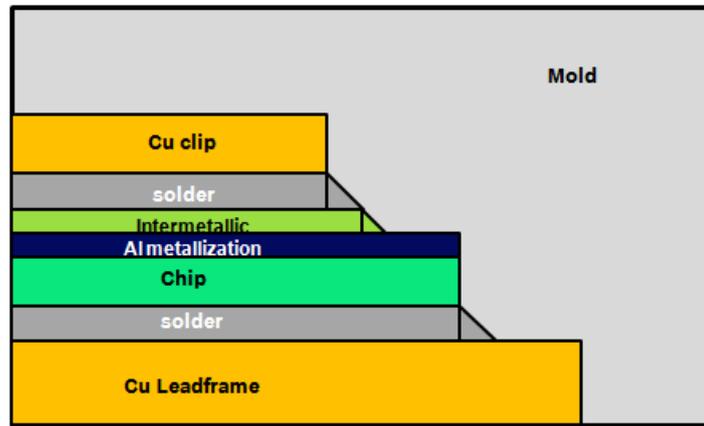


Figure 5.5: Schematic 2D section of the 2D model of one MOSFET structure

The model counts 44 775 elements. The thinnest layers have a minimum of 4 elements in their thicknesses, which means that the smallest elements have a size of about 1 μm . Attention was also paid to refine the mesh in the most critical areas of the module. Both solder layers have fine elements with an aspect ratio of 2,8 and critical areas of the metallization and the IMC layer have elements with an aspect ratio of 6,5, which guarantee reliable results. Some elements have a bigger aspect ratio, up to 35, but these elements are not located in critical areas and thus did neither affect the convergence nor results.

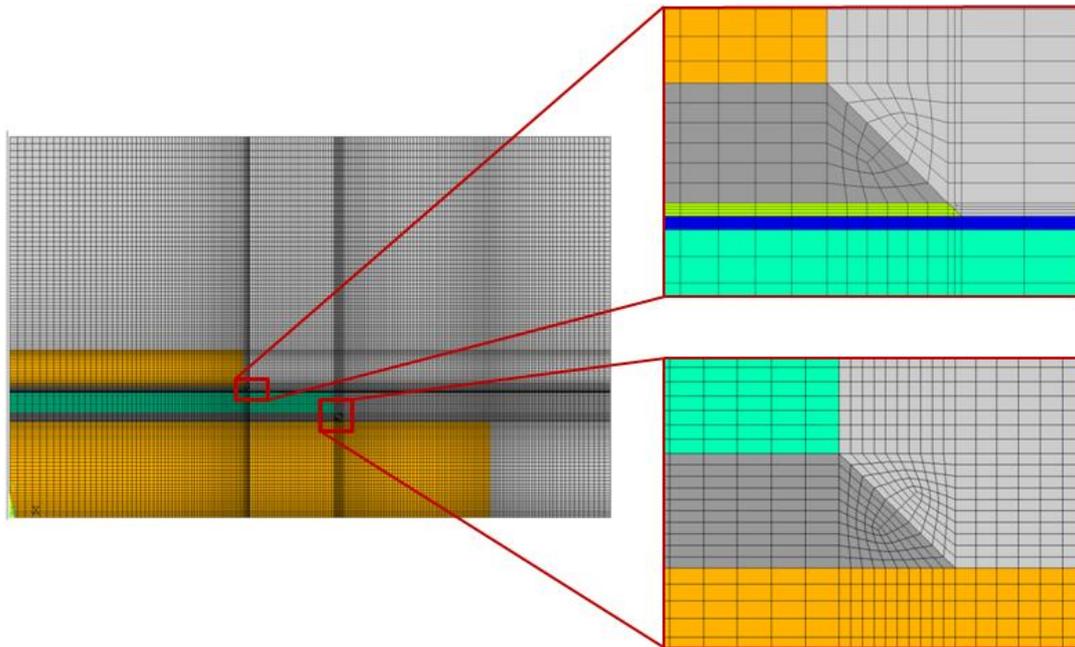


Figure 5.6: Global view of the mesh in the 2D model with zooms at both solders meniscus

5.1.2.3 Comparison 2D/3D

Results obtained with the 2D axisymmetric model are compared to the ones obtained for the 3 different cross-sections of the 3D model (chip middle, chip diagonal and top solder diagonal). Here, in-plane stresses in the chip and creep strains in both solders are analyzed in order to verify that the 2D model represents well the behavior of the module. First we look at the in-plane stress along a path defined in the middle of the chip thickness and running from its center to one extremity of the layer. Thus for the 3D models, 2 paths are defined per cross-section, one for the left side and one for the right side. The in-plane stresses along all paths of 2D and 3D models at -40°C and 150°C are plotted Figure 5.7. One can see that all curves are following the same trend and are reaching very similar stress values for both temperatures. Paths do not have always the same length, as cross-sections are different. Sometimes quite high values are reached at the end of the path, which corresponds to the layer extremity. These high values may be induced by the material interface. One curve named “solder diagonal left” has a slightly different profile: an abrupt decrease in stress appears before

the final stress increase until reaching the extremity of the layer. This comes again from the different geometries of cross-sections. Here the cross-section passes through the top solder meniscus, and ended in the corner of the chip. The decrease occurs in the area where the cross-section cut the top solder meniscus. Except this slightly different curve, one can conclude that the 2D model represents well the in-plane stress state in the chip. The cross-section the best represented by the 2D model is the cross-section through the chip diagonal, as their results are very close.

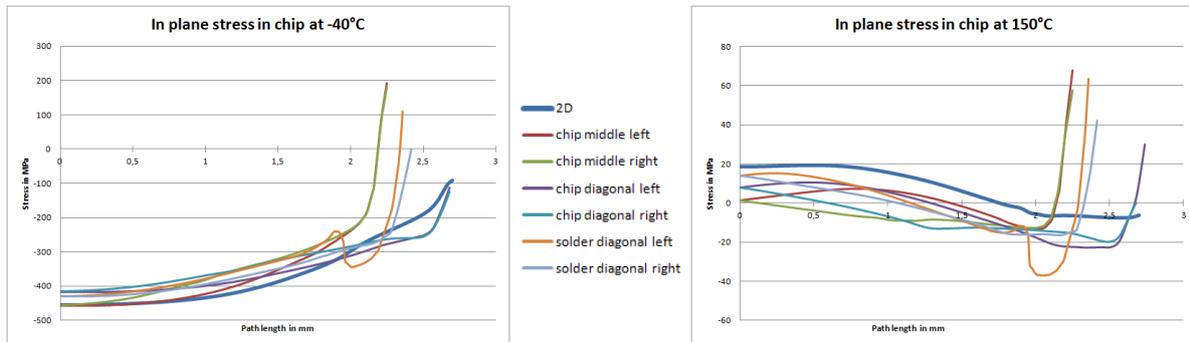


Figure 5.7: Comparison of in-plane stresses along paths in chip for 2D and 3D models. On the left at -40°C and on the right at 150°C .

Then creep strains of both solder layers are analyzed (Figure 5.8). A path is defined in both solders: for the bottom solder the path is at $1/8$ of its thickness beneath the chip, and for the top solder the path is at $1/8$ of its thickness above the chip. Both paths are running from the center of the cross-section to one extremity.

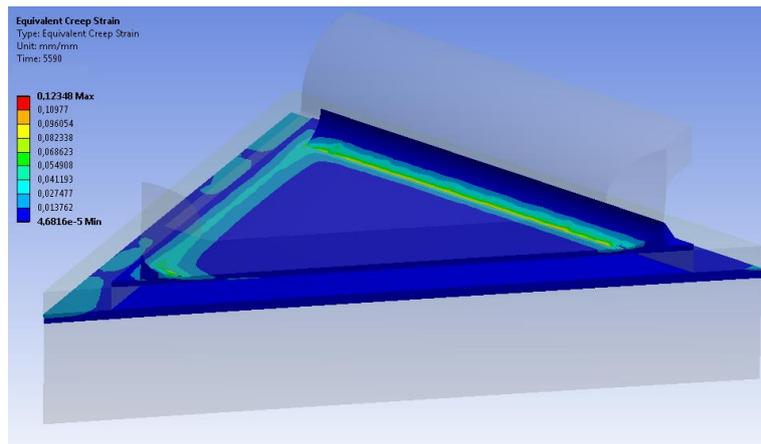


Figure 5.8: Creep strain in the bottom and the top solders of the cross-section through the top solder diagonal at -40°C

The creep strain in the bottom solder along paths of the different models is plotted Figure 5.9 at low and high temperatures. Here also paths have different lengths due to the different cross-sections. All curves are evolving in the same domain, but the creep strain of the 2D model has a slightly different trend line. This can be explained by the fact that the bottom solder layer is not modeled the same way in 2D and in 3D. In 3D the bottom solder is modeled as a quadratic element without meniscus, whereas in 2D the meniscus is taken into account. Nevertheless values reached for all paths are similar, and for all of them it is the extremity of the path which suffers the most from creep strain. Here also it seems like the cross-section through the chip diagonal is the cross-section the best represented by the 2D model.

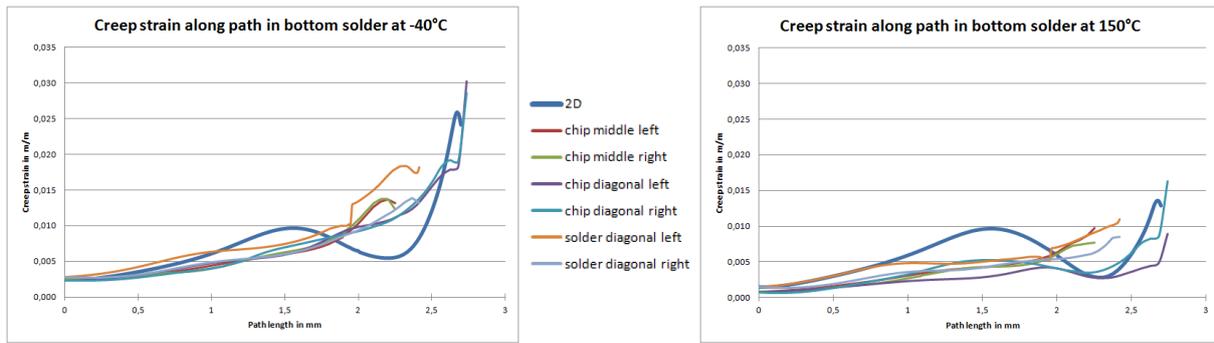


Figure 5.9: Comparison of creep strain along paths in the bottom solder for 2D and 3D models. On the left at -40°C and on the right at 150°C .

The same curves are plotted for the top solder Figure 5.10. Here more differences are visible between the different models. This comes from the way with which the top solder layer was cut by the cross-section. For the cross-section through the chip diagonal, on one side (left) the cross-section passes through the top solder meniscus, while on the other side (right) it does not. This is creating asymmetrical behavior for the 2 paths of one cross-section. Then the solder meniscus is not always located at the same distance to the center depending on the cross-section, thus peaks of creep strain are occurring at different path lengths on the graphic. Here there are also some differences in trend lines between 2D and 3D as the geometry of the top solder is simplified in 2D. Indeed, in 2D there is no Cu clip with a complex form, it is only a quadratic element, and thus the geometry of the top solder is also simple. It does not follow the form of the Cu clip as in 3D models. Despite all these differences, the creep strain reached in 2D stays in the same order of magnitude as the values reached with 3D, and the path extremity is the most critical zone for all models.

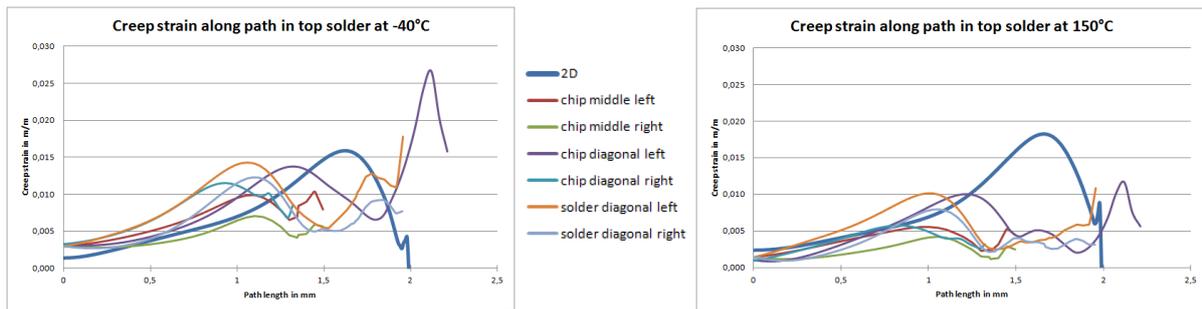


Figure 5.10: Comparison of creep strain along paths in the top solder for 2D and 3D models. On the left at -40°C and on the right at 150°C .

Finally the accumulated (acc) creep strain for both solders is calculated by averaging the 10% of paths extremities, and is plotted Figure 5.11. Concerning the acc creep strain in the bottom solder results are quite different from one model to another. The percentage of acc creep strain reached after the first temperature change is quite different depending on the model, but at the end, almost all results are converging to a similar amount of acc creep strain: 1,8%. The 2D model reaches also the 1,8% of acc creep strain and have the second highest plateau at constant temperature. Thus the amount of acc creep strain in the bottom solder will not be underestimated by the 2D model. Results obtained for the 2D model are close to the ones from the cross-section through the chip diagonal.

Regarding the acc creep strain in the top solder, results are not as scattered as for the bottom solder. Curves from the different models are parallel to each other, and at the end almost all curves are tending to reach a value around 1% of acc creep strain. The 2D model also reaches around 1% of acc creep strain and has the second highest plateau at constant temperature. Thus, for the top solder also there is no risk that the 2D model underestimates the creep strain. The curve of the 2D model is included between both curves of the cross-section through the chip diagonal.

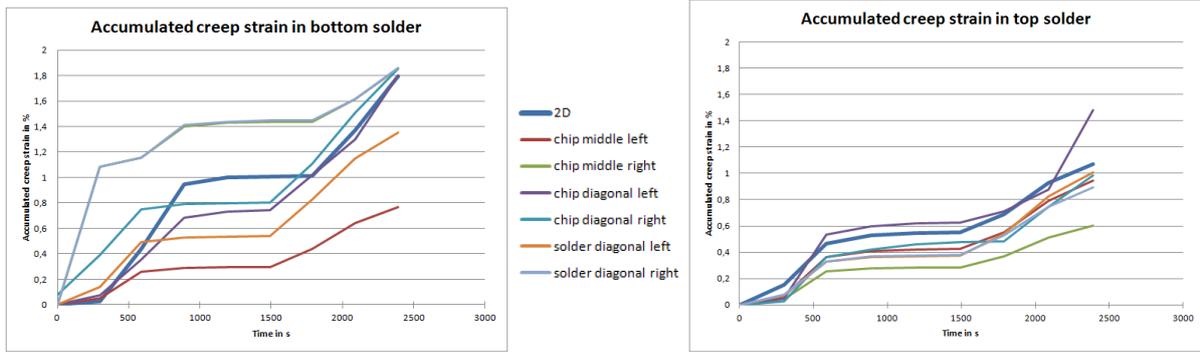


Figure 5.11: Comparison of acc creep strain for 2D and 3D models. On the left for the bottom solder and on the right for the top solder.

To sum up this comparative study between 2D and 3D models, it can be stated that the 2D model provides results that correspond to the ones obtained with 3D model. The cross-section through the chip diagonal is the one that is the best represented by the 2D model. Thus, the 2D model can be further used in our study.

5.1.3 Detailed module behavior under PTC

5.1.3.1 Module behavior

The general behavior of the MOSFET structure is shown on Figure 5.12. At low temperature (here -40°C) and after cycling, a bending of the module and a shrinkage of the mold are observed. The bending of the module is relatively low as the thick Cu lead frame limits this deformation. The chip is entirely submitted to in-plane compression, while the Al metallization, the solder layers, the Cu clip and the lead frame are submitted to tensile stresses. At high temperature (here 150°C) and after cycling, the structure is bended in the other direction than at low temperatures. The chip is under tension whereas the rest of the structure has an in-plane stress close to zero. There is only the Al metallization which is significantly under compression and the IMC which is significantly under tension. Thus this area at the interface Al metallization/IMC may be critical. Because of the mold that compresses the whole assembly together, out-of-plane stresses are almost inexistent in the module. Shear stresses appear to be also limited in the entire MOSFET structure.

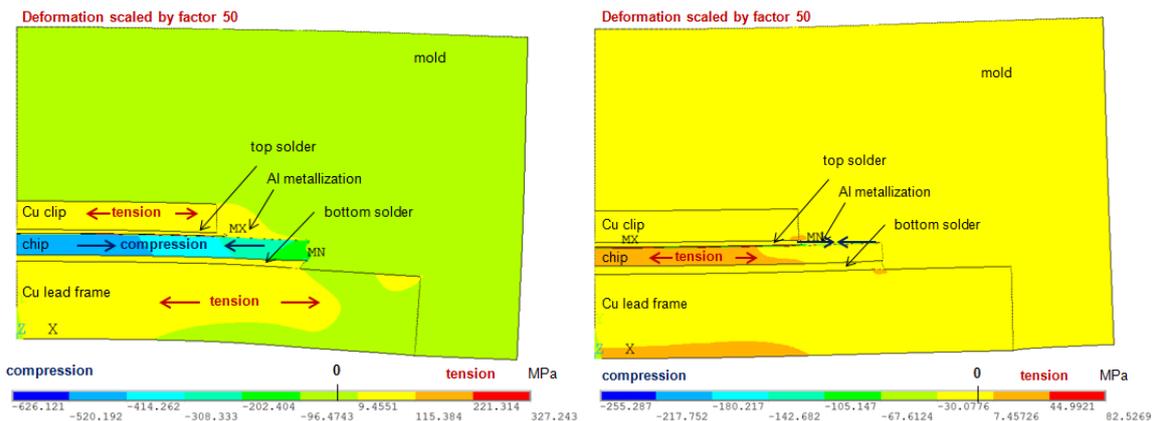


Figure 5.12: In-plane stress in the MOSFET structure at -40°C on the left and 150°C on the right

Paths were defined in several important layers of the structure:

- In the bottom solder: the path is defined at 1/8 of its thickness, close to the chip, to be able to look at the evolution of creep.
- In the chip: the path is defined in the middle of the chip thickness, to be able to look at the warpage and observe the evolution of stresses.
- In the Al metallization: the path is defined in the middle of the Al metallization thickness, to be able to observe the evolution of stresses and plastic strain in function of the position in Al.

- In the IMC: the path is defined in the middle of the IMC thickness, to be able to observe the evolution of stresses.
- In the top solder: 2 paths are defined, one at 1/8 of its thickness, close to the chip, and one at 7/8 of its thickness, close to the clip, to be able to look at the evolution of creep.

Paths were always defined from a point on the axis of symmetry to a point at the extremity of the layer. Paths in solder layers were defined at specific height corresponding to locations where cracks are frequently occurring after cycling. The analysis of stresses and strains in the different layers was always done for the last cycle (6th cycle) as the system begins to be stabilized.

5.1.3.2 Chip behavior

The warpage corresponds to the deformation in the out-of-plane direction along the path in the chip. As seen on the previous figure, at low temperatures the structure is bended down whereas at high temperatures the structure is bended over. The radius of curvature and its inverse value are calculated, thus giving us a quantitative value on the warpage amplitude (Table 5.1). A negative value corresponds to a bending down whereas a positive value stands for bending over.

warpage	-40°C	150°C
Radius of curvature R in m	-3,79	3,52
Inverse of radius of curvature 1/R in 1/m	-0,26	0,28

Table 5.1: Values of radius of curvature and its inverse value for PTC

The in-plane stress along the path in chip is plotted Figure 5.13. At low temperature the in-plane stress is negative, this meaning that the chip is under compression. The maximum of compressive stress is reached at the center of the chip, on the symmetry axis. At high temperature, the chip is under tensile stress. At the center of the chip the stress reaches its maximum while at the end of the path, there is almost no stress or a slight compression. So here, the in-plane stress maximum and thus critical point is located on the symmetry axis. The values of stress reached are not critical, as it is known from Bosch experience that a chip can endure 900MPa of in-plane compressive stress without being damaged.

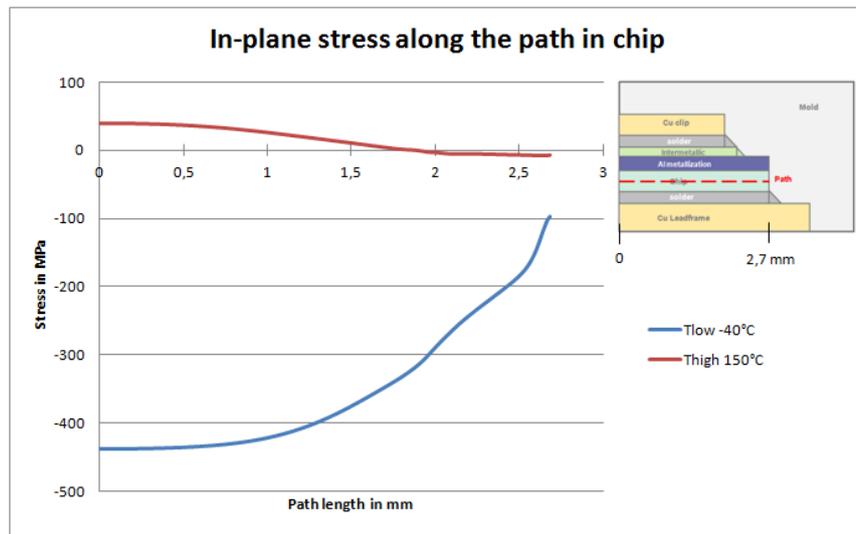


Figure 5.13: In-plane stress along the path in chip for low and high temperatures

As said before, the out-of-plane stress and the shear stress are almost inexistent in the module, and so it is also in the chip. The maximum of out-of-plane stress in the chip is reached at the chip extremity, at the interface with mold and the maximum of shear stress is also reached at the chip extremity but close to the interface with the bottom solder meniscus (Figure 5.14). It is important to study these values of stress reached at these locations as it can influence the growth of a crack induced in the chip by sawing. We looked at the maximum of out-of-plane stress in one cycle at the critical area at the interface with mold.

The maximum out-of-plane stress reached is 95 MPa. This value is not critical as it is known from Bosch experience that such out-of-plane stress at the interface chip-mold is critical when reaching about 200 MPa. The maximum of shear stress in the chip close to the bottom solder meniscus is also taken into account, and reaches a value of 87 MPa. Here it is more difficult to evaluate if the shear stress is critical, as no references are known.

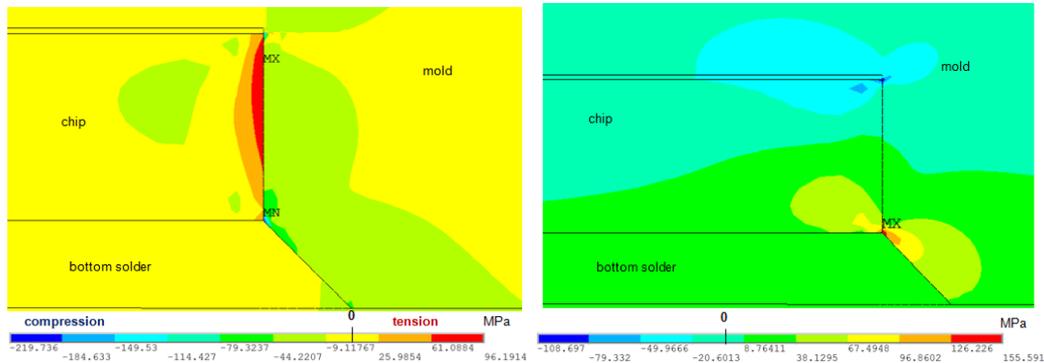


Figure 5.14: On the left, the out-of-plane stress at -40°C at the interface chip-mold. On the right, the shear stress at -40°C at the interface chip/bottom solder meniscus.

5.1.3.3 Bottom solder behavior

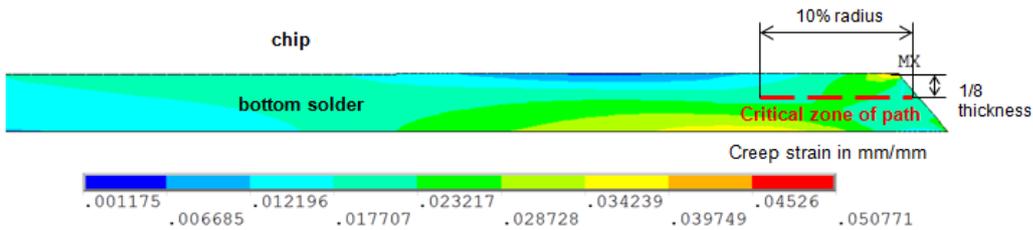


Figure 5.15: Creep strain at high temperature in the bottom solder

Solder are mainly subjected to creep strain, thus it is our center of interest. As can be seen on Figure 5.15 the critical zone for creep strain is at the extremity of the bottom solder, in the area of the meniscus and close to the chip. The path was defined at the height of $1/8$ of the bottom solder thickness, close to the chip, as it corresponds to the location where cracks were found to occur for standard modules. This definition was transferred for our module. A relevant creep parameter to analyze is the acc creep strain during one cycle. This is calculated by averaging the creep strain along the path. So the relevant width of the path in terms of creep strain has to be determined. The averaged creep strain and the acc creep strain during the 6 cycles were calculated for several different widths of path ranging from 20% to 5% of the bottom solder radius. The creep strain is plotted Figure 5.16 and it appears that all curves are parallel to each other. For the acc creep strain plotted Figure 5.17, results are proportional. Thus a radius of 10% was taken, as a crack in the solder with such a length would represents 20% of degradation in the thermal path, which begins to be critical. By calculating the acc creep strain per cycles for the 10% radius path, one can see that the system needs about 4 cycles to be stabilized.

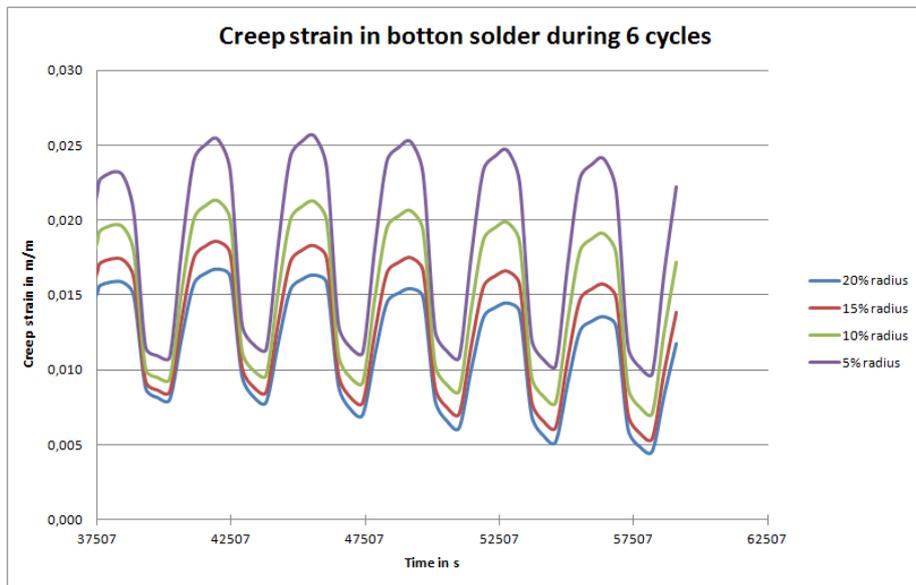


Figure 5.16: Creep strain in the bottom solder during 6 cycles

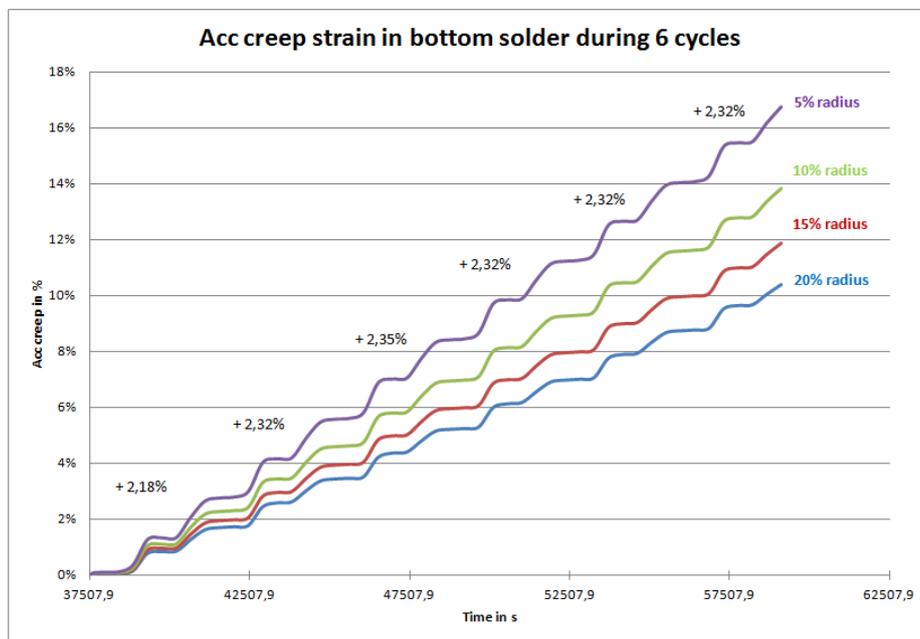


Figure 5.17: Acc creep strain in the bottom solder during 6 cycles

Finally, the evolution of temperature, von Mises stress and acc creep strain in one cycle at the critical area of the bottom solder is plotted Figure 5.18. The initial von Mises stress value originates from the initial conditions: a 175°C stress free temperature is defined and the module is cooled down to room temperature. This gives the frozen internal stresses within the package. Then, when the system heats up, these inner stresses decrease and reach a minimum value. By continuing heating up, the stress changes its direction thus the von Mises stress increases. Then the temperature stays constant, and we observe a stress relaxation. By starting the cooling phase, the stress reaches a minimum value and increase by decreasing temperature. The acc creep strain follows the temperature changes. At constant temperature the creep strain remains constant as well. Thus ramping times are more critical for the solder than dwell times. The accumulation of creep strain is equivalent for heating phase and cooling phase.

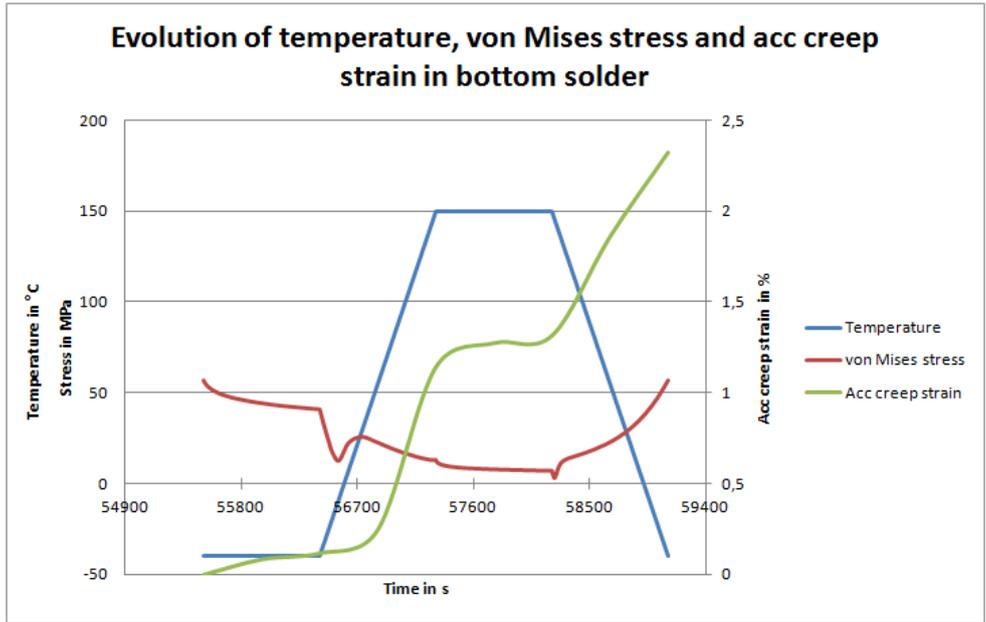


Figure 5.18: Evolution of temperature, von Mises stress and acc creep strain in the critical zone of the bottom solder during one cycle

In 1 cycle the bottom solder already accumulates 2,3% of creep strain, which is important. [Schu03] proposed a creep strain based fatigue lifetime model for SnAgCu solders with high Ag content based on FE simulation results and actual reliability test data from different types of assemblies such as Flip-Chip-On-Board (FCOB) and Plastic Ball Grid Array (PBGA) under different PTC conditions:

$$N_f = 4,5 \cdot (\epsilon_{acc\ creep})^{-1,295} \tag{Eq. 5.1}$$

Where N_f is the number of cycles to failure and $\epsilon_{acc\ creep}$ the acc creep strain in 1 cycle. This lifetime model cannot be directly transferred to our module with double sided soldered chip, but can still be used for relative comparison. Thus in our case, with 2,3% of acc creep strain, the bottom solder would be degraded already after 595 cycles. In comparison it should be reminded that a power module is expected to endure about 2000 cycles with temperature changes from -40°C to 150°C. Thus it can be stated that the amount of creep strain reached in the bottom solder is critical and will constitute the main cause for failure of the device.

5.1.3.4 Top solder behavior

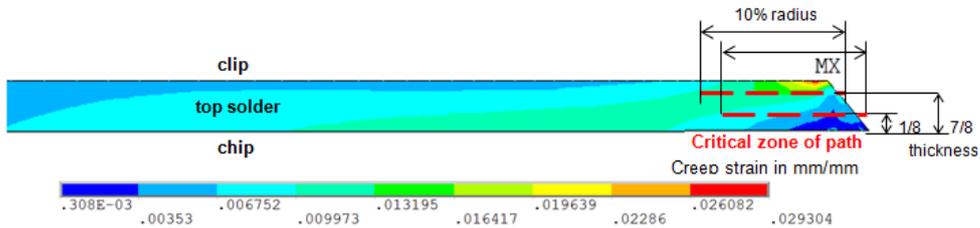


Figure 5.19: Creep strain at high temperature in the top solder

For the top solder, the same analysis is made as for the bottom solder, with the small difference that 2 paths were defined (Figure 5.19). One path is defined at 1/8 of the thickness, close to the chip, as it is the reflected equivalent to the path defined in the bottom solder and another path is defined at 7/8 of the thickness, close to the clip as the maximum of creep strain is to be seen in this region. Here also the relevant width of both paths in terms of creep strain has to be determined. So for both paths, the averaged creep strain and the acc creep strain during the 6 cycles were calculated with different path widths ranging from 20% to 5% of the top solder radius (Figure 5.20 and Figure 5.21).

Resulting curves are proportional, thus we decided to take a radius of 10% for both paths, by analogy with what was done for the bottom solder. By calculating the acc creep strain per cycles for both 10% radius paths, one can see that the system needs about 5 cycles to be stabilized.

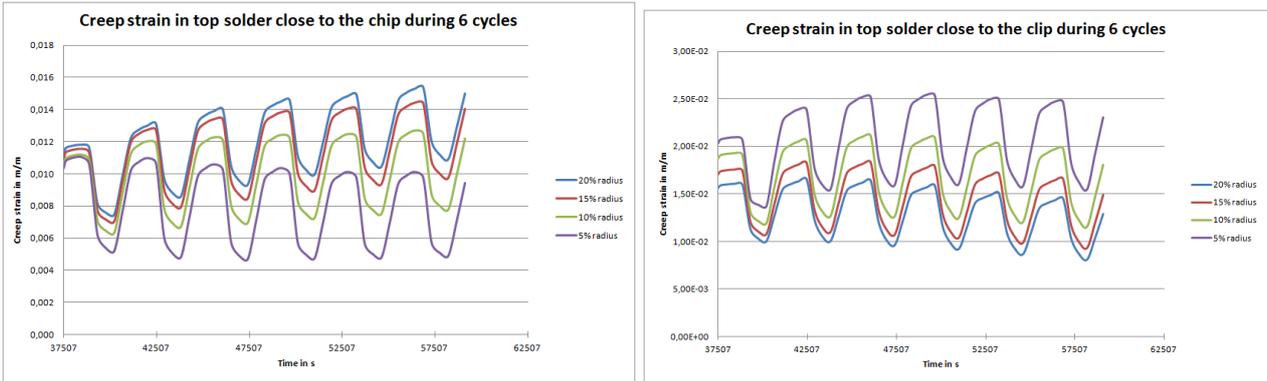


Figure 5.20: Creep strain in the top solder during 6 cycles. On the left, the creep strain is averaged for the path close to the chip and on the right for the path close to the clip.

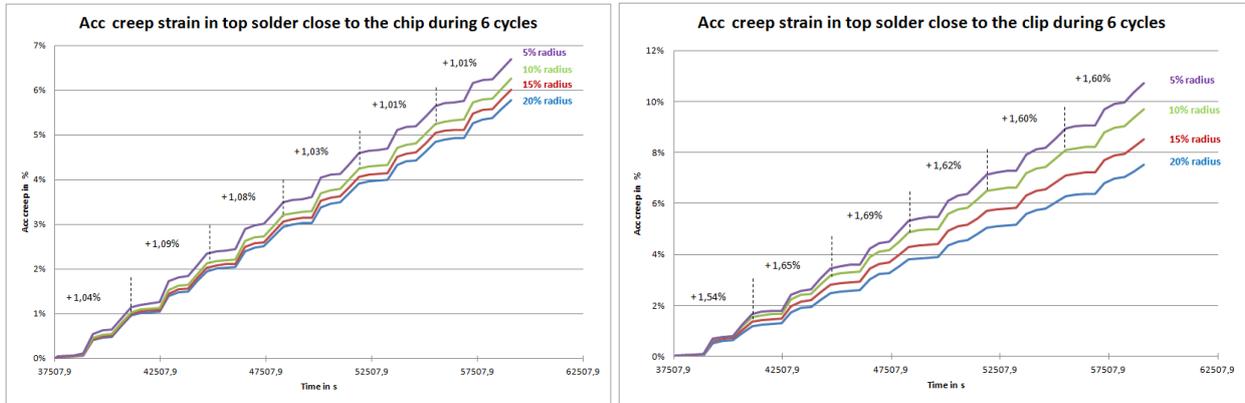


Figure 5.21: Acc creep strain in the top solder during 6 cycles. On the left, the acc creep strain for the path close to the chip and on the right for the path close to the clip.

Then the acc creep strain during one cycle is calculated and plotted Figure 5.22 for both paths. For the path close to the chip, the acc creep strain reaches 1,1% in one cycle, whereas the path close to the clip reaches 1,7%. So the top solder suffers less from creep than the bottom solder, thus more damages are expected in the bottom solder than in the top solder. Nevertheless, the acc creep strain in the top solder already surpasses 1%, thus giving a lifetime ranging from 880 to 1547 cycles according to [Schu03].

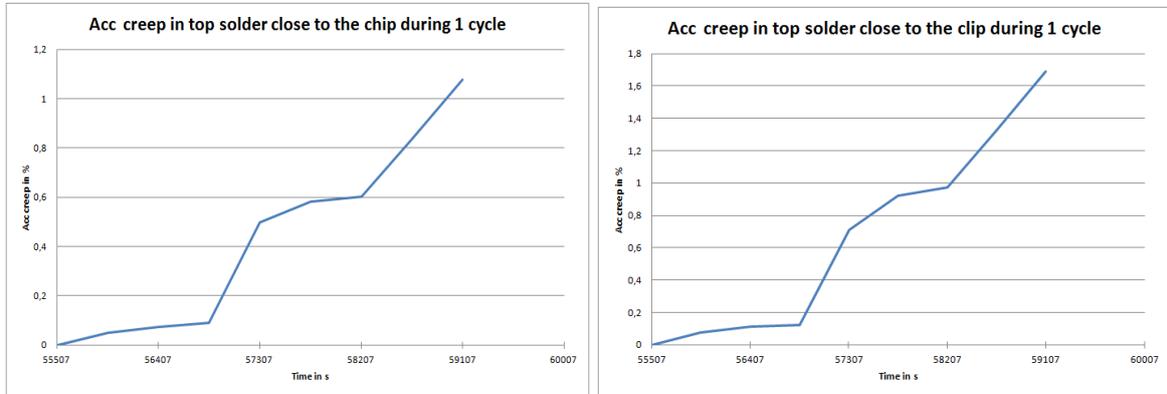


Figure 5.22: Acc creep strain in the top solder during one cycle. On the left, the acc creep strain for the path close to the chip and on the right for the path close to the clip.

5.1.3.5 Al metallization behavior

The von Mises stress along the path in the Al metallization is plotted Figure 5.23. The von Mises stress has a constant value of 82,5MPa along the path length at low temperature, whereas it has a constant value of 71,6MPa at high temperature. A small irregularity appears for both temperatures at about 2 mm, which corresponds to the area beneath the top solder meniscus. The von Mises stress is critical as the yield stress is reached, giving rise to plastic strain.

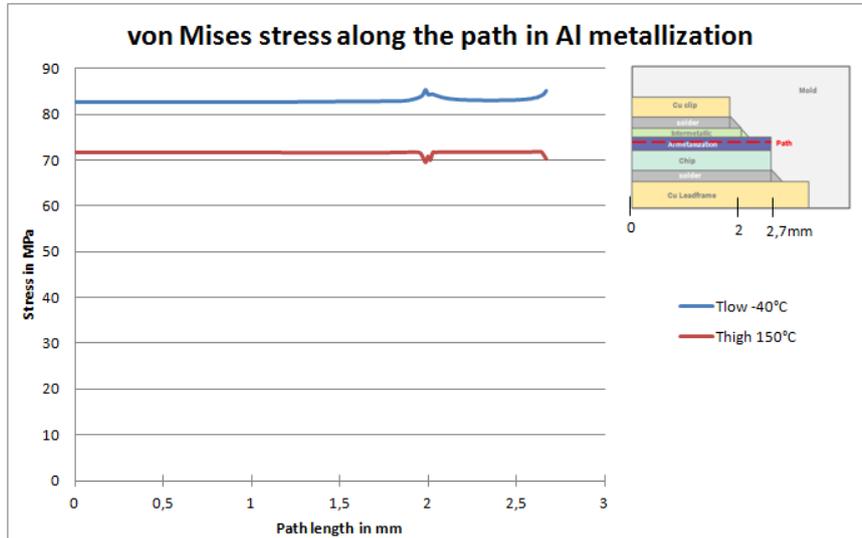


Figure 5.23: von Mises stress along the path in the Al metallization

Then the in-plane stress is analyzed on the Figure 5.24. At high temperatures, the Al metallization is under compressive stress, whereas at low temperatures tensile stress is dominant. In compression the stress varies from -50 MPa to -80 MPa, and in tension it varies from 40 to 80 MPa. These values are close to the yield point. In tension and compression an irregularity also appears at the top solder meniscus area, pointing out the specificity of this area. Concerning the out-of-plane and the shear stress along the path in the Al metallization, both were close to zero. For both stresses, at low temperature a compression is observed up to -20 MPa, whereas at high temperature small tension up to 5 MPa is to be seen. Nevertheless for both stresses, a peak of stress occurs at 2 mm, which corresponds again to the top solder meniscus area. Thus it can be deduced from the stress analysis in the Al, that the area beneath the top solder meniscus seems to be critical, and that the von Mises stress is driven by the in-plane stress.

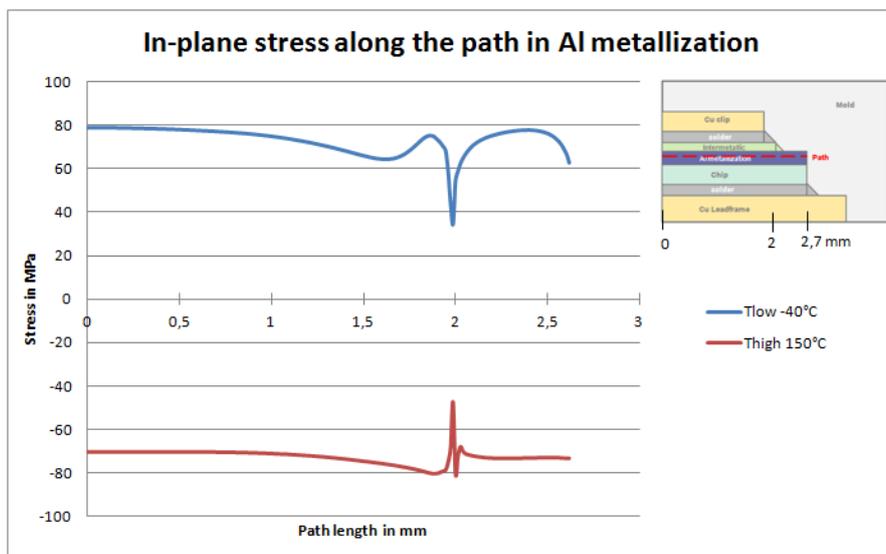


Figure 5.24: In-plane stress along the path in the Al metallization

Plastic strain curves along the Al path confirm the importance of the zone under the top solder meniscus, as a peak of plastic strain for both high and low temperatures is observed exactly at this position (Figure 5.25). To better analyze this plastic deformation, the accumulated (acc) plastic strain per cycle is calculated. This is done by averaging the plastic strain values obtained along the path in the area beneath the top solder meniscus. More precisely, the plastic strain average was calculated for the values obtained between 1,983mm to 1,993mm along the path in the Al. Then the acc plastic strain is plotted together with the temperature and the von Mises stress evolution (Figure 5.26). The evolution of the von Mises stress in Al follows the temperature changes. By heating or cooling down, the stress first decreases to reach a minimum value and then it increases until reaching the yield stress. By constant temperature, the von Mises stress remains constant as well. The acc plastic strain is also following the temperature changes and increases by heating or cooling down, and stays constant at constant temperature. More plastic strain is accumulated during cooling phase than during heating phase. The acc plastic strain in one cycle reaches the value of 0,7%. This is not a negligible value, but remains lower than the values observed for the acc creep strain of both solder layers.

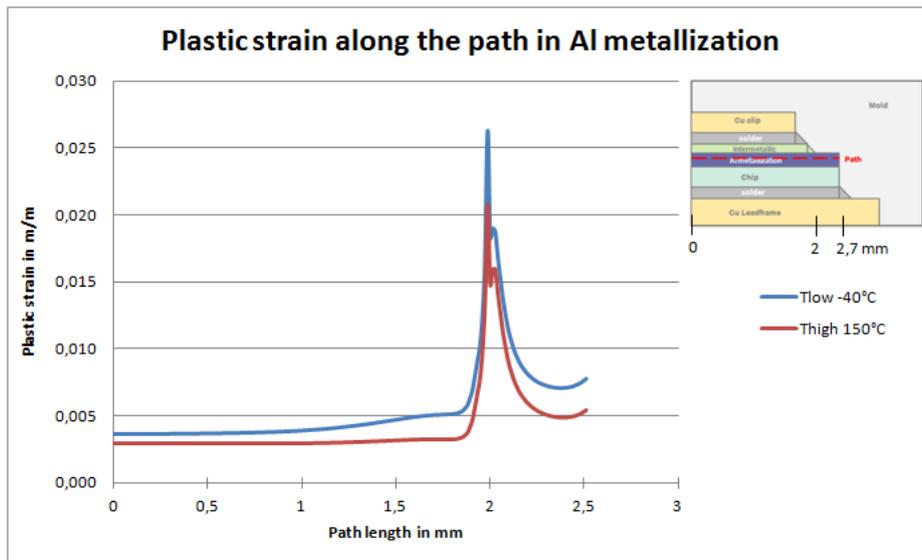


Figure 5.25: Plastic strain along the path in the Al metallization

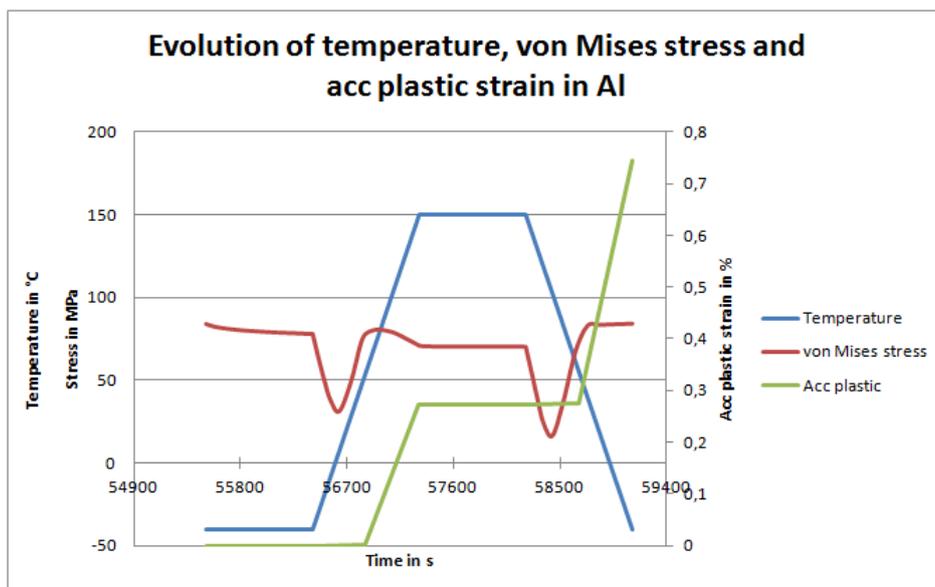


Figure 5.26: Evolution of temperature, von Mises stress and acc plastic strain in the Al metallization at the critical area beneath the top solder meniscus during 1 cycle

5.1.3.6 IMC behavior

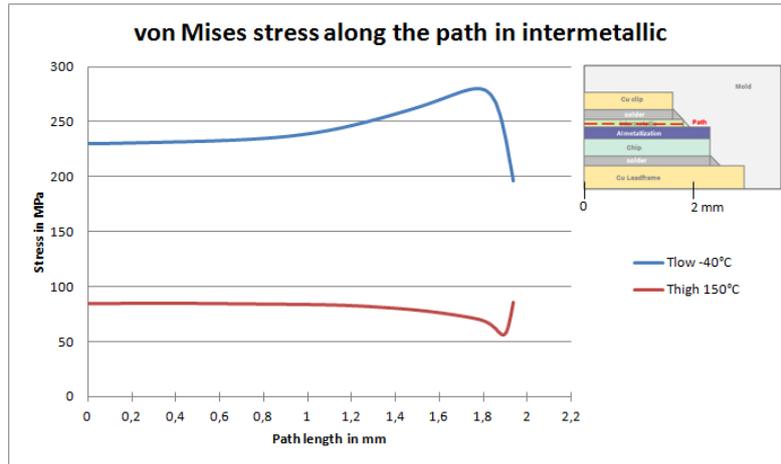


Figure 5.27: von Mises stress along the path in the IMC on top of the chip

The von Mises stress along the path in the intermetallic is plotted Figure 5.27. At low temperature the von Mises stress reaches 230 MPa and is constant along the first half of the layer close to the symmetry axis. Then, at about 1 mm, the stress increases and reaches a peak at the extremity of the layer before a final decrease. At high temperature, the von Mises stress reaches 84 MPa and is constant almost along the entire path. But close before reaching the extremity of the layer, a minimum stress is reached before a final increase. So the area close to the extremity of the IMC can be considered as the most critical area of the layer as the largest amplitude of von Mises stress are occurring. Here it is difficult to determine if the values reached are really critical for the layer, as no stress limits are known for the IMC.

The in-plane, out-of-plane and shear stresses in the IMC were also analyzed. The out-of-plane and shear stresses are close to zero for both high and low temperatures, but some maximum are also observed close to the extremity of the layer. The in-plane stress is very similar to the von Mises stress, as it is the stress component that drives the von Mises stress.

5.2 Active Power Cycling (APC)

5.2.1 Loading conditions for APC

To simulate APC, a coupled thermo-mechanical analysis is performed. This means that thermal results of the transient thermal simulation are imported as loads in the mechanical simulation. In the thermal analysis, the module is mounted onto a heat sink of aluminum with a constant temperature at its bottom line, corresponding to the desired T_{jmin} . Free convection and radiation of $10 \text{ W/m}^2\text{K}$ coming from the air are also taking place on the exterior surfaces of the module. During APC, the chip generates heat which is then dissipated in the entire module. In the mechanical analysis, the power module is not subjected to any pure mechanical loads, the module is only fixed at one point and loads are thermally induced. Three cycles are simulated after an initial cooling down from the stress free temperature of the module (175°C) to the ambient temperature (25°C) (Figure 5.28).

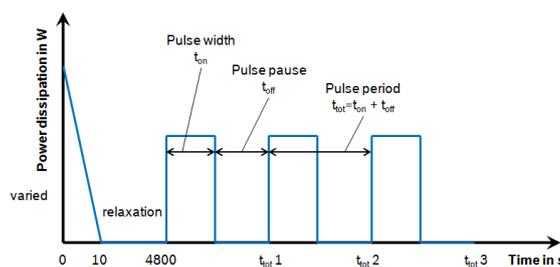


Figure 5.28: Schematic of the 3 APC cycles simulated

5.2.2 2D model

The simplified 2D axisymmetrical model of one MOSFET structure previously presented for PTC is also used here for APC simulations. It is possible to use this simplified model of only one MOSFET structure for APC simulations because MOSFETs included in the package are thermally decoupled, meaning that every MOSFET acts as a single one. The same fine mesh as for PTC simulations is used, but the type of elements is different as the type of analysis differs. For the thermal analysis, the elements used are quadratic plane elements PLANE77 with 8 nodes and the temperature as degree of freedom. Then, for the coupled static structural analysis plane elements PLANE 183 were used.

Another small difference is induced by the loading conditions required for APC. In the thermal analysis, 2 more bodies are defined: a Thermal Interface Material (TIM) and an aluminum heat sink located beneath the MOSFET structure. Those 2 bodies are defined to properly simulate the real cooling down conditions to which the module is submitted to. The TIM and the heat sink are then suppressed via the command “ekill” for the static structural analysis.

5.2.3 Detailed module behavior under APC

For APC, 36 different cases were simulated for the sensitivity study on test parameters. Here one case of the sensitivity study is taken as an example to explain the behavior of the module and its different layers. The case taken as an example is: $T_{jmin} = -40^{\circ}\text{C}$, $\Delta T_j = 120\text{K}$ and $t_{on} = 10\text{s}$. The analysis of stresses and strains in the different layers was always done for the last cycle (3rd cycle) as the system begins to be stabilized.

5.2.3.1 Module behavior

The general behavior of the MOSFET structure is shown on Figure 5.29. At low temperature (here -40°C) and after cycling, a bending of the module and a shrinkage of the mold are observed. The bending of the module is relatively low as the thick Cu lead frame limits this deformation. The chip is entirely submitted to in-plane compression, while the Al metallization, the solder layers, the Cu clip and lead frame are submitted to tensile stresses. At high temperature (here 80°C) and after cycling, the structure is bended in the other direction than at low temperatures. The chip is still under compression and the IMC under tension but the Al metallization turns out to be under compression. The rest of the structure has an in-plane stress close to zero, between -40 MPa to 50 MPa . So the area at the interface Al metallization/IMC may be critical as layers have opposite directions of stress. Because of the mold that compresses the whole assembly together, out-of-plane stresses are almost inexistent in the module. Shear stresses appear to be also limited in the entire MOSFET structure. So the MOSFET structure has the same behavior under APC as under PTC at the difference that even at high temperatures the chip remains under compression under APC.

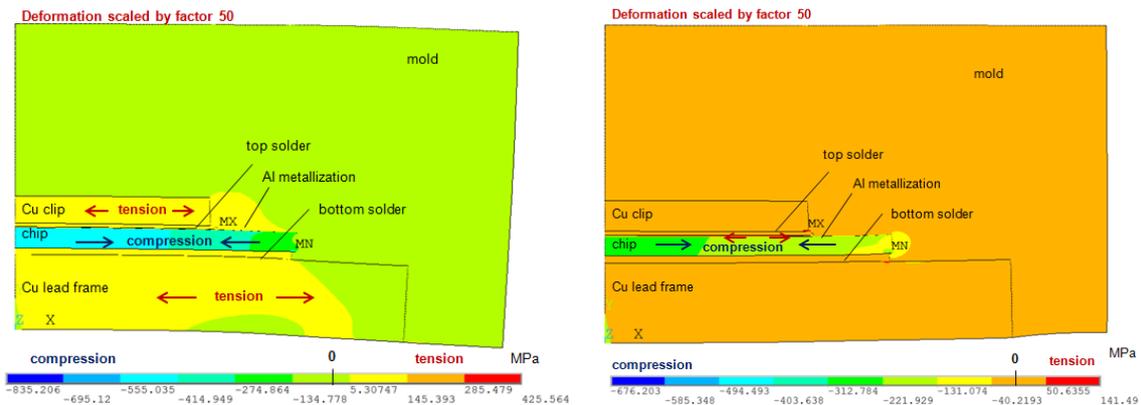


Figure 5.29: In-plane stress in the MOSFET structure at -40°C on the left and 80°C on the right

5.2.3.2 Chip behavior

As seen on the previous figure, at low temperatures the structure is bended down (-) whereas at high temperatures the structure is bended over (+). The radius of curvature and its inverse value are calculated, thus giving us a quantitative value on the warpage amplitude, which can be compared later for all the different cases of the sensitivity study (Table 5.2). Here the same bending directions are observed as for PTC but the structure is less bended.

warpage	-40°C	80°C
Radius of curvature R in m	-5,27	8,82
Inverse of radius of curvature 1/R in 1/m	-0,19	0,11

Table 5.2: Values of radius of curvature and its inverse value for APC

The in-plane stress along the path in chip is plotted Figure 5.30. For both low and high temperatures the chip is under compression and the maximum of compressive stress is reached at the center of the chip, on the symmetry axis. The intensity of compressive stress is higher for low temperatures. So here the in-plane stress maximum and thus critical point is located on the symmetry axis. The values of stress reached are not critical, as they remain under 900 MPa. The in-plane stresses in the chip under APC follow the same trend as for PTC but the difference is that at high temperature the chip remains under compression.

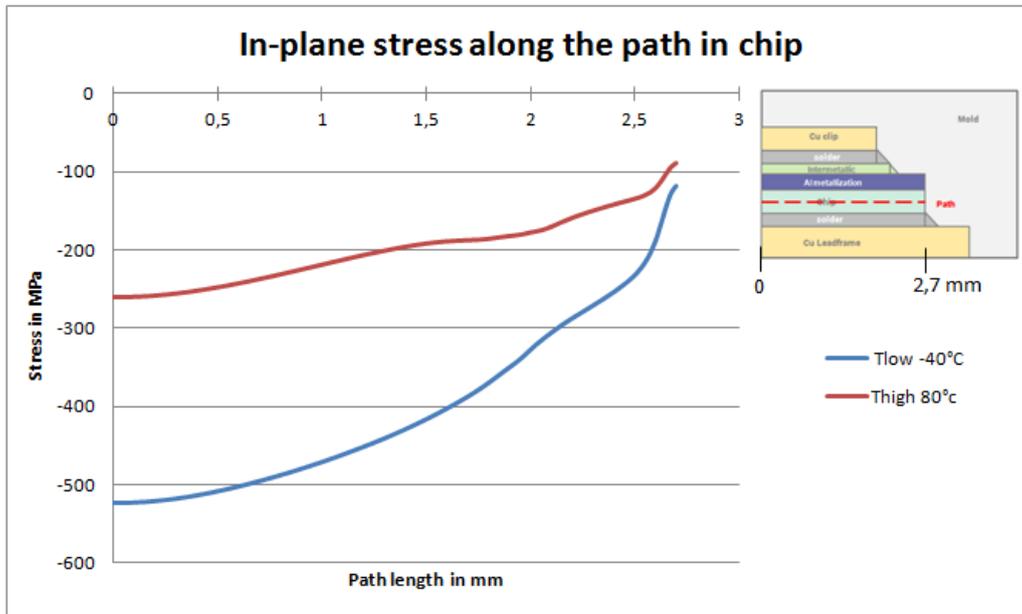


Figure 5.30: In-plane stress along the path in the chip for low and high temperatures

As previously said, the out-of-plane stress and the shear stress are almost inexistent in the module, and so it is also in the chip. The maximum of out-of-plane stress is reached at the chip extremity, at the interface with mold and the maximum of shear stress is also reached at the chip extremity but at the interface with the bottom solder meniscus (Figure 5.31). It is important to study these values of stress reached at these interfaces as it can influence the growth of a crack induced in the chip by sawing. The maximum out-of-plane stress reached at the interface with mold in one cycle is taken as an indicator that can be compared from one simulation case to another. In this present case the maximum out-of-plane stress reaches 98 MPa. This value is not critical as it remains under the critical limit of 200 MPa. The maximum of shear stress occurring close to the interface chip/bottom solder meniscus is also taken as an indicator and reaches value of 109 MPa. Here it is more difficult to evaluate if the shear stress is critical, as no references are known. Here the results are very similar to the PTC ones; there is only more shear stress at the interface chip/bottom solder meniscus under APC than under PTC.

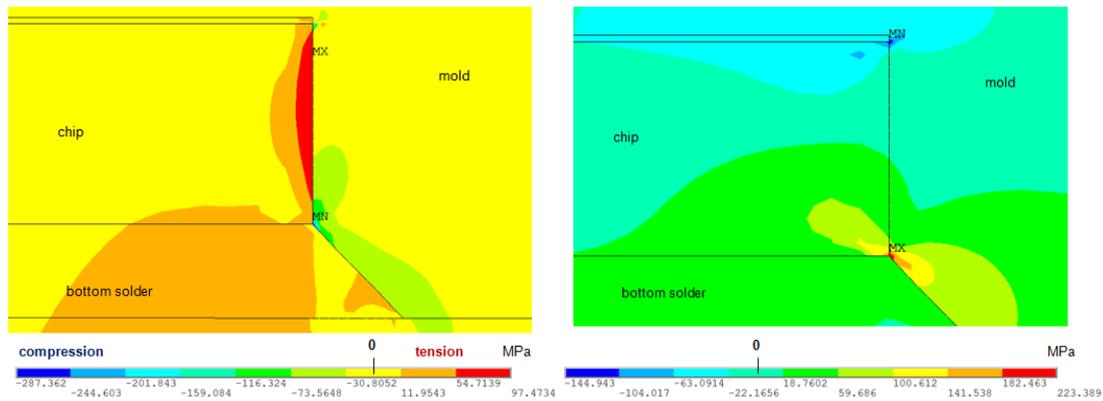


Figure 5.31: On the left the out-of-plane stress at -40°C at the interface chip-mold. On the right the shear stress at -40°C at the interface chip/bottom solder meniscus

5.2.3.3 Bottom solder behavior

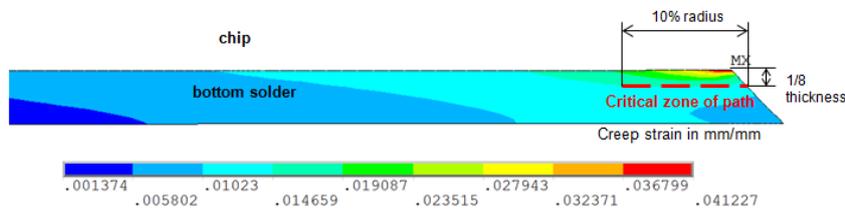


Figure 5.32: Creep strain in the bottom solder

The creep strain in the bottom solder is analyzed via a path defined at its extremity at the height of $1/8$ of the layer thickness, close to the chip (Figure 5.32). This method is used for the analysis of creep strain in standard module and can be transferred for our module as a maximum of creep strain is to be seen in this area. The acc creep strain for one cycle is calculated by averaging the creep strain along the path. Thus the relevant width of the path in terms of creep strain has to be determined. The averaged creep strain and the acc creep strain during the 6 cycles were calculated for several different widths of path ranging from 20% to 5% of the bottom solder radius (Figure 5.33 and Figure 5.34). Curves on both graphic are approximately parallel to each other if we exclude the 5% radius curves. Thus a radius of 10% was taken, as a crack with such a length would represent a degradation of 20% of the thermal path, which is a critical limit. By calculating the acc creep strain per cycle for the 10% radius path, one can see that the system is already stable after 2 cycles.

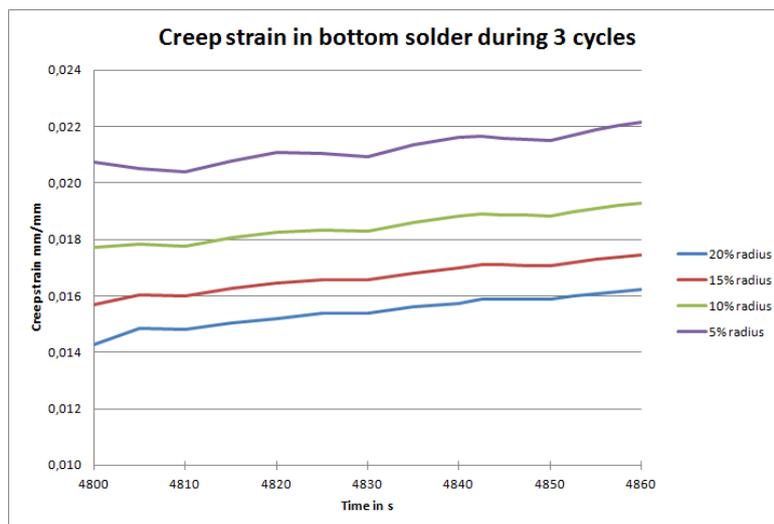


Figure 5.33: Creep strain in the bottom solder during 3 cycles

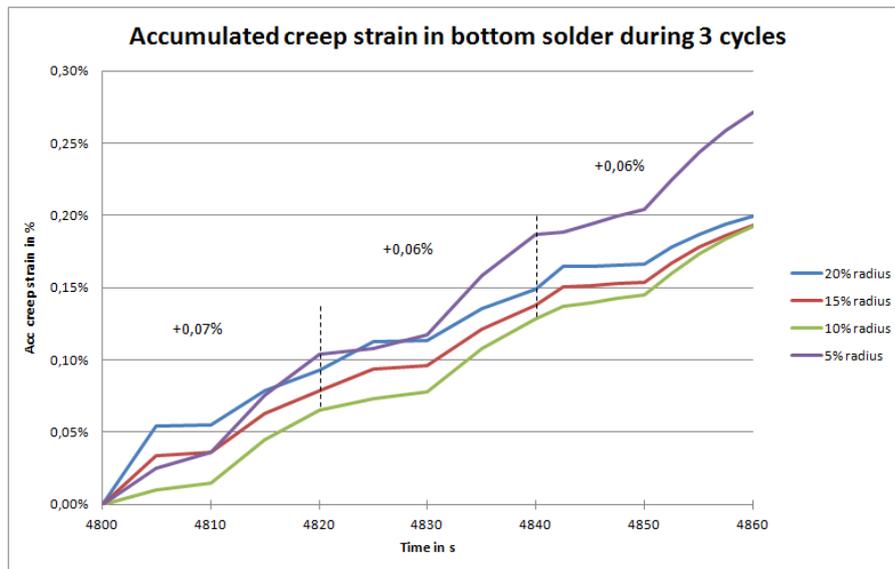


Figure 5.34: Acc creep strain in the bottom solder during 3 cycles

Finally, the evolution of temperature, von Mises stress and acc creep strain in one cycle at the critical area of the bottom solder is plotted Figure 5.35. The initial von Mises stress value is relatively high as a 175°C stress free temperature was defined and the cycle starts at -40°C. By heating up, the stress decreases and reaches a minimum value. By continuing heating up, the stress changes its direction thus the von Mises stress increases. Then the temperature stays constant, and we observe a stress relaxation. By starting the cooling phase, the stress reaches a minimum value and increases by decreasing temperature. The acc creep strain follows the temperature changes and starts to increase at the beginning of heating up or cooling down. At constant temperature the creep strain continues to increase. Thus the t_{on} can have a significant influence on the creep state in solder. The accumulation of creep strain is much lower for heating phase than for cooling phase.

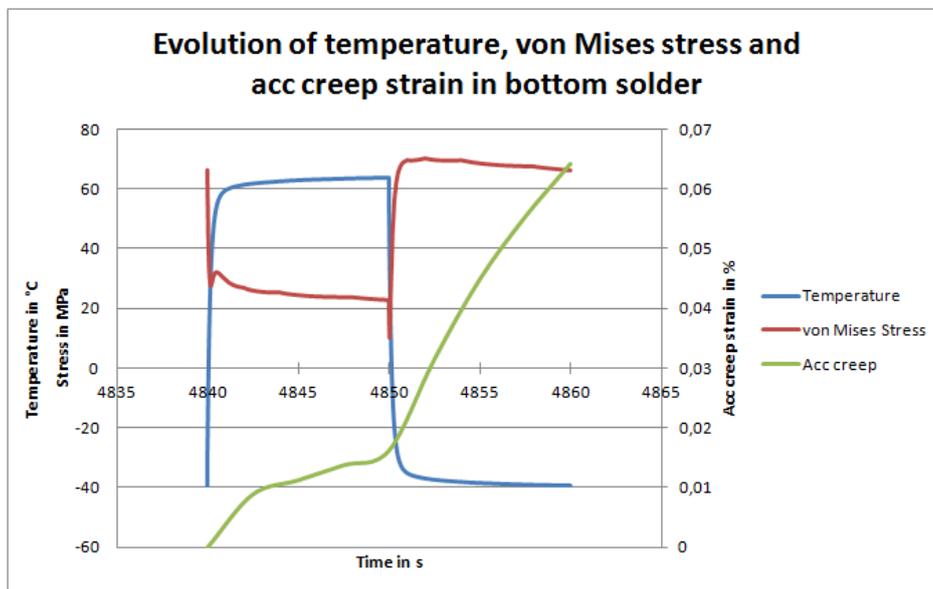


Figure 5.35: Evolution of temperature, von Mises stress and acc creep strain in the bottom solder during one cycle

In 1 cycle the bottom solder accumulates only 0,064 % of creep strain, which is really low in comparison to the 2,3% of creep accumulated under PTC. Thus for APC the creep behavior of the bottom solders is completely different to the one under PTC, and will probably not be the main failure mechanism.

5.2.3.4 Top solder behavior

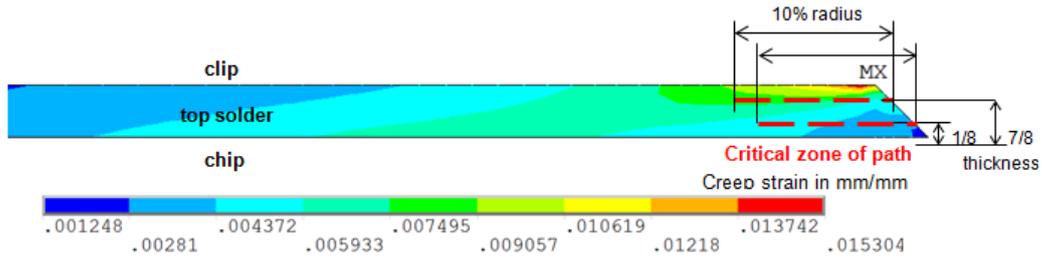


Figure 5.36: Creep strain in the top solder under APC

For the top solder, 2 paths are defined (Figure 5.36). One path is defined at 1/8 of the thickness, close to the chip, as it is the reflected equivalent to the path defined in the bottom solder and another path is defined at 7/8 of the thickness, close to the clip as the maximum of creep is to be seen in this region. Here also the relevant width of both paths in terms of creep strain has to be determined. So for both paths, the averaged creep strain and the acc creep strain during the 3 cycles were calculated with different path widths ranging from 20% to 5% of the top solder radius (Figure 5.37 and Figure 5.38). Resulting curves are proportional, thus we decided to take a radius of 10% for both paths by analogy with what was done for the bottom solder. By calculating the acc creep strain per cycles for both 10% radius paths, one can see that the system needs about 3 cycles maybe more to be stabilized.

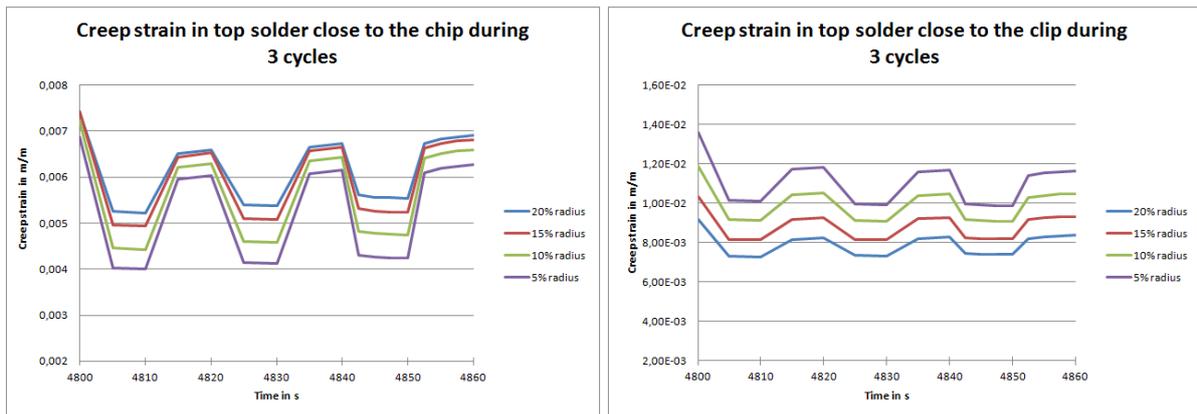


Figure 5.37: Creep strain in top solder during 3 cycles. On the left, the creep strain for the path close to the chip and on the right for the path close to the clip.

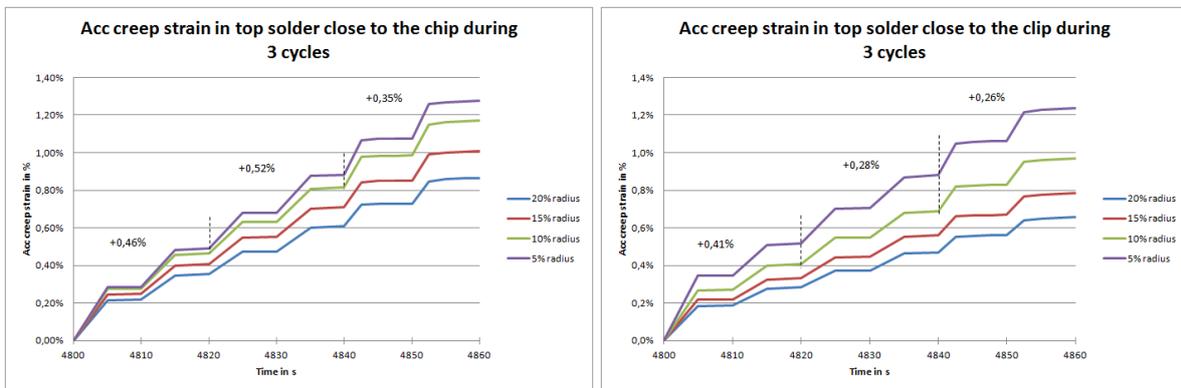


Figure 5.38: Acc creep strain in top solder during 3 cycles. On the left, the acc creep strain for the path close to the chip and on the right for the path close to the clip.

Then the acc creep strain during one cycle is calculated and plotted for both paths Figure 5.39. For the path close to the chip, the acc creep strain reaches 0,35 % in one cycle, whereas the path close to the clip reaches 0,28 %. Again these results are quite low, but already higher than the ones of the bottom solder.

Thus in this case more degradation can be expected in the top solder than in the bottom solder. It was exactly the opposite for PTC. This shows again that the creep behavior of solder is completely different under PTC or under APC.

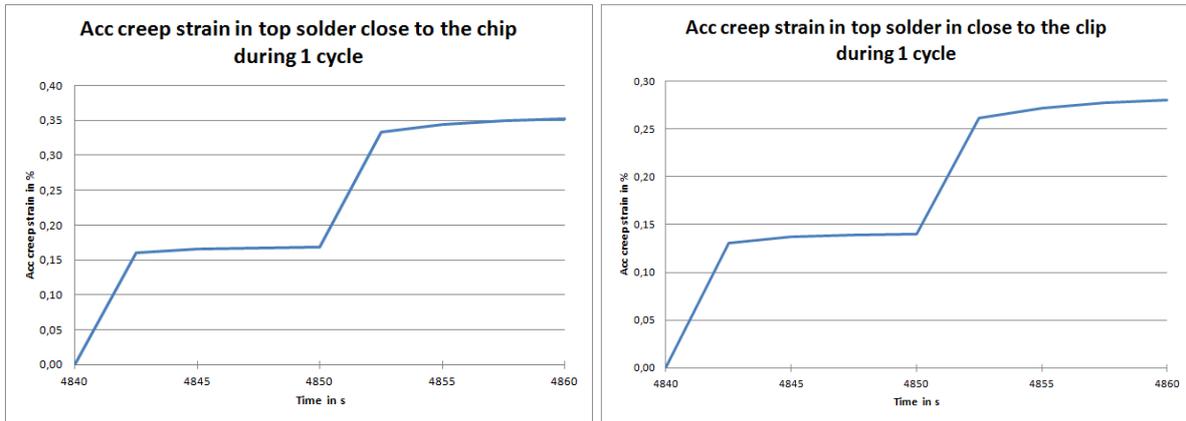


Figure 5.39: Acc creep strain in top solder during one cycle. On the left, the acc creep strain for the path close to the chip and on the right for the path close to the clip.

5.2.3.5 Al metallization behavior

The von Mises stress along the path in the Al metallization is plotted Figure 5.40. At the beginning of the path, the von Mises stress at low temperature reaches a value of 80 MPa and stays constant up to 1,5 mm. Whereas at high temperatures the von Mises stress begins with about 50 MPa, stays constant up to 1 mm and then increases until reaching 80 MPa at about 1,5 mm. Up to this location the von Mises stress of low and high temperatures are almost similar. An irregularity in both curves appears at about 2 mm. It is interesting to note that this point corresponds to the top solder meniscus, which means that, up to this point the chip is only soldered on one side. The von Mises stress in Al is critical, as the yield stress is reached, giving rise to plastic strain.

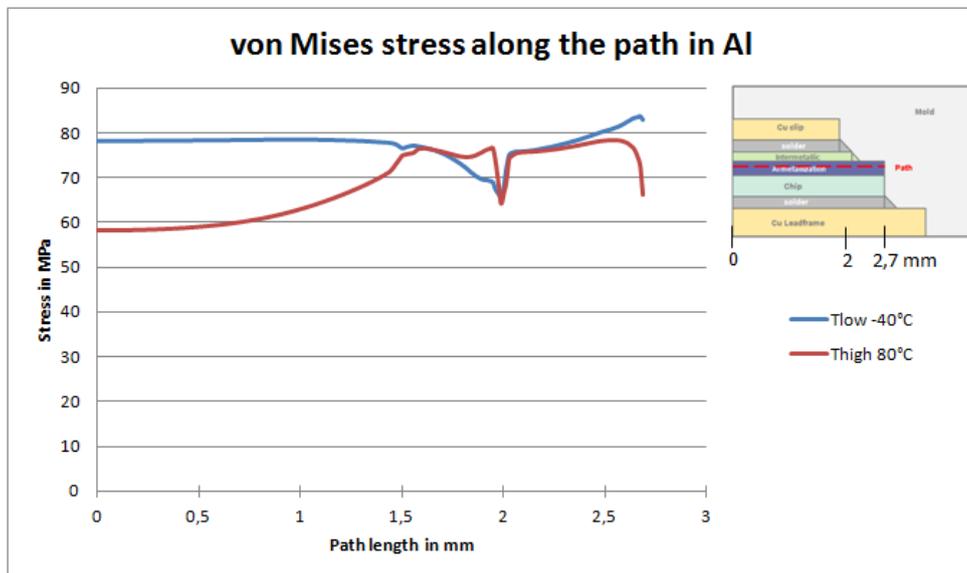


Figure 5.40: von Mises stress along the path in Al metallization

Then the in-plane stress is analyzed (Figure 5.41). At high temperatures, the Al is under compressive stress, whereas at low temperatures tensile stress is dominant. In compression the stress varies from -60 MPa to -100 MPa, and in tension it varies from 40 to 70 MPa. These values are close to the yield point. In tension and compression an irregularity also appears at the top solder meniscus area, pointing out again the specificity of this area. To better evaluate the specificity of this zone, the stress-strain curves of the 3 simulated cycles were plotted for one node located at the center of this top solder meniscus area (Figure 5.42). A hysteresis curve is

to be seen, indicating that the yield point for the in-plane stress was reached in this specific area and that plastic deformations are occurring.

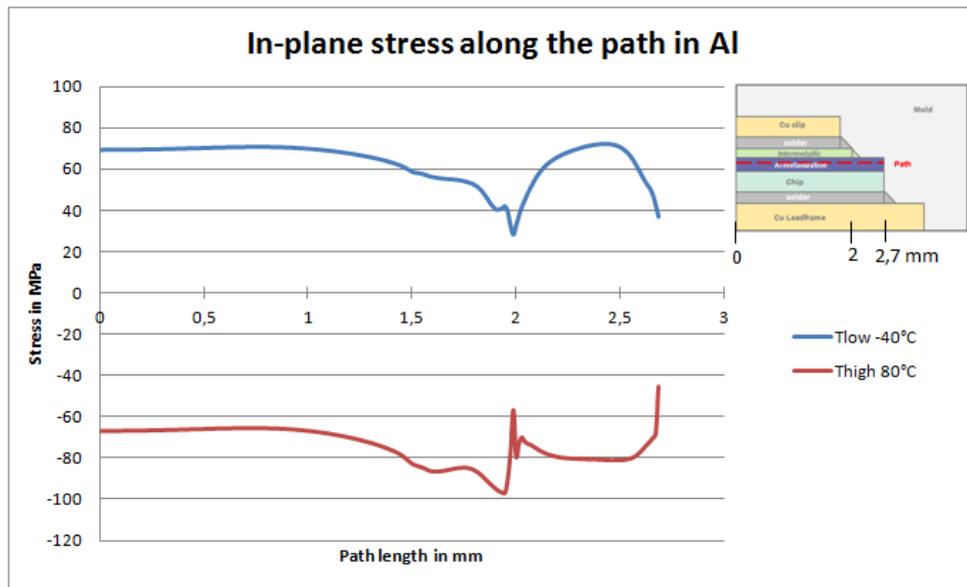


Figure 5.41: In-plane stress along the path in the Al metallization

For the out-of-plane stress, at the beginning of the path curves for high and low temperatures are both around -10 MPa. Then at about 2 mm, a compressive peak of -15 MPa occurs at high temperature, whereas a tensile peak of 15 MPa occurs at low temperature. This shows again the top solder meniscus area as critical. For the rest of the path the out-of-plane stress is close to zero whatever the temperature. Here also the stress-strain curve at one node of the top solder meniscus shows a hysteresis curve, indicating again plastic deformations.

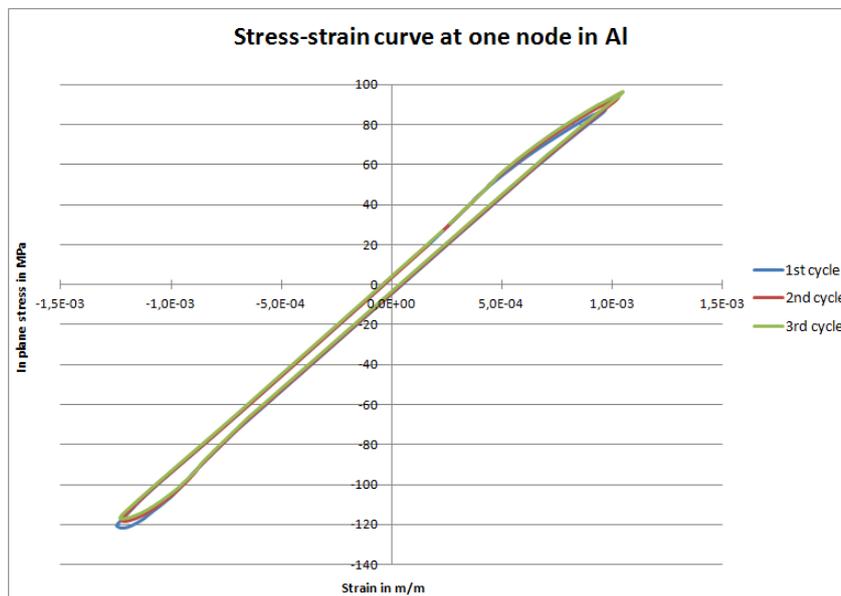


Figure 5.42: Stress strain curve for the in-plane stress at 1 node of the top solder meniscus area in the Al

Finally the shear stress is close to zero at the beginning of the path and whatever the temperature. Then at the top solder meniscus a peak of compression of -35 MPa appears for high temperatures, whereas a peak of tension of 20 MPa appears for low temperatures. So the area under the top solder meniscus appears also to be critical for the shear stress. For the rest of the path stress ranges from -20MPa to -10MPa. In this case the stress strain curve stays purely elastic. So the shear stress remains too low to be a critical component of stress in Al.

From this stress analysis, it can be deduced that the von Mises stress is mostly composed of in-plane and out-of-plane stresses. And by comparing all the curves, it appears that the von Mises is driven by the in-plane stress.

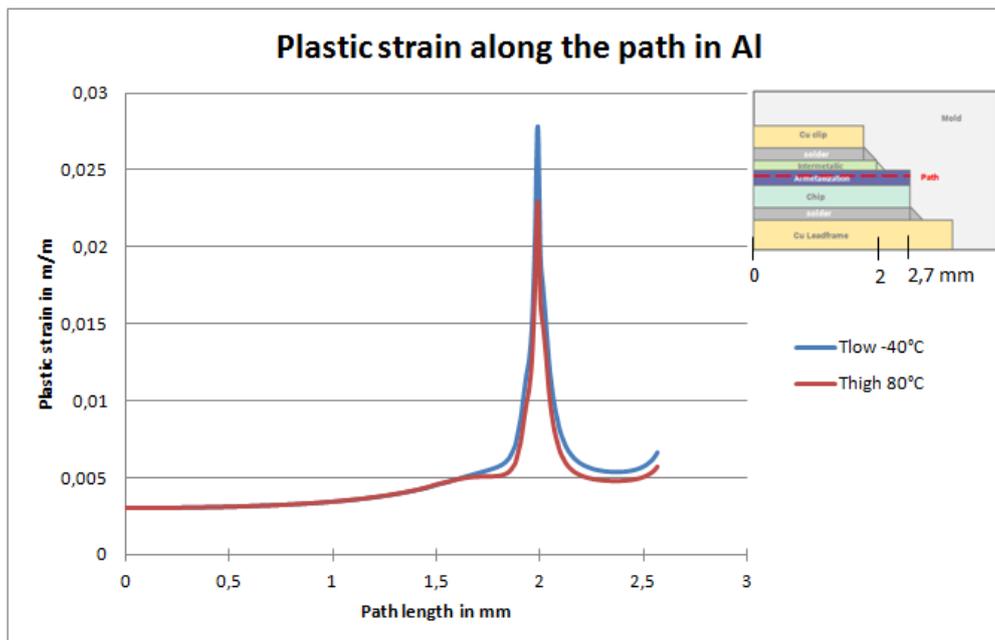


Figure 5.43: Plastic strain along the path in the Al metallization

Plastic strain curves along the Al path confirm the importance of the zone under the top solder meniscus, as a peak of plastic strain is observed exactly at this position (Figure 5.43). In order to better understand the mechanisms Al is submitted to in this critical area, it is interesting to analyze the correlation between the evolution of the temperature, the acc plastic strain and the von Mises stress during one cycle. Therefore, the acc plastic strain per cycle was calculated by averaging the plastic strain obtained along the path in the area beneath the top solder meniscus, and was then plotted together with the evolution of temperature and von Mises stress (Figure 5.44). More precisely, the plastic strain average was calculated for the values obtained between 1,983mm to 1,993mm along the path in the Al. The von Mises stress is chosen as it represents the stress in every direction and defines when the yield stress is reached. At the beginning of the temperature pulse the von Mises stress originates from the initial conditions: a 175°C stress free temperature is defined and the module is cooled down to room temperature. This gives the frozen internal stresses within the package. Now, when the system heats up, these inner stresses decrease and reach a minimum value. By continuing the heating up process, the stress changes its direction and the von Mises stress and the plastic strain increase simultaneously. Then the temperature remains constant, and a stress relaxation without an increase in the plastic strain can be observed. The stress relaxes under constant plastic strain because of the solder layer on top of the Al metallization, which transfers its stress relaxation behavior. In the following cooling phase the same behavior is repeated, with the opposite deformation direction. The acc plastic strain follows the temperature changes and increases by heating up or cooling down, and stays constant at constant temperature. One can also notice that the acc plastic strain is higher during the cooling phase than during the heating phase. In one cycle the acc plastic strain reaches the value of 0,74%. This is comparable and even more than the 0,7% reached under PTC, and it is also much higher than the values of acc creep strain reached for both solders under APC. Thus here the dominant failure mechanism will probably be the degradation of the Al metallization, before solders degradations. This is the opposite of what was observed for PTC.

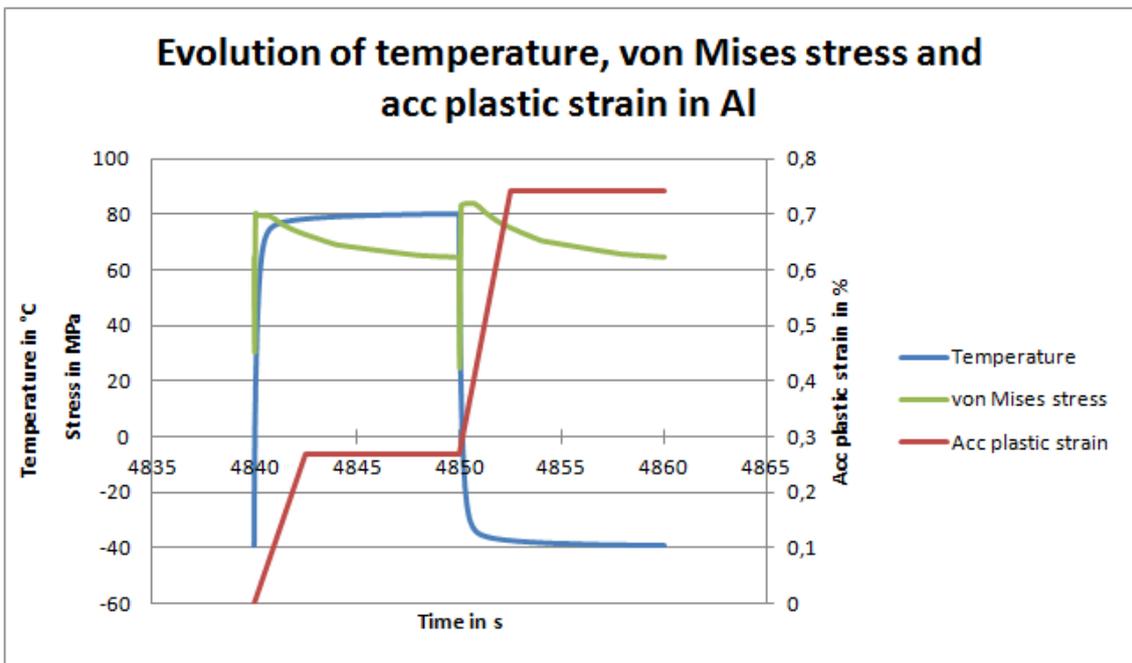


Figure 5.44: Evolution of temperature, von Mises stress and acc plastic strain in Al metallization at the critical area beneath the top solder meniscus during 1 cycle

5.2.3.6 IMC behavior

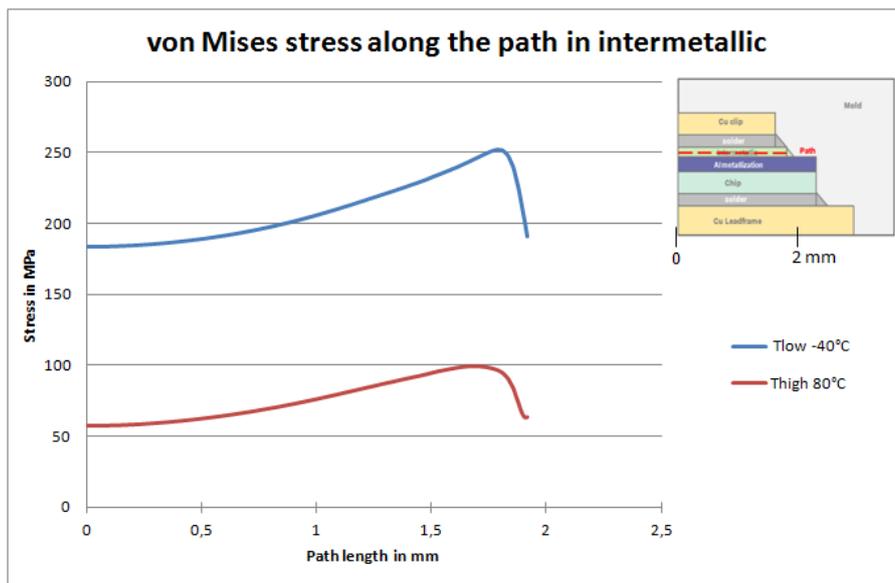


Figure 5.45: von Mises stress along the path in the IMC on top of the chip

The von Mises stress along the path in the IMC is plotted Figure 5.45. For both low and high temperatures, the von Mises stress along the path starts with a minimum value on the symmetry axis, and then increase until reaching a maximum close to the extremity of the layer, before finally decreasing until reaching the layer extremity. Thus the area close to the extremity of the layer is the most critical in terms of stress in the IMC. The highest stress value are reached under low temperature, with a maximum of 250 MPa reached at -40°C in the critical area close to the layer extremity. For the IMC no critical limits of stress are known thus it is difficult to really evaluate how critic or not the situation is.

The in-plane, out-of-plane and shear stresses in the IMC were also analyzed. The out-of-plane and shear stresses are close to zero for both high and low temperatures, but some maximum are also observed close to the extremity of the layer. The in-plane stress is very similar to the von Mises stress, as it is the stress component that drives the von Mises stress.

So here the behavior of the IMC is very similar for PTC and APC.

5.2.4 Sensitivity study

5.2.4.1 Chip behavior

The inverse radius of curvature is taken as an indicator of the intensity of warpage in the chip: the higher the value, the most bended the chip is. A negative value represents a bending down whereas a positive value represents a bending over. The inverse radius of curvature is reported for all cases of the sensitivity study and is plotted Figure 5.46. Three values are taken into account: the minimum (blue) and maximum (red) warpage reached in one cycle, and the amplitude of warpage (green) which is the difference between the maximal and minimal values of inverse radius reached in one cycle. The amplitude is of main interest, but the minimum and maximum permit to see in which direction the warpage occurs. At low temperatures, the warpage is minimal while at high temperatures the warpage is maximal. In the first half of the histogram with $T_{jmin}=-40^{\circ}\text{C}$ to 10°C , minimum value of inverse radius are indicating a bending down of the structure, whereas for the other half of the histogram with $T_{jmin}=10^{\circ}\text{C}$ to 60°C , the structure is always over bended. So the bending direction is directly influenced by T_{jmin} . Then by analyzing the amplitude of warpage, the influence of the other test parameters appears quite clearly. The amplitude of warpage increases by increasing ΔT_j and decreasing t_{on} . T_{jmin} has no influence on the warpage amplitude, but only on the warpage direction. But for the same amplitude of warpage in one cycle, a case with a change of warpage direction is considered as more critical than a case without warpage direction change. Thus the critical set of parameters in terms of warpage is low T_{jmin} , large ΔT_j and short t_{on} . The warpage values obtained under PTC are similar to the ones obtained for the APC case with $T_{jmin}=-40^{\circ}\text{C}$, $\Delta T_j=120\text{K}$ and $t_{on}=0,2\text{s}$, which actually corresponds to the worst case of the sensitivity study. But the PTC experiments did not reveal any failures due to warpage, thus all warpage values reached for the DoE are not critical. Thus the minimum critical limit for the warpage amplitude can be defined by: $1/R_{amplitude\ c} = 0,6\text{ m}^{-1}$. When the warpage amplitude remains under the limit, it is not critical, but when it exceeds the limit, then a case study should be performed to determine how critic it is.

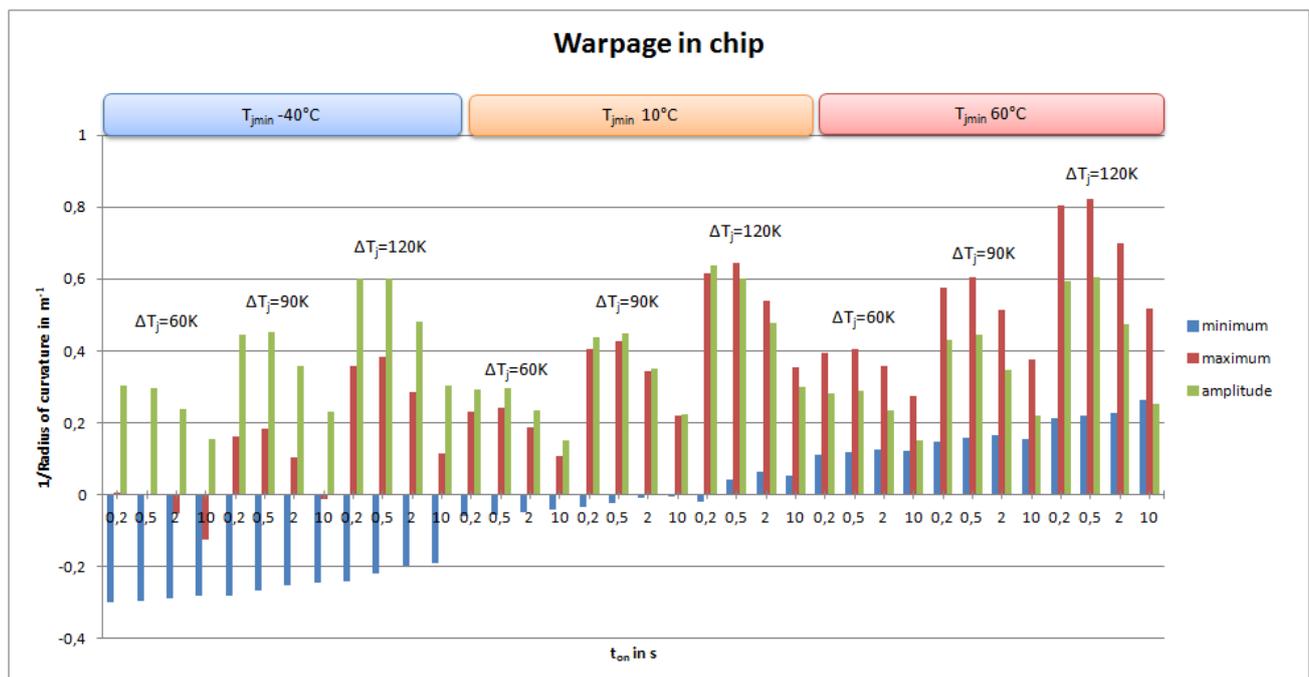


Figure 5.46: Histogram showing the inverse radius of curvature for different sets of test parameters

The minimum and maximum in-plane stress reached at the center of the chip in one cycle are plotted Figure 5.47 together with the stress amplitude. Here also the important value is the stress amplitude, but minimum and maximum of stress allow us to have information on the stress direction. The minimum in-plane stress is reached at low temperatures whereas the maximum occurs at high temperatures. Minimum stress values are directly influenced by T_{jmin} : all cases with a determined T_{jmin} have exactly the same value of minimum stress. Then by looking at the evolution of the stress amplitude, it appears that it increases with an increasing ΔT_j and an increasing t_{on} . T_{jmin} has no influence on the in-plane stress amplitude, with the same ΔT_j and t_{on} but different T_{jmin} , the same stress amplitude is to be found. Thus the critical set of parameters in terms of in-plane stress in chip is a large ΔT_j and a long t_{on} . The worst case occurs then for $T_{jmin}=-40^{\circ}\text{C}$, $\Delta T_j=120\text{K}$

and $t_{on}=10s$ with 263MPa of in-plane stress amplitude. Under PTC, the minimum stress is -439MPa, the maximum 39MPa which gives amplitude of 478MPa. So the stress amplitude reached under PTC is higher than under the different APC cases. But all APC and PTC cases are not critical, as all stress values are remaining smaller than 900MPa which is known as a critical limit for in-plane stress in the chip.

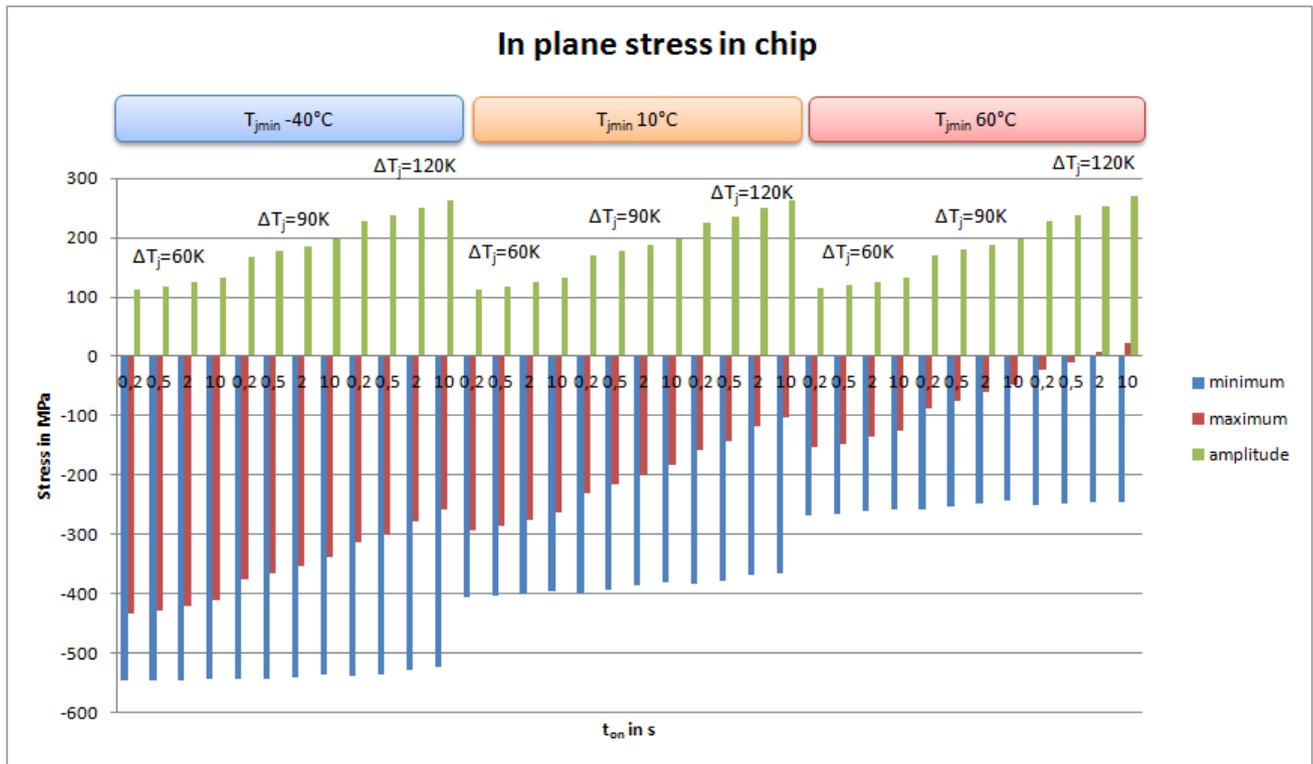


Figure 5.47: Histogram showing the in-plane stress for different sets of test parameters

The minimum and maximum out-of-plane stress reached at the chip extremity at the interface with the mold in one cycle are plotted Figure 5.48 together with the deduced amplitude. The main interest is the stress amplitude, and stress extremes give us an idea about real stress state. At low temperatures the maximum stress is reached while at high temperature the minimum stress state is reached. The minimum stress decreases with increasing T_{jmin} , ΔT_j and t_{on} . The maximum stress slightly increases with decreasing T_{jmin} and increasing ΔT_j and t_{on} . Thus the worst parameters in terms of out-of-plane stress amplitude are a high T_{jmin} , large ΔT_j and long t_{on} . At $T_{jmin}=60^\circ C$, an unexpected decrease in the maximum stress occurs, this may come from a change in the mold properties due to the high temperature. The worst case still occurs for $T_{jmin}=60^\circ C$, $\Delta T_j =120K$ and $t_{on}=10s$ with 60 MPa of out-of-plane stress amplitude. Under PTC the minimum out-of-plane stress was -4MPa, the maximum 92 MPa which gives amplitude of 96 MPa. So the values reached under PTC are worst than the worst case of APC, nevertheless all results for APC and PTC are still not critical, as stresses are not surpassing the limit of 200MPa.

The minimum and maximum of shear stress reached at the chip extremity close to the bottom solder meniscus in one cycle are shown Figure 5.49. Here also the important value of the diagram is the stress amplitude. At low temperatures the maximum stress is reached while at high temperature it is the minimum stress that is reached. The minimum stress decreases with increasing T_{jmin} , ΔT_j and t_{on} . The maximum stress increases with decreasing T_{jmin} and increasing ΔT_j and t_{on} . Thus the worst parameters in terms of shear stress amplitude are low T_{jmin} , large ΔT_j and long t_{on} . At $T_{jmin}=60^\circ C$, an unexpected decrease in the maximum stress occurs, this may also come from a change in the mold properties due to the high temperature, as the mold is also close to the point where the analysis was made. Anyway the worst case occurs for $T_{jmin} = -40^\circ C$, $\Delta T_j =120K$ and $t_{on}=10s$ with 65 MPa of shear stress amplitude. Under PTC the minimum shear stress was 0MPa, the maximum 87 MPa which gives amplitude of 87 MPa. So the values reached under PTC are worst than the worst case of APC. No critical limit is known for the shear stress in chip, but as no systematic failure are occurring in chip, one can consider the shear stress under APC and PTC as not critical.

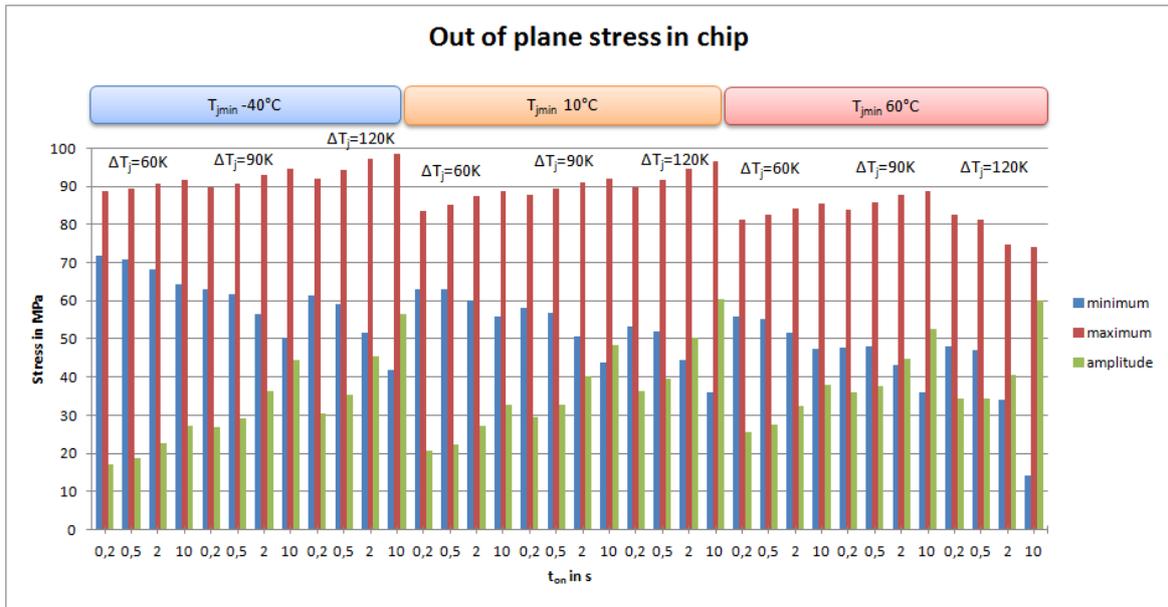


Figure 5.48: Histogram showing the out-of-plane stress for different sets of test parameters

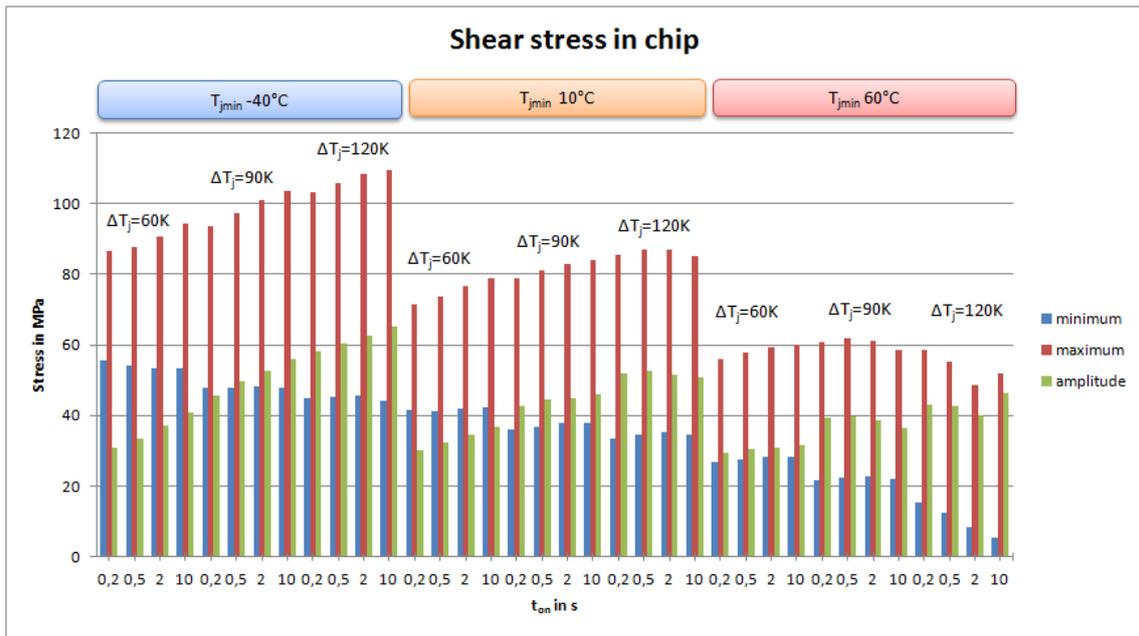


Figure 5.49: Histogram showing the shear stress for different sets of test parameters

This study on deformations and stresses in the chip revealed that in any cases none of the different indicators analyzed were found to be critical. Thus it can be concluded that crack in chip is not a failure mechanism that our module is subjected to.

5.2.4.2 Bottom solder behavior

The acc creep strain in one cycle was taken as an indicator of solder degradation and is plotted for the bottom solder solder and for all cases of the sensitivity study

Figure 5.50. The influence of the test parameters on creep appears clearly: creep strain accumulates with high T_{jmin} , large ΔT_j and long t_{on} . This is quite logical, as creep is known to be typically a plasticity which occurs at high temperature thus necessitating high T_{jmin} and large ΔT_j . Moreover, creep needs time to increase, thus long t_{on} leads to higher percentage of accumulated creep. Thus the worst case of APC occurs with $T_{jmin}=60^\circ\text{C}$,

$\Delta T_j=120K$ and $t_{on}=10s$, and it leads to 0,33% of acc creep strain. This remains a small amount, especially if we compare with the 2,3% reached under PTC. But still some degradations were observed after APC tests and an increase in Z_{th} indicating critical degradations of the bottom solder was sometimes noticed. With this information a first critical value can be developed for the acc creep strain, by stating that the acc creep strain obtained for $T_{jmin}=10^\circ C$ with $\Delta T_j = 120K$ and t_{on} between 0,5s and 2s defines a limit. When the acc creep strain remains under the limit, it is not critical, but when it exceeds the limit, then a case study should be performed to determine how critic it is. Thus a critical limit of 0,1% of acc creep strain can be defined for the bottom solder. So cases susceptible to be critical in terms of acc creep strain are cases with: $T_{jmin}=10^\circ C$, $\Delta T_j=120K$ and $t_{on} > 2s$, $T_{jmin}=60^\circ C$, $\Delta T_j=90K$ and $t_{on} > 2s$ and or $T_{jmin}=60^\circ C$ with $\Delta T_j=120K$.

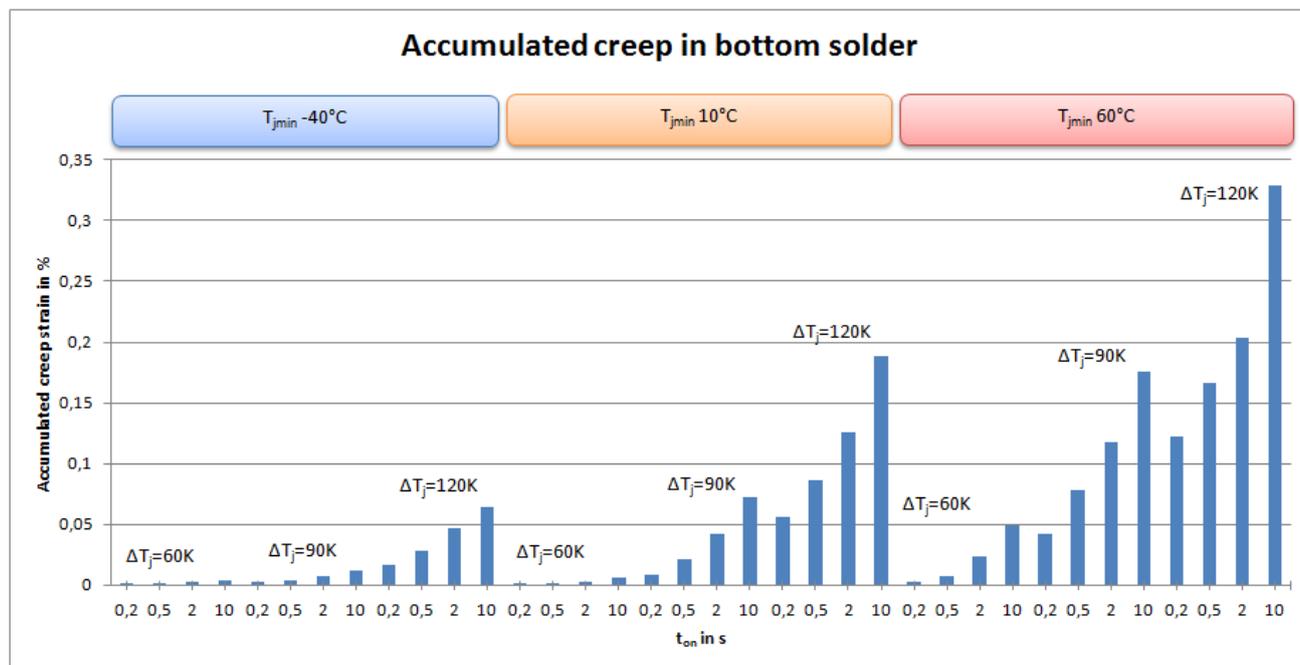


Figure 5.50: Histogram showing the acc creep strain in the bottom solder for different sets of test parameters

5.2.4.3 Top solder behavior

The acc creep strain in the top solder close to the chip is plotted for different sets of parameters on Figure 5.51. The same conclusion can be drawn on the influence of the test parameters: creep strain accumulates with high T_{jmin} , large ΔT_j and long t_{on} . But here we have exceptional cases which do not obey to this rule. These 4 cases have for test parameters: $T_{jmin} = 60^\circ C$, $\Delta T_j = 120K$ and t_{on} ranging from 0,2s to 10s. These exceptional results may be explained by the fact that the mold has an influence on the creep behavior in the top solder. At $T_{jmin}=60^\circ C$ and with $\Delta T_j=120K$, the glass transition temperature of the mold $T_g= 150^\circ C$ is surpassed and therefore the Young's modulus of the mold drops down. This may induce some changes in the behavior of the structure and leads to a decrease of creep strain in the top solder behavior. Thus here, the worst case is not $T_{jmin}=60^\circ C$, $\Delta T_j=120K$ and $t_{on}=10s$ as it would be expected, but $T_{jmin}=10^\circ C$, $\Delta T_j=120K$ and $t_{on}=10s$, with 0,73% of acc creep strain. The amount of acc creep strain is already about 2 times higher than what was accumulated in the bottom solder, and is quite close to the critical limit of 1% defined for PTC. No critical limit is known yet regarding the amount of acc creep strain under APC in the top solder, but a first critical value can be proposed based on the results obtained. As some failure in the top solder appears quite often in experiment, it can be stated that the amount of creep accumulated for $T_{jmin}=10^\circ C$, $\Delta T_j=90K$ and $t_{on}=10s$, that is to say 0,35%, defines a limit. When the acc creep strain remains under limit, no critical degradations are to be expected in solder, but when it exceeds the limit, than a case study should be performed to determine how critic it is. So for the path in the top solder close to the chip, cases susceptible to be critical in terms of acc creep strain are cases with: $T_{jmin}=10^\circ C$ with $\Delta T_j=120K$ and $T_{jmin}=60^\circ C$ with $\Delta T_j=90K$ or $120K$.

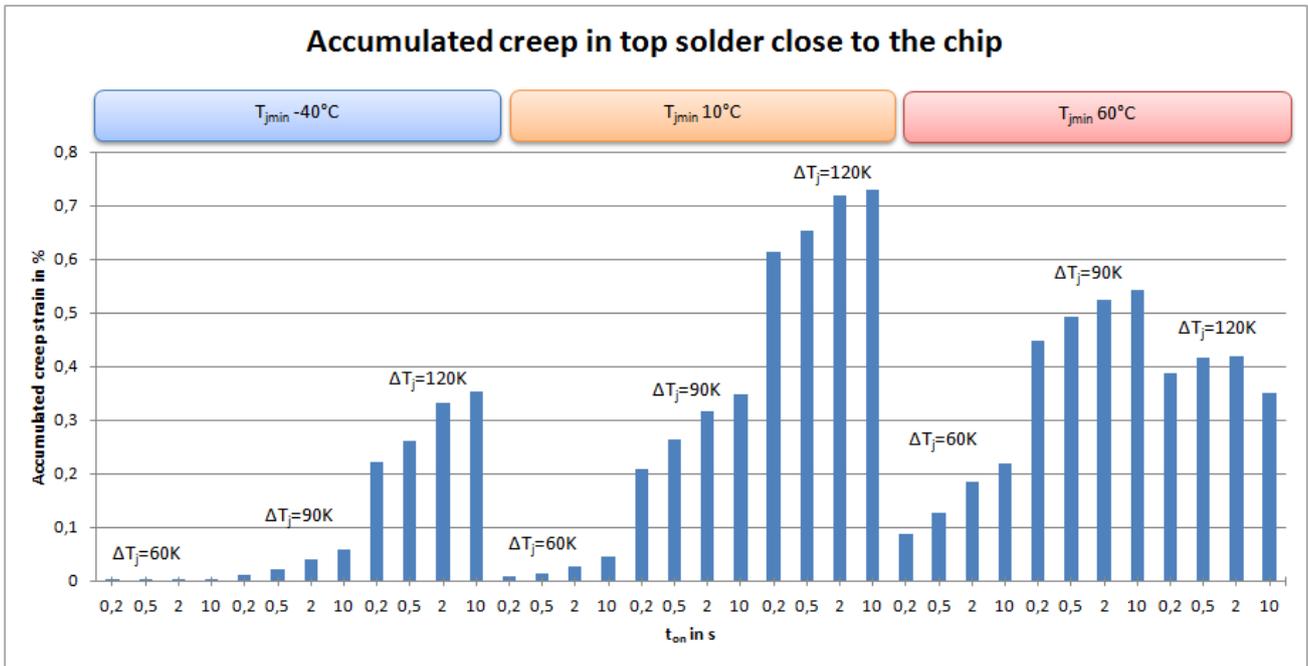


Figure 5.51: Histogram showing the acc creep strain in the top solder close to the chip for different sets of test parameters

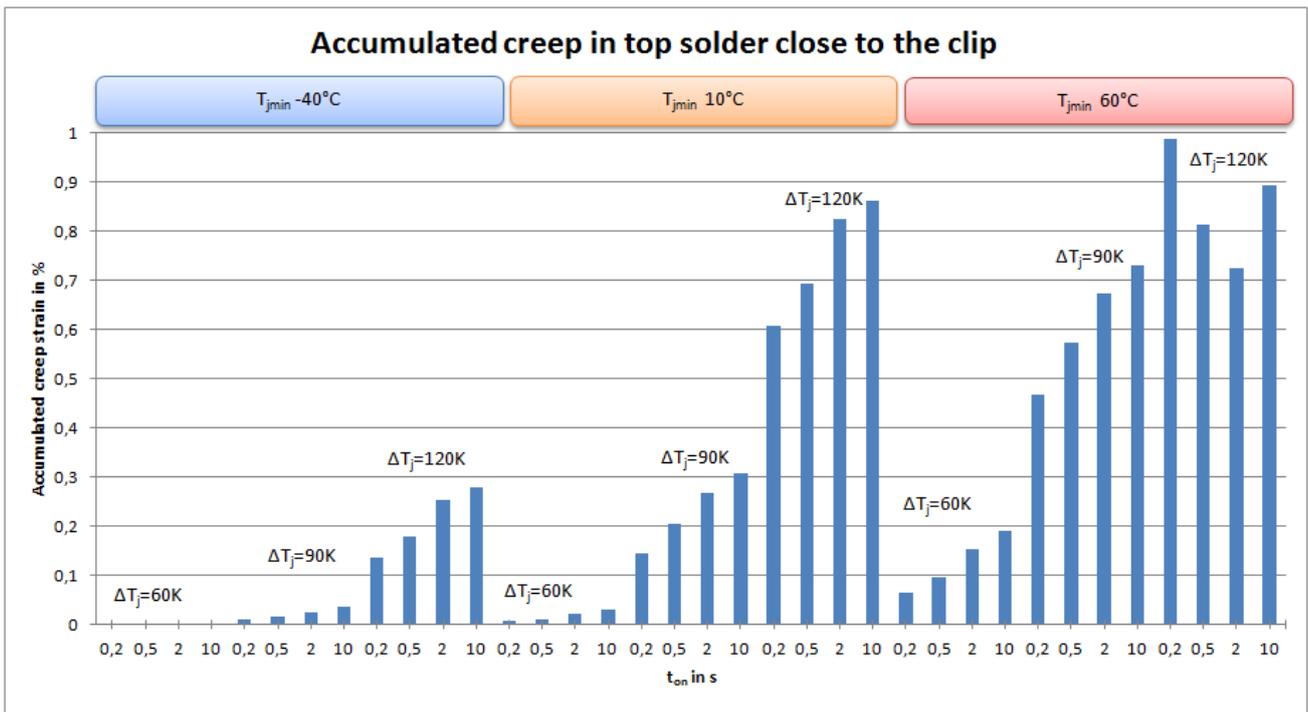


Figure 5.52: Histogram showing the acc creep strain in the top solder close to the clip for different sets of test parameters

The acc creep strain in the top solder close to the clip is plotted for different sets of parameters on Figure 5.52. Here also creep strain accumulates with high T_{jmin} , large ΔT_j and long t_{on} . And there are also 4 cases which do not obey to this rule: cases with test parameters $T_{jmin}=60^{\circ}C$, $\Delta T_j=120K$ and t_{on} ranging from 0,2s to 10s. These results may also be explained by the fact that high temperatures are reached, thus leading to a drop down of the Young's modulus of the mold which may influence the creep behavior. Here the worst case is reached for $T_{jmin}=60^{\circ}C$, $\Delta T_j=120K$ and $t_{on}=0,2s$, with 0,99% of acc creep strain. The amount of acc creep strain for this case is really critical as it has quasi reached the critical limit of 1% defined for PTC. According to the critical limit defined in the previous paragraph for the top solder path close to the chip, the following cases are susceptible to be critical as well: $T_{jmin}=10^{\circ}C$ with $\Delta T_j=120K$ and $T_{jmin}=60^{\circ}C$ with $\Delta T_j=90K$ or $120K$. These

cases were actually already noticed as potentially critical for the acc creep strain in the top solder close to the chip. Under PTC the creep strain accumulated in the top solder close to the clip, is even higher than under APC as it reached 1,7%.

This analysis of acc creep strain in the different solder layers highlighted the fact that solder degradations are probably not the main failure mechanism under APC in opposition to what occur under PTC. Moreover it is the bottom solder that suffer the most from creep under PTC, whereas under APC it is not the bottom solder anymore but the top solder. Under APC the creep strain accumulated in solders can be considered as critical for the following sets of parameters: $T_{jmin}=10^{\circ}C$ with $\Delta T_j=120K$ and $T_{jmin}=60^{\circ}C$ with $\Delta T_j=90K$ or $120K$.

5.2.4.4 Al metallization behavior

The acc plastic strain in the critical area beneath the top solder meniscus is plotted for different sets of parameters (Figure 5.53). The influence of test parameters on plastic strain is quite clear. First of all, the lower T_{jmin} is, the higher the percentage of acc plastic strain will be. High ΔT_j are needed for the accumulation of plastic strain in one cycle. For small temperature swings like $\Delta T_j=60K$ which corresponds to field load, there is no acc plastic strain at all for $T_{jmin} = -40^{\circ}C$ and then really small amount of acc plastic strain of about $1e^{-6}$ are reached for $T_{jmin} = 10^{\circ}C$ and $60^{\circ}C$. These results confirm what was already observed in experiments, as several modules did not shown any degradations in Al after several millions of power cycles with $\Delta T_j=60K$. Finally, short t_{on} also generates more accumulation of plastic strains in Al. Indeed, power pulses lead to spatially inhomogeneous temperature distribution in the module. With short pulses, the spatial temperature gradient is even more important inside the module, thus generating more Al plastic deformations. Consequently, low T_{jmin} with large ΔT_j and short t_{on} are the most critical tests parameters in terms of plastic metallization deformation. Thus the worst case is obtained with $T_{jmin}= -40^{\circ}C$, $\Delta T_j=120K$ and $t_{on}=0,2s$ with 0,9% of acc plastic strain. This is an important amount, no critical values are known, but it is comparable to the highest values of acc creep strain in the top solder close to the clip. Under PTC a lower value of 0,74% of acc plastic strain was reached. Thus the plastic deformation of Al metallization seems to be an important failure mechanism under APC.

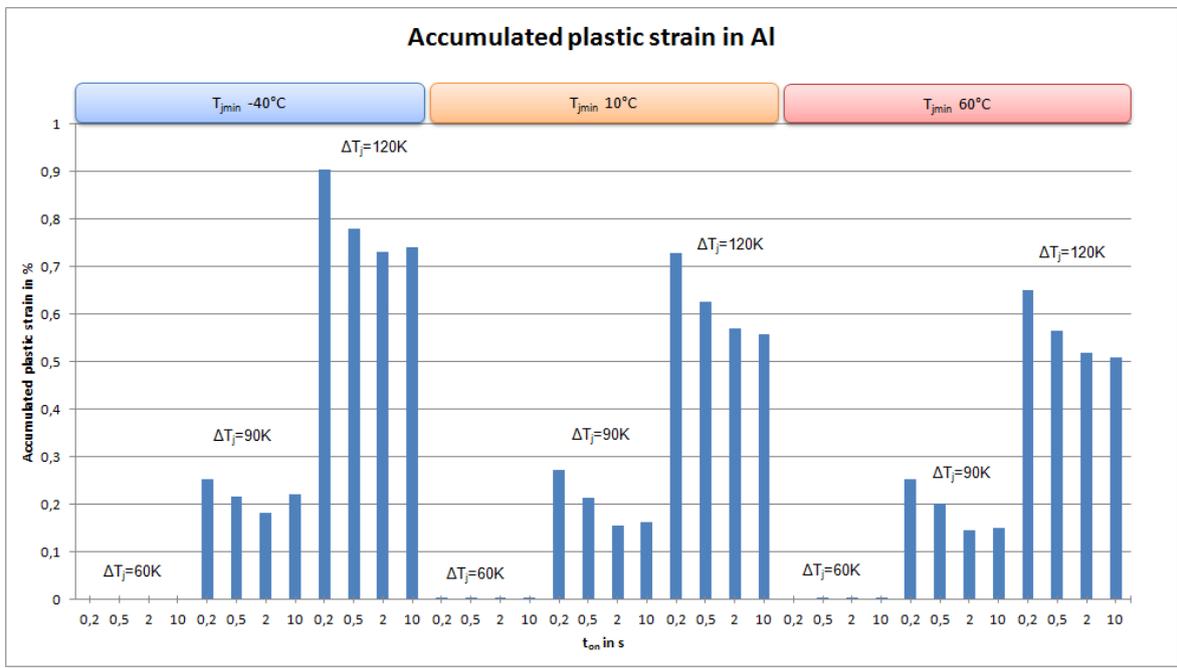


Figure 5.53: Histogram showing the acc plastic strain in Al metallization for different sets of test parameters

5.2.4.5 IMC behavior

The minimum and maximum of von Mises stress close to the IMC extremity in one cycle are shown Figure 5.54. The important value of the diagram is the stress amplitude. At low temperatures the maximum stress is reached while at high temperature it is the minimum stress that is reached. The minimum stress decreases with increasing T_{jmin} , ΔT_j and decreasing t_{on} . But at $T_{jmin}=60^\circ\text{C}$, $\Delta T_j=120\text{K}$ and $t_{on}=10\text{s}$ an unexpected decrease in the maximum stress occurs. This may be also attributed to a change in the mold properties due to the high temperature, as the mold is close to the extremity of the IMC layer. The maximum stress increases with decreasing T_{jmin} and increasing ΔT_j and t_{on} . Thus the worst parameters in terms of von Mises stress amplitude are low T_{jmin} , large ΔT_j and short t_{on} . So the worst case is reached with $T_{jmin} = -40^\circ\text{C}$, $\Delta T_j=120\text{K}$ and $t_{on}=0,2\text{s}$ with 178MPa of stress amplitude. Under PTC the minimum shear stress was 60MPa, the maximum 280 MPa which gives amplitude of 220 MPa. So the values reached under PTC are worst than the worst case of APC. No critical limit are known in this case, but as no important failure are occurring in the IMC, the stress values reached under APC and PTC are considered to be not critical.

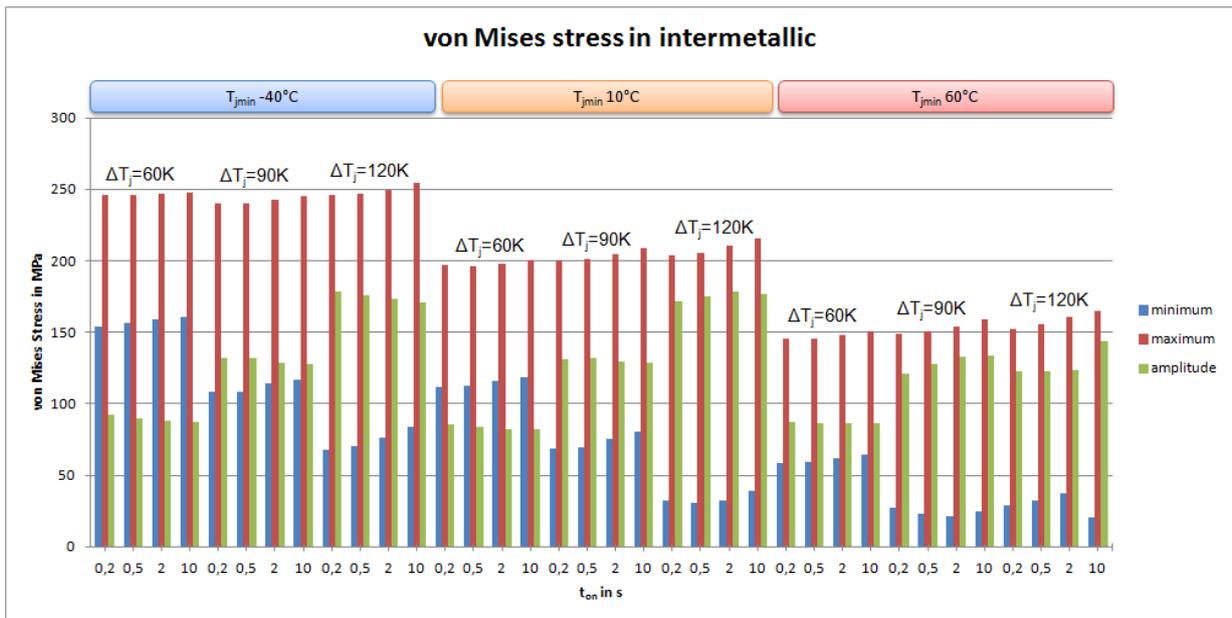


Figure 5.54: Histogram showing the von Mises stress in IMC for different sets of test parameters

It can be concluded from this entire sensitivity study that deformations and stresses in chip as well as stresses in IMC are not critical nor for PTC neither for APC. Under PTC modules are suffering from solder degradations due to creep mostly in the bottom solder, but the top solder is also affected. There is also a plastic strain accumulation in the Al metallization under PTC, but it remains too low to be critical in comparison to the accumulated creep strain in both solder layers. Thus under PTC devices are failing due to solder degradations which is the main failure mechanism, and thus no degradations of the Al metallization are observed. Under APC, modules are suffering from both plastic deformation in the Al metallization and degradations in solder layers due to creep. Thus under APC devices are failing due to plastic deformation in the Al and creep strain in solder layers, which constitute the main failure mechanisms.

5.2.5 Extension of the sensitivity study

The sensitivity study is then extended, by analyzing some cases variations. Thus some cases were simulated with long heating or cooling phase of 100s, or short cooling phase of 2s. A case with a different design was also analyzed: a thicker Cu lead frame was modeled and the resulting stresses and strains were compared to the results obtained with the original design. Another case had a very large ΔT_j in order to verify if this was then the worst case of the study. And finally some cracks were defined in the molding compound to determine their influence on the mechanical behavior of the different layers of the module.

5.2.5.1 Long heating phase t_{on}

Two simulations were performed with long heating phase t_{on} , the test parameters were: $T_{jmin} = -40^{\circ}\text{C}$, $\Delta T_j = 120\text{K}$ and $t_{on} = 100\text{s}$ and 1000s . The aim of these simulations is to determine if an increased t_{on} would induce some increase in the different stresses and strains in the structure studied. It permits also to see if such APC conditions with a large ΔT_j and long t_{on} are giving similar results than the ones obtained under PTC. Thus our different stress and strain indicators were analyzed in function of t_{on} . In the chip, no variations occur between 10s and 1000s for warpage, in-plane, out-of-plane and shear stresses. So, deformations and stresses in the chip are staying constants after 10s of heating pulse. The same occurs in the Al metallization and in the IMC. The acc plastic strain in the Al and the von Mises stress in the IMC are remaining constant after 10s of heating pulse. But the acc creep strains in solder layers continue to increase until 1000s and may be even after. The acc creep strain in the bottom solder in function of t_{on} is plotted Figure 5.55. One can see that between 10s and 1000s the acc creep strain doubled its value. Thus, the increase is not negligible. Actually, the increase of acc creep strain in function of the heating time can be predicted thanks to a logarithmic function. This prediction is only valid for our module and for cases with $T_{jmin} = -40^{\circ}\text{C}$, $\Delta T_j = 120\text{K}$.

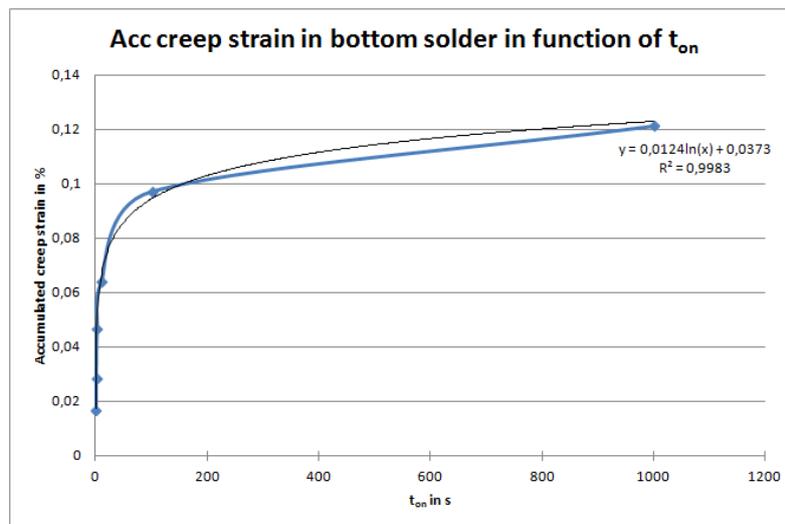


Figure 5.55: Accumulated creep strain in the bottom solder in function of the pulse width t_{on}

The acc creep strain for the top solder in function of t_{on} is also plotted Figure 5.56. For both paths in the top solder an increase of about 0,05% of acc creep strain occurs between 10s and 1000s. These creep increases can also be predicted by logarithmic functions. This continuous increase in creep strain is quite surprising, as this phenomenon does not appear under PTC. Indeed, if we look back at the Figure 5.26, where the evolution of temperature and acc creep strain in the bottom solder under PTC were plotted in function of the time, we can see that the creep strain was constant at constant temperature after about 100s. Thus under PTC the creep strain was quite rapid to stabilize. But this is not the case anymore under APC. This may come from the inhomogeneous temperatures induced by APC and not by PTC. It was seen in the chapter 3 concerning the thermal study of the module that chip heats up very quickly its metallization, its solders and clip, but the mold showed an important inertia. Actually the mold needs more than 100s to completely reach its thermal steady state. Thus the longer t_{on} is, the higher the temperature of the mold will be. And this increase of mold temperature may induce an increase in the acc creep strain for all solders, as they are all in direct contact with the mold. Here the case studied had $T_{jmin} = -40^{\circ}\text{C}$ and $\Delta T_j = 120\text{K}$, thus the maximum temperature that can be reached is 80°C , which remains well under the T_g of the mold and thus does not induce a drop down of the Young's modulus of the mold which may reduce the creep strain in the top solder.

For cases with $T_{jmin} = 10^{\circ}\text{C}$ or 60°C , $\Delta T_j = 120\text{K}$, a long t_{on} of 100s or 1000s, will not necessarily lead to an increase in creep strain as this time the temperature reached in the mold will be close to T_g and this may have some reducing effects on the creep strain.

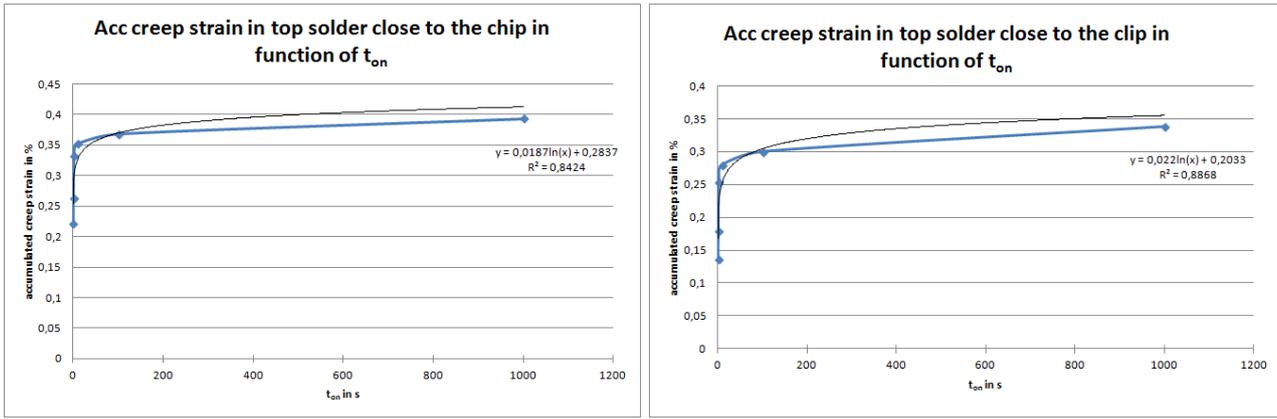


Figure 5.56: Acc creep strain in the top solder in function of t_{on} . One the left, the acc creep strain for the path close to the chip and on the right for the path close to the clip.

5.2.5.2 Long cooling phase t_{off}

One simulation was performed with a long cooling phase $t_{off} = 100s$ and $T_{jmin}=60^{\circ}C$, $\Delta T_j=120K$ and $t_{on}=0,2s$. Its results were compared to the ones coming from the equivalent case of the sensitivity study ($t_{off}=10s$ and $T_{jmin}= 60^{\circ}C$, $\Delta T_j=120K$ and $t_{on}=0,2s$). This allows checking if the fact that the mold almost reached its thermal steady state has an influence on the different stresses and strains in the module. With $t_{off}=100s$, the same results as with $t_{off}=10s$ were obtained for deformations and stresses in chip and stresses in IMC. Thus these indicators are not influenced anymore by the duration of the cooling phase when it exceeds 10s. But this long t_{off} induces less acc plastic strain in the Al metallization and more acc creep strain in the top solder.

First the acc plastic strain in Al metallization is plotted for the 2 different t_{off} on the Figure 5.57. It appears that with $t_{off}=100s$ the Al accumulates less plastic strain than with $t_{off}=10s$. This is surprising as it was seen that with long t_{on} the acc plastic strain reduces, thus a reduction of plastic strain was also expected with a long t_{off} . But this is not the case. This may be explained by a thermal effect. With $t_{off}=100s$, the mold, which is in the vicinity of the Al metallization, has more time to cool down, and thus reaches lower temperature than with a shorter t_{off} . Then by heating up, the mold will have a lower start temperature than with a shorter t_{off} , and will consequently reach a lower maximum temperature. This will then contribute to reduce the ΔT_j to which the Al metallization is submitted, thus leading to a reduced increase in the acc plastic strain. So in this case, thermal effects have more importance on the Al metallization behavior than time effects.

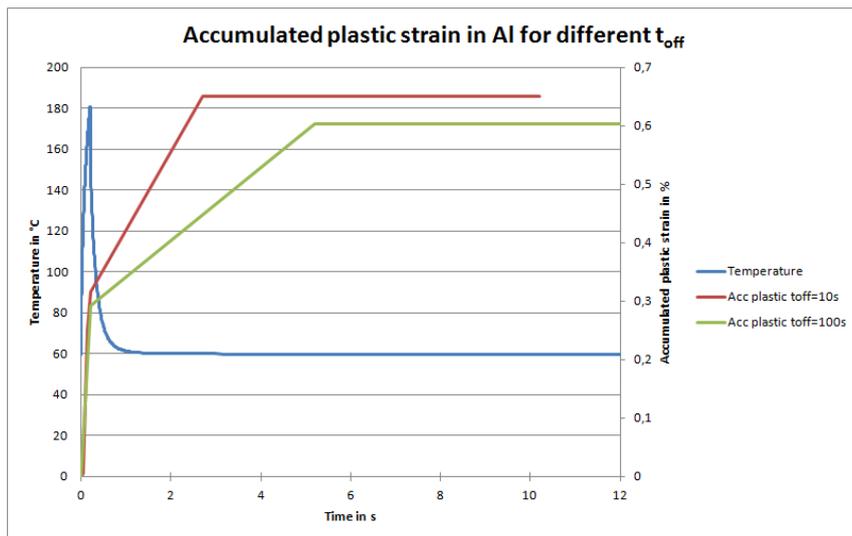


Figure 5.57: Acc plastic strain in the Al metallization in function of time for $t_{off}=10s$ and $100s$

Figure 5.58 shows the evolution of the acc creep strain in solders for different t_{off} . It appears that with $t_{off}=100s$, the top solder accumulates more creep strain than with $t_{off}=10s$. For the bottom solder the same amount of creep strain is accumulated for both t_{off} , but there is a slight increase in creep strain between 10s and 100s for the case with $t_{off}=100s$. These results are not surprising as it was seen that creep needs time to

accumulate and thus that long t_{on} are increasing the amount of acc creep strain. Hence an increase in the acc creep strain was also expected for an increase in t_{off} , and it is actually the case. For the top solder, one can see that the increase in creep strain is also higher for the path close to the clip than for the path close to the chip. For the path in the top solder close to the clip, there is 0,2% more creep strain after 10s for the case with $t_{off}=100s$ than for the case with $t_{off}=10s$. This is not negligible, and the acc creep strain still increase until the 100s of cooling phase. This increase in creep strain induced by a longer t_{off} can be explained by the fact that longer cooling phase leads to a colder mold. And, the lower the temperature of the mold is, the higher its Young's modulus will be. Thus, the less the mold will influence the creep behavior.

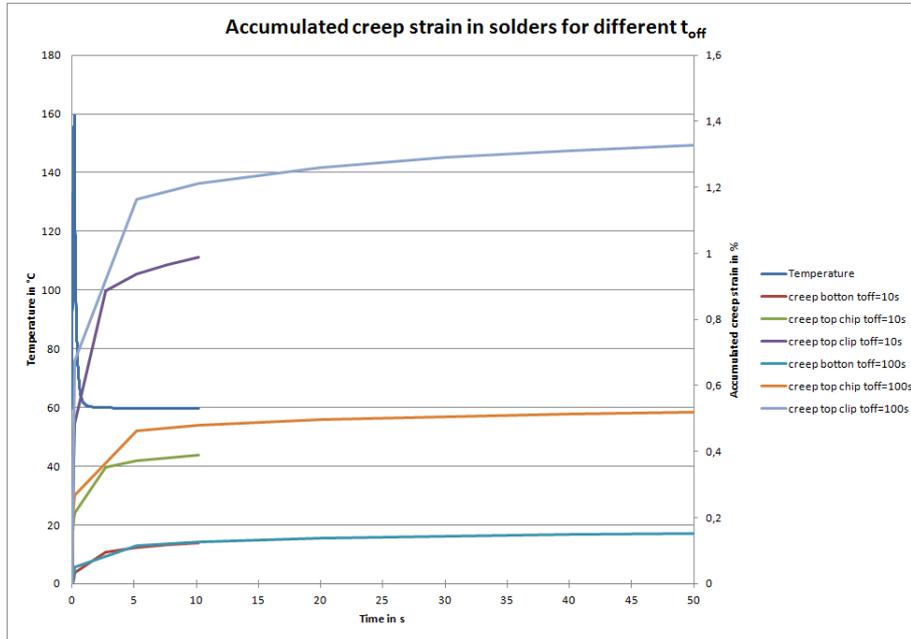


Figure 5.58: Acc creep strain in solder layers in function of time for $t_{off}=10s$ and $t_{off}=100s$

5.2.5.3 Short cooling phase t_{off}

After studying the influence of a long cooling phase on the module, the influence of a short cooling phase was also investigated. Thus a simulation was performed with $t_{off}=2s$ and $T_{jmin}=60^{\circ}C$, $\Delta T_j=120K$ and $t_{on}=0,2s$. Results obtained were compared to the ones coming from the equivalent case of the sensitivity study ($t_{off}=10s$ and $T_{jmin}=60^{\circ}C$, $\Delta T_j=120K$ and $t_{on}=0,2s$). First of all, the temperature at 2 nodes in the mold are plotted and compared to the temperature at one node in the chip (Figure 5.59). It appears that the temperature variations in the mold close to the chip are delayed in comparison to the ones occurring in the chip. Moreover one can see that the temperature of the mold close to the chip is slightly higher than the temperature of the chip itself. Thus, it is inducing a slight and continuous increase in mold temperature. Then, deformations and stresses in chip as well as stresses in IMC are found to be the same for both $t_{off}=2s$ and $t_{off}=10s$. Thus, those deformations and stresses are not influenced by the cooling duration when it exceeds 2s. On the contrary, a decrease in the acc plastic strain in Al metallization and in the acc creep strain in solder layers is observed with a shorter t_{off} . The acc plastic strain in Al is plotted Figure 5.60 for $t_{off}=10s$ and 2s. The case with $t_{off}=2s$, accumulates less plastic strain than the case with $t_{off}=10s$. This is surprising as short t_{on} are leading to more acc plastic strain, more plastic strain was expected as well with a short t_{off} . But this was not the case and it may be explained by a thermal effect. With a short t_{off} , the temperature of the mold slightly increases, and by an increase in the mold temperature a decrease in acc plastic strain occurs. So here thermal effects are dominant compared to times effects, regarding their influences on the Al metallization behavior.

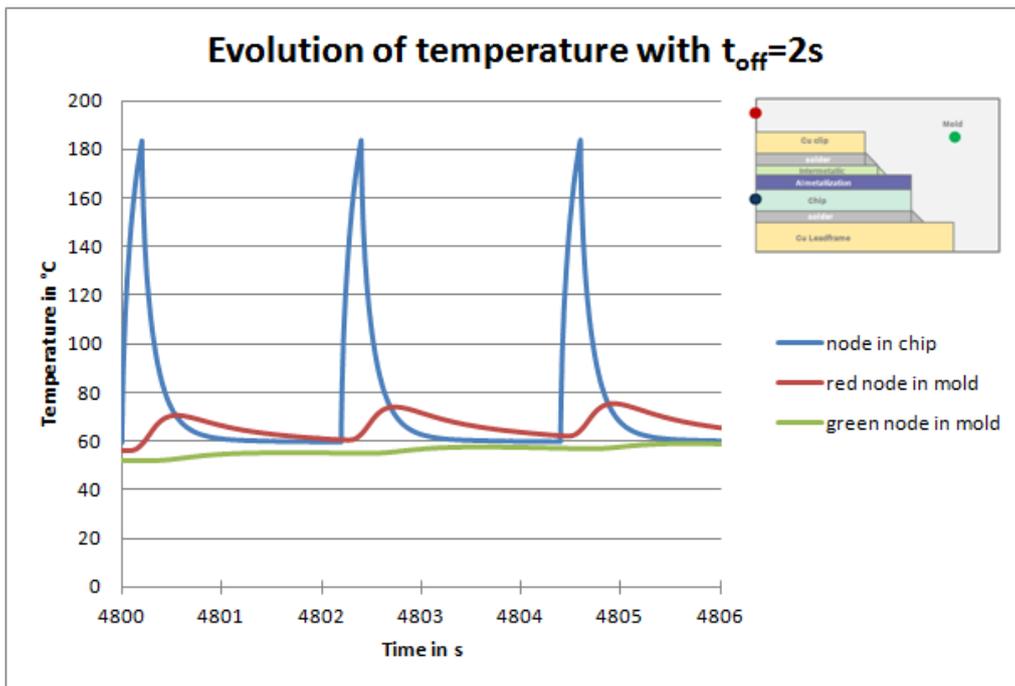


Figure 5.59: Evolution of the temperature at 1 node in the chip and 2 nodes in the mold

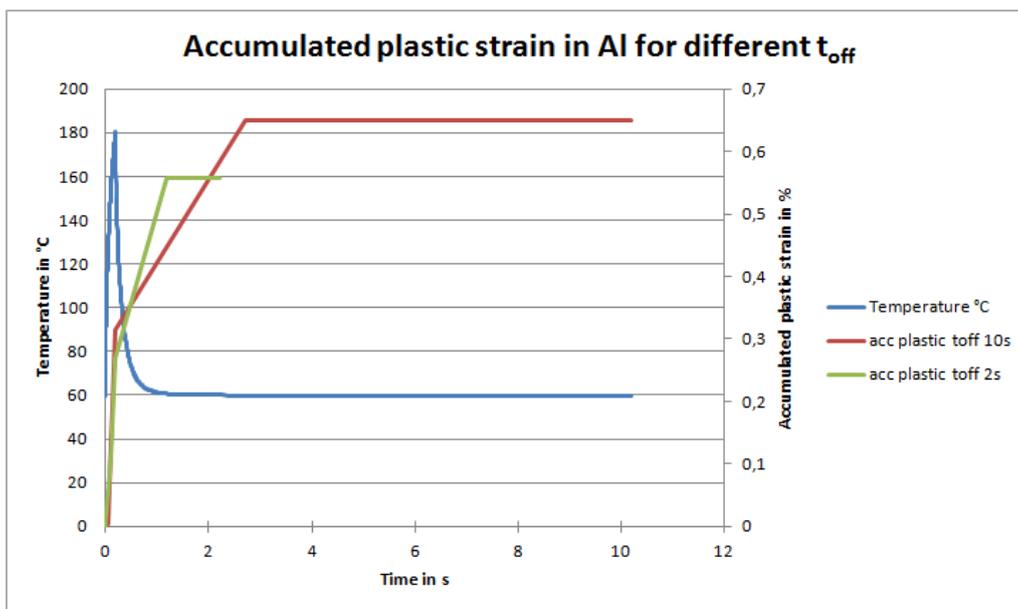


Figure 5.60: Evolution of acc plastic strain in the Al metallization for $t_{off}=10s$ and $2s$

The acc creep strain in solders is plotted for different t_{off} on the Figure 5.61. In the bottom solder whatever t_{off} , the acc creep strain stays constant. For the top solder, less creep strain is accumulated with $t_{off}=2s$ than with $t_{off}=10s$. This result was expected as short t_{on} are also leading to a reduced amount of acc creep strain. A difference of about 0,2% is noticed after 2s of cooling which is not negligible. This difference may come from the increasing temperature of the mold, which at $T_{jmin}=60^{\circ}C$ and $\Delta T_j=120K$ is close to T_g and thus leads to a drop down of the Young's modulus of the mold which may influence the creep behavior in the top solder. But this decrease in acc creep strain in the top solder was also seen for the case with $T_{jmin}= -40^{\circ}C$, $\Delta T_j=120K$ and $t_{on}=0,2s$. Thus, the drop down of the Young's modulus of the mold should not be the only effect.

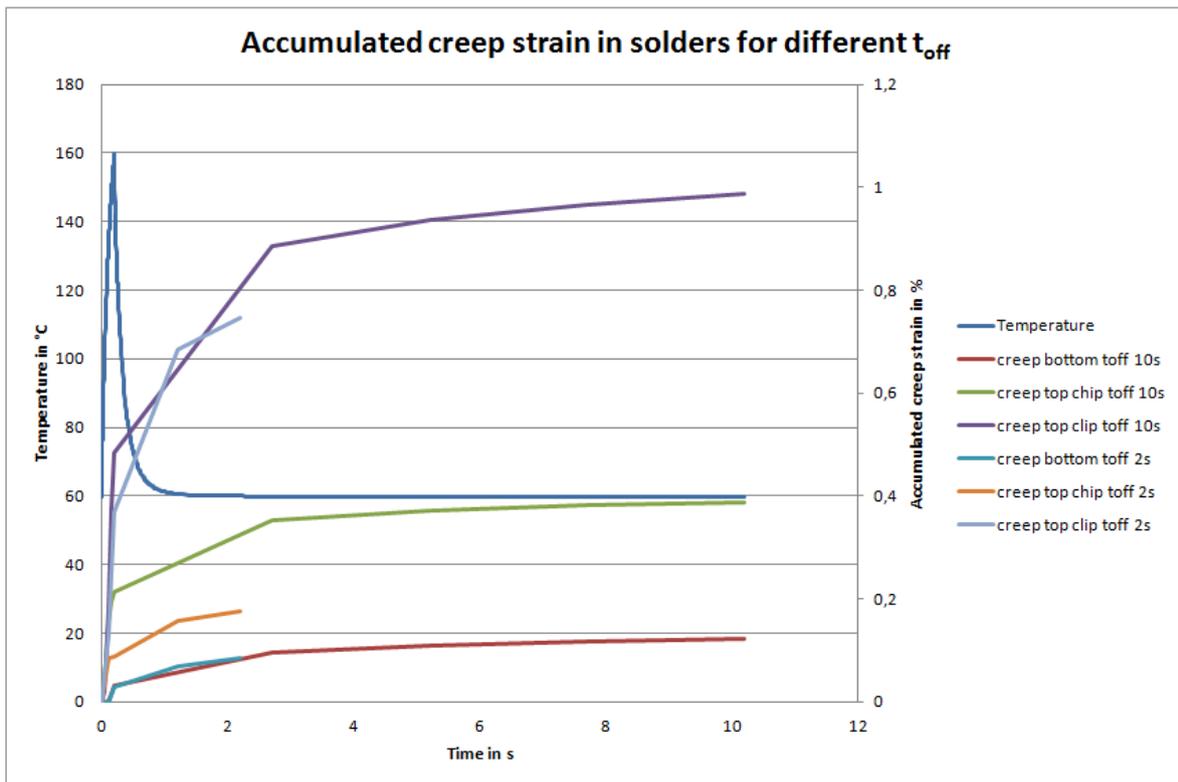


Figure 5.61: Evolution of acc creep strain in solder layers for $t_{off}=10s$ and $2s$

5.2.5.4 Thick Cu lead frame

2 cases of the sensitivity study were simulated with a thicker Cu lead frame. The Cu lead frame has more than doubled its thickness in comparison to the original model. It is interesting to study the effect of the Cu lead frame thickness on the module behavior has a reduction of warpage is expected, and this will certainly generate other variations in the module behavior. The 2 cases studied are the following:

Case 9: $T_{jmin} = -40^{\circ}C$, $\Delta T_j = 120K$ and $t_{on} = 0,2s$

Case 12: $T_{jmin} = -40^{\circ}C$, $\Delta T_j = 120K$ and $t_{on} = 10s$

First, the warpage in chip is plotted for the 2 cases with the 2 different Cu lead frame thicknesses Figure 5.62. For both case 9 and 12, the thick Cu lead frame reduces considerably the warpage amplitude. The bending down of the module at negative temperature is prevented through the thicker Cu layer, and the bending over is almost suppressed. On the contrary no significant changes were observed concerning the in-plane, out-of-plane and shear stresses in the chip. In the Al metallization, the thick Cu lead frame almost suppresses plastic deformations for the case 9, and halves them for the case 12 (Figure 5.63). These are considerable changes, and it leads to think that there is a relation between the amount of warpage and the percentage of acc plastic strain in Al.

Major changes are also occurring in solders (Figure 5.64). For the case 9, the thick Cu lead frame almost suppresses creep in all solder layers. On the contrary for the case 12, the influence of the thickness of the Cu lead frame is more complex. For the bottom solder, the acc creep strain increases due to the thicker lead frame. But for the top solder, the thicker lead frame reduces the percentage of acc creep strain. Thus it is difficult to draw some clear conclusions on the influence of the lead frame thickness on the creep behavior. More simulations have to be performed on this subject. The warpage has certainly an influence but some other parameters may also play a role.

Finally regarding the IMC stress no significant changes were observed due to the design variation.

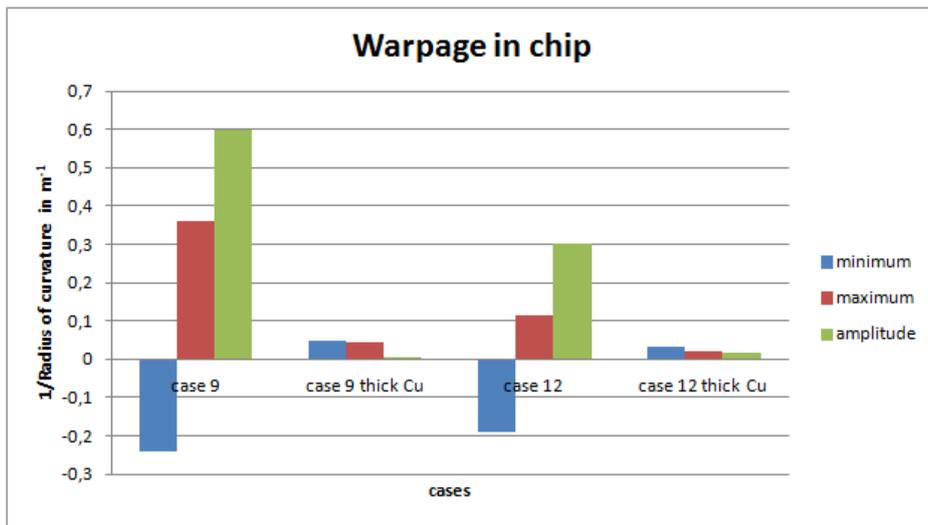


Figure 5.62: Warpage in the chip for different cases with different thicknesses for the Cu lead frame

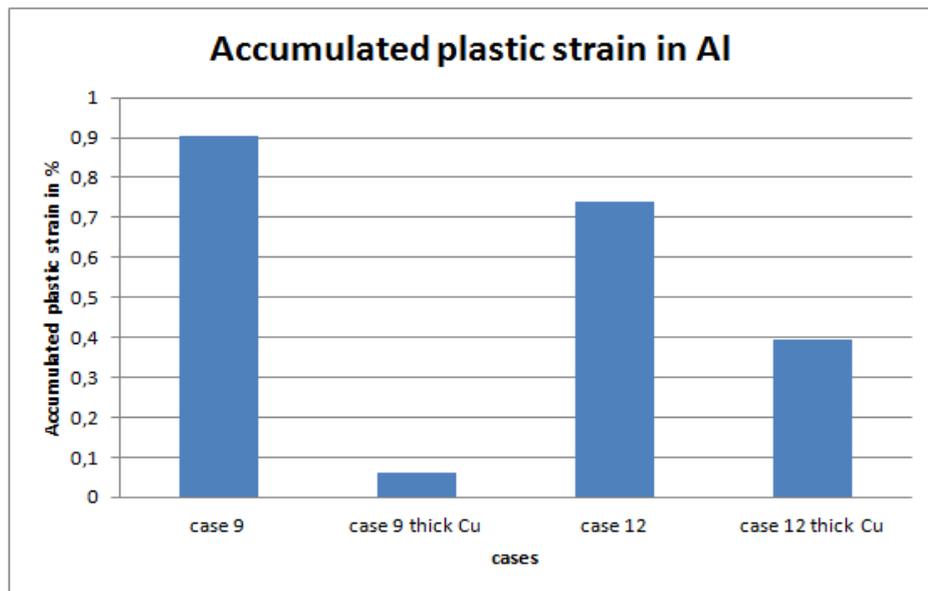


Figure 5.63: Acc plastic strain in the Al metallization for different cases with different thicknesses for the Cu lead frame

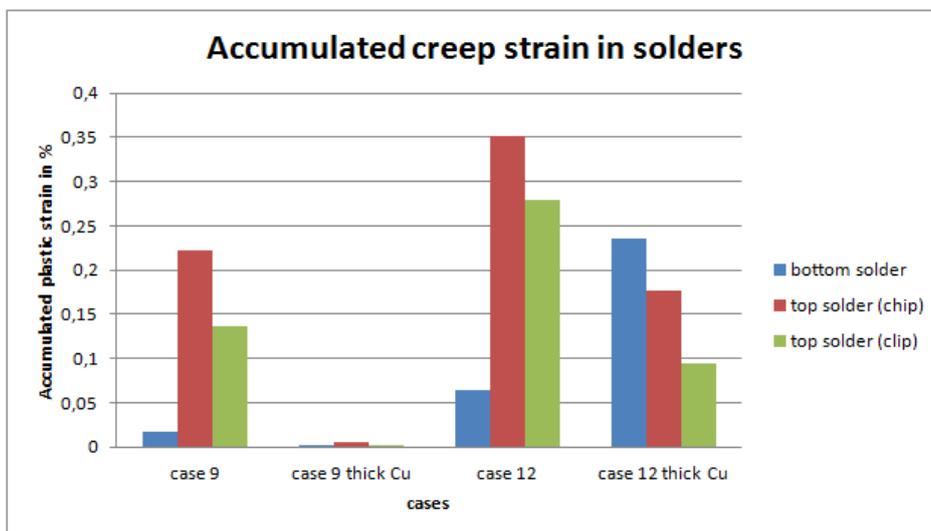


Figure 5.64: Acc creep strain in the solder layers for different cases with different thicknesses for the Cu lead frame

5.2.5.5 Very large ΔT_j

One case was simulated with a very large ΔT_j of 210°C, in order to determine if large ΔT_j are accelerating failure mechanisms and if it leads to results comparable to the ones obtained under PTC. This simulated case should also represent the 4 experimental tests that were performed with large ΔT_j . Thus the following parameters were chosen: $T_{jmin} = -20^\circ\text{C}$, $\Delta T_j=210\text{K}$ and $t_{on}=0,5\text{s}$. Results were then compared to the nearest case of the sensitivity study, which is the case 10 with $T_{jmin} = -40^\circ\text{C}$, $\Delta T_j=120\text{K}$ and $t_{on}=0,5\text{s}$, and to the results of PTC. The first major difference observed between the results of these 3 simulations concerns the warpage in the chip (Figure 5.65). The warpage amplitude with the large ΔT_j almost doubled compared to the warpage of case 10 and of PTC. Then, no bending down is observed with the large ΔT_j as $T_{jmin} = -20^\circ\text{C}$, and not -40°C as in the other cases. It can also be seen that there is an important difference between the warpage behavior under APC and under PTC. Indeed under PTC, $\Delta T_j=190^\circ\text{C}$, which is quite close to the APC case with ΔT_j of 210°C, but the warpage amplitude is even smaller as the one obtained under APC with ΔT_j of 120°C. Thus the loading conditions of APC with short heating times and an inhomogeneous temperature are generating more warpage than long ramping and dwell time and quasi-homogeneous temperature.

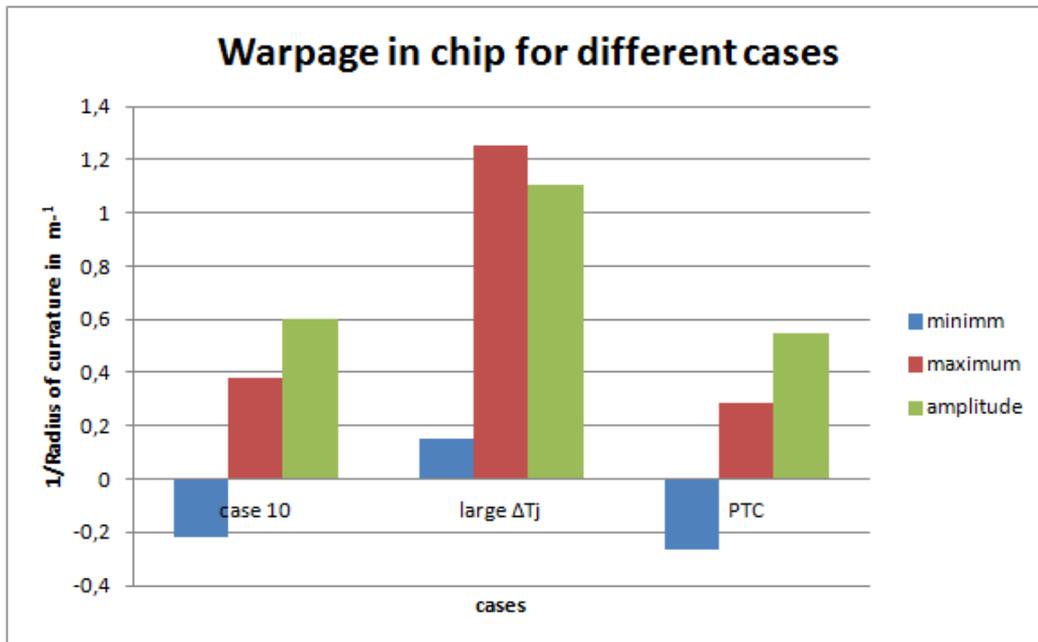


Figure 5.65: Warpage in the chip for different cases with different ΔT_j

No particularities were found concerning stresses in chip with large ΔT_j . In the Al metallization, major differences are noticeable. The acc plastic strain is plotted Figure 5.66 for the 3 different cases. For both PTC and the case 10 of APC, about 0,7% of plastic strain is accumulated whereas for the APC case with large ΔT_j , the plastic strain accumulated reaches 2,3%. This is already a huge increase. Once again, it is remarkable that despite the comparable order of ΔT_j , the behavior in the Al metallization is completely different between PTC and APC. This clearly shows that the plastic deformation of Al is a main failure mechanism under APC but not PTC. And performing APC test with large ΔT_j definitely accelerates failure mechanisms. It seems also to confirm that the amplitude of warpage is related to the plastic deformations in the Al metallization.

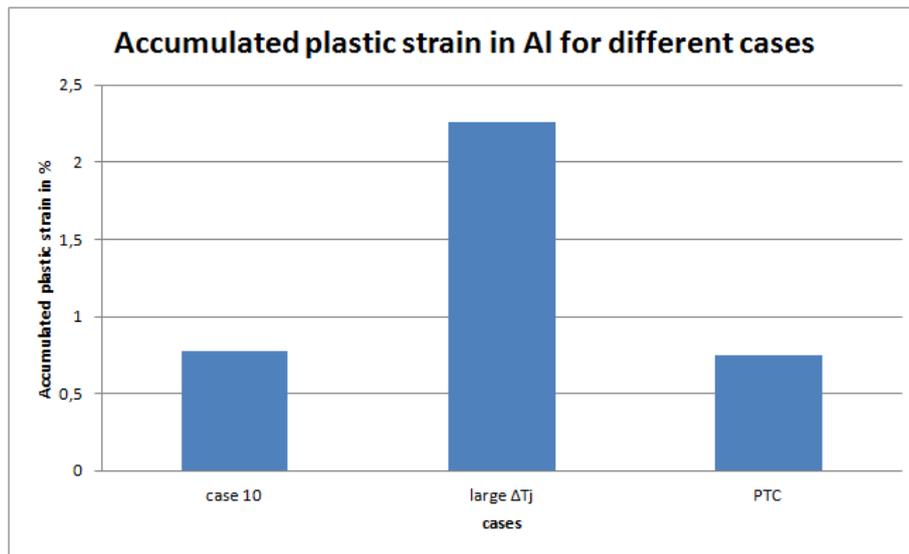


Figure 5.66: Acc plastic strain in the Al metallization for different cases with different ΔT_j

The 3 simulation cases are also showing differences concerning the creep behavior in solder layers (Figure 5.67). The acc creep strain in the bottom solder slightly increases under APC with a large ΔT_j , but it remains negligible in comparison to the creep strain accumulated under PTC. For the top solder, the acc creep strain along the path close to the chip is also increasing slightly with the increased ΔT_j and remains inferior to the 1% of acc creep strain reached under PTC. But along the path in the top solder close to the clip, a significant increase occurs with a large ΔT_j . For this path, the acc creep strain reaches 2%, when only 0,2% were attained for the APC case 10. This 2% are even surpassing the acc creep strain reached at the same place under PTC. This confirms the importance of creep strain in solder layers as failure mechanism occurring under APC. It also shows again, that large ΔT_j accelerates failure mechanisms. In the IMC an increase in the von Mises stress occurs with large ΔT_j , but it remains in the same order of magnitude as for the case 10.

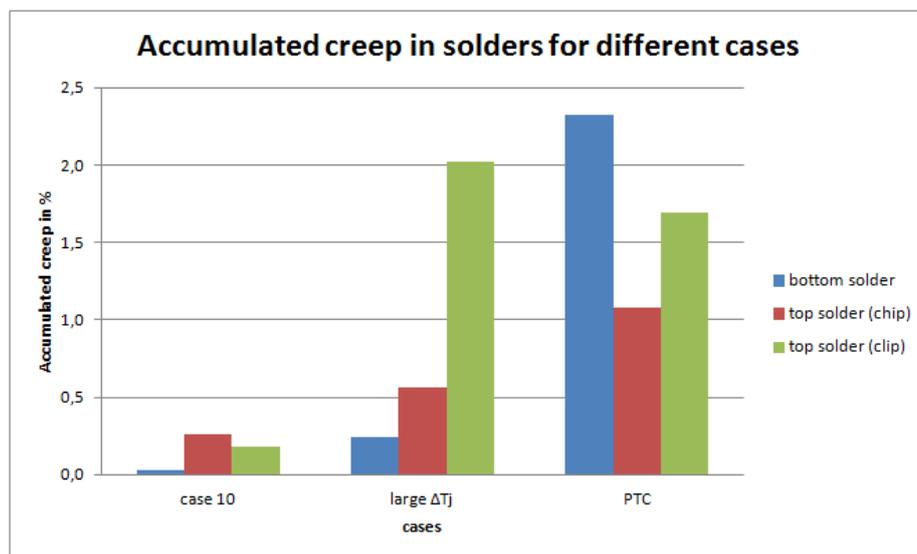


Figure 5.67: Acc creep strain in solders for different cases with different ΔT_j

This study with a simulated APC case with a large ΔT_j confirmed what was seen with the corresponding experiments. Namely, large ΔT_j accelerates failure mechanisms and leads to a rapid failure of the device, but the failure mechanisms occurring are still corresponding to the ones that are typically occurring for APC and not for PTC.

5.2.5.6 Delamination and cracks in the mold

Some simulations were performed with cracks modeled in the molding compound. First the influence of the crack position in the mold was studied. For that, 3 simulations were made with 1 crack in the mold defined at 3 different positions: position A, B and C. The length of the crack was defined to be 80% of the mold height, as shown Figure 5.68. One APC case was simulated: case 36 with $T_{jmin}=60^{\circ}C$, $\Delta T_j=120K$ and $t_{on}=10s$. Stresses and strains in the different layers were analyzed for each crack position, and were compared to each other. Significant differences occur only for plastic deformation in the Al metallization and creep strain in the top solder. For all other stresses and strains in the chip, the IMC and the bottom solder, the same results are obtained with or without cracks and whatever the crack position. The acc plastic strain in the Al decreases slightly when a crack in the mold exists (Figure 5.69). The crack at the position B induces the biggest decrease, with only 0,03% of acc plastic strain lost. This can be explained by the fact that the crack B is the closest one to the critical area of the Al metallization. But still the plastic strain variations are remaining quite small. Then, in the top solder, the presence of a crack in the mold at the position A induces only a slight increase in the acc creep strain in the top solder close to the clip (Figure 5.70). The crack at the position B induces an increase in the acc creep strain for the path in the top solder close to the chip. Finally the crack located at the position C induces a slight increase in acc creep strain for both paths of the top solder. Here also the increase in acc creep strain is staying small.

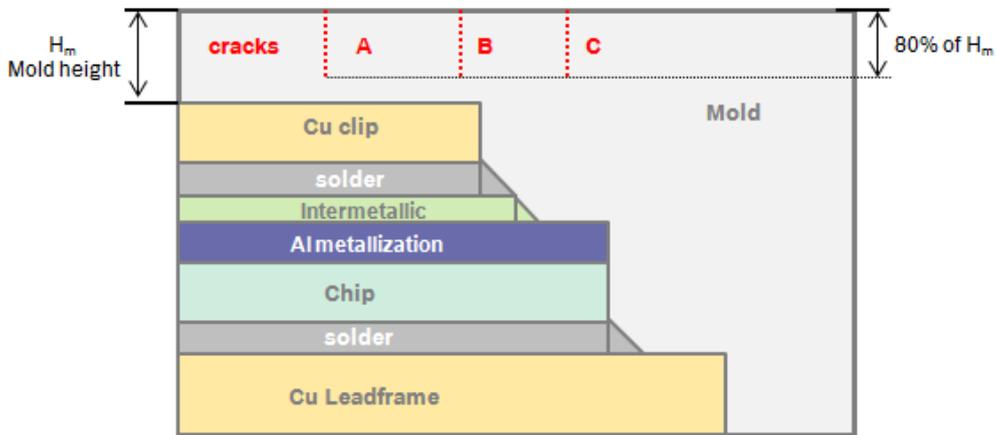


Figure 5.68: Scheme showing the different crack positions A, B and C in the mold

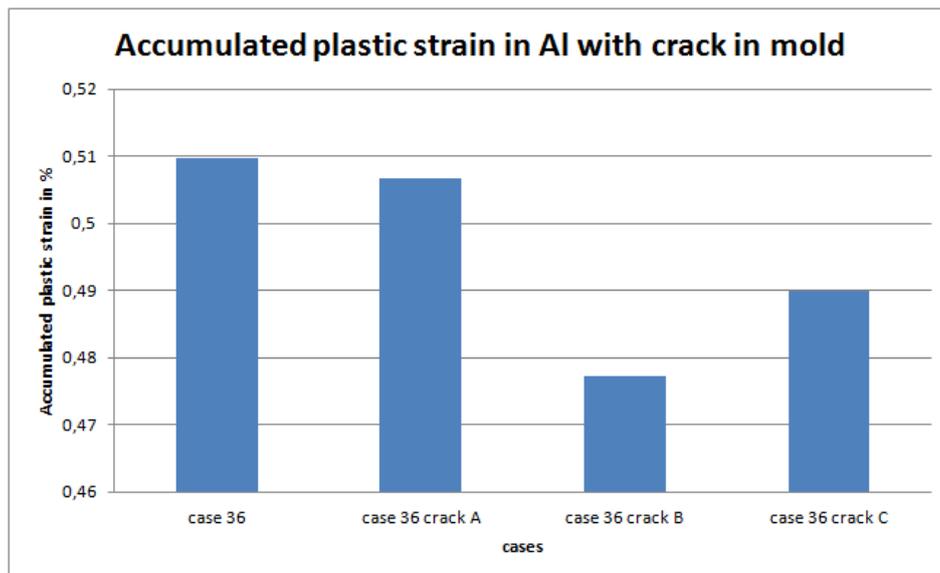


Figure 5.69: Acc plastic strain in the Al metallization with crack in the mold at different positions

After that, we wanted to determine if a longer crack in the mold would have more influence on the module behavior. For that, the crack at the position A was extended so that its crack tip reached the Cu clip. This meaning that the crack length was equal to the mold height. This elongated crack produces only minor

changes: the acc plastic strain in Al is further reduced of 0,01%, and the acc creep strain in the top solder close to the clip is further increased of 0,03%, compared to the original crack A.

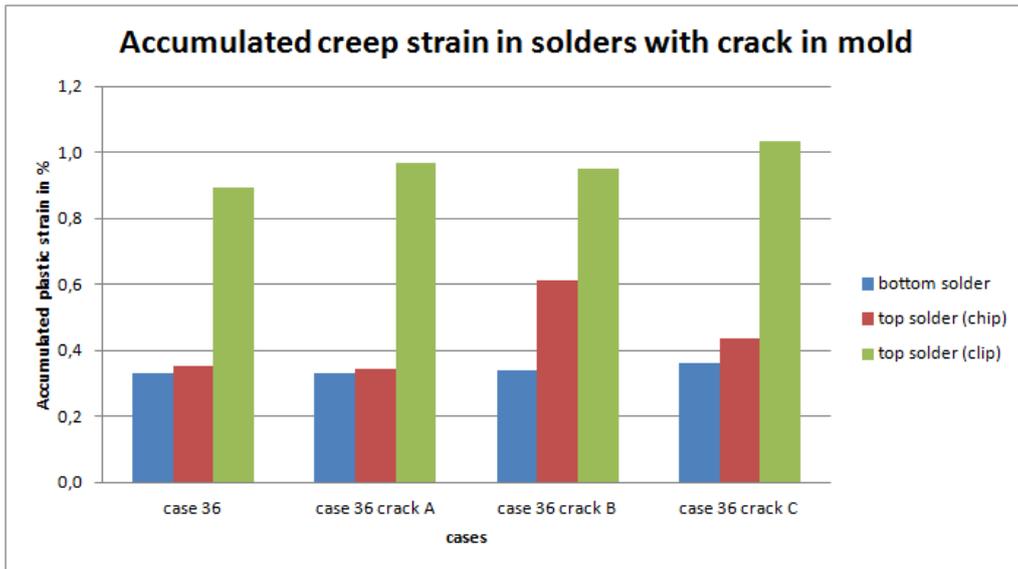


Figure 5.70: Acc creep strain in the solder layers with crack in mold at different positions

Thus it can be concluded that cracks in mold have only minor influences on the module behavior whatever their positions and lengths.

In experiments quite often delamination was observed between the mold and solders meniscus, Cu clip and Cu lead frame. The influence of these delaminations on the module behavior was also studied. Simulations were performed with these delaminations alone, and in combination with cracks: extended crack at the position A, crack along the Cu clip, crack along the Cu lead frame and all cracks together (Figure 5.71). Delaminations in combination with cracks or not, are inducing a slight increase in the warpage amplitude. The in-plane stress in the chip does not change due to the presence of delaminations and cracks, but the out-of-plane and shear stresses do. The out-of-plane stress in the chip at the interface with mold reaches negative values with decreased stress amplitude for all cases with delamination. This is an important change in the behavior at the interface chip/mold, coming from the fact that delaminations are giving more degrees of freedom to the mold. Thus the mold can move more independently to the rest of the module, leading to decreasing stresses. A similar phenomenon is observed for the shear stress in the chip close to the interface with the bottom solder meniscus. Minimum values of stress are negative there and the amplitude of shear stress decreases for all cases with delamination.

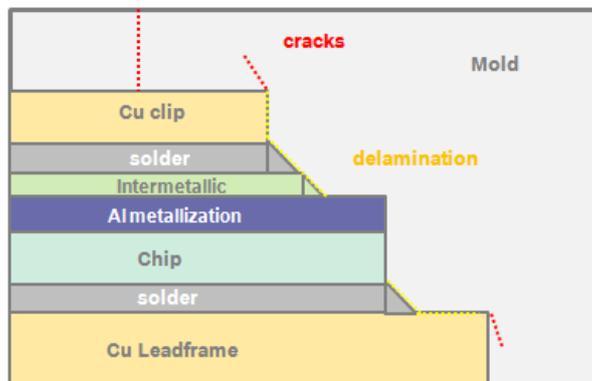


Figure 5.71: Scheme of delamination and cracks in mold

In the Al metallization the acc plastic strain increases with the presence of delamination in the module. The plastic strain can increase between 0,3 to 0,4%, which is not negligible. It can be noticed that cases with cracks at the position A or along the Cu clip are leading to the biggest increase in acc plastic strain. Thus, it can be concluded that the crack along the Cu lead frame has no influence on the plastic deformations in Al.

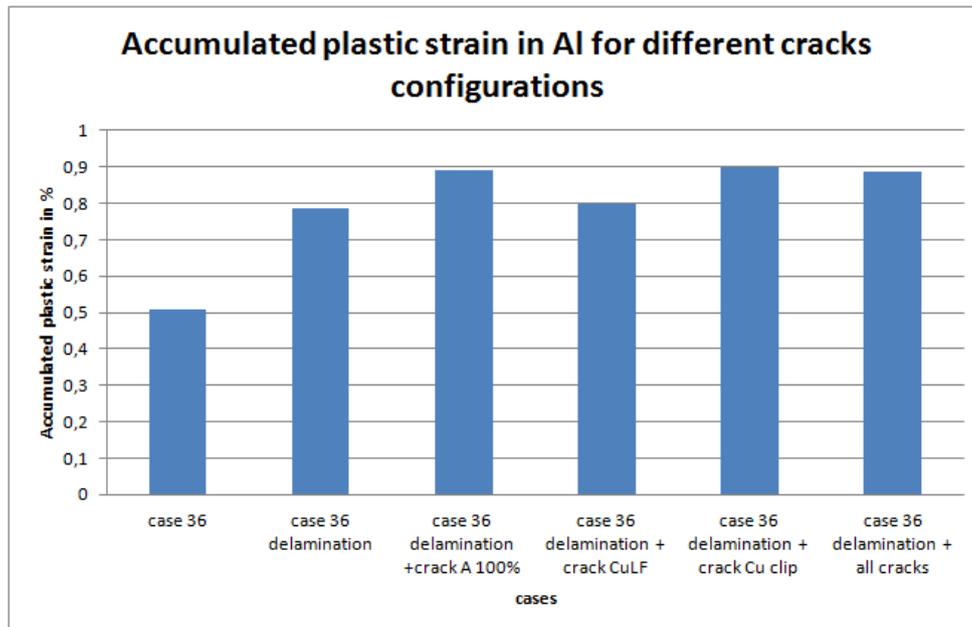


Figure 5.72: Acc plastic strain in the Al metallization for different cracks configurations

Concerning the effects of delaminations and cracks on the solder layers behavior, it is more complex (Figure 5.73). Each crack configuration leads to a different result. First we look at the creep behavior of the bottom solder. All cracks configurations are leading to an increase in the acc creep strain in the bottom solder. It attains values ranging from 0,8% to 1%, whereas without delaminations or cracks, the acc creep strain represented only 0,3%. Thus delaminations and cracks are generating a consequent increase of acc creep strain in the bottom solder. Delamination alone, leads to an acc creep strain of 0,8%. Then it can be observed that the additional presence of a crack at the position A or along the Cu lead frame is leading to the highest amount of acc creep strain, 1%. On the contrary a crack along the Cu clip does not affect the creep behavior of the bottom solder.

For the top solder close to the chip, delamination alone or in combination with a crack along the Cu lead frame are decreasing the acc creep strain. On the contrary delamination combined with a crack at the position A or along the Cu clip are increasing the acc creep strain and it can reach a value of 1,5%, which is quite high. When all cracks are occurring simultaneously the acc creep strain increases but reaches the moderate value of 1%. Thus an accumulation of cracks lead not necessarily to the worst situation in terms of creep.

The top solder close to the clip is subjected to an important increase of acc creep strain for all cracks configurations. Without any cracks the acc creep strain represented less than 0,9%, whereas with delamination and cracks it ranges from 2,6% to 3%. These values are really high and may be critical. With delamination alone, 2,6% of creep strain is accumulated, thus the presence of delamination plays a major role in the increase of acc creep strain. The same value of 2,6% is reached with delamination and a crack along the Cu lead frame. One can conclude that crack along the Cu lead frame are not influencing the creep behavior of the top solder. On the contrary the presence of cracks at the position A or along the Cu clip is leading to the highest value of acc creep strain. When all cracks are present simultaneously the creep strain accumulated is between 2,6% and 3%, so here also the cracks accumulation is not the worst case as cracks have sometimes opposite effects.

Finally, the von Mises stress in the IMC increases slightly and reaches the same values for all crack configurations.

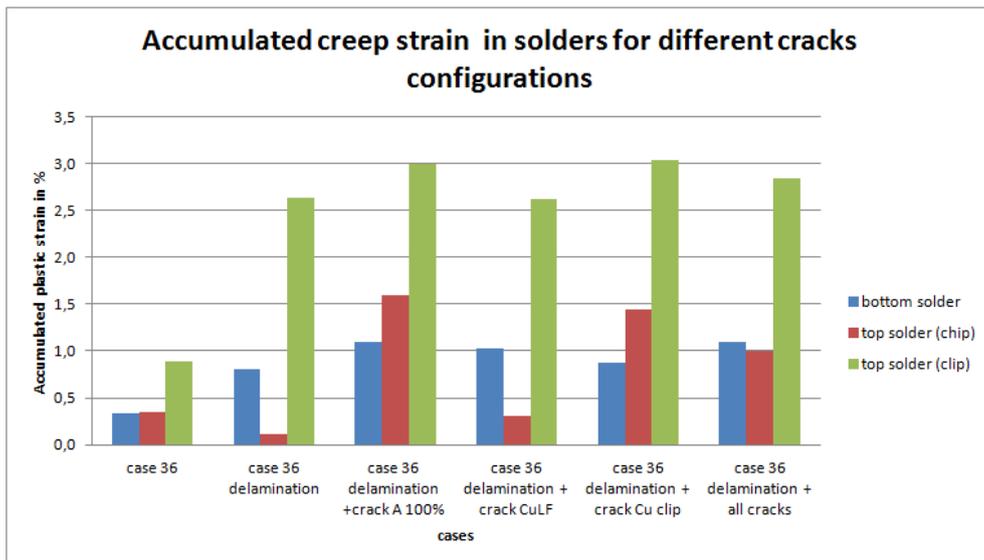


Figure 5.73: Acc creep strain in solder layers for different cracks configurations

This study revealed that cracks in mold alone are not leading to big changes in the module behavior and thus are not critical. But delamination alone or combined with cracks can heavily modify the module behavior. Delaminations with cracks along or above the Cu clip are critically increasing the amount of plastic deformations in the Al metallization and the amount of acc creep strain in all solder layers. On the contrary cracks along the Cu lead frame are not critical even combined to delamination. When all cracks are present simultaneously it does not necessarily mean that it is the worst case. Indeed, some cracks are having opposite effects, thus different negative effects are sometimes compensating each other.

These results are confirming what was already observed with experiments, that is to say: delamination and cracks in mold are leading to more degradations in solder layers. Nevertheless these numerical results were obtained for only one case of the sensitivity study, but with different APC conditions, results may vary.

6 Fracture mechanics simulations

6.1 Fracture mechanics model

6.1.1 Selection of failure mechanisms

As seen previously with experiments, when the B6 Bridge is submitted to APC, several failure mechanisms can occur: cracks in chip, delamination at the interface mold/Cu, cracks in solder layers, cracks in the molding compound, delamination at the interface Al metallization/top solder, cracks in the Al metallization and delamination at the interface IMC/solder or cracks in IMC. But some of these failures are not typically occurring under APC and some other are already extensively studied. Thus a selection of failure mechanisms was done and 3 failure mechanisms were retained to be modeled and simulated with FEM.

To operate the selection, the different failure mechanisms seen in experiments are analyzed one by one. First cracks in chip rarely occur and thus are not a systematical failure in the B6 Bridge. The delamination at the interface mold/Cu is already the main interest of numerous experimental and numerical studies. Numerically, this delamination is often analyzed with the Cohesive Zone Elements (CZE) method. Cracks in solder layers are important failure mechanisms, but the analysis of the acc creep strain at critical zones provides already good results, thus there is no need for another fracture criterion. Cracks in mold usually rarely occur and their consequences on the module behavior were already studied in the previous chapter. Delamination at interface top solder/Al metallization and cracks in Al metallization are major failure mechanisms occurring under APC. Therefore it was chosen to simulate a crack in the Al metallization. Delamination at the interface IMC/solder and cracks in IMC are also of importance, thus a crack in the top IMC was modeled. Finally a delamination between the chip and the bottom IMC layer underneath the chip is also simulated. This failure was never observed for the B6 Bridge module, but used to be an important issue for other modules. Thus the results obtained for that crack can serve as indicators for the design of new power modules.

So the 3 failure mechanisms modeled and simulated with FEM are:

- Delamination at the interface chip/IMC
- Crack in the Al metallization
- Crack in the top IMC

6.1.2 2D fracture mechanics models

For the simulation of these 3 failure mechanisms, 2 models were required. Indeed, the crack in the Al metallization and the crack in the top IMC were too close to each other, thus reciprocally influencing their behavior. This would have altered the results for both cracks. The first model includes the delamination at the interface chip/bottom IMC and the crack in the top IMC, while the second includes the crack in the Al metallization. Both models are 2D axisymmetric just like for the thermo-mechanical simulations. The delamination at the interface chip/bottom IMC starts at the extremity of both layers and propagates toward the center of the chip. The crack in the Al metallization is modeled in the middle of the layer thickness, starts under the top solder meniscus and propagates through Al toward the center of the module. The crack in the top IMC is modeled in the middle of the layer thickness, starts at its meniscus and propagates toward the center of the module. In both models, the delamination between the molding compound and the different solders meniscus, appearing after APC, is also taken into account. All cracks have a fixed length of 150 μm and were defined using contact and target elements with a friction coefficient to prevent material penetration. Here some simulations were performed with varying coefficients of friction and results were not found to be dependent on this value. Thus, the coefficient of friction was arbitrary fixed to 0,2. As the study focuses here on the stress state at the crack tip area, the global mesh of both models is coarser than the mesh of the model shown in the previous chapter. On the other hand, the mesh is refined at every crack tips. In this area, elements are square with a length of about 0,3 μm . The first model with delamination at the interface chip/bottom IMC and crack in the top IMC contains 7908 elements (Figure 6.1). The second model with the crack in Al metallization has 7793 elements (Figure 6.2). For both models, elements do not show disproportionate aspect ratios.

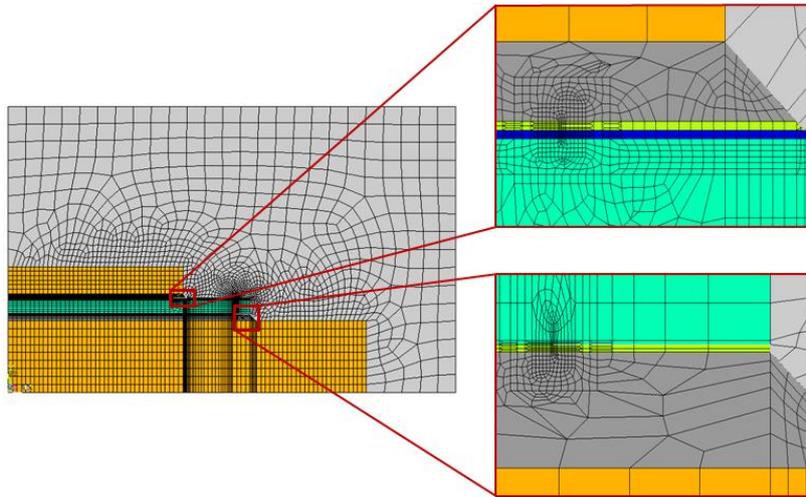


Figure 6.1: Global view of the mesh with zooms at the crack tip area in the top IMC upward, and at the delamination at the interface chip/bottom IMC downward.

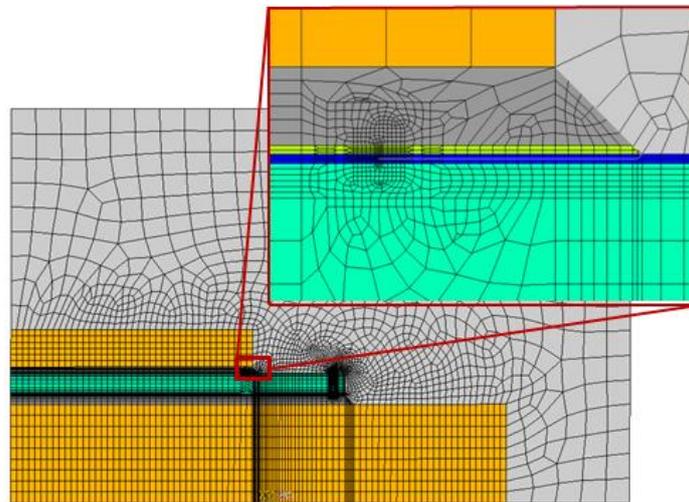


Figure 6.2: Global view of the mesh with a zoom at the crack tip area in the Al metallization

The type of element used remains the same as what was defined in the previous chapter: for PTC, Ansys PLANE183 elements with midside nodes are used, and for APC in the thermal study, PLANE 77 elements are used and are then replaced by PLANE 183 for the static-structural analysis. The loading conditions for PTC and APC are also remaining the same as what was defined in the previous chapter.

6.1.3 Selection of fracture criteria

To interpret cracks growth, fracture mechanical criteria have to be defined. Depending on the model and on the type of analysis performed, those fracture criteria have to fulfill some requirements. In our case, fracture criteria have to be compatible with an axisymmetrical model, and to allow cyclic loading. Moreover some additional requirements are coming from the material in which the crack is located.

For the delamination at the interface chip/bottom IMC, the fracture criterion has to work for material interface. The Cohesive Zone Element (CZE) method is adequate for delamination at material interface, but the method does not work under cyclic load. Another method that could work is the Virtual Crack Closing Technique (VCCT), but not the one already implemented in Ansys under the command “CINT”. Indeed this one is not compatible with axisymmetrical model but only with plane stress and plane strain models. Thus a mixed mode fracture criterion using the VCCT can be manually implemented to interpret the delamination at the interface chip/bottom IMC.

For the crack in the Al metallization, a criterion supporting non linear material properties is required, as the Al is an elasto-plastic material. Thus, only the J-integral, the Crack Tip Opening Displacement (CTOD) and the CZE method are applicable. But the J-integral and the CZE methods are not working for cyclic loads. On the

other hand, the CTOD criterion allows cyclic loading and axisymmetric conditions when manually implemented. Thus, a mixed mode fracture criterion manually implemented using the CTOD at a fixed distance behind the crack tip can be used to interpret the crack growth in the Al metallization. Finally for the crack in the top IMC, the choice of fracture criterion is easier as the IMC is a linear elastic material. Thus many methods are available to interpret this crack, like the K factor, the J integral, the VCCT, or even the CTOD. But as seen before, the J integral is not appropriate for cyclic loading, thus this method should be eliminated. All other methods are acceptable, but as the VCCT method was already used for the delamination between the chip and the bottom IMC, this method was also chosen for this case.

6.1.4 Definition of fracture criteria

6.1.4.1 Virtual Crack Closing Technique (VCCT)

The VCCT was initially developed to calculate the Energy Release Rate (ERR) G of a cracked body. It has since been widely used in the interfacial crack growth simulation of laminate composites, with the assumption that crack growth is always along a predefined path, specially the interfaces.

VCCT is based on the assumption that the energy needed to separate a surface is the same as the energy needed to close the same surface. The manual implementation uses the modified crack closure method and assumes further that stress states around the crack tip do not change significantly when the crack grows by a small amount (Δa). G for mode I opening and mode II shearing is calculated as follow in 2D [Kru04] (Figure 6.3 and Eq. 6.1, Eq. 6.2, and Eq. 6.4):

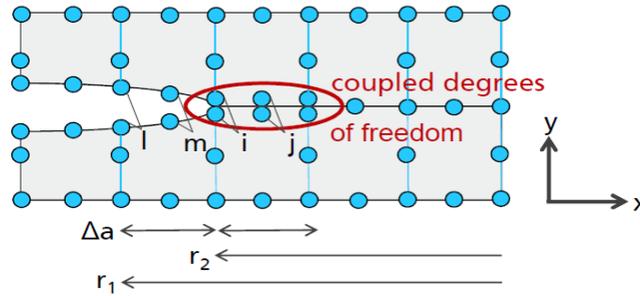


Figure 6.3: Scheme of the 2D crack geometry

$$G_I = - \frac{F_{y,i} \cdot \Delta u_{y,l} + F_{y,j} \cdot \Delta u_{y,m}}{2\Delta A} \quad \text{Eq. 6.1}$$

$$G_{II} = - \frac{F_{x,i} \cdot \Delta u_{x,l} + F_{x,j} \cdot \Delta u_{x,m}}{2\Delta A} \quad \text{Eq. 6.2}$$

$$G_T = G_I + G_{II} \quad \text{Eq. 6.3}$$

Where G_T is the total strain energy release rate, F are the reactions forces at crack tip nodes, Δu the relative displacements between the top and bottom nodes of the crack face, ΔA the crack area determined by the following formulas for an axisymmetric conditions:

$$\begin{aligned} \Delta A &= \pi \cdot (r_1^2 - r_2^2) = \pi \cdot \left[(r_{crack\ tip} + l_{element})^2 - r_{crack\ tip}^2 \right] \\ &= \pi \cdot (2 \cdot r_{crack\ tip} \cdot l_{element} + l_{element}^2) \end{aligned} \quad \text{Eq. 6.4}$$

Where $r_{crack\ tip}$ is the crack tip radius and $l_{element}$ the element's length.

In order to predict delamination onset and growth for 2D problems, the calculated G components are compared to interlaminar fracture toughness properties measured over a range from pure mode I loading to pure mode II loading. Failure is expected when, for a given mixed-mode ratio G_{II}/G_T , the calculated total energy release rate G_T , exceeds the interlaminar fracture toughness G_c [Kru04]. Here the fracture toughness is not known neither for the crack in the top IMC nor for the delamination at the interface chip/bottom IMC. But we do already know that the values reached for the delamination at the interface chip/bottom solder are not

critical as this failure was not observed experimentally. Concerning the crack in the IMC, it can also be supposed that the crack will remain subcritical. Anyways even if the fracture toughness is not known, it is still interesting to analyze the influence of the various test parameters from the sensitivity study on the evolution of the G component value.

6.1.4.2 Crack Tip Opening Displacement (CTOD)

The CTOD analysis takes place at a pair of nodes at a fixed distance in front of the crack tip as shown Figure 6.4.

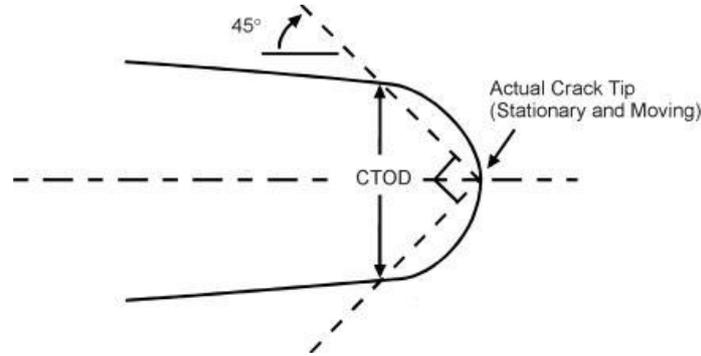


Figure 6.4: Scheme of the definition of crack tip opening displacement (CTOD)

For a linear-elastic case, the CTOD can be converted to K factor with the following formulas:

$$CTOD_1 = \Delta u_y(x_c) = \frac{\kappa + 1}{\mu} \sqrt{\frac{x_c}{2\pi}} \cdot K_1 \quad Eq. 6.5$$

$$CTOD_2 = \Delta u_x(x_c) = \frac{\kappa + 1}{\mu} \sqrt{\frac{x_c}{2\pi}} \cdot K_2 \quad Eq. 6.6$$

Where x_c is the fixed distance in front of the crack tip at which the analysis takes place, μ is the shear modulus and κ is the elastic constant. The shear modulus μ is equal to:

$$\mu = G = \frac{E}{2(1 + \nu)} \quad Eq. 6.7$$

Where E is the Young Modulus and ν is the Poisson's coefficient. And κ the elastic constant is equal to:

$$\kappa = \begin{cases} 3 - 4\nu, & \text{for plane strain} \\ \frac{3 - \nu}{1 + \nu}, & \text{for plane stress} \end{cases} \quad Eq. 6.8$$

These formulas above are only valid for linear elastic problems but not for elasto-plastic materials like our Al metallization.

The CTOD criterion [Ma99] states that crack growth occurs when the current CTOD reaches a critical value and the direction of crack growth is the direction that leads to the maximum opening or shearing CTOD component value at the new crack tip. In our case, the critical value of the CTOD is not known, but the crack growth in Al will probably be subcritical and it is still interesting to see the influence of the various test parameters from the sensitivity study on the evolution of the CTOD component value.

6.1.5 Validation of the fracture criterions implementation

Before to be able to start the simulations, the implementation of the different methods have to be validated. Indeed the mesh at the crack tip areas and the distance at which the CTOD analysis takes place x_c have to be optimized to provide precise results. For the validation of the VCCT and CTOD implementation, a case of a Compact Tension Shear (CTS) sample is taken as a reference and is simulated (Figure 6.5). Values of K factor are calculated for both CTOD and VCCT methods and are compared to the analytical solution taken as a reference. The analytical formulas are given by [Ric85]:

$$K_1 = \frac{F}{wt} \cdot \sqrt{\pi a} \cdot \frac{\cos \alpha}{1 - \frac{a}{w}} \sqrt{\frac{0,26 + 2,65 \cdot \frac{a}{w-a}}{1 + 0,55 \cdot \frac{a}{w-a} - 0,08 \cdot \left(\frac{a}{w-a}\right)^2}} \tag{Eq. 6.9}$$

$$K_2 = \frac{F}{wt} \cdot \sqrt{\pi a} \cdot \frac{\sin \alpha}{1 - \frac{a}{w}} \sqrt{\frac{-0,23 + 1,40 \cdot \frac{a}{w-a}}{1 - 0,67 \cdot \frac{a}{w-a} + 2,08 \cdot \left(\frac{a}{w-a}\right)^2}} \tag{Eq. 6.10}$$

Where F is the force applied, α the angle formed between the direction perpendicular to the crack and the direction of the applied forces, a the crack length, w the width of the sample and t its thickness. With the CTOD method, values of displacements are converted into K factor according to the formulas shown previously (Eq. 6.5 and Eq. 6.6). For the VCCT the following formulas allow to convert the energy release rate components in K factor components:

$$G_I = \frac{K_I^2}{E} \text{ and } G_{II} = \frac{K_{II}^2}{E} \tag{Eq. 6.11}$$

K factors for different loading cases were calculated with the analytical formulas, the CTOD and the VCCT methods and were compared to each other. Results are summarized in Table 6.1. There are only minor differences between analytical and numerical calculus for the different loading cases, thus the implementation of both the CTOD and the VCCT method is validated.



Figure 6.5: Schematic and picture of a CTS specimen [Ric85] and its corresponding FE model

case	K1 (MPa/mm ^{0.5})			K2 (MPa/mm ^{0.5})		
	Analytic	CTOD	VCCT	Analytic	CTOD	VCCT
F=50, α=45	28	26	28	14	13	14
F=100, α=45	56	52	56	28	27	27
F=100, α=0	79	74	79	0	0	0
F=100, α=90	0	0	0	39	38	38

Table 6.1: Comparison of K factor values obtained with analytical formulas and CTOD and VCCT methods

6.2 Crack growth under PTC

Just as defined in the previous chapter for thermo-mechanical simulations, 6 PTC cycles are simulated with temperature changes from -40°C to 150°C (Figure 5.2).

6.2.1 Crack growth at the interface chip/IMC

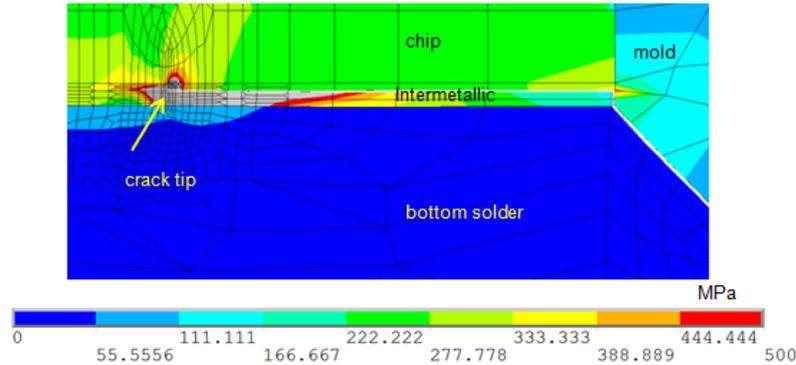


Figure 6.6: von Mises stress at the crack tip at the interface chip/IMC after PTC (areas in grey have a von Mises stress superior to 500MPa)

After the simulation of 6 PTC cycles, the crack at the interface chip/IMC is open (Figure 6.6). Then, the Energy Release Rate (ERR) is calculated for both opening and shearing modes and their evolutions are plotted respectively Figure 6.7 and Figure 6.8. For the opening mode, a negative G_I represents a crack closing and a positive G_I represents a crack opening. In that case the crack remains always open whatever the temperature. At high temperature, the crack is almost close and at low temperature the crack is open at its maximum. It can be observed that at dwell times, G_I is not constant and continues to vary but with a gentler slope as the one of ramping time. This means that the crack is always evolving, either further growing or further closing. The system seems to be stable already after the first cycle as the minimum and maximum values are staying constant cycles after cycles. The values reached by G_I are quite low compared to the ones reached by G_{II} for the shearing mode. Indeed G_{II} is about 4 times higher than G_I .

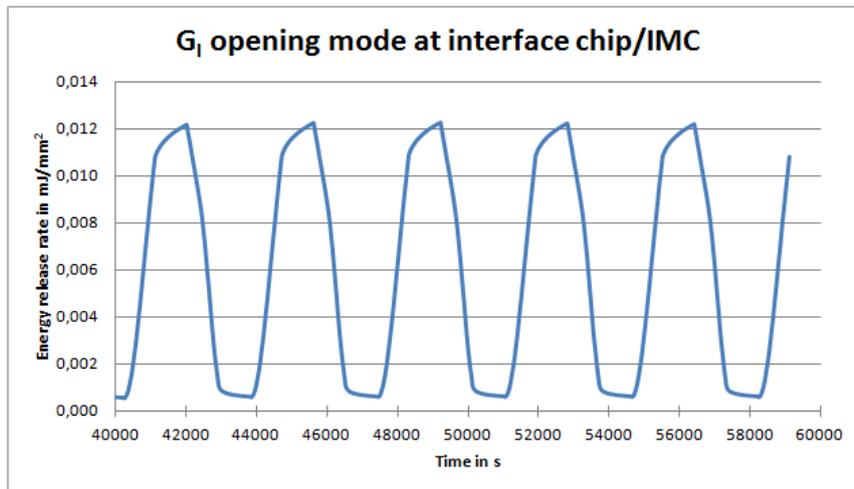


Figure 6.7: Evolution of G_I the opening mode during 6 cycles of PTC at the interface chip/IMC

For the shearing mode, a negative G_{II} represents a displacement to the left and a positive G_{II} represents a displacement to the right for the layer above the crack compared to the layer underneath. Here for the first two cycles a negative G_{II} appears at 150°C , and then there are only positive values of G_{II} . Thus the layer above the crack is almost always moving to the right side compared to the layer underneath. Actually at low temperatures the layer above the crack moves to the right side and comes back more or less to its original position at high temperatures. Here also G_{II} continues to vary at dwell times, thus the crack is always evolving. Regarding the evolution of G_{II} , one can see that the system is stabilized after 3 cycles.

As this kind of crack was never observed, it can be concluded that $G_I=0,012 \text{ mJ/mm}^2$ and $G_{II}=0,04\text{mJ/mm}^2$ are not critical values for crack growth under PTC even if no fracture toughness are known. Then as G_{II} values are 4 times higher than G_I values, it can be deduced that the crack may propagate preferably along a local mode II. But again this is not sure as no values of fracture toughness are known for this case.

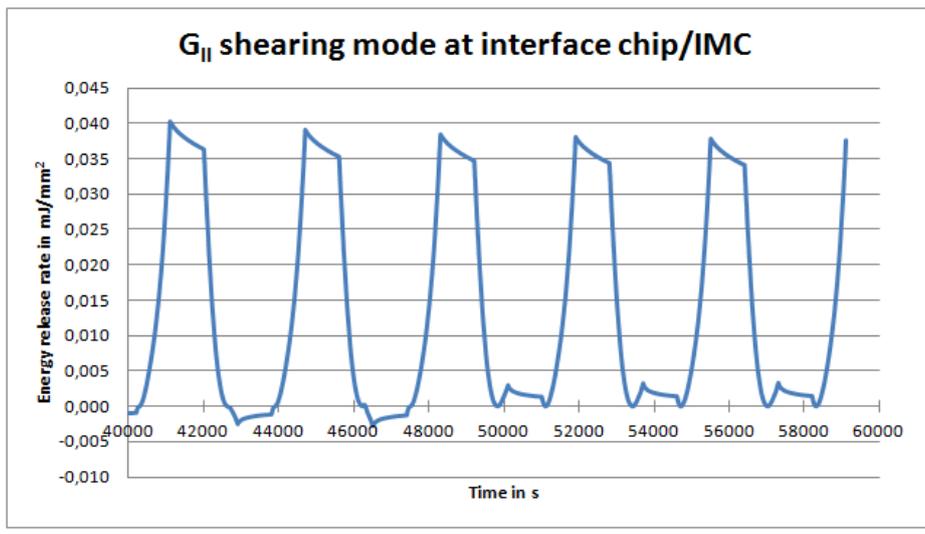


Figure 6.8: Evolution of G_{II} the shearing mode during 6 cycles of PTC at the interface chip/IMC

6.2.2 Crack growth in the Al metallization

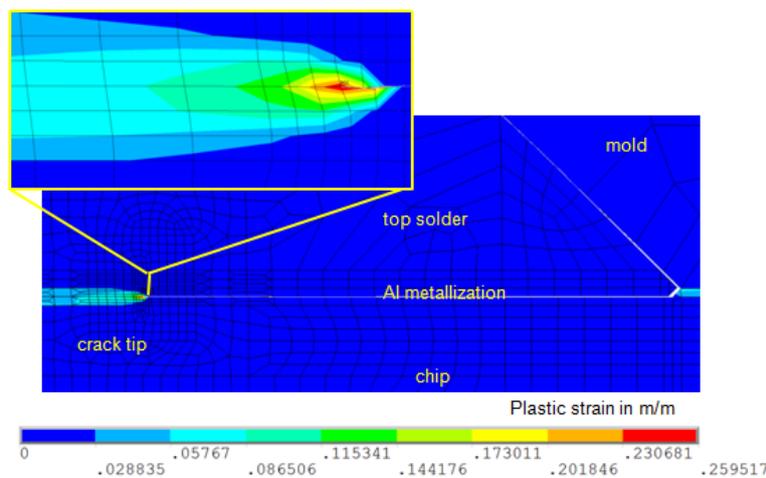


Figure 6.9: Plastic strain at the crack tip in the Al metallization after PTC

At the crack tip in Al metallization, one can see Figure 6.9 that there is a large scale yielding. The evolution of the CTOD for mode I and II is plotted respectively Figure 6.10 and Figure 6.11. For the opening mode, a negative displacement represents a crack closing and a positive displacement represents a crack opening. At low temperatures the crack is open while at high temperatures the crack is closed or tends to close. The system needs about 4 cycles to stabilize. Indeed, for the first 2 cycles the crack remains always open, as its maximum and minimum $CTOD_I$ are both positive. Then for the 3rd cycle the minimum $CTOD_I$ reaches 0. Finally for the last 2 cycles negative values are reached, meaning that for these cycles, the crack is closed at high temperatures. During dwell times at high temperature, $CTOD_I$ is staying constant meaning that layers of the crack are not moving. But for dwell times at low temperature the $CTOD_I$ continues to evolve slightly inducing a slight closing movement of the crack.

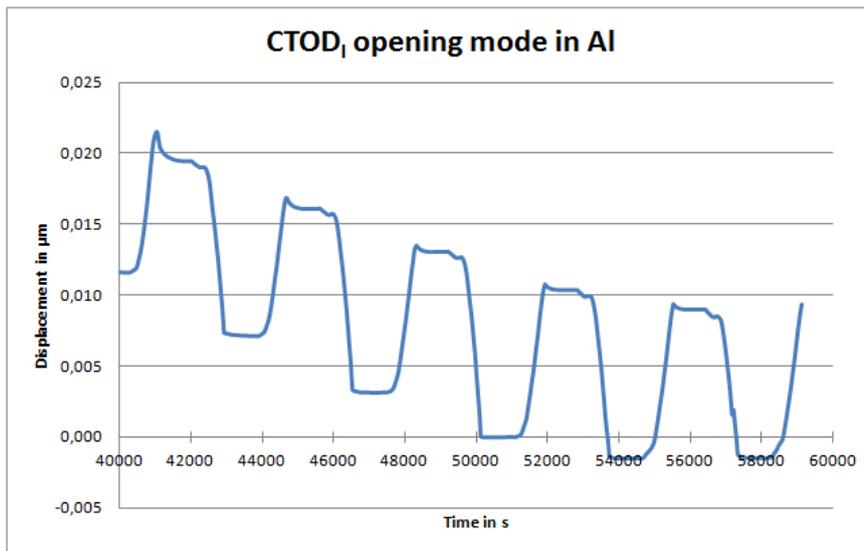


Figure 6.10: Evolution of CTOD_I the opening mode during 6 cycles of PTC in the Al metallization

Concerning the shearing mode of the CTOD, a negative CTOD_{II} represents a displacement to the left and a positive CTOD_{II} represents a displacement to the right for the layer above the crack compared to the layer underneath. In this case, the layer above the crack is always shifted to the left in comparison to the layer underneath. At low temperatures, the layer above the crack is moving further to the left, and at high temperatures, the layer above the crack is coming back to the right. Here also there is a shifting in displacements, as the maximum and minimum of CTOD_{II} are decreasing with increased number of cycles. This shifting in displacement observed for both modes I and II may come from the rate dependent properties of the top solder. In the case of mode II, the system needs about 6 or even more cycles to stabilize. But the amplitude of displacements remains constant, thus calculating 6 cycles was sufficient for our analysis. During dwell times, the shear displacements at the crack tip are staying constant, thus meaning that ramping times are critical for crack growth in mode II, but not dwell times. Thus the same results in terms of crack growth in shear direction can be obtained for short or long dwell times. The amplitude of displacement is 10 times higher in mode II than in mode I. Thus the absolute maximum value of CTOD component at the new crack tip is obtained by the shearing component. According to the definition of the CTOD criterion, this means that the crack growth will occur along a local mode II direction. The values reached in this case for both mode I and II are not critical under PTC, as degradations of the Al metallization layer was not observed with this kind of test.

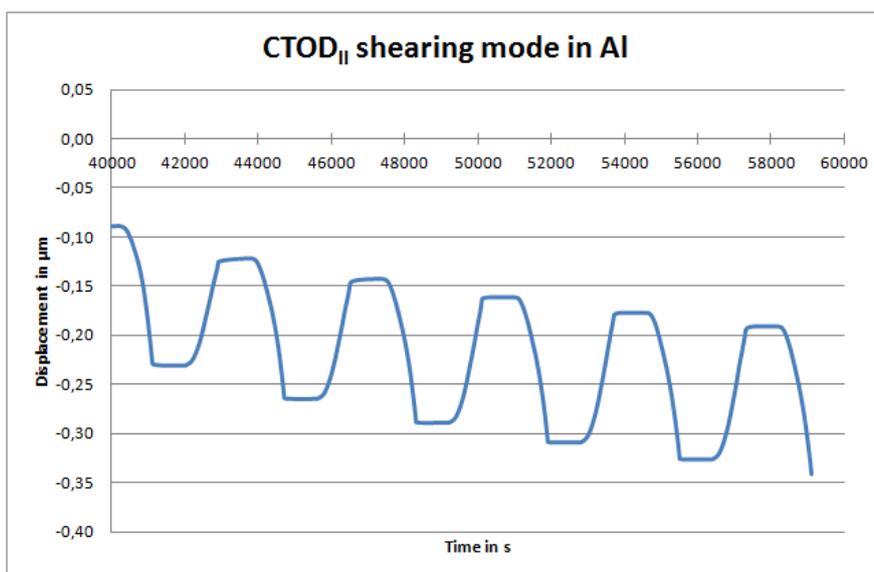


Figure 6.11: Evolution of CTOD_{II} the shearing mode during 6 cycles of PTC in the Al metallization

6.2.3 Crack growth in the top IMC

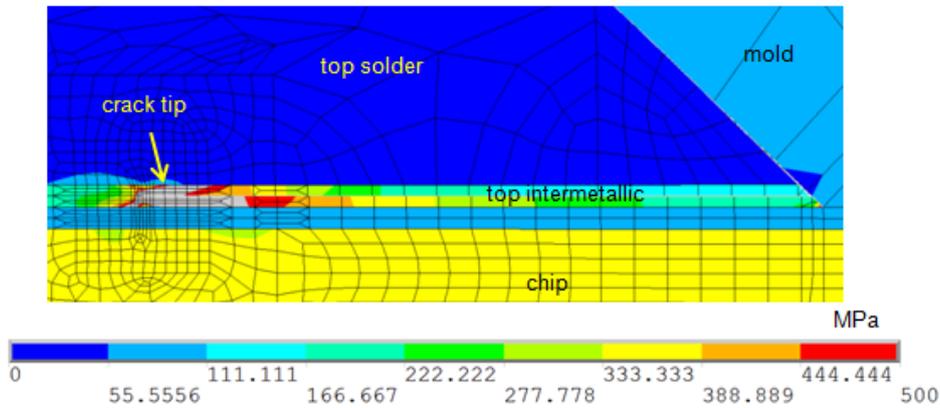


Figure 6.12: von Mises stress at the crack tip at the top IMC after PTC (areas in grey have a von Mises stress superior to 500MPa)

After the 6 PTC cycles, the crack in the top IMC is open (Figure 6.12). The evolution of the ERR for opening and shearing modes is plotted respectively Figure 6.13 and Figure 6.14 for more details. For the mode I, the positive values of G_I are indicating a crack opening. At high temperature the crack is almost close and at low temperature the crack is open at its maximum. For the dwell times at low temperatures, G_I is not constant and continues to increase just like during ramping times. But for dwell times at high temperatures the crack keeps its quasi-closed position and does not further move. So here long dwell times can be critical for crack growth at low temperatures. The system seems to be stable approximately after 4 cycles as the maximum value seems to be constant up to the 4th cycles. The maximal values of G_I reached are really low compared to the absolute maximal values reached for the shearing mode G_{II} . Indeed absolute values of G_{II} are about 100 times higher than values of G_I .

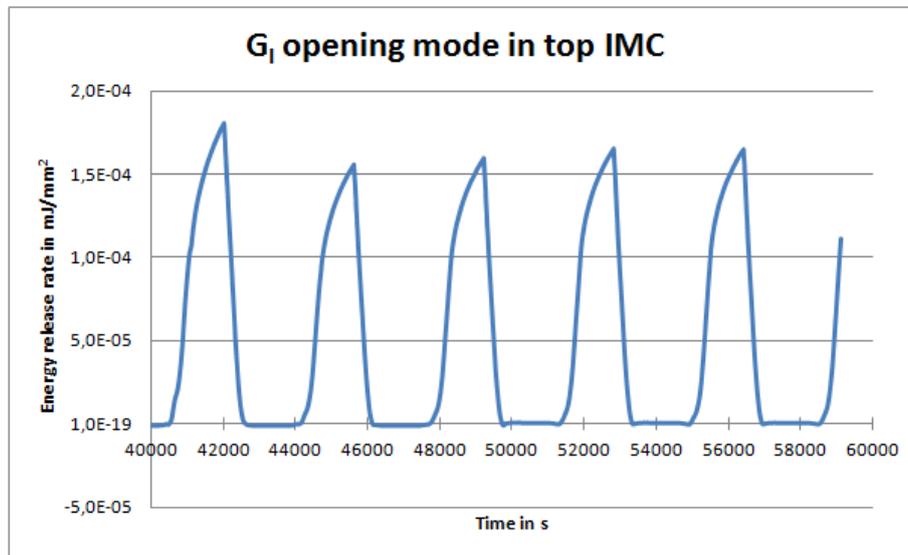


Figure 6.13: Evolution of G_I the opening mode during 6 PTC cycles in the top IMC

For the shearing mode, negative values of G_{II} are representing a displacement to the left for the layer above the crack compared to the layer underneath. At low temperatures the layer above the crack moves to the left side and comes back to its original closed position at high temperatures. Here G_{II} remains constant during dwell times at high temperatures, and slightly decreases for dwell time at low temperatures thus signifying that the layer above the crack tends to come back to its original position. Thus for the shearing mode, long dwell times are not critical at all in terms of crack growth. Regarding the evolution of G_{II} , it can be noticed that the system is already stable after the first cycle.

As no fracture toughness are known for this crack in the IMC, it cannot be determined if the values reached by G are critical for crack growth under PTC. But as absolute values of G_{II} are 100 times higher than values of

G_I , it can be deduced that the crack may propagate preferably along a local mode II. But again this is not sure as no values of fracture toughness are known for this case.

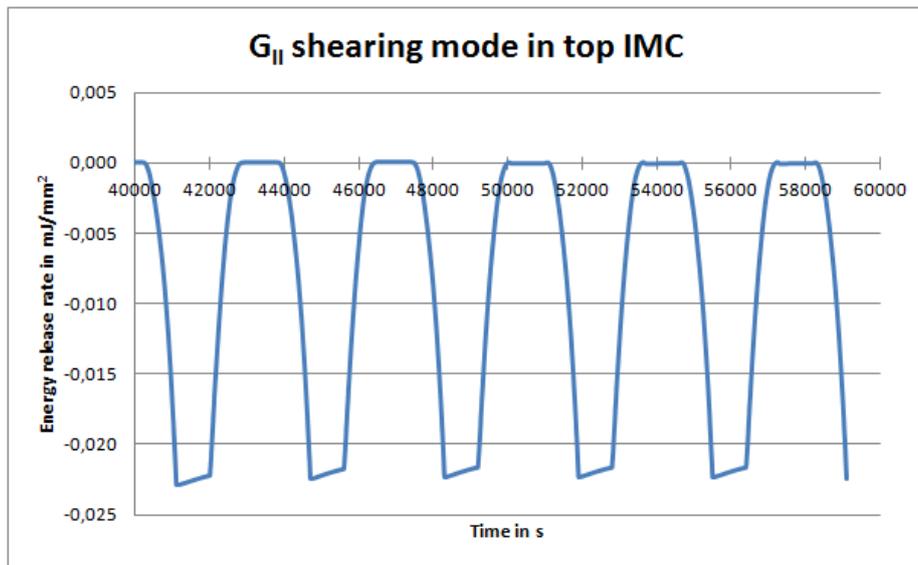


Figure 6.14: Evolution of G_{II} the shearing mode during 6 PTC cycles in the top IMC

6.3 Crack growth under APC

Here also 36 different cases of APC were simulated to complete the sensitivity study on test parameters. The same case as for the thermo-mechanical study is taken as an example to explain the behavior of the 3 different cracks, namely: $T_{jmin} = -40^{\circ}\text{C}$, $\Delta T_j = 120\text{K}$ and $t_{on} = 10\text{s}$.

6.3.1 Crack growth at the interface chip/IMC

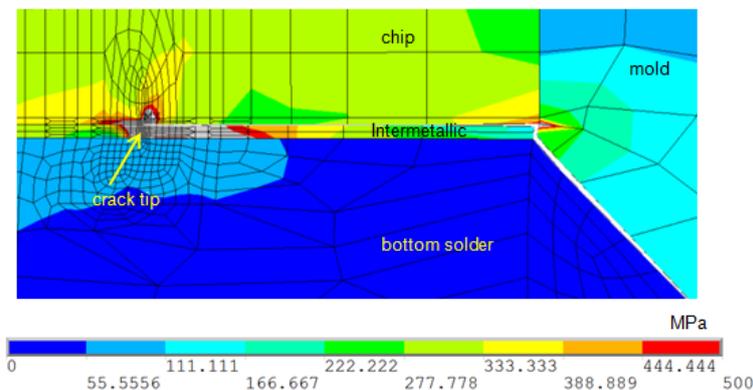


Figure 6.15: von Mises stress at the crack tip at the interface chip/IMC after APC (areas in grey have a von Mises stress superior to 500MPa)

After the simulation of 3 APC cycles, the crack at the interface chip/IMC is open (Figure 6.15). Then, the ERR is calculated for both opening and shearing modes and their evolutions are plotted Figure 6.16 and Figure 6.17. For the opening mode, G_I is always positive, thus the crack remains always open whatever the temperature. Actually at high temperature, the crack tends to close and at low temperature the crack is open at its maximum. At cooling phase, G_I reaches quite rapidly its maximum value and stays constant until the beginning of the heating phase. At heating phase, G_I decreases also rapidly but reaches its minimum value only at the end of the heating time. So in that case long pulse width should not be more critical than short pulse width. The system seems to be stable already after the first cycle as the minimum and maximum values are staying constant cycles after cycles. The maximum value reached by G_I is quite low compared to the one reached by G_{II} . Indeed G_{II} is about 2,5 times higher than G_I .

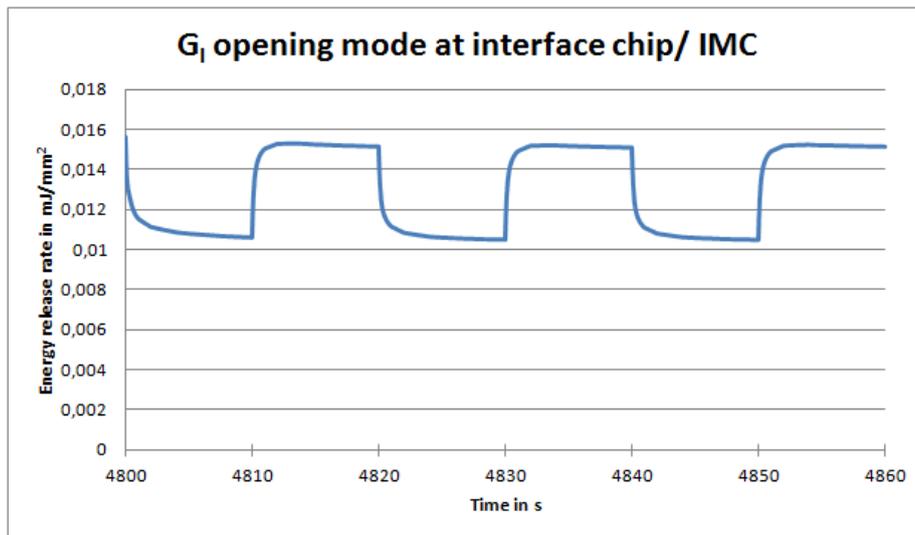


Figure 6.16: Evolution of G_I the opening mode during 3 APC cycles at the interface chip/IMC

For the shearing mode, G_{II} is always positive and thus represents a displacement to the right for the layer above the crack compared to the layer underneath. At low temperatures the layer above the crack moves to the right side and comes back more or less closer to the layer underneath the crack at high temperatures. Here G_{II} varies continuously during heating and cooling phases, thus the crack is always evolving. This means that long pulse width can be more critical than short pulse width in terms of shearing crack growth. Regarding the evolution of G_{II} , minima and maxima are slightly decreasing cycle after cycle. Thus the system may not be stable after 3 cycles, but as the amplitude of G_{II} remains constant, it was sufficient for our analysis to simulate only 3 cycles.

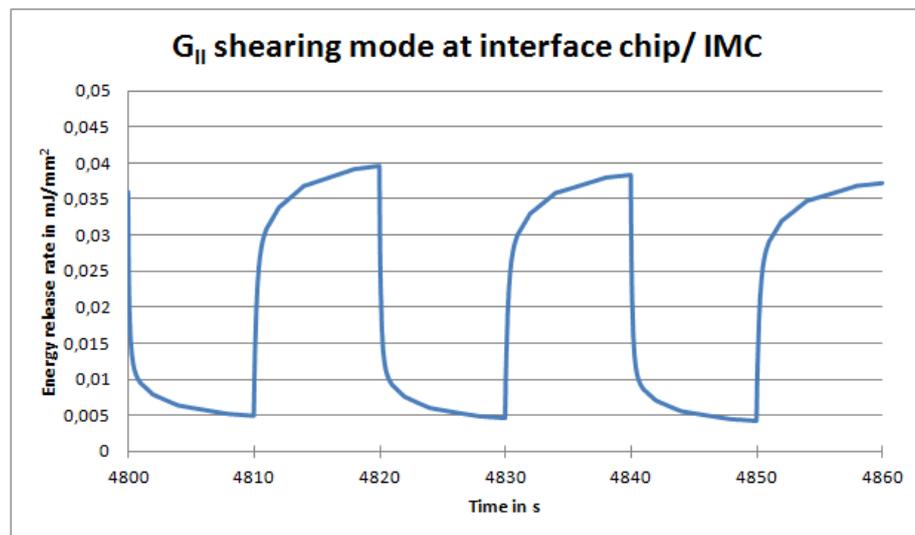


Figure 6.17: Evolution of G_{II} the shearing mode during 3 APC cycles at the interface chip/IMC

As this kind of crack was never observed, it can be concluded that the maximal value of G_I and G_{II} are not critical for crack growth under APC, even if no fracture toughness are known. The maximal values of G_I and G_{II} reached under APC are similar to the ones reached under PTC, and more generally the crack behavior is similar. Then, as the G values reached for the mode II are higher than for the mode I, it can be deduced that the crack may propagate preferably along a local mode II. But again this is not sure as no values of fracture toughness are known for this case.

6.3.2 Crack growth in the Al metallization

Here again, due to the plastic properties of the Al metallization, the crack zone shows a large scale yielding (Figure 6.18). The evolution of the CTOD criterion is plotted for both opening mode (Figure 6.19) and shearing mode (Figure 6.20). For the opening mode, a negative displacement represents a crack closing and a positive displacement represents a crack opening. At high temperatures the crack is closed while at low temperatures the crack is open.

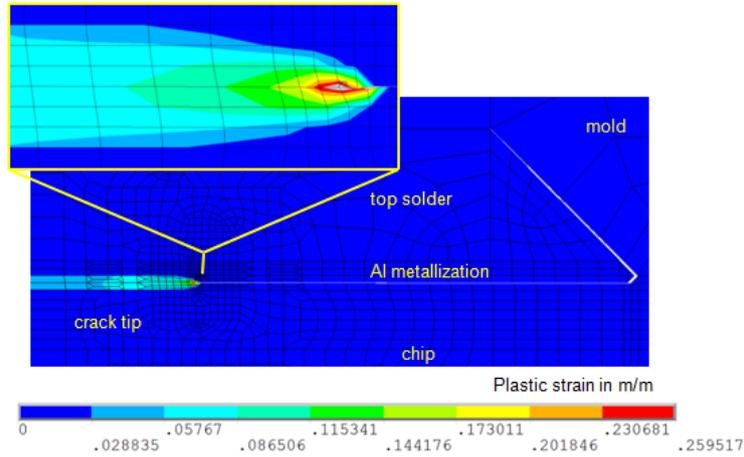


Figure 6.18: Plastic strain at the crack tip in the Al metallization (areas in grey have a plastic strain superior to 0,259517 m/m)

The absolute maximum value of displacement is reached quite at the beginning of heating or cooling phases, and then a slight decrease occurs until the end of the phase. This relaxation behavior may be explained by the rate dependent properties of the top solder located above the Al metallization. The crack opening remains narrow as the maximum displacement observed is under 0,01 μm . This may be explained by the fact that the Cu clip soldered on top of the Al metallization and the mold are restricting out-of-plane displacements and thus crack opening. A slight shift in the maximum and minimum displacement values is noticeable with an increasing number of cycles for both opening and shearing modes. This shift comes from the rate dependent properties of the top solder. The CTOD_I needs a few more cycles to stabilize, but its amplitude stays constant, thus calculating 3 cycles was sufficient for our analysis.

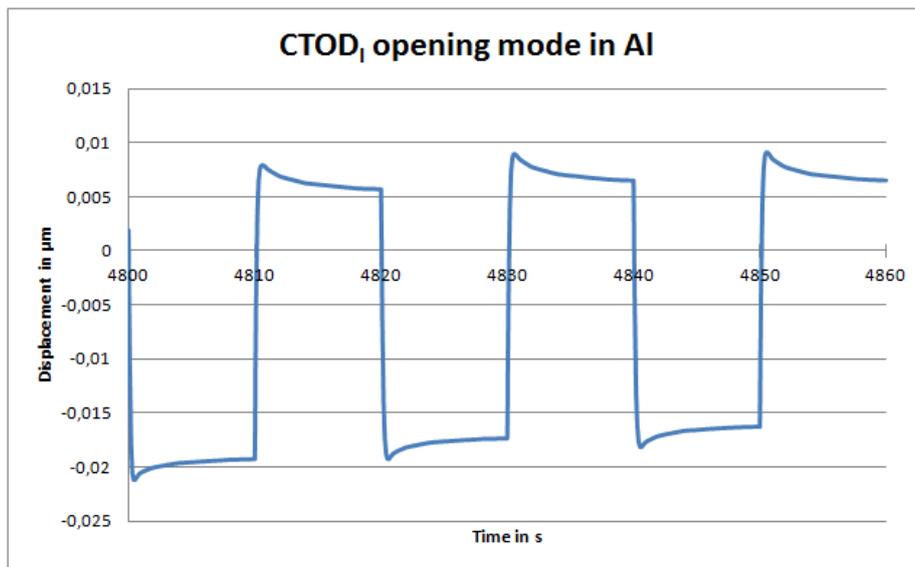


Figure 6.19: Evolution of CTOD_I the opening mode during 3 APC cycles in the Al metallization

For the shearing mode, the negative CTOD_{II} represents a displacement to the left for the layer above the crack compared to the layer underneath. At low temperatures, the layer above the crack is moving further to the left, and at high temperatures, the layer above the crack is coming back to the right. Here also the minimum and

maximum values of displacement are reached quite at the beginning of heating or cooling phases, and then a slight increase or decrease occurs depending on the case, until the end of the phase. Shear displacements are quite important as the maximal $CTOD_{II}$ value reached is about $0,4 \mu\text{m}$. This means that the maximum shearing component $CTOD_{II}$ is 40 times higher than the maximum opening component $CTOD_I$. So the absolute maximum value of $CTOD$ component at the new crack tip is obtained by the shearing component, and thus crack growth will occur along a local mode II direction. But it is not possible to determine if $CTOD$ s have reached critical values as no fracture toughness values are known.

The crack behavior under PTC and APC is very similar, and the same order of values is reached for both $CTOD$ s. There is only slightly bigger amplitude observed for shearing mode under APC than under PTC.

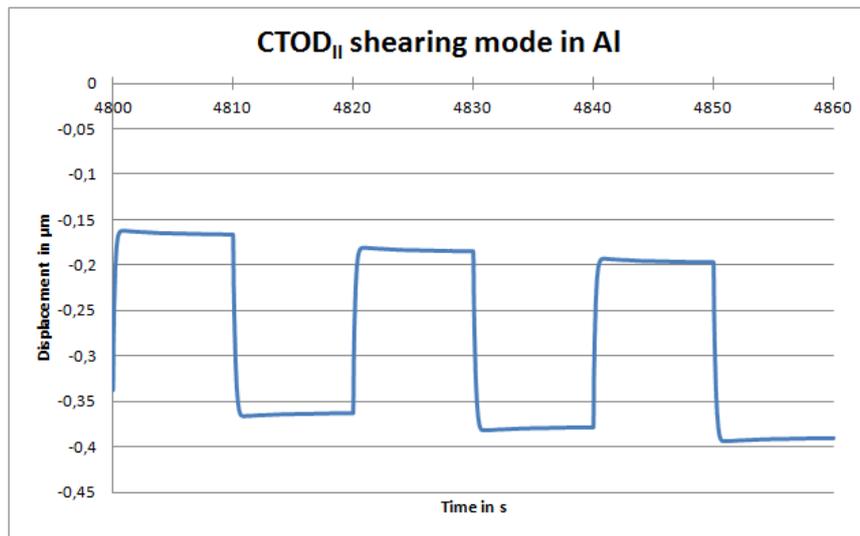


Figure 6.20: Evolution of $CTOD_{II}$ the shearing mode during 3 APC cycles in the Al metallization

6.3.3 Crack growth at the top IMC

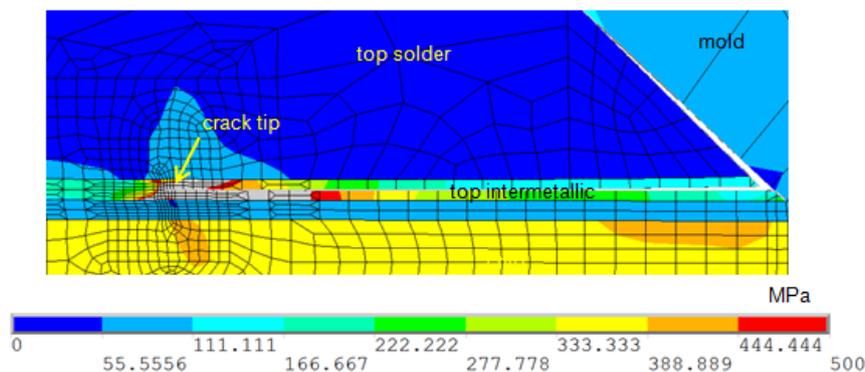


Figure 6.21: von Mises stress at the crack tip in the top IMC (areas in grey have a von Mises stress superior to 500MPa)

After the 3 APC cycles, the crack in the top IMC is open (Figure 6.21). The evolution of the energy release rate for opening and shearing modes is plotted respectively Figure 6.22 and Figure 6.23 for more details. For the mode I, the positive values of G_I are traducing a crack opening. At high temperature the crack is almost closed and at low temperature the crack is open. During heating phases, G_I stays constant thus meaning that the crack remains closed and does not further move. On the other hand, G_I reached its maximum value right at the beginning of the cooling phase and directly after, it severely decreases until the end of the cooling operation. The maximal value of G_I increases cycle after cycle, thus the system may not be stable after 3 cycles. But as the values reached are quite small, there is no significant difference in the amplitude of variations of G_I , thus simulating 3 cycles was sufficient for our analysis. The maximal values reached by G_I are really low compared to the absolute maximal values reached by G_{II} the shearing component. Indeed the absolute value G_{II} is about 100 times higher than G_I .

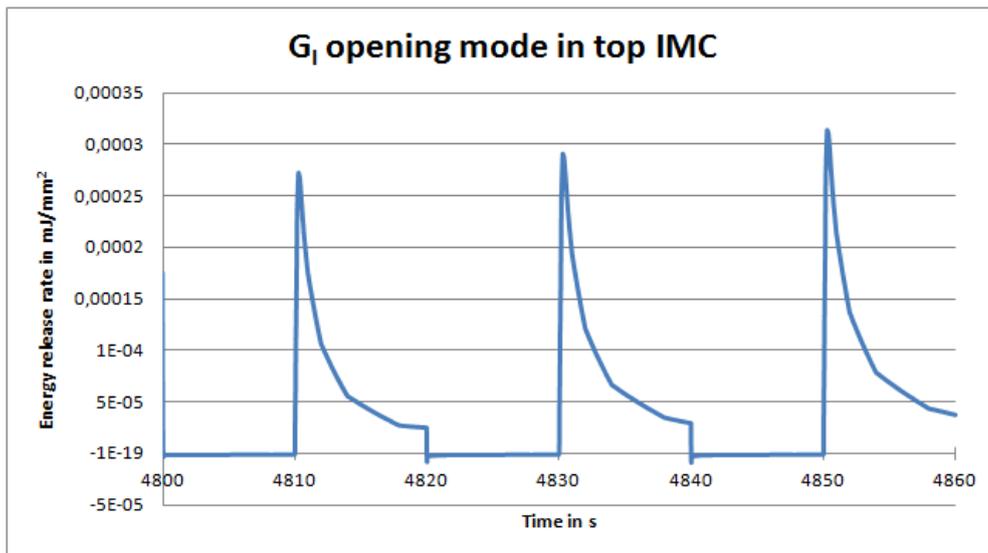


Figure 6.22: Evolution of G_I the opening mode during 3 APC cycles in the top IMC

For the shearing mode, negative values of G_{II} are representing a displacement to the left for the layer above the crack compared to the layer underneath. At low temperatures the layer above the crack moves to the left side and comes back to its original closed position at high temperatures. Right at the beginning of the heating phase the crack joins its original closed position and then some small shearing displacements are occurring. The absolute maximum of G_{II} is also reached right at the beginning of the cooling phase and then a decrease occurs until the end of the phase. Regarding the evolution of G_{II} , it can be seen that the system seems to be already stable after the first cycle.

As no fracture toughness are known for this crack in the IMC, it cannot be determined if the values of G reached are critical for crack growth under APC. But as the absolute values reached by G_{II} are 100 times higher than values reached by G_I , it can be deduced that the crack may propagate preferably along a local mode II. But again this is not sure as no values of fracture toughness are known for this case.

Finally the crack behavior under PTC and APC is very similar and the values reached for both G components are comparable.

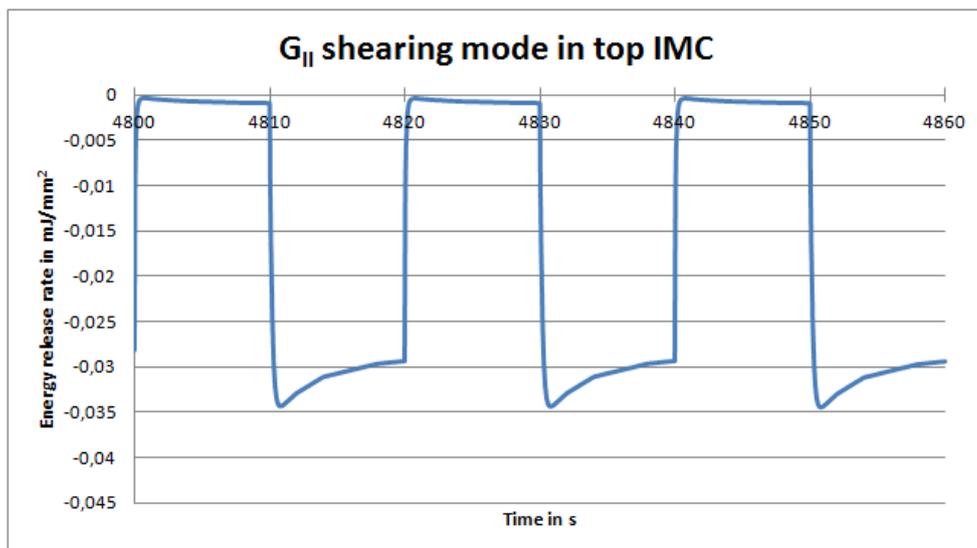


Figure 6.23: Evolution of G_{II} the shearing mode during 3 APC cycles in the top IMC

6.4 Sensitivity study on cracks growth

The analysis of the VCCT and CTOD criteria of the different cracks was always done for the last cycle (3rd cycle) as the system begins to be stabilized.

6.4.1 Crack growth at the interface chip/IMC

For both opening G_I and shearing component G_{II} of ERR (Figure 6.24 and Figure 6.25), three values are to be taken into account: the minimum (blue) and maximum (red) value of each G component reached in one cycle, and the amplitude of ERR variation (green) which is the difference between the maximal and minimal values of each G component. The amplitude is of main interest, and the minimum and maximum allow understanding in which direction the crack is moving. For mode I (Figure 6.24), at high temperatures, displacements are minimal, so the crack tends to close. At low temperatures, displacements are maximal and the crack is open.

All minimal and maximal values of G_I are positive, so the crack is always open. The minimum values of G_I are decreasing with increasing T_{jmin} , ΔT_j and t_{on} . The maximum values of G_I are almost constant for one determined T_{jmin} , but actually a slight decrease can be observed with increasing ΔT_j and t_{on} . So the most influencing parameter on the maximum of G_I is T_{jmin} : an increase in T_{jmin} leads to a decrease in G_I . Consequently the amplitude of G_I is increasing with decreasing T_{jmin} but increasing ΔT_j and t_{on} . Thus in terms of crack opening amplitude at the interface chip/IMC: low T_{jmin} with large ΔT_j and long t_{on} are the most critical parameters.

Under PTC, the minimum value of G_I reached is $0,0006 \text{ mJ/mm}^2$, its maximum is $0,012 \text{ mJ/mm}^2$ thus giving an amplitude of $0,0116 \text{ mJ/mm}^2$. So PTC is even more critical than the worst case of APC in terms of crack opening amplitude at the interface chip/IMC. Indeed the amplitude of G_I reached under PTC is about 2 times higher than the largest amplitude reached with the worst case of the sensitivity study on APC.

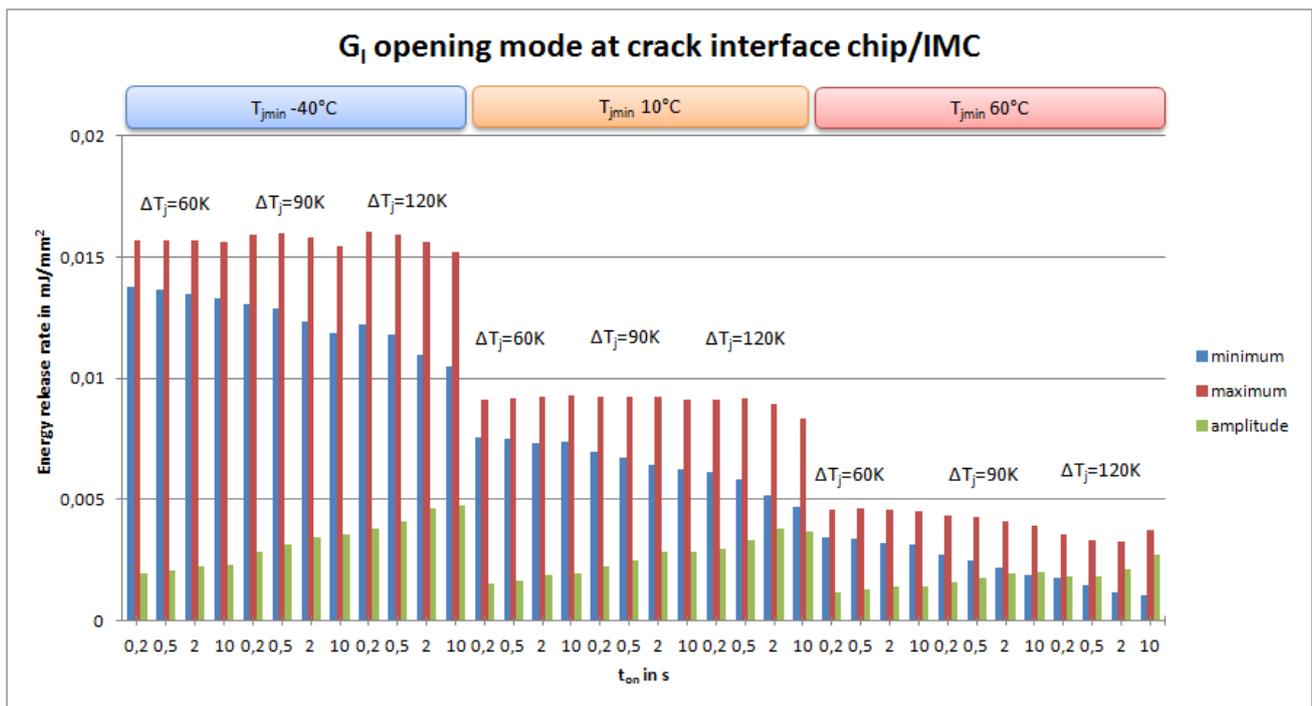


Figure 6.24: Histogram showing G_I the opening component for different sets of test parameters at the interface chip/IMC

For mode II (Figure 6.25), at high temperatures, G_{II} reaches its minimum, meaning that the layer above the crack tends to be aligned with the layer beneath the crack. At low temperatures, G_{II} reaches its maximum, so the layer above the crack is moving to the right side. The minimum value of G_{II} decreases progressively with increasing T_{jmin} , ΔT_j and t_{on} . The maximum values of G_{II} are first influenced by T_{jmin} , as 3 distinct levels of G_{II} are distinguished for the 3 different T_{jmin} . The lower T_{jmin} is, the higher the value of G_{II} . Then G_{II} increases with increasing ΔT_j . The influence of t_{on} on the maximum value of G_{II} is more difficult to determine as for cases with $T_{jmin} = -40^\circ\text{C}$, short t_{on} are increasing the value of G_{II} whereas for cases with $T_{jmin} = 10^\circ\text{C}$ or 60°C short t_{on} are decreasing G_{II} values. But in terms of shearing amplitude for the delamination at the interface chip/IMC

the influence of the different parameters is clear: low T_{jmin} with large ΔT_j and long t_{on} are the most critical parameters.

Under PTC, the minimum G_{II} was really closed to zero ($-2,57e^{-7}$ mJ/mm²) and its maximum reached 0,0378mJ/mm², thus giving an amplitude of about 0,0378 mJ/mm². Thus, the G_{II} amplitude obtained under PTC is higher than the highest amplitude reached under APC with the worst case $T_{jmin} = -40^\circ C$, $\Delta T_j = 120K$ and $t_{on} = 10s$. So PTC is more critical for the crack growth in shearing direction at the interface chip/IMC than APC.

Comparing histograms of G_I and G_{II} components, it is noticeable that the same set of test parameter is critical in terms of amplitudes, namely: low T_{jmin} with large ΔT_j and long t_{on} . The remarkable difference between both modes, is that the shearing mode is dominant (values of G_{II} are approximately 4 time higher than values of G_I) for all loading cases of the sensitivity study. This predominance of shearing component G_{II} compared to G_I , lead us to think that the crack growth may occur preferably along a local mode II, but this cannot be confirmed as no fracture toughness are known for this crack.

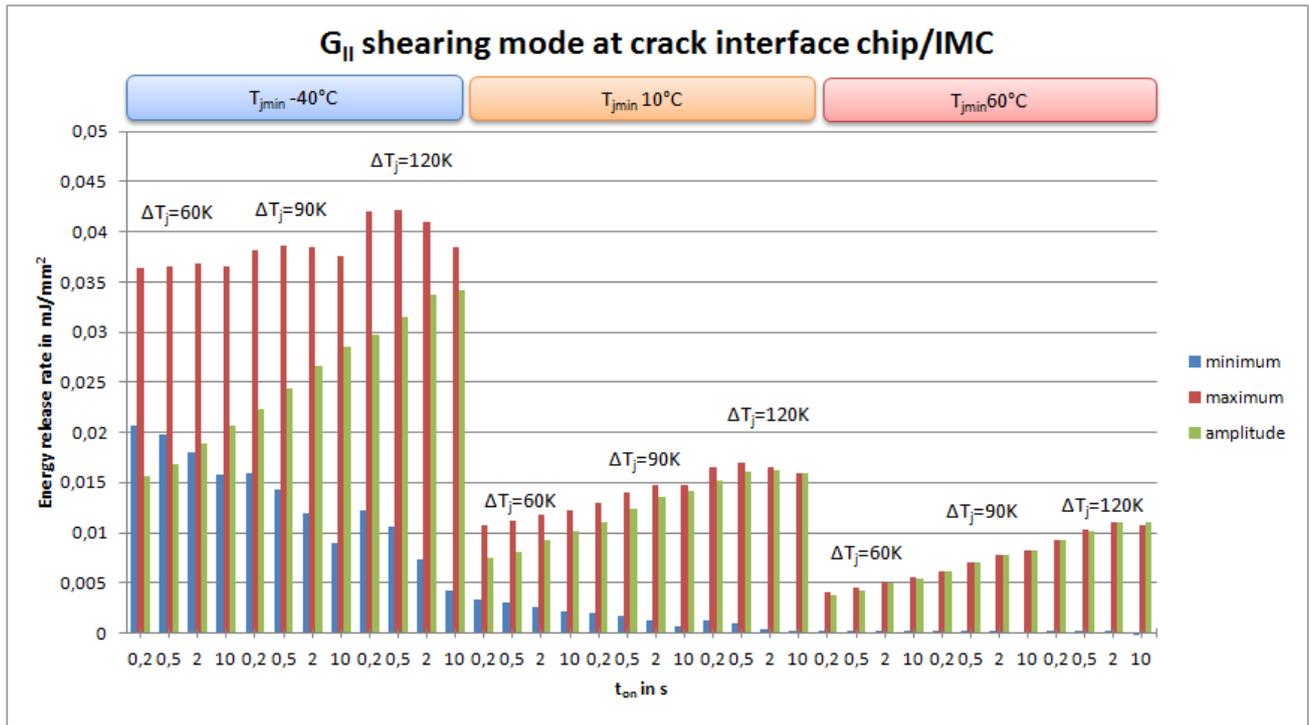


Figure 6.25: Histogram showing G_{II} the shearing component for different sets of test parameters at the interface chip/IMC

Based on experiments it is deduced that the crack growth remains subcritical as no such crack was observed under APC. Thus the maximal values of $G_I = 0,016mJ/mm^2$ and $G_{II} = 0,042mJ/mm^2$ are established as non critical values. Then comparing the results obtained here for the sensitivity study of test parameters on G_I and G_{II} with the results of the sensitivity study on shear stresses in chip (Figure 5.49), one can notice that they are all following approximately the same trend and have the same set of critical parameters. Namely low T_{jmin} with large ΔT_j and long t_{on} are critical for shear stress in chip and crack growth at the interface chip/IMC. Thus analyzing the shear stresses in the chip may be sufficient to have information about the crack growth behavior at the interface chip/IMC, and the fracture mechanics study could have been spared.

6.4.2 Crack growth in the Al metallization

For both opening and shearing component of CTOD (Figure 6.26 and Figure 6.27), three values are to be taken into account: the minimum and maximum value of CTOD component reached in one cycle, and the amplitude of CTOD variation which is the difference between the maximal and minimal values of the CTOD component. Here also the amplitude is of main interest, and the minimum and maximum allow understanding in which direction the crack is moving. For mode I (Figure 6.26), at high temperatures, displacements are minimal, so the crack is closed. At low temperatures, displacements are maximal and the crack is open.

Looking at the histogram, one can notice that all minimal and some maximal values of CTOD for mode I are negative. Those negative values depend on the definition of contact stiffness in simulations and thus do not have a real physical meaning. That is why the interpretation of those results is still in question. Despite that fact, it is possible to identify some main trends regarding the influence of test parameters on the crack opening mode. First, by looking at the amplitude, it appears clearly that increasing the ΔT_j increases the amplitude of displacement. Then, low T_{jmin} are leading to larger amplitude of displacement than high T_{jmin} . The influence of the power-on time t_{on} is difficult to discern. These trends can be explained by observing the influence of test parameters on the decrease of the minimum and the increase of the maximum displacement. Minimal values of $CTOD_I$ decrease with low T_{jmin} , large ΔT_j and short t_{on} . Maximal values are increasing with an increase in ΔT_j and in t_{on} . The highest maxima are reached with low T_{jmin} . For some loading cases, minimum and maximum are negative, meaning that the crack will remain close during APC. To summarize all this information in terms of crack opening amplitude in Al: low T_{jmin} with large ΔT_j are the most critical parameters. The pulse width t_{on} does not seem to have a big influence on the crack opening amplitude. Under PTC, no such negative value was obtained for the minimum $CTOD_I$, the value was closer to zero ($-0,0015\mu m$), thus the $CTOD_I$ amplitude ($0,01\mu m$) is smaller than the one obtained under APC with $\Delta T_j=90K$ or $120K$. But if we consider that these negative values actually mean a crack closing and thus a minimum $CTOD_I$ of zero, results obtained under PTC are really close to the ones obtained under APC with $T_{jmin}=-40^\circ C$, $\Delta T_j=120K$ and $t_{on}=10s$.

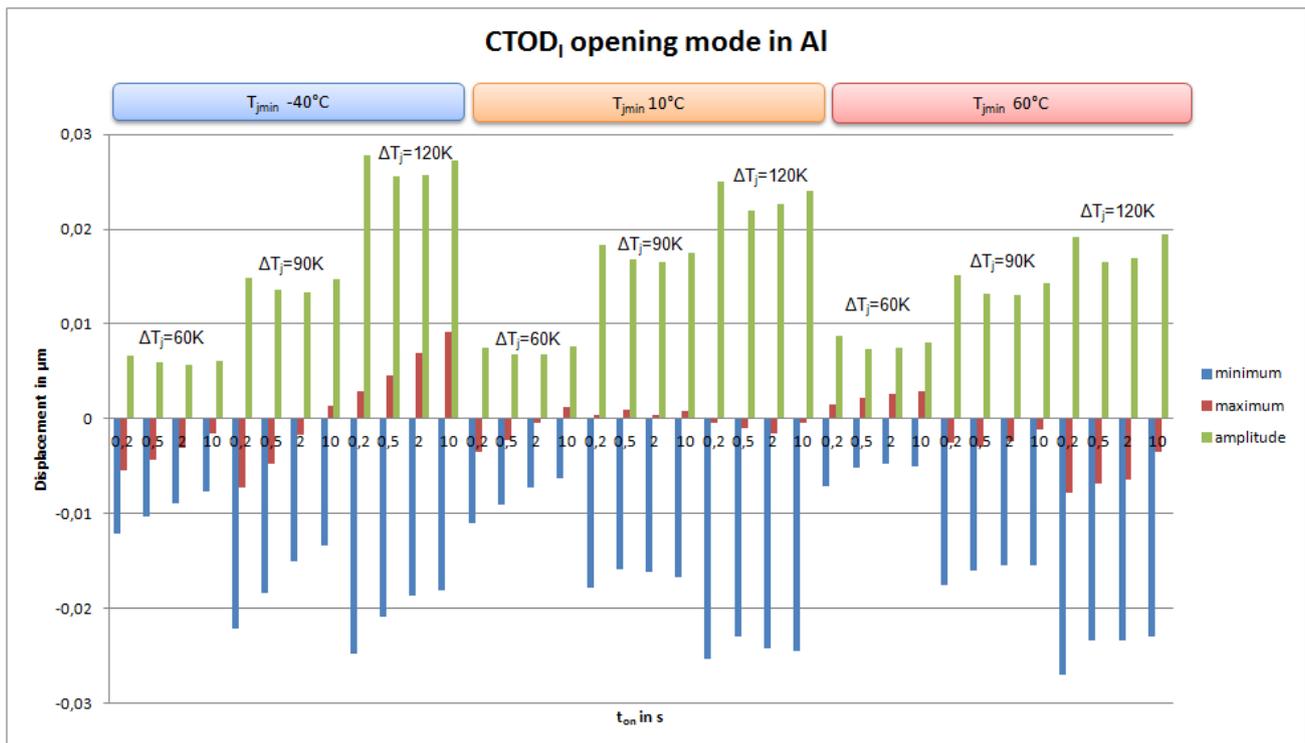


Figure 6.26: Histogram showing $CTOD_I$ the opening component for different sets of test parameters in the Al metallization

Results of shearing mode are also influenced by the closed crack situation, as the closed contact with friction coefficient has effects on stress distribution.

For mode II (Figure 6.27), at high temperatures, the CTOD reaches its absolute minimum, meaning that the layer above the crack is moving to the right side. At low temperatures, the $CTOD_{II}$ reaches its absolute

maximum, so the layer above the crack is moving to the left side. First, one notices that the amplitude of displacement for mode II follows the same trend as for mode I. This means that the amplitude increases with low T_{jmin} and an increase in ΔT_j . Here also the influence of t_{on} is difficult to establish. To better understand these trends, the absolute minimum and maximum variations have to be analyzed. The absolute minimum reaches higher values with low T_{jmin} . It increases with the increase in t_{on} and the decrease in ΔT_j . One can also see that for high T_{jmin} and ΔT_j , the absolute minimum is not negative anymore. This means that for those loading cases, the layer above the crack moves to the right compared to the layer underneath the crack. The absolute maximum is also higher with low T_{jmin} . But it increases with the increase in t_{on} and in ΔT_j . Thus, to summarize: low T_{jmin} with large ΔT_j are the most critical parameters in terms of shearing amplitude for the crack in Al. The influence of t_{on} on the shearing amplitude of crack is difficult to determine. Under PTC, the minimum of $CTOD_{II}$ reaches $-0,34 \mu m$, its maximum $-0,19 \mu m$, thus giving an amplitude of $0,15 \mu m$. These results are very similar to the ones obtained under APC with $T_{jmin} = -40^\circ C$, $\Delta T_j = 120K$ and $t_{on} = 2s$, and are really close to the APC worst case occurring with $T_{jmin} = -40^\circ C$, $\Delta T_j = 120K$ and $t_{on} = 10s$.

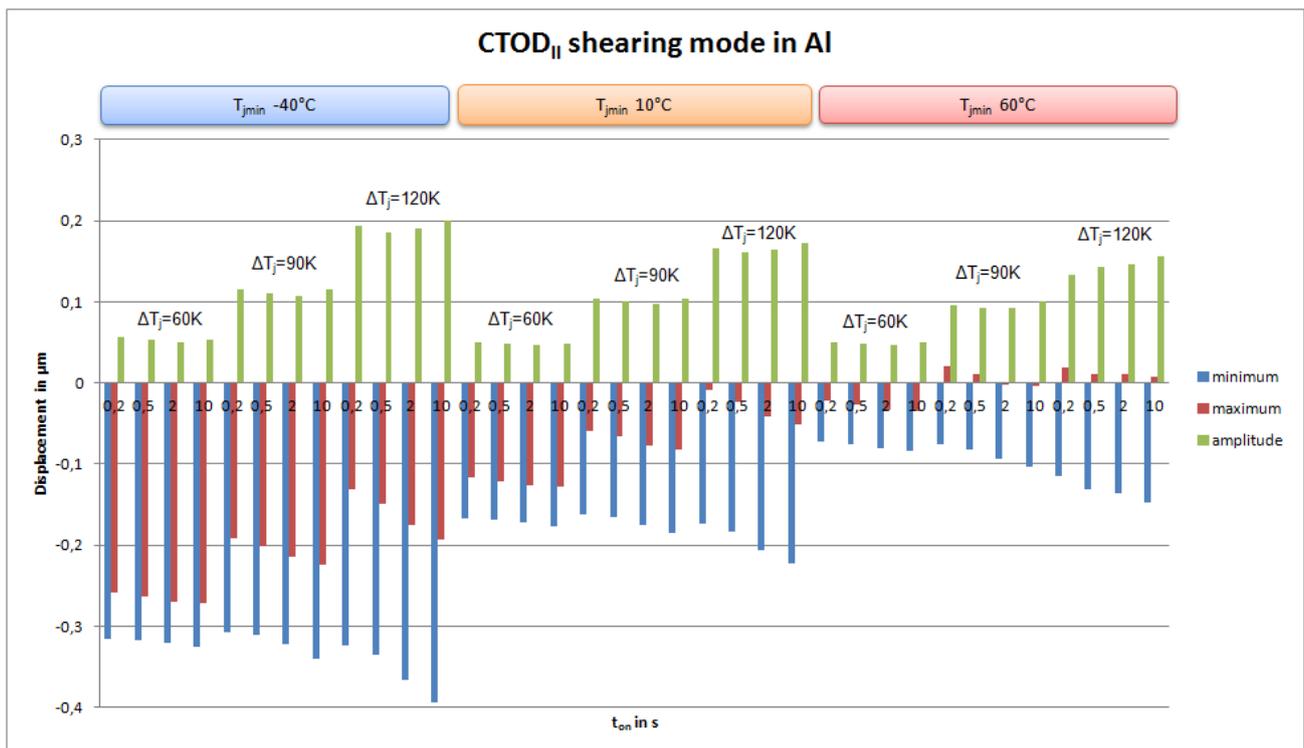


Figure 6.27: Histogram showing $CTOD_{II}$ the shearing component for different sets of test parameters in the Al metallization

Comparing values of CTOD components for mode I and mode II, it is noticeable that shearing displacements are clearly dominant (approximately 10 times higher than opening displacements) for all loading cases of the sensitivity study. This large predominance of $CTOD_{II}$ compared to the $CTOD_I$, added to the difficulties to properly interpret results for $CTOD_I$ component, lead us to conclude that the shearing mode is the most critical one and therefore the only one to be taken into account. And according to the definition of the CTOD criterion the crack growth will occur along a local mode II direction for all cases of the sensitivity study.

Based on experiments it can also be deduced that the crack growth probably remains subcritical as the observed cracks were propagating progressively with the increase of number of power cycles for every set of test parameters. Then comparing results of the sensitivity study of test parameters on plastic strain and on CTOD modes, one can notice that they are all following approximately the same trend and have the same set of critical parameters. Namely large ΔT_j with low T_{jmin} are critical for plastic deformation and crack growth. The only difference is concerning t_{on} . For plastic strain, short pulses are critical, whereas for both CTOD components it is difficult to determine the influence of t_{on} . With this information a first critical value for the CTOD can be developed, by stating that the shearing displacement obtained for the lowest T_{jmin} with a ΔT_j between 60K and 90K defines a limit. When the $CTOD_{II}$ remains under the limit, the crack growth is not critical, but when it exceeds the limit, then a case study should be performed to determine how critical it is. Thus the criterion would be defined by $CTOD_{IIc} = 0,08 \mu m$.

6.4.3 Crack growth in the top IMC

Minima and maxima of G_I and G_{II} of ERR are plotted together with their amplitude, respectively Figure 6.28 and Figure 6.29. The amplitude is of main interest, but minima and maxima give information about the directions along which the crack is moving. For mode I (Figure 6.28), at high temperatures, displacements are minimal, so the crack is closed. At low temperatures, displacements are maximal and the crack is open.

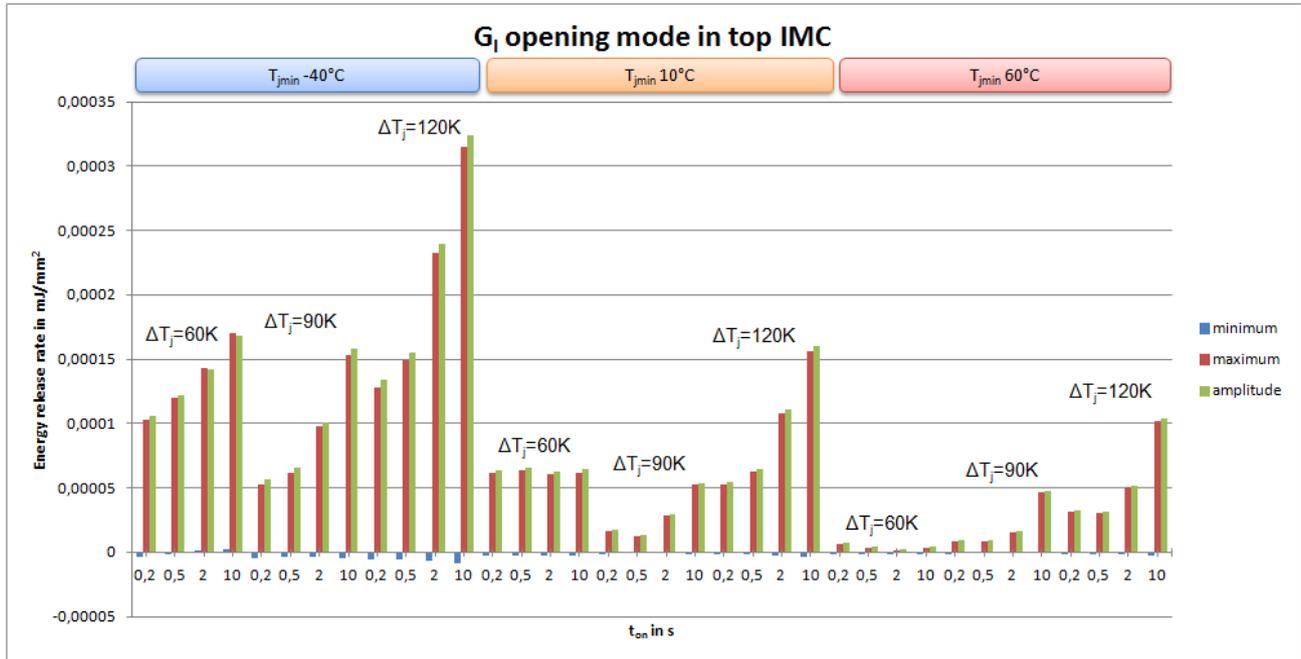


Figure 6.28: Histogram showing G_I the opening component for different sets of test parameters in the top IMC

Minimal values of G_I are sometimes negative, sometimes positive, but they are always really close to zero. Thus the crack always returns to its closed position, whatever the set of test parameters. The maximum values of G_I are increasing with decreasing T_{jmin} and increasing ΔT_j and t_{on} . As the minimum values are close to zero, the amplitude corresponds almost to the maximum of G_I . Thus the most critical set of parameters in terms of G_I amplitude is: a low T_{jmin} with a large ΔT_j and a long t_{on} . The worst case is reached for the case with $T_{jmin} = -40^\circ\text{C}$, $\Delta T_j = 120\text{K}$ and $t_{on} = 10\text{s}$, with an amplitude of $0,00032 \text{ mJ/mm}^2$.

Under PTC, the value of the minimum G_I reached is $-1,5e-8 \text{ mJ/mm}^2$, its maximum is $0,00016 \text{ mJ/mm}^2$ thus giving an amplitude of $0,00016 \text{ mJ/mm}^2$. These results obtained under PTC are similar to the ones obtained under APC with $T_{jmin} = -40^\circ\text{C}$, $\Delta T_j = 60\text{K}$ and $t_{on} = 10\text{s}$.

For the mode II (Figure 6.29), at low temperatures, G_{II} reaches negative values, meaning that the layer above the crack is moving to the left side in comparison to the layer beneath the crack. At high temperatures, G_{II} reaches its maximal values which are close to zero, so crack tends to close or is closed. As the maximal values of G_{II} are close to zero, the amplitude of variations of G_{II} almost corresponds to the inverse of the minimum values of G_{II} . The absolute value of the minimum of G_{II} increases with decreasing T_{jmin} , and increasing ΔT_j and t_{on} . The maximum values of G_{II} are first influenced by T_{jmin} : for $T_{jmin} = -40^\circ\text{C}$ to 10°C , maximum of G_{II} is either negative or equal to zero, and for $T_{jmin} = 10^\circ\text{C}$ to 60°C the maximum of G_{II} is either equal to zero or positive. Then the maximum of G_{II} increases with increasing ΔT_j and decreasing t_{on} . So the worst set of test parameters in terms of amplitude for the mode II is: low T_{jmin} with large ΔT_j and long t_{on} .

Under PTC, the minimum G_{II} reached is $-0,0225 \text{ mJ/mm}^2$ and its maximum was really closed to zero ($9,93e-6 \text{ mJ/mm}^2$), thus giving an amplitude of about $0,0225 \text{ mJ/mm}^2$. These results obtained under PTC are similar to the ones obtained under APC with $T_{jmin} = -40^\circ\text{C}$, $\Delta T_j = 120\text{K}$ and $t_{on} = 0,2\text{s}$.

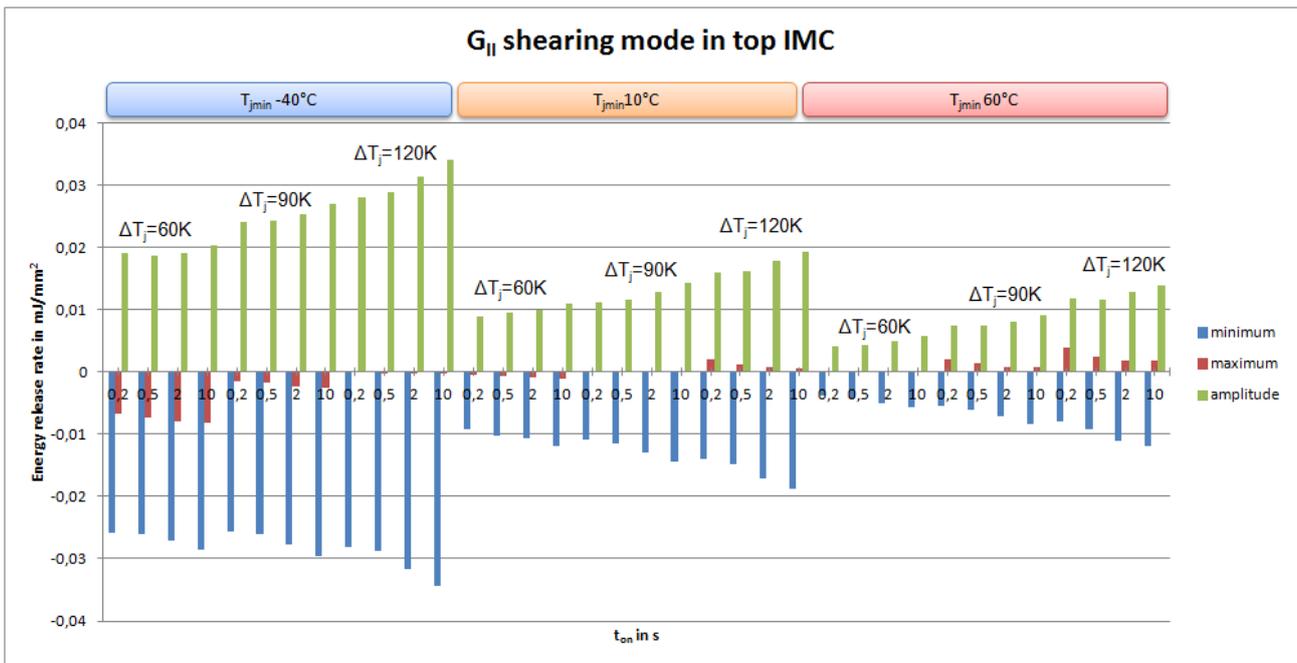


Figure 6.29: Histogram showing G_{II} the shearing component for different sets of test parameters in the top IMC

Comparing histograms of G_I and G_{II} components, it is noticeable that the same set of test parameter is critical in terms of amplitudes, namely: low T_{jmin} with large ΔT_j and long t_{on} . The remarkable difference between both modes, is that the shearing mode is clearly dominant (values of G_{II} are about 100 times higher than values of G_I) for all loading cases of the sensitivity study. This clear predominance of the shearing component G_{II} compared to G_I , leads us to think that the crack growth may occur preferably along a local mode II, but this cannot be confirmed as no fracture toughness are known for this crack.

Based on experiments it can also be deduced that the crack growth probably remains subcritical as the observed cracks were propagating progressively with the increase of number of power cycles for every set of test parameters. Then comparing results of the sensitivity study of test parameters on the von Mises stress (Figure 5.54) and on the components G_I and G_{II} in the top IMC, one can notice that they are all following approximately the same trend and have the same set of critical parameters. Namely large ΔT_j with low T_{jmin} are critical for von Mises stress and crack growth. The only difference is concerning t_{on} . For G_I and G_{II} , long pulses are critical, whereas for von Mises stresses it is difficult to determine the influence of t_{on} . With this information and by taking only the shearing mode G_{II} into account, a first critical value for G_{II} can be developed. Indeed, it can be stated that the shearing displacement obtained for the lowest T_{jmin} with a ΔT_j of 60K defines a limit. When G_{II} remains under the limit, the crack growth is not critical, but when it exceeds the limit, then a case study should be performed to determine how critic it is. Thus the criterion would be defined by $G_{IIc}=0,02 \text{ mJ/mm}^2$.

7 Discussion

7.1 Failure mechanisms under APC

With APC tests it was seen that the module suffers from degradations in both solder layers, sometimes in the IMCs, in the Al metallization and in the mold. No systematical failures are occurring in the chip. These experimental observations are explained thanks to the use of simulations. Indeed, stresses in the chip were not found to be critical whereas important amount of creep strain and plastic strain are accumulated respectively in solder layers and in the Al metallization. Stresses in the top IMC were also studied but it cannot be stated if values reached are critical or not, as no critical limits are known. Finally, the consequences of the presence of cracks in mold on the rest of the module were also investigated. In order to have an overview on tests results and failures that did occur during tests, Table 7.1 summarized 16 of the 30 different tests performed, for reasons of clarity and shows their resulting failures and number of cycles endured. Results are presented layer by layer and finally the number of cycles endured and the lifetime estimation based on the EoL criterion $V_f + 3\%$ are indicated. First the presence of degradations in the bottom solder is summarized by showing modules having a significant increase in Z_{th} (increase in $Z_{th} \geq +10\%$ at 0,01s) with a blue + and modules having cracks with a red x. Then the presence of degradation in the Al metallization is summarized by showing modules having a significant increase in R_{DSon} (increase in $R_{DSon} \geq +20\%$) with a blue + and modules having cracks or deformations with a red x. Degradations in the top solder as well as in the mold are not generating significant modifications neither in electrical nor in thermal parameters monitored, thus only physical degradations are reported in the table. For the top solder, modules having cracks are indicated with a red x, and for the mold the red x was attributed to modules showing delamination at interfaces Cu/mold and/or cracks inside the molding compound. Finally the lifetime prediction was written in red for modules having a lifetime shorter than 500 000 cycles whereas it was written in green for modules having a lifetime superior to 500 000 cycles.

First, looking at the table as a whole, one can see that degradations are often occurring simultaneously in the solder layers, the Al metallization and in the mold.

Now looking at the results concerning the bottom solder, it appears that only 2 modules have a significant increase of Z_{th} but the presence of cracks was reported more often. This shows that even though cracks are often present in the bottom solder, those cracks remain most of the time not critical as they do not degrade significantly the thermal path of the module. Actually it was seen that cracks are formed at the edges of the chip and do not propagate quickly, but are compressed by the mold which hold the module together. Thus the cracks formed in the bottom solder are acceptable and are not the main cause for the device failure.

Then concerning degradations in the Al metallization, one can see that the presence of cracks and/or deformations is reported for all cases except for tests performed with $\Delta T_j = 60K$ for which the End of Life was not reached. Moreover the presence of degradations in the Al metallization is almost always accompanied by a significant increase in R_{DSon} . Thus degradations in the Al metallization are always leading to a degradation of the electrical behavior of the module. So the Al metallization degradation is a systematical failure mechanism with significant electrical consequences.

Degradations in the top solder are not that frequently reported, according to the table. Moreover the top solder degradation does not lead to significant electrical or thermal changes. Indeed, as explained in the chapter 4, the top solder degradation has only a negligible impact on the R_{DSon} increase, and a negligible thermal effect, as the top side thermal path represents only less than 5% of the total cooling path of the module. Besides, it was observed with the failure analysis that cracks in the top solder are forming at the meniscus and do not propagate very quickly as the molding compound applies a pressure on the rest of the module and hold the structure together. So the top solder degradation is definitively not the main failure mechanism in the module. Finally delamination and cracks in the mold appear quite often. These degradations are developing progressively with an increasing number of cycles. Mold degradation itself is not critical as it does not have electrical or thermal consequences, but it can increase the amount of creep strain and plastic strain accumulated respectively in solder layers and in the Al metallization. Thus mold degradation is not the main failure mechanism but can be an issue as it can accelerate other failure mechanisms.

T_{jmin}	-30°C				15°C						65°C			
	60K	120K			60K	90K	120K			60K	80K	95K	110K	
ΔT_j	0,2s	0,5s	2s	5s	0,2s	0,5s	0,2s	0,5s	2s	10s	0,2s	0,5s	6s	0,35s
t_{on}	0,8s	2,5s	7s	10s	3s	4,5s	3,8s	3,5s	3s	5s	1,2s	1s	6s	1,15s
t_{off}														
$Z_{th} +10\%$ at 0,01s			+	+										
Degradation bottom solder		x	x	x			x	x		x		x	x	x
$R_{dson} +20\%$		+	+	+			+	+	+			+		+
Degradation Al		x	x	x		x	x	x	x	x		x	x	x
Degradation top solder		x	x	x						x		x		x
Degradation mold		x		x		x		x	x	x				x
Number of cycles	3.000.000	510.000	110.000	220.000	1.000.000	830.000	428.000	1.430.000	702.000	262.983	2.270.000	1.380.000	519.513	629.543
EoL criterion Vf +3%	not reached	510.000	not reached	not known	not reached	989.000	292.144	981.515	131.000	93.000	not reached	not reached	not reached	387.000

Table 7.1: Recap chart of 16 of the 30 APC tests performed with the resulting degradations in the module (16 of 30 tests are shown for clarity reason. A blue + represents an increase in electrical and thermal parameters, whereas a red x represents the presence of cracks in a material layer)

It can be concluded from experimental results that the degradation of the Al metallization is the main failure mechanism occurring in the module under APC and leading to the device failure. The solder degradation appears as a second failure mechanism which is coupled to Al degradation. Thus it is the opposite of what happen under PTC. Indeed under PTC the bottom solder degradation is the main failure mechanism and the degradation of the Al metallization appears as a second failure mechanism.

The fact that the degradation of the Al metallization is the main failure mechanism under APC has conducted the EoL criterion to be based on the R_{Dson} increase.

7.2 Influence of test parameters

A sensitivity study was performed by the way of APC tests and simulations to determine the influence of the different test parameters on the module behavior. For the experiments, the Table 7.1 gives an idea of the influence of the different test parameters on the lifetime of the module. It can be seen that the major parameter of influence is ΔT_j : the higher ΔT_j , the lower the lifetime. Actually it appears also clearly in the table that with $\Delta T_j = 60K$, which corresponds to field load, no degradations are seen in any layers even after several millions of cycles. This rise the question to know if the same failure mechanisms are taking place under $\Delta T_j=60K$ and under $\Delta T_j=90K$ or $120K$. Simulations give us more insight on the topic. Indeed, in the numerical sensitivity study for the different solder layers (

Figure 5.50, Figure 5.51 and Figure 5.52), it was seen that creep strain was always accumulated whatever the test parameters. Obviously the amounts of creep strain accumulated under $\Delta T_j = 60K$ was really lower than the ones accumulated under $\Delta T_j=120K$, but they were always superior to zero. So the mechanism of solders degradation seemed to be the same whatever ΔT_j . Then, concerning the Al metallization (Figure 5.53), the numerical sensitivity study revealed that for $\Delta T_j=60K$, there is no acc plastic strain at all with $T_{jmin} = -40^\circ C$ and really small amount of acc plastic strain of about $1e^{-6}$ with $T_{jmin} = 10^\circ C$ and $60^\circ C$. Thus, for the Al metallization it is not exactly the same failure mechanism occurring under $\Delta T_j=60K$ and $\Delta T_j=90K$ or $120K$, as there is no plastic deformations for $\Delta T_j=60K$.

The influence of the other test parameters, T_{jmin} and t_{on} on the module behavior is difficult to discern with experiments. But here again simulations allow us to gain more insight on the subject. Indeed, for each result of the numerical sensitivity study, trends concerning the influence of test parameters were determined. The Table 7.2 presents the worst set of test parameters (T_{jmin} , ΔT_j and t_{on}) for each output parameter analyzed (deformation, stress, strain) for each important layer (chip, solder layers, Al metallization, IMC).

It appears first that all deformations, stresses and strains of all layers are increasing with an increase in ΔT_j . Thus a large ΔT_j is indisputably an accelerating factor of failure mechanisms. Then we can look at the different trends layer per layer. First for the chip, one can see that the warpage, the in-plane stress, the out-of-plane stress, the shear stress, and both G for the crack at the interface chip/IMC have different sets of worst parameters. However it can be noticed that the shear stress and both G are all increasing with low T_{jmin} , large ΔT_j and long t_{on} . Thus, the same information comes out of the study of these three output parameters. Then, all solder layers accumulate more creep strain with high T_{jmin} , large ΔT_j and long t_{on} . This was expected, as the

creep effect occurs at high temperature thus necessitating high T_{jmin} and large ΔT_j and needs time to accumulate. Nevertheless, it should be reminded that the Young's modulus of the mold drops down when its temperature is close to its glass transition temperature ($T_g=150^\circ C$), which probably lead to a reduction of the creep effect in the top solder layer. In the Al metallization, plastic deformation and CTOD for both modes are all maximal with a low T_{jmin} and a large ΔT_j . There is only a small difference regarding the influence of t_{on} : the acc plastic strain increases with a short t_{on} , whereas t_{on} does not seem to have a significant influence on none of both CTODs. Finally concerning the IMC, the von Mises stress and both G are increasing with low T_{jmin} , large ΔT_j and long t_{on} . Thus, the same information comes out of the study of these three output parameters, this meaning that the study of crack growth in the IMC may have been spared.

		Inputs		
 of output parameters		T_{jmin}	ΔT_j	t_{on}
Outputs	Warpage Chip			
	In plane stress Chip			
	Out of plane stress Chip			
	Shear stress Chip			
	G_1 Chip/IMC			
	G_2 Chip/IMC			
	Acc creep Bottom solder			
	Acc creep Top solder chip			
	Acc creep Top solder clip			
	Acc plastic Al			
	CTOD ₁ Al			
	CTOD ₂ Al			
	Von Mises stress Top IMC			
	G_1 Top IMC			
	G_2 Top IMC			

Table 7.2: Recap chart of the worst sets of parameters for each output analyzed at each important layer of the module

By comparing the worst set of test parameters for the Al metallization and the solder layers, one can notice that they are not converging. Indeed, the plastic strain in Al accumulates by low T_{jmin} and short t_{on} , whereas the creep strain in solders requires high T_{jmin} and long t_{on} to accumulate. Thus it is not possible to have simultaneously the worst case regarding plastic deformations in the Al metallization and the worst case regarding the accumulation of creep strain in solder layers. There is either high amount of plastic deformations in the Al metallization and moderate amount of creep strain accumulated in solder layers, or high amount of creep strain accumulated in solder layers and moderate plastic deformations in the Al metallization.

7.3 Lifetime models

With the experimental APC tests, a lifetime prediction in function of different sets of test parameters was obtained. With the FEM simulations, amounts of deformations, stresses or strains, also called output parameters, were calculated for different sets of test parameters. Combining the results obtained from both experiments and simulations, allow plotting a lifetime prediction correlating the experimentally obtained lifetime with the corresponding calculated deformations, stresses, or strains... Such a lifetime prediction diagram was deduced for each output parameter studied in each layer. Then a power trend line fitting the best the scattered points was determined. The trend line equation defines then the lifetime model in the form of a Coffin Manson model:

$$N_f = a \cdot (x)^{-b} \quad \text{Eq. 7.1}$$

Where N_f is the number of cycles to failure, a a coefficient and b an exponent determined with experiments and x the output parameter.

Then regarding the lifetime requirements under APC, these ones are strongly dependent on the application of the module. However it can be roughly consider that with $\Delta T_j = 80-90K$, a lifetime of 100 000 cycles is a minimum required while a lifetime of 1 million of cycles characterized already a robust module.

7.3.1 Chip behavior

In the chip no systematical failures are occurring, this meaning that the End of Life (EoL) was never reached in any tests and for any of the failure mechanisms occurring in the chip. Despite that fact, lifetime prediction diagrams with fitting functions were still established for all output parameters studied, by taking the total number of cycles performed for each test as the number of cycles to failure. So, all lifetime models defined for the chip are not representing an exact lifetime prediction, but a minimum of number of cycles that the chip is able to endure. Actually, the chip can survive even more cycles than what is shown. These lifetimes prediction diagrams should not be understood as lifetime models but are showing the Safe Operating Area (SOA) of the Cu clip module.

First the chip lifetime prediction is plotted Figure 7.1 in function of its warpage amplitude. As previously explained, under $\Delta T_j = 80-90K$, a lifetime of 100 000 cycles is a minimum required while a lifetime of 1 million of cycles characterized already a robust module. For our experimental sensitivity study most of the tests were done with $\Delta T_j = 120K$, which is already a large temperature swing. On the graphic, one can see that for the worst case, the inverse of curvature radius amplitude reaches $1,1 \text{ m}^{-1}$ with $\Delta T_j = 170K$ and is able to survive more than 62 000 cycles. This result is acceptable as it represents a minimum of cycles and the loading conditions were really severe with $\Delta T_j = 170K$. The best case shows also quite good result, as with the lower warpage amplitude, more than 3 million of cycles can be reached under $\Delta T_j = 60K$. The best fitting power trend line is plotted on the graphic with its equation and its R^2 value. The R^2 value reveals how closely the estimated values for the trend line correspond to the actual data. The trend line is reliable when its R^2 value is at or near 1. Here it appears that the curve fitting is not optimal as the R^2 value is quite far from 1. This can be explained by the fact that what is taken as the number of cycles to failure is actually not exactly the number of cycles to failure but only the number of cycles until the End of Test (EoT). This generates imprecision in the lifetime prediction fitting function.

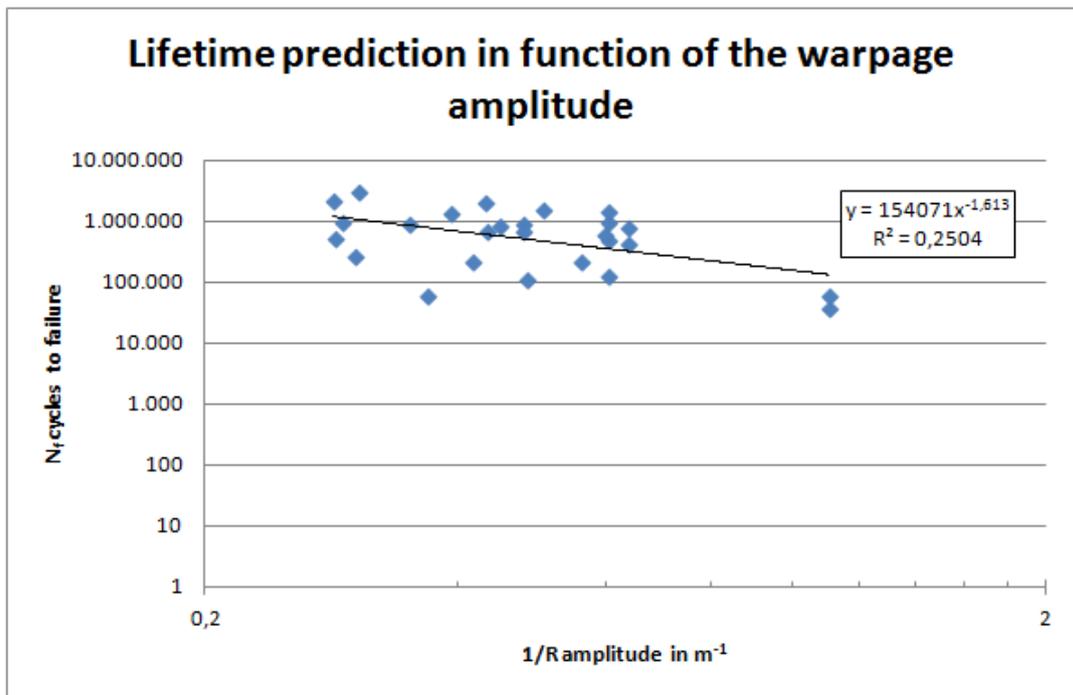


Figure 7.1: N_f EoT cycles in function of the inverse of curvature radius amplitude

Then the prediction of the chip lifetime is plotted in function of the in-plane stress amplitude Figure 7.2. Here the trend line fits quite well the data as $R^2=0,6$, thus the lifetime prediction function is quite reliable. In the best case, more than 3 million of cycles can be reached with an in-plane stress amplitude of 110MPa. In the worst case a stress amplitude of 410MPa leads to a lifetime superior to 62 000 cycles. As it is known from Bosch experience that no premature failure occurs in a chip submitted to 900 MPa of in-plane stress amplitude, the real lifetime should be significantly higher than what is predicted here.

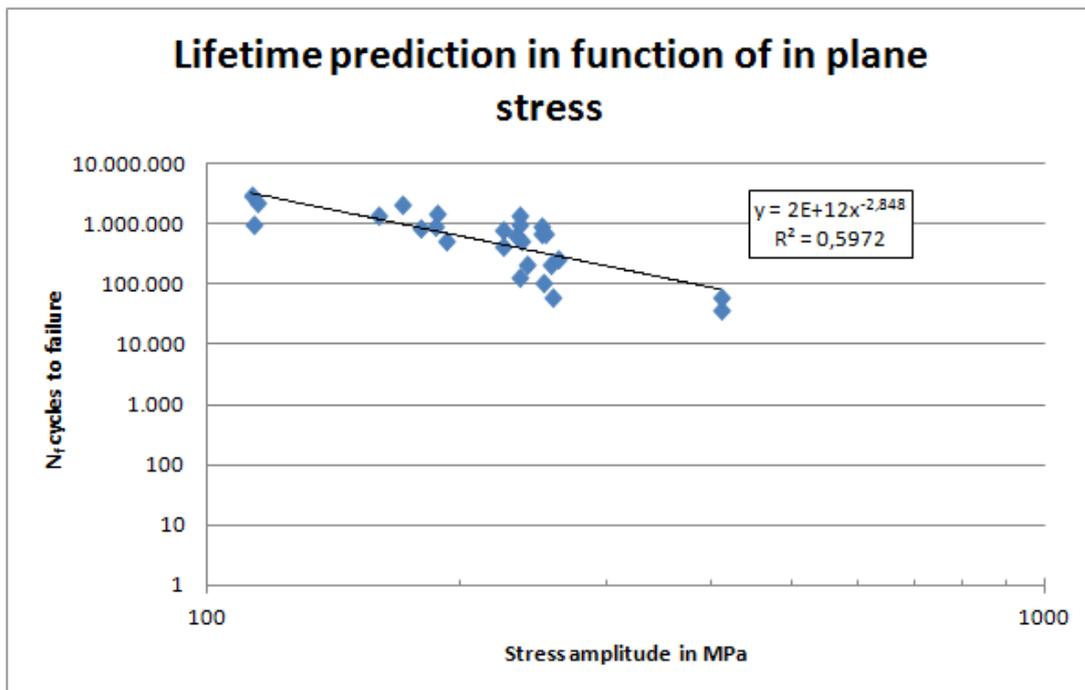


Figure 7.2: N_f EoT cycles in function of the in-plane stress amplitude in the chip

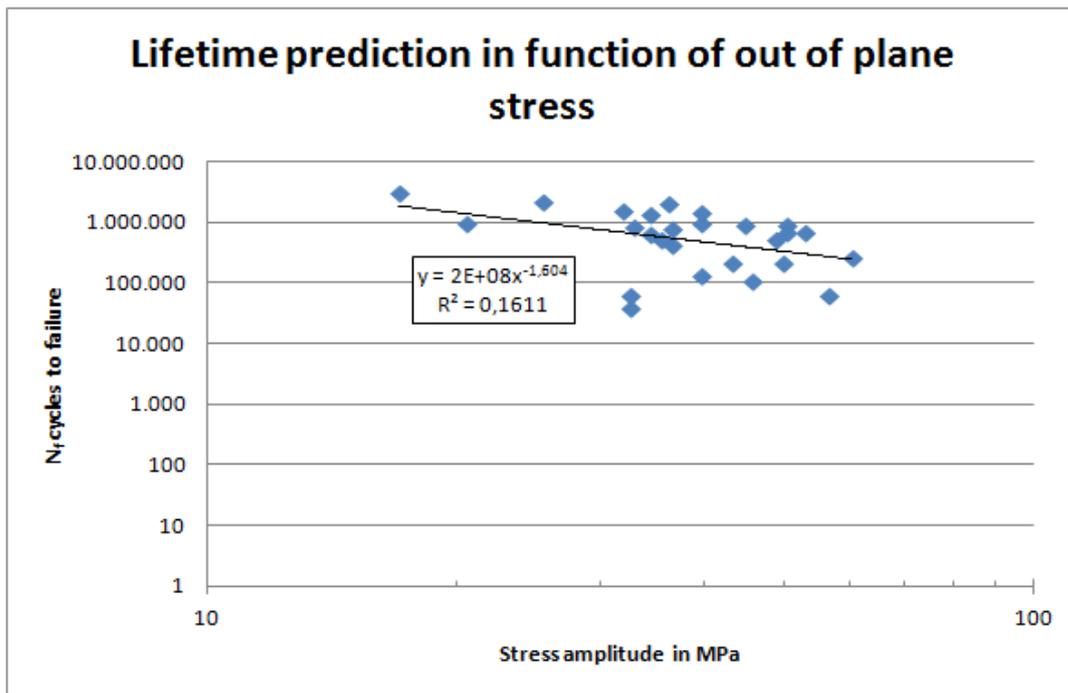


Figure 7.3: N_f EoT cycles in function of the out-of-plane stress amplitude in the chip

The lifetime of the chip is also predicted in function of the out-of-plane stress amplitude Figure 7.3. The data are quite scattered especially for the highest values of stress amplitude, thus the trend line is not very reliable. Nevertheless, results appear to be quite good, as already more than 260 000 cycles are reached under $\Delta T_j=120K$ for the highest stress amplitude of 60 MPa. As it is known from Bosch experience that no premature failure occurs in a chip submitted to 200 MPa of out-of-plane stress amplitude, the real lifetime should be significantly higher than what is predicted here.

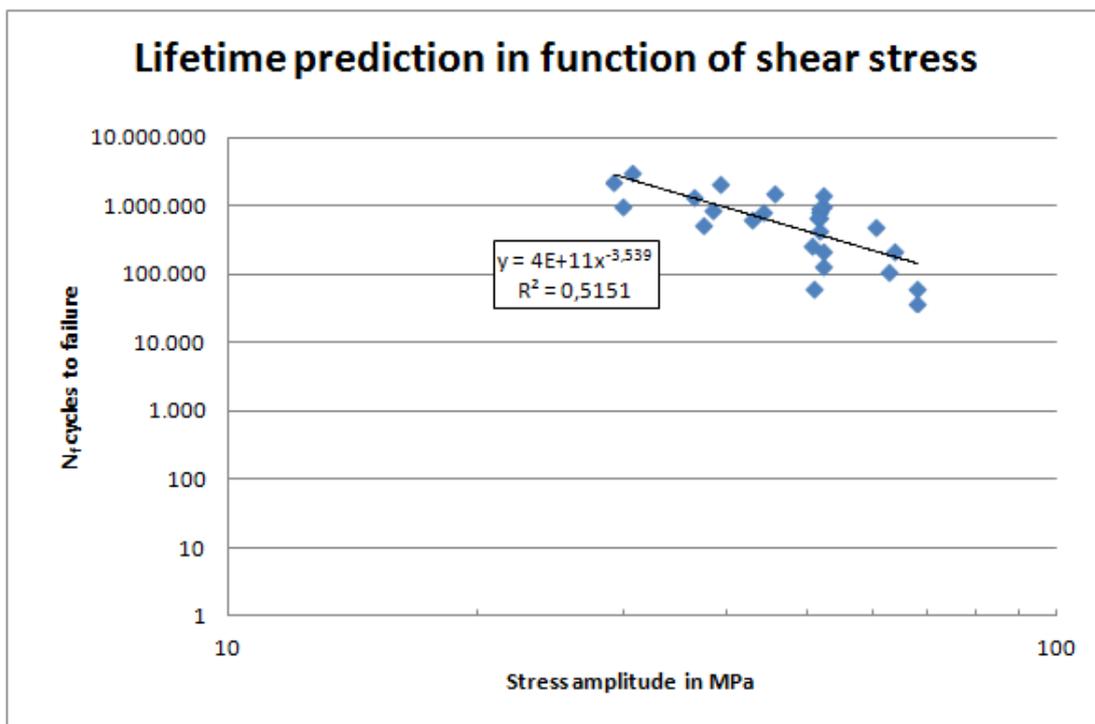


Figure 7.4: N_f EoT cycles in function of the shear stress amplitude in the chip

Finally the Figure 7.4 presents the lifetime prediction of the chip in function of the shear stress amplitude. The trend line is moderately reliable. In the best case, with a stress amplitude of 30MPa the chip can pass minimum 2,3 million of cycles. In the worst case, a stress amplitude of 70MPa leads to a minimum lifetime

of 62 000 cycles. This result is acceptable as it represents a minimum of cycles and the loading conditions were really severe with $\Delta T_j=170K$.

Concerning the crack growth at the interface chip/IMC, the lifetime is predicted in function of both G_I and G_{II} amplitudes

Figure 7.5). For both G_I and G_{II} , their trend lines are only moderately reliable. Then it appears clearly on the graphic that the values reached for G_I amplitude are lower than the ones reached for G_{II} . For the mode I, in the best case, a G_I amplitude of $0,0011mJ/mm^2$ leads to a lifetime superior to 2,3 million of cycles. In the worst case, a G_I amplitude of $0,005mJ/mm^2$ induces a minimum lifetime of 220 000 cycles. These results are describing a very reliable module, as the worst case located on the trend line and happening with a G_I amplitude of $0,005mJ/mm^2$ reached under $\Delta T_j=120K$ has a minimum lifetime already well above 100 000 cycles.

Regarding results for the mode II, values of G_{II} amplitudes are more spread out than the ones obtained for G_I . In the best case, a G_{II} amplitude of $0,004mJ/mm^2$ induces a lifetime superior to 2,3 million of cycles. In the worst case, a G_{II} amplitude of $0,034mJ/mm^2$, induces a minimum lifetime of 220 000 cycles. Here also results are really good, as the worst case close to the trend line and happening with a G_{II} amplitude of $0,034mJ/mm^2$ reached under $\Delta T_j=120K$ has a minimum lifetime already well above 100 000 cycles.

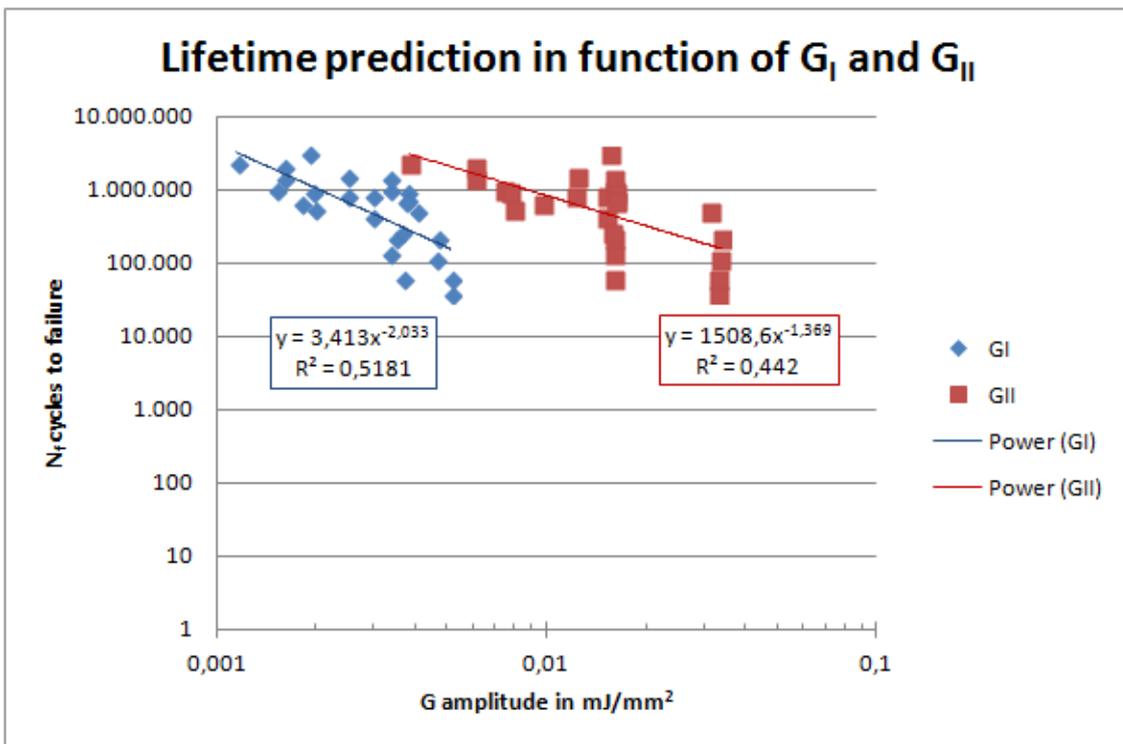


Figure 7.5: N_f EoT cycles in function of G_I and G_{II} amplitude for the crack at the interface chip/IMC

7.3.2 Bottom solder behavior

A lifetime model for the bottom solder is defined by stating that the EoL is reached when an increase in Z_{th} superior to 10%, and/or some cracks were observed in the bottom solder at the EoT. So, for those tests the EoT was defined as corresponding to the EoL. Thus, the results presented on the Figure 7.6, showing the lifetime prediction of the bottom solder in function of its acc creep strain, are not totally exact. But the Figure 7.6 is still a first good approximation of the lifetime prediction.

As it can be seen, the lack of data and of precision in the definition of the EoL, induce a lack of reliability in the determination of the trend line. Values of acc creep strain are spread out, ranging from 0,02% to 0,3% . For the lowest value of acc creep strain a lifetime of 1,5 million of cycles can be expected whereas for the highest amount of acc creep strain, the lifetime is divided by 24, leading to a lifetime of 62 000 cycles. This lifetime of 62 000 cycles appears to be quite low, but it has to be said that this lifetime was reached by testing under $\Delta T_j= 170K$, which is already quite severe loading condition. According to the lifetime model, in order

to have a lifetime equal or superior to 500 000 cycles, the acc creep strain has to stay equal or inferior to 0,08%. Thus this 0,08% of acc creep strain could define a critical limit for the bottom solder lifetime.

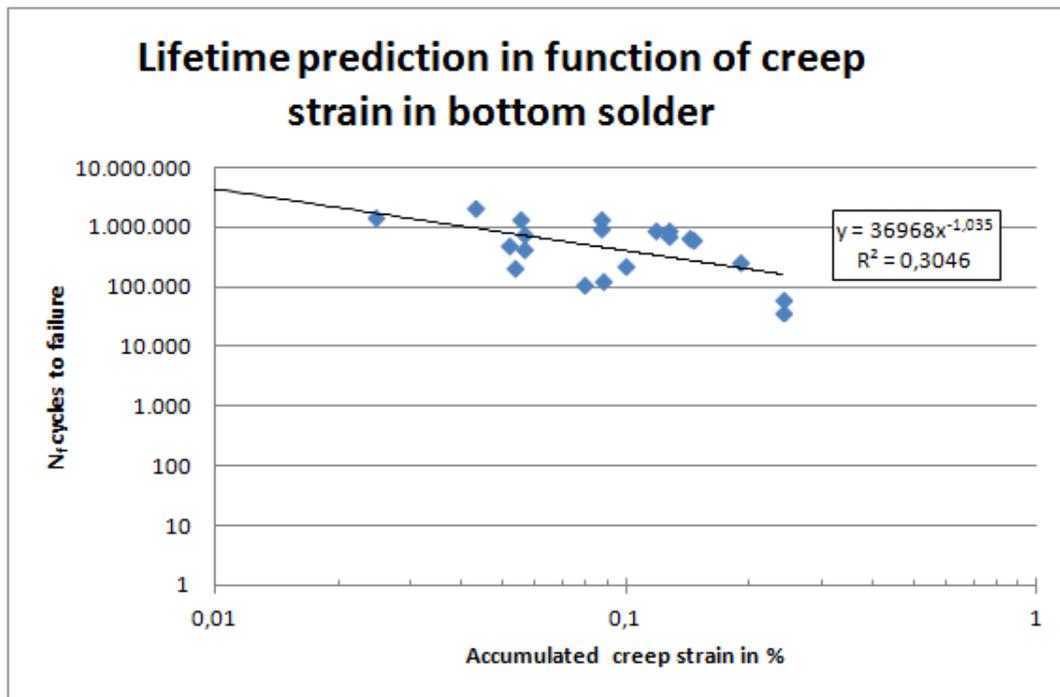


Figure 7.6: N_f cycles to failure in function of the acc creep strain in the bottom solder

7.3.3 Top solder behavior

For the determination of the top solder lifetime model, the method was approximately the same as for the bottom solder. The lifetime model was defined by stating that the EoL was reached when some cracks were observed in the top solder at the EoT. So here also the EoT was defined as corresponding to the EoL. Thus, the lifetime prediction presented Figure 7.7 for both paths of the top solder (close to the chip and close to the clip) is not totally exact but gives a first idea on lifetime expectations.

Data for the path close to the chip and close to the clip are in the same area of the graphic, but higher values of acc creep strain are reached with the path close to the clip. It is remarkable that the trend line of both paths is not really reliable. The worst fit is obtained for the path close to the chip. Actually the trend line is so unreliable for the path close to the chip, and the results so close to the ones obtained with the path close to the clip, that only the results of this last path are taken into account for the lifetime analysis. The lack of reliability also existing for the trend line of the path close to the clip may be explained by a lack of data and of precision in the definition of the EoL. The values of acc creep strain are ranging from 0,3% to 2%. For the lowest value of acc creep strain a lifetime of 1,5 million of cycles can be expected whereas for the highest amount of acc creep strain, the lifetime is divided by 24, leading to a lifetime of 62 000cycles. Just like for the bottom solder, this lifetime of 62 000 cycles appears to be low, but was reached under $\Delta T_j=170K$. Thus, the top solder layer can also be considered as robust. According to the lifetime model, in order to have a lifetime equal or superior to 500 000 cycles, the acc creep strain has to stay equal or inferior to 0,65%.

Thus the top solder is able to accumulate a lot more creep strain than the bottom solder and still reach the same lifetime as the bottom solder. It is so because unlike for the bottom solder, degradations in the top solder do not have any electrical consequences and have only a negligible thermal impact. So, damages in the top solder are less critical than damages in the bottom solder, and high amount of acc creep strain, around 0,6%, are acceptable in the top solder as it will not lead to a premature failure of the device.

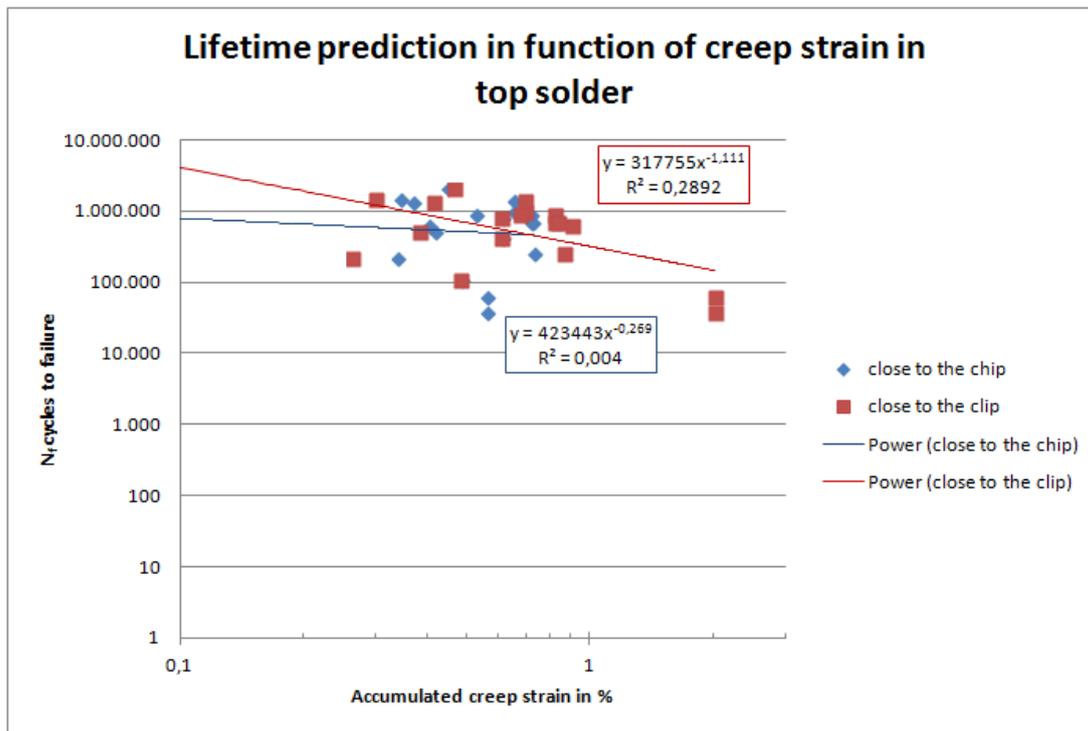


Figure 7.7: N_f cycles to failure in function of the acc creep strain in the top solder

7.3.4 Al metallization behavior

Al metallization lifetime models are determined using the improved EoL criterion, defined in the chapter 4 by an Al metallization degraded surface of 40%, corresponding to an increase of 40% in R_{DSon} and an increase of 3% in V_f . Thus here the lifetime models are more precise than the ones determined for the other layers as they really corresponds to EoL predictions. But with this improved EoL criterion, less data are available than with the initial EoL criterion ($V_f +1\%$), as some tests were stopped before reaching the EoL $V_f +3\%$. Hence a lack of reliability observed for the trend lines. First the lifetime is predicted in function of the acc plastic strain in the Al metallization Figure 7.8. The values of acc plastic strain are ranging from 0,13% to 2,2%, and the lifetime decreases quite rapidly in this interval. For the lowest amount of acc plastic strain, a lifetime of 2,4 million of cycles is reached, and for the highest amount of acc plastic strain the lifetime is divided by 45 and attains only 53 500 cycles. This lifetime of 53 500 cycles is quite short and was obtained by testing under $\Delta T_j = 170K$.

The Coffin Manson lifetime model deduced has the form:

$$N_f = 164309 \cdot (\varepsilon_{acc pl})^{-1,317} \quad \text{Eq. 7.2}$$

With $\varepsilon_{acc pl}$ the acc plastic strain in the Al metallization.

Thus in order to have a lifetime equal or superior to 500 000 cycles, the acc plastic strain has to stay equal or inferior to 0,43%. Thus this 0,43% of acc plastic strain could define a critical limit for the Al metallization lifetime. Here, lifetimes reached are always lower than the ones reached for the other layers, as the degradation of the Al metallization is the main failure mechanism leading to the device failure.

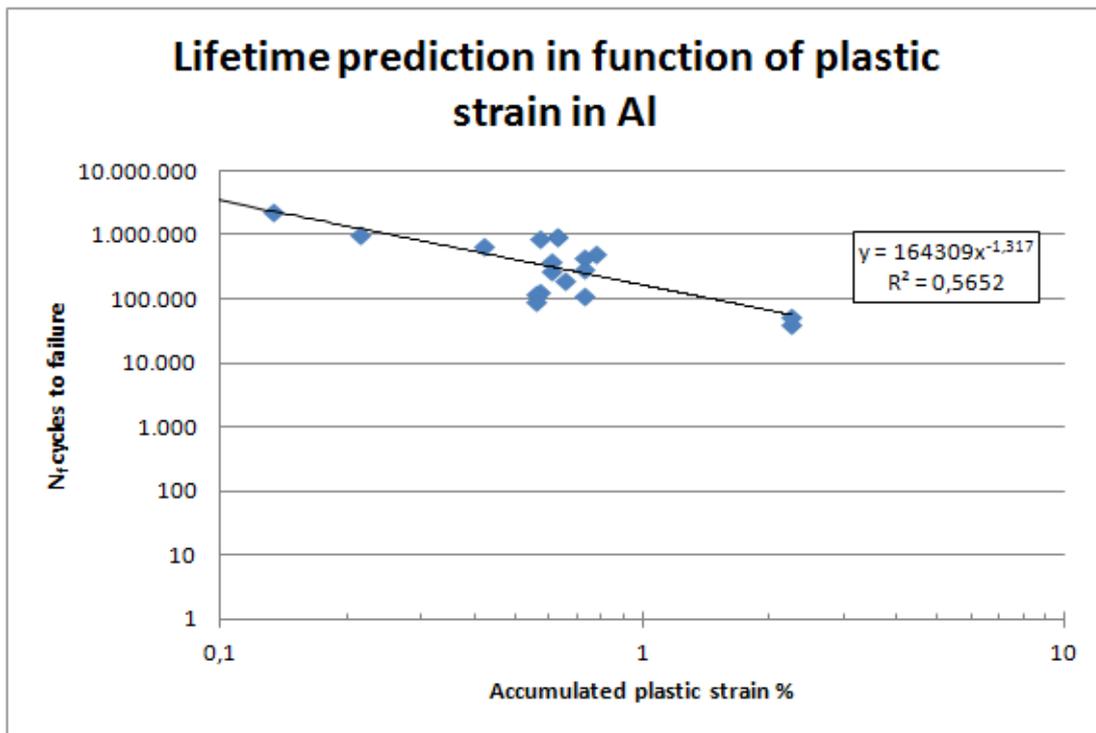


Figure 7.8: N_f cycles to failure in function of the acc plastic strain in the Al metallization

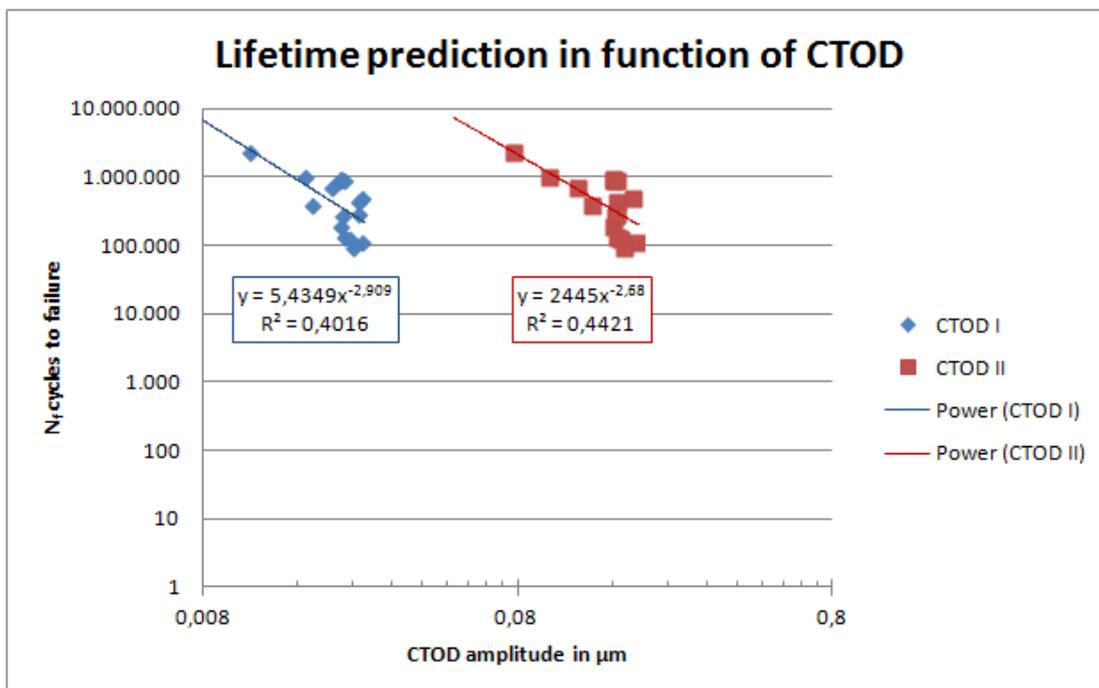


Figure 7.9: N_f cycles to failure in function of the $CTOD_I$ and $CTOD_{II}$ amplitudes in the Al metallization

Concerning the crack growth in the Al metallization, the lifetime is predicted in function of both $CTOD_I$ and $CTOD_{II}$ amplitudes Figure 7.9. For both $CTOD_I$ and $CTOD_{II}$, their trend lines are only moderately reliable. Then it appears clearly on the graphic that the opening mode generates smaller amplitude of displacements than the shearing mode. Trend lines of both CTOD have similar profile with a quite rapid lifetime decrease with increasing amplitude of CTOD, but still do not have the same slope and equation.

With a $CTOD_I$ amplitude of $0,011\mu\text{m}$ a lifetime of 2,4 million of cycles can be reached, whereas a $CTOD_{II}$ amplitude about 2 times higher, of $0,025\mu\text{m}$ induces a lifetime approximately divided by 5, with 450 000 cycles. These results are describing a very reliable module, as the worst case described was reached under $\Delta T_j=120\text{K}$ and has a lifetime already close to 500 000 cycles.

Regarding results of the mode II, with a $CTOD_{II}$ amplitude of $0,08 \mu\text{m}$ a lifetime of 2,4 million of cycles can be reached, and a $CTOD_{II}$ amplitude 2 times higher ($0,16 \mu\text{m}$), divides the lifetime by 8, with 292 000 cycles. Here also results are really good, as the worst case described was reached under $\Delta T_j=120\text{K}$ and still has a lifetime already above 100 000 cycles. The Coffin Manson lifetime model deduced has the form:

$$N_f = 2445 \cdot (\Delta CTOD_{II})^{-2,68} \quad \text{Eq. 7.3}$$

With $\Delta CTOD_{II}$ the amplitude of $CTOD_{II}$ at the crack tip in the Al metallization. Thus in order to have a lifetime equal or superior to 500 000 cycles, the amplitude of $CTOD_{II}$ has to stay equal or inferior to $0,14 \mu\text{m}$. Thus this $0,14 \mu\text{m}$ of amplitude of $CTOD_{II}$ could define a critical limit for the Al metallization lifetime.

7.3.5 IMC behavior

No particular EoL criterion can be defined for the top IMC, thus the number of cycles performed until the EoT is taken as the number of cycles to failure. So, lifetime models concerning the top IMC are not exact but are already giving a first idea of lifetime expectations.

The IMC lifetime is first predicted in function of the von Mises stress amplitude Figure 7.10. The trend line is moderately reliable, probably due to the lack of definition of an appropriate EoL criterion for the IMC layer. Values of von Mises stress amplitude are ranging from 90 MPa to 210 MPa. For the lowest value of stress amplitude a lifetime of 2,27 million of cycles can be expected. For the highest stress amplitude of 170 MPa, the lifetime attains 220 000cycles. This latter result is quite good for a test performed at $\Delta T_j=120\text{K}$. The worst case in terms of stress amplitude (210MPa) was reached with $\Delta T_j=170\text{K}$ and leads to a lifetime of 62 000 cycles. This is quite a short lifetime, but the loading conditions were severe and the data point does not lie on the trend line, thus signifying that this lifetime may be under-estimated. Thus the top IMC layer appears to be quite robust. According to the lifetime model, in order to have a lifetime superior or equal to 500 000cycles, the von Mises stress amplitude should remain equal or inferior to 152 MPa.

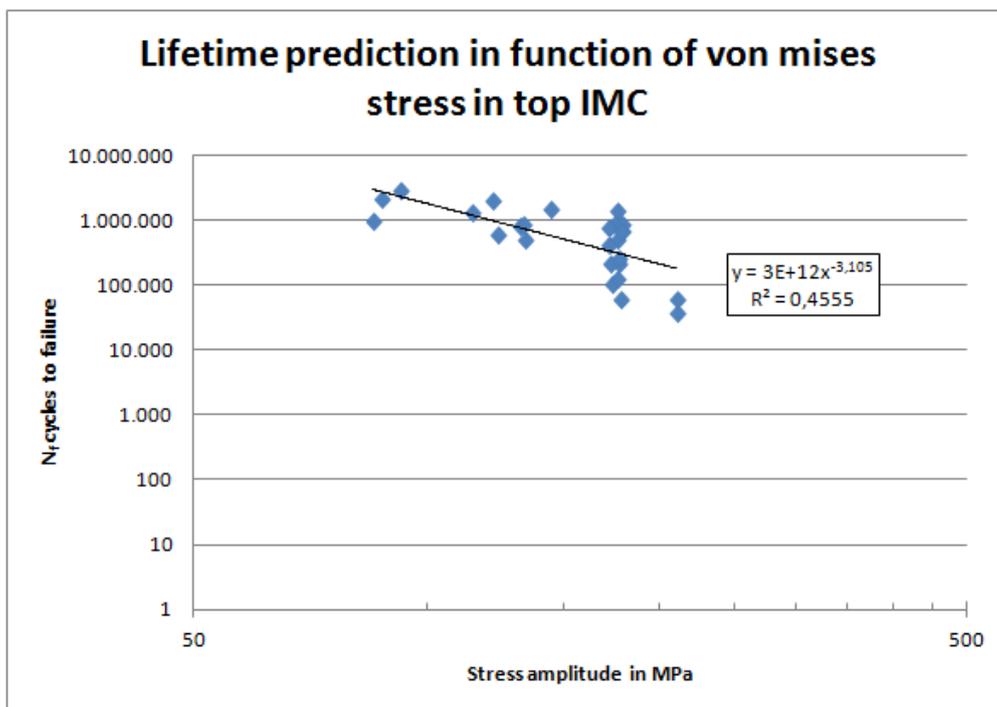


Figure 7.10: N_f cycles to failure in function of the von Mises stress amplitude in the top IMC

Then concerning the crack growth in the top IMC, the lifetime is predicted in function of both G_I and G_{II} amplitudes Figure 7.11. For both G_I and G_{II} , their trend lines are only moderately reliable. Then it appears clearly on the graphic that the values reached for G_I amplitude are lower than the ones reached for G_{II} . Values of G_I amplitudes are more spread out than the one obtained for G_{II} . With a G_I amplitude of $7,7e^{-6} \text{mJ/mm}^2$ a

lifetime of about 2,3 million of cycles can be reached. With a G_I amplitude of $2,7e^{-4} \text{mJ/mm}^2$ a lifetime of 220 000 cycles is expected. These results are quite good, as the worst case was reached under $\Delta T_j=120\text{K}$ and has a lifetime already well above 100 000 cycles.

Concerning the mode II, with a G_{II} amplitude of $0,004 \text{mJ/mm}^2$ a lifetime of about 2,3 million of cycles can be reached. In the worst case, a G_{II} amplitude of $0,04 \text{mJ/mm}^2$ induces a lifetime of 62 000 cycles. This lifetime is quite short but was obtained by testing under $\Delta T_j=170\text{K}$. According to the lifetime model, in order to have a lifetime superior or equal to 500 000 cycles, the G_{II} amplitude should remain equal or inferior to $0,016 \text{mJ/mm}^2$.

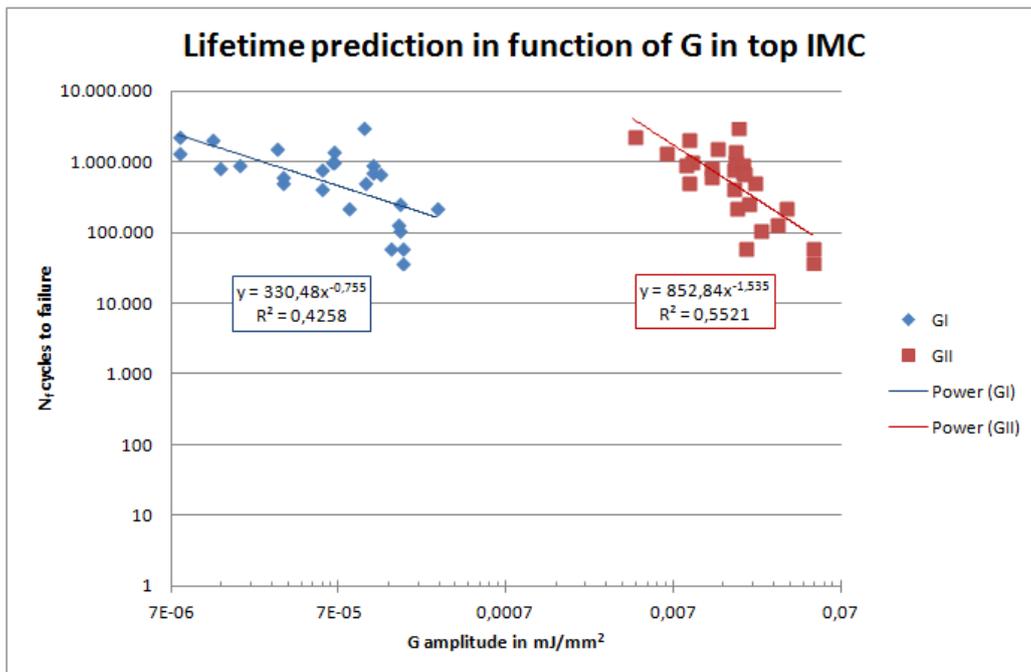


Figure 7.11: N_f cycles to failure in function of G_I and G_{II} amplitude in the top IMC

Conclusion and perspectives

The initial goal of this study was to highlight and understand the failure mechanisms that take place in a Cu clip module under Active Power Cycling (APC) tests. To reach this goal it was indispensable to perform both experiments and numerical simulations in combination.

APC tests are more complex to perform and to analyze in comparison to Passive Temperature Cycling (PTC) tests, which were already extensively studied and whose failure mechanisms are well identified. The first chapter reports the already existing knowledge on failure mechanisms observed to appear under APC for standard modules with wire bonds. Then all publications dealing with APC tests and simulations are reviewed and the types of modules, the test conditions as well as the analysis methods, the goal of studies and the lifetime estimations are summarized. This review highlights a lack of numerical investigations on the influence of tests parameters, especially for power modules with new technologies.

The Cu clip module under study is presented in detail in chapter 2. A particularity of this study is that very thin layers, such as the Al metallization and the IMCs, are taken into account in the simulation models. Moreover a lot of care was taken to properly simulate the material properties, thus resulting in a lot of non-linearity with the creep behavior of the solder layers, the elasto-plasticity of the Al metallization and the viscoelasticity of the mold.

The thermal behavior of the mold is first characterized with 1D and 2D simulations of thermal impedance Z_{th} presented in chapter 3. The 1D simulation shows that the main thermal path is at the back of the device, transporting the heat from the chip to the heat sink and is responsible of 95% of the heat conduction. The other 2 thermal paths with the heat flowing on top of the chip to the air through the mold or laterally to the heat sink through the Cu clip have a negligible thermal impact. Then, the time required for the module to reach its thermal steady state and the thermal inertia of the mold are highlighted through 2D simulation. Based on this knowledge and on the application's requirements a Design of Experiment (DoE) is established for the sensitivity study on test parameters.

About 30 APC tests with varying sets of test parameters (T_{jmin} , ΔT_j , and t_{on}) were carried out and their failure mechanisms are analyzed in chapter 4. Degradations are found to occur systematically in both solder layers, sometimes close to the interface with IMCs, in the Al metallization and in the mold. Cracks in the bottom solder are starting at the meniscus and propagates toward the center of the chip. Bottom solder degradation affects the thermal path and leads to an increase in the Z_{th} curve. In the Al metallization deformations and cracks are occurring beneath the top solder meniscus area. At this location, a migration of the Al layer in the top solder was sometimes observed. The Al metallization degradation induces a slight increase in the Z_{th} curve at the beginning of the measurement, and most importantly it generates also a significant increase in the R_{DSon} . At the top solder cracks are forming at the meniscus close to the interface with the chip or with the Cu clip and are propagating toward the center of the clip. Top solder degradation does not have significant influences neither on electrical functionality nor on the thermal path of the device. Finally delamination and cracks in mold are observed. Delamination takes place at the interface with solder meniscus, Cu lead frame and Cu clip and in the worst cases delamination propagates even more leading to the creation of cracks close to the lead frame or the clip. Tests were carried out without any End of Life (EoL) criterion defined. The definition of an EoL criterion adapted to our Cu clip module and based on the R_{DSon} increase is suggested. The criterion states that the EoL is reached when an increase in the forward voltage V_f of 3% is reached. This corresponds to an increase in R_{DSon} of 40%, which itself corresponds to 40% of degraded area in the Al metallization. Based on this EoL definition, the lifetime of the module is plotted in function of the temperature swing ΔT_j and is compared to lifetime estimations coming from the literature. This comparison shows the reliability of the Cu clip module and also highlights the fact that APC tests were never performed neither with $T_{jmin} = -30^\circ\text{C}$ nor with short pulse width like $t_{on}=0,2\text{s}$. Some tests were carried on longer after reaching the EoL but no catastrophic failure appeared, and the modules were still electrically functional. This shows the robustness of the Cu clip module.

All results of thermo-mechanical simulations are presented in chapter 5. First PTC is simulated and results obtained with the 2D model are compared to the ones obtained with the 3D model. Stresses and strains are found to be similar in both models, only small differences are visible for the top solder meniscus due to the simplified geometry of the 2D model. Thus the 2D model is validated and is further used for the rest of the study. The behavior of the module under PTC and under APC is studied in detail and compared for each layer of importance: the bottom solder, the chip, the Al metallization, the IMC, the top solder. For both PTC and APC, the in-plane stress is dominant in the module with the chip under compression and almost all other layers under tension. For both kinds of tests, solder layers suffer from creep effects at their extremities and the Al metallization undergoes plastic deformations beneath the top solder meniscus area. The major difference between both tests is that under PTC the bottom solder accumulates much more creep strain than under APC. Then, the sensitivity study for APC test is performed and the influence of the test parameters on stresses and strains in the different layers is determined. This study is also extended and some cases are calculated with a long t_{on} , a long and a short t_{off} , a thick Cu lead frame, a very large ΔT_j and with cracks and delamination in the mold. Long and short t_{on} and t_{off} are influencing the creep behavior of solder layers and sometimes the plastic deformation in the Al metallization. The thick Cu lead frame reduces the warpage amplitude and the plastic strain accumulated in the Al metallization as well as the accumulated creep strain under certain conditions. A large ΔT_j accelerates all failure mechanisms as it increases the warpage amplitude, as well as the creep strain accumulated in all solder layers and the plastic strain accumulated in the Al metallization. Finally mold delamination induces an increase in the amount of creep and plastic strain accumulated respectively in the solder layers and in the Al metallization.

Chapter 6 is dedicated to fracture mechanics simulations. 3 cracks are modeled: a delamination at the interface chip/bottom IMC which was an issue for other power modules, a crack in the Al metallization and a crack in the top IMC, as these last 2 cracks are characteristic failures occurring under APC. To interpret the crack growth of these 3 cracks, two different methods are manually implemented. The Virtual Crack Closing Technique (VCCT) which calculates the energy release rate G for mode I and II is used for the crack at the interface chip/IMC and for the crack in the top IMC. To interpret the crack growth in the Al metallization a mixed mode fracture criterion using the Crack Tip Opening Displacement (CTOD) method is implemented. Under PTC and APC and for all cracks the shearing mode attains the highest values of energy and displacements. This can be explained by the fact that the mold compresses the rest of the module and thus impedes the cracks opening. No values of fracture toughness are known for none of the 3 cracks modeled but according to the results obtained, the crack growth will probably occur along a local mode II.

Chapter 7 summarizes all results obtained from both experimental tests and simulations. It appears that under APC the main failure mechanism is the degradation of the Al metallization. Solder degradation occurs as a second failure mechanism. Thus it is the opposite of what happen under PTC. Then, the worst set of test parameters for each output parameter analyzed in each important layer are summarized on the Table 7.2. All deformations, stresses and strains of all layers are increasing with an increase in ΔT_j . Thus a large ΔT_j is indisputably an accelerating factor of failure mechanisms. Creep strain in solders requires high T_{jmin} and long t_{on} to accumulate whereas plastic strain in Al accumulates by low T_{jmin} and short t_{on} . Thus it is not possible to have simultaneously the worst case regarding plastic deformations in the Al metallization and the worst case regarding the accumulation of creep strain in solder layers. Moreover concerning the Al metallization, it is not the same failure mechanism that occurs under field loads $\Delta T_j=60K$ and under accelerated tests with $\Delta T_j=90K$ or $120K$. Thus, it is actually not possible to accelerate the failure mechanism of the Al metallization. Finally lifetime models were deduced by correlating the experimentally obtained lifetime with the corresponding calculated deformations, stresses, or strains.

This study is a first step in the understanding of failure mechanisms occurring in a Cu clip module under APC. The lifetime models deduced from this study can be further improved by carrying out more experiments with an improved test stand. Indeed, in order to improve the EoL criterion of the module, the Z_{th} and the R_{DSon} should be regularly measured during the APC tests and in adequate thermal conditions. Then to better reflect the real working conditions, superimposed tests can be performed. Those tests are combining PTC and APC by submitting the device to APC during the dwell times of the PTC. In the case of our Cu clip module, these tests can be spared as under both PTC and APC the module behavior is similar and the stress and strains have the same directions. This means that no additional information would be obtained by performing superimposed tests. Some further investigations can be carried out regarding the influence that delaminations and cracks in mold have on the rest of the module with different set of test parameters. It would also be

interesting to study the crack propagation in the Al metallization. Finally the method developed here which consists of performing a sensitivity study with experiments, thermo-mechanical and fracture mechanics simulations, can be further used to characterize the failure mechanisms occurring in other modules with different technologies, using, for example, silver sintering or ribbons.

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