Test Techniques for Analog Circuits and Systems

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Test Techniques for Analog Circuits and Systems

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Στο Δημητϱὸ και στη Δὴμητϱα

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Résumé en français

Le rôle des circuits analogiques

Les prévisions du début des années 1970 sur le fait que le traitement analogique serait sur le déclin en raison de l'avènement des ordinateurs numériques ne se sont jamais concrétisées. En fait, les avantages de l'informatique numérique sont devenus un facteur important pour l'omniprésence des circuits analogiques. Les principales raisons sont (a) le rôle important des capteurs et des actionneurs dans les systèmes modernes et la nécessité de créer leur interface avec le processeur de signaux numériques; (b) le rôle important des communications sans fil où les circuits analogiques forment l'interface de l'émetteur-récepteur avec l'extérieur; et (c) la nécessité d'améliorer la performance numérique, par exemple, la nécessité de remodeler par des moyens analogiques les impulsions numériques à haute vitesse qui sont déformées.

De nos jours, la tendance est à l'intégration des circuits analogiques avec des circuits numériques sur le même substrat de silicium. Lorsque cela est possible, il y a des avantages significatifs: le facteur de forme du système et la consommation de puissance sont réduits pendant que la vitesse de fonctionnement est augmentée. L'intégration à très grande échelle des circuits intégrés mixtes analogique-numérique est désormais courante dans presque tous les domaines d'applications qui utilisent des puces électroniques. Ces applications comprennent les télécommunications, l'électronique grand public, les ordinateurs, le multimédia, l'automobile, l'avionique, l'instrumentation biomédicale, la robotique, etc.

Vue générale des défis pour les circuits analogiques

Il y a plusieurs défis encore ouverts liés à la conception, la vérification et le test des circuits analogiques. En ce qui concerne la conception, il y a un manque flagrant d'outils efficaces qui permettent l'automatisation de la conception. La conception est toujours faite sur mesure et est considérée plutôt comme un art car il y a des degrés de liberté infinis, notamment dans le choix des topologies des circuits et des possibilités pratiquement infinies pour le dimensionnement des composants, la génération du layout, le placement et le routage. En outre, plusieurs facteurs doivent être pris en compte lors de la conception, tels que les variations technologiques due à la fabrication, la température, le bruit, les parasites, les effets du layout, etc. Un outil de synthèse qui génère automatiquement un circuit analogique qui présente un compromis concurrentiel parmi les performances souhaitées est devenu un Saint-Graal. En ce qui concerne la vérification pré-silicium, il est très chronophage voire même parfois impossible de vérifier que toutes les performances sont satisfaites à tous les cas extrêmes du procédé, tensions de polarisation et températures. Ceci est particulièrement vrai pour les circuits mixtes larges et complexes et pour certaines catégories des circuits analogiques qui présentent un temps de simulation transitoire très long, comme les convertisseurs et les circuits de type boucle à verrouillage de phase. Il est également très difficile de vérifier qu'un circuit analogique n'entrera pas dans un régime instable. En ce qui concerne la vérification post-silicium, il est très difficile de localiser le défaut à partir des quelques entrées et sorties primaires dont on dispose hors de la puce. L'accès limité aux nœuds internes et les boucles de rétroaction qui typiquement existent dans les circuits analogiques empirent la situation.

Ce travail se concentre sur la problématique du test des circuits analogiques. Dans les deux sections suivantes, nous allons discuter plus en détail l'objet de ce domaine de recherche et les défis qui restent encore ouverts.

Le rôle du test

Les circuits mixtes analogique-numérique intégrés à très grande échelle sont fabriqués en utilisant une série d'étapes, qui incluent l'impression photolithographique, la gravure, l'implantation, et la déposition chimique en phase vapeur. Ce procédé de fabrication est soumis à des imperfections qui peuvent provoquer des défaillances catastrophiques dans le fonctionnement des puces individuelles ou des variations dans les performances entre les puces sur la même plaquette ou entre les plaquettes à travers différentes lots. Les types de défauts catastrophiques comprennent les circuits ouverts et les court-circuits sur les lignes de métallisation et les connexions qui ont disparues ou ont été sous-gravées ou mal alignées. D'autres types de défauts peuvent ne pas être aussi facilement observables, mais aboutir à un écart de performance. Par exemple, les erreurs de dopage et les épaisseurs d'oxyde non-uniformes distribuées à travers la plaquette peuvent introduire des offsets et des distorsions.

De plus, il y a des imperfections dont l'impact est particulièrement important pour les circuits analogiques. Par exemple, en fonction de la forme tridimensionnelle des lignes de métallisation et leur espacement avec les couches adjacentes, il pourrait y avoir des parasites qui peuvent sérieusement affecter la réponse en haute fréquence. En outre, les circuits analogiques comptent beaucoup sur l'appairage entre les composants, pourtant, même si deux composants sont désignés dans une géométrie common-centroid et sont entourés par des environnements identiques, il est peu probable qu'ils se comportent exactement de la même façon en raison des désalignements des masques et des variations du procédé de fabrication.

Enfin, la performance d'un circuit intégré peut varier pendant la mise en boîtier. Par exemple, l'insertion de matière plastique sur la surface de la puce modifie la permittivité électrique près de la surface, ce qui peut affecter nœuds sensibles dans le circuit. D'autres événements catastrophiques qui peuvent se produire lors de la mise en boîtier comprennent les rayures superficielles, les fils de liaison brisés, et la décharge électrostatique.

Différents modes de défaillance, tels que ceux mentionnés ci-dessus, sont la raison pour laquelle chaque puce doit être testée avant d'être utilisée, afin d'assurer qu'elle répond aux spécifications de conception.

Défis pour le test des circuits analogiques

La pratique actuelle de test des circuits analogiques est basée sur la mesure directe des performances qui sont spécifiées dans le cahier des charges, une par une de manière séquentielle. Par la suite les performances sont comparées avec les spécifications pour déterminer si le circuit et bon ou défaillant. Cependant, malgré la facilité d'interpréter le résultat du test, ce processus standard résulte en un coût très élevé. D'une part, la mesure des performances analogiques complexes, comme la figure de bruit, la gigue, les non-linéarités, et le taux d'erreur de bit, nécessite un équipement de test automatique spécialisé avec des fonctionnalités avancées qui est très coûteux. D'autre part, un circuit analogique doit généralement être configuré consécutivement dans plusieurs configurations de test, afin de mesurer toutes les performances, ce qui entraîne des temps de commutation et de stabilisation très longs. En outre, les mesures doivent être répétées plusieurs fois et, par la suite, doivent être moyennées afin de modérer le bruit. Cela est nécessaire car les niveaux de signaux analogiques sont en baisse en raison de la diminution des tensions d'alimentation, tandis que le bruit thermique est en hausse en raison de l'augmentation simultanée des bandes passantes analogiques. La procédure de mesure complexe décrite ci-dessous doit être répétée pour différents modes de fonctionnement, tels que différentes charges en sortie du circuit sous test, conditions de température et plusieurs niveaux de tension d'alimentation. En guise de résumé, ce processus standard pour effectuer le test résulte en un temps très long et, par extension, devient très coûteux.

Le coût pour tester un seul transistor dans un système mixte analogique-numérique est resté presque constant au cours des dernières décennies alors que le coût de fabrication d'un seul transistor est en baisse constante, suivante la fameuse loi de Moore. Si cette tendance se poursuit, il est prédit que très bientôt il coûtera plus cher de tester un seul transistor que de le fabriquer. Ainsi, il n'y aurait pas d'incitation économique à miniaturiser d'avantage la technologie à moins que le coût du test soit réduit. Alors que le coût de test pour les circuits numériques est en baisse constante grâce aux fréquences d'horloge plus élevées et au plus grand parallélisme permis grâce au test par balayage, le coût de test pour les circuits analogiques est en augmentation constante car la complexité des systèmes augmente tandis que l'industrie adhère encore au processus du test standard décrit ci-dessus. En d'autres termes, les circuits analogiques deviennent responsables de la plus grande part du coût de test, en dépit du fait qu'ils occupent un espace beaucoup plus petit sur la puce par rapport aux circuits numériques.

À cet égard, la marge la plus importante pour la réduction des coûts de test est en particulière le test des circuits analogiques. Avec les niveaux toujours croissants d'intégration des systèmes sur puce et en trois dimensions, qui comprennent de plus en plus des circuits analogiques, le coût de l'équipement de test automatique, le temps pour le développement des tests ainsi que le temps d'exécution des tests sont de plus en plus touchés et ne cesseront pas d'augmenter à mesure que nous nous dirigeons vers des nœuds technologiques avancés. Par conséquent, le test analogique est aujourd'hui un domaine d'intérêt et d'innovation pour l'industrie de la microélectronique.

Les niveaux toujours croissants de l'intégration des systèmes sur puce et en trois dimensions, en dehors de l'augmentation du coût de test, posent des défis de test significatifs liés au routage, à la contrôlabilité et l'observabilité limitées des signaux de test. En outre, le nombre élevé de pins des systèmes sur puce et en trois dimensions nécessite une programmation sophistiquée pour tester complètement toutes leurs fonctions. Enfin, même si le processus de test des circuits analogiques individuels décrit ci-dessous peut être appliqué dans ce contexte, il n'est pas garanti que les circuits analogiques fonctionnent correctement dans l'application finale à cause des interférences avec les circuits numériques environnants. Ainsi, plus de tests de niveau système sont nécessaires, afin de répondre à des phénomènes de diaphonie.

Les circuits analogiques qui passent le test de production peuvent tomber en panne plus tard dans le domaine d'application pendant leur fonctionnement normal en raison du vieillissement, des effets de leur environnement, ou des erreurs transitoires. Dans les cas où les circuits analogiques font partie d'un système qui est utilisé dans une application critique ou dans une application qui est commandée à distance, par exemple un réseau de capteurs, il est nécessaire d'équiper les circuits analogiques avec des capacités d'autotest en ligne, afin de détecter le risque de défaillance dès le début, localiser la panne et retraiter l'information. En outre, pour corriger les erreurs permanentes, il est nécessaire de rendre les circuits tolérants aux fautes, dans le sens où ils peuvent s'adapter aux changements à travers des réglages ou même des reconfigurations.

Les techniques de test sont également utiles dans le contexte du diagnostic. Le diagnostic des causes de panne des premiers prototypes aide à réduire les itérations de conception et d'atteindre l'objectif de temps pour la mise sur le marché. Dans la production à grand volume, le diagnostic des causes de panne aide les concepteurs à rassembler des informations précieuses pour améliorer le rendement dans les générations futures de produits. Le diagnostic joue également un rôle crucial dans le cas des défaillances pendent la phase d'opération pour les applications critiques. Plus précisément, il est important d'identifier les causes de panne afin de réparer le système si possible et appliquer des actions correctives qui empêcheront la réapparition de panne et, de ce fait, renforcer la fiabilité des dispositifs.

Contributions

L'essentiel de la discussion ci-dessus est que des techniques de test alternatives à faible coût doivent être développées, qui pourraient efficacement remplacer le processus standard très coûteux qui est actuellement appliqué dans la production à grand volume. Ces techniques devraient cibler la réduction du temps de test et/ou atténuer la nécessité de compter sur des équipements automatiques de test spécialisés. Elles pourraient être génériques, c'est-à-dire pratiquement applicables à toutes les catégories de circuits, ou spécifiques au circuit sous test en exploitant ses propriétés inhérentes.

Cependant, l'introduction des techniques de test alternatives ne devrait pas sacrifier la haute précision des tests standards, qui est mesurée par des métriques de test telles que la couverture de fautes (circuits défectueux détectés par le test) et la perte de rendement (circuits fonctionnels qui ne passent pas le test). Par conséquent, une technique de test alternative devrait être évaluée en estimant les métriques de test qui en résultent.

Les techniques de test sont également nécessaires pour le suivi de l'état du système pendant son opération soit concurremment avec le fonctionnement normal soit en utilisant une période d'inactivité. Dans ce cas, les techniques de test doivent être nécessairement entièrement embarquées, sans compter sur des appareils de mesure externes. Il est clair que les défis sont beaucoup plus importants puisque les circuits de test embarqués devrait (a) avoir une surface minimum dans la puce, (b) être robustes dans le sens où ils devraient avoir une probabilité de défaillance considérablement négligeable par rapport à la probabilité de défaillance du système lui-même, et (c) être non intrusifs dans le sens où ils ne doivent pas dégrader les performances du système sous test obtenues par conception.

Enfin, les techniques de test sont nécessaires pour guider correctement l'analyse de diagnostic et de défaillance. Les techniques de test embarquées peuvent offrir de meilleurs aperçus sur les modes de défaillance et identifier les défauts avec plus de rigueur. Dans ce cas, les techniques de test doivent être accompagnées d'un logiciel de post-traitement dédié pour être en mesure de diagnostiquer les défaillances jusqu'au niveau transistor tout en ayant accès à seulement quelques entrées et sorties primaires et les sorties du circuit de test embarqué.

Dans le chapitre 1, nous présentons une introduction aux défis liés aux circuits analogiques et nous nous concentrons en particulier sur la problématique du test. Nous fournissons également un aperçu du manuscrit.

Dans le chapitre 2, nous nous concentrons sur un paradigme de test alternatif et générique basé sur des idées empruntées au domaine de l'apprentissage automatique. Ce paradigme de test a un potentiel élevé pour réduire le coût de test des circuits analogiques. Nous présentons un flux de test adaptatif basé sur l'apprentissage automatique qui, en plus d'être bas coût, offre également une grande confiance dans les décisions prises. Nous présentons aussi l'application du "Bayesian Model Fusion" dans le but de commencer à déployer ce paradigme de test dès le début de la production à grand volume sans avoir à attendre d'avoir recueilli au préalable un échantillon de circuits large et représentatif des variations du procédé de fabrication. Enfin, nous présentons un algorithme basé sur l'apprentissage automatique afin d'extraire les informations redondantes dans un ensemble de tests standards et, par conséquent, d'identifier un sous-ensemble des tests standards qui peut être appliqué sans sacrifier la précision du résultat du test.

Dans le chapitre 3, nous présentons des techniques de test embarqués de faible surface pour les circuits radiofréquence (RF) et deux types des convertisseurs analogiques-numériques (CAN), en particuliers les $\Sigma\Delta$ et pipeline. La propriété majeure de la technique de test embarqué pour les circuits RF est qu'elle est non-intrusive, ce qui dissocie complètement la conception et le test. La propriété majeure de la technique de test embarqué pour les CAN $\Sigma\Delta$ est qu'elle est entièrement numérique permettant une mise en œuvre robuste. La propriété majeure de la technique de test embarqué pour les CAN pipeline est qu'elle exploite des propriétés inhérentes de leur architecture offrant la plus grande réduction possible du coût de test statique. Enfin, nous présentons une architecture de test embarquée neuro-morphique générique qui emploie un réseau de neurones sur puce pour traiter les mesures à faible coût et pour prendre des décisions directes, par exemple si le circuit est défectueux ou non, sur puce.

Dans le chapitre 4, nous présentons des techniques de simulation statistiques qui sont rapides et génériques et qui peuvent être facilement utilisées pour calculer de manière efficace les métriques de test et, ainsi, pour optimiser les limites de test afin de parvenir à des compromis souhaités entre les mesures de test d'intérêt. En particulier, nous couvrons les techniques d'évaluation des métriques de test basés sur l'estimation de la densité et sur la génération des circuits extrêmes. Nous allons également discuter l'application de la théorie des valeurs extrêmes pour quantifier les métriques de test avec un niveau de précision de l'ordre des quelques parties par millions. Nous nous attendons que des techniques telles que celles proposées vont devenir un outil précieux dans les mains des ingénieurs de test pour affiner les programmes de génération de tests à un stade précoce de la conception, afin d'évaluer des solutions de test existantes et de les comparer avec celles qui sont continuellement proposées en vue de réduire le coût élevé des tests standards.

Dans le chapitre 5, nous présentons une méthodologie pour la modélisation des défauts et le diagnostic des circuits analogiques basées sur l'apprentissage automatique. L'approche proposée est capable de diagnostiquer les défauts à la fois catastrophiques et paramétriques sans faire aucune hypothèse a priori sur le type de défaut qui a eu lieu. Un filtre de défaut reconnaît le type de défaut, paramétrique ou catastrophique, et décide quelle méthodologie à employer. Les circuits avec défauts catastrophiques sont transmis à une combinaison de classificateurs multi-classes qui énumèrent les fautes catastrophiques en fonction de leur probabilité d'occurrence. Les circuits avec défauts paramétriques sont transmis à des fonctions de régression qui prédisent les valeurs d'un ensemble de paramètres de conception prédéfinis en niveau transistor, afin de localiser et de prédire le paramètre défectueux. Nous discutons également brièvement les complexités souvent rencontrées dans les études de cas réels liées à des valeurs manquantes dans les données.

Les méthodes proposées dans tous les chapitres seront démontrées avec des résultats de simulation et des résultats expérimentaux basés sur des données industrielles et sur des puces fabriquées.

Enfin, dans le chapitre 6, nous présentons des directions pour les travaux futurs.

Curriculum Vitae

Personal Data

- Born in Athens, Greece, November 1978

Education

- Yale University, USA, Engineering and Applied Science Department, Sep ’01 - Dec ’06
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- Design-for-test, built-in self-test, self-healing, on-line test, and failure analysis techniques for analog, mixed-signal, and RF circuits and systems, machine learning, computer-aided design

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- Marie Curie MIRG-CT-2007-209653, “Machine Learning-Based Test Solutions for Reliable Mixed-Signal/RF Integrated Devices,” Nov ’07 - ’11
- Catrene CT-302 TOETS, “Towards One European Test Solution,” Apr ’09 - ’12
- Research contract with Infiniscale, “Calcul de haut rendement global,” Jun ’11 - ’12
- ANR SACSO, “Solutions for the self-Adaptation of Communicating Systems in Operation,” Jan ’12 - ’15

- ENIAC No. 296112-2 ELESIS , “European Library-based flow of Embedded Silicon test Instruments,” Apr ’12 - ’15
- CNRS/INS2I Projet P-SoC , “Self-healing and self-adapting RF circuits,” 2013

Awards and Fellowships

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- Best Paper Award, *2012 IEEE European Test Symposium*
- Best Student Paper Award, *2011 IEEE International Mixed-Signals, Sensors, and Systems Test Workshop*
- Best Paper Award, *2009 IEEE European Test Symposium*
- Yale University Fellowship, Sep ’01 - Sep ’06
- Yale Conference Travel Fund (CTF) Award, 2006
- IEEE Computer Society Test Technology Technical Council Doctoral Thesis Award, third place winner, 2005
- Stavros S. Niarchos Research Fellowship, summer 2003
- Commercial Bank of Greece Award for Academic Excellence, 1998-2001

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68. A. Dimakos, M. Andraud, L. Abdallah, H.-G. Stratigopoulos, E. Simeu, and S. Mir, "Test and calibration of RF circuits using built-in non-intrusive sensors ," *IEEE Computer Society Annual Symposium on VLSI*, Invited Talk in Special Session, Montpellier, France, July 2015
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72. H.-G. Stratigopoulos, "RF Built-In Test with Non-Intrusive Sensors," *IEEE VLSI Test Symposium*, Elevator Talk, Napa, CA, USA, April 2014
73. L. Abdallah, H.-G. Stratigopoulos, S. Mir, "Implicit Test of High-Speed Analog Circuits Using Non-Intrusive Sensors," *IEEE European Conference on Circuit Theory and Design*, Invited Talk in Special Session, Linköping, Sweden, August 2011
74. H.-G. Stratigopoulos, "Statistical Learning for Analog Circuit Testing," *Design & Technology of Integrated Circuits in Nanoscale Era*, Embedded Tutorial, Athens, Greece, April 2011
75. H.-G. Stratigopoulos, "Adaptive Analog Alternate Test," *IEEE Latin-American Test Workshop*, Invited Talk in Special Session, Porto de Galinhas, Brazil, March 2011
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77. S. Mir, H.-G. Stratigopoulos, and A. Bounceur, "Density Estimation for Analog/RF Test Problem Solving," *IEEE VLSI Test Symposium*, Invited Talk in IP Session, Santa Cruz, California, USA, April 2010
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Patents

79. S. Mir, H.-G. Stratigopoulos, M. Dubois, "$\Sigma\Delta$ ADC with test circuitry", US Patent 8,830,098, 2014

Teaching Responsibilities

- Teaching Fellow, EENG 462 Testing & Design for Testability, Yale University, Spring 2003
- Teaching Fellow, EENG 227 Circuits & Electronics Lab, Yale University, Fall 2003
- Teaching Fellow, EENG 227 Circuits & Electronics Lab, Yale University, Fall 2004 and Spring 2005

Current Ph.D. Student Advisees

- Mr. Athanassios Dimakos
  Grenoble INP, EEATS
  2nd year Ph.D. student
  Thesis Title: "Built-In Test in Wireless Systems Using Non-Intrusive Sensors"
- Mr. Martin Andraud
  Grenoble INP, EEATS
  2nd year Ph.D. student
  Thesis Title: "Solutions for the Self-Adaptation of Wireless Systems"

Former Ph.D. Student Advisees

- Dr. Asma Laraba
  Grenoble INP, EEATS
  Thesis Title: "Built-In Self-Test of Pipeline ADCs"
  Defense Date: 20/9/2013
  Current Position: XILINX, San Jose, CA, USA
- Dr. Louay Abdallah
  Grenoble INP, EEATS
  Thesis Title: "Non-Intrusive Sensors for Built-in-Test of RF Circuits"
  Defense Date: 22/10/2012
  Current Position: Dolphin Integration, Grenoble, France
- Dr. Ke Huang
  Grenoble INP, EEATS
  Thesis Title: "Fault Modelling and Diagnosis for Nanometric Mixed-Signal/RF Circuits"
  Defense Date: 16/11/2011
  Current Position: Assistant Professor, San Diego State University, San Diego, CA, USA
- Dr. Matthieu Dubois
  Grenoble INP, EEATS
  Thesis Title: "Methodology for Estimating Test Metrics Applied to a Novel Built-In Self-Test (BIST) Technique for $\Sigma\Delta$ Converters"
  Defense Date: 23/6/2011
  Current Position: EASii IC, Grenoble, France

Professional Service

Organizing Committee Member

- Test Technology Technical Council (TTTC) Student Activities Group, E.J. McCluskey Best Doctoral Thesis Contest, *IEEE VLSI Test Symposium* (VTS '09 -'10)

- *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop* (IMS3TW '09 -'10) - Publications Chair
- *IEEE International Workshop on Test and Validation of High Speed Analog Circuits* (TVHSAC '10, '13) - Program Chair
- *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop* (IMS3TW '11) - Program Chair
- *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop* (IMS3TW '12, '14) - Program Co-Chair
- *Design, Automation and Test in Europe Conference* (DATE '14) - Topic Chair
- *Design, Automation and Test in Europe Conference* (DATE '13, '15) - Topic Co-Chair
- *IEEE European Test Symposium* (ETS '14, '16) - Program Co-Chair
- *IEEE European Test Symposium* (ETS '15) - Topic Chair
- *IEEE International Mixed-Signals Test Workshop* (IMSTW '15) - General Chair
- *IEEE European Test Symposium* (ETS '17) - Program Chair

Technical Program Committee Member

- *IEEE International On-Line Testing Symposium* (IOLTS '08 -'15)
- *Design, Automation and Test in Europe Conference* (DATE '11-'16)
- *IFIP/IEEE International Conference on Very Large Scale Integration* (VLSI-SoC '12-'14)
- *IEEE International Conference on Computer-Aided Design* (ICCAD '12-'14)
- *IEEE VLSI Test Symposium* (VTS '13-'16)
- *IEEE Great Lakes Symposium on VLSI* (GLSVLSI '13-'14)
- *European Workshop on CMOS Variability* (VARI '14-'15)
- *International Conference on Design & Technology of Integrated Systems in Nanoscale Era* (DTIS '14-'15)
- *IEEE International Test Conference* (ITC '15)
- *Frontiers on Analog CAD* (FAC '15)
- *IEEE International Workshop on Test and Validation of High Speed Analog Circuits* (TVHSAC '15)

Editor

- *Springer Journal of Electronic Testing: Theory & Applications* (JETTA)

  Guest Editor of Special Issue on “Analog, Mixed-Signal, RF, and MEMS Testing”

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  Associate Editor since January 2012

- *IEEE Design & Test of Computers*
  Guest Editor of Special Issue on "Digitally Enhanced Wireless Transceivers"
  Date of publication: November/December 2012
- *IEEE Design & Test of Computers*
  Associate Editor since December 2011
- *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*
  Associate Editor since October 2012

Technical Referee in additional journals and conferences

- *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* (TVLSI)
- *IEEE Transactions on Circuits and Systems I* (TCAS-I)
- *IEEE Transactions on Circuits and Systems II* (TCAS-II)
- *ASP Journal of Low Power Electronics* (JOLPE)
- *Wiley International Journal of Circuit Theory and Application*
- *IEEE Asian Test Symposium* (ATS)

Participation in Ph.D. Juries

- Eduardo Aldrete, "Strategies for built-in performance monitoring of analog RF circuits with temperature measurements," Universitat Politècnica de Catalunya, Spain, September 2010
- Dídac Gómez Salinas, "Design of Reconfigurable RF circuits for Self-Compensation," Universitat Politècnica de Catalunya, Spain, January 2013

Panelist

- *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop* (IMS3TW '09)
  Title: "AMS/RF/sensor testing: can alternate test or BIST replace functional test? Success stories and their limitations."
- *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop* (IMS3TW '12)
  Title: "How Best Can We Deploy Analog/Mixed-Signal DFT Solutions?"
- *IEEE VLSI Test Symposium* (VTS '15)
  Title: "Analog/RF BIST: Are we there yet?"
- *IEEE European Test Symposium* (ETS '15)
  Title: "Is adaptive testing the panacea for the future test problems?"

Panel/Special Session Organizer

- *IEEE VLSI Test Symposium* (VTS '10)
  Title: "Adaptive Analog Test: Feasibility and Opportunities Ahead"
- *IEEE International On-Line Testing Symposium* (IOLTS '10)
  Title: "On-Line Monitoring for Analog and Sensor-Based Systems"
- *IEEE International On-Line Testing Symposium* (IOLTS '14)
  Title: "Solutions for the Self Adaptation of Communicating Systems in Operation"

Session Chair

- *IEEE VLSI Test Symposium* (VTS ’08 - ’09)
- *IEEE International On-Line Testing Symposium* (IOLTS ’08 -’10,’13)
- *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop* (IMS3TW ’09 -’10, ’12,’14)
- *Design, Automation and Test in Europe Conference* (DATE ’11-’12)
- *IEEE European Test Symposium* (ETS ’11,’13,’15)
- *IEEE European Conference on Circuit Theory and Design* (ECCTD ’11)
- *IEEE International Conference on Computer-Aided Design* (ICCAD ’11)

Professional Associations

IEEE, Test Technology Technical Council, Technical Chamber of Greece

Chapter 1

Introduction

1.1 The role and place of analog circuits

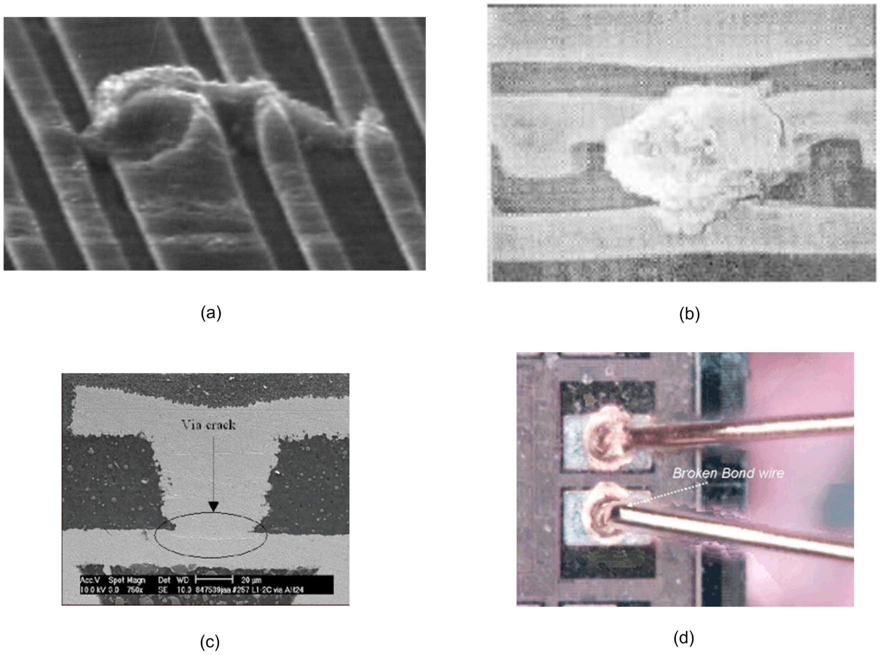
The forecast in the early 1970s that analog processing would decline due to the advent of digital computers was never materialized. In fact, the advantages in digital computing became a key factor for the increased pervasiveness of analog circuits. The main reasons are (a) the expanding role of sensors and actuators in modern systems and the need to interface them with the digital signal processor; (b) the expanding role of wireless communications where analog circuits form the front-end of the transceiver; and (c) the need to enhance digital performance, for example, the need for reshaping distorted high-speed digital pulses by analog means.

The trend nowadays is towards integrating analog circuits together with digital circuits onto the same silicon substrate. When feasible, this marriage offers significant advantages: the system form factor and power dissipation are reduced and the speed of operation is increased. Mixed analog-digital very large-scale integration (VLSI) chips are now commonplace in practically every broad application area in which chips are used. Such areas include telecommunications, consumer electronics, computers and related equipment, multimedia, automotive, avionics, biomedical instrumentation, robotics, etc.

1.2 Overview of analog circuit challenges

There are several open challenges related to the design, verification, and testing of analog circuits. Regarding analog circuit design, there is a striking lack of efficient design automation tools. Analog designs are still custom-made and more like an art since there are endless degrees of analog design freedom. There are several circuit topologies to choose from and practically infinite possibilities for component sizing, layout generation, placement, and routing. In addition, several factors need to be taken into account during the design, such as process and temperature variations, noise, on-chip interferences, parasitics, layout effects, etc. A synthesis tool which automatically generates an analog circuit that presents a competitive trade-off amongst the desired performances has become a holy grail. Regarding pre-silicon verification, it is very time-consuming, if possible at all, to verify that all performances are satisfied at all process, voltage, and temperature corners. This is particularly true for large analog-digital designs and certain classes of analog circuits with long transient simulation times, such as data converters and phase locked loops. It also very challenging to verify that an analog circuit will not enter an unstable regime. Regarding post-silicon verification, it is very challenging to locate the bug due to the few primary inputs and outputs, the limited access to internal nodes, and the feedback loops that typically analog designs contain.

This work focuses on the problem of analog circuit testing. In the following two Sections we will discuss in more details the purpose of testing and the open challenges in analog circuit testing.



(a) (b)

(c) (d)

Figure 1.1: (a) Resistive short in adjacent metallization layers; (b) surface defect caused by particulate matter landing on the surface of the wafer or on a photographic mask during one of the processing steps; (c) a cracked via; (d) broken bond between a wire connecting the lead frame of the package to a bond pad of the die.

1.3 The role of testing

VLSI chips are fabricated using a series of photolithographic printing, etching, implanting, and chemical vapor deposition steps. This process is subject to imperfections that may cause catastrophic failures in the operation of individual chips or variations in performance amongst chips on the same wafer or across different wafers in different lots. Catastrophic defect types include short- and open-circuits, and missing, under-etched or misaligned vias. Fig. 1.1(a)-(c) show a few scanning electron microscope (SEM) photographs of such defects. Other types of defects may not be as easily observable, but result in performance deviation that can range from minor to catastrophic. For example, doping errors and non-uniform distributed oxide thicknesses across the wafer can introduce large offsets and distortions.

Moreover, there are imperfections whose impact is especially important for analog circuits. For example, depending on the three-dimensional shape of metal lines and their spacing to adjacent layers, there might be parasitics that can seriously affect the high frequency response. In addition, analog designs rely heavily on matched devices, yet, even if two devices are laid out in common-centroid geometry and surrounded by identical environments [1], it is unlikely that they behave exactly the same due to mask misalignments and process drifts.

Finally, the performance of an integrated circuit could shift in the post-silicon production flow, during the packaging process. For example, the insertion of plastic over the surface of the die alters the electrical permitivity near the surface. Consequently, trace-to-trace capacitances are increased, which may affect sensitive nodes in the circuit. In addition, the injection-molded plastic introduces mechanical stresses in the silicon. Other catastrophic events that can occur during packaging include surface scratches, broken bond wires, as shown in Fig. 1.1(d), and surface explosions caused by electrostatic discharge in a mishandled device.

Failure modes such as these listed above are the reason why each chip must be tested before it is used, in order to ensure that it meets its design specifications.

1.4 Challenges in analog circuit testing

The current practice for testing analog circuits is specification-based testing [2–5]. Specification-based testing involves direct measurement of the performances that are promised in the specification data sheet one by one in a sequential fashion. However, despite the ease of interpreting the test result, specification-based testing incurs a very high cost. On one hand, measuring complex analog performances, such as noise figure, jitter, nonlinearity, and bit error rate, requires specialized Automatic Test Equipment (ATE) with advanced capabilities which is very costly. On the other hand, an analog circuit typically needs to be configured consecutively in multiple test configurations, in order to address all performance parameters. This results in lengthy switching and settling times. In addition, measurements have to be repeated multiple times and, subsequently, averaged, in order to moderate noise. This is necessary since analog signal levels are decreasing due to decreasing power supply voltages, while thermal noise is increasing due to the simultaneous increase of analog bandwidths. The described elaborate measurement procedure needs to be repeated under various operation modes, such as different output loads, temperatures and power supply levels. Thus, specification-based testing is a time consuming and, by extension, a costly process.

The cost to test a single transistor in a mixed analog-digital system has remained almost constant in the past few decades while the cost to manufacture a single transistor is constantly dropping, following the famous Moore's law. If this trend continues, it is predicted that very soon it would cost more to test a single transistor than to fabricate it. Thus, there would be no economical incentive to further miniaturize the technology unless the test cost is reduced. While the test cost for digital circuits is being constantly reduced thanks to the higher clock rates and the greater parallelism permitted by scan-based tests, the test cost for analog circuits is increasing since the system complexity increases while industry still adheres to the straightforward specification-based testing paradigm. In other words, analog circuits are becoming responsible for the largest fraction of the test cost, despite the fact that they occupy a much smaller area on the die compared to their digital counterparts [6]. In this respect, the most important frontier for test cost reduction is analog circuit testing. With the ever-increasing levels of integration of Systems-on-Chip (SoCs) and three-dimensional (3-D) designs, more and more of which include analog circuits, ATE cost, test development, and test execution times are being increasingly impacted and will keep increasing as we move towards more advanced technology nodes. Therefore, analog testing is nowadays an area of focus and innovation for the microelectronics industry.

The ever-increasing levels of integration of SoCs and 3-D designs, apart from increased test cost, pose significant test challenges related to routing and the limited controllability and observability of test signals. In addition, the high pin count of SoC and 3-D chips requires sophisticated programming to thoroughly test all their functions. Finally, even if specification-based testing of individual analog circuits can be applied in this context, it is not guaranteed that analog circuits would operate correctly in the end application due to interference with the surrounding digital circuitry. Thus, more system-level tests are necessary, in order to address crosstalk phenomena.

Analog circuits that pass post-manufacturing testing might fail later in the field during normal operation due to ageing, environmental effects, or transient errors. In cases where analog circuits are part of a larger safety-critical, mission-critical, or remote-controlled system, it is required to equip them with on-line self-testing capabilities, in order to detect early reliability hazards, pinpoint the failure mechanisms, and reprocess the information. Furthermore, to address permanent errors, it is required to render the circuits fault-tolerant, in the sense that they can adapt to changes through calibration, tuning, or even re-configurability.

Test techniques are also valuable in the context of diagnosis. Diagnosing the root-causes of failures in the first prototypes helps reducing design iterations and meeting the time-to-market goal. In high-volume production, diagnosing the root-causes of failures assists the designers in gathering valuable information for enhancing yield in future product generations. Diagnosis is also of vital importance in the case of failures in the field for safety-critical applications. Here, it is important to identify the root-causes of failures so as to repair the system if possible and apply corrective actions that will prevent failure re-occurrence and, thereby, will expand the safety features.

1.5 Outline

The bottom line of the above discussion is that alternative, low-cost test techniques need to be developed that can effectively replace the standard, costly specification-based tests currently applied in high-volume manufacturing. These techniques should target reducing test times and/or alleviating the need to rely on specialized ATE. They could be generic, that is, virtually applicable to any circuit class, or circuit-specific exploiting the inherent properties of the circuit under test.

Introducing alternative test techniques, however, should not sacrifice the high accuracy of specification-based testing, which is measured by test metrics such as test escape (e.g. faulty circuits passing the test) and yield loss (e.g. functional circuits failing the test). Therefore, any alternative test technique should be assessed by estimating the resultant test metrics.

Test techniques are also required for monitoring the health of the system in the field either concurrently with the normal operation or in idle times. In this case, the test techniques need to be necessarily fully integrated without relying on external test equipment. Clearly the challenges here are more severe since any built-in test circuitry should be (a) low-overhead, (b) robust in the sense that it should have a negligible failure probability considerably compared to the failure probability of the system itself, and (c) non-intrusive in the sense that it should not degrade the performances achieved by the design.

Finally, test techniques are required to guide appropriately the diagnosis and failure analysis. Integrated test techniques can offer better insights on failure modes and pinpoint the failures with more rigor. In this case, test techniques need to be accompanied with dedicated post-processing software to be able to diagnose failures down to transistor-level while having access to only few primary inputs and outputs and the outputs of the integrated test circuitry.

In Chapter 2, we focus on a generic alternative test paradigm based on ideas borrowed from the field of machine learning. In particular, we view the problem from a pattern recognition point of view, where machine learning is used to infer with confidence the outcome of specification-based testing from low-cost measurements or to mine correlations amongst specification-based tests and identify redundant specifications so as to apply more compact specification-based test suites.

In Chapter 3, we focus on integrated test techniques for various classes of analog circuits. In particular, we present generic, non-intrusive, built-in test and calibration techniques for RF circuits, a built-in self-test technique for $\Sigma\Delta$ analog-to-digital converters, a design-for-test technique for pipeline analog-to-digital converters, and a generic neuromorphic built-in self-test architecture.

In Chapter 4, we present test metrics evaluation techniques aiming at assessing alternative test solutions early during the design and test development phases. In particular, we will cover test metrics evaluation techniques based on density estimation and generation of extreme circuit instances. We will also discuss the application of extreme value theory for quantifying test metrics with parts-per-million precision.

In Chapter 5, we present an analog fault diagnosis and failure analysis flow that offers a unified approach regardless the type of fault that has occurred. The flow is based on a defect filter to decide on the type of the fault and offers two possible tiers for diagnosing the location of a defect and off-target process parameters.

The proposed methodologies in all Chapters will be supported with simulation and experimental results.

Finally, in Chapter 6, we present directions for future work.

Chapter 2

Machine learning-based test techniques

2.1 Introduction

The standard approach for testing analog circuits is to measure directly the performances that are promised in the data sheet. The circuit is declared faulty or functional by simply comparing the measured performance values to the design specifications. In this context, the necessary automatic test equipment (ATE) resources are employed and overall the test approach is easy to interpret and implement since the same test benches are used as during the design and prototype characterization phases.

Machine learning-based test aims to circumvent specialized ATE resources and speed up the test execution time by relying solely on measurements that can be rapidly extracted using a low-cost assortment of test equipment. The grounds for achieving the objective of inferring the performances implicitly from low-cost alternative measurements is that both the performances and the alternative measurements are subject to the same process variations [7–9]. Thus, in the presence of process variations, both performances and alternative measurements vary and the objective boils down to identifying alternative measurements that correlate well with the performances, such that any performance shift can be predicted from the corresponding shift in the alternative measurement pattern, as illustrated in Fig. 2.1. For the method to succeed, it is needed first to (a) identify such information-rich alternative measurements and second to (b) build the mapping between alternative measurements and performances.

The identification of appropriate alternative measurements is a circuit-specific problem since the input, output, frequency band, transfer function, etc., depend on the type of the circuit, as well as on its architecture. In the recent years, the machine learning-based test paradigm has been proven for different types of circuits, including, baseband analog [7, 10], RF [11–16], data converters [17, 18], and PLLs [19]. Very often, the alternative measurements are extracted *ad hoc* without a clear rationale. Through simulations it is demonstrated that they can be used indeed to predict the performance values and in the next step the concept is demonstrated experimentally in silicon. The reason is the large number of process parameters and their intricate interactions which makes impossible to justify that an alternative measurement captures all variation scenarios that can occur in practice. A typical approach is to identify as many alternative measurements as possible and then compact this set using feature selection algorithms [7, 20–24], such as genetic algorithms [25], floating search algorithms [26], etc. Another approach is to craft the test stimulus such that the output response becomes appropriate for machine learning-based test [7, 27].

Examples of alternative measurements for baseband analog circuits include sampling the output response when applying at the input a piecewise linear test stimulus [7, 10], a multi-tone sinusoidal [20], or a pseudo-random bit sequence [21, 28]. Popular approaches to extract alternative

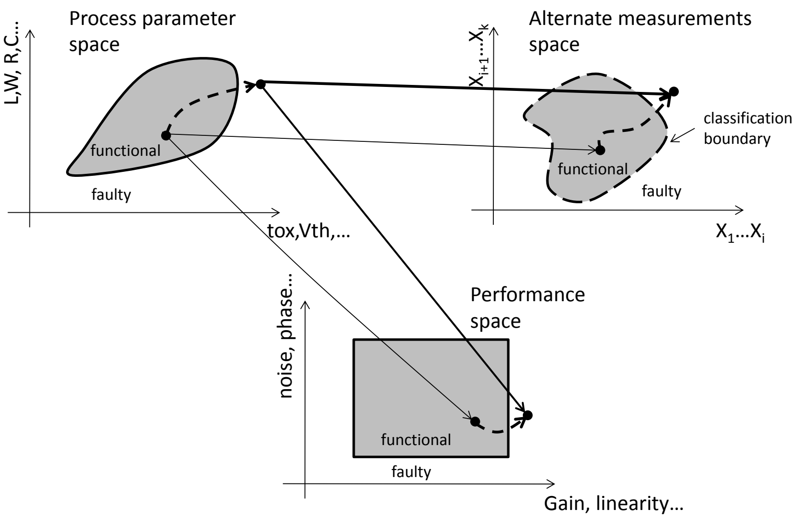


Figure 2.1: Principle of machine learning-based test.

measurements from RF circuits include (a) applying a baseband multi-tone sinusoidal, up-converting it using a mixer that exists on the test load board or on-chip, down-converting the RF output using again a mixer, and sampling the demodulated baseband test response [11, 12, 21]; (b) sensors that tap into the RF signal path, for example, amplitude detectors [29–35] and current sensors [34,36,37].

The intricate relationship among performances and alternative measurements makes impossible to build a mapping in the form of a closed-form mathematical equation. For this reason, the mapping is built through statistical learning. In particular, a set of n circuit instances that is representative of the fabrication process is collected. The d performances $\mathbf{P} = [P_1, \cdots, P_d]$ and alternative measurements $\mathbf{X}$ are obtained on each circuit instance. Part of the circuit instances are used as a training set to learn a regression function $f_i : \mathbf{X} \rightarrow P_i$ for each performance P_i. The circuit instances that are left out are used as an independent validation set. Target performances for the circuit instances in the validation set are assumed to be unknown and they are only used to estimate the test error. In particular, the alternative measurements are given as arguments to the regression functions to obtain performance predictions $\hat{\mathbf{P}} = [\hat{P}_1, \cdots, \hat{P}_d]$. If the test error $P_i - \hat{P}_i$, averaged over all circuit instances in the validation set, is deemed to be small for all performances, then the alternative measurements are satisfactory. This approach is largely known as *alternate test*.

It should be noticed that outliers should be excluded from the training phase since they are inconsistent with the statistical nature of the bulk of the training data stemming from circuits with process variations and will adversely affect the regression fit results. In fact, outliers are non-statistical in nature since their real cause is physical defects that are induced or enhanced during the manufacturing in a random fashion. Likewise, the learned regression functions are not designed to predict the performances of outliers as the test outcome will be somewhat random. Thus, in the testing phase, all circuits should be checked to verify that they are not outliers before the learned regression functions are applied to reach a test decision. This indispensable step in the flow of alternate test makes use of a defect filter [38].

Instead of predicting the actual values of the performances, it is also possible to predict directly whether the performances satisfy their specifications, that is, a form of go/no-go test. In this case, a classifier is used that implements a function $g : \mathbf{X} \rightarrow [pass, fail]$ [20, 21, 39–42]. The classifier should be able to allocate a non-linear decision boundary in the space of alternative measurements such that the population of functional circuits is separated from the population of circuits that violate at least one specification, as illustrated in Fig. 2.1. Various classifiers can be used in this context, including Support Vector Machines (SVM) [43], decision trees [44], ontogenic neural networks [45], feed-forward neural networks [46], etc. Similarly to the regression functions, the better the correlation among performances and alternative measurements is, the smaller will be the overlap between the two populations and the better the classification rate will be.

The advantage of using regression functions is that it offers the possibility of predicting the performance values, which allows binning of functional circuits and gives a better insight into the performance distributions. The classifier has the advantage that it can screen out circuits with defects on top of circuits with excessive process variations. However, this is at the expense of requiring to include circuits with defects in the training set which may be difficult to collect in the production environment in a short period of time [47].

Finally, as any other indirect test method, machine learning-based test is prone to error. To improve confidence in the test decision, it is possible to identify the small fraction of circuits that will be likely erroneously predicted and forward them to a second test tier where more thorough testing is performed. Several techniques exist for this purpose, including the use of guard-bands in the case of classification-oriented approach [21] and the use of multiple regression functions [48] in the case of alternate test.

2.2 Adaptive machine learning-based test

The regression functions cannot give an accurate prediction for circuits that have alternative measurement patterns that fall outside the domain defined by the training set of circuits. Such circuits typically exhibit excessive process variations or contain gross defects. Inevitably, the regression functions are randomly curved (e.g. extrapolated) outside the domain defined by the training set, resulting in a random representation of the underlying correlations. On the other hand, the classification approach, as explained above, requires to include circuits with gross defects in the training set, which are unlikely to be available at the onset of production. In general, it is rather difficult to collect in reasonable time a representative training set that accounts for the actual statistics, covers all process corners, and includes information about occurring defects.

For this reason, machine learning-based test entail a risk and needs to be adapted so as to increase the confidence in the test decisions. The adaptation results in a decision-tree test flow dictated by the observed response of the circuit under test (CUT) and by historical test data. In general, adaptive test concerns the adjustment of the test program on a CUT-by-CUT basis which in the extreme could result in each CUT being uniquely tested. Adaptive test ideas include skipping specification tests that have a high pass probability [49–51], moving test limits to improve outlier detection [52], periodical re-learning of machine learning-based tests [53], and real-time test ordering [54].

2.2.1 Adaptive test flow based on a pair of programmable defect filters

Fig. 2.2 illustrates the flow of the proposed adaptive test scheme [55]. The first step is to obtain the alternate measurements on the CUT. Based on these alternate measurements, a defect filter decides whether the CUT is represented adequately by the training data which have been previously used to learn the regression functions. In this case the regression functions are well-founded to predict the performances of the CUT. On the contrary, the defect filter screens out a suspicious CUT on the grounds that the predictions will entail a risk. This particular defect filter is “strict”, in the sense that it favors the screening of devices such that the devices that are let through are guaranteed to be correctly predicted.

Subsequently, the suspicious CUT goes through a second defect filter that decides whether the CUT contains a defect that leads to a complete malfunction. In this case, the CUT is labeled as faulty and is summarily discarded. This second defect filter is “lenient” to ensure that only CUT with gross defects are screened out. In the opposite scenario where the CUT is considered

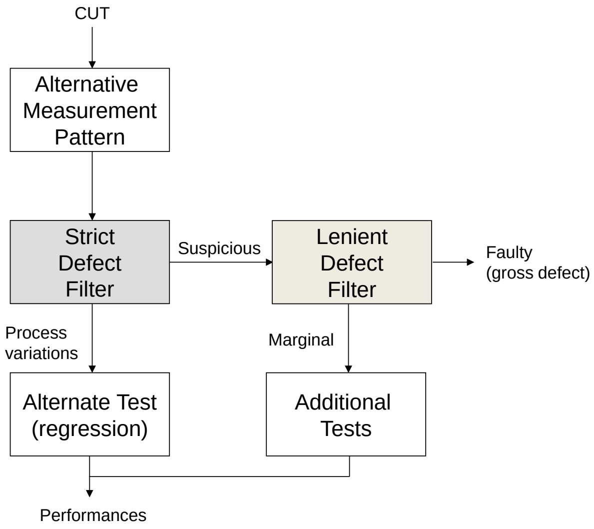


Figure 2.2: Adaptive machine learning-based test flow.

to be marginal, that is, it is considered to contain a mild defect that brings it marginally-in or marginally-out the specifications, the CUT is forwarded to a second test tier where it undergoes more comprehensive testing. In this step, we can choose to apply the specification-based tests or special structural tests that target specific defects.

The proposed scheme acknowledges that the majority of the devices that fall in the main lobe of the distribution space do not require extensive testing and their performances can be easily predicted through low-cost alternate testing. The objective of the "strict" defect filter is to identify the small fraction of marginal devices for which we need to devote more test time and resources so as to support test quality in terms of reducing test escapes. The "lenient" defect filter identifies quickly devices with gross defects for which there is no need to waste resources to carry out further testing. Therefore, the defect filters condition the test flow with respect to the behavior of each individual CUT as this is depicted in the set of alternative measurements.

2.2.2 Programmable defect filter

The defect filter relies on the joint probability density function of the alternative measurements, denoted by $f(\mathbf{X})$. The form of $f(\mathbf{X})$ is unknown, thus we will estimate $f(\mathbf{X})$ using the training set, in particular using the d-dimensional alternative measurement patterns of the n circuits in the training set, denoted by $\mathbf{X}^1, \cdots, \mathbf{X}^n$. The estimate, denoted by $\hat{f}_{\mathbf{X}}$, is derived using a non-parametric kernel density estimator defined by [56]

$$\hat{f}_{\mathbf{X}}(\mathbf{x}, \alpha) = \frac{1}{n} \sum_{j=1}^{n} \frac{1}{(\lambda_j(\alpha) \cdot h)^d} K_e \left(\frac{\mathbf{x} - \mathbf{X}^j}{\lambda_j(\alpha) \cdot h} \right), \tag{2.1}$$

where

$$h = \left\{ 8 c_d^{-1} (d+4) (2\sqrt{\pi})^d \right\}^{1/(d+4)} n^{-1/(d+4)} \tag{2.2}$$

is a smoothing parameter called bandwidth,

$$c_d = 2\pi^{d/2} / (d \cdot \Gamma(d/2)) \tag{2.3}$$

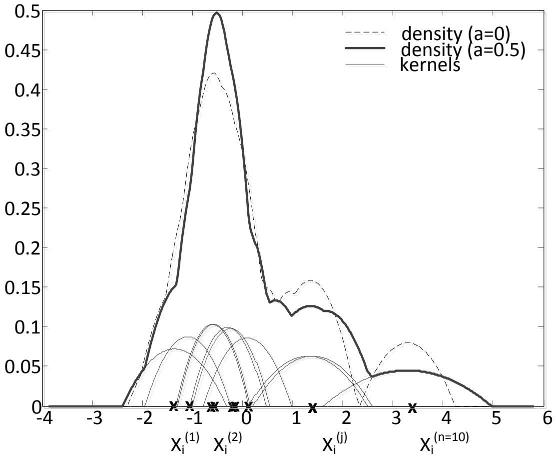


Figure 2.3: Non-parametric kernel density estimation.

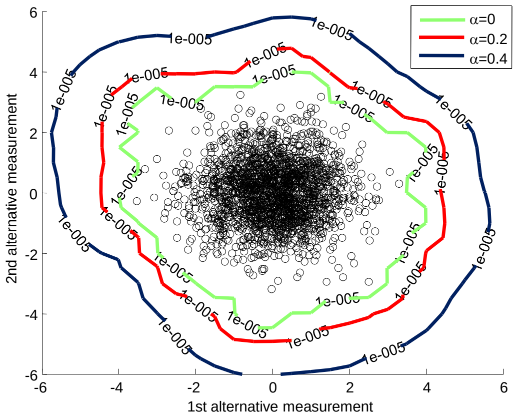


Figure 2.4: Defect filters in a 2-dimensional alternate measurement space. The black circles correspond to 2000 devices with process variations which are used to construct the defect filters.

is the volume of the unit d-dimensional sphere,

$$K_e(\mathbf{t}) = \begin{cases} \frac{1}{2} c_d^{-1} (d+2) \left(1 - \mathbf{t}^T \mathbf{t}\right) & \text{if } \mathbf{t}^T \mathbf{t} < 1 \\ 0 & \text{otherwise} \end{cases} \tag{2.4}$$

is the Epanechnikov kernel, λ_j are local bandwidth factors defined by

$$\lambda_j(\alpha) = \left\{ \hat{f}_{\mathbf{X}}(\mathbf{X}^j, 0)/g \right\}^{-\alpha}, \tag{2.5}$$

and g is the geometric mean

$$\log g = n^{-1} \sum_{j=1}^{n} \log \hat{f}_{\mathbf{X}}(\mathbf{X}^j, 0). \tag{2.6}$$

The density estimate in (2.1) is a weighted sum of kernels centered on the n observations, as shown with the one-dimensional example of Fig. 2.3. The bandwidth h defines the half-width of the kernels. The parameter $\lambda_j(\alpha)$ multiplies the bandwidth of the kernel of the j-th observation. The default value of α is $\alpha = 0$, resulting in $\lambda_j(0) = 1$ for all n observations. By increasing α, the tails of the density estimate become smoother and longer, but less heavier [56].

Noticing that the density estimate vanishes at some point, we can choose naturally to filter a CUT if its alternate measurement pattern $\mathbf{X}$ satisfies

$$\hat{f}_{\mathbf{X}}(\mathbf{X}, \alpha) = 0, \tag{2.7}$$

The solutions to the above equation compose the frontier of the defect filter. The parameter α controls the extent of the filtering. The larger α is, the more “lenient” the defect filter is. This is depicted in two dimensions in Fig. 2.4, where the frontiers of three progressively “lenient” defect filters are displayed with contours of low density.

The proposed defect filter has the following appealing properties: (a) It is nonparametric, in the sense that it does not make any assumption regarding the parametric form of the joint probability

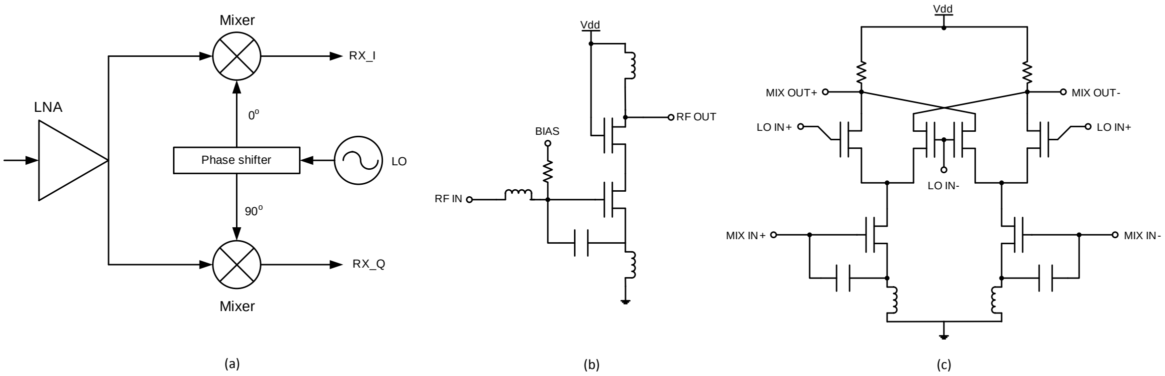


Figure 2.5: (a)Block digram of RF receiver and its sub-circuits: (b) LNA and (c) mixer.

density function of alternative measurements. Instead, the kernel density estimator allows the training data to speak for themselves and, thus, it can handle any alternative measurements; (b) It is an one-class classifier and its construction does not require data from defective devices. This is particularly important in order to start using the adaptive test scheme at the onset of production; (c) It is very flexible since it is parameterized with a single parameter α; (d) It can be easily re-learned periodically incorporating the newest statistical information that is available.

2.2.3 Results

Our test vehicle is an RF receiver front-end, shown in Fig. 2.5. We consider the Error Vector Magnitude (EVM) alternate test originally proposed in [13] which consists of applying a sequence of 3 two-tone stimuli that span the entire channel-bandwidth of the receiver. The test response is obtained by applying a Fast Fourier Transform (FFT) on the signals that are recorded by sampling the I and Q channels at 480kHz. The alternative measurement pattern comprises the amplitude and phase of the fundamentals in each channel. The standard EVM test consists of applying a QPSK modulated test signal with a 25kHz symbol rate and sampling the I and Q channels at 100kHz. The EVM specification is set to 5.33%. The cost per unit time of the EVM machine learning-based test is much lower in comparison to the standard test since it eliminates the need for high performance RF sources with digital modulation capability [13]. It only requires a less demanding two-tone RF signal source and a RF coupler. Test time is also reduced since the alternative test data are captured at a higher speed than the baseband signal samples which comprise the test frame of symbols in the standard EVM test.

The “strict” filter is adjusted such that the circuits that are forwarded to the alternate test are accurately predicted and at the same the smallest possible percentage of circuits with process variations (PV) are being retested since those circuits are expected to be functional. As shown in Fig. 2.6, setting $\alpha_{\text{strict}} = 0.2$ results in an excellent correlation for the alternate test (e.g. $R = 0.993$) and none of the circuits with PV are being re-tested. The “lenient” filter is adjusted such that the smallest possible percentage of circuits with excessive process variations (EPV) fail directly since those circuits most likely will be functional. As shown in Fig. 2.6, setting $\alpha_{\text{lenient}} = 0.8$ results in only 3.11% of circuits with EPV failing directly while 20.78% of circuits with the EPV will lie in between the two filters and will be re-tested. The rest of the circuits with EPV are forwarded to the alternate test and their performances are accurately predicted. Regarding the circuits that contain gross defects (GD), with the previous adjustment of the “strict” and “lenient” filters, as shown in Fig. 2.6, 86.11% fail directly while only 5.28% are being re-tested. The rest of the gross defects have no effect on the operation of the circuit.

Finally, the scatter plot of Fig. 2.7(b) demonstrates what will happen in the hypothetical

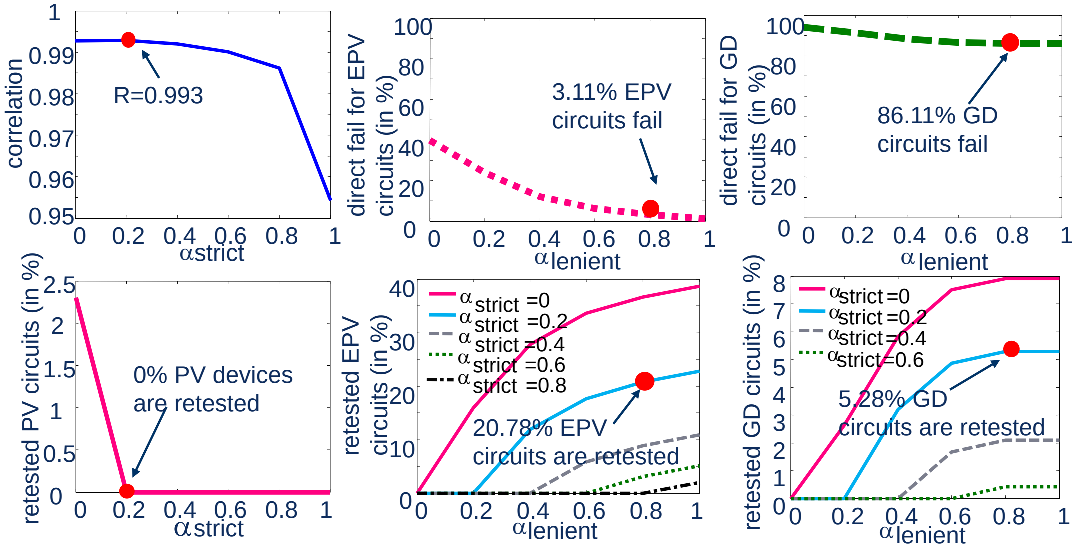


Figure 2.6: Positioning of defect filters to obtain optimal trade-offs.

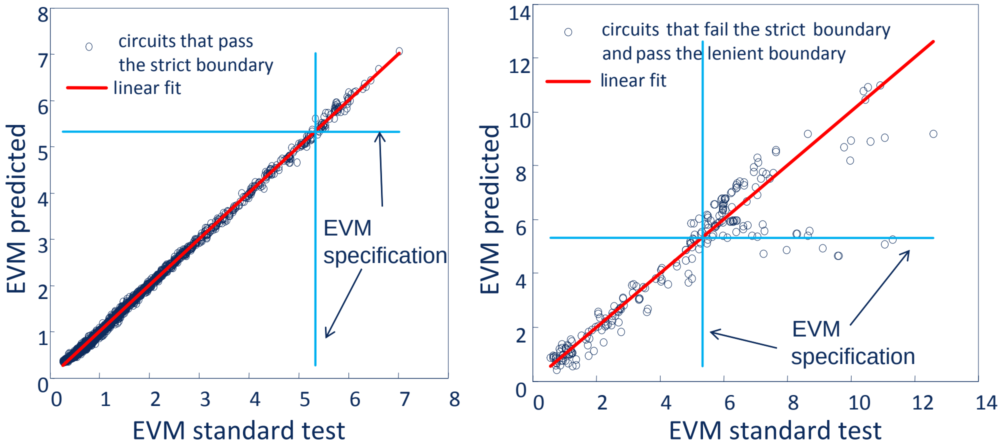


Figure 2.7: Predicted EVM values versus true EVM values using the regression test: (a) circuits that pass the "strict" defect filter and (b) hypothetical scenario where the regression test is used for the circuits that are selected to be retested.

scenario where the circuits that we have chosen to retest were accidentally sent to the regression test. It can be seen that the footprints of these circuits do not lie on the diagonal line as is the case for the circuits that pass the "strict" filter in Fig. 2.7(a). The predictions of some circuits are very inaccurate to the point where they result in test escapes and yield loss.

2.3 Learning based on limited datasets

To learn regression models that are valid across the circuit distribution right at the onset of production, without needing to hold off to collect a representative training set before we can fully trust the alternate test decisions, we can employ the Bayesian model fusion (BMF) technique [57–60]. The underlying idea is to learn the regression functions by employing in addition to the real data prior information from post-layout simulation [61].

2.3.1 Bayesian Model Fusion

We assume without loss of generality a single performance P. Our objective is to learn the regression function $f : \boldsymbol{X} \rightarrow P$. Let us assume that we have at hand data from n real circuits. We define the vectors $\boldsymbol{P}_L = [P^1, \cdots, P^n]$ and $\boldsymbol{X}_L = [\boldsymbol{X}^1, \cdots, \boldsymbol{X}^n]$, where P^j and $\boldsymbol{X}^j$ denote the performance and alternative measurement pattern, respectively, for the j-th circuit, $j = 1, \cdots, n$.

The conventional learning procedure is to use a fraction of the real data for training and the rest of the real data for validating the generalization ability on previously unseen circuits. However, in a practical scenario this real data set contains very limited information about the process corners and the regression function will be valid mainly around the nominal point. The aim of the BMF technique is to learn the regression function by leveraging information about the process corners from a large volume of post-layout simulation data that is readily available and combining this information with the real data. We refer to the post-layout simulation data as *early-stage* data and to the real data as *late-stage* data.

Formally, we consider two versions of the regression function f, namely an early-stage regression function, denoted by f_E, that is trained using only early-stage data and a late-stage regression function, denoted by f_L, that is trained using the BMF learning procedure. We use the following general regression forms

$$f_E(\boldsymbol{x}) = \sum_{m=1}^{M} a_{E,m} \cdot b_m(\boldsymbol{x}) \tag{2.8}$$

$$f_L(\boldsymbol{x}) = \sum_{m=1}^{M} a_{L,m} \cdot b_m(\boldsymbol{x}), \tag{2.9}$$

where $b_m(\boldsymbol{x})$ is the m-th basis function and $a_{E,m}$, $a_{L,m}$ correspond to the m-th coefficient of the early-stage and late-stage regression function, respectively, $m = 1, \cdots, M$.

The BMF learning procedure consists of solving for the late-stage model coefficients that maximize the *posterior* distribution $\mathrm{pdf}(\boldsymbol{a}_L|\boldsymbol{P}_L, \boldsymbol{X}_L)$, that is,

$$\max_{\boldsymbol{a}_L} \mathrm{pdf}(\boldsymbol{a}_L|\boldsymbol{P}_L, \boldsymbol{X}_L), \tag{2.10}$$

where $\boldsymbol{a}_L = [a_{L,1}, \cdots, a_{L,M}]$. By applying Bayes' theorem, we can write

$$\mathrm{pdf}(\boldsymbol{a}_L|\boldsymbol{P}_L, \boldsymbol{X}_L) \propto \mathrm{pdf}(\boldsymbol{a}_L) \cdot \mathrm{pdf}(\boldsymbol{P}_L, \boldsymbol{X}_L|\boldsymbol{a}_L). \tag{2.11}$$

Thus, the problem boils down to

$$\max_{\boldsymbol{a}_L} \mathrm{pdf}(\boldsymbol{a}_L) \cdot \mathrm{pdf}(\boldsymbol{P}_L, \boldsymbol{X}_L|\boldsymbol{a}_L). \tag{2.12}$$

Assuming that the late-stage model coefficients are independent, we can write

$$\mathrm{pdf}(\boldsymbol{a}_L) = \prod_{m=1}^{M} \mathrm{pdf}(a_{L,m}). \tag{2.13}$$

We define the *prior* distribution $\mathrm{pdf}(a_{L,m})$ by involving the prior knowledge from the early-stage data. Specifically, $\mathrm{pdf}(a_{L,m})$ is assumed to follow a Gaussian distribution with mean $a_{E,m}$ and standard deviation $\lambda|a_{E,m}|$

$$\mathrm{pdf}(a_{L,m}) = \frac{1}{\sqrt{2\pi}\lambda|a_{E,m}|} \cdot \exp\left[-\frac{(a_{L,m} - a_{E,m})^2}{2\lambda^2 a_{E,m}^2}\right]. \tag{2.14}$$

This approach accounts for the fact that $a_{L,m}$ is expected to be similar to $a_{E,m}$ and deviate from $a_{E,m}$ according to the absolute magnitude of $a_{E,m}$.

The *likelihood function* $\mathrm{pdf}(\boldsymbol{P}_L, \boldsymbol{X}_L|\boldsymbol{a}_L)$ is expressed in terms of the real data. Specifically, since the real data are obtained independently, we can write

$$\mathrm{pdf}\left(\boldsymbol{P}_L, \boldsymbol{X}_L|\boldsymbol{a}_L\right) = \prod_{j=1}^{n} \mathrm{pdf}\left(P^j, \boldsymbol{X}^j|\boldsymbol{a}_L\right). \tag{2.15}$$

Furthermore,

$$\mathrm{pdf}\left(P^j, \boldsymbol{X}^j|\boldsymbol{a}_L\right) = \mathrm{pdf}(\varepsilon^j), \tag{2.16}$$

where ε^j is the prediction error introduced by the late-stage regression for the j-th real circuit

$$\varepsilon^j = P^j - f_L(\boldsymbol{X}^j). \tag{2.17}$$

This error is a random variable that is assumed to follow a zero-mean Gaussian distribution with some standard deviation σ_0

$$\mathrm{pdf}(\varepsilon^j) = \frac{1}{\sqrt{2\pi}\sigma_0} \cdot \exp\left(-\frac{\left(\varepsilon^j\right)^2}{2\sigma_0^2}\right). \tag{2.18}$$

Therefore, combining (2.16), (2.17), (2.18), and (2.9), we can write

$$\mathrm{pdf}\left(P^j, \boldsymbol{X}^j|\boldsymbol{a}_L\right) = \frac{1}{\sqrt{2\pi}\sigma_0} \cdot \exp\left\{-\frac{1}{2\sigma_0^2} \cdot \left[P^j - \sum_{m=1}^{M} a_{L,m} \cdot b_m\left(\boldsymbol{X}^j\right)\right]^2\right\}. \tag{2.19}$$

By combining (2.13), (2.14), (2.15), and (2.19) and taking the natural logarithm, the maximization problem in (2.12) becomes

$$\max_{\boldsymbol{a}_L} -\left(\frac{\sigma_0}{\lambda}\right)^2 \sum_{m=1}^{M} \frac{\left(a_{L,m} - a_{E,m}\right)^2}{a_{E,m}^2} - \sum_{j=1}^{n}\left[P^j - \sum_{m=1}^{M} a_{B,m} \cdot b_m\left(\boldsymbol{X}^j\right)\right]^2. \tag{2.20}$$

The optimal values of σ_0 and λ are determined by k-fold cross-validation [62].

2.3.2 Results

Our test vehicle is a 2.4 GHz inductively degenerated cascode RF LNA. We consider the machine learning-based approach based on non-intrusive variation-aware sensors proposed in [63], which is described in details in Section 3.2. The RF LNA and the non-intrusive sensors are designed using the 0.25 μm Qubic4+ BiCMOS technology by NXP Semiconductors. The late-stage data come from 140 chips that were fabricated in a Multi-Project-Wafer (MPW) run. The late-stage data are

Table 2.1: Machine learning-based test learning procedures

learning method	training set	validation set
BMF	"intelligent" mixture of early-stage simulation data and late-stage real inliers	late-stage real outliers
standard	late-stage real inliers	
straightforward combination	"raw" mixture of early-stage simulation data and late-stage real inliers	
simulation-based	early-stage simulation data	

divided into inliers which are the most centered circuits and outliers which are the most distant circuits from the sample mean in an Euclidian sense. The early-stage data are generated through a Monte Carlo post-layout simulation with 1000 runs which takes into account the complete signal path, including the circuit, pins, package, test board, etc.

We consider the four learning procedures listed in Table 2.1. The results are shown in Fig. 2.8 where we report the average prediction error and maximum error on the validation set. As it can be seen, for any performance and any accuracy metric and regardless the number of the late-stage real inlier circuits used for training, the BMF learning procedure either performs better than the other three conventional learning procedures or, at worst, it is equivalent to one of them in statistical terms. In particular, the simulation-based learning procedure shows consistently the worst performance. The performance of the standard learning procedure deteriorates monotonically as the size of the training set becomes smaller. This is expected since the information available for training is weakened and our ability to extrapolate the regression towards the tails of the distribution deteriorates, resulting in large prediction error on the validation set. The straightforward combination learning procedure performs better than the standard and simulation-based learning procedures. However, it is observed to be less effective than the BMF learning procedure. This is explained by the fact that the straightforward combination learning procedure combines simulation and real data with equal weight, while the BMF learning procedure appropriately assigns the optimal weight through cross-validation. The improvement that the BMF learning procedure offers as compared to the straightforward combination learning procedure is significant if we project it to parts-per-million. It should also be noticed that the BMF learning procedure shows a remarkably stable behaviour, maintaining nearly constant accuracy metrics even when the number of the late-stage real inliers used for training is small. This implies that the BMF learning procedure, by statistically extracting prior knowledge from simulation data, is capable of generating accurate regression functions across the design space based only on few real circuits. Thus, the BMF learning procedure can be used to start deploying the alternate test right at the onset of production, without needing to wait to collect beforehand a large volume of data, as is the standard practice today.

2.4 Specification test compaction

Specification-based testing still remains the only acceptable industrial practice for analog circuits. In this approach, the performances of the circuit are measured one by one and are verified against the specification limits. Yet the high cost of ATE and the lengthy test times involved have resulted in intensified efforts and interest in reducing the number and types of specification-based tests that

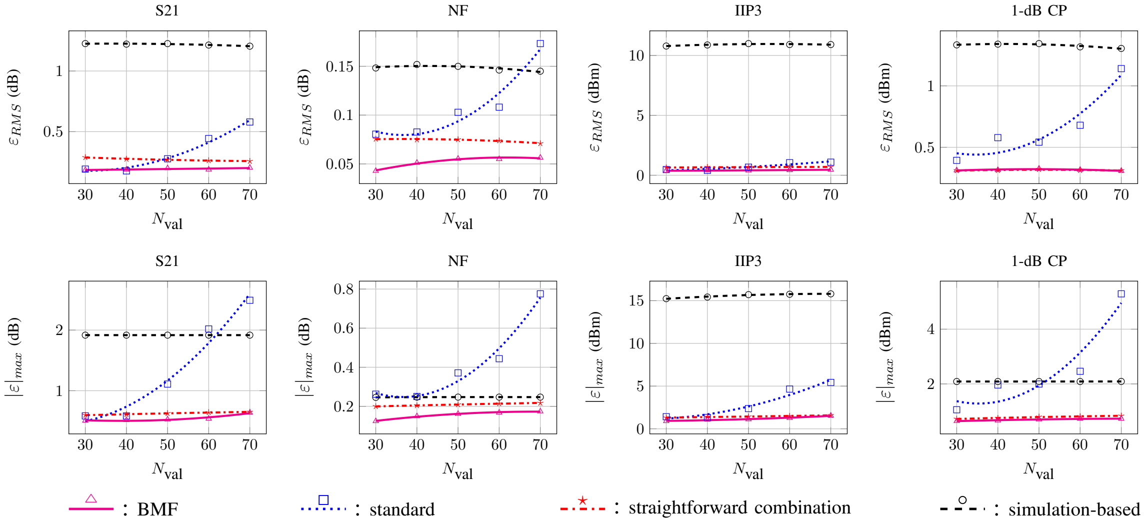


Figure 2.8: Machine learning-based test accuracy metrics for various performances and model construction cases.

are performed during production testing.

A plausible direction towards decreasing cost, akin to test compaction practices in digital circuits, is to identify and eliminate information redundancy in the set of tests, thereby relying only on a subset of them in order to reach a pass/fail decision [64–72]. Such redundancy is likely to exist since groups of performances refer to the same portion of the device and are subject to similar process imperfections. However, it is highly unlikely that it will manifest itself in a coarse and easily observable form of superfluous tests that can be summarily discarded. Hence, more advanced statistical analysis methods are likely to be required.

2.4.1 Machine learning-based test compaction

We view the problem of specification-based test compaction as a binary pass/fail classification problem [73, 74]. This approach entails two components, namely a feature selection algorithm for searching in the power-set of specification-based tests and a prediction model for predicting based solely on a select subset the outcome of the remaining specification-based tests that are excluded from this subset, as shown in Fig. 2.9. The search progresses towards a low-cost, low-dimensional specification-based test subset based on which the classifier predicts correctly the pass/fail outcome of the complete specification-based test suite.

Formally, let $S = [s_1, ..., s_d]$ denote the set of specification-based tests. A set of N circuits is subjected to S. For each circuit, we record s_k, $k = 1, ..., d$, and the resulting ground truth pass/fail label. We split the set of N circuits in a training and validation set.

A genetic algorithm is used to search in the power-set of the 2^d subsets of S [25, 75]. Each visited subset $S^{'} \subseteq S$ is assigned a fitness value based on two criteria: (a) the associated cost, denoted by $C(S^{'})$, and (b) the incurred test error, denoted by $\epsilon_r(S^{'})$, if new circuits coming out of production are subjected only to $S^{'}$. Pass/fail assignments based solely on $S^{'}$ are done as follows. Circuits that fail one or more tests in $S^{'}$ are discarded outright. Circuits that pass all tests in $S^{'}$ are presented to a classifier that establishes a binary mapping of the form $g : S^{'} \rightarrow [pass, fail]$. This prediction model is learned in a training phase which employs the circuits in the training set. The error $\epsilon_r(S^{'})$ is defined as the percentage of circuits in the validation set that pass all tests in $S^{'}$, but are misclassified by the mapping g.

The genetic algorithm explores the trade-off $\epsilon_r - C$ with the aim to converge to the Pareto frontier. Formally, the Pareto frontier is the set of subsets of S that are not strictly dominated by

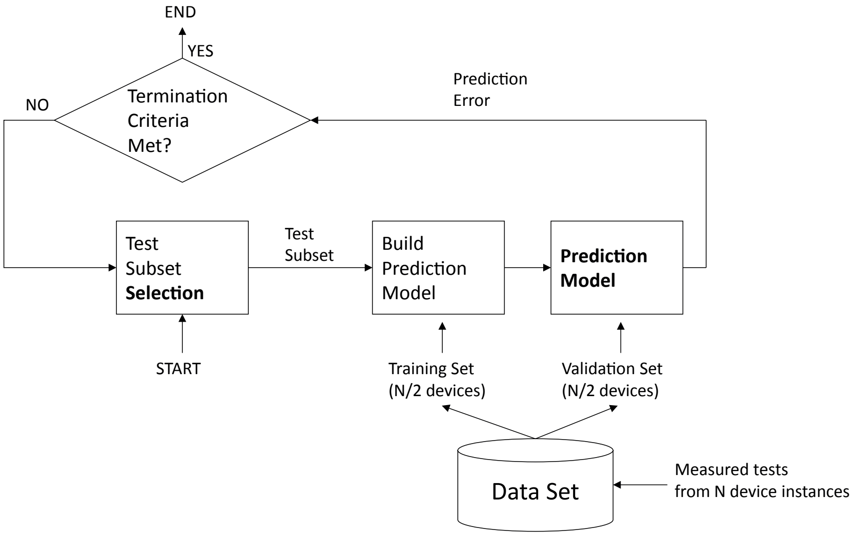


Figure 2.9: Feature selection algorithm for specification-based test compaction.

another subset of S. A subset S^i with fitness criteria $\left(\epsilon_r^i, C^i\right)$ strictly dominates a subset S^j with fitness criteria $\left(\epsilon_r^j, C^j\right)$ if (a) $\epsilon_r^i \leq \epsilon_r^j$ and $C^i < C^j$ or (b) $C^i \leq C^j$ and $\epsilon_r^i < \epsilon_r^j$. The search evolves until an objective for the fitness criteria is met or until a large number of iterations is completed, implying that further optimization of the fitness criteria is not possible.

2.4.2 Cost model

We consider the general case where a specification-based test set comprises tests that require different test instrumentation and execution times. We group the specification tests in S according to their type into M test groups. If we denote by n_i the number of tests in test group i, then $d = n_1 + ... + n_M$ is the number of specification tests. Let T and C be the baseline test time and test cost per second, respectively, when all d specification tests are considered. Then,

$$\begin{aligned} C\left(S\right) &= \sum_{i=1}^{M} \left(c_i C\right)\left(t_i T\right) \\ &= CT \sum_{i=1}^{M} c_i t_i \end{aligned} \tag{2.21}$$

where, t_i is the relative test time contribution of test group i with respect to T and c_i is the relative test cost per second of test group i with respect to C. Let now $x_{ik} = 1$ if test k in the test group i is present, and $x_{ik} = 0$ otherwise. Let also t_{ik} denote the test time of test k in the test group i. The test cost of a subset $S^{'}$ is given by

$$C(S^{'}) = \sum_{i=1}^{M} \left(c_i \left(1 - \overline{x_{i1}} \cdot ... \cdot \overline{x_{in_i}}\right) C \sum_{k=1}^{n_i} t_{ik} x_{ik} \right), \tag{2.22}$$

where the symbol $\cdot$ denotes the logic AND. Assuming that $t_{ik} = t_i T\left(S\right)/n_i$, (2.22) becomes

$$C(S^{'}) = CT \sum_{i=1}^{M} \left(\frac{c_i t_i}{n_i} \sum_{k=1}^{n_i} x_{ik} \right). \tag{2.23}$$

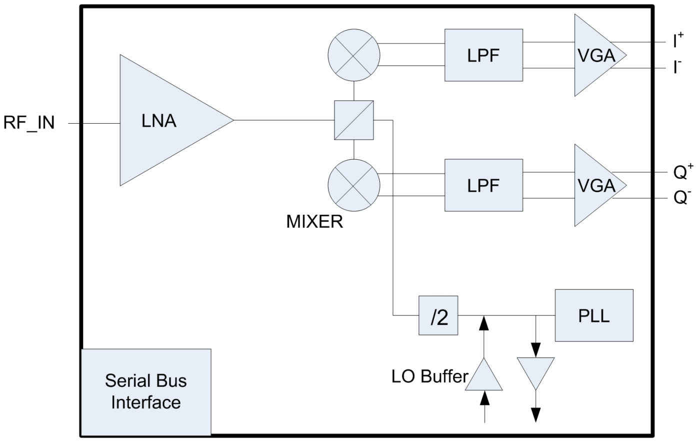


Figure 2.10: Block diagram of the RF device.

Table 2.2: Cost information.

Test Group	*Test Type*	n_i	t_i	c_i
SBI_tests	Digital	25	6.0%	40%
SBI_tests Supply_currents	DC	34	13.3%	
DacTests	Mixed Signal	6	3.3%	60%
Lock_vco		6	13.0%	
Lock_vco	RF	1	1.1%	100%
Filter_tests		20	13.3%	
Mixer_tests		43	30%	
LNA_tests		8	20%	

The normalized test cost fitness criterion of a subset $S^{'}$ is given by

$$\begin{aligned}\tilde{C}(S^{'}) &= \frac{C(S^{'})}{C(S)} \\ &= \frac{\sum_{i=1}^{M}\left(\frac{c_i t_i}{n_i}\sum_{k=1}^{n_i} x_{ik}\right)}{\sum_{i=1}^{M} c_i t_i}. \end{aligned} \tag{2.24}$$

2.4.3 Results

Our case study is a zero-IF down-converter for cell-phone applications designed in RFCMOS technology and fabricated by IBM. The block diagram is shown in Fig. 2.10. The different groups of specification-based tests, the number of tests in each group, as well as the relative test time and cost of each group are given in Table 2.2. Our data set contains the measured specification-based tests for $N = 4450$ circuits that were collected from four different lots within a period of six months. In total, 4142 circuits pass all specification tests while 308 circuits fail at least one test. The training and validation sets comprise a fixed number of $(3/4)N$ and $(1/4)N$ circuits, respectively. Notice that, on average, there will be 77 faulty circuits in a validation set.

We use a multi-objective genetic algorithm, called NSGA-II [76], to jointly optimize in one

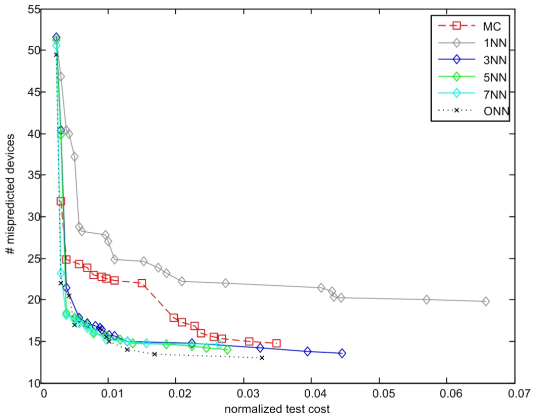


Figure 2.11: Test error vs. normalized test cost when using only non-RF specification tests.

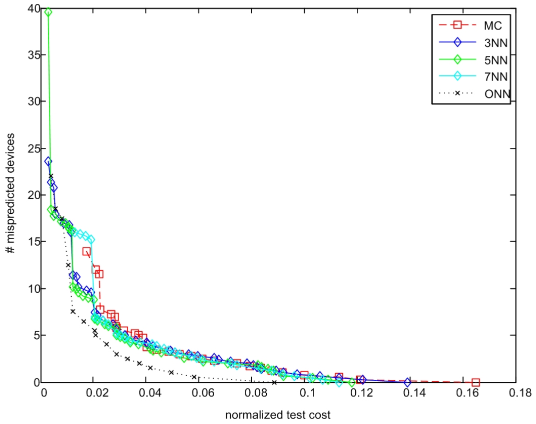


Figure 2.12: Test error vs. normalized test cost when adding RF specification tests to the best selected subsets of Fig. 2.11.

simulation run both the prediction error of the classifier and the test cost. For this purpose, NSGA-II has a diversity preserving mechanism that ensures a good spread of the Pareto frontier. We consider two types of classifiers, namely k-Nearest-Neighbors (k-NN) [46] and an Ontogenic Neural Network (ONN) [45]. As a basis for comparison, we also investigate a simple weighted maximum-cover (MC) formulation of the compaction problem. In this approach, the prediction model is trivialized, the classifier is removed from the flow and the pass or fail decision is reached by simply verifying the kept specification tests in $S^{'}$, while ignoring the rest of specification tests in $\{S - S^{'}\}$. In this scenario, for a given cost, the genetic algorithm will try to identify the subset that covers the maximum number of failing devices.

We first consider the set of specification-based tests whose execution does not require RF ATE. The results are plotted together in Fig. 2.11 where each point in the Pareto frontiers corresponds to a subset which can achieve this trade-off. As it can be seen, the ONN outperforms both k-NN and MC. Only 13 circuits are mispredicted at a small normalized cost of 0.032. Next, we examine the prediction improvement that can be obtained by adding RF specification tests to the best (in terms of minimum test error) identified subsets of non-RF specification tests. The results are plotted in Fig. 2.12. As it can be observed, the ONN again outperforms both k-NN and MC. Zero test error is achieved for a subset of normalized cost 0.09.

The main conjecture drawn from this study is that a relatively small number of only non-RF specification tests (i.e. digital, DC and low frequency) are shown to suffice for predicting correctly the pass/fail label of a very large percentage of circuits, a scenario that would eliminate the need for RF ATE. Moreover, the addition of a few RF specification tests ameliorates this small prediction inaccuracy and results in very powerful prediction models, a scenario that would still require RF ATE but would reduce the time that a circuit spends on it.

2.5 Conclusion

Machine learning-based testing has a high potential for reducing the cost of analog circuit testing. We presented an adaptive machine learning-based testing flow that on top of low-cost it also offers high confidence in test decisions. We also presented the application of BMF with the aim to start deploying machine learning-based testing right at the onset of production without having to wait to collect beforehand a representative training set. Finally, we presented a machine learning-based flow to mine redundant information in large specification-based test sets and, thus, identify a compacted specification-based test subset that can be applied without sacrificing test accuracy.

Chapter 3

Integrated test techniques

3.1 Introduction

Integrated test techniques can be grouped into Design-for-Test (DfT) and Built-In Self-Test (BIST) techniques.

DfT techniques can be broadly grouped into two approaches. The first DfT approach is to facilitate test access into the design by implementing test signal buses according to the IEEE Standards 1149.1 [77] and 1149.4 [78], as illustrated in Fig. 3.1. The IEEE 1149.4 architecture in Fig. 3.1 comprises a test bus interface circuit (TBIC) with analog test stimulus (AT1) and analog test output (AT2) pins, analog boundary modules (ABM) on each analog I/O, digital boundary modules (DBM) on each digital I/O, and a test access port (TAP) controller with test data in (TDI), test data out (TDO), test mode select (TMS), test clock (TCLK), and test reset (TRSTn) pins. This test bus architecture provides the means for bypassing functional blocks in the circuit under test (CUT), in order to apply test stimuli directly to internal blocks and reading out the test responses. Therefore, the test bus can be used to enhance the overall testability, as well as to enable system diagnostics and silicon debugging in post-manufacturing. In addition, the test bus can be used for testing for open- and short-circuits among the interconnections of circuits in a printed circuit assembly.

The second DfT approach is based on reconfiguring the CUT to enhance its testability. A first well-known example is the generic oscillation test where the CUT is reconfigured to oscillate by connecting it into a positive feedback loop. The oscillation frequency and magnitude are information-rich signatures that can be used to gain insight about the functionality of the CUT and to detect abnormal behavior [79–85]. A second example is the loop-back test for RF transceivers where the test signals are generated in the baseband and the transmitter's output is switched to the receiver's input through an attenuator to analyze the test response also in the baseband [86–92], as shown in Fig. 3.2.

BIST techniques can also be broadly grouped into two approaches. The first approach consists of embedding a signal generator and a test response analyzer into the chip [93–99], whereas the second approach consists of embedding sensors into the chip to extract off-chip information-rich, low-cost test signatures from which the status of the performances can be implicitly inferred [31, 32, 37, 63, 100], as shown in Fig. 3.3. The impetus for BIST techniques is to facilitate the use of low-performance automatic test equipment (ATE) or perhaps to eliminate any need whatsoever by adding self-test capabilities, strategic control, and observation points within the circuit.

DfT and BIST are very often *ad hoc* and largely a matter of early engagement with the design community to specify the test architecture. Great strides have been made to make DfT and BIST techniques successful for analog, mixed-signal, and RF circuits, but robust, production deployment of these techniques is not yet widespread. This is due in part to the challenge of evaluating their efficiency with respect to the standard specification-based test, which requires accurate simulation models and speeding up circuit simulation, as it will be discussed in details in Chapter 4. In addition,

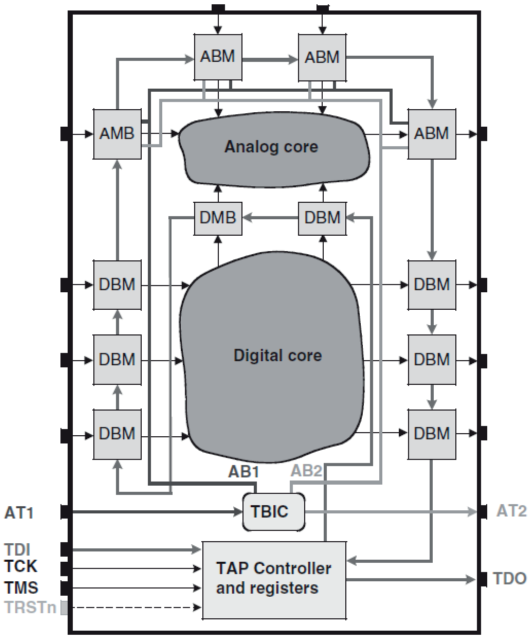


Figure 3.1: IEEE 1149.4 architecture.

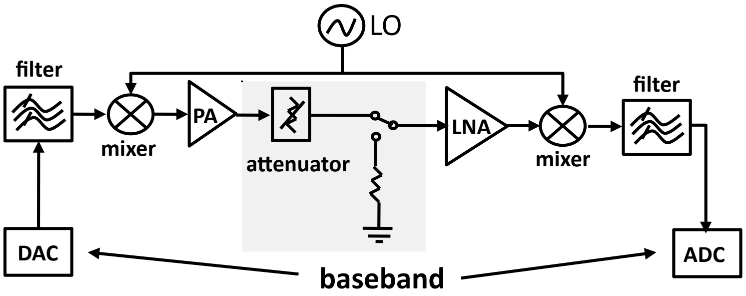


Figure 3.2: Loop-back test for RF transceivers.

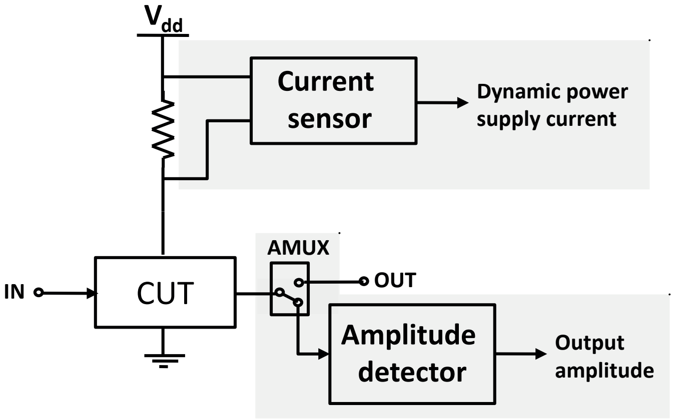


Figure 3.3: BIST employing on-chip sensors.

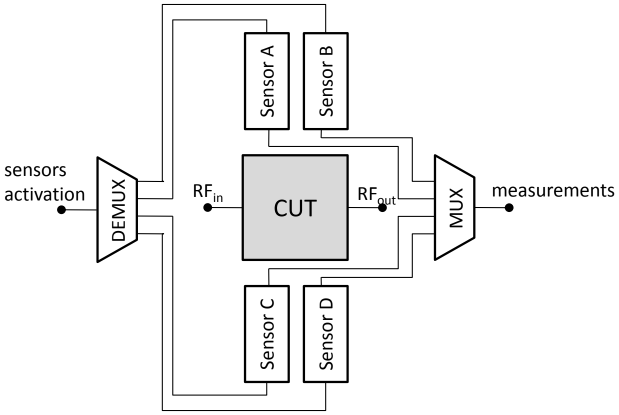


Figure 3.4: BIST based on non-intrusive sensors that are not electrically connected to the CUT.

DfT and BIST techniques should not consume a disproportionate amount of silicon die area and should neither be intrusive to sensitive circuits and design methodologies nor impede the post-silicon debugging process. Trade-offs between DfT and BIST techniques and traditional specification-based testing need to be considered and the test resources need to be intelligently partitioned between integrated and external test methods. Finally, given the rather high development time of DfT and BIST techniques, it is important to focus on their portability, such that they can be reused in different Intellectual Property (IP) blocks or cores. Despite the above challenges, the pressing demand to reduce test cost has sparked an immense effort to materialize DfT and BIST techniques since they arguably constitute very attractive alternatives. This rationale stems from the fact that much of the ATE will be on-chip or in the form of partitioned test that can be executed much faster.

DfT and BIST techniques vary depending the type of the analog, mixed-signal, and RF circuit block and very often even for a particular design style or architecture. In this Chapter we will discuss our research results specifically for RF circuits, pipeline ADCs, and $\Sigma\Delta$ ADCs, as well as a generic neuromorphic BIST architecture.

3.2 Implicit RF circuit test based on non-intrusive variation-aware sensors

Since built-in test assumes some form of monitoring of the CUT, the greatest challenge is to avoid degrading the performances of the CUT during both the test and normal modes of operation. Especially for RF circuits, this objective is hard to obtain. For example, the loop-back connection in Fig. 3.2 requires the insertion of a switch and an attenuator and, for some types of receivers, even an extra mixer is inserted in the RF signal path. Envelope detectors and current sensors in Fig. 3.3 also tap into the RF signal path. In general, adding components in the RF signal path degrades the impedance matching and adds parasitics, which inevitably shift the performances and unbalance the performance trade-offs achieved by design. To address this issue, built-in test circuitry needs to be co-designed with the CUT, which increases design iterations to meet the target design specifications, if this is at all possible. For this reason, designers are rather reluctant to incorporate such built-in test techniques since the design specifications are stringent and exploit the full capabilities of advanced technology nodes.

In this work, we experiment with non-intrusive sensors to enable a built-in test for RF circuits that is totally transparent to the design, thus leaving it intact, as illustrated in Fig. 3.4 [34,63,101].

3.2.1 Principle of operation

The non-intrusive sensors capitalize on the undesired phenomenon of process variations. Process variations can be classified into two categories, according to their physical range on a die or wafer:

- *Die-to-die* (D2D) variations (or inter-die variations) refer to smooth and slow-varying variations that affect all devices on a die in the same way. For example, they cause the gate lengths of identical devices to be larger or smaller than the nominal by the same amount. D2D variations show a large degree of spatial correlation, which means that neighboring devices on the same die are affected in the same way. They include lot-to-lot variations, wafer-to-wafer variations, and across-wafer variations.
- *Within-die* (WID) variations (or intra-die variations) refer to variations rapidly varying over distances smaller than the die dimensions. Thus, WID variations may affect differently identical devices that are placed on the same die causing, for example, some devices to have larger gate lengths and others smaller gate lengths than the nominal. For some process parameters, such as the effective channel length, WID variations show a large degree of local spatial correlation, while for some others, such as the thickness oxide and the dopant concentration, WID variations are uncorrelated.

The underlying idea is to monitor process variations instead of measuring directly the RF performances. For this purpose, we can employ Process Control Monitors (PCMs), such as single layout components (e.g. transistors, capacitors, resistors, inductors), and dummy circuits that are extracted from the CUT topology (e.g. bias stages, current mirrors, gain stages, level-shifters, etc.). These sensors are placed in close physical proximity and are matched to identical structures in the CUT. For example, we can place a dummy bias stage next to the bias stage of the CUT, a dummy transistor next to a critical transistor in the CUT, etc. In this way, the sensors and the CUT "witness" the same D2D and correlated WID process variations and, as a result, the measurements obtained on the sensors will be correlated to the performances of the CUT to a very large extent.

Formally, let P_j denote the j-th performance of the CUT and let $\mathbf{X}$ denote the sensor measurements. The variation of the performance P_j, denoted by ΔP_j, and the variation of sensor measurements, denoted by $\Delta\mathbf{X}$, are linked to the D2D and correlated WID variations, denoted by $\Delta\mathbf{p}$, through some nonlinear functions f_{1j} and f_2:

$$\begin{aligned} \Delta P_j &= f_{1j}(\Delta\mathbf{p}) + r_1 \\ \Delta\mathbf{X} &= f_2(\Delta\mathbf{p}) + \mathbf{r}_2, \end{aligned} \tag{3.1}$$

where the parameters r_1 and $\mathbf{r}_2$ represent the uncorrelated WID variations. From (3.1), we can write

$$\Delta P_j = f_{1j}\left(f_2^{-1}(\Delta\mathbf{X} - \mathbf{r}_2)\right) + r_1. \tag{3.2}$$

Therefore, by tracking variations on the sensor measurements, we obtain information about the variations on the performances. To this end, we can use the machine learning-based test paradigm to infer implicitly the performances from the sensor measurements. Specifically, in an off-line preparatory training phase where we employ a large representative set of circuit instances with process variations, we learn one regression function per performance that maps the sensor measurements to the performance

$$g_j : \mathbf{X} \to P_j. \tag{3.3}$$

Once the training phase is completed, the regression functions can be readily used to predict the performances of any CUT simply from its sensor measurement pattern.

The accuracy of the drawn correlation and, thereby, the predictions of machine learning-based test, is negatively affected by two factors. First, the sensor measurements might not capture all the

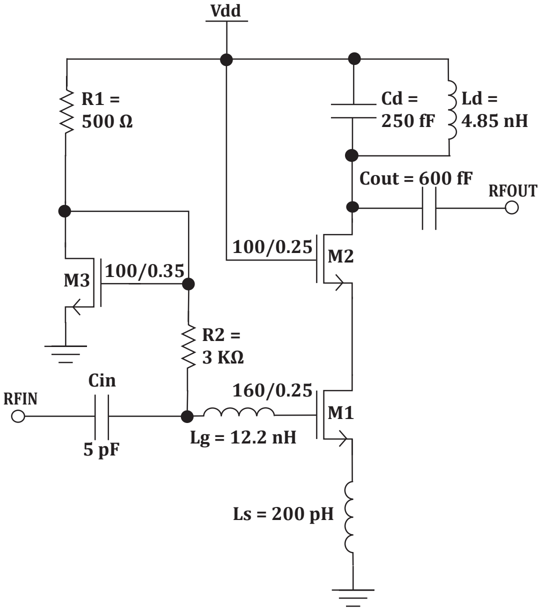


Figure 3.5: CMOS inductive degenerated cascode RF LNA.

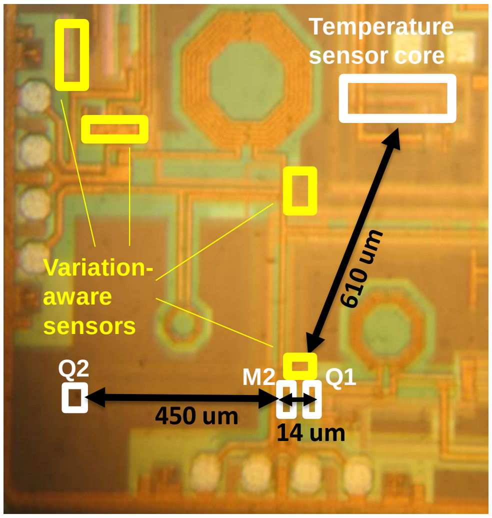


Figure 3.6: Photo of the fabricated chip showing the RF LNA with the embedded sensors.

sources of performance variations. Second, the uncorrelated WID variations can introduce noise in the correlation and the existing trend may be obscured or even eclipse.

This test approach has been inspired by the PCMs typically placed in the scribe lines of a wafer to monitor variability and identify off-target process parameters [102,103]. The idea of using die-level PCMs to extract information about performances has also been applied in the case of Analog-to-Digital Converters (ADCs) in [104]. It should be noted that with this test approach we can verify whether one or more performances violate their specifications due to excessive process variations, but we cannot detect defects within the CUT since the sensors are not electrically connected to it. Non-intrusive, defect-oriented built-in test can be performed using temperature sensors, as it will be discussed in details in Section 3.4.

3.2.2 Results

Our case study is an RF low noise amplifier (LNA), shown in Fig. 3.5. The selected PCMs include (a) a metal-insulator-metal (MIM) capacitor that mimics the geometry and layout of the input and output matching capacitors of the LNA and (b) a stand-alone diode connected MOS transistor that is matched to the gain transistor M_1 of the LNA. The selected dummy circuits include (a) a bias stage identical to the bias stage of the LNA formed by transistor M_3 and resistor R_1, (b) a current mirror using identical components M_3 and M_1 that is “inspired” from the schematic of the LNA by short-circuiting capacitor C_{in} and inductors L_g and L_s, and (c) a MOS gain stage that mimics the gain stage of the LNA formed by M_1 and M_2.

The LNA and the non-intrusive sensors were designed using the 0.25 μm Qubic4+ BiCMOS technology by NXP Semiconductors. The design was taped out in a Multi-Project-Wafer (MPW) run. It was placed in different locations in a reticle and the reticle was reproduced over the wafer. In total, we obtained 142 packaged samples that came from different sites and corners on a wafer. Fig. 3.6 shows a photo of the fabricated chip. As it can be seen, the sensors do not incur any area overhead since they are placed in between the inductors of the LNA, in areas on the die that otherwise would have been left void, in order to respect design-for-manufacturability (DFM) rules. Fig. 3.7 zooms in the dummy bias stage that is placed close to the bias stage of the LNA formed

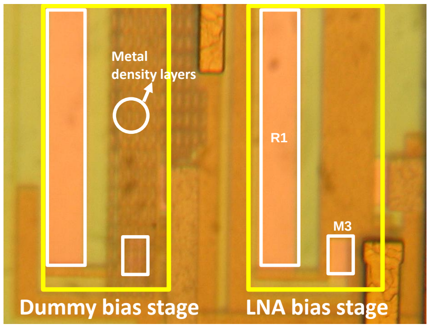


Figure 3.7: Photo of a dummy bias stage placed close to the bias stage of the LNA.

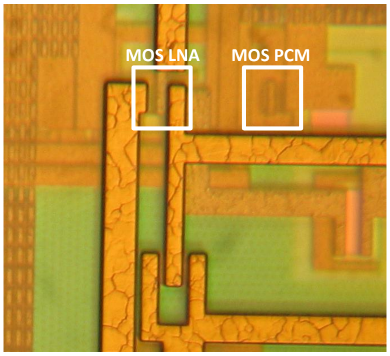


Figure 3.8: Photo of a MOS PCM placed close to the transistor of the gain stage of the LNA.

by resistor R_1 and transistor M_3. Fig. 3.8 zooms in the MOS transistor PCM that is placed close to the transistor M_1 of the gain stage of the LNA.

Fig. 3.9 shows correlation examples between sensor measurements and LNA performances. As it can be seen, the dummy capacitor correlates very well with S_{11}, which is expected since the input capacitor that is being monitored defines the input matching. Furthermore, the transconductance of the dummy transistor correlates very well with the gain, which again is expected because the transistor that is being monitored is critical for defining the gain.

Fig. 3.10 shows the predictions errors by adopting the machine learning-based test paradigm. The mean prediction error is lower than 2% for each performance. This proves that correlations between sensor measurements and LNA performances are very strong. Furthermore, the maximum prediction error is comparable to the measurement error on the ATE. Based on these experimental results, we consider that our findings are very promising and demonstrate that RF performances can be predicted using the non-intrusive variation-aware sensors.

3.3 RF circuit calibration based on non-intrusive variation-aware sensors

To increase performance while reducing the form factor, power consumption, and overall manufacturing costs, the trend nowadays is towards Systems-on-Chip (SoCs), where the RF transceiver is integrated together on the same die with the digital processor, memory, etc. While digital circuit design for advance technology nodes has largely benefited from design automation tools, the design of RF transceivers remains more like an art. For technology nodes below 65 nm, the manufacturing yield of RF transceivers drops significantly due to process variations, which is a show-stopper for the evolution of heterogeneous SoCs. To make the heterogeneous SoC integration possible in advance technology nodes, it is required to perform post-manufacturing calibration of RF transceivers with the aim to correct yield loss and to meet the stringent design specifications [105–109].

In this work, we have developed a post-manufacturing calibration methodology for RF circuits based on non-intrusive built-in sensors and pre-trained regression models [110], as shown in Fig. 3.11. The pre-trained regression models are used to infer the optimal tuning knob values directly from the result of a single test step that involves the non-intrusive built-in sensors. The calibration is succeeded in one-shot, that is, without needing to enter a test/tune loop.

3.3.1 One-shot calibration algorithm

Calibration is enabled by judiciously inserting *tuning knobs* into the circuit. The tuning knobs add degrees of freedom in the design and can act on all the performances irrespectively. The

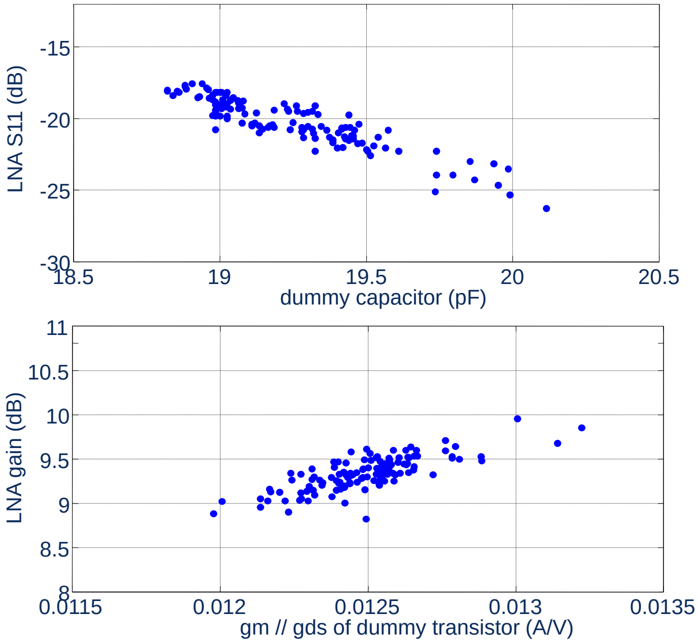


Figure 3.9: Correlations between sensor measurements and LNA performances.

performances $\mathbf{P}$ are related to the process parameters $\mathbf{p}$ and the tuning knobs $\mathbf{TK}$ with a function f

$$\mathbf{P} = f(\mathbf{p}, \mathbf{TK}). \tag{3.4}$$

Since it is not possible to measure directly the process parameters, we rely on a set of measurements $\mathbf{M}$ that are related to the process parameters with a function g

$$\mathbf{M} \approx g(\mathbf{p}), \tag{3.5}$$

where the approximation accounts for the fact that the measurements may not reflect all process parameters. Substituting (3.5) into (3.4) gives

$$\begin{aligned} \mathbf{P} &\approx f(g^{-1}(\mathbf{M}), \mathbf{TK}) \\ &\approx z(\mathbf{M}, \mathbf{TK}). \end{aligned} \tag{3.6}$$

The function z has an unknown and intricate closed form, thus we train a regression model to approximate it. To guarantee a mapping that is accurate across the feasible space of process variations and tuning knobs, we use circuit instances that are representative of the fabrication process and cover all process corners, as well as multiple combinations of tuning knobs that span uniformly the feasible tuning knobs range.

The pre-trained regression model can be readily used to calibrate a circuit according to the scheme in Fig. 3.11. The measurements are taken on non-intrusive sensors which offer an “image” of process variations. Since the non-intrusive sensors are not electically connected to the circuit, they stay invariant under changes of the tuning knob values. This allows us to perform the calibration in one-shot, as shown in Fig. 3.12. First, we obtain the measurements and we predict the performances for the nominal tuning knob setting using the pre-trained regression model. In case the performances

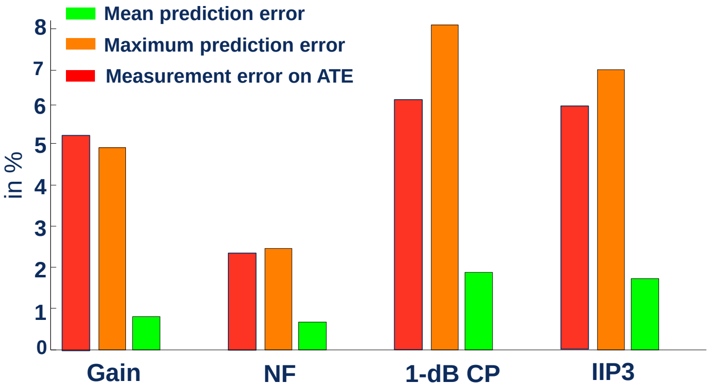


Figure 3.10: Machine learning-based prediction results using measurements from non-intrusive sensors.

are unsatisfactory, we run an optimization using as an underlying function the pre-trained regression model. In the course of optimization, tuning knob values are varied in a directed search towards performance values that meet our calibration objective. Since measurements stay invariant under changes of the tuning knob values they need to be obtained only once for any tuning knob setting and, subsequently, the values are plugged into the regression model and remain fixed during the course of the optimization.

The proposed calibration approach consists of obtaining a set of low-cost measurements only once and running an optimization algorithm quickly in software in the background using the ATE. Thus, it incurs overall a low cost that is a small fraction of the standard test cost. A final standard test may be performed after calibration is completed to measure the performances and confirm whether calibration has succeeded. In this way, we circumvent the risk of labeling a failing circuit as calibrated and functional. However, it should be noticed that the pre-trained regression model not only guides the calibration appropriately, but also predicts the performances for the optimal tuning knob setting at which the calibration converges. Thus, if the regression model predictions are deemed accurate, the final standard specification-based testing may be summarily eliminated. In this scenario, calibration and testing are performed together in one-shot at low-cost.

3.3.2 Results

Our case study is a 2.4 GHz RF power amplifier (PA) designed in the CMOS065 65nm technology provided by STMicroelectronics. The PA is based on a linear self-biased cascode class AB topology shown in Fig. 3.13(a). The complete PA, shown in Fig. 3.13(b), is composed of two similar self-biased cascode stages, namely a driver stage designed for maximum gain and a power stage designed for maximum output power. To optimize power transfer, two matching networks at the input (IM) and at the output (OM) have also been designed. The chosen tuning knobs are the power supply and bias voltage of each stage, as shown in Fig. 3.13(b), that is, no alterations in the design have been made. The non-intrusive sensors used in this case study are a dummy single resistor, a dummy single capacitor, and a dummy cascode gain stage for each PA stage, all extracted from the topology of the PA stages, as shown in Fig. 3.14.

As a first experiment, we perform "standard" calibration on a set of failing circuits to recover yield loss. Fig. 3.15 illustrates the histograms of the performances before we attempt calibration, that is, for the nominal tuning knob setting. As it can be observed, the majority of failing circuits violate the $OCP1$ and P_{DC} specifications. The histograms of calibrated circuits are superimposed on the histograms of non-calibrated circuits in Fig. 3.15. As it can be observed, the model prediction

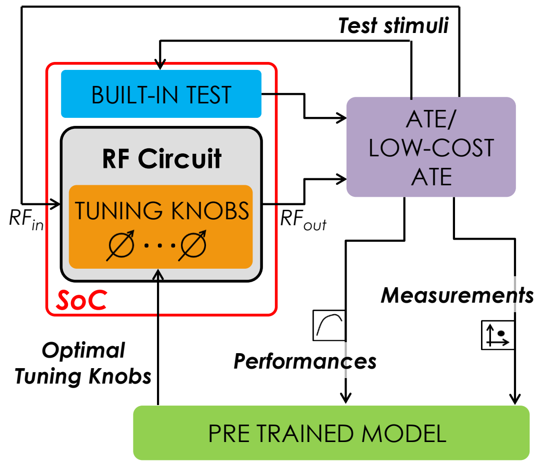


Figure 3.11: Flow of post-manufacturing calibration methodology for RF circuits.

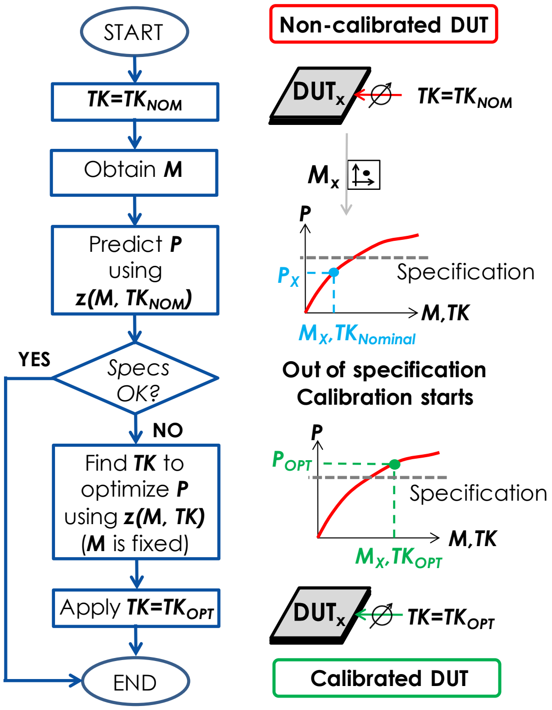


Figure 3.12: One-shot calibration algorithm.

is confirmed and we have recovered 100% of the yield loss. The distributions of the calibrated circuits lie well within the specification limit and, in general, they are more centered showing less dispersion. The fact that the model was not only adequate to achieve calibration, but also predicted correctly the performances of the calibrated circuits, shows that a final test is not really necessary.

As a second experiment, we perform calibration on a set of functional circuits with the aim to obtain a better performance trade-off. We set an "aggressive" goal to improve $Gain$, PAE, and $OCP1$ such that they have values better than the nominal design values while tolerating a slight DC power consumption. The aim of this experiment is to demonstrate that the proposed calibration method can be used to achieve stringent performance goals apart from yield loss recovering. A visual representation of the calibration efficiency is illustrated in Fig. 3.16, which shows the histograms of the performances before and after calibration. As it can be seen, for the three performances $Gain$, PAE, and $OCP1$ that have a lower specification, the sample means are moved clearly to the right. For the P_{DC} that has an upper specification the mean is also moved to the right, but the standard deviation is smaller and the largest part of the distribution lies on the left of the vertical line that corresponds to the goal.

3.4 Defect-oriented RF circuit test based on non-intrusive temperature sensors

When the CUT operates, part of its electric power is dissipated, that is, it is converted to heat due to the electro-thermal Joule effect. The heat is mostly conducted through the silicon substrate and the temperature in a sensing point near the CUT varies due to the power dissipated. This electro-thermal coupling has two main properties [111], as indicated in Fig. 3.17. First, the temperature decreases with the distance from the CUT. Second, high heat frequencies have little effect on the

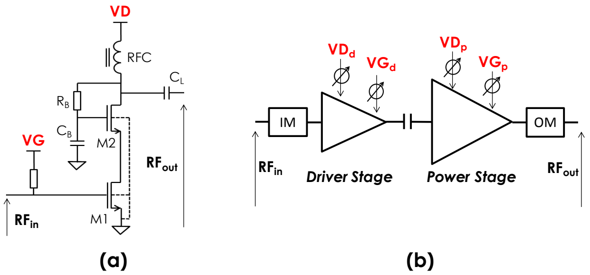


Figure 3.13: (a)Self-biased cascode topology chosen for each PA stage; (b) Two-stage PA with tuning knobs.

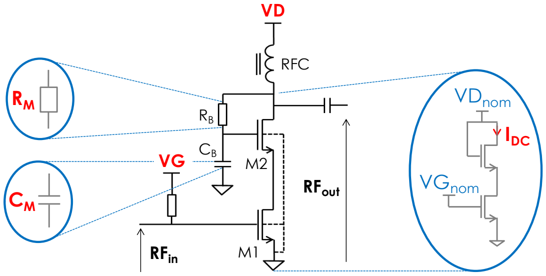


Figure 3.14: Non-intrusive sensors extracted from the topology of each PA stage.

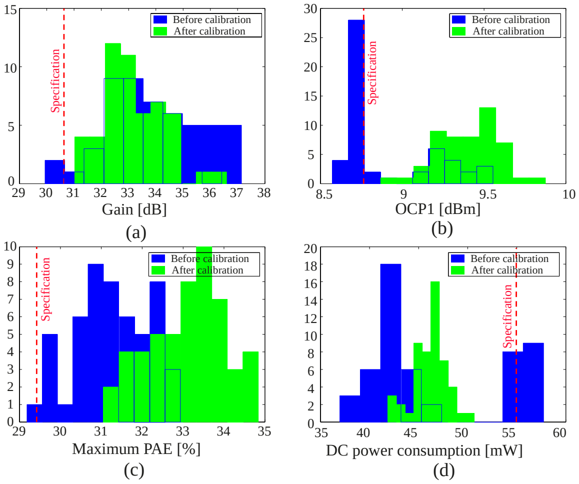


Figure 3.15: Circuit distributions before and after "standard" calibration.

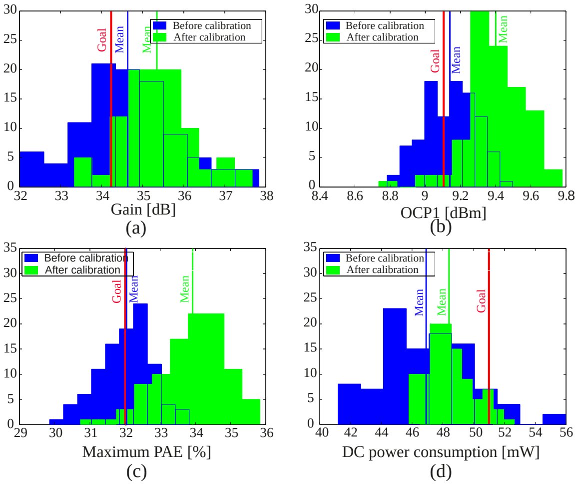


Figure 3.16: Circuit distributions before and after "aggressive" calibration.

temperature in the sensing point. This is because the heat transfer has a low-pass filter behaviour with a time constant defined by the thermal path of a few tens of kHz.

The dissipated power at a resistor (i.e. poly resistor, drain-to-source channel resistor of a transistor, etc.) in the CUT can be expressed as the product of the current that flows through this resistor and the voltage across its terminals

$$\begin{aligned} P(t) &= (V_{DC}+v(t))\cdot(I_{DC}+i(t)) \\ &= (V_{DC}+Acos(\omega_{RF}t))\cdot(I_{DC}+Bcos(\omega_{RF}t)) \\ &= \underbrace{\overbrace{V_{DC}I_{DC}}^{P_{bias}}+\overbrace{\frac{AB}{2}}^{P_{RF}}}_{P_{DC}}+\underbrace{(I_{DC}A+V_{DC}B)cos(\omega_{RF}t)}_{P_{f_{RF}}}+\underbrace{\frac{AB}{2}cos(2\omega_{RF}t)}_{P_{2f_{RF}}}. \end{aligned} \tag{3.7}$$

As it can be seen, the dissipated power has three spectral components at DC, f_{RF}, and $2f_{RF}$, denoted by P_{DC}, $P_{f_{RF}}$, and $P_{2f_{RF}}$, respectively. Since f_{RF} is much larger than the thermal cut-off

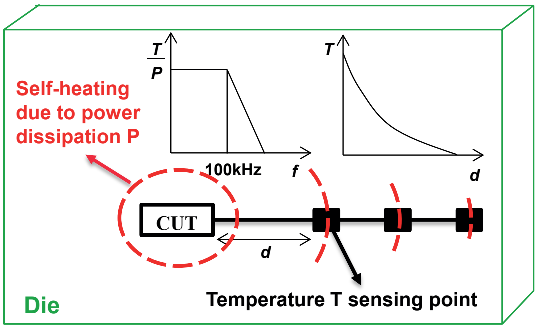


Figure 3.17: Thermal monitoring mechanism.

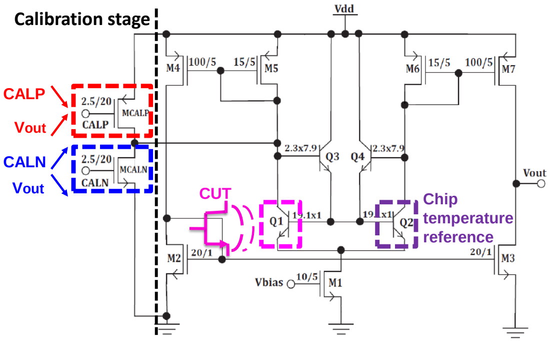


Figure 3.18: Schematic of differential temperature sensor.

frequency, it appears that only P_{DC} induces a temperature variation near the CUT. Yet, P_{DC} carries information about both the DC biasing (e.g. P_{bias} component) and the RF amplitude of the signals (e.g. P_{RF} component). By extension, by measuring temperature near a dissipating device of the CUT, we can monitor both the DC biasing point and RF operation of the CUT.

Now, a defect in the CUT will necessarily change the power dissipation from the expected range of values, thus creating a different temperature profile. This suggests that the defect can be detected by monitoring the temperature variation at a point near the CUT using a temperature sensor [101, 112].

3.4.1 Temperature Sensor

The thermal gradient across the silicon substrate can be measured using a differential temperature sensor. In this work, we have designed the temperature sensor shown in Fig. 3.18 [111], which is an open-loop operational transconductance amplifier with a differential pair formed by the parasitic bipolar transistors Q_1 and Q_2. Recalling that the collector current of a bipolar transistor has an exponential dependence on the temperature, a temperature difference ΔT between the locations of Q_1 and Q_2 will be reflected at the output voltage V_{out}. Thus, if we place Q_1 close to the CUT and Q_2 far away from the CUT, such that Q_1 senses the temperature close to the CUT and Q_2 senses a reference temperature, then V_{out} will respond to changes in the temperature at the location of Q_1 which are induced by the changes in the CUT temperature due to its power dissipation. The sensor strongly rejects common-mode temperature variations and has a high negative differential sensitivity $S_d = \Delta V_{out}/\Delta T$, that is, when ΔT increases V_{out} drops.

Initially, when the CUT is still off and we power on just the sensor (e.g. $\Delta T = 0$), the transfer function of the sensor will be positioned randomly, as shown by the grey curve in Fig. 3.19. The reason is that the sensor works in an open-loop configuration and its output resistance is very high in order to achieve a very high sensitivity. Such sensitivity is required specifically to monitor the RF operation of the CUT and this makes V_{out} very sensitive to process variations. Therefore, before employing the sensor in a test scheme, it is needed to accurately control its transfer function and adjust V_{out} to a desired value V_{ref} which, as it will be made clear later, is chosen to lie in the linear region close to V_{dd}, as shown with the blue curve in Fig. 3.19. For this purpose, we employ transistors $MCALN$ and $MCALP$ which operate as voltage-controlled current sources and introduce a controllable unbalance at the bipolar transistors Q_1 and Q_2. The calibration voltages $CALP$ and $CALN$ are varied to shift the transfer function and calibrate the sensor such that $V_{out} = V_{ref}$ for $\Delta T = 0$.

The effect of the calibration voltages is shown in Fig. 3.20. Initially, they are set to $CALP = V_{dd}$ and $CALN = 0$. Suppose that we want to set $V_{out} = V_{ref}$ and that before calibration $V_{out} = V_0$ and the current flowing in M_5 is $IM5_0$. If $V_0 > V_{ref}$, then we increase $CALN$ while, if $V_0 < V_{ref}$,

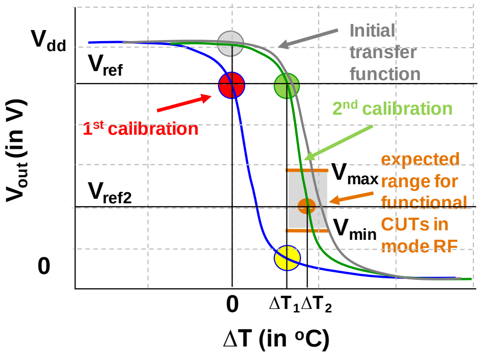


Figure 3.19: Test scheme illustration.

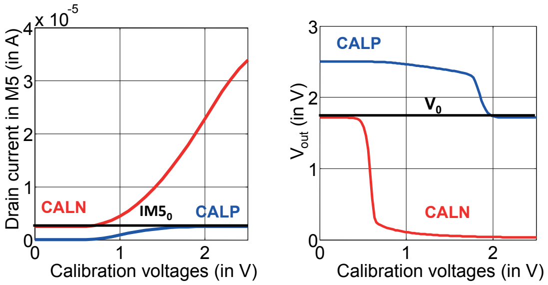


Figure 3.20: Effect of calibration voltages.

then we reduce $CALP$. By reducing $CALP$, we reduce the current flowing in M_5 which, in turn, reduces the gate-to-source voltage of M_3 and increases V_{out}, in order to maintain the balance at the output stage M_3-M_7. Similarly, by increasing $CALN$, we increase the current flowing in M_5 which, in turn, increases the gate-to-source voltage of M_3 and reduces V_{out} always to maintain the balance at the output stage M_3-M_7. The calibration plays an important role in the defect-oriented test scheme as is explained next.

3.4.2 Defect-oriented test scheme

Consider the scenario where both the CUT and the temperature sensor are defect-free. If we power on only the temperature sensor, then we will be able to calibrate it by varying either $CALP$ or $CALN$ such that $V_{out} = V_{ref}$, as explained in the previous section and shown by the blue curve of Fig 3.19. If $CALP$ is varied, let $[CALP^{(1)}_{min}, CALP^{(1)}_{max}]$ be the interval wherein $CALP$ lies in the end of the calibration for any defect-free temperature sensor. If $CALN$ is varied, let $[CALN^{(1)}_{min}, CALN^{(1)}_{max}]$ be the interval wherein $CALN$ lies in the end of the calibration for any defect-free temperature sensor.

Next, we power on the CUT which results in a non-zero ΔT_1 and, thus, V_{out} shifts away from V_{ref}. Typically, biasing the CUT results in a drastic temperature increase ΔT_1 at the vicinity of Q_1 and, thereby, the temperature sensor is saturated at V_{out} close to 0 due to its high sensitivity, as shown in Fig. 3.19. Thereafter, in order to extract the information that reflects the bias operation of the CUT, the sensor is calibrated a second time by reducing $CALP$ such that $V_{out} = V_{ref}$. Thus, the variation of $CALP$ with respect to its typical value (when the CUT is off) is directly related to the power dissipated by the CUT when it is powered on. By re-calibrating the temperature sensor, its transfer function shifts, as shown by the green curve in Fig. 3.19. If $CALP$ was varied in the previous calibration step, let $[CALP^{(2)}_{min,p}, CALP^{(2)}_{max,p}]$ be the interval wherein $CALP$ lies in the end of this calibration for any defect-free temperature sensor. If $CALN$ was varied in the previous calibration step, let $[CALP^{(2)}_{min,n}, CALP^{(2)}_{max,n}]$ be the interval wherein $CALP$ lies in the end of this calibration for any defect-free temperature sensor.

Next, we apply an RF stimulus at the input of the CUT which changes the DC power component and produces a temperature variation ΔT_2 in the vicinity of Q_1. This temperature variation is small and the output of the sensor changes to a value V_{ref2}, where V_{ref2} is still within the linear region, as shown in Fig. 3.19. Let $[V_{min}, V_{max}]$ be the interval wherein V_{ref2} lies for any defect-free temperature sensor.

All the above intervals can be extracted by characterizing a set of defect-free chips across a split matrix lot so as to take into consideration all manufacturing worst case variations.

Based on the above defect-free scenario, the test scheme consists of three phases. In the first phase, we validate that the temperature sensor is defect-free so that it can be used to test the CUT. We attempt to calibrate the temperature sensor at $V_{out} = V_{ref}$ and if we do not succeed or if the required $CALP$ or $CALN$ are outside the pre-defined intervals $[CALP^{(1)}_{min}, CALP^{(1)}_{max}]$ and $[CALN^{(1)}_{min}, CALN^{(1)}_{max}]$, then we conclude that the temperature sensor is defective.

In the second phase, while the temperature sensor is calibrated at $V_{out} = V_{ref}$, we power on the CUT. If V_{out} does not saturate, we conclude that the CUT is defective given that the sensor is designed such that its output saturates for nominal power dissipation. If the temperature sensor saturates, then we attempt to calibrate it again at $V_{out} = V_{ref}$. If we cannot calibrate it or if we succeed to calibrate it and the required $CALP$ is outside the pre-defined intervals $[CALP^{(2)}_{min,p}, CALP^{(2)}_{max,p}]$ or $[CALP^{(2)}_{min,n}, CALP^{(2)}_{max,n}]$, depending on whether $CALP$ or $CALN$ is used for the calibration in the first phase, then we conclude that the CUT is defective. Otherwise, we move on to the third phase.

In the third phase, while the CUT is powered on and the temperature sensor is calibrated at $V_{out} = V_{ref}$, we apply the RF stimulus at the input of the CUT. If V_{out} is outside the pre-defined interval $[V_{min}, V_{max}]$, then we conclude that the CUT is defective. This phase can detect defects across inductors or capacitors that cannot be detected in the second phase when the CUT is only biased.

3.4.3 Results

Our case study is the LNA shown in Fig. 3.5. Fig. 3.6 shows the positioning of the temperature sensor on the die. We have chosen to place the sensing transistor Q_1 of the temperature sensor in close proximity to the cascode transistor M_2 since this transistor will manifest more profoundly variations in the RF signal.

We select $V_{ref} = 1.7$ V. First we power on the temperature sensor while keeping the LNA off. The blue histogram in Fig. 3.21 shows the initial V_{out} values before calibration observed across all 142 samples. As it can be seen, V_{out} varies widely around V_{ref} due to process variations. Thus, in the first phase of the test scheme, we calibrate the temperature sensor to $V_{out} = V_{ref}$ by decreasing either $CALP$, if $V_{out} < V_{ref}$, or by increasing $CALN$, if $V_{out} > V_{ref}$. This is shown in Fig. 3.22 where each curve corresponds to one sample and shows the variation of V_{out} towards V_{ref} as we reduce $CALP$ (curves on the right-hand side) or as we increase $CALN$ (curves on the left-hand side). For example, the curve AB corresponds to a sample that has $V_{out} = 0.55$ V and, thus, $CALP$ is reduced from V_{dd} to 1.72 V, in order to bring V_{out} to V_{ref}. This is the outer curve, thus, the point B defines $CALP^{(1)}_{min}$. Similarly, the outer curve $A^{'}B^{'}$ defines $CALP^{(1)}_{max}$ and, regarding the samples that are calibrated via $CALN$, the outer curves CD and $C^{'}D^{'}$ define $CALN^{(1)}_{max}$ and $CALN^{(1)}_{min}$, respectively. In Fig. 3.21, the histogram of V_{out} values after the first calibration is superimposed on the histogram of initial V_{out} values. As can be seen, V_{out} is set to V_{ref} with a precision better than 50 mV.

Next, we power on the LNA and we step its power supply from 0 to 2.5 V. The sensor is able to track in a contact-less way the power dissipated by the LNA. As expected, by increasing the power supply the DC power dissipated by M_2 increases which, in turn, increases the temperature at Q_1 and V_{out} decreases since the temperature sensor has a negative sensitivity. When the power supply is set to 2.5 V, for all samples the temperature sensor saturates at V_{out} close to 0, as is also shown by the blue histogram of V_{out} in Fig. 3.23. Thus, in the second phase of the test scheme, we calibrate the temperature sensor to $V_{out} = V_{ref}$ by reducing $CALP$ since for all samples $V_{out} < V_{ref}$. This is shown in Fig. 3.24 where each curve corresponds to one sample. The dashed curves correspond to the samples that were calibrated using $CALP$ in the first test phase. For those samples, the initial value of $CALP$ in the calibration of the second test phase is lower than 2.5 V. The continuous curves correspond to the samples that were calibrated using $CALN$ in the first test phase. For those samples, the initial value of $CALP$ in the calibration of the second test phase equals 2.5 V. Fig. 3.24 also indicates the intervals $[CALP^{(2)}_{min,p}, CALP^{(2)}_{max,p}]$ and $[CALP^{(2)}_{min,n}, CALP^{(2)}_{max,n}]$. Fig. 3.23 shows the histogram of V_{out} after the second calibration. As in the previous phase, V_{out} is set

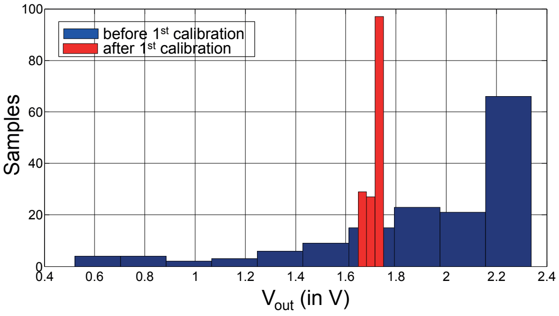


Figure 3.21: Temperature sensor output before and after the first calibration.

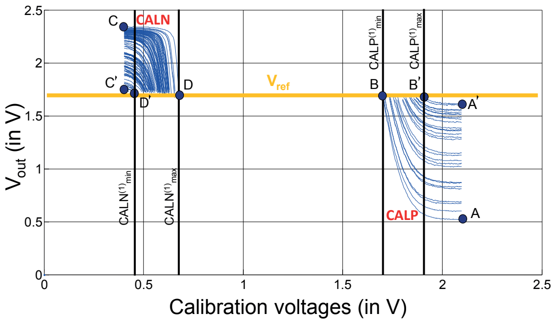


Figure 3.22: First calibration of the temperature sensor.

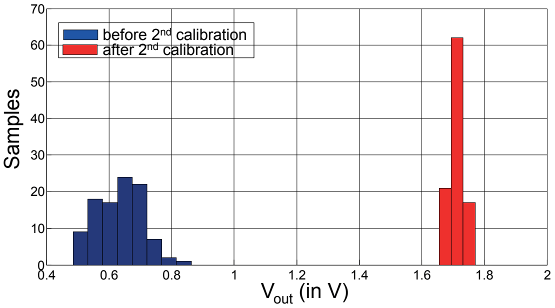


Figure 3.23: Temperature sensor output before and after the second calibration.

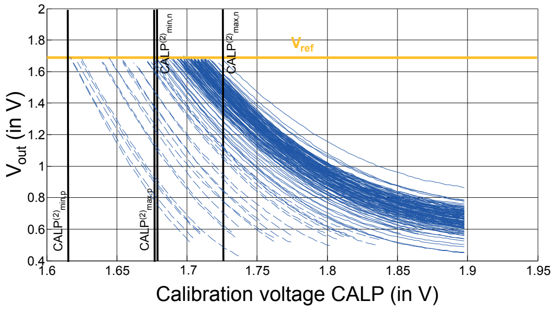


Figure 3.24: Second calibration of the temperature sensor.

to V_{ref} with a precision better than 50 mV.

Next, we apply an RF stimulus at the input of the LNA with frequency 2.4 GHz and amplitude varying from −12 dBm to 10 dBm and we record V_{out}. Fig. 3.25 shows the result of the measurement for all samples. As expected, by increasing the RF amplitude the DC power dissipated by M_2 increases which, in turn, increases the temperature at Q_1 and V_{out} decreases. We also observe the 1-dB compression point of the LNA which corresponds to the knee of the curves at around −7.4 dBm. As it can be seen, for an input amplitude of 10 dBm, for all samples V_{out} decreases linearly to a value in the range $[V_{min}, V_{max}] = [1.08, 1.43]$ which lies in the linear region of the transfer function of the temperature sensor, as expected from Fig. 3.19.

3.5 Built-in self-test of ΣΔ ADCs

The standard approach for characterizing the dynamic performance of an analog-to-digital converter (ADC), i.e. signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SNDR), etc., requires the application of a full-scale sinusoidal analog test stimulus at the input of the ADC and the collection of a high number of output samples to accurately compute the spectrum of the ADC response. Implementing a BIST approach is extremely challenging mainly because the resolution of the analog test stimulus is required to be at least two or three bits above the resolution of the ADC, such that the noise and distortion at the output are predominantly due to the ADC [113–118].

ΣΔ ADCs offer the possibility of replacing the on-chip generation of a high-resolution analog test stimulus with equivalent digital techniques. As shown in Fig. 3.26, the starting point is to use an ideal ΣΔ modulator in software that converts a high-resolution analog sinusoidal to a bitstream [95]. The bitstream is divided in sub-bitstreams of length N and the sub-bitstream with

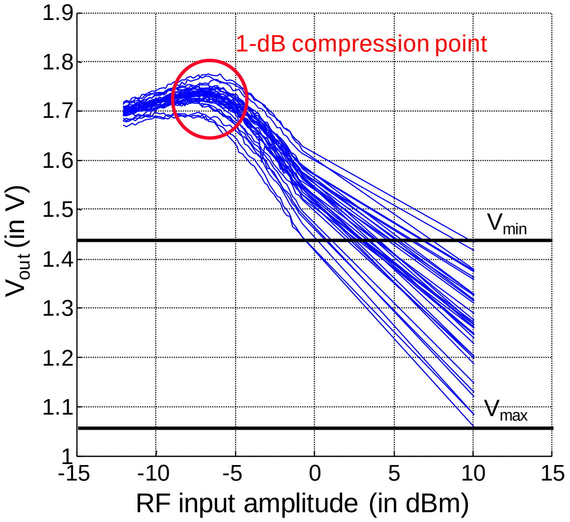


Figure 3.25: Temperature sensor output as a function of the amplitude of the RF stimulus.

the highest resolution (i.e. highest SNR, SNDR, etc.) is selected to be periodically reproduced through a circular shift register. In the case of switched-capacitor (SC) ΣΔ ADCs, the bitstream can be fed directly into the modulator by adding simple circuitry at its input [119–121], which circumvents the need to integrate a 1-bit digital-to-analog converter (DAC) and a low-pass filter to remove the quantization noise [122, 123]. However, the direct application of the bitstream to the input of the ADC will overload the modulator, unless the reference voltages of the 1-bit DAC are adequately attenuated. Unfortunately, by attenuating these reference voltages we also scale down the amplitude of the encoded sinusoidal. The maximum amplitude that can be encoded in the bitstream is in fact less than the actual dynamic range of the ADC and, thereby, we do not test the dynamic performances of the ADC at full scale. Especially for measuring SNDR, the amplitude of the test stimulus has to be as close as possible to full scale such that the harmonic distortion introduced by the ADC under test is amply manifested [124].

A solution to this problem is proposed in [125], however it requires modifying significantly the input stage of the modulator. In this work, we developed an elegant solution based on digital ternary stimuli that incurs minimal overhead and allows measuring SNDR for amplitudes close to full scale [126, 127].

3.5.1 Dynamic test of ΣΔ ADCs using digital ternary stimuli

Stimulus generation

Fig. 3.27 shows the general block diagram of the proposed fully-digital BIST strategy for measuring the SNDR of ΣΔ ADCs. The BIST circuitry is mainly composed of two digital blocks, namely the Stimulus Generator and Response Analyzer. During test mode, the ΣΔ ADC under test is disconnected from the main signal path and is connected to the Stimulus Generator and the Response Analyzer. The Stimulus Generator provides an optimized digital ternary stimulus to the input whereas the Response Analyzer computes the SNDR based on a simplification of the sine-wave fitting algorithm [120, 128–131].

The ternary stimulus is composed of three levels $\{-1, 0, 1\}$ and is generated in the digital domain by adding a ΣΔ encoded binary bitstream with a delayed version of itself, as shown in Fig. 3.28. From a spectral point of view, the Discrete Fourier Transform (DFT) of a length-N bitstream $\{b_0, \cdots, b_{N-1}\}$ is given by

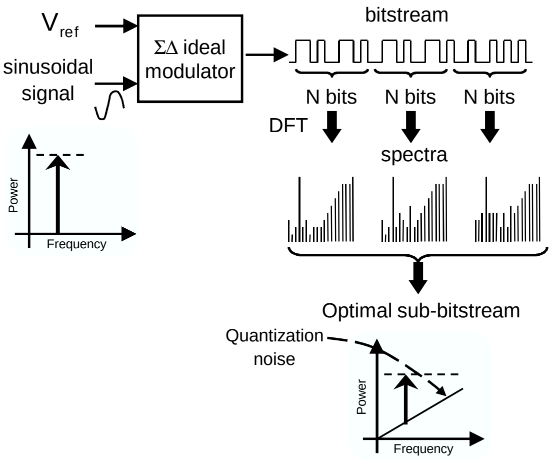


Figure 3.26: Generation of optimized ΣΔ digital bitstreams.

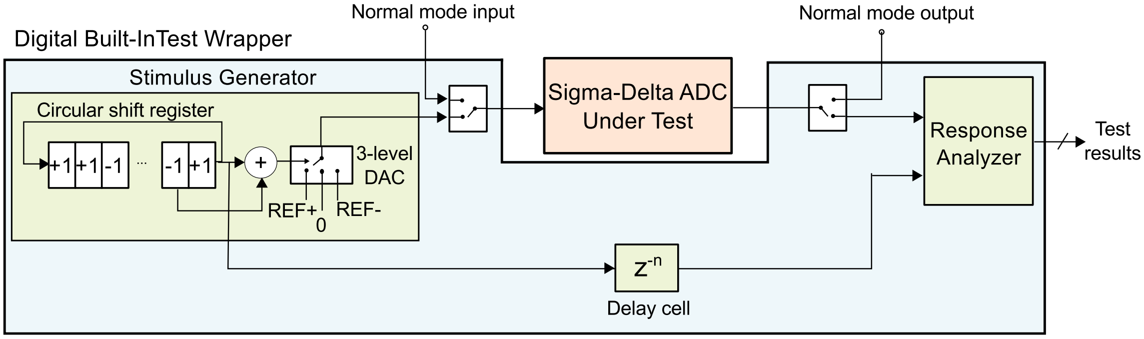


Figure 3.27: General block diagram of the BIST strategy for ΣΔ ADCs.

$$B(k) = \sum_{n=0}^{N-1} b_n \cdot e^{-j\frac{2\pi \cdot n}{N}k}, \quad k = 0, \cdots, N-1. \tag{3.8}$$

The N periodic extension leads to a spectrum made by N lines located at $f_k = kf_s/N$, where f_s is the sampling frequency. The DFT of the circular-shifted bitstream delayed by δ samples $\{b_\delta, \cdots, b_{N-1}, b_0, \cdots, b_{\delta-1}\}$ is obtained by applying the time shift theorem to (3.8)

$$B_\delta(k) = B(k) \cdot e^{-j\frac{2\pi}{N}\delta k}, \quad k, \delta = 0, \cdots, N-1. \tag{3.9}$$

The DFT of the ternary stream is then obtained by averaging the DFT of the original bitstream and the DFT of the circular-shifted version of it and by using the linearity property of the DFT

$$T(k) = \frac{B(k)}{2}\left(1 + e^{-j\frac{2\pi}{N}\delta k}\right), \quad k, \delta = 0, \cdots, N-1. \tag{3.10}$$

The Power Spectral Density (PSD) of the bitstream and the ternary stream are given by

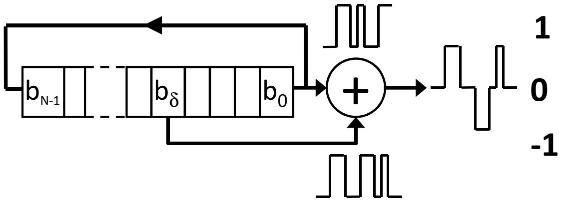


Figure 3.28: Ternary stream construction.

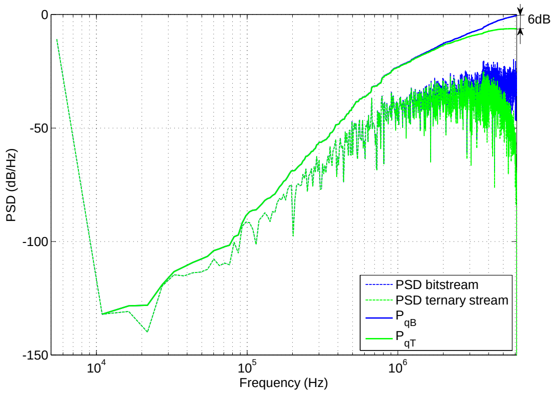


Figure 3.29: Power spectral density and cumulative power spectral density of a bitstream and a ternary stream for $\delta = 1$.

$$\begin{aligned} S_B(k) &= \|B(k)\|^2 \qquad (3.11) \\ S_T(k) &= S_B(k) \cdot cos^2\left(\frac{\pi k \delta}{N}\right) \qquad (3.12) \\ & k, \delta = 0, \cdots, N-1. \end{aligned}$$

Therefore, for $\delta = 1, \cdots, N-1$, $k = 0, \cdots, N-1$, the amplitude of the spectra of the ternary stream is lower than the amplitude of the spectra of the bitstream, i.e. $S_T(k) < S_B(k)$, and the cumulative PSD of the ternary stream $Pq_T(n) = \sum_{k=2}^{n} S_T(k)$ is less than the cumulative PSD of the bitstream $Pq_B(n) = \sum_{k=2}^{n} S_B(k)$, i.e. $Pq_T(n) < Pq_B(n)$, $n = 2, \cdots, N-1$. This is shown graphically in Fig. 3.29 for $\delta = 1$. As it can be observed, the spectra of the ternary stream presents a high frequency filter behaviour and the quantization noise power of the ternary stream is about 6 dB less than the quantization noise power of the bitstream. In other words, the ternary stream overloads less the modulator compared to the bitstream and, thereby, offers the possibility of testing the $\Sigma\Delta$ ADC closer to full scale.

The fundamental of the ternary stream is given from (3.10) for $k = 1$

$$\begin{aligned} T(1) &= \frac{B(1)}{2} \cdot \left(1 + e^{-j\frac{2\pi}{N}\delta}\right) \\ &= B(1) \cdot cos\left(\frac{\pi \cdot \delta}{N}\right) \cdot e^{-j\frac{\pi}{N}\delta}, \qquad (3.13) \\ & \delta = 0, \cdots, N-1. \end{aligned}$$

If we denote by A_T and Φ_T the amplitude and the phase of the fundamental of the ternary stream and by A_B and Φ_B the amplitude and the phase of the fundamental of the bitstream, then from (3.13)

$$\begin{aligned} A_T &= A_B \cdot \left|cos\left(\frac{\pi \cdot \delta}{N}\right)\right| \qquad (3.14) \\ \Phi_T - \Phi_B &= -\frac{\pi}{N}\delta \qquad (3.15) \\ & \delta = 0, \cdots, N-1. \end{aligned}$$

Therefore, when $\delta \ll N$, $A_T \approx A_B$ and $\Phi_T \approx \Phi_B$, i.e. the amplitude and the phase of the fundamental encoded in the ternary stream are practically the same with the amplitude and the phase of the fundamental encoded in the bitstream. As δ increases, A_T decreases with respect to A_B and the phase difference $\Phi_T - \Phi_B$ moves away from zero.

The spectral quality of the ternary stimulus is defined by two parameters, namely the initial bitstream and the delay parameter δ. Concerning the initial bitstream, the optimization loop simulates an ideal $\Sigma\Delta$ modulator of one order higher than the $\Sigma\Delta$ modulator under test using a pure sinusoidal input signal of an amplitude A_T, as shown in Fig. 3.26. From the output of this ideal $\Sigma\Delta$ modulator, the algorithm selects several bitstreams of length N equal to the period of the input signal and it records their total power $P_B = Pq_B(N-1)$. Next, for each bitstream, it computes the SNDR and the total power of the resulting ternary stream $P_T = Pq_T(N-1)$ for different values of δ. The objective of the optimization loop is to select a ternary stream that has a SNDR larger than the SNDR specification of the $\Sigma\Delta$ modulator by at least 3 effective number of bits (ENOB) and a low power P_T or, equivalently, a large ratio P_B/P_T. Finally, this algorithm is repeated for different input signal amplitudes A_T, in order to generate optimized test stimuli that cover the whole dynamic range of the $\Sigma\Delta$ ADC under test.

Response analysis

The analysis of the ADC response is performed by a simplified version of the sine-wave fitting algorithm. This simplification is based on the fact that the test stimulus and reference signal have the same frequency and they are completely synchronized, which saves us from computing the phase of the test response. This synchronization between the response and reference signals is easily achieved in the digital domain by designing the delay cell in Fig. 3.27 to match the delay introduced by the $\Sigma\Delta$ modulator.

In a first step, the algorithm computes the DC component of the response signal as

$$DC = \frac{1}{N}\sum_{i=1}^{N} S_{out}(i), \tag{3.16}$$

where $S_{out}(i)$ are the samples of the ADC output (i. e. the signal under evaluation) and N is the number of samples considered in the evaluation. In a second step, the algorithm computes the point-to-point correlation of the response and reference signals as

$$Correl = \sum_{i=1}^{N} S_{out}(i) S_{ref}(i), \tag{3.17}$$

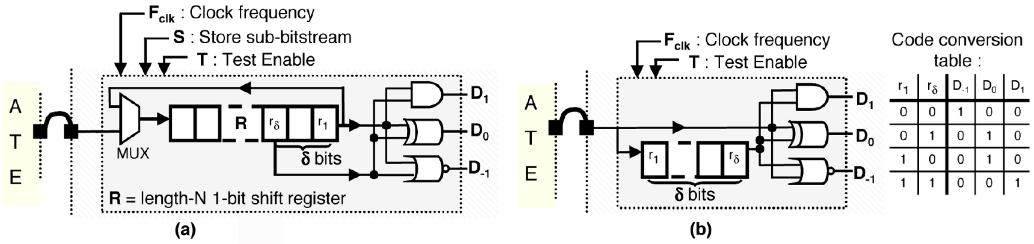
where $S_{ref}(i)$ are the samples of the reference signal. The amplitude of the response signal is related to the computed correlation as

$$A = \frac{2}{NA_{ref}} Correl, \tag{3.18}$$

where A_{ref} is the amplitude of the reference signal, which is known *a priori.* Once the amplitude of the response signal has been computed, the algorithm continues by adjusting the reference signal to the amplitude and DC values obtained

$$S_{ref,adj}(i) = \frac{A}{A_{ref}} S_{ref}(i) + DC. \tag{3.19}$$

Finally, the algorithm computes the noise and distortion power in the response signal, denoted by P_{error}, by comparing the samples of the ADC output with the samples of the adjusted reference signal



Code conversion table :

r_1	r_δ	D_{-1}	D_0	D_1
0	0	1	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1

Figure 3.30: On-chip generation of the ternary stream.

$$P_{error} = \frac{1}{N}\sum_{i=1}^{N}\left(S_{out}(i) - S_{ref,adj}(i)\right)^2. \tag{3.20}$$

With the obtained P_{error} it is straightforward to compute the SNDR of the response signal as

$$SNDR = 10\log\frac{A^2/2}{P_{error}}. \tag{3.21}$$

By performing a comparison with a preloaded threshold, the BIST can provide a go/no-go output signal. Specifically, from (3.21)

$$Go/No\text{-}Go = \begin{cases} 1, & \text{if } \frac{A^2}{2} \geqslant P_{error}10^{SNDR_{spec}/10} \\ 0, & \text{if } \frac{A^2}{2} < P_{error}10^{SNDR_{spec}/10} \end{cases} \tag{3.22}$$

where the threshold value $SNDR_{spec}$ is the actual SNDR specification limit.

3.5.2 On-chip implementation

The ternary stimulus can be efficiently generated on-chip while the response analysis is a purely digital algorithm, making the proposed strategy overall very suitable for a full BIST implementation, as illustrated in the general block diagram in Fig. 3.27.

Specifically, the ternary stimulus generator, although it is mostly digital, requires the introduction of a mixed-signal element, i. e. a 3-level DAC, to interface the digital ternary stimulus to the analog $\Sigma\Delta$ modulator. Fig. 3.30 shows two different possible implementations for the digital part of the ternary stimulus generator. Fig. 3.30(a) shows a strategy where the ATE is occupied for a very small time interval to store in an on-chip shift register the length-N bitstream. During the testing phase, the bitstream circulates in the shift register and three logic gates are used to generate $\{D_{-1}, D_0, D_1\}$ that correspond to the three states $\{-1, 0, 1\}$ of the ternary stream. Another possibility, which incurs a lower area overhead, is to provide periodically the bitstream directly from the ATE, as shown in Fig. 3.30(b). This last implementation is attractive in the case where the bitstream can be generated on-chip using a digital resonator.

Concerning the injection of the digital ternary stimulus into the analog input of the modulator, the necessary digital-to-analog interface can be easily merged into the input section of a SC $\Sigma\Delta$ modulator. Fig. 3.31 shows an implementation example for a generic fully-differential SC $\Sigma\Delta$ modulator. This implementation exploits the inherent linearity of 1-bit DACs built by two switches to perform the conversion. The test is enabled for $T = 1$. The states 1 and -1 are converted to a positive ΔV_{ref} and a negative $-\Delta V_{ref}$ differential voltage, respectively. To preserve the linearity of the test stimulus, the 0 state must correspond to the middle point between ΔV_{ref} and $-\Delta V_{ref}$, that is, the null differential voltage. Thus, the state 0 must be implemented by generating a null differential voltage at the input of the sampling capacitors, which corresponds to fully discharging

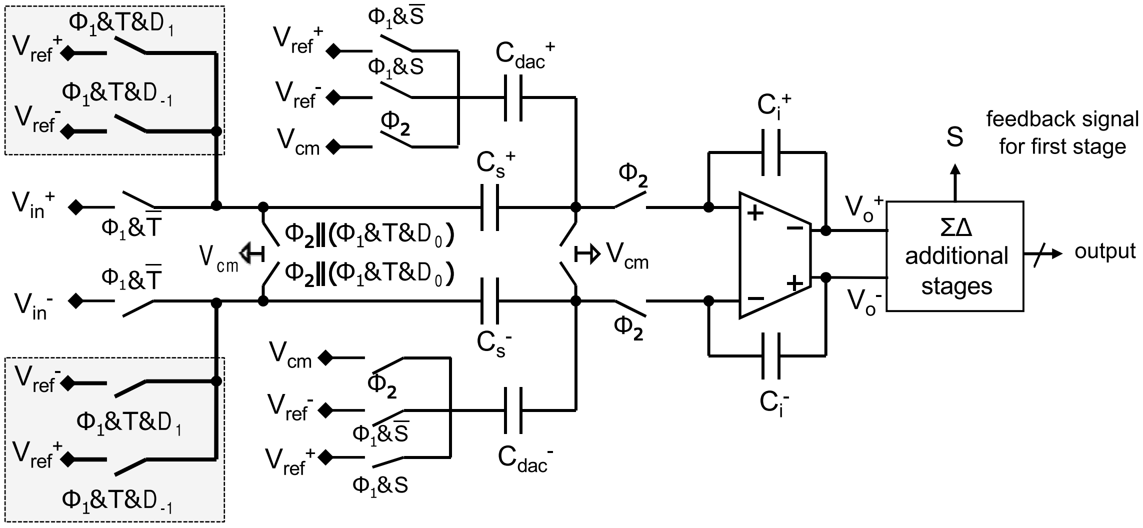


Figure 3.31: Injection of the ternary stream $\{D_{-1}, D_0, D_1\}$ at the input of a SC ΣΔ modulator.

the sampling capacitors. This can be achieved by switching the sampling capacitors to the common-mode voltage V_{cm} during the sampling phase, as shown in Fig. 3.31. Notice that the injection of the 0 state makes use of existing switches while the injection of the 1 and -1 states requires the addition of only four additional switches that are in the highlighted area.

Finally, the decimation filter of the ΣΔ ADC and the Response Analyzer are completely digital blocks and can be synthesized using standard digital design techniques.

3.5.3 Results

The ADC under test in our case study is a stereo 18-bit ΣΔ ADC designed in a 40nm CMOS technology and is provided by ST Microelectronics. The modulator is a fully-differential 2:1 MASH. The modification of the input stage of the 2:1 MASH modulator to accommodate the injection of the digital ternary test stimulus does not degrade the original dynamic performances. Fig. 3.32 shows the SNDR obtained at the output of the modulator by transistor-level simulation using as test stimuli an ideal analog sinusoidal and a digital ternary signal that encodes this ideal analog sinusoidal. The ideal analog sinusoidal has a frequency of 6KHz and an amplitude of 2.25V that corresponds to the maximum input range for the modulator. The spectrum of the output signal of the modulator was computed using a Blackman-windowed Fast Fourier Transform (FFT) over 30 signal periods. As it can be seen from Fig. 3.32, the BIST offers an equivalent measurement of the SNDR with any discrepancies being well into the error introduced by the FFT due to limited number of samples. Fig. 3.33 shows the layout of the designed chip that comprises the ΣΔ ADC with the dynamic BIST. The area overhead introduced by the BIST is only 7.7% and is mostly dominated by the digital test resources for performing the control and for analyzing the response. The chip has been taped out and measurement results are expected in May 2015.

3.6 Design-for-test for pipeline ADCs

Differential Non Linearity (DNL) and Integral Non Linearity (INL) are the two main static performances that are measured during production testing of ADCs. In the standard testing scheme, a saturated sine-wave or ramp is applied to the input of the ADC and the number of occurrences of each code at the output is obtained to construct the histogram, from which DNL and INL can be readily calculated. This standard static test approach requires the collection of a large volume of

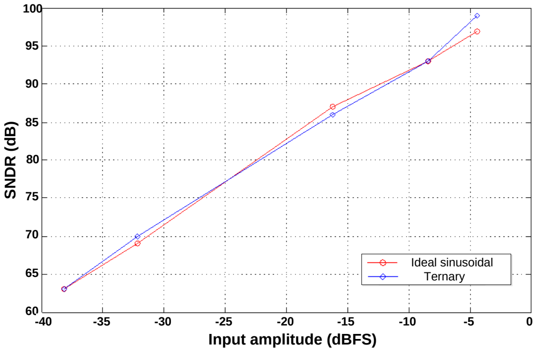


Figure 3.32: SNDR vs. input amplitude curves obtained by transistor-level simulation.

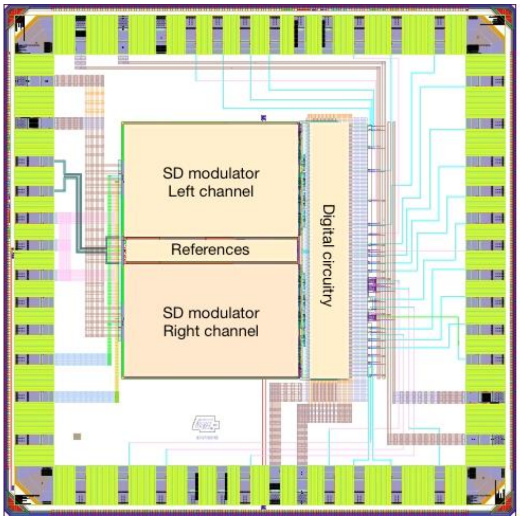


Figure 3.33: Layout view of the developed stereo ΣΔ ADC with dynamic BIST.

data since each code needs to be traversed many times to average noise. The volume of data increases exponentially with the resolution of the ADC to a degree where the static test time becomes prohibitively large for high-resolution ADCs. Nowadays, the static test of high resolution ADCs is addressed with the same standard approach used for low-resolution ADCs. As a result, the static test time is disproportionally high as compared to the silicon area that the ADCs occupy on the die of a System-on-Chip (SoC) and as compared with the test time of other types of mixed-signal circuits in the SoC. According to published data from industry [6], although mixed-signal circuits occupy an area less than 5% in a modern SoC, testing the mixed-signal functions takes up to 30% of the total test time. Given that ADCs are among the most commonly met mixed-signal circuits in SoCs and since high static test times translate to high test costs, reducing the static test time for ADCs is an area of industry focus and innovation.

Many alternative test techniques aiming at reducing the static test cost for ADCs have been reported in the literature [81, 132–148]. In this work, we propose an efficient reduced-code linearity test technique [149–151]. Reduced-code testing can be applied to ADCs that, by virtue of their operation, have groups of output codes which have the same width [152–154]. We have considered specifically pipeline ADCs as our case study. The same principles, however, can be extended to other Niquist rate multi-step ADC architectures, such as Successive Approximation Register (SAR), logarithmic, sub-ranging, cyclic, etc.

3.6.1 Reduced-code linearity testing

Principle

A pipeline ADC consists of a cascade of stages, as shown in Fig. 3.34. Each stage consists of a sample-and-hold (S/H) circuit, a sub-ADC, a sub-DAC, a subtractor, and an amplifier. The input signal to each stage is first converted by the sub-ADC to a digital code which is the output of the stage. The result of the conversion is reconverted by the sub-DAC to an analog signal and subsequently subtracted from the input signal. The result of the subtraction is amplified so as to use the same reference voltage in all stages. The residue of the first stage is sampled by the second stage and so forth. The digital logic assembles the digital codes of the cascaded stages and provides the digital output of the ADC [155].

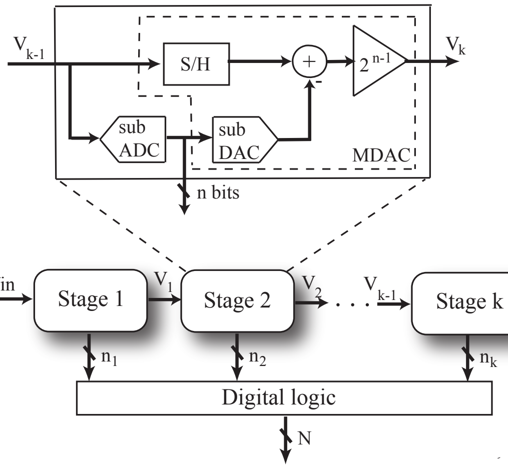


Figure 3.34: Architecture of a pipeline ADC.

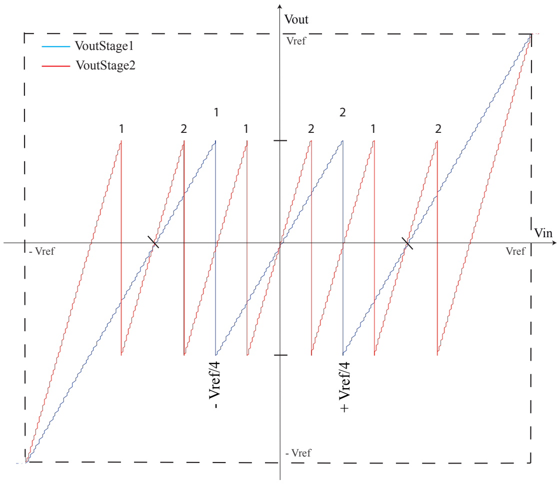


Figure 3.35: Residue of the first and second stages of a 1.5-bit/stage pipeline ADC.

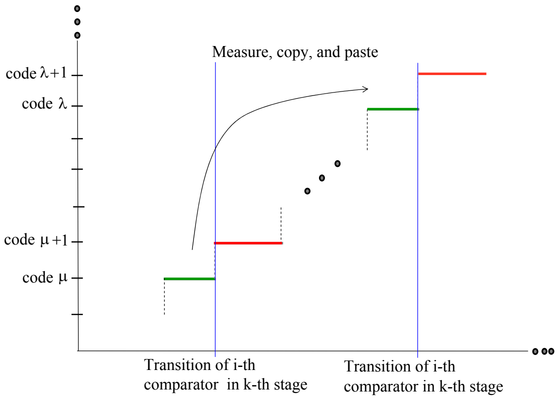


Figure 3.36: Principle of reduced code testing of pipeline ADCs.

Let us consider Fig. 3.35 which plots together the residues of the first and the second stages of a 1.5-bit/stage pipeline ADC. The sub-ADC in each stage is composed of two comparators. The number placed above the peak of a transition indicates which of the two comparators in the stage is being exercised (e.g. its threshold is crossed) at this transition. As it can be seen, if we traverse the input dynamic range of the ADC, the two comparators of the first stage are exercised once. The first, second, and third segment of the first stage residue traverse the output ranges $[-V_{ref}, V_{ref}/2]$, $[-V_{ref}/2, V_{ref}/2]$, and $[-V_{ref}/2, V_{ref}]$, respectively. Therefore, for each segment of the first stage residue, each of the two comparators of the second stage is exercised once, that is, if we traverse the input dynamic range of the ADC, then the two comparators of the second stage are exercised three times each in total. Following a similar argument, if we traverse the input dynamic range of the ADC, then the two comparators of the third stage are exercised seven times each.

The bottom line of the above discussion is that a comparator in a second or later pipeline stage is exercised several times. This implies that in the ADC output there will be transitions that are due to the same comparator. As an illustration, in Fig. 3.36 we show two transitions in the ADC output that are due to the i-th comparator in the k-th stage. An ADC output code shares two adjacent transitions that involve two different comparators in different stages of the pipeline. The DNL error, that is, the variation of the width of the code from the ideal one Least Significant Bit (LSB) width, is mainly due to the presence of different error sources in the comparator that belongs to the stage that is closer to the front of the pipeline. This is due to the fact that a stage in the pipeline dominates all subsequent stages in terms of the error produced in the transfer characteristic. In the example of Fig. 3.36, let us assume that the i-th comparator in the k-th stage dominates the comparators with which it shares codes μ, $\mu + 1$, λ, and $\lambda + 1$. This means that the width of these codes are principally affected by the errors due to process variations in the k-th stage where the i-th comparator belongs to. Furthermore, it means that the widths of the codes λ and $\lambda + 1$ are practically equal to the widths of the codes μ and $\mu + 1$, respectively. Thus, we need to measure the width of either λ or μ and the width of either $\lambda + 1$ or $\mu + 1$.

Extending this argument, let us assume that we know the mapping between the transitions in the ADC output and the comparators in the pipeline stage that are being exercised to produce these transitions. If we measure only the codes around a representative set of ADC output transitions such that this set covers all comparators in all stages and each comparator is represented once in this set, then, by relying on the mapping, we can readily assign values to the widths of unmeasured codes around the unselected ADC output transitions. In other words, we measure a reduced number of codes in the histogram and we fill in the rest of the histogram automatically by relying on the information in the extracted mapping. Relying on a reduced number of code width measurements to extract the complete transfer characteristic of the ADC translates in static test time reduction.

In order to make the reduced-code testing technique successful, we need to meet two objectives. First, we need to ensure that an ADC output transition is mapped to the correct comparator. This holds for all ADC output transitions, i.e. those that are selected and those that are not selected and their surrounding codes will be inferred later. Second, for a comparator in a given stage we should avoid selecting an output transition that involves in addition to this comparator a comparator in one of the previous stages. The reason is that the error of the previous stage will overshadow the error of the target stage. If the above two objectives are not met, then the accuracy of the technique degrades, resulting in an erroneous characterization of the static performances of the ADC.

To meet the aforementioned two objectives, the mapping is derived by monitoring the digital outputs of the internal stages of the pipeline before they undergo digital correction. The rationale is that when a comparator threshold is crossed it necessarily produces a transition in the digital output of the stage to which it belongs to. A transition in the digital output of a stage provides complete information about which comparator has been exercised. Furthermore, a transition in the digital output of a stage can be mapped to the resulting ADC output transition by simply processing the outputs of the different stages as is done by the digital logic block of the ADC.

However, the mapping can be affected by noise in the transitions of the digital outputs of the internal stages of the pipeline. We will define the concepts of natural and forced transitions and root codes. These concepts will be used next to develop an enhanced reduced-code linearity testing technique that is immune to noise.

Natural and forced transitions

Since we will be monitoring the digital outputs of each of the pipeline stages we need to list and label all possible transitions. We classify them into two types: *natural* transitions and *forced* transitions. Looking at the residue of the second stage VoutStage2 of a 1.5-bit/stage pipeline ADC shown in Fig. 3.37, we can observe the six transitions corresponding to the two comparators of this stage. By looking at the corresponding Vdac2 output, we can identify which of the two comparators is being exercised each time. We have indicated on the Vdac2 curve the corresponding digital output at each Vdac2 transition. The first comparator is exercised three times (e.g. transitions 00 → 01) and the second comparator is exercised also three times (e.g. transitions 01 → 10). We observe also that in addition to the transitions 00 → 01 and 01 → 10, there is another transition 10 → 00 happening twice. This transition happens under the influence of transitions in the residue of the first stage VoutStage1. The residue of the first stage becomes suddenly lower than the threshold

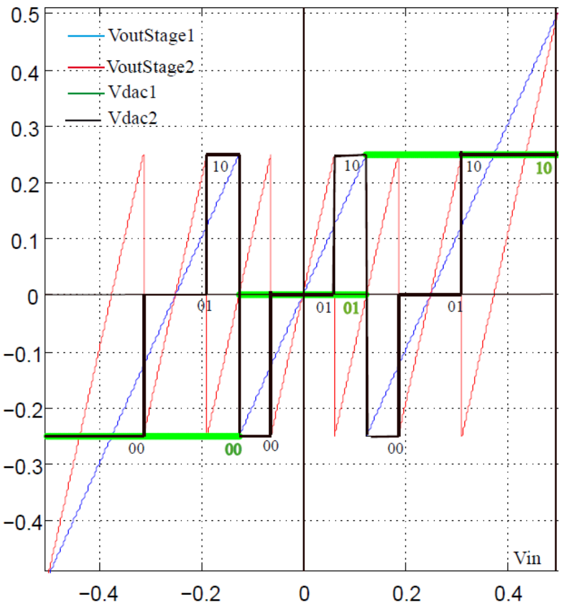


Figure 3.37: Residues of the first two stages of a 1.5-bit/stage pipeline ADC plotted together with the output of the sub-DAC.

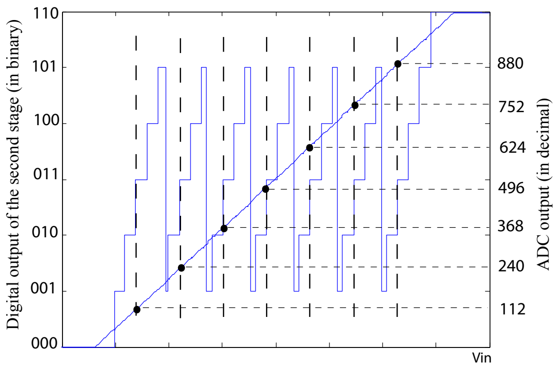


Figure 3.38: Transitions in the second stage and corresponding ADC output codes.

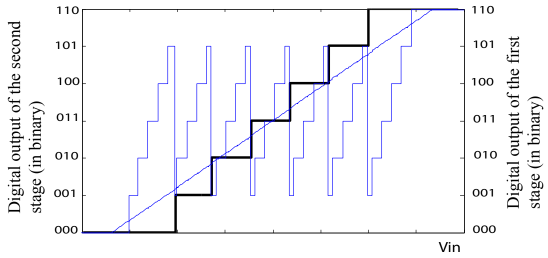


Figure 3.39: Transitions in the first and second stages.

of the second comparator in the second stage and, thus, the digital output of the second stage transitions from 10 to 00. We refer to these transitions as forced transitions because the digital output of the stage transitions due to a sudden change at its input which is caused due to one of the comparators of the previous stages being exercised. Conversely, when the digital output of the stage transitions due to a smooth change at its input causing one of the comparators in this stage to be exercised, we refer to these transitions as natural transitions.

Root codes

Let us consider a 10-bit ADC that comprises four 2.5-bit stages and a last 2-bit stage. Specifically, let us consider the third comparator in the second stage of this ADC. Fig. 3.38 superimposes the output of the ADC (right y-axis in decimal) on the digital output of the second stage (left y-axis in binary) as we traverse the whole dynamic range. From this plot we can identify the output codes of the ADC that are associated with the transitions from 010 to 011 of the second stage that are due to the third comparator in this stage being exercised. On the right y-axis of Fig. 3.38 we show the ADC output codes on the right of these transitions. As it can be seen from Fig. 3.39, the first ADC output code 112 corresponds to the case where the output of the first stage is 000, the second ADC output code 240 corresponds to the case where the output of the first stage is 001, the third ADC output code 368 corresponds to the case where the output of the first stage is 010, and so forth. All these ADC output codes can be derived from code 112 by adding a term that is obtained by multiplying the value in decimal of the output of the first stage with the weight of the first stage. In particular, considering that for this specific ADC the weight of the first stage is equal to 2^7, we can write: $112 = 112 + 0 \cdot 2^7$; $240 = 112 + 1 \cdot 2^7$; $368 = 112 + 2 \cdot 2^7$; $496 = 112 + 3 \cdot 2^7$; $624 = 112 + 4 \cdot 2^7$; $752 = 112 + 5 \cdot 2^7$; $880 = 112 + 6 \cdot 2^7$. We refer to the output code 112 as the *right root code* of the third comparator in the second stage. Similarly, by looking at the ADC output codes on the left of the transitions from 010 to 011 of the second stage that are due to the third comparator in this stage being exercised, we can define the *left root code* of the third comparator in the second stage.

To generalize, let us divide the ADC stages into two groups. The first group contains stages 1 to $k-1$ and the second group contains stages k to N, where N is the total number of stages. Let us also define a function $f(x, comp_k^i, w)$, where x refers to the rank of the stage in the pipeline, $comp_k^i$ refers to i-th comparator of the k-th stage, and w refers to the right side (e.g. $w = R$) or to the left side (e.g. $w = L$) of the transition of the digital output of the stage that is due to the comparator $comp_k^i$ being exercised. We define $f(x, comp_k^i, w)$ as follows. Given that the i-th comparator of the k-th stage is exercised producing a transition in the digital output of the x-th stage, $f(x, comp_k^i, w)$ is the digital output of the x-th stage on the w side of this transition. For example, $f(1, comp_2^3, R)$ refers to the digital output of the first stage on the right of a transition that is due to the third comparator of the second stage being exercised.

By definition, every time the i-th comparator in the k-th stage is exercised, the digital output of the k-th stage transitions from a value equal to $f(k, comp_k^i, L) = i-1$ to a value equal to $f(k, comp_k^i, R) = i$. Furthermore, every time the same comparator is exercised in a stage, the residue of this stage, which is the analog input to the following stages, always transitions between the same two values. This implies that every time the i-th comparator in the k-th stage is exercised, the digital output of the x-th stage, $x = k+1, \cdots, N$, is always equal to the value $f(x, comp_k^i, L)$ before the transition and equal to the value $f(x, comp_k^i, R)$ after the transition.

Let us now define

$$L_i^k = [f(k, comp_k^i, L), f(k+1, comp_k^i, L), \cdots, f(N, comp_k^i, L)] \tag{3.23}$$

$$R_i^k = [f(k, comp_k^i, R), f(k+1, comp_k^i, R), \cdots, f(N, comp_k^i, R)]. \tag{3.24}$$

If we sum up the elements of L_i^k respecting the weight of each stage, then we obtain the left root code of the i-th comparator in the k-th stage. If we sum up the elements of R_i^k respecting the weight of each stage, then we obtain the right root code of the i-th comparator in the k-th stage.

Noise cancellation through majority voting

We first apply a ramp and we observe the type of the transitions at the digital output of each stage. For each natural transition that is due to the i-th comparator in the k-th stage being exercised, we obtain L_i^k and R_i^k from Eq. (3.23) and (3.24). If n is the number of natural transitions, then we have at hand n values of each element $f(x, comp_k^i, L)$ of L_i^k and n values of each element $f(x, comp_k^i, R)$ of R_i^k, $x = k, \cdots, N$. Due to the presence of noise, these n extracted values are not necessarily the same for $x = k+1, \cdots, N$. In other words, the left and right root codes calculated starting from different natural transitions may not be the same.

For $x = k+1, \cdots, N$, let $\mu_{comp_k^i}^{x,L}$ and $\mu_{comp_k^i}^{x,R}$ be the values of $f(x, comp_k^i, L)$ and $f(x, comp_k^i, R)$, respectively, that are most frequently met in the n values that we have at hand. In this way, by applying a majority voting scheme, we obtain the noise-free L_i^k and R_i^k as follows:

$$L_i^k = [i-1, \mu_{comp_k^i}^{k+1,L}, \cdots, \mu_{comp_k^i}^{N,L}] \tag{3.25}$$

$$R_i^k = [i, \mu_{comp_k^i}^{k+1,R}, \cdots, \mu_{comp_k^i}^{N,R}]. \tag{3.26}$$

From the noise free L_i^k and R_i^k we can calculate the noise-free left and right root codes of the i-th comparator in the k-th stage.

Obtaining the mapping

To obtain the mapping, we only need (a) the noise-free L_i^k and R_i^k for each of the comparators and (b) the value of the digital output of each stage at the beginning of the dynamic range, denoted by

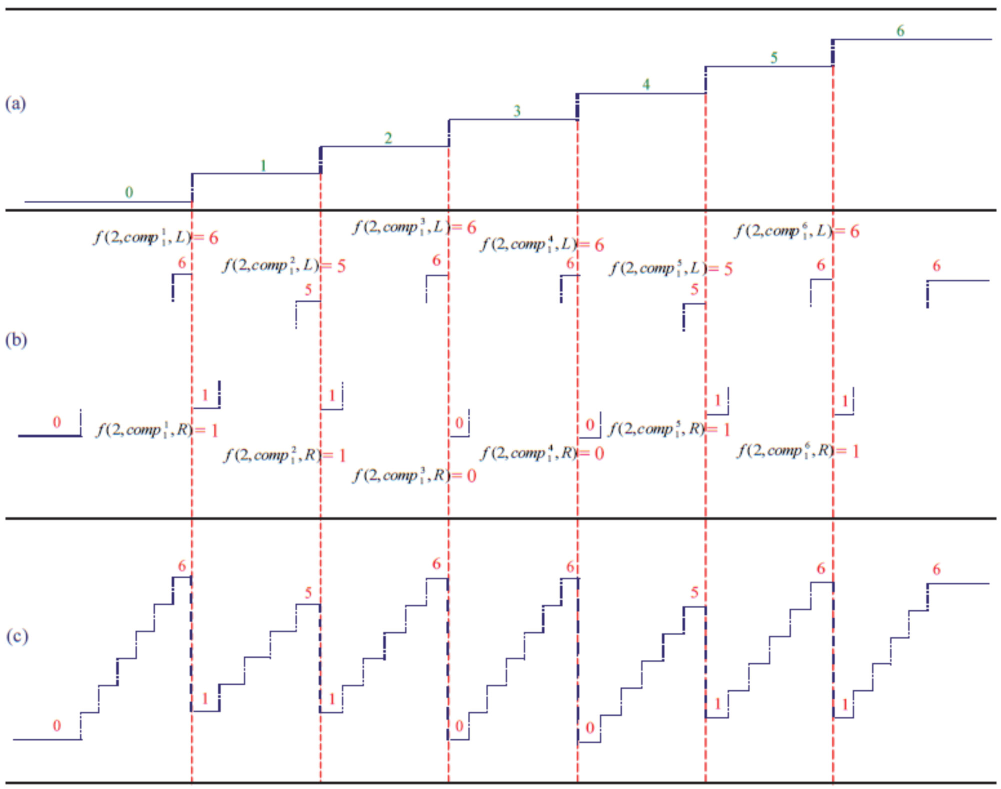


Figure 3.40: Reconstructing the digital output of the second stage using $L_i^1(2)$ and $R_i^1(2)$.

$Out_{k,start}$, and at the end of the dynamic range, denoted by $Out_{k,end}$, where k denotes the number of the stage, $k = 1, \cdots, N$. $Out_{k,start}$ and $Out_{k,end}$ are straightforward to obtain. In decimal, $Out_{k,start} = 0$ for each stage and $Out_{k,start} = 2^B - 2$, where B is the number of output bits of the k-th stage unless considerable offsets are present in the ADC. For example, $B = 2$ for an 1.5-bit stage, $B = 3$ for a 2.5-bit stage, etc. In the following, we will assume that $Out_{k,start} = 0$ and $Out_{k,end} = 2^B - 2$.

By looking at the digital output of any stage as we traverse the input dynamic range (for example, see Fig. 3.38 and Fig. 3.39), we observe that it starts at $Out_{k,start}$ and it ends at $Out_{k,end}$ with natural or forced transitions occurring in between. Fig. 3.40(a) shows the typical digital output of a first 2.5-bit stage. It starts at $Out_{1,start} = 0$, ramping up to $Out_{1,end} = 6$, with the natural transitions of its six comparators occurring in between. Another example is given in Fig. 3.39. Notice that any transition in the digital output of a first stage is a natural transition.

In contrast, a transition in the digital output of a second or later stage could be either natural or forced. As shown in the example of Fig. 3.38, the digital output of a second 2.5-bit stage starts at $Out_{2,start} = 0$ and ends at $Out_{2,end} = 6$, with both natural and forced transitions occurring in between. The forced transitions are due to the natural transitions of the first stage and the natural transitions occur between every two successive forced transitions. The first forced transition of the second stage is due to the first natural transition of the first stage. The value of the digital output of the second stage to the left and to the right of its first forced transition are given by $f(2, comp_1^1, L)$ and $f(2, comp_1^1, R)$, respectively, as shown in Fig. 3.40(b). The second forced transition of the second stage due to the second natural transition of the first stage is a transition from $f(2, comp_1^2, L)$ to $f(2, comp_1^2, R)$, the third forced transition of the second stage due to the third natural transition of the first stage is a transition from $f(2, comp_1^3, L)$ to $f(2, comp_1^3, R)$, and so forth. The digital output values of the second stage between $Out_{2,start}$ and $f(2, comp_1^2, L)$, between $f(2, comp_1^i, R)$ and $f(2, comp_1^{i+1}, L)$, for $2 \leq i \leq 5$, and finally between $f(2, comp_1^6, R)$ and $Out_{2,end}$, will be obtained by simply incrementing $Out_{2,start}$ by 1 until $f(2, comp_1^2, L)$, incrementing $f(2, comp_1^i, R)$ by 1 until $f(2, comp_1^{i+1}, L)$, for $2 \leq i \leq 5$, and finally incrementing $f(2, comp_1^6, R)$ by 1 until $Out_{2,end}$. Between these values the comparators of the second stage are exercised one after the other, incrementing the digital output of the stage by 1.

Similarly, the digital output of the third stage can be reconstructed from the digital output of the second stage based solely on $Out_{3,start}$, $Out_{3,end}$, $f(3, comp_2^i, L)$, $f(3, comp_2^i, R)$, $f(3, comp_1^i, L)$, and $f(3, comp_1^i, R)$. $f(3, comp_2^i, L)$ and $f(3, comp_2^i, R)$ are used to account for the forced transitions of the third stage due to the natural transitions of the second stage while $f(3, comp_1^i, L)$ and $f(3, comp_1^i, R)$ are used to account for the forced transitions of the third stage due to the natural transitions of the first stage.

Following the same argument, based on the elements of the noise-free L_i^k and R_i^k, we can reconstruct the digital output of each stage from the digital outputs of the preceding stages in the pipeline. In this way, with a single sweep of the input dynamic range, we can identify the transitions in digital outputs of each stage and, then, juxtapose them with the ADC digital output to find the mapping. An algorithm based on nested *for loops* can be used for this purpose, starting from the first stage down to the last stage of the ADC, and recording the required mapping information in the course of the algorithm.

3.6.2 Results

Our case study is a 55nm 11-bit pipeline ADC with digital correction provided by ST Microlectronics. The ADC is composed of four 2.5-bit stages and a last 3-bit stage. The reduced-code testing technique with and without cancellation is compared to the standard histogram test. It should be noticed that the reduced-code testing technique relies only on 132 out of 2046 codes of the ADC, that is, on only 6% of the codes, which represents a very significant static test time reduction.

The DNL obtained using the standard histogram technique is shown in Fig. 3.41(a) while the estimated DNL using the reduced-code testing technique without and with noise cancellation is shown, respectively, in Fig. 3.41(b) and 3.41(c). The estimated profiles of DNL in Fig. 3.41(b) and 3.41(c) are more regular since they are extracted from the DNLs of a reduced set of codes. The highest DNL errors in the ADC correspond to the first stages in which the transitions are not so noisy. Thus, the minimum and maximum DNLs are well captured regardless whether noise cancellation is used or not. However, when comparing the profile of the smaller absolute DNLs in Fig. 3.41(b) and Fig. 3.41(c) with the profile of the smaller absolute DNLs in Fig. 3.41(a), we observe that the profile in Fig. 3.41(b) is less "dense" as opposed to the profile in Fig. 3.41(c), which implies that there are many codes that have been assigned smaller absolute DNL values. This implies that, unless noise cancelling is used, there are significant errors in the mapping between the ADC output transitions and the comparators that are being exercised in the case where the comparators belong to stages that are towards the end of the pipeline.

The INL obtained using the standard histogram technique is shown in Fig. 3.42(a) while the estimated INL using the reduced-code testing technique without and with noise cancellation is shown, respectively, in Fig. 3.42(b) and 3.42(c). The inset plots in 3.42(b) and 3.42(c) show a zoom of the estimated INL profiles superimposed on INL profile obtained using the standard histogram technique. From Fig. 3.42(c) it is evident that the reduced-code testing technique with noise cancellation offers an excellent INL estimation, implying that we are summing up a succession of well estimated DNLs despite the noise in the ADC output transitions. In fact, the estimated INL is practically indistinguishable from the INL obtained with the standard histogram technique. In contrast, from Fig. 3.42(b) it is evident that the reduced-code testing technique without noise cancellation, although is capable of capturing the general INL profile, results in evident INL errors due to summing up a succession of poorly estimated DNLs. The general INL profile is captured thanks to the high peaks of DNL. In the case of an ADC with small DNL errors, the reduced-code

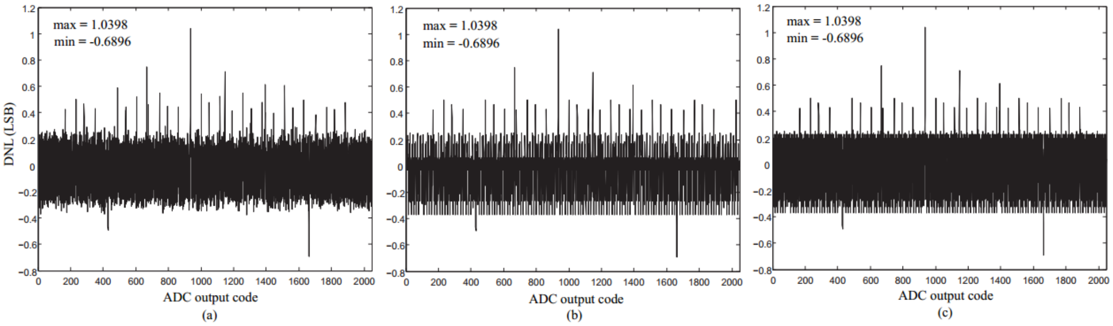


Figure 3.41: DNL obtained with: (a) standard histogram technique; (b) reduced-code testing without noise cancelling; and (c) reduced-code testing with noise cancelling.

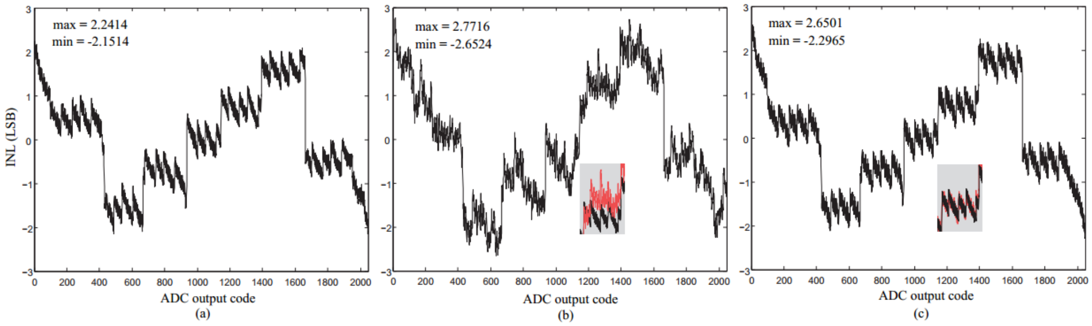


Figure 3.42: INL obtained with: (a) standard histogram technique; (b) reduced-code testing without noise cancelling; and (c) reduced-code testing with noise cancelling.

testing technique without noise cancellation would have failed to capture even the general INL profile. In contrast, if noise cancellation is used, the INL estimation will be excellent independently of the DNL values of the ADC and the level of noise in the measurement environment.

3.7 Neuromorphic Built-In Self-Test

In Chapter 2, we discussed the idea of training a classifier in the space of low-cost alternative measurements, in order to execute a go/no-go test. In this work, we explore the possibility of integrating a hardware version of a neural network classifier along with the CUT, in order to execute a go/no-go built-in test [156]. In particular, the classifier can replace the off-chip extraction and post-processing of measurements since it compacts the measurements to a binary go/no-go test response. A true BIST is possible if the test stimuli are also generated on-chip. Such a stand-alone BIST can then be performed on-line in the field of operation, in order to detect malfunctions due to environmental impact and aging.

3.7.1 Architecture

The envisioned neuromorphic BIST architecture is illustrated in Fig. 3.43. In an off-line training phase, the neural network classifier learns to map a measurement pattern to an 1-bit output, which indicates whether this measurement pattern is a valid or invalid code-word, that is, whether the CUT complies to its specifications or not. Training is carried out on a sample set of fabricated chips, which is enhanced if necessary with synthetic data using the technique in [47]. The training phase results in an appropriate topology for the neural network and it also determines the weights

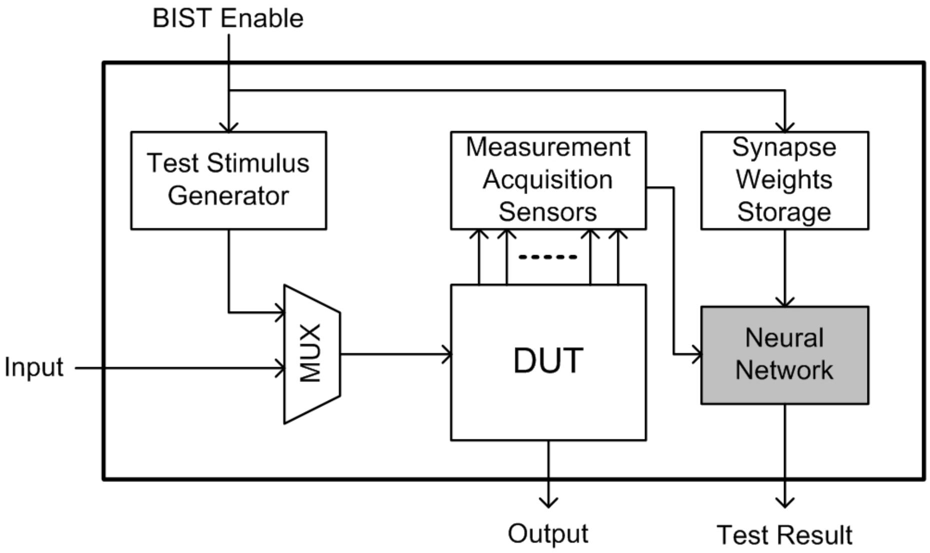


Figure 3.43: Neuromorphic BIST architecture.

of the internal synapses which are stored in a local memory. During the test phase, the weights are downloaded to the neural network. Next, the CUT is connected to the stimulus generator which enables a self-excitation of the CUT. The on-chip sensors monitor the CUT and provide the measurement pattern which is presented to the neural network. The neural network classifies the CUT by processing the measurement pattern and examining its footprint with respect to the learned classification boundary.

This approach presents a number of challenges. More specifically, the peripheral circuits that are dedicated to test should (a) incur low area overhead to minimize the extra die size cost (this would also imply a lower probability of fault occurrence within the test circuitry); (b) be non-intrusive, that is, they should have minimal interference with the CUT; (c) be more insensitive to process, voltage, and temperature (PVT) variations than the CUT itself; (d) make a prudent use of external pins; and (e) consume low power (this is crucial only for concurrent test or when test needs to be performed in the field in frequent idle times). Assuming that the above objectives are met, the overall success of this approach depends on the separation of the footprints of faulty and functional circuits when they are projected in the space that is formed by the selected measurements.

The scope of this work is to demonstrate a hardware neural network classifier that can learn an optimal non-linear classification boundary given a selected measurement pattern.

3.7.2 Hardware Neural Network

Neural networks have an appealing silicon implementation [157–160]. Synapses and computational elements can be densely interconnected to achieve high parallel distributed processing ability, which enables them to successfully solve complex cognitive tasks. Neural networks also provide a high degree of robustness and fault tolerance since they comprise numerous nodes that are locally connected, distributing knowledge among the numerous synapses. Thus, intuitively, damage to a few nodes does not impair performance. We are interested primarily in analog implementations of neural networks as, in comparison to a digital implementation, they have superior time response and computational density in terms of silicon mm^2 per operations per second and, in addition, they consume extremely low power.

The chosen model for the classifier is a 2-layer feed-forward neural network, as shown in Fig. 3.44. Each unit in this network is a linear perceptron which has a simple mathematical model, as shown in Fig. 3.45. A synapse can be considered as a multiplier of an input signal value by the stored

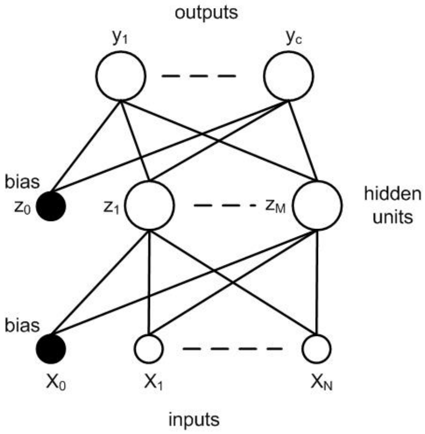


Figure 3.44: 2-layer network diagram.

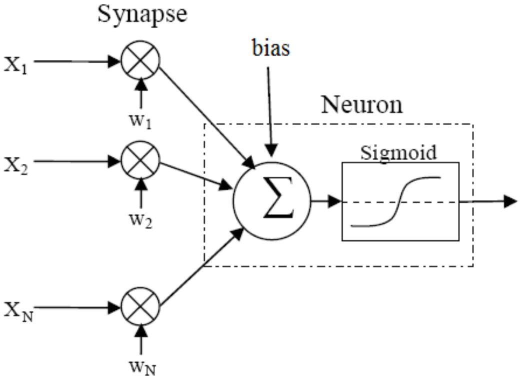


Figure 3.45: Linear perceptron.

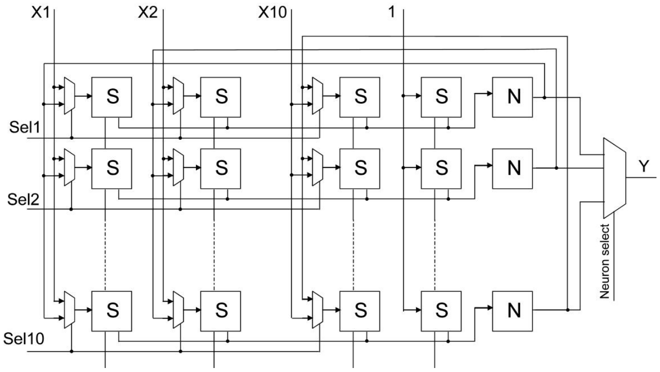


Figure 3.46: Reconfigurable neural network architecture.

weight value. A neuron sums the output values of the connected synapses and passes the resulting sum through a nonlinear sigmoid activation function

$$g(\alpha) = \frac{1}{1+\mathrm{e}^{-\alpha}}. \tag{3.27}$$

An explicit expression for the complete function represented by the diagram of Fig. 3.44 is

$$y_k = g\left(\sum_{i=0}^{M} w_{ki}^{(2)} z_i\right) \tag{3.28}$$

$$z_i = g\left(\sum_{j=0}^{N} w_{ij}^{(1)} X_j\right), \tag{3.29}$$

where $w_{ij}^{(k)}$ denotes the weight of input j for unit i in layer k and $w_{i0}^{(k)}$ denotes the bias for unit i in layer k. Such a neural network with 2 layers is capable of approximating any continuous functional mapping and can separate an arbitrary dichotomy (e.g. a given set of data points which have been labeled as belonging to one of two classes).

Fig. 3.46 illustrates the block-level schematic of a circuit implementation of a 2-layer neural network that can be reconfigured into any one-hidden-layer topology within the given number of inputs and neurons. The circuit consists of a matrix of synaptic blocks (S) and neurons (N).

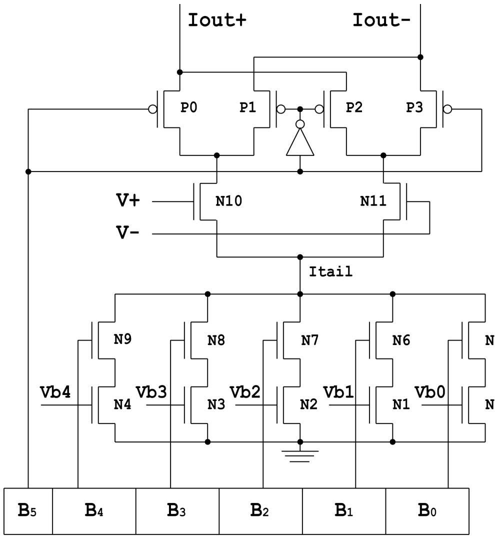


Figure 3.47: Synapse circuit schematic.

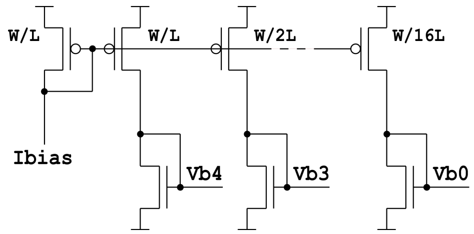


Figure 3.48: Current sources control circuit.

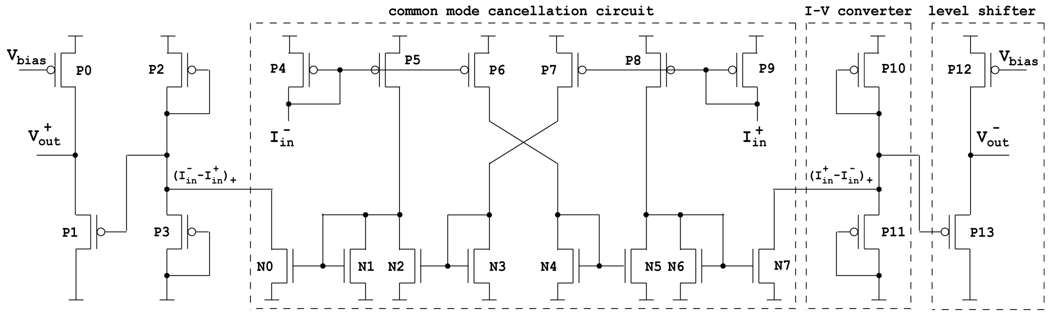


Figure 3.49: Neuron circuit schematic.

The synapses represent mixed-signal devices, in the sense that they conduct all computations in analog form while their weights are implemented as digital words stored in a local RAM memory. Multiplexers before each synapse are used to program the source of its input: either the primary input (for the hidden layer) or the output of a hidden unit (for the output layer). The results of synapse multiplication are summed and fed to the corresponding neuron, which performs a squashing function and produces an output either to the next layer or the primary output. The architecture is very modular and can easily be expanded to any number of neurons and inputs within the available silicon area. Therefore, the efficient implementation of the synapse and neuron circuits is essential for large networks. The output multiplexer is introduced to reduce the number of pins and ADCs. The signal encoding takes different forms: the outputs of the neurons are voltages, while the outputs of the synapses are currents. In addition, all signals are in differential form, thereby increasing the input range and improving noise resilience.

The basic function of a synapse is multiplication. The synapse circuit chosen for this design is a simple multiplying DAC [161], which represents a differential pair with programmable tail current, as shown in Fig. 3.47. A differential input voltage is multiplied by the tail current producing a differential output current which is collected on the summing nodes common to all synapses connected to each neuron. The tail current as a function of a digital weight word (bits $B4 - B0$) can be represented by

$$I_{tail} = \sum_{i=0}^{4} B_i \cdot I_i = \sum_{i=0}^{4} B_i \cdot I_{bias} \cdot 2^{i-4} = I_{bias} \cdot W, \tag{3.30}$$

where B_i are the bits of a weight word, I_i is the current corresponding to the i-th bit, I_{bias} is the external biasing current, and W is the weight value. The biasing voltages Vb_i for the current sources of all synapses are supplied by a single biasing circuit shown in Fig. 3.48. The external biasing current I_{bias} sets the most significant bit (MSB) current component, while the other currents are generated internally using the ratioed current mirrors. The differential output current is given by

$$\Delta I_{out} = K_N \Delta V_{in} \sqrt{\frac{I_{bias} W}{K_N} - (\Delta V_{in})^2}, \tag{3.31}$$

where ΔV_{in} is the differential input voltage and K_N is the transconductance coefficient. Linear multiplication is only valid for a narrow range of differential input voltages.

The main function of a neuron circuit is to convert the sum of differential currents from its synapses into a differential voltage. Two issues need to be taken into account when designing this circuit. First, if the output voltage is propagated to the next layer, it should be compatible with the input requirements of the synapses, i.e. it should have high common mode. Second, the circuit should handle relatively large dynamic range of input currents. While the useful information is contained in the difference, the common mode current may vary significantly depending on the number of connected synapses, as well as on their weight values. A circuit satisfying these requirements is shown in Fig. 3.49. The central part of the circuit is responsible for common mode cancellation by subtracting the input currents from each other and producing a positive difference. The second stage is a simple current-to-voltage converter. It can be shown that, when the transistors are identical, such circuit that exhibits a linear to the first degree characteristic of the following form

$$V = V_{dd} - \frac{I}{2K_P(V_{dd} - 2V_{TP})}, \tag{3.32}$$

where K_P is the transconductance coefficient, V_{TP} is the threshold voltage, and V_{dd} is the supply voltage. The circuit also provides a limiting function when the input current exceeds the internal current flowing through the circuit, thus introducing nonlinearity to the neuron characteristic. Finally, the output of the converter is shifted upwards to meet the requirements of the high common mode input voltage for the synapses in the following layer. This level shifter is a simple source follower circuit where the amount of shift is controlled by V_{bias}.

3.7.3 Training

We employed a popular training algorithm called parallel stochastic weight perturbation [162]. In this algorithm, all weights are perturbed simultaneously by a random vector. Then the mean squared error is evaluated on the entire training set. If the error decreases, the new vector of weights is accepted; otherwise, it is discarded. This algorithm, however, suffers from high likelihood of convergence to a local minimum. Thus, training may need to be performed several times before a good solution is found. To decrease the probability of being stuck in a local minimum, this algorithm has been augmented with the simulated annealing technique, which is known to be efficient in avoiding local minima since it allows the state of the network to move “uphill”. The main difference from the original algorithm consists in its ability to accept weight changes resulting in an increase of the error, however, with a certain probability. This probability depends on the magnitude of the error change and the “temperature” of the system T, i.e. $p \simeq \exp(-\Delta E/T)$. Higher temperatures at the initial stages favor the exploration of the whole search space. A cooling schedule is used to adjust the temperature and magnitude of weight perturbations as the training progresses.

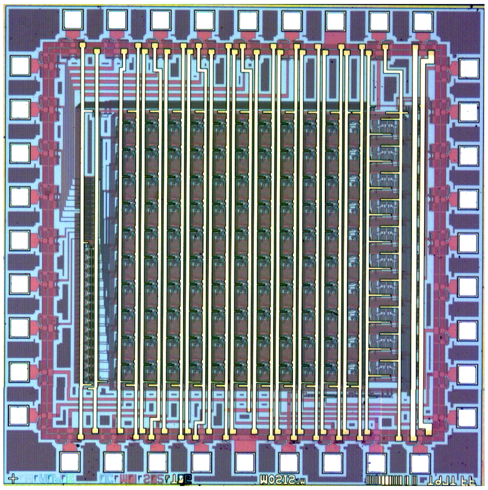


Figure 3.50: Chip photograph.

Table 3.1: Chip key features.

Implementation method	mixed-signal
Network topology	reconfigurable 2-layer
IC process	0.5 μm CMOS
Core area	$1 \times 1.2\ mm^2$
Neurons	10
Synapses	100
Weight resolution	6 bit
Response time	$<\ 1\ ms$
Power supply	3.3 V
Max. current per synapse	3 μA

3.7.4 Results

The analog neural network classifier has been designed as a single chip. The chip has been fabricated using a 0.5 μm digital CMOS process available through MOSIS. Fig. 3.50 shows a photograph of the chip and Table 3.1 summarizes its key features. The chip is put to the test to learn to classify RF low noise amplifier (LNA) instances based on a built-in test measurement pattern. This pattern is obtained by exercising the LNA with two single-tone sinusoidal stimuli of different powers and by recording the outputs of two amplitude (or peak or power) detectors that are placed at the input and output ports of the LNA [32]. A set of 1000 LNA instances reflecting manufacturing process variations is generated through a Monte Carlo post-layout simulation. Then, the non-parametric density estimation technique described in Section 4.2.2 is used [47], in order to generate a balanced synthetic training set of LNA instances of which 1/3 are faulty, 1/3 are marginally functional, and 1/3 are functional close to the nominal design. In this way, the classification boundary can be better approximated since the area around it is populated with many samples. In Fig. 3.51, the training set is projected in a 2-dimensional measurement space. The decision boundary is generated by the hardware classifier. Notice that this training set is “biased” in the sense that it is enhanced with a large number of faulty LNA instances. In contrast, the trained classifier is validated using an unbiased random set of 1 million LNA instances validation set of devices also generated by the non-parametric density estimation technique [47]. Fig. 3.52 illustrates the original set of 1000 LNA instances together with 10^4 randomly generated synthetic LNA instances.

We experiment with three different neural network configurations that consist of a single hidden layer with 2, 4, and 8 neurons, respectively. For comparison purposes, the same experiments are

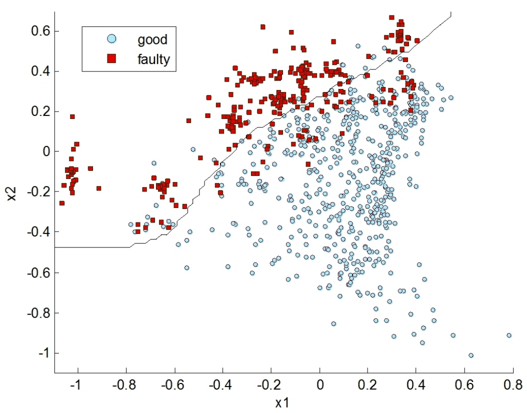


Figure 3.51: Balanced synthetic training set.

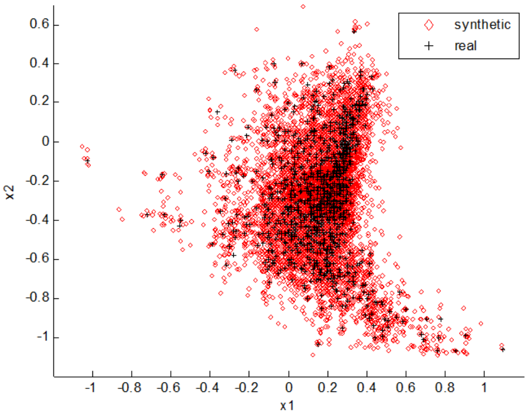


Figure 3.52: Random synthetic validation set.

Table 3.2: Classifier performance.

Number of hidden neurons	2	4	8
Software network			
Training error, %	5.82	4.91	4.88
Validation error, %	0.566	0.548	0.581
Hardware network			
Training error, %	6.82	5.53	5.75
Validation error, %	0.727	0.435	0.491

repeated with software neural networks of identical topologies using the MATLAB Neural Networks toolbox.

The results on the training and validation sets are presented in Table 3.2. A large discrepancy between the training and validation errors is the result of having a "biased" training set with many faulty and marginal devices and a "natural" validation set where the majority of devices is distributed around the nominal point. In terms of training error, the software classifier consistently outperforms the hardware classifier by about 1%. However, the validation errors, representing the true accuracy of classification, are similar for both networks (the difference is $< 0.2\%$). The hardware version achieves even smaller error for the models with more than 2 hidden neurons. In fact, the best performance is shown by the hardware network with 4 hidden neurons resulting in the error of 0.435%.

3.8 Conclusion

In this Chapter, we presented low-overhead integrated test techniques for RF circuits and two classes of ADCs, namely $\Sigma\Delta$ and pipeline. The key property of the integrated test techniques for RF circuits is that they are non-intrusive dissociating the design from the test. The key property of the integrated test technique for $\Sigma\Delta$ ADCs is that it is fully digital allowing a robust implementation. The key property of the integrated test technique for pipeline ADCs is that it exploits inherent properties of their architecture offering the greatest static test cost reduction possible. Finally, we presented a generic neuromorphic BIST architecture that employs an on-chip neural network to process low-cost measurements and make go/no-go test decisions.

Chapter 4

Test metrics estimation

4.1 Introduction

To alleviate the burden of standard specification-based testing, it is required to replace some, if not all, specification-based tests by lower cost alternative tests. To this end, researchers and test practitioners are continuously proposing new ideas, including defect-based tests, built-in self-test (BIST), machine learning-based tests, etc. Yet, these intensified efforts have not been met with success due to the difficulty in corroborating the claim that an alternative test approach is equivalent to the standard specification-based testing.

Specifically, consider a set of alternative tests $\mathbf{T} = [T_1, \cdots, T_{n_t}]$ and suppose that it is a promising candidate to replace a set of costly specification-based tests that target a set of performances $\mathbf{P} = [P_1, \cdots, P_{n_p}]$. In particular, there is strong evidence that $\mathbf{T}$ correlates well with $\mathbf{P}$ and, in addition, $\mathbf{T}$ incurs low direct costs, i.e. it is fast, it requires low cost test instrumentation, low overhead Design for Testability (DfT), etc. To ensure that $\mathbf{T}$ is indeed a palatable choice, we also need to estimate its test metrics, i.e. the probability that a faulty circuit will pass all tests in $\mathbf{T}$ and will be shipped to the customer (e.g. test escape), as well as the probability that a functional circuit will fail one of the tests in $\mathbf{T}$ and will be discarded (e.g. yield loss). Test escapes and yield loss correspond to indirect costs, which can easily wipe out the seeming cost reduction from introducing $\mathbf{T}$ in place of $\mathbf{P}$.

A possible solution for test metrics estimation is to insert $\mathbf{T}$ in the production test suite and to keep measuring both $\mathbf{T}$ and $\mathbf{P}$ for a large number of fabricated circuits, until we reach a conclusion whether $\mathbf{T}$ and $\mathbf{P}$ are equivalent in terms of test accuracy. If the conclusion is affirmative, then we can replace $\mathbf{P}$ by $\mathbf{T}$, thus dropping the test cost for future circuits. However, in the opposite scenario, despite our initial objective, the cost of test increased for a significant period of time during the characterization of $\mathbf{T}$, not to mention the waste of DfT provisions on chip that were possibly taken for measuring $\mathbf{T}$. Therefore, it is necessary to estimate the test metrics of $\mathbf{T}$ during the test development phase through simulation. Ideally, we would like to replace $\mathbf{P}$ with $\mathbf{T}$ right at the onset of production.

Test metrics are defined probabilistically. Let the circuit be designed such that P_i lies within the desired specification limits $s^i = (s^i_\ell, s^i_u)$, $i = 1, \cdots, n_p$, that is, the performance acceptability region is $A_P = [s^1_\ell, s^1_u] \times \cdots \times [s^{n_p}_\ell, s^{n_p}_u]$. Let also the circuit pass the alternative test T_i if T_i lies within the test limits $t^i = (t^i_\ell, t^i_u)$, $i = 1, \cdots, n_t$, that is, the test acceptability region is $A_T = [t^1_\ell, t^1_u] \times \cdots \times [t^{n_t}_\ell, t^{n_t}_u]$. Formally, test escape, denoted by T_E, and yield loss, denoted by Y_L are defined as follows

$$\begin{aligned} T_E &= \Pr\{\mathbf{P} \notin A_P | \mathbf{T} \in A_T\} && (4.1) \\ Y_L &= \Pr\{\mathbf{T} \notin A_T | \mathbf{P} \in A_P\}. && (4.2) \end{aligned}$$

Notice that the computation of T_E assumes the definition of a *fault model.* Broadly speaking, the faulty behavior of a circuit can be due to two reasons: 1) defects in manufacturing that translate into topological changes in the form of short- and open-circuits and 2) variations in the process parameters, which we refer to as *parametric faults*.

Regarding circuits with defects, assuming the availability of a fault model that includes a list of probable defects, T_E can be expressed as the percentage of non-detected defects. Such a fault model can be developed based on defect statistics and inductive fault analysis [163–166]. The design of the simulation campaign to evaluate T_E is straightforward, however, in the case where the number of defects is too high, sophisticated defect sampling techniques must be used [167]. This definition of T_E is used to assess defect-oriented test techniques [168–170], which can be applied for wafer-level testing to detect dies with gross defects or for final testing of robust designs that are highly unlikely to fail due to process variations.

Regarding circuits with process variations, the computation of T_E is not as straightforward since the definition of a fault model that accounts for parametric faults poses a great challenge [171]. Previous proposals for parametric fault modeling made certain assumptions to be able to deal with the simulation burden [172–175]. The widespread approach has been to build a parametric fault model at a higher level of abstraction, for example, by modeling faults as variations in passive components and in transistor parameters, i.e. transconductance, geometry, oxide thickness, threshold voltage, etc., or by considering behavioral simulation instead of transistor-level simulation and modeling faults as variations in the parameters of the behavioral model. Furthermore, a common assumption is that parameters vary independently, which is known as single fault assumption, and that a circuit fails a specification when one parameter exceeds a specific tolerance. These simplified fault models make simulation more traceable, yet their ability to capture correctly faulty behavior due to process variations has never been proven.

The “natural” approach to compute T_E and Y_L for circuits with process variations, which we refer to as *parametric test metrics*, would be to perform a Monte Carlo circuit simulation. However, for robust designs with specifications set to 3σ or higher, T_E and Y_L are rare events and, by default, a Monte Carlo circuit simulation samples with priority the statistically likely cases. This implies that we may not encounter any such rare events in a practical Monte Carlo circuit simulation. In fact, if T_E and Y_L are in the order of a few hundred parts per million (ppm), then for their accurate estimation we would require an untraceable number of simulations of a few millions.

In this chapter, we present fast statistical simulation methods based on density estimation, statistical blockade, and extreme value theory, which can be readily used in the context of parametric test metrics estimation. Other relevant fast statistical simulation methods in this context that are not discussed herein include regression modeling [68] and importance sampling [176].

4.2 Density estimation

The estimation of T_E and Y_L are equivalent from a mathematical point of view. Herein, without loss of generality, we consider the estimation of T_E in (4.1).

Let $\mathbf{X} = [\mathbf{P}, \mathbf{T}] = [X_1, X_2, \cdots, X_d]$ be the d-dimensional random vector that comprises the performances and alternative tests, $d = n_p + n_t$, and let $f_{\mathbf{X}}(\mathbf{x})$ denote the joint probability density function of $\mathbf{X}$. From (4.1) we can write

$$T_E = \frac{\Pr\{\mathbf{P} \notin A_P, \mathbf{T} \in A_T\}}{\Pr\{\mathbf{T} \in A_T\}}. \tag{4.3}$$

Using the indicator functions

$$I_1(\mathbf{P}, \mathbf{T}) = \begin{cases} 1 & : \quad \mathbf{P} \notin A_P, \mathbf{T} \in A_T \\ 0 & : \quad \text{otherwise} \end{cases} \tag{4.4}$$

$$I_2(\mathbf{P},\mathbf{T}) = \begin{cases} 1 & : \quad \mathbf{T} \in A_T \\ 0 & : \quad \text{otherwise} \end{cases}, \tag{4.5}$$

(4.3) becomes

$$T_E = \frac{\int_{\Re^d} I_1(\mathbf{P},\mathbf{T}) f_{\mathbf{X}}(\mathbf{x}) d\mathbf{x}}{\int_{\Re^d} I_2(\mathbf{P},\mathbf{T}) f_{\mathbf{X}}(\mathbf{x}) d\mathbf{x}}. \tag{4.6}$$

If $\hat{f}_{\mathbf{X}}(\mathbf{x})$ is an estimate of the density $f_{\mathbf{X}}(\mathbf{x})$, then an estimate of T_E is obtained as

$$\hat{T}_E = \frac{\int_{\Re^d} I_1(\mathbf{P},\mathbf{T}) \hat{f}_{\mathbf{X}}(\mathbf{x}) dx}{\int_{\Re^d} I_2(\mathbf{P},\mathbf{T}) \hat{f}_{\mathbf{X}}(\mathbf{x}) d\mathbf{x}}. \tag{4.7}$$

The density estimation approach consists of simulating $N \gg 1$ observations $\mathbf{X}^j = [\mathbf{P}^j, \mathbf{T}^j]$ of $\mathbf{X}$ from the density $\hat{f}_{\mathbf{X}}(\mathbf{x})$ and calculating the indicator functions I_1 and I_2 on each observation. Then, an estimate of T_E is obtained as

$$\hat{T}_E = \frac{\sum_{j=1}^{N} I_1(\mathbf{P}^j, \mathbf{T}^j)}{\sum_{j=1}^{N} I_2(\mathbf{P}^j, \mathbf{T}^j)}. \tag{4.8}$$

4.2.1 Multinormal density

The most straightforward approach is to assume that $f_{\mathbf{X}}(\mathbf{x})$ is Gaussian [177] with $d \times 1$ mean vector μ and $d \times d$ covariance matrix Σ, i.e.

$$\hat{f}_{\mathbf{X}}(\mathbf{x}) = \frac{1}{(2\pi)^{\frac{1}{d}} |\Sigma|^{\frac{1}{2}}} e^{-\frac{1}{2}(\mathbf{x}-\mu)^T \Sigma^{-1} (\mathbf{x}-\mu)}. \tag{4.9}$$

The mean vector and the covariance matrix are estimated based on data from an initial Monte Carlo circuit-level simulation with n runs that we can afford. A new sample from $\hat{f}_{\mathbf{X}}(\mathbf{x})$ can be generated as

$$\mathbf{X} = \mu + A\mathbf{W}, \tag{4.10}$$

where A is the Cholesky decomposition of the covariance matrix Σ and $\mathbf{W}$ is a $d \times 1$ vector whose components are independent random samples of the univariate standard normal distribution.

4.2.2 Non-parametric density

The non-parametric kernel density estimation approach, described in details in Section 2.2.2, revokes the normality hypothesis and can be applied regardless of the parametric form of $f_{\mathbf{X}}$, i.e. even when the marginal distributions of $f_{\mathbf{X}}$ have distinct parametric forms resulting in an undocumented form for $f_{\mathbf{X}}$ [47,178,179]. It can be shown that $\hat{f}_{\mathbf{X}}(\mathbf{x}, \alpha) \to f_{\mathbf{X}}(\mathbf{x})$ in probability as $n \to \infty$ provided that the selected bandwidth satisfies $h \to 0$ and $nh \to \infty$ as $n \to \infty$ [56]. The choice of the bandwidth in (2.2) is made following an approach known as rule-of-thumb [56] and satisfies these conditions.

A new sample $\mathbf{X}$ can be generated as follows:

Step 1 Consider an observation $\mathbf{X}^I$ with I chosen from $\{1, ..., n\}$ uniformly at random.

Step 2 Generate $\mathbf{v}$ to have probability density function $K_e(\mathbf{v})$ in (2.4).

Step 3 Set $\mathbf{X} = \mathbf{X}^I + h\lambda_I(\alpha)\mathbf{v}$.

The acceptance-rejection method is used in *Step 2*, in order to simulate from the kernel estimate K_e. The method relies on identifying a density function f_0 that can be (a) simulated much easier

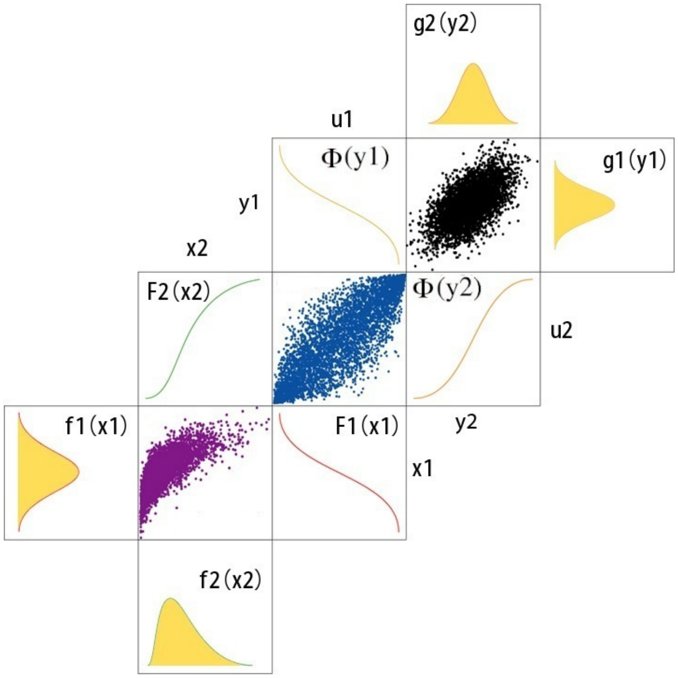


Figure 4.1: Statistical simulation using a copula.

and (b) scaled with some constant c so that it majorizes K_e, that is, so that $K_e(\mathbf{v}) \leq c \cdot f_0(\mathbf{v})$, $\forall \mathbf{v} \in R^d$. The method can be visualized as choosing a subsequence from an independent identically distributed sequence drawn from f_0, in such a way that the subsequence has probability density function K_e:

Step 2a Generate $\mathbf{v}$ to have probability density function f_0.

Step 2b Generate u from a uniform distribution in $[0, 1]$.

Step 2c If $u \leq K_e(\mathbf{v}) / (c \cdot f_0(\mathbf{v}))$ accept and return $\mathbf{v}$, otherwise return to step 2a.

In the case of the Epanechnikov kernel, we can select f_0 to be the uniform distribution in $[-1, 1]^{n+d}$ and $c = c_{n+d}^{-1}(n + d + 2)/2$.

4.2.3 Gaussian copula

Let $F_i(x_i) \equiv \Pr\{X_i \leq x_i\}$ denote the distribution function of X_i, $i = 1, \cdots, d$. This approach uses the transformations $U_i = F_i(X_i)$ to map $\mathbf{X}$ to $\mathbf{U} = [U_1, U_2, \cdots, U_d]$, where $\mathbf{U} \in [0, 1]^d$. The distribution function of $\mathbf{U}$ is called the copula of $\mathbf{X}$. If the distribution $F(\mathbf{x})$ of $\mathbf{X}$ is Gaussian, then the resulting copula is called the Gaussian copula. The key observation is that even if $F(\mathbf{x})$ is not Gaussian, then it is possible that the resulting copula is Gaussian. Under the assumption that the resulting copula is Gaussian, we can apply the following procedure to generate $N \gg 1$ observations of $\mathbf{X}$ [180]. Apply the transformations $Y_i = \Phi^{-1}(U_i)$, $i = 1, \cdots, d$, to map $\mathbf{U}$ to $\mathbf{Y} = [Y_1, Y_2, \cdots, Y_d]$, where Φ denotes the standard Gaussian distribution function. Then, by definition, the density $f_{\mathbf{Y}}(\mathbf{y})$ of $\mathbf{Y}$ is Gaussian. Therefore, we can fit a Gaussian density to the observations $\mathbf{Y} = [\mathbf{Y}^1, \mathbf{Y}^2, \cdots, \mathbf{Y}^n]$ and sample this density to obtain $N \gg 1$ observations of $\mathbf{Y}$, as discussed in Section 4.2.1. Then we apply the inverse transformation $X_i = F_i^{-1}(\Phi(Y_i))$ to obtain $N \gg 1$ observations of $\mathbf{X}$. A graphical illustration is shown in Fig. 4.1.

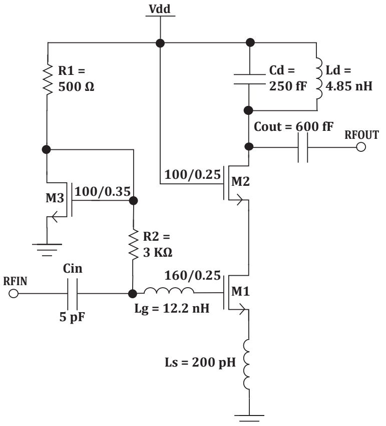


Figure 4.2: Schematic of low noise amplifier (LNA).

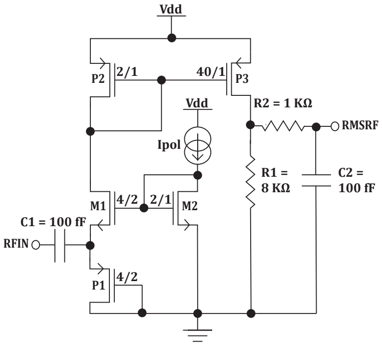


Figure 4.3: Schematic of envelope detector (ED).

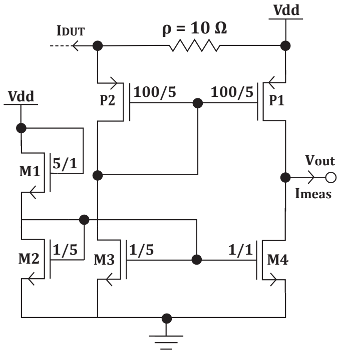


Figure 4.4: Schematic of current sensor (CS).

4.2.4 Results

A comparative study

Our test vehicle is an inductive source-degenerated cascode LNA used in the 802.11g standard receivers that operate in the 2.4 GHz ISM band. The schematic of the LNA is shown in Fig. 4.2. It is designed using the 0.25μm Qubic4+ technology by NXP Semiconductors. In this case study, we are investigating whether it is possible to replace the standard tests for measuring gain, NF, and S_{11} by two built-in tests that employ an envelope detector (ED) and a current sensor (CS) [181]. In the test mode, the LNA is stimulated with a 2.4 GHz sinusoidal of amplitude -30 dBm. The ED, shown in Fig. 4.3, measures the RMS value of the LNA's RF output. The CS, shown in Fig. 4.4, measures the dynamic power supply current flowing through the LNA. Its operation is based on monitoring the voltage drop across the small parasitic resistor ρ between the power supply pad and the core of the LNA. First, we record the output of the ED, then the input of the ED is switched to the output of the CS, in order to record the RMS value of the power supply current. The built-in test approach using envelope detectors and current sensors is cost-effective since only DC signals carrying RF information are extracted off-chip.

The specifications of the three performances are set at $k_1 \cdot \sigma$, i.e.

$$\begin{aligned} \text{gain} &\geq s_{\text{gain}} = \mu_{\text{gain}} - k_1 \cdot \sigma_{\text{gain}} && (4.11) \\ \text{NF} &\leq s_{\text{NF}} = \mu_{\text{NF}} + k_1 \cdot \sigma_{\text{NF}} && (4.12) \\ S_{11} &\leq s_{S_{11}} = \mu_{S_{11}} + k_1 \cdot \sigma_{S_{11}}, && (4.13) \end{aligned}$$

where the means and standard deviations are computed on an initial small Monte Carlo sample and k_1 is a multiplication coefficient. From simulations, we observed that the DC measurements provided by the ED and CS, denoted respectively by T_{ED} and T_{CS}, are proportional to gain and inversely proportional to NF and S_{11}. Thus, we place lower test limits on T_{ED} and T_{CS} at $k_2 \cdot \sigma$, i.e.

$$\begin{aligned} T_{ED} &\geq t_{T_{ED}} = \mu_{T_{ED}} - k_2 \cdot \sigma_{T_{ED}} && (4.14) \\ T_{CS} &\geq t_{T_{CS}} = \mu_{T_{CS}} - k_2 \cdot \sigma_{T_{CS}}, && (4.15) \end{aligned}$$

where as before the means and standard deviations are computed on an initial small Monte Carlo

Table 4.1: T_E 95% confidence intervals using different estimation techniques for $k_1 = 4$.

k_2	MC (10^6)	Multinormal ($5 \cdot 10^3$)	Non-param. $\alpha = 0$ ($5 \cdot 10^3$)	Non-param. $\alpha = -0.1$ ($5 \cdot 10^3$)	Copulas ($5 \cdot 10^3$)
1	[0,1]	[10,14]	[0,0]	[0,0]	[0,0]
2	[27,33]	[27,33]	[31,39]	[17,24]	[8,11]
3	[278,311]	[52,65]	[311,332]	[265,285]	[52,62]
4	[377,400]	[86,93]	[536,584]	[467,487]	[106,115]

Table 4.2: T_E 95% confidence intervals using different estimation techniques for $k_1 = 5$.

k_2	MC (10^6)	Multinormal ($5 \cdot 10^3$)	Non-param. $\alpha = 0$ ($5 \cdot 10^3$)	Non-param. $\alpha = 0.1$ ($5 \cdot 10^3$)	Copulas ($5 \cdot 10^3$)
1	[0,0]	[0,0]	[0,0]	[0,0]	[0,0]
2	[0,0]	[0,0]	[1,1]	[0,2]	[0,0]
3	[10,16]	[0,0]	[9,13]	[13,16]	[0,0]
4	[27,34]	[0,1]	[15,20]	[20,27]	[0,0]

sample and k_2 is a multiplication coefficient. Therefore, the parametric test escape is expressed as

$$T_E = \Pr\{\text{gain} < s_{\text{gain}} \cup \text{NF} > s_{\text{NF}} \cup S_{11} > s_{S_{11}} \,|\, T_{ED} \geq t_{T_{ED}}, T_{CS} \geq t_{T_{CS}}\}. \tag{4.16}$$

We carried out a post-layout Monte Carlo simulation analysis of the LNA with the embedded sensors. We generated in total 10^6 samples which took up about 3 months. For each sample, we recorded the performances and test measurements, that is, the values of $\mathbf{X} = [\text{gain}, \text{NF}, S_{11}, T_{ED}, T_{CS}]$. This allowed us to obtain an estimate of T_E which is close to the true value. Next, we considered a random set of $n = 5 \cdot 10^3$ samples out of the available 10^6 and we used the three techniques discussed above, in order to generate $N = 10^6$ observations of $\mathbf{X}$ corresponding to 10^6 instances of the LNA. These data are used to obtain estimates of T_E. Notice that obtaining 10^6 instances of the LNA using any of the above techniques takes up a few minutes. The fast estimates of T_E are compared to the true value of T_E that is obtained using the time-consuming Monte Carlo experiment.

Table 4.1 shows the 95% confidence intervals of T_E based on 10 bootstrap samples using different density estimation techniques, namely the time-consuming straightforward Monte Carlo (MC), the multinormal density, the non-parametric kernel density using two different values for α, and the Gaussian copula. The specifications are set at $k_1 = 4$ sigma while the test limits are set at k_2 sigma with $k_2 = \{1, 2, 3, 4\}$. Fig. 4.5 plots the results in Table 4.1. Table 4.2 and Fig. 4.6 show the respective results for $k_1 = 5$. The following observations can be made:

1) As shown by the "reference" MC curve, as k_2 increases, the test becomes less strict and, thereby, T_E increases.

2) The techniques based on multinormal density and Gaussian copula underestimate the T_E for certain values of k_2. The reason is that the underlying assumptions for these techniques are not satisfied. In particular, NF and S_{11} turn out to follow a generalized extreme value (GEV) distribution while gain, T_{ED}, and T_{CS} turn out to follow a Gaussian distribution. As a result, the joint distribution $f_{\mathbf{X}}(\mathbf{x})$ is not Gaussian. The resulting copula is not Gaussian either. It turns out to be a mixed copula where most pairs of performances and tests have a Gaussian copula, but others appear to have a Gumbel copula, i.e. a copula resulting from a Gumbel bivariate distribution. The theory for mixed copulas is not well developed yet. Notice that the multinormal density and Gaussian copula techniques should be used only if their assumptions are met, otherwise their utilization entails a risk. Nevetheless, we used them in our case study with the aim to evaluate the prediction errors that we commit.

3) The non-parametric density technique with the default value $\alpha = 0$ provides estimates that track well the increase of T_E with k_2. The confidence intervals of the estimates overlap with those of the MC except in the case of $k_2 = 4$: for $k_1 = 4$ the T_E is overestimated by about 150 ppm while for $k_1 = 5$ the T_E is underestimated by about 10 ppm. There are two reasons for this small

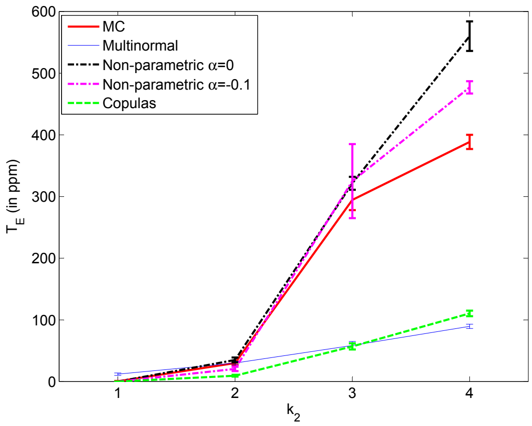


Figure 4.5: Performance of density estimation methods for $k_1 = 4$.

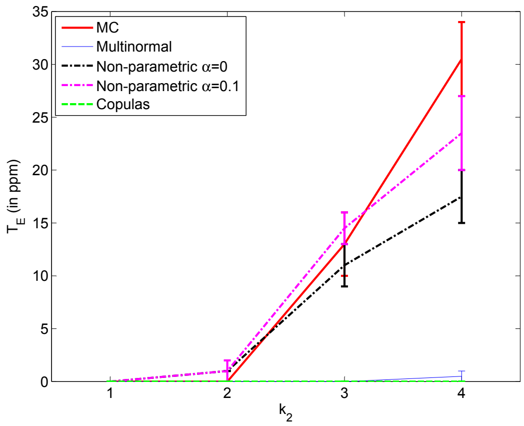


Figure 4.6: Performance of density estimation methods for $k_1 = 5$.

disagreement. First, the convergence of the non-parametric density in (2.1) to the true density $f_{\mathbf{X}}(\mathbf{x})$ is not guaranteed for a small initial sample of size n. Second, there exist no technique to choose optimally the values of h and α such that the convergence is expedited. For $k_1 = 4$, a better choice would have been to choose an α lower than zero, in order to have shorter tails and, thereby, less T_E. Following the same argument, for $k_1 = 5$, a better choice would have been to choose an α larger than zero. As shown in Tables 4.1 and 4.2 and in Fig. 4.5 and 4.6, these choices improve the results for $k_2 = 4$.

Alternative On-chip RF Built-in Tests (ORBiTs)

As a second example, we apply the non-parametric kernel density technique for proving the equivalence between a set of low-cost tests for RF transceivers and the traditional RF specification-based tests [182]. In particular, we evaluate the On-chip RF Built-in Tests (ORBiTs) proposed by Texas Instruments [100], which rely on on-chip sensors to extract digital, DC or low-frequency test signatures that nevertheless carry RF information. Thereafter, these test signatures are transported off-chip and processed by a low-cost tester with minimum requirements.

Our case study is a Bluetooth/Wireless LAN device designed and fabricated by Texas Instruments. Our objective is to reach a quick conclusion on the efficiency of ORBiTs based solely on a small data set that was obtained at the onset of production from the first wafer. This type of proactive analysis is very important in order to avoid undesired surprises later on in high-volume production. It allows convincing test engineers about the efficiency of the ORBiTs, to identify shortcomings, and to come up with remedies for refining the ORBiTs. Our test metric estimates based on the first wafer were confirmed on a much larger data set containing more than 1 million devices.

The results shown in Fig. 4.7 correspond to test metrics estimates in the scenario where a preselected subset of ORBiTs replaces the most sensitive RF specification-based test. In Fig. 4.7, T_E and Y_L denote the true test escape and yield loss per wafer, respectively, $\bar{T}_E$ and $\bar{Y}_L$ denote the true average test escape and average yield loss, respectively, and $\hat{T}_E$ and $\hat{Y}_L$ denote the early estimates based on the first wafer obtained by the non-parametric kernel density estimation technique. As it can be observed, test escape is slightly underestimated and yield loss is very slightly overestimated. Specifically, the true values are $\bar{T}_E = 0.7286\%$ and $\bar{Y}_L = 4.387\%$, whereas the early estimates are $\hat{T}_E = 0.4302\%$ and $\hat{Y}_L = 4.401\%$, that is, a difference of $\Delta T_E = 0.2984\%$ and $\Delta Y_L = -0.014\%$.

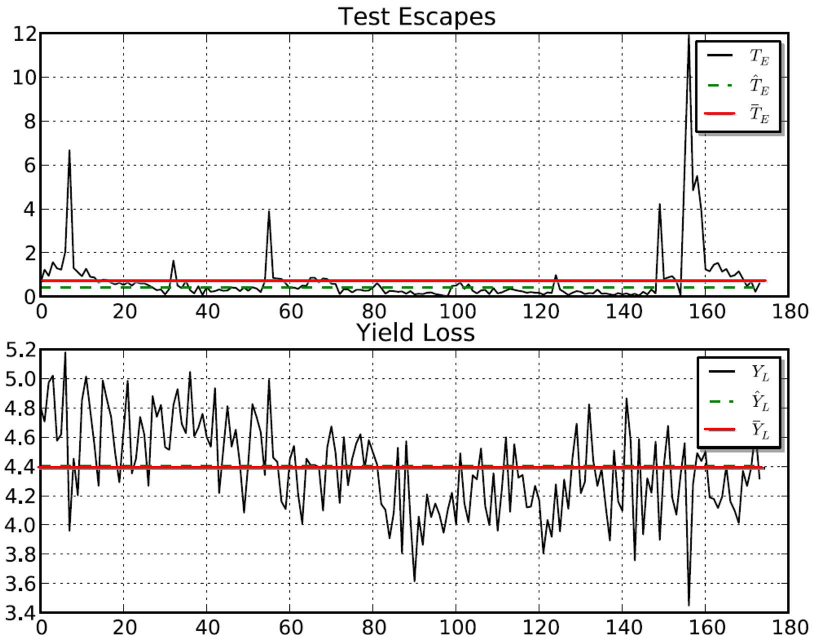


Figure 4.7: Test escape and yield loss prediction for ORBiTs.

4.3 Generation of extreme circuit instances

The density estimation approach is simple to implement, however it has the disadvantage that it relies on synthetic circuits that are not necessarily realistic. In particular, the density is estimated based on an initial Monte Carlo circuit-level simulation that, by default, will produce a set of functional circuits centered around the nominal design point. For this reason, the tails of the distribution, where low-probability test escape and yield loss events occur, may not be well estimated, resulting in inaccurate estimates of test escape and yield loss.

Another possibility is to focus on the tails but targeting specifically the generation of a set of "extreme" circuits that either fail one or more specifications or are marginally functional. Once this set becomes available, we can study the correlation between the performances $\mathbf{P}$ and the alternative low-cost tests $\mathbf{T}$, in order to obtain a qualitative measure of parametric test metrics.

As mentioned already, a straightforward Monte Carlo simulation is too slow to generate such a set of extreme circuits in a time-efficient manner. For this purpose, we employ the statistical blockade technique [183, 184], which acknowledges that, in a Monte Carlo analysis, sampling the process design kit (PDK) and subsequently creating a netlist are steps that can be performed very quickly and what is time-consuming is the actual electrical simulation of the netlist.

4.3.1 Statistical blockade

As shown in Fig. 4.8, the underlying idea is to bias the Monte Carlo simulation by examining whether a generated netlist will result in an extreme circuit before actually performing the simulation. If this scenario is likely to happen, then the simulation is allowed, otherwise it is blocked. The simulation speedup stems from the fact that we focus the simulation effort on generating circuit instances that are relevant for examining parametric test metrics [185–187].

The decision block in Fig. 4.8 is implemented using a classifier in the space of the process parameters. Fig. 4.9 illustrates snapshots of the algorithm. The space of process parameters is divided into two subspaces, namely the subspace $A_{\mathbf{x}a}$ that comprises circuits that are functional and

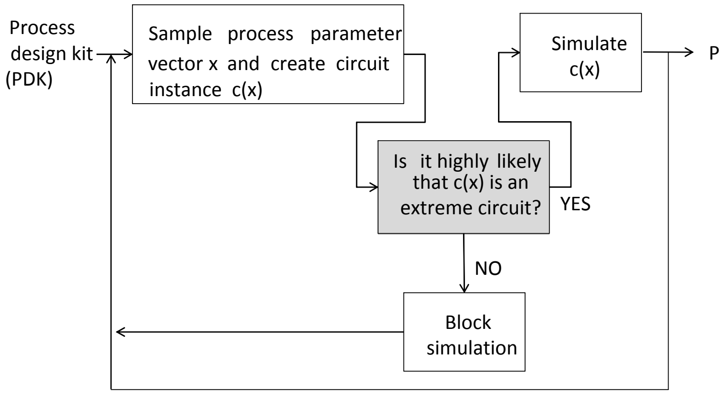


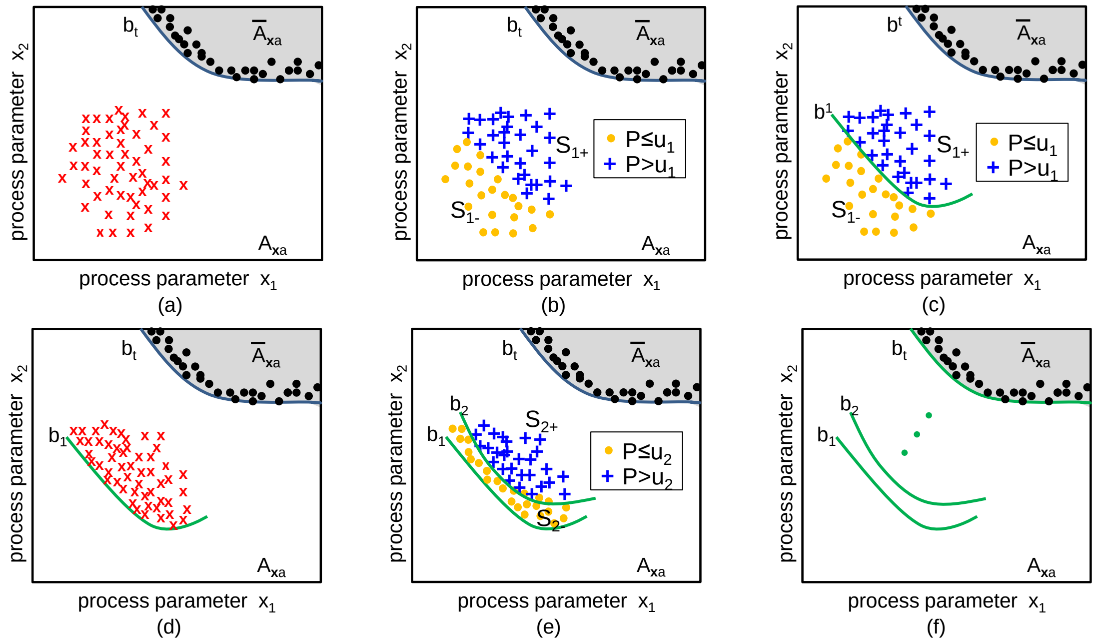
Figure 4.8: Flow of the statistical blockade technique.

the complement subspace $\bar{A}_{\mathbf{x}a}$ that comprises circuits that are faulty. The objective is to generate a parametric fault model that contains a set of most probable faulty circuits that, by default, will be distributed near the boundary b_t that separates $A_{\mathbf{x}a}$ from $\bar{A}_{\mathbf{x}a}$, as shown with the black dots in Fig. 4.9(a). Since test escape is defined probabilistically, considering this “reduced” parametric fault model that includes the most probable faulty circuits practically has no effect on the computation. As it will be seen, in the course of the algorithm we also generate a large set of marginally functional circuit instances which can be readily used thereafter to evaluate yield loss.

In the first step of the algorithm, we run a Monte Carlo simulation of a practical size n that results in a population of circuit instances that is centered around the nominal design point and far from the boundary b_t, as shown with the red crosses in Fig. 4.9(a). Assuming a performance P that has an upper specification s_u, we divide this population into two sets, namely the set S_{1+}, which has performance larger than a threshold u_1, and the set S_1- that has performance lower than u_1, as shown in Fig. 4.9(b). For example, the threshold u_1 could be the median of the population. We then train a classifier to separate the two sets S_{1+} and S_{1-}, as shown in Fig. 4.9(c). The allocated classification boundary b_1 serves as the decision block in Fig. 4.8 in the next iteration of the algorithm. In particular, we sample the PDK to generate a new set of netlists, but we choose to simulate only those netlists that lie in the subspace of S_{1+} since simulating a netlist that lies in the subspace of S_{1-} is unlikely to result in a faulty circuit with $P > s_u$ given that $u_1 < s_u$. The new population of size n shown with the red crosses in Fig. 4.9(d) lies now closer to the boundary b_t. We then divide this new population into two sets S_{2+} and S_{2-}, where the set S_{2+} has performance higher than a threshold $u_2 > u_1$ and S_{2-} has performance lower than u_2, and we allocate boundary b_2 to separate these two sets, as shown in Fig. 4.9(e).

The statistical blockade loop proceeds in this way and in each iteration we find $u_i > u_{i-1}$ and the boundary b_i is pushed more towards the tails of the distribution closer to b_t as compared to the boundary b_{i-1}, as shown in Fig. 4.9(f). In each iteration we update the decision block in Fig. 4.8 to take into consideration the more “extreme” boundary found so far. Practically this means that in each step the decision block is updated so as to have higher confidence about whether a circuit instance is likely to result in $P > s_u$ if it is simulated. As the algorithm evolves, in each iteration the size of the fault model increases and after a few iterations we reach the desirable size N. Notice that this will happen well before we approximate the boundary b_t.

The parameters n and u_i are user-defined. n should be selected as high as possible given the simulation time budget. For selecting u_i, there is trade-off between simulation time and how well the area of failing circuit instances is approximated. By setting u_i equal to the median of the i-th population, we maintain balanced training sets S_{i+} and S_{i-} at each iteration and we populate heavily the area around the boundary that separates them. Therefore, the allocation of the boundary b_i is more accurate and the area of failing circuit instances is well approximated in



(a) (b) (c) (d) (e) (f)

Figure 4.9: Progressive allocation of boundaries to approximate the area of circuit instances that result in performance failure.

the end. However, the boundary moves slowly towards the boundary b_t and, thereby, the algorithm takes more time to terminate. By setting u_i at a value much higher than the median, the boundary moves faster towards the boundary b_t and, thereby, the algorithm terminates faster, however, the set S_{+i} may overshadow the set S_{-i}, risking not to approximate equally well the area of failing circuit instances in the end.

If we define that a marginally functional circuit satisfies $s_u - \epsilon < P < s_u$, then for a large enough and practical value of ϵ, for example, setting ϵ equal to one standard deviation, a circuit instance that fails the specification limit is sampled with lower probability than a marginally functional circuit instance and, thereby, at any time during the course of algorithm, a set of marginally functional circuit instances of size $M > N$ is maintained.

Finally, the algorithm is run separately for each performance and each lower or upper specification limit, so as to ensure that in the end we generate faulty and marginally functional circuits corresponding to all performances.

4.3.2 Simulation effort

It can be proven that the statistical blockade algorithm, compared to the straightforward unbiased Monte Carlo approach, can generate a fault model of size N with a simulation speed up of [187]

$$G = \frac{\frac{1}{\Pr\{P>s_u\}}}{\frac{\Pr\{P>u_{r-1}\}}{\Pr\{P>s_u\}} + \sum_{i=1}^{r-1} \frac{n}{N} \cdot \left(1 - \frac{\Pr\{P>u_{r-1}\}}{\Pr\{P>u_{i-1}\}}\right)}, \tag{4.17}$$

where r is the total number of iterations.

Assuming that P follows a normal distribution with some mean μ and standard deviation σ, that is, $P \sim \mathcal{N}(\mu, \sigma)$, and that the upper specification s_u is set at $k \cdot \sigma$, that is, $s_u = \mu + k \cdot \sigma$, then

Table 4.3: Number of iterations r, number of simulations N_s, and speed up G for different values of k considering median thresholds and $N = 10^2$, $n = 10^3$.

k	2.5	3	3.5	4	4.5
r	5	7	9	12	15
N_s	4096	6173	8683	11542	14796
G	4	12	49.5	273.6	1989

$$\Pr\{P > s_u\} = \frac{1}{2}\left(1 - \operatorname{erf}\left(\frac{k}{\sqrt{2}}\right)\right). \tag{4.18}$$

Furthermore, assuming that u_i is the median of the i-th population, then

$$\Pr\{P > u_i\} = \left(\frac{1}{2}\right)^i. \tag{4.19}$$

Substituting (4.18) and (4.19) in (4.17), we obtain an expression of the speed up G in terms of k, n, and N. Table 4.3 shows the number of iterations r, the total number of circuit simulations N_s, and the speed up G for different values of k using $N = 10^2$ and $n = 10^3$. As it can be observed, the parametric fault model can be generated with a large speedup compared to a straightforward Monte Carlo simulation which is over 10X for moderate specifications placed at $3 \cdot \sigma$ and over 250X for more lenient specifications placed at $4 \cdot \sigma$.

4.3.3 Results

Our case study is an RF LNA designed in the 65nm CMOS065 technology by ST Microelectronics with the same topology as the RF LNA shown in Fig. 4.2. The PDK of this technology has 872 process parameters. The classification boundary in this high-dimensional space is implemented using decision trees. As an example, Fig. 4.10 shows the result for the gain performance. Fig. 4.10(a) shows the gain performance of the simulated circuits across the iterations of the statistical blockade algorithm. The gain has a lower specification set at $3 \cdot \sigma$ shown with the horizontal line. As it can be seen, in each iteration the set of faulty circuits that constitute the fault model increases, the performance median drops linearly, and finally at the 6-th iteration we reach a fault model of size $N = 100$. Fig. 4.10(b) shows the histogram of the initial Monte Carlo simulations and the fault model. The gain follows approximately a normal distribution. The fault model was produced by performing a total of around 5800 simulations which is in close agreement with the theoretical prediction of 6173 simulations in Table 4.3. Fig. 4.10(c) shows the histogram of marginally functional circuits generated in the course of the algorithm assuming $\epsilon = 0.5$ dB.

The fault model can be readily used to study correlations between performances and identify redundancies. For example, Fig. 4.11 plots the fault model together with an initial small-scale Monte Carlo sample onto the space of gain and NF. As it can be seen, if a circuit fails the gain specification, then it always fails the NF specification. Thus, the gain test is redundant and can be eliminated without resulting in any test escape. Notice that the contrary is not true, that is, if a circuit fails the NF specification, then it may not fail the gain specification.

Finally, the extreme circuit instances can be used to examine whether a set of alternative low-cost tests can replace the standard specification-based tests without sacrificing test accuracy. An example is shown in the plot of Fig. 4.12 which projects the fault model together with a set of marginally functional circuits onto the space of an alternative measurement pattern that results from two internal DC probes and an envelope detector measuring the RF power at the output of the LNA. As it can be seen, the fault model and the set of marginally functional circuits are cleanly separated, which proves the efficiency of this alternative measurement pattern.

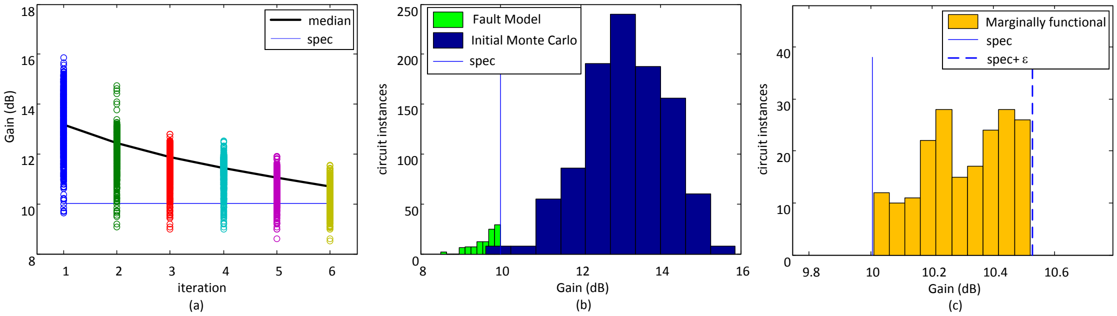
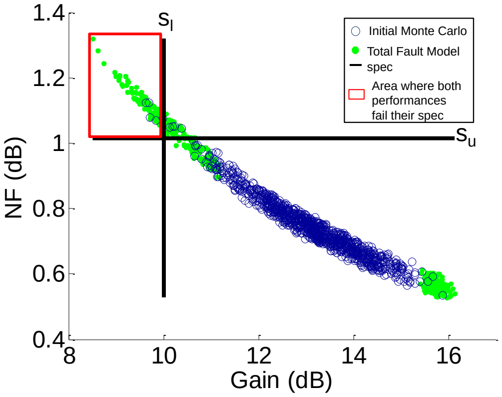


Figure 4.10: Generation of fault model and set of marginally functional circuits for the gain performance of the LNA.



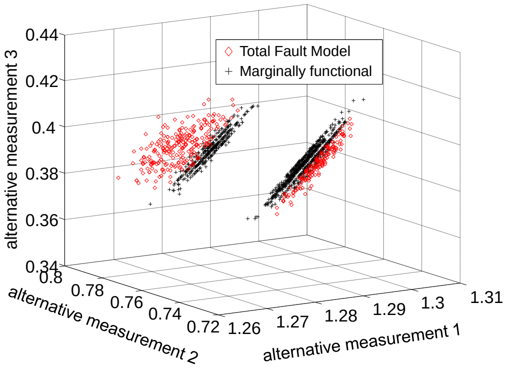


Figure 4.11: Correlation between gain and NF across the design space.

Figure 4.12: Efficiency of low-cost alternative measurement pattern for the LNA.

4.4 Extreme value theory

The algorithm in Section 4.3.1 generates fast a large number of extreme circuit instances, that is, circuit instances that are marginally functional or fail one or more of the specifications. This large number of extreme instances can be used to develop a closed-form mathematical model for the parametric test metrics based on extreme value theory, which is a modern theory in statistics aiming to assign probabilities to rare random events. It can be shown that if the distributions of the circuit performances and alternative tests have smooth tails, then the distribution of the tails is a generalized Pareto. The extreme circuits are used to fit this distribution and, thereby, to quantify parametric test metrics in ppm and provide confidence intervals, given specifications for the performances and test limits for the alternative tests [185, 188, 189].

4.4.1 Test Metrics Model

Following the notation in Section 4.1, we have shown that any parametric test metric can be expressed as

$$T_m = \Pr\{\cup_{i=1}^{n_z} Z_i \notin [z_\ell^i, z_u^i] \,|\, \cap_{i=1}^{n_w} W_i \in [w_\ell^i, w_u^i]\}, \tag{4.20}$$

where $Z = [Z_1, Z_2, \cdots, Z_{n_z}]$ and $W = [W_1, W_2, \cdots, W_{n_w}]$ are sets of either performances or alter-

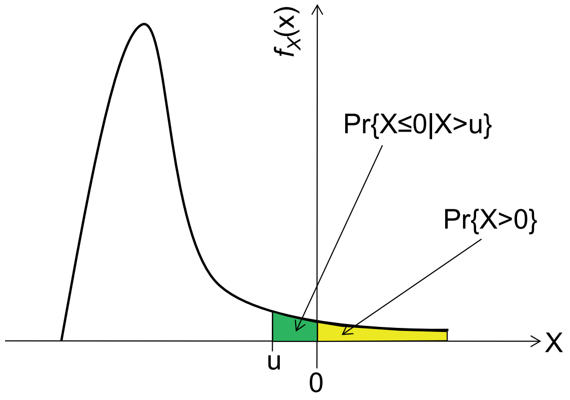


Figure 4.13: Probability density function of X.

native tests, $[z_\ell^i, z_u^i]$ are the acceptance limits for Z_i, and $[w_\ell^i, w_u^i]$ are the acceptance limits for W_i. If we define the random variable

$$V = \{Z \,\big|\, \cap_{i=1}^{n_w} W_i \in [w_\ell^i, w_u^i]\}, \tag{4.21}$$

then we can write (4.20) as

$$T_m = \Pr\{\cup_{i=1}^{n_z} V_i \notin [v_\ell^i, v_u^i]\}, \tag{4.22}$$

where $V = [V_1, V_2, \cdots, V_{n_z}]$ and $[v_\ell^i, v_u^i]$ are the acceptance limits for V_i. Furthermore, if we normalize V_i such that they have similar spread, then we can write

$$\begin{aligned} T_m &= \Pr\{V_1 \notin [v_\ell^1, v_u^1] \cup \cdots \cup V_{n_v} \notin [v_\ell^{n_z}, v_u^{n_z}]\} \\ &= \Pr\{\max(V_1 - v_u^1, v_\ell^1 - V_1) > 0 \cup \cdots \cup \max(V_{n_z} - v_u^{n_z}, v_\ell^{n_z} - V_{n_z}) > 0\} \\ &= \Pr\{X > 0\}, \end{aligned} \tag{4.23}$$

where the random variable

$$X = \max(V_1 - v_u^1, \cdots, V_{n_z} - v_u^{n_z}, v_\ell^1 - V_1, \cdots, v_l^{n_z} - V_{n_z}) \tag{4.24}$$

can be considered as a “dummy” performance. To obtain an observation of X, we first simulate the circuit and we obtain Z and W. If $\forall i$ $W_i \in [w_\ell^i, w_u^i]$, then we define $V = Z$ and $[v_\ell^i, v_u^i] = [z_\ell^i, z_u^i]$ and we compute X, otherwise, if $\exists i$ such that $W_i \notin [w_\ell^i, w_u^i]$, then an observation of X cannot be obtained in this simulation.

We have shown so far that the problem of estimating a test metric T_m is equivalent to estimating the probability of a random variable X being larger than 0, as illustrated in Fig. 4.13. Since a test metric T_m can be as low as a few ppm, that is, 0 is an “extreme” value of X, a Monte Carlo analysis of a reasonable number of runs will result in untrustworthy estimates with large variance. Next, we use the extreme value theory to obtain an analytical mathematical expression for T_m.

Let $u < 0$. We can write

$$\begin{aligned} T_m &= \Pr\{X > 0 \cap X > u\} \\ &= \Pr\{X > 0 | X > u\}\Pr\{X > u\} \\ &= (1 - \Pr\{X \le 0 | X > u\})\Pr\{X > u\} \\ &= (1 - \Pr\{X - u \le -u | X > u\})\Pr\{X > u\} \end{aligned} \tag{4.25}$$

The main result of the extreme value theory states that for any distribution of X that has a smooth tail beyond u and for a large enough u, the tail distribution, that is, the distribution of the random variable

$$Y = \{X - u | X > u\} \tag{4.26}$$

denoted by

$$F_Y(y) = \Pr\{X - u \leq y | X > u\}, \tag{4.27}$$

is a generalized Pareto [190, 191]

$$F_Y(y) = 1 - \left(1 + \frac{\xi y}{\sigma}\right)^{-1/\xi}, \tag{4.28}$$

where $-\infty < \xi < +\infty$ is the shape parameter and $\sigma > 0$ is the scale parameter. The support of the generalized Pareto distribution is $y \geq 0$ for $\xi \geq 0$ and $0 \leq y \leq -\sigma/\xi$ for $\xi < 0$. Therefore, if $\xi < 0$ and $-u > -\sigma/\xi$

$$F_Y(-u) = 1 \tag{4.29}$$

and equation (4.25) gives

$$T_m = 0. \tag{4.30}$$

In any other case

$$F_Y(-u) = 1 - \left(1 - \frac{\xi u}{\sigma}\right)^{-1/\xi} \tag{4.31}$$

and equation (4.25) gives

$$T_m = \left(1 - \frac{\xi u}{\sigma}\right)^{-1/\xi} \zeta_u, \tag{4.32}$$

where

$$\zeta_u = \Pr\{X > u\}. \tag{4.33}$$

We have shown so far that a test metric T_m can be expressed mathematically by the model in (4.32). To fit the model, we need to compute the three unknown parameters ξ, σ, and ζ_u.

4.4.2 Model fitting

The parameter ζ_u can be estimated through a Monte Carlo analysis with a reasonable number of runs since u is a value that does not lie far at the tail of $f_X(x)$. For a Monte Carlo analysis with N runs, if k observations of X satisfy $X > u$, then the maximum likelihood (ML) estimate of ζ_u is $\hat{\zeta}_u = k/N$.

However, the same is not true for ξ and σ since the resulting k observations of Y will probably be too few to allow accurate estimation with small variance. For the purpose of generating enough extreme observations $X > u$ to estimate ξ and σ accurately and with small variance we employ the statistical blockade technique described in Section 4.3.1. If $y_1, y_2, ..., y_k$, $y_j = x_j - u > 0$, denote k observations of Y, then the ML estimates $\hat{\xi}$ and $\hat{\sigma}$ of ξ and σ, respectively, are the values that maximize the log-likelihood function

Table 4.4: Scenarios resulting in different T_E values. In each scenario, only the tests with "x" are carried out.

scenario	power	phase margin	PSRR @ 10MHz	f_0	PSRR @ 1MHz	gain	gain margin	T_E (in ppm)
1	x	x	x	x		x	x	38
2	x		x	x		x		259
3						x		1003

$$\ell(\xi, \sigma) = \log \prod_{i=1}^{k} f_Y(y_i), \tag{4.34}$$

where

$$f_Y(y) = \frac{1}{\sigma}\left(1 + \frac{\xi y}{\sigma}\right)^{-(1+1/\xi)} \tag{4.35}$$

is the probability density function of Y.

Once the ML estimates $\hat{\xi}$, $\hat{\sigma}$, and $\hat{\zeta}_u$ are obtained, a ML estimate $\hat{T}_m$ of T_m can be obtained

$$\hat{T}_m = \left(1 - \frac{\hat{\xi} u}{\hat{\sigma}}\right)^{-1/\hat{\xi}} \hat{\zeta}_u. \tag{4.36}$$

For the derivation of confidence intervals the interested reader is referred to [188, 191].

4.4.3 Results

As a case study we employ a low-dropout regulator designed using the 65nm CMOS065 technology by STMicroelectronics. The circuit is characterized by the 7 performances shown in Table 4.4. We assume 3 different scenarios where in each scenario a different subset of specification tests is eliminated and only the remaining specification-based tests are carried out, as shown in Table 4.4. The last column shows the ground truth T_E for each scenario computed using ten million simulations on a macro-model of the circuit created using the Lysis$^{\text{TM}}$ tool by Infiniscale. Since the actual specification tests are carried out, $Y_L = 0$. As it can be seen, the 3 scenarios result in different T_E values ranging from a few tenths of ppm to hundreds of ppm.

Fig. 4.14 shows the prediction results using statistical blockade and extreme value theory based on a small number of simulations. As it can be seen, for all scenarios, from the second iteration onwards, the true value of T_E always lies within the 95% confidence interval. The number of simulations is considerably smaller than the number required in Monte Carlo analysis. By increasing the number of iterations, the 95% confidence intervals are shortened, e.g. the region where the T_E lies is better confined. One question that arises is when to stop the algorithm. With few iterations we risk to obtain inaccurate estimates and wide confidence intervals that might not be useful to draw conclusions. With many iterations we guarantee accurate estimates that are also confined in a short confidence interval, yet this is at the expense of a larger simulation effort. The choice depends on the number of simulations that we can afford to run in practice and the size of the estimated confidence interval that allows us to draw safe conclusions.

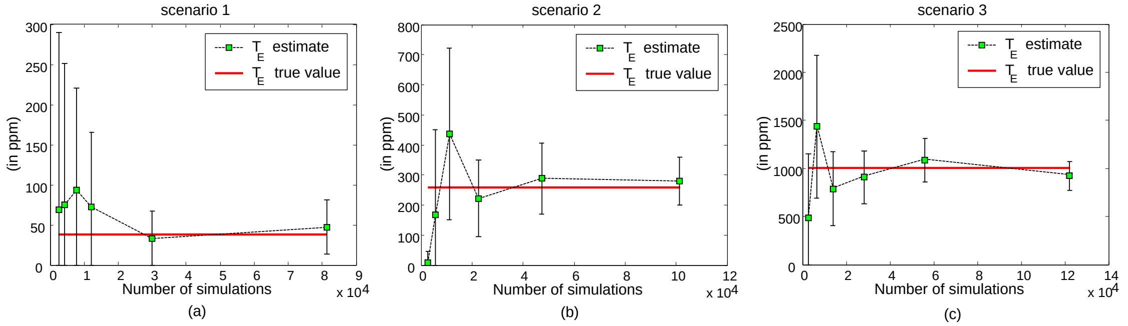


Figure 4.14: Test escape estimation results versus simulation effort for the three scenarios in Table 4.4.

4.5 Conclusion

We presented generic fast statistical simulation techniques that can be readily used to compute test metrics efficiently and, thereby, to optimize test limits, in order to achieve desired trade-offs between test metrics of interest. We expect that techniques such as the ones proposed herein will become a valuable tool in the hands of test practitioners to refine test generation programs at an early stage of the design, to evaluate existing test solutions, and to compare them with ones that are continuously being proposed towards reducing the high cost of standard specification-based test.

Chapter 5

Fault Diagnosis and Failure Analysis

5.1 Introduction

An integrated circuit (IC) is tested several times during its lifetime. A first set of tests are performed at wafer-level before packaging, in order to identify gross instabilities in the manufacturing process. Final module tests are performed after packaging and aim to verify that the actual design specifications of the IC are met. Depending on the end-user application, ICs may also go through burn-in tests, where they are exercised sufficiently long in stress conditions, in order to avoid early in-use system failures. Finally, ICs that are deployed in safety-critical and mission-critical applications need to be tested during their normal operation in idle times or even concurrently. In many cases, whenever an IC fails a test, it is important to diagnose the source of failure.

At the design stage, diagnosing the sources of failures in the first prototypes helps to reduce design iterations and to meet the time-to-market goal. Failures at this stage are related to the incomplete simulation models and the aggressive design techniques that are being adopted to exploit the maximum of performances out of the current technology. Especially for analog circuits, failures at this stage are very common due to the lack of reliable design automation tools.

In a high-volume production environment, diagnosing the sources of failures can assist the designers in gathering valuable information regarding the underlying failure mechanisms. The objective here is to make use of the diagnosis results to enhance yield for future products through improvement of the manufacturing environment and development of design techniques that minimize the failure rate.

Diagnosis is also of vital importance in cases where the IC is part of a larger system that is safety-critical, for example, a system that is deployed in automotive, aerospace, or biomedical applications. During its lifetime, an IC might fail due to aging, wear-and-tear, harsh environments, overuse, or due to defects that are not detected by the production tests and manifest themselves later in the field of operation. Here, it is important to identify the root-cause of failure so as to repair the system if possible, gain insight about environmental conditions that can jeopardize the system's health, and apply corrective actions that will prevent failure re-occurrence and, thereby, will expand the safety features.

Failure analysis (FA) of defective ICs is traditionally performed using light-emission, laser probing, picosecond imaging, etc. All these methods consist of observing failures by their optical characteristics. However, with the increasing reduction in feature sizes and the high complexity of modern ICs, the time-to-diagnose becomes intolerable and the success rate is reducing. To this end, there is a pressing need for an alternative diagnosis approach. The aim is to develop a low-cost approach that is able to reverse-engineer the root cause of failure or to guide appropriately the aforementioned classical FA methods, reducing the required time-to-diagnose and improving their success rate.

IC failures can be due to (a) excessive inter- and/or intra-die process variations, which we often refer to as parametric faults and (b) local spot defects that take forms of open- and short-circuits, which we often refer to as catastrophic faults. Parametric and spot defects can be a result of imperfections in the several steps of the fabrication process or can be induced in the field of operation due to aging, stress conditions, etc. Spot defects have for a long time been recognized as the main root cause of IC failures [192,193], but with the advent of short-channel technologies, parametric faults have become a significant source of failure. As shown in [194,195], spot defects can have a finite resistance value for open-circuits and a non-negligible resistance value for short-circuits, behaving as a parametric fault.

Techniques for diagnosing parametric faults include explicit nonlinear equations [196,197], sensitivity analysis [198,199] and regression functions [200]. The most well-known approach for diagnosing spot defects is the fault dictionary approach. It requires the *a priori* definition of a list of defects and their locations which can be obtained by historical defective data and an inductive fault analysis (IFA). Diagnosis consists of assigning a defect in the dictionary to the device under test (DUT). This is in essence a pattern recognition approach, which can be solved in a deterministic way using, for example, k-nearest neighbors [200], supervised neural networks [28], unsupervised neural networks [201], etc. It can also be solved in a probabilistic way to address the fault ambiguities [202,203].

5.2 Unified fault diagnosis flow

In this work, we propose a unified fault diagnosis flow that relies on an assembly of learning machines which are tuned in a pre-diagnosis learning phase [169,204]. A high-level description is illustrated in Fig. 5.1. The diagnosis starts by obtaining the diagnostic measurements specified in the pre-diagnosis phase. At first, we can reside on a subset of the standard specification-based tests. If the diagnostic accuracy is not sufficient, the complete specification-based test suite can be used or additional special tests can be crafted to target undiagnosed parameters or to resolve ambiguity groups.

The central learning machine is a defect filter that is trained in the pre-diagnosis phase to distinguish devices with catastrophic faults from devices with parametric faults [205]. Thus, the defect filter enables a unified catastrophic/parametric fault diagnosis approach without needing to specify in advance the fault type. This defect filter, discussed in detail in Section 2.2.2, relies on a non-parametric kernel density estimation $\tilde{f}(\mathbf{m})$ of the joint probability density function $f(\mathbf{m})$, where $\mathbf{m} = [m_1, \ldots, m_d]$ is the d-dimensional diagnostic measurement vector. Notice that $f(\mathbf{m})$ is estimated using only devices with process variation, that is, no devices with catastrophic faults are required to estimate $f(\mathbf{m})$. By construction, $\tilde{f}(\mathbf{m})$ is parameterized with a single parameter α, namely $\tilde{f}(\mathbf{m}, \alpha)$, which can be tuned in the pre-diagnosis learning phase to control the extent of the filter, that is, how much lenient or strict it is in filtering out devices [205].

Fig. 5.2 shows an example of a fitted joint probability density function in a 2-dimensional diagnostic measurement space. The density is fitted using the devices with process variations shown with the blue dots. The isoline contour of zero probability density serves as the defect filter. By tuning the parameter α, we can set the location of the isoline contour of zero probability density so as to make the defect filter stricter or more lenient. As it can be seen, the devices with catastrophic faults, shown with the red dots, lie in an area that has zero probability density, that is, $\tilde{f}(\mathbf{m}, \alpha) = 0$, since they are inconsistent with the statistical nature of the bulk of the data from devices with process variations that was used to estimate the density. The devices with catastrophic faults that are filtered out are forwarded to multi-class classifiers that are trained in the pre-diagnosis phase to map any diagnostic measurement pattern to the underlying catastrophic fault. Thus, in this step we follow a fault dictionary approach that employs multi-class classifiers, each with N outputs, where N is the number of modeled catastrophic faults in the pre-diagnosis phase. Details of diagnosis of catastrophic faults will be discussed in Section 5.3. On the other hand, if $\tilde{f}(\mathbf{m}, \alpha) > 0$, the device is considered to contain process variations, that is, a parametric fault

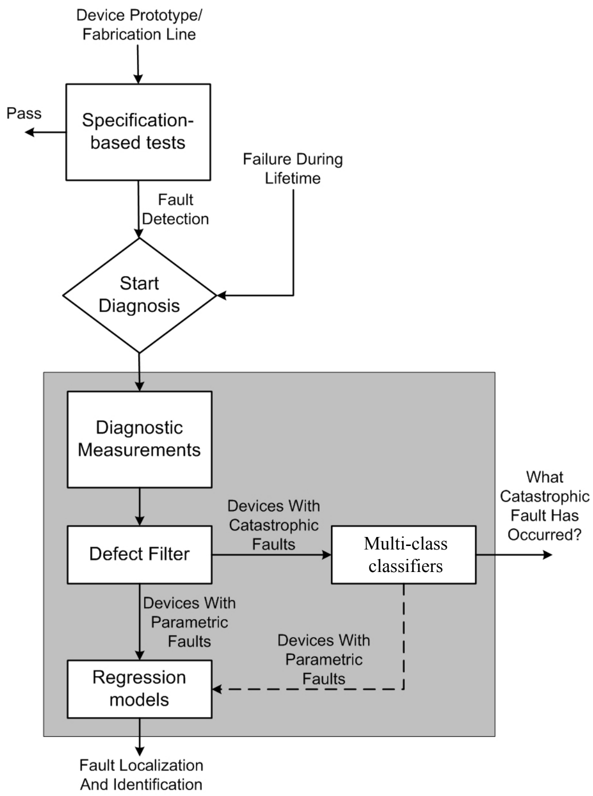


Figure 5.1: Unified fault diagnosis flow.

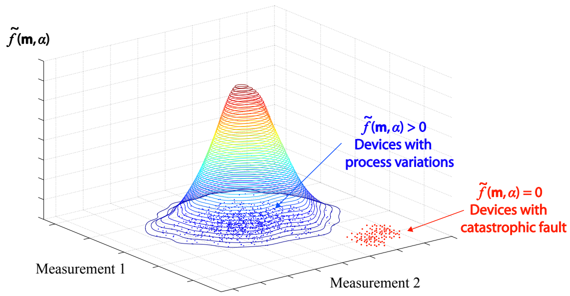
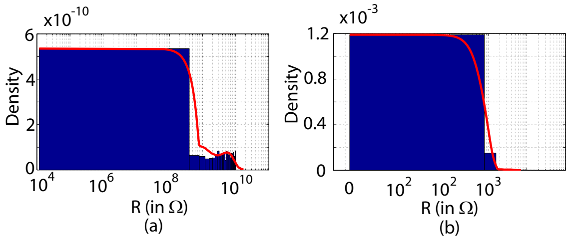


Figure 5.2: Defect filter in a 2-dimensional diagnostic measurement space.



(a)

(b)

Figure 5.3: Estimated probability density function of resistance (in Ω) for (a) open defects and (b) short defects, plotted in logarithmic scale.

has occurred. For parametric fault diagnosis, we use nonlinear inverse regression functions that are trained in the pre-diagnosis phase to map the diagnostic measurement pattern to the values of circuit parameters of interest. Details of diagnosis of parametric faults will be discussed in Section 5.4.

The defect filter is always tuned to filter out devices with catastrophic faults. However, this could inadvertently result in some devices with parametric faults being also screened out and forwarded to the classifier. To correct this leakage, each multi-class classifier is trained during the pre-diagnosis phase to include detection of devices with process variations as well, i.e. an additional output is added, raising the number of outputs to $N+1$. Thus, in the unlikely case where a device with a parametric fault is presented to a classifier, the classifier kicks it back to the regression tier.

5.3 Diagnosing catastrophic faults

From an IFA and historical defect data, we create a list of the N most probable catastrophic short- or open-circuit fault locations. The catastrophic faults are injected sequentially in the netlist of the device and we perform Monte Carlo simulation, where in each pass a different short or open resistance is used. These values are sampled from the resistance distributions for short- and open-circuits [206], as shown in Fig. 5.3. In this way, a fault cluster is created for each catastrophic fault. It is also possible to enhance each fault cluster with more points that represent process spread. This is recommended if we can afford the extra simulation effort. The fault clusters compose the fault dictionary.

The fault dictionary is used in the pre-diagnosis phase to train a set of multi-class classifiers, where each classifier allocates a boundary in the space of diagnostic measurements to separate

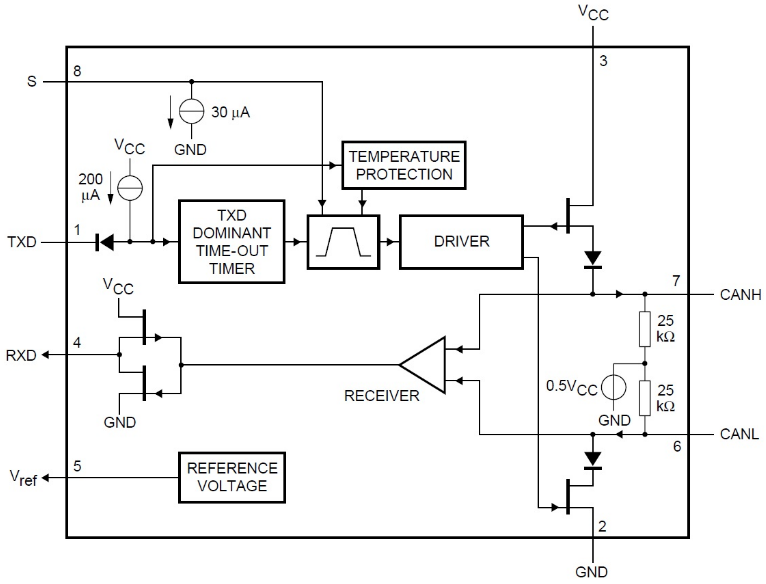


Figure 5.4: High-level block diagram of the CAN transceiver.

one fault cluster from another. For a device that is diagnosed by the defect filter to contain a catastrophic fault, we obtain the same d-dimensional diagnostic measurement pattern and we present it to the classifiers. Each classifier assigns a score to each catastrophic fault, instead of just making a deterministic judgment about which catastrophic fault is present in the faulty device. Thereafter, the individual scores of the classifiers are combined to assign a single score to each catastrophic fault. As suggested by practitioners in the field of pattern recognition [207, 208], the overall classification accuracy can be improved by combining the response of different classifiers. We have chosen the averaging method by reason of its simplicity and its capacity of providing a score for all catastrophic faults. The averaging method consists of computing the average value of scores obtained by different classifiers.

5.4 Diagnosing parametric faults

In the pre-diagnosis phase, we train a set of non-linear regression functions to map the diagnostic measurement pattern to the values of circuit parameters of interest. In particular, for each parameter $\{p_j\}_{j=1,\cdots,n_p}$, we train a regression function $f_j : \mathbf{m} \mapsto p_j$, $j = 1, ..., n_p$ [205]. The training phase employs a set of devices with typical and extreme process variations. Unlike prior work on parametric fault diagnosis, this approach allows an implicit modeling of the unknown dependencies between $\mathbf{m}$ and all p_j using statistical data and domain-specific knowledge. Thus, it avoids the complications related to an explicit formulation (i.e. diagnosability, convergence, problems with large deviations in parameters, etc.) [196–199]. For a device that is diagnosed by the defect filter to contain a parametric fault, we obtain the diagnostic measurement pattern and we use the inverse regression functions to predict the values of circuit parameters. The main goal is to construct regression models with generalization capabilities, i.e. that can accurately predict the parameters of devices other than those in the training set.

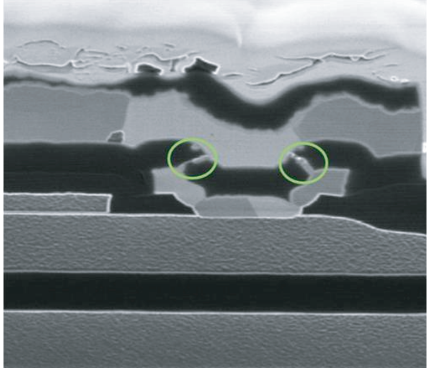


Figure 5.5: FIB image of the short-circuit defect diagnosed in DUT 18.

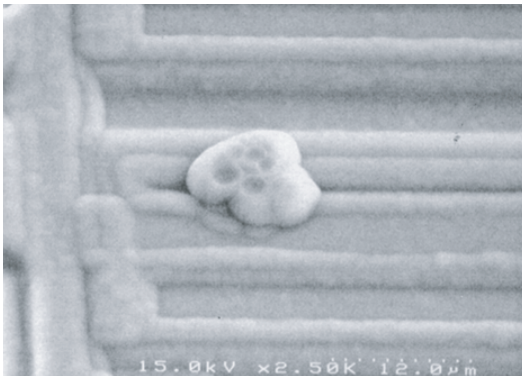


Figure 5.6: SEM image of the short-circuit defect diagnosed in DUT 26.

5.5 Results

Our case study is a Controller Area Network (CAN) transceiver designed by NXP Semiconductors in a BiCMOS-DMOS process. The netlist of this DUT has 1032 elements of which 613 are transistors. A high-level block diagram of the device is shown in Fig. 5.4. This device is produced in high-volume and constitutes an essential part in the electronic system of automobiles. It is deployed in a safety-critical application, thus it has to meet stringent specifications and demands practically zero test escapes. Therefore, it is of vital importance to diagnose the sources of failure, in order to achieve better quality control and, when possible, improve the design such that similar failures do not emerge in the field during the lifetime of the operation.

We have at hand a set of 29 devices from different lots that failed at least one of the specifications during production test. The classical FA was carried out for all these devices and it was observed in all cases that the cause of failure is a short-circuit defect. For example, Fig. 5.5 shows a Focused Ion Beam (FIB) image of the short-circuit defect observed in DUT 18 and Fig. 5.6 shows a Scanning Electron Microscope (SEM) image of the short-circuit defect observed in DUT 26. For the purpose of the experiment, we assume that the actual defects that have occurred in each of these devices are unknown and we set out to diagnose them by applying the proposed flow. The standard production tests for this DUT include digital, analog, and IDDQ tests. We consider $d = 97$ non-digital tests (i.e. voltage, current, timing and hysteresis measurements) which dominate the test time. No additional measurements are performed for the purpose of diagnosis. Each measurement is scaled in the range [-1,1].

For this particular device produced in high volume under a mature technology where process variation is well understood and controlled, device failures due to parametric deviation of process and device parameters are very unlikely to occur. Furthermore, for this particular technology, open-circuit defects are less likely to occur than short-circuit defects. As a result, more than 90% of the observed defects in production are short-circuits. Thus, only catastrophic short-circuit faults are considered for fault modeling.

We have performed an IFA which resulted in a list of N=923 probable short-circuit faults. Each short-circuit is modeled with 3 different bridge resistance values (e.g. 5 Ω, 50 Ω, 200 Ω). These values are chosen according to defect data characterization analysis for this particular technology. Subsequently, a total of $3 \times 923 = 2769$ fault simulations were carried out to generate the fault clusters that we use to build the diagnosis tools. In this large-scale industrial case study, we cannot afford extra simulation effort to consider process variation in fault simulation. Thus, each simulation consists of inserting a short-circuit defect in the netlist with a specific bridge resistance value while the circuit parameters are fixed at their nominal design values. In each fault simulation we collect the same d =97 diagnostic measurements. Fault simulation took approximately 12 hours. Notice that fault simulation is a one time effort. Building the diagnosis tools and performing the diagnosis

Table 5.1: Diagnosis Results.

DUT	True defect	Defect ranking	Normalized scores
1	107	**107** 90 920 114 347	0.924 0.923 0.923 0.923 0.923
2	320	**320** 341 126 374 111	0.948 0.867 0.833 0.827 0.822
3	125	47 616 **125** 681 360	0.914 0.839 0.838 0.837 0.837
4	101	**101** 117 459 50 388	0.831 0.829 0.826 0.817 0.817
5	216	**216** 666 192 516 120	0.831 0.795 0.792 0.788 0.785
6	300	524 608 744 294 789	0.900 0.890 0.862 0.855 0.850
7	20	**20** 126 24 27 111	0.889 0.866 0.862 0.850 0.849
8	27	**27** 111 126 446 341	0.891 0.856 0.837 0.834 0.834
9	104	111 **104** 465 721 126	0.848 0.844 0.839 0.823 0.822
10	21	310 682 524 789 608	0.867 0.858 0.855 0.855 0.851
11	101	**101** 117 459 50 388	0.831 0.829 0.826 0.818 0.817
12	19	**19** 541 106 562 595	0.810 0.794 0.780 0.780 0.780
13	19	**19** 541 562 595 106	0.799 0.791 0.788 0.771 0.771
14	140	401 **140** 457 40 919	0.936 0.912 0.911 0.910 0.910
15	20	**20** 24 126 27 111	0.887 0.865 0.862 0.853 0.849
16	101	**101** 117 459 50 388	0.831 0.829 0.826 0.817 0.817
17	107	**107** 90 920 114 347	0.924 0.923 0.923 0.923 0.923
18	31	117 **31** 50 388 622	0.901 0.888 0.882 0.881 0.880
19	101	252 305 366 363 31	0.883 0.857 0.846 0.844 0.843
20	19	**19** 541 106 562 595	0.821 0.794 0.793 0.780 0.780
21	156	524 608 744 789 682	0.903 0.893 0.872 0.872 0.866
22	20	**20** 126 24 27 111	0.882 0.870 0.867 0.864 0.853
23	107	**107** 90 920 114 347	0.924 0.923 0.923 0.923 0.923
24	22	**22** 19 541 338 106	0.826 0.808 0.808 0.795 0.795
25	107	**107** 90 920 114 347	0.924 0.923 0.923 0.923 0.923
26	380	666 192 516 676 457	0.910 0.906 0.905 0.904 0.903
27	376	383 456 112 34 196	0.924 0.920 0.830 0.826 0.824
28	28	666 192 516 355 676	0.910 0.907 0.898 0.896 0.896
29	300	524 608 744 475 215	0.896 0.896 0.866 0.864 0.862

of a faulty DUT takes only a few minutes.

In this real-world case study, the injection of a defect in the device netlist might render the system of equations during circuit simulation unsolvable. Therefore, it is highly likely that there exist diagnostic measurements that are unattainable for specific defects and specific resistance values. The problem of missing values also concerns the real diagnostic measurement pattern. Indeed, a diagnostic measurement might hit the instrument limit, in which case its value is artificially "forced" to equal the instrument limit. In this case, we can only use the pass/fail information provided by the diagnostic measurement and we should consider the absolute value as missing. To account for missing values, we follow the recommendations in [209]. In short, missing values force us to exclude either diagnostic measurements or defects from the analysis. In the former case, we remove information that may be useful for performing diagnosis. In the latter case, we are bound to obtain misleading diagnosis results if the defect that is present in the faulty device has been inadvertently excluded from the analysis.

We consider three classifiers based on Euclidean distance, non-parametric kernel density estimation, and pass/fail verification.

Table 5.1 shows the 5 most highly ranked defects according to their scores for each of the 29 failed devices. The first column shows the DUT number, the second column shows the actual defect that is present, the third column shows the ranking of defects, and the fourth column shows the corresponding (rounded) final scores. As it can be observed from Table 5.1, the proposed method diagnoses correctly 17 out of the 29 failed devices with the true defect matching with the first choice and for 4 failed devices the true defect appears in the first three choices. In some cases the ranking indicates with high confidence the location of the defect. For example, for DUT 2, the five defects that come first in the ranking (e.g. 320, 341, 126, 374, 111) are short-circuits across nodes of a transistor pair. The ranking of these defects can be subsequently used to speed up a classical FA method by placing the emphasis on the locations of the chip where the defect has probably occurred.

By comparing the diagnosis predictions to the true defect existing in each DUT, we identify the defects that we are unable to diagnose. We were unable to diagnose correctly defects 21, 28, 156, 300, 376, 380, and in one case defect 101. Furthermore, in some cases the true defects are not ranked as the first priority, such as the cases of DUT 3, 9, 14, and 18. The reason for the above fault ambiguities is that there are different defects whose patterns tend to overlap in the diagnostic measurement space. In other words, the impact of these defects on the diagnostic measurements is very similar. Fault ambiguity can be observed as early as in the fault simulation phase. To resolve fault ambiguity we will need to consider additional diagnostic measurements.

5.6 Conclusion

In this chapter, we briefly presented a methodology for fault modeling and fault diagnosis of analog circuits based on machine learning. The proposed approach is able to diagnose both catastrophic and parametric faults without making any prior assumption about the type of fault that has occurred. A defect filter recognizes the type of fault and forwards the faulty circuit to the appropriate tier. Circuits with catastrophic faults are forwarded to a combination of multi-class classifiers which list the catastrophic faults according to their likelihood of occurrence. Circuits with parametric faults are forwarded to inverse regression functions which predict the values of a set of predefined design and transistor-level parameters, in order to locate and predict the faulty parameter. The proposed approach was demonstrated on high-volume manufacturing data showing excellent overall diagnosis rate. We also briefly discussed the complexities often met in real case studies related to missing values in data.

Chapter 6

Perspectives

The research objectives can be grouped into six principal research axes related to analog, mixed-signal (AMS), and RF integrated circuits (ICs), namely: (1) modeling of heterogeneous systems-of-systems; (2) design synthesis; (3) integrated circuit testing and design-for-testability; (4) self-repair, fault tolerance, and self-healing; (5) diagnosis and failure analysis; and (6) computer-aided design techniques for test metrics estimation.

6.1 Modeling of heterogeneous systems-of-systems

Systems of Systems (SoS) is a collection of heterogeneous systems that combine their capabilities and resources to create a new, more complex system that offers more functionality and better performance trade-offs. The heterogeneity means that the individual systems may have different functioning , i.e. digital ICs, AMS ICs, RF ICs, software, sensors, actuators, etc., and may operate in different domains, i.e. electrical, electromechanical, chemical, optical, magnetic, etc. The pre-silicon verification, post-silicon validation and debugging, system-level testing development, and diagnosis and failure analysis of SoS is extremely challenging in particular due to this heterogeneity. To improve design efficiency and to achieve the required levels of yield, robustness, and reliability, it is required to generate efficient simulation methodologies and tools, in order to be able to co-simulate the individual systems, by not only capturing their individual operation, but also their various interactions. The success of pre-silicon verification, post-silicon validation and debugging, system-level testing development, and diagnosis and failure analysis will strongly dependent on the availability and flexibility of such simulation methodologies and tools. The focus in this project will be the development of a simulation framework based on the System C/System C-AMS language especially for capturing the interactions between the analog and digital worlds.

6.2 Design synthesis

Unlike digital design that is based on well-characterized cell libraries which allow fast and reliable design automation, AMS/RF design remains a full-custom and cumbersome task. Nowadays, designing an AMS/RF circuit is more of an art, relying to a very large degree on years of experience of the designer. From behavioral modeling down to transistor-level circuit sizing and layout drawing, there is very little to no automation, requiring in every step the high expertise of the designer. An automatic AMS/RF design framework remains the holy grail in the AMS/RF design community since it will help reduce the design cycle to meet the pressing time-to-market goal and will give the flexibility to the designer to quickly explore different design options to obtain optimal performance trade-offs that fully exploit the capabilities a technology has to offer. AMS/RF circuit synthesis approaches proposed to date have not materialized mainly because the designer believes that the design exploration that these approaches offer is limited and that there is always space for improvement and for a more aggressive design with better performance trade-offs. The objective in this project will be to incorporate during the AMS/RF design synthesis the prior knowledge, know-how, apprehension, and skills of the AMS/RF designer, in a way that the synthesis procedure still remains automatic, transparent, and user-friendly.

6.3 Integrated circuit testing and design-for-testability

Testing the AMS/RF functions of Systems-on-Chip (SoCs) is responsible for the largest fraction of the test cost, despite the fact that AMS/RF circuits occupy a relatively small area on the die. In addition, according to the International Technology Roadmap for Semiconductors (ITRS), we are quickly reaching the point where the manufacturing cost per transistor and the test cost per transistor are becoming equal. While the manufacturing cost drops following Moore's law, the test cost has remained stable during the past decades since the higher the transistor integration is, the more complex the test is. Therefore, reducing the cost of test especially for AMS/RF circuits is an area of focus and innovation for the industry. In this context, integrated circuit testing techniques have the potential to reduce drastically the test cost by alleviating the dependence on elaborate external test equipment and by simplifying the test stimulus generation and test response analysis. The objectives in this project is to continue developing efficient integrated circuit testing techniques that are non-intrusive and transparent to the operation of the circuit under test (CUT), such that the performance of the CUT is not degraded due to monitoring operation. The non-intrusiveness and transparency will be achieved by employing fully-digital techniques and/or by obtaining information-rich test information through temperature and process control monitors instead of actually tapping into the signal paths of the CUT.

6.4 Self-repair, fault tolerance, and self-healing

AMS/RF ICs are highly susceptible to process parameter variations, power supply and temperature variations, environmental disturbances, and ageing effects. The objective of this project is to equip AMS/RF ICs with efficient self-repair, fault tolerance, and self-healing capabilities, both at post-manufacturing and during their lifetime, in order to account for the aforementioned effects. This is of vital importance especially for AMS/RF ICs that are deployed in safety-critical, mission-critical, and remote-controlled systems that demand high reliability, such as medical instrumentation, aerospace, automotive, sensor networks, etc. In these cases, AMS/RF ICs need to be capable of indicating reliability hazards, transient errors, unsafe operation, or aging, and, ideally, they also need to be capable of performing error correction if necessary. Non-intrusive and transparent integrated circuit testing techniques can play a vital role in this context since the extracted on-chip measurements can provide rich information about the health of the IC. This information can be used thereafter to tune knobs that are judiciously inserted into the IC to add several degrees of freedom, in order to calibrate the performances and obtain an optimal trade-off. In this way, in post-manufacturing we can correct yield loss and during the lifetime we can adapt the operation to an unexpected application, harsh environments, and ageing. The self-repair, fault tolerance, and self-healing procedures should be simple enough to be directly implemented with the computing resources available within the system. In addition, as an auxiliary benefit, they can be used to adjust the power supply to the application mode, thus achieving an optimum performance trade-off without wasting energy.

6.5 Fault diagnosis and failure analysis

In the case of safety-critical, mission-critical, and remote-controlled applications, diagnosis offers valuable insight about the failing part of the system that needs to be repaired, about the environmental conditions that can jeopardize the system's health, and about corrective actions that should be applied to prevent failure re-occurrence in future product generations and, thereby, to expand the safety features. Efficient diagnosis schemes are also essential at the design stage to diagnose the sources of failures in the first prototypes. In this case, diagnosis tools can be combined with post-silicon validation tools to improve the debugging procedure. In this way, diagnosis can help to reduce design iterations and to meet the time-to-market goal. Moreover, in high-volume production, diagnosing the sources of failures assists the designers in collecting valuable information regarding the underlying failure mechanisms, in order to enhance yield for future product generations through improvement of the manufacturing environment and development of design techniques that minimize the failure rate. The objective in this project is to develop diagnosis methodologies and tools for AMS/RF ICs with the aim to identify defects down to the transistor level, in order to speed-up and guide appropriately the physical failure analysis (PFA) and improve its success rate. In this context, integrated circuit testing techniques become of vital importance since they can increase controllability and observability of sub-systems, internal Intellectual Property (IP) blocks, and interconnections, thus, allowing to isolate with as much rigor as possible the area wherein the failure has occurred.

6.6 Computer-aided design techniques for test metrics estimation

The complexity and high-cost of AMS/RF standard specification-based functional tests has sparked a lot of interest for developing alternative low-cost test solutions. Researchers and test engineers are continuously proposing new solutions, but few have been materialized in industry to date. The reason is that it is very challenging to prove before moving to high-volume production that these solutions are equivalent to the standard specification-based functional testing in terms of test accuracy. Specifically, it is very challenging to argue with confidence that these solutions achieve high fault coverage (or, equivalently, low test escape), that is, not too many faulty devices are labelled as functional, and high yield coverage, that is, not too many functional devices are labelled as faulty. The test coverage and yield coverage metrics need to be estimated quickly with parts-per-million (ppm) accuracy at the design and test development phases such that when a new solution is crafted it can be studied thoroughly and a decision can be made as to whether we should summarily abandon it, accept it and try it in high-volume production, or refine it. Test metrics estimation methodologies proposed to date target only small, stand-alone circuits that can be simulated fast at transistor-level. The objective of this project is to focus on developing a generic test metrics estimation methodology that can applied to large circuits with long simulation times, such as Analog-to-Digital Converters (ADCs), phase locked loops (PLLs), and complete RF transceivers.

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