Compact modeling and circuit design based on ferroelectric tunnel junction and spin-Hall-assisted spin-transfer torque

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Modélisation compacte et conception de circuit à base de jonction tunnel ferroélectrique et de jonction tunnel magnétique exploitant le transfert de spin assisté par effet Hall de spin

(Compact modeling and circuit design based on ferroelectric tunnel junction and spin-Hall-assisted spin-transfer torque)

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Contents

Abstract

Non-volatile memory (NVM) devices have been attracting intensive research interest since they promise to solve the increasing static power issue caused by CMOS technology scaling. This thesis focuses on two fields related to NVM: one is the ferroelectric tunnel junction (FTJ), which is a recent emerging NVM device. The other one is the spin-Hall-assisted spin-transfer torque (STT), which is a recent proposed write approach for the magnetic tunnel junction (MTJ). Our objective is to develop the compact models for these two technologies and to explore their application in the non-volatile circuits through simulation.

First, we investigated physical models describing the electrical behaviors of the FTJ such as tunneling resistance, dynamic ferroelectric switching and memristive response. The accuracy of these physical models is validated by a good agreement with experimental results. In order to develop an electrical model available for the circuit simulation, we programmed the aforementioned physical models with Verilog-A language and integrated them together. The developed electrical model can run on Cadence platform (a standard circuit simulation tool) and faithfully reproduce the behaviors of the FTJ.

Then, by using the developed FTJ model and STMicroelectronics CMOS design kit, we designed and simulated three types of circuits: i) an FTJ-based random access memory (FTRAM), ii) two FTJ-based neuromorphic systems, one of which emulates spike-timing dependent plasticity (STDP) learning rule, the other implements supervised learning of logic functions, iii) an FTJ-based Boolean logic block, by which NAND and NOR logic are demonstrated. The influences of the FTJ parameters on the performance of these circuits were analyzed based on simulation results.

Finally, we focused on the reversal of the perpendicular magnetization driven by spin-Hall-assisted STT in a three-terminal MTJ. In this scheme, two write currents are applied to generate spin-Hall effect (SHE) and STT. Numerical simulation based on Landau-Lifshitz-Gilbert (LLG) equation demonstrates that the incubation delay of the STT can be eliminated by the strong SHE, resulting in ultrafast magnetization switching without the need to strengthen the STT. We applied this novel write approach to the design of the magnetic flip-flop and full-adder. Performance comparison between the spin-Hall-assisted and the conventional STT magnetic circuits were discussed based on simulation results and theoretical models.

Keywords: Ferroelectric tunnel junction, magnetic tunnel junction, Spin-Hall effect, Spin-transfer torque, compact model, non-volatile circuits.

Résumé

Les mémoires non-volatiles (MNV) sont l'objet d'un effort de recherche croissant du fait de leur capacité à limiter la consommation statique, qui obère habituellement la réduction des dimensions dans la technologie CMOS. Dans ce contexte, cette thèse aborde plus spécifiquement deux technologies de mémoires non volatiles : d'une part les jonctions tunnel ferroélectriques (JTF), dispositif non volatil émergent, et d'autre part les dispositifs à transfert de spin (TS) assisté par effet Hall de spin (EHS), approche alternative proposée récemment pour écrire les jonctions tunnel magnétiques (JTM). Mon objectif est de développer des modèles compacts pour ces deux technologies et d'explorer, par simulation, leur intégration dans les circuits non-volatiles.

J'ai d'abord étudié les modèles physiques qui décrivent les comportements électriques des JTF : la résistance tunnel, la dynamique de la commutation ferroélectrique et leur comportement memristif. La précision de ces modèles physiques est validée par leur bonne adéquation avec les résultats expérimentaux. Afin de proposer un modèle compatible avec les simulateurs électriques standards, nous j'ai développé les modèles physiques mentionnés ci-dessus en langue Verilog-A, puis je les ai intégrés ensemble. Le modèle électrique que j'ai conçu peut être exploité sur la plate-forme Cadence (un outil standard pour la simulation de circuit). Il reproduit fidèlement les comportements de JTF.

Ensuite, en utilisant ce modèle de JTF et le design-kit CMOS de STMicroelectronics, j'ai conçu et simulé trois types de circuits: i) une mémoire vive (RAM) basée sur les JTF, ii) deux systèmes neuromorphiques basés sur les JTF, l'un qui émule la règle d'apprentissage de la plasticité synaptique basée sur le décalage temporel des impulsions neuronale (STDP), l'autre mettant en œuvre l'apprentissage supervisé de fonctions logiques, iii) un bloc logique booléen basé sur les JTF, y compris la démonstration des fonctions logiques NAND et NOR. L'influence des paramètres de la JTF sur les performances de ces circuits a été analysée par simulation.

Finalement, nous avons modélisé la dynamique de renversement de l'aimantation dans les dispositifs à anisotropie perpendiculaire à transfert de spin assisté par effet Hall de spin dans un JTM à trois terminaux. Dans ce schéma, deux courants d'écriture sont appliqués pour générer l'EHS et le TS. La simulation numérique basée sur l'équation de Landau-Lifshitz-Gilbert (LLG) démontre que le délai d'incubation de TS peut être éliminé par un fort EHS, conduisant à la commutation ultra-rapide de l'aimantation, sans pour autant requérir une augmentation excessive du TS. Nous avons appliqué cette nouvelle méthode d'écriture à la conception d'une bascule magnétique et d'un additionneur 1 bit magnétique. Les performances des circuits magnétiques

assistés par l'EHS ont été comparés à ceux écrits par transfert de spin, par simulation et par une analyse fondée sur le modèle théorique.

Mots clés : jonction tunnel ferroélectrique, jonction tunnel magnétique, Effet Hall de spin, transfert de spin, modèle compacte, circuits non-volatiles.

Chapter 1
General introduction

Background

According to the recent prediction by International Technology Roadmap for Semiconductors (ITRS) [1], the static power consumption of System-on-chip (SoC) Consumer Portable chips will dramatically increase in the next decade. For instance, it was predicted that the memory static power in 2026 will be triple that in 2016 (3 W versus 1 W, see Figure *SYSD6* in Ref. [1]). Such a trend is attributed to the fact that leakage current of transistors makes an increasing contribution to the total power consumption with the shrinking feature size of complementary metal-oxide-semiconductor (CMOS) process [2], especially below 90 nm technology node. The growth of static power limits the application prospect of the CMOS circuits, and it urgently needs to be addressed with alternative design.

In the modern CMOS-based digital systems (e.g. microprocessors), memories are the main sources of static power consumption since they store a large number of data which must be maintained by an ongoing power supply. Accordingly, this type of memories is called volatile memories. In contrast, non-volatile memories (NVMs) can retain the stored information without the need of an activated power supply. Therefore, a promising approach for reducing the static power consumption is to replace volatile memories with NVMs. In this background, the present thesis focuses on the study of two types of NVM devices: ferroelectric tunnel junctions (FTJs) and magnetic tunnel junctions (MTJs).

Motivation

The FTJ is an emerging NVM device which utilizes the ferroelectric polarization to store the information [3]–[4]. Actually the concept of the FTJ is not an emerging idea, which has been proposed by *L. Esaki* early in 1971 [5]. However, the experimental demonstration was not implemented until the 2000s [6]–[10] due to the difficulty in fabricating ultrathin ferroelectric films. Since 2000s, FTJs have attracted more and more research interests due to its promising performance. For instance, fast switching of 10 ns and high OFF/ON resistance ratio up to the order of 100 have been demonstrated in a recent FTJ prototype [10]. In 2011, the FTJ was listed as one of “emerging research devices” by ITRS report [11]. More attractively, it was recently found that some FTJs are essentially memristors [12]–[15], a kind of nonlinear circuit elements whose resistance can be continuously adjusted according to their current or voltage history [16]–[18]. Thanks to the memristor-like characteristic, the FTJ can be used as a synapse in neuromorphic systems [19] and thus prompts the research of another emerging field: memristor-based neuromorphic systems.

Nevertheless, the FTJ research is still in its infancy. In particular, the application of FTJs in memories and logic circuits has not been sufficiently studied. Currently most effort is devoted to the performance improvement of the single FTJ nanopillar. Therefore, it is necessary to expand the FTJ research from device level to circuit level. The application potential of FTJs in various circuits and systems (e.g. memories and neuromorphic systems) needs to be assessed. Such a situation prompts us to develop an electrical model for the FTJ and to explore its potential applications in NVMs and NV logic circuits (NVLs).

The MTJ is another promising NVM device which stores the data with magnetization state [20]–[21]. The concept of the MTJ was proposed almost as early as that of the FTJ, which can be traced back to 1975 when *Jullière* reported the first tunnel magnetoresistance effect (TMR effect, will be detailed in Chapter 2) at low temperature (4.2 K) [20]. But the research on the MTJ bloomed earlier than the FTJ, since the room-temperature TMR effect was demonstrated for the first time in 1995 [22]–[23], earlier than the first experimental demonstration of the FTJ in the 2000s. So far, the application of MTJs has been extended to magnetoresistive random access memory (MRAM) [24] and magnetic logic circuits [25]. Various demonstrators and even commercial products [26] have been developed.

One ambitious goal of MRAM development is to substitute for volatile dynamic or static random access memories (SRAMs or DRAMs). But current technologies still have a gap compared with this goal. In particular, the write technology of MTJs desires further breakthrough. Currently, mainstream write approach for the MTJ is spin-transfer torque (STT, will be detailed in Chapter 2) [27]–[29], but it suffers from a large incubation delay and a high risk of barrier breakdown. Recently strong spin-orbit interaction in the heavy metal was experimentally [30]–[33] and theoretically [34] studied to provide novel methods of magnetization switching and to overcome the drawbacks of the STT. These progresses drive us to focus on a promising write approach called spin-Hall-assisted STT for the perpendicular-anisotropy MTJ (p-MTJ), which was originally proposed in Ref. [34]. We expect that spin-Hall-assisted STT can improve the write performance of MRAM or magnetic logic circuits compared with the conventional STT.

Objectives and methods

The above-mentioned motivation sets three objectives for the present thesis:

First, an electrical model of the FTJ needs to be developed in order to bridge the gap between physical behaviors and electrical properties. This model is also indispensable to design and analyze the FTJ-based circuits and systems.

Second, we aim to apply the FTJ to three fields: random access memory (RAM), neuromorphic systems and NV Boolean logic block, where FTJs serve various roles. The influence of FTJ parameters on the performance of these systems should be discussed and analyzed.

Finally, spin-Hall-assisted STT needs to be studied from the viewpoint of magnetization dynamics. Performance improvement over the conventional STT should be validated in some NV applications such as magnetic flip-flop (MFF) and magnetic full-adder (MFA).

These objectives were achieved through the simulation research based on computer-aided design (CAD) software. In the FTJ modeling terms, the experimental results to be fit were extracted from the published literatures. The electrical model was programmed with *Verilog-A* language [35], which is compatible with standard circuit simulation tools. The magnetization dynamics driven by spin-Hall-assisted STT was studied by the numerical simulation based on a modified Landau-Lifshitz-Gilbert (LLG) equation (an equation describing magnetization dynamics, will be detailed in Chapter 2) [36]. An electrical model of spin-Hall-assisted STT-MTJ was developed also with *Verilog-A* language. Hybrid CMOS/FTJ and CMOS/MTJ circuits were designed on *Cadence* platform by using *STMicroelectronics* CMOS 40 nm and 28 nm design kits [37]–[38] in combination with the developed FTJ or MTJ models. Circuit simulation was performed with *Spectre* simulator.

Organization of the present thesis

The present thesis is divided into six chapters as follows.

This chapter presented the background, motivation, objectives and methods.

In Chapter 2, the state-of-the-art of FTJs and MTJs will be reviewed. The basic principle and key technologies related to our work will also be introduced.

In Chapter 3, we will develop a compact electrical model of the FTJ based on related physical theories. The developed model can be well fit to the experimental results extracted from Refs. [10] and [12]. Finally, we will perform single-cell simulation to validate the accuracy and applicability of our developed model.

In Chapter 4, we will design, simulate and analyze hybrid FTJ/CMOS circuits with the developed FTJ model and *STMicroelectronics* CMOS 40 nm design kit. Four circuits or systems will be studied including an FTJ-based random access memory (FTRAM), two FTJ-based neuromorphic systems and an FTJ-based Boolean logic block. Performance analysis for these circuits and systems will be presented as well.

In Chapter 5, based on a modified LLG equation, we will perform numerical simulation to analyze the magnetization dynamics driven by spin-Hall-assisted STT in a p-MTJ. Then we will

develop an electrical model of the spin-Hall-assisted STT-MTJ for the further circuit simulation. By using the developed model and *STMicroelectronics* CMOS 28 nm design kit, we will design and simulate an MFF and an MFA with spin-Hall assistance. Performance comparison between these spin-Hall-assisted magnetic circuits and the conventional STT ones will be discussed based on simulation results.

In Chapter 6, we will summarize the present thesis with conclusions and perspectives.

Chapter 2 State-of-the-art

2.0 Preface

This chapter reviews the history and current status of FTJs and MTJs. The preliminary knowledge for understanding the basics of these two devices is presented as well. In addition, some key technologies involved in the device application are discussed.

2.1 Ferroelectric tunnel junctions (FTJs)

2.1.1 Structure and working principle

Generally, the core structure of an FTJ is composed of ferroelectric ultrathin film sandwiched between two metals (M/FE/M structure) [3], as shown in Figure 2.1(a). The ferroelectric film acts as a barrier through which electrons can flow by means of tunneling effect. The ferroelectric barrier has a spontaneous polarization arising from the displacement of cation with respect to its centrosymmetric position (see Figure 2.1(a) showing an example of barium titanate $BaTiO_3$). This spontaneous polarization can be switched between two directions, as shown in Figure 2.1(b). The polarization switching can be achieved by applying an external voltage or mechanical stress. In the present thesis, mechanical properties are not discussed and thus the switching of an FTJ is voltage-driven. The polarization switching induces the modulation of the barrier potential profile so that the probabilities of electron tunneling are different for the opposite polarization orientations. As a consequence, the tunneling resistance of an FTJ can be switched between ON (low-resistance) and OFF (high-resistance) states by applying an external voltage, which is so-called tunnel-electroresistance (TER) effect [39]. Accordingly, OFF/ON resistance ratio is defined as TER ratio. TER effect enables the FTJ to store 1-bit binary information. Moreover, the storage is non-volatile as the spontaneous polarization can remain in the absence of the external voltage, which allows the FTJ to be applied in the NVMs and NVLs.

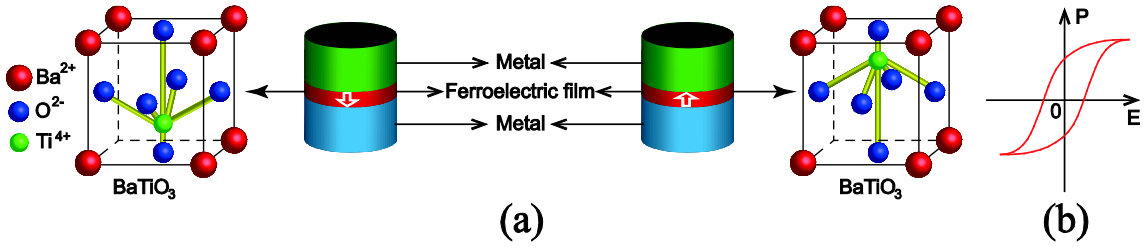


Figure 2.1 (a) Core structure of a typical FTJ. In the left and right sides, $BaTiO_3$ is taken as example to show the lattice of the polarized ferroelectric barrier. (b) Polarization-electric field (P-E) hysteresis loop of the ferroelectric barrier.

To fabricate an FTJ, two requirements are obligatory: first, the ferroelectric film must be thin enough to make electron tunneling feasible. Second, two barrier/metal interfaces must be asymmetric to generate unequal potential barrier heights for the opposite polarization orientations. The detailed working principle will be described below.

Figure 2.2 illustrates the potential profile of an FTJ for the opposite polarization orientations in the absence of the applied voltage. Here two metals (M1 and M2) are designed with different materials to produce asymmetric interfaces. As mentioned above, the potential profile varies when ferroelectric polarization is reversed. The factors modulating the potential profile include, but not limited to [3], [39]–[40]: i) the polarization reversal; ii) the barrier thickness variation caused by converse piezoelectric effect; iii) the change of barrier/electrode interfaces induced by imperfect screening of polarization charges. Among them, the third one is considered to be a dominant factor responsible for TER effect, as discussed below.

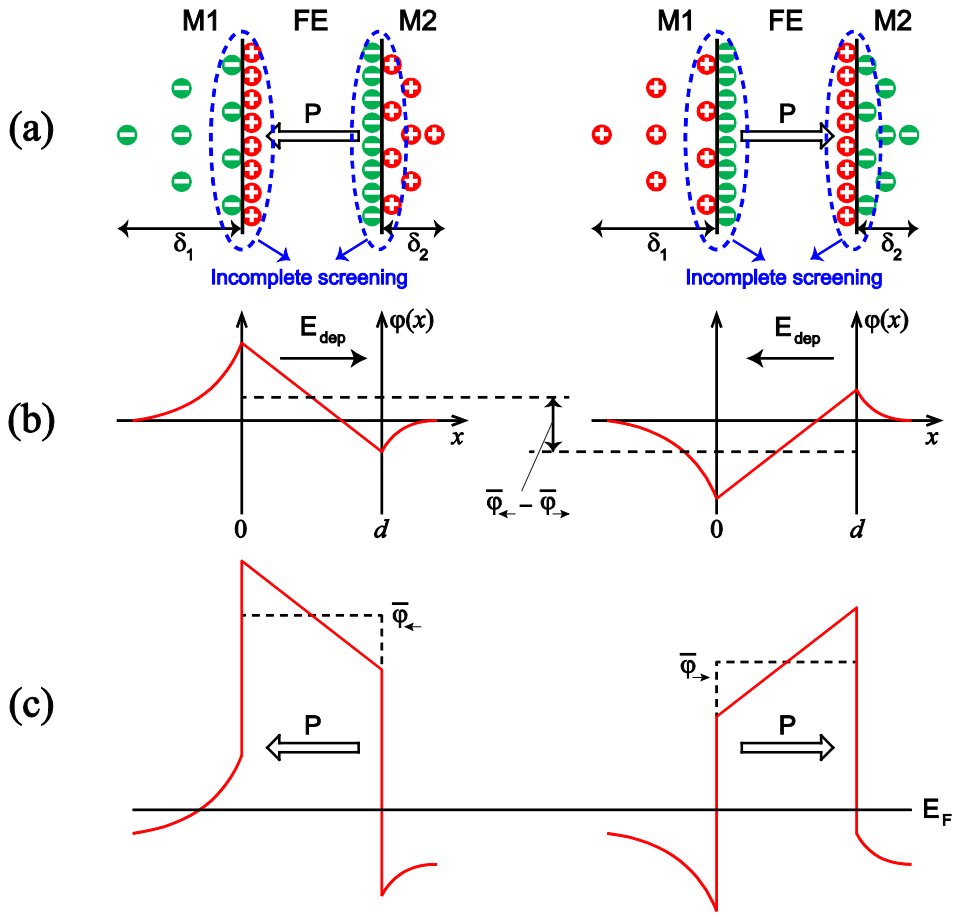


Figure 2.2 (a) Distribution of polarization charges and screening charges at two barrier/metal interfaces, (b) electrostatic potential induced by asymmetric charge screening, (c) Overall potential profile of the FTJ [39].

As shown in Figure 2.2(a), the ferroelectric polarization induces surface charges at the barrier/metal interfaces. These surface charges have to be screened by the charges from the metals. However, the screening is incomplete because the screening charges in one metal usually distributes over a finite distance from the interface, which is called screening length (δ_1 and δ_2 in Figure 2.2(a)). We assumed that there is no other interface effect influencing the distribution of charges. In this case, the incomplete charge screening at barrier/metal interfaces gives rise to a depolarization field [41] opposing the ferroelectric polarization (E_{dep} in Figure 2.2(b)). We also assumed that the depolarization field is the only origin of the tilting of electrostatic potential inside the ferroelectric film. Then, since the screening lengths are unequal for the two metals M1 and M2, electrostatic potential at two barrier/metal interfaces is asymmetric, as shown in Figure 2.2(b). Under these conditions, if the FTJ is short circuited, the electrostatic potential profile ($\varphi(x)$) can be given by a simple Thomas-Fermi model [39], as

$$\varphi(x)=\begin{cases} \pm\dfrac{\sigma_s\delta_1}{\varepsilon_0}\exp\left(\dfrac{x}{\delta_1}\right), & x\le 0 \\ \mp\dfrac{\sigma_s}{\varepsilon_0 d}\left[x\left(\delta_1+\delta_2\right)-\delta_1 d\right], & 0<x<d \\ \mp\dfrac{\sigma_s\delta_2}{\varepsilon_0}\exp\left(-\dfrac{x-d}{\delta_2}\right), & x\ge d \end{cases} \tag{2.1}$$

where δ_1 and δ_2 are the Thomas-Fermi screening lengths in M1 and M2, σ_s is the screening charge per unit area, ε_0 is the vacuum permittivity, d is the FE film thickness. The upper and lower signs ($\pm$ or $\mp$) correspond to the cases where polarization towards M1 and M2, respectively.

The overall potential profile is shown in Figure 2.2(c), which is the superposition of the potential barrier created by the FE film, the difference of Fermi energy between two metals, and $\varphi(x)$. With Eq. (2.1), the average potential barrier heights for the opposite polarization orientations ($\bar{\varphi}_{\leftarrow}$ and $\bar{\varphi}_{\rightarrow}$, see Figure 2.2(c)) are calculated by

$$\begin{cases} \bar{\varphi}_{\leftarrow}=U+\dfrac{\sigma_s}{2\varepsilon_0}\left(\delta_1-\delta_2\right), & \text{polarization towards M1} \\ \bar{\varphi}_{\rightarrow}=U+\dfrac{\sigma_s}{2\varepsilon_0}\left(\delta_2-\delta_1\right), & \text{polarization towards M2} \end{cases} \tag{2.2}$$

where U is the sum of other contributions to potential profile except for $\varphi(x)$.

Since $\delta_1 \neq \delta_2$, the average potential barrier heights are different for the opposite polarization orientations (i.e. $\bar{\varphi}_{\leftarrow} \neq \bar{\varphi}_{\rightarrow}$, see Figure 2.2 (b)–(c)). Accordingly, tunneling resistances are also different due to the exponential dependence of the tunneling current on the square root of the

potential barrier height [42]. This is the source of TER effect in an FTJ. Conversely, if two metals are identical and corresponding barrier/metal interfaces are symmetric, $\delta_1 = \delta_2$ and $\bar{\varphi}_{\leftarrow} = \bar{\varphi}_{\rightarrow}$, the tunneling resistances are identical for the opposite polarization orientations and thus there is no TER effect. In reality, the interfacial condition is more complicated than the ideal assumptions, thus the unequal potential barrier is not always from the use of different metal materials [4]. In one word, asymmetric barrier/metal interface plays a dominant role in generating the TER effect.

Note that although both the conventional ferroelectric capacitor (FeCap) and FTJ store non-volatile information through the ferroelectric polarization, yet their readout operations are totally different [43]–[44]. The ferroelectric film of the FeCap is thicker (typically 100 nm) than that of the FTJ, it is thus impossible that electron tunneling occurs through such a thick barrier in the FeCap. For reading the information stored in a FeCap, a voltage larger than coercive voltage is applied across the ferroelectric barrier, resulting in a transient current flowing through the external circuit (see Figure 2.3(a)). During this process, the transferred charges (Q) are given by [44]

$$Q = \frac{\varepsilon V A}{d} + (\Delta P) A \tag{2.3}$$

where the first item is the charges for the dielectric response, the second item is the charges for the switching current. ε is the absolute permittivity of the ferroelectric film, V is the applied voltage, A is the FeCap area, ΔP is the polarization change. Depending on the relative orientation between the applied voltage and the initial polarization, the ferroelectric polarization is reversed or remains unchanged, accordingly $\Delta P = 2P_s$ or $\Delta P = 0$ (P_s is the spontaneous polarization). As a consequence, the transient currents are different for the opposite initial polarization orientations. The stored information can be read by comparing the transient currents.

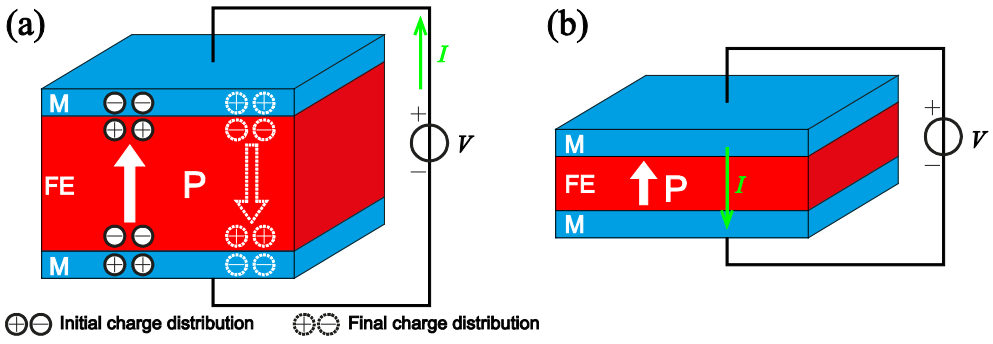


Figure 2.3 Comparison of the readout operation between the FeCap (a) and FTJ (b) [43].

The readout operation of the FeCap brings two drawbacks: first, since the polarization is possibly reversed during the readout, the stored information is destroyed (destructive readout),

which requires an additional reset operation to restore the initial polarization after the readout operation. Second, since the readout is performed by sensing the charges, the cell area must be large enough to provide detectable charges, which limits the scaling of the FeCap. The FTJ can overcome these drawbacks because: the information stored in an FTJ is read by measuring the tunneling resistance (see Figure 2.3(b)) and therefore the read voltage can be small to avoid destabilizing the polarization, achieving non-destructive readout. Moreover the FTJ has better scaling capability than the FeCap thanks to its larger readout current density.

2.1.2 Proposal and implementation of FTJs

2.1.2.1 Critical thickness for ferroelectricity

As mentioned in Chapter 1, the concept of the FTJ appeared early in 1971, when *L. Esaki* proposed a tunnel device whose resistance states can be switched by reversing the polarization of the ferroelectric barrier. This device was named "polar switch" and was considered the prototype of the FTJ [5]. But in the subsequent 30 years, the fabrication of the FTJ was not realized due to a technological paradox: on the one hand, the FTJ requires a thin enough barrier to enable the electron tunnel effect; on the other hand, as the ferroelectricity is a cooperative phenomenon, the polarization in a thin ferroelectric film is apt to collapse due to depolarization field and finite-size effects [45]. The minimal thickness for holding stable polarization is called critical thickness. In 1972, *Batra* and *Silverman*'s theoretical calculation suggested that the critical thickness of triglycine sulphate (a ferroelectric material) is 400 nm [46]. Such a large thickness predetermined the unfeasibility of the FTJ. Therefore little effort was devoted to the FTJ research until the critical thickness was experimentally decreased to several nanometers in the 2000s.

Table 2.1 summarizes some important achievements in reducing the critical thickness of the ferroelectric film. These technical progresses made it feasible to keep the ferroelectricity in a film with a thickness of only a few unit cells. In this context, the FTJ research revived from theoretical prediction [3], [39]–[40], [56] to experimental demonstration [6]–[10], [12]–[15], [57]–[77].

Table 2.1 Demonstrated critical thickness of the ferroelectric film

Year	Group	Material	Thickness	Reference
1996	*J. Karasawa* et al.	$PbTiO_3$	10 nm	[47]
1998	*T. Maruyama* et al.	$PbZr_{0.25}Ti_{0.75}O_3$	10 nm	[48]
1999	*N. Yanase* et al.	$BaTiO_3$	12 nm	[49]
1999	*T. Tybell* et al.	$Pb(Zr_{0.2}Ti_{0.8})O_3$	4 nm	[50]
2003	*J. Junquera* et al.	$BaTiO_3$	2.4 nm	[51]*

2004	*D. D. Fong* et al.	$PbTiO_3$	1.2 nm	[52]
2005	*N. Sai* et al.	$PbTiO_3/BaTiO_3$	1 nm	[53]*
2006	*L. Despont* et al.	$PbTiO_3$	1.2 nm	[54]
2006	*D. A. Tenne* et al.	$BaTiO_3$	0.4 nm	[55]

* Based on the theoretical calculation.

2.1.2.2 General FTJs

In 2003, the authors of Ref. [6] claimed the first experimental demonstration of the FTJ, which was fabricated with a $Pb(Zr_{0.52}Ti_{0.48})O_3$ barrier and achieved an OFF/ON resistance ratio of 400% at room temperature. However, in 2008 the same group suggested that the origin of resistive switching of their first FTJ is possibly not ferroelectricity due to the insufficient evidence [57]. They pointed out that it is necessary to monitor simultaneously the current-voltage (I-V) characteristic and polarization hysteresis loop to confirm the correlation between the resistive switching and ferroelectricity.

In 2009, the direct evidence for polarization-induced resistive switching was experimentally demonstrated by three groups [7]–[9]. In Ref. [7] a sharp metal tip was placed above 30 nm-thick $Pb(Zr_{0.2}Ti_{0.8})O_3$ (PZT) film so that electrons were injected from the tip into PZT by means of Fowler-Nordheim tunneling (FNT) [58]. The polarization reversal induced a 500-fold change in tunneling current. In Ref. [8] the conductive-tip was contacted to $BaTiO_3$ (BTO) films of various thicknesses (1~3 nm). By applying a voltage across the tip and substrate, electrons flowed through BTO by direct tunneling (DT). OFF/ON ratio as high as 750 was reached in a 3 nm-thick film. The authors of Ref. [9] also independently observed TER effect and obtained an OFF/ON ratio of 80 with a 4.8 nm-thick BTO barrier. In 2010, an OFF/ON ratio of 500 was achieved through a 3.6 nm-thick $PbTiO_3$ (PTO) barrier [59] by the same group as Ref. [8]. All these experiments provided the comparison of the results between ferroelectric polarization and tunneling current to prove the dominant role of ferroelectricity in the observed resistive switching. Nevertheless, these results were obtained at the material level instead of device level. That is to say, resistive switching occurred at the local region (near the tip) of a bare ferroelectric film, as shown in Figure 2.4(a). There was no solid-state FTJ with well-defined electrodes demonstrated (see Figure 2.4(b)).

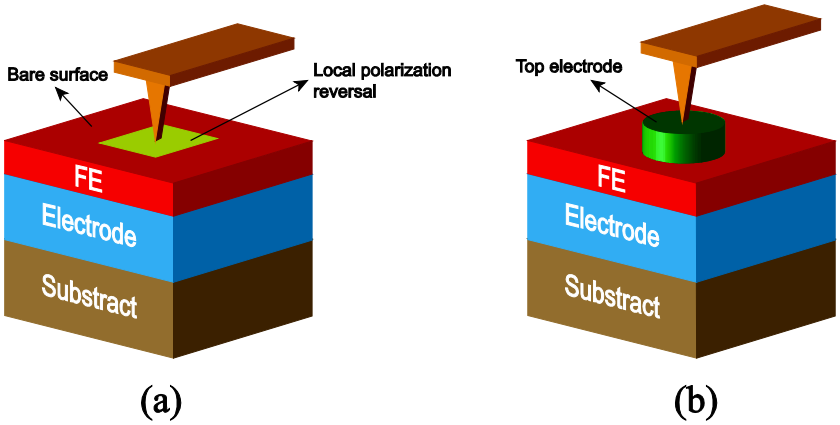


Figure 2.4 TER effect is observed in two experimental environments: (a) a bare FE material is contacted with a measuring tip, (b) FE film is sandwiched between two electrodes to form an authentic solid-state FTJ.

In 2011, resistive switching was demonstrated with a Cu/BTO/$La_{0.7}Sr_{0.3}MnO_3$ (LSMO) structure [60], but it was attributed to thermionic injection instead of electron tunneling due to the relative thick barrier (9 nm). Until 2012, the first solid-state FTJ intended to the memory application was reported in Ref. [10]. It used a Co/BTO(2 nm-thick)/LSMO structure and exhibited a large OFF/ON ratio (~100), high switching speed (~10 ns under 4 V bias) and low write current density (~10^4 A/cm^2). Since then, more solid-state FTJs have been demonstrated by different groups [12]–[14], [61]–[72]. Some of them are summarized in Table 2.2. Although so rapid progresses have been made, some crucial performance metrics of FTJs are still far away from the requirements of the integrated circuits. For instance, FTJs suffer from the polarization relaxation which results in poor data retention [65]. Their endurance is also inferior to other NV memories (e.g. ~10^6 cycles in Ref. [66], which are the best results so far). Hence, fabricating high-performance FTJ nanopillars remains the top priority for this field.

Table 2.2 Solid-state FTJs developed by several groups

Year	Structure	Barrier thickness	Diameter or area	R.A* product for ON state	TER ratio	Ref.
2012	Co/BTO/LSMO	2 nm	0.5 μm	~20 kΩ · μm^2	~100	[10]
2012	Co/PZT/LSMO	1.2–1.6 nm	0.04 μm^2	~6 MΩ · μm^2	~300	[61]
2012	Ag/BTO/SRO*	3 nm	20 nm	–	~100	[62]
2012	Co/BTO/LSMO	1.6–3.2 nm	5 μm	20~100 MΩ · μm^2	~1000	[13]
2013	Co/BFO/CCMO*	4.6 nm	0.18 μm	~2 kΩ · μm^2	~10000	[14]
2013	Cr/BTO/Pt	3 nm	0.8 μm	~300 MΩ · μm^2	~30	[64]

*Some abbreviations: R.A–Resistance-area, SRO–$SrRuO_3$, BFO–$BiFeO_3$, CCMO–$Ca_{0.96}Ce_{0.04}MnO_3$

2.1.2.3 Special FTJs

For those FTJs mentioned in Section 2.1.2.2, TER effect originates from the modulation of potential barrier height in response to the polarization reversal. This mechanism exactly follows the original theoretical description of TER effect mentioned in Section 2.1.1 [3], [39]–[40]. This is the reason why we call them "general FTJs". Actually, ferroelectric polarization can also be used for tuning the other properties to generate TER effect in FTJs, which we call "special FTJs".

In Ref. [67], a layer of $La_{0.5}Ca_{0.5}MnO_3$ (LCMO) was inserted between the ferroelectric barrier (BTO) and an electrode (LSMO) to form a structure shown in Figure 2.5. The LCMO layer was deliberately designed at the transition state between the ferromagnetic-metallic phase and antiferromagnetic-insulating phase. When the ferroelectric polarization points towards the LCMO layer, the charge screening leads to the electron accumulation or hole depletion in the LCMO layer, which drives the LCMO layer to ferromagnetic-metallic phase. In this case, the LCMO layer is considered a part of the electrode. Conversely, the LCMO layer becomes antiferromagnetic-insulating phase and acts as a part of the barrier. As a consequence, the barrier thickness can be changed by switching the polarization. Since the tunneling resistance is exponentially dependent on the barrier thickness [42], TER effect can be produced in this FTJ. Experimentally, an enhanced TER ratio up to 100 was obtained with 3 nm-thick BTO and 0.8 nm-thick LCMO.

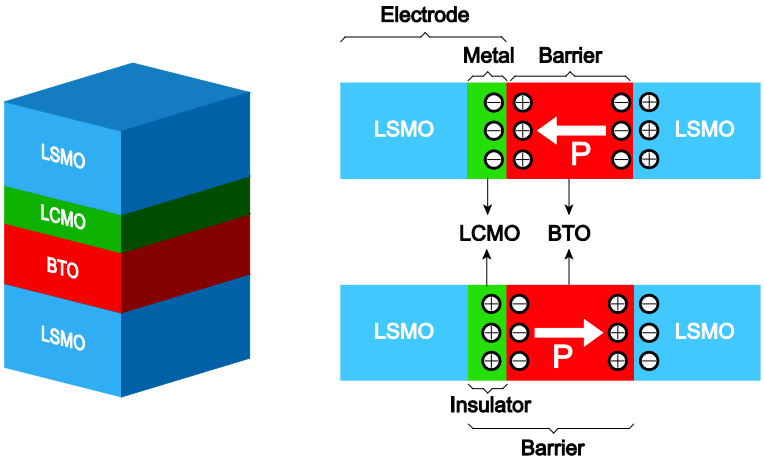


Figure 2.5 FTJ based on polarization-induced metal-insulator transition [67].

In Ref. [68], one of the electrodes in the FTJ was fabricated with Nb-doped $SrTiO_3$ (Nb:STO), which is a n-type semiconductor, as shown in Figure 2.6. Depending on the polarization directions, majority carriers (electrons) deplete or accumulate in the semiconductor layer. If deplete, the space charge region of the semiconductor layer creates an additional Schottky barrier added into the barrier. Conversely, the majority carriers accumulate within a thin region to eliminate the space

charge region and therefore only the ferroelectric layer is included into the barrier. As a result, TER ratio can be enhanced due to the polarization-induced change in barrier thickness, similar to aforementioned Ref. [67]. TER ratio as high as 10^4 was experimentally observed in this FTJ.

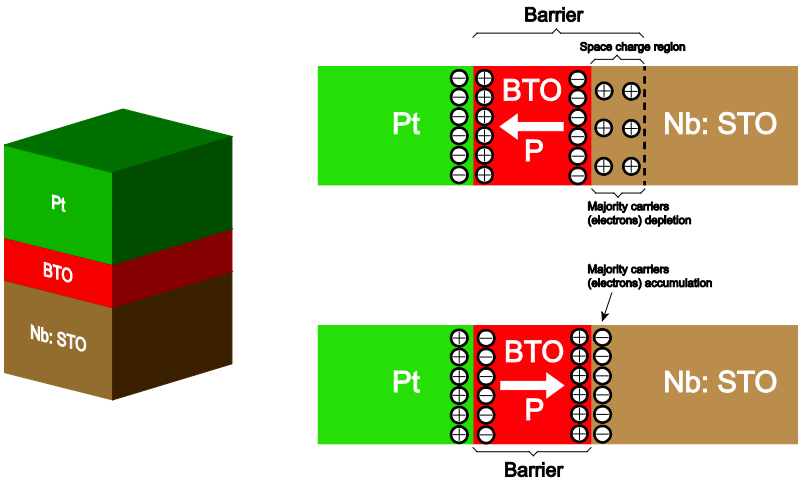


Figure 2.6 FTJ based on polarization-induced modulation of space charge region [68].

Besides the above-mentioned examples, there has been also other special FTJs demonstrated [15], [73]–[77]. Their common feature is that interface property is sensitive to the polarization reversal, which contributes to TER effect. These special FTJs extend the family of NV devices and enrich the ferroelectrics-based physics.

2.1.3 FTJs towards memristive device

In the previous sections, those FTJs are regarded as binary devices. Actually, many of them have the ability of multilevel storage. More exactly speaking, some FTJs are naturally memristors. To describe this issue, below we introduce briefly the concept of the memristor and then explain the memristive effect of FTJs.

2.1.3.1 Memristors

In 1971, the memristor was theoretically discovered by *L. Chua* as a nonlinear circuit element in addition to three basic linear ones: the resistor, the capacitor and the inductor [16]. Chua's theory is illustrated in Figure 2.7, where four basic circuit variables are defined: current i, voltage v, charge q, and magnetic flux φ. Each pair of variables is linked together by an equation. Hence six equations can be derived from different combinations. Among them, Eq. (2.4) describes an unknown circuit element at that time, which was named "memristor" by *Chua*.

$$\mathrm{d}\varphi = M\mathrm{d}q \tag{2.4}$$

where M is the memristance, it has the same unit (Ohm) as the resistance. But unlike the resistance, memristance is defined as a charge-dependent variable instead of a constant. Based on this definition, Eq. (2.4) is written as

$$\mathrm{d}\varphi = M(q)\mathrm{d}q \Rightarrow v\mathrm{d}t = M\left[q(t)\right]i\mathrm{d}t \Rightarrow \begin{cases} v(t) = M\left[q(t)\right]i(t) \\ \dfrac{\mathrm{d}q(t)}{\mathrm{d}t} = i(t) \end{cases} \tag{2.5}$$

where t is the time.

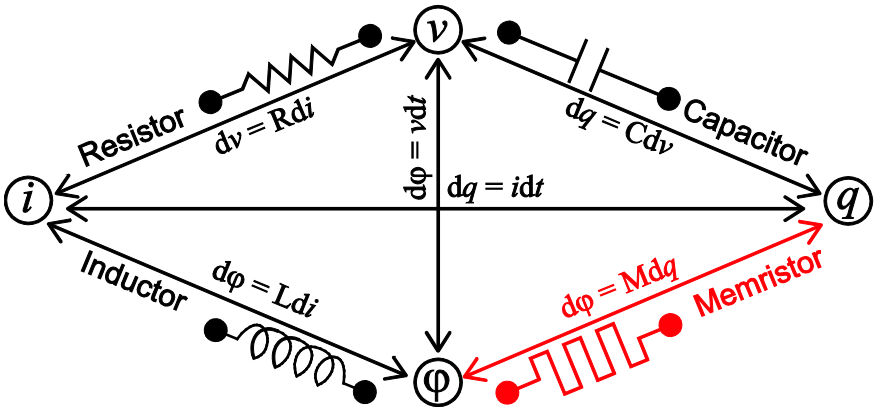


Figure 2.7 Six equations link four circuit variables and define four circuit elements.

Thus the memristor is considered a nonlinear device whose resistance is dependent on the current history. In 1976, *Chua* expanded the concept of the memristor to broader memristive systems [78], where charge q was replaced with an internal state variable w, as

$$\begin{cases} v(t) = R\left[w(t), i\right]i(t) \\ \dfrac{\mathrm{d}w(t)}{\mathrm{d}t} = f(w, i) \end{cases} \quad \text{or} \quad \begin{cases} v(t) = R\left[w(t), v\right]i(t) \\ \dfrac{\mathrm{d}w(t)}{\mathrm{d}t} = f(w, v) \end{cases} \tag{2.6}$$

where two groups of equations describe the current-controlled and voltage-controlled memristive systems, respectively. $f(\cdot)$ is a system-dependent function. Here we substitute R for M. Eq. (2.6) is a mathematical criterion for judging whether a device is a memristor or not. Recently, *Chua* provided a more intuitive definition: most resistive switching devices can be classified as memristors if their I-V pinched hysteresis loops can be adjusted by frequency or amplitude of applied pulses [17].

The memristor research is a similar story to that of FTJs. More than 30 years passed from the proposal of the memristor to the physical realization of the first passive memristor. In 2008, the scientists from *Hewlett-Packard* (*HP*) Labs claimed that they have fabricated the passive

memristor for the first time [18]. Their device modeling is illustrated in Figure 2.8, where a semiconductor film with a thickness of D was sandwiched between two metal electrodes. The semiconductor film includes two regions, one of which has a high concentration of dopants and the other has a low one. These two regions are possessed of high resistance and low resistance, respectively. When an external voltage is applied to the device, the boundary between two regions can be moved due to the drift of the charged dopants. Therefore this device is equivalent to two variable resistors connected in series. Based on the above analysis, *HP* scientists gave a group of equations to describe the I-V relationship, as

$$\begin{cases} v(t) = \left[R_{ON} \dfrac{w(t)}{D} + R_{OFF} \left(1 - \dfrac{w(t)}{D} \right) \right] i(t) \\ \dfrac{\mathrm{d}w(t)}{\mathrm{d}t} = \mu_V \dfrac{R_{ON}}{D} i(t) \end{cases} \tag{2.7}$$

where R_{ON} and R_{OFF} are the resistances corresponding to the fully-doped and fully-undoped states, respectively. μ_V is the average ion mobility, w is the width of the doped region. Eq. (2.7) has the same form as Eq. (2.6), proving that the proposed device is indeed a memristor with a state variable of w.

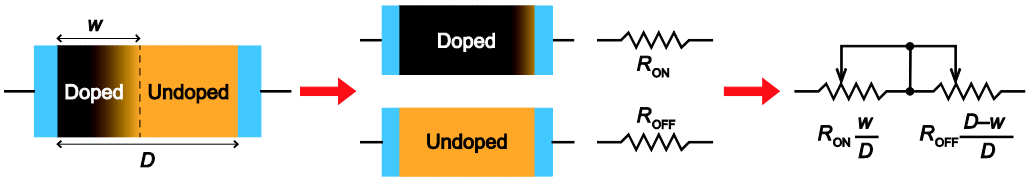


Figure 2.8 The model of the memristor developed by HP lab [18].

The finding of the memristor drives the development of many emerging fields. The fascinating one is in the high-density synapse array of neuromorphic systems [19]. More details about memristor-based neuromorphic system will be presented in Section 4.2. Here we just emphasize a fact that more and more types of memristors have sprung up and attracted much research interest from industry and academia [79] due to the great application potential. In this context, the memristive effect of FTJs was experimentally observed, as detailed below.

2.1.3.2 Memristive effect of FTJs

First of all, the switching process of ferroelectric polarization needs to be introduced since it is closely related to the memristive effect of FTJs. In a ferroelectric material, ferroelectric domain is a region in which dipoles have the same polarization direction. The boundary between neighboring

domains is called domain wall (see Figure 2.9). Experiment measurements demonstrate that polarization reversal is associated with the evolution of switched ferroelectric domain, including the nucleation, forward growth and sideways growth [45], [80]–[82], as shown in Figure 2.9. Since the FTJs use ultrathin films (< 5 nm), the delay of the forward growth can be neglected. Therefore the switching of the FTJ is mainly dominated by the domain nucleation and domain wall propagation. It is seen from Figure 2.9 that the opposite domains possibly coexist in the same film during the polarization reversal. In other words, the polarization is reversed continuously rather than abruptly under the action of an external voltage. Recall the above description that the electrical properties of some FTJs are directly controlled by the ferroelectric polarization, it is feasible that the FTJ resistance varies continuously with the gradual polarization reversal. Therefore the FTJ can be defined as a voltage-controlled memristor with a polarization-controlled state variable.

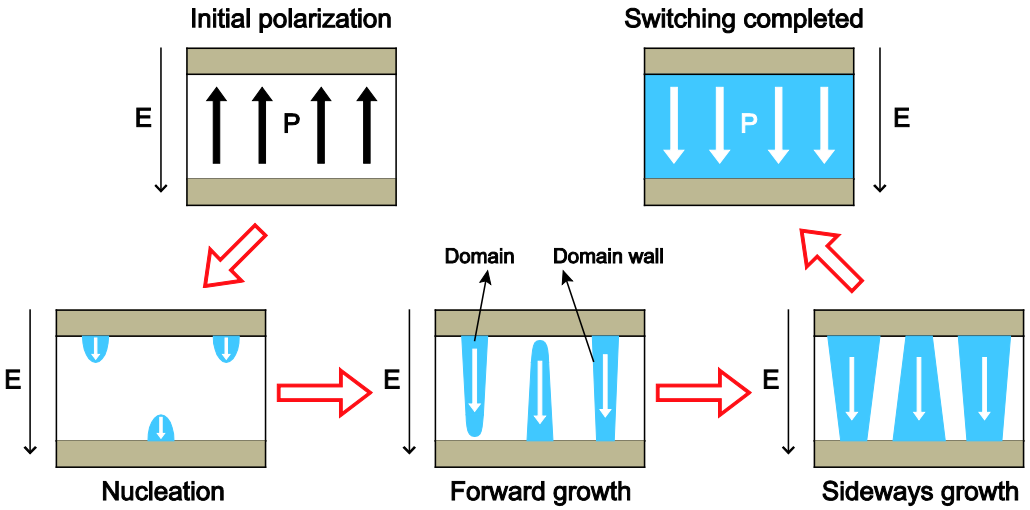


Figure 2.9 Polarization reversal driven by an external electric field (or voltage).

In Refs. [12] and [14], the FTJ was modeled as two resistors connected in parallel, as shown in Figure 2.10. Each resistor is represented by an FTJ full of ON-state or OFF-state domain. Under the action of an external voltage, the total resistance of the FTJ varies with the change in volume fraction of ferroelectric domain, as

$$\frac{1}{R} = \frac{1 - s_{OFF}}{R_{ON}} + \frac{s_{OFF}}{R_{OFF}} \tag{2.8}$$

where s_{OFF} are the volume fraction of the domain corresponding to OFF state. R_{ON} (R_{OFF}) is the resistance when FTJ is in fully-ON (fully-OFF) state. Hence s_{OFF} is regarded as the state variable for this memristor-like FTJ.

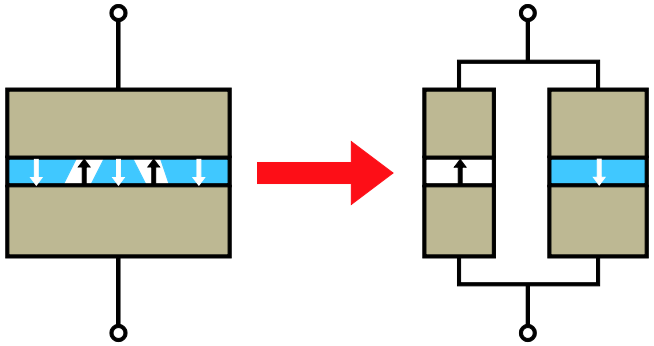


Figure 2.10 Schematic model for the memristive effect of FTJs in Refs. [12] and [14].

In Refs. [13] and [65], the memristive behavior of the FTJ was attributed to the charge migration and accumulation at barrier/metal interface. Depending on the polarity of the applied voltage, the charges/oxygen vacancies accumulate or dissipate at the interface, leading to a tunable barrier height and adjustable resistance.

In Ref. [15], the FTJ has the same structure as Figure 2.6. Since the width of the space charge region is determined by the amount of the polarization charges to be screened, the barrier thickness can be continuously tuned during the polarization reversal. Accordingly, the FTJ resistance also continuously varies with the polarization change, and the memristive behavior can be observed.

In summary, the continuously-adjustability of ferroelectric polarization enables the FTJ to work as a memristor. The application field of FTJs is extended thanks to the memristive effect.

2.2 Magnetic tunnel junctions (MTJs)

2.2.1 Structure and working principle

The core structure of an MTJ is shown in Figure 2.11(a), where an insulating barrier is sandwiched between two ferromagnetic (FM) layers [20]. The barrier is enough thin to enable the electron tunneling effect. Each FM layer has a magnetization which can be switched by a magnetic field between two stable directions along the anisotropy axis. In real electronic application, the magnetization of one FM layer is fixed and the other is switchable. The former is named the reference layer (RL, or pinned layer) while the latter is the free layer (FL). The magnetization of the FL can be switched to be parallel (P) or anti-parallel (AP) to that of the RL, which gives a low or high tunneling resistance (see Figure 2.11(b)). This resistance is specially called tunneling magnetoresistance (TMR). TMR ratio is the primary performance for an MTJ. It is defined as

$$TMR = \frac{\Delta R}{R_P} = \frac{R_{AP} - R_P}{R_P} \tag{2.9}$$

where R_P and R_{AP} are the resistances for P and AP states, respectively. TMR effect qualifies the MTJ as a binary non-volatile memory cell.

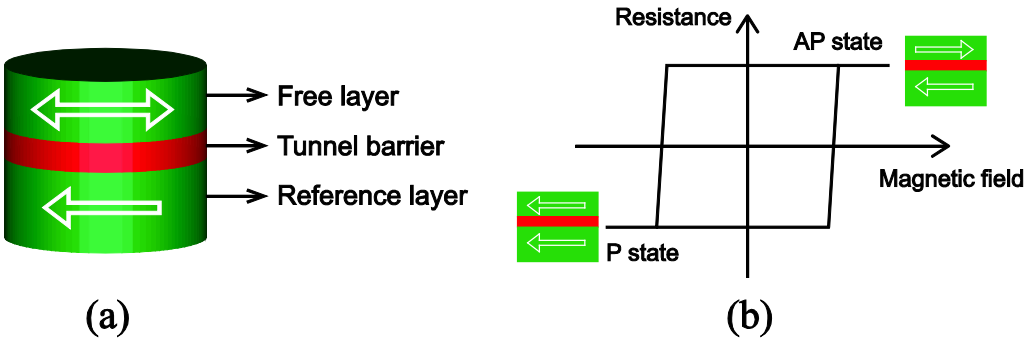


Figure 2.11 (a) Core structure of a typical MTJ, (b) TMR effect of the MTJ.

The mechanisms behind TMR effect is spin-dependent tunneling, which can be explained from the viewpoint of band structure, as illustrated in Figure 2.12. For an FM material, there is an imbalance between the populations of spin-up and spin-down at the Fermi level [21], [83]. The density of states available for spin-up is unequal to those for spin-down, resulting in a net magnetic moment and contributing to the magnetization of the FM material. The electrons near the Fermi level act as the carriers during the transport. Since the barrier is thin enough, the electron conserves its spin while it travels from one FM layer to the other one by tunneling effect. In other words, a spin-up electron can flow through the barrier if and only if it can find a spin-up state to occupy at the Fermi level of the other FM layer, so does spin-down electron. For the P state, the band structures of two FM layers are nearly identical, thereby all the spin-up or spin-down electrons from one FM layer can easily find an available state in the other FM layer. Conversely, in the AP state, only partial electrons can act as carriers for the tunneling current. As a consequence, the TMR for the P state is lower than that for the AP state.

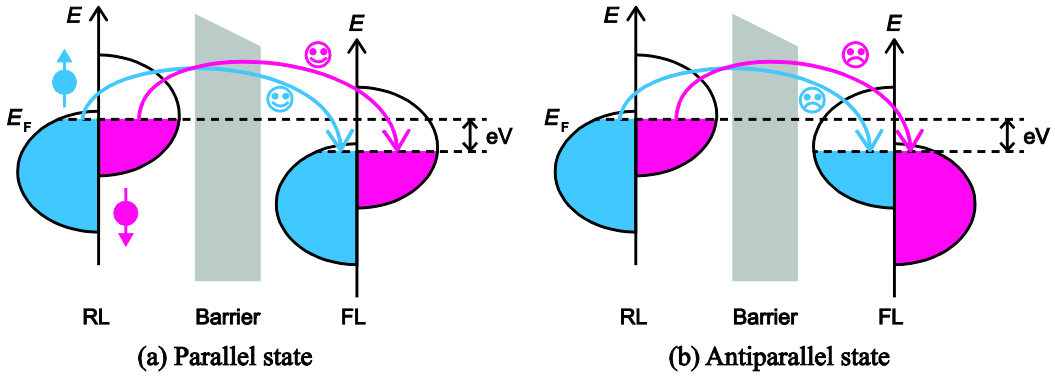


Figure 2.12 Spin-dependent tunneling in an MTJ.

The extent of band imbalance in an FM layer can be evaluated by the spin-polarization P, which is defined as

$$P = \frac{\left| n_{\uparrow} - n_{\downarrow} \right|}{n_{\uparrow} + n_{\downarrow}} \tag{2.10}$$

where $n_{\uparrow}$ and $n_{\downarrow}$ are the numbers of spin-up and spin-down carriers, respectively.

Analysis based on Figure 2.12 indicates that TMR effect is strongly dependent on the spin-polarization. *Jullière* developed a model to describe this dependence [20], as

$$\begin{cases} R_P = \dfrac{2}{1 + P_1 P_2} \\ R_{AP} = \dfrac{2}{1 - P_1 P_2} \end{cases} \Rightarrow TMR = \frac{2 P_1 P_2}{1 - P_1 P_2} \tag{2.11}$$

where P_1 and P_2 are spin-polarization in two FM layers. It is seen that the TMR ratio increases with the spin-polarization.

In addition, it is necessary to distinguish the TMR effect from giant magnetoresistance (GMR) effect, which is generated in metal multilayer films [84]–[86]. In the following text, this metal multilayer film is called GMR device. Similar to the MTJ, a typical GMR device has also two FM layers whose relative magnetization orientation (P or AP) determines the resistance state (low or high resistance). But there are mainly three differences between GMR devices and MTJs, as follows:

First, the GMR device uses a non-ferromagnetic (NFM) metal to separate two FM layers. Thus, electron passes through the device by *spin-dependent scattering*, as shown in Figure 2.13. But in an MTJ, the non-ferromagnetic metal is replaced with an insulator, and the electronic transportation mechanism is *spin-dependent tunneling*.

Second, in a GMR device, current can flow “in the layer plane” (CIP) or “perpendicular to plane” (CPP) [87], as shown in Figure 2.14. But for an MTJ, current passes through the device only perpendicularly.

Third, since each layer of the GMR device is conductor, it generally carries larger current than the MTJ. The GMR device is used for spin-valve read head in hard disk drive (HDD) [88]–[89]. The MTJ preferably acts as the memory cell in non-volatile MRAM [24].

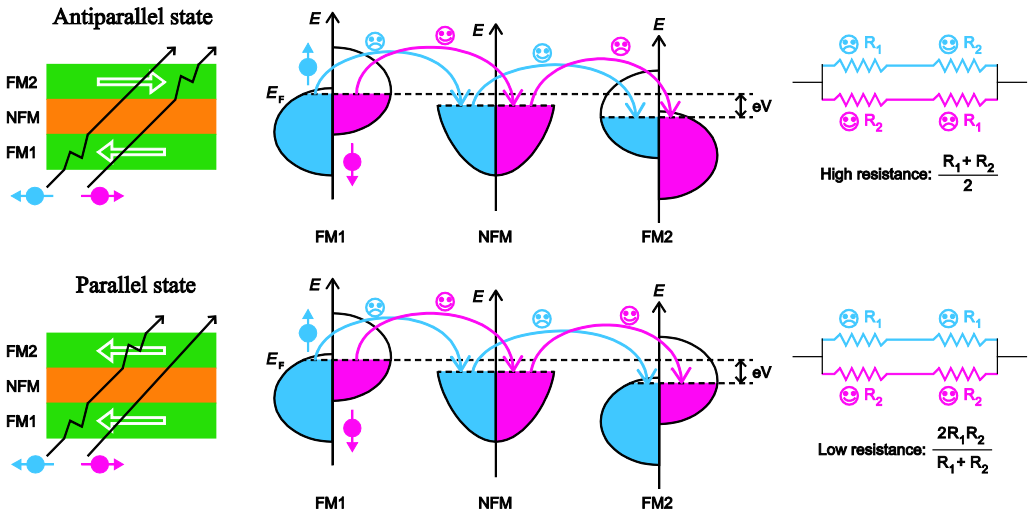


Figure 2.13 GMR effect induced by spin-dependent scattering.

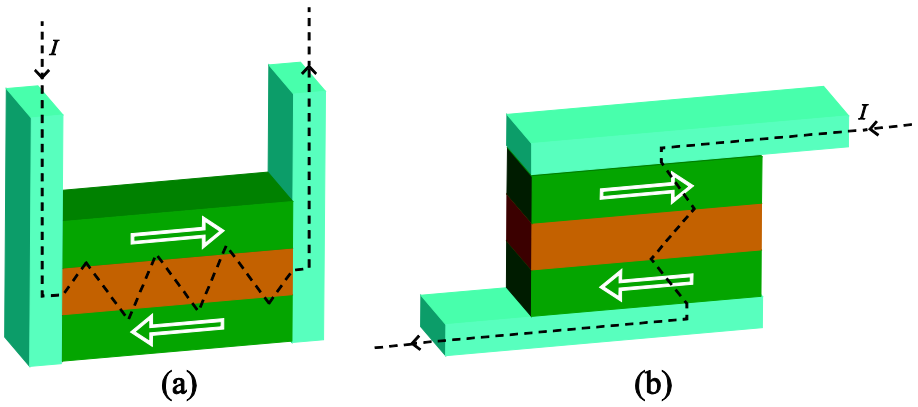


Figure 2.14 Two arrangements for GMR devices: (a) CIP and (b) CPP.

2.2.2 Main milestones in the MTJ development

MTJs and GMR devices flourish an emerging research field called "Spintronics", in which the spin plays a more dominant role than the charge in electron transport. Spintronics can be traced to the first experiment of measuring TMR effect by *Jullière* in 1975 [20], but its rise benefited from the observation of spin-injection by *M. Johnson* [90] and the discovery of GMR effect (2007 Nobel Prize in Physics) by *A. Fert* [84] and *P. Grunberg* [85] in the 1980s. These pioneering works made it possible to control the spin freedom in electronics. Up to nowadays, spintronics has a wide range of subjects and topics [91]–[93], and it is unnecessary to include all aspects in the present thesis. This section will focus on some crucial progresses in MTJ development, which are related to the topic of the present thesis.

2.2.2.1 Enhanced TMR effect

In 1975, for the first time, *Jullière* observed a TMR ratio of 16.3% (as the definition of Eq. (2.9)) in Fe/Ge/Co MTJ at low temperature (4.2 K) [20]. But it cannot be applied to real electronic devices which operate at room temperature (RT) and even higher. Moreover, the observed TMR ratio was much smaller than the predicted value by Jullière model (see Eq. (2.11)). The loss of TMR ratio was attributed to the small tunneling spin-polarization induced by non-ideal fabrication process [94]. In the subsequent years, much effort was devoted to the pursuit of larger TMR ratio at RT.

Significant progress was made in 1994 when large TMR ratio was obtained at RT (18% at 300 K [22] and 11.8% at 295 K [23]) by using amorphous Al_2O_3 insulating barrier. These results opened up the research of room-temperature TMR effect and attracted research interests to Al_2O_3-based MTJ. During that period, observed TMR ratio reached up to 70% in a CoFeB/Al_2O_3/CoFeB MTJ [95].

To further enhance the TMR effect, it was suggested that crystalline MgO should be used for the tunneling barrier to replace amorphous Al_2O_3. Theoretical calculation indicated that TMR ratio can reach the order of 100% even 1000% in a Fe/MgO/Fe MTJ [96]–[97]. The increase in TMR ratio is attributed to the filteration effect of the crystalline MgO: the electrons whose wave functions are symmetrical to the lattice have larger tunneling probabilities than those electrons without this symmetry. Such a symmetry difference makes an additional contribution to TMR ratio. But amorphous Al_2O_3 does not have the ability of filtering the symmetry of wave function, resulting in a smaller TMR ratio. These theoretical works prompted the first experimental demonstrations of giant TMR ratio using Fe/MgO/Fe (180% at RT) [98] and CoFe/MgO/CoFe (220% at RT) [99] in 2004. Since then, MgO has worked as the mainstream material for the MTJ barrier to keep large TMR ratio. So far, TMR ratio as high as 604% has been reported in a CoFeB/MgO/CoFeB MTJ [100].

2.2.2.2 Efficient write approaches

As mentioned in Section 2.2.1, the write operation of an MTJ is achieved by switching the FL magnetization. In the first-generation write approach called field-induced magnetic switching (FIMS), the magnetization switching is driven by an external magnetic field, which is induced by the currents flowing through two orthogonal write lines (digit and bit lines) [101], as illustrated in Figure 2.15(a). To switch an MTJ, two currents are applied to digit and bit lines in order to generate the hard-axis and easy-axis switching fields, respectively. The written state is determined by the polarity of the current flowing through the bit line. This write approach suffers from the

narrow operating window induced by half-selectivity disturbance. Researchers from *Freescale* improved this approach by using a synthetic antiferromagnet FL and proposed a novel toggle switching mode [102]. Based on this technology, *Freescale* launched the first commercial 4-Mbit MRAM product (No. MR2A16A). Nevertheless, FIMS requires large write current (~10 mA), resulting in the poor scalability due to the limit of electromigration.

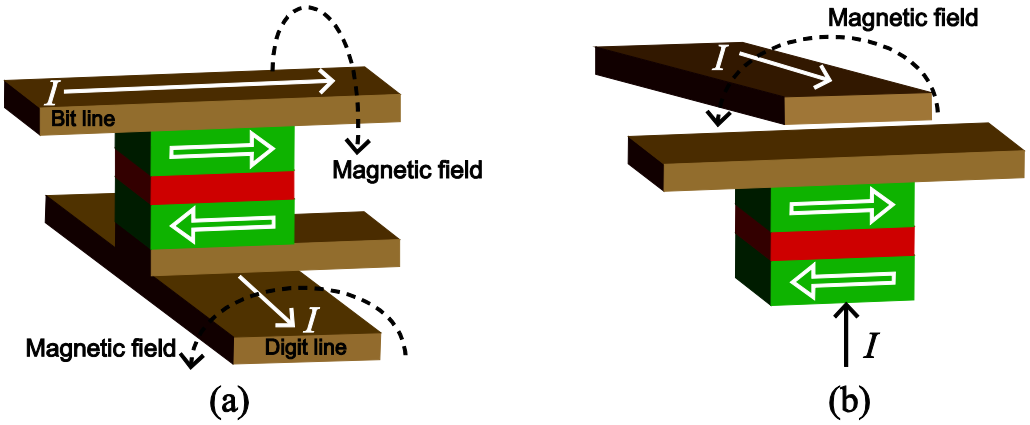


Figure 2.15 Write approaches for the MTJ: (a) FIMS and (b) TAS.

Thermal assisted switching (TAS) [103] is an improved write approach compared with the FIMS. Its procedure is shown in Figure 2.15(b), where one current flowing through the MTJ heats the FL and reduces the write field. In this way, one write line is enough to generate the switching magnetic field. TAS has lower write power than FIMS, but it still cannot overcome the scalability issue. In addition, TAS has lower write speed since it requires a cooling down after the heating.

For eliminating the drawbacks of FIMS and TAS, an alternative write approach without the need of magnetic field is desired. This idea was fulfilled by *Berger* and *Slonczewski*'s theoretical prediction [27]–[28], whose principle is illustrated in Figure 2.16. While electrons flow from the RL to FL, they are spin-polarized by the RL and acquire a spin angular momentum nearly aligned to the RL magnetization. After these spin-polarized electrons pass into the FL, their transverse angular momentum must be transferred to the FL magnetization due to the conservation of angular momentum. This transfer induces a torque to force the FL magnetization to be parallel to the RL one, and then the P state is written. Such a current-induced torque is named spin-transfer torque (STT). If the electrons flow along the opposite direction, they will be spin-polarized against the RL magnetization by the reflection from the RL (see Figure 2.16(b)). In this case the MTJ is switched to AP state by the STT.

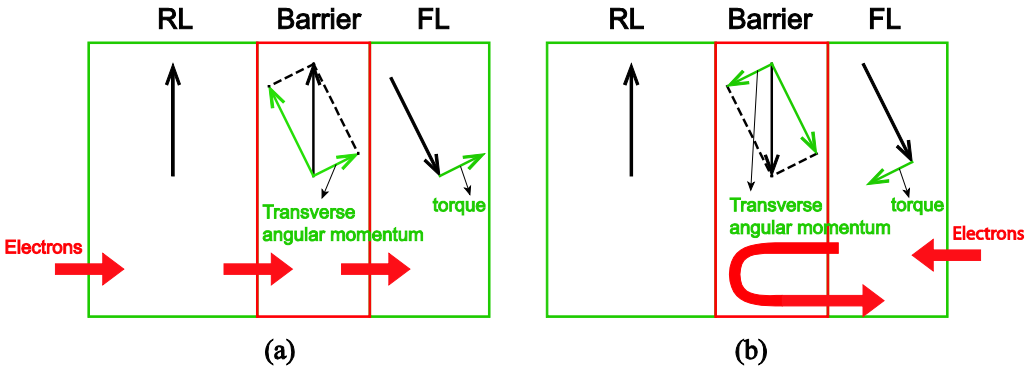


Figure 2.16 Principle of the spin-transfer torque. (a) If electrons flow from the RL to FL, the MTJ is switched to P state. (b) If electrons flow from the FL to RL, the MTJ is switched to AP state.

To understand the STT-induced magnetization switching, the FL magnetization is abstracted to a unit magnetic moment $\vec{m}$ under the macrospin approximation. Then the dynamics of magnetization switching can be described by a Landau-Lifshitz-Gilbert (LLG) equation [36] including the STT, as

$$\frac{\partial \vec{m}}{\partial t} = -\gamma \mu_0 \vec{m} \times \vec{H}_{\text{eff}} + \alpha \vec{m} \times \frac{\partial \vec{m}}{\partial t} - \frac{\gamma \hbar JP}{2et_F M_s} \vec{m} \times \left(\vec{m} \times \vec{m}_r \right) \tag{2.12}$$

where $\vec{H}_{eff}$ is the effective magnetic field, which is the sum of different magnetic fields, such as the external magnetic field, the demagnetization field and the anisotropy field. γ is the gyromagnetic ratio. μ_0 is the vacuum permeability. α is the Gilbert damping constant. $\hbar$ is the reduced Planck constant, P is the spin-polarization, e is the elementary charge, t_F is the FL thickness, M_s is the saturation magnetization, $\vec{m}_r$ is the unit vector along the RL magnetization. J is the write current density.

There are three torques in the right side of Eq. (2.12). Their roles are illustrated by Figure 2.17 [29], [104]. The first item is the field-induced torque which causes the magnetic moment to precess around the effective magnetic field. The second item is the Gilbert damping torque which leads to the relaxation of the precession. The third item is the STT, which is proportional to the write current density. The STT resists or assists the Gilbert damping torque depending on the polarity of the current. For the resisting case, if the current density is larger than a threshold value, the STT is strong enough to overwhelm the Gilbert damping torque and to reverse the magnetization. Accordingly, the current-induced magnetization switching occurs.

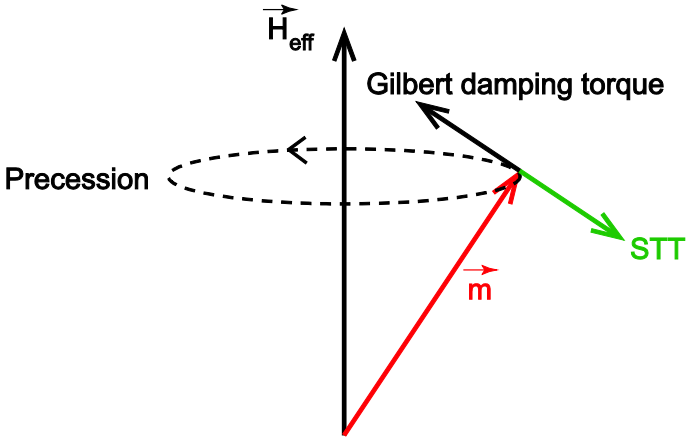


Figure 2.17 Magnetization dynamics described by Eq. (2.12).

Following the above theoretical works, STT switching was experimentally demonstrated in GMR devices [105]–[106] and MTJs [107]–[108] successively. Recently commercial STT-MRAM products have also been launched [109]. The STT switching has lower process complexity than FIMS and TAS since it requires only a bidirectional current. More importantly, the write current density for the STT switching is lower (1–10 MA/cm^2) and the scalability is more promising. Currently, the STT has become the mainstream write technology for the MRAM, which will be detailed in Section 2.3.

2.2.2.3 Perpendicular magnetic anisotropy

Another important advance in the MTJ development is the implementation of perpendicular magnetic anisotropy (PMA). In earlier studies, MTJs had in-plane magnetic anisotropy, which is inferior to PMA due to two reasons as follows.

First, magnetic anisotropy of the MTJ is directly related to the thermal stability and data retention. In-plane anisotropy mainly originates from the shape anisotropy. Thereby an elongated cell surface and a thin thickness are required to provide enough thermal stability. With the shrinking of the MTJ size, the in-plane-anisotropy MTJ (i-MTJ) has difficulty in maintaining the satisfying thermal stability. The perpendicular-anisotropy MTJ (p-MTJ) has no requirement for the elongated shape and thus can overcome this issue.

Second, the p-MTJ is more suitable for the STT switching than the i-MTJ. It is explained as follows. The critical current (I_{c0}) for the STT switching can be derived from LLG equation (see Eq. (2.12)). For the i-MTJ, it is expressed as

$$I_{c0\parallel} \simeq \alpha \frac{\gamma \mu_0 e}{\mu_B P} M_s V_F \left(H_{k\parallel} + \frac{M_s}{2} \right) \tag{2.13}$$

where μ_B is the Bohr magneton, V_F is the FL volume, $H_{k\parallel}$ is the uniaxial in-plane anisotropy field. Other possible fields (e.g. the dipole field) are neglected. The energy barrier of thermal stability (E) of the i-MTJ is given by

$$E_{\parallel} = \frac{\mu_0 M_s H_{k\parallel} V_F}{2} \tag{2.14}$$

The comparison between Eqs. (2.13) and (2.14) indicates that the STT must overcome additional field $M_s/2$ which makes no contribution to the thermal stability. But in a p-MTJ, the critical current is proportional to the thermal stability, as

$$I_{c0\perp} \simeq \alpha \frac{\gamma \mu_0 e}{\mu_B P} M_s V_F H_{k\perp} = 2\alpha \frac{\gamma e}{\mu_B P} E_{\perp} \tag{2.15}$$

Therefore p-MTJ requires lower write current than i-MTJ given the same thermal stability.

Motivated by the above advantages, researchers made much effort to obtain the PMA in the MTJ. In 2002, p-MTJ was experimentally demonstrated for the first time with a TbFeCo/CoFe/Al_2O_3/CoFe/GdFeCo structure, where the PMA is caused by the exchange coupling of TbFeCo/CoFe and CoFe/GdFeCo [110]. In 2006, the STT switching and the PMA were simultaneously implemented in Co/Ni multilayers [111]. Shortly afterwards, in 2007, the same task was achieved in a CoFeB/MgO/CoFeB MTJ [112]. But the TMR ratio of this MTJ was not satisfying (only 15%) due to non-fully crystallized MgO barrier and the insufficient annealing. High-performance CoFeB/MgO-based STT-PMA-MTJs were obtained in 2010 [113]–[114]. Typically, high TMR ratio (120%), small area (40 nm in diameter), high thermal stability factor (40), and low write current (49 μA) can be achieved [113].

2.2.3 Magnetization switching induced by spin-orbit interaction

Recently, lots of progresses have been made in the study of high-performance MTJs. For instance, sub-volume p-MTJ ($\leq$ 40 nm in diameter) has been invested much research effort to accomplish low write current while keeping high thermal stability [115]–[121]. In the aspect of write approach, electric field-assisted mechanism was proposed to achieve ultrafast switching speed (sub-nanosecond) and low write energy by modulating the interfacial perpendicular anisotropy [122]–[123]. This section will introduce another newfound write approach using spin-orbit interaction, which is also the basis for the work of Chapter 5. Before beginning, two main bottlenecks limiting the switching performance of the STT are presented.

First, the STT switching needs an undesirable incubation delay, which is explained as follows. According to Eq. (2.12), initial STT is zero if the magnetizations of the FL and RL ($\vec{m}$ and $\vec{m}_r$) are

exactly collinear. It is thermal fluctuation that causes a little misalignment of the magnetizations and provides a small STT to trigger the switching process. An example of time-resolved STT switching is shown in Figure 2.18, where the magnetic anisotropy is in-plane (X-axis) and an initial angle of 6.5° is assumed. It is seen that the magnetization evolves slowly during a long initial stage, which is so-called incubation delay. Such a delay hinders the STT from achieving ultrafast switching.

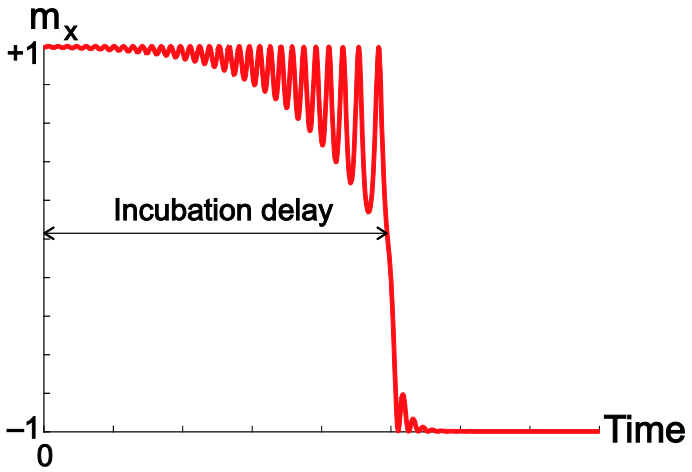


Figure 2.18 Time-resolved X-component of the normalized FL magnetization in an i-MTJ.

Second, faster STT switching requires a larger write current (or write voltage), which adds the risk of barrier breakdown as the write current directly flow through the MTJ.

To overcome the above bottlenecks, spin-orbit interaction was recently investigated to provide an alternative write approach. Spin-orbit interaction means that the electron's spin angular momentum interacts with its orbital angular momentum. In some materials, spin-orbit interaction can be strong enough to generate significant spin accumulation from an unpolarized charge current. The spin accumulation induces a torque (called spin-orbit torque, SOT) to switch the magnetization [124]. Such an SOT-induced magnetization switching has been experimentally demonstrated in three device geometries shown in Figure 2.19. In Figure 2.19(a), an FM layer with perpendicular magnetization is sandwiched between an oxide-insulator and an NFM heavy metal strip (e.g. Pt, Ta) [30]–[33], [125]–[128]. In Figure 2.19(b)–(c), the heavy metal strip is contacted to the FL of the overlying i-MTJ [33], [129]–[130] and p-MTJ [131], respectively. The key idea of these designs is that an in-plane charge current flowing through the heavy metal (Y-axis) can generate the SOT for the magnetization switching. The origin of this SOT is still under the debate, possibly Rashba effect [30]–[31], spin Hall effect (SHE) [32]–[33], [127]–[130] or both [126]. These two effects are explained below.

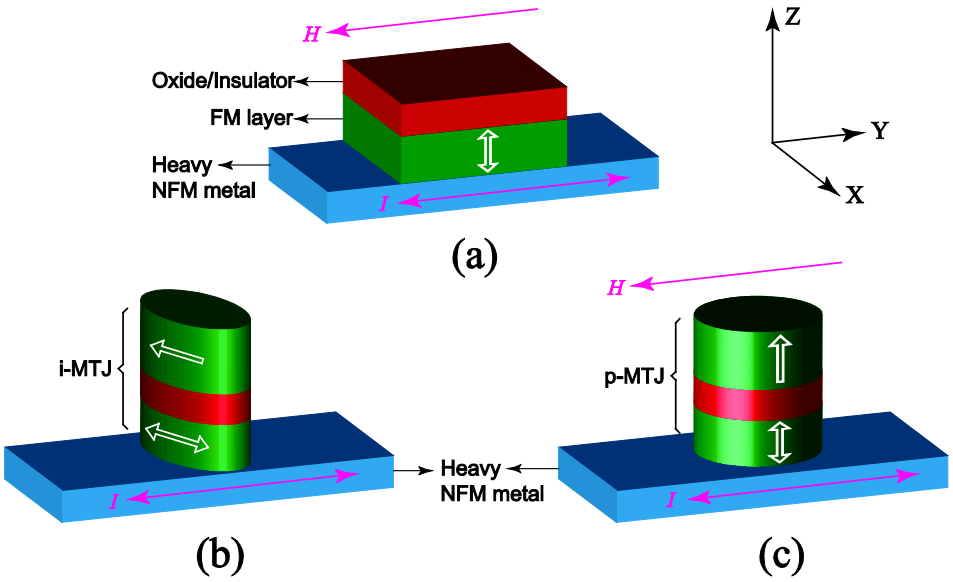


Figure 2.19 Three device geometries used in the experiments of spin-orbit torque-induced magnetization switching.

Rashba effect originates from the breaking of structural inversion symmetry [132]–[133]. It can occur in those devices shown in Figure 2.19 since the FM layer or FL is sandwiched between two different materials to break the vertical inversion symmetry. Rashba effect results in an effective magnetic field ($\vec{H}_R$) as

$$\vec{H}_R = \alpha_R \vec{e}_z \times \vec{J} \tag{2.16}$$

where α_R is a dimensionless coefficient, $\vec{e}_z$ is the unit vector along the Z-axis, $\vec{J}$ is the vector of in-plane current (along Y-axis in Figure 2.19).

This effective magnetic field contributes a torque (i.e. SOT, $\propto \vec{m} \times \vec{H}_R$) exerting on the magnetization of the adjacent FM layer or FL. The strong spin-orbit interaction in the heavy metal makes this SOT sufficiently large to trigger the magnetization switching. However, for the case of PMA (see Figure 2.19 (a) and (c)), an additional in-plane magnetic field is required to achieve the deterministic switching since $\vec{H}_R$ and anisotropy axis (Z-axis) are not collinear. For the case of i-MTJ (see Figure 2.19(b)), single Rashba effect can control the magnetization switching if the easy-axis is set to the direction of $\vec{H}_R$ (it is X-axis in Figure 2.19(b)).

SHE is another possible mechanism responsible for the SOT. The principle of SHE is illustrated by Figure 2.20(a). A charge current flowing through the heavy metal can generate spin accumulation on the lateral surfaces due to the strong spin-orbit interaction, which forms a pure spin current along the direction orthogonal to both the charge current and electron spin [134]–

[138]. In one word, SHE can generate spin current from an unspin-polarized charge current. Inverse process (inverse spin Hall effect, iSHE [139]) can also occur due to the same spin-orbit interaction, as shown in Figure 2.20(b), where a pure spin current injected into the heavy metal causes the charge accumulation at one side of the sample and forms a charge current along the direction orthogonal to both the spin current and electron spin. SHE and iSHE conform to the Onsager reciprocal relationship, as

$$\begin{cases} \vec{J}_s = \eta_{SH}\vec{J}_c \times \vec{\sigma}_{SH}, & \text{SHE} \\ \vec{J}_c = (1/\eta_{SH})\vec{J}_s \times \vec{\sigma}_{SH}, & \text{iSHE} \end{cases} \tag{2.17}$$

where $\hbar|\vec{J}_s|/(2e)$ is the spin current density, $\vec{J}_s$, $\vec{J}_c$ and $\vec{\sigma}_{SH}$ are vectors of spin current, charge current and electron spin, respectively. η_{SH} is the spin Hall angle.

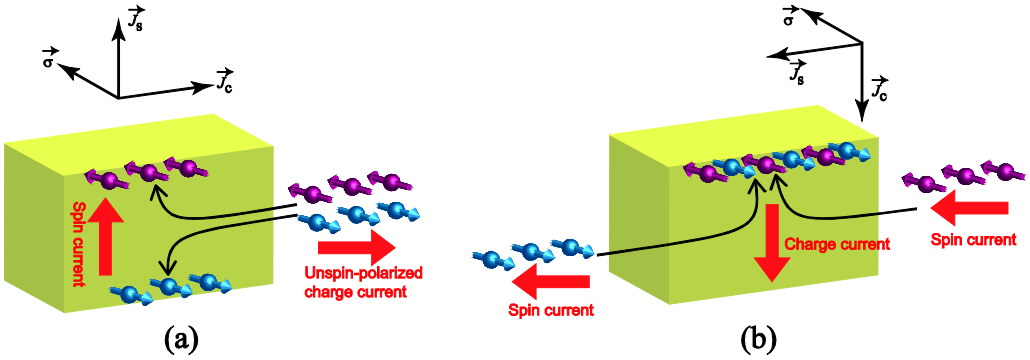


Figure 2.20 (a) Spin-Hall effect and (b) Inverse spin-Hall effect.

The SHE-induced spin current can be injected into the adjacent FM layer or FL, resulting in a torque (also is SOT, or is called spin Hall torque, $\propto \vec{m} \times (\vec{m} \times \vec{\sigma})$) through the transfer of spin angular momentum, similar to the mechanism of the STT (see Section 2.2.2.2). Like the Rashba effect, a single SHE-induced torque cannot achieve the deterministic switching of perpendicular magnetization since the direction of injected electron spin is not collinear with the anisotropy axis, thereby an additional in-plane magnetic field is required (see Figure 2.19(a) and (c)). For the i-MTJ whose easy-axis is aligned to the injected spin direction, deterministic switching can be implemented by the SHE (see Figure 2.19(b)).

Such switching induced by Rashba effect or SHE requires only one in-plane write current running through the heavy metal instead of through the MTJ, thus the risk of barrier breakdown is reduced. Moreover, for the case of perpendicular magnetization, the initial SOT is more easily triggered than the conventional STT since both the Rashba effective field ($\vec{H}_R$) and the injected spin ($\vec{\sigma}_{SH}$) are orthogonal to the anisotropy axis. This can eliminate the incubation delay of the

STT and achieve an ultrafast switching. These advantages have been validated by the experimental demonstrations [30]–[33], [125]–[131].

Nevertheless, the further application of the SOT switching is hindered by some drawbacks. For an SOT-p-MTJ, the use of an additional magnetic field is undesirable since it adds the design complexity. Although this magnetic field is a constant and can be provided by a permanent magnet layer integrated into the MTJ stack, yet it reduces the thermal stability and is sensitive to the process variation. This additional magnetic field can be avoided by replacing p-MTJ with i-MTJ, but the i-MTJ has poorer scalability and lower thermal stability than p-MTJ. Besides, in contrast to SOT-p-MTJ, SOT-i-MTJ cannot solve the incubation delay issue since the relative orientations between initial SOT and easy-axis is the same as that of the conventional STT. To solve this dilemma, Ref. [133] proposed lateral asymmetry-breaking to achieve the deterministic switching of the perpendicular magnetization in the absence of the magnetic field. But this approach requires advanced process to fabricate a film of varying thickness. Another solution is to replace the role of magnetic field with an STT write current, which was proposed by Ref. [34]. In Chapter 5, we will focus on this write approach in terms of magnetization dynamics and circuit application.

2.3 Related non-volatile memories and logic circuits

FTJs and MTJs provide new routes to the next generation NVMs and NVLs. However, so far few FTJ-based NVM or NVL has been demonstrated since current research is still focused on the optimization of the FTJ nanopillar. MTJ-based applications, by contrast, have been widely explored and even been produced commercially. In particular, MRAM is attracting more interests due to its increasing competiveness. This section will review briefly some achievements on MRAM and magnetic logic circuits.

Figure 2.21(a)–(b) shows the elementary cell and architecture used in the most common MRAM, where one MOS transistor is connected with one MTJ in series to form 1T1R (one transistor and one resistor) memory cell [140]. Besides, other structures such as 2T1R [141] and 4T2R [142] memory cells were also proposed, as Figure 2.21(c). In 1T1R memory cell, the gate and source of the transistor are connected to the word line (WL) and source line (SL), respectively. Two electrodes of the MTJ are connected to the bit line (BL) and transistor drain, respectively. This architecture provides high compatibility since MTJ can be fabricated above the CMOS circuits by back-end-of-line (BEOL) process [143]. Alternative architecture is the cross-point arrangement [144] shown in Figure 2.21(d), where each MTJ is located at the intersection of the column line and row line. The cross-point architecture allows high-density integration, but it suffers from the sneak path issue [145], which needs to be overcome by the optimized design.

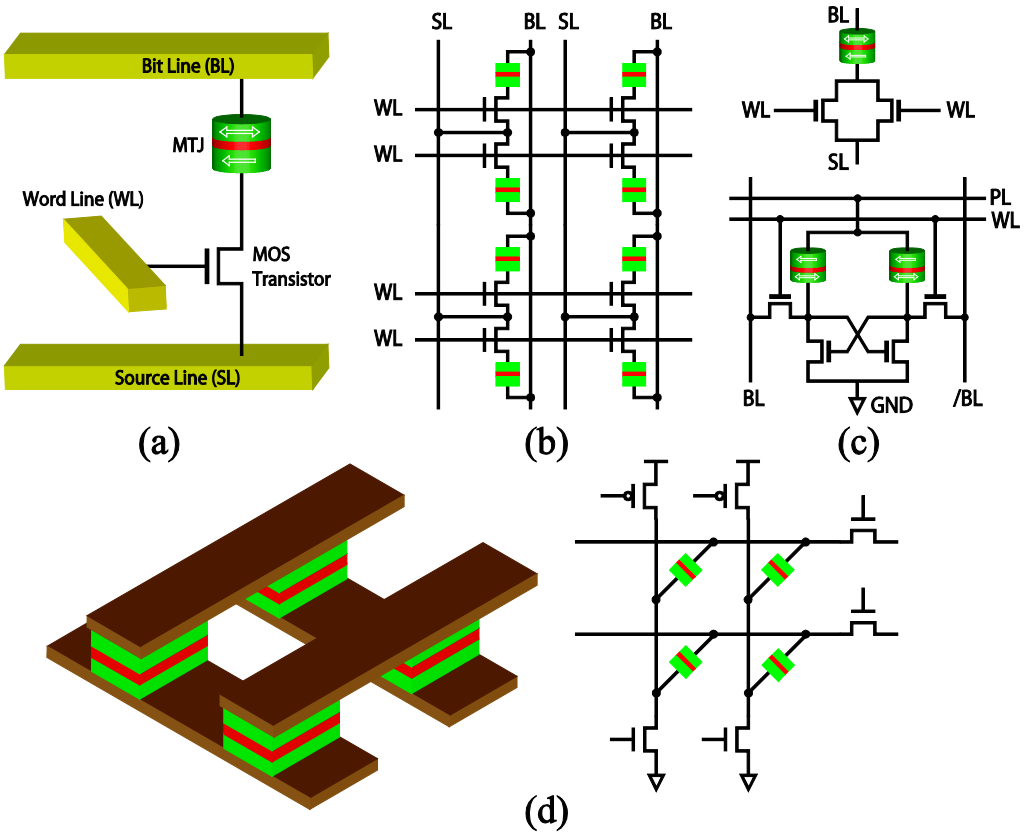


Figure 2.21 (a) 1T1R memory cell [140], (b) MRAM architecture based on 1T1R memory cell [140], (c) 2T1R and 4T2R memory cells [141]–[142], (d) Cross-point architecture for MRAM [144].

The type of the MRAM is mainly determined by the write approach and magnetic anisotropy. The early MRAMs had in-plane magnetic anisotropy and were written by FIMS. But currently almost all the attention has been paid to the STT-switched PMA-MRAM, since it is more promising in write power and scalability. Table 2.3 summarizes selected MRAM demonstrators in the past decade. It is seen that the MRAMs kept pace with the progress of the MTJ development, indicating the increasing application potential.

Table 2.3 Some demonstrators of MRAMs

Year	Group	Type	Capacity	Cell area (μm^2)	Speed (ns)	Power or current	Ref.
2000	Motorola	FIMS i-MTJ	512-bit	7.2	14	*W: 8 mA *R: 800 μA	[146]
2000	IBM	FIMS i-MTJ	1-Kbit	3	10	W: 40 mW R: 5 mW	[147]

2002	Samsung	FIMS i-MTJ	64-Kbit	2.06	–	–	[148]
2003	Motorola	FIMS i-MTJ	1-Mbit	7.2	< 50	4 mA 10 μA	[101]
2004	Freescale	Toggle i-MTJ	4-Mbit	1.55	25	–	[149]
2004	IBM/ Infineon	Toggle i-MTJ	16-Mbit	1.42	30	80 mA 25 mA	[150]
2005	Sony	STT i-MTJ	4-Kbit	–	W: 10	W: 400 μA	[140]
2006	Honeywell	Toggle i-MTJ	1-Mbit	–	R: < 67 W: < 107	< 500 mW	[151]
2006	Toshiba/ NEC	FIMS i-MTJ	16-Mbit	1.872	34	–	[152]
2006	NEC	Toggle i-MTJ	16-Mbit	1.3	32	W: 80–400 mW	[153]
2007	Hitachi/ Univ. Tohoku	STT i-MTJ	2-Mbit	2.56	R: 40 W: 100	W: 200 μA	[154]
2008	Toshiba	STT p-MTJ	1-Kbit	–	W: 4	W: 50 μA	[155]
2009	Hitachi/ Univ. Tohoku	STT i-MTJ	32-Mbit	1	R: 35 W: 40	W: 300 μA	[141]
2010	Toshiba	STT p-MTJ	64-Mbit	0.3584	30	–	[156]
2010	Hynix/ Grandis	STT i-MTJ	64-Mbit	0.041	–	W: 140 μA	[157]
2012	Everspin	STT p-MTJ	64-Mbit	–	10–50	–	[158]
2014	TDK-Headway technologies	STT p-MTJ	8-Mbit	0.04	W: < 5	–	[159]
2015	Avalanche Technology	STT p-MTJ	64-Mbit	–	–	–	[160]

* W means write, and R means read.

Also there were some attempts to develop magnetic logic circuits. Most of them were targeted to the realization of the logic-in-memory architecture, which was proposed early in the 1960s [161]. The basic idea of the logic-in-memory is illustrated in Figure 2.22, where two main units of the typical computer are seen: the logic unit performing the arithmetic operation and the memory unit storing the data used for the computing. In the conventional Von-Neumann architecture (see Figure 2.22(a)), these two units are spatially separate, resulting in a data-transfer bottleneck between them. In contrast, the logic-in-memory architecture can solve this bottleneck by distributing memory cells over the logic circuits (see Figure 2.22(b)). The MTJ is a promising candidate for constructing the logic-in-memory architecture due to two reasons: first, BEOL process enables MTJs to be integrated above the CMOS logic circuits; second, the non-volatility of MTJs can eliminate the static power for maintaining the stored data, especially suitable for normally-off electronics. In addition, the continuous progress in the fabrication technology of the MTJ provides the logic-in-memory architecture with a broad prospect.

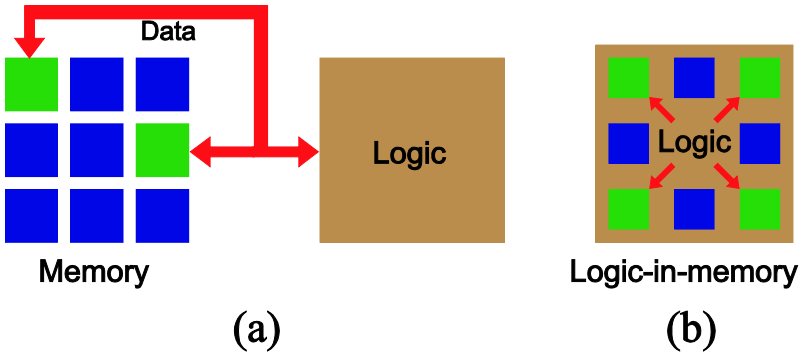


Figure 2.22 (a) Von-Neumann architecture, and (b) Logic-in-memory architecture.

Various digital logic systems have been proposed and demonstrated with the MTJ-based logic-in-memory architecture. For instance, in Refs. [162]–[163] TAS-MRAM cells were integrated into field-programmable gate arrays (FPGAs), which allowed reducing static power consumption and achieving real time reconfiguration. In Ref. [164] a non-volatile MFF embedding a couple of MTJs was proposed for the FPGA application. In Ref. [165], an MFF targeted to SoC design was demonstrated in 150 nm CMOS and 240 nm MRAM technology. In Ref. [166] a non-volatile MFA based on hybrid MTJ/CMOS architecture was fabricated with 0.18 μm CMOS process. Recently, a more complicated MTJ/CMOS hybrid video coding hardware was demonstrated [167]. In these examples, the MTJ works as not only an operand but also a storage cell, in agreement with the logic-in-memory design.

2.4 Summary

In this chapter, we reviewed the state-of-the-art FTJs and MTJs. For the FTJ part, we mainly investigated various FTJ nanopillars and explained their working principles. Memristive effect of the FTJ was independently introduced because it is closely related to our work in Chapters 3–4. In the aspect of MTJs, so far massive progresses have been made in both device fabrication and circuit design, from which some important milestones were presented in this chapter. In particular, we devoted a large number of pages to introduce the write approaches of the MTJ, especially the recent demonstrated SOT switching, which are essential for understanding our work in Chapter 5.

Currently, the FTJ is mainly studied at the device level, but its application potential in the NV memories and circuits has not been evaluated. Hence, in Chapters 3–4 we will develop an electrical model of the FTJ and explore the FTJ-based circuit-level applications by simulation. As for the MTJ, various SOT-induced magnetization switching schemes were recently proposed to improve the conventional STT switching. Among them, the spin-Hall-assisted STT switching may be a promising solution since it can achieve pure-electric fast switching in a p-MTJ. Therefore we will focus on the study of this switching scheme in Chapter 5.

Chapter 3

Compact modeling of the FTJ

3.0 Preface

Simulation is an efficient technique for comprehending the working mechanism of the FTJ and analyzing the FTJ-based circuits. To research the FTJ with simulation tools, a compact electrical model needs to be developed, which is just the objective of this chapter.

In this chapter, we develop a compact electrical model for the FTJ reported in Refs. [10] and [12]. We firstly investigate the physical models describing the electrical properties of the FTJ such as tunneling resistance, dynamic switching and memrisitve effect. Then, these physical models are programed with *Verilog-A* language in order to produce a compact electrical model which can run on standard circuit simulation platform (e.g. *Cadence*).

3.1 Physical models of the FTJ

3.1.1 Tunneling resistance model

First of all, a tunneling resistance model is desired to describe the I-V characteristic of the FTJ. Figure 3.1 shows the simplified band diagram of an FTJ. Under the WKB approximation, the tunneling current density (j) is given by [168]

$$j \propto \frac{4\pi e}{\hbar}\int_{-\infty}^{+\infty}\rho_1(E)\rho_2(E-eV)P(E_x)\left[f(E)-f(E-eV)\right]dE_x \tag{3.1}$$

where E_x is the energy of electron in the X-direction, V is the applied voltage, $\rho_1(E)$ and $\rho_2(E)$ are the densities of states in metal-1 and metal-2, respectively. $f(E)$ is the Fermi distribution function, $P(E_x)$ is the tunneling probability, which is expressed as

$$P(E_x) \propto \exp\left(-\frac{2}{\hbar}\int_0^d 2m\sqrt{\varphi(x,V)-E_x}\,\mathrm{d}x\right) \tag{3.2}$$

where m is the effective electron mass, d is the barrier thickness, $\varphi(x,V)$ is the barrier potential.

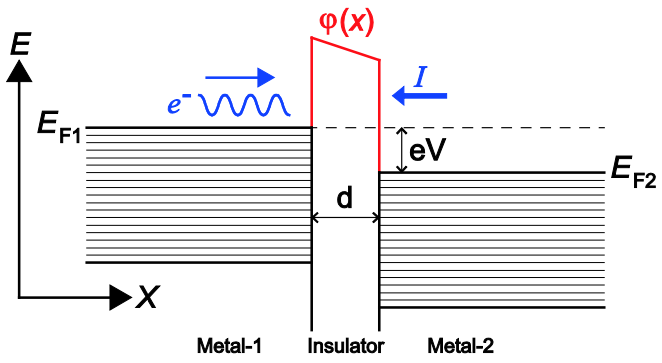


Figure 3.1 Simplified band diagram of an FTJ. E_F is the Fermi energy.

There are mainly two theoretical models proposed by *Simmons* and *Brinkman*, respectively, to simplify the calculation of Eqs. (3.1) and (3.2). Simmons model [42] assumes a rectangular barrier and substitutes the average barrier height for $\varphi(x,V)$. Brinkman model [169] assumes a trapezoidal barrier to take into account the potential asymmetry between two metal/insulator interfaces. Obviously, Brinkman model is more suitable for the case of the FTJ because the ferroelectric barrier is trapezoidal rather than rectangular (see Figure 2.2). By assuming $d > 1$ nm, $\Delta\varphi/\bar{\varphi} < 1$ and $V < \bar{\varphi}$, Brinkman expanded the Eq. (3.1) in powers of V and neglected higher powers to obtain the expressions of differential tunneling resistance, as

$$R(0) = \frac{dV}{dI}\Big|_{V=0} = \frac{2\sqrt{2}\pi^2\hbar}{e^2 A} \cdot \frac{t_B}{\bar{\varphi}^{1/2} \cdot S} \exp\left(2\sqrt{2}A \cdot t_B \cdot \bar{\varphi}^{1/2}\right) \tag{3.3}$$

$$R_{diff}(V) = \frac{dV}{dI} = \frac{R(0)}{1 - \frac{\sqrt{2}}{12} \cdot \frac{A \cdot t_B \cdot \Delta\varphi}{\bar{\varphi}^{3/2}} \cdot V + \frac{1}{4} \cdot \frac{A^2 {t_B}^2}{\bar{\varphi}} \cdot V^2} \tag{3.4}$$

where

$$A = \frac{\sqrt{me}}{\hbar}$$

$R(0)$ is the resistance under the zero bias voltage. I is the current. t_B is the barrier thickness, S is the surface area of the device, $\bar{\varphi}$ is the average barrier potential height, $\Delta\varphi$ is the difference of barrier potential height between two metal/insulator boundaries. The units of $\bar{\varphi}$ and $\Delta\varphi$ are volts. I-V curve can be derived from Eq. (3.4), as

$$I(V) = \frac{V - \frac{\sqrt{2}}{24} \cdot \frac{A \cdot t_B \cdot \Delta\varphi}{\bar{\varphi}^{3/2}} \cdot V^2 + \frac{1}{12} \cdot \frac{A^2 {t_B}^2}{\bar{\varphi}} \cdot V^3}{R(0)} \tag{3.5}$$

Thus the static tunneling resistance under a low voltage is expressed as

$$R_{static}(V) = \frac{V}{I} = \frac{R(0)}{1 - \frac{\sqrt{2}}{24} \cdot \frac{A \cdot t_B \cdot \Delta\varphi}{\bar{\varphi}^{3/2}} \cdot V + \frac{1}{12} \cdot \frac{A^2 {t_B}^2}{\bar{\varphi}} \cdot V^2} \tag{3.6}$$

The values of $\bar{\varphi}$ and $\Delta\varphi$ need to be determined by the fitting of experimental results. Here the I-V data of a 700 nm-diameter Co/BTO(2 nm thick)/LSMO FTJ extracted from Ref. [10] serves as the experimental data to be fit. However, we cannot achieve a good fit to these data by

adjusting only $\bar{\varphi}$ and $\Delta\varphi$. Therefore we followed the suggestion in Ref. [10] that m should also be adjusted together with $\bar{\varphi}$ and $\Delta\varphi$. Finally the fitting results are shown in Figure 3.2 and Table 3.1.

Table 3.1 Parameters fitted with Brinkman model

States	φ_1	φ_2	m	$\bar{\varphi} = (\varphi_1 + \varphi_2)/2$	$\Delta\varphi = \varphi_2 - \varphi_1$
ON state*	–0.080 V	0.696 V	1.413 m_e	0.308 V	0.776 V
OFF state*	–0.014 V	0.616 V	2.671 m_e	0.301 V	0.630 V

* ON state corresponding to a ferroelectric polarization oriented towards Co electrode. OFF state has an opposite meaning.

Here m_e is the free electron mass, φ_1 and φ_2 are potential barrier heights at LSMO/BTO and Co/BTO interfaces, respectively. Positive bias voltage means that electrons flow from LSMO to Co (current flows from Co to LSMO).

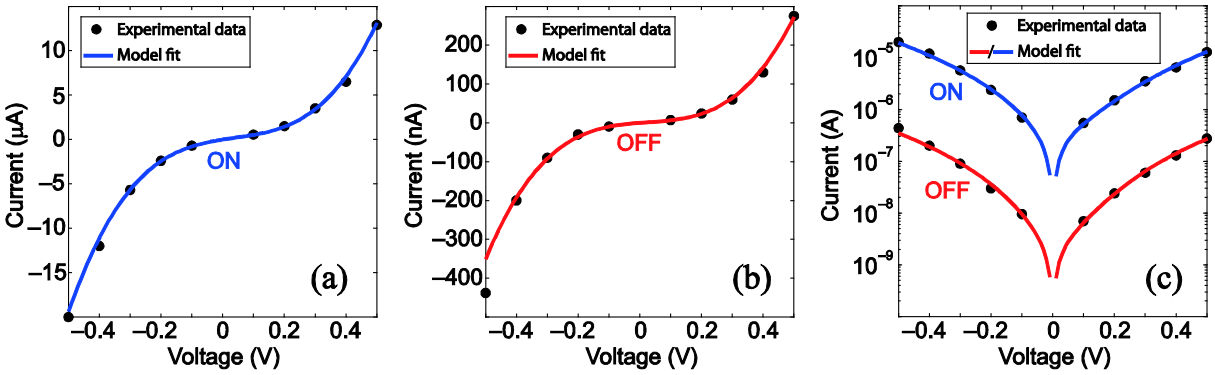


Figure 3.2 I-V curve fitted with Brinkman model.

Unfortunately, the fitting gave unreasonable values which deviate from the assumptions of $\Delta\varphi/\bar{\varphi} < 1$ and $V < \bar{\varphi}$. In addition, $\varphi_1 < 0$ and $\bar{\varphi}_{ON} > \bar{\varphi}_{OFF}$ are against the real physics. One solution is to introduce additional scaling factors into Eq. (3.5) [170], but this leads to an ambiguous physical meaning. Therefore we employed another model developed by *Gruverman* [9] to fit the experimental data, as

$$I(V)=S\cdot C\frac{\exp\left\{\alpha(V)\left[\left(\varphi_2-\frac{V}{2}\right)^{3/2}-\left(\varphi_1+\frac{V}{2}\right)^{3/2}\right]\right\}}{\alpha^2(V)\left[\left(\varphi_2-\frac{V}{2}\right)^{1/2}-\left(\varphi_1+\frac{V}{2}\right)^{1/2}\right]^2}\times\sinh\left\{\frac{3}{2}\alpha(V)\left[\left(\varphi_2-\frac{V}{2}\right)^{1/2}-\left(\varphi_1+\frac{V}{2}\right)^{1/2}\right]\frac{V}{2}\right\} \tag{3.7}$$

where

$$C=-\frac{4me^3}{9\pi^2\hbar^3},\quad \alpha(V)=\frac{4t_B(2me)^{1/2}}{3\hbar(\varphi_1+V-\varphi_2)}$$

The fitting with Eq. (3.7) gave more reasonable parameter values than with Eq. (3.5), as listed in the upper two rows of Table 3.2. Corresponding fitted I-V curves are shown in Figure 3.3. Nevertheless, electrostatic model (see Figure 2.2) shows that, when the ferroelectric polarization is switched from ON to OFF states, φ_1 increases whereas φ_2 decreases. Hence we had to adjust the fitted results for OFF state to meet this criterion, as the last row of Table 3.2. Such a little adjustment hardly degrades the accuracy of the fitting results, as shown in Figure 3.4.

Table 3.2 Parameters fitted with Gruverman model

States	φ_1	φ_2	m	$\bar{\varphi}=(\varphi_1+\varphi_2)/2$	$\Delta\varphi=\varphi_2-\varphi_1$
ON state	0.329 V	0.693 V	0.829 m_e	0.511 V	0.364 V
OFF state	0.409 V	0.709 V	1.383 m_e	0.559 V	0.300 V
OFF state (adjusted)	0.434 V	0.684 V	1.383 m_e	0.559 V	0.250 V

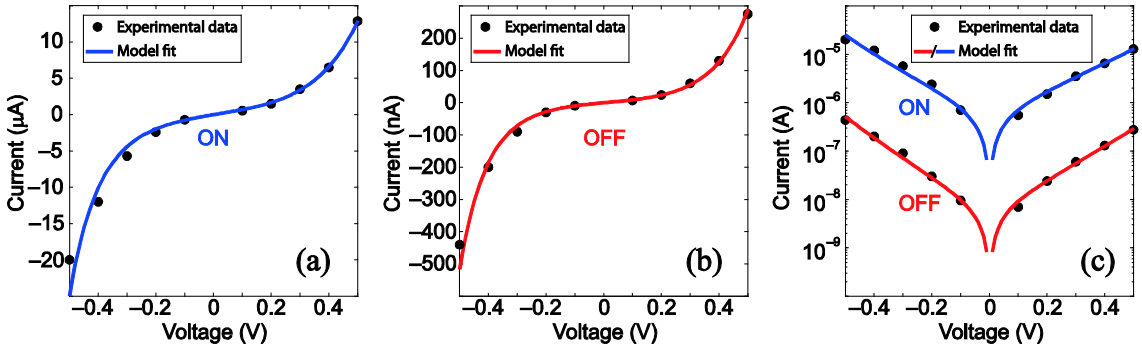


Figure 3.3 I-V curve fitted with Gruverman model.

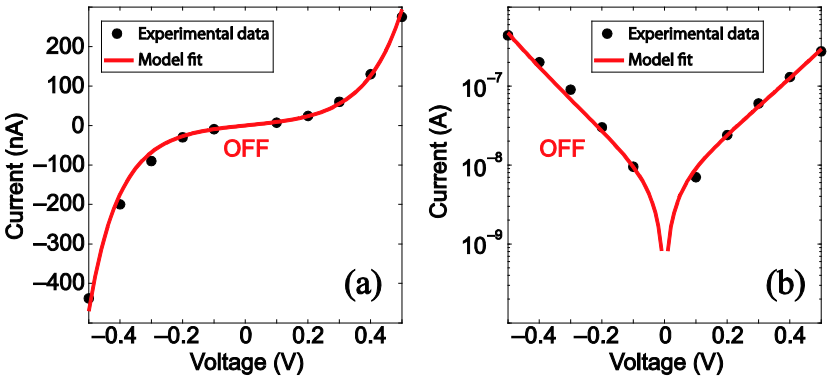


Figure 3.4 I-V curve for OFF state after the adjustment.

It is worth noting that Eq. (3.7) is available only for the direct tunneling (DT) in the low-voltage regime. In the high-voltage regime, the mechanisms responsible for the electron transport are complicated and not well known. It was believed that the Fowler-Nordheim tunneling (FNT) [58] is a dominant factor [4], [171]. In the case of the FNT, barrier potential becomes triangle shown in Figure 3.5. The FNT current is expressed as

$$I(V) = \mathrm{sgn}(V) \cdot S \cdot \frac{e^2 m V^2}{16\pi^2 \hbar m_{ox} \varphi_B t_B{}^2} \exp\left(-\frac{4 t_B \sqrt{2 m_{ox}} e \varphi_B{}^{3/2}}{3\hbar |V|} \right) \tag{3.8}$$

where $sgn(V)$ is sign function. m_{ox} is effective electron mass in the barrier. Its value is given by Table 3.2. φ_B is the tunneling barrier for electrons. $\varphi_B = \varphi_1$ for $V > 0$, or $\varphi_B = \varphi_2$ for $V < 0$. Here the depolarization field [41] and built-in field [172]–[173] are not taken into account.

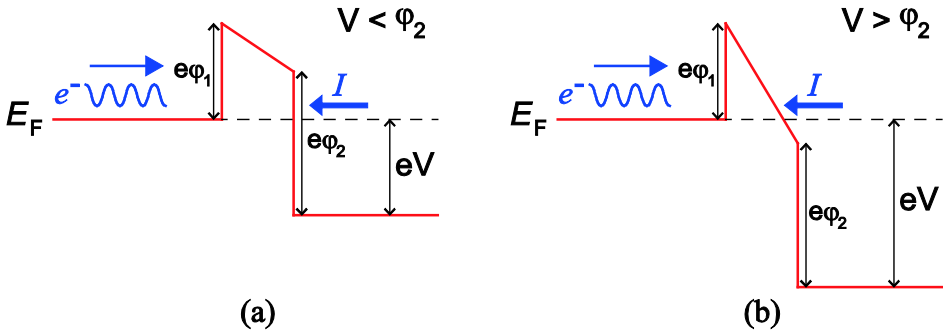


Figure 3.5 Schematic band diagrams for (a) DT and (b) FNT.

However, by substituting Table 3.2 into Eq. (3.8), we obtained unreasonable I-V curves shown in Figure 3.6. For $V < 0$, there is no transition voltage between the DT and FNT. For $V > 0$,

both the transition voltages are less than 0.5 V, which is, however, in the DT regime. In order to obtain reasonable transition voltages, we introduced two scaling factors F_1 and F_2 into Eq. (3.8), as

$$I(V) = \mathrm{sgn}(V) \cdot F_1 \cdot S \cdot \frac{e^2 m V^2}{16\pi^2 \hbar m_{ox} \varphi_B t_B^2} \exp\left(-F_2 \cdot \frac{4 t_B \sqrt{2 m_{ox}} e \varphi_B^{3/2}}{3\hbar |V|} \right) \tag{3.9}$$

where $F_1 > 0$ and $F_2 > 0$. It is not easy to determine the values of F_1 and F_2 since there are no sufficient I-V experimental results in the high-voltage regime. This issue will be discussed in Section 3.2.2.

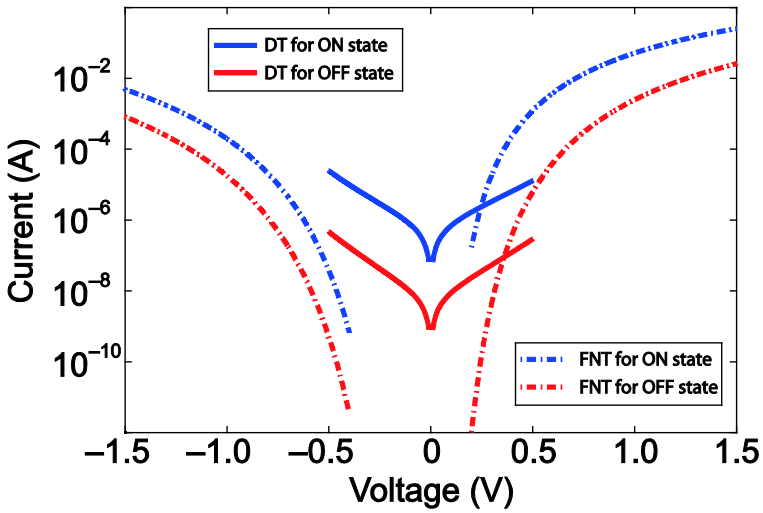


Figure 3.6 I-V curves for DT and FNT with the values of Table 3.2.

3.1.2 TER ratio model

TER ratio is a crucial parameter evaluating the ability of an FTJ to be sensed in binary memories. Giant TER ratio is desired by the FTJ for achieving high-reliability readout. Thus it is necessary to develop a model for estimating the TER ratio of the FTJ. Since the read voltage of the FTJ is kept at a low level to avoid the unexpected polarization change, TER ratio model will be discussed with the assumption of the small bias voltage.

In Section 3.1.1, although Brinkman model failed to give reasonable fitting parameter values, it is still available for describing qualitatively the I-V characteristic of the FTJ. Thereby TER ratio under zero bias voltage can be derived from Eq. (3.3), as

$$TER(0)=\frac{R_{OFF}(0)}{R_{ON}(0)}=\sqrt{\frac{m_{ON}\bar{\varphi}_{ON}}{m_{OFF}\bar{\varphi}_{OFF}}}\exp\left[\frac{2\sqrt{2e}t_B}{\hbar}\left(\sqrt{m_{OFF}\bar{\varphi}_{OFF}}-\sqrt{m_{ON}\bar{\varphi}_{ON}}\right)\right] \quad (3.10)$$

On the other hand, by assuming $\Delta\varphi/2<\bar{\varphi}$ (it is available for our case, see Table 3.2), *Gruverman* gave the approximation of Eq. (3.7) under the small bias voltage [9], as

$$I(V)\simeq V\cdot S\cdot\frac{e^2}{2\sqrt{2}\pi^2\hbar^2}\cdot\frac{\sqrt{me\bar{\varphi}}}{t_B}\exp\left(-2\sqrt{2}t_B\frac{\sqrt{me\bar{\varphi}}}{\hbar}\right) \quad (3.11)$$

which can arrive at the same expression of TER ratio as Eq. (3.10).

Therefore Eq. (3.10) is an efficient model for studying the TER effect of the FTJ. It provides two approaches to obtain larger TER ratio, as follows.

First, based on Eq. (3.10), Figure 3.7 shows the TER ratio as a function of $\Delta\bar{\varphi}=\bar{\varphi}_{OFF}-\bar{\varphi}_{ON}$ for two barrier thicknesses. Here only $\bar{\varphi}_{OFF}$ varies while other parameters are configured as Table 3.2. As indicated in the figure, an efficient approach to increase TER ratio is to enlarge $\Delta\bar{\varphi}$, in agreement with the conclusion of Ref. [39]. According to Eq. (2.2), this approach can be achieved by choosing two electrodes with larger difference of screening lengths.

Second, Eq. (3.10) and Figure 3.7 indicate that TER ratio can also be exponentially increased by depositing thicker barrier. This law is consistent with experimental measurement [8] and other theoretical calculation [39]–[40], [171]. Actually, $\Delta\bar{\varphi}$ also increases with the barrier thickness [9], therefore the increase in TER ratio is stronger than exponential.

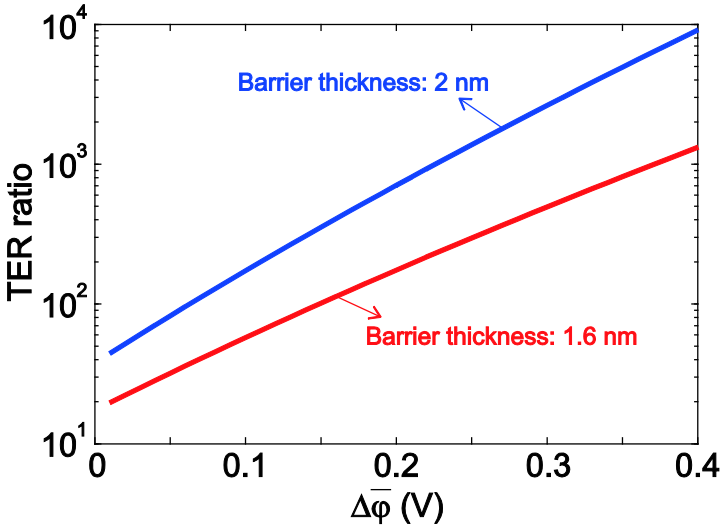


Figure 3.7 TER ratio as a function of $\Delta\bar{\varphi}$ for 1.6 nm and 2.0 nm-thick barriers.

3.1.3 Dynamic switching model

As mentioned in Section 2.1.1, the switching of an FTJ is achieved through the voltage-driven polarization reversal. The voltage-dependent switching speed of the FTJ is the major concern in the circuit application. Here we present a dynamic switching model for calculating it.

Two physical models have been proposed to describe the kinetics of polarization reversal: Kolmogorov-Avrami-Ishibashi (KAI) model [174] and nucleation-limited-switching (NLS) model [175], as discussed below.

According to KAI model, the probability that an arbitrary point O is covered by the switched domain at time t is

$$Q(t) = 1 - \exp\left[-\int_0^t P_N(\tau) V_O(t,\tau) d\tau\right] = 1 - \exp(-A) \tag{3.12}$$

where $P_N(\tau)$ is the nucleation probability at time τ per unit volume per unit time. $V_O(t,\tau)$ is a volume around point O, as

$$V_O(t,\tau) = C_n \left\{r_c + v(t-\tau)\right\}^n \tag{3.13}$$

where r_c is the radius of the nucleus, v is the velocity of domain wall propagation, n is the dimensionality, C_n is a dimensionality-dependent factor. For the case of thin film, $n = 2$ and $C_n = \pi$. Eq. (3.12) can be explained by Figure 3.8, if and only if a nucleus is formed inside $V_O(t,\tau)$ at time τ, the point O can be covered by the switched domain before time t.

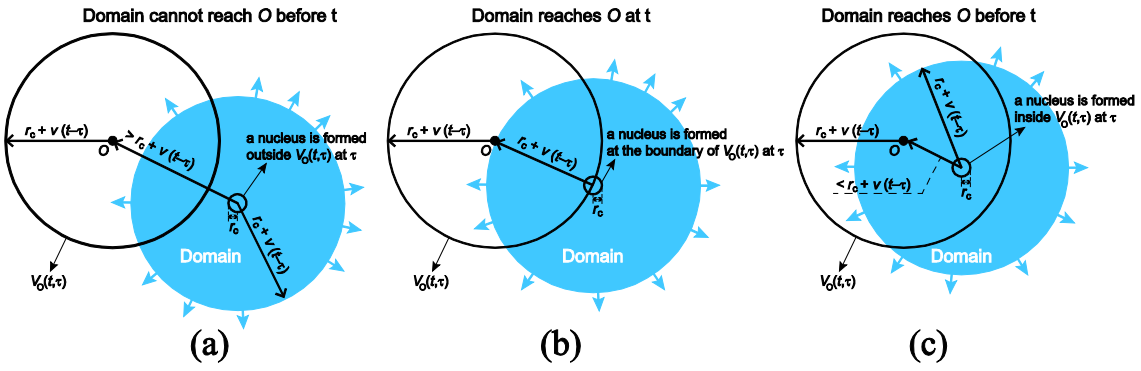


Figure 3.8 Schematic explaining how to judge whether the point O is covered by the switched domain.

Thereafter, the reversed polarization (ΔP) is expressed as

$$\Delta P(t) = 2P_s \cdot Q(t) = 2P_s \cdot \left[1 - \exp(-A)\right] \tag{3.14}$$

where P_s is the spontaneous polarization.

Two types of scenarios were considered by KAI model: the one is α-type assuming that the nucleation occurs throughout the entire switching process with a constant probability P_N; the other is β-type assuming that the nucleation only occurs at the beginning of switching process. Then, Eq. (3.14) is written as

$$\frac{\Delta P(t)}{2P_s} = \begin{cases} 1-\exp\left[-\left(\dfrac{t}{t_{0\alpha}}\right)^{n+1}\right], & \text{for α-type} \\ 1-\exp\left[-\left(\dfrac{t}{t_{0\beta}}\right)^{n}\right], & \text{for β-type} \end{cases} \tag{3.15}$$

where $t_{0\alpha}$ and $t_{0\beta}$ are the characteristic time. It is inferred from Eqs. (3.12) and (3.13) that $t_{0\alpha}$ and $t_{0\beta}$ are functions of C_n, r_c, v and P_N.

KAI model has been successfully used to describe the polarization reversal of the single-crystalline and epitaxial ferroelectric film [176]–[177], in which ferroelectric domain can propagate unrestrictedly over a large region. However, KAI model failed to fit the switching kinetics of the polycrystalline ferroelectric film [82], [175], [178]–[179]. Accordingly, some alternative models were proposed to explain the deviation from KAI model. Among them, NLS model is widely accepted as a preferable choice.

NLS model assumes that a ferroelectric film consists of massive elementary regions, each of which has independent switching kinetics and its domain cannot penetrate into neighboring regions. Each region is so small that the delay of domain wall propagation can be neglected, that is to say, the switching delay of each region is dominated by the domain nucleation. Typically, the reversed polarization can be expressed as

$$\Delta P(t) \simeq 2P_s \cdot \left[1-\int_{-\infty}^{+\infty} e^{-t/\tau_0} g\left(\ln\tau_0\right) d\left(\ln\tau_0\right)\right] \tag{3.16}$$

where $1/\tau_0$ is the nucleation rate, $g(ln\tau_0)$ is a distribution function of τ_0.

Our model will be fit to the experimental results exacted from Ref. [12], where the evidence of domain wall propagation was clearly demonstrated. Therefore NLS model is not applicable for this case. Alternatively, a modified KAI model was proposed in Ref. [12] to achieve a good fit to experimental data. According to this model, the ferroelectric film is divided into N regions. In each region, the nucleuses are formed at τ_{Ni}, then domain wall propagates without new nucleation occurring. This behavior is similar to β-type KAI model. The percentage of the reversed polarization is written as

$$\frac{\Delta P(t)}{2P_s} = \sum_{i=1}^{N} \lambda_i \times h\left(t - \tau_{Ni}\right) \times \left\{ 1 - \exp\left[-\left(\frac{t - \tau_{Ni}}{\tau_{Pi}} \right)^2 \right] \right\} \tag{3.17}$$

where λ_i is the proportion of i-th region to the entire film, $h(t)$ is Heaviside step function, τ_{Pi} is the characteristic time of domain wall propagation.

The experimental results of $\tau_{Ni,Pi}$ showed different voltage dependences for two switching directions. For the case of OFF-to-ON switching, it was found that τ_{Ni} and τ_{Pi} can be described by Merz's law [80], [180]–[181], as

$$\tau_{N,P} = \tau_{0N,0P} \times \exp\left(\frac{E_{aN,aP}}{E} \right) = \tau_{0N,0P} \times \exp\left(\frac{E_{aN,aP}}{V} t_B \right) \tag{3.18}$$

where the subscript i is omitted, $E_{aN,aP}$ is called activation field, $\tau_{0N,0P}$ is the attempting time, V is the applied voltage.

On the other hand, polarization reversal can also be modeled as a creep process [182]. Eq. (3.18) can be further written as

$$\tau_{N,P} = \tau_{0N,0P} \times \exp\left(\frac{E_{aN,aP}}{V} t_B \right) = \tau_{0N,0P} \times \exp\left(\frac{U_{N,P} E_0}{k_B T} \cdot \frac{1}{V} t_B \right) \tag{3.19}$$

where $U_N$and U_P are the creep energy barrier for domain nucleation and domain wall propagation. E_0 is the characteristic field, T is the temperature, k_B is the Boltzmann constant.

However, for the case of ON-to-OFF switching, values of τ_{Ni} and τ_{Pi} were much smaller than expected by Merz's law. This was attributed to the existence of pinned down-polarized domains [183]. In our model and simulation, the experimental results of the ON-to-OFF switching were discarded since they show weak regularity. We assumed that both two switching directions follow Merz's law.

In Eq. (3.17) the values of N and λ_i are stochastic, depending on the fabrication process and material properties. For example, some experiments showed that domain nucleation prefers to occur at some particular sites, possibly where defects are situated [184]. These phenomena add the complexity into the modeling. For the sake of compactness, we simplified the ferroelectric film to be a uniform system governed by the identical τ_N and τ_P. Thus Eq. (3.17) is reduced to

$$\frac{\Delta P(t)}{2P_s} = h(t-\tau_N) \times \left\{ 1 - \exp\left[-\left(\frac{t-\tau_N}{\tau_P} \right)^2 \right] \right\} \tag{3.20}$$

Experimentally, this uniform ferroelectric film might be fabricated with a fully patterned and epitaxial process [12]. From the modeling point, Eq. (3.20) can still get relative good agreement with experiment results by setting appropriately parameters, as discussed in the next section.

3.1.4 Memristive model

In Section 3.1.1, a tunneling resistance model was developed to calculate the resistances for ON and OFF states. However, as mentioned in Section 2.1.3.2, the FTJ resistance is continuously adjustable between ON and OFF states due to the memristive effect. At the intermediate state, the FTJ resistance can be determined by Eq. (2.8), accordingly, the current can be written as

$$I = I_{ON}\left(1 - s_{OFF}\right) + I_{OFF} s_{OFF} \tag{3.21}$$

where I_{ON} and I_{OFF} are the currents corresponding to ON and OFF states, respectively, both of which can be calculated by Eqs. (3.7) and (3.9).

Eq. (3.21) gives the I-V characteristic of the FTJ at any domain configuration. But it fails to provide the relationship between the resistance and time. For that, an additional memristive model is required.

Following the description in Section 2.1.3.2, we set s_{OFF} to be the state variable (simplified to s), the memristive behavior of the FTJ can be described by *Chua*'s definition [78], as

$$\begin{cases} V = R(\mathrm{s}, V) I \\ \dfrac{ds}{dt} = f(\mathrm{s}, V) \end{cases} \tag{3.22}$$

where $\{V, R, I\}$ are voltage, resistance, and current. $f(s, V)$ is a system-dependent function.

Considering $s = \Delta P(t)/(2P_s)$ and combining Eqs. (3.20) and (2.8), Eq. (3.22) is written as

$$\begin{cases} V(t) = \dfrac{1}{\left[1 - s(t,V)\right] / R_{ON} + s(t,V) / R_{OFF}} \times I(t) \\ \dfrac{ds}{dt} = (1-s) \times \dfrac{2}{\tau_P(V)} \times \sqrt{\ln\left(\dfrac{1}{1-s} \right)} = f(s,V) \end{cases} \tag{3.23}$$

where $\tau_P(V)$ is given by Eq. (3.19). Note that Eq. (3.23) is available only for $t > \tau_N$. When $t < \tau_N$, s remains unchanged and therefore no memristive behavior occur. In the following text, $s(t)$ will be discussed under the premise of $t > \tau_N$, unless otherwise specified.

The key issue for this memristive model is to derive s at a given time t. In a circuit where the FTJ is connected with other devices, the voltage (V) across the FTJ is usually time-varying, resulting in a time-varying τ_P. Then $s(t)$ is given by

$$s(t) = s(t_0) + \int_{t_0}^{t} f\left[s, V(t)\right] dt \tag{3.24}$$

where $s(t_0)$ is the initial value at $t = t_0$.

In many cases, the analytical solution of $\int_{t_0}^{t} f[s, V(t)]dt$ cannot be derived. Therefore, we developed a low-complexity iterative algorithm to derive the numerical solution of Eq. (3.24). Assume that the time step is Δt, $t = t_0 + \Delta t$, if Δt is sufficiently small, $\tau_P(V)$ is consider a constant during the interval $(t_0, t_0 + \Delta t)$. Then $s(t)$ is given by

$$\begin{cases} t_r = \tau_P(V) \times \sqrt{\ln\left[\dfrac{1}{1 - s(t_0)}\right]} \\ s(t) = 1 - \exp\left\{-\left[\dfrac{t_r + \Delta t}{\tau_P(V)}\right]^2\right\} \end{cases} \tag{3.25}$$

where t_r is derived from Eq. (3.20) by assuming $\tau_N = 0$. It is the relative time corresponding to $s(t_0)$ in a single KAI process. An example shown in Figure 3.9 explains the principle of Eq. (3.25). In this example, the write voltage is changed at time t_0. Therefore the switching processes during $0 \sim t_0$ and $t_0 \sim t_0 + \Delta t$ are described by two KAI curves (the red and the blue, respectively) with different τ_P (see Figure 3.9(a)). Using Eq. (3.25), we can obtain a continuous curve of $s(t)$, which consists of two segments cut out from the respective KAI curves (see Figure 3.9(b)).

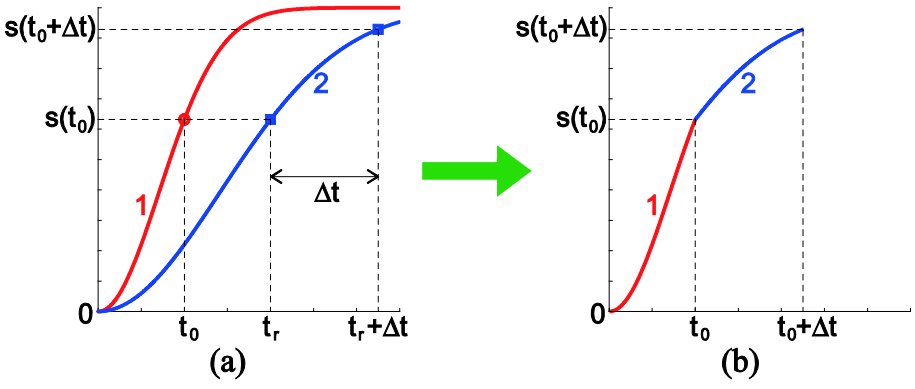


Figure 3.9 Schematic explaining the algorithm of Eq. (3.25).

Note that the state variable s refers to s_{OFF} in Eqs. (3.23) and (3.25), thus the voltage V should be positive to drive the growth of the OFF-state domain. Otherwise, s should be replaced with $s_{ON} = 1 - s_{OFF}$ if the voltage V is negative.

The accuracy of the proposed memristive model was validated by a relative good agreement between the model simulation and experimental measurement, as shown in Figure 3.10, where various types of pulses shown in Figure 3.10 (c)–(d) were applied to write (or program) and read the FTJ. In each period, the FTJ resistance was measured by a 100 mV readout pulse following the write pulse (see the insets of Figure 3.10 (c)–(d)). The experimental results were extracted from Ref. [12]. The simulation results were obtained based on Eqs. (3.19), (3.21) and (3.25). The time step for the simulation was set to 0.1 ns. Other parameters were configured based on the experimental measurement. R_{on} and R_{off} at 100 mV were set to 1.6×10^5 Ω and 4.6×10^7 Ω, respectively. $\tau_{P0} = 9 \times 10^{-14}$s. U_p was set to 0.52 eV and 0.56 eV for Figure 3.10(a) and (b), respectively.

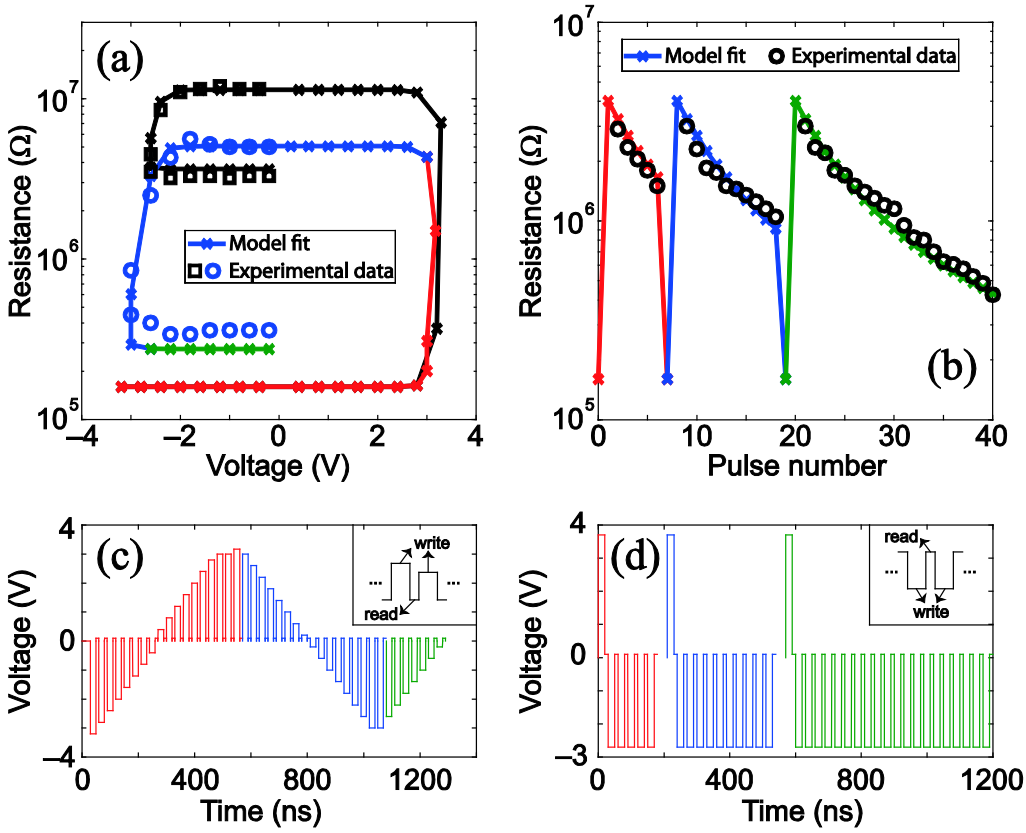


Figure 3.10 Relative good agreement between experimental data and model fit. Note that the applied pulses for the black hysteretic loop of (a) are not shown in (c).

In Figure 3.10(a), a series of 20 ns programming pulses with different amplitudes were applied to the FTJ. It is seen that the change in the resistance is dependent on the programming pulse amplitude. Moreover, the scope of the hysteretic loop can be modulated by changing the peak value of the programming pulses. In Figure 3.10(b), three groups of resistance results are shown. For each group, the FTJ was firstly set to the same state (~4 MΩ), then repetitive programming pulses with the same amplitude (–2.7 V) and duration (20 ns) were applied to the FTJ. The number of the pulses was set to 5, 10 and 20 for three groups, respectively. Clearly, the FTJ can be programmed to the different state by changing the number of the programming pulses. In other words, the FTJ resistance can be adjusted by changing the duration of the programming pulse. All of these results not only provide the direct evidence of the memristive behavior of the FTJ, but also validate the accuracy of the proposed memristive model.

3.1.5 Discussion on the static switching model

Generally, a static switching model calculates the threshold voltage (or current) for switching the device state. Below the threshold value, the switching is impossible regardless of the duration of the applied pulse. Since the FTJ is a voltage-controlled device, this threshold value refers to the coercive voltage (or coercive field) of the ferroelectric film. Theoretically, intrinsic ferroelectric coercive field can be calculated with Landau-Ginzburg (LG) mean-field theory [185]–[186], which gives a polynomial expansion of the free energy density, as

$$G = F_0 + \frac{\alpha'}{2}P^2 + \frac{\beta'}{4}P^4 + \frac{\gamma'}{6}P^6 - P \cdot E \tag{3.26}$$

where F_0 is the free energy of the paraelectric phase at zero electric field, α' is temperature-dependent coefficient, β' and γ' are considered to be independent on the temperature, P is the ferroelectric polarization, E is the applied electric field.

At the thermodynamic equilibrium, the free energy density is minimum, which gives

$$\frac{\partial G}{\partial P} = 0 \Rightarrow E(P) = \alpha' P + \beta' P^3 + \gamma' P^5 \tag{3.27}$$

The inverse function of the Eq. (3.27) describes the polarization hysteresis $P(E)$, as shown in Figure 3.11. The coercive field E_c corresponds to the turning point of $P(E)$, as

$$\begin{cases} \left.\dfrac{\partial E}{\partial P}\right|_{P=P_r} = 0 \\ E_c = \alpha' P_r + \beta' P_r^{\,3} + \gamma' P_r^{\,5} \end{cases} \tag{3.28}$$

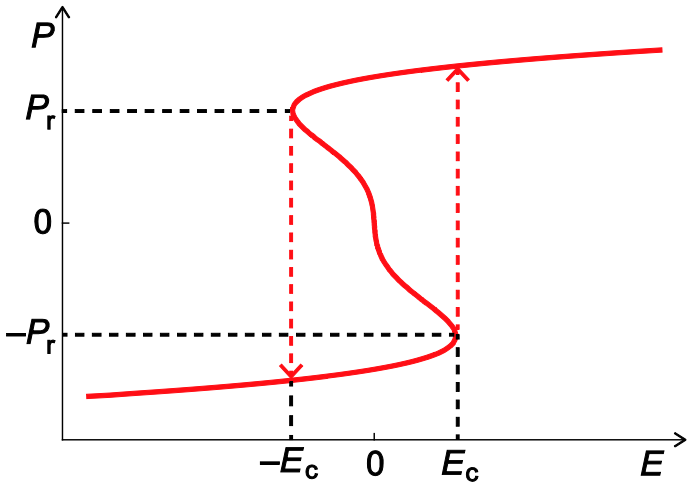


Figure 3.11 P(E) curve calculated by Eq. (3.27).

The LG mean-field theory is established from the viewpoint of the thermodynamic equilibrium. It describes the ferroelectric switching as a process of collective polarization reversal. However, as mentioned in Section 3.1.3, real ferroelectric polarization reversal is activated by the localized domain nucleation around the defects, which is not taken into account by the LG mean-field theory. As a result, the experimentally measured coercive field is mostly much smaller than the intrinsic value predicted by the LG mean-field theory. Actually, as pointed out by some researchers [187]–[188], one cannot define a true coercive field for the ferroelectric polarization reversal because the domain nucleation can occur at an arbitrarily small field if the duration of the applied pulse is long enough. In fact, experimentally measured coercive field is a function of the frequency of the applied pulse. The static switching threshold can be approximated by the coercive voltage measured at the very low frequency.

Experimentally measured coercive field is strongly related to the film thickness [189]–[195]. Generally, the coercive field decreases as the thickness increases, but the quantitative results observed by many groups are different from each other. Various theories have been proposed to explain their respective results. Among them, a famous semi-empirical law was developed by Janovec [196], Kay and Dunn [189], as

$$E_c \propto {t_B}^{-2/3} \tag{3.29}$$

which is called JKD scaling law and has been verified in several thick samples (typically, > 100 nm) [45], [189], but it disagreed with the experimental results of some ultrathin films [194]–[195]. *M. Dawber* suggested that depolarization field should be taken into account to correct the JKD scaling law [197]. In addition, other mechanisms have also been proposed to explain this disagreement [194]–[195]. But in conclusion, all these proposals are very material and fabrication process-specific. It is impossible to develop a universal theory of the coercive field suitable for all the ferroelectric devices.

Base on the above analysis, we will not propose the static switching model for the FTJ. Depending on the frequency of the write pulse in a simulation task, we can set a pseudo-threshold voltage below which the change in the FTJ resistance is enough tiny to be negligible. For instance, in Figure 3.10(a), the threshold voltage can be considered around 2.8 V for a 20 ns write pulse.

3.2 Electrical model of the FTJ for the circuit simulation

3.2.1 Modeling language

In order to simulate and analyze the hybrid CMOS/FTJ circuits, it is indispensable to develop an electrical model of the FTJ. For that, we need to choose an appropriate hardware description language to model the physical behaviors of the FTJ. Recently, various languages and tools have been used for the compact modeling of emerging electron devices, such as *SPICE* [198]–[199], *C* [200], *VHDL-AMS* [201], *Verilog-A* [202]–[204]. Among them, *Verilog-A* language is considered to be a good choice due to the following advantages.

First, *Verilog-A* supports the description of the analog system and allows to process continuous-time signals [35]. Second, it is compatible with the standard circuit simulation tools (e.g. *Cadence* platform) and can run in a variety of circuit simulators (e.g. *Spectre*, *Eldo*, *ADS*). Third, it provides a user-friendly interface and good programming flexibility, which makes it easy to maintain and update the model with the progress of the FTJ technology.

3.2.2 Model parameters

Like in Section 3.1, the parameter values were determined by the fitting of experiment results. Since those sub-models presented in Section 3.1 need to be integrated into a complete electrical model, the experimental data for the fitting must be extracted from the identical literature for the sake of consistency. However, in Section 3.1 tunneling resistance model were fit with Ref. [10] but dynamic switching and memristive models with Ref. [12]. Actually, these two literatures are

from the same group and present the similar FTJs. Here, Ref. [12] is selected for the fitting since it is more recent than Ref. [10].

Following the experimental results from Ref. [12], we determined all the parameter values, which are summarized in Tables 3.3–3.7 with a list of constants. Among them, only size parameters and simulation environment parameters are user-reconfigurable. Other parameters are assumed to be dependent on the fabrication process and cannot be modified.

Table 3.3 Size parameters

Parameters	Description	Default value
t_B	Barrier thickness	2 nm
r	Junction surface radius	175 nm

Table 3.4 Simulation environment parameters

Parameters	Description	Default value
Δt	Time step for the simulation	100 ps
s_0	Initial fraction of the OFF-state domain	5×10^{-5}
T	Temperature	300 K

Table 3.5 Parameters for the dynamic switching memristive models

Parameters	Description	Default value
U_N	Creep energy barrier for the domain nucleation	0.67 eV
U_P	Creep energy barrier for the domain wall propagation	0.52 eV
τ_{0N}	Attempt time of the domain nucleation	2.8×10^{-15} s
τ_{0P}	Attempt time of the domain wall propagation	9×10^{-14} s

Table 3.6 Parameters for the tunneling resistance model

Parameters	Description	Default value	
		ON state	OFF state
φ_1	Barrier potential height at LSMO/BTO interface	0.53 V	0.678 V
φ_2	Barrier potential height at Co/BTO interface	1.014 V	0.978 V
m	Effective electron mass	0.437 m_e	0.931 m_e
F_1	Scaling factor for	3.549×10^{-4} for V > 0	2.6×10^{-3} for V > 0

	the FNT model	3.273×10^{-4} for V < 0	1.2×10^{-3} for V < 0
F_2	Scaling factor for the FNT model	9.41×10^{-2} for V > 0 1.2×10^{-3} for V < 0	0.7608 for V > 0 0.283 for V < 0

Table 3.7 General constants

Constant	Description	Value
m_e	Free electron mass	9.11×10^{-31} kg
e	Elementary charge	1.6×10^{-19} C
$\hbar$	Reduced Planck constant	1.054×10^{-34} J·s
k_B	Boltzmann constant	1.38×10^{-23} J/K
E_0	Characteristic field	1 GV/m

In Table 3.5, the accuracy of the parameter values for dynamic switching and memristive models has been validated in Sections 3.1.3–3.1.4. However, in Table 3.6 the parameter values for the tunneling resistance model are different from those in Table 3.2 since Ref. [10] used in Section 3.1.1 is replaced with Ref. [12] here. Table 3.6 is not easily determined because there are only a few available I-V data in Ref. [12]. Here the listed values were obtained based on a number of attempts and adjustments. These values give a complete I-V curve shown in Figure 3.12. From this curve, the transition voltages between the DT and FNT are $-\varphi_1$ and φ_2. i.e. (–0.53 V, 1.014 V) for ON state and (–0.678 V, 0.978 V) for OFF state, consistent with the discussion in Ref. [171]. In addition, some points in this curve can achieve good agreement with experimental measurement. For example, at 0.1 V, the resistances for ON and OFF states are 1.6×10^5 Ω and 4.6×10^7 Ω, respectively; at –2.5 V, the current for ON state is 170 μA; at 2.5 V, the current for OFF state is 100 μA. These values are very close to experimental results [12].

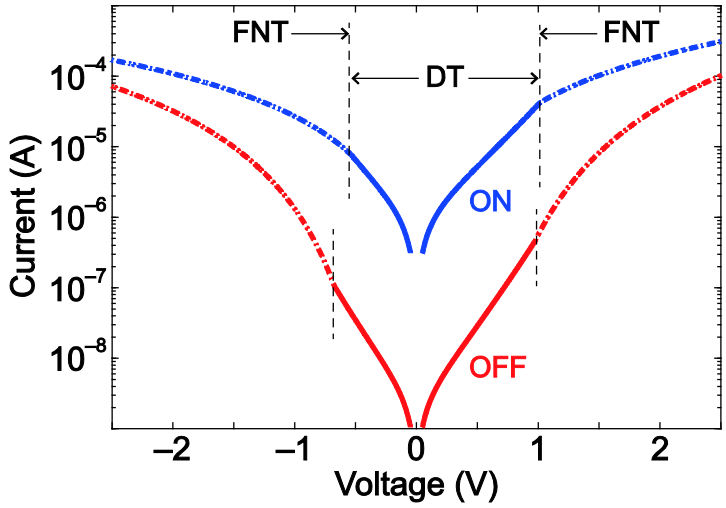


Figure 3.12 Complete I-V curve obtained from the developed model.

Since there are no more experimental I-V results in Ref. [12], the accuracy of the parameter values in Table 3.6 cannot absolutely be confirmed. Nevertheless, the dependences of current on the physical parameters are still correctly described by the tunneling resistance model (i.e. Eqs. (3.7) and (3.9)). In the following simulation of Chapter 4, when it comes to I-V characteristic, we will pay more attention to the qualitative conclusion than quantitative results.

In addition, for a specific simulation task, sometimes the barrier thickness (t_B) need to be changed to observe its influence on the performance. The change in t_B might induce the variation of some technology parameters (e.g. barrier potential $\varphi_{1,2}$). But this effect has not been well quantitatively studied, thus our model assumes that the technology parameters are independent on t_B. With this assumption, the transition voltages between the DT and FNT are the same for various t_B. To keep continuity of I-V curve at the transition voltages, scaling factor F_1 needs to be modified with the change in t_B. Considering that the unit cell of BTO is 0.4 nm, we set additional three values for t_B: 1.2 nm, 1.6 nm and 2.4 nm. Corresponding values of F_1 and complete I-V curve are shown in Table 3.8 and Figure 3.13, respectively.

Table 3.8 Values of F_1 for various barrier thicknesses

	t_B = 1.2 nm		t_B = 1.6 nm		t_B = 2.4 nm	
	ON state	OFF state	ON state	OFF state	ON state	OFF state
V > 0	7.211×10^{-3}	3.739×10^{-2}	1.605×10^{-3}	9.795×10^{-3}	7.843×10^{-5}	6.707×10^{-4}
V < 0	1.354×10^{-2}	3.55×10^{-2}	2.133×10^{-3}	6.517×10^{-3}	4.964×10^{-5}	2.168×10^{-4}

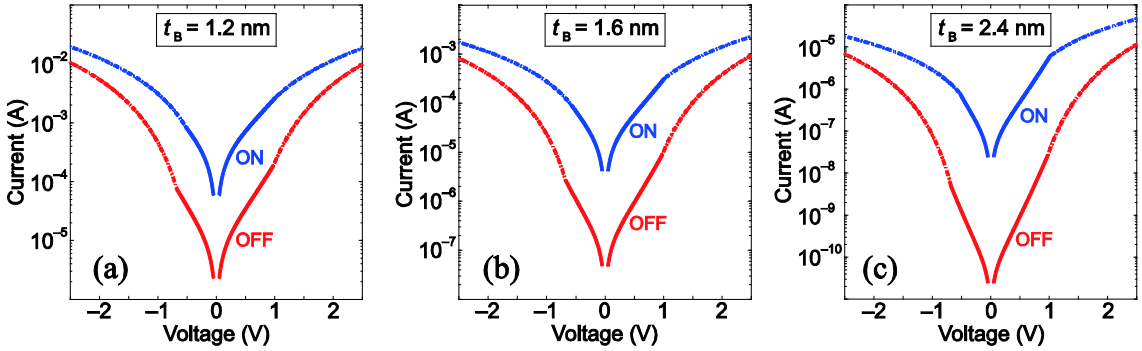


Figure 3.13 I-V curves for various barrier thicknesses.

3.2.3 Model hierarchy

The hierarchy of the developed electrical model is illustrated by Figure 3.14. The main physical equations are mathematically described with *Verilog-A* language. 14 parameters and 5 constants feed into this model. We assumed that the switching must experience nucleation process if and only if the volume fraction of the switched domain is smaller than 10^{-4}. This model resolves the FTJ state at each time step (Δt) by means of the iterative calculation. The output at the present time $t_0 + \Delta t$ is dependent on the device state at previous time t_0, in agreement with memristive effect. Generally, Δt should be no larger than the period of the applied pulse to guarantee the accuracy. A smaller Δt can improve the precision of the results, but decreases the simulation speed, which forms a tradeoff between them.

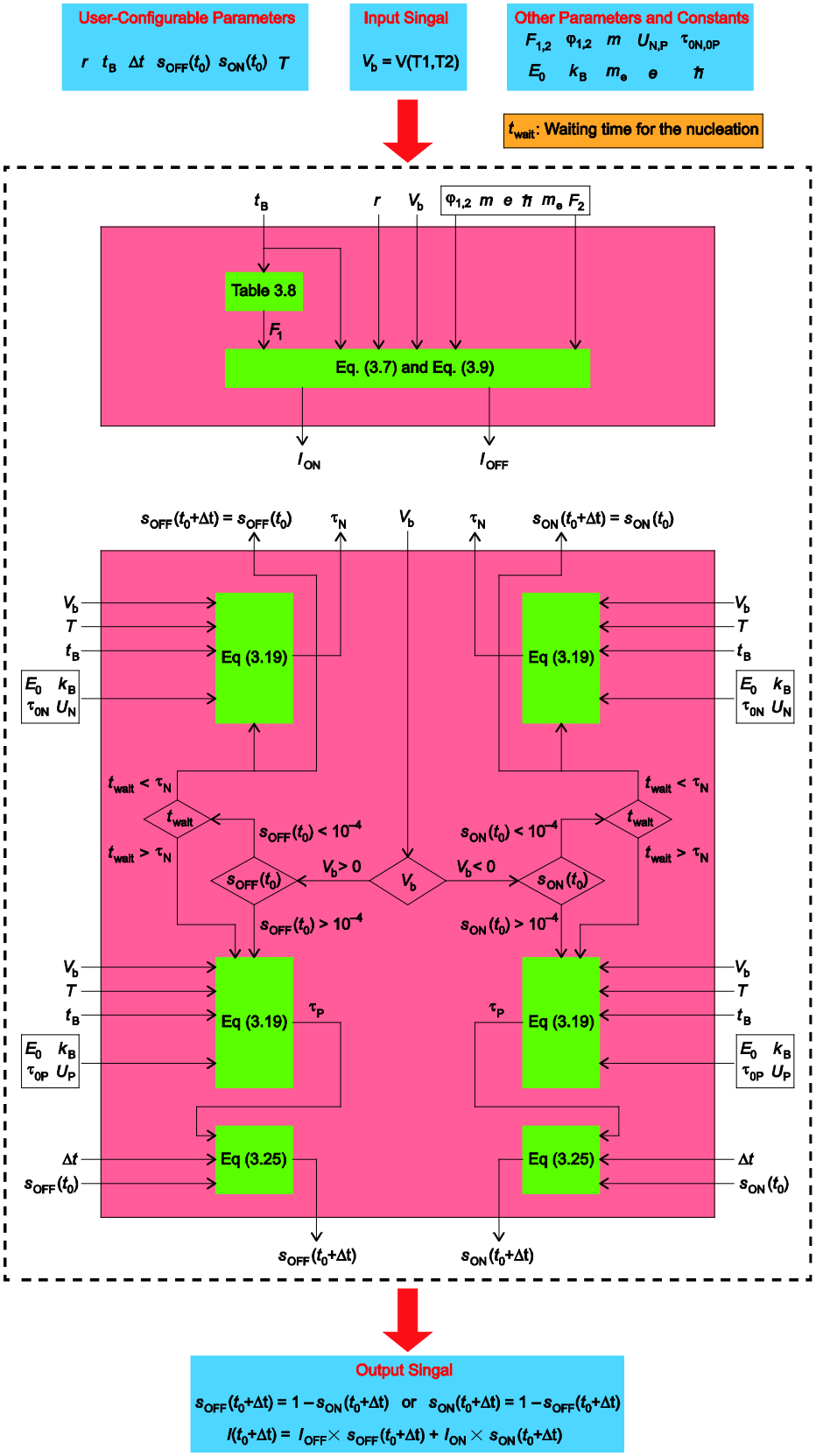


Figure 3.14 Hierarchy of the developed FTJ model.

Figure 3.15 shows the symbol of the developed electrical model on *Cadence* platform. Three terminals are defined: 'T1' and 'T2' are real terminals corresponding to Co and LSMO electrodes, respectively. 's' is a virtual terminal which outputs the value of s_{OFF} ranging from 0 to 1. The arrows show the polarization orientations corresponding to ON and OFF states. They also indicate the polarities of the applied voltage for two switching directions. If the potential of 'T1' is higher than that of 'T2', the FTJ is programmed towards OFF state and conversely towards ON state.

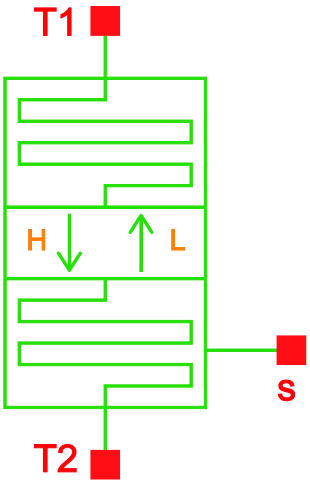


Figure 3.15 Symbol of the developed FTJ model on Cadence platform.

3.2.4 Validation of the electrical model

We performed single-cell simulation to validate the function of the developed FTJ electrical model. The schematic is shown in Figure 3.16, where a user-defined pulse was applied to a single FTJ. The current and s_{OFF} were monitored at terminals 'T1' and 's', respectively.

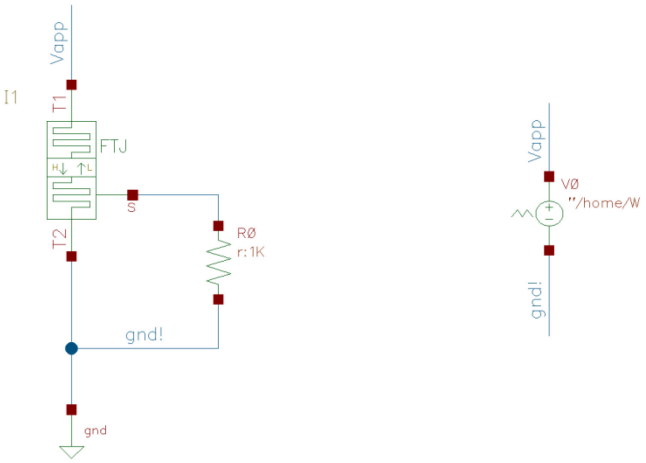


Figure 3.16 Schematic for the single-cell simulation.

Firstly, pinched I-V hysteresis loop, which is regarded as the typical characteristic of a memristor, was reproduced by simulation results shown in Figure 3.17. These results were obtained by sweeping voltage from –2.5 V to 2.5 V and then back to –2.5 V (as the arrows in Figure 3.17(a) and (d)), at a 0.1 V interval. The initial domain configuration was set to $s_{OFF} = 0.9999$. The simulation time step was set to $1/(10f)$, where f is the sweeping frequency. The barrier thickness was successively set to 2 nm and 1.6 nm during the simulation. The other parameters were configured as Tables 3.3–3.8.

Figure 3.17(a) and (b) show the comparison of I-V loops between different sweeping frequencies (1 kHz and 100 Hz), while (a) and (c) show the comparison between different barrier thicknesses (2.0 nm and 1.6 nm). Figure 3.17(d) is the same results as Figure 3.17(a) in log scale. It is seen that the profile of I-V loop curve can be adjusted by changing the sweeping frequency and barrier thickness. The switching voltage decreases as the sweeping frequency or barrier thickness decreases, as expected by Merz's law (i.e. Eq. (3.19)). Moreover, the result in Figure 3.17(a) is in relative good agreement with the experiment measurement [12].

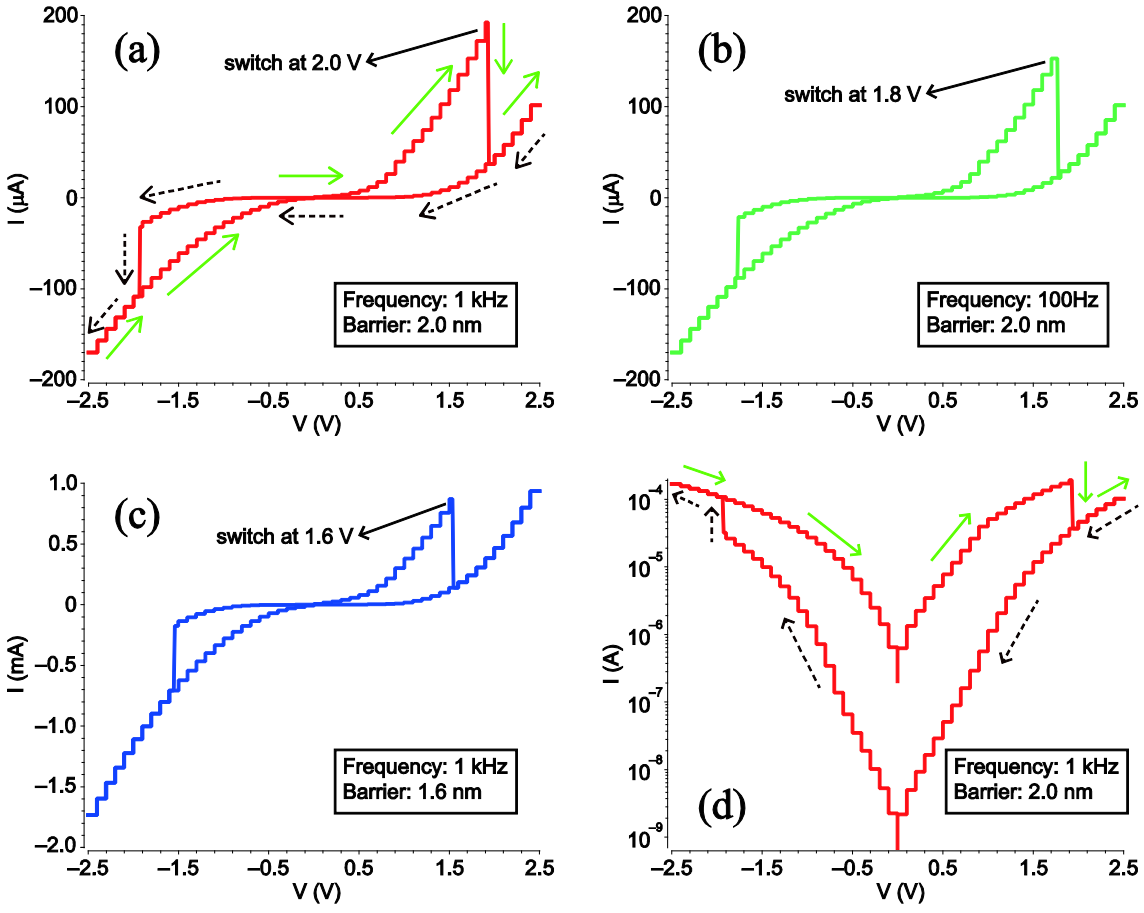


Figure 3.17 I-V pinched hysteresis loops simulated with the developed model.

Afterwards, transient simulation was performed to demonstrate the domain growth and resistance variation under the action of a user-defined pulse, as shown in Figure 3.18. During 5~15 ns, a negative write pulse of –4 V sets the FTJ to the fully ON state, which is confirmed by $s_{OFF} = 0$. During 25~35 ns, a positive write pulse of 3.75 V activates the domain nucleation and domain wall propagation. During the domain nucleation, the FTJ is still at fully ON state and thus the resistance does not change, which is verified by an invariable current at 25~27.8 ns of Figure 3.18(c). Then, during 45~125 ns, two negative and two positive write pulses with an amplitude of 3.25 V are successively applied to program the FTJ. As expected, the back-and-forth growth of the domain can be clearly seen. In the whole simulation, each write pulse is followed by a read pulse of 0.1 V, it is seen that the read current increases or decreases with the decrease or increase of s_{OFF}. These results validate the voltage-controlled memristive behavior of the FTJ.

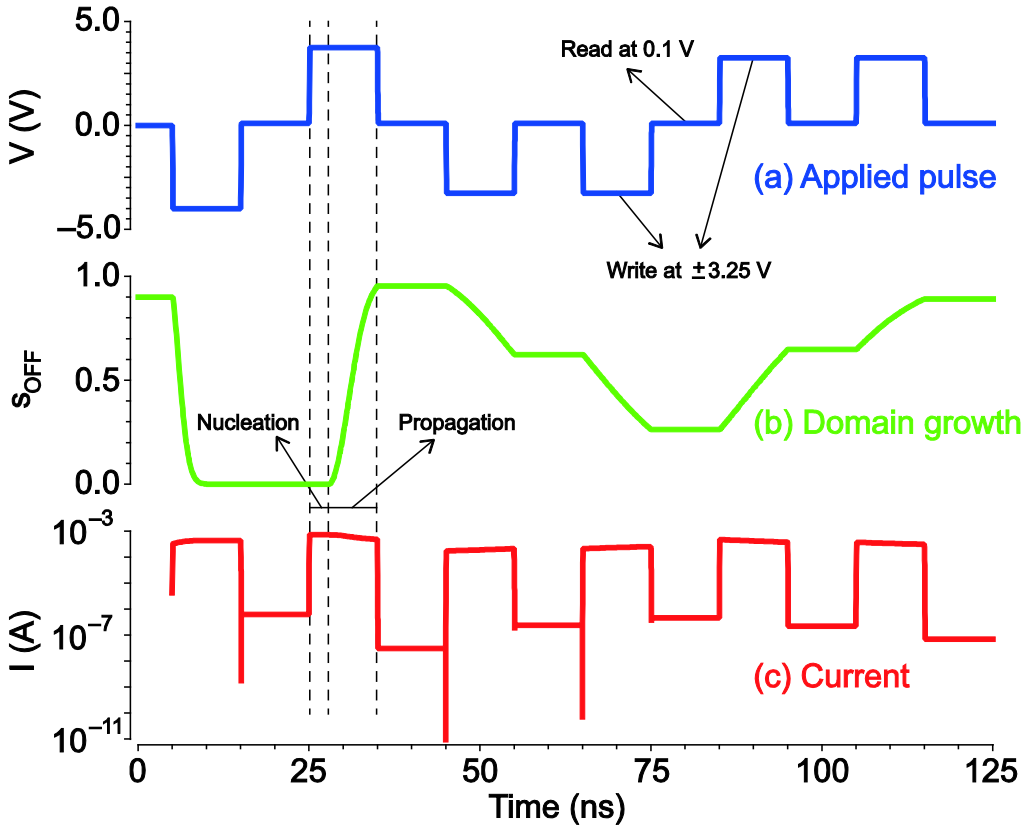


Figure 3.18 Transient simulation with the developed electrical model.

3.3 Conclusion

We have developed a compact electrical model of the FTJ based on the physical theories and experimental results. This model includes four interconnected modules: firstly, it calculates the

tunneling resistances for ON and OFF states with *Gruverman* model (at low-voltage regime) and FNT theory (at high-voltage regime). Secondly, it describes the dynamic switching behavior with KAI model, Merz's law and creep process. Thirdly, it links the memristive effect to a parallel resistor model governed by ferroelectric domain kinetics. Finally, an iteration algorithm was developed to resolve the time-dependent memristance. In addition, TER ratio model and static switching mechanism were also discussed to provide more knowledge. Aforementioned physical models gave a good fit to the experimental results, validating the accuracy of our compact model.

The developed model was programmed with *Verilog-A* language, which makes it compatible with standard circuit simulation tool (e.g. *Cadence*). The single-cell simulation was performed with our model to reproduce the electrical behavior of the FTJ. As expected, clear pinched I-V loop and voltage-controlled memristance were obtained.

Our compact model paves the way for the simulation and analysis of hybrid CMOS/FTJ circuits. As a result, the application potential of the FTJ in the non-volatile circuits or neuromorphic systems can be evaluated by means of simulation, which will be discussed in the next chapter.

Chapter 4

Circuit design and simulation based on the FTJ

4.0 Preface

By using the FTJ electrical model developed in Chapter 3, we can simulate and analyze various FTJ-based non-volatile circuits to explore the potential applications of FTJs. In this chapter, the FTJ is applied to three typical fields: Firstly, it is used as a binary memory cell in an FTJ-based random access memory (FTRAM). The read/write performances are discussed by analyzing the simulation results. Secondly, the FTJ serves as the synapse in two proposed neuromorphic systems, which implements the spike-timing dependent plasticity (STDP) learning rule and an on-chip supervised learning, respectively. Finally, inspired by the emerging NV logic block, we propose to implement Boolean logic function inside a single FTJ. NAND and NOR logic functions are demonstrated in an FTJ-based logic block.

4.1 FTJ-based random access memory

In this section, we design and simulate an FTJ-based random access memory (FTRAM) with the developed FTJ model and *STMicroelectronics* CMOS 40 nm design kit [37]. Simulation results are analyzed to evaluate the influence of the device parameters on the read/write performance.

4.1.1 Memory architecture

The architecture of a random access memory should include at least memory cells, read/write circuits, bit lines (BLs), source lines (SLs), word lines (WLs) and decoders. Among them, memory cell and read/write circuits should be particularly designed to meet the performance requirement.

First of all, the structure of memory cell needs to be established. Initially, we tried the conventional 1T1R cell used in other memories (e.g. MRAM [140]), which is the same as Figure 2.21(a) except for replacing the MTJ with an FTJ. Since typical RAM requires a nanosecond-order write speed, the write voltage for the FTJ should be 3~4 V (see simulation results in Figure 3.18). In order to support such a high voltage, the transistor should be equipped with a thick oxide and large channel area. Therefore, we selected n-channel MOS (NMOS) transistor ‘nsvt25’ from *STMicroelectronics* CMOS045 library to construct the 1T1R cell [37]. The channel length of ‘nsvt25’ is 270 nm. Actually, a voltage of 3~4 V is still dangerous to this transistor, thus additional protection technology is required. Such a high write voltage limits the integration capability of the FTJ with nanoscale CMOS technology.

A typical simulation example based on 1T1R cell is shown in Figure 4.1, where the parameters of the FTJ were set to the default values shown in Tables 3.3–3.6 (In this chapter, “default values” always means these values, unless otherwise specified), and the width/length

(W/L) of the transistor was set to 10. Note that 'T1' of the FTJ is connected to the access transistor, thus applying a positive voltage to 'BL' will drive OFF-to-ON switching.

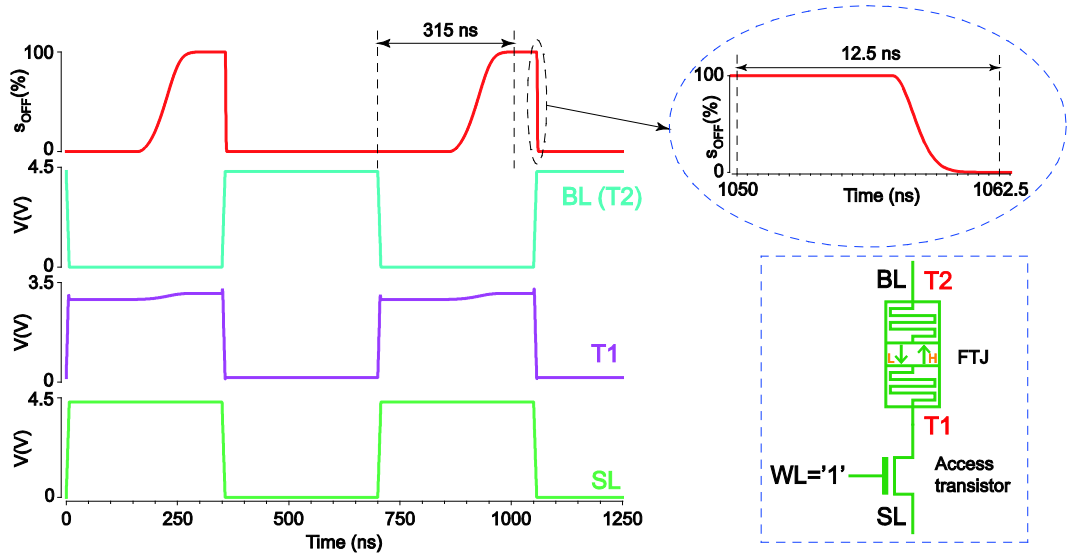


Figure 4.1 Simulation results of the write operation based on 1T1R cell.

Unfortunately, 1T1R cell causes the asymmetry between two write directions. It is seen that the write delay of ON-to-OFF switching is much larger than that of OFF-to-ON switching (315 ns versus 12.5 ns). The reason for this asymmetry is that the drive capability of the access transistor is unequal for two write directions. When the positive voltage as high as 3~4 V is applied to 'SL', the NMOS transistor suffers from serious threshold-loss problem. As a consequence, the effective write voltages allocated to the FTJ are different for two write directions. Merz's law (see Eq. (3.18)) indicates that the write delay is exponentially dependent on the write voltage, thus a small change in write voltage can induce a huge difference of write delay. Even if the FTJ are reversely connected (i.e. 'T2' is connected to the access transistor), the asymmetry cannot be eliminated.

In reality, the asymmetry may be not so significant because the ON-to-OFF switching is experimentally demonstrated to be faster than expected by Merz's law [12]. However, here we aim to solve the asymmetry from the viewpoint of circuit design. Therefore, we replaced the access transistor with an access transmission gate (TG), which can eliminate the threshold-loss problem and relieve the asymmetry but at the expense of a more complicated process and a larger cell area.

The overall structure of the FTRAM is shown in Figure 4.2(a). WL and its opposite state are connected to two gates of the access TG through an inverter. BL and SL are connected to the FTJ and the transistor sources, respectively. To read/write a memory cell, the corresponding WL is activated to turn on the TG, and read/write signals are applied to the cell through BL and SL.

Considering the drive capability of p-channel MOS (PMOS) transistor is worse than that of NMOS transistor [205], we connect 'T1' to the BL in order that a positive voltage applied to 'SL' can drive OFF-to-ON switching and that the initial OFF state enables FTJ to obtain large enough voltage for triggering the switching process.

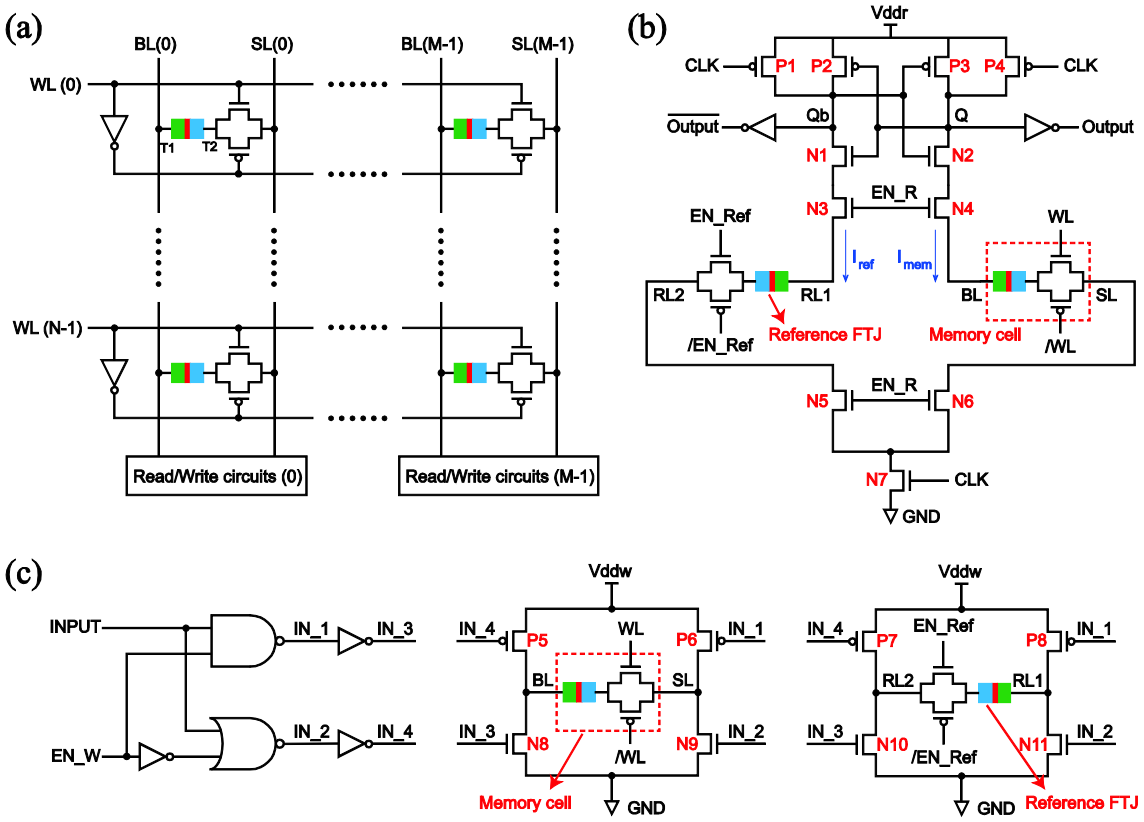


Figure 4.2 (a) Architecture of an N × M bits FTRAM, (b) read circuit and (c) write circuit.

The read circuit is implemented with a pre-charge sensing amplifier (PCSA) [206] shown in Figure 4.2(b). It consists of the left and the right branches, each of which includes a charging transistor (P1 or P4), an inverter (P2+N1 or P3+N2), and two isolating transistors (N3+N5 or N4+N6). A discharging transistor N7 is shared by two branches. A reference cell is connected to the left branch through an access TG, and likewise a memory cell to the right branch. Two FTJs in the memory and reference cells are always written to the opposite states by the write circuits (see Figure 4.2(c), will be explained later). The stored binary information is represented by the ON or OFF state of the memory FTJ (in the right branch). The resistance difference between two FTJs can be translated into a binary output at 'Q' by the PCSA. Note that the FTJ is readout at a small bias voltage, thus PCSA can be designed with low-power low-threshold transistors ('nlvtlp' and

'plvtlp' from *STMicroelectronics* CMOS045 library), whose channel width is 40 nm. Detailed operation will be described in Section 4.1.2.

The write circuit is shown in Figure 4.2(c), including several logic gates and two groups of drive transistors (P5+P6+N8+N9 and P7+P8+N10+N11). 'EN_W' = '1' enables the write operation, and vice versa. The 'INPUT' state determines the polarities of the write voltages across the memory and reference FTJs. Two FTJs are reversely placed with respect to the drive transistors in order that they are always switched to the opposite states. For instance, 'EN_W' = '1' and 'INPUT' = '1' will activate drive transistors (P6, N8, P8, N10) and deactivate the others. In this case, a positive write voltage is applied to the memory FTJ from 'T2' to 'T1', while a negative write voltage to the reference FTJ. The change of 'INPUT' reconfigures each group of drive transistors and reverses the polarities of two write voltages. As a result, the 'INPUT' data can be written into the FTJs.

4.1.2 Simulation and validation

Figure 4.3(a) shows the transient simulation of the proposed FTRAM. The memory capacity was set to 4×8 bits, but here only one bit of them is shown for the sake of clarity. Some parameters were configured as Table 4.1, the other parameters were set to the default values. In the access TG, the W/L of the PMOS transistor was set to 1.3 times that of the NMOS transistor so that the asymmetry between two write directions can almost be eliminated. As can be seen from the results, 'INPUT' is written into the cell through the polarization reversal of the memory and reference FTJs during 'EN_W' = '1'. The state of the FTJ is read at 'Output' during the rising edge of 'CLK'.

Table 4.1 Parameters for the transient simulation of the proposed FTRAM

Parameters	Values	Parameters	Values
W/L of the drive transistors	35	Vddr	1.1 V
W/L of the transistors in the access TG	NMOS: 5 PMOS: 6.5	Vddw and V_{WL}*	4 V and 4.2 V
W/L of transistors in the PCSA	3	Rise time and fall time of the applied pulses	100 ps

* The voltage applied to the WL while accessing one cell.

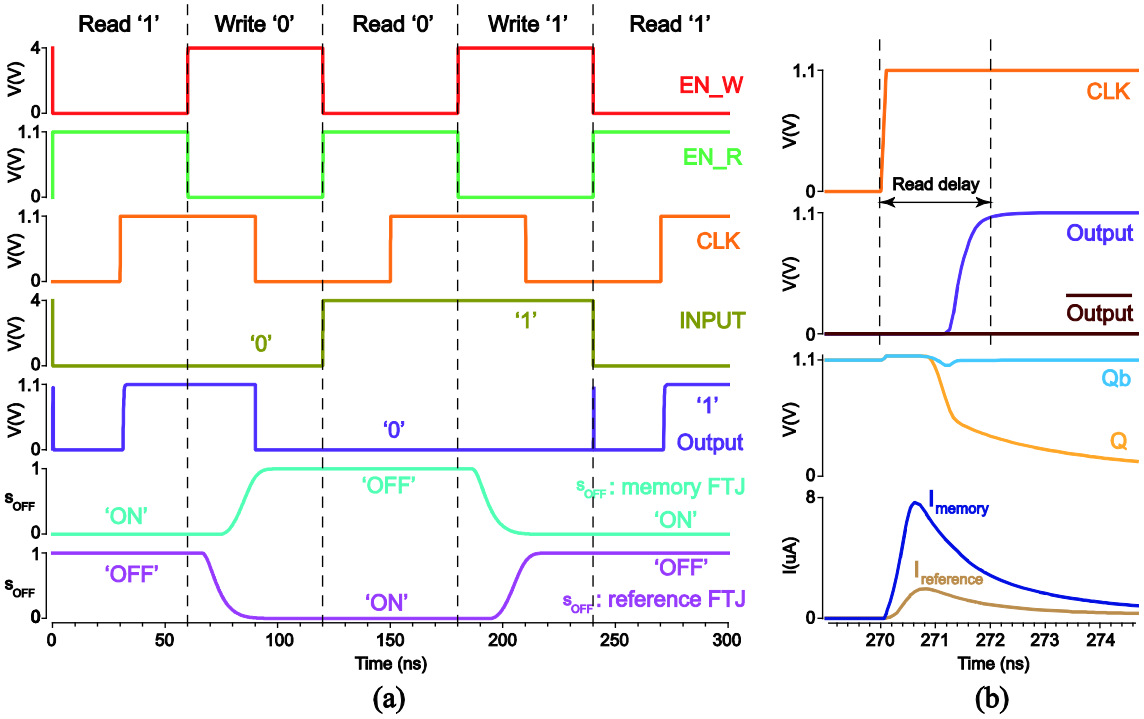


Figure 4.3 (a) Transient simulation of the proposed FTRAM, (b) Transient signals of the PCSA while reading '1' around t = 270 ns.

The read operation of the PCSA is illustrated by the simulation results shown in Figure 4.3 (b). Here we take reading '1' for example, i.e. the resistance of the memory FTJ is smaller than that of the reference FTJ. The read operation includes two phases as follows.

i) During the pre-charging phase, 'CLK' = '0'. N7 is deactivated to isolate the PCSA from 'GND'. P1 and P4 are activated in order that both 'Q' and 'Qb' are pulled up to 'Vddr'.

ii) During the evaluation phase, 'CLK' jumps from '0' to '1'. P1 and P4 are deactivated to isolate the PCSA from 'Vddr'. N7 is activated to form two discharging paths from 'Q' and 'Qb' to 'GND' through the memory and reference FTJs, respectively. As the resistance of the memory FTJ is smaller, the discharging current through the memory FTJ (I_{mem}) is larger than that through the reference FTJ (I_{ref}). Moreover, the discharging speed of the right branch is faster than that of the left branch. In this case, 'Q' decreases to the threshold voltage of PMOS transistor earlier than 'Qb', as a result, P2 is activated to pull up 'Qb' to 'Vddr' (logic '1') while 'Q' continues to decrease to 'GND' (logic '0').

4.1.3 Read performance

The read performance is firstly evaluated in terms of delay and energy. The influences of various device parameters will be discussed. Except for the concerning parameter, other parameters were

set to the values shown in Tables 3.3–3.6 and 4.1 (the same in the next Section 4.1.4). We only considered the case of reading '1', but our conclusion is also applicable for reading '0'. The read delay is defined as the difference between the rising edge of 'CLK' and the time when the level of 'Output' increases to $0.9 * \mathrm{Vddr} = 990$ mV (see Figure 4.3(b)). The read energy is calculated by

$$E_r = Vddr \times \int_{t_{r1}}^{t_{r2}} i_r(t)dt \tag{4.1}$$

where $t_{r2} - t_{r1}$ is the read delay defined above, $i_r(t)$ is the total current flowing through the power supply.

4.1.3.1 Dependence on the FTJ size

Figure 4.4 shows the read performance as a function of the FTJ area under the various barrier thicknesses. As is indicated in the figure, the FTJ with a larger area gives a smaller read delay and a lower read energy. This is explained as follows. For the FTJ, when its area increases, its resistance decreases (see Eq. (3.7)), then the discharging currents in the PCSA increase while the discharging time constant decreases according to Eqs. (4.2) and (4.3). Hence, it takes less time for 'Q' or 'Qb' to fall to the threshold of PMOS transistor, resulting in a smaller read delay. The read energy also decreases thanks to the reduction of the read delay.

$$I_{mem,\,ref} \simeq \frac{Vddr}{R_{MOS} + R_{FTJ\_mem,\,FTJ\_ref}} \tag{4.2}$$

$$\tau_{mem,\,ref} \simeq R_{FTJ\_mem,\,FTJ\_ref} C_{MOS} \tag{4.3}$$

where R_{MOS} and C_{MOS} are the total resistance and parasitic capacitance associated with each branch, respectively. R_{FTJ_mem} and R_{FTJ_ref} are the resistances of the memory and reference FTJs, respectively.

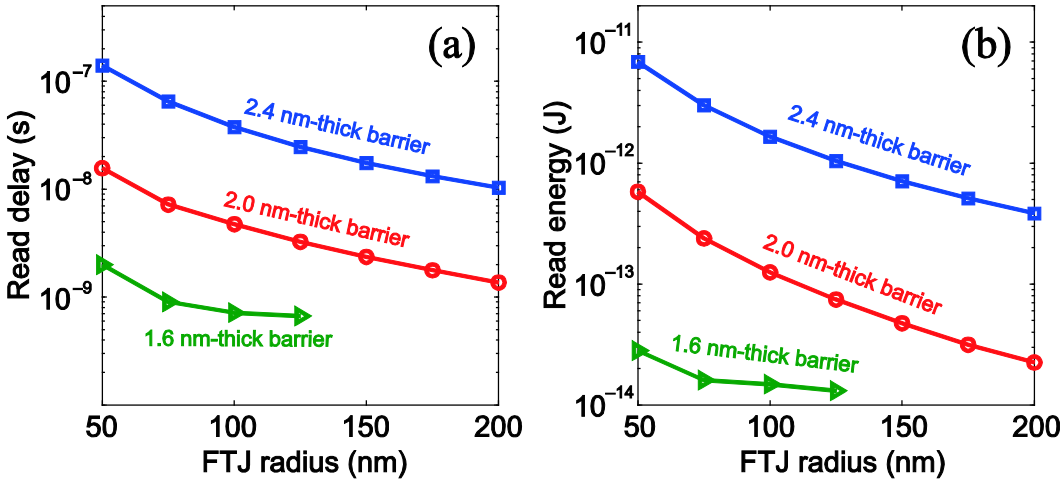


Figure 4.4 FTRAM read delay (a) and read energy (b) versus the FTJ size.

From Figure 4.4, given the same FTJ area, the read speed and read energy can be improved by using a thinner barrier. The reason is similar to the aforementioned explanation: a thinner barrier leads to a smaller FTJ resistance (see Eq. (3.7) and Figure 3.13) and then to a larger discharging current and a faster discharging speed. It is worth noting that the change in the read performance induced by the barrier thickness is stronger than by the area, because the FTJ resistance is inversely linear proportional to the area but approximately exponentially dependent on the barrier thickness (see Eq. (3.7)).

4.1.3.2 Dependence on the access transistor size

Since the FTJ can be fabricated above the CMOS circuits by the BEOL, the cell area of an FTRAM is mainly determined by the area of the access TG. Therefore it is necessary to study the relationship between the access transistor size and the read performance.

Figure 4.5 shows the read performance versus the W/L of NMOS transistor in the access TG. During the simulation, the access TG for the reference FTJ always used the same size as the memory one. As we can see from the results, both the read delay and read energy increase as the transistor is enlarged. The increasing channel width has two-sided influences on the transistors: on the one hand, it reduces the transistor resistance and strengthens the discharging current (see Eq. (4.2)); on the other hand, it increases the parasitic capacitance [205] and results in a smaller discharging speed (see Eq. (4.3)). These two factors will lead to opposite change trends of the read performance. From the results of Figure 4.5, we argue that the increase in parasitic capacitance is a more dominant factor.

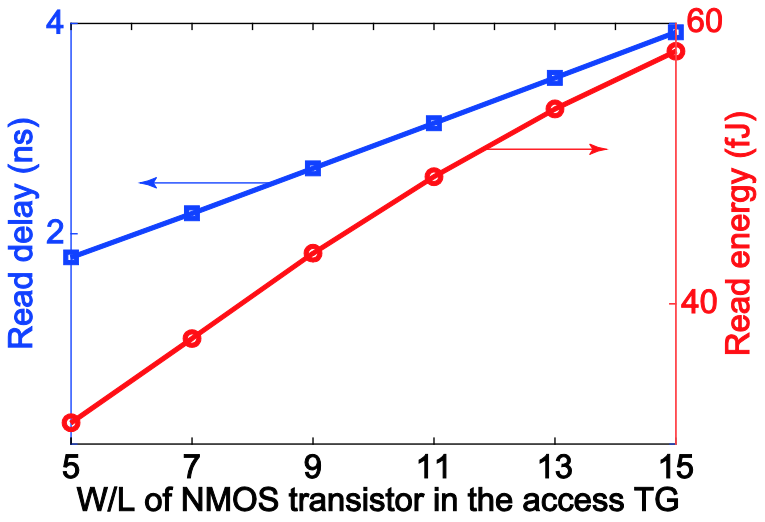


Figure 4.5 FTRAM read performance versus the size of access transistors.

4.1.3.3 Reliability analysis

For the PCSA, reliable readout requires a large enough ratio of discharging currents between two branches, which is estimated from Eq. (4.2), as

$$\frac{I_{mem}}{I_{ref}} \simeq \frac{R_{MOS} + R_{FTJ\_ref}}{R_{MOS} + R_{FTJ\_mem}} \tag{4.4}$$

In addition, the difference of the time constants (τ_{mem} and τ_{ref}) between two discharging currents also has an impact on the read operation, as

$$\tau_{mem} - \tau_{ref} \simeq \left(R_{FTJ\_mem} - R_{FTJ\_ref}\right) C_{MOS} \tag{4.5}$$

The real nanofabrication process inevitably leads to the stochastic device size variation and mismatch, which causes the uncertain resistance variation of each branch in the PCSA. After considering these non-ideal conditions, Eqs. (4.4) and (4.5) are written as

$$\frac{I_{mem}}{I_{ref}} \simeq \frac{R_{MOS} + R_{FTJ\_ref} + \Delta R_1}{R_{MOS} + R_{FTJ\_mem} + \Delta R_2} \tag{4.6}$$

$$\begin{aligned} \tau_{mem} - \tau_{ref} \simeq & \left(R_{FTJ\_mem} - R_{FTJ\_ref} + \Delta R_1 - \Delta R_2\right) C_{MOS} + \\ & \left(R_{FTJ\_mem} + \Delta R_1\right) \Delta C_1 - \left(R_{FTJ\_ref} + \Delta R_2\right) \Delta C_2 \end{aligned} \tag{4.7}$$

where ΔR_1 and ΔR_2 are the resistance change induced by process variation and mismatch at two branches, respectively. ΔC_1 and ΔC_2 the change in the transistor parasitic capacitance.

It is inferred from Eqs. (4.6) and (4.7) that the process variation and mismatch may alter the balance of two discharging currents and discharging speed due to the added ΔR and ΔC. As a result, stochastic read errors can occur and cause a read reliability issue.

For evaluating the read reliability of the PCSA, we performed *Monte-Carlo* statistical simulation to count the read error rate (RER). For the transistor part, the process variation and mismatch have been set by *STMicroelectronics* library. For the FTJ part, we set its radius to be Gaussian-distributed with $3\sigma = 10\%$ (σ is the standard deviation). But barrier thickness variation was not taken into account since it involves complicated modifications of the scaling factor F_1 in Eq. (3.9). In reality, the barrier thickness can be well controlled by molecular beam epitaxy (MBE).

With the above settings, a group of *Monte-Carlo* simulation results of reading '1' is shown in Figure 4.6, where the mean value of the FTJ size was set to 1.2 nm in barrier thickness and 175 nm in radius. As we can see from the results, one read error indeed occurs among 10 runs. In order to analyze the relationship between device parameters and the RER, we have carried out 2500 or 5000 simulation runs at each group of device parameters. Figure 4.7 shows a typical histogram of the FTJ resistance (use the same device size as Figure 4.6) during 2500 simulation runs, which confirms the approximate Gaussian distribution of the resistance. The statistical results about the RER are listed in Tables 4.2–4.3.

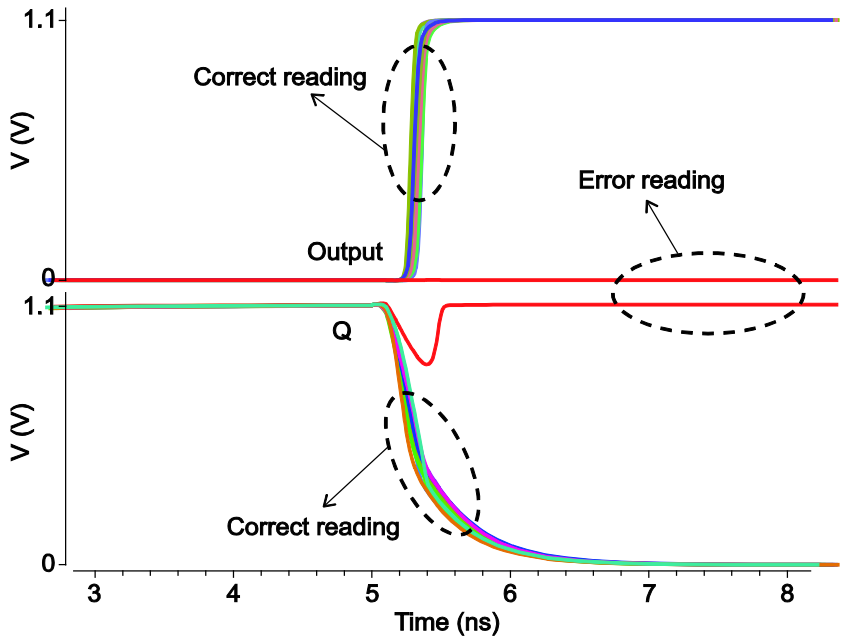


Figure 4.6 Monte-Carlo simulation results of reading '1'. One error occurs among 10 runs.

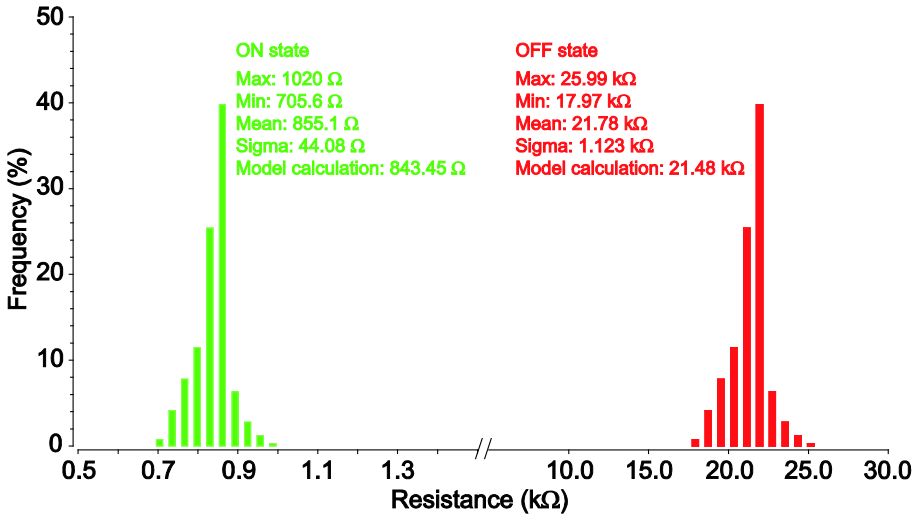


Figure 4.7 Histogram of the FTJ resistance during 2500 *Monte-Carlo* simulation runs.

Table 4.2 RER at various FTJ size

Barrier thickness \ Radius	125 nm	150 nm	175 nm	200 nm
1.2 nm	34/2500	75/2500	127/2500	221/2500
1.6 nm	0/5000	0/5000	0/5000	0/5000
2.0 nm	0/5000	0/5000	0/5000	0/5000
2.4 nm	0/5000	0/5000	0/5000	0/5000

Table 4.3 RER at various W/L of the access NMOS transistor

FTJ size* \ W/L	5	9	13
1.2 nm/200 nm	221/2500	330/2500	372/2500
1.2 nm/175 nm	127/2500	219/2500	273/2500

* Barrier thickness and radius

As can be seen from Table 4.2, read error can be avoided if the barrier is thicker than 1.6 nm. This result is to be expected since the TER ratio for 1.6 nm-thick barrier has been up to ~80 according to Eq. (3.10), which provides the large ratio of discharging currents between two branches (see Eq. (4.6)) and ensures the correct readout. Since the TER ratio of the FTJ is much higher than TMR ratio of the MTJ (usually < 10), the FTJ outperforms the MTJ at read reliability.

On the other hand, the RER can be optimized by decreasing the FTJ area, since the FTJ resistance increases so that the disturbance from ΔR and ΔC is weakened in Eqs. (4.6) and (4.7). The results about 1.2 nm-thick barrier in Table 4.2 validates this conclusion.

Table 4.3 indicates that the RER increases with the size of the access transistor. Theoretically, smaller access transistor leads to a lower R_{MOS} and a larger I_{mem}/I_{ref} (see Eq. (4.6)), hence the RER is expected to be smaller, which is against Table 4.3. We argue that the change in the transistor parasitic capacitance may play a more dominant role. The read error possibly is caused by the difference of discharging speed between two branches rather than of discharging current.

4.1.4 Write performance

Like in Section 4.1.3, the write delay and write energy were also evaluated. We define the write delay as the time difference between the rising edge of 'EN_W' and the time when the switched domains of both the memory and the reference FTJs arrive at 99.99%, which agrees with our assumption in Section 3.2.3 that nucleation process is required when the switched domain is smaller than 10^{-4}. Accordingly, the write energy is calculated by

$$E_w = Vddw \times \int_{t_{w1}}^{t_{w2}} i_w(t)dt \tag{4.8}$$

where $t_{w2} - t_{w1}$ is the write delay defined above, $i_w(t)$ is the total current flowing through the power supply.

While varying device parameters, the ratio of W/L between PMOS and NMOS transistors in the access TG may need to be adjusted to recover a good symmetry between two write directions. But in our following analysis, we kept using the ratio of 1.3. In this way, we can confirm that the change in write performance is caused by the concerned parameters instead of the change in the W/L. The larger delay between two write directions is considered to be the write delay.

4.1.4.1 Dependence on the FTJ size

Figure 4.8 shows the simulation results of the write speed and write energy while varying the FTJ size. Clearly, as the FTJ area decreases, both the write delay and write energy are improved. This trend is consistent with the prediction of the models, as discussed below.

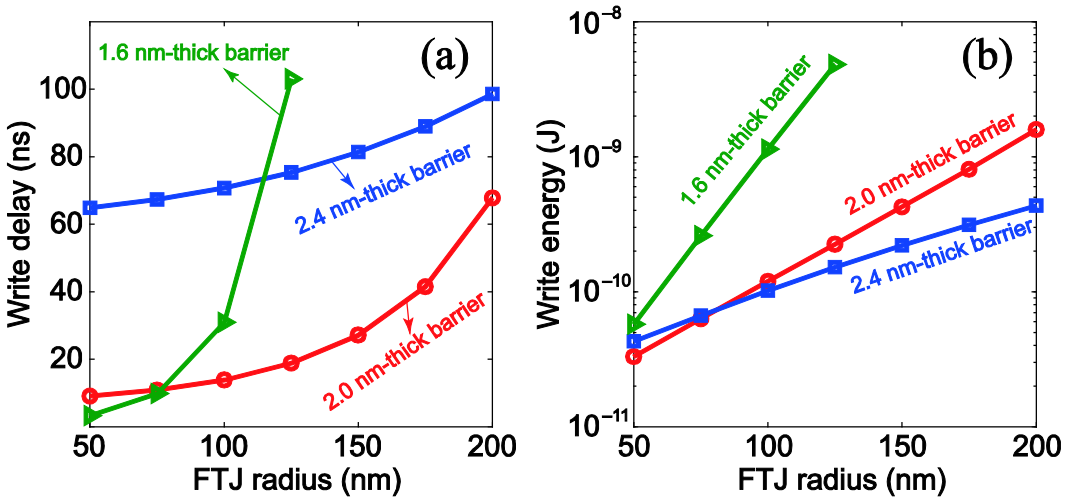


Figure 4.8 FTRAM write delay (a) and write energy (b) versus the FTJ size.

The effective write voltage across the FTJ can be estimated by

$$V_{w\_eff} = \frac{V_{ddw} \times R_{FTJ}}{R_{drive} + R_{access} + R_{FTJ}} \simeq \frac{V_{ddw} \times R_{FTJ}}{R_{access} + R_{FTJ}} \tag{4.9}$$

where R_{drive}, R_{access}, and R_{FTJ} are the resistances of the drive transistors, the access TG's transistors and the FTJ, respectively. Since the W/L of the drive transistors is much larger than that of the access TG, R_{drive} is small enough to be neglected. In addition, in either write directions, one of the transistors in the access TG operates in the linear region while the other in the saturation region, thereby the resistance of the access TG is mainly determined by the former transistor, which can be roughly regarded as a resistor, as [205]

$$R_{access} \simeq \frac{1}{\mu_{n,p} C_{ox} (W/L)\left(V_{gs,sg} - V_{th}\right)} \tag{4.10}$$

where $\mu_{n,p}$ is the electron (or hole) mobility, C_{ox} is the gate oxide capacitance per unit area, W and L is the channel width and length, respectively, V_{gs} is the gate-source voltage, and V_{th} is the threshold voltage.

Based on Eq. (4.9), the higher FTJ resistance can provide the larger effective write voltage. Since the shrink of the FTJ area leads to the increase in the FTJ resistance (R_{FTJ}), accordingly the effective write voltage is raised. Merz's law (see Eq. (3.18)) indicates that the switching delay falls as the write voltage rises. The total effect is that the write delay decreases with the shrinking FTJ area, consistent with the trend of Figure 4.8(a). In Figure 4.8(b), the decrease in the write energy is due to the double reduction of the write delay and write current caused by the decreasing FTJ area.

However, the influence of barrier thickness is more complicated. The increase in barrier thickness produces a larger FTJ resistance (see Eq. (3.9)), then the effective write voltage increases (see Eq. (4.9)). In this case, the change trend of write delay cannot be deterministically predicted by Merz's law, since both the write voltage and the barrier thickness increases (see Eq. (3.18)). This dilemma is also shown in Figure 4.8 (a), where the intersections of three curves can be seen. This demonstrates that the write delay is more sensitive to the change in the FTJ area if the barrier is thinner. In other words, the write delay is positively correlated with the barrier thickness if the FTJ area is small, but negatively if large.

Similarly, the dependence of the write energy on the barrier thickness is also not monotonous, as Figure 4.8 (b). The dependence is opposite for the cases of small and large FTJ area.

4.1.4.2 Dependence on the access transistor size

Also we studied the write performance as a function of the access transistor size. As is indicated in Figure 4.9, both the write speed and write energy can be optimized at the expense of the transistor size overhead. This can be explained by Eqs. (4.9) and (4.10). A larger transistor size leads to a smaller resistance (R_{access}), which strengthens the effective write voltage of the FTJ (V_{w_eff}) and speeds up the write operation (Merz's law, see Eq. (3.18)). However, the change in the write energy cannot be simply predicted, since the write current increases as the access transistors are widened. Figure 4.9 reveals a decline trend of the write energy with the transistor size. We explain it as follows. While the transistor size varies, the change in the write delay is exponential according to Merz's law (see Eq. (3.18)) but it is linear for the write current (see Eq. (4.10)). Therefore, as the transistor size increases, the decrease of the write delay is a more dominant factor compared with the increase in the write current, resulting in the decrease of the write energy.

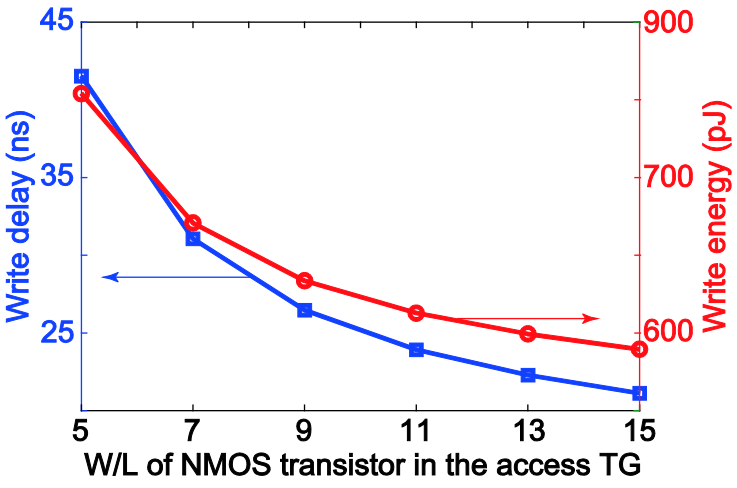


Figure 4.9 FTRAM write performance versus the size of the access transistors.

It is worth noting that in Figure 4.9 the improvement of write performance is more and more insignificant with the access transistors widened. This agrees with the Eqs. (4.9) and (4.10). As the resistance of the access transistors keeps decreasing with the size, the relative change in the effective write voltage of the FTJ becomes tiny due to the reduced R_{access}/R_{FTJ}. As a result, for a wider access transistor, its ability to adjust the write performance is weaker.

4.1.4.3 Dependence on the creep energy barrier

Aforementioned simulation results show that the write performance of the proposed FTRAM is not very competitive (write delay: > 10 ns, and write energy: tens or hundreds of pJ). This is partly due to the non-optimized circuit design, for example, the write operation requires to switch a couple of FTJs and thus consumes more energy, partly due to the relative high creep energy barrier. We expect that the write performance can be improved by reducing the creep energy barrier. This idea is validated by the simulation results shown in Figure 4.10, where we varied the creep energy barriers for the domain nucleation (U_n) and domain wall propagation (U_p) while keeping U_n/U_p constant. Significant performance improvement can be seen from the results. In addition, the decrease in the creep energy barrier allows a lower write voltage. Through a simulation example with the default values, we found that, to keep the same write delay, the write voltage can be reduced from 4 V/4.2 V to 3.5 V/3.7 V if U_p and U_n are decreased to 0.46 eV and 0.59 eV. This is an efficient solution to enhance the compatibility of the FTJ with nanoscale CMOS technology.

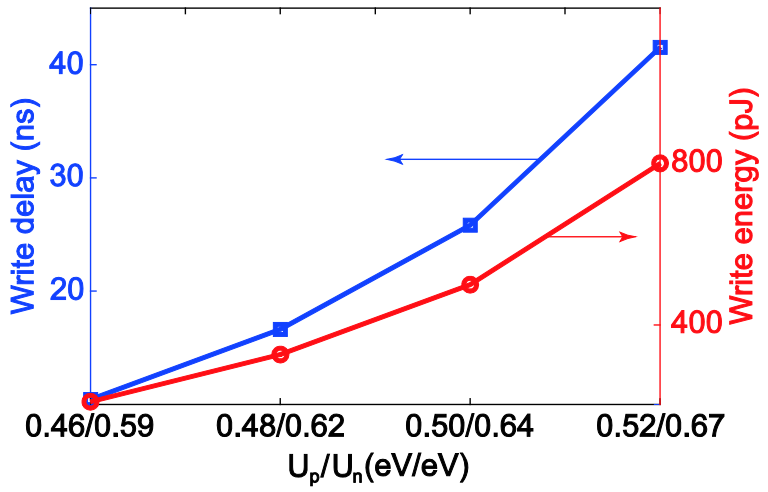


Figure 4.10 FTRAM write performance versus the creep energy barrier.

However, a small creep energy barrier is detrimental to the data retention time, which is defined as an upper limit of the time when the ferroelectric polarization decays too low to be successfully detected. Depending on the various polarization failure mechanisms, the retention

time (t_{re}) is described by Arrhenius reaction model or logarithmic polarization decay model [207]–[209], as

$$\log\left(t_{re}\right) = \frac{\Delta E}{k_B T} + constant \tag{4.11}$$

$$\log\left[\log\left(\frac{t_{re}}{t_0}\right)\right] = \frac{\Delta E}{k_B T} + constant \tag{4.12}$$

where t_0 is the characteristic time, T is the temperature, ΔE is the activation energy responsible for the polarization failure. It is considered that ΔE is proportional to the creep energy barrier. Hence the data retention time drops with the creep energy barrier decreasing.

4.1.5 Summary

The influences of both the FTJ and access transistors on the performance of the proposed FTRAM are summarized in Table 4.4, which shows how to adjust the parameters to meet high-performance FTRAM. Note that the retention time is only discussed in terms of creep energy barrier in Section 4.1.4.3, but actually it is also related to the ferroelectric material size. As mentioned in Section 2.1.2.1, it is more difficult to keep a stable ferroelectric polarization in a smaller ferroelectric material. Therefore, a large enough size for the FTJ is crucial to keep satisfying retention time.

As we can see from the table, there are too many tradeoffs between various performance metrics. The device parameters need to be optimized according to the specific application.

Table 4.4 Parameter requirements for the high-performance FTRAM

Performance requirement	FTJ area	FTJ barrier	Access transistor size	Creep energy barrier
High read speed	Larger	Thinner	Smaller	–
Low read energy	Larger	Thinner	Smaller	–
High read reliability	Smaller	Thicker	Larger	–
High write speed	Smaller	Non-monotonous	Larger	Smaller
Low write energy	Smaller	Non-monotonous	Larger	Smaller
Long retention time	Larger	Thicker	–	Larger
Small cell area	–	–	Smaller	–

4.2 FTJ-based neuromorphic systems

Another application field of the FTJ is the neuromorphic electronic system (abbreviated as neuromorphic system) [210]. In this section, we firstly introduce briefly the structure and function of neuromorphic systems. Then we design two FTJ-based neuromorphic systems to simulate two typical learning rules. The one aims to implement spike-timing dependent plasticity (STDP) [211] and the other is used for the on-chip supervised learning.

4.2.1 Preliminary knowledge on the neuromorphic systems

The typical architecture of a neuromorphic system is analogous to that of a biological neural network, which is constructed with massive interconnected neurons and synapses, as shown in Figure 4.11. In neuroscience, a neuron is an electrically excitable cell consisting of one soma, multiple dendrites, and one axon. The dendrites and the axon are responsible for receiving and carrying the excited electrical signals, respectively. Once the sum of the received signals surpasses a threshold, the neuron generates an all-or-none electrochemical pulse called a spike. The spike is transmitted from one neuron (pre-neuron) to the next (post-neuron) via the synapse, which is defined as the region between the axon-terminal of the pre-neuron and the dendrite of the post-neuron (see Figure 4.11). Each synapse is characterized by a synaptic weight reflecting the connection strength between neighboring neurons. The ability of synaptic weight to change with the neuronal activity is so-called synaptic plasticity, which is widely believed to be the root of the memory and learning.

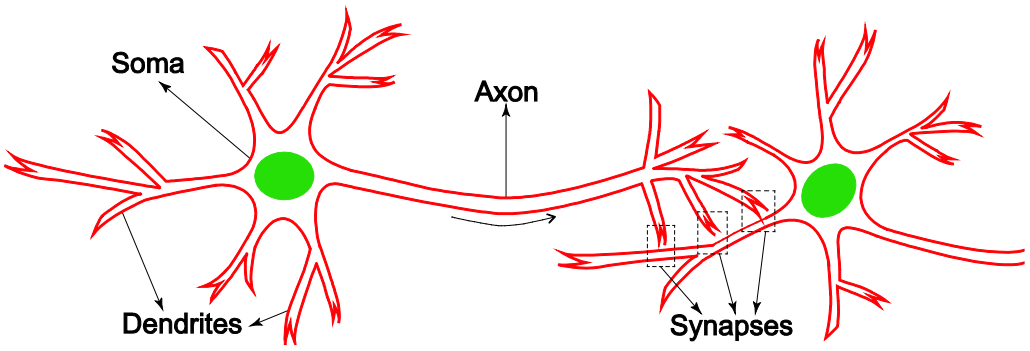


Figure 4.11 Biological neural network consisting of neurons and synapses.

In a neuromorphic system, neurons and synapses are implemented with circuits or electron devices. Spikes are represented by the input or output electrical signals [210]. A typical mathematical model for the elementary unit of neuromorphic systems is shown in Figure 4.12. As we can see, the synapse weighs the input signal before delivering it to the neuron. The neuron

includes an integration function for collecting the weighted inputs and an activation function for limiting the range of the output signal. From the viewpoint of mathematics, the model can be described by

$$v_j = \begin{bmatrix} x_0 & x_1 & \cdots & x_n \end{bmatrix} \begin{bmatrix} w_{0j} \\ w_{1j} \\ \vdots \\ w_{nj} \end{bmatrix} = \boldsymbol{x}\boldsymbol{w}^T \tag{4.13}$$

$$y_j = f\left(v_j\right) \tag{4.14}$$

where subscript j is the index of the neuron. $\boldsymbol{x}$ is the input, $\boldsymbol{w}$ is the synaptic weight, y is the output, $f(\cdot)$ is the activation function.

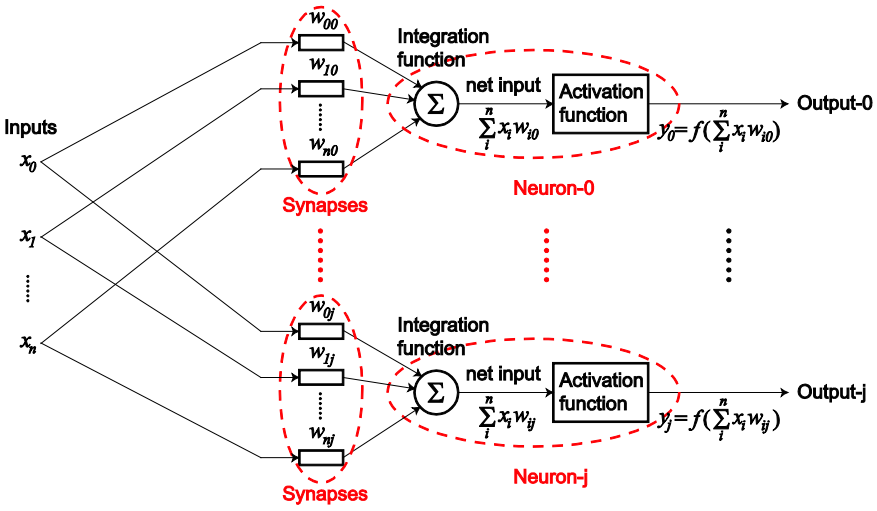


Figure 4.12 Schematic model of a neuromorphic system.

The performance of a neuromorphic system can be flexibly tuned by adjusting the synaptic weights. Therefore, it is feasible for a neuromorphic system to optimize the synaptic weight according to environmental inputs and outputs. This process is called learning, which is the most attractive advantage of the neuromorphic system. There are various learning rules used in neuromorphic system for solving specific problems. Commonly they are divided into two groups: first, the unsupervised learning operates without an external teacher. It aims to find the hidden regularities of the input data. Second, the supervised learning is performed under the supervision of an external teacher (i.e. the targeted response to be learnt). It adjusts the synaptic weights iteratively to minimize the error between the targeted and actual responses [212].

Since the FTJ has an adjustable resistance, it can serve as a synapse in neuromorphic systems. Assume that the input is a voltage and that the output is a current, the FTJ conductance can be considered as the synaptic weight.

4.2.2 Spike-timing dependent plasticity (STDP) implemented by the FTJ-based synapse array

4.2.2.1 General introduction of STDP

STDP, an unsupervised learning rule that adjusts the synaptic weight according to the relative timing of spikes between pre- and post-neurons, has been observed in massive biological experiments [211]. Specifically, considering a synapse connecting a pre-neuron to a post-neuron, assume that the output spike of the pre-neuron arrives at the post-neuron at time t_1, and that the output spike of the post-neuron occurs at time t_2. If t_1 is before t_2, the synaptic weight is increased, otherwise the synaptic weight is decreased. The persistent increase and decrease of the synaptic weight induced by repetitive spikes are called long-term potentiation (LTP) and long-term depression (LTD), respectively. The percentage synaptic change is strongly dependent on the timing difference $t_1 - t_2$ (called spike timing). The STDP results experimentally measured in real biological synapses [211] are shown in Figure 4.13. Although the data is noisy, they can be approximated by two decaying exponential functions [213], as

$$\xi(\Delta T) = \begin{cases} A_+ \exp\left(-\dfrac{\Delta T}{\tau_+}\right), & \Delta T > 0 \\ -A_- \exp\left(\dfrac{\Delta T}{\tau_-}\right), & \Delta T < 0 \end{cases} \tag{4.15}$$

where ΔT is the spike timing, $A_+ > 0$ and $A_- > 0$, τ_+ and τ_- are exponential time constants. Note that the two functions are generally asymmetric, i.e. $A_+ \neq A_-$ and $\tau_- \neq \tau_+$. It is seen that the synaptic change vanishes when the spike timing is larger than a critical value, which is defined as the critical time window.

STDP is a principal mechanism describing the learning and memory of mammalian brains. Its main advantage is the ability of self-organized learning since it does not require a supervisor. STDP has been used in several neuromorphic systems for achieving various learning tasks such as pattern recognition and image processing [214]–[215]. Below, we will simulate an STDP learning scheme with a hybrid FTJ/CMOS synapse array. The simulation results will be discussed with the theoretical models to evaluate the synaptic performance of the FTJ.

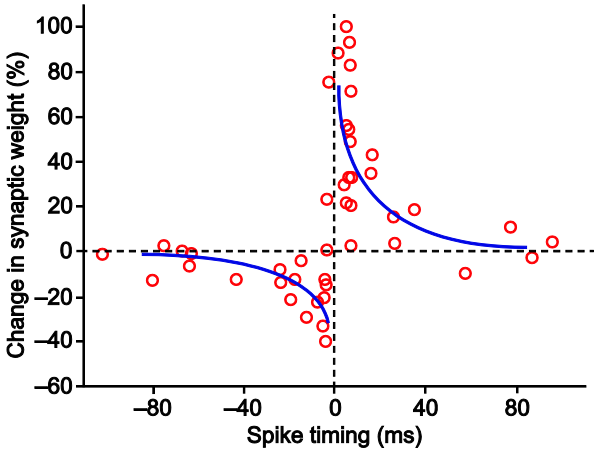


Figure 4.13 STDP experimental results from Ref. [211].

4.2.2.2 Architecture and operation

The synapse array was constructed with the cell structure proposed by Ref. [216]. As shown in Figure 4.14(a), a synapse is formed by connecting in series an FTJ to an NMOS transistor, which is a typical 1T1R cell. Three terminals are defined: the transistor gate, the top electrode of the FTJ ('TE') and the transistor source ('BE'). The pre-neuron is connected to the transistor gate and 'BE' while the post-neuron to 'TE' and 'BE'. The synaptic weight is measured as follows. The pre-neuron outputs a voltage to the transistor gate, simultaneously the post-neuron also generates a voltage across 'TE' and 'BE'. Both voltages have fixed amplitudes. In this case a current (called communication current, I_{COM}) flows from 'TE' to 'BE'. We define the synaptic weight as

$$w = I_{COM} / (V_{TE} - V_{BE}) \simeq \frac{1}{R_{FTJ} + R_{MOS}} \tag{4.16}$$

where $V_{TE} - V_{BE}$ is the voltage applied across 'TE' and 'BE'. R_{FTJ} and $R_{MOS}$are the resistance of the FTJ and transistor, respectively. Since $V_{TE} - V_{BE}$ is fixed, the modulation of the synaptic weight (called synaptic change) is represented by the change in the communication current (I_{COM}), which is induced by adjusting the FTJ resistance (R_{FTJ}).

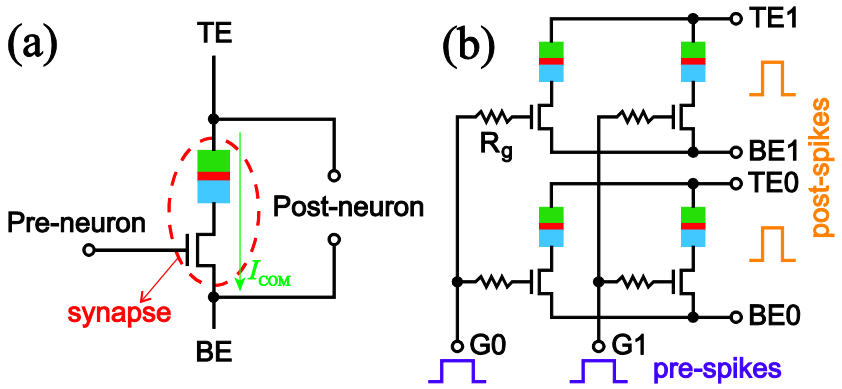


Figure 4.14 (a) Schematic 1T1R synapse between pre-neuron and post-neuron, (b) 2 × 2 crossbar-like synapse array.

Note that the FTJ acts as a synapse (more exactly speaking, the FTJ and transistor work together as the synapse) in the neuromorphic system but as a binary memory cell in the FTRAM. The role of synapse allows the FTJ to be programmed to the intermediate state between ON and OFF states, thus it is not mandatory to keep the symmetry between two write directions. This is the reason why here we use 1T1R structure rather than 2T1R TG as in Section 4.1. In addition, in the neuromorphic application the waveforms of pre-spike and post-spike can be flexibly designed to relieve the asymmetry between two programming directions.

Such a 1T1R synapse can be extended to a crossbar-like synapse array, as shown in Figure 4.14 (b). The transistor gates within the same column carry the identical pre-spike generated by a pre-neuron. Each gate is connected in series with a resistor (R_g) in order to mitigate the signal oscillation. 'TE' and 'BE' within the same row are shared by a post-neuron. This network topology relieves the sneak path issue suffered by the classical crossbar [145], because the column line is linked to the transistor gate leading to a high enough interconnection resistance.

Based on the above synapse array, we designed an STDP learning scheme by referring to the ideas of Refs. [216]–[218]. The operation is organized by time division multiplexing (TDM). The working mechanism and signal sequences are illustrated in Figure 4.15. The timeline is divided into the consecutive timeframes, each of which is composed of the successive three timeslots: the communication timeslot, the LTP timeslot and the LTD timeslot. The activities occurring in these three timeslots are described as follows.

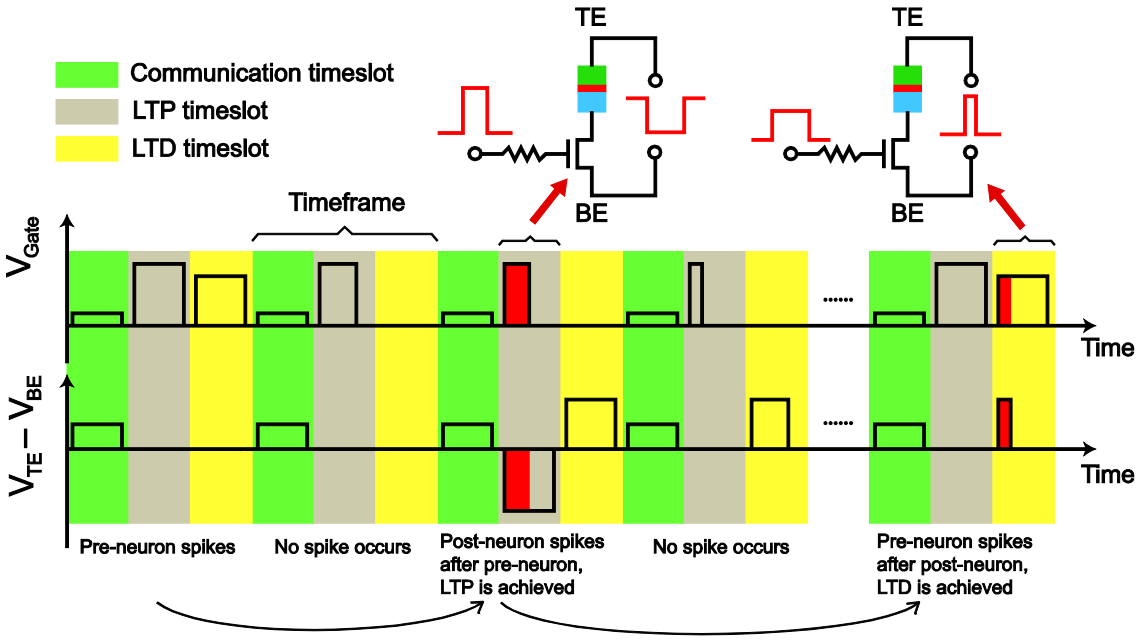


Figure 4.15 Diagram of the detailed time sequence describing the implementation of STDP learning rule in the proposed synapse array.

i) In the communication timeslot, the synaptic weight is measured by applying appropriate voltages to the transistor gate and the branch 'TE'~'BE'. The values of voltages must be set to small enough to avoid programming the FTJ and changing the synaptic weight.

ii) In the LTP timeslot, a positive pulse is generated at the transistor gate when the pre-neuron spikes. This pulse will not disappear during the following LTP timeslots until the critical time window arrives, but the pulse width decays with the time frame. When the post-neuron spikes, a negative pulse is triggered between 'TE' and 'BE'. This pulse lasts for only one timeslot and will not appear in the following timeslots. Note that the pulse amplitude in LTP timeslot should be large enough to program the FTJ and to trigger the LTP process.

iii) In the LTD timeslot, a positive pulse is produced at the transistor gate when the pre-neuron spikes. This pulse lasts for only one timeslot. When the post-neuron spikes, a positive pulse is launched between 'TE' and 'BE'. The pulse width decays with the timeframe and finally vanishes when the critical time window arrives. Similar to the LTP timeslot, the pulse in the LTD timeslot should also have large enough amplitude to enable the programming of the FTJ.

Aforementioned operations show that the spike of neurons can induce pulses in both the LTP and LTD timeslots. From the neurons' standpoint, the activities in the LTP and LTD timeslots are also described as follows.

i) When a pre-neuron spikes, it successively gives rise to two positive pulses at the transistor gate during the LTP and LTD timeslots, respectively. The former pulse decreases its width with the timeframe till the critical time window arrives. The latter one lasts for only one timeslot.

ii) When a post-neuron spikes, a negative pulse lasting for only one timeslot appears in the LTP timeslot. Then a positive pulse whose width decays with the timeframe occurs in the LTD timeslot.

The STDP learning rule can be implemented by performing the above operations. For instance, when a post-neuron spikes after a pre-neuron within the critical time window, in the LTP timeslot the transistor gate is activated by a decaying-width positive pulse from the pre-neuron, meanwhile a negative pulse from the post-neuron is applied to the branch 'TE'~'BE'. During the overlapping width of the two pulses (see the red region in Figure 4.15), a current flows from 'BE' to 'TE' and provides the FTJ with a negative programming voltage. Hence the FTJ resistance decreases, and the synaptic weight increases according to Eq. (4.16). Since the pulse width of the pre-spike decays with the timeframe, the pulse duration (i.e. overlapping width) for programming the FTJ decreases as the spike timing increases, accordingly the change in the synaptic weight also diminishes. This is consistent with the LTP process (see Figure 4.13). Similarly, LTD process can also be achieved.

In sum, our proposed STDP scheme translates the spike timing into the programming duration of the FTJ. In this way, the synaptic change (actually, the change in the FTJ resistance) is associated with the spike timing.

4.2.2.3 Simulation and validation

The proposed STDP scheme was simulated with the developed FTJ model and *STMicroelectronics* CMOS 40 nm design kit. The simulation was performed in a 2×2 synapse array shown in Figure 4.14. Some simulation parameters were configured as Table 4.5. The other parameters were set to the default values. The decaying-width pulse sequences can be produced by a pulse-width modulator. As can be seen in Table 4.5, the operation voltage of the synapse array is smaller than that of the FTRAM, because here the FTJ resistance is adjusted gradually rather than abruptly between ON and OFF states. The decrease in operation voltage is beneficial to the compatibility of the FTJ with CMOS technology.

Table 4.5 Parameters for the simulation of STDP learning rule

Parameters	Values
Timeslot	500 ns

W/L of the transistor	5
R_g	10 kΩ
Initial s_{OFF}	50%
Decaying pulse width	{500, 387, 295, 222, 165, 122, 89, 65, 47} ns
V_{Gate} in three timeslots	COM*: 1.5 V ; LTP: 3.8 V/0V ; LTD: 3.0V/0V
$V_{TE} - V_{BE}$ in three timeslots	COM: 0.3 V ; LTP: –3.6 V/0V ; LTD: 2.8 V/0V

* 'COM' means communication.

We found that the simulation speed was very slow because the total simulation time is nearly 10^5 times larger than the simulation time step (10 μs vs. 0.1 ns), which requires massive iterative calculation. In order to accelerate the simulation, we set a pseudo-threshold voltage of 0.1 V for the FTJ model to avoid unnecessary iterative calculation at the small voltage. The introduction of this pseudo-threshold voltage hardly decreased the accuracy of the model, because at 0.1 V the FTJ resistance is nearly invariable due to the very slow domain nucleation and domain wall propagation ($\tau_N \sim 10^{210}$s and $\tau_p \sim 10^{161}$s for a 2 nm-thick barrier).

Simulation results shown in Figure 4.16 validate the proposed STDP learning scheme. All the operation was performed within the critical time window. Here the subscript 'ij' represents the column and the row indexes. First, a pre-neuron spikes at 'G0' in the first timeframe (0~1.5 μs). Then two post-neurons spike at 'TE0'~'BE0' and 'TE1'~'BE1' in the third and the fourth timeframes (3.0~4.5 μs and 4.5~6.0 μs), respectively. As we can see from the results, 'FTJ_{00}' and 'FTJ_{01}' are successively programmed towards the ON state. As a result, their communication currents (I_{COM_00} and I_{COM_01}) increase, so do the synaptic weights (see Eq. (4.16)). Moreover, the synaptic change for the 'FTJ_{00}' is larger due to the smaller spike timing, in agreement with the LTP process. Similarly, 'FTJ_{10}' and 'FTJ_{11}' are programmed towards the OFF state when one pre-neuron spikes at 'G1' in the sixth timeframe (7.5~9.0 μs). The change trends of their communication currents (I_{COM_10} and I_{COM_11}) validate the occurrence of the LTD process.

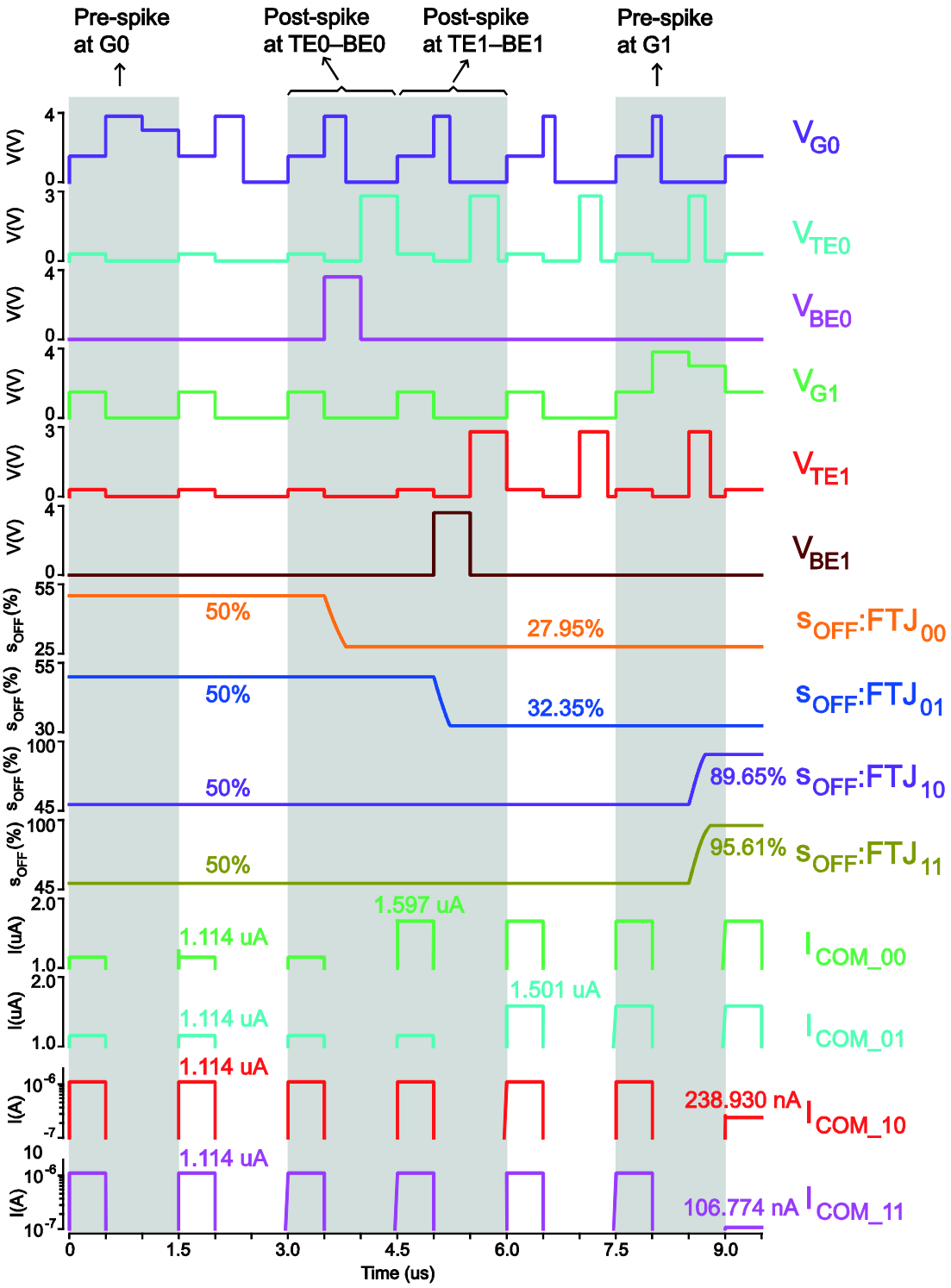


Figure 4.16 Transient simulation of STDP learning based on a 2 × 2 synapse array.

Finally, we measured the change in the synaptic weight as a function of the spike timing, as shown in Figure 4.17(a). Remarkably, the synaptic change decreases approximately exponentially

with the spike timing, which faithfully reproduces the characteristic of STDP learning rule. Figure 4.17(b) demonstrates that the change trend of the synaptic weight is associated with the pulse-width-controlled ferroelectric domain growth, which validates the dominant role of the FTJ resistance in the synaptic weight.

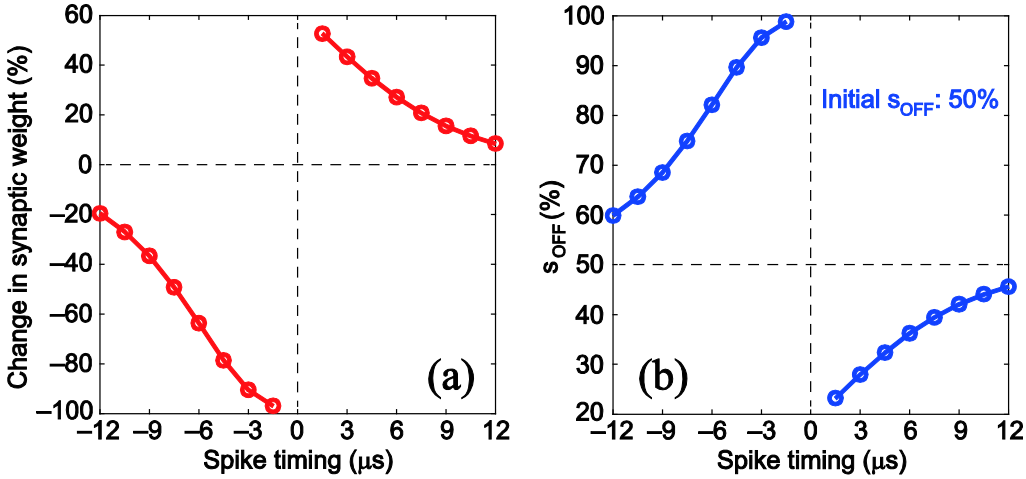


Figure 4.17 Change in the synaptic weight (a) and in s_{OFF} (b) versus the spike timing.

4.2.2.4 Performance analysis

In the proposed synapse array, the learning performance is influenced by a variety of parameters, such as the spike amplitude, the timeslot width, the device size, etc. Here we analyze the range of the synaptic change in terms of the domain configuration. Three learning curves for the initial s_{OFF} = 30%, 50% and 90% are shown in Figure 4.18. As can be seen from the results, the range of the synaptic change is narrower for the smaller initial s_{OFF}. This trend is explained with a model-based theoretical analysis as follows.

Eq. (4.16) shows the positive correlation between the synaptic weight and the FTJ resistance. The relative change rate of the FTJ resistance is given by

$$\frac{1}{R}\cdot\frac{\mathrm{d}R}{\mathrm{d}t}=\frac{1}{R}\cdot\frac{\mathrm{d}R}{\mathrm{d}s_{OFF}}\cdot\frac{\mathrm{d}s_{OFF}}{\mathrm{d}t} \tag{4.17}$$

where $(dR/ds_{OFF})/R$ is derived from Eq. (2.8), as

$$\frac{1}{R}\cdot\frac{\mathrm{d}R}{\mathrm{d}s_{OFF}}=\frac{R_{OFF}-R_{ON}}{R_{OFF}-\left(R_{OFF}-R_{ON}\right)s_{OFF}}=\frac{R_{OFF}/R_{ON}-1}{R_{OFF}/R_{ON}-\left(R_{OFF}/R_{ON}-1\right)s_{OFF}} \tag{4.18}$$

Considering $(R_{OFF}/R_{ON}) \gg 1 \Rightarrow (R_{OFF}/R_{ON}) - 1 \simeq (R_{OFF}/R_{ON})$, Eq. (4.18) is reduced to

$$\frac{1}{R}\cdot\frac{\mathrm{d}R}{\mathrm{d}s_{OFF}}\simeq\frac{1}{1-s_{OFF}} \tag{4.19}$$

This equation is accurate enough when s_{OFF} is not very close to 1. It partly explains why a larger initial s_{OFF} gives a larger range of synaptic weight. For example, when spike timing is negative (see the third quadrant of Figure 4.18(a) and the left-half plane of Figure 4.18(b)), the largest range of synaptic change is provided by the largest initial s_{OFF} (90%, blue curves), even if the corresponding change in s_{OFF} is smallest (< 10%).

Then, ds_{OFF}/dt is given by Eq. (3.23), hence Eq. (4.17) is expressed as

$$\frac{1}{R}\cdot\frac{dR}{dt}\simeq\frac{2}{\tau_P}\sqrt{\ln\left(\frac{1}{1-s_{OFF}}\right)} \tag{4.20}$$

Eq. (4.20) indicates that the relative change rate of the FTJ resistance increases with s_{OFF}. Moreover, this increase is stronger than expected because: the larger s_{OFF} leads to the larger FTJ resistance and thus the higher efficient programming voltage for the FTJ (see the analysis in Section 4.1.4.1 and Eq. (4.9)). Then, τ_P is smaller according to Merz's law, which makes an additional contribution to the increase in the relative change rate of the FTJ resistance. As a result, the range of the synaptic change is wider when s_{OFF} is larger, as shown in Figure 4.18.

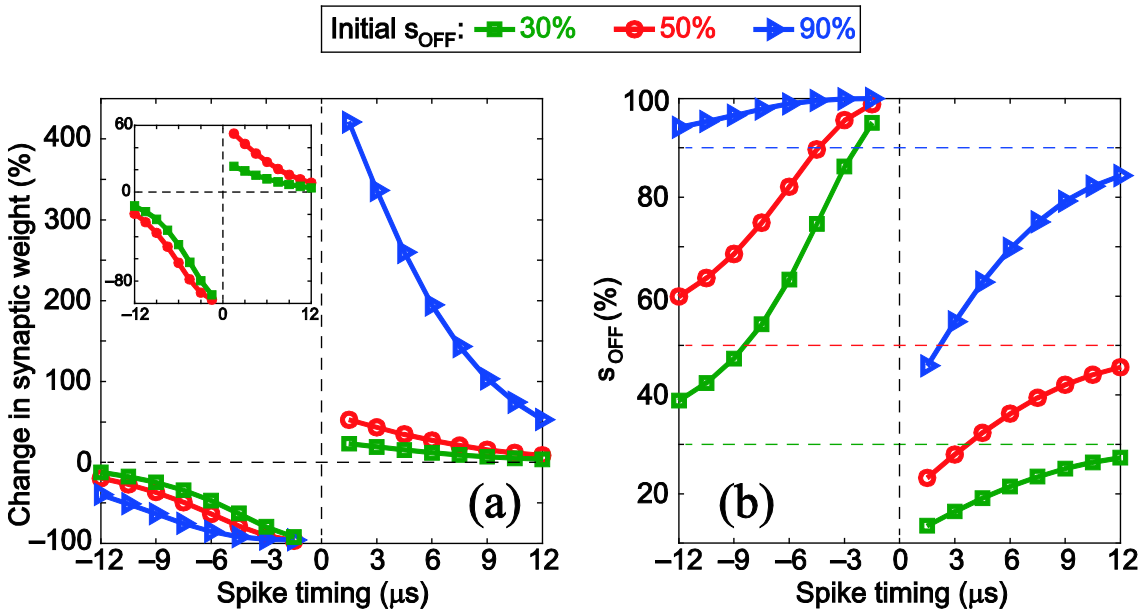


Figure 4.18 STDP learning results for various initial domain configurations. (a) Results about the change in the synaptic weight. The inset shows two curves for better visibility. (b) Results about the domain growth.

The range of the synaptic change is related to the learning speed. If this range is extended, the timeslot can be set to be smaller to achieve faster learning. Based on Eq. (4.20), decreasing τ_P is an efficient solution to extend the range of the synaptic change, which requires to strengthen the efficient programming voltage for the FTJ according to Merz's law. Following the conclusion in Table 4.4, we expect that this goal can be achieved by decreasing the FTJ area or increasing the transistor size. This prediction is validated by the simulation results shown in Figures 4.19 and 4.20, where the initial s_{OFF} is set to 50%, all the other parameters are set to default values.

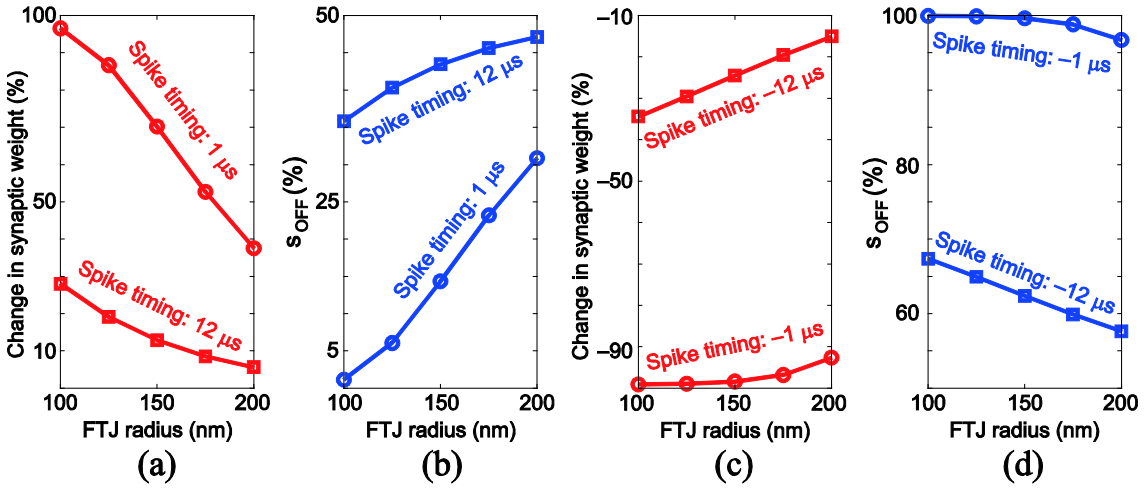


Figure 4.19 Ranges of the synaptic weight ((a), (c)) and the domain ((b), (d)) versus the FTJ radius. (a)–(b) correspond to LTP process and (c)–(d) to LTD process.

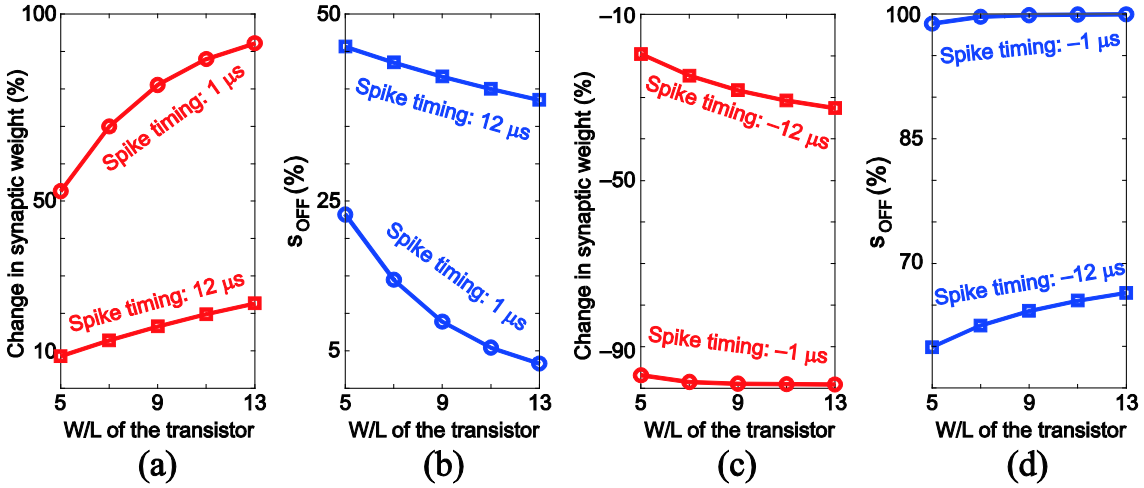


Figure 4.20 Ranges of the synaptic weight ((a), (c)) and the domain ((b), (d)) versus the transistor size. (a)–(b) correspond to LTP process and (c)–(d) to LTD process.

4.2.3 Supervised learning implemented with the FTJ-based crossbar

Besides unsupervised STDP learning, the FTJ promises to be used for implementing the supervised learning rule in neuromorphic systems. Thanks to the presence of the teacher, the supervised learning is intrinsically suitable for the learning of logic functions and compatible with traditional digital circuits. Here we propose an FTJ-based neural crossbar (NC) to implement the on-chip supervised learning.

4.2.3.1 Architecture and operation

Figure 4.21 illustrates the architecture of the proposed FTJ-based NC. The FTJ connects the row and column wires at each crossbar junction. A pair of differential inputs X_{i+}/X_{i-} are applied to the neighboring column wires through an input converter. The actual output O_j and the targeted output Y_j are generated at the row wire. i and j are the column and row indexes. A pair of extra bias inputs X_{0+}/X_{0-} is added to implement the threshold of the neuron. In this system, we use "active-high" logic, i.e. the logic '0' and '1' correspond to a low voltage 'L' and a high voltage 'H', respectively. Overall, the proposed NC consists of three modules as follows.

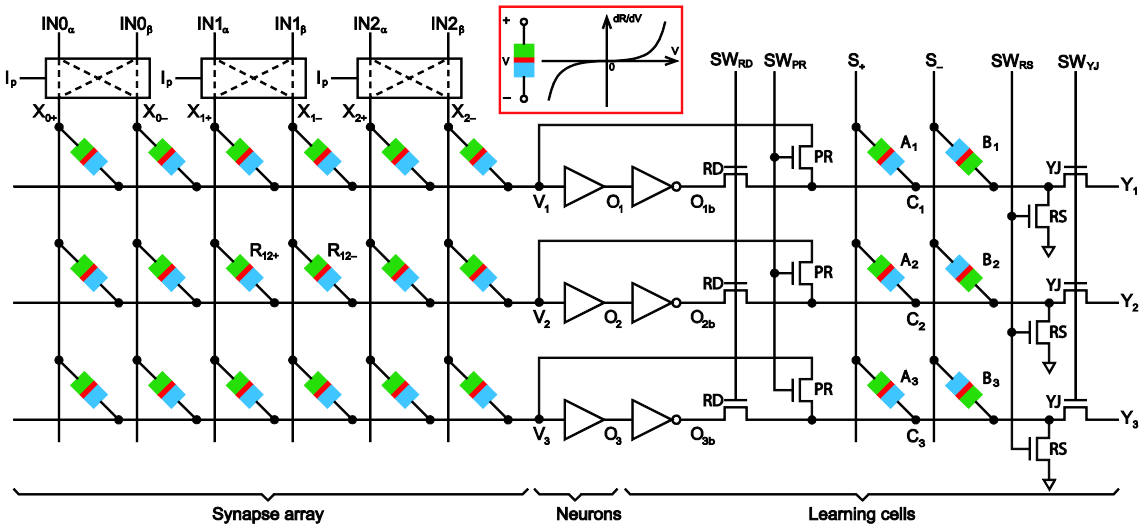


Figure 4.21 Architecture of the proposed FTJ-based neural crossbar. Inset shows the resistance variation of the FTJ in response to the applied voltage.

i) Synapse array. Each synapse is composed of a pair of neighboring FTJs within the same row. The synapse R_{ij+}/R_{ij-} weighs differential input signals X_{i+}/X_{i-} and produces the output (postsynaptic potential, V_j) at the row wire. The logical value of the input is determined by the relative polarities of X_{i+}/X_{i-} and the level of I_p, as shown in Table 4.6. During the read stage, I_p

is set to 'H'. Only during a specific step of learning stage, it is set to 'L' to reverse the X_{i+}/X_{i-}, which will be detailed later.

Table 4.6 Criteria of input logic

	$I_p = H$		$I_p = L$	
	X_{i+}	X_{i+}	X_{i+}	X_{i+}
Logic '0'	H	L	L	H
Logic '1'	L	H	H	L

Given a group of input signals X_{i+}/X_{i-}, the postsynaptic potential V_j can be tuned by adjusting the resistance configuration of the FTJs within the row j. Take an n-input NC for example, the V_j can be calculated by

$$V_j = \sum_{k=0}^{n} f_k(R)\left(X_{k+} - X_{k-}\right) \tag{4.21}$$

where $f_k(R)$ is the linear combination of the FTJ resistances within the row j. This equation indicates the close relationship between the synaptic weight and the adjustable FTJ resistance.

ii) Neuron, which is implemented with a CMOS buffer at each row. It receives the postsynaptic potential V_j and then generates the actual output O_j, which is a binary logical signal.

iii) Learning cell, which includes a couple of anti-parallel oriented FTJs, four switch transistors and an inverter at each row [219]. This design is more compact than the traditional CMOS learning cell (e.g. a large number of transistors are required in Ref. [220]). Thanks to such a compact design, the proposed NC promises to achieve high integration density and is suitable for constructing multi-layer network for the learning of complex functions.

It is worth noting that the FTJs play different roles in the synapse array and the learning cell. The FTJ used in the synapse array is called analog FTJ, which has a continuously-adjustable resistance. However, in the learning cell, the FTJ acts as a binary switch between the row and column wires, which is called binary FTJ. Its resistance is only set to ON or OFF state without staying any intermediate states. The reason will be explained later.

In the proposed NC, the targeted output Y_j acts as a teacher. The goal of the learning is to minimize the error $Y_j - O_j$ by adjusting the synaptic weights (i.e. the resistances of the analog FTJ). The on-chip adjusting algorithm operates as Table 4.7. In the cases (C0, C3, C4, C7), $\Delta R_{ij\pm} = 0$ means that the logic function has been successfully learnt, and thus the resistances of the analog FTJs are left unchanged. In other cases (C1, C2, C5, C6), the FTJ resistance needs to be adjusted

until the error $Y_j - O_j$ is nearly eliminated. During the learning process, four switch transistors are successively activated to connect C_j (the common terminal of two binary FTJs) to different signals. The detailed operations are illustrated in Figure 4.22, including three phases as follows.

Table 4.7 Resistance adjustment algorithm for the supervised learning

Case	Input $X_{i+}X_{i-}$	Targeted output Y_j	Actual output O_j	ΔR_{ij+}	ΔR_{ij-}	Programming signals
C0	LH	L	L	0	0	Null
C1	LH	L	H	−	+	S1
C2	LH	H	L	+	−	S2
C3	LH	H	H	0	0	Null
C4	HL	L	L	0	0	Null
C5	HL	L	H	+	−	S3
C6	HL	H	L	−	+	S4
C7	HL	H	H	0	0	Null

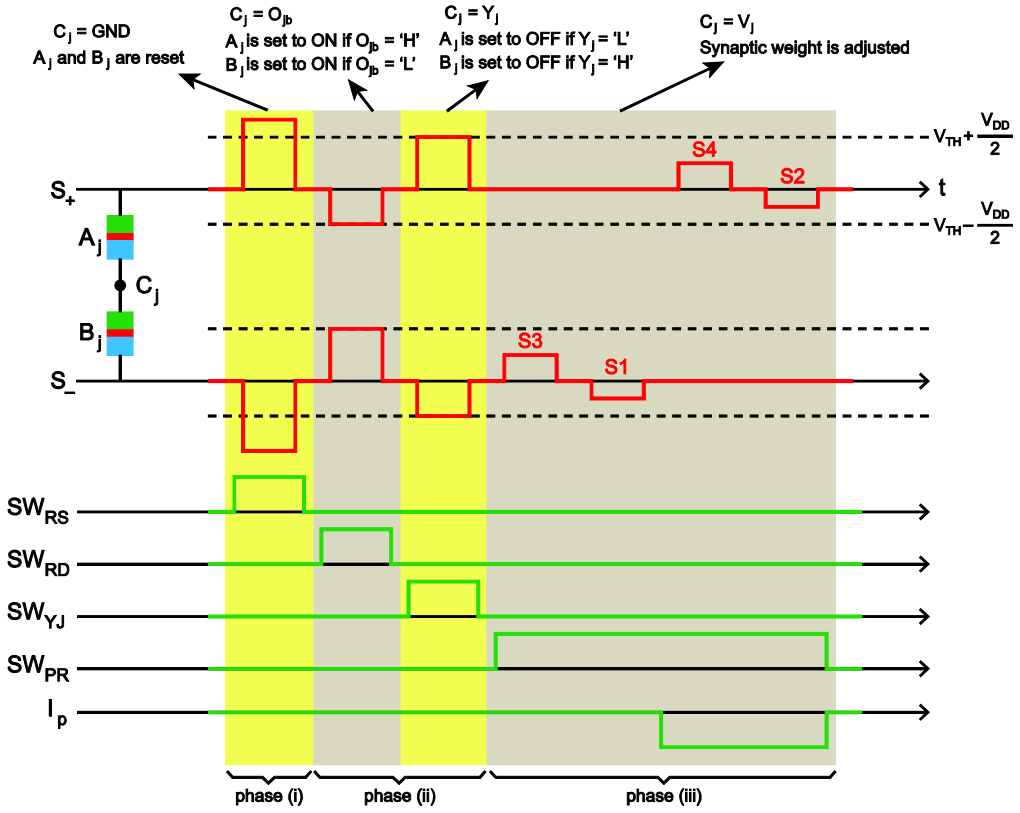


Figure 4.22 Signal sequence during one learning epoch.

i) Reset of the binary FTJs. Only the transistor 'RS' is activated to connect C_j to ground. Two binary FTJs are reset to OFF state (i.e. is opened) by applying two large enough pulses to S_+/S_-. The polarities of two pulses are opposite since the two binary FTJs are anti-parallel oriented.

ii) Configuration of the binary FTJs. The operation contains two steps:

During the first step, only the transistor 'RD' is activated to connect C_j to the inverse signal O_{jb} of the actual output. A positive and a negative pulses are applied to S_- and S_+, respectively. These two pulses switch one and only one of the binary FTJs to ON state. For that, we must define a threshold V_{TH} for the binary FTJ. Considering the range of O_{jb} is 0~V_{dd}, we set the amplitude of these two applied pulses to $(V_{dd}/2)+V_{TH}$ and $(V_{dd}/2)-V_{TH}$, respectively (V_{dd} is the power supply of the inverter). Then, if $O_j = H$, $O_{jb} \approx 0 < (V_{dd}/2)$, the voltage across the FTJ-B_j is larger than the threshold V_{TH} while it is contrary for the FTJ-A_j, thus the FTJ-B_j is set to ON state but the FTJ-A_j remains OFF state. Otherwise, only the FTJ-A_j is set to ON state.

Note that V_{TH} is actually a pseudo-threshold, as discussed in Section 3.1.5. Its value is related to the duration of applied pulse. There is inevitably an "ambiguous" range around V_{TH} in which the FTJ is possibly programmed to an intermediate state. Figure 4.23 shows an example of switching the FTJ from ON to OFF states, where the barrier thickness is 2.4 nm, and the applied pulse width is 100 ns. As we can see, 3.6~3.8 V is the "ambiguous" voltage. In order to prevent the voltage across the binary FTJ from staying in the "ambiguous" range, the inverter used in the learning cell is required to have a sharp transition region.

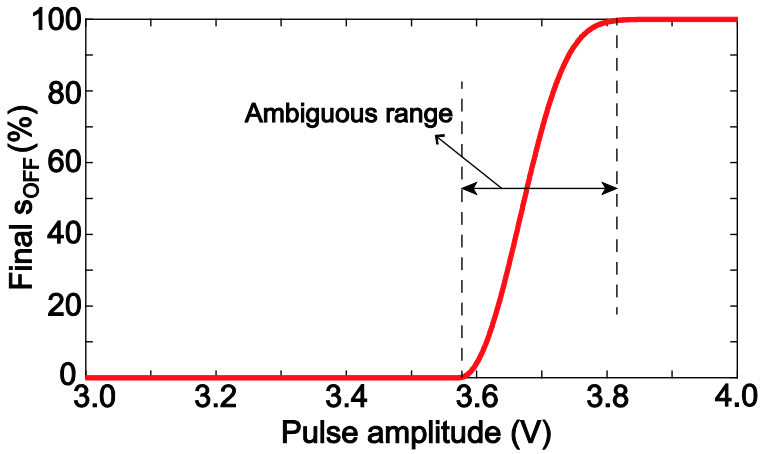


Figure 4.23 Final state of the FTJ versus the pulse amplitude, the pulse width is fixed to 100 ns.

During the second step, only the transistor 'YJ' is activated to connect C_j to the targeted output Y_j. Two pulses are applied to S_- and S_+, respectively. They are the same as those pulses

used in the first step except for the polarities. Similarly, depending on the potential of Y_j, one binary FTJ is set to OFF state while the other one remains unchanged.

In the above two steps, the states of two binary FTJs are shown in Table 4.8. As is indicated in this table, if the actual output is the same as the targeted one ($O_j = Y_j$), both FTJ-A_j and FTJ-B_j are set to OFF state in order to disconnect S_+ and S_- from the row wire. Otherwise, if $O_jY_j = LH$, S_+ is connected to the row wire through the ON-state FTJ-A_j. If $O_jY_j = HL$, S_- is connected to the row wire through the ON-state FTJ-B_j.

Table 4.8 States of the binary FTJs during the learning process

			After the first step		After the second step	
O_j	O_{jb}	Y_j	FTJ-A_j	FTJ-B_j	FTJ-A_j	FTJ-B_j
H	L	L	OFF	ON	OFF	ON
H	L	H	OFF	ON	OFF	OFF
L	H	L	ON	OFF	OFF	OFF
L	H	H	ON	OFF	ON	OFF

iii) Adjustment of the synaptic weights. Only the transistor 'PR' is activated to connect C_j to the postsynaptic output V_j. The operation is also performed at two steps. During the first step, programming signals 'S3' and 'S1' are successively applied to S_-. During the second step, I_p is inverted to exchange the X_{i+} and X_{i-}. 'S4' and 'S2' are successively applied to S_+. Then I_p returns to the original state. As a consequence, the resistances of the analog FTJs are adjusted as Table 4.7. For example, if $O_j = Y_j$, the programming signals 'S1'~'S4' have no impact on the synapse array since two OFF-state binary FTJs disconnect S_+ and S_- from the row wire. Otherwise, S_+ or S_- is connected to the row wire through the ON-state FTJ-A_j or FTJ-B_j. The resistances of the analog FTJs can be adjusted under the action of 'S1'~'S4'.

Note that the amplitude of programming signals 'S1'~'S4' need to be appropriately designed in order that they can program the analog FTJs but cannot change the states of the binary FTJs. This requires the binary FTJs to have a higher threshold than the analog FTJs. It can be achieved by using the thicker barrier in binary FTJs (Merz's law). But thicker barrier leads to a higher resistance (see Eq. (3.7)), which may make the ON-state binary FTJ unqualified for an ideal switch. This issue is resolved by enlarging the area of the binary FTJs.

4.2.3.2 Simulation and validation

With the proposed FTJ-based NC, we validated the supervised learning of logic functions 'AND' and 'OR' through the simulation. Thanks to the crossbar architecture, two logic functions can be learnt in parallel. The related parameters were configured as Table 4.9. The other parameters were set to the default values.

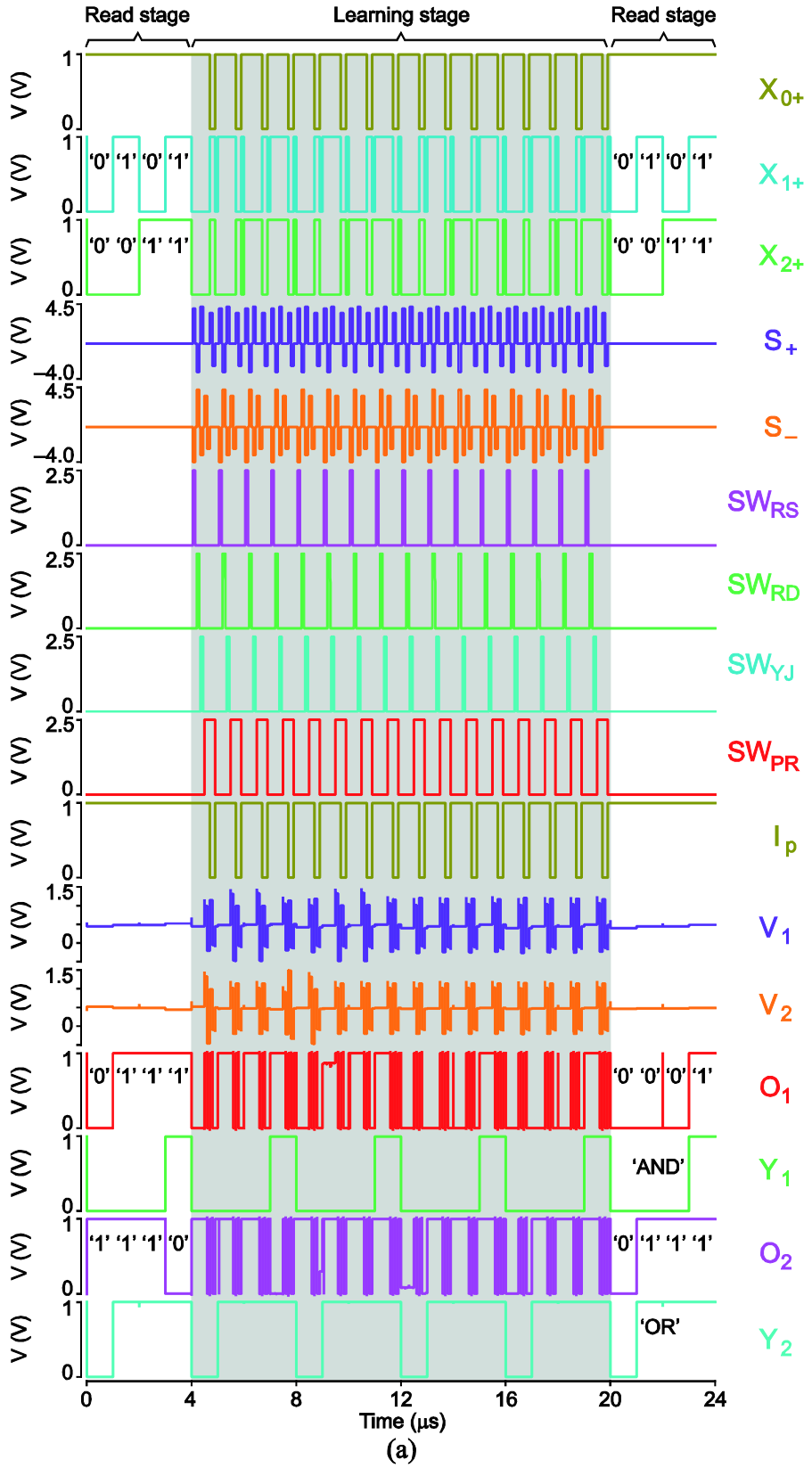
Table 4.9 Parameters for the simulation of supervised learning

Logic signal amplitude (X_{i+}/X_{i-} and Y_j)	H: 1 V, L: 0 V
Vdd for buffers and inverters	1 V
W/L of the switch transistors*	RS: 5, RD: 10, YJ: 5, PR: 10
Amplitudes of the pulses for activating the switch transistors	2.5 V
Amplitudes of the pulses applied to S_+	Reset: 4 V, S2: –2.5 V, S4: 3.5 V
Amplitudes of the pulses applied to S_-	Reset: –4 V, S1: –2.5 V, S3: 3.5 V
Size of the binary FTJs	Radius: 450 nm, barrier thickness: 2.4 nm
Size of the analog FTJs	Radius: 15 nm, barrier thickness: 1.2 nm
Threshold for the binary FTJ	3.7 V**
Learning epoch	1 μs
Duration of each learning pulse	100 ns
Initial s_{OFF} for the analog FTJs (ij are column/row indexes)	{01+, 01–, 02+, 02–}: 50% {11+, 21+, 12–, 22–}: 40% {11–, 21–, 12+, 22+}: 60%

* Use 'nsvt25' in *STMicroelectronics* CMOS045 library.

**Determined by Figure 4.23.

Simulation results in Figure 4.24 demonstrate the parallel learning process of a 2-input AND and a 2-input OR logic functions. All patterns of logic inputs ('00', '10', '01', '11') are repeatedly applied to $X_{1+}X_{2+}$ with a period of 4 μs. At first, during 0~4 μs, the neuron output is not agreement with the targeted 'AND' and 'OR' logic functions ($O_j \neq Y_j$). Then, during 4~20 μs, the learning process is performed for four epochs (1 epoch = 4 μs). It is seen that the signal sequences are organized as the aforementioned solutions. The resistance of the analog FTJs is adjusted until the error between O_j and Y_j is nearly eliminated (see Figure 4.24(b)). Finally, during 20~24 μs, the readout operation is performed to confirm the successful learning of the targeted logic functions.


Read stage
Learning stage
Read stage
V (V)
'0' '1' '0' '1'
'0' '0' '1' '1'
'AND'
'OR'
X0+
X1+
X2+
S+
S_
SWRS
SWRD
SWYJ
SWPR
Ip
V1
V2
O1
Y1
O2
Y2
0
4
8
12
16
20
24
Time (μs)

(a)

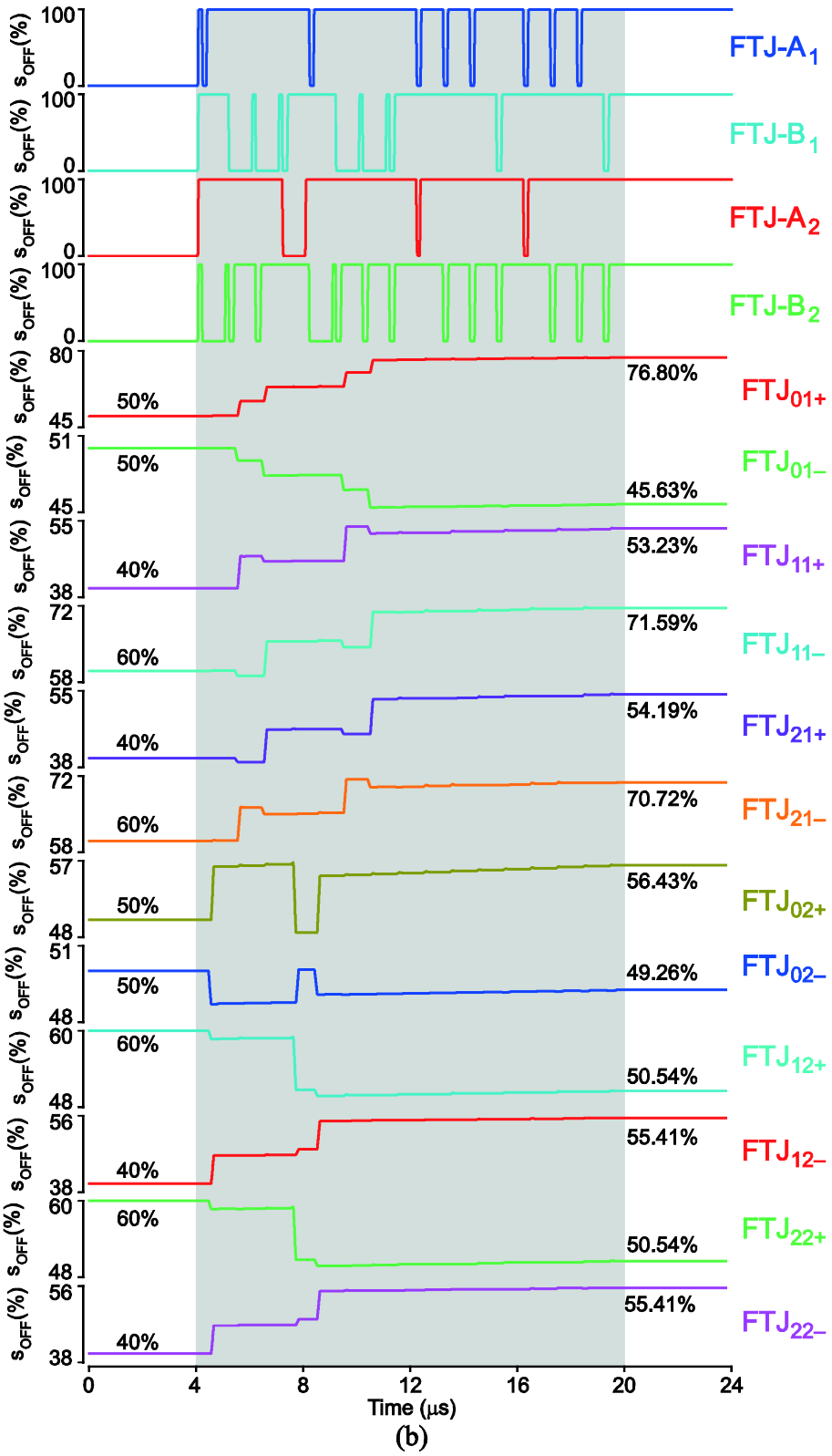


Figure 4.24 Transient simulation of the proposed FTJ-based NC. (a) Inputs, outputs and controlling signals, (b) Evolution of the ferroelectric domain in the binary FTJs (A and B) and analog FTJs (i.e. synapse array).

4.2.3.3 Fault-tolerance analysis

The learning based on neuromorphic system has inherent tolerance against the faults such as variation and defect, since the synaptic weights can be adjusted in response to the faults [212]. This is an attractive advantage over the conventional logic gates. We performed *Monte-Carlo* statistical simulation to evaluate the fault-tolerance of the proposed NC. Two types of faults were considered: the one is size variation including the radius variation of the FTJs and the process variation/mismatch of transistors, as mentioned in Section 4.1.3.3. The other is the stuck defect occurring in the analog FTJs, which means that the FTJ cannot work and has a constant resistance (Note that the NC will fail if the stuck defect occurs in the binary FTJs). The random radius was assumed to be Gaussian distributed, and the stuck defect was uniformly distributed. The statistical results of 'AND' logic learning with 100 simulation runs are summarized in Table 4.10.

Table 4.10 Learning success rate in the presence of faults

Learning epochs	3σ for the random FTJ radius*				Probability of the stuck defect			
	5%	10%	15%	20%	5%	10%	15%	20%
4	100/100	98/100	96/100	90/100	93/100	86/100	80/100	76/100
6	100/100	99/100	93/100	97/100	95/100	90/100	87/100	85/100

* σ is the standard deviation

As can be seen from the table, the learning success rate decreases as the fault is aggravated. The stuck defect can cause more damage to the learning process because it disables the adjustment of a synaptic weight. Generally, some unsuccessful learning can be avoided by increasing the number of learning epochs. However, an anomaly occurs when $3\sigma = 15\%$, which can be explained by the simulation example shown in Figure 4.25. There, initially the targeted output has been successfully learnt (0~4 μs, $O_1 = Y_1$) and therefore the synaptic weight should remain unchanged. However, FTJ-B_1 is not completely switched to the expected OFF state in the following learning epoch (see dash circle in Figure 4.25). As a result, the programming pulses cannot be isolated from $S\_$, leading to ongoing adjustment in the resistance of the analog FTJs (e.g. synaptic weights). Due to this undesired adjustment, original correct output O_1 gets wrong after 6 learning epochs. Nevertheless, successful learning can still be achieved if the number of learning epochs is between 1 and 5. The fault-tolerance advantage of the proposed NC is confirmed.

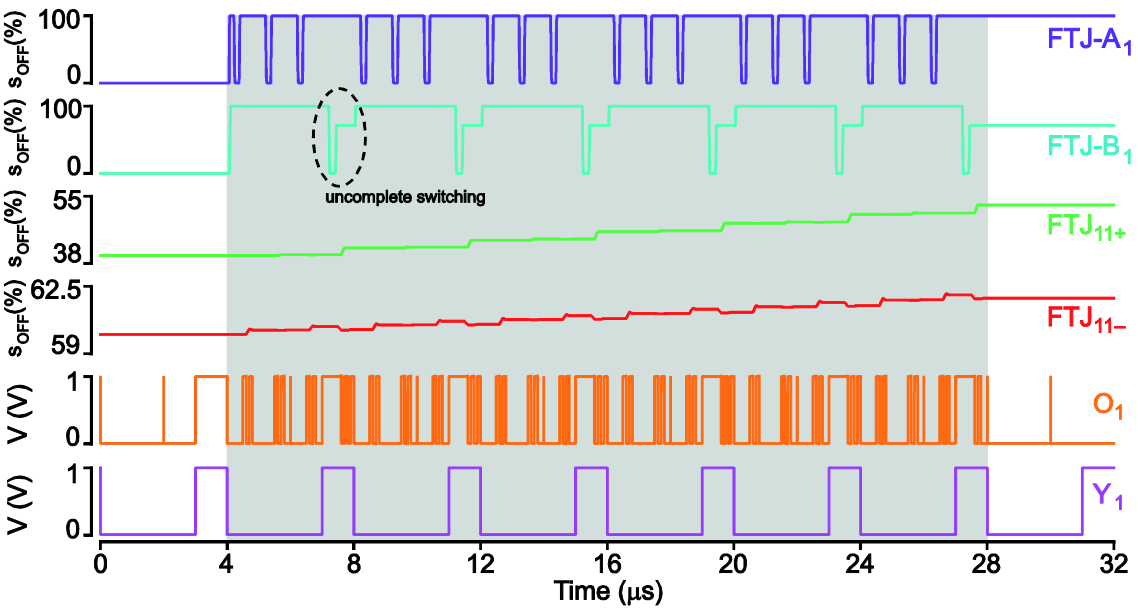


Figure 4.25 A simulation example showing the unsuccessful learning. Here only two analog FTJs are shown for simplicity.

4.3 An idea: logic is implemented inside a single FTJ

NV memory devices have been widely used for designing the NV Boolean logic blocks [221]–[225]. Several typical examples are shown in Figure 4.26. These designs are consistent with the idea of logic-in-memory architecture, where NV memory devices not only perform the logic computing but also store the computing results. In this section, we propose a compact Boolean logic block which consists of only an FTJ, a load resistor and a transistor. Logic operation can be implemented inside the single FTJ thanks to the nonlinear dependence of the FTJ resistance on the volume fraction of the OFF-state domain.

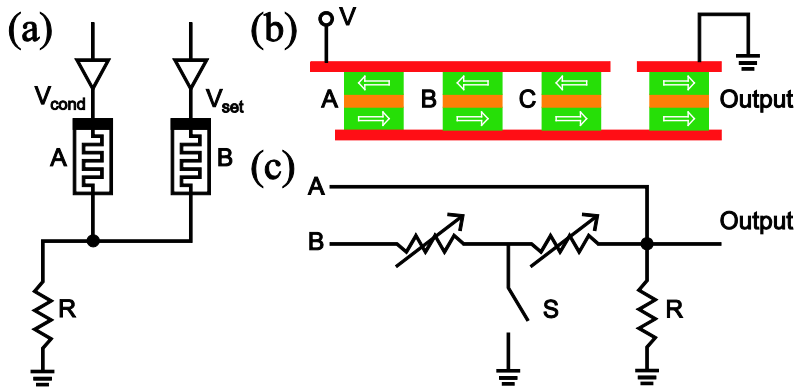


Figure 4.26 Logic blocks implemented with (a) memristors [221], (b) MTJs [222] and (c) phase change memories [223].

4.3.1 Working principle

Figure 4.27 shows the FTJ resistance as a function of the volume fraction of the OFF-state domain (s_{OFF}), which is calculated by Eq. (2.8). Here the parameters are set to default values. The resistance is readout at 0.1 V. As we can see, the resistance remains much smaller than R_{OFF} during a long-range initial OFF-state domain growth. This characteristic is similar to the short-circuit effect of the parallel resistors. To explain it, we rewrite Eq. (2.8) with the approximation of $(R_{OFF}/R_{ON}) - 1 \simeq (R_{OFF}/R_{ON})$, as

$$R \simeq \frac{R_{ON}}{1 - s_{OFF}} \tag{4.22}$$

Similar to Eq. (4.19), the above equation is of high accuracy if s_{OFF} is not very close to 1.

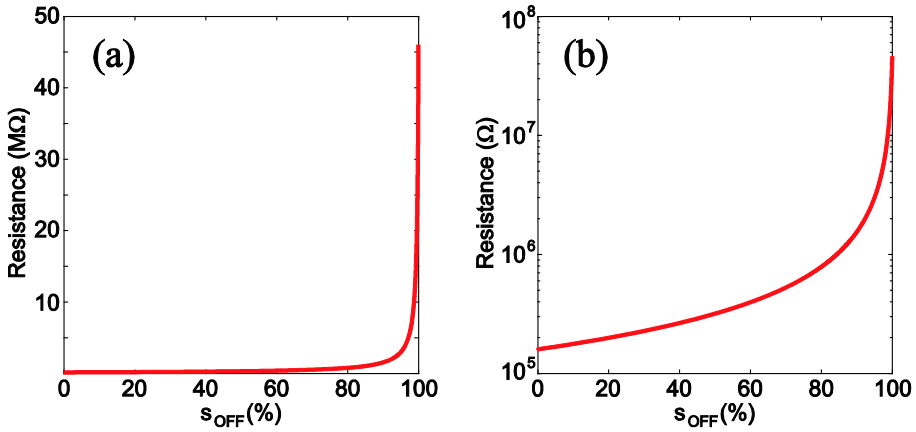


Figure 4.27 (a) FTJ resistance as a function of s_{OFF}. (b) The same results in log scale.

According to Eq. (4.22), even if s_{OFF} grows up to 80%, the resistance reaches $5R_{ON}$, which is still much smaller than R_{OFF}~$300R_{ON}$. This result is in agreement with Figure 4.27. Therefore the FTJ resistance is strongly nonlinear to s_{OFF}, in particular, the resistance varies more slowly if s_{OFF} is smaller.

Interestingly, similar effect is found in the curve of the FTJ resistance versus the programming duration. A typical example is shown in Figure 4.28, where a voltage of 3 V with varying duration is applied to program an ON-state FTJ while the resistance is readout at 0.1 V. Clearly, the FTJ resistance rises slowly during the earlier stage, but more and more quickly with the duration increasing, till the saturation at R_{OFF}. Two reasons can explain this effect: first, the resistance remains ON state before the domain nucleation is activated; second, the grow rate of the

FTJ resistance increases with the domain wall propagation time, as Eqs. (4.23)–(4.24), which are obtained by combining Eq. (3.20) with Eq. (4.22).

$$R \simeq R_{ON} \times \exp\left(\frac{T_P^2}{\tau_P^2}\right) \tag{4.23}$$

$$\frac{\mathrm{d}R}{\mathrm{d}T_P} \simeq \frac{2T_P R_{ON}}{\tau_P^2} \times \exp\left(\frac{T_P^2}{\tau_P^2}\right) \tag{4.24}$$

where T_P is the domain wall propagation time.

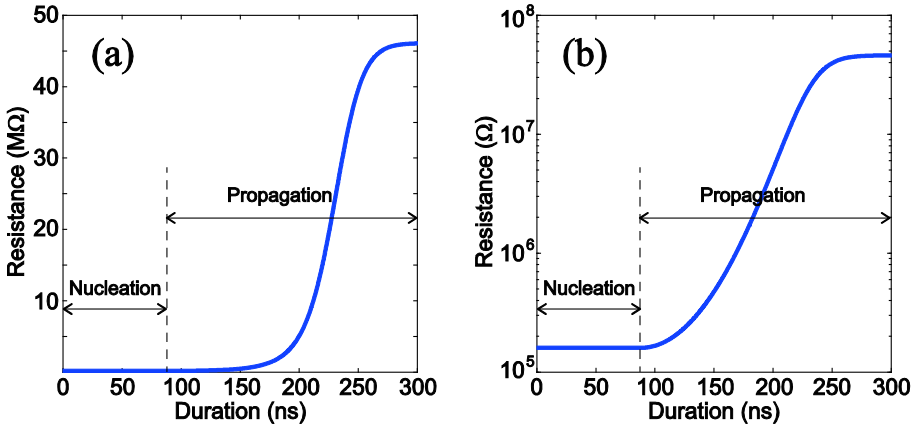


Figure 4.28 (a) FTJ resistance versus the duration of the applied voltage. (b) The same results in log scale.

The above effect provides the possibility of performing two-input Boolean logic functions inside a single FTJ. At the beginning of each logic operation, the FTJ is set to the ON state. The logic inputs '0' and '1' are represented by two sequential programming pulses with large and small amplitudes, respectively. The logic outputs '0' and '1' corresponds to the OFF and ON states of the FTJ, respectively. Logic functions can be implemented by setting appropriately the width and amplitude of the input pulses. Generally, the pulse amplitude for input '0' is too small to change the FTJ resistance. Thus the focus is on the design of the pulse for the input '1'. Below, we demonstrate the implementation of NOR and NAND logic functions, either of which is functionally complete.

For implementing the NOR logic function, the pulse amplitude for the input '1' is set to large enough so that the FTJ can be programmed to OFF state as long as at least one input is '1'. This method also applies to all the binary memories with a threshold. Using these memories, NOR logic function can be implemented if the pulse amplitudes for inputs '0' and '1' are set to lower and higher than the threshold, respectively.

For implementing the NAND logic function, the pulse amplitude for the input '1' needs to be decreased in order that the FTJ is left at low resistance state unless both two inputs are '1'. This idea is feasible because the FTJ resistance indeed remains relative small value during the initial stage of ON-to-OFF switching, as mentioned above (see Figure 4.28).

A possible design for the FTJ-based Boolean logic block is illustrated in Figure 4.29, where three terminals ('T1', 'T2', and 'EN') are defined. A load resistor is used for the readout. An NMOS transistor serves as a controlling switch. The FTJ is oriented to appropriate direction so that the reset pulse can program it to the ON-state. The logic computing operates in three phases:

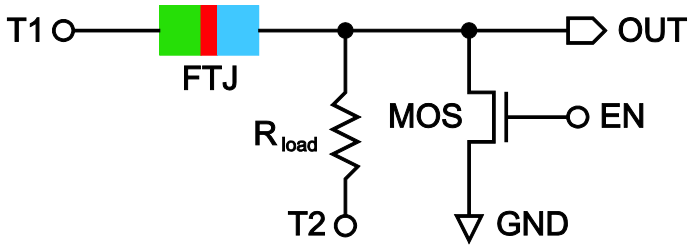


Figure 4.29 A possible design for the FTJ-based Boolean logic block.

i) During the reset phase, 'EN' is set to '1' to activate the transistor. The reset pulses are simultaneously applied to 'T1' and 'T2'. The FTJ is set to the ON state.

ii) During the computing phase, the input pulses are simultaneously applied to 'T1' and 'T2'. The FTJ is programmed to the expected state as the above-mentioned mechanism.

iii) During the readout phase, 'EN' is set to '0' to deactivate the transistor. A readout pulse is applied across the branch 'T1'~'T2'. The logic output is represented by the potential of 'OUT', which depends on the FTJ resistance. High-resistance FTJ results in a low output voltage at 'OUT', which corresponds to logic '0'. Conversely, it corresponds to logic '1'.

Simulation results shown in Figure 4.30 validate NOR and NAND logic functions. The parameters were configured as Table 4.11. The load resistor was set to $\sqrt{R_{ON}R_{OFF}}$ for reliable readout. The other parameters were set to the default values. It is worth noting that the NAND logic suffers from a loss in the output margin (471.6–56.3 mV versus 447.0–56.3 mV). The reason for this loss is that input patterns '01' and '10' inevitably program the FTJ to an intermediate state (see for example, $s_{OFF} = 48.5\%$ in Figure 4.30), but input pattern '00' makes the FTJ remain ON state. Nevertheless, it is seen that the loss in the output margin is very little, because the FTJ resistance is still close to ON state if s_{OFF} is not very large, as discussed above (see Eq. (4.22) and Figure 4.27).

Table 4.11 Parameters for the simulation of the FTJ-based logic block

Parameter	NOR logic	NAND logic
Pulse amplitude for input '1'	3.6 V	3.35 V
Pulse amplitudes for the other signals	Reset: 4 V; Input '0': 500 mV; Readout: 500 mV	
Pulse width	Reset: 50 ns; Programming: 100 ns; Readout: 50 ns	
Load resistor	2.7 MΩ	
W/L of the transistor	25	

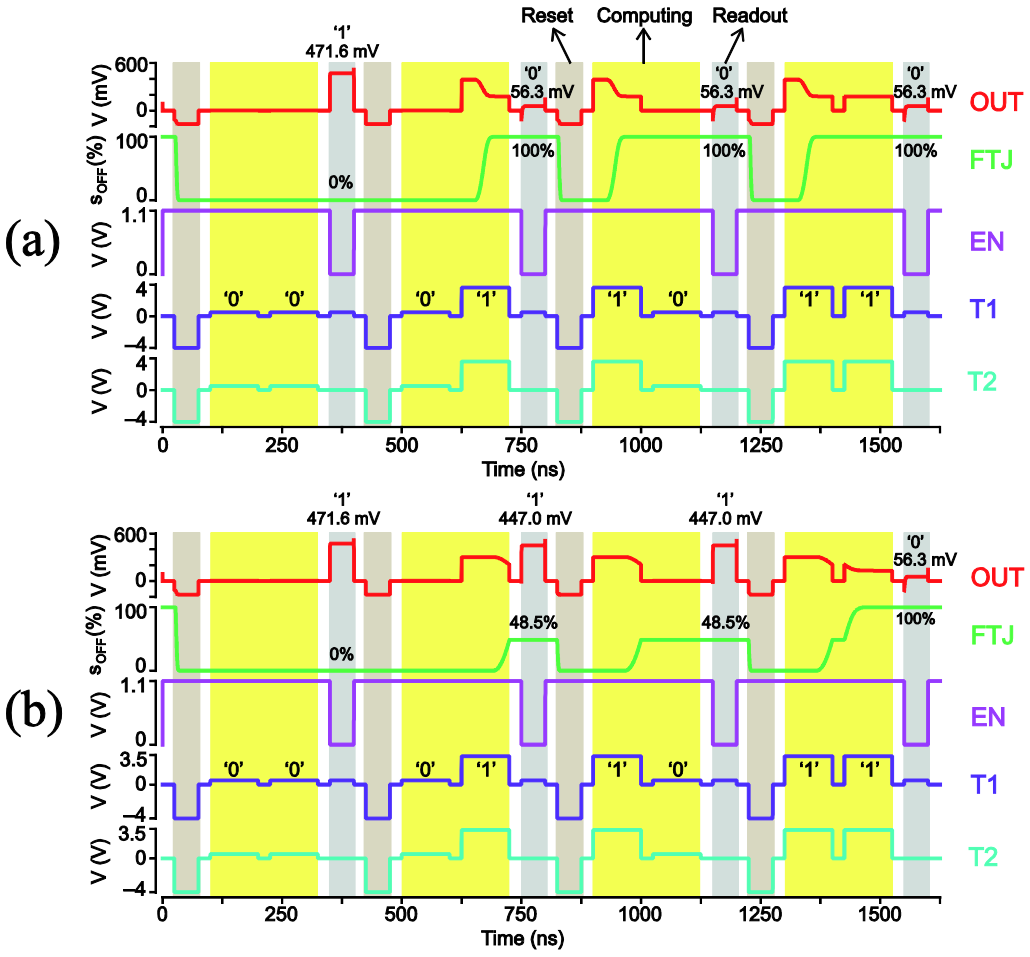


Figure 4.30 Transient simulation of the FTJ-based logic block: (a) NOR logic, (b) NAND logic.

4.3.2 Performance optimization

The performance of the proposed logic block is strongly related to the width and amplitude of the input pulse. Here we aim to improve the output margin and computing energy by optimizing the input pulses. They are calculated by

$$\Delta V = V_H - V_L \tag{4.25}$$

$$E_{\text{com}} = V_{\text{in}} \times \int_0^{T_{in}} \left[i_{\text{FTJ}}(t) + i_{\text{load}}(t) \right] \mathrm{d}t \tag{4.26}$$

where V_H and V_L are the voltages of outputs '1' and '0', respectively. i_{FTJ} and i_{load} are the currents flowing through the FTJ and the load resistor, respectively. V_{in} is the amplitude of the input pulse. T_{in} is the input pulse width.

As is indicated in Figure 4.30, the computing result of '01' (or '10') directly determines the output margin. Moreover, it dictates the type of logic function to be implemented. If the computing result of '01' (or '10') is close to 471.6 mV, the logic block fitter for implementing NAND logic function. Otherwise, if close to 56.3 mV, NOR logic function is a better choice.

With regard to the computing energy, the input pattern '00' has a fixed amplitude of 500 mV and consumes a tiny energy compared with the other input patterns. Therefore, we only calculate the sum of the computing energy for input patterns '01', '10' and '11'.

Figure 4.31(a)–(b) show the output margin as a function of the pulse width and amplitude of input '1'. Take the 80 ns pulse width (the blue curve) for example, three voltage regions can be seen, as follows.

i) If the pulse amplitude for input '1' is smaller than 3.3 V, the domain nucleation cannot be activated within 80 ns so that the FTJ remains ON state regardless of input pattern, thus the output margin is zero (see Figure 4.31(a)).

ii) If between 3.33 V and 3.54 V, for NAND and NOR logic, the output margins reveal the opposite change trends with the pulse amplitude. The reason is that the sum of output margins for NAND and NOR logic is fixed to 471.6 mV. An input pulse of a larger amplitude programs the FTJ closer to OFF state, which results in a decrease in the output margin for NAND logic but an increase for NOR logic (see Figure 4.30 and Figure 4.31(a)–(b)).

iii) If larger than 3.54 V, the output margin for NOR logic saturates because the input patterns '01', '10' and '11' can program the FTJ to the complete OFF state. The FTJ resistance remains the maximum even if the pulse amplitude continues to increase.

The other two curves (for the pulse width of 90 and 100 ns) also show similar trend. The difference is that the transition voltage between two regions is shifted left with the pulse width increasing.

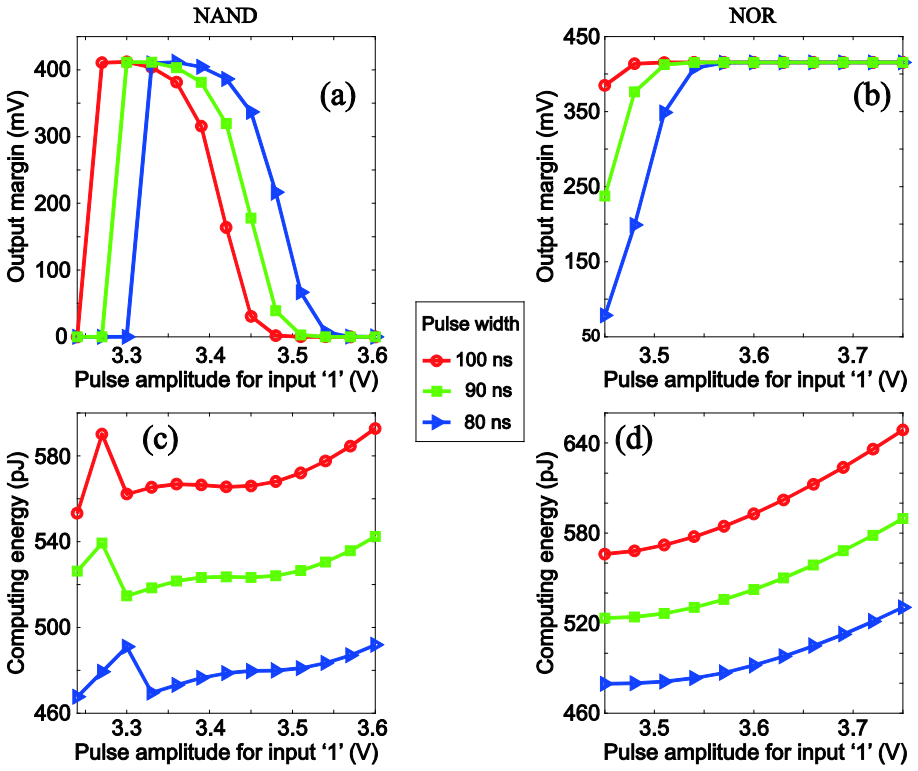


Figure 4.31 (a)–(b): output margin versus pulse amplitude of input '1' for NAND and NOR logic functions, respectively; (c)–(d): computing energy versus pulse amplitude of input '1' for NAND and NOR logic functions, respectively.

Figure 4.31 (c)–(d) show the results of the computing energy. Generally, the computing energy increases with the pulse width and amplitude. One exception is that the energy decrease when the pulse amplitude crosses from the region-(i) to region-(ii), because in region-(i) the FTJ is kept at ON state and carries larger current.

From the results in Figure 4.31, we infer that the two transition voltages (i.e. 3.33 V and 3.54 V when the pulse width is 80 ns) are the optimum pulse amplitudes for input '1' of NAND and NOR logic, respectively. At these two voltages, the logic block obtains the maximum output margin while avoids the exceeding energy consumption. Decreasing the pulse width can improve the computing energy and speed, but it increases the optimum pulse amplitudes due to the left shift of the curves in Figure 4.31 (a)–(b).

4.4 Conclusion

The FTJ is essentially a nanoscale, non-volatile and passive memristor, thus its application involves NV memories, neuromorphic systems and NV logic circuits, all of which have been demonstrated through the circuit simulation in this chapter.

Firstly, we designed an FTRAM where the FTJ is used as the binary memory cell. We found that the classic 1T1R cell structure leads to the asymmetric write speed since the high write voltage of the FTJ (3~4 V) causes the serious threshold-loss in the access transistor. For resolving this problem, we used a TG as the access unit to form a 2T1R memory cell, based on which a complete FTRAM equipped with read/write circuits were constructed and simulated.

By using the developed FTJ model and *STMicroelectronics* CMOS 40 nm design kit, we performed a series of simulation to analyze the read/write performance of the proposed FTRAM in terms of device parameters such as the FTJ size and the transistor width. It was demonstrated that the change in device parameters strengthens some performance metrics but lessens the others. Many tradeoff needs to be evaluated to meet specific application requirement.

Secondly, we applied the FTJ to two neuromorphic systems for implementing the unsupervised STDP learning and on-chip supervised learning. In these systems, the FTJ mimics the synapse with its adjustable conductance (or resistance) serving as the synaptic weight. For the STDP learning, we designed a synapse array with crossbar-like architecture. As a synapse, the FTJ can be programmed to the intermediate state, and we need not to keep the symmetric write operation like in the FTRAM. Therefore 1T1R structure is available for our synapse array, where the transistor controls the access of the synapse. A signal scheme was proposed for the synapse array to emulate the STDP learning rule. Transient simulation has been performed to validate the learning process. Theoretical analysis on the simulation results demonstrated that the range of the synaptic change can be adjusted by changing the initial domain configuration, FTJ radius or transistor size.

On-chip supervised learning was demonstrated with a proposed FTJ-based NC, where the FTJ acts as a synapse or a binary switch. An attractive advantage of our NC is the compact learning cell, which includes only two FTJs, four transistors and an inverter. We designed the learning procedure for this NC and demonstrated the parallel learning of ‘AND’ and ‘OR’ logic functions through the transient simulation. *Monte-Carlo* statistical simulation was also performed to validate the fault-tolerance of the proposed NC against the size variation and stuck defect. It was found that the stuck defect is more damaging to the proposed NC. The learning success rate can be improved by adjusting the number of learning epochs.

Finally, we proposed to implement the NV logic computing with the FTJ. We noted that the FTJ resistance varies nonlinearly with the ferroelectric domain growth. This characteristic was used for implementing NAND and NOR logic inside a single FTJ. We designed a compact logic block with an FTJ, a resistor and a transistor. Logic operation was validated by the transient simulation. The optimization of the output margin and computing energy were discussed. Two optimum pulses amplitude for input '1' were found for NAND or NOR logic, respectively, at which the maximum output margin can be obtained without an excess of the computing energy.

This research opens the way to the circuit-level application of the FTJ. Our work demonstrates that ferroelectric polarization can act as a useful state variable in non-volatile circuits and systems.

Chapter 5

Spin-Hall-assisted spin-transfer torque

5.0 Preface

As mentioned in Section 2.2.3, SOT induced by SHE or Rashba effect has been experimentally demonstrated to provide better write performance in both i-MTJs and p-MTJs than the conventional STT. However, for the SOT-i-MTJs, the incubation delay of the conventional STT cannot be eliminated. Moreover, the scalability and retention of i-MTJs are not satisfying. For the SOT-p-MTJs, good scalability, long retention and fast switching speed can be obtained, but an external magnetic field is required to achieve the deterministic switching, which limits its application. To solve this dilemma, we aim to develop a pure-electric SOT-induced switching method for the p-MTJ in this chapter.

Here, a novel switching mechanism called spin-Hall-assisted STT is investigated through the simulation. This mechanism only needs two write currents to switch the p-MTJ in the absence of magnetic field. Firstly, a modified LLG equation considering SHE and STT is proposed to describe the FL magnetization dynamics in the p-MTJ. Numerical simulation is performed to reveal the roles played by SHE and STT in the magnetization switching. The influences of the related parameters on the switching speed are discussed as well. Afterwards, we design and simulate spin-Hall-assisted MFF and MFA to demonstrate the applications of the proposed spin-Hall-assisted STT switching in non-volatile memory and logic circuit. Their write performances such as speed and energy are analyzed and evaluated.

5.1 Simulation and discussion on the spin-Hall-assisted STT

5.1.1 Model and assumptions

The structure of the spin-Hall-assisted p-MTJ and coordinate system are shown in Figure 5.1, where a p-MTJ is deposited above a heavy metal strip. The FL of the p-MTJ is contacted to the heavy metal. Three terminals (‘T1’~‘T3’) are defined at both sides of the heavy metal and the top of the MTJ, respectively. To switch the FL magnetization, two write currents need to be applied to this device. One is called STT write current which flows through the MTJ between ‘T1’ and ‘T3’ (or ‘T2’). The other one is called SHE write current which passes the heavy metal from ‘T2’ to ‘T3’. The STT write current can be spin-polarized by the RL and exerts a conventional STT on the FL magnetization. The SHE write current can generate +X and –X polarized spin currents flowing along both directions of Z-axis. Depending on the sign of spin Hall angle, one of spin currents is injected into the FL and thus exerts a spin torque on the FL magnetization. This torque is called spin Hall torque (SHT) in the present thesis. Under the action of the STT and SHT, the magnetization dynamics in the FL can be described by a modified LLG equation, as

$$\frac{\partial \vec{m}}{\partial t} = -\gamma\mu_0 \vec{m} \times \vec{H}_{\text{eff}} + \alpha \vec{m} \times \frac{\partial \vec{m}}{\partial t} - \frac{\gamma \hbar}{2et_{\text{F}} M_{\text{s}}} \left[PJ_{\text{STT}} \vec{m} \times \left(\vec{m} \times \vec{m}_{\text{r}} \right) + \eta_{SH} J_{\text{SHE}} \vec{m} \times \left(\vec{m} \times \vec{\sigma}_{\text{SH}} \right) \right] \tag{5.1}$$

where the last three items in the right side of the equation are, in turn, Gilbert damping torque, STT and SHT. $\vec{\sigma}_{SH}$ represents the polarization orientation of the injected spin current. J_{STT} and J_{SHE} are the STT and SHE write current densities, respectively. Here a positive J_{STT} means that the STT write current flows from FL to RL (along +Z direction). A positive J_{SHE} means that the direction of the SHE write current is from 'T2' to 'T3' (along +Y direction). The other parameters have been described in Eq. (2.12).

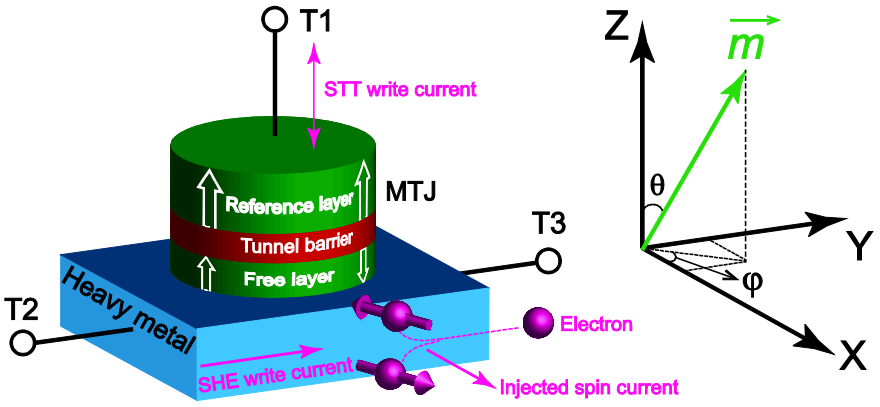


Figure 5.1 Structure of the spin-Hall-assisted MTJ and coordinate system.

To perform numerical simulation with Eq. (5.1), unit magnetization vector in the FL are defined as

$$\vec{m} = \sin\theta\cos\varphi\vec{e}_x + \sin\theta\sin\varphi\vec{e}_y + \cos\theta\vec{e}_z = m_x\vec{e}_x + m_y\vec{e}_y + m_z\vec{e}_z \tag{5.2}$$

where θ and φ are the polar and azimuthal angles, respectively. The objective of the numerical simulation is to resolve time-dependent (θ, φ), which can completely describe the magnetization direction of the FL.

Besides the STT and SHT, both write currents can induce field-like torques, which are expressed as

$$\tau_{FL-STT} = \frac{\gamma \hbar}{2et_F M_s} J_{STT} \xi_{FL-STT} \left(\vec{m} \times \vec{m}_r \right) \tag{5.3}$$

$$\tau_{FL\text{-}SHT} = \frac{\gamma\hbar}{2et_F M_s} J_{SHE}\xi_{FL\text{-}SHT}\left(\vec{m}\times\vec{\sigma}_{SH}\right) \tag{5.4}$$

where ξ_{FL-STT} and ξ_{FL-SHT} are coefficients evaluating the relative strength of the field-like torques with respect to STT and SHT, respectively. Here the action of field-like SHT is equivalent to an in-plane magnetic field, which is collinear to Rashba field [30]–[31] (see Eq. (2.16)).

Although field-like torques are experimentally observed in some MTJs [30]–[31], [226], their strengths are dependent on the specific properties (e.g. material and structure) of the device [104]. Moreover, in some other experiments, magnetization dynamics can be correctly described even if ignoring field-like torques [32]–[33], [114], [227]. Therefore, the field-like torques are not taken into account by Eq. (5.1). Their roles and influences will be discussed in Section 5.1.5.

In addition, thermal fluctuation has an impact on the magnetization dynamics and may cause stochastic switching [227]–[228]. Here we assume that the thermal fluctuation only results in a random deviation of the initial polar angle θ_0 around the anisotropy axis. Other thermal effects are ruled out in order to observe clearly the roles played by STT and SHE write currents in the magnetization switching. This assumption is valid if the STT or SHT is strong enough to suppress the thermal fluctuation [227]. That is true for our proposed circuit application in Sections 5.3~5.4, where SHE write current needs to be larger than a critical value to produce a large enough torque (will be explained later). In the following simulations, the initial magnetization in the FL is assumed to have a small deviation from $-Z$-axis, the deviation θ_0 is set to the root square average value [229] at room temperature (300 K), as

$$\theta_0 = \pi - \sqrt{\frac{k_B T}{\mu_0 M_s H_k V_F}} = \pi - \sqrt{\frac{k_B T}{2E}} \tag{5.5}$$

where T is the temperature. E is the thermal stability energy.

The initial azimuthal angle φ_0 is set to 0 without loss of generality. Other system vectors in Eq. (5.1) are listed as follows

$$\vec{\sigma}_{SH} = -\vec{e}_x \tag{5.6}$$

This equation is consistent with the sign of the spin Hall angle of tungsten (W), which is used as the heavy metal in our study.

$$\vec{H}_{eff} = H_k \cos\theta \vec{e}_z \tag{5.7}$$

which includes the contributions of interfacial anisotropy field, uniaxial anisotropy field and demagnetization field.

$$\vec{m}_r = \vec{e}_z \tag{5.8}$$

which means that the RL magnetization is aligned to +Z axis. The initial state of the MTJ is AP magnetic configuration as FL magnetization is close to –Z axis (see Eq. (5.5)).

With the above assumption, Eq. (5.1) was numerically resolved by Runge-Kutta iterative algorithm. The default values of the parameters are listed in Table 5.1. These values give a thermal stability factor of 60 and a critical current density of 0.9 $\mathrm{MA/cm^2}$ for the STT, which is in agreement with the future technology requirement [230]. The simulation results will be discussed in the following sections.

Table 5.1 Parameters for the simulation of LLG equation

Parameters	Description	Values
t_F	FL thickness	0.7 nm
S	MTJ surface area	90 nm × 90 nm
P	Spin polarization of the tunnel current	0.62 *
M_s	Saturation magnetization	8.8×10^5 A/m
H_k	Anisotropy field	8×10^4 A/m
α	Gilbert damping constant	0.03
η_{SH}	Spin Hall angle	0.3

* determined by TMR ratio = 120%.

5.1.2 Magnetization dynamics in the absence of STT

Firstly, we studied the magnetization dynamics in the FL under the action of a single SHE write current, meanwhile no STT write current is applied. In this case, the polarization orientation (X-axis) of the injected spin current is perpendicular to the magnetic anisotropy (Z-axis) of the MTJ. This geometrical relationship is analogous to the orthogonal spin transfer (OST) proposed by Ref. [231], as shown in Figure 5.2. In an OST device, the anisotropies of the FL and RL are aligned along the in-plane direction, and an additional perpendicular-magnetized layer (PL) serves as the polarizer. When a current flows through the OST device, it is polarized along Z-axis by the PL and injected into the FL with the anisotropy along X-axis. Therefore, compared to the spin-Hall-assisted MTJ, the directions of the anisotropy and injected spin polarization in the OST device are swapped. Corresponding LLG equation is expressed as

$$\frac{\partial \vec{m}}{\partial t} = -\gamma\mu_0 \vec{m} \times \vec{H}_{\text{eff}} + \alpha \vec{m} \times \frac{\partial \vec{m}}{\partial t} - \frac{\gamma \hbar P}{2et_{\text{F}} M_{\text{s}}} J\vec{m} \times \left(\vec{m} \times \vec{m}_p\right) \tag{5.9}$$

where $\vec{m}_p = \vec{e}_z$ is the unit vector along the PL magnetization. J is the write current density. The spin torque caused by the polarization of the RL is neglected in this equation.

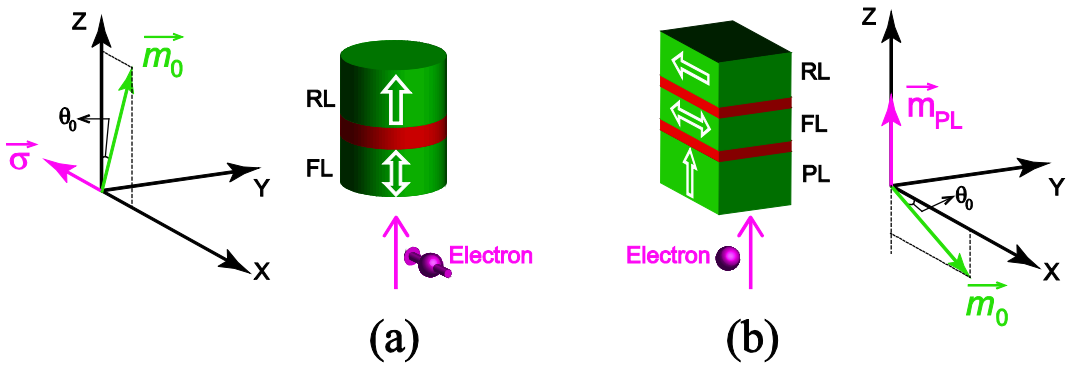


Figure 5.2 Geometrical relationship between magnetization and the injected spin in (a) spin-Hall-assisted MTJ, and (b) OST device.

If $J_{STT} = 0$, Eq. (5.9) has the similar form to Eq. (5.1). The spin torques in Eq. (5.1) and Eq. (5.9) are expressed as

$$\vec{\tau}_1 = -\frac{\gamma \hbar \eta}{2et_{\text{F}} M_{\text{s}}} J_{\text{SHE}} \vec{m} \times \left(\vec{m} \times \vec{\sigma}_{\text{SH}}\right) \tag{5.10}$$

$$\vec{\tau}_2 = -\frac{\gamma \hbar P}{2et_{\text{F}} M_{\text{s}}} J\vec{m} \times \left(\vec{m} \times \vec{m}_{\text{p}}\right) \tag{5.11}$$

Assume that the angles between the initial magnetization $\vec{m}_0$ and anisotropy axis are the same for both equations, these two spin torques exert the same influence on their respective $\vec{m}_0$, since two configurations are equivalent if X- and Z-axis are exchanged, as shown in Figure 5.2.

However, the magnetization dynamics of these two devices are not exactly the same, because the effective field in an OST device has a different expression from that in the spin-Hall-assisted MTJ, as

$$\vec{H}_{\text{eff}} = H_{\text{k}} \left(\vec{m} \cdot \vec{e}_x\right) \vec{e}_x - M_{\text{s}} \left(\vec{m} \cdot \vec{e}_z\right) \vec{e}_z \tag{5.12}$$

where the first and the second terms in the right side of the equation are the anisotropy field and the demagnetization field, respectively. They are not collinear with each other, different from the case of p-MTJs.

Despite of the different $\vec{H}_{eff}$, we argue that the simulation results of Eq. (5.1) can still be explained by some theories about OST device, especially during the initial switching stage when the demagnetization field is not significant. Detailed results and analysis are discussed below.

Figure 5.3 shows the evolution of the FL magnetization driven by four SHE write current of different densities. It is seen that a small J_{SHE} exerts little influence on the magnetization. Only a little disturbance occurs during the initial stage and vanishes with the time proceeding. As J_{SHE} increases, the extent of the disturbance becomes larger. Once J_{SHE} is larger than a critical value (about 25 MA/cm^2), the magnetization is rotated to the in-plane direction ($m_z = 0$) at a high speed (< 1 ns). Similar behavior has also been demonstrated in the OST device, where the magnetization is ultrafast pulled from the in-plane to perpendicular directions if the write current is larger than a critical value [231]. But the magnetization dynamics of these two devices is not exactly identical. In the OST device, the magnetization precesses around the perpendicular axis due to the strong demagnetization field (see Eq. (5.12)). Instead, in the spin-Hall-assisted MTJ the magnetization is stabilized at the in-plane orientation (X-axis) when all the torques become zero, as shown in Figure 5.3(d).

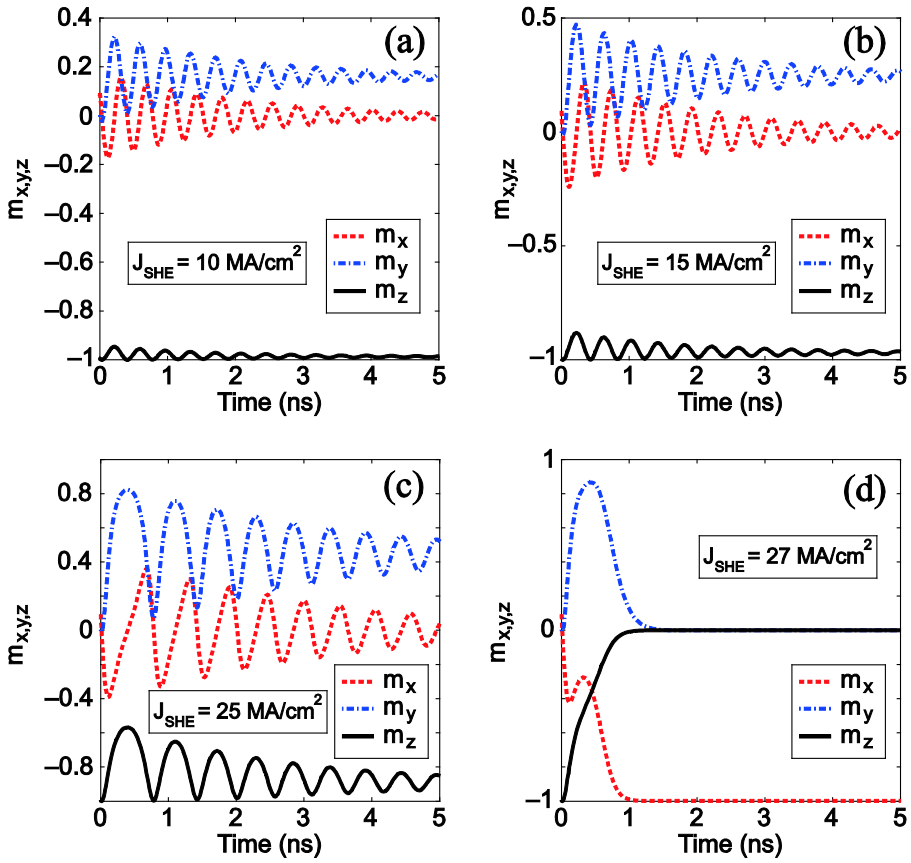


Figure 5.3 Magnetization dynamics driven by a single SHE write current with various densities.

The critical current density ($J_{c,SHE}$) for generating ultrafast rotation is an important parameter. Ref. [232] provided the analytical solution of the critical current density for the OST device. We argue that this solution also applies to the spin-Hall-assisted MTJ since the magnetization dynamics of these two devices are similar during the initial stage of the magnetization switching. The solution is rewritten as

$$J_{c,SHE} = \frac{e}{\hbar} \times \frac{\mu_0 M_s H_k t_F}{\xi \eta_{SH}} \tag{5.13}$$

where ξ is an empirical coefficient, which is determined by fitting to simulation results. Figure 5.4 shows $J_{c,SHE}$ as a function of the anisotropy field (H_k), FL thickness (t_F) and spin Hall angle (η_{SH}) under the various Gilbert damping constants (α). As indicated in the simulation results, the dependences of the critical current density on H_k, t_F and η_{SH} are in good agreement with Eq. (5.13). The fitting between simulation results and analytical solution gives nearly the same values of ξ, which are (1.2214, 1.2298, 1.2385) in Figure 5.4(a), (1.2210, 1.2292, 1.2379) in Figure 5.4(b), and (1.2226, 1.2310, 1.2397) in Figure 5.4(c) when $\alpha = (0.03, 0.02, 0.01)$. The critical current density increases with the damping constant, but the change is negligible. Therefore, Eq. (5.13) is a good estimation expression of $J_{c,SHE}$.

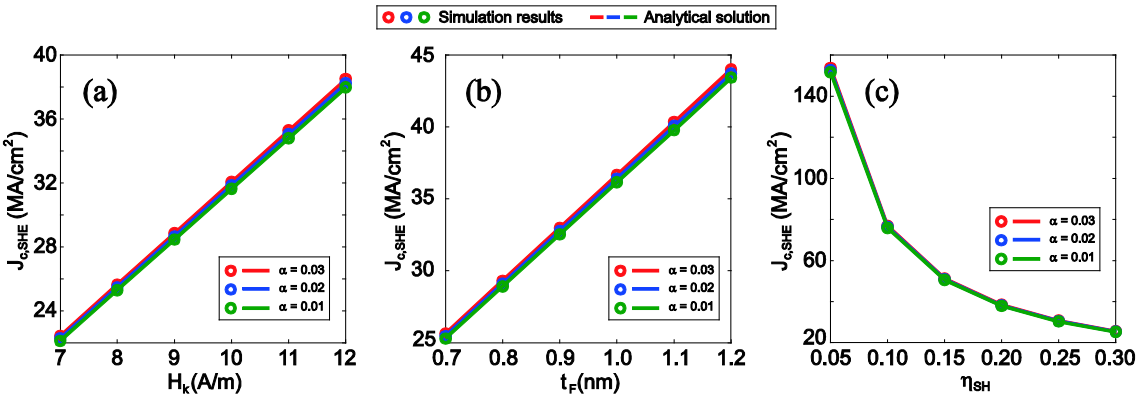


Figure 5.4 Critical current density versus (a) anisotropy field, (b) FL thickness, and (c) spin Hall angle.

In-plane direction ($m_z = 0$) is considered to be a critical point for judging the deterministic magnetization switching. Once the magnetization surpasses the in-plane direction, even if the write currents are removed, the magnetization can relax to the perpendicular anisotropy axis (+Z axis, $m_z = 1$) under the action of the anisotropy field and Gilbert damping torque. In the above simulation, the final FL magnetization cannot surpass the in-plane direction (i.e. $m_z \leq 0$). Therefore we conclude that a single SHE write current cannot achieve deterministic magnetization

switching in the p-MTJ, which is consistent with the experimental observations [30]–[33]. An additional driving force is necessary to achieve the deterministic switching. This is one of the reasons why a magnetic field is required in the works of Refs. [30]–[33]. Our present study aims to replace the magnetic field with an STT write current, as discussed in the following section.

5.1.3 Magnetization dynamics driven by the combination of STT and SHT

Figure 5.5 shows the magnetization dynamics in the FL after adding an STT write current into the configuration of Figure 5.3. Here J_{STT} is fixed while J_{SHE} is set to the same values as Figure 5.3. An additional case of $J_{SHE} = 0$ (see Figure 5.5(a)) is also shown for the comparison. From these results we find that the deterministic switching can be achieved by the combination of STT and SHT, because all the final magnetization pass the in-plane direction.

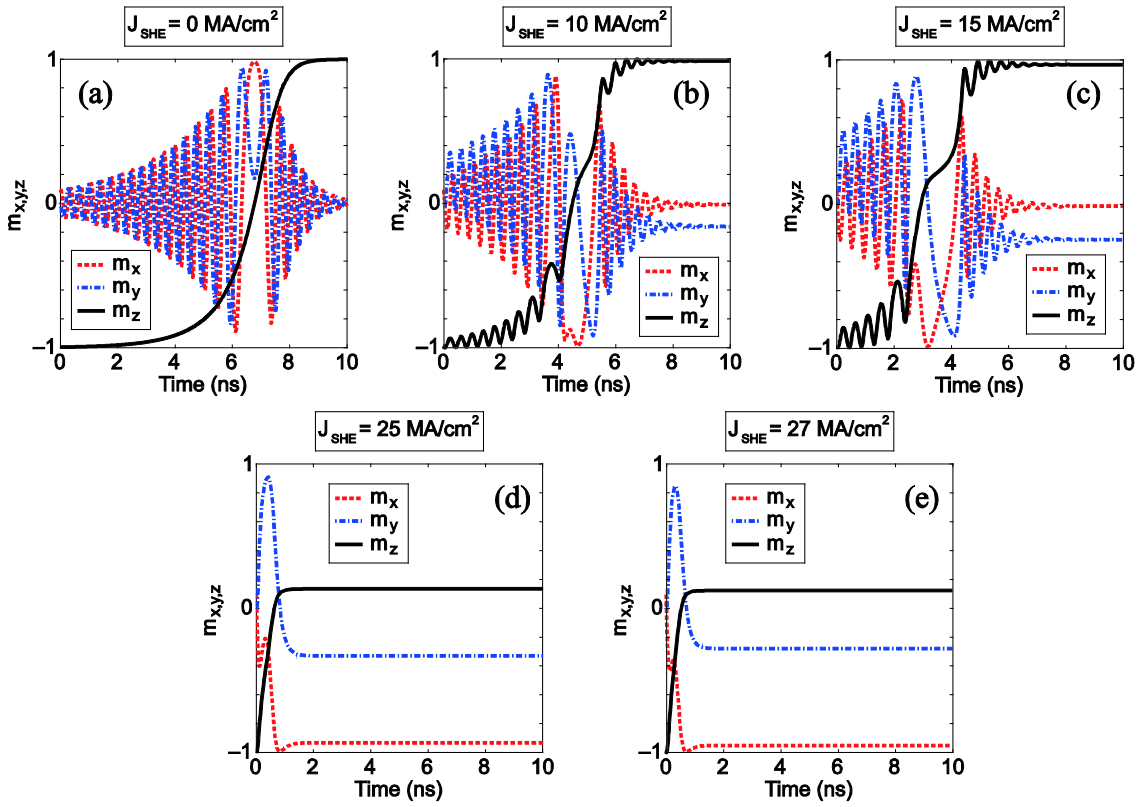


Figure 5.5 Magnetization dynamics driven by the combination of the STT and SHE write currents. Here J_{STT} is fixed to 1.55 MA/cm^2.

In Figure 5.5, the curve profile of the magnetization switching is strongly related to the amount of J_{SHE}. Three types of switching behaviors are summarized as follows:

i) The conventional STT switching occurs if no SHE write current is applied (see Figure 5.5(a)). It is seen that a long incubation delay is required during the initial stage, since the initial magnetizations of the FL and RL are nearly collinear and leads to a small spin torque.

ii) if J_{SHE} is smaller than the critical value $J_{c,SHE}$, some disturbances appear during the switching process, but the overall switching curve is still similar to the conventional STT switching (see Figure 5.5(b)–(c)).

iii) if J_{SHE} is close to or larger than $J_{c,SHE}$, a novel switching behavior totally different from the previous two ones are observed (see Figure 5.5(d)–(e)). The magnetization is directly rotated across the in-plane direction within a short delay (< 1 ns) and stabilized at a specific orientation between in-plane and +Z axis ($0 < m_z < 1$). This result is similar to the Figure 5.3(d) where only a single SHE write current larger than $J_{c,SHE}$ is applied. This demonstrates that the magnetization switching is mainly dominated by SHT rather than STT in this case. This novel switching mechanism produces two advantages: first, the incubation delay of the STT is eliminated by SHT to achieve ultrafast switching. Second, the switching speed is improved without the need to increase the STT write current, thus the risk of barrier breakdown is reduced. The rest of this chapter will be focused on this novel switching mechanism.

We define switching delay as the time required to pull the magnetization across the in-plane direction. The dependence of the switching delay on J_{SHE} is shown in Figure 5.6, where two curves correspond to different J_{STT}. Overall, the switching delay decreases as J_{SHE} increases, but some fluctuations appear in this curve. These fluctuations may result from the back-to-forth motion of m_z during the initial stage of the magnetization switching, as illustrated in Figure 5.5(b)–(c). In addition, the gap between two curves decreases and even vanishes with the increasing J_{SHE}, which confirms the above conclusion that the role of the SHT becomes more and more dominant as J_{SHE} increases. When J_{SHE} is larger than $J_{c,SHE}$, the change in J_{STT} has almost no impact on the switching speed.

Although this novel switching mechanism promises to achieve ultrafast write operation for the MTJ, its application is inhibited by the fact that the magnetization cannot be completely switched to the perpendicular anisotropy axis (see Figure 5.5(d)–(e), where m_z cannot reach 1). This demonstrates that the large SHT play an assisting role during the initial stage of the magnetization switching but an obstructive role after the magnetization passes the in-plane direction. To achieve the complete switching, one solution is to remove the SHE write current at an appropriate time. This idea is validated by the comparison of simulation results between Figure 5.7(a) and (b). For Figure 5.7(a), the STT and SHE write currents with the same duration (4 ns) are simultaneously applied, but the magnetization remains unchanged after 0.5 ns. It means that the

optimum duration of the SHE write current is 0.5 ns. Hence in Figure 5.7(b) we remove the SHE write current at 0.5 ns so that the STT continues to achieve the complete switching.

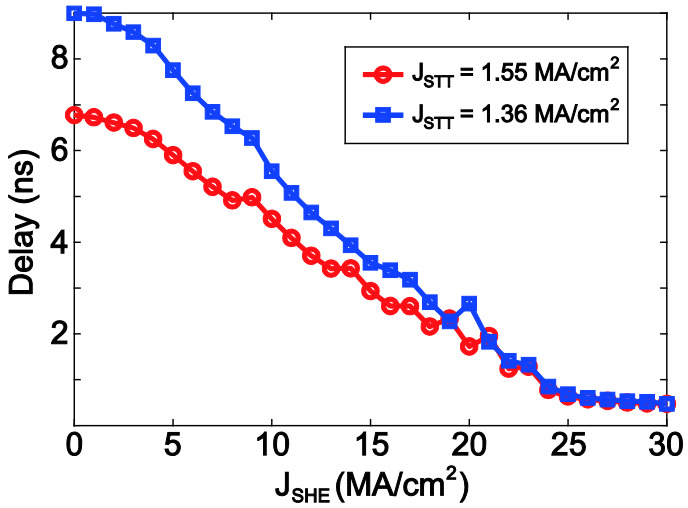


Figure 5.6 Switching delay as a function of the SHE write current density.

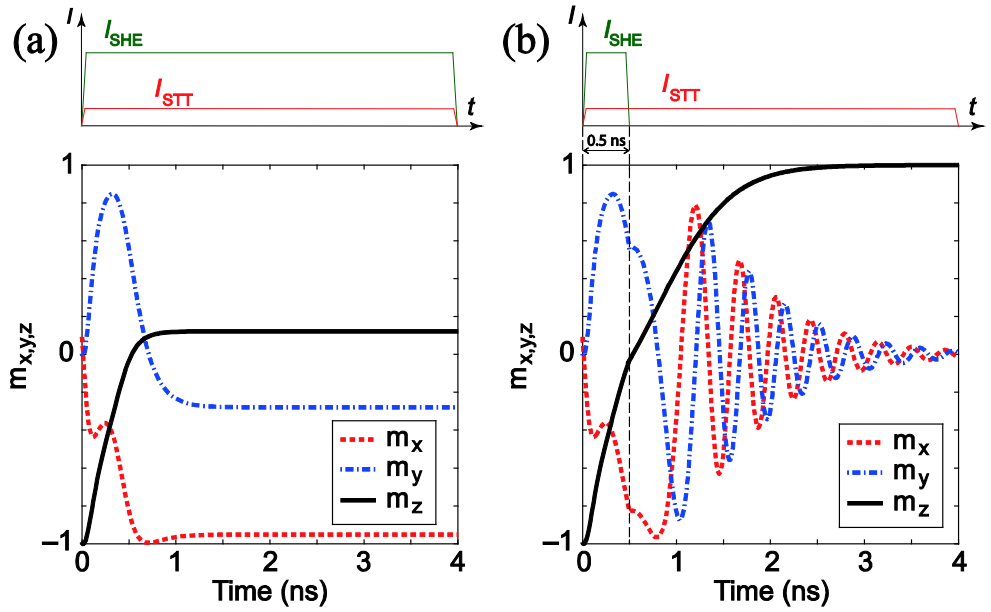


Figure 5.7 Influence of the duration of the SHE write current on the magnetization dynamics. Upper insets show the waveform of the write currents. The STT and SHE write current are set to 1.55 MA/cm^2 and 27 MA/cm^2, respectively.

In sum, a large enough SHE write current with an appropriate duration can assist the STT to eliminate the incubation delay and to achieve the ultrafast magnetization switching. Such a switching mechanism is named spin-Hall-assisted STT switching, which means that SHE and STT

play assisted and deterministic roles, respectively, in the magnetization switching. Figure 5.8 shows the comparison of the magnetization trajectories between the conventional STT and the spin-Hall-assisted STT switching. The elimination of the incubation delay can be clearly seen.

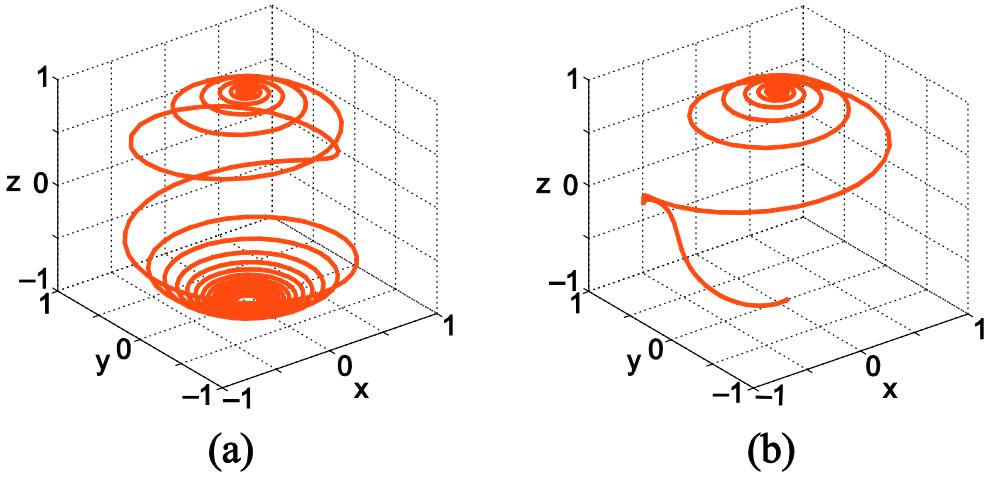


Figure 5.8 Trajectories of the magnetization driven by (a) the conventional STT switching and (b) the spin-Hall-assisted STT switching.

5.1.4 Influences of the initial azimuthal angle and the SHE write current direction

The influence of the initial azimuthal angle on the switching delay is illustrated by the simulation results of Figure 5.9. It is seen that, unlike the STT, the efficiency of the SHT is sensitive to the initial azimuthal angle. More interestingly, while inverting SHE write current, the curve of the switching delay versus the initial azimuthal angle has a phase shift of π. For explaining this phenomenon, we solved Eq. (5.1) and obtain a pair of coupled differential equations, as

$$\begin{cases} \dfrac{\mathrm{d}\varphi}{\mathrm{d}t} = \dfrac{\gamma\mu_0 H_k \cos\theta - \alpha\xi P J_{STT}}{1+\alpha^2} + \dfrac{\xi\eta_{SH} J_{SHE}}{\left(1+\alpha^2\right)\sin\theta}\left(\sin\varphi - \alpha\cos\theta\cos\varphi\right) \\ \dfrac{\mathrm{d}\theta}{\mathrm{d}t} = -\dfrac{\alpha\gamma\mu_0 H_k \cos\theta + \xi P J_{STT}}{1+\alpha^2}\sin\theta - \dfrac{\xi\eta_{SH} J_{SHE}}{1+\alpha^2}\left(\alpha\sin\varphi + \cos\theta\cos\varphi\right) \end{cases} \tag{5.14}$$

It is inferred from the above solution that (J_{SHE}, φ) and $(-J_{SHE}, \varphi + \pi)$ can give the same results. In other words, inverting the SHE write current is equivalent to adding the initial azimuthal angle by π. Therefore the direction of the SHE write current cannot make a deterministic contribution to the magnetization switching, since the azimuthal angle is actually stochastic.

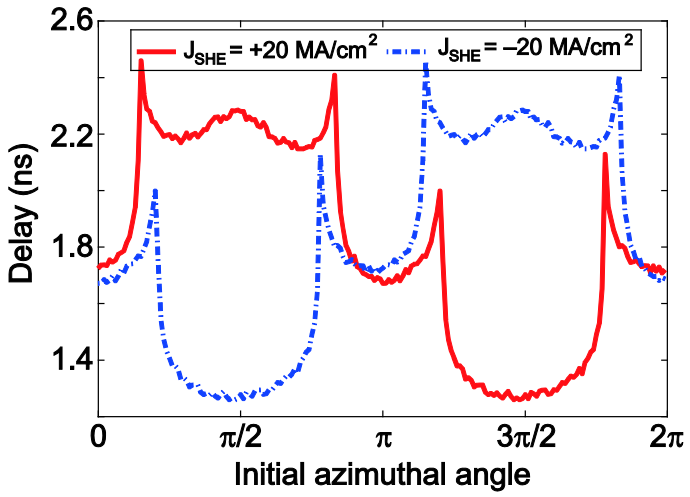


Figure 5.9 Switching delay versus the initial azimuthal angle. Here the STT write current is fixed to 1.55 $\mathrm{MA/cm^2}$.

5.1.5 The influence of field-like torques

The influences of the field-like STT and field-like SHT on the magnetization dynamics were evaluated. Figure 5.10 shows the evolution of the magnetization driven by the combination of the SHT, STT and a single field-like STT. Compared with Figure 5.5, the field-like STT hardly change the overall curve profile of the magnetization switching. Especially when the SHE write current density is larger than the critical value (see Figure 5.10(c)–(d)), the field-like STT is almost suppressed and its action can be neglected.

However, the influence of field-like SHT is more significant and more complicated, as shown in Figure 5.11. If the SHE write current density is smaller than the critical value, the field-like SHT blocks the magnetization switching (see Figure 5.11(a)–(c)), and moreover the blocking impact becomes more strong with the field-like SHT increasing. On the other hand, if it is larger than the critical value, the field-like SHT produces two-sided effect: it may play an assisting role to switch the magnetization closer to the anisotropy axis ($m_z \to 1$, see Figure 5.11(d) and (f)). Or it may pull the magnetization backwards the initial state ($m_z \to -1$, see Figure 5.11(e)). But the quantitative dependence is not very clear.

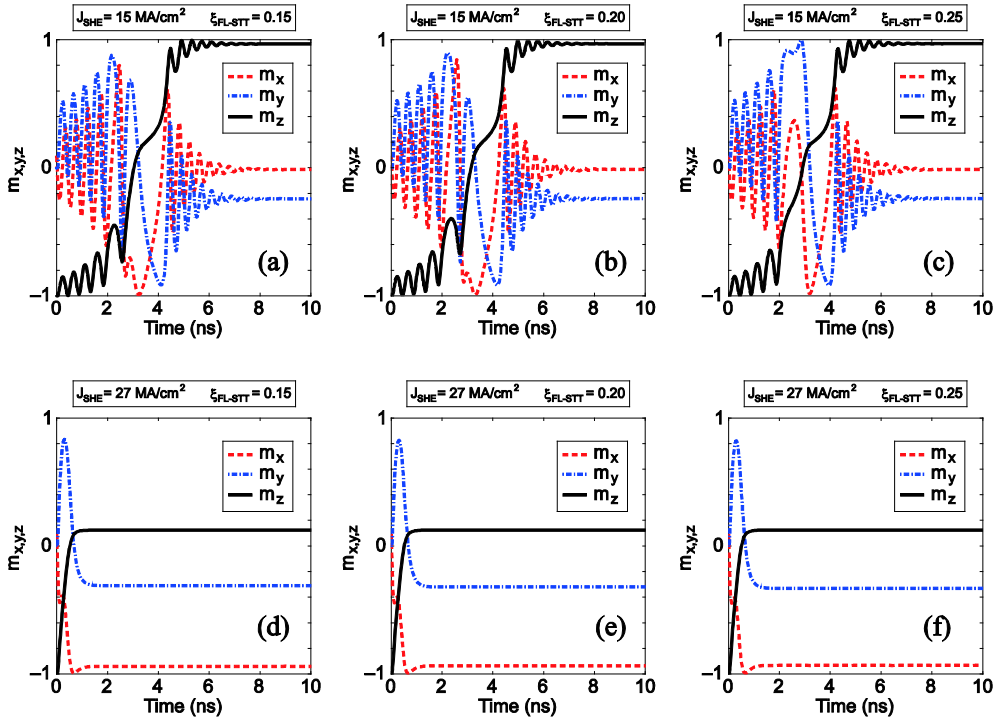


Figure 5.10 Influence of the field-like STT on the magnetization dynamics. Here the STT write current density is fixed to 1.55 MA/cm^2.

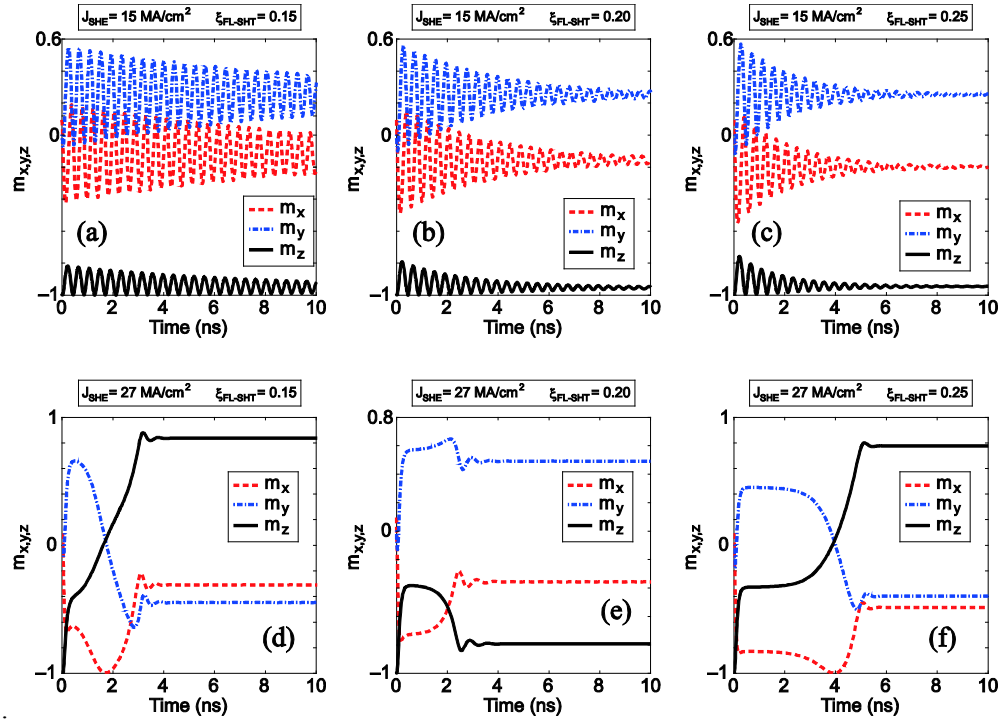


Figure 5.11 Influence of the field-like SHT on the magnetization dynamics. Here the STT write current density is fixed to 1.55 MA/cm^2.

As mentioned in Section 5.1.1, the field-like SHT can be regarded as the torque induced by Rashba field since they are collinear. Currently, Rashba fields observed by various groups are very different. Refs. [30]–[31] suggested that Rashba field dominates the magnetization switching in the perpendicular-magnetized FM layer. However, Refs. [32]–[33] claimed that the perpendicular magnetization is switched by SHE without the measurable Rashba field. In addition, the authors of Ref. [233] presented a simulation study on the SOT-induced magnetization dynamics in the presence of a field-like SHT. They also concluded that a large enough field-like SHT can assist the magnetization switching. Our present results in Figure 5.11 involve the combined action of STT, SHT and field-like SHT, which has not been experimentally studied so far. Here we just provide a general conclusion that field-like SHT may have a non-ignorable impact on the reversal of the perpendicular magnetization.

Recall Figure 5.7, for the spin-Hall-assisted STT switching, the aim of SHT is just to eliminate the incubation delay during the initial stage of the magnetization switching. Here, from Figure 5.11(d)–(f), we note that this aim can still be achieved in the presence of the field-like SHT (see the black curves where no incubation delay exist). Therefore, following the idea in Figure 5.7, we found that, even if the field-like SHT is considered, the fast and deterministic switching can still be achieved by removing the SHE write current at an appropriate time, as shown in Figure 5.12, where the switching behavior is very similar to Figure 5.7 and Figure 5.8(b). We conclud that the field-like SHT has little impact on the efficiency of spin-Hall-assisted STT switching.

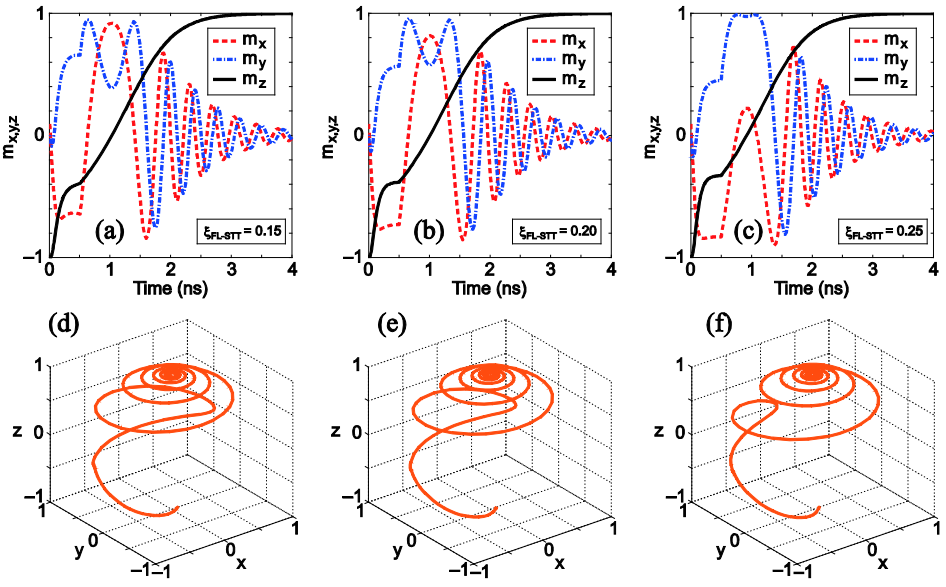


Figure 5.12 Spin-Hall-assisted STT switching in the presence of the field-like SHT. Here the applied currents are the same as Figure 5.7. (a)–(c) The time-dependent magnetization for various strength of field-like SHT. (e)–(f) Corresponding trajectories of the magnetization.

5.2 Compact electrical model of the spin-Hall-assisted MTJ

Based on the above simulation, we aim to further explore the application potential of the spin-Hall-assisted STT in the MTJ-based circuits. For that, an electrical model is required. Following the procedure of Chapter 3, we firstly investigate the related physical models and then translate them into an electrical model with *Verilog-A* language.

The developed model consists of the tunneling resistance model and dynamic switching model. The former is expressed as Eqs. (5.15)–(5.17), which considers the Brinkman model [169], bias-dependent TMR ratio [202], Jullière model [20] and Slonczewski model [94].

$$R_P = \frac{t_B}{F \times \bar{\varphi}^{1/2} \times S} \times \exp\left(\frac{2\left(2m_e e\bar{\varphi}\right)^{1/2}}{\hbar} \times t_B \right) \tag{5.15}$$

$$TMR_0 = \frac{2P^2}{1-P^2} = \frac{R_{AP} - R_P}{R_P} \tag{5.16}$$

$$R_{MTJ}\left(V,\theta\right) = R_P \frac{1+\left(V/V_h\right)^2 + TMR_0}{1+\left(V/V_h\right)^2 + TMR_0\left[\left(1+\cos\theta\right)/2\right]} \tag{5.17}$$

where R_P and R_{AP} are resistances of MTJ under zero bias voltage for the P and AP states, respectively. R_{MTJ} is the resistance of the MTJ at the given V and θ. Other parameters are listed in Tables 5.1~5.2.

Table 5.2 Parameters for the compact model of spin-Hall-assisted MTJ

Parameters	Description	Default values
F	Factor determined by R.A product	3.3141×10^4*
$\bar{\varphi}$	MgO barrier potential height	0.4 V
TMR_0	TMR ratio under zero bias voltage	120%
V_h	Bias voltage at which TMR ratio is divided by 2	0.5 V
ρ_{hm}	Resistivity of the heavy metal	200 μΩ · cm
l, w, d	Length, width and thickness of the heavy metal strip	110 nm, 90 nm, 3 nm

* gives a R.A product of 10 Ω · μm²

The equivalent resistor network for 3-terminal MTJ is shown in Figure 5.13 (a). The STT and SHE write current densities can be calculated by Kirchhoff's circuit laws. The resistance of the heavy metal is calculated by

$$R_{hm} = \beta_{hm} \frac{l}{wd} \tag{5.18}$$

where the related parameters are listed in Table 5.2.

In the dynamic switching model, the field-like STT is neglected since its influence is tiny (see Section 5.1.5). The field-like SHT is not taken into account since its strength and role are still under the discussion. Langevin thermal field is also considered to be negligible because in the following circuits the SHE write current density is set to be larger than the critical value so that the thermal fluctuation is suppressed by the strong SHT. Based on these assumptions, the dynamic switching model can be given by differential equations in Eq. (5.14). The initial polar angle of the FL magnetization is calculated by Eq. (5.5).

Above physical models were programmed and integrated together with *Verilog-A* language. The hierarchy of the electrical model is illustrated in Figure 5.13(c). This model operates with iterative algorithm. At each step, it firstly resolves the FL magnetization with dynamic switching model and then calculates the MTJ resistance with Eqs. (5.15)–(5.17). The model symbol is shown in Figure 5.13(b), which mimics the shape of the three-terminal MTJ. Besides three actual terminals, an additional virtual terminal 'Tmz' is defined to output the perpendicular component of the FL magnetization (m_z).

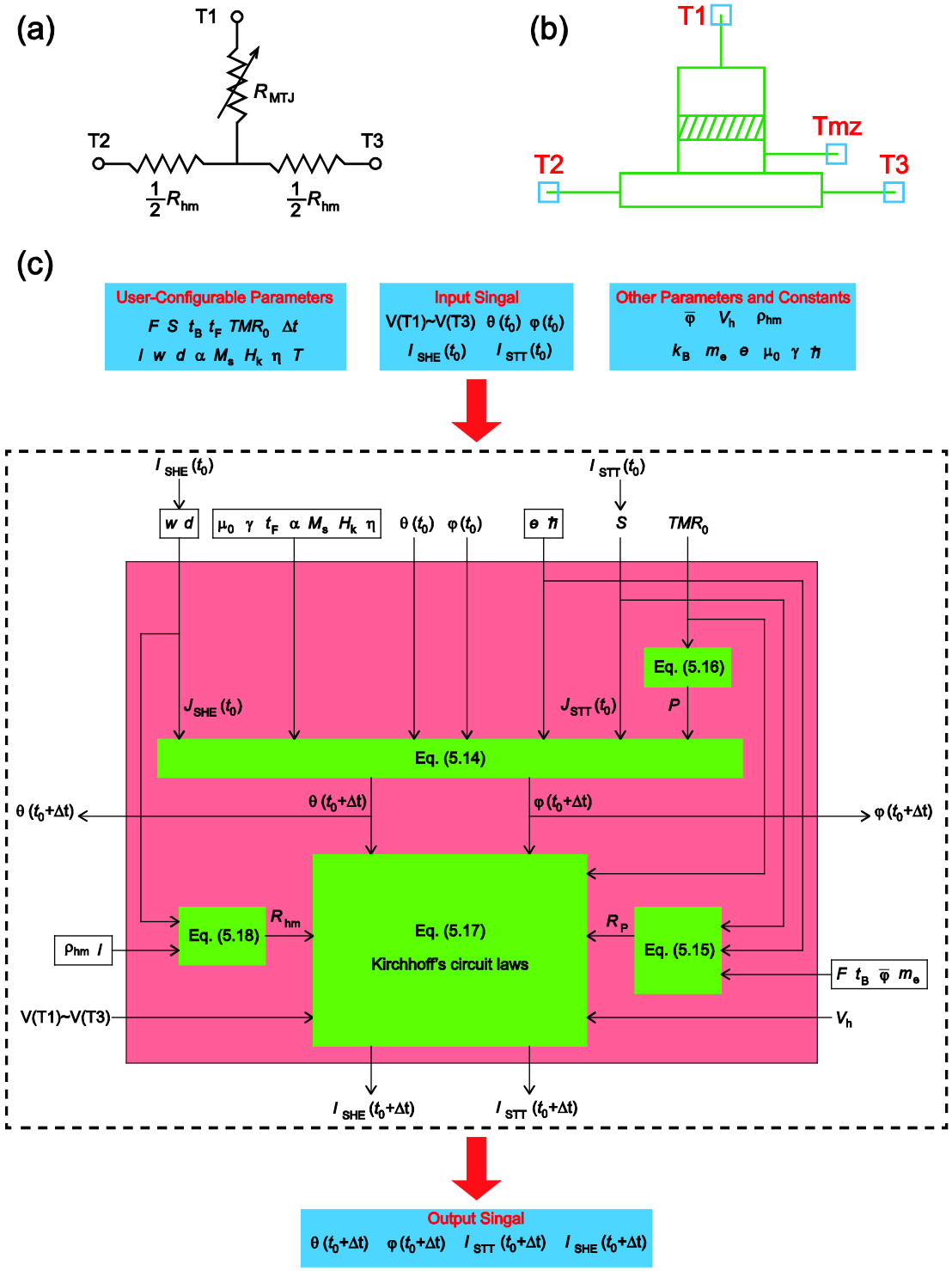


Figure 5.13 (a) Equivalent resistor network for the three-terminal MTJ. (b) Symbol of the developed three-terminal MTJ model on *Cadence* platform. (c) Hierarchy of the developed model.

Single-cell simulation was performed to validate the function of the developed model. The schematic for the simulation is illustrated by Figure 5.14(a), where three voltage sources are

applied to the terminals 'T1'~'T3'. Simulation results are shown in Figure 5.14(b)–(c). During 0~0.5 ns, only a positive voltage is applied to 'T2' while 'T1' and 'T3' are grounded. The SHE write current flows from 'T2' to 'T3' while the STT write current from 'T2' to 'T1'. It is seen that the FL magnetization is switched toward $m_z = 1$ without the incubation delay, in agreement with the simulation results of Section 5.1. During 0.5~5 ns, V3 is set to the same positive voltage as V2 so that no SHE write current flow between 'T2' and 'T3'. Two STT write currents from 'T2' and 'T3' to 'T1' are responsible for achieving the deterministic switching. Similarly, the opposite switching process is also demonstrated during 5~10 ns. These results reproduce the spin-Hall-assisted STT switching as expected. Moreover, it is seen that the currents through the MTJ vary with the FL magnetization, which validates the dependence of the MTJ resistance on the FL magnetization (see Eq. (5.17)). With this developed electrical model, spin-Hall-assisted magnetic circuits can be simulated and analyzed. The present thesis will show two typical applications, MFF and MFA, as discussed below.

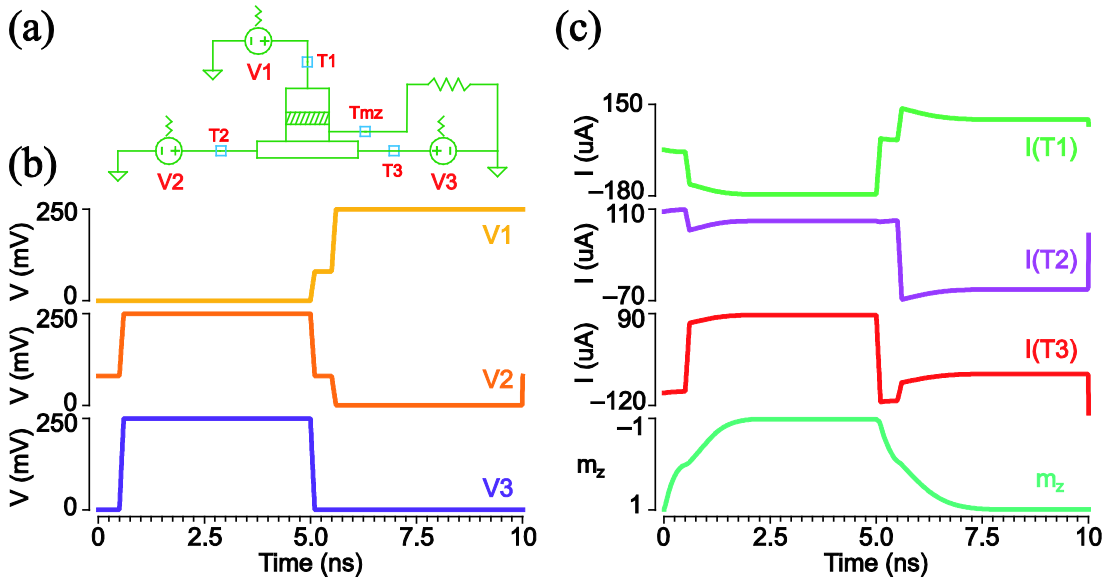


Figure 5.14 (a) Schematic for the single-cell simulation. (b) Signals applied to three device terminals. (c) Simulation results of the current and FL magnetization.

5.3 Magnetic flip-flop array with spin Hall assistance

A flip-flop can store 1-bit data and be used as a key unit in modern digital systems such as microprocessors and filters. Especially, flip-flop is the elementary module for constructing a register file. Recently MFF using the STT-MTJ attracted massive research interest thanks to its advantages such as high speed, unlimited endurance, and CMOS compatibility [164]–[165],

[234]–[235]. In this section, by using the proposed spin-Hall-assisted STT switching, we design a novel MFF array and present the comparison of the write performance with the conventional STT-MTJ-based MFF.

5.3.1 Circuit design

Compared with the previous 1-bit MFF, one remarkable advantage of our proposed MFF array is to be naturally extended to a register file, as illustrated in Figure 5.15. Here the MTJs are organized as the hierarchy of a RAM. Since the used MTJ has three terminals, two access transistors and three BLs are equipped with each cell, forming a 2T1R structure. Each flip-flop is shared by those cells within the same column. When a WL is activated, those cells at the corresponding row are loaded into respective flip-flops to perform read/write operations.

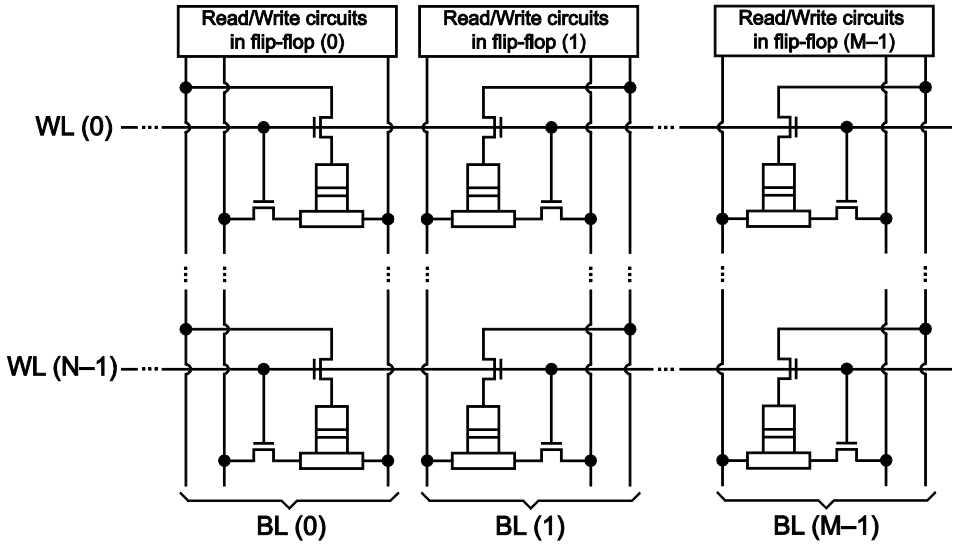


Figure 5.15 Architecture of an N × M bits spin-Hall-assisted MFF.

Figure 5.16 shows the structure of the read/write circuits for the proposed MFF. Our MFF uses master-slave structure to improve the reliability. The master latch is designed with the PCSA mentioned in Section 4.1. Its sensing mechanism has been presented over there. The slave latch is implemented with a conventional CMOS latch [165]. However, the design of the write driver is more complicated since it needs to control appropriately the direction and duration of the STT and SHE write currents. Here the write driver consists of four driving transistors and a series of logic gates. Three input signals are defined: ‘INPUT’ carries the data to be written into the MTJ; ‘EN_W’ and ‘EN_SHE’ controls the activation of the STT and SHE write currents.

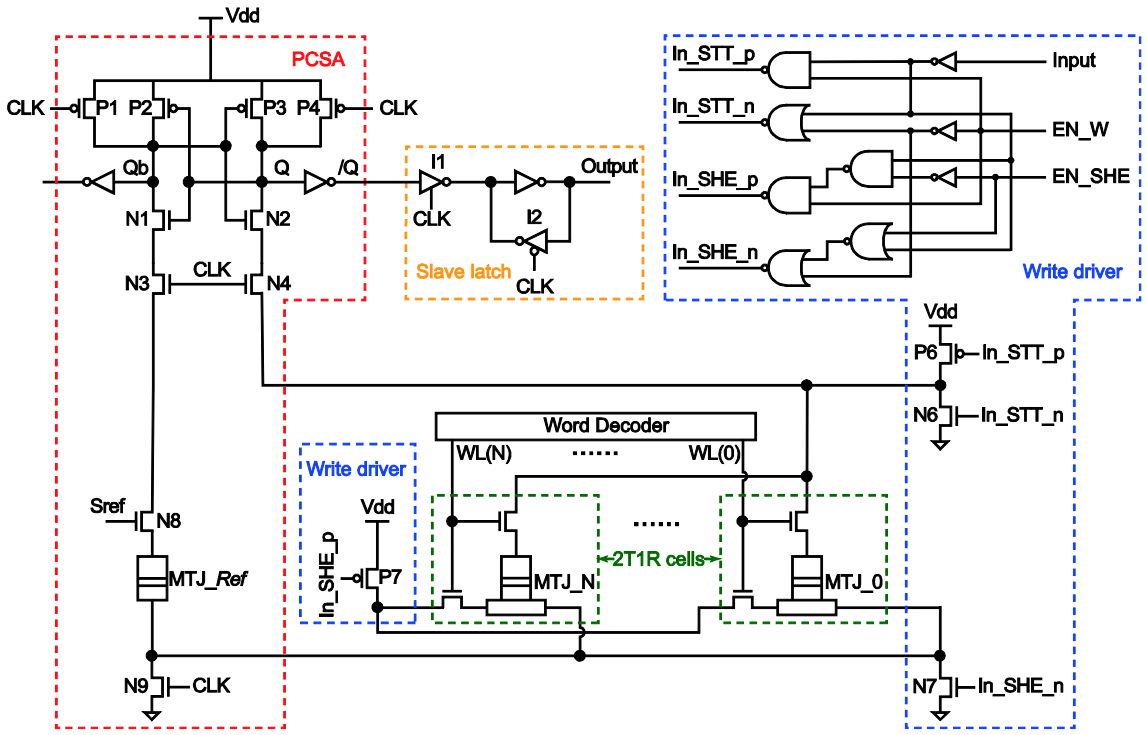


Figure 5.16 Schematic of the read/write circuits for the proposed MFF.

The detailed operation of the proposed MFF will be demonstrated through the simulation results in the next section.

5.3.2 Simulation and validation

Transient simulation of the proposed MFF has been performed with the developed electrical model of the three-terminal p-MTJ and *STMicroelectronics* CMOS 28 nm design kit [38]. The parameters were configured as Table 5.3. The other parameters were set to the default values shown in Tables 5.1~5.2. Simulation results shown in Figure 5.17(a) reproduce the behavior of a positive-edge-triggered flip-flop at an operation frequency of 200 MHz. The change of output state only occurs at the positive edge of the clock signal ('CLK'). Three modes are demonstrated in this figure:

Table 5.3 Parameters for the simulation of the MFF

Parameters	Values
Free layer volume	50 nm × 50 nm × 0.7 nm
Dimension of heavy metal strip	60 nm × 50 nm × 0.7 nm
Gilbert damping constant	0.02*
Thermal stability factor	31.3*

Power supply	1 V
Resistance of reference MTJ	6.4 kΩ**
Transistor width	500 nm for driving, 120 nm for access, 80 nm for PCSA

* gives a data-retention time of 10 hours, and a critical current density of 1 MA/cm^2 for the STT.

**determined by $\sqrt{R_P R_{AP}} + R_{hm}/2$

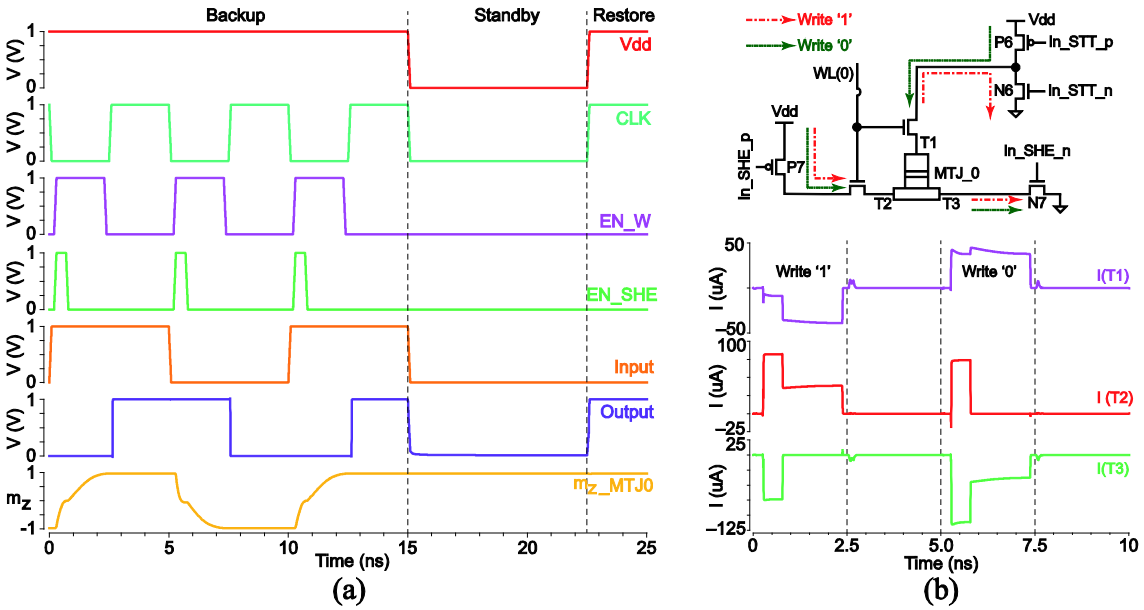


Figure 5.17 Transient simulation of the proposed MFF. (b) Details of the write currents flowing through three device terminals.

i) Backup mode (0~15 ns): the read/write operations are clearly shown during this mode. While 'CLK' = '0', inverter I1 is disabled but I2 is enabled, so that the slave latch can keep precedent data regardless of the state of the master latch. Meanwhile, transistors N3~N4 are deactivated to isolate the write driver from the PCSA. Therefore the charging of PCSA and the write of INPUT data can be simultaneously performed without interactive disturbances. The write operation is triggered after a short time margin (200 ps). The details of write currents are shown in Figure 5.17(b), as analyzed below.

Four driving transistors are controlled by the logic computing of 'INPUT', 'EN_W' and 'EN_SHE'. While writing '1', during the initial 0.5 ns, 'INPUT' = 'EN_W' = 'EN_SHE' = '1'. P6 is deactivated while other three transistors are activated. P7 acts as the shared source of SHE and STT write currents. N6 and N7 act as the sinks of the STT and SHE write currents, respectively. After 0.5 ns, 'EN_W' is set to '0' to deactivate N7. The SHE write current is removed, and the

STT write current achieves the remaining switching process. Writing '0' operates as the same principle, except for changing the roles of transistors as current sources and sinks.

While 'CLK' jumps from '0' to '1' (at the rising edge), transistors P1 and P4 are deactivated but N3~N4 and N9 are activated. PCSA starts to discharge and outputs the data to 'Q'. To avoid the disturbance, the write driver has been turned off by setting 'EN_W' = 'EN_SHE' = '0' just before the jumping of 'CLK'. Once 'CLK' arrives at '1', I1 is enabled while I2 is disabled. The slave latch updates its output from PCSA.

ii) Standby mode (15~22.5 ns): the power and clock signal are turned off ('Vdd' = 'CLK' = '0') to avoid the leakage current. All the active devices are disabled. But the non-volatile data is still stored in the MTJ, as indicated by unchanged m_z.

iii) Restore mode (22.5~25 ns): while the power and clock signal is restarted ('Vdd' and 'CLK' increase from '0' to '1'). PCSA translates the MTJ state into the output data through the charging and discharging processes. That is to say, the output before turning off the power is restored, validating the non-volatility of the proposed MFF.

5.3.3 Performance analysis

For the sake of comparison, we also designed and simulated an STT MFF array. The circuit architecture is similar to the above spin-Hall-assisted MFF, except for replacing the three-terminal MTJ with a two-terminal STT-MTJ. Correspondingly, the 2T1R cell was changed to 1T1R one, and the write driver was also redesigned as Figure 5.18(a). Corresponding results are shown in Figure 5.18(b)–(c). Here the driving transistor width was set to 700 nm for P1/N2 and 300 nm for P2/N1. The reference MTJ was set to 6 kΩ. The other parameters were configured as Table 5.3 except for the access transistor width, which was set to 900 nm in order to achieve the same operation frequency as the above spin-Hall-assisted MFF (200 MHz).

The cell area and write energy of two MFFs were evaluated at the same operation frequency. The cell area is determined by the access transistor width, since the MTJ can be fabricated above CMOS circuits by BEOL. Note that the peripheral circuits (read/write circuits) can be shared by multiple cells and thus cannot dominate the storage density. The write energy is calculated by

$$E_{avg} = \frac{1}{2} V_{dd} \times \left(\int_0^{T_c} i(t)_{0\to1} dt + \int_0^{T_c} i(t)_{1\to0} dt \right) \tag{5.19}$$

where V_{dd} is the supply voltage, T_c is the period of the clock signal, $i(t)_{0\to1}$ and $i(t)_{1\to0}$ are the total currents through the power supply while writing from 0 to 1 and from 1 to 0, respectively.

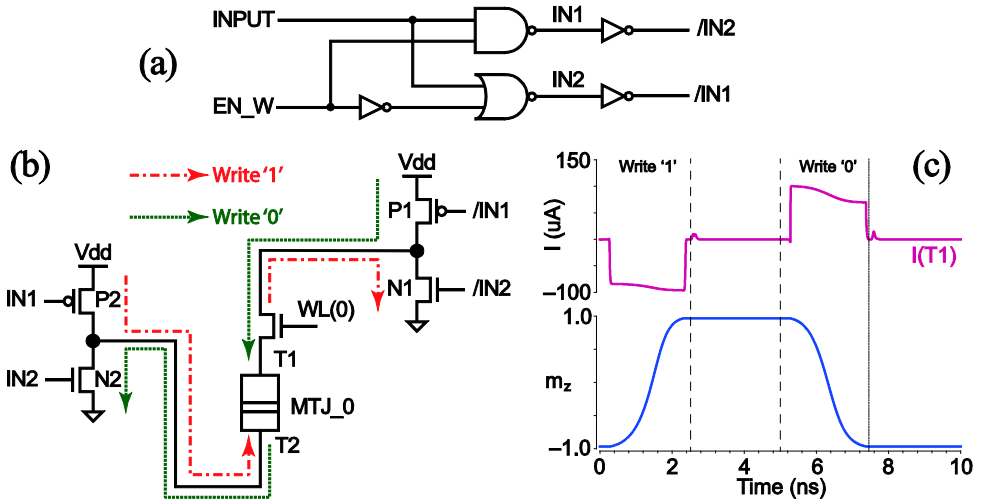


Figure 5.18 (a) Write driver for the STT MFF, (b)–(c) details of the write current and FL magnetization in the STT MFF.

Simulation results demonstrate that the spin-Hall-assisted MFF can use smaller access transistor (120 nm × 2) to shrink the cell area than the conventional STT MFF (900 nm) since it requires smaller write currents. As can be seen from Figure 5.17(b) and Figure 5.18(c), for the spin-Hall-assisted MFF, a 0.5 ns SHE write current of ~74 μA combined with a 2.5 ns STT write current of 37~44 μA is sufficient to write '0', but the conventional STT MFF requires a 2.5 ns STT write current of 70~100 μA. The decrease in the write current brings two improvements: first, the write energy can be saved (122.45 fJ vs. 188.3 fJ). Second, the write voltage across the MTJ is reduced (50~280 mV for the spin-Hall-assisted MFF, but 390~520 mV for the STT MFF), which decreases the risk of the barrier breakdown.

Finally, performance change with the MTJ scaling was further studied. The MTJ shape was designed as a square. For various MTJ size, the thermal stability factor and STT critical current density were fixed (31.3 and 1 MA/cm^2), which was achieved by adjusting the anisotropy field H_k and Gilbert damping constant α. In addition, the size of the heavy metal strip was set to $(L + \Delta L) \times L \times d$, where L is the side length of the MTJ, $\Delta L = 10$ nm, and $d = 3$ nm. The total width of four driving transistors is 4 μm. For the STT MFF, the width ratio of P1~N2 to P2~N1 (see Figure 5.18) needs to be adjusted in each simulation run to keep the symmetry between two write directions. But in the spin-Hall-assisted MFF, symmetric write operation can be always achieved with four driving transistors of the same width (1 μm). Simulation results at the same operation frequency are summarized in Figure 5.19.

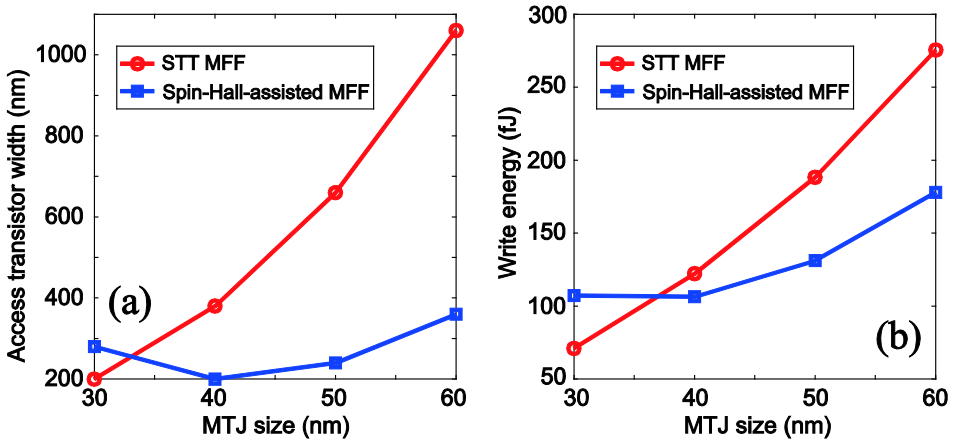


Figure 5.19 Access transistor width (a) and write energy (b) required by an operation frequency of 200 MHz under the various MTJ size.

As indicated in Figure 5.19, both the cell area and write energy are improved by shrinking the MTJ size. The advantage of the spin-Hall-assisted MFF over the STT MFF is significant for the large-size MTJ, but it is weakened with the MTJ scaling and even vanishes below 40 nm node. These results can be explained by Eq. (5.20), which describes the STT switching delay as a function of write current [114]. Both the volume (V_F) and critical STT current ($I_{c,STT}$) increases with the MTJ size, hence, in order to keep the switching speed, the access transistor has to be widened to provide larger write current (I).

$$\frac{1}{\langle\tau\rangle}=\left[\frac{2}{C+\ln\left(\pi^2\zeta/4\right)}\right]\frac{\mu_B P}{eM_s V_F\left(1+P^2\right)}\left(I-I_{c,STT}\right) \tag{5.20}$$

where $\langle\tau\rangle$ is the average switching delay, C is Euler's constant, ζ is the activation energy in units of k_BT, I_c is the critical current for the STT, I is the write current, The other parameters have been described in Table 5.1.

Below 40 nm node, the spin-Hall-assisted MFF suffers from the performance degradation. We attribute it to the dramatic increase in the critical SHE current, as Eq. (5.21). Based on this equation, the critical SHE current is estimated to be 107 μA at $L = 30$ nm, much higher than the critical STT current (only 9 μA). Therefore wider access transistor is required by the spin-Hall-assisted MFF. In addition, part of STT current is consumed by half of the heavy metal strip in the spin-Hall-assisted MFF, which also contributes to the performance degradation. For large-size MTJ, the gap between critical SHE and STT currents is not so great (for example, 54 μA versus 36 μA at $L = 60$ nm), thus spin-Hall-assisted MFF outperforms the STT MFF above 40 nm node.

$$I_{c,SHE} = \frac{e}{\hbar} \times \frac{\mu_0 M_s H_k t_F}{\xi \eta_{SH}} \times Ld = \frac{e}{\hbar} \times \frac{\mu_0 M_s H_k t_F L^2}{\xi \eta_{SH}} \times \frac{d}{L} = \frac{e}{\hbar} \times \frac{2E}{\xi \eta_{SH}} \times \frac{d}{L} \tag{5.21}$$

where all the parameters have been described above.

Although the performance improvement of the spin-Hall-assisted MFF in cell area and write energy is limited, we found that the write voltage of the MTJ in spin-Hall-assisted MFF is always smaller than in the STT MFF, even if below 40 nm node. This means that the spin-Hall-assisted MFF is competitive in high-reliability write technology.

5.4 Magnetic full-adder with spin Hall assistance

Besides the flip-flop, the full-adder is also a core component in all sorts of processors. It achieves the basic addition computation of the arithmetic unit and thus dominates the processor performance. Here, we apply the spin-Hall-assisted STT switching to the design of an MFA.

Similar to MFF, the spin-Hall-assisted MFA was also designed based on the PCSA, as Figure 5.20(a)–(b). It consists of the PCSA, CMOS logic tree, and write circuits. Two output signals SUM and C_{out} (output carry) are computed by two sub-circuits, both of which use the same structure except for the CMOS logic tree. Thereby the other parts of the sub-circuit for computing C_{out} are omitted in Figure 5.20(b). Two volatile input operands A and B are associated with the CMOS logic tree. Another non-volatile input C_i (carried in) is represented by the states of a couple of MTJs. The input patterns of $\{A, B, C_i\}$ configure the resistances of the CMOS logic tree and MTJs so that the PCSA computes SUM and C_{out} by sensing the resistance difference between the left and right branches. This operation should conform to addition logic, as

$$\begin{cases} SUM = A \oplus B \oplus C_i = ABC_i + \overline{B}A\overline{C_i} + \overline{A}B\overline{C_i} + \overline{A}C_i\overline{B} \\ C_{out} = AB + AC_i + BC_i \end{cases} \tag{5.22}$$

For SUM, the CMOS logic tree shown in Figure 5.20(a) directly follows Eq. (5.22). However, for C_{out}, the CMOS logic tree is simplified compared to Eq. (5.22), as shown in Figure 5.20(b). Corresponding resistance configuration is listed in Table 5.4. As can be seen, for the cases of $\{A, B, C_i\} =' 001'\text{and}\,'110'$, the addition logic is correctly performed only if $R_{OFF} - R_{ON} > 2(R_{AP} - R_P)$. Fortunately, that is true for the transistors and MTJs.

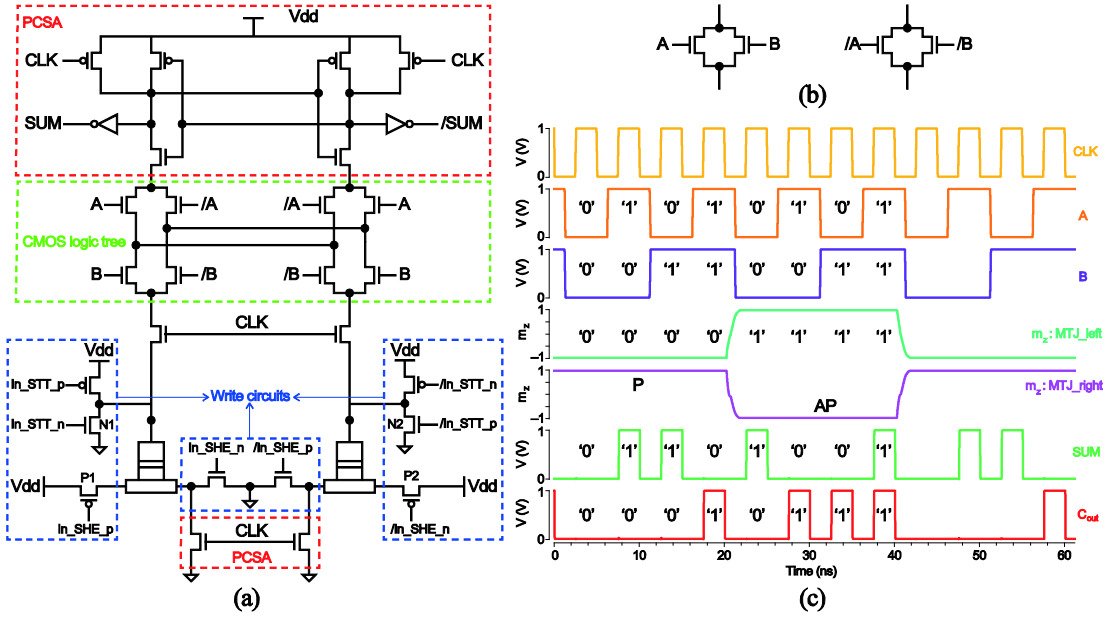


Figure 5.20 (a) Schematic of the spin-Hall-assisted MFA, (b) CMOS logic tree for C_{out}, (c) transient simulation results.

Table 5.4 Truth table and resistance configuration for C_{out}

A	B	C_i	Expected resistance comparison	C_{out}	Left branch	Right branch
0	0	0	$R_L > R_R$*	0	$R_{AP} + 0.5R_{OFF}$*	$R_P + 0.5R_{ON}$
0	0	1	$R_L > R_R$	0	$R_P + 0.5R_{OFF}$	$R_{AP} + 0.5R_{ON}$
0	1	0	$R_L > R_R$	0	$R_{AP} + \frac{R_{ON}R_{OFF}}{R_{ON}+R_{OFF}}$	$R_P + \frac{R_{ON}R_{OFF}}{R_{ON}+R_{OFF}}$
0	1	1	$R_L < R_R$	1	$R_P + \frac{R_{ON}R_{OFF}}{R_{ON}+R_{OFF}}$	$R_{AP} + \frac{R_{ON}R_{OFF}}{R_{ON}+R_{OFF}}$
1	0	0	$R_L > R_R$	0	$R_{AP} + \frac{R_{ON}R_{OFF}}{R_{ON}+R_{OFF}}$	$R_P + \frac{R_{ON}R_{OFF}}{R_{ON}+R_{OFF}}$
1	0	1	$R_L < R_R$	1	$R_P + \frac{R_{ON}R_{OFF}}{R_{ON}+R_{OFF}}$	$R_{AP} + \frac{R_{ON}R_{OFF}}{R_{ON}+R_{OFF}}$
1	1	0	$R_L < R_R$	1	$R_{AP} + 0.5R_{ON}$	$R_P + 0.5R_{OFF}$
1	1	1	$R_L < R_R$	1	$R_P + 0.5R_{ON}$	$R_{AP} + 0.5R_{OFF}$

* $R_{L,R}$ means the resistances of the left and right branches. $R_{P,AP}$ means the MTJ resistances corresponding to P and AP states. $R_{ON,OFF}$ means the transistor resistances corresponding to the activated and deactivated states. Here the resistance of the heavy metal is not taken into account.

Complete computing process of the proposed MFA was validated by the simulation results in Figure 5.20(c). Here the transistors in the write circuits were set to 210 nm/80 nm. The other parameters were configured as Section 5.3.2. During 20~22.5 ns or 40~42.5 ns, the input C_i is inverted by switching a couple of MTJs. The write signals are generated by the write driver shown in Figure 5.16. But the signals 'In_STT_n' and '/In_STT_p' need to be delayed to ensure that the transistors N1 and N2 are deactivated later than P1 and P2 when the write operation is finished. From the simulation results, we confirm that the magnetization switching is triggered without the incubation delay, in agreement with the characteristic of the spin-Hall-assisted STT switching.

Since the write operation of the proposed MFA is nearly identical to that of the above MFF, the same conclusion can be drawn and therefore the related analysis is omitted here.

5.5 Conclusion

The conventional STT suffers from two mainly bottlenecks: on one hand, the incubation delay limits the switching speed; on the other hand, to achieve faster switching, the write current needs to be strengthened, resulting in an increasing risk of barrier breakdown. In order to overcome these bottlenecks, this chapter is devoted to the study of a new magnetization switching mechanism, which is called spin-Hall-assisted STT switching.

First, we performed the numerical simulation to analyze the magnetization dynamics based on a modified LLG equation including STT and SHT. We found that a single SHT cannot achieve deterministic switching of the perpendicular magnetization. By combining the STT with SHT, deterministic switching can occur, but two types of switching behaviors are demonstrated. If the SHE write current density is smaller than a critical value, the switching process is still governed by the conventional STT. If larger, the SHT plays a more dominant role in the magnetization switching, as a result, the incubation delay is eliminated and an ultrafast switching is achieved.

Afterwards, we analyzed the influences of the duration and direction of the SHE write current on the magnetization dynamics. It was demonstrated that the SHE write current should be removed at an appropriate time because it cannot efficiently assist the magnetization switching during the later stage. The direction of the SHE write current makes no deterministic contribution to the switching because its inversion is just equivalent to a shift of π in the initial azimuthal angle.

Also the influences of the field-like torques were studied. The field-like STT has little impact on the magnetization dynamics, but the role of field-like SHT is relative significant and complicated, which deserves more research effort.

Based on the above simulation study, we further explored the application of the spin-Hall-assisted STT switching in the magnetic circuits. For that, we developed a compact electrical model

of the three-terminal p-MTJ with *Verilog-A* language and validated its function by single-cell simulation. By using the developed model and *STMicroelectronics* CMOS 28nm design kit, we designed and simulated an MFF array and an MFA with spin-Hall assistance. A conventional STT MFF was also presented for the sake of comparison. Simulation results demonstrated that, under the same operation frequency, spin-Hall-assisted STT switching can improve the cell area and energy dissipation while reduces the write voltage across the MTJ. But the improvement in the cell area and energy dissipation is weakened and even vanishes with the MTJ scaling. We explained these results with related theoretical models.

Chapter 6

Conclusions and perspectives

General conclusions

This thesis is devoted to the compact modeling and circuit design based on the FTJ and spin-Hall-assisted STT. Through our work, two goals are met: one is that the FTJ research is extended from the physical field to the circuit-level application; the other one is that the principle, performance and application of the spin-Hall-assisted STT have been discussed and studied by simulation.

We started with a state-of-the-art, which reviews the history and recent progress of FTJs and MTJs. Based on our investigation, currently the FTJ research is mainly focused on the fabrication and optimization of the nanopillar. This encouraged us to explore the circuit-level application of the FTJs. As for the MTJ, SOT is attracting much research interest since it promises to overcome the bottlenecks of the conventional STT such as the incubation delay and high write voltage. However, to switch a p-MTJ, SOT has to function together with an external magnetic field, which weakens its applicability. For solving this problem, we focused on the study of a pure-electric magnetization switching mechanism called spin-Hall-assisted STT.

Afterwards, a compact electrical model of the FTJ was developed with *Verilog-A* language based on related physical theories and experimental results. To the best of our knowledge, this is the first FTJ electrical model. This model mainly includes three sub-models: the tunneling resistance model (*Gruverman* model and FNT model) for describing I-V characteristic, the dynamic switching model (KAI model) for the calculation of the switching speed, and the memristive model for determining the time-dependent memristance. Each sub-model shows a good agreement with the experimental results. Single-cell simulation validated the function of our model and faithfully reproduced the electrical behaviors of the FTJ (e.g. a series of pinched I-V loops were successfully simulated).

By using the developed FTJ model and *STMicroelectronics* CMOS 40 nm design kit, we designed and simulated four hybrid CMOS/FTJ circuits: an FTRAM for the NV data storage, an FTJ-based synapse array for the unsupervised STDP learning, an FTJ-based NC for the on-chip supervised learning, an FTJ-based logic block for implementing NAND and NOR logic functions.

The FTRAM was constructed based on a 2T1R cell structure where an access TG and an FTJ are connected in series. Classical 1T1R cell is not suitable for the integration between FTJs and 40 nm-technology CMOS transistor because it suffers from serious threshold-loss due to the high write voltage (3~4 V), which results in significant asymmetry between write directions. The read circuit is implemented with a PCSA. The write circuit consists of a controlling logic unit and four driving transistors. Through transient simulation and *Monte-Carlo* statistical simulation, we discussed the influences of device parameters on the read/write performance of the FTRAM. It

was demonstrated that, to optimize the FTRAM, tradeoff needs to be evaluated for each parameter. For example, decreasing the FTJ area can improve the write performance and read reliability, but it weakens the data retention, read speed and read energy.

In the FTJ-based synapse array, each synapse consists of an FTJ and an NMOS transistor. Unlike in FTRAM, 1T1R cell is feasible for the synapse design, because here the FTJ is allowed to be programed to intermediate state between ON and OFF states. Therefore the asymmetry is not an obstacle. We proposed an STDP learning scheme for this synapse array and validated its working principle with transient simulation. Simulation results were analyzed with the FTJ physical models. Our simulation and analysis revealed that the range of synaptic change is related to the initial domain configuration and device size. For instance, this range can be enlarged by decreasing the FTJ radius or widening the transistor.

The FTJ-based NC is composed of FTJ array, neurons and learning cells. It is worth mentioning that the learning cell uses a very compact structure including only four transistors, two FTJs and a CMOS inverter. Such a compact learning cell improves the integration density and can be easily extended to multilayer learning. We designed an on-chip learning scheme for the proposed NC and simulated the parallel learning of AND and OR logic functions. In addition, *Monte-Carlo* statistical simulation was performed to demonstrate the fault-tolerance of the proposed FTJ-based NC against the size variation and stuck defect. It was found that the proposed NC is more sensitive to the stuck defect, and that fault-tolerance can be enhanced by adjusting the number of learning epochs.

The design of FTJ-based logic block was inspired by the non-linear dependence of the FTJ resistance on the ferroelectric domain growth. We found that, for the case of the ON-to-OFF switching, the FTJ resistance increases slowly during the long-range initial stage of the domain growth. This mechanism enables NAND and NOR logic functions to be implemented inside a single FTJ. Such an idea was validated by the simulation of our designed compact logic block including an FTJ, a load resistor and a MOS switch. The optimization of the output margin and computing energy in the proposed logic block was discussed. An important conclusion is that the output margin can be adjusted by changing the input pulse amplitude. Two optimum amplitudes for NAND and NOR logic functions were determined.

Then, we studied perpendicular-magnetization dynamics driven by SHE and STT through the numerical simulation of a modified LLG equation. It was demonstrated that a single SHE write current cannot deterministically switch the perpendicular magnetization. The combination of STT and SHE write currents gives two types of switching behaviors depending on the magnitude of the SHE write current density. If the SHE write current density is smaller than a critical value, the

magnetization dynamics is similar to the conventional STT switching. If larger, the magnetization dynamics is dominated by SHT and hence an ultrafast switching can be achieved without the incubation delay. However, after the magnetization passes the in-plane direction (which is the critical point for the switching), SHT hinders the magnetization switching towards the anisotropy axis. A better solution is to remove the SHE write current at an appropriate time in order to achieve the remaining switching process with the STT. Such a novel switching approach is called spin-Hall-assisted STT. We also found that the field-like STT and the direction of the SHE write current has little impact on the spin-Hall-assisted STT switching, but the influence of field-like SHT is significant and complicated, which needs more research efforts.

Finally we applied the spin-Hall-assisted STT switching to the write operation of an MFF array and a 1-bit MFA. An electrical model of three-terminal p-MTJ was developed for the circuit design and simulation. Simulation results demonstrated that, if the MTJ size is large (> 40 nm), the spin-Hall-assisted MFF can achieve smaller cell area and lower energy dissipation than the conventional STT MFF at the same operation frequency. But for the small-size MTJ, this improvement vanishes. The reason is that the critical SHE write current increases with the MTJ scaling. Nevertheless, we noted that the write voltage across the MTJ of the spin-Hall-assisted MFF is smaller than the conventional STT MFF regardless of the MTJ size, which decreases the risk of barrier breakdown. These conclusions are also applicable to the 1-bit MFA.

Perspectives

This thesis has developed compact electrical models of the FTJ and spin-Hall-assisted MTJ, explored related circuit-level applications, and presented some useful simulation results. But it is not the end of the story. Here we propose some points which can further improve our work.

In the high-voltage regime, the I-V characteristic of the FTJ was not well-studied, and also experimental data for the model fit is not sufficient. Our model follows the viewpoint of Ref. [171] that the tunneling in high voltage is governed by FNT. But in order to fit a few experimental results, we introduced two factors into FNT equation (Eq. (3.9)). This is actually a rough assumption. Recently, Ref. [72] proposed to use a combination of DT and FNT to describe the I-V characteristic of the FTJ, which may be a good solution.

With regard to FTRAM, the integration between FTJ and nanoscale CMOS technology is hindered by high write voltage. The access transistors need to be large enough to provide sufficient write voltage, which limits the storage density. An alternative design is to use cross-point architecture, where a driving transistor can be shared by multiple cells and thus the storage density can be improved [144]. Another solution is to develop multilevel memory [236], where an FTJ can

be programed to intermediate state and store multi-bit data. In this way, the write voltage can be efficiently decreased.

As for the spin-Hall-assisted MFF, the energy improvement over the conventional STT MFF is limited. One reason is that the STT write current is partly consumed by half of the heavy metal in the spin-Hall-assisted MFF. As a result, the spin-Hall assistance is partly offset by the decreasing STT write current. An optimized circuit design is desired to resolve this problem. Otherwise, a more promising switching mechanism needs to be developed.

In this thesis, the electronic application based on FE polarization and FM magnetization was separately studied. Actually, the combination of these two ferroic orders has become an emerging and promising topic. Especially, polarization-controlled magnetism has been attracting intensive research interests. For instance, the barrier of an MTJ can be replaced with a ferroelectric material (forming an FM/FE/FM structure) so that TMR effect can be modulated through the polarization reversal [237]–[238]. In addition, magneto-electric coupling in multiferroic materials were also used for mediating the magnetism in the tunnel junction and multiferroic/FM heterostructure [239]–[240]. Recently, it was experimentally demonstrated that the magnetic anisotropy can be adjusted by the strain from the ferroelectric material [241]. These effects are induced by an electric field rather than a current, thus it promises to decrease the energy dissipation of the magnetic device. Exploring the circuit-level application of these effects may be an extension of our work.

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Appendix A:

Source code of the FTJ electrical model

```
`resetall
`include "constants.vams"
`include "disciplines.vams"

/*---------------------- Electrical Constants ----------------------*/

`define e 1.6e-19       //Elementary charge
`define kB 1.38e-23     //Boltzmann constant
`define hbas 1.054e-34  //Reduced Planck constant
`define m 9.11e-31      //Vacuum electron mass
`define E0 1.0e9        //Characteristic field in V/m
`define PI 3.141592653

/*------------------------------ End ------------------------------*/

module BTOFTJ(T1,T2,s);

inout T1,T2;            //Real pins of the FTJ
output s;               //Virtual pin outputting the volume fraction of
                        the OFF-state domain
electrical T1,T2,s;

/*---------------------- Technology Parameters ----------------------*/

parameter real PhiH_1 = 0.678;      //Barrier potential height in volt at
                                    LSMO/BTO interface, OFF state
parameter real PhiH_2 = 0.978;      //Barrier potential height in volt at
                                    Co/BTO interface, OFF state
parameter real mH_fac = 0.931;      //Coefficient of effective electron
                                    mass, OFF state
parameter real PhiL_1 = 0.530;      //Barrier potential height in volt at
                                    LSMO/BTO interface, ON state
parameter real PhiL_2 = 1.014;      //Barrier potential height in volt at
                                    Co/BTO interface, ON state
parameter real mL_fac = 0.437;      //Coefficient of effective electron
                                    mass, ON state

parameter real tau0n = 2.8e-15;     //Attempt time of domain nucleation
                                    in second
parameter real tau0p = 9e-14;       //Attempt time of domain wall
                                    propagation in second
parameter real Un = 0.67;           //Creep energy barrier in volt for
                                    domain nucleation
parameter real Up = 0.52;           //Creep energy barrier in volt for
                                    domain wall propagation

/*------------------------------ End ------------------------------*/

/*------------------------ Size Parameters ------------------------*/
```

```
parameter real r = 175e-9;                              //Surface radius in
                                                        meter
parameter real t_B = 2e-9 from [1.2e-9:2.4e-9];         //Barrier thickness
                                                        in meter

/*------------------------------- End --------------------------------*/

/*---------------------- Simulation Parameters ----------------------*/

parameter real sim_step = 1e-10;                        //Time step in second for
                                                        simulation
parameter real s_OFF = 0.9 from (0:1);                  //Initial volume fraction
                                                        of the down-polarized
                                                        domain
parameter real T = 300;                                 //Temperature

/*------------------------------- End --------------------------------*/

/*---------------------------- Variables ----------------------------*/

real area;              //Surface area of junction

real FH1_pos;           //Fitting factor for FN tunneling, positive bias,
                        OFF state
real FH2_pos;           //Fitting factor for FN tunneling, positive bias,
                        OFF state
real FH1_neg;           //Fitting factor for FN tunneling, negative bias,
                        OFF state
real FH2_neg;           //Fitting factor for FN tunneling, negative bias,
                        OFF state
real FL1_pos;           //Fitting factor for FN tunneling, positive bias,
                        ON state
real FL2_pos;           //Fitting factor for FN tunneling, positive bias,
                        ON state
real FL1_neg;           //Fitting factor for FN tunneling, negative bias,
                        ON state
real FL2_neg;           //Fitting factor for FN tunneling, negative bias,
                        ON state

real TransH_pos;        //Transition voltage between DT and FNT, positive
                        bias, OFF state
real TransH_neg;        //Transition voltage between DT and FNT, negative
                        bias, OFF state
real TransL_pos;        //Transition voltage between DT and FNT, positive
                        bias, ON state
real TransL_neg;        //Transition voltage between DT and FNT, negative
                        bias, ON state

real IH;                //Current for OFF state
real IL;                //Current for ON state

real FacH_C;            //Factor used in Gruverman model, OFF state
real FacH_alpha;        //Factor used in Gruverman model, OFF state
real FacL_C;            //Factor used in Gruverman model, ON state
real FacL_alpha;        //Factor used in Gruverman model, ON state

real mH;                //Effective electron mass, OFF state
```

```
real mL;                //Effective electron mass, ON state

real taun;              //Nucleation time in second
real taup;              //Characteristic propagation time in second

real Vb;                //Voltage across the FTM from T1 to T2
real Id;                //Current through the FTM from T1 to T2

real t_pre;             //Last simulation time recorded
real t_rel;             //Relative time with respect to a single KAI
                        curve

real s_OFF_real;        //Real-time volume fraction of OFF-state domain
                        during the simulation
real s_ON_real;         //Real-time volume fraction of ON-state domain
                        during the simulation

integer NucleReq;       //Flag indicating whether nucleation activation
                        is required or not
                        //0, no nucleation is required; 1, nucleation is
                        required for ON-to-OFF switching
                        //-1, nucleation is required for OFF-to-ON
                        switching

real NucleStage_HL;     //Percentage of the proceeding nucleation
                        activation for OFF-to-ON switching
real NucleStage_LH;     //Percentage of the proceeding nucleation
                        activation for ON-to-OFF switching

integer Num_t_B;        //Number of the unit cell in the barrier
integer IsTrue_t_B;     //Flag indicating whether the barrier thickness
                        is reasonable or not

/*------------------------------- End -------------------------------*/

/*------------------------------ Analog -----------------------------*/
analog      begin

      //Initialization
      @(initial_step)   begin
            IsTrue_t_B = (t_B*1e10)%4;
            if(IsTrue_t_B != 0) begin
                  $strobe("Warning: Specified t_B = %g not
                  reasonable!",t_B);
                  $finish(0);
            end

            area = `PI*r*r;
            t_pre = $abstime;
            s_OFF_real = s_OFF;
            s_ON_real = 1.0 - s_OFF_real;

            TransH_pos = PhiH_2;
            TransH_neg = -PhiH_1;
            TransL_pos = PhiL_2;
            TransL_neg = -PhiL_1;
```

```
        mH = mH_fac*`m;
        mL = mL_fac*`m;

        FacH_C = -4*mH*pow(`e,3)/(9*`PI*`PI*pow(`hbas,3));
        FacL_C = -4*mL*pow(`e,3)/(9*`PI*`PI*pow(`hbas,3));

        FH2_pos = 0.7608;
        FH2_neg = 0.283;
        FL2_pos = 9.41e-2;
        FL2_neg = 1.2e-3;

        Num_t_B = (t_B*1e10)/4.0;

        case(Num_t_B)
              3: begin
                    FH1_pos = 3.739e-2;
                    FH1_neg = 3.55e-2;
                    FL1_pos = 7.211e-3;
                    FL1_neg = 1.354e-2;
              end
              4: begin
                    FH1_pos = 9.795e-3;
                    FH1_neg = 6.517e-3;
                    FL1_pos = 1.605e-3;
                    FL1_neg = 2.133e-3;
              end
              5: begin
                    FH1_pos = 2.6e-3;
                    FH1_neg = 1.2e-3;
                    FL1_pos = 3.549e-4;
                    FL1_neg = 3.273e-4;
              end
              6: begin
                    FH1_pos = 6.707e-4;
                    FH1_neg = 2.168e-4;
                    FL1_pos = 7.843e-5;
                    FL1_neg = 4.964e-5;
              end
              default: begin
                    $strobe("Warning: Specified t_B = %g not
                    reasonable!",t_B);
                    $finish(0);
              end
        endcase

        NucleStage_HL = 0;
        NucleStage_LH = 0;

end
//Initialization ends here

Vb=V(T1,T2);

if(abs(Vb+PhiH_1-PhiH_2) <= 1e-6)   begin
        Vb = PhiH_2-PhiH_1+1e-4;        //Reset the polar point to
                                        avoid zero denominator
end
```

```
if(abs(Vb+PhiL_1-PhiL_2) <= 1e-6)   begin
      Vb = PhiL_2-PhiL_1+1e-4;      //Reset the polar point to
                                    avoid zero denominator
end

FacH_alpha = 4*t_B*sqrt(2*mH*`e)/(3*`hbas*(PhiH_1+Vb-PhiH_2));
FacL_alpha = 4*t_B*sqrt(2*mL*`e)/(3*`hbas*(PhiL_1+Vb-PhiL_2));

//Calculate the current for OFF state
if(Vb > TransH_neg && Vb < TransH_pos)    begin
            //Direct tunneling occurs
            IH = area*FacH_C*limexp(FacH_alpha*(pow((PhiH_2-
            0.5*Vb),1.5) -
            pow((PhiH_1+0.5*Vb),1.5)))*(sinh(0.75*FacH_alpha*Vb*(po
            w((PhiH_2-0.5*Vb),0.5) -
            pow((PhiH_1+0.5*Vb),0.5))))/(FacH_alpha*FacH_alpha*pow(
            (pow((PhiH_2-0.5*Vb),0.5) -
            pow((PhiH_1+0.5*Vb),0.5)),2));
      end
else if(Vb >= TransH_pos)     begin       //FN tunneling occurs
            IH = FH1_pos*area*`e*`e*`m*Vb*Vb*limexp(-
            FH2_pos*4*t_B*sqrt(2*mH*`e)*pow(PhiH_1,1.5)/(3*`hbas*ab
            s(Vb)))/(16*`PI*`PI*`hbas*mH*PhiH_1*t_B*t_B);
      end
else if(Vb <= TransH_neg)     begin       //FN tunneling occurs
            IH = -(FH1_neg*area*`e*`e*`m*Vb*Vb*limexp(-
            FH2_neg*4*t_B*sqrt(2*mH*`e)*pow(PhiH_2,1.5)/(3*`hbas*ab
            s(Vb)))/(16*`PI*`PI*`hbas*mH*PhiH_2*t_B*t_B));
end

//Calculate the current for ON state
if(Vb > TransL_neg && Vb < TransL_pos)    begin
            //Direct tunneling occurs
            IL = area*FacL_C*limexp(FacL_alpha*(pow((PhiL_2-
            0.5*Vb),1.5) -
            pow((PhiL_1+0.5*Vb),1.5)))*(sinh(0.75*FacL_alpha*Vb*(po
            w((PhiL_2-0.5*Vb),0.5) -
            pow((PhiL_1+0.5*Vb),0.5))))/(FacL_alpha*FacL_alpha*pow(
            (pow((PhiL_2-0.5*Vb),0.5) -
            pow((PhiL_1+0.5*Vb),0.5)),2));
      end
else if(Vb >= TransL_pos)     begin       //FN tunneling occurs
            IL = FL1_pos*area*`e*`e*`m*Vb*Vb*limexp(-
            FL2_pos*4*t_B*sqrt(2*mL*`e)*pow(PhiL_1,1.5)/(3*`hbas*ab
            s(Vb)))/(16*`PI*`PI*`hbas*mL*PhiL_1*t_B*t_B);
      end
else if(Vb <= TransL_neg)     begin       //FN tunneling occurs
            IL = -(FL1_neg*area*`e*`e*`m*Vb*Vb*limexp(-
            FL2_neg*4*t_B*sqrt(2*mL*`e)*pow(PhiL_2,1.5)/(3*`hbas*ab
            s(Vb)))/(16*`PI*`PI*`hbas*mL*PhiL_2*t_B*t_B));
end

//Check if nucleation is required
if(Vb > 0) begin
      if(s_OFF_real < 1e-4 && NucleStage_LH < 1) begin
```

```
            //require nucleation process while switching toward OFF
            state
            NucleReq = 1;
            NucleStage_HL = 0;
      end
      else if(s_OFF_real < 1e-4 && NucleStage_LH >= 1) begin
            //nucleation is finished, but sOFF is still smaller
            than critical value
            NucleReq = 0;
            NucleStage_LH = 0;
            NucleStage_HL = 0;
            s_OFF_real = 1e-4;
      end
      else begin
            //no nucleation process is required
            NucleReq = 0;
            NucleStage_LH = 0;
            NucleStage_HL = 0;
      end
end

if(Vb < 0) begin
      if(s_ON_real < 1e-4 && NucleStage_HL < 1) begin
            //require nucleation process while switching toward ON
            state
            NucleReq = -1;
            NucleStage_LH = 0;
      end
      else if(s_ON_real < 1e-4 && NucleStage_HL >= 1) begin
            //nucleation is finished, but sON is still smaller than
            critical value
            NucleReq = 0;
            NucleStage_LH = 0;
            NucleStage_HL = 0;
            s_ON_real = 1e-4;
      end
      else begin
            //no nucleation process is required
            NucleReq = 0;
            NucleStage_LH = 0;
            NucleStage_HL = 0;
      end
end

//Case 1: Positive bias voltage, trigger the nucleation of OFF-
state domain
if(Vb > 0 && NucleReq == 1)   begin
      taun = tau0n*limexp(t_B*Un*`e*`E0/(`kB*T*abs(Vb)));
      NucleStage_LH = NucleStage_LH + ($abstime - t_pre)/taun;
      t_pre = $abstime;
end

//Case 2: Negative bias voltage, trigger the nucleation of ON-
state domain
if(Vb < 0 && NucleReq == -1)  begin
taun = tau0n*limexp(t_B*Un*`e*`E0/(`kB*T*abs(Vb)));
NucleStage_HL = NucleStage_HL + ($abstime - t_pre)/taun;
```

```
            t_pre = $abstime;
        end

        //Case 3: Positive bias voltage, Drive the down-polarized domain
        wall propagation
        if(Vb > 0 && NucleReq == 0)   begin
            taup = tau0p*limexp(t_B*Up*`e*`E0/(`kB*T*abs(Vb)));
            t_rel = taup*sqrt(ln(1/(1-s_OFF_real)));
            s_OFF_real = 1 - limexp(-pow((t_rel + $abstime -
            t_pre)/taup,2));
            s_ON_real = 1 - s_OFF_real;
            t_pre = $abstime;
        end

        //Case 4: Negative bias voltage, Drive the up-polarized domain
        wall propagation
        if(Vb < 0 && NucleReq == 0)   begin
            taup = tau0p*limexp(t_B*Up*`e*`E0/(`kB*T*abs(Vb)));
            t_rel = taup*sqrt(ln(1/(1-s_ON_real)));
            s_ON_real = 1 - limexp(-pow((t_rel + $abstime -
            t_pre)/taup,2));
            s_OFF_real = 1 - s_ON_real;
            t_pre = $abstime;
        end

        //Results
        Id = IH*s_OFF_real + IL*s_ON_real;
        I(T1,T2)<+(Id);
        V(s)<+(s_OFF_real);

        //Set the time step
        $bound_step(sim_step);

end

/*------------------------------- End --------------------------------*/

endmodule
```

Appendix B:

Source code of the spin-Hall-assisted STT MTJ electrical model

```
`resetall
`include "constants.vams"
`include "disciplines.vams"

//MTJ Shape definition
`define rec 1
`define ellip 2
`define circle 3

/*---------------------- Electrical Constants ----------------------*/

`define e 1.6e-19       //Elementary charge
`define m 9.11e-31      //Electron mass
`define uB 9.274e-24    //Bohr Magneton
`define u0 1.256637e-6  //Vacuum permeability
`define hbas 1.0545e-34 //Reduced Planck constant
`define kB 1.38e-23     //Boltzmann constant

/*------------------------------- End -------------------------------*/

module model(T1,T2,T3,Tmz,Tx);

inout T1,T2,T3;
electrical T1,T2,T3;    //Real terminals

output Tmz;
electrical Tmz;         //Virtual terminal outputting the magnetization

output Tx;
electrical Tx;          //Virtual terminal outputting the potential of
                        the node amongst T1~T3 (Optional function)


/*---------------------- Technology parameters ----------------------*/

parameter real  alpha = 0.03; //Gilbert damping constant
parameter real  TMR = 1.2;    //TMR ratio under zero bias voltage
parameter real  eta = 0.3;    //Spin Hall angle

parameter real  Hk = 8e4;     //Perpendicular Magnetic Anisotropy in A/m
parameter real  Ms = 8.8e5;   //Saturation Field in the Free Layer in A/m
parameter real  PhiBas = 0.4; //MgO barrier potential height in volt
parameter real  Vh = 0.5;     //Voltage bias when the TMR(real) is
                              1/2TMR(0) in Volt

/*------------------------------- End -------------------------------*/

/*------------------------- Size parameters -------------------------*/

parameter integer  SHAPE = 1  from[1:3];            //MTJ Surface shape
```

```
parameter real  tsl = 0.7e-9 from[0.5e-9:1.5e-9];     //Free layer
                                                      thickness in meter
parameter real  a = 90.0e-9;          //MTJ Surface length in meter
parameter real  b = 90.0e-9;          //MTJ Surface width in meter
parameter real  r = 45e-9;            //MTJ Surface radius in meter
parameter real  tox = 8.5e-10 from[8e-10:15e-10];     //MgO barrier
                                                      thickness in meter

parameter real  d = 3e-9;             //Heavy-metal thickness in meter
parameter real  l = 110e-9;           //Heavy-metal Length in meter
parameter real  w = 90e-9;            //Heavy-metal Width in meter

/*------------------------------- End --------------------------------*/

/*------------------------- State parameters -------------------------*/

parameter integer PAP = 1 from[0:1];      //Initial state of the MTJ, 0 =
                                          parallel, 1 = anti-parallel
parameter real  RA = 10e-12 from[5e-12:15e-12];       //Resistance-area
                                                      product of the MTJ
                                                      in ohm-m2
parameter real  rho = 2e-6;           //Resistivity of W in ohm-m
parameter real  T = 300;              //Temperature in Kelvin
parameter real  sim_step = 1e-12;     //Simulation time step in second

/*------------------------------- End --------------------------------*/

/*---------------------------- Variables -----------------------------*/

real P;                         //Spin polarization
real FA;                        //Coefficient used in Brinkman model
real gamma;                     //GyroMagnetic Ratio
real surface;                   //MTJ surface area
real V12,V13,V23;               //Voltages across two terminals
real Rp;                        //MTJ Resistance when the relative
                                magnetization is parallel
real R_MTJ;                     //Real resistance of the MTJ
real R_W;                       //Resistance of the heavy-metal stripe
real theta,phi;                 //Angles of the magnetic moment
real delta_phi,delta_theta;     //Change in the angles
real delta_aver;                //Average root square of theta deviation
real V_MTJ;                     //Voltage across the MTJ
real ksi;                       //Coefficient used in LLG equation
real J_STT;                     //Current density for STT
real J_SHE;                     //Current density for SHE
real mz;                        //Magnetization in z direction
real E_thermal;                 //Thermal stability energy
real t_previous;                //Recording the simulation time

/*------------------------------- End --------------------------------*/

/*------------------------------ Analog ------------------------------*/
analog begin

      //Initialization
      @(initial_step)begin
            if (SHAPE == 1)
```

```
            surface = a*b;                  //SQUARE
      else if (SHAPE == 2)
            surface = `M_PI*a*b/4.0;        //ELLIPSE
      else begin
            surface = `M_PI*r*r;            //ROUND
      end

      P = sqrt(TMR/(2+TMR));
      gamma = 2*`uB/`hbas;
      ksi = gamma*`hbas/(2*`e*tsl*Ms);
      E_thermal = 0.5*`u0*Ms*Hk*tsl*surface;
      delta_aver = sqrt(2.0*`kB*T/E_thermal);

      FA = 3.3141e-7/RA;
      Rp =
      (tox/(FA*sqrt(PhiBas)*surface))*exp(2*sqrt(2*`m*`e*PhiBas)*t
      ox/`hbas);

      R_W = rho*l/(d*w);

      //Initial angles and mz
      phi = 0;
      if (PAP == 0) begin
            theta = delta_aver;
            end
      else begin
            theta = `M_PI-delta_aver;
      end
      mz = cos(theta);
      t_previous = $abstime;

end
//Initialization is finished here

//Calculation of STT and SHE write current densities
J_STT = -I(T1,Tx)/surface;
if (V(T2) > V(T3))
      J_SHE = min(abs(I(T2,Tx)),abs(I(Tx,T3)))/(w*d);
else if (V(T2) < V(T3))
      J_SHE = -min(abs(I(T3,Tx)),abs(I(Tx,T2)))/(w*d);
else begin
      J_SHE = 0;
end

//Solving LLG equation including STT torque and SHE torque
if (analysis("tran")) begin
      delta_phi = ($abstime-
      t_previous)*(1.0/(1+alpha*alpha))*(gamma*`u0*Hk*cos(theta)-
      alpha*ksi*P*J_STT-ksi*eta*J_SHE*(alpha*cos(theta)*cos(phi)-
      sin(phi))/sin(theta));

      delta_theta = ($abstime-t_previous)*(1.0/(1+alpha*alpha))*(-
      alpha*gamma*`u0*Hk*cos(theta)*sin(theta) -
      ksi*P*J_STT*sin(theta) -
      ksi*eta*J_SHE*(alpha*sin(phi)+cos(theta)*cos(phi)));
      phi = phi + delta_phi;
```

```
            theta = theta + delta_theta;
            t_previous = $abstime;
            $bound_step(sim_step);
      end

      //Limit the theta under the thermal fluctuation
      if(theta > `M_PI-delta_aver)
            theta = `M_PI - delta_aver;
      else if (theta < delta_aver)
            theta = delta_aver;

      //Output mz
      mz = cos(theta);
      V(Tmz)<+mz;

      //Renew the current
      V(Tx)<+(0.5*V(T1)*R_W+(Rp*(1+(V(T1)-V(Tx))*(V(T1)-
      V(Tx))/(Vh*Vh)+TMR)/(1+(V(T1)-V(Tx))*(V(T1)-
      V(Tx))/(Vh*Vh)+0.5*(1+mz)*TMR))*(V(T2)+V(T3)))/(2*(Rp*(1+(V(T1)-
      V(Tx))*(V(T1)-V(Tx))/(Vh*Vh)+TMR)/(1+(V(T1)-V(Tx))*(V(T1)-
      V(Tx))/(Vh*Vh)+0.5*(1+mz)*TMR))+0.5*R_W);

      R_MTJ = Rp*(1+(V(T1)-V(Tx))*(V(T1)-V(Tx))/(Vh*Vh)+TMR)/(1+(V(T1)-
      V(Tx))*(V(T1)-V(Tx))/(Vh*Vh)+0.5*(1+mz)*TMR);

      I(T1,Tx)<+((V(T1)-V(Tx))/R_MTJ);
      I(T2,Tx)<+(2*(V(T2)-V(Tx))/R_W);
      I(T3,Tx)<+(2*(V(T3)-V(Tx))/R_W);

end

/*-------------------------------- End --------------------------------*/

endmodule
```

(Note: In this file we resolve LLG equation with Euler method, because we confirmed that the results are equally accurate as those resolved by Runge-Kutta method, as long as 'sim_step' is set to small enough. Usually, it is set to 1 ps. However, the simulation speed will be very slow due to such a small time step. In the further, this model can be improved by using a higher efficient algorithm for resolving LLG equation.)

Appendix C: List of Figures

Appendix D: List of Tables

Appendix E: List of Abbreviations

1T1R	One transistor and one resistor
2T1R	Two transistors and one resistor
4T2R	Four transistors and two resistors
AP (state)	Anti-parallel (state)
BEOL	Back-end-of-line
BL	Bit line
BTO	$BaTiO_3$
CIP	Current in the layer plane
CMOS	Complementary metal-oxide-semiconductor
CPP	Current perpendicular to the layer plane
DT	Direct tunneling
FeCap	Ferroelectric capacitor
FIMS	Field-induced magnetic switching
FL	Free layer
FM	Ferromagnetic
FNT	Fowler-Nordheim tunneling
FPGA	Field-programmable gate array
FTJ	Ferroelectric tunnel junction
FTRAM	FTJ-based random access memory
GMR	Giant magnetoresistance
HDD	Hard disk drive
i-MTJ	In-plane-anisotropy magnetic tunnel junction
I-V	Current-voltage
iSHE	Inverse spin-Hall effect

ITRS	International Technology Roadmap for Semiconductors
JKD	Janovec-Kay-Dunn
KAI	Kolmogorov-Avrami-Ishibashi
LCMO	$La_{0.5}Ca_{0.5}MnO_3$
LG	Landau-Ginzburg
LLG	Landau-Lifshitz-Gilbert
LSMO	$La_{0.7}Sr_{0.3}MnO_3$
LTD	Long-term depression
LTP	Long-term potentiation
MBE	Molecular beam epitaxy
M/FE/M	Metal/ferroelectric film/metal
MFA	Magnetic full-adder
MFF	Magnetic flip-flop
MRAM	Magnetoresistive random access memory
MTJ	Magnetic tunnel junction
Nb:STO	Nb-doped $SrTiO_3$
NC	Neural crossbar
NFM	Non-ferromagnetic
NLS	Nucleation-limited-switching
NMOS	n-channel metal-oxide-semiconductor
NVL	Non-volatile logic circuit
NVM	Non-volatile memory
OST	Orthogonal spin transfer
P (state)	Parallel (state)
PCSA	Pre-charge sensing amplifier
PMA	Perpendicular magnetic anisotropy

p-MTJ	Perpendicular-anisotropy magnetic tunnel junction
PMOS	p-channel metal-oxide-semiconductor
PZT	$Pb(Zr_{0.2}Ti_{0.8})O_3$
R.A	Resistance-area
RER	Read error rate
RL	Reference layer
RT	Room temperature
SHE	Spin-Hall effect
SHT	Spin Hall torque
SL	Source line
SoC	System-on-chip
SOT	Spin-orbit torque
STDP	Spike-timing dependent plasticity
STT	Spin-transfer torque
TAS	Thermal assisted switching
TDM	Time division multiplexing
TG	Transmission gate
TMR	Tunnel magnetoresistance
WKB	Wentzel–Kramers–Brillouin
W/L	Width/length
WL	Word line

Appendix F: List of Universal Symbols

ε_0	Vacuum permittivity
σ_s	Screening charge per unit area
$\delta_{1,2}$	Thomas-Fermi screening lengths in metals.
d	Thickness
R	Resistance
t	Time
$R_{ON,OFF}$	Resistance of the binary memory device at ON or OFF state
s_{OFF}	Volume fraction of the domain corresponding to OFF state in an FTJ
$R_{P,AP}$	Resistance of the MTJ at parallel or anti-parallel state
TMR	Tunneling magnetoresistance ratio
$\vec{m}$	Unit magnetic moment in the free layer of an MTJ
$\vec{H}_{eff}$	Effective magnetic field
$\vec{m}_r$	Unit magnetic moment in the reference layer of an MTJ
γ	Gyromagnetic ratio
μ_0	Vacuum permeability
α	Gilbert damping constant
e	Elementary charge
$\hbar$	Reduced Planck constant
t_F	Thickness of the free layer in an MTJ
M_s	Saturation magnetization
V_F	Free-layer volume in an MTJ
μ_B	Bohr magneton
H_k	Magnetic anisotropy field
$\vec{e}_{x,y,z}$	Unit vectors along X-, Y-, Z-axis in Cartesian coordinate system

η_{SH}	Spin Hall angle
$\vec{\sigma}_{SH}$	Unit spin polarization of electrons induced by spin Hall effect
m	Effective electron mass
t_B	Barrier thickness
S	Surface area of the FTJ or MTJ
$\bar{\varphi}$	Average barrier potential height
$\Delta\varphi$	Difference of the barrier potential height between two boundaries
m_e	Free electron mass
$F_{1,2}$	Fitting factors used in Fowler-Nordheim tunneling equation
P_s	Spontaneous polarization
τ_N	Domain nucleation time
τ_P	Characteristic time for the domain wall propagation
$\tau_{0N,0P}$	Attempt time for the domain nucleation or domain wall propagation
k_B	Boltzmann constant
E_c	Coercive field
$J_{SHE,STT}$	SHE and STT write current densities
(θ, φ)	Polar and azimuthal angles of the magnetic moment

Appendix G: List of Publications

Journals

[1] **Z. H. Wang**, W. S. Zhao, W. Kang, A. Bouchenak-Khelladi, Y. Zhang, J. O. Klein, D. Ravelosona, and C. Chappert, "Write operation study of Co/BTO/LSMO ferroelectric tunnel junction," *J. Appl. Phys.*, vol. 114, no. 4, pp. 044108, 2013.

[2] **Z. Wang**, W. Zhao, W. Kang, A. Bouchenak-Khelladi, Y. Zhang, Y. Zhang, J. O. Klein, D. Ravelosona, and C. Chappert, "A physics-based compact model of ferroelectric tunnel junction for memory and logic design," *J. Phys. D: Appl. Phys.*, vol. 47, no. 4, pp. 045001, 2014.

[3] **Z. Wang**, W. Zhao, W. Kang, Y. Zhang, J. O. Klein, D. Ravelosona, and C. Chappert, "Compact modelling of ferroelectric tunnel memristor and its use for neuromorphic simulation," *Appl. Phys. Lett.*, vol. 104, no. 5, pp. 053505, 2014.

[4] **Z. Wang**, W. Zhao, W. Kang, Y. Zhang, J. O. Klein, D. Ravelosona, Y. Zhang, and C. Chappert, "Nonvolatile Boolean Logic Block Based on Ferroelectric Tunnel Memristor," *IEEE Trans. Magn.*, vol. 50, no. 11, pp. 9100604, 2014.

[5] **Z. Wang**, W. Zhao, E. Deng, J. O. Klein, and C. Chappert, "Perpendicular-anisotropy magnetic tunnel junction switched by spin-Hall-assisted spin-transfer torque," *J. Phys. D: Appl. Phys.*, vol. 48, no. 6, pp. 065001, 2015.

[6] **Z. Wang**, W. Zhao, E. Deng, Y. Zhang, and J. O. Klein, "Magnetic non-volatile flip-flop with spin-Hall assistance," *Phys. Status Solidi RRL.*, vol. 9, no. 6, pp. 375–378, 2015.

[7] D. Chabi, **Z. Wang**, C. Bennett, J.-O. Klein, and W. Zhao, "Ultra High Density Memristor Neural Crossbar for On-chip Supervised Learning," *IEEE Trans. Nanotechnology*, to be published, 2015.

[8] E. Deng, **Z. Wang**, W. Zhao, J.-O. Klein, G. Prenat, and B. Dieny, "High-frequency low-power magnetic full-adder based on magnetic tunnel junction with spin-Hall assistance," *IEEE Trans. Magn.*, to be published, 2015.

[9] W. Kang, W. S. Zhao, **Z. Wang**, Y. Zhang, J.-O. Klein, Y. Zhang, C. Chappert, and D. Ravelosona, "A low-cost built-in error correction circuit design for STT-MRAM reliability improvement," *Microelectron. Reliab.*, vol. 53, no. 9, pp.1224–1229, 2013.

[10] W. Kang, W. Zhao, **Z. Wang**, Y. Zhang, J.-O. Klein, C. Chappert, and D. Ravelosona, "DFSTT-MRAM: Dual Functional STT-MRAM Cell Structure for Reliability Enhancement and 3D MLC Functionality," *IEEE Trans. Magn.*, vol. 50, no. 6, pp. 3400207, 2014

[11] W. Kang, Z. Li, **Z. Wang**, E. Deng, J.-O. Klein, Y. Zhang, C. Chappert, D. Ravelosona, and W. Zhao, "Variation-Tolerant High-Reliability Sensing Scheme for Deep Submicrometer STT-MRAM," *IEEE Trans. Magn.*, vol. 50, no. 11, pp. 3400904, 2014.

[12] W. Kang, Y. Zhang, **Z. Wang**, J.-O. Klein, C. Chappert, D. Ravelosona, G. Wang, Y. Zhang, and W. Zhao, "Spintronics: Emerging Ultra-low power circuits and systems beyond MOS technology," *ACM J. Emer. Tech.*, vol. 12, no. 2, 2015.

[13] W. S. Zhao, J. M. Portal, W. Kang, M. Moreau, Y. Zhang, H. Aziza, J.-O. Klein, **Z. H. Wang**, D. Querlioz, D. Deleruyelle, M. Bocquet, D. Ravelosona, C. Muller, and C. Chappert, "Design and analysis of crossbar architecture based on complementary resistive switching non-volatile memory cells," *J. Parallel Distr. Com.*, vol. 74, no. 6, pp. 2484–2496, 2014.

International Conferences with publications

[1] **Z. Wang**, W. Zhao, A. Bouchenak-Khelladi, Y. Zhang, W. Lin, J. O. Klein, D. Ravelosona, and C. Chappert, "Compact Modelling for Co/BTO/LSMO Ferroelectric Tunnel Junction," in *Proc. IEEE NANO*, pp. 229–232, 2013.

[2] **Z. Wang**, W. Zhao, W. Kang, Y. Zhang, J.-O. Klein, and C. Chappert, "Ferroelectric tunnel memristor-based neuromorphic network with 1T1R crossbar architecture," in *Proc. IEEE IJCNN*, pp. 29–34, 2014.

[3] D. Chabi, **Z. Wang**, W. Zhao, and J.-O. Klein, "On-Chip Supervised Learning Rule for Ultra High Density Neural Crossbar using Memristor for Synapse and Neuron," in *Proc. IEEE/ACM NanoArch*, pp. 7–12, 2014.

[4] W. Zhao, J.-O. Klein, **Z. Wang**, Y. Zhang, N. Ben-Romhane, D. Querlioz, D. Ravelosona, and C. Chappert, "Spin-electronics based logic fabrics," in *Proc. IEIP/IEEE VLSI-SoC*, pp. 174–179, 2013.

[5] W. Kang, W. Zhao, **Z. Wang**, J.-O. Klein, Y. Zhang, D. Chabi, Y. Zhang, D. Ravelosona, and C. Chappert, "An overview of spin-based integrated circuits," in *Proc. ASP-DAC*, pp. 676–683, 2014.

[6] E. Deng, Y. Wang, **Z. Wang**, J.-O. Klein, B. Dieny, G. Prenat, and W. Zhao, "Robust Magnetic Full-Adder with Voltage Sensing 2T/2MTJ Cell," in *Proc. IEEE/ACM NanoArch*, pp. 27–32, 2015.

[7] N. Ben-Romdhane, W. S. Zhao, Y. Zhang, J.-O. Klein, **Z. H. Wang**, and D. Ravelosona, "Design and analysis of Racetrack memory based on magnetic domain wall motion in nanowires," in *Proc. IEEE/ACM NanoArch*, pp. 71–76, 2014.

Other conferences, workshops and summer schools

[1] "Memristors for computing (MemCo)" Workshop, Fréjus, France, 2012.

[2] IEEE Magnetics Society Summer School, Assisi, Italy, 2013.

[3] IEEE International Magnetics Conference (INTERMAG), Dresden, Germany, 2014.

[4] Journées Nationales du Réseau Doctoral en Microélectronique (JNRDM), Lille, France, 2014.

[5] Introductory course on Magnetic Random Access Memory (InMRAM), Grenoble, France, 2014.

[6] IEEE International Magnetics Conference (INTERMAG), Beijing, China, 2015.

Appendix H : Synthèse en Français

Chapitre 1 Introduction générale

Avec la réduction des dimensions dans la technologie métal-oxyde-semi-conducteur complémentaire (CMOS), la puissance statique consommée par les circuits intégrés croît considérablement, conséquence de l'augmentation du courant de fuite des transistors [1]–[2]. Les mémoires non-volatiles (MNV) apportent une solution à ce problème, car elles peuvent conserver leurs données, même en l'absence d'alimentation. Dans ce contexte, la présente thèse aborde plus spécifiquement l'étude de deux technologies de MNV: les jonctions tunnel ferroélectriques (JTF) et les jonctions tunnel magnétiques (JTM).

Bien que le concept de JTF ait été proposé au début de l'année 1971 [5], sa réalisation physique n'a pas été effective avant les années 2000 [6]–[10]. Après des décennies de développement, la JTF a été répertorié comme l'un des « dispositifs émergents» dans le rapport de l'ITRS en 2011 [11]. Cependant, actuellement la recherche sur la JTF est toujours axée sur l'amélioration de la performance du seul nanopilier. Il y a eu peu d'applications aboutissant à un circuit démontrée jusqu'ici. Par conséquent, nous visons à développer un modèle électrique pour la JTF et à explorer ses applications potentielles dans les mémoires et circuits logiques non-volatiles.

Le concept de la JTM remonte à 1975, lorsque *Jullière* a montré l'effet de magnétorésistance tunnel (TMR) à basse température (4,2 K) [20] pour la première fois. Beaucoup de progrès ont été accomplis depuis la première fois que l'effet de TMR a été démontré à température ambiante en 1995 [22]–[23]. Pourtant, l'émergence de la technologie d'écriture de la JTM reste conditionnée à de nouvelles percées. Actuellement, l'approche générale d'écriture pour la JTM est le transfert de spin (TS) [27]–[29], qui souffre d'un délai d'incubation important et un risque élevé de rupture de la barrière tunnel. Pour surmonter ces difficultés, nous avons étudié une approche d'écriture appelée « TS assisté par effet Hall de spin (EHS) » [34] du point de vue de la dynamique d'aimantation et de la conception de circuits.

Nos objectifs ont été atteints par la simulation reposant sur les outils de conception assistée par ordinateur (CAO). Les modèles électriques de la JTF et JTM ont été décrits en langue *Verilog-A* [35]. Pour la JTF, les résultats expérimentaux utilisés pour l'ajustement du modèle ont été extraits de la littérature. Pour la JTM, la dynamique d'aimantation sous 'TS assisté par EHS' a été simulée numériquement avec une équation modifiée de Landau-Lifshitz-Gilbert (LLG). Les circuits hybrides de CMOS/JTF et CMOS/JTM ont été conçus sur la plate-forme *Cadence* en utilisant le design kit « *STMicroelectronics* CMOS 40 nm and 28 nm» [37]–[38] conjointement

avec les modèles développés de JTF ou JTM. La simulation des circuits a été effectuée avec le simulateur *Spectre*.

Chapitre 2 État de l'art

La structure de base d'une JTF est présentée sur la Figure S.1, où un film ultra-mince ferroélectrique est pris en sandwich entre deux métaux [3]. Le film ferroélectrique agit comme une barrière, à travers laquelle les électrons peuvent passer par effet tunnel. La barrière ferroélectrique a une polarisation spontanée qui peut être renversée par une tension externe. Le renversement de polarisation modifie la hauteur moyenne de barrière de potentiel. En conséquence, les résistances tunnels de la JTF sont différentes pour des polarisations opposées (voir Figure S.1). Il s'agit de l'effet d'électro-résistance tunnel (TER) [3], [39]–[40]. Le facteur dominant pour l'effet de TER est l'écrantage partiel des charges à l'interface asymétrique barrière/métal (voir Figure S.1).

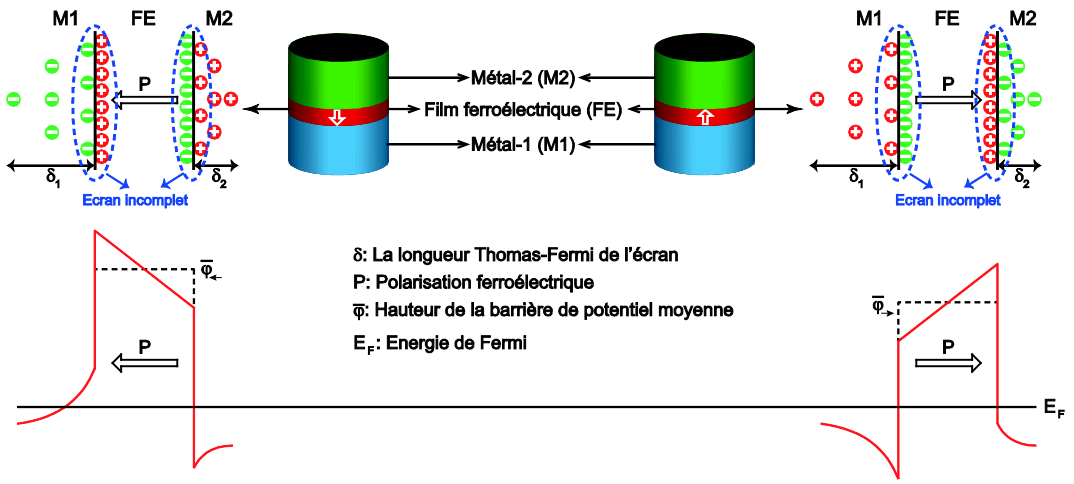

Figure S.1 Structure de base d'une JTF typique, et le profil de la barrière de potentiel pour les deux directions de polarisation.

Comme mentionné dans le Chapitre 1, la JTF a été conceptuellement proposée au début de 1971 par *L. Esaki* [5], mais n'a été physiquement fabriqué qu'en l'an 2000 [6]–[10]. Cela est dû à la difficulté de fabrication d'un film ultra-mince ferroélectrique. Dans les années 2000, des progrès techniques ont rendu possible le maintien la ferroélectricité dans un film d'une épaisseur de seulement quelques cellules unitaires [47]–[55], ce qui a facilité la démonstration expérimentale de divers JTFs [6]–[10], [12]–[15], [57]–[77].

Fait intéressant, quelques JTFs non seulement agissent comme un mémoire binaire, mais est aussi naturellement un memristor. Le memristor a été théoriquement découvert par *L. Chua* en 1971 comme un élément non-linéaire de circuit, s'ajoutant aux trois éléments linéaires de base: la

résistance, le condensateur et l'inductance [16]. Dans une définition plus large, le memristor a une résistance réglable qui dépend d'une variable d'état interne (voir Eq. (S.1)). En 2008, les scientifiques de *Hewlett-Packard* (HP) Lab ont fabriqué le premier memristor passive [18], qui présente un effet memristif en modifiant la largeur de la zone dopée dans un film semi-conducteur. L'effet memristif de JTFs provient du renversement de polarisation ferroélectrique [12]–[15], [65]. Il est expérimentalement démontré qu'il s'agit d' un processus dynamique, y compris la nucléation de domaine et la propagation de paroi de domaine [45], [80]–[82], comme l'illustre la Figure S.2. Suivant ce principe, nous pouvons définir la JTF comme un memristor commandé en tension avec une variable de l'état commandée en polarisation. L'effet memristif permet à la JTF d'être utilisée comme une synapse dans un système neuromorphique [19]. Cette opportunité incite à pousser la recherche sur les réseaux neuronaux basés sur des memristors.

$$\begin{cases} v(t) = R\left[w(t), i\right] i(t) \\ \dfrac{\mathrm{d}w(t)}{\mathrm{d}t} = f\left(w, i\right) \end{cases} \quad \text{ou} \quad \begin{cases} v(t) = R\left[w(t), v\right] i(t) \\ \dfrac{\mathrm{d}w(t)}{\mathrm{d}t} = f\left(w, v\right) \end{cases} \tag{S.1}$$

où deux équations correspond aux memristors commandés en courant et en tension. $\{v, R, I, w\}$ sont la tension, la résistance, le courant, et le variable d'état. $f(\cdot)$ est une fonction relative à système.

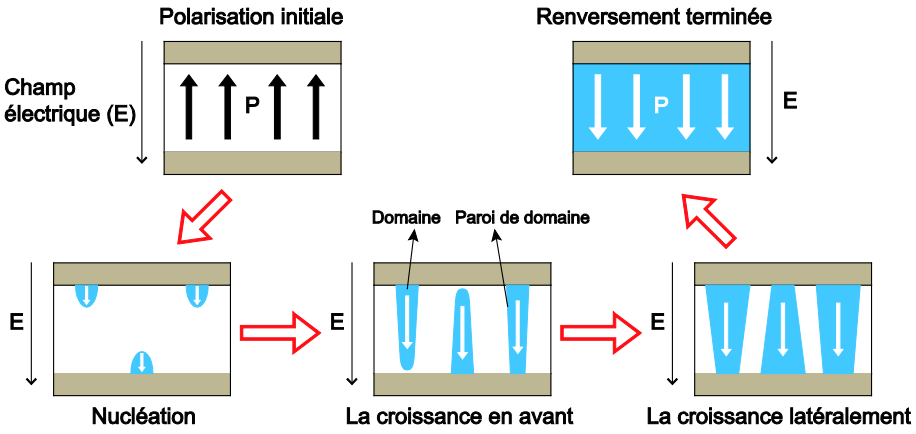

Figure S.2 Le renversement de la polarisation sous un champ électrique externe

La structure de base d'une JTM est composée d'une barrière isolante prise en sandwich entre deux couches ferromagnétiques (FM), comme présenté sur la Figure S.3 [20]. Pour les applications électroniques, une couche FM a son aimantation fixée tandis que l'autre peut basculer. Ces couches sont nommés respectivement la couche de référence (CR) et la couche libre (CL),. L'aimantation de la CL peut être commutée entre les configurations parallèle (P) ou anti-parallèle

(AP) à l'aimantation de la CR, ce qui donne une résistance tunnel faible ou élevée. Ceci est ce qu'on appelle l'effet de TMR. L'effet tunnel dépendant du spin est le principal mécanisme pour l'effet de TMR (voir Figure S.3) [21], [83].

Depuis que *Jullière* a rapporté l'effet TMR pour la première fois en 1975 [20], de nombreux progrès ont été réalisés au cours du développement de JTM. Le présent travail se concentre sur l'amélioration de la méthode d'écriture. Actuellement, le TS [27]–[29] est considéré comme une approche prometteuse d'écriture par rapport à la commutation traditionnellement induite par un champ magnétique (FIMS) [101]–[102] ou la commutation assistée thermiquement (TAS) [103]. Le TS est produit dans une JTM quand un courant polarisé en spin par la CR transfère son moment angulaire transversal à la CL (voir Figure S.4). Ce mécanisme de commutation a été théoriquement proposé par *Berger* et *Slonczewski* en 1996 [27]–[28], et a été démontré expérimentalement dans les années 2000 [105]–[108]. Aujourd'hui, le TS est devenue la technologie générale d'écriture pour la JTM.

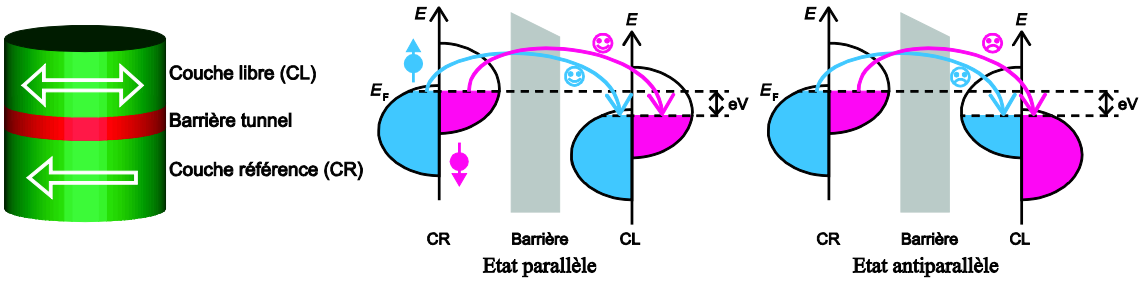

Figure S.3 La structure de base d'une JTM typique, et le schéma de l'effet de tunnel dépendant du spin.

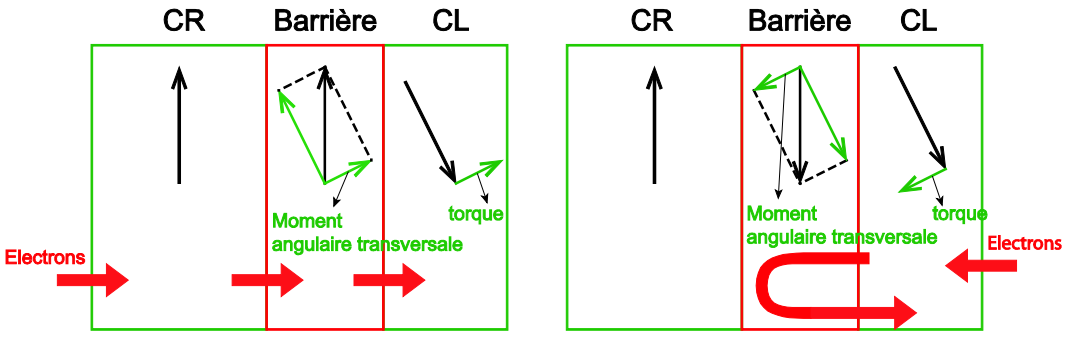

Figure S.4 Principe de transfer de spin.

Néanmoins, deux problèmes subsistent qui limitent la performance de TS. Tout d'abord, le TS a requière un délai d'incubation pénalisant la vitesse. Deuxièmement, pour une commutation plus rapide, le courant d'écriture doit être plus grand, ce qui augmente le risque de claquage de la barrière. Récemment l'interaction spin-orbite (en anglais: spin-orbit torque, SOT) a été étudiée

pour résoudre ces problèmes [30]–[33], [125]–[131] (voir Figure S.5). L'origine du SOT fait encore débat, entre l'effet Rashba [30]–[31], l'EHS [32]–[33], [127]–[130] ou les deux [126]. Dans les expériences publiées, le SOT a été produit par un courant électrique qui passe une bande de métal lourd. Le claquage de la barrière peut être évité puisque aucune circulation de courant n'a lieu à travers la JTM. Toutefois, pour la JTM à une anisotropie perpendiculaire (p-JTM), il faut que le SOT fonctionne avec un champ magnétique supplémentaire (voir Figure S.5 (a) et (c)). Pour la JTM à une anisotropie planaire (i-JTM), l'utilisation du champ magnétique est évité (voir Figure S.5 (b)), mais la stabilité thermique et la vitesse de commutation sont inférieures à celles de la p-JTM. Afin de résoudre ce dilemme, nous allons étudier une commutation rapide purement électrique de l'aimantation. Elle est appelé TS par EHS [34] dans le Chapitre 5.

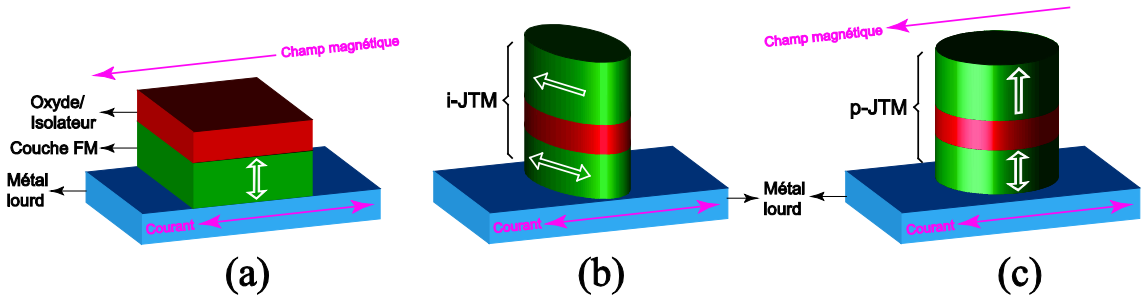

Figure S.5 Trois géométries de dispositifs utilisés dans les expériences de renversement de l'aimantation induite par SOT.

Au niveau du circuit, jusqu'à présent, la JTF n'a guère été appliquée à la conception de circuit ou système puisque la recherche actuelle est toujours centrée sur l'optimisation du nanopilier JTF. En revanche, la mémoire vive magnétorésistif (MRAM) et les circuits logiques magnétiques intégrés avec la JTM ont fait des progrès significatifs. Pour la MRAM, divers démonstrateurs ont été fabriqués au cours de la dernière décennie avec des progrès importants. Quelques produits commerciaux ont même été lancés (par exemple, 4-Mbit MRAM par *Freescale*, 16-Mbit MRAM par *EverSpin*). Les circuits logiques magnétiques sont destinés à réaliser les architectures intriquant la logique et la mémoire [161]. Quelques prototypes tels que des bascules magnétiques (MFF) [162]–[165] et additionneurs complets magnétiques (MFA) [166] ont été démontrés.

Chapitre 3 Modélisation compacte de la JTF

Afin de concevoir et analyser des circuits hydrides de CMOS/JTF, nous avons développé un modèle électrique pour la JTF rapporté par Réfs. [10] et [12]. Ce modèle comprend trois sous-modèles comme suit.

Tout d'abord, le modèle de résistance tunnel a été proposé pour décrire la caractéristique courant-tension (I-V) de la JTF. Dans le régime à basse tension, les électrons circulent à travers la barrière par effet tunnel direct (TD). Un modèle physique développé par *Gruverman* [9] permet d'obtenir un bon accord avec les résultats expérimentaux de Réf. [10], comme présenté sur l'Eq. (S.2) et la Figure S.6 (a). Dans le régime à haute tension, l'effet tunnel Fowler-Nordheim (TFN) est considéré comme le mécanisme dominant pour le transport électronique [4], [58], [171]. Une équation TFN avec deux paramètres d'ajustement permet de bien retrouver les résultats expérimentaux de la Réf. [12], comme l'Eq. (S.3). La courbe I-V complète est présentée sur la Figure S.6 (b). Après avoir réglé les paramètres de l'Eq. (S.2), elle est fidèle à la Ref. [12]).

$$I(V) = S \cdot C \frac{\exp\left\{\alpha(V)\left[\left(\varphi_2 - \frac{V}{2}\right)^{3/2} - \left(\varphi_1 + \frac{V}{2}\right)^{3/2}\right]\right\}}{\alpha^2(V)\left[\left(\varphi_2 - \frac{V}{2}\right)^{1/2} - \left(\varphi_1 + \frac{V}{2}\right)^{1/2}\right]^2} \times \sinh\left\{\frac{3}{2}\alpha(V)\left[\left(\varphi_2 - \frac{V}{2}\right)^{1/2} - \left(\varphi_1 + \frac{V}{2}\right)^{1/2}\right]\frac{V}{2}\right\} \tag{S.2}$$

avec $C = -\frac{4me^3}{9\pi^2\hbar^3}$, $\alpha(V) = \frac{4t_B(2me)^{1/2}}{3\hbar(\varphi_1 + V - \varphi_2)}$.

$$I(V) = \mathrm{sgn}(V) \cdot F_1 \cdot S \cdot \frac{e^2 m V^2}{16\pi^2 \hbar m_{ox} \varphi_B {t_B}^2} \exp\left(-F_2 \cdot \frac{4t_B\sqrt{2m_{ox}e}{\varphi_B}^{3/2}}{3\hbar|V|}\right) \tag{S.3}$$

où S est l'aire de jonction, m ou m_{ox} est la masse effective de électron, e est la charge élémentaire, $\hbar$ est constante de Planck réduite, t_B est l'épaisseur de la barrière, φ_1 and φ_2 sont les hauteurs de barrière de potentiel à deux interfaces de barrière/métalliques. $sgn(V)$ est la fonction signe. φ_B est la barrière tunnel pour les électrons. $\varphi_B = \varphi_1$ pour $V > 0$, ou $\varphi_B = \varphi_2$ pour $V < 0$. $F_1 > 0$ et $F_2 > 0$ sont les facteurs d'ajustement.

Deuxièmement, un modèle de commutation dynamique a été développé pour étudier la vitesse de commutation. Sur la base des résultats expérimentaux de la Réf. [12], le comportement de commutation de la JTF est conforme à un modèle KAI multiple [174]. Cependant, nous l'avons réduit à un simple formule pour accroître sa compacité, dans l'Eq. (S.4). Les vitesses de nucléation de domaine et de propagation du paroi de domaine peut être calculée par la loi de Merz [80], [180]–[181] et le modèle du processus de reptation [182], comme décrit par l'Eq. (S.5).

$$\frac{\Delta P(t)}{2P_s} = h(t-\tau_N) \times \left\{ 1 - \exp\left[-\left(\frac{t-\tau_N}{\tau_P} \right)^2 \right] \right\} \tag{S.4}$$

$$\tau_{N,P} = \tau_{0N,0N} \times \exp\left(\frac{E_{aN,aP}}{V} t_B \right) = \tau_{0N,0P} \times \exp\left(\frac{U_{N,P} E_0}{k_B T} \cdot \frac{1}{V} t_B \right) \tag{S.5}$$

où ΔP est la polarisation inversée. P_s est la polarisation spontanée. $h(t)$ est la fonction de Heaviside, τ_N et τ_P sont le temps de nucléation du domaine et le temps caractéristique de propagation de la paroi de domaine, respectivement. $E_{aN,aP}$ est champ d'activation, $\tau_{0N,0P}$ est le temps d'essai. U_N et U_P sont la barrière de reptation pour la nucléation du domaine et la propagation de la paroi de domaine. E_0 est le champ caractéristique, T est la température, k_B est la constante de Boltzmann.

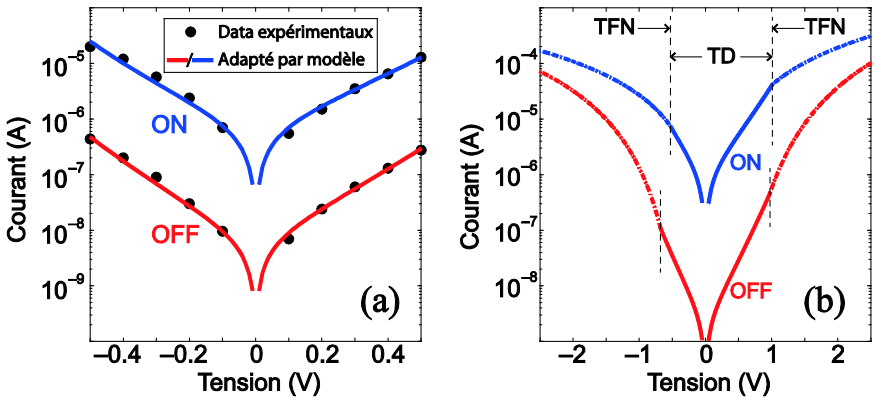

Figure S.6 (a) Courbe I-V ajusté par modèle de *Gruverman* dans le régime à basse tension. (b) courbe I-V complète simulée par le modèle développé.

Troisièmement, un modèle memristif est nécessaire pour définir la memristance de la JTF en fonction du temps. Pour la JTF que nous étudions, le comportement memristif peut être expliqué par la Figure S.7 (a) [12]. Au cours du renversement de la polarisation, les domaines opposés coexistent dans la barrière (rappeler Figure S.2). La JTF est équivalente à deux résistances connectées en parallèle. Chaque résistance est représentée par une JTF dont le domaine est entièrement à l'état ON ou OFF. Nous définissons son comportement memristif avec l'Eq. (S.6), où la fraction volumique du domaine de l'état OFF (s_{OFF}) est choisie comme variable d'état. Un algorithme itératif de faible complexité est développé pour résoudre s_{OFF} à un moment donné, comme Eq. (S.7). Le bon accord entre la simulation de modèle et les résultats expérimentaux [12] a été validé par la Figure S.7(b)–(e).

$$\begin{cases} V(t) = \dfrac{1}{\left[1 - s_{OFF}(t,V)\right]/R_{ON} + s_{OFF}(t,V)/R_{OFF}} \times I(t) \\ \dfrac{ds_{OFF}}{dt} = (1 - s_{OFF}) \times \dfrac{2}{\tau_P(V)} \times \sqrt{\ln\left(\dfrac{1}{1 - s_{OFF}}\right)} = f(s_{OFF}, V) \end{cases} \tag{S.6}$$

$$\begin{cases} t_r = \tau_P(V) \times \sqrt{\ln\left[\dfrac{1}{1 - s_{OFF}(t_0)}\right]} \\ s_{OFF}(t_0 + \Delta t) = 1 - \exp\left\{-\left[\dfrac{t_r + \Delta t}{\tau_P(V)}\right]^2\right\} \end{cases} \tag{S.7}$$

où $\tau_P(V)$ est résolu par l'Eq. (S.5). On notera que l'Eq. (S.6) est disponible uniquement pour $t > \tau_N$. Si $t < \tau_N$, s_{OFF} reste inchangé, il n'y a pas de comportement memristif. R_{ON} (R_{OFF}) est la résistance lorsque FTJ est entièrement dans l'état ON (OFF). t_r est dérivée par Eq. (S.4) en supposant $\tau_N = 0$. Δt est le pas de temps de simulation.

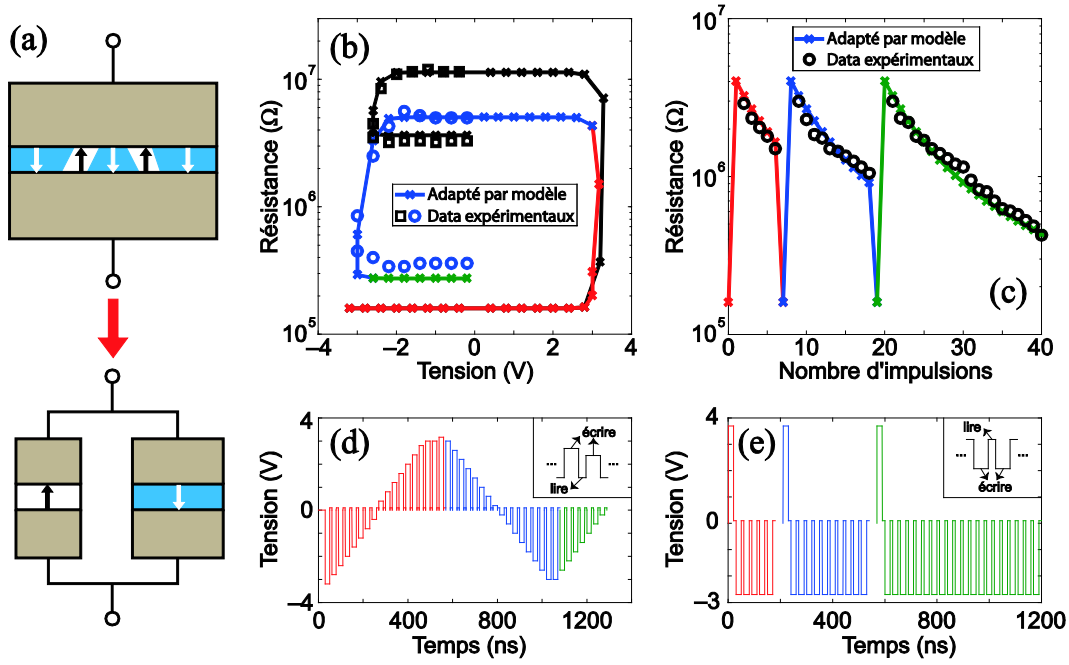

Figure S.7 (a) Modèle schématique de l'effet memristif de la JTF. (b)–(c) bon accord entre les données expérimentales et modèle ajusté. (d)–(e) impulsions appliquées pour le test.

En plus des sous-modèles ci-dessus, nous avons également étudié le modèle du rapport de TER et le modèle de commutation statique. Le premier indique que le rapport de TER peut être augmenté en augmentant la différence de hauteur moyenne de la barrière de potentiel entre les

états ON et OFF, ou en augmentant l'épaisseur de la barrière, comme le montre l'Eq. (S.8). Ce modèle est responsable du calcul de la tension de seuil de la JTF. Cependant, sur la base de l'étude [185]–[195], nous avons trouvé que la tension de seuil est très dépendante du matériau et du processus de fabrication. En outre, quelques chercheurs ont fait remarquer qu'il est impossible de définir une véritable tension de seuil pour le renversement de polarisation [187]–[188]. Par conséquent, nous ne proposerons pas le modèle de commutation statique pour la JTF.

$$TER(0)=\frac{R_{OFF}(0)}{R_{ON}(0)}=\sqrt{\frac{m_{ON}\bar{\varphi}_{ON}}{m_{OFF}\bar{\varphi}_{OFF}}}\exp\left[\frac{2\sqrt{2e}t_B}{\hbar}\left(\sqrt{m_{OFF}\bar{\varphi}_{OFF}}-\sqrt{m_{ON}\bar{\varphi}_{ON}}\right)\right] \qquad (S.8)$$

où $TER(0)$ est le rapport de TER sous le tension de zéro, mais cette équation est aussi une bonne approximation à basse tension.

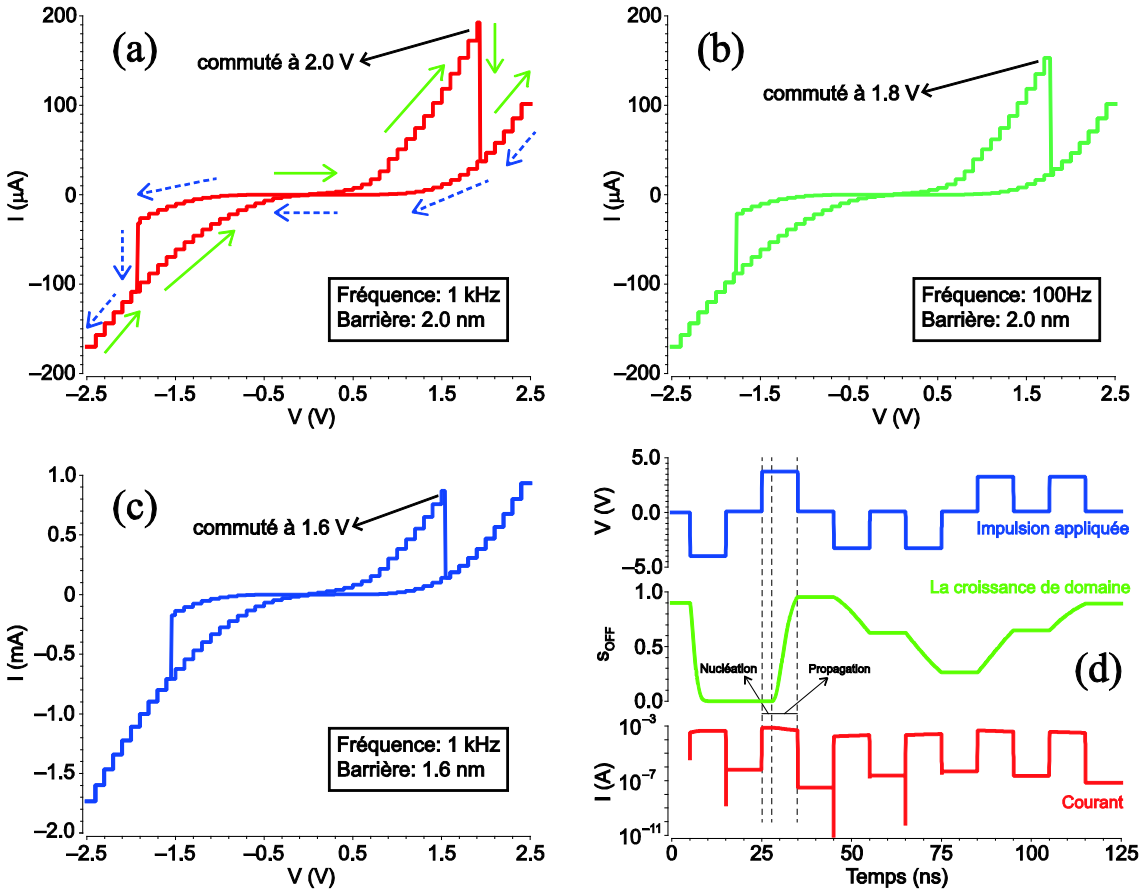

Figure S.8 Résultats des simulation basés sur le modèle développé: (a)–(c) d' hystérésis I-V pincé . (d) simulation transitoire.

Les trois sous-modèles ci-dessus ont été décrits en langue *Verilog-A* [35], ce qui le rend compatible avec les outils standards de simulation de circuit (par exemple, *Cadence*). La

simulation basée sur une cellule unique a été réalisée avec le modèle développé pour reproduire le comportement électrique de la JTF. Typiquement, des boucles d'hystérésis I-V pincés et des memristances commandées en tension ont été obtenues, comme présenté par la Figure S.8.

Chapitre 4 Conception et simulation de circuits à base de JTF

En utilisant le modèle de JTF développé dans le Chapitre 3 et le design kit « *STMicroelectronics* CMOS 40 nm » [37], nous avons conçu et simulé quatre circuits ou systèmes pour illustrer les applications potentielles de la JTF.

Le premier circuit que nous avons étudié est une mémoire vive basée sur la JTF (FTRAM), où la JTF est utilisé comme cellule de mémoire binaire. La question principale est la conception de la structure de la cellule. Au début, nous avons essayé la structure classique comprenant un transistor et une résistance (1T1R), mais elle conduit à une vitesse asymétrique d'écriture car la tension élevée d'écriture (3~4 V) de la JTF cause une dégradation importante due à la tension de seuil dans le transistor d'accès (voir Figure S.9). Pour résoudre ce problème, nous avons utilisé une cellule 2T1R où une porte de transmission (TG) est utilisée comme élément d'accès. L'architecture complète de la FTRAM est illustrée par la Figure S.10(a), où le circuit de lecture a été réalisé par un amplificateur de lecture à pré-charge (PCSA, voir Figure S.10(b)), et le circuit d'écriture se compose d'une unité de contrôle et de quatre transistors d'écriture (voir Figure S.10(c)). La fonction de cette FTRAM a été validée par la simulation transitoire présentée sur la Figure S.10(d).

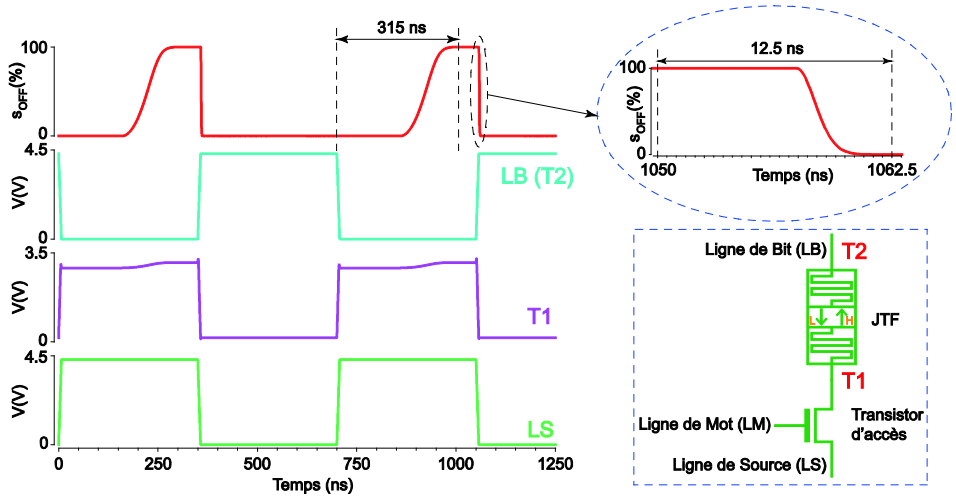

Figure S.9 Les résultats de simulation de l'opération d'écriture sur la base de la cellule 1T1R.

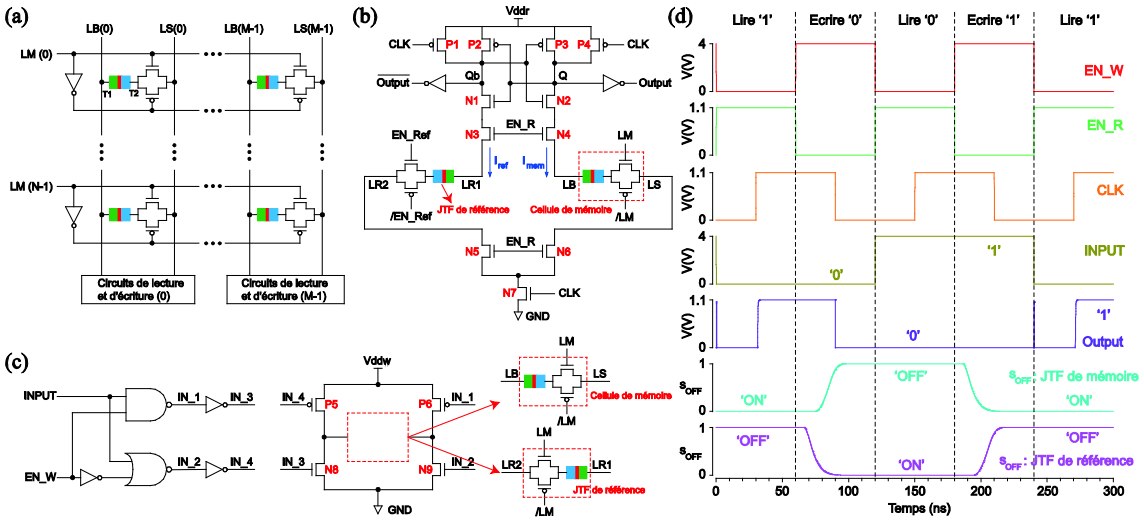

Figure S.10 (a) Architecture d'une FTRAM N × M bits, (b) circuit de lecture, (c) circuit d'écriture, et (d) simulation transitoire.

Par simulation transitoire et simulation statistique *Monte-Carlo*, nous avons étudié l'influence des paramètres des dispositifs sur la performance de la FTRAM proposée. La conclusion est résumée dans le Tableau S.1, qui indique comment ajuster les paramètres pour concevoir une FTRAM de haute performance. Comme nous pouvons le voir dans le tableau, le compromis est délicat entre les différents objectifs contradictoires de performance. Les paramètres des dispositifs doivent être optimisés en fonction de l'application visée.

Tableau S.1 Exigences des paramètres pour la FTRAM haute-performance

Exigence de performance	Aire de la JTF	Barrière de la JTF	Taille de transistor d'accès	barrière de fluage
Haute vitesse de lecture	Plus grande	Plus mince	Plus petite	–
Faible énergie de lecture	Plus grande	Plus mince	Plus petite	–
Grande fiabilité de lecture	Plus petite	Plus épais	Plus grande	–
Haute vitesse d'écriture	Plus petite	Non monotone	Plus grande	Plus petite
Faible énergie d'écriture	Plus petite	Non monotone	Plus grande	Plus petite
Temps de rétention important	Plus grande	Plus épais	–	Plus grande
Surface réduite de la cellule	–	–	Plus petite	–

Ensuite, la FTJ a été utilisée en tant que synapse dans deux systèmes neuromorphiques : un réseau de synapses pour émuler l'apprentissage exploitant la modification de la plasticité fonction de la corrélation des instants d'occurrence des impulsions pré et post-synpatiques, (en anglais : spike-timing dependent plasticity, STDP) [211], [213], et un crossbar neuronal (NC) pour exécuter l'apprentissage supervisé.

La Figure S.11 présente la structure cellulaire et l'architecture globale d'un réseau de 2×2 synapses à base de JTF. Une synapse est formée en connectant en série une JTF à un transistor, correspondant typiquement une cellule 1T1R. Notez qu'il est inutile d'utiliser la cellule de 2T1R comme dans la FTRAM ci-dessus, puisque le rôle de synapse permet à la JTF d'être programmé dans un état intermédiaire entre l'état ON et l'état OFF sans garder la symétrie entre deux directions d'écriture. Le poids synaptique (w) est calculé par l'Eq. (S.9). La modification du poids synaptique de w est directement liée à la variation de la résistance de la JTF (R_{JTF}).

$$w = I_{COM} / \left(V_{TE} - V_{BE}\right) \simeq \frac{1}{R_{JTF} + R_{MOS}} \tag{S.9}$$

où I_{COM} est le courant de communication circulant dans la JTF, $V_{TE} - V_{BE}$ est la tension appliquée à travers 'TE' et 'BE'. R_{JTF} et R_{MOS} sont les résistances de la JTF et du transistor, respectivement.

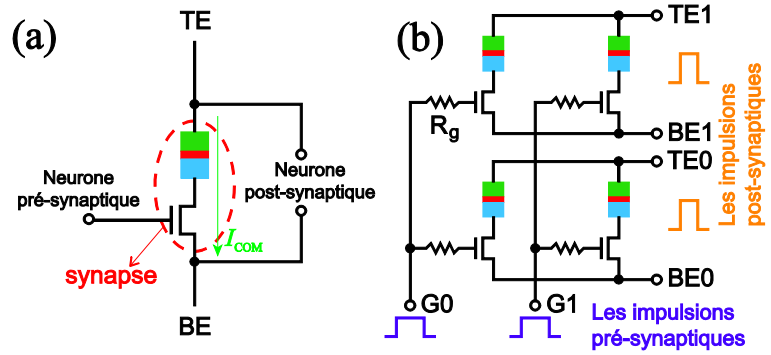

Figure S.11 (a) Schéma de synapse 1T1R entre pré-neurone et post-neurone, (b) 2×2 réseau de synapse 'crossbar-like'.

A partir du réseau de synapse proposé, nous avons conçu un programme d'apprentissage par STDP en se référant aux idées des Réfs. [216]–[218], comme illustré par la Figure S.12. L'opération est organisée par multiplexage temporel (TDM). Quand une impulsion pré-synaptique apparaît, deux impulsions positives sont successivement appliquées à la grille du transistor, dans les créneaux temporels de PLT (potentialisation à long terme) et de DLT (dépression à long terme),. La première impulsion est modulée en largeur par sa coïncidence avec une fenêtre

temporelle critique. L'autre impulsion dure seulement le temps de son créneau temporel. Quand une impulsion post-synaptique apparaît, une impulsion négative occupant un seul créneau temporel est générée dans créneaux temporels de PLT. Ensuite, une impulsion positive dont la largeur se réduit avec la fenêtre temporelle est déclenchée dans le créneau temporel de DLT. Sous l'action de ces signaux, le décalage temporel d'impulsions synaptiques se traduit par la durée de la programmation de la JTF, qui détermine le changement synaptique.

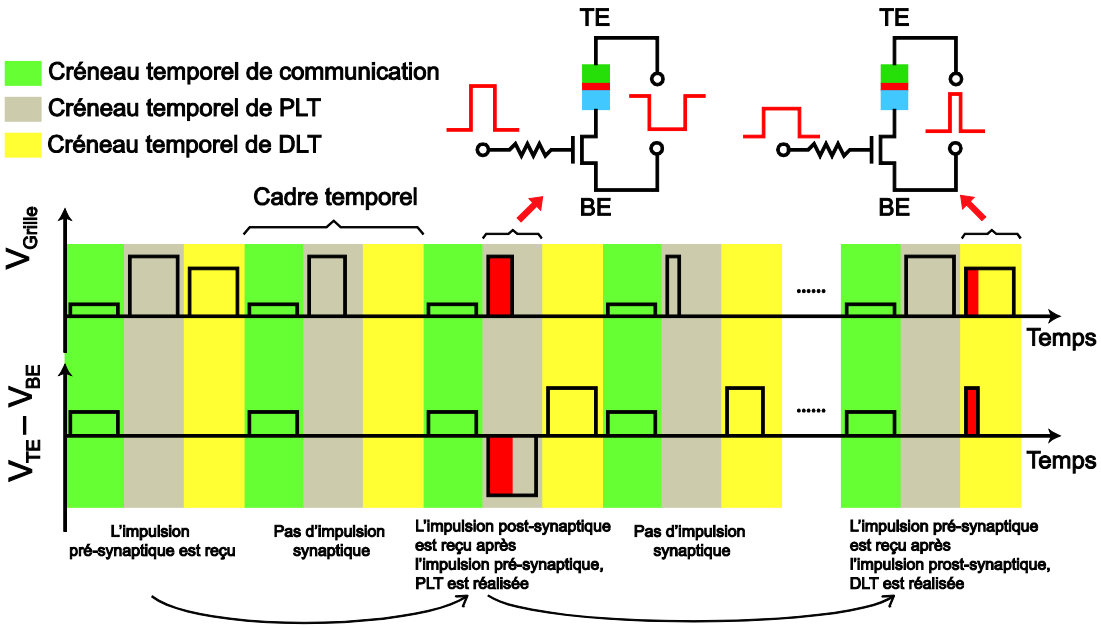

Figure S.12 Diagramme de la séquence de signaux détaillé décrivant la réalisation d'apprentissage STDP dans le réseau de synapse proposé.

Figure S.13(a) présente la simulation transitoire du réseau de 2×2 synapses, où le PLT et DLT sont validés par la variation du courant. Les Figure S.13(b) et (c) présentent respectivement le changement synaptique et la croissance de domaine en fonction du décalage temporel d'impulsions synaptiques, , qui reproduisent fidèlement la caractéristique du STDP [211] et valident le rôle dominant de la résistance de la JTF dans le poids synaptique.

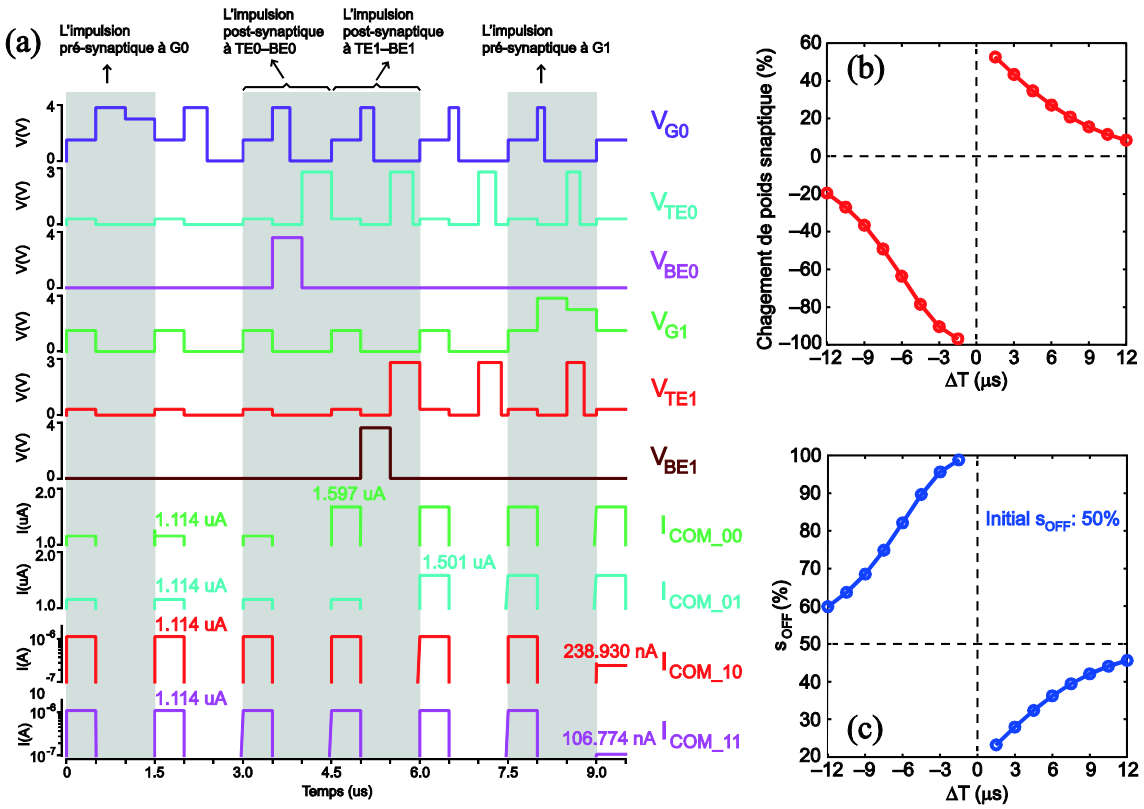

Figure S.13 (a) La simulation transitoire d'apprentissage basé sur le réseau de 2 × 2 synapse. (b)–(c) Changement du poids synaptique (b) et de s_{OFF} (c) en fonction du décalage temporel d'impulsions synaptiques.

Nous avons analysé le taux relatif de variation de la résistance de la JTF au cours du processus d'apprentissage, qui peut directement influencer la vitesse d'apprentissage. Une expression approximative a été obtenue comme le montre l'Eq. (S.10). On voit que l'augmentation de s_{OFF} ou la diminution de τ_P peut améliorer la vitesse d'apprentissage, ce qui a été validée par simulation.

$$\frac{1}{R}\cdot\frac{dR}{dt} \simeq \frac{2}{\tau_P}\sqrt{\ln\left(\frac{1}{1-s_{OFF}}\right)} \tag{S.10}$$

La Figure S.14 illustre l'architecture de NC proposée, basé sur la JTF, qui consiste en un réseau de synapses, des neurones et des cellules d'apprentissage. Un avantage attrayant de cette NC est la cellule compacte d'apprentissage réduite à un couple de JTFs orientées de façon anti-parallèles [219], quatre transistors et un inverseur. La règle d'apprentissage supervisé est illustrée par la Figure S.15(a). Pendant une époque d'apprentissage, quatre transistors sont successivement activés pour connecter C_j à des signaux différents. Le poids synaptique est ajusté jusqu'à ce que

l'erreur entre la sortie réelle O_j et la sortie attendue Y_j soit nulle. L'apprentissage parallèle de fonctions logiques 'AND' et 'OR' a été validé par simulation transitoire. Les résultats partiels sur l'apprentissage de 'AND' sont présentés par Figure S.15(b).

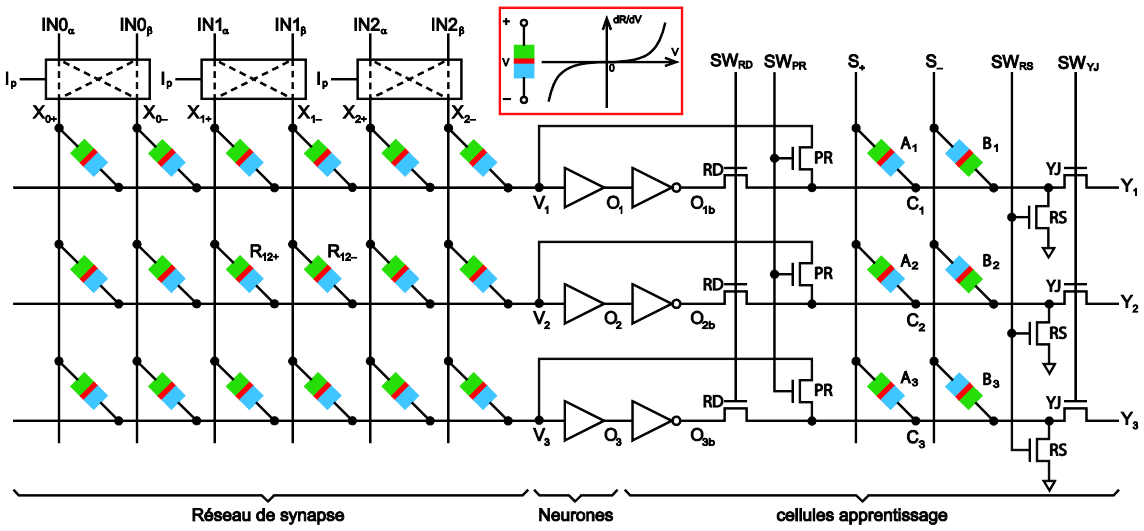

Figure S.14 Architecture du crossbar basé sur la JTF.

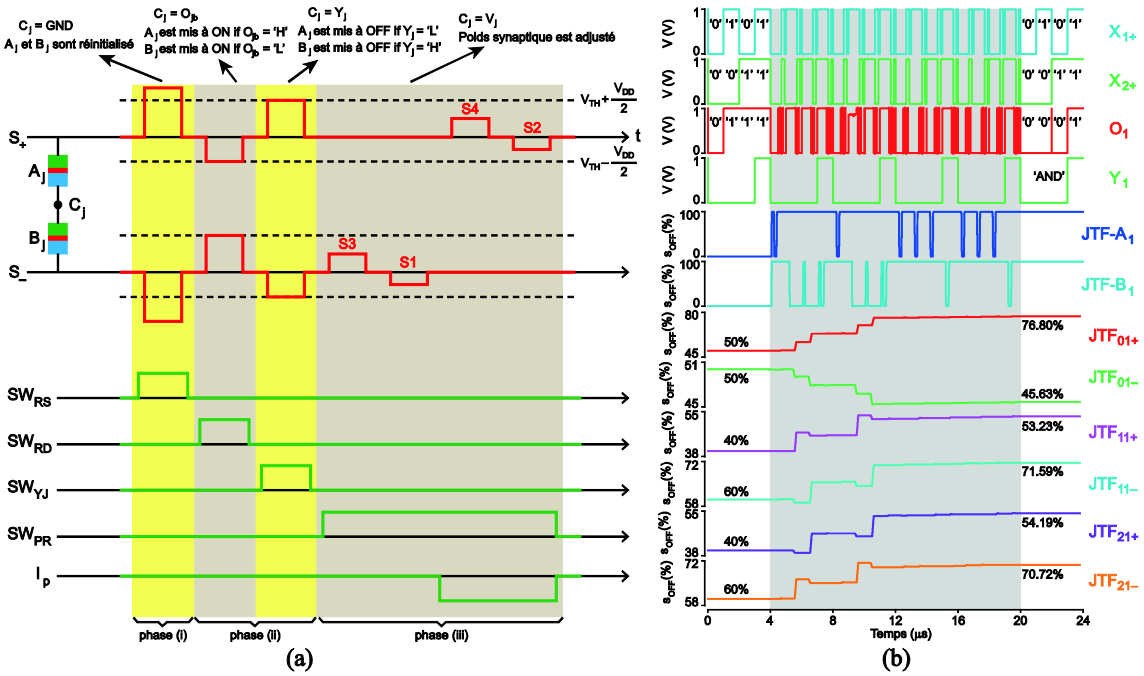

Figure S.15 (a) Séquence signal pendant une époque d'apprentissage. V_{TH} est le seuil de la JTF-A ou JTF-B, V_{DD} est le niveau de sortie du neurone. (b) des résultats partiels de simulation sur l'apprentissage de 'AND'.

Par simulation statistique de *Monte-Carlo*, nous avons analysé la tolérance du NC proposé contre les défauts tels que la variation de taille et le défaut de collage. Nous avons constaté que la tolérance aux pannes peut être améliorée en modifiant le nombre d'époques d'apprentissage.

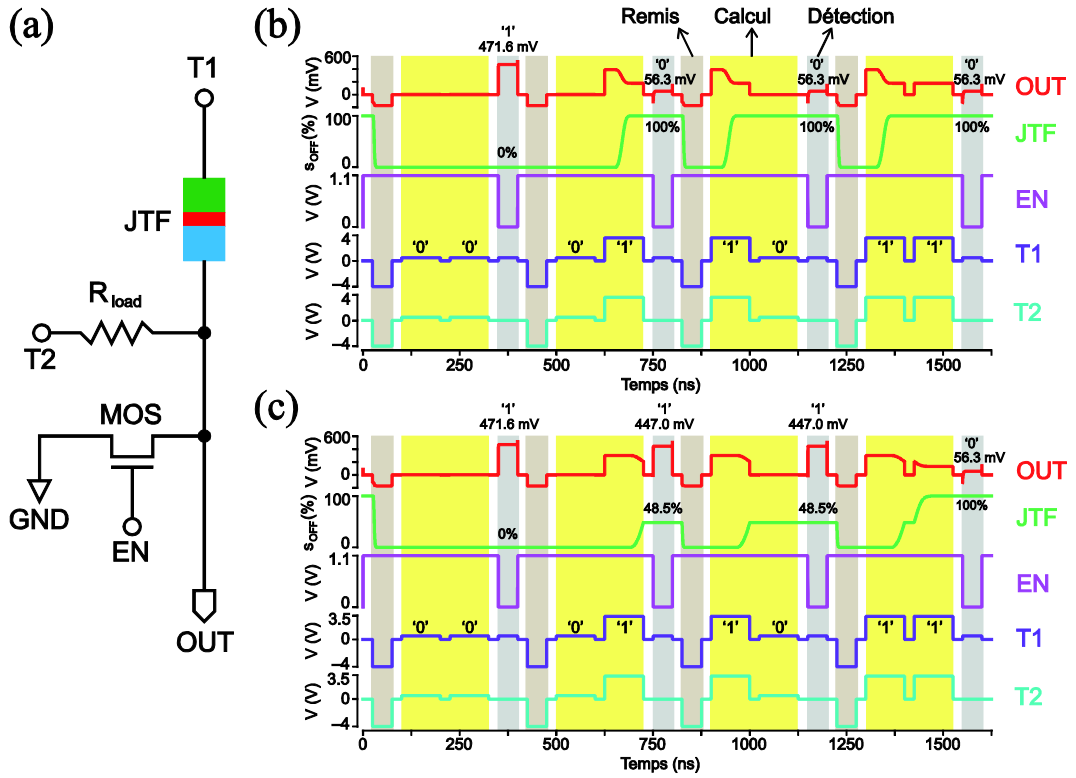

Figure S.16 (a) Le bloc logique basé sur la JTF proposé. (b)–(c) Simulation transitoire des fonctions logiques 'NOR' et 'NAND'.

Enfin, nous avons proposé un bloc logique composé d'une JTF, d'une résistance et d'un transistor, comme présenté par la Figure S.16(a). En utilisant ce bloc logique, les fonctions 'NOR' et 'NAND' peuvent être réalisées dans une JTF seule. Les entrées logiques '0' et '1' sont représentées par deux impulsions successives de programmation de grandes et petites amplitudes, respectivement. Les sorties logiques '0' et '1' correspond respectivement aux états ON et OFF de la JTF. Avant le calcul logique, la JTF est réinitialisée à l'état ON. Pour réaliser la fonction 'NOR', l'amplitude d'impulsion pour l'entrée '1' est choisie à assez grande pour que la JTF puisse être programmée à l'état OFF, à condition qu'au moins l'une des entrées soit à '1'. Pour réaliser la fonction 'NAND', l'amplitude d'impulsion pour l'entrée '1' doit être diminué afin que la JTF reste l'état basse-résistance sauf quand les deux entrées sont '1'. Cette idée est réalisable pour la JTF, parce que la résistance de la JTF reste petite au cours de la phase initiale de commutation ON-à-OFF, comme exprimé par l'Eq. (S.11).

$$R \simeq R_{ON} \times \exp\left(\frac{{T_P}^2}{{\tau_P}^2}\right) \tag{S.11}$$

où T_P est le temps de propagation de mur de domaine.

Les résultats de simulation présentés par les Figure S.16(b) et (c) illustrent et valident le processus de calcul des fonctions logiques 'NOR' et 'NAND', respectivement. Nous avons analysé l'influence des paramètres des impulsions d'entrée sur la marge de sortie et l'énergie de calcul. Deux amplitudes optimales pour l'impulsion entrée '1' ont été déterminées pour les fonctions 'NAND' et 'NOR', pour lesquelles la marge maximum de sortie peut être obtenue sans consommation d'énergie de calcul excessive.

Chapitre 5 Transfert de spin assisté par effet Hall de spin

Dans ce chapitre, nous avons étudié un nouveau mécanisme de renversement de l'aimantation qui est générée dans un dispositif à trois électrodes illustré par Figure S.17. Dans ce cas, une p-JTM est déposé au dessus d'une bande de métal lourd. Deux courants d'écriture (courants TS et EHS dans Figure S.17) sont nécessaires pour produire respectivement TS et EHS. Une équation LLG modifiée pour prendre en compte EHS et TS permet de décrire la dynamique de l'aimantation de la CL, comme le montre l'Eq. (S.12).

$$\begin{aligned}\frac{\partial \vec{m}}{\partial t} &= -\gamma\mu_0 \vec{m} \times \vec{H}_{\text{eff}} + \alpha \vec{m} \times \frac{\partial \vec{m}}{\partial t} \\ &\quad -\frac{\gamma \hbar}{2et_{\text{F}}M_{\text{s}}}\left[PJ_{\text{STT}}\vec{m} \times \left(\vec{m} \times \vec{m}_{\text{r}}\right) + \eta_{SH}J_{\text{SHE}}\vec{m} \times \left(\vec{m} \times \vec{\sigma}_{\text{SH}}\right)\right]\end{aligned} \tag{S.12}$$

où les trois derniers termes du côté droit de l'équation sont, par ordre, couple amorti de Gilbert, TS et couple induit par EHS. $\vec{\sigma}_{SH}$ représente l'orientation de polarisation du spin injecté. J_{STT} and J_{SHE} sont les densités de courant TS et EHS, respectivement. $\vec{H}_{eff}$ est le champ magnétique efficace. γ est le rapport gyromagnétique. μ_0 est la constante magnétique. α est la constante d'amortissement de Gilbert. P est la polarisation de spin, t_F est l'épaisseur de CL, M_s est l'aimantation à saturation, $\vec{m}_r$ est le vecteur unitaire le long de la magnétisation de CR.

Tout d'abord, nous avons effectué une simulation numérique basée sur l'Eq. (S.12) afin de révéler les rôles joués par TS et EHS. Ici, nous supposons que la fluctuation thermique entraîne uniquement une déviation aléatoire de l'angle polaire initial autour de l'axe d'anisotropie [227]. Les résultats et conclusions importantes sont résumés comme suit:

La Figure S.18 (a)–(c) présente l'évolution de l'aimantation de la CL sous un seul courant EHS d'écriture. On voit que d'une petite J_{SHE} exerce peu d'influence sur l'aimantation. Une fois

J_{SHE} supérieure à une valeur critique (qui peut être calculée par Eq. (S.13)), la direction d'aimantation peut être tournée dans le plan ($m_z = 0$) à une vitesse élevée. Néanmoins, la commutation déterministe ne peut pas être atteinte par un seul courant EHS d'écriture.

$$J_{c,SHE} = \frac{e}{\hbar} \times \frac{\mu_0 M_s H_k t_F}{\xi \eta_{SH}} \tag{S.13}$$

où $\xi \approx 1.22 \sim 1.24$ est un coefficient empirique déterminée par ajustement aux résultats de simulation.

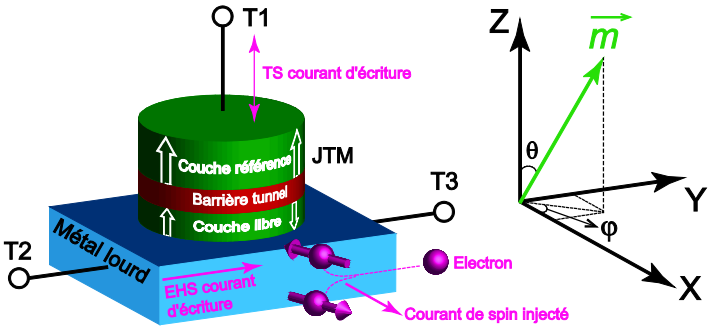

Figure S.17 Structure de la JTM assisté par EHS et système de coordonnées.

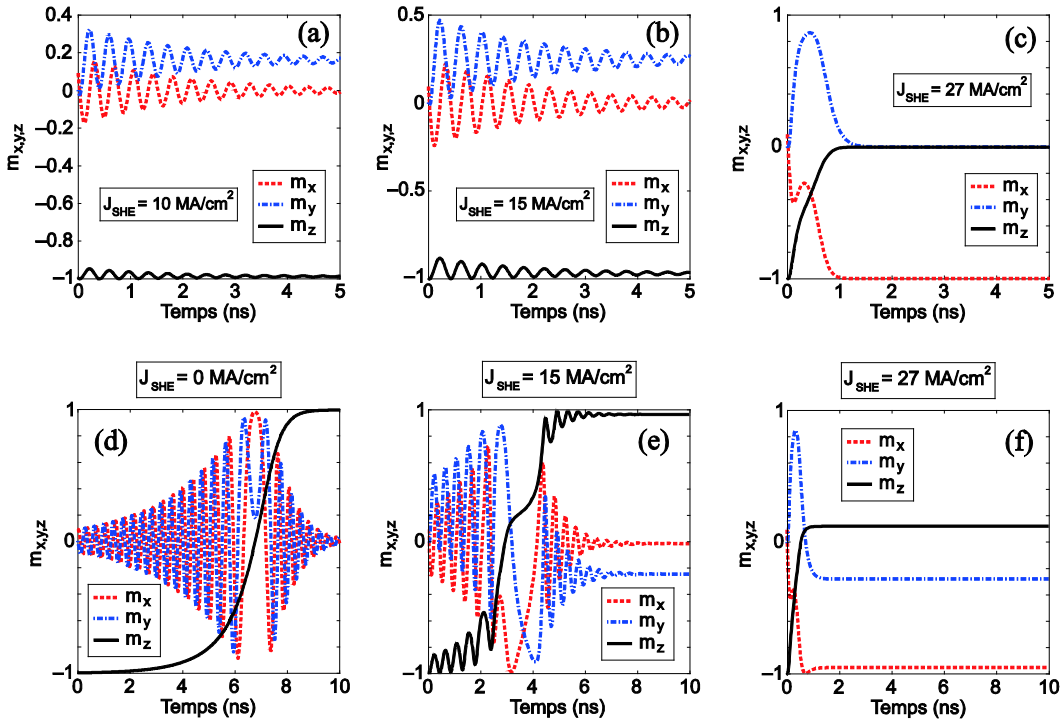

Figure S.18 (a)–(c) Dynamique de l'aimantation sous un seul courant EHS d'écrire avec différentes densités. (d)–(f) Dynamique de l'aimantation sous la combinaison des courants TS et EHS. Ici J_{STT} est fixé à 1.55 $\mathrm{MA/cm^2}$.

Les Figures S.18 (d)–(f) présentent la dynamique d'aimantation sous la combinaison d'un J_{STT} fixe et divers J_{SHE}. Si $J_{SHE} = 0$, la commutation par TS conventionnel se produit. Si J_{SHE} est inférieure à la valeur critique $J_{c,SHE}$, le comportement de commutation est encore semblable à TS mais avec des perturbations. Si J_{SHE} est proche de ou supérieure à la valeur critique, l'aimantation est rapidement tournée au-dessus plan et se stabilise dans une orientation spécifique entre dans le plan et l'axe +Z axis ($0 < m_z < 1$). Ce comportement est similaire à la Figure S.18 (c), ce qui signifie que la commutation de l'aimantation est dominée par l'EHS plutôt que le TS dans ce cas.

La figure S.18(f) prévoit un mécanisme de commutation ultrarapide éliminant le délai d'incubation, mais l'aimantation ne peut pas être complètement tournée dans l'axe d'anisotropie perpendiculaire. Ceci démontre que le grand EHS joue un rôle d'aide lors de la phase initiale de la commutation de l'aimantation, mais un rôle limitant quand l'aimantation passe le plan. Une solution à ce problème est illustrée sur Figure S.19, où le courant EHS d'écriture est supprimé après 0,5 ns afin que le TS finisse de réaliser la commutation complète. Ce nouveau mécanisme de commutation est appelé 'TS assisté par EHS'.

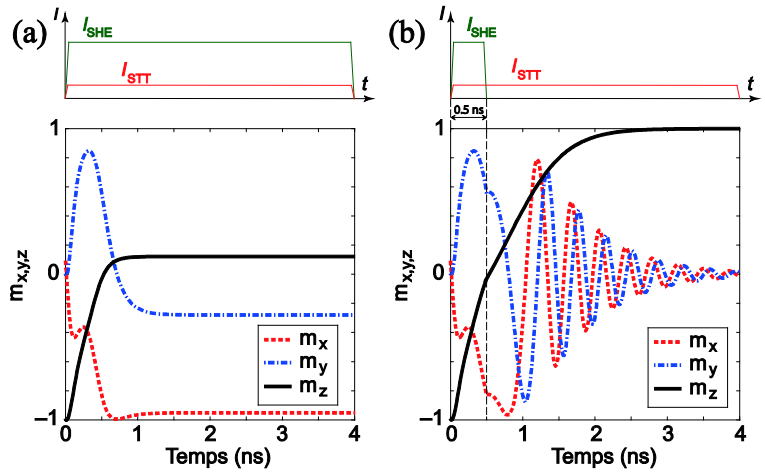

Figure S.19 Influence de la durée du courant EHS d'écrire sur la dynamique de d'aimantatiion. Cartons supérieurs montrent la forme d'onde des courants d'écriture.

En outre, nous avons étudié les influences des couples 'field-like' et la direction du courant EHS d'écriture. Le couple 'field-like' induit par TS a peu d'impact sur la dynamique de l'aimantation, mais le rôle du couple 'field-like' induit par EHS est relativement important et complexe. Il mérite plus d'efforts de recherche. La direction du courant EHS d'écriture ne contribue pas au processus de commutation déterministe parce que son inversion est simplement équivalente à un décalage de π dans l'angle azimutal initiale.

Ensuite, nous avons développé un modèle électrique compact pour la JTM à trois terminaux, commuté par 'TS assisté par EHS'. Ce modèle consiste en un modèle de résistance tunnel et un modèle de commutation dynamique. Le premier peut être calculé par les Eq. (S.14) [94], [169], [202], et celles-ci peuvent être obtenues par résolution de Eq. (S.12).

$$\begin{cases} R_P = \dfrac{t_B}{F \times \bar{\varphi}^{1/2} \times S} \times \exp\left(\dfrac{2(2me\bar{\varphi})^{1/2}}{\hbar} \times t_B \right) \\ R_{JTM}(V,\theta) = R_P \dfrac{1+(V/V_h)^2 + TMR_0}{1+(V/V_h)^2 + TMR_0\left[(1+\cos\theta)/2\right]} \end{cases} \tag{S.14}$$

où R_P est la résistance de la JTM dans l'état parallèle sous tension nulle. R_{JTM} est la résistance de la JTM à la V et θ donné. F est un facteur déterminé par le produit résistance-aire. $\bar{\varphi}$ est la hauteur de barrière de potentiel. TMR_0 est le rapport TMR sous tension nulle. V_h est la tension à laquelle le rapport TMR est divisée par 2.

En utilisant le modèle électrique développé et le design kit « *STMicroelectronics* CMOS 28 nm » [38], nous avons conçu et simulé une bascule magnétique écrit par 'TS assisté par EHS', dont le schéma est illustré par la Figure S.20. Cette bascule utilise la structure maître-esclave et la cellule 2T1R. Les résultats de simulation présentés dans Figure S.21(a) valident la fonction de la bascule proposée. Les courants d'écriture détaillés sont présentés dans Figure S.21(b). Elle concorde avec l'exigence de 'TS assisté par EHS' (voir Figure S.19).

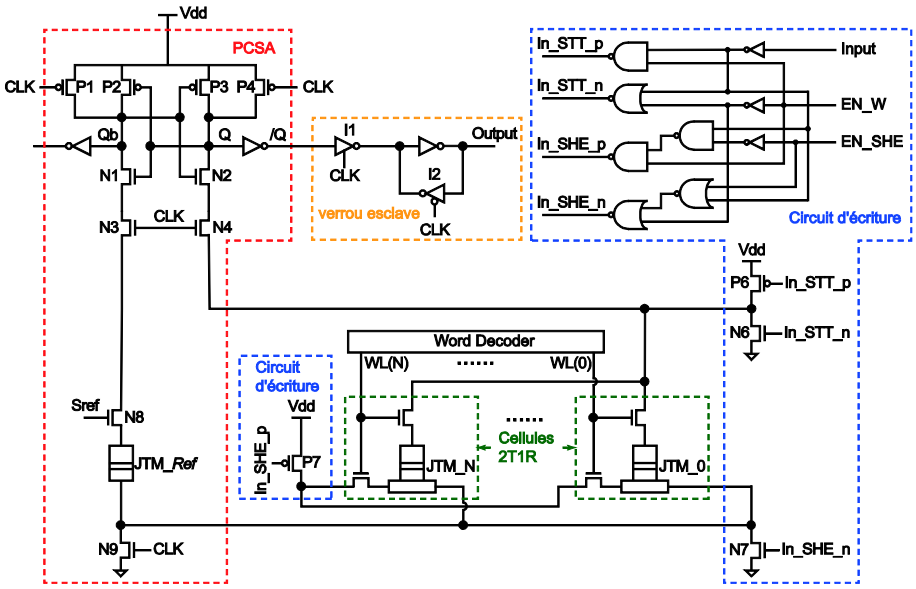

Figure S.20 Schéma des circuits de lecture et d'écriture pour la bascule magnétique proposée.

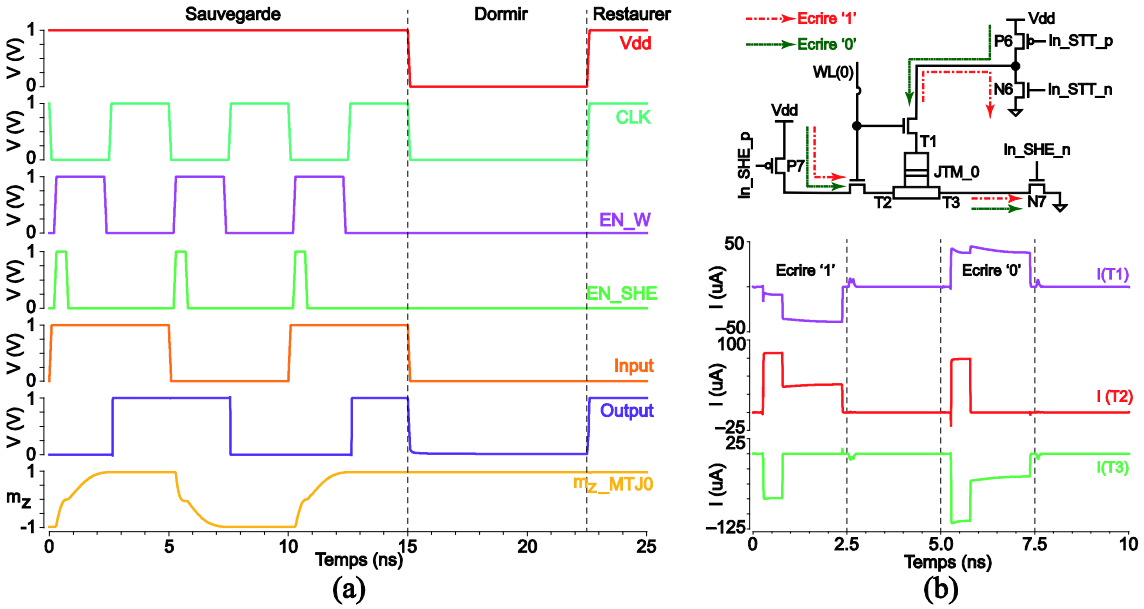

Figure S.21 Simulation transitoire de la bascule magnétique proposée. (b) détails des courants d'écriture qui circulent à travers trois bornes du dispositif.

Nous avons discuté de la comparaison des performances entre la bascule proposée et la bascule écrit par TS conventionnel. La Figure S.22 présente la largeur du transistor d'accès et l'énergie d'écriture en fonction de la taille de JTM sous la même fréquence de fonctionnement. Clairement, l'avantage de la bascule assistée par EHS face à la bascule écrit par TS est important pour de grandes tailles de JTM, mais il est moindre avec la réduction de la taille de la JTM et même disparaît en dessous de 40 nm. La dégradation de performance est attribuable à l'augmentation spectaculaire du courant EHS d'écriture. En outre, indépendamment de la taille de la JTM, le risque de rupture de la barrière dans la bascule assisté par EHS est limité grâce à la réduction de la tension d'écriture.

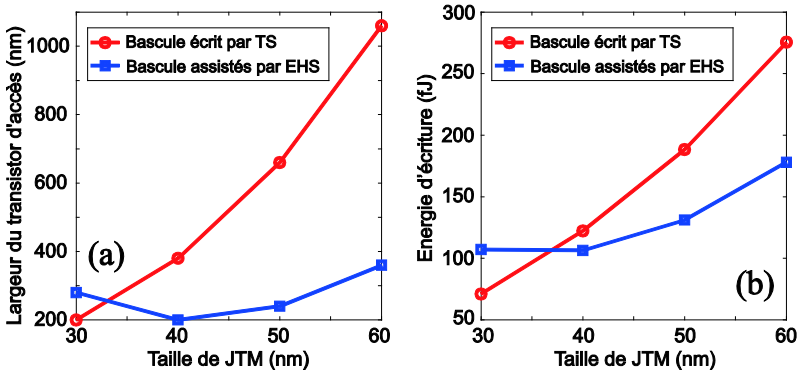

Figure S.22 Largeur de transistor d'accès (a) et énergie d'écrire (b) en fonction de la taille de JTM sous une fréquence de fonctionnement de 200 MHz.

De plus, la méthode 'TS assisté par EHS' a été appliquée à la conception et la simulation d'un additionneur 1 bit magnétique. La même conclusion que la bascule ci-dessus peut être tirée.

Chapitre 6 Conclusions et perspectives

Deux objectifs sont atteints par le travail de cette thèse. Tout d'abord, la recherche sur la JTF est étendue du domaine de la physique à l'application dans ces circuits. Deuxièmement, le principe, la performance et l'application de 'TS assisté par EHS' a été discuté et étudié par simulation.

Dans l'état de l'art, nous avons introduit l'histoire, les progrès récents, et l'état de l'art des JTFs et JTMs. Notre étude démontre la nécessité de la recherche présentée dans cette thèse.

Tout d'abord, un modèle électrique compact de la JTF a été développé en langue *Verilog-A* basé sur les théories physiques et les résultats expérimentaux. A notre connaissance, ce modèle est le premier modèle électrique de la JTF. Le modèle développé a montré un bon accord avec les résultats expérimentaux. La simulation basée sur une cellule unique a validé la fonctionnalité de notre modèle et reproduit fidèlement les comportements électriques de la JTF (par exemple, une série de boucles d'hystérésis I-V pincés a été simulée avec succès).

Puis, en utilisant le modèle développé de la JTF et le design kit « *STMicroelectronics* CMOS 40 nm », nous avons conçu et simulé quatre circuits hybrides de CMOS/JTF: une FTRAM pour le stockage non-volatile, un réseau de la synapse basé sur la JTF pour l'apprentissage par STDP, un NC basé sur la JTF pour l'apprentissage supervisé sur puce, et un bloc logique basée sur la JTF pour le calcul logique. Les performances de ces circuits ont été analysés sur la base de la simulation transitoire et de la simulation statistique de *Monte-Carlo*.

Pour la FTRAM, les influences des paramètres du dispositif sur la performance de lecture/ écriture ont été discutés. Il a été démontré que, pour optimiser la FTRAM, un compromis doit être trouvé pour chaque paramètre. Dans le réseau des synapses basé sur la JTF, chaque synapse est constituée d'un transistor et d'une JTF. L'analyse basée sur la simulation a montré que la vitesse d'apprentissage est liée à la configuration de domaine et au temps caractéristique de propagation de paroi de domaine. Le NC basé sur la JTF utilise des cellules compactes d'apprentissage qui sont constituées de seulement quatre transistors, deux JTFs et un inverseur. L'apprentissage parallèle de fonctions logiques 'AND' et 'OR' a été réalisé par simulation transitoire. Des simulations statistiques de *Monte-Carlo* montrent que la tolérance aux pannes du NC proposé peut être améliorée en augmentant le nombre d'époques d'apprentissage. Le bloc logique basé sur les JTF peut exécuter des fonctions logiques 'NAND' et 'NOR' dans un seul JTF,. Ceci a été validée par simulation. Deux amplitudes optimales pour les impulsions d'entrée de fonctions logiques 'NAND' et 'NOR' ont été déterminées.

Enfin, nous avons étudié la dynamique d'aimantation perpendiculaire sous le TS et l'EHS par la simulation numérique d'une équation modifiée de LLG. Il est démontré qu'un courant EHS d'écriture suffisant avec une durée appropriée permet d'éliminer le délai d'incubation du TS conventionnel. Ce mécanisme est appelé 'TS assisté par EHS'. Nous avons également constaté que le couple 'field-like' induit par TS et la direction du courant EHS d'écriture ont peu d'impact sur le 'TS assisté par EHS', mais l'influence du couple 'field-like' induit par EHS est importante et complexe. Elle nécessite plus d'efforts de recherche. Le 'TS assisté par EHS' a été appliqué à l'écriture d'une bascule magnétique et un additionneur 1 bit magnétique. Leur fonctions ont été validées par la simulation transitoire basée sur un modèle développé de JTM à trois terminaux et le design kit « STMicroelectronics CMOS 28 nm ». Les résultats des simulations ont montré que, si la taille de JTM est grande (> 40 nm), les circuits magnétiques assisté par EHS peuvent atteindre surface réduite de la cellule et une plus faible énergie d'écriture comparées à celles écrites par TS conventionnel sous la même fréquence de fonctionnement. Mais pour la JTM de petite taille, cette amélioration disparaît en raison du plus fort courant EHS d'écriture. Néanmoins, le 'TS assisté par EHS' permet de réduire la tension d'écriture de la JTF sous toutes les tailles, ce qui diminue le risque de rupture de la barrière.

Le travail de cette thèse peut être encore amélioré et étendu. Par exemple, dans le régime à haute tension, la caractéristique I-V de la JTF n'a pas été bien étudiée. Plus de données expérimentales et un modèle plus précis de résistance tunnel sont nécessaires. En ce qui concerne la FTRAM, l'intégration entre la JTF et la technologie nanométrique CMOS est contrainte par la haute tension d'écriture. L'utilisation de l'architecture 'cross-point' [144] ou la conception de mémoires multiniveaux [236] serait une bonne solution. Pour les circuits magnétiques assistés par EHS, un circuit optimisé est souhaitable pour surmonter la limitation de l'amélioration des performances. Récemment, un sujet plus émergent est la combinaison de la polarisation et de l'aimantation [237]–[241], qui promet d'atteindre une meilleure performance dans les mémoires et circuits logiques non-volatiles.

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ÉCOLE DOCTORALE
Physique et ingénierie : électrons, photons, sciences du vivant (EOBE)

Titre : Modélisation compacte et conception de circuit à base de jonction tunnel ferroélectrique et de jonction tunnel magnétique exploitant le transfert de spin assisté par effet Hall de spin

Mots clés : jonction tunnel ferroélectrique, jonction tunnel magnétique, Effet Hall de spin, transfert de spin, modèle compacte, circuits non-volatiles

Résumé : Les mémoires non-volatiles sont l'objet d'un effort de recherche croissant du fait de leur capacité à limiter la consommation statique, qui obère habituellement la réduction des dimensions dans la technologie CMOS. Dans ce contexte, cette thèse aborde plus spécifiquement deux technologies de mémoires non volatiles: les jonctions tunnel ferroélectriques (JTF) et le transfert de spin (TS) assisté par effet Hall de spin (EHS).
J'ai d'abord développé un modèle électrique compact de la JTF basé sur les modèles physiques connexes et les résultats expérimentaux. Ce modèle peut être exploité sur la plate-forme Cadence (un outil standard pour la simulation de circuit). Il reproduit fidèlement les comportements de JTF.
Ensuite, en utilisant ce modèle de JTF et le design -kit CMOS de STMicroelectronics, j'ai conçu, simulé et analysé trois types de circuits: i) une mémoire vive (RAM) basée sur les JTF, ii) deux systèmes neuromorphiques basés sur les JTF pour l'émulation de la plasticité synaptique basée sur le décalage temporel des impulsions neuronale (STDP) et pour l'apprentissage supervisé de fonctions logiques, respectivement, iii) un bloc logique booléen basé sur les JTF.
Finalement, nous avons effectué une simulation numérique basée sur l'équation de Landau-Lifshitz-Gilbert pour étudier le retournement de l'aimantation perpendiculaire induite par le TS et assisté par l'EHS. Cette nouvelle méthode de la commutation de l'aimantation a été appliquée à la conception et l'analyse d'une bascule magnétique et d'un additionneur 1 bit magnétique.

Title : Compact modeling and circuit design based on ferroelectric tunnel junction and spin-Hall-assisted spin-transfer torque

Keywords : Ferroelectric tunnel junction, magnetic tunnel junction, Spin-Hall effect, Spin-transfer torque, compact model, non-volatile circuits

Abstract : Non-volatile memories have been attracting intensive research interest since they promise to solve the increasing static power issue caused by CMOS technology scaling. This thesis focuses on two fields related to non-volatile memories: ferroelectric tunnel junction (FTJ) and spin-Hall-assisted spin-transfer torque (STT).
First, we developed a compact electrical model of the FTJ based on the related physical models and experimental results. This model can run on Cadence platform (a standard circuit simulation tool) and faithfully reproduce the electrical behaviors of the FTJ.
Then, by using the developed FTJ model and STMicroelectronics CMOS design kit, we designed, simulated and analyzed three types of circuits: i) an FTJ-based random access memory, ii) two FTJ-based neuromorphic systems for the emulation of spike-timing dependent plasticity (STDP) and the supervised learning of logic functions, respectively, iii) an FTJ-based Boolean logic block.
Finally, we performed numerical simulation based on Landau-Lifshitz-Gilbert equation to study the reversal of the perpendicular magnetization driven by spin-Hall-assisted STT. This novel approach of magnetization switching was applied to the design and analysis of the magnetic flip-flop and full-adder.

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