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# Electrothermal device-to-circuit interactions for half THz SiGe C HBT technologies

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N° d'ordre:



# THÈSE

PRÉSENTÉE A

**L'UNIVERSITÉ BORDEAUX 1**

**ECOLE DOCTORALE DE SCIENCES PHYSIQUES ET DE L'INGENIEUR**

Par **Mario WEIß**

POUR OBTENIR LE GRADE DE

**DOCTEUR**

SPECIALITE: **ELECTRONIQUE**

\*\*\*\*\*

## **Electrothermal device-to-circuit interactions for half THz SiGe:C HBT technologies**

\*\*\*\*\*

Soutenance prévue le : 25<sup>th</sup> Novembre 2013

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-- 2013 --



## Résumé

Ce travail concerne les transistors bipolaires à hétérogène TBH SiGe. En particulier, l'auto-échauffement des transistors unitaires et le couplage thermique avec leurs plus proches voisins périphériques sont caractérisés et modélisés. La rétroaction électrothermique intra-et inter-transistor est largement étudiée. En outre, l'impact des effets thermiques sur la performance de deux circuits analogiques est évalué. L'effet d'auto-échauffement est évalué par des mesures à basse fréquence et des mesures impulsionnelles DC et AC. L'auto-échauffement est diminué de manière significative en utilisant des petites largeurs d'impulsion. Ainsi la dépendance fréquentielle de l'auto-échauffement a été étudiée en utilisant les paramètres H et Y. De nouvelles structures de test ont été fabriqués pour mesurer l'effet de couplage. Les facteurs de couplage thermique ont été extraits à partir de mesures ainsi que par simulations thermiques 3D. Les résultats montrent que le couplage des dispositifs intra est très prononcé. Un nouvel élément du modèle de résistance thermique récursive ainsi que le modèle de couplage thermique a été inclus dans un simulateur de circuit commercial. Une simulation transitoire entièrement couplée d'un oscillateur en anneau de 218 transistors a été effectuée. Ainsi, un retard de porte record de 1.65ps est démontré. À la connaissance des auteurs, c'est le résultat le plus rapide pour une technologie bipolaire. Le rendement thermique d'un amplificateur de puissance à 60GHz réalisé avec un réseau multi-transistor ou avec un transistor à plusieurs doigts est évalué. La performance électrique du transistor multi-doigt est dégradée en raison de l'effet de couplage thermique important entre les doigts de l'émetteur. Un bon accord est constaté entre les mesures et les simulations des circuits en utilisant des modèles de transistors avec le réseau de couplage thermique. Enfin, les perspectives sur l'utilisation des résultats sont données.

**Mots-clés:** Hétéro-transistors bipolaires (HBT), les technologies térahertz, modélisation électrothermique, le couplage thermique mutuel, le dispositif à des interactions de circuit, oscillateur en anneau, les retards de grille de multiplication, un amplificateur de puissance, le transistor à plusieurs doigts, résistance thermique, capacité thermique, l'impédance thermique, des caractérisations de dispositifs à semi-conducteurs, mesures impulsion, la modélisation d'un dispositif semi-conducteur, la simulation TCAD thermique



## Abstract

The power generated by modern silicon germanium (SiGe) heterojunction bipolar transistors (HBTs) can produce large thermal gradients across the silicon substrate. The device operating temperature modifies model parameters and can significantly affect circuit operation. This work characterizes and models self-heating and thermal coupling in SiGe HBTs. The self-heating effect is evaluated with low frequency and pulsed measurements. A novel pulse measurement system is presented that allows isothermal DC and RF measurements with 100ns pulses. Electrothermal intra- and inter-device feedback is extensively studied and the impact on the performance of two analog circuits is evaluated. Novel test structures are designed and fabricated to measure thermal coupling between single transistors (inter-device) as well as between the emitter stripes of a multi-finger transistor (intra-device). Thermal coupling factors are extracted from measurements and from 3D thermal simulations. Thermally coupled simulations of a ring oscillator (RO) with 218 transistors and of a 60GHz power amplifier (PA) are carried out. Current mode logic (CML) ROs are designed and measured. Layout optimizations lead to record gate delay of 1.65ps. The thermal performance of a 60GHz power amplifier is compared when realized with a multi-transistor array (MTA) and with a multi-finger transistor (MFT). Finally, perspectives of this work within a CAD based circuit design environment are discussed.

**Keywords:** Hetero-junction bipolar transistors (HBTs), terahertz technologies, electrothermal modeling, mutual thermal coupling, intra-device coupling, inter-device coupling, device to circuit interactions, ring oscillator, propagation gate delay, power amplifier, multi-finger transistor, thermal resistance, thermal capacitance, thermal impedance, semiconductor device characterizations, pulse measurements, semiconductor device modeling, thermal TCAD simulation



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## Chapter 1 General introduction

The lecture of Richard Feynman [1] in 1959 “There is plenty of room at the bottom” predicts “an enormously greater range of properties that substances can have, and of different things that we can do” if we can arrange atoms and molecules in the way we want. Indeed, since the invention of the first transistor in 1947 (see Figure 1.1), semiconductor industry has witnessed exceptional growth and achievements in integrated circuit (IC) manufacturing. Until now, transistor scaling has driven the chip performance by even accelerating the Moore's law [2]. But will it last forever [3] or will transistors reach their limiting size within a decade? In order to predict the challenges of Moore's law, the International Technology Roadmap for Semiconductors (ITRS) [4] gives an outlook 15 years into the future.

The further down scaling of device dimensions leads to higher operating frequencies that open a new spectrum of future terahertz applications. In this chapter, a general introduction is given comparing different competing THz technologies. In particular, the future prospects of silicon germanium (SiGe) heterojunction bipolar transistor (HBT) technology are discussed. Ultimate limits are illustrated with special focus on the thermal issue which is one of the main motivations of this work. When the integration level further increases, the power density on a chip becomes a critical issue [5]. The maximum power per chip is limited without using expensive cooling systems. Innovative solutions are required otherwise the power dissipation constraints limit the integration level and not device physics or economics [3].

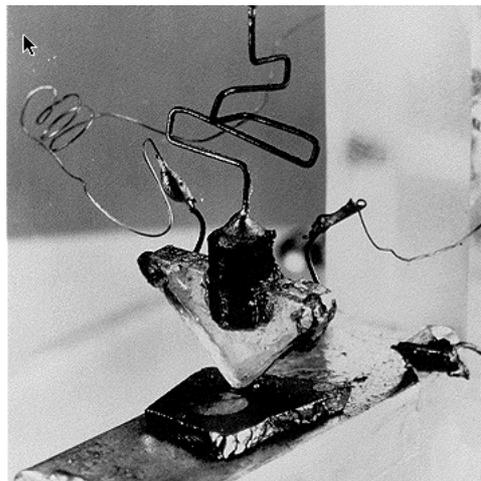


Figure 1.1: First transistor (two gold point contacts were applied to a crystal of germanium) invented at AT&T's Bell Labs in 1947.

## 1.1 From RF to THz

### 1.1.1 THz applications

The terahertz (THz) region as part of the electromagnetic spectrum lies between microwaves and infrared light, which is typically referred to frequencies from 300GHz up to 3THz [6], although there is no stated convention. Terahertz waves can penetrate various materials (clothing, plastic, ceramics, etc.) as well as tissue with low water content (Millimeter wave dosimetry of human skin). Unlike X-rays, THz radiation is not ionizing, and, therefore, probably causes no damage to live biological tissues.

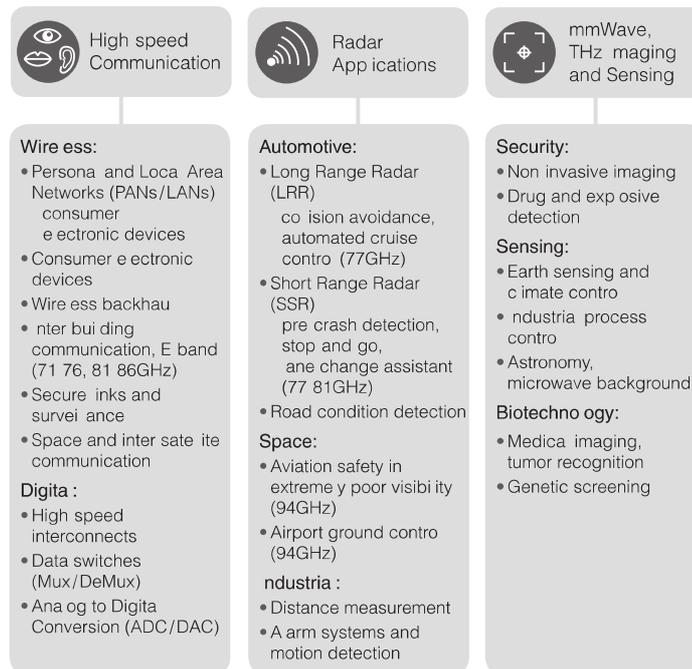


Figure 1.2: Potential applications for silicon integrated mm-wave and THz circuits. Figure taken from [7].

These characteristics allow a large number of new innovative applications [8] (see Figure 1.2) in the field of THz imaging and sensing for biology and medical sciences [9]–[11], non-destructive evaluation [12], [13], homeland security [14], [15]. Moreover, ultra high-speed communication systems at THz frequencies [16], [17] will be attractive for the professional as well as the consumer market. THz radiation imaging technology was selected as one of the "10 emerging technologies that will change your world" by MIT's magazine "Technology Review" (31 January 2004). The large variety of useful THz applications will be driving force for the economy to develop new or enhance existing technologies.

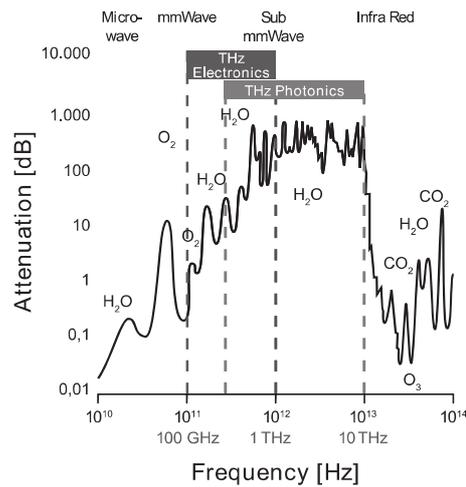


Figure 1.3: The atmospheric attenuation at terahertz frequencies shows the challenges of signal generation and detection for THz electronics and photonics. Figure taken from [18].

However, with currently available and practical THz detectors and sources, measurements over distances larger than 20m are very difficult. THz waves are not very useful for long-range communications [19]. The attenuation level in the earth atmosphere for THz waves (see Figure 1.3) is higher than for the neighboring bands. The lack of suitable devices to generate, detect, or properly process THz signals is the so called THz-gap.

### 1.1.2 The THz-gap

Generating THz signals with sufficient output power is exceptionally challenging. In Figure 1.4, the output power achieved with conventional sources is illustrated. Designers try to close the THz-gap from the low frequency edge with electric sources (upward approach) and also from the high frequency edge with photonic sources (downward approach). In solid state devices (e.g. transistors, Gunn oscillators, Schottky diodes frequency multipliers etc.), THz radiation is generated through the motion of free carriers in the bulk or at the surface. Photonic sources such as laser diodes generate THz radiation through oscillating bound charges. The output power rapidly drops from either side of the spectrum. As shown in Figure 1.4, between 1THz and 10THz there is no conventional source available. Electronic sources like transistors or multipliers can go up to 1THz at room temperature [20], [21]. Conventional laser diodes can easily generate signals at very high frequencies, but not below 10THz [22].

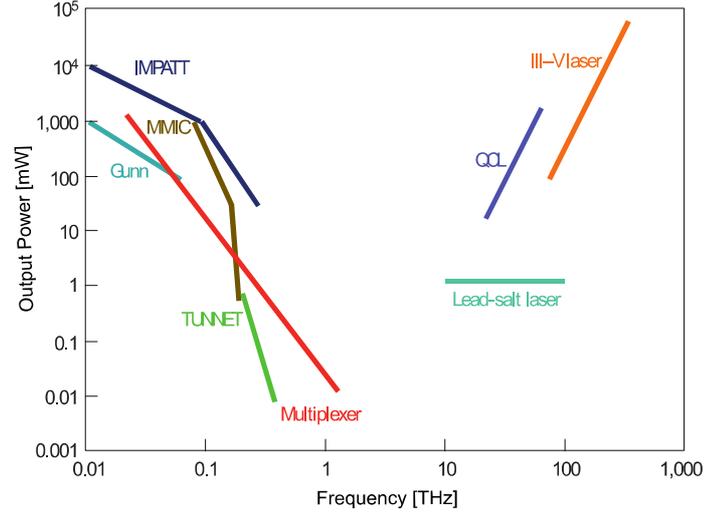


Figure 1.4: THz-emission power as a function of frequency for the conventional THz sources; IMPATT diode stands for impact ionization avalanche transit-time diode, MMIC stands for microwave monolithic integrated circuit, TUNNET stands for tunnel injection transit time [23] and the multiplexer is a Schottky barrier diode (SBD) frequency multiplier, OCL stands for quantum cascade laser. Figure taken from [8].

There are two fundamental reasons for these restrictions that can be explained with the help of the Maxwell equations. First, the term that defines the generation of electromagnetic waves has to be confined. The Maxwell–Faraday equation

$$\nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t} \quad (1.1)$$

connects the electric field  $\vec{E}$  and the magnetic field  $\vec{B}$ . It describes the propagation of electromagnetic waves without any source term. The Gauss laws defined as

$$\nabla \cdot \vec{B} = 0 \quad (1.2)$$

and

$$\nabla \cdot \vec{D} = \rho \quad (1.3)$$

describe only the static fields. The only equation that contains sources for generating electromagnetic waves is the Ampère's circuital law (with Maxwell's correction)

$$\nabla \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t} \quad (1.4)$$

where  $\vec{H}$  is the magnetic field,  $\vec{J}$  is the current density and  $\vec{D}$  is the electric displacement field. This is more obvious in the following form

$$\nabla \times \vec{H} = \left( \vec{J} + \frac{\partial \vec{P}}{\partial t} \right) + \epsilon_0 \frac{\partial \vec{E}}{\partial t} \tag{1.5}$$

where  $\epsilon_0$  is the vacuum permittivity and  $\vec{P}$  is the density of the permanent and induced electric dipole moments in the material or the polarization density.  $\vec{J}$  represents the conduction current in electronic sources. Photonic sources are based on the term  $\partial \vec{P} / \partial t$  that represents the displacement current of oscillating charges. The first term is restricted by a high frequency limit whereas the latter is restricted by a low frequency limit.

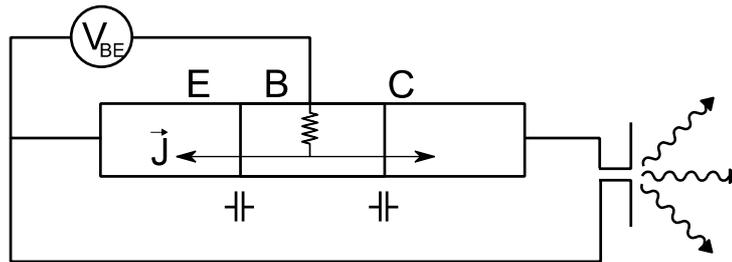


Figure 1.5: Illustration of a bipolar transistor with an antenna.

In Figure 1.5, a simplified illustration of a conventional electronic source is shown including a bipolar transistor connected with an antenna. The AC voltage  $v_{BE}$  creates an alternating conduction current,  $\vec{J}$ . The input signal is amplified and then transmitted over the antenna. Electrical sources are limited by the transit time  $\tau_f$  of the transistor, which is the amount of time an electron needs to go from the emitter to the collector. Moreover, in every circuit there are unavoidable resistances and capacitances. Due to these limitations, the output power drops significantly at very high operating frequencies as shown in Figure 1.4.

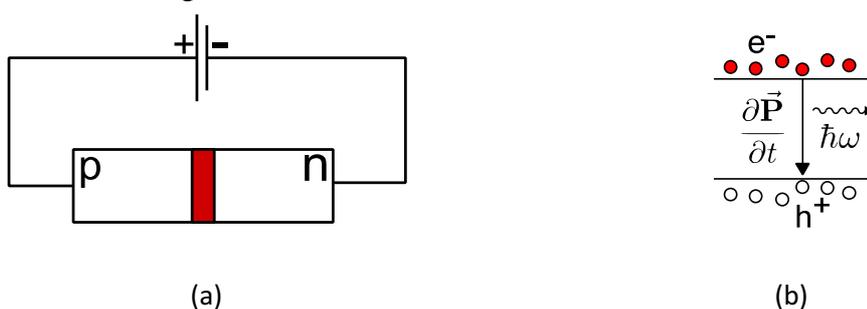


Figure 1.6: (a) Bipolar laser diode. (b) Bandgap – generation of free charges through light.

In Figure 1.6a, an illustration of a bipolar laser diode is shown as an example for a conventional photonic source. The forward bias across a pn diode creates population inversion at the pn junction which means that more carriers are in an excited state than in lower energy states. Electron ( $e^-$ ) hole ( $h^+$ ) pairs oscillate and generate a displacement current  $\partial \vec{P} / \partial t$  which produces radiation. Optical sources are not restricted by the trans-

it time or RC roll off. However the frequency of radiation is limited by the energy bandgap which is greater than 40meV (even for lead-salt materials), meaning that the frequency of radiated light lies above 10THz.

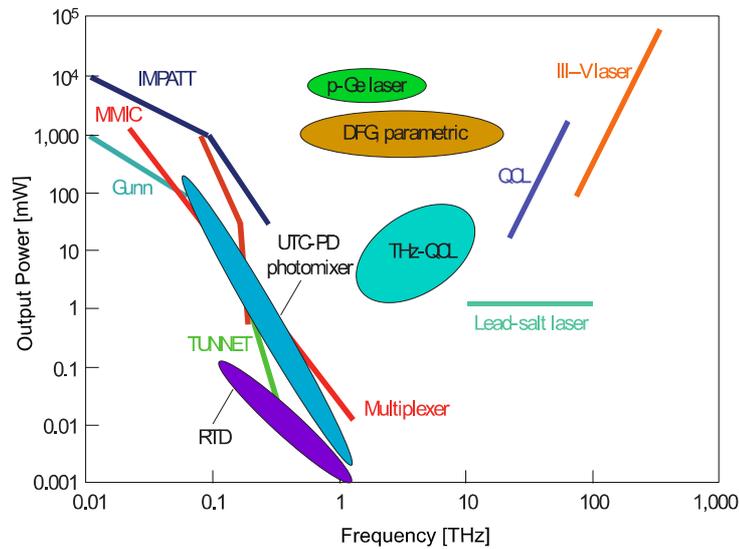


Figure 1.7: THz-emission power as a function of frequency. Solid lines are for the conventional THz sources. Ovals denote recent THz sources; RTD stands for resonant tunneling diodes, UTC-PD stands for uni-travelling carrier photodiode, DFG stands for difference-frequency generation. Figure taken from [8].

These two examples should illustrate the problems that have to be dealt with in order to generate THz signals with sufficient output power. However, recent technological innovations in photonics and nanotechnology have led to the realization of THz devices. Many innovations in photonics have been published recently such as the development of terahertz quantum cascade lasers (QCL) [22], the uni-travelling carrier photodiode (UTC-PD) [24] and the resonant tunneling diodes (RTDs) [25].

A THz QCL can provide a powerful continuous-wave THz source above 1 THz. The three main operational methods for THz QCLs are bound-to-continuum, interlaced and resonant phonon. Another promising device is the UTC-PD that can produce THz waves through photomixing of two laser diodes. RTDs can generate THz waves via tunneling of electrons through some resonant states at certain energy levels. RTDs provide only a limited power. As THz detectors, deuterated triglycine sulphate (DTGS) crystals, bolometers, Schottky barrier diodes (SBDs) and superconductor–insulator–superconductor (SIS) junctions are widely used [26]–[28], and their performance have improved steadily.

Photonic devices are currently the main focus of terahertz research. However, these devices still have to be cooled that results in high fabrication costs and low level of integration. Therefore, the upward approach is the preferred method for portable applications.

### 1.1.3 Comparison of low cost solid state technologies for THz circuits

Due to significant improvements in the high frequency performance, low cost solid state technologies tend to be a promising alternative for realizing THz systems. High frequency diodes are widely employed as sources e.g. impact avalanche transit time (IMPATT) diodes [29], Gunn diodes, and resonant tunneling diodes (RTDs) and as detectors e.g. SBDs. But the range of applications is limited due to their passive behavior. Transistors can be better integrated in multistage systems than diodes. Using a low noise amplifier (LNA) for detection reduces the noise figure (NF) and increases the overall gain of the system [30]. Therefore, a main focus lies on the development of high speed transistors integrated in complementary metal oxide semiconductor (CMOS) or in III-V technologies.

Two main figures of merit (FoMs), the transit frequency  $f_T$  and the maximum oscillation frequency  $f_{max}$ , are often used in order to estimate the performance of a transistor.  $f_T$  is the unity gain cut-off frequency in the common emitter configuration which is the frequency where the extrapolated small-signal current gain  $\beta_F$  (Figure 1.8a) equals one.

$$|\beta_F(f = f_T)| = \left. \frac{dI_C(f_T)}{dI_B(f_T)} \right|_{V_{CE}} = 1 \quad (1.6)$$

$f_T$  can be calculated accurately from y-parameters [31]

$$f_T = \frac{f_{Meas}}{\Im \left\{ \begin{array}{c} Y_{11} \\ Y_{21} \end{array} \right\}} \quad (1.7)$$

according to [32].  $f_{max}$  is defined as the frequency at which the unilateral power gain (or Mason's invariant gain)  $U$  (Figure 1.8b) becomes unity [33].

$$|U(f = f_{max})| = 1 \quad (1.8)$$

$$U = \frac{|Y_{21} - Y_{12}|}{4(\Re\{Y_{11}\}\Re\{Y_{22}\} - \Re\{Y_{12}\}\Re\{Y_{21}\})} \quad (1.9)$$

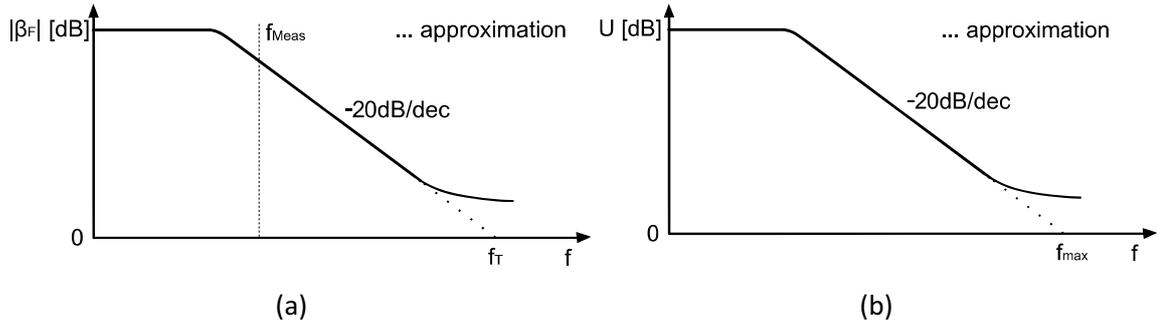


Figure 1.8: Illustration of (a) the small-signal current gain  $\beta_F$  and (b) the unilateral power gain  $U$  vs. frequency  $f$ .

Generally,  $f_{\max}$  is a more relevant parameter for analog and radio frequency (RF) circuit designers [30]. However, it is more sensitive to the device layout and its extraction is less reliable than that of  $f_T$ . Therefore,  $f_T$  is more often used for comparisons between technologies. Published records of  $f_T$  or  $f_{\max}$  are difficult to interpret, since they are correlated. It is possible to achieve a high  $f_T$  but at the expense of a low  $f_{\max}$  and vice versa. For example, reducing the base width of a bipolar transistor, on the one hand, results in a lower transit time that causes a higher  $f_T$ , but on the other hand, the increased (external) base resistance reduces the  $f_{\max}$ . Examples for state of the art performance records for solid state technologies are listed in Table 1 and illustrated in

Technology	CMOS	SiGe HBT	III-V HEMT	III-V HBT
$f_T/f_{\max}$	485GHz/? [34]	410GHz/150GHz [35]	644GHz/681GHz [36]	765GHz/227GHz [37]
$f_T/f_{\max}$	395GHz/410GHz [38]	300GHz/500GHz [39]	385GHz/1200GHz [40]	430GHz/800GHz [41]

Table 1: Published records for state of the art CMOS, BiCMOS and III-V technologies.

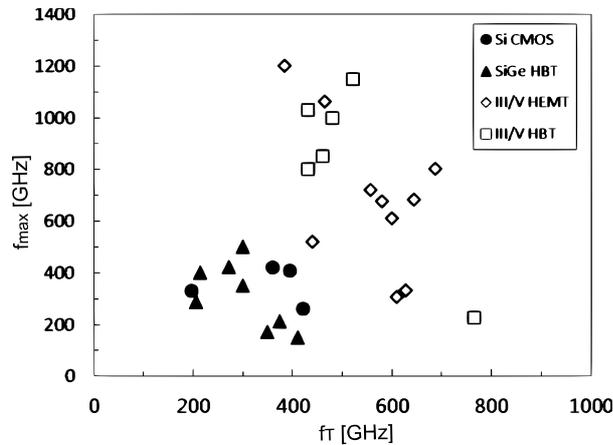


Figure 1.9: Recent trend of device operation speed in terms of  $f_{\max}$  and  $f_T$ . Figure taken from [42].

III-V devices tend to have a superior performance compared to Si devices due to higher carrier mobilities. The high speed of III-V transistors comes along with an excellent noise figure (NF). However, the high fabrication costs due to expensive and small wafers and the poor reliability are not attractive for high volume applications. The hole mobility of III-V devices is worse in comparison to silicon. Hence, complementary logic blocks as in CMOS technology are rather hard to realize. Moreover, due to high thermal resistance the integration level is much lower than for silicon. The power-handling capability on Si is 3.5 and 2.7 times as large as that on GaAs and InP substrates, respectively [43]. These arguments make silicon even with less performance the favorable technology for large scale applications. High performance SiGe HBTs integrated in a BiCMOS technology seem to be a promising solution.

## 1.2 SiGe HBT technology

### 1.2.1 General overview

SiGe HBTs provide a higher current driving capability, higher linearity, larger transconductance  $g_m$ , lower  $1/f$  noise property, excellent reliability, better device matching and superior performance in comparison to standard silicon metal oxide semiconductor field effect transistors (MOSFETs). This makes them ideal devices for microwave power applications [44], [45]. Therefore, several companies have chosen to integrate their high performance SiGe HBTs in a lower cost CMOS process (BiCMOS) which allows an improved functionality but at the same time increases process complexity due to HBT integration.

In contrast to high speed III-V technologies (with  $f_{max}$  exceeding 1.2THz [40]) the intrinsic material properties of Si limits the device operation speed. Nevertheless, operation frequency can be increased by adoption of frequency multipliers [46] and plasma wave detectors [47] to enable circuit operation beyond  $f_{max}$ . Moreover, SiGe HBT technology continues to gain momentum as shown in Figure 1.10. Optimized device structure along with aggressive scaling lead to comparable performance as III-V devices ( $f_T=300\text{GHz}$ ,  $f_{max}=500\text{GHz}$  [39]) as reported within the Seventh Framework Programme (FP7) project DOTFIVE [7] (further explanation given in 1.4.3). The follow up project DOTSEVEN is targeting the development of SiGe:C HBTs technologies with cut off frequencies  $f_{max}$  of around 700GHz.

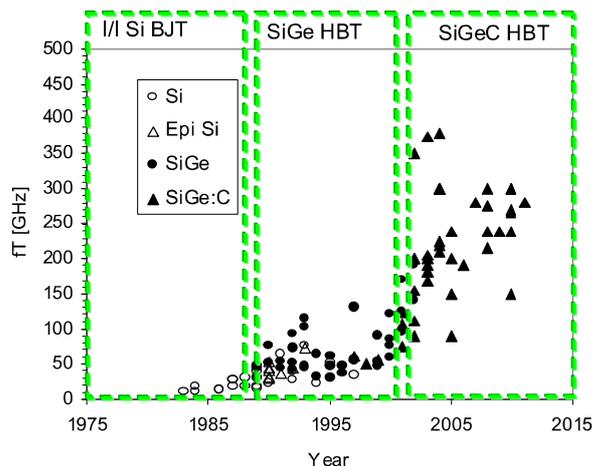


Figure 1.10: Recent trend of SiGe HBT in terms of  $f_T$  (figure taken from [48]).

Future applications require a sufficient output power at high frequencies. A state-of-the-art power density of  $18.5\text{mW}/\mu\text{m}^2$  at 1dB compression was obtained at 94GHz [49] with a B5T SiGe HBT from STMicroelectronics (the same device is also used in this work). Moreover, a 300GHz signal source was demonstrated having an output power of 1.7dBm around 290GHz [50]. In a similar technology (IHP) an 820GHz transceiver chipset for terahertz active imaging applications was fabricated [46]. In this work, a record gate delay of 1.65ps is demonstrated [51]. This opens the door for terahertz (THz) applications [52] that can be mass-produced in a cost-effective way.

### 1.2.2 Ultimate limits

There have been a number of attempts to predict the ultimate performance of SiGe HBTs [53], [54] using advanced device simulation tools. Recently, a more rigorous approach was presented by M. Schröter et al. [55], [56]. In [55] an ultimate vertical doping profile was developed only based on physical- and application-oriented considerations. The resulting device structure has a peak transit frequency  $f_T$  close to 1.5THz at  $V_{BC}=-1\text{V}$ . The most important limiting factor was seen to be the high current density ( $100\text{mA}/\mu\text{m}^2$  at peak  $f_T, f_{max}$ ) in the metal contacts that can cause reliability issue due to electromigration (especially of the contact vias).

For a given semiconductor, the Johnson's approach [53] allows calculating the ultimate power performance of an electronic device. However, due to self-heating the device performance at such a high power density is often limited by thermal effects before the electronic limitations of the semiconductor are reached [57]. Future trends like 3-D integrated circuits (ultimate density limit) [58] further aggravate the thermal issue due to increased mutual heating effects (e.g. mutual thermal coupling).

## 1.3 Problem statement: The thermal issue

### 1.3.1 General overview

Higher device performance is mainly achieved with downscaling of device dimensions and by improving the device architecture [7], [59], [60]. The higher the speed of advanced HBTs, the higher are their current densities and internal electric fields which leads to increased power dissipation [61]. Structural innovation has contributed to reduce the parasitic elements and to decrease the transit time by introducing shallow trench, deep trench, and other technological process steps [62]. Major improvements are the following: (i) Deep trench isolation improve the RF performance through the reduction of parasitic capacitances and crosstalk [62], [63]. The drawback is that the heat flow is confined within the deep trenches resulting in larger thermal impedance  $Z_{th}$  [64]–[66]. (ii) In order to boost transit frequency  $f_T$ , a lot of attention is paid to carefully design the base–collector (BC) junction and the epitaxial collector. It permits to push the Kirk effect to higher current densities, resulting in a higher  $f_T$  on the one hand, but on the other hand, to lower breakdown voltages. Finally, it shifts the operating point to higher current densities [67].

Both aspects result in a more pronounced self-heating effect leading to higher circuit operating temperatures which affects the circuit performance, the reliability and the packaging costs. Moreover, thermal instabilities can occur due to the positive feedback between collector current  $I_C$  and the device temperature of a bipolar transistor [68], [69].

### 1.3.2 Internal thermal feedback in bipolar transistors

In a first guess, it might be supposed that the collector current would decrease with increasing temperature, however, in contrast to MOS devices, bipolar transistors are driven by minority carriers which have a positive temperature coefficient [68]. At constant base-emitter voltage  $V_{BE}$  and base current  $I_B$ , an increase of collector-emitter voltage  $V_{CE}$  results in higher power dissipation,

$$P_{diss} = I_B V_{BE} + I_C V_{CE} \approx I_C V_{CE} \quad (1.10)$$

and therefore, an increase in Temperature

$$\Delta T \approx R_{th} I_C V_{CE} \quad (1.11)$$

where  $R_{th}$  is the thermal resistance of the device.

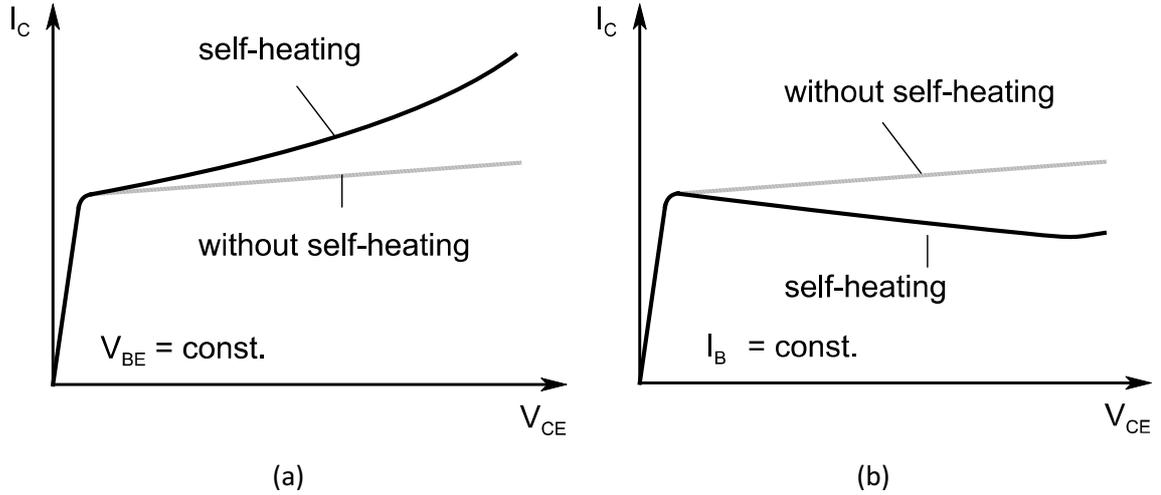


Figure 1.11: Thermal feedback (self-heating) for (a) constant  $V_{BE}$  and (b) constant  $I_B$ .

This is the so called thermal feedback [70]. The slope of the output characteristics at constant  $V_{BE}$  (Figure 1.11a) or constant  $I_B$  (Figure 1.11b) can be described with

$$\frac{dI_C}{dV_{CE}} = \left. \frac{\partial I_C}{\partial V_{CE}} \right|_{T=const.} + \left. \frac{\partial I_C}{\partial T_j} \right|_{V_{CE}=const.} \cdot \frac{dT_j}{dV_{CE}} \quad (1.12)$$

where  $T_j$  is the junction temperature of the transistor. Since

$$\frac{dT_j}{dV_{CE}} = \frac{dT_j}{dP_{diss}} \frac{dP_{diss}}{dV_{CE}} = R_{th} \left( I_C + V_{CE} \frac{dI_C}{dV_{CE}} \right) \quad (1.13)$$

it follows that [71]

$$\frac{dI_C}{dV_{CE}} = \frac{\left. \frac{\partial I_C}{\partial V_{CE}} \right|_{T=const.} + R_{th} I_C \left. \frac{\partial I_C}{\partial T_j} \right|_{V_{CE}=const.}}{1 - R_{th} V_{CE} \left. \frac{\partial I_C}{\partial T_j} \right|_{V_{CE}=const.}} \quad (1.14)$$

which means, that the slope of the output characteristics increases with temperature.

If

$$R_{th} V_{CE} \left. \frac{\partial I_C}{\partial T_j} \right|_{V_{CE}=const.} \rightarrow 1 \quad (1.15)$$

the device is unstable which results in an uncontrolled increase in  $I_C$  (thermal runaway).

This can be critical especially for constant  $V_{BE}$  since temperature coefficient [71]

$$\left. \frac{\partial I_C}{\partial T_j} \right|_{V_{CE}, V_{BE}=const.} \approx \frac{I_C}{T_j} \left( \frac{V_g - V_{BE}}{V_T} + X_{TI} \right) \quad (1.16)$$

is much greater than

$$\left. \frac{\partial I_C}{\partial T_j} \right|_{V_{CE}, I_B = \text{const.}} \approx \alpha_B I_C \quad (1.17)$$

where  $X_{TI}$  is temperature exponent of the saturation current  $I_S$ ,  $V_g$  is the bandgap voltage,  $V_T$  is the temperature voltage and  $\alpha_B$  is the temperature coefficient of the current gain  $\beta_f$ . Thermal runaway would be impossible if the following condition is true [71].

$$P_{diss} \approx I_C V_{CE} < \frac{T}{R_{th}} \frac{V_T}{V_g - V_{BE} + X_{TI} V_T} \quad (1.18)$$

Thermal stability at constant  $V_{BE}$  can be increased with a ballasting resistance  $R_E$  due to the negative voltage feedback. This is especially relevant if several transistors are used in parallel (Figure 1.12) due to thermal coupling effects.

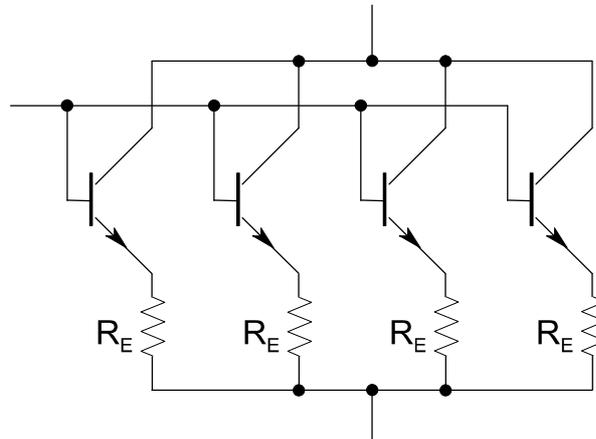


Figure 1.12: Stabilization of parallel bipolar transistors with emitter resistance  $R_E$  in series (figure taken from [71]).

In multi-finger transistors (MFTs) or in multi-transistor arrays (MTAs), temperature rises are mainly caused by self-heating and thermal coupling between neighboring devices. The positive thermal feedback between the heat sources (mainly the base-collector space charge region) results in a temperature distribution across the device as shown in Figure 1.13. At a certain dissipated power, the hottest finger dominates the others becoming hotter. This can lead to thermal runaway and destruction of the device in the worst case. Silicon has a good thermal conductivity; hence, unlike for III-V and SOI technologies, this can result in large thermal gradients across devices designed in close proximity. These wide variations need to be treated in a distributed manner [72].

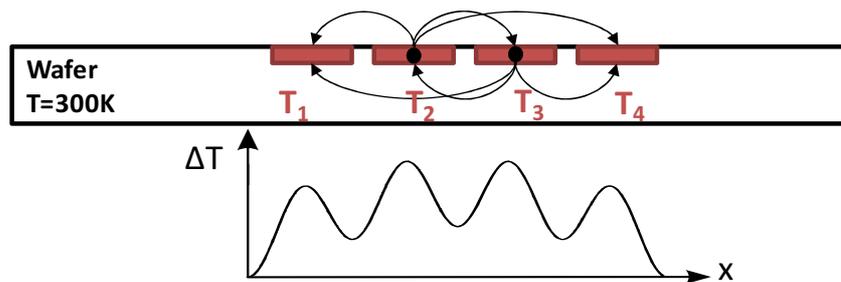


Figure 1.13: Sketch of the temperature distribution in multi-finger transistors (MFTs) or multi-transistor arrays (MTAs) due to positive thermal feedback.

## 1.4 This thesis

### 1.4.1 Motivation

As discussed, scaling in combination with higher integration makes the electrothermal effect one of the key factors limiting the performance, the stability and the reliability of future high power, high frequency applications. Therefore, accurate circuit simulations in terms of device and circuit temperature are mandatory for circuit designers to optimize the thermal performance of their circuits. Hence, compact models are required that take into account the specific circuit layout, for example, the distance between neighboring devices. Modeling engineers need isothermal measurements for accurate determination of model parameters. Transistor compact models should be also verified on circuit level. Sensitivity analysis of device to circuit interactions can be used, for example, to reduce the model complexity or to analyze process variations (see Appendix A.5).

Whether or not thermal issues will limit the speed of future high speed circuits, they must be taken into account in the design phase and so must be accurately predictable and, measurable. In this work, state of the art SiGe HBTs are characterized using DC, AC, pulsed and load pull measurements. Accurate measurement and modeling of the devices' thermal impedance is presented. Circuit simulations are carried out that takes into account the thermal coupling between neighboring devices. Note that the circuit and device measurements were made on the same wafer.

### 1.4.2 Organization and contributions to the state of the art

The thesis is organized as follows:

**Chapter 2: SiGe:C HBT technology and device characterizations** - The chapter provides a brief description of the state of the art SiGe HBT technology from STMicroelectronics and the advanced high-current model (HICUM) for high-frequency bipolar transistors. Compact model parameters are verified with on-wafer measurements.

Contribution: The chapter validates the applicability of the latest version 2.3 of HICUM/L2 (including the new extended formulation of transfer current [73]) for a modern SiGe HBT technology over a large bias and temperature range.

**Chapter 3: Advanced electrothermal device characterization** – The chapter presents advanced measurement and modeling techniques that provide accurate information about the dynamic self-heating effect inside the device as well as the thermal coupling effect between neighboring devices.

Contribution: The chapter validates a novel pulse measurement system that allows state of the art isothermal DC and RF measurements with 100ns pulses.

Publication: “Pulsed I (V)—pulsed RF measurement system for microwave device characterization with 80ns/45GHz”, M. Weiß et al., Solid-State Electronics, vol. 84, pp. 74-82, June 2013.

Contribution: The chapter identifies and evaluates the significant impact of electrothermal intra-device coupling in multi-finger SiGe HBTs using novel, specially designed test structures.

Publication: “Mutual thermal coupling in SiGe: C HBTs”, M. Weiß et al., Conference SBMicro, Sept. 2013, Curitiba, Brazil.

**Chapter 4: Circuit-level electrothermal investigations** - The chapter studies two circuits, electrically and thermally. First, several realizations of a large scale current mode logic (CML) ring oscillator (RO) with 218 transistors are presented. Second, two transistor arrays are operated as 60GHz power amplifiers.

Contribution: The chapter presents layout optimizations of a RO that lead to record gate delay of 1.65ps.

Publication: “Optimized Ring Oscillator With 1.65-ps Gate Delay in a SiGe:C HBT Technology”, M. Weiß et al., IEEE Electron Device Letters, vol. 34, pp. 1214-1216, Oct. 2013.

**Contribution:** The chapter demonstrates accurate thermally coupled circuit simulations of the investigated multi-finger SiGe HBTs.

**Publication:** “Coupled electrothermal circuit simulation for high frequency multi-finger SiGe HBTs”, in progress.

**Chapter 5: Conclusions and recommendations** – Major results of this work are summarized. Finally, it is proposed how the findings of this work can be used within a CAD based circuit design process.

### 1.4.3 Projects

#### *DOTFIVE* [7]

**Objective:** To develop SiGe heterojunction bipolar transistors operating at maximum oscillation frequencies of up to 500GHz at room temperature.

**Year:** 2008-2010 (successfully finished)

**Partners:** The project involves 15 partners from industry and academia in five countries teaming up for research and development work on silicon-based transistor architectures, device modeling, and circuit design: STMicroelectronics (France), Infineon (Germany), IHP (Germany), IMEC (Belgium), XMOD Technologies (France), IMS Laboratory (France), TU Dresden (Germany), University Wuppertal (Germany), Bundeswehr University Munich (Germany), TU Delft (Netherlands), University of Naples (Italy), etc.

#### *RF2THz SiSoC* [74]

**Objective:** To meet the needs of future RF and high-speed equipment, the CATRENE RF2THz project aims to develop silicon technology platforms for emerging RF, millimeter-wave (MMW) and THz consumer applications such as 77/120GHz automotive radars, MMW imaging and sensing, fast measurement equipment, 60GHz wireless networking and fast downloading systems, 400 Gbit/s fibre optics data communications systems, 4G photonic mobile communications and high performance RF wireless communication systems as well as two-way satellite communications systems.

**Year:** 2011-2013 (running)

**Partners:** The project involves 31 partners from industry and academia in five countries teaming up for research and development work on silicon-based transistor architectures, device modeling, and circuit design: STMicroelectronics (France), NXP Semiconductors (France, Netherlands), IHP (Germany), Alcatel Lucent (Germany), BOSCH (Germany), Agilent Technologies (Germany), XMOD Technologies (France), IMS Laboratory (France), TU Dresden (Germany), Fraunhofer (Germany), TU Delft (Netherlands), TU Eindhoven (Netherlands), ESIEE (France), ENSICAEN (France), IEMN (France), NEWTEC(Belgium) etc.

***DOTSEVEN*** [75]

**Objective:** To develop SiGe heterojunction bipolar transistors operating at maximum oscillation frequencies of up to 700GHz at room temperature.

**Year:** 2012-2014 (running)

**Partners:** The project involves 14 partners from industry and academia in six countries teaming up for research and development work on silicon-based transistor architectures, device modeling, and circuit design: Infineon (Germany), Dice Danube Integrated Circuit Engineering (Austria), IHP (Germany), XMOD Technologies (France), IMS Laboratory (France), TU Dresden (Germany), University Wuppertal (Germany), TU Delft (Netherlands), University of Naples (Italy), etc.



## **Chapter 2 SiGe:C HBT technology and device characterization**

### **2.1 Introduction**

Modern SiGe HBT technology continues to gather momentum due to its use for a wide variety of high frequency applications. These applications require advanced process technologies in combination with a reliable process design kit (PDK) that contains accurate models of the devices fabricated in the underlying process.

The chapter is organized as follows: First, a state of the art SiGe HBT technology from STMicroelectronics is presented. The fabricated devices exhibit a maximum peak transit frequency  $f_T$  of 320GHz and a peak maximum oscillation frequency  $f_{max}$  of 400GHz. Second, the advanced high-current model (HICUM) is introduced that addresses the new challenges for such an advanced technology. Moreover, compact model parameters are validated with experimental results. The test bench for measuring DC and S parameters is explained and on-wafer measurements are compared to transistor simulations.

## 2.2 SiGe:C HBT technology from STMicroelectronics

Within DOTFIVE, the developments of STMicroelectronics are based on a state of the art 130nm SiGe BiCMOS technology optimized for very high frequency applications (BiCMOS9MW) [76]. The back-end of line (BEOL) includes six copper metallization scheme with two 3 $\mu$ m thick levels to reduce the signal attenuation  $\alpha$  at 80GHz to 0.6dB/mm [59]. A scanning electron microscope (SEM) picture illustrating main BiCMOS9MW process features taken from [59] is shown in Figure 2.1. The high speed HBTs have a peak transit frequency  $f_T$  of 220GHz and a peak maximum oscillation frequency  $f_{max}$  of 280GHz.

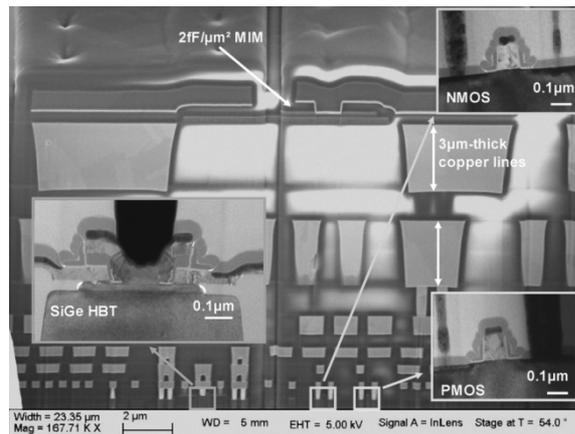


Figure 2.1: SEM picture illustrating main BiCMOS9MW process and device features. Figure taken from [59].

In order to meet the goals of the DOTFIVE project process capabilities were analyzed and CMOS integration constraints were left aside. Vertical and horizontal scaling was achieved by modifying collector doping, SiGe:C/Si base profile, inside spacer width, process thermal budget and device layout rules to optimize the device performances (see Figure 2.2). This has led to the B3T, B4T [77] and B5T [45] SiGe HBT technologies, with  $f_T/f_{max}$ =260/330GHz, 270/370GHz and 300/400GHz, respectively. These technologies were available to DOTFIVE partners for modeling and circuit design purposes. Figure 2.3 summarizes the various steps in the optimization from BiCMOS9MW to B4T.

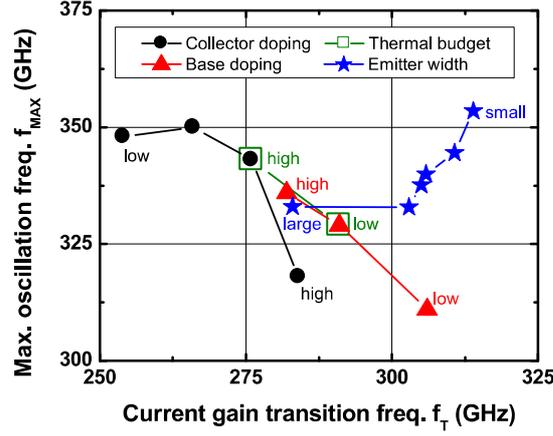


Figure 2.2:  $f_{max}$  vs.  $f_T$  chart of CBEB Si/SiGe:C HBTs featuring different vertical profiles and emitter widths  $L_E=5\mu\text{m}$ . Figure taken from [45].

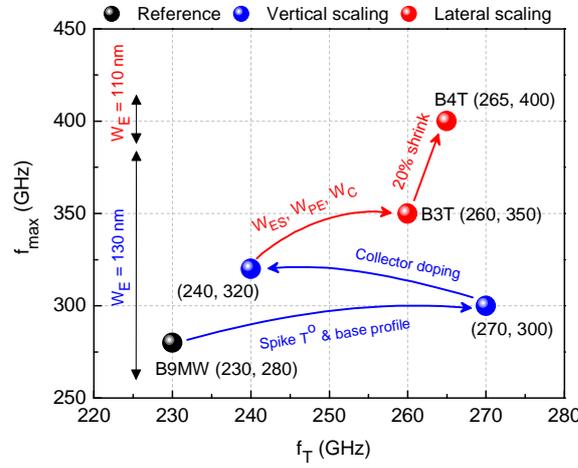


Figure 2.3: From BiCMOS9MW to B3T and B4T technology. Figure taken from [59].

Finally, the effective emitter width was optimized to 120nm in the B5T technology. Note that in this work, the effective emitter area is defined as the drawn emitter window minus the area of the inner spacers. The area reduction also helped to minimize the base resistance  $R_B$ , the collector resistance  $R_C$ , the collector-base capacitance  $C_{CB}$  and the collector-substrate capacitance  $C_{CS}$ . Figure 2.4 shows the double-polysilicon fully self-aligned (FSA) selective epitaxial growth (SEG) HBT. The Si/SiGe:C HBTs feature a self-aligned double-polysilicon architecture with a selective epitaxial growth (SEG) of the base. The process, based on a 120-nm CMOS core process, uses a standard collector module (n+ buried layer, thin collector epitaxy and collector sinker), a selective implanted collector, a boron doped SEG SiGe:C base and an arsenic in-situ doped mono-emitter. BEOL (as in BiCMOS9MW) consists of 6 copper levels, the upper two being 3- $\mu\text{m}$  thick.  $BV_{CBO}$  and  $BV_{CEO}$  are 5.3V and 1.5V, respectively. The devices exhibit a pinched base resistance of 1.8k $\Omega$ /sq and a current gain  $\beta$  of around 1300 at  $V_{BE}=0.7V$ . Furthermore, a record output power [49] of 18.5mW/ $\mu\text{m}^2$  at 1dB compression point, accompanied by a PAE of 25% was achieved.

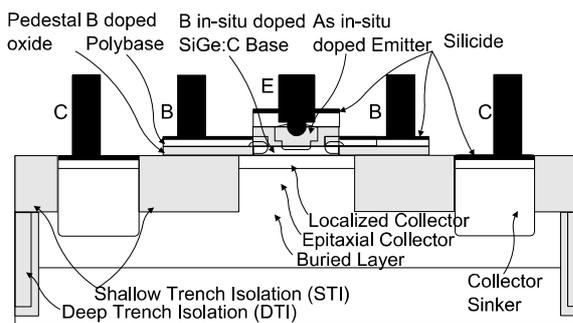


Figure 2.4: Sketch of the FSA-SEG SiGe HBT architecture. Figure taken from [77].

### 2.3 A compact model for high frequency HBTs

A compact model should be a physics-based mathematical description of the electrical behavior of a device for use in a circuit simulator. There is a large demand for fast and reliable compact models that are accurate for a great variety of technologies. A “good” compact model provides high accuracy over a wide electrical (and temperature) range, laterally scalable parameter calculation, numerical stability and fast execution time. Furthermore predictive and statistical modeling as well as a reliable and well-defined extraction procedure should be available. All these requirements are addressed by the compact model HICUM.

HICUM (High-Current Model) [31] is a scalable physics-based compact bipolar transistor model taking into account the high current effects which are significant for certain high speed transistor applications. The first version was introduced in 1986 by H.M. Rein and M. Schröter and arrived in the public domain since 1999. It is now a Compact Model Council (CMC) [78] standard model and integrated in a wide range of simulators like ADS, ELDO, SPECTRE, HSPICE, GoldenGate, etc. HICUM is based on an extended and generalized integral charge-control relation (GICCR). However, in contrast to the (original) Gummel-Poon model, in HICUM the GICCR concept is applied without simplifications and additional fitting parameters (such as the Early voltages). Therefore it allows a reliable design and circuit optimization. Some of the important physical effects taken into account by HICUM/L2 are briefly summarized below [79]:

- high-current effects (incl. quasi-saturation)
- distributed high-frequency model for the external base-collector region
- emitter periphery injection and associated charge storage
- emitter current crowding (through a bias dependent internal base resistance)
- two- and three-dimensional collector current spreading
- parasitic capacitances between base-emitter and base-collector terminal
- vertical non-quasi-static (NQS) effects for transfer current and minority charge

- temperature dependence and self-heating
- weak avalanche breakdown at the base-collector junction
- tunneling in the base-emitter junction
- parasitic substrate transistor
- band-gap differences (occurring in HBTs)
- lateral (geometry) scalability

### 2.3.1 General overview

HICUM is based on a description of the GICCR [80] from which the transfer current  $i_T$ , is modeled as

$$i_T = \frac{c_{10}}{Q_{p,T}} \left( e^{\frac{v_{B'E'}}{V_T}} - e^{\frac{v_{B'C'}}{V_T}} \right) \quad (2.1)$$

with the GICCR constant

$$c_{10} = (qA_E)^2 V_T \overline{\mu_{nB} n_{iB}^2} \quad (2.2)$$

and the weighted hole charge  $Q_{p,T}$  is expressed as

$$Q_{p,T} = Q_{p0} + h_{jEi} Q_{jEi} + h_{jCi} Q_{jCi} + Q_{f,T} + Q_{r,T} . \quad (2.3)$$

$v_{B'E'}$  and  $v_{B'C'}$  are the (time dependent) terminal voltages,  $V_T$  is the thermal voltage,  $Q_{p0}$  is the zero-bias hole charge,  $Q_{jEi}$  and  $Q_{jCi}$  are the base-emitter (BE) and base-collector (BC) depletion charges of the internal transistor.  $h_{jEi}$  and  $h_{jCi}$  are the weighting factors that take into account bandgap and mobility variations within the structure of HBTs. The weighted diffusion charges  $Q_{f,T}$  and  $Q_{r,T}$  are calculated from the integral of the forward and reverse transit time.

The transit time of the entire transistor can be determined by the change of the minority charges  $Q_p$  in dependence of the collector current  $I_C$

$$\left. \frac{dQ_p}{dI_C} \right|_{V_{CE}} = \tau_f = \tau_E + \tau_{BE} + \tau_B + \tau_{BC} + \tau_C \quad (2.4)$$

The transit time consists of different parts according to the neutral and space-charge regions of the transistor. The bias dependence of the forward transit time is described in HICUM through

$$\tau_f(V_{C'E'}, i_{Tf}) = \tau_{f0}(V_{B'C'}) + \Delta\tau_f(V_{C'E'}, i_{Tf}) \quad (2.5)$$

where  $\tau_{f0}$  is the low-current component, and  $\Delta\tau_f$  represents the increase of the transit time at high collector current densities. At low current densities, the transit time (Figure 2.5) is modeled as nearly constant.

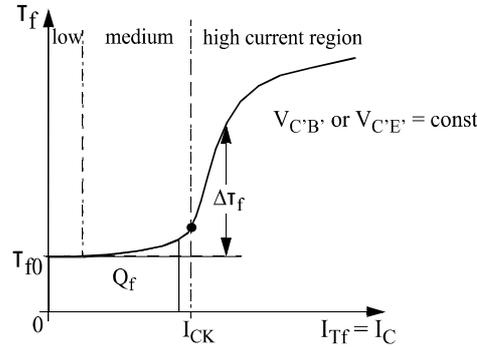


Figure 2.5: Illustration of the forward transit time  $\tau_f$  as function of collector current  $I_C$ . Figure taken from [31].

The critical current  $I_{CK}$  characterizes the onset of high current effects. When the minority charge density exceeds the doping-induced charge density in the base collector space charge region (SCR), the SCR is further widened into the collector due to its lower doping level (base push-out or Kirk effect). This reduces the electrical field at the base-collector junction. The electrons no longer move through the collector with saturation velocity, and therefore, the transit time  $\tau_f$  rises strongly.  $\tau_f$  can be extracted from the measured transit frequency  $f_T$  versus collector current  $I_C$  for different voltages  $V_{CE}$  or  $V_{BC}$  using

$$\frac{1}{2\pi f_T} = \tau_f + \left( r_{Cx} + r_E + \frac{r_B}{\beta_0} \right) C_{BC} + \frac{C_{BC} + C_{BE}}{g_m} \quad (2.6)$$

where  $r_{Cx}$  is the external collector resistance,  $r_E$  is the emitter resistance,  $r_B$  is the base resistance,  $\beta_0$  is the low-frequency small-signal current gain,  $C_{BC}$  is the base-collector capacitance and  $C_{BE}$  is the base-emitter capacitance. The voltage dependent parts are combined in the low-current forward transit time  $\tau_{f0}$  (Figure 2.6).

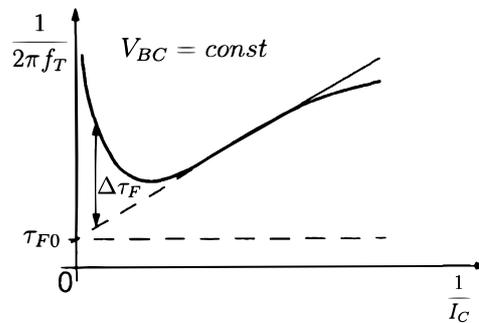


Figure 2.6: Extraction of transit time  $\tau_f$  measured transit frequency  $f_T$ .

Depletion capacitances, transit time of carriers as well as the associated charges as a function of bias mainly determine the dynamic behavior of the transistor. These are

basic quantities in HICUM. Hence, the small-signal, the large-signal and the DC behavior are described very accurately with a single set of parameters. Through the coupling of static and dynamic behavior, the fitting parameters like Early voltages and knee currents in SGPM are not required anymore. In order to reflect the physically independent mechanism of base and collector currents all base currents are modeled independently of the transfer current.

The HICUM large signal equivalent circuit is shown in Figure 2.7. The internal transistor has the four nodes E', B', B\* and C'. The internal circuit consists of the diode current  $i_{jBEi}$  and the depletion charge  $Q_{jEi}$  of the base-emitter (BE) junction, the diode current  $i_{jBCi}$  and the depletion charge  $Q_{jCi}$  of the base-collector (BC) junction, and the voltage controlled transfer current source  $i_T$ . Furthermore, the minority charge is represented by its forward and reverse component,  $Q_f$  and  $Q_r$ . In addition, breakdown in the BC SCR is taken into account by the avalanche current source,  $i_{AVL}$ , and possible tunneling through the BE SCR is represented by  $i_{BEti}$ . By comparing with the equivalent circuit of SGPM, there are two additional nodes named B\* and S' in HICUM. The node B\* has been added to separate the internal base resistance  $r_{Bi}$  (bias dependent) from the external component  $r_{Bx}$ . The internal substrate node S' is connected to the substrate network with the capacitance  $C_{Su}$  and the resistance  $r_{Su}$ . Moreover, an emitter-base isolation capacitance  $C_{BEpar}$  as well as a base-collector oxide capacitance  $C_{BCpar}$  is taken into account.

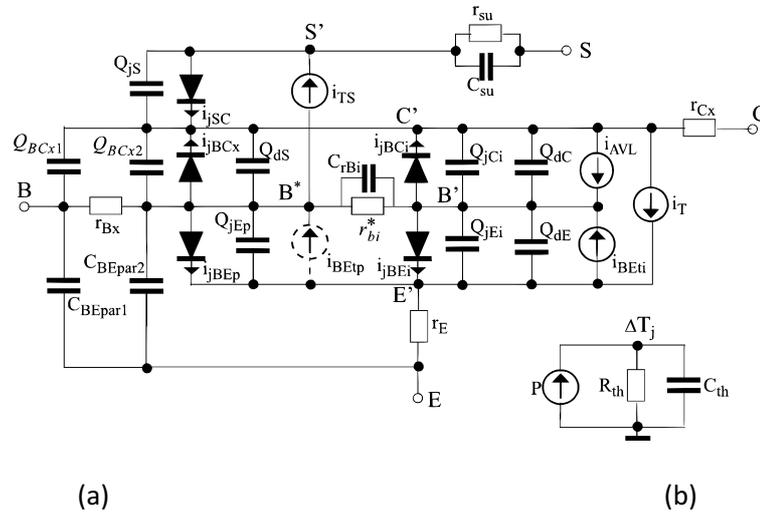


Figure 2.7: a) Large-signal HICUM/L2 equivalent circuit. b) Thermal network used for self-heating calculation (figure taken from [31]).

### 2.3.2 The self heating model

Heat is generated in all active areas of a device which results in an increase of the device temperature. Self-heating leads to a shift in device characteristics and can be described with an electrical equivalent circuit. The simplest form for calculating the

increase  $\Delta T_j$  of the junction temperature is a single pole sub-circuit consisting of one thermal resistance  $R_{th}$  and one thermal capacitance  $C_{th}$  shown Figure 2.7b. The current source corresponds to the dissipated power  $P_{diss}$  and represents the amount of heat that is generated by the device.

$$P_{diss} = V_{BE} I_B + V_{CE} I_C \quad (2.7)$$

The voltage node corresponds to the temperature rise  $\Delta T$

$$\Delta T = T_j - T_{amb} = P_{diss} R_{th} \quad (2.8)$$

where  $T_j$  and  $T_{amb}$  are the junction and ambient temperatures respectively. The units for  $R_{th}$  and  $C_{th}$  is K/W and Ws/K, respectively. The thermal time constant is the product of the  $R_{th}$  and  $C_{th}$ .

$$\tau_{th} = R_{th} C_{th} \quad (2.9)$$

In other words it is the time required for a transistor to change 63.2% of the total difference between its initial ( $T_{amb}$ ) and final junction temperature ( $T_j$ ) when subjected to a step function change in temperature. Note that this is a very basic simplification.

The thermal network and the transistor model are solved together for each DC and transient operation. The temperature dependent model parameters are calculated taking into account the voltage of the temperature node. Furthermore, this node can be connected with an external network consisting of thermal resistances and capacitances that describe the thermal device behavior more accurately (internal  $R_{th}$  and  $C_{th}$  should be deactivated). This option is further explained in the following chapters where it is used to improve the accuracy of the thermal impedance and to consider thermal coupling between neighboring devices.

In HICUM,  $P_{diss}$  is calculated from all relevant dissipative elements in the equivalent circuit if the self-heating flag  $fl_{SH}=2$  [31]

$$P_{diss} = |I_T V_{C'E'}| + |I_{AVL} V_{B'C'}| + \sum \frac{|\Delta V_n|^2}{R_n} + |I_{TS} V_{B^*S}| \quad (2.10)$$

where  $I_{AVL}$  is the avalanche current,  $I_{TS}$  is the substrate current,  $R_n = \{r_{Bi}, r_{Bx}, r_E, r_{Cx}\}$  are the series resistances and  $\Delta V_n$  the corresponding voltage drop across those resistances. However, considering all dissipative elements can further increase the computational effort. The setting  $fl_{SH}=1$  includes only the most relevant dissipative elements in the power calculation

$$P_{diss} = |I_T V_{C'E'}| + |I_{AVL} V_{B'C'}|. \quad (2.11)$$

Note that simulation results can be different depending on whether  $fl_{SH}$  is set to 1 or 2 as shown in the following example (see Figure 2.8). After a delay of 10ns, a transient voltage pulse of 0.95V is applied at the base of a transistor model (B5T HBT with drawn emitter area  $A_E=0.18 \times 5 \mu\text{m}^2$ ) with the emitter resistance  $r_E=5.3\Omega$  and external collector resistance  $r_{CX}=11.5\Omega$ .  $V_{CE}$  stays constant at 1.5V. The thermal network consists of  $R_{th}=4000\text{K/W}$  and  $C_{th}=2.9\text{pWs/K}$ , thus resulting in a thermal time constant  $\tau_{th}=11.6\text{ns}$ . The obtained transient temperature rises for  $fl_{SH}=1$  and  $fl_{SH}=2$  are displayed in Figure 2.8.

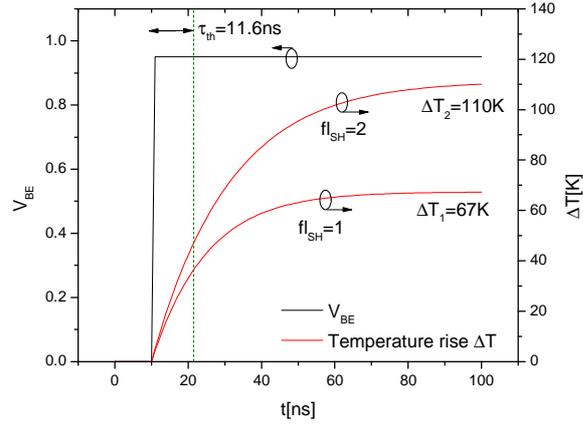


Figure 2.8: Simulated temperature rise for  $fl_{SH}=1$  and  $fl_{SH}=2$  when a voltage pulse of 0.95V (delay of 10ns,  $V_{CE}=1.5\text{V}$ ) is applied at the base of a transistor model with the emitter resistance  $r_E=5.3\Omega$  and external collector resistance  $r_{CX}=11.5\Omega$ .

The difference in the steady state junction temperatures of about  $\Delta T_j=43\text{K}$  has certainly a significant impact on the device characteristics. In this case, it leads to different steady state collector currents of  $I_C=19.0\text{mA}$  and  $I_C=23.3\text{mA}$  for  $fl_{SH}=1$  and  $fl_{SH}=2$ , respectively. In order to verify this we consider

$$\left| I_{TS} V_{B^*S} \right| \approx 0 \quad (2.12)$$

and

$$\sum \frac{|\Delta V_n|^2}{R_n} \approx I_C^2 (r_E + r_{CX}). \quad (2.13)$$

Hence, the difference in steady state temperature rise between both options  $\Delta fl_{SH}$  can be approximated as

$$\Delta fl_{sh} \approx I_C^2 (r_E + r_{CX}) R_{th} \approx 39\text{K}. \quad (2.14)$$

The made assumption is simplified since it neglects e.g. the temperature dependence of the transfer current etc. Nevertheless, the presented example demonstrates that the self-

heating flag can have a strong impact on the simulated junction temperature. In this work, the self-heating flag is set to  $fl_{SH}=2$ .

### 2.3.3 Parameter extraction

A proper parameter extraction methodology is required to derive the model parameters from measured data in order to fully exploit a compact model. The classical method of extracting model parameters is the direct extraction approach where all model parameters are directly determined with analytical expressions. A better way is a physics-based scalable extraction using I-V, C-V and S parameter measurements on transistors with several geometries, contact configurations etc. as well as special test structure (e.g. tetrode, Kelvin structures). A general overview on a standard extraction procedure together with the extracted parameters is given in Figure 2.9 [81]. A full compact model parameter extraction is quite a wide area and beyond the scope of this thesis.

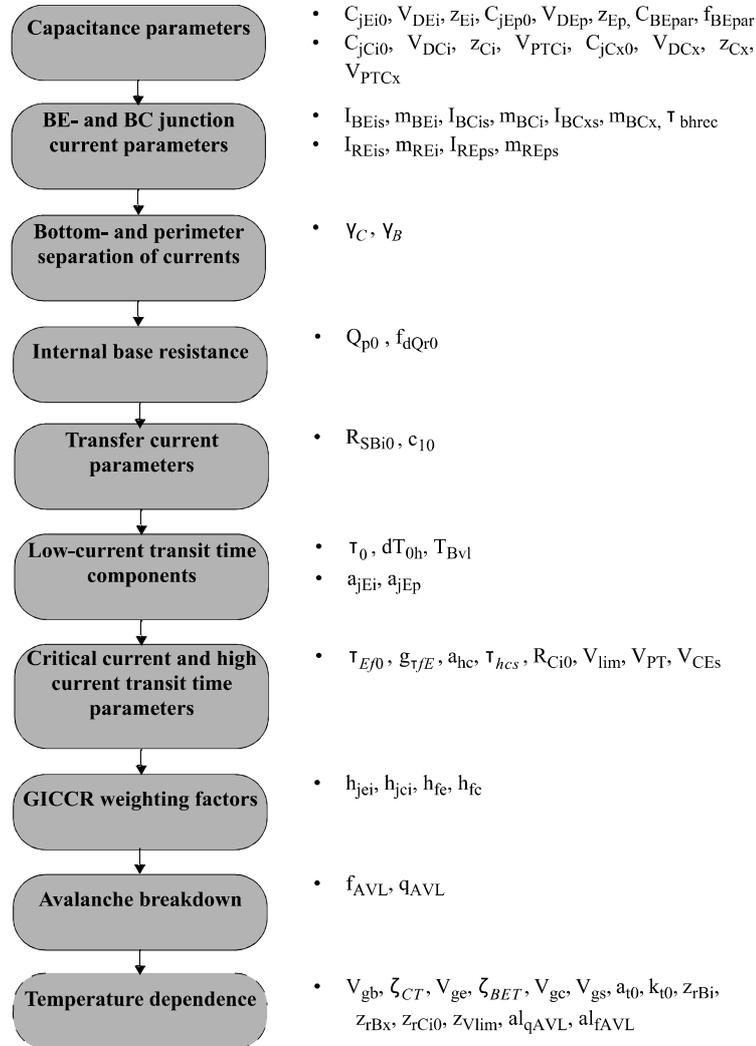


Figure 2.9: Illustration of a standard extraction procedure.

## 2.4 Model verifications

Within the DOTFIVE project, fully scalable model libraries were provided by XMOD Technologies (B3T, B4T) and STMicroelectronics (B3T, B4T and B5T). Several parameters of the B5T model cards had to be improved to achieve a better agreement with our measurements. For instance, the thermal resistance  $R_{th}$  and thermal capacitance  $C_{th}$  were extracted from measurements and numerical simulations within the work of A.K. Sahoo et al. [82]. The values for  $R_{th}$  and  $C_{th}$  are also verified in this work with pulse measurements and low frequency S parameter measurements in Chapter 3.

Transistor measurements for model parameter verification purpose and circuit measurements have been taken from the same wafer in order to avoid simulation inaccuracies due to process optimizations. In fact, a great number of process optimizations were applied in order to reach the performance goals in DOTFIVE, for example, the extreme Germanium grading in the base-emitter (BE) space-charge region. Therefore, the latest version 2.3 of HICUM/L2 including a new extended formulation [73] of the HICUM transfer current needs to be used.

In this work, the main focus lies on the extension of the state of the art compact model by applying different thermal networks. Therefore, an accurate standard model (lumped model) is crucial to ensure reliable results. The main transistor in this work is the B5T HBT with  $A_E=0.18 \times 5 \mu\text{m}^2$  and with double collector and base contacts. In the following paragraphs, a brief overview of all measurements necessary for an accurate parameter extraction and model verification is given. Measurements for DC and RF excitation at different temperatures are presented and compared with model simulations.

### 2.4.1 Measurements to characterize advanced semiconductor devices

The measurement quality and accuracy is the basis for the generation and the validation of compact models. Complex equipment in combination with elaborate calibration procedures is required. Moreover, a significant amount of time is spent on the collection of the measurement data.

Historically, advances in transistor modeling have often coincided with the development of new measurement techniques [83]: (i) The vector network analyzer (VNA) to measure small-signal scattering (S) parameters [84]; (ii) mechanical and electronic load-pull systems to map small- and large-signal performance parameters as a function of the load and source impedance [85]; (iii) pulsed DC [86] and S-parameter [87] systems used to overcome dispersive phenomena (e.g. self-heating, trapping); (iv) large-signal vector network analyzer to characterize transistors under realistic large-signal modulations [88].

In this work, measurements were performed directly on-wafer with a semi-automatic wafer prober (Süss Microtec) and coplanar probes (Süss Microtec, Cascade). Software automation (with Agilent ICCAP) over GPIB allows many measurements to be recorded quickly. On-wafer probing avoids issues related to manufacturing or packaging and is therefore adequate method to characterize active and passive devices and circuits. A temperature regulator (thermo chuck) controls the ambient device temperature. DC measurements were made with the semiconductor parameter analyzer HP4155. For RF measurements the HP4155 was combined with the VNA Rohde & Schwarz ZVA67. The system was calibrated using the short-open-load-thru (SOLT) technique on an impedance standard substrate (ISS). For the de-embedding of metal parasitics (pads, interconnections and vias) STMICROELECTRONICS has provided on-wafer Open and Short dummies.

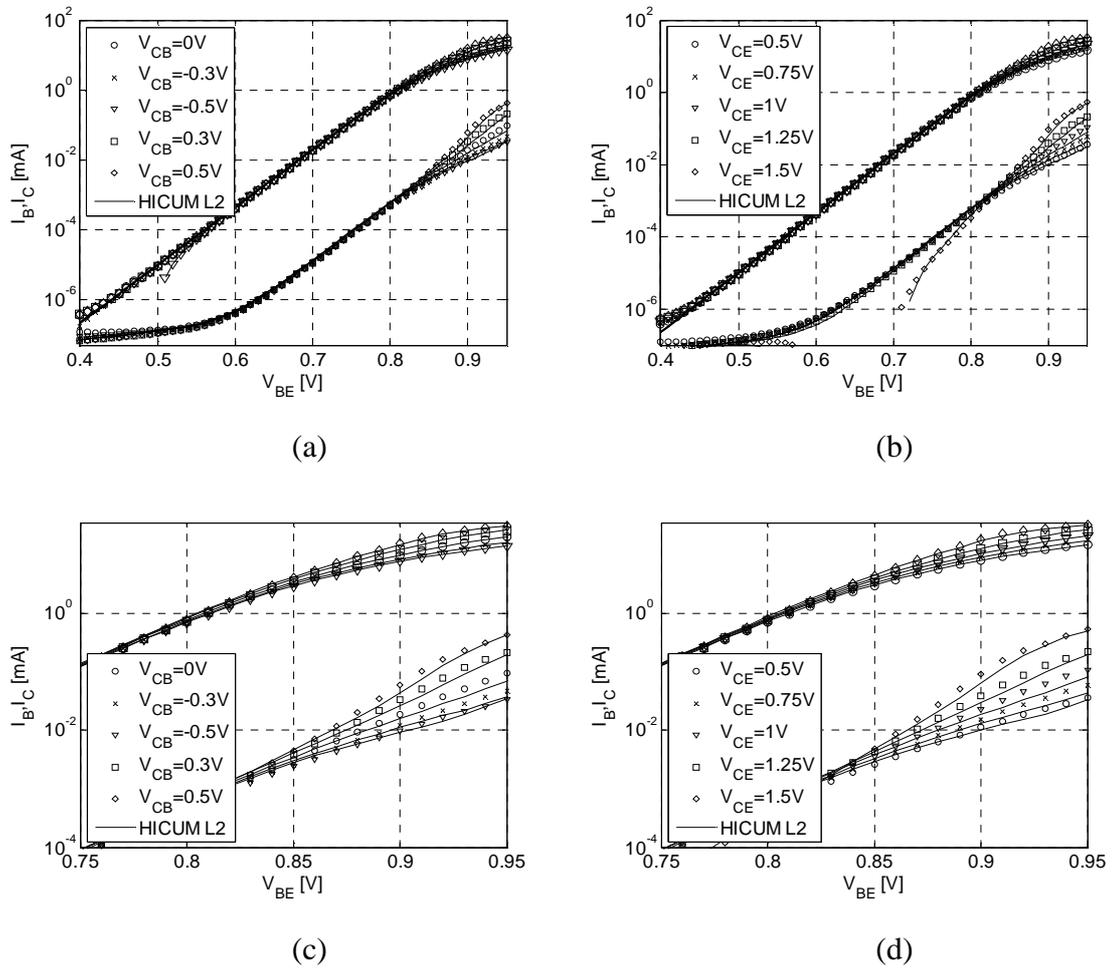


Figure 2.10: Forward Gummel plot (a) at constant  $V_{BC}$  and (b) at constant  $V_{CE}$ : Comparison between measurements (symbols) and compact model simulations (solid lines) for B5T CBEBC HBT with  $A_E=0.18 \times 5 \mu\text{m}^2$ . Enlarged section for high current injection in (c) and (d).

## 2.4.2 DC characteristics

The measurement of the current-voltage I-V relationships is the most basic form to characterize transistors. Continuous DC measurements are widely used since they require only a simple measurement setup and provide fast and accurate measurements in combination with a low noise floor.

The forward Gummel plot is shown in Figure 2.10 where the base and collector current ( $I_B$ ,  $I_C$ ) are plotted versus the base-emitter voltage  $V_{BE}$  on a semi-logarithmic scale for constant base-collector voltage  $V_{BC}$  (Figure 2.10a) or constant collector-emitter voltage  $V_{CE}$  (Figure 2.10b). At high current injection the device characteristics can be better observed in the enlarged sections displayed in Figure 2.10c and Figure 2.10d.

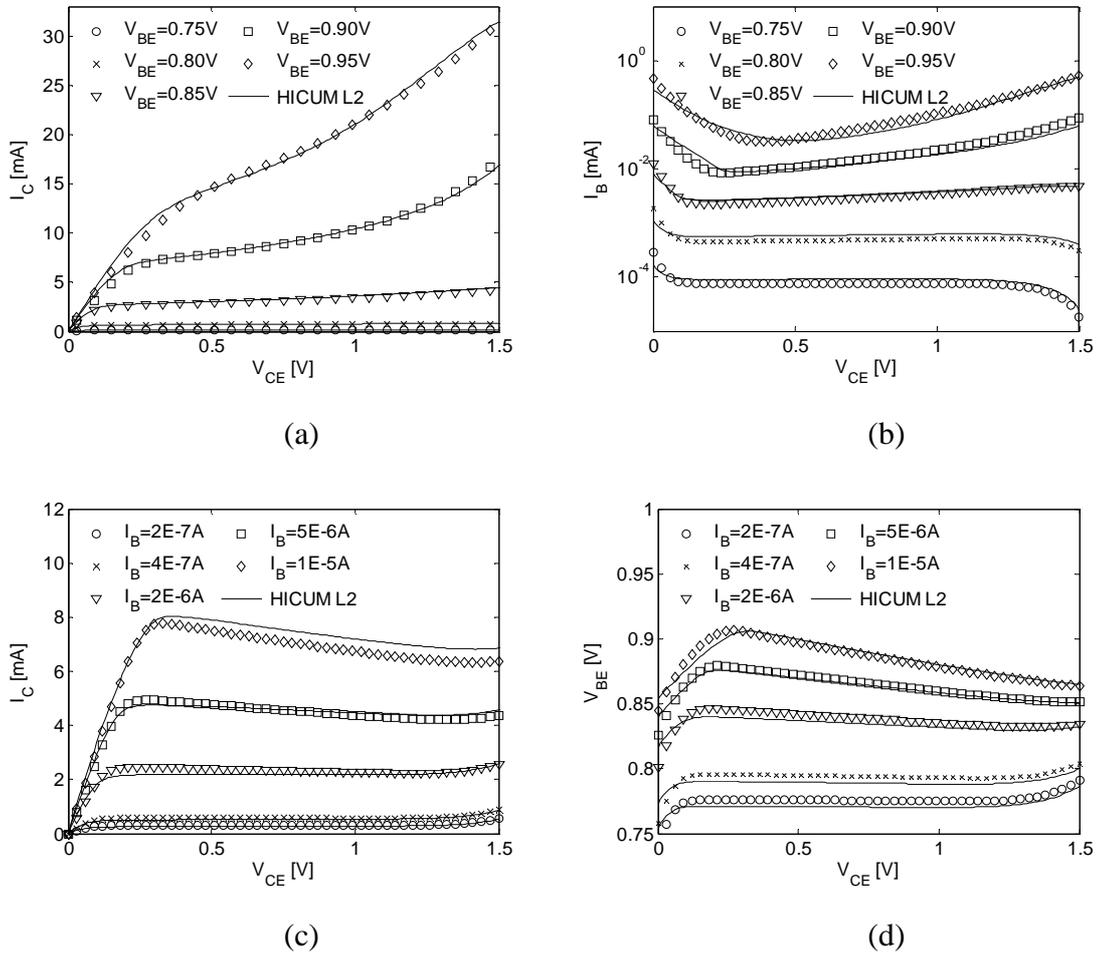


Figure 2.11: DC output characteristics of B5T CBEB C HBT with  $A_E=0.18 \times 5 \mu\text{m}^2$  where  $I_C$  (a) and  $I_B$  (b) is shown against  $V_{CE}$  for five constant values of  $V_{BE}$  and  $I_C$  (c) and  $V_{BE}$  (d) is plotted against the  $V_{CE}$  for five constant values of  $I_B$ .

The DC output characteristics for constant  $V_{BE}$  and constant  $I_B$  are illustrated in Figure 2.11a and in Figure 2.11c, respectively. The corresponding  $I_B$  and  $V_{BE}$  plotted against  $V_{CE}$  are shown Figure 2.11b and Figure 2.11d, respectively. DC measurements

are in good agreement with the compact model in almost all operating regions (hard saturation, high injection, avalanche).

### 2.4.3 Depletion capacitances

The junction capacitances can be extracted from capacitance-voltage C-V measurements or in our case from “cold” S-parameter measurements made at a frequency of 5GHz. The base-emitter  $C_{BE}$  (Figure 2.12a) and the base-collector  $C_{BC}$  (Figure 2.12b) junction capacitances are determined with (2.15) and (2.16), respectively.

$$C_{BE} = \frac{\Im(Y_{11} + Y_{12})}{\omega} \Big|_{V_{CE}=0V} \quad (2.15)$$

$$C_{BC} = -\frac{\Im(Y_{12} + Y_{21})}{2\omega} \Big|_{V_{BE}=0V} \quad (2.16)$$

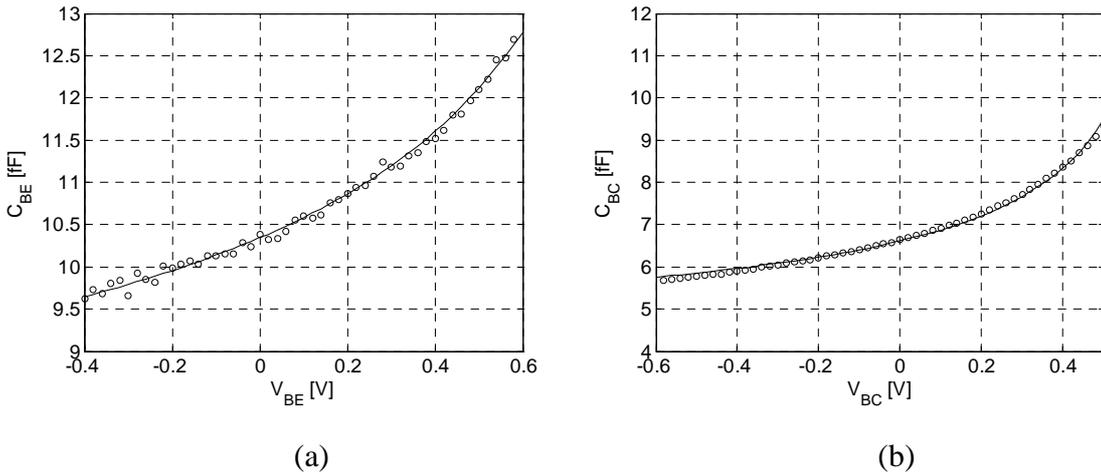


Figure 2.12: Depletion capacitances of B5T CBEB C HBT with  $A_E=0.18 \times 5 \mu\text{m}^2$ : (a) Base-emitter capacitance  $C_{BE}$  vs. base-emitter voltage  $V_{BE}$  at  $V_{CE}=0V$  and (b) base-collector capacitance  $C_{BC}$  vs. base-collector voltage  $V_{BC}$  at  $V_{BE}=0V$ .

### 2.4.4 RF characteristics

The high frequency performance of the device can be represented by  $f_T$  and  $f_{max}$  that were obtained through S-parameter measurements (see Figure 2.13) up to 45GHz.  $f_T$  (Figure 2.14a) and  $f_{max}$  (Figure 2.14b) are calculated using Equations (1.7) and (1.9), respectively. The compact model is in good agreement with the measured S parameters versus frequency as well as with the calculated  $f_T$  and  $f_{max}$  versus  $I_C$ . Peak  $f_T$  and peak  $f_{max}$  are 320GHz and 400GHz at an  $I_C$  of 10mA and 8mA, respectively. A similar device was measured in [89] up to 300GHz. Note that probably the considered transistor comes from another wafer lot fabricated with modified process parameters [45], [90] since the device has a lower peak  $f_T$ .

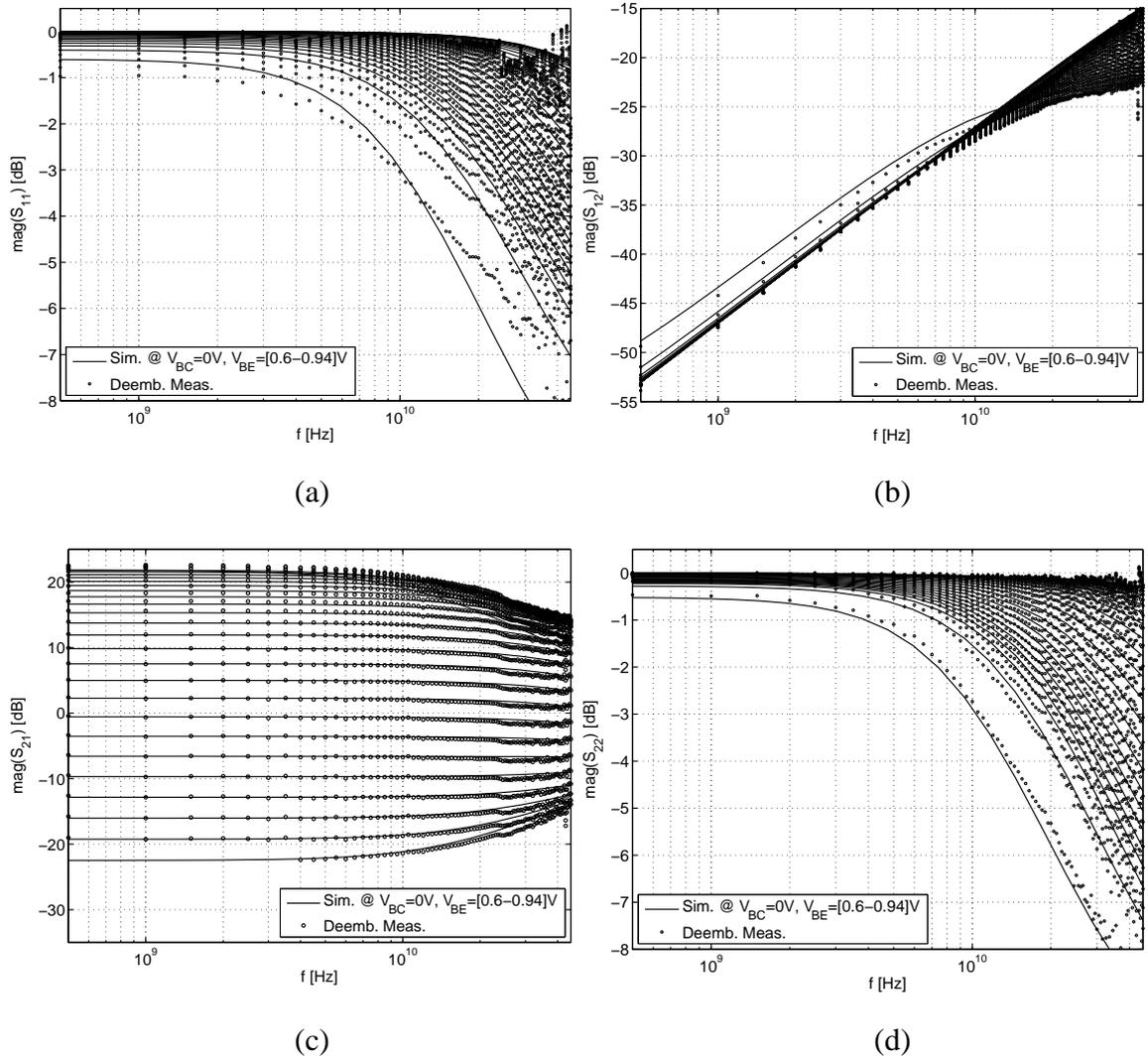


Figure 2.13: Magnitude of (a)  $S_{11}$ , (b)  $S_{12}$ , (c)  $S_{21}$ , (d)  $S_{22}$  versus frequency. Comparison between measurements (symbols) and compact model simulations (solid lines) for a B5T CBEB C HBT with  $A_E=0.18 \times 5 \mu\text{m}^2$ .

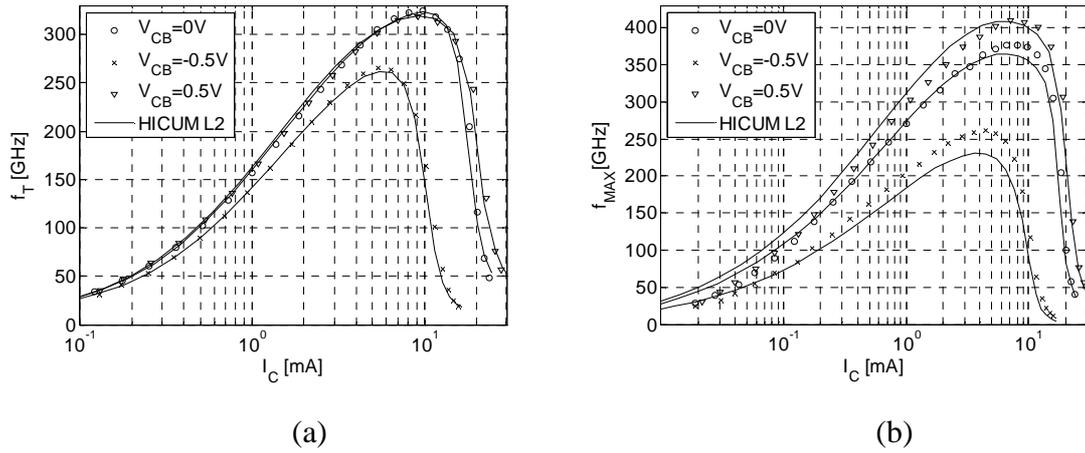


Figure 2.14: Transit frequency  $f_T$  (a) and maximum oscillation frequency  $f_{max}$  (b) vs. collector current  $I_C$  at  $V_{BC}=[0, -0.5, 0.5]V$ . Comparison of measurements (symbols) and HICUM model (solid lines) for B5T CBEBC HBT with  $A_E=0.18 \times 5 \mu m^2$ .

#### 2.4.5 Temperature dependence

DC and RF measurements were carried out at different ambient temperatures (27°C–100°C) to validate the temperature dependence of the compact model parameters.  $I_C$  and  $I_B$  versus  $V_{BE}$  and  $f_T$  versus  $I_C$  at a  $V_{BC}$  of 0V are shown in Figure 2.15a and Figure 2.15b, respectively. Good agreement between compact model and measured device in the considered temperature range can be observed. Peak  $f_T$  is reduced from 320GHz to 270GHz by increasing the temperature up to 100°C.

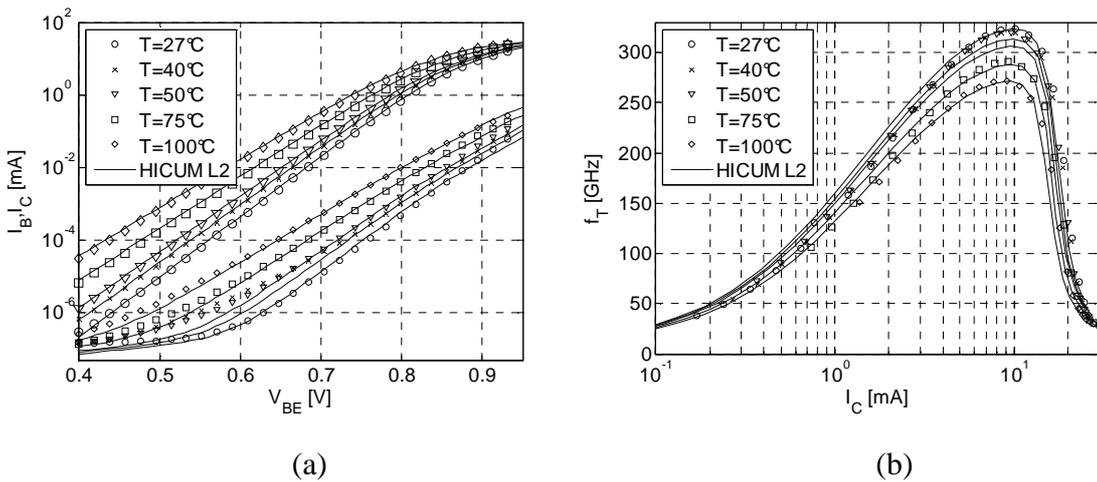


Figure 2.15: Temperature dependence validation: (a) Forward Gummel plot at constant  $V_{BC}=0V$ , (b) transit frequency  $f_T$  versus collector current  $I_C$  at  $V_{BC}=0V$  for ambient temperatures  $T=[27, 40, 50, 75, 100]^\circ C$  for B5T CBEBC HBT with  $A_E=0.18 \times 5 \mu m^2$ .

## 2.5 Conclusions

An advanced SiGe HBT technology provided by STMicroelectronics featuring  $f_T/f_{\max}$  of 320GHz/400GHz was presented. A brief overview on the basic operation principle of the physics-based compact bipolar transistor model HICUM has been given with special focus on the device self-heating. It can be stated that HICUM addresses the challenges of this advanced high frequency HBT technology. An accurate transistor model is mandatory for further investigations in Chapter 3 and 4. The compact model parameters of the main device have been extensively validated with a large number of measurements for various temperatures.



## **Chapter 3    Advanced electrothermal device characterization**

### **3.1    Introduction**

In Chapter 2, the lumped transistor model was validated. However, for advanced silicon technologies lumped models have their limitations regarding thermally distributed effects. The chapter characterizes electrothermal effects using advanced measurement and modeling techniques. Firstly, the thermal impedance of advanced SiGe:C HBTs is extracted from low-frequency S parameter measurements. Secondly, a combined pulsed DC - pulsed RF state of the art measurement system is presented. Isothermal DC and AC measurement data can be achieved allowing a complete characterization and exploration of the safe operating area (SOA). Thirdly, distributed thermal networks are applied at the temperature node of the transistor compact model. (i) A recursive network that permits a better description of the dynamic self-heating effect inside one device in comparison to the standard single pole network. (ii) A thermal coupling network that characterizes the thermal coupling between neighboring devices.

## 3.2 Characterization of self-heating

### 3.2.1 Thermal impedance extraction from low frequency S parameters

The characterization of electro-thermal self-heating inside devices remains an essential task for model developers in order to determine the device operating temperature. In the literature, several DC measurement techniques for the extraction of the thermal resistance  $R_{th}$  are proposed [91]–[93]. In steady-state thermal models, the device temperature instantaneously follows the power that is dissipated and the dynamic thermal behavior is disregarded. The dynamic behavior can be described by the thermal impedance  $Z_{th}$  which can be expressed as in Equation (3.1) [70]. In general, the thermal impedance  $Z_{th}$  can be determined from transient [94]–[98] and AC measurement techniques [99]–[101]. The device thermal response ranges from about few kilohertz to about 200MHz in SiGe HBTs [99]. Hence,  $Z_{th}$  is limited to low frequencies where it can be extracted. Low frequency S-parameter measurements are suitable since it is a relatively simple and precise measurement procedure.

$$Z_{th}(j\omega) = \sum_{n=1}^{n=\infty} \frac{R_{thn}}{1 + j\omega R_{thn} C_{thn}} \quad (3.1)$$

#### 3.2.1.1 Theoretical background

Collector current  $I_C$  and base current  $I_B$  are functions of the three independent variables: (i) the base-emitter voltage  $V_{BE}$  (ii) the collector-emitter voltage  $V_{CE}$  and (iii) the junction temperature  $T$ . To generalize the following equations  $V_{BE}$ ,  $V_{CE}$ ,  $I_B$  and  $I_C$  are replaced by  $V_1$ ,  $V_2$ ,  $I_1$  and  $I_2$ , respectively.

$$\begin{aligned} I_1 &= f_1(V_1, V_2, T) \\ I_2 &= f_2(V_1, V_2, T) \end{aligned} \quad (3.2)$$

A linearization valid for small signal excitations at a constant bias condition leads to

$$\begin{aligned} i_1 &= y_{11}v_1 + y_{12}v_2 \\ i_2 &= y_{21}v_1 + y_{22}v_2 \end{aligned} \quad (3.3)$$

where each y-parameter is defined as

$$y_{mn} = \frac{\partial f_m}{\partial V_n} \quad m = 1; 2 \quad n = 1; 2. \quad (3.4)$$

Here, index 1 and 2 indicate the base and collector ports, respectively.

From Equation (1.12) one obtains the following expression [70] for the  $\bar{Y}$  parameters (the bar indicates that the parameter is temperature dependent)

$$\bar{y}_{mn} = \left. \frac{dI_m}{dV_n} \right|_{V_m=const.} = \left. \frac{\partial f_m}{\partial V_n} \right|_{V_m, T=const.} + \left. \frac{\partial f_m}{\partial T} \cdot \frac{dT}{dV_n} \right|_{V_m=const.} = y_{mn\_iso} + \left. \frac{\partial f_m}{\partial T} \cdot \frac{dT}{dV_n} \right|_{V_m=const.} \quad (3.5)$$

where  $y_{mn\_iso}$  is temperature independent. The temperature dependence is approximated for small signal excitations with

$$\alpha_m = \left. \frac{\partial f_m}{\partial T} \right|_{V_m=const.} \quad (3.6)$$

where  $\alpha_m$  is the relative change of  $I_m$  per degree temperature change at a constant voltage  $V_m$  ( $\partial f_2/\partial T = \partial I_C/\partial T$  is defined in Equation (1.16)). The junction temperature  $T$  is defined as

$$T = T_{amb} + Z_{th} \cdot P_{diss} \quad (3.7)$$

where  $T_{amb}$  is the ambient temperature (chuck temperature) and  $P_{diss}$  is the dissipated power in the device that results from

$$P_{diss} = V_1 I_1 + V_2 I_2 \quad (3.8)$$

The change in dissipated power  $dP_{diss}$  with small signal excitation can be written as

$$dP_{diss} = dV_1 I_1 + V_1 dI_1 + dV_2 I_2 + V_2 dI_2. \quad (3.9)$$

From the Equations (3.7) and (3.8) it follows that

$$\left. \frac{dT}{dV_n} \right|_{V_m=const.} = Z_{th} \left( I_n + V_n \left. \frac{\partial I_n}{\partial V_n} \right|_{V_m=const.} + V_k \left. \frac{\partial I_k}{\partial V_n} \right|_{V_m=const.} \right) \quad k = 3 - n \quad (3.10)$$

which can be transformed to

$$\left. \frac{dT}{dV_n} \right|_{\Delta V_m} = Z_{th} (I_n + V_n \bar{y}_{mn} + V_k \bar{y}_{kn}). \quad (3.11)$$

Using the Equations (3.5) and (3.11), the following expression for  $Z_{th}$  is obtained.

$$Z_{th} = \frac{\bar{y}_{mn} - y_{mn\_iso}}{\left( \partial f_m / \partial T_j \right) \left[ I_n + V_n \bar{y}_{mn} + V_k \bar{y}_{kn} \right]} \quad (3.12)$$

Since in Equation (3.5) the term  $dT/dV_n$  is greater for  $V_2$  ( $V_{CE}$ ) than for  $V_1$  ( $V_{BE}$ ),  $y_{12}$  and  $y_{22}$  are the most affected, and therefore, should be the most suitable for extraction of  $Z_{th}$ .

In case of  $y_{22}$ ,  $Z_{th}$  would be

$$Z_{th} = \frac{\bar{y}_{22} - y_{22\_iso}}{\alpha_2 [I_2 + V_2 \bar{y}_{22} + V_1 \bar{y}_{12}]} = \frac{\bar{y}_{22} - y_{22\_iso}}{\alpha_{IC} [I_C + V_{CE} \bar{y}_{22} + V_{BE} \bar{y}_{12}]} \quad (3.13)$$

Since  $V_{BE} \bar{y}_{12}$  is very small compared to  $V_{CE} \bar{y}_{22}$ , Equation (3.13) can be simplified to

$$Z_{th} = \frac{\bar{y}_{22} - y_{22\_iso}}{\alpha_{IC} [I_C + V_{CE} \bar{y}_{22}]} \quad (3.14)$$

Measurements at different ambient temperatures are required to extract the temperature dependence of the collector current  $\alpha_{IC}$ . However, if the thermal resistance

$$R_{th} = Z_{th}(\omega \rightarrow 0) = Z_{th\_0} = \frac{\bar{y}_{mn\_0} - y_{mn\_iso\_0}}{(\partial f_m / \partial T_j) [I_n + V_n \bar{y}_{mn\_0} + V_k \bar{y}_{kn\_0}]} \quad (3.15)$$

is already known, Equation (3.12) can be normalized to

$$\frac{Z_{th}}{R_{th}} = Z_{th\_norm} = \frac{(\bar{y}_{mn} - y_{mn\_iso})}{(\bar{y}_{mn\_0} - y_{mn\_iso\_0})} \cdot \frac{(I_n + V_n \bar{y}_{mn\_0} + V_k \bar{y}_{kn\_0})}{(I_n + V_n \bar{y}_{mn} + V_k \bar{y}_{kn})} \quad (3.16)$$

In this case, low frequency S parameter measurements at room temperature are sufficient to extract  $Z_{th}$ . In the case of  $y_{22}$ ,  $Z_{th\_norm}$  would be

$$Z_{th\_norm} = \frac{(\bar{y}_{22} - y_{22\_iso})}{(\bar{y}_{22\_0} - y_{22\_iso\_0})} \cdot \frac{(I_2 + V_2 \bar{y}_{22\_0})}{(I_2 + V_2 \bar{y}_{22})} \quad (3.17)$$

However, if  $R_{th}$  is unknown,  $\alpha_{IC}$  has to be extracted due to Equation (3.14) which appears not trivial especially when  $V_{BE}$  is constant as it can be seen in Equation (1.16).

Another approach presented in [99] uses H parameters to calculate the thermal impedance. The measured S parameters are transformed into H parameters [102].

$$\begin{aligned} v_1 &= h_{11} i_1 + h_{12} v_2 \\ i_2 &= h_{21} i_1 + h_{22} v_2 \end{aligned} \quad (3.18)$$

Repeating the steps (3.5)-(3.11) for  $\bar{h}_{12}$  leads to [99]

$$\bar{h}_{12} = \frac{h_{12\_iso} + Z_{th} (\alpha_{VBE} V_{BE} I_C - V_{CE} (\alpha_{IC} I_C h_{12\_iso} - \alpha_{VBE} V_{BE} h_{22\_iso}))}{1 - \alpha_{VBE} V_{BE} Z_{th} I_B - \alpha_{IC} I_C Z_{th} V_{CE}} \quad (3.19)$$

where the arising  $\bar{h}_{22}$  is also separated into isothermal and temperature dependent part.

Using Equation (3.7),  $\alpha_{VBE}$  can be described as [99]

$$\alpha_{VBE} = \frac{\partial V_{BE}}{\partial T_{amb}} \cdot \left( 1 - \frac{\partial R_{th}}{\partial T} P_{diss} - R_{th} \frac{\partial P_{diss}}{\partial T} \right) \cong \frac{\partial V_{BE}}{\partial T_{amb}} \quad (3.20)$$

Since  $\partial R_{th}(T)/\partial T \cdot P_{diss}$  and  $\partial P_{diss}/\partial T \cdot R_{th}$  are small in respect to 1, the first order approximation can be used. Note that,  $\alpha_{IC}$  is now defined as in Equation (1.17) due to constant  $I_B$ . Solving for  $Z_{th}$  yields

$$Z_{th} = \frac{\bar{h}_{12} - h_{12\_iso}}{\alpha_{VBE}(I_C + \bar{h}_{12}I_B + h_{22\_iso}V_{CE}) + \alpha_{IC}V_{CE}(\bar{h}_{12} - h_{12\_iso})}. \quad (3.21)$$

The temperature dependence of  $V_{BE}$  ( $\alpha_{VBE}$ ) and  $I_C$  ( $\alpha_{IC}$ ), used in Equation (3.19) and (3.21), is extracted from the output characteristics with constant  $I_B$  at different chuck temperatures  $T_{amb}$  (27°C-100°C). The measurements (symbols) of  $V_{BE}$  and  $I_C$  versus the  $T_{amb}$  at a  $V_{CE}$  of 1.5V for a B5T HBT (with drawn  $A_E=0.18 \times 5 \mu m^2$ ) compared with a first order mathematical fit (lines) is shown in Figure 3.1a and Figure 3.1b, respectively. In this case, the use of a constant  $\alpha_{VBE}$  of 1.1mV/K and a constant  $\alpha_{IC}$  of 0.062mA/K is valid since the H parameters were measured at the same DC bias.

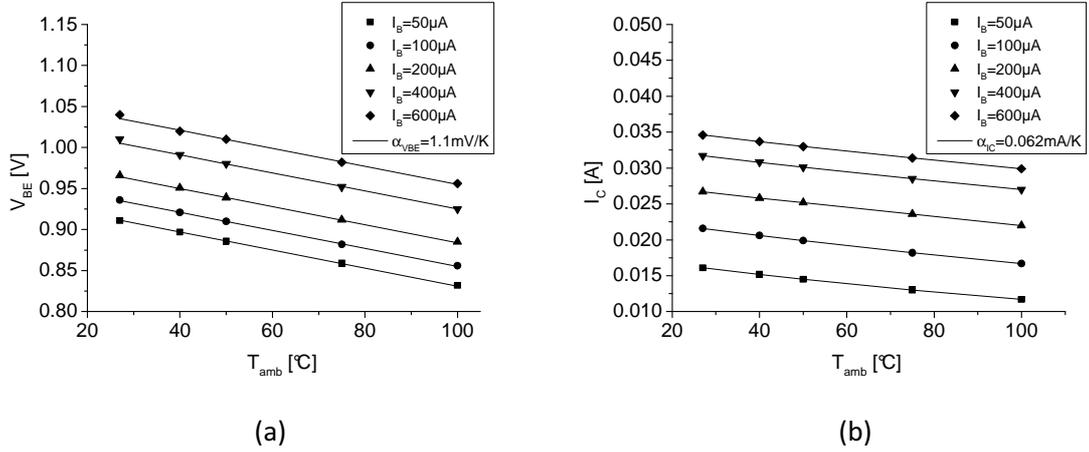


Figure 3.1: Measured values of  $V_{BE}$  (a) and  $I_C$  (b) for constant values of  $I_B$  are shown versus different chuck temperatures  $T_{amb}$  (27°C-100°C) for a B5T HBT with drawn  $A_E=0.18 \times 5 \mu m^2$ . The measurements (symbols) are approximated with a first order mathematical fit (lines) using constant temperature dependencies  $\alpha_{VBE}$  of 1.1mV/K and  $\alpha_{IC}$  of 0.062mA/K.

The terms  $\bar{h}_{12}I_B$  and  $h_{22\_iso}V_{CE}$  ( $h_{22\_iso}$  calculated from isothermal model simulations) are negligible against  $I_C$ . Moreover, due to the very small value of  $\alpha_{IC}$ , the term  $\alpha_{IC}V_{CE}(\bar{h}_{12} - h_{12\_iso})$  can be neglected compared to  $\alpha_{VBE}I_C$  (simplifications also validated in [99]). Hence,  $Z_{th}$  can be approximated as

$$Z_{th} \cong \frac{\bar{h}_{12}}{\alpha_{VBE}V_{BE}I_C}. \quad (3.22)$$

### 3.2.1.2 Low frequency S parameter measurements

Low frequency S parameters were obtained in the frequency range from 30kHz to 3GHz (corresponding to the thermal time constant) where dynamic self-heating is visible. A commercial low-frequency (LF) vector network analyzer (VNA) Agilent E5061B (5Hz-3GHz) is used with noncommercial bias tees specially developed to cover the frequency range of interest. The VNA was calibrated on-wafer using SOLT method and the data was de-embedded using Open and Short test structures.

In order to extract the isothermal small signal parameters it is necessary to define the high frequency edge  $f_{th\_max}$

$$\tau_{th} = R_{th}C_{th} > \frac{1}{2\pi f_{th\_max}}. \quad (3.23)$$

of the frequency range where thermal feedback influences the electrical comportment of the measurements. There are various studies in literature to identify thermal feedback in electrical characteristics, for example, in [103]  $z_{22}$  is used which is defined as follows.

$$z_{22}(\omega) = \left. \frac{v_{CE}(\omega)}{i_C(\omega)} \right|_{i_B=0} \quad (3.24)$$

For frequencies much lower than the thermal time constant  $\tau_{th}$ ,  $z_{22}$  approaches negative values (negative differential resistance) which is caused due to self-heating. The negative slope

$$z_{22}(\omega \rightarrow 0) \cong \left. \frac{\Delta V_{CE}}{\Delta I_C} \right|_{I_B=const.} \quad (3.25)$$

can be observed in the output characteristics for constant  $I_B$  (Figure 1.11b). In Figure 3.2a, the real part of  $z_{22}$  versus frequency is simulated with the validated compact model (measurements vs. simulation in Paragraph 2.4).  $I_B$  is constant ( $I_B=350\mu A$ ) and  $V_{CE}$  is varied between 1.49V and 1.51V. The real part of  $z_{22}$  for  $\omega \rightarrow 0$  corresponds to the negative slope of the output characteristic at same bias conditions as shown in Figure 3.2b.

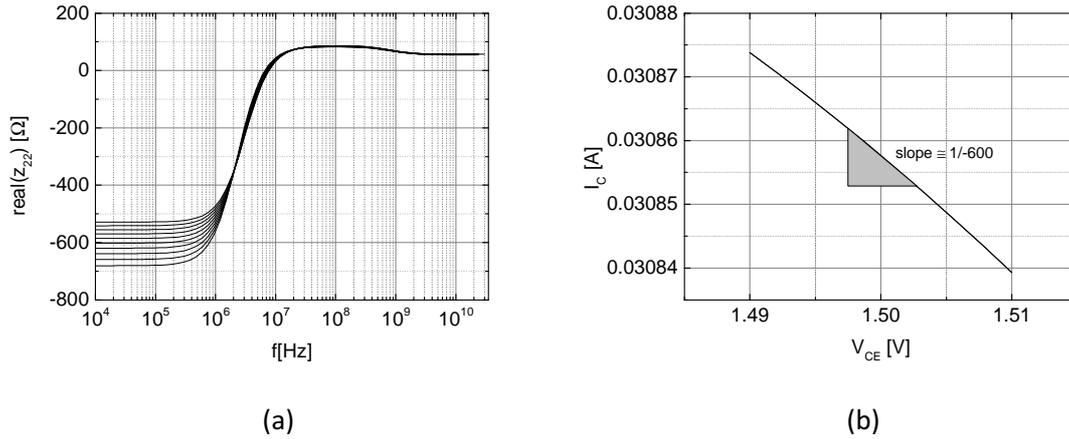


Figure 3.2: Simulation: (a) Real part of  $z_{22}$  versus frequency of B5T HBT model ( $A_E=0.18 \times 5 \mu\text{m}^2$ ) for  $I_B=350 \mu\text{A}$  and  $V_{CE}=1.49\text{V}-1.51\text{V}$  and (b) corresponding slope on the output characteristics of the device.

At higher operating frequencies where signal changes over time are much shorter than  $\tau_{th}$  the device temperature stays essentially constant and there is no longer a thermally induced negative differential resistance [103]. Therefore, the real part of  $z_{22}$  gets positive due to Early and Kirk effect. However, it is difficult to define a distinct value of  $f_{th\_max}$ .

A more precise localization is achieved with the phase of  $y_{22}$  (see Figure 3.3a). Isothermal compact model simulation does not lead to negative values of the phase. Therefore, the zero crossing can be used to define  $f_{th\_max}$ . In this work,  $f_{th\_max}$  lies in the range of 300-500MHz. Measurements (solid black) and isothermal simulations (dashed red) of the magnitude of  $y_{22}$  at  $V_{BE}=[0.95, 0.96, 0.97, 0.98, 0.99, 1]\text{V}$  and  $V_{CE}=1.5\text{V}$  are displayed in Figure 3.3b. At frequencies lower than  $f_{th\_max}$ , the isothermal magnitude of  $y_{22}$  is constant.

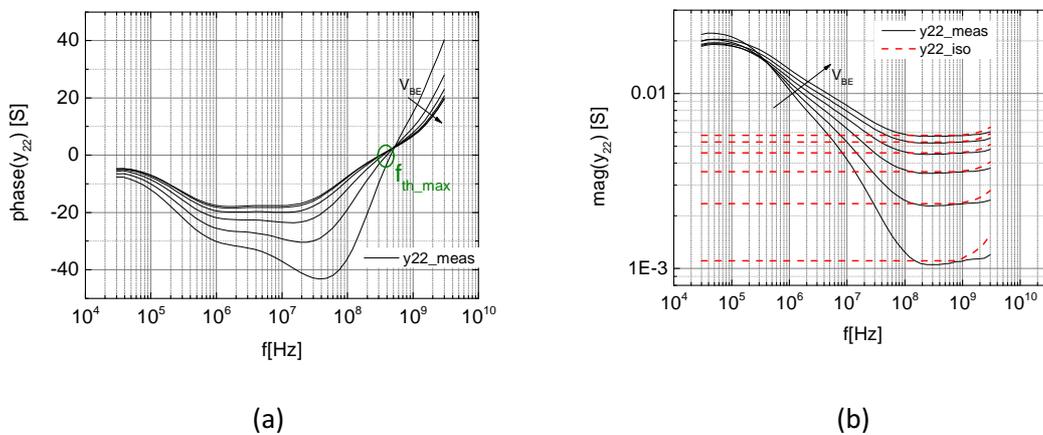


Figure 3.3: Phase (a) and magnitude (b) of measured  $y_{22\_meas}$  (solid line) and simulated  $y_{22\_iso}$  (dashed line) versus frequency for B5T HBT ( $A_E=0.18 \times 5 \mu\text{m}^2$ ) at  $V_{BE}=[0.95, 0.96, 0.97, 0.98, 0.99, 1]\text{V}$  and  $V_{CE}=1.5\text{V}$ .

Having determined  $y_{22\_iso}$ , one can calculate the normalized thermal impedance  $Z_{th\_norm}$  with (3.17). Magnitude and phase of  $Z_{th\_norm}$  for a  $0.18 \times 5 \mu\text{m}^2$  SiGe HBT is shown in Figure 3.4a and Figure 3.4b, respectively. In Figure 3.4c and Figure 3.4d, the magnitude and phase of  $Z_{th}$  is calculated using the second proposed method (3.22) which requires the measured  $h_{12}(\omega)$  and  $\alpha_{V_{BE}}$ . The result is compared with magnitude and phase of  $R_{th}Z_{th\_norm}$  ( $R_{th} \approx 4000\text{K/W}$ , see in [82]). Good agreement can be observed comparing the results of the two methods.

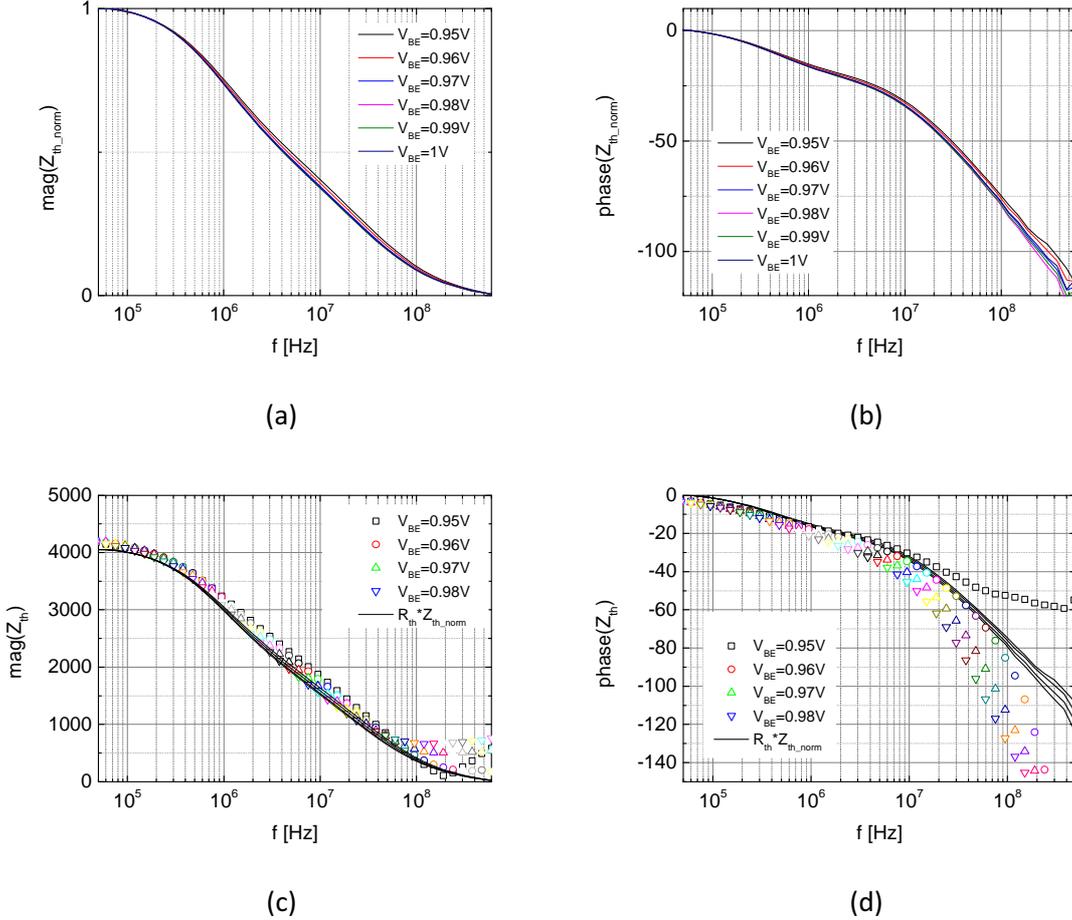


Figure 3.4: Magnitude (a) and phase (b) of the normalized thermal impedance  $Z_{th\_norm}$  calculated with (3.17) from low frequency  $y_{22}$  measurements for B5T HBT ( $A_E = 0.18 \times 5 \mu\text{m}^2$ ). Magnitude (c) and phase (d) of  $Z_{th}$  calculated with (3.22) from low frequency  $h_{12}$  measurements compared with  $R_{th}Z_{th\_norm}$  using  $R_{th} \approx 4000\text{K/W}$ .

### 3.2.1.3 Discussion

The thermal effect is very pronounced for the considered device. Thermal feedback disappears at frequencies above  $f_{th}$  ( $\approx 500\text{MHz}$ ) when the magnitude of  $Z_{th}$  becomes almost zero. The four-pole parameters, especially the short circuit output admittance ( $y_{22}$ ) and the reverse voltage gain ( $h_{12}$ ), can be strongly temperature dependent at low frequencies. The presented approach allows the extraction of  $R_{th}$  and  $C_{th}$  in dependence of power and temperature. In our case, the calculation of  $R_{th}$  appears very sensitive to the

term  $\partial f_m / \partial T_j$ . Thus, small inaccuracies in  $\alpha_{VBE}$  can lead to large errors in the calculated  $R_{th} = Z_{th}(\omega=0)$ . Therefore, an  $R_{th}$  extraction using DC measurements at different temperatures as presented, for example, in [93] is preferred. However, robust results have been achieved for  $C_{th}$  extraction using the normalized  $Z_{th\_norm}$  with Equation (3.16) using  $y_{22}$ . Note that the proposed approach supposes a unique average temperature and has to be used with care for multi-finger devices.

### 3.2.2 Pulse measurements for microwave device characterization

Due to increased self-heating, measured DC and AC characteristics become intrinsically temperature dependent, e.g. for two different bias points the internal device temperature is different. This makes compact model parameter extraction very cumbersome because these parameters are very often temperature dependant e.g. access (base, emitter, collector) resistances, transit times and saturation currents. In order to characterize the temperature dependence of model parameters, isothermal data is in principle necessary. This can be achieved by performing DC and S parameter measurements under pulsed condition. Even if pulsed measurements may not completely eliminate self-heating, they do reduce the device temperature significantly and thus allow (i) achieving quasi-isothermal measurement data, (ii) extracting thermal resistance  $R_{th}$  and capacitance  $C_{th}$  [104], (iii) extending the measured bias range towards higher voltages and current densities. The latter is necessary in order to verify the compact model and its extracted parameters under realistic conditions: the device characterization needs to go beyond the standard measurements since most high frequency applications require large-signal operation, in which currents and charges have to be modeled accurately over a sufficiently wide bias range.

An automatic measurement setup is presented that can be applied to high speed microwave devices. The system enables simultaneous measurements of pulsed DC and pulsed S-parameter characteristics. Measurements with pulse widths down to 80 ns are shown for DC and 150 ns for RF in a broad frequency range (500 MHz–45 GHz) with current resolution in the  $\mu A$  range. These performances are beyond those of the pulsed measurement systems (PMSs) in [105]–[107]. A detailed description of the PMS is given including the general principle, the experimental setup and the related measurement procedure. Moreover, system optimization and verification using a homemade pulsed simulation environment is presented.

#### 3.2.2.1 Principle

Pulse measurements are based on recording the transistor response to short pulsed stimuli applied at its terminals. The main idea is that if the pulse width is sufficiently

short, there is not enough time for the internal temperature of the device to change significantly.

A pulse generator produces short pulses starting from a defined DC quiescent condition at low power dissipation. The applicability for different device technologies and geometries is limited by the internal resistance and the I-V compliance values of the generator. In order to avoid high-frequency oscillations, the pulses pass through a bias tee (diplexer) with a  $50\ \Omega$  RF load on its RF port. A calibration that takes into account the resistance of bias tees and cables is required.

The pulse width  $T_w$  and the pulse period  $T_p$  must be adapted to define the duty cycle  $D$  for the device under test (DUT), as  $D = T_w/T_p \cdot 100\%$ . The pulse duration must be large enough to achieve sufficient measurement precision, but much smaller than the thermal time constant to ensure isothermal behavior of the device. Besides, the duty cycle has to be sufficiently small to allow that the device can cool down within one period. According to the DUT a duty cycle lower than 10% is generally adequate.

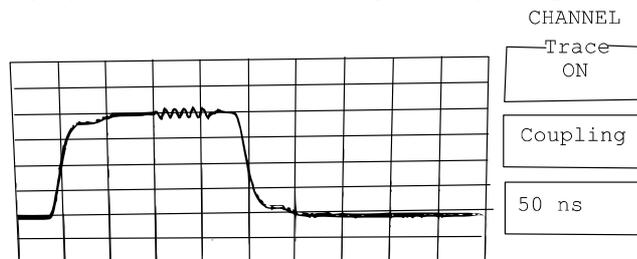


Figure 3.5: (a) Oscilloscope measurement of synchronized DC and RF pulse.

Since the pulses are applied for a small time compared to the total period, pulsed measurements cause little stress to the DUTs, so they allow measurements outside the SOA without damaging the transistors and study phenomena such as the pinch-in effect of the emitter current [108]. Moreover, it is possible to perform pulsed RF measurements, where an RF and a DC pulse can be superimposed using DC and RF port of a bias tee (see Figure 3.5). The DC pulse form strongly depends on the input resistance of the pulse generator and of the DUT as well as lumped parasitics of cables and bias tees. Therefore, the pulse form should be verified with an oscilloscope in order to define the measurement window to be in a steady region of the pulse.

### 3.2.2.2 Experimental setup

On-wafer measurements were made on B3T and B5T SiGe HBTs (see Paragraph 2.2) in GSG configuration at controlled room temperature. Pulse measurements were carried out with the pulsed DC analyzer Keithley 4200-SCS in combination with the VNA Rohde & Schwarz ZVA67 (with ZVAX extension unit) as shown in Figure 3.6. The 4200-SCS consists of two pulse measurement units (4225 PMUs) that generate the pulse and measure the pulse response. The pulses are applied directly to the base of the

DUT, while the collector voltage is held constant and the emitter is connected to the ground. The PMU allows to create pulses larger than 80ns with minimum rise and fall times of 20ns. Measurements with sufficient accuracy were obtained using a time window between 60% and 90% of the DC pulse duration.

In order to synchronize the DC and RF pulses, the 4200-SCS sends a trigger signal generated with the pulse generator unit (4220 PGU) to the ZVA67. The synchronization has been adapted with delay parameters and verified with the oscilloscope LeCroy Wavepro960. The input resistance of channel 1 (base monitor) and channel 2 (collector monitor) of the oscilloscope are set to  $50\Omega$  and  $1M\Omega$ , respectively, to prevent the system from oscillations. A reasonable trade-off between accuracy and measurement time has been reached using an averaging factor between 5 and 10.

In this configuration, a duty-cycle of up to 50% is possible, however accurate results were achieved using values between 1% and 10%. Below 1%, the RF pulsed measurements exhibit insufficient accuracy, while above 10%, thermal dispersion can occur in the DUT. RF pulsed measurements could be performed up to 67GHz, but cables and connectors set the limit to 45GHz. The maximum measurable current is 200mA, while the maximum admissible voltage is 10V. The measured RF data is transferred from the ZVA67 to the 4200-SCS over a GPIB interface.

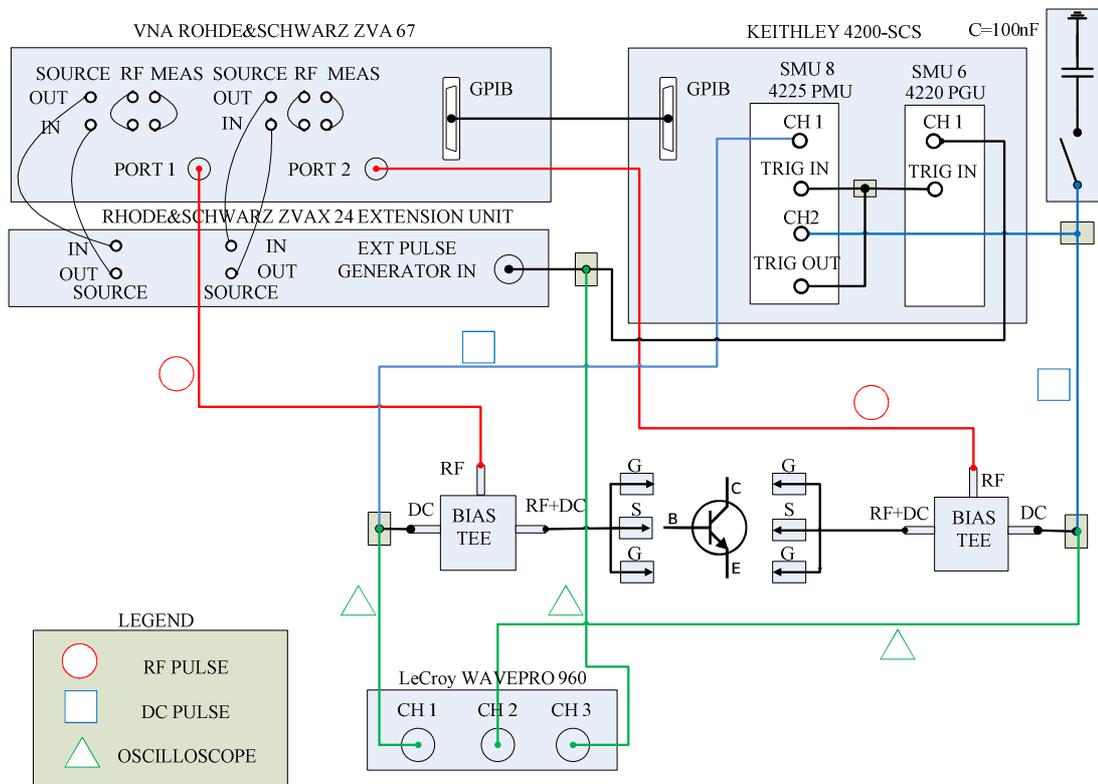


Figure 3.6: Experimental set-up of the PMS, where DC and RF pulses are applied through the DC and RF ports of the bias tees at the base and the collector of the DUT.

### 3.2.2.3 Software

Accurate device characterization with pulse measurements requires accurate data acquisition. The company NMDG was instructed to implement a special library in the 4200-SCS allowing automatic pulsed DC and pulsed DC/RF measurements with focus on SiGe HBT characterization. DC bias conditions are reached with a corrective algorithm. For example, due to the load impedance at the collector, the  $I_C$  response produces a negative  $V_{CE}$  pulse that has to be compensated. Therefore, an iterative algorithm determines a corrected  $V_{CE}$  pulse using the setpoint value, the load impedance and the measured current response in order to keep the collector voltage constant during the measurement.

### 3.2.2.4 Pulsed S parameter

To characterize the small-signal behavior of active devices, low RF power has to be used (especially for bipolar transistors). The source level was chosen to be -28dBm (at the RF port of the bias network) in order to ensure the linear condition and at the same time to have a sufficient accuracy level. First of all, a power calibration with an RF power of -20dBm is performed that adapts the source level for each frequency to achieve a constant RF power level. After that, a standard SOLT calibration (-28dBm) is carried out. During measurement, biasing level and pulse synchronization is verified by monitoring port 1, port 2 and the trigger trace on the oscilloscope LeCroy WAVEPRO 960 (see Figure 3.6).

### 3.2.2.5 System optimization

In this section, the operation principle of the PMS is reproduced using pulsed simulations. The simulation environment helps to better understand the operating principle of the PMS and is an effective tool to optimize the pulse stability and system parameters as duty cycle, measurement window, etc. Moreover, pulsed and non-pulsed DC and S parameter characteristics are compared in order to verify the consistency of the PMS with conventional measurements.

#### 3.2.2.5.1 Pulse simulations

Since the PMS is rather complex for theoretical treatment, pulsed simulations were carried out imitating the behavior of the system. The pulse shape strongly depends on the input resistance of the pulse generator and the DUT as well as lumped parasitics like cables and bias tees. Therefore, a circuit model of the PMS was implemented in ICCAP (Figure 3.7) including all passive and active components as for example the bias network (Figure 3.8).

The impedance of the coaxial cables delays the pulse signal by about 20ns and is characterized with a distributed coaxial cable model. Simulating the measurement bench requires not only the consideration of all passive components but also the same data acquisition procedure. For instance, in simulation and measurement, the transient base and collector currents are calculated using the voltage drop across a  $50\Omega$  resistor. Besides, it is possible to select the same input parameters like amplitude and width of the DC pulse, as well as the position of the measurement window. This enables the optimization of these parameters, e.g. data sampling in the stable region of the pulse or optimization of the duty cycle.

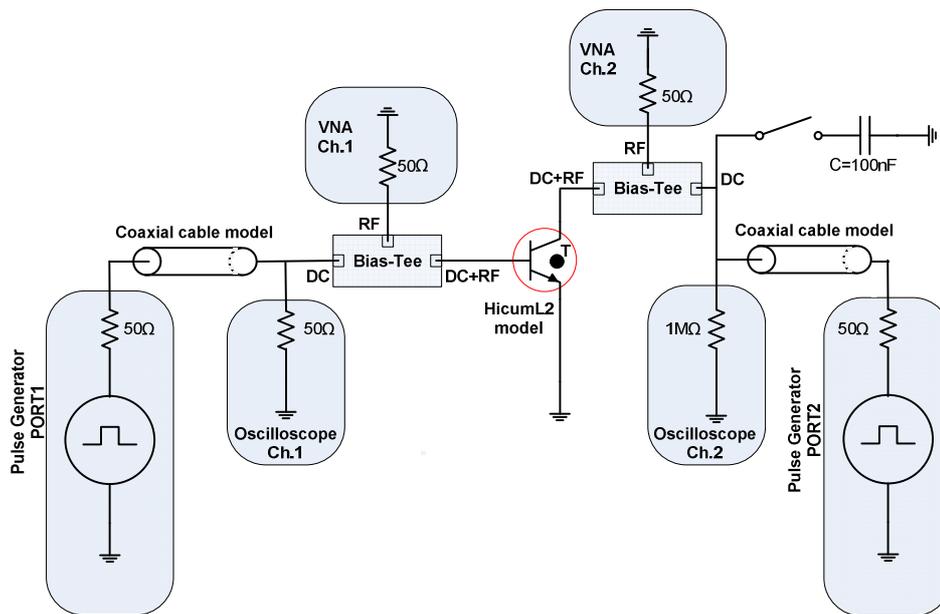


Figure 3.7: Schematic circuit diagram of the pulse measurement simulation environment, where DC pulses are applied through the DC and RF ports of the bias tees at the base and the collector node of the transistor compact model.

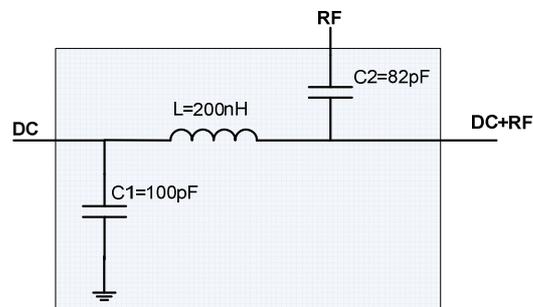


Figure 3.8: Schematic circuit diagram of the bias tee network.

During simulation it is possible to monitor all parasitic currents as well as the temperature of the transistor. The latter requires an accurate compact model of the DUT. The temperature node of the transistor model is connected to a thermal network in order

to precisely determine the transient thermal heating inside the device when a short pulse is applied. Simulation results are presented in Paragraph 3.3.1.2.

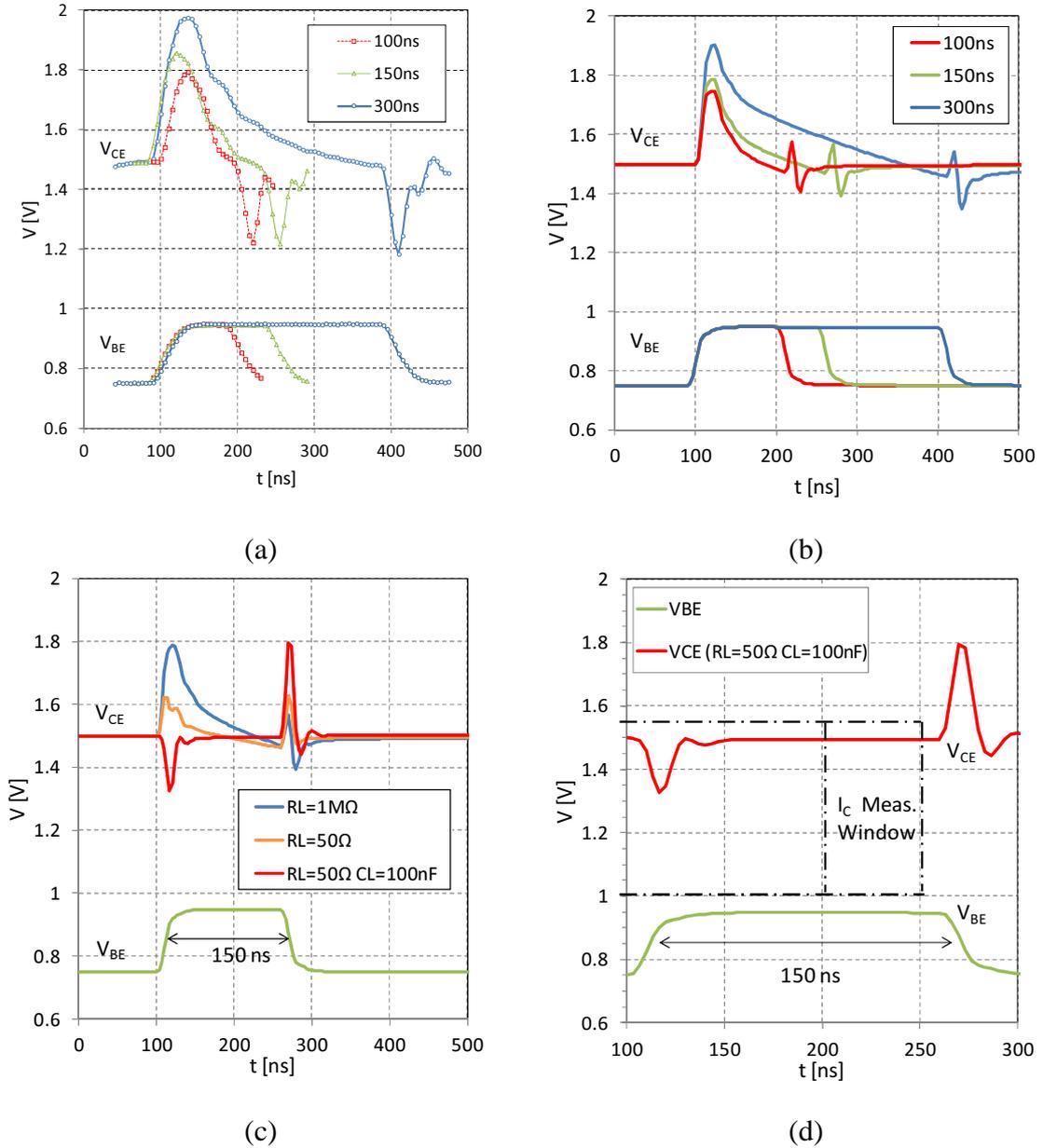


Figure 3.9: Base voltage pulses  $V_{BE}(t)$  from 0.75V to 0.95V with pulse widths  $T_w$  of 100ns, 150ns and 300ns and a constant collector voltage  $V_{CE}$  of 1.5V are (a) applied to the HBT and (b) simulated with an HBT model. (c)  $V_{CE}$  stability optimization by applying (i) a load resistance  $R_L$  of  $1M\Omega$ , (ii)  $R_L$  of  $50\Omega$  or (iii)  $R_L$  of  $50\Omega$  and a load capacitance  $C_L$  of 100nF at the collector node of the HBT model. (d) Enlarged image section of pulse simulation with stabilized condition (iii) with indicated measurement window for collector current  $I_C(t)$ .

### 3.2.2.5.2 $V_{CE}$ stability

In Figure 3.9a, base voltage pulses  $V_{BE}(t)$  from 0.75V to 0.95V with pulse widths  $T_w$  of 100ns, 150ns and 300ns and a constant collector voltage  $V_{CE}$  of 1.5V applied at the

base of a high speed HBT are shown. During the base pulse, a  $V_{CE}$  overshoot is observed that results in a maximum  $V_{CE}$  deviation of 15% in the measurement window for a base pulse of 100ns. Similar overshoot effects have been reproduced with circuit simulations of the PMS, shown in Figure 3.9b. The stability of  $V_{CE}$  during the pulse can be improved by applying at the collector node (i) a load resistance  $R_L$  of  $50\Omega$  or (ii) a load resistance  $R_L$  of  $50\Omega$  and a load capacitance  $C_L$  of 100nF as shown in Figure 3.9c. Best results are achieved with the latter configuration (see Figure 3.9d). However, the current flowing through the capacitance  $I_{C_{cap}}$  modifies the measured collector current  $I_{C,meas}$  while the actual collector current  $I_C$  does not change. In order to assure that  $I_{C,meas}=I_C$ , DC pulsed I-V characteristics are measured in a first run without connecting the capacitance. In a second step, the capacitance is connected and pulsed RF measurements are carried out.

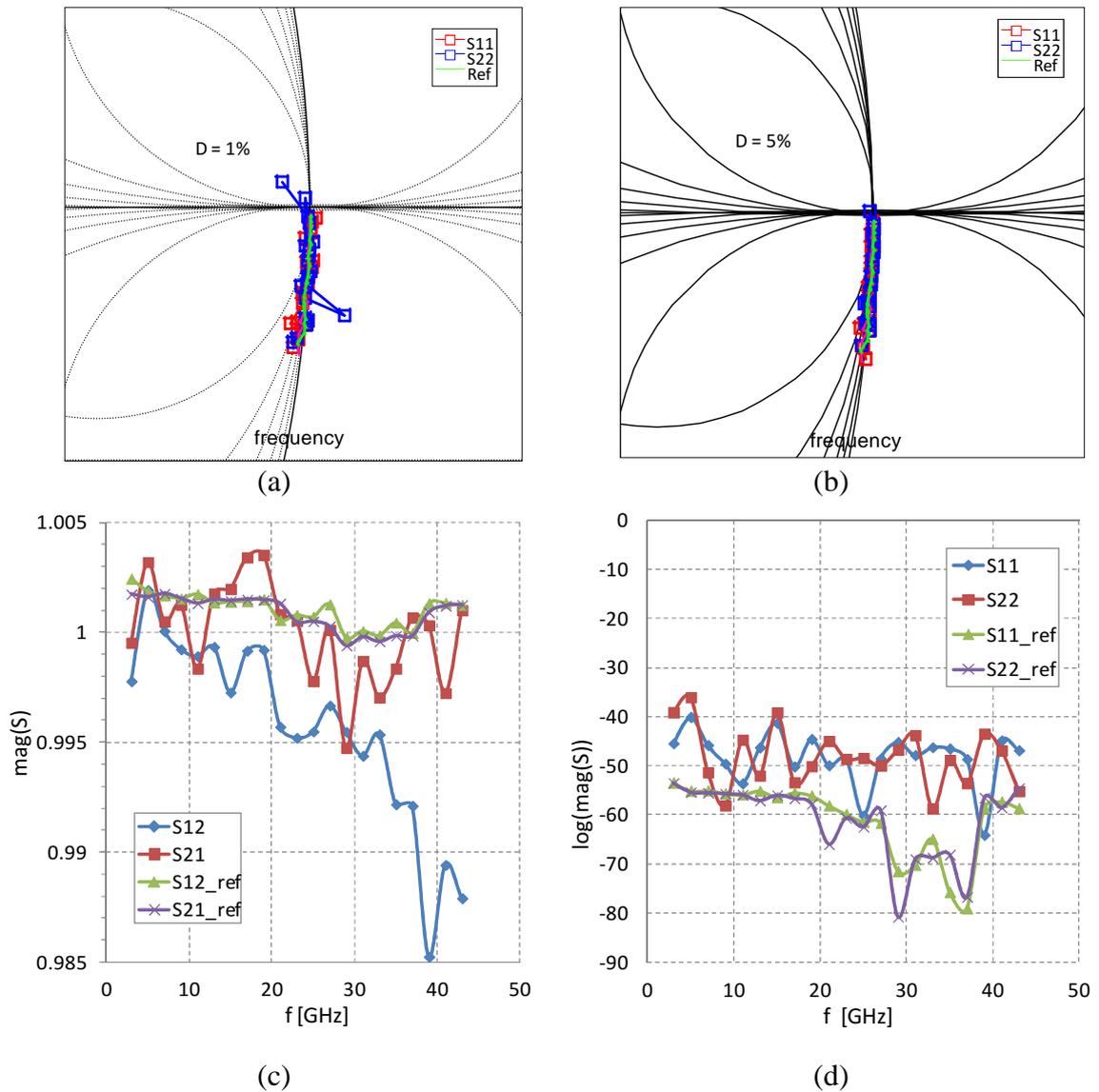


Figure 3.10: Comparison of conventional RF (as reference) and pulsed RF measurements from 3GHz to 43GHz performed on calibration standards (ISS): (a)  $S_{11}$ ,  $S_{22}$  of an

Open structure with a duty cycle  $D$  of 1%; (b)  $S_{11}$ ,  $S_{22}$  of an Open structure with a duty cycle  $D$  of 5%; (c)  $S_{12}$ ,  $S_{21}$  and (d)  $S_{11}$ ,  $S_{22}$  of a Thru structure with duty cycle  $D$  of 5%.

### 3.2.2.5.3 Duty cycle

The duty cycle defines the time that the DUT operates in an active state as a fraction of the total period. Moreover, it is a limiting factor for achieving sufficient measurement precision. Therefore, pulsed S parameters have been compared with standard S parameter measurements, as shown for a measured Open (see Figure 3.10a and Figure 3.10b) and Thru structure (see Figure 3.10c and Figure 3.10d). Since the VNA measures during the full pulse period, a small duty cycle brings the RF signal level close to the VNA noise level [106]. In this configuration, pulsed S parameters with a duty cycle below 1% lack of accuracy (see in Figure 3.10a measured Open standard). Good agreement was achieved between conventional and pulsed RF measurements with a duty cycle  $D$  of 5%.

Pulsed simulations allow us to verify if the device has enough time to cool down within a period. In Figure 3.11, two pulse periods of  $V_{BE}(t)$  as well as the internal temperature rise  $\Delta T(t)$  calculated by the compact model are shown. The device is pulsed from 0.25V to 0.95V at the base node with  $T_w$  of  $3\mu\text{s}$  and a constant  $V_{CE}$  of 1.5V. It is shown that the device needs around  $2\mu\text{s}$  in order to completely cool down. Hence, for a pulse width of 100ns, the duty cycle should not be larger than 5%.

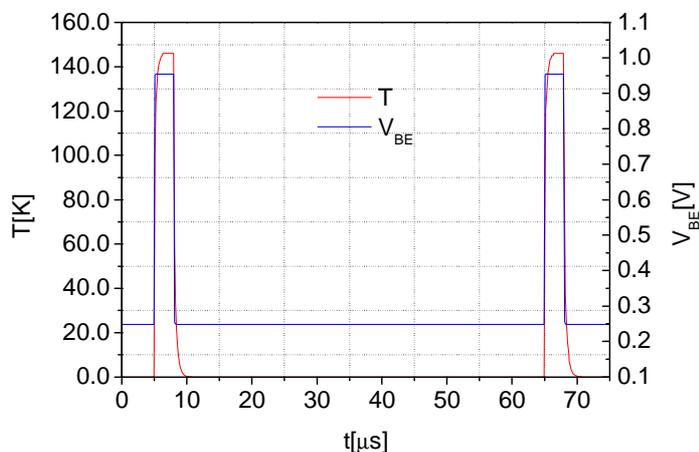


Figure 3.11: Duty cycle verification with pulsed simulations: Pulse width  $T_w=3\mu\text{s}$  and duty cycle  $D=5\%$ .

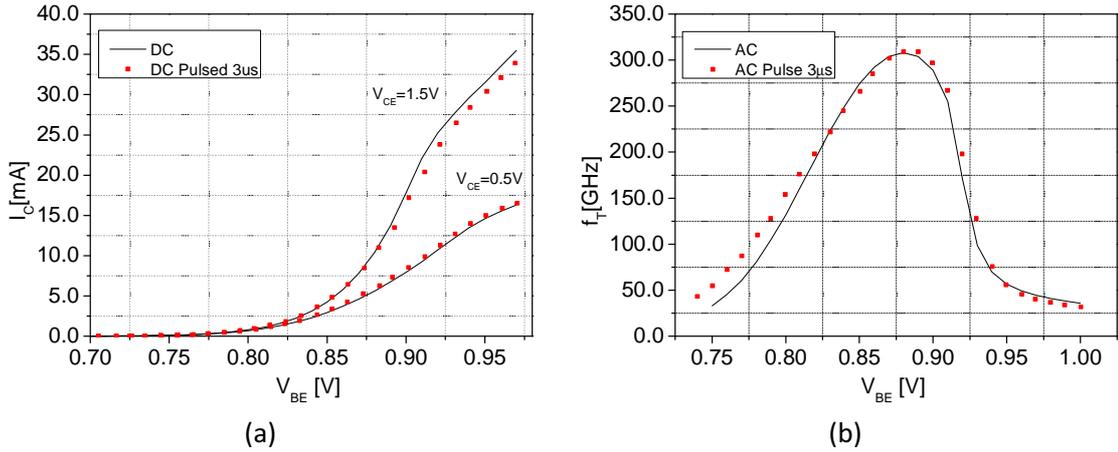


Figure 3.12: Validation of PMS with conventional DC and RF measurements: (a) Base-emitter voltage  $V_{BE}$  versus collector current  $I_C$  and (b) transit frequency  $f_T$  versus base emitter voltage  $V_{BE}$  measured with 3 $\mu$ s pulse width for constant collector emitter voltages  $V_{CE}=[0.5,1.5]V$  for an HBT with a drawn emitter area  $A_E=0.18 \times 5 \mu m^2$ .

### 3.2.2.6 Verification with conventional DC/AC measurements

From measurements and simulations it has been found that the thermal steady state of a B5T HBT with a drawn emitter window  $A_E=0.18 \times 5 \mu m^2$  is reached above a pulse width of 3 $\mu$ s. Therefore, conventional DC measurements (Agilent 4155B) and 3 $\mu$ s pulsed measurements are compared in Figure 3.12a. Moreover, S parameters were measured from 1GHz to 45GHz using VNA Rohde & Schwarz ZVA67. The transit frequency  $f_T$  shown in Figure 3.12b is extracted at 15GHz. In steady state condition, pulsed and conventional measurements give consistent results, as expected.

### 3.2.2.7 Pulsed DC results

Figure 3.13a and Figure 3.13c show pulsed measured output curves obtained for a HBT with a drawn emitter window  $A_E=0.27 \times 5 \mu m^2$  and  $A_E=0.84 \times 5 \mu m^2$ . Measurements were carried out with pulse widths from 80ns up to 50 $\mu$ s. The good agreement between long pulse widths and standard DC measurements validates the consistency of the system. It can be observed that  $I_C$  increases as pulse duration becomes longer. The longer the pulse width, the more DC power is dissipated in the device and, therefore, the higher is the internal device temperature. Figure 3.13b and Figure 3.13d show the  $I_C$  increase for a given  $V_{CE}$  as a function of the pulse width. These characteristics have been extracted from Figure 3.13a and Figure 3.13c, respectively, by collecting the measured  $I_C$  values at a given  $V_{CE}$  for each pulse width. For the narrowest pulse widths, it can be observed that  $I_C$  tends to a steady value; hence, an almost isothermal measurement is achieved.

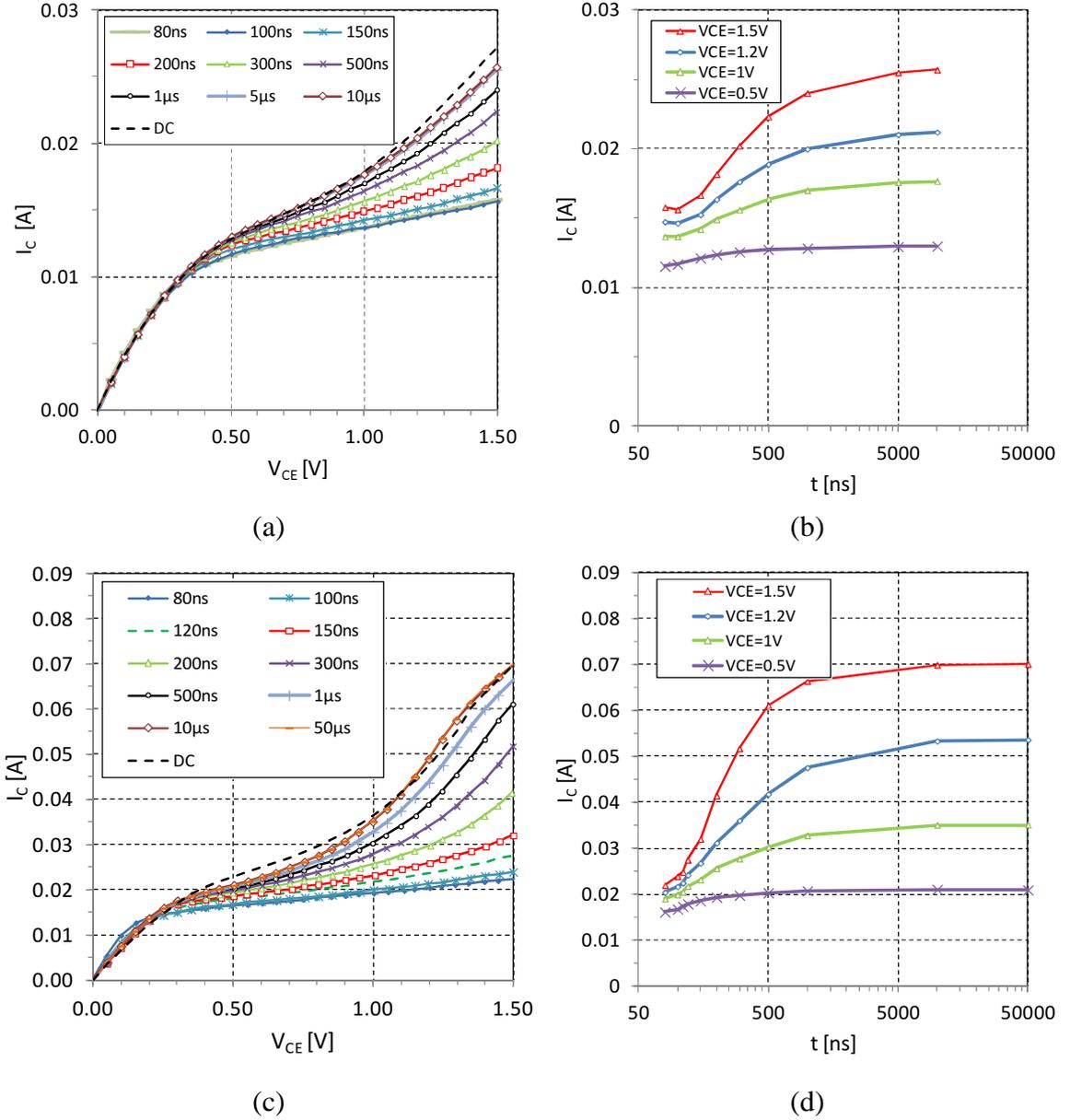


Figure 3.13: Output characteristics for  $V_{BE}=0.95V$  measured with various pulse widths from 80ns up to  $50\mu s$  for an HBT with (a)  $A_E=0.27 \times 5\mu m^2$  and (c)  $A_E=0.84 \times 5\mu m^2$ . Collector current  $I_C$  versus pulse width  $T_w$  for different collector emitter voltages  $V_{CE}$  for an HBT with (b)  $A_E=0.27 \times 5\mu m^2$  and (d)  $A_E=0.84 \times 5\mu m^2$ .

### 3.2.2.8 RF results

Figure 3.14 shows  $V_{BE}$  versus  $I_C$  and the current gain cut-off frequency  $f_T$  versus  $V_{BE}$  for a HBT with  $A_E=0.5 \times 5\mu m^2$ . S parameters are obtained up to 45GHz as a function of  $V_{BE}$  from 0.8V to 0.98V for  $V_{CE}=[0.5, 1.5]V$ . S parameters were de-embedded with an Open structure and the  $f_T$  is extracted at 15GHz. For  $V_{CE}=0.5V$  internal self-heating is very small, therefore, measurements for various pulse widths should be close to each other, as can be observed in Figure 3.14. On the other hand, for  $V_{CE}=1.5V$ , the transistor is significantly heated resulting in higher  $I_C$  and lower peak  $f_T$  for longer pulse widths.

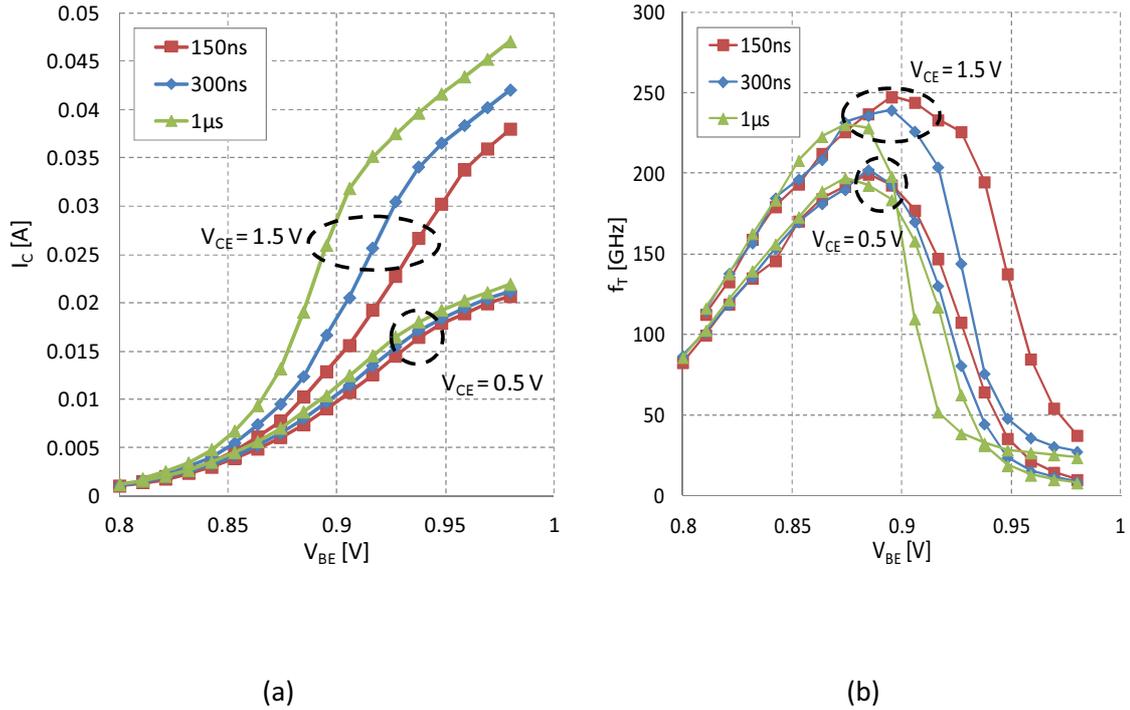


Figure 3.14: (a) Base-emitter voltage  $V_{BE}$  versus collector current  $I_C$  and (b) transit frequency  $f_T$  versus base emitter voltage  $V_{BE}$  measured with 150ns, 300ns and 1μs pulse widths at constant collector emitter voltages  $V_{CE}=[0.5,1.5]$ V for an HBT with  $A_E=0.5 \times 5 \mu\text{m}^2$ .

### 3.2.2.9 Discussion

In Figure 3.15, the DC compact model of an HBT with  $A_E=0.18 \times 5 \mu\text{m}^2$  (lines) is compared with pulsed measurements (symbols). Two simulations have been carried out: (i) Using the compact model with the extracted thermal network (green line); (ii) using the compact model without self-heating (black line). The comparison of the pulse measurement for 100ns with isothermal simulation shows that isothermal condition is not fully reached but that the internal junction temperature of the device is significantly reduced. Nonetheless the obtained device characteristics are almost isothermal and enable new possibilities for model parameter determination. Moreover, the system allows transient thermal impedance measurement [82] for further investigations.

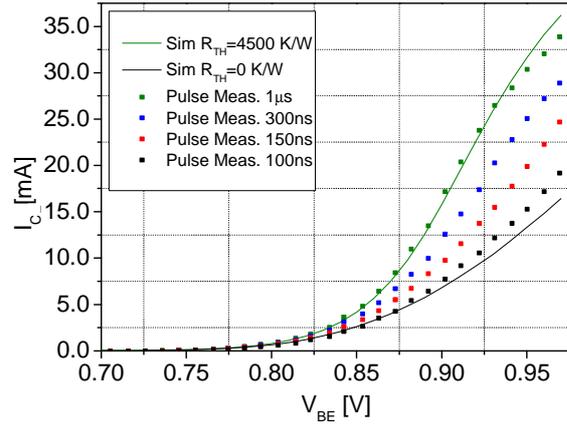


Figure 3.15: Base-emitter voltage  $V_{BE}$  versus collector current  $I_C$ : Comparison of pulsed measurement (symbols) and DC simulation (line) with self-heating and without self-heating at a constant collector emitter voltage  $V_{CE}=1.5V$  for an HBT with  $A_E=0.18 \times 5 \mu m^2$ .

### 3.3 Distributed electrothermal modeling

In general, distributed models describe spatial and temporal variations more realistic than simpler lumped models. Lumped models are rather inadequate when the data have high spatial and temporal resolution. For example, transient thermal heating effects or thermal coupling between devices cannot be accurately modeled with the standard thermal network integrated in most compact models. In this Section, the conventional single pole thermal network is replaced with higher order networks that better embodies the physics background of the electrothermal heating phenomenon.

#### 3.3.1 Thermal impedance model

##### 3.3.1.1 Recursive electrothermal network

The passive thermal network represents the dynamic link between instantaneous power dissipation and the temperature variation due to self-heating. In most common compact models, the distributed thermal network is reduced to a single pole electrothermal equivalent network as shown in Figure 3.16a. The corresponding thermal impedance is given by (3.1) with  $n=1$

$$Z_{th}(j\omega) = \frac{R_{th}}{1 + j\omega R_{th} C_{th}}. \quad (3.26)$$

In many cases, a single  $R_{th}$  and  $C_{th}$  is sufficient since the temperature at microwave frequencies is considered to be constant. However, at intermediate frequencies the device thermal impedance is not purely resistive. Instead, it corresponds to a distributed low pass filter with an infinite number of time constants.

In the literature, several thermal equivalent circuits like Foster, Nodal or recursive networks were proposed in order to model the dynamic thermal behavior more accurately. Such networks should be related to the real physical structure of the device and should have as less as possible additional model parameters. Moreover, good convergence in a circuit simulator and low calculation time are necessary. A comparative study has been proposed in [82] where a recursive thermal network (Figure 3.16b) equivalent to a transmission line was found to be the most suitable. Several studies [100], [104], [109] have verified the accuracy and the applicability of this network, and therefore, it is applied in this work.

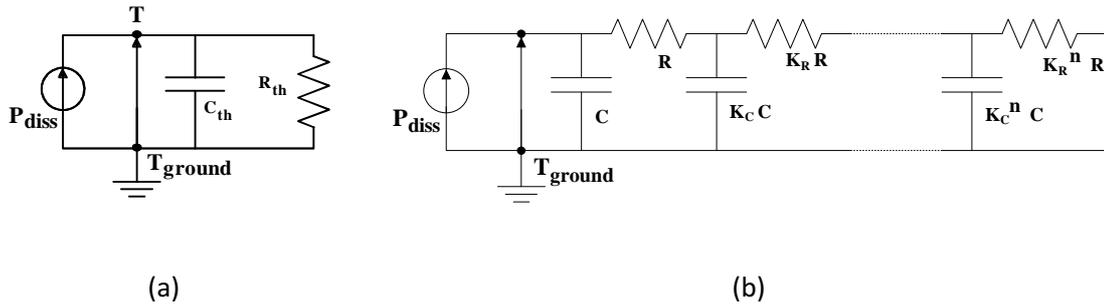


Figure 3.16: (a) Single pole thermal network (b) n-cell Recursive thermal network.

The recursive network shown in Figure 3.16b consists of distributed resistance capacitance (RC) pairs where the sum of series resistances is equal to  $R_{th}$  of the single pole network.

$$R_{th} = \sum_{n=0}^N K_r^n \cdot R \quad (3.27)$$

In DC condition both networks give the same results since the thermal capacitance  $C_{th}$  has no effect and  $Z_{th}(\omega \rightarrow 0) = R_{th}$ .

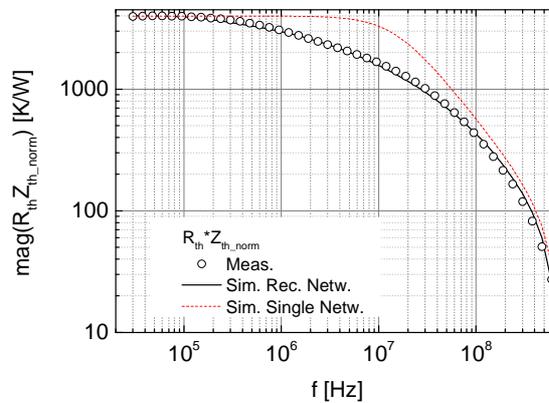


Figure 3.17: Magnitude of  $R_{th} Z_{th\_norm}$  vs. frequency for a SiGe HBT with  $A_E=0.18 \times 5 \mu\text{m}^2$ . Measurements (symbols) are compared to simulations using single pole (solid line) and recursive network (dashed line).

The recursive network was verified in terms of accuracy with increasing number of cells in [82]. Note that, using only one cell is equal to the single-pole network. In [82], it is observed that a higher number of cells provides better accuracy. However, in this work, a nine cell network is used since the difference to higher order networks is deemed not significant enough to further enhance the accuracy of the simulation. Magnitude of the normalized thermal impedance multiplied with  $R_{th}$  is shown in Figure 3.17. It is obvious that, the measured thermal impedance is not accurately modeled with the standard single pole thermal network ( $R_{th}=4000\text{K/W}$ ,  $C_{th}=2.9\text{pWs/K}$ ). Thermal parameters for the 9 cell recursive network are extracted from normalized  $Z_{th\_norm}$  ( $R=1300\text{K/W}$ ,  $C=2.8\text{pWs/K}$ ,  $K_R=0.9$  and  $K_C=1.8$ ). The recursive network in combination with extracted parameters is significantly more precise at lower frequencies. Furthermore, this can be observed by magnitude and phase of  $y_{22}$  in Figure 3.18.

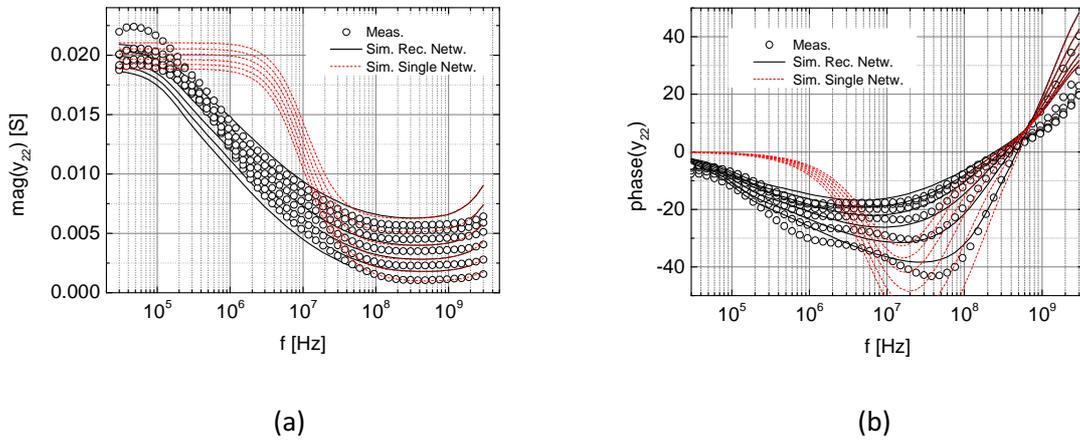


Figure 3.18: Comparison of (a) magnitude and (b) phase of  $y_{22}$  among different electrothermal networks.

For higher frequencies, no thermal feedback occurs; thus, there is no difference between the two networks. However, millimeter-wave circuits often generate also low frequency products due to intermodulations. In [110], it was observed that self-heating process can have a significant impact on intermodulation of broad-band signals. Moreover, in [111], it was demonstrated that thermal memory effects seriously limit the maximum achievable cancellation performance of predistortion linearization of a power amplifier.

### 3.3.1.2 The recursive network and pulsed characteristics

In this section, pulse measurements are compared with pulse simulations (see Paragraph 3.2.2.5.1) using the transistor compact model. The compact model should provide good accuracy for frequencies lower than the thermal time constant to accurately determine the transistor junction temperature in pulsed condition. In the measurements and the simulations pulse widths from 100ns up to 1 $\mu$ s were applied. Pulsed simulations

using the conventional single pole (Figure 3.19a) and the nine stage recursive network (Figure 3.19b) were compared in terms of accuracy. Simulations using the conventional thermal network are inadequate to fit properly the measured output characteristics. The deviation is caused due to the mismatch of thermal impedance in the frequency domain (Figure 3.17). In contrast, very good agreement for output (Figure 3.19b) and  $V_{BE}$  versus  $I_C$  characteristics (Figure 3.19c) can be observed using the recursive network. When a transient pulse is applied to the device, theoretically an infinite number of thermal time constants are necessary to represent the thermal response. Hence, dynamic self-heating could not be properly modeled using a single pole network, as it has only a single time constant [112].

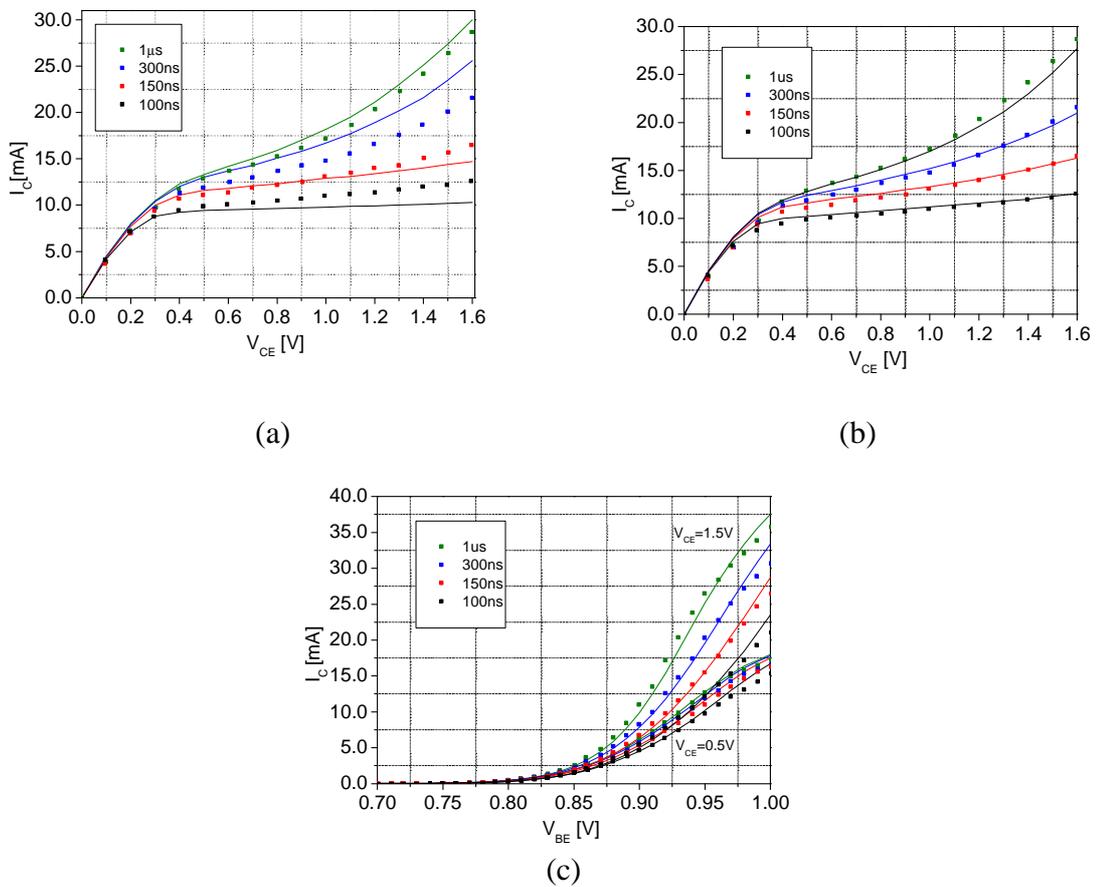


Figure 3.19: Simulations (lines) and measurements (symbols) for a SiGe HBT with  $A_E = 0.18 \times 5 \mu\text{m}^2$ . Output characteristics at  $V_{BE} = 0.95$  V for various pulse widths from 100ns up to 1  $\mu$ s obtained by applying a single pole (a) and recursive (b) network at the temperature node of the compact model. (c)  $I_C$  versus  $V_{BE}$  characteristics for  $V_{CE} = [0.5, 1.5]$  V (simulations with the recursive network).

### 3.3.2 Distributed thermal coupling model

In addition to their own self-heating, devices in close proximity can experience a temperature increase due to thermal coupling. In [113], it was demonstrated that thermal

coupling can have significant impact on circuit performance. A common case where thermal coupling should be considered is in multi-transistor arrays (MTAs) and multi-finger transistors (MFTs). The individual transistors/fingers, depending on trench isolation and proximity, can be strongly thermally coupled through the substrate. MFTs are often used since they are more suitable for high frequency operation due to small base access resistance and capacitance.

In the design process the center fingers are considered to be the most critical. Assuming a device temperature during the design phase that differs too much from the real value, can result in thermal runaway under actual working conditions and destruction of the device in the worst case. In this section, intra-device thermal coupling in a MFT and inter-device coupling in a MTA is studied using measurements on specially designed test structures. In addition, the MFT is investigated by physical simulation. Thermal coupling parameters are extracted and implemented in a distributed transistor model.

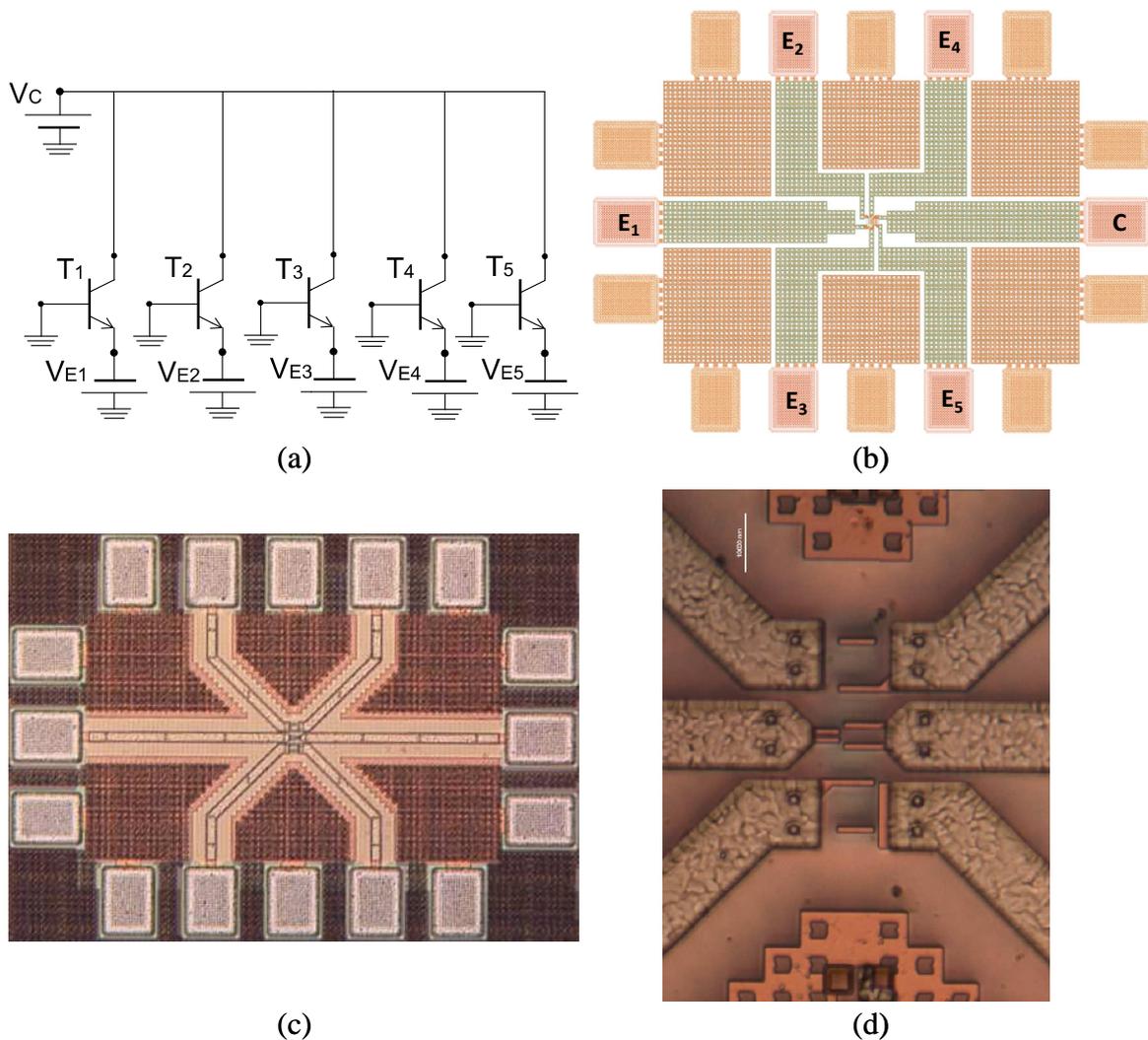


Figure 3.20: Schematic diagram (a) and layout (b) of the test structures. Micrograph (c) of test structure suitable for RF measurements and (d) of the enlarged section where the six transmission lines are connected to the emitter/collector stripes.

### 3.3.2.1 Test structures

In order to accurately model the electro-thermal behavior of high power devices, test structures are required to characterize self-heating and thermal coupling. The first test structure contains five transistors in parallel to measure the effect of inter-device coupling. The second test structure contains a MFT to measure thermal coupling between the emitter stripes (intra-device coupling).

The two test structures are similar: (i) each emitter has a drawn emitter area  $A_E=5 \times 0.18 \mu\text{m}^2$ , (ii) the five fingers/transistors are electrically connected as shown in the schematic diagram (Figure 3.20a). In this configuration each finger/transistor can be used either for heating or sensing. Each emitter port can be biased by independent voltage/current sources to control the dissipated power. The common collector is accessible which allows the base-collector voltage to be significantly reverse biased in order to generate the desired heat. The  $I_E(V_{BE})$  characteristic is used in order to sense the temperature. Therefore, each transistor has to be calibrated by measuring  $I_E(V_{BE})$  at low current densities (negligible heat generation) at different chuck temperatures. Thermal interactions can be easily studied due to the various possible heat/sense combinations.

For each structure two different versions were designed: (i) optimized for DC measurements; and (ii) optimized for RF measurements. The layout of the DC structure is displayed in Figure 3.20b. The resistance of interconnects between pads and transistors is reduced using the metal layers M3, M4, M5 and M6 in parallel. For RF measurements this would lead to a high parasitic capacitance. Therefore, a second structure with  $50\Omega$  transmission lines (only M6) was designed that is suitable for RF measurements (Figure 3.20c). The enlarged section is shown in Figure 3.20d where the six transmission lines are connected to the emitter/collector stripes. In both structures, a slotted ground plane (M1 and M2 in parallel) is connected to all base contacts.

The multi transistor array (Figure 3.21a, only two transistors are shown) has a shallow trench isolation (STI) between emitter and collector contact and each transistor is surrounded by a deep trench isolation (DTI). In the MFT (Figure 3.21b) the adjacent fingers share the collector stripes at the side, hence, the emitters (heat sources) have no thermal isolation (DTI) and are closer to each other in comparison to the MTA (distance between emitter fingers  $D_{\text{Finger}}=5\mu\text{m}$ , distance between emitter contacts of single transistors  $D_{\text{Transistor}}=[7, 9, 11]\mu\text{m}$ ). Therefore, higher thermal coupling is expected in the MFT. A 3D sketch of both devices is shown in Figure 3.22.

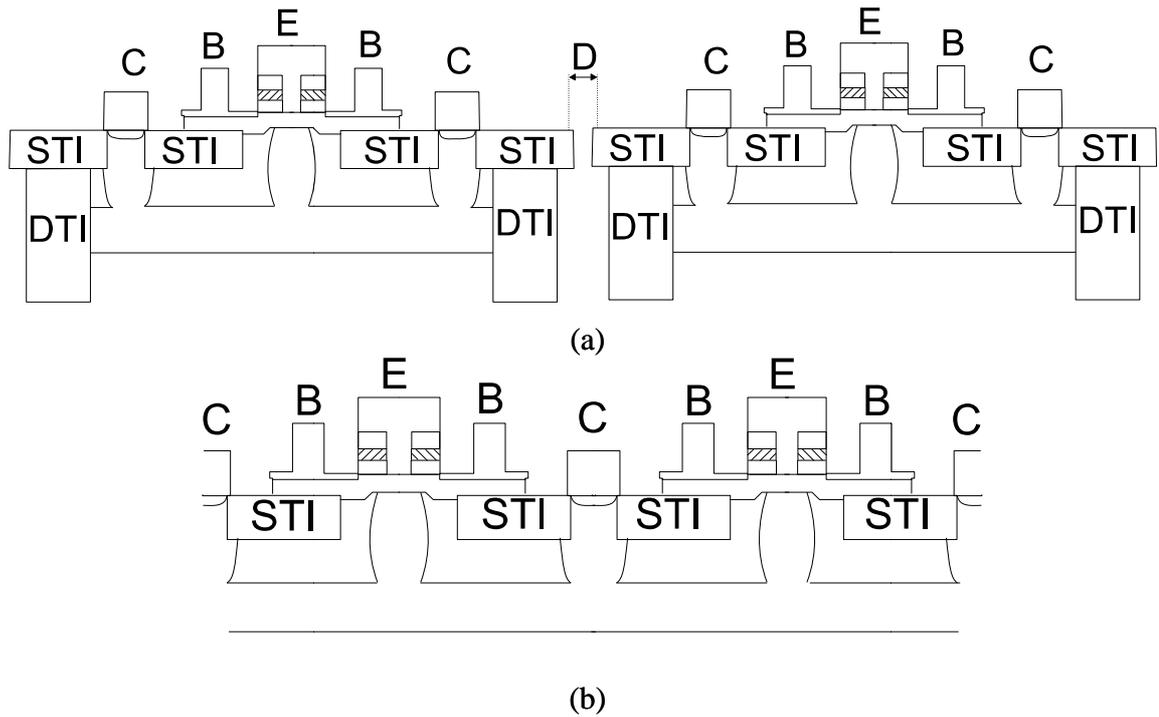


Figure 3.21: (a) Multi-transistor structure with STI and DTI (distance  $D$  between the deep trench walls). (b) Multi-finger-transistor structure with shared collector contacts.

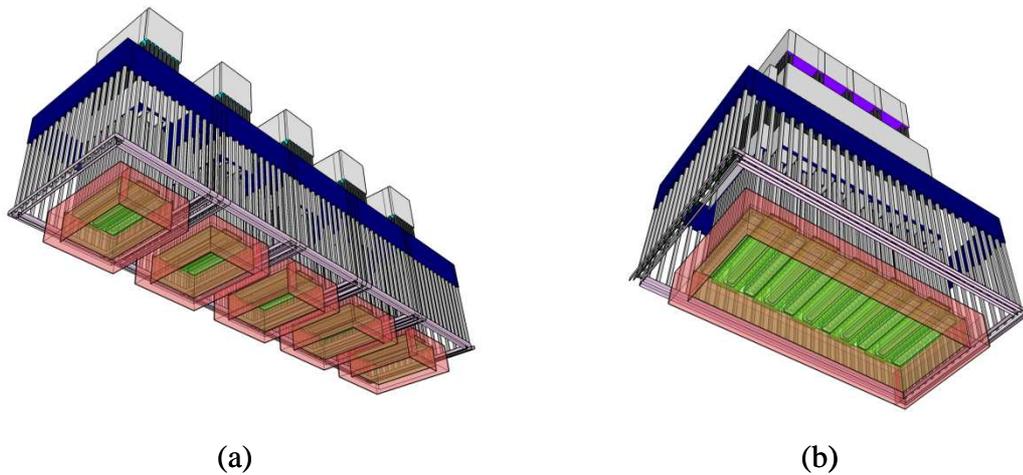


Figure 3.22: A 3D sketch of (a) the five-transistor array (MTA) with STI and DTI (distance  $D$  of  $3\mu\text{m}$  between the deep trench walls) and (b) the five-finger transistor (MFT).

### 3.3.2.2 $V_{BE}$ variation as thermometer

When using bipolar transistors as thermometer there are mainly three temperature sensitive quantities that have been widely used in the literature [94]: (i) collector reverse saturation current, (ii) current gain and (iii) forward base-emitter junction voltage  $V_{BE}$ . The latter has been chosen since  $V_{BE}(T, I_E=\text{const})$  is almost linear, easy predictable and varies little among similar devices.

In constant current mode, the negative thermal feedback leads to a decrease in  $V_{BE}$  with temperature. In the proposed setup, an emitter current is forced while  $V_{BE}$  is meas-

ured. In order to calibrate the fingers/transistors  $V_{BE}$  was measured at different chuck temperatures ranging from 300K to 373K and for different forced emitter currents  $I_E$  (see Figure 3.23a). In general, the temperature coefficient  $K$  (Figure 3.23b) is calculated with

$$K = \frac{T_{high} - T_{low}}{V_{BE}(T_{high}) - V_{BE}(T_{low})} \cdot \quad (3.28)$$

Having  $K$  and the measured change in base-emitter voltage  $\Delta V_{BE}$  the temperature rise can be determined with

$$\Delta T_j = K \cdot \Delta V_{BE} \cdot \quad (3.29)$$

For further investigations, the forced emitter current  $I_E$  is chosen to be  $1\mu\text{A}$  where the internal self-heating can be neglected and where the BE junction has a sufficiently high temperature sensitivity to enable the required measurement accuracy.  $K$  does not significantly differ between transistors/fingers having the same emitter dimensions.

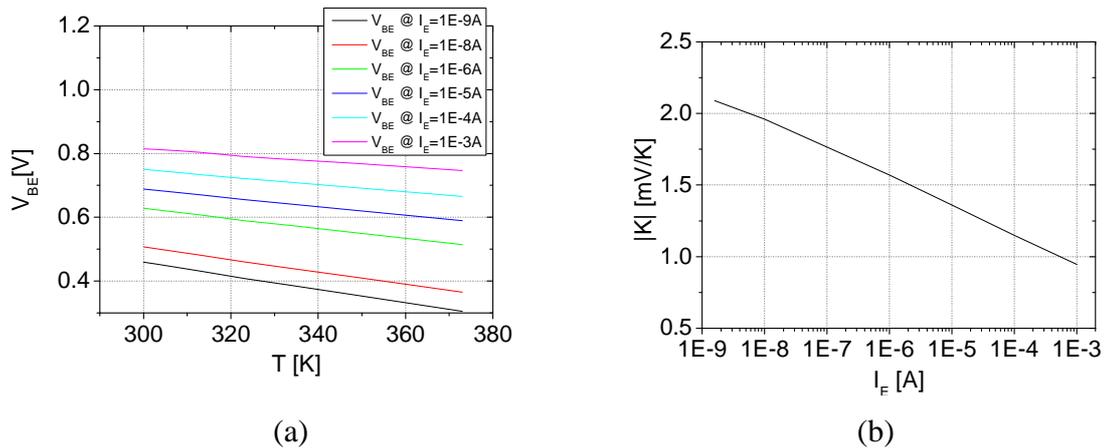


Figure 3.23: (a) Measured  $V_{BE}$  at different chuck temperatures ranging from 300K to 373K and for several forced emitter currents  $I_E$ . (b) Absolute value of the temperature coefficient  $K$  vs. the emitter current  $I_E$ .

### 3.3.2.3 Extraction of thermal coupling factors from measurements

On-wafer measurements were carried out at room temperature using a SUSS MicroTec probing station equipped with a thermal chuck. DC as well as RF structures are embedded in GSG pads to avoid oscillations. Probing was done with two differential GSGSG probes (SUSS MicroTec) and two GSG probes (Picoprobe). Measurements were obtained using the DC analyzer HP4155A using the four Source/Monitor Units (SMUs) and two Voltage Monitor Units (VMUs). The sensing transistors are forced with an emitter current  $I_E$  of  $1\mu\text{A}$  while  $V_{BE}$  is measured. The temperature is then calculated using the extracted  $K$ . In this operating condition a sensitivity of around  $-1.55\text{mV/K}$  (see Figure 3.23b) is achieved. The heating transistors are operated in forward direction at different dissipated power levels  $P_{diss}$ .

Figure 3.24 shows the resulting temperature rises  $\Delta T$  in the case when only T4 (see schematic diagram in Figure 3.20a) is heating.  $V_{BE}$  of T4 is increased while  $V_{BC}$  is held constant at 0.5V. Firstly, T measurement in the MFT is presented in Figure 3.24a. If T4 dissipates a power of 18mW ( $I_C \approx 12\text{mA}$ ,  $V_{BE} \approx 0.91\text{V}$ ), the temperature of the adjacent fingers is increased by 11°C. If all fingers operate together this value would be more than doubled with respect to the central emitter. The thermal coupling resistance (slope) is almost linear with the dissipated power of T4. It is rather governed by the thermal conductivity and the device architecture than by the electrical operation regime. Thermal coupling between single transistors is much smaller (see Figure 3.24b). If T4 operates at the same power ( $\approx 18\text{mW}$ ) the temperature of the neighboring transistors (distance between the DTI  $D=1.5\mu\text{m}$ , see Figure 3.21) is increased by a little more than 3°C. The reduced thermal coupling effect is mainly due to the deep trench isolation around each transistor and the larger distance between the heat sources (see Figure 3.21,  $D_{\text{Finger}}=5\mu\text{m}$ ,  $D_{\text{Transistor}}=[7, 9, 11]\mu\text{m}$ ). As expected, thermal coupling further decreases with wider spacing as shown in Figure 3.24b.

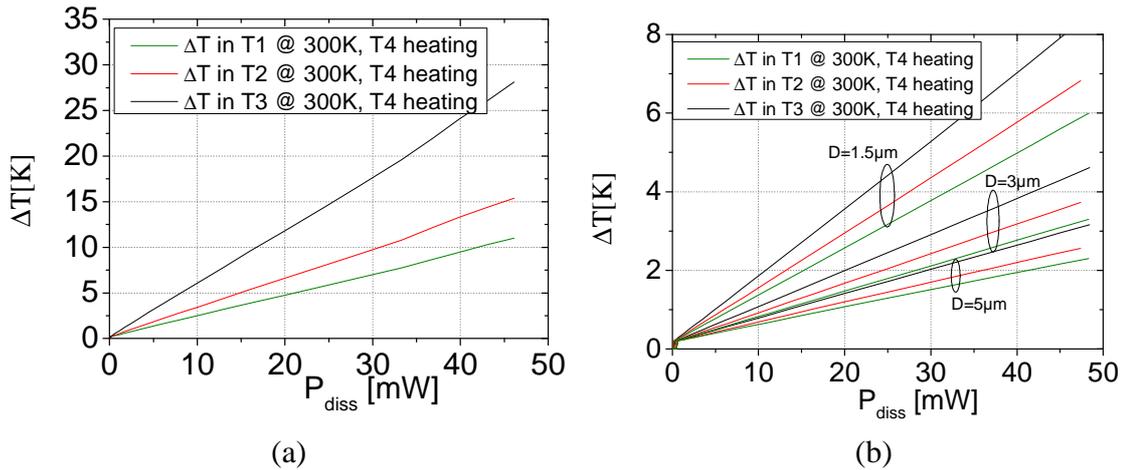


Figure 3.24: (a) Temperature increase inside emitter fingers of the MFT in the case when only T4 is heating. (b) Temperature increase inside the single transistors of the MTA for three different distances between the DTI ( $D=[1.5, 3, 5]\mu\text{m}$ ).

By measuring various heat/sense combinations the coupling factors between the fingers can be determined with

$$C_{XY} = \frac{dT_X / dP_Y}{dT_Y / dP_Y} = \frac{R_{th\_XY}}{R_{th\_YY}} \quad (3.30)$$

where  $P$  is the dissipated power and  $T$  is the temperature inside the sensing (index X) and the heating (index Y) transistor. The junction temperature  $T_Y$  is calculated with the transistor compact model ( $A_E=0.18 \times 5\mu\text{m}^2$ , validated for chuck temperatures from 27°C to 100°C in 2.4.5). The transistor measurements were carried out on the same wafer where the test structures were fabricated. In order to adapt this model also for each finger transistor the external collector resistance  $r_{cX}$  and the thermal resistance  $R_{th}$  have

been recalculated. The coupling factors for intra- and inter-device mutual thermal heating (including different transistor spacing) are plotted versus dissipated power of the heating device in Figure 3.25a and in Figure 3.25c-d, respectively.

Thermal coupling slightly decreases with  $P_{\text{diss}}$ . Since the sensed temperature rise must be smaller than the temperature rise in the heating device, it follows that  $R_{\text{th}_{YY}} > R_{\text{th}_{XY}}$ . Moreover,  $R_{\text{th}}$  rises with temperature due to nonlinear thermal conductivity of silicon [114]. Considering this for  $R_{\text{th}_{YY}}$  and  $R_{\text{th}_{XY}}$  in (3.30),  $R_{\text{th}_{YY}}$  increases faster than  $R_{\text{th}_{XY}}$  with  $P_{\text{diss}}$ , and therefore,  $C_{XY}$  decreases. The coupling factors between direct neighbors ( $C_{12}$ ,  $C_{21}$ ,  $C_{32}$ , etc.) and indirect neighbors with one ( $C_{13}$ ,  $C_{31}$ ,  $C_{35}$  etc.) or two ( $C_{14}$ ,  $C_{25}$ ) devices in between hardly differ from each other due to symmetric heating. Differences are a little more pronounced for the multi-finger transistor due to varying distances between finger positions and deep trench walls.

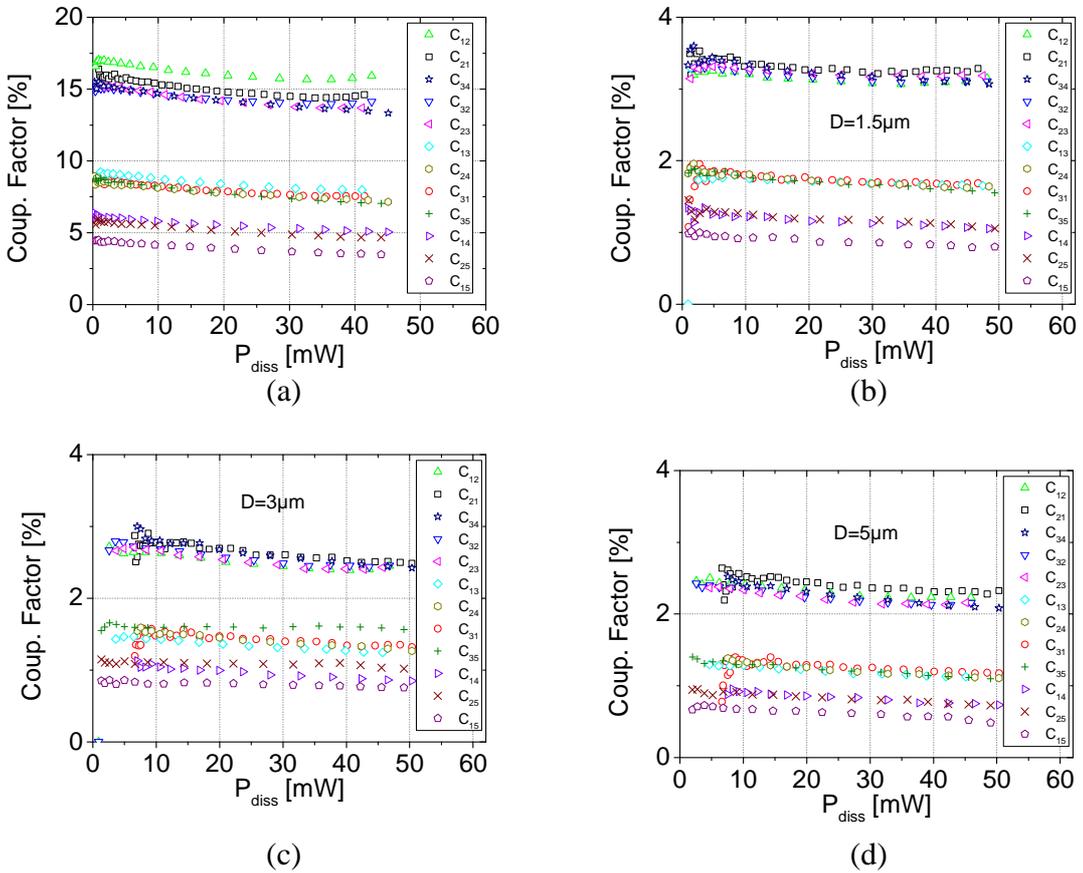


Figure 3.25: Thermal coupling parameters  $C_{XY}$  plotted versus the dissipated power of the heating transistor  $T_Y$  for intra- and inter-device coupling: (a) MFT, (b, c and d) MTA with distance between DTI  $D=[0.15, 0.3, 0.5]\mu\text{m}$ , respectively.

At low power, thermal coupling is negligible. Hence, a practical region to extract the coupling parameters is probably before peak  $f_T$  is reached. Regarding Figure 3.26, where  $f_T$  versus  $P_{\text{diss}}$  is plotted, it is rather not useful to operate the transistor higher than 15mW. Therefore, thermal coupling factors for intra- (see Table 2) and inter-device (see

Table 3, Table 4 and Table 5) heating are extracted at a dissipated power  $P_{\text{diss}} \approx 10\text{mW}$ . In addition, the  $C_{XY}(P_{\text{diss}})$  dependence is rather weak in this case (see Figure 3.25); the extracted  $C_{XY}$ -values can be used for a wide bias range.

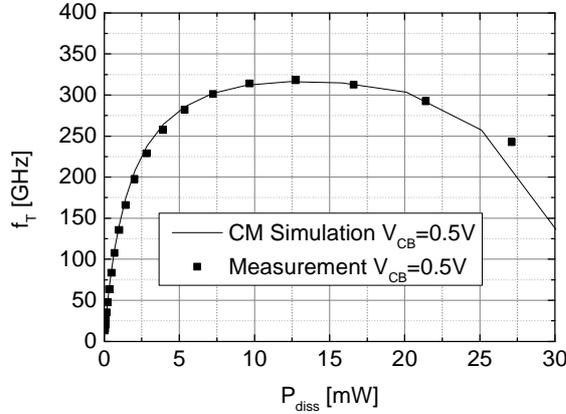


Figure 3.26: Transit frequency  $f_T$  versus dissipated power  $P_{\text{diss}}$  at collector-base voltage  $V_{\text{CB}}=0.5\text{V}$ .

Heating Finger	Thermal coupling factors $C_{XY}$ [%]				
	T1	T2	T3	T4	T5
T1	100%	15.30%	8.22%	5.29%	4.04%
T2	16.33	100%	14.55%	8.05%	5.70%
T3	8.70	14.62%	100%	14.62%	8.70%
T4	5.70	8.05%	14.52%	100%	16.33%
T5	4.04	5.29%	7.96%	15.30%	100%

Table 2: Thermal coupling parameters between the five transistor fingers ( $A_E=[0.18 \times 5]\mu\text{m}^2$ ) T1, T2, T3, T4 and T5 extracted from measurements at a dissipated power  $P_{\text{diss}} \approx 10\text{mW}$ .

Heating transistor	Thermal coupling factors $C_{XY}$ [%]				
	T1	T2	T3	T4	T5
T1	100%	3.41%	1.79%	1.25%	0.93%
T2	3.21%	100%	3.24%	1.84%	1.25%
T3	1.75%	3.28%	100%	3.28%	1.75%
T4	1.25%	1.84%	3.44%	100%	3.21%
T5	0.93%	1.25%	1.76%	3.41%	100%

Table 3: Thermal coupling parameters between parallel connected transistors ( $A_E=[0.18 \times 5]\mu\text{m}^2$ ) T1, T2, T3, T4 and T5 (distance between deep trench walls  $D=1.5\mu\text{m}$ ) extracted from measurements at a dissipated power  $P_{\text{diss}} \approx 10\text{mW}$ .

Heating transistor	Thermal coupling factors $C_{XY}$ [%]				
	T1	T2	T3	T4	T5
T1	100%	2.69%	1.54%	1.11%	0.81%
T2	2.63%	100%	2.68%	1.50%	1.04%
T3	1.43%	2.66%	100%	2.66%	1.43%
T4	1.04%	1.50%	2.81%	100%	2.63%
T5	0.81%	1.11%	1.59%	2.69%	100%

Table 4: Thermal coupling parameters between parallel connected transistors ( $A_E=[0.18 \times 5] \mu\text{m}^2$ ) T1, T2, T3, T4 and T5 (distance between deep trench walls  $D=3 \mu\text{m}$ ) extracted from measurements at a dissipated power  $P_{\text{diss}} \approx 10 \text{mW}$ .

Heating transistor	Thermal coupling factors $C_{XY}$ [%]				
	T1	T2	T3	T4	T5
T1	100%	2.49%	1.30%	0.88%	0.67%
T2	2.41%	100%	2.36%	1.33%	0.91%
T3	1.29%	2.34%	100%	2.34%	1.29%
T4	0.91%	1.33%	2.38%	100%	2.41%
T5	0.67%	0.88%	1.30%	2.49%	100%

Table 5: Thermal coupling parameters between parallel connected transistors ( $A_E=[0.18 \times 5] \mu\text{m}^2$ ) T1, T2, T3, T4 and T5 (distance between deep trench walls  $D=5 \mu\text{m}$ ) extracted from measurements at a dissipated power  $P_{\text{diss}} \approx 10 \text{mW}$ .

### 3.3.2.4 Extraction of thermal coupling factors from TCAD simulations

The 3D-nature of the heat flow inside transistors makes simple approximations of compact models of limited value. Predictive methods, therefore, require the accurate representation derived from numerical simulation. Thermal TCAD simulations were made with the Sentaurus device version E-2010.12 [115] which is a multidimensional simulator for semiconductor devices.

In this steady state thermal analysis, the BC junction of the device is considered to be the “heat source” due to the high power density. The heat source is defined by a thermode in Sentaurus, which is an isothermal surface. The available model is the “Sentaurus Electrothermal Resistance” model as shown in Figure 3.27. The electrothermal resistance has two electrical contacts (electrodes  $u_1$  and  $u_2$ ) and one thermal contact (thermode  $t$ ). The electrical behavior of the resistance is described by the Ohm’s law and the dissipated power ( $P_{\text{diss}}=(U_1-U_2)I$ ) is equivalent to the generated heat flow inside the device.

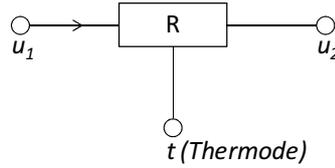


Figure 3.27: Senterius electrothermal resistance model.

Due to the symmetry of the device,  $\frac{1}{2}$  of the five finger HBT structure is built on a semi-infinite Si-block (see Figure 3.28). The thickness of the substrate region is  $300\mu\text{m}$  as the wafer thickness. The five base-collector (BC) junctions (heat sources) are equal to effective emitter area ( $L_{E\_eff} \times W_{E\_eff}$ ) and have been placed with exact technological (B5T) distances from each other. The heat sources are surrounded by  $\text{SiO}_2$  shallow trench isolation (STI) and the whole structure is surrounded by  $\text{SiO}_2$  (filled with polysilicon) deep trench isolation (DTI). The boundary surfaces of the Si-block are adiabatic, i.e. there is no heat flow to the surroundings. The wafer back-side is isothermal and initially kept at ambient temperature ( $300\text{K}$ ) which is considered as the “thermal ground” ( $T_{amb}$ ). Only the lower device part starting from BC junction to  $T_{amb}$  is simulated. A temperature dependent thermal conductivity  $\kappa$  is used in Senterius Device which is given by the following equation

$$\kappa(T) = \frac{1}{\kappa_a + \kappa_b T + \kappa_c T^2} \quad (3.31)$$

where  $\kappa_a = 0.03 \text{ cmKW}^{-1}$ ,  $\kappa_b = 1.56 \times 10^{-3} \text{ cmW}^{-1}$  and  $\kappa_c = 1.65 \times 10^{-6} \text{ cmW}^{-1}\text{K}^{-1}$  (for silicon). The range of validity is from  $200\text{K}$  to well above  $600\text{K}$  (taken from Senterius device [115] user manual).

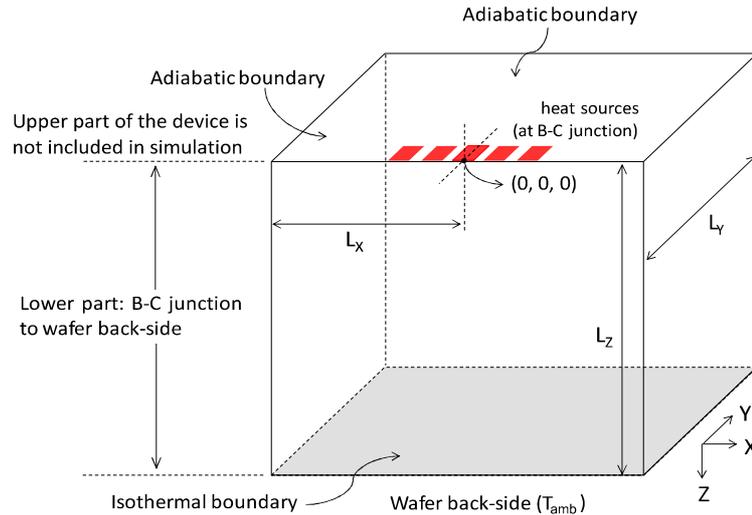
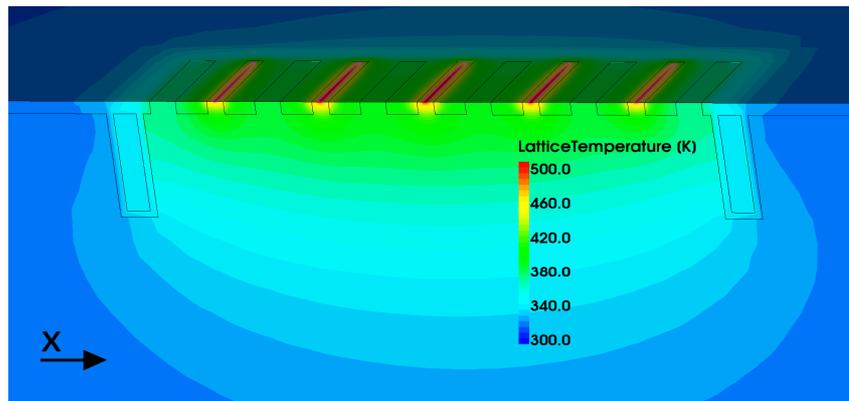


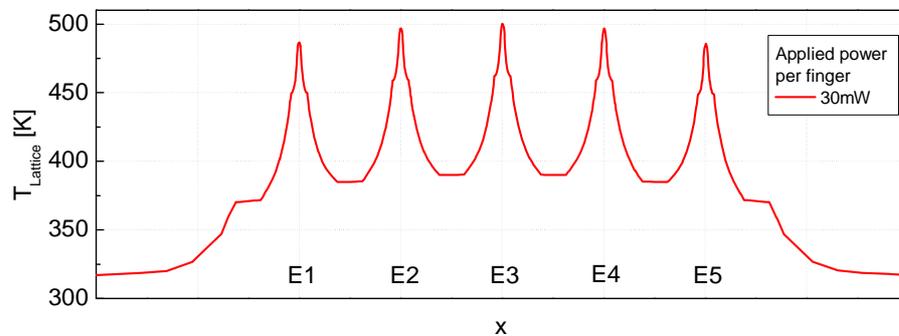
Figure 3.28: Semi-infinite Si substrate including heat sources and boundary conditions.

Different power values are applied at five rectangular heat sources (placed at the base-collector junction of each finger). Figure 3.29a shows the lattice temperature  $T_{Lattice}$  distribution inside the device for an applied power of  $30\text{mW}$ . A cross section of  $T_{Lattice}$

along the heat source in x direction is displayed in Figure 3.29b where a temperature difference between center and side fingers of  $\Delta T=15\text{K}$  is observed.



(a)



(b)

Figure 3.29: (a) Lattice temperature  $T_{Lattice}$  distribution inside the device when a power of 30mW is applied at five rectangular heat sources. (b) A cross section of  $T_{Lattice}$  along the heat source in x direction.

The steady state temperature at each BC junction is measured when several constant power values are applied at one finger. In Figure 3.30a measurements and TCAD results of the temperature increase  $\Delta T$  inside the neighboring fingers are compared when only T4 is operated as heat source. The compact model determines a slightly higher  $\Delta T$ . In Figure 3.30b, the coupling factors extracted from the measurements and TCAD simulations are in good agreement. The coupling factors extracted from TCAD for  $P_{diss}=10\text{mW}$  are shown in Table 6.

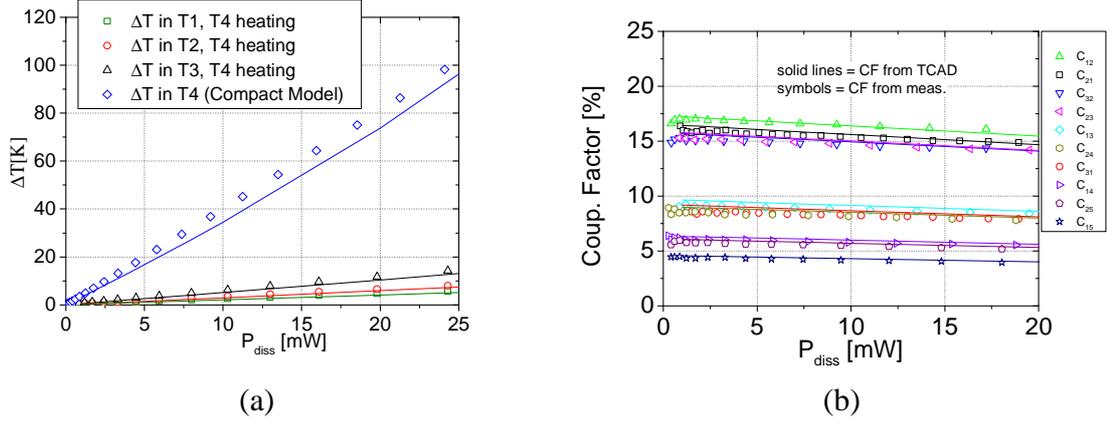


Figure 3.30: (a) Temperature increase  $\Delta T$  inside the neighboring fingers in the case when only T4 is heating; comparison of measurements (symbols) and TCAD results (solid lines).  $\Delta T$  of T4 (symbol) is calculated by the compact model. (b) Thermal coupling parameters  $C_{XY}$  plotted versus the dissipated power of the heating transistor  $T_Y$ . Comparison between extracted parameters from measurements (symbols) and TCAD simulation (solid lines).

Heating finger	Thermal coupling factors $C_{XY}$ [%]				
	T1	T2	T3	T4	T5
T1	100%	15.61%	8.66%	5.70%	4.30%
T2	16.39%	100.00%	14.93%	8.52%	5.98%
T3	9.15%	15.01%	100.00%	15.00%	9.14%
T4	5.98%	8.52%	14.93%	100%	16.39%
T5	4.30%	5.70%	8.66%	15.61%	100%

Table 6: Coupling factors for intra-device coupling extracted from 3D TCAD simulations ( $P_{diss}=10\text{mW}$ ) for a five finger HBT with drawn emitter area  $A_E=[0.18 \times 5]\mu\text{m}^2$ .

### 3.3.2.5 Thermal coupling model

In this section, the thermal model from [116] is applied which allows substrate thermal coupling between the active fingers/transistors of the test structures to be accurately represented in a circuit simulation environment. The thermal equivalent circuit contains resistors and voltage-controlled voltage sources. The derivation of the coupling coefficients has been described in Paragraph 3.3.2.3.

A linearized thermal coupling model in the case of two transistors (shown in Figure 3.31) is defined as

$$\Delta T_1 = \Delta T_{11} + c_{12}\Delta T_{22} = R_{th\_11}P_1 + c_{12}R_{th\_22}P_2 \quad (3.32)$$

$$\Delta T_2 = c_{21}\Delta T_{11} + \Delta T_{22} = c_{21}R_{th\_11}P_1 + R_{th\_22}P_2$$

where  $\Delta T_1$  and  $\Delta T_2$  are the temperature increases in the two transistors,  $R_{th\_11}$  and  $R_{th\_22}$  are the self-heating thermal resistances,  $c_{12}$  and  $c_{21}$  are the mutual thermal coupling factors and  $P_1$  and  $P_2$  are the dissipated powers. As shown in the previous section, thermal coupling factors are not constant with temperature since the silicon substrate and the dielectric materials have temperature dependent thermal conductivities. Thus, the linearity principle of (3.32) is only valid for small signal excitations. However, in our case this is sufficient since the coupling factors vary little with  $P_{diss}$  (see Figure 3.25).

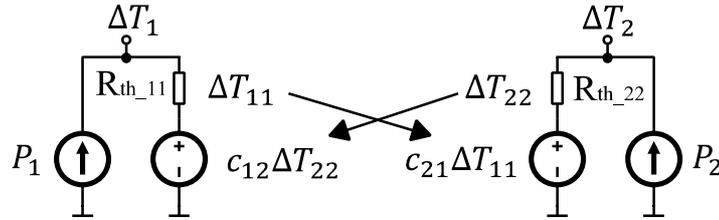


Figure 3.31: Extended thermal network for self-heating and thermal coupling for two sources.

A netlist-based method calculating the thermal coupling between devices in an electrical simulator is very suitable for circuit designers. Therefore, the thermal nodes of five lumped HICUM transistor models are connected to a distributed thermal network proposed by [116]. The method retains the thermal resistance of each device. The thermal coupling terms are implemented using voltage controlled voltage sources (see Figure 3.31). The thermal interaction can be exactly represented by the extracted coupling coefficients of the controlled sources. This simple approach makes the construction of the thermal coupling network very straightforward.

In Figure 3.32, output characteristics of the MFT test structure for a constant  $V_{BE}=[0.85, 0.9, 0.95]V$  are compared to circuit simulations using the extracted distributed thermal network (coupling parameters in Table 2). In Figure 3.32a, emitter 1, 2 and 3 operates solely, which means that the differences are mainly caused by the difference in thermal resistance of each finger. The parallel operation of 2, 3 and 5 fingers is displayed in Figure 3.32b, c and d, respectively. Since the device structure is symmetrical, other combinations will not provide significant information. Coupled electro-thermal simulation of the five lumped finger models is in very good agreement with all measured configurations.

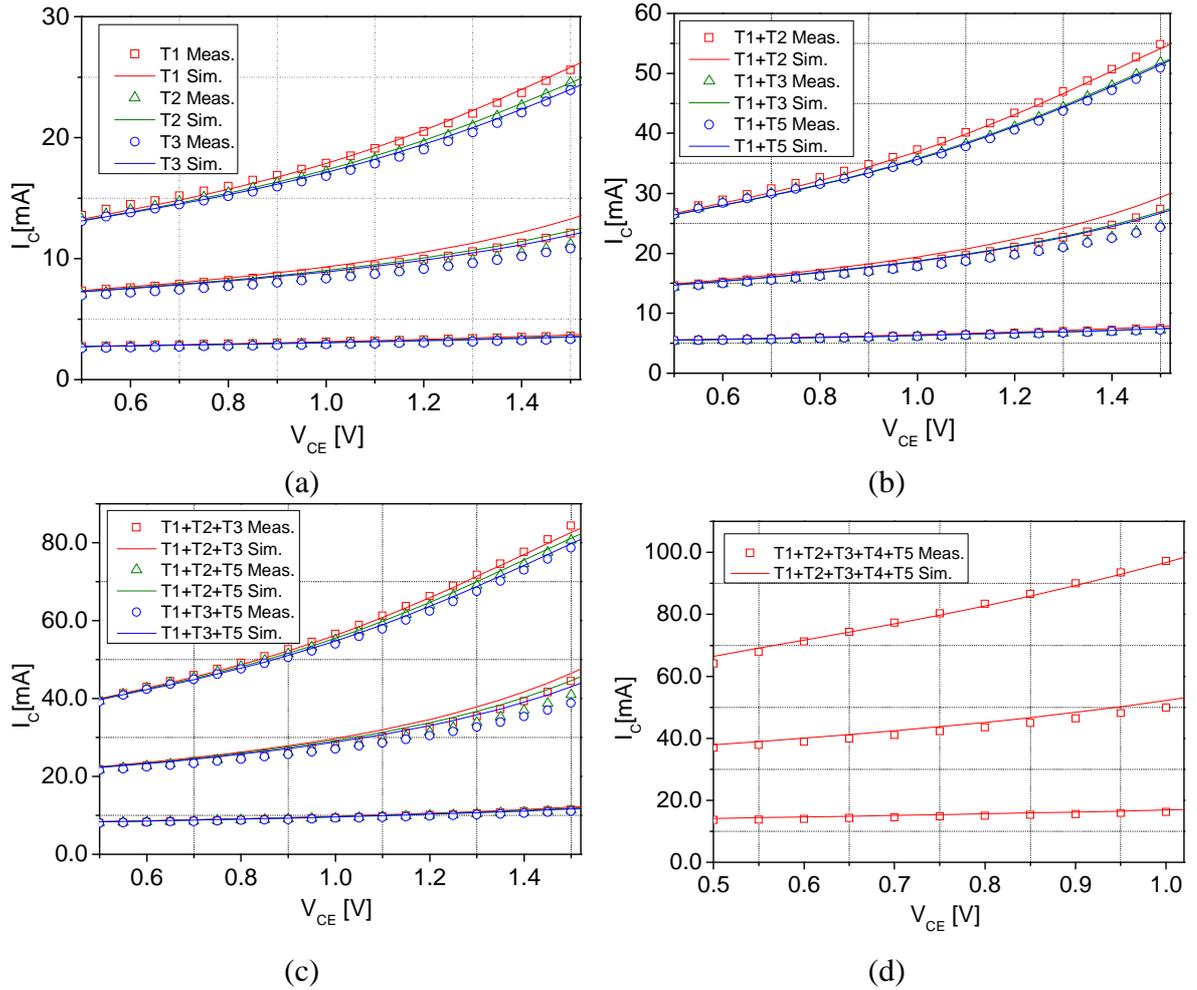


Figure 3.32: Output characteristics of a multi-emitter HBT with a drawn emitter finger area  $A_E = 0.27 \times 5 \mu\text{m}^2$ . The measurements and circuit simulations using a distributed network were carried out for a  $V_{BE} = [0.85, 0.9, 0.95]\text{V}$  and different finger combinations where (a) 1 emitter (b) 2 emitters (c) 3 emitters (d) 5 emitters operate in parallel.

In addition, measurements of the MFT and MTA embedded in standard transistor modeling structures (see also Paragraph 4.3.1) were carried out. Within these structures the transistors are biased through common base and common collector and the emitters are on ground. Hence, MFT and MTA can be measured normally with two GSG probes. Measured results of the MFT and the MTA are displayed in Figure 3.33a and Figure 3.33b, respectively. As expected, measured collector currents of the MFT test structure (Figure 3.32d) and of the MFT standard modeling structure (Figure 3.33a) are very close. Circuit simulations (solid lines) using the coupling network are compared to measured output characteristics. Coupling factors of the MTA can be found in Table 3. Furthermore, simulations are added without thermal coupling. Difference in  $I_C$  when thermal coupling is deactivated, is almost negligible in the MTA, whereas it is significant in the MFT.

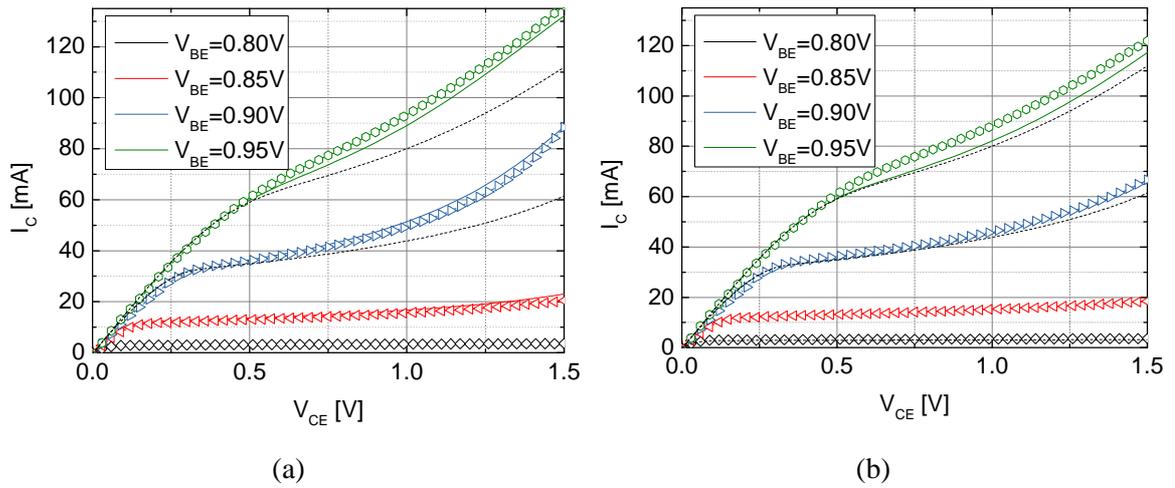


Figure 3.33: Measured (symbols) and simulated (lines) output characteristics for  $V_{BE}=[0.8, 0.85, 0.9, 0.95]$ V of (a) the MFT and (b) the MTA (distance between deep trenches  $D=3\mu\text{m}$ ) with a drawn emitter area  $A_E=0.18\times 5\mu\text{m}^2$ . Simulations with thermal coupling (solid lines) and without thermal coupling (dashed lines) are shown.

### 3.4 Conclusions

Firstly, the self-heating effect in SiGe HBTs was evaluated with low frequency measurements and pulsed measurements. A generalized methodology was presented for frequency domain thermal impedance extraction using small signal two port measurements in the frequency range below thermal cut-off. Moreover, an advanced pulsed I-V and pulsed RF measurement system has been presented which allows adapting the duty cycle, the pulse width and the synchronization of DC pulse and RF pulse. Collector bias voltage as well as duty cycle was optimized and validated by pulsed simulation. Self-heating inside the device was significantly decreased using small pulse widths.

Secondly, the standard thermal network was replaced by higher order networks in order to model accurately dynamic self-heating and thermal coupling between neighboring devices. The better accuracy of the recursive network was verified comparing pulsed compact model simulation with pulsed measurements. Furthermore, the effect of thermal inter- and intra-device coupling for trench isolated HBTs was measured and modeled. Thermal coupling between single devices (inter-device) and between the emitter stripes of a multi-finger transistor (intra-device) was measured using novel test structures that were specially designed and fabricated. Thermal coupling factors were extracted from these measurements as well as from 3D thermal simulations and found to be in good agreement.

Inter-device coupling between transistors having a distance of  $1.5\mu\text{m}$  between the deep trench walls was found to be less than 5% due to better thermal isolation. The

thermal coupling effect, as expected, is further reduced with wider spacing between the transistors. In contrast, intra-device coupling is more pronounced. A maximum coupling of 17% between neighboring fingers was measured. Due to restrictions by the design rules of the PDK it was not possible to study a wider spacing of the emitter fingers.

The two presented models are easy to use for circuit designers and predict accurately thermal effects in high speed SiGe HBTs. Regarding the simulation of multi-finger transistors, a similar accuracy could be probably also achieved using a lumped model with a single fitted thermal resistance. However, this would totally ignore the non-homogeneous temperature distribution across the multi-finger device. The proposed thermal network would give the designer access to thermal nodes of each finger. The resulting benefits for the designer are further discussed in Chapter 4.

## Chapter 4 Circuit-level electrothermal investigations

### 4.1 Introduction

In the Chapters 2 and 3, HBT modeling methods for DC and small-signal excitation have been discussed and analyzed. However, transistor compact models should not only be verified on device-level. Circuit-level investigations can, for example, (i) verify the device operation under large signal regime, (ii) study the electrical and thermal interaction between devices in close proximity or (iii) evaluate the sensitivity of the circuit performance to device characteristics. An example is shown in Appendix A.5 where the impact of process variations on the FoMs of a 94GHz low noise amplifier (LNA) was investigated.

Due to an increased density of transistors on a given chip thermal effects can significantly affect the performance (reliability, propagation delays, power dissipation) of the overall circuit [117], [118]. Hence, a more accurate thermal analysis is required to study the thermal issues at the device and circuit level. The design of analog circuits requires accurate device models for computing the impact of the junction temperature on device characteristics. For analog/RF designers it would be advantageous to include thermal analysis in the state of the art CAD based design and optimization process. Thermal analysis should include, e.g. the impact of the distance between devices on the gain, stability factor, input and output matching, etc. This would allow direct computation of the resulting circuit performance, hence providing an initial valid solution for circuit designers.

In this chapter, the device's large signal dynamical behavior is studied by means of two circuits. Firstly, several realizations of a large scale current mode logic (CML) ring oscillator (RO) with 218 transistors are presented. The circuit architecture as well as optimization steps are explained. The accuracy of circuit simulations is improved considering the measured circuit temperature. Electrothermal simulations of the whole circuit are carried out using the distributed thermal coupling compact model extracted in the previous chapter. Secondly, two transistor arrays are operated as 60GHz power amplifiers. Harmonic balance simulations are compared with 60GHz RF power measurements using load pull variation. Electrical and thermal performance between multi-finger transistor and multi-transistor are compared. Lumped and distributed transistor models are verified under large signal conditions. The nonlinear behavior of microwave devices can only be investigated at large-signal operation. This is very important to predict accurately the performance of microwave nonlinear circuits such as power amplifiers, mixers and oscillators.

## 4.2 Ring oscillator

In order to benchmark the technology performance for high-speed circuit operation, the transit frequency  $f_T$ , the maximum oscillation frequency  $f_{\max}$  and the RO gate delay  $\tau_{\text{gate}}$  are powerful figures-of-merit. Evaluating a device technology using ring oscillators is a simple and widely used method. There have been a number of demonstrations of ring oscillator gate delays less than 5ps [119]–[123]. In comparison to figures of merit like  $f_T$  or  $f_{\max}$ , the gate delay  $\tau_{\text{gate}}$  seems more relevant since it evaluates a technology at circuit level, including the specific back-end of line (BEOL) wiring. Indeed, interconnect parasitics can have a significant impact on high-speed switching operations [124].

This section examines different RO circuits fabricated in B4T and B5T technology. The proposed CML ROs comprise 53 inverter stages with a single ended voltage swing of 200mV. These specifications were agreed upon by DOTFIVE partners (IHP, Infineon) to allow a direct comparison between the different technologies. The circuit performance as well as the circuit temperature is studied. Through an optimization of process and circuit layout,  $\tau_{\text{gate}}$  is reduced from 2.72ps [122] to 1.65ps [51] which beats the lowest reported value of 1.9ps [123] (the RO architecture of this work is similar to Ref. [123]).

### 4.2.1 Working principle and specifications

An RO consists of a number of inverter stages where the output of the last stage is fed back to the input of the first stage. Each (inverting) stage can be modeled by a single-pole transfer function in the frequency domain

$$H(j\omega) = \frac{-A_v}{1 + j\omega/\omega_0} \quad (4.1)$$

where  $A_v$  is the voltage gain and  $\omega_0 = 2\pi f$  is the frequency that the inverter stage will attenuate to half its original power. The loop gain of the RO  $L(j\omega)$  results to [125]

$$L(j\omega) = (-1)^{n+1} \left[ \frac{-A_v}{1 + j\omega/\omega_0} \right]^n \quad (4.2)$$

where  $n$  is the number of stages. The term  $(-1)^{n+1}$  must be positive to ensure a negative feedback. Hence, an odd number of inverting stages must be used. However, an even number of stages can also be used if the inverting stages have a differential output and the output nodes of one stage are inverted. The phase margin  $m_\phi$  of an  $n$ -stage RO is expressed as [126]

$$m_\phi \cong 180 - n \cdot \arctan(A_v) \quad (4.3)$$

Hence, the number of stages  $n$  must be

$$n > \frac{180}{\arctan(A_V)}. \quad (4.4)$$

to guarantee a negative phase margin which allows oscillation.

The signal must go through each of the  $N$  inverter stages twice to provide a full period ( $f_{osc}$ ). Thus, the propagation delay  $\tau_{gate}$  can be calculated with

$$\tau_{gate} = \frac{1}{2 \cdot N \cdot f_{osc}}. \quad (4.5)$$

A simplified CML model is presented in [127].  $\tau_{gate}$  can be approximated as a function of device and circuit parameters

$$\tau_{gate} = 0.69 \left( \frac{r_E + r_B}{1 + g_m r_E} C_{BE} + r_B C_{BCi} \left( 1 + \frac{g_m (r_C + R_L)}{1 + g_m r_E} \right) + (r_C + R_L) (C_{BCi} + C_{BCx} + C_{CS}) + R_L C_L \right) \quad (4.6)$$

where  $r_B$ ,  $r_C$  and  $r_E$  are base, collector and emitter resistances,  $C_{BE}$  is the total BE capacitance,  $C_{BCi}$  and  $C_{BCx}$  are intrinsic and extrinsic base-collector capacitances and  $C_{CS}$  is the substrate capacitance.

## 4.2.2 First RO circuit

### 4.2.2.1 Circuit description

A sketch of the RO including 53 inverter stages is shown in Figure 4.1a and the schematic diagram of one CML stage is displayed in Figure 4.1b. The tail current of each stage is controlled via a simple current mirror. The current flowing through each stage is defined by the current tuning terminal  $V_{POL}$  and the resistors  $R_E$  and  $R_M$ . An output buffer (emitter follower) provides the voltage swing without voltage amplification. The RO layout should monitor the performance of STMicroelectronics B3T (B3T RO measurements see in Appendix A.3) and B4T process (see Paragraph 2.2). Therefore, the CBEB HBT with drawn emitter length  $L_E=5\mu\text{m}$  was chosen to be the main transistor since it has a high  $f_T$  and  $f_{max}$  in combination with an accurate compact model (information provided from STMicroelectronics modeling team). In this work, a scalable model library of B4T transistors is used that was developed by XMOD within the DOTFIVE project. The transistor compact model (CBEB HBT with drawn  $A_E=0.23 \times 5\mu\text{m}^2$ ) was verified with DC and RF measurements carried out on a transistor modeling structures fabricated next to the RO. Measurements and simulations are presented in the Appendix A.1.

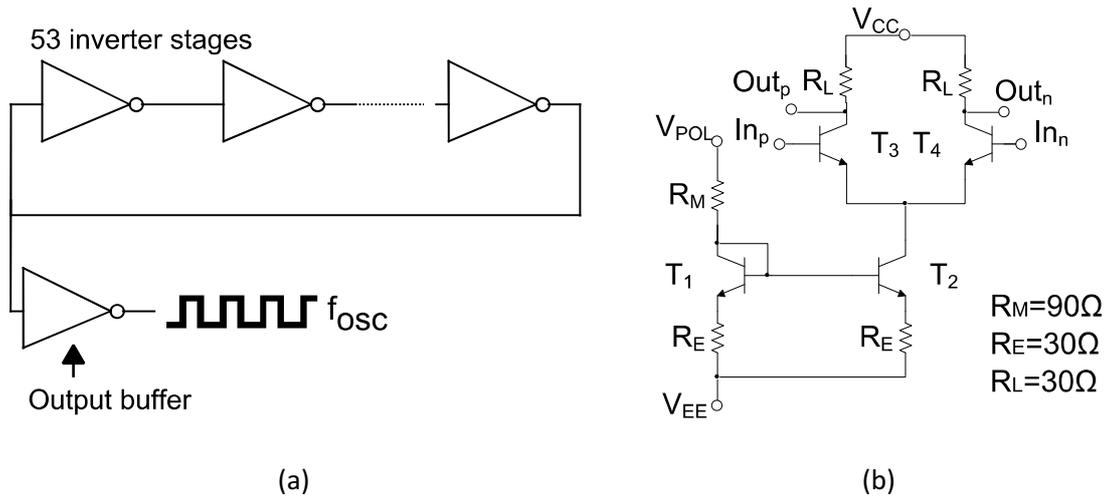


Figure 4.1: (a) Sketch of the ring oscillator with 53 CML inverter stages. (b) Schematic view of one CML inverter stage.

The layout of the RO and a micrograph of the fabricated circuit are shown in Figure 4.2. The RO is biased through five DC Pads situated in the middle of the ring. The voltage source  $V_{POL}$  is proportional to the current of the current mirror. Through variation of  $V_{POL}$  and  $V_{CC}$ ,  $\tau_{gate}$  can be measured as a function of current per gate  $I_{gate}$ . The output signal is taken from the RF signal port. The RF pads are designed for RF probes with a  $100\mu\text{m}$  pitch and ground-signal-ground (GSG) configuration.

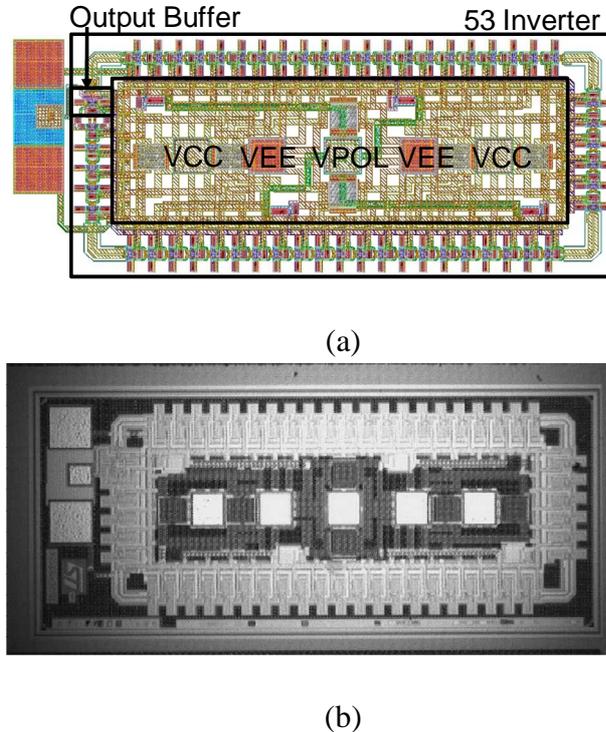


Figure 4.2: (a) The layout of the RO and (b) a micrograph of the fabricated circuit.

The 3D sketch of one inverter stage including the inter-stage wiring is displayed in Figure 4.3. The inverter stages are connected via metal 6 (M6). Parasitic resistances and

capacitances between all inverter stages have been extracted through the 3D fast field solver StarRC (Synopsys).

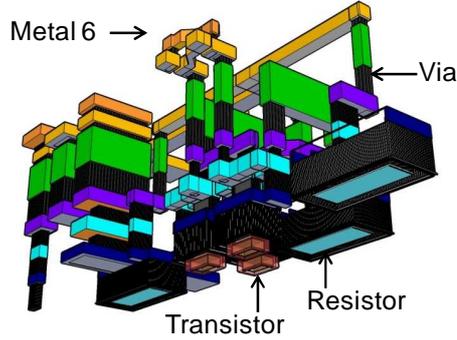


Figure 4.3: 3D sketch of one inverter stage including back-end wiring.

#### 4.2.2.2 Calculation of circuit environment temperature

In a circuit, the most part of the heat is generated from the power dissipated by the devices embedded in the substrate. In general, compact models consider the temperature rise caused by self-heating using a thermal impedance network. For a single transistor the ambient temperature can be considered to be approximately room temperature. This is not valid in our case, as we have a highly integrated circuit with hundreds of active and passive devices. The real operating temperature in the local circuit area results from mutual heating of all active and passive components.

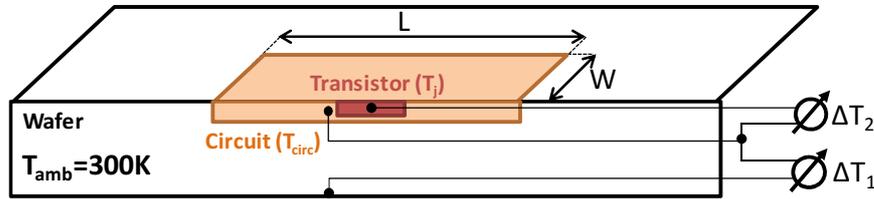


Figure 4.4: Device junction temperature  $T$  results from the local circuit temperature  $T_{\text{circ}}$  and the ambient temperature  $T_{\text{amb}}$ .

As shown in Figure 4.4, in a circuit the self-heating-induced temperature rise inside a device  $\Delta T$  can be described as

$$\Delta T_j = \Delta T_1 + \Delta T_2 \quad (4.7)$$

where  $\Delta T_1$  is the temperature difference between the chuck temperature  $T_{\text{amb}}$  and the average temperature in the local circuit area  $T_{\text{circ}}$  ( $\Delta T_1 = T_{\text{circ}} - T_{\text{amb}}$ ) and  $\Delta T_2$  is the temperature difference between  $T_{\text{circ}}$  and the device temperature  $T_j$  ( $\Delta T_2 = T_j - T_{\text{circ}}$ ).  $\Delta T_1$  is caused by mutual heating of all active and passive components within the circuit. In order to calculate  $T_{\text{circ}}$  that is given by

$$T_{\text{circ}} = T_{\text{amb}} + R_{\text{th,circ}} \frac{P_{\text{diss}}}{A_{\text{circ}}} \quad (4.8)$$

the RO circuit is assumed as a rectangular heat source at the top with an adiabatic surface. Integrating the temperature rise of a thermal point source over the whole source area yields the total temperature rise [128]

$$\Delta T = \frac{1}{2\pi\kappa} \frac{P_{\text{diss}}}{LW} \left( \frac{1}{L} \log \left( \frac{L + \sqrt{W^2 + L^2}}{-L + \sqrt{W^2 + L^2}} \right) \right) + \frac{1}{W} \log \left( \frac{W + \sqrt{W^2 + L^2}}{-W + \sqrt{W^2 + L^2}} \right). \quad (4.9)$$

where  $\kappa$  is the thermal conductivity of silicon,  $P_{\text{diss}}$  dissipated power and  $W$  and  $L$  are effective width and length of the circuit area. It is difficult to determine the effective area  $A_{\text{circ}}$  of the circuit since it is very dependent on the layout. In this case, the effective area is defined by the area of all inverter stages (the center region including the pads is not taken into account). The lateral dimension of the substrate as well as the substrate thickness is considered to be infinite regarding the circuit dimension. For the latter this is not the case, thus, the calculated value is only intended to be a rough approximation. For example, a collector current per gate  $I_{\text{gate}}$  of 11.3mA resulting in a circuit power consumption  $P_{\text{circ}}$  of 1860mW and a  $\Delta T_1$  of about 23K.  $\Delta T_2$  is then determined through the thermal resistance  $R_{\text{th}}$  of the transistor model.

The presented approach is rather simple since it considers a homogeneous temperature distribution across the circuit. Therefore, it will be compared with on-wafer temperature measurements in a next step. However, adapting the simulation temperature (local circuit temperature) as a function of the bias conditions (power consumption of the whole circuit) would be a convenient way to consider mutual heating of all passive and active devices without increasing the computation time.

#### 4.2.2.3 Simulation versus measurement

Figure 4.5 exhibits a wafer map of measured gate delays. An average gate delay of 2.76ps was measured with a maximum relative deviation over the wafer of only 2% demonstrating good homogeneity. In Figure 4.6a, measurement and simulation results for the gate delay  $\tau_{\text{gate}}$  are shown.  $\tau_{\text{gate}}$  decreases with higher  $I_{\text{gate}}$  at low power. After  $\tau_{\text{gate}}$  has reached its minimum it increases as  $I_{\text{gate}}$  further increases. This behavior corresponds with the transit frequency  $f_T$  versus collector current  $I_C$  of the main transistor in Figure 4.6b. The minimum gate delay  $\tau_{\text{gate,min}}$  and peak  $f_T$  are at an  $I_{\text{gate}}$  and an  $I_C$  of around 7mA, respectively. Pre-layout and post-layout simulation considering the parasitics of all inverter stages is displayed. The underestimated  $\tau_{\text{gate}}$  for the post-layout simulation (PLS) is probably the result of additional parasitics like pads or cables that have not been taken into account. Post layout extraction of the RC network yields to a  $\tau_{\text{gate}}$  reduction of around 25%. The significant decrease of  $\tau_{\text{gate}}$  at high power dissipation could not be reproduced by simulation with a constant temperature of 300K. Taking into account the circuit temperature  $T_{\text{circ}}$  due to mutual heating (as described in previous paragraph) gives much more realistic results. However, at high power dissipation  $\tau_{\text{gate}}$  is

still underestimated which is probably due to the simplifications made for calculating the circuit temperature.

		2,73		2,76		
	2,72	2,77	2,79		2,77	
2,73	2,76	2,79		2,8		2,77
2,73	2,77		2,77		2,77	
2,72	2,76	2,77		2,83		2,83
2,73	2,77		2,83		2,8	
		2,8		2,82		
			2,8			

Figure 4.5: Measured wafer map of the gate delay  $\tau_{\text{gate}}$  for an  $I_{\text{gate}}$  of 7mA.

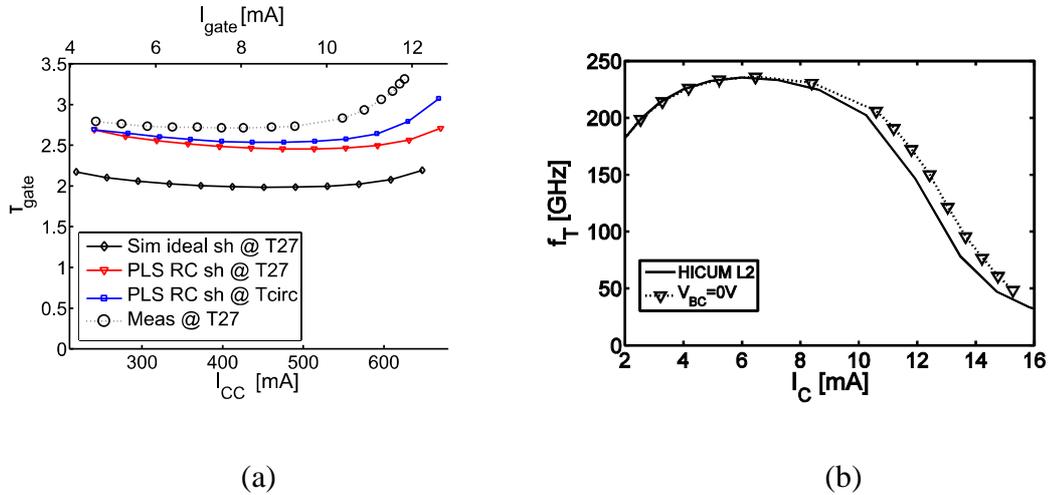


Figure 4.6: (a) Propagation gate delay  $\tau_{\text{gate}}$  vs. total current  $I_{\text{CC}}$  and current per gate  $I_{\text{gate}}$ . Pre-layout (ideal) and post-layout (PLS) simulation results including self-heating and circuit average temperature  $T_{\text{circ}}$  are compared with measurements at an ambient temperature  $T_{\text{amb}}$  of 300K. (b) Transit frequency  $f_T$  versus collector current  $I_C$  of the main transistor (CBEBC HBT with a drawn emitter area of  $0.23 \times 5 \mu\text{m}^2$ ).

### 4.2.3 Circuit optimization

The design of millimeter-wave circuits requires accurate compact models of active and passive devices including their three-dimensional (3D) physical effects and parasitics. In order to enable circuit optimization such models need to be scalable including variations of geometry (i.e. emitter width/length), contact configuration (i.e. number of base, emitter and collector fingers) as well as number of transistors in parallel. The targeted specifications of the circuit should be fulfilled at best in the first run to avoid enormous costs of additional design cycles and decrease the time to market.

For the next technology step (B5T) the performance of the RO should be further improved. The RO circuits should be fabricated with B4T and B5T lateral dimensions on the same wafer. Hence, the impact of lithographic (lateral) scaling on the circuit performance can be analyzed. Note that, the vertical profiles correspond to the B5T pro-

cess. The major difference is a reduction in the effective emitter width from  $0.13\mu\text{m}$  to  $0.12\mu\text{m}$ . A new B4T and B5T scalable model library extrapolated from the previous process node B4T was provided by STMicroelectronics to enable circuit design. The optimum transistor where the gate delay reaches its minimum  $\tau_{\text{gate,min}}$  was determined by means of transient simulations. For several emitter lengths  $l_E$ , contact configurations and number of devices in parallel (CBEBC1, CBEBC2, ...), transistor model cards were generated using a scalable model library of the B4T and B5T technology.

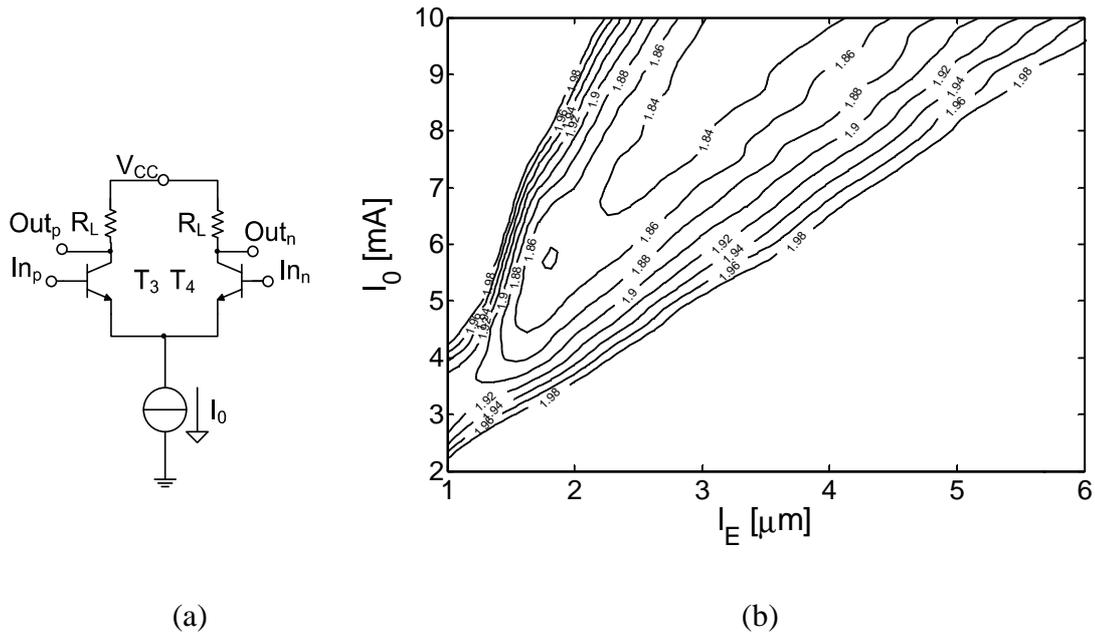


Figure 4.7: (a) Simplified inverter with an ideal current source to reduce the computing time of the circuit simulations. (b) Simulation results for a single B5T HBT with CBEBC configuration are shown as contours for constant  $\tau_{\text{gate}}$  for variation of ideal tail current  $I_0$  and emitter length  $l_E$ .

In addition to the influence of the transistor,  $\tau_{\text{gate}}$  is affected by the voltage swing and the load resistance of each inverter. A simplified inverter with an ideal current source (see Figure 4.7a) was used to reduce the computing time. The ideal tail current  $I_0$  and the load resistance  $R_L$  were varied to find  $\tau_{\text{gate,min}}$  at 200mV voltage swing. The text files including the circuit netlist were generated automatically using a script that also launches the circuit simulator in batch mode for the ca. 3500 transient simulations. The simulation results for a single B5T HBT with CBEBC configuration are shown as contours for constant  $\tau_{\text{gate}}$  in Figure 4.7b.

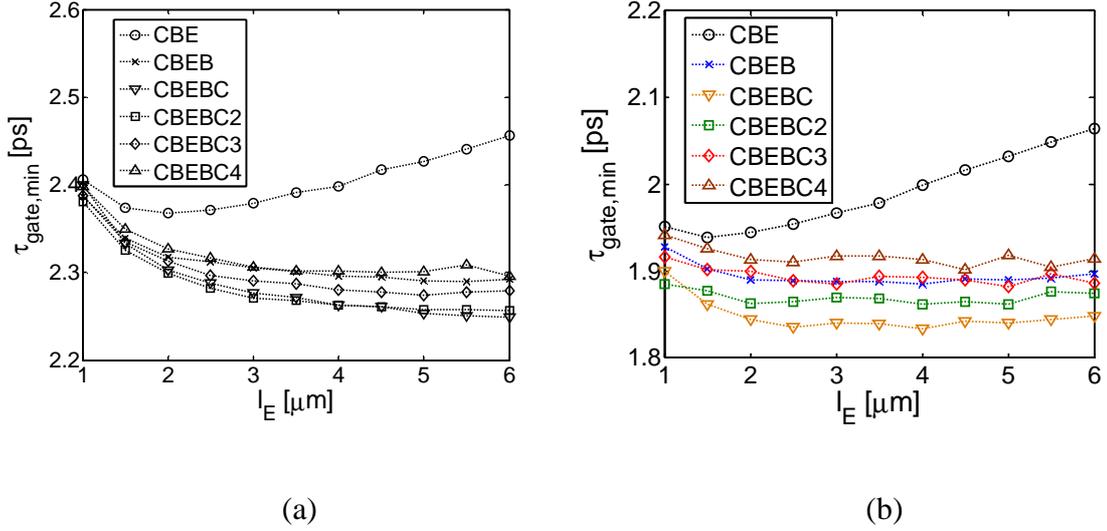


Figure 4.8: Simulated  $\tau_{\text{gate,min}}$  versus drawn emitter length  $l_E$  using devices with various contact configurations and number of transistors in parallel (CBEBBC1, CBEBBC2, ...) for (a) B4T and (b) B5T model cards.

The resulting  $\tau_{\text{gate,min}}$  versus drawn emitter length  $L_E$  for various device configurations is shown in Figure 4.8a and Figure 4.8b for B4T and B5T model cards. In this simulation, a  $\tau_{\text{gate,min}}$  of 2.25ps and 1.84ps was reached for B4T and B5T devices, respectively. Except for the CBE configuration,  $\tau_{\text{gate}}$  further decrease (B4T, B5T with  $L_E < 2.5\mu\text{m}$ ) or stay constant (B5T with  $L_E > 2.5\mu\text{m}$ ) with  $L_E$ . However, at high power levels the performance can be reduced due to thermal effects (e.g. mutual thermal coupling) that are not considered in the simulation. Depending on the layout features, MTC can be significant [113]. Therefore, CBEBBC HBT with a drawn emitter area of  $0.23 \times 5\mu\text{m}^2$  tend to be a good trade-off between device performance and dissipated power. However, in order to study the geometry dependence of  $\tau_{\text{gate}}$ , the same RO architecture was designed with several drawn emitter lengths of the main transistor: (i)  $L_{E,\text{drawn}} = 1.5\mu\text{m}$  [129], (ii)  $L_E = 3\mu\text{m}$  and (iii)  $L_E = 5\mu\text{m}$  (full test chip in Appendix A.4, see Figure A.5).

## 4.2.4 Second RO circuit

### 4.2.4.1 Circuit description

The circuit architecture is similar to the previous design. The CML ROs consist of 53 inverter stages with a single ended voltage swing of 200mV. The schematic diagram of the modified CML stage is displayed in Figure 4.9a. The tail current is controlled via a current mirror (T1, T5, T6) where the transistors T5 and T6 copy the current in order to have a more symmetric design. A low pass filter ( $R_F$ ,  $C_F$ ) was included to remove AC spurious signals from the power supply. The value of the current flowing through each

stage is defined by the voltage  $V_{pol}$  of the current mirror. The output buffer (Figure 4.9b) is designed as simple emitter follower with voltage gain of almost unity.

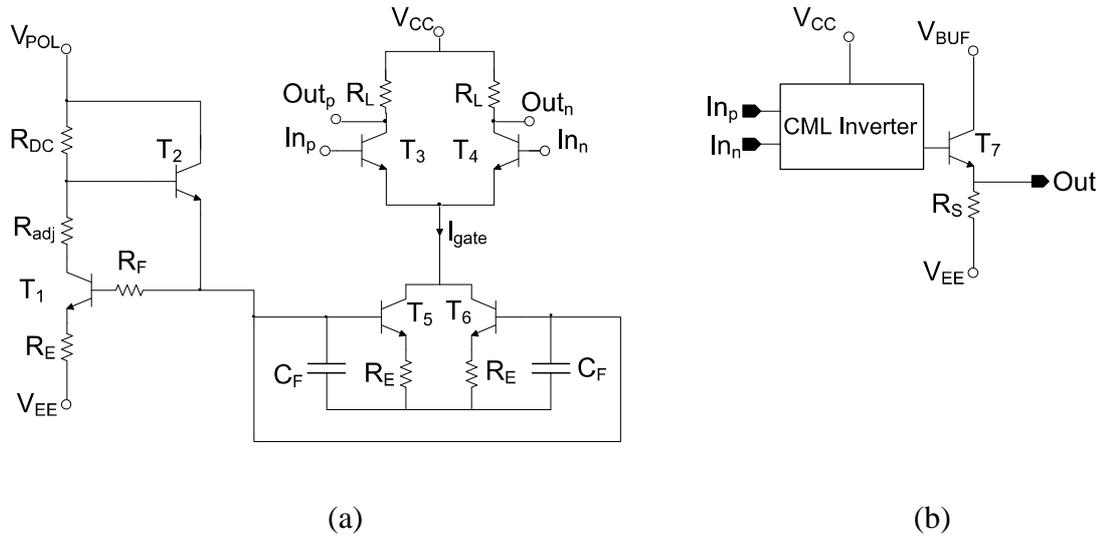


Figure 4.9: The schematic diagram for the CML inverter with the current mirror in (a) and for the output buffer in (b).

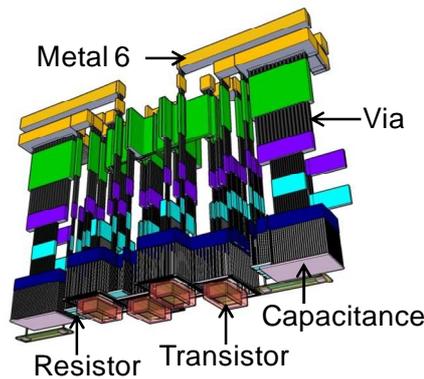


Figure 4.10: 3D sketch of modified inverter stage including back-end wiring.

The 3D sketch of the modified inverter stage is shown in Figure 4.10 including the 6 copper level metallization scheme. For the B5T process the BEOL was not changed. The new circuit layout (see Figure 4.11a) was improved in terms of parasitic interconnections. A micrograph of the fabricated circuit is displayed in Figure 4.11b. The increased number of pads reduces the voltage drop between power supply and circuit. The pads are positioned at the periphery to permit a more compact design. Comparing the 3D sketches of the new (Figure 4.10) and the previous inverter layout (Figure 4.3), transistors and passive components are placed closer together resulting in a reduced wire length.

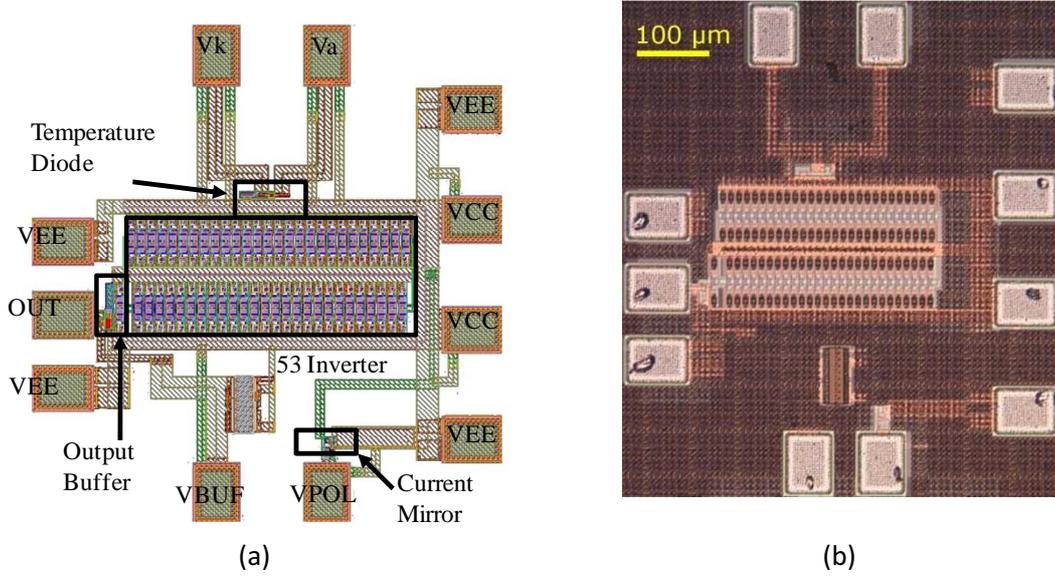


Figure 4.11: The layout view (a) of the improved RO and (b) a micrograph of the fabricated circuit.

#### 4.2.4.2 Inductive peaking

In Figure 4.12, an enlarged section of the RO layout is shown including five inverter cells (schematic diagram in Figure 4.9a). The load resistor  $R_L$  is connected to the DC power supply  $V_{CC}$  through a narrow microstrip line with a length of  $28\mu\text{m}$ , a width of  $2.4\mu\text{m}$  and a thickness of  $3\mu\text{m}$  (dimensions of the microstrip line are the same for all designed ROs). The mutual inductance of the rectangular microstrip line is derived with Equation (4.10) [130]. It is considered that the conductor length  $l$  is much greater than the width  $w$  and the thickness  $t$ . Furthermore, the magnetic permeability of the metal conductors is approximated to the permeability of free space  $\mu_0$ . Hence, the equation is solely dependent on the physical dimensions of the conductor

$$L(l, w, t) = \frac{0.42\mu_0 l}{\pi} \left( \ln \left( \frac{2l}{GMD(w, t)} \right) + \frac{GMD(w, t)}{l} - 1 \right) \quad (4.10)$$

$$GMD(w, t) = 0.2235(w + t)$$

where the term  $GMD$  (geometric mean distance) replaces the distance between the filaments within the section of the conductor. Further details on the GMD would go beyond the focus of this work, however, more detailed explanations can be found in [131]. Using (4.10) the self-inductance of the microstrip line is estimated to be around  $10\text{pH}$ . Circuit simulations have shown that this value has already a significant impact on the oscillation frequency of the RO (a detailed discussion is provided in 4.4.4.3).

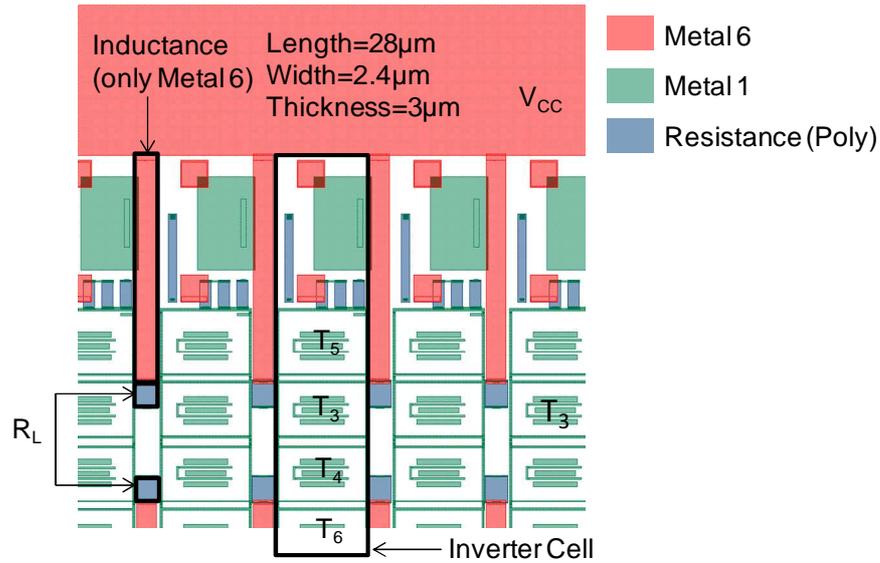


Figure 4.12: Enlarged section of the RO layout where the load resistor  $R_L$  and the DC supply are connected through a narrow microstrip line.

This effect can be explained as follows: The load resistor, the capacitances of the transistor and the wiring capacitances form an RC-lowpass. The charging/discharging of the capacitances through the load resistor adds a delay to the output voltage. This delay is partially compensated by the microstrip line acting as an inductor (inductive peaking) in series with the load resistor [132]. The inductive peaking decreases the transistor switching time.

#### 4.2.4.3 Performance results and discussion

As mentioned, the RO circuits were fabricated with B4T and B5T lateral dimensions on the same wafer. The measured propagation delays for all geometries at 200mV voltage swing are shown in Table 7 where  $\tau_{\text{gate}}$  is calculated with (4.5). For better comparison of circuit performances due to transistor geometries, in Table 7, effective dimensions are used. Note that here the effective emitter area is defined as the drawn emitter window minus the area of the inner spacers.

RO	Main Transistor		$R_L$ [ $\Omega$ ]	Voltage Swing [mV]	Average Gate Delay [ps]
	$W_{E\_eff}$ [ $\mu\text{m}$ ]	$L_{E\_eff}$ [ $\mu\text{m}$ ]			
I (B4T)	0.13	1.4	50.7	199.9	2.59
II (B4T)	0.13	2.9	29.7	199.5	2.31
III (B4T)	0.13	4.9	16.4	198.7	2.03
IV (B5T)	0.12	1.44	49.4	200.4	2.24 [129]
V (B5T)	0.12	2.94	25.4	200.8	1.91
VI (B5T)	0.12	4.94	16.1	201.4	1.65

Table 7: RO performances.

For example, an average  $\tau_{\text{gate}}$  of 2.24ps was measured in a B5T RO\_IV using transistors with  $L_{E,\text{eff}}=1.44\mu\text{m}$  [129]. This result is also confirmed in [45]. Due to horizontal scaling of the effective emitter width (from  $0.13\mu\text{m}$  to  $0.12\mu\text{m}$ ) we have an improvement of 13.5%, 17.3% and 18.7% in  $\tau_{\text{gate}}$  for the drawn emitter lengths  $1.5\mu\text{m}$ ,  $3\mu\text{m}$  and  $5\mu\text{m}$ , respectively. The rather high decrease of 25% in  $\tau_{\text{gate}}$  between the previous RO layout [122] ( $\tau_{\text{gate}}=2.7\text{ps}$ , fabricated in B4T technology) and RO\_III ( $\tau_{\text{gate}}=2.03\text{ps}$ , see Table 7) can be explained in the following way: (i) the vertical profile between B4T and B5T is different. This is well illustrated in Figure 4.13a where it is obvious that  $f_{T,\text{B5T}} \gg f_{T,\text{B4T}}$ . Only a small part of this increase comes from the emitter width reduction. Furthermore, the emitter width reduction between B4T and B5T is not solely due to a change in the layout, the narrower inside spacers in B5T also have a large impact. The latter also helps reducing the external base resistance  $R_{\text{BX}}$ . (ii) The circuit layout was optimized (previous layout in Figure 4.2a and optimized layout Figure 4.11a) and an on-chip microstrip line was added in series with the load resistor (inductive peaking see previous paragraph).

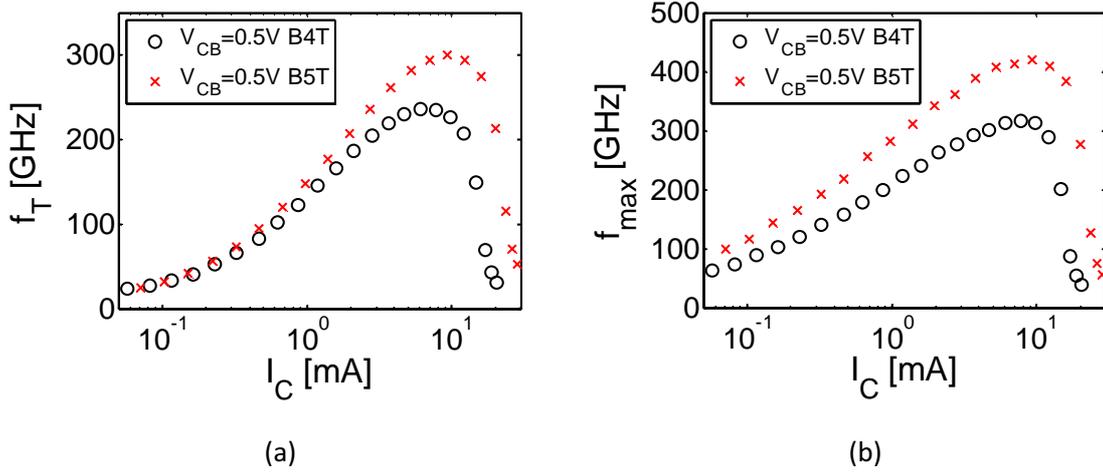


Figure 4.13: Measurement of (a) transit frequency  $f_T$  and (b) maximum oscillation frequency  $f_{\text{max}}$  vs. collector current  $I_C$  for B4T and B5T CBEBT HBT with a drawn emitter area of  $A_{E,\text{B4T}}=0.23 \times 5\mu\text{m}^2$  and  $A_{E,\text{B5T}}=0.18 \times 5\mu\text{m}^2$ .

Comparing only the B5T ROs, it can be observed that there is a rather large variation of the gate delay for different emitter lengths. The fact that  $\tau_{\text{gate}}$  significantly decreases for longer emitter lengths cannot be explained solely by the higher device performance ( $f_T$  and  $f_{\text{max}}$  shown in Figure 4.13a and b) and the related capacitor and resistance values given in Table 8. At higher transfer currents the value of the load resistance  $R_L$  which is needed to achieve the same voltage swing is smaller (see Table 8). In our case, the smaller load resistance associated with longer emitter and higher current causes the effect of inductive peaking to be more pronounced. Circuit simulations have shown that adding an inductor of 10pH (between  $V_{\text{CC}}$  and  $R_L$ ) gives an improvement in  $\tau_{\text{gate}}$  of 11.2% for RO\_IV, 12.6% for RO\_V and 23.3% for RO\_VI (see Table 9).

$A_{E\_eff}$	$0.12 \times 1.44 \mu\text{m}^2$	$0.12 \times 2.94 \mu\text{m}^2$	$0.12 \times 4.94 \mu\text{m}^2$
$C_{BE0}$	2.4fF	5.3fF	9.2fF
$C_{BC0}$	2.2fF	4.2fF	6.7fF
$R_{Bi0}$	$16 \Omega$	$7 \Omega$	$4 \Omega$
$R_{BX}$	$90 \Omega$	$42 \Omega$	$25 \Omega$
$R_E$	$18.5 \Omega$	$7.5 \Omega$	$4.2 \Omega$
$R_{CX}$	$33.9 \Omega$	$17.6 \Omega$	$10.8 \Omega$
peak $f_T$ (@ $V_{CB}=0.5\text{V}$ )	302GHz	304GHz	311GHz
peak $f_{max}$ (@ $V_{CB}=0.5\text{V}$ )	354GHz	362GHz	398GHz

Table 8: B5T transistor parameters.

$A_{E\_eff}$	$0.12 \times 1.44 \mu\text{m}^2$	$0.12 \times 3.94 \mu\text{m}^2$	$0.12 \times 4.94 \mu\text{m}^2$
$R_{Load}$	$55 \Omega$	$29 \Omega$	$17 \Omega$
$L_{Series}$	10pH	10pH	10pH
Increase in performance due to inductive peaking	11.2%	12.6%	23.3%

Table 9: Increase in performance due to inductive peaking.

In Figure 4.14a, the measured  $\tau_{gate}$  of the previous RO circuit [122], the recent record from IHP [123] and the optimized B5T RO\_VI design are plotted versus the voltage swing. The output spectrum of the latter circuit is shown in Figure 4.14b where the fundamental oscillation frequency of 5.93GHz corresponds to a gate delay of 1.58ps. In order to show the consistency of the proposed results, a wafer map of  $\tau_{gate}$  measured at same bias conditions was generated in Figure 4.15. An average gate delay of 1.65ps was achieved with a standard deviation of 4% over the wafer demonstrating good homogeneity of the process. 1.54ps at an oscillation with an amplitude of 200mV is the lowest gate delay measured in this study.

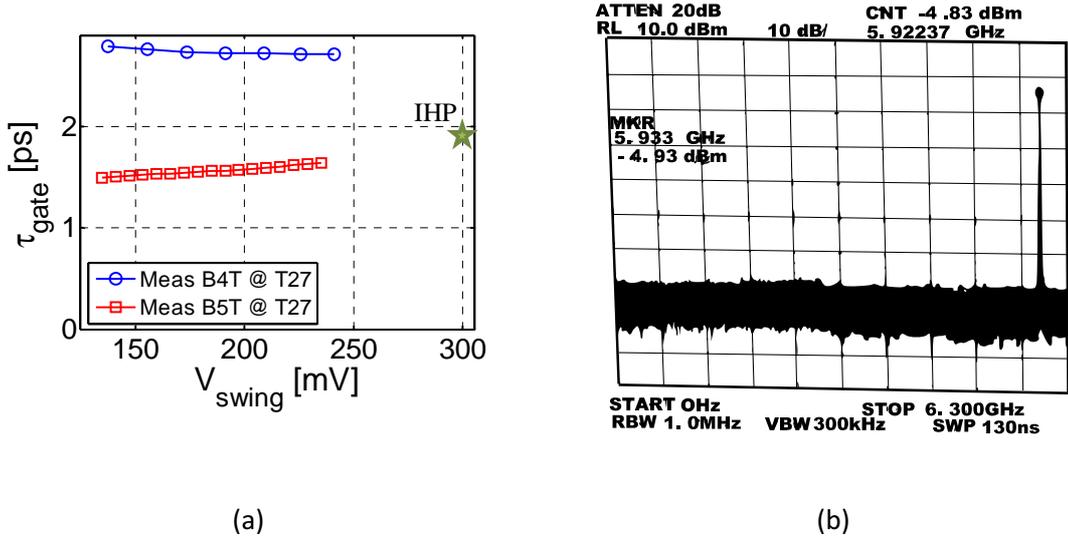


Figure 4.14: (a) Measured  $\tau_{\text{gate}}$  of the previous RO design (B4T), the former record value from IHP [123] and the optimized B5T RO\_VI design are plotted vs. single ended voltage swing for a CBEB C HBT with a drawn emitter area of  $A_{E,B4T}=0.23 \times 5 \mu\text{m}^2$  and  $A_{E,B5T}=0.18 \times 5 \mu\text{m}^2$ . (b) The output spectrum of B5T RO\_VI with the fundamental oscillation frequency of 5.93GHz, corresponding to a gate delay of 1.58ps and a fundamental output power  $P_{\text{out}}$  of -4.83dBm.

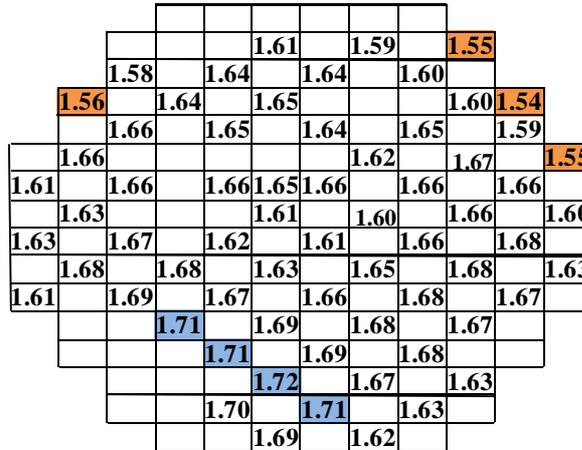


Figure 4.15: Measured wafer map of the gate delay  $\tau_{\text{gate}}$  in ps for a constant current per gate  $I_{\text{gate}}=12.5\text{mA}$  (dies without number were not measured).

#### 4.2.4.4 Circuit temperature

The dynamic surface temperature of an IC is a projection of the circuit’s behavior. The temperature is a relevant physical variable for the design and the characterization of devices and circuits [133]. An overview of the capabilities and different architectures for integrated temperature sensors was provided in [134]. BJT-based, MOSFET-based, ring oscillator-based and propagation delay-based temperature sensors were compared with respect to power consumption, temperature range, accuracy, resolution, etc. If power consumption is not a constraint, the most suitable solution was found to be the

BJT-based approach achieving the highest temperature range ( $-50^{\circ}\text{C}$  to  $120^{\circ}\text{C}$ ) together with a good resolution ( $\pm 0.05^{\circ}\text{C}$ ). In this design, a temperature sensor (SiGe HBT) was placed near (at  $15\mu\text{m}$  distance) to the circuit (see Figure 4.16) to measure the temperature rise in the local circuit area and to consider it later in circuit simulations.

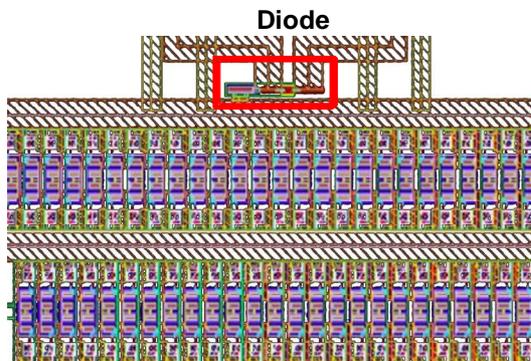


Figure 4.16: Distance between diode and circuit is around  $15\mu\text{m}$ .

The schematic view of the temperature diode is shown in Figure 4.17a. The sensor consists of a CBEBBC HBT with drawn emitter window  $A_E=0.84\times 5\mu\text{m}^2$ . Through connection of base and collector node, the transistor operates as a simple diode. At the terminal  $V_F$ , a current is forced through the resistor  $R$  while the diode voltage  $V_S$  is measured. Since the sensor has to be calibrated  $V_S$  was measured from  $10^{\circ}\text{C}$  to  $100^{\circ}\text{C}$  for different forced currents  $I_D$  (see Figure 4.17b).  $I_D$  was chosen to be  $100\mu\text{A}$  where self-heating is rather not significant and a sufficient measurement accuracy is achieved. Thermal sensitivity  $K$  is determined with (3.28).

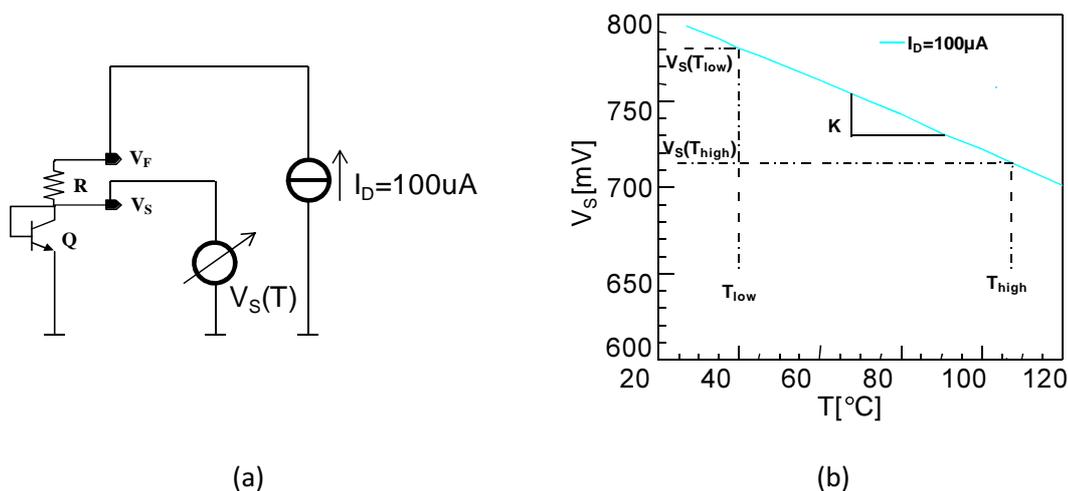


Figure 4.17: (a) Schematic view of the temperature diode; and (b) calculation of temperature coefficient.

Figure 4.18 shows a block-diagram of the experimental set-up for automatized RO characterization. The RO circuit is biased with three DC power suppliers (Agilent E3631A) through DC probes contacted to six DC pads ( $V_{BUF}$ ,  $V_{POL}$ ,  $2\times V_{CC}$ ,  $2\times GND$ ).

$V_{CC}$ ,  $V_{POL}$ ,  $V_{BUF}$  are the supply voltages for the inverter stages, the current mirror and the output buffer, respectively. The output signal is taken from the RF signal port and measured with the spectrum analyzer (HP8563E). The temperature diode is biased and measured with the DC analyzer HP4155A. A custom-made software program controls all instruments over GPIB. The program allows the variation of bias conditions ( $V_{CC}$ ,  $V_{POL}$  and  $V_{BUF}$ ) and at the same time the measurement of the oscillation frequency  $f_{osc}$  and the circuit temperature  $T_{circ}$ .

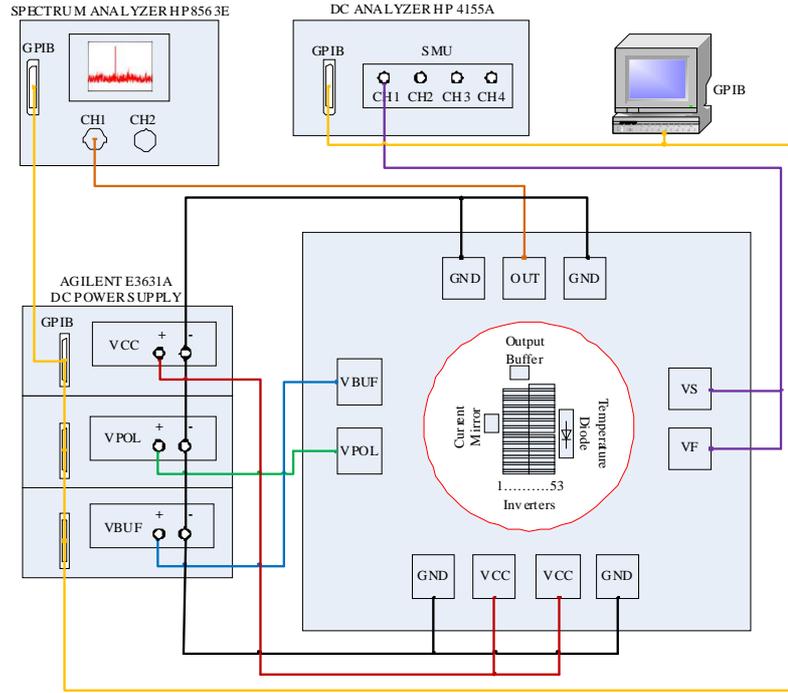


Figure 4.18: Experimental set up for automatized RO characterization in combination with circuit temperature measurement.

#### 4.2.4.5 Circuit simulations considering the circuit temperature

Here, circuit measurements of the B5T RO\_IV using transistors with drawn  $L_E=1.5\mu\text{m}$  are presented. Transistor model is validated with on-wafer measurements presented in Appendix A.2. The oscillation frequency (gate delay) in combination with circuit temperature was measured at room temperature using a spectrum analyser.  $\tau_{gate}$  is calculated with Equation (4.5) and plotted versus the current per RO gate  $I_{gate}$  in Figure 4.19a.  $\tau_{gate}$  increases due to performance loss at high power dissipation. This could not be sufficiently reproduced by simulation with a constant temperature of 300K. Taking into account circuit temperature  $T_{circ}$  calculated with (4.8) improve the simulation results (solid blue line) with respect to the measurements. However, at high power dissipation,  $\tau_{gate}$  is still underestimated. A comparison of calculated and measured  $T_{circ}$  is displayed in Figure 4.19b. It can be observed that for  $I_{gate}$  greater than 2.5mA, it is not sufficient to approximate the circuit temperature with a constant thermal circuit resistance  $R_{th,circ}$ .

Therefore, the simulation temperature is set to the measured circuit temperature as a function of the dissipated power. Better agreement is observed at high power levels.

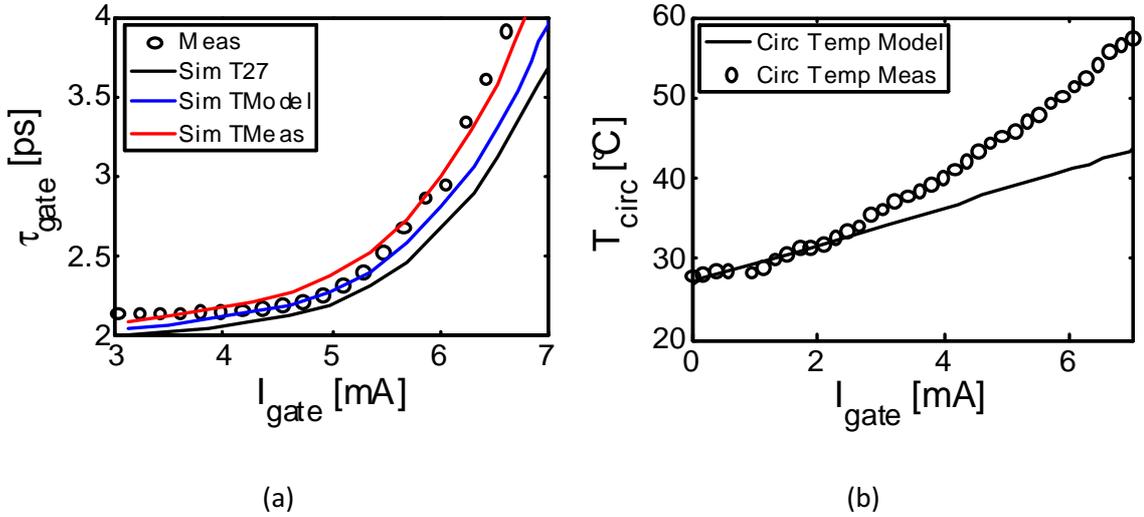


Figure 4.19: (a) The gate delay  $\tau_{\text{gate}}$  versus the current per gate  $I_{\text{gate}}$ . Measurements (symbols) and HICUM simulation (solid lines) at 300K (Sim T27), calculated circuit temperature (Sim TModel) and measured circuit temperature (Sim TMeas). (b) Measured and simulated circuit temperature versus the current per gate  $I_{\text{gate}}$ .

#### 4.2.4.6 Circuit simulations considering thermal coupling

Trends in industry are to design very large scale integration (VLSI) circuits with smaller devices, higher clock speeds, and more integration of analog and digital circuits. This increases the importance of modeling layout-dependent effects. Simulation accuracy is often limited since thermal interactions between neighboring devices are neglected. Moreover, hot spots can significantly impact the reliability of applications. In this paragraph, the extracted thermal coupling network is applied to the thermal nodes of each inverter cell of the RO. The goal is to see the impact of thermal coupling on the RO performance.

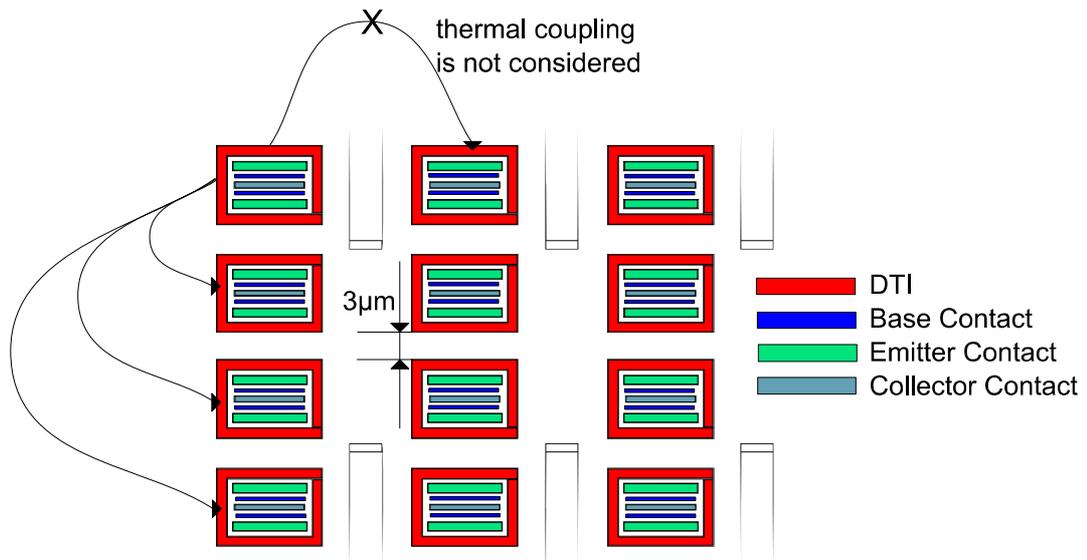


Figure 4.20: Enlarged section of RO, periodical transistor alignment, only vertical coupling considered

Figure 4.20 shows the enlarged section of the periodic RO structure. One column of four transistors represents one inverter (see layout Figure 4.21a and schematic diagram Figure 4.21b). Dimensions correspond to the inter-device coupling test structure with  $3\mu\text{m}$  distance between the DTI that is described in Paragraph 3.3.2.1. The thermal coupling network is implemented as VerilogA module. The multiport instance including the coupling parameters from Table 4 is connected to the thermal nodes of the four transistors within the inverter cell. The device's operating temperature is independently set by the operating point (power dissipation). The simulator simultaneously converges on the thermal and electrical operating conditions. The device temperatures are automatically adjusted during transient analysis to reflect the dynamic power dissipation, and at each iteration the temperature dependent model parameters are adjusted. As shown in Figure 4.20, thermal coupling is only considered between the four devices in one row. This simplification is certainly sufficient since thermal coupling in the other direction must be much lower due to the smaller adjacent surface and the larger distance ( $7.3\mu\text{m}$  between DTI) between the heat sources.

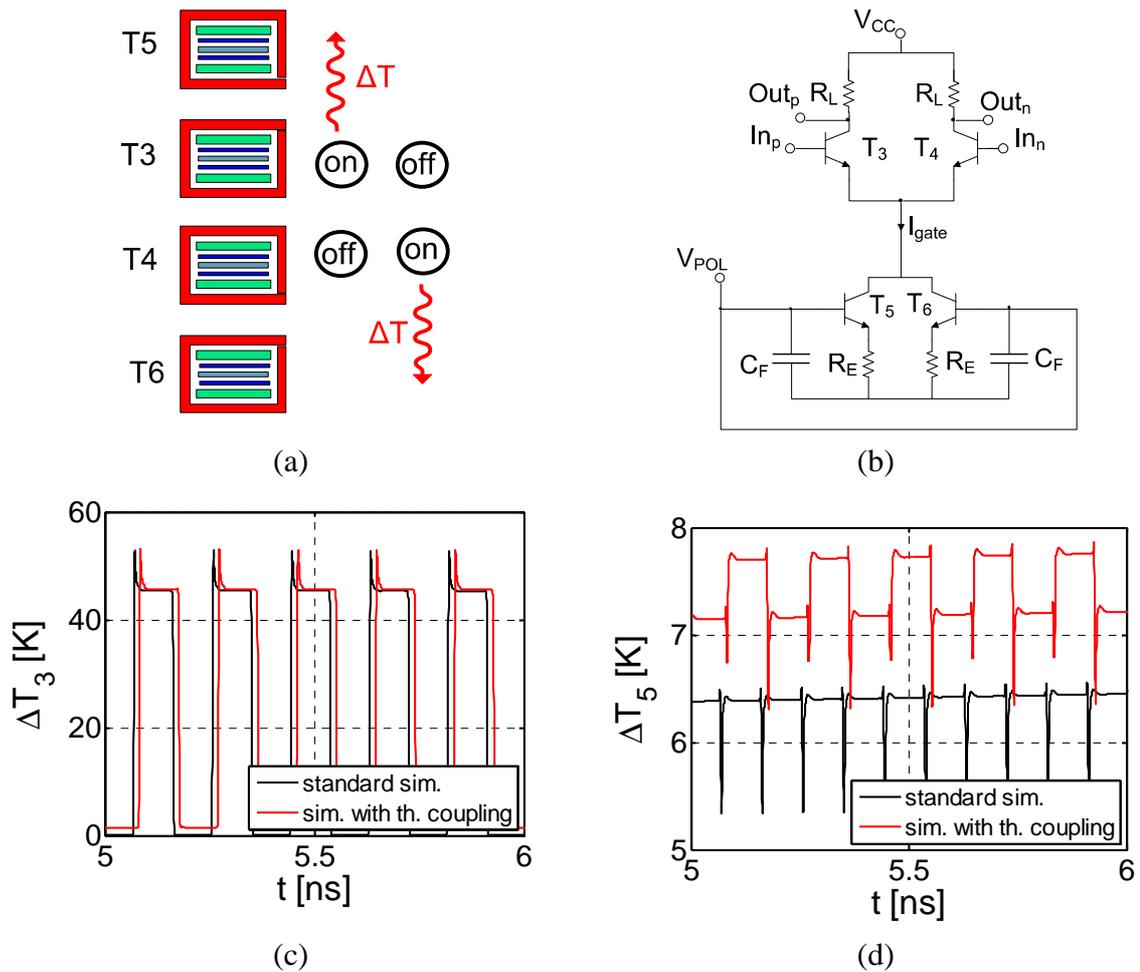


Figure 4.21: (a) Illustration of the inverter layout including the 4 transistors (T3-T6) and their operating principle. (b) Corresponding schematic diagram of the inverter cell. Transient temperature rise of transistor T3 (c) and T5 (d): Standard (black) and thermally coupled (red) transient simulation are compared.

The electrothermal dynamic interaction between the transistors is clarified with the aid of an example. First, we investigate the transient temperature rises of transistor T3 (Figure 4.21c) and T5 (Figure 4.21d). The input ( $In_p$ ,  $In_n$ ) and output ( $Out_p$ ,  $Out_n$ ) voltages are alternating with the oscillation frequency. Due to the differential operating principle of the inverter, T3 and T4 operate anti-cyclical. In other words, when T3 is “on” it means that T4 is “off” and vice versa (Figure 4.21a). The resulting temperature rise over time inside T3 and T5 using a standard ADS simulation (solid black line) is shown in Figure 4.21c and Figure 4.21d, respectively. The temperature rise in T5 is almost constant. When the circuit is simulated using the thermal network the device temperature of T5 shifts slightly when T3 heats up, as shown in red.

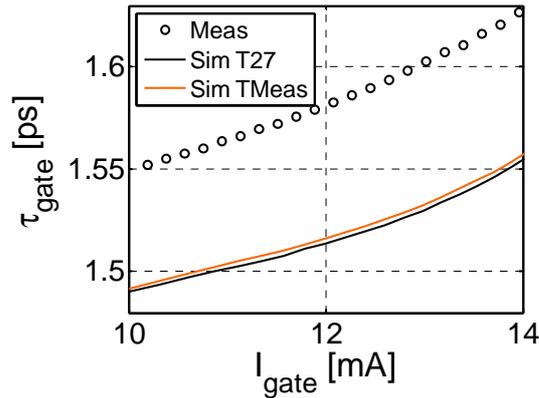


Figure 4.22: The gate delay  $\tau_{\text{gate}}$  versus the current per gate  $I_{\text{gate}}$  for B5T RO\_VI. Comparison of measured characteristic (symbols) with a standard simulation at 300K (Sim T27) and a simulation where thermal coupling is considered (Sim TCoup).

In Figure 4.22, we see the gate delay  $\tau_{\text{gate}}$  versus the current per RO gate  $I_{\text{gate}}$ . The measurement is compared with a standard ADS simulation where thermal coupling is neglected (black line). In this case, considering thermal coupling during transient simulation (red line) does not significantly change the results due to small coupling factors and the anti-cyclical operation inside the differential pair. For further improvement, thermal coupling capacitances should be extracted and considered in the model since the junction temperature in real devices does not change instantly. The fact that the transistors do not heat up significantly their environment brings up the question of whether the measured circuit temperature in Figure 4.19b is correct. Apart from the transistors there are only resistors that are able to generate the necessary heat. Indeed, looking in the process description shows that the thermal resistance of the poly resistors used in the layout is relatively high. However, this is a subject for future investigations.

As shown, the approach can be integrated in the design process and thermal interactions between neighboring devices can be easily studied. One main concern is that the coupling network could get so large that simulation becomes impractical or impossible due to given time and memory constraints. This was also a reason for us to adapt this approach for use in a relatively large circuit. Although the simulation includes 218 transistors no convergence problem was observed. Table 10 provides statistics on the simulation of the network, and shows that use of the thermal network slows the simulation by a factor around 3. Simulations were carried out under Windows XP with a quad core processor (each 3.33GHz) and an internal RAM of 3GB.

Simulation ADS	Tmin-Tmax [s]	Resistors	Transistors	Convergence Problems
RO_VI Sim Tcoup	2408.77-6411.42	599	218	no

RO_VI Sim T27	1556.77-2249.23	329	218	no
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Table 10: Comparison of the required CPU time using a conventional and a thermal coupled simulation for the RO circuit.

#### 4.2.5 Layout of the third RO version

A new layout (Figure 4.23) is proposed for the next generation STMicroelectronics B55 BiCMOS technology which is a full BiCMOS technology. Due to the distance between circuit and sensor there is a temperature difference. Therefore, a layout is proposed that integrates six temperature sensors at different positions as shown in Figure 4.24. Furthermore, non-homogeneous temperature distribution across the circuit can be studied. The parasitic resistance of the DC interconnections was further decreased using a slotted grid of M6-M8 that includes also a metal insulator metal (MIM) capacitance. The MIM capacitance protects the circuit against voltage peaks of the DC source. A slotted ground plane over the whole circuit area improves the ground resistance.

Furthermore, the presented as well as novel thermal test structures (impact of BEOL on the thermal resistance) are added on the test chip to further characterize electro-thermal effects a SiGe BiCMOS technology (full test chip in Appendix A.4, see Figure A.6).

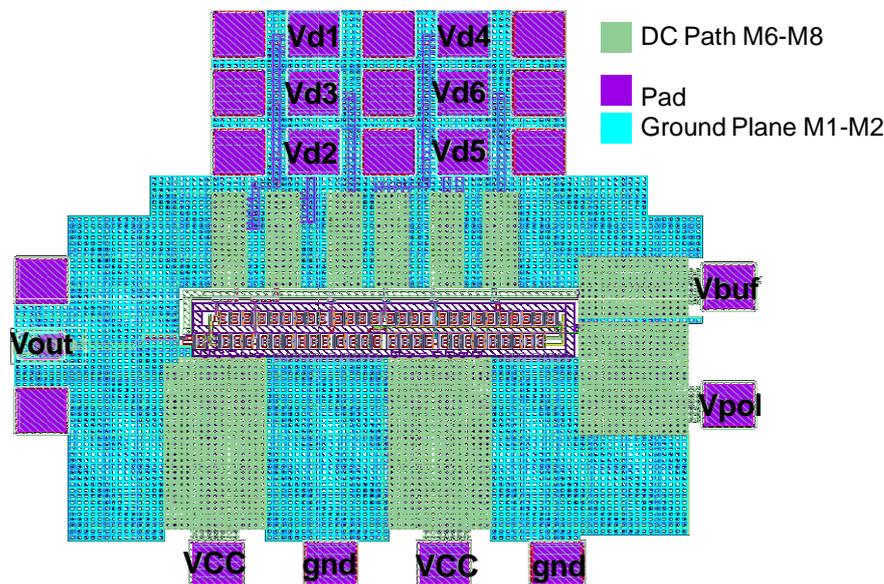


Figure 4.23: The layout of the BiCMOS55 RO.

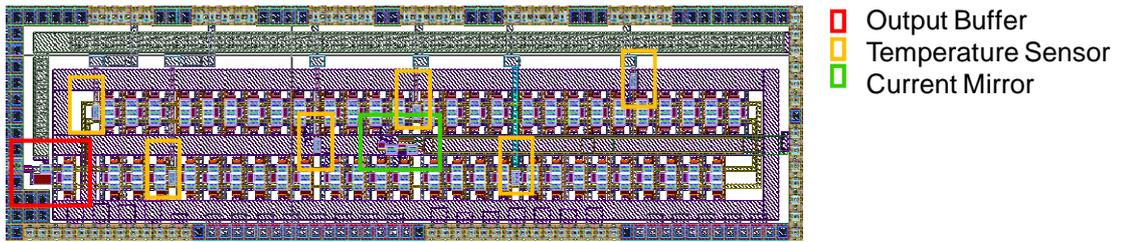


Figure 4.24: Enlarged section of the RO where the positions of six temperature sensors are indicated.

### 4.3 Transistor arrays for power amplifiers

The design of power amplifiers (PAs) often relies on experimental approaches rather than on simulation which results in an increased number of design iterations and cost. Due to large-signal excitations the operation of a PA can be strongly non-linear. Moreover, a PA is the most power-dissipating component in an RF transceiver, and therefore, its thermal performance should be analyzed. A common problem in transistor arrays is a thermal imbalance between individual devices that can cause different bias conditions. In the extreme, this imbalance can result in thermal runaway, where collector current increases until device failure occurs. Therefore, compact models are required that predict accurately the performance and individual device temperatures within a transistor array.

In this paragraph, two transistor arrays (a multi-transistor and a multi-finger PA cell) are investigated under large signal excitation regimes considering FoMs that are relevant for circuit design purposes as the power gain and the power added efficiency (PAE).

$$G = \frac{P_{out}}{P_{in}} \quad (4.11)$$

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \quad (4.12)$$

$P_{in}$  and  $P_{out}$  are the RF input and output power, respectively, and  $P_{DC}$  is the total power provided by the power supply. The thermal model presented in Paragraph 3.3.2.5 is applied to improve the accuracy of circuit simulations and to study thermal device performances.

#### 4.3.1 Test structures

The PA structures are similar to the test structures described in Paragraph 3.3.2.1. A five-finger transistor (see Figure 3.22a) and five transistor array (Figure 3.22b) based on a CBEBC HBT with drawn emitter area  $A_E$  of  $5 \times 0.18 \mu\text{m}^2$  are operated as a PA. The multi-finger device has only one surrounding DTI and the transistors in the array are placed with a distance  $D$  of  $3 \mu\text{m}$  between the DTI walls. In contrast, here the emitters are connected to ground and the base and collector contacts are respectively connected to GSG pads through  $50 \Omega$  RF transmission lines (the layout is displayed in Figure 4.25). This allows an easy DC/RF characterization and the operation as common emitter amplifier.

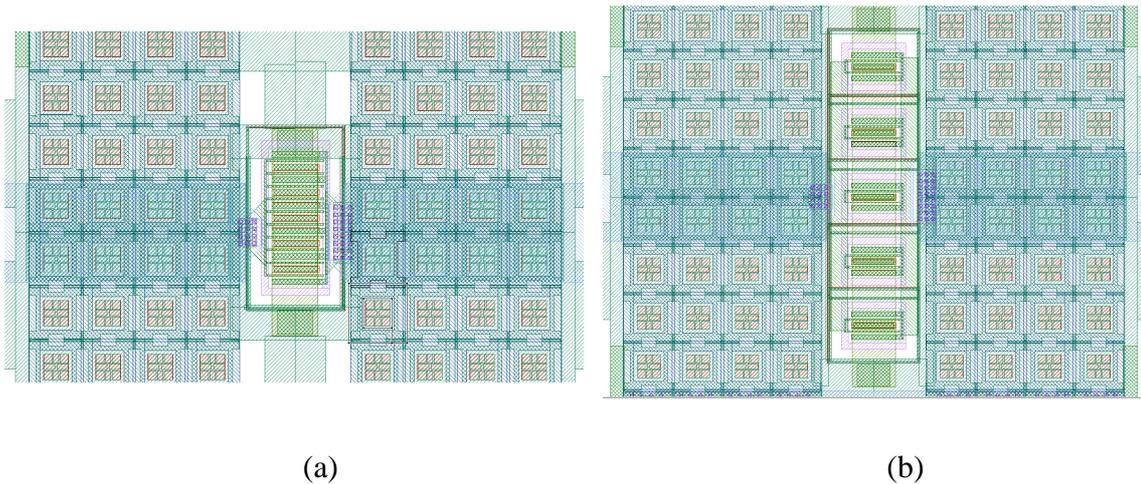


Figure 4.25: (a) Layout of the five-finger transistor test structure and (b) of the five-transistor array including slotted ground plane (M1-M2) and RF transmission lines (M6) between base/collector contacts and pads.

The impact of intra/inter-device coupling on the RF performance can be evaluated. For this study, matching networks are not required; on the contrary it allows a better comparison from the modeling perspective. However, the performance in matched condition is measured using load-pull tuners. Load-pull measurements are compared to Harmonic Balance simulations.

### 4.3.2 Harmonic Balance analysis

In large-signal regime the linearization of the transistor behavior around operating point is not valid anymore due to the nonlinear device characteristics. Strongly nonlinear circuits as PAs do not fit the definition of weak nonlinearity. Hence, rather than using an AC simulation, they should be analyzed by harmonic balance or time-domain methods [135]. Therefore, the test structures are characterized with single-tone Harmonic Balance analysis combined with load-pull variation.

In general, Harmonic Balance (HB) is a frequency domain analysis technique which is applicable primarily to strongly nonlinear circuits (power amplifiers, mixers, etc.) excited by a single large-signal source [135]. The goal is to determine a steady state time-domain solution. A system of nonlinear differential equations is generated using Kirchhoff's current law (written in frequency domain). They consist of linear and nonlinear parts. The linear part is readily described and calculated using nodal analysis directly in the frequency domain. Since nonlinear devices are described in the time domain the nonlinear components are evaluated in the time domain using an inverse fast Fourier transform (connection between time and frequency domain is shown in Figure 4.26). After evaluation using the time-domain voltage waveforms the resulting currents are then transformed back into the frequency domain. An iterative process repeats these steps since Kirchhoff's current law is fulfilled (convergence is reached). Since a large

part of the calculations is carried out directly in the frequency domain HB analysis has crucial advantages in comparison with transient analysis due to time and memory requirements [7].

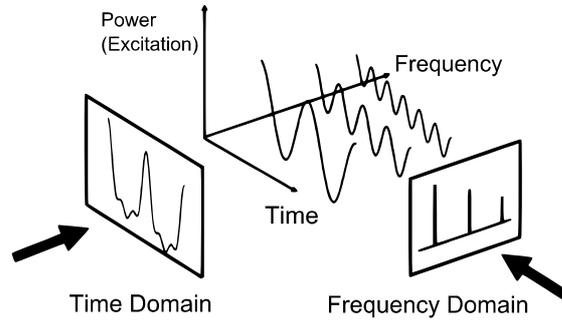


Figure 4.26: Transformation between time and frequency domain.

The basic simulation test bench that was used is shown in Figure 4.27. The RF power source having an input resistance  $Z_S$  of  $50\Omega$  generates an input signal at  $60\text{GHz}$ . RF signal and DC bias is combined/separated using a bias network. The ideal bias networks consist of one capacitance ( $C_{\text{Block}}$ ) and one inductor ( $L_{\text{Feed}}$ ). The load impedance and input resistance  $Z_S$  can be automatically varied (load/source-pull analysis). Since the de-embedding of large signal measurements is rather complex, the parasitic elements (pads, interconnections, etc.) are embedded using a RCL network. The parasitic capacitances  $C_{Pn}$  are calculated with the Equations (4.13) from measured Y parameters of an Open dummy and the parasitic inductances  $L_{Pn}$  are calculated with the Equations (4.14) from measured Z parameters of a Short dummy.

$$C_{p1} = \frac{\Im\{Y_{11} + Y_{12}\}}{2\pi f} \quad C_{p2} = \frac{\Im\{Y_{22} + Y_{12}\}}{2\pi f} \quad (4.13)$$

$$L_{p1} = \frac{\Im\{Z_{11} - Z_{12}\}}{2\pi f} \quad L_{p2} = \frac{\Im\{Z_{22} - Z_{12}\}}{2\pi f} \quad (4.14)$$

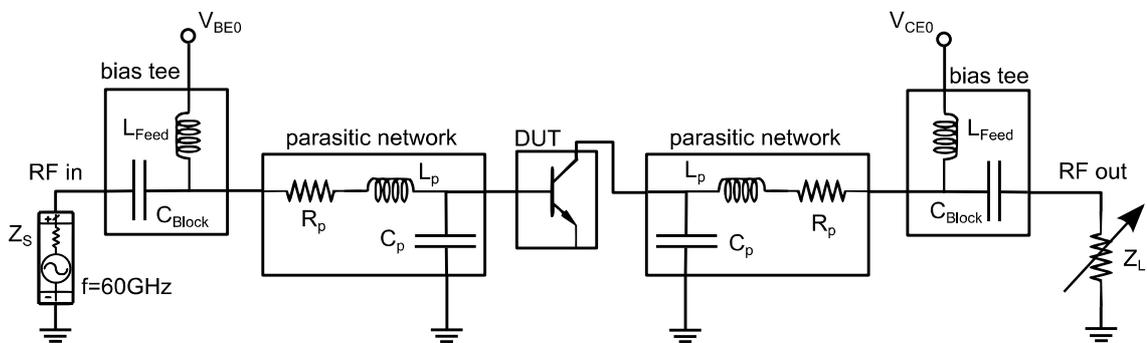


Figure 4.27: Harmonic Balance test bench (for array test structures:  $L_{\text{Feed}}=1\mu\text{H}$ ,  $C_{\text{Block}}=1\mu\text{F}$ ,  $R_p=1\Omega$ ,  $L_p=20\text{pH}$ ,  $C_p=25\text{fF}$ ).

### 4.3.3 Load-pull measurements

The load-pull technique uses impedance tuners that systematically vary the source and load impedances presented to the ports of the DUT while measuring its performance. Load/source-pull is generally used to characterize nonlinear devices in actual large signal operating conditions where the operating point may change with power level or tuning. Various matching conditions of the device can be studied to achieve, for example, optimum power gain, noise figure or PAE.

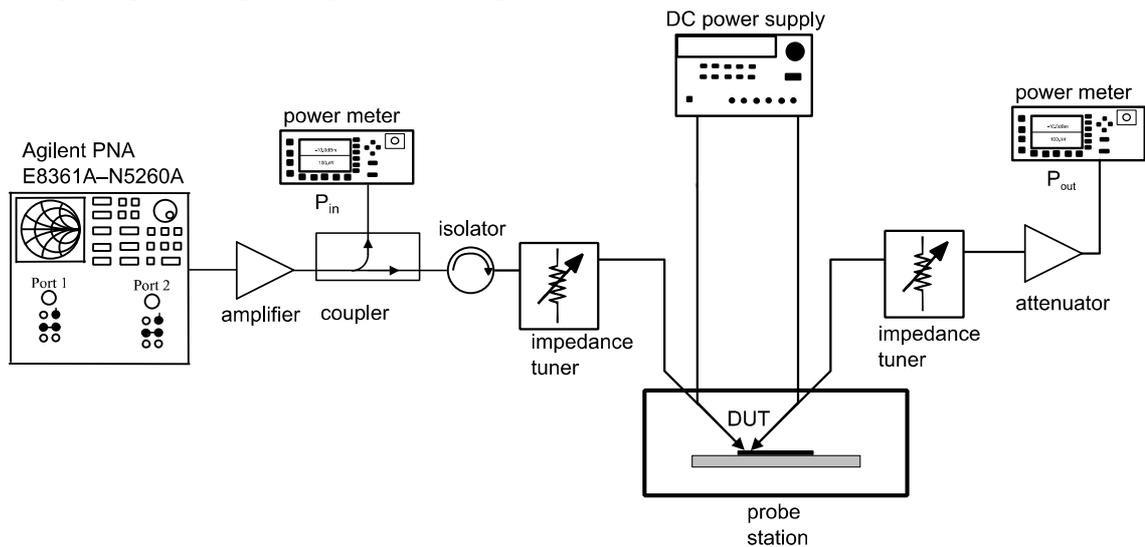


Figure 4.28: Load pull measurement bench

The load-pull measurement test bench [136] is presented in Figure 4.28. The passive load and source tuners (FOCUS CCMT) allow generating complex impedances between 57-90GHz. The network analyzer Agilent PNA E8361A-N5260A is used for calibration and as a signal generator up to 110GHz. A directional coupler divides the input signal into two parts. One is guided to the power meter for measuring the power delivered to the DUT and the other one is the actual input signal. The isolator prevents the reflected signal from returning in the coupler. A manual probe station permits the connection to the DUT using RF on-wafer probes (GSG infinity probes from CASCADE with integrated bias tees). The measurement is controlled by the Focus Explorer via GPIB and Ethernet.

### 4.3.4 Results and discussion

As observed in Figure 3.33b for the RO, the effect of inter-device coupling is rather small. Therefore, it is not considered for the MTA. Circuit simulation is carried out using five CBEB transistor models (verified in Paragraph 2.4) in parallel. In contrast, intra-device thermal coupling cannot be neglected. Hence, the MFT is simulated using five thermally coupled transistor finger models (different values for  $R_{th}$  and  $r_{cx}$ ) as described in Paragraph 3.3.2.5 using the extracted coupling parameters from Table 2.

4.3.4.1 Large signal analysis

The B5T HBT (drawn  $A_E$  of  $5 \times 0.18 \mu\text{m}^2$ ) and the PA arrays were measured on-wafer at 60GHz with the single-tone load-pull measurement system presented in the previous paragraph. The single transistor was biased in Class A operation at a  $V_{BE}$  of 0.9V with a collector bias  $V_{CE}$  of 1V. First, a source pull measurement was carried out and the optimum source impedance  $Z_s$  with respect to maximum output power was found to be  $[22.16+j15.13]\Omega$ . Second, the load impedance was varied using an input power  $P_{in}$  of -6dBm.

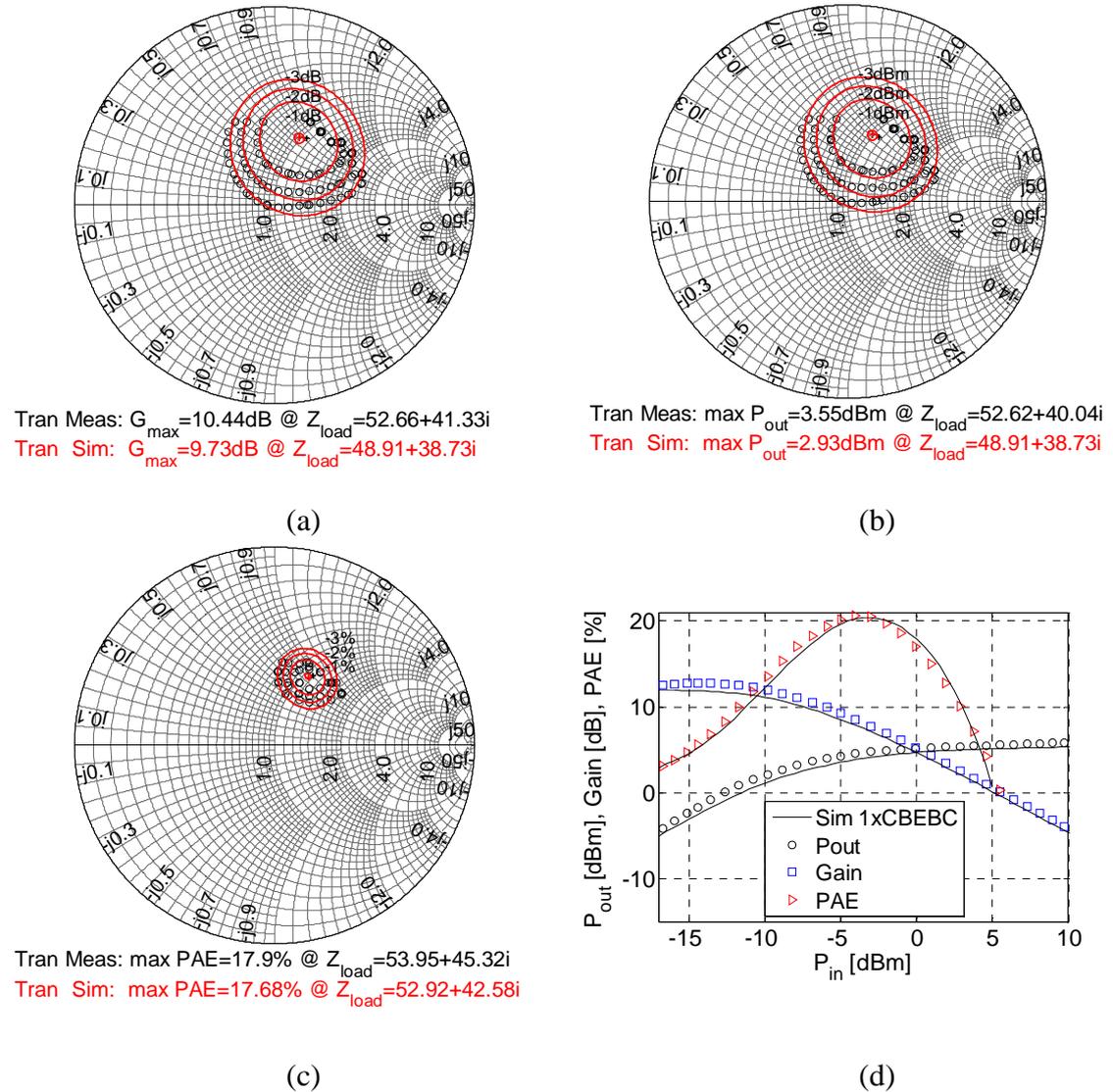


Figure 4.29: The normalized impedance ( $50\Omega$ ) seen by the collector of the DUT under matched and mismatched load is plotted on a Smith chart. Load pull contours for constant power gain (a), output power  $P_{out}$  (b) and power added efficiency PAE (c) at an input power  $P_{in}$  of -6dBm and an optimum source impedance  $Z_s$  of  $[22.16+j15.13]\Omega$ . (d)  $P_{out}$ , Gain, PAE resulting from power measurement using a load impedance match to achieve maximum  $P_{out}$  ( $Z_{load}=[52.66+j41.33]\Omega$ ).

Load pull contours for the power gain, the output power  $P_{\text{out}}$  and the power added efficiency PAE are shown in Figure 4.29a, b and c, respectively. The load impedance to achieve maximum output power is found to be  $Z_{\text{load,opt}}=[52.66+j41.33]\Omega$ . The input power  $P_{\text{in}}$  versus output power  $P_{\text{out}}$ , Gain and PAE in matched condition ( $Z_{\text{load,opt}}$ ) is presented in Figure 4.29d. The maximum RF power gain is 12.8dB and the measured maximum PAE is 20.1% at a  $P_{\text{out}}$  of -4dBm. The collector current  $I_C$  near maximum PAE is 10mA. Very good agreement is observed between Harmonic Balance simulation (lines) using the transistor compact model (verified in Paragraph 2.4) and RF power measurement (symbols). A load pull analysis at 94GHz of the same device was presented in [49].

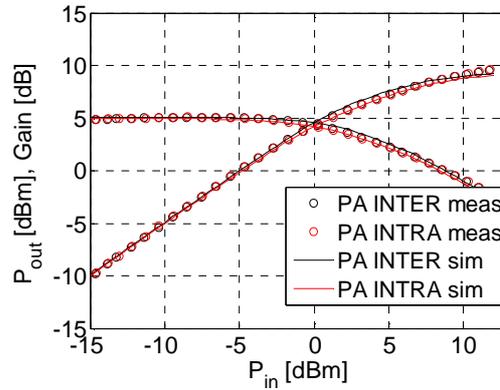


Figure 4.30: Output power  $P_{\text{out}}$  and power gain vs. input power  $P_{\text{in}}$  for multi-finger and the multi-transistor device with  $A_E=0.18 \times 5 \mu\text{m}^2$  using a source impedance  $Z_s=50\Omega$  and a load impedance  $Z_{\text{load}}=50\Omega$ .

The MFT (INTRA) and the MTA (INTER) are measured at same bias conditions ( $V_{\text{BE}}=0.9\text{V}$ ,  $V_{\text{CE}}=1\text{V}$ ). Output power and power gain is shown in Figure 4.30. For these bias conditions the electrical characteristics for both devices are close and in good agreement with circuit simulations. From the DC measurements presented in Figure 3.33a and Figure 3.33b, it can be observed that at this bias condition the influence of the thermal coupling effect is relatively small.

In the following measurement the collector bias  $V_{\text{CE}}$  is increased to 1.5V. The resulting load pull contours for the MTA and MFT are displayed in Figure 4.31a and b, respectively. Measured and simulated gain contours are in fair agreement. Simulation and measurement result in different optimum load impedance for the five-finger transistor. This can be caused due to insufficient accuracy of the extracted parasitic network that is used within the simulation (see Figure 4.27). The difference of around 1dB in maximum achievable gain  $G_{\text{max}}$  is probably due to the transistor model that lacks accuracy at this relatively high bias condition.

The output power and power gain in matched condition is shown in Figure 4.31c. The RF characteristics of both PA structures differ significantly that is certainly caused

due to thermal coupling within the MFT. A difference in maximum gain of nearly 4dB can be observed. Circuit simulations considering thermal coupling confirm this observation.

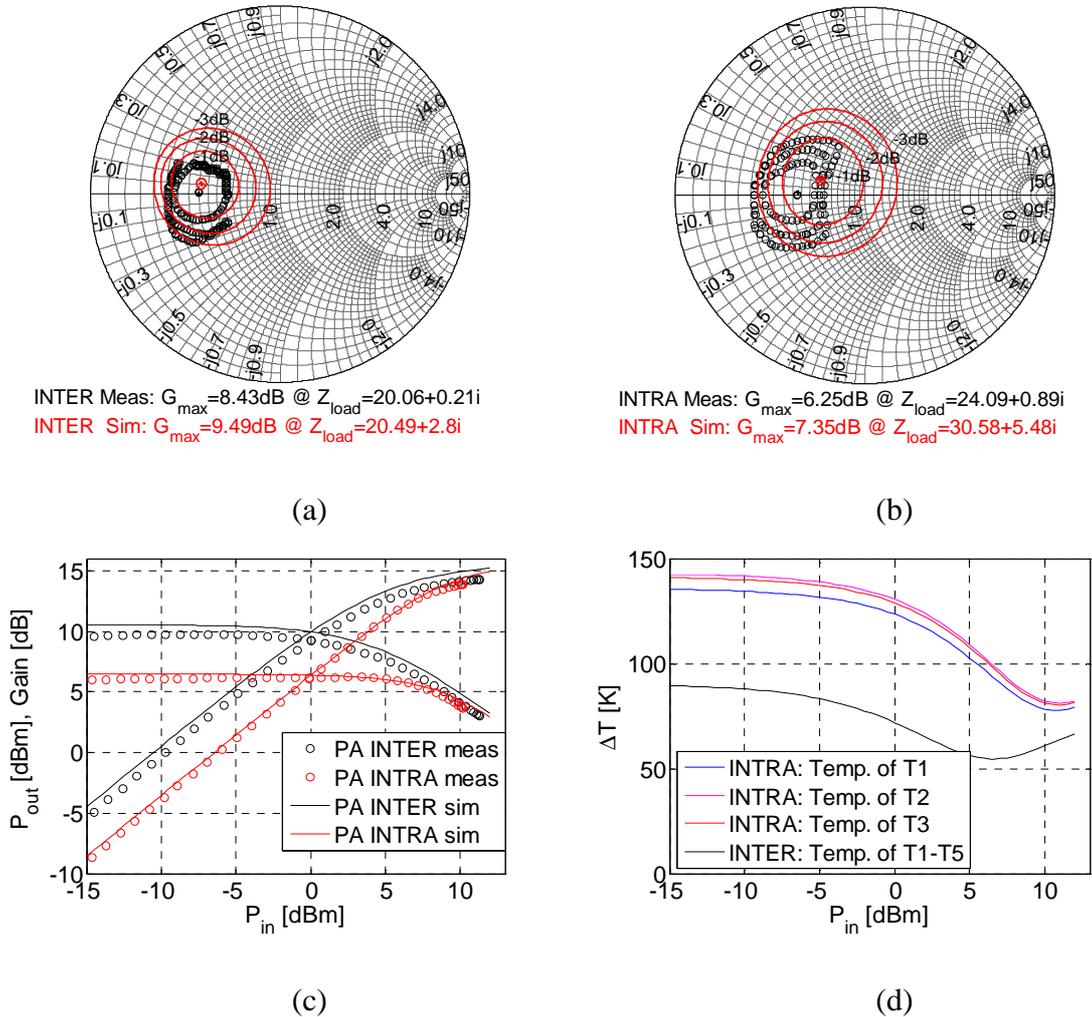


Figure 4.31: Measured and simulated gain contours (-1dBm, -2dBm, -3dBm from the maximum) at (a)  $V_{CE}=1.5V$ ,  $P_{in}=2.41dBm$ ,  $Z_{s,opt}=[13.17-j3.50]\Omega$  for the transistor array (INTER) and at (b)  $V_{CE}=1.5V$ ,  $P_{in}=0.7dBm$ ,  $Z_{s,opt}=[10.46-j6.75]\Omega$  for the five-finger device (INTRA). (c)  $P_{out}$  and power gain vs.  $P_{in}$  for optimum power matching  $Z_{load}=[20.06+j0.21]\Omega$  (INTER) and  $Z_{load}=[24.09+j0.89]\Omega$  (INTRA). (d) Simulated temperatures of the finger transistors T1, T2 and T3 (T4, T5 symmetrical to T2, T1) are compared with the array transistor temperature (same for T1-T5).

In Figure 4.31d, the simulated temperatures of the finger transistors T1, T2 and T3 (see schematic diagram in Figure 3.20a) are compared with the transistor temperatures of the array (that are all equal). At a first glance it seems odd that the temperature decreases with input power. However, the collector current decreases due to clipping of the output signal. Therefore, the power dissipation, and thus, the device temperature are reduced. At lower  $P_{in}$ , the temperature of the transistor array is almost  $50^{\circ}C$  lower using same bias conditions. Moreover, a temperature difference of  $7^{\circ}C$  between the peripheral

and the central finger transistor can be observed resulting in a difference in collector current  $\Delta I_C \approx 7\text{mA}$ . The proposed model simplifies the work for the designer to compensate this thermal imbalance. Having access to the thermal nodes (junction temperatures) of each finger additional emitter resistances can be easily estimated to distribute the collector current more equally within the multi-cell structure.

#### 4.4 Conclusions

Two state of the art Si/SiGe:C HBT CML ROs with a single ended voltage swing of 200mV were designed with more than 200 transistors. An average gate delay of 1.65ps has been demonstrated. To the authors' knowledge, this is the fastest result for a bipolar transistor based technology. Improvements in this work were obtained for an advanced process by an optimized ring oscillator design with inductive peaking in series with the load resistor. This work demonstrates that RO design can have a significant impact on the gate delay.

The electrical and thermal behavior of the ROs was studied. Circuit simulation at high power dissipation has been improved through considering the temperature rise within the circuit due to mutual heating of all active and passive components. This approach is still limited due to simplifications made in the estimations. Moreover, it neglects the inhomogeneous temperature distribution across the circuit. However, in general the presented approach is a simple method for circuit designers to consider the circuit temperature as a function of the dissipated power, if advanced thermal models are not available or not applicable due to e.g. high simulation time or convergence issues.

Furthermore, the method of [116] for the representation of static substrate thermal coupling in circuit simulation applications was applied for the full RO circuit. The presented approach facilitates the realization of circuits with temperature critical layout regions. In the RO, the impact of thermal coupling between the transistors is negligible small due to the small coupling factors and the anti-cyclical operation of neighboring devices. Nonetheless, this information is useful for the designer since the transistors can be placed even closer together to reduce wiring parasitics. The characterization of the thermal coupling effect should be further improved considering thermal coupling capacitances. They can be measured using the presented test structures using a locked-in amplifier as presented in [137]. Moreover, the mutual heating between resistors and transistors in close proximity should be investigated.

In the second part, two transistor arrays were operated as 60GHz power amplifier cells to study electrical and thermal performances. The investigated CBEB transistor has a maximum RF power gain of 12.8dB and a maximum PAE is 20.1% at a  $P_{\text{out}}$  of -4dBm which confirms its potential for high-frequency applications. Excellent accuracy

of the single transistor compact model for large signal operation was presented. Moreover, the electrical and thermal performance between multi-finger transistor and multi-transistor array was compared. For lower bias the devices have similar behavior due to the same number of transistors/fingers and the same emitter window. However, for higher voltages their comportment significantly differs due to the different device temperatures. In general, multi-transistor arrays have higher access capacitances. Therefore, normally multi-finger devices are preferred for millimeter-wave circuit designs. However, their thermal performances in terms of homogenous temperature distribution and junction temperature at same bias conditions are degraded due to higher thermal coupling.

Moreover, the intra-device coupling model with implementation of thermal resistances and temperature coupling parameters obtained through numerical thermal simulation and measurements was applied. Very good agreement between the model and measurements was shown. A similar accuracy in circuit simulation can be probably also achieved using a lumped model with a single fitted thermal resistance. However, this would totally ignore the non-homogeneous temperature distribution across the multi-finger device. Moreover the designer would have no access to thermal nodes of each finger. Therefore, he cannot compensate different finger temperatures by adapting the finger distances (unfortunately this option is not often available) or including ballasting resistors (as shown in Figure 1.12). To improve the thermal stability in multiple-finger

## Chapter 5 Conclusions and recommendations

### 5.1 General conclusions

In this work, self-heating of single devices and thermal coupling of multiple devices in a state of the art SiGe HBT technology was characterized and modeled. Electrothermal feedback intra-and inter-device was extensively studied. Moreover, their impact on the performance of two analog circuits was evaluated. Circuit and device characterization were carried out on the same wafer which was required to verify compact models on circuit level (device to circuit interaction).

The self-heating effect has been evaluated with low frequency measurements and with a state of the art pulse measurement system. Self-heating inside the device has been significantly decreased using small pulse widths. Hence, compact model parameter extraction methodology becomes more accurate and the safe-operating-area of the device can be expanded. Frequency dependent thermal heating was investigated using Y and H parameters. A generalized equation has been validated, which can be used to extract device thermal impedance in the frequency range below thermal cut-off frequency. The frequency dependence of the thermal impedance should not be neglected for a number of circuits. The 1/f or flicker noise can be influenced to some extent [70]. At low modulation frequencies, thermal memory effects can be harmful for most linearizers, such as predistorters [111].

Novel test structures were fabricated for the measurement of thermal coupling effect between single devices (inter-device) as well between the emitter stripes of a multi-finger transistor (intra-device). Thermal coupling factors were extracted from measurements as well as from 3D thermal simulations. Inter-device coupling using a minimum distance between the deep trenches of 1.5 $\mu\text{m}$  was found to be less than 5% due to the thermal isolation achieved with deep trench walls around each transistor. The thermal coupling effect, as expected, is reduced with wider spacing. In contrast, intra-device coupling is much more pronounced. A maximum coupling of 17% between neighboring fingers was measured. Due to restrictions in the design rules of the PDK it was not possible to study a wider spacing of emitter fingers.

The single pole thermal network of HICUM was extended with a nine element recursive thermal resistance model as well as a thermal coupling model. The models can be implemented, for example, as a netlist or as a VerilogA model which makes them easy to use for a circuit designer. The better accuracy of the recursive network has been verified comparing pulsed compact model simulation with pulsed measurements. Ther-

mal coupling model allows studying the impact of neighboring heat sources on the steady state and the transient device temperature. A fully coupled transient simulation of a PA and of a RO with 218 transistors was performed.

A CML ROs with a record gate delay of 1.65ps has been demonstrated. To the authors' knowledge, this is the fastest result for a bipolar transistor based technology. It has been shown that the circuit layout can have a significant impact on the circuit performance. RO circuit simulation at high power dissipation has been improved through considering the temperature rise within the circuit due to mutual heating of all active and passive components.

The thermal performance of a 60GHz power amplifier was compared when realized with a multi-transistor array and with a multi-finger transistor. Due to same emitter dimensions similar electrical behavior is observed at lower power dissipation. At high power dissipation their comportment significantly differs due to the different device temperatures. Electrical performance of the multi-finger transistor is degraded due to the significant thermal coupling effect between the emitter stripes. Measurements are in good agreement with circuit simulations using lumped transistor models in combination with the thermal coupling network. A similar accuracy could be probably also achieved using a lumped model with a single fitted thermal resistance. However, this would totally ignore the non-homogeneous temperature distribution across the multi-finger device. Moreover the designer would have no access to thermal nodes of each finger.

## **5.2 Electrothermal simulation in a CAD based circuit design**

Circuit simulations using the standard single pole thermal network have only limited value for transistors placed in close proximity since the constant temperature operation is an unrealistic constraint. The thermal interaction inside multi-finger structures should be treated in a physical manner. In this paragraph a scenario is proposed in order to include thermal analysis into a CAD based circuit design process.

The benefits for the designers would be various. The accuracy of steady state and transient simulation for circuits with a high power density is significantly improved. Thermal performances can be optimized with changes in the circuit layout to meet the electrical specifications (power, gain, efficiency, area, thermal stability, etc.). The thermal stability in multiple-finger transistors can be increased by adjustment of emitter to emitter distances to make the spatial temperature distribution across the device approximately uniform [57], [138], [139]. Moreover, the access to thermal nodes of each emitter of a multi-finger device would allow estimating ballasting resistors. Thermal shut-down circuit [140] for the protection of electronic circuits can be easily implemented.

Certainly, the investigations in this work are still very basic, they are far from complete. The implementation of such a system would require a fast thermal solver that calculates thermal coupling factors from the circuit layout and creates automatically a netlist. Similar to conventional post-layout simulations the designer can then monitor the operating temperature of critical devices and if necessary he can adapt the circuit layout. Since the thermal simulation carried out in Paragraph 3.3.2.4 would require too much computational effort simplified approach as presented in [128], [141] is preferred. However, such a simulator could be calibrated with the proposed test-structures due to material parameters that can differ for each technology (e.g. the thermal conductivity). Furthermore, the circuit environment temperature can be considered using the thermal resistance of the circuit that can be calculated by indicating the effective chip surface. This was shown in Paragraph 4.2.2.2 using a very rudimentary equation. However, whether or not thermal issues will limit the speed of future high speed circuits, they must be taken into account in the design phase and so must be accurately predictable.



# Appendix A

## A.1 Model verification for B4T CBEBE HBT with $A_E=0.23 \times 5 \mu\text{m}$

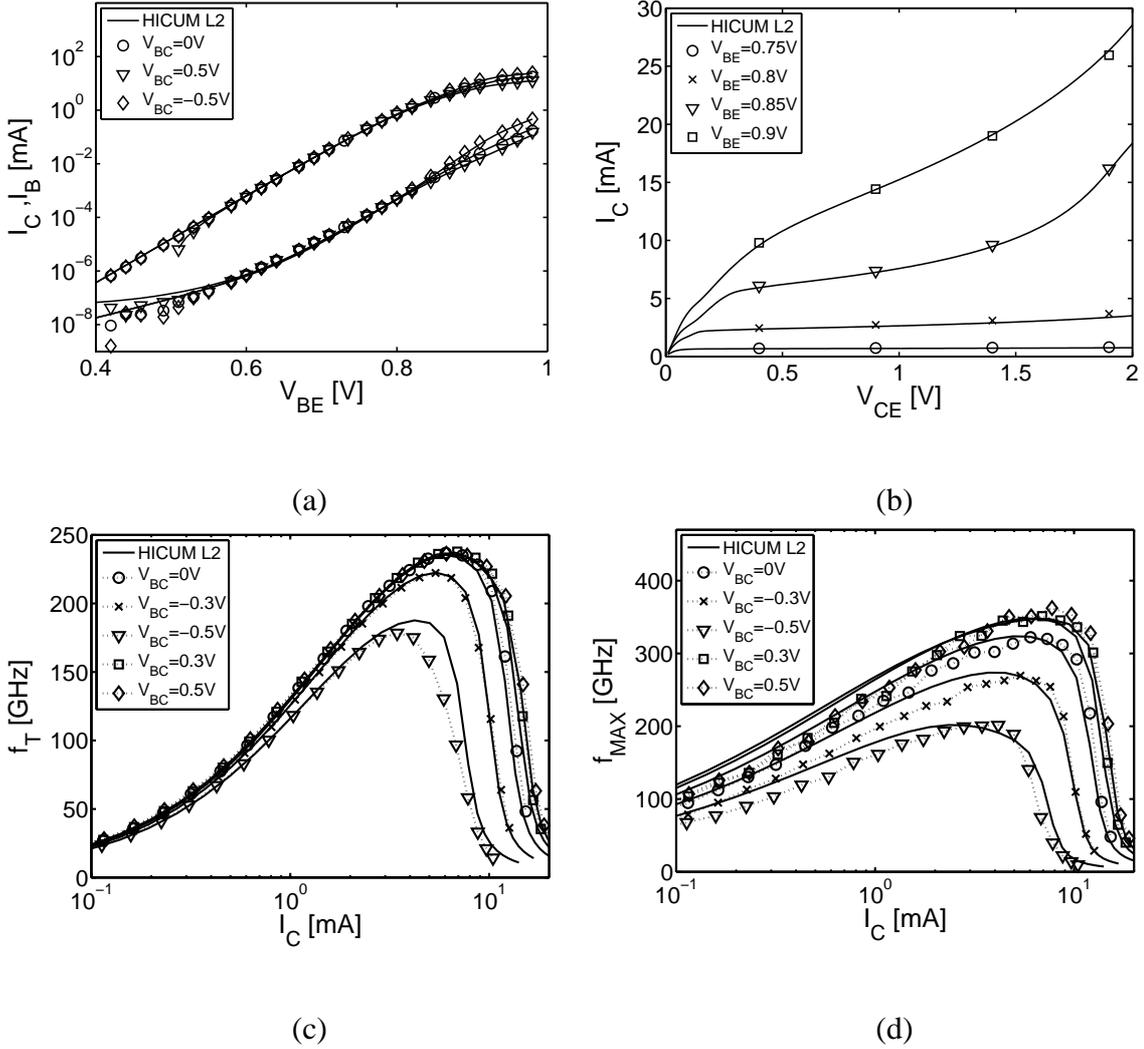


Figure A.1: Measurements (symbols) and HICUM simulation (solid lines) for B4T HBT (CBEBE) with drawn emitter area  $A_E=0.23 \times 5 \mu\text{m}$ : (a) Forward Gummel plot at base-collector voltage  $V_{BC}=(-0.5, -0.3, 0, 0.3, 0.5)\text{V}$ . (b) Output characteristics at base-emitter voltage  $V_{BE}=(0.75, 0.80, 0.85, 90, 0.95)\text{V}$ . (c) Transit frequency  $f_T$  at  $V_{BC}=(-0.5, -0.3, 0, 0.3, 0.5)\text{V}$ . and (b) maximum oscillation frequency  $f_{\text{max}}$  at  $V_{BC}=(-0.5, -0.3, 0, 0.3, 0.5)\text{V}$ .

## A.2 Model verification for B5T CBEBC HBT with $A_E=0.18 \times 1.5 \mu\text{m}$

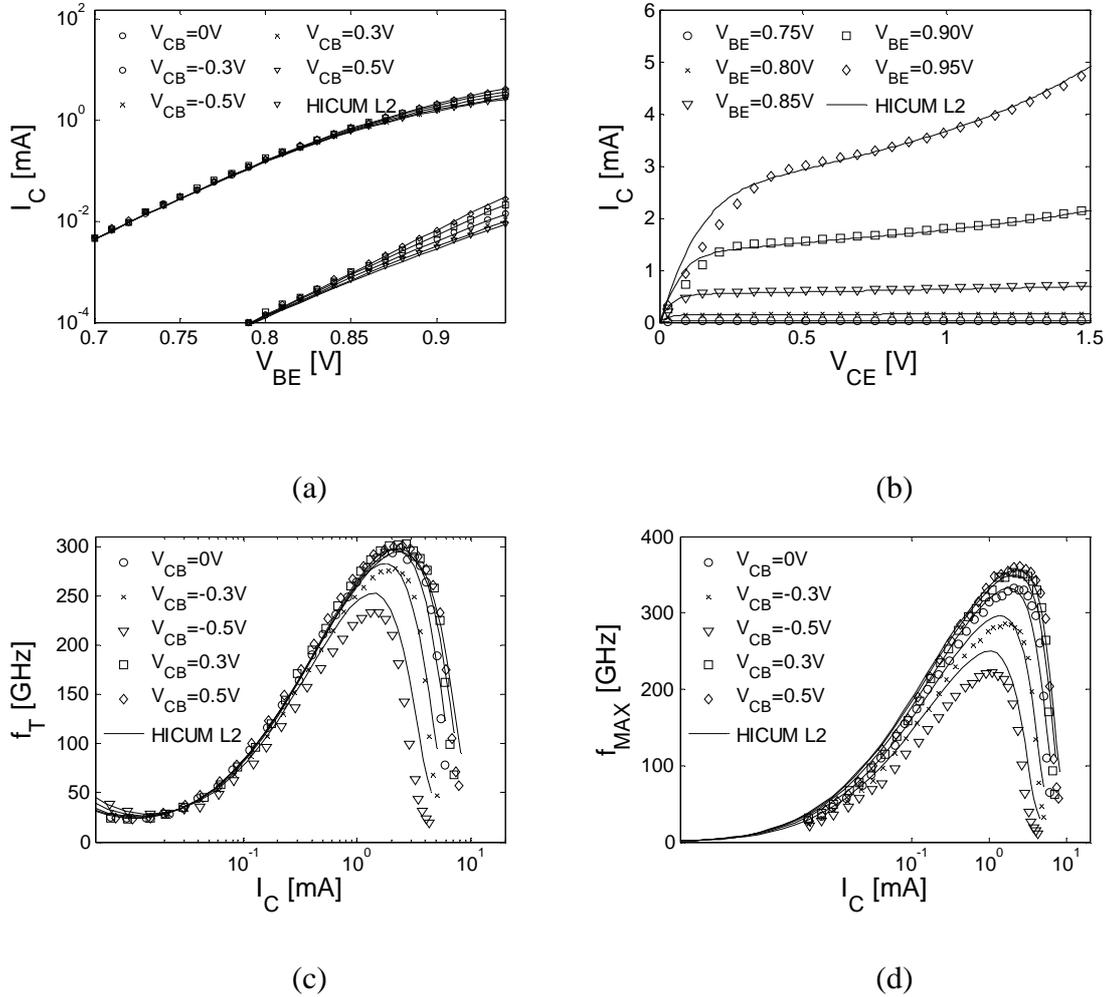


Figure A.2: Measurements (symbols) and HICUM simulation (solid lines) for B5T HBT (CBEBC) with drawn emitter area  $A_E=0.18 \times 1.5 \mu\text{m}$ : (a) Forward Gummel plot at base-collector voltage  $V_{BC}=(-0.5, -0.3, 0, 0.3, 0.5)V$ . (b) Output characteristics at base-emitter voltage  $V_{BE}=(0.75, 0.80, 0.85, 0.90, 0.95)V$ . (c) Transit frequency  $f_T$  at  $V_{BC}=(-0.5, -0.3, 0, 0.3, 0.5)V$ . and (b) maximum oscillation frequency  $f_{max}$  at  $V_{BC}=(-0.5, -0.3, 0, 0.3, 0.5)V$ .

A.3 RO measurements: 1<sup>st</sup> layout on B9MW, B3T and B4T (first run) technology

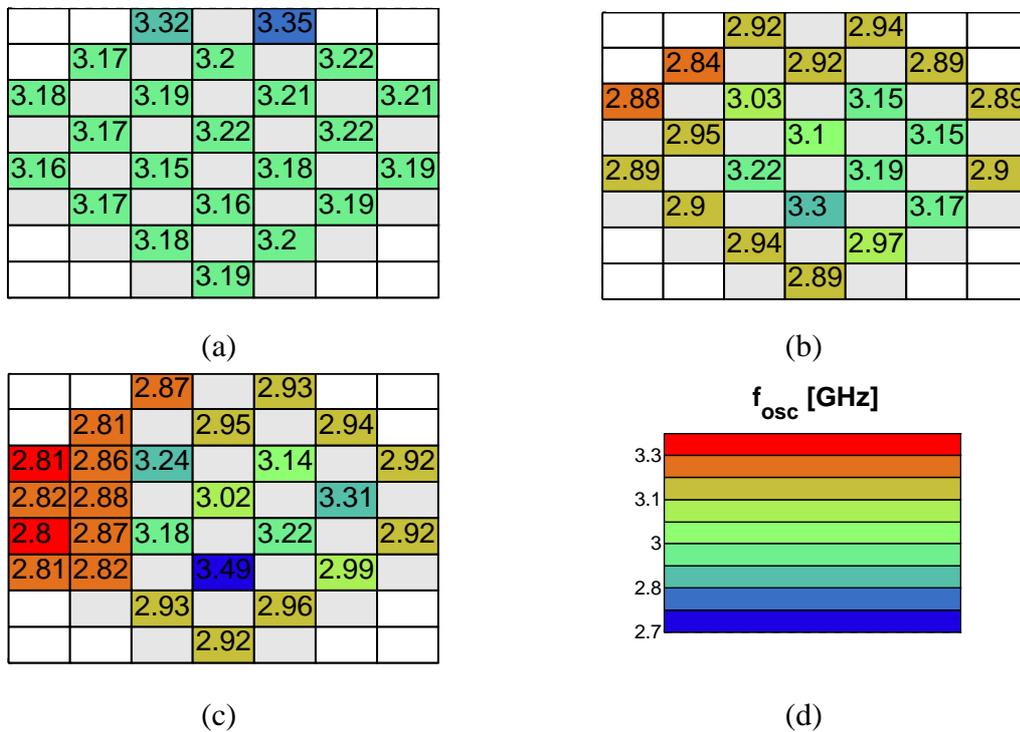


Figure A.3: Wafer-map of RO gate delays measured on (a) B9MW (b) B3T (c) B4T (first run) technology at  $V_{CC}=3V$  and  $V_{POL}=1.9V$ . (d) The colors show the corresponding oscillation frequency.

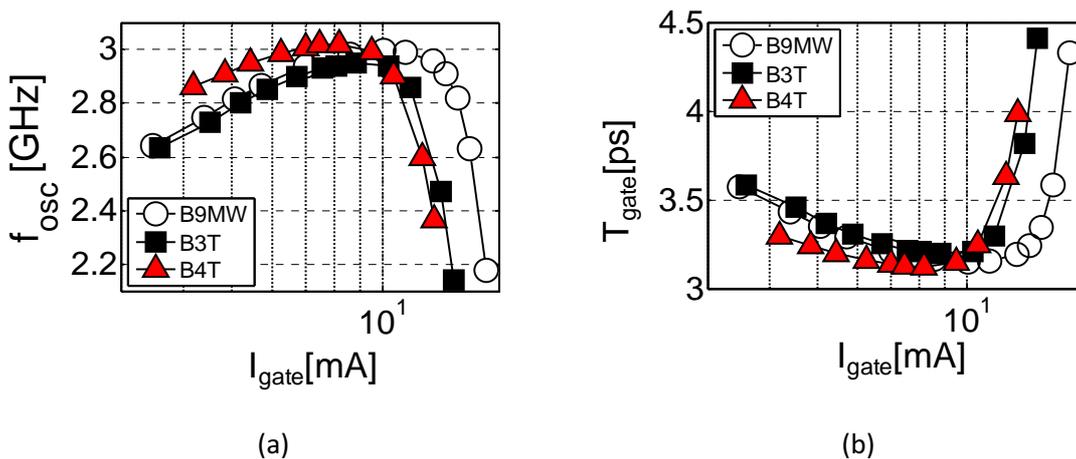


Figure A.4: (a) Oscillation frequency  $f_{osc}$  vs. current per gate  $I_{gate}$ . (b) Propagation gate delay  $\tau_{gate}$  vs. current per gate  $I_{gate}$ .

A.4 Designed test chips for B5T and B55 technology

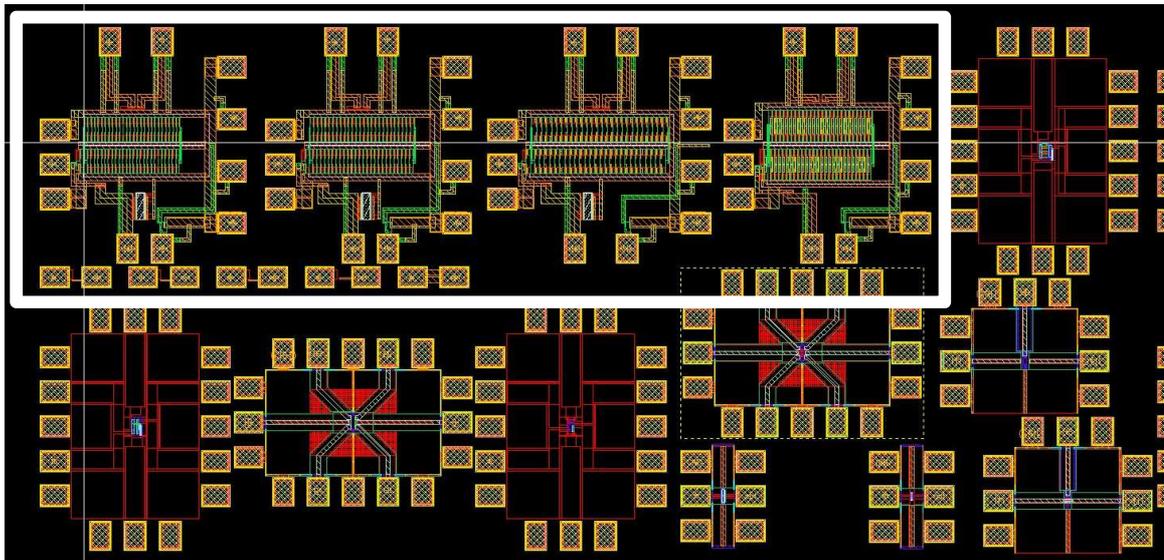


Figure A.5: Test chip including the ROs and all specially designed test structures for the B5T technology.

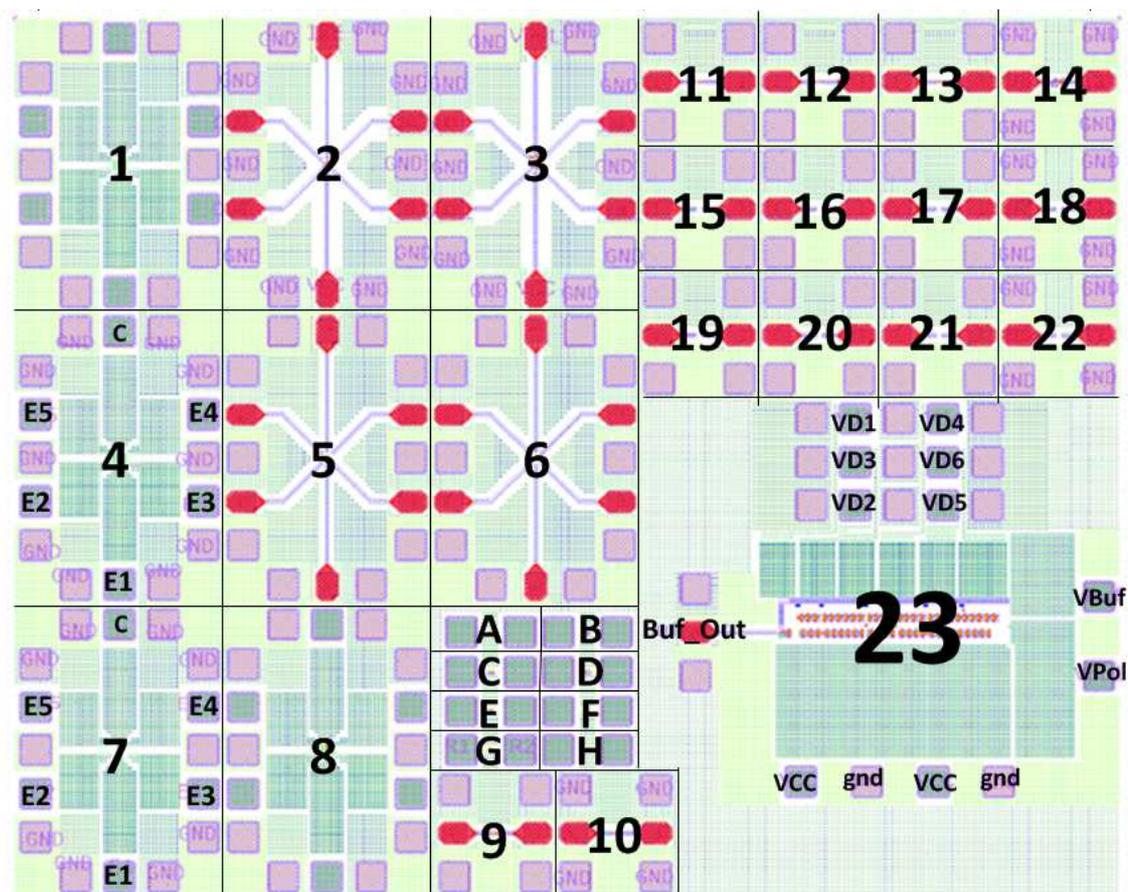


Figure A.6: Test chip including the RO and all specially designed test structures for the BiCMOSB55 tape-out (in fabrication).

### A.5 Sensitivity analysis of process parameter on the performance of LNA 94GHz

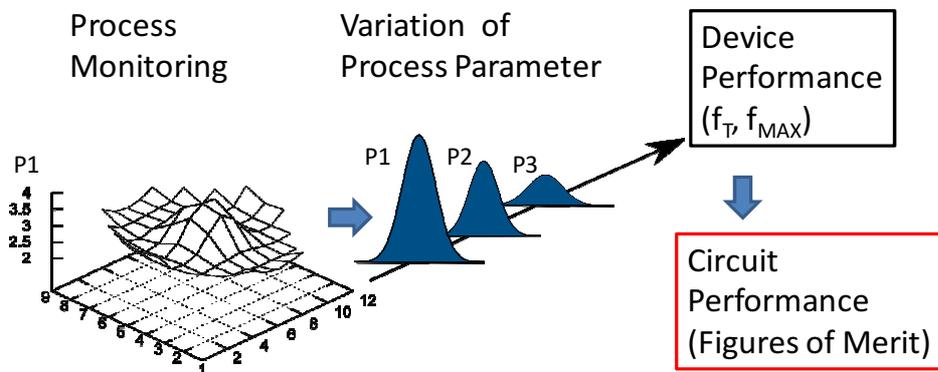


Figure A.7: Impact of process parameter on the circuit performance.

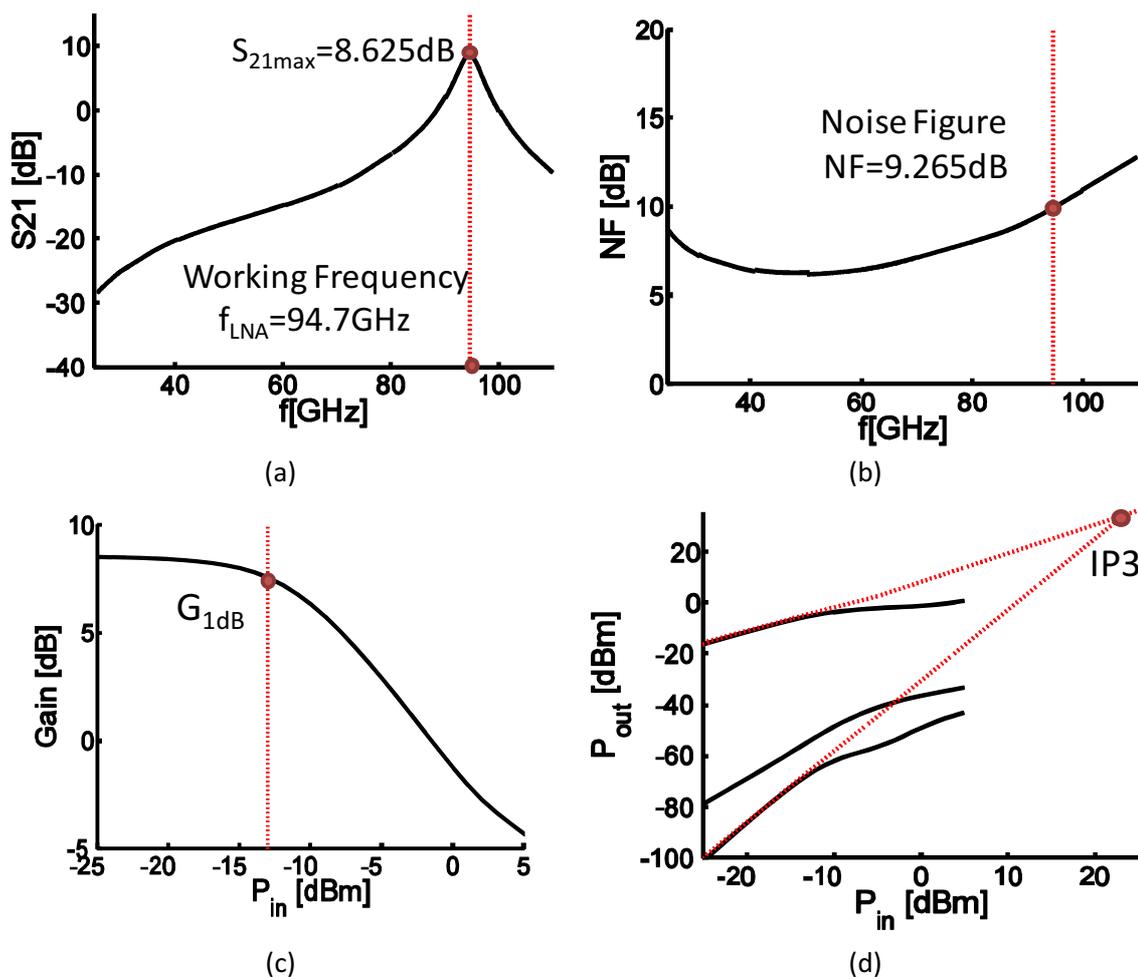


Figure A.8: Investigated LNA was presented [142]. (a) Maximum small signal gain (b) Noise Figure (c) 1dB compression point  $P_{in\_1dB} = -13$  dBm,  $P_{out\_1dB} = -5.43$  dBm (d) 3<sup>rd</sup> order intercept point IIP3=19.86dBm, OIP3=24.78dBm

Parameter	Description	Determination
rsbx	Extrinsic base sheet resistance	PCM based parameter
rea	Emitter sheet resistance	PCM based parameter
rsbl	Buried layer sheet resistance	PCM based parameter
rsbp	Pinch base sheet resistance	PCM based parameter
nepi	Epi layer doping parameter (Variation of SIC doping for BC capacitance variation)	Fitting parameter
nsub	Substrate doping level parameter (for CS capacitance variation)	Fitting parameter
wepi	Thickness of epi layer (for BC capacitance variation)	Fitting parameter
rec	BE saturation current parameter (Base current is monitored and rec is fitted)	Fitting parameter
deg	Impact of bandgap variation on $I_c$ (Collector current is monitored and deg is fitted)	Fitting parameter
irec	BE recombination saturation current parameter (Base current is monitored and irec is fitted)	Fitting parameter
wctf	Tuning parameter for transit time (Monitoring of $f_t$ and wctf is fitted)	Fitting parameter

Table A.1: Investigated process parameter (STMMicroelectronics).

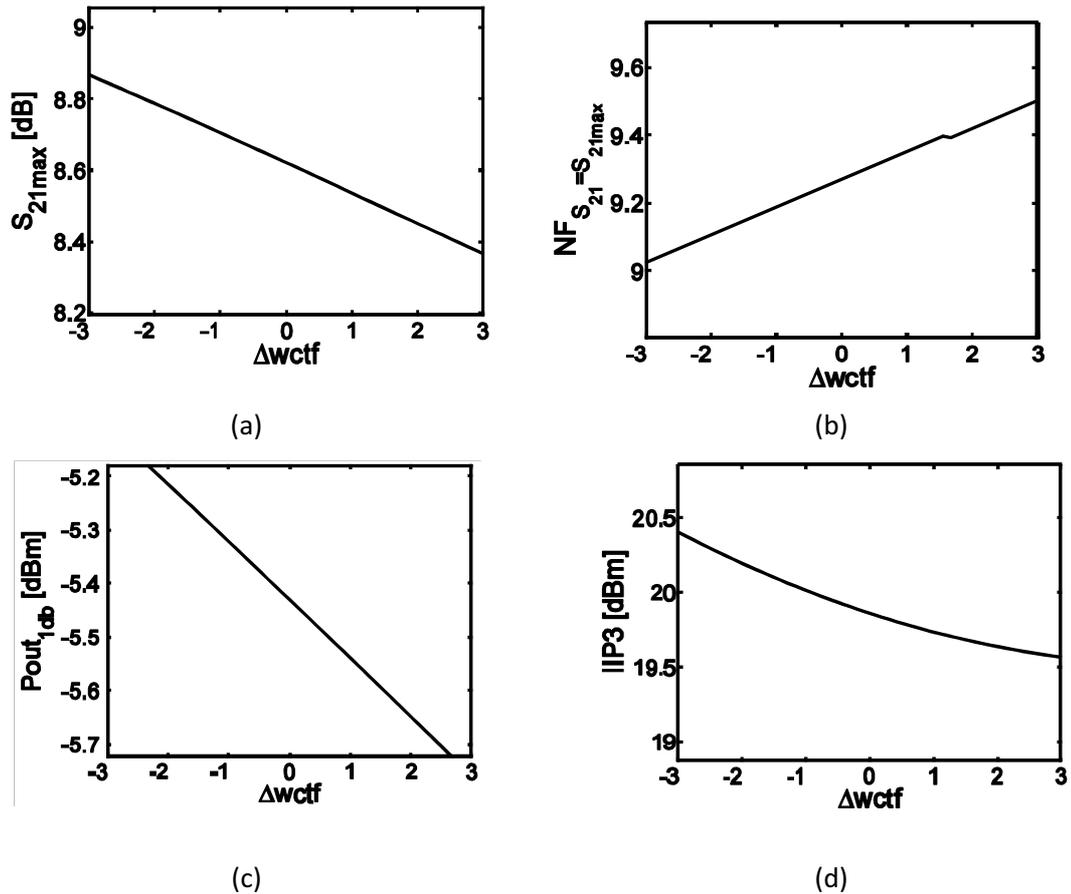


Figure A.9: FoM vs. standard deviation  $\sigma$  of wctf (from  $-3\sigma$  to  $3\sigma$ ): (a) Variation maximum small signal gain  $dS_{21\_max} = \pm 2.94\%$  (b) Variation Noise Figure  $dNF = \pm 2.62\%$  (c) Variation output power at 1dB compression point  $P_{out\_1dB} = \pm 2.36\%$  (d) Variation input power  $IIP3 = \pm 2.09\%$  and output power  $OIP3 = \pm 3.08\%$  at 3<sup>rd</sup> order intercept point  $IIP3 = 19.86\text{dBm}$ ,  $OIP3 = 24.78\text{dBm}$ .

## References

- [1] R. P. Feynman, "There's plenty of room at the bottom [data storage]," *Journal of Microelectromechanical Systems*, vol. 1, no. 1, pp. 60–66, 1992.
- [2] G. E. Moore, "Progress in digital integrated electronics," in *Electron Devices Meeting, 1975 International*, 1975, vol. 21, pp. 11–13.
- [3] M. Lundstrom, "Moore's Law Forever?," *Science*, vol. 299, no. 5604, pp. 210–211, Jan. 2003.
- [4] W. M. Arden, "The International Technology Roadmap for Semiconductors—Perspectives and challenges for the next 15 years," *Current Opinion in Solid State and Materials Science*, vol. 6, no. 5, pp. 371–377, Oct. 2002.
- [5] J. D. Meindl, Q. Chen, and J. A. Davis, "Limits on Silicon Nanoelectronics for Terascale Integration," *Science*, vol. 293, no. 5537, pp. 2044–2049, Sep. 2001.
- [6] P. H. Siegel, "Terahertz technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 910–928, Mar. 2002.
- [7] DOTFIVE, "Towards 0.5 THz Silicon/Germanium Heterojunction Bipolar Technology." [Online]. Available: EUFP7 funded IP, number 216110, <http://www.dotfive.eu/>.
- [8] M. Tonouchi, "Cutting-edge terahertz technology," *Nat Photon*, vol. 1, no. 2, pp. 97–105, Feb. 2007.
- [9] M. Nagel, P. Haring Bolivar, M. Brucherseifer, H. Kurz, A. Bosserhoff, and R. Büttner, "Integrated THz technology for label-free genetic diagnostics," *Appl. Phys. Lett.*, vol. 80, no. 1, p. 154, 2002.
- [10] R. M. Woodward, B. E. Cole, V. P. Wallace, R. J. Pye, D. D. Arnone, E. H. Linfield, and M. Pepper, "Terahertz pulse imaging in reflection geometry of human skin cancer and skin tissue," *Phys. Med. Biol.*, vol. 47, no. 21, pp. 3853–3863, Nov. 2002.
- [11] B. Fischer, M. Hoffmann, H. Helm, R. Wilk, F. Rutz, T. Kleine-Ostmann, M. Koch, and P. Jepsen, "Terahertz time-domain spectroscopy and imaging of artificial RNA," *Opt. Express*, vol. 13, no. 14, pp. 5205–5215, Jul. 2005.
- [12] D. M. Mittleman, J. Cunningham, M. C. Nuss, and M. Geva, "Noncontact semiconductor wafer characterization with the terahertz Hall effect," *Appl. Phys. Lett.*, vol. 71, no. 1, p. 16, 1997.
- [13] Hua Zhong, Jingzhou Xu, Xu Xie, Tao Yuan, R. Reightler, E. Madaras, and Xi-Cheng Zhang, "Nondestructive defect identification with terahertz time-of-flight tomography," *IEEE Sensors Journal*, vol. 5, no. 2, pp. 203–208, Apr. 2005.
- [14] D. L. Woolard, J. O. Jensen, and R. J. Hwu, *Terahertz Science and Technology for Military and Security Applications*. World Scientific, 2007.
- [15] K. Kawase, Y. Ogawa, Y. Watanabe, and H. Inoue, "Non-destructive terahertz imaging of illicit drugs using spectral fingerprints," *Opt Express*, vol. 11, no. 20, pp. 2549–2554, Oct. 2003.

- [16] N. Kukutsu, A. Hirata, M. Yaita, K. Ajito, H. Takahashi, T. Kosugi, H.-J. Song, A. Wakatsuki, Y. Muramoto, T. Nagatsuma, and Y. Kado, "Toward practical applications over 100 GHz," in *Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International*, 2010, pp. 1134–1137.
- [17] Kao-Cheng Huang and Zhaocheng Wang, "Terahertz Terabit Wireless Communication," *IEEE Microwave Magazine*, vol. 12, no. 4, pp. 108–116, Jun. 2011.
- [18] U. R. Pfeiffer and E. Ojefors, "Terahertz imaging with CMOS/BiCMOS process technologies," in *ESSCIRC, 2010 Proceedings of the*, 2010, pp. 52–60.
- [19] R. Piesiewicz, T. Kleine-Ostmann, N. Krumbholz, D. Mittleman, M. Koch, J. Schoebel, and T. Kurner, "Short-Range Ultra-Broadband Terahertz Communications: Concepts and Perspectives," *IEEE Antennas and Propagation Magazine*, vol. 49, no. 6, pp. 24–39, Dec. 2007.
- [20] Eunyoung Seok, Dongha Shim, Chuying Mao, Ruonan Han, S. Sankaran, Changhua Cao, W. Knap, and K. O. Kenneth, "Progress and Challenges Towards Terahertz CMOS Integrated Circuits," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 8, pp. 1554–1564, Aug. 2010.
- [21] J. V. Siles and J. Grajal, "Physics-Based Design and Optimization of Schottky Diode Frequency Multipliers for Terahertz Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 7, pp. 1933–1942, Jul. 2010.
- [22] Q. Hu, B. S. Williams, S. Kumar, H. Callebaut, S. Kohen, and J. L. Reno, "Resonant-phonon-assisted THz quantum-cascade lasers with metal-metal waveguides," *Semicond. Sci. Technol.*, vol. 20, no. 7, pp. S228–S236, Jul. 2005.
- [23] S. Balasekaran, K. Endo, T. Tanabe, and Y. Oyama, "Patch antenna coupled 0.2 THz TUNNETT oscillators," *Solid-State Electronics*, vol. 54, no. 12, pp. 1578–1581, Dec. 2010.
- [24] H. Ito, F. Nakajima, T. Furuta, and T. Ishibashi, "Continuous THz-wave generation using antenna-integrated uni-travelling-carrier photodiodes," *Semicond. Sci. Technol.*, vol. 20, no. 7, pp. S191–S198, Jul. 2005.
- [25] A. Masahiro, S. Safumi, and K. Naomichi, "Resonant Tunneling Diodes for Sub-Terahertz and Terahertz Oscillators," *Jpn J Appl Phys*, vol. 47, no. 6, pp. 4375–4384, Jun. 2008.
- [26] A. J. Miller, "Micromachined antenna-coupled uncooled microbolometers for terahertz imaging arrays," in *Proceedings of SPIE*, Orlando, FL, USA, 2004, pp. 18–24.
- [27] T. Yasui, A. Nishimura, T. Suzuki, K. Nakayama, and S. Okajima, "Detection system operating at up to 7 THz using quasi-optics and Schottky barrier diodes," *Rev. Sci. Instrum.*, vol. 77, no. 6, p. 066102, 2006.
- [28] S. Ariyoshi, C. Otani, A. Dobroiu, H. Sato, K. Kawase, H. M. Shimizu, T. Taino, and H. Matsuo, "Terahertz imaging with a direct detector based on superconducting tunnel junctions," *Appl. Phys. Lett.*, vol. 88, no. 20, p. 203503, 2006.
- [29] T. Al-Attar, A. Hassibi, and T. H. Lee, "A 77GHz monolithic IMPATT transmitter in standard CMOS technology," in *Microwave Symposium Digest, 2005 IEEE MTT-S International*, 2005.

- [30] Jae-Sung Rieh and Dong-Hyun Kim, "An Overview of Semiconductor Technologies and Circuits for Terahertz Communication Applications," in *2009 IEEE GLOBECOM Workshops*, 2009, pp. 1–6.
- [31] P. M. Schroter and A. Chakravorty, *Compact Hierarchical Bipolar Transistor Modeling With Hicup*. World Scientific, 2010.
- [32] H. K. Gummel, "On the definition of the cutoff frequency  $f_T$ ," *Proceedings of the IEEE*, vol. 57, no. 12, pp. 2159–2159, 1969.
- [33] M. S. Gupta, "Power gain in feedback amplifiers, a classic revisited," *IEEE Transactions on Microwave Theory and Techniques*, vol. 40, no. 5, pp. 864–879, May 1992.
- [34] Sungjae Lee, B. Jagannathan, S. Narasimha, A. Chou, N. Zamdmer, J. Johnson, R. Williams, L. Wagner, Jonghae Kim, J.-O. Plouchart, J. Pekarik, S. Springer, and G. Freeman, "Record RF performance of 45-nm SOI CMOS Technology," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 255–258.
- [35] B. Geynet, P. Chevalier, B. Vandelle, F. Brossard, N. Zerounian, M. Buczeko, D. Gloria, F. Aniel, G. Dambrine, F. Danneville, D. Dutartre, and A. Chantre, "SiGe HBTs featuring  $f_T \gg 400\text{GHz}$  at room temperature," in *IEEE Bipolar/BiCMOS Circuits and Technology Meeting, 2008. BCTM 2008*, 2008, pp. 121–124.
- [36] Dae-Hyun Kim and J. A. del Alamo, "30-nm InAs PHEMTs with  $f_T = 644\text{ GHz}$  and  $f_{\text{max}} = 681\text{ GHz}$ ," *IEEE Electron Device Letters*, vol. 31, no. 8, pp. 806–808, Aug. 2010.
- [37] W. Snodgrass, W. Hafez, N. Harff, and M. Feng, "Pseudomorphic InP/InGaAs Heterojunction Bipolar Transistors (PHBTs) Experimentally Demonstrating  $f_T = 765\text{ GHz}$  at  $25^\circ\text{C}$  Increasing to  $f_T = 845\text{ GHz}$  at  $-55^\circ\text{C}$ ," in *Electron Devices Meeting, 2006. IEDM '06. International*, 2006, pp. 1–4.
- [38] C.-H. Jan, P. Bai, S. Biswas, M. Buehler, Z.-P. Chen, G. Curello, S. Gannavaram, W. Hafez, J. He, J. Hicks, U. Jalan, N. Lazo, J. Lin, N. Lindert, C. Litteken, M. Jones, M. Kang, K. Komeyli, A. Mezhiba, S. Naskar, S. Olson, J. Park, R. Parker, L. Pei, I. Post, N. Pradhan, C. Prasad, M. Prince, J. Rizk, G. Sacks, H. Tashiro, D. Towner, C. Tsai, Y. Wang, L. Yang, J.-Y. Yeh, J. Yip, and K. Mistry, "A 45nm low power system-on-chip technology with dual gate (logic and I/O) high-k/metal gate strained silicon transistors," in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, 2008, pp. 1–4.
- [39] B. Heinemann, R. Barth, D. Bolze, J. Drews, G. G. Fischer, A. Fox, O. Fursenko, T. Grabolla, U. Haak, D. Knoll, R. Kurps, M. Lisker, S. Marschmeyer, H. Rücker, D. Schmidt, J. Schmidt, M. A. Schubert, B. Tillack, C. Wipf, D. Wolansky, and Y. Yamamoto, "SiGe HBT technology with  $f_T/f_{\text{max}}$  of  $300\text{GHz}/500\text{GHz}$  and  $2.0\text{ ps}$  CML gate delay," in *Electron Devices Meeting (IEDM), 2010 IEEE International*, 2010, pp. 30.5.1–30.5.4.
- [40] R. Lai, X. B. Mei, W. R. Deal, W. Yoshida, Y. M. Kim, P. H. Liu, J. Lee, J. Uyeda, V. Radisic, M. Lange, T. Gaier, L. Samoska, and A. Fung, "Sub 50 nm InP HEMT Device with  $f_{\text{max}}$  Greater than  $1\text{ THz}$ ," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 609–611.
- [41] V. Jain, E. Lobisser, A. Baraskar, B. J. Thibeault, M. J. Rodwell, Z. Griffith, M. Urteaga, D. Loubychev, A. Snyder, Y. Wu, J. M. Fastenau, and W. K. Liu,

- “InGaAs/InP DHBTs in a Dry-Etched Refractory Metal Emitter Process Demonstrating Simultaneous  $f_T/f_{max} \sim 430/800$  GHz,” *IEEE Electron Device Letters*, vol. 32, no. 1, pp. 24–26, Jan. 2011.
- [42] J.-S. Rieh, Y. Oh, D. Yoon, N. Kim, D.-H. Kim, J. Yun, H. Kim, and K. Song, “An overview of challenges and current status of Si-based terahertz monolithic integrated circuits,” in *2012 IEEE 11th International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, 2012, pp. 1–4.
- [43] G.-B. Gao, M.-Z. Wang, X. Gui, and H. Morkoc, “Thermal design studies of high-power heterojunction bipolar transistors,” *IEEE Transactions on Electron Devices*, vol. 36, no. 5, pp. 854–863, 1989.
- [44] H. Rücker, B. Heinemann, and A. Fox, “SiGe BiCMOS Technologies for Applications above 100 GHz,” in *2012 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2012, pp. 1–4.
- [45] P. Chevalier, T. Lacave, E. Canderle, A. Pottrain, Y. Carminati, J. Rosa, F. Pourchon, N. Derrier, G. Avenier, A. Montagne, A. Balteanu, E. Dacquay, I. Sarkas, D. Celi, D. Gloria, C. Gaquiere, S. P. Voinigescu, and A. Chantre, “Scaling of SiGe BiCMOS Technologies for Applications above 100 GHz,” in *2012 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Oct., pp. 1–4.
- [46] E. Ojefors, J. Grzyb, Yan Zhao, B. Heinemann, B. Tillack, and U. R. Pfeiffer, “A 820GHz SiGe chipset for terahertz active imaging applications,” in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International*, 2011, pp. 224–226.
- [47] M. I. Dyakonov and M. S. Shur, “Plasma wave electronics: novel terahertz devices using two dimensional electron fluid,” *IEEE Transactions on Electron Devices*, vol. 43, no. 10, pp. 1640–1645, Oct. 1996.
- [48] D. Hame, A. Joseph, P. Cheng, V. Jain, and R. Camillo-Castillo, “(Keynote) History and Future Directions in SiGe HBT BiCMOS Technology and Its Applications,” *ECS Trans.*, vol. 49, no. 1, pp. 3–14, Aug. 2012.
- [49] A. Pottrain, T. Lacave, D. Ducatteau, D. Gloria, P. Chevalier, and C. Gaquiere, “High Power Density Performances of SiGe HBT From BiCMOS Technology at W-Band,” *Electron Device Letters, IEEE*, vol. 33, no. 2, pp. 182–184, Feb. 2012.
- [50] S. P. Voinigescu, A. Tomkins, E. Dacquay, P. Chevalier, J. Hasch, A. Chantre, and B. Sautreuil, “A Study of SiGe HBT Signal Sources in the 220-330-GHz Range,” *IEEE Journal of Solid-State Circuits*, vol. Early Access Online, 2013.
- [51] M. Weis, C. Majek, A. K. Sahoo, C. Maneux, O. Mazouffre, P. Chevalier, A. Chantre, and T. Zimmer, “Optimized Ring Oscillator With 1.65-ps Gate Delay in a SiGe:C HBT Technology,” *IEEE Electron Device Letters*, vol. 34, no. 10, pp. 1214–1216, Oct. 2013.
- [52] U. R. Pfeiffer, E. Ojefors, A. Lisauskas, and H. G. Roskos, “Opportunities for silicon at mmWave and Terahertz frequencies,” in *2008 IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Monterey, CA, 2008, pp. 149–156.
- [53] E. Johnson, “Physical limitations on frequency and power parameters of transistors,” in *IRE International Convention Record*, 1965, vol. 13, pp. 27–34.

- [54] S. P. Gaur, "Performance limitations of silicon bipolar transistors," *IEEE Journal of Solid-State Circuits*, vol. 14, no. 2, pp. 337–343, 1979.
- [55] M. Schroter, G. Wedel, B. Heinemann, C. Jungemann, J. Krause, P. Chevalier, and A. Chantre, "Physical and Electrical Performance Limits of High-Speed SiGeC HBTs - Part I: Vertical Scaling," *IEEE Transactions on Electron Devices*, vol. 58, no. 11, pp. 3687–3696, Nov. 2011.
- [56] M. Schroter, J. Krause, N. Rinaldi, G. Wedel, B. Heinemann, P. Chevalier, and A. Chantre, "Physical and Electrical Performance Limits of High-Speed Si GeC HBTs - Part II: Lateral Scaling," *IEEE Transactions on Electron Devices*, vol. 58, no. 11, pp. 3697–3706, Nov. 2011.
- [57] L. L. Liou and B. Bayraktaroglu, "Thermal stability analysis of AlGaAs/GaAs heterojunction bipolar transistors with multiple emitter fingers," *IEEE Transactions on Electron Devices*, vol. 41, no. 5, pp. 629–636, May.
- [58] K. Puttaswamy and G. H. Loh, "Thermal Herding: Microarchitecture Techniques for Controlling Hotspots in High-Performance 3D-Integrated Processors," in *IEEE 13th International Symposium on High Performance Computer Architecture, 2007. HPCA 2007*, Feb., pp. 193–204.
- [59] A. Chantre, P. Chevalier, T. Lacave, G. Avenier, M. Buczko, Y. Campidelli, L. Depoyan, L. Berthier, and C. Gacquièr, "Pushing conventional SiGe HBT technology towards 'Dotfive' terahertz," in *Microwave Integrated Circuits Conference (EuMIC), 2010 European*, 2010, pp. 21–24.
- [60] P. Chevalier, T. F. Meister, B. Heinemann, S. Van Huylbroeck, W. Liebl, A. Fox, A. Sibaja-Hernandez, and A. Chantre, "Towards THz SiGe HBTs," in *Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), 2011 IEEE*, 2011, pp. 57–65.
- [61] D. Vasileska, K. Raleva, and S. M. Goodnick, "Modeling heating effects in nanoscale devices: the present and the future," *J Comput Electron*, vol. 7, no. 2, pp. 66–93, Jun. 2008.
- [62] D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbe, J. Y.-C. Sun, B. S. Meyerson, and T. Tice, "Si/SiGe epitaxial-base transistors. I. Materials, physics, and circuits," *IEEE Transactions on Electron Devices*, vol. 42, no. 3, pp. 455–468, 1995.
- [63] D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbe, J. Y.-C. Sun, B. S. Meyerson, and T. Tice, "Si/SiGe epitaxial-base transistors. II. Process integration and analog applications," *IEEE Transactions on Electron Devices*, vol. 42, no. 3, pp. 469–482, 1995.
- [64] D. J. Walkey, T. J. Smy, C. Reimer, M. Schröter, H. Tran, and David Marchesan, "Modeling thermal resistance in trench-isolated bipolar technologies including trench heat flow," *Solid-State Electronics*, vol. 46, no. 1, pp. 7–17, Jan. 2002.
- [65] I. Marano, V. d' Alessandro, and N. Rinaldi, "Effectively modeling the thermal behavior of trench-isolated bipolar transistors," in *EuroSimE 2008 - International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Micro-Systems*, Freiburg im Breisgau, Germany, 2008, pp. 1–8.
- [66] J.-S. Rieh, J. Johnson, S. Furkay, D. Greenberg, G. Freeman, and S. Subbanna, "Structural dependence of the thermal resistance of trench-isolated bipolar transis-

- tors,” in *Bipolar/BiCMOS Circuits and Technology Meeting, 2002. Proceedings of the 2002*, 2002, pp. 100–103.
- [67] G. Freeman, J.-S. Rieh, Z. Yang, and F. Guarin, “Reliability and performance scaling of very high speed SiGe HBTs,” *Microelectronics Reliability*, vol. 44, no. 3, pp. 397–410, Mar. 2004.
- [68] R. H. Winkler, “Thermal properties of high-power transistors,” *IEEE Transactions on Electron Devices*, vol. 14, no. 5, pp. 260–263, May.
- [69] W. Liu, “Thermal coupling in 2-finger heterojunction bipolar transistors,” *IEEE Transactions on Electron Devices*, vol. 42, no. 6, pp. 1033–1038, Jun. 1995.
- [70] E. K. Mueller, “Internal thermal feedback in four-poles especially in transistors,” *Proceedings of the IEEE*, vol. 52, no. 8, pp. 924–930, 1964.
- [71] M. Reisch, *Halbleiter-Bauelemente*. Springer DE, 2007.
- [72] J. Andrews, C. Grens, and J. D. Cressler, “The effects of layout variation on the thermal characteristics of SiGe HBTs,” in *Bipolar/BiCMOS Circuits and Technology Meeting, 2005. Proceedings of the*, Oct., pp. 50–53.
- [73] A. Pawlak, M. Schroter, J. Krause, D. Céli, and N. Derrier, “HICUM/2 v2.3 Parameter Extraction for Advanced SiGe-Heterojunction Bipolar Transistors,” in *Bipolar/BiCMOS Circuits and Technology Meeting, 2011. Proceedings of the*, 2011, pp. 1–4.
- [74] RF2THz SiSoC, “From Radio Frequency to Millimeter Wave and THz Silicon System-On-Chip Technologies.” [Online]. Available: CATRENE UREKA Cluster, CT209, [http://www.catrene.org/web/projects/project\\_list.php](http://www.catrene.org/web/projects/project_list.php).
- [75] DOTSEVEN, “Towards 0.7 THz Silicon/Germanium Heterojunction Bipolar Technology.” [Online]. Available: EUFP7 funded IP, number 316755, <http://www.dotseven.eu/>.
- [76] G. Avenier, M. Diop, P. Chevalier, G. Troillard, N. Loubet, J. Bouvier, L. Depoyan, N. Derrier, M. Buczko, C. Leyris, S. Boret, S. Montusclat, A. Margain, S. Pruvost, S. T. Nicolson, K. H. . Yau, N. Revil, D. Gloria, D. Dutartre, S. P. Voinigescu, and A. Chantre, “0.13  $\mu\text{m}$  SiGe BiCMOS Technology Fully Dedicated to mm-Wave Applications,” *IEEE Journal of Solid-State Circuits*, vol. 44, no. 9, pp. 2312–2321, Sep. 2009.
- [77] P. Chevalier, F. Pourchon, T. Lacave, G. Avenier, Y. Campidelli, L. Depoyan, G. Troillard, M. Buczko, D. Gloria, D. Celi, C. Gaquiere, and A. Chantre, “A conventional double-polysilicon FSA-SEG Si/SiGe:C HBT reaching 400 GHz fMAX,” in *IEEE Bipolar/BiCMOS Circuits and Technology Meeting, 2009. BCTM 2009*, 2009, pp. 1–4.
- [78] “Compact Model Council (CMC) Webpage.” [Online]. Available: <http://www.si2.org/>.
- [79] M. Schroter and A. HICUM, “Scalable Physics-Based Compact Bipolar Transistor Model,” Available on the web: [http://www.iee.et.tu-dresden.de/iee/eb/comp\\_mod.html](http://www.iee.et.tu-dresden.de/iee/eb/comp_mod.html), *consulta*, vol. 25, no. 10, 2004.
- [80] M. Schroter, M. Friedrich, and H.-M. Rein, “A generalized integral charge-control relation and its application to compact models for silicon-based HBT’s,” *IEEE Transactions on Electron Devices*, vol. 40, no. 11, pp. 2036–2046, Nov.

- [81] Julia Krause, “Modellierung von Bipolartransistoren für Leistungsverstärker in HF-Anwendungen,” Chair for Electron Devices and Integrated Circuits, TU Dresden, Germany, 2008.
- [82] A. K. Sahoo, “Electro-thermal Characterizations, Compact Modeling and TCAD based Device Simulations of advanced SiGe: C BiCMOS HBTs and of nanometric CMOS FET,” Bordeaux 1, 2012.
- [83] P. Aaen, J. A. Plá, and J. Wood, *Modeling and Characterization of RF and Microwave Power FETs*. Cambridge University Press, 2007.
- [84] G. F. Engen and R. W. Beatty, “Microwave Reflectometer Techniques,” *IRE Transactions on Microwave Theory and Techniques*, vol. 7, no. 3, pp. 351–355, 1959.
- [85] J. Cusack, S. Perlow, and B. Perlman, “Automatic Load Contour Mapping for Microwave Power Transistors,” in *Microwave Symposium Digest, 1974 S-MTT International*, 1974, vol. 74, pp. 269–271.
- [86] M. Paggi, P. H. Williams, and J. M. Borrego, “Nonlinear GaAs MESFET modeling using pulsed gate measurements,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 12, pp. 1593–1597, 1988.
- [87] J. F. Vidalou, J. F. Grossier, M. Chaumas, M. Camiade, P. Roux, and J. Obregon, “Accurate nonlinear transistor modeling using pulsed S parameters measurements under pulsed bias conditions,” in *Microwave Symposium Digest, 1991., IEEE MTT-S International*, 1991, pp. 95–98 vol.1.
- [88] F. van Raay and G. Kompa, “A new on-wafer large-signal waveform measurement system with 40 GHz harmonic bandwidth,” in *Microwave Symposium Digest, 1992., IEEE MTT-S International*, 1992, pp. 1435–1438 vol.3.
- [89] S. P. Voinigescu, E. Dacquay, V. Adinolfi, I. Sarkas, A. Balteanu, A. Tomkins, D. Celi, and P. Chevalier, “Characterization and Modeling of an SiGe HBT Technology for Transceiver Applications in the 100-300-GHz Range,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 12, pp. 4024–4034, 2012.
- [90] E. Canderle, P. Chevalier, A. Montagne, L. Moynet, G. Avenier, P. Boulenc, M. Buczko, Y. Carminati, J. Rosa, C. Gaquiere, and A. Chantre, “Extrinsic base resistance optimization in DPSA-SEG SiGe:C HBTs,” in *2012 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2012, pp. 1–4.
- [91] H. Tran, M. Schroter, D. J. Walkey, D. Marchesan, and T. J. Smy, “Simultaneous extraction of thermal and emitter series resistances in bipolar transistors,” in *Proceedings of the 1997 Bipolar/BiCMOS Circuits and Technology Meeting*, Minneapolis, MN, USA, pp. 170–173.
- [92] J.-S. Rieh, D. Greenberg, B. Jagannathan, G. Freeman, and S. Subbanna, “Measurement and modeling of thermal resistance of high speed SiGe heterojunction bipolar transistors,” in *2001 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems. Digest of Papers (IEEE Cat. No.01EX496)*, Ann Arbor, MI, USA, pp. 110–113.
- [93] R. Menozzi, J. Barrett, and P. Ersland, “A new method to extract HBT thermal resistance and its temperature and power dependence,” *IEEE Transactions on Device and Materials Reliability*, vol. 5, no. 3, pp. 595 – 601, Sep. 2005.

- [94] Joy, R.C. and Schlig, E.S., "Thermal properties of very fast transistors," *IEEE Transactions on Electron Devices*, vol. 17, no. 8, pp. 586–594, Aug. 1970.
- [95] R. M. Fox and S.-G. Lee, "Predictive modeling of thermal effects in BJTs," in *Bipolar Circuits and Technology Meeting, 1991., Proceedings of the 1991*, Sep, pp. 89–92.
- [96] D. T. Zweidinger, R. M. Fox, J. S. Brodsky, T. Jung, and S.-G. Lee, "Thermal impedance extraction for bipolar transistors," *IEEE Transactions on Electron Devices*, vol. 43, no. 2, pp. 342–346, Feb.
- [97] D. J. Walkey, T. J. Smy, D. Marchesan, Hai Tran, C. Reimer, T. C. Kleckner, M. K. Jackson, M. Schroter, and J. R. Long, "Extraction and modelling of thermal behavior in trench isolated bipolar structures," in *Proceedings of the 1999 Bipolar/BiCMOS Circuits and Technology Meeting*, Minneapolis, MN, USA, 1999, pp. 97–100.
- [98] C. Anghel, R. Gillon, and A.-M. Ionescu, "Self-heating characterization and extraction method for thermal resistance and capacitance in HV MOSFETs," *IEEE Electron Device Letters*, vol. 25, no. 3, pp. 141–143, 2004.
- [99] A. El-Rafei, A. Saleh, R. Sommet, J. M. Nebus, and R. Quere, "Experimental Characterization and Modeling of the Thermal Behavior of SiGe HBTs," *IEEE Transactions on Electron Devices*, vol. 59, no. 7, pp. 1921–1927, 2012.
- [100] A. K. Sahoo, S. Fregonese, M. Weiß, B. Grandchamp, N. Malbert, and T. Zimmer, "Characterization of self-heating in Si-Ge HBTs with pulse, DC and AC measurements," *Solid-State Electronics*, vol. 76, pp. 13–18, Oct. 2012.
- [101] O. Sevimli, A. E. Parker, A. P. Fattorini, and S. J. Mahon, "Measurement and Modeling of Thermal Behavior in InGaP/GaAs HBTs," *IEEE Transactions on Electron Devices*, vol. 60, no. 5, pp. 1632–1639, 2013.
- [102] D. A. Frickey, "Conversions between S, Z, Y, H, ABCD, and T parameters which are valid for complex source and load impedances," *IEEE Transactions on Microwave Theory and Techniques*, vol. 42, no. 2, pp. 205–211, 1994.
- [103] S. Bruce, A. Trasser, M. Birk, A. Rydberg, and H. Schumacher, "Extraction of thermal time constant in HBTs using small signal measurements," *Electronics Letters*, vol. 33, no. 2, pp. 165–167, 1997.
- [104] A. K. Sahoo, S. Fregonese, M. Weiss, N. Malbert, and T. Zimmer, "Electro-thermal characterization of Si-Ge HBTs with pulse measurement and transient simulation," in *Solid-State Device Research Conference (ESSDERC), 2011 Proceedings of the European*, 2011, pp. 239–242.
- [105] B. Schaefer and M. Dunn, "Pulsed measurements and modeling for electro-thermal effects," in *Bipolar/BiCMOS Circuits and Technology Meeting, 1996., Proceedings of the 1996*, 1996, pp. 110–117.
- [106] J.-P. Teyssier, P. Bouysse, Z. Ouarch, D. Barataud, T. Peyretailade, and R. Quere, "40-GHz/150-ns versatile pulsed measurement system for microwave transistor isothermal characterization," *IEEE Trans. Microwave Theory Techn.*, vol. 46, no. 12, pp. 2043–2052, Dec. 1998.
- [107] A. Saleh, M. A. Chahine, T. Reveyrand, G. Neveux, D. Barataud, J. M. Nebus, R. Quere, Y. Bouvier, J. Godin, and M. Riet, "40 ns pulsed I/V set-up and measurement method applied to InP HBT characterization and electro-thermal modeling,"

- in *2009 IEEE Radio Frequency Integrated Circuits Symposium*, Boston, MA, USA, 2009, pp. 401–404.
- [108] M. Rickelt, H.-M. Rein, and E. Rose, “Influence of impact-ionization-induced instabilities on the maximum usable output voltage of Si-bipolar transistors,” *IEEE Transactions on Electron Devices*, vol. 48, no. 4, pp. 774–783, avril 2001.
- [109] A. K. Sahoo, S. Fregonese, M. Weiss, N. Malbert, and T. Zimmer, “Electro-thermal dynamic simulation and thermal spreading impedance modeling of Si-Ge HBTs,” in *2011 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2011, pp. 45–48.
- [110] A. E. Parker and J. G. Rathmell, “Broad-band characterization of FET self-heating,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 7, pp. 2424–2429, Jul. 2005.
- [111] J. H. K. Vuolevi, T. Rahkonen, and J. P. A. Manninen, “Measurement technique for characterizing memory effects in RF power amplifiers,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 8, pp. 1383–1389, 2001.
- [112] A. K. Sahoo, S. Fregonese, M. Weis, N. Malbert, and T. Zimmer, “A Scalable Electrothermal Model for Transient Self-Heating Effects in Trench-Isolated SiGe HBTs,” *IEEE Transactions on Electron Devices*, vol. 59, no. 10, pp. 2619–2625, Oct. 2012.
- [113] J. M. Andrews, C. M. Grens, and J. D. Cressler, “Compact Modeling of Mutual Thermal Coupling for the Optimal Design of SiGe HBT Power Amplifiers,” *IEEE Transactions on Electron Devices*, vol. 56, no. 7, pp. 1529–1532, Jul. 2009.
- [114] C. J. Glassbrenner and G. A. Slack, “Thermal Conductivity of Silicon and Germanium from 3°K to the Melting Point,” *Phys. Rev.*, vol. 134, no. 4A, p. A1058, May 1964.
- [115] Synopsys Inc., “TCAD Sentaurus User Guide E-2010.12.” 30-Dec-2010.
- [116] D. J. Walkey, T. J. Smy, R. G. Dickson, J. S. Brodsky, D. T. Zweidinger, and R. M. Fox, “Equivalent circuit modeling of static substrate thermal coupling using VCVS representation,” *IEEE J. Solid-State Circuits*, vol. 2, no. 9, pp. 1198–1206, Sep. 2002.
- [117] K. Fukahori and P. R. Gray, “Computer simulation of integrated circuits in the presence of electrothermal interaction,” *Solid-State Circuits, IEEE Journal of*, vol. 11, no. 6, pp. 834–846, Dec. 1976.
- [118] M. Pedram and S. Nazarian, “Thermal Modeling, Analysis, and Management in VLSI Circuits: Principles and Methods,” *Proceedings of the IEEE*, vol. 94, no. 8, pp. 1487–1501, Aug. 2006.
- [119] M. Sokolich, A. R. Kramer, Y. K. Boegeman, and R. R. Martinez, “Demonstration of sub-5 ps CML ring oscillator gate delay with reduced parasitic AlInAs/InGaAs HBT,” *IEEE Electron Device Letters*, vol. 22, no. 7, pp. 309–311, Jul. 2001.
- [120] B. Jagannathan, M. Meghelli, A. V. Rylyakov, R. A. Groves, A. K. Chinthakindi, C. M. Schnabel, D. A. Ahlgren, G. G. Freeman, K. J. Stein, and S. Subbanna, “A 4.2-ps ECL ring-oscillator in a 285-GHz fMAX SiGe technology,” *IEEE Electron Device Letters*, vol. 23, no. 9, pp. 541–543, Sep. 2002.

- [121] H. Rücker, B. Heinemann, W. Winkler, R. Barth, J. Borngraber, J. Drews, G. G. Fischer, A. Fox, T. Grabolla, U. Haak, D. Knoll, F. Korndörfer, A. Mai, S. Marschmeyer, P. Schley, D. Schmidt, J. Schmidt, M. A. Schubert, K. Schulz, B. Tillack, D. Wolansky, and Y. Yamamoto, "A 0.13 $\mu$ m SiGe BiCMOS Technology Featuring fT/fMAX of 240/330 GHz and Gate Delays Below 3 ps," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1678–1686, Sep. 2010.
- [122] M. Weiß, A. K. Sahoo, C. Maneux, and T. Zimmer, "Rigorous investigations of a SiGe:C BiCMOS ring oscillator with optimized gate delay," in *Microwave Conference (GeMiC), 2012 The 7th German*, 2012.
- [123] A. Fox, B. Heinemann, R. Barth, S. Marschmeyer, C. Wipf, and Y. Yamamoto, "SiGe:C HBT architecture with epitaxial external base," in *2011 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2011, pp. 70–73.
- [124] V. N. Hoang, G. Doornbos, J. Michelon, A. Kumar, A. Nackaerts, and P. Christie, "Balancing Resistance and Capacitance of Signal Interconnects for Power Saving," in *International Interconnect Technology Conference, IEEE 2007*, 2007, pp. 126–128.
- [125] M. Alioto and G. Palumbo, *Model and design of bipolar and MOS current-mode logic: CML, ECL and SCL digital circuits*. Springer, 2005.
- [126] M. Alioto and G. Palumbo, "Oscillation frequency in CML and ESCL ring oscillators," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 48, no. 2, pp. 210–214, Feb. 2001.
- [127] M. Alioto and G. Palumbo, "Highly accurate and simple models for CML and ECL gates," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 18, no. 9, pp. 1369–1375, Sep. 1999.
- [128] N. Rinaldi, "Thermal analysis of solid-state devices and circuits: An analytical approach," *Solid-State Electronics*, vol. 44, no. 10, pp. 1789–1798, 2000.
- [129] M. Weis, M. Santorelli, S. Ghosh, P. Chevalier, A. Chantre, A. K. Sahoo, C. Maneux, and T. Zimmer, "Characterization of mutual heating inside a SiGe ring oscillator," in *2012 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2012.
- [130] B. Leite, E. Kerherve, J.-B. Begueret, and D. Belot, "An Analytical Broadband Model for Millimeter-Wave Transformers in Silicon Technologies," *IEEE Transactions on Electron Devices*, vol. 59, no. 3, pp. 582–589, 2012.
- [131] F. Grover, *Inductance calculations*. Courier Dover Publications, 2004.
- [132] M. Wurzer, T. F. Meister, H. Schafer, H. Knapp, J. Bock, R. Stengl, K. Aufinger, M. Franosch, M. Rest, M. Moller, H.-M. Rein, and A. Felder, "42 GHz static frequency divider in a Si/SiGe bipolar technology," in *Solid-State Circuits Conference, 1997. Digest of Technical Papers. 43rd ISSCC., 1997 IEEE International*, Feb, pp. 122–123.
- [133] J. Altet, W. Claeys, S. Dilhaire, and A. Rubio, "Dynamic Surface Temperature Measurements in ICs," *Proceedings of the IEEE*, vol. 94, no. 8, pp. 1519–1533, 2006.
- [134] J. P. M. Brito and A. Rabaeijs, "CMOS Smart Temperature Sensors for RFID Applications," in *2012 26th Symposium on Integrated Circuits and Systems Design (SBCCI)*, Curitiba, Brazil, 2013.

- 
- [135] S. A. Maas, *Nonlinear Microwave and Rf Circuits*. Artech House, 2003.
- [136] M. De Matos, E. Kerherve, H. Lapuyade, J.-B. Begueret, and Y. Deval, "Millimeter-wave and power characterization for integrated circuits," in *EAAEIE Annual Conference, 2009*, 2009, pp. 1–4.
- [137] N. Nenadovic, S. Mijalkovic, L. K. Nanver, L. K. J. Vandamme, V. d' Alessandro, H. Schellevis, and J. W. Slotboom, "Extraction and modeling of self-heating and mutual thermal coupling impedance of bipolar transistors," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 10, pp. 1764–1772, Oct. 2004.
- [138] C.-W. Kim, N. Goto, and K. Honjo, "Thermal behavior depending on emitter finger and substrate configurations in power heterojunction bipolar transistors," *IEEE Transactions on Electron Devices*, vol. 45, no. 6, pp. 1190–1195, 1998.
- [139] P. R. Gray, D. J. Hamilton, and D. Lieux, "Analysis and design of temperature stabilized substrate integrated circuits," *IEEE Journal of Solid-State Circuits*, vol. 9, no. 2, pp. 61–69, 1974.
- [140] M. H. Nagel, M. J. Fonderie, G. C. M. Meijer, and J. H. Huijsing, "Integrated 1 V thermal shutdown circuit," *Electronics Letters*, vol. 28, no. 10, p. 969, 1992.
- [141] S. Lehmann, M. Weiss, Y. Zimmermann, A. Pawlak, K. Aufinger, and M. Schroter, "Scalable compact modeling for SiGe HBTs suitable for microwave radar applications," in *2011 IEEE 11th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, 2011, pp. 113–116.
- [142] R. R. Severino, J. B. Begueret, D. Belot, Y. Deval, and T. Taris, "A SiGe:C BiCMOS LNA for 94GHz band applications," presented at the BCTM, 2010.



## List of Publications

### International Journals

1. A. K. Sahoo, **M. Weiß**, S. Fregonese, N. Malbert, and T. Zimmer, “Transient electro-thermal characterization of Si–Ge heterojunction bipolar transistors,” *Solid-State Electronics*, vol. 74, pp. 77–84, Aug. 2012.
2. A. K. Sahoo, S. Fregonese, **M. Weiß**, B. Grandchamp, N. Malbert, and T. Zimmer, “Characterization of self-heating in Si–Ge HBTs with pulse, DC and AC measurements,” *Solid-State Electronics*, vol. 76, pp. 13–18, Oct. 2012.
3. A. K. Sahoo, S. Fregonese, **M. Weiß**, N. Malbert, T. Zimmer, “A Scalable Electrothermal Model for Transient Self-Heating Effects in Trench-Isolated SiGe HBTs”, *IEEE Transactions on Electron Devices*, vol. 59, pp. 2619 – 2625, Oct. 2012.
4. **M. Weiß**, S. Fregonese, M. Santorelli, A. K. Sahoo, C. Maneux, and Thomas Zimmer, “Pulsed I (V)—pulsed RF measurement system for microwave device characterization with 80ns/45GHz”, *Solid-State Electronics*, vol. 84, pp. 74-82, June 2013.
5. **M. Weiß**, C. Majek, A. K. Sahoo, C. Maneux, O. Mazouffre, P. Chevalier, A. Chantre, T. Zimmer, “Optimized Ring Oscillator With 1.65-ps Gate Delay in a SiGe:C HBT Technology”, *IEEE Electron Device Letters*, vol. 34, pp. 1214-1216, Oct. 2013.

### International Conferences

1. S Lehmann, **M Weiß**, Y Zimmermann, A Pawlak, K Aufinger, M Schroter, “Scalable compact modeling for SiGe HBTs suitable for microwave radar applications,” *IEEE 11th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, Jan. 2011, Phoenix, Arizona, USA.
2. A. K. Sahoo, S. Fregonese, **M. Weiß**, N. Malbert, and T. Zimmer, “Electro-thermal characterization of Si-Ge HBTs with pulse measurement and transient simulation,” in *European Solid-State Device Research Conference (ESSDERC)*, Sept. 2011, Helsinki Finland.
3. A. K. Sahoo, S. Fregonese, **M. Weiß**, N. Malbert, and T. Zimmer, “Electro-thermal dynamic simulation and thermal spreading impedance modeling of Si-Ge HBTs,” in *2011 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Oct. 2011, Atlanta, Georgia, USA.

4. **M. Weiß**, A. K. Sahoo, C. Maneux, and T. Zimmer, "Rigorous investigations of a SiGe:C BiCMOS ring oscillator with optimized gate delay," in German Microwave Conference (GeMiC), March 2012, Ilmenau, Germany.
5. **M. Weiß**, S. Fregonese, M. Santorelli, A. K. Sahoo, C. Maneux and T. Zimmer, "Pulsed I(V) - pulsed RF measurement system for microwave device characterization with 80ns/45GHz", in Solid-State Device Research Conference (ESSDERC), Sept. 2012, Bordeaux, France.
6. **M. Weiß**, M. Santorelli, S. Ghosh, P. Chevalier, A. Chantre, A. K. Sahoo, C. Maneux and T. Zimmer, "Characterization of Mutual Heating inside a SiGe Ring Oscillator," in IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), Oct. 2012, Portland, Oregon, USA.
7. **M. Weiß**, A. K. Sahoo, C. Raya, S. Ghosh, M. Santorelli, S. Fregonese, C. Maneux and T. Zimmer, "Characterization of intra-device mutual thermal coupling in multi finger SiGe: C HBTs," in IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC), June 2013, Hong Kong.
8. **M. Weiß**, A. K. Sahoo, C. Maneux and T. Zimmer, "Mutual thermal coupling in SiGe: C HBTs" in Symposium on Microelectronics Technology and Devices (SBMicro), Sept. 2013, Curitiba, Brazil.
9. A. K. Sahoo, S. Fregonese, **M. Weiß**, C. Maneux, N. Malbert and T. Zimmer, "Impact of Back-end-of-line on Thermal Impedance in SiGe HBTs", in 18th International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Sept. 2013, Glasgow, Scotland, United Kingdom.
10. A. K. Sahoo, S. Fregonese, **M. Weiß**, C. Maneux and T. Zimmer, "A Scalable Model for Temperature Dependent Thermal Resistance of SiGe HBTs," in IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), Oct. 2013, Bordeaux, France.

## Workshops

- M. Weiß**, C. Majek, C. Maneux and T. Zimmer, "Impact of process variation on the circuit performance (RO / LNA)", BipAk, 15 October 2010, Crolles, France
- M. Weiß**, C. Majek, C. Maneux and T. Zimmer, "Ring Oscillator: Simulation versus Measurement", HiCuM Workshop, 28 June 2011, Bordeaux, France
- M. Weiß**, S. Fregonese, M. Santorelli, A. K. Sahoo, C. Maneux and T. Zimmer, "On pulsed RF measurements", BipAk, 14 November 2012, Munich, Germany
- S. Fregonese, A. K. Sahoo, **M. Weiß**, C. Maneux and T. Zimmer, "Electro-thermal device characterization and modelling", BCTM, 3rd October 2013, Bordeaux, France