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Minju Shin

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## THÈSE

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préparée au sein des **Laboratoires IMEP-LaHC et Nano Device Laboratory**

dans **les Écoles Doctorales EEATS et School of Electrical Engineering**

# **Caractérisation électrique et modélisation des transistors FDSOI sub-22nm**

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**Ph.D. thesis**

**Under co-supervision between Korea University (Seoul, South Korea)  
and Grenoble INP (Grenoble, France)**

**Electrical Characterization and Modeling of advanced  
FD-SOI transistors for sub-22nm nodes**

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# Abstract

The advanced fully-depleted silicon-on-insulator (FD-SOI) devices with an ultra-thin body and BOX (UTBB) structure have received a great attention as one of the most possible candidates for sub-20nm CMOS technology nodes since the ultra-thin channel layer causes enhancement of gate controllability which is of help to suppress short channel effects of bulk CMOS technologies. In addition, the FD-SOI devices have other benefits such as a significant improvement of variability and mobility and threshold voltage tenability by using back-gate biasing and so on. In this dissertation, the 14nm-node FD-SOI CMOS transistors were deeply investigated in terms of their electrical characterization depending on back-gate bias, temperature, magnetic field and germanium (Ge) concentration in the case of PMOS. For the capacitive analysis, a 1D-numerical simulation was carried out in order to strengthen the variability and,  $C_{gb}$  characterization of FD-SOI devices was introduced for improving the geometrical parameter extraction methodologies. Various ways of transport characterization and the low-frequency noise measurement were conducted with varying channel materials and dimension of devices, experimentally.

In introduction of the thesis, the context of CMOS technology is explained with short channel effects. In order to overcome them, alternative techniques such as strain engineered-channel, SOI configurations, high- $\kappa$  and metal gate, multiple gates structure and beyond CMOS technology have been studied. In addition, the devices under test in our experiments are described which is 14nm-node FD-SOI CMOS transistors with high- $\kappa$  and metal gate. Finally, the dissertation scope and outline are introduced.

In the theoretical and experimental backgrounds the conventional device parameters which are generally used for evaluating the device performance and their extraction methodologies are being introduced such as Y-function method, effective mobility, split CV for mobility and series resistance extraction. In addition, the principle of magnetoresistance mobility extraction is explained in terms of geometrical magnetoresistance effects. At the end of this chapter, we deal with the definition of noise in device physics and introduce fundamental noise sources such as thermal random motion, trapping and de-trapping of charge carriers and lattice vibration.

The feasibility of both gate-to-channel and gate-to-bulk modes in ultra-thin body and BOX (UTBB) FDSOI devices is demonstrated, emphasizing the usefulness of

gate-to-bulk capacitance. In addition, the well calibrated TCAD simulation and the improved interface coupling model strengthened the validity of our analyses. These enabled us to propose an improved parameter extraction methodology for the whole vertical FDSOI stack from gate to substrate using back biasing effect.

Carrier transport properties in ultra-scaled (down to 14nm-node) FDSOI CMOS devices are demonstrated for wide range temperature. From the NMOS long channel devices, surface optical phonon (SOP) and remote Coulomb scattering (RCS) can be the dominant contribution of additional mobility scatterings in different temperature regions. Then, electron mobility degradation in short channel devices was deeply investigated. It can be stemmed from additional scattering mechanisms, which were attributed to process-induced defects near source and drain. Finally, we found that mobility enhancement by replacing Si to SiGe channel in PMOS devices is validated and this feature is not effective anymore in sub-100nm devices. The critical lengths are around 50nm and 100nm for NMOS and PMOS devices, respectively.

In the cryogenic operation under interface coupling measurement condition, we demonstrate the powerful methodology of electronic transport characterization. Thanks to this approach, the underlying scattering mechanisms were revealed in terms of their origin and diffusion center location. At first we study quantitatively transport behavior induced by the high-k/metal gate stack in long channel case, and then we investigate the transport properties evolution in highly scaled devices. Mobility degradation in short devices is shown to stem from additional scattering mechanisms, unlike long channel devices, which are attributed to process-induced defects near source and drain region. Especially in PMOS devices, channel-material related defects which could be denser close to front interface also induce mobility degradation.

We applied the magnetoresistance (MR) characterization technique on n-type FD-SOI devices of the 14nm-node technology. A notable advantage of MR is that it can probe the sub-threshold region, where Coulomb scattering influence is unscreened, while classical methods are validated to the strong inversion regime. At first, we discuss the influence of series resistance depending on gate bias, gate stack and temperature in this technology. Secondly, for long channel devices, we show that Coulomb scattering plays no significant role below threshold voltage at room temperature, in spite of the presence of a high-k/metal gate stack. MR-mobility ( $\mu_{MR}$ ) measurements were also performed in interface coupling conditions in order to further assess the role of the high-k/metal gate stack on transport properties and to analyze back bias induced mobility variations, depending on temperature range. Finally, the comparative study of low field effective mobility ( $\mu_0$ ) and  $\mu_{MR}$  shows that critical gate length of mobility degradation can be overestimated by using  $\mu_0$  at low temperature due to a lack of ability of Y-

function method to capture unscreened Coulomb scatterings. The feasibility of geometric MR measurement from linear to saturation operation regime is also demonstrated. Besides, we propose a new physical compact model for MOSFET drain current under high field transport, which reproduces experimental MR mobility from linear to saturation operation region and serves as the basis for a new extraction method of carrier saturation velocity. A benchmarking with state-of-the-art saturation velocity extraction methodologies is also conducted. Our saturation velocity results indicate that, for this technology, non-stationary transport prevails as manifested by an overshoot velocity behavior, still far from the ballistic limit.

Finally, the low-frequency (LF) noise properties in highly scaled (down to 14nm-node) FDSOI CMOS devices are presented. We analyzed LF noise behavior in the linear region for NMOS and PMOS with different channel lengths and Ge concentration. We found that the carrier number fluctuation with correlated mobility fluctuation model rather the Hooge mobility fluctuation model shows good agreement with the experimental results. In addition, we extracted electrical parameters such as the trap density ( $N_t$ ) at interfacial layer between channel and oxide layers and corrected Coulomb scattering coefficient ( $\alpha_{sc}'$ ), which generally imply the quality of interfacial layer. Then, the LF noise characterization was also performed to NMOS and PMOS long channel devices from the linear to saturation region. In the whole operational regions, the CNF with CMF model can well describe the LF noise characteristics and these results are consistent with them of the linear region.

**Keywords:** fully-depleted Silicon-on-insulator (FD-SOI), 14nm-node, Carrier transport, Low temperature, Full split CV, Low frequency noise, Coupling measurement, Magnetoresistance, mobility



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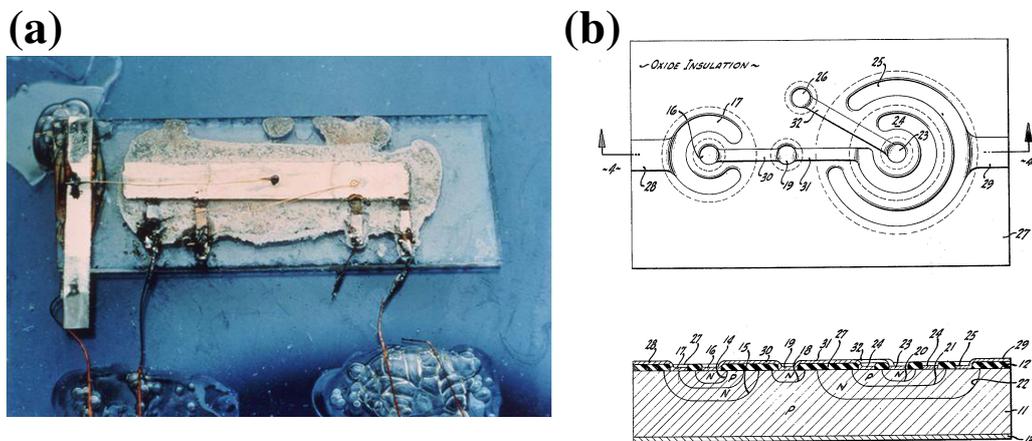
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# Chapter 1

## Context of the work

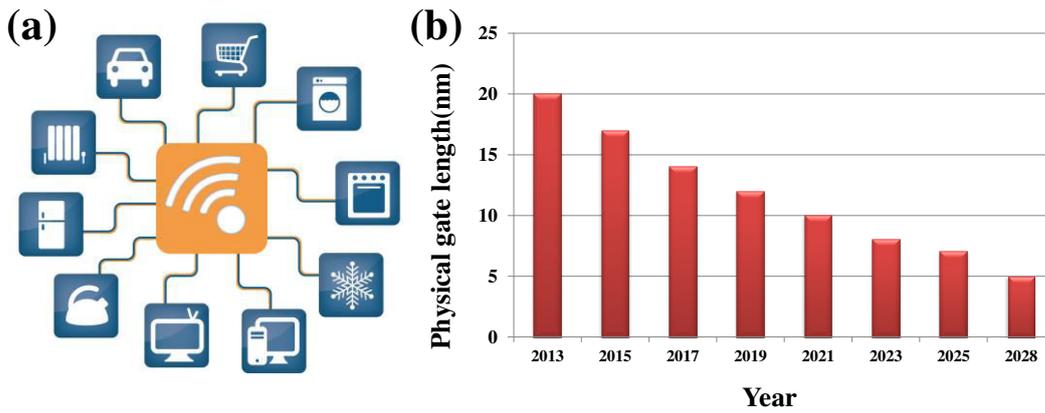
### 1.1 The context of CMOS technology



**Figure 1.1** (a) Photograph of firstly demonstrated IC with germanium and (b) schematic diagram of IC by R. Noyce [4,5]

As the history of the transistors dates back, the “bipolar junction transistors” (BJT) with germanium and the “metal–oxide–semiconductor field–effect transistors” (MOSFET) on silicon substrates were firstly reported by W. Shockley, J. Bardeen and W. Brattain in 1947, and by D. Kahng and M.M. Atalla in 1960, respectively [1,2]. Furthermore, we cannot help mentioning that the integrated circuits(IC) by using germanium and silicon with grown  $\text{SiO}_2$  were demonstrated by J. Kilby in 1958 and R. Noyce in 1959, respectively [3,4]. After these remark-

able and historical inventions, the semiconductor industry has been explosively developed and shrunk to a few tens of nanometer scale devices so far. Recently, the CMOS technology has kept downscale of the transistor dimension in the era of internet of things (IoT), which is the network of physical objects equipped with electronics, software, sensors and communication for exchanging data among operators and other objects [6]. Fig. 1.2(a) well explains the concept of IoT. Consequently, it demands transistors with high performance at low power and a high degree of integration in the CMOS technology.



**Figure 1.2** (a) Conceptive diagram for Internet of Things (IoT) and (b) the trend of physical gate length variation from International Technology Roadmap of Semiconductor (ITRS) in 2013 [7,9]

Gate length reduction in the devices brings many benefits such as high speed of electric devices, low power dissipation and high density. In terms of speed, we can take the RC delay ( $\tau$ ) of an inverter as one example:

$$\tau = \frac{V_{DD} C_G}{I_{D.sat}} \quad (1.1)$$

where  $V_{DD}$  and  $C_G$  are supply voltage and gate capacitance (F). As considering the saturation condition [8],  $\tau$  can be proportional with  $L^2 / (\mu_{eff} \cdot V_{DD})$ . In other words, the speed of circuits is proportional with  $L^{-2}$ . Thus, the gate length of transistors has been continuously reduced as following the Moore's law which predicted that the number of transistors in IC would approximately double every two years for economic (cost and performance) reasons. As shown in Fig. 1.2(b), international technology roadmap of semiconductor (ITRS) in 2013 forecasted that the physical gate length will decrease until 5nm in 2028 [9].

### 1.1.1 CMOS scaling down and Short channel effects

In order to achieve various benefits and proper function of electric circuits from scaling the devices, the other structure parameters should be correctly scaled together with channel length reduction. These are summarized in Table 1.1 [8]. For an instance, if the channel length is reduced by a factor of  $k$ , other geometrical parameters such as thickness of gate-oxide, width and source/drain junction depth should be scaled with  $1/k$ .

MOSFET parameters	Scaling factor
Surface dimensions (W, L)	$1/k$
Vertical dimensions ( $t_{ox}$ , $x_j$ )	$1/k$
Doping concentration	$k$
Current, Voltage	$1/k$
Current density	$k$
Capacitance per unit area	$k$
Transconductance	1
Power dissipation	$1/k^2$
Power density	1

**Table 1.1** Initial scaling rules for MOSFETs according to a constant factor,  $k$  [8]

Following these initial rules, doping concentration should increase with  $k$  due to the reduction of depletion width. In addition, the power supply voltages should be decreased with  $k$  for sustaining internal electric field to the next generation of CMOS technology, appropriately. Unfortunately, in the case of practical technology, these scaling rules could not be followed due to a combination of physical and system-related limitations. It is obvious when we consider the power supply voltages in the industry. For the 250nm, 180nm and 130nm transistors they were 2.5V, 1.8V and 1.3V in the industry, respectively. This trend was good in term of the scaling rules. However, for the 90nm and 45nm transistors, the industry used 1.2V and 0.9V instead of 0.9V and 0.45V. But at the same time, a diversity of problems arose, such as hot carrier effects, drain induced barrier lowering (DIBL), short channel effects and velocity saturation, which results in deviation of electric devices from their ideal operation [8,10,11].

## 1.2 Advanced CMOS technology

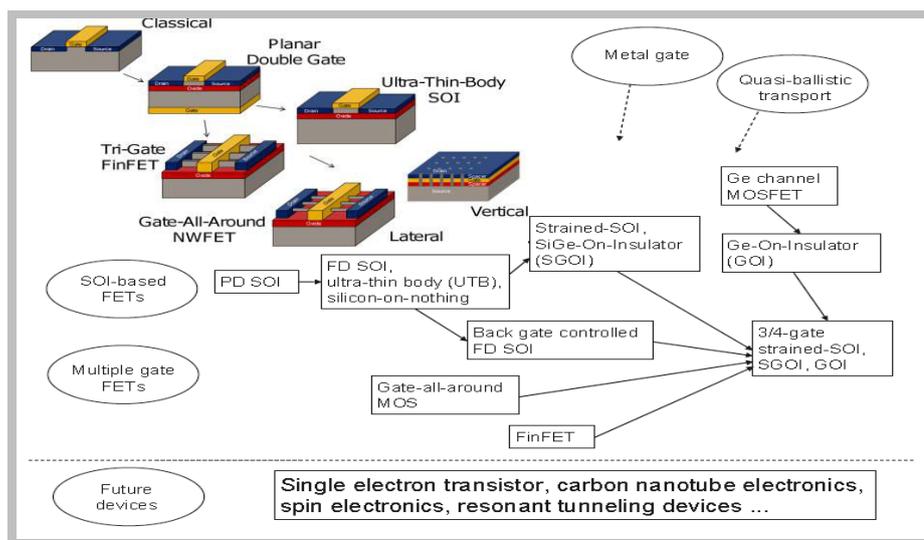
In order to suppress the short channel effects and hot carrier effects, and keep the devices scale down, the device channel engineering was introduced such as lightly doped drain (LDD), pocket or halo implant. Furthermore, many kinds of technologies have been introduced

like multiple gate device, high- $\kappa$  and metal gate, SOI device, strain engineering and alternative channel engineering. Fig. 1.3 is the overview of advanced CMOS technology [10,12].

### High- $\kappa$ and Metal gate (HKMG)

As aforementioned, the physical thickness of gate oxide ( $t_{ox}$ ) has been initially decreased for proper scaling down. However, while silicon dioxide was used as gate oxide,  $t_{ox}$  reached a limit, around 1.1nm in 2006. Indeed, gate current became unacceptably high as exponentially increases with  $t_{ox}$  reduction. It was a serious problem in terms of device life, standby power consumption and reliability. Thus, the researchers sought other materials with a higher dielectric constant, high- $\kappa$  materials, for increasing  $t_{ox}$  and replacing  $\text{SiO}_2$ . The equivalent oxide thickness can be derived as

$$t_{EOT} = \frac{\kappa_{\text{SiO}_2}}{\kappa_{\text{high-}\kappa}} t_{\text{high-}\kappa} \quad (1.2)$$



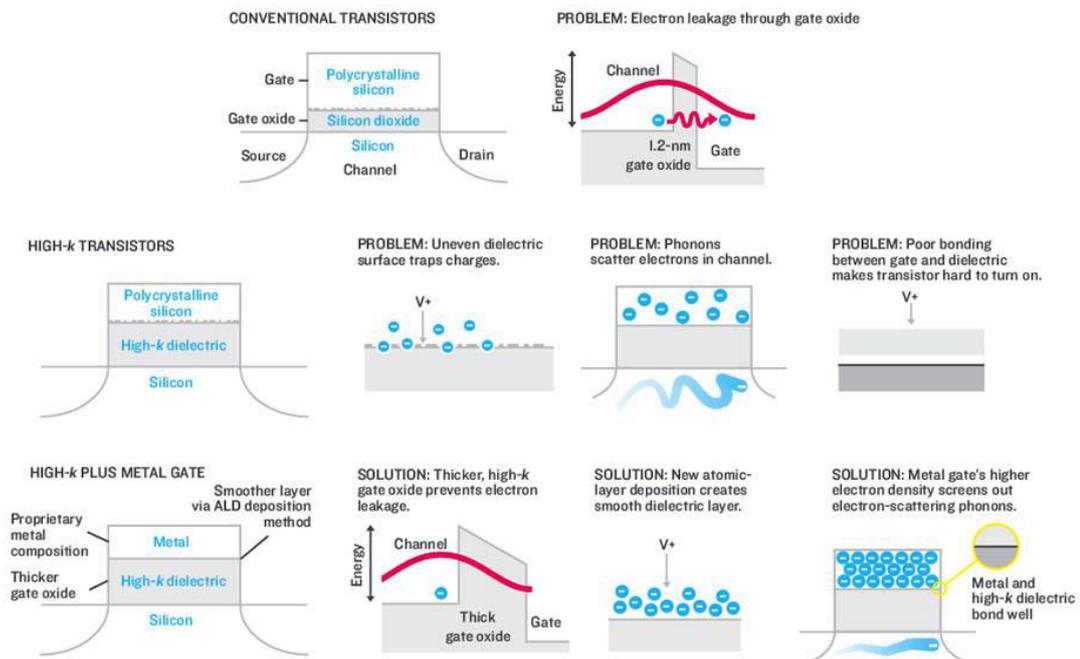
**Figure 1.3** The overview of advanced CMOS technology [10,12]

As listed in Table 1.2 [13], various high- $\kappa$  materials have been studied for the future technology. Moreover, as compared to  $\text{SiO}_2$  and  $\text{HfO}_2$ , there are intermediate solutions for compromising between defect density and high- $\kappa$ , such as oxynitrides ( $\text{SiON}$ ) and hafniumsilicates ( $\text{HfSiON}$ ).

Material	Dielectric constant $k$	Band gap $E_g$ (eV)	$\Delta E_C$ to Si (eV)	$\Delta E_V$ to Si (eV)
SiO <sub>2</sub>	3.9	8.9	3.2	4.6
Si <sub>3</sub> N <sub>4</sub>	7	5.1	2	2
Al <sub>2</sub> O <sub>3</sub>	9	8.7	2.8	4.8
Y <sub>2</sub> O <sub>3</sub>	15	5.6	2.3	2.2
La <sub>2</sub> O <sub>3</sub>	30	4.3	2.3	0.9
Ta <sub>2</sub> O <sub>5</sub>	26	4.5	1-1.5	1.9-2.4
TiO <sub>2</sub>	80	3.5	1.2	1.2
HfO <sub>2</sub>	25	5.7	1.5	3.1
ZrO <sub>2</sub>	25	7.8	1.4	5.3

**Table 1.2** Properties of the commonly researched high- $k$  dielectric materials from Wilk et al. [13]

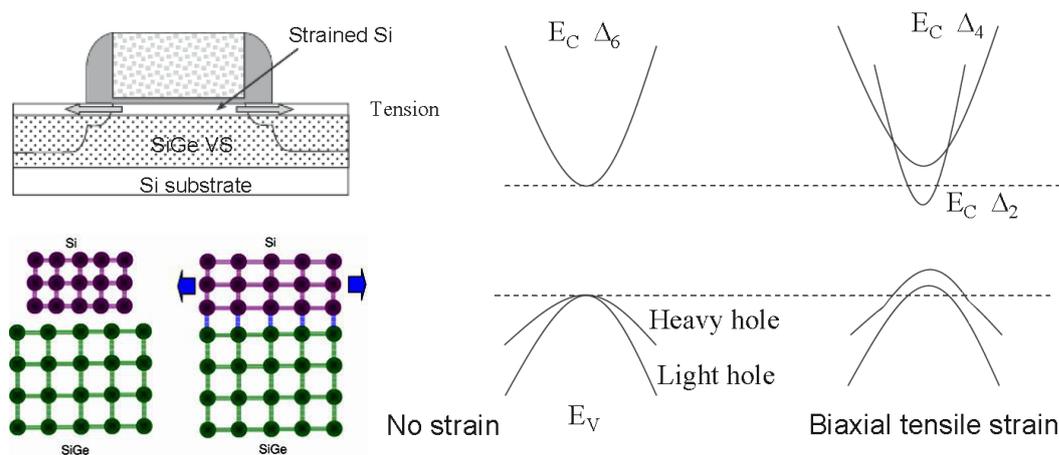
The metal gate was introduced for blocking of added capacitance from poly-Si since it can act as the additional capacitor which is connected with gate oxide in series. Furthermore, the use of metal gate can suppress dopant penetration through the gate oxide and Fermi level pinning [10]. For controlling threshold voltages, the metal gate electrode should be properly chosen in terms of work function. For the first time, these high- $k$  and metal gate (HKMG) stack were introduced in 45nm-node. In short, Fig.1.4 summarizes why the HKMG technology was needed, and obstacles and solutions of adapting the HKMG to 45nm-node [14].



**Figure 1.4** Schematic diagram of describing the necessity, problems and solutions related with high- $k$  and metal gate processes [14]

## Strain engineering

The strain engineering in CMOS technology has been introduced to enhance mobility. The mismatch of lattice constants in heterostructures creates local deformations (i.e. compressive or tensile strain) [8]. The strain engineering has been a striking method for enhancing the carrier mobility of the CMOS technology at 90nm–node in 2003 and beyond. One general method is to get a tensile strain in Si channel on the relaxed SiGe virtual substrate since SiGe has larger lattice constant than that of Si. As shown in Fig. 1.5, the tensile strain induces variations of the energy band spectrum, which results in reduction of effective electron mass and suppression of inter–band scattering since the curvature of energy band spectrum in  $k$  space presents effective mass and there are splits of energy bands. Thus, the tensile strained Si channel can have higher electron mobility than unstrained ones. In the SiGe channel in pMOSFET, the compressive strain has a positive effect on hole mobility [15]. It is worth noting that the strain engineering is the trade–off between mobility enhancement and dislocation formation. In other words, there is a certain limitation in terms of lattice mismatch.

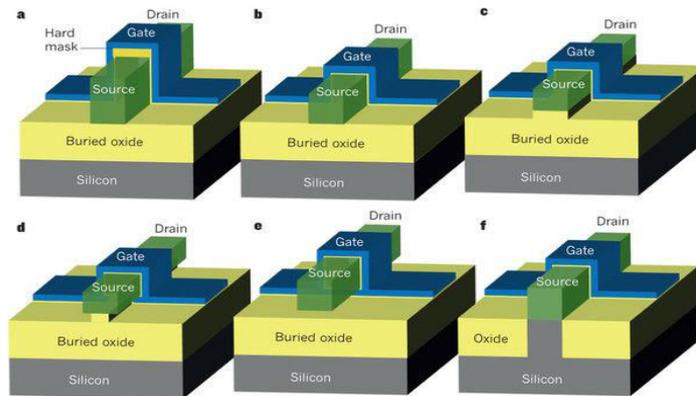


**Figure 1.5** Schematic structure of a MOSFET with tensile strained Si on the relaxed SiGe virtual substrate and energy band diagram of strained Si in  $k$  space [10,26]

## Multiple–gate and tridimensional gate devices

A variety of new gate structures have been introduced with the aim of better controlling the potential in the channel. They have been proposed in order to eliminate the short channel effects and punch through from source to drain in MOSFETs. Some of these architectures are using independent gates (e. g. double–gate structures). Others are using 3D gates with the aim of wrapping the channel as much as allowed by the fabrication technology such as FinFETs, gate–all–around FETs and Omega gate FETs. They are sometimes named under the general

term of “multiple–gate” structures in order to bring attention on the fact that the channel is no longer a simple planar channel but can be viewed as the addition of several channels in parallel, some with different crystal orientations and different dielectric thicknesses for gate control. Recently, these device architectures have also been studied with SOI and Silicon substrates as shown in Fig. 1.6 [17].



**Figure 1.6** Schematic structure of different type of gate transistors with 3D gates such as ‘fin’ gate, tri-gate,  $\Pi$ -gate and so on [17]

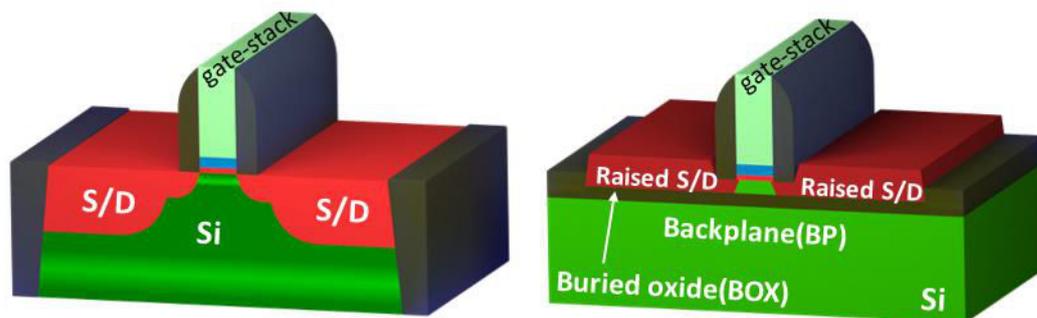
The multiple gate transistors can bring high on–current, reduction of DIBL and superior properties of on–off operations since the increase of gate number can improve electrostatic control of devices. Quantitatively, it was reported that the planar FD–SOI devices require  $1/3$  of gate length as a channel thickness ( $L/3 > t_{si}$ ) to control short channel effects while the double gate FinFETs need  $2L/3 > t_{si}$  [10,16]. In the CMOS industry, the FinFET architecture was introduced at 22nm–node in 2011 by Intel. Intel expected an outstanding combination of performance and energy efficiency by 3D tri–gate transistors. In addition, these ultra–low power transistors could be widely used in portable electric devices like cell phones and tablets. There are some challenges in the viewpoint of economic and technological aspects like high process complexity and low yield as compared with FD–SOI and bulk CMOS technologies even though FinFETs have tremendous advantages such as enhancement of performance and variability due to reduction of channel doping concentration and vertical field [17,18].

### Silicon–on–insulator architecture

SOI devices were introduced to overcome short channel effects by physically decreasing channel thickness since the short channel effects can be efficiently managed by thin Si body layer, roughly less than  $1/3$  of gate length [16]. Fig. 1.7 displays the difference between bulk transistors and fully–depleted SOI (FD–SOI) devices. One of the remarkable changes between

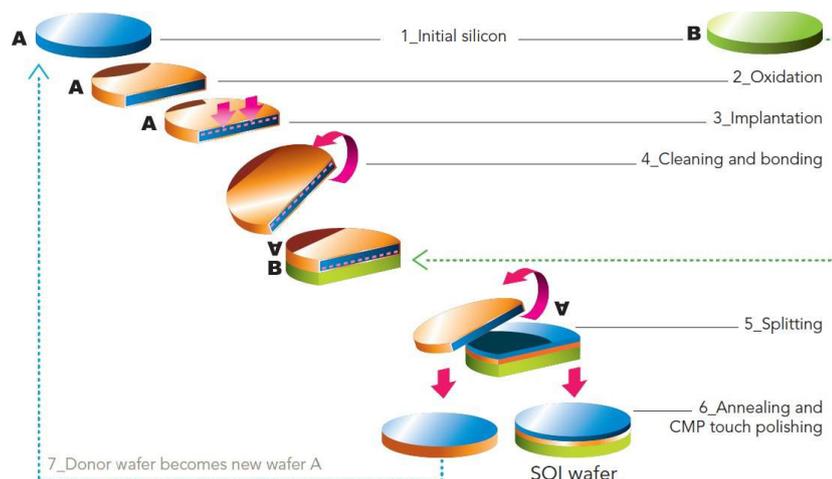
two structures is the thin Silicon layer (Channel) on a buried oxide layer. Depending on the channel layer thickness, we can classify with partial-depleted SOI (PD-SOI) and FD-SOI with thinner channel layers. In order to make a FD-SOI transistor, it should be ensured that the body thickness of is smaller than depletion width [8]:

$$t_{si} < \sqrt{4\epsilon_{si}\phi_B / qN_{body}} \quad (3)$$



**Figure 1.7** Comparative schematic structures of bulk and FD-SOI transistors

In SOI structure, to achieve thin layer of Si with the outstanding crystalline quality is the key point for optimizing FD-SOI transistors, which was solved by a “smart-cut” process of one French company, Soitec in Fig. 1.8.



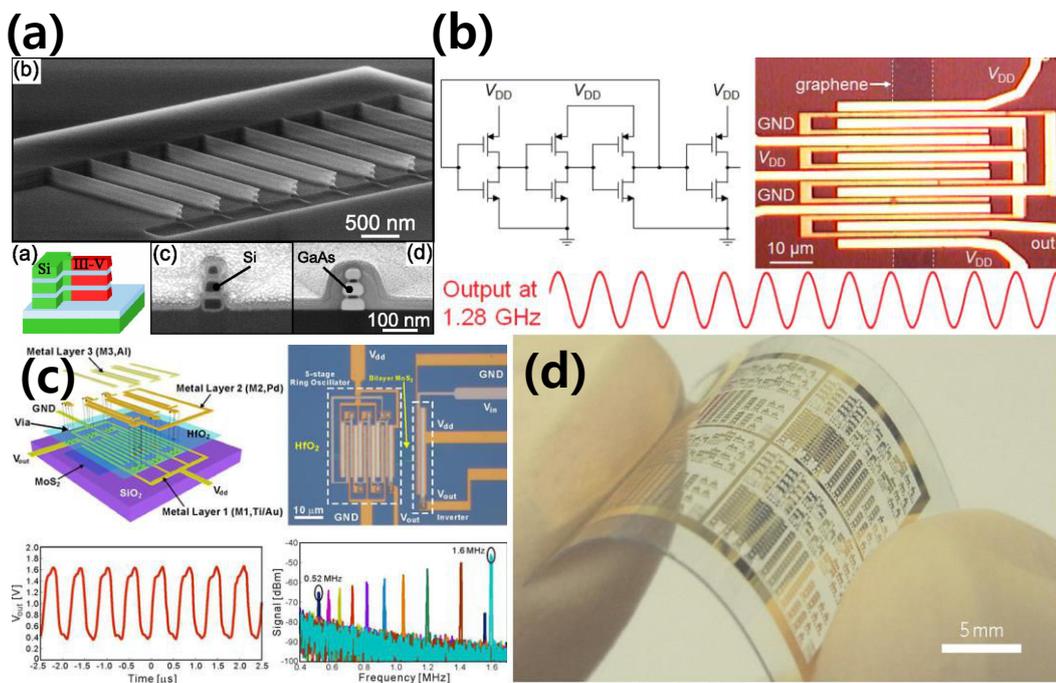
**Figure 1.8** Schematic illustration of the “smart-cut” process [19,20]

There are various benefits of FD-SOI structures; 1) excellent electrostatic control due to ultra-thin channel layer, 2) no channel doping required (i.e. less variability and reduction random dopant fluctuation), 3) performance enhancement and  $V_T$  tenability by back-gate biasing with

ultra-thin BOX layer and 4) simple processes. However, the cost of SOI substrates is the drawback of FD-SOI transistors [21] although wafer cost tends to be an ever smaller fraction of the total cost of a technology and can even be partly counterbalanced by a simpler process flow.

### Alternative channel materials

III–V semiconducting materials, such as InP, InGaAs, GaAs and InAs, and Ge are excellent candidates for the channel materials in the next CMOS generation since they have better mobility and less effective mass as compared with Si and SiGe [22]. In addition, for cost reasons, the introduction of these materials should not be performed at the expense of huge changes of CMOS platform and fabrication processes. In order to use them, it is mandatory to obtain at the same time high crystalline III–V and Ge layers, outstanding interfacial quality between channel and oxide, low access resistance and CMOS integration methods.



**Figure 1.9** Various example of demonstrating future CMOS technologies: (a) stacking of Si and GaAs nanowire [22], ring oscillator based on (b) graphene [23] and (c) bilayer MoS<sub>2</sub> [24], and (d) flexible integrated circuits with CNT [25]

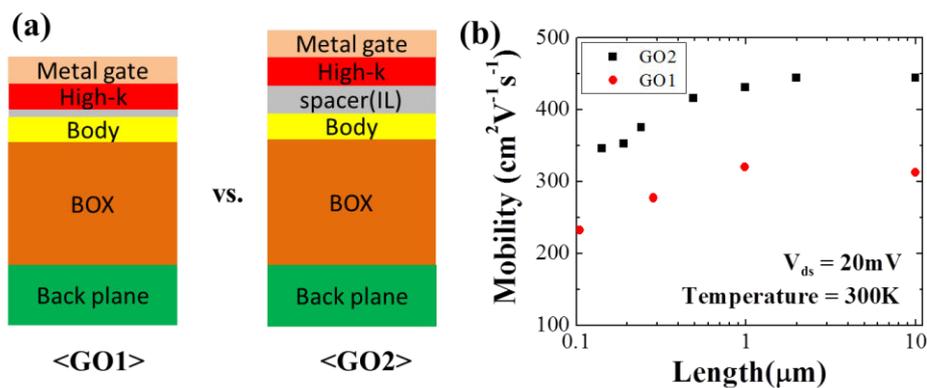
As shown in Fig. 1.9, Carbon based materials (i.e. CNT and graphene), nanowires and 2D transition metal di-chalcogenides (TMDs) such as MoS<sub>2</sub> and WSe<sub>2</sub> are another route which has recently started to be explored [22–25]. Even though these materials require a number of studies in term of reproducibility and optimization before they can be used in the industry, they have a potential for future technologies such as flexible and transparent devices.

### 1.3 Devices under study

In our study, the devices under test were fabricated by STMicroelectronics using their 14nm–node technology [26–28]. UTBB FDSOI devices with high–k and metal gate were made on (100) SOI wafers with 25nm BOX. The body thickness was thinned down to 7nm for the undoped channel. The UTBB devices can provide outstanding electrostatic control as well as performance enhancement and a switching variability by back-biasing. For the PMOS devices, SiGe channel layers were fabricated by the condensation method (with 10%, 13%, 15% and 20% of Ge) in order to achieve better hole transport properties [29,30]. In our devices, the gate–oxide stack consists of high–k gate dielectric (HfSiON) on top of SiON interfacial layer, with an equivalent oxide thickness (EOT) of 1.4nm for GO1 and 4.0nm for GO2 since there is intentional thicker interfacial layer (IL) between the high–k layer and channel in GO2 devices, while other characteristics of the gate stack remained unchanged as shown in Fig 1.10(a). On–mask gate length ( $L_M$ ) ranged from 10 $\mu\text{m}$  to 30nm for GO1 devices and from 10 $\mu\text{m}$  to 100nm for GO2 devices. The information of GO1 and GO2 devices is summarized in Table 1.3.

	GO1	GO2
Body thickness	~7nm	
Body doping	undoped channel	
BOX thickness	~25nm	
EOT	~1.4nm	~4.0nm
Gate length ( $L_M$ )	10 $\mu\text{m}$ ~ 30nm	10 $\mu\text{m}$ ~ 100nm
Ge content in PMOS	10%, 13%, 15%, 20%	

**Table 1.3** The specifications of device under study



**Figure 1.10** (a) comparative schematic structures of GO1 and GO2 devices (b) mobility properties of GO1 and GO2 devices as a function of channel length at 300K

As shown in Fig. 1.10(b), the transport characteristics of GO2 devices displays better performance than them of GO1 devices with similar channel length (cf. the extraction methodology and process can be found in Chapter 2.1 and 4.3). It might be due to the distance between channel and high-k layers, which caused by different IL thickness. The various mobility analyses were conducted in order to prove it, which are demonstrated in Chapter 4 to 6.

## 1.4. Dissertation scope and outline

The work described in this dissertation has been mainly carried out at IMEP–LaHC laboratory, with the support of the REACHING 22 CATRENE and Places2Be ENIAC European projects under Grant Agreement No. CT208 and JTI 325633.

The aim of this thesis is to investigate the electrical properties of 14nm–node FD–SOI CMOS transistors, which is the one of most promising candidates for adoption in sub–20nm CMOS technology nodes because of their interesting potentialities, such as superior electrostatic integrity, low variability and so on.

**Chapter 2** introduces the main parameters which are used to investigate final device characteristics as well as their extraction methodologies. These parameters can be utilized with the base of device evaluation and modeling. In addition, the principle of magnetoresistance (MR) effects and low frequency noise are described.

**Chapter 3** describes the split CV method and how it recovers its full potential with UTBB FD–SOI transistors. We show how it enabled us to extract geometrical parameters related with whole vertical FD–SOI stack as well as complementary information on back–plain doping concentration. 1D TCAD simulations were carried out for validation and a new corrected coupling capacitance model was developed in support.

**In Chapters 4 and 5**, transport properties in ultra–scaled FD–SOI transistors were studied. The different scattering mechanisms were de–correlated by varying temperature from 77K to 300K.

Chapter 4 compares transport in devices that defer by their gate stacks. The additional scattering times associated to the introduction of the high–k dielectric layer were identified. Temperature dependence of the additional mobility was clarified with in–depth study of the role of the different scattering mechanisms. Furthermore, carrier mobility reduction in short channel devices was intensely characterized. It can originate from additional scattering mecha-

nisms induced by process-induced defects o near source and drain.

In Chapter 5, we added the interface coupling condition, which is a combination of front gate and back gate biasing, to cryogenic operation. It was possible to tune the vertical position of the channel depending on coupling conditions, and we analyzed the influence of this tuning on transport characteristics and mobility enhancement of mobility both quantitatively and qualitatively in long channel devices. The results obtained in short gate devices demonstrated a weaker mobility improvement with back gate biasing. This was found consistent with the fact that transport properties would then be governed by process induced defects distributed around source and drain regions. As compared to NMOS, PMOS transistors with short channel show the surface-like behavior.

**Chapter 6** analyzes geometrical magnetoresistance (MR) effects on ultra-scaled FD-SOI devices. The transport characteristics of transistors with an undoped channel was shown from weak inversion regime to strong inversion regime with the advantage that MR effect brings information about transport in the sub threshold regime, while this is out of the range of validity of other extraction methods. For the first time, we applied interface coupling conditions to MR mobility measurements in order to further assess the role of the high-k/metal gate stack on transport properties and to analyze back bias induced mobility variations, depending on temperature range. In addition, we revealed that the critical gate length which is used to characterize mobility degradation at short gate length can be overestimated by using low field mobility ( $\mu_0$ ) at low temperature due to a lack of ability of the Y-function method to capture unscreened Coulomb scattering.

We also proved usability of MR mobility characterization from the linear regime of operation to saturation. Besides, a new physical compact model for MOSFET drain current under high field transport was developed. The non-stationary and ballistic transport properties of this technology were investigated based on saturation velocity.

**Chapter 7** analyzes low frequency (LF) noise behavior of the CMOS technology at 14nm-node with FD-SOI. The  $1/f$  noise behavior was well explained with the carrier number fluctuation (CNF) with correlated mobility fluctuation (CMF) model, which is grounded on the trapping and de-trapping of free carriers at interfacial layers (i.e. at the interfaces between channel and gate dielectric or BOX) and the correlated changes in Coulomb scattering induced by variations in trapped charges. In addition, we confirmed that CNF with CMF model can fully reproduce LF noise properties from linear to saturation regime.

Finally, **Chapter 8** concludes all results and discussion in this work.

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# Chapter 2

## Theoretical and experimental back-grounds

### 2.1 Parameter extraction methods for MOSFETs

#### 2.1.1 Mobility

Free carriers mobility is the key parameter to determine electrical device performance. Without electric field, electron distribution follows a random distribution with no preferred moving direction and a mean energy equal to thermal energy. When an electric field  $E$  is applied, the distribution shows a mean group velocity which, in the case of electrons in an isotropic material, is opposite to electric field. Under low field, linear assumptions can hold and this drift velocity is proportional to  $E$ . The coefficient  $\mu$ , called the mobility, defines how fast the charge carriers can move with electrical field in a given material:

$$v = \mu \cdot E \quad (2.1).$$

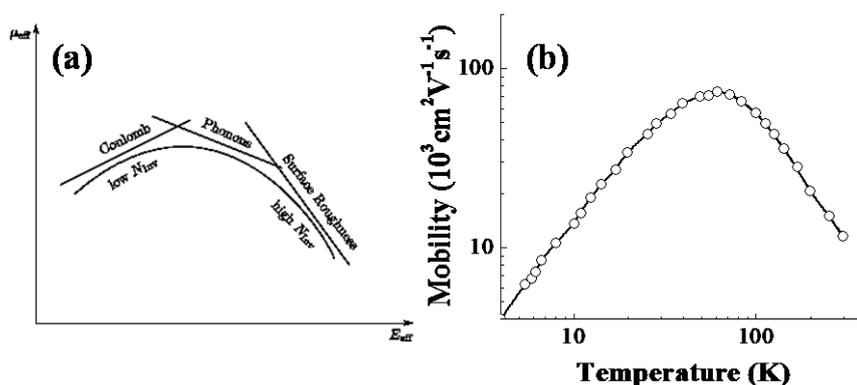
where  $v$  and  $E$  represent free carriers velocity and electric field, respectively.

##### 2.1.1.1 Matthiessen's rule

As charge carriers flow through a material, they experience many kinds of scattering processes, for instance with phonons, fixed charges (Coulomb scattering) or surface roughness. It limits mobility as shown in Fig. 2.1(a) [1]. Thus, the mobility can be described the reciprocal of the sum of the reciprocals of the mobility terms related to each scattering mechanism:

$$\frac{1}{\mu} = \frac{1}{\mu_{\text{ph}}} + \frac{1}{\mu_{\text{C}}} + \frac{1}{\mu_{\text{SR}}} \quad (2.2)$$

where  $\mu_{\text{ph}}$ ,  $\mu_{\text{C}}$  and  $\mu_{\text{SR}}$  are the mobility terms related to phonon, Coulomb and surface roughness scattering, respectively. The Matthiessen's rule assumes that the different scattering mechanisms are independent from each other. In addition, the scattering with the lowest mobility is critical to decide the total mobility.



**Figure 2.1** (a) The effective mobility as a function of the effective electrical field [1] (b) Electron Hall mobility versus temperature for  $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$  [2]

### 2.1.1.2 Temperature dependence of mobility

Phonon scattering (also called lattice scattering) decreases as temperature decrease since lattice vibration becomes weak. In contrast, Coulomb scattering is strengthened at low temperature due to slower thermal motion which results in larger deflections by ionized impurities, stronger velocity randomization and thus smaller equivalent scattering time. Finally, surface roughness scattering, which is enhanced in the strong inversion regime of MOSFET operation, as well as scattering by neutral defect have no temperature dependence. Fig. 2.1(b) displays the typical temperature dependence of mobility resulting from Coulomb and phonon scattering mechanisms [2]. Low field mobility is ruled by phonon-like behavior around room temperature as mobility is inversely proportional with temperature while it shows Coulomb-like behavior at low temperature, where this mobility term is proportional to temperature. Since low field mobility does not concern strong inversion regimes,  $\mu_{\text{SR}}$  can be neglected. In addition, for some short channel devices, it can be necessary to account for neutral defect scattering. As a result, the empirical model of low field mobility with temperature dependence can be modelled by

$$\frac{1}{\mu} = \frac{1}{\mu_{\text{ph}} \left(\frac{300}{T}\right)^\alpha} + \frac{1}{\mu_{\text{C}} \left(\frac{T}{300}\right)^\beta} + \frac{1}{\mu_{\text{neu}}} \quad (2.3)$$

where  $\mu_{\text{ph}}$ ,  $\mu_{\text{C}}$  and  $\mu_{\text{neu}}$  are the phonon, Coulomb and neutral defect scattering mobility terms at room temperature [3].

### 2.1.1.3 Mobility extraction methods for MOSFETs

#### (1) Field-effect mobility ( $\mu_{\text{FE}}$ )

In linear operational regime of MOSFET, the drain current is typically expressed by

$$I_{\text{ds}} = \frac{W}{L} C_{\text{ox}} \mu_{\text{eff}} (V_{\text{gs}} - V_{\text{T}}) V_{\text{ds}} \quad (2.4)$$

where  $C_{\text{ox}}$  is the gate capacitance per unit area ( $\text{F}/\text{cm}^2$ ) and  $V_{\text{T}}$  is the threshold voltage. The field-effect mobility is derived from transconductance ( $g_{\text{m}}$ ), derivative of Eq. 2.4:

$$g_{\text{m}} = \frac{W}{L} C_{\text{ox}} \mu_{\text{eff}} V_{\text{ds}} \quad (2.5).$$

So, the field-effect mobility can be defined by

$$\mu_{\text{FE}} = \frac{g_{\text{m}} L}{V_{\text{ds}} C_{\text{ox}} W} \quad (2.6).$$

The field-effect mobility can be calculated easily and simply. As compared to low-field mobility ( $\mu_0$ ), the maximum value of field-effect mobility usually is lower due to the effect of series resistance.

#### (2) Effective mobility ( $\mu_{\text{eff}}$ )

In the MOSFETs, the effective mobility can be defined as

$$\mu_{\text{eff}} = \frac{L^2 I_{\text{ds}}}{V_{\text{ds}} Q_{\text{n}}} \quad (2.7)$$

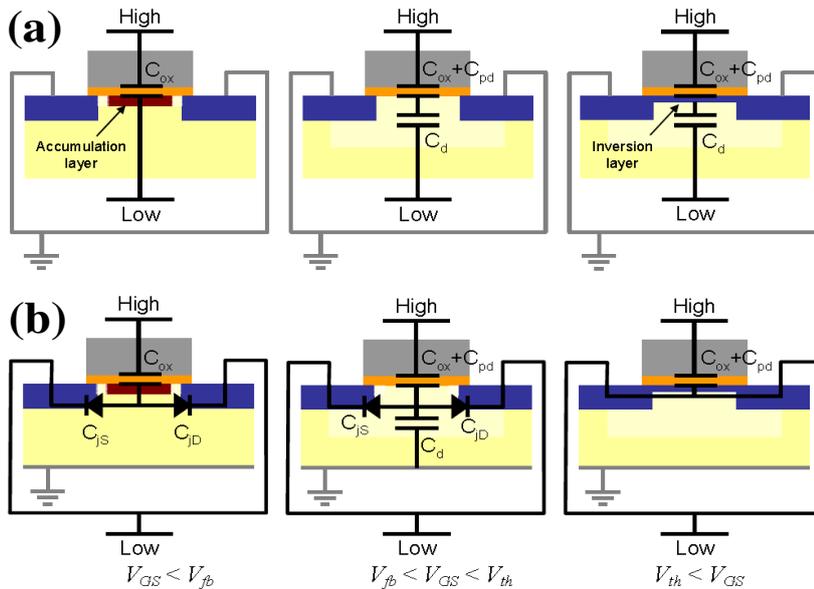
where  $Q_{\text{n}}$  is the mobile carrier charge. In strong inversion,  $Q_{\text{n}}$  can be approximated by  $\sim WL \times C_{\text{ox}} (V_{\text{gs}} - V_{\text{T}})$ . This approximate expression for  $Q_{\text{n}}$  is only valid above threshold voltage.

However, the split CV measurement is essential for the precise calculation of  $Q_n$  since a small amount of mobile charge is already present before the gate voltage reaches threshold voltage. The split CV method is also used for analyzing the trapped interface states in weak inversion and the bulk doping concentration. It consists in measuring the capacitance–voltage characteristics of the transistors in two different measurement configurations as shown in Fig. 2.2 so as to extract (a) gate–to–channel capacitance ( $C_{gc}$ ) and (b) gate–to–bulk capacitance ( $C_{gb}$ ) [4]. Fig. 2.2(a) shows that the  $C_{gc}$  measurement is closely related with inversion carriers. On the other hand the  $C_{gb}$  measurement represents the accumulation carriers (Fig. 2.2(b)) [5]. By using  $C_{gc}$  measurement, we can accurately estimate  $Q_n$ :

$$Q_n(V_{gs}) = \int_{-\infty}^{V_{gs}} C_{gc}(V_{gs}) dV_{gs} \quad (2.8)$$

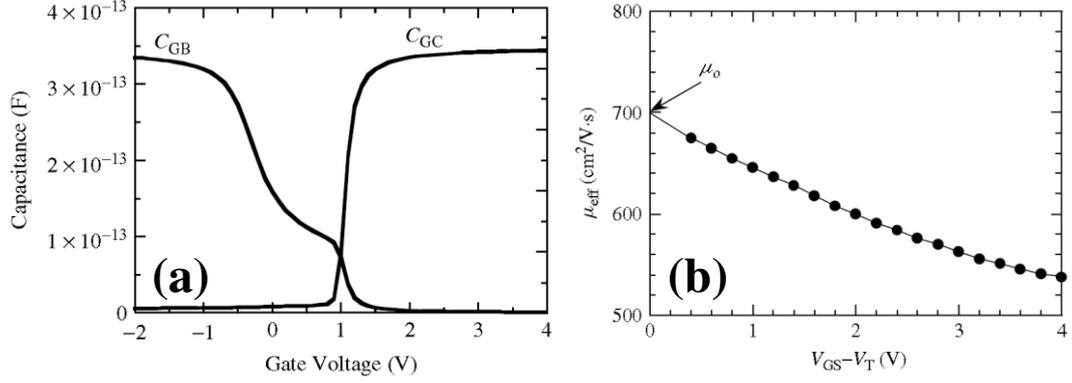
The degradation of effective mobility at larger transverse effective field or gate voltage is normally observed in mobility characterization of conventional MOSFETs. Fig. 2.3(b) well demonstrates this mobility degradation. It can be explained by enhanced surface roughness scattering in strong inversion and this tendency is usually modelled by the following empirical model [6, 7]:

$$\mu_{eff} = \frac{\mu_0}{1 + (E_{eff} / E_c)^\alpha} \quad (2.9)$$



**Figure 2.2.** Schematic figures for (a) gate-to-channel capacitance measurement configuration and (b) gate-to-bulk capacitance measurement configuration [4]

where  $E_{\text{eff}}$ ,  $E_c$  and  $\alpha$  indicate the transverse effective electric field, critical electric field and exponent of mobility reduction, respectively. The typical values used for  $\alpha$  are  $\sim 1.5$  and  $\sim 1$  for electrons and holes, respectively. [5]



**Figure 2.3** Typical example of (a) capacitance variation as a function of gate voltage in the split CV configurations and (b) low field mobility and effective mobility degradation with overdrive gate voltage [5]

### (3) Low field mobility ( $\mu_0$ ) with Y-function method

The Y-function method was introduced by [8]. As considering gate dependence of effective mobility, Eq. 2.4 can be developed to

$$I_{\text{ds}} = \frac{W}{L} C_{\text{ox}} \frac{\mu_0}{1 + \theta(V_{\text{gs}} - V_{\text{T}})} (V_{\text{gs}} - V_{\text{T}}) V_{\text{ds}} \quad (2.10)$$

where  $\theta$  and  $\mu_0$  are the mobility attenuation factor and low field mobility. After differentiating Eq. 2.10, the transconductance can be solved to

$$g_{\text{m}} = \frac{\partial I_{\text{ds}}}{\partial V_{\text{gs}}} = \frac{W}{L} C_{\text{ox}} \frac{\mu_0}{[1 + \theta(V_{\text{gs}} - V_{\text{T}})]^2} V_{\text{ds}} \quad (2.11)$$

The low field mobility and threshold voltage can be found out of the linear fit of the Y-function, which has been defined as the ratio between drain current and square root of transconductance:

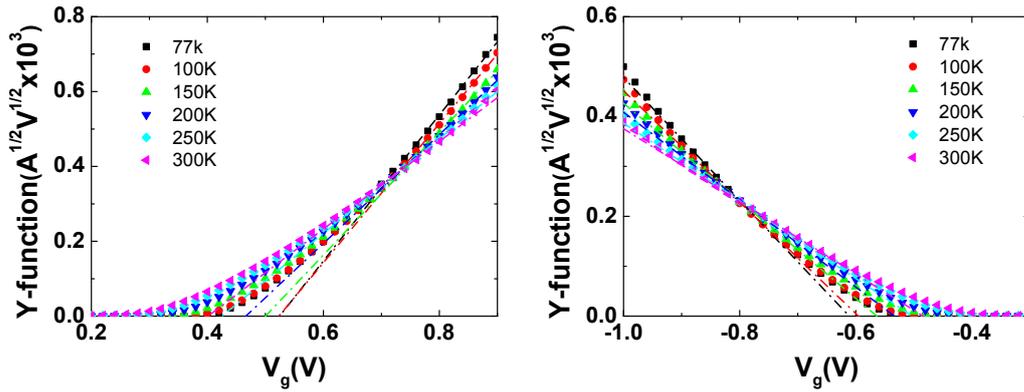
$$\frac{I_{\text{ds}}}{\sqrt{g_{\text{m}}}} = \left( \frac{W}{L} C_{\text{ox}} \mu_0 V_{\text{ds}} \right)^{0.5} (V_{\text{gs}} - V_{\text{T}}) \quad (2.12)$$

In this step,  $\theta$  is eliminated and the only unknown parameters are  $\mu_0$  and  $V_{\text{T}}$  if we assume that

targeted gate dimensions can be safely used for L (channel length) and W (channel width). One can notice that  $I_{ds}/g_m^{0.5}$  shows a linear dependence on gate voltage. Therefore, we can easily extract  $\mu_0$  and  $V_T$  from the slope and intercept point as shown in Fig. 2.4. Another benefit of this method is immunity to series resistance. So we can evaluate intrinsic transport properties. The Y-function method has been further developed to account for surface roughness scattering for MOSFET with very thin gate oxide layer [4]:

$$I_{ds} = \frac{W}{L} C_{ox} \frac{\mu_0}{1 + \theta_1 (V_{gs} - V_T) + \theta_2 (V_{gs} - V_T)^2} (V_{gs} - V_T) V_{ds} \quad (2.13)$$

where  $\theta_1$  and  $\theta_2$  are the first and second order mobility attenuation factor. In this case, the simple extraction method is insufficient. Thus, other method such as iterative method [9], Mac Larty method [10] and polynomial regression method [11] were suggested in order to extract low field mobility.



**Figure 2.4** Typical  $Y(V_g)$  curves for various temperatures used for mobility extraction for n and p MOS devices ( $V_d=20mV$ ,  $L=10\mu m$ ,  $W=1\mu m$ ).

### 2.1.2 Series Resistance from the Y-function method

As shown in Fig. 2.5(a), the drain current in the linear operational regime can be derived with account to series resistance ( $R_{sd}$ ):

$$I_{ds} = \frac{W}{L} C_{ox} \frac{\mu_0}{1 + \theta_0 (V_{gs} - V_T)} (V_{gs} - V_T) (V_{ds} - I_{ds} R_{sd}) \quad (2.14)$$

where  $\theta_0$  is the intrinsic mobility attenuation factor without influence of series resistance. We reorganize Eq. 2.14 in terms of  $I_{ds}$ :

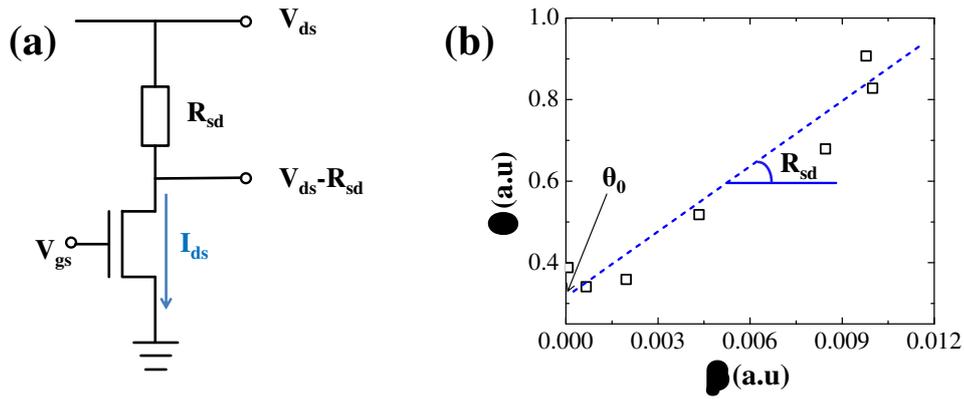
$$I_{ds} = \frac{\beta(V_{gs} - V_T)V_{ds}}{1 + (\theta_0 + \beta R_{sd})(V_{gs} - V_T)} \quad (2.15)$$

$$\beta = \frac{W}{L} C_{ox} \mu_0 \quad (2.16)$$

By using Eqs. (2.10) and (2.15), the relationship between the series resistance and extrinsic mobility attenuation factor can be obtained:

$$\theta = \frac{\beta V_{ds}}{I_{ds}} - \frac{1}{V_{gs} - V_T} = \theta_0 + \beta R_{sd} \quad (2.17)$$

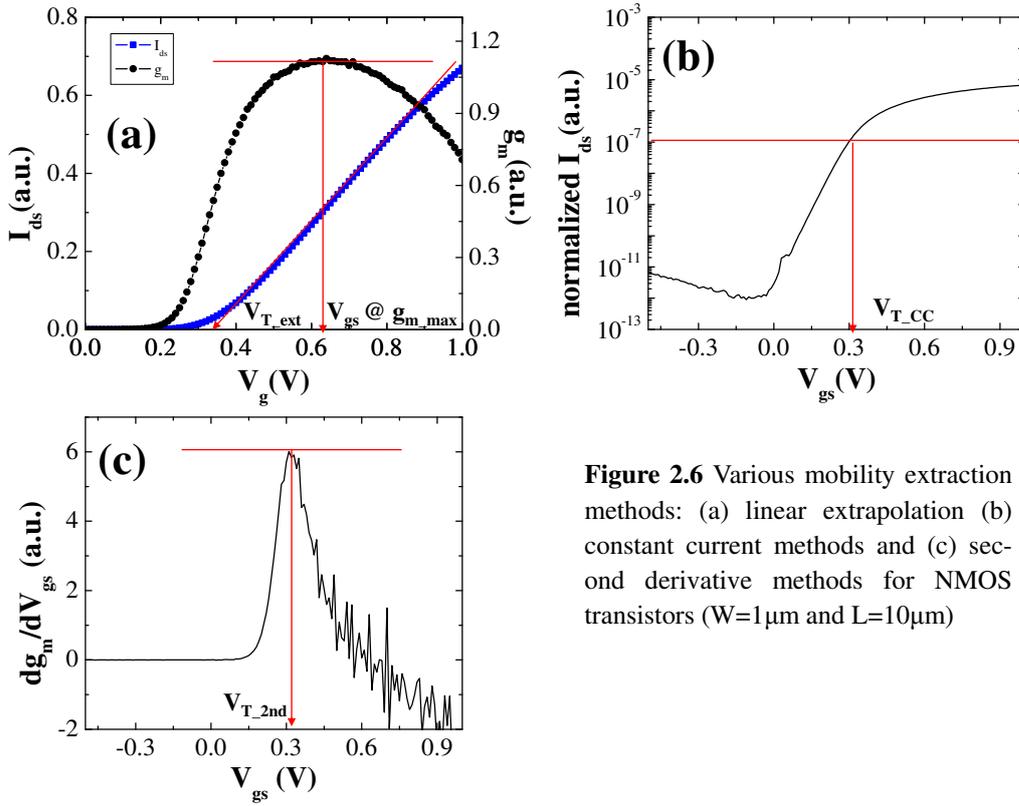
So, we can draw  $\theta$  as a function of  $\beta$  after extracting  $\mu_0$  and  $V_T$ . Then, series resistance can be extracted from the slop of  $\theta$  vs.  $\beta$  as shown in Fig. 2.5(b).



**Figure 2.5** (a) A schematic circuit of a transistor and  $R_{sd}$  and (b)  $\theta_0$  and  $R_{sd}$  extraction for NMOS transistors by using Y-function method from  $\theta$  as a function of  $\beta$ . ( $W=1\mu\text{m}$  and  $L=10\mu\text{m}$  to  $30\text{nm}$ )

### 2.1.3 Threshold voltage ( $V_T$ )

The threshold voltage is the important parameter to characterize the MOSFETs operation and is the requirement for generating the conduction path in semiconductor materials, qualitatively. The  $V_T$  should be included in other characterization processes such as extracting mobility and contact resistance. So, we need to carefully estimate  $V_T$ . In the literature [13], there are many different extraction methods like linear extrapolation, second derivative, Y-function and constant current methods as shown in Fig. 2.6. In this section, we will briefly deal with these methods for the proper  $V_T$  extraction, beyond the Y-function method which has already been presented in 2.1.1.3.



**Figure 2.6** Various mobility extraction methods: (a) linear extrapolation (b) constant current methods and (c) second derivative methods for NMOS transistors ( $W=1\mu\text{m}$  and  $L=10\mu\text{m}$ )

### 2.1.3.1 Linear extrapolation method

This method is often used for  $V_T$  extraction. At first, find the maximum point of transconductance ( $g_m$ ) and then, make a linear regression with the transfer curve. From the x-intercept point of the linear extrapolation, we can get  $V_T$ .

### 2.1.3.2 Second derivative method

In the second derivative method,  $V_T$  is determined by the maximum point of derivative  $g_m$ - $V_{gs}$  curve. The benefit of this method is to exclude contact resistance impact on  $V_T$ . In ideal case of MOSFET, drain current is almost zero below  $V_T$ , and increases proportionally with gate bias above  $V_T$ . So, the first and second derivative of drain current show step function and delta function, respectively. Even though we cannot find infinite delta function in the practical case, it is enough to find the  $V_T$  with the maximum point of the second derivative.

### 2.1.3.3 Constant current method

This method is well known and is widely used in the industry because it is simple and

fast. It consists in extracting the gate voltage that gives a given current density with a proper normalization which accounts for drain current variation with  $L$  and  $W$ . The value of drain current which is typically used is  $W/L \times 10^{-7}$  A [14]. In order to increase the reliability of this method, one can use a combination of the constant current method and second derivative method.

### 2.1.4 Subthreshold swing (SS)

When gate voltage is smaller than the threshold voltage, it is known as the subthreshold conduction. In this regime, it is important that drain current decreases as sharply as possible when gate voltage decreases, which is significant for low power applications, such as switch in digital circuits, and memory applications. The current in subthreshold regimes is a diffusion current from source to drain, and can be modelled as [12];

$$I_{ds} = \mu(C_d + C_{it}) \frac{W}{L} \left(\frac{kT}{q}\right)^2 \left(1 - e^{-\frac{-qV_{ds}}{kT}}\right) \left(e^{\frac{q(V_{gs} - V_T)}{C_r kT}}\right) \quad (2.18)$$

where

$$C_r = \left[1 + \frac{C_d + C_{it}}{C_i}\right]$$

and  $C_d$ ,  $C_{it}$  and  $C_i$  are depletion, interface state and gate insulator capacitance per unit area. The subthreshold slope (SS) quantifies drain current variation with gate voltage below threshold. Due to the exponential dependence of Eq. 2.18, it is defined as

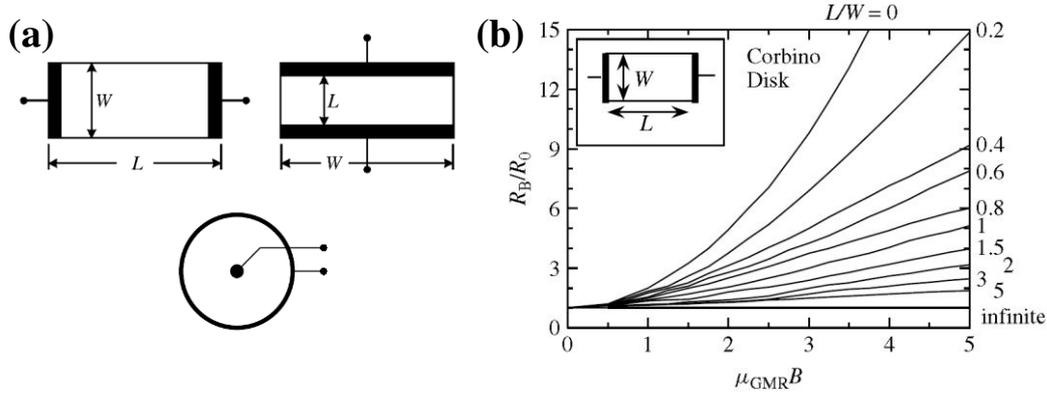
$$SS = \frac{dV_{gs}}{d(\log I_{ds})} = \ln 10 \frac{dV_{gs}}{d(\ln I_{ds})} = 2.3 \frac{kT}{q} \left[1 + \frac{C_{it} + C_d}{C_i}\right] \quad (2.19)$$

In MOSFET operation, SS is physically limited by the tail of the Fermi distribution. The smallest achievable value (ideal value) at room temperature is  $\sim 60$  mV/decade.

## 2.2 Magnetoresistance

Magnetoresistance is the variation of material resistance with transverse magnetic field (normal to the conduction plane). For direct mobility extraction from the magnetoresistance, wide channel devices ( $W \gg L$ ) or Corbino disk in Fig. 2.7(a) are necessary unlike Hall

measurement which geometrically require rather long channel device ( $L \gg W$ ) with four or more contact [5]. For other geometries, correction factors must be introduced (Fig. 2.7(b)). In practice, conventional FETs are usually fabricated with wide and short channels, so that one can measure the magnetoresistance of wide FETs without additional fabrication processes.



**Figure 2.7** (a) Long, wide and Corbino disk samples and (b)  $R_B/R_0$  vs.  $\mu_{GMR}B$  as a function of length/width ratio [5,15]

The increase of resistivity for semiconducting materials is the general phenomenon with the magnetic field, which is the physical magnetoresistance (PMR) effect. It can be observed with anisotropic conduction and conduction with more than one type of carrier [5]. On the other hand, the magnetic field can create an increase of resistance which is originated from the deviation of carrier moving path. It results in an increase of semiconducting materials resistance which is called the geometrical magnetoresistance (GMR) effect. The intensity of the GMR effect depends strongly on sample geometry. As compared to PMR effect, the GMR effect is usually larger. As mentioned above, the amount of resistance variation with the magnetic field can vary with the channel length over width ratio. Fig. 2.7(b) displays that the GMR effect,  $R_B/R_0$  is negligible for the long channel devices ( $W \ll L$ ), while the resistance of wide and short channel devices and Corbino disk ( $W \gg L$ ) pointedly increase by the GMR effect [5, 15].

### 2.2.1 Principle of magnetoresistance mobility extraction

The velocity of two-dimensional electron gas under magnetic field, which is perpendicular with the current flowing plane, can be derived in semi-classical approach from the Lorentz force,  $\vec{F} = q \cdot (\vec{E} + \vec{v} \times \vec{B})$ , as:

$$v_x = \mu \cdot (E_x + v_y B_z) \quad (2.20)$$

$$v_y = \mu \cdot (E_y - v_x B_z) \quad (2.21)$$

where  $q$ ,  $v$ ,  $E$  and  $B$  are the elementary charge, velocity, electric and magnetic field, respectively. The  $z$  direction is normal to the gate to channel interface, while  $v_x$  and  $v_y$  are the components of in-plane electron velocity along channel direction and normal to it, respectively. In the case of devices with  $W \gg L$ , the Hall voltage generated by the applied magnetic field is short-circuited by source and drain equipotential lines [16], so that,  $E_y$  is nearly zero, and, in turn, Eqs. 2.20 and 2.21 simplify as:

$$v_x = \mu E_x / (1 + \mu^2 B_z^2). \quad (2.22)$$

Current density along the channel direction using Eq. 2.22 follows as [12]:

$$J_x = qn v_x = qn \mu E_x / (1 + \mu^2 B_z^2) = \sigma_0 E_x / (1 + \mu^2 B_z^2). \quad (2.23)$$

where  $\sigma_0$  refers to channel conductivity with zero magnetic field. Thus, the current density is proportional to  $(1 + \mu^2 B^2)^{-1}$  where  $\mu$  is the magnetoresistance mobility,  $\mu_{MR}$ . Therefore, provided the device under study is wide and short, the magnetoresistance mobility can be extracted directly, without any coefficient of any kind, from the relative change of current or resistance with transverse magnetic field, using:

$$-\frac{\Delta I}{I_B} = \frac{\Delta R}{R_0} = \mu^2 B_z^2 \quad (2.24)$$

where  $\Delta I$  ( $\Delta R$ ) is the difference between drain current (resistance) at field  $B$  and at zero magnetic field

### 2.2.2 Comparison between $\mu_{eff}$ , $\mu_H$ and $\mu_{MR}$

In the case of small magnetic field, the effective, Hall and magnetoresistance mobility can be derived by the Kubo–Greenwood formalism [4, 16]:

$$\mu_{eff} = \frac{q \langle \tau \rangle}{m^*} \quad (2.24)$$

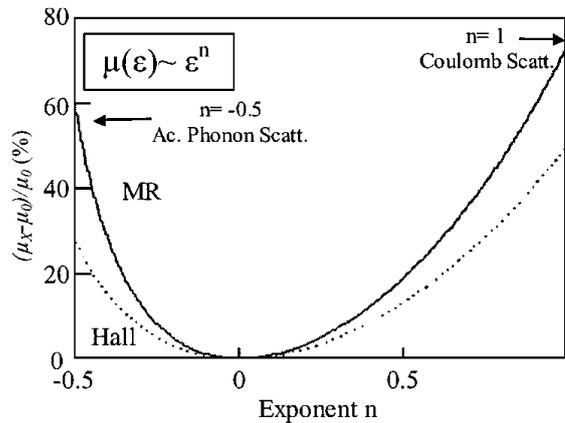
$$\mu_H = \frac{q \langle \tau^2 \rangle}{m^* \langle \tau \rangle} \quad (2.25)$$

$$\mu_{MR} = \frac{q}{m^*} \sqrt{\frac{\langle \tau^3 \rangle}{\langle \tau \rangle}} \quad (2.26)$$

where  $m^*$  is the electron effective mass and  $\langle \tau \rangle$  is the Maxwellian average value of scattering relaxation time;

$$\langle \tau \rangle = \frac{\int_0^\infty \varepsilon N(\varepsilon) \cdot \tau(\varepsilon) \left(-\frac{\partial f}{\partial \varepsilon}\right) d\varepsilon}{\int_0^\infty \varepsilon N(\varepsilon) \cdot \left(-\frac{\partial f}{\partial \varepsilon}\right) d\varepsilon} \quad (2.27)$$

In Eq. 2.27,  $\varepsilon$ ,  $N(\varepsilon)$  and  $f(\varepsilon)$  stand for kinetic energy, total density of state and Fermi–Dirac distribution function. Thus, the  $\mu_{\text{eff}}$  is equivalent with  $\mu_{\text{MR}}$  when  $\tau(\varepsilon)$  is independent with  $\varepsilon$ , which can be satisfied with a degenerate electron gas or scattering mechanisms with no kinetic energy dispersion such as the neutral defect scattering [16]. Fig. 2.8 displays the relative difference between  $\mu_{\text{MR}}$  (or  $\mu_{\text{H}}$ ) and  $\mu_{\text{eff}}$  assuming that a scattering relaxation time features a power law dependence of exponent  $n$  with energy (i.e.  $\tau(\varepsilon) \sim \varepsilon^n$ ) [16, 17]. The deviation between  $\mu_{\text{MR}}$  (or  $\mu_{\text{H}}$ ) and  $\mu_{\text{eff}}$  is enhanced in the presence of acoustic phonon scattering ( $n=-0.5$ ) or Coulomb scattering ( $n=1$ ) [4, 16]. However, the difference is negligible in the case of strong inversion ( $n=0$ ) [17].



**Figure 2.8** Relative differences between  $\mu_{\text{H}}$  or  $\mu_{\text{MR}}$  and  $\mu_0$  depending on the scattering mechanism power law exponent  $n$  [16]

### 2.3 Low frequency noise

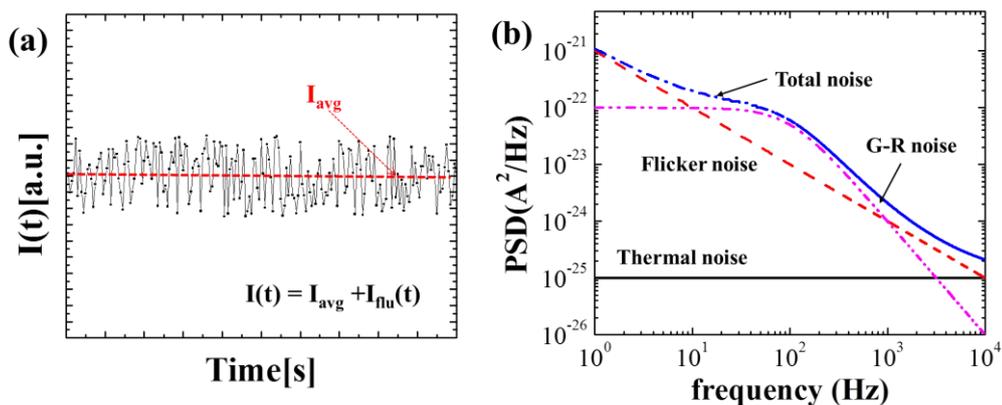
Noise is the unwanted signal in the measured or detected signal, which can be originated from external sources (i.e. adjacent circuit, AC power lines and disturbances from electrostatic and electromagnetic couplings) and internal sources (i.e. random fluctuations affecting carrier transport and carrier concentration in electric devices). The former can be removed by proper shielding, filtering and circuit design. However, the latter combines intrinsic and process–induced effects, and cannot be fully eliminated. It must be minimized for enhancing the

accuracy of measured signals. In addition, the internal low frequency noise is considered as an important concern in analog circuits and systems since small signal for operating circuits and systems should be larger than internal low frequency noise. Thus, the importance of low frequency noise analysis increases with shrinking devices. It becomes an increasingly important concern and source of dynamic variability for coming technology nodes. Conversely, low frequency noise characterization can be used as a diagnostic tool for the quality of interface layer in MOSFET configurations. It is therefore an important effect to characterize.

Fig. 2.9(a) illustrates the concept of current noise in electronic systems. When we measure current during certain time (i.e.  $I(t)$ ), there is a random fluctuation of current around the average value. It can be derived as

$$I(t) = I_{\text{avg}} + I_{\text{flu}}(t) \quad (2.28)$$

where  $I_{\text{ave}}$  and  $I_{\text{flu}}(t)$  stand for the average bias current and current fluctuation. The fast Fourier transform (FFT) is usually applied to convert noise signal from time domain to frequency domain for clearer and better noise characterization. After Fourier transform, the noise can be represented by the variation of its Power Spectral Density (PSD) with frequency as shown in Fig. 2.9(b). In addition, Fig. 2.9(b) displays the power spectral densities (PSDs) of various fundamental noise sources (i.e. low frequency noise and white noise) [18]. The low frequency noise can be understood as the superposition of  $1/f$  noise (of flicker noise) with generation–recombination (g–r) noise. These will be dealt with in following section. For the accurate noise measurement, proper shielding is needed and a battery is typically used for avoiding 60Hz or 50Hz interferences from an AC power supply.



**Figure 2.9** (a) A measured current with fluctuation and (b) various power spectral densities with different noise sources

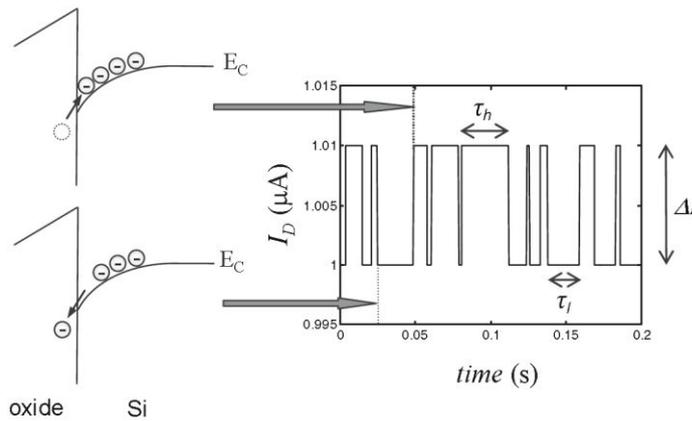
### 2.3.1 Fundamental noise sources

#### 2.3.1.1 Thermal noise

The thermal noise (i.e. Johnson or Nyquist noise) is generated by the random thermal motion of electrons in materials. As predicted, it is closely related to temperature. The thermal noise always exists as the back-ground noise except at  $T=0K$ . In addition, it does not have frequency dependence in the range of low-frequency, so we call it as the white noise. The current (voltage) power spectral density (PSD) of thermal noise is defined as;

$$S_I = \frac{4kT}{R} \text{ (or } S_V = 4kTR) \quad (2.29)$$

where  $R$  and  $kT$  are resistance of device under test and thermal energy. The thermal noise defines the minimum level of measurement for an electronic circuit.



**Figure 2.10** A schematic illustration of the two-level RTS noise mechanism and drain current

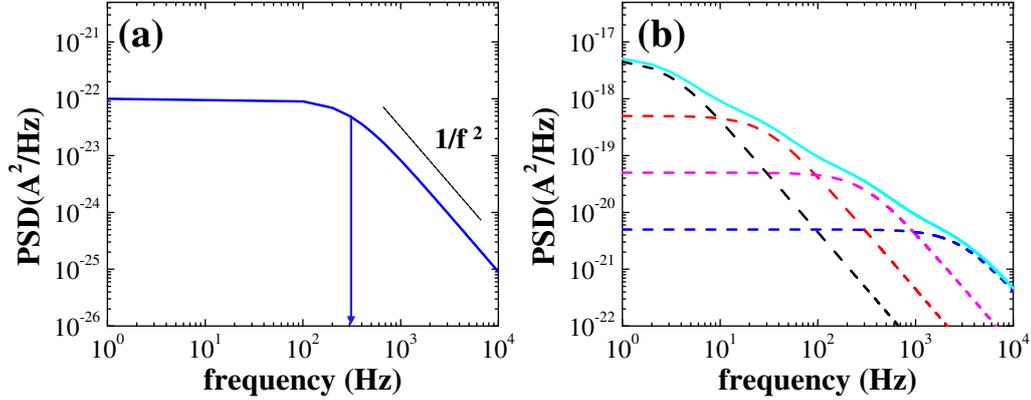
#### 2.3.1.2 Random-Telegraph-Signal (RTS) noise

The RTS noise originates from carrier trapping and de-trapping of free carriers by a small number of traps. Thus, it is typically observed in devices with very small area (~less than  $1\mu m^2$ ). Because the RTS noise behavior in the time domain has discrete properties, it is also called as burst or popcorn noise. Fig. 2.10 shows how current varies with time in the presence of strong RTS noise [18]. For two-level RTS noise [19], the PSD can be derived as

$$S_I = \frac{4(\Delta I)^2}{(\tau_l + \tau_h)[(1/\tau_l + 1/\tau_h)^2 + (2\pi f)^2]} \quad (2.30)$$

where  $\Delta I$ ,  $\tau_l$  and  $\tau_h$  are amplitude of current variation, Poisson distributed time duration in the

lower state and in high state, respectively. The PSDs of g–r noise and RTS noise exhibit a Lorentzian behavior as shown in Fig. 2.11(a). The g–r noise can be thought as a sum of RTS noise sources with identical time constants. From the RTS noise characterization, we can study the trap energy level, capture and emission kinetics and spatial location of the traps.



**Figure 2.11** (a) A conventional PSD of RTS noise and (b) superposition of  $1/f^2$ , Lorentzian curves with different time constants,  $\tau$  [18]

### 2.3.1.3 1/f noise (flicker noise)

The noise which has  $1/f^\gamma$  frequency dependence ( $\gamma$  being usually in the range of 0.7 to 1.3) is called 1/f noise or flicker noise. The PSD of 1/f noise can be expressed as

$$S_I = \frac{K \cdot I^\beta}{f^\gamma} \quad (2.31)$$

where  $K$  is a constant and  $\beta$  is an exponent of current. The 1/f noise has been detected in metals and conventional MOSFETs in the range of low frequency from  $10^{-5}$ Hz to  $10^7$ Hz [18]. Two main models have been proposed to explain 1/f noise behavior: Hooge mobility fluctuation (or carrier mobility fluctuation) and carrier number fluctuation. In addition, the latter model has been further developed by Gerard Ghibaudo [20] to include mobility fluctuations correlated to carrier number fluctuations.

#### Hooge mobility fluctuation model

The Hooge mobility fluctuation (HMF) is originated from phonon scattering or lattice vibration [21]. Following Hooge's empirical model:

$$\frac{S_I}{I_d^2} = \frac{q\alpha_H}{fWLQ_1} \quad (2.32)$$

where  $Q_i$  is the inversion or mobile charge carrier density and  $\alpha_H$  is the Hooge parameter, which was firstly considered as constant. But it was revealed that  $\alpha_H$  was dependent with modifications of channel position under the gate oxide with bias, due to changes in the probability of the different scattering mechanisms. In the linear regime of MOSFET operation, Eq. 2.32 can be developed as

$$\frac{S_I}{I_d^2} = \frac{q\alpha_H}{fWLC_{ox}(V_{gs} - V_T)} = \frac{q\alpha_H\mu_{eff}V_{ds}}{fL^2I_{ds}} \quad (2.33)$$

The normalized current PSD of HMF model is proportional with drain current and voltage. This remarkable property makes it easy to distinguish Hooge's mobility fluctuation model from the carrier number fluctuation model presented below. Even though the HMF model is not strongly supported theoretically with physical principles, it has pretty well described the low frequency noise behavior of pMOSFETs [22] and of some nanomaterials such as CNTs and graphene [23,24].

### Carrier number fluctuation with correlated mobility fluctuation model

Another model for giving an account of a  $1/f$  noise behavior is the carrier number fluctuation which is based on the trapping and de-trapping of charge carriers at the interface between the channel and neighboring  $SiO_2$  layers. It is worth noting that the PSD of  $1/f$  noise can be generated mathematically by the superposition of  $1/f^2$ , Lorentzian curves with different time constants,  $\tau$ . The physical principles of CNF model were suggested by McWorther in 1957 [25]. He inferred that the  $1/f$  noise behavior was the result of the fluctuation of carrier number associated with quantum mechanical tunneling transitions of the electrons between the channel and uniformly distributed traps in the gate dielectrics [18, 25]. To account for mobility fluctuation caused by trapped charges, the carrier number fluctuation with correlated mobility fluctuation model was introduced in 1991 [20].

The carrier number fluctuation by oxide charge fluctuation can be regarded as the flat band voltage fluctuation in the MOSFET configuration:

$$\delta V_{fb} = -\delta Q_{ox} / \delta C_{ox} \quad (2.34)$$

By adding mobility fluctuation  $\delta\mu_{eff}$ , the current fluctuation can be derived as

$$\delta I_d = \delta V_{fb} \frac{\partial I_d}{\partial V_{fb}} + \delta\mu_{eff} \frac{\partial I_d}{\partial \mu_{eff}} \quad (2.35)$$

Since  $g_m = \partial I_d / \partial V_{gs} = -\partial I_d / \partial V_{fb}$  and  $1/\mu_{\text{eff}} = 1/\mu_{\text{eff0}} + \alpha Q_{\text{tot}}$  where  $\alpha$  is the Coulomb scattering coefficient ( $\sim 10^4$  C/Vs for electrons) [26], Eq. 2.35 can be developed as

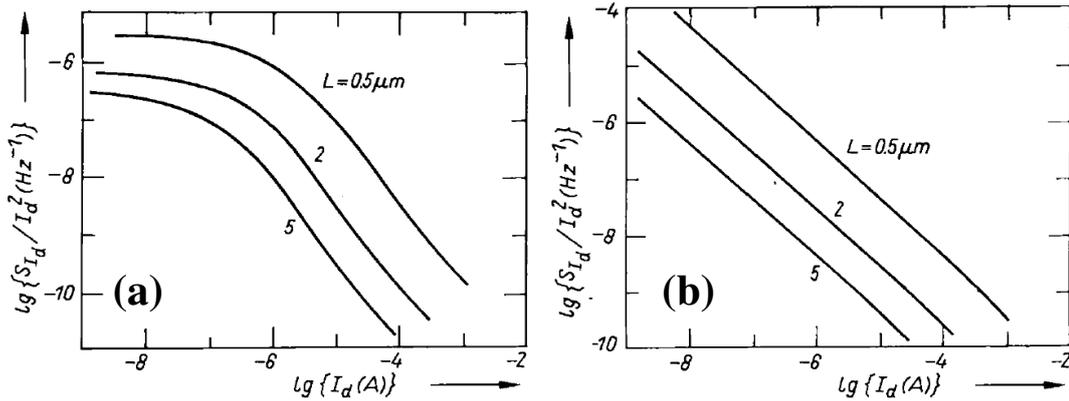
$$\delta I_d = -[1 + \alpha \mu_{\text{eff}} C_{\text{ox}} \frac{I_d}{g_m}] g_m \delta V_{fb} \quad (2.36)$$

Finally, the normalized current PSD of carrier number fluctuation with correlated mobility fluctuation model can be defined as

$$\frac{S_{I_d}}{I_d^2} = S_{V_{fb}} [1 + \alpha \mu_{\text{eff}} C_{\text{ox}} \frac{I_d}{g_m}] \frac{g_m^2}{I_d^2} \quad (2.37)$$

Where  $S_{V_{fb}}$  is the flat band voltage spectral density:

$$S_{V_{fb}} = \frac{q^2 k T \lambda N_t}{W L C_{\text{ox}}^2 f} \quad (2.38)$$



**Figure 2.12** Theoretical calculations of PSD curves with (a) the carrier number fluctuation with correlated mobility fluctuation model and (b) the Hooge mobility fluctuation model [20]

In Eq. 2.38,  $N_t$  and  $\lambda$  stand for the surface trap density and the tunneling attenuation distance ( $\sim 0.1$  nm for  $\text{SiO}_2$ ). Fig. 2.12(a) shows the PSD of carrier number fluctuation with correlated mobility fluctuation model [20]. Unlike Hooge mobility fluctuation in Fig. 2.12(b), the saturation in weak inversion regime is found.

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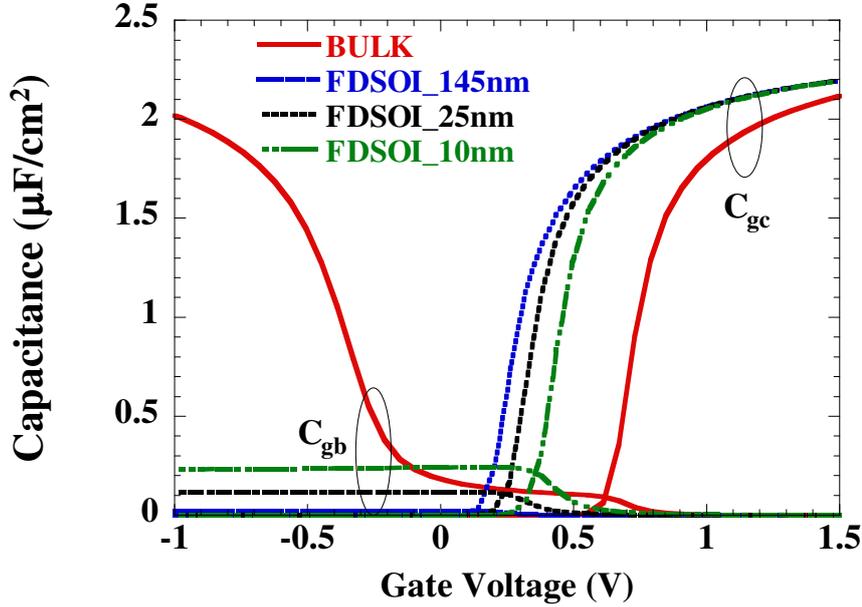
# Chapter 3

## Full split C–V method for parameter extractions

### 3.1 Introduction

Advanced FDSOI CMOS technology is on the way to intercept the 22/20nm node and below, which can be one of the alternative ways to the low power / high speed design within the timescales required by the semiconductor industry [1]. In addition, ultra-thin body and BOX (UTBB) architecture allows full use of static and dynamic back plane (BP) biasing opportunities, such as bias-engineered multi- $V_{th}$  strategy [2,3]. However, with strong scaling, methodologies of parameter extraction from electrical characterization need to be adapted. The split C–V technique has been one of the reliable conventional methods for electrical characterization, initially developed for bulk CMOS [4,5]. The gate-to-channel capacitance ( $C_{gc}$ ) and gate-to-bulk capacitance ( $C_{gb}$ ) were then used together to extract electrical parameters such as substrate doping level, threshold voltage ( $V_{th}$ ) and flat-band voltage ( $V_{fb}$ ) [5,6]. However, in thick BOX SOI technology,  $C_{gb}$  could not be exploited any more as it had become too small (Fig. 3.1). The parameter extraction in FDSOI has thus been relying only on  $C_{gc}$  [7], with recent improvement allowing  $V_{th}$ ,  $V_{fb}$ , equivalent oxide thickness (EOT,  $T_{ox}$ ) and body thickness ( $T_{si}$ ) to be extracted [8,9].

### 3.2 Experiment details

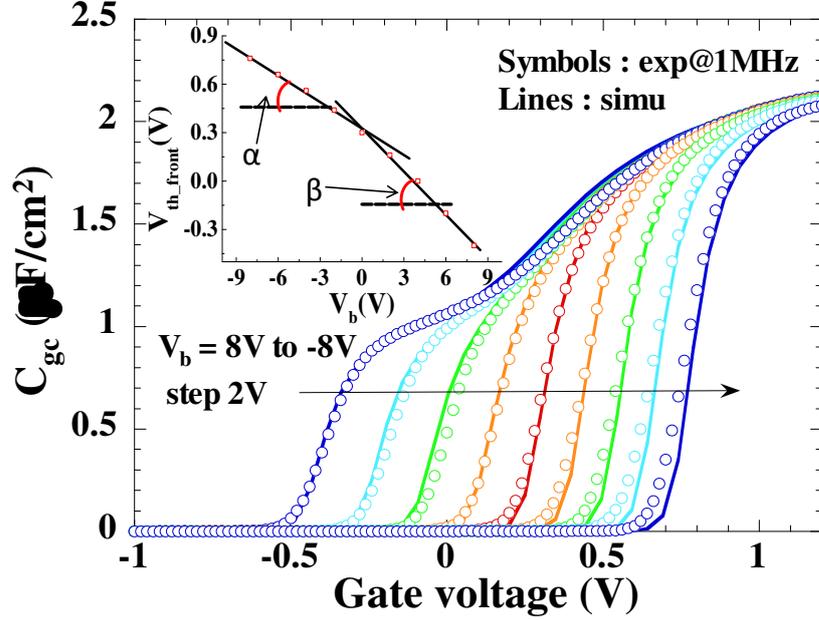


**Figure 3.1** TCAD simulated  $C_{gc}(V_{gs})$  and  $C_{gb}(V_{gs})$  characteristics of Bulk and FDSOI nMOS devices with various BOX thicknesses. Other parameters:  $T_{ox}=1.4\text{nm}$ ,  $T_{si}=7\text{nm}$  (FDSOI),  $T_{sub}=100\text{nm}$  (BULK) and  $N_a = 10^{17}\text{cm}^{-3}$  (BULK).

The devices under study were UTBB FD-SOI MOSFETs provided by ST Microelectronics (14nm-node technology). The description of DUT was explained in Chapter 1.4 and the detail information can be found elsewhere [3]. For capacitance measurements, we considered large devices with  $10\mu\text{m}$  gate mask length and  $1\mu\text{m}$  channel width. The C-V measurements were carried out using HP4294A impedance-meter with a 40mV small signal at 1MHz. The  $C_{gc}$  was measured with standard procedure with additional back-biasing on BP ( $V_b$ ) [4,5]. For the  $C_{gb}$  measurement, the “high” and “low” terminals were connected to gate and BP electrodes, respectively, whereas source and drain electrodes were grounded. In order to study back biasing effect on  $C_{gb}(V_g)$ , common bulk configuration was used, unlike in  $C_{gc}$  mode. So, instead of applying DC bias to back side, the BP was set to zero and we changed source/drain ( $V_s$ ) and gate ( $V_g$ ) bias, keeping  $V_{bs}=V_b-V_s$  constant. The threshold voltage  $V_{th}$  was extracted from the location of the maximum derivative of  $C_{gc}(V_{gs})$  curves. In addition, the FDSOI stack was simulated in 1D (like in Fig. 3.1) using the finite element method with FlexPDE 5.0 software in order to validate our extraction procedure.

### 3.3 Results and Discussions

#### 3.3.1 Refinement of gate-to-channel capacitance analysis



**Figure 3.2** Experimental and simulated values of  $C_{gc}$  (symbols and lines, respectively) as a function of front gate voltage, with back bias  $V_{bs}$  as a parameter. Inset:  $V_{th\_front}(V_{bs})$  and front to back coupling factors ( $\alpha$  and  $\beta$ ).

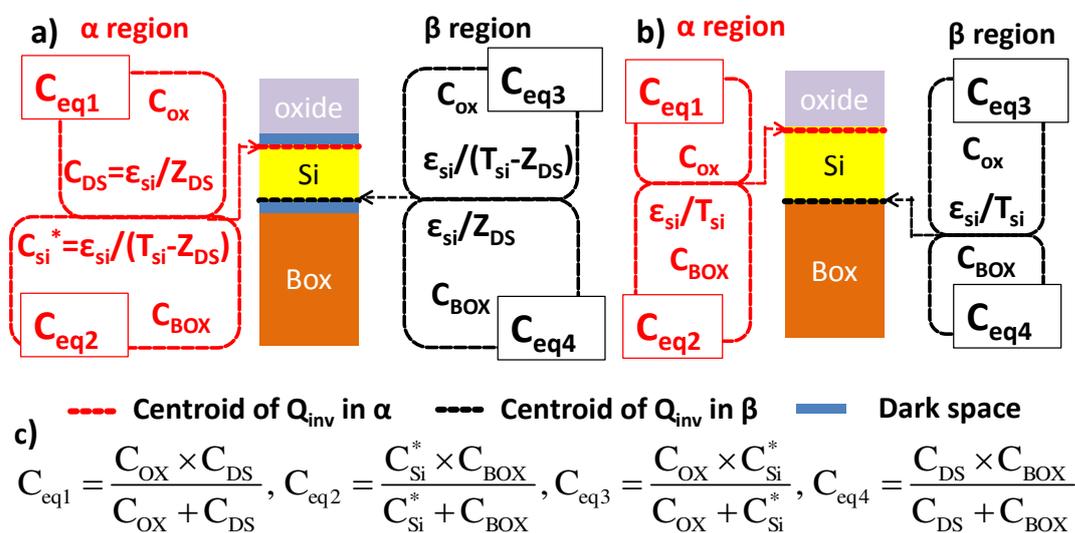
Fig. 3.2 shows typical experimental  $C_{gc}(V_{gs})$  curves with back bias as a parameter. The capacitive coupling between front and back interfaces is clearly observed by plotting  $V_{th}(V_{bs})$  curve (insert of Fig. 3.2).  $T_{ox}$  can directly be extracted from the maximum of  $C_{gc}$  and  $T_{si}$  estimated from the shoulder which is clearly visible for  $V_b=8V$ . In order to analyze this behavior, TCAD simulations were performed to solve Poisson equation. In the simulations, Hanch's correction was introduced to account for quantum confinement effects [10]. Simulation results (lines in Fig. 3.2) reproduced  $C_{gc}(V_{gs})$  experimental data very well (symbols in Fig. 3.2). Starting from previously extracted values, a slight adjustment of geometrical parameters such as  $T_{ox}$  and  $T_{si}$  was sufficient to obtain best fit (results on Table 3.1).

Beyond that, we developed a compact model to describe capacitive coupling effects in such UTBB stacks. The front-to-back threshold voltage coupling model developed by Lim and Fossum for FDSOI [7] is the basis of the most widely used methods to extract body and BOX thicknesses [9]. However, in UTBB SOI devices, the dark-space at front interface is no longer negligible compared to  $T_{si}$ . With an UTBOX, this correction becomes mandatory as well at the back interface. Accordingly, we propose an improved interface coupling model, described in

Fig. 3.3(a-c), which accounts for dark-space thickness ( $Z_{DS}$ ) at both interfaces. We used the standard value for dark-space thickness in Silicon (i.e.  $Z_{DS} \approx 1.2\text{nm}$ ) [10]

Parameter	Simulation inputs		Extracted values from experimental curves with improved coupling model	
	Fit of $C_{gc}(V_{gs})$ curves	Fit of $C_{gb}(V_{gs})$ curves	From $C_{gc}$ curves	From $C_{gb}$ curves
$T_{ox}$ (nm)	1.43		1.43	-
$T_{si}$ (nm)	6.8		6.5	-
$T_{BOX}$ (nm)	30	32	31.5	-
$T_{BP}$ (nm)	100		-	-
$Z_{DS}$ (nm)	1.2		-	-
$N_{BP}$ ( $\text{cm}^{-3}$ )	$1.1 \times 10^{18}$		-	$1.0 \times 10^{18}$
$V_{fb,b}$	-		-	-0.47
$V_{fb}$	-0.27		-	-

**Table 3.1** Optimized parameters used in TCAD simulations with N type BP and Extracted results from  $C_{gc}$  and  $C_{gb}$  measurement.

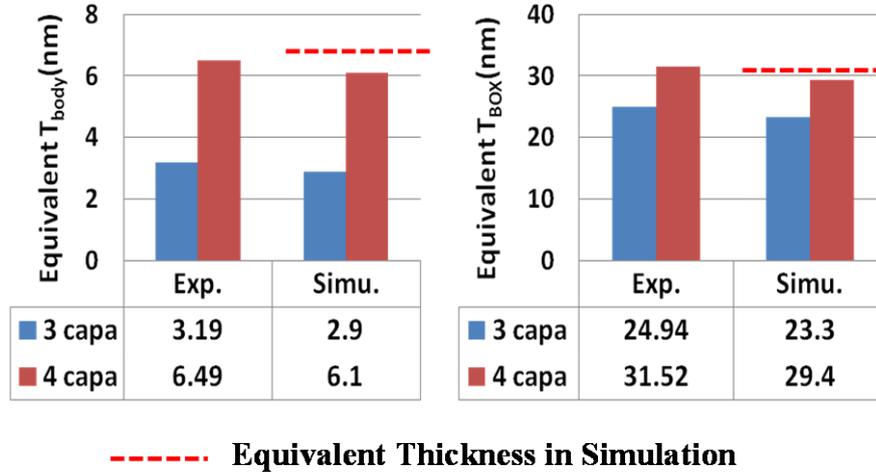


**Figure 3.3** a) Improved and b) conventional capacitance model for interface coupling effect. For NMOS,  $\alpha$  regime: reverse bias on back gate, back interface is depleted;  $\beta$  regime: forward bias on back gate, back interface is inverted. These regimes are shown in the insert of Figure 3.2. In the conventional model,  $Z_{DS}=0$ . c) Equations for improved model.

The front-to-back coupling factors are obtained from the slopes of  $V_{th}(V_{bs})$  characteristic (insert of Fig. 3.2). They are equal to  $\alpha = -C_{eq2}/C_{eq1}$  and  $\beta = -C_{eq4}/C_{eq3}$ , where the capacitances are defined in Fig. 3.3(a-c). By solving these 2 equations,  $T_{si}$  and  $T_{BOX}$  were expressed as a function of  $T_{ox}$  as:

$$T_{Si} = \frac{(2\beta - \frac{1}{\alpha} - 1)Z_{DS}\epsilon_{ox} + (1 - \frac{\beta}{\alpha})T_{ox}\epsilon_{Si}}{(\beta - 1)\epsilon_{ox}}, T_{BOX} = \frac{(\beta - \frac{1}{\alpha})Z_{DS}\epsilon_{ox} + (1 - \frac{1}{\alpha})T_{ox}\epsilon_{Si}}{(1 - \beta)\epsilon_{ox}} \quad (3.1)$$

The  $\alpha$  and  $\beta$  values were extracted both from characterization results and from TCAD simulation data.  $T_{ox}$  was obtained from the maximum capacitance in inversion, corrected from quantum dark space. Then,  $T_{si}$  and  $T_{BOX}$  were computed from coupling factors, using either Eq. 3.1 or the conventional method [7,9]. We applied our model both to simulated and experimental CV characteristics. As it is clear from Fig. 3.4, the values extracted with our new capacitance model are much closer to the physical parameters (equivalent thickness) used in TCAD simulation, demonstrating its superiority over conventional methods for UTBB FDSOI.



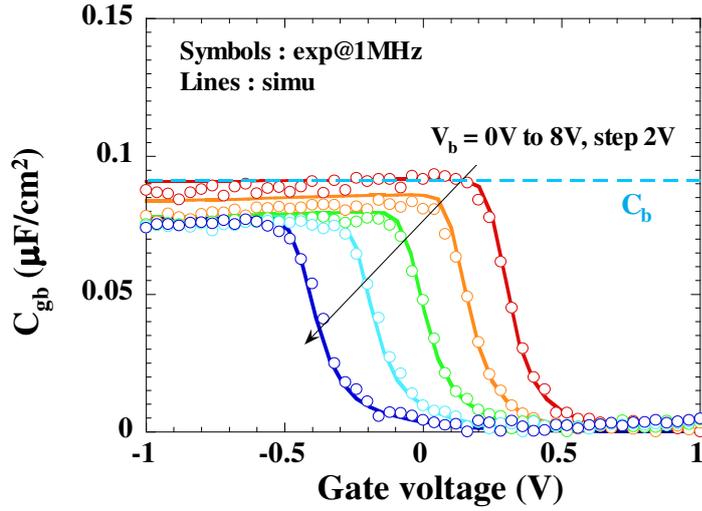
**Figure 3.4**  $T_{si}$  and  $T_{BOX}$  values extracted from experiment and from simulation. "4 capa": improved model, "3 capa": conventional model of [7,9].

### 3.3.2 Gate-to-bulk capacitance exploitation in UTBB FDSOI

Hereafter, we report, for the first time,  $C_{gb}(V_{gs})$  measurement consistently performed on advanced FDSOI devices (Fig. 3.5). As in bulk devices (Fig. 3.1), the  $C_{gb}$  cancels out when  $C_{gc}$  increases, due to screening by the growing inversion layer [4,5]. However, contrary to bulk,  $C_{gb}$  remains constant in depletion and does not reach its accumulation value. This is due to the absence of AC response of holes in such FDSOI n-type devices. Therefore, if substrate or BP

doping concentration is sufficiently high ( $>10^{18}\text{cm}^{-3}$ ), the maximum value of  $C_{gb}$  for zero back bias ( $C_b$ ) corresponds to the series capacitances between gate and substrate so that  $C_b=(1/C_{ox}+1/C_{si}+1/C_{BOX})^{-1}$ . From the  $C_b$  value, one can roughly estimate equivalent BOX thickness since  $C_{BOX}$  is much smaller than  $C_{si}$  and  $C_{ox}$ . The plateau value variation with  $V_{bs}$  allowed doping type and concentration to be extracted (Fig. 3.5). This had never been tried until now.

**Figure 3.5**  $C_{gb}$  as a function of gate voltage, with back bias  $V_{bs}$  as a parameter. Experiments (symbols) and simulation (lines). Dashed line:  $C_b$ .

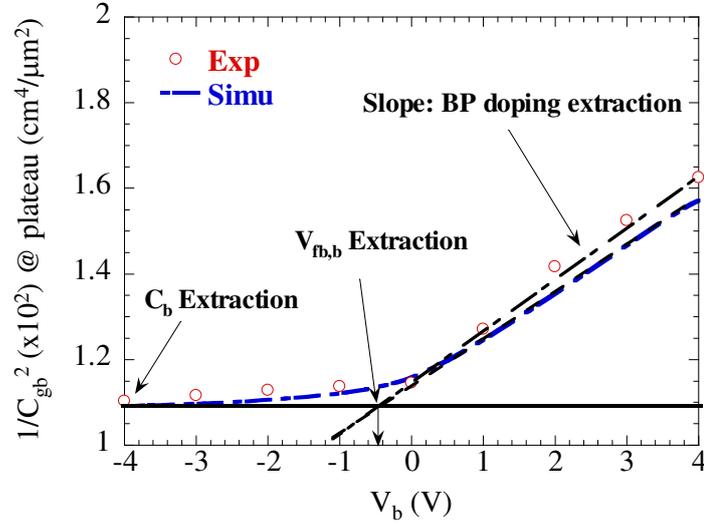


As shown in Fig. 3.5, the simulation of  $C_{gb}$  was also well calibrated with experimental results. Here, we supposed that the thickness of the doped back plane region,  $T_{BP}$ , was thick enough to allow a neutral zone to remain when back gate boundary bias condition was applied. The parameters used in  $C_{gb}$  simulation (see Table 3.1) were the same as for  $C_{gc}$ , except for  $T_{BOX}$  (2 nm difference). This  $T_{BOX}$  value is now closer to the value extracted from the capacitance model of Eq. 3.1. This indicates that  $C_{gb}$  analysis is well suited for  $T_{BOX}$  extraction. Note that the back biasing effect was also very well reproduced.

Moreover, since forward back biasing modulates the space charge in the BP, as in bulk structures, it can be used to probe the silicon substrate. Therefore, like in bulk devices, the standard C–V technique can be applied for BP flat–band voltage ( $V_{fb,b}$ ) and doping concentration ( $N_d$ ) extraction [6]. Fig. 3.6 plots  $1/C_{gb}^2$  at plateau versus  $V_{bs}$ , from BP accumulation to depletion regime. In depletion, the slope of  $1/C_{gb}^2$  and intercept with x–axis can give direct information about BP doping  $N_d$  and about  $V_{fb,b}$ , in agreement with Eq. 3.2 [6]:

$$\frac{1}{C_{gb}^2} = \frac{1}{C_b^2} + \frac{2}{qN_d\epsilon_{si}} \cdot (V_{bs} - V_{fb,b}) \quad (3.2)$$

Table 3.1 summarizes the input parameters which allowed consistent fitting of all experimental results.



**Figure 3.6**  $1/C_{gb}^2$  as function of  $V_{bs}$ . Values obtained from experiments (symbols) and simulation (lines).  $C_{gb}$  values are taken at plateau, before screening by  $C_{gc}$ . This plot enables extraction of BP doping level and  $V_{fb}$  at back gate in the BP depletion regime, and extraction of  $C_b$  in accumulation regime (Eq. 3.2).

The very good match between simulated ( $1.1 \times 10^{18} \text{cm}^{-3}$ ) and extracted ( $1 \times 10^{18} \text{cm}^{-3}$ ) values of BP doping level confirms the validity of the extraction procedure. Moreover, the  $C_b$  value ( $=0.095 \mu\text{F}/\text{cm}^2$ ) evaluated from  $C_{gb}$  curve is from  $C_{gc}$  coupling ratio analysis ( $=0.098 \mu\text{F}/\text{cm}^2$ ) in previous section, which was, however, obtained indirectly and with a more complex extraction procedure.

### 3.4 Conclusions

In this chapter, we successfully demonstrated extensive split C–V characterization with interface coupling for ultra–thin BOX FDSOI devices, enabling parameter extraction for the full stack, from back plane to front gate in a reliable and fully consistent way. In addition, it was shown that  $C_{gb}$  configuration in FDSOI devices does provide complementary information on BP doping level, which is not available in  $C_{gc}$  mode, and more direct evaluation of  $C_b$ . By using well calibrated simulation and an improved coupling capacitance model, we also increased the reliability of the extracted parameters. This new parameter extraction methodology can be very useful to directly assess full stack information in UTBB FDSOI structures without destructive analysis.

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# Chapter 4

## In depth characterization of carrier transport in 14nm FD-SOI CMOS transistors

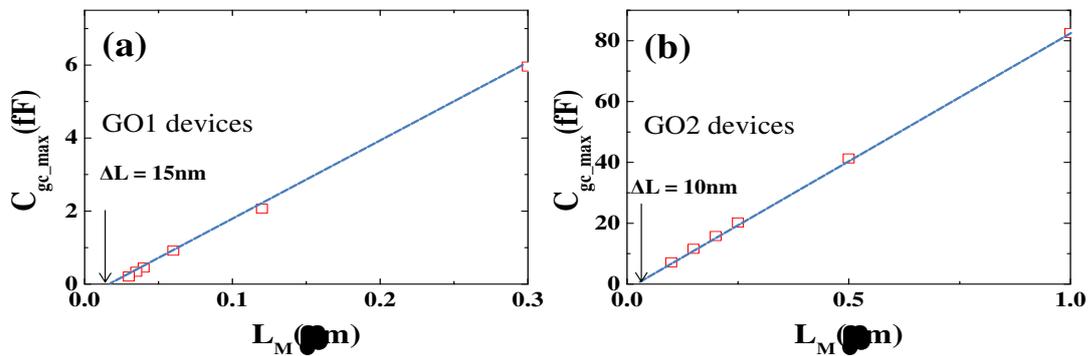
### 4.1 Introduction

Ultra-thin body and BOX (UTBB) fully depleted silicon-on-insulator (FD-SOI) devices are among the most promising candidates for future CMOS technology nodes since they offer excellent electrostatic integrity, high performance and low variability [1]. In addition, there provide interesting potentialities such as the usage of static and dynamic back plane (BP) biasing engineering in UTBB architecture, which makes it possible to exploit multi- $V_T$  strategies with a planar implementation [2]. To continue CMOS downscaling with high performance in FD-SOI devices, high- $k$  and metal gate have been also introduced for smaller equivalent oxide thickness (EOT) and less gate leakage current. Carrier transport properties of ultra-scaled devices are affected by severe downscaling and by the presence of the high- $k$  layer, which technological progress remains despite the fact that it is defective compared to  $\text{SiO}_2$ . Moreover, in order to increase hole mobility, a Silicon-Germanium (SiGe) layer has been used in PMOS devices instead of pure Si channel. In these complex FD-SOI devices which combine high- $k$  dielectric, ultra-small dimensions and SiGe alloy in the channel, it is important to investigate transport properties to get deeper insight of their operation mechanisms.

In this chapter, we extensively characterized both NMOS and PMOS UTBB FD-SOI devices at low temperature. At first, we investigated the influence of the high- $k$  layer for electron transport characteristics in long channel NMOS devices, where the channel is long enough to avoid lateral defects associated to S/D regions. The transport properties depending on temperature were investigated for revealing the origin of additional mobility related with high- $k$  layers since it is expected that surface optical phonon (SOP) or/and remote Coulomb scattering (RCS) can be present due to the high polarizability inherent to high- $k$  materials and their larger density of defects compared to SiO<sub>2</sub> in high- $k$  dielectric stacks. Then, we focused on short channel devices and demonstrated how dominant transport scattering mechanism varied with decreasing channel length. Finally, the mobility enhancement obtained by introducing Ge incorporation in long channel PMOS devices was proven with various Ge concentrations before detailed analysis of the influence of Ge in short channel devices.

## 4.2 Experiment details

The devices under study were UTBB FD-SOI MOSFETs provided by ST Microelectronics (14nm-node technology). The description of DUT was explained in Chapter 1.4 and the detail information can be found elsewhere [3,4]. I-V measurements were carried out using HP4156b with a cryogenic probe station. In addition, the C-V measurements were taken out from HP4294A impedance-meter with a 40 mV small signal at 1MHz. The gate-to-channel capacitance ( $C_{gc}$ ) was measured by connecting “high” terminal to gate electrode and “low” terminal to source/drain electrodes.

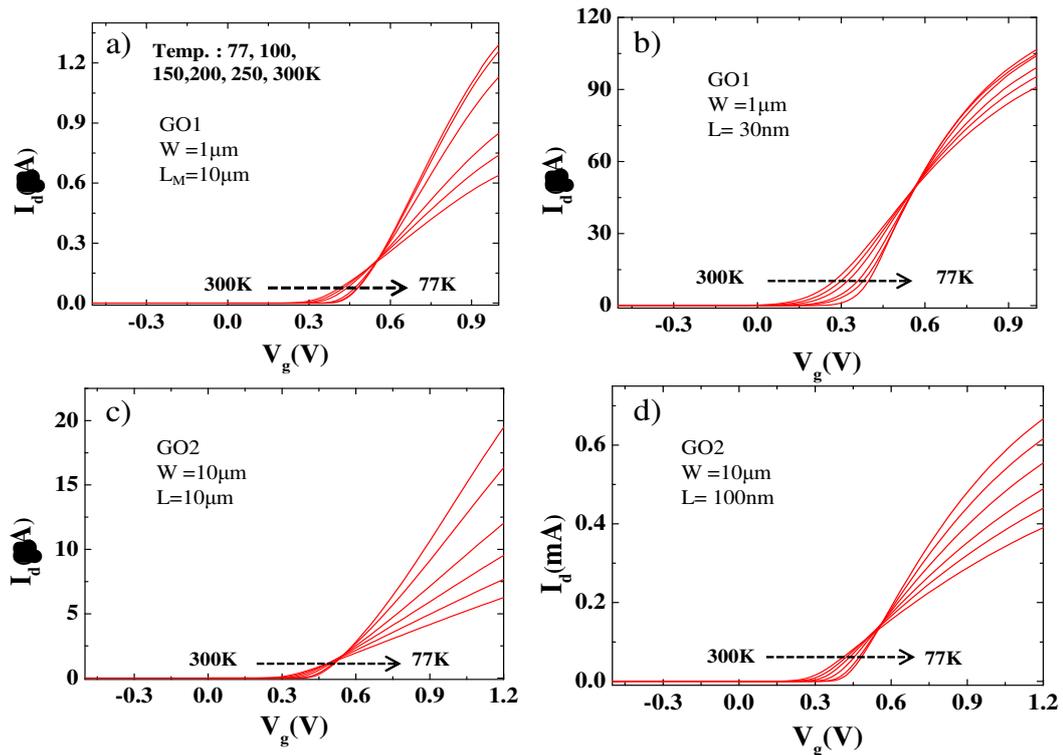


**Figure 4.1** Extraction of effective channel length using extrapolation of  $C_{gc}$  at  $V_{gs}=1\text{V}$  to zero channel length.  $\Delta L$  for (a) GO1 ( $W=1\mu\text{m}$ ) and (b) GO2 ( $W=10\mu\text{m}$ ) devices were  $\sim 15\text{nm}$  and  $\sim 10\text{nm}$ , respectively.

At first, for the precise evaluation of transport properties, we extracted effective channel length ( $L_{eff}$ ) using gate-to-channel C-V measurement ( $C_{gc}$ ). Indeed, there is discrepancy between effective channel length and physical gate length due to source/drain contact processing, while physical gate length itself is different from on-mask gate length because of lithography / etching processes. To do so, the  $C_{gc}$  value measured in the strong inversion regime ( $V_{gs}=1V$ ) was plotted in Fig. 4.1 as a function of  $L_M$  after having eliminated the parasitic capacitance, estimated from the minimum value of  $C_{gc}$  in accumulation regime [5]. The  $\Delta L$  ( $=L_M-L_{eff}$ ) values were extracted by extrapolation to zero channel length [5,6]. Extracted  $\Delta L$  values were around 15nm and 10nm for GO1 and GO2 devices, respectively.

### 4.3 Results and Discussions

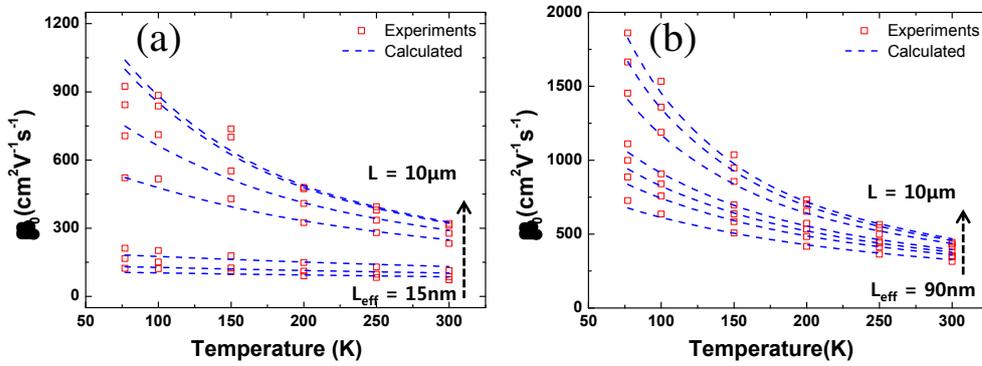
#### 4.3.1 General transport characteristics of NMOS devices and methodologies



**Figure 4.2** Typical drain current of (a,b) GO1 and (c,d) GO2 devices as a function of  $V_{gs}$  with temperature varying in the range of 77K-300K. Drain voltage was 20mV for linear regime operation.

Fig. 4.2 displays the typical I-V characteristics obtained for our devices, with the longest and shortest gate length, and with GO1 and GO2 stacks. Temperature ranged from 77K

to 300K and drain voltage ( $V_{ds}$ ) was equal to 20mV. As is standard bulk MOS transistors, the transfer curves show the conventional behavior, with mobility and threshold voltage ( $V_T$ ) increase as temperature decreases. Also, a common intersection point was found for all the devices at the bias which corresponds to the so-called zero-temperature coefficients (ZTC). At this point, the drain current is independent of temperature due to the mutual compensation of mobility and  $V_T$  change with temperature, like in standard bulk Si MOSFETs. In order to further investigate how transport characteristics is affected by the different gate-dielectric stacks and by channel length variation in the low temperature range, we extracted low field mobility ( $\mu_0$ ) with the Y-function method ( $Y=I_d/g_m^{0.5}$ ) [7].



**Figure 4.3** Temperature dependence of low field mobility ( $\mu_0$ ) for both (a) GO1 and (b) GO2 devices with various channel length. The empirical model (blue dot line) was used in order to find mobility contribution related to phonon, Coulomb and neutral defect scattering according to their temperature dependence, which was well fitted with experimental results.

Fig. 4.3 demonstrates that  $\mu_0$  increases as temperature decreases in almost all the devices, for both GO1 and GO2, regardless of gate oxide. However, for the ultimately scaled-down devices, the temperature dependence of  $\mu_0$  became very small unlike for long channel devices. In addition, a strong mobility reduction was observed in sub-100nm devices. Thus, it seems that transport properties are changed as channel length decreases.

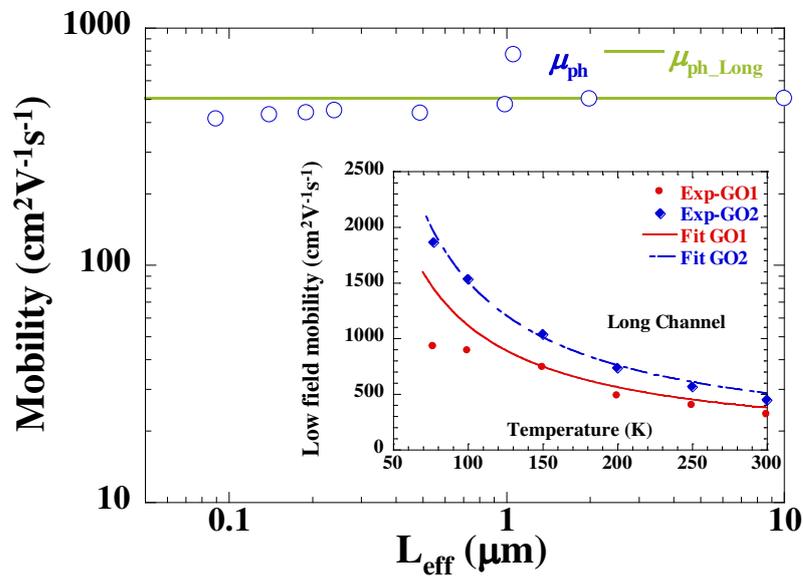
In order to get a quantitative analysis of mobility dependence with temperature, we used the empirical model of [8]:

$$\frac{1}{\mu_0} = \frac{1}{\frac{300}{T} \cdot \mu_{ph}} + \frac{1}{\frac{T}{300} \cdot \mu_C} + \frac{1}{\mu_{nd}} \quad (4.1)$$

which is based on Matthiessen's rule and includes three terms corresponding to scattering with

phonons, fixed charges (Coulomb scattering) and neutral defects ( $\mu_{ph}$ ,  $\mu_C$  and  $\mu_{nd}$ , respectively). As known in Eq. 4.1, the phonon scattering mobility term varies with the inverse of temperature, while Coulomb scattering mobility term varies proportionally to temperature. Moreover, neutral defect scattering is independent with temperature, but it has shown strong channel length dependence in the literature [8–10]. Using this model, we were able to reproduce quite well the general trend of mobility variation with temperature (Fig. 4.3). In this fitting procedure, the fitting values for  $\mu_{ph}$  were almost independent of channel length as shown in Fig. 4.4. This is consistent with [8–10].

#### 4.3.1.1 Comparative investigation with different gate oxides in long channel devices

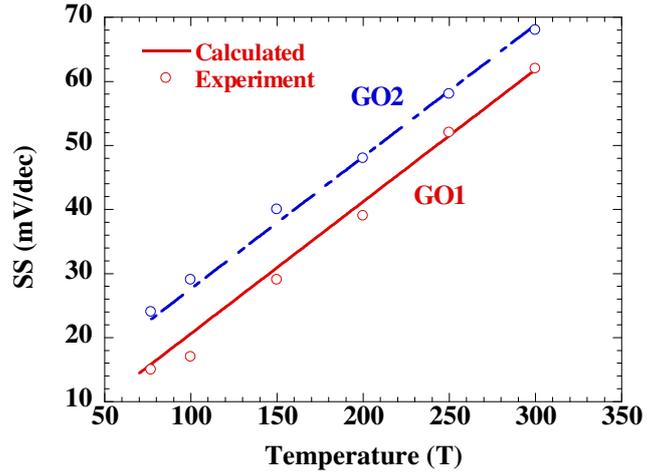


**Figure 4.4** Evolution with gate length of  $\mu_{ph}$  in GO2 devices (symbols) and comparison with its value for the longest channel (horizontal line). Inset: Temperature dependence of long channel  $\mu_0$  (symbols) fitted with the sole contribution of phonon mobility contribution (lines) for GO1 and GO2 devices.

Before analyzing the transport properties variation depending on channel length, we will first focus on mobility behavior in the long channel devices ( $L=10\mu\text{m}$ ) with different gate oxides, since the long devices are more adequate to analyze how carrier transport depends on gate dielectrics. The fitting of mobility temperature dependence with the sole contribution of phonon scattering shows good agreement with experimental results in GO2 devices as shown in the inset of Fig. 4.4. This means that mobility in GO2 devices is consistent with the universal mobility in silicon [11]. So, transport in GO2 devices can be used as our reference. In contrast, with the GO1 stack, it is no more possible to fit experimental results with phonon scattering only. A deviation is observed at low temperature. In other words, the phonon contribution is not

sufficient to explain the temperature dependency of mobility and we must consider an additional scattering contribution for GO1 devices. In the following paragraphs, we will analyze the gate control ability and high-k layer induced mobility behavior in sub-threshold and inversion regimes, separately.

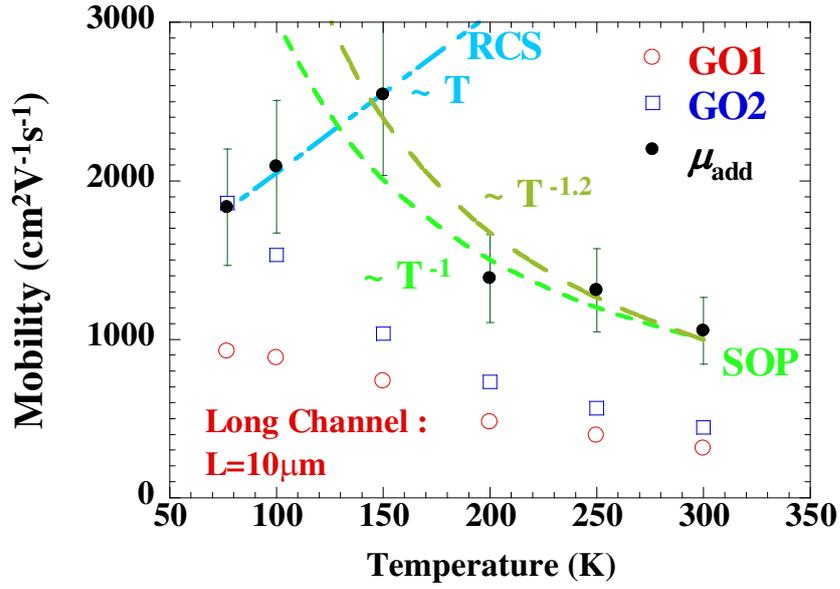
**Figure 4.5** Temperature variation of sub-threshold swing (symbols) and theoretical fitting curves (lines) allowing extraction of back and front interface trap density



At first, we investigated device operation in the sub-threshold regimes and extracted sub-threshold swing (SS) for different temperature and gate oxides as seen in Fig. 4.5. The SS has been used to extract the density of fast interface states which can contribute to Coulomb scattering at the silicon/oxide. For quantitative and detail analysis, we extracted the fast interface trap density ( $D_{it}=C_{it}/q$ ) from the variation of SS depending on temperature following [12]:

$$SS = 2.3 \frac{kT}{q} \left[ 1 + \frac{C_{itf}}{C_{ox}} + \frac{C_{si} \cdot C_{BOX}}{C_{ox} (C_{si} + C_{BOX} + C_{itb})} \left( 1 + \frac{C_{itb}}{C_{BOX}} \right) \right] \quad (4.2)$$

where  $C_{itf}$  and  $C_{itb}$  are front and back interface trap capacitance, respectively, and other parameters take their usual meaning. Eq. 4.2 provided a good fit to experimental data as shown in Fig. 4.5. This fitting demonstrates that  $D_{itb}$  values extracted for the back interface of GO1 and GO2 devices are almost the same, around  $\approx 10^{10} \text{eV}^{-1} \text{cm}^{-2}$ , which is reasonable considering the high quality of the Si/SiO<sub>2</sub> interface between channel and BOX [13].



**Figure 4.6** Temperature dependence of  $\mu_{0\_GO1}$ ,  $\mu_{0\_GO2}$  and additional mobility,  $\mu_{add}$  (symbols).  $\mu_{add}$  is well fitted with a combination of different power laws of temperature,  $\sim T$  and  $T^{-1}$ , in different temperature regimes (lines).

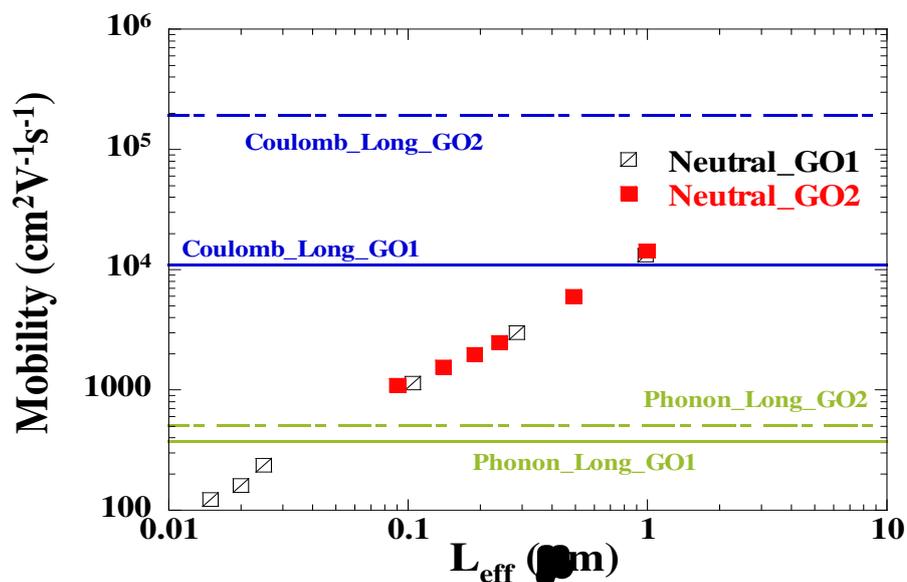
On the other hand, GO1 and GO2 stacks include interface layers with different thicknesses between defective high- $k$  layer and silicon body. However, the values of  $D_{if}$  obtained for both devices are similar, about a few  $10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ . Indeed, this method can only capture fast interface traps at the very interface, ignoring the additional contribution of slow states which are located deeper into the dielectric layer, thus ignoring the potential contributions of traps associated to the high- $k$  layer. These results indicate that in terms of fast interface trap density ( $D_{if}$  and  $D_{itb}$ ), back interface quality of back interface is better than that of front interface. However, the  $D_{if}$  value extracted from SS cannot distinguish the difference of IL thickness in our study. It can be due to the fact that SS analysis is less sensitive to the presence of distant charges, while diffusion by charged centers (which generate the so-called remote Coulomb scattering), is effective at longer distances. Therefore, this methodology is not enough sensitive to detect the presence of traps from the high- $k$  dielectric layer with our different types of gate dielectric stacks.

Next, in order to clarify the origin of the differences in mobility behavior and to quantify the additional scattering contribution in GO1 compared to GO2, we applied the additional mobility extraction method following [14]:

$$\frac{1}{\mu_{add}} = \frac{1}{\mu_{0\_GO1}} - \frac{1}{\mu_{0\_GO2}} \quad (4.3)$$

where  $\mu_{\text{add}}$  is the mobility term associated with the additional scattering mechanism. In this method, we assumed that the bulk properties of GO1 and GO2 devices, such as volume phonon and Coulomb scattering, were identical for both stacks and that the analysis of  $\mu_{\text{add}}$  would then capture the effect from higher proximity of high- $k$  layer to channel in GO1. As shown in Fig. 4.6, it was possible to fit  $\mu_{\text{add}}$  quite well with two temperature dependences. Above 150K,  $\mu_{\text{add}}$  approximately followed a  $T^{-1}$  trend while below 150K, it was proportional to temperature. These temperature dependencies observed in GO1 are consistent with the dominance of SOP above 150K, and of RCS below 150K. One or the other explanation has been brought in the literature, partly due to the fact that the dominant mechanism may strongly depend on the details of stack characteristics and process quality. Here, we show that, SOP and RCS scattering are both present in  $\mu_{\text{add}}$ , although their influence on electron transport is visible in a different range of temperature.

#### 4.3.1.2 Dominant scattering mechanism in short channel devices



**Figure 4.7** Effective length dependence of the contributions of the different scattering mechanisms extracted at room temperature, independently in GO1 and GO2 and at every gate length, from fitting of the temperature dependence of  $\mu_0$ .

So far, we have shown that the higher proximity of high- $k$  layer in GO1 devices affects the carrier transport behavior in the different temperature ranges. In this section, we will provide a comparative study of transport mechanisms depending on channel length. Fig. 4.7

plots the different scattering contributions to mobility at room temperature as a function of  $L_{\text{eff}}$ , which can be extracted by Eq. 4.1 as mentioned in Chapter 4.3.1. In terms of phonon and Coulomb scattering, the mobility values from GO1 devices were always smaller than that of GO2 devices, which is quite reasonable considering the thinner interface layer of GO1.

On the other hand, it is worth noting that the neutral defect contributions of GO1 and GO2 were aligned, even though the dielectrics are different, indicating that the neutral defects were independent of gate-stack. This supports the idea that these neutral defects are mainly originating from S/D process, as reported in [15]. Moreover,  $\mu_{\text{nd}}$  is decreasing at smaller channel length and becomes finally similar to phonon contribution at around 50nm gate length. It means that neutral defect scattering becomes the dominant mobility limiting factor below  $\approx 50\text{nm}$ . This limit is called the critical length ( $L_c$ ) for gate length induced mobility degradation. For the qualitative analysis of  $\mu_{\text{nd}}$  with channel length, we will develop an analytical model in the following paragraph.

The inset of Fig. 4.8 describes the schematic neutral defect distribution that can be expected from S/D engineering. Assuming that the neutral defect density ( $N_{\text{nd}}$ ) profile follows an exponentially decreasing behavior in the channel, the  $N_{\text{nd}}$  profile is simply expressed as:

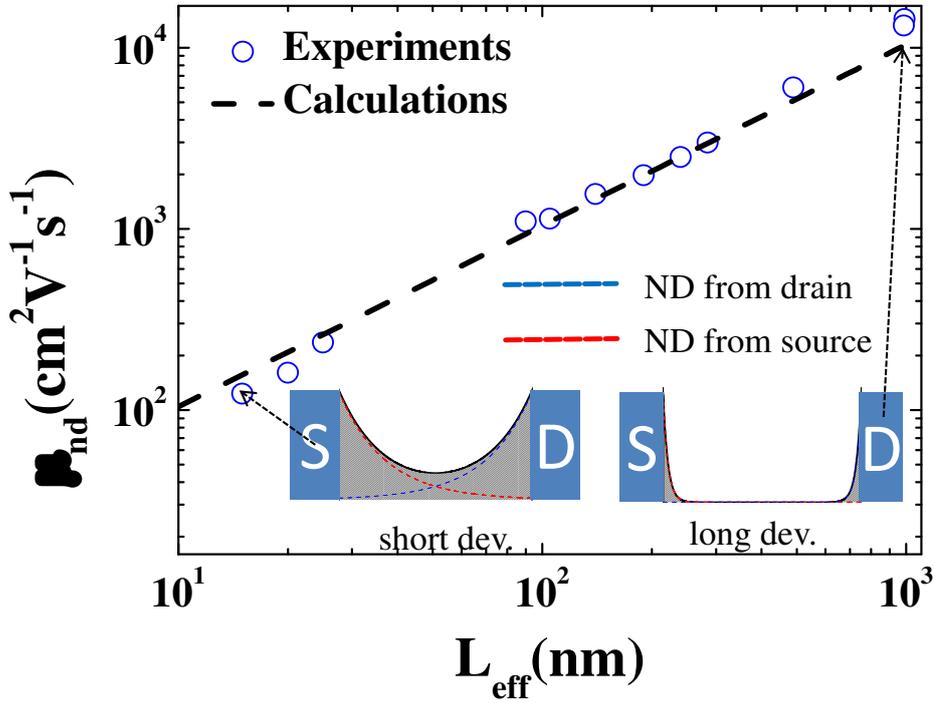
$$N_{\text{nd}}(x) = N_m \exp\left(-\frac{x}{\lambda_n}\right) + N_m \exp\left(-\frac{L-x}{\lambda_n}\right) \quad (4.4)$$

where  $L$ ,  $\lambda_n$  and  $N_m$  are channel length, attenuation length of neutral defects and neutral defect density at the S/D region, respectively. Through the visualizing schematic of Fig. 4.8, it can be easily recognized that we are able to find neutral defects just near S/D in the long devices. However, in our highly scaled devices, the  $N_{\text{nd}}$  profiles from S and D regions are overlapping each other. Therefore, we have a high density of  $N_{\text{nd}}$  even at the middle of the channel. Bases on neutral defect density profile,  $\mu_{\text{nd}}$  can be evaluated as [16–18]:

$$\mu_{\text{nd}} = \left[ \frac{1}{L} \int_0^L \frac{N_{\text{nd}}(x)}{\alpha_{\text{nd}}} dx \right]^{-1} \approx \frac{L \cdot \alpha_{\text{nd}}}{2 \cdot N_m \cdot \lambda_n} \quad (4.5)$$

where  $\alpha_{\text{nd}}$  is the coefficient that determines the weight of the  $\mu_{\text{nd}}$  term for the Matthiessen's rule. We reproduced  $\mu_{\text{nd}}$  behavior as the function of channel length and compared with experimental extraction. As seen in Fig. 4.8, good agreement was obtained with  $\lambda_n=10\text{nm}$  and  $N_m=8 \times 10^{19} \text{cm}^{-3}$ . Key features of this analytical model are that  $\mu_{\text{nd}}$  has a linear dependence with channel length and is inversely proportional to  $\lambda_n$  and  $N_m$ . Therefore, neutral defect scattering can govern the carrier transport mechanism in ultimately scaled-down devices, and optimized

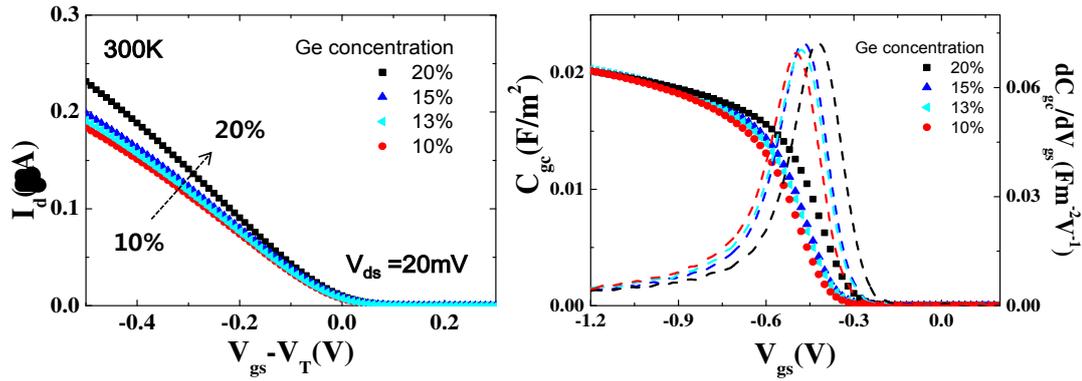
S/D fabrication processes are needed to achieve better transport properties.



**Figure 4.8** Effective length dependence of neutral defect scattering mobility (symbols) and the fitting curve of Eq. 4.4. Inset: schematics of neutral defect distribution from source and drain for long and short channel devices

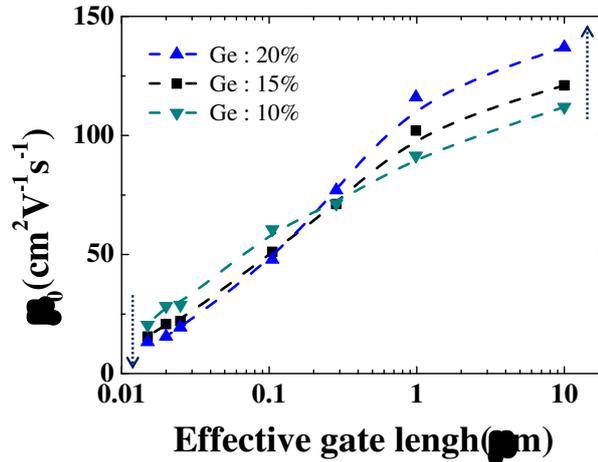
### 4.3.2 Transport properties of PMOS devices

For SiGe devices, it is well known that increasing Ge content or/and compressive strain (biaxial or uniaxial) in the channel enhances hole mobility due to the suppression of inter valley phonon scattering, band degeneracy lifting and reduced effective mass [19–21]. In addition, the threshold voltage ( $V_{th}$ ) shifts linearly with Ge concentration because of the dependence of valence band offset between Si and SiGe alloys with Ge content [22]. As shown in Fig. 4.9(a), long devices ( $L=10\mu\text{m}$ ,  $W=1\mu\text{m}$ ) actually show clear mobility enhancement depending on Ge fraction. In our case, we obtained the best drain current results with 20% Ge content. From the gate-to-channel capacitance ( $C_{gc}$ ) measurement (cf. Fig. 4.9(b)), it was verified that identical capacitance equivalent thickness ( $CET\approx 1.6\text{nm}$ ) were obtained in all the wafers with their various Ge contents. Also,  $V_{th}$  intrinsic shift according to Ge fraction, which is around  $\approx 8\text{mV}/\%$ , was observed from derivative of  $C_{gc}$ .



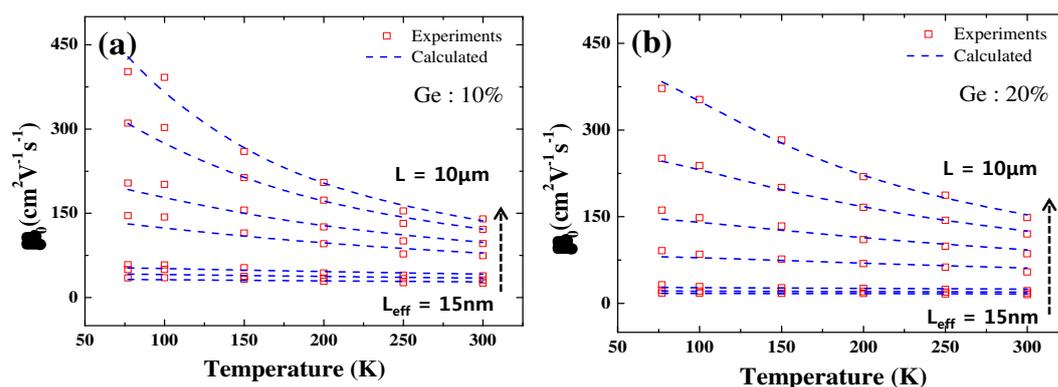
**Figure 4.9** (a) Typical drain current as a function of overdrive voltage, (b) gate-to-channel capacitance ( $C_{gc}$ ) and derivative of  $C_{gc}$  as a function of  $V_{gs}$  for PMOS long channel devices with different Ge content ( $W=1\mu\text{m}$  and  $L=10\mu\text{m}$ ).

**Figure 4.10** Low field mobility ( $\mu_0$ ) degradation as a function of effective gate length with varying Ge content at room temperature

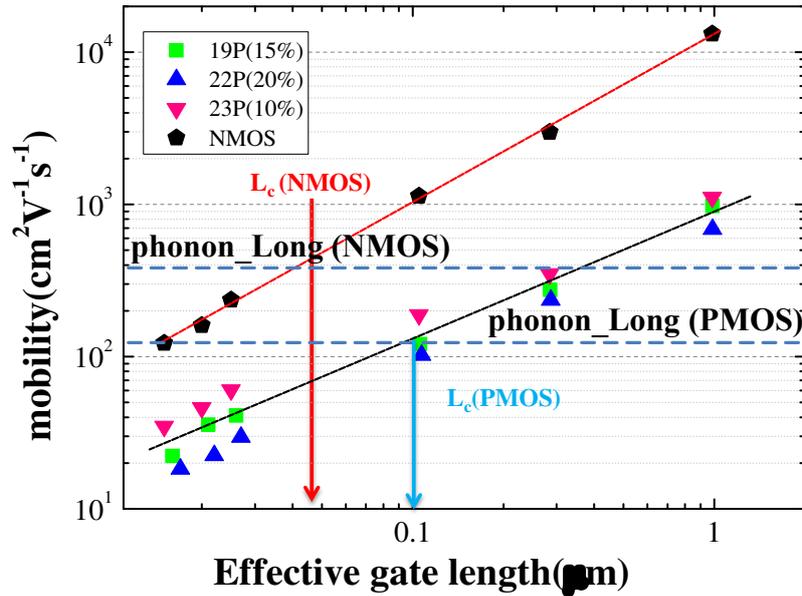


Then, we measured transfer characteristics for different gate length values and extracted  $\mu_0$  at room temperature as plotted in Fig. 4.10. It is worth noting that the effect of Ge content is validated solely in long channel devices. In contrast, in short channel devices, such as below 100nm, the transport is degraded by an increase in Ge content. Such a mobility degradation behavior has already been reported by Cassé et al. [23]. This feature indicates that the dominant transport mechanism in short channel devices is totally different from that in long channel devices. In order to have an insight into transport behavior dependence with channel length, the empirical model of Eq. 4.1 was also applied to the PMOS devices. In order to do that, we measured transfer curves of our PMOS devices with various channel length and temperature varying in the range of 77K–300K and extracted  $\mu_0$  as for NMOS devices. Fig. 4.11 shows that the empirical model matches experimental data. Besides, even though mobility values are

smaller in PMOS than in NMOS devices, mobility shows approximately the same temperature dependence for each channel length. Based on these results, we extracted neutral defect mobility contribution as a function of channel length and plotted extracted values in Fig. 4.12. Overall, the neutral defect mobility in PMOS devices is lower than in NMOS devices. As already found in NMOS devices, the contribution of neutral defect scattering is inversely proportional to channel length. The critical length  $L_c$  is around 100nm for PMOS devices. In addition, we find that neutral defect scattering shows Ge content dependency, where  $\mu_{nd}$  is lower when Ge% increases whatever the channel length. In other words, the number of neutral scattering centers in the channel is larger with the highest Ge content (20%) than with other tested values. Therefore, these results are fully consistent with our previous observation that the mobility enhancement due the Ge content or/and strain in the channel is no more activated for the devices below 100nm and that, rather, it might even cause mobility degradation in short channel devices. This would be the result of stronger neutral defect scattering.



**Figure 4.11** Temperature dependence of low field mobility ( $\mu_0$ ) for the PMOS devices with (a) 10% and (b) 20% of Ge. The empirical model (blue dot line) was used in order to find mobility contribution related with phonon, Coulomb and neutral defect scattering which was well fitted with experimental results.



**Figure 4.12.** Effective length dependence of neutral defect scattering mobility ( $\mu_{nd}$ ) for NMOS and PMOS devices with different Ge content. As for NMOS devices,  $\mu_{nd}$  of PMOS devices was found proportional to channel length and the critical length ( $L_c \approx 100\text{nm}$ ) of PMOS devices was larger than that of NMOS devices.

#### 4.4 Conclusions

The electrical performances of UTBB FD-SOI devices were deeply investigated under low temperature measurement conditions. In NMOS devices, the scattering mechanisms were analyzed by comparing two high- $k$  gate stacks, GO1 and GO2. With GO1, RCS and SOP scattering, which are both originating from close high- $k$  dielectric proximity to channel, were found to bring the dominant contribution for long channels. One or the other mechanism was dominant depending on temperature, soft optical phonon scattering being dominant at room temperature. Mobility degradation below 50nm gate length was clearly attributed to neutral defects induced by source/drain formation, and independent of gate oxide stack. For the PMOS long channel devices, mobility enhancement and  $V_T$  shift related to Ge incorporation were clearly demonstrated by using technological splits with varying Ge content. Also, we confirmed that the mobility boost is no more effective in highly scaled devices since the transport properties are governed by the neutral defect scattering which is mainly caused by high Ge content and source/drain engineering.

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# Chapter 5

## Low temperature characterization of mobility in 14nm FD–SOI CMOS devices under interface coupling conditions

### 5.1 Introduction

For sub–20nm CMOS technology nodes, the ultra–thin body and BOX (UTBB) fully depleted silicon–on–insulator (FD–SOI) MOSFET is considered as one of the best competitors. While keeping a planar architecture, they have been shown to feature competitive performance, high electrostatic integrity and low variability, and to allow hybrid channel and bias–engineered multi– $V_t$  strategies [1]. Carrier transport properties are an essential ingredient in overall performance. Their detailed study requires in–depth analysis of static characteristics as a function of temperature, gate overdrive and device dimensions. On the other hand, using room temperature characterization of long channel devices, a recent work has demonstrated that mobility improvement could be obtained by back–gate biasing [2,3]. The mobility gain was explained using the notions of "return point of the effective field" and "multi–branch" mobility curves. It was demonstrated that a given value of the effective field could be obtained with different bias configurations of front– and back–gates, and thus with different contributions of each interface

to channel conduction, and different effective mobility values [2,3]. Because of the non-univocal relationship between effective field and channel depth, it is clear from these papers that it is difficult to draw conclusions about the detailed mechanisms at the origin of back-gate induced mobility improvement using the dependence of effective mobility with effective field. Moreover, Silicon-Germanium (SiGe) layer has been used in PMOS devices in order to boost hole mobility, instead of pure Si channel [4]. In these complex device architectures affecting to electrical and physical characteristics of devices, such as high-k layer, scaling-down and Ge alloy, it is necessary to deeply investigate the transport properties of advanced FD-SOI devices to understand their operation mechanisms.

In this chapter, we extracted the electrical parameters of UTBB FD-SOI devices in the low-temperature range under interface coupling measurement conditions, where a combination of top-gate and back-gate biases is used to tune the vertical position of the channel. This “crossover” extraction technique is a very powerful tool to get deeper insight into operation mechanism and more quantitative information about device performance. The carrier transport characterization for both NMOS and PMOS devices was performed from 77K to 300K not only in long channel but also for ultra-scaled device representative of the 14 nm technology node [5]

## 5.2 Experiment details

The devices under study were UTBB FD-SOI MOSFETs provided by ST Microelectronics (14nm-node technology). The description of DUT was explained in Chapter 1.4 and the detail information can be found elsewhere [6,7]. The I-V measurements were carried out using HP4156b with a cryogenic probe station. In addition, the C-V measurements were taken out from HP4294A impedance-meter with a 40 mV small signal at 1MHz. The gate-to-channel capacitance ( $C_{gc}$ ) was measured by connecting “high” terminal to gate electrode and “low” terminal to source/drain electrodes [8]. In addition, 1D numerical TCAD simulation of FD-SOI stack was performed to estimate the charge profiles from top-gate to back-gate [8].

## 5.3 Results and Discussions

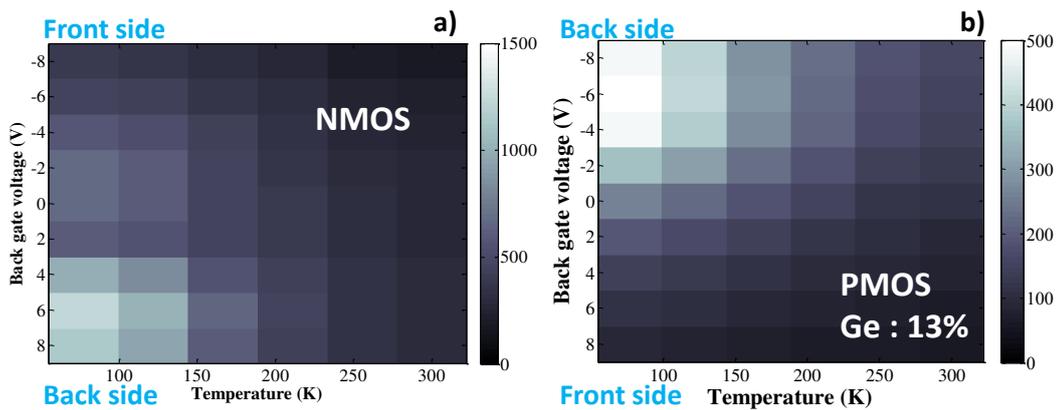
### 5.3.1 Long channel

This section investigates carrier transport properties of long channel (10  $\mu\text{m}$ ) UTBB

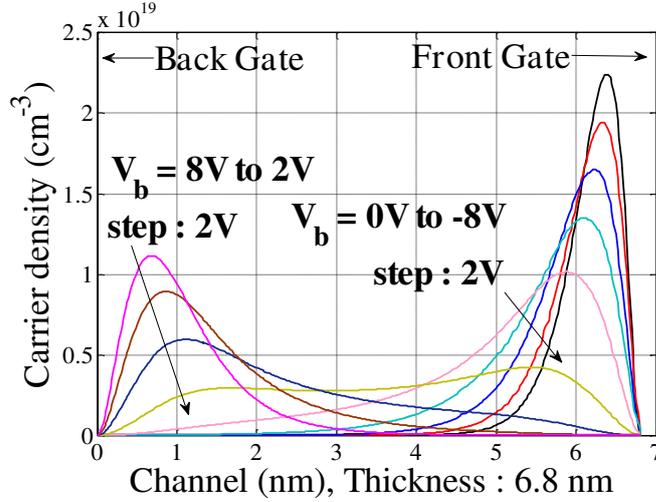
FD–SOI devices. In a previous chapter [9], we have shown that mobility in GO2 follows the universal mobility curve of [10]. In contrast, due to its higher proximity to the channel, the high- $k$  layer of GO1 introduced additional scattering mechanisms compared to GO2. For long channel devices, the dominant additional scattering mechanism in NMOS was remote Coulomb scattering (RCS) below 150K and scattering with surface optical phonons (SOP) above 150K. Here, the study is extended to interface coupling conditions and also to hole mobility characterization, where front- and back-biasing is used to modify channel centroid position and carrier density.

### 5.3.1.1 GO1 vs. GO2 in interface coupling conditions

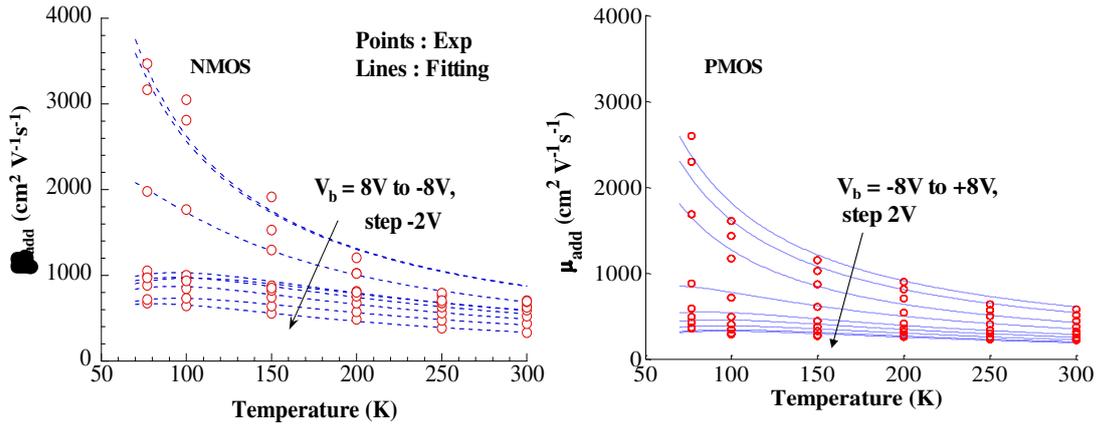
Under coupling conditions, the linearity of  $Y$ -function ( $=I_d/g_m^{0.5}$ ) becomes questionable and low field mobility extraction was no longer suited to this analysis. Instead, we propose to use field effect mobility,  $\mu_{FE}=(L \cdot g_m)/(W \cdot V_{ds} \cdot C_{ox})$  where  $g_m=dI_{ds}/dV_{gs}$  and  $C_{ox}$  are the transconductance and gate surface capacitance, respectively. As shown in Fig. 5.1, the maps of the maximum  $\mu_{FE}$  in GO1 as a function of temperature and back-gate bias ( $V_b$ ) clearly illustrate the significant mobility enhancement induced by  $V_b$ . The optimized bias values are between 6V (–6V) and 8V (–8V) in NMOS (PMOS) devices, regardless of temperature. Conduction is then taking place close to the back interface as shown in Fig. 5.2 based on TCAD simulation. These TCAD simulations, which solve Poisson equation with Hanch’s quantum correction, are the same ones as those which we used for split  $C$ - $V$  in Chapter 3 [8,11].



**Figure 5.1** Maps of maximum field effect mobility  $\mu_{FE}$  for (a) NMOS and (b) PMOS devices vs. temperature and back-gate voltage  $V_b$ , which is extracted from maximum of  $g_m$ . ( $L_{eff}=10\mu\text{m}$  of GO1 devices)



**Figure 5.2** Simulated carrier profile (300K) for different values of  $V_b$  and for a given value  $V_g = V_g (g_{m\_max})$  in NMOS case.



**Figure 5.3** Experimental  $\mu_{add}$  (symbols) in NMOS (PMOS) device vs. temperature with  $V_b$  varying from 8V (-8V) to -8V (+8V) by steps of  $-2V$  ( $2V$ ). Good fit with Eq. 5.2 (lines) with two temperature dependence ( $T$  and  $1/T$ ).

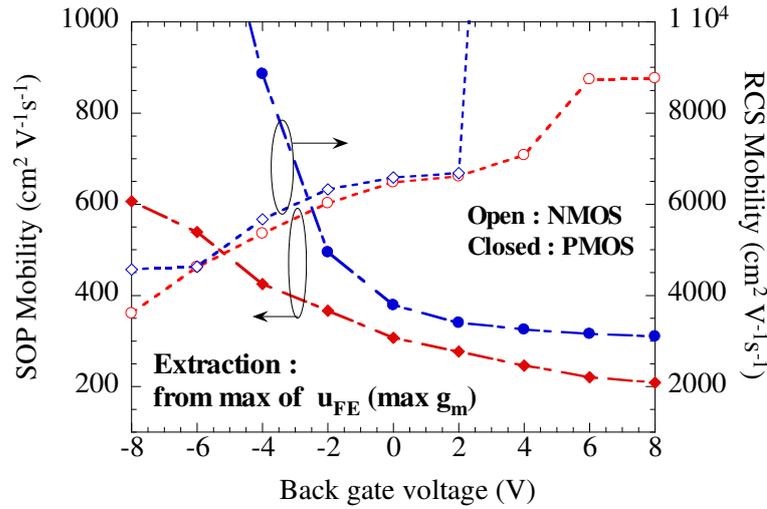
Following the methodology of [12], we extracted the additional scattering mechanisms present in GO1 compared to GO2, using the additional mobility ( $\mu_{add}$ ) defined by the Matthiessen's rule:

$$\frac{1}{\mu_{add}} = \frac{1}{\mu_{0\_GO1}} + \frac{1}{\mu_{0\_GO2}} \quad (5.1)$$

Temperature dependence is shown in Fig. 5.3 and can be well fitted with the following empirical model [9]:

$$\frac{1}{\mu} = \frac{1}{(300/T) \cdot \mu_{ph}} + \frac{1}{(T/300) \cdot \mu_C} \quad (5.2)$$

which includes one term varying as  $1/T$  associated to scattering with SOP and the other varying as  $T$  corresponding to RCS, where  $T$  is absolute temperature [13–15]. In this analysis, value in large excess of the resulting mobility is non-significant as they correspond to a very small difference in the Matthiessen's rule combination. The two contributions are displayed in Fig. 5.4.

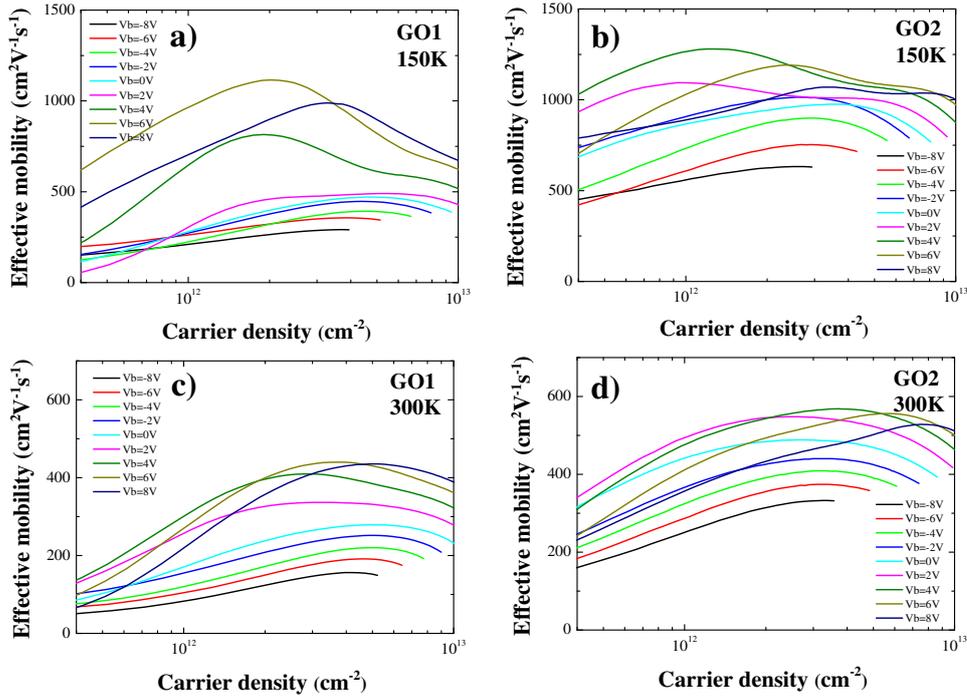


**Figure 5.4** Fitting value of  $\mu_{ph}$  and  $\mu_C$  represent the extracted values of SOP and RCS associated mobility at 300K in NMOS and PMOS devices.

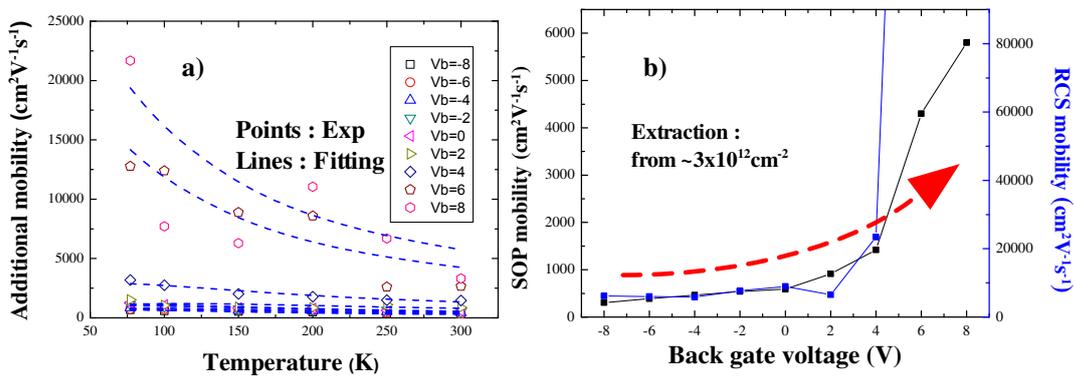
The results show that both SOP and RCS mobility value can be modulated by  $V_b$  changes since the channel centroid moves from front to back interface as shown in Fig. 5.2. This is consistent with Fig. 5.3, which shows that positive back bias (negative back bias in PMOS case) improves carrier mobility in the whole range of temperatures. This result is consistent with the nature of the dielectrics i.e. high- $k$  layer for the front-gate and  $\text{SiO}_2$  for the buried oxide, respectively. The reduction of SOP at the back interface is due to weakly polarizable  $\text{SiO}_2$ , which does not favor propagation of optical phonons. The reduction of Coulomb scattering is associated with the reduced trap density at back interface [9]. It is worth noticing that the SOP scattering dominates transport properties at the maximum of  $g_m$  at 300K while RCS can be neglected. In addition, SOP scattering is much more significant in PMOS case compared to that of NMOS.

In parallel, we extracted effective mobility of GO1 and GO2 NMOS devices using front-gate split CV method (Eq. 2.7) for different temperatures and  $V_b$ . Fig. 5.5 shows representative results such as mobility at 150K and 300K. Then, mobility of both GO1 and GO2 de-

VICES was picked up at same carrier density ( $\sim 3 \times 10^{12} \text{cm}^{-2}$ ) and  $\mu_{\text{add}}$  was calculated in Fig. 5.6(a). Finally, SOP and RCS mobility were deduced within the same methodology as shown in Fig. 5.6(b) which also shows that mobility increases as  $V_b$  goes up and SOP is much more critical in terms of additional mobility. Therefore, we can clearly confirm that these two different approaches indicate consistent conclusion.



**Figure 5.5** Representative extracted  $\mu_{\text{eff}}$  as a function of carrier density with different  $V_b$  for NMOS devices. a) GO1 and b) GO2 at 150K, c) GO1 and d) GO2 at 300K

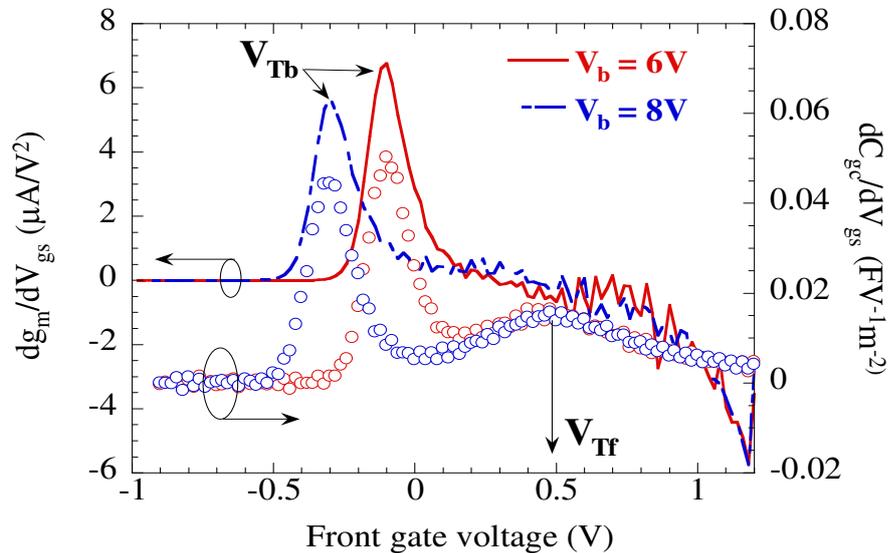


**Figure 5.6** a) Experimental  $\mu_{\text{add}}$  (symbols) from effective mobility ( $N_{\text{inv}} \approx 3 \times 10^{12} \text{cm}^{-2}$ ) as a function of temperature with different  $V_b$  in NMOS devices. Fitting (lines) was performed by Eq. 5.2. b) Fitting value of  $\mu_{\text{ph}}$  and  $\mu_{\text{C}}$  represent the extracted values of SOP and RCS associated mobility at 300K in NMOS

### 5.3.1.2 Front and back channel mobility in interface coupling conditions

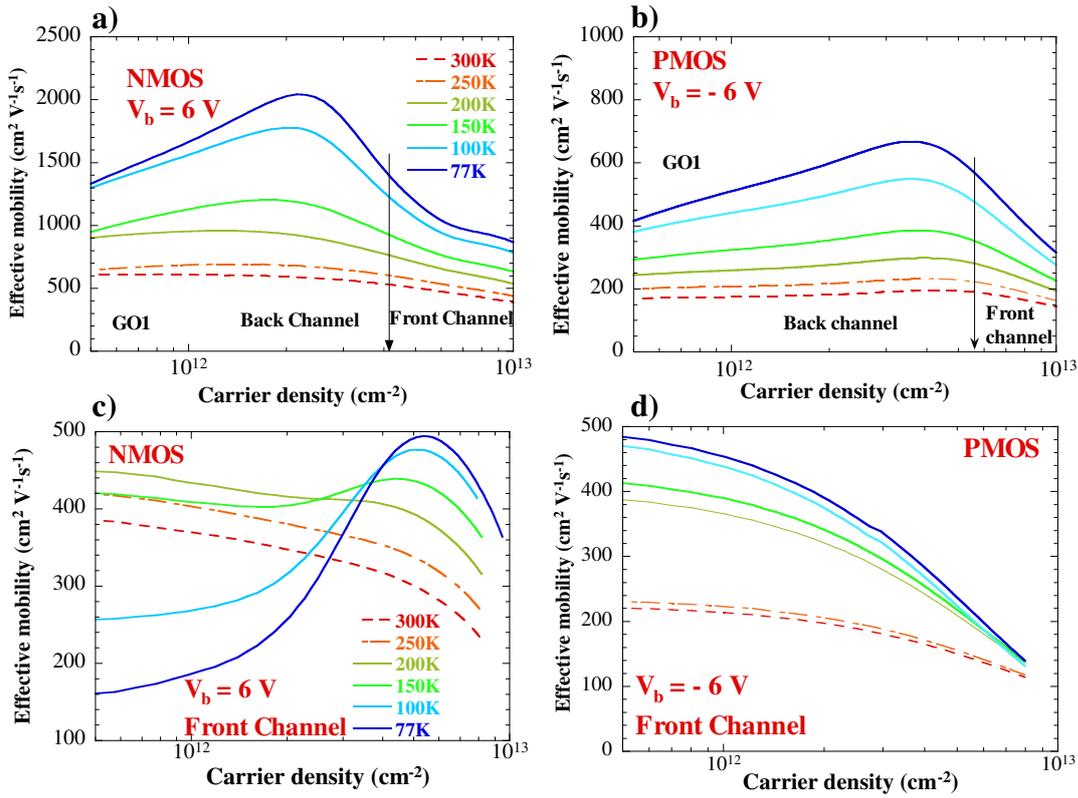
This section analyzes front- and back-channel effective mobility extracted by using the front-gate split CV method [16, 17]. This method is well suited to high  $V_b$  values, where inversion at back interface occurs before inversion at front interface as front-gate voltage increases. In our analysis, we assumed that temperature variation can result in a shift in threshold voltage but does not influence the shape of gate to channel capacitance ( $C_{gc}$ ). Back-channel threshold voltage ( $V_{Tb}$ ) can be extracted both from the peak of the transconductance derivative ( $dg_m/dV_{gs}$ ) and from the first peak of  $dC_{gc}/dV_{gs}$  as a function of  $V_{gs}$ , as illustrated in Fig. 5.7 which shows that both methods give the same results. The second peak in  $dC_{gc}/dV_{gs}$  corresponds to the onset of the front-channel, which is nearly independent of  $V_b$ . It is used to define  $V_{Tf}$ . Back-channel conduction prevails for  $V_{gs} < V_{Tf}$ , while front-channel conduction dominates for  $V_{gs} > V_{Tf}$  (for NMOS case). The limit of back-channel conduction is obtained by  $C_{gc}$  integration between  $-1V$  ( $1V$  in PMOS case) and  $V_{Tf}$ . The onset of front-channel conduction is indicated by an arrow in Fig. 5.8. The corresponding inversion charge depends on  $V_b$  but is independent of temperature. It is used to extract front-channel effective mobility as [17]:

$$\mu_{\text{eff\_front}} = \frac{L}{W} \cdot \frac{I_d - I_{d\_back}}{V_{ds} (Q_{\text{inv}} - Q_{\text{inv\_back}})} \quad (5.3)$$



**Figure 5.7** a) Experimental  $\mu_{\text{add}}$  (symbols) from effective mobility ( $N_{\text{inv}} \approx 3 \times 10^{12} \text{cm}^{-2}$ ) as a function of temperature with different  $V_b$  in NMOS devices. Fitting (lines) was performed by Eq. 5.2. b) Fitting value of  $\mu_{\text{ph}}$  and  $\mu_{\text{c}}$  represent the extracted values of SOP and RCS associated mobility at 300K in NMOS

The best effective mobility values were reached for  $V_b=6V$  in NMOS and  $-6V$  in PMOS. Fig. 5.8(a) and (b) show back- and front-channel  $\mu_{eff}$  as a function of carrier density for temperatures ranging from 77K to 300K. For both devices, by looking the carrier density dependence, we can see a slight screened Coulomb scattering at low temperature ( $\leq 200K$ ). However, temperature dependence shows that scattering with surface and volume phonons is the dominant mechanisms at back interface since the mobility always decreases with increasing temperature.



**Figure 5.8** Effective mobility vs. carrier density for T ranging from 77K to 300K and for (a)  $V_b=6V$  for NMOS and (b)  $V_b=-6V$  for PMOS in GO1 device. Back- and front-channel contributions are separated by arrow. Front-channel effective mobility calculated with Eq. 5.3 for both (c) NMOS and (d) PMOS devices with their respective value of  $V_b$ . ( $W=1\mu m$ ,  $L=10\mu m$  for both NMOS and PMOS)

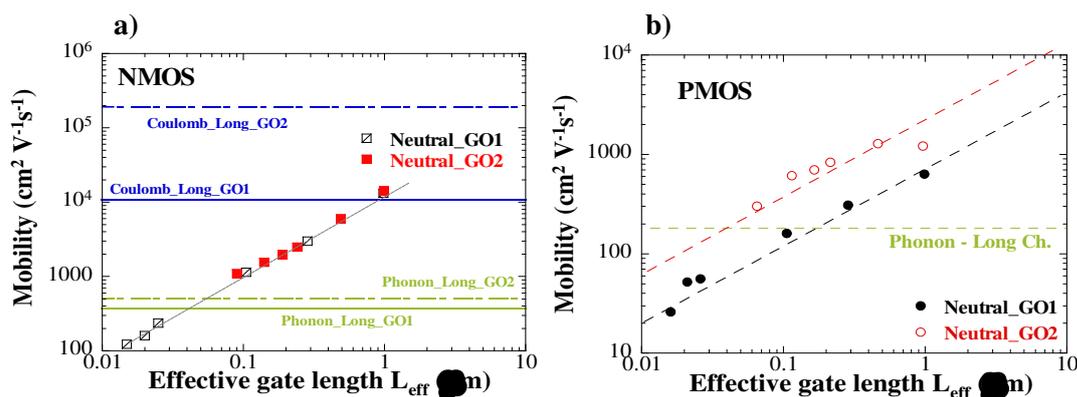
Fig. 5.8(c) and (d) specifically demonstrate the front-channel  $\mu_{eff}$  for  $|V_{gs}| > |V_{Tf}|$ . In this regime, the carrier centroid is closer to front interface than to back interface. In NMOS, very clear RCS and screening behavior can be observed at low temperature. At low carrier density, we can also estimate the critical temperature separating the regimes of predominance of Coulomb or Phonon scattering. This critical temperature is in the range of 150K–200K, depending on  $V_b$ . Thus, SOP can be observed at low and moderate carrier density regime for  $T > 200K$ . In contrast, it can be seen that the Coulomb-like behavior cannot be recognized in the

PMOS device, even at low temperature in Fig. 5.8(d). Hole transport in front-channel at low and moderate carrier density is totally governed by surface phonon in the whole explored range of temperatures (from 77K to 300K). In addition, as usual, we found mobility degradation at high carrier density in both NMOS and PMOS regardless of  $T$  and  $V_b$  as shown in Fig. 5.8(c) and (d). This is due to surface roughness scattering.

### 5.3.2 Gate-length variations

In previous section, we focused the analysis on scattering mechanisms in long channel UTBB FD-SOI devices. We analyzed the influence of gate stack on electron transport and by which mechanisms back-gate bias could improve device performance. The aim of this section is to push the analysis towards shorter gate lengths.

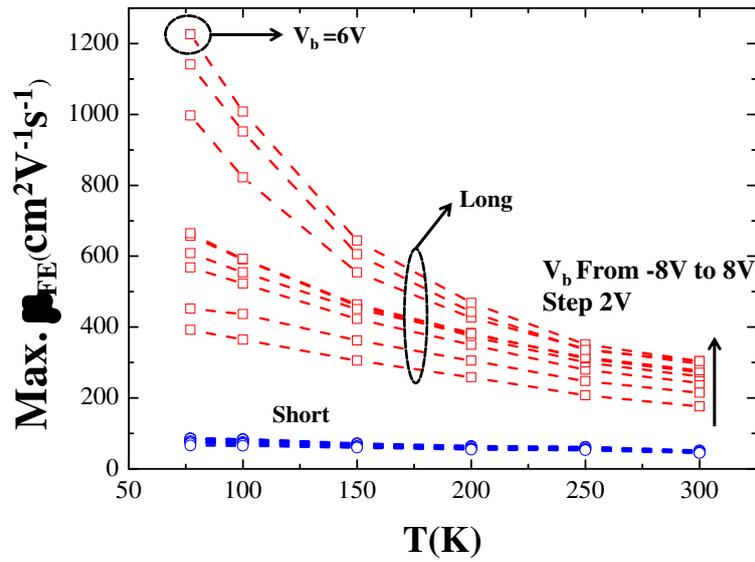
Here, we come back to the low field mobility  $\mu_0$  approach to characterize the transport properties because of its immunity to series resistance effects. As already explained,  $\mu_0$  can be extracted with Y-function ( $=I_d/g_m^{0.5}$ ) [9]. We extracted  $\mu_0$  as a function of temperature and with different gate length values, for both GO1 and GO2 devices. Then, we used the fitting function as in Eq. 5.2 including all three temperature dependence ( $T^{-1}$ ,  $T^{+1}$ ,  $T^0$ ) associated with phonon, Coulomb and neutral defects scattering mechanisms,  $\mu_{ph}$ ,  $\mu_C$  and  $\mu_{nd}$  [9, 18, 19]. As shown in Fig. 5.9, the different mobility terms were extracted as function of effective gate length ( $L_{eff}$ ) in NMOS and PMOS, respectively. It is worth noticing that in NMOS the neutral defect mobility of GO1 and GO2 is aligned, even though they have different gate dielectrics, indicating that neutral defects are independent of the gate-stack. We believe that these neutral defects could originate from source/drain process and act as volume diffusion centers located inside the channel. Moreover, we have demonstrated that decreasing channel length does not induce strong changes in phonon and Coulomb contributions to electronic transport in FD devices [9]. So, the neutral defect scattering is the dominant factor that limits mobility below the critical effective length ( $50\text{nm}\pm 10\text{nm}$ ) because of  $\mu_{nd} < \mu_{ph}$  and  $\mu_{nd} \ll \mu_C$ . In PMOS case (cf. Fig. 5.9 (b)), the neutral defect scattering shows the same trend as for NMOS in terms of channel length variation. However, unlike NMOS case,  $\mu_{nd}$  depends on the nature and thickness of the gate stack layers. It means that some diffusion centers have surface-like behavior and that they might be located at the interface between channel and gate stack. We will discuss these arguments in more details in the next section where we will deeply analyze the short channel devices. The critical length in PMOS device could be estimated around  $100\text{nm}\pm 10\text{nm}$ .



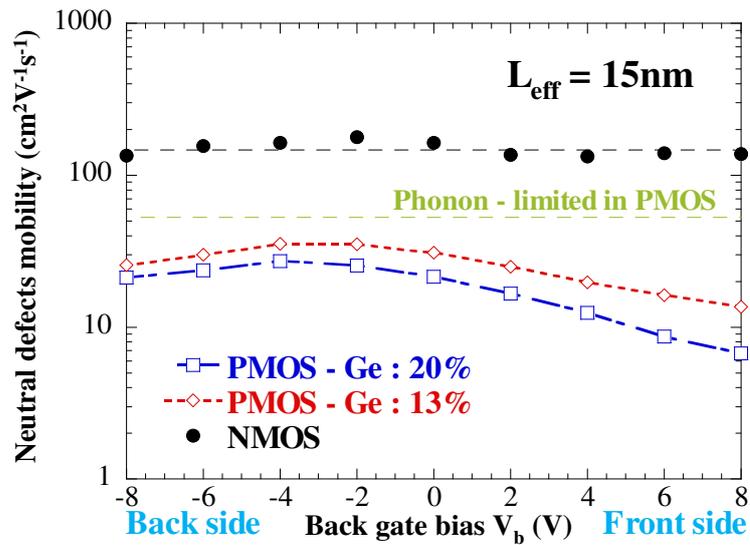
**Figure 5.9** Components of the mobility associated to the different scattering mechanisms as a function of effective channel length. a) NMOS and b) PMOS ( $V_b=0V$ )

### 5.3.2 Short channel in interface coupling conditions

A more in depth analysis is necessary to understand the underlying scattering in short channel devices. Here, we tested the short channel devices in interface coupling conditions. Again, we take the  $\mu_{FE}$  approach at maximum of  $g_m$ . As shown in Fig. 5.10 (for the example of NMOS devices) there is no significant mobility enhancement with back-gate bias in the shortest channel devices of GO1. This is in contrast with long channel case. In long devices, it is clearly seen that back-gate biasing has a large influence on transport. Forward back bias ( $V_b > 0V$ ) brings a strong boost to mobility with mobility enhancement up to a factor of 3. In contrast, in short devices, mobility improvement with back-bias is almost negligible as compared to long devices. Moreover, the slight mobility improvement occurs under reverse back bias ( $V_b < 0V$ ) where the charge centroid is closer to front interface, which is opposite to long devices case. This confirms that, in short devices, scattering is not dominated by mechanisms related to front- and back-gate stacks. Rather, scattering centers such as neutral defects lying close to S/D regions are the most limiting factors.



**Figure 5.10** Maximum of  $\mu_{FE}$  in NMOS devices vs. temperature with various back-gate bias  $V_b$  (from -8 to 8V by steps of 2V) for long ( $L_{eff}=10\mu m$ ) and short ( $L_{eff}=15nm$ ) channel of GO1 devices



**Figure 5.11** Neutral defect limited mobility in NMOS and PMOS (with two Ge%: 13% and 20%) devices with  $L_{eff} = 15nm$  as function of back-gate bias. For PMOS case, the back side and front side of carrier centroid position are also indicated

In order to complement this study of carrier transport in the shortest NMOS and PMOS devices, we finally applied the empirical mobility fitting model (including phonon, Coulomb, neutral scattering and ballistic contribution [20]) to short channel devices ( $L_{eff}=15nm$ ) with coupling conditions and extracted defects limited mobility (Fig. 5.11). Unlike NMOS devices [21], the PMOS device was more sensitive to  $V_b$ . It shows surface-like behavior, which

means that defects centers could be located close to front interface. Considering that is proportional to the density of scattering defects, Fig. 5.10 shows that the defects density would be larger close to front interface and that it would increase with Ge content. We also found that defect density could be denser close to front interface and that this density rises with increment of Ge content in channel.

## 5.4 Conclusions

In this chapter, we characterized for the first time the electron transport in UTBB n-type and p-type FD-SOI devices using cryogenic operation under interface coupling conditions. In long channel case, mobility was governed by high-k/metal front-gate stack related scattering mechanisms, RCS or SOP playing the main role in different temperature ranges in NMOS devices. Back-bias induced mobility improvement could be both quantitatively and qualitatively analyzed by separating the back- and front-channel contributions using the front-gate split CV method. By analyzing gate length dependence, for NMOS, we found an additional contribution which does not depend of front-gate oxide stack and is consistent with neutral defects scattering. We think that these neutral defects could be occurred from source/drain fabrication process. In addition, below some critical gate length ( $\approx 50\text{nm}$ ), mobility improvement by back-biasing was not effective anymore unlike for long channel devices. This confirmed the prevailing role of channel defects in mobility degradation for ultra-scaled devices. Besides, in PMOS, the defect centers demonstrated surface-like behavior (they were sensitive to carrier centroid modulation by  $V_b$ ). The defects density could be denser close to front interface and larger for higher Ge contents.

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# Chapter 6

## Magnetoresistance mobility characterization in advanced FD–SOI transistors

### 6.1 Characterization of magnetoresistance in linear regime of FD–SOI nMOS devices

#### 6.1.1 Introduction

Over the last few decades, shrinking the size and cost of transistors has aggressively occurred in CMOS technology [1,2]. The range of even 10nm channel length is achievable. In order to maintain the accuracy of parameter extraction at such small dimensions, it is necessary to develop the capacities of electrical characterization and make extraction less dependent on assumptions about physical dimensions or device operation models.

It is already known that magnetoresistance (MR) measurements in the linear regime of operation of MOS transistors have the advantage of directly measuring mobility, without any extraction methodology limitation while usual methods require channel dimensions and gate surface capacitance to be measured or extracted. This is a strong asset for ultra-scaled devices where channel length differs from physical gate length due to source/drain contact processing, while physical gate length itself is different from on-mask gate length due to lithography /etching processes which usually include some trimming. Moreover, usual methods are exploit-

ing the strong inversion regime of operation. They are thus ill-suited to probe the presence of charged defects, which are mostly screened in the range of application. In contrast, MR measurement is the only accurate characterization method to capture transport properties in sub-threshold regime.

Previous studies have already highlighted the potential of magnetoresistance measurements in the linear regime for mobility extraction in bulk and SOI technology [3–5]. In this chapter, we applied this technique to NMOS devices from a 14nm-node FD-SOI technology. Moreover,  $\mu_{MR}$  characterization was performed for the first time in interface coupling conditions, in order to identify the scattering mechanisms induced by the high-k/metal gate stack and to understand mobility enhancement with back-gate biasing at room and low temperature. Additionally, from a methodological point of view,  $\mu_{MR}$  mobility was compared with the low field mobility ( $\mu_0$ ) extracted from static characteristics and their respective values were discussed with respect to their Coulomb scattering contribution in the overall mobility.

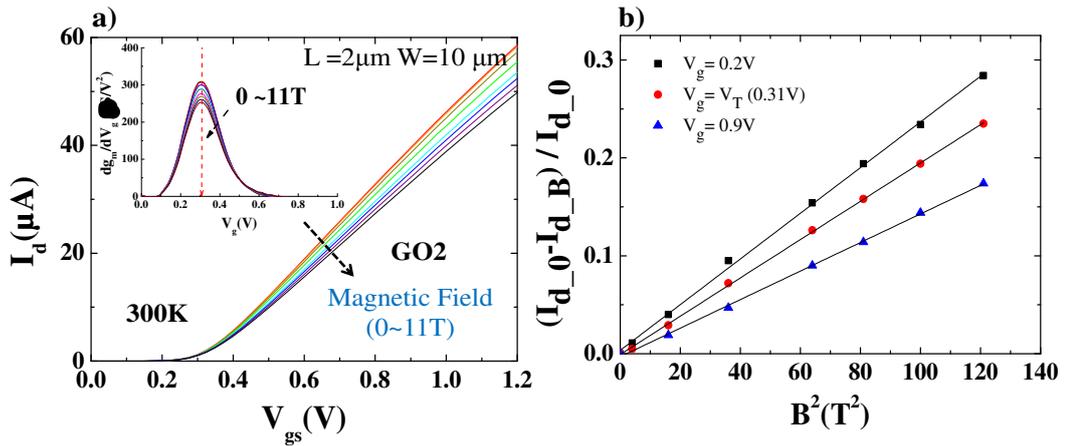
The chapter is organized as follows. At first, the devices under test and the extraction of channel magnetoresistance mobility with series resistance ( $R_{sd}$ ) correction are dealt with in Chapter 6.1.2. Then we reports  $\mu_{MR}$  results obtained for two different gate stacks, with various gate lengths (mask length from  $2\mu\text{m}$  to 30nm), and for two temperatures. A detailed analysis was carried out as a function of gate voltage and back-bias. This allowed the main scattering mechanisms to be identified and the temperature and bias conditions where they are dominant to be determined. Moreover, using back-biasing, it was possible to tune vertically the position of the channel. For back-bias voltages where it was localized at front interface, main contributions arisen from the top interface with its high-k layer make it possible to explore these effects. Finally, the ability of MR mobility and low field mobility to reveal the origin of mobility degradation at short gate length will be discussed.

### 6.1.2 Experiment details

The devices under study were UTBB FD-SOI MOSFETs provided by ST Microelectronics (14nm-node technology). The description of DUT was explained in Chapter 1.4 and the detail information can be found elsewhere [2]. We analyzed several  $\mu_{MR}$  variations with the gate length, the gate stack (GO1 and GO2), and the front/back gate biasing. These analyses could be enriched by the influence of temperature (100K and 300K). Also, the gate mask length ( $L_{mask}$ ) varies from 300nm to 30nm for GO1 devices while, in GO2 devices, it changes from  $2\mu\text{m}$  to 150nm. Since GO1 devices have much thinner gate dielectric, so smaller gate lengths are avail-

able. The channel width ( $W$ ) is  $10\mu\text{m}$  and  $1\mu\text{m}$  for GO2 and GO1 devices, respectively, so that channel length ( $L$ ) needed to be carefully selected in order to fulfill the geometrical magnetoresistance requirement [5]. Magneto-transport measurements were carried out in the Grenoble High Magnetic Field Laboratory, with  $B$  ranging from  $0\text{T}$  to  $11\text{T}$  and the measurement were performed in a cryostat where the magnetic field was applied using superconducting coils. The  $I$ - $V$  measurements were carried out using semiconductor parameter analyzer, HP4156b. In this measurement, we swept gate voltage ( $V_{\text{gs}}$ ) with fixed  $B$  and back-gate voltage ( $V_{\text{b}}$ ), then we repeated the same procedure for each  $B$  and  $V_{\text{b}}$  for two temperatures ( $100\text{K}$  and  $300\text{K}$ ), respectively.

Fig. 6.1(a) shows the influence of magnetic field on the transfer characteristics  $I_{\text{d}}(V_{\text{gs}})$  in the linear regime of operation ( $V_{\text{ds}}=20\text{mV}$ ), for the devices with GO2 at  $300\text{K}$ .  $L$  and  $W$  were  $2\mu\text{m}$  and  $10\mu\text{m}$ , respectively. As shown in inset of Fig. 6.1(a), the drain current second derivative method was used to extract threshold voltage ( $V_{\text{T}}\approx 0.31\text{V}$ ) which is independent of  $B$ . It is verified that the MR effect can be observed in the whole range of gate voltages, even below  $V_{\text{T}}$  as seen in Fig. 6.1(b). This feature means that the MR mobility can be accurately extracted from weak to strong inversion regime. Thus, we can plot  $\mu_{\text{MR}}$  as a function of  $V_{\text{gs}}$  or inversion carrier density ( $N_{\text{inv}}$ ). In order to estimate  $N_{\text{inv}}$ , we assumed that MR mobility and effective mobility are not too different, so that  $N_{\text{inv}}$  can be calculated from drain current as [5]:  $N_{\text{inv}}\approx(L/W)\cdot I_{\text{d}}/(V_{\text{d}}\cdot\mu_{\text{MR}})$ .

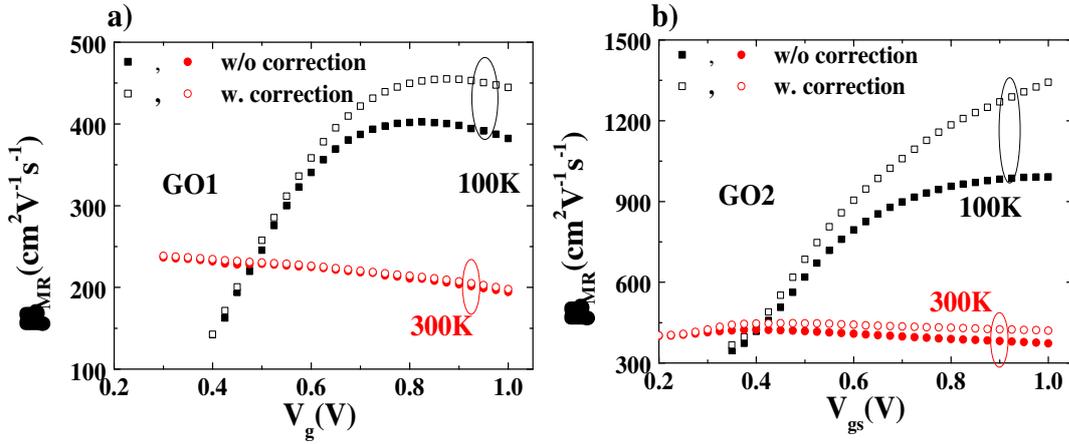


**Figure 6.1** a) Transfer characteristic of drain current ( $I_{\text{d}}-V_{\text{gs}}$ ) at linear regime ( $V_{\text{ds}} = 0.02\text{V}$ ) for different  $B$  from  $0\text{ T}$  to  $11\text{ T}$  at  $300\text{ K}$  for GO2 devices ( $W=10\mu\text{m}$  and  $L=2\mu\text{m}$ ). The inset shows  $V_{\text{T}}$  extraction by using the drain current second derivative method for different  $B$ . The  $V_{\text{T}}$  is indicated by an arrow. ( $V_{\text{T}} \approx 0.31\text{V}$ ) b) Relative drain current variation  $\Delta I_{\text{d}}/I_{\text{d}}$  vs.  $B^2$  below threshold ( $V_{\text{gs}} = 0.2\text{V}$ ), equal to threshold ( $V_{\text{gs}} \approx 0.31\text{V}$ ) and above threshold ( $V_{\text{gs}} = 0.9\text{V}$ ).

Details about the physical background of  $\mu$  extraction can be found in Chapter 2.2.1. In short, under the condition that  $W \gg L$ , the Hall voltage generated by the applied magnetic field is almost short circuited by source and drain equipotential lines, so that  $\mu_{MR}$  can be extracted from the drain current variation as a function of the magnetic field from:

$$\frac{I_{d_0} - I_{d_B}}{I_{d_B}} = \mu_{MR}^2 B^2 \quad (6.1)$$

where  $I_{d_0}$  and  $I_{d_B}$  are drain current values without and with  $B$ , respectively. In addition, in order to discriminate the intrinsic channel transport and  $R_{sd}$  access limitation,  $\mu_{MR}$  can be divided into channel and  $R_{sd}$  parts following Chaisantikulwat et al [3]. This method is based on the comparison of two devices from the same chip featuring different gate lengths. It is assumed that  $R_{sd}$  is independent of gate length. Moreover, the gate length of the two devices must be close to each other, so that the two devices have similar threshold voltage and channel mobility. In the same manner as for Eq. 6.1, the  $\mu_{MR}$  of pure channel can be extracted by:



**Figure 6.2**  $\mu_{MR}$  without/with  $R_{sd}$  correction in a) GO1 ( $L_g=300$  and  $120\text{nm}$ ) and b) GO2 ( $L_g=250$  and  $200\text{nm}$ ) as function of gate voltage at  $100\text{K}$  and  $300\text{K}$ .

$$R_T = R_{ch} + R_{sd} \quad (6.2)$$

$$\mu_{ch}^2 B^2 = \frac{\Delta R_{T1} - \Delta R_{T2}}{R_{T1} - R_{T2}} = \frac{\Delta R_{ch1} - \Delta R_{ch2}}{R_{ch1} - R_{ch2}} \quad (6.3)$$

$$R_{ch1,2} = \frac{\delta R_{ch}}{\delta L_{ch}} \cdot L_{ch1,2} \quad (6.4)$$

where  $\mu_{ch}$ ,  $R_T$  and  $R_{ch}$  are pure channel mobility, total and channel resistance, respectively, and  $\Delta R$  means resistance increase by magnetic field [3]. Also, Eq. 6.4 was used in order to find  $R_{ch}$ , where  $\delta R_{ch}=R_{T1}-R_{T2}=R_{ch1}-R_{ch2}$  and  $\delta L_{ch}=L_{ch1}-L_{ch2}$ . After  $R_{ch1}$  and  $R_{ch2}$  are calculated,  $R_{sd}$  can be easily extracted [3].

	$L_G$ (nm)	100 K				300 K			
		$R_{tot}$ ( $\Omega \cdot \mu m$ )	$R_{sd}$ ( $\Omega \cdot \mu m$ )	$R_{sd} / R_{tot}$	$V_t$ (V)	$R_{tot}$ ( $\Omega \cdot \mu m$ )	$R_{sd}$ ( $\Omega \cdot \mu m$ )	$R_{sd} / R_{tot}$	$V_t$ (V)
GO1	300	584	160	0.27	0.45	1029	138	0.13	0.34
	120	330	160	0.48	0.42	495	138	0.28	0.32
GO2	250	620	210	0.34	0.44	1300	200	0.22	0.31
	200	550	210	0.40	0.43	1100	200	0.18	0.31

**Table 6.1** Extracted  $V_T$ , total and series resistance at  $V_g = 1V$  for GO1 and GO2 devices at 100K and 300K, respectively. ( $V_{gs}=1V$  and  $V_{ds}=20mV$ )

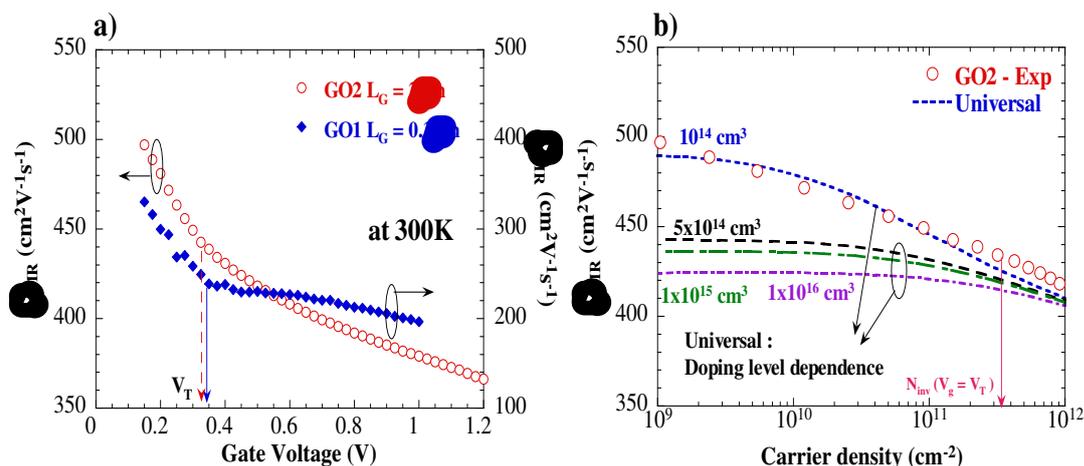
The  $R_{sd}$  effect on  $\mu_{MR}$  is shown in Fig. 6.2 with different gate stacks, for two temperatures, 100K and 300K. With GO1 (GO2), the devices with  $L_{mask}$  values of 300nm and 120nm (250nm and 200nm) were used since the  $\mu_{MR}$  and threshold voltage should be almost the same to extract the channel  $\mu_{MR}$ . Overall, it is clear that the  $R_{sd}$  correction effects are more visible at low temperature and in strong inversion, with a stronger impact for GO2. In order to consistently understand Fig. 6.2, we extracted the values of total resistance and series resistance [3], and summarized these values in Table 6.1 for a given  $V_{gs}$  in strong inversion ( $V_{gs}=1V$ ). We can see that i) the gate-stack has a significant influence on  $R_{sd}$  value, in our case,  $R_{sd}$  (GO1) <  $R_{sd}$  (GO2), ii)  $R_{sd}$  is not very sensitive to temperature due to the degenerate nature of access regions, and, iii) at 300K,  $R_{sd}$  has a negligible impact in GO1 devices.

## 6.1.3 Results and discussions

### 6.1.3.1 $\mu_{MR}$ extraction in long channel at 300K

At first, we focused on long channel devices at room temperature. Fig. 6.3(a) shows  $\mu_{MR}$  as a function  $V_{gs}$  for both GO1 and GO2 devices. Above threshold, we observed the conventional mobility degradation trend with  $V_{gs}$  due to the increase of phonon and/or surface roughness (SR) scattering for increasing electric field and confinement. However,  $\mu_{MR}$  increases as  $V_{gs}$  decreases below threshold voltage in Fig. 6.3(a), which is in contrast with standard MR results obtained with doped channels where degradation by Coulomb scattering with ionized

doping atoms was clearly visible. Moreover, we can observe this behavior even in GO1 case which has relatively short gate length and thinner interface layer of gate-stack. This feature is consistent with the fabrication process with undoped channel and indicates that gate interface and gate stack do not generate significant remote Coulomb scattering (RCS) at room temperature.



**Figure 6.3** a) Magnetoresistance mobility  $\mu_{MR}$  as function of gate voltage for GO2 ( $L_G = 2\mu\text{m}$ ) and GO1 ( $L_G = 0.3\mu\text{m}$ ) at 300K. b)  $\mu_{MR}$  as function of inversion carrier density and reproduced universal behavior in GO2 device. The Si film doping level dependence within universal model is also shown. The  $V_T$  is indicated by arrows.

It is worth mentioning that this nearly Coulomb-free mobility behavior of GO2 devices is quite consistent with the universal mobility model, which takes into account the screened Coulomb scattering [6], SR and acoustic phonon scattering processes, and with a Si film doping level below  $10^{15}\text{ cm}^{-3}$  [7], as shown in Fig. 6.3(b). In addition, such universal mobility behavior has been experimentally confirmed in Bulk technology with low doping level [18]. Thus, like the additional mobility analysis in Chapter 4, the long channel devices of GO2 can be considered as the reference to extract the additional mobility term associated with the proximity of the high- $k$  dielectric. This will be discussed in Chapter 6.1.4.3. In next section, we will investigate the transport properties evolution with temperature and gate length.

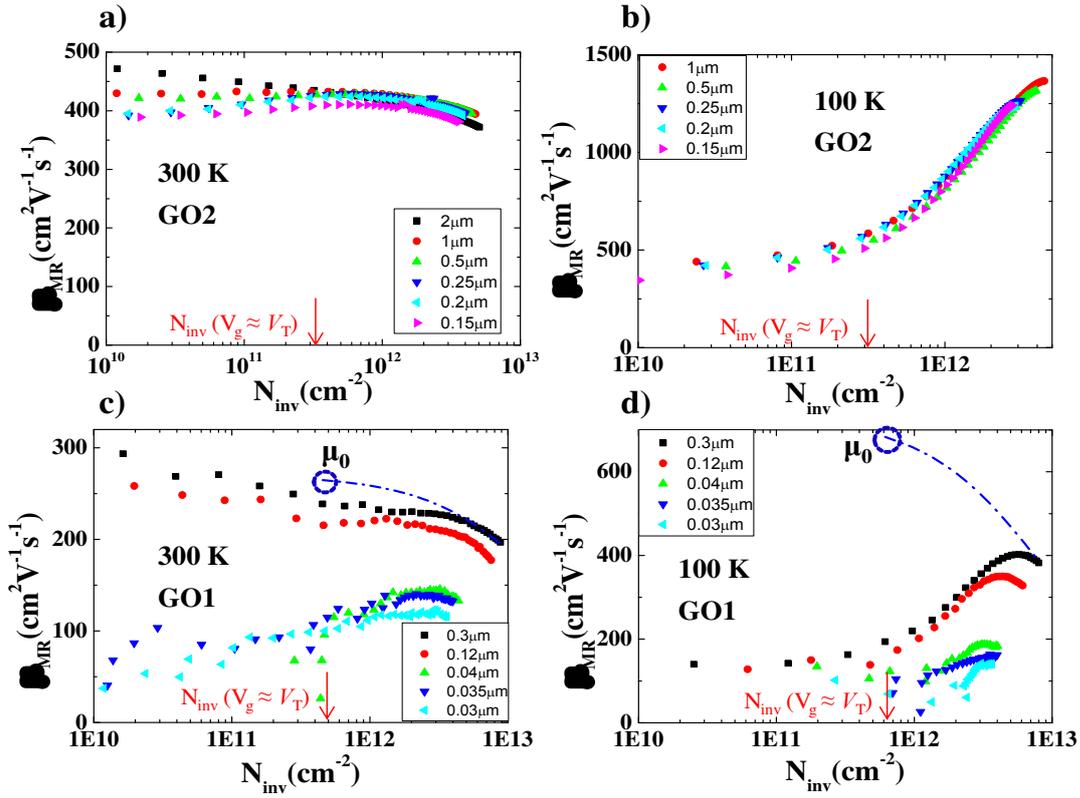
### 6.1.3.2 Influence of temperature and gate length variations

In the general temperature-dependent transport analysis, the transport properties are considered to be governed by phonon-like behavior above threshold voltage when mobility is inversely proportional with temperature, while Coulomb-limited mobility is proportional to

temperature and inversion charge density when Coulomb scattering is unscreened [16]. As the devices have high density of neutral defects, these temperature dependencies are hard to be recognized. On the other hand, channel-length dependent mobility degradation has found different explanations as fabrication technology evolved. For bulk or thick body SOI MOSFETs, which used a doped channel, with highly doped pocket implants around S/D regions, mobility degradation was associated to an increase of Coulomb scattering because the apparent doping level in the channel was increasing as channel length decreased. [19] With present technologies, which are using undoped channels, the temperature signature of the additional scattering at short gate length is rather compatible with the presence of neutral defects associated to the fabrication process of S/D regions.

With the devices studied during this thesis, we obtained the following magnetoresistance mobility results. Fig. 6.4(a) and (b) show  $\mu_{MR}$  with  $R_{sd}$  correction as function of  $N_{inv}$  for different gate lengths in GO2 device at 100K and 300K, respectively. At 300K, the Coulomb scattering below threshold voltage increases in shorter channel devices. Above threshold voltage, we can observe typical phonon and SR behaviors which are almost independent with channel length. However, at 100K, we can clearly identify the unscreened Coulomb scattering at low charge density regime where the mobility reaches a plateau versus  $N_{inv}$ . In addition, the screened Coulomb scattering behavior is obviously shown above threshold voltage, where  $\mu_{MR}$  increases as  $N_{inv}$  increases. Both unscreened and screened effects do not depend strongly with the gate length and they are almost negligible at 300K.

It is worth noting that  $\mu_{MR}$  generally increases as temperature decreases due to the phonon freezing. However, for ultra-scaled devices such as  $L_{mask}=30nm$ , the  $\mu_{MR}$  does not significantly depend on temperature anymore as shown in Fig 6.4(c) and (d), which is fully consistent with our previous analysis of low field mobility ( $\mu_0$ ) at low temperature range [8]. This feature can be attributed to the defects scattering induced by source/drain engineering [9–10]. It should be noted that Fig. 6.4(d) clearly shows a huge difference between  $\mu_0$  and  $\mu_{MR}$  for GO1 long channel devices at 100K, which is no longer observed at room temperature or/and for short channel devices. Further analysis about the origin of these differences will be discussed in Chapter 6.1.3.4.



**Figure 6.4**  $\mu_{MR}$  as function of carrier density for different gate mask length (indicated by different color and symbol): a) for GO2 at 100K, b) for GO2 at 300K, c) for GO1 at 100K, d) for GO1 at 300K. Extrapolated  $\mu_0$  is described in (c) and (d). The approximate inversion charge densities at  $V_T$  are indicated by arrows.

As seen in Fig. 6.4, the value of  $\mu_{MR}$  in GO1 devices is always lower than that of GO2 case even though  $\mu_{MR}$  shapes with  $N_{inv}$  do not show remarkable differences between GO1 and GO2 devices of similar channel length, regardless of temperature. In the next section, we will focus on the scattering processes induced by the high- $k$ /metal gate stack. In order to confirm their nature and find their location, we studied MR transport properties with the interface coupling conditions for the first time.

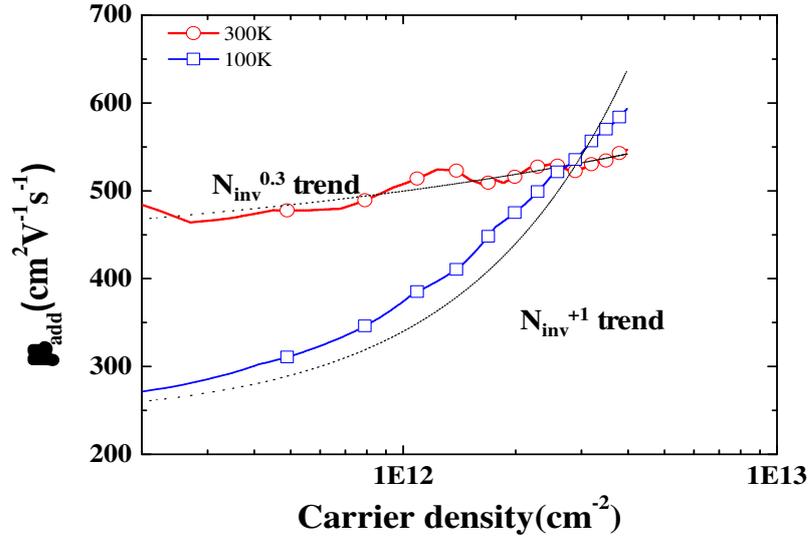
### 6.1.3.3 Additional mobility induced by high- $k$ layer

In a previous work, we have confirmed that the transport characteristics of GO2 devices were similar to universal mobility behaviour because of good electrical quality of both front and back interface, mainly controlled by pure  $\text{SiO}_2$  oxide, while the high- $k$  material of GO1 introduced additional scattering mechanism as compared to GO2 [8]. So as to understand the origin of transport properties with varying  $N_{inv}$ , we exploited the Matthiessen's approach

which can estimate the additional mobility ( $\mu_{\text{add}}$ ) contribution in GO1 using [16],

$$\frac{1}{\mu_{\text{add}}(N_{\text{inv}})} = \frac{1}{\mu_{\text{MR\_GO1}}(N_{\text{inv}})} - \frac{1}{\mu_{\text{MR\_GO2}}(N_{\text{inv}})} \quad (6.5)$$

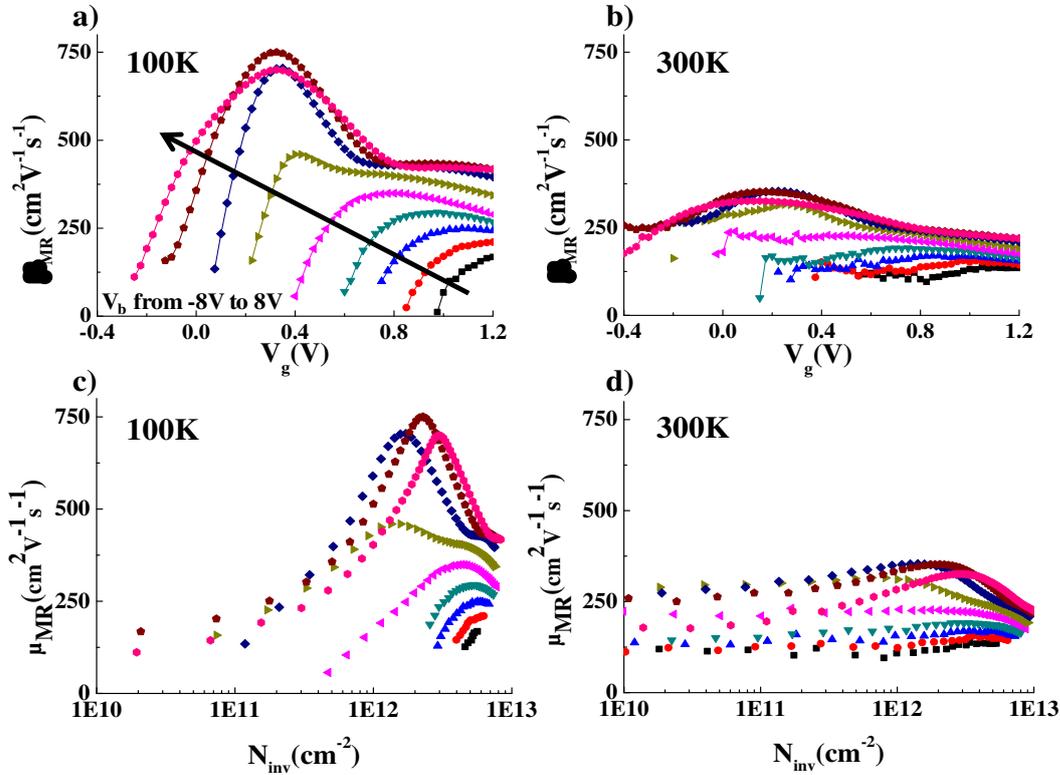
Fig. 6.5 shows  $\mu_{\text{add}}$  as function of  $N_{\text{inv}}$  in GO1 and GO2 devices at two temperatures. This assessment was performed using devices with as close as possible values of gate length, here  $L_G=120\text{nm}$  for GO1 and  $150\text{nm}$  for GO2.



**Figure 6.5** Additional mobility  $\mu_{\text{MR\_add}}$  in GO1 device ( $L_G = 120\text{nm}$ ) compared to GO2 ( $L_G = 150\text{nm}$ ) as function of carrier density for both temperature 100K and 300K, respectively. The  $N_{\text{inv}}^{+1}$  and  $N_{\text{inv}}^{0.3}$  trend are also indicated.

As seen in Fig. 6.5,  $\mu_{\text{add}}$  evolution with  $N_{\text{inv}}$  is totally different at 100K and 300K. Indeed,  $\mu_{\text{add}}$  at 100K follows the  $N_{\text{inv}}^{+1}$  trend which is a characteristic of screened Coulomb scattering over a very large carrier density range. On the other hand,  $\mu_{\text{add}}$  at 300K is governed by the phonon limited mobility which dominates across a wide range of carrier density and has  $N_{\text{inv}}^{0.3}$  dependence. This feature has strong relation with the surface soft polar optical phonon scattering [11, 14]. In these previous works, this kind of “remote” phonon scattering related with high- $k$  dielectric has been recognized by similar carrier density dependence and also was quantified for the mobility degradation by comparing to the universal mobility behavior at room temperature. In our case, the scattering mechanism caused by high- $k$ /metal gate stack can be mainly represented by remote Coulomb scattering (RCS) and surface optical phonon (SOP). These kinds of scattering are usually due to the front gate interface between high- $k$  layer and body in FDSOI devices. Indeed, the devices with GO1 have higher interface trap density than

GO2 case and have big discontinuity between static and optical permittivity. So, according to Fig. 6.5, RCS and SOP are likely the dominant scattering mechanisms at 100K and 300K, respectively.



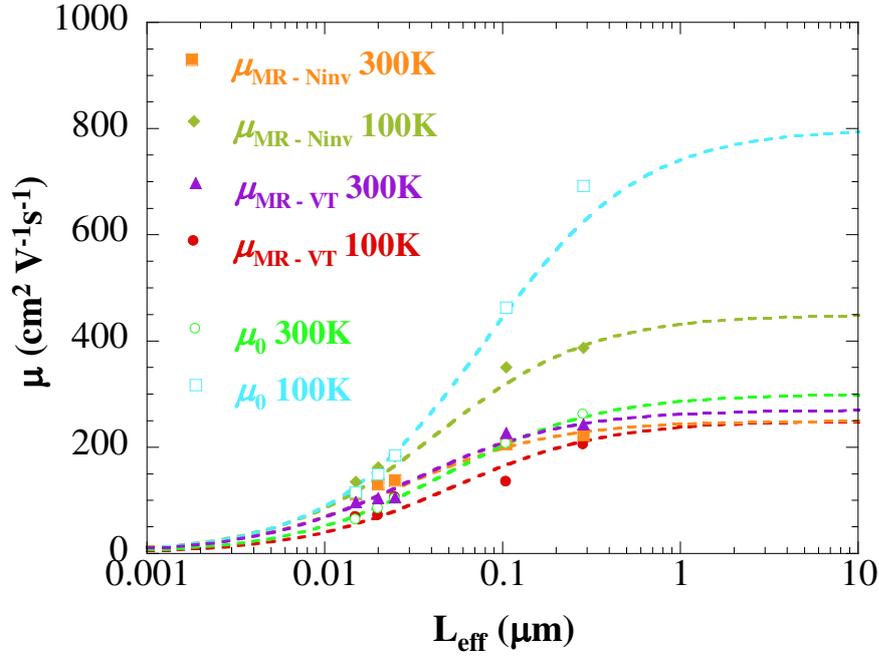
**Figure 6.6** Extracted  $\mu_{MR}$  with  $V_{gs}$  and carrier density  $N_{inv}$  for  $V_b$  varies from  $-8$  to  $8V$  by steps of  $2V$  (indicated by arrow) for GO1 device with  $L_G$  120nm. a), c) at 100K and b), d) at 300K

It is already known that the main centers of additional scattering are located at front side, which means that RCS and SOP associated to the high- $k$  front interface could be attenuated due to increased distance, if the channel carrier centroid can be vertically tuned far from the front side and towards the back side Si/SiO<sub>2</sub> interface which shows better electrical interface quality. This forecast has been convincingly proved by the interface coupling analysis of effective mobility [9]. Moreover, the  $\mu_{MR}$  characterization in interface coupling configuration is demonstrated for the first time to our knowledge. Fig. 6.6 shows the results of GO1 device ( $L_G=120nm$ ) at two temperatures, where a combination of front-gate ( $V_{gs}$ ) and back-gate biases ( $V_b$ ) was used to tune the position of the channel centroid [9]. For forward  $V_b$  and  $V_{gs}$  corresponding to the maximum mobility, we can clearly see that the mobility is enhanced by positive back bias as the carrier centroid is getting closer to the back side. Therefore, it is likely that RCS and SOP weakening (at 100K and 300K, respectively) is partly responsible for the mobility improvement, where the optimized bias value was 6V regardless of temperature. It is also

worth noting that the overall reduction of effective electric field across the silicon channel for a given carrier density leads to a decrease of the SR scattering contribution [17].

#### 6.1.3.4 Mobility degradation factor

In this section, we discuss the comparison between  $\mu_{MR}$  and  $\mu_0$  variation with gate length by using the concept of mobility degradation factor [12]. This approach allows us to empirically characterize mobility degradation in ultra-short channel. It consists of decomposition on the extracted mobility into a long channel component ( $\mu_{long}$ ), which is independent of gate length, and a short channel one which could be fitted by a linear function of gate length. It has been suggested to introduce a parameter  $\alpha$ , namely a mobility degradation factor, defined as follows [12]:



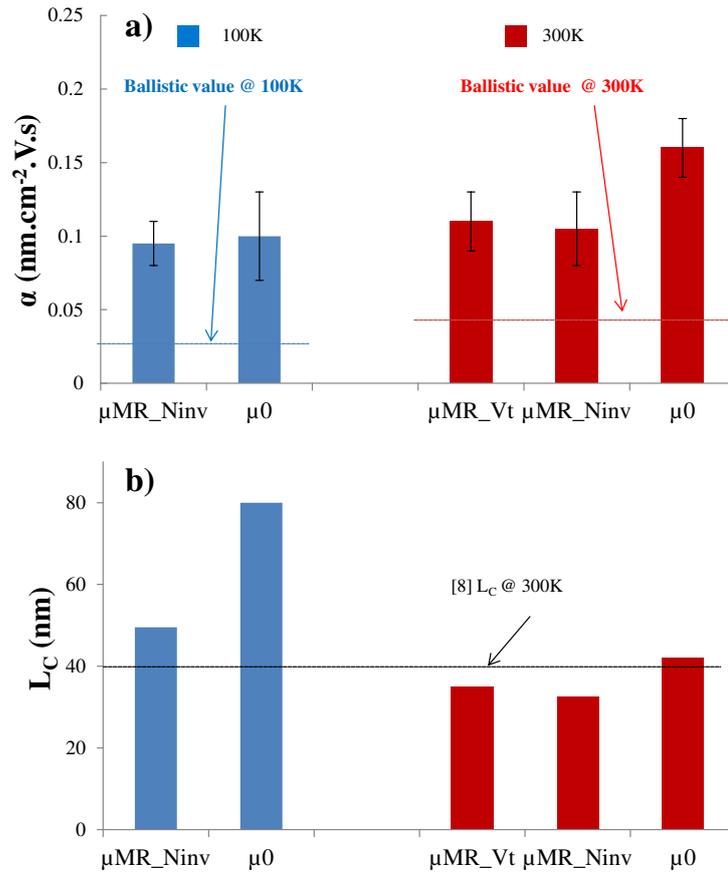
**Figure 6.7** Low field mobility  $\mu_0$  and  $\mu_{MR}$  as function of effective gate length at 100K and 300K, respectively. Points: Experimental data. Lines: fitting function using the mobility degradation factor model. ( $\mu_{MR\_VT}$  and  $\mu_{MR\_Ninv}$  are  $\mu_{MR}$  at  $V_T$  and  $N_{inv} \approx 4 \times 10^{12} \text{cm}^{-2}$ )

$$\frac{1}{\mu_0} = \frac{1}{\mu_{long}} + \frac{\alpha}{L_G} = \frac{1}{\mu_{long}} \left(1 + \frac{L_C}{L_G}\right) \quad (6.6)$$

where  $\alpha$  can be considered as a figure of merit that quantifies the amount of mobility degradation at short gate length featured by a given technology. However, it should be noted that  $\alpha$  can-

not be lower than its minimum value given by the ballistic limit. Several models exist to calculate this limit. Their results are different but the order of magnitudes is similar. We used  $\alpha_{\text{bal}}=2k_{\text{B}}T/(q \cdot v_{\text{inj}})$ , where  $v_{\text{inj}}$  is the injection velocity at source ( $v_{\text{inj}}=1.2 \times 10^7 / 7 \times 10^6 \text{ cm/s}$  and  $\alpha_{\text{bal}}=0.04/0.025 \text{ nm.V.s.cm}^{-2}$  for electron at 300K / 100K without degeneracy consideration [10, 12]. In addition,  $L_{\text{C}} (= \alpha \cdot \mu_{\text{long}})$  corresponds to the critical length where the mobility decreases with factor of 2 as compared with  $\mu_{\text{long}}$ .

Fig. 6.7 depicts the effective gate length dependence of  $\mu_0$  and  $\mu_{\text{MR}}$  at 100K and 300K in GO1 devices. At first, we used Y-function method ( $=I_{\text{d}}/g_{\text{m}}^{0.5}$ ) in order to evaluate  $\mu_0$  which is defined as the extrapolation of effective mobility ( $\mu_{\text{eff}}$ ) at zero gate-overdrive [13]. For proper comparative study,  $\mu_{\text{MR}}$  was extracted for each device both at  $V_{\text{T}}$  ( $\mu_{\text{MR}-V_{\text{T}}}$ ) and for a given value of the inversion charge,  $N_{\text{inv}} \approx 4 \times 10^{12} \text{ cm}^{-2}$ , ( $\mu_{\text{MR}, N_{\text{inv}}}$ ). Also these transport behaviors were reproduced by fitting function of Eq. 6.6. It can be seen that  $\mu_0$  and  $\mu_{\text{MR}}$  are comparable in the whole range of gate lengths at 300K, while there is a huge discrepancy at 100K (cf. Fig. 6.4(d)), especially for long channels, where the neutral defect influence is not significant [8], and unscreened remote Coulomb scattering is actually predominant in this low carrier density regime (around  $10^{11} \text{ cm}^{-2}$ ). There could be two possibilities for origins of the differences; i) in the literature, the difference between the effective and MR mobility has been theoretically studied by the 2 dimensional transport analyses within the Kubo-Greenwood formalism [5]. The calculation is based on the power-law exponent of the mobility on kinetic energy dependence  $\mu(\varepsilon) \propto \varepsilon^n$  (kinetic-energy dispersion relations). If the transport is governed by RCS,  $n$  is equal to 1.5, so that the discrepancy between  $\mu_{\text{eff}}$  and  $\mu_{\text{MR}}$  is more important than for other kind of scattering mechanisms, especially near  $V_{\text{T}}$  (i.e.  $\mu_0 \approx \mu_{\text{eff}} (V_{\text{gs}}=V_{\text{T}})$ ), since it could exceed more than 80% with  $n=1.5$  [15]. For neutral defect scattering, the power-law exponent for  $\mu(\varepsilon)$  is zero, so that  $\mu_{\text{eff}} \approx \mu_{\text{MR}}$  [15]. Since, for small gate lengths,  $\mu_0$  is close to  $\mu_{\text{MR}}$ , it confirms that the relevant scattering mechanisms in the short channel devices is due to neutral defects, which is consistent with our previous analysis based on the  $\mu_0$  temperature dependence [8]. ii) Especially the huge discrepancy was found in the low temperature and long channel devices. As mention earlier, MR mobility method can capture transport properties of low inversion regime in terms of the device operation, which is not available with conventional method, such as Y-function method. It is worth indicating that  $\mu_0$  is extracted by extrapolation from the strong regime. So, it cannot account unscreened RCS as shown in Fig. 6.4(d). Otherwise, the  $\mu_0$  and  $\mu_{\text{MR}}$  are comparable to each other at room temperature.



**Figure 6.8** Comparative benchmarking of a) mobility degradation factor and b) critical length estimated from  $\mu_{MR}$  and  $\mu_0$  approach for 100K and 300K, respectively. Theoretical values of mobility degradation in ballistic transport limits are also indicated [12].

Fig. 6.8(a) summarizes the experimental degradation factor and theoretical value in the ballistic limit at both temperatures [10]. We cannot present  $\alpha$  for  $\mu_{MR\_VT}$  at 100K since the uncertainty of  $\mu_{MR}$  near threshold voltage in short channel devices is too big for a reliable extraction of  $\mu_{MR}$ . In Fig. 6.8(a), we confirmed that the transport properties of our devices are far from ballistic limit based on extracted  $\alpha$  value in different condition even though gate length is ultimately scaled-down. Moreover, even though  $\mu_{long}$  depending on mobility extraction condition is different,  $\alpha$  value for this technology is almost constant around  $0.12 \pm 0.05$  nm.cm<sup>-2</sup>.V.s, regardless of temperature. This uncertainty might become from fitting errors. The mobility performance of such short channel devices can be estimated by the mobility degradation factor. In Fig. 6.8(b) are shown the associated values, the critical length  $L_C (= \alpha \cdot \mu_{long})$ . At first, it can be noted that the  $L_C$  from  $\mu_0$  at low temperature is significantly longer than those obtained with other conditions. This is related to the fact that, as indicated in Fig 4(d),  $\mu_0$  in long channel devices is largely overestimated at 100K. Therefore,  $L_C$  can be strongly exaggerated for similar  $\alpha$ .

The  $L_C$  value at room temperature is around  $35 \pm 5$ nm which is in good agreement with our previous finding [8].

In that paper, we experimentally confirmed that neutral defect scattering becomes predominant for gate length below  $L_C$  as compared to that of phonon. As well as considering the temperature dependence, phonon-limited mobility increases with a temperature reduction, which leads an increase of  $L_C$ . This feature is also well observed in this analysis where  $L_C$  at 100k is slightly longer than that of 300K as seen in Fig. 6.8(b). Therefore, this means that mobility characterization at 300K only could be sufficient to obtain a reliable estimation of the critical length  $L_C$  with the mobility degradation factor.

### 6.1.4 Conclusions

In this chapter, we have presented an extensive study of advanced UTBB FD-SOI devices using magnetoresistance measurements in interface coupling conditions. At first, we found that the gate stack process could influence series resistance. For the advanced devices with high- $k$  / metal gate stack from this technology, series resistance correction in  $\mu_{MR}$  was actually not significant at room temperature. Then, from the analysis of transport mechanisms, we found a nearly Coulomb scattering-free behavior in sub-threshold regime for long channel device at 300K. This behavior is hard to demonstrate using conventional mobility approach, such as low field mobility and effective mobility, because they lose their accuracy or their validity below threshold. The additional scattering mechanisms associated with the high- $k$ /metal gate stack were visible, leading to mobility limitation by RCS or SOP depending on temperature. A bias-induced mobility improvement could be obtained by tuning channel position away from the scattering centers of top interface using the back biasing effect. Finally, it was found that the mobility degradation factor in a given technology does not exhibit big deviation regardless temperature and extraction method. However, critical length can be overestimated by using low field mobility at low temperature due to a lack of ability of Y-function method to capture un-screened RCS.

## 6.2 Experimental and theoretical investigation of magnetoresistance from linear to saturation regime in 14-nm FD-SOI MOS devices

### 6.2.1 Introduction

Ultra-thin body and BOX (UTBB) fully depleted silicon-on-insulator (FD-SOI) MOSFETs are good candidates for adoption in sub-20nm CMOS technology nodes thanks to their interesting potentialities such as superior electrostatic integrity, low variability, hybrid channel and bias-engineered multi- $V_T$  strategies, and performance enhancement [2,20]. Recently, their scalability has been convincingly demonstrated at both device and circuit level, with a low variability suitable for low power specification [1]. In this context, electrical characterization methods and parameter extraction methodologies must be improved to enable the accurate extraction of transport properties from the linear operation to the saturation regime, which actually governs ON current state in real circuit operation.

The mobility concept is no longer meaningful in the saturation regime, due to non-stationary or ballistic effects [21]. Carrier velocity is then a more relevant parameter. The conventional method of velocity extraction is straightforward since we just need to know the ratio of drain current to inversion charge. However, accurate evaluation of the inversion charge is becoming very challenging when the devices are highly scaled-down and are operating at high drain voltage [22]. In this case, the saturation threshold voltage determination is not reliable due to difficult account of drain induced barrier lowering (DIBL) [23]. Recently, gate-to-channel capacitance extraction has been achieved using S-parameters measurements at high frequency, up to 10GHz, in order to properly evaluate inversion charge in the high  $V_d$  regime, allowing direct carrier velocity extraction in deca-nanometer MOS transistors [24]. Nevertheless, even then, an assumption about effective channel length is still mandatory for inversion charge evaluation and, in turn, for velocity extraction.

This chapter reports the first demonstration about the feasibility of geometric magnetoresistance (MR) measurements in the whole range of operation of UTBB FDSOI devices from 14nm-node technology, from linear regime to saturation. It allows an accurate mobility extraction without any need for precise information on the exact physical dimensions and surface carrier density of the devices. A first attempt has already been performed in bulk technology [4], but with no drain current modeling aspects and no consideration of carrier saturation velocity effect. With this work, we developed a new calibrated physical compact model of drain current, which includes magneto-transport phenomenon, and allows physical interpretation of MR mobility and subsequent extraction of carrier saturation velocity.

### 6.2.2 Experiment details

The devices under study were UTBB FD–SOI MOSFETs provided by ST Microelectronics (14nm–node technology). The description of DUT was explained in Chapter 1.4 and the detail information can be found elsewhere [Ref]. We analyzed magnetoresistance mobility ( $\mu_{MR}$ ) variation for different gate length values and gate stack options (GO1 and GO2), in the whole range of operation from linear regime to saturation. These analyses can be enriched by the influence of temperature. The explored range of channel length ( $L$ ) values was selected accordingly, in order to fulfill the geometrical MR requirement [5]. Device fabrication details could be found in the references [2,20,28]. Magneto–transport measurements were carried out using superconducting coils which allowed magnetic field variation between 0T and 11T. Measurements were performed in a cryostat filled by helium where the temperature of the sample could be controlled. The I–V measurements were carried out using an HP4156b semiconductor analyzer.

Once  $\mu_{MR}$  mobility is extracted in linear regime (i.e. at low drain voltage) by using Eq. 6.1, the inversion charge is calculated in first approximation from the drain current by assuming that the effective mobility  $\mu_{eff}$  is close to  $\mu_{MR}$  [5]. However, analysis of the saturation regime requires new developments which are detailed as follows.

### 6.2.3 Physical compact model of high field transport with magnetoresistance effect

In this section, we develop a physical compact model which allows us to calculate the current–voltage characteristics in the drift–diffusion regime under high electric and magnetic field. Within the gradual channel approximation [30], the drain current at any longitudinal position ( $y$ –position) along the channel is given by:

$$I_d(y) = W \cdot \frac{Q_n(y) \cdot \mu_{eff}}{1 + \mu_{eff} E_y(y) / v_{sat}} \frac{dU_c(y)}{dy} \quad (6.7)$$

where  $Q_n(y)$  is the inversion charge density,  $\mu_{eff}$  is the effective mobility in linear regime where the mobility only depends on the transverse electric field ( $E_x$ ) or inversion charge ( $Q_n$ ),  $U_c$  is the quasi Fermi level shift between source and drain (i.e.  $U_c$  at  $y=0$  is zero and  $U_c$  at  $y=L$  is drain voltage ( $V_d$ )),  $v_{sat}$  is the saturation carrier velocity,  $E_y(y) = -d\phi_s(y) / dy$  is the longitudinal field and  $\phi_s$  is the surface potential along the channel. The integration of Eq. 6.7 from 0 to  $L$  in  $y$ –direction after change of variable ( $y \rightarrow U_c$ ) yields:

$$I_d(V_g, V_d) = \frac{\frac{W}{L} \int_0^{V_d} \mu_{\text{eff}}(V_g, U_c) \cdot Q_n(V_g, U_c) \cdot dU_c}{1 + \frac{1}{L} \int_0^{V_d} \frac{\mu_{\text{eff}}(V_g, U_c)}{v_{\text{sat}}} \cdot R(V_g, U_c) \cdot dU_c} \quad (6.8)$$

where the factor  $R = d\phi_s/dU_c$ . In the gradual channel approximation,  $R$  is related to inversion capacitance and gate oxide capacitance as [31]:

$$R(V_g, U_c) = \frac{d\phi_s}{dU_c} \approx \frac{C_{\text{inv}}(V_g, U_c)}{C_{\text{inv}}(V_g, U_c) + C_{\text{ox}}} \quad (6.9)$$

In particular, in the sub-threshold regime,  $R$  is close to zero and there is no  $v_{\text{sat}}$  effect as the longitudinal field is nearly zero in the channel at high  $V_d$ , whereas in strong inversion,  $R \approx 1$ , so that the  $v_{\text{sat}}$  effect is fully activated.

For the inversion charge in Eq. 6.8, we used an explicit analytical model as function of gate voltage and channel potential, based on the Lambert  $W$ -function [32]:

$$Q_n(V_g, U_c) = C_{\text{ox}} \cdot \frac{k_B T}{q} \cdot \text{Lw} \left( \exp \left( \frac{V_g - V_T}{k_B T / q} - \frac{U_c}{p \cdot k_B T / q} \right) \right) \quad (6.10)$$

where the factor  $p$  could refine the  $U_c$  effect in order to reproduce the experimental data. Here, we used 1.2 instead of unity. We used the experimental threshold voltage which contains the work-function difference, fixed oxide charges and interface states contribution. The shift due to drain induced barrier lowering (DIBL) was taken into account by using the effective gate voltage  $V_g^{\text{eff}}$  defined as:

$$V_g^{\text{eff}} = V_g + \lambda \cdot V_d \quad (6.11)$$

where  $\lambda$  is the DIBL coefficient. Moreover, for the magneto-transport, we used the Drude-Boltzmann approach [5]. We suppose that the magnetic field does not change the threshold voltage. For the calculation of  $I_D(V_g, V_d, B)$  under magnetic field, we replace  $\mu_{\text{eff}}$  of Eq. 6.8 by:

$$\mu_{\text{eff}}(B) = \frac{\mu_{\text{eff}}}{1 + (\mu_{\text{eff}} B)^2} \quad (6.12)$$

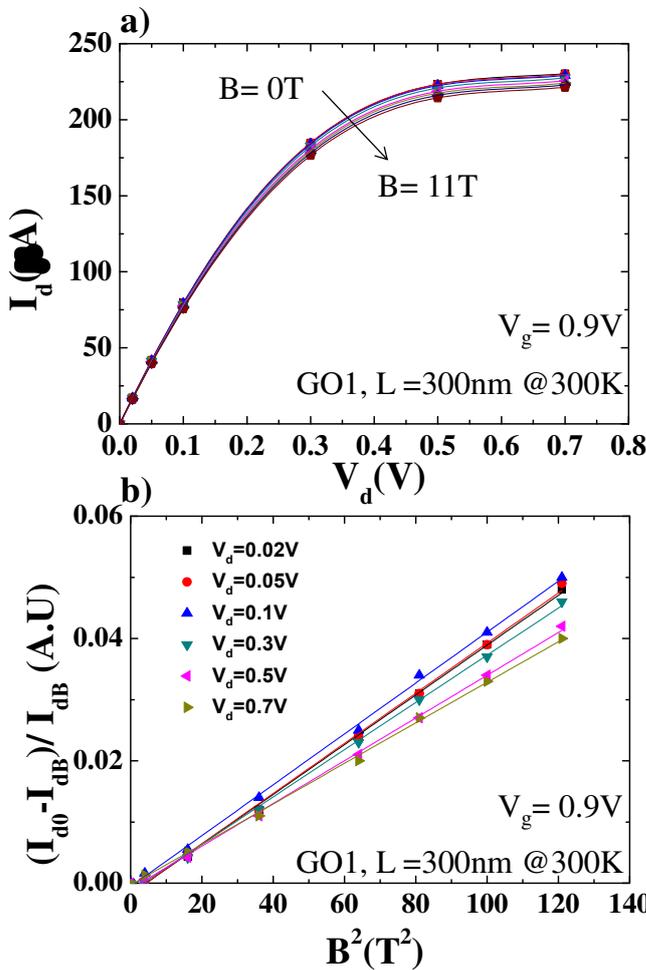
in order to account for the MR effect. The apparent  $\mu_{\text{MR}}$  for the whole device can then be

obtained from simulated results as:

$$\mu_{MR}(V_g, V_d) = \frac{1}{B} \sqrt{\frac{I_d(V_g, V_d, B=0) - I_d(V_g, V_d, B)}{I_d(V_g, V_d, B)}} \quad (6.13).$$

## 6.2.4 Results and discussions

### 6.2.4.1 $\mu_{MR}$ extraction procedure



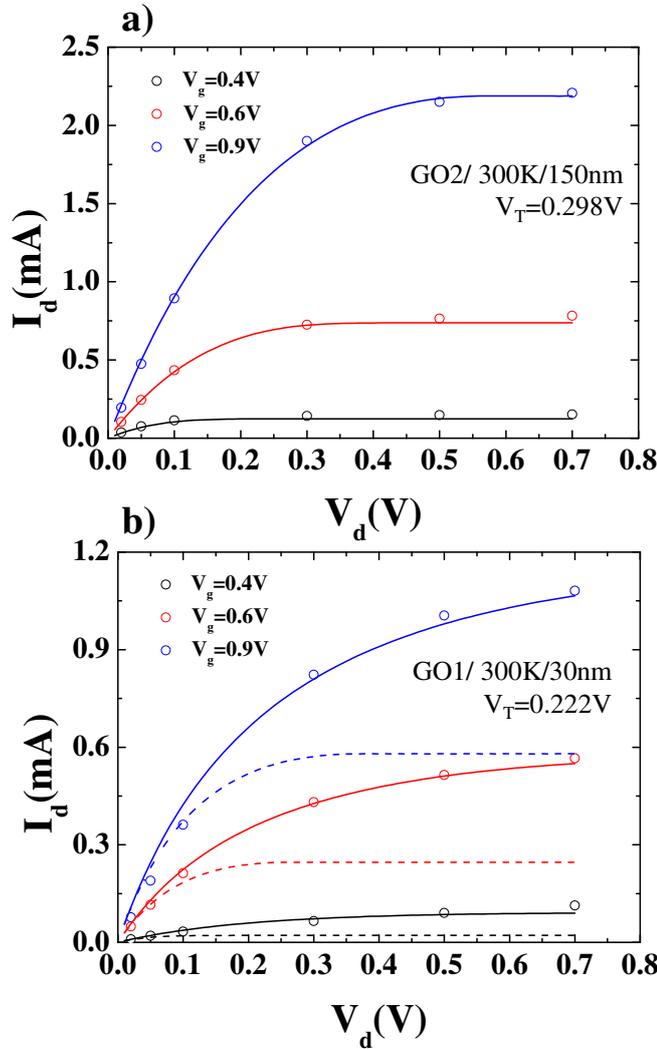
**Figure 6.9** a) Output characteristic ( $I_d$ - $V_d$ ) at strong inversion regime ( $V_g = 0.9\text{V}$ ) for different magnetic fields  $B$  from  $0\text{T}$  to  $11\text{T}$  at  $300\text{K}$  for GO1 device ( $W=1\mu\text{m}$ ,  $L=0.3\mu\text{m}$ ). b) Relative drain current variation ( $\Delta I_d/I_{dB}$ ) vs.  $B^2$  from linear ( $V_d = 0.02\text{V}$ ) to saturation regime ( $V_d = 0.7\text{V}$ ).

Fig. 6.9(a) shows the influence of magnetic field  $B$  (varied from  $0\text{T}$  to  $11\text{T}$ ) on the output characteristics, i.e. drain current variation with  $V_d$  from linear regime to saturation, in strong inversion ( $V_g=0.9\text{V}$ ), for the GO1 devices, at  $300\text{K}$ . We can observe the MR behavior in the whole range of drain voltages, especially in saturation. As shown in Fig. 6.9(b), the relative drain current variation is proportional to  $B^2$  in the whole range of drain voltage, with excellent

linearity. Interestingly, this feature means that an apparent MR mobility can be directly extracted from linear regime to saturation without any assumption on dimensions [4].

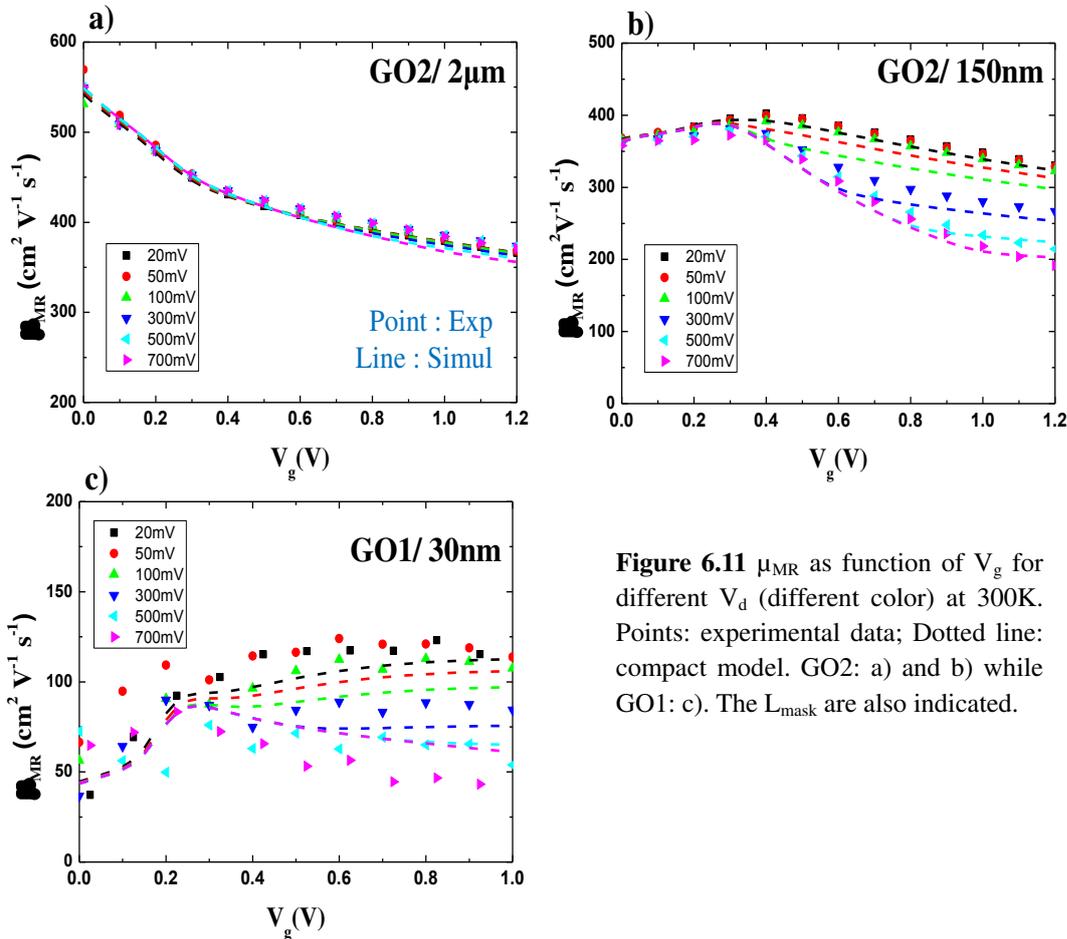
#### 6.2.4.2 Modeling of I–V and $\mu_{MR}$ in all operation regimes

In this section, we assess the ability of our compact model for drain current and  $\mu_{MR}$  modeling in all operation regimes of gate and drain voltages. In order to avoid any fitting of the low field mobility, we first extract  $\mu_{MR}$  in the linear regime, at  $V_d=0.02V$ , for various gate voltages, enabling the effective  $\mu_{eff} \approx \mu_{MR}$  to be known vs inversion charge for each gate length. This empirical law  $\mu_{eff}(Q_n)$  is then used in the model of Eq. 6.8 for further drain current and  $\mu_{MR}$  calculations in all other operation regimes from linear to saturation.



**Figure 6.10** Output characteristics ( $I_d$ - $V_d$ ) for different  $V_g$  at 300K without B. Lines: compact model ( $v_{sat}$  is set to  $10^7$  cm/s and  $2 \times 10^7$ , respectively). Points: experimental data. a) For GO2 devices,  $L_{mask}=50nm$ . b) For GO1 devices,  $L_{mask}=30nm$ . Dotted lines: the SCE is ignored. Solid lines: SCE is taken into account with  $\lambda=0.7$ . The threshold voltages  $V_T$  in linear regime are also indicated.

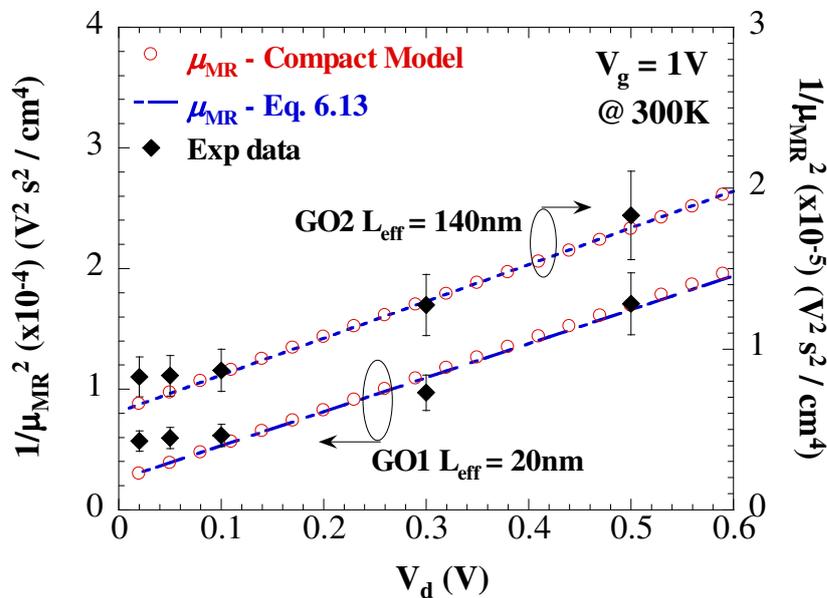
Fig. 6.10 shows the output characteristics  $I_D-V_d$  with different  $V_g$  at 300K, for devices of GO2 ( $L_{\text{mask}}=150\text{nm}$ ) and GO1 ( $L_{\text{mask}}=30\text{nm}$ ). As can be observed from Fig. 6.10, a good agreement between experiment and compact model of Eq. 6.8 is obtained. For the long channel devices (cf. Fig. 6.10(a)), the short channel effect (SCE), effective length and saturation velocity effects could be neglected overall. In other words,  $V_g^{\text{eff}}=V_g$  and  $L=L_{\text{mask}}$ . However, in the short channel case (cf. Fig. 6.10(b)), these effects had to be taken into account. Good agreement between experimental results and compact modelling was obtained with a DIBL factor  $\lambda$  in Eq. 6.11 equal to 0.7 and an effective channel length  $L=L_{\text{mask}}-\Delta L$  where  $\Delta L=15\text{nm}$ , which is consistent with  $L_{\text{eff}}$  extraction from split CV measurements [8]. The fitting value of carrier saturation velocity is around  $v_{\text{sat}}\approx 2\times 10^7\text{cm/s}$ , which is larger than in bulk case or in longer devices, consistently with the possible contribution of non-stationary transport.



**Figure 6.11**  $\mu_{\text{MR}}$  as function of  $V_g$  for different  $V_d$  (different color) at 300K. Points: experimental data; Dotted line: compact model. GO2: a) and b) while GO1: c). The  $L_{\text{mask}}$  are also indicated.

As shown in Fig. 6.11, quite acceptable agreement can be obtained for  $\mu_{\text{MR}}$  between experimental data and compact model in both gate and drain voltage range. It is worth noting that, for very long channel devices (cf. Fig. 6.11(a)),  $\mu_{\text{MR}}$  is almost independent of  $V_d$ , which

means that the longitudinal field  $E_y$  is too small to significantly influence effective mobility. Thus, in this case, mobility attenuation by the longitudinal electric field can be ignored for drain current calculation. However, as the gate length gets shorter, the longitudinal field in the channel increases. Then, as can be seen in Fig. 6.11(b), the MR mobility becomes drain voltage dependent above threshold. This means that the saturation velocity effect now starts to play a significant role in Eqs. 6.7 and 6.8, and cannot be neglected in drain current and MR mobility evaluation. Moreover, for highly scaled device, the effective length is downscaled to 15nm, which could intuitively lead to a stronger  $V_d$  effect. So, in order to make a proper comparison of  $V_d$  effect between long and short devices, it is better to normalize the mobility variation with  $V_d$  for a given gate voltage, using  $(\mu_{\text{linear}} - \mu_{\text{saturation}}) / \mu_{\text{linear}}$ . As can be seen, there is up to 38% and 50% mobility reduction for these devices with  $L_{\text{mask}} = 150\text{nm}$  and  $L_{\text{mask}} = 30\text{nm}$ , respectively. It is worth noting that the longitudinal electrical field ( $V_d / L_{\text{eff}}$ ) for ultra-scaled devices is 10 times stronger in the shortest devices, which means that the mobility degradation induced by such longitudinal field could be expected to be larger. However, this effect is attenuated because the low field mobility in 30nm GO1 devices (effective length is 15nm) is much smaller than in 150nm GO2 ones. This mobility degradation at short channel lengths in GO1 devices has been attributed to enhanced process-induced neutral defect scattering due to source/drain proximity [8,9,25,27].



**Figure 6.12**  $1/\mu_{\text{MR}}^2$  as function of  $V_d$ . Eq. 6.13 is assessed by experimental data and compact model. For GO2 device (right scale), mask length  $L_{\text{mask}} = 150\text{nm}$ . For GO1 device (left scale),  $L_{\text{mask}} = 35\text{nm}$ .

### 6.2.4.3 Carrier velocity extraction

In the previous sections, we focused on the transport behavior from linear regime to saturation by modeling the apparent MR mobility  $\mu_{MR}$ , versus  $V_g$  for various  $V_d$ , and the carrier velocity was used as a fitting parameter. Here, we suggest a simple  $\mu_{MR}-V_d$  relationship, in the strong inversion regime where  $V_d$  effect is maximized. To this end and for the sake of simplicity, we consider that, in Eq. 6.8, mobility is a constant,  $\mu_{eff}=\mu_0$ , and we evaluate the drain current in strong inversion. This yields after integration of Eq. 6.8 for  $I_D$  in the presence of a magnetic field:

$$I_d(V_g, V_d) = \frac{W}{2L} \cdot \frac{\mu_{0B} \cdot C_{ox}}{1 + \frac{\mu_{0B} \cdot V_d}{L \cdot v_{sat}}} \cdot \left[ (V_g - V_T)^2 - (V_g - V_T - V_d)^2 \right] \quad (6.14)$$

where  $\mu_{0B}=\mu_0/(1+\mu_0^2B^2)$ . So, by using Eq. 6.1, the apparent MR mobility  $\mu_{MR}$  can be obtained as:

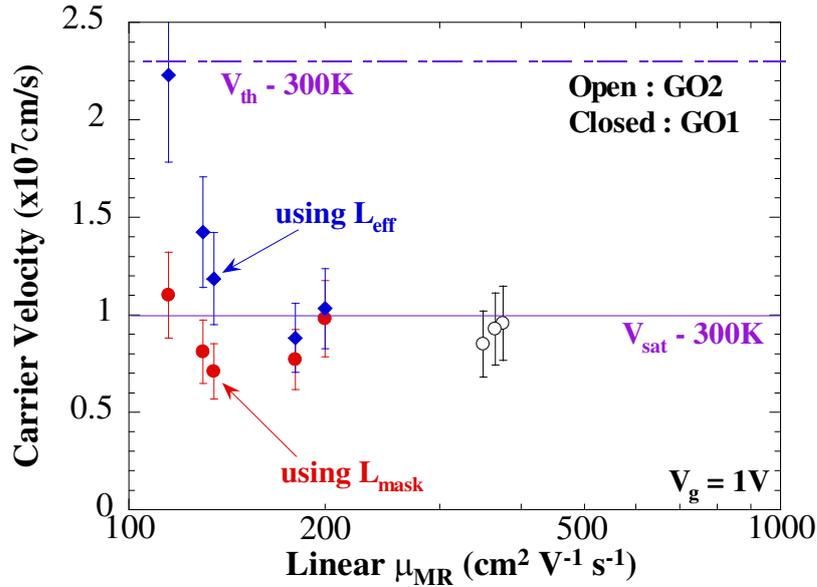
$$\mu_{MR}(V_d) = \frac{\mu_{MR\_Lin}}{\sqrt{1 + \frac{V_d \cdot \mu_{MR\_Lin}}{L_{eff} \cdot v_{sat}}}} \quad (6.15)$$

Therefore, by plotting the variation of  $1/\mu_{MR}^2$  as function of  $V_d$ , a straight line should be obtained with the slope giving information about the carrier saturation velocity. As shown in Fig. 6.12, this behavior is well verified experimentally for  $V_d > 0.1V$ . Moreover, both the analytical model of Eq. 6.15 and the compact model of Eqs. 6.8–13) are providing good fit to experimental data. This has been achieved by properly adjusting the carrier saturation velocity to  $v_{sat}=10^7$ cm/s and  $v_{sat}=1.4 \times 10^7$ cm/s, respectively for GO2 and GO1 devices, provided the use of proper effective channel lengths. These values are consistent with those used to fit the  $I_d-V_d$  curves of Fig. 6.10, emphasizing the reliability of this carrier saturation velocity extraction method. Fig. 6.13 summarizes all the carrier saturation velocities values which were extracted using this method and plots them as a function of the  $\mu_{MR}$  value extracted in linear regime, for GO1 and GO2 devices of different gate lengths.

For GO2 devices, which have good interface quality, the gate mask lengths are 250nm, 200nm and 150nm. So, the extracted carrier saturation velocity is very close to the saturation velocity in bulk case. Using mask length and effective length does not change these results. Same behavior could also be observed in GO1 devices (300 nm and 120 nm). But for short channel devices, we can clearly see the velocity overshoot effect due to non-equilibrium

transport, resulting in an increase of the saturation velocity as the gate length is reduced, especially when using effective gate lengths [35–37].

#### 6.2.4.4 Comparative analysis of carrier velocity



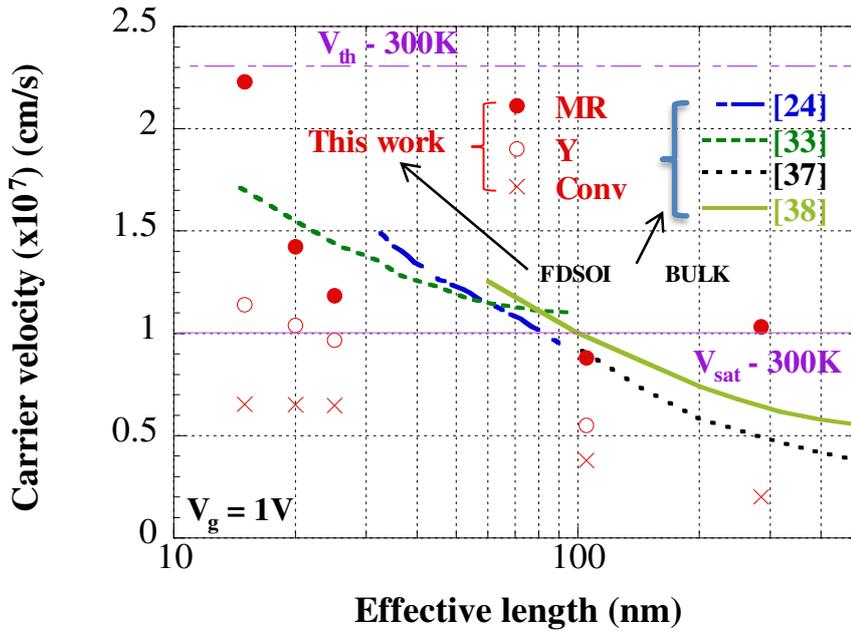
**Figure 6.13** Extracted average carrier velocity as function of  $\mu_{MR}$  in linear regime at 300K for  $V_g = 1\text{V}$  in GO1 (closed) and GO2 (open) devices. The results using the effective gate length and mask length are indicated. The gate length is decreased as decreasing of  $\mu_{MR}$  in linear regime. In addition, the corrected thermal velocity by degeneracy factor and saturation velocity in bulk semiconductor at 300K are also indicated [33, 34].

The carrier velocity values extracted by using this new procedure were benchmarked with other results. Before doing so, we will first recall existing methods for carrier velocity extraction. The conventional method is based on saturation drain current expressed at source end as [38]:

$$v_{\text{sat}} = I_{\text{dsat}} / W \cdot C_{\text{ox}} \cdot (V_g - V_{\text{Tsat}}) \quad (6.16)$$

where  $V_{\text{Tsat}}$  is the saturation threshold voltage.  $V_{\text{Tsat}}$  can be directly extracted in saturation or deduced from linear  $V_{\text{Tlin}}$  as  $V_{\text{Tsat}} = V_{\text{Tlin}} + \text{DIBL} \cdot V_d$ , the DIBL being extracted in subthreshold regime. Another method consists in using the  $Y$ -function,  $Y = I_d / \sqrt{g_m}$ , extended to the high  $V_d$  regime. The saturation velocity could then be obtained from the plot of low charge apparent mobility versus  $V_d$  [39]. High frequency (HF)  $C_{gc}$  measurements have also been used to calcu-

late the inversion charge as a function of  $V_d$  and, in turn, to directly evaluate the carrier velocity from  $I_{dsat}/(W \cdot Q_{inv})$  [22, 24]. Finally, the concept of apparent mobility was employed to obtain the limiting velocity in saturation, which is obtained from the plot of the gate length normalized difference between mobility in linear regime and apparent mobility in saturation, as a function of gate overdrive [34].



**Figure 6.14** Extracted carrier velocity at 300K in strong inversion from MR, Y and Conventional method as a function of effective gate length. Other results published for Bulk MOSFET technologies in [24] using HF  $C_{gc}$  method, [33] using limiting velocity, [37] and [38] using the drift velocity fitting parameter and saturated transconductance within resistive gated MOS approximation are also plotted for comparison, for similar operation point.

For the sake of comparison, we have extracted the carrier velocity of device GO1 at 300K in strong inversion using MR, Y-function and conventional method and we have also compared our results to previously published data [24, 34, 37, 38] obtained under similar operation conditions in Bulk MOSFET technologies (see Fig. 6.14). First, we note that the extracted velocities are increasing as the gate length is reduced, regardless of the extraction method. However, the conventional method reaches a strongly underestimated limit at small device length, compared to the bulk limit. In contrast, Y-function and MR results show similar trend with a clear velocity increase for short channel devices, but with larger values for MR. This velocity increase at small gate length is expected and has been interpreted as a velocity overshoot effect due to non-stationary transport [34–38]. The comparison of MR velocity data to other published results from HF  $C_{gc}$  measurement [24] and limiting velocity extraction [24]

shows similar trends, with values exceeding bulk saturation velocity for the shortest devices. It should be noted that the large  $v_{\text{sat}}$  value obtained for the shortest device could be due to the underestimation of the effective channel length. However, our results underline the global consistency of MR based saturation velocity extraction in ultra-short MOS transistors, offering alternative and complementary means compared to other techniques.

### 6.2.5 Conclusions

In this chapter, we have demonstrated for the first time the feasibility of geometric MR extraction in the whole range of operation (from linear to saturation regime and also from sub-threshold regime to strong inversion regime) of advanced FDSOI devices from 14nm-node technology. A physical compact model of high field transport was proposed, which, by using field-dependent mobility approach and magnetic field dependence, was capable of reproducing experimental  $\mu_{\text{MR}}$  in this whole range of operation regimes. The extracted values of saturation velocity were showing physically meaningful trends and were comparing well with other methods and published data, which emphasizes the reliability of our new methodology of carrier velocity extraction. The high field transport properties were well interpreted by both saturation velocity and overshoot effects due to non-stationary transport in highly scaled devices. MR characterization technique and our theoretical methodologies demonstrated their advantages and potentialities for future ultimately scaled devices with specific supply voltage requirement.

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# Chapter 7

## Low-frequency noise characterization of 14nm-node FD-SOI CMOS transistors

### 7.1 Introduction

The LF noise is one of the most important indicators related with the electronic devices in terms of interfacial quality and reliability [1–8]. And, the characterization of LF noise does not require the devices destruction unlike other methods such as the transmission electron microscopy. As the CMOS technology has progressed scaling-down, the thickness of gate dielectric has decreased [2]. Thus, the evaluation of interface quality is essential for the proper operation of analog and digital circuits with nano-scaled CMOS technologies [9,10]. In MOSFET, the LF noise behavior typically shows 1/f or flicker noise which could be interpreted with either the Hooge mobility fluctuation model or the carrier number fluctuation (CNF) with/without correlated mobility fluctuation (CMF) model [1,6,11,12]. The former is explained with phonon scattering and the latter is originated by trapping and de-trapping near interface between the channel and the gate dielectric layer.

In this chapter, we characterized the LF noise properties of the 14nm-node fully depleted silicon-on-insulator (FD-SOI) CMOS transistors. Ultra-thin body and BOX (UTBB)

FD-SOI devices have a lot of interest as the promising candidates for future CMOS technology nodes due to excellent electrostatic integrity, high performance and low variability [13]. In addition, the multi- $V_T$  strategies with a wide range of the voltage bias can be useful for UTBB architecture with static and dynamic back plane (BP) biasing engineering [14]. The aim of this chapter is to investigate LF noise characteristics of various FD-SOI devices depending on type of devices (NMOS and PMOS), channel length and Ge content, especially for SiGe channel. In addition, we revealed that the CNF with CMF model is well explained  $1/f$  noise behavior of advanced FD-SOI devices in not only linear operation regime to saturation regime [4,5].

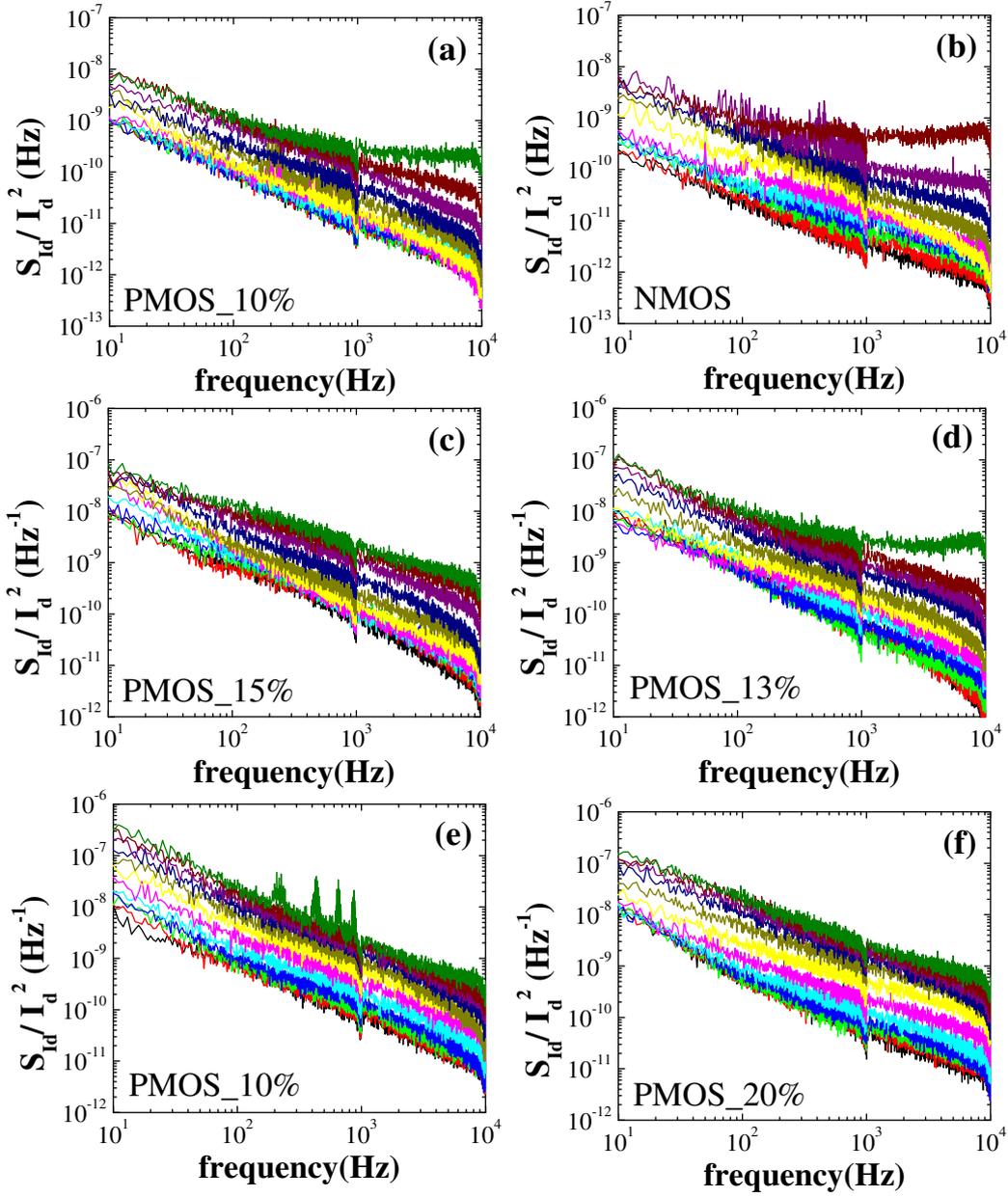
## 7.2 Experiment details

The devices under study were UTBB FD-SOI MOSFETs provided by ST Microelectronics (14nm-node technology). The description of DUT was explained in Chapter 1.4 and the detail information can be found elsewhere [15,16]. The  $\Delta L (=L_M - L_{eff})$  were found around 15nm, which were extracted by extrapolation to zero channel length [17,18]. For the appropriate comparative study, we selected the devices with common width ( $W=1\mu\text{m}$ ) and different channel length ( $L_M=1\mu\text{m}$ , 120nm and 30nm). The I-V and noise measurements were carried out using HP4156b and Programmable Pint-Probe Noise Measuring System (3PNMS) with elite 300 probe station [19]. The noise measurement bandwidth is from 10Hz to 10kHz.

## 7.3 Results and Discussions

### 7.3.1 Noise characterization in the linear regime

The noise measurement was carried out for various devices from 10Hz to 10kHz, where drain voltage ( $V_d$ ) was 20mV in linear regime and gate voltage ( $V_g$ ) varied from weak inversion to strong inversion regime. As shown in Fig. 7.1, normalized drain current power spectral density (PSD) with different  $V_g$  shows  $1/f$  dependence regardless of device type, channel length and Ge content. This LF noise behavior can be accounted by two models. One is Hooge mobility fluctuation model which is related with phonon scattering [1,6,11]. The other one is carrier number fluctuation (CNF) model with correlated mobility fluctuation (CMF) [1,6,12]. It is originated from charge trapping and de-trapping at interfacial layer between channel and oxide, which is equivalent with fluctuation of flat band voltage ( $V_{fb}$ ) [1,6,12]. In addition, the carrier transport properties can be influenced by oxide charges. The drain current PSD of this model can be expressed by:



**Figure 7.1** The drain current power spectral density for (a) PMOS (Ge 10%) with  $L=1\mu\text{m}$ , (b) NMOS with  $L=1\mu\text{m}$ , (c) PMOS (Ge 15%) with  $L=120\text{nm}$ , (d) PMOS (Ge 13%) with  $L=120\text{nm}$ , (e) PMOS (Ge 10%) with  $L=30\text{nm}$  and (f) PMOS (Ge 20%) with  $L=30\text{nm}$  as a function of frequency. (All devices with  $W=1\mu\text{m}$ )

$$\frac{S_{I_d}}{I_d^2} = \frac{g_m^2}{I_d^2} S_{v_{fb}} \left(1 + \Omega \frac{I_d}{g_m}\right)^2 \quad (7.1)$$

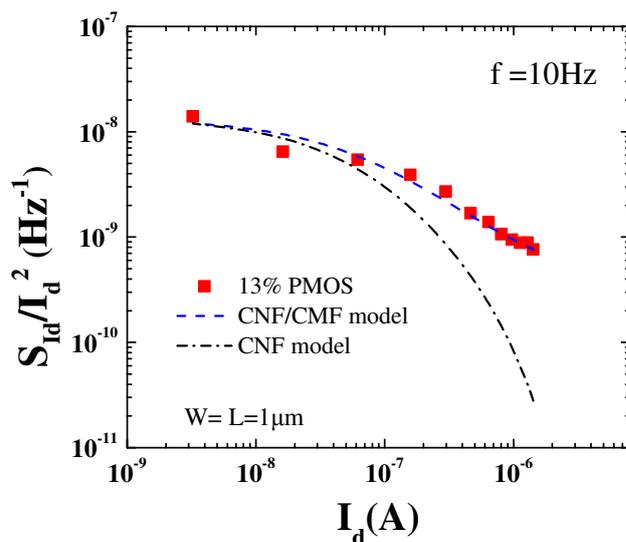
where  $S_{v_{fb}}$  is flat band voltage PSD. The  $S_{v_{fb}}$  and  $\Omega$  are defined:

$$S_{v_{fb}} = \frac{q^2 kT \lambda N_t}{W L C_{ox}^2 f} \quad (7.2)$$

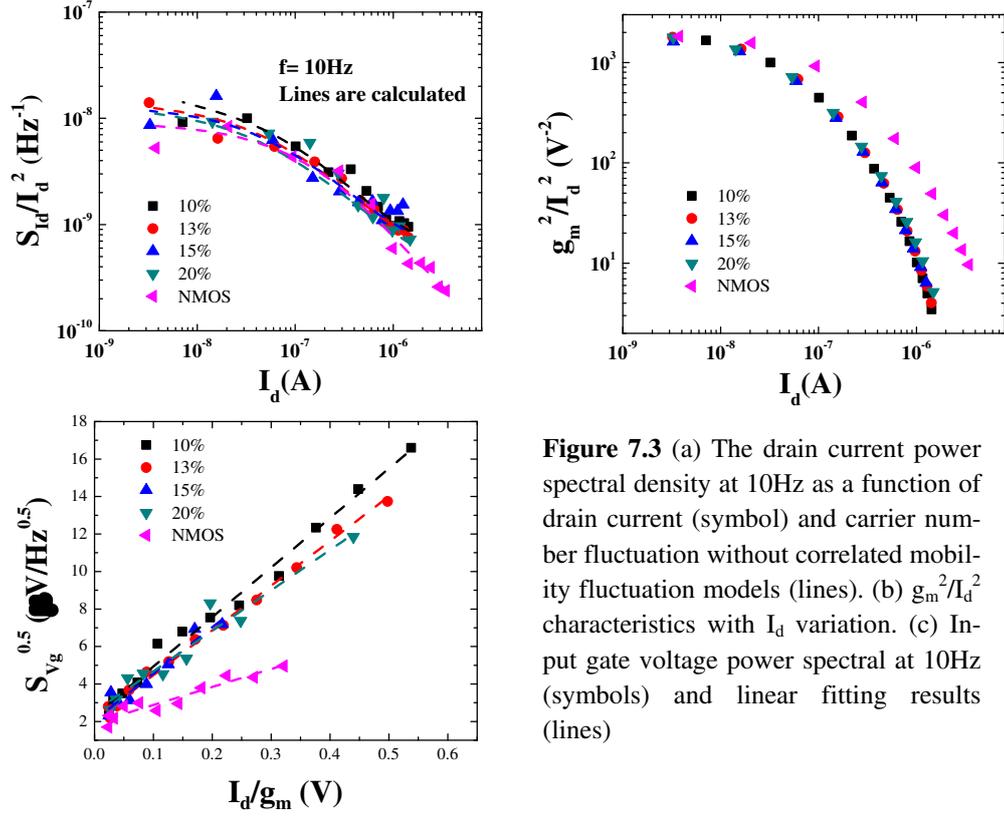
$$\Omega = \alpha_{sc} \mu_{eff} C_{ox} \quad (7.3)$$

where  $kT$  is the thermal energy,  $\lambda$  is the tunneling attenuation distance ( $\sim 0.1\text{nm}$  in  $\text{SiO}_2$ ),  $C_{ox}$  is the gate oxide capacitance per unit area,  $N_t$  is the trap density in the gate dielectrics  $\alpha_{sc}$  is the Coulomb scattering coefficient, and  $\mu_{eff}$  is the effective carrier mobility.

In order to confirm which model is well matched with experimental results, we plotted how drain current PSD at 10Hz changes with drain current variation in Fig. 7.2 ( $W=L=1\mu\text{m}$  and PMOS with Ge 13%). It is clear that CNF with CMF model describes more appropriately as compared to CNF model ( $\alpha=0$ ). This behavior commonly appears conventionally other LF noise researches with FD-SOI devices [20–22]. So, we are focusing to this model for analyzing LF noise properties of our devices.



**Figure 7.2** The drain current power spectral density at 10Hz as a function of drain current (symbol) and carrier number fluctuation with/without correlated mobility fluctuation models (lines).



**Figure 7.3** (a) The drain current power spectral density at 10Hz as a function of drain current (symbol) and carrier number fluctuation without correlated mobility fluctuation models (lines). (b)  $g_m^2/I_d^2$  characteristics with  $I_d$  variation. (c) Input gate voltage power spectral at 10Hz (symbols) and linear fitting results (lines)

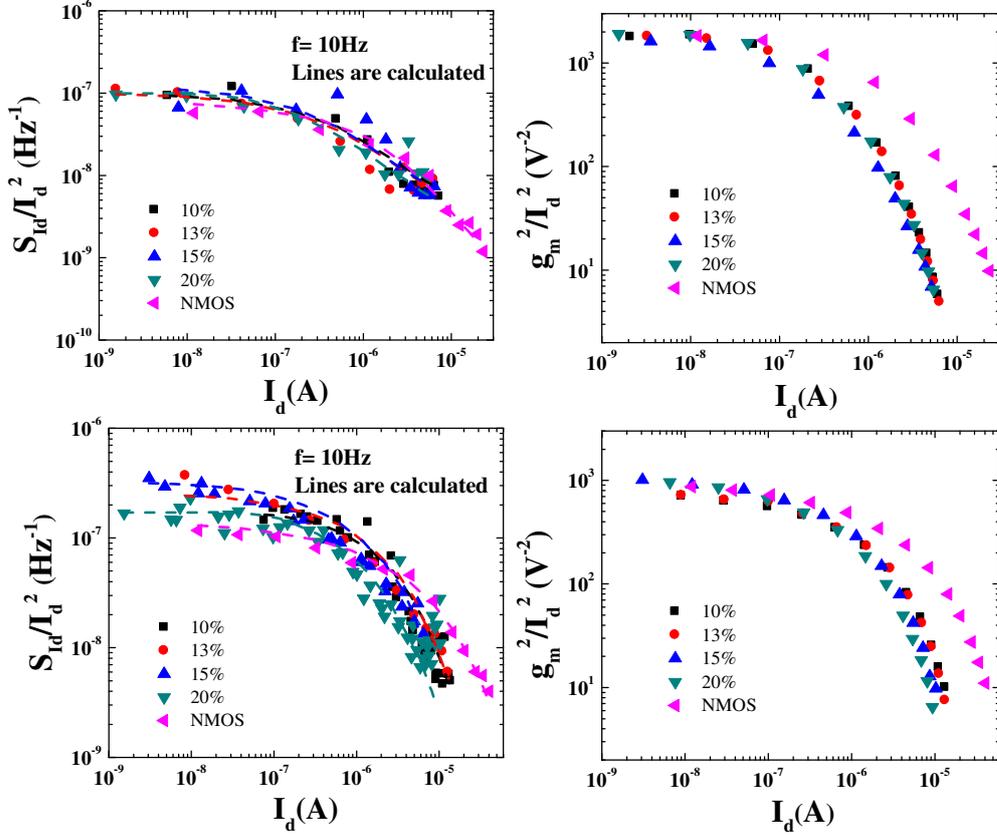
In the same manner, Fig. 7.3(a) denotes drain current PSD of all kinds of device with  $L=1\mu\text{m}$  as a function of drain current. The normalized PSD level from all devices is somehow identical. We cannot find marked deviation among NMOS and PMOS with different Ge content. The shape of  $S_{I_d}/I_d^2$  and  $g_m^2/I_d^2$  shows similar tendency with drain current in Fig. 7.3(a) and (b). It means that CNF with CMF model well explains LF noise behavior of FD-SOI transistors as considering Eq. 7.1. In order to extract electrical parameters such as  $N_t$ , input gate voltage spectral density ( $S_{V_{\text{fg}}} = S_{I_d}/g_m^2$ ) was exploited,

$$S_{V_{\text{fg}}} = S_{V_{\text{fb}}} \left(1 + \Omega \frac{I_d}{g_m}\right)^2 \quad (7.4),$$

$$\sqrt{S_{V_{\text{fg}}}} = \sqrt{S_{V_{\text{fb}}}} \left(1 + \Omega \frac{I_d}{g_m}\right) \quad (7.5).$$

As shown in Fig. 7.3(c),  $S_{V_{\text{fg}}}^{0.5}$  has linear relationship with  $I_d/g_m$ . So,  $S_{V_{\text{fb}}}$  and  $\Omega$  can be extracted from the slope and intercept point of Eq. 7.5, which are consistent with fitting results of Eq. 7.1 with experimental data of  $S_{I_d}/I_d^2$  versus  $I_d$  in Fig. 7.3(a). It is worth noting that  $\Omega$  shows constant from in weak inversion to strong inversion. In other words,  $\alpha_{\text{sc}}\mu_{\text{eff}}$  product is constant for

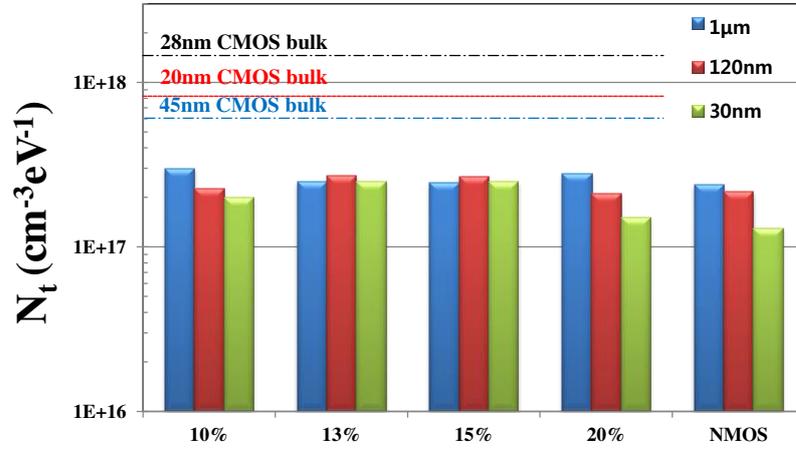
whole operation regime, which is consistent with [4]. However, each  $\alpha_{sc}$  and  $\mu_{eff}$  cannot be uniform since  $\mu_{eff}$  definitely varies with gate voltage due to surface roughness scattering [23].



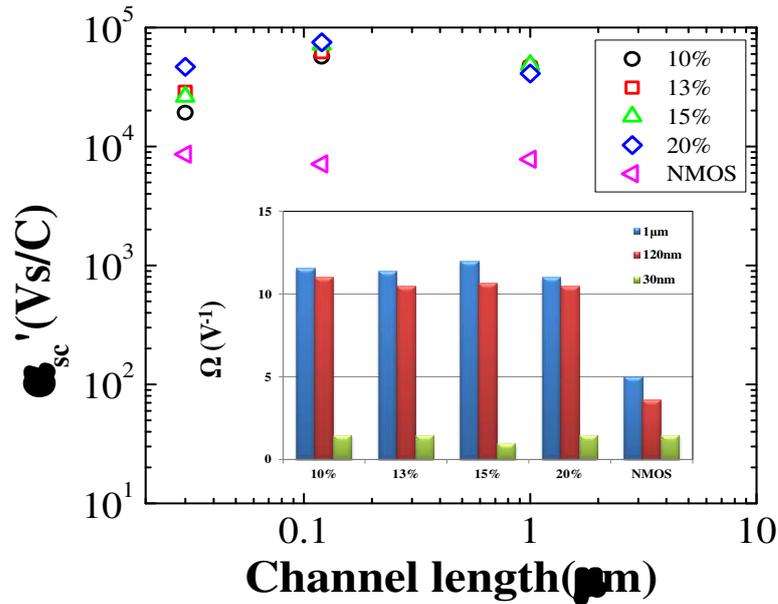
**Figure 7.4** The drain current power spectral density at 10Hz as a function of drain current (symbol) and carrier number fluctuation with correlated mobility fluctuation models (lines) for (a)  $L=120\text{nm}$  and (c)  $L=30\text{nm}$ .  $g_m^2/I_d^2$  characteristics with  $I_d$  variation for (b)  $L=120\text{nm}$  and (d)  $L=30\text{nm}$ .

Fig. 7.4(a) and (c) display normalized PSD at 10Hz versus drain current for various devices with smaller channel lengths ( $L=120\text{nm}$  and  $L=30\text{nm}$ ). As the long channel devices, the  $g_m^2/I_d^2$  variation with drain current in Fig. 7.4(b) and (c) is similar with that of normalized PSD. Consequently, the fitting results with Eq. 7.1 can well reproduce the characteristics of LF noise. Thus, the CNF with CMF model is still validate regardless decrease of the channel length. The all extracted  $N_t$  and  $\Omega$  by using Eqs. 7.1 and 7.5 are summarized in Figs. 7.5 and 7.6. When we take a look Fig. 7.5,  $N_t$  values indicate more or less constant ( $\approx 1\sim 3 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$ ), which is not dependent with type of devices, channel length and Ge content. It manifests that the device fabrication process was properly controlled and the high quality of interfacial layer between channel and oxide layers was demonstrated with not only long channel devices, but also ultra-scaled devices. Moreover, this quality was enhanced when we compare to the previous

technologies such as the 20nm CMOS bulk technology of STMicroelectronics [2]



**Figure 7.5** The extracted trap density ( $N_t$ ) for different Ge concentrations and channel lengths. The  $N_t$  values from previous STMicroelectronics' CMOS technologies are indicated with lines [2].



**Figure 7.6** The extracted corrected Coulomb scattering coefficient and (inset)  $\Omega$  for different Ge concentrations and channel lengths.

The inset of Fig. 7.6 displays the extracted  $\Omega$  values, which are affected by  $\mu_{\text{eff}}$  of each device as known in Eq. 7.3. Therefore, to compare  $\Omega$  values is not relevant to investigate correlated mobility fluctuation characteristics. Since the  $\mu_{\text{eff}} \cdot \alpha_{\text{sc}}$  product is constant as mentioned above, we need to suggest a comparative number like corrected  $\alpha_{\text{sc}}$  ( $\alpha_{\text{sc}}'$ ):

$$\alpha_{sc}' = \frac{\Omega}{\mu_o C_{ox}} = \frac{\alpha_{sc} \mu_{eff}}{\mu_o} \quad (7.6)$$

where  $\mu_o$  is low-field mobility from Y-function method [24]. As shown in Fig 6, the extracted  $\alpha_{sc}'$  of NMOS is less than that of PMOS and  $\alpha_{sc}'$  values of NMOS and PMOS are close to  $\sim 10^4$  Vs/C and  $\sim 10^5$  Vs/C, respectively. These results are comparable with typical values with electron and hole in MOSFETs [25]. In addition,  $\alpha_{sc}'$  is insensitive with decrease of channel length in common with  $N_t$ .

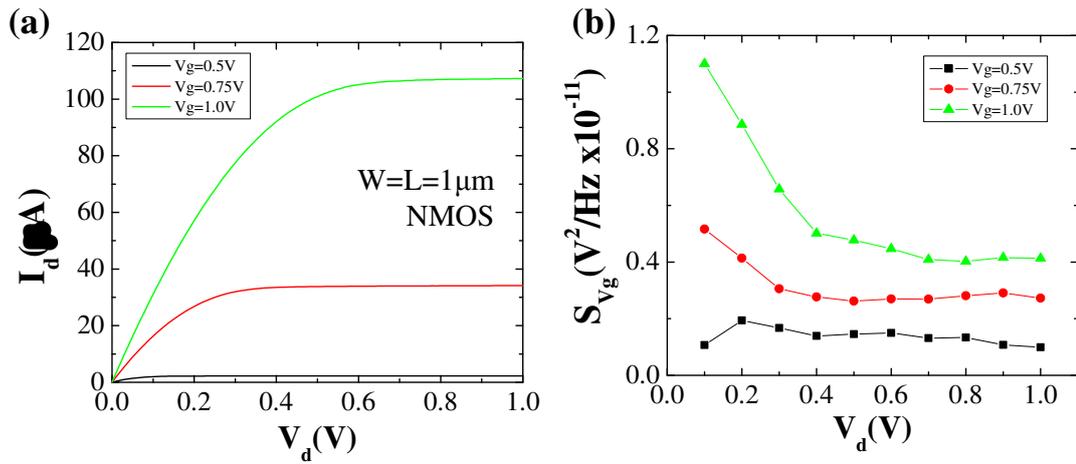
### 7.3.2 Noise characterization from the linear to saturation regime

In this section, we measured LF noise from linear to saturation operational regime, from 100mV to 1V with 100mV step. Fig. 7.7(a) shows typical I–V characteristics of NMOS long channel device in these regimes and the measured LF noise data also reveals 1/f dependency. From the input gate voltage PSD at 10Hz with  $V_d$  variation in Fig. 7.7(b), we can recognize that the LF noise behavior follows CNF with CMF model since it was confirmed that  $S_{Vg}$  decreases with  $V_d$  before saturation when CMF prevails in strong inversion [5,26]. However,  $S_{Vg}$  from strong inversion regime is higher in small  $V_d$  and steeply reduces before saturation with accounting correlated mobility fluctuation, which has good agreement with Fig. 7.7(b).

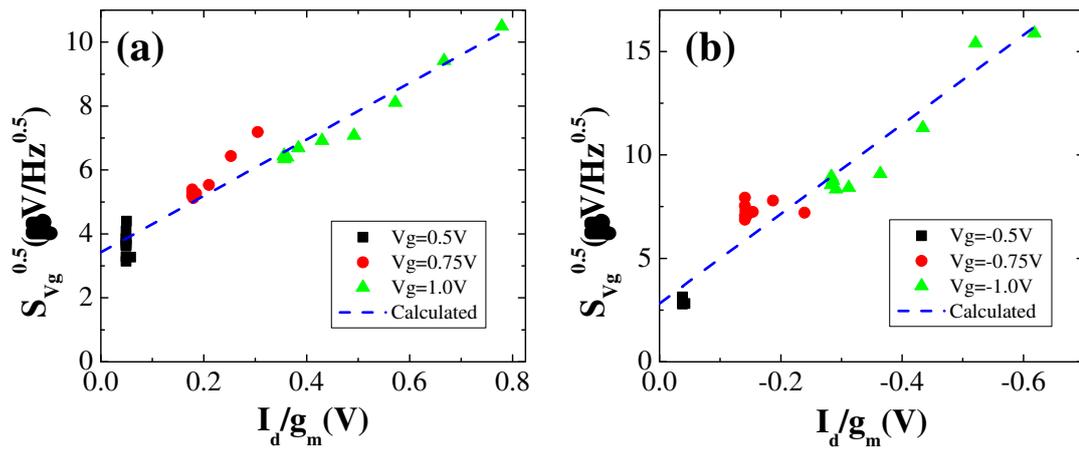
Recently, Boutchacha and Ghibaudo developed CMF with CNF model in non-linear regime [5]:

$$\frac{S_{I_d}}{I_d^2} = S_{V_{fb}} \frac{\int_0^{V_d} \left( \frac{1}{\sigma} \frac{\partial \sigma}{\partial V_{fb}} + \Omega \right)^2 \mu_{eff} Q_i dU_c}{\int_0^{V_d} \mu_{eff} Q_i dU_c} \quad (7.7)$$

where  $Q_i$  is the inversion charge,  $\sigma$  is channel conductivity and  $U_c$  is the quasi-Fermi level shift along the channel. Base on Eq.7.7, Ioannidis et al. proved that Eq.7.1 can be applicable in non-linear regime. As shown in Fig. 7.8,  $S_{Vg}^{0.5}$  with different drain voltage for long channel NMOS and PMOS (20%) devices has linear relationship with  $I_d/g_m$  and we can find the clear linearity with  $V_g=1V$ . Moreover, the used model shows good agreement with experimental data. From the fitting with Eq. 7.1, we also extracted  $N_t$  values of these devices, which are  $\sim 7 \times 10^{17} \text{cm}^{-3} \text{eV}^{-1}$  and  $\sim 4 \times 10^{17} \text{cm}^{-3} \text{eV}^{-1}$  for NMOS and PMOS, respectively. These values are comparable with the results from linear regime.



**Figure 7.7** (a) The output characteristics of NMOS devices ( $W=L=1\mu\text{m}$ ) with different gate voltages and (b) the input gate voltage power spectral density as a function of drain voltage.



**Figure 7.8** The measured  $S_{V_g}^{0.5}$  with different drain voltage for long channel (a) NMOS and (b) PMOS (20%) devices as a function of  $I_d/g_m$  (symbols) and linear fitting results based on Eq. 7.5 (lines)

## 7.4 Conclusions

In this chapter, we demonstrated that the LF noise behavior in the whole range of operation (from linear to saturation regime) of advanced FDSOI CMOS transistors from 14nm-node technology follows the CNF with CMF model, which is dominated from carrier trapping and de-trapping motion near the interfacial region between body and oxide layers. The extracted  $N_t$  reveals that the devices fabrication process, especially related with the interfacial

quality between channel and oxide layers, was well managed regardless type of devices, channel length and Ge content, as comparing previous technologies. Moreover, we confirmed that extracted  $\alpha_{sc}$ ' is insensitive with the geometric factor and comparable with typical value ( $\sim 10^4$  and  $10^5$  Vs/C for NMOS and PMOS, respectively)

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# Chapter 8

## Conclusions

In this thesis, we fully demonstrated the electrical and physical characterization of the 14nm-node FD-SOI CMOS transistors by using the various device parameter extraction methodologies such as C-V, I-V, magnetoresistance and low frequency noise and varying temperature. **Chapter 1** briefly dealt with recent trend of CMOS technologies. We introduced different device structures for suppressing short channel effects, including FD-SOI devices. In addition, the device architecture of 14nm FD-SOI CMOS transistors was elucidated.

**In Chapter 2**, the basic parameters and their extraction methods were discussed containing the low field mobility, effective mobility, split CV and series resistance. Details of the geometrical magnetoresistance (MR) effects were also indicated as well. In addition, the physical backgrounds of MR mobility were reminded. Moreover, the low frequency noise models with different description, such as carrier trapping and de-trapping motion and lattice vibrations or phonon scattering, were debated.

**In Chapter 3**, we successfully demonstrated extensive split C-V characterization of 14nm-node FD-SOI CMOS transistors with high-k and metal gate with interface coupling for ultra-thin BOX FDSOI devices. It enables parameter extraction from back plane to front gate in a reliable and fully consistent way. In addition, the  $C_{gb}$  analysis of FDSOI devices does provide complementary information on BP doping level ( $\sim 1 \times 10^{18}/\text{cm}^{-3}$ ) and flat band voltage of BP, which is not available in  $C_{gc}$  mode. By using the well calibrated 1D simulation and the improved coupling capacitance model, we also increased the reliability of the extracted parameters. This new parameter extraction methodology can be very useful to directly assess full stack

information in UTBB FDSOI structures without destructive analysis.

**In Chapters 4 and 5**, in-depth investigation under low temperature measurements (77K~300K) with interface coupling conditions were carried out for the electrical performances of highly scaled UTBB FD-SOI devices. From the comparative study between long channel devices with different high-k dielectric stacks, we found that additional mobility is governed by front-gate stack related scattering mechanisms, RCS or SOP playing the main role in different temperature ranges in NMOS devices. Back-bias induced mobility improvement could be both quantitatively and qualitatively analyzed by separating the back- and front-channel contributions. Mobility enhancement and  $V_T$  shift of the PMOS long channel devices were clearly demonstrated by using technological splits with varying Ge content. By analyzing gate length dependence, for NMOS, we found an additional contribution which does not depend of front-gate oxide stack and is consistent with neutral defects scattering. We believe that these neutral defects could be originated from source/drain regions. Furthermore, below some critical gate length, the mobility enhancement by back-biasing is not effective in both NMOS and PMOS. Thus, this feature confirms the prevailing role of channel defects in mobility degradation for ultra-scaled devices. Besides, in PMOS, the defect centers show surface-like behavior (more sensitive to carrier centroid modulation biased by  $V_b$ ). In addition, we proved that defects density could be denser close to front interface and with higher Ge% content.

**In Chapter 6**, we have presented an extensive study of advanced UTBB FD-SOI devices using magnetoresistance measurements with interface coupling condition. At first, we found that the gate stack process could impact on series resistance. Then, from the transport investigation, a nearly Coulomb scattering-free behavior in sub-threshold regime for long channel device at 300K was observed. This feature is reliable since MR is trustful even below threshold voltage. The additional scattering mechanisms associated with the high-k/metal gate stack were visible and consistent with results with the effective mobility analyzes. A bias-induced mobility improvement was demonstrated by tuning channel position. Finally, it was found that the mobility degradation factor in a given technology does not exhibits huge discrepancy regardless temperature and extraction method.

Furthermore, we have experimentally and theoretically demonstrated geometric MR extraction in the whole range of operation (from linear to saturation regime and also from sub-threshold regime to strong inversion regime) of advanced FDSOI device. In a proposed physical compact model with high field transport, it was capable of reproducing experimental  $\mu_{MR}$  in this whole range of operation regimes by using field-dependent mobility approach and magnetic field dependence. We found the reliability of our new methodology of carrier velocity extrac-

tion and a similar physical trend from the comparative study between our extracted saturation velocity and other methods in the literature. The high field transport properties were well interpreted by both saturation velocity and overshoot effects due to non-stationary transport in highly scaled devices. MR characterization technique and our theoretical methodologies demonstrated their advantages and potentialities for future ultimately scaled devices with specific supply voltage requirement.

**In chapter 7**, the LF noise properties of advanced FDSOI CMOS transistors were investigated in the whole range of operation (from linear to saturation regime). They show  $1/f$  dependency and were well reproduced with the CNF with CMF model, which is based on the trapping and de-trapping motion of carriers. The extracted  $N_t$  indicates that the devices fabrication process, especially related with the interfacial quality between body and oxide layers, was well controlled regardless type of devices, channel length and Ge content, as comparing previous technologies. In addition, we noticed that extracted  $\alpha_{sc}$  is insensitive with reduction of channel length and comparable with typical value ( $\sim 10^4$  and  $10^5$  C/Vs for NMOS and PMOS, respectively).



# List of Publications

**A. Journals**

*B. Conference proceedings*

*C. Conferences*

## A. Journals

1. **M. Shin**, M. Shi, M. Mouis, A. Cros, E. Josse, G.-T. Kim, and G. Ghibaudo, "In depth characterization of electron transport in 14nm FD-SOI CMOS devices," *Solid. State. Electron.*, vol. 112, pp. 13–18, Oct. 2015.
2. **M. Shin**, M. Shi, M. Mouis, A. Cros, E. Josse, G.-T. Kim, and G. Ghibaudo, "Full split C–V method for parameter extraction in ultra thin BOX FDSOI MOS devices," *Solid. State. Electron.*, vol. 99, pp. 104–107, Sep. 2014.
3. **M. Shin**, M. Shi, M. Mouis, A. Cros, E. Josse, S. Mukhopadhyay, B. Piot, G. T. Kim, and G. Ghibaudo, "Magnetoresistance mobility characterization in advanced FD-SOI n-MOSFETs," *Solid. State. Electron.*, vol. 103, pp. 229–235, 2014.
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1. **M. Shin**, M. Shi, M. Mouis, A. Cros, E. Josse, G. T. Kim, and G. Ghibaudo, "Low temperature characterization of 14nm FDSOI CMOS devices," in 2014 11th International Workshop on Low Temperature Electronics (WOLTE), 2014, no. 1, pp. 29–32.
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### ***C. Conferences***

1. **M. Shin**, M. Shi, M. Mouis, A. Cros, E. Josse, G. T. Kim, and G. Ghibaudo, "Low temperature characterization of 14nm FDSOI CMOS devices," 2014 11th International Workshop on

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5. J. Kim, Y Choi, J Na, **M. Shin**, M-J Han, J Huh and G-T Kim, "Effects of Geometrical Shapes of Electrodes on the Electric Contact Resistance of IZO Nanowire Device", MRS Spring meeting, 2012
6. **M. Shin**, J Huh, H Du, J Kim, W Kim, S Seo and G-T Kim, "Degradation of MoS2 field-effect transistors in ambient condition", Nano-Korea symposium, 2012

# Résumé en français

Parmi les architectures candidates pour les générations sub-22nm figurent les transistors sur silicium sur isolant (SOI). A cette échelle, les composants doivent intégrer des films isolants enterrés (BOX) et des canaux de conduction (Body) ultra-minces. A ceci s'ajoute l'utilisation d'empilements de grille avancés (diélectriques à haute permittivité / métal de grille) et une ingénierie de la contrainte mécanique avec l'utilisation d'alliages SiGe pour le canal des transistors de type P. La mise au point d'une telle technologie demande qu'on soit capable d'extraire de façon non destructive et avec précision la qualité du transport électronique et des interfaces, ainsi que les valeurs des paramètres physiques (dimensions et dopages), qui sont obtenues effectivement en fin de fabrication. Des techniques d'extraction de paramètres ont été développées au cours du temps. L'objectif de cette thèse est de reconsidérer et de faire évoluer ces techniques pour les adapter aux épaisseurs extrêmement réduites des composants étudiés. Elle combine mesures approfondies et modélisation en support. Parmi les résultats originaux obtenus au cours de cette thèse, citons notamment l'adaptation de la méthode split CV complète qui permet désormais d'extraire les paramètres caractérisant l'ensemble de l'empilement SOI, depuis le substrat et son dopage jusqu'à la grille, ainsi qu'une analyse extrêmement détaillée du transport grâce à des mesures en régime de couplage grille arrière à température variable ou l'exploitation de la magnétorésistance de canal depuis le régime linéaire jusqu'en saturation. Le mémoire se termine par une analyse détaillée du bruit basse fréquence.

# English abstract

Silicon on insulator (SOI) transistors are among the best candidates for sub-22nm technology nodes. At this scale, the devices integrate extremely thin buried oxide layers (BOX) and body. They also integrate advanced high-k dielectric / metal gate stacks and strain engineering is used to improve transport properties with, for instance, the use of SiGe alloys in the channel of p-type MOS transistors. The optimization of such a technology requires precise and non-destructive experimental techniques able to provide information about the quality of electron transport and interface quality, as well as about the real values of physical parameters (dimen-

sions and doping level) at the end of the process. Techniques for parameter extraction from electrical characteristics have been developed over time. The aim of this thesis work is to reconsider these methods and to further develop them to account for the extremely small dimensions used for sub-22nm SOI generations. The work is based on extended characterization and modelling in support. Among the original results obtained during this thesis, special notice should be put on the adaptation of the complete split CV method which is now able to extract the characteristic parameters for the entire stack, from the substrate and its doping level to the gate stack, as well as an extremely detailed analysis of electron transport based on low temperature characterization in back-gate electrostatic coupling conditions or the exploitation of channel magnetoresistance from the linear regime of operation to saturation. Finally, a detailed analysis of low-frequency noise closes this study.