Development of predictive models for the electromagnetic robustness of electronic components

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Abstract

One important objective of the electromagnetic compatibility (EMC) studies is to make the products compliant with the EMC requirement of the customers or the standards. However, all the EMC compliance verifications are applied before the delivery of final products. So we might have some new questions about the EMC performance during their lifetime. Will the product still be EMC compliant in several years? Can a product keep the same EMC performance during its whole lifetime? If not, how long the EMC compliance can be maintained?

The study of the long-term EMC level, which is called "electromagnetic robustness", appeared in the recent years. Past works showed that the degradation caused by aging could induce failures of electronic system, including a harmful evolution of electromagnetic compatibility. In this study, the long-term evolution of the EMC levels of two electronic component groups has been studied. The first electronic component type is the integrated circuit. The high-frequency currents and voltages during the switching activities of ICs are responsible for unintentional emissions or coupling. Besides, ICs are also very often the victim of electromagnetic interference. Another group of components is the passive component. In an electronic system, the IC components usually work together with the passive components at PCB level. The functions of passive components in an electronic system, such as filtering and decoupling, also have an important influence on the EMC levels.

In order to analyze the long-term evolution of the EMC level of the electronic components, the study in this thesis tends to propose general predictive methods for the electromagnetic compatibility levels of electronic components which evolve with time.

Key words:

- Electromagnetic robustness, Electromagnetic compatibility, Aging, Degradation mechanisms, EMC modeling, Degradation modeling, Integrated circuits, Passive components, Electromagnetic Reliability

Résumé

Un objectif important des études de la compatibilité électromagnétique (CEM) est de rendre les produits conformes aux exigences CEM des clients ou les normes. Cependant, toutes les vérifications de la conformité CEM sont appliquées avant la livraison des produits finis. Donc nous pourrions avoir de nouvelles questions sur les performances CEM des systèmes électroniques au cours de leur vie. Les comportements CEM de ces produits seront-ils toujours conformes dans plusieurs années ? Un produit peut-il garder les mêmes performances CEM pendant toute sa durée de vie ? Si non, combien de temps la conformité CEM peut-elle être maintenue ?

L'étude à long terme de l'évolution des niveaux CEM, appelée "robustesse électromagnétique», est apparue ces dernières années. Les travaux précédents ont montré que la dégradation causée par le vieillissement pourrait induire des défaillances de système électronique, y compris une évolution de la compatibilité électromagnétique. Dans cette étude, l'évolution à long terme des niveaux CEM de deux groupes de composants électroniques a été étudiée. Le premier type de composant électronique est le circuit intégré. Les courants de hautes fréquences et les tensions induites au cours des activités de commutation de circuits intégrés sont responsables des émissions électromagnétiques non intentionnelles. En outre, les circuits intégrés sont aussi très souvent les victimes d'interférences électromagnétiques. Un autre groupe de composants est formé par les composants passifs. Dans un système électronique, les circuits intégrés fonctionnent souvent avec les composants passifs sur un même circuit imprimé. Les fonctions des composants passifs dans un système électronique, telles que le filtrage et le découplage, ont également une influence importante sur les niveaux de CEM.

Afin d'analyser l'évolution à long terme des niveaux CEM des composants électroniques, les travaux présentés dans cette thèse ont pour objectif de proposer des méthodes générales pour prédire l'évolution dans les temps des niveaux de compatibilité électromagnétique des composants électroniques.

Mots clés:

- Robustesse électromagnétique, Compatibilité électromagnétique, Vieillissement, Mécanismes de dégradation, Modélisation CEM, Modélisation de la dégradation, Circuits intégrés, Composants passifs, Fiabilité électromagnétique

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Chapter I. General introduction

I.1. Thesis context

The problem studied in this thesis is about the prediction of long-term EMC (Electromagnetic compatibility) evolution at IC (integrated circuit) and Printed circuit board (PCB) level which is related with the degradation of ICs and passive components.

Due to their numerous advantages (such as low cost, limited size and weight, low power requirement, high performance…), integrated circuits are widely employed in electronic systems. With the continuous development of IC technology from the invention of ICs in 1958, their performances like operating speed have been greatly improved, and it also plays a more and more important role in the electromagnetic compatibility studies. The ICs are one major source of signals and noise that produce interference. The high-frequency currents and voltages during their switching activities are responsible for unintentional emissions or coupling. Besides, ICs are also very often the victim of electromagnetic interference. In an electronic system, the IC components always work together with the passive components. The functions of passive components in an electronic system, like filtering and decoupling, also have an important influence on the EMC levels. For this reason, EMC design guidelines for ICs and electronic systems are required, in order to get improved EMC performances. The proposed EMC design guidelines contain the hardware methods (such as additional on-chip capacitance) and the software methods (such as I/O management). Another important trend is the application of simulation during the design phase to predict the EMC levels before the fabrication of the final products. All these works aim at making electronic products compliant with the EMC requirement of the customers or the standards [BEND06] [REDO10] [VRIG05].

However, all the EMC compliance verifications are applied before the delivery of final products, so we might have some new questions about the EMC performance during their lifetime. Will the product still be EMC compliant in several years? Can a product keep the same EMC performance during its whole lifetime? If not, how long the EMC compliance can be maintained?

So the study comes to another research activity of reliability. The aging phenomenon is very normal for the electronic devices. The degradation of electronic components can be caused by aging during the operating of system, and some conditions can accelerate the aging process, such as high

temperature, vibration, voltage surge and current spike. I guess that is why the warranty period of electronic devices provided by the manufacturer is usually limited. Like a mobile phone, the warranty period is normally only 2 years.

Sometimes, the failure mechanisms do not compromise the operation of the system, but it can have a significant impact on EMC performances. Some experimental results have shown significant reduction of susceptibility levels after aging stress. Thus how to ensure EMC during the whole lifetime of IC products? This new topic called electromagnetic robustness (EMR) becomes a new challenge in the recent years. The need to predict EMC of ICs after several years of operating life is driven by the trend towards extended warranty [BEND13].

For example, the electronic devices including a large amount of ICs are integrated in an aircraft, such as the electronic flight instrument system in the cabin of an Airbus A380 shown in Figure I-1. Besides, the extreme operating temperature of the aircraft at high altitude (from -55 °C to 125 °C [LI11]) could accelerate the aging process of the electronic devices. A commercial airplane's service lift could be very long, which might be longer than 30 years. As a result, the high level of the operating safety and reliability is required. Thus, it is very important to ensure that the electronic systems are always EMC compliant during the whole lifetime. The current method used in the aeronautic equipment is a large EMC margin of safety during the design phase to ensure that the EMC levels remain acceptable for years. However, the long-term EMC analysis presented in this study could also be useful to predict and verify the reliability of EMC compliance with time.

Figure I-1 A view inside the double-deck A380's cockpit [AIRBUS]

I.2. Scope of this dissertation

The objective of our work is to propose a systematical modelling and predicting method of the EMC evolutions of integrated circuit and passive components in a long-term. We begin by a global introduction of long-term EMC. As EMR is a mixed research of "Reliability" and "EMC", so the characterization and modeling methods of these two topics are presented respectively in the following chapters. Then two case studies about the long-term EMC levels' prediction are presented. The devices under test of these two case studies are respectively an integrated circuit and the passive components. Finally, the statistical analysis used in EMR and the modeling are discussed in the last chapter.

The dissertation is organized as followed:

Chapter II details the state of the art for our research context. It begins with a global presentation of EMC domain and its historical evolution. Then the presentation of EMC of integrated circuits includes the mechanisms, the influences of technology evolution, measurement standards and modeling methods. Finally the EM robustness issues and the objectives in this study are presented.

Chapter III investigates the degradation of the components which could be the source of the EMC evolution. After an introduction of the reliability of electronic devices and the aging stress, the degradation mechanisms and modeling for two sorts of electronic components (active MOSFET in integrated circuits and passive devices) are presented and analyzed.

Chapter IV deals with the prediction of EMC evolution with aging time. The general characterization flow and modeling methods are discussed. Two cases study present respectively the prediction process for electromagnetic emission (EME) and electromagnetic immunity (EMI) evolution. Besides, the alternative modeling methods (macro models, black-box models) are presented and discussed. Also the validity of the model is defined.

Chapter V is devoted to the statistical analysis for the EMR study. It firstly presents the statistical elements in EMR studies. Then the statistical methods in device degradation and in the EMC drift modeling are discussed.

Finally, the general conclusion summarizes the contribution of this dissertation and offers perspectives in regard to the future work.

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Chapter II. Long term electromagnetic compatibility

II.1. Introduction

Electromagnetic compatibility is an important performance for electronic devices. According to the standards of International Electrotechnical Commission (IEC), electromagnetic compatibility is defined as "The ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbance to anything in that environment" [IEC 60050-161]. A qualified electronic device is also EMC compliant according to the standard or the requirement of client. However, with the operating time, especially under the harsh operating condition, the degradation of electronic components induced by aging could produce the great variation of EMC level. As a result, the issues about the long term EMC of electronic devices appeared in the recent years, to analyze the EMC evolution during the lifetime of electronic products.

The state of the art for our research context is presented in this chapter. The presentation begins from the global EMC domain, with the presented topics more and more orientated to Electromagnetic Robustness (EMR) of electronic system. An explicit location of the work in this thesis will be defined.

II.2. Electromagnetic compatibility issues

II.2.1. A small discussion about EMC

In spite of the existence of this phenomenon everywhere, electromagnetic compatibility (EMC) is not a usual term for our ordinary life. Every time I describe my PhD subject, the most frequent responses are: "What's that?", "Something like electromagnetic radiation, of electromagnetic wave?". I can understand their reaction, because we can always hear the discussion about the harm of electromagnetic radiation to the human being health. My answer is always yes, EMC is a related research domain, but our study focuses more on the problems of compatibility between electric/electronic devices caused by electromagnetic phenomena.

Not many people could really understand this explanation, sometimes they are more confused. In the beginning, for me it's really not easy to explain the EMC in detail, because some basic scientific knowledge about the electromagnetic phenomenon is needed to understand the problem, and it seems far away from our life, something like the 'black magic' as mentioned in [CHAR00]. Until one day, a colleague told me an example that he used to explain EMC: the forbidden use of the electronic devices on aircraft, as the notification that we can usually find in the airline safety card (Figure II-1).

Figure II-1 **Notification about the use of electronic devices in United Airlines Boeing 747-400 Passenger Safety Instruction Card [AERO04]**

This example illustrates very well the possible influence of electromagnetic emission (EME) from electronic devices (cell phone for example) to its environment or another system (airplane). It helps me a lot to make clear to people, for example my parents, in which domain I work exactly. But a new question arrives: is it really dangerous to use the mobile phone in the plane? Sometimes they found that people do not respect this regulation, but the plane has never crashed.

Honestly, I have to say I have not many ideas about this question. Actually, about this subject, there is always the debate and I don't think we can have a conclusion in the coming years. Electromagnetic interference is always considered as one main argument for banning electronic devices on planes. Theoretically, every electronic device such as mobile phone, portable computer or gaming device could be a possible interference source for airplane system, though the power level of the radiated EME of these electronic devices is relatively low. Besides, the aircraft system has improved a lot their immunity level to electromagnetic interference. In September 2014, the European Aviation Safety Agency removed its ban on mobile phone use during flights, because they considered that electronic devices do not pose a safety risk.

Nevertheless, EMC is not the only problem for the use of electronic devices in aircraft. The other factors, like telecommunication system for mobile phones or some other business reasons, are also the support arguments to prohibit the use of personal electronic devices on board. This problem is similar to nuclear power station. Even though the risk level is very limited, there is always the theoretical possibility that the electromagnetic radiations emitted by electronic devices affect the aircraft electronics, and no one could guarantee a 100 % safety. I have no idea about what is the exact regulation for each airplane company at this time, but the use of electronic devices on board is always limited, especially during take-off and landing.

Except the compatibility problem between the aircraft and personal electronic devices, many other examples could be found in an interesting "Banana skins", which is a regular feature in the EMC Compliance Journal [ARMS07] and briefly describes many EMC incompatibility cases in real world. Here is a droll example extracted from this website which took place in south west England: "Villagers in Dorset were baffled when their pop-up toasters began to speak Russian. Phones and other electrical appliances in Hooke also chatter away in foreign languages and play music. The phenomenon has been blamed on a powerful radio transmitter in nearby Rampisham that transmits BBC World Service. John Dalton, chairman of the parish council, says: "I've heard foreign voices through an electric organ. And I was amazed when I got the World Service signature tune through a toaster". (From "Weirdness of the week" in the Sunday Times' 'News Review', 12th May 2002, page 4.12)" However, not all the electromagnetic interferences produce such amusing results. More other incidents are harmful, which might result in loss of money or transport accident. The most serious cases are even life-threatening, especially for some critical medical devices like artificial cardiac pacemaker, which is also much reported in "Banana skins".

So we can find that EMC is a not subject far away from our life. Maybe not everyone could have the experience to feel the influence caused by the electromagnetic incompatibility, but it doesn't mean that the problem doesn't exist. Fortunately, a lot of EMC problems could find the solution, and that is the significance and objective of the work in the EMC domain.

II.2.2. What is EMC?

This definition of EMC in [IEC 60050-161] presented in II.1 contains two requirements: Electromagnetic Emission (EME) and Electromagnetic Susceptibility (EMS), as shown in Figure II-2.

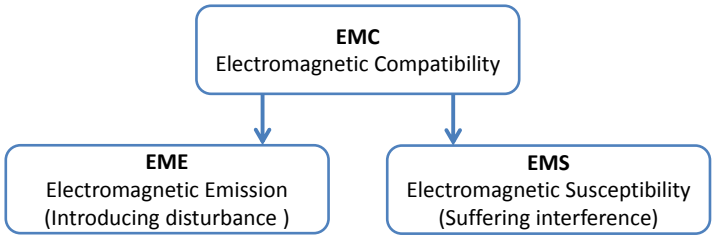

Figure II-2 Two parts of EMC definition [REDO10]

EME is sometimes as the byproduct of an electronic device's operation, which could be presented by the energy transmitted through an electromagnetic field (Radiated emission), or through a propagating wave (Conducted emission). These undesirable generated emissions could be a noise or interference for the normal performance of other devices. On the other hand, the devices should be able to work as expected in their electromagnetic environment, which means it should be able to suffer the electromagnetic interference up to a certain level. Electromagnetic susceptibility level could be measured by the minimum interference level under what the system could no more maintain the

predefined performance level. Often, we also use electromagnetic immunity (EMI) to express the susceptibility performance, since immunity signifies the opposite of susceptibility [REDO10] [MONT98].

As presented below, the electromagnetic emission generated by electronic devices might be a possible electromagnetic interference source. In fact, most electromagnetic pollution is man-made. The applications, like microwave ovens, electric motors or communication systems, contribute to a polluted radio spectrum in a very board frequency range. Another electromagnetic interference is from the nature. Lightning is the most common phenomenon of atmospheric noise. Another kind of electromagnetic pollution is the cosmic noise primarily in space, such as cosmic microwave background radiation, solar radio noise and galactic noise [REDO10].

Besides, in the definition of EMC, the electronic equipment should "function satisfactorily". However, the sense of satisfaction is very subjective. As a result, the threshold of satisfactory performance, or the limit of system failure in contrary, should be well defined in the EMS study. The following performance classes in Table II-1, proposed by the standard IEC 62132-1 [IEC 62132-1], could be a reference used to characterize the performance specified in immunity analysis.

Table II-1 Performance classes of an electronic system [IEC 62132-1]

Class	Description
A	Normal performance within the specification limits
B	Temporary degradation or loss of function or performance which is self-recoverable
C	Temporary degradation or loss of function or performance, which requires operator intervention or system reset
D	Degradation or loss of function which is not self-recoverable due to damage of system or loss of data

II.2.3. History scope

The phenomena of electricity and magnetism exist before the human race. And since ancient times, people have discovered these phenomena existed in the nature and learned to make use of them. Like the use of loadstone as a magnetic compass adopted for navigation from the Chinese Song Dynasty (960 – 1279). In the manuscript "Wu Ching Tsung Yao", written in 1040, "an iron fish" suspended in water could point to the south [VARD13]. In 1600, William Gilbert published his primary scientific work "De Magnete, Magneticisque Corporibus, et de Magno Magnete Tellure" (On the Magnet and Magnetic Bodies, and on the Great Magnet the Earth), which is the beginning of the modern research of electricity and magnetism.

However, the unity of electric and magnetic phenomena was revealed by Hans Christian Ørsted until 1820, where he noticed a compass needle deflected from magnetic north when an electric current from a battery was switched on and off. With the work of Hans Christian Ørsted and André-Marie Ampère, electromagnetism began to be recognized as an entirety of electricity and magnetism. Electricity and magnetism (and light, which is proved as a visible electromagnetic radiation) were definitively linked by James Clerk Maxwell and the famous Maxwell's equations presented in his great publication "A Dynamical Theory of the Electromagnetic Field" in 1864. Nowadays, the modern form of Maxwell's equations contains 4 equations. In fact there were 20 equations in the original paper of Maxwell, because of the lack of vector calculus at this moment. These important scientific discoveries provided the theoretical bases for the following applications of wireless and wireline communication.

One of the most following important invention is the radio appeared at the end of 19th century. In 1892, an edict issued by the German parliament recorded the event that electromagnetic disturbances perturb the correct operation of telegraph cables or telegraph equipment. During the First World War, the US military found out compatibility problems when trying to equip a car with a radio, because the motor noise could be an interference to other sensitive systems. With the wide use of more and more radio services, it became necessary to define the different parts of radio spectrum for different radio transmission technologies and applications, which is nowadays the work done by International Telecommunications Union (ITU). With the appearance of radar and the more prevalent use of on-board radio communication in cars, aircraft and ships, the awareness of EMC kept growing throughout the Second World War. However, it was the first time the electromagnetic interferences like radio or radar of highly focused power were used as intentional electromagnetic weapons at the same moment, which are called Directed Energy Weapons (DEW) in modern wars [REDO10].

With the popularization of personal electronic devices after wars, EMC issues were no more a concern for the military but also for civilian, especially from the development of telecommunication and the come of information age in the 1970s. Many more countries were aware of EMC which became a growing problem. So they created the necessary EMC requirements or standards of the electronic products for the manufacturers. In order to limit the EMC problems and promote international co-operation on standardization of product, several important EMC directives have been proposed by several international and national standard organizations, such as FCC (Federal Communications Commission) in the United States, and CISPR (International Special Committee on Radio Interference) of the IEC (International Electrotechnical Commission) in Europe [REDO10] [WILL07]. However, the standards vary a lot according to the applications. As shown in Figure II-3, the limits of radiated emission level at a 1 meter measurement distance are defined by different applications. FCC Class A is for digital devices that are marketed in US exclusively for use in business, industrial and commercial environments, MIL-STD-461 is the military standard and GM9100 is the own limit definition of General Motors vehicle. The difference of several frequency parts between the

FCC CLASS A and GM9100 NARROWBAND is larger than 50 dB, which means the radiation strength difference is about 300 times.

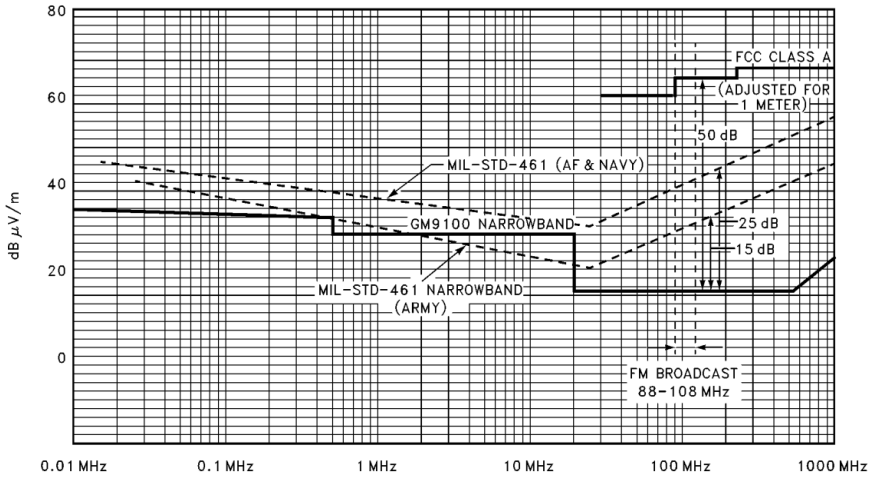

Figure II-3 **Comparison of radiated emission specifications of commercial application (FCC), Military (MIL-STD-461) and Automotive (GM9100) [BAYN96]**

Besides, for the products sold in the international market, especially for the European or US market, we can find the CE or FCC marks on the products, as demonstrated in Figure II-4. Using these marks declare the conformity of the products with the required directives including the needed EMC directives. However, the mark is not a quality mark or an approval mark. But as the declarations of conformity, they present the responsibility of the manufacturer or his authorized representative for their products [WILL07].

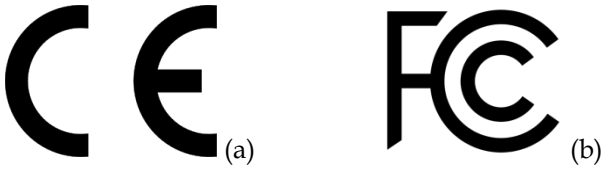

Figure II-4 **CE mark (a) for European Economic Area and FCC Declaration of Conformity label (b) for US**

Nowadays, EMC becomes a large multidisciplinary research domain to help electronic device and equipment manufacturers to satisfy EMC requirements. It includes and is not limited to:

- EMC standard and management
- EMC measurement and instrumentation
- Electromagnetic environment
- EMC interference
- Power system EMC and smart grid
- System level EMC and protection
- Low frequency EMC
- Antenna and wave propagation
- Electronic packaging EMC

- Printed circuit board EMC
- Integrated circuit EMC
- Signal integrity and power integrity
- Wireless communication EMC
- Computational electromagnetics
- EMC in nanotechnology and advanced materials
- Aerospace and automotive EMC
- Biomedical electromagnetics
- Electromagnetic fields and human health

In this study, what we will talk about is under the category of the EMC of integrated circuits (IC) at circuit level and the passive components at PCB level.

II.3. EMC of integrated circuits

Considering the power level and the length of power cable, the EMC problems caused by external cables or connectors are considered more important than that of components. That's why EMC has been taken into account at system, cable and printed-circuit board (PCB) levels for a long time [CHAR00]. As shown in Figure II-5, the troubleshooting of EMC at system level focuses on the noise filtering through various well-known solutions [SICA11].

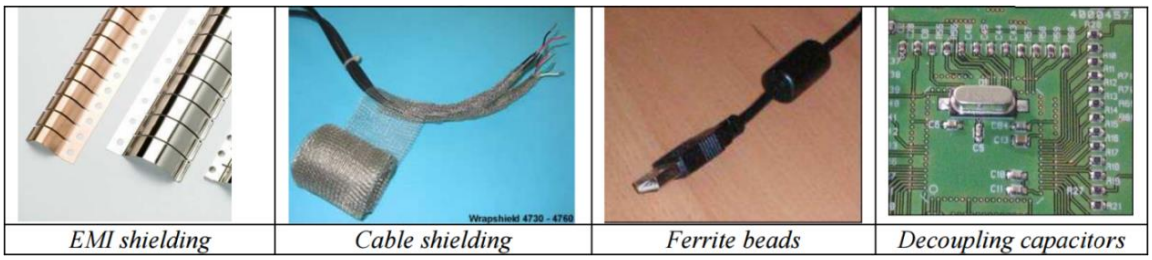

Figure II-5 Different techniques used at system, cable and PCB level to overcome EMC problems [SICA11]

With the significant evolution in integrated circuit (IC) technology, the performance of electronic devices has been much improved these last decades. At the same time, the integrated circuits become more and more important source of EMC problems for electronic systems, and considering only EMC at system level is no more sufficient. As shown in Figure II-6, semiconductor devices are usually the source of EMC interference and also simultaneously the victim of extra EM noise. The objective of the EMC study at circuit level is to reduce the noise origins and to improve the ability of IC suffering the EM interference, also to decrease EMC compliance costs by removing additional EMC protections.

Since the interference could be coupled through cables and PCB tracks, the EMC problem in circuit level should consider not only IC components but also the PCB and other devices in the same PCB board (like filtering/decoupling passive devices). Although this part presents the EMC at circuit

level, some mechanisms, measurement and modeling methods could be also applied to explain the EMC issue in a simple electronic PCB system which contains both IC components and passive components. As a result, the EMC related with passive components are not presented separately.

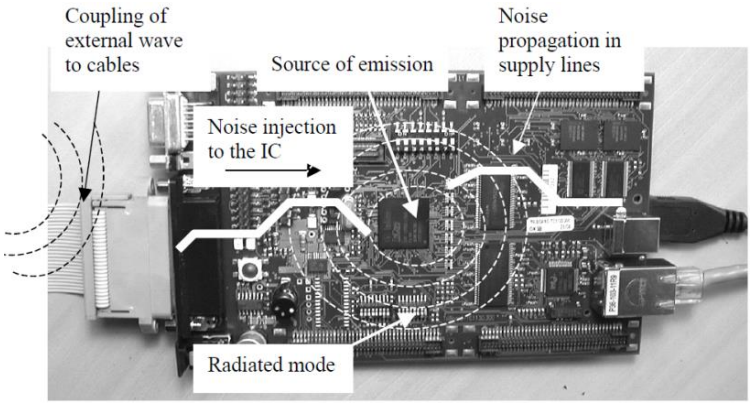

Figure II-6 Conducted, radiated emission and susceptibility of an integrated circuit at PCB level [SICA11]

II.3.1. Brief historical review

It's well known that Jack Kilby demonstrated the first working integrated example on 12 September 1958, but not many people know that the first EMC study on integrated circuits stated in 1965 at the Special Weapons Center at Kirtland Air Force Base, New Mexico. The study dealt with the effects of the electromagnetic fields trigged by nuclear explosions on electronic devices used in missile launch site. In order to simulate the effects of nuclear radiation on electronic components, a simulation software called SPECTRE was developed by IBM [SEDO67].

With the massive home computer proliferation starting from the 1970s, interference problems from computing devices became a significant problem to radio and television broadcasting. In the other side, the protection techniques were developed to withstand the increasing coupling from radio and television signals [REDO10] [BEND06]. In 1979, a special issue on "RF interference effects in semiconductor discrete devices and integrated circuits" of the IEEE Transitions on Electromagnetic Compatibility was devoted to electromagnetic interference problems on semiconductor devices and the prediction of these behaviors by means of dedicated simulation tools [WHAL79].

Because of the rising use of electronic devices and the integration of various systems in the same product, EMC problems persisted throughout the 1980s and became more stringent in the 1990s. A typical example is our mobile phones, a teardown demonstration of the latest IPhone (IPhone 6 Plus preleased in September 2014) is shown in Figure II-7, where microprocessor, camera, antennas for Bluetooth, LTE and Wi-Fi and other blocks coexist and work simultaneously in a very limited closed space. How to avoid the coupling of each block and protect from the external interference requires a better product EMC design.

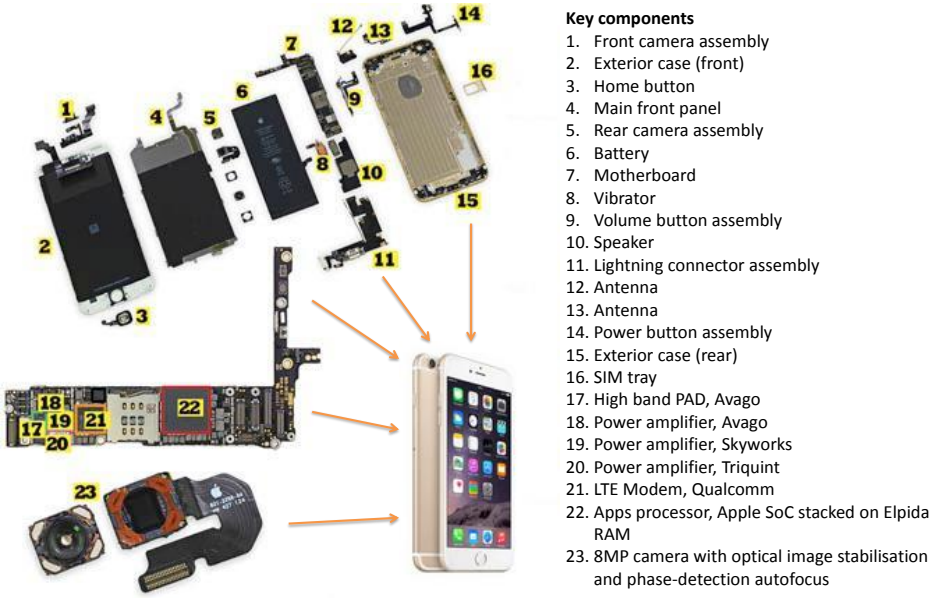

Figure II-7 Teardown analysis of an IPhone 6 Plus [DEMP14]

II.3.2. Mechanisms of EMC at circuit level

II.3.2.1. Interference coupling modes of integrated circuits

According to the coupling trajectory, there are three electromagnetic interference coupling modes from interference source to victim: Radiative coupling over distance, Near field coupling and Conductive coupling.

- Radiative coupling

Radiative coupling is the transfer of electromagnetic energy over distance which is greater than a few source wavelengths. The metallic part of victim device can be seen as an antenna of RF signals. The electromagnetic interference to radio frequency interference covers a great range from tens of Hz to hundred GHz. According to the theory of antenna, one quarter of wavelength ($\lambda/4$) corresponds to the length of an efficient antenna. As a result, the victim by radiative coupling could be many objects of various scales, as shown in Figure II-8. With the increase of frequency, the size of potential impacted device is smaller. From 300 MHz, the PCB tracks and the package leads begin to act as antennas to receive a large amount of noise. However, integrated circuit package or lead frames are too small at frequencies below 10GHz. So the radiative interference is not the main coupling mode for integrated circuits.

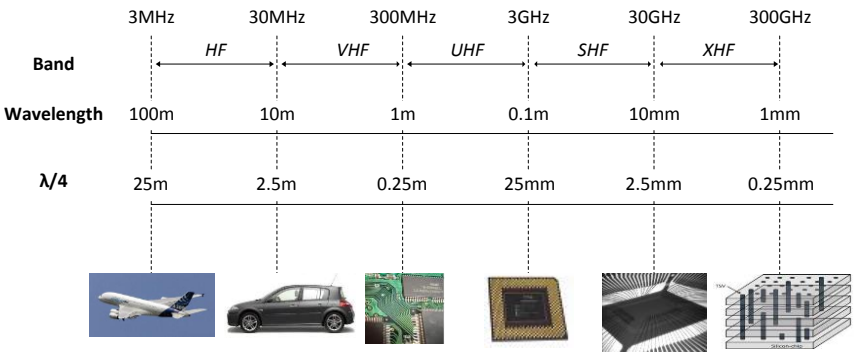

Figure II-8 **Frequency bands of RF disturbance and the corresponding wavelength**

- Near field coupling

As explained in Figure II-9, there are two major near field coupling modes: capacitive coupling by electric field and inductive coupling by magnetic field. The electric field coupling occurs between two parallel conductors of two circuits, which could be represented schematically by a parasitic capacitance. This coupling could create an unexpected current in the victim circuit. Besides, due to the inductive elements of the conductors, two parallel conductors could be considered as the primary and secondary of a transformer in magnetic field coupling, where a voltage could be generated in the victim circuit [BEND06]. This coupling is very important for integrated circuits. The mechanisms of the magnetic and electric near field coupling in a package of an IC are shown in Figure II-10. The fine wires which connect the integrated circuit die to the legs of the packaging could be the main source of near field coupling.

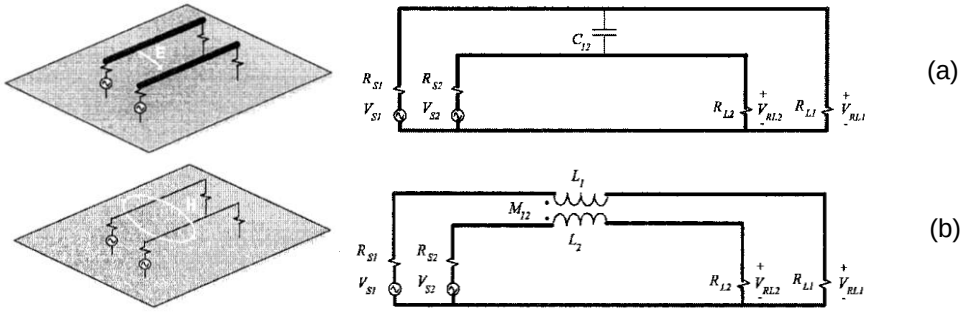

Figure II-9 **Electric field coupling (a) and Magnetic field coupling (b) between two signal rails [BEND06]**

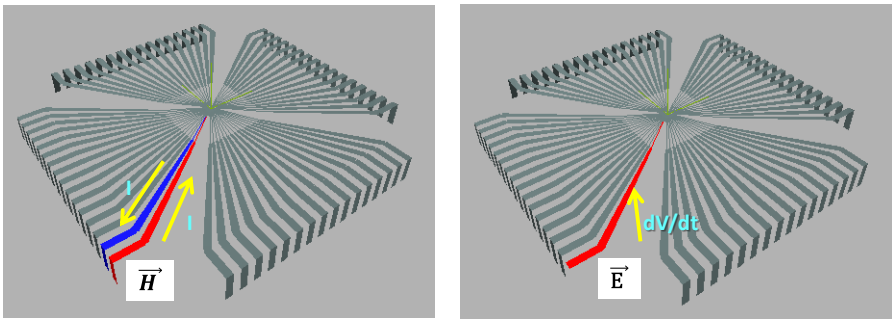

Figure II-10 **Mechanisms of the magnetic (right) and electric (left) near field coupling [BOYE05]**

- Conductive coupling

Conductive coupling is also called common-impedance coupling. This coupling is usually caused by the shared current paths of two circuits. The most general situation is the common ground metallization, as illustrated in Figure II-11. The finite impedance of the shared conductor brings out a voltage drop that appears across both circuits. The problem of the substrate coupling is a good example for the conductive coupling of ICs.

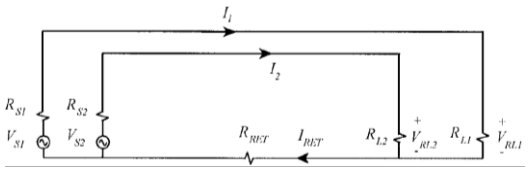

Figure II-11 Two circuits sharing a common current return path [BEND06]

The near field coupling and the conductive coupling are two major mechanisms of a typical EMC problem called "crosstalk", where the voltage or current in one circuit is unintentionally coupled to a second victim circuit. Generally, crosstalk problems in ICs could be reduced or avoided by several basic routing design guidelines, like reducing impedance of common path or isolating circuits with grounded conductor [BEND06].

II.3.2.2. Mechanisms of electromagnetic emission

Electromagnetic emission of ICs is mainly produced by the internal switching activities, which induce the transient current circulation within the circuit and its direct environment (PCB, cables). This phenomenon is also known as Simultaneous Switching Noise (SSN) [LI11], which is mainly related to the switching activities in circuits, such as digital circuits, output buffers, switching power supplies, and bus drivers.

An example of a CMOS inverter is shown in Figure II-12. The short current peaks correspond to charge and discharge of the output capacitor during the switching activity of the transistors. The peak current value depends on the saturation current of each transistor (PMOS for I_{DD} and NMOS for I_{SS}) and the terminal load (Output capacitor).

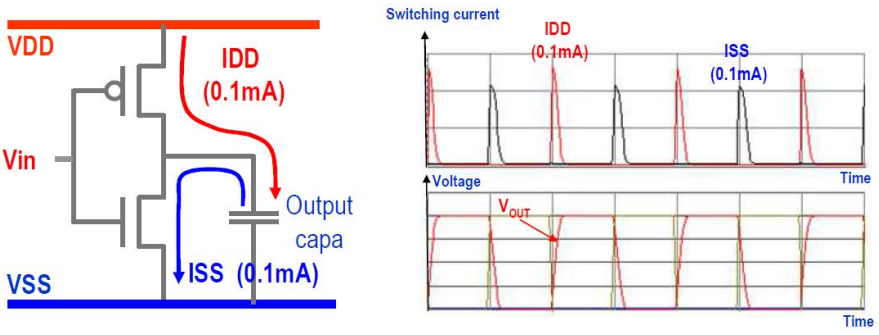

Figure II-12 Basic mechanisms of CMOS circuit current – inverter example [SICA11]

However, the transistor current itself does not directly generate conducted and radiated interference. Suppose ideal power supply and ground voltage reference, voltage should remain constant whatever the consumed current is. In practice, IC is powered by a non-ideal reference voltage (power supply and grand) through long interconnections such as package leads, PCB tracks and cables, and these interconnection mediums are not ideal conductors. As shown in Figure II-13, due to their parasitic resistance, inductance and capacitance, the interconnections cannot be considered as equipotential, and they might convert the transient current peaks into voltage drops.

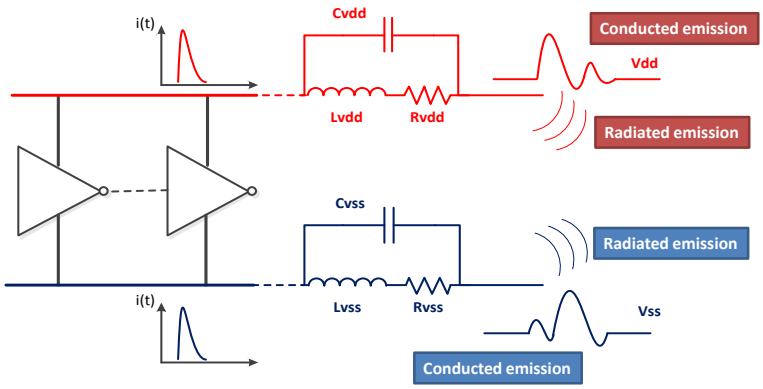

Figure II-13 IC parasitic emission due to switching activity and parasitic power supply interconnections [SICA11]

Parasitic inductive elements of interconnections are the main cause of voltage drops [SENT91]. The conversion of transient current to voltage bounces is given by Equation II-1.

$$\Delta V_{noise} = L\frac{di}{dt} \qquad \text{Equation II-1}$$

Where

ΔV_{noise} is the voltage fluctuations between power and ground conductors produced by transient current surges i, which is also called "Delta-I" noise.

L is the inductive elements of interconnections.

This voltage drop could spread to the other blocks of circuit which share the same power supply network without isolation, which is called conducted emission. In addition, current flows and voltage variation along the interconnections generate electromagnetic fields, in another word radiated electromagnetic emission [LI11].

II.3.2.3. Mechanisms of electromagnetic susceptibility

As demonstrated in Figure II-14, due to the various natural noises (like lightning, solar radio noise) and the increasing artificial electromagnetic noises (as mobile phones, communication

transmitters, Wi-Fi, radar, ESD, etc.), susceptibility ability of ICs to electromagnetic noise becomes a more and more important concern during the product design [RAMD09].

Figure II-14 Parasitic radio-frequency sources which may disturb integrated circuits

According to the definition of EMI in II.1, the failure of system is defined strongly according to the circuits and their applications. Here we present several failure examples of two main types of ICs: digital circuit and analog circuit, because their failures induced by electromagnetic influence are very different.

- Digital circuits' failures induced by interference

In digital circuit, the logic states "0" and "1" could be presented by the signal level, as an example of inverter gates explained in Figure II-15. There is already a noise margin for each state. If the deviation induced by noise is inside the acceptable region ($V_H \sim V_{DD}$ for "1" and $V_L \sim V_{ss}$ for "0"), the digital circuit could maintain its original operation. Contrarily, if the deviation exceeds the defined region, undesirable logic states might occur.

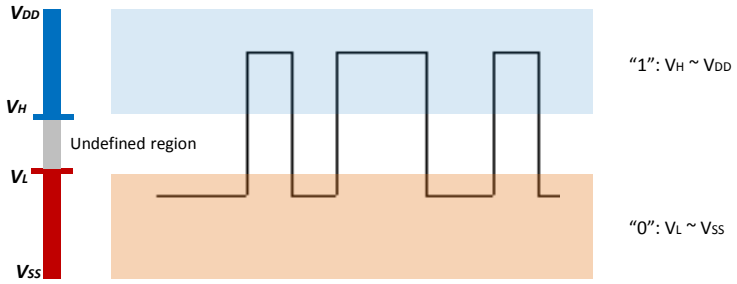

Figure II-15 Definition of logic state of digital circuits

Figure II-16 illustrates two failure modes of a digital inverter. The RF interferences are injected in the input side of the inverter. If the noise level is sufficient to go through to the region of another state, the errors like "Glitch" could be observed in the output (Figure II-16 (a)). Yet, even if the RF disturbance is not sufficient to change the logic state, they could also affect propagation delay of the

signal, as shown in Figure II-16 (b). This phenomenon is called "Jitter", it is very common in the digital circuits, and we can define a threshold of the jitter width as the judgment of failure.

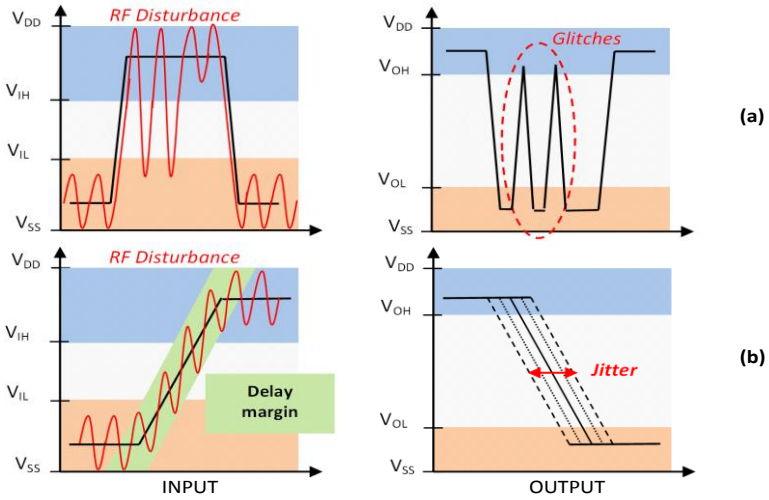

Figure II-16 Failures of an inverter induced by RF disturbance [LI11]

- Analog circuits' failures induced by interference

Unlike digital circuits which exhibit an intrinsic noise margin against small variations, analog circuits are usually very susceptible to electromagnetic disturbance. When EMI is injected in the input of analog circuits, the circuits treat the noise as a normal input signal. The distortion of the signal is a general result of EMI for the analog circuits.

We do not have the method of distinguishing unwanted in-band noises from the intended signal. In order to distinguish the noise from the desired signal, the differential signals are applied, because the interferences tend to manifest themselves as common-mode signals on neighboring PCB tracks or wires. This method could improve the EMI performance of the circuit. However, the common-mode rejection ratio (CMRR) of the circuit should be very high to reject the common-mode signals. Besides, theoretically we can use the filter to remove the out-band disturbances from in-band signal. But, because of the intrinsic nonlinear behaviors of analog circuits, inappropriate filtering may cause nonlinear distortion and generate unintended DC offset. The DC shift induced by RF disturbances coupled on the input or power supply of operational amplifiers is an issue widely discussed [FIRO02] [REDO10]. An example of the influence of RF disturbances injected in the power supply of a bandgap voltage reference is illustrated in Figure II-17. The DC offset produced in the output is harmful and hard to be removed.

According to the different functions of analog blocks, we can define the failure of each circuit by a drift limit of certain critical parameters, for example in [BOYE11] a failure is defined as the period jitter on the PLL output signal exceeds 2 ns or when the PLL is unlocked, and in [WU14] a +/− 0.1 V offset at the output of a voltage regulator is defined as the threshold of failure. In addition, the failures

of analog circuits are normally temporary: when the interferences are removed, the failures disappear [LI11].

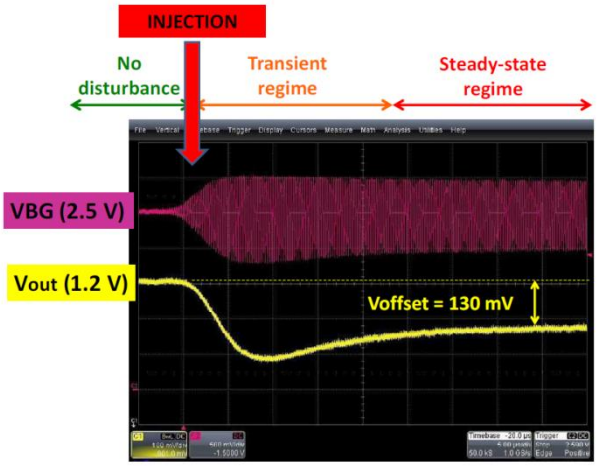

Figure II-17 DC offset induced by the EMI injected in the power supply of a bandgap voltage reference

II.3.3. Influence of IC technological evolution on EMC

In 1965, Gordon Earle Moore the co-founder of Inter Corporation published "Cramming more components onto integrated circuits". In this brief article, Moore proposed the famous Moore's law which predicted the long-term exponential growth of integrated circuits: "The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years."[MOOR65]. In the original version, the device complexity (available memory, calculation speed or transistor number) doubles every year. Then in 1975, Moore altered the doubling speed to approximate every two years. However, the common accepted speed of Moore's law is 18 months.

As shown in Figure II-18, Moore's law has held more than half a century. As Moore's law is not a physical or natural law, it might reach its saturation in the coming years. Although the speed of increase might slow down, the transistor density will continue to increase with the introduction of new technologies such as 3-D integration, which is widely used to increase memory density. To increase the circuits' performance, the studies begin to focus not only on reducing the size of transistors to increase performance but techniques, like the use of multi-core. We call this new trend "More-than-Moore".

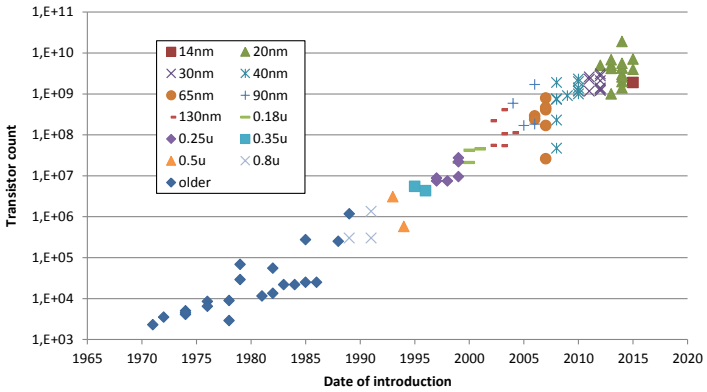

Figure II-18 Microprocessor transistor counts & Moore's law

The following Table II-2 demonstrates the evolution of several parameters of developing IC technology which have an impact on EMC levels of integrated circuits.

Table II-2 Evolution of current peak of the IC

Year	Technology	External Supply (V)	Internal supply (V)	Density of gate (k/mm²)	Current peak per gate (mA)
1990	1.2µm	5	5	15	0,9
1993	0.8µm	5	5	28	0,75
1995	0.5µm	5	3,3	50	0,6
1997	0.35µm	5	2,5	90	0,4
1999	0.25µm	3,3	1,8	160	0,3
2001	0.18µm	2,5	1,2	240	0,2
2004	0.12µm	2,5	1	480	0,1
2006	90nm	2,5	1	900	0,07
2008	65nm	1,8	1	2 000	0,05
2010	45nm	1,8	0,9	3 500	0,04
2012	32nm	1,5	0,9	4 800	0,03
2014	28nm	1,2	0,8	8 000	0,02

As presented in II.3.2.1, the EME level (conducted and radiated) of an integrated circuit is related with the transient current amplitude which is defined by Equation II-1. As resumed in Table II-2, although the power supply and the current peak per gate decline with the technology scale-down,

however, with the increasing density of gate, the current peak density year after year. Besides, as shown in Figure II-19 (left), even the CPU clock frequency tends to saturate due to the power reduction and the parasitic capacitances, an increase processor frequency and a faster switching speed is still a trend, which means a larger $\frac{di}{dt}$ noise in Equation II-1. In addition, the increasing number of I/Os, which follows a nearly exponential low (Figure II-19 (right)), might create more parasitic emissions.

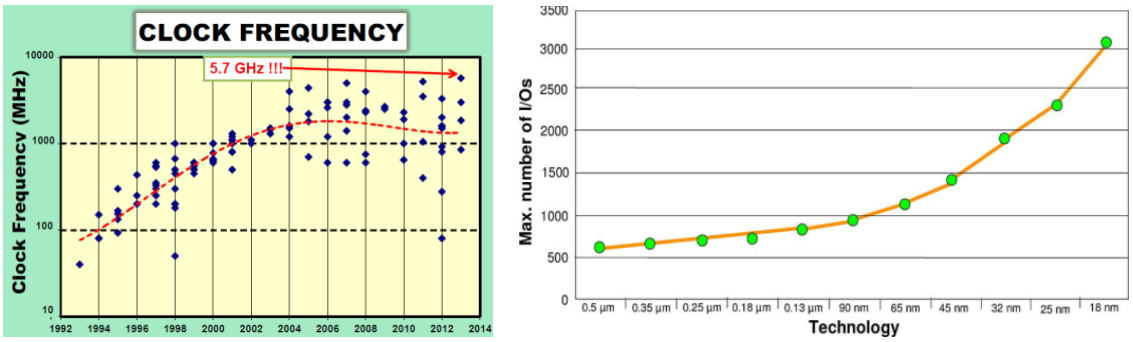

Figure II-19 (left) Trends towards a saturation of the CPU clock frequencies [ISSCC]; (right) Evolution of maximum number of I/Os [ITRS]

Another EMC challenge is the decreasing noise margin which is related with the reduction in the power supply. We know that ICs with lower power supply consume less battery, but also have a lower associated noise margin (normally the noise margin is the power supply divided by 5). As shown in Figure II-20, the voltage reduction slows down in the future, and the noise margin is predicted to be less than 0.1 V in the near future. A reduced noise margin means lower EM interference level could provoke the failure of system, in other words the circuit will become more and more susceptible to the EM interference.

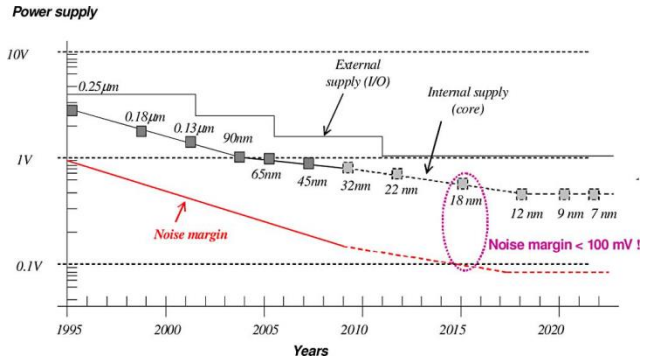

Figure II-20 Reduction of internal supply voltage leads to a reduced noise margin [RAMD09]

II.3.4. EMC measurement of ICs

Standard measurement systems are required to qualify EMC of ICs. These standards have to take into account of the high complexity and the small size of ICs. In 1996, IEC established a specific subcommittee WG9 which focused on test procedures and measurement methods for EMC of ICs

(Figure II-21). The objective of their work is to establish steadily low-cost, easy-to-use and reliable methods for characterization of EMC level of integrated circuits. The EMC measurement standards include emission measurement methods and immunity measurement methods.

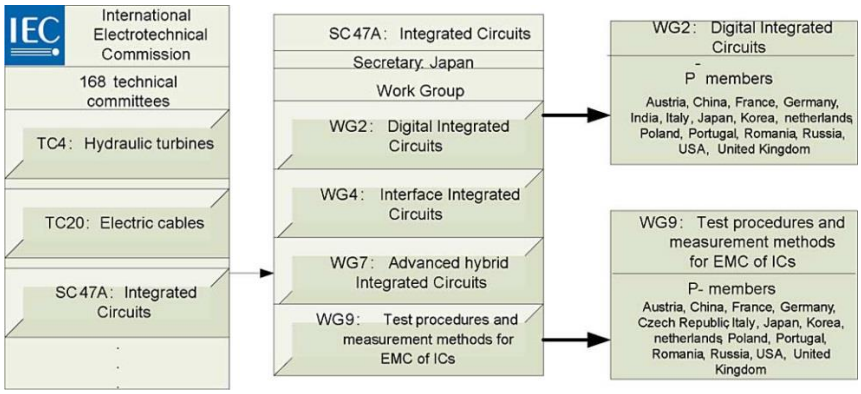

Figure II-21 Structure of IEC working groups for EMC of ICs [RAMD09]

II.3.4.1. EME measurement methods

The EME measurement standards of ICs are grouped under the IEC 61967 standard [IEC61967]. The general title of the IEC 61967 series is "Integrated circuits – Measurement of electromagnetic emissions". According to the information from the IEC official site, the latest published standards until 2015 are listed in Table II-3.

Table II-3 Published Standard IEC 61967—measurement of IC EME

Standard ID	Title
IEC 61967-1:2002	Integrated circuits - Measurement of electromagnetic emissions, 150 kHz to 1 GHz - Part 1: General conditions and definitions
IEC TR 61967-1-1:2010	Integrated circuits - Measurement of electromagnetic emissions - Part 1-1: General conditions and definitions - Near-field scan data exchange format
IEC 61967-2:2005	Integrated circuits - Measurement of electromagnetic emissions, 150 kHz to 1 GHz - Part 2: Measurement of radiated emissions - TEM cell and wideband TEM cell method
IEC TS 61967-3:2014	Integrated circuits - Measurement of electromagnetic emissions - Part 3: Measurement of radiated emissions - Surface scan method
IEC 61967-4:2002 +AMD1:2006 CSV	Integrated circuits - Measurement of electromagnetic emissions, 150 kHz to 1 GHz - Part 4: Measurement of conducted emissions - 1 Ω/150 Ω direct coupling method
IEC TR 61967-4-1:2005	Integrated circuits - Measurement of electromagnetic emissions, 150 kHz to 1 GHz - Part 4-1: Measurement of conducted emissions - 1 Ω/150 Ω direct coupling method - Application guidance to IEC 61967-4

IEC 61967-5:2003	Integrated circuits - Measurement of electromagnetic emissions, 150 kHz to 1 GHz - Part 5: Measurement of conducted emissions - Workbench Faraday Cage method
IEC 61967-6:2002 +AMD1:2008 CSV	Integrated circuits - Measurement of electromagnetic emissions, 150 kHz to 1 GHz - Part 6: Measurement of conducted emissions - Magnetic probe method
IEC 61967-8:2011	Integrated circuits - Measurement of electromagnetic emissions - Part 8: Measurement of radiated emissions - IC stripline method

The standard ID contains the information about the publication date. Except the general conditions and definitions in IEC 61967-1, there are 7 planned measurement methods (IEC 61967-2 to IEC 61967-8), and only IEC 61967-7 about the reverberant chamber radiated emission is still a proposal and not published. The early proposed standards have the definition of frequency range from 150 kHz to 1 GHz, but from 2010, the new published standard removed this frequency limit, so the frequency range is extended above 1 GHz. Figure II-22 illustrates several emission measurements in these standards. In this study, TEM radiated measurement and 1 Ω/150 Ω conducted measurement will be used in the examples presented in this PhD report, because of the good repeatability of these two measurements.

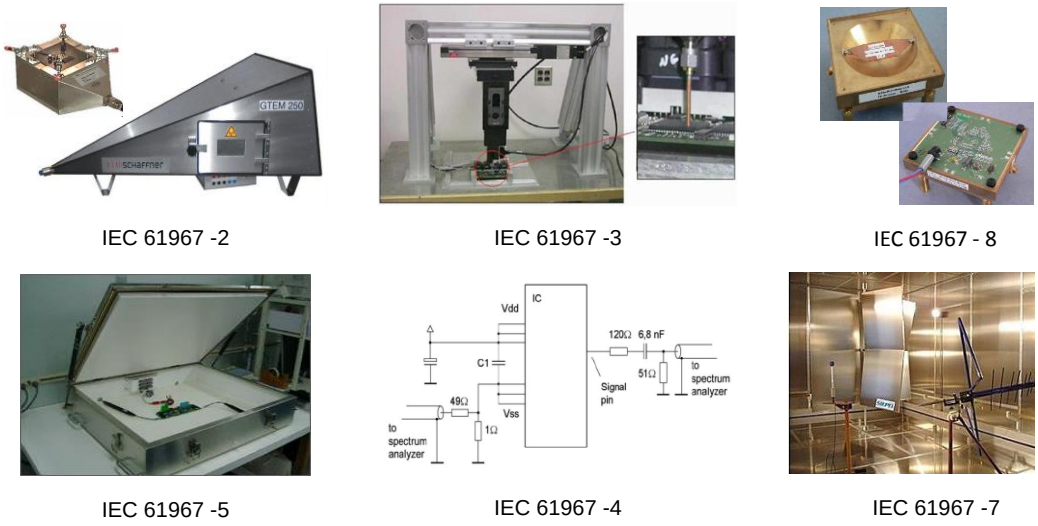

Figure II-22 IC electromagnetic emission measurement methods

II.3.4.2. EMI measurement methods

IEC 62132 is the standard dedicated to measure the electromagnetic susceptibility level of ICs [IEC62132]. Similarly to the EME standard IEC 61967, the frequency range in IEC 62132 is originally set up to 1 GHz, and recently extended above 1 GHz from 2010. As presented in Table II-4, there are 8 planed methods (IEC 62132-2 to IEC 62132-9), and two of them (IEC 62132-6 for Local Injection Horn Antenna (LIHA) method and IEC 62132-7 for Mode Stirred Chamber (MSC) method) are still during the preparation until today.

Table II-4 Published Standard IEC 62132—measurement of IC EMI

Standard ID	Title
IEC 62132-1:2006	Integrated circuits - Measurement of electromagnetic immunity, 150 kHz to 1 GHz - Part 1: General conditions and definitions
IEC 62132-2:2010	Integrated circuits - Measurement of electromagnetic immunity - Part 2: Measurement of radiated immunity - TEM cell and wideband TEM cell method
IEC 62132-3:2007	Integrated circuits - Measurement of electromagnetic immunity, 150 kHz to 1 GHz - Part 3: Bulk current injection (BCI) method
IEC 62132-4:2006	Integrated circuits - Measurement of electromagnetic immunity 150 kHz to 1 GHz - Part 4: Direct RF power injection method
IEC 62132-5:2005	Integrated circuits - Measurement of electromagnetic immunity, 150 kHz to 1 GHz - Part 5: Workbench Faraday cage method
IEC 62132-8:2012	Integrated circuits - Measurement of electromagnetic immunity - Part 8: Measurement of radiated immunity - IC stripline method
IEC TS 62132-9:2014	Integrated circuits - Measurement of electromagnetic immunity - Part 9: Measurement of radiated immunity - Surface scan method

Figure II-23 illustrates several EMI measurement methods for ICs. Several methods have the similar measurement instruments which are used in some EME measurements in Figure II-22, like TEM, Workbench Faraday cage (WBFC) and Near-field scan test bench. In emission tests, these instruments work as the receivers of the RF signals emitted by the tested IC devices. Contrarily, some test instruments work as the EM interference emitters in an opposite mode, to inject the electromagnetic noise to ICs under test. In our study, DPI test is selected because of its good repeatability and a precise localization of interference injection.

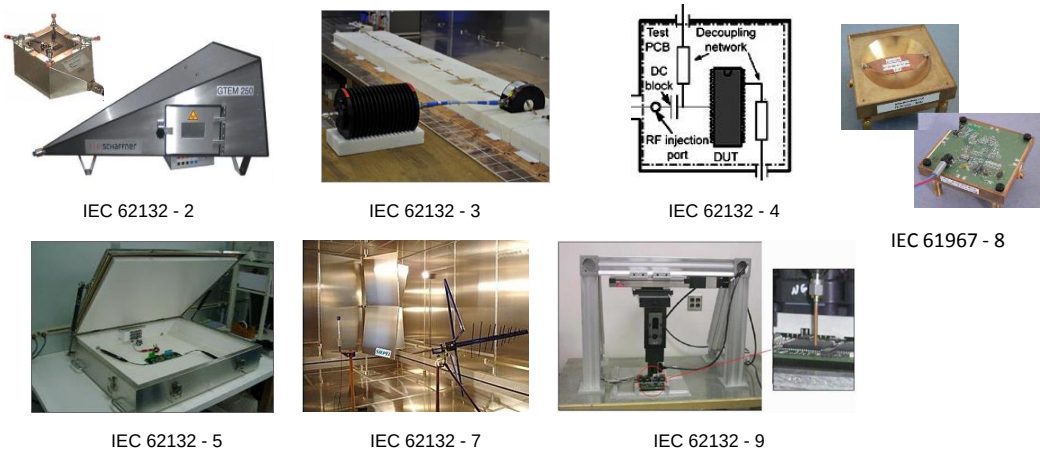

Figure II-23 IC electromagnetic immunity measurement methods

IEC 62132 is only devoted to the RF disturbance immunity. However, in practice, the ideally harmonic disturbances are uncommon. The interferences in real world are modulated perturbations (such as interferences from radio systems) or pulse noises (from choppers, motor controls, switching activities of electrical distribution networks, or Electrostatic discharge (ESD)). So electrical fast transient (EFT) is another common EM interference type to study in recent years. For this reason, the measurement methods for characterizing the impulse immunity of circuits are proposed by a new standard IEC 62215 [IEC62215]. This standard covers the transient immunity modes, such as ESD, EFTs and the electrical overstress (EOS) [RAMD09].There are already two parts of this standard have been published in the IEC site, as presented in Table II-5. As a recent proposal, even the first part of general conditions and definitions is not yet available. Except the two published methods, three other transient immunity measurements are also planned about Surge, Supply dips and Near field scan immunity.

Table II-5 Published Standard IEC 62215 — measurement of IC transient EMI

Standard ID	Title
IEC TS 62215-2:2007	Integrated circuits - Measurement of impulse immunity - Part 2: Synchronous transient injection method
IEC 62215-3:2013	Integrated circuits - Measurement of impulse immunity - Part 3: Non-synchronous transient injection method

There are already a lot of EMC measurement standards for ICs, and some of them have been widely used for real EMC tests. However, the measurements should be improved to adapt the technology development. One important restriction of the existed methods is the frequency range, which cannot adapt the increasing on-chip clock frequency of ICs. As presented in [RAMD09], the fastest processer could reach about 20 GHz by 2022. However, we haven't enough solutions yet, especially within high frequency range between 10 GHz and 40 GHz.

II.3.4.3. Margins of EMC level

In the industry, to verify and validate if the device is EMC compliant, the electronic products are tested in an EMC laboratory, using standardized EMC test methods as mentioned above. This process is called the "conventional" approach to achieve EMC compliance [ARMS08]. As explained in [ARMS08], the actual EMC validation methods are inadequate to assure safety in the real operation of electronic systems. For example, the foreseeable faults and misuse of circuits are not taken into account in the EMC measurement. Also, the simultaneous disturbances of different types are not tested, and only one port is tested at a time. Besides, the physical environment is usually ignored in the EMC measurement. The effects of the physical environment include the following issues:

- Mechanical (static forces, shock, vibration, etc.)

- Climatic (temperature, humidity, air pressure, etc. – both extremes and cycling effects)
- Chemical (oxidation, galvanic corrosion, conductive dusts, condensation, drips, spray, immersion, icing, etc.)
- Biological (e.g. mould growth, etc.)
- Operational 'wear and tear' over the lifecycle (friction, fretting, repetitive cleaning, grease build-up, etc.)

The physical environment could have a significant influence on the EMC measurement results. For example, in [BEND07], the great variation of conducted emission level on a port of a microcontroller can be observed under different ambient temperatures, as shown in Figure II-24. In additions, the EMC compliance validation tests do not consider the variation of EM performance induced by the aging degradation over the whole lifecycle. This long-term EMC issue will be discussed in section II.4.

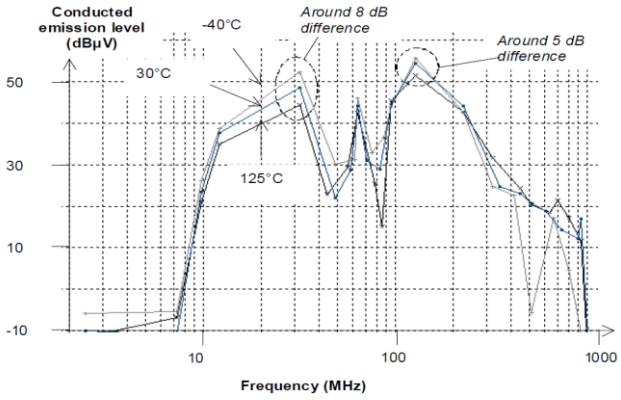

Figure II-24 Conducted emission measured on Port S (port inactive) of a 16-bits microcontroller for varying temperature (-40°C, 30°C, 125°C) [BEND07]

As shown in Figure II-25, in the EMC compliance validation tests, some supplementary margins, like dispersion between the different samples, the measurement errors and the additional safety margin, should also be considered in order to avoid the unforeseen impact caused by ignored EMC effects during the measurement process. The EMC measurement results could not be extracted from a single device but a sufficient amount of DUTs. IC dispersion margin can be obtained from the statistical analysis of the EMC measurement results of a large amount of DUTs, which should cover almost all the possible EMC level from measurements. Measurement error level is rather related with the random variation from observation to observation and the accuracy of experimental instruments. And finally, a safety margin is set to assure the EMC compliance is in a superior level than the basic EMC performance requirement, which could reduce the EM influence induced by ignored factors in the standardized measurement methods [BEND09].

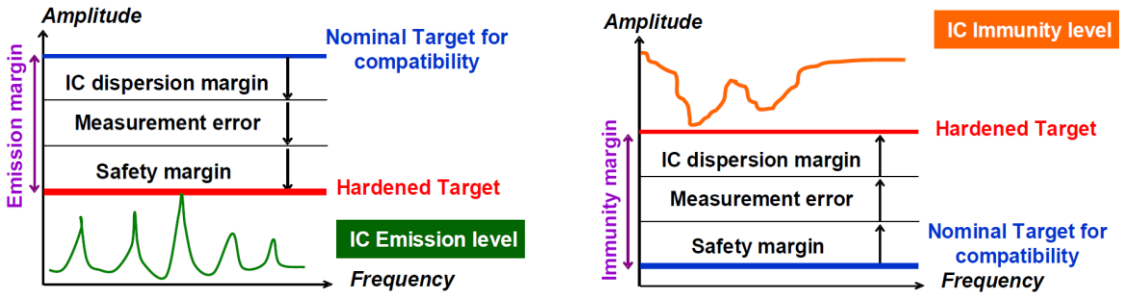

Figure II-25 Verification of EMC compliance with additional margins [BEND09]

II.3.5. EMC modeling for IC design

As presented above, EMC problem becomes a major concern for the semiconductor industry. However, EMC was a subject little considered during the former IC design flow in the last century. As shown in Figure II-26 (a), in 1990s, the EMC levels of ICs were characterized in the end of the design flow which was after the design and the fabrication of prototype devices. Owing to the lack of EMC consideration, re-designs are usually required caused by the non-compliance to EMC regulation, which has become the 3rd re-design reason in IC design flow. The unexpected IC re-design increased the cost of product and delayed the final production to market [VRIG05].

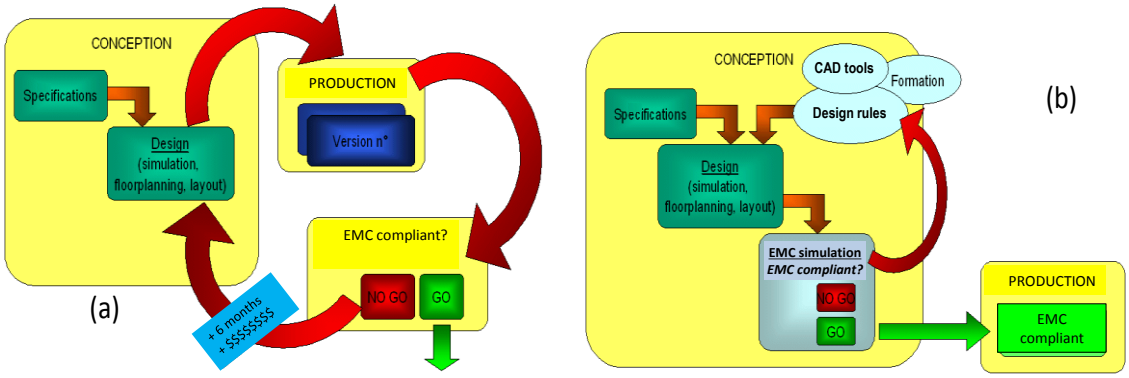

Figure II-26 IC design flow evolution [VRIG05]

To avoid the costly phase of re-design of integrated circuits, the EMC compliance verification by simulation was advanced during the design phase, before the prototype fabrication, as illustrated in Figure II-26 (b). The objective is to establish a predictive model of the EMC levels of circuits as early as possible during their design flow and to optimize the design to ensure the EMC compliance.

During the development of a new product, several mature blocks from the design libraries are usually re-used by semiconductor industry in order to reduce the cost and time. So if we have the EMC model library of each functional block, the EMC performance of a new product could be simply simulated and optimized. Additionally, the system equipment manufacturers, especially the manufacturers in automotive or aeronautic applications who integrate a large numbers of IC chips in their systems, require sufficient EMC characterization information of ICs. However, the detailed

architectures of integrated circuits are often confidential for the industry, and they cannot provide the information like design libraries to the users of their products. For this reason, a simplified EMC model of IC which does not contain the confidential information (black box or gray box) could be interesting for both IC fabricators and system equipment manufacturers.

In the early 90s, I/O Buffer Information Specification (IBIS) dedicated to electric performance simulation of the input/output structures of ICs was created by Intel. The first version of IBIS standard IEC 62014 was published in April 1993, and the latest version 3.2 as an IEC standard was updated in 2001 [IEC62014-1]. However, IBIS have its own official site IBIS Open Forum (http://www.eda.org/ibis) [ref forum IBIS] which is the industry organization responsible for the management of the IBIS specifications and standards, and the update is much more frequent than the IEC standard. The latest specification IBIS version 6.0 is ratified on 20 September 2013.

However, IBIS modeling method is not specified for the EMC analysis but rather for the signal integrity analysis, and its usefulness in EMC simulations is limited. As a result, in 1997, the subcommittee WG 2 of the IEC in Figure II-21 began to extend the standards of EMC modeling for integrated circuits. In 2002, a new IEC standard 62014-3 about ICEM method (in IEC 62014, ICEM means "Integrated Circuit Electrical Model" [IEC TS 62401-3], but in the later standard IEC 62433, ICEM means "Integrated Circuit Emission Model" [IEC 62433-2], which is also used in our study) was proposed by the French standardization committee "Union Technique de l'Electricité" (UTE) for the modeling of conducted and direct radiated emissions [RAMD09]. Simultaneously, the Interface Model for Integrated Circuits (IMIC) was proposed by Japanese and be published as standard IEC 62404 at the end of 2003, which provides analytical interface models for the simulation of signal integrity, power integrity and conducted EM emission. Besides, another modeling method named Linear Equivalent Circuit and Current Source (LECCS) is proposed for a fact EME/EMI simulation of digital devices and printed circuit boards, which is implemented with a High Speed EMI simulator (HISES) software[OSKA03] [WADA03]. In additions, the study of standard immunity methods Integrated Circuit Immunity Model (ICIM) are in writing to be submitted for standardization.

These works and propositions provided the basis for a new systematical standard IEC 62433, which aims to evaluate EMC levels and performances for ICs. All the published IEC standards about EMC modeling at IC level are summed in the following Table II-6.

Table II-6 Published IEC standards related to EMC modeling for ICs

Standard ID	Title
IEC 62014-1:2001	Electronic design automation libraries - Part 1: Input/output buffer information specifications (IBIS version 3.2)
IEC TR 62014-3:2002	Electronic design automation libraries - Part 3: Models of integrated

	circuits for EMI behavioral simulation
IEC TS 62404:2007	Logic digital integrated circuits - Specification for I/O interface model for integrated circuit (IMIC version 1.3)
IEC TS 62433-1:2011	EMC IC modelling - Part 1: General modelling framework
IEC 62433-2:2008	EMC IC modelling - Part 2: Models of integrated circuits for EMI behavioral simulation - Conducted emissions modelling (ICEM-CE)
IEC TR 62433-2-1:2010	EMC IC modelling - Part 2-1: Theory of black box modelling for conducted emission

There are totally 6 modeling methods in the projected plan of standard IEC 62433, the modeling method of each standard and their state are listed in Table II-7.

Table II-7 Modeling methods in standard IEC 62433 and their state

Standard ID (planned)	Modeling method	State
IEC 62433-2	ICEM-CE (conducted emission)	Available
IEC 62433-3	ICEM-RE (radiated emission)	Draft of standard
IEC 62433-4	ICIM-CI (conducted immunity)	Draft of standard
IEC 62433-5	ICEM-RI (radiated immunity)	Research undergoing
IEC 62433-6	IC model for impulse immunity	Research undergoing
IEC 62433-7	IC model for intra-bloc EMC	Research undergoing

Nowadays, the available EMC models for ICs have been used by various IC manufacturers and system integrators. The tools like Sigrity of Cadence could provide power and signal integrity EMC system-level analysis solutions for PCB board and package designers [SKYT09]. IBIS is supported by most semiconductors and Electronic design automation (EDA) tool vendors [HUQ98].

There are already a lot of modeling studies of EMC levels of ICs. Not only the officially published ICEM-CE method is widely applied, some other methods have been also applied in several studies which demonstrated a good accuracy of their EMC models. In the work of [LOCH03], ICEM is applied of a 16-bit commercial microcontroller (MOTOROLA) in order to predict the results of 1 Ω/150 Ω conducted emission measurements, and the simulation results demonstrated a reasonable accuracy with the measurement. The work in [LABU08] demonstrates that a single EMC model, built according to the ICEM model, can be used to predict the emission measurement, both for conducted emission method (1 Ω/150 Ω conducted emission method) and radiated emission methods (TEM method and surface scan method). In the other hand, the susceptibility level of ICs is also studied. In [BOYE07],

modelling of the susceptibility of 90 nm Input Output Buffer had a good fit with measurement until 500 MHz. And [MAO12] and [WU14] demonstrated respectively the EMI levels of ESD protection pads and a low dropout voltage regulator could be modeled with the method ICIM. In additions, in [ZHAN10], an accurate immunity model for an 8-bit microcontroller to EFTs is developed and verified.

However, there are still some difficulties for the future EMC modeling work, like the requirement of the accuracy of interconnection models at high frequencies, the reduction of simulation times on complex non-linear circuits [GIEL09]. Besides, the confidential protection is always a problem for the non-linear modeling, like the radiated emission and the immunity modeling of mixed-signal blocks [RAMD09] [GAZD12]. Several EMC modeling methods are detailed in Chapter IV, and the EME and EMI modeling process are demonstrated respectively through two case studies, where the black-box modeling methods are briefly discussed.

II.4. EM Robustness

II.4.1. Context

Nowadays, the performance of devices and systems are largely enhanced due to the increasing use of electronic modules. However, the degradation of electronic pieces becomes one important critical source of system failure [WHIT08] [VICH06]. The degradation of electronic components can be caused by aging during the operating of system, and some conditions can accelerate the aging process, such as high temperature, vibration, voltage surge and current spike. Here we enumerate several typical critical applications as the examples under the hard operation environment, and the EMC problems for each one.

- Spatial applications

In order to reduce the volume for the applications, such as satellite, space station or interplanetary space probe, the different functional modules are highly integrated in a spacecraft, which produces the inter-system EMC problems. Likewise, spacecraft are submitted to the EM interference in outer space, such as spatial electromagnetic radiation and ionizing radiation from the sun and the other stars.

For the spatial equipment, their working environmental temperature is very unstable and extreme. For example the temperature range for an artificial satellite is from -115 °C to 260 °C. Besides, without few on-site maintenance and repair, the spatial devices should work for a long time. The average life of a satellite or a space station is from 5 years to 20 years, and for an interplanetary space probe, the life is often as long as possible. Like the space probe Voyage 1 which has left the solar system in 2013, it has operated more than 37 years and it still operates and communicates with earth.

During their long operation period, the extreme operating conditions accelerate the aging mechanisms of the embedded electronic devices, which could be the evolution source of EMC levels of the system.

- Aeronautic applications

There is little protection by atmosphere for an aircraft flying at an altitude of 12000m against cosmic radiation. Lightning and radar radiation are two other possible external EM disturbances for airplanes. Besides, the integration of various electronic systems in airplane cabin leads to complicated intra-system interference. The operation environment for a plane is also extreme, and the electronic devices embedded should be able to work from -55 °C to 125 °C [LI11]. Besides, the strong vibration is also an important factor to accelerate the aging degradation. Although we have the recurrent maintenances to ensure a good state of the aircrafts, the aging mechanisms should be also accounted for safety reason. For the electronic devices, it's important to ensure the EMC compliance during the whole operation life.

- Automotive applications

Nowadays, with the rising needs in functions like safety, multimedia and telecommunication, automotive electronic systems contain over one hundred microcontrollers [DAVI08]. The life of a car is usually designed for 10 years, while the electronic systems operate under a much larger temperature range (-40 °C to 125 °C, 150 °C at junction level) than that of commercial applications (0 °C to 70 °C). The reliability and EMC are popular subjects to automotive electronics manufacturers, because both problems are crucial to the whole system security.

There are a large number of works focused on the detection of the degradation source and the prediction of the system failure, like Prognostics and Health Management (PHM) proposed to predict and assess the reliability or the "health state" of the electronic system during its operating life [VICH06]. All these studies aim rather at the performance analysis or life-time prediction of system, in order to assure the long-term functionality in certain margin. However, the long-term electromagnetic compatibility evolution of system is often neglected.

II.4.2. EMC problem in long term

In Figure II-27, two unexpected evolution possibilities of EMC levels are illustrated. Here the increase of emission level or the decrease of immunity level in some frequency-ranges, caused by the aging mechanisms during the operation lifetime of the devices, represent a reduced EMC performance. When the EMC drift of a device exceeds the threshold limit, this device is no more EMC compliant.

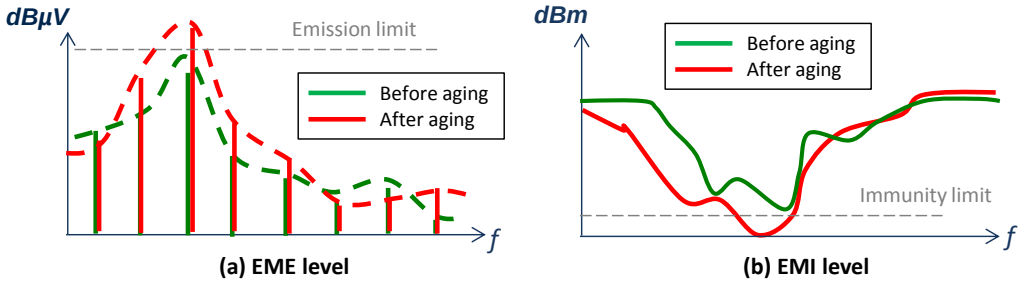

Figure II-27 Possible evolution of EMC levels after aging: (a) EME level, (b) EMI level

Some studies have demonstrated the possible EMC risks. In [LESS93], the shielding effectiveness (SE) of an aluminum flange decreased after 192 hours of sulfur dioxide alt fog exposure, the degradation was 36 dB at some frequencies (Figure II-28), which means the shielding protection performance against the external RF interference decreased, and of course the EMI level of the system using this device also decreased.

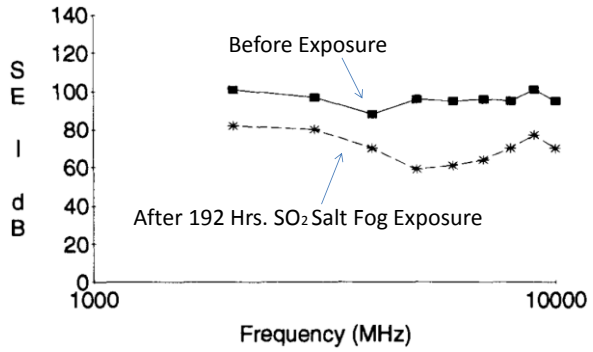

Figure II-28 Shielding effectiveness versus frequency for NiGr Gasket-6061-T6 aluminum flange [LESS93]

Another example in [LAHY98] is the degradation of aluminum electrolytic capacitor, which was used as the output filtering capacitor of a Switching-mode Power Supply (SMPS). Due to the increase in equivalent series resistor (ESR) after 175 hours of thermal aging, the output-voltage ripple had a significant increase, as shown in Figure II-29. The increase of the amplitude of voltage ripple means an increase of the electromagnetic emission level at the switching frequency (66 kHz).

The current and practical EMC test to quantify the components is often carried out only on the fresh devices or the devices after a very early infant mortality, using standardized test methods. This is the conventional approach for the EMC compliance verification. Although the accelerated life tests are applied to ensure the functionality of the system, but the EMC levels are usually not characterized after the aging process. Thus, the EMC issue needs to be studied with the reliability tests under the real-life conditions, to ensure a long-term EMC compliance and "functional safety" during the whole lifetime [ARMS05].

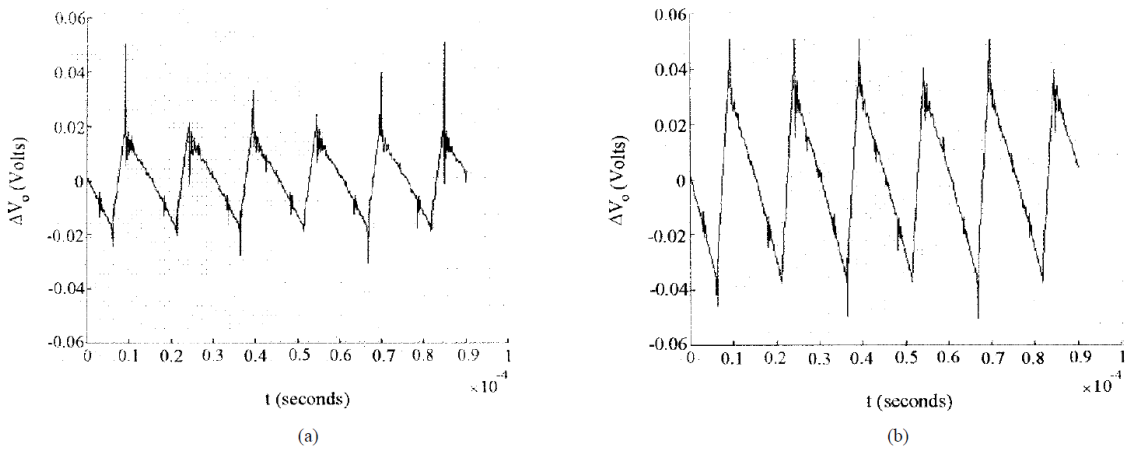

Figure II-29 **Influence on output voltage of a SMPS with different output filtering capacitor: (a) Sound capacitor, (b) aged capacitor [LAHY98]**

II.4.3. Prediction of EMC evolution induced by aging

Nowadays, with the performance development of electronic models, the system manufactures are forced to optimize system reliability within a reduced market delivery time and a controllable manufacturing cost. As a result, this trend has induced an increasing demand to predict the lifetime and future statements of the product to the design stage, ranging from electromagnetic effects (EMC/RF) to thermal management and thermomechanical reliability forecasts, similar to the EMC simulation during the product design illustrated in Figure II-26 (b) [BEND13].

Technological development of ICs brings performance enhancement and dimension shrink. However, as resumed in II.3.3, the increase of dissipated power and leakage current generates more EM emissions, and the reduced supply voltages and increasing external and intra-system EM noise tend to decrease the immunity ability to RF interference. EMC has become a major cause of IC redesign. Adequate design methods and expertise are required to reduce the parasitic noise and improve immunity [RAMD09] [LI11].

Simultaneously, working under harsh conditions provokes the acceleration of degradation mechanisms on several electronic devices (like MOSFET or passive devices, their degradation mechanisms will be presented in Chapter III), which threats the reliability of circuits [WHIT08]. Even under normal environmental conditions, the degradation mechanisms would still occur after years' operation. Sometimes the failure mechanisms don't compromise the circuit operation, and the device could continue to work without failure, but the performances (reliability, operation frequency, static noise margin…) of devices would be degraded. Among these circuit performances, EMC margins could be significantly impacted by the IC intrinsic degradations, increasing the risk of EMC compliance failure, as immunity decreases or emission increases (Figure II-27) [LI11] [BEND13].

As a result, ensuring the electromagnetic compatibility for the full lifetime has become an important requirement for the industry [BEND13]. So the study of EMRIC (Electromagnetic

Robustness of Integrated Circuits) is proposed, which aims at ensuring the EMR of embedded systems at the IC level [PFAF05]. This new research activity builds a bridge between "IC reliability" and "EMC of ICs". These two communities are not much overlapped before. The objectives of the EMRIC study could be resumed in 4 points:

- Prove the aging effects on EM emission and immunity of ICs
- Evaluate the effect of technology and design on long-term EMC
- Understand mechanisms that affect emission and susceptibility
- Model IC emission and susceptibility level drift after aging

In our study, except the IC components, we add the analysis of the influence of passive components aging.

Nowadays, we have already several EMR studies on ICs. Publications such as [BOY14] have shown the electromagnetic emission (EME) of digital circuits and I/O buffers changes with time because of the activation of intrinsic degradation mechanisms, as illustrated in Figure II-30.

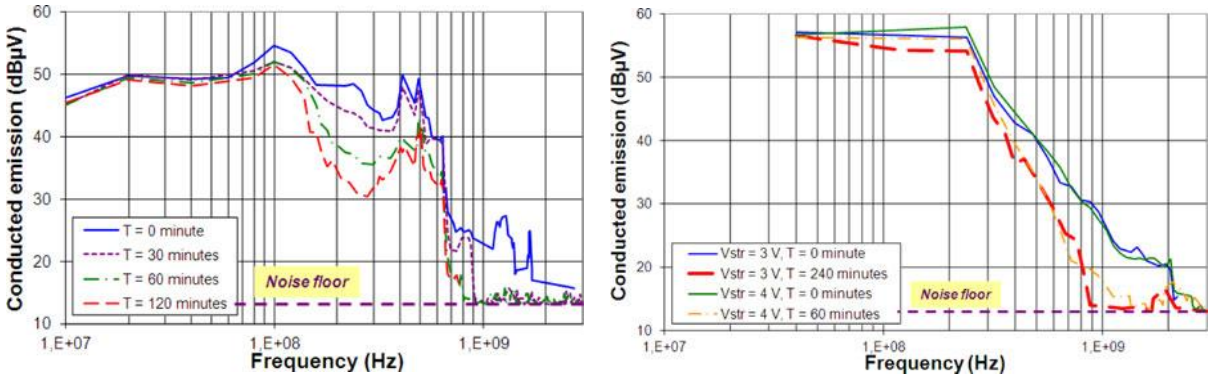

Figure II-30 Change in conducted emission of the output buffer after 7-V electrical stress over 120 min (left) and a digital core before and after 3- and 4-V electrical stress (right) [BOYE14]

As presented in only few works, the simulation can be used to predict the long-term EMC level. For example, in [BOYE11], the simulation results confirm the evolution of the electromagnetic susceptibility (EMS) of a phase-locked loop (PLL) before and after aging, as demonstrated in Figure II-31. The aging affects the threshold voltage and the mobility of the MOSFET of the PLL. However, in these case studies only two statuses (the device before and after a period of aging) are measured and simulated. Thus there is a lack of more precise insight about the evolution of the different phases during the whole aging time.

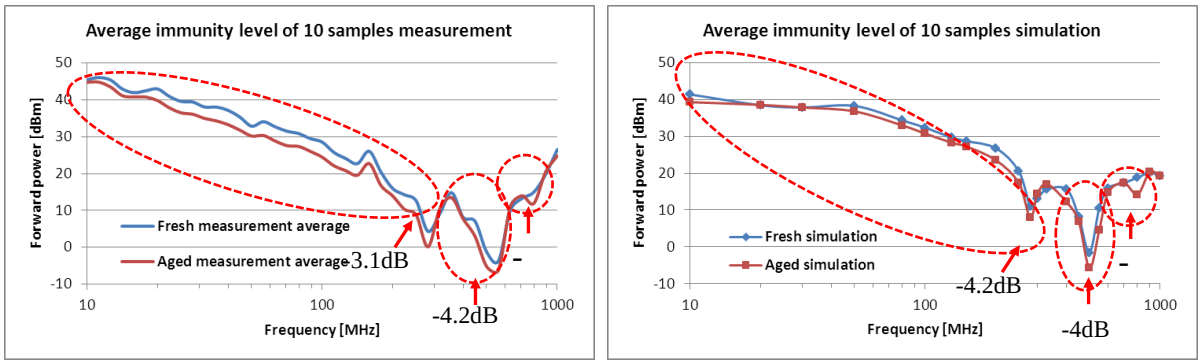

Figure II-31 **PLL EM immunity measurement (left) and simulation (right) before and after ageing [LI11]**

II.4.4. EMC drift dispersion induced by aging

The EMC drifts dispersion might be observed from the different samples of the same device reference. An example of the immunity drift of 10 PLL samples under the same aging stress is illustrated in Figure II-32. Although the immunity level decreases for most of the tested samples, the sample number 5 demonstrated a slightly improved immunity. Even for the samples which have a decreased immunity level, the drift values for each sample have a significant difference.

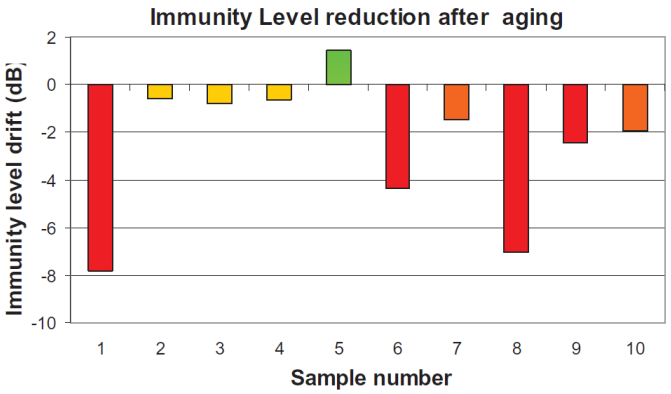

Figure II-32 **Immunity Evolution to conducted injection of PLL after aging of 10 samples [BOYE11]**

From statistical point of view, the EMC levels of whole components are assumed to respect a Gaussian distribution [LI11]. An example of immunity variation induced by aging is presented in Figure II-33. In left, the EMI evolution of a sample after aging stress surpasses both safety target and immunity limit, and the device is no more EMC compliant. However, only one sample could not represent all the other samples, as shown in Figure II-32.

For a group of samples, the EMC evolution should be studied from a statistical point of view, as shown in Figure II-33 (right). In this figure, the EMC non-compliance of a group of samples is represented by a failure probability, since we cannot predict precisely the EMC drift value of a single sample, but the evolution of failure probability for all samples could be obtained. Some other information related to the EMC evolution, like the mean EMC compliant time and EMC failure rate at

each aging phase, could be obtained from the statistical analysis, which it very useful in the EMR study. The statistical analysis in EMR studies will be presented in last chapter.

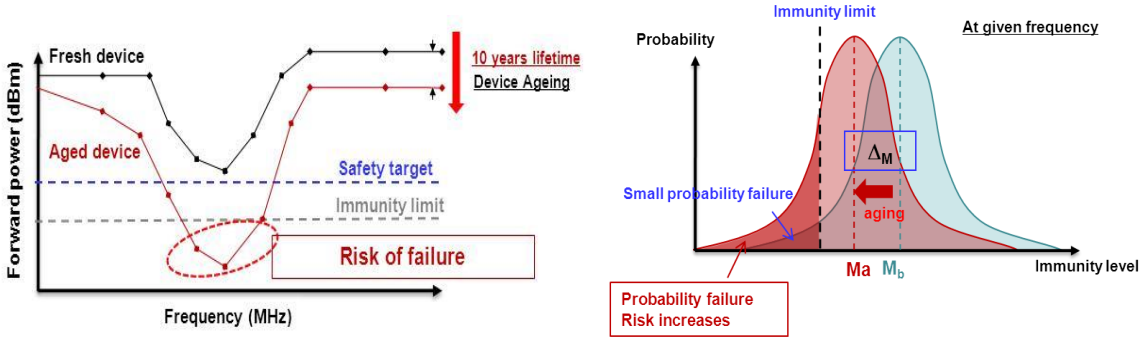

Figure II-33 Immunity level decrease with device aging (left) worst case, (right) statistical view [LI10]

II.4.5. General EMR prediction flow

The objective of this study is to construct models to predict the EMC evolution related with the degradation of components (IC components and passive components) induced by aging. In the EMR study of this thesis, the first stage is the characterization of EMR of a circuit in measuring its emission and/or susceptibility level before and after aging. We need to prove the aging effects on EMC and to understand the link between the physical degradation of components and EMC drifts. This link should be verified by either experimental measurements or simulation analysis. Then we need to identify the source of EMC drift which is usually the degradation mechanisms of certain components in the whole system. After the identification of EMC drift source, we can start the EMR modeling procedure. This process should take into account the operational conditions and operating time.

The general EMR modeling flow is shown in Figure II-34. Usually the EMC model is presented by an equivalent electrical model of the whole system which contains not only the components, but also PCB traces or planes and the test environment.

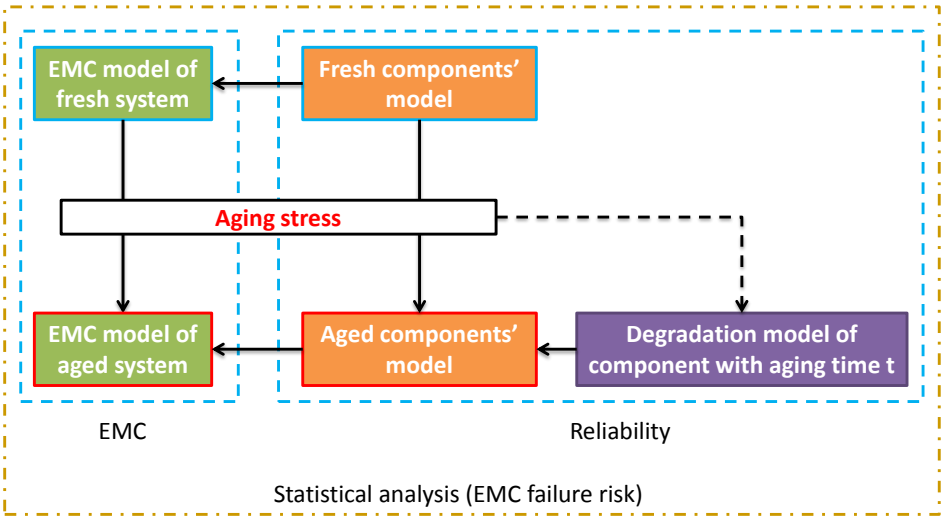

Figure II-34 General EMR modeling flow

The fresh EMC model could be validated by the comparison with experimental measurements. If the EMC drift is caused only by the degradation of certain components in the system, we can then use the same EMC modeling structure in the EMR studies. The aged components' models could be obtained based on the degradation models of each component with aging time t. The aging degradation of two types of components: IC components and the passive components are studied here, and they are assumed as the major source of the EMC drift. Then with the embedding of aged components' model in the EMC model, EMC levels in the long-term could be modeled. The EMR model is the combination model of "reliability" model and "EMC" model, which will be presented respectively in the following chapters.

In this thesis, based on the former studies, we focus on the prediction of the EMC drift in a long-term, and we try to provide a general modeling method to predict the aging impact on electromagnetic levels. To achieve this goal, the degradations of components, which are the source of aging impact on EMC levels, are studied. In the other hand, the EMC models are constructed based on the existing studies. With the degradation models injected in the EMC models, the evolution of EMC levels over time could be predicted in two case studies: EME drift of a DC-DC converter and EMI drift of an operational amplifier. Besides, the additional subject about black-box EMR modeling which could protect the intellectual property of EMC design details is presented.

As there is the dispersion of the aging impact on different samples under the same aging conditions, the statistical analysis is necessary in EMR modeling of a group of devices. With the statistical analysis, the EMC evolution is not only a simple evolution level of a single sample, but the EMC compliance failure risk of the global sample group. The statistical analysis methods will be detailed in Chapter V.

II.5. Conclusion

In this chapter, we introduce the EMR issues, which is a combination study of "reliability" and "EMC". The context of the EMR issues and also the general EMR modeling flow are presented in this chapter. As two part of EMC modeling, the reliability and EMC modeling process will be presented in two following chapters, respectively. Besides, this chapter explains the importance of the statistical analysis in the EMR prediction, due to the dispersion of aging impact on different samples. The statistical analysis of EMC reliability will be presented in the last chapter.

According to the discussion of this chapter, the objective of this study could be defined. We tend to propose the general modeling methods which is based on the measurement and simulation, in order to determine the evolution of EMC level of components (ICs and passive components), and to anticipate the possibility of EMC non-compliance in the long-term.

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Chapter III. Origin of EMC drift with time: Reliability issues of electronic devices

III.1. Introduction

Nowadays, the performance of devices and systems are largely enhanced due to the increasing using of electronic modules. However, the degradation of electronic pieces becomes one important critical source of system failure [BOWL92] [VICH06] [SAHA09]. A typical example in our life experience is the decrease of the performances of Personal Computers (PCs) over the years. Normally they become slower and noisier to remind us it's time to consider changing a new one. This is partly related with the update of software which usually requires a better hardware, but the degradations of the hardware, like the hard disk drives or CPUs, cannot be neglected.

The degradation of electronic components can be caused by aging during the operation of system, and some conditions can accelerate the aging process, such as high/low temperature, vibration, overvoltage, voltage surge and current spike. This degradation of components could induce the decline of the performances of system, which include the EMC level. Although the EMC level could not be presented directly by the electrical activities of system, the decline of EMC performances can increase the probability of unexpected system failure [BEND05] [BEND13]. EMC is one important performance of electronic systems, which is always related to their embedded components. An example of the top side of PCB card of a SSD disk is shown in Figure III-1. Here, the switching activities like clock provided by the microcontroller and the high speed I/O activity of the memories are usually the source of electromagnetic emissions. Except the IC components, there are also a lot of passive components like capacitors in this card. Here the passive components are always used for filtering and decoupling between the modules, which have also strong influence to the EMC levels of the system. That is why the degradation of these two groups of electronic devices (IC and passive components) is discussed in this chapter.

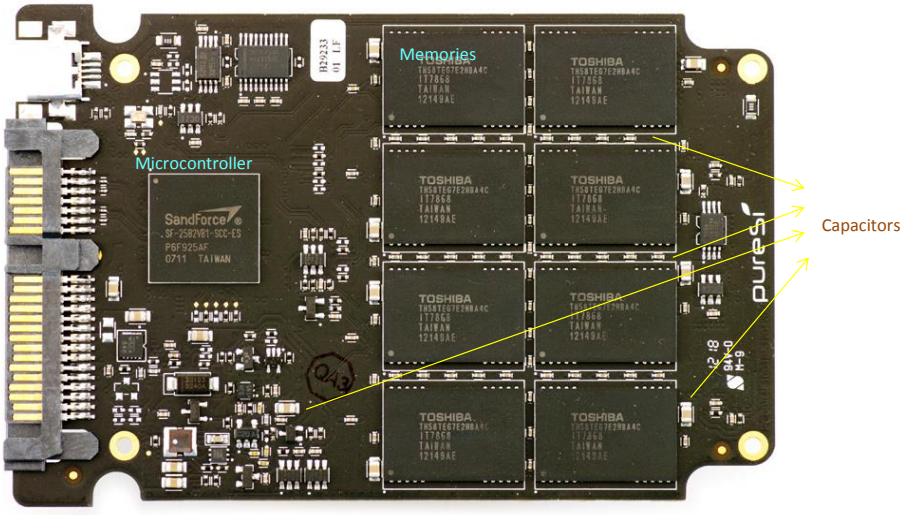


Figure III-1 Example of the PCB card of a SSD disk (pureSilicon Kage K1 Enterprise SSD) [LIND12]

Several former studies have shown that small changes in the parameters of the components could provoke a significant drift of EMC levels, and the evolution of EMC levels at long-term are related to the degradation phenomenon of components[BOYE09] [BOYE11] [WU13]. Theoretically, all the embedded components in an electronic system, even the packages and the transmission line could suffer from degradation mechanisms over the life time of system, and any part which could influent the EMC levels should be accounted in the EM reliability study.

However, in practice, the different components of system have the different reliability quality and some parts play more important roles to the EMC performance than the others. Thus, a good knowledge of the electronic system is required to identify the origin of the long-term EMC evolution. In other words it's necessary to single out which components in the system are degraded, and the degradation of which components affects the EMC level. The method to identify the source of EMC evolution will be detailed in next chapter of EMR analysis.

In this chapter, we focus on the study of the degradation of several common components (IC active transistors and passive components) which could have important impact in the EMC levels, as shown in the example of SSD card in Figure III-1. This chapter begins with a global introduction about the reliability of electronic devices. As two typical groups of electronic components, the degradation of semiconductor components and passive components are discussed in this chapter respectively. The main degradation mechanisms of semiconductor transistors are introduced. Then some former studies about the characterization and the modeling of these degradation mechanisms are resumed. Besides, the aging impact on several typical passives components is introduced. The aging characterization and modeling methods of passive devices are presented. A case study is used to show the variation of passive devices' impedance after different accelerated aging tests and the degradation modeling of two typical passive components (electrolytic capacitors and iron powder inductors).

III.2. Reliability of electronic devices

III.2.1. Definition of reliability

The reliability of electronic devices is defined as the probability that a product operates correctly for a given time period under specified conditions without failure [OHRI98]. A reliable electronic device means a low probability of failure during the service, vice versa. It's very hard to predict the lifetime of an individual sample, but with the failure test and the statistical analysis of sufficient samples, an average lifetime and its statistical distribution of a large numbers of components can be obtained. The reliability function is described by:

$$R(t) = \frac{n - \mathrm{r}(t)}{n} \qquad \text{Equation III-1}$$

Where

R(t) is the reliability function, which indicates the probability for functioning correctly without failure until time t.

n is the number of the samples used under the same conditions.

r(t) is the number of failures occurring until time t.

Normally, the reliability R(t) of a mature electronic product decreases from 1 to 0 over time, i.e. $R(0) = 1$ and $R(\infty) = 0$, which means that there is no failure for fresh devices, but more and more failures occur over the lifetime. According to the definition of reliability, three important parameters of "reliability" are discussed here to better understand this property:

- Lifetime period

As an important part of quality assurance, the service lifetime is a key parameter of any commercial electronic device. The mean lifetime period of a product could be explained by Mean Time Between Failures (MTBF) for repairable product and Mean Time To Failure (MTTF) for non-repairable product. These two terms refer to the estimated mean time to failure based upon a statistical sample.

In some special cases, the notions like the mileage for a car, or switching times for an interrupter, which are related with operating time period can be also used in the definition of reliability.

- Specified conditions

The ordinary operation of an electronic product usually requires specified conditions, like the level of power supply and environmental factors such as temperature, humidity and vibration.

Besides, the lifetime tests usually apply the thermal/electrical stressors to decline the test time, because they could accelerate the degradation mechanisms as it will be explained later.

It seems that the reliability problem of the electrical products is caused by the electrical activity during its service, but the products in a non-operating condition for a long period of time also have reliability problem. The products not in direct service are either in a state of dormancy or storage. In dormancy state, the equipment is connected and ready to operate but not operating. While in the storage state the equipment is completely inactivated. The dormant and storage environments of electronic products are always considered as secure, but as revealed in [PECH95], the electronic material could approach equilibrium through atomic diffusion or mechanical relaxation processes.

- Failure

As a state description of an electronic device, the failure should be well defined for the reliability study. The basic failure modes have been classified as short circuit, open circuits, degraded performance and functional [JENS95]. The complete failure (hard failure), which means the end of service of a device, is easy to understand, but sometime an inacceptable decrease of certain performances can also be defined as a failure (soft failure). The definition of failure depends on the device, its application and the expected functional performances. In the EMC study, the failure could be explained by EMC non-compliant, which means the EMC level of a device exceeds the defined EMC limit. As a result, usually when we consider the EMC drift, only soft failures are considered.

Actually, the reliability study is a probability study of system failure, so more detailed statistical analysis will be present in Chapter V.

III.2.2. Failure rate and Bathtub curve

Typically, the deterioration and destruction of the material is due to changes in the atomic and molecular levels. These change mechanisms include diffusion, oxidation, adsorption, dislocation (displacement), electrolysis, and the development of corrosion cracks. The different failure mechanisms coexist, and their failure rates are not the same. The failure rate λ is the number of appearing failed devices per unit time. The failure rate λ is not a probability. It presents a total number of failures per a particular measurement interval, so it could exceed 1. In the semiconductor domain, Failures In Time (FIT) is a commonly used unit to measure failure rate, a unit of FIT of a device means one failure per one billion (10^9) device-hours of operation.

The reliability of electronic devices could be presented by the famous “bathtub curve”, as illustrated in Figure III-2. The observed “bathtub curve” (purple, upper solid line) is a combination of a decreasing of early failure (blue, dotted line) and an increasing of wear-out failure (green, dotted line), plus some constant random failure (red, lower solid line) appearing in useful lifetime.

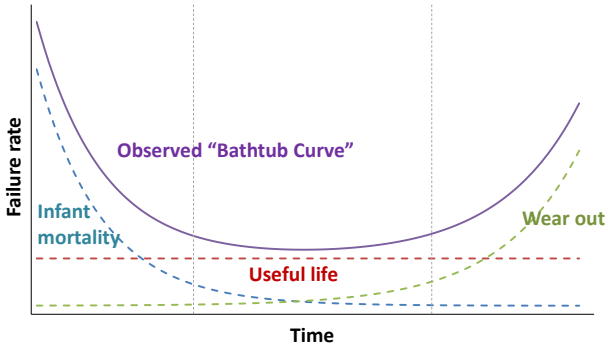


Figure III-2 Bathtub curve

The early "Infant mortality" failure is primarily due to problems in the manufacturing process, and this type of failure will be gradually reduced over time. In order to ensure a steady supply of good products on the market, strict quality control and process control are required. In addition, by burn-in or stress aging, the early failure impact could be eliminated in a short time. The random failure contains a roughly constant failure rate during the whole lifetime of the devices, and it depends on the design quality. As the "Useful life" period is more related with the external circumstance, this region normally corresponds to the operating life of the devices, and the characteristics of component remain stable during this period. Then the failure rate tends to increase rapidly in the last "Wear out" stage. Like human beings, after a long period of working, the electronic devices become fatigued and finally wear out. As the "Wear out" usually means the end of the product service, it's important to ensure the durability of products against wear out failure, to ensure a long lifetime [OHRI95].

The traditional lifetime analysis methods of components, like the measurements of MTBF or FIT, are simply statistical reliability tests from a large number of samples. However under real situation, the wear out failure of a component is caused by different degradation mechanisms rather than a single type of degradation. Furthermore, soft failure (degradation of performance) becomes the main failure rather than a hard failure where device is completely destroyed for the submicron technology [BAJE10]. Indeed, different wear out failure mechanisms should be analyzed and modeled to obtain more accurate reliability prediction.

III.2.3. Accelerated aging test

The failure rates of mature electronic devices are usually very low under ambient operating conditions. As a result the MTBF could be very long. For example, the MTBF of the new hard disk generation can reach 2 million hours, which means more than 250 years [SAMS]. It's not possible to apply the reliability analysis during such long time. In order to analyze the failures or the lifetime of electronic devices in a relative short period, accelerated aging tests are applied. Accelerated aging test is a method based on the artificial aging stress to speed up the normal aging processes of components.

The accelerated aging stresses facilitate the progress of deterioration of materials, and eventually lead to failures of components [RENE08]. The degradation speed of electronic devices depends greatly the operating and environment factors (e.g. temperature, humidity, supply voltage and current, operating frequency, vibration, pressure). For a given device, one or several aging conditions could be used to accelerate the failure and reduce the service time of products, the selection and definition of aging conditions should consider the devices' nature and their failure mechanisms.

The relationship between the accelerated aging time T_s and its represented real life time T_o is defined by an acceleration factor AF, we have:

$$AF = \frac{T_o}{T_s} \qquad \text{Equation III-2}$$

This acceleration factor is also a representation of the degradation speed. With this factor, we can predict the long-term evolution of an electronic device after several years. In addition, the aging stress level should be reasonable, it should assure a relative short aging time to accelerate the failure modes, and meanwhile the over-stress should be avoided because it may introduce failure modes that would never occur under use conditions.

III.2.3.1. Thermal accelerated aging

The temperature stress is widely used to accelerate the wear out failure of electronic devices. Oxide breakdown, Electromigration, and many packaging-related failure mechanisms are aggravated by an increase in temperature. On the contrary, the Hot Carrier Injection (HCI) effect is known to be enhanced with decreasing temperature [KUO98]. We could use the Arrhenius equation to calculate the failure rates. The Arrhenius equation describes the temperature dependence of reaction rates, it was proposed by Svante Arrhenius in 1889. The thermal acceleration factor AF_T could be defined by:

$$AF_T = e^{\frac{E_a}{k}(\frac{1}{T_o}-\frac{1}{T_s})} \qquad \text{Equation III-3}$$

Where

E_a is the activation energy of the failure mechanism. The activation energy is an energy threshold. If the energy supplied from the outside surpasses E_a, the component passes though the normal state to the deteriorated state. The value of E_a could be extracted by experiment.

k is the Boltzmann's constant, the value is about 8.617×10^{-5} eV/K.

T_s and T_o are absolute temperatures in Kelvin of the stress temperature and the normal ambient temperature, respectively.

The activation energy E_a is normally positive, so when the stress temperature T_s is higher than the ambient temperature T_o, the acceleration factor is higher than 1. Besides, a larger acceleration factor can be obtained with a higher aging temperature, as shown in Figure III-3. With the Arrhenius equation, we can consider the influence of the temperature during the aging process. An example in [KUO98] shows that for a given activation energy of 0.4 eV, if a device is to be burned-in with a temperature of 125 °C for 7 days, the equivalent time at the ambient temperature of 40 °C is more than 166 days (3989 hours), and here the acceleration factor is 23.7.

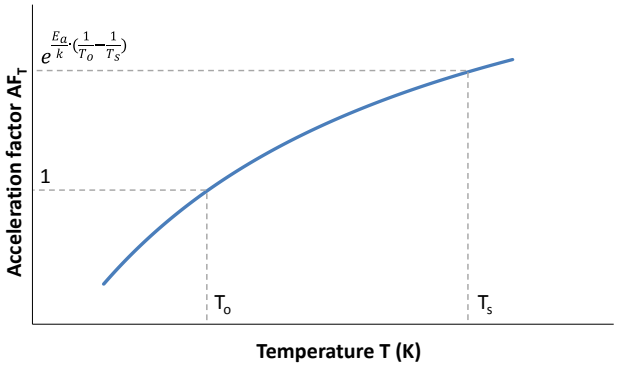


Figure III-3 Acceleration factor AF_T vs. operating temperature

A typical thermal stress test is the high temperature storage (HTS) test [AMER87]. In this test, the tested samples are not powered. The test temperatures are normally 250 °C for hermetic devices and 150 °C for plastic encapsulated devices. The tested samples usually should still pass the qualification test after HTS test of 1000 hours. Except the ambient temperature, the self-heating of component should be also considered. During a thermal aging process, the case temperature of DUT is given by:

$$T_{DUT} = T_a + \Delta T \qquad \text{Equation III-4}$$

Where

T_{DUT} is the real case temperature of DUT during the aging process,

Ta is the ambient temperature,

ΔT is the self-heating or the steady state over temperature attained at the hottest part of the device surface in relation with the surrounding atmosphere.

III.2.3.2. Voltage accelerated aging

Except the temperature stress, the voltage stress is also widely used to accelerate the aging of electronic devices. Time-dependent gate oxide breakdown (TDDB) and Negative-bias temperature instability (NBTI) are the well-known effects caused by the electrical stress on ICs. The failure speed which is due to oxide breakdown and hot-carrier damage goes up exponentially as the voltage stress

is increased, and the lifetime owing to electromigration are almost inversely proportional to the square of the current density [SABN90] [LAKS14]. The most widely used transformation model for voltage stress is expressed by [KUO98].

$$AF_V = e^{\beta \cdot (V_s - V_o)} \qquad \text{Equation III-5}$$

Where

AF_V is the acceleration faction for voltage stress

V_s is the accelerated stress voltage

V_o is the normal operating voltage stress

β is a constant which is related with the failure mechanisms and oxide thickness. It can be determined by experimental measurements according to Equation III-6.

$$\beta = \frac{\ln(\frac{r_1}{r_2})}{V_1 - V_2} \qquad \text{Equation III-6}$$

Where

V_1 and V_2 are two test voltages

r_1 and r_2 are respectively the failure rates at V_1 and V_2

However, the extraction of this kind of experimental coefficient β requires a large number of samples and tests. If we need a more reliable value of β, only two test voltages are not sufficient.

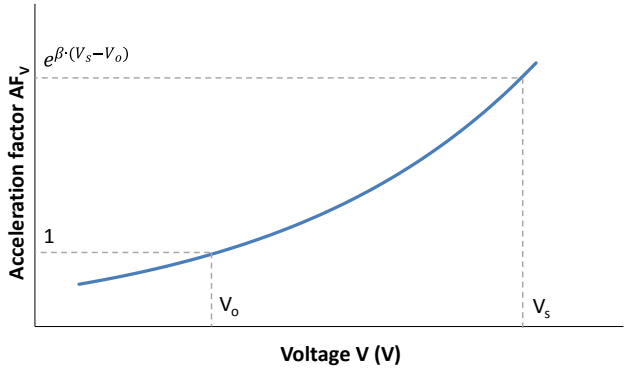


Figure III-4 Acceleration factor AFV vs. operating voltage

The acceleration factor with the operating voltage is illustrated in Figure III-4. Like all the other stress methods, the voltage stress should not be too large to provoke a direct damage to devices. According to an example in [LI11], for a device with technology 0.25 µm, the β value is about 3. So for the component whose standard voltage supply is 3.3 V, when we increase the operating voltage to 5

V, the voltage acceleration factor is about 164. It means that if the devices operate under the stress voltage during 100 minutes, the equivalent time at the typical ambient condition is more than 11 days.

III.2.3.3. Combined accelerated aging

The operation activity of electronic device induces a self-heating effect, and this effect becomes more important when the operating voltage increases, so the stress condition should consider both stress types. Besides, the combination of several different aging conditions could have a faster aging acceleration. To consider the interaction of multiple aging stresses, as a modification of Arrhenius equation, the Eyring reaction rate model are applied by [KUO98]:

$$r = A \cdot e^{\frac{E_{a1}}{kT}} \cdot e^{\frac{E_{a2}E}{kT}} \cdot e^{E_{a3}E} \qquad \text{Equation III-7}$$

Where

r is the failure rate,

A is a constant,

E_{a1}, E_{a2} and E_{a3} are the activation energies at which the failure mechanisms occur,

k is the Boltzmann's constant, the value is about 8.617×10^{-5} eV/K,

T is the absolute temperature in Kelvin (K),

E is the electric field.

In this equation, the first term $e^{\frac{E_{a1}}{kT}}$ describes an Arrhenius model of temperature. The second term $e^{\frac{E_{a2}E}{kT}}$ demonstrates the interaction between the temperature stress and the stress other than temperature. The third term $e^{E_{a2}E}$ refers to the second stress.

In some studies, the voltage stress and temperature stress are considered as two independent stress conditions [JIN06]. So for the combined accelerated aging condition of voltage and temperature, the acceleration factor can be obtained by:

$$AF_C = AF_T \cdot AF_V = e^{\frac{E_a}{k}\left(\frac{1}{T_o}-\frac{1}{T_s}\right)+\beta\cdot(V_s-V_o)} \qquad \text{Equation III-8}$$

Several standards, like JEDEC and AEC standard, have resumed different existed reliability aging method [AEC-Q100] [JEDEC22]. The high temperature operating life (HTOL) test, called high temperature with bias (HTB) test sometimes, is a common acceleration method for electronic devices. During this test, the DUT keeps on running with a high ambient stress temperature, where the bias applied to the DUT is equal or greater than the nominal value in the datasheet. HTOL test is usually used for the acceleration of Electromigration, NBTI and TDDB failure mechanisms. Another combined

test names low temperature operating life (LTOL) test is a similar test like HTOL just the ambient temperature is lower than the nominal value (-40 °C for example). The HCI mechanism can be accelerated under this combined accelerated stress.

There are lots of other accelerated aging methods for electronic devices, like ESD stress test, temperature cycling (T/C) test, humidity test, etc. And also there are numbers of methods of life-stress transformation methods, like Inverse power law model, Temperature-humidity model and Temperature non-thermal model [RELI14], that we do not detail here.

III.3. Aging impact on semiconductors and modeling

In [ORHI98], the author resumed that all failures in electronic materials and devices are caused by "the physical movement of atoms or charge carriers from benign locations associated with normal level to other sites where they contribute to creating or enlarging defects that lead to component malfunction". There are a large number of studies about the degradation of semiconductors as an independent discipline in the electronic domain. The propose of this part is not to provide a complete state of art of this discipline, but give some essential information about several typical semiconductor degradations, which could be served for the following EMC drift analysis.

III.3.1. Degradation mechanisms of semiconductors

There are different degradation mechanisms of semiconductors according various operating condition. In this part, three degradation mechanisms are presented: Hot carrier injection (HCI), Time dependent dielectric breakdown (TDDB) and Negative bias temperature instability (NBTI). That is because these three degradation mechanisms relate to the defect of the gate oxide of transistor which affects the transistor physical parameters. And these parameters like the threshold voltage or mobility might affect the EMC level of the electronic systems. Table III-1 sums up the brief descriptions and the impacts of these three transistor degradation mechanisms [WU05] [SCHR03].

With the presentation of the degradation mechanisms, we try to show an insight into the degradation in physical level, which can be served for the degradation modeling of the semiconductors, and also for the following EMR analysis of ICs.

III.3.1.1. **Hot Carrier** injection

Hot carrier injection is a phenomenon occurring in solid-state electronic device. When electrons or holes obtain sufficient kinetic energy, they will be able to pass through a potential barrier existing between the silicon substrate and the gate oxide film. Here, the term "hot" means the effective temperature used for carrier density modeling, rather than the temperature of the device itself. Because of the interface trap of the hot carriers in the gate dielectric layer of a MOSFET, the transistor

performances, like several important transistor parameters, can be permanently changed over a period of time.

Table III-1 Oxide defects based degradation mechanism description and impact

	HCI	TDDB	NBTI
Origin	High kinetic energy carrier induced interface trap and fixed oxide charge generation	Formation a conducting path through gate to substrate	Bias induced interface trap and fixed oxide charge creation
Transistor type	Primarily on NMOS	NMOS/PMOS	Primarily on PMOS
Accelerated conditions	High V_{DS} Low temperature	High absolute V_{GS} High temperature	High absolute V_{GS} High temperature
Activation energy	-1.0eV	0.7eV	0.4eV
Recovery	no	no	yes
Threshold voltage ($\|V_{TH}\|$)	↑	↑	↑
Transconductance (Gm)	↓	↓	↓
Mobility (μ)	↓	↓	↓
Gate oxide capacitance (Cgs/Cgd)	↓	↓	↑
Channel resistance (Rds)	↑	--	↑
Drain saturation current (Idsat)	↓	↓	↓
Transistor linear current (Idlin)	↓	↓	↓
Other	Substrate current (Ib) ↑	Gate leakage current (Ig) ↑ Input impedance ↓	Channel off current (Ioff) ↑

The hot carrier injection is usually caused by a high electric field. Compared to the energy needed for electrons (about 3.2 eV), holes require more energy (4.7 eV) to overcome the potential energy barrier [WHIT08]. As a result, the effect of HCI is more usual for N-channel MOSFETs which channel contains rather electrons. Nevertheless, with the reduced size of the semiconductor, the P-channel MOSFET becomes also sensible for this kind of degradation [ROSA97], [CHAP00]. The HCI mechanisms for these two transistor types are similar. Here we use n-channel MOSFETs as the example to explain the HCI mechanism.

According to the different voltage condition applied in the MOSFET terminals, there are four distinguished injection mechanisms for the injection of hot carriers into the dielectric: Drain avalanche

hot carrier (DAHC) injection, Channel hot electron (CHE) injection, Secondary generated hot electron (SGHE) injection and Substrate hot electron (SHE) injection. Although these injection mechanisms of carriers are not the same, but in most situations, more than one injection mechanisms occur at the same time. Among all injection mechanisms, DAHC induces the worst device degradation in the normal operating temperature range [ENTN07]. Figure III-5 illustrates the injection mechanisms DAHC. This injection is significant with a high drain voltage (V_{ds}) and a low gate voltage (V_{gs}). The electron-hole pairs gain enough energy due to a high electric field in the drain region to overcome the Si/SiO2 barrier. The carriers are injected into the oxide, while some holes flow back to the bulk substrate, forming the substrate current I_b.

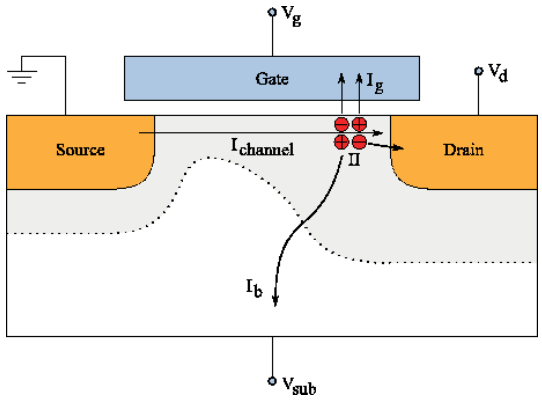


Figure III-5 DAHC injection mechanism for an N-channel MOSFET [ENTN07]

The effects of HCI are enhanced at low temperature, as in this condition the activation energy is negative (around -1eV). The results in [TAKE95] revealed that the substrate current at 77K is five times greater than that at room temperature. So the aging test LTOL of low temperature is intended to look for failures caused by hot carriers. Besides, the operating voltage has great impact on hot carrier effect. The degradation strongly depends on the electric field level in the MOS transistor, which directly relates to the operating voltage. Typically, for a defined drain voltage, we should choose a gate voltage to have the maximum substrate current in HCI aging test, as shown in Figure III-6.

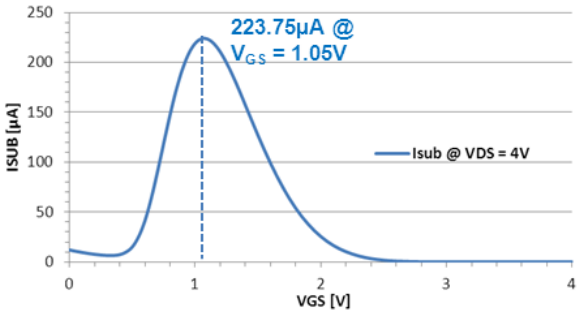


Figure III-6 Choice of V_{GS} to obtain maximum I_{SUB} of a NMOS in technology 90 nm of thin oxide [LI11]

As resumed in Table III-1, the direct results of degradation could be demonstrated by several transistor parameters drifts. The variation of main parameters degradation with stress time is widely

studied, like the increase of threshold voltage V_{TH}, the decrease of transconductance G_m due to mobility decrease and the drifts of gate parasitic capacitances [SAGO09]. In [TAKE83b], the evolution of threshold voltage with aging time is proposed by:

$$\Delta V_{th} = At^{n} \qquad \text{Equation III-9}$$

Here the threshold voltage shift ΔV_{TH} is resumed as a power law expression with two coefficients A and n. As shown in Figure III-7, this expression is based on the experimental data. It suggests that the magnitude of degradation A is strongly dependent on V_D, and the value n changes according to the hot carrier injection mechanism, i.e. this value depends on the aging conditions (voltage, temperature, etc.).

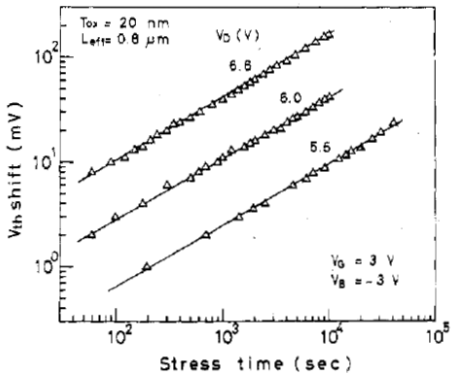


Figure III-7 Device degradations in V_{TH} as a function of stress time and drain voltage [TAKE83b]

This approximate power law expression is particularly valid for short stress times, while for long stress times, the parameters of transistors begin to saturate. It has been validated also for some other parameters like transconductance, saturation current and mobility, by several following studies of other different MOSFET technologies like in [BRAV05], [CHEN09], [LI11] and [WANG15]. However, as this power law expression is based on the experimental data, the more precise model based on the complex physical degradation analysis is needed [WANG11].

III.3.1.2. Time dependent dielectric breakdown

Time dependent dielectric breakdown (TDDB) is the second common reliability concern for semiconductors. It is caused by the formation of a conducting path through the gate oxide between the channel and the substrate due to electron tunneling current. This degradation is not an immediate breakdown which could be induced by a strong electric field applied in the gate oxide, for example under the condition of ESD. The gate oxide dielectric material has maximum electric field strength (known as *dielectric strength*). When the electric field in the gate oxide is below the maximum dielectric strength, the material could withstand intrinsically without immediate breakdown. However after a long-time application of a relative low electric field (for example 3 MV/cm), the TDDB degradation

can be excited, the dielectric gate layer can wear out after long term application and finally break down completely [SANYO].

The dielectric strength is defined by the applied voltage (or current), and it is directly proportional to the thickness of the layer and inversely proportional to the operation temperature, switching frequency and humidity. All these operating conditions could affect the TDDB failure process. Moreover, for PMOS the oxide breakdown speed is much slower than that of NMOS, so the TDDB mechanism is more discussed in NMOS [KACZ02a].

As shown in Figure III-8, the TDDB failure mechanism occurs in two stages [CHEN85] [WANG07]. The first stage may last for a long time. The localized holes and bulk electrons are trapped within the gate oxide and at the Si/SiO2 interface, so the gate oxide is slowly damaged and degraded and percolation paths are created with the increase density of trapped holes and electrons. The second stage begins with the creation of percolation path. In this stage, one or two types of failure may occur. At the beginning these conductive paths might disappear after an initial injection high current density which generates high temperature that could relocate some of the oxide traps and, break the conduction path and create other conductive path. The result may be a soft breakdown (SBD) i.e. the device continues to function with a small change of voltage or current after breakdown. And then when the gate leakage reaches a critical threshold, the breakdown evolves into the hard breakdown (HDB) which has a catastrophe level of leakage current through the oxide, which means an ohmic short circuit current across the gate [ALAM02a]. However, for the transistor with thin oxide or under low operation voltage, the hard breakdown is not easy to be triggered. According to [ALAM00], the probability of HBD is negligible if the operation voltage is under 1V.

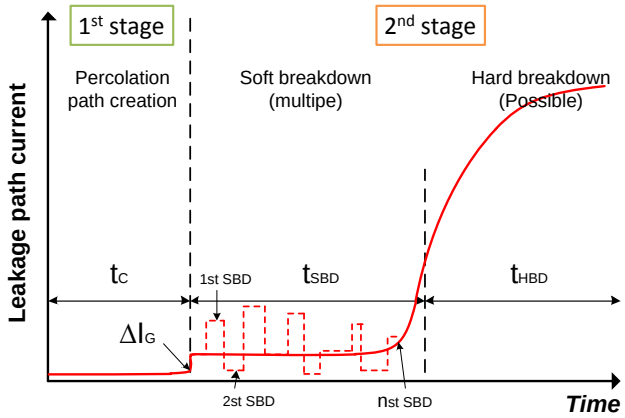


Figure III-8 Two stages of breakdown in thin oxide transistor [KAZC04]

The transistor could be suffered multiple SBD, and the cumulative failure could attain 20% variation of threshold voltage. The absolute threshold voltage increase 75mV from its origin value 0.3V in [HAGG06]. Transconductance and mobility follow the same trends. They decrease up to 30% after multiple SBD [LI01]. Another result is a drain current decreases about 10% after multiple SBD

[HAGG06] [LI01]. When the degradation mechanism passes to HBD, transistor gate loses its isolation and ability to control the channel current, thus accompanying with the decrease of the gate resistance, the drain current and gate capacitance. The increasing of traps around percolation path made more degradation on V_{TH} and G_m [POMP99].

III.3.1.3. Negative bias temperature instability

The Bias Temperature Instability (BTI) is a degradation problem for MOSFETs, which has been studied since the 1960s. In the recent year, gate electric fields have largely increased with transistor dimension, buried channel technology is replaced by surface channel, and chip operating temperature increases. All these reasons make BTI as a widely concern issue in IC reliability.

In the BTI issue, the most discussed is the Negative bias temperature instability (NBTI) for PMOS. This degradation could be produced by either negative gate voltage or elevated temperature, and the combination of the conditions lead to a stronger and faster effect. The typical stress conditions for NBTI is 100 to 250 °C and the oxide electric fields are above 6 MV/cm. Although NBTI is one common reliability issue for semiconductor, its mechanism is not fully understood. However, it's widely accepted that NBTI is controlled by the electro-chemical reaction. Under the condition of NBTI, either at the Si/SiO2 interface or in the gate oxide layer positive charge accumulates, which is the source of the change of the transistor parameters [MAHA04] [ENTN07].

The most impacted transistor parameter is the increasing absolute value of the threshold voltage, which is also widely studied. As resumed in Table III-1, the transistor performance like threshold voltage, mobility, transconductance, drain current are all degraded. One example of the V_{TH} shift is shown in Figure III-9. Like the HCI degradation, according to experimental measurement results under different aging stress conditions, the V_{TH} shift is also time-dependent and follows a power law as described in Equation III-9. However, as resumed in [BERN06], the degradation of V_{TH} can be expressed by other forms as Logarithmic time dependence or Exponential time dependence according to the applications.

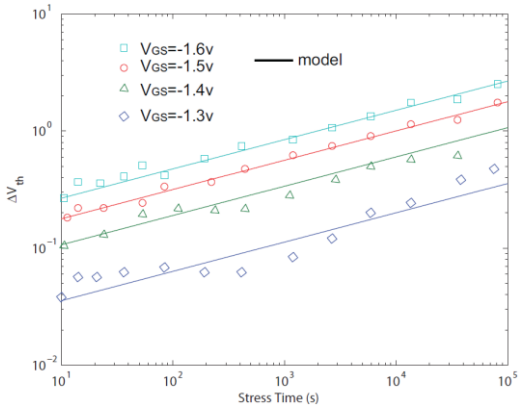


Figure III-9 V_{TH} shift vs. NBTI stress time [WANG11]

This temperature dependence of NBTI follows the Arrhenius law with activation energies ranging from 0.18V to 0.84V [LI11]. There are some other time dependence equations to express the transistor parameters evolution with aging time during the degradation process, like exponential time dependence or logarithmic time dependence. However, the power law time dependence has the most observed features and is widely accepted [BERN06].

Another important phenomenon of NBTI is the saturation and recovery, as shown in Figure III-10. The saturation is caused by the limitation of physical parameter shift, and the recovery could be produced by a positive gate voltage [SCHR06]. The recovery phenomenon exists also in the HCI degradation [BRAV05]. However, since the recovery phenomenon occurs usually after long stress times, it is not taken into account in the study of this thesis.

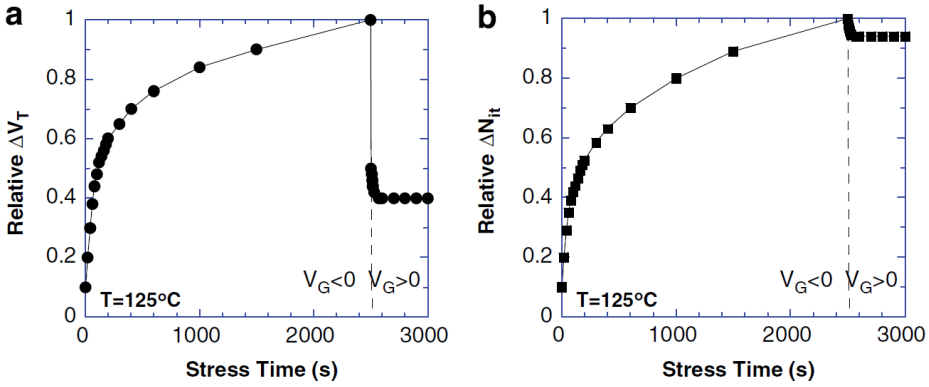


Figure III-10 **Saturation and recovery phenomenon of NBTI for two parameters: threshold voltage (a) and interface traps charge (b)**

III.3.2. Degradation characterization of transistors

As presented above, various degradation mechanisms occur under different aging conditions. The typical experimental voltage aging conditions for the CMOS technology around 0.25 µm are resumed in the Table III-2 [SCHR06] [LI11]. In this table V_{DDMAX} is the recommended maximum power supply voltage, and $V_{DSTRESS}$ is a stress voltage on drain which is between V_{DDMAX} and oxide breakdown voltage V_{BD}. Besides, the thermal aging conditions could be also applied in the degradation analysis of transistors. For example, the low temperature aging test LTOL is widely applied to analyze the HCI degradation, and TDDB and NBTI could be accelerated by high temperature. In order to simplify the experimental set-up, only the electrical aging factor is discussed in this study.

Although the stress aging conditions are defined, in real applications the degradation mechanisms are always mixed and applied in parallel. Generally, HCI and TDDB are the dominant degradation mechanisms for NMOS, while TDDB and NBTI are more important for PMOS. In this section, the characterization methods of two degradation mechanisms, HCI on NMOS and NBTI on PMOS, are selected. Then, the extraction methods of several important transistor parameters are also discussed.

Table III-2 Voltage stress conditions for HCI, TDDB and NBTI degradation

Degradation mechanism	N-channel MOSFET	P-channel MOSFET
HCI	• Normally, V_{GS} where the substrate current is maximum • For technology below 0.25 µm, V_G=$V_{DSTRESS}$	
TDDB	Constant high gate voltage compares to bulk potential |VG|>V_{DDMAX}	
NBTI		Negative gate bias stress compares to source |V_{GS}|>V_{DDMAX}

III.3.2.1. Characterization of HCI on NMOS

As presented in 4.1, the degradation mechanism of HCI is provoked by the strong electric field near the drain region. The stress condition used to activate HCI in NMOS transistor is demonstrated in Figure III-11 (a).

The drain stress voltage $V_{DSTRESS}$ is a value between V_{DDMAX} and oxide breakdown voltage V_{BD}. When $V_{DSTRESS}$ is fixed, V_G should be adjusted to obtain a maximum bulk current. This substrate current could be measured by a precise ampere meter. Besides, the source and bulk terminals are connected to the ground. The MOSFET I_{DS} vs. V_{DS} curves are measured during the stress process. As shown in Figure III-11 (b), as a result of HCI degradation, the drain current I_{DS} decreases along the aging time.

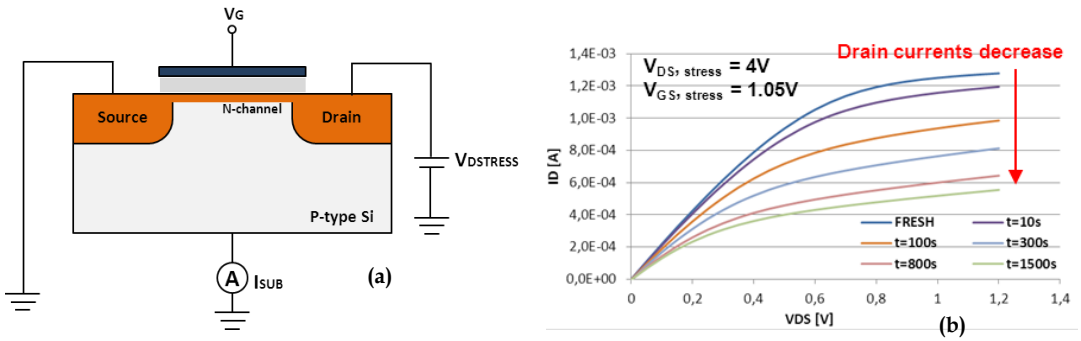


Figure III-11 NMOS HCI test method: (a) Experimental stress condition for NMOS HCI test, (b) IDS vs. VDS curve evolution due to HCI degradation [LI11]

III.3.2.2. Characterization of NBTI on PMOS

NBTI of PMOS is excited by a negative gate bias voltage, in particular at elevated temperature. A fast NBTI evaluation method (fast ΔI_D method) is proposed in [KACZ05], as demonstrated in Figure III-12.

Here the small drain-source voltage V_{DS} (typically -0.05V) keeps unchanged to ensure that the stress voltage across the gate dielectric is almost the same, and I_D vs. V_G curve is measured only up to

the gate voltage (Figure III-12 (a)). For the initial state of PMOS, we measure the initial V_{TH} and the corresponding source current I_{D0}, and we define this initial V_{TH} as the gate voltage value $V_{G.MEAS}$ during the measurement. The first blue point is the initial characterization (Figure III-12 (b)). After a short time of stress, the new value of drain current I_{D1} is measured with the same $V_{G.MEAS}$ (the second blue point). Due to the NBTI degradation, the drain current decreases, that means $I_{D1} < I_{D0}$. For this I_{D1} we can find a corresponding voltage in the initial I_D vs. V_G curve, and we call this voltage $V_{G.CALC}$. In the fast NBTI method, the approximate variation of V_{TH} (ΔV_{TH}) could be calculated by:

$$\Delta V_{TH} \approx V_{G.MEAS} - V_{G.CALC} \qquad \text{Equation III-10}$$

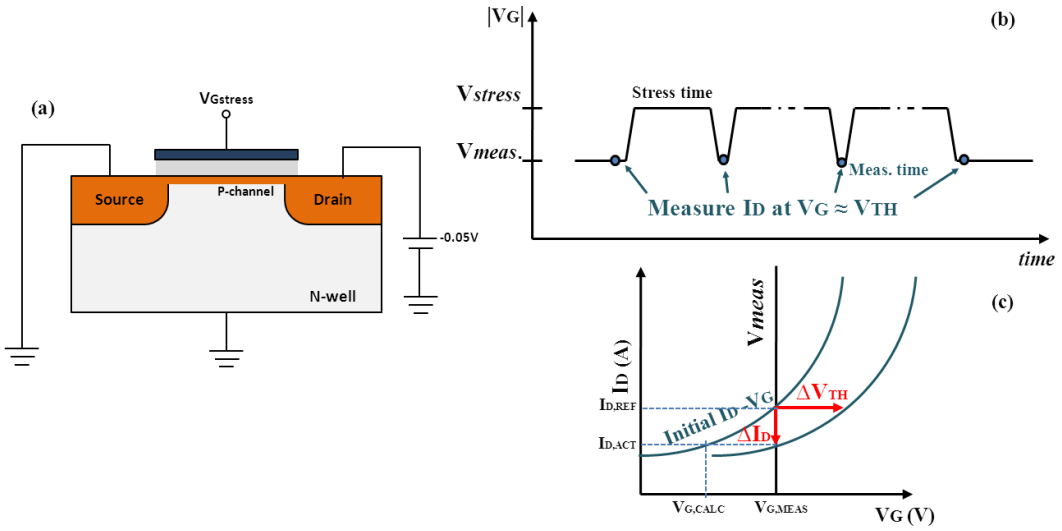


Figure III-12 PMOS NBTI fast ΔID method: (a) Experimental stress condition for PMOS NBTI test, (b) Stress and measurement gate voltage during the fast ΔID method, (c) IDS vs. VG curve for ΔV_{TH} calculation [LI11]

According to the former study, the increasing threshold value obtained by this fast NBTI method has a good approximation within 1 mV of the real V_{TH}.

III.3.2.3. Parameter extraction: Threshold voltage

The threshold voltage is a fundamental electrical parameter for the transistor modeling and characterization, and it is susceptible to degradations related to aging. So the precise extraction method of threshold voltage is required. The most accepted extraction method for threshold voltage is the Extrapolation of the Linear Region (ELR) method [ORTI02]. The ideal situation is to find the gate-voltage axis intercept (i.e., I_D=0) of the linear extrapolation of the ID-Vg curve at its maximum derivation point (i.e., point of maximum transconductance gm), as illustrated in Figure III-13. However, the main drawback of ELR method is the maximum slope point is not always easy to define, and the method can be strongly influenced by parasitic series resistances and mobility degradation effects.

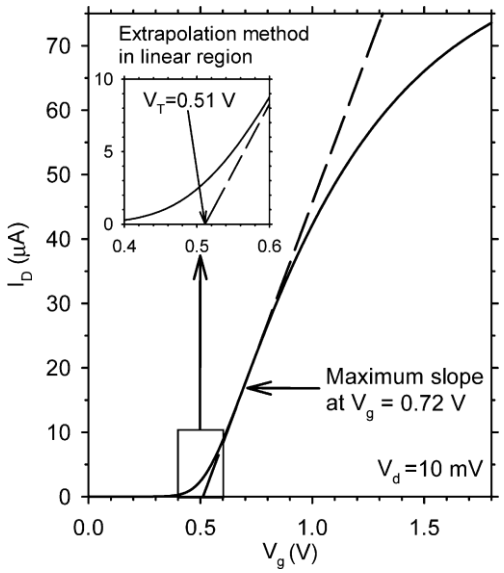


Figure III-13 ELR method implemented on the ID–Vg characteristics of the test bulk device [ORTI02]

There exist various other methods to extract threshold voltage, like constant current method where the MOSFET is biased in the linear region, and the extrapolation in the saturation region method where the transistor is biased in saturation region. More than ten V_{TH} extraction methods are resumed in [ORTI02], and we could choose the correct method according to the application and the test transistors.

III.3.3. Modeling of transistor aging

In order to evaluate the circuit performance and reliability under the degradation mechanism, the degradation models are required to simulate the degradation impact on circuit performance. A lot of transistor models are proposed for the different degradation mechanisms. With these degradation models, the value of the transistor parameters which are affected by the degradation mechanisms could be predicted accurately. Furthermore, these models can be incorporated into the global circuit simulation such as SPICE, to analyze and predict the evolution of circuit performances, which include the EMC level (emission and susceptibility) at any given time.

The first modeling method is the failure mechanism equivalent models. These models are always constructed based on the degradation physical mechanisms and the transistor parameters variation caused by degradation. In these models, the underlying concept of the circuit models is modeling degradation of device parameters with some additional lumped circuit elements (resistors, transistors or dependent current sources, etc.) to capture the level of a damaged MOSFET in circuit operation environment. The values of these additional lumped elements are determined by device wearout parameters which are time dependent. There are several successful transistor degradation equivalent circuit models which are proposed in the former studies, some of them have been embedded into commercial reliability simulation tools [BERN06] [WHIT08].

Another kind of modeling method focuses on the evolution of parameters with aging time in the chosen transistor SPICE models (like SPICE level 3 model, Nth power law model and BSIM models). This method is rather based on the experimental measurement results. The method for the extraction of the degradation parameters of transistors under aging condition are presented in the second part. In comparing with the failure mechanism equivalent models, this method does not require the precise physical analysis of the degradation mechanisms, but focuses rather on the variation of the parameters of transistor models with time. In practice, under stress conditions, several degradation mechanisms might coexist, the extraction of correct equivalent circuit models becomes relatively complex, but the transistor SPICE models could be a good choice.

III.3.3.1. Transistor equivalent circuit models

In this section, several examples of failure mechanism equivalent models are briefly presented. According to the degradation type and the application, we can choose the correct model in the simulation. The detailed extraction methods are not detailed in this section, and they can be found in the references of each model.

- HCI degradation models

One equivalent model of HCI degradation is called BERT (Berkeley Reliability Tools) model. It models directly n-MOSFET hot carrier damage in drain current degradation. As shown in Figure III-14, here the HCI-induced interface traps ΔN_{it} is illustrated as the source of the HCI degradation, so the drain current degradation is the direct results from channel mobility degradation. Lf and Lr represent forward and reverse hot carrier damaged regions.

The model BERT is illustrated in Figure III-14 (b), the variation of drain current ΔId is implemented as an asymmetrical voltage controlled current source in parallel with the original NMOS, it considers that the HCI mechanism occurs not only at drain terminal side but also at the source terminal side. The main contribution of BERT ΔId model is the ability to characterize bi-directional hot carrier stress effects. The detailed ΔId model equation and parameters are defined in former studies like [QUAD91]. However, this model requires extraction of six process parameters from device testing, which is a non-trivial work.

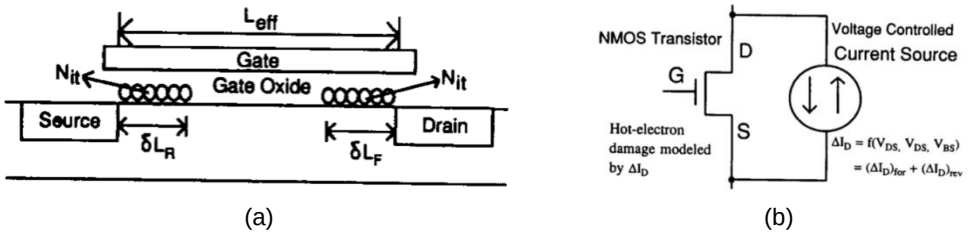


Figure III-14 Bidirectional mode interface trap generation near both drain and source (a) and BERT n-MOSFET HCI drain current ΔId circuit model (b) [QUAD91]

Another equivalent circuit model is the Hot Carrier Induced Series Resistance Enhancement Model (HISREM). This simple HCI failure equivalent circuit model, also named ΔR_d model, is based on the fact that the drain current decrease caused by interface trap generation near the drain end and can be modeled by the increase of HCI induced series drain resistance, this additional resistor also could account for the channel mobility reduction and threshold voltage drifts. The model is illustrated in Figure III-15. ΔR_d is a voltage dependent resistor in series with the original n-MOSFET. The ΔR_d is also dependent of the hot carrier induced interface trapped charge ΔN_{it} and oxide trapped charge ΔN_{ox}. These two charges ΔN_{it} and ΔN_{ox} are both time dependent. The detailed derivation of parameters can be found in the study of [HWAN95].

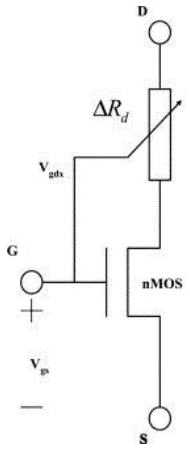


Figure III-15 HISREM HCI circuit model [BERN06]

- TDDB degradation models

One TDDB equivalent circuit model is proposed by [RODR03], which is called Power law leakage current model. In this model, the oxide soft-breakdown is modeled as a progressive wear out phenomenon. Nonlinear voltage-dependent current source, which is located between gate and drain or gate and source depending on the region of degradation, is used to model the oxide leakage current (Figure III-16 (a)).

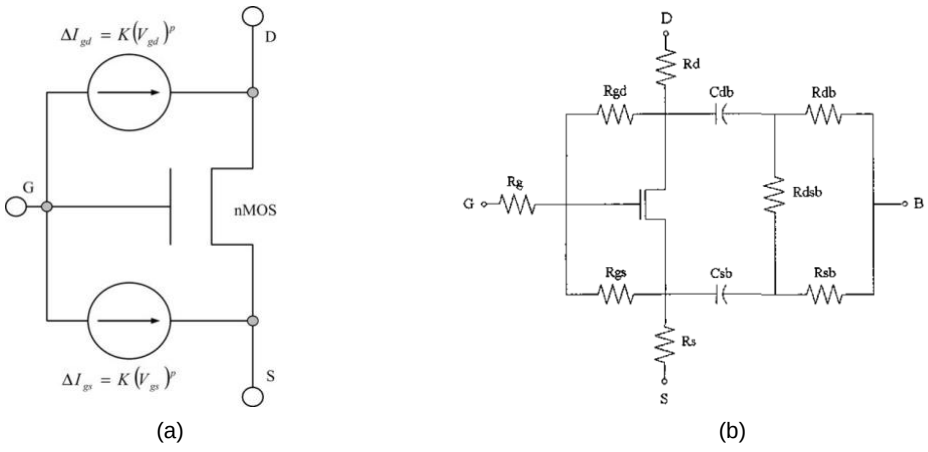


Figure III-16 Power law leakage current model (a) and RF failure circuit model (b) [BERN06] [YANG03]

Another RF failure circuit model is a model dedicated for RF application which is proposed by [YANG03]. As shown in Figure III-16 (b), some extra passive elements are added around the original NMOS transistor. Here R_{gd} and R_{gs} represent respectively the conducting paths from gate to drain and from gate to source. As a result, the gate-to-channel or gate-to-extension breakdown may be distinguished and modeled. Besides, R_g and the RC network between the drain, source and substrate are used to get an accurate RF modeling.

There are some other existing successful TDDB circuit models proposed in former studies, like GOS model and two transistors model mentioned in [BERN06] [WHIT08].

- NBTI degradation model

As discussed below, the main effect of NBTI on PMOS is the absolute value increase of threshold voltage. In this proposed model (Figure III-17), the threshold voltage increase is modeled as absolute gate-to-source voltage decrease. Gate tunneling current is modeled with two voltage controlled current sources I_{GD} and I_{GS}. These currents flowing through the gate resistance R_G leads to the increase of voltage at point G', which corresponds to the decrease of PMOS absolute gate-to-source voltage and therefore mimics the threshold voltage degradation effect [BERN06] [WHIT08]. A similar structure model could be constructed for PBTI on NMOS, except the reversed direction of current sources and the different model fitting parameters (threshold voltage and leakage current) [LEE04].

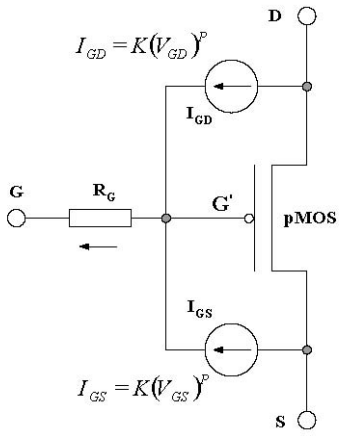


Figure III-17 NBTI circuit model [BERN06]

Although the equivalent circuit models have already provided successful simulation results, the drawback should also be considered. Firstly, the model construction needs a good knowledge of the transistor and the physical degradation mechanisms. Then the parameters' extraction in these models needs a large number of experimental data and complex calculations. Furthermore, the real operation of a MOSFET could meet more than one degradation mechanisms, so only one equivalent circuit model is hard to cover all degradation shifts.

III.3.3.2. Degradation modeling based on transistor models

The second way to demonstrate the transistor degradation is to take into account the degradation effects in the transistor SPICE models. That means the degradation impacts are expressed by the variation of certain parameters of the transistor models. The primary objective is also to transfer the stress effects from the device level to the circuit level, and to simulate the degradation influence during the design stage. In this section, three relatively simple transistor models, SPICE level-3 model, Nth power law model, and BSIM4 model are presented.

- SPICE level-3 model

A SPICE level-3 model module in the simulator software ADS is illustrated in Figure III-18. In comparison with the other common transistor models (like the BSIM models), SPICE level-3 model has less parameters, and the parameters could be easily extracted from current curve fitting. We can find in this model there are more than 60 parameters, but the adjusting of several main parameters (like V_{TH}, K_p, R_d, R_s, PHI and THETA) could provide a reasonable matching with the experimental I-V measurement [LI11].

LEVEL3_Model
Example

NMOS=yes	Cgdo=	Uo=	Trise=	Wmlt=
PMOS=no	Cgbo=	Vmax=	N=	Xw=
Idsmod=3	Rsh=	Xqc=	Tt=	Rdc=
Capmod=1	Cj=	Nlev=	Ffe=	Rsc=
Vto=	Mj=	Gdsnoi=1	Imax=	AllParams=
Kp=	Cjsw=	Kf=	Imelt=	
Gamma=	Mjsw=	Af=	wVsubfwd=	
Phi=	Js=	Fc=	wBvsub=	
Rd=	Tox=	Delta=	wBvg=	
Rs=	Nsub=	Theta=	wBvds=	
Cbd=	Nss=	Eta=	wIdsmax=	
Cbs=	Nfs=	Kappa=	wPmax=	
Is=	Tpg=	Rg=	Acm=	
Pb=	Xj=	Rds=	Hdif=	
Cgso=	Ld=	Tnom=	Ldif=	

Figure III-18 SPICE level 3 transistor model

In the study of LI [LI11], the degradation of HCI of a NMOS (W = 10 µm and L = 0.4 µm) is modeled by level-3 model under a HCI degradation conditions with a high substrate current for 1500 seconds. As shown in Figure III-19, the simulated I_{DS}-VDS curves fit well with the experimental measurement results, except some difference in linear region.

In this study, according to the comparison of the parameters of transistor models before and after aging, here the degradation could be simply simulated by the variation of three major parameters of level 3 model: V_{TH} (+56%), K_p (-19%) and R_d (+30%). To extract the evolution function f(t) of the parameters with time t (like the form of Equation III-9), the characterization of transistor's parameters at more precise aging phases are needed.

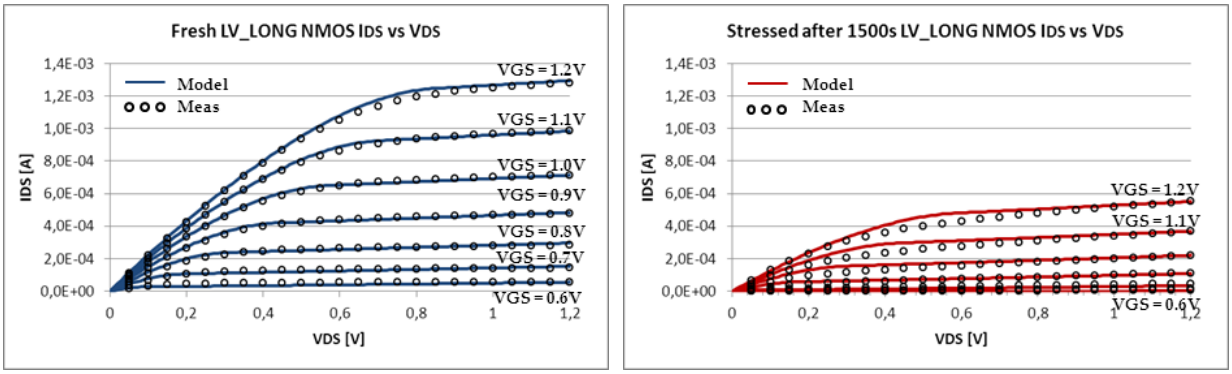


Figure III-19 Comparison of measurement and simulation with SPICE level 3: Fresh device (left) and device stressed after 1500s (right) [LI11]

- Nth power law model

In order to develop a simple model for short channel transistor, a simple model called Alpha-power law or N_{th} power law MOSFET model were proposed by Sakurai [SAKU90]. Although this model consists of only six main parameters, it could provide a good accuracy for short channel devices, especially in linear and saturation regions. The equations of the model are given below.

$$V_{DSAT} = K * (V_{GS} - V_{TH})^m \quad \text{Equation III-11}$$

$$I_{DSAT} = B * (V_{GS} - V_{TH})^n \quad \text{Equation III-12}$$

For $V_{GS} < V_{TH}$ (cut-off region):

$$I_{DS} = 0 \quad \text{Equation III-13}$$

For $V_{GS} >= V_{TH}$ and $V_{DS} < V_{DSAT}$ (triode region):

$$I_{DS} = I_{DSAT} * (1 + \lambda V_{DS}) * \left(2 - \frac{V_{DS}}{V_{DSAT}}\right) * \left(\frac{V_{DS}}{V_{DSAT}}\right) \quad \text{Equation III-14}$$

For $V_{GS} >= V_{TH}$ and $V_{DS} >= V_{DSAT}$ (saturation region):

$$I_{DS} = I_{DSAT} * (1 + \lambda V_{DS}) \quad \text{Equation III-15}$$

Where

V_{DSAT} and I_{DSAT} are the drain saturation voltage and the drain saturation current,

V_{GS} and V_{DS} are the gate-source and drain-source voltages,

V_{TH} is the threshold voltage,

K and m are two constants which control the linear region characteristics,

n is a constant which determines the saturated region characteristics,

B is a constant related to the transconductance,

λ is the finite drain conductance in the saturation region.

The six parameters in this model are V_{TH}, K, B, m, n and λ. The extraction of parameters can start with the selected 11 fitting points, which are used to solve the sub equations for each parameter [SAKU91]. These calculations could be applied with Matlab programs. Then, these parameters are provided to SPICE model for the simulation analysis. The previous measurements of HCI on NMOS are also simulated by Nth power law model. As shown in Figure III-20, the result demonstrates that the Nth power law model is able to reproduce the degradation impact on I_{DS} caused by HCI. The variation of six parameters is also significant: V_{TH} (+25%), K (-28.7%), B (-46.5%), m (-17.1%), n (+32%) and λ (+43%) [LI11].

Compared with SPICE level-3 model, the extraction of the parameters is much easier for Nth power law model, and the results in Figure III-20 demonstrate a better modeling fit with the measurement in the linear region. However, one important disadvantage of Nth power law model is the lack of physical sense for their parameters. Besides, the parameters extraction strongly depends on the selected 11 fitting points, which is a great limitation of this model.

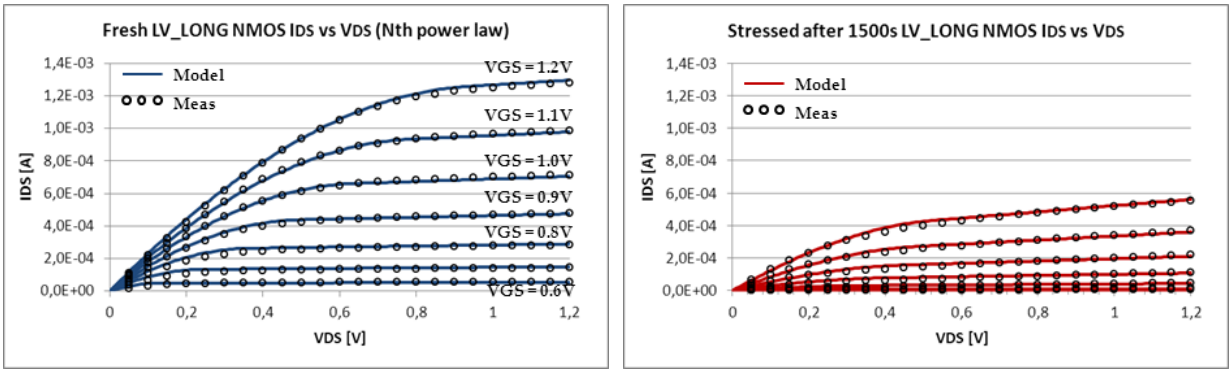
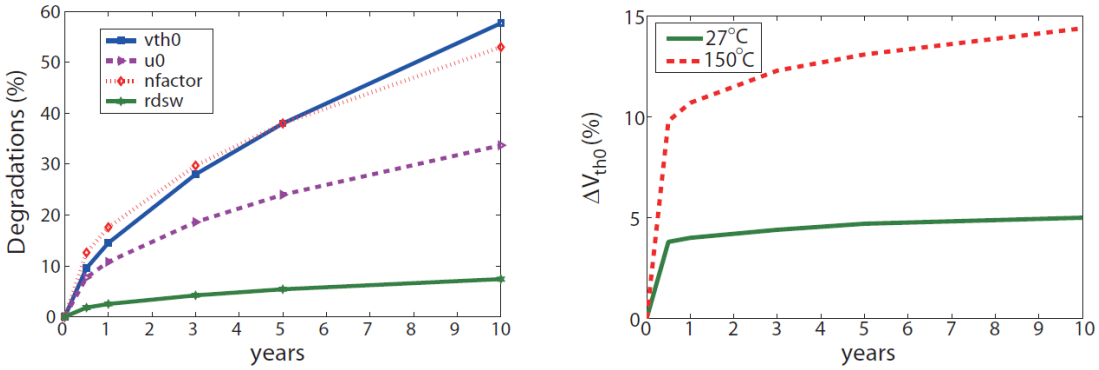


Figure III-20 Comparison of measurement and simulation with Nth power law: Fresh device (left) and device stressed after 1500s (right) [LI11]

- BSIM4 model

BSIM models are a physics-based and accurate MOSFET SPICE model for circuit simulation and CMOS technology development. They are developed by the BSIM Research Group in the Department of Electrical Engineering and Computer Sciences at the University of California, Berkeley. The BSIM4 model is based on the former BSIM3 model, which is designed for the MOSFET physical effects into sub-100nm regime, and it has been used for until 22/20nm technology nodes [BSIM] [PAYD13].

The latest version of BSIM4 model is v4.8.0 released in November 2013. This model is much complex than both models described above, and the total parameters is more than 800. According to the study in [CAI13], the main parameters affected by HCI and NBTI degradations are demonstrated in Figure III-21. These parameters are extracted from the matching with the experimental data and physical analysis. There are four main parameters of BSIM4 affected by HCI degradation, which contain intrinsic threshold voltage (V_{th0}), intrinsic mobility (μ_0), sub-threshold swing coefficient (n_{fac}) and drain source resistance per width (r_{dsw}). Besides, for the NBTI degradation, V_{th0} is the only affected main BSIM4 parameter of PMOS transistor. With a higher operating temperature (150°C), more V_{th0} variation induced by NBTI degradation could be observed in Figure III-21 (b).



(a) HCI effect to NMOS (b) NBTI effect to PMOS

Figure III-21 HCI and NBTI induced physical parameters degradation in NMOS and PMOS transistor [CAI13]

With the curves of the parameters' degradation extracted from the measurement, we can extract the time dependent functions for each parameter. Then with these functions, the aging impact on the transistors caused by the aging degradations could be simulated. In comparison with the SPICE level 3 model, BSIM4 model can provide a better accuracy for the IC technology less than 100nm. However, BSIM4 model is also much complex than SPICE level 3 model.

All these transistor degradation models presented above could be served in the model of global system for the simulation of the EMC evolution analysis. In our study, we select the relatively simple SPICE level 3 model as the transistor model in the EMR simulation, which could provide a satisfactory accuracy with the measurement results of both transistors and the system's EMC levels.

The work in [LI11] has provided several detailed modeling case studies of transistor's degradation, and the degradation models of transistors have demonstrated good fit with the experimental data. The IC test chips used in our study have the same technology as [LI11], so there is not a separated case study for the modeling of transistor aging, but as a part in the case study of EMR modeling of an operational amplifier in the next chapter. The modeling results demonstrate a good accuracy with the measurement data, and also confirm the degradation models constructed in [LI11].

III.4. Aging impact on passive devices and modeling

A passive device is normally a component that does not require energy to operate. A typical passive component would be a resistor, inductor, capacitor or transformer. Usually, the reliability study of passive component is more or less neglected in favor of the more "interesting" studies about active components. However, in an electronic system, passive components are integrated into printed circuit boards with all the other active devices and the EMC study is strongly related with the switching activity of the circuit, especially for the power electronics. So the passive components always play an important role (like filtering, decoupling or resonance) on the failure of electronic systems, also on their EMC levels. In the study of [LAHY98], among all electronic devices, the output filtering electrolytic capacitors of a switching mode power supply is highest probable source for system failure (Figure III-22). That is why the failure study of passive devices should be taken into account. In the following, several former studies about the reliability issues linked to passive electronic parts are detailed. Then, the characterization and modeling methods are presented.

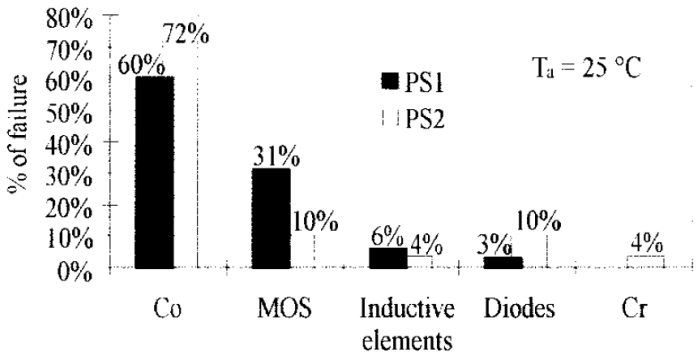


Figure III-22 Distribution of failure according to component type in a power application [LAHY98]

This section begins by some former aging degradation studies about several typical passive components, and then the characterization and modeling method of the degradation on passive components are presented.

III.4.1. Aging impact on passive components

III.4.1.1. Resistor

There are three main classes of resistors: Carbon composition resistors, Film resistors and Wirewound resistors. They are different from each other in size, cost, range of resistance value and power, etc. All resistors could be impacted by aging process, and the major influence of aging on resistors is a slight variation of the resistance value. This variation depends on temperature, humidity, and operating voltage. Especially the temperature plays an important role.

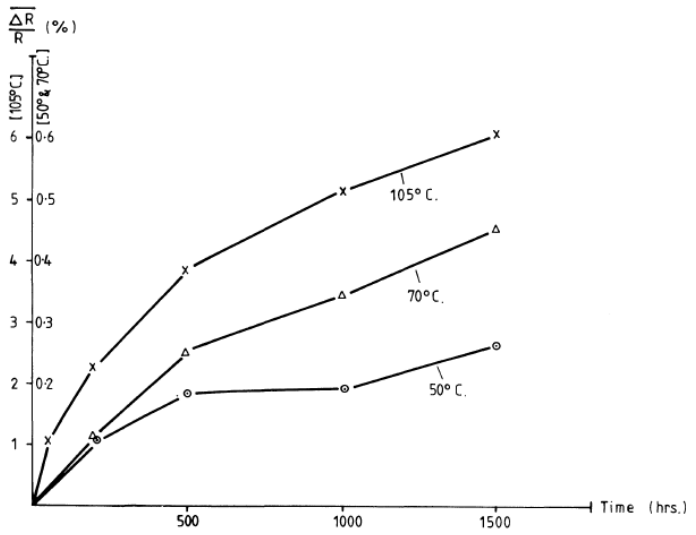


Figure III-23 Variation of resistance value of thick film resistors at different storage temperature [PRAN84]

An example of resistance variation of the same thick film resistors at three different storage temperatures is shown in Figure III-23. Normally, the resistance variation is much greater at the beginning. And in fact, after a long period of operation (about 5000 hours, which is called burn-in period), the variation of resistance becomes so small that the device could be considered as stable. The long-term stability of resistance value is usually specified by the term ppm/year (10^{-6}/year). For example, the typical value for metal film resistors is from 50 ppm/year to 70 ppm/year after burn-in [PRAN84] [BAJE10].

III.4.1.2. Capacitors

A typical capacitor is built from two electrodes isolated with dielectric materials, serving to store an electrical charge. There are a lot of types of capacitors, and their constitutive materials are very different, so the degradation mechanisms are not always the same. So the reliability performance is an important parameter for selecting the right capacitor for the right applications. In this section, several common capacitor types (aluminum, tantalum and ceramic) used in EMC studies are discussed.

- Aluminum electrolytic capacitor

An aluminum electrolytic capacitor is formed by an oxidized aluminum foil (anode and dielectric) and a conducting electrolyte (cathode) where a second aluminum foil is utilized as covering cathode layer (Figure III-24). This kind of capacitors has large loss factor which is dependent on the frequency and temperature. The lifetime is limited and they are not very reliable. So for a high operating temperature (more than 65 °C), the choice of capacitor is always ceramic capacitors [BAJE10].

There are already several works focused on the aging impact on a variety of capacitors. It is well known that aluminum electrolytic capacitors wear out under electrical or thermal stress condition. According to the former analysis of aluminum electrolytic capacitors, the vaporization of the

electrolyte accelerated by heat, and the degradation of electrolyte caused by ion exchange during charging/discharging are two major reasons of the degradation.

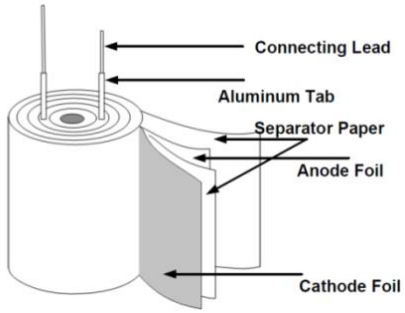


Figure III-24 Physical model of aluminum electrolytic capacitor [KULK12]

The degradation is usually caused by the temperature increase, not only under the thermal stress, but also the electrical stress. When the capacitor is operating under high temperature, the heat travels from the body surface to the core of the capacitor increasing the internal temperature. For the electrical stress, the flow of current during the charge/discharge cycle induces the rise of internal temperature in the core, and the heat is transmitted in the opposite direction to the surface of the capacitor body, but not all the heat can escape. No matter which stress type, the rise in the internal temperature during the aging process results in the vaporization of electrolyte, which could be measured by the decrease of electrolyte volume [KULK12]. The consequence of the degradation of aluminum capacitor is the drift of two important electrical parameters, the ESR increases after aging while the terminal capacitance decreases [LAHY98] [KULK12]. The examples of degradation parameter evolution are illustrated in Figure III-25.

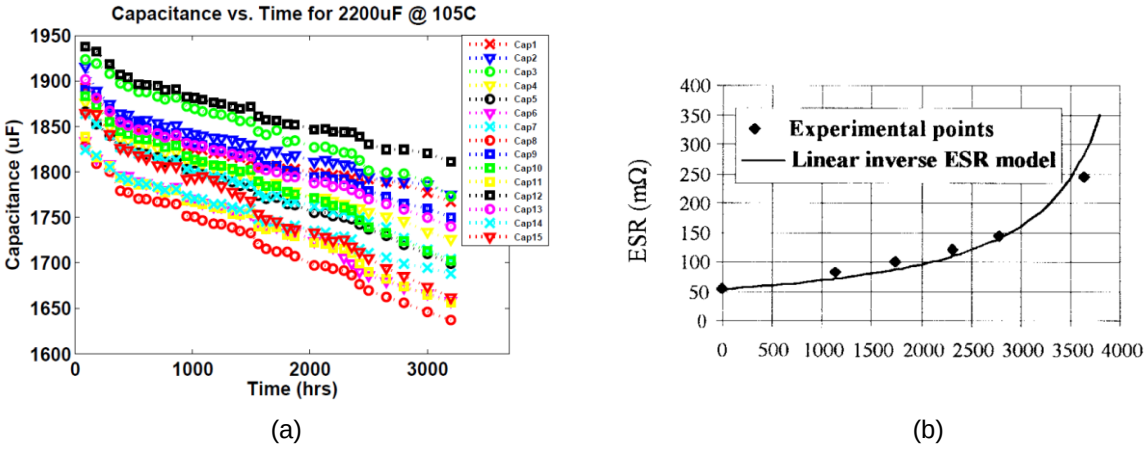


Figure III-25 Parameters' evolution of aluminum electronic capacitors with time: (a) Capacitance evolution [KULK12]; (b) ESR evolution [LAHY98]

The relationship between the ESR and the volume of electrolyte could be resumed by [GASP97]:

$$\frac{ESR(t)}{ESR(0)} = \left(\frac{V(0)}{V(t)}\right)^2$$ Equation III-16

Where

ESR (0) and ESR(t) are the initial ESR and the ESR at aging time t,

V(0) and V(t) are the initial electrolyte volume and the electrolyte volume at aging time t.

Normally, the variation of ESR is more significant than that of nominal capacitance C. The failure threshold of capacitance under storage conditions is 10 %, while that of ESR is around 280 – 300 % [KULK12].

- Tantalum electrolytic capacitor

In some studies, the term "electrolytic capacitor" is associated to aluminum capacitor. However, that is not really correct, because in total there are three major families of electrolytic capacitors, categorized according to their dielectric. Except aluminum capacitor, two others are tantalum electrolytic capacitor and niobium electrolytic capacitor. In comparison with aluminum capacitors, the tantalum capacitors are widely accepted more reliable. Until now, few works have discussed the wear-out processes for tantalum capacitors. Besides, with the other advantages like good temperature and frequency level and relatively reduced dimension, nowadays aluminum electrolytic capacitors are partially replaced by tantalum capacitors [BAJE10].

Failures of tantalum capacitors under steady-state conditions (at a temperature from 105 °C to 170 °C, voltages up to twice of the rated voltage) may occur as a sudden leakage current increase without significant degradation, and can be described as a time-dependent breakdown in anodic tantalum pentoxide films [TEVE09]. The study in [QAZI14] indicated that High-Leakage/Short Failures, High-ESR Failures and Low Capacitance/Open are three broad failure categories of tantalum capacitors. Besides, [HUAN11] demonstrated that leakage current (LC) and capacitance are two characteristics of tantalum capacitors which are changed under thermal aging conditions, because these two parameters are the most sensitive to defects and processes in the dielectric of capacitors.

However, in practice the measured variations caused by aging are usually very small, as shown by the experimental results in [HUAN11] (Figure III-26). The similar degradation results of different types of solid tantalum capacitors were provided in [TEVE07], except the LC and capacitance variation mentioned above, ESR and breakdown voltage are two other parameters impacted by temperature cycling aging.

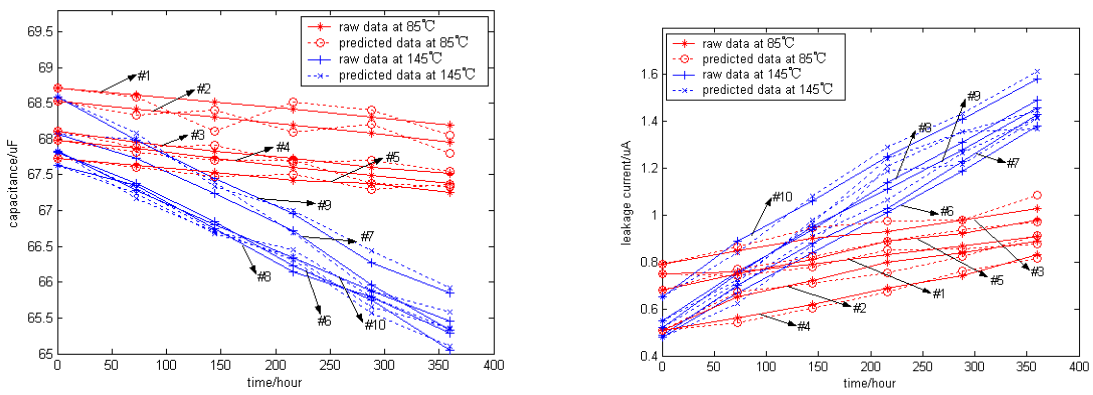


Figure III-26 Parameters evolution of tantalum capacitors with time: Capacitance (left) and Leakage current (right) [HUAN11]

- Ceramic capacitor

There are two main types of ceramic capacitors: fixed leaded disc capacitors and multilayer ceramic capacitors (MLCC). Ceramic capacitors, especially the MLCC, are the most produced and used capacitors in electronic products [HO10]. For the reason of their relatively small size and high reliability, surface-mount MLCCs are intensively used in circuit-card assemblies.

According to the standard IEC/EN 60384, ceramic capacitors are normally divided into three classes according to their volumetric efficiency and reliability level. The larger class means a higher volumetric efficiency and a lower reliability level. Class 1 ceramic capacitors offer high stability and low losses for resonant circuit applications. The study in the [OVER93] revealed that C0G ceramic capacitors of Class 1 experienced little change in capacitance as a function of thermal aging time. The discussion about the reliability is open for the other classes, for example for the type X7R, Y5V and Z5U in Class 2.

The dielectric constant of the material used in the capacitors determines the volumetric capacity. A major change observed in ceramic capacitor of high dielectric constant is the decrease of the capacitance value. As shown in Figure III-27, the effect of time imposes a predictable loss of capacitance in two Class 2 capacitors. This aging rate is expressed in decade hours.

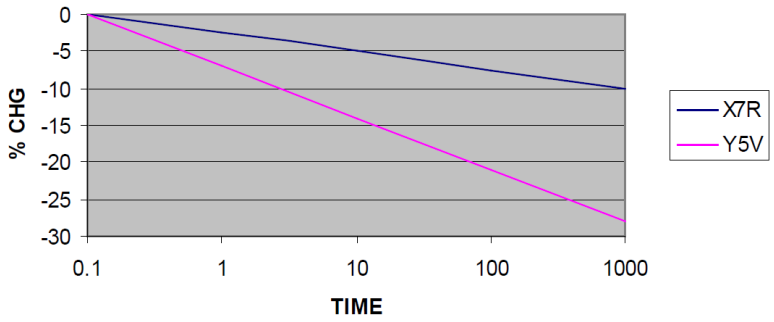


Figure III-27 Capacitance evolution of Class 2 ceramic capacitors [JOHA12]

We can find that in this result, the capacitance aging drift is illustrated per logarithmic decade of time. This can be resumed in the following capacitance aging law [KNOW]:

$$C(t) = C(0) \cdot (1 - k \cdot log(t)) \qquad \text{Equation III-17}$$

Where

C(t) is the capacitance at aging time t,

C(0) is the initial capacitance value before aging process,

k is the aging constant which depends strongly with the dielectric constant.

The following Table III-3 resumes the aging speed k of several typical ceramic capacitors.

Table III-3 Aging constant of typical ceramic capacitors [LAFO10]

Class of capacitor	Dielectric	Aging constant k
Class I	NPO (C0G)	<0.1%
Class II	X7R, X5R	1.5% - 4% per decade of hour
Class III	Y5V	7% per decade of hour

The aging mechanism is shown in Figure III-28. Over a period of time after the generation of spontaneous polarization, gradual spontaneous polarization is rearranged in a stable state. In the boundary layer, space charge domains are generated and they inhibit spontaneous polarization reversal. Since the dielectric constant is equivalent to the reversal of the spontaneous polarization per unit volume, if the number of domains with low-field reversal is reduced, the capacitance decreases.

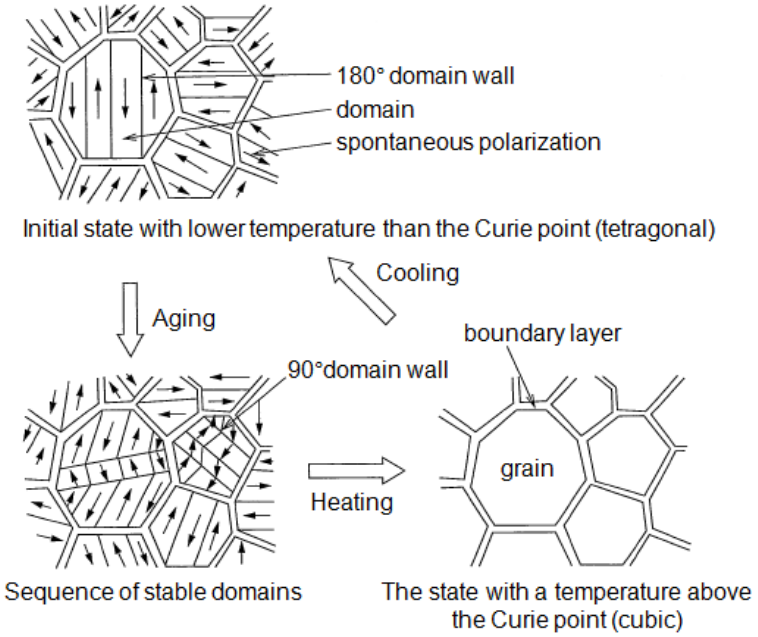


Figure III-28 Aging mechanism and reversing aging mechanism for the ceramic capacitor [MURA]

However, the aging process of the ceramic capacitors is reversible, by heating the devices above the Curie temperature (about 125°C) during a manufacturing process such as soldering. Normally exposure to 150 °C for 1.5 hours is sufficient. This mechanism is also revealed in Figure III-28. After the heating, the crystalline structure of the capacitor is returned to its original state and the original capacitance value could be observed. When the capacitor cools down below the Curie point, aging starts again [MURA] [JOHA12].

- Film capacitor

Plastic film capacitors usually present high RMS current, small capacitance variation regardless of applied voltage and good reliability. The aging impact on film capacitors is very small but still measurable. The degradation mechanism is related with the plastic film shrinkage, which could be induced by high ambient temperatures or high current load [MAKD15].

Similar aging impacts of aluminum capacitors were found in the aging study of Metallized Film Capacitors, the capacitance and ESR value are two major parameters impacted by the aging conditions. One example result is shown in Figure III-29.

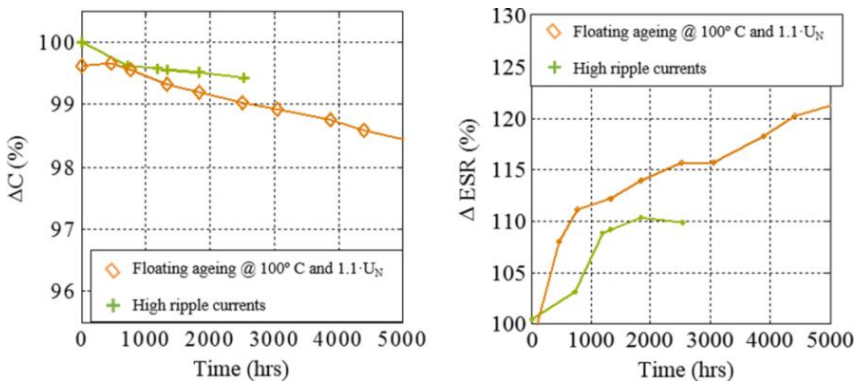


Figure III-29 Comparison of ESR and C evolution for a metallized film capacitor under two different aging conditions [MAKD15]

III.4.1.3. Inductor

An inductor is a passive electronic component that stores energy in the form of a magnetic field. It contains a conductor such as a wire, wound into a coil around a core. The inductors could be cataloged according to the different coil types. In comparing with capacitor and resistor, there is very little study about the aging impact on inductor, except some works about iron powder core inductors which are widely used in both DC and AC conditions in reason of their excellent inductance stability [JOHA13][MANZ][MICR].

Generally, iron powder cores use the organic material as binder, such as epoxy. The organic material is very susceptible to high temperature and the resin breakdown temperature is only about 125C° to 150C°. The former studies revealed that when the iron powder inductors are exposed to elevated temperatures for a long time, there is an increase of core losses for all iron powder cores. The

aging process is irreversible and the core losses increase with aging time, as shown in Figure III-30. Except the ambient temperature, other elements like self-heating, core volume and shape, operating frequency, peak AC flux density, material type and core manufacturer also have an influence to aging levels of inductors [MATE].

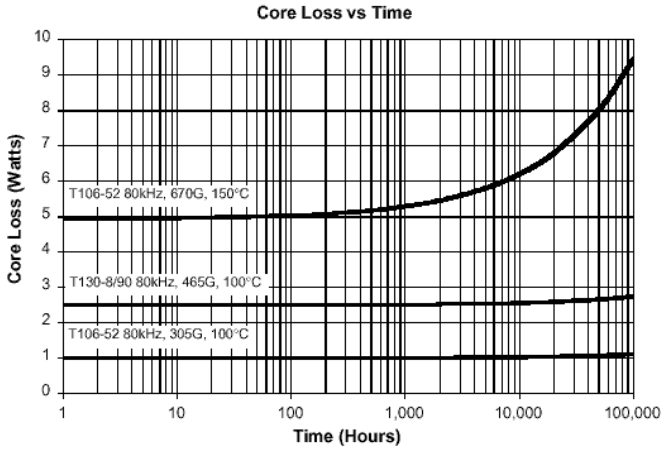


Figure III-30 Core loss evolution under different operating conditions (temperature, peak AC flux density) vs. aging time [MATE]

III.4.2. Aging characterization of passive devices

The degradation impact on passive devices could provoke a lot of drift of device performance, like the reliability or thermal characteristic. However, the most important performance related to EMC levels is the impedance, which presents the frequency response of each component and often the filtering quality in real applications. The impedance of a passive component demonstrates not only the basic value of this component, but also the parasitic elements which play an important role at high frequency for EMC levels. For example, the impedance of a capacitor contains not only the nominal capacitance value, but also the parasitic resistances and inductances, which relate strongly with the filtering performance of the capacitor.

As presented in [AGIL13], there are already many impedance measurements. The choice of measurement approach should consider several measurement factors, such as the frequency coverage, the measurement accuracy and the ease of operation. Considering only measurement accuracy and ease of operation, the auto-balancing bridge method is the best choice for measurements up to 110 MHz. For measurements from 100 MHz to 3 GHz, the RF I-V method has the best measurement capability, and from 300 kHz the network analysis is the recommended technique. In this study, as a widely applied method and available instrument, the network analysis method is presented.

Besides, the aging impact on passive devices could be provided directly by the impedance evolution with aging stress. The measurement of impedance during the aging process is also discussed in this section. In this study, we are interested only in the evolution of impedance under the nominal temperature and polarization. However, the passive components have a strong dependence

on the operating polarization and temperature. For reason of the simplification, they are not discussed in this study and not taken into account in the perdition study of EMC levels.

III.4.2.1. Network analysis method

Network analysis is the process of finding the voltages across, and the currents through, every component in the network. It is also widely used in the impedance measurement. Figure III-31 illustrates a typical two-port network. The two-port network could be characterized by a scattering matrix, as shown in Equation III-18. The matrix elements S_{11}, S_{12}, S_{21} and S_{22} are referred to as the scattering parameters or the S-parameters. The parameters S_{11} and S_{22} are reflection coefficients, and S_{21} and S_{12} are transmission coefficients.

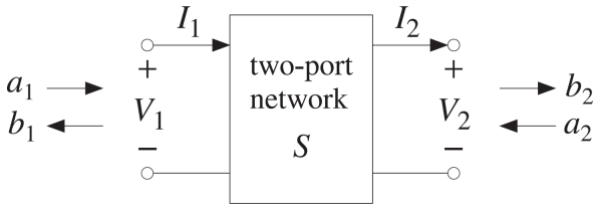


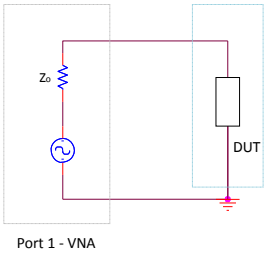
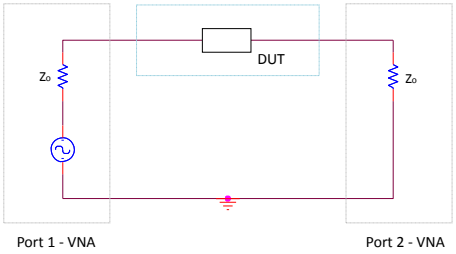
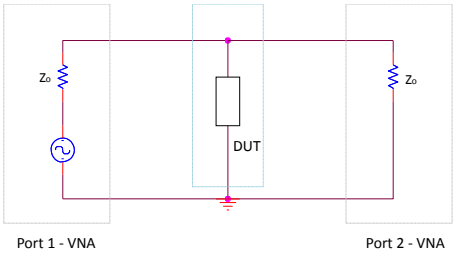
Figure III-31 Two-port network [ORFA08]

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \qquad \text{Equation III-18}$$

The network analyzer is an instrument which measures the network parameters. Network analyzers could be used at high frequencies, and nowadays some could cover up to more than 1 THz. There are two basic types of network analyzers: Scalar Network Analyzer (SNA) which measures amplitude properties only, and Vector Network Analyzer (VNA) which measures both amplitude and phase properties. VNAs are the most used, and sometimes a "network analyzer" means a VNA. To measure the impedance of a two terminal device, there are three possible configurations: one-port reflection coefficient method, two-port series-through network method and two-port shunt-through network method. The configuration of the three methods and the equations used to extract the device impedance are resumed in Table III-4.

The most important difference of these configurations is the level of uncertainty over the different impedance range, as shown in Figure III-32. For characterization of small impedance, like the ESR value of a capacitor which is always less than 10 Ω, the two-port shunt-through network method offers a better accuracy. And for the large impedance value, like the inductance value at high frequency, the first choice should be the two-port series-through network method.

Table III-4 Three configuration of impedance measurement by VNA

Method	Measurement configuration	Impedance $\underline{Z}$
One-port reflection coefficient method		$\underline{Z} = Z_o \frac{1+S_{11}}{1-S_{11}}$
Two-port series-through network method		$\underline{Z} = \frac{2 \cdot Z_o \cdot (1-S_{21})}{S_{21}}$
Two-port shunt-through network method		$\underline{Z} = \frac{Z_o \cdot S_{21}}{2 \cdot (1-S_{21})}$

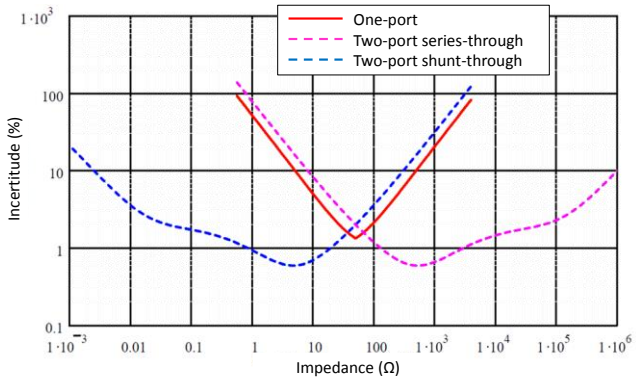


Figure III-32 Incertitude level of three impedance measurement configurations [LAFO10]

III.4.2.2. Impedance characterization during aging

An impedance measurement test bench with VNA and the Z probes is shown in Figure III-33. Here a dedicated impedance characterization test card is designed for certain forms of Surface-mount device (SMD) passive devices. For each form, this card provides three possible configurations. Before the characterization, the passive devices are soldered on this card. The soldering process should be fast and precise, to avoid the effect of high temperature on passive impedance.

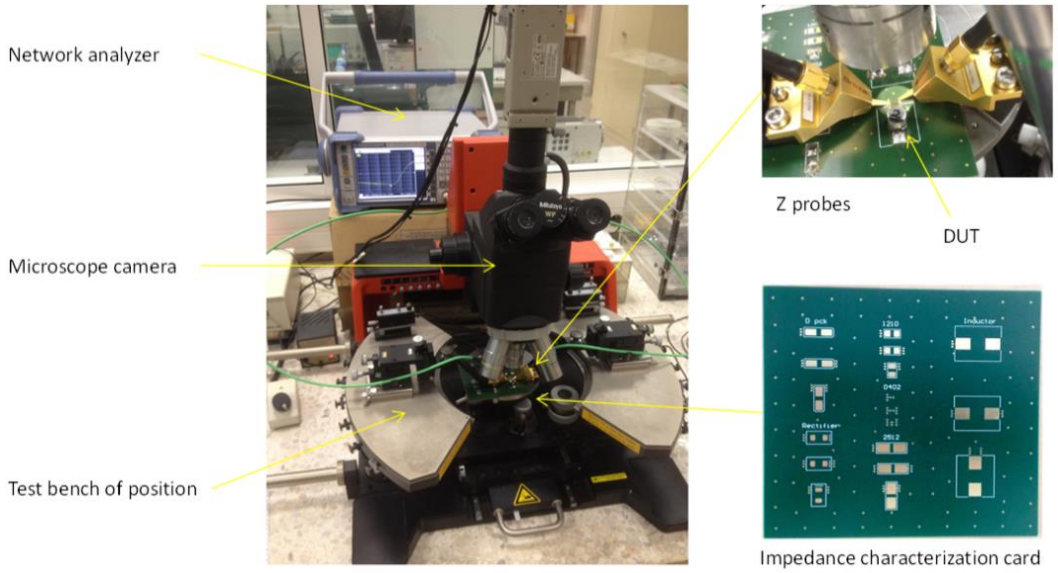


Figure III-33 Impedance measurement test bench by VNA

The aging impact on passive devices could be illustrated by the impedance measurement. The impedance characterization of passive devices during aging process requires stable measurement conditions and configurations over time. Hence, the measurement instrument, like VNA, should be calibrated each time before the impedance characterization. Besides, the VNA measurement could cover the impedance measurement in a large frequency range, especially at high frequency. So sometimes an accurate multimeter is used as a supplementary measurement method for the impedance characteristics at low frequency or DC impedance (resistance).

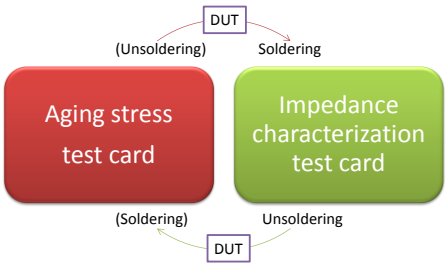


Figure III-34 Impedance characterization during aging process for passive devices

The main aging stresses for passive devices are thermal stress and electrical stress. Usually, the aging process and the impedance characterization of passive devices need additional test cards, and the test cards for these two processes are always not the same. As a result, the soldering and unsoldering are required between the two processes, as shown in Figure III-34. However if the aging stress is only high temperature thermal stress, the solder/unsoldering is not necessary for aging process as the extra power supply is not required.

III.4.3. Degradation modeling of passive devices

The impedance of three common passive devices (resistance, inductor and capacitor) at low frequency range could be simply modeled by purely a basic component, as shown in Figure III-35, where these models are presented ideally. However, in reality, especially for EMC studies, more accurate models of passive devices are required for a wide frequency range which includes high frequencies. As a result, the parasitic elements, like the effect of discrete component leads and skin effect, should be considered in the modeling of passive devices. In this section, the equivalent circuit models of three passive devices are discussed. Besides, the method to implement the aging impact in the circuit models is also presented in the end of this section.

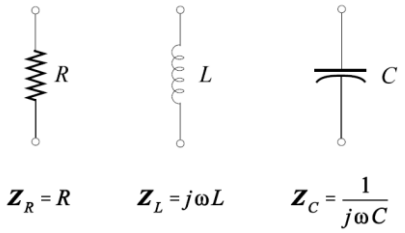


Figure III-35 Basic impedance model of passive devices

III.4.3.1. Equivalent circuit model of Resistor

According to the former studies, a commonly accepted simple model is illustrated in Figure III-36. In this model, R is the basic resistance of the component, the parallel parasitic capacitor C_p is due to the charge leakage along the resistor body and also the effect of leads, and the parasitic inductor L_s is mainly caused by the component leads.

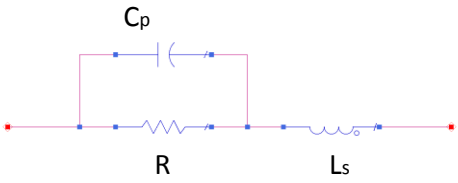


Figure III-36 Equivalent circuit model for resistor

The total impedance of the equivalent circuit is expressed by:

$$Z_{R.total} = \frac{j\omega L_s + R(1 - \omega^2 L_s C_p)}{j\omega R C_p + 1} \qquad \text{Equation III-19}$$

Sometimes this equivalent circuit model could be simplified according to the resistance value, especially for SMD film resistors. As shown in Figure III-37, for the parasitic elements, the resistors tend to have either a dominant shunt capacitance, or a serial inductance, depending on the resistor value. For small value resistors, the main parasitic element is L_s. In contrary, C_p becomes the main parasitic element for the large value resistors.

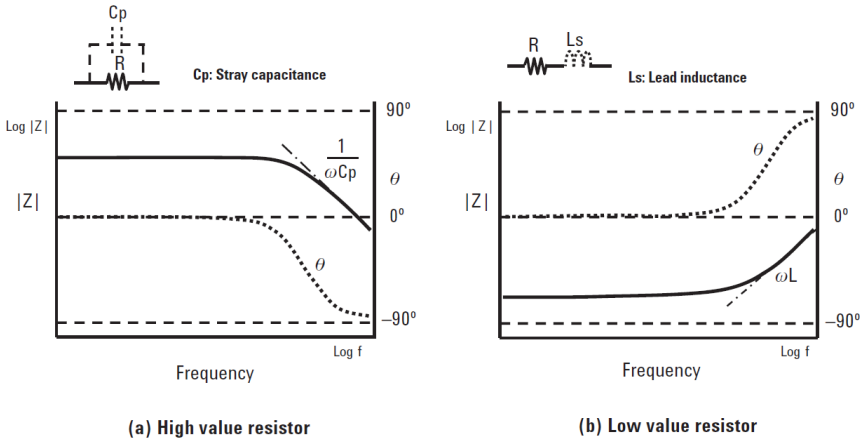


Figure III-37 Resistor frequency response and corresponding models [AGIL13]

Moreover, for the components in the same case size (e.g. 0201, 0603) from the same manufacturer, since the termination style, size and material are all the same, usually we can consider that the parasitic elements' value are identical, which means whatever the resistance value, the value of C_p and L_s are almost constant for the same resistor type [LAFO10] [VISH06]. A modeling example of 5 thin film resistors of same case size (0603) is shown in Figure III-38 . The DC resistance value (unity: Ω) of each resistor is indicated beside the curves. The equivalent circuit models of five resistors have the same parasitic value (C_p: 0.0403 pF, L_s: 0.0267 nH), just the DC resistance values are different (from 50 Ω to 1000 Ω). As illustrated in Figure III-38, the models demonstrate a good fit with the measured impedance, even in high frequency range.

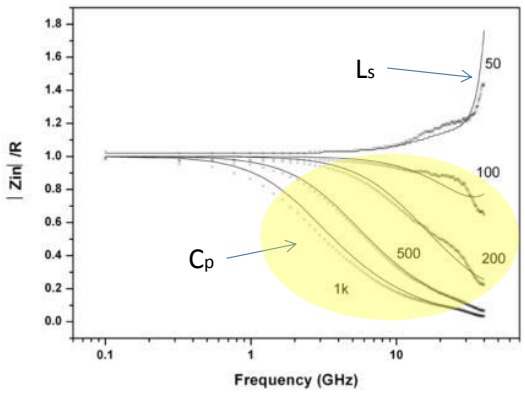


Figure III-38 Impedance measurement (dotted line) and modeling (solid line) of thin film chip resistors of different value [VISH06]

III.4.3.2. Equivalent circuit model of Capacitor

There are a lot of equivalent circuit models proposed for capacitor, the model illustrated in Figure III-39 (a) is an proposition which takes into account almost all important factors. In this model, C is the nominal capacitance. R_p in parallel represents the isolation and leakage resistance, which is generally not linear with the applied voltage. R_s and L_s in series, named Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL) respectively, are mainly created by the terminals and the plates

that constitute the capacitor. Normally, the resistive part ESR is the main source of self-heating. The last part of the model R_{da} and C_{da} are used to simulate the absorption phenomenon of the dielectric, which is the incomplete discharge effect of a capacitor when it's briefly discharged.

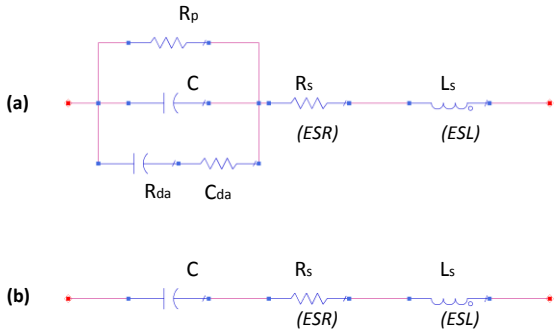


Figure III-39 Equivalent circuit models for capacitor: (a) complete model, (b) simplified model

In most case studies, including some EMC studies, a simplified equivalent circuit model is used, as shown in Figure III-39 (b). The parameters in this model could be obtained by impedance measurement. The total impedance associated with this simplified model is expressed in Equation III-20.

$$Z_{C.total} = R_s + j(\omega L_s - \frac{1}{\omega C}) \qquad \text{Equation III-20}$$

The typical frequency responses for capacitors are shown in Figure III-40. At low frequencies, the phase angle θ is around -90°, which means the impedance is almost purely capacitive. The absolute impedance value decreases until a self-resonant frequency (SRF), where is also the minimum impedance point. At the SRF, $Z_{C.total} = R_s$ and the phase is 0, which means the reactance value of $Z_{C.total}$ is zero, so we can calculate the self-resonant frequency by Equation III-21. At frequencies above the SRF, capacitors behave as inductive devices, so they cannot be used as a capacitor in this frequency range [AGIL13].

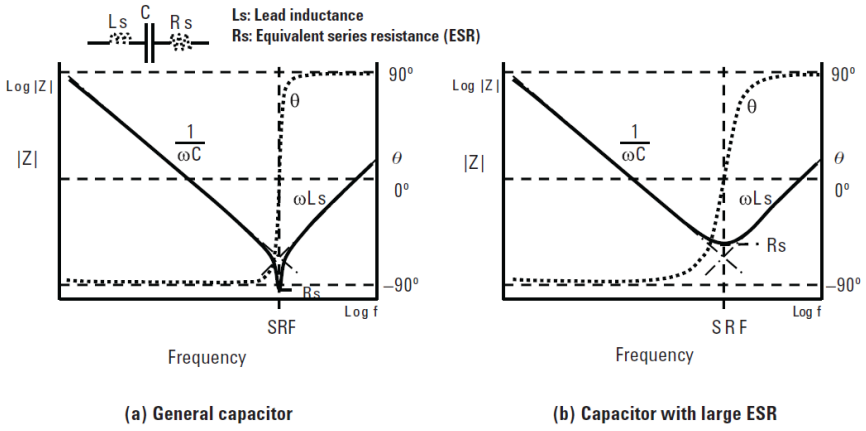


Figure III-40 Capacitor frequency response and corresponding models [AGIL13]

$$f_{SRF} = \frac{\omega_{SRF}}{2\pi} = \frac{\sqrt{\frac{1}{CL_s}}}{2\pi}$$ Equation III-21

In both cases shown in Figure III-40, the ESR value is simply defined by the minimum impedance value at SRF. However, the real ESR is much complex. Commonly, ESR can be extracted directly as the real part of the impedance, as shown in Figure III-41. Here the ESR is no more a constant, but a frequency-dependent resistance value.

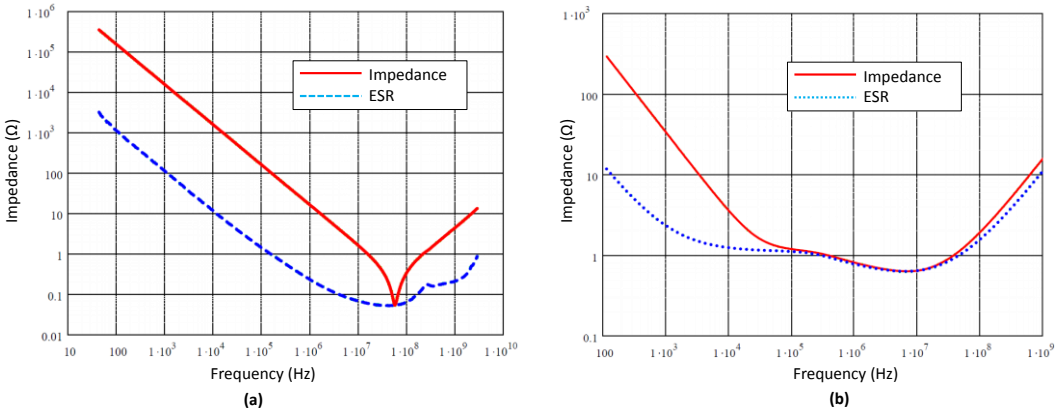


Figure III-41 Impedance and ESR of capacitors: (a) TDK 0603 X7R 10 nF, (b) KEMET tantalum capacitor 4.7 µF [LAFO10]

For a ceramic capacitor (Figure III-41 (a)), ESR decreases roughly according to 1/f in low frequency range, which is linked to the losses in the dielectric. For the frequency above SRF, ESR is mainly caused by the skin effect of ending and plates, and it increases with a $\sqrt{f}$ law [LAFO10]. However, to model the ceramic capacitor, commonly a simple resistance R_s is sufficient as the ESR value is very low. One modeling example is shown in Figure III-42. In this model, the ESR is presented by a single small value resistance (0.018 Ω). As illustrated in Figure III-43, the impedance modeling fit well with the measurement.

Figure III-42 Basic equivalent circuit model for a X7R ceramic capacitor 100 nF

Besides for the electrolytic capacitors, the ESR could be expressed by a combination of three resistors: R_1: Frequency-sensitive resistance as a result of oxide thickness; R_2: Temperature-sensitive resistance as a result of electrolyte; R_3: Resistance related to foil length, tabs, lead wires and ohmic contact resistance.

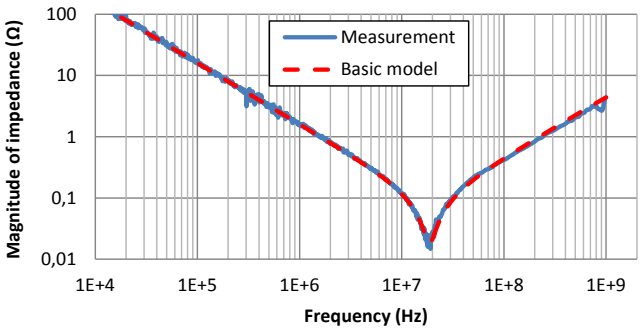


Figure III-43 Impedance measurement (solid line) and modeling (dotted line) of a X7R ceramic capacitor 100 nF

Because of the sensible characteristic of electrolyte to temperature (the part of R_2), the thermal effect to ESR is much important for electrolytic capacitors than for ceramic capacitors. For most electrolytic capacitor devices, the ESR declines significantly with the increasing temperature [LAFO10] [PERI04]. In some studies, like in [PERI04], the ESR variation with temperature is presented in the capacitor models. To simplify the work, the temperature influence to the devices is not considered in this study. However, it's a very important subject in real applications, and it should be taken into account in future studies.

Definitely, since the ESR varies with the frequency, the simplified model composed by only 3 elements in Figure III-39 (b) is not precise enough, especially for electrolytic capacitors which have a relatively large ESR. To model the frequency-dependent part of ESR, [GASP97] proposes additional resistor-capacitor pairs to achieve a better fit to both ESR and capacitance level. Figure III-44 illustrates a model example with a single resistor-capacitor pair. In this model, ESR is expressed by a combination of three passive elements. Here R_1 is the frequency-sensitive resistance which is in parallel with a dielectric loss capacitance C_1. R_2 and R_3 are all the other resistive factors which are not related with frequency.

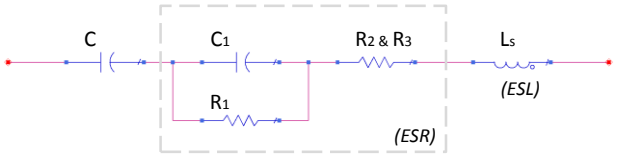


Figure III-44 Equivalent circuit models for capacitor with a resistor-capacitor pair [GASP97]

The total complex impedance and the ESR of the model in Figure III-44 are respectively:

$$Z_{C.total} = \frac{1}{\frac{1}{R_1} + j\omega C_1} + R_2 + R_3 + j(\omega L_s - \frac{1}{\omega C}) \qquad \text{Equation III-22}$$

$$ESR = Real\,(Z_{C.total}) = \frac{R_1}{1 + (\omega C_1 R_1)^2} + R_2 + R_3 = \frac{R_1}{1 + (2\pi f C_1 R_1)^2} + R_2 + R_3 \qquad \text{Equation III-23}$$

According to Equation III-23, one part of ESR ($\frac{R_1}{1+(2\pi f C_1 R_1)^2}$) depends on the frequency f. Sometimes one single resistor-capacitor pair is not enough to cover a large frequency range, so more resistor-capacitor pairs in series are required to obtain better fit. Three aluminum electrolytic capacitor models are presented in Figure III-45. In these models, the value of nominal capacitance and the parasitic inductance are equal, and the only difference is the construction of ESR. The modeling results in Figure III-46 demonstrated that with more resistor-capacitor pairs, the modeling is more accurate for the ESR variation with frequency.

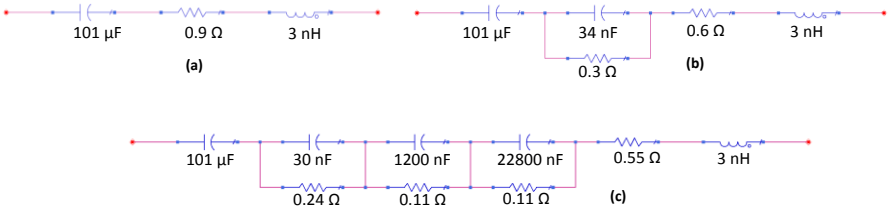


Figure III-45 Three equivalent circuit models for an aluminum electrolytic capacitor 100 µF: (a) Basic model, (b) Model with one resistor-capacitor pair, (c) Model with three resistor-capacitor pairs

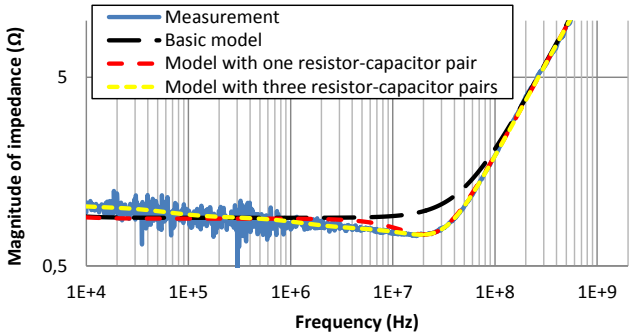


Figure III-46 Impedance measurement and three modeling results of an aluminum electrolytic capacitor 100 µF

III.4.3.3. Equivalent circuit model of Inductor

One commonly accepted basic equivalent circuit model of inductors is illustrated in Figure III-47. In this model, L is the nominal inductance of the device. R_s in series represents the resistance of conductor, which evolves with the frequency as a result of skin effect. The parallel capacitance C_p is created by the endings in the SMD case particularly, and by the proximity of successive turns. R_p in parallel reflects the magnetic core loss [LAFO10].

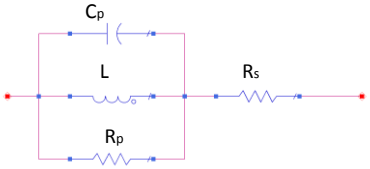


Figure III-47 Basic equivalent circuit models for inductor

The total impedance associated with this simplified model is expressed by:

$$Z_{L.total} = R_s + \frac{j\omega R_p L}{R_p - \omega^2 R_p L C_p + j\omega L} \qquad \text{Equation III-24}$$

The typical frequency responses for inductors are shown in Figure III-48. For an ideal inductor, the DC impedance is zero. However, in reality there is always a small value DC resistance (R_s). With the increase of frequency, R_s has less and less influence and the phase angle θ becomes almost 90°. Similarly to capacitors, there is also a self-resonant frequency for inductors. The difference is that the absolute impedance value of inductor is maximal at the frequency of SRF. At the SRF, the phase is 0° and the reactance value of $Z_{C.total}$ is zero, so we can calculate the self-resonant frequency by Equation III-25 [AGIL13].

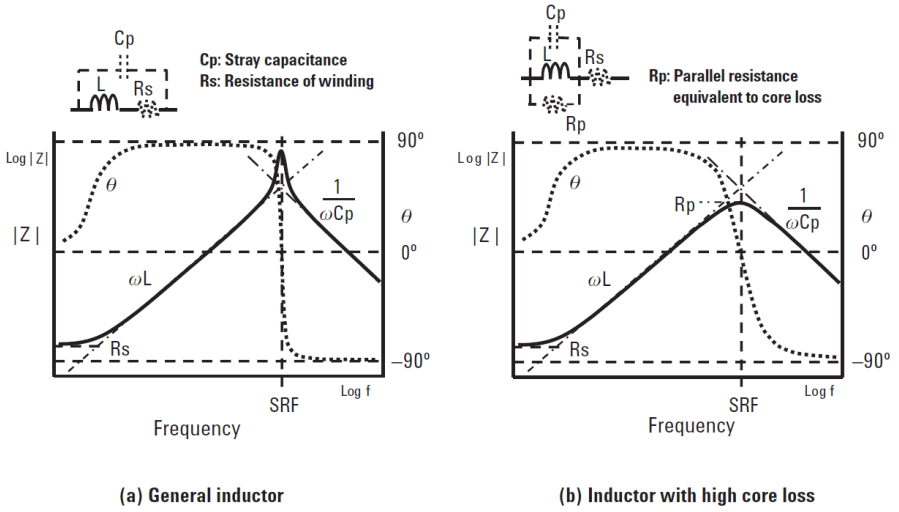


Figure III-48 Inductor frequency response and corresponding models [AGIL13]

$$f_{SRF} = \frac{\omega_{SRF}}{2\pi} = \frac{\sqrt{\frac{1}{LC_p}}}{2\pi} \qquad \text{Equation III-25}$$

One important parameter for inductor is the quality factor (or Q factor), which is the ratio of its inductive reactance to its resistance at a given frequency (Equation III-26), and is a measure of its efficiency. However, since above the SFR the inductor behaves as a capacitive device, we always discuss the quality factor for the frequency range below SFR, where the approximate quality factor of the model in Figure III-47 could be expressed by Equation III-27 at low frequency, or by Equation III-28 if we consider the influence of R_p.

$$Q = \frac{Reactance\ of\ L}{Resistance\ of\ L} = \frac{Imag(Z_L)}{Real(Z_L)} \qquad \text{Equation III-26}$$

$$Q' = \frac{\omega L}{R_s}$$ Equation III-27

$$Q'' = \frac{\omega L {R_p}^2}{\omega^2 L^2 (R_p + R_s) + {R_p}^2 R_s}$$ Equation III-28

One inductor modeling example is demonstrated in Figure III-49. For the frequency response of inductor, the complex parasitic elements at high frequencies from about 50 MHz (Figure III-50) are modeled by several RLC combinations, which have no influence to the parameters in the basic model. The values in these models are obtained by the optimization tool in ADS to fit well with the experimental data.

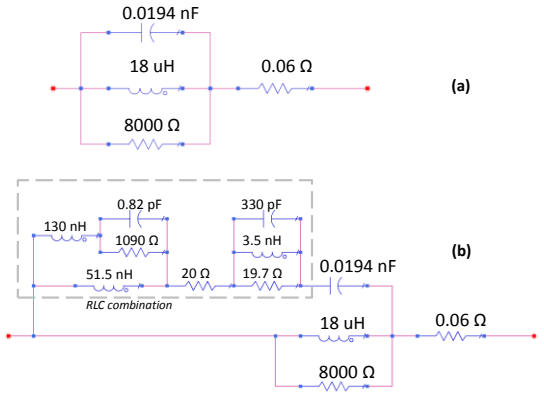


Figure III-49 Two equivalent circuit models for an powder iron inductor 22 µF: (a) Basic model, (b) Model with RLC parasitic elements

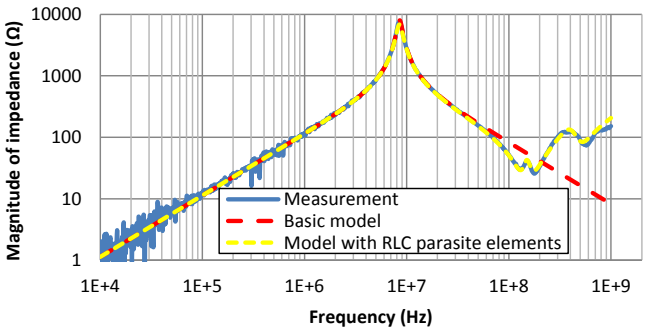


Figure III-50 Impedance measurement and two modeling results of an powder iron inductor 22 µF

III.4.3.4. Aging impact modeling for passive devices

As presented in section III.4, the degradation of passive devices due to aging affects several parameters, like the nominal value of devices. Besides, significant changes could be often observed by impedance measurement. In Figure III-51, the evolution of the impedance of an aluminum capacitor after 4 phases of thermal aging process (85 °C) is presented. The magnitude of the impedance in the frequency range from 1 kHz to 1 MHz demonstrates a gradual increase according to the aging time.

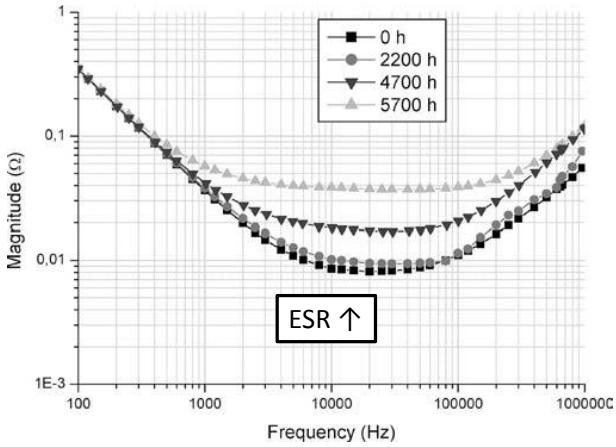


Figure III-51 Variation of impedance vs. aging time of an aluminum electrolytic capacitor [PERI04]

To resume the evolution of impedance, we use the equivalent circuit models proposed below in this section to model the evolution of the impedance according to its aging over a large frequency range. Comparing the equivalent circuit models of each phase during the aging, we can try to resume the aging impact by the evolution of certain model parameters. For example, if we use the model in Figure III-39 (b) to present the impedance characteristics of the capacitor in Figure III-51, the aging impact could be expressed by the increase of ESR (R_s in the model).

The degradation mechanism of passive devices can be explained by some changes at the physical level, which are excited by the aging stress. For the aging impact modeling, there is one approach which is based on the physical degradation mechanism, like the example of aluminum capacitor in [KULK]. However, this method requires good acknowledges about the precise physical constructions and degradation mechanisms. Another approach, which is simpler and more commonly used, is the simplified approximate model based rather on the experimental measurement results, like the model of electrolytic capacitors ESR under thermal stress proposed in [LAHY98], which is considered as a good prediction model based on the Arrhenius equation, where 4700 is the activation energy (Equation III-29).

$$\frac{1}{ESR(t)} = \frac{1}{ESR(0)}\left(1 - kt \cdot e^{\left(\frac{-4700}{T+273}\right)}\right) \qquad \text{Equation III-29}$$

Where

ESR (0) and ESR(t) are the initial ESR and the ESR at aging time t,

T is the thermal aging temperature in Celsius degrees,

k is a constant which depends on the design and the construction of the capacitor.

For aluminum electrolytic capacitors, there are also some other degradation models based on the physical degradation analysis and experimental data. Because of the differences between the tested

devices and modeling methods, the proposed models are not always the same. For example, the capacitance of the aluminum capacitor tends to decrease during a thermal stress. It has a linear relation with aging time in the model of [PERI04], but an exponential relation in the model of [KULK12].

The aging impact model extracted from the measurement should ensure a good accuracy over a long operating period, so more test points and longer aging time of more samples can help to improve the model quality and also the dispersion characterization between the samples related with the aging process. Besides, with accurate degradation models of passive devices, we can simply implant the aging impact in a simulator like SPICE, to simulate the system behavior including also EMC. More details about the modeling of aging impact on passive devices could be found in the case study presented in the next section.

III.5. Case study: Modeling of aging impact on passive devices

III.5.1. Experimental set-up

To analyze the evolution due to the aging stress, several passive devices are selected in this study, as listed in the following Table III-5. Here all the components are surface-mount devices. So we have totally 4 different capacitor references and 2 different inductor references under test. There are several reasons for the selection of these components under test. Firstly, these passive component types are very common in the real applications. Secondly, they are the passive components embedded in a DC-DC converter, which will be studied in a case study of the EME evolution induced by aging in next chapter.

Table III-5 List of passive devices under test

ID	Type	Value	Reference	Manufacturer	Max. ratings
C1	Aluminum capacitor	100 µF	EEEHBA101UAP	PANASONIC	50 V, 105 °C
C2	Tantalum capacitor	100 µF	T491D107K010AT	KEMET	10 V,125 °C
C3	Aluminum capacitor	47 µF	EEEFP1E470AP	PANASONIC	25 V, 105 °C
C4	X7R ceramic capacitor	100 nF	GCM21BR71H104KA37L	MURATA	50 V, 125 °C
L1	Shield powder iron inductor	22 µH	IHLP4040DZ11	VISHAY	4.5 A, 125 °C
L2	Shield powder iron inductor	22 µH	HCM1103220R	COILTRONICS	5 A, 125 °C

To accelerate the aging degradation of the passive components, they are placed under an aging stress condition. In order to compare the impact of different stress condition, in this test, we define two different conditions for certain components, as listed in Table III-6.

Table III-6 Stress conditions for passive devices

Stress type	ID	Description	Samples under test
Thermal with power supply	C1	3.3 V.DC, 0.3 V.AC, 150 °C	C1_1, C1_2, C1_3, C1_4
	C2	3.3 V.DC, 0.03 V.AC, 150 °C	C2_1, C2_2, C3_3, C4_4
	C3	12 V, 150 °C	C3_1, C3_2, C3_3,C3 _4
	C4	3.3 V.DC, 0.3 V.AC, 150 °C	C4_1, C4_2, C4_3, C4_4
	L1	1 A.DC, 150 °C	L1_1, L1_2, L1_3, L1_4
	L2	1 A.DC, 150 °C	L2_1, L2_2, L2_3, L2_4
Thermal without power supply	C1,C2,L1,L2	150 °C	C1_5, C1_6, C2_5, C2_6, L1_5, L1_6, L2_5, L2_6

The selection of stress level (temperature and voltage/current) in this test ensures a relative short aging time without damaging the tested devices definitively. For the thermal aging with power supply, the high temperature is provided by an oven where the ambient temperature is fixed to 150 °C. During the accelerated aging process, the passive devices continue to be powered by an external power supply which is placed outside the oven, as shown in Figure III-52.

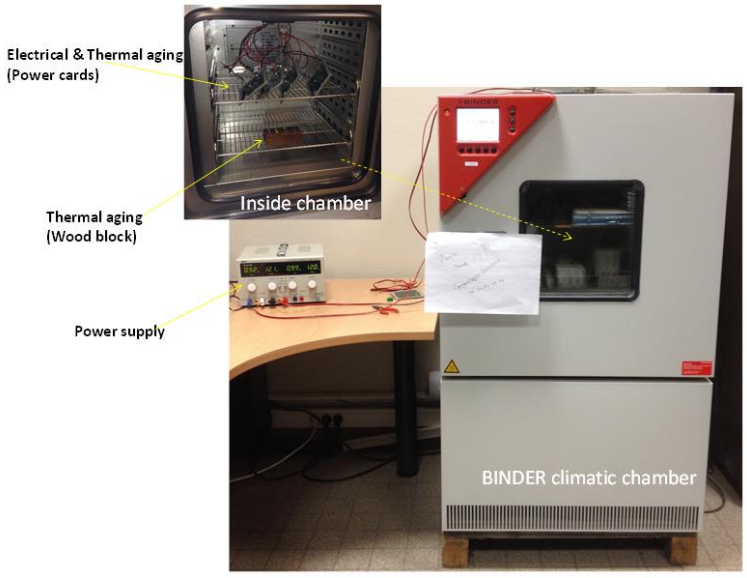


Figure III-52 Aging stress configuration of passive devices

As a second aging condition, the thermal aging stress without power supply applied on C1, C2, L1 and L2 use the same aging temperature 150 °C to simplify the aging configuration. The components are deposited above a wood block to remove undesirable supplementary thermal conductance. This condition is rather applied to compare the impact with the first aging condition which has an additional electrical power supply.

The total aging time for each device is 200 hours. With this aging duration, significant degradations could be observed by the characterization measurements. Besides, the stress condition is

interrupted each 20 hours in order to measure the evolution of the impedance. The impedance measurements and other characterization measurements of each component are applied under a nominal environment temperature of about 25 °C, as presented in III.4.2.

In this test, S-parameter measurements are performed with a network analyzer to extract the impedance profile of passive devices between 9 kHz and 2 GHz. As explained in Figure III-32, to obtain a better accuracy, the best measurement configuration is chosen according to the impedance value to be measured. For the capacitors which have a low value of ESR, two-port shunt-through network method is chosen. Instead, for the inductance, to get an accurate value of the peak impedance at SRF, two-port series-through network method is applied. With the characterization results of each phase during the aging process, we can observe a gradual evolution of the impedance on certain devices. With the degradation modeling method presented in III.4.3, we could construct empirical degradation models of each component.

III.5.2. Characterization of aging impact

The aging impact on passive devices is similar for both thermal aging conditions: with and without power supply, where the operating voltage/current values applied on the components are all in the limit of maximum operating range as resumed in Table III-5 and Table III-6. So in this part the results present only one device of each type under thermal stress with power supply, but the plotted data are representative of all the tested samples of the same type. The comparison of the impact on impedance profile caused by both aging conditions is discussed in the end of this part.

III.5.2.1. Evolution caused by aging stress: effect on capacitors

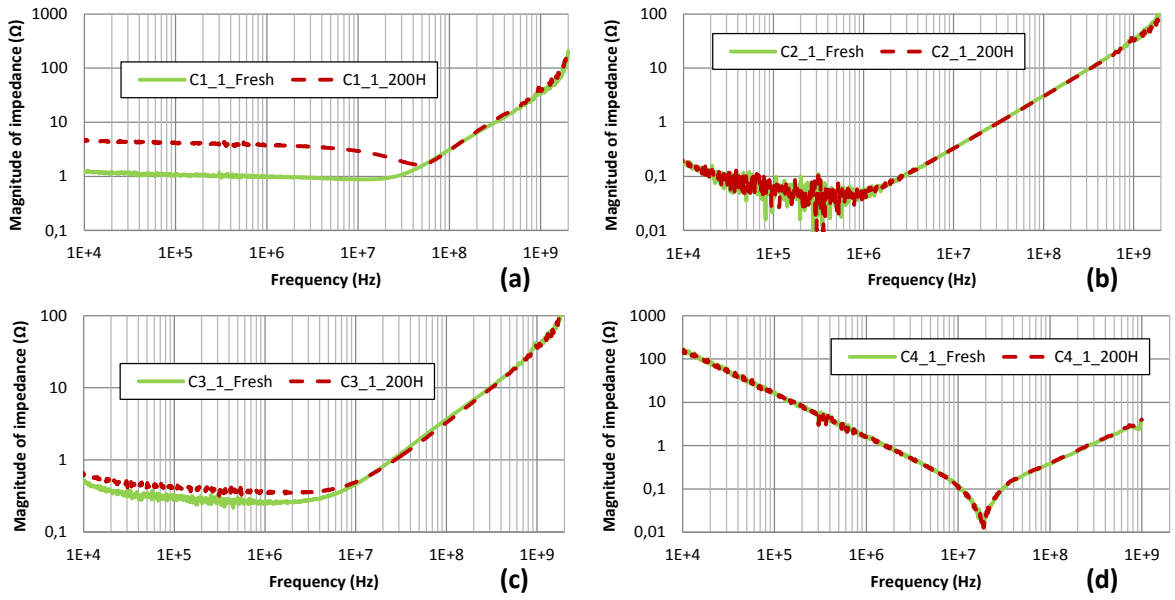


Figure III-53 Impedance evolution of capacitors before and after thermal aging: (a) C1: Aluminum electrolytic capacitor 100 µF; (b) C2: Tantalum capacitor 100 µF; (c) C3: Aluminum electrolytic capacitor 47 µF; (d) C4: X7R ceramic capacitor 100 nF

Three different types of capacitors: aluminum capacitor, tantalum capacitor and ceramic capacitor suffered the thermal overstress with power supply for 200 hours. The comparison of impedance profiles before and after aging shows that a significant degradation is only observed with aluminum electrolytic capacitors, as illustrated in Figure III-53.

The results present only one capacitor of each type, but the plotted data are representative of all the tested samples of the same type. Besides, a graduate increase of ESR (the real part of complex impedance) of electrolytic capacitors for a large frequency range is illustrated in Figure III-54. ESR is not a constant. It decreases with frequency from 10 kHz to 10 MHz.

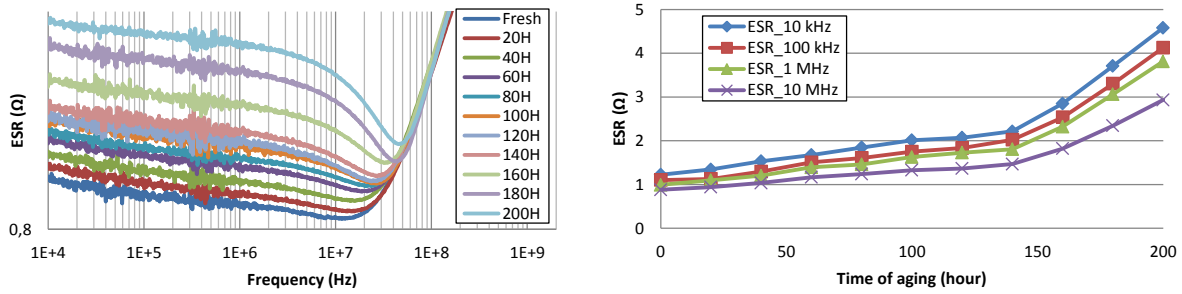


Figure III-54 ESR evolution of C1_1 aluminum electrolytic capacitor 100 µF with time: ESR of each phase during aging (left); Evolution at different frequencies (right)

According to Figure III-55, it's interesting to find that ESR(0)/ESR(t) is almost a constant from 10 kHz to 10 MHz, which means in this frequency range, the variation of ESR value comparing with the initial value is nearly the same. This observation could largely simplify the degradation modeling.

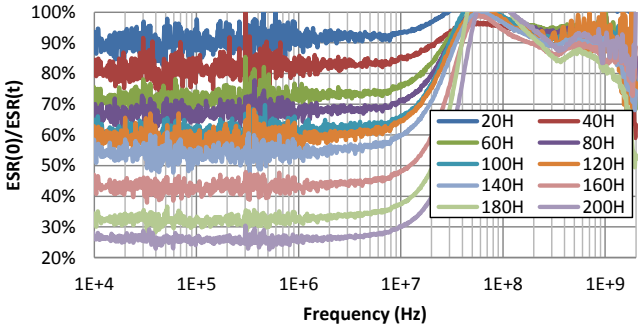


Figure III-55 ESR(0)/ESR(t) with aging time t of C1_1 aluminum electrolytic capacitor 100 µF

Besides, the capacitance value is measured by a multimeter. The results show a similar aging impact on the three different types of capacitors. Little change of capacitance is measured for ceramic capacitors. The aluminum and tantalum capacitors go through a gradual decrease of capacitance over time. The average variation level is illustrated in Figure III-56. The variation is more important for the aluminum capacitors.

As presented in III.4.1.2, according to the former analysis of aluminum electrolytic capacitors, the degradation of this capacitor is due to the vaporization of the electrolyte accelerated by heat and the

degradation of electrolyte caused by ion exchange during charging/discharging. The consequence of the degradation of aluminum capacitor is the drift of two important electrical parameters: the ESR of capacitor increases after aging while the terminal capacitance decreases [KULK12]. However, few studies discussed the aging impact on tantalum capacitors, which are known to have good reliability. It is commonly accepted that tantalum capacitors have no wear-out mechanisms. The slight degradation of capacitance illustrated in Figure III-56 confirms the results presented in [HUAN11]. Finally, as the crystalline structure of the ceramic capacitor is returned to its original state at temperature over the Curie point [JOHA12], no aging impact could be observed.

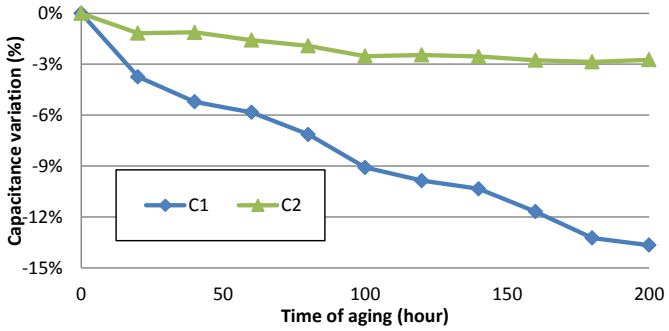


Figure III-56 **Mean variation of capacitance with aging time of aluminum electrolytic capacitor C1 and tantalum capacitor C2**

III.5.2.2. Evolution caused by aging stress: effect on inductors

The tested powder iron inductors are produced by two different manufacturers, and they have similar characteristics. As illustrated in Figure III-57, both inductor references have the similar degradation trend after aging. The self-resonant frequency of inductor declines and the impedance reduces between the resonant frequency and 150 MHz. Above the SRF, the inductor can no more be used as an inductive device, so there is a great decrease of operating frequency range for inductor. Like capacitors, a gradual degradation is also measured over the aging time, as shown in Figure III-58, the impedance peak values at the resonant frequency decrease with time.

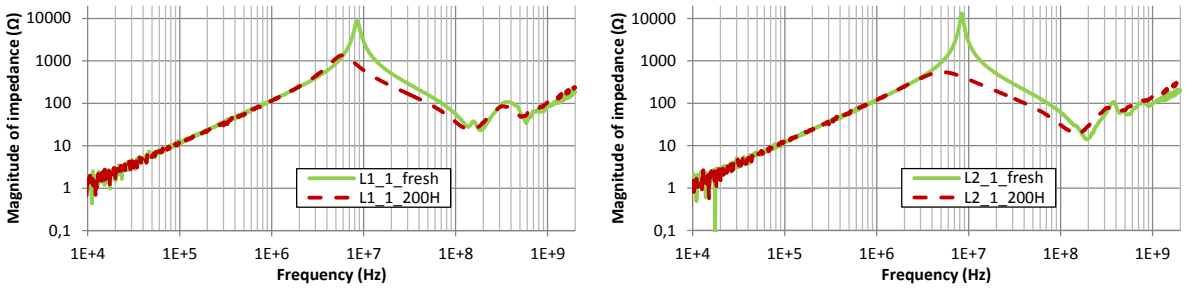


Figure III-57 **Impedance evolution of inductors before and after thermal aging: L1, manufacturer Vishay (left); L2, manufacturer Coiltronics (right)**

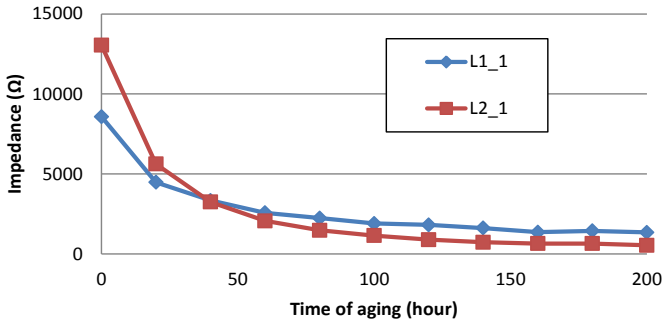


Figure III-58 Evolution of impedance at the resonant frequency with time

As presented in III.4.1.2, the degradation of the impedance profile of powder iron inductor can be explained by an increase of core loss after the thermal stress [KIND13]. The source of the aging is the organic binding material of the powder, such as epoxy. Due to the organic material's low resistance at high temperature, the thermal environment can accelerate the core loss. In addition, for the impedance profile above 200 MHz, no significant variation could be observed. In this frequency range, the impedance is rather related with the parasitic elements such as winding capacitors.

III.5.2.3. Comparison of evolution in two aging conditions

The second aging condition uses only the high temperature. As shown in Figure III-59, the degradation results are similar for both aging conditions, but the degradation level is not the same. Except the tantalum capacitors, the degradation caused by thermal stress with power supply seems more important than that caused by only thermal stress. This phenomenon is easy to be explained, because normally the electrical operating activity could produce the self-heating, which could be a supplementary factor to accelerate the aging degradation process.

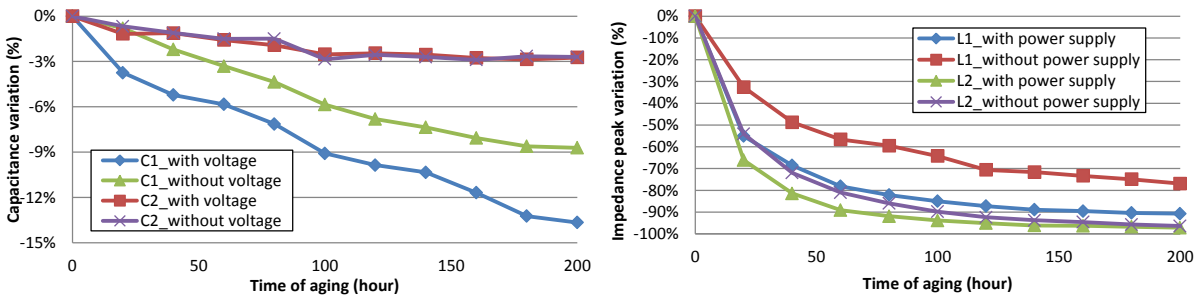


Figure III-59 Comparison of degradation evolution under two aging condition: mean capacitance variation of capacitors C1 and C2 (left); mean impedance peak variation of inductors L1 and L2 (right)

III.5.3. Modeling of aging impact on passive devices

Among all the passive devices under aging stress, the most significant degradations are only observed on aluminum electrolytic capacitors and powder iron inductors. So the work of degradation modeling focuses on these two passive component types. The degradation models are based on accurate high frequency modeling of passive devices, which takes into account the evolution of

electrical characteristics after aging. As the aging process is assumed to be "random" [LOMA03], the degradation model cannot fit perfectly with the measurement, but it can illustrate an important evolution trend of impedance caused by aging. All the simulations are performed with Agilent's Advanced Designed System (ADS). One thing has to be mentioned here: the proposed models are especially adapted to the profile of the devices under test in this study. They could be used as a reference but not as a standard for the other devices of the same type.

III.5.3.1. Modeling of aluminum capacitor degradation

Basic model of capacitor based on basic serial topologies (Figure III-39(b)) are not sufficient to achieve a high accuracy. To model the frequency dependence of the electrolytic capacitor ESR, parallel resistor capacitor pairs are placed in series with a constant resistance, like the example in Figure III-45 (c). The used model is resumed in Figure III-60, where the ESR is not a constant resistor, but varies with frequency.

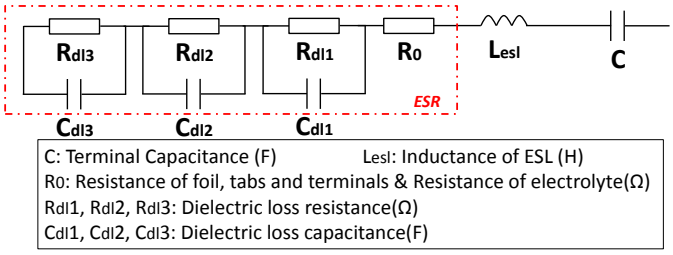


Figure III-60 Electrical model of aluminum electrolytic capacitor

In the model, ESR and C_0 are the two parameters affected by thermal aging. The variation of these two parameters is obtained by measurement: ESR from impedance measurement with a VNA, and C_0 from a multimeter. According to several degradation predictive models of aluminum capacitor [PERI04] [KULK12] and the experimental results, the degradation model up to 10 MHz is given by:

$$ESR(t) = \frac{ESR(0)}{(1 - k_1 t)} \qquad \text{Equation III-30}$$

$$C_0(t) = \frac{C_0(0)}{(1 + k_2 t)} \qquad \text{Equation III-31}$$

Where

ESR(0), $C_0(0)$ is the ESR and C_0 initial value;

ESR(t), $C_0(t)$ is the ESR and C_0 value at aging time t;

k_1, k_2 are two aging constants which depend on the design of the capacitor and the aging condition, which are related with the degradation rate.

The values of k_1 and k_2 are extracted from measurements, which are listed in Table III-7. Though the aging condition is the same, a small dispersion of degradation coefficients of the same aging stress is observed. Moreover the aging constants under the stress condition with power supply are much larger than that under the stress condition without power supply, which confirms the results resumed in III.5.2.3. However, the proportion between k_1 and k_2 is nearly constant.

Table III-7 Parameter values of degradation model of C1

ID	Aging stress	k_1	R^2_ESR(t)	k_2	R^2_C_0(t)	k_1/k_2
C1_1	Thermal stress with power supply	3.68e-3	0.979	9.16e-4	0.93	4.01
C1_2		3.61ae-3	0.975	9.05e-4	0.968	3.99
C1_3		3.36e-3	0.975	8.09e-4	0.967	4.15
C1_4		3.32e-3	0.796	8.11e-4	0.753	4.09
C1_5	Thermal stress without power supply	1.85e-3	0.807	5.21e-4	0.962	3.55
C1_6		1.89e-3	0.824	5.56e-4	0.938	3.4

The comparison between degradation models and experimental results of a sample is shown in Figure III-61, where the models show a good fit with the real degradation parameter drifts. As resumed in Table III-7, the coefficients of determination R^2 between the models and the experimental results are used to conclude the quality of degradation models. The R^2 values of most samples are close to 1, which indicates that the degradation models fit well with the aging effects. Owing to the random aging impact and the measurement errors of impedance, the degradation model cannot fit perfectly with the measurement, but it can illustrate an important evolutionary trend of impedance caused by aging.

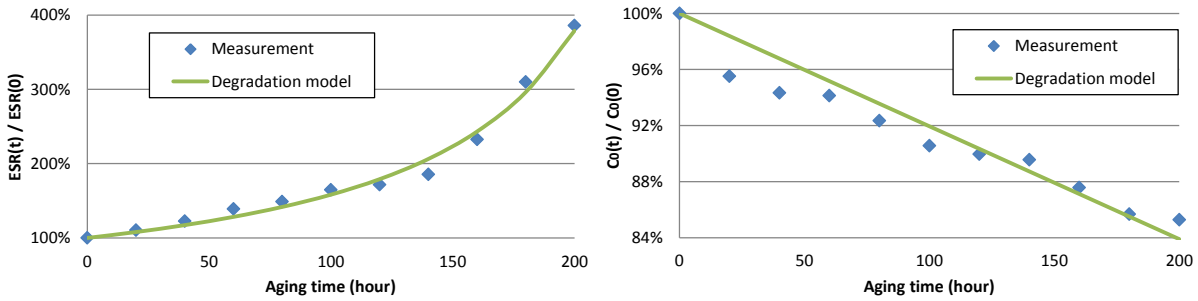


Figure III-61 Degradation parameters of aluminum capacitor C1_1 with time: ESR(t)/ESR(0) (left) and $C_0(t)/C_0(0)$ (right)

In the model shown in Figure III-60, here the ESR (t) in the electrical model is not a single parameter but a group of elements. So to construct the electrical models which could be used in simulator, we should calculate ESR(t) value based on the initial ESR (Equation III-30) at first, and then rebuild the electrical models. However the simulation process is very long and we cannot apply the aging time as a single variable in the simulator.

To simplify this construction, we can replace the initial ESR block in Figure III-60 by a function of frequency, as expressed in Equation III-32.

$$ESR(0) = A - B \cdot ln(f + 0.001) \qquad \text{Equation III-32}$$

Where

f is the frequency in Hz;

A and B are two constants extracted from the initial ESR profile.

Since ESR plays an important role in the impedance profile from 10 kHz to 10 MHz, ESR(0) function needs to coincide with the real ESR profile in this frequency range. Besides, here we use $ln(f + 0.001)$ rather than $ln(f)$, because $ln(0)$ is an infinite value. According to Equation III-30 and Equation III-32, we have an ESR expression of time and frequency as following:

$$ESR(t, f) = \frac{A - B \cdot ln(f + 0.001)}{(1 - k_1 t)} \qquad \text{Equation III-33}$$

In ADS, we can construct an equation based Z-parameters module (named Z1P_Eqn) to represent the $ESR(t, f)$ function, as shown in Figure III-62.

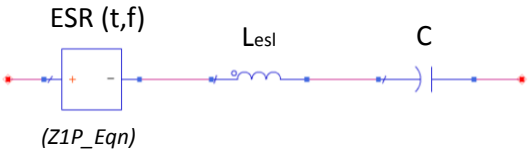


Figure III-62 Electrical model of aluminum capacitor in ADS, using ESR equation block

As shown in Figure III-63, except the differences between 10MHz to 100 MHz, the model could well simulate the impedance profile and its evolution caused by aging. For the sample C1_1, the three constants in Equation III-33 are: A=1.5, B=0.043 and k_1=3.68e-3.

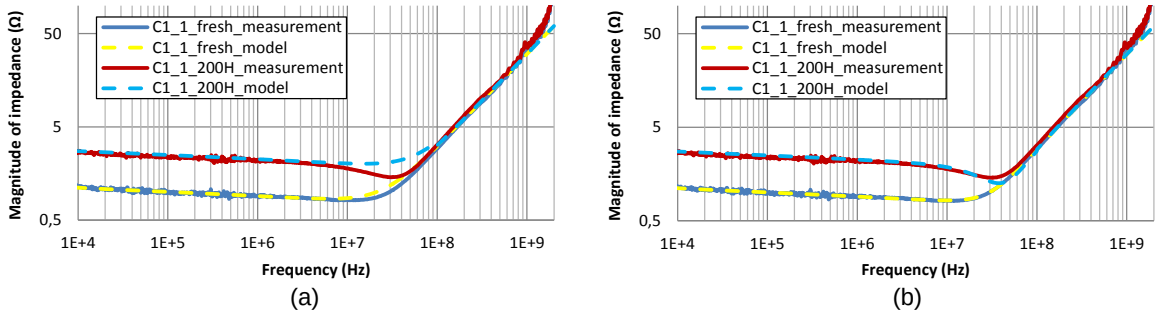


Figure III-63 Model of C1_1 impedance profile before and after aging: using ESR equation block (right); using ESR equation block with parasitic elements (left)

To reduce the difference between the simulation and the measurement shown in Figure III-63 (a), additional parasitic resistor and capacitor are added in parallel with ESR block, as shown in Figure III-64, where C_p = 1800 pF and R_p = 1 Ω. The ESR equation block with additional parasitic elements provides a better fit with the measurement, as shown in Figure III-63 (b).

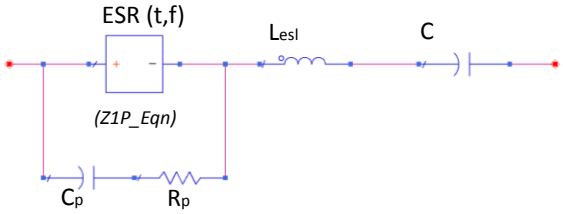


Figure III-64 Electrical model of aluminum capacitor in ADS, using ESR equation block with parasitic elements

III.5.3.2. Modeling of powder iron inductor degradation

The model of the powder iron inductor is illustrated in Figure III-65. To model the fluctuation of impedance of inductor observed above 100MHz, a combination of resistances, inductances and capacitances (RLC) is added, which is already used in Figure III-49 (b). Besides, for the RLC combination in the model of inductor, the construction is only based on the impedance measurement of parasitic elements at high frequency. As a result, this RLC combination does not make much physical sense, and the form could be changed according to the devices and their impedance profiles.

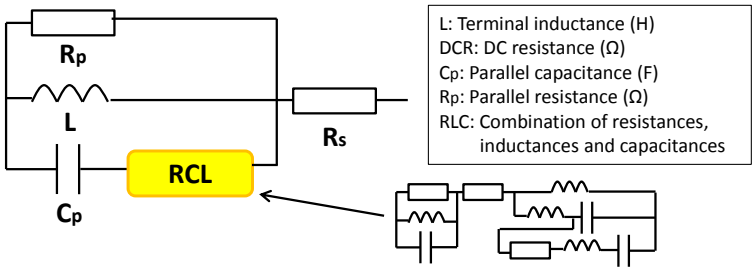


Figure III-65 Electrical model of powder iron inductor

According to the degradation results of powder iron inductor, the impedance above 200 MHz does not significant change after accelerated aging, which is related to the RCL combination. The modeling results before and after aging is shown in Figure III-66.

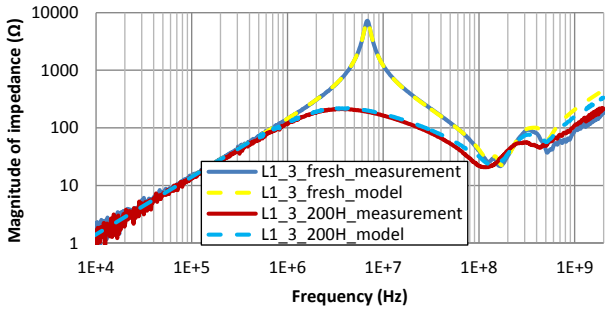


Figure III-66 Model of L1_3 impedance profile before and after aging

The thermal aging affects two parameters: R_p and C_p. Unlike electrolytic capacitor, these two parameters should be extracted from the built electronic models of each phase during aging process. We have not found former studies about the degradation modeling of powder iron inductor. According to the experimental results, an empirical model of degradation parameters is given by:

$$R_p(t) = \frac{R_p(0)}{(1 + k_3 t)} \qquad \text{Equation III-34}$$

$$C_p(t) = C_p(0) \cdot (1 + k_4 t) \qquad \text{Equation III-35}$$

Where

$R_p(0)$, $C_p(0)$ is the R_p and C_p initial value;

$R_p(t)$, $C_p(t)$ is the R_p and C_p value at aging time t;

k_3, k_4 are two constants which depend on the design of the inductor and the aging condition.

Unlike aluminum capacitors, the degradation of inductor demonstrates a great dispersion, as resumed in Table III-8. Besides, it seems that there is no constant relation between k_3 and k_4. However, the results in this table also confirm that the degradation rate is faster for the thermal stress with power supply, and good correlation coefficients R^2 are found between the proposed model and measurement. The proposed empirical degradation model of inductors fits well with the experimental measurement results, as illustrated in Figure III-67.

Table III-8 Parameter value of degradation model of inductors

ID	Aging stress	k_3	$R^2\_R_p(t)$	k_4	$R^2\_C_p(t)$	k_3/k_4
L1_1	Thermal stress with power supply	0.03	0.943	3.6e-3	0.979	8.33
L1_2		0.064	0.916	4.4e-3	0.972	14.55
L1_3		0.142	0.921	7.53e-3	0.935	18.86
L1_4		0.056	0.892	5.54e-3	0.912	10.11
L1_5	Thermal stress without power supply	0.018	0.983	1.76e-3	0.9	10.23
L1_6		0.018	0.941	2.26e-3	0.966	7.96
L2_1	Thermal stress with power supply	0.112	0.983	5.86e-3	0.978	19.11
L2_2		0.371	0.764	21.02e-3	0.914	17.65
L2_3		0.095	0.969	5.85e-3	0.996	16.24
L2_4		0.33	0.905	26.95e-3	0.812	12.24
L2_5	Thermal stress without power supply	0.117	0.945	4.57e-3	0.989	25.6
L2_6		0.11	0.925	4.73e-3	0.982	23.26

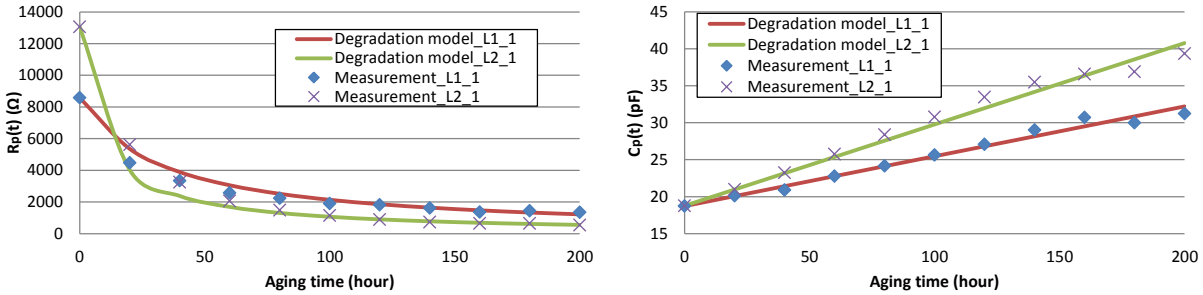


Figure III-67 Degradation parameters of inductors with time: $R_p(t)$ (left) and $C_p(t)$ (right)

III.5.4. Conclusion of the case study

In this case study, the aging impacts of thermal aging stress on several selected passive components (capacitors and inductors) are studied. Different references of passive components are tested and compared under the same aging condition. From impedance measurement, we have a precise insight of the aging impact on the impedance evolution of passive components. Among three different capacitor types under test, only the aluminum capacitors demonstrate significant variations of the impedance after aging process. And for the tested powder iron inductors, their impedances also vary a lot after aging. Based on physical/experimental degradation analysis, we observe that several electrical parameters in the electrical models of passive components evolve gradually during the aging process.

Then we tend to construct the degradation models of passive components. As expressed by several simple equations, the empirical degradation models of these electrical parameters with aging time of aluminum capacitors and powder iron inductors are constructed. There are already some former studies about the degradation of aluminum capacitors, but few works of the degradation of inductors have been shown in literature. This study presents a first study about the degradation model of powder iron inductor. The degradation models of both passive components demonstrate a good fitting with the experimental data, and these models will be served for the EMC modeling of the DC-DC converter case study in the next chapter.

Besides, increased dispersions between device performances after aging are observed. The dispersion of the aging rate under the same aging condition could be expressed by the different aging coefficient k of each samples mentioned in Table III-7 and Table III-8. As a result, the statistical analysis will be led in the last chapter.

III.6. Conclusion

This chapter aimed at studying the origin of EMC level evolution due to electronic component aging. Some basic important knowledge about reliability and accelerated aging theories have been presented in the beginning of this chapter. Then the mechanisms, characterization and modeling of

the degradation of two groups of electronic devices: active MOSFET transistors that constitute the building brick of most of integrated circuits, and passive devices, are discussed. Besides, a case study for passive devices is presented to demonstrate the detailed degradation modeling process. The modeling results fit well with the measurement and the former studies.

One original point in this chapter is the study about the aging impact on powder iron inductor, which has been little discussed in the former studies. However, as few information of degradation could be found about this device, so more studies are needed to understand better the degradation mechanism and the drifts caused by degradation.

As the source of EMC drift, the degradation presentations in this chapter provide a good insight for the analysis of EMC evolution at circuit and PCB level. Moreover, with the degradation models established, the prediction of EMC levels with time becomes possible, which is the subject of the next chapter.

As a result of the limit of time, not all the modeling methods are applied in the case studies, and the tested samples are also limited. However, the objective of this study is not to try to construct a global degradation modeling library but to demonstrate the process and the important points during the degradation modeling process. Besides, the models that we selected in the case studies are applicable and simple, but a good accuracy could be ensured. In future studies, more samples should be tested to verify and improve the models proposed in this thesis. Besides, the influences of temperature and polarization are not taken into account in this study, but they should be studied in future works.

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Chapter IV. Characterization and modeling of long-term EMC evolution

IV.1. Introduction

In the previous chapter, we discussed the reliability issue of electronic components which is an important part of the EMR study. The degradation mechanisms of electronic components (active transistors in integrated circuits and passive components) caused by the aging process which might be the source of EMC drift have been presented. Simple degradation models are proposed based on the former studies and the experimental results. The degradation models demonstrate a satisfactory fitting with the experimental measurements.

As another important part of EMR study, the characterization and modeling of EMC levels are presented in this chapter. It begins with the characterization methodology of the EMR of a circuit, where the EMC measurement of ICs and simple electronic blocks are detailed. Several EMC modeling methods of ICs (ICEM, ICIM) are detailed in the following part. Besides, an additional alternative EMR simulation based on confidential black-box modeling is discussed, which could include both EMC model and effect of the aging. In the end of this chapter, two case studies (EME drift of an operational amplifier and EMI drift of a DC-DC converter) are presented to demonstrate the prediction procedure of EMC levels.

IV.2. EMR characterization

IV.2.1. Characterization flow

The characterization of the EMR of a circuit consists in observing the EMC evolution induced by aging stress. The main objective is to evaluate electromagnetic emission/immunity drifts as function of stress conditions and duration. A global accurate characterization flow is illustrated in Figure IV-1. As presented in Chapter II, the EMR characterization should also consider the statistical analysis. So during the first step test set-up, a sufficient number of samples should be defined to obtain a precise

evolution and to ensure a satisfied confidence level and a reasonable characterization times and costs. The choice of sample number is a statistical calculation based on the confidence interval and confidence level.

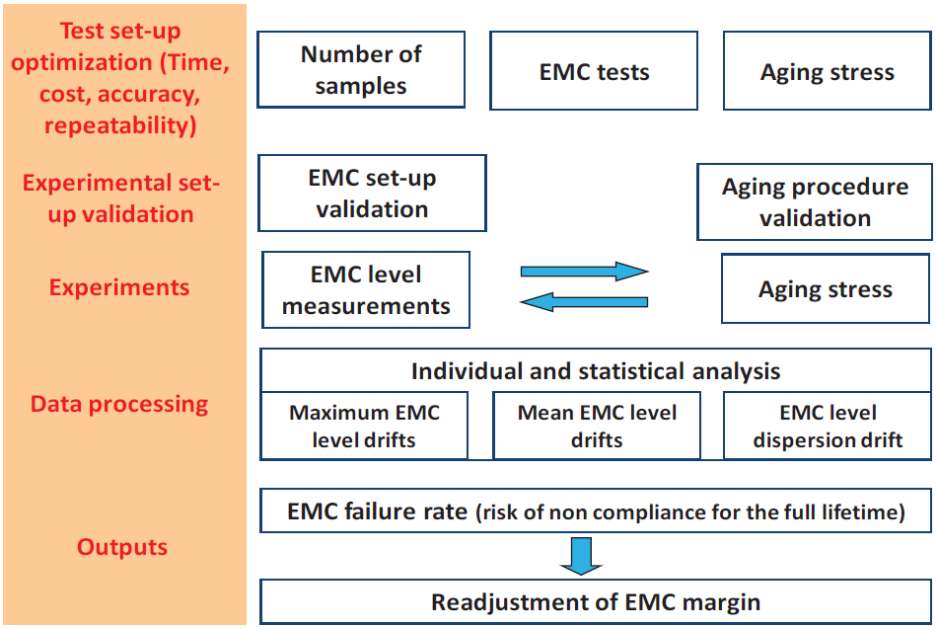


Figure IV-1 ICs electromagnetic robustness experimental methodology [BEND13]

Then the EMC tests are selected in order to ensure a good accuracy and repeatability. The construction of the EMC test plan must be carefully optimized to assure controllable measurement errors during the whole EMR characterization. The EMC tests' environment (test bench configuration, experimental instruments, environmental temperature…) should remain unchanged. Therefore, before the EMC tests between each aging phase, the EMC validation step is required to ensure that the EMC measurements are enough repeatable. Thus, the test environment needs a precise calibration (like the test temperature, the calibration of experimental instruments and test bench), in order to reduce the possible EMC variation caused by the factors other than the device degradation related to aging effects.

Besides, the aging stresses consist in applying an overstress conditions during a short time in order to accelerate the degradation mechanisms. The stress type (extreme temperatures, strong humidity, vibration, shocks, over voltage…) and the overstress level (temperature degree, voltage/current value…) are selected in considering the tested devices' type and application. For all experiments, the components should be still functional without any hard damages in nominal condition after aging. Accelerated aging stage is also a source of uncertainty, so the aging stress and duration must be the same for all samples. Sometimes, the recovery phenomenon should be verified in waiting a period after the stress condition is removed.

To characterize the EMC evolution during the stress, the experiment was based on a measurement–stress–measurement flow, as shown in Figure IV-2. The EMC measurements and the

other characterizations are applied while interrupting the aging stress [BOYE14_a]. As a result, before the start of all tests, a detailed test program is mandatory, where the sequence of all the EMC and aging experimental tests, the duration and the delays between different tests need to be defined.

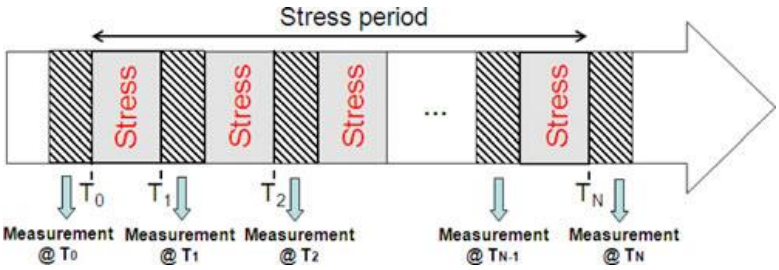


Figure IV-2 Principle of characterization of aging effect: measurement-stress-measurement flow [BOYE14_a]

Once the EMC measurement results are obtained at the end of the measurement campaign, the statistical analysis should be applied on the experimental data. The statistical data concerning the EMC drifts, such as maximum EMC drifts, mean EMC drifts and EMC drifts dispersion would be extracted. We can use these data to analyze the EMC drift and to predict the risk probability of EMC incompliance after aging [LI11] [BEND13]. The statistical analysis will be discussed in Chapter V. After all the EMR analysis, if necessary, the EMC margins at the design level need to be readjusted, such as the safety target drift of IC emission level which is illustrated in Figure IV-3.

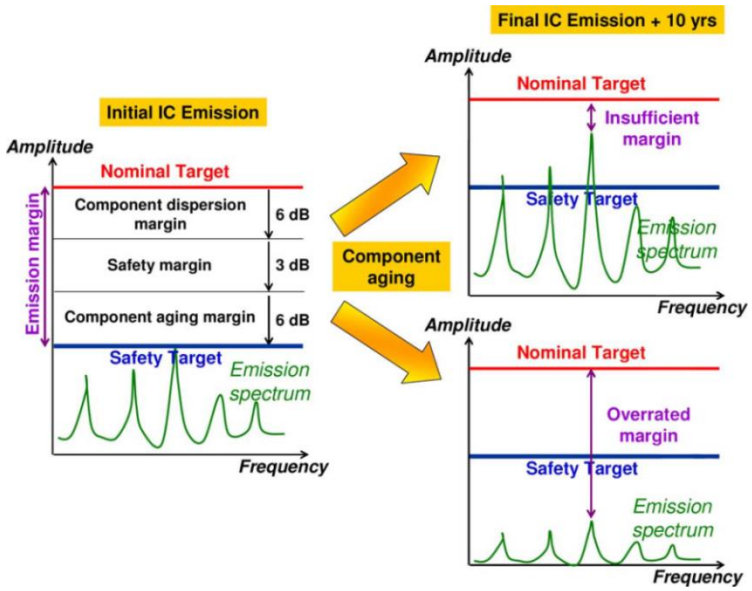


Figure IV-3 Impact of component aging on emission level [BOYE09]

IV.2.2. EMC measurements for ICs adapted to EMR

As mentioned in Chapter II, IEC standards such as IEC 61967 and IEC 62132 propose several EMC measurement dedicated to ICs. Generally, the conducted measurement methods are considered more repeatable than radiated measurement methods. That's because the radiated coupling is strongly influenced by the measurement configuration (distance, orientation) and by the test environment. For

example, it is accepted that the measurement uncertainty of the emission radiated in an anechoic chamber is 6 dB. In addition, the dimensions of the IC circuit are electrically small, so the radiated electromagnetic measurement of a circuit is easily perturbed by the emission generated by the PCB traces, the ground plane and the power supply cables. Among all the radiated electromagnetic measurement, TEM/GTEM cell method (IEC 61967-2 and 62132-2) has a good isolation from the external environment and an acceptable repeatability. However, the TEM/GTEM method is global emission/immunity measurement of system, which is relatively harder to be modeled at system level, so it's not applied in this study. Finally, two conducted EMI and EME measurement methods are chosen in our test, because their uncertainty level and repeatability are acceptable to ensure the consistency of EMR results, and they could also be used in a simple electronic PCB block.

IV.2.2.1. Measurement of conducted emissions: 1 Ω/150 Ω direct coupling method

As demonstrated in Figure IV-4, the EME measurement of 1 Ω/150 Ω direct coupling method [IEC 61967-4] contains two measurement configurations: 1 Ω conducted measurement method and 150 Ω conducted measurement method.

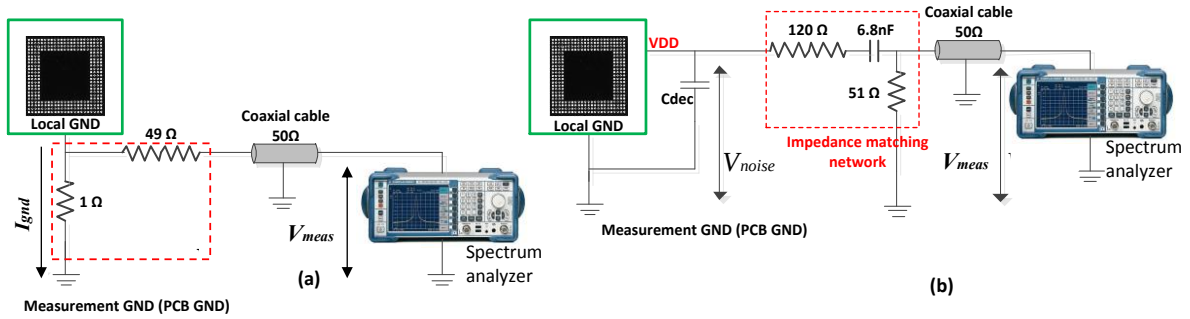


Figure IV-4 Configuration of 1 Ω/150 Ω direct coupling method: (a) 1 Ω probe (b) 150 Ω probe [IEC 61967-4] [LI11]

The first 1 Ω conducted measurement is also called direct RF current measurement, which is dedicated to the measurement of the parasitic conducted emission on ground pins of a component up to 1 GHz. The current flows out of local ground of IC could be measured by an additional resistor of 1 Ω between the local ground of IC and measurement ground. A 49 Ω resistor is placed in serie with the 1 Ω resistor to achieve a 50 Ω impedance matching. The current I_{gnd} is converted to voltage V_{meas} by the 1 Ω probe, and then measured by a spectrum analyzer. The relation between I_{gnd} and V_{meas} can be expressed by Equation IV-1.

$$V_{meas} \approx \frac{I_{gnd} \cdot 1\Omega}{2} \qquad \text{Equation IV-1}$$

The second 150 Ω conducted measurement is used to identify the contribution of a single pin or a group of pins to the EME of the IC under test. This measurement is applied to those pins of the IC under test, that are intended to be connected directly to long (longer than 10 cm) PCB traces or wiring harness [IEC 61967-4]. The impedance matching network in Figure IV-4 (b) provides equivalent input load impedance as a typical antenna impedance of 150 Ω (145 Ω +/- 20 Ω) in order to get accurate measurement results over the full frequency range, and an output-impedance of 50 Ω to match the measurement equipment. The frequency range of this impedance matching network is from 150 kHz to 1 GHz. Similarly to the 1 Ω probe, the transfer function between the measured voltage at tested pin V_{noise} and the measured voltage V_{meas} by the spectrum analyzer could be expressed by Equation IV-2, measured as insertion loss within the 50 Ω system [IEC 61967-4].

$$\frac{V_{meas}}{V_{noise}} \approx 0.2586 = (-11.75\ dB\ \pm\ 2\ dB) \qquad \text{Equation IV-2}$$

One drawback of 1 Ω/150 Ω direct coupling method is that we need to design a supplementary PCB test board for the DUT. Besides, the passive devices for 1 Ω/150 Ω probes should have a small tolerance value and remain a good stability throughout the measurements. Then, the design of probes needs to limit the effect of high-frequency noise, which could disrupt the response of these probes.

IV.2.2.2. Measurement of conducted immunity: Direct RF power injection method

The direct power injection (DPI) method [IEC 62132-4] is used to characterize IC immunity to conducted electromagnetic interference coupled on one or several chosen pins of a circuit [IEC 62132-4]. Since the EMI frequency and amplitude could be controlled manually or automatically, we can obtain the minimum of electromagnetic immunity level which could excite the system failure.

A typical DPI set-up is shows in Figure IV-5. The RF generator provides a sinusoidal disturbance with variable frequency and amplitude, which is then amplified by a RF power amplifier. The directional coupler and the RF power meters are used to measure the forward power P_{for} and the reflected power P_{refl} in the coupler. The RF disturbance is superimposed on the original signal of the injected pin through a decoupling network (usually a bias tee), which could isolate the DC supply or signal generator of DUT from the RF disturbance. A typical basic bias tee is composed of a capacitor that allows AC through but blocks the DC bias and an inductor that blocks AC but allows DC. The value of the bias tee components is chosen depending on the RF frequency range, to ensure a low reflection loss between the RF disturbance and the IC pin and a high isolation between the RF disturbance and DC supply.

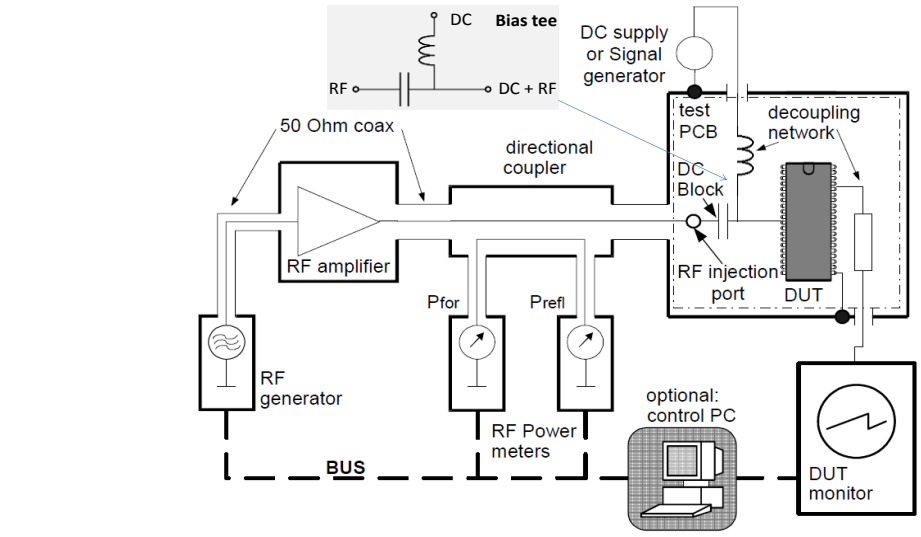


Figure IV-5 Arrangement of a direct injection test set-up [IEC 62132-4]

The advantage of DPI test is that we can measure the real transmitted power with a directive coupler and RF power meters. An example of directive coupler is demonstrated in Figure IV-6 (a), which is a 4-port network. According to the characterization by VNA shown in Figure IV-6 (b), the transmission path from power input to power output is a transmission line with little loss. With the measurement of forward power by the power meter in a large frequency range, we can get the real transmission power in the output P_{out} by the coupling relation between these two ports. With the consideration of the other interconnections, we can get the real injected disturbance level on the test chip.

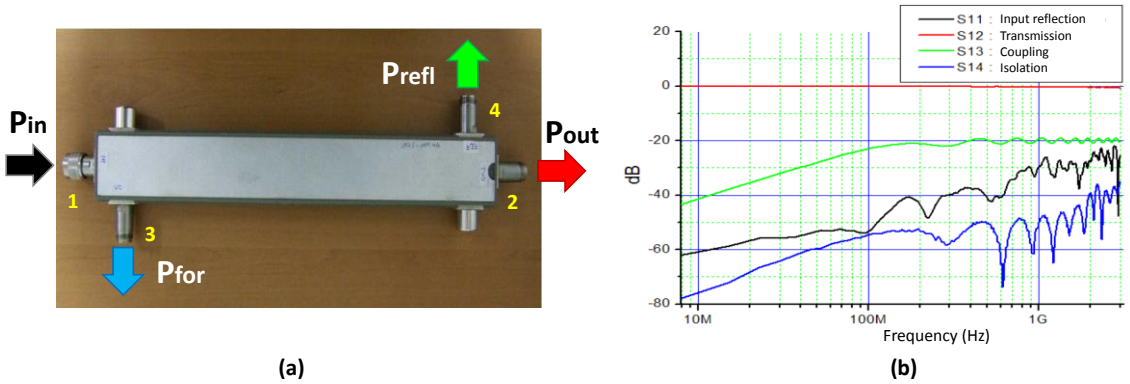


Figure IV-6 Directive coupler: (a) Dual Directional Coupler AGILENT HP 778D; (b) Characterization of coupler by VNA [BOYE09]

To verify if the failure of the DUT is triggered off by the conducted RF disturbance, the response of the DUT can be monitored by an oscilloscope or other monitoring devices preferably with a pass/fail function. Besides, we can use a computer to control automatically the measurement hardware by a program like LabVIEW. The computer can send the commands to modify the output signal of RF generator (frequency, power level), and receive and record the values measured by power meters and oscilloscope.

As discussed in the Chapter II, the failure of an electronic device should be defined according to the DUT and its application: it could be a soft failure, i.e. performance decrease or a recoverable failure, or a hard failure, i.e. a definitive damage. Sometimes we can define more than one failure criterion, which means the failure types for each tested frequency might be different. In the EMR tests, the failure criteria of the same frequency before and after aging should be the same. Besides, to protect the measurement instruments and DUT, we need to define a maximum RF power level. If no failure could be observed with this power, we need to record "no failure" with the maximum RF injected power for this frequency and jump to next test frequencies.

The DPI test usually follows a sequence of power level steps and frequency steps. Figure IV-7 shows a flowchart example of the typical RF power injection sequence. The idea is that the power generated from the RF generator is increased gradually by a fixed step until a failure occurs for each test frequency. Then we change to the next test frequency until the EMI level is obtained for all test frequencies. Each injected RF disturbance (power level or frequency) in every measurement step shall be kept long enough (dwell time in Figure IV-7) to allow the test chip to react and reach a stable state.

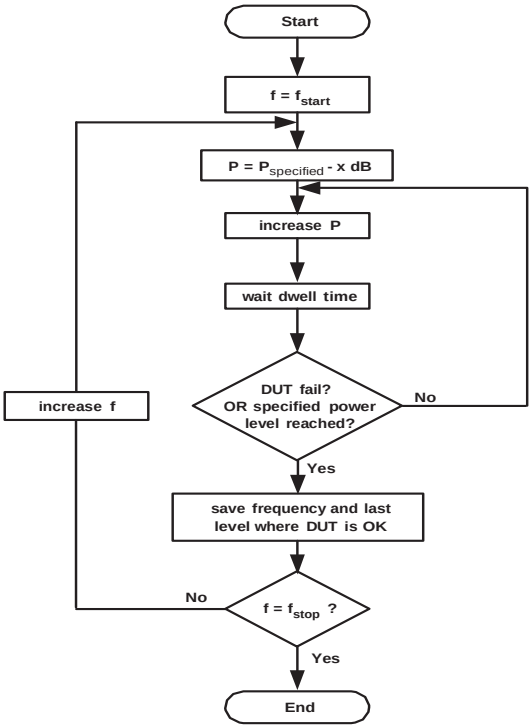


Figure IV-7 Flowchart of the test procedure for Direct Power Injection [IEC 62132-4]

To increase the efficiency of DPI test, some improvements are proposed. In [WU14], the RF source power is increased with a relatively large step (1 dB) to reach the failure area faster, and then the source power step is decreased to a smaller value (0.1 dB) to find the final EMI level with a better accuracy. This optimized method could decrease largely the test time, so it's employed in this study.

Except the two measurement methods presented in this section, with the development of measurement reproducibility, more and more measurement method could be the alternative choices

in the EMR study for ICs, like near-field scanning [IEC TS 61967-3] [IEC TS 62132-9] and TEM/GTEM cell as discussed above [IEC 61967-2] [IEC 62132-2].

IV.3. EMC modeling of ICs

As presented in Chapter II, several modeling methods have been proposed to simulate emission and immunity issues of integrated circuits. This section details two modeling methods for EMC levels of ICs (ICEM and ICIM), which could be applied in the EMR study for the EMC levels modeling during each aging phase.

IV.3.1. ICEM model

The ICEM (Integrated Circuits Emission Model) is dedicated to the simulation of radiated and conducted electromagnetic emission, which could be caused by the internal activity of the circuits and/or the switching in the input/output pins. Also it could be used for the auto-compatibility or the internal immunity analysis at low level. As only the conducted EM measurements are applied in this study, so this part presents rather the ICEM model for conducted emission (ICEM-CE), the modeling for radiated emission will be discussed briefly. More details about the methods of ICEM-RE (Radiated emission) are presented in the standard IEC 62433-3 [IEC 62433-3].

At the beginning, ICEM was proposed to deal with an extension of the IBIS [LEVA02]. Now the ICEM modeling for the conducted emission has been proposed as IEC standard IEC 62433-2 [IEC 62433-2], and have been widely used [LOCH03] [LEVA07] [BERB14] [LABU08]. The ICEM model provides macro-models for ICs to simulate EME on a PCB, which takes into account the internal activities of ICs. Both digital and analog ICs can be modeled by ICEM-CE, which can be applied for modeling an IC-die, a functional block and an Intellectual Property block (IP). Besides, the conducted emission through both the I/O terminals and power supply/ground reference structures could be simulated. As an open modeling source, the ICEM-CE model can be implemented in different formats or languages such as SPICE, VHDL-AMS and Verilog. Usually, SPICE is chosen as default simulation environment to cover all the conducted emissions [IEC 62433-2].

IV.3.1.1. Structure of ICEM

The architecture of ICEM model is based on the functional blocks and interfaces of an integrated circuit. The structure of a typical ICEM model is demonstrated in Figure IV-8, where a set of ICEM blocks could be included in a global ICEM model. The model describes the generation and propagation of electromagnetic emissions produced by ICs. The electromagnetic noise is generated by the internal digital/analog activity and then propagates along the power supply and I/O pads, the package and then the PCB traces and planes. This noise could also be spread through the interconnections or other interfaces (I/O pads, other power supply or substrate) and disturb other

blocks. ICEM model could be used to demonstrate the noise propagation track, and to simulate the overall EMC levels of the circuit without external interference.

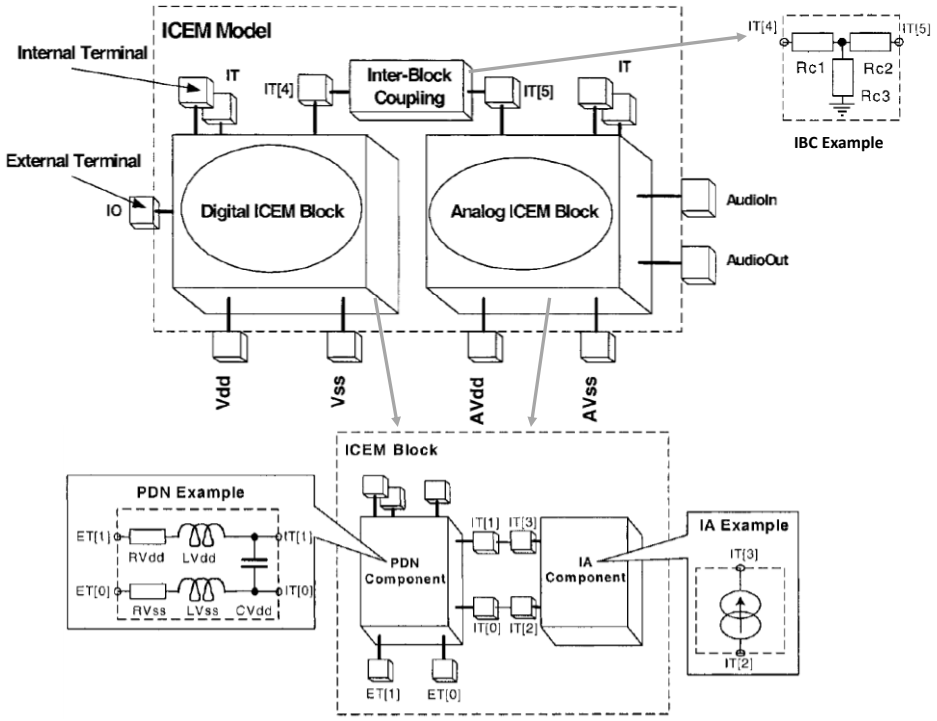


Figure IV-8 Structure of a ICEM model [BEND06]

There are three basic components in the ICEM model: Internal Activity (IA) component, Passive Distribution Network (PDN) component and Inter-Block Coupling (IBC) component. Here IA and PDN components are the two components for a basic ICEM block and IBC component describe the coupling interconnection between the ICEM blocks.

- PDN component

In conducted emission analysis, this component represents the impedance networks of one or more ports of ICs, for example between the power supply and the ground. The format is not defined by the ICEM standard, so in the simulation this component can be expressed by passive elements, block containing S-parameters or distributed elements like the transmission lines. The model of PDN depends a lot on the requirement of frequency range. For example at high frequencies, the skin effect of package interconnects has to be taken into account.

In radiated emission analysis, the PDN describes an electromagnetic dipole used to model the electromagnetic field around the dipole, so the package geometry information or equivalent radiation source structure is included [BEND06] (Figure IV-9), or a set of dipoles configured by simulation to replicate the measured emission data [VIVE07] (Figure IV-10). Because of its complexity, the radiated emission modeling methods are still under study, and they will not be detailed in this thesis.

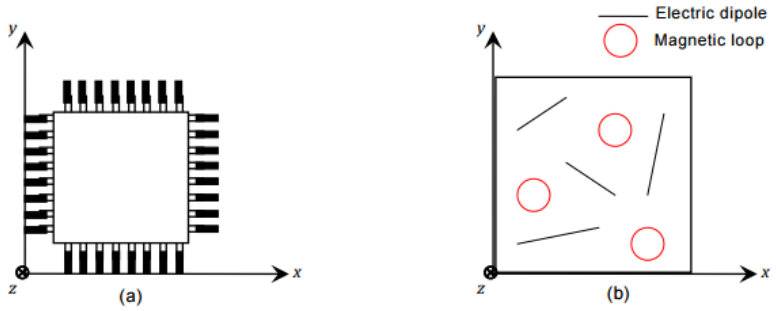


Figure IV-9 Geometrical representation of the ICEM-RE PDN: (a) Integrated Circuit under test (b) Equivalent PDN described with a set of elementary dipole sources [IEC 62433-3]

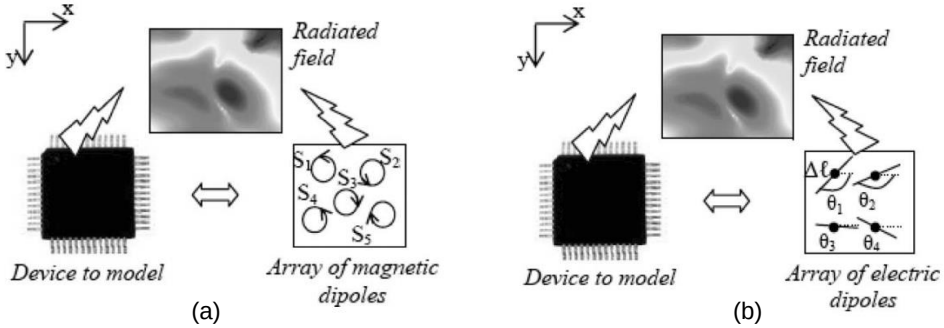


Figure IV-10 Equivalent model of ICEM-RE PDN configuration extracted from measurement: (a) based on a set of magnetic dipoles; (b) based on a set of electric dipoles [VIVE07]

- IA component

In conducted emission modeling, this component represents the internal activity of the circuit by a current source in time or frequency domain. Spice current source such as Triangular, Pulse or Piecewise linear (PWL) source could be applied when the signal form is not very complex. For radiated emissions, the IA component describes the electromagnetic emissions by current vectors, which represent the flowing of currents in the active parts of the devices. Each current vector is expressed with a current module for a set of frequencies [BEND06] [LAFO14].

- IBC component

The IBC component represents the coupling path interconnected between two internal terminals. The IBC example shown in Figure IV-8 models the linkage through the circuit substrate between two different ground references, here IT[4] is the digital ground terminal and IT[5] is the analog ground terminal.

Besides, two kinds of terminals, Internal Terminal (IT) and External Terminal (ET) simulate the interfaces of the model respectively with other on-chip components and external environment (I/O or external power supply blocks).

IV.3.1.2. ICEM-CE modeling structures

An ICEM block contains two components PDN and IA. Although the internal structure and functions of ICs vary a lot, the basic structure of their ICEM model for conducted emission could be constructed in several basic structures. According to [IEC TR 62014-3], a typical ICEM power supply line model is shown in Figure IV-11, and the parameters in this model are listed in Table IV-1. We can use this model to determine the peak harmonics spectrum and main resonances.

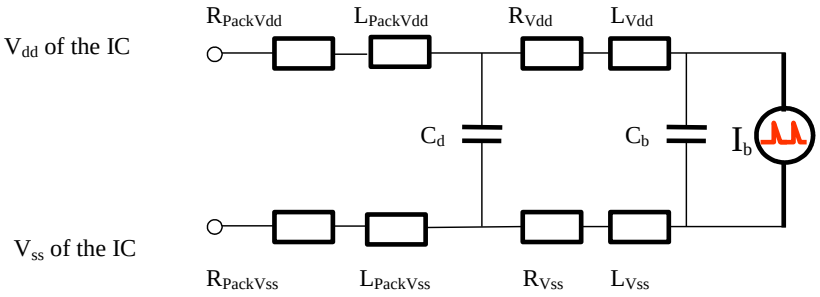


Figure IV-11 Model structure of the IC supply lines [IEC TR 62014-3]

Table IV-1 Parameters of a basic ICEM block of the IC supply lines [IEC TR 62014-3]

Symbol	Description
I_b	Current generator, which is also the IA component in ICEM model
$R_{PackVdd}$, $L_{PackVdd}$	Package resistance and inductance of the positive supply V_{dd}
$R_{PackVss}$, $L_{PackVss}$	Package resistance and inductance of the ground V_{ss}
C_d	Parasitic capacitor between Vdd and Vss package pins
R_{vdd}, L_{vdd}	Series resistance and inductance of Vdd, bonding and die connection
R_{vss}, L_{vss}	Series resistance and inductance of Vss , bonding and die connection
C_b	Internal die capacitor

If we add an I/O pin block which shares the same power supply, the modified model is shown in Figure IV-12, which demonstrates the coupling between the core and I/Os. The I/O stages could be modeled by the model IBIS, IMIC or SPICE. The I/O block could be active or inactive in the simulation. When an I/O is activated, a new equivalent current generator $I_{I/O}$ should be added in parallel with the IA block I_b, where $I_{I/O}$ represents the peripheral current activity [IEC TR 62014-3].

However, in some cases, the I/O stage and the core have separate power supplies. The new model structure is illustrated in Figure IV-13, where a substrate coupling path Z_{sub} between two power supply networks and a decoupling capacitance $C_{I/O}$ are added.

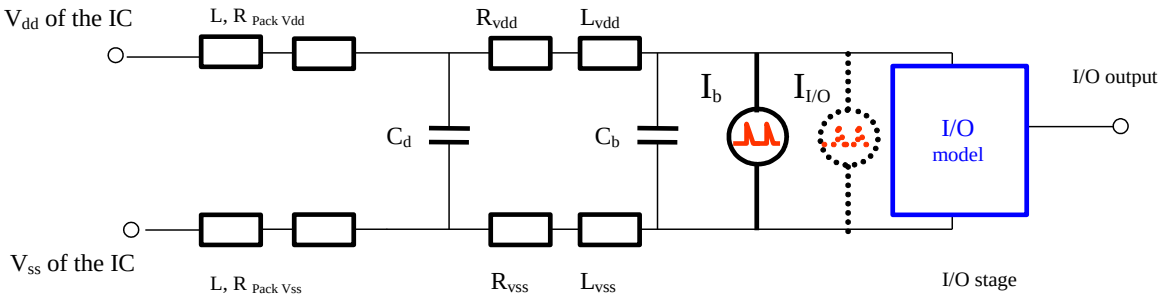


Figure IV-12 Model structure of the coupling between core and I/O buffer [IEC TR 62014-3]

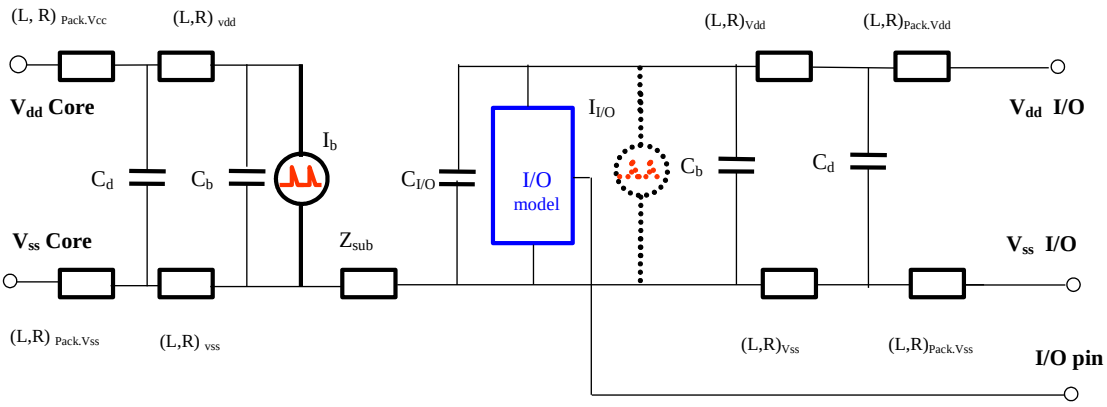


Figure IV-13 Model structure of the coupling between core and I/O buffer with separate supplies [IEC TR 62014-3]

Here three basic ICEM modeling structures are presented. However, in practice the proposed ICEM model should be adapted for the modeled devices and for the modeling applications. For example, an ICEM-CE model of a clock generator chip whose two power supply networks share a same IA block is shown in Figure IV-14. In the ICEM model, the PDN models for the PCB tracks are taken into account, which is also very general in other ICEM-CE modeling practice [BERB14].

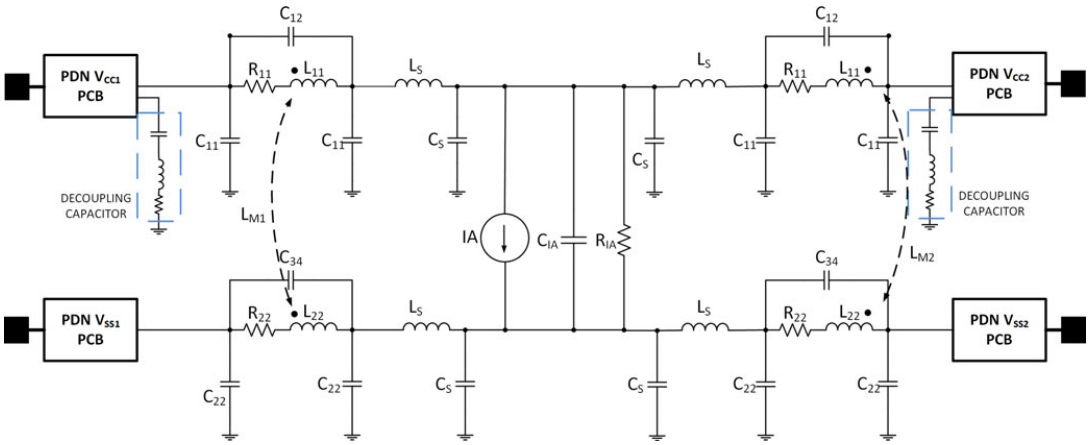


Figure IV-14 ICEM model of a clock generator [BERB14]

IV.3.1.3. Modeling process of ICEM-CE

[IEC 62433-2] defines the environmental constraints for the parameter extractions, which has to be performed under normal room temperature conditions: 23 °C ± 5 °C, without additional requirement on air pressure and humidity. There are three possible ways to generate the ICEM-CE model: using default parameters, extraction from design information, and extraction from measurement.

If no other data is available, default parameters based on the CMOS technology and CPU technology resumed in [IEC 62433-2] could be used. However, the accuracy of this method is relatively low compared to other extraction methods. Besides, the ICEM model could be extracted from the layout simulation of IC manufacturers from parasitic element extractor tools. This method can be applied during the design process. The parameters of the PDN can be extracted by using a 3D EM solver or from the package supplier data-base. Then we can use the modern EDA tools to rebuild the current activity IA of a large amount of transistors. The standard [IEC 62433-2] presents more details about this extraction approach. The third extraction method is based on the measurements when the IC is already available. No silicon design information is required in this method, and a good accuracy could be ensured. As a result, this method is very interesting and useful for the equipment manufacturer and EMC research.

In the following part of this section, the detailed extraction process based on measurements is presented. As an ICEM block contains two basic components: PDN and IA, the process to extract these two components for conducted emissions is presented respectively.

- Passive Distribution Network (PDN) extraction

As presented below, PDN describes the internal passive impedance network of an IC. So like the measurement of passive devices, the VNA measurement of S-parameters is also applied in the PDN extraction, and the VNA measurement configuration should be selected according to the impedance range to get a good accuracy. An additional test board is usually required. A test board example used in [SERP09] is shown in Figure IV-15, where each tested port of the IC use two-port shunt-through network method for the PDN measurement, which could get a good accuracy for the low impedance range. In addition, the measurement probes and the measurement board should be modeled and be de-embedded to get a pure PDN impedance of tested ICs. According to [IEC 62433-2], the main PDN extraction flow is presented in Figure IV-16.

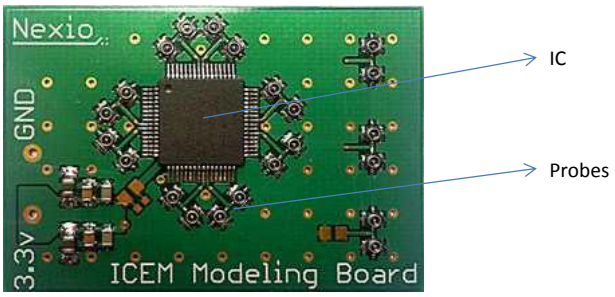


Figure IV-15 ICEM-CE modeling test board of a 64 pins microcontroller [SERP09]

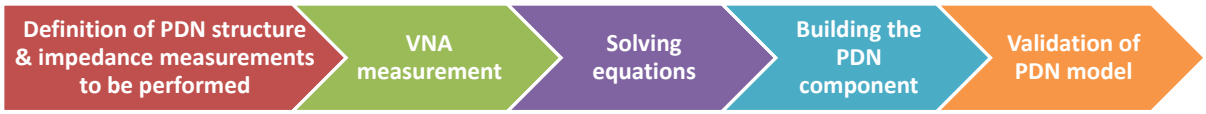


Figure IV-16 PDN modeling extraction process

The definition of PDN structure is based on the experience and the basic models as mentioned in the previous part. With the information about ICs (like the silicon technology, the package, the size, the number of power pins, the IBIS files …) and a first VNA measurement, a predefined structure could be built. A predefined structure example (Figure IV-17) is built for a device that has one pair of digital pins and one pair of analog pins [IEC 62433-2]. Usually a connector is modeled by a serial RL circuit, with a decoupling capacitor. And then between the different block, there is a substrate coupling path Zsub (which is the role of IBC). The predefined structure could be optimized in the following modeling stages. The unknown parameters are determined from this predefined structure, like the 11 parameters (LVcc, RVcc…) in Figure IV-17.

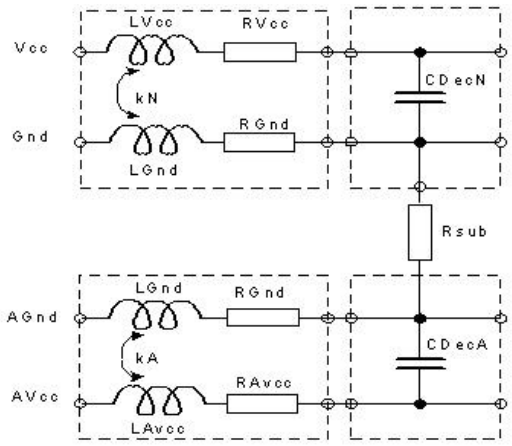


Figure IV-17 Example of a predefined PDN structure [IEC 62433-2]

The VNA measurements are applied to obtain the parameters in the predefined structure. For example in Figure IV-17, the measurement between the Vcc and Gnd (Vcc is connected to the excitation port of VNA and Gnd is connected to the ground) represents the impedance between these two ports (LVcc, RVcc, LGnd, RGnd and CDecN). Besides, the impedance between AGnd and Gnd (AGnd is connected to the excitation port of VNA and Gnd is connected to the ground, or inverse) allows extracting not only the components of conductors but also the IBC component (Rsub). The S-parameter measurement results are converted to impedance Z, according to the equation listed in Table III-4. One thing has to be mentioned: the magnetic coupling between two close pins should be taken into account in the modeling. In some cases, the PDN model parameters vary a lot with the power supply, especially for the internal decoupling capacitors which represent the sum of all parasitic capacitors of CMOS transistors. As a result, some PDN parameters are required to be extracted while the power supply is on [IEC 62433-2]. Usually, the VNA could provide the voltage

supply to the test chip with an incorporated bias tee. If not, an external bias is needed to be inserted between the power supply and the experimental equipment, in order to protect the experimental instruments.

A group of equations is obtained from the measurements. A mathematical solver is used to solve the equations respectively for resistances, inductances and capacitances, and we can get the value of each parameter in the PDN structure. Finally, to check the accuracy of PDN parameters and valid the PDN model, a correlation test with different configuration needs to be applied.

Normally, an IC contains power/ground pins and input/output pins. It cannot be activated by itself, and it should be powered by power supplies. Besides, a set of input signals and appropriate loads for output pins are required. As a result, we need an additional test board to activate the circuit, as shown in Figure IV-18. Usually, this test board is adapted to the EMC measurement, and is also used to extract the parameters of IC models. In the ICEM modeling process, these models are rather specified to the EME levels of circuits.

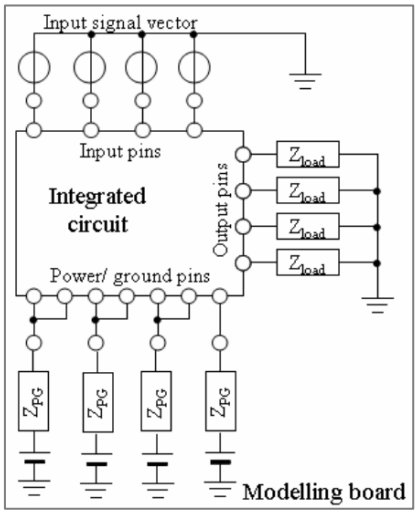


Figure IV-18 The Integrated circuit and its modeling board [IEC TR 62433-2-1]

Usually, the PCB track as the interconnection of the signal in the test chip is considered as a part of PDN. We can use the VNA measurement to extract the model if we have the connector for the experimental instrument. If not, the equivalent model of PCB tracks could be extracted by various methods: analytical formulations or 2D/3D electromagnetic simulation tools. For example, we can model the PCB path from the closed-form equations according to the PCB tracks' type (micro strip, via, loop, plan…), form (length, width, height, thickness…), properties (dielectric, metal…) and modeling frequency range [SICA11]. For another type of tools like ADS Momentum, we can import the layout files of PCB card (DXF or DWG format) to extract the PDN model, which could be applied directly in the SPICE simulation.

- Internal activity (IA) extraction

In most cases, the internal current activity is not accessible directly. However, once the PDN is constructed and validated, we can use the measurement of the external current I_{ext} to extract the IA. The methodology is explained in Figure IV-19, which is demonstrated with a simplified PDN network. Here Z1 and Z2 are the parameters of constructed PDN, and Rm is the impedance of measurement environment. With the measurement of external current in frequency domain $I_{ext}(f)$, the IA current $I_{int}(f)$ could be obtained from Equation IV-3. Here the impedances are presented in a complex value form.

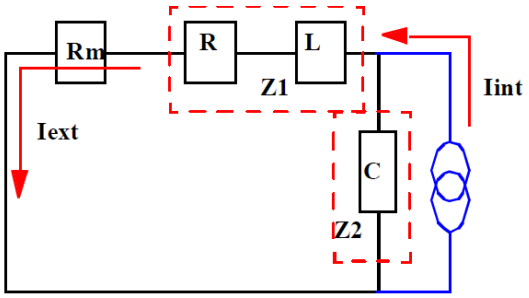


Figure IV-19 Principle of the IA computation [LEVA02]

$$I_{int}(f) = I_{ext}(f)\frac{Zm + Z1 + Z2}{Z2} \qquad \text{Equation IV-3}$$

We can also use the current measurement in time domain to generate the IA component, with the convolution of the FFT (Fast Fourier Transform) or DFT (Discrete Fourier Transform) [IEC 62433-2]. Here we express the transfer function between I_{int} and I_{ext} (such as $\frac{Zm+Z1+Z2}{Z2}$ in Equation IV-3) as Kz(f), and the IA extraction flow from the current in time domain is demonstrated in Figure IV-20.

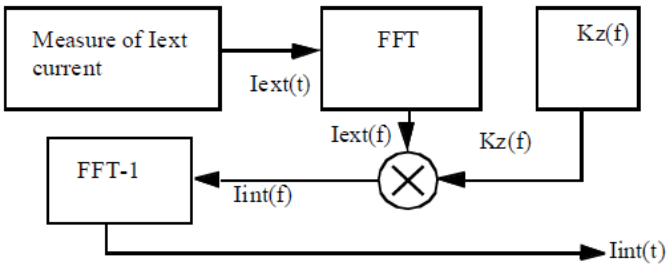


Figure IV-20 IA extraction flow from the current measurement in time domain [LEVA02]

According to the application, sometimes we can use a simplified approximate IA model. For example in [BOYE13], the IA model at each clock edge is presented by a simple triangular waveform, which contains only three parameters: the amplitude, the rising time and the falling time. Even though this model seems very simple and ideal, it provides a good accuracy in the final emission simulation with the measurement.

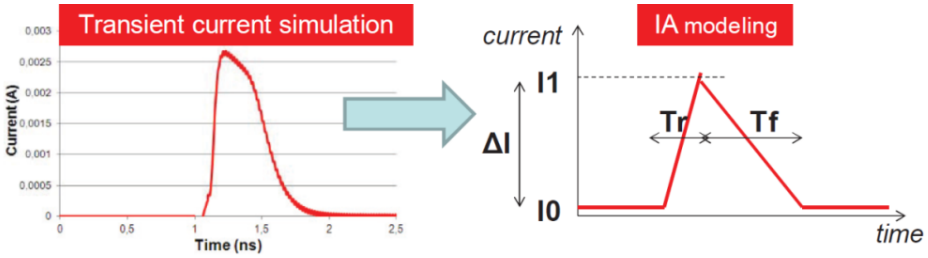


Figure IV-21 IA model of the digital core [BOYE13]

IV.3.2. ICIM model

For a same IC, the immunity model is relatively different to the parasitic emission model. The current generator IA in ICEM model is no more used in the immunity model, and it's replaced by another block, like a simple resistive load in [BEND06] for a 16-bit microcontroller core, or an immunity behavior (IB) block which is related with the internal immunity behavior of the IC in the ICIM model, as shown in Figure IV-22 [IEC 62433-4].

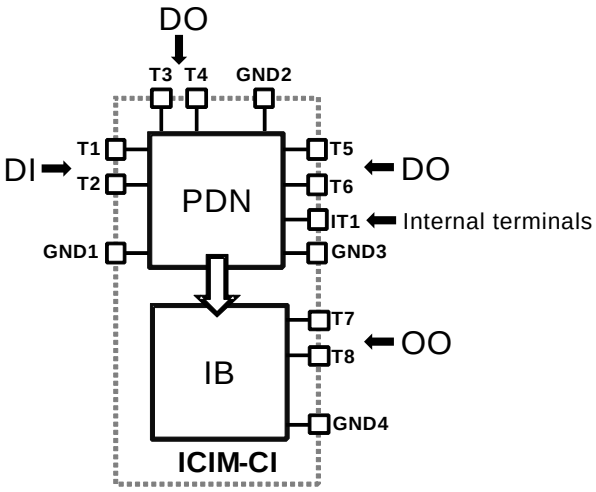


Figure IV-22 General ICIM-CI model structure [IEC 62433-4]

ICIM for conducted immunity is still a proposal standard (IEC 62433-4), and already some case studies are proposed based on this method. In [SU08], the immunity model for a microcontroller is resented. Besides, in [MAO12] and [WU14], the immunity level of ESD protection pads and a low dropout voltage regulator are modeled based on basic information about the circuits' construction and S parameter measurements.

IV.3.2.1. Structure of ICIM-CI

The general structure of ICIM-CI model is illustrated in Figure IV-22. Like the ICEM model, the passive distribution network (PDN) represents the passive elements (like the package, the on-chip interconnections) which conduct the external disturbance to the internal IC active block. For small signal disturbances, the PDN acts as a linear filtering function. In this block, there are several different types of terminals:

- Disturbance Input (DI): Terminals to which disturbances are applied.
- Disturbance output (DO): Terminals that influence the impedance of the DI terminals and consequently receive a part of the disturbance applied on the DI terminals.
- GND: PDN can have one or more ground terminals.
- Internal terminals: Terminals that can influence the impedance of the DI terminals and are internal to the IC (at chip level).

The Immunity Behavioral (IB) block, which replaces the IA block in ICEM, describes the response of ICs to applied disturbances. This block is related with the active parts of the IC, generally integrated functions based on transistors, like CPU core, clock system, memory and analog blocks [IEC 62433-4]. IB covers both in band and out-of-band frequency response. The residual disturbances applied to the IB input are converted to a behavioral output, which can be either a signal in time or frequency domain on which a failure criterion (voltage, current, jitter…) is applied, or directly a pass/fail result according to a failure criterion defined in the IB block. The output terminals of IB block is called Observable Output (OO). Besides, IB shall contain at least one ground terminals. Unlike the direct connection between PDN and IA in ICEM model, there is no direct electrical connection between the PDN block and IB block. The role of the PDN is to define the transmitted power P_T entering the DI terminals, as shown in Figure IV-23, and then the IB block converts P_T to an immunity behavior monitored at OO.

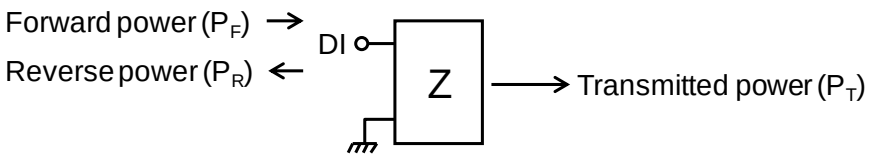


Figure IV-23 Single-ended DI [IEC 62433-4]

The transmitted power P_T could be computed as Equation IV-4. Where S_{11} is the reflection coefficient of the tested IC's pin, and P_F is the forward power injected in this tested pin.

$$P_T = P_F(1 - |S_{11}|^2) \qquad \text{Equation IV-4}$$

As a result, the function of a global ICIM model in the simulation is explained in Figure IV-24. The input of the ICIM model is the disturbance power, and the output of the ICIM model is either the failure detection result (red arrows in Figure IV-24, here the pass/fail test is applied in IB block) or observable signals (blue arrows in Figure IV-24, here the pass/fail test is applied with an external failure detection block). In this figure, the link between the PDN block and the IB block is the transmitted power P_T. However, the output of PDN could be other types of signal which could be served for the failure detection in the following IB stage.

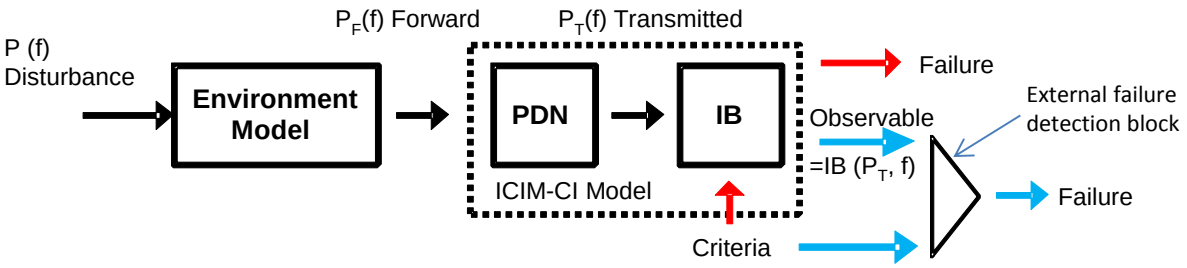


Figure IV-24 Use of the ICIM-CI model for simulation [IEC 62433-4]

Also in complex ICs, there are several independent blocks, and these blocks are internally coupled. The ICIM model of an IC which contains a digital and an analog block is demonstrated in Figure IV-25. Similar to ICEM model, the coupling between different PDN blocks is also modeled by an IBC network. However, two PDN blocks in this IC are both related with the immunity behaviors. As a result, the PDN blocks of digital and analog component and the IBC block are the sub-model of a larger PDN model, which defines the transmitted power to IB block.

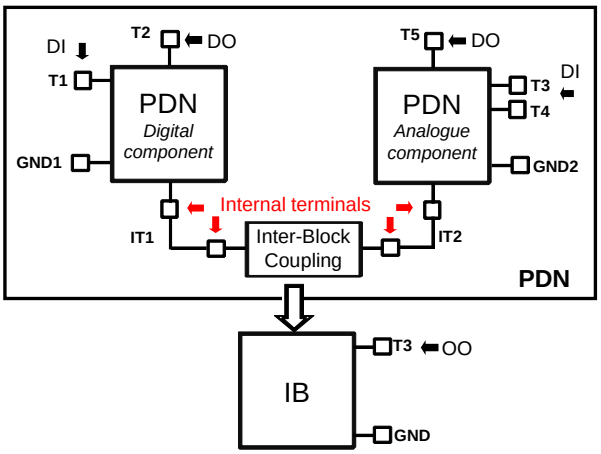


Figure IV-25 ICIM-CI model representation with different blocks [IEC 62433-4]

IV.3.2.2. Modeling process of ICIM-CI

As presented in Figure IV-22, the model ICIM –CI contains two components: PDN and IB. In the former studies, several approaches are applied to extract the PDN and IB blocks in ICIM-CI model.

- PDN extraction

For the PDN block, there are two main methods. The first is the same method in ICEM using a VNA based on S-parameter measurements. This method is already applied in several former immunity studies like [KOO09], [BOYE11] and [WU14], and the results demonstrated a good accuracy with the measurement. However, unlike ICEM model, there is not a direct electrical link between PDN and IB, so the function of PDN block is to obtain the transmitted power P_T (or the absorbed power P_{abs} as mentioned in [AYED15]) which is responsible for the failures. Another PDN extraction method is called RF Injection Probe (RFIP), which is based on a DPI test setup [IEC 62132-4]. This

method could be applied during immunity test and do not need to perform extra measurements [AYED15]. The RFIP test setup for a single port is shown in Figure IV-26. For the measurements of several ports, more RFIP probes are required for each port. The RFIP probe can be passive (RLC elements) or active (RLC + transistors), which is defined by the Z matrix characterized by two-port S-parameter measurements. The PDN impedance Z_{DUT} and the outputs of the PDN (V_{DUT}, and I_{DUT}) could be calculated by the equations detailed in [IEC 62132-4], where the transmitted power P_T is calculated from Equation IV-5. All calculations in frequency domain could be performed by a software tool, such as MATLAB and SCILAB [IEC 62132-4].

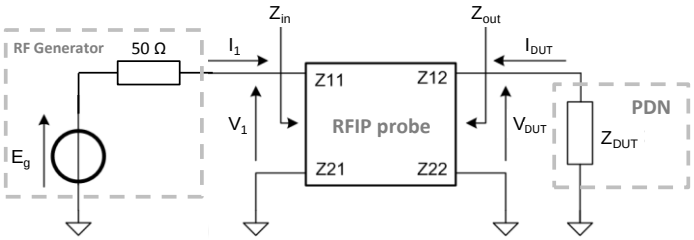


Figure IV-26 RFIP setup [IEC 62433-4]

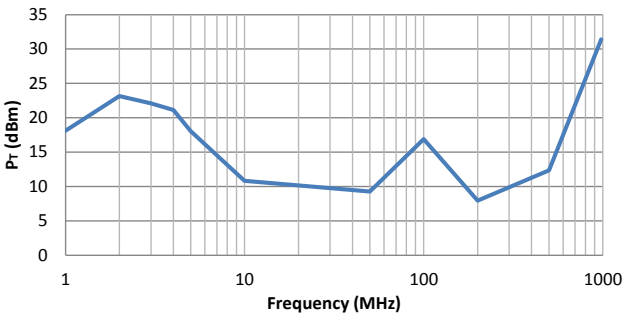
$$P_T = \frac{1}{2} Re\left[\frac{V_{DUT} V_{DUT}^*}{Z_{DUT}}\right] = \frac{1}{2} Re[I_{DUT} I_{DUT}^* Z_{DUT}] \qquad \text{Equation IV-5}$$

- IB extraction

With the PDN model, we can get the transmitted power P_T entering into the device. The IB is the function of this transmitted power for the immunity behaviors at one or more OOs. For the OO which is a direct failure detection signal, an intrinsic value of transmitted power which induces the failure at each frequency is noted as a power threshold. Besides, for the OO which is a waveform for an external pass/fail test, IB block needs to convert the output of PDN to an observable signal.

Frequency (MHz)	P_T (dBm)
1	18.11
2	23.15
3	22.10
4	21.13
5	18.04
10	10.82
50	9.25
100	16.88
200	7.95
500	12.34
980	31.40

(a)



(b)

Figure IV-27 IB block for immunity level: (a) IB table pass/fail criteria; (b) IB table exhibited in figure

In this case, the IB could be extracted by several conducted immunity measurement method, like DPI and RFIP, as detailed in [IEC 62132-4]. However, for each measurement method, the objective is

to extract the function between the transmitted power and the immunity output OO. In a simple case where the pass/fail detection is integrated in IB block, the IB block could be represented by a simple table which summarizes the level of transmitted power at which the failure occurs, or usually the minimum transmitted power level which could induce the failure at each frequency. An example of this table is shown in Figure IV-27 (a), and we can also demonstrate this immunity level in the form of curve (Figure IV-27 (b)).

For the IB block which needs to provide one or several output signals for the external failure detection, a simple IB table is usually not sufficient. For example, the electrical parameters (such as voltage, current, jitter, rise/fall time, delay, etc…) which is related with the immunity behaviors at each value of transmitted power need to be resumed, in a form of discrete database, or in a form of precise or approximate mathematical functions. However, the extractions of these detailed IB by the measurement without internal IC information require a large amount of measurements (a large number of frequencies and injected powers), so an automatic measurement system is recommended.

IV.3.3. EMC black-box model

Two current EMC modeling methods are presented above. In fact, the propositions of these EMC models are based on the ideas of macro-models, which are simplified representations of the original circuits. These models shall retain a sufficient accuracy to model the complex EMC levels of real circuit and make EMC assessments during the design phase.

In some EMC modeling study, like the immunity simulations in [ALAE08], the information about the original netlist of the IC was used. As a result, the proposed model can only be used by the IC manufacturer but not be shared because of the protection of intellectual property. As discussed below, for the EMC modeling, IBIS models could be used to model the input/output buffers and the package effect of IC without real netlist details. And for the modeling of emission and immunity, there are also some modeling methods with different names proposed for the consideration of IP protection, like “Black Box” modeling applied in the IEC technical report for ICEM-CM [IEC TR 62433-2-1], “Trajectory-Based Macromodel” in [GIEL09] or “Behavioral Model” in [DEJO11] to model the EMI-induced rectification effects in nonlinear analog circuits, and also “Surrogate-Based” immunity modeling in [GAZD13]. Although the names of each method are different, some of them have the similar background theory. Besides, the objectives of these proposed models are almost the same. In the form of simplified models, they could hide the real netlist, reduce the simulation time, avoid expensive and time-consuming measurements after tape-out, and still provide high accuracy by the simulation [GAZD13]. As these models do not disclose any intellectual property, so in this study we will call all of them "black box model".

As explained in Figure IV-28, a black box is a block which can be viewed in terms of its inputs and outputs without any knowledge of its internal workings. The opposite of a black box is a white box

where the inner components or logic are available for inspection [WIKI]. Even through the accuracy could be guaranteed with a white box model, the problem is that the model could be very complex, especially for the non-linear activities of the system, which enhances largely the simulation time. Another important disadvantage is the disclosing of internal information, which could be the intellectual property for the industry. In EMC modeling, for the reason of IP protection, the original electronic structure and netlist information are usually required to be replaced by alternative models (usually as a simplified form) which do not provide any confidential information. However, the black box needs to represent the correct relationship between the input stimulus and the output response. Besides, a good accuracy needs to be maintained.

Figure IV-28 Principle of black box modeling [WIKI]

In this section, some of black box methodology examples are presented. In the real practice of EMC modeling, we can select the method according to the applications and the available data.

IV.3.3.1. Black box modeling in EME model

Black box modeling in ICEM-CE model is presented in [IEC TR 62433-2-1]. Here the PDN is described by a numerical matrix (either an impedance matrix or an admittance matrix). The ICEM-CM model structure could be demonstrated in Figure IV-29 (a). The internal activities (IAs) are given as the current sources as presented in IV.3.1, and the PDN is expressed by an admittance matrix [Y].

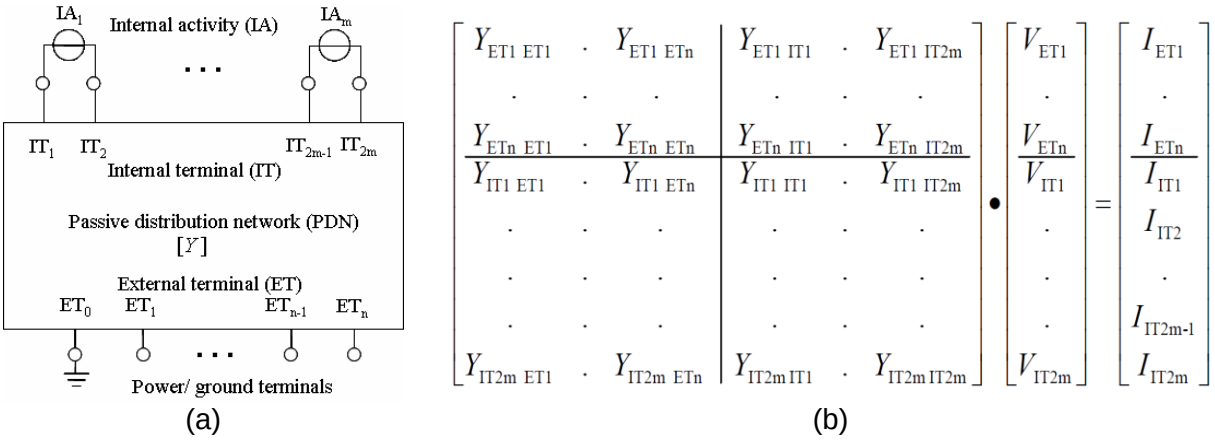


Figure IV-29 ICEM-CE model (a) Structure of the ICEM-CE for IC black box modeling; (b) ICEM-CE model expressed by equation [IEC TR 62433-2-1]

The ICEM-CE model in Figure IV-29 (a) can be expressed by the equation demonstrated in Figure IV-29 (b). The admittance matrix [Y] is based on the nodal analysis method, and its dimension is

(n+2m, n+2m), where n is the number of external terminals except the ground reference, and m is the number of IAs. This equation could be represented in a simplified form in Equation IV-6.

$$[Y] \cdot \begin{bmatrix} [V_{ET}] \\ [V_{IT}] \end{bmatrix} = \begin{bmatrix} [Y_{ETET}] & [Y_{ETIT}] \\ [Y_{ITET}] & [Y_{ITIT}] \end{bmatrix} \cdot \begin{bmatrix} [V_{ET}] \\ [V_{IT}] \end{bmatrix} = \begin{bmatrix} [I_{ET}] \\ [I_{IT}] \end{bmatrix} \quad \text{Equation IV-6}$$

Where

$[V_{ET}]$ and $[I_{ET}]$ (1×n dimension) are respectively the noise voltage and current of ETs, and $[V_{IT}]$ and $[I_{IT}]$ (1×2m dimension) are respectively the noise voltage and current of ITs;

$[Y_{ETET}]$ and $[Y_{ITIT}]$ are respectively the regular admittance sub-matrix that represents interactions between ETs and between ITs, and $[Y_{ETIT}]$ and $[Y_{ITET}]$ are the admittance sub-matrix that represents interactions between ETs and Its and between ITs and ETs.

Besides, the current vector $[I_{IT}]$ could be expressed directly by the internal activities' current. For example, $I_{IT1} = IA_1$, and $I_{IT2} = -IA_1$. Equation IV-6 can be expended into two following equations.

$$[Y_{ETET}] \cdot [V_{ET}] + [Y_{ETIT}] \cdot [V_{IT}] = [I_{ET}] \quad \text{Equation IV-7}$$

$$[Y_{ITET}] \cdot [V_{ET}] + [Y_{ITIT}] \cdot [V_{IT}] = [I_{IT}] \quad \text{Equation IV-8}$$

Then, $[V_{IT}]$ could be eliminated out from Equation IV-7 and Equation IV-8.

$$([Y_{ETET}] - [Y_{ETIT}] \cdot [Y_{ITIT}]^{-1} \cdot [Y_{ITET}]) \cdot [V_{ET}] = [I_{ET}] - [Y_{ETIT}] \cdot [Y_{ITIT}]^{-1} \cdot [I_{IT}] \quad \text{Equation IV-9}$$

We define that

$$[IA'] = [Y_{ETIT}] \cdot [Y_{ITIT}]^{-1} \cdot [I_{IT}] \quad \text{Equation IV-10}$$

$$[Y'_{ETET}] = [Y_{ETET}] - [Y_{ETIT}] \cdot [Y_{ITIT}]^{-1} \cdot [Y_{ITET}] \quad \text{Equation IV-11}$$

Where the dimension of [IA'] is n, and the dimension of $[Y'_{ETET}]$ is (n, n). Then Equation IV-9 is transformed to a very simple form in Equation IV-12. In this equation, [IA'] and $[Y'_{ETET}]$ are named as "Equivalent internal activities (equivalent IAs)" and "Equivalent passive distribution network (equivalent PDN)", respectively. According to Equation IV-10 and Equation IV-11, both of them are based on the PDN matrix and the internal activities, so they are both constant. As a result, a black box model which consists of an equivalent PDN and equivalent IAs are illustrated in Figure IV-30.

$$[Y'_{ETET}] \cdot [V_{ET}] = [I_{ET}] - [IA'] \quad \text{Equation IV-12}$$

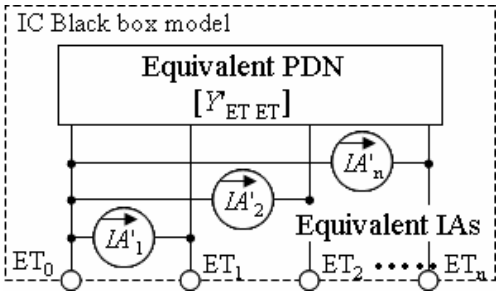


Figure IV-30 IC Black box model structure [IEC TR 62433-2-1]

Compared with Figure IV-29 (a), the internal constructions are completely different, and the internal information is well hidden. Even the amount of real IAs (m) is not disclosed in this black box. Besides, as the interface with the external system, external terminals keep unchanged. Except the reference ground ET_0, the number of the independent external terminals is n, which is identical as the number of the equivalent IAs.

The parameters of the black box model (equivalent IAs [IA'] and equivalent PDN matrix [Y'_{ETET}]) could be extracted from the measurement or simulation. For example, the extraction of [IA'] can be obtained by measuring the external current [I_{ET}] with all the external terminals are RF shorted to the reference terminal. Because when [V_{ET}] = [0], [IA'] = - [I_{ET}]. The extraction process is detailed in [IEC TR 62433-2-1]. Besides, except the model for the PDN of IC, the PDN of board could also be represented in a form of a numerical matrix, which could simplify the simulation process.

IV.3.3.1. Black box modeling in EMI model

In comparing with the EME modeling, the immunity modeling is usually more complex. That's because the immunity model usually need to represent the response of a mixed signal nonlinear system to a disturbance, so usually the susceptibility modeling requires the IC function knowledge which is not really needed in the emission model as explained below.

In ICIM-CI model, the IB block presents the response of the internal non-linear activities to the disturbance power. Usually, it could be a simple behavioral model about failure detection by the threshold table of the RF disturbance power, as demonstrated in Figure IV-27. However, though this model is very simple, the problem is that no detailed response information is revealed in this model, so the model cannot be implemented in a larger system with the other active functions. Besides, if the definition of the failure criterion changes, the model will be no more valid.

As a result, a model consisting in the detailed response (waveforms or certain important parameters) of the circuit to the RF disturbance is usually required. Usually, the susceptibility model could be built in terms of a "black box" (like mathematical expression or other form) which is able to hide the confidential data of ICs. A black box which could substitute a real circuit by a less computationally intensive approximation is also called a surrogate model (or Macromodel or

Behavioral model). These models always have solid mathematical foundations and a strong intuitive linkage to the physical world, so a sufficient accuracy can be provided in a relative expedited simulation time [GIEL09] [YELT12].

One common method used in the electrical engine is the artificial neural network (ANN, or neural network (NN)). This method is a computing model mainly inspired by the nervous systems of brain, and it could be the expression of a logical strategy. It is constituted by the nodes (or neurons) and the interconnections. Each node represents a specific output function, called activation function, which converts a neuron's input to its output activation. Each interconnection between two nodes represents a weight for the connection, which is equivalent to the memory in ANN. The output of the network is defined according to the network structure, the weights of the interconnections, and different excitation functions. In most cases, ANN is a self-adaptive system, which could update the weights for the interconnections by the defined learning process, as shown in Figure IV-31.

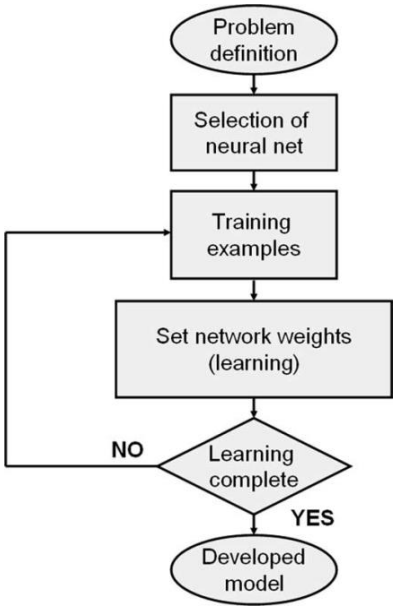


Figure IV-31 Sample of a model using an NN [CHAH08]

Modern neural network is a non-linear statistical data modeling tools, used to model complex relationships between inputs and outputs, or to explore the data model. Several studies, like [GORI09] and [MEVA11] have demonstrated a good fitting of this method with the nonlinear activities of complex input-output relations in the electronic systems.

This method is also used in several EMI modeling studies [CHAH08] [GAZD13].For an IC susceptibility model, the input could be the interference signal, and the output is the response of the system. The nonlinear behavior of the system could be expressed by the following mathematical expression:

$$y_p(t) = f_d\left(x_p(t), \frac{\partial x_p(t)}{\partial t}, \frac{\partial^2 x_p(t)}{\partial t^2}, \frac{\partial^3 x_p(t)}{\partial t^3}, \ldots, \frac{\partial^n x_p(t)}{\partial t^n}\right) \quad \text{Equation IV-13}$$

For a EMI model, $f_d()$ is the general dynamic model of the system, $x_p(t)$ is the disturbance signal, and $y_p(t)$ is the output response. Since a RF interference depends on amplitude and frequency, and they could be revealed by $x_p(t)$ and $\partial x_p(t)/\partial(t)$. Usually, we use the first-order approximation by Equation IV-14.

$$y_p(t) = f_d\left(x_p(t), \frac{\partial x_p(t)}{\partial t}\right) \quad \text{Equation IV-14}$$

Here NN could be considered as a black box with two inputs ($x_p(t)$, and $\partial x_p(t)/\partial t$) and one output $y_d(t)$. The function $f_d()$ could be get by the method NN. For example, in [CHAH08], a tan-sigmoid function was used to extract the final $f_d()$, as shown in Equation IV-15. Where $W_{i,1}$ and $W_{i,2}$ are both the weights, B_i is the bias nodes. The weights and the bias nodes are obtained while the training process of NN, which is based on the EMI measurement results in the study [CHAH08].

$$f_d = tansig\left(\sum_{i=1}^{n}\left(W_{i,1} \times x_p(t) + W_{i,2} \times \frac{\partial x_p(t)}{\partial t} + B_i\right)\right) \quad \text{Equation IV-15}$$

Normally, the RF disturbance pass over a large range of frequencies and amplitudes, thus the amount of the state characterization could be immense. As a result, a reasonable sum of the samples used in learning process of NN should be defined to evident a huge computation, but the accuracy of model should be maintained. In [CHAH08] only 20 frequencies have been chosen, but they represent well the whole DPI bandwidth from 50 MHz to 1 GHz, according to the modeling results. Besides, the quality of model could be measured by the errors like the root relative square error (RSSE), the average relative error (ARE) and the maximum relative error (MRE) [GORI09], or by a regression analysis between the NN model and the corresponding targets [CHAH08].

In addition, the model could also be expressed by the surface plots which do not need the exact mathematical equations. As demonstrated in Figure IV-32 (a), an immunity model of a voltage regulator contains not only the output response of the interference, but also the input impedance ($R_{in,DC}$, $Z_{in,RF,1}$) which plays the role of the PDN block in ICIM-CI model. Here the approximate input current contains only the DC part and the first harmonic could be defined by the input impedance. The input of the EMI block is the RF interference with a variable noise frequency f_{noise} and amplitude $V_{in,RF}$. Finally, four factors of the output response and the input impedance in the NN models are extracted in the form of 3D surface plots, based on 252 samples (selected by a Lola-Voronoi sampling algorithm) obtained by the simulations of the original netlist, as shown in Figure IV-32. Finally, all

these components in the black box immunity model could be implemented simply into the simulator, like the frequency-domain defined device (FDD) block in this case study [GAZD13].

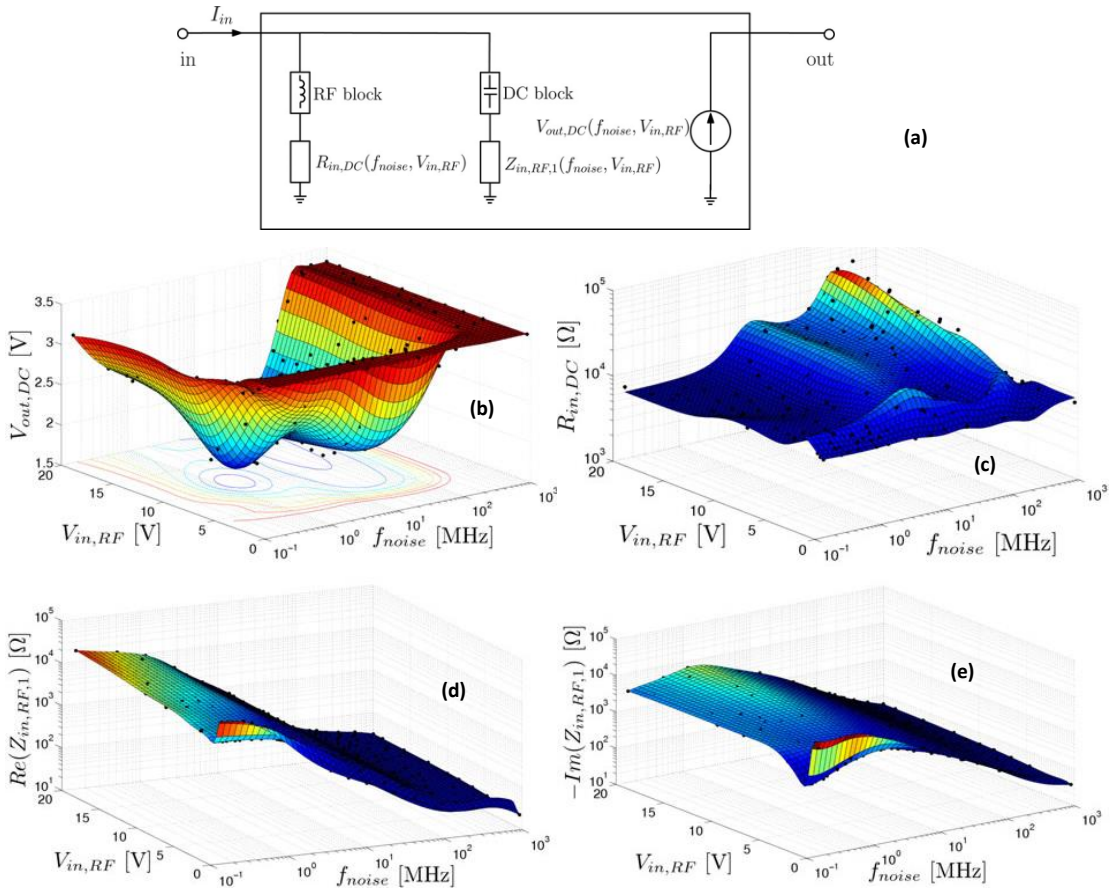


Figure IV-32 ANN surrogates (colored surface plots) of the output voltage and input impedances, based on 252 samples (black dots): (a) Architecture of voltage regulator's immunity model, (b) $V_{out,DC}$ surface plots; (c)$R_{in,DC}$ surface plots; (d) $Re(Z_{in,RF,1})$ surface plots; (e) $-IM(Z_{in,RF,1})$ surface plots [GAZD13]

Another important advantage is the efficiency of the simulation with the black box model. With the same simulation program, the simulation of the original netlist takes 50.2s, but that of the model in Figure IV-32 (a) takes only 1.5s [GAZD13].

IV.3.4. Validation of model

If we do not have the complete IC information, the model structure from the measurements and the experiences is usually based on some hypotheses. For example, a typical IA modeled by a triangular waveform is only an approximate model, which is not the real current activity of ICs. Besides, in the PDN modeling by a RLC network based on S-parameters measurements, the non-linearity is not taken into account. As a result, the verification is need to validation the established model and to ensure that the EMC model works in other conditions than that we extract the model. In the presentation for ICIM model, we have mentioned that a validation of a different configuration to verify the PDN model is required. But it's difficult to validate the IA model, because it is difficult to achieve a good correlation between the IA measurements with a triangular signal [BERB14].

There are some criteria proposed to validate the model. For the PDN, if there is no more than 3 dB deviation between the VNA measurement and the model, we can conclude that the linearity hypothesis of PDN model is verified, and that the PDN model is validated [IEC 62132-4].

Besides, for the global EMC model, the validation is based on the comparison between the experimental EMC levels and the simulation results. There are several statistical rules could be selected to demonstrate the correlation between the simulation and the measurement, such as z-score (also called standard score) and determination coefficient R^2. Besides, a specific Feature selective validation (FSV) method was proposed to describe the quality of electromagnetic simulation results compared to measurement results [DUFF06] [ORLA06]. It is the method chosen in a recent IEEE standard for validation of simulation results (IEEE standard 1597.1) [IEEE09]. However, the basic concept of this method is the comparison of goodness of the fit between two sets of data.

FSV proposes three measures: Amplitude Difference Measure (ADM), which compares the amplitudes and trends information of the two data sets; Feature Difference Measure (FDM), which compares the rapidly changing features; and Global Difference Measure (GDM) which is a combination of ADM and FDM. One original point of this method is that the difference measure values (ADM, FDM and GDM) are divided into six categories as presented in Table IV-2. These natural language descriptions of fitting level make the results more intelligible.

Table IV-2 FSV interpretation scale

FSV value (quantitative)	FSV interpretation (qualitative)
Less than 0.1	Excellent
Between 0.1 and 0.2	Very good
Between 0.2 and 0.4	Good
Between 0.4 and 0.8	Fair
Between 0.8 and 1.6	Poor
Greater than 1.6	Very poor

More details of the algorithm for these measures could be found in the standard and the website of the FSV project [FSV]. A free copy of the FSV software tool injected in Matlab which is used to calculate difference measure values can be downloaded from this site. With this method, the validation of simulation could be represented as a quality level.

An example using this method is demonstrated in Figure IV-33. The comparison of the data forms (Figure IV-33 (a)) in frequency domain is hard to conclude about the similarity level. The FSV results could be represented by the measurements on a point-by-point basis per frequency point (Figure

IV-33 (b)) and a confidence histogram (Figure IV-33 (c)). The latter using probability density function histograms of the six "Levels" gives a better understanding of how close these two set of data are. Finally, the overall GDM is calculated by the mean value of GDM at all frequency points (the mean value of all GDM results at Figure IV-33 (b)), which gives an overall single-figure goodness-of-fit. In this case, the overall mean GDM is 0.335, which is in the quality level 3 "Good" [DUFF06]. In practice, we can predefine the quality level of simulation in FSV that we need to validate the EMC models.

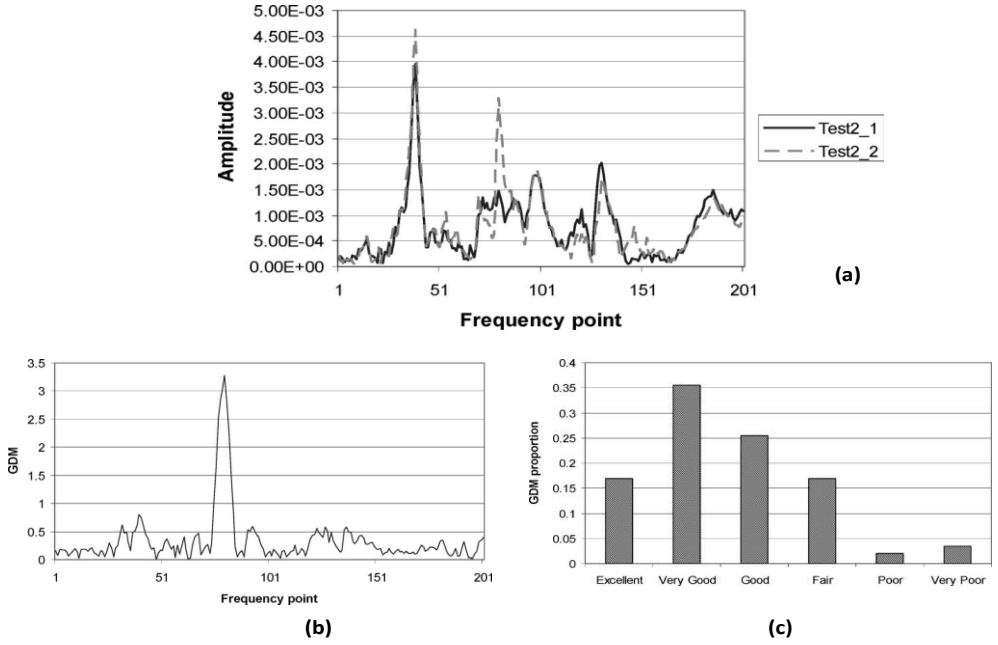


Figure IV-33 FSV method example: (a) Original data for comparison; (b) GDM result per each frequency; (c) GDM confidence histogram for the comparison [DUFF06]

IV.4. EMR modeling process

Several former studies like [BEND13], [BOYE14_a] and [WU13] have demonstrated that the significant variation of EMC levels occurred after the aging stress in numerous circuits, and the EMC variation level depends a lot on the operating conditions and stress duration. In this study, we tend to develop a general EMR modeling methodology, which is dedicated to predict the evolution of circuit EMC levels on the long-term. A general methodology used to simulate the EMC drift induced by aging process proposed in our study is described in Figure IV-34. Several part of this modeling flow like the EMC modeling before and after aging has been practiced in several former studies to analyze the EMC drift, like the emission drift of a digital core in [BOYE13] and the immunity drift of a phase-locked loop in [BOYE11]. However, only two aging state (fresh and aged) are analyzed in these studies, so more precise EMR analysis during the different phases of the whole aging time are needed.

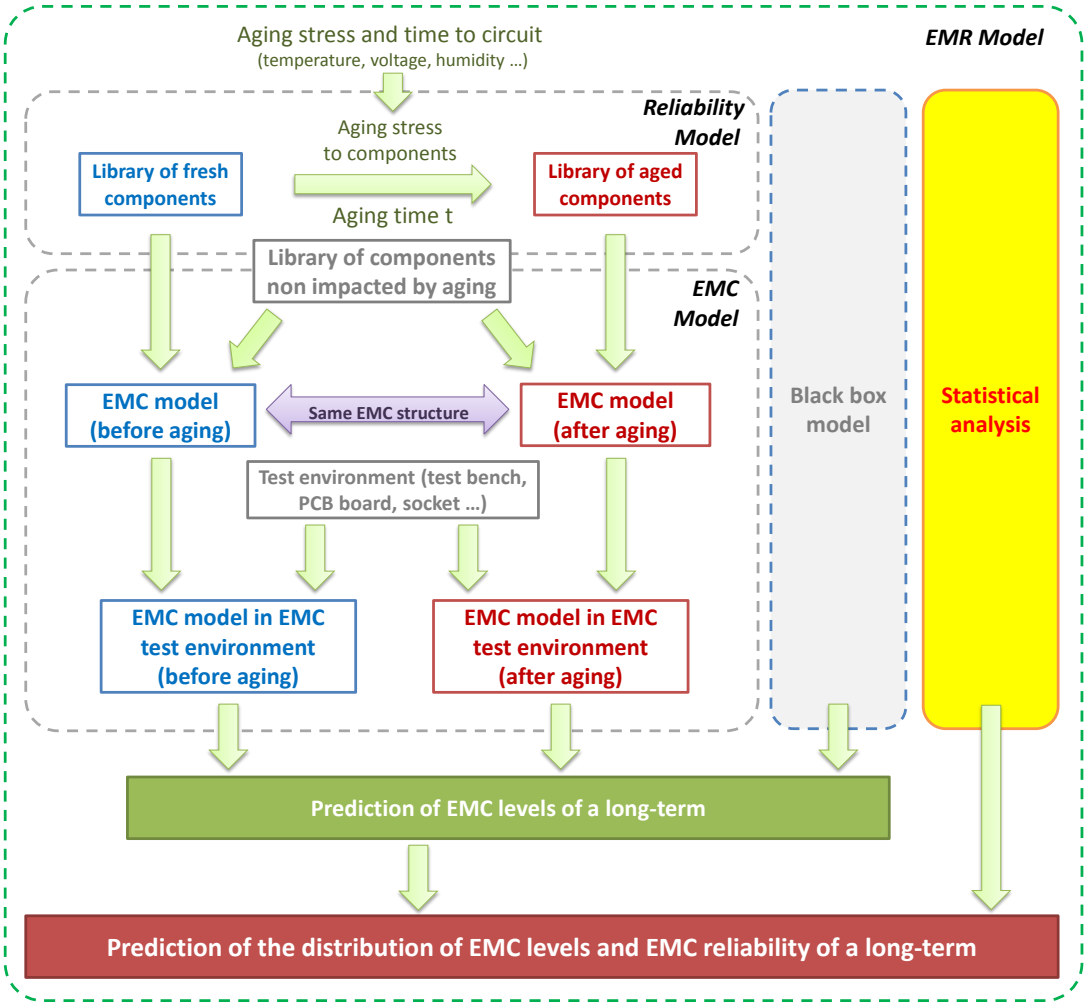


Figure IV-34 Long-term EMC levels prediction flow

The objective of this proposed EMR prediction model is that in design stage we could predict the EMC levels of circuits on the long-term with a predefined operating environment (or a real future operating environment). Then with the statistical analysis, we could get the statistical distribution of EMC levels during each aging phase, and also predict the probability of EMC compliance. Generally, the modeling process contains two main parts: reliability modeling of degraded components, EMC modeling of ICs and electronic blocks. Besides, for the reason of the protection of IP, the black box model could be an alternative method in the EMR prediction model.

- Reliability model of degraded components

The reliability model was discussed in the previous chapter. Some former EMR studies like [LI11] and [BOYE11] focused on rather aging impact on the transistors of integrated circuits, regardless the aging effect on PCB board and associated passive components and the chip package [LI11]. However, as presented in II.4, except the active transistor, the other parts of circuit, like passive components or transmission cable could also be the source of EMC drift [LAHY98] [LESS93]. For this reason, the complete EMR study should consider each degraded possibility caused by aging process which is

related with the EMC levels. The critical parts of circuit which are degraded during the aging process could be identified by the experimental analysis (replace each part of the circuit by a fresh component to identify the degradation source) [BOYE14_b] or by the analysis of operating conditions of each component during the design phase (e.g. the voltage at transistor terminal) [LI11]. Besides, the operating condition of the global system could be different than that of the degraded components. For example, the self-heating phenomenon of components increases the component temperature in comparing with the ambient temperature. With the accurate information of the operating conditions, we can conclude about the degradation mechanisms of impacted components, and then propose the correct degradation model with aging time t.

The reliability degradation models used in the EMR study should contain all necessary evolution information with time about the factors which are related with the EMC levels of integrated circuits. To facilitate the following EMR modeling, the degradation models could be represented as SPICE compact models with modifiable parameters expressed by mathematic function of aging time t (e.g. degradation ratio σ(t) in [BOYE13]), or equivalent circuit models with additional components which represent the aging impact. With the degradation models, we can get the model of components before and after aging, and then these models could be implemented directly in electronic simulation tools like SPICE.

- EMC modeling of ICs and electronic blocks

The EMC modeling process is discussed in the previous section. Depending on the EMC tests, different EMC models could be proposed respectively for emission and susceptibility levels. The EMC models are created for both fresh and aged circuit, based on the model library of components and the test environment models. The degradation impacts are presented by the difference of the degraded components' models before and after aging process. Normally, the EMC model structure does not change during the aging process, and the test environment (test bench, test PCB) keeps the same before and after aging.

Once the tested ICs are produced and available, it's better to validate the fresh EMC models with experimental measurements. Then the EMC drifts could also be verified by the measurements under the stress tests. The objective is that the prediction of long-term EMC levels can achieve a satisfactory accuracy with the correct models and modeling methods.

- Black box modeling

The modeling of EMC should consider the intellectual proprietary protection about the circuit design, and also for the degradation models. So the black box modeling mentioned in the previous section could be a good approach.

- Statistical analysis

The statistic information, like the dispersion of impact of aging between different samples, could be an additional factor in the model to predict not only the EMC drift value, but also the long-term distribution of EMC level and reliability probability related with EMC levels. The statistical aspects in EMR study will be discussed in the next chapter.

The EMR modeling process will be detailed in the following case studies.

IV.5. Case study 1: Prediction of aging impact on EMI of an operational amplifier

As a common electronic block, the operational amplifier (opamp) is very susceptible to external electromagnetic interference. The coupling of EMI on opamp inputs and power supply leads to a distortion of the output voltage, especially the generation of a voltage offset on its output which is harmful and hard to remove. The generation of offset is explained in detail in numerous research studies, such as those of of Fiori and Redoute [FIOR02] [REDO10]. This offset could be explained by the asymmetric slew rate for low to medium EMI frequencies. While at higher EMI frequencies, the EMI is filtered by the parasitic capacitances of the input stage, the DC shifts caused by RF interferences are no more related with slew rate but with the parasitic capacitances and the nonlinear behavior of the differential pair [RICH14].

In this case study, we define the EMI level by the output offset voltage. With the aging stress injected in the amplifier, a worse DC output offset value could be observed, that means the device becomes more susceptible to the EMI with the aging. So the prediction of EMS evolution of operational amplifier is important to help the IC designers to prevent EMC failure during the ICs' lifetime. This case study aims at demonstrating the impact of aging on electromagnetic susceptibility of an operational amplifier, and the practice of the EMR prediction method of the aging impact in Figure IV-34. Firstly the experimental set-up and the aging process are presented briefly. Then the measurement results are shown and analyzed. Finally, the modeling process of the EMI levels against conducted interferences with aging time is presented.

IV.5.1. DUT and experimental set-up

IV.5.1.1. Device under test

The operational amplifier under test is embedded in a test chip ELMER22 designed in Freescale® CMOS 90-nm process. The structure of this amplifier is illustrated in Figure IV-35. It is a simple Miller operational amplifier with a P-channel differential pair, in order to accept a common mode-voltage down to zero. The bias voltage of the opamp is defined by an external resistor, and the output terminal (V_{out}) is an amplified copy of the voltage difference between the two input terminals (V_+ and V_-). The nominal power supply voltage is 3.3 V.

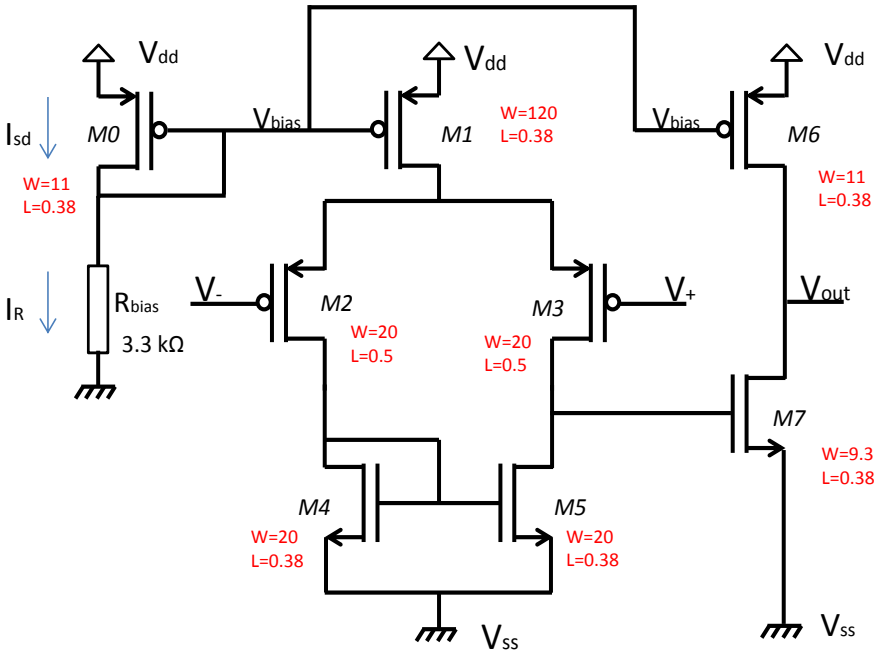


Figure IV-35 Operational amplifier structure under test

IV.5.1.2. Immunity test configuration

A test board is designed for the immunity test, as shown in Figure IV-36. We use a socket to measure different samples in the same configuration. Except the conducted immunity test, this test board lets the possibility for the future TEM cell measurements for radiated immunity.

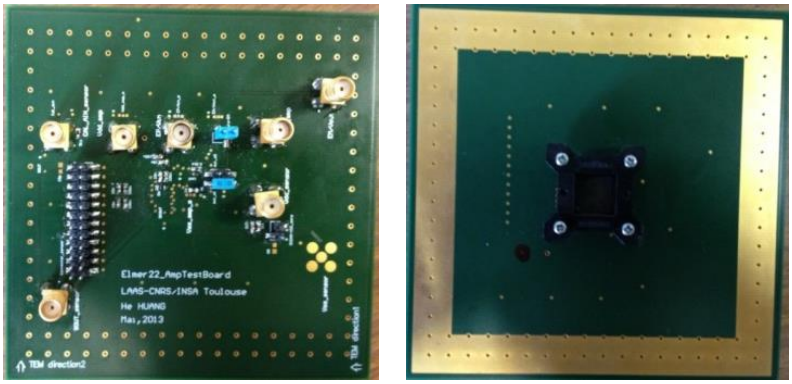


Figure IV-36 PCB test board for ELMER22 test chip

DPI conducted immunity measurement configuration is selected in this test. As described in Figure IV-37, the operational amplifier is in voltage-follower configuration, because this topology maximizes the susceptibility to EMI [MASE96]. Normally, if there is no disturbance injected in the input terminal of a voltage-follower opamp, the output will track the input voltage from 0.2 V to 3.1 V. The harmonic disturbances are produced by a RF signal synthesizer followed by a RF power amplifier, and they are superimposed to a constant voltage equal to 1.2 V and applied to the input of voltage-follower. The injected power is sensed with a directional coupler and a power meter. Both

input and output voltage waveforms are observed with a 2 GHz digital storage oscilloscope equipped with 2.5 GHz active probes. The evolution of the EMI-induced DC offset on opamp output is measured according to the different EMI amplitude and frequency. The AOP is powered by a DC power supply 3.3 V. The range of test frequency is from 10 MHz to 1 GHz. For the DPI test, we defined a threshold of output offset ±0.1 V as the failure. Besides, the output offsets with different frequencies and amplitudes of RF interference injected in the input of the amplifier are also measured.

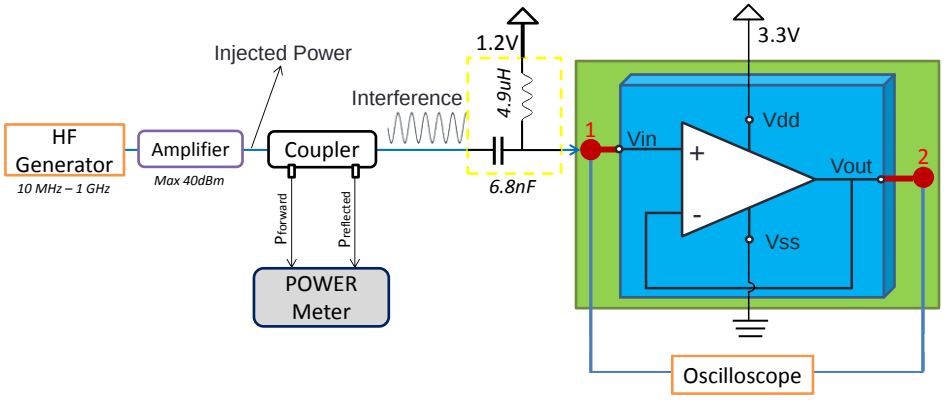


Figure IV-37 Experimental setup for the susceptibility analysis of the amplifier

In addition, several key parameters of the amplifier are also measured, like the bias voltage which defines the bias current of the differential pair, and the slew rate (SR) of the output voltage, which play an important role in the DC offset generation at low and middle frequencies [REDO10].

IV.5.1.3. Accelerated aging test

Because of the use of IC socket which is not tolerant to high temperature, the thermal aging stress is not selected in this study. We choose the electric stress as the accelerated aging stress. This aging stress is simple to apply, and the degradation mechanisms in silicon level (soft degradation) could be produced with this accelerated aging stress. The voltages of each pin of the chip during the stress test are listed in Table IV-3.

Table IV-3 Voltage values of test chip pins during the aging test

Pin name	Voltage	Description
V_{dd}	6V (5.5V)	Source terminal (Body terminal) of M0 and M6
V_{bias}	0V	Gate terminal of M0 and M6; Drain terminal of M0
V_{out}	0V	Drain terminal of M6
V_{ss}	0V	GND
V_+ and V_-	6V (5.5V)	Isolation for the differential pair

As shown in Figure IV-38, the aging stress is applied from the limited external IC pins. The power supply voltage V_{dd} is risen to accelerate the aging of the opamp, and V_{ss}, V_{out} and V_{bias} are connected to the ground. Besides, the V+ and V- terminals are also connected to same power supply voltage of V_{dd} to block the differential pair (no current in the differential pair). To specify the aging effect and to simplify the stress analysis and modeling, the aging stress is localized in certain parts of op-amp. Only certain MOSFETs are aged under a fixed electric condition, and other parts of op-amp are isolated from the aging stress. The selected aged transistors are located in bias stage and output stage, respectively, which are strongly related with the output offset. According to the voltage analysis of each transistor, two P-channel MOSFETs (M0 and M6 in Figure IV-38) of the same size (length and width) are the most affected by the aging stress. The aging condition of these two transistors is illustrated in Figure IV-38. The voltage stress is over the nominal functional voltage of the MOSFET of 3.3 V. Two components (component #1 and #2) are aged under 6 V, and one other (component #3) is aged by applying 5.5 V to observe the effect of different aging condition. The aging stress is applied to the component in a separated aging test card, and then we use the test card in Figure IV-36 for the EMC measurement and other characterization.

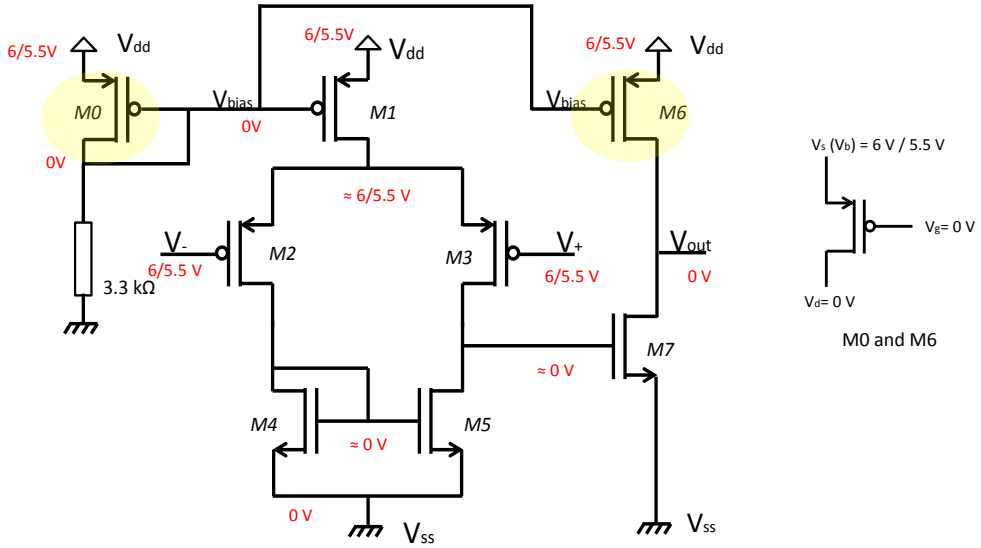


Figure IV-38 Voltage stress on each transistor of the amplifier

The component sockets are embedded in each card in order to facilitate the transposition between the aging test and characterization. The opamp are aged for 1000 minutes. The stress conditions are interrupted regularly (e.g. after 1 minute, 2 minutes, 5 minutes...) in order to measure the evolution of the opamp parameters and the output offset voltage induced by the external conducted RF interference while the opamp operates under a nominal power supply of 3.3 V. In addition, all the experimental manipulations, including the accelerated aging test, are applied under room temperature (between 20 and 26 °C). According to the degradation analysis of transistors in Chapter III, the high drain-source and gate-source voltages of both P-channel MOSFETs accelerate degradation mechanisms such as Hot Carrier Injection (HCI) and Negative Bias Temperature Instability (NBTI).

They could result in the increase of threshold voltage, the decrease of mobility, trans-conductance and drain current [HUAR07].

IV.5.2. Measurement results

Here firstly the evolution of two electrical parameters which are related with the output offset values is presented. And then the EMI drifts induced by aging are demonstrated.

IV.5.2.1. Evolution of the electrical parameters of the opamp during aging

As two important parameters of the op-amp related to the output offset voltage, the bias voltage Vbias and the output slow rate SR are measured during the aging process.

The bias voltage for the differential pair is defined by a P-channel MOSFET with an external resistance, as shown in Figure IV-35. The bias voltage could be approximately calculated by Equation IV-16 with simplified small-signal equivalent circuit models of the MOSFET before the aging test to analyze the possible future evolution of AOP. In this equation, the number of current/voltage is the transistor numbers in Figure IV-35 (here is M0).

$$I_{sd0} = \frac{W_0}{L_0}\mu C_{ox}\,(V_{sg0} - V_{th0})^2 = \frac{W_0}{L_0}\mu C_{ox}\,(V_{dd} - V_{bias} - V_{th0})^2 = I_R = \frac{V_{bias}}{R_{bias}} \qquad \text{Equation IV-16}$$

With the predicted increase of the threshold voltage V_{th} of the PMOSFET induced by aging stress, the calculation results demonstrate that V_{bias} decreases gradually during the aging process. As shown in Figure IV-39, the bias current is intersection of curves I_R and I_{sd}. With the increase of threshold voltage V_{th} of M0, V_{bias} decreases.

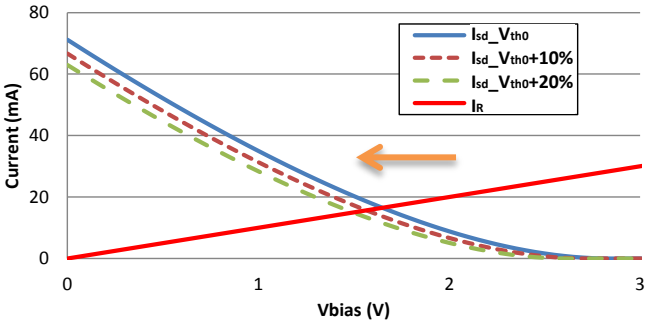


Figure IV-39 Simulation of bias voltage evolution with the aging time

Another parameter is the output slew rate. The slew rate is defined as the maximum rate of change of output voltage per unit of time and is expressed as volt per second. As explained in Figure IV-40 (a), the op-amp is in voltage follower configuration, and a square wave of 0.2 V – 2.2 V with a frequency of 3 MHz is applied at the input side of the voltage follower. The input and output waveforms are observed with the oscilloscope (Figure IV-40 (b)) and the value of slew rate (20 % - 80 %) of the output signal is also measured directly by the oscilloscope.

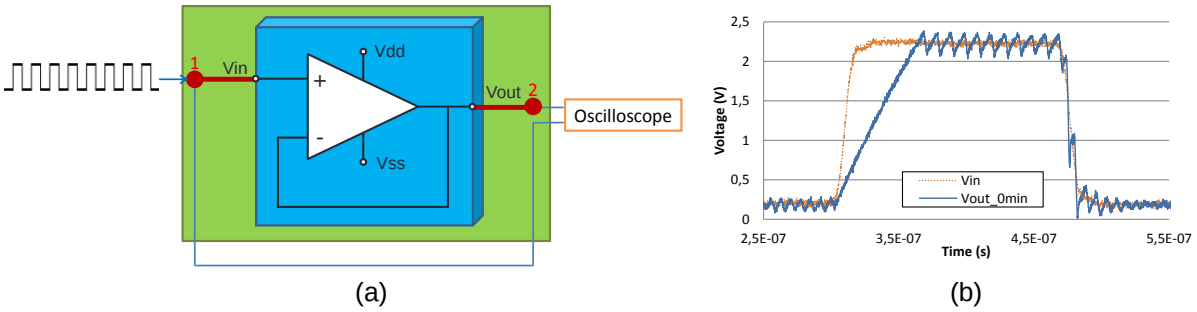


Figure IV-40 Slew rate measurement: (a) Experimental set-up; (b) Output slew rate measurement result by oscilloscope, component # 2 fresh

According to the former study like [MASE96] and [REDO10], the slew rate asymmetry plays a key role in the output offset generation for low to medium frequencies of EMI injected in the input side of amplifier, because the asymmetric slew rates can cause even-order nonlinear distortions. Where when the SR+ is larger than SR-, the output offset is positive, and when SR+ is less than SR-, the output offset is negative. Because of the inequality of positive and negative slew rate, the charge and the discharge paths are not equal to each other. One example of positive offset case related with the slew rate asymmetry is shown in Figure IV-41.

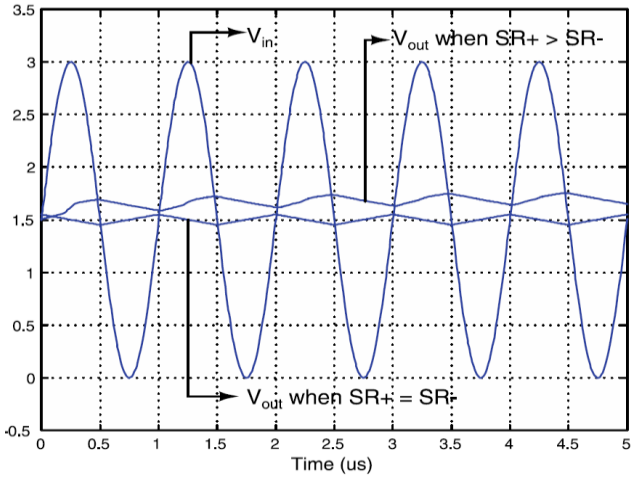


Figure IV-41 Effect of unequal slew rate in a basic op-amp [REDO10]

For the device under test in our study, according to the measurements shown in Figure IV-39, the positive SR (SR+, around 35 MV/s) is much smaller than the negative SR (SR-, around 200 MV/s), so the output offset is negative. The slew rate is related with the saturation current and the load capacitance value C_{out} of the output stage [REDO10]. For the positive slew rate, this saturation current is the saturation source-drain current I_{sat6} of transistor M6, it could be calculated according to Equation IV-17.

$$SR+= \frac{I_{sat6}}{C_{out}} = \frac{\frac{W_6}{L_6}\mu C_{ox}\,(V_{sg6}-V_{th6})^2}{C_{out}} = \frac{\frac{W_6}{L_6}\mu C_{ox}\,(V_{dd}-V_{bias}-V_{th6})^2}{C_{out}} \qquad \text{Equation IV-17}$$

M0 and M6 have the same sizes ($W_0 = W_6$ and $L_0 = L_6$). Except the differences related to process variations within the same circuit, their electrical characters are also assumed identical, that means they have the same threshold voltage ($V_{th0} = V_{th6}$). According to Equation IV-16 and Equation IV-17, we have an estimation of the value of SR_+ with Equation IV-18. Since the simulation of the impact of stress induced on M6 shows the V_{bias} decreases (Figure IV-39), so SR_+ is also estimated to decrease during the aging test.

$$SR_+ = \frac{I_{sd0}}{C_{out}} = \frac{(\frac{V_{bias}}{R_{bias}})}{C_{out}} \qquad \text{Equation IV-18}$$

The experimental measurements of these two parameters confirm the estimation by calculation. For example, the SR_+ decreases over the aging process, as illustrated in Figure IV-42. The output stage reacts more and more slowly to the input switching because of the aging stress.

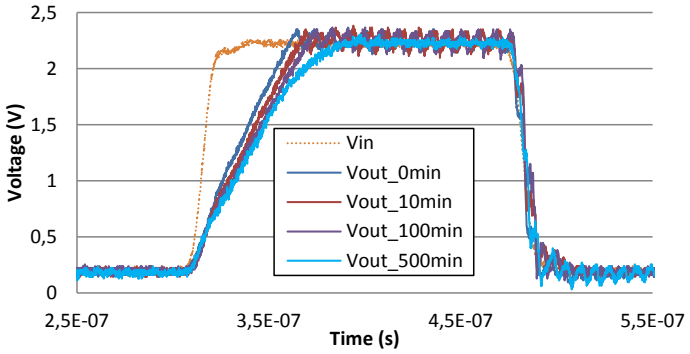


Figure IV-42 Slew rate measurements with aging time illustrated by oscilloscope: V_{in} and V_{out}, component #3

The measured evolution of the bias voltage and positive slew rate during the aging is presented in Figure IV-43. Here three tested samples are numbered #1, #2 and #3, and the dashed curves in two figures are the trend line of experimental data. Though the parameters initial values of the devices are different because of the dispersion between the test chips, all these results reveal a decrease trend of both the bias voltage and positive slew rate after aging.

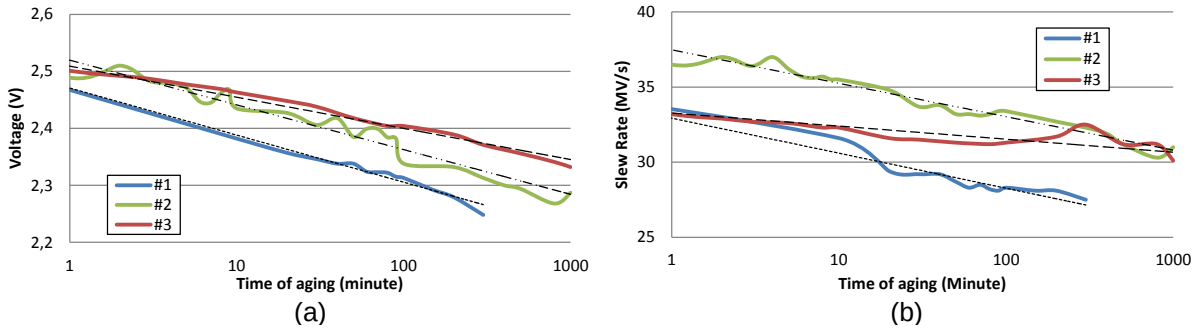


Figure IV-43 Evolution of opamp parameters during the aging of three samples (#1, #2 and #3): (a) Bias voltage; (b) Positive slew rate (SR_+) in the output

The evolutions of these both parameters are resumed in Table IV-4. The parameters' variation of each component is expressed by a trend line with the form y = A · ln (t) + B, where y is the tested parameter, t is the aging time in minute, A is the evolution coefficient which could demonstrate the evolution speed and B is defined by the initial value. As the voltage stress of component #3 (5.5 V) is less than the other two devices (6 V), the evolution coefficient A of component #3 is smaller than that of two others, that means the parameters decrease less fast during the aging process.

Table IV-4 Evolution of opamp parameters

Parameter	Comp. No	Stress voltage	Initial value	Trend line
Bias voltage (V)	#1	6 V	2.553	y = -0.036 ln (t) + 2.472
	#2		2.577	y = -0.035 ln (t) + 2.525
	#3	5.5 V	2.546	y = -0.025 ln (t) + 2.515
SR+ (MV/s)	#1	6 V	35.3	y = -0.991 ln (t) + 32.84
	#2		39.6	y = -0.974 ln (t) + 37.51
	#3	5.5 V	35	y = -0.307 ln (t) + 32.96

IV.5.2.2. Evolution of electromagnetic susceptibility

The worst immunity levels are observed after aging for most tested frequencies. The DPI test results of two components under different stress level (Component #2 under 6 V, and Component #3 under 5 V) before and after aging are shown in Figure IV-44. Here the immunity criterion is defined as the offset should not exceed ± 0.1 V. As the component #2 is under a higher voltage stress, so we can observe that its EMI variation is larger than that of #3. One problem of DPI test is the dispersion of measurement data. The standard deviation of injected power in the measurement is around 1 dB.

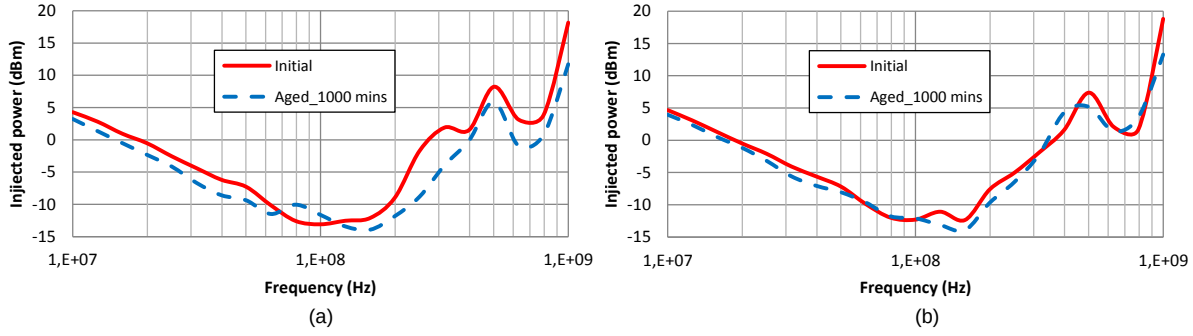


Figure IV-44 Susceptibility level by DPI test before and after aging of two components: (a) #2 and (b) #3

Besides, the evolution of the DC output offset of component #3 during the aging process at 6 tested frequencies is shown in Figure IV-45, where the incertitude of measurement of offset is about

±0.02 V. Except at 50 MHz and 100 MHz where the variation are very small, a global gradual falling trend is observed during the aging process for test frequencies, which means that after aging the same EMI produces a larger DC offset in the output, or a less powerful EMI is sufficient to provoke the same DC output offset. For example, at 10 MHz, about 0.6 dBm less injected power could produce the same offset (like -0.1 V) after aging. At 200 MHz, a larger offset (about 0.05 V more) could be observed in the output for the same injected power. In the low frequency range (e.g. 10 MHz), the increase of output offset could be explained by the decline of SR_+ which is observed by the measurement.

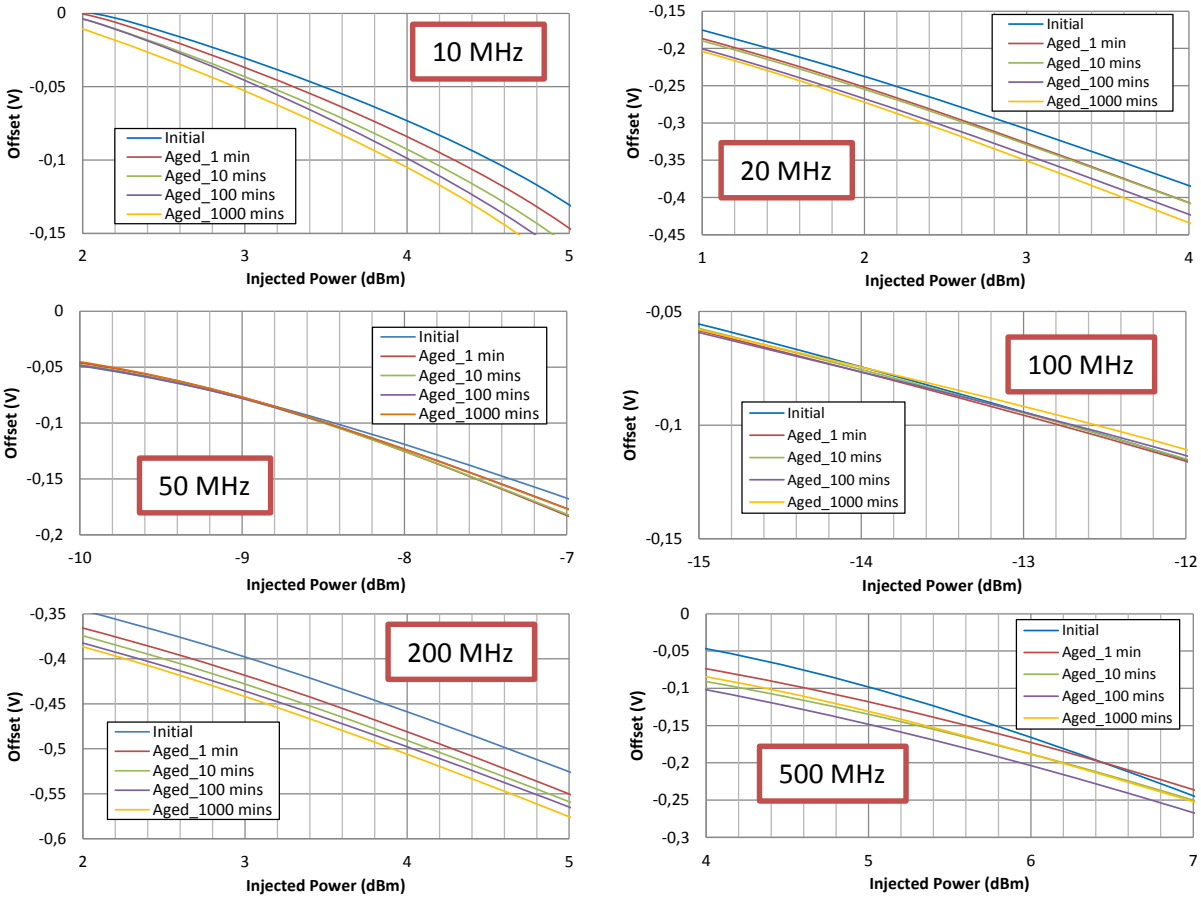


Figure IV-45 Evolution of the DC output offset during the aging process of component #3

The input and output waveforms before and after at 10 MHz observed by oscilloscope are shown in Figure IV-46. With the decrease of positive slew rate, the output capacitor charge less fast, and the output voltage needs more time to reach "high" level, so a decrease of DC offset could be observed. The exception in 50 MHz and 100 MHz could be explained by a resonance in the system around 80 MHz which could be observed in the waveform of output signals in Figure IV-46. Two other components demonstrate the similar evolution of offset after aging, as #3 has the most tested frequencies of output offset, so it is chosen to be presented here.

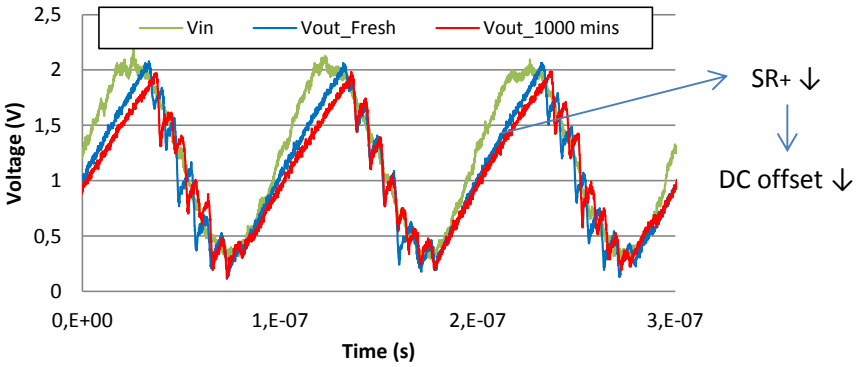


Figure IV-46 Waveform of output signal with a RF disturbance injected in input (Component #3)

IV.5.3. Long-term immunity prediction

As presented in the EMR IC modeling flow (Figure IV-34), the long-term immunity prediction model contains two parts: a model of the susceptibility of the circuit and a model which integrates the aging effect of devices. All the simulations are based on SPICE and performed with Agilent's Advanced Design System (ADS). As one sample #3 has more test points in interference frequencies of output offset than other two samples, so it is chosen to demonstrate the modeling process.

IV.5.3.1. Susceptibility model

As demonstrated in Figure IV-47, the structure of the susceptibility model relies on ICIM standard proposal [IEC 62433-4] which comprises two parts: PDN and IB.

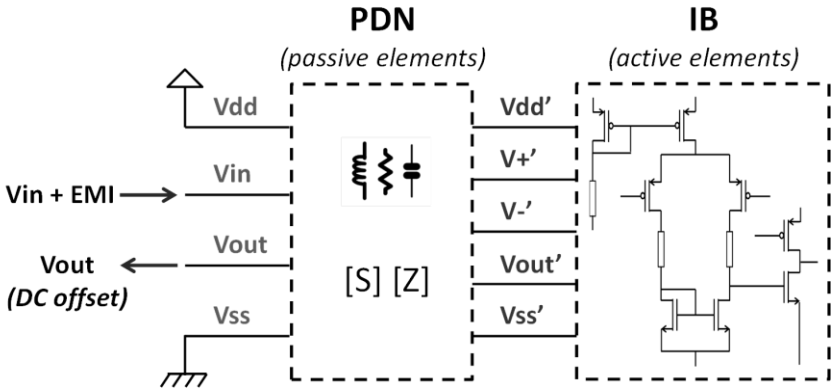


Figure IV-47 Simplified susceptibility model of opamp

The Power Distribution Network (PDN) block describes the coupling path of the EMI to the injected nodes of the opamp (the package, interconnectors and coupling between pins). These elements are extracted by S-parameters measurements. A PDN network with 4 terminals (V_{dd}, V_{in}, V_{out} and V_{ss}) is constructed, as illustrated in Figure IV-48 (a). The PDN structure is built based on the proposed models in some former studies [LI11] [WU14] which study the other blocks of the same test chips and the VNA measurement data. An example of the PDN structure between the V_{dd} and V_{ss} is depicted in Figure IV-48 (b).

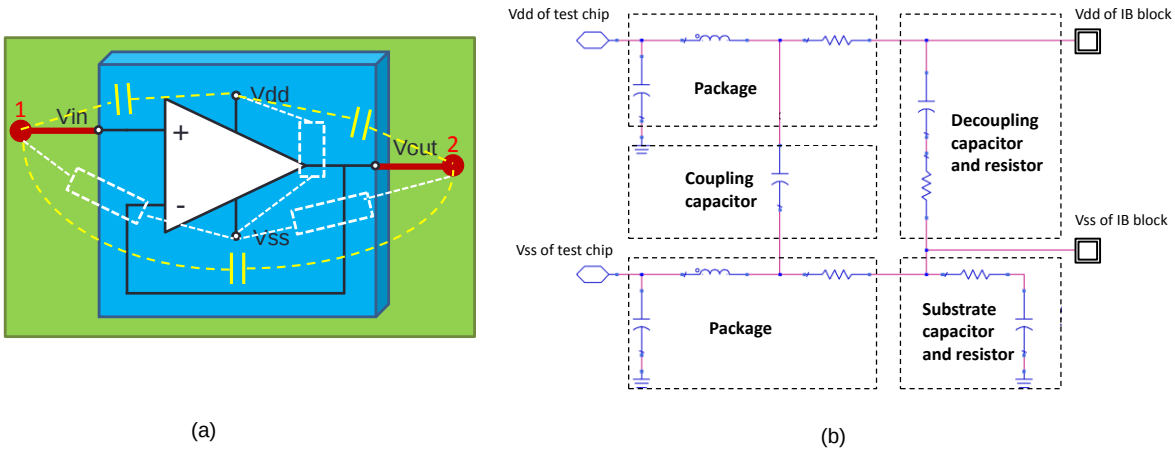


Figure IV-48 PDN structure: (a) PDN network of the op-amp mounted in follower configuration; (b) PDN structure example between Vdd and Vss

Besides, the PCB tracks and the interconnections are also taken into account in this PDN network. The PDN structure example between Vdd and Vss including the PCB part is shown in Figure IV-49. Except the component part, the PDN model consists of the connector, PCB tracks and the socket for the component. In this study, the PCB tracks are extracted with the "Interconnector parameters" tool in IC-EMC, based on the form, the size, the working frequency range and the other information of the PCB tracks. The models of the connector and the socket are based on the library which has been built and verified in the former studies like [LI11] and [WU14].

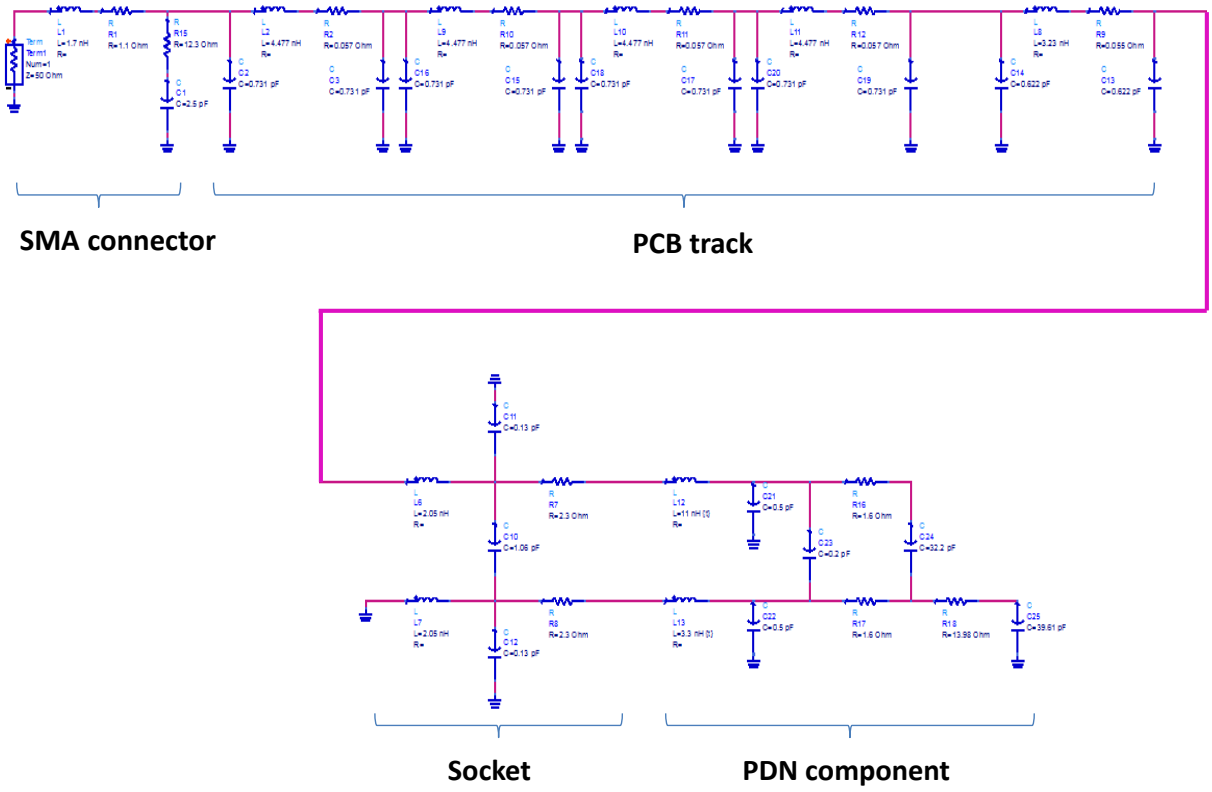


Figure IV-49 PDN structure example between Vdd and Vss including the PCB part

The PDN modeling results of the impedance between each component pins are demonstrated Figure IV-50. According to the comparison between the simulation and the measurement, although some differences could be observed, especially in the high frequency range which is related with the complex parasitic elements, the modeling results (in red) demonstrates a good fitting with the experimental measurements (in blue) between 1 MHz and 500 MHz.

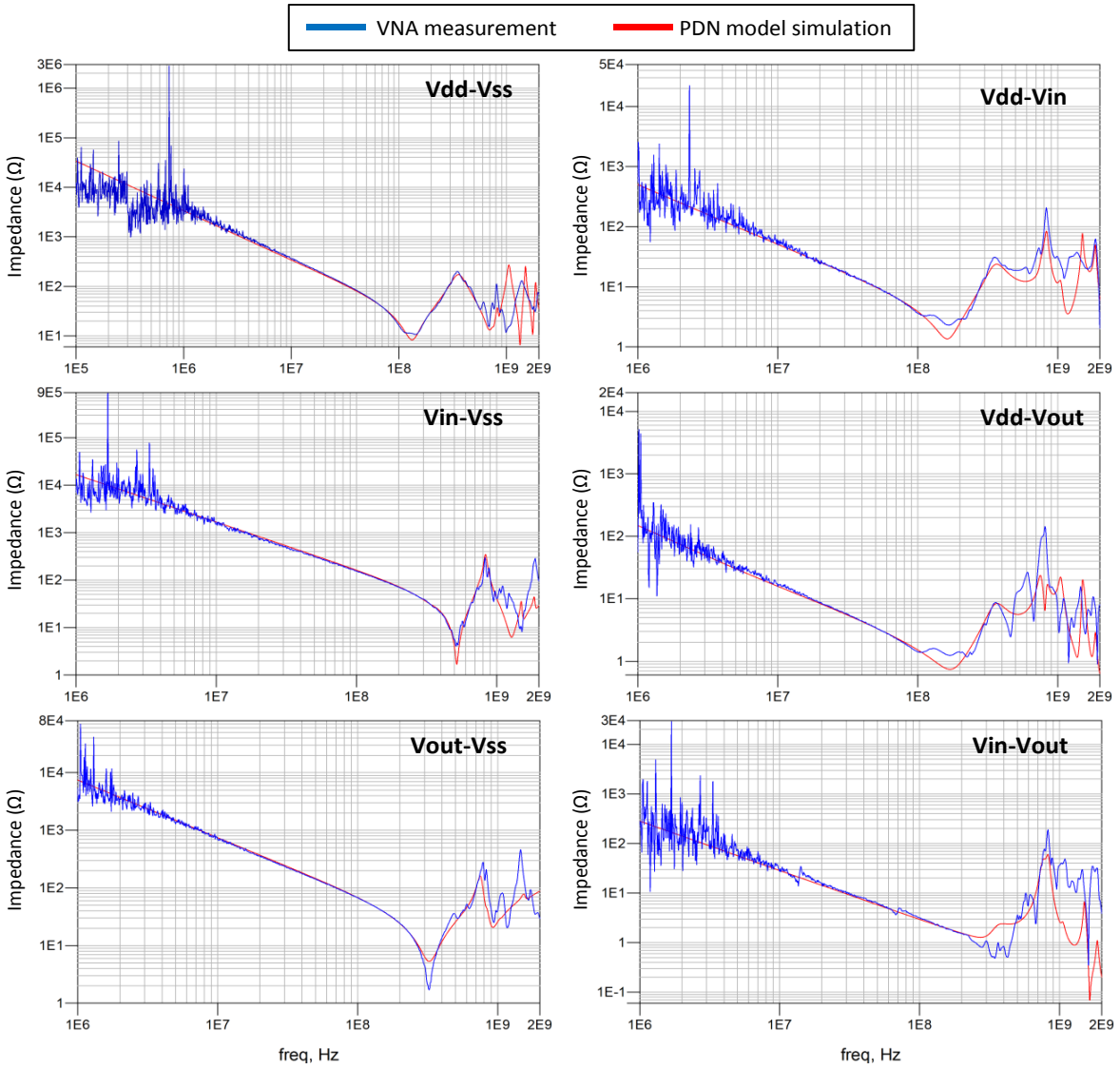


Figure IV-50 Comparison between the VNA measurement and the PDN model

Besides, the output of the immunity model is the offset level with different disturbance, but not direct failure detection. As a result, the Internal Behavior (IB) block models the operation of opamp and especially its reaction to electromagnetic disturbance. This block consists in the transistor netlist of the opamp. The schematic of the internal construction is obtained from the data sheet of the test chip provided by manufacturer. Besides, the transistor models are extracted from the former studies in [LI11] which studied the other blocks of the same test chip, which are the Spice level-3 model which has been presented in III.3.3.2.

In addition, the power injection track from the RF generator to the PCB card is described in Figure IV-51, which consists of the model of the directional coupler, the bias card and the transmission cables.

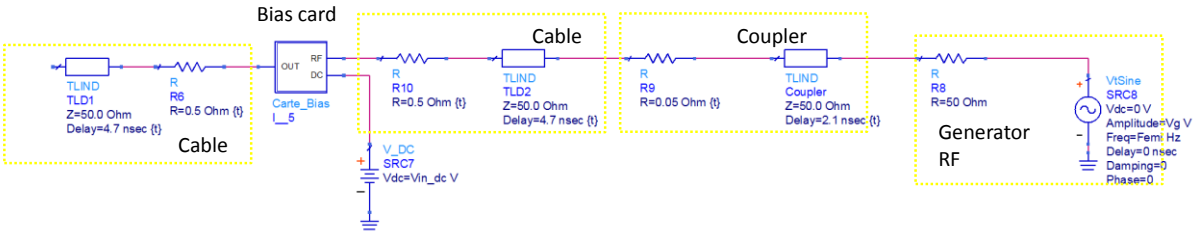


Figure IV-51 Disturbance injection model for the DPI measurement (from right to left)

The simulation of the output offset before aging is demonstrated in Figure IV-52 for 6 tested frequencies. Although we can observe the differences between the simulations and the measurements which might be related to the measurement errors and the simulation accuracy, the offset simulation results demonstrate a satisfactory correlation with the measurement points.

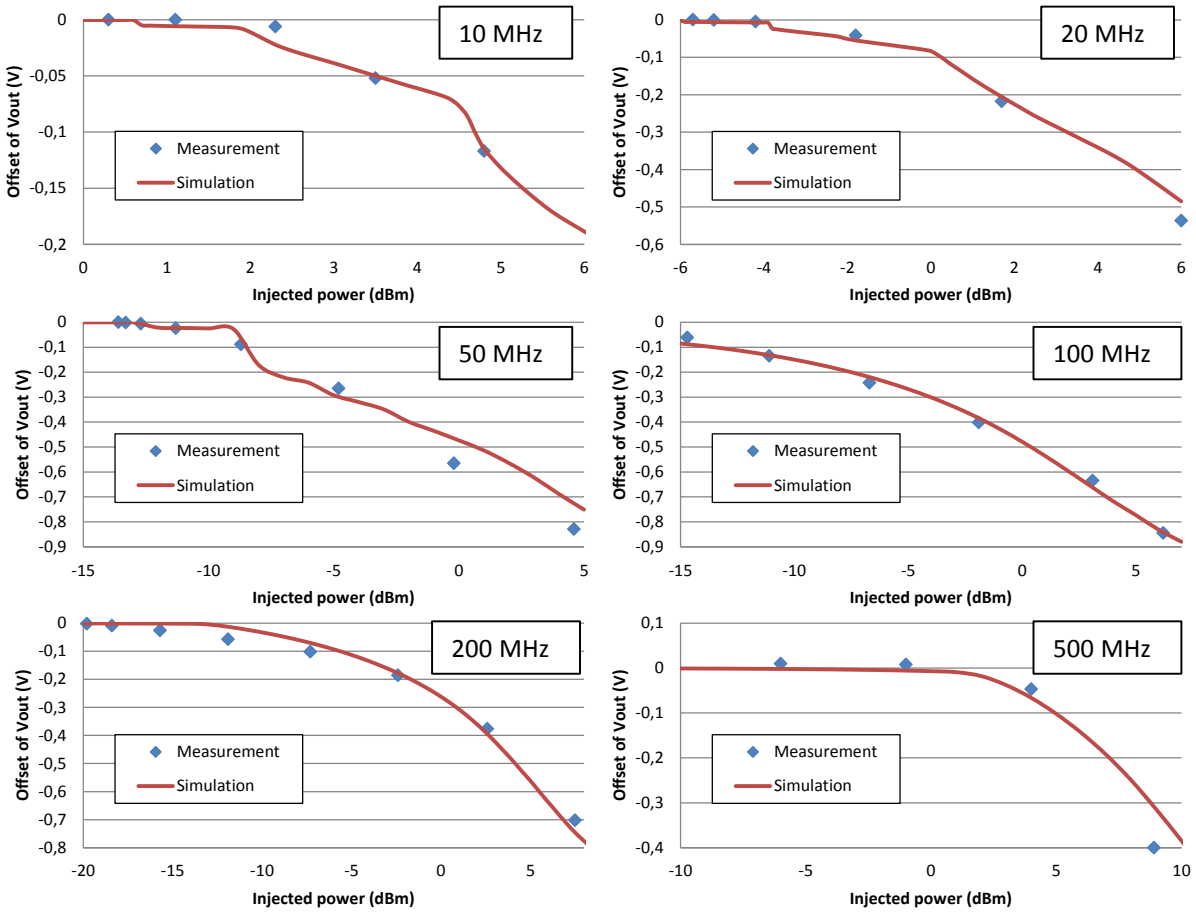


Figure IV-52 Comparison of the output offset between measurement and simulation before aging

The previous immunity criterion (the offset should not exceed +/- 0.1 V) is reused in the simulation. As shown in Figure IV-53, a good correlation of the susceptibility level before aging is observed between the measurement and the simulation up to about 500 MHz because of a limit of

PDN accuracy shown in Figure IV-50. Although the precision of the model at higher frequency is not perfect, it predicts the correct trends. The GDM level of FSV between the simulation and the measurement is shown in Figure IV-54. The mean GDM of FSV is 0.3242, which is in the level "Good". As a result, we consider that this susceptibility model is satisfactory for the integration of aging impact in the following EMR modeling process.

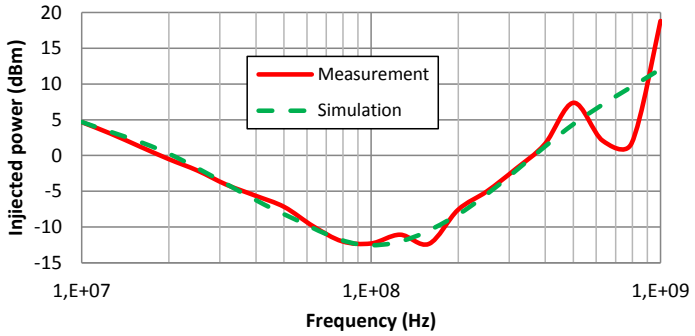


Figure IV-53 Comparison between measured and simulated susceptibility level before aging

Figure IV-54 GDM confidence histogram for the comparison of the simulation and measurement results in Figure IV-53

IV.5.3.2. Aging effect model

An example of the impedance measurement between V_{in} and V_{out} pins before and after aging is shown in Figure IV-55. The aging effect is included only in the IB block as the PDN measurements do not show any change after aging.

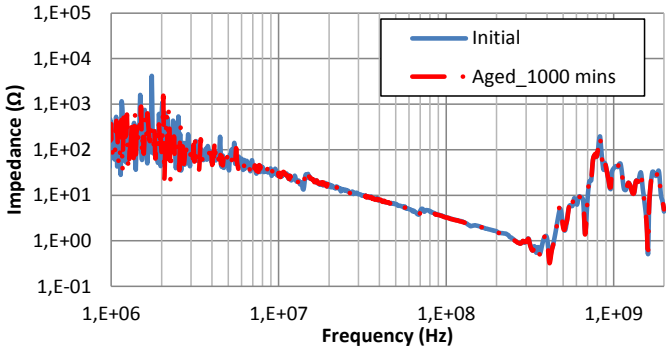


Figure IV-55 Impedances between V_{in} and V_{out} pins before and after aging

As explained below, the high V_{ds} and V_{gs} voltages in Figure IV-38 applied on P-channel MOSFETs accelerate the degradation. The degradation mechanisms activated by this stress are mainly the Negative Bias Temperature Instability (NBTI), and also Hot Carrier Injection (HCI) [HUAR07] [LI11]. They result in the variation of several parameters in the transistor model, such as increase of threshold voltage, the decrease of mobility and trans-conductance. With the help of SPICE simulations (Figure IV-56), the variation of threshold voltage shows a much more important role in the offset generation than the other parameters. So in our case study, only the threshold voltage is set as the parameter which is affected by aging and the effect on the other parameters are neglected.

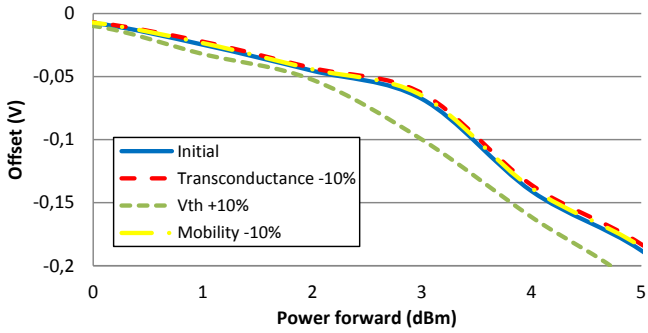


Figure IV-56 Simulation test of offset drift with the variation of different MOSFET parameters

The threshold voltage of PMOSFET is extracted by simulation of the bias voltage stage (M0 and external bias resistor R_{bias} in Figure IV-35) from the measurement data of the bias voltage. We vary the threshold voltage parameter in the transistor model of M0 to simulate the bias voltage. The threshold voltage evolution with stress time is plotted in Figure IV-57. As expected in previous chapter, the threshold voltage increases with stress time according to an approximate power law dependence ($\Delta V_{th}(t) = A \cdot t^n$). Here the coefficient A is obviously related with the aging stress magnitude. The other coefficient n does not show a great difference between the samples, and its value is around 0.21. These results confirm the NBTI experimental results of P-channel MOSFETs in [LI11] where the tested transistors are designed in the same technology than our test chip. In the model extracted of [LI11], the same power law equation is used. Except the difference of coefficient A because of the different accelerated aging conditions, the n values of two samples in [LI11] are respectively 0.2018 and 0.2163, which are very close to the value extracted in our study.

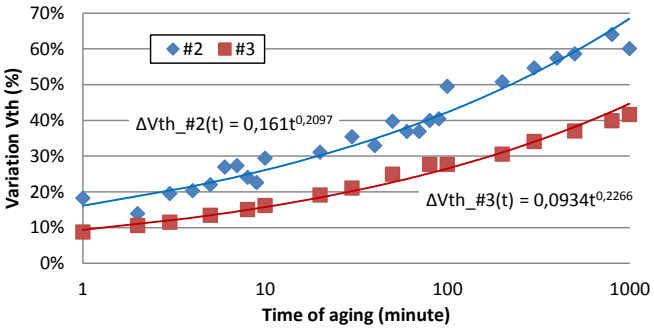


Figure IV-57 Threshold voltage shift during the aging time

IV.5.3.3. Long-term Susceptibility Simulation

In Figure IV-52, the susceptibility model of the converter has demonstrated a good fit with the measurement data before aging. As shown in Figure IV-58, to model the long-term susceptibility level, the threshold voltage variation with stress time ($\Delta V_{th}(t) = A \cdot t^n$) can be included in the transistor netlist so that the evolution of the susceptibility level according to the stress time can be simulated.

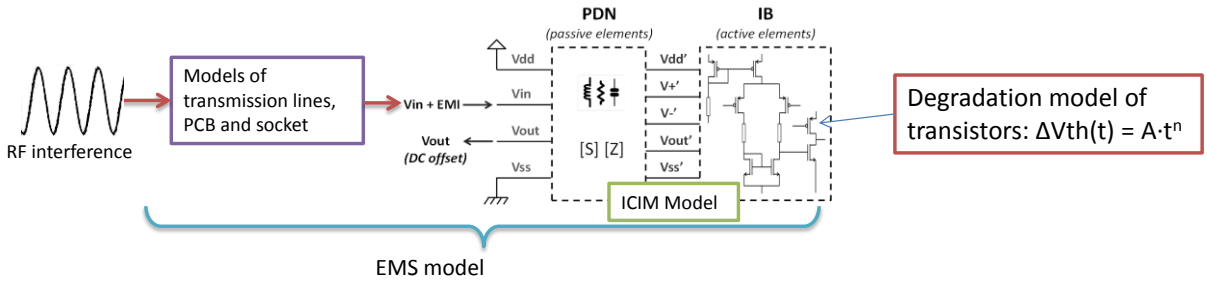


Figure IV-58 Long-term susceptibility model of the DC-DC converter

Similarly to the simulation results presented in Figure IV-53, the simulation results presented here also show an acceptable global fitting with the DPI measurement data after aging, especially at frequency below 100 MHz, as shown in Figure IV-59. Here the GDM confidence histogram between the simulation and the measurement is shown in Figure IV-60. Besides, the mean GDM of FSV analysis is 0.3427, which is also in the level "Good".

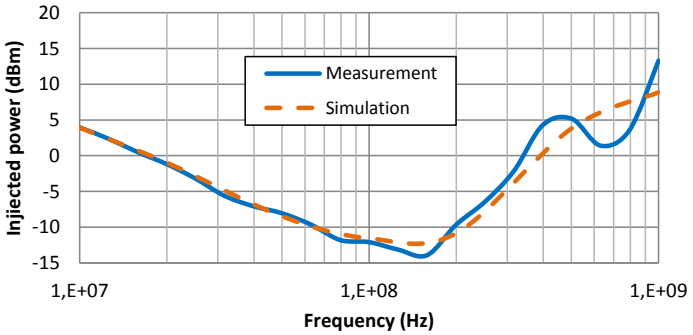


Figure IV-59 Comparison between measured and simulated susceptibility level after aging

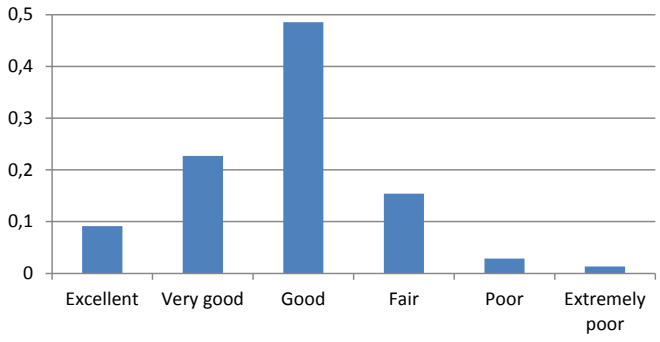


Figure IV-60 GDM confidence histogram for the comparison of the simulation and measurement results in Figure IV-59

Except the simulation of DPI test for the offset of 0.1 V, the simulation results of the output offset level before and after the aging of 1000 minutes at 6 tested frequencies are shown in Figure IV-61. Although some differences can be found between the simulation and the measurement, the simulation results demonstrate a good accuracy with the offset level of experimental data in most test frequencies, and the variations of offset induced by aging are also well simulated. Though the immunity drifts at certain frequencies like 50 MHz and 100 MHz do not fit well with the measurement results, the global reduction of immunity level drifts during the aging process is found at most tested frequencies by the simulation.

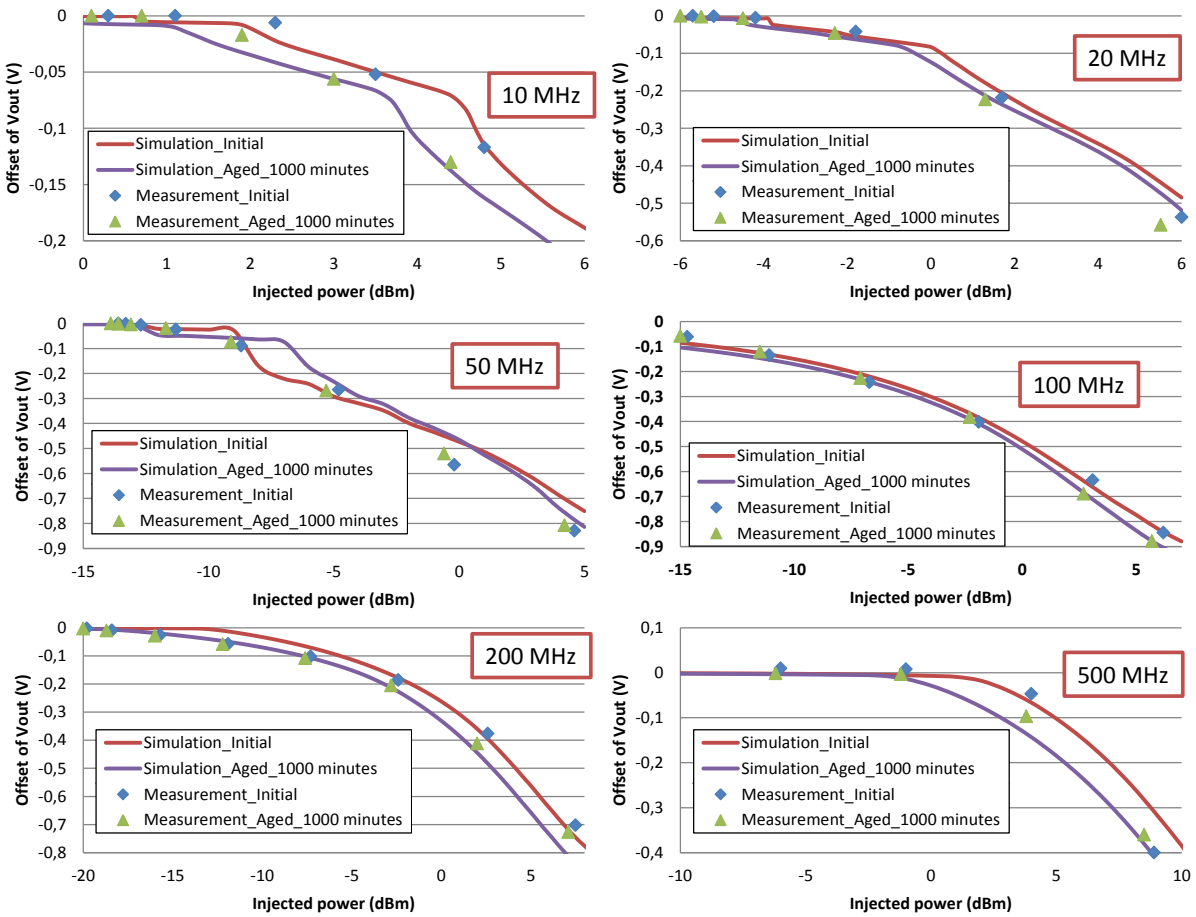


Figure IV-61 Comparison of the offset between the simulation and experimental data before and after aging at different frequencies

Besides, the gradual variation of offset at certain frequencies is also observed in the simulation. For example, the simulation results at 10 MHz and 200 MHz of different aging phase in Figure IV-62 confirm not only the offset level produced by the injected power, but also the gradual increase of DC output offset at these frequencies during the aging process.

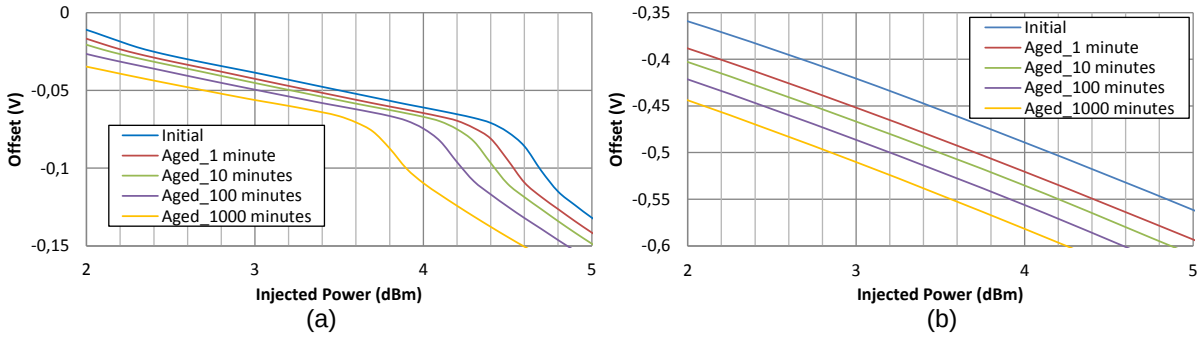


Figure IV-62 Simulated evolution of DC output offset during the aging process at two different interference frequencies: (a) 10 MHz; (b) 200 MHz

This long-term EMI simulation uses the susceptibility model injected with the degradation model presented by the variation of transistors' parameter. The susceptibility model and the degradation model are validated with the measurement data, respectively. The simulation results of the EMI evolution, especially the output offset, also demonstrate a good fit with the experimental data. However, some differences could be observed between the simulation and the measurement, which might relates with simplified degradation models as only one parameter V_{th} is considered, the accuracy of the transistor models, and the uncertainty of the measurement data (like ±0.02 V for offset voltage).

However, one weakness of this method is the use of the transistor netlist and the internal structure of the amplifier. As a result of the need of protection of intellectual property, one primary "black box" EMI model is proposed below.

IV.5.4. Black box modeling

IV.5.4.1. Description of the method

In the previous modeling process, the EMI model demonstrated a satisfactory accuracy with the measurement in most tested frequency. However, the internal structure netlist of the original circuit is used in the model. For the consideration of the IP protection, this model shall be used only for the manufacturer himself. If we do not want to reveal the internal information of the op-amp, the black box modeling method should be used to replace the model proposed above.

The offset analysis of the op-amp is applied when the op-amp is in a voltage-follower configuration. However, the negative feedback is realized by the connection between the output pin V_{out} and the negative input pin V- in the PCB level. As a result the first version of black box which considers the aging impact is proposed for the global voltage-follower in PCB level as demonstrated in Figure IV-63. The model consists in not only the circuit (ICIM block in Figure IV-58), but also the socket and PCB connection. Here only V_{in} and V_{out} are the terminals of the black box model. V_{dd} and

V_{ss} are considered as internal nodes, where their decoupling capacitors to V_{in} and V_{out} are considered inside the black box model.

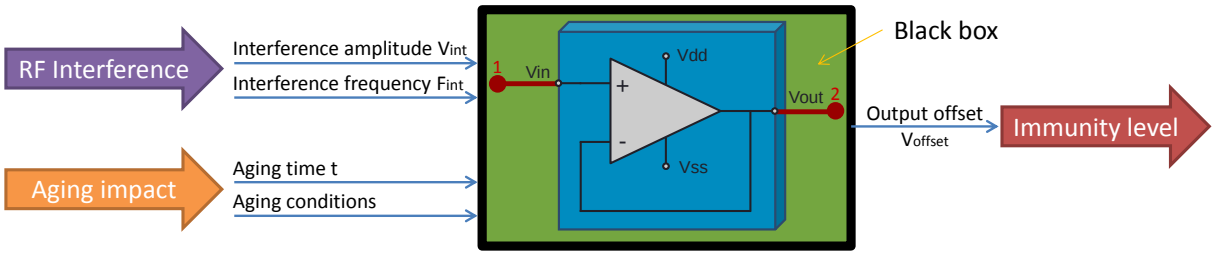


Figure IV-63 Architecture of the EMI black box of the op-amp in PCB level

As shown in Figure IV-63, the objective of this black box EMI model is to simulate the EMI level induced by both EM interference injected in the input side V_{in} and aging impact on circuit, without any information about the internal IC netlist. The RF interference could be defined by two variables: the amplitude V_{int} and the interference frequency F_{int} of the interference in V_{in}. The aging impact can be defined by the aging conditions and the aging time t. As presented in last chapter, the aging conditions could have many possible combinations in very large ranges. Here we simulate one aging stress case already applied below in IV.5.1.3. The only one output of the black box is the output offset V_{offset}, which could be the representation of the system immunity level. As a result, the black box in the figure can be expressed by a function f_{bb} which contains three variables, as described in Equation IV-19.

$$V_{offset} = f_{bb}(V_{int}, F_{int}, t) \qquad \text{Equation IV-19}$$

To simplify the extraction of the equation, Equation IV-19 could be expressed by sub-equations $V_{offset.i} = f_{bb}(V_{int}, t)$ at frequency f_i. As the first model, 6 sub-equations at 6 tested frequencies are extracted below.

IV.5.4.2. Extraction of the black box model

Considering the model constructed in the simulation has a satisfactory accuracy, so the black box is constructed based on the simulation data. The primary extraction of the equations uses the linear regression (high order polynomials) in the curve fitting toolbox of Matlab, as demonstrated in Figure IV-64. Here the polynomial degrees for each variable are 3, and the fitting method we used in this tool is the least-squares fitting, as defined in Equation IV-20.

$$S = \sum_{i=1}^{n} r_i^2 = \sum_{i=1}^{n} (y_i - y_{i.model})^2 \qquad \text{Equation IV-20}$$

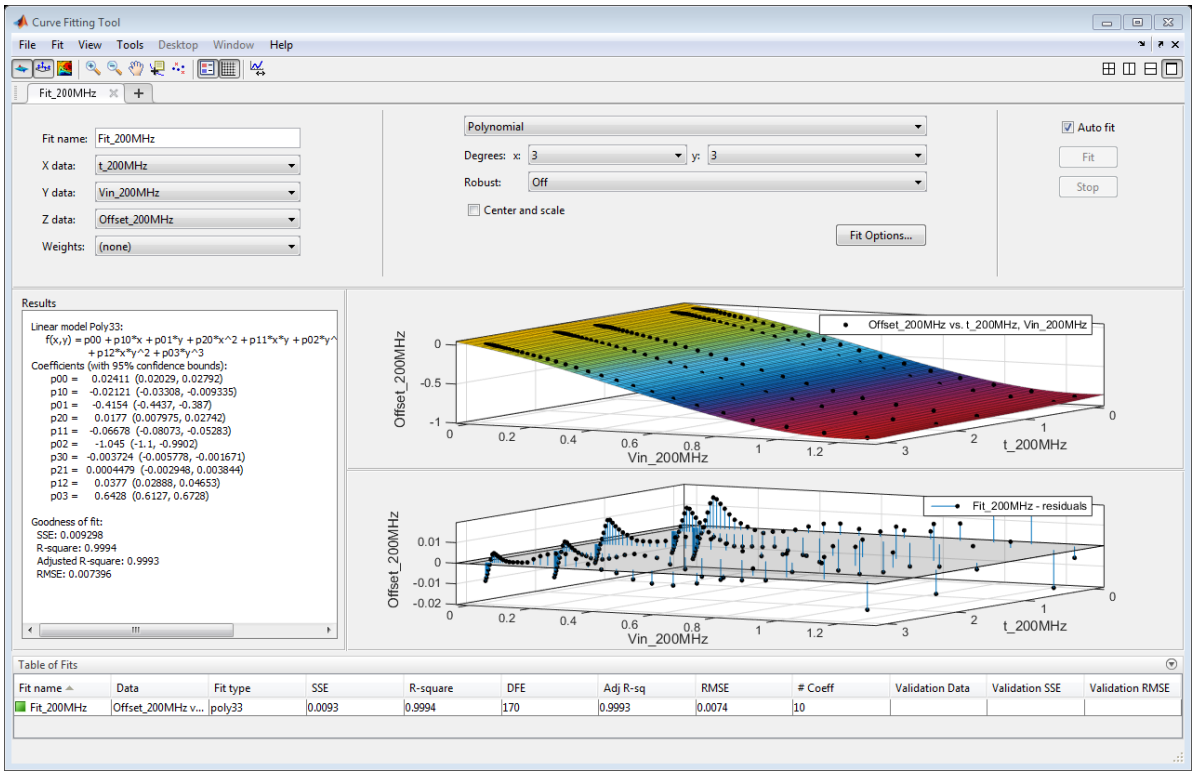


Figure IV-64 Curve fitting tool of MATLAB used to extract the black box functions

Where S is the summed square of residuals, r_i is the residual for the ith data, which is defined as the difference between the data sample y_i and the value in the model $y_{i.model}$. In the least-squares fitting method, the model is calculated to minimize the summed square of residuals S. There are also some other fitting methods, like Weighted Least Squares which has been also applied in [GAZD13], and Least absolute residuals (LAR) and Bisquare weights which are less sensible to outliers than least-squares [MOLE13]. The least squares fitting method is selected because of its simplicity and the sufficient good fitting level.

The modeling are applied with 100 samples in the (V_{int}, t) space for each tested frequency f_{int}. The range for aging time t is up to 1000 minutes. Besides, considering the aging time degradation is power law dependence (Figure IV-57), so here we define t'=log(t+1) to better cover the stress time range. Finally, we can obtain an approximate polynomial function at each frequency fi, as expressed in Equation IV-21. In this equation, there are totally 10 coefficients to be defined in the fitting process.

$$V_{offset.i} = p_{00} + p_{10}\cdot t' + p_{01}\cdot V_{int} + p_{20}\cdot t'^2 + p_{11}\cdot t'\cdot V_{int} + p_{02}\cdot V_{int}^{\ 2} + p_{30}\cdot t'^3 + p_{21}\cdot t'^2\cdot V_{int} + p_{12}\cdot t'\cdot V_{int}^{\ 2} + p_{02}\cdot V_{int}^{\ 3} \qquad \text{Equation IV-21}$$

The 10 coefficients of each frequency are resumed in Table IV-5. The quality of the fitting is concluded by a coefficient of determination R^2 and the root-mean-square error (RMSE) in the end of the table, which demonstrate the goodness of fit at each tested frequency.

Table IV-5 Coefficient of the fitting polynomial functions

Frequency	10 MHz	20 MHz	50 MHz	100 MHz	200 MHz	500 MHz
p00	-0,4729	-0,1385	0,1807	-0,006115	0,02411	0,1032
p10	0,0384	0,006775	0,0143	-0,02312	-0,02121	-0,04725
p01	1,888	1,154	-1,592	-0,7902	-0,4154	-6,409
p20	0,005359	0,002855	-0,01491	0,01387	0,0177	0,04753
p11	-0,1106	-0,04103	0,09504	0,002181	-0,06678	-0,9998
p02	-2,216	-2,789	0,8467	-0,2707	-1,045	-16,19
p30	-0,001182	-0,0007622	0,002597	-0,002563	-0,003724	-0,01056
p21	-0,001691	-0,001121	-0,003689	-0,003693	0,0004479	0,08671
p12	0,05838	0,02791	-0,104	-0,004555	0,0377	1,971
p03	0,6133	1,319	-0,1732	0,2741	0,6428	137,7
R^2	0.9891	0.9959	0.987	0.9999	0.9994	0.9848
RMSE	0.006864	0.009769	0.02981	0.002831	0.007396	0.0413

Except these 6 frequencies, more sub-equation $V_{offset.i} = f_{bb}(V_{int}, t)$ could be extracted based on the simulation results from the EMI model in IV.5.3.3. And then, a complete function of V_{offset} is extracted for all the test frequencies. This method could also be applied to extract directly the Equation IV-19 with three variables (V_{int}, F_{int}, t), but the complexity of proposed model will largely increase.

IV.5.4.3. Simulation of susceptibility evolution

To simulate the EM susceptibility evolution, we integrate the model "Black box" expressed by the Equation IV-21 in the global DPI test environment, as shown in Figure IV-65.

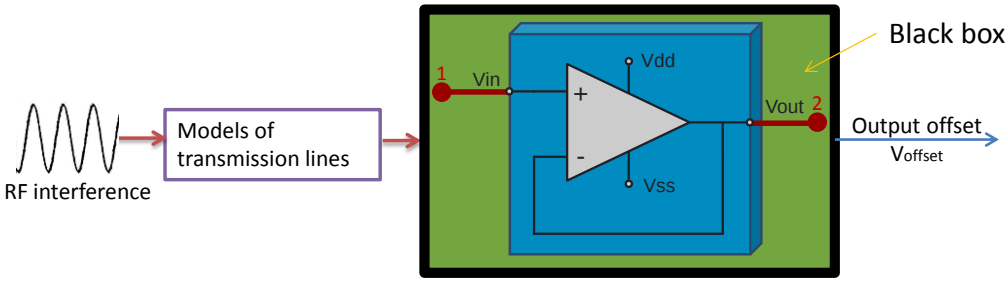


Figure IV-65 Long-term susceptibility "black box" model of the operational amplifier

Since the black box model is based on the simulation results in IV.5.3.3, the simulation results represent well the previous simulation results based on the netlist of circuit, as illustrated in Figure IV-66. The mean GDMs of FSV of the DPI simulation results between the two models (with and without netlist information) before and after aging are both in the level "Excellent", as shown in their confidence histograms in Figure IV-67. Except the frequencies modeled in Table IV-5, the EMI level at other frequencies are obtained by the linear interpolation. However, if we need the model more precise, we need to extract the model in more frequencies.

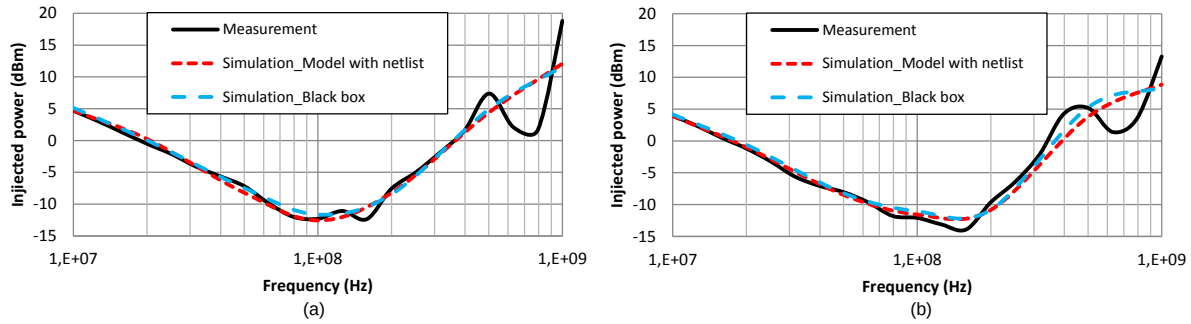


Figure IV-66 Comparison between measured and simulated susceptibility level by two models: (a) before aging; (b) after aging

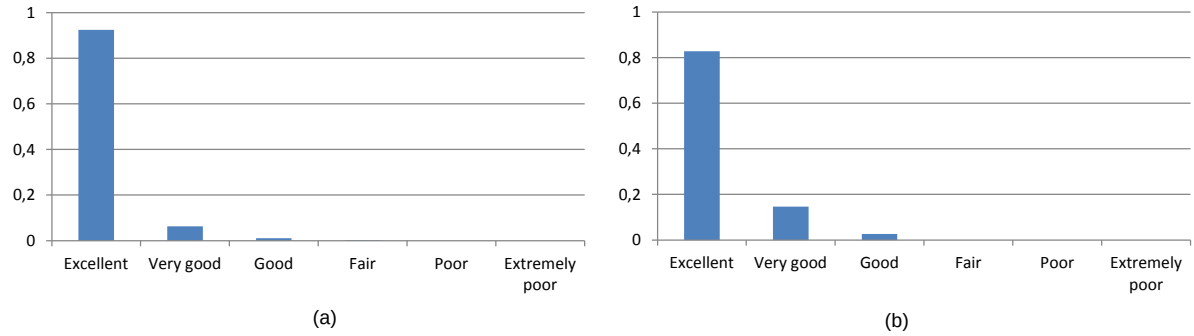


Figure IV-67 GDM confidence histogram for the comparison of the simulation results of two models: (a) before aging; (b) after aging

Besides, as demonstrated in Figure IV-68, with the variable aging time t in the black box block, the gradual EMI drifts induced by aging at certain frequencies are also well modeled.

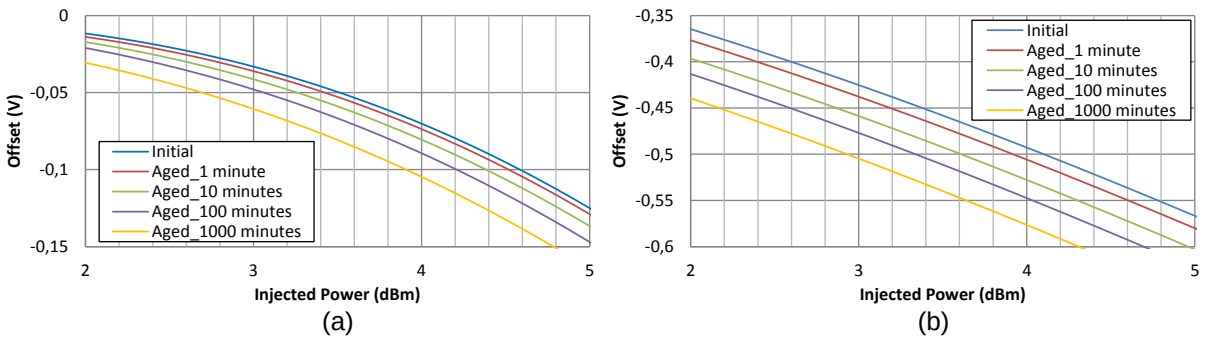


Figure IV-68 Simulated evolution of DC output offset during the aging process of different EMI frequencies with the black box block: (a) 10 MHz; (b) 200 MHz

This black box model could simulate the EMI level of the op-amp without the internal netlist information, and the time of simulation passes from about 12 seconds to less than 5 seconds at each test frequencies. However, the drawback is also very clear that the model is in a PCB level but not an IC level, so this model cannot be reused in other applications. To apply the model in other cases, the black box model of op-amp should be built in IC level. The black box modeling approach could be explained by Figure IV-69. In IC level, there is no more negative feedback, so the output V_{out} should be not only a offset but the waveform. Besides, the common-mode input voltage V_{com} and the differential-mode input voltage V_{dif} contain respectively the information of their amplitude, phase (of phase shift between V_{com} and V_{dif}) and frequency, which are all variables in the black box model. Besides, with an additional aging impact, the model will contains a large numbers of variables. As a result, too many parameters need to be extracted, and the characterization process and also the extraction time tend to become oversized. So this black box block in IC level is not studied finally, but it could be an interesting perspective work.

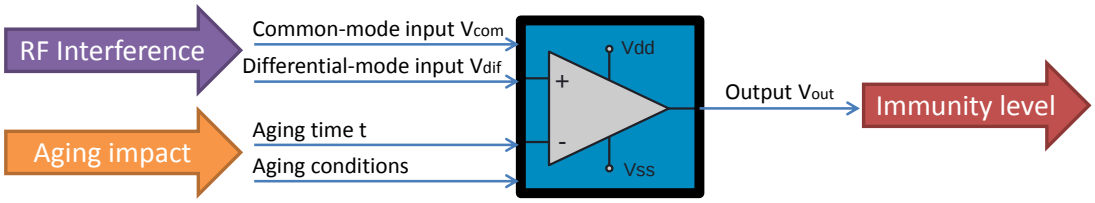


Figure IV-69 Architecture of the EMI black box of the op-amp in IC level

IV.5.5. Conclusion of case study

The aim of this case study is to find a practical method to predict the susceptibility level drift during the aging of an IC. An operational amplifier is chosen for this study, and the devices are submitted to electrical stress in order to accelerate its aging. The experimental results show a gradual decrease of the immunity level depending on the stress amplitude. Based on the degradation mechanism analysis and the simulation comparison, the threshold voltage of the MOSFET of the circuit is chosen as an internal parameter to model the aging impact.

This study proposed two modeling method to model the long-term evolution of the susceptibility level. The first long-term immunity prediction model is constructed with the original netlist information, where the aging effect is included within the susceptibility model. Besides, based on this model, another model which uses a black box approach to model the susceptibility of the circuits is also proposed. A global gradual reduction of immunity level is simulated correctly by both models, and the simulation results also demonstrate a good fitting with the measurement at most tested frequencies.

The two approaches proposed in this case study could be applied in other cases to predict the long-term EMI level, but there are also some limits of each one. The first modeling method requires the physical analysis of the circuit to find the aging source, and then the precise degradation model is

needed, and also in the modeling process, the internal netlist information of component is used. However, all of the information is hard to obtain in practice because of the protection of IP. Comparing with the model containing the original netlist information, the black box model can be extracted only by the experimental data, and the model can well protect the intellectual proprietary. But sometimes when the variables and the parameters in the model are numerous, its model can be very complex. Besides, the black box should be extracted from sufficient sample points to assure a good accuracy, which increases greatly the extraction time. Finally, the accuracy level of black box could be lost because of the use of the simplified approximate models and limited sample numbers. So we should choose the correct model in the long-term EMI prediction study according to the application.

Besides, because of the limit of time and available devices, only 3 components are tested, so in this case study we do not have enough samples for the statistical analysis, which will be discussed in next chapter. It could be a perspective for the future work.

IV.6. Case study 2: Prediction of the Electromagnetic Emission Evolution of a Buck DC-DC Converter

Because of their high power efficiency, switch-mode power supplies (SMPS) are widely used in electronic applications [BASS08]. However, one main drawback of SMPS is the noise produced by the switching activity, responsible for conducted and radiated electromagnetic emission. Therefore, the management of the parasitic emission of SMPS is a frequent topic in the literature on electromagnetic compatibility. Numerous papers dealt with the origin and the modeling of electromagnetic emission, and also the development of design guidelines to improve these issues [KAM12] [MAIN10]. Several recent studies presented the long-term behavior of SMPS. As presented in the previous chapter, passive devices could be degraded in harsh conditions. As a result of the degradation of the electrolytic capacitors which are used to filter the output voltage of SMPS, an increase of ripple in the output voltage of SMPS was illustrated in [LAHY98] [CHEN05]. Another consequence is the increase of EME, but this topic is less discussed in the literature.

This case study presents the impact of the accelerated thermal aging on the electromagnetic emission of a buck DC-DC converter. The roles of passive components in the EME drift are also discussed. The experimental analysis indicates that the aging degradation of several passive components (electrolytic capacitor and powder iron inductor) is the main source of EME evolution. Based on experimental measurement and physical analysis, the empirical degradation models of related passive devices are proposed. Finally, with the passive degradation models, an electrical model of the converter is proposed to simulate the effect of aging of each part of the converter, and the

long-term evolution of the EME of the buck DC-DC converter under a thermal aging condition is predicted.

The case study is organized as follows. The first part describes the studied converter and tested passive components, the experimental set-up and the accelerated aging condition are also presented in this part. The experimental results about the evolution of EME are presented in the second part. Then, with the degradation models of passive devices proposed in previous chapter, the model of the EME evolution of the converter is constructed.

IV.6.1. DUT and experimental set-up

The studied SMPS is based on the NCP3163 monolithic switching regulator from On Semiconductor. A simplified schematic of the converter is presented in Fig. 1. It is configured in step-down operation in order to convert the voltage 12 V provided by a battery into a regulated voltage 3.3 V for a constant resistive load equal to 3.4 Ω. The output voltage is adjusted by resistors R_1 and R_2 through the Feedback pin. The switching frequency is set to 237 kHz.

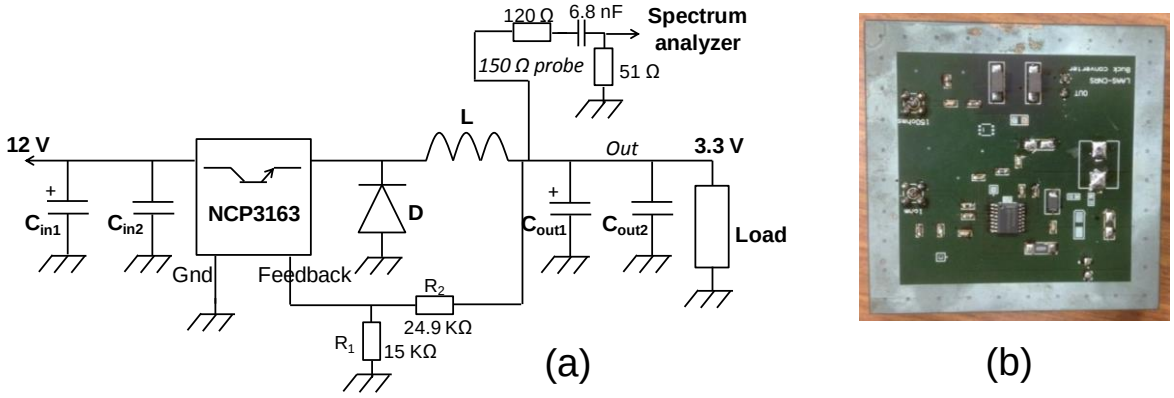


Figure IV-70 Studied buck DC-DC converter: (a) Schematic; (b) PCB test card

The test board has been designed to characterize conducted EME which is measured through a 150 Ω probe [IEC 61967-4]. It ensures a measurement of the output voltage fluctuations across a non-intrusive impedance up to 1 GHz. The output voltage is also monitored with an oscilloscope to measure its ripple. The converter is mounted on a dedicated test board designed to ensure radiated emission in TEM cell [IEC 61967-2]. All the devices are mounted on the top layer of the test board. As the measured level depends on the orientation of the device under test, the orientation of the test board compared to the TEM cell remains the same for all measurements. Besides, the conducted emission in the input side could be measured by the method LISN or a measurement of current.

As presented in IV.5.2, the conducted measurements are usually more repeatable than the radiated measurements. Besides, the current measurement of the converter input depends a lot on the DC power supply 12 V in the input and the position of power cable, where the uncertainty is hard to

be controlled. As a result, the conducted emission level by a 150 Ω probe in the output side of the DC-DC converter is selected in this EMR study.

The characteristics of filtering passive devices and rectifier are given in Table IV-6. According to the primary tests used to identify the devices degraded by thermal stress which will be detailed in IV.6.2.3, among all components embedded in the converter board, the degradation of output filtering capacitor C_{out1} affects the output voltage ripple amplitude in the low-frequency range of the emission spectrum (from 200 KHz up to about 1.8 MHz), while the degradation of the inductor L induces an increase of the EME level above 2 MHz. All the other devices have only a slight impact [BOYE14_b]. For this reason, we focus especially on these two output filtering passive components (C_{out1} and L). In order to test and compare more samples, two references are selected for each output filtering passive component (C_{out1} of two kinds of capacitor, and L from two different manufacturers).

Table IV-6 Filtering passive device characteristics

Name	Reference	Manufacturer	ID	Type	Value
C_{out1}	EEEHBA101UAP	Panasonic	C1	Aluminum capacitor	100 µF
	T491D107K010AT	Kemet	C2	Tantalum capacitor	
L	IHLP4040DZ11	Vishay	L1	Shield powder iron inductor	22 µH
	HCM1103220R	Coiltronics	L2		
C_{in1}	EEEFP1E470AP	Panasonic	--	Aluminum capacitor	47 µF
C_{in2}, C_{out2}	GCM21BR71H104KA37L	Murata	--	X7R ceramic capacitor	100 nF
D	STPS340	STMicroelectronics	--	Power Schottky rectifier	--

In addition, the different combinations of these two passive devices (C_{out1} and L) are employed in 8 test cards, and they are noted from Card1 to Card8, as listed in Table IV-7.

Accelerated aging test is always applied to obtain reliability data of electronic components in a short period. In order to accelerate the converter aging, 8 converter test boards are placed 200 hours in a thermal oven, which regulates the ambient temperature at 150 °C. Unlike the electrical stress which is applied in certain parts of the system (like input or power supply), the thermal stress accelerates the aging of all the components in the system at the same ambient temperature. As a result, we can find which parts of the system are the most sensitive under the aging stress. The stress temperature in this test could ensure a relative short aging time without damaging the tested devices definitively. During the accelerated aging process, the converters continue to run. They are powered by an external power supply which is placed outside the oven. The stress condition is interrupted each 20 hours in order to

measure the evolution of the passive device's impedance and the output conducted emission level while the converters operate under a nominal environment temperature of about 25 °C.

Table IV-7 Different combinations of output filtering devices

No. Card	No. C_{out1}	Description	No. L	Description
Card1	C1_1	Aluminum capacitor	L1_1	Shield powder iron inductor, manufactured by Vishay
Card2	C1_2		L1_2	
Card3	C2_1	Tantalum capacitor	L1_3	
Card4	C2_2		L1_4	
Card5	C1_3	Aluminum capacitor	L2_1	Shield powder iron inductor, manufactured by Coiltronics
Card6	C1_4		L2_2	
Card7	C2_3	Tantalum capacitor	L2_3	
Card8	C2_4		L2_4	

Besides, during the aging process, S-parameter measurements are performed using a vector network analyzer to extract the impedance profile of passive devices between 9 kHz and 2 GHz. As explained in previous chapter, in order to obtain better accuracy, the measurement configuration (one port or two port measurement, serial or parallel configuration) is selected according to the impedance value to be measured. The impedance characterizations are performed at room temperature with the passive devices which have been also cooled down to the room temperature.

IV.6.2. Measurement results

In this section, the results of two samples (Card3 and Card6) are presented, since they are representative of all eight tested converter samples. The biggest difference between both cards is the type of output filtering capacitor. Contrary to Card6, Card3 embeds a tantalum capacitor.

IV.6.2.1. Evolution of the output voltage ripple

After thermal stress, all the tested converters remain operational, but for the converters which employ an aluminum capacitor as the output filtering capacitor, the output voltage ripple increased strongly by 100 or 200 % (Figure IV-71 (b)). As mentioned in numerous publications such as [LAHY98], it is a direct consequence of the degradation of the filtering electrolytic aluminum capacitors placed at the converter output (C_{out1}). The high temperature contributes to an increase of its Equivalent Serial Resistance (ESR) combined with a decrease of capacitance. As the tantalum capacitor has very small ESR value, the output ripple amplitude of Card3 is much smaller than that of Card6.

Besides, according to the impedance measurements, the tantalum capacitors have no great changes after aging, so the ripple voltage at the output of the converters which embed the tantalum output filtering capacitor keeps the same amplitude, like that of Card3 which is shown in Figure IV-71 (a). However, the high frequency noise during each switching becomes more pronounced after aging.

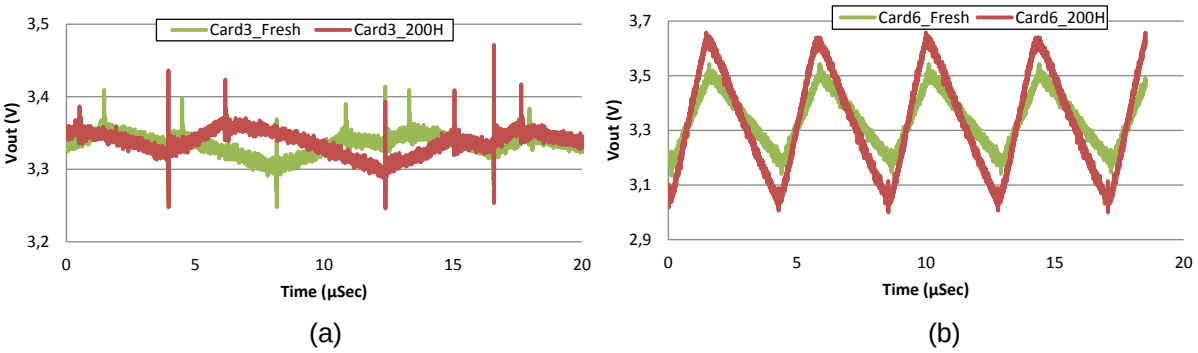


Figure IV-71 Variation of output waveform before and after aging of 200 hours: (a) with C_{out1} tantalum capacitor; (b) with C_{out1} aluminum capacitor

Besides, when we replace the stressed aluminum output filtering capacitor in the aged converters by a sound one, the output ripple amplitude returns to the initial level, as shown in Figure IV-72. The output ripple measurements confirm the impact of output filtering capacitor revealed in former studies.

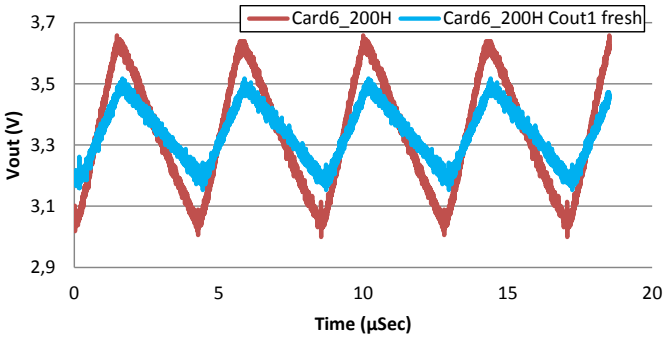


Figure IV-72 Output waveform of Card6 after aging of 200 hours with a replaced fresh C_{out1}

IV.6.2.2. Evolution of the conducted emission

The variation of output conducted electromagnetic emission before and after aging measured on both cards is shown in Figure IV-73. For clarity purpose, only the envelopes of emission spectra of two converters are plotted for emission measurement and simulation results. The average increase ranges of cards with a C_{out1} electrolytic aluminum capacitor (e.g. Card6) are between 6 and 20 dB over a large frequency range. The output conducted EME of all converters increases over a large frequency range. Because of the small output ripple amplitude, the emission in the low frequency range of Card3 is also much smaller than that of Card6. Besides, as the tantalum capacitor does not have great degradation,

the conducted emission level of the converters with this kind of capacitor does not demonstrate a significant rise in the low frequency range up to 1.4 MHz.

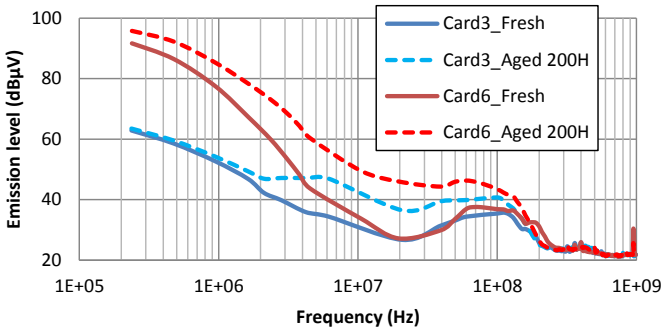


Figure IV-73 Variation of conducted emission envelope after thermal stress

Besides, the evolution of the emission level at two frequencies is illustrated in Figure IV-74, where 237 kHz is the fundamental frequency of the switching activity, and 70 MHz is the frequency which has the highest emission level above 20 MHz. Here the evolution of conducted emission over the aging time is gradual except for converters (e.g. Card3) which embed tantalum capacitor at low frequency.

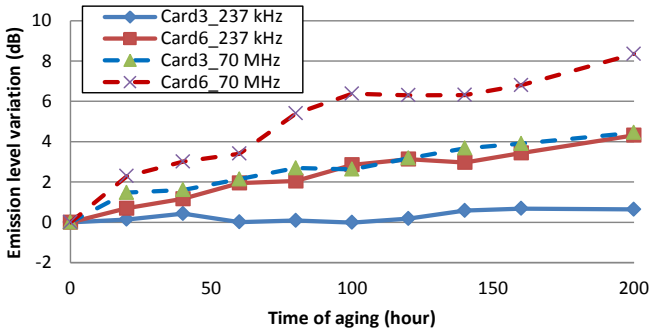


Figure IV-74 Evolution of conducted emission variation at 237 kHz and 70 MHz

IV.6.2.3. Identification of degraded devices

The role of electrolytic capacitors in the increase of SMPS output voltage ripple is widely exhibited in scientific literature. Most of the failures of SMPS are related to electrolytic capacitors, followed by the switching device [LAHY98]. The following tests aim at identifying if the increase of conducted emission is only attributed to the degradation of the electrolytic capacitors, or if other devices have to be taken into account.

The identification test is applied to identify which devices of the converter have an important impact on the emission increase. We change one or several stressed devices by sound devices of the same reference on one aged test board, and then the variation of emission levels is measured once again. If the emission variation is significant and leads to a return to the initial emission level, we can conclude that the changed device has a major influence on the change of EME levels.

Figure IV-75 presents the evolution of conducted emission for different combination of sound and aged passive devices in the identification test. For the converters with tantalum capacitor, only one replacement of the aged output filtering inductor is sufficient to make all the emission level return back to the initial level. However, for the converters using aluminum output filtering capacitor, the test results show that the degradation of both aluminum electrolytic capacitor Cout1 and inductor L affects the emission level. The aluminum electrolytic capacitor degradation has an impact on the low frequency range while the inductor degradation increases the emission above 2 MHz. Changing both output filtering capacitor (C_{out1}) and inductor (L) is enough to bring emission and output voltage ripple at their initial levels. Besides, all the other devices have a minor impact on emission level change. The results confirm the predominant influence of the output aluminum filtering capacitor on the output voltage ripple and on the low frequency range of the emission spectrum (from 200 KHz up to 1.8 MHz). It is interesting to notice that the inductor degradation L has a major impact on the medium and high frequency range of the emission spectrum (above 3 MHz).

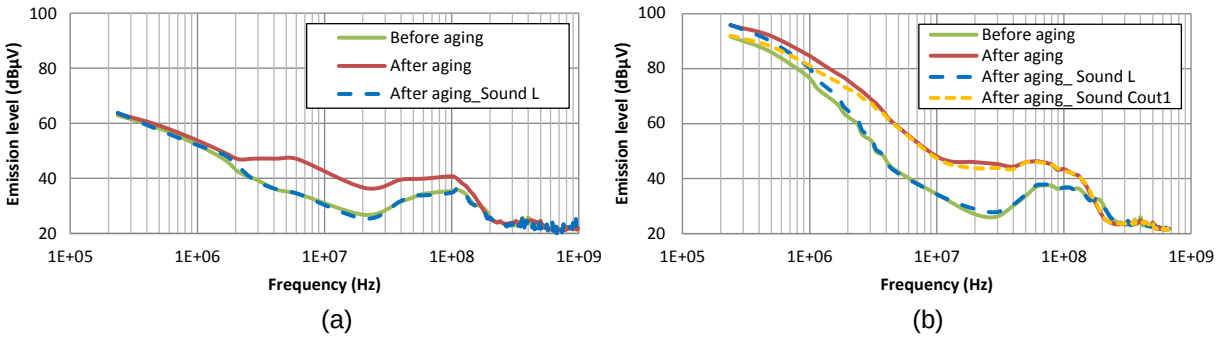


Figure IV-75 Degradation source identification test: (a) Card3; (b) Card6

However, for each single component, the measurements are also applied to verify if it is affected by aging stress. Except the impedance measurement of the passive components shown in the case study III.5, some other parameters of certain components have been also measured. For example, the characterization I (V) of the rectification diode was not affected by aging. Besides, no change has been observed in both the current consumed and the output voltage waveform of the converter. In the output side of the converter, the aging impact is only observed in the output filtering components C_{out1} and L, presented by the variations of their impedances. So finally we can resumed that the variation of the output conducted EME level is caused by the degradation of the output filtering passive components over a large frequency range.

IV.6.2.4. Aging impact on passive devices

The aging impact on the output filtering capacitors and inductors has already been presented precisely in previous chapter as a separated case study.

As presented in III.5, different references of passive components are tested and compared under the aging condition. From impedance measurement, two-port S parameter characterizations leaded on

fresh and aged electrolytic capacitors C_{out1} and inductors L demonstrated the significant change of their impedances related with the aging stress, and we have a precise insight of the aging impact on the impedance evolution of passive components. Based on physical/experimental degradation analysis, we observe that several electrical parameters in the electrical models of passive components evolve gradually during the aging process. The consequence of the degradation of aluminum capacitor is the drift of two important electrical parameters: the equivalent series resistor (ESR) of capacitor increases after aging while the terminal capacitance (C_0) decreases. And for the powder iron inductor, the parallel resistance (R_p) decreases sharply during the aging process while the parallel capacitance (C_p) increases. As expressed by several simple equations, the empirical degradation models of these electrical parameters with aging time of aluminum capacitors and powder iron inductors are constructed.

IV.6.3. Modeling of the evolution of conducted emission

Figure IV-76 details the preliminary model of the output side of converter. This model of the converter is dedicated for the simulation of the output signal and the output conducted EME level. The converter is modeled by a simplified switch block which contains an ideal switch and RLC parasite elements to simulate the temporal signal form, where the switch is controlled by a rectangular voltage source. For the diode rectifier, characterization I(V) and the VNA measurement are performed to extract the equivalent model. Besides, the equivalent models of other passive devices in the output side of the switch are characterized by VNA measurement. As shown in Figure IV-77, the transient simulations are performed with Agilent's Advanced Designed System (ADS), and the emission level in frequency domain is obtained by the Fast Fourier transform (FFT) of the output voltage waveform in time domain. To model the long-term behavior of converters, the degradation models over time of filtering capacitors and inductors presented in III.5.3 are added in the simulation, i.e. the aging impact is presented by the variation of four parameters (ESR, C_0 for C_{ou1} and R_p, C_p for L) in the simulation. As presented in Figure IV-77, the degradations of these parameters are presented by four functions extracted in III.5.3.

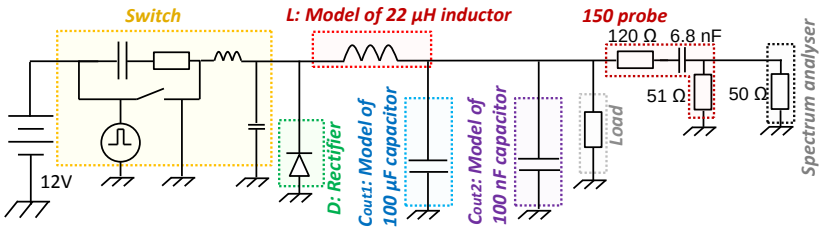


Figure IV-76 Output conducted emission modeling of the DC-DC buck converter

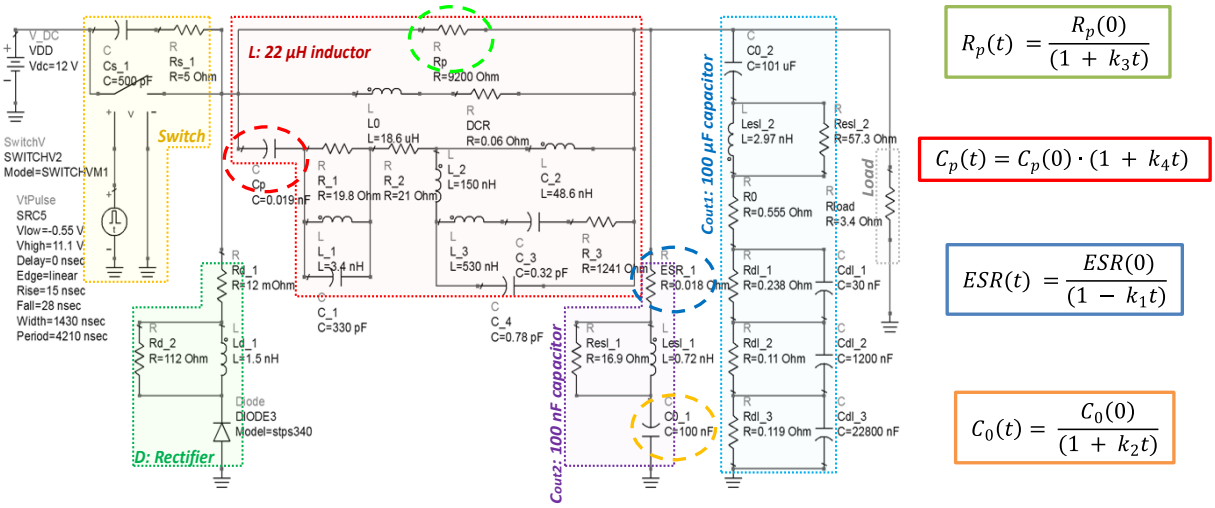


Figure IV-77 Output conducted emission models in ADS with the degradation model of four parameters

As shown in Figure IV-78, the output waveforms are well simulated. The variations of the output waveform could be observed in the simulation results, like the increase of the noise during the commutation, and the increase of the ripple amplitude of the converter with the aluminum output filtering capacitor. However, in the simulation, a very slight decrease of the DC offset about 0.01 V is observed in the converters which embed the tantalum capacitor as the output filtering capacitor, which is not observed in the measurement as a reason of the limit of measurement accuracy.

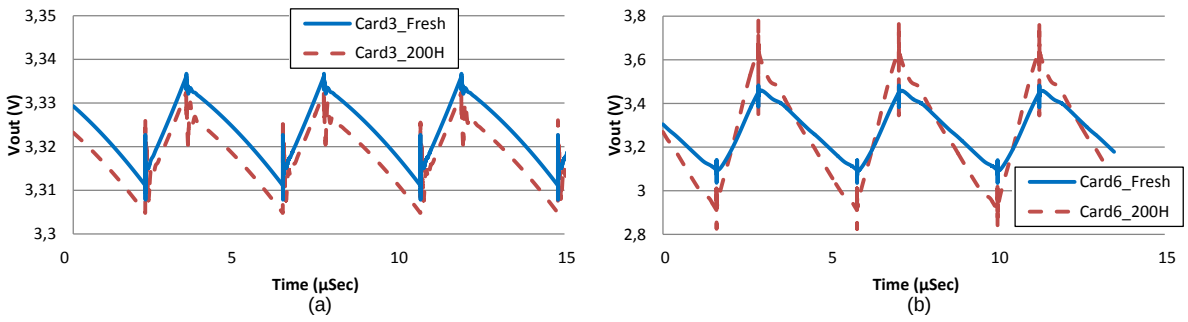


Figure IV-78 Simulation of output waveform before and after aging of 200 hours: (a) with C_{out1} tantalum capacitor; (b) with C_{out1} aluminum capacitor

As shown in Figure IV-79, the simulation results of output conducted emission envelope which is based on the model in Figure IV-77 fit well with the measurement, for both before and after the aging. Since the EME envelops extracted from the measurement and the simulation do not have the same frequency points, so the FSV method cannot be applied here to verify the simulation quality.

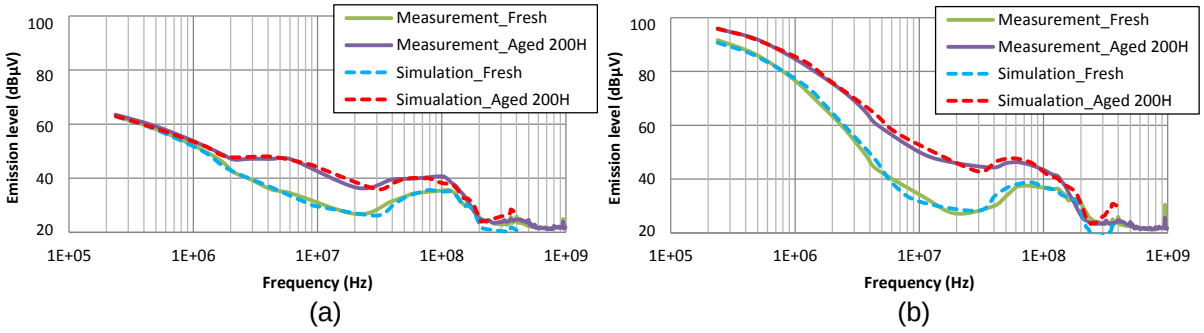


Figure IV-79 Output conducted emission envelope simulation results: (a) Card3; (b) Card6

Besides, the simulations of emission level variation of Card3 and Card6 at two different frequencies (237 kHz and 70 MHz) are presented in Figure IV-80. In these results, the gradual evolution of the conducted emission level with time is also modeled correctly. The differences in this figure and in Figure IV-79 between the simulation and measurement can be explained by the accuracy limit of degradation models of passive components as the aging impacts are considered to be random [LOMA03]. Besides, the temperature increase of components during the operation of system and the emission measurement error (about ± 1 dB) are not taken into account in the simulation.

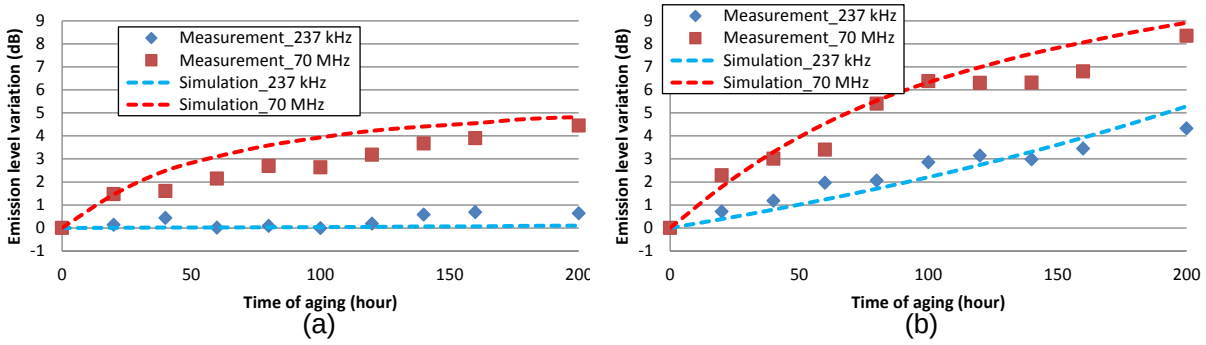


Figure IV-80 Simulation results of output conducted emission variation with time: (a) Card3; (b) Card6

IV.6.4. Prediction of EME drift by the impedance drift of the passive devices

In the previous modeling method, the prediction of the drift of the EME level has used the EME model of the whole system, where the aging impacts was simulated by the impedance drifts of certain passive components. However, as the switching regulator, which is the emission source of the whole system, is concluded has little influence to the emission drifts induced by aging degradation. The immunity drifts are rather related with the output filtering passive elements. As a result, we could tend to analyze the EMI drift only based on the degradation of the output filtering passive components, i.e. the EMI drift could be represented by the evolution of the low-pass filter formed by the two components L and C_{out1} in the output stage as indicated in Figure IV-81.

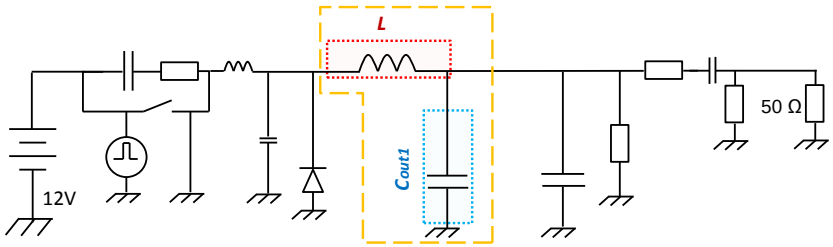


Figure IV-81 Output filtering components degraded by aging

The filtering characterization of these two components can be simply demonstrated by the transmission s-parameter S_{21}, which is also called the forward voltage gain. The s-parameters characterization is applied with ADS, as shown in Figure IV-82. Here Card6 is chosen as the tested sample. According to the simulation, the complex RLC combination in the model of inductor has no impact on the EME drift. As a result, this part is omitted in the simplified model of inductor in this simulation.

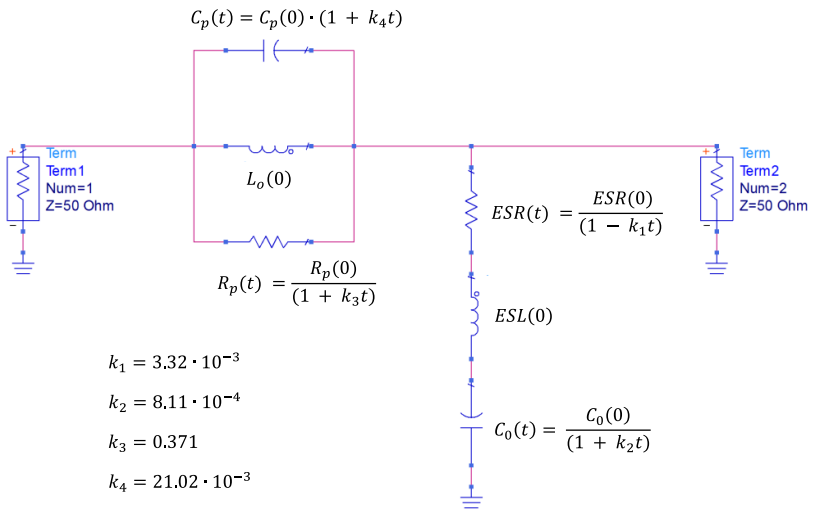


Figure IV-82 S parameters characterization simulation of Card6 by ADS

The variation of S_{21} before and after aging is illustrated in Figure IV-83. We can find under the accelerated aging stress, the filtering quality of the output filtering network decreases.

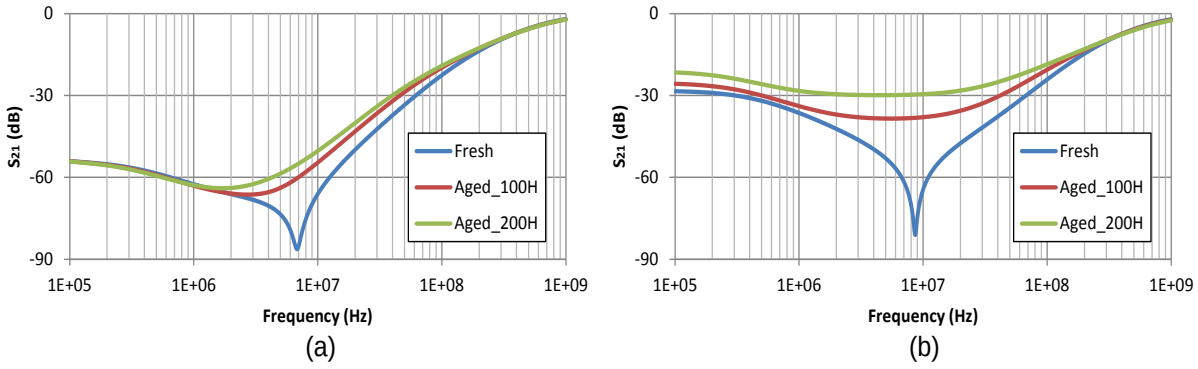


Figure IV-83 Simulation results of S_{21} before and after aging of the filtering network: (a) Card3; (b) Card6

The direct result of the decrease of the filtering quality is the increase of the emission noise in the output. As shown in Figure IV-84, the increase of the emission level of the converter can be explained by the quality decrease of the output filtering network. The major differences for the frequency range between 5 MHz to 20 MHz is due to the low emission level in this frequency range, and the EME envelopes in measurement do not include the emission level less than or around the noise level.

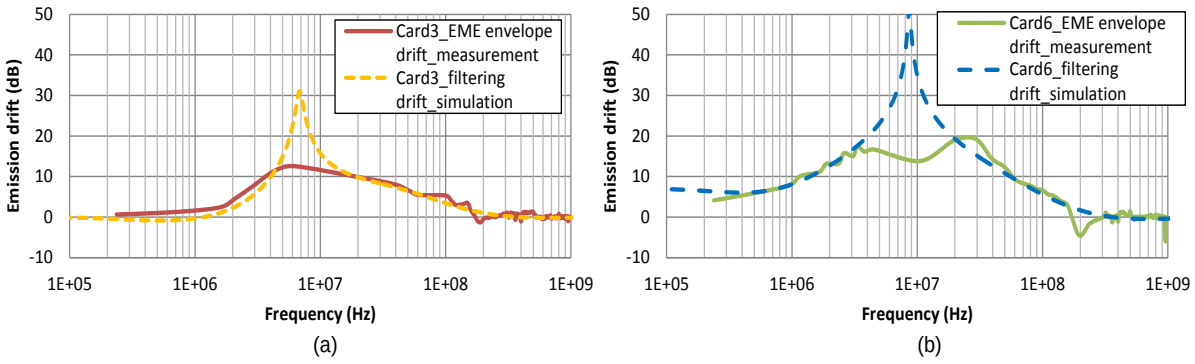


Figure IV-84 Comparison of the EME envelope drift by measurement and the filtering drift by simulation after 200 hours of aging: (a) Card3; (b) Card6

And then the emission evolution during the aging process could also be simulated by the increasing of the transmission coefficient S_{21} of the filtering network induced by aging. The modeling results over aging time is shown in Figure IV-85. The simulation results by the variation of the transmission coefficient demonstrate a good fitting with the experimental measurement. Like the simulation in Figure IV-80, the differences between the simulation and measurement are related with the accuracy limit of degradation models of passive components, and the temperature factor. The slight decrease of the Card3 at 237 kHz in this simulation could be explained by the approximation limit of the equivalent model of passive components based on impedance measurements.

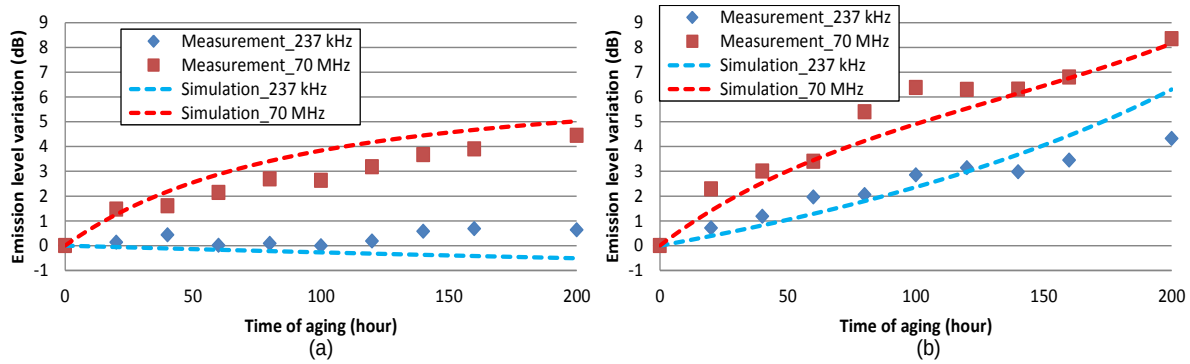


Figure IV-85 Simulation results of output conducted emission variation with time based on the output passive filtering characterization: (a) Card3; (b) Card6

As a result, for the emission aging drift induced by the degradation of output filtering components, we only need to model the decrease of the output filtering network to obtain the emission drift. And then with the initial emission level which could be simply obtained from the EME

measurement with the available fresh devices, the evolution of the emission level after aging can be predicted without the simulation of the global system. This modeling method is very simple for the EME drift caused by the degradation of filtering passive components. Because the EME model of the whole system is not needed, so it can reduce greatly the time of modeling and simulation. However, the degradation source should be well located and the precise degradation models are needed.

IV.6.5. Conclusion of case study

This case study aims at studying the modeling of thermal accelerated aging impact on the emission of a buck DC-DC converter with time, based on the degradation analysis of passive devices. The measurements are applied to observe the gradual evolution of conducted emission level under thermal accelerated aging condition, which is explained by the degradation of filtering capacitors and inductors.

Different references of passive devices are chosen, tested and compared. The experimental results demonstrate that the aluminum capacitor and the powder iron inductor have a gradual evolution over the aging time. According to the former studies and experimental measurements, a degradation model of aluminum electrolytic capacitor is proposed where ESR and capacitance vary during the thermal aging process. Besides, the evolution of both parameters seems to have a proportional relation. A preliminary degradation model of the powder iron inductor is constructed based on experimental data, where the loss resistance and parallel capacitor are impacted by aging.

We use two approaches to simulate the EME drift induced by aging. The first approach is an electrical model of the converter output side, where the degradation models of passive components are used. And the second approach is the simulation based on the transmission coefficient of the output filtering network. The second approach simplifies greatly the simulation process because the model of the whole system is not needed. The simulation results of both methods prove that the evolution of the output conducted EME of converter over aging time could be predicted with a good accuracy.

The methods of prediction of EME drift in this case study could be applied in the other studies where the EME drift of the system are related with the degradation of the filtering passive devices. In future studies, more passive samples should be tested to verify and improve the preliminary passive models proposed in this case study. Besides, complete libraries of the degradation models of passive components under different aging conditions need to be constructed. In addition, as presented in III.5, the aging impacts on different samples under the same aging conditions vary a lot. We can observe an increase of the dispersion of the degradation drift between the components with aging time. This effect needs to be integrated in the simulation. Since this is a random effect, we cannot accurately predict the EME drift, but rather a variation of the failure risk. As a result, the statistical analysis of this case study is led in next chapter to consider the evolution of EMC safety margins.

IV.7. Conclusion

The main objective of this chapter is to propose the general EMR modeling process, and to demonstrate the application of this modeling process on two case studies, one covering susceptibility issues of an analog integrated circuit, the second one dealing with the conducted emission of a SMPS.

Following the reliability study of electronic components presented in last chapter, another part of the EMR study has been introduced in this chapter: the EMC modeling. Several typical characterization measurement methods of both emission and immunity with good reproducibility were presented, and then the modeling methods used for the EMC levels of integrated circuits, with the black-box modeling were discussed. From our knowledge about reliability and EMC, the general EMR modeling process has been proposed. The EMR predictive model is based on the EMC model of the system. The structure of this EMC model keeps unchanged during the EMR modeling. Then the aging impacts are usually presented by degradation models with time of the components in the system. With the implementation of the degradation models of the components in the EMC model of the whole system, the evolution of EMC level could be simulated and predicted.

Then according to the EMR modeling flow, two case studies have been presented. The first case study is the prediction of aging impact on EMI of an operational amplifier. The aging test demonstrates that the immunity level of the device decreases after aging in a large frequency range. Then with the modeling of impact of the transistors induced by aging, the aging impact on EMI is well predicted. The second case study is the prediction of electromagnetic emission evolution of a buck dc-dc converter. This work is no more the EMC study only in the IC level but in a PCB level. We analyzed the drift of output EME of a converter. The roles of output passive filtering components in the EME drift were also discussed. With the application of passive degradation models in the whole EME model of the converter, we can predict the evolution of EME level of a buck DC-DC converter under a thermal aging process.

Based on the basic EMR modeling flow, both case studies have demonstrated satisfactory modeling results. Moreover, in each case study, we have proposed an alternative method for the long-term EMR modeling. In the study of op-amp, the black-box modeling method which hides all the confidential information has been applied. Besides, in the study of DC-DC converter, the EME drift could be obtained simply from the passive degradation modeling instead of the EME modeling of the system.

The advantage and the insufficiency of both case studies have been concluded in the end of each one. The characterization of the aging process requires a large amount of manipulations. Because of the limit of time and the available samples, the number of devices under tested is relatively limited. However, the DUTs of the finite amount demonstrated a good repeatability for the EMC levels' drifts.

Finally, as an important part of the EMR analysis, the statistical analysis of the long-term EMC levels will be detailed in next chapter.

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Chapter V. Statistical analysis for the EMR prediction

V.1. Introduction

As the results of the random nature of signals, real systems also demonstrate statistical behaviors in their parameters and responses, including their EMC levels. Theoretically, there are never two components which are the same [CHRI07]. The previous studies in this thesis have demonstrated that the EMC levels vary greatly under hard operating conditions, which are related with the degradation of components (ICs and passive components). Besides, the EMC evolutions could be predicted by simulations based on the reliability degradation modeling.

However, the studies above have also revealed that under the same aging stress the aging impact on different components of the same reference might differ from one to another. The difference of the aging impact is related with the dispersion between the different samples and the random phenomenon during the aging degradation [LOMA03]. So for the long-term EMC study of a sample group, the evolution of EMC level is not only the deterministic variation of the emission or immunity level, but also the statistical distribution of the EMC level and the probability of EMC compliance for a defined EMC limit (called "EMC reliability" [WU12]) at each aging phase.

The objective of the statistical analysis in the EMR study is to determine the statistical distribution of the emission and immunity levels, then to calculate the evolution of the probability of EMC compliance (or non-compliance) against a given limit. In this study, we begin with a general discussion about the statistical analysis in EMC studies, where several statistical distributions of EMC level are presented. The statistical characterization of EMC drift is detailed in the following part. Then, the statistical analysis methods used in prediction of long term "EMC reliability" are presented, where some common distributions used in the reliability study of electronic devices are presented. Finally, a primary EMR prediction case study of the statistical analysis, which is based on the case study of DC-DC buck converter and passive devices in the last chapter, is proposed in the end in order to validate the proposed method and discuss about the improvement of the method.

V.2. Statistical analysis in EMC study

V.2.1. Statistics and EMC

As presented above, there are not two electronic systems that could have completely identical EMC levels. In practice, the most random variations of parameters and performances are around their mean values. The variations are due to the differences between samples, even of the same type and of the same batch. Except the measurement errors between the samples, the process variation during the fabrication is the main source. For the EMC levels at high frequencies, the parasitic elements at high frequencies are very hard to control. As a result, the statistical analysis becomes very useful and sometimes necessary in certain EMC applications. However, nowadays, most of EMC studies, in measurements and simulations, focus rather on the studies of deterministic electronic systems, which have fixed parameters and performances.

In comparing with a deterministic analysis method, the statistical analysis always means the increasing complexity of system analysis. That's why the statistical analysis is usually ignored in practice, even though we can get a closer accuracy to the reality. In recent years, the statistical analysis methods have been more and more applied in EMC studies [LARB15]. The studies in [PIGN06] and [CHRI07] have indicated several reasons for the utilization of statistical analysis in EMC studies, which included:

- The EMI sources in nature (frequency, amplitude, propagation direction and polarization) are always imprecise and vary random.
- The immunity level of electronic devices is a statistical phenomenon. For a set of devices, their failure thresholds are never equal to a certain fixed value for all the tested samples. The failure probability at each RF interference level could be a much more reasonable and more correct expression to quantify the susceptibility level of devices.
- The knowledge and control of the geometrical and electrical data, and also the parasitic nature of electronic devices are always incomplete. Usually, these uncertainties could be concluded by statistical analysis.
- Most current EMC standards are expressed in deterministic mode, and the statistical measurements of failures in consideration of the safety are usually required by the industry.
- The increasing complexity, the co-existence between different systems, and the modifications and updates through the whole lifetime require more the statistical information of the parameters and EMC levels of devices.
- The assessments of EMC levels by measurements represent the errors and uncertainties related to the experimental manipulations and instruments.

Besides, the random nature in the variation of the EMC performances induced by aging degradation after a long-term operation is also an important reason for the application of statistical

analysis in EMC studies [CHRI07], which will be discussed in this chapter. Here in this section, we will discuss briefly the usual statistical distributions for EMC level description.

V.2.2. Statistical distributions for EMC levels

The dispersion of the EMC level of a device under test is caused by the measurement uncertainty, the material inhomogeneity, or the fabrication and placement tolerance [AJAY08]. In some statistical EMC studies like [HOLL98], [BRON99] and [CARO03], the statistical distribution of EMC levels are resumed as normal distribution for the linear units (such as V, mV…), or lognormal distribution for the logarithmic units (such as dB, dBm, dBµV…).

V.2.2.1. Normal distribution

The normal distribution is a very common distribution to represent real-valued random variables. It is also call Gaussian or bell curve distribution. The probability density function (PDF) f of the normal distribution is expressed in Equation V-1.

$$f(x) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{-\frac{(x-\mu)^2}{2\sigma^2}} \qquad \text{Equation V-1}$$

Where x is the random variable µ is the mean value and also the median of the distribution, and σ is the standard deviation with its variance σ². In statistical analysis, the variance value demonstrates how far a set of numbers is spread out. The normal distribution can be defined by these two parameters and be expressed by N (µ, σ²). An example of three immunity level distribution is shown in Figure V-1 (a), where the unit of immunity power is W. We can also convert the unit to dBW, as shown in Figure V-1 (b), where the distribution is no more symmetrical around the mean value µ.

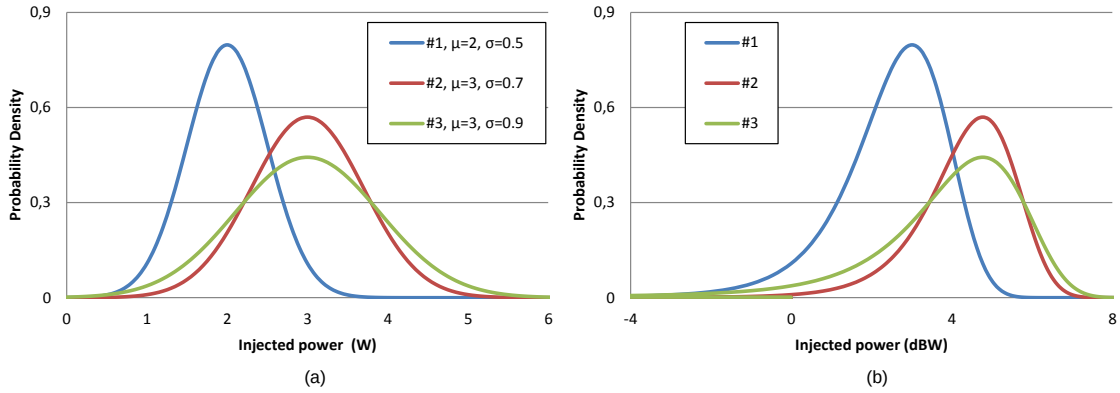

Figure V-1 **Probability density functions for three sets of immunity level: (a) immunity level is in linear unit W; (b) immunity level unit is converted into logarithmic unit dBW**

According to the three-sigma rule (68–95–99.7 rule), the probability of 68.27%, 95.45% and 99.73% of the random values lie within one, two and three times the standard deviation σ around the mean µ, respectively. Besides, we can use cumulative distribution function (CDF) F(x) of a random variable X

to describe the probability that the variable has a value less than or equal to x, as defined in Equation V-2.

$$F(x) = \int_{-\infty}^{x} f(y)dy \qquad \text{Equation V-2}$$

The CDFs of the same variables in Figure V-1 are shown in Figure V-2, in W and in dBW, respectively.

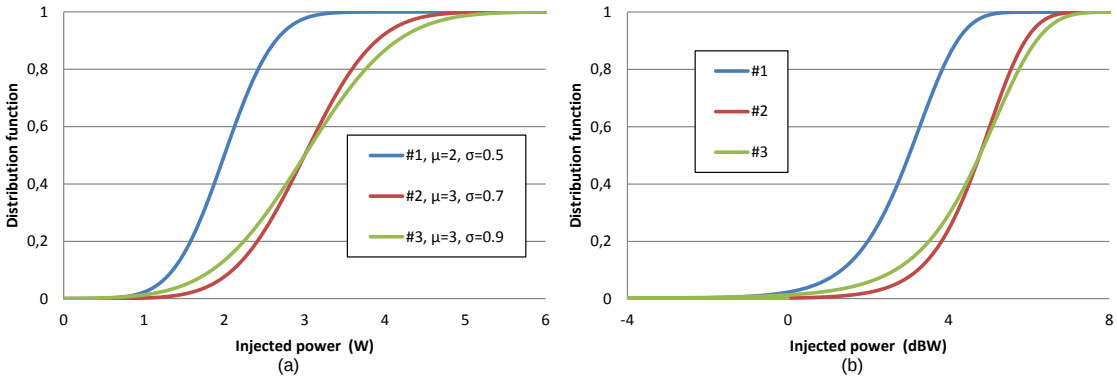

Figure V-2 **Cumulative distribution functions for three sets of immunity level: (a) immunity level is in linear unit W; (b) immunity level unit is converted into logarithmic unit dBW**

V.2.2.2. Lognormal distribution

However, in the most cases, EMC measurements use directly logarithmic units. As presented in [CARO03], for the uncertainty estimation, it is assumed that the EMC levels using dBs are normally distributed. The probability density function using dBs in normal distribution are expressed in Equation V-3 (a). When the unit of immunity level is converted to the linear unit W, the symmetry of density functions disappears, as shown in Equation V-3 (b). And their cumulative distribution functions are presented in Figure V-4.

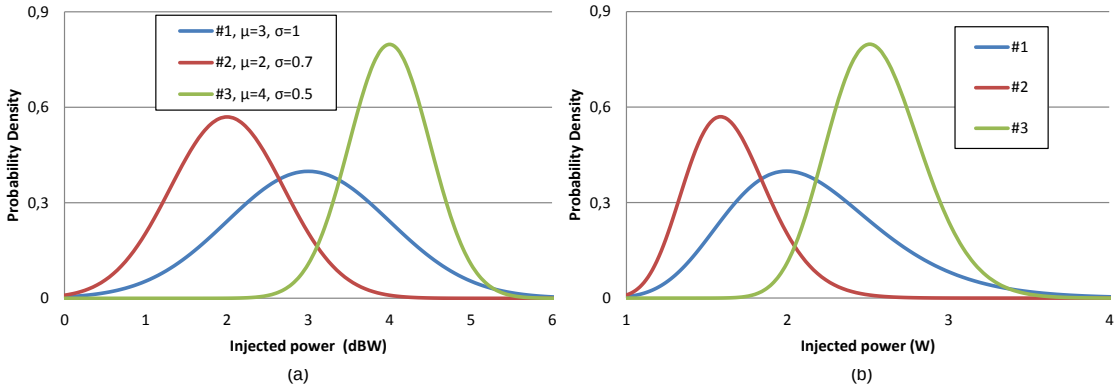

Figure V-3 **Probability density functions for three sets of immunity level : (a) immunity level is in logarithmic unit dBW; (b) immunity level unit is converted into linear unit W**

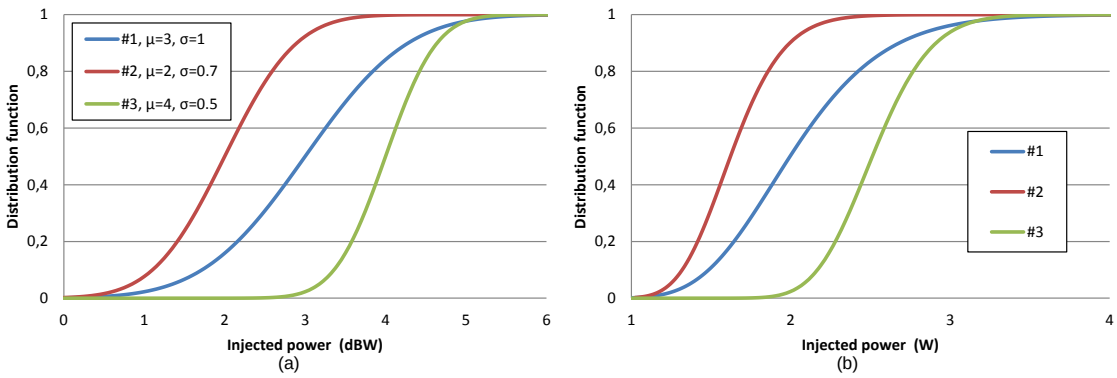

Figure V-4 Cumulative distribution functions for three sets of immunity level : (a) immunity level is in logarithmic unit dBW; (b) immunity level unit is converted into linear unit W

Here the statistical distribution using linear unit is another type of distribution called lognormal distribution. In fact, the lognormal distribution is mathematically the transformed normal distribution, where all the data are taken in natural logarithms. Thus, if Y = ln(X) has a normal distribution which is expressed by Y~N (μ, σ²), the random variable X has a lognormal distribution. The probability density function of X is expressed in Equation V-3, with the same parameters μ and σ of Y.

$$f(x) = \frac{1}{\sqrt{2\pi\sigma^2 x^2}} e^{-\frac{(lnx-\mu)^2}{2\sigma^2}} \qquad \text{Equation V-3}$$

In the lognormal distribution, the two parameters μ and σ are called the location and the scale, respectively. The mean value $\overline{X}$ and the variance var{X} of the lognormal distribution can be calculated by Equation V-4 and Equation V-5.

$$\bar{X} = e^{\mu+\frac{\sigma^2}{2}} \qquad \text{Equation V-4}$$

$$\sigma_x^2 = (e^{\sigma^2} - 1)e^{2\mu+\sigma^2} \qquad \text{Equation V-5}$$

However, the dB expression is not the natural logarithm. We define that a random variable Y in dB has a normal distribution Y~N (μ, σ²). Y is expressed by Y = A·log(X), where A is either 10 (like for power) or 20 (like for voltage), we have:

$$X = 10^{\frac{Y}{A}} = e^{\frac{ln(10)\cdot Y}{A}} \qquad \text{Equation V-6}$$

We define that $Z = \frac{\ln(10)\cdot Y}{A}$, so we have:

$$X = e^{Z} \qquad \text{Equation V-7}$$

Since Y has a normal distribution, and ln(10)/A is a constant, so Z has also a normal distribution which could be expressed by Z~N (μ_z, σ_z^2) with the following parameters:

$$\mu_z = \frac{\ln(10) \cdot \mu}{A} \qquad \text{Equation V-8}$$

$$\sigma_z = \frac{\ln(10) \cdot \sigma}{A} \qquad \text{Equation V-9}$$

So according to Equation V-3, we can have the probability density function of X by:

$$f(x) = \frac{1}{\sqrt{2\pi}\sigma_z x} e^{-\frac{(lnx-\mu_z)^2}{2{\sigma_z}^2}} \qquad \text{Equation V-10}$$

Therefore

$$\bar{X} = e^{\mu_z + \frac{{\sigma_z}^2}{2}} = e^{\frac{\ln(10)\cdot\mu}{A} + \frac{(\frac{\ln(10)\cdot\sigma}{A})^2}{2}} = 10^{\mu A^{-1} + 0.5\ln(10)\cdot\sigma^2 A^{-2}} \qquad \text{Equation V-11}$$

$$\sigma_x^2 = \left(e^{{\sigma_z}^2} - 1\right)e^{2\mu_z + {\sigma_z}^2} = \left(e^{\left(\frac{\ln(10)\cdot\sigma}{A}\right)^2} - 1\right)\bar{X}^2 = (10^{\ln(10)\cdot\sigma^2 A^{-2}} - 1)\bar{X}^2 \qquad \text{Equation V-12}$$

Here μ and σ are the parameters of the normal distribution of Y.

V.2.2.3. EMC distribution based on distribution of sub-components

Another method of distribution analysis for EMC level is based on the components in the system whose statistical distributions are already known. Here we use a simple example with a single parameter to explain the method. We suppose that the EMC level of the whole system is a random variable M. A single parameter N of the system is the only variable of all the parameters which affects the EMC level. It has a probability density function $f_n(x)$, mean value $\bar{N}$ and variance σ_n^2. The relation between the EMC level M and the parameter N is defined by a function M=g(N). The PDF of EMC level $f_m(x)$ of the whole system and also the approximate values of the mean value $\bar{M}$ and variance σ_m^2 could be calculated by:

$$f_m(x) = \frac{f_n(x)}{\left|\frac{dg(x)}{dx}\right|} \qquad \text{Equation V-13}$$

$$\bar{M} \cong g(\bar{N}) + \frac{\sigma_n^2}{2}\left[\frac{dg(x)}{dx}\right]_{x=\bar{N}} \qquad \text{Equation V-14}$$

$$\sigma_m^2 \cong \sigma_n^2 \left\{ \left[\frac{dg(x)}{dx} \right]_{x=\bar{N}} \right\}^2$$ Equation V-15

Theoretically, with this method, we can calculate the EMC distribution based on the known statistical distributions of sub-components. However, the real function g(x) of EMC levels is usually very complex and sometimes contains the non-linear activities. Besides, the number of variables which influence the EMC levels is often much larger than 1, which increases greatly the complexity of the calculation. So this calculation method works only for the simplest systems in practice.

V.2.2.4. Determination of statistical distributions for EMC levels

Based on several former studies, we have presented two common statistical distributions of EMC level according to the measurement units. However, since the EMC levels usually relate with several statistical variables, sometimes with also the non-linear activities of circuits, so we cannot resume that the normal or lognormal distribution are the general statistical distribution style for all EMC levels. As a result, theoretically the most precise extraction method of the statistical distribution for a certain component should be based on the measurement of sufficient samples to reduce the confidence interval. But in practice, the normal or lognormal distribution is always acceptable for the EMC dispersion analysis for the random EMC levels whose distributions are not known.

Besides, all the statistical distributions discussed here work only at single tested frequency. The EMC level at each frequency is considered as a random variable. Usually, we do not know the relationship between these random variables, so it is difficult to determine the dependence of EMC level at different frequencies. As a result, in this study we consider that these random variables are all independent from each other, and the EMC level of each frequency has its own statistical distribution. As shown in Figure V-5, the immunity level measured in dBmW are assumed to have normal distribution, and the standard deviation at each frequency is chosen to quantify the dispersion among 10 samples. We can observe that the standard deviation value varies according to the frequency.

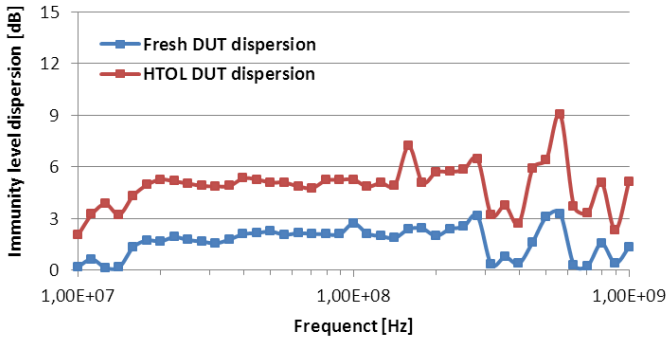

Figure V-5 Evolution of the dispersion of the immunity level of a PLL power supply after HTOL test [LI11]

There are already several statistical studies in EMC domain, like the statistical analysis of crosstalk problem presented in [GAO10], and also the statistical characterization in a reverberation chamber in [VOGT13] and [KOVA15]. In [NAUS08], the author has resumed the former studies about statistical electromagnetics. As indicated in this paper, the commonly accepted statistical distribution for the electromagnetic field has to be considered as a hypothesis, which has not been contradicted by experiments. However, the most recent statistical analysis studies of EMC level focus only on the EMC levels of circuits at fresh state. The EMC distributions over the operating life are little considered, which will be discussed in the following section.

V.3. Statistical analysis of EMC drift

As presented in Chapter III, the reliability of electronic devices is basically a statistical notion. In reliability study, because of the variation of the aging impact on a set of samples under the same operating conditions (or aging stress conditions), statistical analyses are widely used to summarize the variation of the parameters which are indications of the aging impact. As a result, there are several distribution models proposed which are based on real experimental measurements and physical degradation analysis, such as Weibull distribution and lognormal distribution [OHRI98]. With these models, we can predict the performances' evolution of individual devices and their lifetime. Besides, the EMC levels of the global systems which integrate these random changes produced during the aging process should also be taken into account. However, the relationship between the EMC level and the internal variables of the system is usually not easy to extracted, so the determination of the dispersion of the EMC level after aging is complex. In this section, the statistical method to characterize the EMC drifts induced by aging and the EMC distribution after aging are presented.

V.3.1. Statistical characterization for EMC drift

An example of the EMC level of five samples measured before and after aging at a single frequency fj is presented in Figure V-6. The EMC level tends to increase after aging. As a result, the mean EMC level after aging M_a is higher than that M_b before aging. But the increase of the average EMC value ΔM cannot represent the EMC variation of every sample. For example, the increase of sample no.4 at frequency j $\Delta S4j$ is much larger than that the average increase ΔM, and the EMC level of sample no.1 at frequency fj decreases after the aging process.

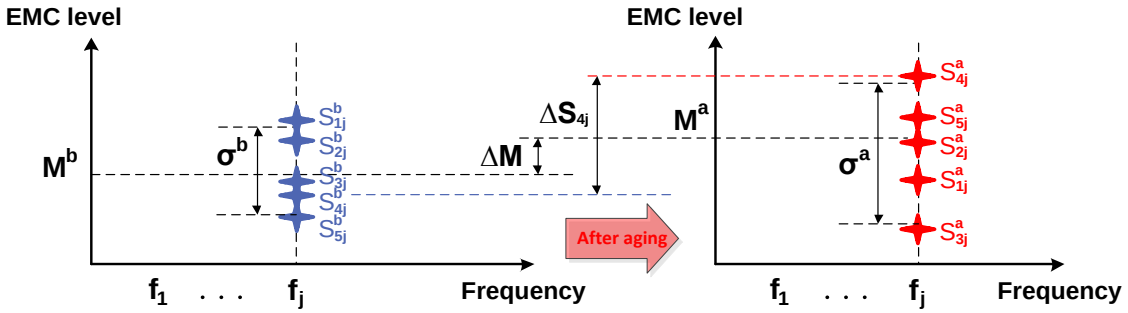

Figure V-6 Measurement of EMC level drift after aging with a set of samples [LI11]

As a result, for a set of samples, the EMC variations need to be calculated with different samples at different frequencies, which could be expressed by a matrix:

$$\begin{bmatrix} \Delta S_{11} & \cdots & \Delta S_{1j} \\ \vdots & \ddots & \vdots \\ \Delta S_{i1} & \cdots & \Delta S_{ij} \end{bmatrix} = \begin{bmatrix} {S^a}_{11} & \cdots & {S^a}_{1j} \\ \vdots & \ddots & \vdots \\ {S^a}_{i1} & \cdots & {S^a}_{ij} \end{bmatrix} - \begin{bmatrix} {S^b}_{11} & \cdots & {S^b}_{1j} \\ \vdots & \ddots & \vdots \\ {S^b}_{i1} & \cdots & {S^b}_{ij} \end{bmatrix} \qquad \text{Equation V-16}$$

Here S^b_{ij} and S^a_{ij} are respectively the EMC level of the sample no.i at frequency j before and after aging, and ΔS_{ij} is the EMC level drift of the sample no.i at frequency j. As explained above in V.2.2.3, the EMC level is assumed independent from one frequency to another, so the statistical characterizations of EMC level are applied separately at each tested frequency. The common EMR statistical qualification for N samples at frequency j consists in the mean drift value ΔM_j (Equation V-17) and the dispersion of the aging impact by the variance $\Delta\sigma_j^2$ of the EMC level drifts (Equation V-18).

$$\Delta M_j = \frac{1}{N}\sum_{i=1}^{N}(S_{ij}^a - S_{ij}^b) \qquad \text{Equation V-17}$$

$$\Delta {\sigma_j}^2 = \frac{1}{N-1}\sum_{i=1}^{N}(S_{ij}^a - S_{ij}^b - \Delta M_j)^2 \qquad \text{Equation V-18}$$

Except the statistical qualification at a single frequency, in [LI11], the author has proposed the global mean value of all the tested frequencies as a global indicator of the aging impact on the EMC level. However, the more reasonable analysis is the mean value of the statistical values over a certain frequency range where the aging impact are observed rather than the whole frequency range, in order to demonstrate more precisely the EMC evolution. As shown in Figure V-7, the average variation of the immunity levels of the tested devices in different frequency range presents the different evolution trends after aging. Besides, the evolutions under the different aging conditions (LTOL and HTOL) are completely different, not only for the accelerated factor, but also for the EMC drift trend (increase or decrease).

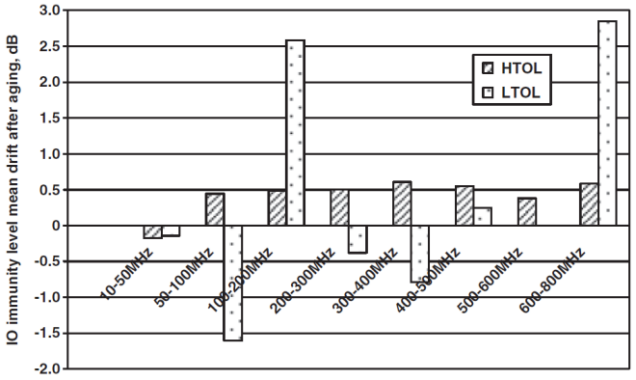

Figure V-7 **Comparison between HTOL and LTOL aging impact on IO immunity (interference injected on IO input): mean drift for all samples [BEND10]**

V.3.2. EMC distribution after aging

The study in [BEND10] has indicated that the EMC levels of ICs cannot be accurately known due to the measurement errors and the dispersion among samples. As a result, the EMC drifts for a set of components are not only the drift of EMC level, but also the variation of the failure probability of EMC non-compliance to a given limit. In this part, to simplify the presentation, all the following EMC level evolutions are calculated at a certain single frequency.

An example in [LI11] of the EMC drifts of digital I/O devices is explained in Figure V-8. In this figure, the probability density functions of the EMC level measured before and after aging are illustrated, and are compared with a level limits. In this example, the EMC levels before and after aging are supposed to follow a normal distribution. With the EMC drifts induced by the aging, the probabilities of non-compliance change and need also to be evolved. As shown in Figure V-8 (a), with the decrease trend of emission level, the EMC non-compliance probability for a fixed emission limit decreases. Besides, in Figure V-8 (b) with the decrease trend of immunity level, the EMC non-compliance risk for a defined immunity threshold increase, which means the EMI failure occurs more possibly after aging.

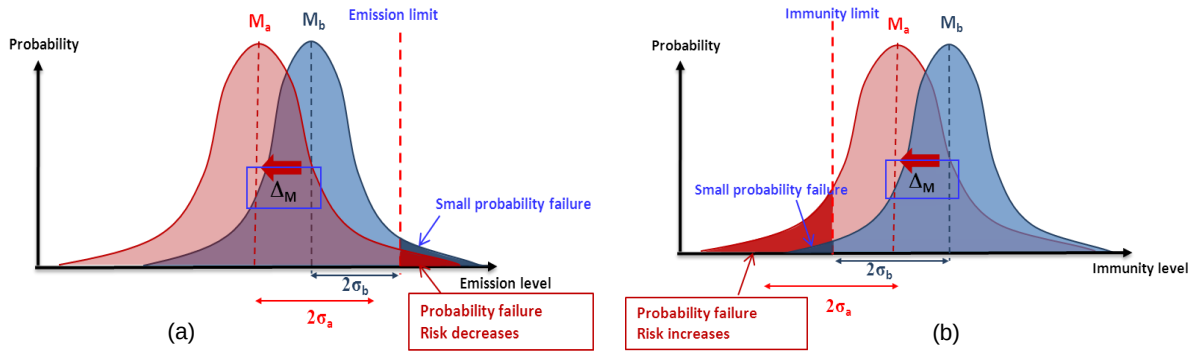

Figure V-8 **Examples of EMC level drift of digital I/O devices: (a) Conducted emission level statistical distribution moves away from the emission limit, so the EMC non-compliance probability decreases after aging; (b) Conducted immunity level statistical distribution moves towards the immunity limitation, so the EMC non-compliance probability increases after aging [LI11]**

As a result, the prediction of EMC levels in the long-term means the forecast of the distribution of EMC levels after aging. If we assume that the aging process and the dispersion during the aging are independent of the EMC dispersion among fresh samples, the EMC distribution after aging could be calculated by Equation V-19.

$$A = B + D \qquad \text{Equation V-19}$$

Where

B is the EMC level before aging, with a probability density function $f_b(x)$;

D is the EMC drift during aging process, with a probability density function $f_d(x)$;

A is the EMC level after aging, with a probability density function $f_a(x)$.

Here A, B and D are all continuous random variables.

According to the theorem in [GRIN97], for continuous random variables, the sum of two independent random variables is a random variable with the density function which is the convolution of the density functions of the two independent random variables. So the density function f_a can be calculated by Equation V-20.

$$f_a(x) = (f_b * f_d)(x) = \int_{-\infty}^{+\infty} f_b(y)\, f_d(x-y)dy = \int_{-\infty}^{+\infty} f_b(x-y)\, f_d(y)dy \qquad \text{Equation V-20}$$

In several former studies like [CHRI07] and [LI11], the EMC level distribution of the fresh samples was assumed as normal distribution which could be defined by the mean value $\overline{B}$ and the variance σ_b^2. Here we also assume that the random variable of the EMC drift also follows a normal distribution $N(\overline{D}, \sigma_d^2)$, the two parameters in this normal distribution can be calculated respectively by Equation V-17 and Equation V-18. According to Equation V-20, the density function f_a of the EMC level after aging A is still a normal distribution, which can be calculated simply by Equation V-21.

$$f_a(z) = N(\bar{A}, \sigma_a^2) = N(\bar{B} + \bar{D}, \sigma_b^2 + \sigma_d^2) \qquad \text{Equation V-21}$$

An example of the probability density function of the EME level after aging based on the calculation of the fresh EME level and the EME drift induced by aging is shown in Figure V-9. Here the standard variation σ after aging becomes larger than that before aging, which means a larger dispersion of the EME level between samples is produced by the aging process. With the evolution of the mean value and dispersion, we can observe an increasing failure probability of EME level which exceeds the threshold in Figure V-9. In theory, there is an EMC failure probability at each aging phase,

even at the fresh state B in Figure V-9. This failure probability evolution with time will be discussed in the following section about the EMC reliability.

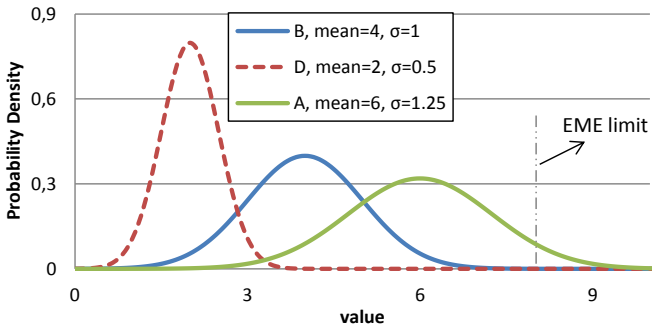

Figure V-9 **Probability density function of the EME level after aging (A) based on the fresh EMC level (B) and EMC drift (D): A=B+D**

However, all the calculations proposed in Equation V-21 are based on the assumption that both fresh EMC level and EMC drift follow the normal distribution. In fact, there are not any systematical EMC drift studies that have proved that the EMC drift at each aging phase is in normal distribution, although this is a very common distribution type. In our study, we will not tend to conclude the distribution type for the EMC drift neither, but to propose the methods which could be used in the analysis of EMC drift and the EMC level after aging, and also the EMC reliability presented in the next section.

V.4. EMC reliability

As presented above, the EMC levels of electronic systems evolve with aging time. For a set of devices, the EMC level at each aging time t ($t \geq 0$) can be resumed by a statistical distribution. Here the time t becomes the random variable under study. However, at each aging phase, the EMC level could be simply resumed by a reliability probability (or failure probability) for a given EMC limit. This evolution of reliability probability of EMC levels with time could be resumed by the EMC reliability function.

In the reliability study of electronic devices, except the normal distribution and lognormal distribution presented above, there are also several other useful distribution functions [KUO98] [OHRI98]. The statistical distribution of reliability over time can help us to have a good insight of the failure probability of the electronic systems over the global lifetime. In this section, three common distributions (exponential distribution, lognormal distribution and Weibull distribution) used in the reliability studies are briefly discussed. And then, the extraction methods of EMC reliability are presented in the end of this section.

V.4.1. Main statistical distributions for reliability study

V.4.1.1. Exponential distribution

The failure probability distribution function and the cumulative distribution function of exponential distribution with the random variable t (time) are expressed in Equation V-22 and Equation V-23, respectively. Where λ_o is a constant, which is the single parameter in this distribution.

$$f(t) = \lambda_o e^{-\lambda_o t} \qquad \text{Equation V-22}$$

$$F(t) = 1 - e^{-\lambda_o t} \qquad \text{Equation V-23}$$

Plots of the PDF and CDF of exponential distribution with two λ_o values as a function of time t are presented in Figure V-10.

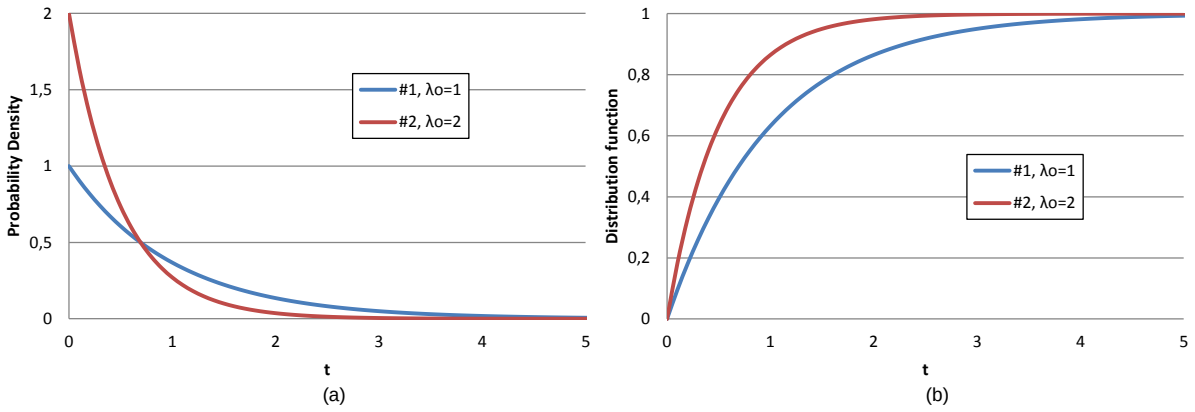

Figure V-10 Plots of exponential distribution: (a) Probability distribution functions; (b) Cumulative distribution functions

The failure rate λ(t) during the aging process in the exponential distribution can be calculated by Equation V-24. That means the failure rate of the exponential distribution is a constant λ_o.

$$\lambda(t) = \frac{f(t)}{1 - F(t)} = \lambda_o \qquad \text{Equation V-24}$$

Moreover, the mean time to failure (MTTF) is the mean value of PDF, and the MTTF of exponential distribution is λ_o^{-1}. Besides, the variance of this distribution is λ_o^{-2}. As a result, if we implement the components with a high-reliability, which means with a lower failure rate λ_o, we can get a longer mean lifetime.

Because of the ease in dealing with a constant failure rate which is independent of time, the exponential distribution is adopted as a basis for reliability modeling. Besides, the exponential distribution is observed in practice during the operating life of some electronic devices without wearout properties and infant mortality. However, as presented in Chapter III, the failure rate of semiconductor products displays an important decrease with time during the infant-mortality period.

For this reason, the exponential distribution with time becomes too ideal for electronic devices [ORHI98] [KUO98].

V.4.1.2. Lognormal distribution

The PDF of lognormal distribution as a function of time t is presented in Equation V-25. Here the variable t does not contain 0 for the reason of natural logarithm ln(t). There is no simple expression for the cumulative distribution function, which could be calculated by Equation V-2. An example of lognormal distribution (PDF and CDF) is illustrated in Figure V-11.

$$f(t) = \frac{1}{\sqrt{2\pi\sigma^2 t^2}} e^{-\frac{(lnt-\mu)^2}{2\sigma^2}} \qquad \text{Equation V-25}$$

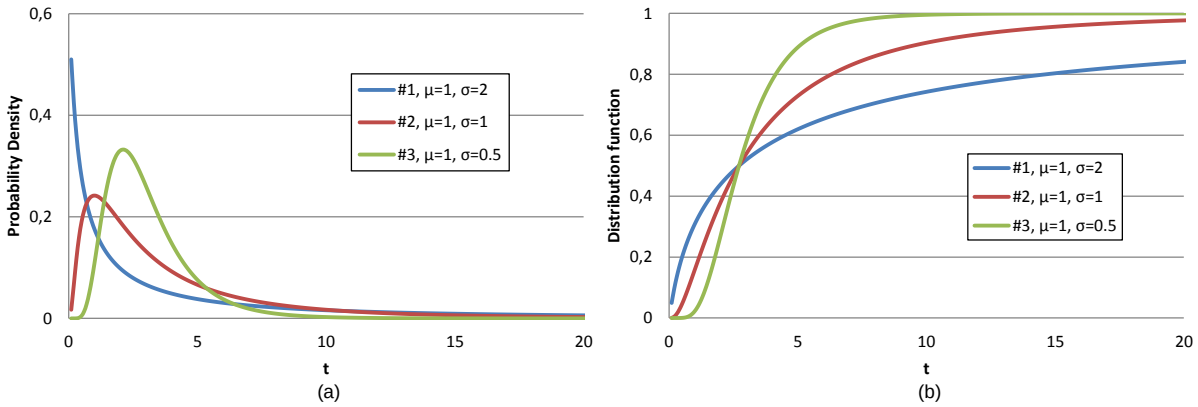

Figure V-11 Plots of lognormal distribution: (a) Probability distribution functions; (b) Cumulative distribution functions

The failure rate function with time can also be calculated according to Equation V-24, which is demonstrated in Figure V-12.

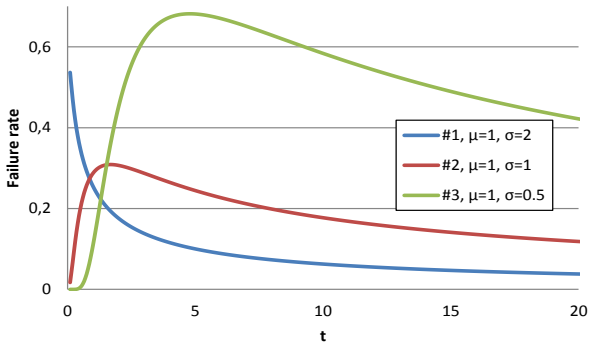

Figure V-12 Failure rate functions of lognormal distribution

In this figure, for different values of σ, the failure rate is always an increasing failure rate followed by a decreasing failure rate. Its value approaches zero for initial time and infinite time [KUO98]. For a large value of σ (like 2 for sample #1 in Figure V-12), the failure reaches a peak value in a very early

time, then decreases with time. So an σ value larger than 2 indicates that the failures of components are out of control. For a good reliability application, we need σ is around 1 or less. The failure rate form represents well the early infant failure, steady state and the wear-out period in the whole life of electronic devices.

V.4.1.3. Weibull distribution

The probability density function for Weibull distribution is expressed as:

$$f(t) = \frac{k}{\lambda}(\frac{t}{\lambda})^{k-1}e^{-(\frac{t}{\lambda})^k} \qquad \text{Equation V-26}$$

And the cumulative distribution function as:

$$F(t) = 1 - e^{-(\frac{t}{\lambda})^k} \qquad \text{Equation V-27}$$

Where k is the shape parameter and λ is the scale parameter of the distribution. In a special case of k = 1, the distribution becomes an exponential distribution. And when k = 2, it is a Rayleigh distribution, which are normally not used in reliability study of electronic products [OHRI98]. An example of Weibull distribution with the same scale parameter and several different shape parameters is demonstrated in Figure V-13.

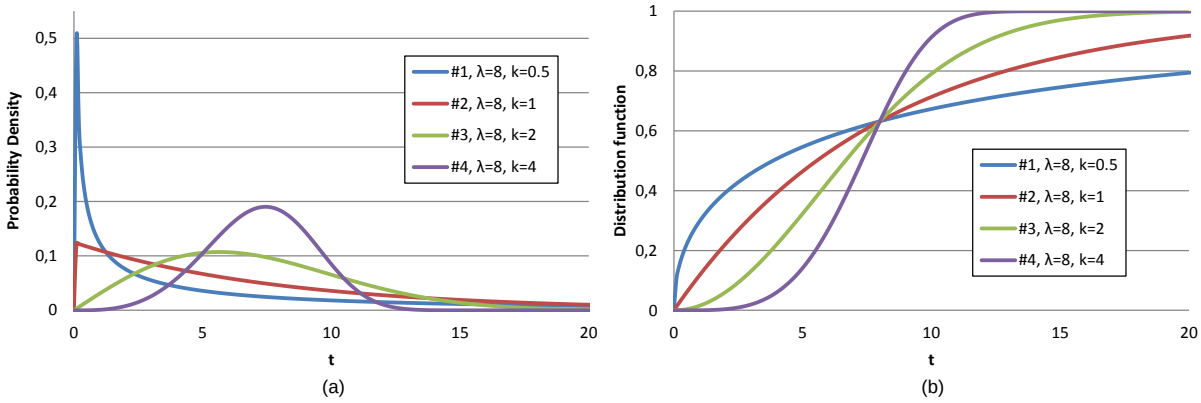

Figure V-13 **Plots of Weibull distribution: (a) Probability distribution functions; (b) Cumulative distribution functions**

From Equation V-24, the failure rate function is expressed by Equation V-28. According to this equation, the failure rate functions of the distributions in Figure V-13 are shown in Figure V-14.

$$\lambda(t) = \frac{k}{\lambda}(\frac{t}{\lambda})^{k-1} \qquad \text{Equation V-28}$$

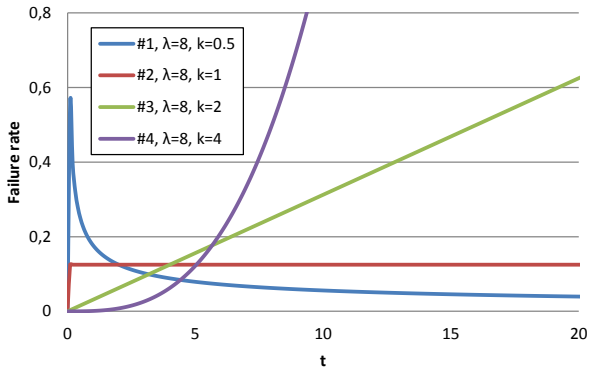

Figure V-14 Failure rate functions of Weibull distribution

Besides, the MTTF of Weibull distribution can be calculated by:

$$MTTF = \lambda \cdot \mathrm{r}\left(1 + \frac{1}{k}\right) \qquad \text{Equation V-29}$$

Here r() is the gamma function, which can be calculated by:

$$\mathrm{r}(n) = \int_0^\infty x^{n-1} e^{-x} dx \qquad \text{Equation V-30}$$

The Weibull distribution is widely used in the failure distribution with time. Normally, except the process with time, we cannot observe other stochastic processes which follow Weibull distribution. Unlike the lognormal distribution, except the special case of k=1 where the failure rate is a constant λ, the Weibull distribution has either an increasing failure rate with time (when k is above 1) or a decreasing failure rate (when k is below 1). As a result, the Weibull distribution provides an infinite possibility to represent various failure processes. For example, the three regions of the bathtub curve can be modeled by the Weibull distribution with different value of k [KUO98] [ABER06]:

- k < 1.0 indicates infant mortality
- k = 1.0 means random failures (independent of age)
- k > 1.0 indicates wear out failures

According to [ABER06], with extremely small samples, the Weibull analysis is able to provide reasonably accurate failure analysis and failure forecasts, so the cost and time required is under control. Another advantage is the simplicity of the graphical plot of the failure data to extract the two parameters λ and k in the distribution, which will be presented in the following section.

V.4.1.4. Extraction of distribution

The extraction of each distribution is usually based on the measurement results of the failure probability F(t) of the devices. Based on the cumulative distribution function of each distribution, we

can plot the probability functions as straight lines on special probability papers of each distribution. In these papers, the distributions are linearized in order to be expressed by a straight line. For example, according to Equation V-27, the cumulative distribution function of Weibull distribution can be expressed by Equation V-31. So if the distribution is expressed by a straight line y=mx+b, we have y=ln{-ln[1-F(t)]} and x=ln(t), which are two axes of the probability paper. The parameters k and λ of the distribution can be calculated by m=k and b=-k·lnλ.

$$\ln\{-\ln[1-F(t)]\} = k \cdot \ln(t) - k \cdot \ln\lambda \qquad \text{Equation V-31}$$

The probability papers of the lognormal distribution and the Weibull distribution are shown in Figure V-15. The differences between these two probability papers are demonstrated in their y axes. Here the same measured failure probability over time of laser diodes are plotted as the points in the probability papers. In each paper, a straight line which could have the best goodness of fit with the measurement points is extracted. Then based on the parameters of the straight line, the parameters of the distribution could be obtained. In this example, because of the limit of measurement points, both distributions demonstrate a good fitting with the experimental results. As a result, it is difficult to determine which distribution is the best choice.

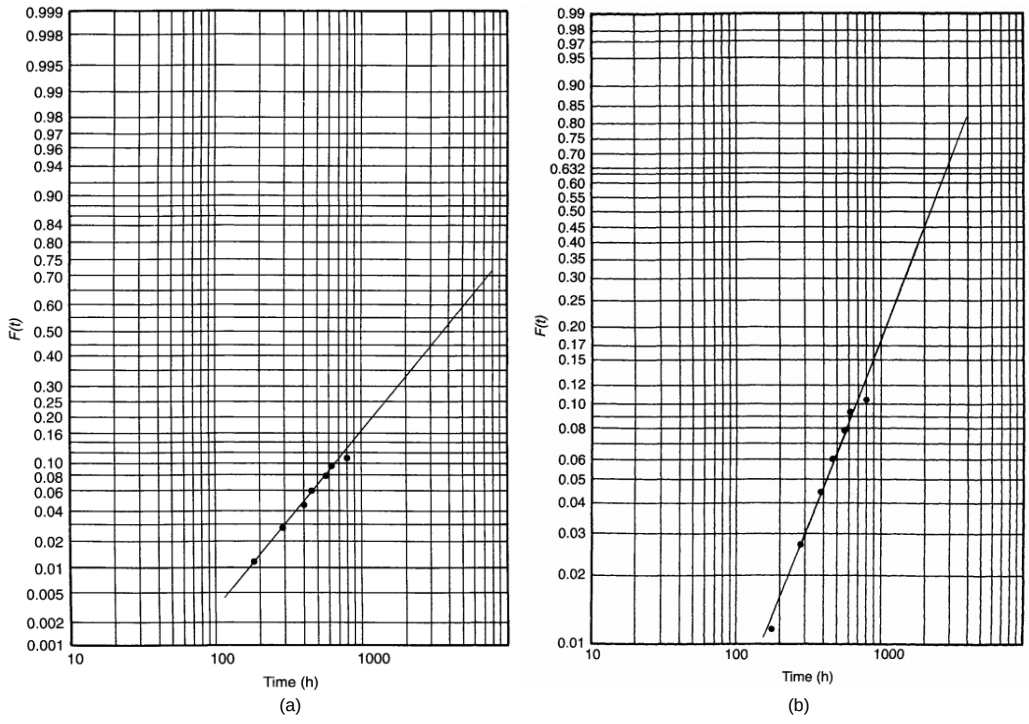

Figure V-15 Laser diode failure times (a) plotted on lognormal probability paper; (b) plotted on Weibull probability paper [ORHI98]

V.4.1.5. Determination of distribution

The selection of the distributions could be based on their physical significance. Lognormal distribution can be applied for the gradual degradation over time induced by diffusion effects,

corrosion processes and chemical reactions. Several wearout failure mechanisms, such as TDDB and electromigration, and the lifetimes of semiconductor devices after burn-in are well described by the lognormal distribution. On the other hand, the Weibull distributions appear to be applicable for systems composed of a number of independent components and whose failure is caused by the most severe flaw in the system. Dielectric breakdown, capacitor failures and fracture in ceramics are the typical degradations described by Weibull distribution [KUO98] [OHRI98] [LIU97].

However, because of the various accelerated aging conditions and degradation mechanisms, and also the lack of several degradation knowledge, it becomes difficult to resume the degradation distribution only by the physical analysis. As a result, plotting the measured failure probability of the devices in the distribution papers could be the method to verify the desired distribution and also to extract the parameters of distribution. For example, if the lognormal distribution is the best representation of the data's distribution, the data will demonstrate a straighter line on lognormal probability paper than other distribution papers. However, this method requires sufficient samples and measurement points during the lifetime to demonstrate the quality of fitting of each distribution. If the measurement points are very finite like the example in Figure V-15, it is hard to compare the fitting quality in each distribution paper.

However, among the distribution proposed below, the Weibull distribution could provide an acceptable accuracy with small samples in a lot of cases. In addition, the parameters λ and k in the Weibull distribution is easy to be extracted with the simple data plot (Equation V-31). As a result, this distribution is selected to be applied in the case study of EMC reliability distribution presented in V.5.

V.4.2. EMC reliability distribution

For the EMC study, the reliability can be defined as the EMC compliance during the lifetime. As presented below, the EMC level of a set of samples at each aging phase cannot be presented by a single value but a statistical distribution. Likewise, the EMC reliability, even for the fresh devices, should be presented by a probability. The EMC reliability with time could be expressed by a reliability function $R_{emc}(t)$ (also called survival function), which describes the probability of no failure (EMC compliance) at aging time t ($t \geq 0$). Here, to simplify the presentation, the following EMC reliability analysis is discussed at a given single frequency f_0.

Usually, the EMC compliance is defined by a fixed EMC limit provided by a standard. Like in Figure V-8, the EME level limit is defined by a maximum threshold for the RF emission level, and the EMI level limit is defined by a minimum threshold for the RF interference level. The probability of EMC compliance over time $R_{emc}(t)$ at a given single frequency f_0 for EME and EMI could be obtained in Equation V-32 and Equation V-33, respectively.

$$R_{eme}(t) = \int_{-\infty}^{x_0} f_t(x)\,dx = F_t(x_0)$$ Equation V-32

$$R_{emi}(t) = \int_{x_0}^{+\infty} f_t(x)\,dx = 1 - F_t(x_0)$$ Equation V-33

Where

$R_{eme}(t)$ and $R_{emi}(t)$ are the reliability functions of EME and EMI at aging time t, respectively;

x_0 is the EMC limit of the EMC level at frequency f_0;

$f_t(x)$ is the probability density function of the EMC level at aging time t.

$F_t(x)$ is the cumulative distribution function value of the EMC level at aging time t.

According to these equations, an example of calculation process of the EMC reliability $R_{emc}(t)$ based on the statistical distribution of EMC level at three time phases (T1, T2 and T3) at a given frequency is shown in Figure V-16. Here we can find the $R_{eme}(t)$ is equal to the CDF value $F_t(x_0)$ of EME level at time t, and the $R_{emi}(t)$ is equal to $(1 - F_t(x_0))$ at time t.

Based on the function of $R_{eme}(t)$ and $R_{emi}(t)$, we can also calculate other statistical parameters. Here we define the probability density function of EMC failure as $f_{emc}(t)$, the failure probability distribution function as $F_{emc}(t)$, the EMC failure rate (or hazard rate) as $\lambda_{emc}(t)$, and the mean time to EMC failure (MTTF) as $MTTF_{emc}$. So we have:

$$F_{emc}(t) = 1 - R_{emc}(t)$$ Equation V-34

$$f_{emc}(t) = \frac{d}{dt} F_{emc}(t)$$ Equation V-35

$$\lambda_{emc}(t) = \frac{f_{emc}(t)}{R_{emc}(t)}$$ Equation V-36

$$MTTF_{emc} = \int_0^{\infty} R_{emc}(t)\,dt$$ Equation V-37

These statistical parameters are useful to analysis the long-term EMC reliability. For example, the MTTF is the mean time to failure, i.e. the mean time of EMC compliance of the system. This parameter is very important, because it conditions the instant of maintenance, it might provide a period after that it would recheck the EMC compliance of the system.

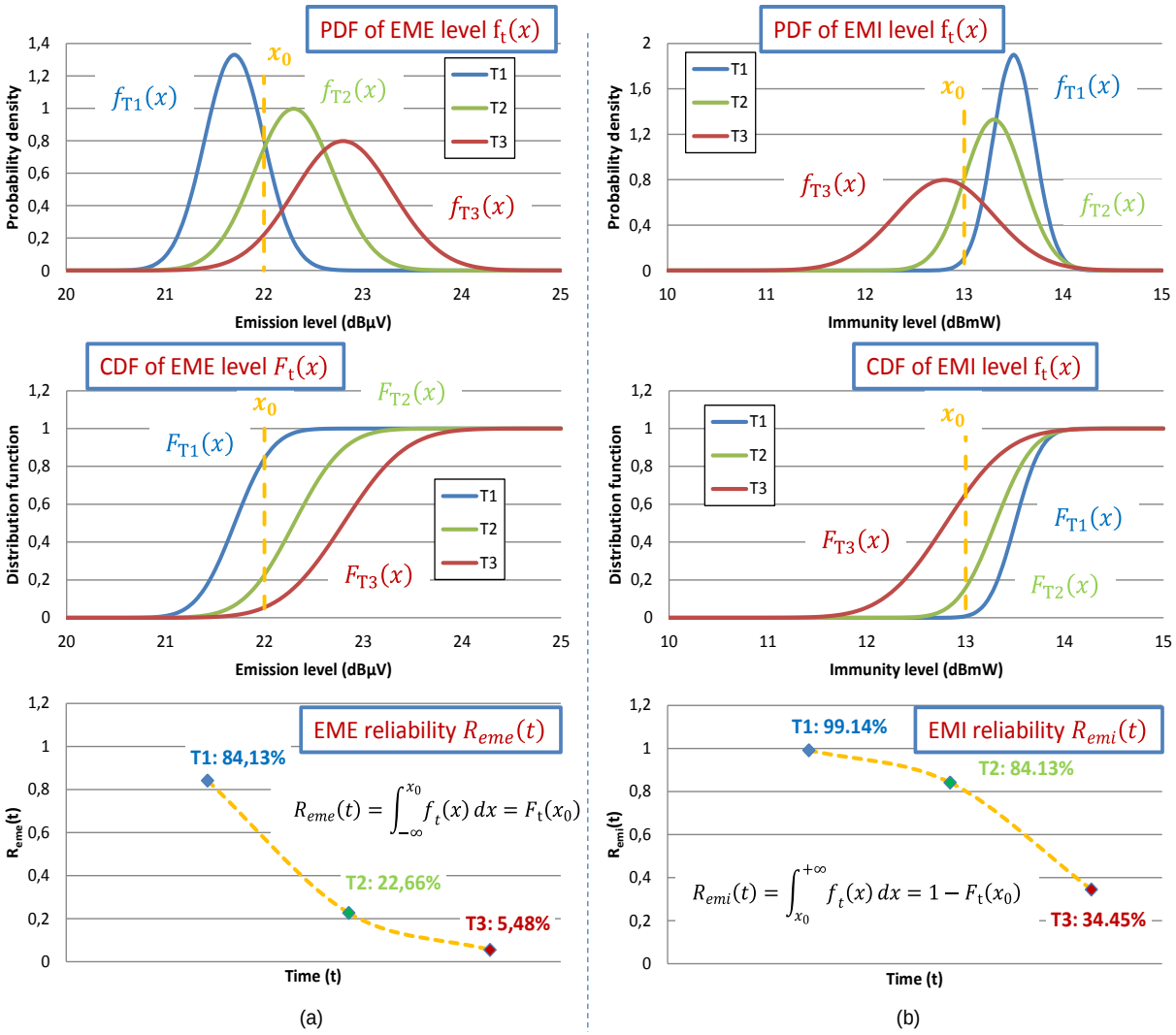

Figure V-16 Calculation of EMC reliability based on the statistical distribution of EMC level at three time phases (T1, T2 and T3) at a given single frequency: (a) EME reliability $R_{eme}(t)$; (b) EMI reliability $R_{emi}(t)$

As presented above, the EMC reliability is presented by the EMC compliance for a defined threshold of EMC level. The statistical distribution of EMC reliability could be extracted by the methods based on the failure probability distribution function $F_{emc}(t)$ presented in V.4.1.4. However, as the EMC levels are usually related with the behaviors of the parasitic elements and the non-linear activities, the distribution of EMC reliability could be very complex and not a traditional distribution type. Moreover, to assure a good accuracy by this method, a large number of samples and measurement points during the lifetime are required, which is very time consuming and needs a good repeatability of EMC characterizations over time.

The calculation method based on the statistical distribution of sub-components presented inV.2.2.3 also could be applied for the EMR prediction, if the statistical distributions of the internal parameters with time are available. However, as a reason of its complexity, this calculation method is only applied for the simplest system. For more complex system, the automatic analytical approach by simulators like Monte Carlo simulation based on the limited random samples [RAYC08], and some

other improved sampling methods could be applied, like First-Order Reliability Method (FROM), Second-Order Reliability Method (SROM), Subset Simulation (SS), and Importance Sampling (IS) applied in [LARB15].

The EMC reliability distribution takes into account both the dispersion related with the different samples and also the impact of degradation induced by aging. Besides, its distribution function could be a good demonstration for the evolution of EMC failure probability over time. However, as presented above, sometimes the extraction of the EMC reliability distribution is very complex. Besides, the EMC reliability is based on a fixed EMC limit level, so for the same system, the EMC reliability distribution should be rebuilt if the definition of EMC limit is changed. As a result, sometimes only the EMC reliability function is not sufficient, the detailed distributions of EMC level at each aging time t are required to compute precisely the evolution of EMC compliance with time.

Here the EMC reliability function was discussed at a single frequency f_0. In practice, it should be calculated for all frequencies where might have the EMC problem, and the EMC reliability of each frequencies could be completely different. The EMC failure of the whole system occurs when the EMC level at any frequency exceeds the EMC limit. As a result, the EMC reliability level of the whole system $R_{emc.global}(t)$ could be expressed by the minimum EMC reliability value of all frequencies at time t.

Finally, the safety performance can be based for example on the SIL (Safety Integrity Level) as proposed in [IEC 61508]. This indicator defines the safety level of a function. The definitions of SILs for high demand / continuous mode in this standard are resumed in Table V-1. According to the statistical analysis of the EMC reliability, we can define the SIL of a system for EMC failure with the parameters like λ_{emc} and MTTF. The relevance of SIL levels to the problem of EMR should be discussed in the future to define practical limit for MTTF and failure rate or to qualify the electromagnetic reliability of a system.

Table V-1 Definitions of SILs for high demand / continuous mode [IEC 61508]

SIL	Range of λ (failures per hour)	Range of MTTF (year)
4	$10^{-9} \leq \lambda \leq 10^{-8}$	$10^4 \leq MTTF \leq 10^5$
3	$10^{-8} \leq \lambda \leq 10^{-7}$	$10^3 \leq MTTF \leq 10^4$
2	$10^{-7} \leq \lambda \leq 10^{-6}$	$10^2 \leq MTTF \leq 10^3$
1	$10^{-6} \leq \lambda \leq 10^{-5}$	$10 \leq MTTF \leq 10^2$

V.5. Case study: Statistical analysis of the EME reliability of a buck DC-DC converter

V.5.1. Problematic analysis

In the previous chapter, the evolution of the electromagnetic emission of a buck DC-DC converter induced by aging impact has been studied. The previous studies have revealed that the EME evolution is related with the degradation of passive filtering components. Based on the degradation models of the passive components, the EME drift could be predicted by simulation.

However, as shown in Figure V-17, the experimental measurements in this study demonstrate significant dispersions between the emission level of the different samples, especially after aging. Card5 and Card6 in Figure V-17 are two converter test boards which integrate the components of the same reference, so their emission levels before aging have only very few differences. In the other hand, even though the aging duration and aging conditions for both test boards are completely same, their emission levels after aging process are very different. After aging, Card5 produces a higher emission level in the low frequency range up to about 400 kHz. Contrarily, for the frequency range higher than 600 kHz, a much larger emission increase is observed on Card6.

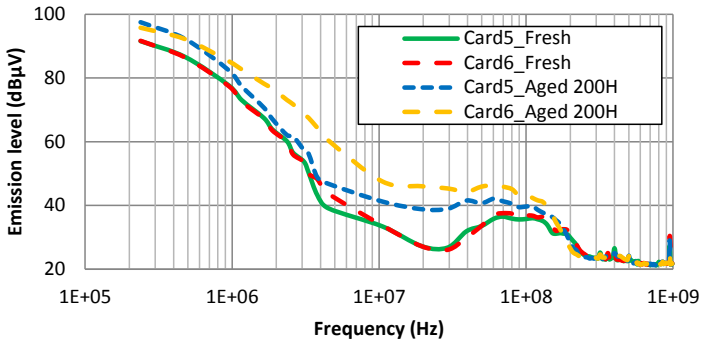

Figure V-17 EME envelope before and after aging of two DC-DC converter cards

The evolution of the emission level can be explained by the variation of the filtering quality of the output LC filtering network. As the degradation sources of the EME drift, the impedances of the two filtering passive components in both cards before and after aging are illustrated in Figure V-18. The impedances of both passive components before aging demonstrate very little difference. But after 200 hours under the same aging stresses, significant differences between their impedance profiles could be observed for both passive components. Since the degradation of aluminum capacitors is rather related with the EME increase in the relatively low frequency range, and the degradation powder iron inductors impact on the EME level in higher frequency range, the differences of evolution of the emission level between both converters in Figure V-17 could be explained by the impedance variation of passive components.

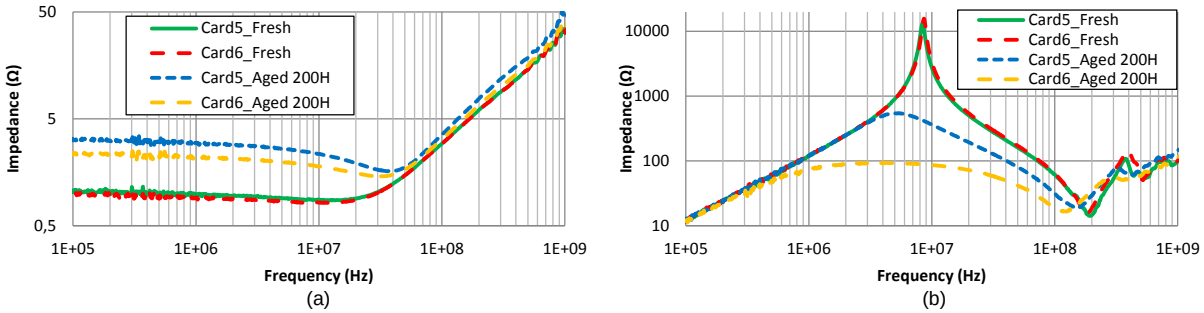

Figure V-18 Impedance evolution before and after aging of two output filtering passive components: (a) Aluminum capacitors; (b) Powder iron inductors

Here the dispersion of EME level induced by the aging of both samples is demonstrated above, which proves well that the statistical analysis is needed in the EMC robustness studies. In this case study, the EME level covers a large number of frequencies. Since we assume that the EMC reliability distribution at a single frequency is independent with that at other frequencies, the complete EME reliability of the DC-DC converter requires having the distribution function with time at each frequency, which enhances greatly the repeated works. To simplify the analysis, only the EME reliability at 237 kHz is detailed here. This frequency is the fundamental frequency of the switching activity in the DC-DC converter. Besides, the maximum EME level can be observed at this frequency, which is also related with the amplitude of the output ripple voltage. Moreover, the emission levels at this frequency of different samples demonstrate a much better repeatability than that at other frequencies. As the EME drift at this frequency is rather related with the output aluminum capacitor, so only the converters which integrate this kind of filtering capacitor are studied.

The EME reliability at other frequencies could also be extracted by the two following methods. Otherwise, the confidence level of the statistical analysis in this case study is not very high in reason of the limited number of samples. As a result, the objective of this case study is not to extract the general distribution type of the EMC reliability by the test of a large number of frequencies, but rather to detail the extraction methods used to extract the EMC reliability.

V.5.2. Extraction of EME reliability based on measurement results

V.5.2.1. Characterization of EME evolution

In the aging experiments, there are totally 4 DC-DC converters using the aluminum capacitor as the output filtering capacitor. The emission levels of 4 samples at the switching frequency 237 kHz before and after aging (200 hours) are presented in Figure V-19. Here the emission measurements are applied 3 times for each emission test. As a result, in this figure there are 12 emission measurement points before and after aging, respectively. The dispersion between the measurement points are related with both the measurement errors and the samples' difference.

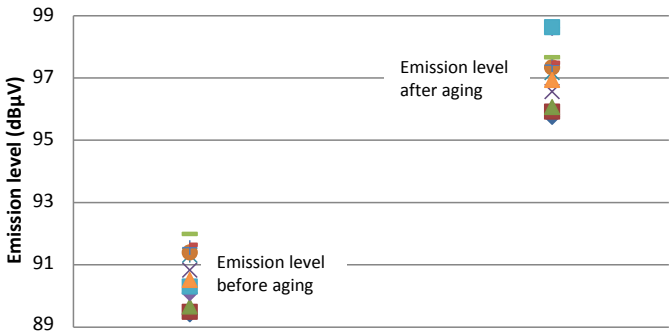

Figure V-19 Output emission level of 4 converters before and after aging (200 hours)

The mean value and the variance value of the emission level before aging and at nine aging phases are resumed in Table V-2.

Table V-2 Two statistical values of the emission level before and after aging

Aging time t (hour)	0	20	40	60	80	100	120	140	160	200
Mean value	90.68	91.22	91.6	93.39	93.39	94.12	94.75	94.67	95.5	97.13
Variance	0.74	0.75	0.75	0.78	0.78	0.81	0.80	0.80	0.81	0.82

We suppose that the EME level has a normal distribution (here we use the logarithm unit dBµV, but in fact it's a lognormal distribution with the linear unit like µV), both before and after aging. The PDF and CDF of the EMC level are plotted in Figure V-20. Here if we define an EME level x_0 as the maximum limit, the CDF of x_0 is the same value of the reliability function $R_{emc}(t)$ at this aging time according to Equation V-32. According to the CDF figure, with the increase of EME level with time, the reliability level of the components decreases. For example, if the maximum EME limit is 95 dBµV, the reliability probability is 99.99997% before aging ($R_{emc}(0)$) but decreases to 0.93766% after aging of 200 hours ($R_{emc}(200)$). On the other hand, according to Equation V-34, the EMC failure probability ($F_{emc}(t) = 1-R_{emc}(t)$) increases greatly with the aging process.

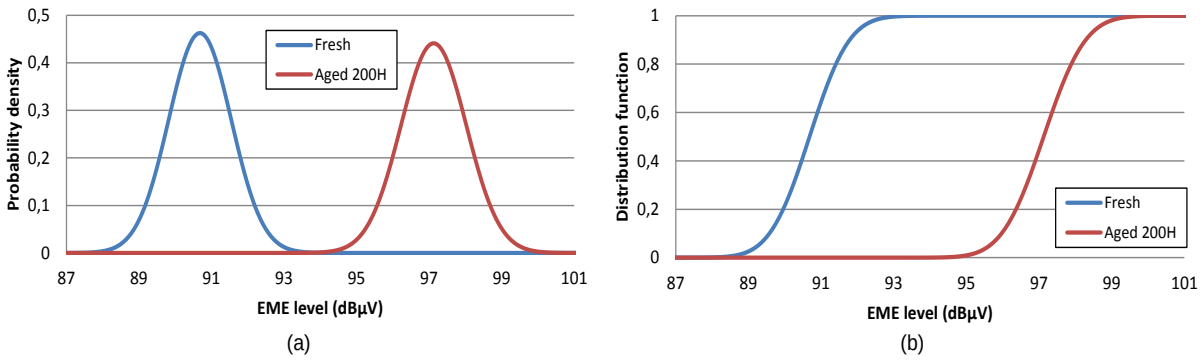

Figure V-20 Normal distribution of EME level before and after aging (200 hours): (a) Probability distribution functions; (b) Cumulative distribution functions

V.5.2.2. Extraction of EME reliability

With the measurement of EME distributions at each aging phase resumed in Table V-2, we can calculate the reliability probability and also the failure probability with time. Figure V-21 shows the EMC reliability function $R_{emc}(t)$ and EMC failure distribution function $F_{emc}(t)$ obtained with four different EME threshold. With the variation of the definition of EME limit, the reliability function and the failure probability change a lot.

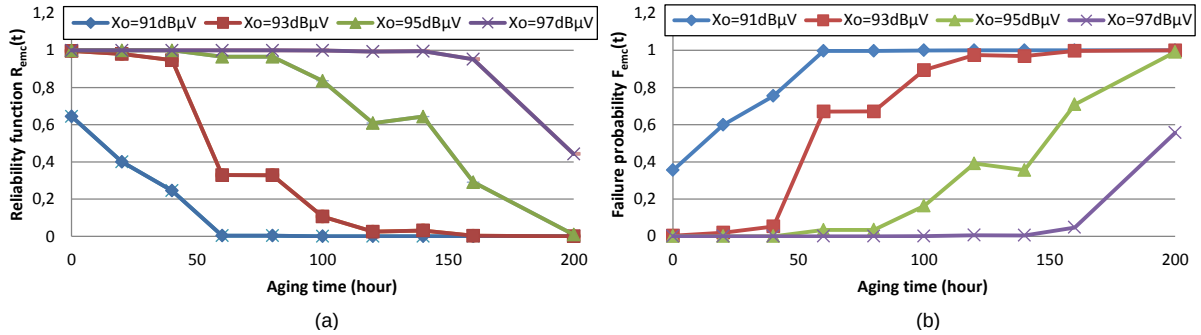

Figure V-21 Statistical distribution of EMC robustness for different emission level limits x_0 of EMC compliance: (a) Reliability function $R_{emc}(t)$; (b) EMC failure distribution $F_{emc}(t)$

Here the EMC failure probability with time could be used to extract the reliability distribution over time, using the graphical method which was presented in V.4.1.4. Here we suppose the EMC reliability follows the Weibull distribution. Because of its relatively ease of calculation, the Weibull distribution paper is applied to extract $F_{emc}(t)$ according to Equation V-31. The extraction method is described in Figure V-22.

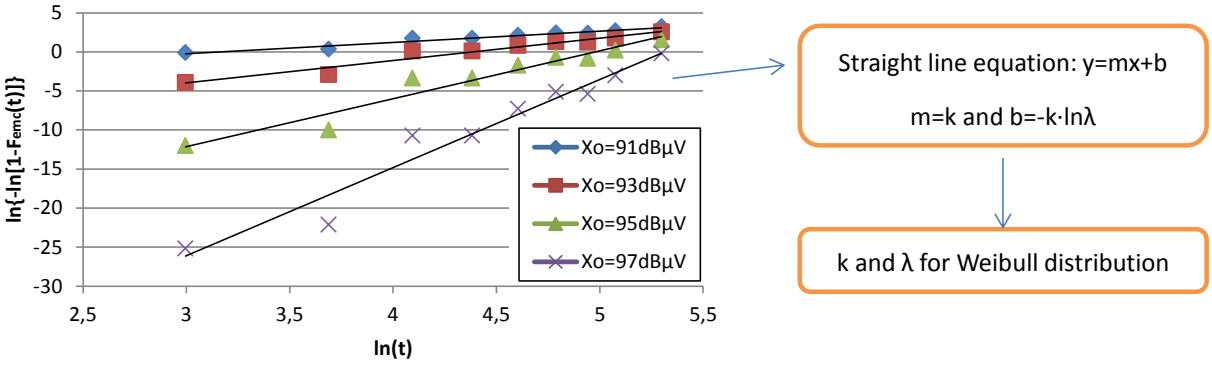

Figure V-22 $F_{emc}(t)$ extraction based on Weibull distribution paper for different emission thresholds x_0

The two parameters (k and λ in Equation V-26 and Equation V-27) of the Weibull distribution for different emission limits in Figure V-22 are resumed in Table V-3.

Table V-3 Two parameters of Weibull distribution of EMC reliability based on the measurements

Emission limit (dBµV)	91	93	95	97
Shape parameter k	1.45	2.86	6.13	11.28
Scale parameter λ	23.44	80.49	145.13	203.15
R^2 with measurements	0.9551	0.9476	0.9415	0.9526
MTTF (hour)	21.25	71.73	134.80	194.22

The extracted $F_{emc}(t)$ of Weibull distributions with four different EME limits are presented in Figure V-23. Here the failure distribution function $F_{emc}(t)$ fits very well with the evolution of the failure probability over time. The good quality of fitting between the failure distribution and the probability extracted from the measurement is resumed by the coefficient of determination R^2 in Table V-3. Besides, the MTTFs computed by the Weibull distribution are also resumed in this table, in order to demonstrate the mean time when EMC failure occurs.

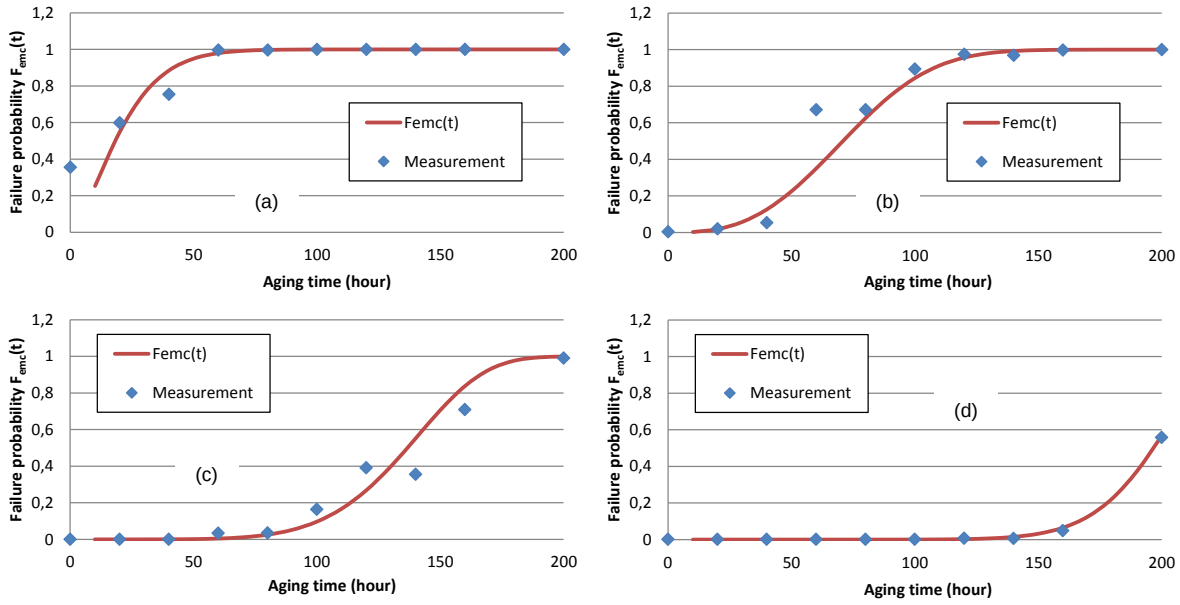

Figure V-23 Weibull distribution $F_{emc}(t)$ extracted from experimental measurements for four different EME limits: (a) 91 dBµV; (b) 93 dBµV; (c) 95 dBµV; (d) 97 dBµV

Based on the measurement results of several samples, the EME reliability distribution with time could be extracted. Because of the limited test time, the number of the tested samples and the measurement repeated times are also limited. Although the statistical analysis in this case study cannot achieve a very high confidence level, the EMC reliability extraction process is well demonstrated in this case study.

V.5.3. Prediction of EME reliability

V.5.3.1. Description of method

In the last chapter, the drifts of conducted emission level produced by a buck DC-DC converter with time was simulated based on the degradation models of the output filtering components, where the emission increase was explained by the decrease of the output filtering quality. Here, except the drift of EMC level induced by aging, we will also predict the evolution of the probability of EMC compliance with time.

Unlike the method presented in the last section which is based on EMC measurements at each aging phase, this method is based on the EME models and the statistical distributions of the parameters, which include the degradation parameters. The distributions of the parameters are extracted from the experimental measurement of the impedances of passive components and their evolution with time. As a reason of the limit of samples, the parameters in the EME models, including the degradation coefficient, are assumed to follow the normal distribution. The simulation is based on the Monte-Carlo method, because of its simplicity and good precision [RAYC08]. Besides, as the emission dispersion of the switching source is not available, here we use the model of the output filtering network presented in IV.6.4 to simulate the EMC drift and predict the EME reliability with time.

The output filtering network of DC-DC converter in Figure IV-82 is also used in this simulation. The S-parameters' simulation configuration of the output filtering network to extract by ADS are presented in Figure V-24. There are 10 variables in this model. They contain 6 initial parameters of two passive components and 4 degradation coefficients (k_1 for ESR, k_2 for C_0, k_3 for R_p and k_4 for C_p). Here in order to simplify the presentation, only the EMC reliability at 237 kHz is detailed below. However, the EMC reliability at other frequencies could also be extracted by this model with the accurate distribution of these variables.

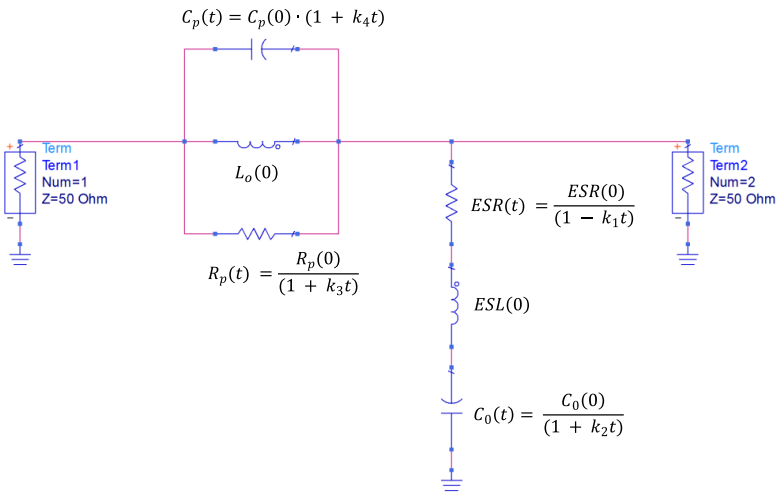

Figure V-24 Simulation configuration of S-parameters in ADS of the output filtering network

The random variables of 6 initial parameters of the inductance and the resistance in the filtering network in Figure V-24 are listed in Table V-4. Their statistical distributions are extracted from 16 samples of each. During the aging process, two parameters $L_0(0)$ and ESL(0) are almost unchanged. The aging impact on this LR filter can be represented by the variation of the resistance value, which can be expressed by the four functions with time, as presented in Chapter III. The statistical distributions of the aging coefficients are resumed in Table V-5. Their statistical parameters are based on 4 tested samples of output filtering components (C1 and L2) under the same aging conditions.

Table V-4 **Random variables of the initial parameters in the output filtering network and their mean and variance value**

Random variable	L_0 (µH)	C_P (pF)	R_P(kΩ)	R_0 (Ω)	C_0(µF)	ESL (nH)
Mean	21.84	17.2	14.5	1.01	100.02	2.98
Standard deviation	1.32	0.93	1	0.03	0.52	0.14

Table V-5 **Random variables of the degradation coefficients in the output filtering network and their mean and variance value**

Random variable	k_1 (C1)	k_2 (C1)	k_3 (L2)	k_4 (L2)
Mean	3.45e-3	8.60E-4	0.227	0.015
Standard deviation	1.9e-4	5.82E-5	0.144	0.011

V.5.3.2. Simulation of EME reliability

We suppose the variables in Figure V-24 are all normally distributed with the parameters listed in Table V-4 and Table V-5. We use the Monte Carlo simulation tool in ADS to simulate the distribution of the S_{21} value of the output LR filter [RAYC08]. At each aging time, the simulation applies 5000 random samples, because this sample number could get a good accuracy in a relatively short time. The simulation results are presented in Figure V-25, where the transmission coefficient S_{21} is expressed in dB.

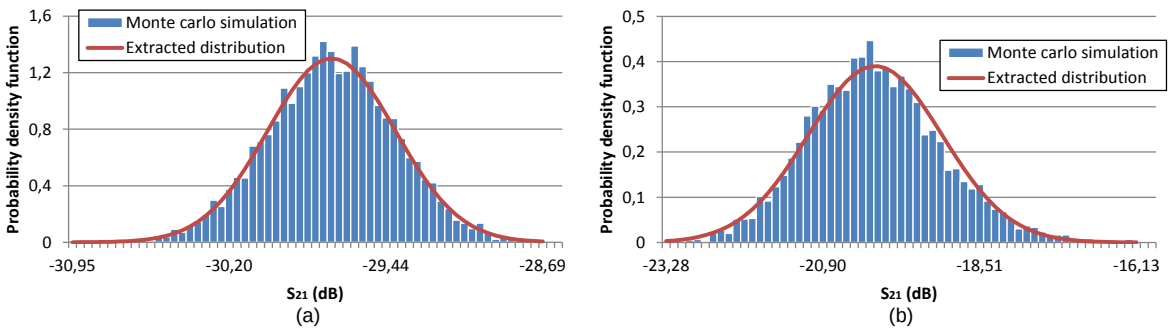

Figure V-25 **Monte Carlo simulation results of the forward voltage gain S_{21} and the extracted normal distribution in unit dB: (a) Before aging; (b) After aging 200 hours**

At each aging phase a normal distribution can be extracted. The extracted distributions' parameters of several aging phase are listed in Table V-6. The distributions of the drift of S_{21} are also resumed in this table, calculated by the difference of S_{21} before and after aging, according to Equation V-21. An increase in the average value and variance is observed over time.

Table V-6 Normal distribution parameters of S_{21}, its drifts and EMC level at difference aging phases

Aging time t (hour)	Mean of S_{21}	Variance of S_{21}	Mean of S_{21} drift	Variance of S_{21} drift	Mean of EMC level	Variance of EMC level
0	-29.705	0.094	0	0	90.68	0.74
20	-29.106	0.096	0.599	0.002	91.279	0.742
40	-28.464	0.1	1.241	0.006	91.921	0.746
60	-27.766	0.103	1.939	0.009	92.619	0.749
80	-27.605	0.121	2.1	0.027	92.78	0.767
100	-26.17	0.144	3.535	0.05	94.215	0.79
120	-25.253	0.194	4.452	0.1	95.132	0.84
140	-24.229	0.262	5.476	0.168	96.156	0.908
160	-23.067	0.396	6.638	0.302	97.318	1.042
180	-21.716	0.625	7.989	0.531	98.669	1.271
200	-20.101	1.045	9.604	0.951	100.284	1.691

As analyzed above, the EME drift at 237 kHz could be explained by the drift of S_{21} induced by the degradation of the output filtering aluminum capacitors. According to Equation V-19, the EMC level after aging could be obtained by the addition of the initial EMC level and the EMC drift, where initial EMC distribution could be extracted from measurements of fresh samples. The distribution parameters at different aging phases are also resumed in Table V-6. According to these distribution parameters, the same extraction process of Weibull distribution used in the last section with Weibull paper are applied here. The two parameters (k and λ) of Weibull distribution for different emission limits are resumed in Table V-7. We can find here the values extracted by simulation and also the MTTF are closed to that extracted based on the measurement results in Table V-3.

Table V-7 Two parameters of Weibull distribution of EMC reliability extracted by simulation

Emission limit (dBµV)	91	93	95	97
Shape parameter k	1.57	3.08	6.63	12.723
Scale parameter λ	24.61	77.05	134.03	175.72
MTTF (hour)	22.10	68.89	125.02	168.75

The failure distribution functions $F_{emc}(t)$ extracted by the simulation is shown in Figure V-26. The comparison between the distribution functions based on measurement and simulation approaches demonstrates a good fitting, especially in the short aging period (less than 100 hours), and for low EME limit. The difference between two distributions could be explained by the small number of samples in the measurement, and the accuracy of the degradation distribution model of capacitors. Besides, as the normal distribution applied is considered as unbounded, we lose the precision when the values are distant from the average value.

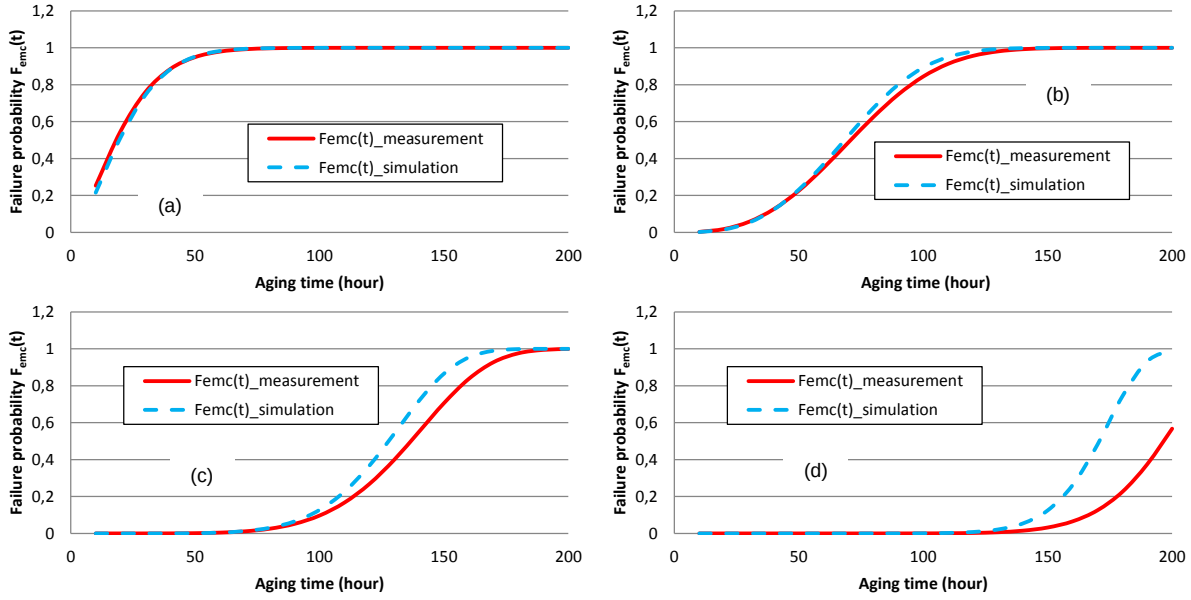

Figure V-26 Comparison of the failure distribution functions $F_{emc}(t)$ extracted respectively based on the measurement results and on the simulation for different EME threshold at 237 kHz: (a) 91 dBµV; (b) 93 dBµV; (c) 95 dBµV; (d) 97 dBµV

The simulation method could be also applied at other frequencies, like the emission level at 70 MHz whose evolution is also studied in IV.6. At this frequency the emission increase is mainly related with the degradation of the inductor. The converters with the same output filtering inductor (ID of the inductor is L2 in IV.6) are selected as the samples. The complete model of output filtering network in Figure V-24 is used. The comparison between the failure probability functions based on respectively the measurement and the simulation is shown in Figure V-27. Like the distribution at 237 kHz, here the EMC reliability also follows a Weibull distribution. The results demonstrate a larger difference

between the measurement and the simulation than that at 237 kHz. Here two parameters of the inductor are dependent on time, and they affect the emission level at this frequency. The dispersion of the degradation coefficient of these two parameters (k_3 for R_p and k_4 for C_p) are much greater than that of k_1 for ESR at 237 kHz, as resumed in Table V-5.

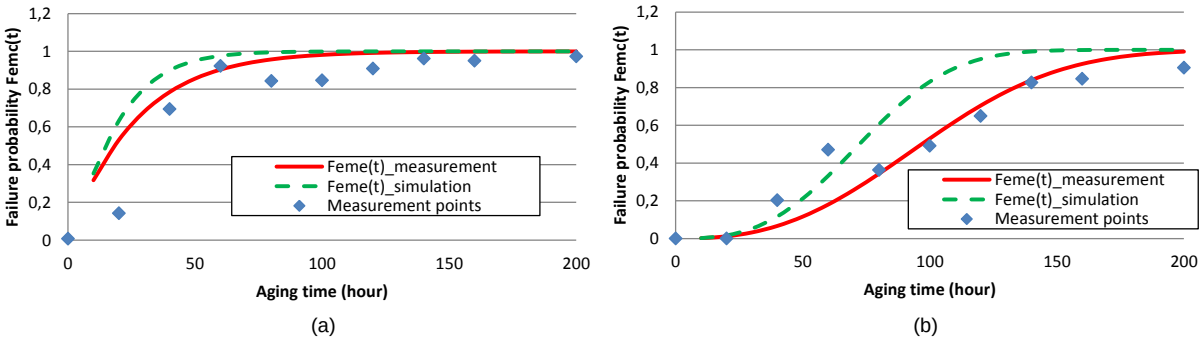

Figure V-27 Comparison of the failure distribution functions Femc(t) extracted respectively based on the measurement results and on the simulation for different EME threshold at 70 MHz: (a) 39 dBµV; (b) 41 dBµV

The simulation method in this study could be applied in other applications. If we have accurate degradation models of the internal components, we can use this method to predict the EMC drift and EMC reliability.

V.5.4. Conclusion of case study

As the result of the dispersion of the aging impact of the output passive filtering components, the significant difference of the emission level after aging could be observed between the buck DC-DC converters. In this case study, two approaches have been applied to extract the emission distribution at each aging phase and the EME reliability distribution functions ($R_{emc}(t)$ or $F_{emc}(t)$) with the aging time. One approach is based on the electromagnetic emission measurements along the aging process, and another is based on Monte Carlo simulation with the statistical distribution of degraded components. In both approaches, the Weibull distributions are selected as the EMC reliability distributions, and they are extracted by the method of distribution paper.

In this case study, we have still a lot of limits, like the samples' quantity which is not enough large to achieve a high confidence level. Moreover, normal distribution of the EMC level is assumed. However, the extraction processes are well explained in this study, and the extracted EMC reliability functions demonstrate a good fitting with the measurement results.

V.6. Conclusion

Because of the dispersion between the different samples, the EMC levels could not be presented simply by an average EMC level but by a statistical distribution. For a given EMC failure definition, a probability of EMC compliance should be provided. Since the EMC levels could be impacted by the

aging stresses, the probability of EMC compliance might evolve with aging time, and its evolution could be expressed by a EMC reliability distribution with time $R_{emc}(t)$ (or a EMC failure probability with time $F_{emc}(t)$ for the probability of EMC non-compliance).

As presented in Chapter II, the reliability of the electronic devices is basically a statistical problem. Although the EMC dispersion is a very common phenomenon, the statistical analysis is still not commonly applied in the EMC studies. In this chapter, the statistical analysis methods for the EMC characterization, especially for the EMC reliability, are presented. Several common distribution types used for both EMC levels and reliability analysis are explained. Also the methods to calculate the EMC drift and to extract the EMC reliability distribution are detailed in this study.

A case study about the EME reliability analysis of a buck DC-DC converter is presented in the end of this chapter. The distribution of EME level at each aging phase and the EME reliability for different emission limits are extracted according to the measurement results and the simulation, respectively. Although there are still some limits like the number of samples, two extraction approaches are well detailed in this case study. The Weibull distribution is used to model the evolution of the EMC reliability, and the results demonstrate a good correlation. With these methods, the EME reliability (or failure) probability with aging time of the output conducted emission of DC-DC converter could be well predicted.

With these methods of EMC reliability presented in this chapter, we could analyze the EMC distribution and the EMC compliance probability (or EMC failure probability) at each aging phase, and we can also study their evolution over time. Besides, other statistical parameters, like the mean failure time, failure rate could be served for the safety analysis in the practice. The random variation is a general phenomenon in EMC and reliability studies. Except the case study of the DC-DC converter, the EMC reliability analysis presented in this chapter could be applied for more EMR studies.

However, as a statistical analysis, more statistical notions could be used in the EMC reliability study, like the confidence level, the sample numbers, and more statistical distributions. Because of the limit of time, they are not all detailed in this study, but they could be useful in future studies about EMR. Besides, some conclusions in this study, like the statistical distribution of the aging coefficient of passive components, are still based on assumption. More EMC reliability cases studies are needed to achieve more systematical EMC reliability analysis.

Moreover, the computational simulation method like Monte-Carlo method is used in this study, which could assure a good precision. However, with the increase of the system's complexity and the number of variables, how to improve the efficacy of simulation like the Monte-Carlo method should be studied in future studies.

V.7. Reference

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Chapter VI. General conclusion

During the operating lifetime of electronic components, which include the integrated circuits and the passive components, their performances might be affected by failure mechanisms. Especially under the harsh environment, like the extreme temperature or electrical overstress, the degradation of electronic components could be accelerated. The EMC level of the electronic systems at IC level and at PCB level, such as the EM emission and immunity level could be also strongly impacted. As a result, the study of the long-term EMC level, which is called "electromagnetic robustness", appeared in the recent years. In this study, the long-term evolution of the EMC levels of two electronic component groups has been studied. The first electronic component type is the integrated circuit. The high-frequency currents and voltages during the switching activities of ICs are responsible for unintentional emissions or coupling. Besides, ICs are also very often the victim of electromagnetic interference. Another group of components is the passive component. In an electronic system, the IC components usually work together with the passive components at PCB level. The functions of passive components in an electronic system, such as filtering and decoupling, also have an important influence on the EMC levels.

In order to analyze the long-term evolution of the EMC level of the electronic components, the study in this thesis tends to propose general predictive methods for the electromagnetic compatibility levels of electronic components which evolve with time.

Except the general introduction in Chapter I, the manuscript of this thesis has been divided in four chapters.

The state of the art for the research context has been presented in Chapter II. The development of the technology does not only induce improvement of the performance of circuits, but also the growth of the circuit complexity, higher switching frequencies and reduced supply voltage. As a result, the electromagnetic compatibility has become an important concern for the electronic systems at circuit level and at PCB level. Besides, the degradations of the electronic devices induced by aging during the operating time could also affect the EMC level. The presentation in this chapter has begun from the global EMC domain. Then the EMC issue of integrated circuits has been presented, which includes the mechanisms, the influences of technology evolution, measurement standards and modeling methods. Finally we discussed the EM robustness issue, which is a combination study of "EMC" and

"reliability". A general EMR prediction flow has been proposed in the end of this chapter. This chapter provides an explicit location of the work and also the definition of the objective of this thesis.

As the source of EMC evolution induced by aging, the reliability issue of electronic devices has discussed in Chapter III. The basic reliability notions of electronic devices and the accelerated aging tests have been presented in the beginning of this chapter. Then the degradation mechanisms, characterization and modeling methods of two groups of electronic components, the semiconductor components and passive components have been discussed, respectively. The main degradation mechanisms which relate to the defect of the gate oxide of transistor which affects the transistor physical parameters, like HCI, TDDB and NBTI of semiconductor transistors have been introduced. These mechanisms can induce drift of electrical parameters of transistors and thus change the EMC levels gradually with time. Then several former studies about the characterization and the modeling of these degradation mechanisms have been resumed. Besides, the aging impacts on three typical passives components (capacitors, inductors and resistors) have been introduced. The aging characterization of impedance measurement and degradation modeling methods of passive devices were also presented. In the end, a case study describes experimental tests of the variation of passive devices' impedance after different accelerated aging conditions. From these experiments, the degradation models of two typical passive components (electrolytic capacitors and iron powder inductors) have been constructed.

Chapter IV has presented the EMR characterization and modeling methods, which is another important part of EMC prediction process. The general characterization flow of EMC evolution during the aging time and the EMC modeling methods has been presented. Considering the protection of intellectual propriety, the alternative black-box modeling methods were also discussed. Besides, the validity method FSV of the model in the EMC simulation has been introduced. In the end of this chapter, two cases studies presented respectively the prediction process for electromagnetic immunity evolution of an operational amplifier and electromagnetic emission evolution of a DC-DC converter. In each case study an alternative modeling method has been proposed. In the study of op-amp, the black-box modeling method at PCB level has been applied. While in the study of DC-DC converter, the EME drifts are obtained from the degradation modeling of passive filtering components instead of the modeling of whole system. Both case studies have demonstrated satisfactory simulation results with the measurement data.

Finally, the statistical analysis for the EMR study is discussed in Chapter V. As the aging impact on different components of the same reference might differ from one to another, the evolution of EMC level of a sample group is not only the deterministic variation of the emission or immunity level, but also the statistical distribution of the EMC level and the probability of EMC compliance for a defined EMC limit (called "EMC reliability" in this study) at each aging phase. The common statistical distributions of EMC level and some common distributions used in the reliability study of electronic

devices have been presented. The notions of "EMC reliability" were defined and the statistical analysis methods used in prediction of long term "EMC reliability" were presented. In the end, the statistical analysis of the emission drift of the DC-DC buck converter is presented to demonstrate the detailed process of the proposed methods.

There are several original points of this study:

- The general methodology to predict the variation of EMC level at circuit level and at PCB level is proposed in this study, which consists the modeling of EMC level and the degradation modeling of the electronic components with time. The presented case studies have validated the EMR modeling flow.
- The statistical analysis is applied in the EMR study. The notion of "EMC reliability" is presented, which quantifies the evolution of the probability of EMC compliance.
- As an alternative method, the black box modeling methods to protect the intellectual propriety in the EMR study are discussed.
- The degradation models of several typical electronic components are constructed in this study. Especially, the degradation models of powder iron inductors are constructed for the first time.

Besides, some improvements and perspectives of the EMR study can be applied in future works:

- As a result of the limit of time, not all the modeling methods proposed below are applied in the case studies, and the samples' type and number are also limited. More samples are needed in the future to verify and improve the models proposed in this study.
- The construction of the degradation models' library of different components (both active and passive components) under different operating/stress conditions could be the source very useful for the future EMR modeling study. As a result, more studies of the degradation mechanisms of electronic devices are required to extract the precise degradation models. Besides, in this study the influences of temperature and bias are not taken into account in the model of electronic components, they should be studied in future works.
- Some other statistical notions like the confidence level, the sample numbers, and more statistical distributions could be applied in the EMC reliability study. Then, more EMC reliability case studies are needed to achieve more systematical EMC reliability analysis.

The EMR study is a mixed research of "Reliability" and "EMC". Thus other improvements of both characterization and modeling methods in these scientific and technical domains could be served for the future study of the prediction of EMC level with time.

Chapter VII. Résumé en français

VII.1. Introduction

Le problème étudié dans cette thèse est dédié à la prédiction de l'évolution de la compatibilité électromagnétique (CEM) à long terme au niveau circuit intégré et circuit imprimé (PCB). Cette évolution est liée à la dégradation des circuits intégrés et des composants passifs.

En raison de leurs nombreux avantages (tels que le faible coût, la taille et le poids limité, la basse consommation d'énergie, et la haute performance, ...), les circuits intégrés sont largement utilisés dans les systèmes électroniques. Avec le développement de la technologie depuis l'invention des circuits intégrés en 1958, leurs performances (comme la vitesse de fonctionnement) ont été grandement améliorées. En parallèle, les circuits intégrés prennent également une part de plus en plus importante dans les études de compatibilité électromagnétiques. Les circuits intégrés sont une source importante de signaux et de bruit qui produisent des interférences électromagnétiques. Les courants de haute fréquence et les tensions induits au cours de leurs activités de commutation sont responsables des émissions non intentionnelles ou couplage. En outre, les circuits intégrés sont aussi très souvent les victimes d'interférences électromagnétiques. Dans un système électronique, les composants de circuits intégrés fonctionnent souvent avec des composants passifs. Les fonctions des composants passifs dans un système électronique, telles que le filtrage et le découplage, ont également une influence importante sur les niveaux de CEM. Pour cette raison, des lignes directrices de conception de CEM pour les circuits intégrés et les systèmes électroniques sont nécessaires, afin d'obtenir de meilleures performances de CEM. Une autre tendance importante est l'application de la simulation au cours de la phase de conception pour prévoir les niveaux CEM avant la fabrication des produits finaux. Tous ces travaux visent à rendre les produits électroniques conformes aux exigences de CEM des clients ou des normes [BEND06] [REDO10] [VRIG05].

Cependant, toutes les vérifications de la conformité CEM sont appliquées avant la livraison des produits finis. Donc nous pourrions avoir de nouvelles questions sur les performances CEM des systèmes électroniques au cours de leur vie. Les comportements CEM de ces produits seront-ils toujours conformes dans plusieurs années ? Un produit peut-il garder les mêmes performances CEM pendant toute sa durée de vie ? Si non, combien de temps la conformité CEM du système peut-elle être maintenue ?

Donc, l'étude vient à une autre activité de recherche sur la fiabilité des composants électroniques. Le phénomène du vieillissement est très normal pour les appareils électroniques. Pendant la durée de fonctionnement des composants électroniques, leurs performances peuvent être affectées par des mécanismes de défaillance. Surtout dans les environnements hostiles, soumis à des températures extrêmes ou des surcharges électriques, la dégradation des composants électroniques est accélérée. Parfois, les mécanismes de défaillance ne compromettent pas le fonctionnement du système, mais ils peuvent avoir un impact significatif sur la CEM. Les niveaux CEM des systèmes électroniques au niveau des circuits intégrés et au des PCB, tels que les niveaux d'émission et d'immunité, peuvent également être fortement impactés. L'étude à long terme de l'évolution des niveaux CEM, appelée "robustesse électromagnétique (REM) », est apparue ces dernières années. Les travaux précédents ont montré que la dégradation causée par le vieillissement pouvait induire des défaillances des systèmes électroniques, y compris une évolution de la compatibilité électromagnétique. La nécessité de prévoir la CEM des systèmes électroniques après plusieurs années de durée de vie est entraînée par la tendance à l'extension de garantie [BEND13].

Par exemple, dans le cas d'un équipement électronique embarqué dans un avion, une grande quantité de circuits sont intégrés. La température de fonctionnement extrême de l'avion à haute altitude (de -55 ° C à 125 ° C [LI11]) peut accélérer le processus de vieillissement des appareils électroniques. La durée du service d'un avion commercial est aussi très longue (au moins 30 ans). En conséquence, un haut niveau d'exigence en sécurité et en fiabilité est nécessaire. Ainsi, il est très important d'assurer que les systèmes électroniques restent conformes aux exigences CEM pendant toute leur durée de vie. La méthode actuelle utilisée dans la spécification d'équipements aéronautiques est de dimensionner une grande marge de sécurité de CEM au cours de la phase de conception pour assurer que les niveaux CEM restent acceptables pendant des années. Cependant, l'analyse de la CEM à long terme présentée dans cette étude pourrait également être utile afin de prévoir et de vérifier la fiabilité de la conformité CEM avec le temps.

Afin d'analyser l'évolution à long terme des niveaux CEM des composants électroniques, les travaux présentés dans cette thèse ont pour objectif de proposer des méthodes générales pour prédire l'évolution dans le temps des niveaux de compatibilité électromagnétique des composants électroniques.

La thèse est organisée comme suit:

Le chapitre II détaille l'état de l'art. Il commence par une présentation globale du domaine CEM et son évolution historique. Ensuite, la présentation de la CEM des circuits intégrés comprend les mécanismes, les influences de l'évolution de la technologie, les normes de mesure et les méthodes de modélisation. Enfin, le problème de la REM et les objectifs de cette étude sont présentés.

Le chapitre III décrit les mécanismes de dégradation des composants à la source de l'évolution CEM. Après une introduction à la fiabilité des composants électroniques et les conditions stress de vieillissement, les mécanismes de dégradation et de la modélisation pour deux sortes de composants électroniques (transistors MOSFET dans les circuits intégrés et les composants passifs) sont présentés et analysés.

Le chapitre IV traite de la prédiction de l'évolution de la CEM avec le temps dans des conditions de vieillissement accéléré. Les méthodes générales de caractérisation et de modélisation sont discutées. Deux études de cas présentent respectivement le processus de prédiction pour l'évolution de l'émission électromagnétique et l'immunité électromagnétique. En outre, les méthodes alternatives de modélisation (les modèles dits boîte noire) sont présentés et discutés. Aussi la validité du modèle est définie.

Le chapitre V est consacré à l'analyse statistique pour l'étude de la REM. Il présente tout d'abord les éléments statistiques dans les études de REM. Ensuite, les méthodes statistiques dans la dégradation des composants et dans la modélisation de la dérive CEM sont discutées.

Enfin, la conclusion générale résume la contribution de cette thèse et offre des perspectives en ce qui concerne les travaux futurs.

VII.2. Compatibilité électromagnétique à long terme

VII.2.1. Contexte de la robustesse électromagnétique

La compatibilité électromagnétique est une performance importante pour les appareils électroniques. La compatibilité électromagnétique est définie comme «l'aptitude d'un appareil ou d'un système à fonctionner dans son environnement électromagnétique, de façon satisfaisante et sans produire lui-même des perturbations électromagnétiques intolérables pour tout ce qui se trouve dans cet environnement". Un dispositif électronique qualifié est également conforme aux normes CEM selon la norme ou de l'exigence du client. Cependant, avec le temps de fonctionnement, en particulier dans les conditions de fonctionnement difficiles, la dégradation des composants électroniques induite par le vieillissement pourrait produire une grande variation des niveaux CEM.

Aujourd'hui, les performances des appareils électroniques sont largement améliorées en raison de l'utilisation croissante de modules électroniques. Toutefois, la dégradation des pièces électroniques devient une source essentielle importante de défaillance du système [WHIT08] [VICH06]. La dégradation des composants électroniques peut être causée par le vieillissement au cours de l'exploitation du système, et certaines conditions peuvent accélérer le processus de vieillissement.

Il existe un grand nombre de travaux sur la détection de la dégradation et la prédiction de la défaillance du système. Mais toutes ces études visent plutôt à la prédiction de l'analyse de la

performance ou de la durée de vie du système, afin d'assurer la fonctionnalité à long terme dans une certaine marge. Cependant, l'évolution à long terme de la compatibilité électromagnétique des systèmes est souvent négligée.

Dans la Figure II-27, deux possibilités d'évolution inattendue des niveaux CEM sont illustrées. Ici, l'augmentation du niveau d'émission ou la diminution du niveau d'immunité dans certaines gammes de fréquence, provoquée par les mécanismes de vieillissement pendant la durée de fonctionnement des dispositifs, induit un niveau réduit de CEM. Lorsque la dérive de CEM d'un dispositif dépasse les limites d'exigence de certification CEM, ce dispositif n'est plus conforme aux normes CEM.

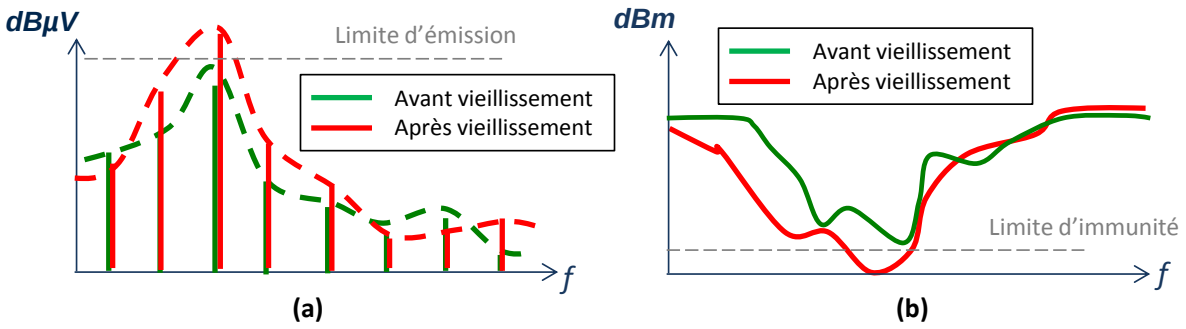

Figure VII-1 L'évolution possible des niveaux CEM après vieillissement: (a) le niveau d'émission électromagnétique, (b) le niveau d'immunité électromagnétique

Certaines études ont mis en évidence les risques possibles d'évolution de la CEM. Un exemple dans [LAHY98] est la dégradation des condensateurs électrolytiques, utilisés en tant que condensateur de filtrage de sortie d'un bloc d'alimentation à découpage. En raison de l'augmentation de la résistance série équivalente après 175 heures de vieillissement thermique, l'ondulation de tension de sortie a subi une augmentation significative. L'augmentation de l'amplitude de la tension d'ondulation signifie une augmentation de l'émission électromagnétique au niveau de la fréquence de commutation.

Les tests de CEM pour quantifier les composants sont souvent effectués uniquement sur les composants neufs après une phase dite de « burn-in » (permettant d'éliminer par "mortalité infantile" les composants présentant des défauts majeurs), en utilisant des méthodes d'essai normalisées. Bien que les essais de vieillissement accéléré soient appliqués pour assurer la fonctionnalité du système, généralement les niveaux de CEM ne sont pas caractérisés après le processus de vieillissement. Ainsi, la question de la CEM doit être étudiée avec les tests de fiabilité dans des conditions de vie réaliste, afin d'assurer la conformité CEM à long terme et la "sécurité fonctionnelle" pendant toute la durée de vie, comme suggéré [ARMS05].

VII.2.2. Prédiction de CEM évolution induite par le vieillissement

En raison d'une exigence accrue des performances et de la fiabilité des équipements électroniques, les fabricants de système sont forcés d'optimiser la fiabilité de leur système dans des délais réduits et

en contrôlant les coûts de fabrication. En conséquence, cette tendance a induit une augmentation de la demande à prédire les performances des équipements électroniques dès les étapes de conception, avec l'aide de la simulation [BEND13].

Le développement technologique des circuits intégrés apporte une amélioration des performances. Cependant, l'augmentation de la puissance dissipée et du courant de fuite génère plus d'émissions électromagnétiques. Les tensions d'alimentation réduites et l'augmentation du bruit électromagnétique ont tendance à diminuer l'immunité contre les interférences électromagnétiques. La CEM est devenue une cause majeure de la ré-conception des circuits intégrés [RAMD09] [LI11].

Simultanément, dans le cas de conditions de fonctionnement "difficiles", les mécanismes de dégradation sur les composants (comme les transistors MOSFET ou des composants passifs) sont accélérés [WHIT08]. Parfois, les mécanismes de défaillance ne compromettent pas le fonctionnement du circuit, et le système pourrait continuer à fonctionner sans défaillance, mais certaines performances (la fiabilité, la fréquence de fonctionnement, la marge de bruit statique ...) de dispositifs seraient dégradées. Parmi ces performances de circuits, les marges de CEM pourraient être affectées significativement par les dégradations intrinsèques des composants [LI11] [BEND13].

Plusieurs études de REM sur circuits intégrés ont déjà été publiées. Des publications comme [BOYE14] ont montré que l'émission électromagnétique de circuits numériques et d'E/S change avec le temps, en raison des mécanismes de dégradation intrinsèques aux transistors MOSFET. Comme présenté dans quelques œuvres, la simulation peut être utilisée pour prédire le niveau CEM à long terme. Par exemple, dans [BOYE11], les résultats de la simulation confirment l'évolution de la susceptibilité électromagnétique d'une boucle à verrouillage de phase avant et après vieillissement. Cependant, dans ces études de cas, seulement deux états du dispositif (avant et après une période de vieillissement) sont mesurés et simulés. Ainsi, il y a un manque de vision plus précise de l'évolution des niveaux CEM pendant toute la durée de vieillissement.

L'objectif de cette étude est de construire des modèles pour prédire l'évolution de la CEM liée à la dégradation des composants (circuits intégrés et composants passifs) induite par le vieillissement. Dans l'étude de la REM de cette thèse, la première étape est la caractérisation d'un circuit dans la mesure de son niveau d'émission et / ou de susceptibilité avant et après vieillissement. Nous avons besoin de prouver les effets du vieillissement sur la CEM et de comprendre le lien entre la dégradation physique des composants et les dérives de CEM. Ce lien doit être vérifié soit par des mesures expérimentales, soit par les analyses de simulation. Après l'identification de la source de dérive de CEM, nous pouvons commencer la procédure de la modélisation de REM. Ce processus devrait tenir compte des conditions opérationnelles et le temps de fonctionnement.

Le flux général de modélisation de REM est montré dans Figure II-34. Normalement, le modèle de CEM est présenté par un modèle électrique équivalent (ou un modèle 3D de carte électronique) de

l'ensemble du système qui contient non seulement les composants, mais aussi les circuits imprimés et l'environnement de test.

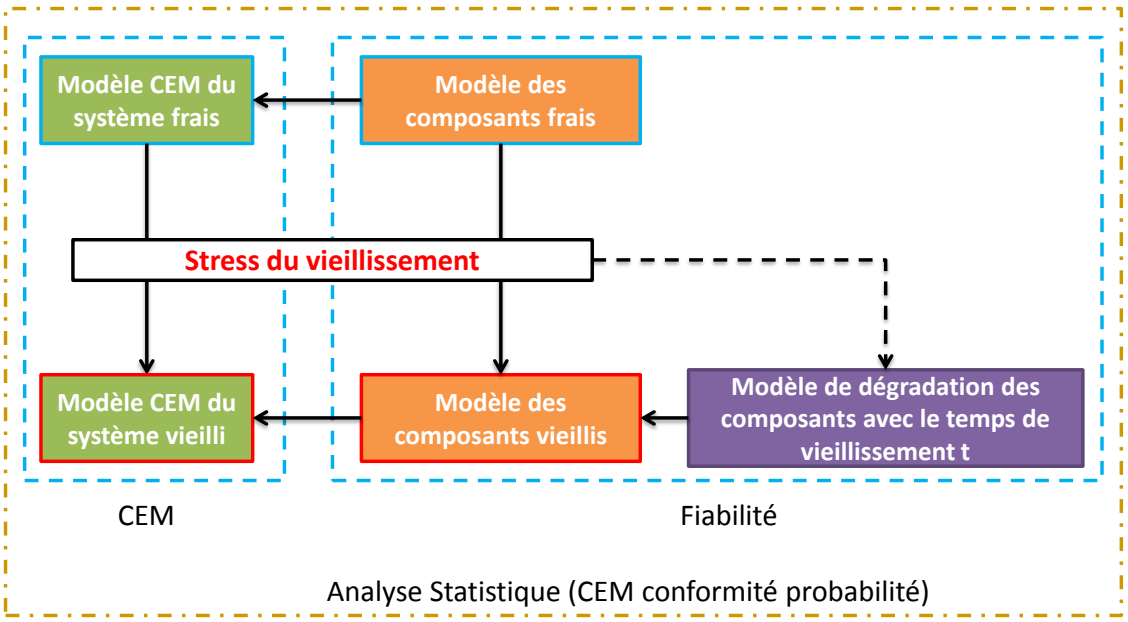

Figure VII-2 Flux de modélisation de REM

Le modèle de CEM pourrait être validé par la comparaison avec les mesures expérimentales. Si la dérive de CEM est causée uniquement par la dégradation de certains composants dans le système, nous pouvons ensuite utiliser la même structure de modélisation de CEM. La dégradation liée au vieillissement de deux types de composants: es circuits intégrés et les composants passifs sont étudiés ici. Ils sont supposés être la principale source de la dérive de CEM. Puis, avec l'intégration du modèle de composants vieillis dans le modèle de CEM, les niveaux de CEM à long terme peuvent être prédits. Le modèle de REM est la combinaison du modèle de «fiabilité» et le modèle "CEM".

Dans cette thèse, nous nous concentrons sur la prédiction de la dérive de CEM à long terme, et nous essayons de proposer une méthode générale de modélisation pour prédire l'impact du vieillissement sur les niveaux électromagnétiques. Pour atteindre cet objectif, les dégradations de composants, qui sont la source de vieillissement impact sur les niveaux de CEM, sont étudiés. De plus, les modèles de CEM sont basés sur les études existantes. Avec les modèles de dégradation injectés dans les modèles CEM, l'évolution des niveaux de CEM au fil du temps est étudiée dans deux études de cas: la dérive de l'émission électromagnétique d'un convertisseur DC-DC et la dérive de l'immunité électromagnétique d'un amplificateur opérationnel.

Comme l'existe une dispersion de l'effet de vieillissement sur différents échantillons dans les mêmes conditions de vieillissement, l'analyse statistique est nécessaire dans la modélisation de la REM. Avec l'analyse statistique, l'évolution de la CEM est non seulement l'évolution moyenne d'un seul échantillon, mais aussi le risque de la conformité CEM d'un groupe d'échantillon.

VII.3. Modélisation de la dégradation des composants

Aujourd'hui, la dégradation des composants électroniques devient une source essentielle importante de défaillance du système [BOWL92] [VICH06] [SAHA09]. Cette dégradation des composants induit la baisse des performances du système, incluant les niveaux de CEM. Le déclin de la performance en CEM peut augmenter la probabilité de défaillance inattendue du système [BEND05] [BEND13].

Plusieurs études précédentes ont montré que de petits changements dans les paramètres des composants peuvent provoquer une dérive importante des niveaux de CEM du système [BOYE09] [BOYE11] [WU13]. Dans la pratique, les différentes composantes du système ont des fiabilités différentes et certaines parties jouent un rôle plus important que les autres sur les niveaux de CEM. Ainsi, une bonne connaissance du système électronique est nécessaire pour identifier l'origine de l'évolution à long terme de la CEM.

Comme deux groupes typiques de composants électroniques, la dégradation des composants semi-conducteurs et des composants passifs sont présentées. Les principaux mécanismes de dégradation des transistors MOSFET sont introduits. Il existe différents mécanismes de dégradation en fonction des conditions de fonctionnement et de dégradation. Dans cette étude, trois mécanismes de dégradation sont présentées: « Hot carrier injection » (HCI), « Time dependent dielectric breakdown » (TDDB) et « Negative bias temperature instability » (NBTI). Ensuite, un état de l'art succinct sur la caractérisation et la modélisation de ces mécanismes de dégradation est proposé.

En outre, l'impact du vieillissement sur plusieurs composants passifs (condensateur, inductance et résistance) est introduit. La caractérisation et la modélisation du vieillissement de composants passifs sont présentées. Une étude de cas est utilisée pour montrer la variation de l'impédance de deux composants passifs (condensateurs électrolytiques et inductances de poudre de fer).

Plus de détails sur la modélisation des composants électroniques peuvent être trouvées dans le Chapitre III. Un point d'origine dans ce chapitre est l'étude sur l'impact du vieillissement sur inductance de poudre de fer, qui a été peu étudié dans les études antérieures. Cependant, comme peu d'informations sur sa dégradation sont disponibles sur ce composant, plus d'études sont nécessaires pour mieux comprendre le mécanisme de dégradation et les dérives causées par cette dégradation. Par ailleurs, comme la source de la dérive de CEM, les présentations de dégradation dans ce chapitre donnent un bon aperçu de l'analyse de l'évolution de CEM. En outre, avec les modèles de dégradation mis en place, la prédiction des niveaux de CEM avec le temps devient possible.

En raison de la limite de temps, toutes les méthodes de modélisation CEM ne sont pas appliquées dans les études de cas, et le nombre d'échantillons testés est également limité. Cependant, l'objectif de cette étude est de ne pas essayer de construire une bibliothèque complète de la modélisation de la

dégradation, mais de démontrer le processus et les points importants au cours du processus de modélisation de la dégradation. En outre, les modèles que nous avons choisis dans les études de cas sont applicables et simple, mais une bonne précision peut être assurée. Dans les études futures, un nombre d'échantillons plus large doit être testé afin de valider complètement et d'améliorer les modèles proposés. Par ailleurs, les influences de la température et de polarisation, notamment sur les composants passifs, ne sont pas prises en compte dans cette étude, mais ils devraient être étudiés dans les travaux futurs et ajoutés aux effets du vieillissement.

VII.4. Caractérisation et modélisation de la CEM à long terme

Nous avons discuté de la fiabilité des composants électroniques qui est une partie importante de l'étude de la REM. Les mécanismes de dégradation des composants électroniques (transistors actifs dans les circuits intégrés et composants passifs) causés par le vieillissement pourraient être la source de la dérive de CEM. Comme un autre élément important de l'étude REM, la caractérisation et la modélisation des niveaux CEM sont présentées dans Chapitre IV. Il commence avec la méthodologie de caractérisation de REM, où les mesures de CEM de circuits intégrés et des blocs électroniques samples sont détaillées. Plusieurs méthodes de modélisation de la CEM des circuits intégrés (ICEM, ICIM) sont détaillées dans la partie suivante. Par ailleurs, une alternative de simulation de la REM basée sur une modélisation confidentielle (boîte noire) est discutée. À la fin de ce chapitre, deux études de cas (l'évolution de l'immunité électromagnétique d'un amplificateur opérationnel et l'évolution de l'émission électromagnétique d'un convertisseur DC-DC) sont présentés pour démontrer la procédure de prédiction des niveaux de CEM.

VII.4.1. Caractérisation de la CEM à long terme

La caractérisation de la REM d'un circuit consiste à observer l'évolution de la CEM induite par le stress de vieillissement. L'objectif principal est d'évaluer l'émission et l'immunité électromagnétiques en fonction des conditions et de la durée de stress. Les tests de compatibilité électromagnétique sont sélectionnés de manière à assurer une bonne précision et une répétabilité suffisante. La construction du plan de test CEM doit être soigneusement optimisée pour assurer des erreurs de mesure contrôlables pendant toute la caractérisation de la REM. L'environnement des tests de compatibilité électromagnétique (les configurations de banc d'essai, les instruments expérimentaux, la température de l'environnement ...) doit rester inchangé, afin de réduire la variation des niveaux CEM causée par des facteurs autres que la dégradation du système liée au vieillissement.

En outre, le type de stress (les températures extrêmes, la forte humidité, les vibrations, les chocs, les surtensions ...) et le niveau de surcharge sont choisis en considérant la nature et l'application des composants testés. Pour toutes les expériences, les composants doivent être toujours fonctionnels sans dommages définitifs après vieillissement. Le vieillissement accéléré est également une source

d'incertitude, donc les conditions et la durée de vieillissement doivent être les mêmes pour tous les échantillons.

Pour caractériser l'évolution de la CEM au cours de la période de stress, les mesures de CEM et les autres caractérisations sont appliquées tout en interrompant le stress du vieillissement. En conséquence, avant le début de tous les essais, un programme de test détaillé est obligatoire, où la séquence de toutes les mesures de CEM et des essais vieillissement, la durée et la phase entre les différents tests doivent être définies.

Les normes CEI telles qu'IEC 61967 et IEC 62132 proposent plusieurs mesures de la CEM dédiées aux circuits intégrés. En général, les méthodes de mesure conduite sont considérées plus reproductibles que les méthodes de mesure rayonnée. En effet, le couplage du rayonnement est fortement influencé par la configuration de mesure (distance, orientation des antennes de mesure) et par l'environnement de test. Par exemple, il est admis que l'incertitude de mesure de l'émission rayonnée dans une chambre anéchoïque est de 6 dB. En outre, les dimensions des circuits intégres sont relativement petites, en faisant des antennes faiblement efficaces.. La mesure électromagnétique rayonné d'un circuit est facilement perturbée par les émissions générées par les pistes des circuits imprimées ou les câbles d'alimentation. Parmi toutes les méthodes de mesure rayonnée, la méthode de la cellule TEM / GTEM (CEI 61967-2 et 62132-2) a une bonne isolation vis-à-vis de l'environnement externe et une répétabilité acceptable. Cependant, la méthode TEM / GTEM fournit une mesure globale du système et pas d'un circuit. Elle n'est donc pas appliquée dans cette étude, dédiée aux composants. Enfin, deux méthodes de mesure conduite (Mesure des émissions conduites: 1 Ω / 150 Ω méthode de couplage direct, et Mesure de l'immunité conduite: méthode d'injection de puissance RF directe) sont choisies dans nos tests, parce que leur niveau d'incertitude et de répétabilité sont acceptables pour assurer la cohérence des résultats de REM.

VII.4.2. Modélisation de la CEM à long terme

Plusieurs méthodes de modélisation ont été proposées pour simuler les problèmes d'émission et d'immunité des circuits intégrés. Cette étude décrit deux méthodes de modélisation pour les niveaux CEM de circuits intégrés (ICEM : « Integrated Circuits Emission Model » et ICIM : « Integrated Circuits Immunity Model »), qui pourraient être appliquées à l'étude de REM pour la modélisation des niveaux CEM au cours de chaque phase de vieillissement. Ces deux méthodes sont détaillées dans le Chapitre IV.

Plusieurs études antérieures comme [BEND13], [BOYE14_a] et [WU13] ont démontré que la variation significative des niveaux de CEM a eu lieu après le stress de vieillissement, et la variation de CEM dépend beaucoup des conditions de fonctionnement et la durée de stress. Dans cette étude, nous avons tenté de développer une méthodologie de modélisation générale de la REM, qui se consacre à prédire l'évolution de CEM à long terme. Une méthodologie générale utilisée pour simuler la dérive

de la CEM induite par le vieillissement est décrit dans la Figure VII-3. Plusieurs parties de ce flux de modélisation, comme la modélisation de CEM avant et après vieillissement a été pratiqué dans plusieurs études pour analyser la dérive de CEM, comme la dérive d'émission d'un composant numérique dans [BOYE13] et la dérive de l'immunité d'une boucle à verrouillage de phase dans [BOYE11]. Toutefois, seulement deux états de vieillissement (frais et vieilli) sont analysés dans ces études, donc une analyse plus précise de la REM lors des différentes phases de l'ensemble du temps de vieillissement est nécessaire.

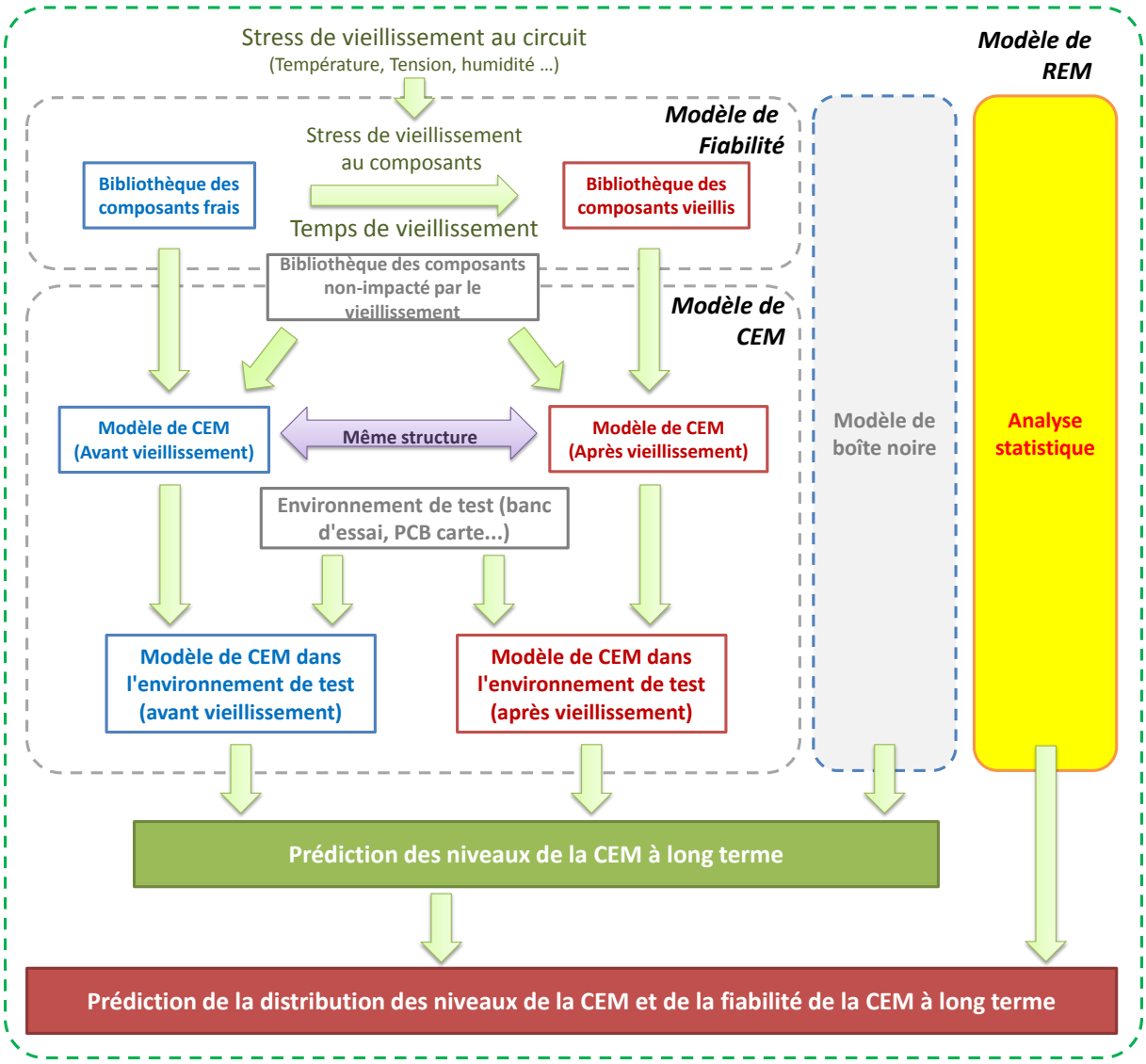

Figure VII-3 Flux de la prédiction de la CEM à long terme

L'objectif de ce projet de modèle de prédiction de REM est que dans l'étape de conception, nous pourrions prédire les niveaux CEM des circuits sur le long terme avec un environnement d'exploitation prédéfinie. Puis, avec l'analyse statistique, nous pourrions obtenir la distribution statistique des niveaux CEM au cours de chaque phase de vieillissement, et de prévoir également la probabilité de la conformité CEM. Généralement, le processus de modélisation comprend deux

grandes parties: la modélisation de la fiabilité des composants dégradés, la modélisation de la CEM des circuits intégrés et des blocs électroniques. En outre, pour la raison de la protection de la propriété intellectuelle, le modèle de boîte noire pourrait être une méthode alternative dans le modèle de prédiction de REM. Par ailleurs, l'analyse statistique, comme la dispersion de l'impact du vieillissement entre les différents échantillons, pourrait être un facteur supplémentaire dans le modèle pour prédire non seulement la valeur de dérive de la CEM, mais aussi la distribution à long terme des niveaux de CEM et de la probabilité de non-conformité CEM.

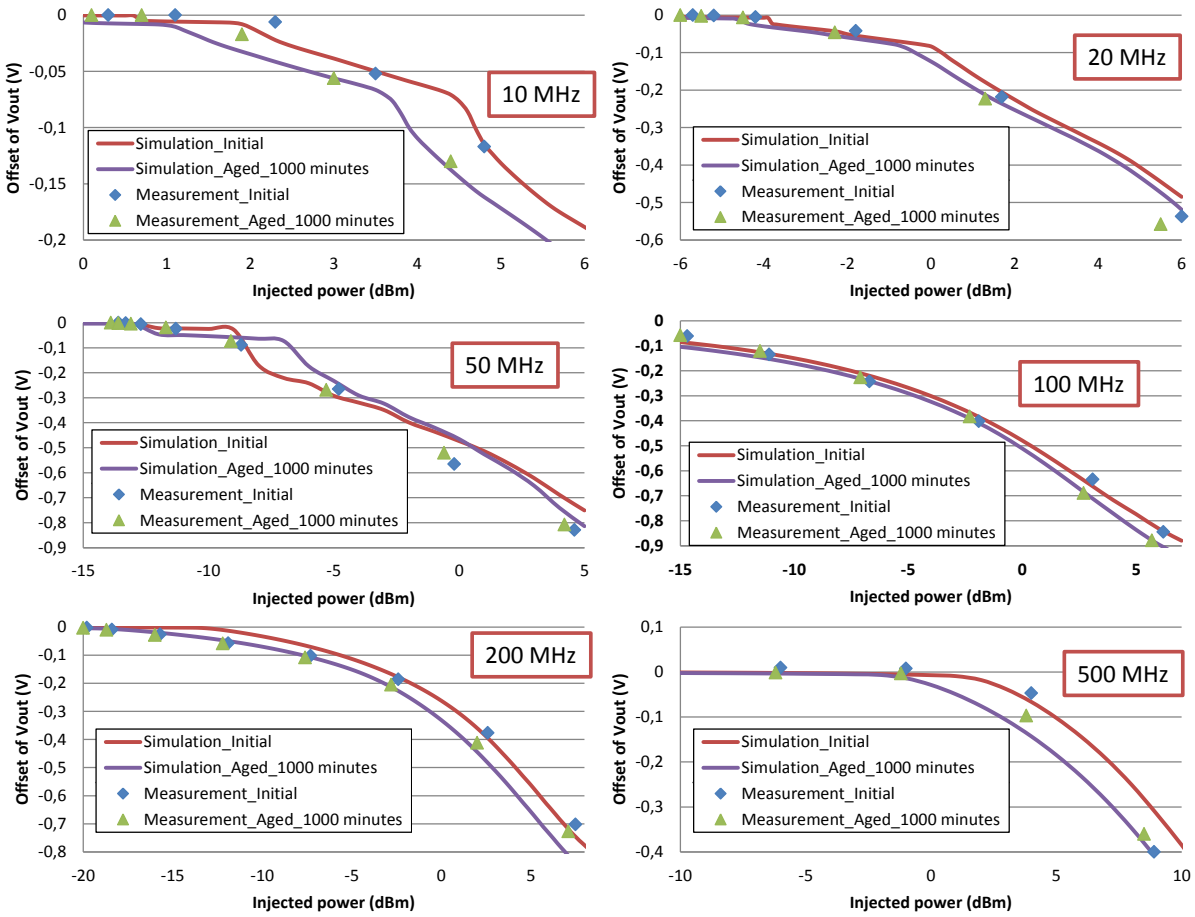

Figure VII-4 Comparaison de l'offset d'un amplificateur entre les simulations et les mesures avant et après le vieillissement à des fréquences différentes

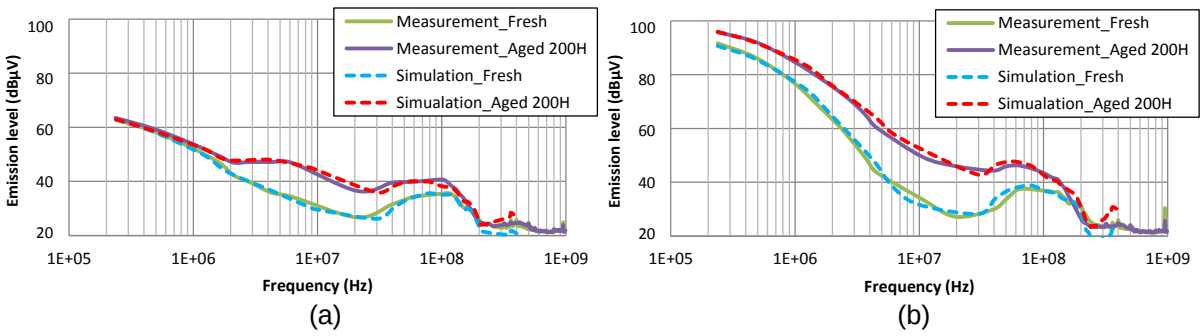

Figure VII-5 Comparaison de l'émission électromagnétique d'un DC-DC convertisseur entre les simulations et les mesures avant et après le vieillissement des cartes différentes

Basé sur le processus général de modélisation de la REM, le Chapitre IV a démontré l'application de ce processus de modélisation par deux études de cas. La première étude de cas est la prédiction de l'impact de vieillissement sur l'immunité d'un amplificateur opérationnel. L'essai de vieillissement montre que le niveau d'immunité diminue après vieillissement sur une large bande de fréquences. Ensuite, avec la modélisation de l'impact des transistors vieillis, l'effet du vieillissement sur l'immunité est correctement prédit. La deuxième étude de cas est la prédiction de l'évolution de l'émission électromagnétique (EME) d'un convertisseur DC-DC. Ce travail est plutôt l'étude de la CEM au niveau d'un circuit imprimée embarquant plusieurs composants vieillis. Nous avons analysé la dérive d'émission électromagnétique du convertisseur. Les rôles des composants passifs de filtrage sur la dérive de l'EME ont également été discutés. Avec l'application de modèles de dégradation des composants passifs dans l'ensemble du modèle de CEM du convertisseur, nous pouvons prédire l'évolution du niveau d'émission sous les conditions du vieillissement thermique.

Basée sur le flux général de modélisation de la REM dans la Figure VII-3, ces deux études de cas ont présenté des résultats de modélisation satisfaisants, comme démontré dans Figure IV-61 et Figure IV-79. En outre, dans chaque étude de cas, nous avons proposé une méthode alternative pour la modélisation de CEM à long terme. Dans l'étude de l'amplificateur, une modélisation de type boîte noire, cachant toutes les informations confidentielles derrière un modèle mathématique équivalent, a été appliquée. En outre, dans l'étude sur le convertisseur DC-DC, la dérive d'émission électromagnétique peut être obtenue simplement à partir de la modélisation de la dégradation des composants passifs au lieu de la modélisation du système entier.

VII.5. Analyse statistique pour la prédiction de la REM

Les études antérieures à cette thèse ont démontré que les niveaux de CEM varient considérablement dans des conditions de fonctionnement difficiles, en raison de la dégradation de composants (circuits intégrés et composants passifs). En outre, les évolutions CEM peuvent être prédites par des simulations basées sur la modélisation de la dégradation des composants.

Cependant, les études ci-dessus ont également révélé que l'ampleur des dérives des niveaux CEM liées au vieillissement sur plusieurs échantillons d'une même référence de composant peut variée de l'un à l'autre. En raison de la nature aléatoire du vieillissement, les systèmes électroniques présentent des comportements stochastiques dans l'évolution de leurs paramètres et de leurs réponses, ainsi que leurs niveaux de CEM. Théoriquement, il n'y a jamais deux composants qui sont les mêmes [CHRI07]. Par ailleurs, la différence des effets du vieillissement est en relation avec la dispersion entre les différents échantillons et le phénomène aléatoire lors de la dégradation de vieillissement [LOMA03].

Donc, pour l'étude de la CEM à long terme, l'évolution du niveau de CEM est non seulement la variation moyenne du niveau d'émission ou d'une immunité, mais aussi l'évolution de la distribution

statistique du niveau de CEM et la probabilité de conformité CEM vis-à-vis d'une limite de CEM donnée (appelé «fiabilité électromagnétique» [WU12]) à chaque phase de vieillissement.

L'objectif de l'analyse statistique dans l'étude de la REM est de déterminer la distribution statistique des niveaux d'émission et d'immunité, puis de calculer l'évolution de la probabilité de la conformité CEM (ou non-conformité) vis-à-vis d'une limite donnée. Dans cette étude, nous commençons par une discussion générale sur l'analyse statistique dans des études de CEM, où plusieurs distributions statistiques de niveau CEM sont présentées (Distribution normal et log-normal). La caractérisation statistique de la dérive de CEM est détaillée dans la partie suivante. Ensuite, les méthodes d'analyse statistique utilisées dans la prévision de la fiabilité électromagnétique sont présentées, où quelques distributions les plus communes utilisées dans les études de fiabilité des composants électroniques sont présentées (distributions exponentiel, log-normal et Weibull). Enfin, une étude de cas de l'analyse statistique, qui est basée sur l'étude de convertisseur abaisseur DC-DC et des composants passifs, est proposée à la fin de ce chapitre, afin de valider la méthode proposée.

Pour l'étude de la CEM, la fiabilité peut être définie comme la probabilité de conformité CEM pendant la durée de vie d'un composant ou d'un système. Comme présenté ci-dessous, le niveau CEM d'un ensemble d'échantillons à chaque phase de vieillissement ne peut être seulement présenté par une valeur unique, mais par une distribution statistique. De même, la fiabilité CEM, même pour les dispositifs frais, devrait être présentée par une probabilité. La fiabilité CEM avec le temps pourrait être exprimée par une fonction de fiabilité R_{EMC} (t) (aussi appelé fonction de survie), qui décrit la probabilité qu'aucune défaillance (liée à la conformité CEM) n'apparaissent après un temps de vieillissement t ($t \geq 0$). Ici, pour simplifier la présentation, l'analyse de fiabilité électromagnétique est discutée à une seule fréquence donnée. Elle pourrait bien entendu être calculée sur un ensemble de fréquence.

Habituellement, la conformité CEM est définie par une limite fixée par une norme ou une exigence client. La limite de niveau d'émission est définie par un seuil maximal pour le niveau d'émission, et la limite de niveau d'immunité est définie par un seuil minimal pour le niveau d'interférence. La probabilité de la conformité CEM au fil du temps $R_{EMC}(t)$ à une fréquence donnée pour l'émission électromagnétique et l'immunité électromagnétique peut être obtenue avec les distributions statistiques du niveau de CEM au temps du vieillissement t, comme expliqué dans Figure VII-6.

Basé sur la fonction de fiabilité $R_{EMC}(t)$, nous pouvons également calculer d'autres paramètres statistiques, comme la densité de probabilité de défaillance, la distribution de probabilité de l'échec, le taux d'échec, et aussi le temps moyen avant défaillance CEM. Le processus de calcul de tous ces paramètres statistiques est détaillé dans Chapitre V.

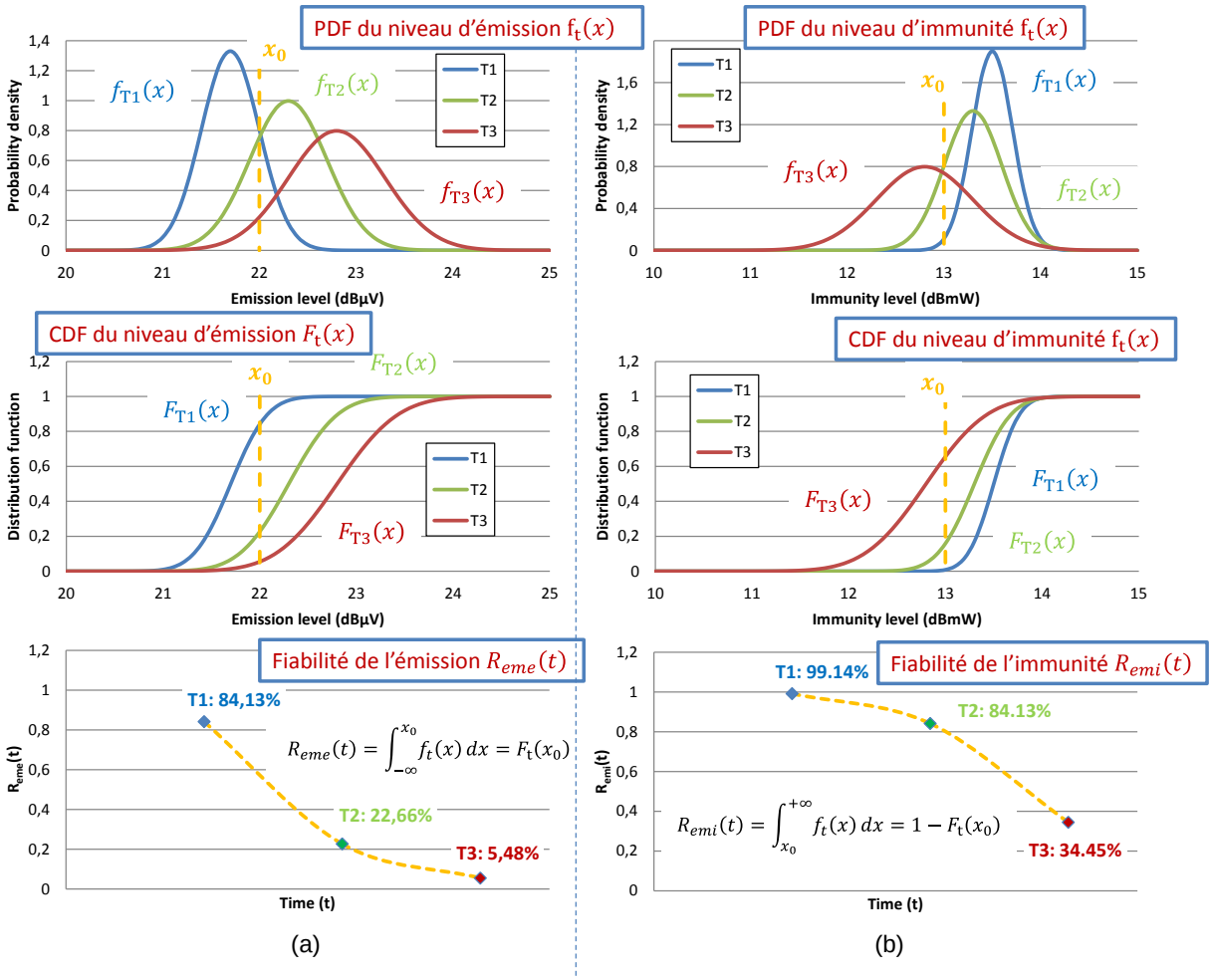

Figure VII-6 Calcul de l'évolution de la fiabilité électromagnétique basée sur la distribution statistique du niveau de CEM au cours du temps (à T1, T2 et T3) et à une fréquence unique donnée: (a) la fiabilité vis-à-vis de l'émission électromagnétique (b) la fiabilité vis-à-vis de l'immunité électromagnétique

Comme présenté ci-dessus, la fiabilité CEM est présentée par la conformité CEM pour un seuil défini. La distribution statistique de la fiabilité EMC peut être extraite par les méthodes basées sur la fonction de distribution de probabilité de défaillance. Cependant, comme les niveaux de CEM sont généralement liés aux comportements des éléments parasites et non-linéaires des circuits, la distribution de la fiabilité CEM peut être très complexe. En outre, pour assurer une bonne précision par cette méthode, un grand nombre d'échantillons et de points de mesure au cours de la durée de vie sont nécessaires, ce qui est très long et a besoin caractérisations reproductibles de la CEM au fil du temps. Par ailleurs, dans le cas de problèmes complexes contenant un grand nombre de variables aléatoires, l'approche analytique automatique par des simulateurs comme la simulation de Monte Carlo sur la base d'un échantillonnage des variable aléatoire est rapidement limitée [RAYC08]. D'autres méthodes d'échantillonnage améliorées ou d'analyses statistiques rapides pourraient être appliqués pour accroître l'efficacité des méthodes de prédiction de la fiabilité électromagnétique.

La distribution de la fiabilité CEM prend en compte à la fois la dispersion liée aux différents échantillons et aussi l'impact de la dégradation induite par le vieillissement. En outre, sa fonction de

distribution peut être une bonne démonstration de l'évolution de la probabilité de défaillance de CEM au fil du temps. Toutefois, tel que présenté ci-dessus, parfois l'extraction de la distribution de la fiabilité CEM est très complexe. En outre, la fiabilité CEM est basée sur une limite CEM fixe, donc pour un même système, la fiabilité CEM devrait être reconstruite si la définition de la limite CEM est modifiée. Par conséquent, la fonction de fiabilité CEM ne suffit pas. Les distributions statistiques détaillées du niveau CEM à différents instant de la durée de vie sont nécessaires pour calculer précisément l'évolution de la conformité CEM avec le temps.

Une étude de cas de l'analyse de la fiabilité CEM d'un convertisseur DC-DC est présentée à la fin du Chapitre V. Les distributions de la REM à chaque phase de vieillissement sont extraites selon les résultats de la mesure et de la simulation, respectivement. Bien qu'il existe encore certaines limites comme le nombre d'échantillons, deux approches d'extraction sont bien détaillées dans cette étude de cas. La distribution de Weibull est utilisée pour modéliser l'évolution de la fiabilité électromagnétique, et les résultats de mesure et de simulation montrent une bonne corrélation. Avec ces méthodes, la probabilité fiabilité vis-à-vis de l'émission électromagnétique du convertisseur DC-DC avec le temps de vieillissement est correctement prédite.

VII.6. Conclusion

Afin d'analyser l'évolution à long terme des niveaux CEM des composants électroniques, l'étude présentée dans cette thèse propose des méthodes prédictives générales pour les niveaux de compatibilité électromagnétique de composants électroniques qui évoluent avec le temps.

Plusieurs propositions originales ont été faites au cours de cette étude:

- Une méthodologie générale pour prédire la variation des niveaux CEM au niveau d'un circuit intégré et au niveau d'un circuit imprimé est proposée, qui consiste en la modélisation conjointe de la CEM et des mécanismes de dégradation des composants électroniques avec le temps. Les études de cas présentées ont validé le flux de modélisation de REM.
- L'analyse statistique est appliquée à l'étude de la REM. La notion de «fiabilité CEM » est présentée, qui montre l'évolution de la probabilité de la conformité CEM.
- Comme une méthode alternative pour protéger la propriété intellectuelle des circuits intégrés, la méthode de modélisation "boîte noire" est intégrée dans l'étude de la REM.
- Les modèles de dégradation de plusieurs composants électroniques typiques sont construits dans cette étude. En particulier, les modèles de dégradation d'une inductance de poudre de fer sont réalisés pour la première fois.

En outre, des améliorations et des perspectives de l'étude de la REM pourront être appliquées dans les travaux futurs:

- En raison de la limite de temps, les méthodes de modélisation proposées ne sont appliquées que sur deux études de cas. En outre, le type et le nombre des échantillons testés sont également limitées. Plus d'échantillons sont nécessaires à l'avenir pour vérifier et améliorer les modèles proposés.
- La construction de bibliothèques de modèles de la dégradation des composants (les composants actifs et passifs) dans différentes conditions de fonctionnement/de stress pourrait être une source très utile pour l'étude future de la modélisation de la REM. En conséquence, les autres études sur les mécanismes de dégradation de composants électroniques sont nécessaires pour extraire de nouveaux modèles de dégradation. De plus, dans cette étude, l'influence de la température n'est pas prise en compte dans le modèle de composants électroniques, alors qu'elle peut influencer l'émission et l'immunité électromagnétique. Celle-ci devrait être étudiée dans les travaux futurs.
- Certaines autres notions statistiques comme les indices de confiance, le nombre d'échantillons, et plusieurs distributions statistiques pourraient être appliquées dans l'étude de fiabilité CEM. Puis, plus d'études de cas de la fiabilité CEM sont nécessaires pour rendre l'analyse de fiabilité CEM plus systématique.

L'étude REM est un domaine de de recherche commun à la "fiabilité" et à la "CEM". Ainsi d'autres améliorations des méthodes de caractérisation et de modélisation dans ces deux domaines pourraient être utiles pour la future étude de la prédiction du niveau CEM avec le temps.

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Glossary

ADM	Amplitude Difference Measure
ADS	Advanced Designed System
ANN	Artificial Neural Network
ARE	Average Relative Error
BCI	Bulk Current Injection
BERT	Berkeley Reliability Tools
BTI	Bias Temperature Instability
CDF	Cumulative Distribution Function
CE	Conducted Emission
CHE	Channel Hot Electron
CI	Conducted Immunity
CISPR	International Special Committee on Radio Interference
CMRR	Common-Mode Rejection Ratio
DAHC	Drain Avalanche Hot Carrie
DEW	Directed Energy Weapon
DI	Disturbance Input
DO	Disturbance Output
DPI	Direct Power Injection
EDA	Electronic Design Automation
EFT	Electrical Fast Transient
ELR	Extrapolation of the Linear Region

EM	Electromagnetic
EMC	Electromagnetic Compatibility
EME	Electromagnetic Emission
EMI	Electromagnetic Immunity
EMR	Electromagnetic Robustness
EMRIC	Electromagnetic Robustness Of Integrated Circuits
EMS	Electromagnetic Susceptibility
EOS	Electrical Overstress
ESD	Electrostatic Discharge
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistor
ET	External Terminal
FCC	Federal Communications Commission
FDD	Frequency-Domain Defined Device
FDM	Feature Difference Measure
FFT	Fast Fourier Transform
FIT	Failures In Time
FROM	First-Order Reliability Method
FSV	Feature Selective Validation
GDM	Global Difference Measure
HCI	Hot Carrier Injection
HDB	Hard Breakdown
HISES	High Speed EMI Simulator
HISREM	Hot Carrier Induced Series Resistance Enhancement Model
HTB	High Temperature With Bias
HTOL	High Temperature Operating Life

HTS	High Temperature Storage
I/O	Input/Output
IA	Internal Activity
IB	Internal Behavior
IBC	Inter-Block Coupling
IBIS	I/O Buffer Information Specification
IC	Integrated Circuit
ICEM	Integrated Circuit Emission Model
ICIM	Integrated Circuit Immunity Model
IEC	International Electrotechnical Commission
IMIC	Interface Model for Integrated Circuits
IP	Intellectual Property
IS	Importance Sampling
IT	Internal Terminal
ITU	International Telecommunications Union
LAR	Least Absolute Residuals
LC	Leakage Current
LECCS	Linear Equivalent Circuit and Current Source
LIHA	Local Injection Horn Antenna
LTOL	Low Temperature Operating Life
MLCC	Multilayer Ceramic Capacitors
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MRE	Maximum Relative Error
MSC	Mode Stirred Chamber
MTBF	Mean Time Between Failures
MTTF	Mean Time To Failure

NBTI	Negative-Bias Temperature Instability
NN	Neural Network
OO	Observable Output
opamp	Operational Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PDF	Probability Density Function
PDN	Passive Distribution Network
PHM	Prognostics and Health Management
PLL	Phase Locked Loop
PWL	Piecewise Linear
RE	Radiated Emission
RF	Radio Frequency
RFIP	RF Injection Probe
RI	Radiated Immunity
RLC	Resistances, Inductances and Capacitances
RMSE	Root-Mean-Square Error
RSSE	Root Relative Square Error
SBD	Soft Breakdown
SE	Shielding Effectiveness
SGHE	Secondary Generated Hot Electron
SHE	Substrate Hot Electron
SIL	Safety Integrity Level
SMD	Surface-Mount Device
SMPS	Switching-Mode Power Supply
SNA	Scalar Network Analyzer

SPICE	Simulation Program with Integrated Circuit Emphasis
SR	Slew Rate
SR-	Negative Slew Rate
SR+	Positive Slew Rate
SRF	Self-Resonant Frequency
SROM	Second-Order Reliability Method
SS	Subset Simulation
SSN	Simultaneous Switching Noise
T/C	Temperature Cycling
TDDB	Time-Dependent Gate Oxide Breakdown
UTE	Union Technique de l'Electricité
VNA	Vector Network Analyzer
WBFC	Workbench Faraday Cage

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