

Packaging for Power Electronics

“Habilitation à Diriger des Recherches”

Cyril BUTTAY

Laboratoire Ampère, Lyon, France

2015

Outline

Professional Record

Background

Contributions

Perspectives

Conclusion

Professional Record

Background

Contributions

- Packaging for High Temperatures

- New Packaging Structures for Power Modules

Perspectives

- New Packaging Structures for Power Modules

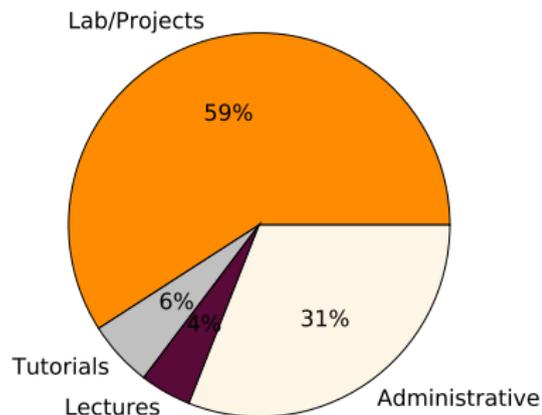
- Packaging for High Temperature

- Packaging for High Voltages

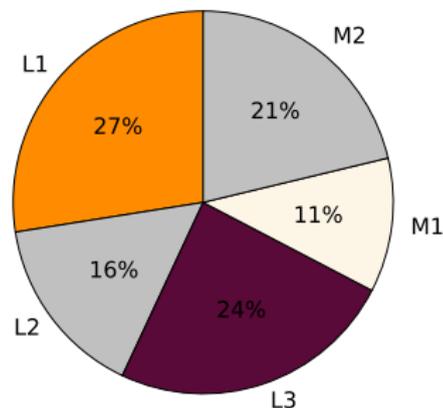
Conclusion

- 1996 – 2001: Electrical Engineer training (INSA Lyon)
 - 2001 – 2004: PhD thesis (CIFRE grant with Valeo) at CEGELY
 - 2004 – 2005: Teaching assistant (ATER at INSA Lyon), LGEF
 - 2005 – 2007: Research Associate with Sheffield and Nottingham Universities
 - 2008 – . . . : Researcher (*Chargé de recherche*) with CNRS.
- ➔ From pure Electrical Engineering to Packaging

Type of classes

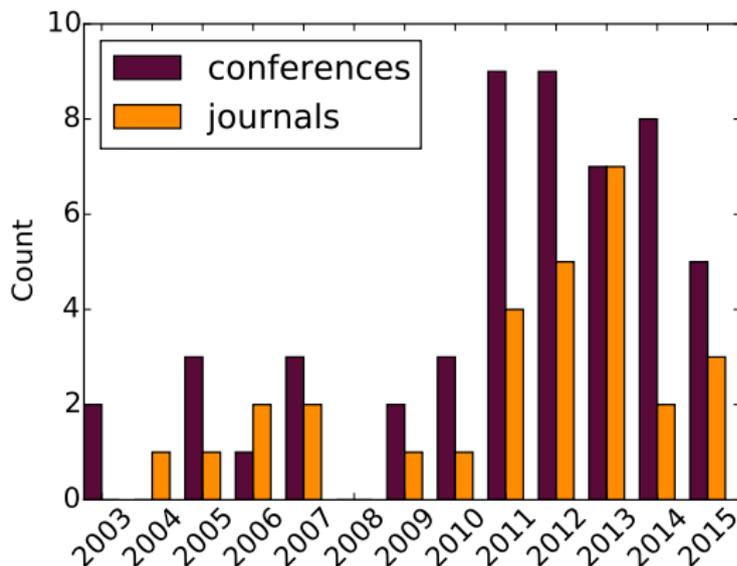


Student Level (Licence/Bachelor or Master)



Total 2001–2015: 645 h

Publications



- ▶ Journals:

- ▶ 9 IEEE

- ▶ 6 Elsevier

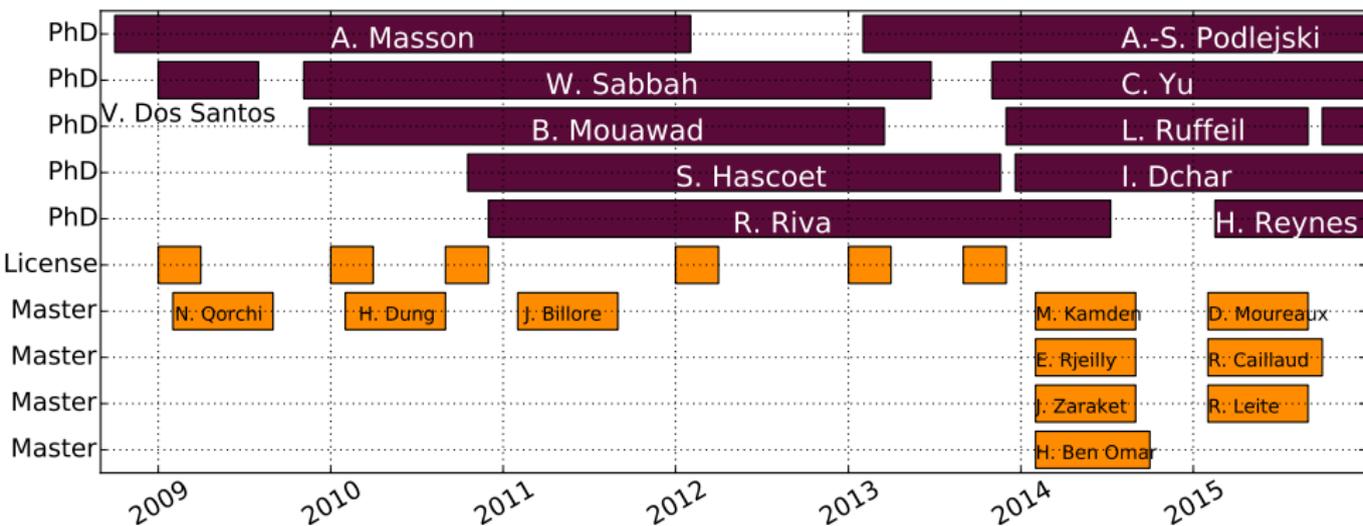
- ▶ 2 invited conferences

- ▶ 2008: Starting with CNRS

- ▶ 2013-2014: HDR writing-up

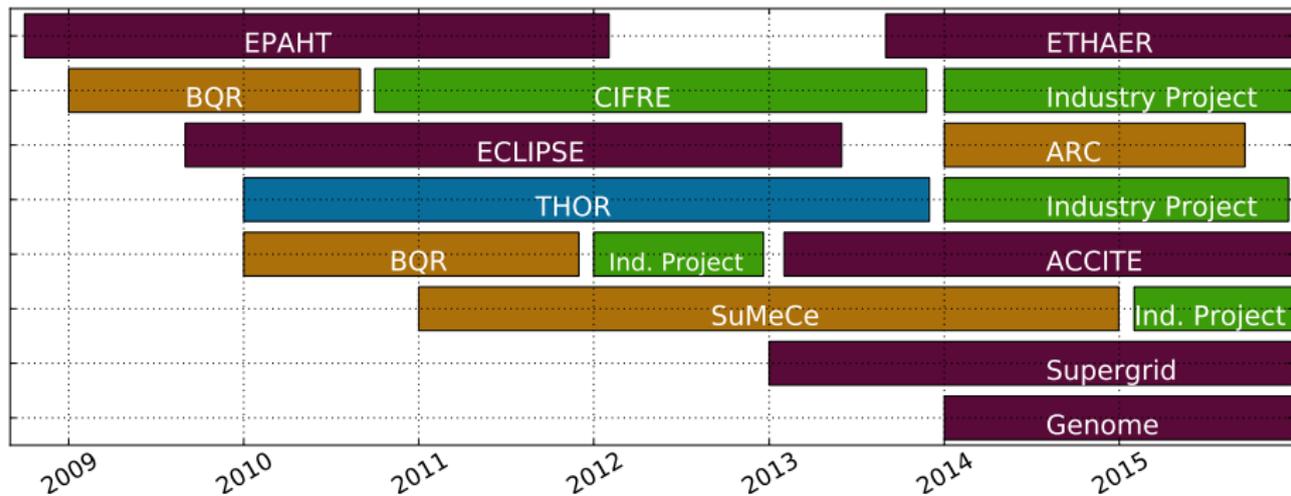
	WOS	Google
Citations	182	610
h-index	6	12

Supervision



- ▶ Shared supervision, various degrees
- ▶ Funded by the industry or by research projects
- ▶ Increase in Master's projects

Research Projects



- ▶ Some projects with lower involvement not mentioned
- ▶ Various funding schemes:
 - ▶ **European:** Euripides-Catrene (THOR)
 - ▶ **National:** Agency for Research (ETHAER, ECLIPSE), Aerospace and Space –FNRAE– (EPAHT, ACCITE)
 - ▶ **Local fundings:** BQR, Carnot institute (SuMeCe)
 - ▶ Direct funding by the **industry** (5 companies)

- ▶ In the lab
 - ▶ Member of the laboratory board
 - ▶ Installation and management of shared equipment:
 - ▶ Packaging lab ($\approx 300\text{k€}$)
 - ▶ Computer cluster (2009–2014)
- ▶ In the research community
 - ▶ Reviewer for journals/conferences (20-30 publications/year)
 - ▶ Reviewer for projects proposals (Cleansky, 7 days)
 - ▶ Member of 3 selection panels (hiring of lecturers)
 - ▶ Member of PhD juries (10)
 - ▶ Member of an evaluation committee (LN2, Sherbrooke)
 - ▶ Management of the “3DPHI” platform on power integration (Toulouse) with 2 colleagues.

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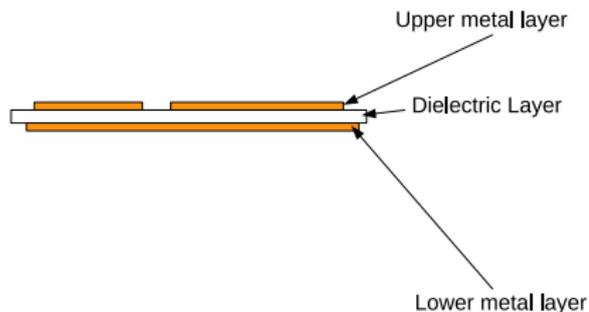
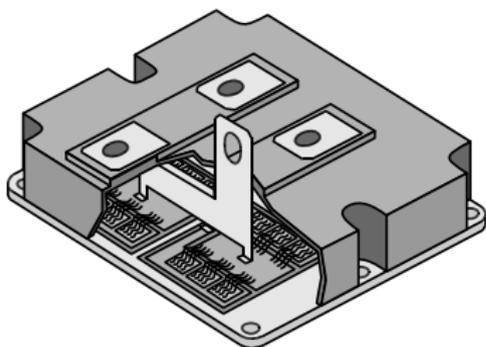
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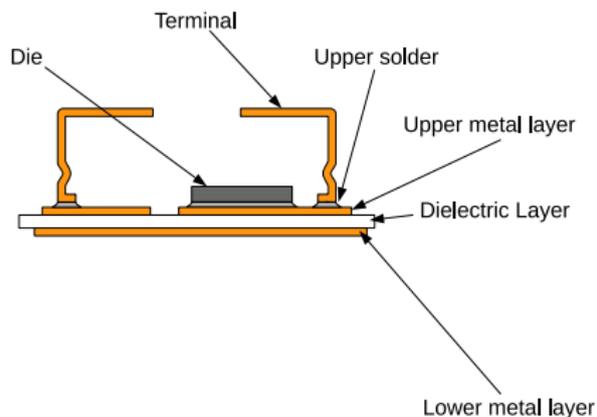
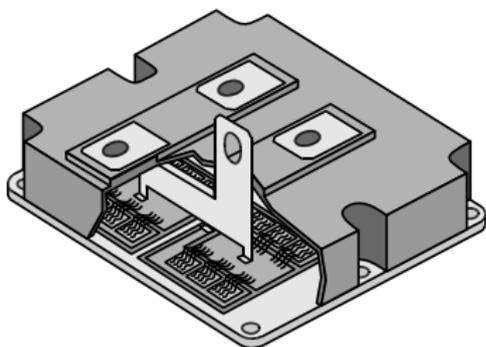
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The Power Module



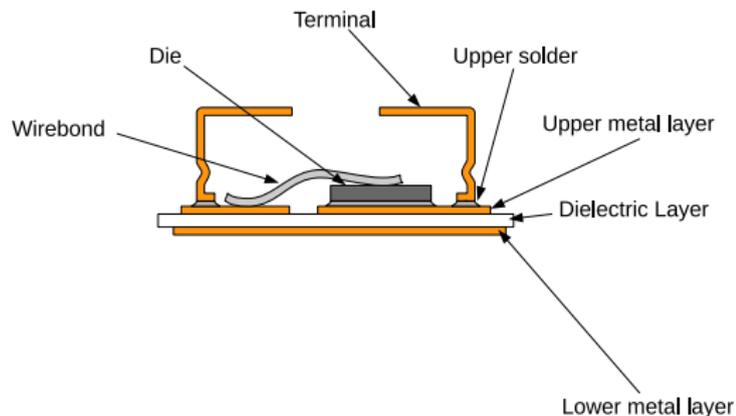
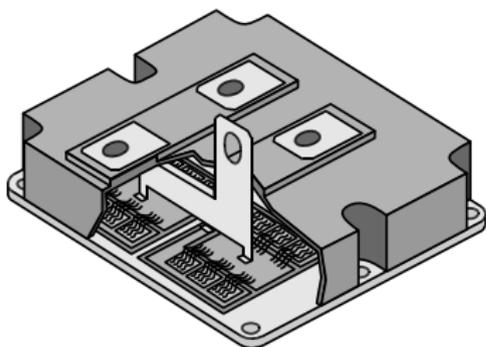
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 - ▶ Thermal management
 - ▶ Electrical insulation
 - ▶ Interconnects
 - ▶ Mechanical/chemical protection
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 - ▶ Ceramics
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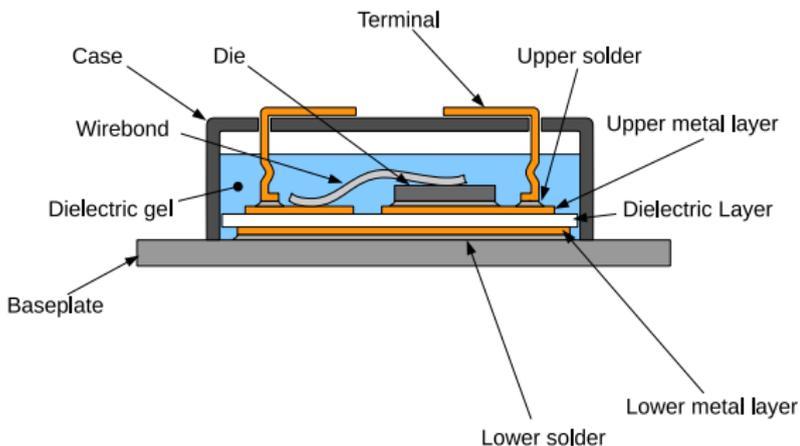
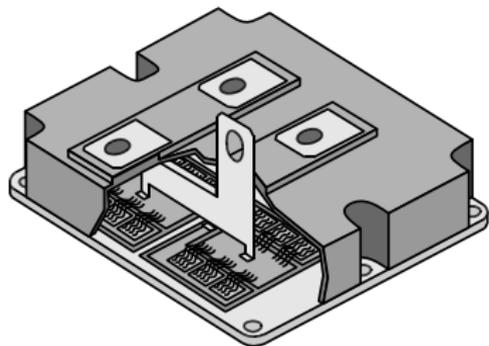
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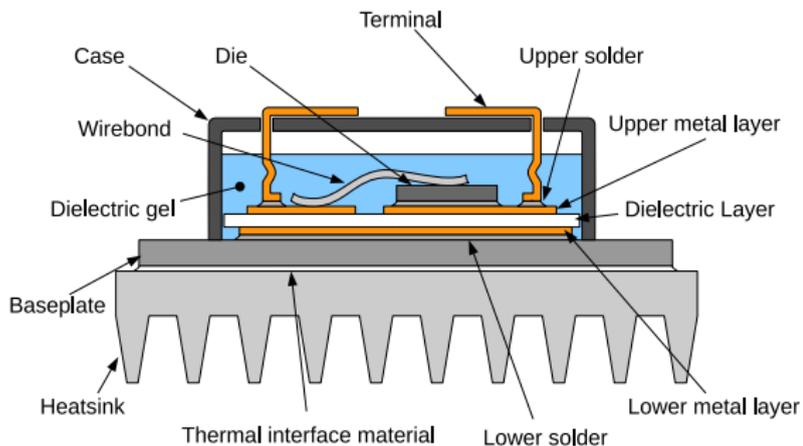
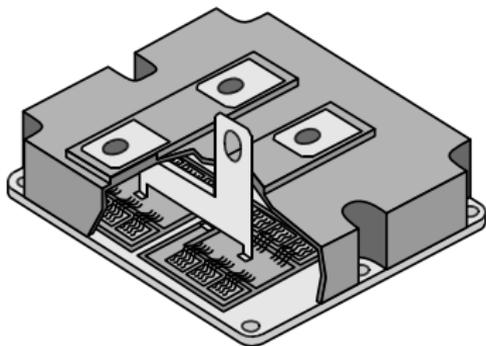
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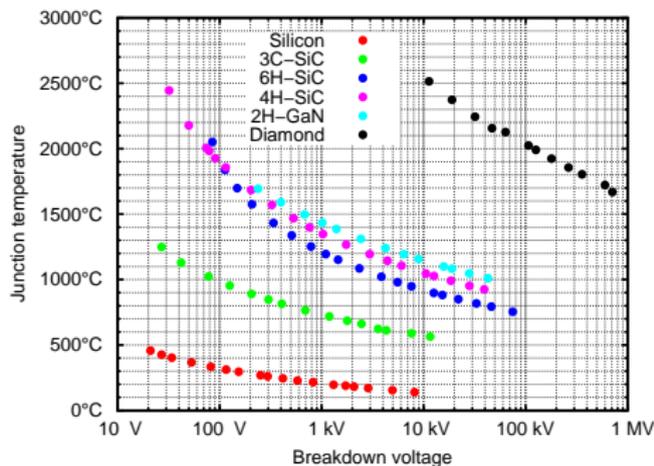
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Operating Temperature Limits



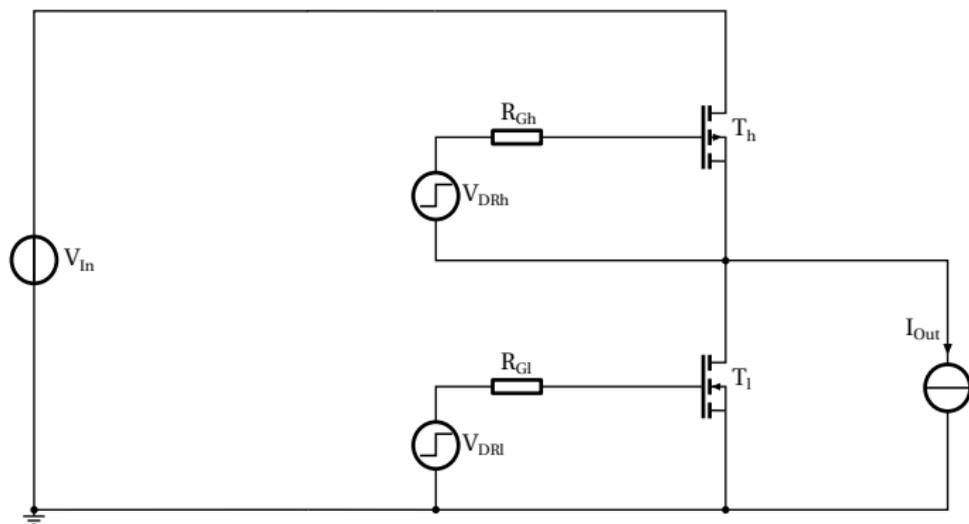
Some limits:

- 660 °C Aluminium melts
- ≈ 300 °C Die Solder melts
- 200 – 250 °C Silicone gel degrades
- ≈ 200 °C Board solder melts

Source: C. Raynaud et al. "Comparison of high voltage and high temperature performances of wide bandgap semiconductors for vertical power devices" *Diamond and Related Materials*, 2010, 19, 1-6

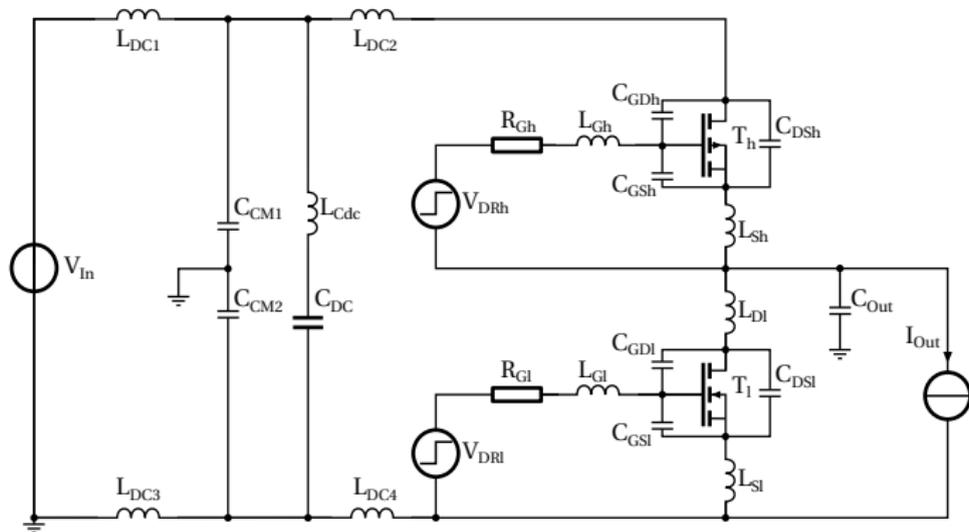
- ▶ **For Wide-Bandgap devices, limits set by packaging**
- ▶ Additional packaging issues with thermal cycling

Effect of the Packaging on Electrical Performance



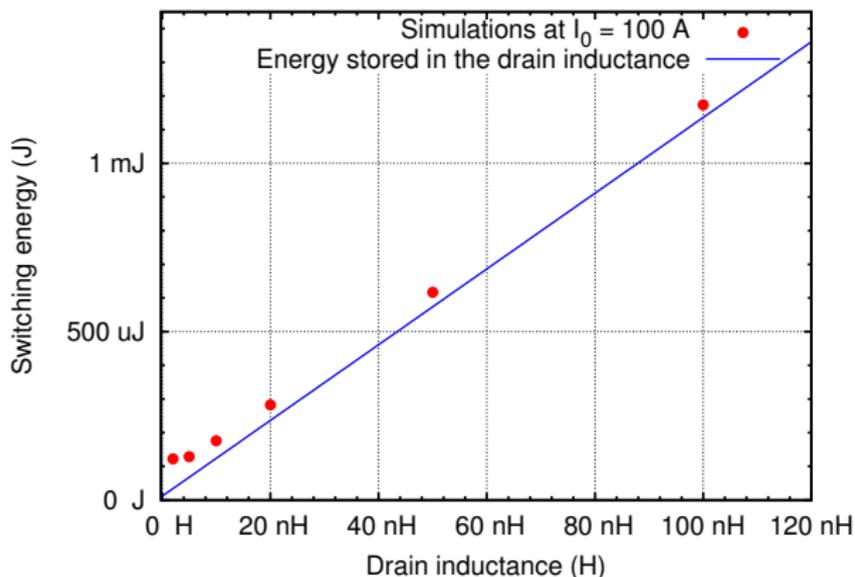
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- ▶ Parasitic capacitances cause common-mode current
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- ▶ Both are **caused by packaging**

Effect of the Packaging on Electrical Performance – 2



- ▶ Low voltage switching cell (30 V Si MOSFETs) simulations
- ▶ Most of the losses can be attributed to circuit layout
- ▶ Here all stray inductances 1 nH, except L_D

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- ▶ Actuators and electronics close to the jet engine
- ▶ Deep thermal cycling ($-55/+225\text{ }^{\circ}\text{C}$)
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- ▶ Mission to Jupiter: 100 bars, $400\text{ }^{\circ}\text{C}$

Applications of High Temperature Electronics



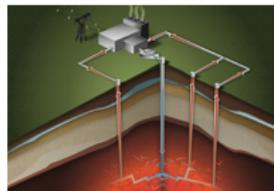
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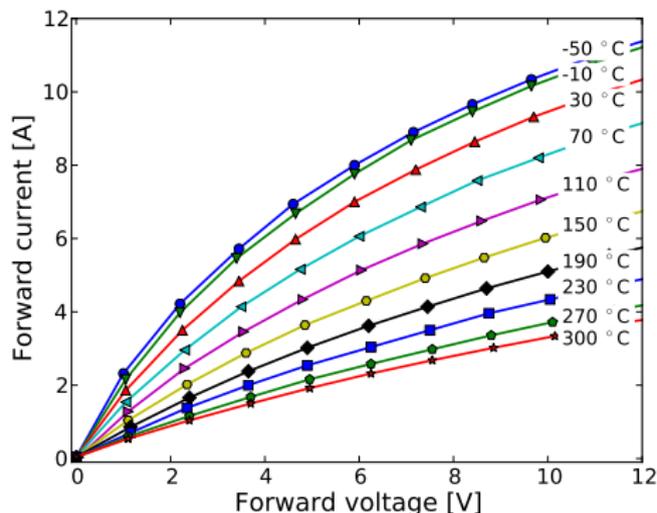
- ▶ NASA mission to Venus: up to $480\text{ }^{\circ}\text{C}$
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- ▶ Oil, gas and geothermal drilling
- ▶ Low thermal cycling, high ambient temp. ($200\text{ to }>300\text{ }^{\circ}\text{C}$)

High temperature behaviour of SiC devices

Static Characterization of 490 mΩ JFET

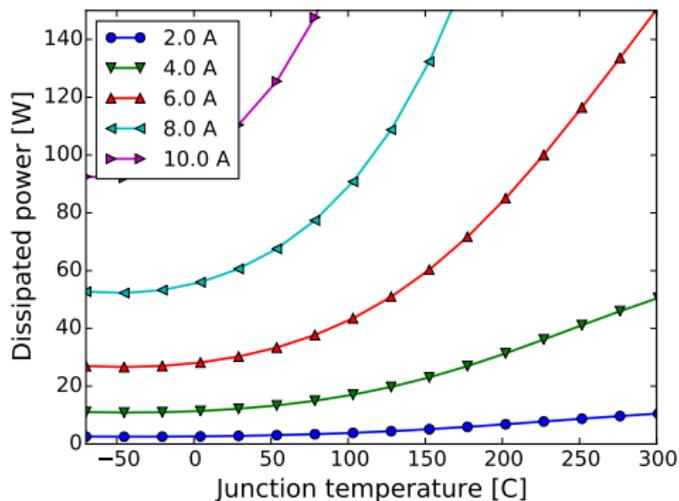
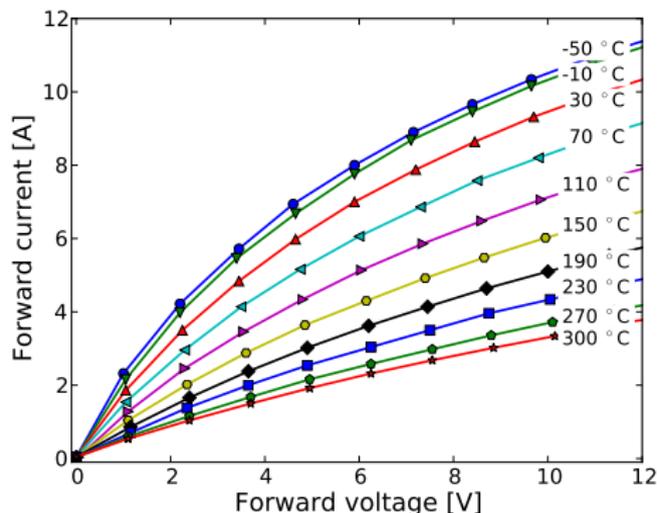


$V_{GS} = 0 \text{ V}$, i.e. device fully-on

- ▶ Large increase in on-state resistance with temperature;
- ▶ Strong sensitivity of conduction losses to temperature.

High temperature behaviour of SiC devices

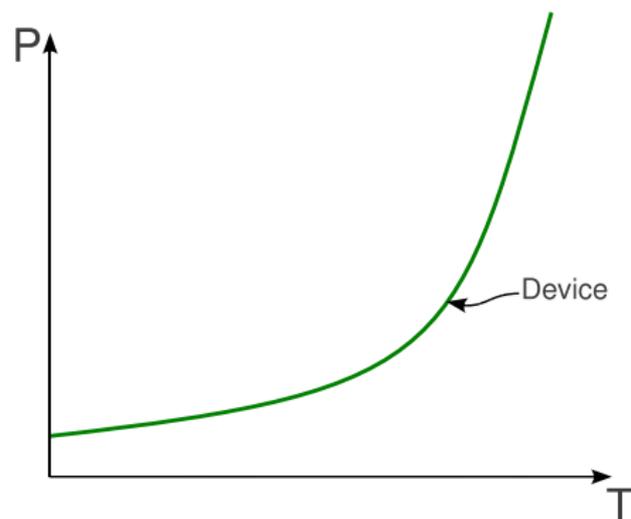
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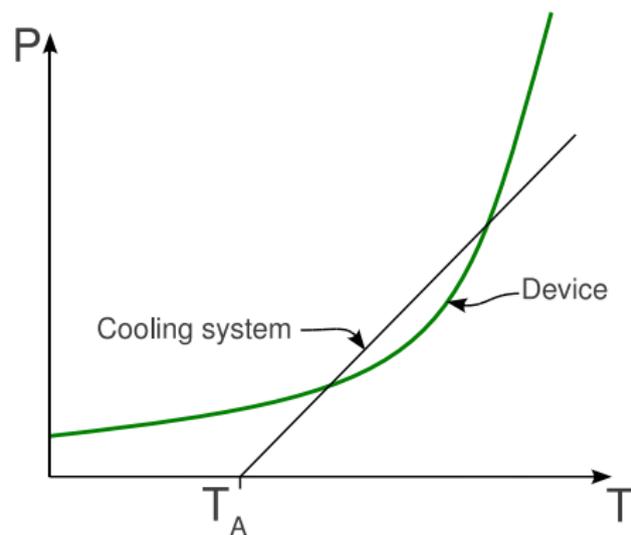
High temperature behaviour of SiC devices



Thermal Run-away mechanism

- ▶ The device characteristic
- ▶ Its associated cooling system
- ▶ Two equilibrium points: one stable and one unstable
- ▶ Above the unstable point, run-away occurs

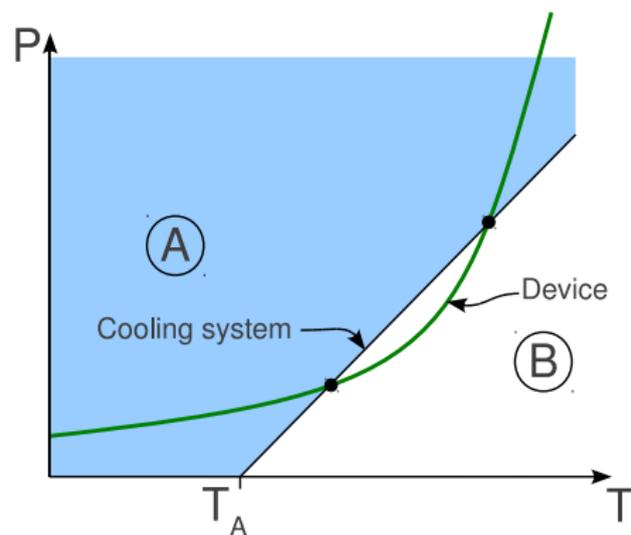
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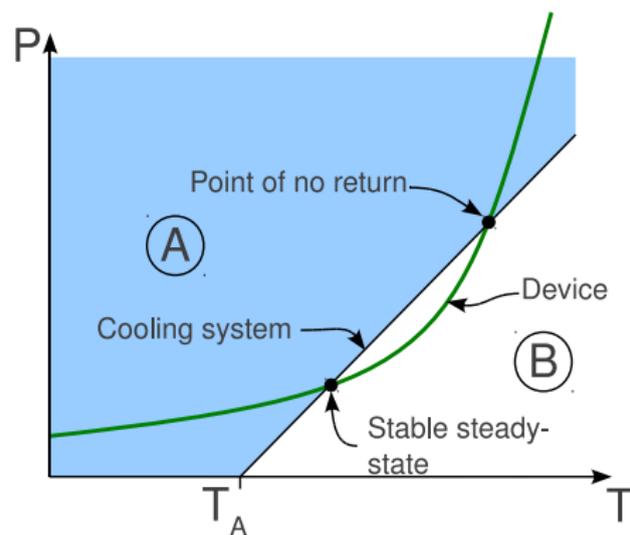
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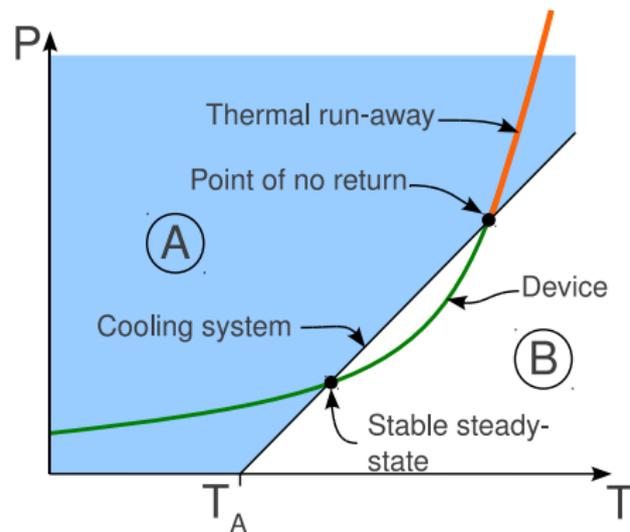
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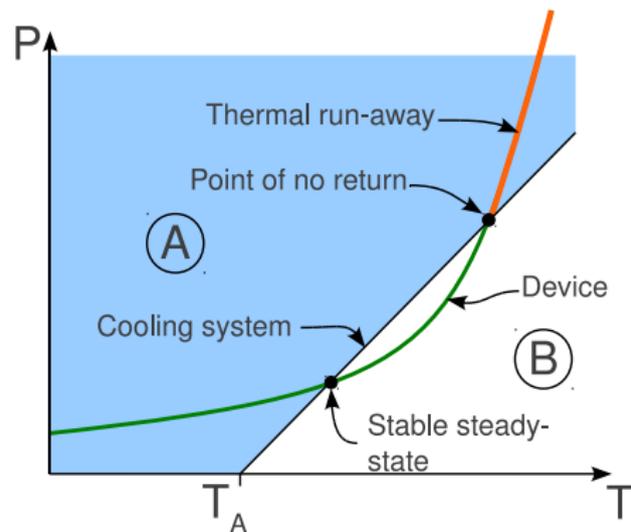
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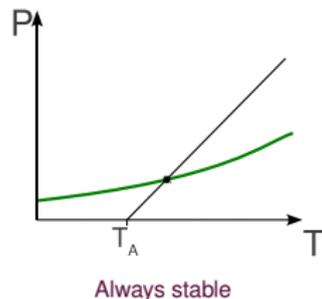
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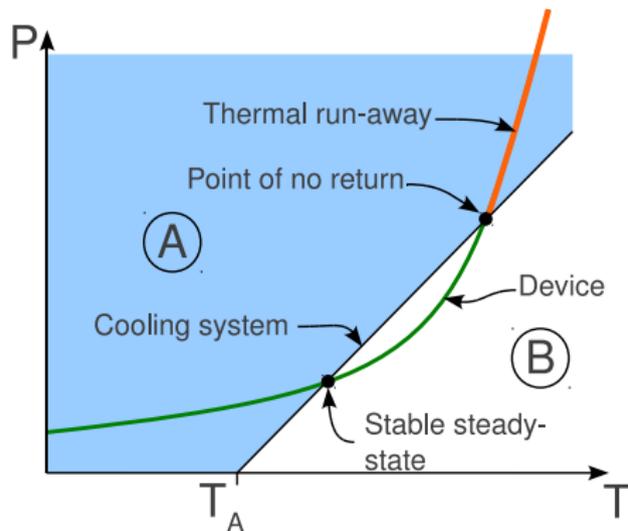


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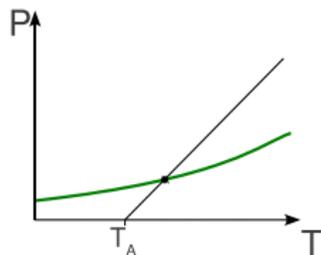


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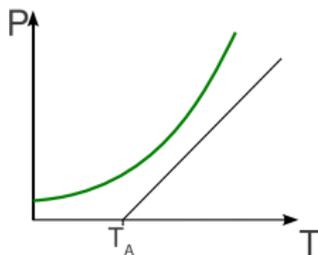


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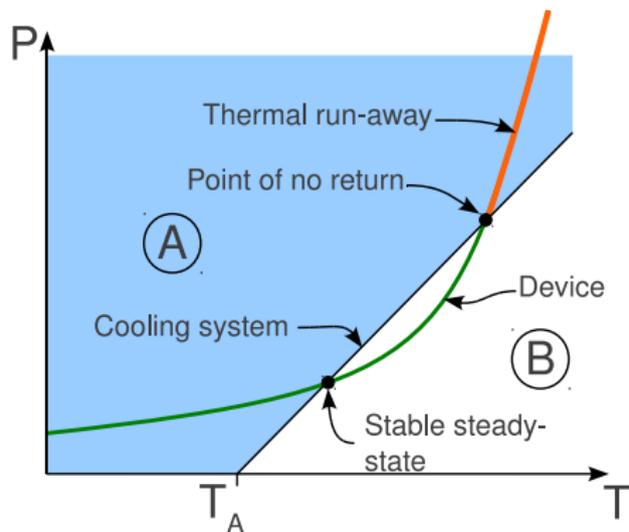


Always stable



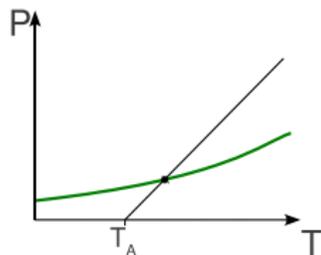
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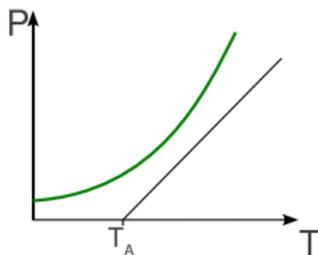


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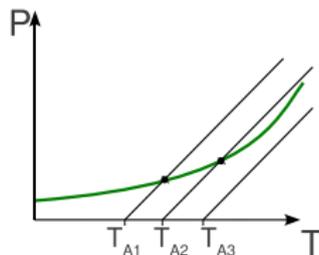
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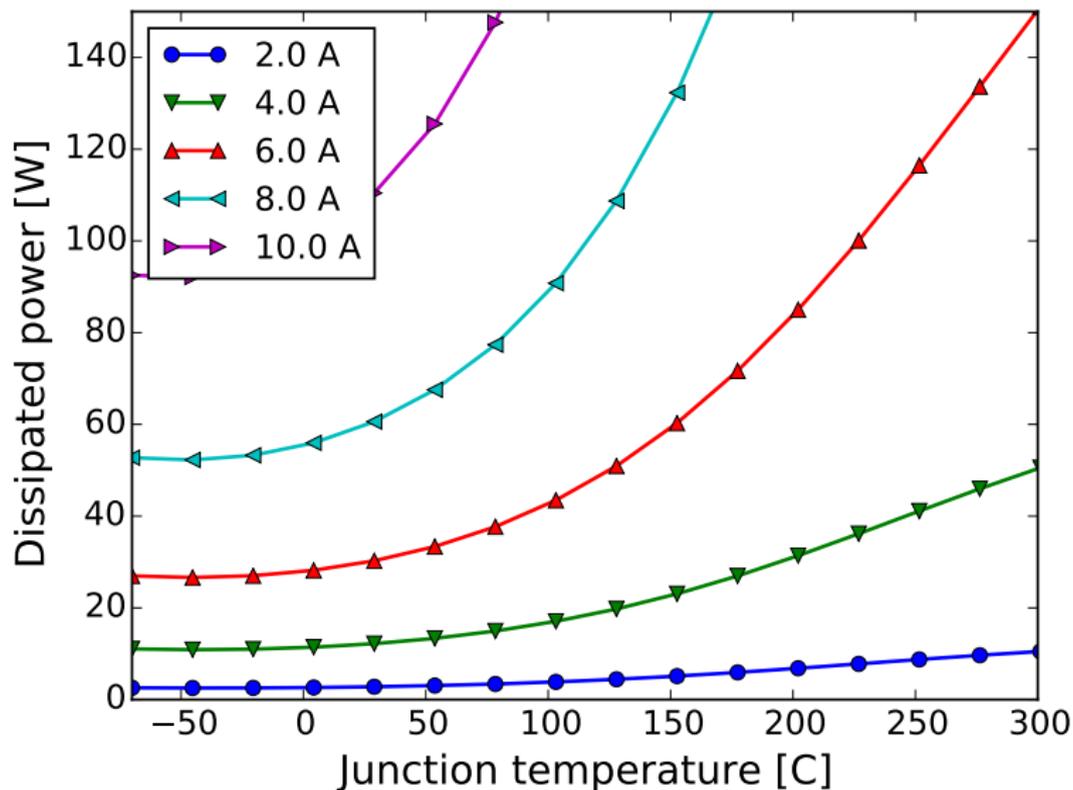


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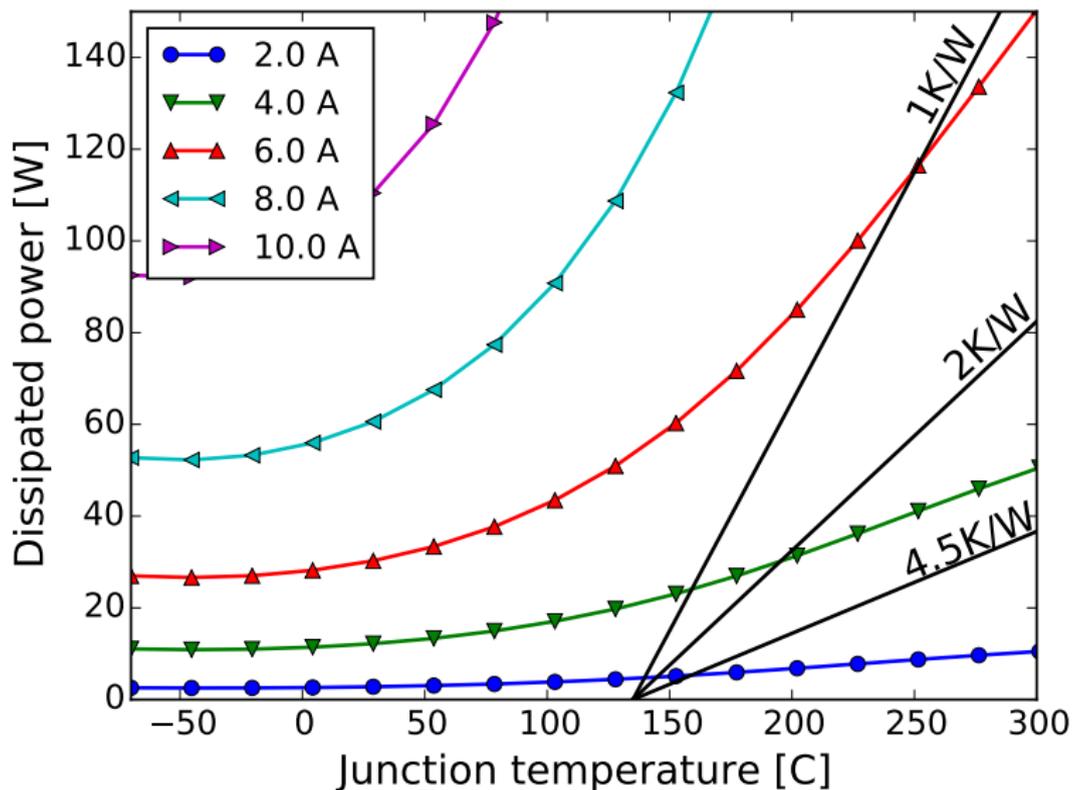


Becoming unstable with ambient temperature rise

Power dissipation as a function of the junction temp.

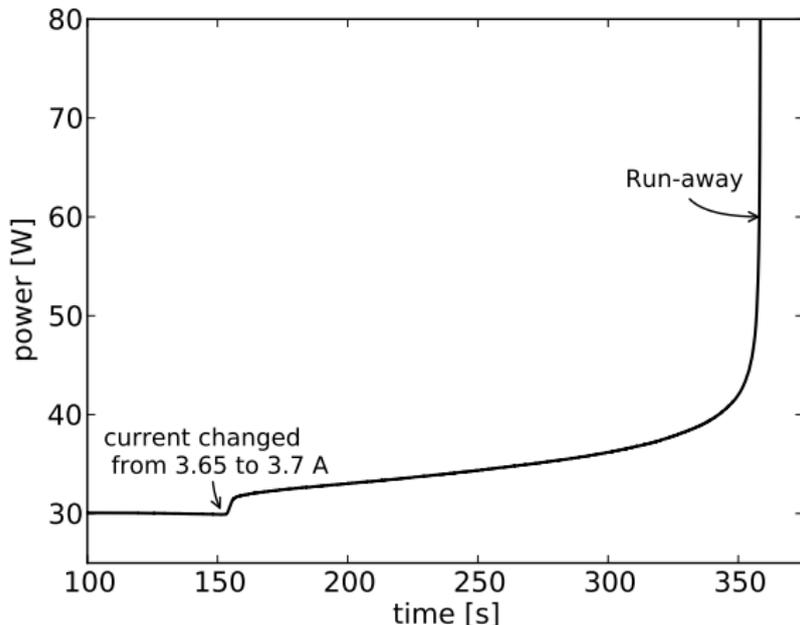


Power dissipation as a function of the junction temp.



High Temperature Thermal Management

Buttay et al. "Thermal Stability of Silicon Carbide Power JFETs", IEEE Trans on Electron Devices, 2014



SiC JFET:

- ▶ 490 m Ω , 1200 V
- ▶ $R_{ThJA} = 4.5 K/W$
- ▶ 135 °C ambient
- ▶ On-state losses

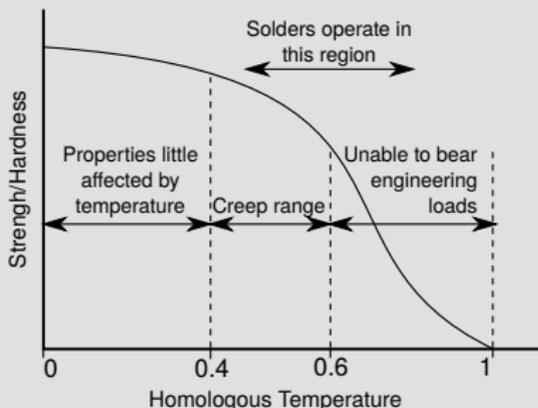
High temperature capability \neq reduced cooling needs!

SiC JFETs must be attached to a low- R_{Th} cooling system.



High Temperature die attaches

The problem with solders



Source:
http://www.ami.ac.uk/courses/topics/0164_homt/

Homologous temperature:

$$T_H = \frac{T_{Oper}[K]}{T_{Melt}[K]}$$

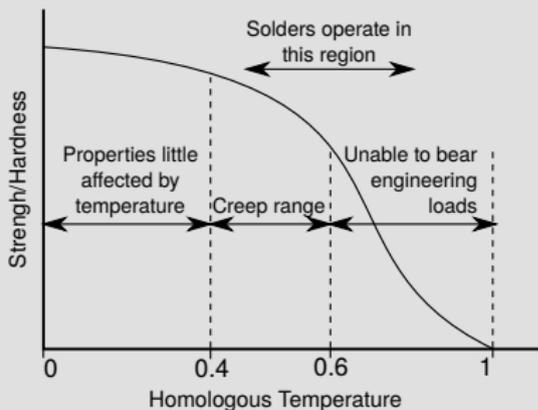
Example:

- ▶ AuGe solder: $T_{Melt} = 356^\circ\text{C} = 629\text{ K}$
- ▶ $T_H = 0.8 \rightarrow T_{Oper} = 503\text{ K} = 230^\circ\text{C}$

- ▶ High temperature solder alloys not practical
- ▶ Need to decouple process temperature and melting point:
 - ▶ Sintering (solid state, process below melting point)
 - ▶ Diffusion soldering/TLFB (creation of a high melting point alloy)

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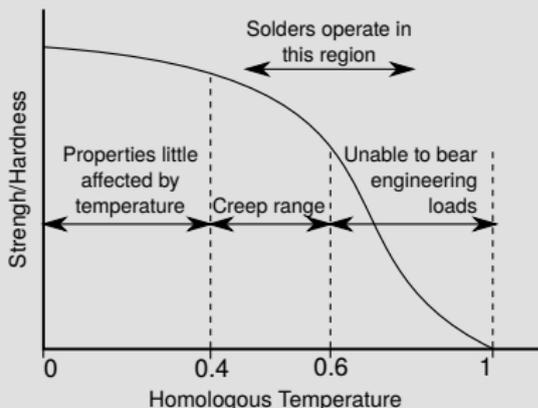
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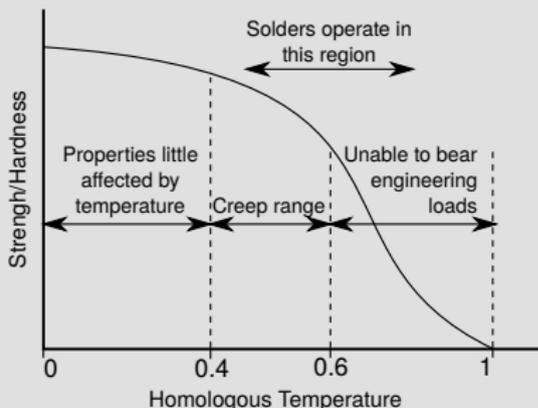
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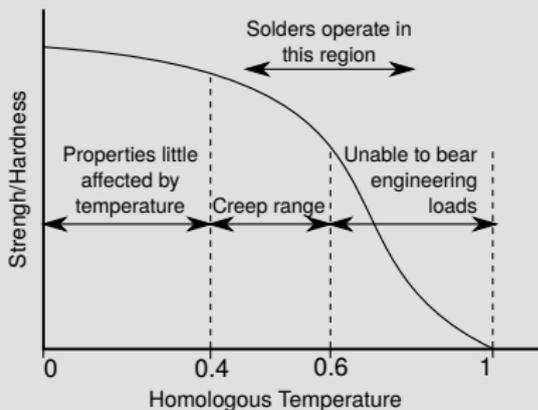
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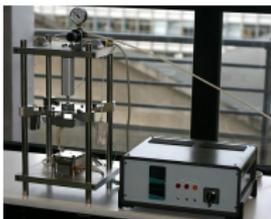
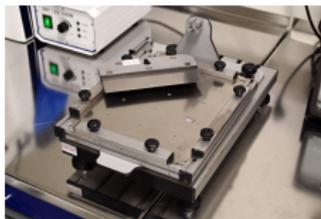
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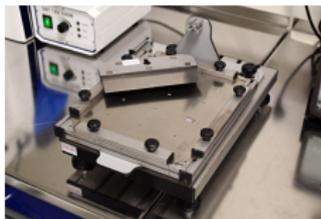
High Temperature Die Attaches — PhD A. MASSON



- ▶ development of the sintering process
- ▶ Nano-particles paste from NBE Tech

- ▶ Evaluation of many parameters
 - ▶ Sintering pressure
 - ▶ Surface roughness
 - ▶ Thickness of stencil
 - ▶ Substrate finish...
- ▶ **Once set, process is robust**

High Temperature Die Attaches — PhD A. MASSON

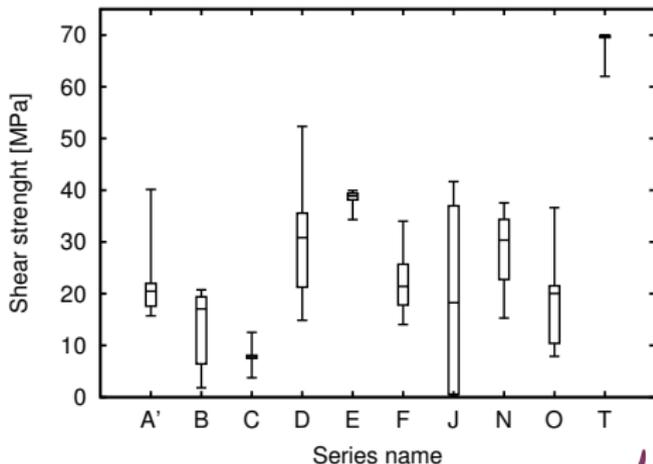


- ▶ development of the sintering process
- ▶ Nano-particles paste from NBE Tech

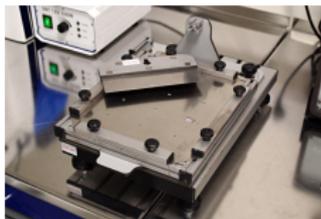
▶ Evaluation of many parameters

- ▶ Sintering pressure
- ▶ Surface roughness
- ▶ Thickness of stencil
- ▶ Substrate finish. . .

▶ Once set, process is robust

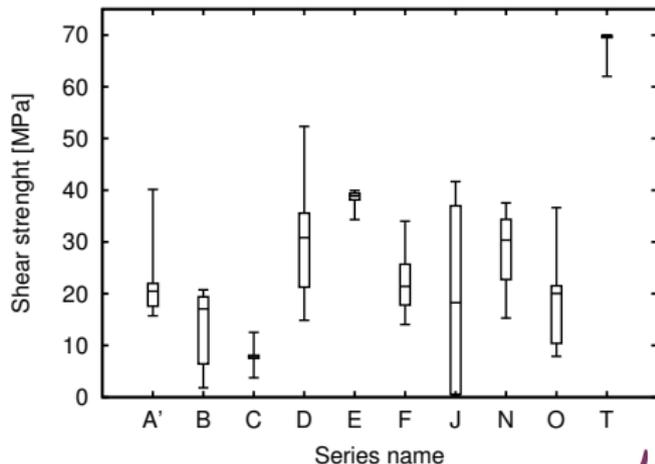
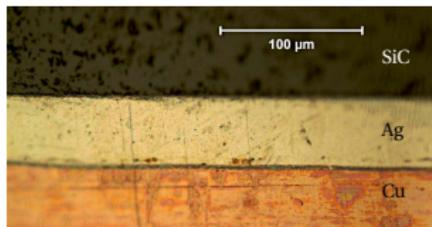


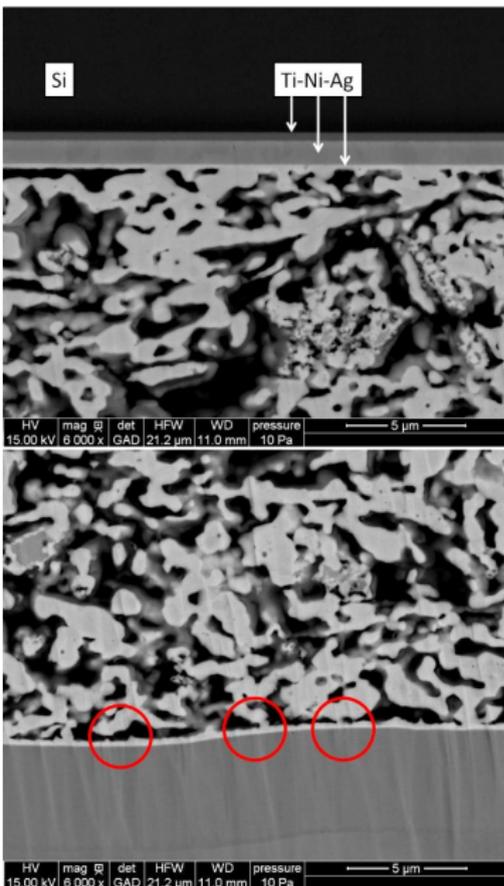
High Temperature Die Attaches — PhD A. MASSON



- ▶ development of the sintering process
- ▶ Nano-particles paste from NBE Tech

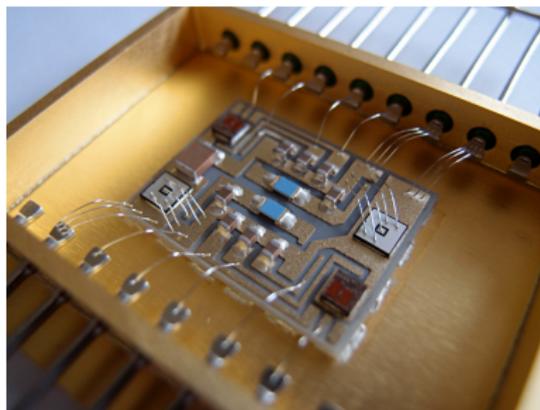
- ▶ Evaluation of many parameters
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- ▶ **Once set, process is robust**



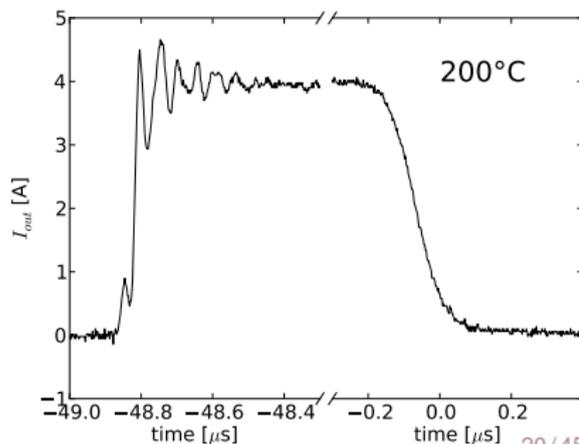
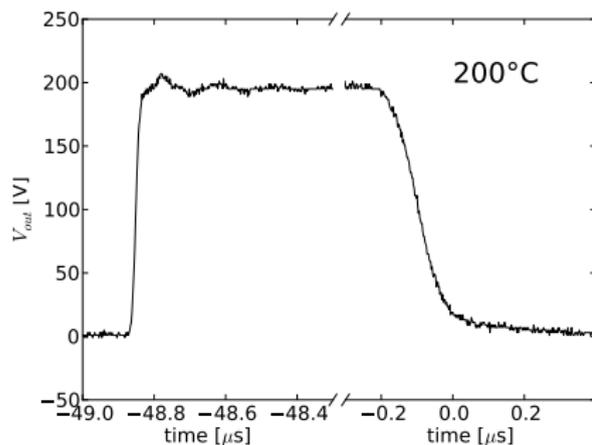


- ▶ “Pressureless” sintering process
- ▶ Based on micro-particles
- ▶ Findings:
 - ▶ Oxygen is necessary
 - ▶ Bonding on copper (oxide)
 - ▶ Standard Ni/Au finish not ideal
 - ▶ Confirmed by several teams
 - ▶ weak bonds at Ag/Au interface
 - ▶ Bond strength lower
 - ▶ Porosity higher
 - ▶ Can be used to attach fragile components

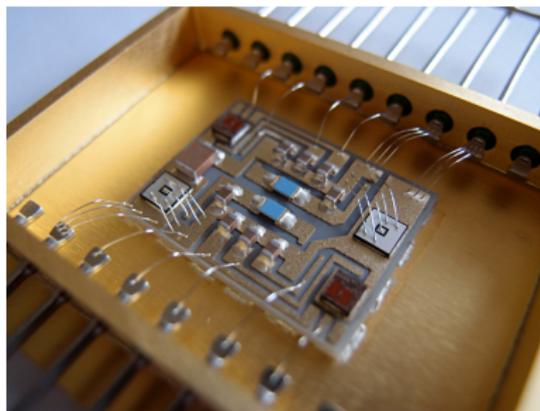
High Temperature Die Attaches



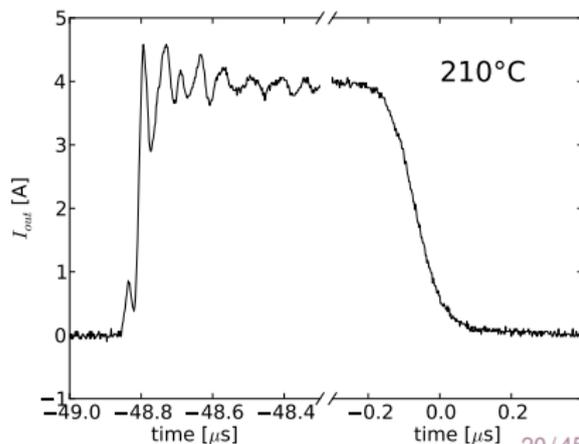
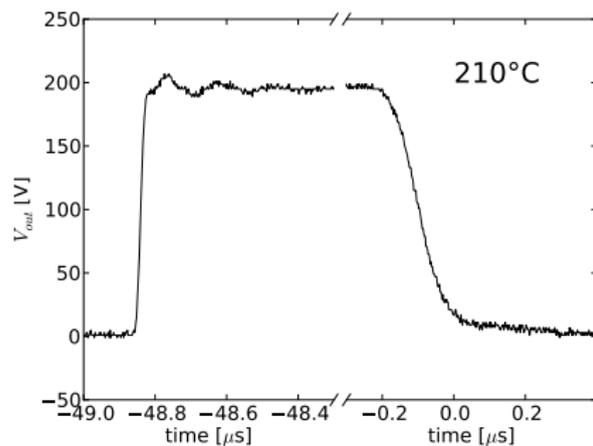
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- ▶ Integrated gate drivers (Ampère)
- ▶ Ceramic capacitors
- ▶ Isolation function not integrated



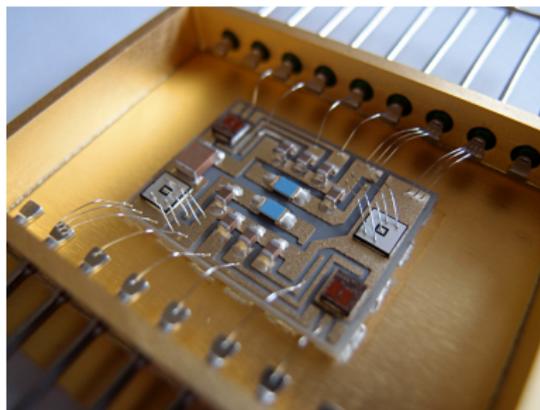
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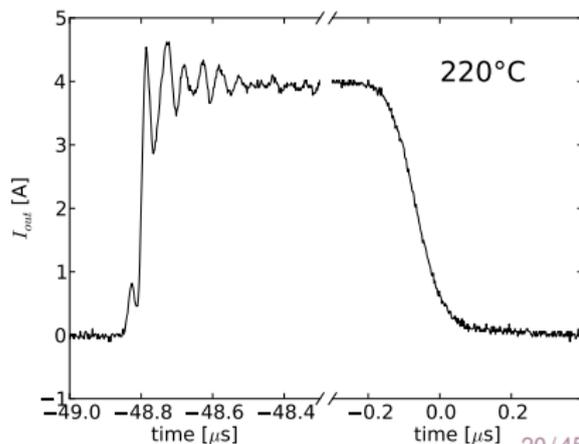
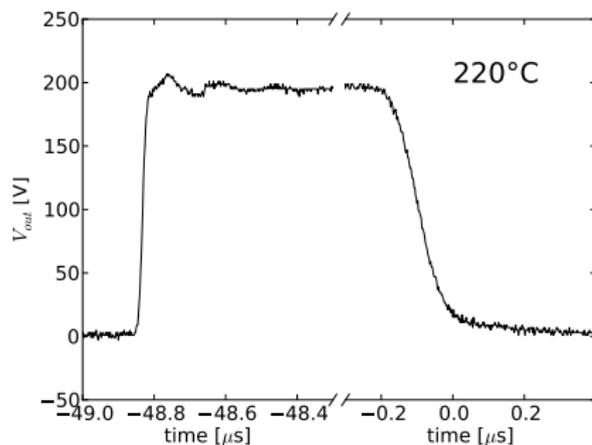
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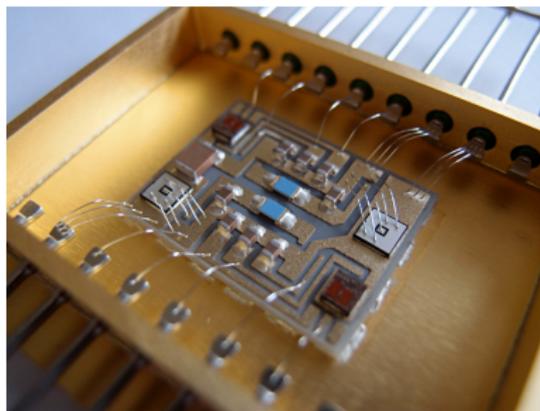
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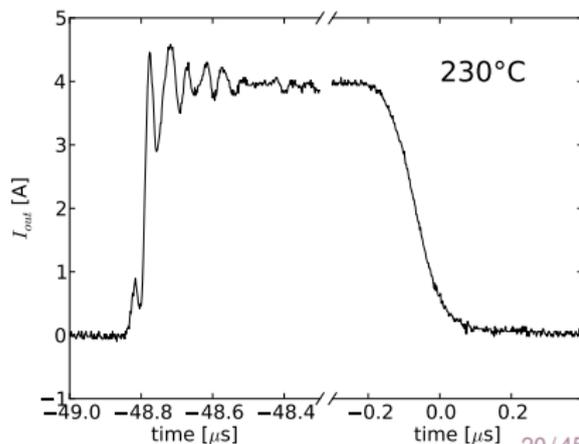
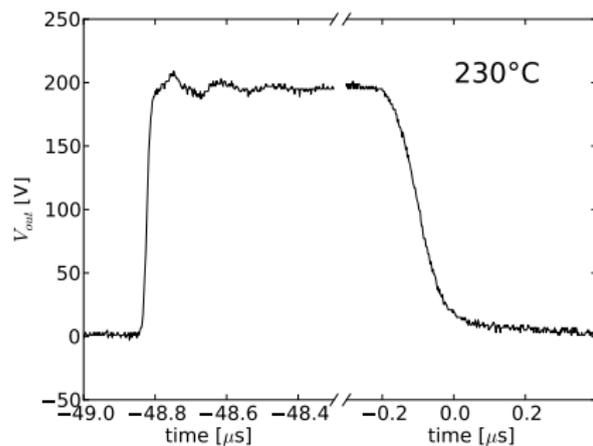
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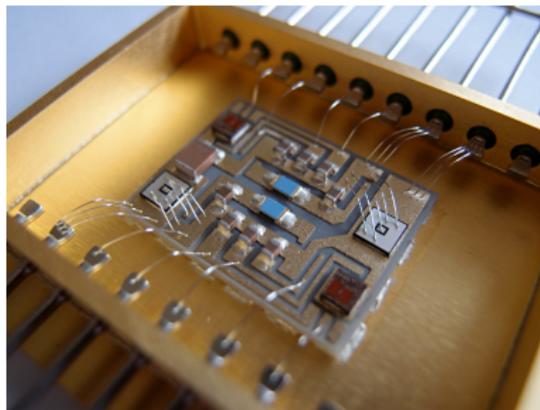
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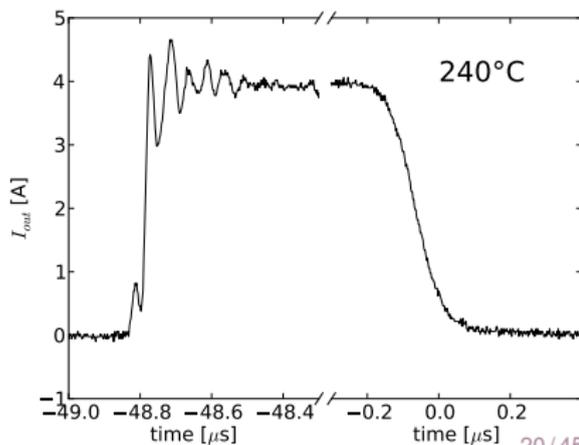
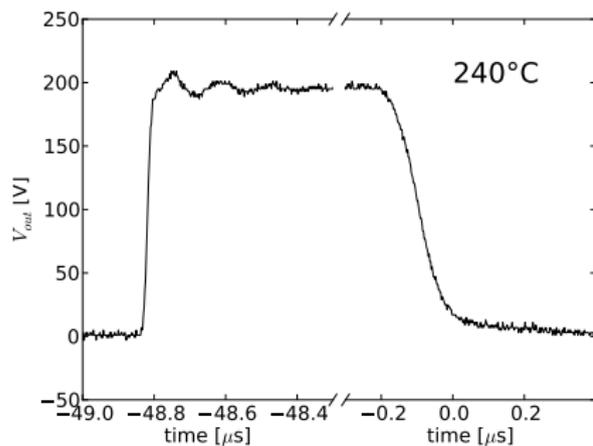
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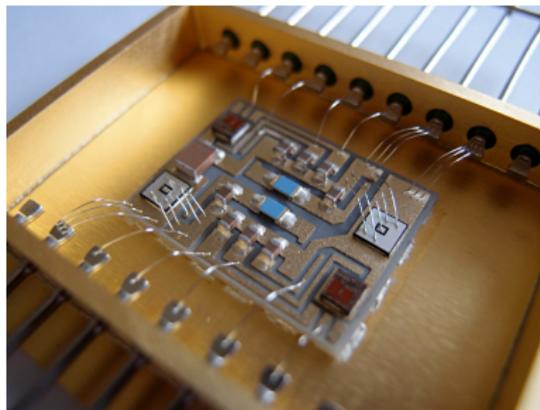
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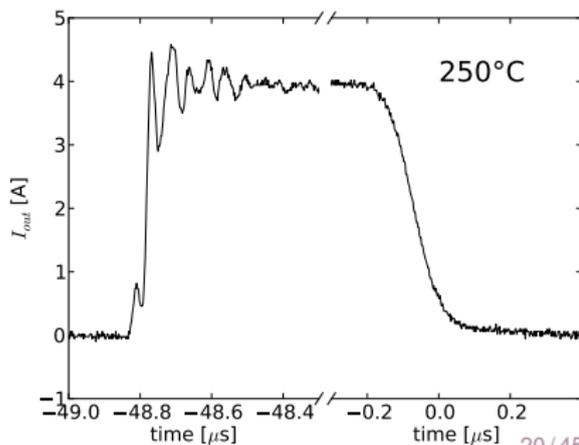
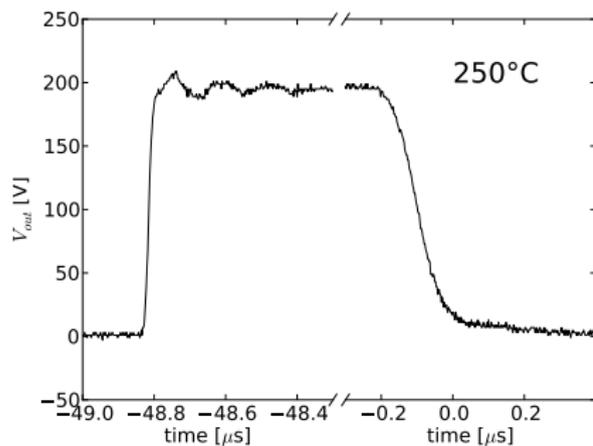
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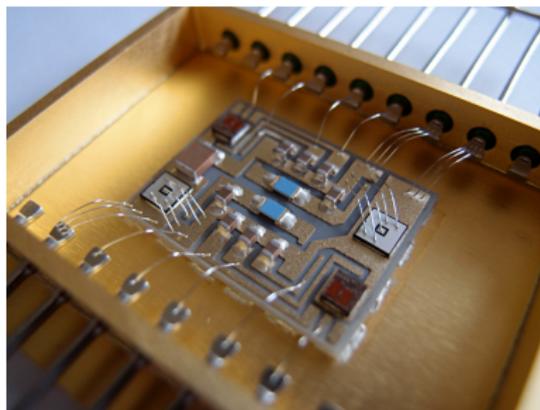
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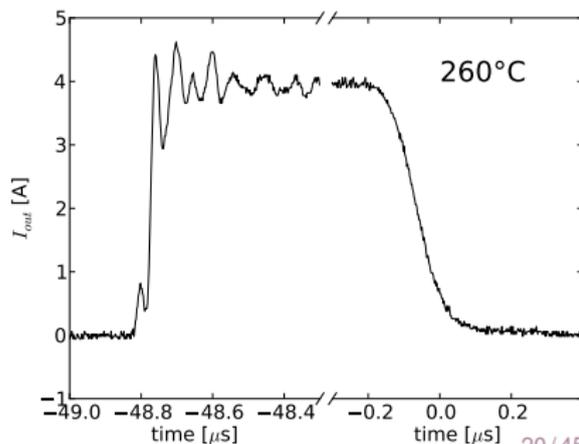
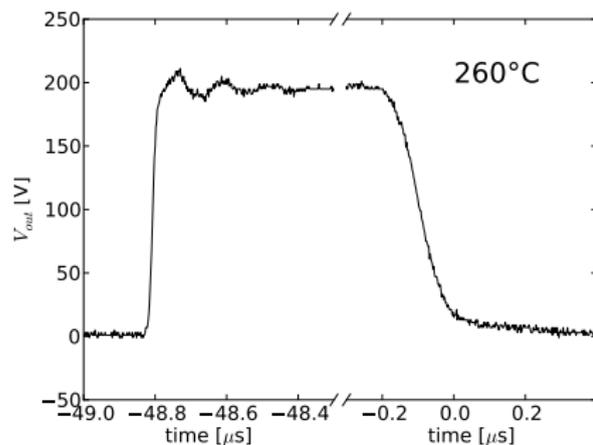
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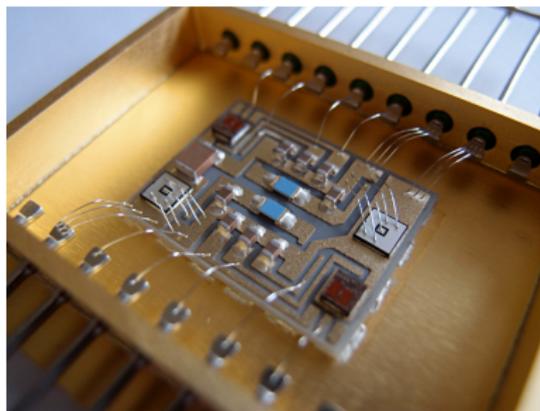
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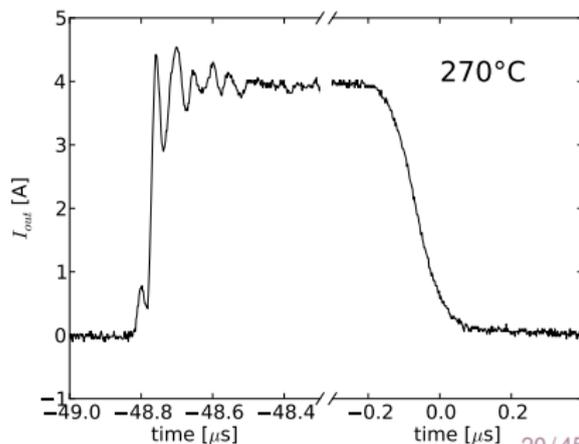
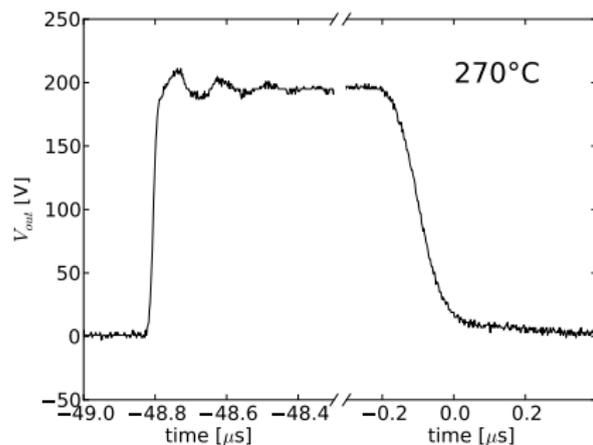
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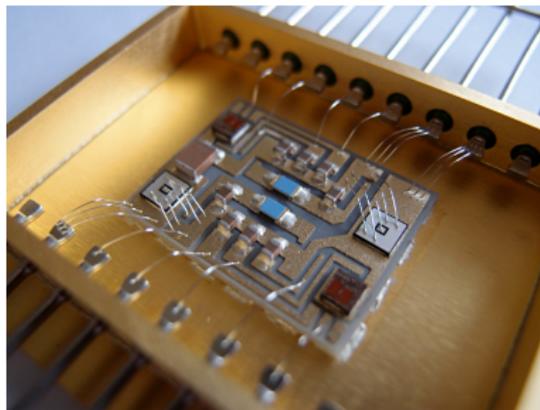
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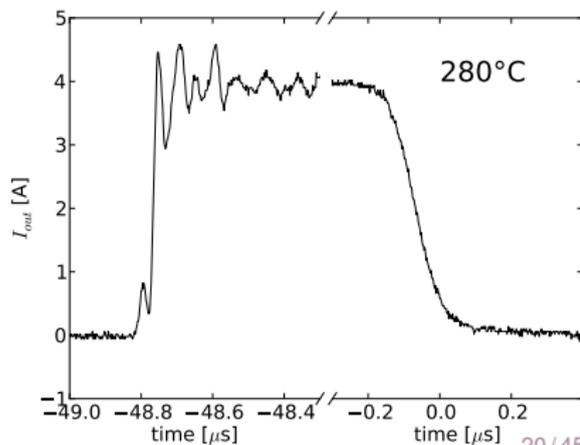
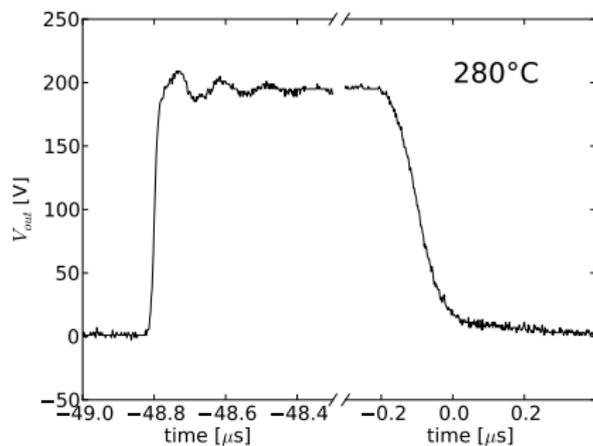
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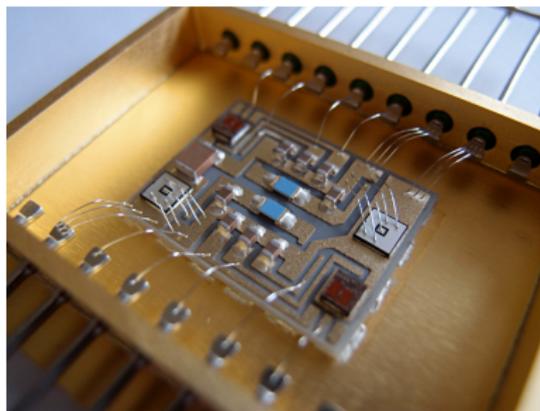
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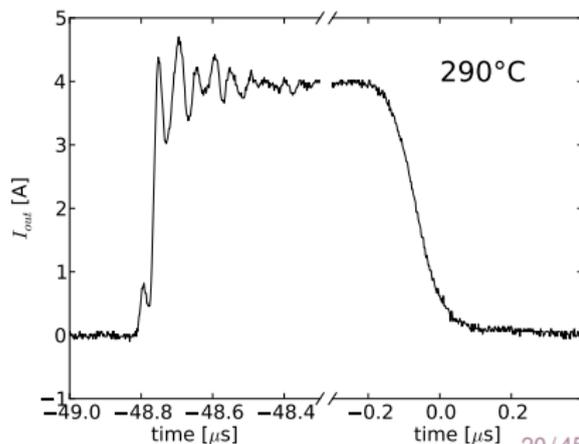
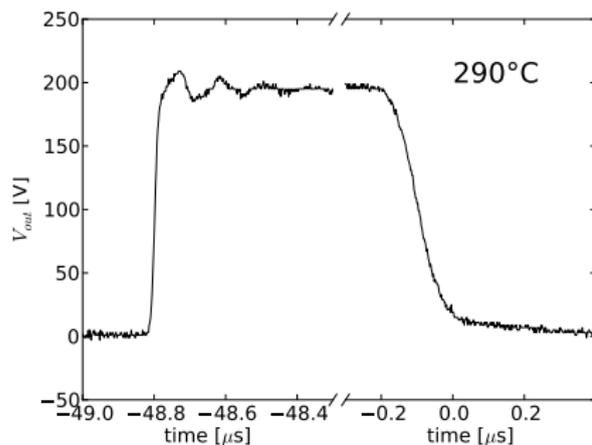
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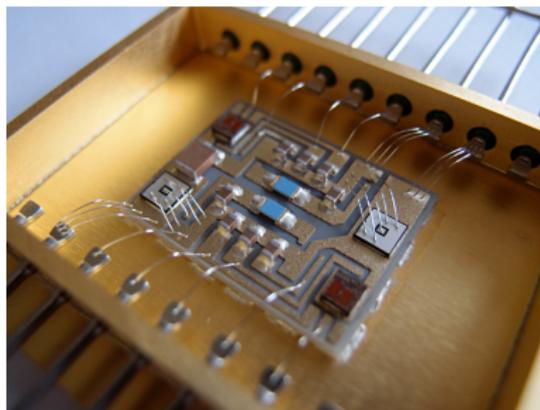
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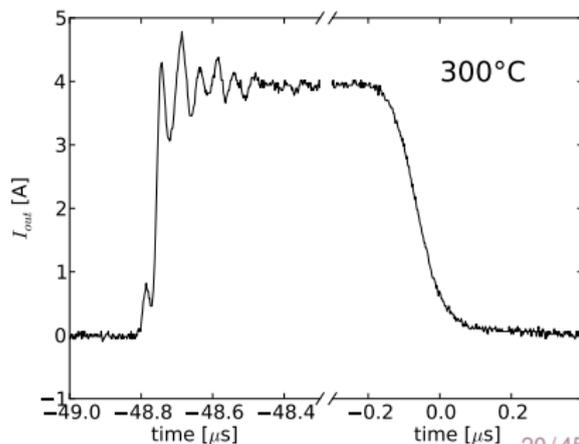
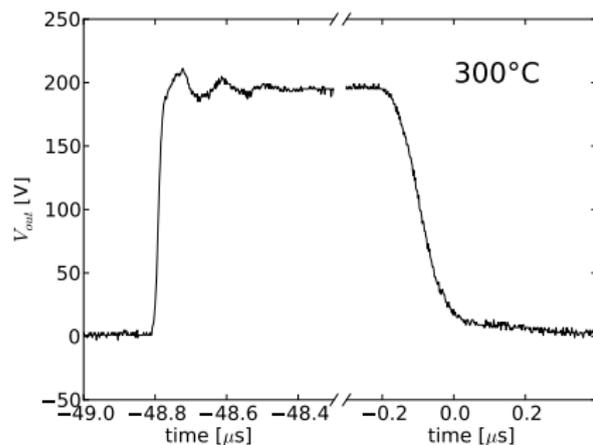
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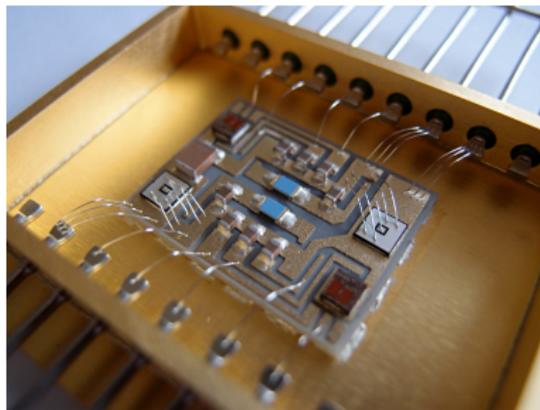
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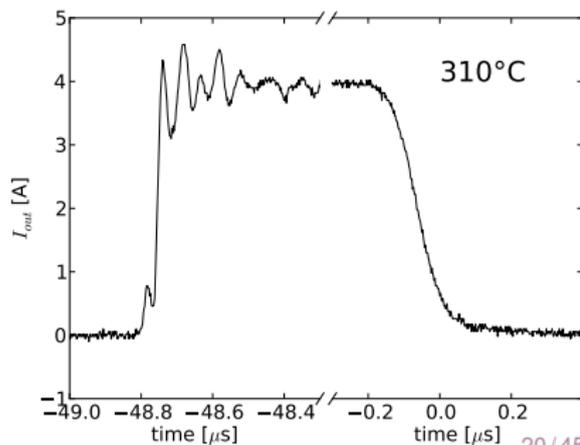
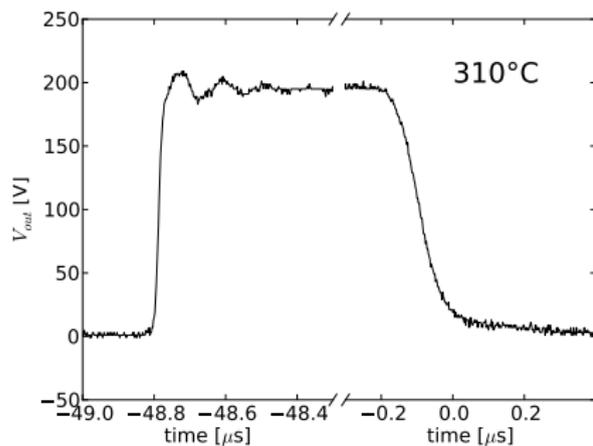
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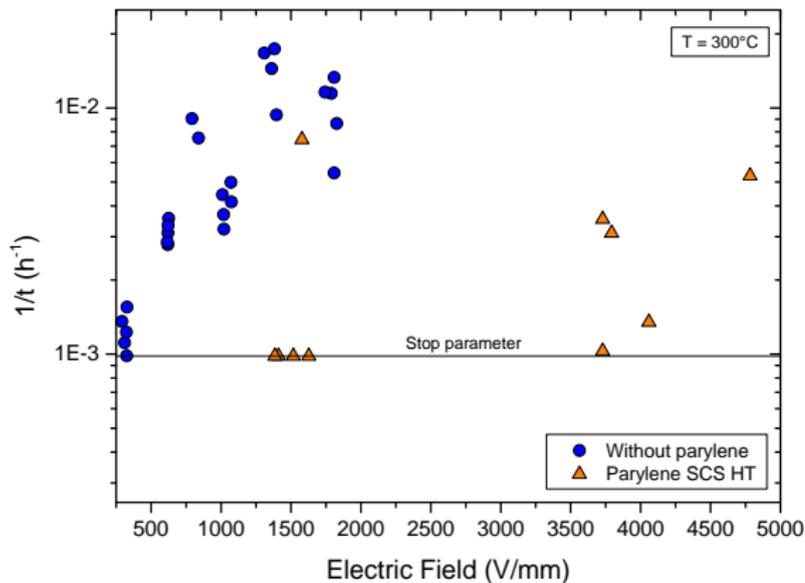
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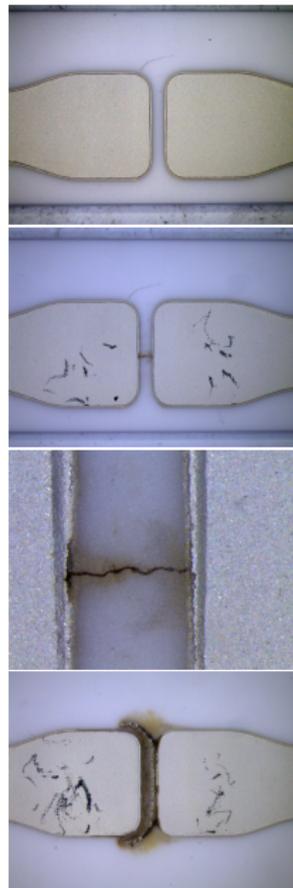
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High Temperature Die Attaches — Silver migration, R. RIVA



- ▶ Causes: electric field, high temperature and oxygen
- ▶ Large differences between similar test vehicles:
- ▶ **Short life without encapsulation (100–1000 h)**
- ▶ **Much longer life with parylene HT protection**



Conclusion on Packaging for High Temperature

SiC devices can operate at high temperature (>300 °C)

- ▶ With efficient thermal management!
- ▶ R_{Th} must remain low

Silver sintering for high temperature die attaches

- ▶ Compatible with standard die finishes
- ▶ Very good results
- ▶ High thermal/electrical performance
- ▶ Industry is catching on
- ▶ **Research:** long-term behaviour at elevated temperature
 - ▶ pressureless processes are a good model

Professional Record

Background

Contributions

Packaging for High Temperatures

New Packaging Structures for Power Modules

Perspectives

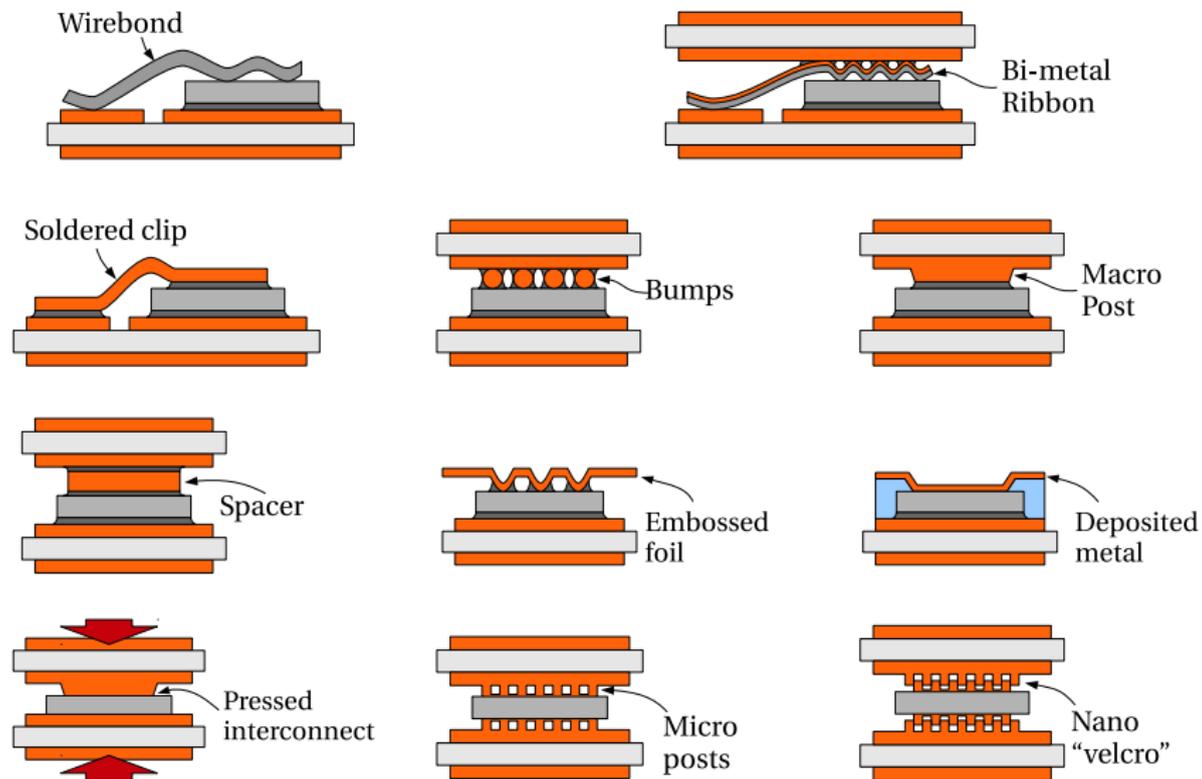
New Packaging Structures for Power Modules

Packaging for High Temperature

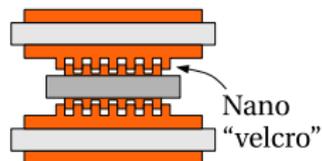
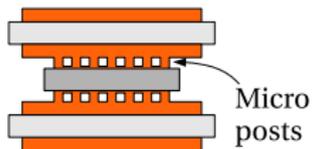
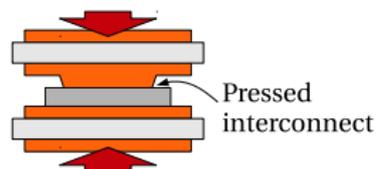
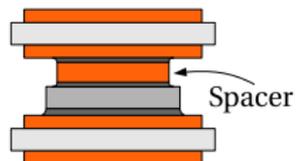
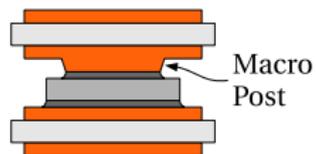
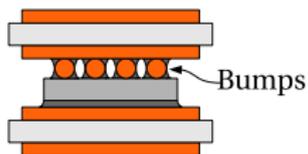
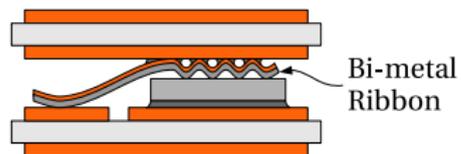
Packaging for High Voltages

Conclusion

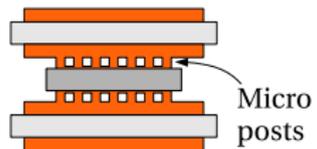
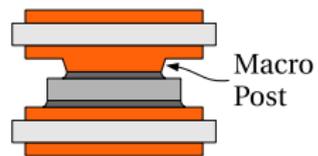
New Structures



New Structures



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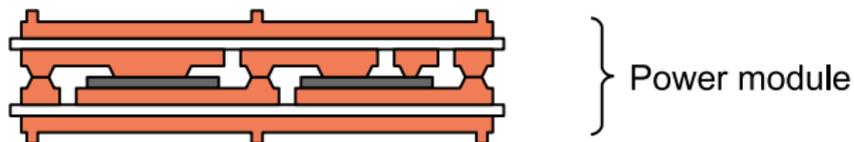


New Packaging Structures – Macro post 1



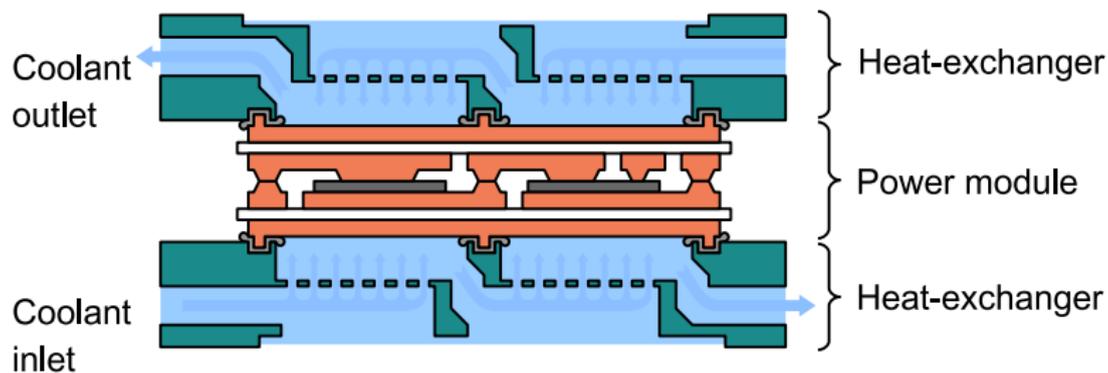
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New Packaging Structures – Macro post 1



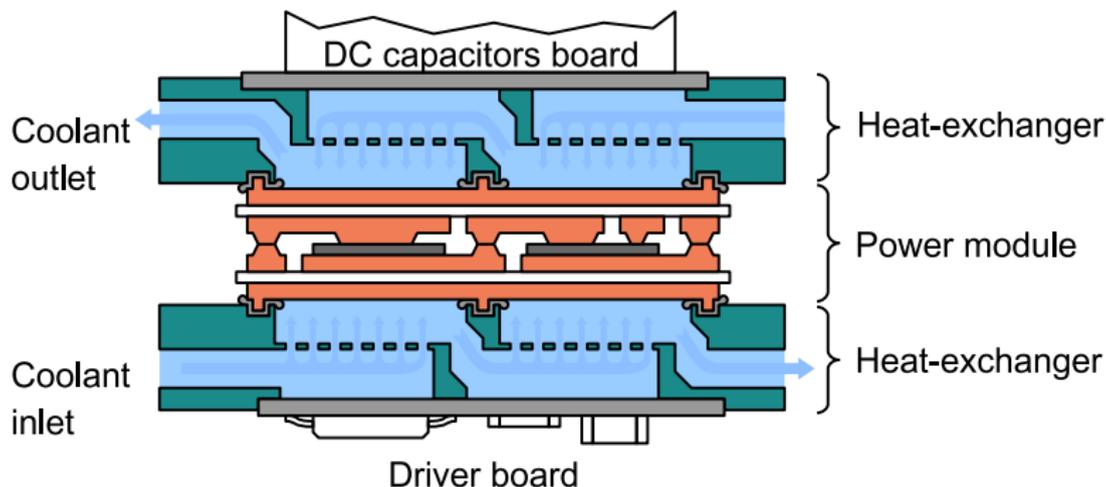
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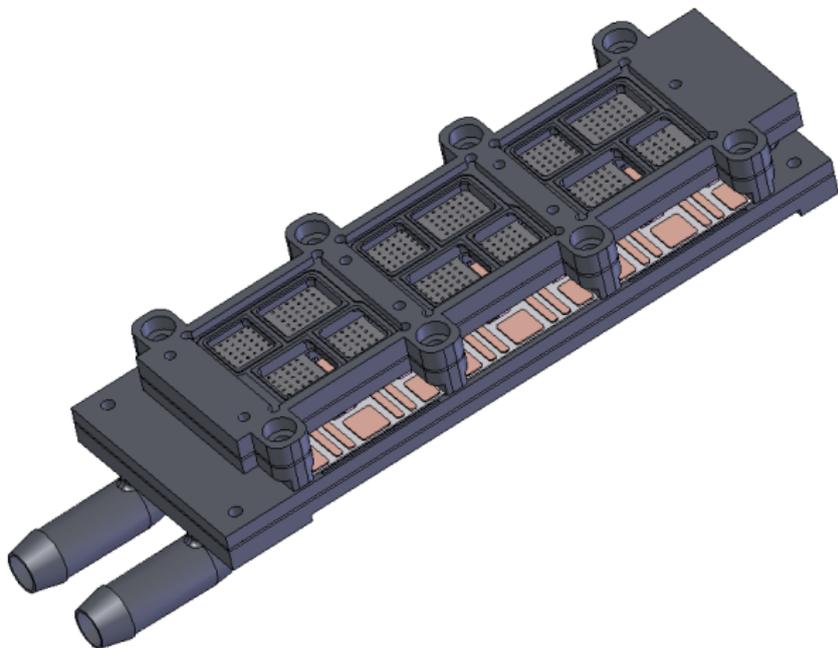
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- ▶ capacitor board;
- ▶ power terminals;
- ▶ busbar;
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New Packaging Structures – Macro post 1



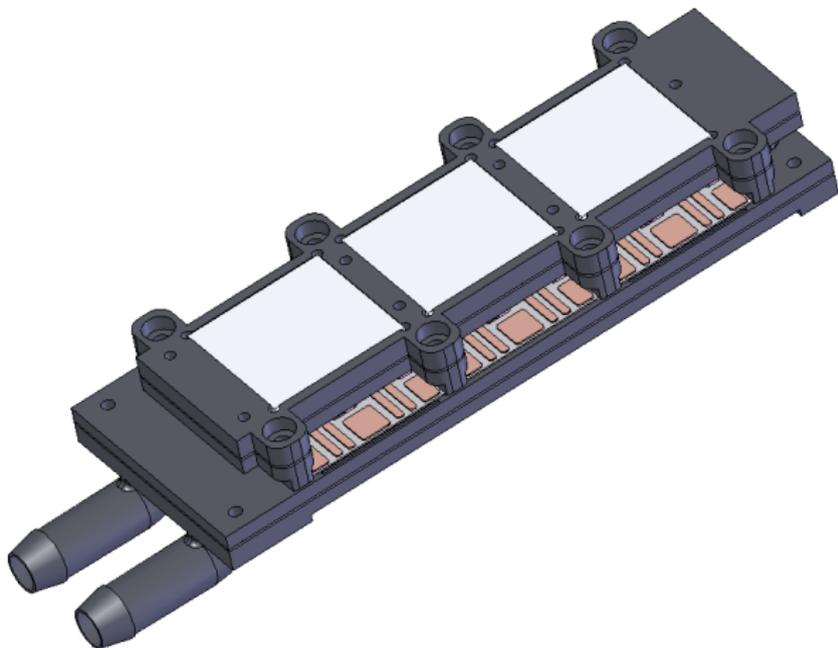
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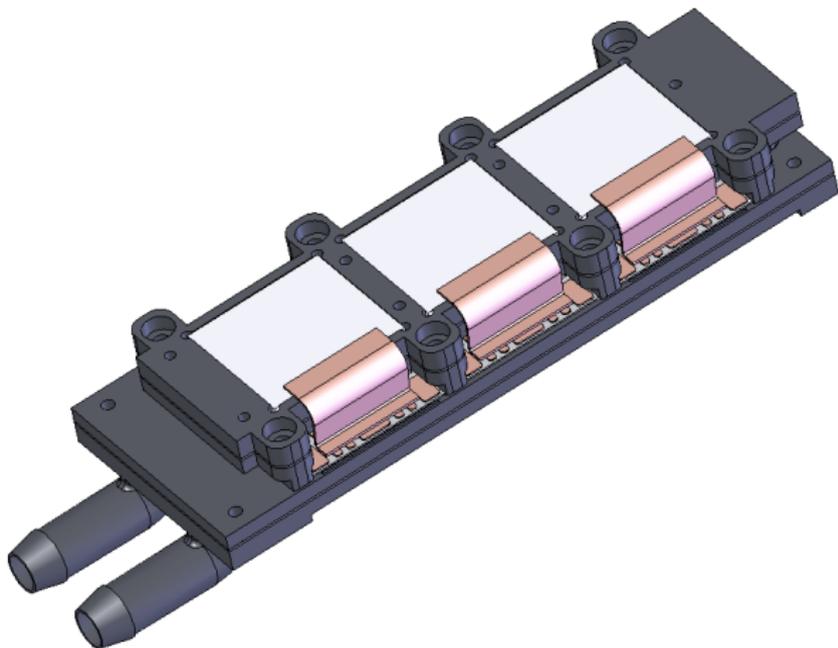
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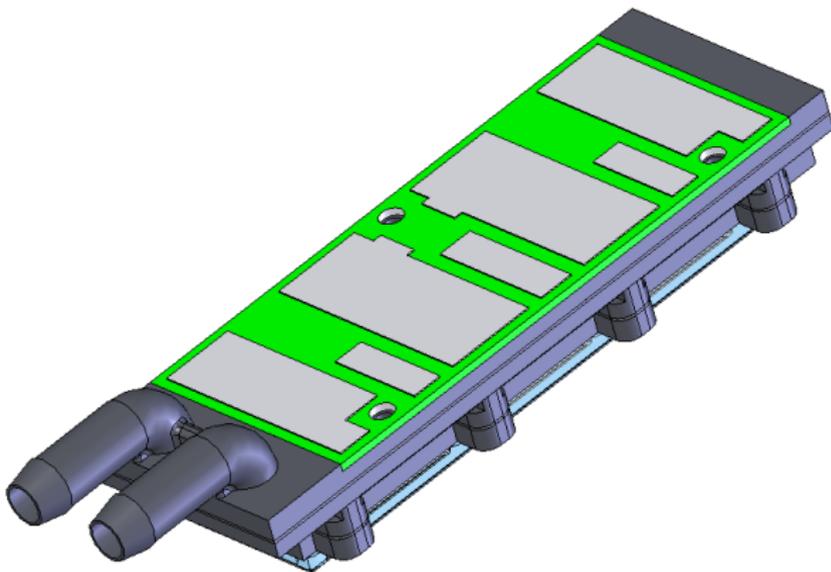
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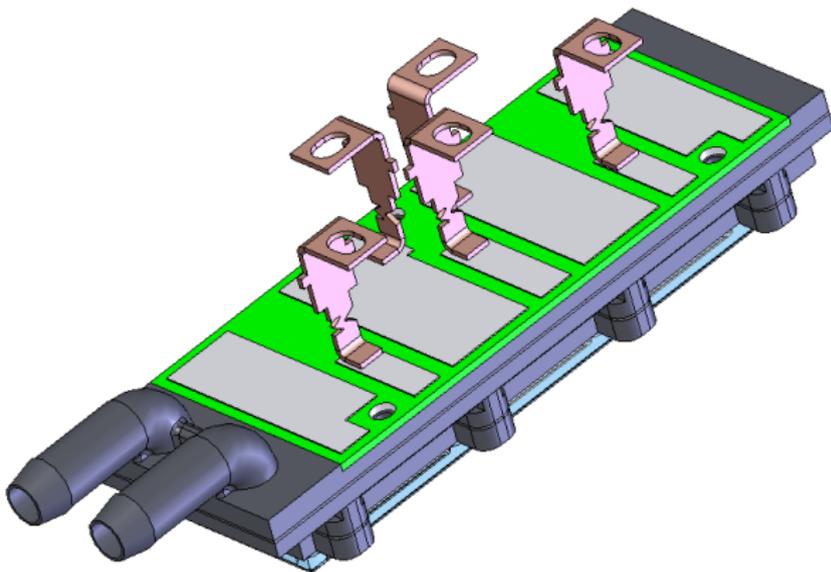
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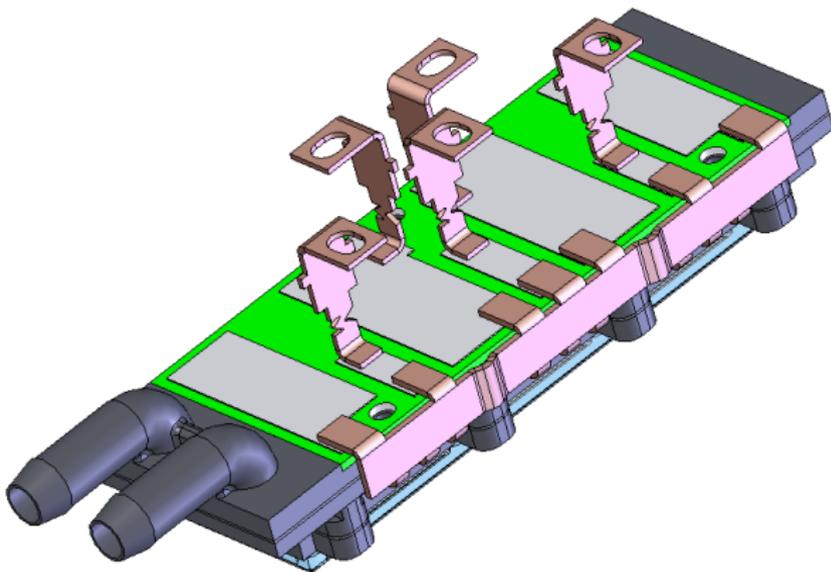
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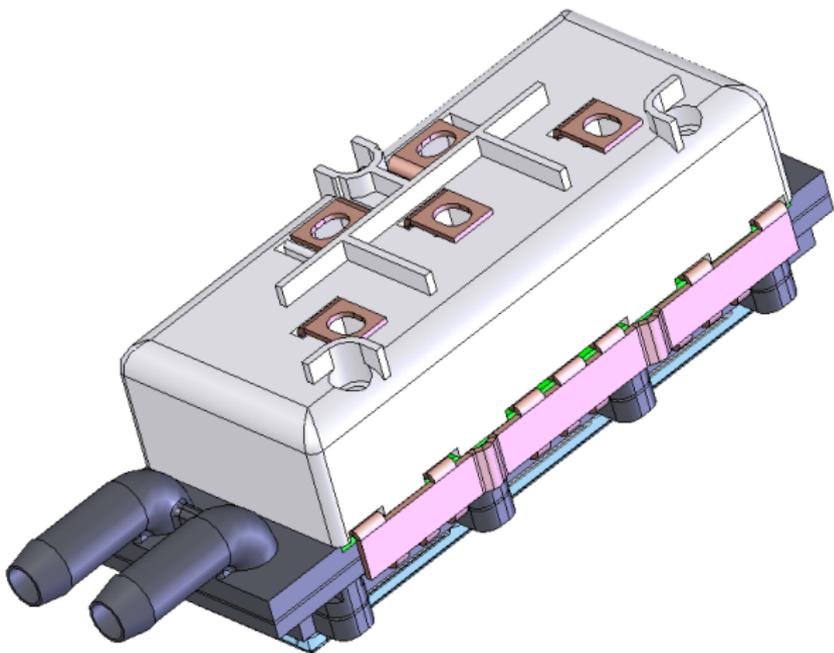
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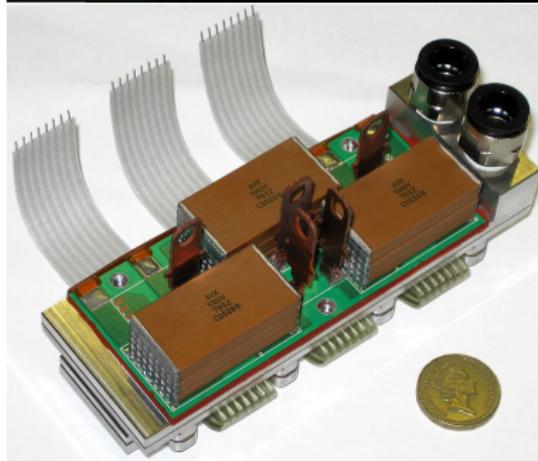
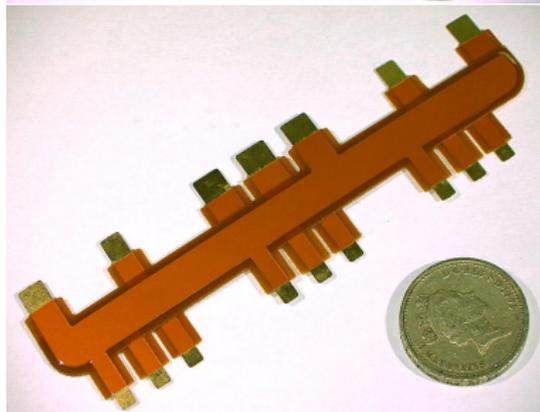
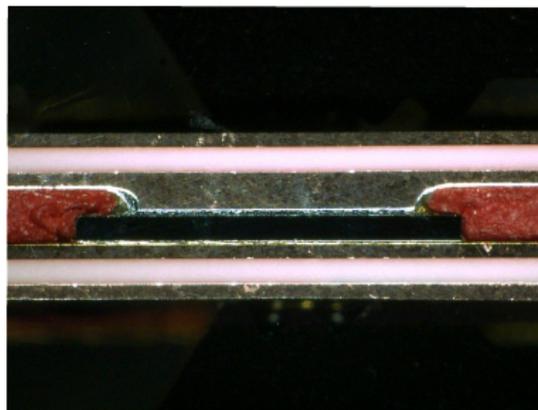
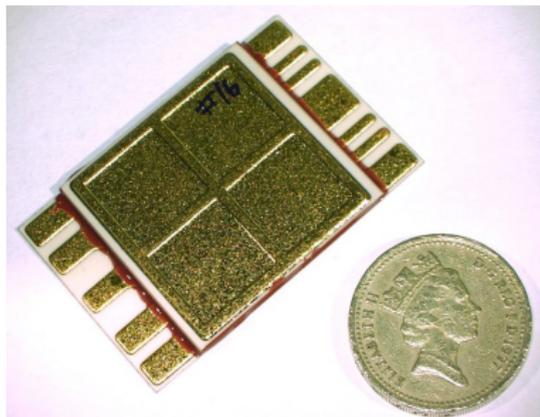
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- ▶ power modules
- ▶ “bottom” heat-exchanger;
- ▶ driver boards;
- ▶ driver interconnects;
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- ▶ capacitor board;
- ▶ power terminals;
- ▶ busbar;
- ▶ capacitor cover.

New Packaging Structures – Macro post 1

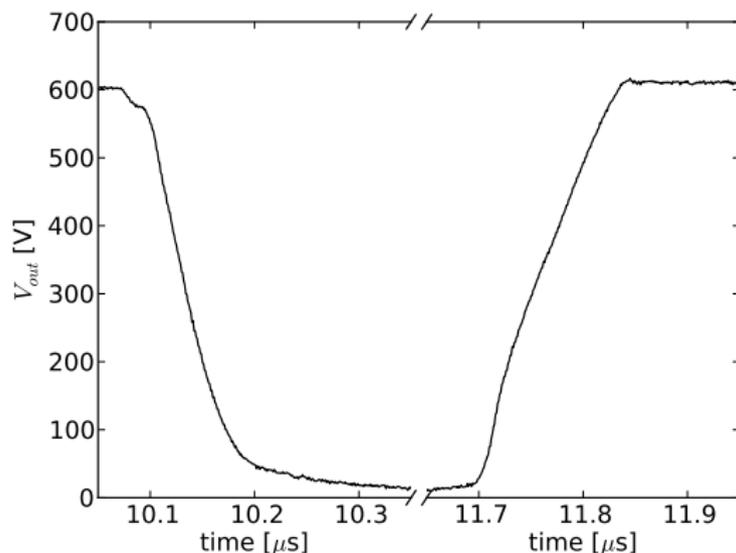


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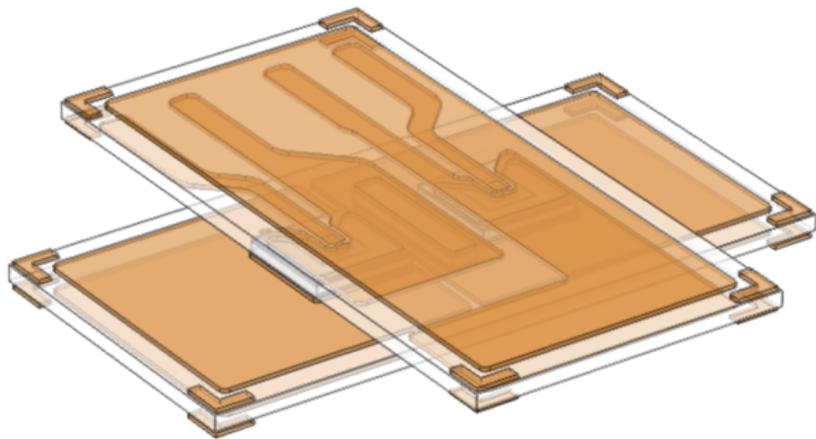
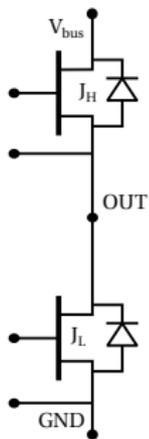


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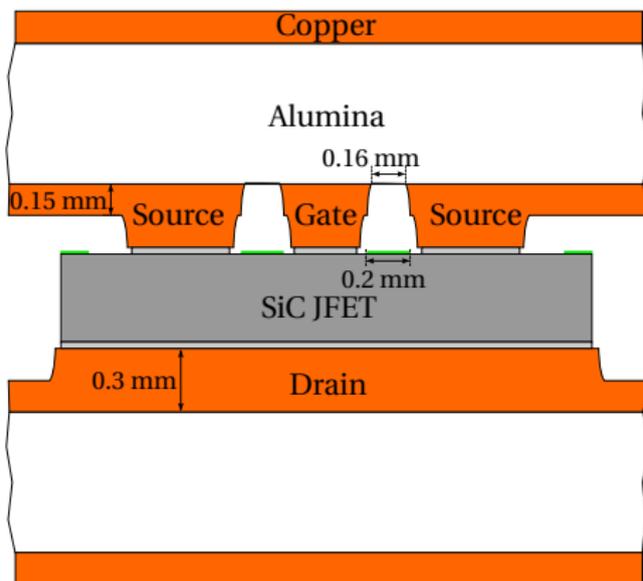
- ▶ Switching speed limited by switches (Si IGBTs, SiC diodes);
- ▶ No ringing measured at the terminals of the modules;
- ▶ DC link inductance estimated at 10 nH.

New Packaging Structures – Macro post 2 (R RIVA)



- ▶ Two ceramic substrates, in “sandwich” configuration
- ▶ Two SiC JFET dies (SiCED)
- ▶ assembled using silver sintering
- ▶ 25.4 mm×12.7 mm (1 in×0.5 in)

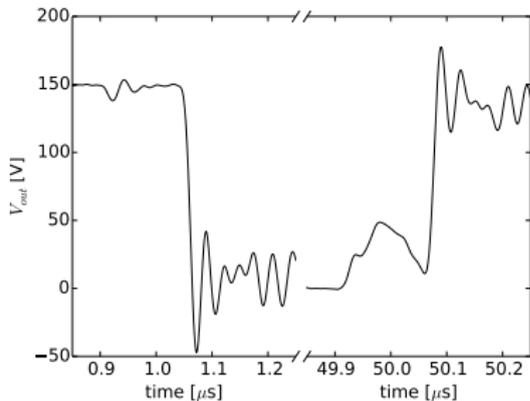
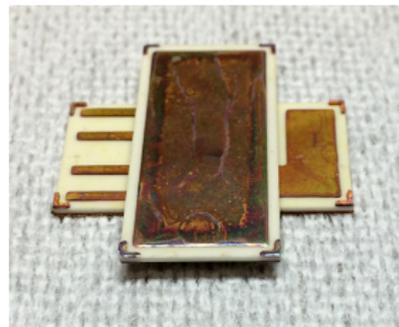
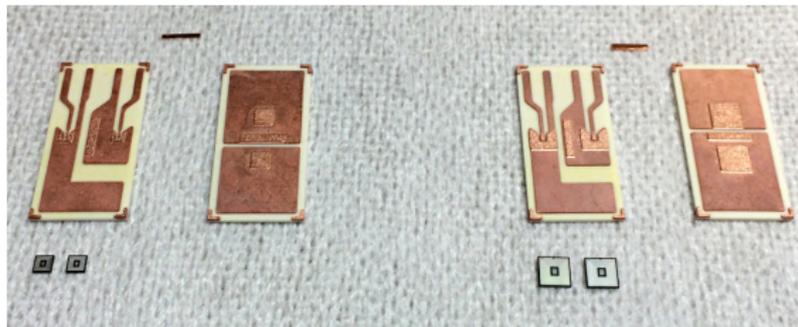
New Packaging Structures – Macro post 2 (R RIVA)



Scale drawing for $2.4 \times 2.4 \text{ mm}^2$ die

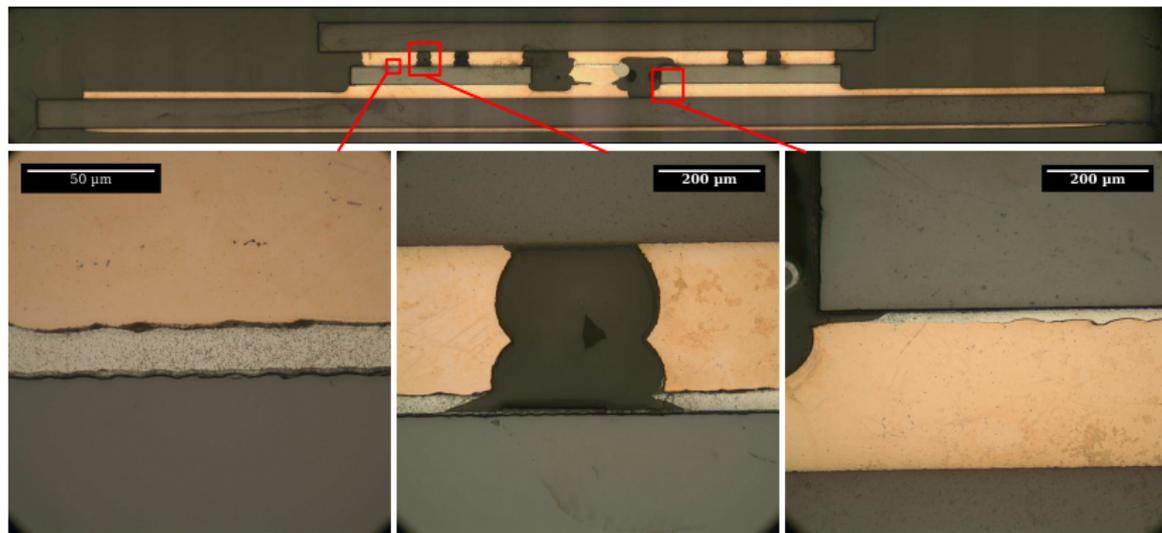
- ▶ Etching accuracy exceeds standard design rules
- ▶ Double-step copper etching for die contact
- ➔ Custom etching technique

New Packaging Structures – Macro post 2 (R RIVA)

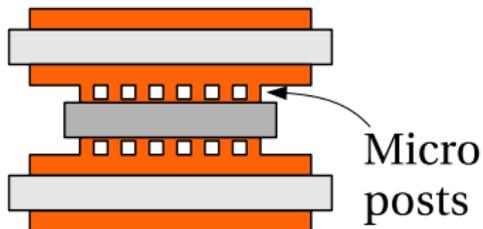


- ▶ Two-step etching of copper
- ▶ Ti/Ag PVD using shadow mask on dies
- ▶ Set of alignment jigs for assembly
- ▶ Proper drying of silver paste
- ▶ First electrical tests on 300Ω load

New Packaging Structures – Macro post 2 (R RIVA)



- ▶ Good form factor achieved using the two-step copper etching process
- ▶ Satisfying alignment
- ▶ Poor quality of Al-Cu attach



- ▶ First studies during L. MÉNAGER PhD
 - ▶ Copper posts growth on die (electroplating)
 - ▶ Original die/DBC assembly technology: SnCu diffusion bonding
- ▶ Proposition of M. SOUEIDAN: **direct copper bonding**

New Packaging Structures – Micro posts (B MOUAWAD)

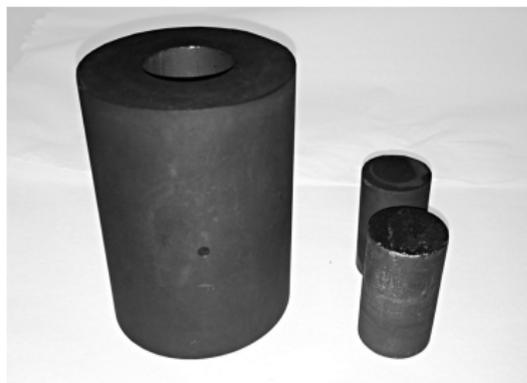


Parameters:

- ▶ SPS press
- ▶ Cu/Cu bonding
- ▶ 5 or 20 min
- ▶ 200 or 300 °C
- ▶ 16 or 77 MPa

- ▶ **Very good bond**, without any interface material
 - ▶ All configuration but one yield to bonding
 - ▶ Tensile strength 106 to 261 MPa (365 MPa for bulk copper)
- ▶ Parameters compatible with the process of a semiconductor die
- ▶ **Bonding mechanism still unclear**
 - ▶ Some investigations performed, much more needed

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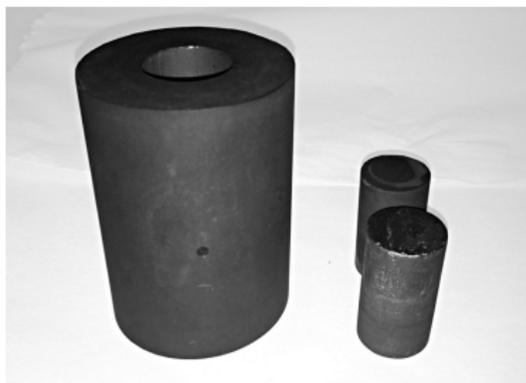


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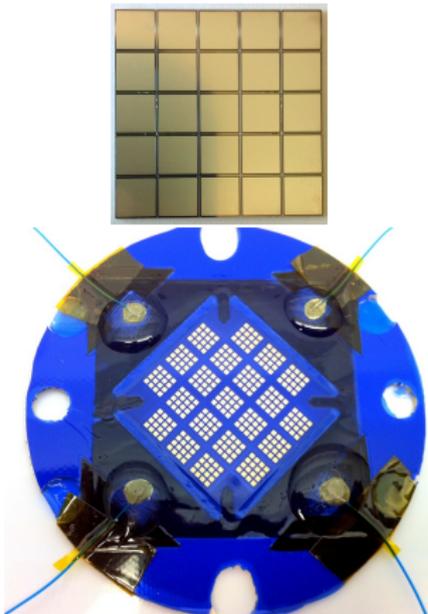


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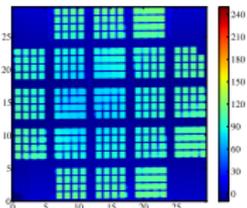
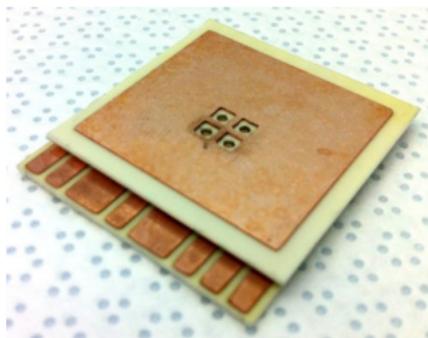
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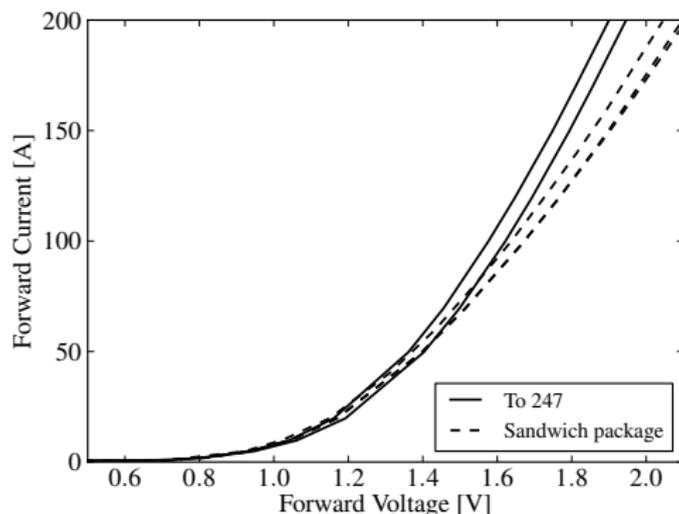
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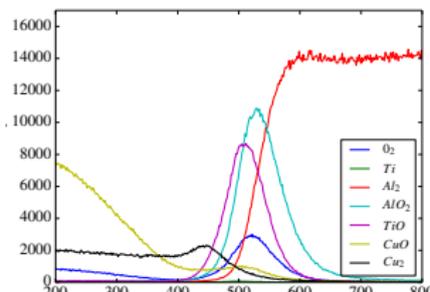
- ▶ “Wafer”-level process
- ▶ Based on copper electroplating
- ▶ Assembly of DBC/die/DBC “sandwiches”
- ▶ No damage to dies



New Packaging Structures – Micro posts (B MOUAWAD)



- ▶ Higher resistance than expected
 - ▶ Due to seed layer/die topside interface
 - ▶ Would not happen with suitable dies
- ▶ **Simple and reproducible process**
 - ▶ Tens of sample assembled, with good yield

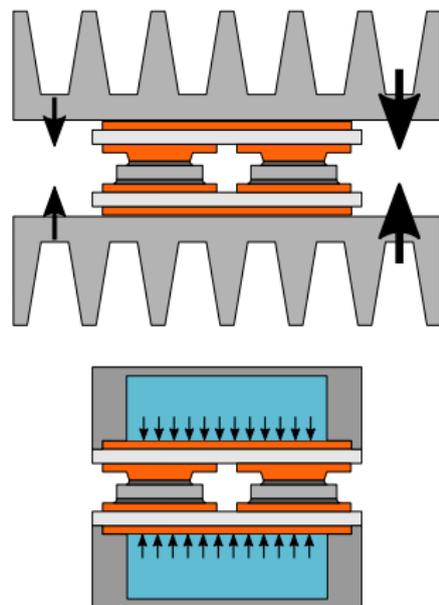


Conclusions on New Packaging Structures

- ▶ Several sandwich configurations:
 - ▶ Solder
 - ▶ Silver sintering
 - ▶ Direct Cu/Cu bonding (Micro-posts)
- ▶ More suited to direct liquid cooling
 - ▶ Solid/liquid interface
 - ▶ Homogeneous compressing force
 - ▶ No issue with flatness
- ▶ Remaining issues:
 - ▶ Dies topside finish
 - ▶ Mechanical relief structures
 - ▶ Intrinsic thermo-mechanical reliability

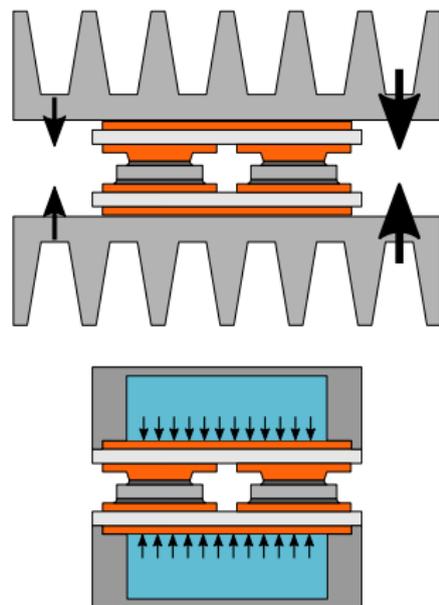
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 - ▶ Need for further investigation



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- Packaging for High Temperatures

- New Packaging Structures for Power Modules

Perspectives

- New Packaging Structures for Power Modules

- Packaging for High Temperature

- Packaging for High Voltages

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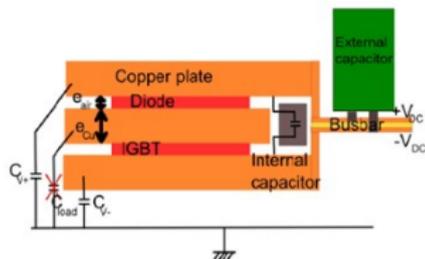
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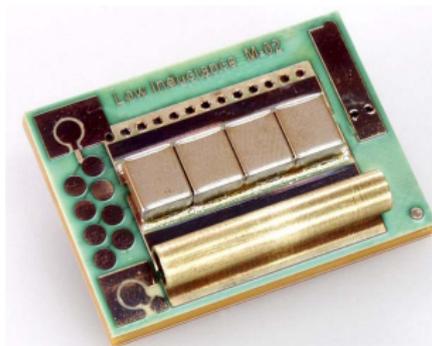
- ▶ Simulation-based design to evaluate
 - ▶ Thermo-mechanical stress in assemblies (esp. “Sandwiches”)
 - ▶ Thermal resistance
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J.-L. Marchesini et al., "Realization and Characterization of an IGBT Module Based on the Power Chip-on-Chip 3D Concept", ECCE 2014



E. Hoene, "Ultra Low Inductance Package for SiC" ECPE workshop on power boards, 2012

New Packaging Structures – PCB Embedding

PCB technology offers:

- ▶ High interconnect density (multilayers, $< 50 \mu\text{m}$ tracks)
- ▶ Advanced design tools
- ▶ Simple process (can be performed in-house, 3DPHI, industry)

To take advantage of previous developments

- ▶ Silver sintering for accurate positioning of devices
- ▶ Adaptation of die topside metallization
- ▶ Advanced DBC etching for thermal management



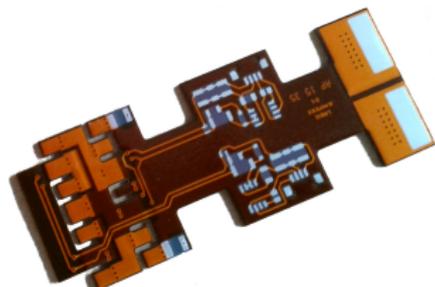
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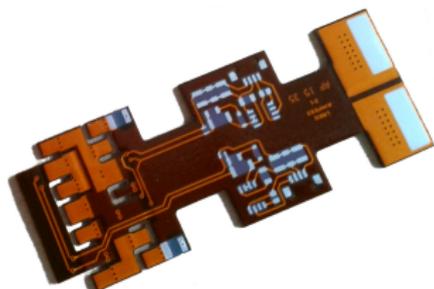
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PCB Embedding, ANR Project
ETHAER



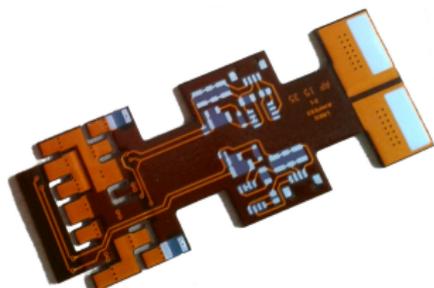
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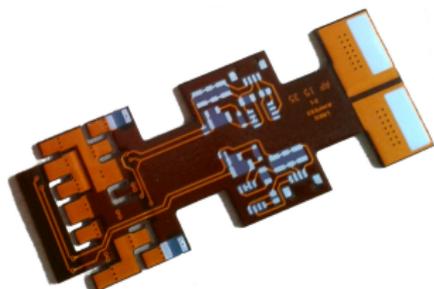
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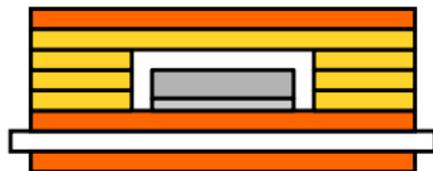
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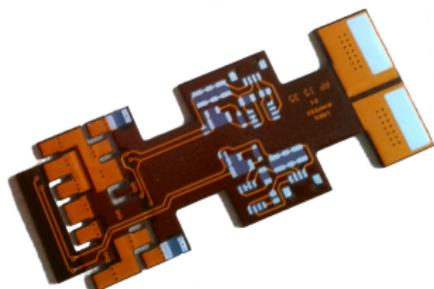
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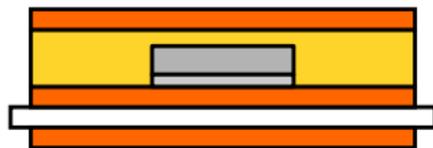
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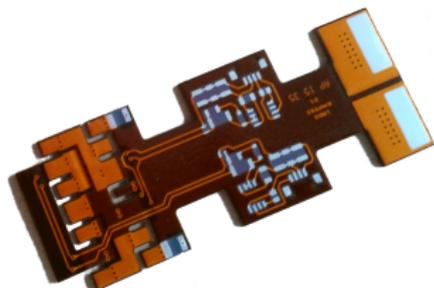
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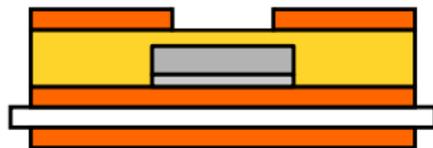
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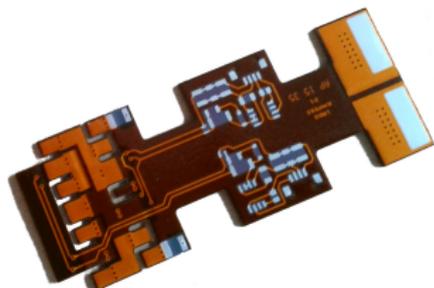
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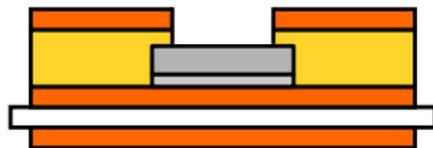
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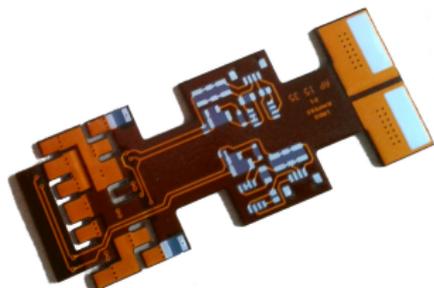
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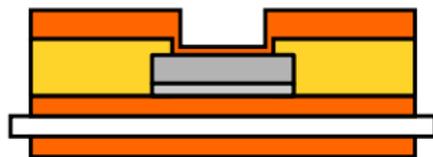
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PCB Embedding, ANR Project ETHAER



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Perspectives

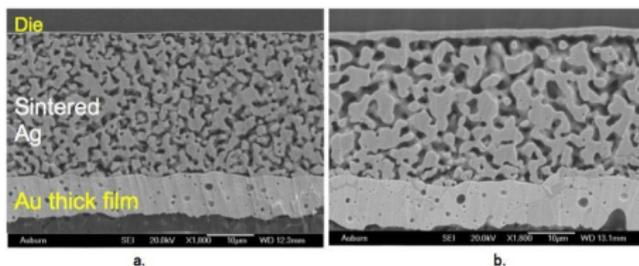
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- Packaging for High Temperature**

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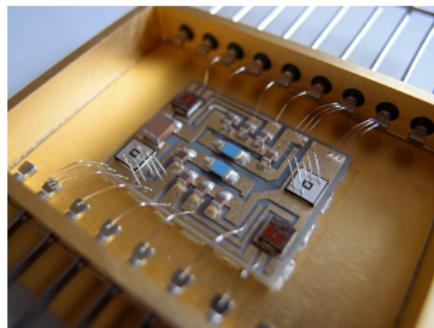
Reliability of High Temperature Packaging



Source: Pressureless Sintering of Microscale Silver Paste for 300°C Applications, Fang Yu et al., IEEE trans. on CMPT, vol. 5, No.9, p 1258–1264

- ▶ Silver sintered assemblies are increasingly available in the industry
- ▶ Need to assess its reliability for high temperature
 - ▶ Assessment of migration phenomenon
 - ▶ Next step: effect of atmosphere (oxygen content)
 - ▶ Use of pressureless sintered silver as a material model
 - ▶ Behaviour in high temperature storage conditions
 - ▶ Mechanisms are accelerated and highlighted

- ▶ Other elements of packaging:
 - ▶ High temperature ageing of PCBs
 - ▶ Thermo-mechanical analysis of structures
 - ▶ Manufacturing of integrated inductors
(C. MARTIN)



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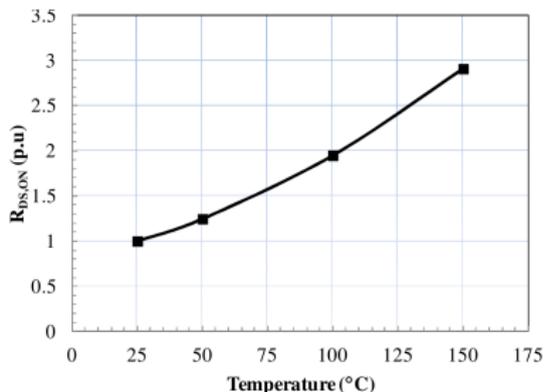
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Packaging of high voltage power devices

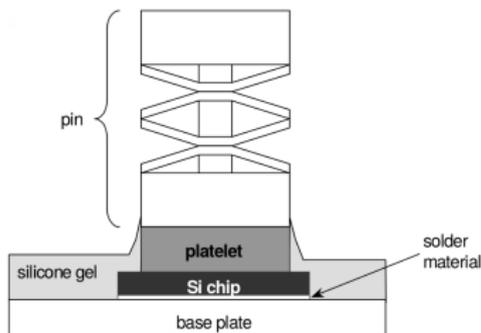
- ▶ Context: Supergrid Institute
- ▶ Development of HVDC networks
- ▶ Need for HV devices (>10 kV) and packaging



Source: 10 kV SiC MOSFET from Wolfspeed

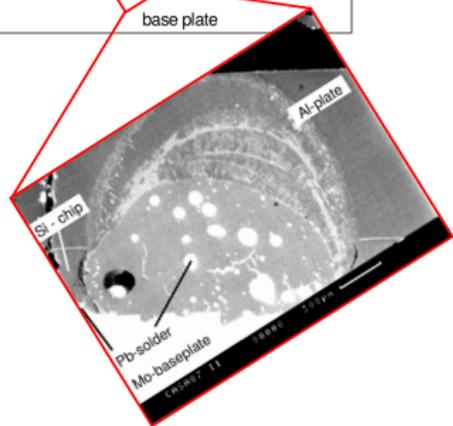
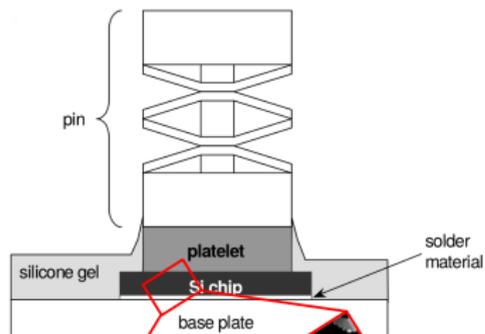
- ▶ Increase in switching speed
 - ▶ Ensure low inductance
 - ▶ Large creepage distance (> 8 cm !)
 - ▶ High conversion efficiency
 - ▶ Trade-off: Insulation/Junction temp.
- ➔ (Very) efficient cooling required!

Special Features of High Voltage Packaging



- ▶ Series connexions of many switches
 - ▶ A single failed switch should not stop the converter
- ➔ *Fail-to-short behaviour*
- ▶ For Si dies:
 - ▶ Melting of silicon
 - ▶ Alloying with surrounding metals
 - ▶ Formation of conductive area
 - ▶ SiC only sublimates at $> 2500^{\circ}\text{C}$!

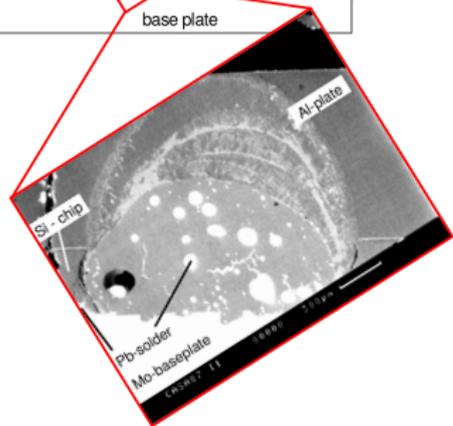
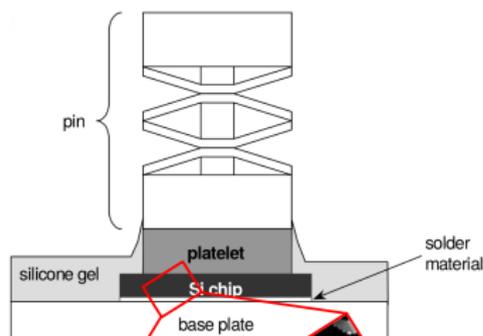
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Conclusion

Conclusion

- ▶ PhD 11 years ago
 - ▶ From electrical engineering to packaging
 - ▶ 11 PhD students supervised (5 theses defended)
- ▶ Until recently, most activity on high temperature packaging
- ▶ Broadening of my research focus
 - ▶ High temperature packaging
 - ▶ High voltage packaging
 - ▶ Integration for WBG devices
- ▶ Packaging is an active domain
 - ▶ Strong support from the industry
 - ▶ Many scientific challenges

Acknowledgements

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- ▶ picture of the Airbus A350: airbus
- ▶ picture of the Toyota Prius: Picture by Pawel Golsztajn, CC-SA, available on Wikimedia Commons http://commons.wikimedia.org/wiki/File:Toyota_Prius.2.JPG
- ▶ geothermal power plant: <http://energy.gov/eere/geothermal/photos/geothermal-photo-gallery>
- ▶ picture of Jupiter: NASA http://en.wikipedia.org/wiki/File:PIA04866_modest.jpg