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Robert Polster

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Architecture of Silicon Photonic Links

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Architecture of Silicon Photonic Links

Robert Paul Polster

September 30, 2015

“Everybody’s worried about stopping terrorism. Well, there’s a really easy way: stop participating in it.”

Noam Chomsky

Abstract

Future high performance computer (HPC) systems will face two major challenges: interconnection bandwidth density and power consumption. Silicon photonic technology has been proposed recently as a cost-effective solution to tackle these issues. Currently, copper interconnections are replaced by optical links at rack and board level in HPCs and data centers. The next step is the interconnection of multi-core processors, which are placed in the same package on silicon interposers, and which define the basic building blocks of these computers. Several works have demonstrated the possibility of integrating all elements needed for the realization of short optical links on a silicon substrate.

The first contribution of this thesis is the optimization of a silicon photonic link for highest energy efficiency in terms of energy per bit. The optimization provides energy consumption models for the laser, the de- and serialization stage, the ring resonator as modulator and supporting circuitry, the receiver front-end and the decision stage. The optimization shows that in optical links the main consumers are the laser and the modulator's supporting circuitry. Using consumption parameters either gathered by design and simulation or taken from recent publications, the optimal bit rate is found in the range between 8 Gbps and 22 Gbps, depending on the used CMOS technology. Nevertheless, if the static power consumption of modulators is reduced it could decrease even below 8 Gbps.

To apply the results of the optimization an optical link receiver was designed and fabricated. It is designed to run at a bit rate of 8 Gbps. The receiver uses time interleaving to reduce the needed clock speed and elevate the need of a dedicated deserialization stage. The front-end was adapted for a wide dynamic input range. In order to take advantage of it, a fast mechanism is proposed to find the optimal threshold voltage to distinguish ones from zeros.

Furthermore, optical clock channels are explored. Using silicon photonics a clock can be distributed to several processors with very low skew. This opens up the possibility to clock all chips synchronously, relaxing the requirements for the necessary buffers within the communication channels. The thesis contributes to this branch of research by presenting two novel optical clock receivers. Clock distribution inside chips is a major power consumer. With small adaptation the clock receivers could also be used inside on-chip clocking trees.

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Chapter 1

Introduction

“Nothing can have value without being an object of utility.”

Karl Marx

1.1 Motivation

The invention of the computer changed the work flow in nearly all industries and research directions. Modern computers are used for data storage, media preparation, industrial control and many more applications. From the beginning computers have been used for complex numerical problems. The growth of computing power in the last decades gathered a lot of interest in finding solutions for various problems numerically. This led to so called high performance computing (HPC) systems, see Fig.1.1. HPCs are used for applications such as weather forecasts, aerodynamic simulations, geological simulations, drug discovery or high energy physics simulations.



Figure 1.1: IBM's Blue Gene P Supercomputer¹and applications of HPC Systems

¹Credits: Argonne National Laboratory

Although Moore’s Law seems to lose its validity, HPCs continue to gain one order of magnitude in performance every four years. This trend is shown in Fig. 1.2. The fastest HPC system that is currently running is the Tianhe-2, it reaches 33.86 PFlops/s. Tianhe-2 is composed of 3,120,000 cores and consumes 20 MW. These two figures illustrate well the bottleneck of modern HPCs: interconnect bandwidth and power consumption. 20 MW corresponds to a yearly energy cost of 17 MEuro if a price of 10 cents per kWh is considered. Apart from the financial problem, the heat evacuation of these systems also poses a problem that sets limits to HPCs today.



Figure 1.2: Performance Development of HPCs²

The second bottleneck becomes apparent when it is considered that 3,120,000 cores need to exchange data in order to work together. HPCs are hierarchical systems that are ordered in sub divisions. In order to reduce the internal traffic, programs are optimized to limit the necessary communication between a sub division and its environment. The following table lists common sub divisions and common data throughput between these divisions.

Division	Communication [bits/FLOP]
Rack	0.12
Blade	1
Module	2
MPU	4

²Credits: www.top500.org

MPU represents here Microprocessor unit. High throughput electronic connections are generally well designed transmission lines, but their bandwidth is limited due to the skin effect and matching problems. In [1] the following relation is derived:

$$B < B_0 \frac{A}{l^2},$$

where l is the length of the link and A the cross section of the link. B_0 is a constant, it is $\approx 10^{16}$ on-chip and $\approx 10^{17}$ off-chip. In order to sustain the growth of HPCs, MPUs with 10 TFLOP are predicted for 2020. They will require an MPU to memory bit rate of 40 Tbps. If a chip distance of 5 cm and a line width of 50 μm is assumed, the needed perimeter to accommodate all the I/O transmission lines becomes 20 cm! This result shows clearly that copper lines will not be capable of providing the bit rates densities needed in future HPCs.

Data centers (DC) are a specific type of supercomputers. They are adapted to handle big data bases and they have, for this reason, an architecture focused on fast memory access. This leads eventually to the same bottlenecks as for HPCs.

1.2 General Trends of Optical Links

Optical links are deployed since the 1980s, see Fig. 1.3. Until now the only commercialized products replace copper cables with optical fibres. The main reason to do that used to be the low loss of optical fibers allowing long-haul communication with only a few repeater stations. Increasing bit rates in local area networks (especially those of HPCs and DCs) made optical fibres interesting for links in the range of meters, as their superior bandwidth loss product allows faster links with less latency. While fibres are still used to connect neighbouring racks, new technologies have to be introduced to be implemented on optical backplanes, blades or modules. Therefore, waveguides are about to be integrated at the PCB level that are used in the next generation of HPCs. This brings optical I/O closer to the computing processors and communication interfaces. An MCU in 2020, performing 10 TFlops, will contain over 100 processing units. In order to connect these nodes so called Systems in Package (SiPs) are under development. In these SiPs several CPUs are flip-chipped onto a silicon photonic interposer, that connects all nodes using an optical network.

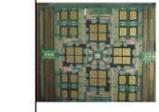
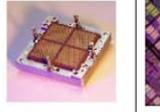
	Internet, Wide Area Network	Local Area Network	Rack-to-Rack	Card-to-Card	On-Card	On-MCM	On-Chip
							
Distance	multi-km	10 - 2000 m	30+ m	1 m	0.1 - 0.3 m	5 - 100 mm	0.1 - 10 mm
Number of lines	1	1 - 10	~100	~100-1000	~1000	~10'000	~100'000
Use of optics	Since the 80s and the early 90s	Since the late 90s	Now	2010+	2010-2015	Probably after 2015	Later, if ever

Figure 1.3: Development of optical links²

Fig. 1.4 gives a more detailed idea about the recent developments inside HPCs and the corresponding optical links. Optical links that are connected to electric-optic converters at the blade edge are standard nowadays. In the second scenario optical fibers reach the single modules on the blade. Electric-optic converters for this usage are already applied and on the market [2]. The next evolution that is currently in development is the already mentioned waveguides containing PCB. The final step to a maximal penetration depth of the optical network into HPCs is the direct coupling of the MCUs and on-chip memories using optical links.

²Credits: IBM

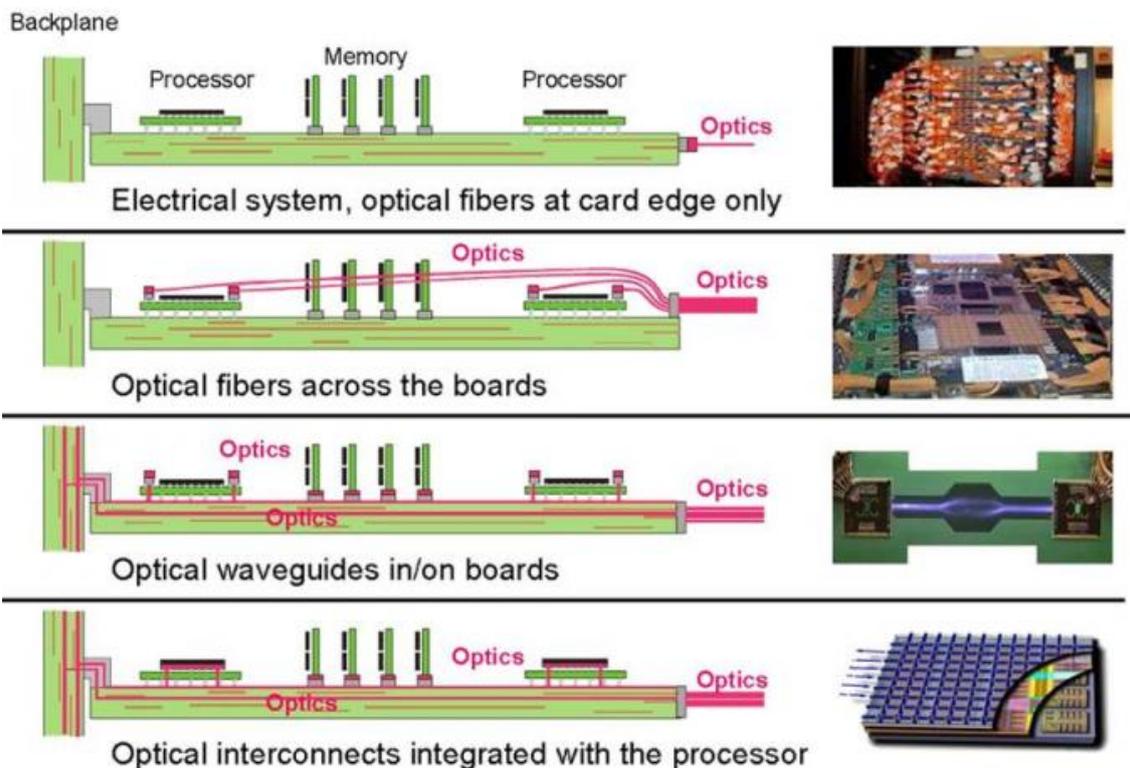


Figure 1.4: Penetration depth of optical links inside HPC racks ²

This final step leads to a change in the development of optical links. For all cable-replacement solutions size and technology are only minor factors but production price and maximal bit rate are of highest priority. This simplifies the optical communication by minimizing the number of optical fibres that need to be aligned. Cable replacement circuitry is most of the time discrete electronics in order to combine the best technologies for each part of the transceiver. The electronics are therefore mainly produced in III-V bipolar technologies. The optical part of the transmitter is often a vertical-cavity surface-emitting laser (VCSEL). These discrete devices can have large output powers while being directly modulated at high bit rates. Although, this approach seems to be optimal for fibre connections, it is not adapted to connect chips in proximity to each other. It might be also disadvantageous for the mentioned optical PCBs.

Therefore, a paradigm change is required. The electric transceivers driving the optics must be designed in CMOS technologies to become very low cost if they are supposed to become the standard I/Os of MCUs. The energy efficiency of these short range optical links is of highest importance. In order to compete with the efficiency of copper connections optical links must reach an energy efficiency of 1 pJ/b or lower. One important parameter to optimize the energy efficiency is the

link's bit rate.

Silicon photonics combines the production techniques of CMOS technologies with optics. It offers nowadays all elements needed for high speed optical links, such as waveguides, modulators, splitters, filters and receivers. Due to the high optical index contrast of air and silicon, silicon photonics can offer very high bit rate densities. A silicon photonic waveguide can be as thin as 400 nm and carry up to 80 standardized channels. Recent publications report bit rates for silicon photonic transceivers up to 25 Gbps per channel. The total achievable throughput of a silicon waveguide is therefore 2 Tbps, i.e. that 20 waveguides ($\approx 20 \mu\text{m}$ wide) are sufficient to carry the needed 40 Tbps of future MCU to memory links. This means that the bit rate does not need to be as fast as possible but it becomes part of the general optimization of a link. This is why silicon photonics is considered to replace short range copper connections in the near future.

1.3 Objective of this Thesis

This work's goal is to contribute to the optimization of silicon photonic links for future multi-chip modules in DC and HPC applications. In order to contribute to the solution of the explained bottlenecks the focus lies on the reduction of the energy per transmitted bit and the footprint of the circuitry. Furthermore, an entire receiver circuit is developed and presented.

Detailed objectives of this thesis are:

1. **Energy Efficiency:** Parametrizing an optical link with an energy efficiency better than the community goal of 1 pJ/bit.
2. **Bit Rate:** Finding the most energy efficient bit rate for short range optical links.
3. **Architecture:** Defining the most energy efficient optical receiver architecture for optical links, adapted for system in package applications.
4. **Design:** Designing an optical receiver for optical links in a 65nm CMOS technology.
5. **Characterization:** Proving the validity of the developed concepts by characterizing the receiver under different conditions.

The work was carried out in the framework of the HUBEO+ project. This program envisions a MCU as shown in Fig. 1.5. Using 3D-Integration techniques, memory chips are stacked upon computing chips that are interconnected with each other using an optical network integrated on a silicon photonic interposer. This framework puts certain constraints on the degrees of freedom of this work. The electric front-ends of the receivers are included on the computing chips and copper-pillars will be used to connect these to the photodiodes or to optical modulators.

The optical components are fabricated on the optical interposer. The technology was defined to be a CMOS 65nm technology for the first runs and only future steps will use the more advanced FDSOI 28nm technology. Any big components such as inductors are forbidden to optimize the footprint. This is necessary because many receivers and transmitters inside a single processing unit will be required to achieve the foreseen overall bit rate. Finally, the bit rate of the demonstrator was fixed to 8 Gbps. It will be shown that the bit rate is a critical parameter in the design of optical links, as the power efficiency of different devices, in terms of energy per bit, scales differently with the bit rate. This work will argue for another value which was obtained during the project.

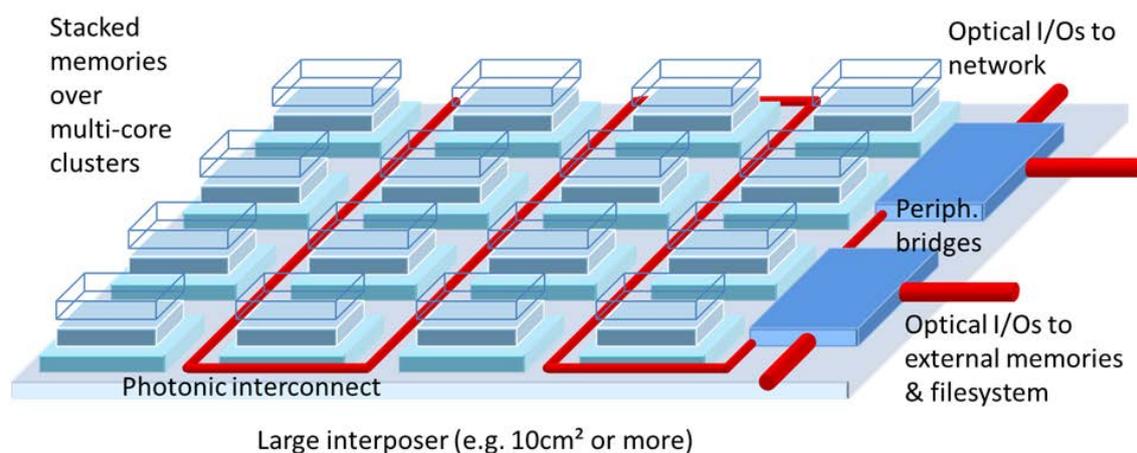


Figure 1.5: Model of the HUBEO Vision of MCMs

1.4 Structure and Methodologies

The first chapter introduces the reader to the state of the art of optical links in general as well as to the state of the art of silicon photonic links.

In the second chapter an optimization study for optical links is presented. The optimization study serves mainly to find the optimal bit rate of silicon photonic links, as the previous paradigm of maximizing bit rate over everything cannot be sustained if optics is supposed to be introduced in short range optical links inside HPCs. The study starts by explaining the main trade-offs when designing optical links and uses rough analytical models to define the range of interesting bit rates.

The transimpedance amplifier (TIA) is the front-end of most optical receiver topologies. In the second part of the chapter a study of different TIA configurations is presented and possible performances of TIAs in different environments are explained. The study is based on extensive transistor level simulations using models from the 65nm bulk and 28nm FDSOI technology. Furthermore, simulation-based

power consumption models are introduced for all components of the link. A significant contribution is the derivation of a relation between the TIAs bandwidth and possible bit rates under the consideration of sensitivity. The third part develops a model to optimize these trade-offs. Finally, the results of the optimization are presented.

The third chapter describes in detail the designed transimpedance amplifier. The optimization of the TIA for a wide average optical input signal acceptance range is explained in detail along with layout considerations. The designed TIA was fabricated and its characterization results are presented to conclude the chapter.

The complete receiver is the subject of the fourth chapter. This work argues for a receiver architecture using time interleaving. Therefore, the TIA is directly followed by a bench of comparators that need to be carefully designed as they dictate the needed output swing of the TIA. The second part of the chapter is therefore devoted to the designed comparators. Comparators need a reference voltage that follows the average optical input signal. A novel threshold control block was invented. It is presented in the third part of the chapter. Afterwards, considerations of the full receiver schematic and the layout are presented as well as simulation results. The final part discusses possible measurement setups, schemes and measurement results.

Silicon photonics enables the possibility to broadcast a common optical clock inside a MCM, due to the precise control of signal delays. The synchronization of all dices inside the MCM would allow higher efficiency for parallel computing. For this reason, chapter five presents novel optical clock receiver concepts. The first concept consists of a self-triggering integrate and dump receiver which is interesting because it can be used to receive signals from pulsed lasers. This elevates the need of optical modulators for the clock channel and hence improves the power efficiency. The second solution to receive pulsed signals is an injection locked oscillators (ILOs). Injection locked oscillators gained a lot of interest over the recent years but pose one major problem: their sensitivity to process, temperature and voltage variations. If ILOs are supposed to be used for highly efficient highly sensitive receivers they must be calibrated. This work presents an ILO based optical clock receiver featuring self calibration.

Chapter 2

State of the Art

“Before all else, be armed.”

Niccolo Machiavelli

2.1 Silicon Photonics

As described in the introduction, the only commercialized products for optical links are those which replace copper cables with optical fibres. The dominant reason is that electric links are well studied and cheap in production. Historically optics was only used for long distance communication which demands highest possible bit rates over a physical channel. To achieve high speeds optical transceivers were assembled with discrete components, each produced in its optimal technology. A speed record was set 2013 with a bit rate of 1 Pb/s [3].

Silicon photonics on the other hand seeks to use the know-how of CMOS production to produce small, power efficient and fast optical systems. This means that silicon photonics is a planar technology based on wafer processing. All steps during the production of silicon photonic systems should be CMOS compatible to enable tight integration between optics and electronics. The tight integration triggers several other advantages. The close connection between optical and electronic components reduces parasitic loadings leading to higher power efficiency and faster systems. Moreover, the lithography based production technology allows producing the systems very cheap and in high volume. The modern silicon photonic design kit integrates all (and even more) components to build optical links and networks, see Fig. 2.1. From the left to the right the image shows a grating coupler, a ring resonator based modulator, a Mach Zehnder interferometer based modulator, a ring resonator based drop filter and a germanium based photodiode. The individual elements will be explained within this chapter. Note that the two types of modulators are only for illustrative reasons inside the same link and would probably not be used together in an actual implementation.

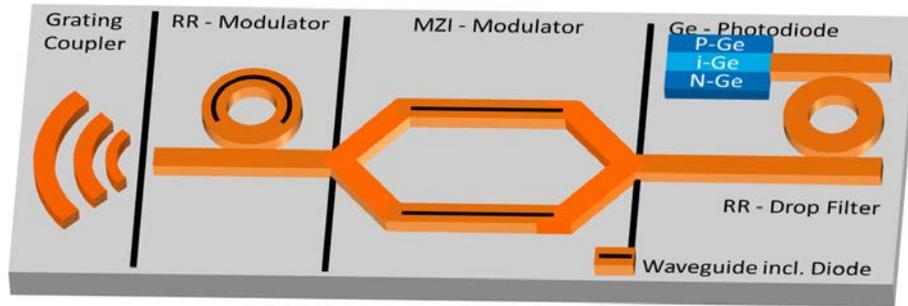


Figure 2.1: Silicon photonic elements that can be used to build an optical link. The elements will be later explained in more detail. RR - Ring Resonator, MZI - Mach Zehnder Interferometer

Waveguides

As the name states, silicon photonics uses silicon as main material. Furthermore, it uses, like fibre optics, the difference of refractive indexes to confine light in waveguides or other structures. The three most important materials and their refractive indices for an optical wavelength of 1550 nm are: silicon $n_{Si} = 3.48$, silicon dioxide $n_{SiO} = 1.44$ and air $n_{air} = 1.0$. As will be discussed later, the design kit based on this key materials has limitations or disadvantages, therefore also other materials are used and studied. Optical fibres based on glass have a minimal absorption at optical wavelength around 1550 nm and 1300 nm. In order to stay compatible with this standard, silicon photonics adopted this wavelength range.

Most silicon photonic designs are based on silicon on insulator (SoI) wafers. They provide a thin layer (sub μm to few μm) of crystalline silicon on a thick layer of silicon dioxide. The refractive index steps air - silicon and silicon - silicon dioxide allows to confine near infra-red light in this layer. To confine the light in a 2D waveguide different structures are used. Fig. 2.2 shows common structures: a) rib b) strip c) buried waveguide.

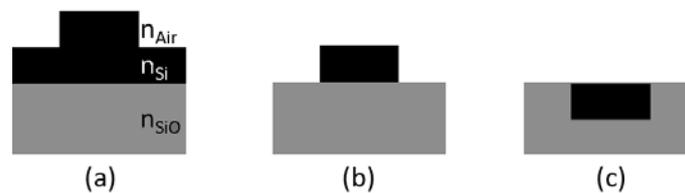


Figure 2.2: Waveguide structures: a) rib b) strip and c) buried waveguide

The different structures have different advantages. Rib and buried waveguides show less losses due to less rough edges, while the light is stronger confined in strip waveguides allowing smaller bending radii. Common width for single mode

waveguides are about 400 nm and bending radii as low as 3 μm were presented [4]. Losses in silicon waveguides can be as small as 0.5 db/cm [5] but common waveguides exhibit losses of 2-3 db/cm. Fig. 2.3.a shows a scanning electron microscope image of a rib waveguide and Fig. 2.3.b an intensity profile corresponding to the light propagation inside such a guide.

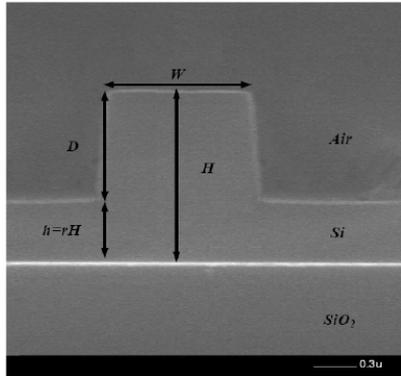


Figure 2.3.a: Scanning Electron Microscope image of a rib waveguide. From [6]

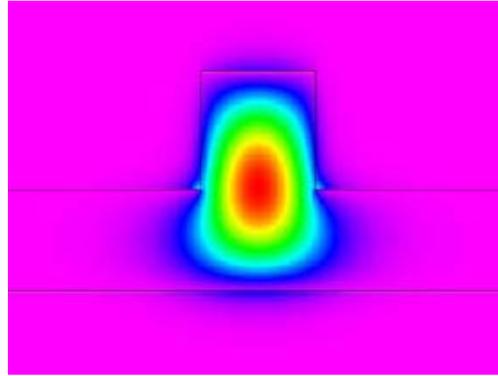


Figure 2.3.b: Light intensity distribution inside rib waveguide

The use of silicon photonics can be motivated directly by the advantages offered from waveguides. A first benefit is the galvanic isolation of chips; this can be helpful for noise sensitive systems or if different chips are running on different supply voltages. The fact that the carrier frequency ($\approx 10^{14}$ Hz) is much higher than the transmitted signal ($\approx 10^{10}$ Hz) has several advantages. The signal experiences only negligible frequency dependent attenuation, which leads to a low distortion of the signal. Although the optical mode is not trapped entirely inside the waveguides the evanescent field around them can be computed and the field strength becomes negligible within a few micro meters. This means that there is no cross talk between closely placed lines, which allows increasing the interconnection density in comparison with copper lines. Finally, ambient light has a very low efficiency in coupling into single mode waveguides, consequently optical waveguides do not pick up noise.

The optical mode travelling inside waveguides is not trapped entirely inside the waveguide but has evanescent tails outside the waveguide core. This can be used in order to couple light from one waveguide into another. Depending on the exact geometry the coupling strength can be tuned from 0 to 100% [6].

Ring Resonators

Although waveguides and power splitters have already advantages over ordinary copper wires, further elements are needed inside an optical link. Most importantly modulators, but switches and filters allow more complex network designs.

If a waveguide is formed as a ring it can act as a filter. It acquires its property by the fact that the light that is travelling inside the ring interferes with itself. In a

configuration as shown in Fig. 2.4 the light can couple from the straight waveguide into the ring resonator but only if the ring's effective optical circumference L_{eff} is an integer multiple N of the light's wavelength λ . The ring's effective optical circumference can be approximated as the ring's geometrical diameter d times π times the refractive index of the ring n_R . Note that n_R does not have the classical simple meaning of a material property but is a function of the waveguide geometry, notably its bending radius. Using this effect different applications can be realized such as a filter, a wavelength dependent coupler or even a modulator.

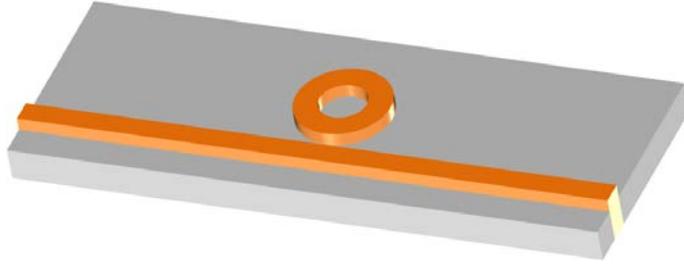


Figure 2.4: A silicon photonic ring resonator coupled to a waveguide

The resonance condition requires only that N is an integer. This means that the ring filters not only one wavelength but a set of wavelengths whose distance in the spectral space is equal to

$$FSR = \Delta\lambda = \frac{\lambda_R^2}{2\pi R n_R}, \quad (2.1)$$

with λ_R being the resonance wavelength. This quantity is called the free spectral range (FSR). Using strip waveguides ring resonators with diameters below $10 \mu\text{m}$ can be fabricated. The corresponding FSRs are in the range of few tens of nano-meters. Filters based on resonance have in common that the decay time of their resonators dictates the full width at half maximum (FWHM) value of their absorption peaks. For ring resonators this can be expressed as:

$$FWHM = \frac{\omega_r}{Q} \quad (2.2)$$

$$Q = \omega_r t N_{Decay}, \quad (2.3)$$

where ω_r is the resonance frequency, t the time of one round trip and N_{Decay} the number of round trips until the signal strength is reduced to $1/e$ of the injected signal strength. Q factors of well designed filters reach values of several hundred thousand, e.g. 740 000 in [7] and 142 000 in [4]. Very narrow FWHMs in the sub nm range follow, turning optical signal processing into a very interesting option.

Just as any micro fabrication process, silicon photonic designs suffer from process variations (PV). High Q factors in combination with PV lead to non-functional systems if they could not be calibrated. Ring resonators show a very high sensitivity

to temperature, as it changes the refractive index of the ring. Therefore, temperature is commonly used to calibrate ring resonators [8]. Although this temperature sensitivity is used to tune the rings, it also poses severe problems, as micro electronic circuitry will be used in direct proximity that consumes a lot of power and heats its surroundings.

If ring resonators are quickly tuned in and out of resonance to the wavelength, they modulate the transmitted light inside the waveguide. Changing the ring's temperature to tune the ring allows its calibration but it is too slow to transmit data at high bit rates. Instead the free carrier concentration inside the waveguide can be used to change its refractive index and therefore its resonance frequency [9]. In order to change the free carrier density inside the ring a diode needs to be placed around the waveguide, see Fig.2.5. There are two possibilities: either placing a p-n junction around the waveguide and deplete the waveguide by a negative voltage or placing a p-i-n junction around the waveguide and injecting free carriers by a positive voltage. Injection mode modulators offer the advantage of lower driving voltages but for the price of lower achievable bandwidth, which is limited by the minority carrier lifetime. The forward bias also results in higher power consumption. The bandwidth of these devices is in the few hundred MHz range [10]. Depletion mode devices on the other hand achieve bandwidth in the range of some tens of GHz (19 GHz are reported in [11]), but need driving voltages that exceed common CMOS supply voltages to obtain good extinction ratios (the ratio between the optical power transmitted when sending a 0 or a 1). E.g. in [12] an extinction ratio of 8 dB is reported for a voltage swing of only 200 mV for an injection mode modulator. On the other hand for a depletion mode modulator in [13] 4 V swing is needed to reach an extinction ratio of 8 dB.

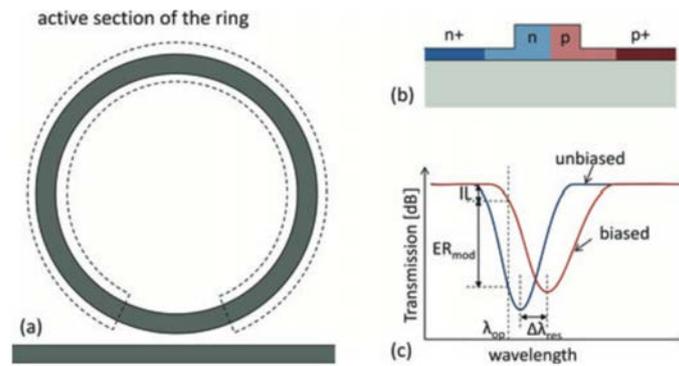


Figure 2.5: Schematic of a silicon photonic ring modulator. (a) Top view: the ring has an active section, where (b) a diode is embedded in the cross section. (c) Change of transmission due to the changed bias. From [4]

Alternative modulator approaches are modulated Mach-Zehnder-Interferometers (MZI) or vertical-cavity surface-emitting lasers (VCSEL). In MZIs a waveguide is

split into two paths, in each path the light travels through a phase modulator and is afterwards recombined in one waveguide, see Fig. 2.1. The benefit of these designs is their temperature insensitivity due to the symmetric design. The disadvantage is that in order to achieve sufficient phase modulation based on carrier injection, MZIs need to be several mm long. The most common approach outside the silicon photonic technology are VCSELs. These laser diodes can be directly modulated, omitting the need of an extra laser source. Furthermore, due to their shape they can be efficiently coupled to fibres and reach very high bandwidth. Bandwidth higher than 20 GHz are reported in [14]. Nevertheless, VCSELs active regions are made out of III-V material such as GaAs or InP and are not compatible with standard CMOS processes.

In this thesis ring resonators will be assumed to be the modulators and drop filters of choice. Due to their small size and possible high bandwidth they fulfill the demands of a high-speed dense-integration platform like multi chip modules.

Grating Couplers

As the silicon laser is still an open research topic and molecular bonded lasers require expensive post processing techniques, the light needs to be injected into the chip from an external laser source. Injecting light poses two problems: mode matching and lifting or injecting the beam in- or outside the chips optical plane. The mode matching problem is the fact that the confined light mode inside a silicon photonic waveguide is much smaller than the mode travelling in single mode fibres, which leads to high coupling losses. The second problem is due to the fact that mass produced optics need to be tested on wafer level. The light must therefore be injected from the top of the wafer. Both issues are addressed by grating couplers. Grating couplers have a structure as shown in Fig. 2.6. In Fig. 2.6.a a top view of a grating coupler is shown. The connected waveguide on the left side directs the light to the grating structure on the right side, where the light diffracts and leaves the plane. The asymmetric cross section of the grating, shown in b), causes the light field to be scattered dominantly into one direction where it can be coupled into a fibre. Grating coupler can have coupling efficiencies up to 75 % [15].

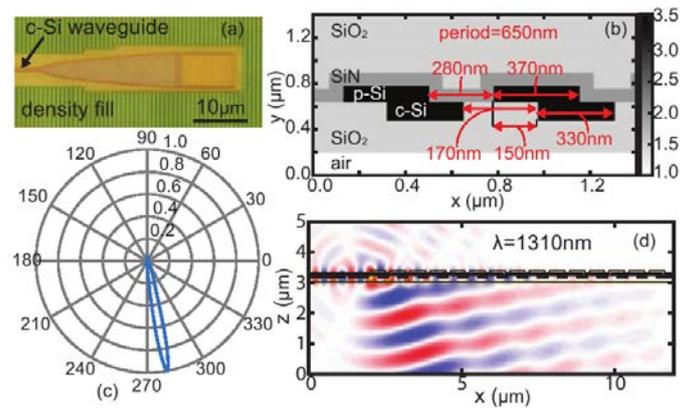


Figure 2.6: (a) Microscope image of a grating from the bottom surface of the chip. (b) Index profile of an optimized grating. (c) Angular power distribution and (d) corresponding simulation showing high directionality. [15]

Light Detectors

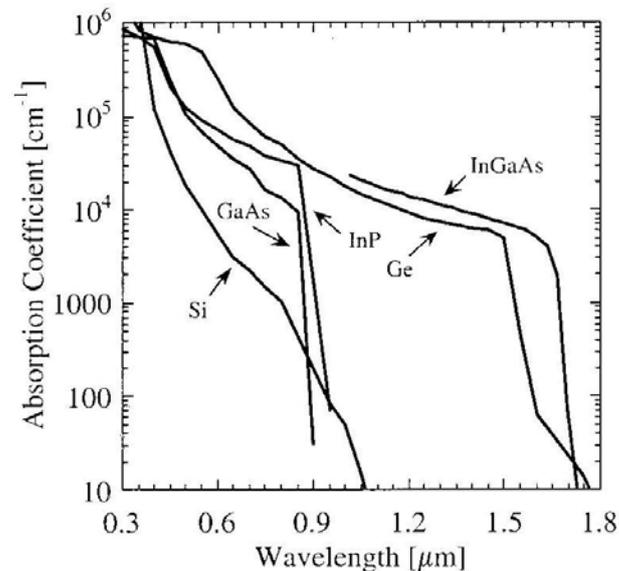


Figure 2.7: Absorption coefficients for different semiconducting materials. Taken from [16]

As the wavelength was chosen for minimal absorption in the silicon waveguides, silicon can not act as an efficient photo detector. Germanium (Ge) is a material compatible with the CMOS fabrication process, still showing absorption in the near-infrared, see Fig. 2.7. Highly sensitive diodes can be designed by implanting Ge

in the silicon substrate, forming a P-I-N diode in it. For a high coupling efficiency the waveguide can stop right at the Ge implant's facet. An important parameter of photodetectors is their responsivity (R) which describes the detection efficiency in terms of generated current divided by injected optical power. This value obviously depends on the operation wavelength, as two devices can have equal quantum efficiencies (efficiency expressed as fraction of photon converted to electrons), but different responsivities due to different operation wavelength. For the near-infrared responsivities of around 1 A/W were reported for germanium photodiodes [17]. The P-I-N diodes can be negatively biased which reinforces the internal electric field and helps to sweep and collect the light generated carriers. This reduces the parasitic capacitance of these devices and increases therefore their intrinsic bandwidth. In [18] a bandwidth of 40 GHz is presented. It is interesting to notice that the biasing does not influence the responsivity of the diodes. This opens up applications (for example in oscillators) in which the biasing undergoes strong and fast variations.

Finally, Fig. 2.8 shows a cross section of a silicon photonic front-end including a ring modulator, a heater, a photodiode and passive structures.

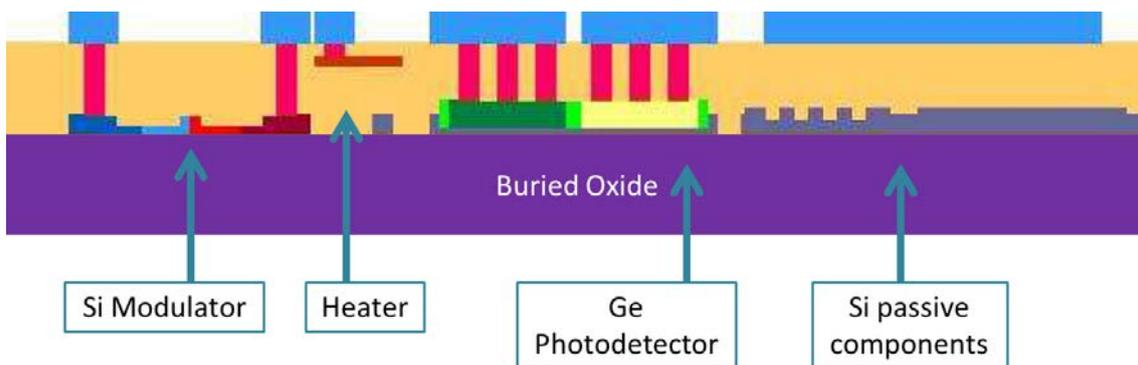


Figure 2.8: Cross section of a silicon photonic front-end

2.2 Link Architectures

The described components and corresponding electric circuitry allow to build an optical link. A basic link comprises a laser source, a coupler, a modulator and a photo detector, compare Fig. 2.1. Such a point-to-point link might serve to transfer data quickly from one node to another but as already mentioned in the introduction a single channel won't be sufficient for the needs of future processor to memory links. To densify the data stream several wavelengths are coupled into the link and several modulators, each tuned to a separate wavelength, are used to send data over different channels in the same waveguide. On the receiver side several drop filters can be used to pick up a wavelength and direct it to a channel dedicated photodiode.

In this fashion not only direct links such as processor to memory connection can be realized but also optical networks on chip (ONoC). High-density, high-speed

networks can be realized by for example using the Corona architecture [19]. In this architecture one waveguide bus is laid out in a ring topology, see Fig. 2.9, to omit waveguide crossings which would introduce too high losses. Inside this ring each node has dedicated waveguides. The only connected receivers are from the waveguide's master node, all other nodes can write on these waveguides. This multiple-writer single-reader structure allows communication between all nodes without using complex and lossy routers. Challenges arising from this architectures are the optical losses due to passing several ring resonators, the power variations due to different writers and the need of fast wake-up times of the receiver from a moment no data was transmitted.

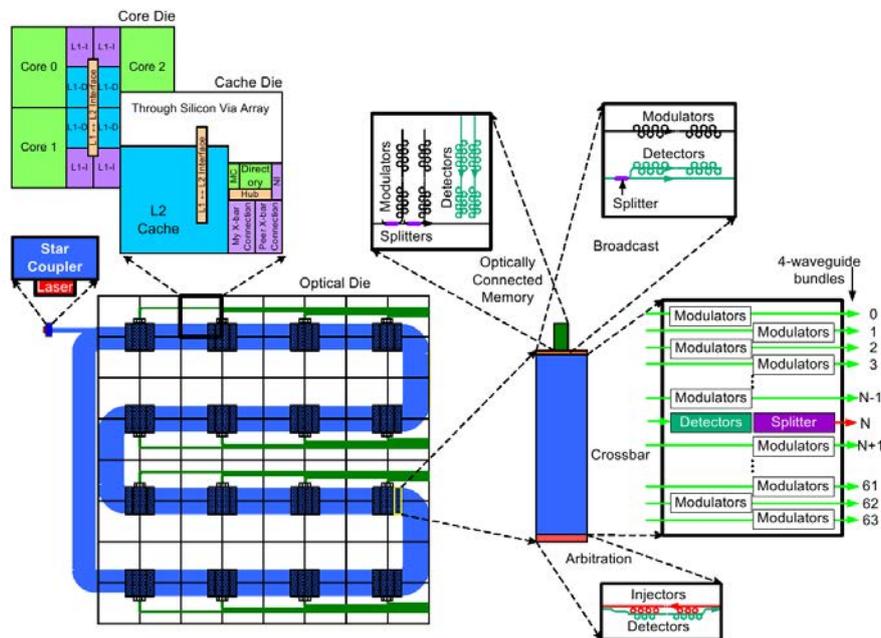


Figure 2.9: Optical Network on Chip Architecture proposed in [19]

Writer depending signal strength arises from a different tuning of each ring resonator. This leads to different average signal strengths at the receiver input depending on which writer originated the signal. Depending on the receiver circuitry this might lead to changes in its biasing and to its failure. The time needed to react to changed biasing conditions dictates also the wake-up time of the receiver. Usually, prespecified data headers precede useful data for adjusting the receiver bias. Long wake-up times are not acceptable as they lead to long data overheads. Therefore, these two points need to be considered when designing circuitry for these systems.

Other architectures such as Chameleon [20] argue for a higher flexibility of the waveguide occupation. In this case, each node is equipped with the same set of wavelength to emit into a waveguide and the same set of drop filters to read from the waveguide, see Fig. 2.10. An arbitration algorithm decides which node can

establish its communication to its target. These multiple-writer multiple-reader links add the challenge to the receiver that the signal strength will also depend on the receiver node. This is a static problem and can be solved by node dependent receiver design but a receiver being suitable for the entire signal strength range would ease the design of the system.

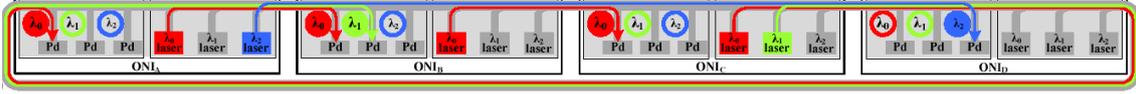


Figure 2.10: The Chameleon architecture proposed in [20]

Corona and Chameleon are passive optical networks as the light does not have to be routed. Due to the amount of ring resonator that the signal has to traverse they are limited in the possible number of nodes. Systems with active routing employing a two dimensional grid such as the Cygnus router [21] can reduce the number of passed ring resonators but need them as active routers, see Fig. 2.11. This adds complexity to the calibration schemes of the ring resonators. The signal strength variations at the receiver side would also increase.

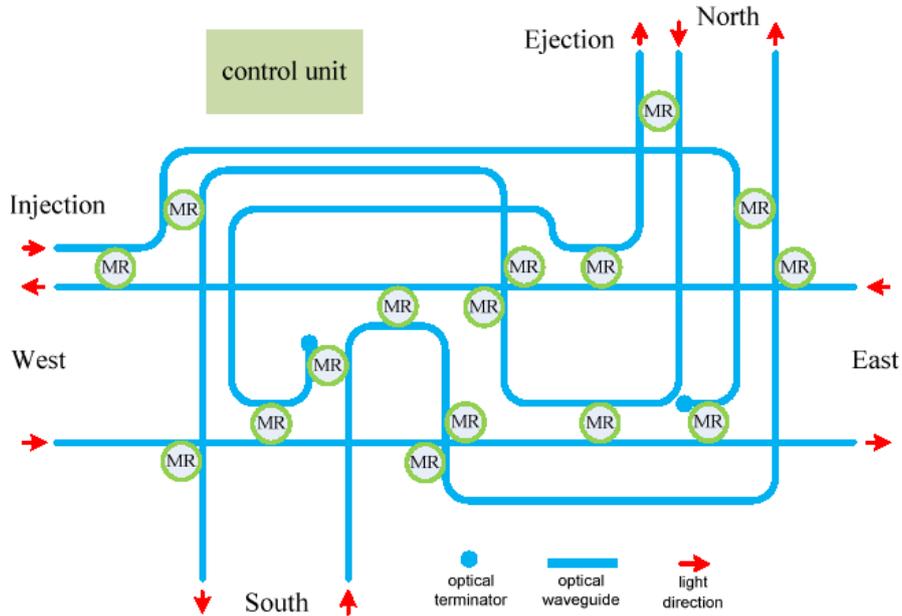


Figure 2.11: The Cygnus router proposed in [21]

A possibility to use an optical grid without routing is the introduction of two optical layers; one layer carrying waveguides that run east-west and another layer carrying north-south waveguides. Oracle's macrochip concept [22] envisioned such

a system using direct passive coupling between these two layers, see Fig. 2.12. The increasing amount of complexity and routing leads to flexibility and higher theoretical performance. However, [23] states, that under consideration of optical losses and the limitation of optical power, switched networks outperform point-to-point networks only when optical losses of switches and inter-layer coupler losses drop below 0.75 dB. These low loss devices have yet to be fabricated.

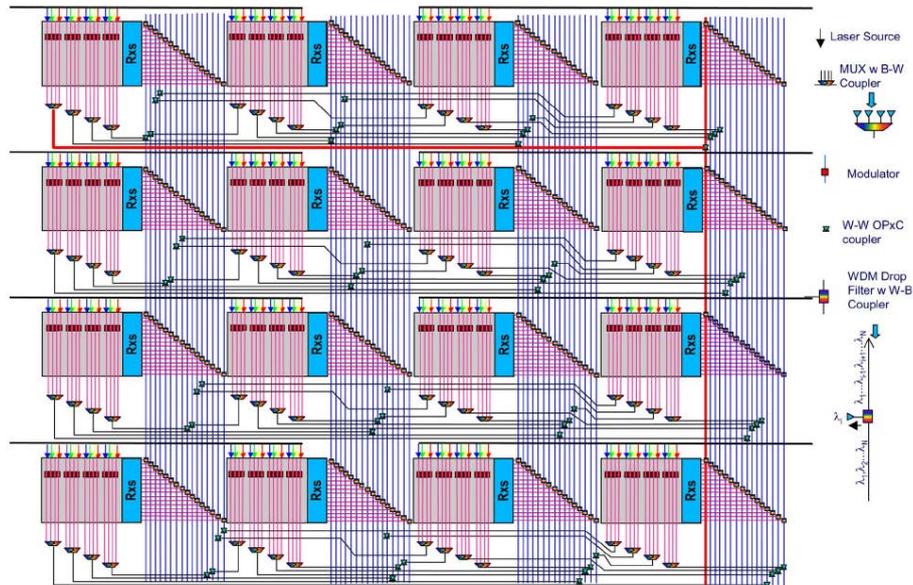


Figure 2.12: The optical grid based Macrochip architecture proposed in [22]

2.3 Assembling Technology

Independently from the network architecture a major question is whether to integrate optics and electronics on the same substrate or not. The advantage of integration would be the low packing-complexity and the big reduction of parasitic capacitance due to short connections between the optical and electronic devices. These two advantages can make this idea appealing for cable replacement approaches as successively commercialized by Luxtera [24], see Fig. 2.13. However, in this case silicon photonics has to outperform classic methods based on VCSELs, as in the cable replacement market the reduction of footprint is not the dominant constraint. As VCSELs and silicon photonic devices show comparable bandwidth, this superiority has to be provided by more complex data encoding systems such as pulse-amplitude modulation (PAM) [25].

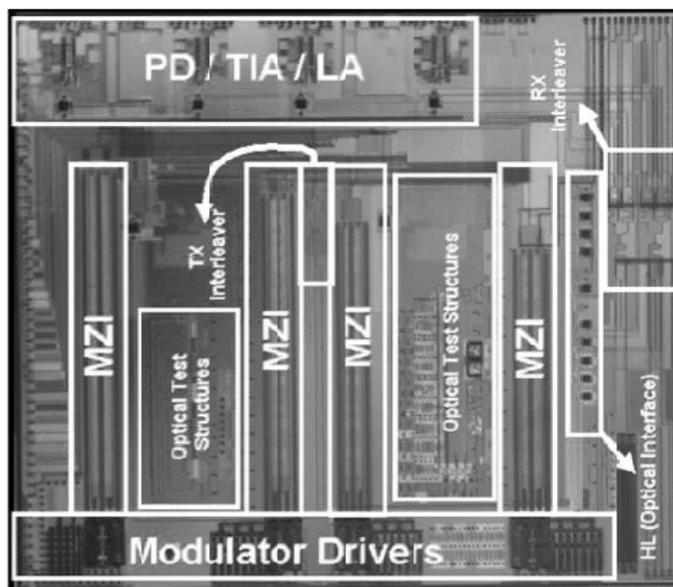


Figure 2.13: Monolithic integration approach followed by Luxtera for high speed cable replacement purposes [26]

An alternative approach foresees electronics and optics on separated and dedicated dices. This approach is certainly applied in the realm of multiple chip modules. Real estate in modern deep-submicron technology nodes is too expensive to dedicate $500 \mu\text{m}^2$ just for an optical coupler. Apart from the reduced cost effectiveness other problems exist as well. First of all the majority of processing nodes is still fabricated in a bulk technology and not in a SOI technology. Furthermore, SOI wafers for electronics are fabricated with a very thin isolation layer for maximal heat transport, down to 50 nm, which does not allow to confine the light in the waveguides.

The disadvantage of the stacking approach are the increased parasitic capacitances. The classic approach is the wire bonding of the two chips. This introduces indeed high parasitic capacitances (several tens of fF), and increases the packaging process complexity. Nevertheless, advances in the 3D integration of chips introduced copper pillars, Fig. 2.14.a, as a possibility to connect two chips face to face, see Fig. 2.14.b.

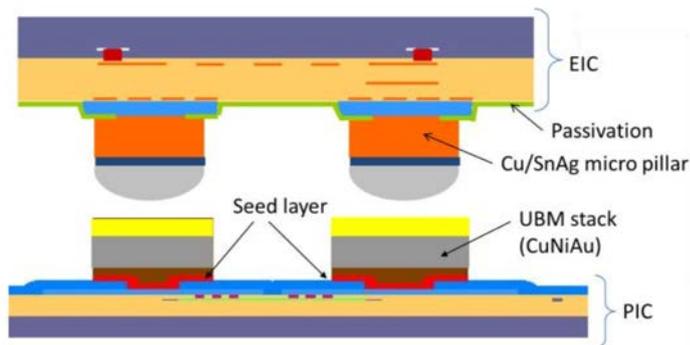


Figure 2.14.a: Layer stack used for Cu-Pillars. Here, the electric integrated circuit (EIC) is flip-chipped onto the photonic integrated circuit (PIC).

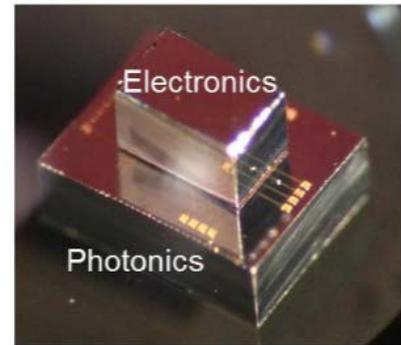


Figure 2.14.b: Photography¹ of a EIC - OIC stack

This technique requires the two chips to have matching pads on their faces. On the pads of one chip copper is deposited, afterwards it is flipped (therefore these techniques are also called flip chipping) and placed on top of the other chip. Finally the chips are connected by reflowing the copper. This technique allows tight integration and high interconnect density as the pillars can have pitches below $40 \mu\text{m}$. The introduced parasitic capacitances are still not negligible, but they can be as low as 3 fF according to CEA internal measurements.

2.4 Circuitry for Optical Links

Drivers

Many types of silicon photonic modulators need driving voltages bigger than $2 V_{PP}$ in order to generate an optical signal with sufficient extinction ratio. Modern technology nodes have very thin gate oxides, leading to low supported V_{DD} voltages around 1 V. Therefore, a digital buffer consisting of a chain of digital inverters with increasing fan outs is not sufficient. Drivers for depletion mode modulators are commonly build by a double rail buffer structure, meaning that the digital input signal is split into one buffer operating between ground and V_{DD} , and a second buffer operating between V_{DD} and $2V_{DD}$. Their signals are then recombined at the output to achieve high signal swings at the modulator input [27], see Fig. 2.15.a. Realizations with different output voltage swings and their power consumptions are presented in table 2.15.b.

¹Credits: California Institute of Technology

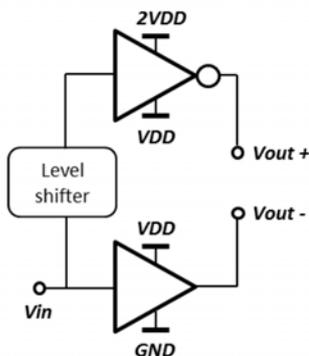


Figure 2.15.a: Basic schematic of a double rail ring resonator driver

Reference	Swing	Bit rate	Consumption
[28]	2.4 V	10 Gbps	537 fJ/b
[29]	2.0 V	10 Gbps	135 fJ/b
[30]	1.5 V	10 Gbps	350 fJ/b
[13]	4.4 V	25 Gbps	2.48 pJ/b

Figure 2.15.b: Reported drivers for different output voltage swing and their energy efficiencies

Injection mode modulators on the other hand have bandwidth below 1 GHz. In order to run high bit rates through them the signal needs to be pre-emphasized. This means that the drop of the high frequency part of the signal is anticipated and amplified beforehand in the driver, so called feed forward equilibration (FFE). Fig. 2.16 shows a solution presented in [13]. In the case of rising edge, the Tap0 signal generates a short high voltage signal which is then reduced to the signal generated by Tap1.

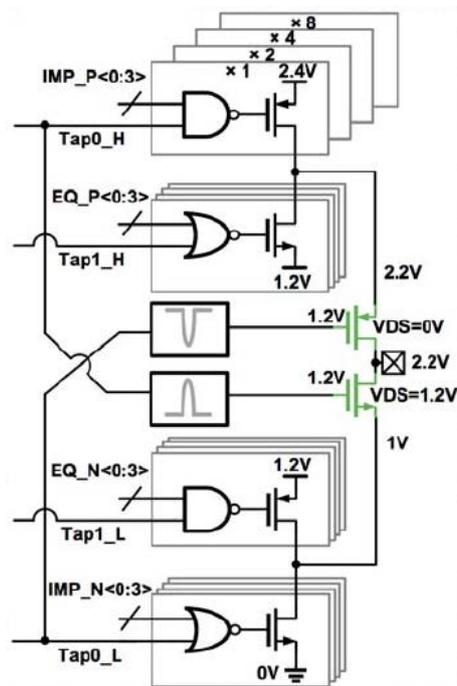


Figure 2.16: Ring driver with feed forward equilibration. From [13]

The VCSEL driver in [31] proves the capability of VCSELs to provide a PAM

modulated signal. A PAM 4 VCSEL driver is presented including 2 Tap FFE at 10 Gbps achieving an energy efficiency of 4.7 pJ/b, including the power of the VCSEL, which is missing in all other mentioned transmitters.

The diodes in MZI arms can be split corresponding to phase shift steps needed for different PAM encodings. In Fig. 2.17 splittings for a thermometer code and a binary code are illustrated. This allows direct conversion from a digital to a PAM encoded signal. In [32] a PAM 4 driver running at 20 Gbps is reported with an energy efficiency of 290 fJ/b.

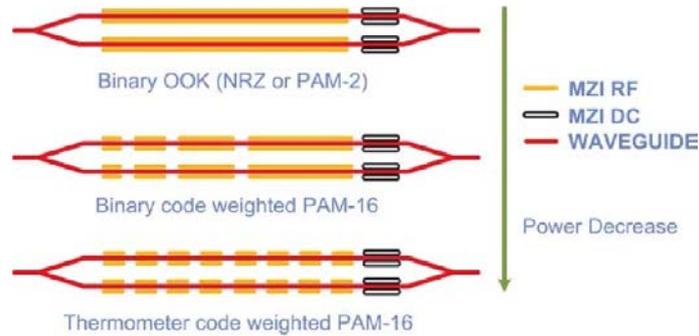


Figure 2.17: An MZI allows splitting the diodes of the MZI and by that inherent conversion from a digital code to a PAM code. From [32]

Receivers

Photo detectors such as photodiodes convert the detected photons to a charge that is injected into the electrical front-end. As the signal is encoded in the intensity of the light illuminating the detector, the signal is converted into a varying current signal. The purpose of the receiver is to translate the small currents into the voltage domain. Depending on the link either a linear amplification, for example for coherent transmission systems, or a non-linear amplifications into the digital domain is needed.

The simplest possibility is to run the generated current through a resistor R . The voltage drop over the resistor corresponds to the converted signal. The limitation of this approach arises from the parasitic capacitance C_{PD} of the photodiode, as the bandwidth of this circuit is limited to $1/(R \cdot C_{PD})$, while the signal swing $\Delta V = R \cdot I_{In}$. This trade-off could be broken by a following voltage amplifier. Nevertheless, the input noise power is fixed to kT/C_{PD} , stemming from the thermal voltage noise power density $4kTR$ of the resistor, integrated from 0 to $1/(R \cdot C_{PD})$, the system's bandwidth. This means that there is a trade-off to be made between the signal to noise ratio (SNR) and the bandwidth of the front-end.

Transimpedance Amplifier

A possibility to break the above mentioned trade-off between sensitivity and bandwidth, is the introduction of active components. The most common solution is the transimpedance amplifier (TIA). A TIA is obtained by shunting a voltage amplifier with an impedance Z_F . In many cases Z_F is a simple resistor R_F , compare Fig. 2.18.

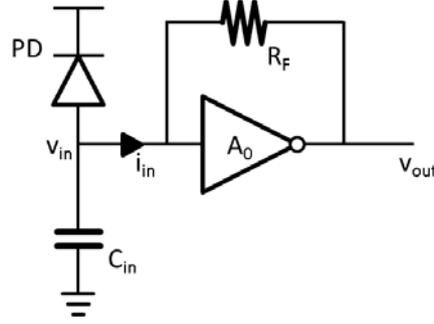


Figure 2.18: Basic schematic of a TIA

The transfer function of this system is readily derived: the input current splits into

$$i_{in} = i_R + i_C, \quad (2.4)$$

where i_R is the current passing through the feedback resistor and i_C is the current sinking in the input capacitance of the system. The voltage at the input node of the voltage amplifier is therefore

$$v_{in} = \frac{i_C}{j\omega C_{in}}. \quad (2.5)$$

For an ideal voltage amplifier follows

$$v_{out} = -v_{in}A_0, \quad (2.6)$$

but due to the feedback resistor also

$$v_{in} - v_{out} = i_R R_F \quad (2.7)$$

has to hold. Solving this linear system of equations, we obtain the transfer function H:

$$H = \frac{v_{out}}{i_{in}} = \frac{-A_0}{A_0 + 1} \frac{R_F}{1 + j\omega C_T \frac{R_F}{A_0 + 1}}. \quad (2.8)$$

The transimpedance stays for large A_0 's approximately R_F , while the bandwidth of the systems becomes

$$f_{BW} = \frac{A_0 + 1}{2\pi R_F C_T}. \quad (2.9)$$

Hence the benefit of bandwidth overcompensates the small loss in transimpedance, which would lead to the SNR reduction, and brakes the trade-off. The concept of TIAs does not specify which kind of voltage amplifier should be used, therefore many realizations have been demonstrated.

In [29] a TIA realized by a common push-pull inverter is presented. It is followed by a further push-pull inverter that acts as a g_m stage and a final push-pull inverter. This structure was fabricated in a 40 nm CMOS process loaded with an input capacitance of 50 fF. The authors obtained a bandwidth of 7 GHz and a transimpedance of 4 k Ω . This front-end is followed by two parallel clocked comparators for the final conversion from the analog to the digital domain, the so called decision stage, see Fig. 2.19. The parallelization of clocked comparators is interesting as it allows to halve the working speed of each comparator as they compare alternately the received bits. This technique is called time interleaving. The entire receiver achieves an energy efficiency of 395 fJ/b.

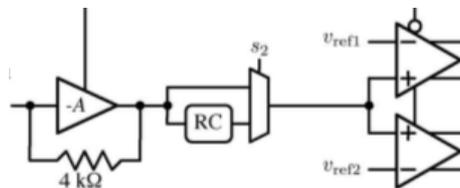


Figure 2.19: The connection of the TIA to a bench of parallel comparators allows to reduce the working speed of each comparator to the expense of higher loading of the TIA. From [29]

A possible variation is the introduction of a pair of cascode transistors inside the inverter [33], see Fig. 2.20. The presented design in 40nm CMOS achieves 8 GHz bandwidth and a gain of 500 Ω at an energy efficiency of 1.92 pJ/b, mainly due to the high input loading of 450 fF.

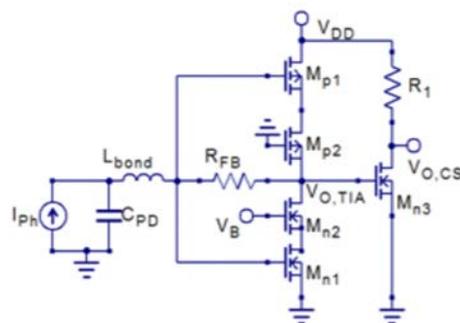


Figure 2.20: If the voltage headroom is sufficient, cascode transistors can be used to extend the bandwidth of TIAs. From [33]

To extend the bandwidth of a TIA inductive peaking can be applied. Inductive

peaking is based on the introduction of an inductor in the circuitry (for example in the feedback path) so that the higher frequencies are stronger amplified, see Fig. 2.21. Using this technique, [34] presents a TIA showing a bandwidth of 21 GHz and a transimpedance of 100Ω , in a 65nm technology node at one input capacitance of 80 fF. The use of inductors makes the footprint of this approach very big and therefore not usable for multi chip modules. Furthermore, the wide bandwidth integrates a lot of noise while the low impedance generates not enough signal for a good SNR. This paper states therefore a sensitivity of -10 dBm. The reported energy efficiency of the isolated TIA is 650 fJ/b.

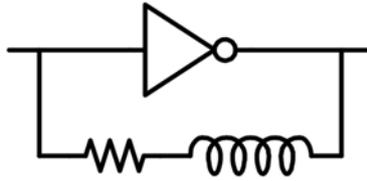


Figure 2.21: TIA with resistive and inductive feedback for bandwidth extension. From [34]

To overcome the two drawbacks of inductive peaking, namely large footprint and high noise integration, [35] proposes to use a TIA running at 11 GHz and continuous-time linear equilibration (CTLE). The lower bandwidth reduces the noise integration. The CTLE is performed in a second stage, shown in Fig. 2.22. In this stage the resistive impedance of the differential stage introduces a zero in its transfer function that leads to a peaking behaviour, this technique omits the use of inductors and therefore reduces the footprint. The presented receiver features furthermore a calibration technique for the CTLE by monitoring the eye opening with a dedicated comparator. The receiver channel runs at 24 Gbps with an energy efficiency of 560 fJ/b. It achieves a sensitivity of -7.9 dBm connected to a photodiode with a responsivity of only 0.45 A/W. The paper proposes furthermore a clock channel receiver based on a TIA followed by a LC-tank injection locked oscillator, this channel runs at 12 GHz and consumes 14 mW.

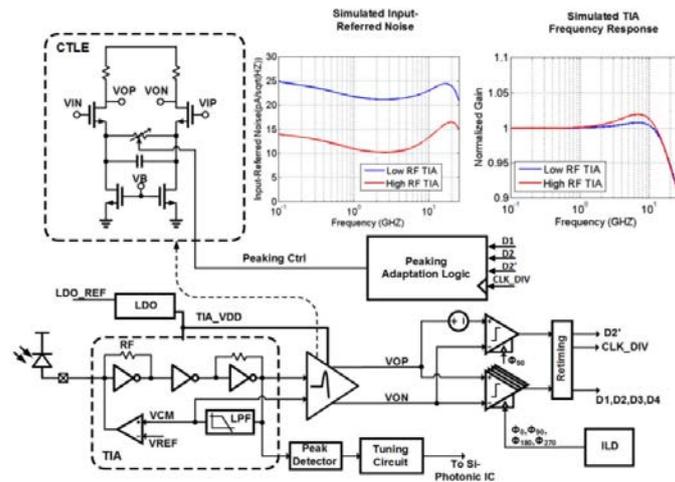


Figure 2.22: TIA with resistive and inductive feedback for bandwidth extension. From [35]

Another mean to extend the bandwidth is the introduction of decision feedback equilibration (DFE). DFE uses the history of transmitted bits to correct the received signal of a front-end with a too low bandwidth. Intuitively spoken, a slow TIA receiving a 1 will not be able to increase the output voltage sufficiently over the threshold voltage if it received a 0 before. To counteract the DFE will support the raise of the TIA's output voltage due to the previously received 0. Find a possible implementation in Fig. 2.23. In [36] a DFE system provides 9 Gbps output although the used TIA has only a bandwidth of 1.5 GHz. The complete receiver achieves an energy efficiency of 0.93 pJ/b. The digital aspect of this technique allows very high sensitivities (-25 dBm in [37]) because the low bandwidth of the TIA integrates only very few noise.

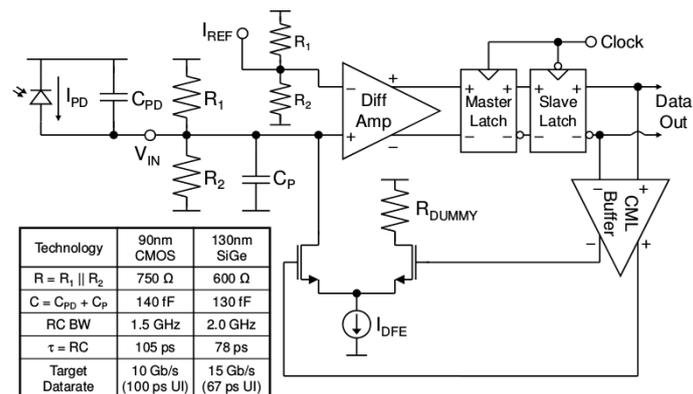


Figure 2.23: A receiver including decision feedback equilibration. From [36]

In the discussion of ONoCs the problem of quickly changing optical input power levels was introduced. In [38] a burst-mode receiver is presented, that calibrates

the TIA and the clock-data-recovery (CDR) mechanism within 31 ns. The receiver features three dedicated feedback loops working sequentially, see Fig. 2.24. The first feedback loop sets the current sink at the TIA input, so that the DC part of the input current is subtracted. Afterwards, the second feedback loop searches the edges of the data input stream, which needs to be 101010 during the calibration. The found parameters are then sent to a continuously turning CDR. The presented receiver runs at a bit rate of 25 Gbps with an overall energy efficiency of 4.4 pJ/b at run time. The system was tested using a diode with a responsivity of 0.5 A/W and achieved a sensitivity of 10.9 dBm.

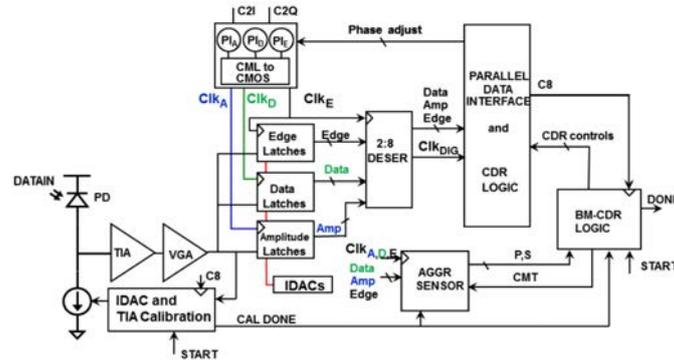


Figure 2.24: A burst mode receiver featuring dedicated control loops for DC current subtraction and CDR. From [38]

Integrating Front-Ends

If the photodiode is connected without a static DC path to ground, the front-end is integrating the charge generated by the photodiode. A broader understanding of integrating front-ends also includes TIA or resistive front-ends if their bandwidth is several times smaller than the transmitted data rate. Depending on the architecture it can either be speculated that there is an equality of the amount of 1s and 0s, accepting the drifts of the DC part of the signal, or the input node needs to be periodically reset, see Fig. 2.25. The latter approach is called integrate and dump receiver, as proposed in [39].

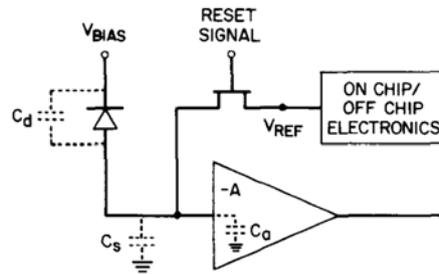


Figure 2.25: Receiver based on the integration of the current signal onto the input capacitance of the following stage. From [39]

A differential system based on the integration principle is presented in [40]. The two ports of the photodiode are connected to the two inputs of a clocked sense amplifier and a pair of tunable capacitors as well as constantly discharging current sources, see Fig. 2.26. The receiver is fabricated in a 45nm SOI CMOS process and monolithically integrates the photodiode. The receiver achieves a bit rate of 3.5 Gbps at a sensitivity of -19 dBm. This receiver achieves a very high energy efficiency of 50 fJ/b.

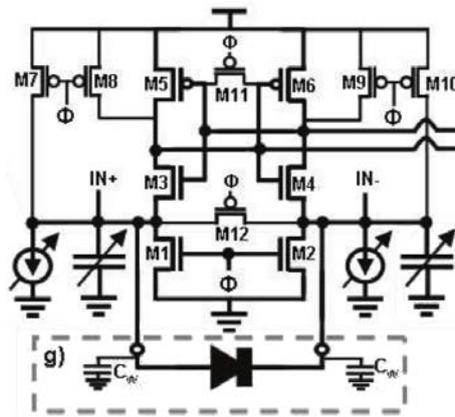


Figure 2.26: Electro-optical front-end based on integration. The photodiode is directly connected to a sense amplifier. From [40]

The benefits of combining an integrating front-end with time-interleaving are demonstrated in [41]. The circuit generates a 1 bit derivative of the signal by comparing successively taken samples of the signal, see Fig. 2.27. Therefore, after the integrating front-end a two channel sample-hold circuit follows, taking the samples. The samples are depending on their common mode amplified and then compared in a sense-amplifier. The receiver, fabricated in a 28 nm technology node, achieved bit rates of 25 Gbps. The measured sensitivity is -6.8 dBm, using a photodiode with a responsivity of 0.8 A/W. The receiver shows an energy efficiency of 170 fJ/b.

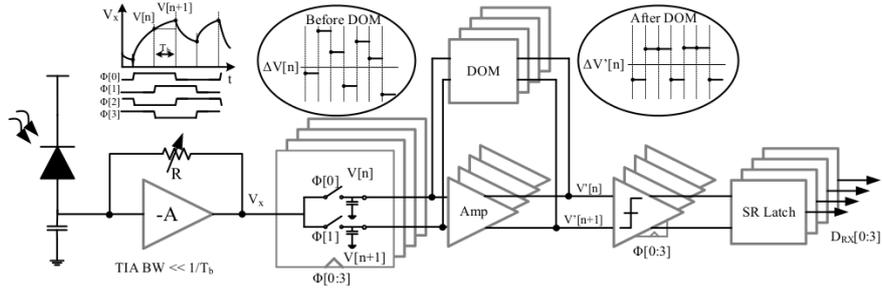


Figure 2.27: Receiver integrating the data stream with a slow front-end and performing the decision making by comparison of successively taken samples. From [41]

2.5 Full Link Demonstrations

A transceiver, a module that comprises a transmitter and a receiver, circuit is presented in [12]. Fig. 2.28.a illustrates the heterogeneous approach in which the transceiver circuitry is placed on a separate chip next to the CPU or the memory. This solution allows the heavy use of inductors for bandwidth extension. The described receiver uses an inductively peaked regulated cascode inverter followed by a series of 6 inductively peaked differential amplifiers. The receiver consumes 2 pJ/bit running at 25 Gbps and has a sensitivity of -8.0 dBm. The driver incorporates FFE as the transceiver uses injection mode ring modulators. The driver consumes 2.9 pJ/b. The entire system consumes 4.9 pJ/b but neither the thermal control is integrated in this system nor is the needed laser power included in the power budget.

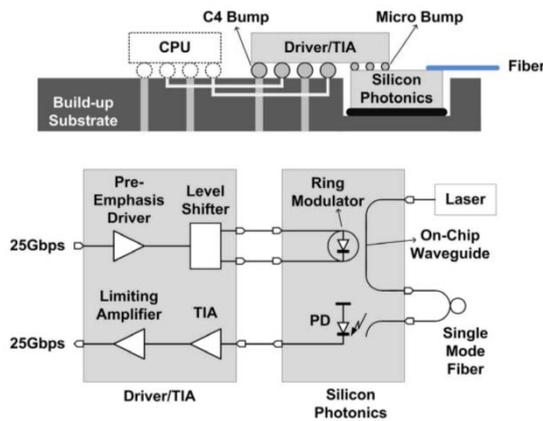


Figure 2.28.a: Schematic of a heterogeneous approach where the communication circuitry is placed on a separate chip. From [12]

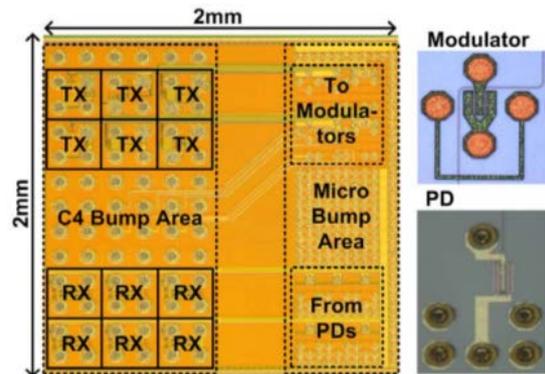


Figure 2.28.b: Picture of the transceiver circuitry presented in [12]

[42] demonstrated 2012 a full silicon photonic link using depletion ring modu-

lators, see Fig. 2.29. The single channel link runs at 10 Gbps and achieves a bit efficiency of 2.1 pJ per bit. The power consumption comprises all consumers including optical input power, except the wall-plug efficiency of the light source. The energy splits into 14 mW optical power and only 7 mW for the circuitry. The optical power strongly dominates therefore the power consumption. The design foresees the transmitter and the receiver on two different hybrid modules which are coupled to a fibre using optical couplers, introducing 15.5 dB of a total of 24.5 dB loss. If this design was used on a single optical interposer, it would be much more efficient. The group used a 65nm technology for the circuitry and a 130nm SOI technology for the optical interposer.

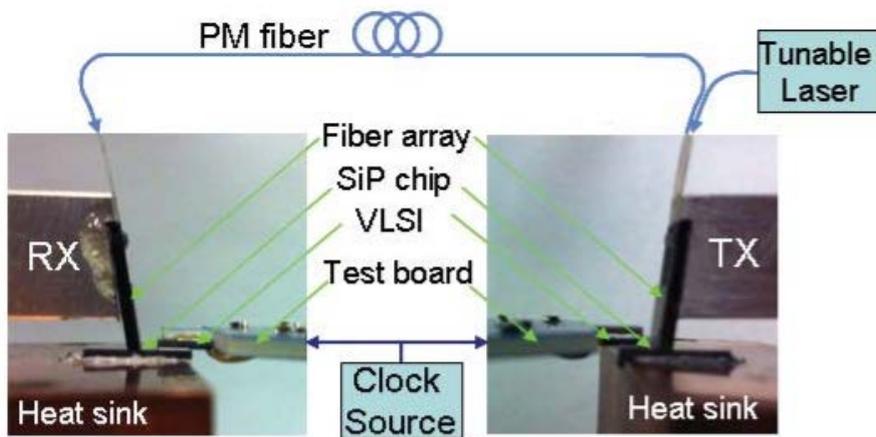


Figure 2.29: Complete optical link using heterogeneous technologies. From [42]

A full optical link including wavelength division multiplexing is reported in [43]. The heterogeneous transceiver includes 4 WDM channels. Instead of using a single ring oscillator as drop filter, a double ring structure is proposed for sharper filtering. The design foresees furthermore only a single heater for the entire drop filter bench, see Fig. 2.30.a. The system runs at 20 Gbps per channel. The transmitter including thermal control of the ring resonators consumes 1.6 pJ/bit/channel, excluding the serialization stage. The receiver is based on a seven stage TIA - G_M chain but misses the decision stage as well as the deserialization. It consumes 730 pJ/b/channel at a sensitivity of -7.2 dBm. The full system consumes therefore 2.3 pJ/b, not counting the needed laser power.

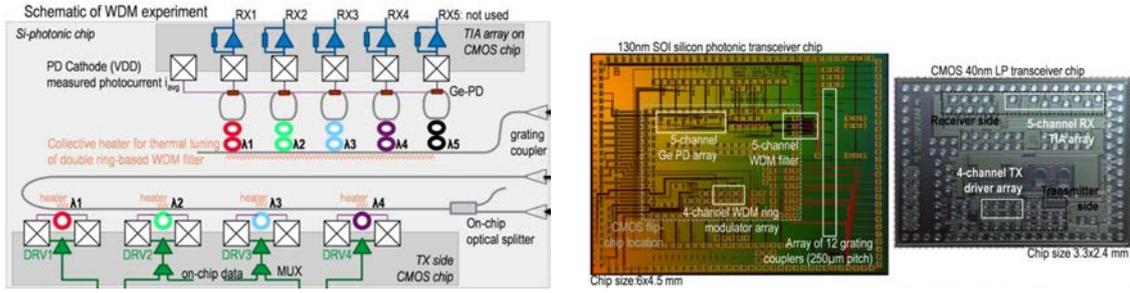


Figure 2.30.a: Schematic of IMECs heterogenous transceiver featuring 4 channel WDM with double rings as drop filters. From [43]

Figure 2.30.b: Picture of the optical interposer and the electronic IC of the transceiver presented in [43]

It is also possible to integrate silicon photonics in a bulk technology process, proven by [44]. A link based on a monolithically integrated transceiver is presented, see Fig. 2.31. The transceiver is as in [42] coupled to another transceiver using a fibre. The link operates 9 channels summing up to a bit rate of 45 Gbps. It consumes 3 pJ/b electrical power and 12 pJ/b optical power. The group uses a 180 nm CMOS bulk technology for chips including optics and electronics.

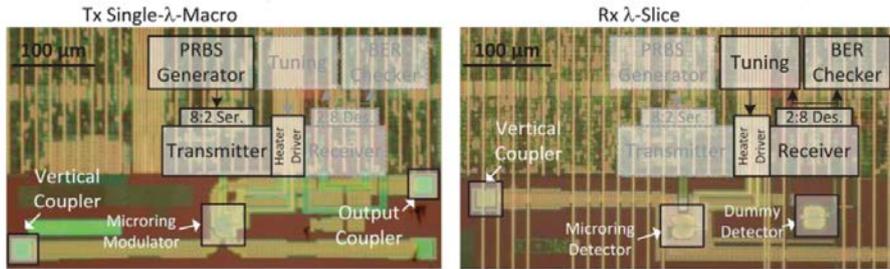


Figure 2.31: Monolithically produced transceiver from [44]

This concludes the presentation of the state of the art. The following optimization chapter introduces the theoretical study conducted to evaluate the optimal bit rate of optical links. The optimization is motivated by the energy efficiency dependence on the bit rate of state of the art optical links shown in Fig. 2.32.

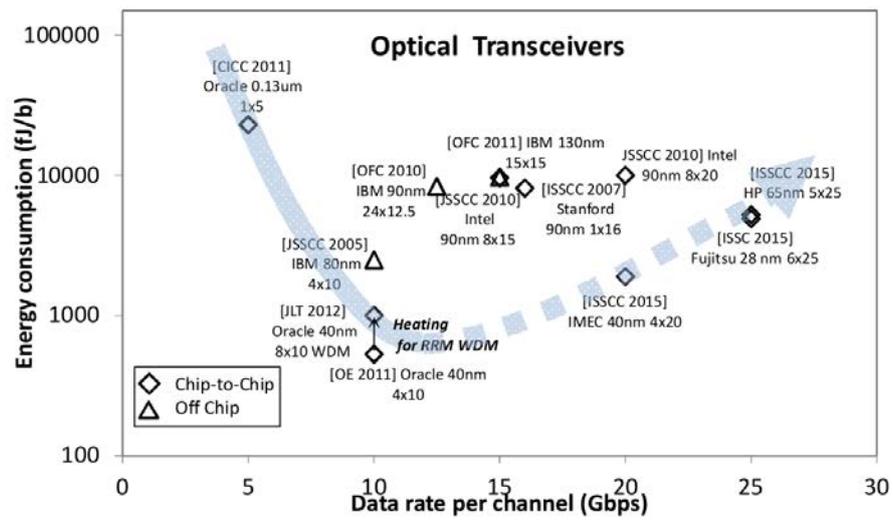


Figure 2.32: Energy efficiency as a function of data-rate for state of the art chip-to-chip and off-chip and optical links

Chapter 3

Optimization of Silicon Photonic Links

“There is nothing more difficult to take in hand, more perilous to conduct, or more uncertain in its success, than to take the lead in the introduction of a new order of things.”

Niccolo Machiavelli

The first step in the design of complex systems is an architecture study. The conducted optimization is split in three parts:

1. The first part explores the parameter space based on general considerations and a literature study.
2. The TIA defines most link parameters, hence the second part studies in detail TIA topologies.
3. The third part examines the entire link based on a TIA database and analytical models for all other elements of the link. It investigates the optimal bit rate for minimal energy consumption, with a focus on the relation of the TIA's bandwidth and the links bit rate.

3.1 Introduction

For this work a link as shown in Fig. 3.1 is considered. The point to point link consists of a serialization stage, a laser, an optical modulator, a modulator driver and a temperature control, a photodiode, a transimpedance amplifier, a decision stage and a deserialization stage.

It is assumed that an external laser is continuously emitting light into the link's waveguide through a grating coupler. The light intensity is then modulated by a ring modulator. Such devices do not consume power but need to be driven electrically and their temperature needs to be controlled. As the most energy efficient bit rate lies probably higher than 1-3 Gbps (the clocking frequency range of modern processing units) the driver needs to be preceded by a serialization stage to connect the processing units to the link, running at its optimal bit rate. The waveguide is injecting the light directly into a photodiode that converts the light intensity to a current. The photodiode is followed by the TIA that converts the current into voltage and injects the signal into the final decision and deserialization stages. There are several approaches on how to realize decision stages and deserialization stages. Many of these integrate both stages into a single block, hence the decision - deserialization function is considered as a single block for the moment.

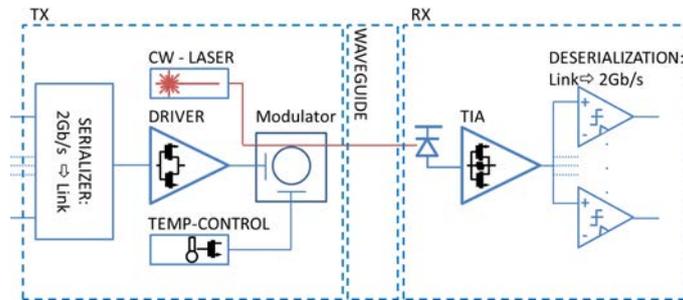


Figure 3.1: Block scheme of the optical point-to-point link

Typical values taken from recent publications for the power consumptions of the above described stages are:

Element	Consumed Power	References
Serialization ¹	1.5 mW	
Laser ²	30 mW	[27, 29, 43]
Driver	3 mW	[28–30]
Temperature Control	6 mW	[43]
TIA	2 mW	[33, 34, 45]
Decision + Deserialization ³	1 mW	[46, 47]

These data show that the two most dominant power consumers inside an electro-optical link are the laser and the temperature control circuitry of ring modulators. These two consumers also define the most important trade-off in these designs: bit

¹Approximated by gate consumptions taken from a 65nm CMOS technology design kit description.

²Laser power is estimated by reported receiver sensitivities under consideration of 20% wall plug efficiency and 16 db of optical loss.

³The power consumption is assessed from state of the art comparators running at 10 Gbps.

rate versus receiver sensitivity. Higher bit rates allow reducing the energy per bit consumption of the temperature control as its consumption is independent of the bit rate. On the other hand, higher receiver sensitivities allow lower laser powers. The relation between bit rate and sensitivity becomes intuitive if the classic gain bandwidth trade-off of transistors is considered.

Some bit rates and sensitivities reported in recent publications are shown in Fig. 3.2. The lower trend line follows $S = 5\frac{fJ}{bit}BR - 50\mu W$ and the higher trend line follows $S = 15\frac{fJ}{bit}BR - 30\mu W$, where S represents the sensitivity and BR the bit rate. The roughest possible link consumption model is $\frac{TP}{BR} + \frac{S}{LE}$, where TP represents the consumption of the Temperature Control and LE the laser efficiency (assumed to be 20% throughout this work). Note that in this approximation the losses of the waveguides and modulators are neglected. Using this simple link consumption model and the two trend lines, optimal bit rates are found at 8 Gbps and 14 Gbps, respectively. These values are not yet of any importance but they allow to limit the range for studied bit rates between 1 and 50 Gbps.

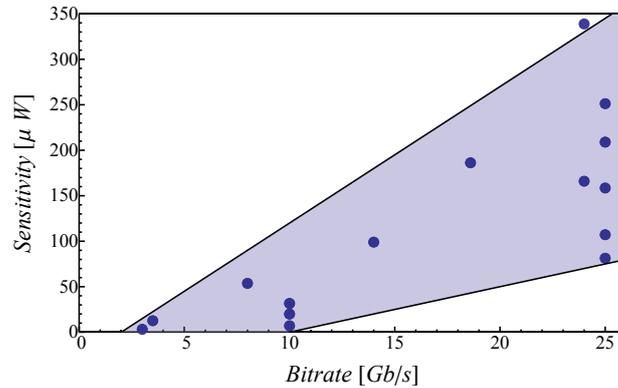


Figure 3.2: Sensitivity dependence on bit rates for reported receivers [12, 27, 29, 33, 35–38, 40–42, 45, 48–54]

In order to assess the previous optimal bit rate estimation recently published optical link receivers (2004, 2011-2015) were analysed by calculating their energy consumption in terms of energy per bit. The total consumption is evaluated by the sum of the receiver's consumption, the minimal laser energy computed from the receiver's sensitivity and the temperature control's power consumption divided by the reported bit rate. The results are shown in Fig. 3.3. They lead to the conclusion that the optimal bit rate should be found between 10 Gbps and 20 Gbps.

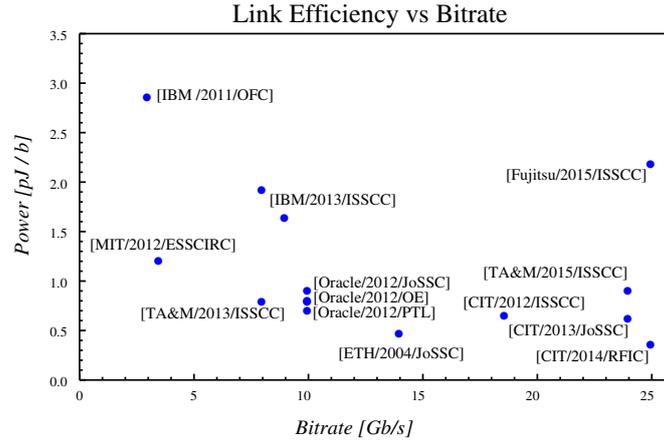


Figure 3.3: Estimated full link power consumption dependence on bit rates based on reported receivers

3.2 TIA Optimization

The trade-off between bit rate and laser power is ultimately set by the TIA of the receiver circuit. For this reason the TIA is at the core of the link optimization and must be very well understood. In the context of silicon photonic links for optical networks on chip (ONoC) three parameters are of high importance: footprint, power consumption and robustness. ONoCs will be used whenever very high data throughput is necessary, hence one chip will employ many link drivers and receivers to communicate with many other chips in a massively parallel computing architecture based on multiple processors. This means that the footprint of the receiver must be very small, forbidding the use of large elements such as inductors. For the same reason, very low power consumption of the receiver is a must. Robustness is required as complex systems to monitor the links functionality can not be afforded. Accounting for these three aspects the topologies for the Rx front-end, studied in this work, are the feedback versions of a common source (CS) amplifier, a single stage push-pull (PP) inverter and a double stage push-pull inverter, shown in Fig. 3.4.

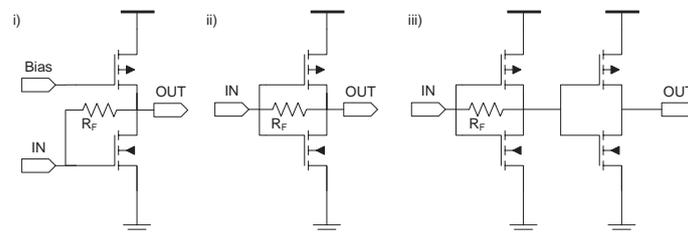


Figure 3.4: TIA Topologies studied in this work: i) Common Source Topology ii) Push-Pull Topology iii) Double Stage Push-Pull Topology

To understand the design degrees of freedom of these three topologies, a parameter extraction was performed for the 65nm technology. To reach high bit rate at low power consumption, low power low threshold voltage transistors are used throughout this work, if not mentioned otherwise. The used small signal model of the transistor is a standard Π -model, the following set of formulas [55] was used to describe the transistors behaviour including short channel effects:

$$I_{dsat} = W\beta \frac{(V_{gs} - V_T)^2}{2(1 + \Theta(V_{gs} - V_T))}, \quad (3.1)$$

$$g_m = I_{dsat} \left(\frac{2}{V_{gs} - V_T} - \frac{\Theta}{1 + \Theta(V_{gs} - V_T)} \right), \quad (3.2)$$

$$g_{ds} = I_{dsat} \frac{\eta}{(V_{gs} - V_T)^m}, \quad (3.3)$$

where the gate length was assumed to be constant and minimal, W is the transistors width, I_{dsat} stands for the saturation current of the transistor, V_{gs} the voltage between the gate and the source terminal, V_T is commonly referred to as threshold voltage, g_m is the transistors transconductance, g_{ds} corresponds to the transistors transconductance between the drain and source node. Finally β , Θ , η and m are fitting parameters. Using the obtained values and the described model the bandwidth and transimpedance range of the CS topology were studied and depicted in Fig. 3.5. For these calculations an input capacitance of 10 fF and a capacitive output loading of 10 fF were assumed. Bandwidth higher than 10 GHz seems possible as well as transimpedances as large as 8 k Ω . The transimpedance bandwidth product was computed and is presented in the rightmost panel of Fig. 3.5. It shows maxima in the range of 5 to 10 μm for the NMOS transistor width. Saturating growth of transimpedance with higher feedback resistance can be observed in the middle panel, which is limited by the increasing noise of the amplifier as will be discussed later.

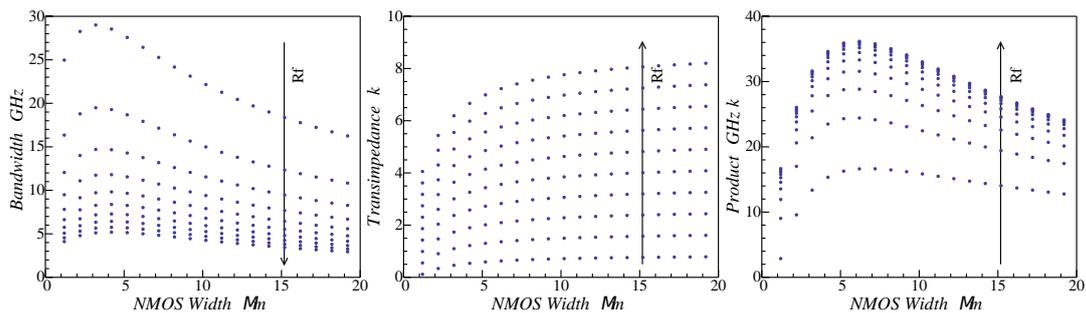


Figure 3.5: Analytically obtained bandwidth and transimpedance values for the CS topology

For the CS TIA topology the results from the analytical model are compared to AC transistor level simulations in Fig. 3.6. All simulations within this work were

carried out either using the ADS or the Eldo simulator. The analytically obtained results achieve to follow the trends obtained from the simulations. Nevertheless, they show non-negligible deviations from the simulated results. These deviations are in the range of 10%. Moreover, they shift the position of the maxima in the parameter space. As a result, the analytical solutions were used to find the correct parameter space but not to proceed in the optimization study.

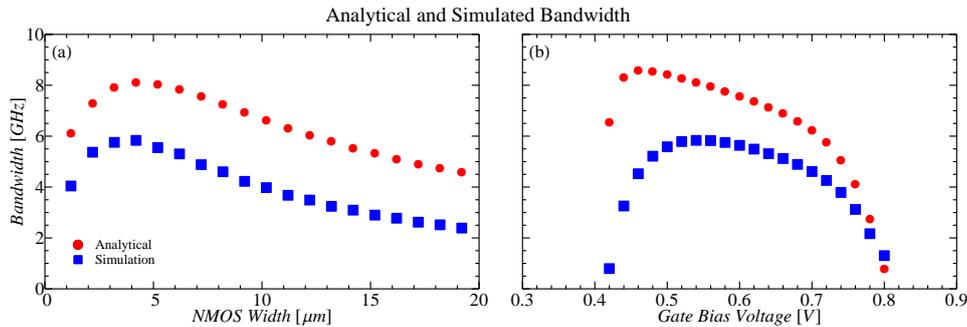


Figure 3.6: Comparison between bandwidth values obtained by analytical calculations and computer aided simulations

3.2.1 Simulated Database Approach

Instead of relying on the analytical relations a database was constructed based on transistor level simulations of the considered TIA topologies. These simulations were carried out for the 65nm and 28nm technology nodes with the following parameter sweeps.

Technology	65 nm	28nm
Output Load [fF]	10, 100	10, 40
Input Load [fF]	10 .. 200	10 .. 200
Feedback Resistance [kΩ]	0.5 .. 40	0.5 .. 40
NMOS Transistor Width [μm]	0.135 .. 20	0.60 .. 20
V_{DD} [V]	1.2	1.0

For the CS topology the biasing voltage of the PMOS was also swept between 0.4 and 0.8 V for both technologies. The PMOS transistor in the PP topologies was sized so that the trip point stayed at $\frac{V_{DD}}{2}$, achieved by a factor of 2.3 between PMOS and NMOS transistor widths.

This database has been used in several ways throughout the optimization. First conclusions can be drawn from sorting the database by power consumption for defined triplets of bandwidth (B), transimpedance (T) and input capacitance (C_{in}) after eliminating all solutions which exceed a given input referred noise (IRN) limit, set by the demanded bit error rate (BER).

Noise Theory and Bit Error Rate

Setting a maximal input referred noise limit is important as it strongly impacts the design of the link. To understand its influence we compute the bit error rate's dependence on the IRN.

The IRN is the noise contribution of the circuit, expressed as the noise that needs to be injected at the input into a noiseless circuit so that the output noise of the ideal circuit is equal to the output noise of the real circuit. As such it corresponds to the standard deviation of the input noise current $\langle \delta i_{full}^2 \rangle$ and defines the distribution of input currents:

$$p_{(x|0)}(i) = \frac{1}{\sqrt{2\pi\langle \delta i_{full}^2 \rangle}} \exp\left(-\frac{(i - \langle i_0 \rangle)^2}{2\langle \delta i_{full}^2 \rangle}\right), \quad (3.4)$$

where i is the current flowing into the input of the TIA and $\langle i_0 \rangle$ is the mean current value when a 0 is transmitted, as illustrated in Fig. 3.7. If it can be assumed that the noise distributions $p_{(x|0)}$ and $p_{(x|1)}$ are equal, the optimal threshold current to distinguish between a received 0 or 1 will be at

$$i_{Thresh} = \frac{\langle i_1 \rangle + \langle i_0 \rangle}{2}. \quad (3.5)$$

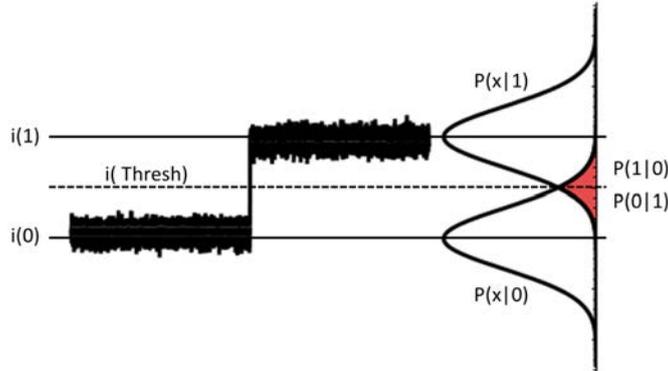


Figure 3.7: Noisy input current signal and corresponding noise distributions

The bit error rate can now be expressed as the probability that a 0 was transmitted but the measured current exceeded i_{Thresh} and is received as an 1. See red marked $p_{(1|0)}$ area in Fig. 3.7. This probability can be expressed as

$$BER_0 = p_{(1|0)} = \int_{V_{Thresh}}^{\infty} p_0(i) di = \frac{1}{\sqrt{2\pi}} \int_Q^{\infty} e^{-u^2/2} du, \quad (3.6)$$

with $u = (i - \langle i_0 \rangle) / \sqrt{\langle \delta i_{full}^2 \rangle}$, where the noise distance

$$Q = \frac{(\langle i_1 \rangle - \langle i_0 \rangle)}{2\sqrt{\langle \delta i_{full}^2 \rangle}} \quad (3.7)$$

has been introduced, too. From symmetry reasons it follows that $BER_1 = BER_0 = BER$, which can be approximated as

$$BER = \frac{1}{\sqrt{2\pi}} \int_Q^\infty e^{-u^2/2} du \approx \frac{1}{Q\sqrt{2\pi}} \exp\left(-\frac{Q^2}{2}\right). \quad (3.8)$$

As high performance computing is based on the massive communication of single processing units, BERs of 10^{-12} are the norm for links inside these machines. A BER of 10^{-12} is achieved when Q exceeds 7. This means that if $\langle i_0 \rangle$ can be assumed to be 0 A, the input referred noise can be expressed as

$$i_{IRN} = \frac{\langle i_1 \rangle}{14}.$$

It can be finally concluded that the minimal required input current is linearly dependent on the input referred noise, hence only TIAs with equal IRN can be meaningfully compared. An interesting sensitivity might be -18 dBm optical power; it corresponds to a maximal IRN of $0.9 \mu A_{RMS}$, if a photodiode with a responsivity of 0.8 A/W is assumed. Therefore, the database was filtered for configurations with IRN inferior to $0.9 \mu A_{RMS}$.

3.2.2 Results from TIA database

The first result obtained is that the CS topology is inferior to the PP topologies in terms of power consumption in each of the studied points. Therefore the rest of our analysis will focus on the single stage PP and the double stage PP topologies. To visualize the results Fig.3.8-3.13 show the power consumption as a function of the bit rate (B), transimpedance (T) or input capacitance (C_{in}) for different situations. The solid lines represent the PP topology while the dashed lines represent the PP-PP topology. In the rest of this subsection we discuss some particularly interesting results, but Fig.3.8-3.13 can be used by the reader to choose the optimal TIA for other situations, not explicitly discussed here.

Results for the 65nm technology node

Fig.3.8 gives us several pieces of information. Firstly, for a very small input capacitance of 10 fF and a small transimpedance of 1 k Ω the highest directly achievable bit rate is 18 Gb/s (Fig.3.8.a), for a BER of 10^{-12} with the ST65nm technology. The PP TIA topology reaching this bit rate uses $R_F = 1.5$ k Ω , $W_N = 1.635 \mu m$ and consumes 0.24 pJ/bit. 18 Gb/s is derived from the system bandwidth of 14 GHz and a bandwidth to bit rate factor of around 1.25 [55] which accounts for the fact that some bandwidth can be sacrificed before inter symbol interference (ISI) will

take effect. Nevertheless, higher bit rates can be achieved when Decision Feedback Equilibration (DFE) is used. In [36] the input bandwidth of the DFE system is 1.5 GHz and a bit rate of up to 9 Gb/s is achieved. If higher transimpedances are required, the bandwidth decreases naturally. If the input capacitance stays low, the PP topology remains the faster topology. Nonetheless, in a system containing a bonded PD the input capacitance rapidly exceeds 100 fF and the PP-PP topology becomes the faster one. The fastest configuration of PP-PP with an input capacitance of 110 fF and a transimpedance of 10 k Ω reaches a bit rate of 3.6 Gb/s using $W_{N1} = 3.885 \mu\text{m}$, $R_F = 1.5 \text{ k}\Omega$ and $W_{N2} = 4.885 \mu\text{m}$. Intuitively, a single-stage solution is in most cases more power efficient than a two-stage solution. Still, in the particular case of low bandwidth and high transimpedance, in order to avoid a decision stage, the PP-PP topology is the more power efficient approach. As depicted in Fig.3.9.a the PP topology already consumes 0.20 pJ/b at a transimpedance of 35 k Ω while the PP-PP topology consumes the same power at 310 k Ω for $C_{IN} = 10 \text{ fF}$ and a bandwidth of 1 GHz.

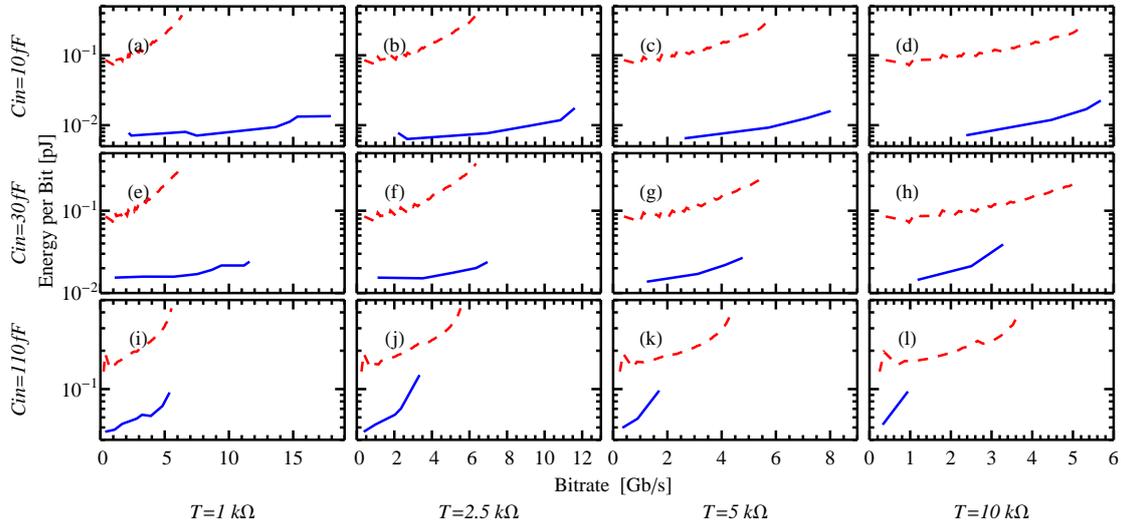


Figure 3.8: Based on extensive sweeps, a database was built up to find for the topologies under study (Push-Pull topology [solid, blue line] and double staged push-pull topology [dashed, red line]) the least power consuming sizing parameters, depending on a minimal demanded bit rate (B) - Each subdiagram represents certain system criteria like minimal transimpedance or capacitance presented by the photodiode (C_{in}).

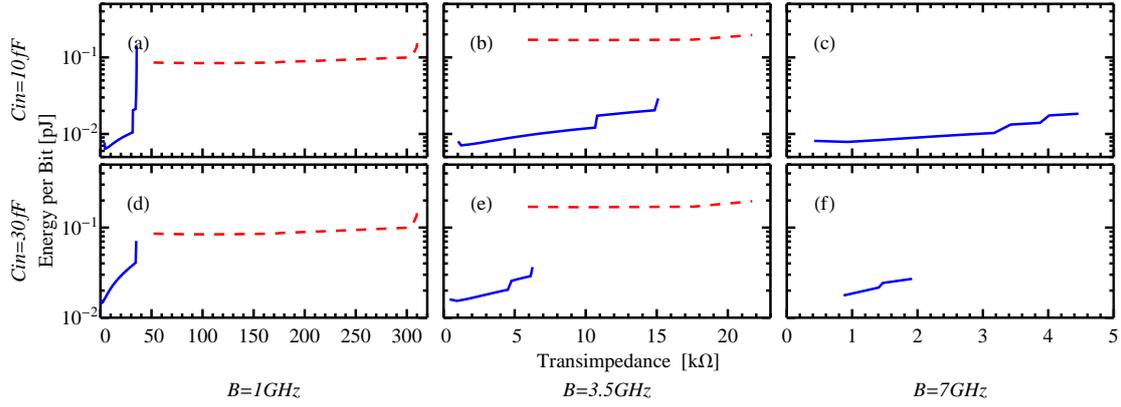


Figure 3.9: Power consumptions in dependence on minimal transimpedance (T)

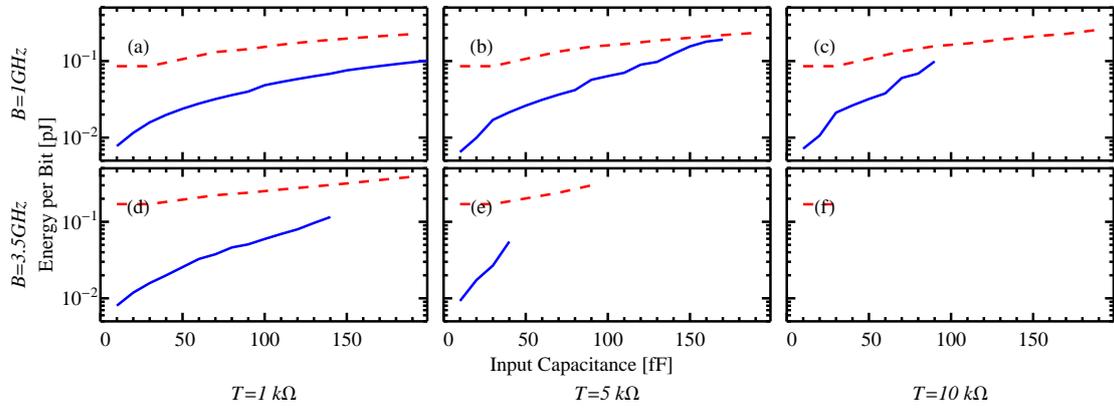


Figure 3.10: Power consumptions in dependence on input capacitance (C_{in})

Results for the 28nm technology node

The benefits of technology scaling in terms of speed and power consumption are clearly visible when comparing Fig.3.8 and 3.11. The highest bit rate in this technology node with a very small input capacitance of 10 fF and a low transimpedance of 1 kΩ is 36 Gb/s (Fig.3.11.a). The TIA realization achieving these values is a PP topology with $W_{N1} = 3.56 \mu\text{m}$ and $R_F = 1.25 \text{ k}\Omega$, consuming only 18 fJ/b.

If it comes to a system with a bonded photo diode and a demand for a high transimpedance, this technology can achieve bit rates up to 5.5 Gb/s (Fig.3.11.l). Here an input capacitance of 110fF and a transimpedance of 10 kΩ is assumed. The TIA configuration would be a double stage PP-PP topology with $W_{N1} = 5.0 \mu\text{m}$, $W_{N2} = 5.9 \mu\text{m}$ and $R_F = 2 \text{ k}\Omega$, consuming 38 fJ/b. Apart from the general improvements of the system performance, Fig.3.11 - 3.13 show the same trends as the 65nm technology node.

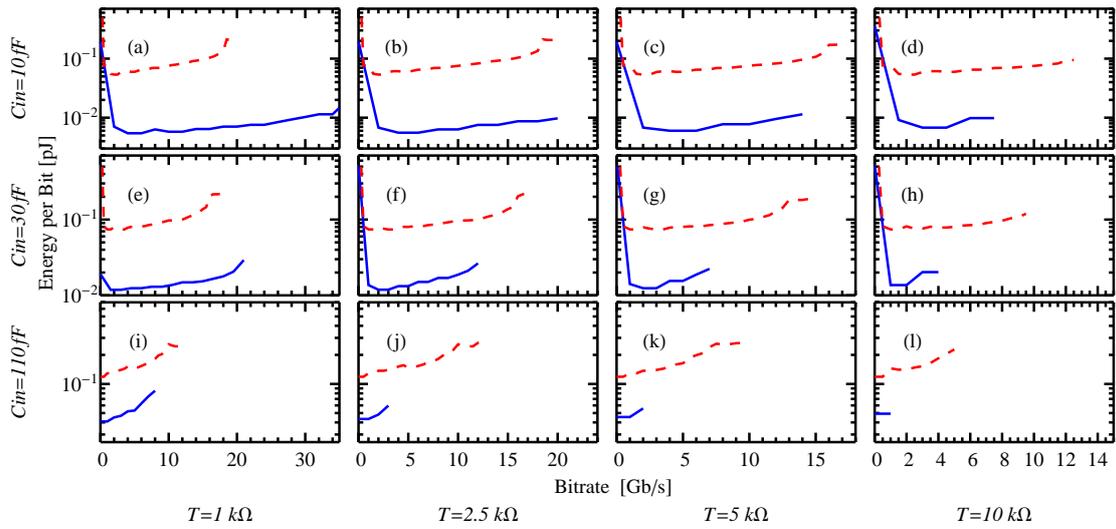


Figure 3.11: Power consumptions in dependence on the minimal bit rate (B)

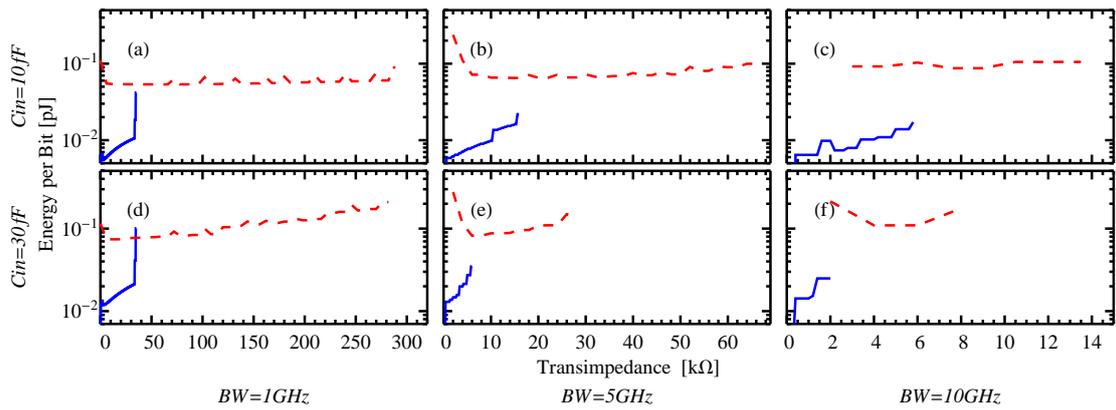


Figure 3.12: Power consumptions in dependence on minimal transimpedance (T)

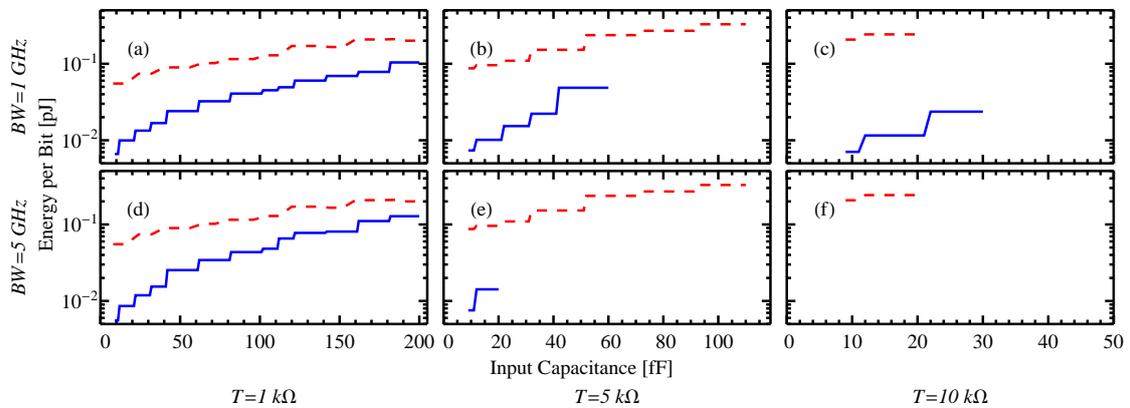


Figure 3.13: Power consumptions in dependence on the input capacitance (C_{in})

Conclusion TIA optimization

These results give a good overview of the possibilities of basic TIA topologies. It is important that the TIAs cover the bandwidth range needed to cover the interesting bit range developed in the introduction of this chapter. Nevertheless, they are not sufficient to make any judgement about the optimal bit rate. A major result is that the energy efficiency decreases with increasing bit rates, because the current consumption of the TIAs rises faster than their bandwidth.

3.3 Receiver Architecture Choice

In this work optical links for short range inter chip networks are considered. Therefore, the environment is a determining factor in the choice of the receiver architecture. The receiver has two main interfaces with the digital circuitry of the computing unit which it will serve, the clock input and the data output. The data output has to run at a clocking frequency compatible with digital logic from standard cell libraries. Thus a deserialization stage is required between the receiver and the digital logic to reduce the data rate by parallelization. There are two options to integrate this stage. The first possibility, shown in Fig. 3.14.a, is to design a receiver that incorporates everything necessary to produce a high speed digital output stream and add a dedicated deserialization stage. The second option, depicted in Fig. 3.14.b, integrates the deserialization as early as possible in the receiver. The first solution includes no parallelization until the last stage leading to smaller footprint in the core of the receiver and less overall capacitance that has to be charged and discharged. On the contrary, the second approach relaxes severely the bandwidth constraints of the decision stage allowing its integration in the deserialization unit. The strength of parallelization is understood when the energy consumption in terms of energy per bit is considered. While all elements in the first approach will have a higher consumption per bit with higher bit rates, in the second approach only the TIA is concerned, because for parallel working circuitry the energy per bit stays the same, independently of the amount of parallel branches.

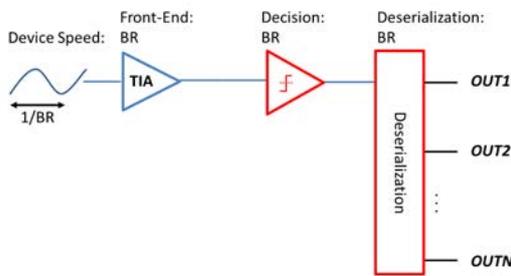


Figure 3.14.a: Serial

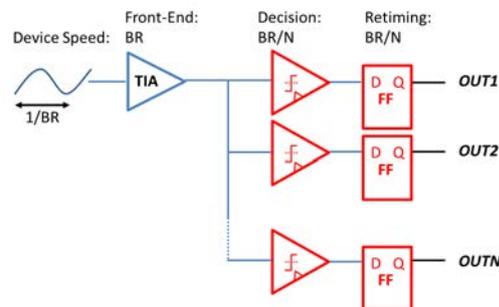


Figure 3.14.b: Parallel

Figure 3.14: Receiver architecture approaches

Furthermore, it has to be considered that for most TIAs the input capacitive pole is the limiting one, hence the loading of the output does not impact the TIAs bandwidth until the output pole frequency approaches the input pole frequency. This argues for a minimally sized TIA whose bandwidth and transimpedance are adapted for the sensitivity of a following parallelized decision stage, that realizes a first deserialization stage.

A further argument for this choice is the superiority of clocked latch-based comparators (please find further details in the receiver chapter 5) over non clocked comparators or simple limiting amplifiers.

These arguments lead, for the 65nm technology, to a receiver architecture based on a single stage TIA, followed by a bench of comparators succeeded by a bench of flip-flops.

3.4 Link Component Models

The considered link architecture corresponds to the link shown in Fig. 3.1. In order to find the optimal bit rate analytical models for all other elements in the link but the TIA were used. In this approach the proceeding stage defines the minimal requirements for the preceding stage in the link, hence the analyse starts with the deserialization / comparator stage in the RX. Although models are used for most stages, they are based on designs of the components. Therefore every component was optimized and simulated at transistor level in both technology nodes, 65nm and 28nm. Only afterwards important parameters are taken from the results to build the models.

Comparators

The parameter that defines the preceding stages of the comparators is their sensitivity, as it defines the minimal output swing of the TIA. In simulation we achieved sensitivities of 30 mV in the 65 nm technology and 15 mV in the 28 nm technology. The number of comparators also define the loading of the TIA; the input capacitance in the 65nm technology is 5 fF and in the 28nm technology 2 fF. How the different loadings impact the optimization process is explained later. The last parameter used is the energy per comparison which is 50 fJ per comparison in 65nm and 20 fJ per comparison for 28nm. Please find further details in the comparator section inside the receiver chapter 5.

TIA

The TIAs are represented by the corresponding quadruplets of bandwidth, transimpedance, power consumption and input related noise, as explained in the previous section.

Laser and Waveguides

The laser output power is the sensitivity of the comparator divided by the gain of the TIA plus 14 times the IRN . Adding 14 times the IRN is needed to sustain a BER of 10^{-12} , as shown in section 3.2.1. Furthermore, optical losses are considered to be 3 dB for coupling the laser inside the chip using a grating coupler, 2 dB loss inside the ring modulator, 1 dB loss inside the waveguide and another 10 dB due to the ring filter, used to drop the signal with the correct wavelength in the RX. The laser is assumed to have a wall-plug-efficiency of 20 %.

Temperature Control

The temperature control is necessary to control the resonance wavelength of the ring modulator. Depending on the number of wavelength and therefore on the number of parallel links employed, the ring resonator has to be tuned either over its entire free spectral range or until the next channel. Hence there are many power scenarios to be differentiated. The study will present results for different consumptions but if not other indicated a consumption of 3 mW independent of the bit rate [8] is assumed.

Modulator Driver

Since modern CMOS technology nodes can not support much more than 1 V, double rail drivers are necessary to correctly drive resonant ring modulators. Independent from their exact architecture, they work like standard digital buffers [29]. Taking this into account, the energy consumed by the circuit can be described in a first order approximation as

$$E = \left(\sum_{i=0}^N f^i C_{IN} + C_{OUT} \right) \frac{V^2}{2}, \quad (3.9)$$

where C_{IN} represents the gate capacitance of the first buffer stage, C_{OUT} the modulator capacitance, f the growing factor between consecutive stages, V the supply voltage and N the number of needed stages. The parameter f is mainly defined by the technology and can be handled as a constant in this consideration. Therefore, N is the only undefined variable when designing this buffer. It can be approximated when it is assumed that the current driving capability of the N th stage has to load C_{OUT} four times faster than the bit rate (B_r). The factor four was chosen to guarantee an open eye:

$$f^N = \frac{4B_r C_{OUT} V}{I_{IN}}, \quad (3.10)$$

where I_{IN} describes the current of a minimal sized inverter. This leads to an logarithmic behaviour of N :

$$N = \frac{\log\left(\frac{4B_r C_{OUT} V}{I_{IN}}\right)}{\log(f)}. \quad (3.11)$$

Combining Eq.3.9 and 3.11 leads to a linear behaviour of the driver's energy consumption per bit as a function of the bit rate:

$$E(B_r) = \left(\frac{(4VC_{OUT} \cdot B_r - I_{IN})fC_{IN}}{I_{IN} \cdot (f - 1)} + C_{OUT} \right) \frac{V^2}{2}. \quad (3.12)$$

As this is just a first order approximation transistor level simulations of three- four- and five stage double rail drivers were used to acquire their maximal bit rate. These datasets were used for linear regressions in the two technologies, to tune the models of the driver power consumption. Furthermore, the modulator was assumed to have an input capacitance of 50 fF in all cases. The datapoints used for the linear regression are:

Data Rate Limit [Gbps]	0	6	6.5	14	16
Consumption 65 nm [fJ/b]	0		175	280	
Consumption 28 nm [fJ/b]	0	100			120

Serialization Stage

The basic topology considered for this study consists of two stages. The first stage performs the gating of the digital signals with individual clock phases ϕ when entering the serializer, using AND gates. The second stage combines all gated signals, using OR gates, see Fig. 3.15. This topology leads intrinsically to a logarithmic energy increase with raising data rate. While in the 65nm technology node this topology has to be strictly followed to achieve high data rates, the 28nm technology node libraries provide a more efficient implementation of this function. The obtained simulation values are shown in the table below. The fields filled with ... denote that further increase in bit rate has only negligible effect on the increase of the power consumption and therefore stays constant.

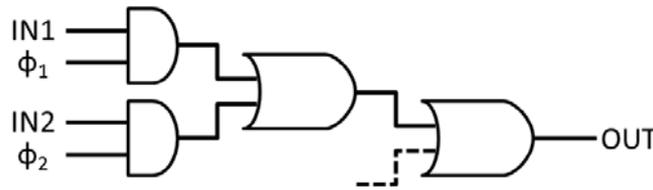


Figure 3.15: Basic serializer architecture

Data Rate [Gbps]	0	2	4	6	8	10	12	14	16	18	20
Cons. 65 nm [fJ/b]	0	84	116	116	148	148	148	148	180
Cons. 28 nm [fJ/b]	0	5.7	7.2	7.9	9.4	9.4	10.1

3.5 Relation of Bit Rate and Bandwidth

The relation between the bandwidth of a TIA and the optimal bit rate that can be processed depends on various system properties. In the previous sections a constant factor of 1.25 was used to relate the bit rate to the TIAs bandwidth but a deeper understanding of the system shows a more complex relation. Hereafter, an approach is shown to find the optimal bit rate depending on the TIA's bandwidth its gain and the timing uncertainty of the decision taking (jitter).

If the electrical front-end of a receiver is understood as a first-order low pass filter and the input is considered to be a perfect square wave, then the following equation holds for a low to high transition:

$$V_{out} = V_{IN} \left(1 - \exp^{-\frac{t}{RC}} \right), \quad (3.13)$$

where R represents the output resistance and C the capacitive load of the circuit. Furthermore, for a first order RC filter $RC = 1/2\pi BW$ holds, where BW stands for the bandwidth of the circuit. This means that the maximal rise of the output signal within one bit period (T_{Bit}) will be:

$$V_{out} = V_{IN} \left(1 - \exp^{-2\pi T_{Bit} BW} \right). \quad (3.14)$$

As the front-end of an optical receiver will in some way act as a transimpedance, we can write $V_{IN} = Z_T \cdot I_{IN}$, where Z_T is the DC transconductance of the circuit and I_{IN} is the current generated in the photodiode for an optical 1 signal. This leads us to the following expression:

$$V_{Rise} = Z_T \cdot I_{IN} \left(1 - \exp^{-2\pi T_{Bit} BW} \right), \quad (3.15)$$

compare Fig. 3.16. Moreover, we can conclude for a high to low transition, also shown in Fig. 3.16, the following expression:

$$V_{Drop} = Z_T \cdot I_{IN} - V_{out} = Z_T \cdot I_{IN} - Z_T \cdot I_{IN} \left(1 - \exp^{-2\pi T_{Bit} BW} \right). \quad (3.16)$$

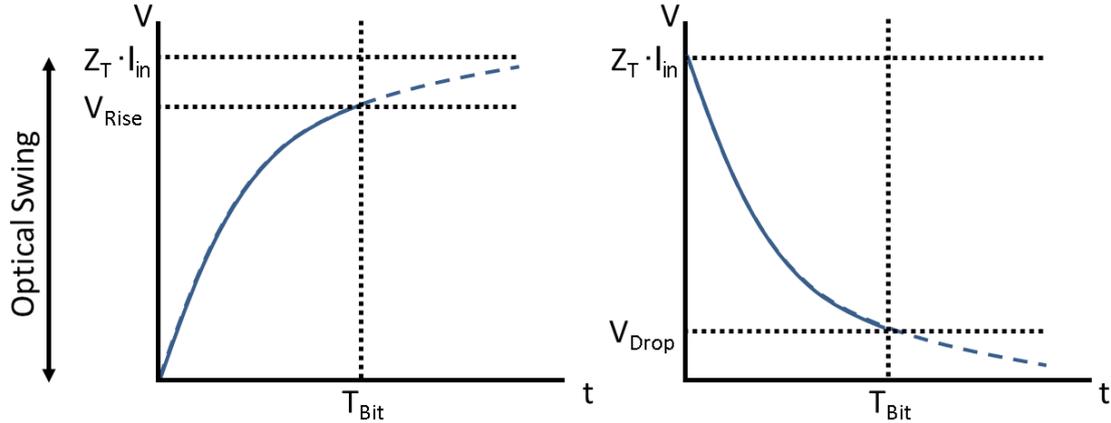


Figure 3.16: Rising and falling transition of a first order low pass filter

Equation 3.15 and 3.16 allow us now to understand and optimize the connections between bandwidth, gain, noise, minimum output swing and optical input power.

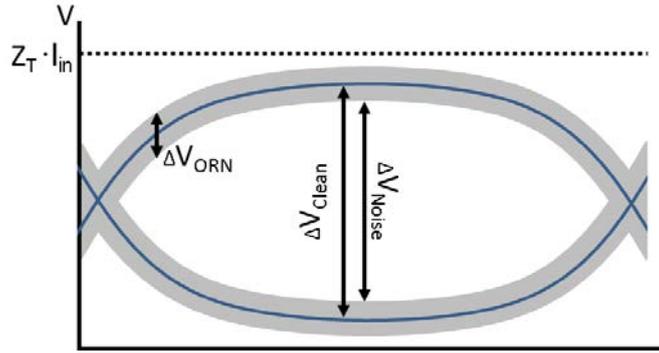


Figure 3.17: Eye diagram

Fig. 3.17 shows a sketch of an eye diagram. If this input is fed into a decision stage ΔV_{Noise} has to exceed the minimal input swing for the decision stage. ΔV_{Noise} already incorporates the noise of the output signal. The amount of noise that has to be incorporated in this analysis depends on the desired bit error rate. If the bit error rate has to be inferior to 10^{-12} , the incorporated noise is $\approx 14\Delta V_{ORN}$, where ΔV_{ORN} represents the RMS value of the output referred noise. The factor 14 corresponds to the 7σ environment needed to ensure this bit error rate. It follows:

$$\Delta V_{Noise} = \Delta V_{Clean} - 14\Delta V_{ORN}. \quad (3.17)$$

Using Equation 3.15 and 3.16, ΔV_{Noise} and ΔV_{Clean} can be represented as:

$$\Delta V_{Clean} = V_{Rise} - V_{Drop} = Z_T \cdot I_{IN} \left(1 - 2 \exp^{-2\pi \frac{BW}{BR}} \right), \quad (3.18)$$

$$\Delta V_{Noise} = Z_T \cdot I_{IN} \left(1 - 2 \exp^{-2\pi \frac{BW}{BR}} \right) - 14\Delta V_{ORN}, \quad (3.19)$$

where $BR = 1/T_{Bit}$, denotes the bit rate. Eqn. 3.19 can now be used to compute the maximal bit rate set by the condition $\Delta V_{Noise} = \Delta V_{Min}$:

$$BR = \frac{-2\pi BW}{\ln\left(\frac{1}{2} - \frac{\Delta V_{Min} + 14\Delta V_{ORN}}{2 \cdot Z_T \cdot I_{In}}\right)}, \quad (3.20)$$

where \ln represents the natural logarithm. This model can be expanded to include jitter. To incorporate the jitter, it is assumed that the jitter only influences the timing uncertainty. Hence a minimal time period is needed in which the eye remains open. This requirement is obviously fulfilled when T_{Bit} is replaced by $T_{Bit} - T_{Jit}$. The new maximal bit rate is therefore:

$$BR = \frac{-2\pi BW}{\ln\left(\frac{1}{2} - \frac{\Delta V_{Min} + 14\Delta V_{ORN}}{2 \cdot Z_T \cdot I_{In}}\right) - 2\pi T_{Jit} BW}. \quad (3.21)$$

Note that a higher optical input power (I_{In} in 3.21) allows a higher bit rate for a given bandwidth. This relation has to be optimized for an electro-optical link in terms of power efficiency. The term that needs to be optimized is:

$$\varepsilon_{E/B} = I_{In}/BR. \quad (3.22)$$

$\varepsilon_{E/B}$ is directly correlated to the power consumption of the laser regarding the energy per bit, as I_{In} defines the required laser output power and is divided by the links bit rate. A compact form of this formula is:

$$\varepsilon = -\frac{x T_{Jit}}{B} \left(\ln\left(\frac{1}{2} - \frac{A}{x}\right) - B \right), \quad (3.23)$$

with $A = \frac{\Delta V_{Min} + 14\Delta V_{ORN}}{2Z_T}$, $B = 2\pi T_{Jit} BW$ and $x = I_{In}$. The derivative of this equation is:

$$\frac{d\varepsilon}{dx} \cdot \frac{B}{T_{Jit}} = -\frac{A}{\left(\frac{1}{2} - \frac{A}{x}\right) x} - \text{Log} \left[\frac{1}{2} - \frac{A}{x} \right] + B. \quad (3.24)$$

To find the optimum, the derivative has to be set to zero. In order to solve this equation, the substitution $y_0 = \frac{1}{2} - \frac{A}{x_0}$ has to be made. Using this substitution we can find that:

$$0 = -\frac{A}{y_0 \left(-\frac{A}{y_0 - \frac{1}{2}}\right)} - \ln(y_0) + B, \quad (3.25)$$

$$-B = 1 - \frac{1}{2y_0} - \ln(y_0), \quad (3.26)$$

$$\exp^{-B-1} = \exp^{-\frac{1}{2y_0} + \ln(y_0)}, \quad (3.27)$$

$$-\frac{1}{2} \exp^{-1-B} = -\frac{1}{2y_0} \exp^{\frac{-1}{2y_0}}. \quad (3.28)$$

There is no known closed analytical solution for this type of formula. It is nevertheless possible to express the solution, which is called Lambert's W function¹, as a series expansion. x_{min} can therefore be described as:

$$x_{min} = \frac{2A \cdot PL[-\frac{1}{2} \exp^{-1-B}]}{PL[-\frac{1}{2} \exp^{-1-B}] + 1}, \quad (3.29)$$

where PL represents Lambert's W function. If we put everything back into place we get:

$$I_{Opt} = \frac{(\Delta V_{Min} + 14\Delta V_{ORN})}{Z_T} \cdot \frac{PL[-\frac{1}{2} \exp^{-1-2\pi T_{Jit}BW}]}{PL[-\frac{1}{2} \exp^{-1-2\pi T_{Jit}BW}] + 1}. \quad (3.30)$$

The first term of Eq. 3.30 can be understood as a minimal input current, I_{Min} . It represents the input signal needed to achieve a sufficient eye opening for a system in which the rise or fall time is negligible compared to T_{Bit} . The second factor represents the plus of power required to reach optimal conditions in a realistic system, f_I . The branch of the W function needed in this calculation maps $[-\frac{1}{e}, 0]$ on $[-\infty, -1]$, hence f_I is always superior to 1. The remaining question is which relation between bit rate and bandwidth is optimal:

$$f_{BW} = \frac{BR}{BW} = \frac{-2\pi}{1 + PL[-\frac{1}{2} e^{-1-2\pi T_{Jit}BW}]}. \quad (3.31)$$

It is highly interesting to notice in Eq.3.31, that the optimal ratio between bandwidth and bit rate depends only on the product of the bandwidth itself and the jitter of the system. Fig. 3.18 shows the dependence of f_I and f_{BW} on the systems jitter for a fixed bandwidth of 20 GHz.

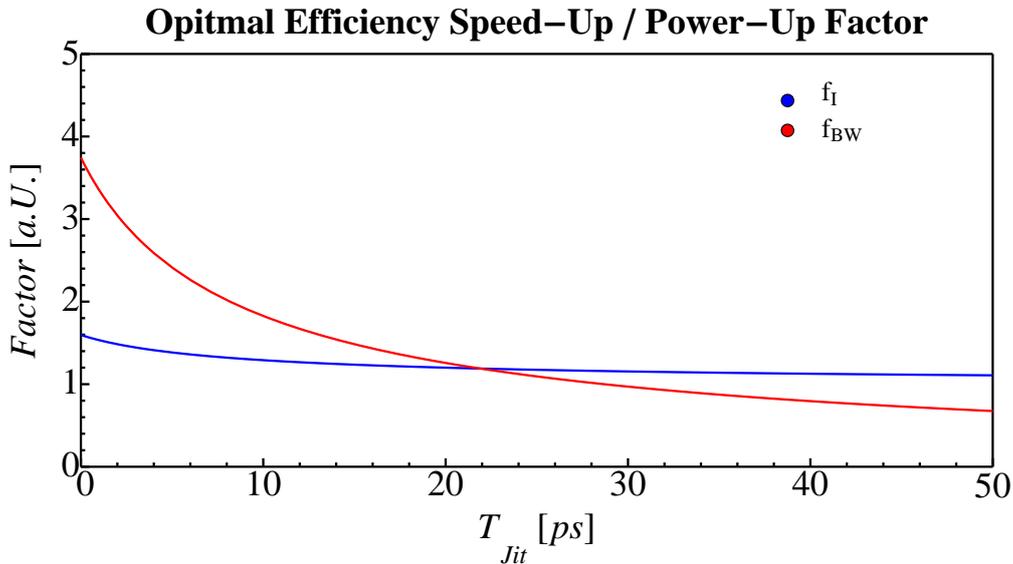


Figure 3.18

¹see "http://mathworld.wolfram.com/LambertW-Function.html"

For large T_{Jit} f_I tends towards 1 while f_{BW} drops below 1. It is obvious that for highly jittering systems the possible bit rate is lower than the bandwidth, but it is interesting to notice that it does not imply that more input power is needed. Furthermore, for low jitter systems f_{BW} exceeds 1 and more importantly it rises faster than f_I . If the jitter is considered to be 0 than $f_I = 1.6$ while $f_{BW} = 3.7$. Following this result older designs should be revisited and checked whether the energy per bit ratio can be optimized by increasing the system's optical input power and bit rate.

This analysis applies only for first order systems, meaning that any system including inductors or having multiple poles do not necessarily follow these trends. Nevertheless, designs based on TIA front-ends feeding decision stages will in most cases follow. It can be concluded that for silicon photonic receivers it is not optimal to chase designs with highest optical sensitivity, as a small increase in input power might lead to strong increase in bit rate, reducing the overall energy consumption of the system.

3.6 Full Link Optimization

Although the comparators, being the last part of the link, set the start of the condition chain of the link, it is the TIA database that is used as core for the full link optimization. The optimization algorithm computes for each TIA in the database the power consumption of the entire link and then searches through the database to find the least power consuming solution.

The first step is to find from the bandwidth of a TIA in the database the corresponding bit rate. In the preceding chapter equation 3.31 was derived for this purpose, but it has also to be considered that a higher bit rate needs more comparators for deserialization and therefore the TIA is stronger loaded. To account for that, a linear interpolation is used. The equations describing the linear interpolation are:

$$C_{Int} = \frac{BR}{f_0} C_0, \quad (3.32)$$

$$BW = (C_{Int} - C_1) \frac{BW_2 - BW_1}{C_2 - C_1} + BW_1. \quad (3.33)$$

C_{Int} denotes the interpolated output capacitance stemming from the extra loading, C_0 the capacitance of a single comparator, C_1 the capacitive load used in a first simulation leading to the bandwidth BW_1 , C_2 the capacitive load used in a second simulation leading to BW_2 . f_0 corresponds to the clocking rate of the comparators being 2 GHz for both technologies. The relation between BR and BW is defined by 3.31 as:

$$BR = \frac{-2\pi BW}{1 + PL[-\frac{1}{2} \exp^{-1-2\pi T_{Jit} BW}]}, \quad (3.34)$$

Due to Lambert's W function this set of equations (3.32 - 3.34) cannot be solved analytically but needs to be solved numerically for each entry of the database. Within this step the optimal input current needs to be computed too, as it depends on the assumed jitter and the optimized bit rate. To conclude, in the first step of the optimization process the optimal bit rate and the input current are added to the database for each TIA.

In the second step the power consumption of all other elements for each database entry is calculated, depending on the entry's bit rate. Finally the least power consuming solution in the database is searched.

3.6.1 Optimization Results

All assumptions and design parameters for both technologies are given in the following table.

	65 nm	28 nm
Comparator C_{IN}	5 fF	2 fF
Comparator V_{IN-MIN}	30 mV	15 mV
Comparator Consumption	50 fJ/b	20 fJ/b
TIA C_{IN} [27]	20 fF	20 fF
Photodiode Responsivity	1 A/w	1 A/W
Optical Losses	16 dB	16 dB
Laser Efficiency	20 %	20 %
Temperature Control [29]	3 mW	3 mW
Base Bit Rate for Serialization	2 Gbps	2 Gbps

Under these assumptions the optimal bit rate of the link for the 65nm technology is

$$BR_{65} = 10 \text{ Gbps.}$$

It would consume

$$P_{65} = 0.67 \text{ pJ/b.}$$

This link would embody a TIA with the following parameters:

Bandwidth	C_{out}	Trans.	Cons.	IRN	Sens
4.1 GHz	25 fF	6.3 k Ω	160 μ W	0.13 μ A _{RMS}	7 μ A
Component Sizes					
W_N	W_P	R_F			
1.135 μ m	2.6 μ m	7.5 k Ω			

These results are very interesting because they allow to asses that the goal of an energy consumption of less than 1 pJ / bit can already be achieved. It is also very interesting to see that with the assumed jitter of 20 ps the factor between bandwidth and bit rate found to be optimal is 2.5. On the other hand the decrease

of sensitivity is only a factor of 1.4, if the optimized sensitivity is compared to the maximal sensitivity obtained by dividing the output swing plus the noise overhead divided by the transimpedance.

The optimal bit rate found in the 28nm technology is:

$$BR_{28} = 16.5 \text{ Gbps},$$

consuming

$$P_{28} = 0.40 \text{ pJ/b}$$

and embodying the following TIA:

Bandwidth	C_{out}	Trans.	Cons.	IRN	Sens
8.3 GHz	16 fF	4.2 k Ω	330 μ W	0.24 μ A _{RMS}	9.1 μ A
Component Sizes					
W_N	W_P	R_F			
1.76 μ m	4.05 μ m	5 k Ω			

The optimal link in 28nm consumes nearly half the amount of power as the 65nm version. It also shows a factor of 2 between bandwidth and optimal bit rate as well as a factor of 1.3 between maximal and optimal sensitivity. It is interesting to notice that the sensitivity of the 28nm front-end is lower than sensitivity of the 65nm front-end. In both technologies a static thermal tuning power of 3 mW was assumed, which is, according to the power splits in Fig. 3.19, the biggest consumer in both links. In the 28nm technology the other components consume less power than in the 65nm technology, therefore increasing the bit rate on costs of sensitivity raises the overall power efficiency of the link.

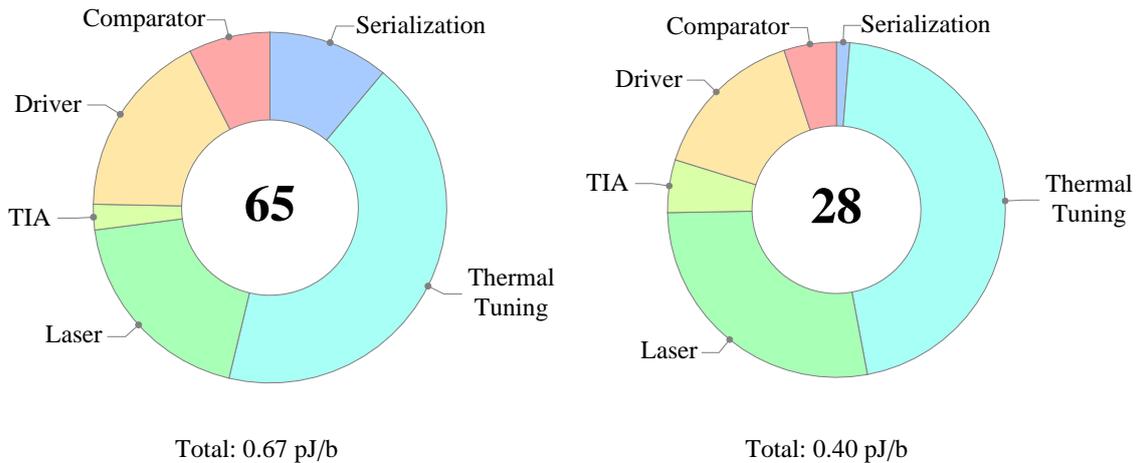


Figure 3.19: Power split of the modelled links for both technologies

To compare the two technologies and to evaluate the environment of the described minima least consuming solutions were computed for fixed bit rates in Fig. 3.20. The first and intuitive conclusion is that the 65nm technology leads to more power consuming links that cannot run as fast as the 28nm links. More interesting is the fact that the energy consumption functions in both technologies are shaped like a bathtub with extensive bottom sections. This means that the exact placement of the bit rate is not crucial. With regard to the 65 nm technology any bit rate between 8 Gbps and 15 Gbps leads to low energy consumption and the same holds for the 28nm technology for bit rates between 12 Gbps and 22 Gbps. This leaves some design freedom that can be used for optimising other aspects of the overall system structure.

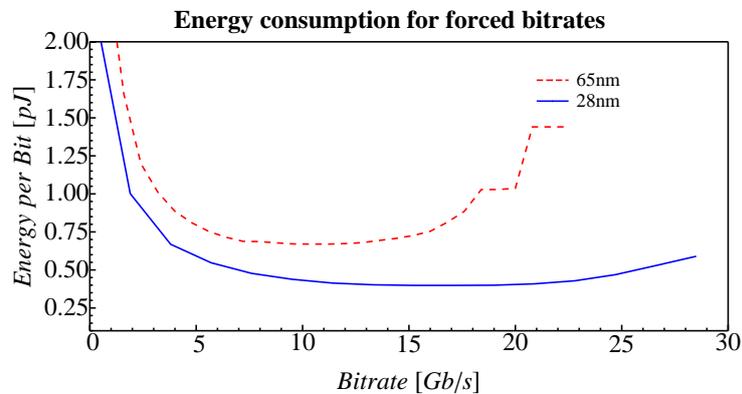


Figure 3.20: Energy consumption in energy per bit depending on a forced bit rate

Given the importance of the thermal tuning of the ring modulator it is interesting to see how the optimal bit rate behaves if it is changed. Fig. 3.21 shows the energy consumption depending on the bit rate for different thermal tuning powers. It is clearly visible that lowering the thermal tuning power leads to a linear decrease of the optimal bit rate. This is a very important result because it means that future work on the development of silicon photonic links should focus on reducing the thermal tuning power and not on increasing its speed, as long as the energy per bit optimization is the ultimate goal.

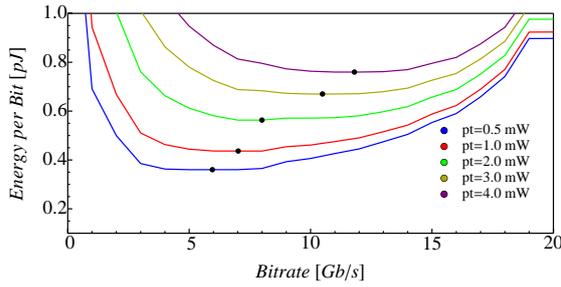


Figure 3.21.a: 65nm

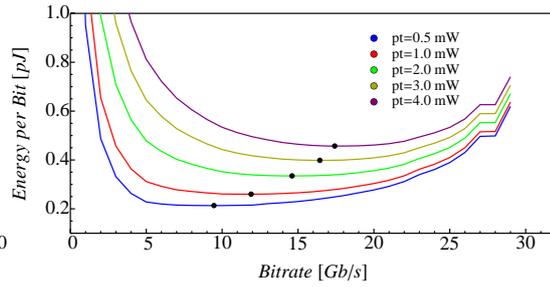


Figure 3.21.b: 28nm

Figure 3.21: Development of optimal bit rate with changing thermal tuning powers

In Fig. 3.22 the energy consumption's development is shown for different RX input capacitance from 10 fF to 200 fF, contributed by the photodiode in the RX. In this case, future photodiodes with smaller capacitance will lead to higher optimal bit rates. Nevertheless, even for the 10 fF photodiode the optimal bit rate is at 18 Gbps.

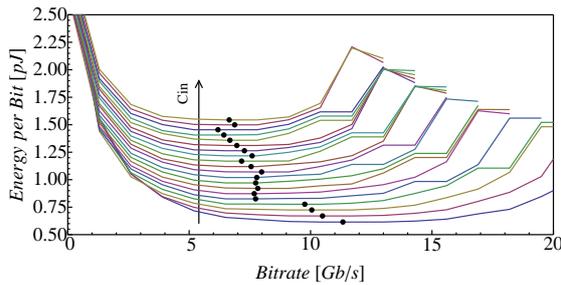


Figure 3.22.a: 65nm

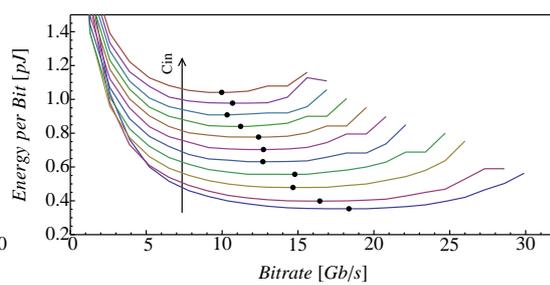


Figure 3.22.b: 28nm

Figure 3.22: Lowering the input capacitance leads to increased optimal bit rates

3.7 Conclusion

In this chapter an optimization was presented based on a simulated database of basic TIA topologies, single stage push pull topology, double stage push pull topology and common source topology. Furthermore, power consumption models for all components in the link, based on simulations, were presented.

To link the TIAs bandwidth to a possible bit rate a theoretical study was performed based on a first order model of the TIA. The highly interesting outcome of this study is that the optimal bit rate depends only on the TIA's bandwidth and the system jitter. This results in bandwidth to bit rate factors higher than 2.

The TIA database was used as a starting point to drive the optimization for the entire link. In this optimization it was found that a bit rate of 10 Gbps is ideal for the 65nm technology while a bit rate of 16 Gbps is optimal for the 28nm

technology. Due to the big share of thermal tuning and laser power in the power budget, the priorities for future developments should be led by the reduction of the thermal tuning power, which would lead to even lower optimal bit rates. Followed by increased receiver sensitivities; higher bit rates should be targeted only subsequently.

Chapter 4

The Transimpedance Amplifier

“The philosophers have only interpreted the world, in various ways. The point, however, is to change it.”

Karl Marx

4.1 Introduction

Although the optimization leads to the conclusion that an optimally working link runs at a bit rate of 10 Gb/s for the chosen 65nm CMOS technology, the realized TIA was designed for a bit rate of 8 Gb/s. This is because this work was carried out in the framework of the HUBEO+ project that defined that bit rate. Furthermore, inside the optimization analysis it was assumed that the feedback is realized by a resistor. As already discussed in the state of the art there are many implementations with more complex feedback paths including inductors, to make use of inductive peaking, or resistor-switch pairs to set the gain of the TIA. The HUBEO+ project targets a network based on multiple-writer single-reader links. Therefore, in addition to the demands of low power consumption and small footprint, the TIA is also required to accept a wide range of optical input powers, because different tunings of the multiple writers may vary the received average input power at the receiver, see Fig. 4.1. Recent receiver topologies address this problem by adding a feedback loop around the TIA that steers a current source in parallel with the TIA in order to keep the DC current flowing through the TIA equal to zero. This approach is very robust but adds further input capacitance to the receiver input which defines the limiting pole. Hence, in this work a TIA is presented that accepts a high range of DC input current without adding any further component to the input node. The optimal parameters for a basic TIA running at 8 Gb/s were taken as a base but they were further developed to account for the new requirement.

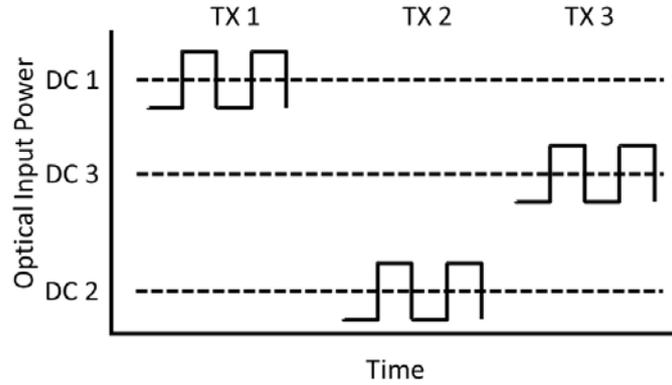


Figure 4.1: Optical signals received from different transmitters

4.2 Optimization for wide I_{DC} acceptance range

It was concluded from the optimization that the single-stage push-pull topology is the most power efficient solution in the frequency range around 10 GHz for an input capacitance of 20 fF. Further requirements are defined by the project, such as the demand for the receivers's optical sensitivity to be -18 dBm, which is equal to an input current of $-13 \mu\text{A}$, if a photodiode with a responsivity of $0.8 \frac{\text{A}}{\text{W}}$ is assumed. The designed receiver, including this TIA, discussed in chapter 5, will feed the output of the TIA into comparators that have a sensitivity of 15 mV. Accordingly, the TIA needs to have a minimal transimpedance of 2.3 k Ω . The TIA with the following parameters, taken from the optimization database, accounts for all these requirements:

Requirements:		
Bandwidth	Transimpedance	C_{PD}
7.7 GHz	2.3 k Ω	20 fF
Component Sizes		
W_N	W_P	R_F
1.4 μm	3.2 μm	3 k Ω
Performances		
Power Consumption	IRN	
26 fJ/b	0.3 μA_{RMS}	

The bandwidth of 7.7 GHz was deliberately chosen higher than needed for an 8 Gb/s system, as this data is based on schematic simulations and a drop of around 10% has to be expected due to additional parasitic loads after layouting.

This conventionally sized Push-Pull TIA (i.e. with the PMOS transistor about two times larger than the NMOS) is optimally operating if no DC current is flowing through the feedback resistance, i.e. when both input and output DC voltages

are equal. Without an input bias source that suppresses the average photodiode's photocurrent (I_{DC}), a DC current will flow through the TIA. This current would displace the biasing point of the TIA to a non-desired operation point with very low transimpedance, due to the current induced voltage drop over the feedback resistor.

However, this work proposes to optimize the PMOS/NMOS ratio to achieve a proper operating point for a non-zero I_{DC} . Therefore, the transistor ratio should be sized so that the TIA is optimally biased with the most likely I_{DC} running through it. Nevertheless, changes in I_{DC} will still induce unwanted changes in the biasing condition of the circuit. This includes a higher voltage drop over the feedback resistor, leading to a smaller g_{ds} and rising/falling saturation voltages in the PMOS and NMOS transistors, respectively. This interplay leads to a rising bandwidth with I_{DC} but a falling gain. An obvious improvement of the system is therefore to replace the feedback resistor by a transistor working as a controllable resistance. The gate voltage of the feedback transistor (V_{FB}) can now be used as a tuning knob to counteract the effects of varying I_{DC} currents. The new TIA schematic is shown in Fig. 4.2.

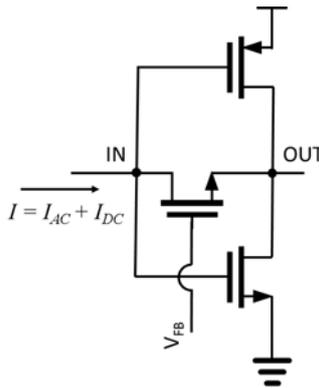


Figure 4.2: Schematic of the designed TIA with active resistor feedback

The final design of the TIA has the following parameters:

Component Sizes		
W_N	W_P	W_{FB}
1.8 μm	1.8 μm	0.8 μm
Performances		
Power Consumption	IRN	$\Delta_{acc}I_{DC}$
38 fJ/b	$< 0.9 \mu\text{A}_{RMS}$	0 to 40 μA

, W_{FB} represents the width of the NMOS feedback transistor and $\Delta_{acc}I_{DC}$ the accepted range of DC input currents. All transistor lengths are of minimal length, i.e. 65 nm, because there is no exact matching between components needed.

Fig. 4.3 shows the transimpedance and the bandwidth of the TIA depending on I_{DC} . These results were obtained by transistor level simulations. In a non optimized

but conservative approach [55] a factor 1.2 should be chosen between bit rate and bandwidth, hence the required BW should be 6.7 GHz. With these requirements, $BW = 6.7$ GHz and $T = 2.3$ k Ω , a static setting of $V_{FB} = 0.8$ V would allow a working range of I_{DC} from 10 μ A to 38 μ A. It is only the possibility of changing V_{FB} to 1.1 V that allows extending the working range down to 0 μ A.

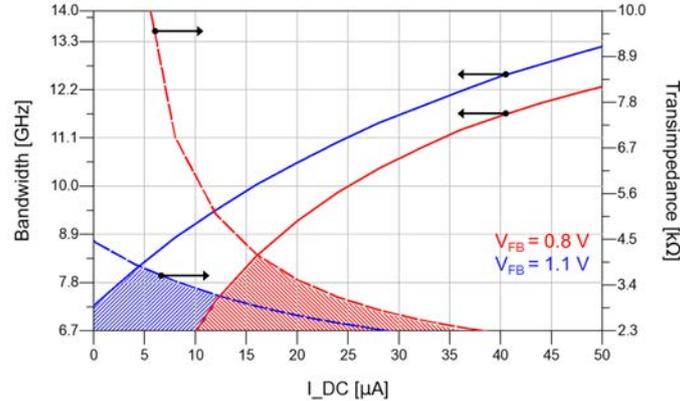


Figure 4.3: Simulated transimpedance and bandwidth dependence on I_{DC} and V_{FB}

4.3 Layout Considerations

During the layout of a circuit, it is inevitable to introduce parasitic capacitance and resistance. There are often trade-offs to be made between the parasitic capacitance and the parasitic resistance introduced to the circuitry. For example, it is always possible to use a low metal layer close to the bulk of the chip, which will be the shortest connection between two components and therefore the one with the least resistance. On the other hand, going to higher metal layers increases the distance between the bulk (i.e. the ground) and the line and therefore allows reducing its parasitic capacitance to ground. Hence, depending on the circuit there is an optimal layout to be found.

An important parameter in the transistor layout is the amount of used fingers. Alternative layouts are shown in Fig. 4.4. While the effective transistor width is the same in both cases, the overall metal used for the source and drain is less in the three fingers case. On the contrary the amount of poly silicon used for the gate is larger in the three finger case. If the maximal bandwidth for a single transistor is studied, an optimal finger width of about 800 μ m is found. If this transistor is part of a bigger layout-sensitive design though, other width might be optimal.

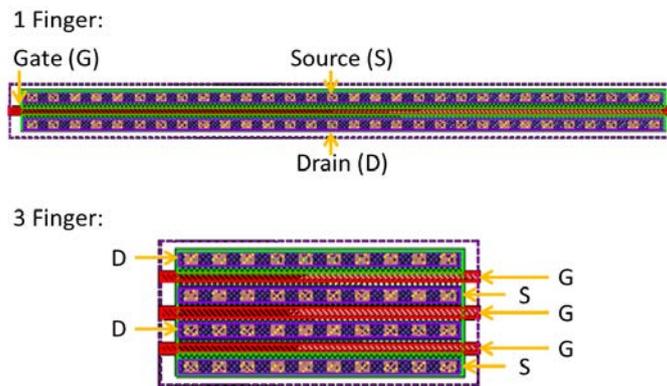


Figure 4.4: Layout of the same transistor with different amount of fingers

The layout chosen for the TIA is presented in Fig. 4.5. To achieve the most compact design possible each transistor was cut in two halves. This allows an H like distribution path of the input signal (purple central line) routed in metal 1. The H like distribution allows short symmetrical connections from the central injection node to all fingers of the transistors. The same argument holds for the routing of the output (green central line) routed in metal 4. Further shrinking of the circuit could have been possible but only by modifying the standard cells of the transistors, leading to insufficient simulation accuracies. For the PMOS and NMOS a 10 finger layout was chosen. The TIA is $4 \mu\text{m}$ wide and $10 \mu\text{m}$ high; therefore it fulfils very well the requirement of small footprint.

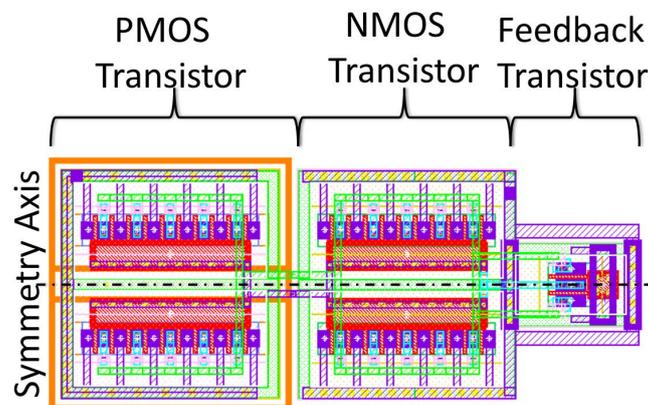


Figure 4.5: Layout of the designed TIA

4.4 Characterization

The designed TIA was fabricated in ST's 65nm CMOS process. In order to characterize the TIA's performances it was fabricated in two versions. A first version

including a photodiode emulation front-end and a second front-end with direct connection of the TIA's input to a bonding pad. The latter version has been bonded to an external photodiode in order to verify the final functionality. Furthermore, the TIA has been optimized for a purely capacitive output load of 10 fF. It is therefore necessary to buffer its output to measure it outside the chip with 50 Ω environment equipment.

4.4.1 Electro-Electro Test

The electronic-input to electronic-output test setup is important because in this case the TIA's environment is controllable. The input capacitance in this case was designed to be the same size as expected from a photodiode built in a silicon photonic interposer onto which this circuit is flip-chipped and bonded using cu-pillars.

Front End

The schematic of the designed photodiode emulation front-end is shown in Fig. 4.6. The signal is injected into the channel with an external signal generator connected by on-chip probing pads. The pads are 50 Ω terminated and DC decoupled from the rest of the circuitry by a 10 pF in-series capacitor. The injected signal will be a voltage signal. To convert the signal into current an in-series resistor of 10 k Ω is used. As this TIA was designed for a wide DC current acceptance range, the DC current needs to be controlled to test this ability. To do this, an SPI controlled DAC injects currents from 0 μ A to 50 μ A into the input signal. A further DAC generates V_{FB} in the interval of 1.0 V to 1.4 V. A small minimal sized NMOS transistor is connected to the input node of the TIA to bind the input signal to ground if the TIA is not used. The signal B_{ON} is controlled by the on-chip SPI registers. This is done to stop the TIA from consuming power when it is switched off; this frees the V_{DD} net for power measurement for several connected TIAs. The parasitic capacitance, acquired by post-layout parasitic extraction, of all of these components equals 5 fF and is assumed to emulate the parasitic capacitance of the photodiode.

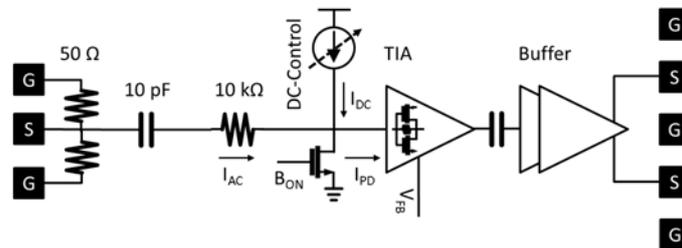


Figure 4.6: Implemented electro-electro TIA characterization channel

The output of the TIA is equally DC decoupled to allow optimal biasing conditions for the following buffer. Fig. 4.7.a and b show the layout of the channel. The overall added input capacitance equals 5 fF.

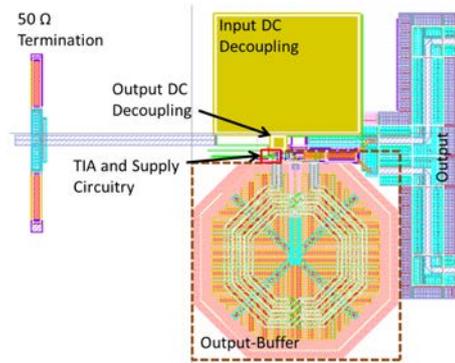


Figure 4.7.a: Layout of the electro-electro TIA characterization channel

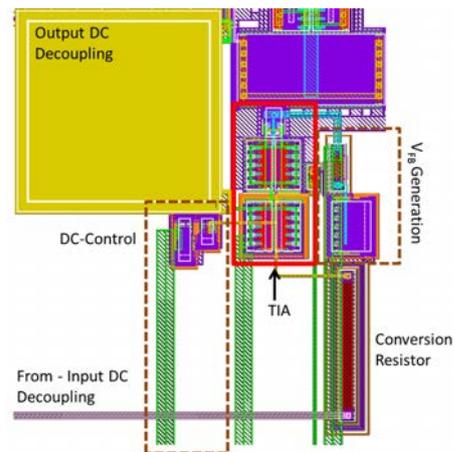


Figure 4.7.b: Layout of the TIA surrounding circuitry

Buffer

The probing pads need to be in a Ground Signal Ground configuration to grant impedance matching from the buffer output to the measuring device. Therefore, and due to their size, they represent a high capacitive load of 50 fF. Additionally, the measurement probes present further loading to the output of about 15 fF. To have some margin, the load of the output was assumed to be 75 fF. This load is a factor 7 higher than what the TIA was designed for. Moreover, in order to measure high frequency signals, all cables and devices are terminated at 50Ω , which would also render the TIA non-functional. Accordingly, a buffer is needed to output the TIA's signals. The requirements are an input capacitance at the order of a few fF and the capability of driving the mentioned loadings. The bandwidth of the buffer must also succeed the TIA's maximal bandwidth if no de-embedding techniques shall be used. To have enough headroom, 15 GHz was chosen as bandwidth requirement.

The chosen architecture is based on a differential Cherry-Hooper amplifier with inductive peaking and an fT doubler taken from [56], as shown in Fig. 4.8.

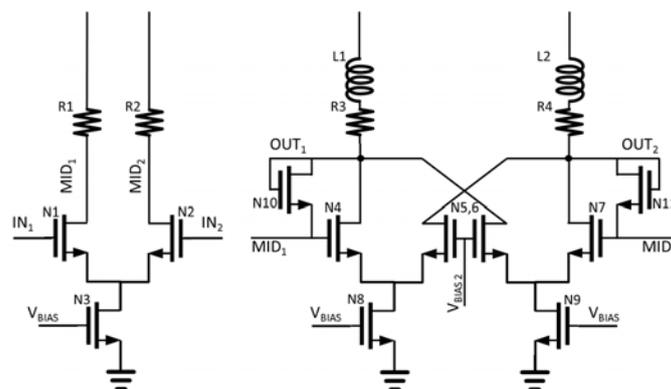


Figure 4.8: Implemented output buffer

The element parameters are the following:

Transistors					
Group N:	1,2	3	4,5,6,7	8,9	10,11
Width [μm]	10	90	40	360	160
Length [nm]	60	120	120	120	120
Resistors					
Group R:	1,2	3,4			
Resistance [Ω]	600	50			
Inductors					
Group L:	1,2				
Inductance [nH]	2.1				

The buffer was also capacitively decoupled from the TIA, presenting in sum an output loading of 16 fF to the TIA. It reaches a bandwidth of 15 GHz and a single-ended gain of 1.1 in post-layout simulations, see Fig. 4.9. The buffer consumes 28 mA if it is loaded with 50 Ω and correctly biased.

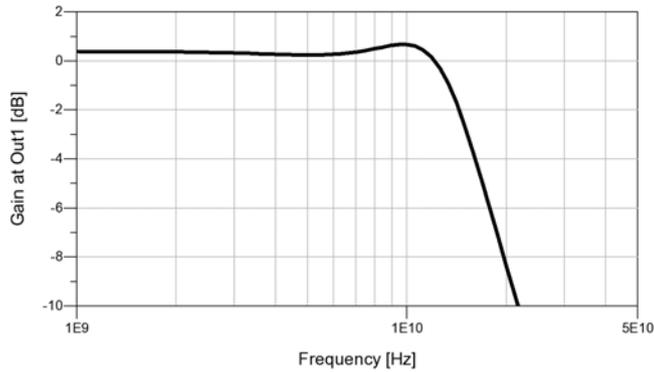


Figure 4.9: Gain roll-off of the designed buffer in post-layout simulation

The layout of this double stage differential amplifier needs to be very carefully done, as local process variation induced component mismatch would otherwise degrade the buffer's performance severely. Therefore, all transistors composing differential pairs, are laid out with a common centroid strategy, so that possibly appearing gradients on the chip have less impact on the circuit. Fig. 4.10 shows the layout of the transistors; the inductor is not shown as it is several times bigger than the transistors. As this buffer consumes a lot of current, the sizes of all components have to be designed with respect to electromigration. This is the reason why the 50 Ω resistors are 2 μm wide.

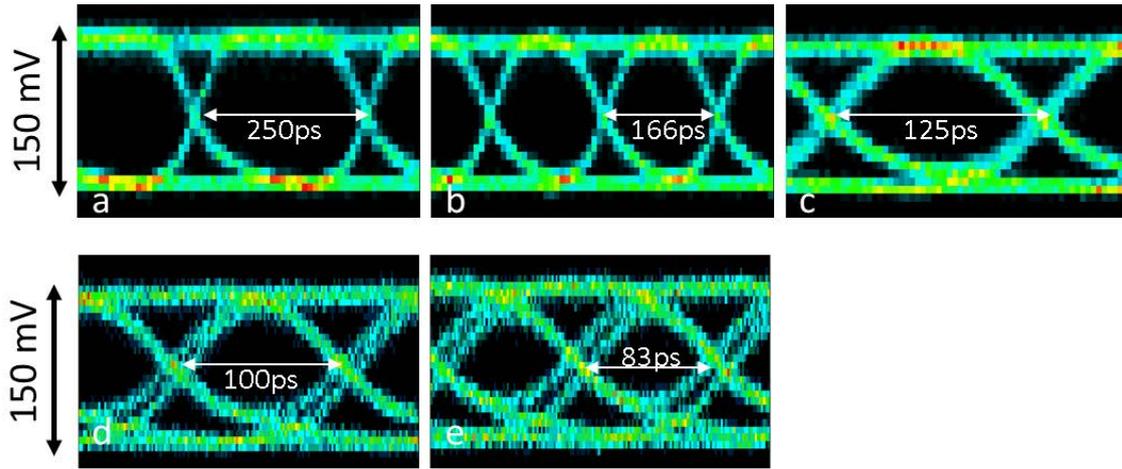
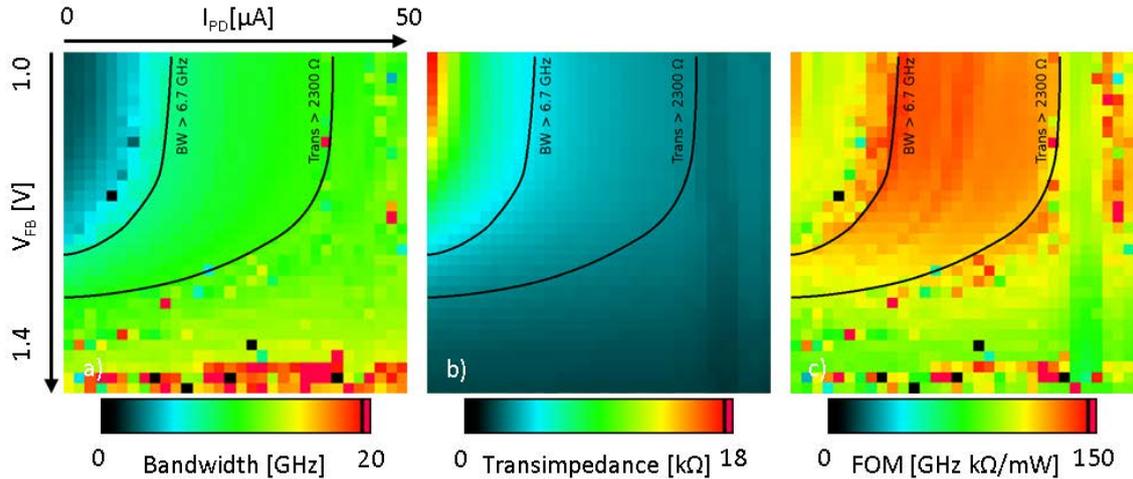


Figure 4.11: Measured eye diagrams

To demonstrate the use of V_{FB} to widen the I_{DC} range where the TIA presents acceptable performance, the measurements of bandwidth, transimpedance and FOM were mapped for a wide range of V_{FB} and I_{DC} values (see Fig. 4.12.a-c). The black lines on the maps indicate the areas where the TIA fulfils the minimal requirements of a bandwidth superior to 6.7 GHz and a gain superior to 2.3 k Ω . For the lower range of V_{FB} values, the TIA is functional in a wide range of average input currents, centered about 20 μ A. Moreover, if dynamic control of V_{FB} is implemented, the range spans 0 to 40 μ A, using V_{FB} from 1.4 V to 1.0 V. It is also noteworthy that the best FOMs for the TIA are found within the indicated boundaries.

Figure 4.12: Mapped performances on V_{FB} and I_{DC}

4.4.2 Opto-Electro Test

To verify the produced TIA as an optical receiver front-end, it was bonded to an external germanium photodiode. This step has to be understood as a purely functional verification as the TIA was not designed for high input capacitances introduced by the bonding and long internal connections from the TIA to the bonding pads.

Front-End

The front-end for the electro optical test comprises only the V_{FB} generation circuitry and the transistor to bind the input to ground. The generated I_{DC} can be controlled with the injected light levels or more precisely with the extinction ratio of the signal. To bring the photodiode signal to the TIA with as few losses as possible, microstrip lines were implemented from the bonding pads to the TIA input, as shown in Fig. 4.13.

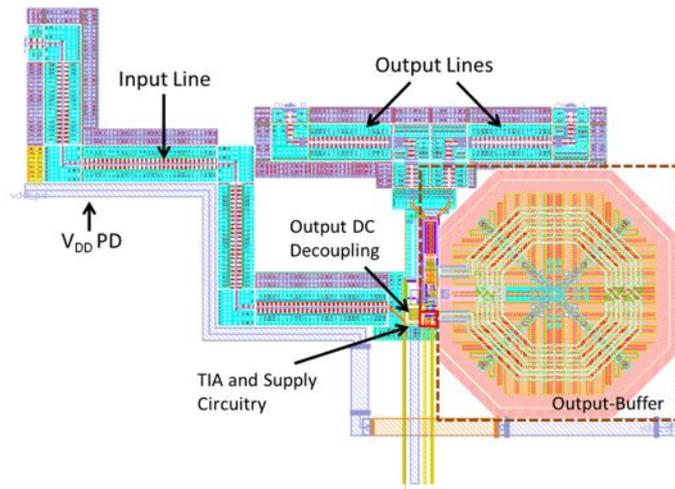


Figure 4.13: Layout of the opto-electro TIA characterization channel

The front-end alone presents an input capacitance of 22.3 fF to the TIA. The bonding wires on the used sample are about 550 μm long and add a further capacitance of ≈ 3 fF. Finally, the photodiode adds 8 fF of input capacitance. With the full input capacitance of 33 fF presented to the TIA, only bandwidths a factor 2 smaller compared to the electro-electro channel characterization can be reached.

The output buffering of the TIA stays the same as for the electro-electro characterization channel.

Measurement Setup

The used measurement setup strongly resembles the setup mentioned earlier. The chip was connected using a G-S-G-S-G RF probe for the output signals and a single mode fibre injected the light signal into a grating coupler on the substrate of the

photodiode. The wire bonded photodiode had a measured responsivity of 0.2 A/W (including losses at the grating and in the waveguide).

To record eye diagrams, a random bit generator with a pattern length of $2^{12} - 1$ was used. The output was connected to a sampling oscilloscope. The connected chip photodiode assembly is shown in Fig. 4.14. In the south the DC probe for the SPI control and most supply voltages is visible, in the west is a further pair of probes supplying another V_{DD} , at the north side the used G-S-G-S-G RF probe is visible and in the east the fibre for the optical input can be seen.

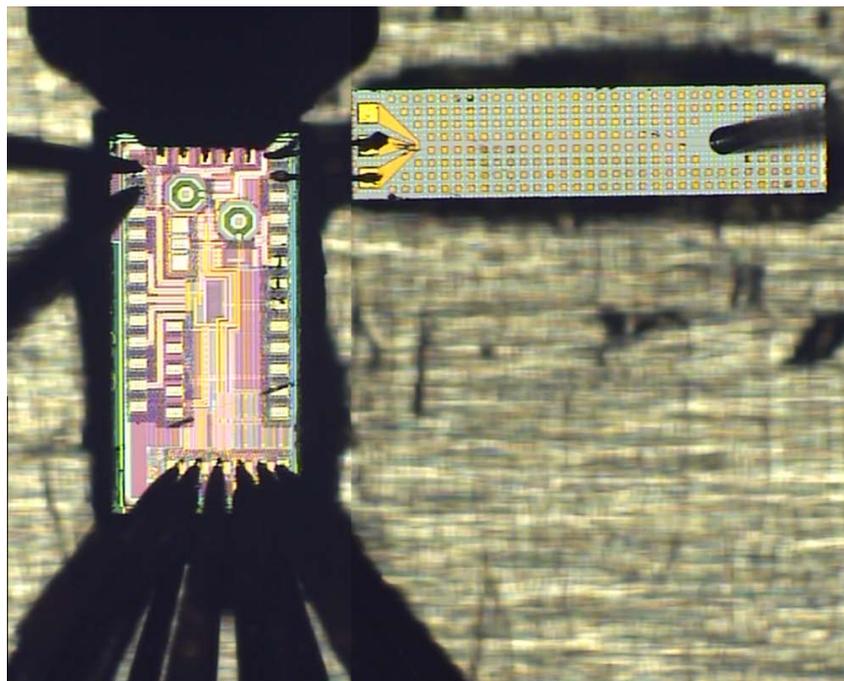


Figure 4.14: Picture of the connected chip photodiode assembly

Results

As mentioned before, the expected bandwidth of this setup is considerably lower than for the electro-electro test, hence only eye diagrams of 2.6, 4 and 5 Gbps could be measured. The first row of Fig. 4.15 shows the corresponding eyes for $V_{FB} = 1.2$ V and the second row for $V_{FB} = 1.4$ V.

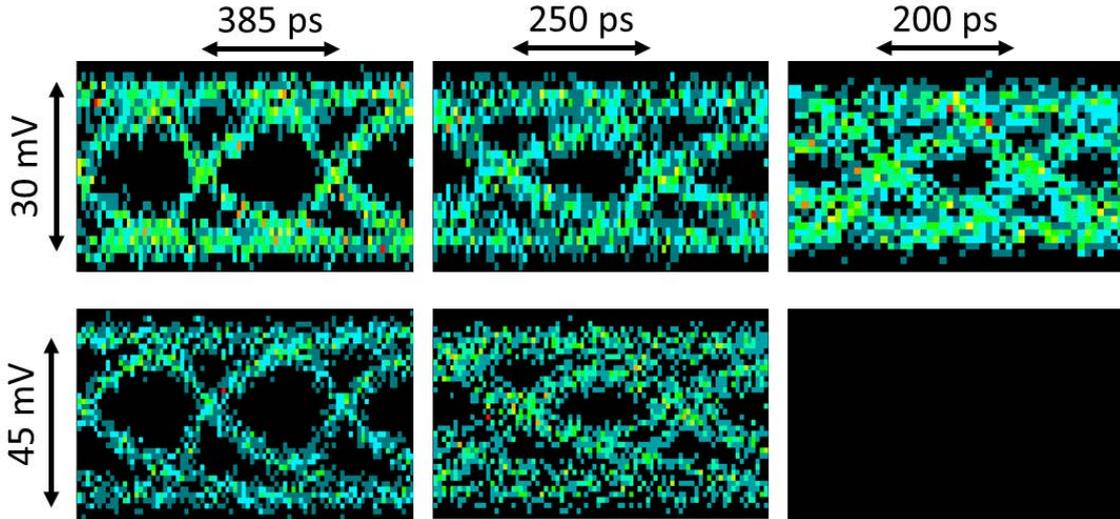


Figure 4.15: Measured eye diagrams of the opto-electric test setup

The measured eyes at up to 5 Gbps prove the functionality of the TIA also in the optical domain. Furthermore, it could be verified that the mechanism to change the transimpedance of the TIA is functional.

4.5 Conclusion

A low-power low-footprint TIA was presented accepting a wide range of DC input currents, which is very important if it is used in multiple-writer single-reader links. The wide acceptance range was achieved by introducing a transistor as feedback element and using its gate voltage to compensate for DC current introduced changes in the TIA's biasing conditions.

The TIA was characterized with a photodiode emulation and compares very favourably (using these data) with other state of the art solutions as can be seen in the following table, where LA denotes solutions using limiting amplifiers as a second stage:

Ref, Tech	Topology	T [dBΩ]	BW [GHz]	P_{DC} [mW]	Area [$\mu m \cdot \mu m$]	FOM [THzΩ/mW]	C_{IN} [fF]
[27] 130nm	TIA + LA	75	25	30	252 · 147	4.6	20
[34] 65nm	TIA + LA	79	11	25.3	470 · 80	3.8	380
[57] 40nm	TIA + LA	72	7	2.53	-	8.8	60
HERE 65nm	TIA	85-60	1.7 - 17	0.26	10 · 5	150	5

The TIA's functionality was also verified using a bonded photodiode. The TIA introduced in this thesis constitutes the front-end of the optical receiver that will be explained in the following chapter.

Chapter 5

The Receiver

“Never was anything great achieved without danger.”

Niccolo Machiavelli

5.1 Introduction

A complete receiver for silicon photonics based high speed links in 65nm technology was designed, fabricated and characterized. The receiver is using the TIA presented in the previous chapter as its front-end. Therefore, it was designed for a bit-rate of 8 Gbps, an input sensitivity of $13 \mu\text{A}$ and a bit error rate of 10^{-12} . It was furthermore required to deliver a parallel data output at 2 Gbps. The HUBEO+ project moreover incorporates a dedicated optical clock channel. Accordingly, the receiver assumes an external clocking signal and does not incorporate a clock data recovery system.

The receiver architecture is shown in Fig. 5.1 as a block diagram. This architecture was already the basis for the optimization in chapter 3. In the first stage the photodiode is connected directly to the TIA (blue) without any current biasing circuitry. The implications of this choice are discussed in the Threshold Control Block section 5.4. The TIA feeds the signal into a bench of comparators (red) used for decision making and deserialization of the data stream. The comparator needs a second voltage (threshold voltage) to which the TIA signal is compared in order to make its decision. This signal is generated in the Threshold Control Block (green). The deserialization is done by time shifted triggering of the comparators realized by the clock phases ϕ_1 to ϕ_N . In order to achieve a true parallel output the comparators are followed by a bench of flip-flops.

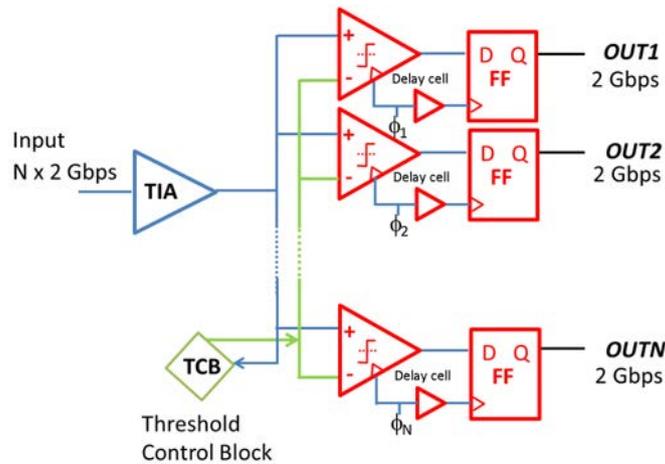


Figure 5.1: Basic architecture of the developed receiver

It was argued that this architecture is the most adapted architecture to the problem of optical links for systems in package because the data has to be serialized and deserialized at the beginning and end of the link. The architecture is efficient because the deserialization and decision making is done in the same stage. Furthermore, parallelizing the decision stage does not increase the energy per bit figure of merit as long as the increased load of the TIA does not lead to a more power consuming TIA. In addition, it allows easy scaling for different bit rates which helps porting developed blocks to other technologies. Finally, due to the minimal amount of elements in the receiver it is very compact.

This chapter will first discuss the designed comparators for the 65nm as well as for the 28nm technology. An entire receiver could be developed only in 65nm, all further sections of this chapter cope therefore only the developments in 65nm. These include the strategic Threshold Control Block. Afterwards the schematics of the full receiver, its layout, the measurement setups, the simulation schemes and finally the obtained results are presented.

5.2 Comparators

Comparators are strongly non-linear differential amplifiers. In systems that code the informations in a binary form, like non-return to zero codes, comparators are often used to convert a signal from the analogue, small signal domain into the digital, large signal domain. This is why they are used in the so called “decision stage” of receivers.

The figures of merit for comparators regarding their functionality are the same as for any other differential stage. The first figure of merit is their speed. Depending on the implementation the speed can be expressed as the comparators bandwidth. A more general parameter is comparisons per unit of time. The second figure of

merit is the comparators sensitivity which is the minimal difference of the input signals needed to acquire a correct full swing output. This parameter can be translated into offset for differential stages, but can be influenced by various parameters depending on the implementation. The third figure of merit is the comparator's power consumption. An implementation independent value is the power consumption per comparison. A final measurable property is the footprint of the comparator. Another property to consider, when choosing a comparator, is their implication on the preceding circuitry. First of all it has to be considered whether the system, in which the comparator is used, can serve a clock or whether it has to be generated just for the comparator. A further implication is the kick back noise. Due to the fast full swing transitions inside comparators, voltage peaks can travel into earlier stages and distort the signal.

There are three basic comparators topologies with some variations. The classical approach uses a pair of cross coupled transistors to compare small currents with each other [58] (see Fig. 5.2). This topology needs at least one more stage to generate the input currents and a further stage to generate the full swing output after the cross coupled pair. It is therefore rather large and power consuming, but it generates continuously the comparison result.

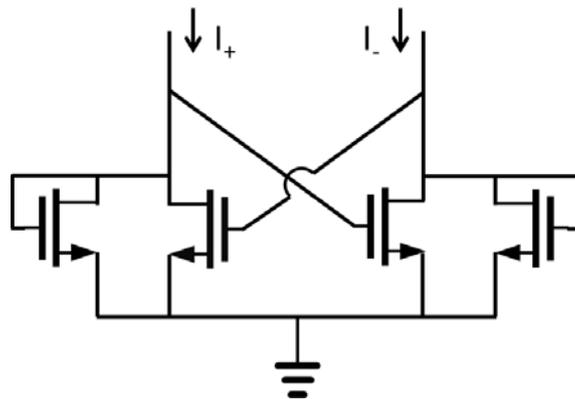


Figure 5.2: Comparator based on a cross-coupled transistor pair

A second solution is shown in Fig. 5.3. It is based on a self-calibrated inverter [47]. The comparator is balanced closing switch S3 and S2, so that the threshold voltage V_- is stored in the capacitor. In comparison-mode S3 and S2 are open and S1 closed which will unbalance the inverter depending on V_+ . The voltage reference information is therefore stored on C1 and needs periodic re-calibration.

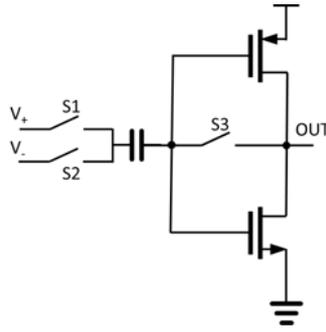


Figure 5.3: Comparator based on a self-balanced inverter

The third topology is shown in Fig. 5.4. This design is based on a sense-amplifier [46]. The input stage, a differential pair, steers the latch into the corresponding state. As a latch will remain in its state, this solution needs a clock to trigger the comparison at the right moment and to reset the latch.

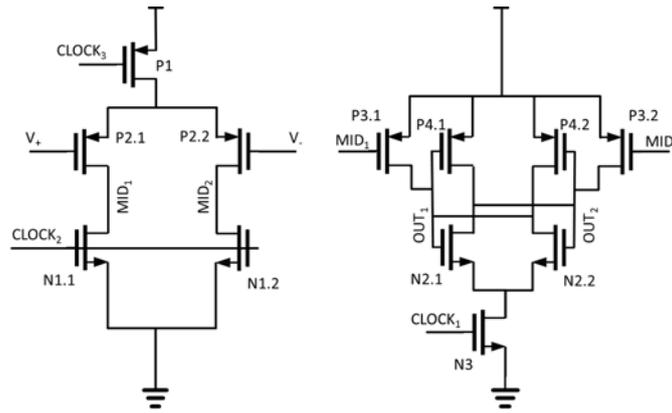


Figure 5.4: Comparator based on a latch

To decide which topology to use for the receiver the performances from recent publications were collected and depicted in the following table (the cross coupled pair was designed in schematics to compare it to the other solutions):

	Cross Coupled	Self-Biased Inverter	Latch-Type
Speed [GSps]	10	2	4
Sensitivity [mV]	50	5	10
Consumption [fJ/S]	200	20	100
Consumption [$(\mu m)^2$]	$\gg 100$	≈ 100	≈ 100

The latch-type comparator compares well with the other solutions. Moreover, the deserialization can be integrated into this stage without any need for further pass

gate or other signal steering circuitry. For these reasons, the latch-type topology has been taken as basis to develop the receiver's comparators.

5.2.1 Design

The design of the comparators for the receiver stayed very close to the comparator presented in [46], with two major modifications. The comparator was mirrored with respect to the N-/PMOS flavours of the transistors to adapt it to common modes below $\frac{V_{DD}}{2}$. This was necessary as the receiver was optimized for DC Currents running through the TIA, pushing the average output signal below $\frac{V_{DD}}{2}$. A further variation is the optimization of the supplied clock signals. While in [46] $Clock_2$ and $Clock_3$ are equal and represent the inverted $Clock_1$, they are independent in this design and instead of having a duty cycle of 50% a duty cycle of 25% , or respectively 75% was used, as shown in Fig. 5.5. To understand the benefit of this variation the signals development should be further explained. In the initial stage the latch and differential stage are switched off and OUT_1 and OUT_2 are connected to V_{DD} , while MID_1 and MID_2 are connected to ground. The rising edge of $Clock_1$ and the falling edge of $Clock_3$ trigger a comparison by powering on the latch and differential stage. After the switching the rise times of MID_1 and MID_2 depend on the input voltages V_+ and V_- of the comparator. This difference in rise time binds OUT_1 and OUT_2 longer, or respectively shorter, to V_{DD} which decides which arm of the latch goes down to ground and which stays at V_{DD} . The 75% duty cycle of $Clock_1$ allows now longer settling times for the output signal which relaxes the timing demands for the following stages. The independence of $Clock_2$ and $Clock_3$ is beneficial because $Clock_2$ triggers the reset of the comparator. It can therefore only go high in the last 25% of the period. On the other hand it is advantageous if $Clock_3$ rises earlier to stop the differential stage before MID_1 and MID_2 settle at V_{DD} .

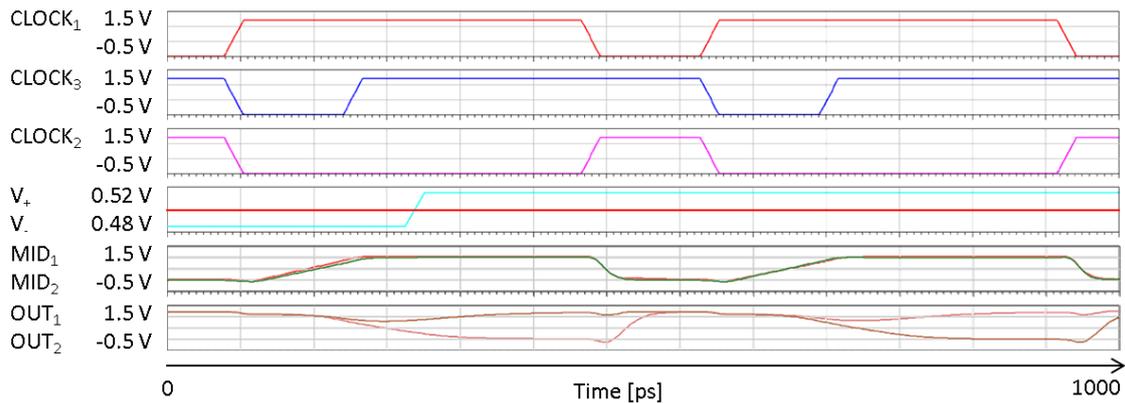


Figure 5.5: Waveforms inside the comparator

The designed comparator has the following transistor properties:

Transistor	P1	P2	N1	P3	P4	N2	N3
Width [μm]	1.5	3	0.5	1.5	0.25	0.25	1.5
Length [nm]	90	180	60	180	180	180	120

Offset Reduction techniques

To determine the main contributor to the degradation of the receiver's sensitivity two sweeps were performed. The first sweep, shown in Fig. 5.6.a, is a series of transient simulations including time domain noise. The error count after transmitting 100 bits is 0 if the swing exceeds 3 mV. In a second sweep the impact of mismatch was tested. Shorter transient simulations (10 bits) were performed coupled to 100 different Monte Carlo mismatch configurations. The mean error counts are shown in Fig. 5.6.b. In this case the error rate is still in the range of 10 % even at an input voltage swing of 15 mV. The noise has therefore a negligible impact on the comparators sensitivity.

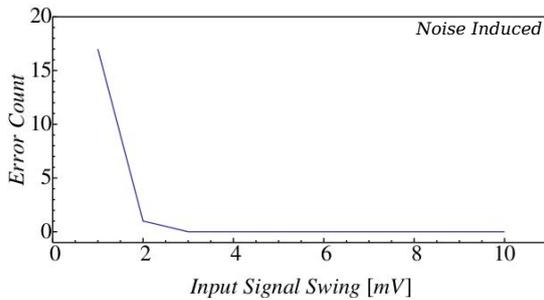


Figure 5.6.a: Error count in transient simulations comparing 100 bits, including time domain-noise.

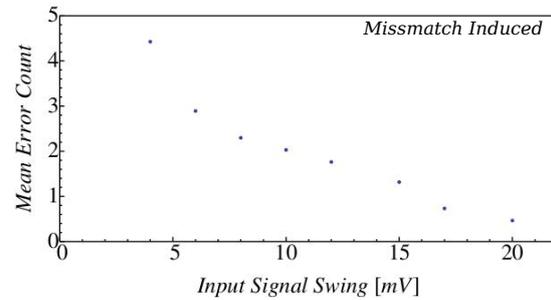


Figure 5.6.b: Mean error count of 100 Monte Carlo transient simulations each comparing 10 bits

As process variations only introduce mismatch between elements, calibration circuitry can be used to increase the sensitivity of comparators. In this case configurable loads have been chosen to balance the latch to slow down its stronger arm. The circuitry in Fig. 5.7 is connected to the outputs of the comparator and steered digitally by an external register.

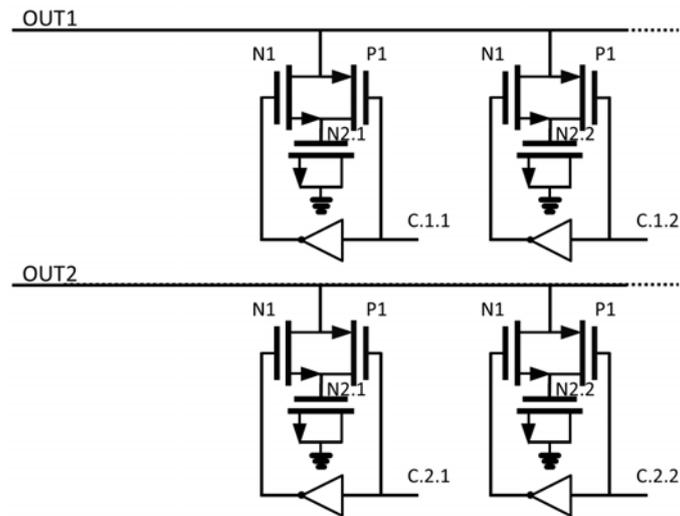


Figure 5.7: Loading stage of comparator

The circuit in Fig. 5.7 could be extended for further bits and the calibration resolution could be increased arbitrarily. The comparator's sensitivity could therefore reach its noise limit. Nevertheless, the comparators loading and footprint would increase. Here, a sensitivity of 15 mV was chosen as optimization goal which could be achieved with the 4 bit resolution presented in Fig. 5.7. The used transistor sizes are shown in the table below and the used inverters are minimal sized standard inverters from the library:

Transistor	N1	P1	N2.1	N2.2
Width [nm]	270	270	135	135
Length [nm]	120	120	60	120

To prove the functionality of the offset reduction circuitry 100 Monte Carlo simulations were run. In each simulation 400 random bits were sent into the comparators with a differential amplitude between V_+ and V_- of ± 15 mV. The bit stream had a bit rate of 8 Gbps while the comparator sampled at a rate of 2 Gbps to show the time interleaving possibility. This has been done for all digital settings of the offset reduction circuitry. The results of these simulations are shown in Fig.5.8. Each row represents one setting of the circuitry and each column one Monte Carlo simulation and thus one mismatch configuration. The color represents the amount of errors made within one simulation, black indicates 0 errors while red shows 50 or more errors. As expected, the most error free runs are in the C1:00 and C2:00 setting and therefore in the uncalibrated state. Yet, there are several simulations where the C1:11 is needed for an error free functioning or the C2:11 state. Most importantly, the lowest row shows the minimum of each column, which is always 0.

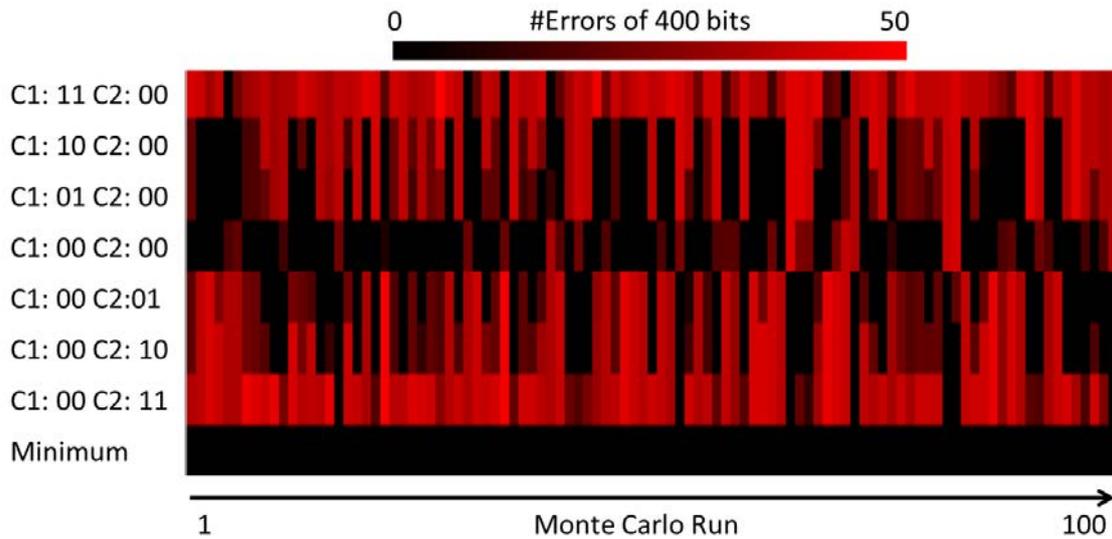


Figure 5.8: Simulated bit errors

5.2.2 Layout

The layout of the comparator is shown in Fig. 5.9. For mismatch reduction purposes the transistors are arranged along a symmetry axis. Additionally, the big transistors P2 are split and assembled in a common centroid orientation. For a minimal footprint, further splitting of transistors was avoided and the transistor flavours were assembled in two blocks. With this layout the comparator occupies an area of $12 \mu\text{m} \cdot 5 \mu\text{m}$.

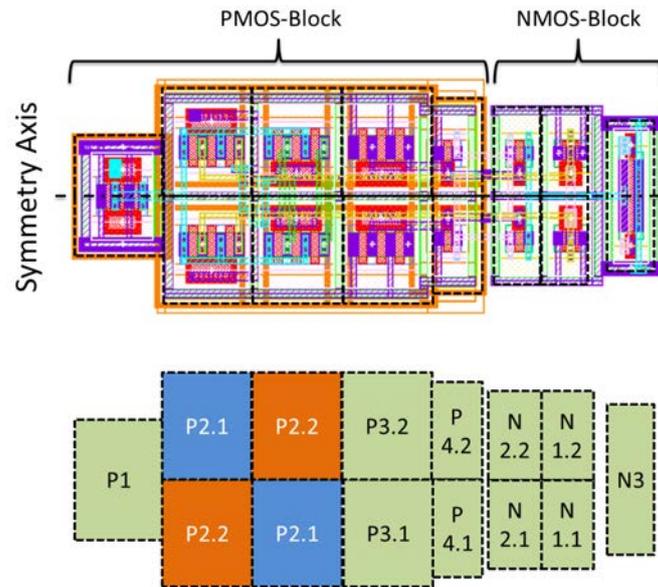


Figure 5.9: Comparator layout and transistor map

Conclusion

The presented comparator is based on the strong positive feedback of a latch, it achieves a comparison rate of 2 Gbps while being able to demultiplex signals higher than 8 Gbps. The achieved sensitivity is 15 mV. It consumes 50 fJ per comparison and occupies an area of $12 \mu\text{m} \cdot 5 \mu\text{m}$.

5.2.3 Advanced Comparator in FDSOI28

A more advanced comparator was developed in the FDSOI 28nm technology. The aim was set to increasing the comparator's sensitivity and decrease its power consumption, instead of increasing its speed. It is used as deserialization stage, hence following digital blocks are unlikely to work faster than 2 Gbps. A benefit of the FDSOI technology is the increased matching between elements due to the lack of dopants in the transistor channel. An increase of sensitivity is thus ensured. It also allows to work with smaller transistor length and width, posing smaller capacitive loadings on preceding stages. The calibration capabilities of the comparator in the 65nm technology were of limited use because each comparator has to be calibrated by hand, based on long test runs. In a receiver design comprising more than 10 comparators and more than 4 calibration bits, this approach is inapplicable. Therefore a self-calibrating comparator was developed, allowing the use of more calibration bits. The developed comparator is based on [59]. The proposed idea in that publication is to short the input signals and balance the two arms until the output signals start alternating. [59] chooses a charge pump to steer the correction signal but here a digital solution was chosen instead. This is beneficial if the start-up time of the

system is a concern, as the calibration values can be stored and directly applied. Moreover, they do not get lost over time. Finally, the digital control block can be used to calibrate all comparators in the receiver.

Fig. 5.10 shows the proposed calibration system. The comparator follows the same schematic as shown in Fig. 5.4, with a new calibration mechanism shown in Fig. 5.11. The inverters Inv2 and Inv3 are used as buffers and to steepen the signal edges after the comparator. The outputs are then fit into the calibration logic, which generates the calibration settings for the comparator and the run signal that steers the switches S1 and S2. The switch S1 shortens the two inputs and therefore S2 needs to disconnect the signal input to not short the rest of the receiver. The threshold input was chosen to define the calibration point because the connected circuitry is more stable and the signal voltage will vary around the decision threshold voltage.

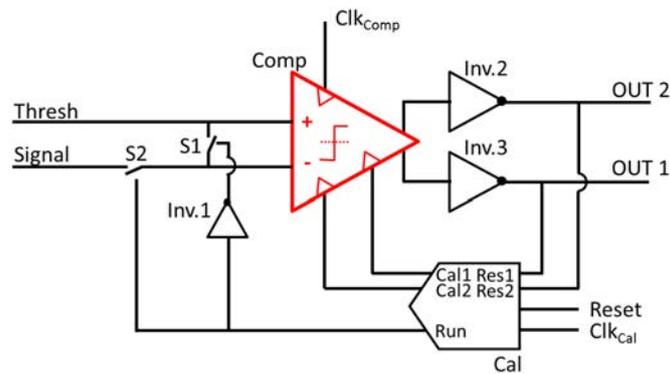


Figure 5.10: Self calibrating comparator with digital feedback loop

The code below shows the verilog code used to describe the calibration logic. After the reset (in the first if case) the calibration registers are empty and the run signal is set to 1. Therefore the comparator inputs are connected together, which should in an ideal world lead to no defined comparison result. However, due to mismatch of the system the comparison will favour one output result. The logic checks at each clock edge the results of the last comparison. If no register is unequal zero or the result of this comparison is equal to the last one, the run signal stays one and the calibration register corresponding to the other arm is increased. If the result changed, the run signal is set to zero and the calibration is over.

```

23 always @(posedge clk or negedge rst_n) begin
24   if (rst_n==1'b0) begin
25     in_cal1<=16'b0;
26     in_cal2<=16'b0;
27     run<=1'b1;
28   end else if (clk==1'b1) begin
29     run = ((~|in_cal1) && (~|in_cal2)) || (((~|in_cal1) && res2)

```

```

|| ((~|in_cal2) && res1)) && run);
30   if (run==1'b1) begin
31     in_cal1<=in_cal1+res1;
32     in_cal2<=in_cal2+res2;
33   end
34 end
35 end
    
```

The old calibration mechanism used for the design in 65nm has the disadvantage of slowing down the comparator. In the new design, for the 28nm technology, the calibration is done by aiding the slower arm instead. In this approach each input transistor P2.1 and P2.2 (marked in red in Fig. 5.11) is shunted with a configurable current source, as shown in the dashed box. Transistor C.P2 is the shunting element to the transistors P2. The mirroring of the currents using C.P1 and C.P2, was chosen to add minimal capacitive loading on the comparator arms.

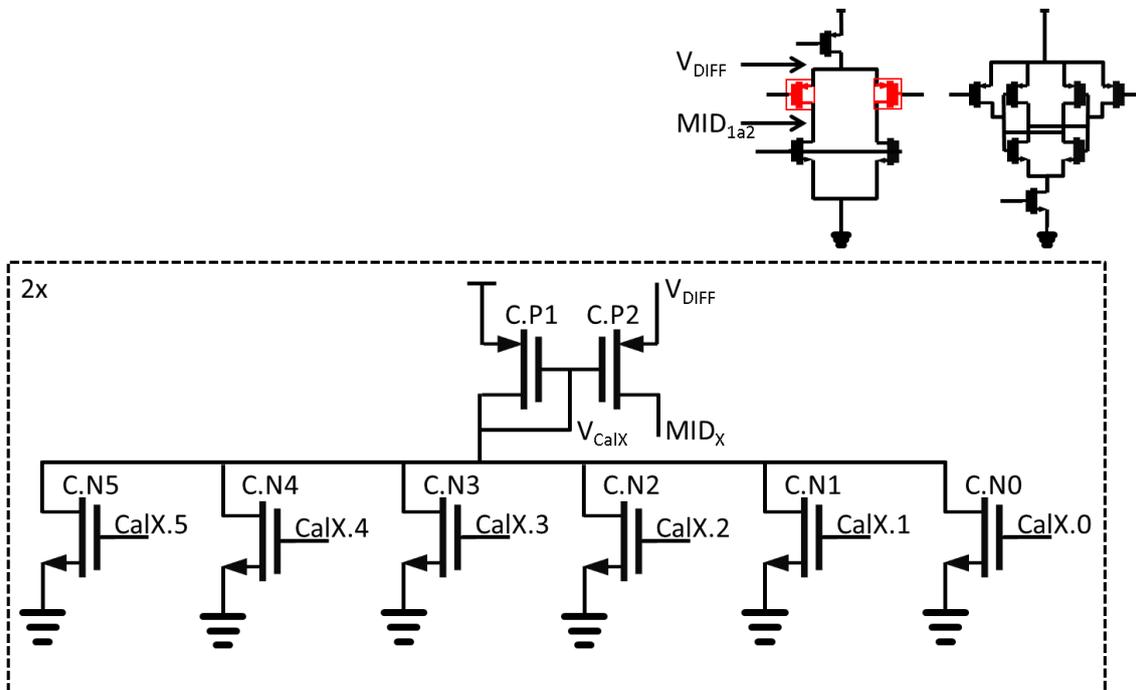


Figure 5.11: Calibration for the 28 nm comparators by balancing input currents

The used transistor parameters in the calibration circuit are:

Transistor	C.P1	C.P2	C.N0	C.N1	C.N2	C.N3	C.N4	C.N5
Width [nm]	80	80	80	160	320	640	1280	2560
Length [μm]	0.12	0.03	5.5	5.5	5.5	5.5	5.5	5.5

The used transistor parameters inside the comparator are:

Transistor	P1	P2	N1	P3	P4	N2	N3
Width [μm]	0.6	0.4	0.1	0.6	0.15	0.15	0.6
Length [nm]	30	30	60	30	60	60	30

Fig. 5.12 shows the transient evolution of the system during calibration. This result was obtained using a transient Monte Carlo simulation. The first two panels show the outputs of the comparator. As expected, during the calibration one output stays low, whereas the other one always rises. The bottom panel shows the rising Cal1 register and the fourth panel shows the dropping V_{Cal1} , that steers the gate of the shunt transistor C.P2. At the end of the calibration Res1 is rising, triggering the Run signal to fall. Now the switches S1 and S2 are flipped and an input signal of ± 5 mV is applied to the comparator. The input signal has the bit pattern 110 that can be found error free on Res1 and Res2.

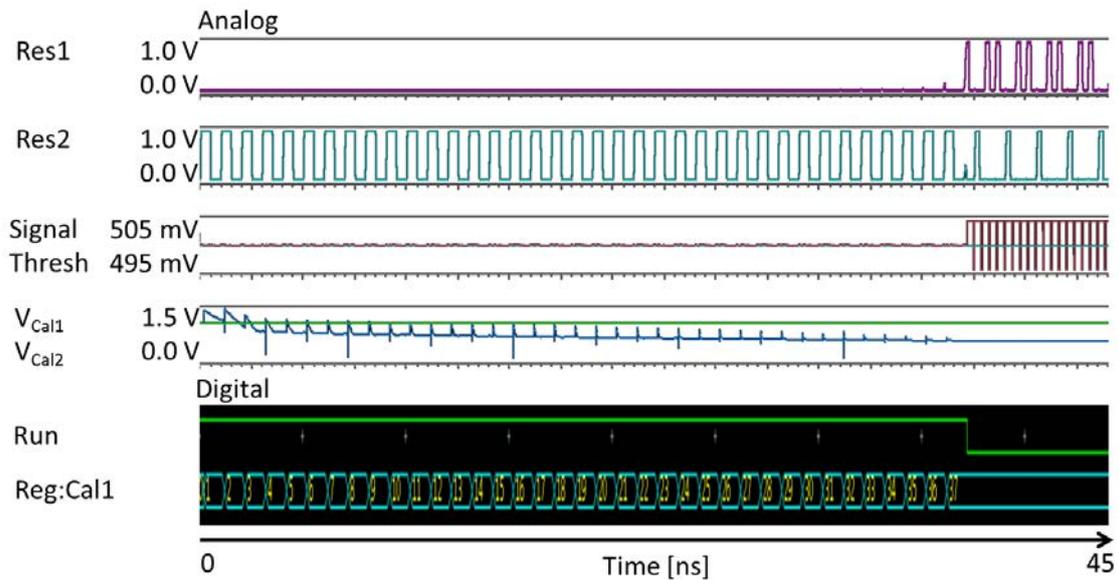


Figure 5.12: Transient evolution during calibration

To demonstrate the functioning of the calibration, Fig. 5.13 shows the rising voltages at the nodes MID1 and MID2, see Fig. 5.4. At the beginning MID1 rises faster leading to the rise of Res2. At the end of the calibration MID2 rises faster because the preamplification stage needs to compensate for mismatch inside the latch, too.

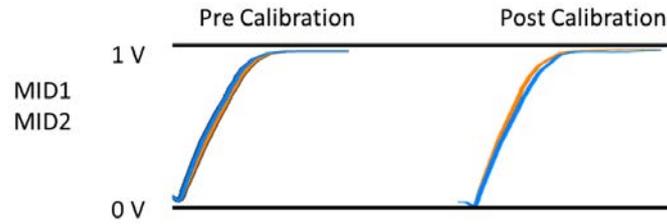


Figure 5.13: Rising voltages at nodes MID_1 and MID_2 before and after calibration

This simulation was part of a series of 100 Monte Carlo simulations that verified the comparators sensitivity of 5 mV. This advanced design consumes in average (as it depends on the calibration currents) 20 fJ per comparison.

5.3 Clock Generation

The comparators fabricated in the 65nm technology need three clock phases, compare Fig. 5.5. All three phases have a duty cycle of 75 % or 25 %, respectively. $Clock_1$ and $Clock_3$ are shifted versions of the same polarity, while $Clock_2$ is the inverted $Clock_1$. There are four comparators working inside the receiver, each 25% shifted with respect to the clock period. Because $Clock_1$ is the $Clock_3$ of the previous comparator, the total number of clock phases is 8 and not 12.

To generate these $4 \cdot 2$ clock phases a 4 GHz clock is injected and buffered in the receiver, see Fig. 5.14. The following stage (2) regenerates the signal and a synchronous but inverted copy. Each of these two signals is fed into separate digital frequency dividers (3), generating two clocks at 2 GHz shifted 90° to each other. The two clock signals are used to produce, again by inverting, (4) clock phases at 0° , 90° , 180° and 270° . Finally, in stage (5) the signals are combined using AND and OR gates to generate the required clock phases for the comparators. In Fig. 5.14 only clock phases for one comparator are sketched.

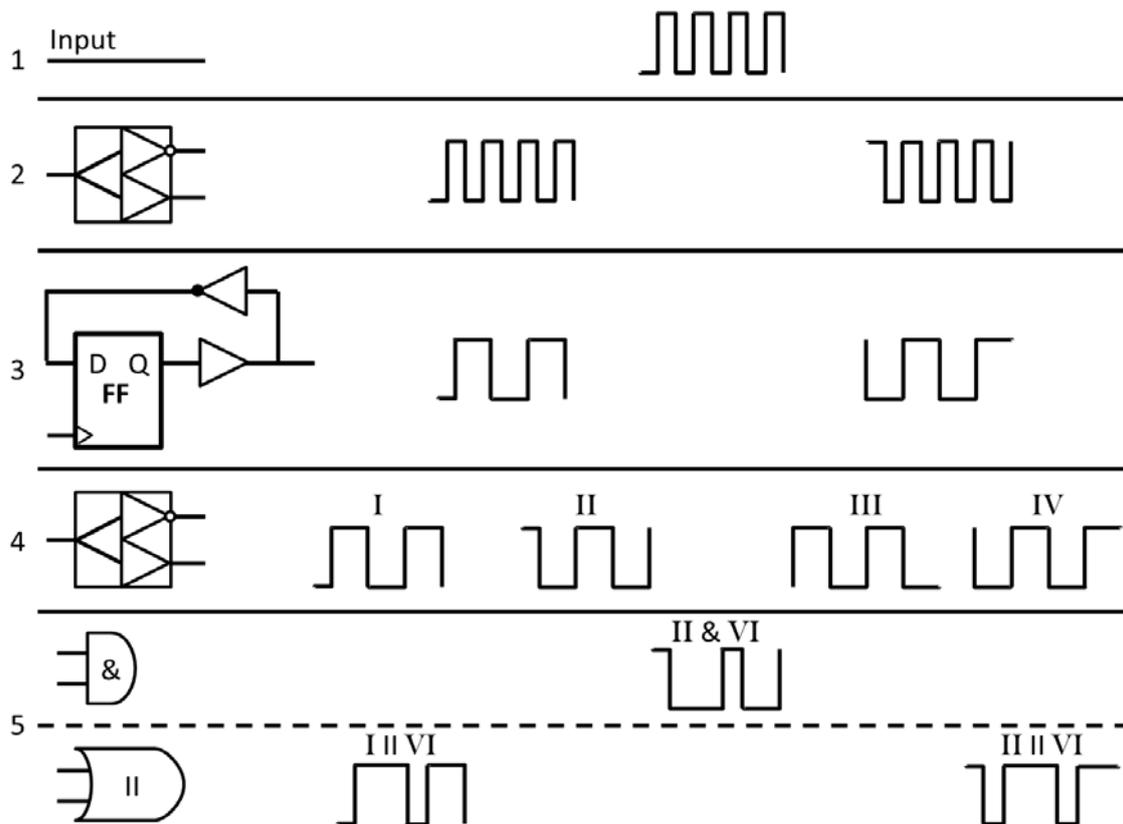


Figure 5.14: Stages generating the needed clock phases

5.4 Threshold Control Block

As already discussed in the TIA chapter, this receiver is designed to work without adding a further current source to the input node. Therefore, the AC and DC part of the photocurrent are running through the TIA. One challenge of this approach is the needed wide DC current acceptance range of the TIA. A further challenge is the increased range of DC output voltages of the TIA. The TIA output is fed into the comparators which require a threshold voltage to make their decision. The task of the threshold control block (TCB) is to generate this threshold voltage from the data stream.

Mathematically spoken, the threshold voltage should be equal to the average of the voltage signal, hence equal to the DC voltage value. Therefore, a basic approach is to use a low pass filter to obtain the DC part of the signal and feed it to the comparators. The problem with this concept is sketched in Fig. 5.15. The low pass filter must be fast enough to react to changes of the optical signal especially when switching the link on (first section of Fig. 5.15). On the other hand, if the cut off frequency is too high, longer sequences of the same bit start to alter the threshold voltage, leading to bit errors (third section of the waveforms in Fig. 5.15).

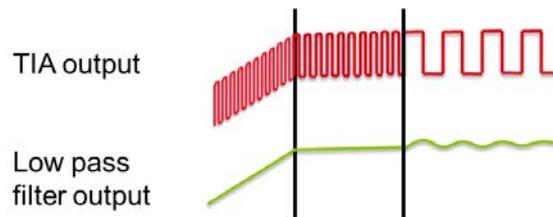


Figure 5.15: Signal development using a low pass filter as TCB

A possibility to break this trade-off is to replace the continuous processing of the data stream for a sampling approach. If a sampling approach is used the problem arising with long sequences of equal bits is solved. In this case, a switch is placed between the TIA output and the low pass filter. A sampling approach needs a defined training sequence, e.g. 101010101010, as it cannot rely on statistics. This training sequence must be as short as possible in order to reduce the data overhead, as it will be send regularly. Fig. 5.16 shows the trade-off inside the sampling approach. This time a low cut-off frequency will lead to long training sequences, and a high cut-off frequency will lead to reduced accuracy. These two effects are amplified by the fact that the training sequences are needed periodically, e.g. before each data packet, and that an inaccurately sampled threshold voltage leads to errors until the next training sequence is received.

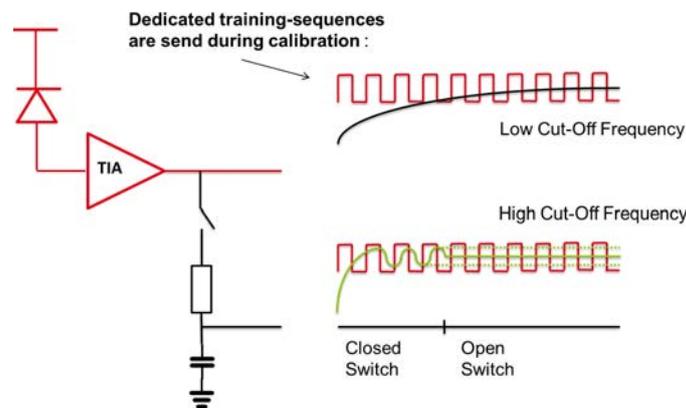


Figure 5.16: Using a sampling approach for the TCB

The final solution, proposed in this thesis, uses two sampling low-pass filters to enable short training sequences without sacrificing the accuracy of the average calculation. Fig. 5.17 presents the idea of sampling twice inaccurately and using the average of these values to obtain an accurate result. Both low pass filters are designed with a very high cut off frequency, i.e. in the final realization the switch and the resistive component are the same transistor, meaning that their output voltages will tend to follow the data signal. The technique works by first sampling

a voltage on C1, second opening S1, third sampling a voltage on C2 and fourth opening S2. At this moment it is important that the opening of S1 and S2 are an odd number of bit periods time shifted, because now (and the absolute timings are unimportant) the errors accumulated on C1 and C2, with respect to the correct average value, are equal in absolute value but different in sign for an alternating 0101 training sequence. The last step is to close S3 which will lead to the wanted averaging process due to the charge redistribution between the two capacitors.

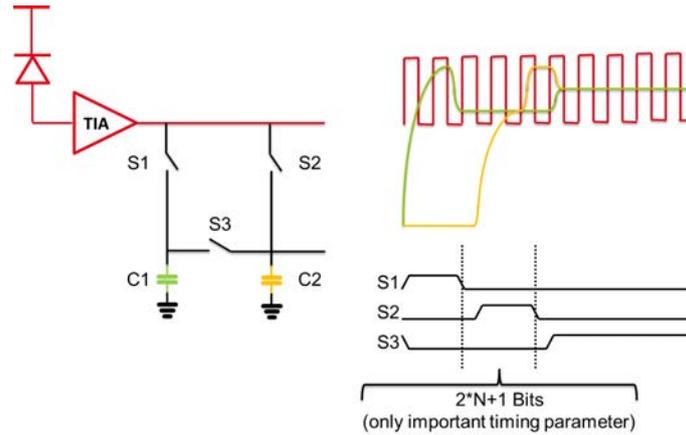


Figure 5.17: Using a double sampling approach for the TCB

5.4.1 Design

The transistor level schematic of the proposed TCB is shown in Fig.5.18. This TCB comprises everything to act as explained above but also features, as alternative, a simple RC low pass filter channel. This allows, if needed, to quickly find the average and then track it steadily. The precision of the average finding mechanism translates directly into the needed TIA output swing and therefore into the receiver's sensitivity. For this reason it is important to consider that switches realized by simple transistors can place further charges on the capacitors due to clock feedthrough, hence decrease the TCB's accuracy. To counteract this effect each transistor is accompanied by at least one half as big transistor (all transistors whose last index is $\neq 1$ in Fig. 5.18) facing the capacitors. These transistors have no function as they are shunted by a direct connection, but they are controlled by the inverted control signal of the main transistors and therefore counteract the clock feedthrough effect.

Switch S1 is realized by the transistors N1.1.X and switch S2 is realized by the transistors N1.2.X. The transistors N2.X and P2.X constitute switch S3. In the schematic the two standard outputs OUT_L and OUT_R are depicted. These need to be equally loaded as otherwise the averaging does not work correctly. This constraint is no disadvantage for the realized receiver as an even number of comparators has to be connected to the output of the TCB, which can be easily split into two groups.

A further central output (OUT_{PAD}) is shown. It is directly connected to a probing pad and only used if the current threshold voltage shall be surveyed externally. The transistors N3.X and N4.X are the realization of the resistive part of the common RC low pass filter. All transistors are steered with digital timing logic depending on whether only double sampling, double sampling and tracking or only tracking is needed.

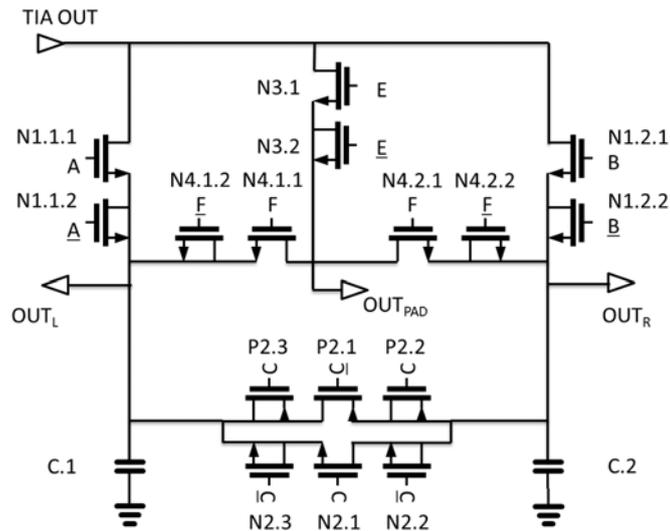


Figure 5.18: Schematic of the developed double sampling TCB

C1 and C2 are realized by 50 fF MOM capacitors. This high value is needed to compensate for the kickback noise of the comparators. For the same reason transistors N2 and P2 had to be chosen very wide. Because there is always one comparator switching on and one comparator switching off at the same time, their kickbacks can ideally cancel each other. Therefore, a very low resistive connection between all comparators is needed, realized by transistors N2 and P2. The used transistor parameters are shown in the following table. Note that all compensation transistors are half as wide as their main transistor.

Transistor	N1	N2	P2	N3	N4
Width [μm]	3	15	15	0.27	0.27
Length [nm]	120	60	60	60	60

5.4.2 Layout

The layout of the TCB is shown in Fig. 5.19 including a map of the transistors in the bottom. The footprint of the TCB is $35 \mu\text{m} \cdot 12 \mu\text{m}$. Most of it is taken by the capacitors C1 and C2 which could be greatly reduced in size by using comparators with less kickback. This means that with more modern technologies, e.g. FDSOI

28, the footprint of the TCB will shrink faster than linearly. As the averaging is an important part of the technique, which is based on the symmetry of the device, the layout was also made symmetrical concerning the two arms.

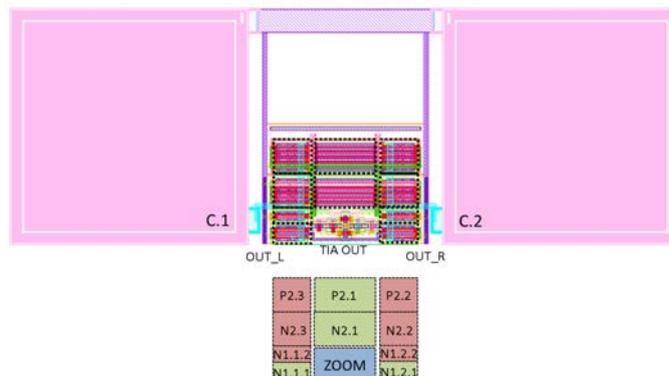


Figure 5.19: Layout of the developed double sampling TCB

The block called "Zoom" in Fig. 5.19 is shown in detail in Fig. 5.20.

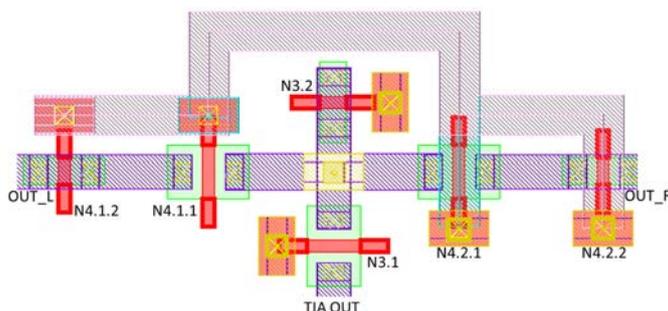


Figure 5.20: Block called "Zoom" inside the TCB layout

Transient simulation results are shown in Fig. 5.21. The green signal shows the TIA output voltage for an alternating 1010 training sequence. The red signal shows the voltage at C1 and the blue signal the voltage at C2. At the beginning S1 is closed and OUT_L starts to follow the TIA signal. After 4 bits S1 is opened and after a further bit S2 is closed, now OUT_R starts to follow the signal for 4 bits. For demonstration reasons all switches are hold open for 3 bits until switch S3 is closed and both output signals settle at the same value. The TIA signal is reduced in swing due to the increased capacitive loading when one of the switches is closed. This does not pose any problem as the sourcing capabilities of the TIA are symmetrical and hence the DC average value stays the same.

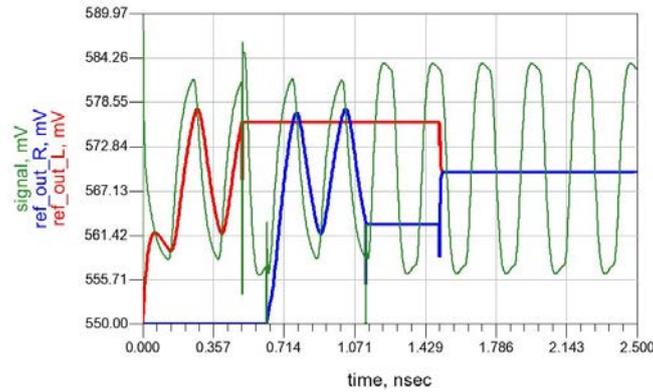


Figure 5.21: Simulation of the TIA connected to the TCB

5.4.3 Conclusion

The presented threshold control block is based on sampling and breaks the trade-off between data overhead and threshold value accuracy. Depending on the following stages it can be designed very small (only 7 transistors and 2 capacitors needed). It works purely passively and has therefore no power consumption. The acquisition time can be as low as 6 bit cycles and absolute timings with respect to the data stream are unimportant. This is relevant if several parameters (the clock delay might be one of these) have to be tuned depending on each other.

5.5 Full Receiver Schematic

The full receiver is designed to work at 8 Gbps. The comparators are optimized to run at 2 Gbps, therefore the final design comprises four comparators in four data output channels. In each data channel the comparator is followed by the comparator calibration circuitry. In the final design the data signal is delayed, instead of the clock signal, to synchronize the data signal and the clocking signal at the flip-flops. This allows to add a buffer stage behind the comparing stage, which eases the timing constraints for the flip-flop clocking, as the data edges are steeper. The buffering stage is realized by minimal sized inverters from the library and serve also to equally load the two outputs of the comparator, see Fig. 5.22. The clocking of the comparators is depicted as a single signal ϕ_N , while it is a bus consisting out of the three clocking signals described in the comparator chapter.

The clocking signal is produced in the clock phase generator that is fed with an external clock. The generator also feeds the signal into the TCB Control that generates the triggers for the TCB. The mode of the TCB is selected using an on chip SPI but the final trigger is sent via the external sync input. At the front-end of the receiver is the TIA, its feedback voltage is set via a current-mode on-chip DAC.

To convert the current signal to a voltage signal a simple resistor is inserted to the path.

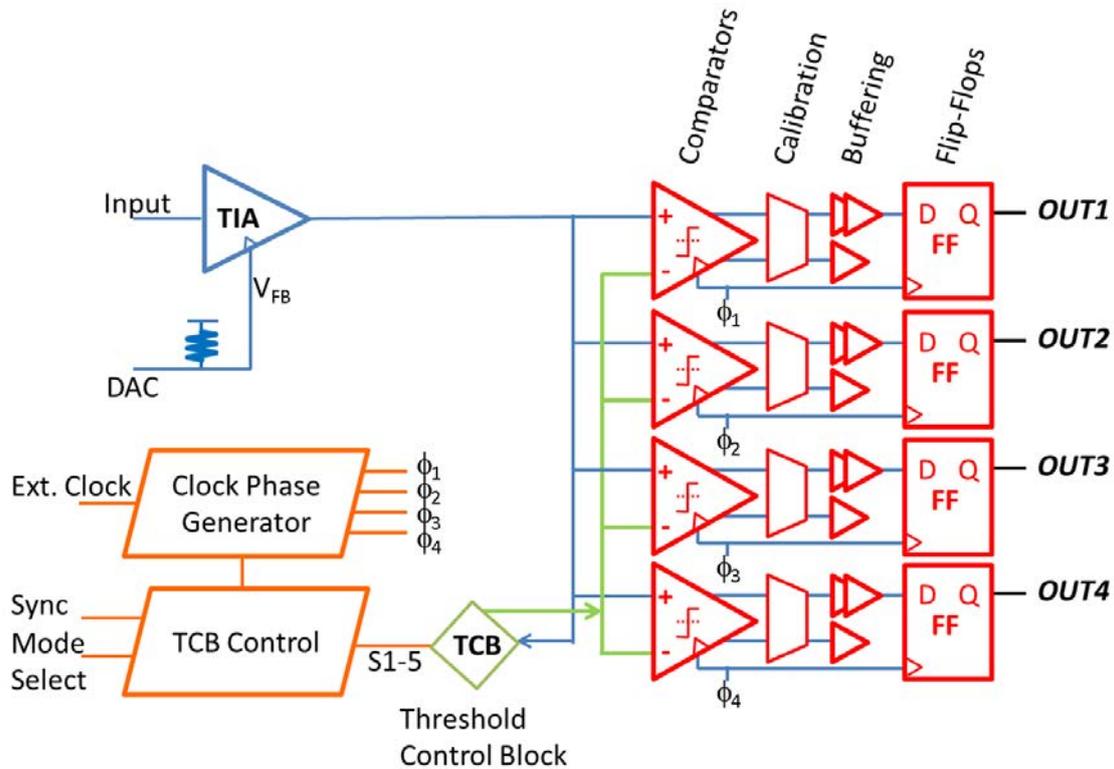


Figure 5.22: Schematic of the complete receiver

5.6 Layout

While designing the full receiver the most critical part is to find the configuration of elements that leads to the least parasitic capacitance at the input and output of the TIA. Fig. 5.23 shows the chosen star-like configuration with the TIA being the central element. It allows shortest and equal connection from the TIA output to the comparators. Because this receiver is meant to be flip-chipped on an optical interposer the input can come directly from the aluminium cap to the input of the TIA. This layout does not yet include the clock phase generation but all other blocks shown in schematic 5.22. The dimensions of the receiver block are $60\mu\text{m} \cdot 25\mu\text{m}$.

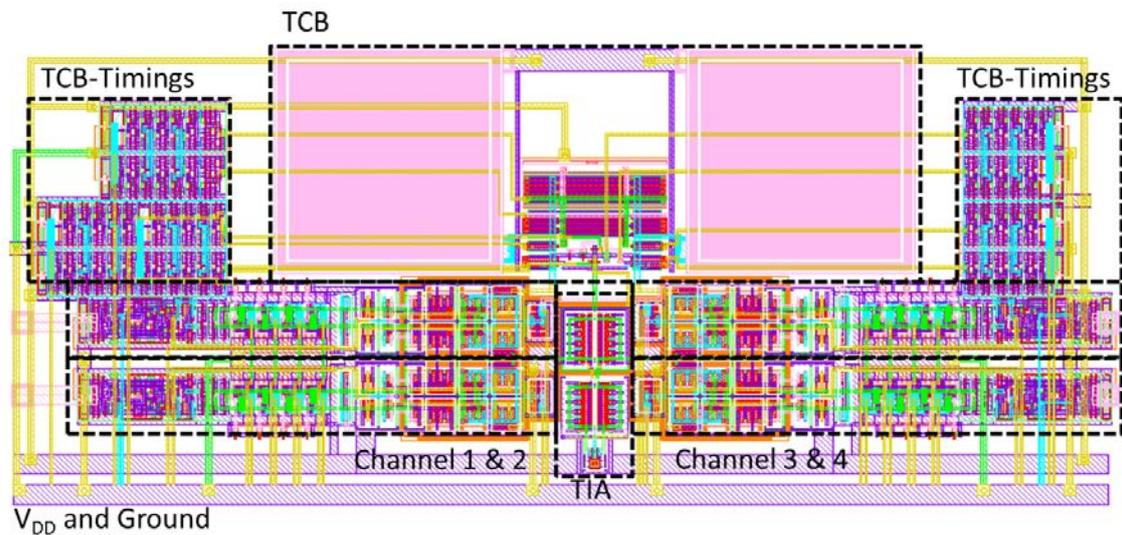


Figure 5.23: Layout of the complete receiver

For better clarity Fig. 5.24 shows the TIA and a single data channel. For good integrability the calibration circuitry was designed using the same rail to rail width as the inverters used in the buffers and the flip-flop. The length of a data channel is $25 \mu\text{m}$.

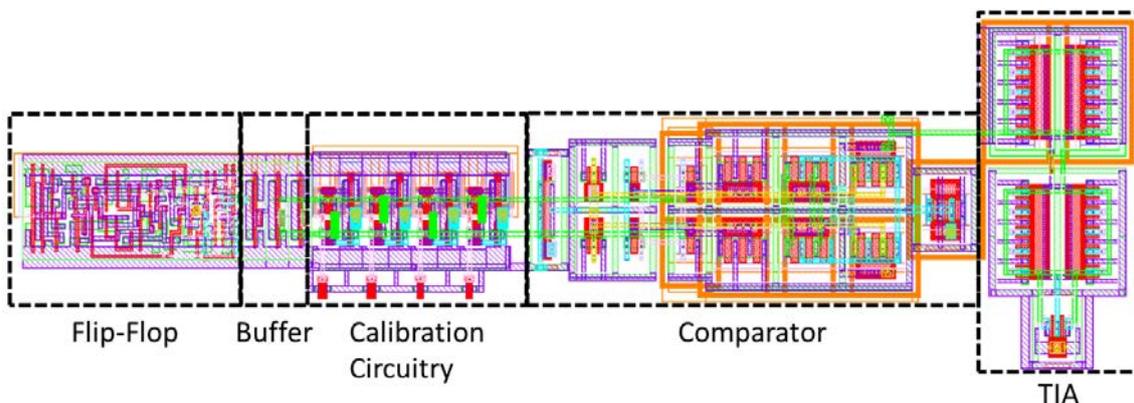


Figure 5.24: Layout of a single data channel in the receiver

5.7 Verification by Simulation

All elements have been separately tested to achieve the minimal needed specifications in FF and SS corners as well as at 0° and 80° degree Celsius. Further tests included Monte Carlo simulations and transient noise simulations. Full system tests need a

long computing time, thus could not be carried out for every test case. To verify the full receiver a 120 ns long transient noise simulation has been carried out, based on a full receiver post layout extraction. At the input a current source shunted by a 20 fF capacitor was used to emulate the photodiode sourcing $(15 \pm 7) \mu\text{A}$.

Instead of using a pseudo random bit stream for this simulation the injected bit stream starts by 20 alternating bits as training sequence header. It is succeeded by a stream like '01010110011100011110000' to quickly test the receivers capability to handle short and long sequences of the same bit. The amount of equal bits rises until 6 and than restarts. During other tests equal bit sequences until 65 bits have been tested, but are of no higher interest because due to the sampling approach the long sequences do not pose problems.

In this full system test the receiver circuitry without clock phase generation consumes 600 μA . This corresponds to a bit efficiency of 75 fJ/b if the receiver runs at 8 Gbps. In a full receiver many channels will run using the same clock phases. For this reason, the energy consumption will be shared by many receivers and can be neglected at this point. Nevertheless, the clock phase generation consumes 3 mA providing the eight 4 GHz clock phases. To estimate the full links power consumption the models described in the optimization chapter were taken and parametrized for this receiver. Following these results the entire link would consume 860 fJ/b. The goal of an optical link below 1 fJ/b is therefore undercut.

A cutout of the simulation results is shown in Fig. 5.25. The top panel shows the input current signal, the second panel shows the TIA output signal as a voltage. The clock in this simulation was switched on after 1 ns, therefore no comparator was running before and the TIA signal is clean. Nevertheless, after 1 ns the TIA signal shows clear traces of the comparators kickback noise. The third and fourth panels show the two outputs of the double sampling TCB. The fifth panel shows the output of the first data channel's comparator output. When comparing the signal to the bit stream note that this comparator only samples every fourth bit. The sixth panel shows the buffered comparator signal and therefore the flip-flop's input signal. The seventh signal is the flip-flop's output signal with the correct bit length as the signal does not rise after each bit back to V_{DD} . The bottom signal is the sync signal to start the TCB. The results of all four channels over the entire 120 ns did not show any bit errors.

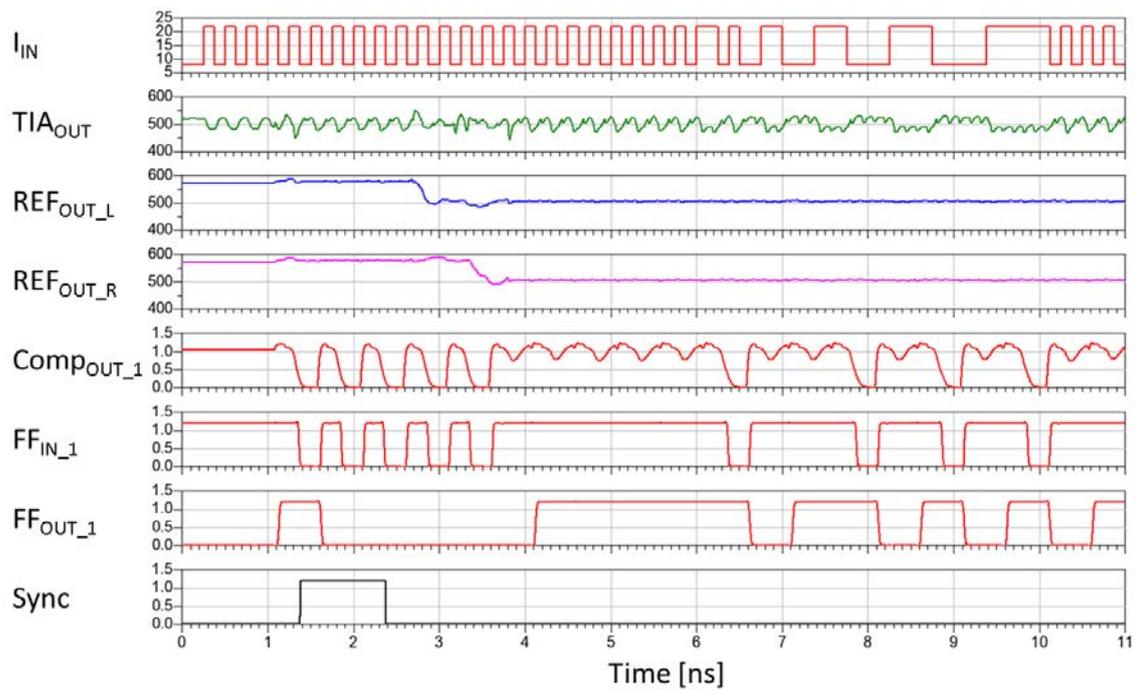


Figure 5.25: Complete receiver verification by simulation. Please find the used labels defined in Fig.5.26

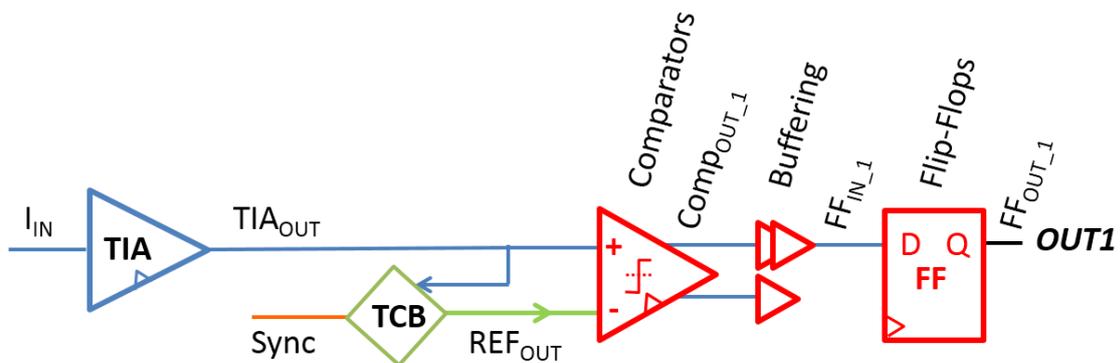


Figure 5.26: Simplified receiver architecture for label definition used in Fig.5.25

5.8 Measurement Setup

5.8.1 Design for Measurement

The receiver was, similarly to the TIA, measured in an electronic-input electronic-output configuration. For this reason it had to be padded in a corresponding environment as shown in Fig. 5.27. As in the TIA version the data input consists of a $50\ \Omega$ terminated pad in a G-S-G configuration, followed by a $10\ \text{pF}$ capacitor serving as a DC-Block. The conversion from voltage to current is done using a $10\ \text{k}\Omega$ resistor. The DC current is controlled using an on-chip DAC. A further transistor serves to pull down the input node to ground and therefore to switch of the TIA. Another set of $50\ \Omega$ terminated pads serves to connect the sync signal to the chip. The four outputs are on the opposing side of the chip. As the outputs of the receiver are very fast acting flip-flops, a bench of output buffers is needed to drive the output connections. The clock input is placed in the middle of the output pads. The output pads and the clock input pad in the final realization are also in a G-S-G configuration, but for reasons of readability they have not been drawn in this schematic.

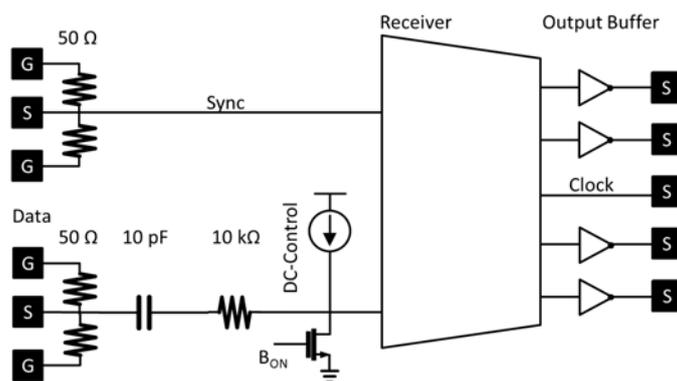


Figure 5.27: Schematics of the top layer for testing the receiver electrically

The TOP layout of the entire receiver is shown in Fig. 5.28. In order to bridge the distance between the input pads and the DC-block with the smallest input capacitance possible a micro strip line was placed in between. In this layout the clock phase generator is visible between the output buffers on the top and the receiver.

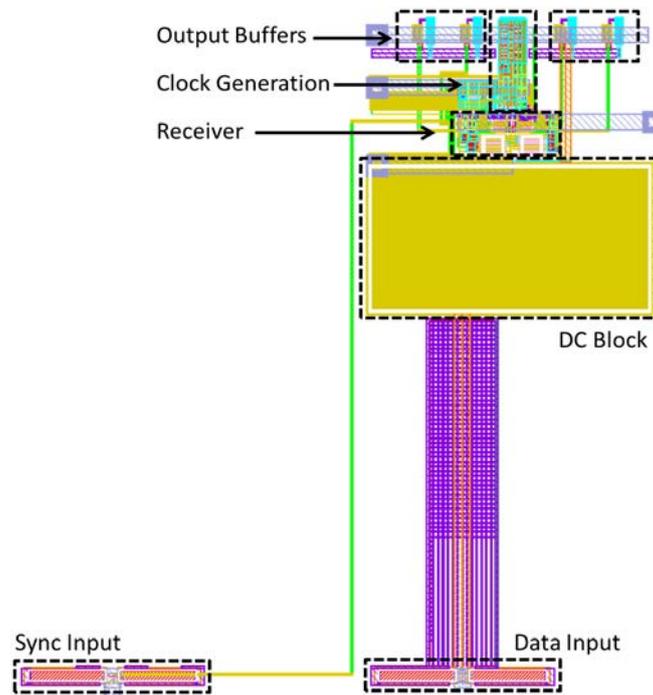


Figure 5.28: Layout of the top layer for testing the receiver electrically

To ensure the least supply noise possible, the blocks of the receiver are provided with separate power supplies. The functional groups sharing power supplies are:

1. TIA and Data Channels
2. Clock Phase Generator and TCB Control
3. DACs, SPI, Current Mirrors for DC input current and Resistor for V_{FB} generation
4. Output Buffers

Another supply is needed to generate a $24 \mu\text{A}$ biasing current for the DACs. The sum of all signals needed is 15, not including the corresponding ground connections.

5.8.2 Bit Error Rate Measurement Scheme

To measure the bit error rate (BER) an Anritsu 1800 Signal Quality Analyzer was used. It is capable of generating precise bit streams with configurable voltages and bit rates upto 12 Gbps. It can furthermore measure bit streams and compare them with either the input bit stream or a different saved bit stream. It can also supply the clock to the receiver to have a synchronously working measuring system. The designed receiver splits the incoming data stream into four channels. It is therefore

not possible to generate a random bit pattern and try to compare it to itself. It is, further, impossible to just split a defined data pattern into each fourth bit, as the offset between receiver channels and signal analyser is not defined. Instead, a random bit pattern is generated, as shown in Fig. 5.29, that is then “rotated” around itself three times with different “angles” (see coloured boxes in the figure). Finally, the four patterns are intertwined with each other. Consequently, a data pattern is generated that will be the same at each output of the receiver without having each bit stretched to four bits.

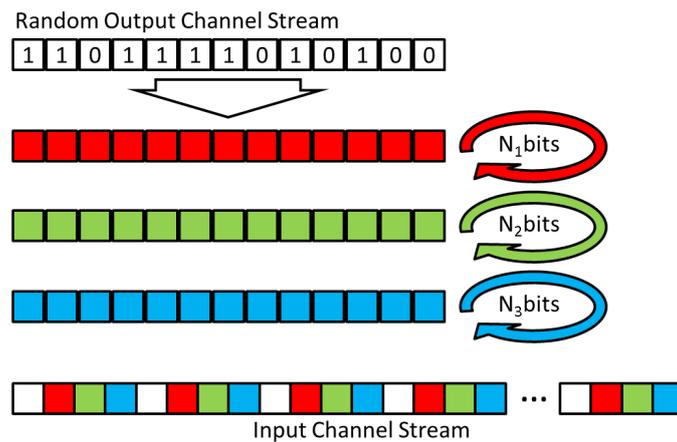


Figure 5.29: Layout of the fabricated PCB to test the receiver

5.9 Results

Fig. 5.30 presents output waveforms of two channels measured with a sampling oscilloscope and validates the basic functioning of the fabricated chip. The input rate for this measurement was 4 Gbps. The waveforms do not represent an eye diagram; the input stream was on purpose generated in a way that the output streams would be 1000 , 1100, 1010 and 1110. This allowed a quick visual test of the chip. The threshold control block (TCB) was in RC tracking mode.

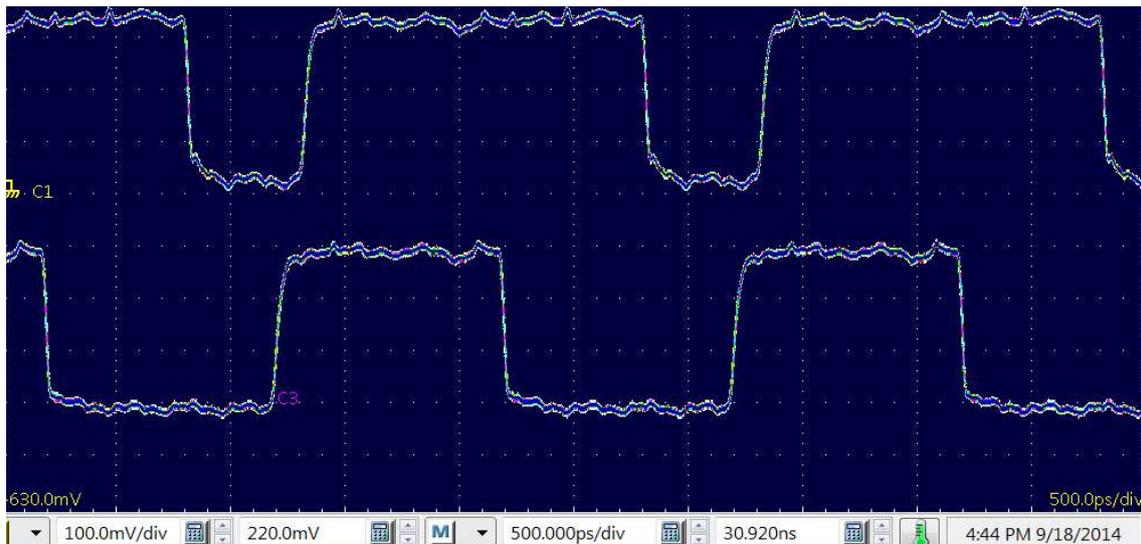


Figure 5.30: Output waveforms of two channels at 4 Gbps input

In Fig. 5.31 the input and two output waveforms are shown. This measurement was done with a PRBS at 8 Gbps.

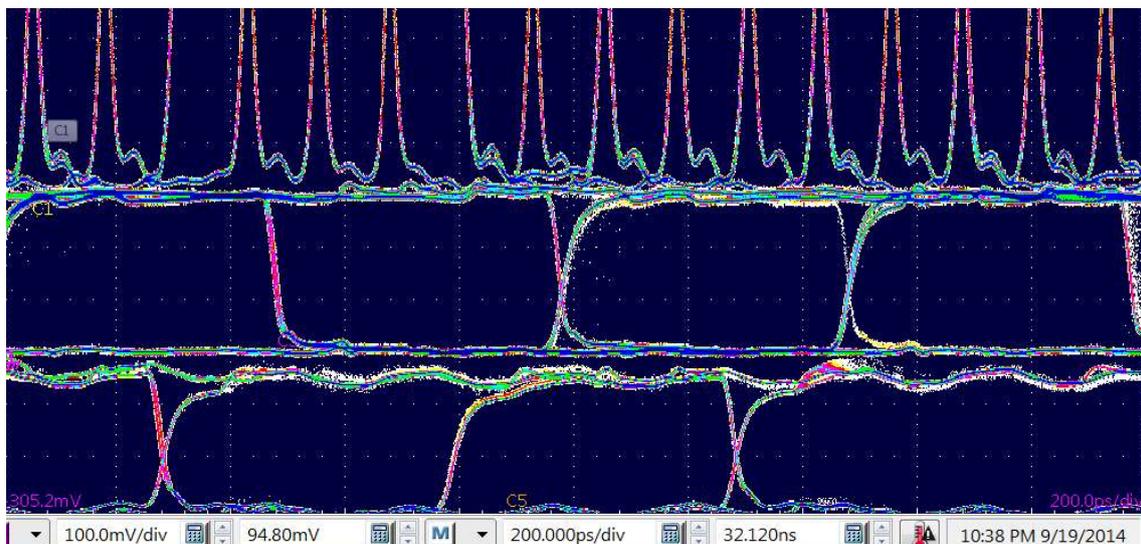


Figure 5.31: Input and 2 output waveforms at 8 Gbps PRBS input

After these basic tests BER have been measured. The BER was measured with an input signal of $33 \mu\text{A}_{pp}$ and a frequency of 8 Gbps. If a BER of 10^{-12} is considered single bit errors appear every two minutes at this bit rate. This means that a statistically valuable measurement will last around one hour. The BERs in Fig. 5.32 show these measurements. The receiver achieved a BER of 10^{-10} . Fig. 5.32

also presents the recorded results before and after this measurement that ran during an entire night of which the worst BER was 10^{-6} .

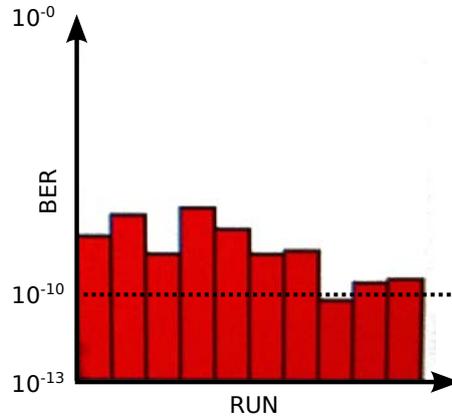


Figure 5.32: Instable BER measurement results

These strong fluctuations appear because the chip was characterized using mechanically unstable probes. The characterization was stopped at this point and a PCB was designed to securely bond the chip onto. Fig. 5.33 shows the layout of the PCB.

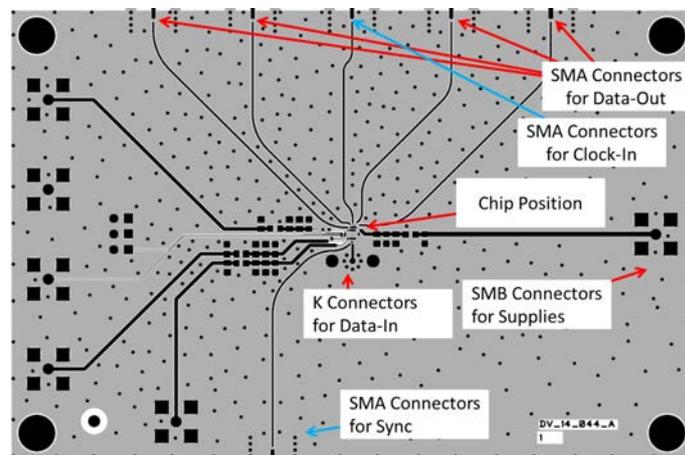


Figure 5.33: Layout of the fabricated PCB to test the receiver

The PCB was at the point of submission of this report still in production, hence all missing characterization steps will be presented in the defence of the thesis. Anticipated measurements are the dependence of the BER on the input signal strength, the jitter and skew of the supplied clock.

5.10 Conclusion

Based on the preceding chapters, this chapter concluded the design of an optical receiver optimized for silicon photonic links. The chapter explained in detail the chosen comparators and introduced a new mechanism for auto-tuned comparators. Furthermore, the threshold control block (TCB) and its trade-offs were presented, including a novel architecture for such a circuit. Afterwards, the assembly of the full receiver was shown in schematics as well as in layout. Simulations were presented to prove the functionality of the circuit. In simulation the full link energy efficiency was 860 fJ/b. It reaches therefore the goal of 1 pJ/b. Measuring bit error rates (BER) of a device having a single input stream but four output streams is not an obvious task, hence the developed measuring scheme was laid out. Finally, preliminary characterization results were given. The receiver proved to work correctly at an input bit rate of 8 Gbps. It achieved a BER of 10^{-10} at an input signal of 33 μ A. Measuring high quality BERs has challenged the mechanical stability of the system and undermined the characterization of the chip. A PCB was designed to eliminate this problem and characterization results of the new measurements will be presented during the defence.

Chapter 6

Clock Channel Receiver

“I’m not interested in preserving the status quo; I want to overthrow it.”

Niccolo Machiavelli

6.1 Introduction

As described in chapter 5, most state of the art optical receivers use clocked comparators as decision stages. It has also been demonstrated in chapter 3 that the exact sampling time is of high importance as it influences directly the necessary optical power consumption. Precise low jitter clocks are therefore required.

There are two major ways of recovering an on-chip clock. The Clock Data Recovery (CDR) is a widely applied technique that uses an on chip oscillator and calibrates it with a PLL, so that the oscillator edges get aligned with the edges of the incoming data stream. Data channels often use non return to zero codes, hence not every clock edge can be aligned to a corresponding data edge. This makes these systems less stable and precise than the second option which uses a dedicated clock channel that can be distributed optically.

There are three major advantages if optically clock forwarding is applied. First, the low signal distortion of the optical signal, and the fact that the optical signal does not pick-up environmental noise nor noise due to cross talk enables optical clock distribution channels to have low jitter and skew [60]. The second advantage is the possibility to integrate the clock and data channel into the same waveguide reducing design complexity. Silicon photonics allows to design precise power splitters other than 3 dB splitters. This opens the possibility of bus-like distribution of the clock with a single waveguide instead of a real-estate consuming H-tree structure.

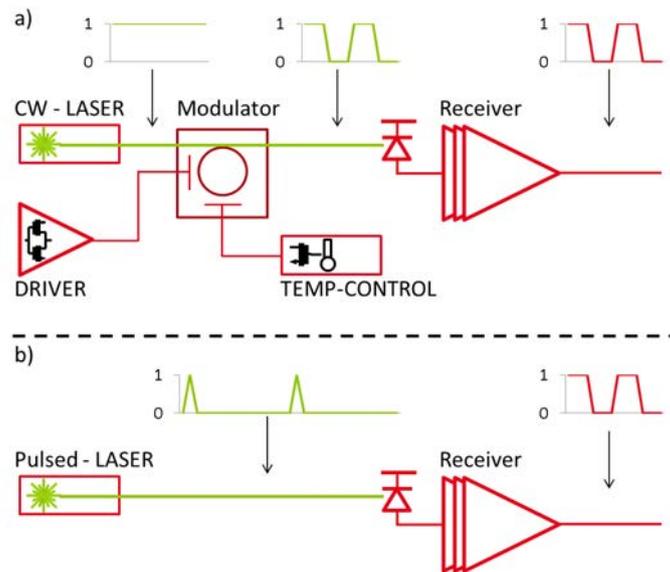


Figure 6.1: Possible clock channel implementations: a) usage of a cw emitting laser and a modulator or b) usage of a pulsed laser

Dedicated clock channels, see Fig. 6.1, differ from data channels for several reasons. The first and most important difference is, that the signal is periodic and even the frequency range is known. This knowledge about the signal can be used to optimize every element in the channel. For example, the light modulator and all the supporting circuitry as temperature controller and driver can in certain cases be replaced by a pulsed laser, as shown in Fig. 6.1 a) and b). This reduces power consumption and footprint enormously. Nevertheless, pulsed lasers do not emit pulses with a 50% duty cycle but only short pulses [61]. This demands for dedicated clock receivers that can handle this optical clock waveform and translate it into a conventional electrical clock signal.

Furthermore, the clock receiver should make use of the periodicity of the signal, allowing receiver topologies such as injection locked oscillators (ILO) or self-triggered integrate and dump receivers. In this context, the state of the art presents three solutions for optical clock channel receivers.

1. The front-end stays a TIA as presented in chapter 4. In contrast to TIAs in data receivers, the TIA in this case cannot be followed by a clocked decision stage, but the signal has to be amplified using limiting amplifiers. These high speed amplifier chains are power inefficient because they need to be biased at around $\frac{V_{DD}}{2}$, causing a high DC current passing through them.
2. The receiverless approach [62] makes use of the periodicity of the signal by connecting two photodiodes to a voltage amplifier, as illustrated in Fig. 6.2. One photodiode charges the input capacitance of the amplifier while the other one is discharging it. The major drawback of this technique is the doubling of

the input capacitance due to the second photo diode, which halves the optical sensitivity of this architecture. This is because even modern integrated germanium photodiodes with parasitic capacitances in the order of 5 fF to 10 fF present a loading one order of magnitude higher than an ordinary transistor from a modern technology. Furthermore, the second photodiode and its environment, waveguide and copper pillars, increase the complexity and footprint of the system considerably more than single photodiode based solutions.

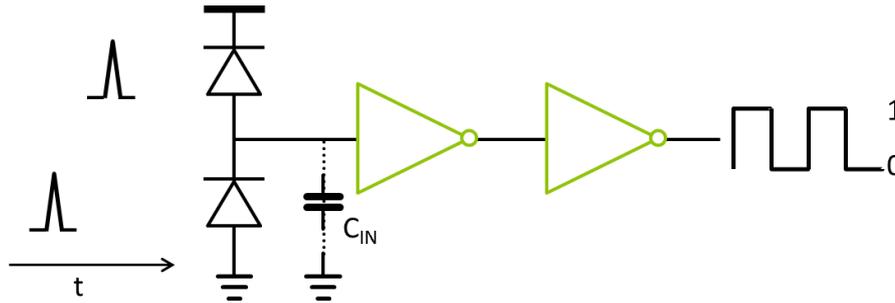


Figure 6.2: The receiverless architecture

- ILO based optical clock receivers are based on local oscillators that run approximately at the frequency of the optical clock channel. They can be locked to the clock signal with low injection powers, if the free running frequency of the ILO is close to the injected frequency. Process voltage and temperature variations alter the nominal free running frequency, so that higher injection powers would be necessary. Therefore, recent research started to develop calibration techniques to gain high optical sensitivity [63,64], even in the presence of PVT variations.

6.2 Integrate and Dump Receiver

6.2.1 Towards a self triggered Integrate and Dump Receiver

As mentioned above, the receiverless architecture has a great electrical efficiency but a very poor optical sensitivity. This is due to the connection of the second photodiode, which introduces further parasitic capacitance. In order to understand the impact of the parasitic capacitance, the signalling process at the front-end has to be understood. The photodiode generates a current I_{PD} depending on its illumination. If a light pulse arrives at the photodiode, the I_{PD} can be integrated over time and we can say that a charge Q_{PD} has been generated. As there is no DC path to ground, this charge will be deposited on the connected capacitor C_{IN} (parasitic capacitors of the photodiodes and input capacitance of the CMOS inverter). For a capacitor holds $V = Q / C$, this means that the node voltage rises, which will be amplified

inside the amplifier chain. If a minimal voltage rise has to be generated to trigger the amplifier chain, the optical sensitivity reducing property of any capacitance at the input node becomes obvious. The parasitic capacitance of the photodiode in addition with the capacitance due to the wiring (no matter whether the connection is done by bonding or flip chipping) is several times bigger than the input capacitance of the CMOS inverter C_{IN} . Therefore, in a first order approximation we can link the receiver sensitivity directly to the photodiode capacitance. It can be concluded that a second photodiode will result in half the optical sensitivity.

A first optimization of the system, shown in Fig. 6.2, might lead to the circuit shown in Fig. 6.3, where the second photodiode is replaced by a constantly biased transistor, acting as a current source. Now the parasitic capacitance is almost halved and the footprint is considerably smaller, but in this approach half of the photodiode's current signal is sacrificed. It leaves the circuitry directly through the current source, without charging C_{IN} .

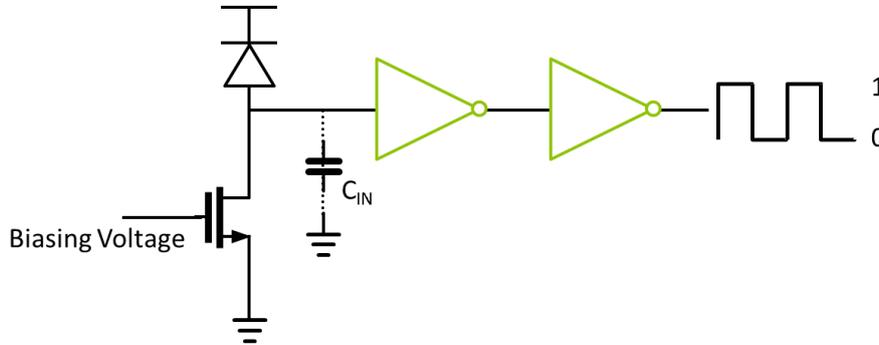


Figure 6.3: Replacement of the second photodiode with a constant current source

Nevertheless, this work proposes to integrate a novel feedback loop in this architecture, as shown in Fig. 6.4, to control the biasing voltage of the current source. If the average photocurrent, generated by the optical clock signal, is well matched to the current drawn by the current sink, the second inverter in the inverter chain outputs already the full-swing clock signal. If, furthermore, a low pass filter is connected to this node, its DC voltage V_{DC1} will correspond to the duty cycle of the clock DC_{CLK} by $DC_{CLK} = V_{DC1} / V_{DD}$, see Fig. 6.5. If the succeeding inverter output is also connected to another low pass filter its DC voltage V_{DC2} will be $V_{DD} - V_{DC1}$. These two voltages are perfectly suited (and well shielded against process variations) to serve as an error signal to steer the current source V_{REF} . Moreover, using the duty cycle as error signal makes duty cycle control stages [65] unnecessary; accordingly the architecture accepts a larger range of input signals with reduced power consumption. Fig. 6.4 shows a possible implementation of this circuit, where the signal is fed into an integrator and into a second common-source stage to combine the proportional V_{PROP} and integral V_{INT} correction signal.

Fig. 6.5 shows how, based on the duty cycle measurements, V_{Ref} is increased

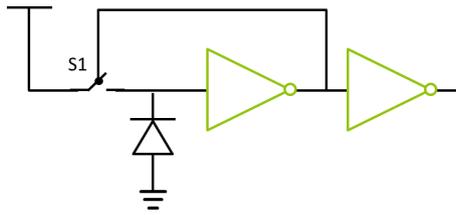


Figure 6.6: Using the output of the first inverter to trigger a charge dump switch connected to the input node, qualifies this circuit as a self-triggered integrate and dump receiver.

To reduce this problem a diode-connected transistor $P1$ is placed between V_{DD} and the switch $S1$ (see Fig. 6.7). Note that no trade-off has to be made between the sourcing strength of the new transistor and extra parasitic capacitance (both depend on the width of the transistor), as $P1$ is only connected to the circuitry by $S1$, when no photocurrent is generated. The new transistor can therefore be as wide as necessary to achieve fast enough discharge times for C_{IN} . This architecture is still not operational because of the discharge/reset mechanism. The output of the first inverter will be short pulses, because the mechanism resets the inverter the moment it reaches $V_{DD}/2$, which is sufficient to trigger simple CMOS switches.

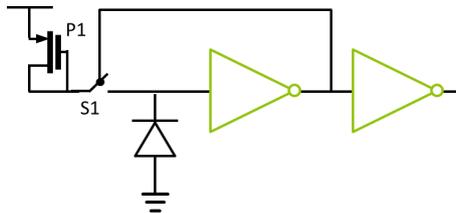


Figure 6.7: A diode-connected transistor serves as voltage reference, to reset C_{IN} close to the inverter's trip point.

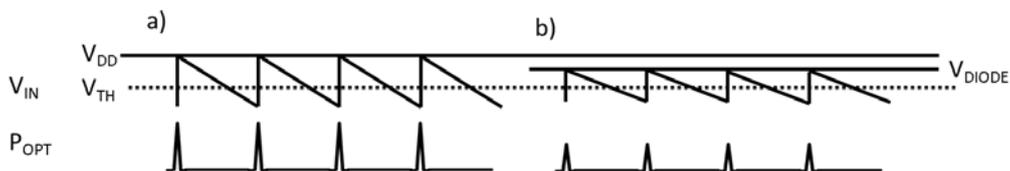


Figure 6.8: Swing of V_{IN} for a) the basic topology and b) the topology with clamping diode

Indeed, a more complex triggering mechanism is needed. To control the resetting time, a low pass filter is connected to the output of the first inverter. The output

of this filter will follow its input signal slowly. This slow signal can be compared to a reference voltage V_{REF} , which allows generating exact timing events to reset the circuit. V_{REF} defines the reset time of the signal, which corresponds directly to its duty cycle. Fig. 6.9.a shows a block diagram of the new circuitry, proposed in the context of this thesis. Fig. 6.9.b shows the signal propagation inside the circuit. This concludes the general concept of the new receiver architecture. All following steps are further optimization of this idea.

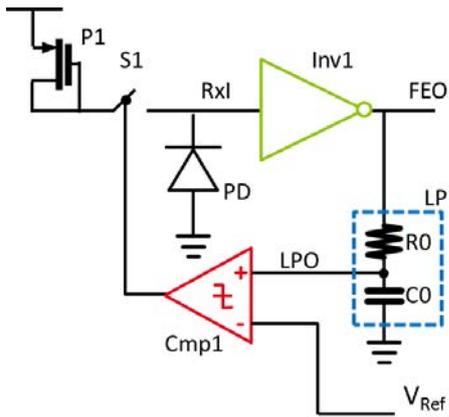


Figure 6.9.a: Block diagram of the proposed clock receiver

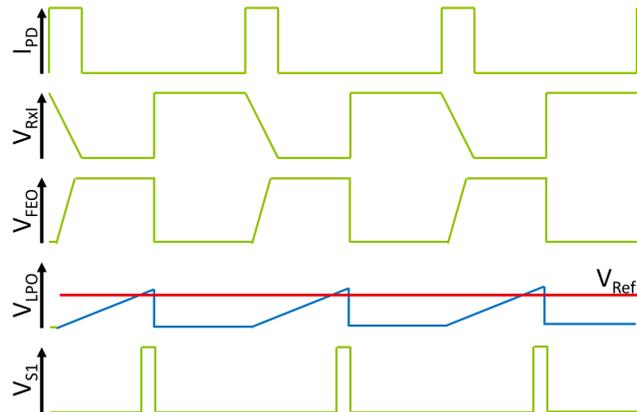


Figure 6.9.b: Timing diagram of the signals propagation

6.2.2 Receiver Architecture

To reduce the circuit's footprint and power consumption, the comparator should be replaced by a simple inverter that acts here as a fixed reference comparator (Cmp2), see Fig. 6.10. Doing this, a new way of setting the dump time and therefore the duty cycle is needed. A good possibility is to use a configurable low pass filter. To implement the time constant control, the resistor of the low pass filter is shunted with a transistor, working as controlled resistor. Note that in the following the 28nm fdsoi technology was used for the design of the proposed circuits.

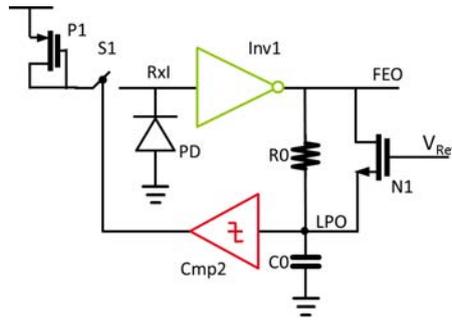


Figure 6.10: Footprint and power reduction by replacing the comparator with an inverter

Furthermore, the photodiode should not be connected to the NMOS transistor of the first CMOS inverter, as it represents unnecessary input capacitance. The CMOS inverter is split into the P_{INV} , which remains connected to the photodiode, and the NMOS transistor. The NMOS transistor is replaced by the diode-connected NMOS N2 transistor and the switches S2 and S3, which are controlled with the delayed comparator output, see Fig. 6.11.a. Transistor N2 serves like P1 as a voltage reference to discharge the node FEO close the V_{th} of the following inverter (not shown in Fig. 6.11.a). The delay is used to generate a voltage pulse, by closing S2 and S3, long enough to achieve full discharge of FEO.

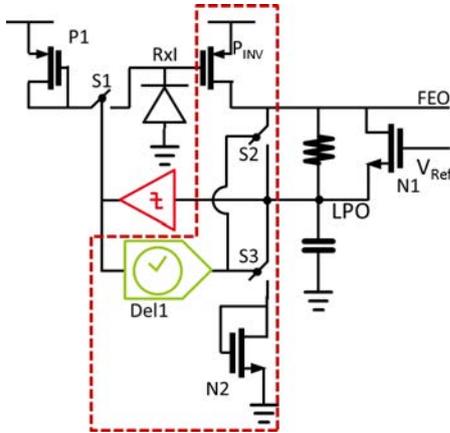


Figure 6.11.a: Further optimization by splitting the first inverter into P_{Inv} and N1

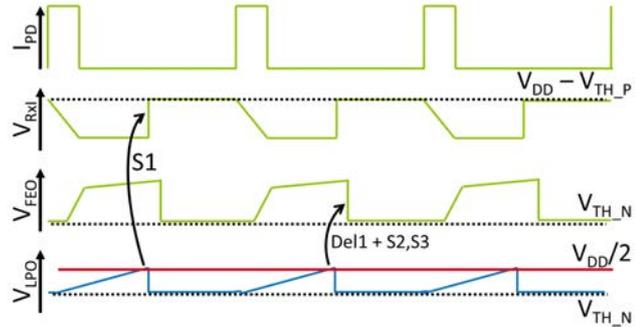


Figure 6.11.b: Timing diagram of the signals propagation

The results of the changes are visible in the difference between the waveforms of the unoptimized (Fig. 6.9.b) and the optimized (Fig. 6.11.b) architecture. Due to the replaced comparator the reset signal is directly generated when V_{LPO} reaches $V_{DD}/2$. More importantly, V_{Rxl} rises only until $V_{DD} - V_{TH_P}$ and the two voltages V_{FEO} and V_{LPO} only fall until V_{TH_N} . Finally V_{Ref} has to be generated. This is done

by using the circuit discussed in Fig. 6.4. The entire proposed circuit is shown in Fig. 6.12.

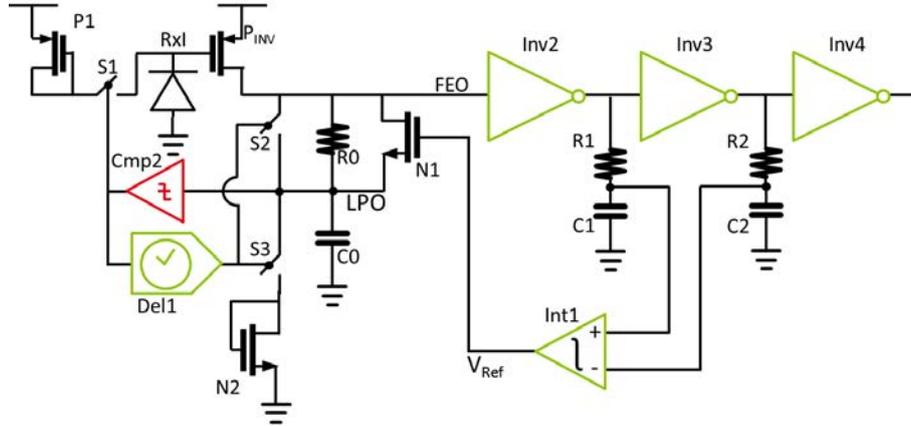


Figure 6.12: Complete receiver architecture

S1 is realized by a single PMOS transistor with a width of 400 nm, S2 is also implemented as a single NMOS transistor of 240 nm of size. S3 is realized by two transistors (shown in Fig. 6.13) to compensate clock feedthrough, where $W_{Gate} = 400$ nm.

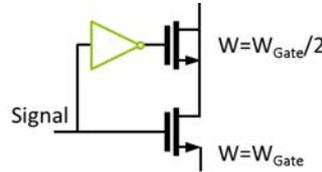


Figure 6.13: Clock feedthrough compensated switch

The capacitor C0 is implemented by an NMOS transistor, whose gate serves as one connection and the shorted back-gate, source and drain as the second connection. The used NMOS has a width of 800 nm and a length of 300 nm. All other element parameters are shown in the following table:

$W_{P1}[\mu m]$	$W_{P_{INV}}[\mu m]$	$W_{N1}[\mu m]$	$W_{N2}[\mu m]$
4	3.2	1.6	1.2
$R_{R0}[k\Omega]$	$R_{R1}[k\Omega]$	$R_{R2}[k\Omega]$	
400	80	80	
$C_{C1}[pF]$	$C_{C2}[pF]$		
1	1		

The same guidelines were taken for the integrator design as for the entire circuit, namely small footprint and small power consumption. To achieve high power and footprint efficiency a novel integrator architecture is proposed in this work, shown in Fig. 6.14. Since the integrator is part of a calibration-feedback-loop, there are only low requirements concerning speed and linearity but high demands on a well defined static behaviour. The architecture consists of two voltage controlled current sources (CS1, CS2) that transform the input voltages into the currents I_+ and I_- . Their difference, $I_+ - I_-$, charges C_{Out} and integrate therefore the differential error on V_{Ref} . Furthermore, the final design features immunity against global process variation and suffers very little from local process variations, due to its symmetry.

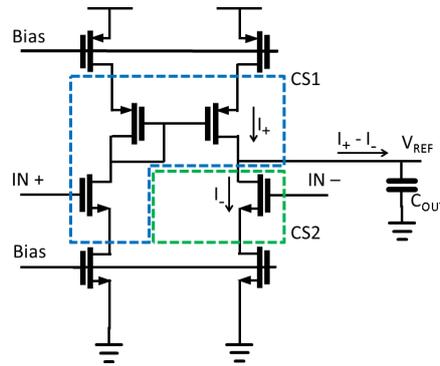


Figure 6.14: The developed integrator stage

The used transistor sizes are all equal for symmetrical pairs and are shown in the following table. Please notice that the biasing NMOS and PMOS transistors are not necessary for the correct functioning of the circuit and serve only for controlling the speed of the integrator. The length of all transistors is 28 nm.

$W_{N-CS}[nm]$	$W_{P-CS}[nm]$	$C_{Out}[pF]$
80	160	1

The used delay element in the receiver has to output a defined pulse length that is applied at the gates of the switches S2 and S3. The used circuit is shown in Fig. 6.15. It is based on an asymmetric delay cell, where the driving strength of the PMOS exceeds the driving strength of the NMOS. The used parameters are $W_{P_{asym}} = 500nm$, $W_{N_{asym}} = 80nm$ and $C_{C_{asym}} = 10fF$.

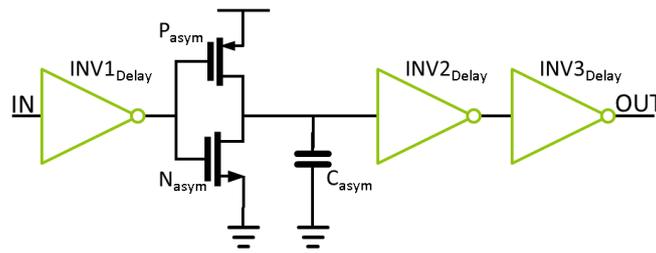


Figure 6.15: Asymmetric delay stage for forcing minimal pulse length

6.2.3 Simulation Results

The performance of the proposed architecture has been validated through transistor level simulations. The photodiode model used includes a parasitic capacitance of 10 fF. All performed simulations include time domain noise. In Fig. 6.16.a the relevant internal signal waveforms are presented. The input current signal shown in the first panel has an amplitude of $10 \mu\text{A}$, a frequency of 2 GHz and a duty cycle of 25 %. The second panel shows the voltage at node RxI (see Fig. 6.12). The third panel shows the voltage at the output of Inv1 (FEO) and the first low pass filter output LPO. The lowest panel shows the output of the optical clock receiver RxO, where it is clearly visible that the output clock duty cycle is 50 %.

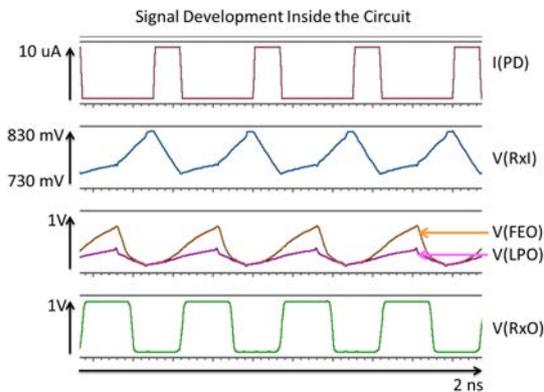


Figure 6.16.a: Steady state waveforms

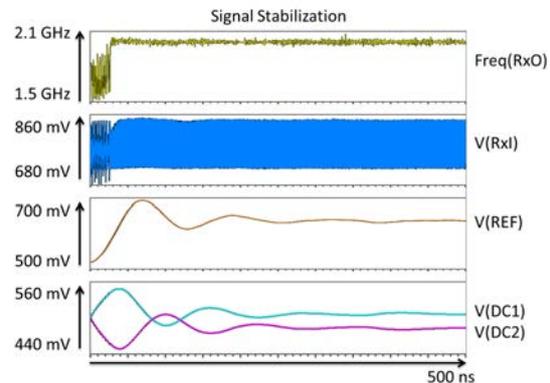


Figure 6.16.b: Transient evolution of the system

While Fig. 6.16.a shows steady state waveforms of the circuit, Fig. 6.16.b presents the transient evolution of the system before reaching the steady state. At the start-up of the system, V_{REF} is not yet correctly set to match the desired duty cycle and the circuit is not running properly, as the chaotic voltage at the RxI node indicates. Nevertheless, after about 250 ps V_{Ref} , shown in the third panel, is stable at the value set by the duty cycle control loop. At this moment the output signal frequency becomes stable at 2 GHz (see first panel). The bottom panel in Fig.

6.16.b shows the error signals (DC1, DC2) produced by the duty cycle to voltage converters realized by the second and third RC filters shown in Fig. 6.12.

Fig. 6.17 presents the working range of the circuit under different input current and duty cycle conditions. Note that the output duty cycle is automatically regulated to be 50 % in all conditions. All pixels in Fig. 6.17 represent simulations in which the steady state output frequency was equal to 2 GHz, which was the condition used to assess the correct operation of the proposed circuit. The colouring of the pixels denote the jitter of the output signal. In the interesting low-input-power area (bottom-left corner of the plot), the jitter is always inferior to 5 ps. A big advantage of integrate and dump receivers is their capability to work with short pulse input signals, as they integrate the charge delivered in one pulse. This behaviour is proven in Fig. 6.17. The working range boundary has the form of a hyperbole, meaning that the product of input current I_{PD} and duty cycle stays constant along the line. The hyperbole drawn in Fig. 6.17 represents all data points where the integrated optical input power $(DC \cdot I_{PD}) / R_{PD}$ is equal to 2 fJ/cycle. R_{PD} represents the responsivity of the photodiode and it is assumed to be 1 A/W. Furthermore, the jitter values also follow this trend.

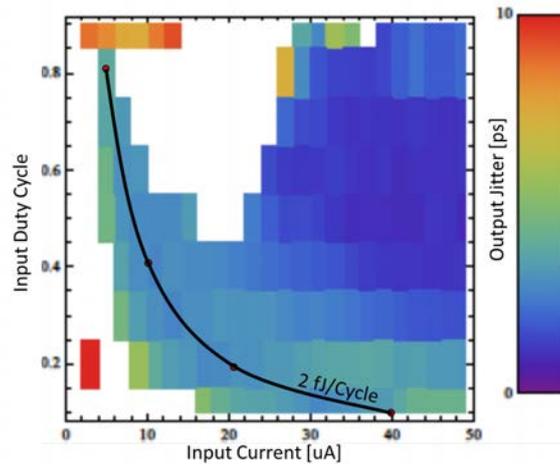


Figure 6.17: Working range of the system

In order to compare the novel architecture with state of the art architectures, other receiver architectures have been designed and tested using the same 28nm fd-soi technology. Their performances are compared to the new architecture, proposed in this thesis, in the following table. The optical sensitivity S_O is normalized to a 50 % duty cycle clock input. The overall link power (P_L) is computed as $S_O / (R_{PD} \cdot E_L) + P_R$, where E_L is the power plug efficiency of a laser, which is assumed to be 20 %. P_R is the receiver's electrical power consumption. Although the suggested architecture is neither superior in optical sensitivity nor electrical power consumption, it is superior in the overall link power consumption when the laser power is taken into account. It has also to be considered that the overall power consumption does not

include losses in waveguides or losses due to the coupling of an external laser; these would shift the results further to the benefit of the proposed architecture. Finally, the power consumption could be further improved if the integrator in Fig. 6.12 was turned off to reduce its power consumption after establishing V_{REF} .

Front Ends:	TIA	Receiverless	This Work
S_O [μA]	1	30	5
P_R [μW]	2000	20	135
P_L [μW]	2005	170	160

6.2.4 Conclusion

This chapter covered the presentation of a novel optical clock receiver architecture. It shows high sensitivity while having very low power consumption and footprint. This is achieved by using a self triggered integrate and dump topology, that takes advantage of the periodicity of the signal. It features intrinsic duty cycle control and accepts arbitrary short pulses as input signals, enabling the use of pulsed lasers as highly stable clock sources.

6.3 Injection Locking in Ring Oscillators

An injection locked oscillator (ILO) is any oscillator that is fed with a signal, in such away that the oscillator's frequency will equal the injected signal when the signal strength is strong enough to lock it. Depending on the realization of the ILO, not only the frequency is locked but also the phase relation between the oscillator's output signal and the injected signal can be controlled. These two properties make ILOs a good basis for clock channel receivers [67]. ILOs have further interesting applications such as frequency division or multiplication [68] [69]. Concerning time interleaved receivers, as presented in the preceding chapter, ILOs can integrate the phase generation for the different comparators. Lastly, if the clock signal is sent over a noisy channel, ILOs can serve to restore the signal integrity.

6.3.1 Introduction

ILOs used for clock distribution purposes are commonly ring oscillators, because LC-tank oscillators are too big to be incorporated several times into a processor and they do not provide a square waveform at their outputs. In order to lock a ring oscillator to an optical clock input signal, a photodiode (PD) is used, having its anode connected to V_{DD} while its cathode is connected to one of the inverter nodes inside the ring oscillator (see Fig. 6.18).

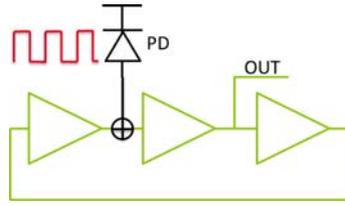


Figure 6.18: Optical clock receiver based on injection locked ring oscillator

In this topology, the photodiode introduces current pulses into the node whenever light is shine on it. These periodically injected current pulses, provided that they are strong enough, will eventually lock the ring oscillator frequency to the optical clock frequency. The minimum optical power needed to lock an ILO to the injected signal depends inversely on the difference between the ILO's free running frequency and the received optical clock frequency. Hence, a power efficient design needs to match the free running frequency of the ILO to the input clock frequency as much as possible. Process, temperature, and supply voltage variations pose a big problem here, as they severely alter the free running frequency of ring oscillators. To solve this problem, ILOs are often equipped with calibration functionality [64] [63]. Process variations are easy to handle, as the calibration has to be done only once, but ageing and especially temperature and supply voltage variations occur and change during runtime. Furthermore, tracking environmental variations is of high importance if a constant phase difference between optical clock input signal and the receiver's output signal is crucial. This is in particular true if data receivers are connected to the clock receiver, because the frequency difference between the free running frequency and the locking signal defines the output phase of the locked ILO. Therefore, if due to voltage or temperature variations the free running frequency alters, the phase of the ILO would change and trigger the data receiver at wrong time instances. To resolve these difficulties, two solutions are presented in this thesis: the first solution is based on the comparison of the ILO clock output with a reference clock, acquired with a separate high power clock receiver. In this solution the high power clock receiver will only be switched on occasionally to recalibrate the ILO. The second solution continuously compares internal phases of the ILO to calibrate itself.

6.3.2 Theoretical Background

The locking phenomenon, in ring oscillators, is best explained in time domain as described in [70]. The ring oscillator's frequency is defined by $2N \cdot t_{Delay}$, where N stands for the number of inverters inside the ring and t_{Delay} is a single inverter's delay time. In a rough model of the injection process, the injected current leads to an altered delay time, $t_{Delay} - \Delta t_{Inj}$ of the inverter, whose output is connected to the injection node. Without loss of generality, in the following this inverter is considered to be the first inverter of the ring. The delay time (Δt_{Inj}) changes because the injected current contributes to the net current charging/discharging the output

capacitance (see Fig. 6.19). Reduced delay times will occur when the injected current pulse arrives during the rising edge, while longer delay times result from current pulses arriving during falling edges. The amount of delay change depends on the amplitude and the duration of the current pulse (and therefore on the optical power) as well as on the time or phase difference between the injection event and the edge.

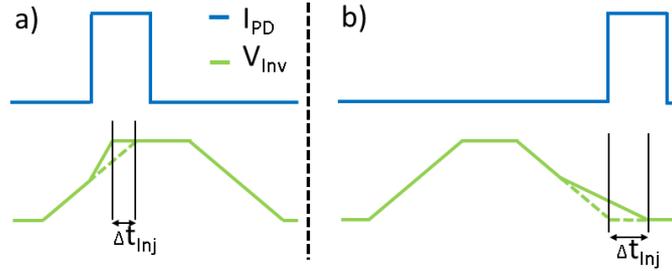


Figure 6.19: Change of an inverter's delay time due to current injection

Based on these ideas a new theoretical model was developed in this work. In a first order approximation, the inverters can be modelled as voltage controlled current sources. In this case the delay time of the inverter can be expressed as:

$$t_{Delay} = \frac{V_{DD}C_{out}}{2I_{Inv}}, \quad (6.1)$$

where C_{out} is the capacitance to ground at the inverter output node and I_{Inv} the current sourced by the inverter. The factor $1/2$ stems from the fact that to compute the delay time the following inverter's threshold voltage is the voltage reference and therefore $V_{DD}/2$. The highest possible Δt_{Inj} is achieved when current is sourced from the photodiode during the entire transition. In this case t'_{Delay} and Δt_{Inj} become:

$$t'_{Delay} = \frac{V_{DD}C_{Inj}}{2(I_{Inv} \pm I_{PD})}, \quad (6.2)$$

$$max(\Delta t_{Inj}) = \frac{V_{DD}C_{Inj}I_{PD}}{2I_{Inv}(I_{Inv} \pm I_{PD})}, \quad (6.3)$$

where C_{Inj} is the capacitance at the injection node and I_{PD} the current injected by the photodiode. Depending on whether the injection starts at the beginning of the edge or later, Δt_{Inj} will change linearly with the percentage of the edge time covered by the injected pulse. The complete expression for Δt_{Inj} is therefore:

$$\Delta t_{Inj} = \frac{V_{DD}C_{Inj}I_{PD}}{2I_{Inv}(I_{Inv} \pm I_{PD})} \cdot \left(1 - \frac{\phi}{t_{Delay}}\right), \quad (6.4)$$

where ϕ is the time difference between corresponding edges in the injected clock signal and the ILO's clock signal, expressed as percentage of t_{Delay} . This formula only holds under the condition that the photocurrent pulses are long enough, so that the injection node is charged at the time it ends, and short enough to not influence the following edge.

From Eqn. 6.4 the locking range can be derived, since for the steady state

$$T_{Ck} = 2N \cdot t_{Delay} - \Delta t_{Inj} \quad (6.5)$$

has to hold, where T_{Ck} represents the period of the injected signal. If Eqn. 6.3 is inserted the locking range is obtained:

$$2N \cdot t_{Delay} - \frac{V_{DD} C_{Inj} I_{PD}}{2I_{Inv}(I_{Inv} + I_{PD})} < T_{Ck} < 2N \cdot t_{Delay} + \frac{V_{DD} C_{Inj} I_{PD}}{2I_{Inv}(I_{Inv} - I_{PD})}. \quad (6.6)$$

Before the ILO gets locked to the injected signal its phase will roll over the injected phase. This continues until a first pulse hits the correct edge, so that the following edge will also hit this edge, as shown in Fig. 6.20. Without loss of generality but for better clarity it is assumed that the injected frequency f_{Ck} is higher than the oscillator's free running frequency f_{FR} . Therefore their periods behave like $T_{Ck} < T_{FR}$ and the earlier called "correct" edge is the rising edge.

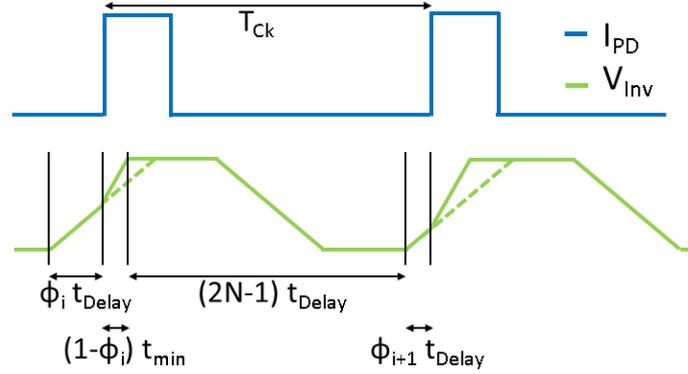


Figure 6.20: Timings while converging towards a locked steady state

From Fig. 6.20 the following equation can be derived:

$$T_{Ck} = (1 - \phi_i)t_{min} + \xi + \phi_{i+1}t_{Delay}, \quad (6.7)$$

where t_{min} is the positive version of Eqn. 6.2 and ξ equals $(2N - 1)t_{Delay}$. This recursive description of ϕ can be solved to

$$\phi_i = \left(\frac{t_{min}}{t_{Delay}} \right)^i \phi_0 + \frac{T_{Ck} - \xi - t_{min}}{t_{rise}} \sum_{k=0}^{i-1} \left(\frac{t_{min}}{t_{Delay}} \right)^k, \quad (6.8)$$

$$= \left(\frac{t_{min}}{t_{Delay}} \right)^i \phi_0 + \frac{T_{Ck} - \xi - t_{min}}{t_{rise}} \frac{1 - \left(\frac{t_{min}}{t_{Delay}} \right)^i}{1 - \left(\frac{t_{min}}{t_{Delay}} \right)}. \quad (6.9)$$

To prove that the model converges towards a steady and locked state, three things have to be shown: first, $\lim_{i \rightarrow \infty} \phi_i$ has to converge. Second, the convergence value has to be in the interval $[0..1]$, because ϕ and therefore the model has only meaning on this interval. Third, during the entire convergence process ϕ must stay within this interval for the same reason. To prove these three points it is assumed that T_{Ck} lies in the locking range and that therefore

$$t_{min} \leq T_{Ck} - \xi \leq t_{Delay} \quad (6.10)$$

holds. The first point can be easily verified knowing that $t_{min} < t_{Delay}$:

$$\lim_{i \rightarrow \infty} \phi_i = \frac{T_{Ck} - \xi - t_{min}}{t_{rise} - t_{min}}. \quad (6.11)$$

Using 6.10 and substituting $T_{Ck} - \xi$ with either t_{min} or t_{Delay} the second point is also proven, as the interval for the limit is:

$$0 \leq \lim_{i \rightarrow \infty} \phi_i \leq 1. \quad (6.12)$$

To prove that ϕ_i stays in the interval for every i , the two cases $T_{Ck} - \xi = t_{min}$ and $T_{Ck} - \xi = t_{Delay}$ are considered and afterwards the function's monotonicity concerning $T_{Ck} - \xi$ is shown. For $T_{Ck} - \xi = t_{min}$ it follows that

$$\phi_i = \left(\frac{t_{min}}{t_{Delay}} \right)^i \phi_0 \quad (6.13)$$

which is always in the interval because ϕ_0 is per definition inside and $\left(\frac{t_{min}}{t_{Delay}} \right)$ is in the interval as both values are positive and $t_{min} < t_{Delay}$. Therefore, also their product lies between 0 and 1. For $T_{Ck} - \xi = t_{min}$ it follows that

$$\phi_i = \left(\frac{t_{min}}{t_{Delay}} \right)^i \phi_0 + \left(1 - \left(\frac{t_{min}}{t_{Delay}} \right)^i \right), \quad (6.14)$$

$$= 1 - \left(\frac{t_{min}}{t_{Delay}} \right)^i (1 - \phi_0). \quad (6.15)$$

The same arguments as for t_{min} hold in this case. Combining these arguments with the fact that the value of the expression 1 minus a value of the interval $[0..1]$ stays in the same interval, it is proven that ϕ_i stays also for this case in the $[0..1]$ interval. To prove the functions monotonicity it is enough to realize that the function is linear with respect to $T_{Ck} - \xi$. It is therefore proven that the system converges to a phase stable point once the current pulse was injected at the correct edge. To show the models validity a ring oscillator comprising 7 inverters with $T_{Fr} = 197.6$ ps was injected with a clock signal of 5 μ A of amplitude and a $T_{Ck} = 196.1$ ps. The simulation and the model results are shown in Fig. 6.21.

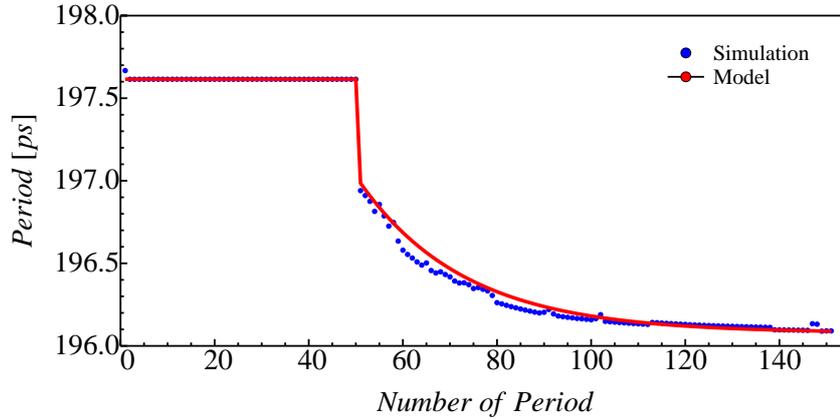


Figure 6.21: Comparison between the model and simulation, when the system converges towards the steady state.

Limits of this approximation are: firstly, the assumption of the constant sourcing strength of the inverters, independent from the output voltage. Secondly, the dependence of the second inverter's delay time on the rise time of its input is neglected, which is altered due to the injection. This effect can even propagate through the inverter chain for a few inverter instances.

Nevertheless, using this model it becomes evident that if environmental variations change the free running frequency to f'_{FR} (because the inverter's delay change to t_{Env}), the amount of corrections will be modified to maintain the lock so that $T_{Ck} = 2N \cdot t_{Env} - \Delta t'_{Inj}$ is still fulfilled.

Delay Control Techniques

For a ring oscillator comprising three inverters with $W_{NMOS} = 200$ nm, $W_{PMOS} = 420$ nm, length equal to 28 nm and additional parasitic capacitive loads of 10 fF the free running frequency dependence on corner variations was simulated to be:

	SS	TT	FF
f_{FR} [GHz]	3.6	4.0	4.4

To lock this oscillator to an input clock signal of 4 GHz under every condition, a locking range of 800 MHz would be required. The locking range, as shown in Eqn.6.6, depends on the amplitude of the injected current. It is therefore important to be able to calibrate the ring oscillator's free running frequency in order to reduce the need of a wide locking range. There are several known ways to control inverter delays and therefore the free running frequency of a ring oscillator. One option is the current starved ring oscillator. This technique inserts a PMOS transistor on-top of the PMOS-NMOS stack of the CMOS inverters to regulate the maximal drawn current by the inverter using the PMOS's gate voltage, controlling the delay

of the inverter. Another possibility is to introduce a transistor in series to the connections between successive inverters in order to regulate the charge time of the succeeding inverter input, using the controlled resistance of the series transistor. In the circuit proposed in this work a third option is implemented, taking advantage of the fully-depleted SOI CMOS 28nm technology. It is based on the biasing of the transistor back-gate, which allows changing the threshold voltage of the transistor and therefore the inverter's delay time.

6.3.3 Aided Calibration

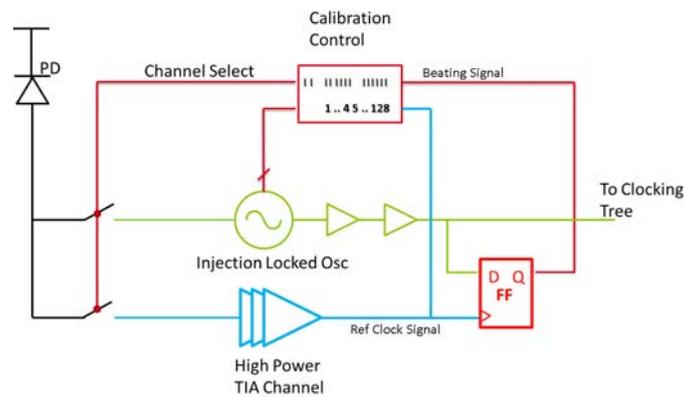


Figure 6.22: Calibration loop architecture based on a reference clock signal

Fig. 6.22 presents the proposed architecture of an optical clock receiver incorporating an injection locked oscillator surrounded by a tuning mechanism. The idea is to compare the signal of the ILO to another clock signal reference and use the error signal to tune the ILO.

The signal flow in the proposed architecture is the following: during the calibration of the system only a high-power-consumption, high-sensitivity TIA is connected to the photodiode (blue circuitry). It provides the reference clock signal. The ILO runs at its free running frequency (f_{FR}). In order to measure the frequency difference of the two clock signals they are used as trigger and data signal of a flip flop (red circuitry). The output signal of the flip flop oscillates at the frequency difference (beating frequency) of the reference signal f_{CK} and f_{FR} , see Fig. 6.23. The clock input triggers the flip flop to copy the present state of the data input to its output, the circuit works therefore comparably to a stroboscope.

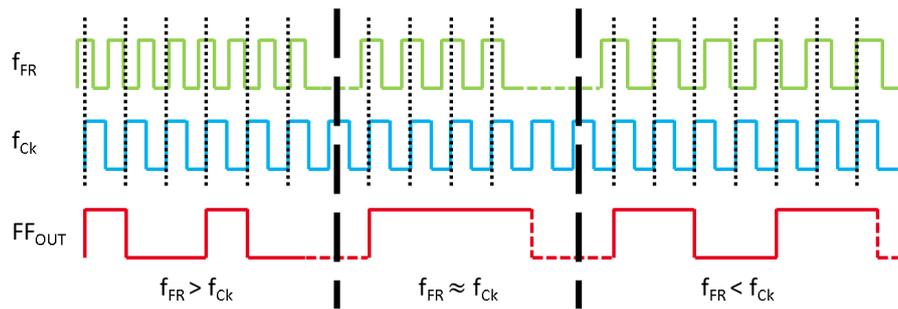


Figure 6.23: Beating signal generated by the flip flop

This beating signal is fed into a calibration control unit. This unit can be built in several ways. One possibility is to use digital electronics implementing the algorithm depicted in Fig. 6.24, represented as a block diagram. This particular algorithm assumes that the ILO was designed in a fashion that if the ILO control register is zero, f_{FR} is bigger than f_{Ck} . During runtime the length of the beating times is measured and compared to a pre-set minimum. If it is not high enough (and therefore the two frequencies not identical) the calibration control circuit increments the ILO Ctrl register.

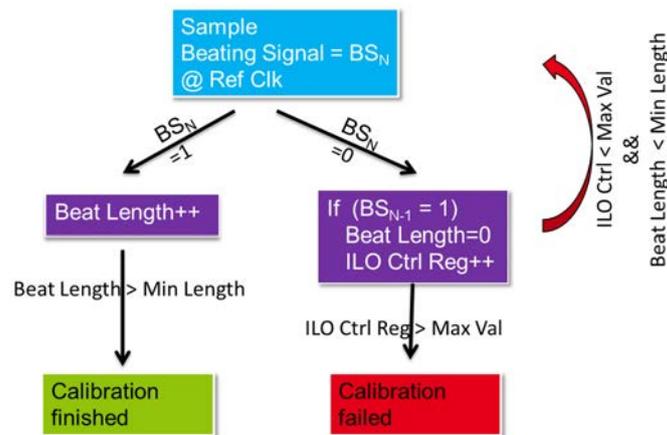


Figure 6.24: Calibration algorithm

This algorithm could be easily expanded to also search in the other direction. For example, by measuring whether the beating time decreases after changing the ILO control register. After finishing the calibration the channel selection signal is used to disconnect the power-hungry TIA and connect the ILO to the photodiode. If the system is carefully designed it can be assured that after calibration the ILO runs in a locked mode with the signal from the PD leading to a phase stable ILO signal.

The algorithm was implemented in verilog and the used ring oscillator comprised 3 inverters, each with $W_{NMOS} = 80$ nm, $W_{PMOS} = 168$ and loaded with 3.5 fF. The digital to analog conversion from the calibration logic for the back-gate voltages was done using coupled binary scaled current sources loaded by a resistor. This was done in a symmetrical way so that a voltage from 0 upto 1 V was created for the NMOS transistors as well as a voltage from 0 to -1 V for the PMOS transistors, see Fig. 6.25.

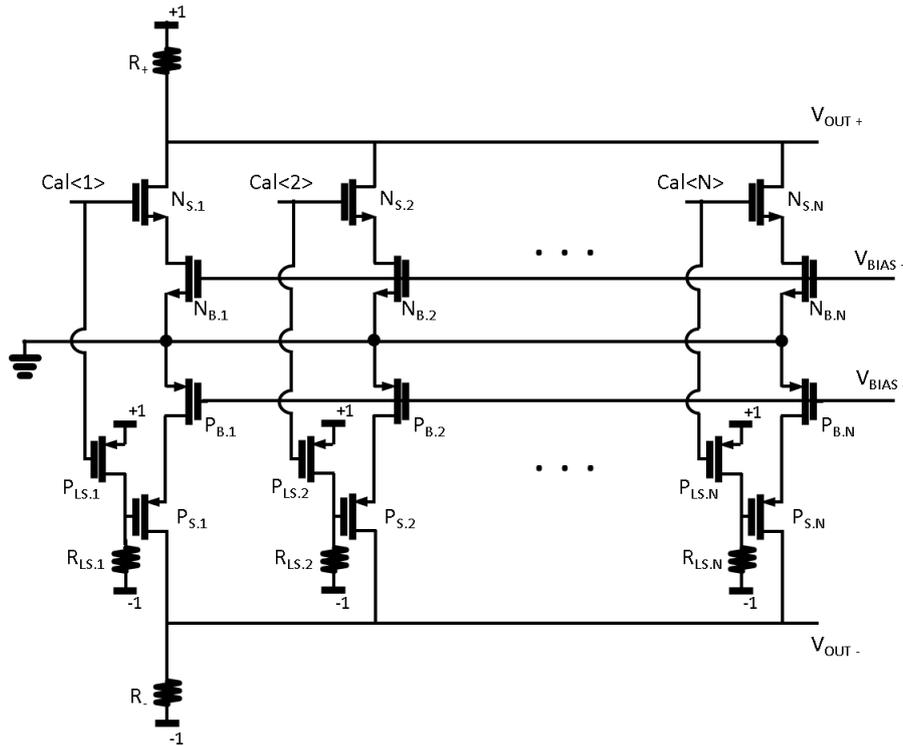


Figure 6.25: Symmetric digital to analog converter for ILO

Finally, transient time simulations were run to test the architecture's behaviour. Fig. 6.26 shows waveforms of the system's calibration process. At the beginning of the calibration f_{FR} is 4.2 GHz (central panel), while f_{CK} is set to 3.7 GHz. It is clearly visible how f_{FR} is lowered due to the adaptation of the back-gate voltages (first panel), which are steered by the DAC-IN register (fourth panel). The expansion of the beating pulses (second panel) is also visible. In the end the channel select signal switches when f_{FR} equals f_{CK} .

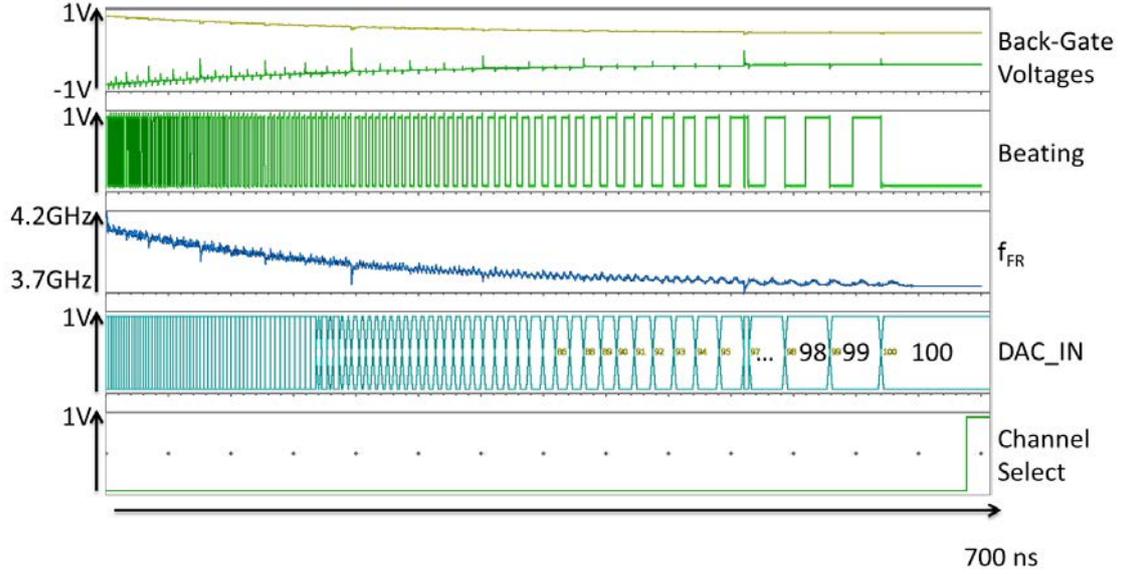


Figure 6.26: Calibration of the ILO's f_{FR} based on its beating signal with a reference clock signal

6.3.4 Calibration by phase detection

A major drawback of the aided calibration approach is that even if the system is able to adapt the free running frequency in both directions and could therefore be used during runtime, the data flow has to be stopped for at least a few clock cycles. This is needed to feed the TIA reference clock signal into the clocking tree. Another pause has to be made after the calibration ends to feed the ILO signal back into the clocking tree. Furthermore, the theory has shown that the phase difference of the ILO's output and the injected clock signal (ϕ) depends on the difference of f_{Ck} and f_{FR} . This makes continuously calibration necessary as the phase has to stay constant for high-speed data receivers. Therefore, a continuously working calibration technique based on phase detection was developed.

The underlying idea of the newly proposed circuit is based on the measurement of the amount of correction each injection forces on the ILO when it is locked. In other words $\Delta t_{Inj} = T_{Ck} - T_{FR}$ needs to be measured. Our solution is proposed in Fig. 6.27.a, for the particular case of $N = 3$. The ring oscillator ILO is connected to its own open loop replica. The open loop replica shares the input node with the first inverter of the ILO. The timings of the different nodes in both circuits are shown in Fig. 6.27.b. The panel labels correspond to the voltages of the related nodes in Fig. 6.27.a. We consider the case in which $f_{Ck} > f_{FR}$. Without loss of generality but for easing the comprehension of the signal development inside the circuit we represent a rising edge in the real ILO by a positive voltage pulse in Fig. 6.27.b. Note that the same figure can be used for the case $f_{Ck} < f_{FR}$ if the voltage pulses are considered to

be falling edges, and the delay signs are reversed. Following this representation, let's assume that the ring ILO starts with a pulse on node X_{A1} . The pulse is propagated along the chain with t_{Delay} between two outputs. We consider for the moment that both inverter chains are perfectly matched. If the open loop total delay along the chain is larger than the injected clock period, a correction in the delay of the ring ILO will happen. Accordingly, the pulse will arrive earlier to the node X_{A1} in order to match the input clock period. Hence, while the pulse appears after $t_{Delay} - \Delta t_{Inj}$ at node X_{A1} , it appears t_{Delay} later at X_{B1} . The two pulses travel through the ring and the open loop inverters chain with a small time shift equal to Δt_{Inj} , that can now be measured with a phase detector at any corresponding pair of nodes.

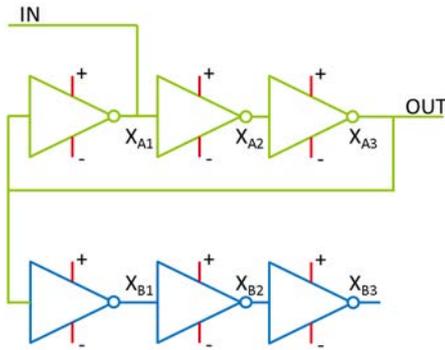


Figure 6.27.a: Proposed auto-calibration circuit

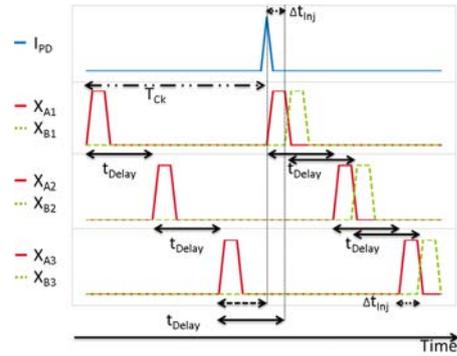


Figure 6.27.b: Timing diagram of the proposed ILO based clock receiver

Early/Late Detection

The challenge of the proposed continuous, self-calibration technique is that the error signal (Δt_{Inj}) is in the range of pico-seconds, if the system shall work with small injection signal powers in the GHz regime. Classical phase detector topologies [58] designed for PLLs are not fast enough to resolve such a small time difference. This work proposes to use an early/late detector instead. The suggested topology is based on positive feedback, shown in Fig. 6.28. In order to achieve high speed detection, the circuit only detects which of the two signals arrives earlier, containing the information whether the free running frequency is higher or lower than the injected frequency. The proposed early/late detector is based on a latch. Its inputs ϕ_1 and ϕ_2 relate to corresponding nodes inside the ring and the open loop replica. During reset (when ϕ_1 and ϕ_2 are low) the latch is drawn into a metastable state at which the two output signals OUT1 and OUT2 equal $\frac{V_{DD}}{2}$. The moment one of the input signals goes high the corresponding latch arm is connected to ground. After a small delay (introduced by an inverter in the path of the input signals), the latch is released from the forced metastable state and latches into the corresponding state. The bottom circuitry, in Fig. 6.28, comprising a flip-flop, two switches and

two capacitors, is used to steer the phase detector's output when the input signals arrive with time difference below the phase detectors temporal resolution. The circuitry will unbalance the latch alternately leading to an alternating output that can be filtered out easily. This creates a "dead zone" comparable to the behaviour of classical phase detectors.

The proposed circuit was designed at transistor level in the 28nm fdsoi cmos technology. The switches S1 and S2 were realized by parallel NMOS and PMOS transistors each $1 \mu\text{m}$ wide. The switches S3 and S4 correspond to the clock feedthrough compensated switches shown in Fig. 6.13 and are $160 \mu\text{m}$ wide. The switches S5 and S6 are minimal sized NMOS transistors. The capacitors C1 and C2 have 1 fF of capacitance. All inverters are constituted by NMOS transistors of 378 nm width and PMOS transistors of 538 nm width.

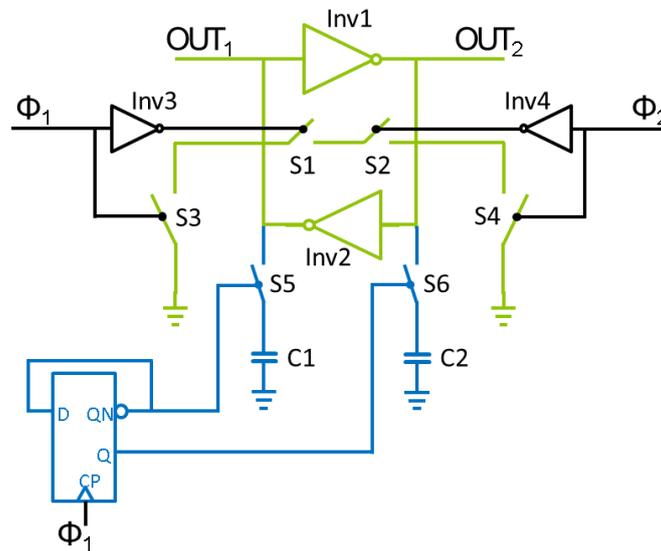


Figure 6.28: High resolution early/late detector

The detector's temporal resolution is defined as the time offset between two signals needed so that the detector will give the correct output. The necessity of this offset stems from imperfections like mismatch or false triggering due to noise. To determine these two influences Monte Carlo simulations of transient time simulations were run including time domain noise. The rms value of the time offset obtained by these simulations is 1.5 ps, proving the detectors high temporal resolution.

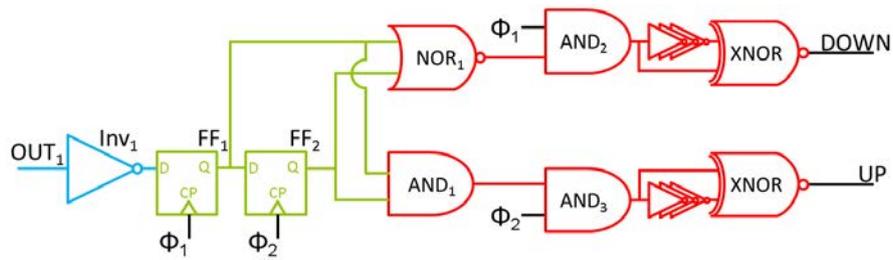


Figure 6.29: Alternating output filter

In order to filter out the alternating output of the early/late detector when the signals arrive too close to each other, the circuit of Fig. 6.29 has been invented. It uses two flip-flops as a shift register to store the last two results and generates only pulses when the last two successive results were equal. In Fig. 6.30.a the case of alternating inputs is shown. The shifting of the alternating bits, see FF₁ and FF₂, results only in zeros at the output of the NOR₁ and the AND₁ gate. On the other hand in Fig. 6.30.b the case of three sequential zeros is presented. The NOR₁ gate rises its output and in combination with the AND₂ gate three pulses on the DOWN output are generated.

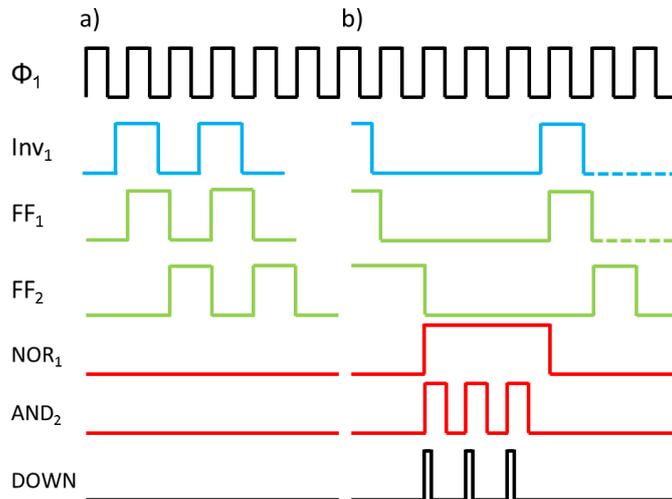


Figure 6.30: Filter outputs for an alternating input and an input with 3 successive bits of equal value

The full calibration system is shown in Fig. 6.31, including the ILO, the proposed early/late detector and a switched capacitor circuit to control the ILO. The switched capacitor circuit comprises a PMOS, whose gate is connected to the UP signal, a NMOS, whose gate is connected to the DOWN signal and a capacitor connected to their drains. The NMOS is 80 nm wide, the PMOS is 200 nm wide and the capacitor

has a capacitance of 500 fF. An inverted and signal shifted version of this circuit supplies the back-gate voltages for the PMOS transistors inside the ring.

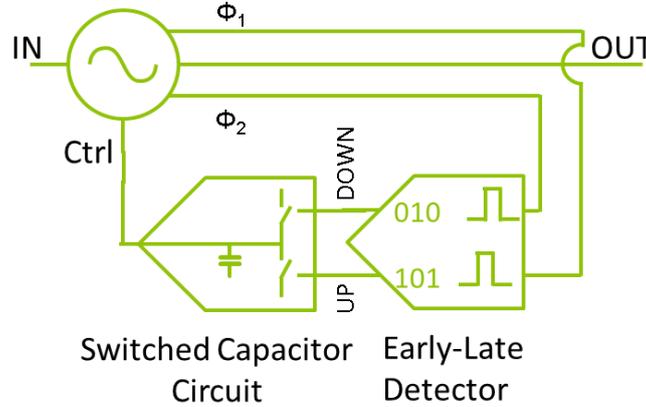


Figure 6.31: The full calibration system

Jitter Studies

The minimal optical power needed for the proposed optical clock receiver is defined by the system's ability to match f_{FR} to f_{Ck} . This capability is limited by timing uncertainties, notably noise and random mismatch induced jitter. Therefore, transient simulations of the free running oscillator, including time domain noise, were run to measure the jitter due to noise at the phase detector inputs. Additionally, Monte Carlo simulations were run to determine jitter due to the random mismatch between the corresponding nodes in the ILO and its open loop replica. The test device consisted of a ring oscillator realized in a 28nm FDSOI process comprising three minimal sized inverters and its open loop replica. The ring oscillator's free running frequency was 2.5 GHz. The resulting noise and random mismatch induced jitter at the phase detector inputs are 680 fs and 8.9 ps, respectively. Their combined effect introduces uncertainty in the calibration loop, that has to be compensated by the locking mechanism described in the theoretical section, of $\Delta t_{Injection} = 9.6$ ps. In order to warranty this correction the current pulses need to have at least $5 \mu\text{A}$ of amplitude and a duty cycle of 10%. Since the biggest timing uncertainty is due to random mismatch, increasing the size of the transistors and load capacitors will reduce the uncertainty leading to lower minimal injection currents. Hence, depending on the systems needs, electrical power consumption and footprint can be traded off against minimal injection currents, and therefore reduced power consumption in the optical clock generator.

Results

To prove the circuit's functionality, full system transient simulations were run, including time domain noise. Fig. 6.32 shows the calibration technique operating through different waveforms. For the first 5 ns the ILO runs free at a frequency of 3 GHz, with the optical input clock switched off. Afterwards a 2.9 GHz optical clock is switched on, resulting in a $25 \mu\text{A}$ injected current signal with a duty cycle of 10 %. During the acquisition phase the ILO's frequency falls quickly to 2.9 GHz (first panel). During this time the back-gate voltage control circuitry is kept off and the free running frequency stays at 3 GHz, because the back-gate voltage remains constant and t_{Delay} does not change (see panel 2). The early/late detector measures the difference between the input clock frequency and the free running frequency. Accordingly, it rises the DOWN output in panel 3. At $t = 25 \text{ ns}$ the calibration is turned on by activating the back-gate voltage control circuitry, which leads to the drop of the back-gate voltage shown in the second panel. During the decrease of the back-gate voltage the output frequency of the ring oscillator stays constant at 2.9 GHz as it is permanently locked. There is nevertheless a small influence visible, which is due to the speed of the descent, changing t_{Delay} during one cycle. After the back-gate voltage settles to the right value the DOWN and UP signals stay low and the output frequency and the free running frequency remain constant at 2.9 GHz.

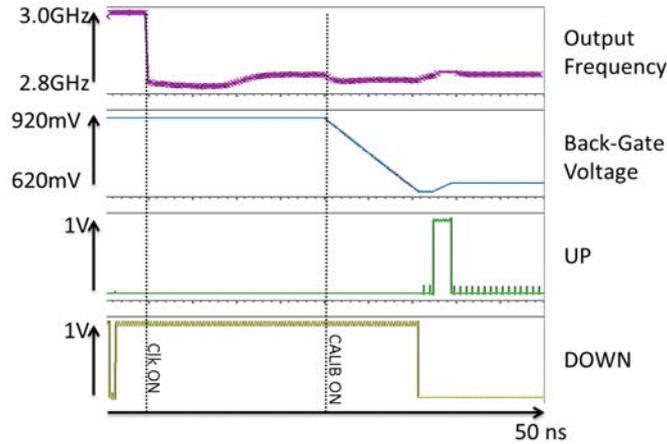


Figure 6.32: Transient simulations showing the tracking capabilities of the circuit

The proposed topology is also capable of calibration assisted lock acquisition as shown in Fig. 6.33. At the start-up of the system the back-gate voltage is initialized to 0 V, which corresponds to a free running frequency of 2.25 GHz. After 5 ns a clock signal at 2.9 GHz is injected, having an amplitude of $5 \mu\text{A}$ and a duty cycle of 10 %. In this case, the initial difference between $f_{FR}=2.25 \text{ GHz}$ and $f_{CK}=2.9 \text{ GHz}$ is so large that the injection mechanism alone would not be able to lock the ILO, with the low amplitude input current provided. However, the calibration loop operates in

the initial non-locked state, changing f_{FR} up to a value in which the injection occurs. The underlying mechanism is that even if the current injection occurs initially at rolling phases, when the pulse hits the right edge it will increase the chance that the following pulse will also hit the right edge. This will eventually lead to repeated phase shifts in the same direction inside the ILO, triggering the calibration loop to act in the right direction. On the other hand if the pulse hits the wrong edge it will reduce the chance that the next pulse also hits this edge, reducing the probability of driving the calibration loop in the wrong direction. Fig. 6.33 shows that the right back-gate voltage is found after 90 ns, locking the ILO to the injected signal at 2.9 GHz. The acquisition range of the system spans the full range of accessible free running frequencies, from 2.25 GHz up to 3 GHz in any case. This range could be further expanded using other frequency tuning techniques or increasing the back-gate control voltage range, but the current range is already sufficient to cover the entire range of PVT variations for this circuit. The full system consumes 500 μW . Further power reduction can be achieved when after the establishment of the back-gate voltage the calibration loop is switched off and only powered up if needed, resulting in a power consumption as low as 60 μW .

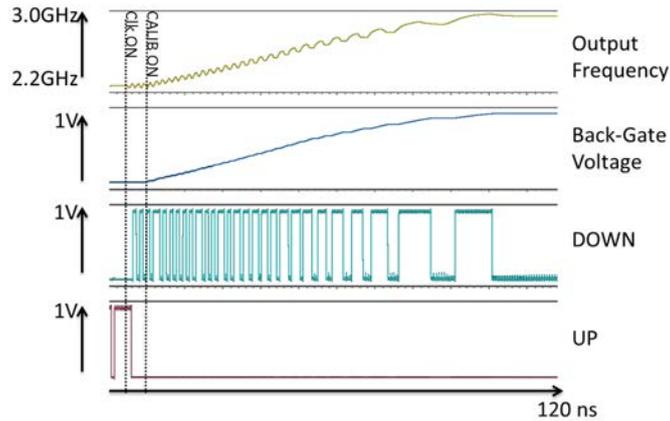


Figure 6.33: Calibration assisted lock acquisition

6.3.5 Conclusion

Injection locked oscillators have various applications, especially ring oscillator based designs are very interesting due to their low power consumption and footprint. The biggest problem in using these devices in VLSI products is their sensitivity to process temperature and supply voltage variations (PVT). This work presented calibration techniques for injection locked ring oscillators. The phase detection based on early-late detection of phases inside the ILO and its open loop copy enables ILOs to track the entire range of PVT variations while still supplying the right clock signal to the circuit. The presented circuit consumes 500 μW during calibration and only 60 μW

during idle time. Its optical sensitivity is $5 \mu\text{A}$ and it has a very small footprint. If the feedback chain is running the solution shows comparable results to the state of the art shown in the following table. In this case the integrate and dump receiver based solution is even more power efficient although it has to be considered that ILOs can be used to generate several clock phases. If the feedback loop is turned off, the presented circuit compares favourable to the state of the art.

Front Ends:	[63]	[64]	IdA ²	This Work
Freq [GHz]	11	1	2	3
S_O [μA]	55^1	8.6	5	5
P_R [μW]	2770	186	135	60 - 500
P_L [μW]	3050	230	160	85 - 525

Finally, please note that the current pulses could also be injected by an external inverter which might be at the end of a clock tree. The architecture could therefore also serve for clock distribution inside chips.

6.3.6 General Conclusion

This chapter presented two approaches for optical clock channel receivers. The first receiver is based on the integrate and dump receiver architecture. A self-triggering mechanism was proposed to make it suitable as a clock receiver. This architecture presents the smallest overall energy consumption for continuously calibrating clock receivers and has a very robust and simple tuning mechanism. The tuning mechanism is based on measuring the duty cycle of the output signal. Therefore, it always provides a 50 % duty cycle independently from the shape of the input signal.

The second solution proposed is an injection locked oscillator. It was explained that ILOs need calibration due to PVT variations. A mechanism was introduced that is based on monitoring the phase shift induced by the locking signal. The phase shift is measured by comparing an internal phase with the phase of an open loop copy of the oscillator. With the feedback loop being active, this solution consumes slightly more than the integrate and dump solution but it presents a good base for clock phase generation as well as clock division and multiplication.

Concludingly, the integrate and dump receiver technology is preferable for basic data receivers that only need a single phase from the clocking signal. For more complex receiver designs the injection locked oscillator is the more interesting solution.

¹A TIA with $T = 3 \text{ k}\Omega$ and a photodiode with a responsivity of 0.9 A/W were assumed to convert the given minimal voltage swing to an optical sensitivity.

²Self-Triggered Integrate and Dump architecture from the previous section.

Chapter 7

Conclusion and Outlook

“The promise given was a necessity of the past; the word broken is a necessity of the present.”

Niccolo Machiavelli

In this thesis silicon photonic links for future multi-chip modules were optimized, in order to contribute to the solution of the bottlenecks, faced in modern high performance computing systems. These bottlenecks are the power consumption of HPCs and the interconnect bandwidth between the computing nodes. The thesis presented optimized solutions for a 65nm bulk and a 28nm FDSOI technology. This work contributed to the state of the art with the following aspects:

1. **State of the Art:** In order to introduce the reader into the basics of silicon photonic links, all needed optical elements were discussed in the first chapter. It was explained why future multi-chip modules are expected to use a silicon photonic interposer for data transport and chips produced in modern CMOS technology nodes for data processing. For minimal parasitic loadings and high computing density, the chips will be connected to the silicon interposer using flip-chip techniques. The optical interposer is expected to incorporate grating couplers to couple light from an external laser into the chip, ring resonators to modulate and filter the light, and germanium photodiodes to detect the light. The chapter also introduced the concepts of different transmitter circuits. Highly efficient drivers with consumptions as low as 135 fJ/b were reported. Furthermore receiver topologies, such as transimpedance amplifiers or integrating front-ends, were explained. The highest reported power efficiency was 170 fJ/b at a sensitivity of -6.8 dBm for a heterogeneous system. The sensitivity corresponds to a laser power consumption of 100 fJ/b if the system runs at 10 Gbps and a wall plug efficiency of 20% is assumed. These three consumptions sum up to 405 fJ/b and would therefore succeed in undercutting the goal of 1 pJ/b. Finally, several implementations of full optical links were discussed. The most power efficient full link reports a consumption of 2 pJ/b.

This shows that a full transceiver including serialization, thermal control and optical coupling is a complex system that needs to be further optimized to reach the 1 pJ/b goal.

2. **Modelling:** It is inevitable to use models to optimize a complex structure such as optical links. It was demonstrated that purely analytical models of circuits fabricated in deep submicron technologies can be used to determine general trade-offs. But they are not capable of predicting the right location of extrema in the design parameter space. For this reason, a performance database, based on transistor level simulations was built for three different transimpedance amplifier topologies: feedback versions of a common source topology, a push-pull topology and a double stage push-pull topology. The swept design parameters were:

Technology	65 nm	28nm
Output Load [fF]	10, 100	10, 40
Input Load [fF]	10 .. 200	10 .. 200
Feedback Resistance [k Ω]	0.5 .. 40	0.5 .. 40
NMOS Transistor Width [μ m]	0.135 .. 20	0.60 .. 20
V_{DD} [V]	1.2	1.0

Furthermore, for all other elements of the photonic link analytical models were constructed predicting the power consumption of these elements depending on the link's bit rate. Also in this case, the models were based on an analytical construct of the functioning of the elements and were calibrated using results from designed and simulated elements.

3. **Trade-Offs:** Using the analytical models and a database from the literature study, the main trade-off in the design of silicon photonic links was identified as needed optical power against bit rate. It can be found in various stages of the link. A first encounter of this trade-off is inside the studied TIAs, where bandwidth can be traded against transimpedance, e.g. for the 65nm technology the push-pull topology could have a bandwidth of 15 GHz and a transimpedance of 1 k Ω or a transimpedance of about 40 k Ω and a bandwidth of 1 GHz. Equally, for the 28nm technology a maximal bandwidth of 30 GHz was shown at a transimpedance of 1 k Ω and a transimpedance of about 40 k Ω at a bandwidth of 1 GHz. A second encounter is the conversion between bandwidth and bit rate, where higher input powers allow higher conversion factors. This leads to the top level trade-off between the receiver's sensitivity and the bit rate independent power consumption of the ring resonator tuning. The same trade-off can also be found inside the transmitter, as lower bit rates might allow higher output swings, reducing the power penalty due to a finite extinction ratio.

4. **Energy Efficiency:** The energy efficiency is the central point of the proposed circuitry and the optimization chapter. The optimization was oriented to find the parameter set with the highest efficiency. This was achieved by using the TIA database as central point of the optimization and construct the least consuming link around it. Using the analytical models the power consumption of the entire link was deduced and added to the database. Finally, the database was sorted and the least consuming links were discussed.
5. **Bit Rate:** The central parameter of the optimization is the bit rate of the link. Optimal bit rates were found to be 10 Gbps for the 65 nm technology and 16.5 Gbps for the 28nm technology. Following the analytical models optimal energy efficiencies of 0.67 pJ/b (65nm) and 0.40 pJ/b (28nm) could be achieved. This includes the consumption of the laser, the driver, the de- and serialization, the thermal tuning of the ring resonators and the receiver. This means that the community goal of energy consumptions below 1 pJ/b is already achievable if a correct parametrization of the link is done. The bit rate should be chosen carefully, however the energy per bit versus bit rate curves have a bath tube shape. It followed that bit rate ranges from 8 Gbps to 15 Gbps (65nm) and 12 Gbps to 22 Gbps (28nm) lead to approximately equally efficient links. The optimization did not account for the rising need of complexity in the clock distribution tree which would lead to higher power consumptions inside the receiver and the transmitter. It has therefore to be assumed that the optimal bit rates for complete systems are shifted towards lower bit rates.
6. **Architecture:** The receiver chapter presents fast comparators with high sensitivity (30 mV in 65nm and 15 mW in 28nm). Their availability led to a receiver architecture based on a single stage push-pull inverter as TIA. The TIA is followed by a bench of four comparators sampling the signal time interleaved. Each comparator runs at 2 GSps, summing up to the 8 Gbps bit rate demanded by the HUBEO+ project.
7. **Design:** For the HUBEO+ project a receiver was designed and fabricated in the 65nm technology. The HUBEO+ project envisions a multi chip module with an optical interposer and multiple-writer single-reader links. This means that the receivers will not receive a constant bit stream but there will be periods where no data is transmitted over the channel. Furthermore, depending on the writer configuration, a different optical signal strength will illuminate the receiver photodiode.

This generates two needs: firstly, a wide dynamic range of the receiver. Secondly, the requirement to quickly generate and update the reference voltage for the comparators, based on the average received optical power. For the latter problem this thesis proposes to use an alternating binary training sequence, e.g. 101010, at the start of each packet sent. A new circuit is proposed as well, to obtain the data stream's average value. This threshold control block is

based on taking two samples of the signal with a 180° phase shift to each other and averaging these two samples. To account for the necessary wide average optical power acceptance range, the TIA chapter proposes the possibility to counteract the effects of a changed biasing of the TIA by changing its feedback resistance using a transistor as feedback element.

In total one prototype was designed and fabricated to characterize the complete receiver using electric circuitry to emulate the photodiode. Another prototype was designed to characterize the designed TIA, also in an electro-electro measurement setup. A third prototype allowed to bond the TIA to an external photodiode to test the TIAs opto/electrical functionality.

8. **Characterization:** The designed chip was fabricated and tested. The results for the TIA are very promising and the working range from 0 to $40 \mu\text{A}$ of tolerated average input photocurrent could be verified. Depending on the gate voltage of the feedback transistor a maximal bandwidth of 17 GHz and a maximal transimpedance of $18 k\Omega$ was measured.

The functionality of the TIA could be proven also for the prototype allowing to bond the TIA to an external photodiode. The bonding wires plus bonding pads represent a much higher input capacitance than what the TIA was designed for, hence open eye diagrams could be only measured until 5 GHz.

The receiver without the clocking circuitry consumes only 75 fJ/b. In a complete transceiver for a multi-chip module one clocking circuitry would serve several receivers, for this reason it is neglected at this point. The receiver has a simulated sensitivity of -18 dBm. If the link was realized following the analytical models presented in the optimization chapter, this link would have an efficiency of 860 fJ/b, therefore satisfying the goal of 1 pJ/b.

The receiver was tested and a BER of 10^{-10} was successfully measured at an input photocurrent of $33 \mu\text{A}_{pp}$. The test was done using on-wafer probes which are mechanically unstable over the time it takes to measure BERs. For this reason, further characterization was abandoned and a PCB to characterize the receiver was designed. Unfortunately, at the moment of writing this report, the PCB is still in fabrication.

9. **Clock:** Using silicon photonics an optical clock signal can be distributed in a multiple-chip module with low skew. Furthermore, pulsed lasers can be used to generate a clock signal power efficiently, omitting the need of a modulator. To take advantage of these possibilities, two optical clock receiver architectures are presented in this work, that can be used with short pulsed input. The first topology is based on integrate and dump receivers. This architecture commonly needs a reset signal provided by a clock, which is not suitable for clock receivers, indeed. In order to be capable of receiving a clock, a self-triggering mechanism is proposed. The second architecture is based on an injection locked oscillator. The common problem of injection locked

oscillators is their sensitivity to process temperature and voltage variations. Nevertheless, they provide a good basis as clock buffer and clock divider or multiplier. This work presented a modelling approach and a self-calibration technique based on phase comparison of the actual ILO and an open loop replica. Both approaches achieved high photocurrent sensitivities of $5 \mu\text{A}$ and power consumptions below $150 \mu\text{W}$ running at 2 GHz and 3 GHz, respectively.

7.1 Future Work

The next step to be taken for the HUEBO+ project is the complete characterization of the receiver on the designed PCB. The stable running receiver will also allow to test the presented bit rate to bandwidth conversion formula along with the validity of the optimization results. The validating test consists of finding for each bit rate the needed input power so that the BER stays constant. To verify the role of the jitter in these systems the same test should be done for several jitter values of the injected clock.

The next step in the validation of the concept of silicon photonic links is the fabrication of a full link including all elements. This demonstrator is already in production and incorporates the presented receiver in this thesis. It also includes wavelength division multiplexing as well as several transmitters and receivers in close proximity in order to test the vulnerability of the system concerning cross-talk.

It was proven that the DC current acceptance range of a TIA can be widened if the gate voltage of the TIA's feedback transistor is used as a calibration parameter. To take full advantage of this possibility a feedback loop should be designed.

The performances of the presented clock receivers are based on transistor level simulations including time domain noise and Monte Carlo simulations. Nevertheless, their performances need to be tested using post-layout parasitic extraction based simulations. Finally, they should be implemented in a fabricated chip.

7.2 Outlook

The nowadays-bottlenecks of high performance computers will become bottlenecks of private user systems in the future. It is evident that the interconnect bandwidth density will keep on rising and optics seems to be the only solution at hand to deliver the necessary performances.

It was shown in the optimization chapter that with less static power consumption (e.g. thermal tuning of ring oscillators) the optimal bit rate will decrease. It is predictable that compact optical modulators will be developed in the near future that do not consume any static power (e.g. ring oscillators using materials with counteracting temperature dependencies). Hence the optimal bit rate will be very low; a trend that goes very well with the paradigm of massive parallelization with reduced clock speeds, considered for high performance processing nodes. Therefore,

I expect minimally complex circuitry with very high sensitivities to be the circuitry that will be used in future high performance multiple-chip modules.

Publications

- I R. Polster, J. L. Gonzalez Jimenez, E. Cassan, and P. Vincent, "Optimization of TIA topologies in a 65nm CMOS process," in 2014 IEEE Optical Interconnects Conference, 2014, pp. 117-118.
- II R. Polster, J.-L. Gonzalez Jimenez, and E. Cassan, "TIA optimization for optical network receivers for multi-core systems-in-package," in Microelectronics and Electronics (PRIME), 2014 10th Conference on Ph.D. Research in, 2014, pp. 1-4.
- III R. Polster, J. L. G. Jimenez, E. Cassan, and L. Vivien, "A TIA for optical networks-on-chip in 65nm CMOS," in 2015 IEEE Optical Interconnects Conference (OI), 2015, pp. 109-110.
- IV R. Polster, J.-L. Gonzalez Jimenez, and E. Cassan, "A Novel Optical Integrate and Dump Receiver for Clocking Signals," in IEEE International New Circuits And Systems Conference (NEWCAS), 2015.
- V R. Polster, J.-L. Gonzalez Jimenez, and E. Cassan, "An optical clock receiver based on an injection locked ring oscillator featuring auto-calibration," in IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS), 2015.

Submitted Journal Publications

- I R. Polster, Y. Thonnart, G. Waltener, J.-L. Gonzalez Jimenez, and E. Cassan, "Efficiency optimization of silicon photonic links in 65nm CMOS and 28nm FDSOI technology nodes", submitted to JSTQE.
- II R. Polster, G. Waltener, J.-L. Gonzalez Jimenez, and E. Cassan, "10 Gbps, 570 fJ/b TIA and modulator driver for optical networks-on-chip in CMOS 65nm", submitted to TCASII.

Patent Proposals

- I R. Polster, J. L. Gonzalez Jimenez, I. Miro Panades, "Injection Locked Clock Receiver".
 - II R. Polster, J. L. Gonzalez Jimenez, "Optical Link Clock Receiver".
 - III R. Polster, J. L. Gonzalez Jimenez, "Optical Link Receiver for multi-core system-on-package".
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