Contribution to the design of switched-capacitor voltage regulators in 28nm FDSOI CMOS

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Contribution to the design of switched-capacitor voltage regulators in 28nm FDSOI CMOS

Contribution à la conception de régulateurs de tension à capacités commutées en technologie 28nm FDSOI CMOS

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Abstract

Mobile and multimedia devices offer more and more innovations, enhancements to satisfy user requirements. Chip manufacturers thus propose high performances SoC to address these needs. Unfortunately the growth in digital resources inevitably increases the power consumption while battery life-time does not rise so fast. Aggressive power management techniques such as dynamic voltage and frequency scaling have been introduced in order to keep competitive and relevant solutions. Nonetheless continuing in this direction involves more disruptive solutions to meet space and cost constraints. Fully integrated power supply is a promising solution. Switched-capacitor DC-DC converters seem to be a suitable candidate to keep compatibility with the digital SoCs manufacturing process. This thesis focuses on the design of embedded power supplies architecture using switched-capacitor DC-DC converters. Addressing a large range of output power with significant efficiency leads to consider a multi-ratio power stage. With respect to the typical digital SoC, the input voltage is $1.8\ V$ and the converter is specified to deliver an output voltage in the $0.3-1.2\ V$ range. The reference voltage is varying according to typical DVFS requirements. A modular architecture accommodates the digital design flow where the flying capacitors are situated above the digital block to supply. Power switches are located as an external ring. Such an architecture offers high flexibility. Interleaving strategy is considered to mitigate the output voltage ripple. Such a converter admits the switching frequency as a control variable, linear regulation and hysteretic control are analyzed. Prototypes were fabricated in 28nm FDSOI technology by STMicroelectronics. A power density of 310 $^{mW}/_{mm^2}$ is achieved at 72.5% peak efficiency with a silicon area penalty of 11.5% of the digital block area. The successful design methodology has been also applied to design a negative SC converter for body-biasing purpose in FDSOI. Simulation results demonstrate a strong interest for low power application.

Résumé

Les appareils multimédias portables nécessitent toujours plus d'innovation pour satisfaire les besoins des utilisateurs. Les fabricants de système-sur-puces font donc face à une forte demande en capacité de calcul jusqu'à lors réservée aux ordinateurs de bureau. Ce transfert de performance se répercute inévitablement sur la consommation de ces appareils alors que dans le même temps la capacité des batteries n'est pas en mesure de répondre à cet accroissement. De nombreux compléments matériels et logiciels sont mis en places afin d'économiser l'énergie au maximum sans toutefois dégrader les performances. La modulation de la fréquence de fonctionnement et de la tension d'alimentation est certainement la plus efficace mais reste néanmoins limitée par les coûts et les contraintes d'encombrement exigées par la taille des appareils. La réponse à un tel problème passe nécessairement par l'intégration d'une partie de l'alimentation dans la puce. La conversion DC-DC basée sur des convertisseurs à capacités commutées est prometteuse car elle permet de garder un maximum de compatibilité avec les process CMOS actuels. Cette thèse explore donc la conception d'une architecture d'alimentation utilisant des convertisseurs à capacités commutées.

Un étage de puissance avec une tension d'entrée est de 1.8 V et des ratios programmables permet d'obtenir le rendement maximum pour une plage de tension de sortie allant de 0.3 V à 1.2 V. La tension de sortie peut varier en fonction du point de fonctionnement requit par le système. Afin d'assurer le maximum de compatibilité avec la conception du circuit numérique à alimenter, une architecture modulaire basée sur les capacités MIM est privilégiée. Les capacités sont placées au dessus de la fonction numériques et les interrupteurs de puissance sont insérés à sa périphérie. Cette architecture permet également d'entrelacer les cellules de conversion afin de réduire l'ondulation de la tension de sortie. La fréquence de commutation du convertisseurs est communément utilisée pour réguler la tension de sortie et des stratégies de contrôles linéaires et non linéaires sont donc explorées. Un prototype de convertisseur présentant une densité de puissance de 310 $^{mW}/_{mm^2}$ pour un rendement de 72.5% a été fabriqué dans la technologie 28nm FDSOI de STMicroelectronics. La surface requise pour le convertisseur nécessite que 11.5% de la surface du circuit à alimenter. La méthodologie de conception du convertisseur a finalement été appliquée à un régulateur de tension dans le domaine négatif pour des applications de polarisation de caisson à basse consommation.

Acronym

CMOS Complementary metal oxide semiconductor . . . 1
SoC System on chip . . . 2
IOs Inputs-outputs . . . 2
FDSOI Fully depleted silicon on insulator . . . 4
SMPS Switch-mode power supply . . . 4
SC Switched-capacitor . . . 4
ICs Integrated circuits . . . 5
MOSFET Metal oxide semiconductor field effect transistor . . . 5
SOI Silicon on insulator . . . 8
RTL Register transfer language . . . 8
IP Intellectual property . . . 8
SRAM Static random access memory . . . 11
PCB Printed circuit board . . . 14
C4 Controlled collapse chip connection . . . 14
BGA Ball grid array . . . 15
LDO Low drop-out . . . 16
RF Radio frequency . . . 18
PDN Power delivery network . . . 19
SiP System in package . . . 19
PMICs Power management integrated circuits . . . 19
BOM Bill of material . . . 20
PFM Pulse frequency modulation . . . 20
MIM Metal insulator metal . . . 21
PWL Piecewise linear . . . 39
FM Frequency modulation . . . 57
PI Proportional-integral . . . 63
UTBB Ultra thin body & buried oxide . . . 113
BOX Buried oxide . . . 114
OTA Operational transconductance amplifier . . . 132
GIDL Gate induced drain leakage . . . 149
MOM Metal oxide metal . . . 162

Contents

CHAPTER 1

Introduction

The mass market of multi-media devices exhibits products with ever increasing functions in number and complexity. Behind this offer is hidden a world of powerful integrated circuits. For instance Fig. 1.1 pictures the evolution in computing power and reference clock frequency of various products. To serve these products IC manufacturers employ advanced technology nodes with benefit in density and velocity. Unfortunately these advanced CMOS[1] nodes are not progressing in term of power losses. Jointly the lithium-whatever batteries are indeed progressing in term of energy density but not enough to balance the net increase in power consumption of the circuits. Energy management has thus become a major concern.

The valuable functions in products are designed inside ever growing circuits called

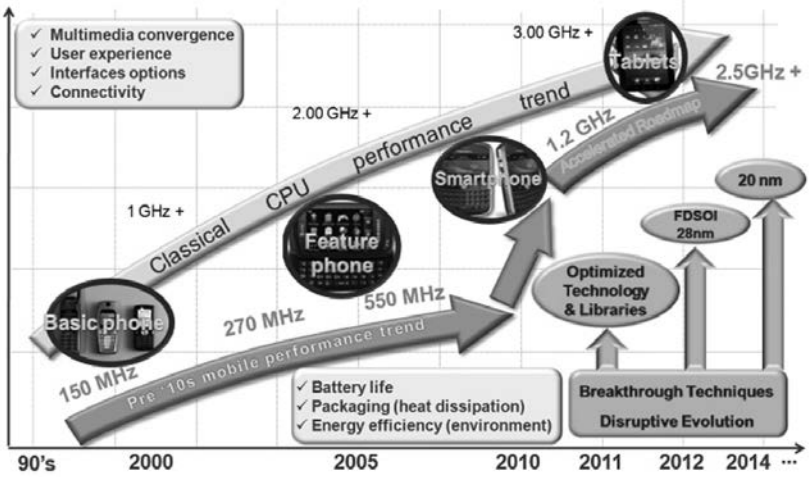


Figure 1.1: Evolution of embedded processor performances over the last decade

[1]Complementary metal oxide semiconductor

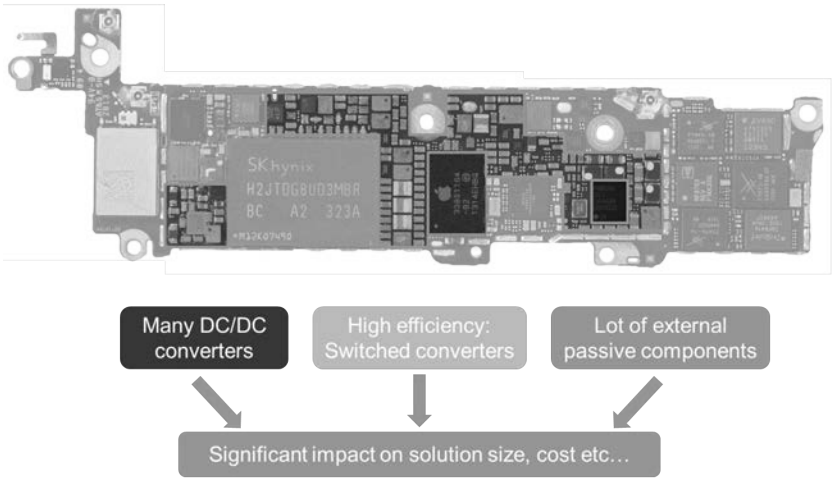


Figure 1.2: Tear-down of a smart-phone main board

system-on-chips. However a SoC[2] remains a collection of individual functions or macro blocks. Each of them have a specific life and the fundamental of energy management is to address the dedicated instantaneous needs of each macro blocks. For instance the power supply voltage of each blocks is different and the time pattern is also different. This in fact conducts to a situation where a lot of voltage levels have to be fed to a given SoC. At board level this requires to produce the voltage levels from the unique battery voltage level. A bunch of converters have to be implemented on board. Fig. 1.2 depicts the board of a standard smart-phone. A small number of SoCs appears and a large number of passive devices and other small active circuits are inserted in between, dedicated to voltage converters. The total footprint of the energy conversion aspect is quite huge.

Basically the power solution is to deliver as much as necessary voltage levels as required by each SoC. When the voltage levels may not be shared, additional converters have to be implemented with the necessary passive devices. Moreover a lot of IOs[3] are sacrificed in the SoC package to accommodate the voltage grid. This is described in Fig. 1.3. There is an antagonism between the growth of a SoC set of functions and the available number of IOs as more functions call for more voltage levels and more dedicated IOs. There is clearly a limit to this power supply approach.

A change of paradigm is explored with the idea to disseminate part of the energy converters inside the SoC with only a limited number of external power supply lines. Ultimately one can think to install only one main board converter of the battery voltage to deliver one fixed input voltage to SoCs. The required voltage levels for

[2]System on chip
[3]Inputs-outputs

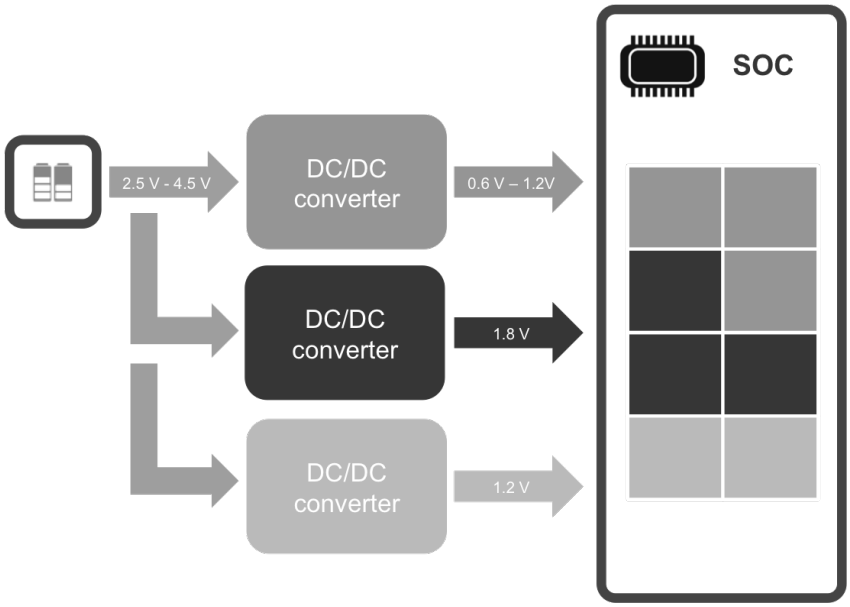


Figure 1.3: Schematic of power solution at board level of the system in Fig. 1.2

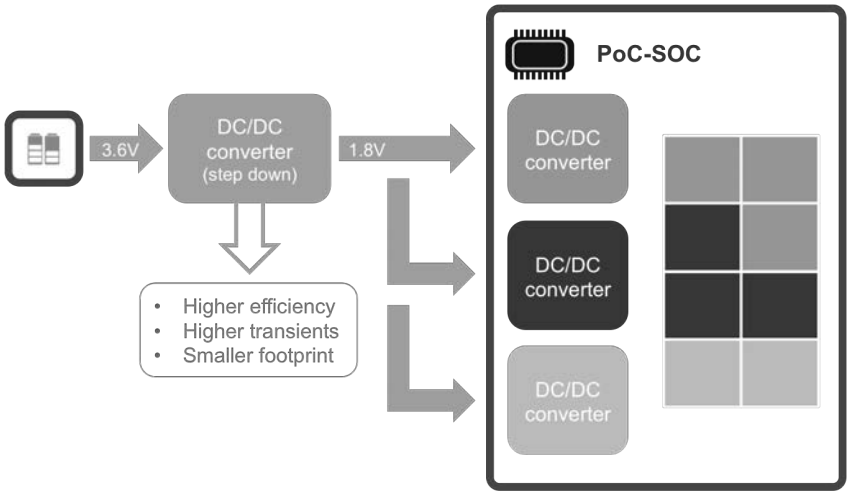


Figure 1.4: A change of paradigm in power supply of a SoC.

the various macro blocks inside the SoC would be embedded along with the macro blocks. This situation is illustrated in Fig. 1.4. The board converter is exposed to severe constraints for example in term of load transient. The embedded voltage converters are supposed to benefit from a very stable input voltage. Embedding a large number of voltage converters is challenging in terms of silicon area and efficiency.

Present work addresses a solution of embedded voltage converters with a high integration level but a limited silicon area penalty at the largest possible efficiency. The

switched-capacitor DC-DC converter has been selected and the manuscript wishes to demonstrate an industrial vehicle in 28nm FDSOI[4] technology.

- Chapter 2 reviews the published techniques of power management of blocks in a SoC. The switched-capacitor converter is compared to inductive SMPS[5] to highlight its main advantages. The chapter ends with a list of specifications for the solution to be demonstrated.
- Chapter 3 details the fundamentals of SC[6] converter. A modeling approach is introduced and various models are constructed. The losses mechanism is presented to optimize the efficiency of the converter. Then the regulation principle is depicted as well as various control strategies.
- Chapter 4 exposes the implementation of frequency modulation control with linear and non-linear schemes.
- Chapter 5 presents the proposed power stage and the design in 28nm FD-SOI process. A test-chip is then characterized and measurement results are successfully compared to simulation ones. A feedback loop scheme is then implemented to complete a final demonstrator attached to an emulator of a digital macro block. A test-chip is designed in the 28nm FDSOI technology and measured in steady-state and transient conditions.
- Chapter 6 details the application of a SC converter to the specific assistance in 28nm FDSOI so-called *body biasing*. The interest is in the negative voltage level.
- Conclusion and perspectives are given in chapter 7.

[4]Fully depleted silicon on insulator
[5]Switch-mode power supply
[6]Switched-capacitor

CHAPTER 2

Literature review

2.1 Sources of power consumption

The power consumption of a digital circuit comes from two fundamental contributions: the static power consumption and the dynamic power consumption [1]. Hardware functionalities in modern digital CMOS ICs[1] are implemented with a lot of digital gates. CMOS logic gates are made of MOSFET[2] transistors and the gates of the transistors are charged or discharged when a transition occurs. The rate of the transition is determined by the operating frequency and a high frequency yields a fast execution. Fig. 2.1 depicts the switching behavior of a simple inverter. When

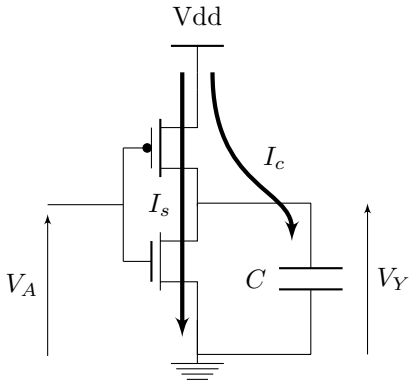


Figure 2.1: Switching behavior of a simple inverter

the input of the inverter falls to 0 V, the PMOS transistor is turned on and the NMOS is turned off. This causes the output to rise to V_{dd}. The current that charges the output node is denoted I_c. The average value of this current depends on the

[1] Integrated circuits
[2] Metal oxide semiconductor field effect transistor

capacitor at the output node, C, the value of V_{dd} and the switching frequency, f. Considering the charge of the capacitor, the power consumption, P_c, and the energy consumption, E_c, normalized over a switching cycle are:

$$P_c = C \cdot V_{dd}^2 \cdot f \tag{2.1}$$

$$E_c = C \cdot V_{dd}^2 \tag{2.2}$$

The power depends on the digital clock frequency while the energy does not. Autonomy of battery powered systems is determined by the energy losses and the thermal aspects.
The energy required for a number of cycle, n, is sometimes introduced as follows:

$$E = n \cdot C \cdot V_{dd}^2 \tag{2.3}$$

An efficient digital design must perform an instruction set with the lowest value of n.
In addition to the consumption induced by the charge of capacitive nodes, a rush current occurs at each transition because NMOS and PMOS are both conducting during a small lapse of time. This is the so-called shoot-through current, denoted I_s in Fig. 2.1. The energy dissipated during the transition is written in a first approximation as:

$$E_t = t_s \cdot I_s \cdot V_{dd} \tag{2.4}$$

Where t_s is the duration of the short circuit and I_s its value. The total dynamic power consumption is obtained by:

$$P_{dynamic} = P_c + E_t \cdot f \tag{2.5}$$

The static power dissipation is considered when the logic state does not change. This consumption is the result of the leakage currents in the MOS transistors. The total leakage current includes the sub-threshold current, the gate leakage current and the junction leakage current in the transistor. The sub-threshold current is written in a first approximation as follows:

$$I_{sub} = \mu C_{ox} \frac{W}{L} V_{th}^2 \exp\left(\frac{V_{dd} - V_t}{n\, V_{th}}\right) \tag{2.6}$$

where W is the width of the transistor, L its length, μ the mobility, C_{ox} the oxide capacitance, V_t the threshold voltage, $V_{th} = \frac{kT}{q}$ and n is a technology factor. The static power consumption can be written as:

$$P_{static} = I_{static} \cdot V_{dd} \tag{2.7}$$

Where I_{static} is the sum of the leakage currents like the one in (2.6).
Finally the total power consumption, P, is a function of the dynamic and the static power consumptions:

$$P = P_{static} + P_{dynamic} \tag{2.8}$$

2.2 Power vs performance

Designers are concerned by the performances as well as the power consumption. However simultaneous improvements of both aspects is quite complicated. The dynamic power consumption is reduced when the power supply and the clock frequency are reduced as shown by (2.1) and (2.4). However the on-current of the MOS transistor is also reduced (2.9):

$$I_{DS} = \mu C_{ox} \frac{W}{L} \frac{(V_{GS} - V_t)^2}{2} \tag{2.9}$$

where W is the width of the transistor, L its length, μ the mobility, C_{ox} the oxide capacitance, V_t the threshold voltage and V_{GS} is the gate-source voltage depending on the voltage supply. Reduction of the threshold voltage increases the current of the transistor resulting in a higher speed but static power is increased too. Generally the sub-threshold current increases with on-current as described by (2.6) and (2.9).
Energy-delay product has been introduced to provide a good metric of the improvement of speed and consumption [2]. Power-delay product is less used due to the clock frequency dependency. Reducing the clock frequency reduces the power consumption but the digital circuit is not better. This figure of merit can be used to compare technology and architecture and demonstrates the best improvements.

2.3 The technology scaling

Scaling the technology is profitable regarding performance and integration. That is the reason why high performance digital circuits are usually fabricated in the most advanced nodes. Two opposing approaches of scaling exist: constant field scaling and constant voltage scaling [3]. Constant field scaling preserves the electrical field in the transistor while its dimensions are scaled down. The power-delay product is reduced but the power supply must be scaled down as well. Constant voltage scaling is preferred to keep compatibility of the voltage between each generation. The dimensions are scaled down too but the doping densities are increased to preserve the transistor performances. The electrical fields increase leading to the

well-known short channel effect (velocity saturation, hot carrier, mobility degradation,...). Leakage current and power density are also increased. New processing techniques that disrupt the traditional approaches have been introduced. Gate stack using high-k dielectric has been developed to improve the leakage current. Silicon-on-insulator substrate offers also a better efficiency and performance trade-offs than the bulk counter part. SOI[3] technology provides lower parasitic capacitances as well as latch-up immunity due to the buried oxide isolation.
Technological aspects are essential to propose both high performance and low power digital circuits. However the rapid growth of the number of functionalities provided by SoCs has called for low power design methodology. These low power techniques are detailed in next Section.

2.4 Low power techniques

2.4.1 Design for energy efficiency

Smart and power-oriented architectures have emerged to make more energy efficient SoCs. Clock gating technique has been firstly introduced during the design phase to save part of dynamic power consumption. A large amount of power is indeed consumed by the clock tree and the clock can be turned off when it is not required [1]. This is performed during RTL[4] coding in the design flow of digital blocks. Libraries with multiple threshold devices are also available in advanced technology platforms. Synthesis tools are able to choose a low-threshold voltage device when the performance is critical and a high-threshold voltage device when it is not compromising [4, 5]. The overall leakage current is therefore reduced. Similar approaches use poly-biasing to modulate the gate length of the transistor to optimize the static power consumption [6, 7]. Optimal architecture choice can result in considerable power savings. A SoC usually comprises a processing core. Many functionalities are then implemented with software approaches. The best way to achieve performances and power optimization is to introduce dedicated IP[5] blocks to replace the software functionalities at the cost of area penalty. These hardware accelerators are widely used in multimedia mobile applications [8]. Pipelining is also an efficient feature that improves the energy-delay product [2].
ARM, a microprocessor design company, goes further with heterogeneous processing architecture. This is the so-called Big.LITTLE technology [9]. Two types of processor are co-integrated: one is optimized for high computing performances and the other one is designed for power efficiency. The tasks are dynamically allocated

[3]Silicon on insulator
[4]Register transfer language
[5]Intellectual property

to the proper processor depending on the performance requirement. This is particularly interesting to address the need for a wide range of performances in mobile devices.

2.4.2 Power gating

Power gating is a technique that turns-off unused digital blocks to save static power consumption. Power switches are implemented to cut-off the power supply of a block. A header PMOS power switch is used when Vdd path is cut-off while a footer NMOS power switch is required to cut-off the ground path [10]. Header switch configuration is usually preferred in SoC design because ground is common. The gated blocks are isolated from the powered blocks with a simple pull-down transistor that clamps signals to ground. There are two options for the architecture level implementation: the ring or the distributed approach. Fig. 2.2 depicts the ring implementation. The power switches are inserted around the power-gated blocks.This is thus a suitable option for existing IP blocks. However significant IR-drop can occur in the center of the domain. This voltage drop degrades the block performances. The grid configuration shown in Fig. 2.3 can address this issue. The power switches are distributed through the domain close or inside the standard cells to minimize the IR-drops [11]. Unfortunately this requires dedicated standard cell libraries or a specific synthesis flow. As a consequence, the grid configuration has to be included during the design architecture phase and cannot be applied to existing blocks. Furthermore, the distributed approach is more area efficient than the ring approach.

The design of the devices in power gating approach is essential. The I_{on}/I_{off} ratio is used to evaluate the efficiency of a switch. A good switch is therefore a switch with a low leakage current and a high on-state current (low resistance). The area overhead is also an important metric in SoC design. Literature has covered several improvements of the power switch. Body effect can be used to decrease the leakage current [12]. Dynamic threshold tunning is also offered in SOI process to improve the leakage current [13]. Super-cut-off scheme is used for low voltage supply system [14]. The control voltage of the PMOS switch is raised above the supply voltage in order to reduce the leakage current.

Latency and power integrity are also critical aspects in power gating design. The power supply has to be turned off as often as possible to achieve the lowest static dissipation with fast wake-up and small sleep-time to not alter block operation. Unfortunately the turning-on of the power switches causes a large inrush current. The power supply collapses and the operation of the neighbor blocks is disturbed. The power switches are then progressively turned-on in order to limit the current

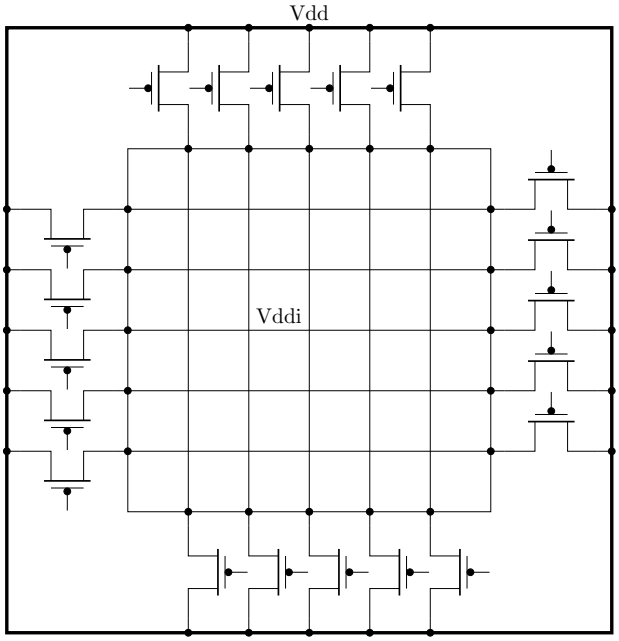


Figure 2.2: Ring implementation of power gating

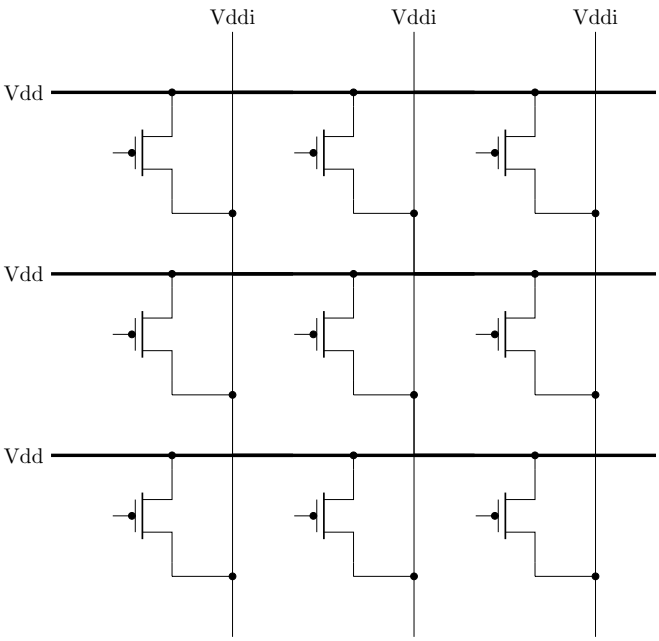


Figure 2.3: Grid configuration of power gating

surge [15]. A technique using two power line distribution network is proposed in [16]. The inrush current is reduced and the wake-up time is improved but at the cost of a complex power grid.
Power gating in the most effective method to reduce the static power dissipation during standby mode of digital blocks. That is the reason why this technique is widely used in low power systems.

2.4.3 Voltage scaling

Voltage scaling is certainly the most aggressive power reduction technique. The dynamic power and the static power drastically scale with the supply voltage. Unfortunately the reduction of power supply is correlated to the operating frequency. The supply voltage is indeed determined by the critical timing path. When considering a single voltage supply, the highest voltage must be applied to the whole circuit to meet the performance constraints. However some IPs or blocks may run at lower voltage at the same time. Voltage scaling allows to partition the SoC into different voltage domains to optimize performance objectives. The major implementations are static voltage scaling, multi-voltage scaling, dynamic and adaptive voltage scaling.

Static Voltage Scaling This is the simplest approach of voltage scaling. The SoC is partitioned into a small number of power domains powered by a fixed voltage supply [17]. An example is given in Fig. 2.4. The most demanding blocks require the maximum voltage sustained by the technology. The other IP blocks can work at a lower voltage supply and lower frequency. The number of power domains can be increased to save more power but the power grid becomes more complex. It is also limited by the number of off-chip regulators.

Multi-Voltage Scaling This extension of the static voltage scaling offers supply voltages to vary with discrete values. This is so-called Vdd-hopping or Vdd-dithering in literature. Strategy with two supply voltages demonstrates good results [18] and is applied to a multi-processor chip in [19]. The concept is depicted in Fig. 2.5. The voltage levels are generated off-chip and selected by a controller with a power line multiplexer. Two operating frequencies are also associated with the operating voltage. The number of external power supplies can be maintained as low as with the static voltage scaling. An area overhead of 12% but an improvement by 48% in energy consumption is reported in [19]. Application of multi-voltage scaling has been applied to SRAM[6] in low power SoCs. Memory arrays can be large

[6]Static random access memory

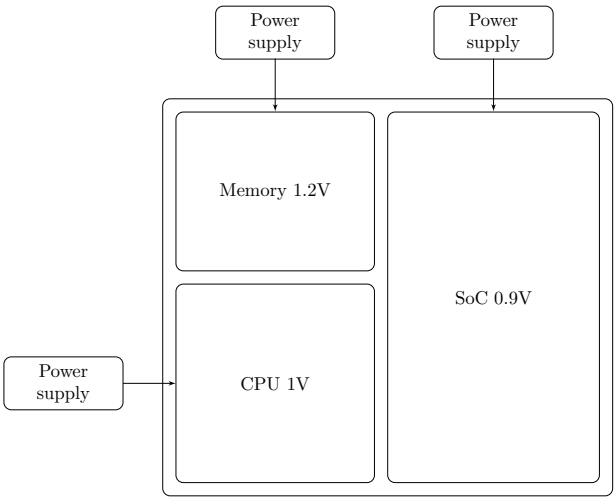


Figure 2.4: Example of multi-voltage power domain

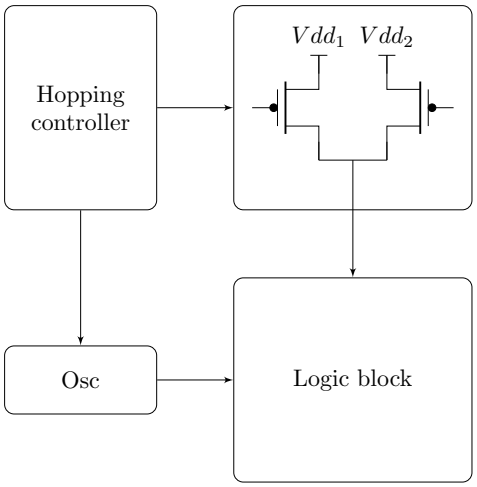


Figure 2.5: Illustration of Vdd-hopping

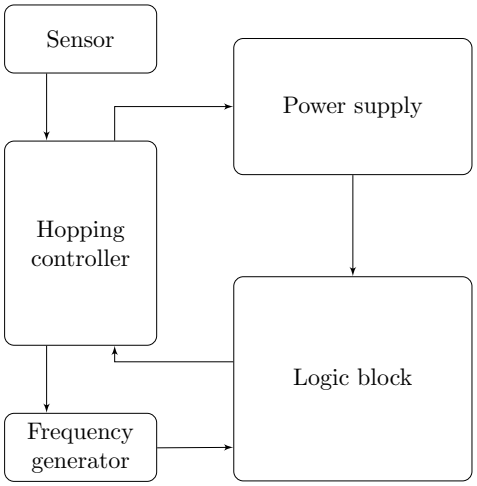


Figure 2.6: Illustration of AVFS strategy

for some applications leading to a significant leakage current. The power supply of non-used bit-cell arrays can be put in standby mode. The standby mode is a retention state where the power supply is as low as possible to both reduce the leakage current and keep data. The technique has been extended to active mode as well [20]. Memory blocks are kept in retention state until an access request. The power supply is restored during the read/write operation and then returns to the retention state. This technique known as retention-till-access is very efficient but the memory latency is increased.

Dynamic & Adaptive Voltage Scaling This solution is introduced when more than few voltage levels are required. Operating points are defined as voltage and frequency pairs. The operating points are changed on the fly accordingly to the workload. The voltage domain with dynamic voltage scaling necessitates a dedicated voltage regulator and level-shifters to interact with other domains. The operating point is selected by a controller and in the adaptive voltage scaling a closed-loop scheme is implemented to determine the operating point over process and temperature variations. Process and temperature monitorings are generally used. A diagram of AVFS is depicted in Fig. 2.6. The voltage regulators must exhibit enough bandwidth and reactivity to allow fast transitions between the operating points. Otherwise excess power is wasted during ramping time. The efficiency of the converter is also essential to achieve a high gain in power losses. These techniques are attractive but they are highly limited by the number of external regulators and only some blocks such as CPU and GPU can be properly addressed.

2.4.4 Body-biasing

Body-biasing uses the body effect of the transistor to adjust the threshold voltage. The body of the transistor is often called the back-gate. The back-gates of an inverter are represented in Fig. 2.7. No body-biasing scheme is applied when V_{bbp} and V_{bbn} are respectively equal to vdd and gnd. Otherwise two cases are considered: the reverse body-biasing (RBB) and the forward body-biasing (FBB).

- RBB: $V_{bbp} > vdd$ and $V_{bbn} < gnd$. The threshold voltage is increased. This decreases the current capability of the transistor and the leakage current as well. The speed performances are reduced and this configuration is mostly applied to low power mode such as standby mode.

- FBB: $V_{bbp} < vdd$ and $V_{bbn} > gnd$. The threshold voltage is lowered. The transistor current increases what speeds-up the device. The leakage current is

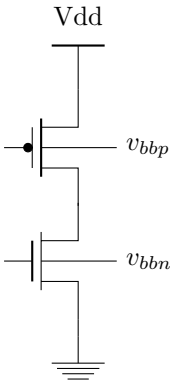


Figure 2.7: Body-biasing of PMOS and NMOS transistors

also increased. FBB is used to boost the performances of digital functionalities at the cost of a power consumption penalty.

Body-biasing is also used to compensate process variations or temperature deviation in digital circuits [21–23]. This is the so-called adaptive body-biasing. On-die process monitoring is required to determine the proper biasing scheme. This is particularly interesting for sensitive design such as ultra-low voltage circuits.

2.5 Power delivery

The objective of a power delivery network is to dispatch the voltage supply from the energy sources to the consumers in the most efficient and cleanest manner. Performances of a power delivery network depends on the design of the PCB[7], the packaging technology of the circuit and the power management strategy. A classical power delivery is represented in Fig. 2.8. The primary source of energy is a battery. The voltage level is adapted by the voltage regulator module located on the board. The regulated voltage is then routed to the on-die load through the board tracks, the balls or the pins of the package and the on-die power grid. Each elements and discontinuity in the power delsivery network introduce parasitic effects. The parasitic effects are responsible for voltage fluctuation within the power delivery network. These effects are mitigated by a proper package, board and decoupling strategy. It involves the analysis of the power delivery performances. Power delivery network can be modeled with lumped RLC network [24, 25]. Power grids and connections are represented with RL networks such C4[8] bumps, package balls, etc. Decoupling capacitors are modeled with the equivalent series-resistance and series-inductance with RLC network. The performances of the power delivery network are evaluated

[7]Printed circuit board
[8]Controlled collapse chip connection

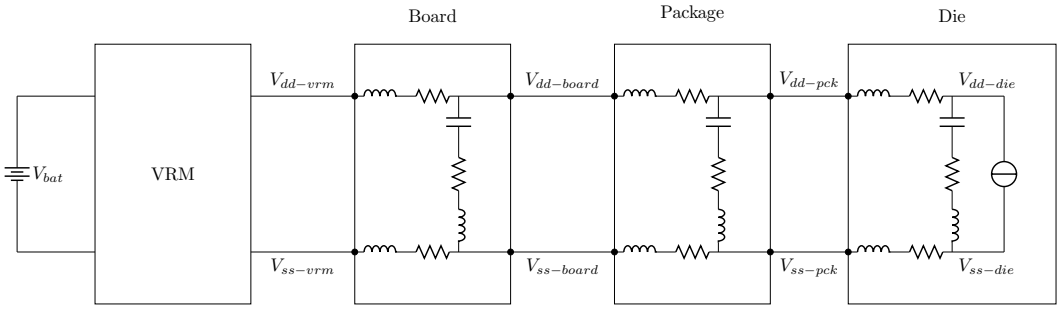


Figure 2.8: Power delivery network representation

by extracting the impedance of the power net [26, 27]. Objectives are defined for each element to meet the performance constraint and the targeted impedance :

$$Z_{target} = \frac{V_{supply} \cdot \Delta V_{\%}}{I_{max}} \tag{2.10}$$

Where V_{supply} is the voltage level needed for the application, $\Delta V_{\%}$ is the maximum allowed voltage fluctuation in percent and I_{max} is the maximum transient current surge. The first elements that respond to the current surge are on-die and on-package decoupling capacitors. Then comes the board decoupling capacitors and finally, the voltage regulators. Several types of capacitor are combined to optimize the frequency response as much as possible.

The packaging technology has a strong impact on the power delivery network and on the power management strategy. Even more IOs are required to meet power density and memory requirements [28]. Integration remains the biggest challenge. Packaging solution is determinant to achieve both high performance and energy efficient SoC. Fig. 2.9 shows the competitive edge of Samsung in packaging technology. Flip-chip assembly with BGA[9] package is one of the technique that provides the highest number of IO resources. Nonetheless 3D structures have emerged to increase the integration level but the complexity is prohibitive for low-cost solutions.

2.6 Power supply

Nowadays, digital SoC for mobile applications always include a power management companion chip. The power management circuit has several goals. First, the battery cannot maintain a constant voltage during the whole operating time. The voltage of a battery also depends on the technology uses for the electrochemical cell. Moreover many voltages level are required for multi voltage strategy. Therefore some

[9]Ball grid array

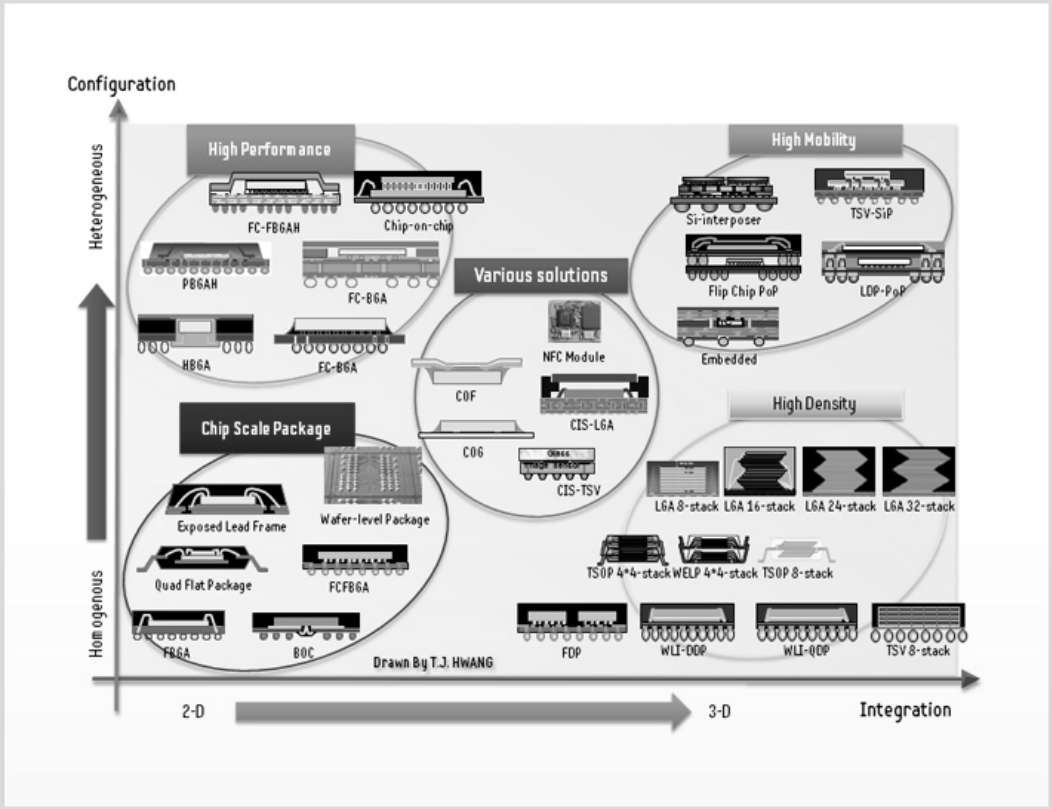


Figure 2.9: Samsung's competitive edge in packaging technology [29]

voltage regulators are mandatory to fulfill the voltage level standards. Then a gas gauge monitors the battery energy level to indicate the remaining time of use. A battery charger is also used to put energy in the battery from a mains adapter. The companion chip has finally a communication bus to receive the request of voltage change and so on.

Various voltage regulators are available in the companion chip. Linear regulators and inductive DC-DC converters are often associated to address wide range of needs [30–33]. A PMOS LDO[10] is depicted in Fig. 2.10. It comprises a pass transistor and a feedback amplifier. The gate voltage of the pass transistor is controlled by the amplifier in such a way that the pass transistor operates in the active region. When the output current is increased by the load consumption the output voltage decreases. The difference of the output voltage and the reference voltage increases and the amplifier decreases the gate voltage to reduce the difference at its inputs. More current is injected and the output voltage raises. Analog operation happens when the load current decreases. The dynamics of LDO depends on the output capacitor and the bandwidth of the amplifier. PMOS LDO presents strong

[10]Low drop-out

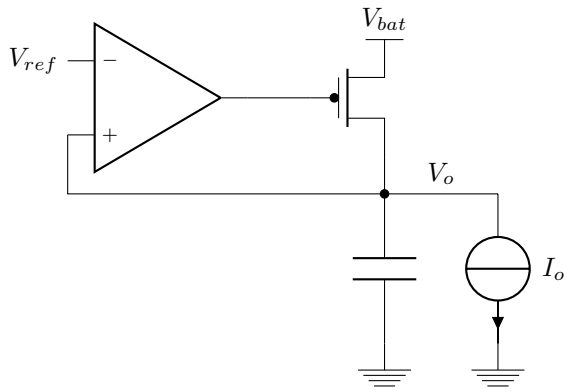


Figure 2.10: Diagram of a classical PMOS LDO

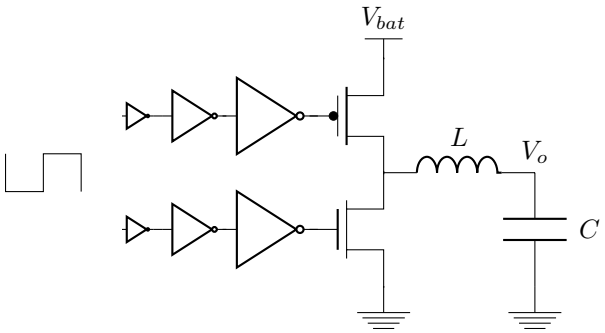


Figure 2.11: Diagram of an inductive DC-DC converter

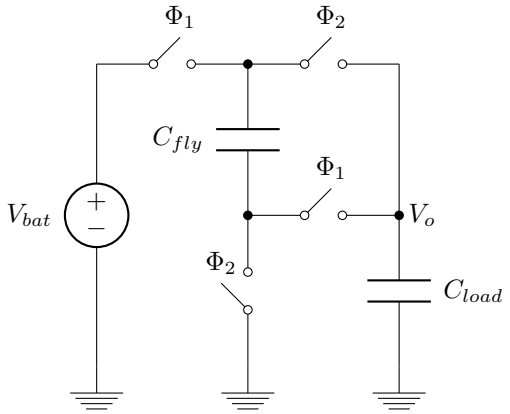


Figure 2.12: Diagram of a capacitive DC-DC converter

disturbance rejection capability making them popular for analog and RF[11] system power supply. Nonetheless, the usage of linear regulators is restricted to low and medium power because of the efficiency:

$$\eta_{LDO} = \frac{V_{in} I_{out}}{V_{out} \left(I_{out} + I_q \right)} \tag{2.11}$$

The quiescent current, I_q, is relatively low and can be neglected if I_{out} is high, generally true when LDO is regulating. Hence the efficiency depends on the output voltage to input voltage ratio. Poor efficiency is therefore achieved for large drop-out and this is not suitable for high power load.
Inductive DC-DC converter are preferred to supply large power load. A step-down converter is shown in Fig. 2.11. The battery voltage and the ground are alternatively fed to the inductance by the power switch bridge. The voltage of the bridge is filtered across a low pass LC filter. Energy is stored into the inductor during one phase and restored during the other one. The efficiency is ideally 100% but the parasitic losses including resistive losses and switching losses reduce the efficiency at the nominal load conditions. Special modes such as the discontinuous conduction mode are implemented to improve the efficiency at light load. The output voltage is controlled by the duty-cycle of the switching action. On the contrary to linear regulator they offer step-up and inverting capabilities instead of step-down only. Display requires for instance bipolar supply of $\pm 5V$ while the battery voltage can be 3.6 V in lithium-ion technology. Audio devices also need bipolar supply. The downside of inductive DC-DC converter are the cost due to the external components (inductor and capacitor). Capacitive DC-DC converter (Fig. 2.12) are sometimes used in audio power management but they are still little used in power management platform. Capacitive regulators are detailed in Chapter 3.

2.7 Challenges in advanced SoC power management

Reduction in the power consumption in advanced SoC is challenging. Power management techniques have significantly changed the design of SoCs. The most promising strategy is massive DVFS to deliver power according to performance requirements. DVFS is widely used for the most demanding blocks in a SoC such as CPU but cannot be further extended to other blocks for various reasons. Traditional architectures are based on off-chip power supplies. Each domain is independently powered by a voltage regulator with low impedance connection. Increasing the number of power domains will increase the number of regulators and increase the board area. It becomes difficult to optimize routing on constrained board. The power

[11] Radio frequency

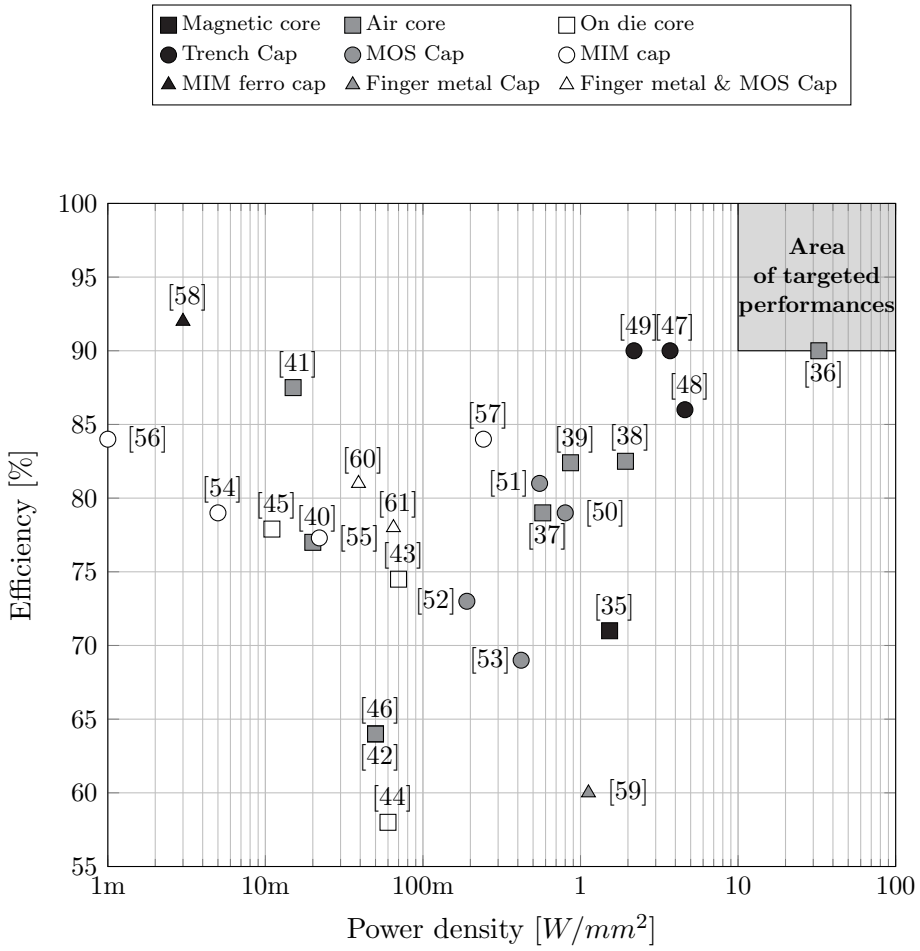


Figure 2.13: Peak efficiency vs power density of recent published integrated inductive and capacitive DC-DC

delivery network is also impacted. The resources required for the power supply rails in the package and in the die are limited and have to be shared. This causes impedance degradation of the PDN. The performances and current consumption of SoCs continue to increase while the voltage tend to decrease to mitigate the power consumption. The impedance of the PDN[12] must decrease as well to keep the same performances [34]. Moreover complex power delivery and bus speed limit the timing transition between different operating points.

Recent advances in magnetics [62] and packaging technologies offer new platforms with high integration level. Power supply manufacturers integrate passive devices on the die (homogeneous architectures) or using SiP[13] (heterogeneous architectures). A comparative analysis of commercial PMICs[14] published in 2010 is

[12]Power delivery network
[13]System in package
[14]Power management integrated circuits

presented in [63]. Relative sizes of inductors tend to decrease while the switching frequency of the DC-DC converters increases. Since the switching losses increase, a lot of efforts are made to improve or maintain high efficiency. TPS8267 series by Texas Instrument are examples of commercial product where a 600 mA step-down DC-DC is integrated along with the inductor and input/output capacitors. A maximum efficiency of 90% is reported as well as a quiescent current of 17 μA during PFM[15] operation. Those PMICs significantly reduce the BOM[16] and board area.
Fully or partially integrated voltage regulation appears as a suitable approach to increase DVFS usage. A recent growth of literature demonstrates the interest of such methods [64–68]. The linear voltage regulator is certainly the simplest approach since no passive devices are required. Such an approach is presented in [66, 68] and a practical implementation for the POWER8 microprocessor is demonstrated in [69]. The comparator-based voltage regulator allows fast transition with a maximum efficiency of 90%. Efficiency decreases at low voltage but is still sufficient to enhance power consumption saving. A power density of 34.5 $^{W}/_{mm^2}$ is reported that is appropriate for server-class microprocessor. Per-core voltage generation is interesting in these systems in terms of cost and area but thermal limitations and efficiency can only be improved by switching voltage regulators. 3D integration through stacking voltage regulator die above the IC is a possibility [70] but semiconductor manufacturers have also developed and integrated magnetic devices and high density capacitors in their process to enable inductive and capacitive voltage regulation on the die. Efficiency versus power density is one of the most frequently used performance metric to compare DC-DC converters. Other figures of merit offer the possibility for a more detailed analysis [71–73]. A landscape of the most recent and relevant works on integrated conversion is depicted in Fig. 2.13. The challenge is to achieve both high efficiency and high power density at an acceptable cost or in a manner compatible with the synthesis of the circuit to be powered. The usual common value for the SoC power density is 1 $^{W}/_{mm^2}$ but a small silicon area penalty would require in fact a density of 10 $^{W}/_{mm^2}$ for the DC-DC converter. The quality of the passive devices is essential. As expected the highest performances are achieved by Intel Haswell architecture with non-magnetic core inductance but the technology is unaffordable for many applications [36]. Some DC-DC converters using air core inductors on package exhibit acceptable efficiency near 1 $^{W}/_{mm^2}$ [37–42] while those using on-die air core inductors still suffer from lower power density [43–46]. Switched-capacitor (SC) converters demonstrate a high efficiency at a density mainly limited by the density of the capacitors [50–55, 58–60, 74]. The limit in power density featured in [59] clearly calls for high density capacitors. Deep trench capacitors have been

[15] Pulse frequency modulation
[16] Bill of material

introduced and enable a peak efficiency of $85-90\%$ up to 1 $^{W}/_{mm^2}$ [47–49]. Architectures distributed across digital core also bring a relevant point [57]. The flying capacitors are distributed over the digital core and the area penalty is limited to the one of the power switches and the controller. Generally SC converters present the best trade-off for low-cost monolithic integrated solution and they are more and more investigated [73]. Resonant SC converters or cascaded SC converters with inductive converters are also explored to take advantages of both capacitors and inductors. Resonant SC converters use an inductor in series with the flying capacitor to produce a resonant energy transfer [75,76]. Efficiency can be improved for a given power density but inductors remain costly. SC converters cascaded with inductive converters seems promising [77]. An unregulated SC converter is used to convert the high input voltage to a lower one. Then an inductive converter achieves a fine regulation. This combination allows large voltage step-down and high bandwidth regulation.

2.8 Proposed architecture

Earlier was mentioned the monitoring of voltage through power switches connected between the digital block unique power lines and a quite complex power grid. The silicon area of the power switches is in the range of 3% to 10% of the digital block area. The power grid consumes as much IOs as voltage levels. The change of paradigm proposed here is to limit the IO consumption to one input voltage level (due to IR-drop more than one IO will be needed). The area dedicated to the power switches in a conventional approach will be diverted to implement a full voltage converter. For the sake of integration, the SC converter is the suitable candidate. Fig. 2.14 illustrates the targeted implementation. The converter silicon area should be restricted to the reasonable value of 10% of the one of the digital block. It is obvious that capacitors cannot fit a so constrained area. An economic and none complex solution is to consider MIM[17] capacitors to be located above the digital core. Referring to Fig. 2.14 it is expected the following performances:

- Peak efficiency will be over 75% for a targeted power density of 1 $^{W}/_{mm^2}$
- The digital core design flow should not be affected by the SC converter implementation.
- The transient performances should be sufficient to afford a DVFS application.

[17] Metal insulator metal

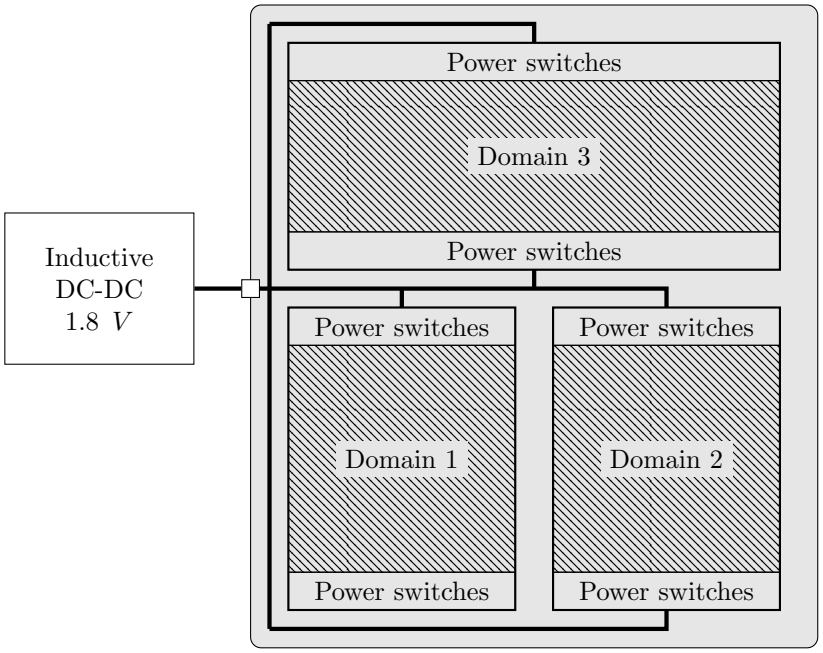


Figure 2.14: Paradigm

- The stability of the SC converter must be assessed by a suitable analytical approach.

Obviously the pointed target area in Fig. 2.14 cannot be reached. The objective of the demonstrator is then to join the best-in-class literature results based on MIM capacitors. The idea is to provide better performances and systematic design approach at a similar cost. A demonstrator in FDSOI 28nm will add a relevant and original point in the landscape in 2.13.

CHAPTER 3

Fundamentals of Switched-capacitor converter

The chapter summarizes the behavior of a SC converter, evaluation of losses and modeling of dynamics toward control design.

3.1 Principles

SC converters are a part of switched-mode converters. They are built only with capacitors and switches. Flying capacitors are charged and discharged between the input and output nodes during operation. The configuration of both switches and

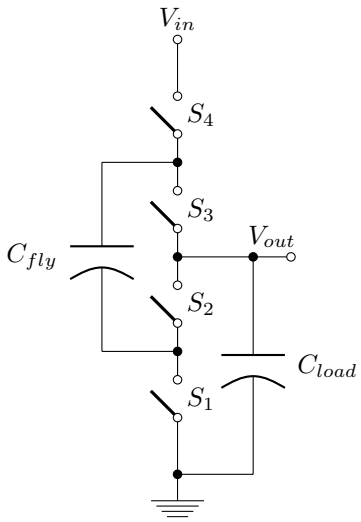


Figure 3.1: SC converter

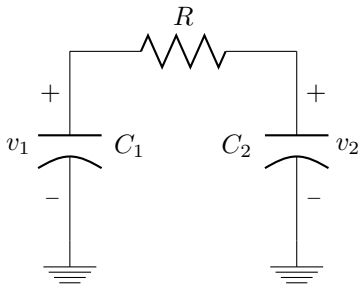


Figure 3.2: Charge transfer illustration

capacitors forms a topology which defines the discrete converter ratio. An example of a 2:1 step down SC converter is given in Fig. 3.1. The switches S_2 and S_4 are turned on in a first phase while S_1 and S_3 are off. The flying capacitor, C_{fly}, is charged between the input voltage, V_{in}, and the output voltage, V_{out}. Then, in a second phase S_2 and S_4 are off and S_1 and S_3 are turned on. The flying capacitor is connected between the ground and the output voltage. The first phase is a charging phase while the second one is the discharging phase with respect to the flying capacitor. When the output voltage and the input voltage are swapped the converter becomes a step-up structure, doubling the voltage.

The theoretical efficiency of inductive DC-DC converters reaches 100%. This not the case of SC DC-DC converters. The conversion mechanism based on the charge transfer between the capacitors is unfortunately lossy. Explanations are given in Fig. 3.2. The capacitors C_1 and C_2 are initially charged at v_1 and v_2 respectively. The total available energy is:

$$E_1 = \frac{1}{2}\left(C_1 v_1^2 + C_2 v_2^2\right) \tag{3.1}$$

Then these capacitors are connected in parallel though a resistance R. The charges are redistributed and the voltage across each capacitor equilibrates at a voltage v_3:

$$v_3 = \frac{C_1 v_1 + C_2 v_2}{C_1 + C_2} \tag{3.2}$$

The energy available is now:

$$E_2 = \frac{C_1 + C_2}{2} v_3 \tag{3.3}$$

$$= \frac{\left(C_1 v_1 + C_2 v_2\right)^2}{2\left(C_1 + C_2\right)} \tag{3.4}$$

The difference between the initial energy, E_1 and the final energy, E_2, is the energy lost by the system:

$$E_{loss} = \frac{C_1 C_2}{2\left(C_1 + C_2\right)}\left(v_1 - v_2\right)^2 \tag{3.5}$$

The system has less energy than in initial state. This energy is dissipated in the resistance but does not depend on its value.
The 2:1 SC converter will be used for illustration purpose throughout the chapter. The various parameters of this converter are gathered in Table 3.1. The nominal input voltage is V_{in}, the nominal load current is I_{load}, the flying capacitor is C_{fly}, the output capacitor is C_{load}, the on-state resistance of the switches, R_{on}, is identical for each switch and the duty-cycle of the charging topology is DC.

Parameter	V_{in}	C_{fly}	R_{on}	C_{load}	I_{load}	DC
Value	$2\ V$	$200\ pF$	$10\ \Omega$	$10\ nF$	$5\ mA$	$50\ \%$

Table 3.1: Parameter of the 2:1 SC converter considered as an illustration vehicle

3.2 Modeling

Various methods are proposed in literature. Historically SC filters have been explored first. The time-domain and frequency-domain analysis are performed with state equation formulation [78] or nodal analyses [79]. Special purpose simulators have been also proposed to easily perform the analysis [80]. SC filters usually operate at a fixed switching frequency and in the slow switching region while SC converters have variable frequency and operate toward the boundary of the fast switching region. The latter regions are explained here after. That is the reason why further analyses have been recently extended to SC converters. The next sections details the most relevant.

3.2.1 Static model

The static model of a SC converter is depicted in Fig. 3.3. The ratio of the topology is represented by an ideal transformer and a turning ratio. An output resistance is inserted to symbolize the voltage drop when the converter is loaded. The method

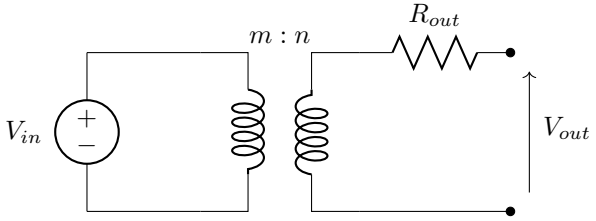


Figure 3.3: SC converter static model representation

developed in [74] provides a powerful framework to determine the ratio and the output resistance of any topology. This method is based on the charge flow analysis. Two operation regions are defined according to the switching frequency: the Slow Switching Limit (SSL) and the Fast Switching Limit (FSL). A charge/discharge time-constant is formed by the on-state switch resistance and the flying capacitors. When the switching period is large compared to this time-constant, the converter operates in the SSL region. On the contrary, when the switching period is small regarding the time-constant, the converter is in the FSL region. The charge balance analysis is used to determine both the output resistance in the SSL and FSL regions. In the SSL region, the switching frequency is low and the flying capacitor is completely charged and discharged in each phase. Thus the resistive effect can be neglected. A set of charge multiplier vector, a^n, is defined to represent the charge flow when the switches are closed for the n phase of the converter.

$$a^n = \begin{bmatrix} -q_{in}^n & q_{c,1}^n & \dots & q_{c,i}^n & q_{out}^n \end{bmatrix} \tag{3.6}$$

where q_{in} is the charge at the input, q_{out} at the output and $q_{c,i}^n$ the charge accumulated in the i-*th* capacitor. The charge multipliers of the capacitors are gathered in a vector a_c^n and the input and output ones in a_{in}^n and a_{out}^n respectively.

$$a^n = \begin{bmatrix} a_{in}^n & a_{c,i}^n & a_{out}^n \end{bmatrix} \tag{3.7}$$

The charge multiplier vectors are normalized with respect to the total charge at the output, q_{out}

$$a^n = \begin{bmatrix} a_{in}^n & a_{c,i}^n & a_{out}^n \end{bmatrix} / q_{out} \tag{3.8}$$

The ratio of the topology is given by the ratio between the total amount of charge at the input and the total amount of charge at the output:

$$\frac{m}{n} = -\frac{q_{in}}{q_{out}} \tag{3.9}$$

The output resistance in SSL is then computed using the results in [74]:

$$R_{SSL} = \sum_{i \in caps} \sum_{j=1}^{n} \frac{\left(a_{c,i}^j\right)^2}{2 \cdot C_i \cdot f_{sw}} \tag{3.10}$$

The charging/discharging phase in not completed in the FSL region and the resistive effects cannot be neglected. Similarly to the SSL analysis, switch charge multipliers, $a_{r,i}^n$ are introduced to represent the charge flowing in the switches i during the phase n.

$$a_r^n = \begin{bmatrix} a_{r,1}^n & \dots & a_{r,i}^n \end{bmatrix} \tag{3.11}$$

The output resistance is derived as follows [74]:

$$R_{FSL} = \sum_{i \in switches} \sum_{j=1}^{n} \frac{R_i}{D_j} \left(a_{r,i}^{j} \right)^2 \tag{3.12}$$

where R_i is the on-state resistance of the i-th switch and D_j the duty-cycle of the phase j. The output resistance in both operating regions have been introduced. However the output resistance must be determined for any switching frequency. The output resistance can be approximated using a combination of the resistance in the two regions:

$$R_{out} \approx \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{3.13}$$

The method is applied to the 2:1 SC converter in Fig. 3.1. The charge multipliers in the SSL region are:

$$a^1 = \begin{bmatrix} -0.5 & 0.5 & 0.5 \end{bmatrix} \tag{3.14}$$

$$a^2 = \begin{bmatrix} 0 & -0.5 & 0.5 \end{bmatrix} \tag{3.15}$$

The value of the ratio is given by (3.9)

$$\frac{m}{n} = -\frac{-0.5}{1} = \frac{1}{2} \tag{3.16}$$

and the output resistance in SSL is

$$R_{SSL} = \frac{0.25}{C_{fly} f_{fsw}} \tag{3.17}$$

Then charge multipliers of the switches are derived in the FSL region:

$$a_r^1 = \begin{bmatrix} 0.5 & 0.5 & 0 & 0 \end{bmatrix} \tag{3.18}$$

$$a_r^2 = \begin{bmatrix} 0 & 0 & -0.5 & -0.5 \end{bmatrix} \tag{3.19}$$

The output resistance in FSL is calculated with a duty-cycle of 50%:

$$R_{FSL} = 2R_{on} \tag{3.20}$$

The output resistance and the two asymptotic limits are evaluated with the parameters in Table 3.1 and the results are plotted in Fig. 3.4. The converter is simulated in the SSL region with a switching frequency of 10 MHz and in the FSL region for a switching frequency of 400 MHz. The current waveforms are plotted in Fig. 3.5a and Fig. 3.6a and the waveforms of voltage across the flying capacitor in Fig. 3.5b and Fig. 3.6b respectively.

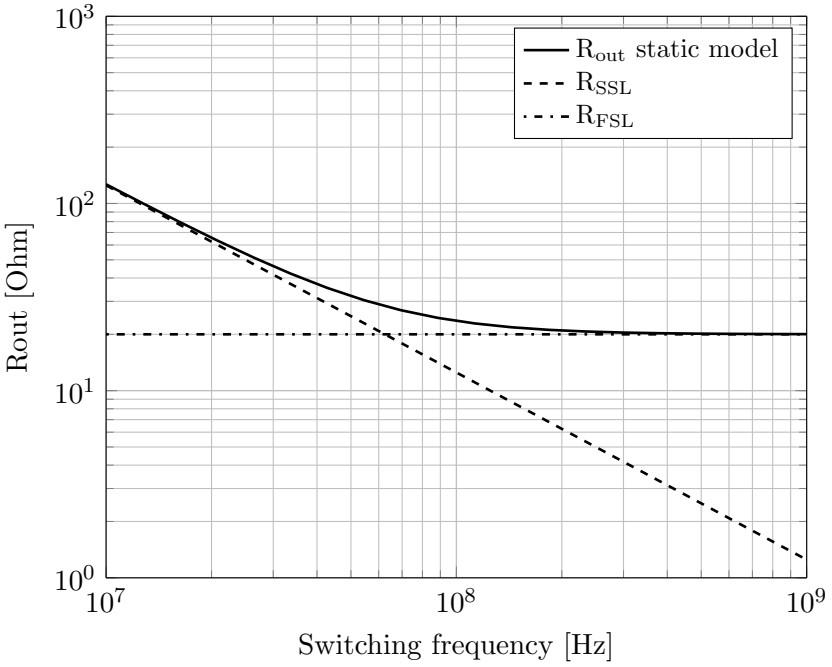
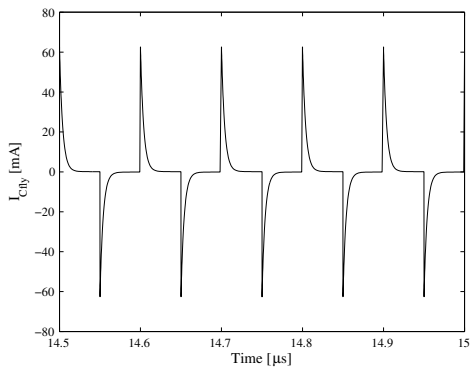
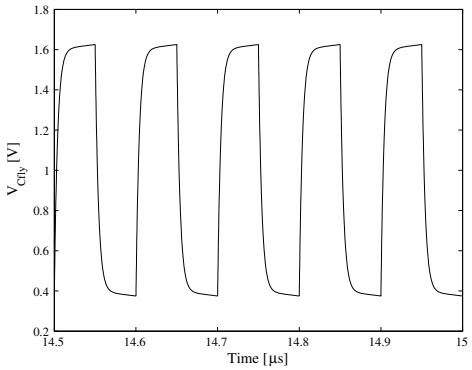


Figure 3.4: Output impedance diagram

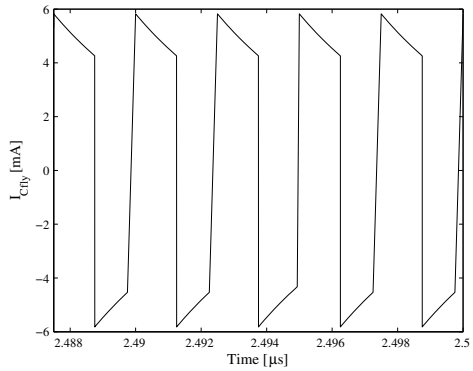


(a) Current in the flying capacitor

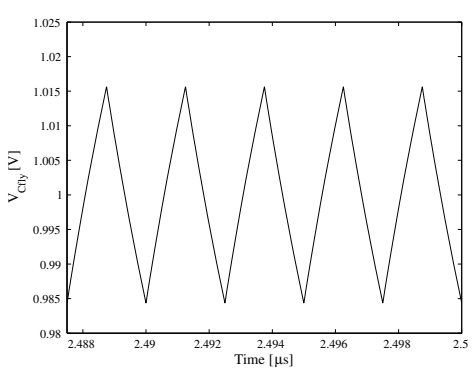


(b) Voltage across the flying capacitor

Figure 3.5: Current and voltage waveforms in the flying capacitor in the SSL region for the converter in Fig. 3.1 ($f_{sw} = 10\ MHz$)



(a) Current in the flying capacitor



(b) Voltage across the flying capacitor

Figure 3.6: Current and voltage waveforms in the flying capacitor in the FSL region for the converter in Fig. 3.1 ($f_{sw} = 400\ MHz$)

3.2.2 Modified static model

The previous model does not take in account the impact of the output capacitor on the output resistance of the converter. The previous model is valid for large output capacitance value but when this value is small regarding the flying capacitors, the model is not accurate [81]. The charges are transfered between the input and the output nodes. The discrete behavior imposes the usage of an output capacitor to maintain the output node during the charging phase. The output capacitor is discharged by the load during operation. Therefore an amount of charge is transfered from the flying capacitors to the output capacitor. As previously explained, charge transfers are lossy and the latter mechanism is no exception. The demonstration in [81] shows that the output resistance in the SSL region can be written with respect to the output capacitor, C_{load} as:

$$R_{SSL} = \sum_{i \in caps} \sum_{j=1}^{n} \frac{C_{load}}{C_{load} + C_i} \cdot \frac{\left(a_{c,i}^{j}\right)^2}{2 \cdot C_i \cdot f_{sw}} \tag{3.21}$$

3.2.3 Non linear averaged model

The previous method is suitable to determine the ratio and the output resistance of a complex topology. However the approximation of the output resistance cannot yield an accurate model. That is the reason why average modeling approaches have been introduced [82]. The charging and discharging phases are represented using RC networks as in Fig. 3.7 where ΔV_i represents the voltage across the switch before it is closed, R_i gathers the resistive effects in the switches and the interconnection parasitics, C_i is the total capacitance and i denotes the corresponding phase. The

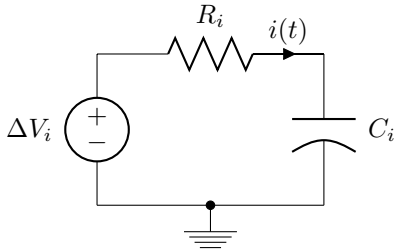


Figure 3.7: Instantaneous representation of the RC network

equivalent resistance, R_{e_i}, is derived using the instantaneous power dissipated in each phase. The power losses can be evaluated as a function of the output current I_o as follows

$$P_{R_i} = k_i^2 \cdot I_o^2 \cdot \frac{1}{2 f_{sw} C_i} \cdot \coth\left(\frac{\beta_i}{2}\right) \tag{3.22}$$

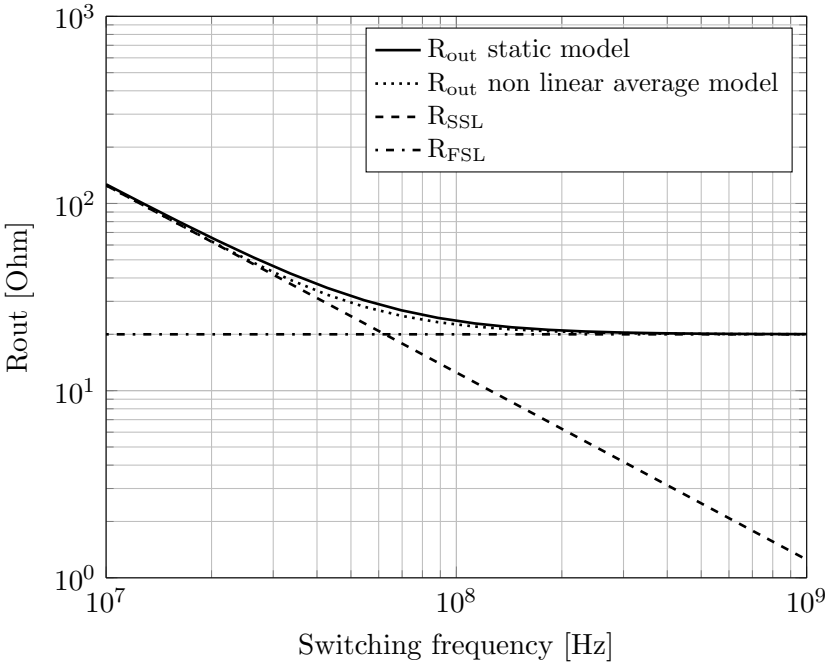


Figure 3.8: Output impedance diagram

where $\beta_i = \dfrac{T_i}{R_i C_i}$, T_i is the duration of the phase i and k_i is a proportional factor corresponding to the charge multiplier of the flying capacitors. The equivalent resistance is

$$R_{e_i} = k_i^2 \cdot \frac{1}{2 f_{sw} C_i} \cdot \coth\left(\frac{\beta_i}{2}\right) \tag{3.23}$$

The whole resistance is simply calculated summing the partial resistance in each phase of operation

$$R_{out} = \sum_{i=1}^{n} R_{e_i} \tag{3.24}$$

This method also offers to derive the equivalent output resistance of resonant converters [82].

The method is applied to the 2:1 SC converter in Fig. 3.1: $k_1 = k_2 = 0.5$ and $\beta_1 = \beta_2 = \dfrac{1}{4 R_{on} C_{fly} f_{sw}}$.

$$R_{e_1} = R_{e_2} = \frac{1}{8 f_{sw} C_{fly}} \cdot \coth\left(\frac{1}{8 R_{on} f_{sw} C_{fly}}\right) \tag{3.25}$$

Finally

$$R_{out} = \frac{1}{4 f_{sw} C_{fly}} \cdot \coth\left(\frac{1}{8 R_{on} f_{sw} C_{fly}}\right) \tag{3.26}$$

The output resistance and the two asymptotic limits are evaluated with the parameters in Table 3.1 and the results are plotted in Fig. 3.8. The average model is more accurate than the static model because the static model relies is an approximation of the resistance in the SSL and FSL region.

3.2.4 Sampled-data modeling

As suggested in [83], the modeling of switched-mode converters is usually specific. Sampled-data modeling has been introduced as a practical and uniform approach. DC-DC converters are variable discrete structures and hybrid automaton is a convenient method for representation and simulation purpose [84, 85]. A cyclic hybrid automaton with N states is represented in Fig. 3.9. The dynamics of a state is

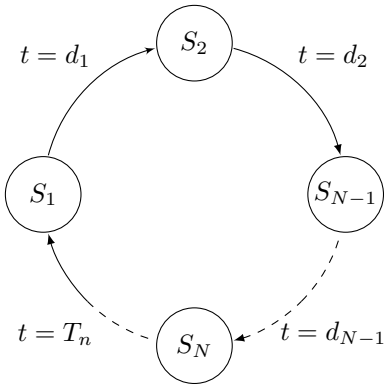


Figure 3.9: Hybrid automaton of a DC-DC converter

described with a set of ordinary differential equations or with a state-space model. This dynamics corresponds to the continuous behavior while the discrete behavior takes place when a transition between two states occurs. In Fig. 3.9, the first state, S_1, starts at $t = t_n$. Then the automaton jumps to state S_2 at $t = t_n + d_{1n}$, to the state S_N at $t = t_n + d_{(N-1)n}$ and finally returns to the state S_1 at $t = t_n + T_n$. Thus the nth-switching cycle is denoted $[t_n, t_n + T_n]$ where T_n is the duration of the nth cycle. The switching instants between the state are set manually in open-loop or imposed by a control law in closed-loop. Thus linear or hysteresis controls can be described with this uniform approach without any restrictions.
The classical sampled-data modeling approach detailed in [86] is now formulated for a cyclic hybrid automaton. In this thesis, dynamics of each states are described with state-representation and linear-time invariant (LTI) elements as follow

$$S_1 : \begin{cases} \dot{x} = A_1 x + B_1 U \\ y = C_1 x + D_1 U \end{cases} \text{ for } t \in [t_n, t_n + d_{1n}] \tag{3.27}$$

$$\vdots$$

$$S_i : \begin{cases} \dot{x} = A_i x + B_i U \\ y = C_i x + D_i U \end{cases} \text{ for } t \in [t_n + d_{(i-1)n}, t_n + d_{in}] \tag{3.28}$$

$$\vdots$$

$$S_N : \begin{cases} \dot{x} = A_N x + B_N U \\ y = C_N x + D_N U \end{cases} \text{ for } t \in [t_n + d_{(N-1)n}, t_n + T_n] \tag{3.29}$$

where x represents the state-vector, U, the input and y, the output. The state vector, x_i, corresponding to the state i of the hybrid automaton is determined for an initial state-vector, x_0 by

$$x_i\left(t, x_0\right) = e^{A_i t} x_0 + \int_0^t e^{A_i (t-\sigma)} d\sigma B_i u \tag{3.30}$$

At time t_i, (3.30) becomes (3.31)

$$x_i\left(t_i, x_0\right) = \Phi_i x_0 + \Gamma_i u \tag{3.31}$$

where,

$$\Phi_i = e^{A_i t_i} \tag{3.32}$$

$$\Gamma_i = \int_0^{t_i} e^{A_i \sigma} d\sigma B_i \tag{3.33}$$

Two distinct mathematical cases occur when Γ_i is analytically derived. If A_i is nonsingular, its inverse exists and

$$\Gamma_i = \left[e^{A_i t_i} - I\right] A_i^{-1} B_i \tag{3.34}$$

Where I is the identity matrix.
If A_i is singular, its inverse does not exist analytically and we use the Jordan Form to rewrite A_i as

$$A_i = P_i \begin{bmatrix} L_i & 0 \\ 0 & M_i \end{bmatrix} P_i^{-1} \tag{3.35}$$

Where L_i is strictly upper triangle and M_i is nonsingular. Then

$$\Gamma_i = \int_0^{t_i} e^{A_i \sigma} d\sigma B_i \tag{3.36}$$

$$= P_i \begin{bmatrix} \int_0^{t_i} e^{L_i \sigma} d\sigma & 0 \\ 0 & M_i^{-1}\left(e^{M_i t_i} - I\right) \end{bmatrix} P_i^{-1} B_i \tag{3.37}$$

Let's now evaluate the value of the state vector at each switching instant using (3.31) to assure the continuity between each state of the hybrid automaton. The cycle-to-cycle dynamics can be thus determined with a recurrence function by sampling the

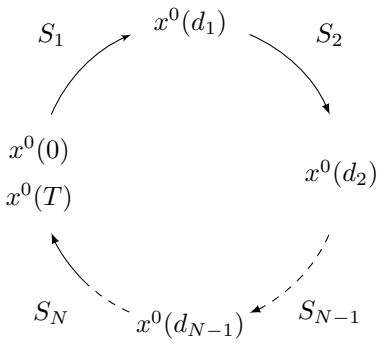


Figure 3.10: Periodic orbit in steady-state operation

system at $t = t_n$. We denote x_n and x_{n+1}, the state vectors at time t_n and $t_n + T_n$ respectively. The input vector, U is assumed constant over a cycle (this is generally true since we consider power supplies are established) and at t_n becomes u_n. The output vector is denoted y_n. The sampled-data model is

$$\begin{aligned} x_{n+1} &= f\left(x_n, u_n, \tau_n\right) \\ &= \Phi x_n + \Gamma u_n \\ y_n &= C x_n + D u_n \end{aligned} \tag{3.38}$$

where

$$\Phi = \prod_{k=1}^{N} \Phi_k \tag{3.39}$$

$$\Gamma = \sum_{k=1}^{N-1} \left(\prod_{j=2}^{N-k} \Phi_j \right) \Gamma_k + \Gamma_N \tag{3.40}$$

$$\tau_n = \begin{bmatrix} d_{1n} \\ \vdots \\ d_{Nn} \\ T_n \end{bmatrix} \tag{3.41}$$

The matrices C and D are used to determine outputs of the system at the end of the cycle.

The steady-state operation of the automaton corresponds to a T-periodic solution in the sampled-data model. The system describes a periodic orbit as depicted in Fig. 3.10. The solution $\left(x^0(0), U, \tau\right)$ is called the fixed point. The steady-state operation is reached when $x_{n+1} = x_n$ and the fixed point satisfies

$$x^0\left(0\right) = f\left(x^0\left(0\right), U, \tau\right) \tag{3.42}$$

$$x^0\left(0\right) = \Phi x^0(0) + \Gamma U \tag{3.43}$$

Finally the periodic solution of the state vector is

$$x^0(0) = (I - \Phi)^{-1} \Gamma U \tag{3.44}$$

Sampled-data modeling offers a powerful framework to analyze switched-mode converter. The converter can be modeled with the parasitics elements. The dead-time of switching can be represented with an extra state in the hybrid automaton. Finally sampled-data modeling offers the description of interleaved converters. This method is thus widely used along the thesis due to its uniform and systematic approach. The first application is the output resistance determination introduced in [87]. The sampled-data model of the converter is

$$\begin{aligned} x_{n+1} &= f(x_n, u_n, \tau_n) \\ v_{out_n} &= E x_n \end{aligned} \tag{3.45}$$

The output voltage of the converter, v_{out_n}, is isolated by the vector E when the converter has an ideal output capacitor. The output voltage is indeed the state variable representing the output capacitor voltage. The authors in [87] propose to evaluate it for any SC converter with a turning ratio $\frac{n}{m}$ as follows:

$$R_{out} = \frac{\frac{n}{m} V_{in} - V_{out}}{I_{load}} \tag{3.46}$$

$$= \frac{\frac{n}{m} V_{in} - E x^0(0)}{I_{load}} \tag{3.47}$$

For illustration purpose the sampled-data modeling is derived for a 2:1 SC converter and a 4-interleaved 2:1 SC converter. The diagram of the interleaved converter is depicted in Fig. 3.15 and the interleaving strategy is detailed in Section 3.5. The first step involved in the methodology is to extract the state-space matrices of each states. However manually deriving the state-space model using Kirchoff laws requires a lot of efforts. Fortunately dedicated tools have been developed to address this issue. A state-space model generator for SC converter is proposed in [88] and considerably simplifies the derivation but still requires some manual interventions. An automated extraction tool called HySim is therefore introduced. The extractions are perform using Spice circuit netlists with LTI elements avoiding any hand derivation mistakes. Therefore the complexity of the model does not depend on the number of elements and the time required for the derivation. HySim is presented in Appendix A. The state-space representation for the 2:1 SC converter where $\tau_1 = R_{on} C_{fly}$ and $\tau_2 = R_{on} C_{load}$ is

$$A_1 = \begin{bmatrix} \frac{-1}{2\tau_1} & \frac{-1}{2\tau_1} \\ \frac{-1}{2\tau_2} & \frac{-1}{2\tau_2} \end{bmatrix}, \; A_2 = \begin{bmatrix} \frac{-1}{2\tau_1} & \frac{1}{2\tau_1} \\ \frac{1}{2\tau_2} & \frac{-1}{2\tau_2} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 0 & \frac{1}{2\tau_1} \\ \frac{-1}{C_{load}} & \frac{1}{2\tau_2} \end{bmatrix},\ B_2 = \begin{bmatrix} 0 & 0 \\ \frac{-1}{C_{load}} & 0 \end{bmatrix}$$

$$C_1 = C_2 = E = \begin{bmatrix} 0 & 1 \end{bmatrix},\ D_1 = D_2 = 0$$

$$U = \begin{bmatrix} I_{load} \\ V_{in} \end{bmatrix},\ x = \begin{bmatrix} v_{C_{fly}} \\ v_{C_{load}} \end{bmatrix},\ \tau = \begin{bmatrix} d \\ T \end{bmatrix}$$

Mathematical issue is encountered for this case. The determinant of the matrix A_1 and A_2 are

$$det[A_1] = \frac{-1}{2\tau_1}\frac{-1}{2\tau_2} - \frac{-1}{2\tau_1}\frac{-1}{2\tau_2} = 0 \tag{3.48}$$

$$det[A_2] = \frac{-1}{2\tau_1}\frac{-1}{2\tau_2} - \frac{1}{2\tau_1}\frac{1}{2\tau_2} = 0 \tag{3.49}$$

As a consequence the matrices are singular. The Jordan decomposition is used to compute the matrices Γ_1 and Γ_2:

$$A_1 = P_1 J_1 P_1^{-1} = \begin{bmatrix} -1 & \frac{\tau_2}{\tau_1} \\ 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} 0 & 0 \\ 0 & -\frac{\tau_1+\tau_2}{2\tau_1\tau_2} \end{bmatrix} \cdot \begin{bmatrix} -\frac{\tau_1}{\tau_1+\tau_2} & \frac{\tau_2}{\tau_1+\tau_2} \\ \frac{\tau_1}{\tau_1+\tau_2} & \frac{\tau_1}{\tau_1+\tau_2} \end{bmatrix} \tag{3.50}$$

$$A_2 = P_2 J_2 P_2^{-1} = \begin{bmatrix} 1 & -\frac{\tau_2}{\tau_1} \\ 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} 0 & 0 \\ 0 & -\frac{\tau_1+\tau_2}{2\tau_1\tau_2} \end{bmatrix} \cdot \begin{bmatrix} \frac{\tau_1}{\tau_1+\tau_2} & \frac{\tau_2}{\tau_1+\tau_2} \\ -\frac{\tau_1}{\tau_1+\tau_2} & \frac{\tau_1}{\tau_1+\tau_2} \end{bmatrix} \tag{3.51}$$

The matrices Γ_1 and Γ_2 are given using (3.37)

$$\Gamma_1 = \int_0^d e^{A_1\sigma} d\sigma B_1 \tag{3.52}$$

$$= P_1 \cdot \begin{bmatrix} d & 0 \\ 0 & -\frac{2\tau_1\tau_2}{\tau_1+\tau_2}\left(e^{-d\frac{\tau_1+\tau_2}{2\tau_1\tau_2}} - 1\right) \end{bmatrix} \cdot P_1^{-1} B_1 \tag{3.53}$$

$$\Gamma_2 = \int_0^{(T-d)} e^{A_2\sigma} d\sigma B_2 \tag{3.54}$$

$$= P_2 \cdot \begin{bmatrix} T-d & 0 \\ 0 & -\frac{2\tau_1\tau_2}{\tau_1+\tau_2}\left(e^{-(T-d)\frac{\tau_1+\tau_2}{2\tau_1\tau_2}} - 1\right) \end{bmatrix} \cdot P_2^{-1} B_2 \tag{3.55}$$

Numerical integration can be used instead. Introduction of an off-state switch resistance can also transform the system into non-singular matrices. The state-space representation of such a system in given in Appendix B.1. The state-space representation for the 2:1 SC converter with four interleaved cells where $\tau_1 = R_{on}C_{fly}$

and $\tau_2 = R_{on}C_{load}$ is

$$A_1 = \begin{bmatrix} \frac{-1}{2\tau_1} & 0 & 0 & 0 & \frac{-1}{2\tau_1} \\ 0 & \frac{-1}{2\tau_1} & 0 & 0 & \frac{1}{2\tau_1} \\ 0 & 0 & \frac{-1}{2\tau_1} & 0 & \frac{1}{2\tau_1} \\ 0 & 0 & 0 & \frac{-1}{2\tau_1} & \frac{-1}{2\tau_1} \\ \frac{-1}{2\tau_2} & \frac{1}{2\tau_2} & \frac{1}{2\tau_2} & \frac{-1}{2\tau_2} & \frac{-2}{\tau_2} \end{bmatrix}, \quad A_2 = \begin{bmatrix} \frac{-1}{2\tau_1} & 0 & 0 & 0 & \frac{-1}{2\tau_1} \\ 0 & \frac{-1}{2\tau_1} & 0 & 0 & \frac{-1}{2\tau_1} \\ 0 & 0 & \frac{-1}{2\tau_1} & 0 & \frac{1}{2\tau_1} \\ 0 & 0 & 0 & \frac{-1}{2\tau_1} & \frac{1}{2\tau_1} \\ \frac{-1}{2\tau_2} & \frac{-1}{2\tau_2} & \frac{1}{2\tau_2} & \frac{1}{2\tau_2} & \frac{-2}{\tau_2} \end{bmatrix}$$

$$A_3 = \begin{bmatrix} \frac{-1}{2\tau_1} & 0 & 0 & 0 & \frac{1}{2\tau_1} \\ 0 & \frac{-1}{2\tau_1} & 0 & 0 & \frac{-1}{2\tau_1} \\ 0 & 0 & \frac{-1}{2\tau_1} & 0 & \frac{-1}{2\tau_1} \\ 0 & 0 & 0 & \frac{-1}{2\tau_1} & \frac{1}{2\tau_1} \\ \frac{1}{2\tau_2} & \frac{-1}{2\tau_2} & \frac{-1}{2\tau_2} & \frac{1}{2\tau_2} & \frac{-2}{\tau_2} \end{bmatrix}, \quad A_4 = \begin{bmatrix} \frac{-1}{2\tau_1} & 0 & 0 & 0 & \frac{1}{2\tau_1} \\ 0 & \frac{-1}{2\tau_1} & 0 & 0 & \frac{1}{2\tau_1} \\ 0 & 0 & \frac{-1}{2\tau_1} & 0 & \frac{-1}{2\tau_1} \\ 0 & 0 & 0 & \frac{-1}{2\tau_1} & \frac{-1}{2\tau_1} \\ \frac{1}{2\tau_2} & \frac{1}{2\tau_2} & \frac{-1}{2\tau_2} & \frac{-1}{2\tau_2} & \frac{-2}{\tau_2} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 0 & \frac{1}{2\tau_1} \\ 0 & \frac{1}{2\tau_1} \\ 0 & 0 \\ 0 & 0 \\ \frac{-1}{C_{load}} & \frac{1}{\tau_2} \end{bmatrix}, \; B_2 = \begin{bmatrix} 0 & \frac{1}{2\tau_1} \\ 0 & 0 \\ 0 & 0 \\ 0 & \frac{1}{2\tau_1} \\ \frac{-1}{C_{load}} & \frac{1}{\tau_2} \end{bmatrix}$$

$$B_3 = \begin{bmatrix} 0 & 0 \\ 0 & \frac{1}{2\tau_1} \\ 0 & \frac{1}{2\tau_1} \\ 0 & 0 \\ \frac{-1}{C_{load}} & \frac{1}{\tau_2} \end{bmatrix}, \; B_4 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & \frac{1}{2\tau_1} \\ 0 & \frac{1}{2\tau_1} \\ \frac{-1}{C_{load}} & \frac{1}{\tau_2} \end{bmatrix}$$

	V_{in}	C_{fly}	R_{on}	C_{load}	I_{load}	f_{sw}
Simple	$2\ V$	$200\ pF$	$10\ \Omega$	$10\ nF$	$5\ mA$	$10\ MHz$
4 interleaved structure	$2\ V$	$50\ pF$	$40\ \Omega$	$10\ nF$	$5\ mA$	$10\ MHz$

Table 3.2: Parameters for the evaluation of the sampled-data model

$$x = \begin{bmatrix} v_{C_{fly1}} \\ v_{C_{fly2}} \\ v_{C_{fly3}} \\ v_{C_{fly4}} \\ v_{C_{load}} \end{bmatrix},\ U = \begin{bmatrix} I_{load} \\ V_{in} \end{bmatrix},\ \tau = \begin{bmatrix} d_1 \\ d_2 \\ d_3 \\ T \end{bmatrix}$$

$$C_1 = C_2 = C_3 = C_4 = E = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

$$D_1 = D_2 = D_3 = D_4 = 0$$

Three cases are considered for the sampled-data model evaluation: the 2:1 SC converter, a 4-interleaved 2:1 SC converter with equal interleaving times and a 4-interleaved 2:1 SC converter with non-equal interleaving times. The fixed point solution $\left(x^0(0), U, \tau\right)^{(1)}$ denotes the 2:1 SC converter case, $\left(x^0(0), U, \tau\right)^{(2)}$ the 4-interleaved with equal interleaving times and $\left(x^0(0), U, \tau\right)^{(3)}$ in the case of non-equal interleaving times. The parameter values for each case are given in Table 3.2.

$$\left(x^0(0), U, \tau\right)^{(1)} = \begin{cases} x^0(0) = \begin{pmatrix} 0.375 & 0.373 \end{pmatrix}' \\ U = \begin{pmatrix} 5 \cdot 10^{-3} & 2 \end{pmatrix}' \\ \tau = \begin{pmatrix} 5 \cdot 10^{-8} & 1 \cdot 10^{-7} \end{pmatrix}' \end{cases}$$

$$\left(x^0(0), U, \tau\right)^{(2)} = \begin{cases} x^0(0) = \begin{pmatrix} 0.3751 & 0.3751 & 1.6249 & 1.6249 & 0.3749 \end{pmatrix}' \\ U = \begin{pmatrix} 5 \cdot 10^{-3} & 2 \end{pmatrix}' \\ \tau = \begin{pmatrix} 2.5 \cdot 10^{-8} & 5 \cdot 10^{-8} & 7.5 \cdot 10^{-8} & 1 \cdot 10^{-7} \end{pmatrix}' \end{cases}$$

$$\left(x^0(0), U, \tau\right)^{(3)} = \begin{cases} x^0(0) = \begin{pmatrix} 0.3751 & 0.3751 & 1.6249 & 1.6249 & 0.3749 \end{pmatrix}' \\ U = \begin{pmatrix} 5 \cdot 10^{-3} & 2 \end{pmatrix}' \\ \tau = \begin{pmatrix} 2 \cdot 10^{-8} & 5.5 \cdot 10^{-8} & 7.5 \cdot 10^{-8} & 1 \cdot 10^{-7} \end{pmatrix}' \end{cases}$$

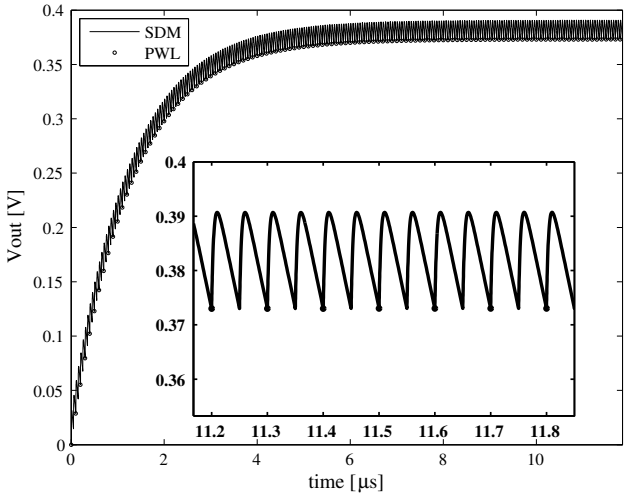


Figure 3.11: Transient simulation of a simple 2:1 SC converter: PWL model and sampled-data model

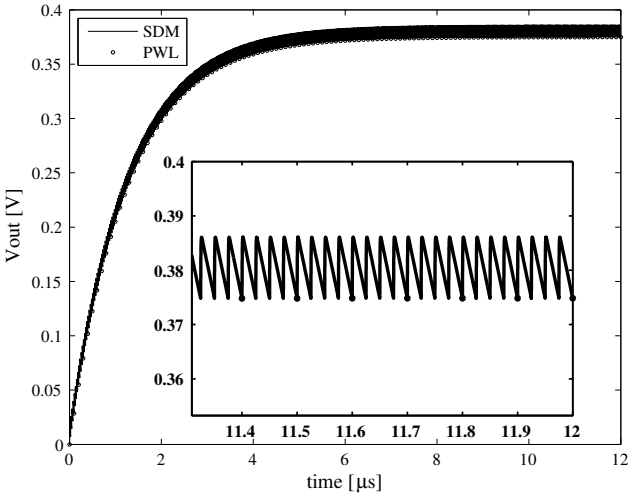


Figure 3.12: Transient simulation of a four phases 2:1 SC converter with equal interleaving times: PWL model and the sampled-data model

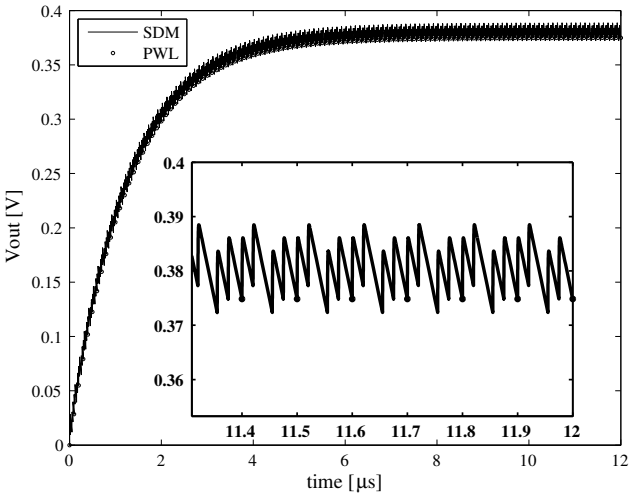


Figure 3.13: Transient simulation of a four phases 2:1 SC converter with non-equal interleaving times: PWL model and the sampled-data model

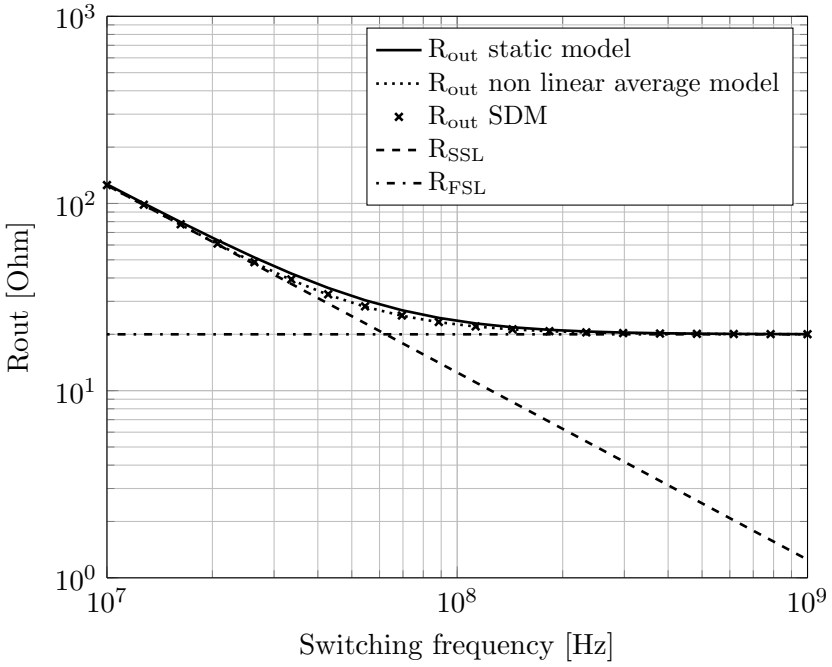


Figure 3.14: Output resistance diagram

The hybrid automata are implemented using PWL[1] models in *Matlab/Simulink* (state-flow toolbox could also be used). Then simulations are performed and compared to sampled-data model results. The transient simulation of the simple converter is shown in Fig. 3.11. Fig. 3.12 covers the equal interleaving and Fig. 3.13 the case of non equal interleaving times. The results about the output resistance calculation of the various model are compared in Fig. 3.14. The non linear average model and the sampled-data model give similar results while the static model exhibits a small discrepancy near the curvature between the SSL and FSL region. This comes from the approximation in the output resistance.

3.3 Losses

The losses and the efficiency of a SC converter are evaluated with non ideal devices. The switches are implemented with MOSFET transistors and the capacitors are implemented with devices available in the CMOS process. The equivalent model used for losses derivation is shown in Fig. 3.16a for a CMOS switch and in Fig. 3.16b for the flying capacitor . The on-state resistance is R_{on} and C_{gate} corresponds to the equivalent capacitance charged/discharged when the switch is turned on/off. The flying capacitor exhibits an equivalent series-resistance, R_{ESR}, accounting the

[1] Piecewise linear

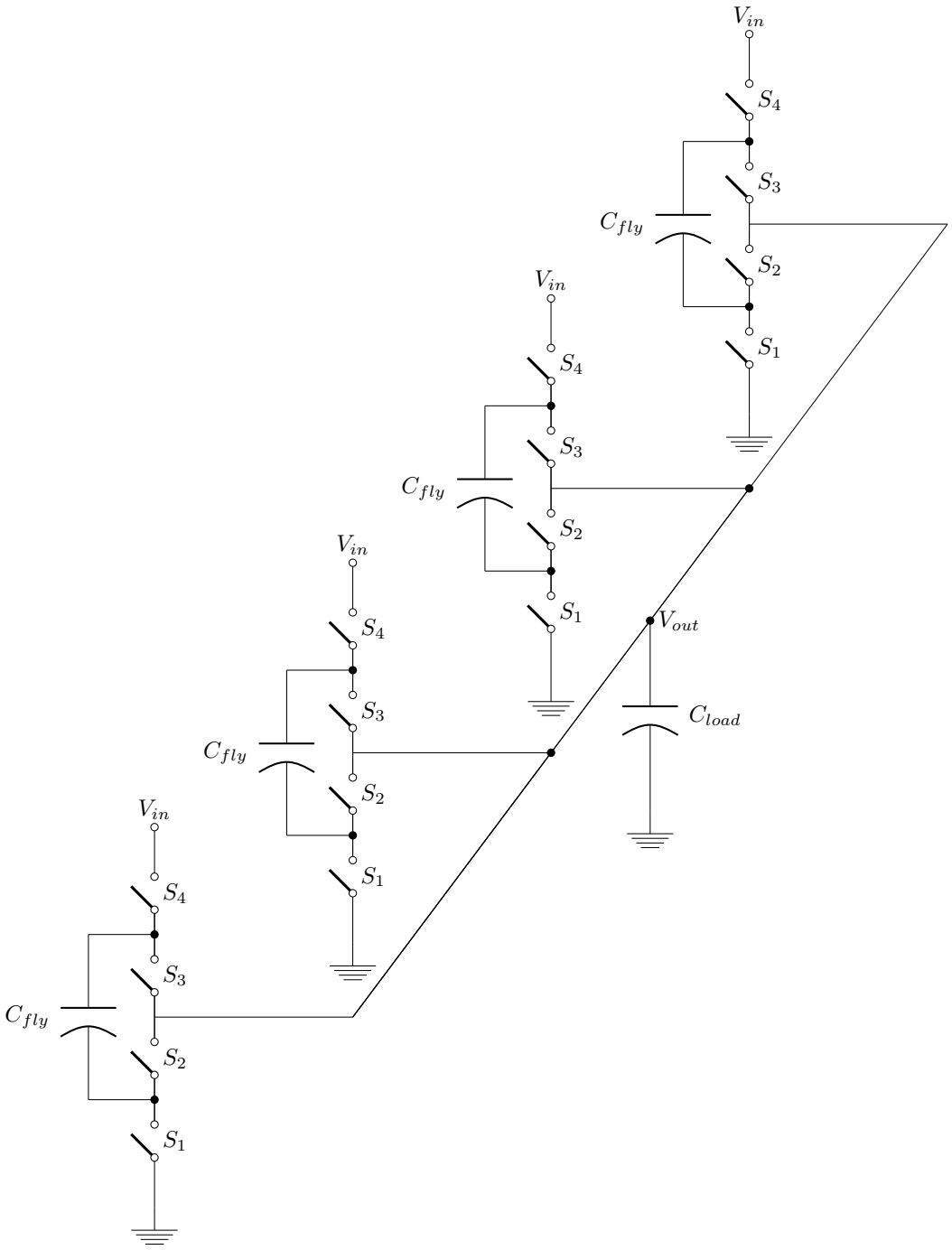
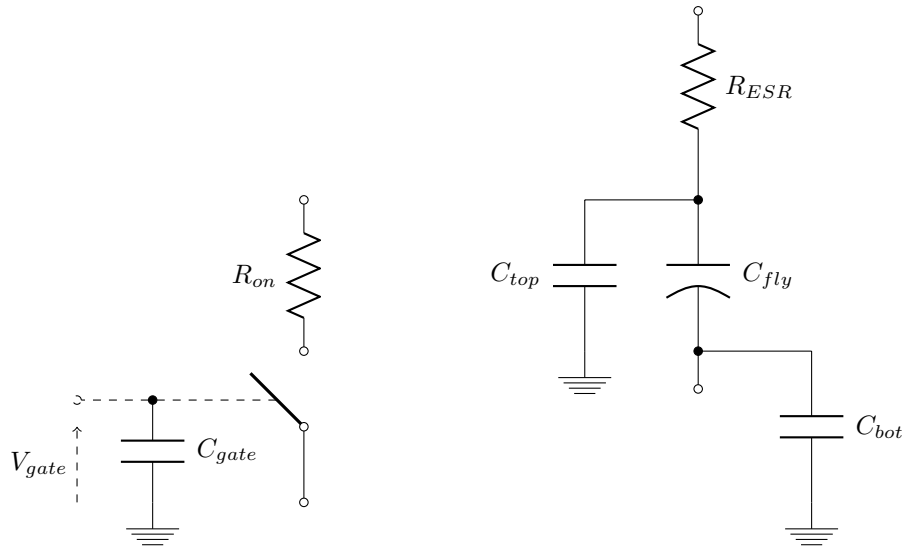


Figure 3.15: SC converter interleaved with 4 sub-cell



(a) Representation of a switch (b) Representation of a capacitor

Figure 3.16: Representation of the parasitic elements

resistance of the plate. The value of R_{ESR} depends on the materials used for the plates. The coupling between the plate and the substrate is represented by the capacitors C_{top} and C_{bot}. This coupling depends on the distance and the isolation to the substrate. The losses encountered in a SC converter are separated in two types: the inherent losses (static) and the parasitic losses (switching). The inherent losses are accounted by the output resistance. They are proportional to the load current. The power losses in the output resistance are:

$$P_{R_{out}} = R_{out} I_{load}^2 \tag{3.56}$$

In the SSL region, the losses are associated to the capacitor and the switching frequency. Let W_c be the width of the flying capacitor, L_c the length of the flying capacitor and C_c^0 the density of the flying capacitor:

$$C_{fly} = W_c L_c C_c^0 \tag{3.57}$$

The losses in the SSL are expressed as

$$P_{SSL} \propto \frac{1}{W_c L_c C_c^0 f_{sw}} \tag{3.58}$$

On the contrary the losses are dominated by the resistive losses in the FSL region. The derivation of the output resistance includes the on-state resistance, R_{on}, as well as the equivalent series-resistance of the capacitor, R_{ESR}. The equivalent series-resistance is expressed with W_c, L_c and σ_c, the resistivity of the plate in $\Omega/\square$:

$$R_{ESR} = \frac{L_c}{W_c} \sigma_c \tag{3.59}$$

Power loss	C_c^0	W_c	L_c	α_{top}	α_{bot}	σ_c	C_g^0	W_s	L_s	σ_s	f_{sw}	D
P_{SSL}	↓	↓	↓	–	–	–	–	–	–	–	↓	–
P_{FSL}	–	↓	↑	–	–	↑	–	↓	↓	↑	–	↓
P_{gate}	–	–	–	–	–	–	↑	↑	↑	–	↑	–
P_{top}	–	↑	↑	↑	–	–	–	–	–	–	↑	–
P_{bot}	–	↑	↑	–	↑	–	–	–	–	–	↑	–

Table 3.3: Wrap-up of the parameter influences on the losses

Similarly the on-state resistance is defined as:

$$R_{on} = \frac{L_s}{W_s}\sigma_s \tag{3.60}$$

where W_s is the width of the transistor, L_s the length and σ_c the resistivity in Ω/□. The power losses of the output resistance in the FSL region are:

$$P_{FSL} \propto \frac{L_c\sigma_c}{W_c D} + \frac{L_s\sigma_s}{W_s D} \tag{3.61}$$

The parasitic losses of the switches and the capacitors are included in addition to the output resistance losses. The switching losses of the gate capacitance are computed as follows:

$$P_{gate} = C_{gate}V_{gate}^2 f_{sw} \tag{3.62}$$

Let C_g^0 be the density of the gate capacitance of the switch, (3.62) becomes:

$$P_{gate} = W_s L_s C_g^0 V_{gate}^2 f_{sw} \tag{3.63}$$

Then the power losses of the parasitic capacitances are:

$$P_{top} = C_{bot}V_{top}^2 f_{sw} \tag{3.64}$$

$$= \alpha_{top}C_{fly}V_{top}^2 f_{sw} \tag{3.65}$$

$$= \alpha_{top}W_c L_c C_c^0 V_{top}^2 f_{sw} \tag{3.66}$$

where V_{top} and V_{bot} are the voltages across C_{top} and C_{bot} respectively, α_{top} and α_{bot} are the ratios between the parasitic capacitances and the flying capacitance. The influence of each parameters on the various losses are shown in Table 3.3. A up-arrow (↑) indicates that the corresponding loss increases with parameter while a

down-arrow (↓) indicates that it decreases. It is important to note that the parasitic capacitance losses do not increase with the flying capacitor density but only with the area and the parasitic ratio (α_{top} and α_{bot}).
The efficiency of the converter is finally computed as follows:

$$\eta = \frac{V_{out} I_{load}}{V_{out} I_{load} + P_{R_{out}} + P_{gate} + P_{top} + P_{bot}} \tag{3.67}$$

3.4 Efficiency optimization

The output power of the converter is determined by the load requirement and the efficiency can be maximized. The output power constrains the output impedance as follow:

$$V_{max} = \frac{n}{m} V_{in} - R_{out} I_{max} \tag{3.68}$$

$$R_{out} = \frac{\frac{n}{m} V_{in} - V_{max}}{I_{max}} \tag{3.69}$$

where I_{max} is the maximal load current and V_{max} is the maximal output voltage at I_{max}. The optimization involves to reach the output resistance target while minimizing the power losses. The characteristic of the components (C_c^0, α_{bot}, α_{top}, σ_c, C_g^0 and σ_s) are determined by the type of selected devices and the design parameters are thus W_c, L_c, W_s and L_s. The area constraint is included in the optimization method. The area is often determined by the flying capacitor in fully integrated SC converters. The area available for the capacitors is set as well as the form factor (W_c and L_c) for a given capacitor type. Then the switches are selected and L_c is set to the minimal possible value. The length of the switches can be increased for ultra low power target to reduce the leakage current and increase the I_{on}/I_{off} ratio. However the leakage current has a small impact on the efficiency in high power conditions whereas the gate capacitance increases the associated losses. Thus the two design variables, W_s and f_{sw} are swept to achieve the highest efficiency for the targeted output power. Different figures of merit are generated using Seeman's framework [74,89] to illustrate the optimization trade-off for various flying capacitor specifications. The first figure of merit shown in Fig. 3.17 is the efficiency of the converter versus the area of the flying capacitor for a fixed output current. Each point corresponds to the optimal efficiency achieved for a given switching frequency and a switch width. The highest efficiency is always achieved for the highest area of capacitor for a given specification. The efficiency is here limited by the capacitor parasitic ratio (α_{top} and α_{bot}). The optimal efficiency decreases when the area decreases and the capacitor density is a major parameter. The second well-known figure of merit

presented in Fig. 3.18 is the efficiency versus the power density. The power density is defined as the output power to silicon area ratio. High power density design requires high density capacitors and low ESR values while low power density ones must consider low parasitic ratio values. The efficiency versus the current density value is an alternative to the previous one. The output current is divided by the area and the results are depicted in Fig. 3.19. The corresponding output voltage is added in Fig. 3.20. Finally, the optimal switching frequency and the optimal area of the switches in term of efficiency are given versus area in Fig. 3.21 and Fig. 3.22 respectively. The switching frequency decreases almost linearly with the area. Thus the switching losses are reduced and the width of the switches can be increased to lower the resistive losses. As a consequence, an increase in area benefits the efficiency point of view. However the parasitic ratio limits the efficiency value in this region. As a conclusion regarding area constrained design with high power density, the designer has to choose high capacitor density with low ESR values.

3.5 Ripple reduction technique

The inherent charge transfer of a SC converter causes output voltage ripple. The noise of the output voltage could alter the behavior of the powered blocks. An output capacitor is usually used to mitigate the issue. The current in the capacitor is the difference between the instantaneous current delivered by the converter, I_{out} and the instantaneous current consumed by the load, I_{load}. This difference is integrated by the output capacitor over a switching period yielding a voltage ripple. The value of the output voltage ripple is approximated by:

$$\Delta V_{out} \propto \frac{I_{load}}{f_{sw} \cdot C_{load}} \tag{3.70}$$

Where C_{load} is the output capacitor and f_{sw} is the switching frequency. [90] has reported that the output voltage ripple value can be improved with proper on-state switch resistance. Fundamentally, the output capacitor value should be increased to reduce the output voltage ripple. However in compact and fully integrated solution, the output capacitor costs an area penalty and this solution is not suitable. Interleaving schemes have been introduced to address this issue. The initial converter is split in N subsets of converter where N is the so-called interleaving factor. The converter subsets operate in parallel and the clocks are shifted by T_{sw}/N, where T_{sw} is the switching period seen by the capacitor. Thus the values of the flying capacitors may be divided by N and the on-state resistance would be multiplied by N. Small amounts of charge are delivered regularly during the switching period rather than a large amount with less recurrence. The operation of interleaving is described in Fig. 3.23. The ripple voltage is theoretically almost canceled with a large

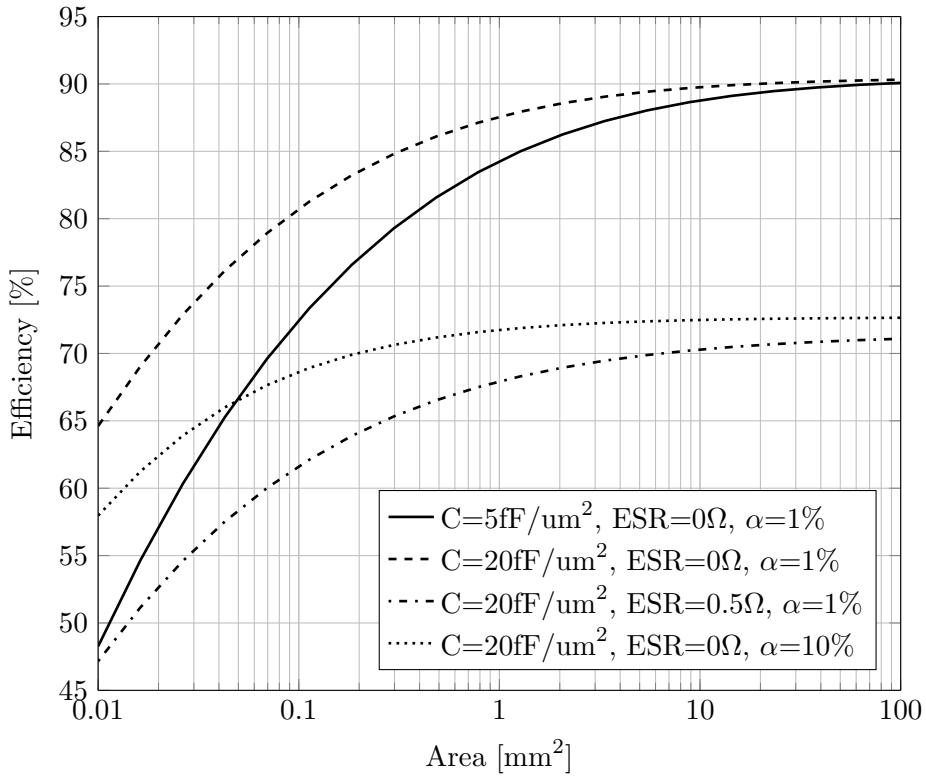


Figure 3.17: Efficiency vs flying capacitor area for various flying capacitor specifications

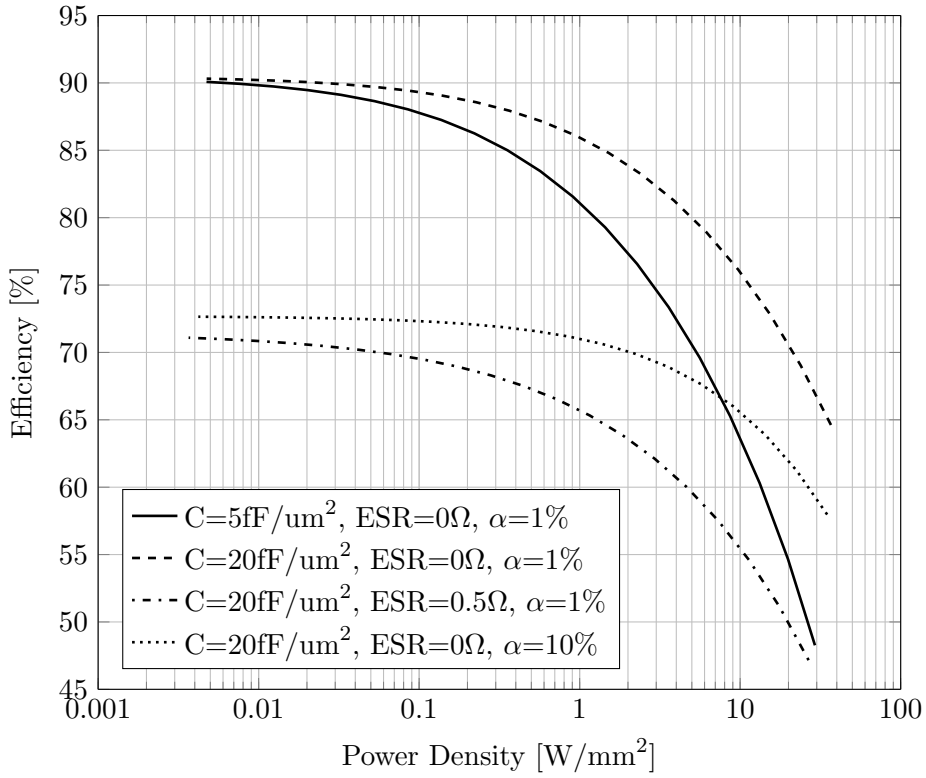


Figure 3.18: Efficiency vs power density for various flying capacitor specifications

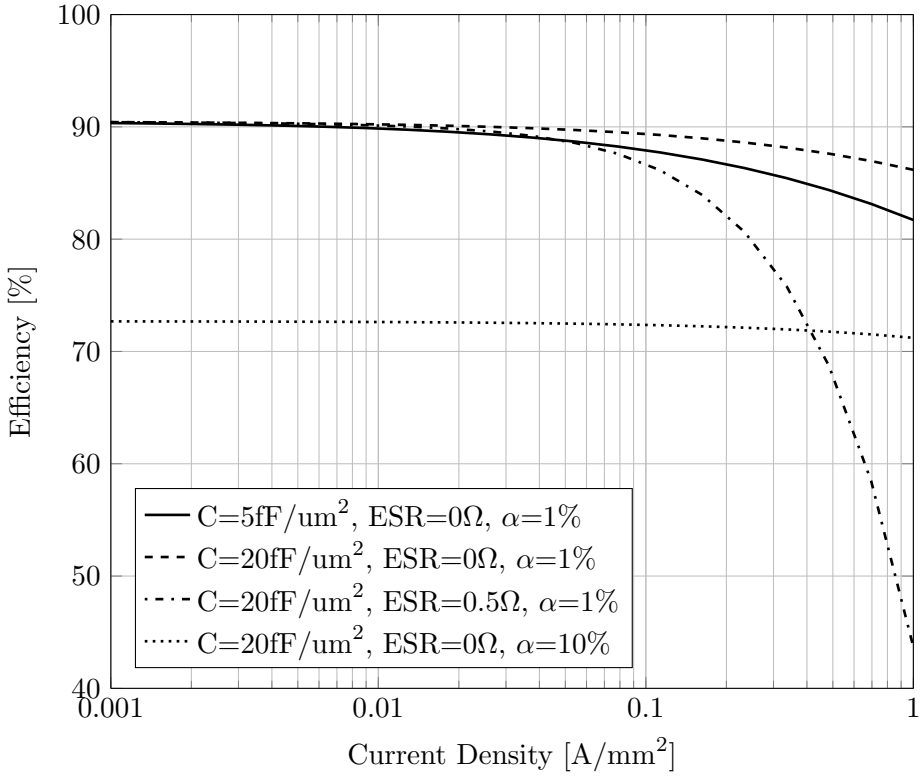


Figure 3.19: Efficiency vs current density for various flying capacitor specifications

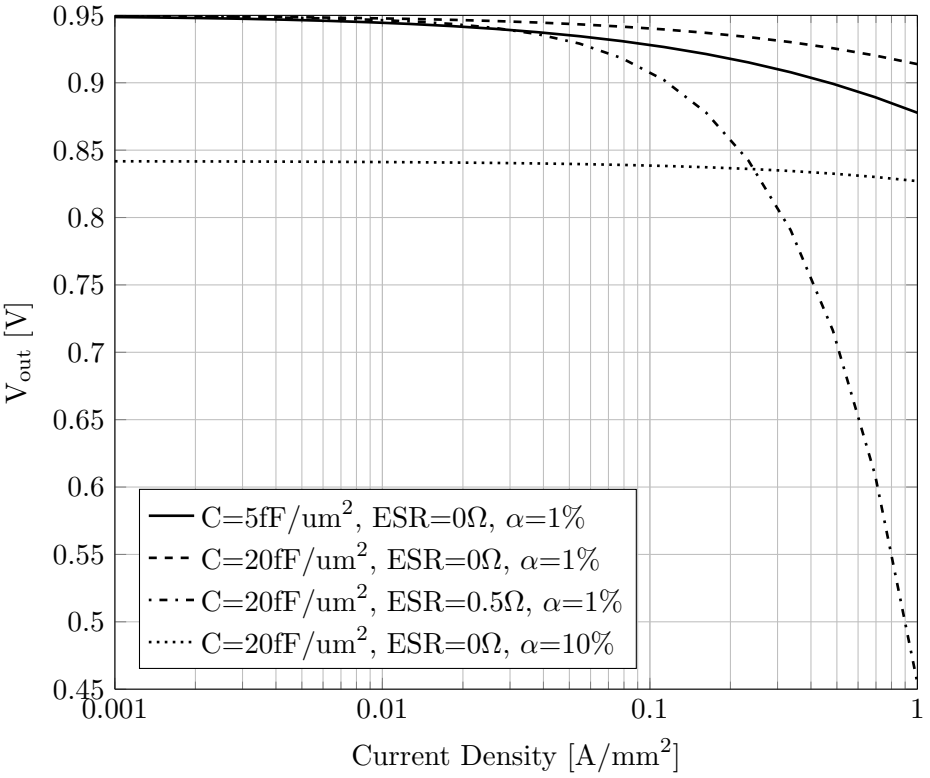


Figure 3.20: Output voltage vs current density for various flying capacitor specifications

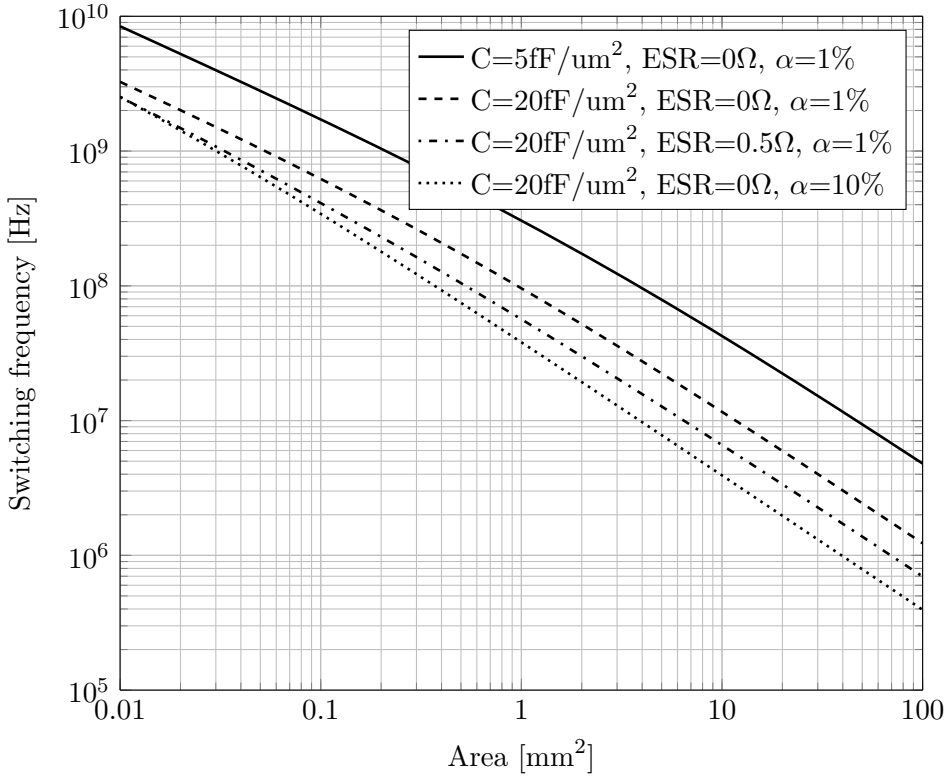


Figure 3.21: Efficiency vs current density for various flying capacitor specifications

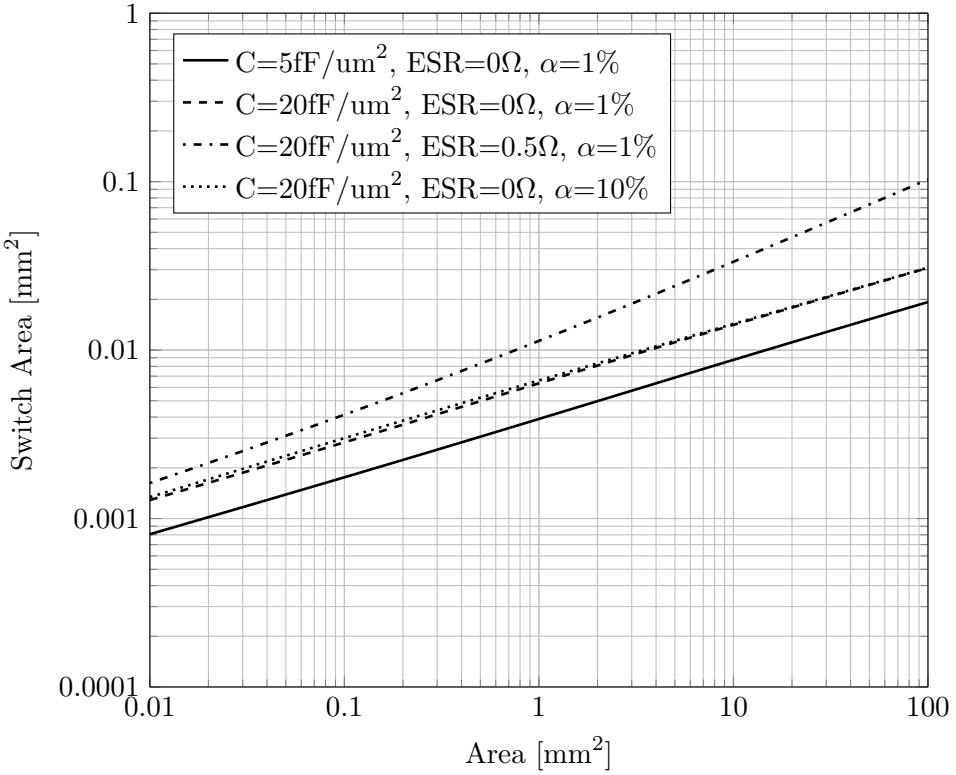


Figure 3.22: Output voltage vs current density for various flying capacitor specifications

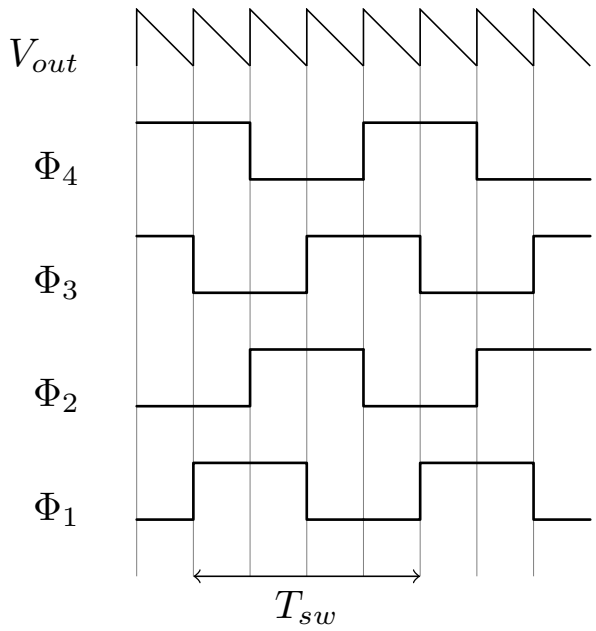


Figure 3.23: Diagram of the operation of an 4-interleaved SC converter

interleaving factor. The output capacitor is reduced and possibly even removed. However the complexity of the clock generation limits in practice the interleaving factor value. Moreover inaccuracy in the delay between each clocks results in a random ripple cancellation.

3.6 Control & regulation

3.6.1 Regulation principle

SC converter are represented by transformer model and an output resistance. The input voltage is converted by the transformer ratio. The output voltage never reaches the ideal ratio due to the voltage drop on the output resistance under non-zero load condition. Thus the output voltage, V_{out}, is a function of the converter ratio and the output resistance drop as follows

$$V_{out} = \frac{n}{m} \cdot V_{in} - R_{out}\left(C_{fly}, f_{sw}, R_{on}, D\right) \cdot I_{load} \tag{3.71}$$

Two control strategies come from (3.71): either the converter ratio or output resistance can be adjusted. The reconfiguration of ratio requires multi-ratio topologies and a gear-box with a control to properly choose the ratio [55]. This allows only a coarse regulation and it is required in case of wide input/output voltage range. The converter can operate close to the best ratio to maintain the efficiency as high as possible. The output resistance modulation offers a fine grain regulation capa-

bility but it cannot be achieved without any power dissipation. This is identical to linear regulator where the efficiency is limited by the ratio between the output and input voltage. Thus the output resistance modulation is realized through capacitance modulation or frequency modulation when the converter operates in SSL while pulse width modulation or conductance modulation is used in the FSL region.

3.6.1.1 Capacitance modulation

Capacitance modulation modifies the value of the flying capacitor dynamically. This can be achieved with scalable capacitors. The net value of capacitor is selected by a digital control [91]. Unfortunately the capacitor value can only be varied with discrete value step. Fine grain regulation is therefore quite complicated. Moreover the switching frequency is kept constant in such control and the switching losses become significant at light load condition.

3.6.1.2 Frequency modulation

Frequency modulation is a very popular technique. The switching frequency can be varied over a wide range to achieve fine grain regulation. The switching frequency also scales with the load current and the efficiency of the converter can be maintained constant for a given regulated output voltage. Such a regulation in the SSL region implies a proportional dependency of the output voltage ripple to the switching frequency and the load current. Non constant frequency may cause trouble to radio-frequency systems.

3.6.1.3 Pulse width modulation

Pulse width modulation is widely used in inductive DC-DC converter. This control can be used in the FSL region because the resistive losses are the main contributors to the output resistance losses. This techniques is highly limited to a small range of duty cycle [92].

3.6.1.4 Conductance modulation

Conductance modulation is performed playing on the on-state resistance of the switches. As for capacitance modulation scalable switches can be implemented. The width of the transistors is varied with discrete values [90]. An adaptive gate driver is required to achieve continuous regulation [93, 94]. This techniques has demonstrated good results on the output voltage ripple. The voltage ripple is significantly reduced at light load condition as well [90].
The frequency modulation is the most suitable control to fulfill the fine grain wide

regulation control and high efficiency requirements. Chapter 4 will detail the implementation of a frequency modulation control.

3.6.2 Small-signal behavior

The frequency response of a converter is essential to understand the input-to-output relation as well as to design a controller. The small-signal model of switched-mode converters is not straightforward. The switching behavior must be described with a discrete system or approximated with a continuous model.
The continuous models are described using the output voltage relation (3.71) and the Laplace block diagram in Fig. 3.24. The input voltage, V_{in} and the output current,

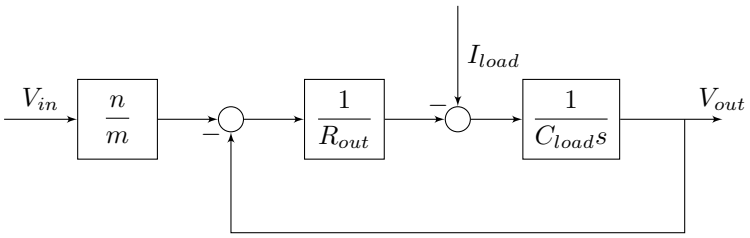


Figure 3.24: Representation of SC converter dynamics

I_{load} are the inputs of the system while the output voltage, V_{out}, is the output. In case of perturbations in the input voltage, the output current contribution is set to zero yielding the audio susceptibility:

$$\frac{\hat{v}_{out}(s)}{\hat{v}_{in}(s)} = \frac{n}{m}\frac{1}{1 + R_{out}C_{out}s} \tag{3.72}$$

Then output impedance is derived when a perturbation is applied to the output current while the input voltage is set to zero:

$$\frac{\hat{v}_{out}(s)}{\hat{i}_{load}(s)} = \frac{R_{out}}{1 + R_{out}C_{out}s} \tag{3.73}$$

The system is a first order type with a pole determined by the output resistance and the output capacitor. The value of R_{out} depends on the operating point. Therefore the pole value will change according to the operating point resulting in a non linear behavior. Moreover this model does not offer straight derivation of the control-to-output transfer function. A linearization must be performed around an operating point when the output resistance is written as $R_{out} = f(f_{sw}, D)$. The expression of the output resistance can be either the static model in Section 3.2.1 or the non linear average model in Section 3.2.3. Then the block diagram of Fig. 3.24 can be implemented in *Matlab/Simulink* to compute the transfer functions using the linear

analysis toolbox. We propose to linearize the sampled-data model around the fixed point solution to derive the small-signal dynamics [86]:

$$\hat{x}_{n+1} \approx \frac{\partial f}{\partial x_n}\hat{x}_n + \frac{\partial f}{\partial u_n}\hat{u}_n + \frac{\partial f}{\partial \tau_n}\hat{\tau}_n \tag{3.74}$$

$$\hat{x}_{n+1} \approx \Phi_0\hat{x}_n + \Gamma_u\hat{u}_n + \Gamma_\tau\hat{\tau}_n \tag{3.75}$$

$$\hat{y}_n \approx C\hat{x}_n + D\hat{u}_n \tag{3.76}$$

with

$$\frac{\partial f}{\partial x_n} = \Phi_0 = \prod_{k=1}^{N}\Phi_k \tag{3.77}$$

$$\frac{\partial f}{\partial u_n} = \Gamma_u = \sum_{k=1}^{N-1}\left(\prod_{j=2}^{N-k}\Phi_j\right)\Gamma_k + \Gamma_N \tag{3.78}$$

$$\frac{\partial f}{\partial \tau_n} = \Gamma_\tau = \begin{bmatrix} \Gamma_{d_1} & \Gamma_{d_2} & \dots & \Gamma_{d_{N-1}} & \Gamma_T \end{bmatrix} \tag{3.79}$$

$$= \Gamma_\tau = \begin{bmatrix} \dfrac{\partial f}{\partial d_{1n}} & \dfrac{\partial f}{\partial d_{2n}} & \cdots & \dfrac{\partial f}{\partial d_{(N-1)n}} & \dfrac{\partial f}{\partial T_n} \end{bmatrix} \tag{3.80}$$

$$\frac{\partial f}{\partial d_{in}} = \Gamma_{d_i} = \left(\prod_{k=i+1}^{N}\Phi_k\right)\left[(A_i - A_{i+1})\,x^0(d_i) + (B_i - B_{i+1})\,U\right] \tag{3.81}$$

$$\frac{\partial f}{\partial T_n} = \Gamma_T = \Phi_N\left[A_N x^0(d_{N-1}) + B_N U\right] \tag{3.82}$$

The linearized dynamics is derived in discrete time. The input-to-output transfer functions are

$$\frac{y(z)}{u(z)} = C\cdot(zI - \Phi_0)^{-1}\cdot\Gamma_u + D \tag{3.83}$$

The switching instant-to-output transfer functions in z-domain are:

$$\frac{y(z)}{d_i(z)} = C\cdot(zI - \Phi_0)^{-1}\cdot\Gamma_{d_i} \tag{3.84}$$

$$\frac{y(z)}{T(z)} = C\cdot(zI - \Phi_0)^{-1}\cdot\Gamma_T \tag{3.85}$$

The z-domain transfer functions are useful for discrete control design but the s-domain expression is required for continuous control. The zero-order hold method is suitable since the inputs are assumed to be constant over two sampling instants and the output signal is sampled without band-limiting anti-aliasing filter [86, 95]. We propose to illustrate the small-signal model derivation for the 2:1 SC converter. The operating point is defined by a switching frequency of 100 MHz and a duty-cycle of 50%. The system has two switching instants, d_n and T_n, and the system is written as follow

$$\hat{x}_{n+1} \approx \frac{\partial f}{\partial x_n}\hat{x}_n + \frac{\partial f}{\partial u_n}\hat{u}_n + \frac{\partial f}{\partial d_n}\hat{d}_n + \frac{\partial f}{\partial T_n}\hat{T}_n \tag{3.86}$$

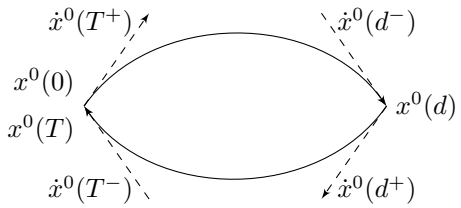


Figure 3.25: Periodic solution with the derivative

$$\hat{x}_{n+1} \approx \Phi_0 \hat{x}_n + \Gamma_u \hat{u}_n + \Gamma_d \hat{d}_n + \Gamma_T \hat{T}_n \tag{3.87}$$

$$\hat{v}_{out_n} \approx E \hat{x}_n \tag{3.88}$$

where

$$\frac{\partial f}{\partial x_n} = \Phi_0 = \Phi_2 \Phi_1 \tag{3.89}$$

$$\frac{\partial f}{\partial u_n} = \Gamma_u = \Phi_2 \Gamma_1 + \Gamma_2 \tag{3.90}$$

$$\frac{\partial f}{\partial d_n} = \Gamma_d = \Phi_2 (\dot{x}^0(d^-) - \dot{x}^0(d^+)) \tag{3.91}$$

$$\frac{\partial f}{\partial T_n} = \Gamma_T = \dot{x}^0(T^-) \tag{3.92}$$

The expression of Γ_d and Γ_T are reduced with the expression of the time derivatives of the state-space vector $x^0(t)$ evaluated at various switching instants. The periodic solution of the state vector is shown in Fig. 3.25 with the derivatives. These expressions will be widely used throughout the thesis to compact the equation expression.

$$\dot{x}^0(d^-) = A_1 x^0(d) + B_1 U = \Phi_1 \left(A_1 x^0(0) + B_1 U \right) \tag{3.93}$$

$$\dot{x}^0(d^+) = A_2 x^0(d) + B_2 U \tag{3.94}$$

$$\dot{x}^0(T^-) = A_2 x^0(0) + B_2 U = \Phi_2 \left(A_2 x^0(d) + B_2 U \right) \tag{3.95}$$

$$\dot{x}^0(T^+) = A_1 x^0(0) + B_1 U \tag{3.96}$$

- The audio susceptibility is

$$T_{ov}(z) = \frac{\hat{v}_{out}(z)}{\hat{v}_{in}(z)} = E \cdot (zI - \Phi_0)^{-1} \Gamma_{u_{2,*}} \tag{3.97}$$

- The output impedance is

$$T_{oi}(z) = \frac{\hat{v}_{out}(z)}{\hat{i}_{load}(z)} = E \cdot (zI - \Phi_0)^{-1} \Gamma_{u_{1,*}} \tag{3.98}$$

- The switching instant d_n to the output voltage transfer function is

$$T_d(z) = \frac{\hat{v}_{out}(z)}{\hat{d}(z)} = E \cdot (zI - \Phi_0)^{-1} \Gamma_d \tag{3.99}$$

- The duty-cycle-to-the output voltage transfer function is

$$T_D(z) = \frac{\hat{v}_{out}(z)}{\hat{D}(z)} = T_d(z) \cdot T \tag{3.100}$$

- The switching instant T_n to the output voltage transfer function is

$$T_T(z) = \frac{\hat{v}_{out}(z)}{\hat{T}(z)} = E \cdot (zI - \Phi_0)^{-1} \Gamma_T \tag{3.101}$$

- The switching frequency-to-the output voltage transfer function is

$$T_f(z) = \frac{\hat{v}_{out}(z)}{\hat{f}(z)} = -T_T(z) \cdot T^2 \tag{3.102}$$

The transfer functions obtained by the sampled-data model linearization are second order transfer functions. The components of the state vector are the voltages across the capacitors. Therefore the system has only real poles. The poles of the sampled-data model are given by the Eigenvalues of the sensitivity matrix, Φ_0 (parameters are listed in Table 3.1):

$$\lambda_1 = 9.1249 \cdot 10^{-12} \approx 0 \tag{3.103}$$

$$\lambda_2 = 0.9231 \tag{3.104}$$

The value of λ_1 is close to zero and the system can be reduced to a first order system with the eigenvalue, λ_2. The transfer functions are expressed in s-domain after the reduction and compared to the linearization of the continuous models. The Bode diagram of the audio susceptibility, the output impedance, the duty-cycle-to-output voltage transfer functions and the switching frequency-to-the output voltage are shown in Fig. 3.26, Fig. 3.27, Fig. 3.28 and Fig. 3.29 respectively.

3.7 Conclusion

This chapter has established the behavior of the SC converter necessary for the design of CMOS implementation. Modeling of losses yields the theoretical maximum efficiency and subsequently the trade-offs to reach in this design. Modeling of dynamics with the list of transfer functions are ready to be used for controller design. It is the purpose of next chapter.

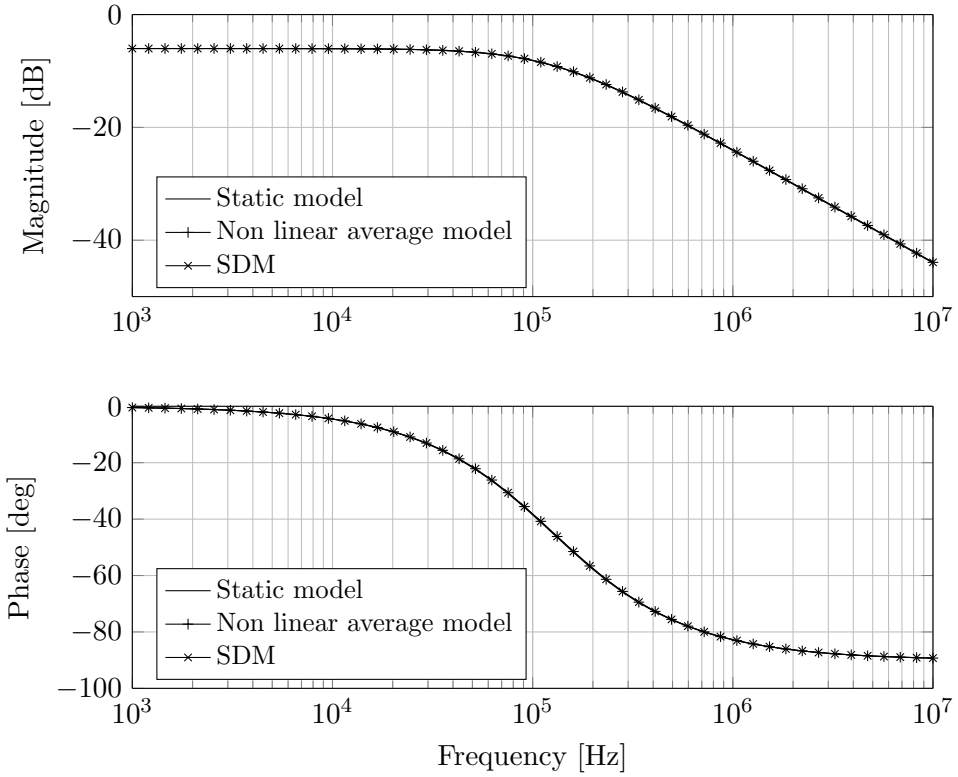


Figure 3.26: Audio susceptibility

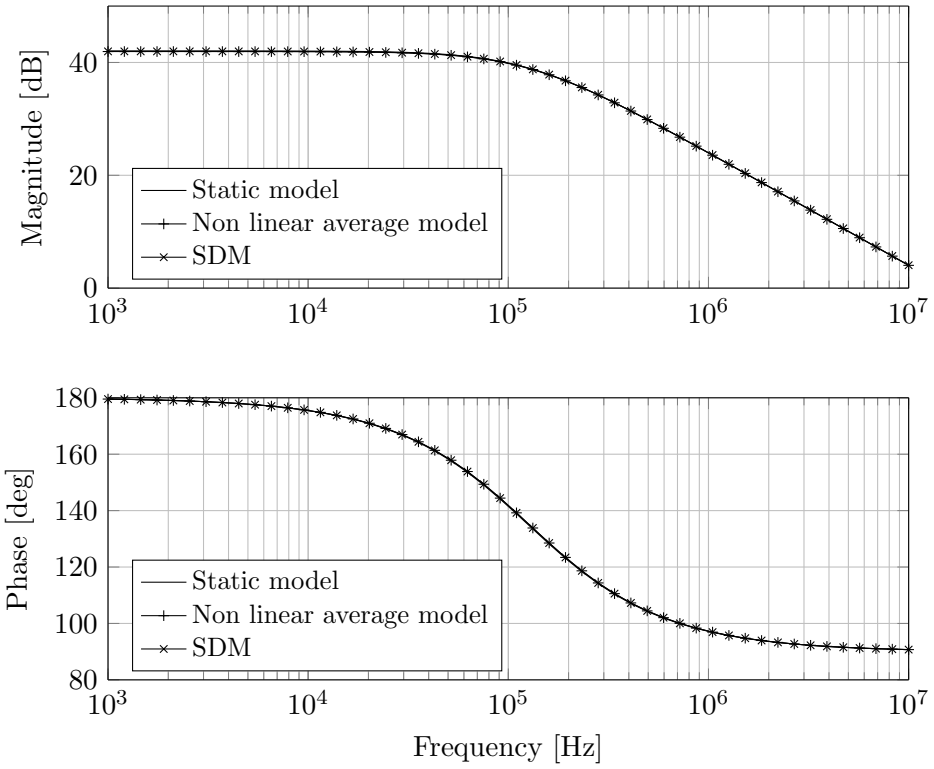


Figure 3.27: Output impedance

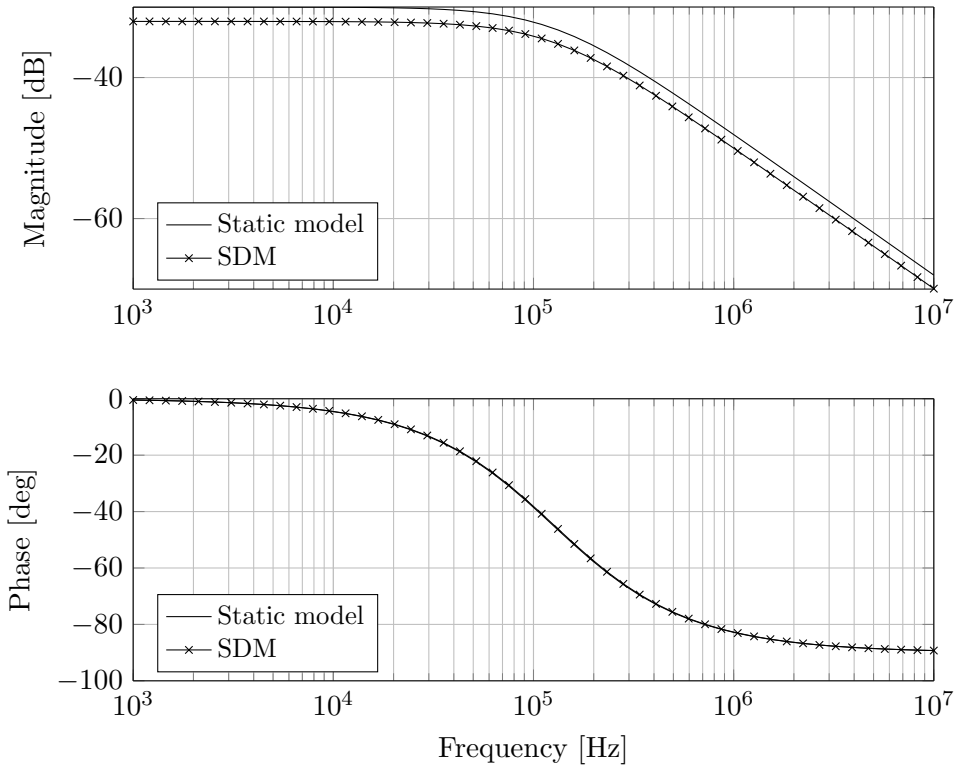


Figure 3.28: Duty-cycle to output transfer function

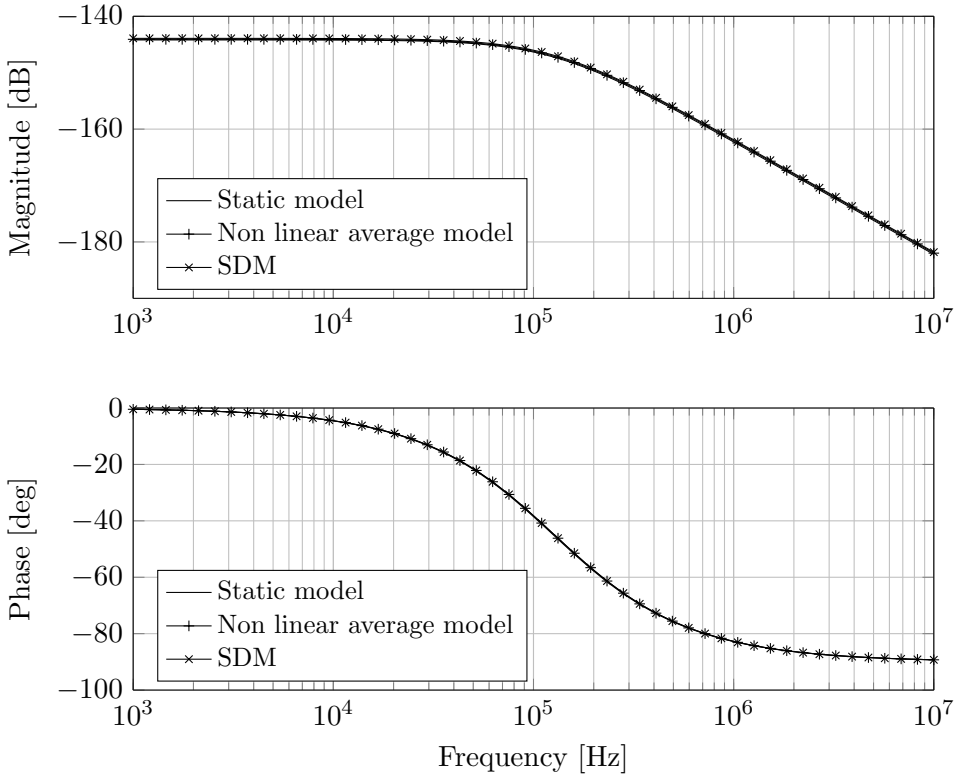


Figure 3.29: Switching frequency to output transfer function

CHAPTER 4

Frequency modulation: controller implementation

On-off control scheme is often the method that comes to mind in SC converter context. The converter operates with a high switching frequency when the output voltage is lower than the reference voltage. Then it is turned-off when the output voltage raises above the reference voltage but this technique is not as good as it seems. First an hysteresis band must be introduced to avoid chartering behavior. This contributes to increase the output voltage ripple. Second a small output capacitor yields fast charging that can increase the chartering behavior. Last but definitely not least, the hopping between OFF and ON mode does not track the optimal efficiency. The efficiency is not a linear law with respect to the switching frequency except in the SSL region. Unfortunately, the ON-mode is in the FSL region, i.e. high switching losses. Despite that, good hysteretic controls have been reported. The single bound approach is the most essential. This technique is illustrated in Section 4.1. Frequency modulation has also been explored with a linear approach. As an example a voltage controlled oscillator is used to tune the switching frequency of the SC converter [54]. Combined with a burst mode, a fast response can be achieved [52]. In [96] a SC converter is cascaded with a low-drop-out regulator. Optimal control law is also proposed through a combination of FM[1] and a pulse width modulation [97]. The design of a linear frequency modulation with a voltage loop is proposed in Section 4.2. The burst mode technique is dismissed because it yields an unexpected and unpredictable behavior. An extra current feedback loop is proposed in Section 4.3. Finally, as suggested in [98] but not deeply analyzed,

[1] Frequency modulation

sliding mode control appears to be a possible alternative. Sliding mode controls are covered in Section 4.4, 4.5 and 4.6.

4.1 Single bound hysteretic control

The single bound hysteretic control or also called the lower bound hysteretic control has been patented by Intel [99]. This control is depicted in Fig. 4.1. The output

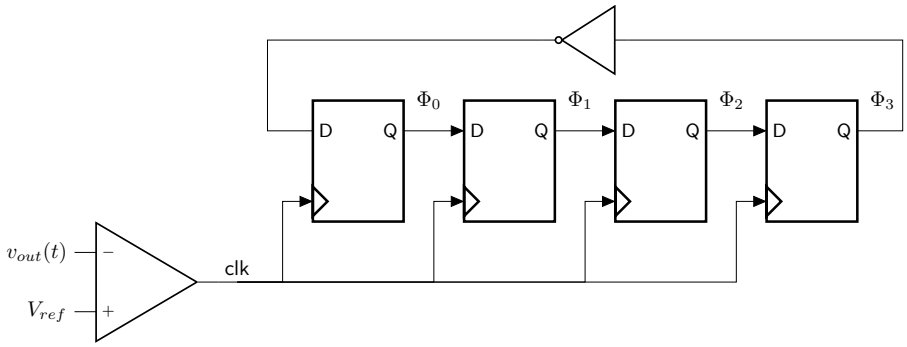


Figure 4.1: Diagram of the single bound hysteretic control [99]

voltage is sensed and compared to a voltage reference through a comparator. The output of the comparator is fed to one or cascaded flip-flop in case of an interleaving scheme. The flip-flops form a circular shift register. The operation is the following: when the output voltage falls bellow the reference voltage, the comparator output toggles. A pulse is delivered to the flip-flops as shown in the time diagram of the Fig. 4.2. The shift register scheme provides the multiphase clocks required for an interleaving operation. Each time a pulse occurs, an amount of charges is delivered by the converter. The output voltage raises and the cycle is repeated to reach the steady state operation. This control has a downside: if the output voltage does not

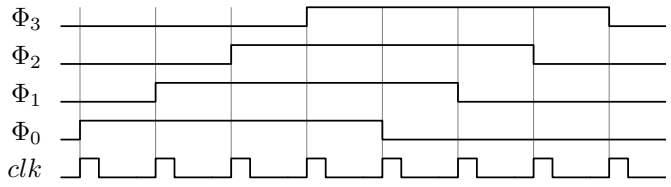


Figure 4.2: Time diagram of the single bound hysteretic control operation

raise above the reference voltage no pulse is delivered anymore and the regulation is lost. This also requires a start-up circuit to initiate the regulation. This point is fixed using a latch-based sense amplifier instead of a simple comparator. The output of the comparator switches at the sampling frequency when the output voltage is under the reference voltage. Thus the converter operates at a factor

of the sampling frequency (depending on the number of flip-flops) and the output voltage raises. This mechanism is well described in [98]. The sampling frequency is chosen much higher than the maximal steady-state switching frequency otherwise subharmonics oscillations may occur. Furthermore the ripple frequency increases with the interleaving factor. The sampling frequency may become very large with interleaved converter. The steady-state criterion proposed in [94] is:

$$T_{delay} < T_{clk} < T_{ripple} \tag{4.1}$$

where T_{delay} is the delay between the output of the comparator and the next charge injection into the output node (i.e. the propagation time), T_{clk} is the sampling period and T_{ripple} is the maximum period of the voltage ripple. The latch sense amplifier saves static power consumption over a simple comparator but the dynamic power consumption can be high in case of high sampling rate.
The single bound control is tested on the 2:1 SC converter. The sampling frequency of the comparator is set to 1.5 GHz. The transient results are shown in Fig. 4.3. The load current is increased to 5 mA at 2 μs and decreased to 1 mA at 4 μs. No voltage drop is visible and the output voltage is regulated to 0.6 V value of he reference voltage. The same simulation is performed with a sampling frequency of 500 MHz. The results are shown in Fig. 4.4. Subharmonic oscillations occur after the load transient and disappear when the load current returns to the nominal value.
The single bound hysteretic control has been successfully implemented in [47,57,98]. However during a load transient, the switching frequency of the converter is very high and the switching losses are significant when the recovery time is important (around 200 ns in [47]).

4.2 Linear frequency modulation with a voltage loop

The linear frequency modulation with a voltage loop is depicted in Fig. 4.5. This loop comprises a SC converter power stage, a voltage-controlled oscillator (VCO) and a controller. The regulation principle is the following: the output voltage, V_{out}, is sensed and subtracted to the reference voltage, V_{ref}, forming an error signal, V_{err}. This signal is provided to a compensator which determines the value of the control voltage, V_{ctrl}. The control voltage is transformed into a switching frequency through the VCO and fed to the power stage. The design of the controller required the frequency response of the plant formed by the VCO and the power stage. The VCO is a voltage-to-time converter and the switching behavior must be linearized. The transfer characteristic of a linear VCO is shown in Fig. 4.6 and its expression

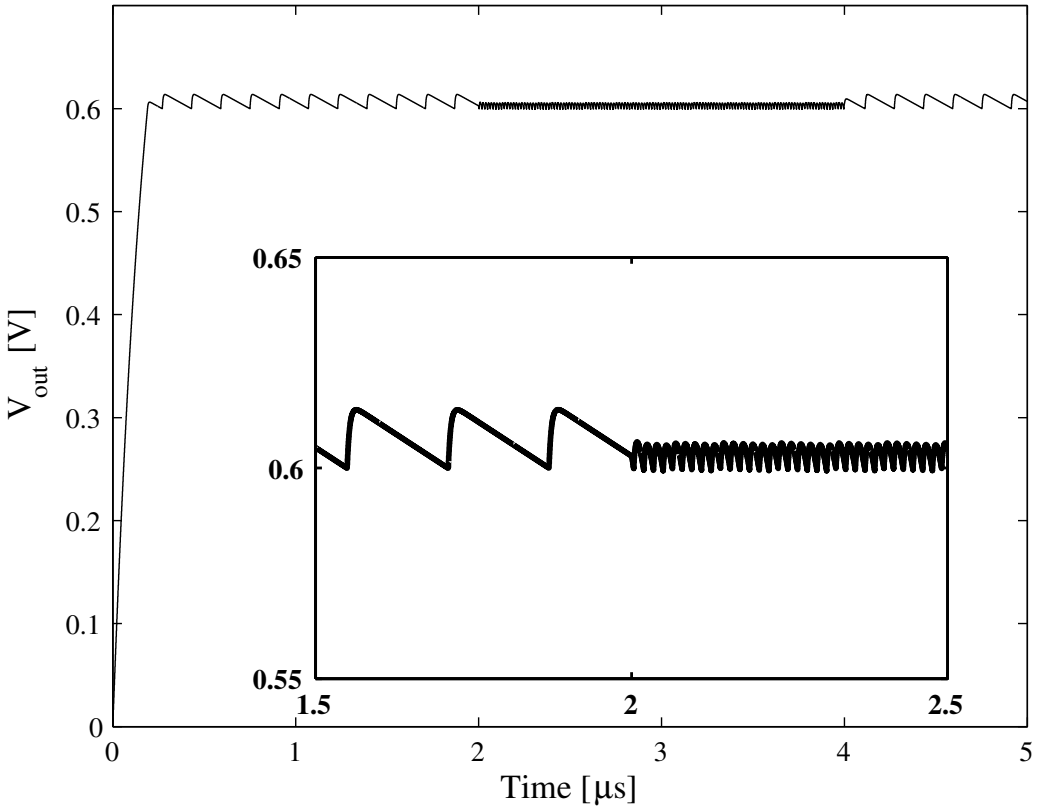


Figure 4.3: Transient simulation results of the output voltage under single bound control

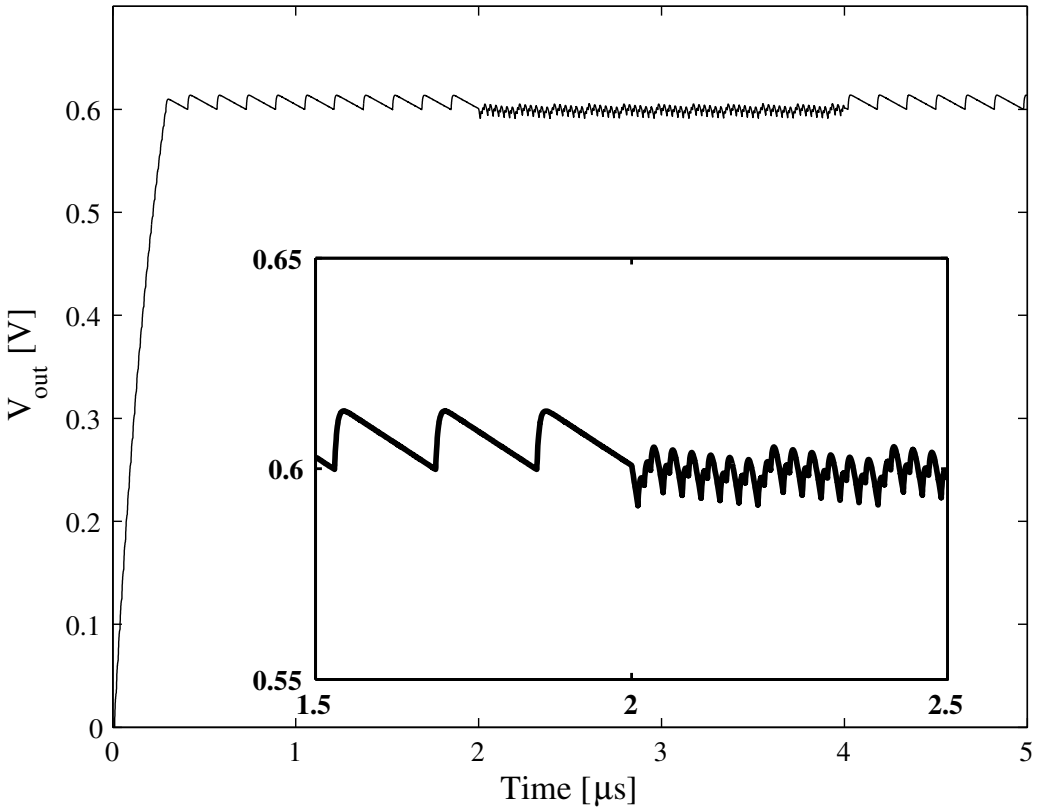


Figure 4.4: Transient simulation results of the output voltage under single bound control with subharmonic oscillations

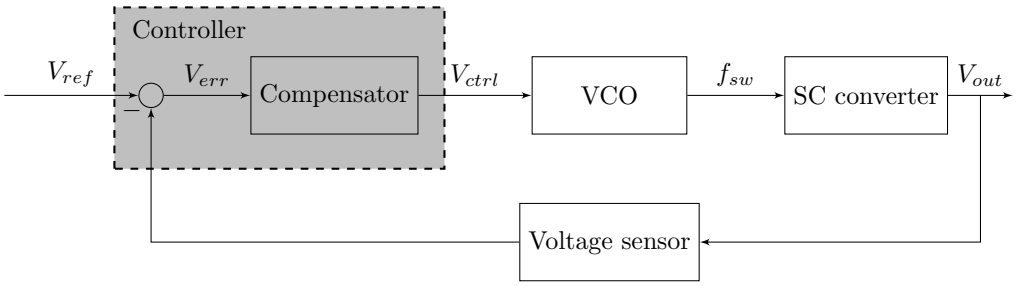


Figure 4.5: Diagram of a linear frequency modulation with a voltage loop

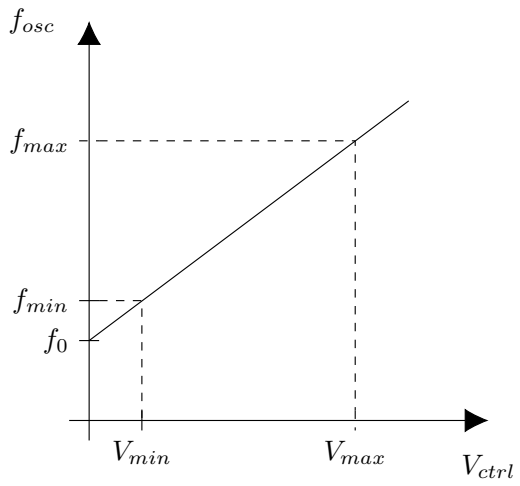


Figure 4.6: Transfer characteristic of a linear VCO

is:

$$f_{osc}(t) = K_{vco} \cdot V_{ctrl}(t) + f_0 \tag{4.2}$$

The output frequency, f_{osc}, is proportional to the control voltage, V_{ctrl}. The gain of the VCO, K_{vco}, represents the sensitivity of the oscillation frequency to a voltage change and f_0 corresponds to the zero voltage oscillation frequency. The frequency range of the VCO, $\Delta_f = [f_{min}, f_{max}]$, is chosen according to the frequency excursion of the power stage. The control voltage range $\Delta_V = [V_{min}, V_{max}]$, depends on the maximal excursion of the controller. Thus the gain K_{vco} can be set to $\dfrac{\Delta_f}{\Delta_V}$ and $f_0 = f_{min} - K_{vco} \cdot V_{min}$ as shown in Fig. 4.6. The expression in the frequency domain of (4.2) is:

$$\hat{f}_{osc}(s) = K_{vco} \cdot \hat{v}_{ctrl}(s) \tag{4.3}$$

hence, the transfer function of V_{ctrl}-to-f_{osc} is

$$\frac{\hat{f}_{osc}(s)}{\hat{v}_{ctrl}(s)} = K_{vco} \tag{4.4}$$

The power stage linearization is performed using the sampled-data model in Section 3.6.2. The linearization requires the computation of an operating point (fixed point). The operating point is usually the targeted output voltage and we can write:

$$Ex^0\left(0\right) - V_{target} = 0 \tag{4.5}$$

The fixed-point solution $\left(x^0(0), U, (d, T)', \right)$ is determined by solving the set of equation (3.44) and (4.5). The so-called Trust-Region Dogleg algorithm [100] gives

$$x^0(0) = \begin{pmatrix} 0.6022 & 0.6 \end{pmatrix}' \tag{4.6}$$

$$d = 3.1824 \cdot 10^{-8} \tag{4.7}$$

$$T = 6.3649 \cdot 10^{-8} \tag{4.8}$$

Then the system is linearized around the fixed point to build the transfer functions of the plant. The switching frequency-to-the output voltage transfer function exhibits one pole yielding a transfer function of the plant as:

$$H(s) = \frac{G_0}{1 + \tau_0 s} \tag{4.9}$$

Where G_0 is the static gain depending on K_{vco} and τ_0, the time constant of the plant. The pole is $1/\tau_0$ and τ_0 is equal to $R_{out} \cdot C_{load}$ where R_{out} is the static output resistance and C_{load}, the output capacitor.
The first order behavior of the plant calls for a proportional-integral (PI) compensator. The transfer function is:

$$C(s) = K_p \cdot \left(1 + \frac{1}{T_i s}\right) \tag{4.10}$$

K_p is the proportional gain and T_i is the time integral constant. Then the open-loop transfer function, $L_o(s)$, is established:

$$L_o(s) = C(s) \cdot H(s) = \left[\frac{K_p\left(1 + T_i s\right)}{T_i s}\right] \cdot \left[\frac{G_0}{1 + \tau_0 s}\right] \tag{4.11}$$

as well as the closed-loop $L_c(s)$:

$$L_c(s) = \frac{1 + T_i s}{1 + T_i\left(1 + \frac{1}{G_0 \cdot K_p}\right) s + \left(\frac{\tau_0 \cdot T_i}{G_0 \cdot K_p}\right) s^2} \tag{4.12}$$

In case of a closed-loop first order behavior, the denominator of the plant is simplified by the numerator of the compensator in (4.11). Let $1 + T_i s = 1 + \tau_0 s$, the open loop is now:

$$L_o(s) = \frac{K_p \cdot G_0}{T_i \cdot s} \tag{4.13}$$

and the associated closed-loop, $L_c(s)$ is:

$$L_c(s) = \frac{1}{1 + \dfrac{T_i}{K_p \cdot G_0} s} = \frac{1}{1 + \tau_c s} \tag{4.14}$$

Where $\tau_c = \dfrac{T_i}{K_p \cdot G_0}$ is the time-constant giving the closed loop behavior. The controller parameters are then :

$$K_p = \frac{\tau_0}{G_0 \cdot \tau_c} \tag{4.15}$$

$$T_i = \tau_0 \tag{4.16}$$

The integration constant, T_i, is equal to the time-constant of the system, τ_0. The gain, K_p, is chosen regarding the desired closed-loop time-constant, τ_c.
In case of a second order closed-loop behavior, (4.12) is expressed with the undamped angular frequency, ω_0 and the damping factor ζ_0.

$$L_c(s) = \frac{1 + T_i s}{1 + \dfrac{2 \cdot \zeta_0 \cdot s}{\omega_0} + \dfrac{s^2}{\omega_0^2}} \tag{4.17}$$

The compensator set two poles in the closed-loop. The identification of the denominators in (4.12) and (4.17) gives

$$\omega_0^2 = \frac{G_0 \cdot K_p}{\tau \cdot T_i} \tag{4.18}$$

$$\frac{2 \cdot \zeta_0}{\omega_0} = T_i \cdot \left(1 + \frac{1}{G_0 \cdot K_p}\right) \tag{4.19}$$

The undamped angular frequency, ω_0, sets the time response while the damping ratio, ζ_0, dictates the overshoot in the case of a step response. Finally the PI[2] parameters are expressed with G_0 and τ_0 and the feedback requirements, ω_0 and ζ_0:

$$T_i = \frac{2 \cdot \zeta_0 \cdot \omega_0 \cdot \tau_0 - 1}{\omega_0^2 \cdot \tau_0} \tag{4.20}$$

$$K_p = \frac{\omega_0^2 \cdot T_i \cdot \tau_0}{G_0} \tag{4.21}$$

[2]Proportional-integral

The action derived from (4.20) and (4.21) has to be positive. It implies that $\zeta_0 \cdot \omega_0 \geq \frac{1}{2 \cdot \tau_0}$. As a starting point, ω_0 can be chosen equal to the inverse of the plant time-constant, τ_0. The dynamic speed is increased with ω_0 until the system saturates. Regarding ζ_0, a small overshoot is achieved with $\zeta_0 = 0.7$ and no overshoot comes with $\zeta_0 \geq 0.9$.

A voltage loop control is designed for the 2:1 SC converter as an illustrative example. The reference voltage is $V_{ref} = 0.6\ V$ and the nominal load current is $I_{load} = 5\ mA$. The parameter of the VCO are $K_{vco} = 100\ {}^{MHz}/_{V}$ and $f_0 = 1\ MHz$. Then the large signal sampled-data dynamics is evaluated and the fixed point is $x^0(0) = \begin{bmatrix} 0.6022 & 0.6 \end{bmatrix}^T$. The switching period is $T = 63.64\ ns$ ($f_{sw} = 15.71\ MHz$). Finally the sampled-data dynamics is linearized around the fixed-point and the various transfer functions are computed in z-domain and expressed in s-domain. The transfer function of the plant including the VCO is thus:

$$H(s) = \frac{G_0}{1 + \tau_0 s} = \frac{2.57}{7.95 \cdot 10^{-7} s + 1} \tag{4.22}$$

A second order behavior is set with $\zeta = 0.6$ and $\omega_0 = 1/\tau_0 = 1.25 \cdot 10^6\ {}^{rad}/_{s}$. Thus $K_p = 0.078$ and $T_i = 159$ ns. The Bode diagram in Fig. 4.7 shows the plant, the controller and the open-loop frequency response. The phase margin is 61 ° ensuring a stable closed-loop. The controller is implemented in *Matlab/Simulink* and the response is simulated for the PWL model, the linear model and the non linear averaged model. Fig. 4.8 and Fig. 4.9 depict a negative and a positive load transient for a load step of 1 mA and 5 mA respectively. In Fig. 4.8, the linear and the non linear model follow the PWL model. However mismatch appears in the linear model in case of a larger load transient. The difference comes from the moving pole of the converter lost during linearization. As a consequence the linear model can only be used to derive the small-signal behavior or to evaluate the response for reasonably small perturbations.

The undershoots occurring in Fig. 4.8 and Fig. 4.9 are an important specification for a regulated power supply. The undershoot can degrade or alter the behavior of the load. The small-signal output impedance must be as low as possible to guaranty satisfying undershoot values. The closed-loop output impedance is derived with:

$$Z_{closed-loop} = \frac{Z_{open-loop}}{1 + L_o} \tag{4.23}$$

The bandwidth of the controller and the output capacitor value can be increased to lower the output impedance. A first controller with $\omega_0 = 1/\tau_0$ and a second one with $\omega_0 = 10/\tau_0$ are evaluated. The Bode diagram of the open-loop output impedance, the two closed-loop output impedances and the output capacitor impedance are given in Fig. 4.10. The fastest controller shows the lowest output impedance. This

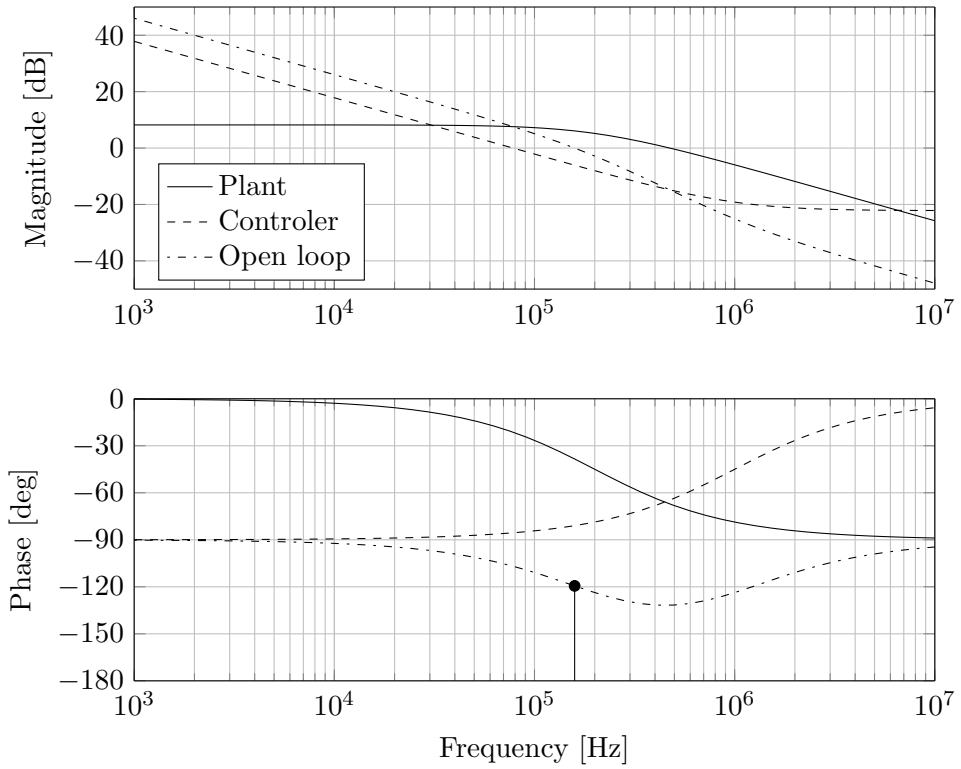


Figure 4.7: Bode diagram of the voltage loop control of the 2:1 ratio SC converter with target of a second order behavior

improvement brings more benefits to save area than to increase the output capacitor. However high bandwidth controller increases the constraint on the compensator such as the power consumption or the saturation.

The robustness and the stability of switched-mode converter are key points. As previously mentioned, the power stage of a SC converter under frequency modulation has a pole depending on the instantaneous switching frequency. This non linearity causes discrepancy between the real response and the predicated behavior during the compensator design. The controller is indeed designed around an operating point. Therefore, outside this operating point the behavior and the stability can be altered. The switching frequency depends on the load current and the output voltage. The open-loop is computed for various reference voltages (100 mV to 800 mV) and for the nominal load current value, $I_{nom} = 5\ mA$ and a lower current value, $I_{low} = 1\ mA$. The phase margin of the loop is then evaluated and the results are shown in Fig. 4.11. When the switching frequency increases the pole of the plant moves to higher frequency and the system moves toward a first order system. On the contrary, when the switching frequency decreases, the phase margin decreases. The phase margin reaches a minimum of 20 ° at the lowest load current. The system

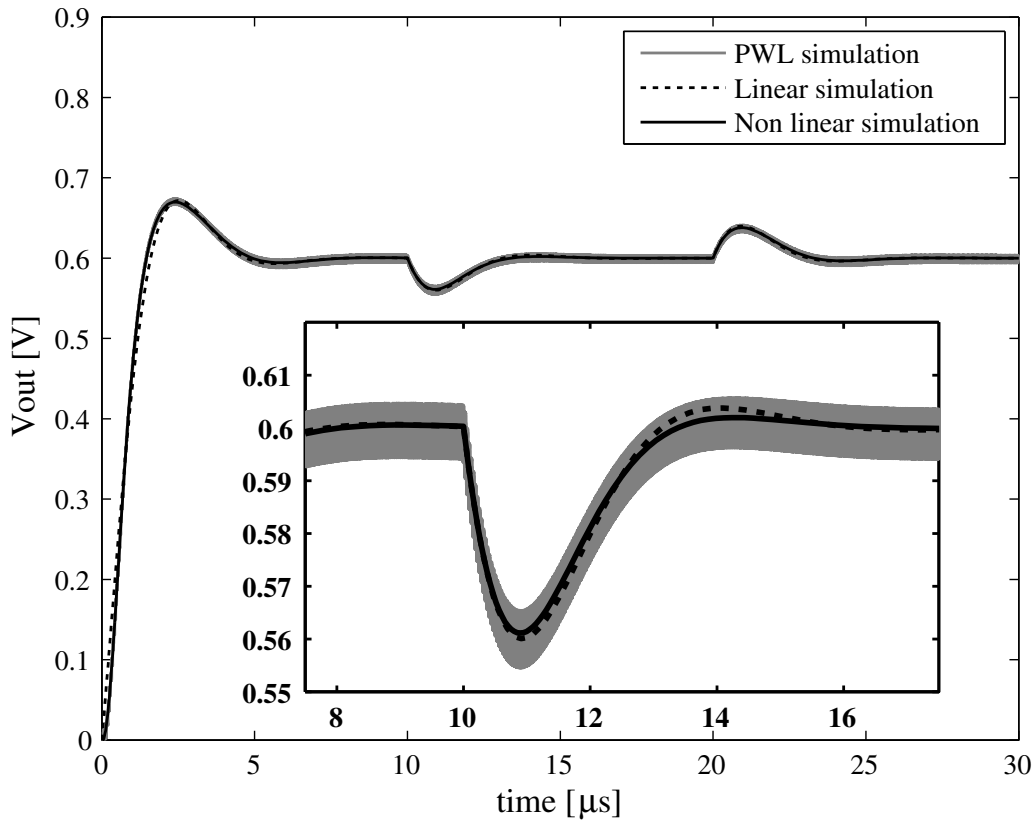


Figure 4.8: Results for a small load transient (1 mA)

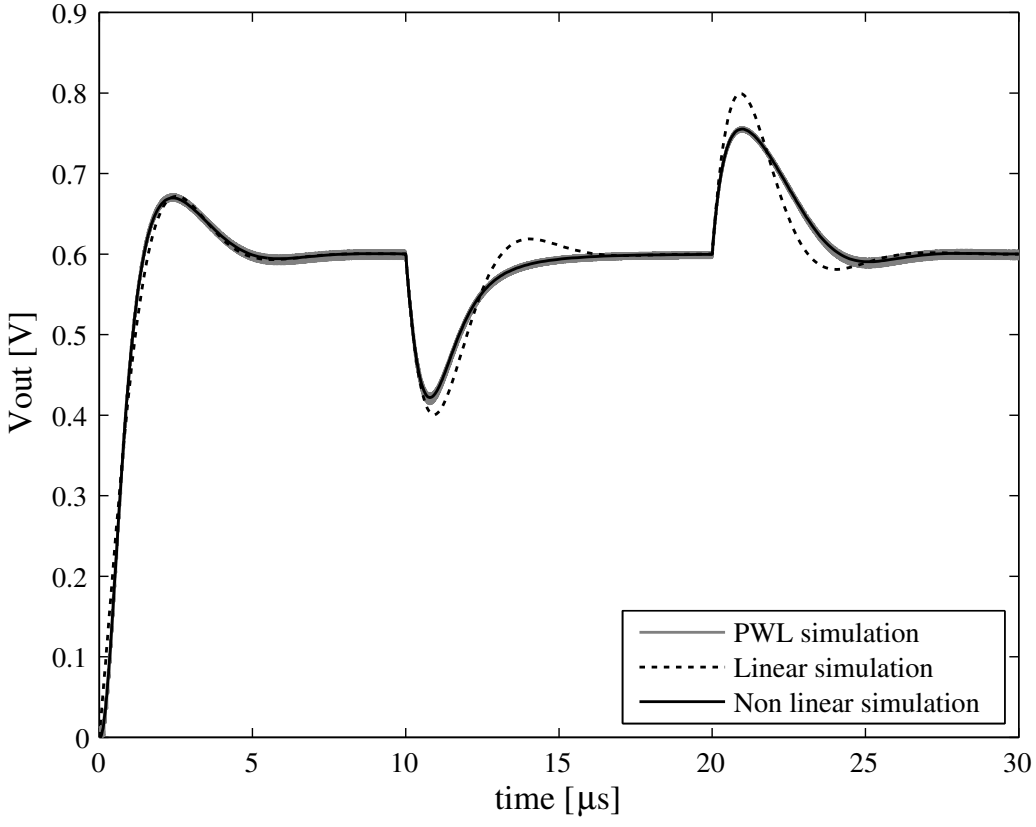


Figure 4.9: Results for a large load transient (5 mA)

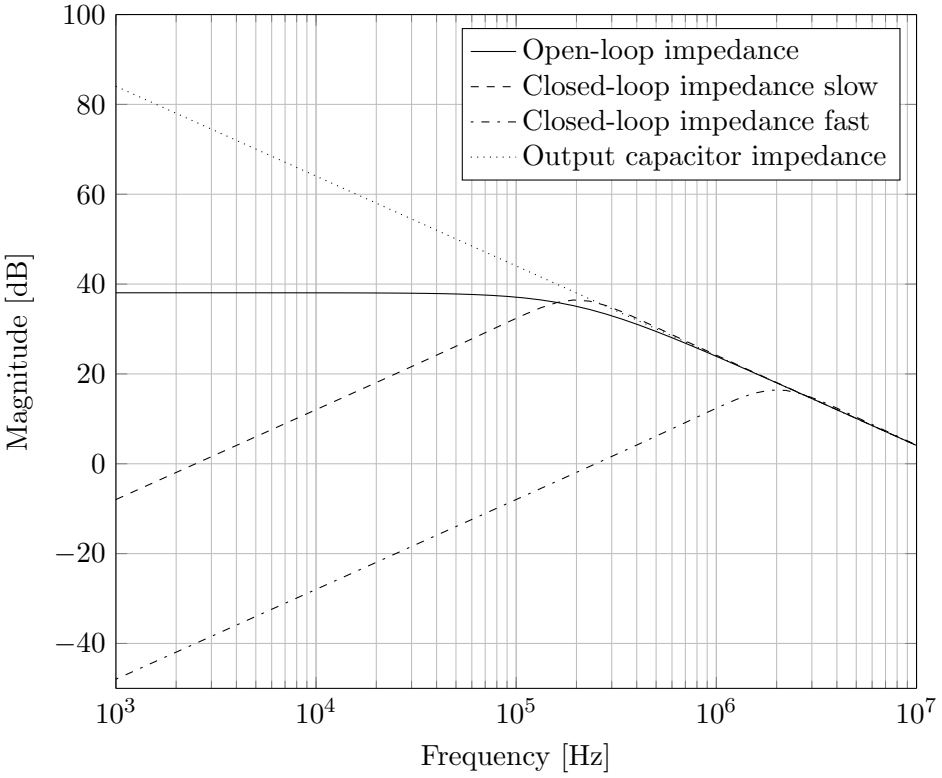


Figure 4.10: Load transient simulation results

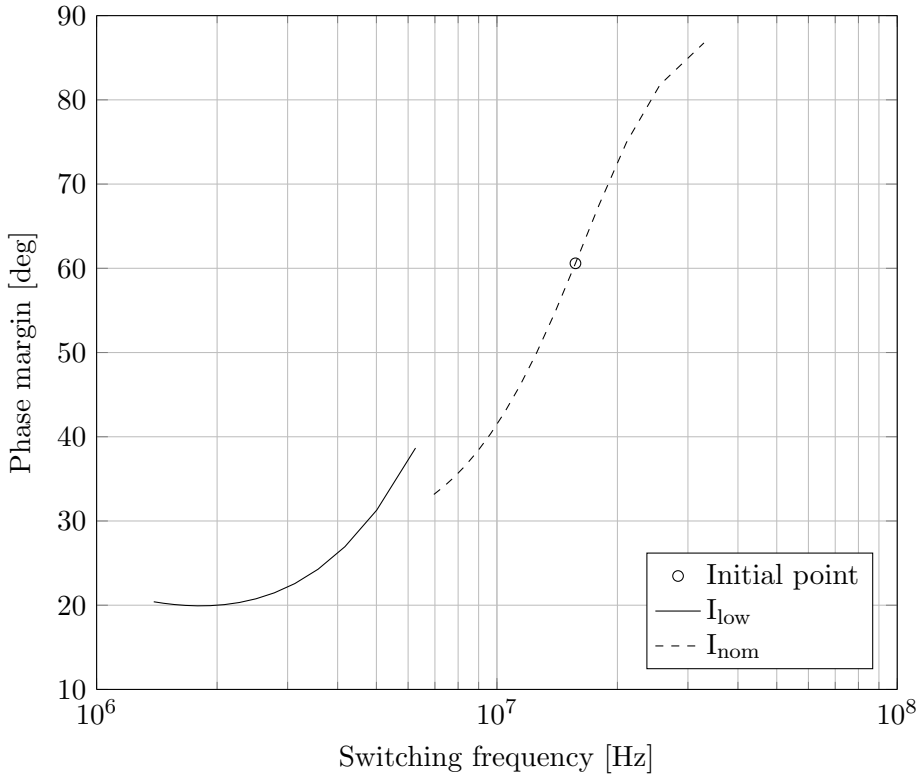


Figure 4.11: Phase margin as a function of the switching frequency

still remains stable but the transient performances are degraded. The system must designed against a minimal load current to ensure minimum stability margin.
Sampled-data modeling has been extensively used to offer a comprehensive stability analysis against an averaged approach. Subharmonic oscillations and other bifurcations can occur. These bifurcations can be predicted with sampled-data model where the averaged approach fails [86]. This is primarily because the sampled-data model yields a periodic solution depending on the switching instants while the average model has a continuous solution. The stability analysis requires to build the closed-loop model using sampled-data modeling. The stability is checked from the Eigenvalues of the sensitivity matrix. The system is asymptotically stable if all the Eigenvalues are inside the unit circle [101].
The sampled-data modeling approach of a frequency-modulation control is applied to the SC converter. The operation of the SC converter is considered within a cycle $[t_n, t_n + T_n]$. The duration of the nth-cycle is T_n which is the instantaneous switching period of the converter. The instantaneous switching frequency is then $f_n = 1/T_n$. We assume that the inputs are constant over a cycle and perturbations are introduced at the beginning of a cycle. Due to the discrete operation, the switching instants in the coming cycle are considered to be determined at $t = t_n$, the beginning of the cycle. The state-space representation of each states of the converter including the controller is:

$$S_1 : \begin{cases} \dot{x} = A_1 x + B_1 u \\ v_{err} = Cx + Du \quad \text{for } t \in [t_n, t_n + d_n] \\ v_{out} = Ex \end{cases} \tag{4.24}$$

$$S_2 : \begin{cases} \dot{x} = A_2 x + B_2 u \\ v_{err} = Cx + Du \quad \text{for } t \in [t_n + d_n, t_n + T_n] \\ v_{out} = Ex \end{cases} \tag{4.25}$$

Where v_{err} is the error signal driving the VCO. During a cycle, the VCO delivers a square wave, with a 50% duty cycle. As a consequence the switching instant d_n is the half of the switching period T_n. The VCO continuous time-domain model is

$$f_{sw}(t) = K_{vco} \cdot V_{err}(t) + f_0 \tag{4.26}$$

Sampling (4.26) at the beginning of each cycle yields the discrete time-domain operation of the VCO

$$f_{sw}(t_n) = K_{vco} \cdot v_{err}(t_n) + f_0 \tag{4.27}$$

$$f_n = K_{vco} \cdot v_{err}(t_n) + f_0 \tag{4.28}$$

The switching instants d_n and T_n are then determined by the following expressions :

$$T_n = \frac{1}{K_{vco} \cdot v_{err}(t_n) + f_0} \tag{4.29}$$

$$d_n = \frac{0.5}{K_{vco} \cdot v_{err}(t_n) + f_0} \tag{4.30}$$

Reciprocally the error signal, v_{err} at the beginning of the cycle can be expressed as a function of T_n

$$v_{err}(T_n) = h(T_n) = \frac{1}{T_n \cdot K_{vco}} - \frac{f_0}{K_{vco}} \tag{4.31}$$

and we have

$$V_{err}(t_n) = Cx(t_n) + Du_n \tag{4.32}$$

We can establish the constraint function that determine the switching instant from (4.31) and (4.32)

$$g\left(x_n, u_n, \tau_n\right) = Cx_n + Du_n - h(T_n) = 0 \tag{4.33}$$

and the sampled-data dynamics is

$$x_{n+1} = f\left(x_n, u_n, \tau_n\right) \tag{4.34}$$

$$= \Phi x_n + \Gamma u_n \tag{4.35}$$

$$v_{out_n} = Ex_n \tag{4.36}$$

The dynamics is constrained by (4.33) and the steady-state operation of the SC converter with FM control is reached when the averaged output voltage value is equal to the reference voltage. The solution is a periodic orbit and the fixed-point in the sampled-data dynamics is

$$x^0(0) = f(x^0(0), U, \tau) \tag{4.37}$$

$$g(x^0(0), U, \tau) = 0 \tag{4.38}$$

Finally the fixed point solution, $\left(x^0(0), U, (d, T)'\right)$ is obtained solving the set of equations (4.37) and (4.38). The steady-state duty cycle is d/T and the steady-state switching frequency is $f_{sw} = 1/T$. The large-signal sampled-data model dynamics under closed-loop constraint can be linearized around the fixed-point solution to give the small-signal behavior of the closed-loop system. The linearizion of (4.35) and (4.33) gives the linear sampled-data dynamics

$$\hat{x}_{n+1} \approx \frac{\partial f}{\partial x_n}\hat{x}_n + \frac{\partial f}{\partial u_n}\hat{u}_n + \frac{\partial f}{\partial \tau_n}\hat{\tau}_n \tag{4.39}$$

$$0 \approx \frac{\partial g}{\partial x_n}\hat{x}_n + \frac{\partial g}{\partial u_n}\hat{u}_n + \frac{\partial g}{\partial \tau_n}\hat{\tau}_n \tag{4.40}$$

from (4.40) it comes:

$$\hat{\tau}_n \approx \left(-\frac{\partial g}{\partial \tau_n}\right)^{-1}\left[\frac{\partial g}{\partial x_n}\hat{x}_n + \frac{\partial g}{\partial u_n}\hat{u}_n\right] \tag{4.41}$$

Injecting (4.41) into (4.39) gives

$$\begin{aligned}\hat{x}_{n+1} &\approx \Phi_0\hat{x}_n + \Gamma_u\hat{u}_n \\ \hat{v}_{out_n} &= E\hat{x}_n\end{aligned} \tag{4.42}$$

with

$$\Phi_0 = \frac{\partial f}{\partial x_n} - \frac{\partial f}{\partial \tau_n}\left(\frac{\partial g}{\partial \tau_n}\right)^{-1}\frac{\partial g}{\partial x_n} \tag{4.43}$$

$$\Gamma_u = \frac{\partial f}{\partial u_n} - \frac{\partial f}{\partial \tau_n}\left(\frac{\partial g}{\partial \tau_n}\right)^{-1}\frac{\partial g}{\partial u_n} \tag{4.44}$$

$$\frac{\partial f}{\partial x_n} = \Phi_2\Phi_1 \tag{4.45}$$

$$\frac{\partial f}{\partial u_n} = \Phi_2\Gamma_1 + \Phi_1 \tag{4.46}$$

$$\frac{\partial f}{\partial \tau_n} = \begin{bmatrix} \Phi_2(\dot{x}^0(d^-) - \dot{x}^0(d^+)) & \dot{x}^0(T^-) \end{bmatrix} \tag{4.47}$$

$$\frac{\partial g}{\partial x_n} = C\Phi_2\Phi_1 \tag{4.48}$$

$$\frac{\partial g}{\partial u_n} = C\left(\Phi_2\Gamma_1 + \Phi_1\right) + D \tag{4.49}$$

$$\frac{\partial g}{\partial \tau_n} = \begin{bmatrix} C\Phi_2\left(\dot{x}^0(d^-) - \dot{x}^0(d^+)\right) & C\dot{x}^0(T^-) - \dot{h} \end{bmatrix} \tag{4.50}$$

The closed-loop model is determined for the frequency modulation with a PI controller. The ideal controller can be included in the state-space representation with the following relation:

$$\frac{\hat{v}_{err}(s)}{\hat{v}_{ref}(s) - \hat{v}_{out}(s)} = \frac{\hat{v}_{err}(s)}{\hat{\epsilon}(s)} = K_p(1 + \frac{1}{T_i s}) \tag{4.51}$$

However some practical mathematical problems occur when the fixed point is solved. The integral term is infinite except in steady-state. Since the algorithm tries to find the steady-state solution by iteration the state of the controller cannot be determined a priori. The integral term must have a finite value to let find solution. This is always the case in practice because the controller saturates. One way

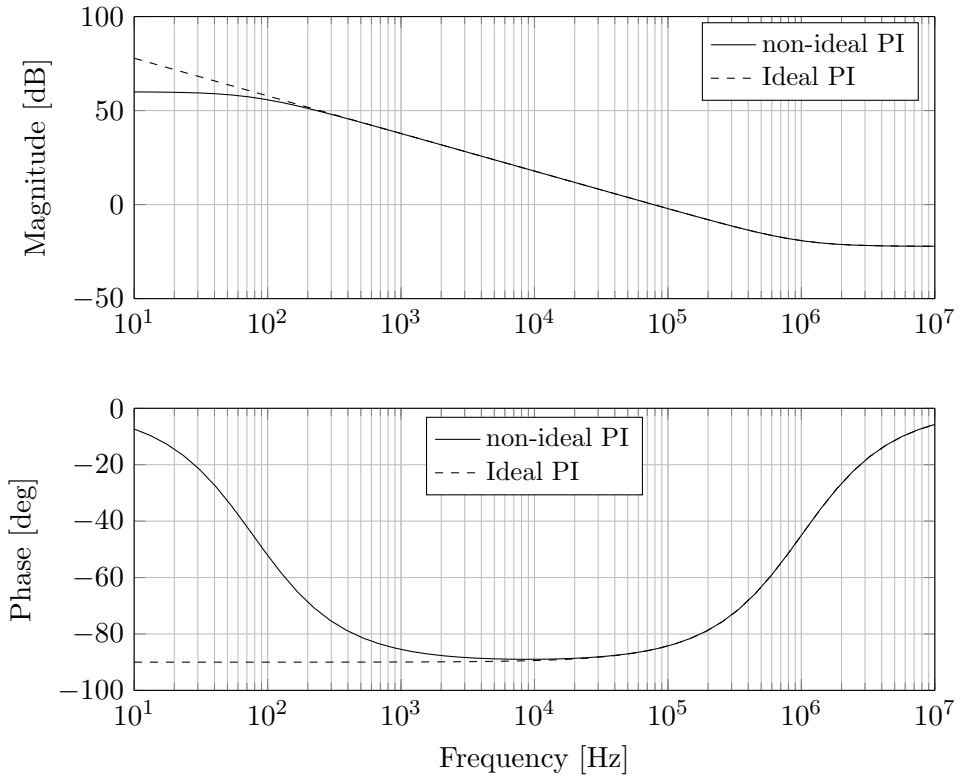


Figure 4.12: Bode diagram comparison of the ideal and the non-ideal controller

to proceed is to replace the pole at the origin by a non-zero pole. The zero-pole-gain form is then:

$$\frac{\hat{v}_{err}(s)}{\hat{\epsilon}(s)} = k_0 \cdot \frac{s + z_0}{s + p_0} \tag{4.52}$$

For the ideal PI control, we have $k_0 = \dfrac{K_p}{T_i}$, $z_0 = \dfrac{1}{T_i}$ and $p_0 = 0$. We introduce a value limiting the integral value, A_0 so that

$$k_0 = \frac{A_0 K_p}{1 + A_0 + K_p} \tag{4.53}$$

$$z_0 = \frac{1}{T_i} \tag{4.54}$$

$$p_0 = \frac{K_p}{T_i} \frac{1}{1 + A_0 + K_p} \tag{4.55}$$

The value of A_0 is set to 1000, K_p and T_i have the value previously calculated. The ideal and the non-ideal PI controllers are compared in Fig. 4.12. The DC gain is limited to A_0, 60 dB in the Bode diagram. The higher gain the lower the static error. The state-space for the 2:1 SC converter with the non-ideal PI controller

where $\tau_1 = R_{on}C_{fly}$ and $\tau_2 = R_{on}C_{load}$ and x_c the state of the controller, is:

$$A_1 = \begin{bmatrix} \frac{-1}{2\tau_1} & \frac{-1}{2\tau_1} & 0 \\ \frac{-1}{2\tau_2} & \frac{-1}{2\tau_2} & 0 \\ 0 & p_0 - z_0 & -p_0 \end{bmatrix}, \; A_2 = \begin{bmatrix} \frac{-1}{2\tau_1} & \frac{1}{2\tau_1} & 0 \\ \frac{1}{2\tau_2} & \frac{-1}{2\tau_2} & 0 \\ 0 & p_0 - z_0 & -p_0 \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 0 & \frac{1}{\tau_1} & 0 \\ \frac{-1}{C_{load}} & \frac{1}{2\tau_2} & 0 \\ 0 & 0 & z_0 - p_0 \end{bmatrix}, \; B_2 = \begin{bmatrix} 0 & 0 & 0 \\ \frac{-1}{C_{load}} & 0 & 0 \\ 0 & 0 & z_0 - p_0 \end{bmatrix}$$

$$E = \begin{bmatrix} 0 & 1 & 0 \end{bmatrix}, \; C = \begin{bmatrix} 0 & -k & k \end{bmatrix}, \; D = \begin{bmatrix} 0 & 0 & k \end{bmatrix}$$

$$U = \begin{bmatrix} I_{load} \\ V_{in} \\ V_{ref} \end{bmatrix}, \; x = \begin{bmatrix} v_{C_{fly}} \\ v_{C_{load}} \\ x_c \end{bmatrix}, \; \tau = \begin{bmatrix} d \\ T \end{bmatrix}$$

The determinant of the matrices A_i are:

$$det[A_1] = \frac{-1}{2\tau_1} \cdot \frac{-1}{2\tau_1} \cdot -p_0 - \frac{-1}{2\tau_1} \cdot \frac{-1}{2\tau_1} \cdot -p_0 = 0 \tag{4.56}$$

$$det[A_2] = \frac{-1}{2\tau_1} \cdot \frac{-1}{2\tau_1} \cdot -p_0 - \frac{1}{2\tau_1} \cdot \frac{1}{2\tau_1} \cdot -p_0 = 0 \tag{4.57}$$

The matrices are singular and the Jordan form decomposition may be used. The fixed-point solution $\left(x^0(0), U, (d, T)', \right)$ is determined solving the set of equation (4.37) and (4.38). The Trust-Region Dogleg algorithm gives

$$x^0(0) = \begin{pmatrix} 0.5960 & 0.5939 & 1.8512 \end{pmatrix}' \tag{4.58}$$

$$d = 3.2318 \cdot 10^{-8} \tag{4.59}$$

$$T = 6.4636 \cdot 10^{-8} \tag{4.60}$$

The system is linearized around the fixed-point solution and compared to the linear model with respect to the transfer functions and the transient simulations. Fig. 4.13 shows the load transient simulation. The closed-loop from the sampled-data model takes into account the ripple of the output voltage since the output voltage is sampled at the beginning of each cycle. On the contrary, the linear model is insensitive to the ripple and the output voltage value is averaged. Both models are also impacted by the non-linear behavior of the converter lost during the linearization step. The small-signal closed-loops are compared in Fig. 4.14 and the models are in good agreement. The stability is checked evaluating the modules of the Eigenvalues of

the sensitivity matrix Φ_0. The system comprises a compensator tuned for a closed-loop second order behavior. The closed-loop sampled-data model has three state variables hence three Eigenvalues:

$$\begin{aligned}\lambda_1 &= 7.5253 \cdot 10^{-8} \\ \lambda_2 &= 0.9508 + 0.0605i \\ \lambda_3 &= 0.9508 - 0.0605i\end{aligned}$$

The system is reduced to a second order system because λ_1 is close to zero. The eigenvalues λ_2 and λ_3 are conjugate and inside the unit circle. The system is thus asymptotically stable. We can analyze the robustness of the system using the unit circle and the margin stability definition. The unit circle with constant damping factors lines and natural frequency lines is depicted in Fig. 4.15. For illustration purpose, two areas are defined: one area delimits the location where the poles have a higher angular frequency than $0.2\pi/T$ and an other location where the poles have a damping factor above 0.6. The intersection of the two surfaces is the dark gray area where the design point will fulfill both specifications. Sensitivity analysis to the reference voltage is performed first and the results are presented in Fig. 4.16. The lowest value of V_{ref} gives an eigenvalue with the fastest frequency but with also the lowest damping factor. When the voltage reference increases the Eigenvalues move toward low frequencies and the real axis. The system has a first order behavior for $V_{ref} = 0.75\ V$ and $V_{ref} = 0.8\ V$. Therefore the stability is improved but the system is slower. Then a similar analysis is performed against the load current variation in Fig. 4.17. As well as for the voltage reference variation, the lowest load current yields a fast eigenvalue with a low damping factor. This is the worst case in term of stability margin while the highest current value gives a first order system. The reactivity and the stability cannot be achieved at the same time for different operating points. If the controller is designed for the worst case (lowest current and lowest reference voltage values), the controller will always fulfill the damping factor requirement but the bandwidth will always be small. Finally the robustness is analyzed for controller parameter variations of $\pm 20\%$ in Fig. 4.18. The bandwidth of the system is maintained when the parameter values vary in the same way. The worst case of damping factor is determined when $\Delta T_i = -20\%$ while K_p impact the Eigenvalue frequency.

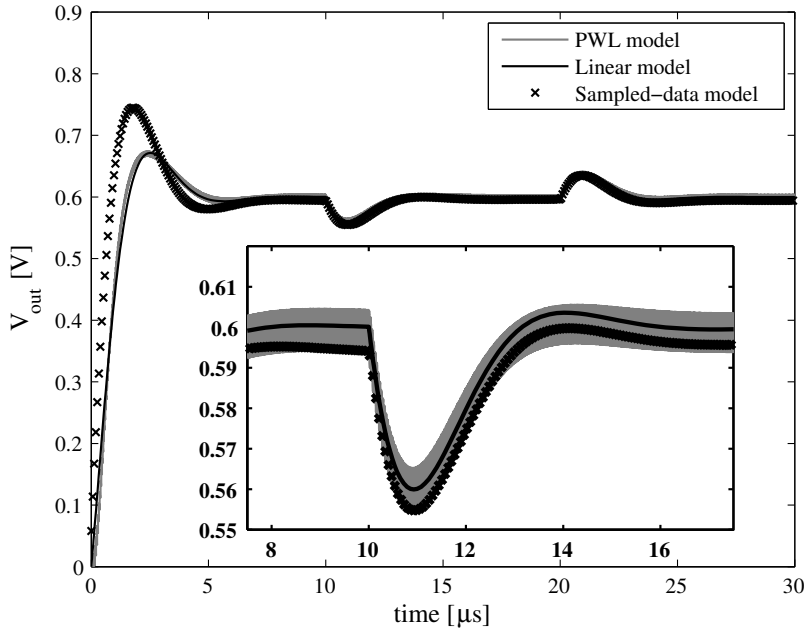


Figure 4.13: Transient simulation of the closed loop from sampled-data model and linear model

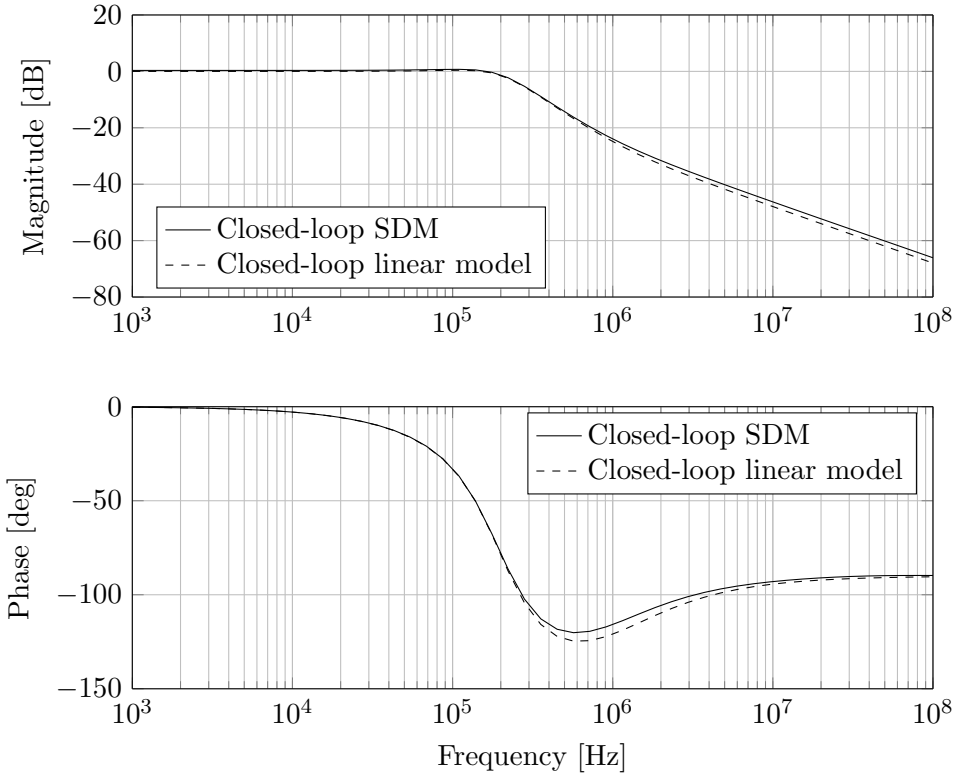


Figure 4.14: Bode diagram comparison of the closed-loops from sampled-data model and linear model

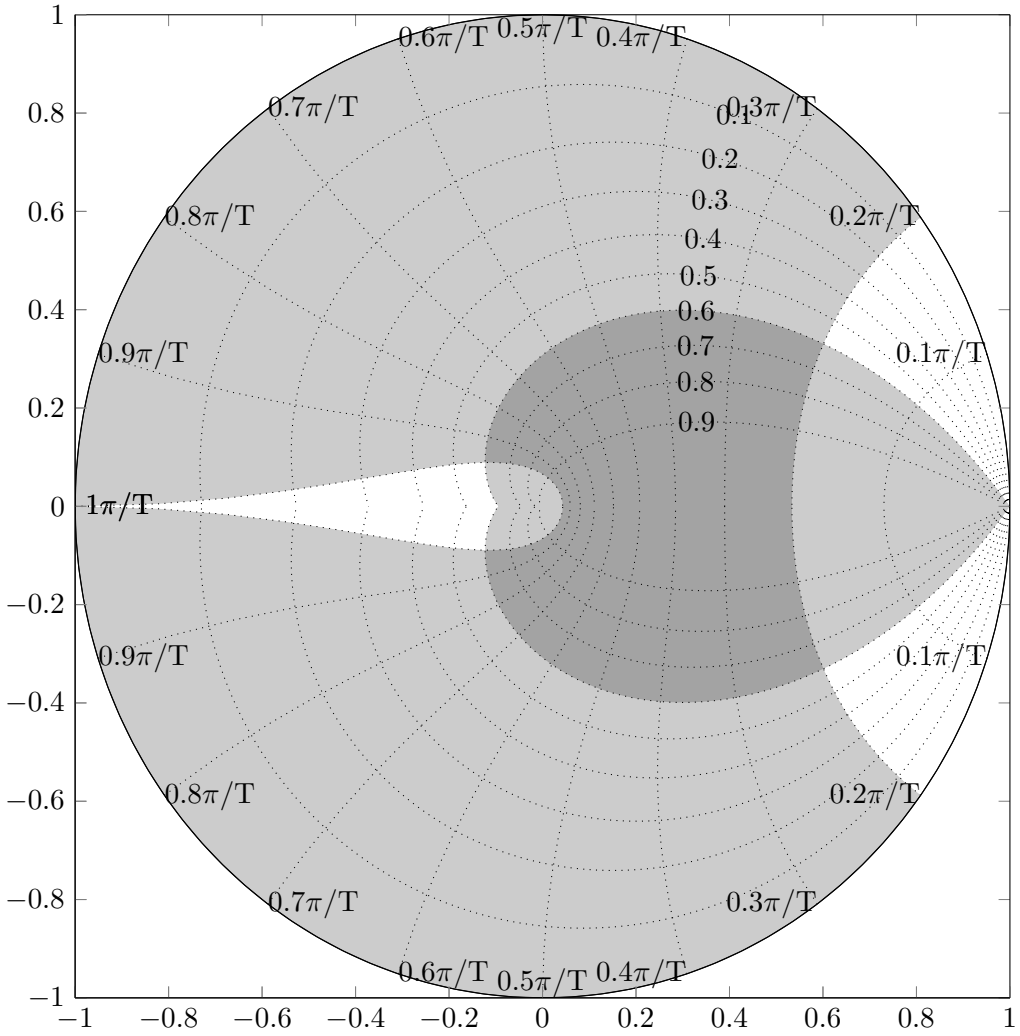


Figure 4.15: Location of Eigenvalues

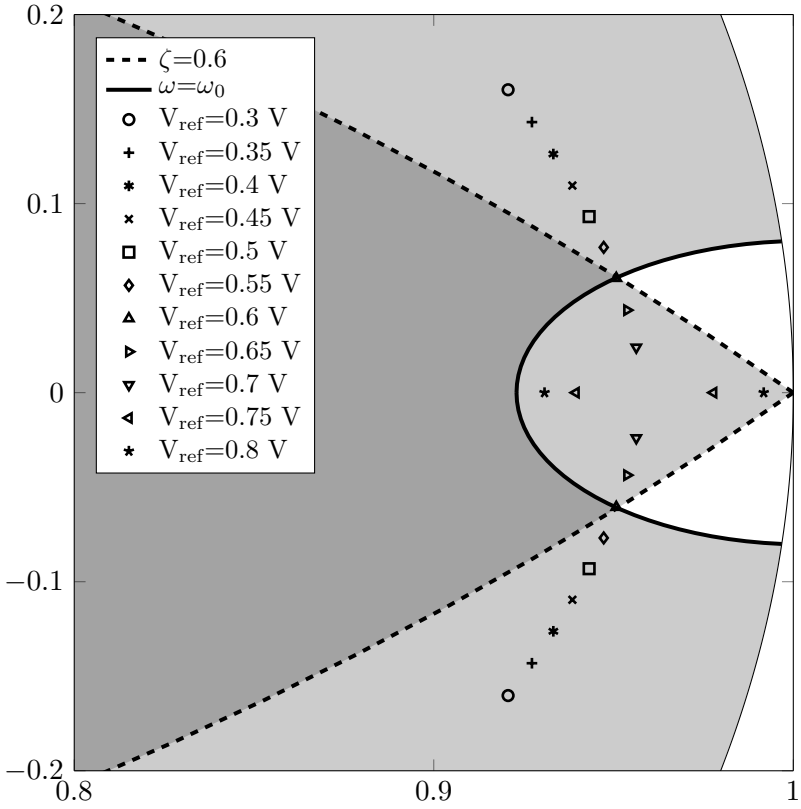


Figure 4.16: Diagram of Eigenvalues dispersion against the reference voltage variations

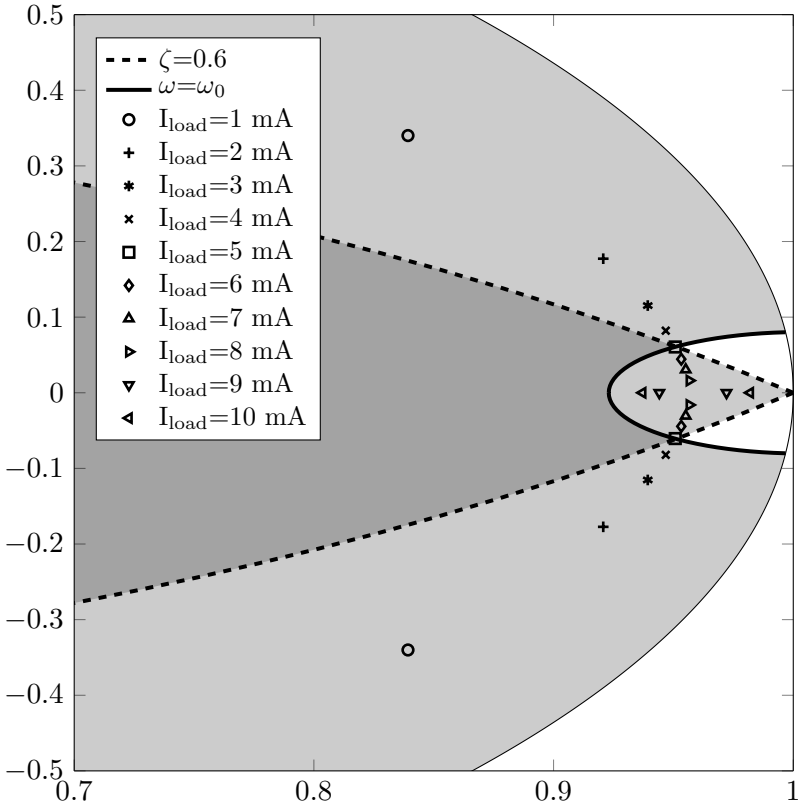


Figure 4.17: Diagram of Eigenvalues dispersion against load current variations

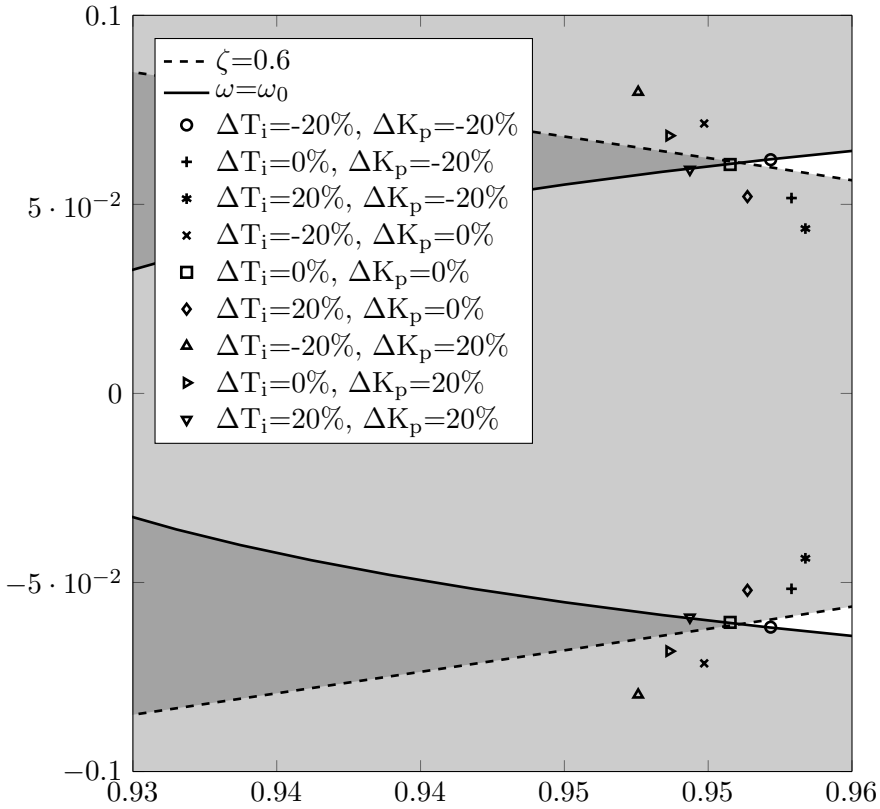


Figure 4.18: Location of Eigenvalues against variation in T_i and K_p, parameters of the controller

4.3 Linear frequency modulation with voltage and current loops

The voltage drop across the output resistance is proportional to the load current. An extra current feedback is therefore introduced along the voltage loop control as shown in Fig. 4.19. The output current, I_{out}, delivered by the converter is sensed using a current sensor. The output of the current sensor can be directly added to the voltage error of the voltage loop. The switching frequency is thus adjusted proportionally to the load current with a fast feedback scheme. However the speed of the current loop is limited by the bandwidth of the current sensor. A positive feedback is required otherwise the converter is configured in current source. Current mode

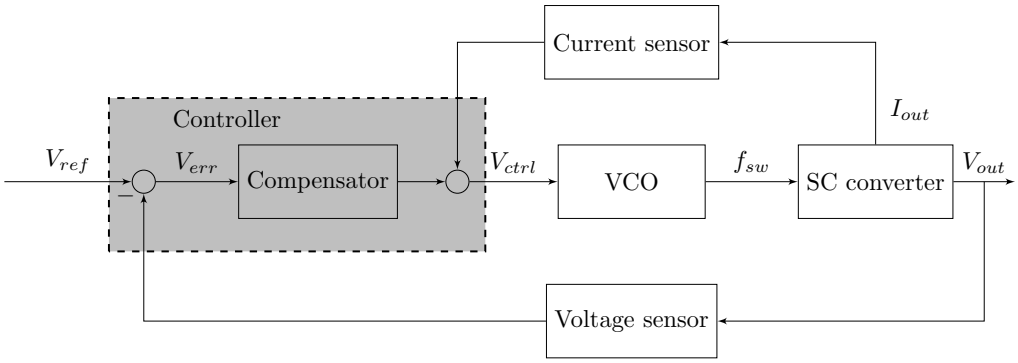


Figure 4.19: Diagram of a linear frequency modulation with a voltage loop assisted of a current loop

control has already been introduced in inductive DC-DC converters but efficient current sensing is still complicated. The shunt resistance-based current sensor is the simplest implementation. The voltage drop across the resistance is proportional to the load current. The value of the resistance must be high enough to ensure sufficient sensitivity. However the resistance introduced extra losses in the FSL region and decreases the original output voltage capability. For example purpose, a shunt resistance in inserted at the output of the converter to sense the output current as shown in Fig. 4.20. The converter parameters are unchanged and the shunt resistance value is $R_{shunt} = 1\ \Omega$. The voltage across the resistance is sensed and amplified with a gain G_{sens}. Then the voltage is averaged by a low-pass filter with a time-constant, τ. The transfert function of the current sensor is thus:

$$F(s) = \frac{V_{sens}(s)}{I_{out}(s)} = \frac{G_{sens}R_{shunt}}{1+\tau s} \tag{4.61}$$

The behavior of the current loop is analyzed using the diagram of Fig. 3.24. The output resistance of the converter is modeled using the non-linear average model in

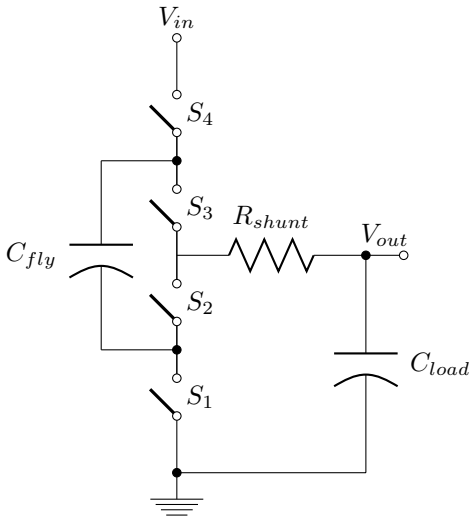


Figure 4.20: SC converter with a shunt resistance

Section 3.2.3. The shunt resistance is incorporated into (3.26) giving:

$$R_{out} = \frac{1}{4 f_{sw} C_{fly}} \cdot \coth\left(\frac{1}{8 R_{on} f_{sw} C_{fly}}\right) + R_{shunt} \tag{4.62}$$

This model is implemented and simulated in *Matlab/Simulink*. The operating point is found for the targeted output voltage, $V_{target} = 0.6\ V$ and the load current, $I_{load} = 5\ mA$ with:

$$R_{out}(f_{sw}) - \frac{0.5 V_{in} - V_{target}}{I_{load}} = 0 \tag{4.63}$$

The non-linear averaged model is linearized around this operating point and the small-signal block diagram is shown in Fig. 4.21. The open-loop expression is therefore:

$$H_{open}(s) = K_{vco} \cdot H_{fi}(s) \cdot F(s) \tag{4.64}$$

$$= K_{vco} \cdot \frac{as}{s+b} \cdot \frac{G_{sens} R_{shunt}}{1 + \tau s} \tag{4.65}$$

The transfer function of the control voltage, V_{ctrl}, to the switching frequency, f_{sw}, is now:

$$H_{cf}(s) = \frac{K_{vco}}{1 - H_{open}(s)} \tag{4.66}$$

The stability of the system is checked looking to $H_{open}(s)$. This transfer function is a bandpass filter like as shown in Fig. 4.22. The value of the bandwidth is defined by $B_w = b - \frac{1}{\tau}$ and the gain value is $K_{vco} G_{sens} R_{shunt} a$. Therefore the time constant of the filter, τ, must be higher than the time constant of the converter, $1/b$. Otherwise

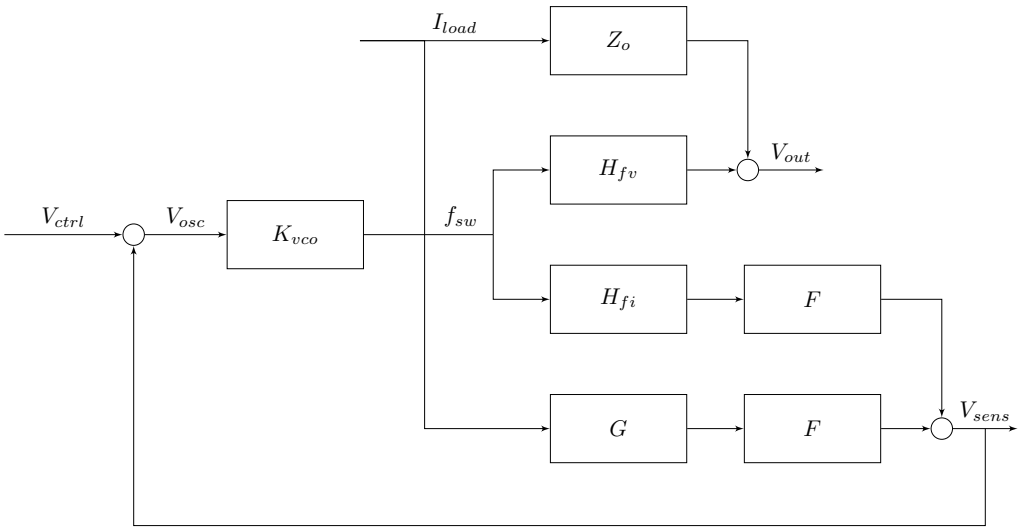


Figure 4.21: Block diagram of the small-signal model of the current loop

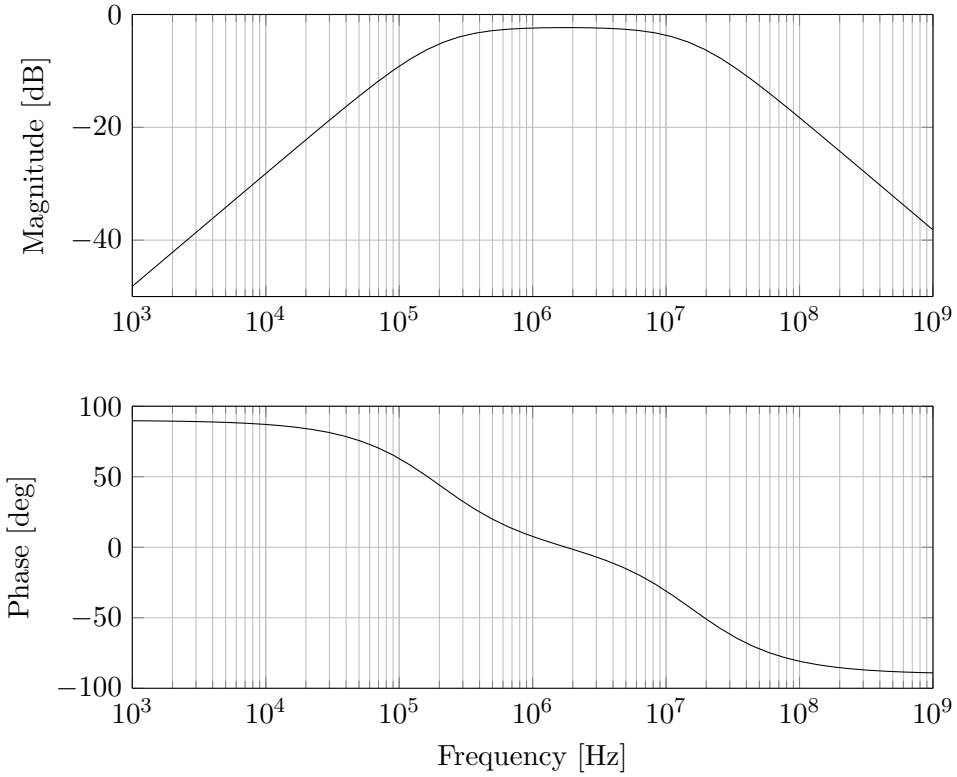


Figure 4.22: Control to switching frequency transfer function

the feedback will have little interest. The phase crosses 0° for the center angular frequency, $\omega_c = B_w/2$. The phase is shifted by $+180^\circ$ due to the positive feedback. As a consequence the system will be stable in closed loop if the gain in H_{open} is less than $0dB$, i.e. $K_{vco}G_{sens}R_{shunt}a < 1$. The control-to-switching frequency transfer function is:

$$H_{cf}(s) = K_{vco} \cdot \frac{\tau s^2 + (1+\tau b)s + b}{\tau s^2 + (b\tau - G_{sens}K_{vco}R_{shunt}a + 1)s + b} \tag{4.67}$$

The system thus behaves like the VCO in low and high frequency. The frequency response of H_{cf} is shown in Fig.4.23. The switching frequency also depends on the load current. The transfer function of the load current-to-the switching frequency is:

$$H_{if}(s) = G(s) \cdot F(s) \cdot H_{cf}(s) \tag{4.68}$$

The results are plotted in Fig. 4.24. The transfer function of control-to output voltage is compared with and without the feedback loop in Fig. 4.25 as well as for the load current-to-output voltage transfer function in Fig. 4.26. The control-to-output voltage transfer function exhibits a higher bandwidth with the current feedback than without it. The output impedance of the current feedback is lower than without it at low frequency.

The control-to-output voltage transfer function shown in Fig. 4.25 is a second order type with a zero:

$$H_{cv}(s) = H_{cf}(s) \cdot H_{fv}(s) \tag{4.69}$$

$$= K_{vco} \cdot G_0 \cdot \frac{\left(s + \frac{1}{\tau}\right)(s+b)}{\left(s^2 + \frac{b\tau - G_{sens}K_{vco}R_{shunt}a+1}{\tau}s + \frac{b}{\tau}\right)(s+b)} \tag{4.70}$$

$$= K_{vco} \cdot G_0 \cdot \frac{s + \frac{1}{\tau}}{s^2 + \frac{b\tau - G_{sens}K_{vco}R_{shunt}a+1}{\tau}s + \frac{b}{\tau}} \tag{4.71}$$

No resonance is visible in the Bode diagram in Fig. 4.25 and the decomposition of the denominator of (4.71) gives the damping factor, ζ_0 and the natural angular frequency, ω_0:

$$\zeta_0 = \frac{b\tau - G_{sens}K_{vco}R_{shunt}a + 1}{\tau} \cdot \frac{\sqrt{b}}{2\sqrt{\tau}} \tag{4.72}$$

$$\omega_0 = \sqrt{\frac{b}{\tau}} \tag{4.73}$$

The evaluation of the damping factor is 1.06 and the system can be decomposed with two separate real poles due to over-damping:

$$H_{cv}(s) = K_{vco} \cdot G_0 \cdot \frac{s + \frac{1}{\tau}}{(s+p_1)(s+p_2)} \tag{4.74}$$

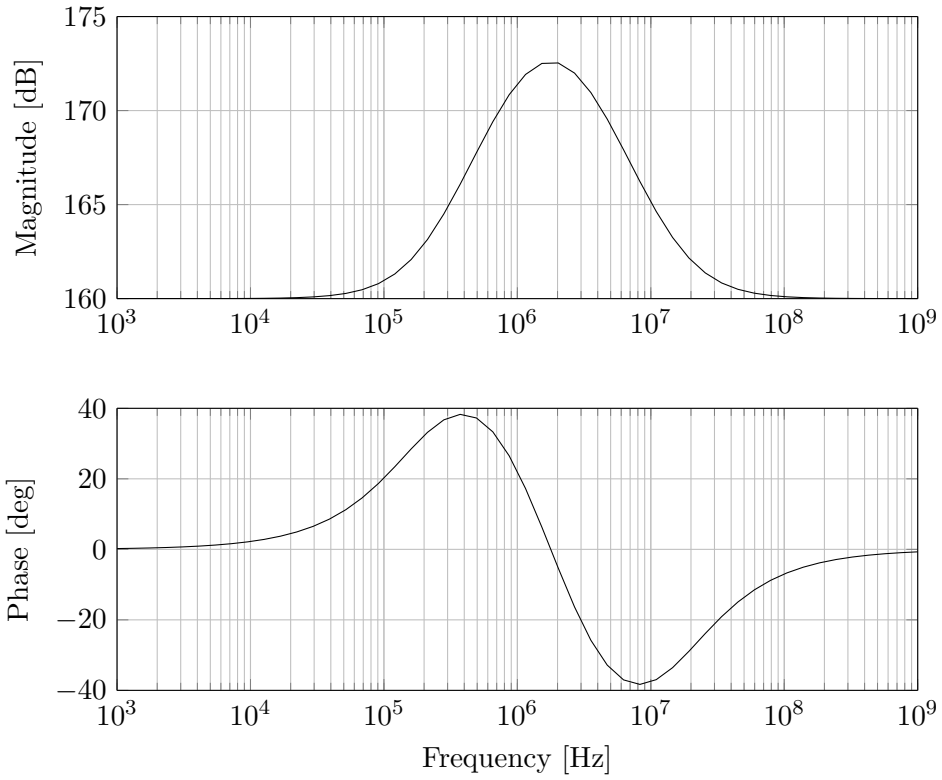


Figure 4.23: Control-to-switching frequency transfer function

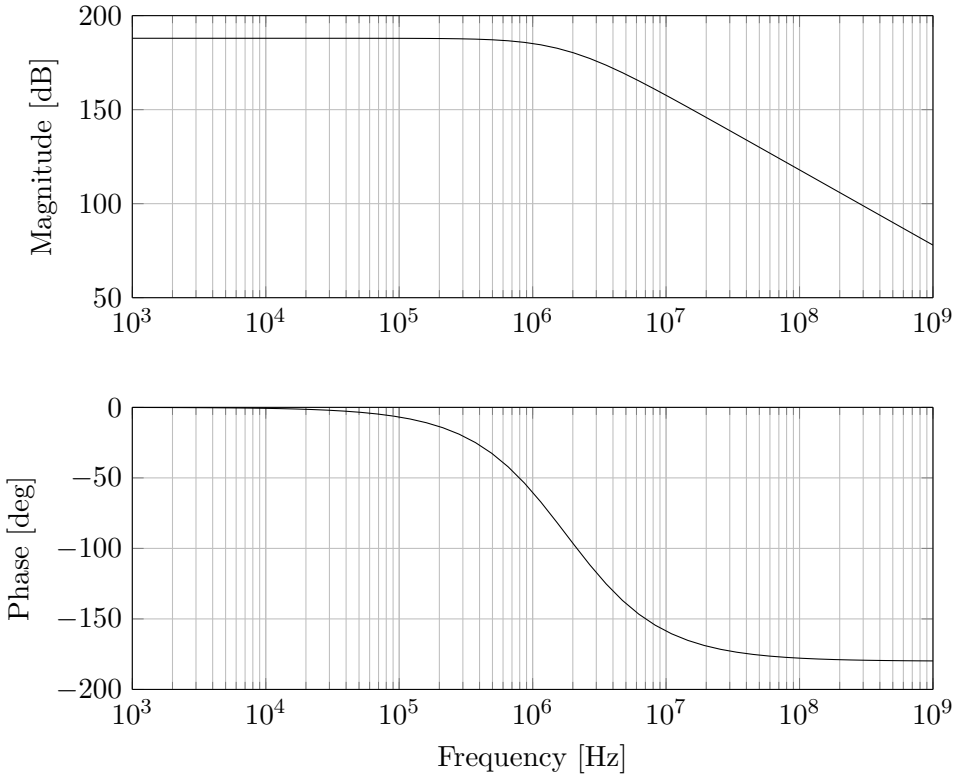


Figure 4.24: Load current-to-switching frequency transfer function

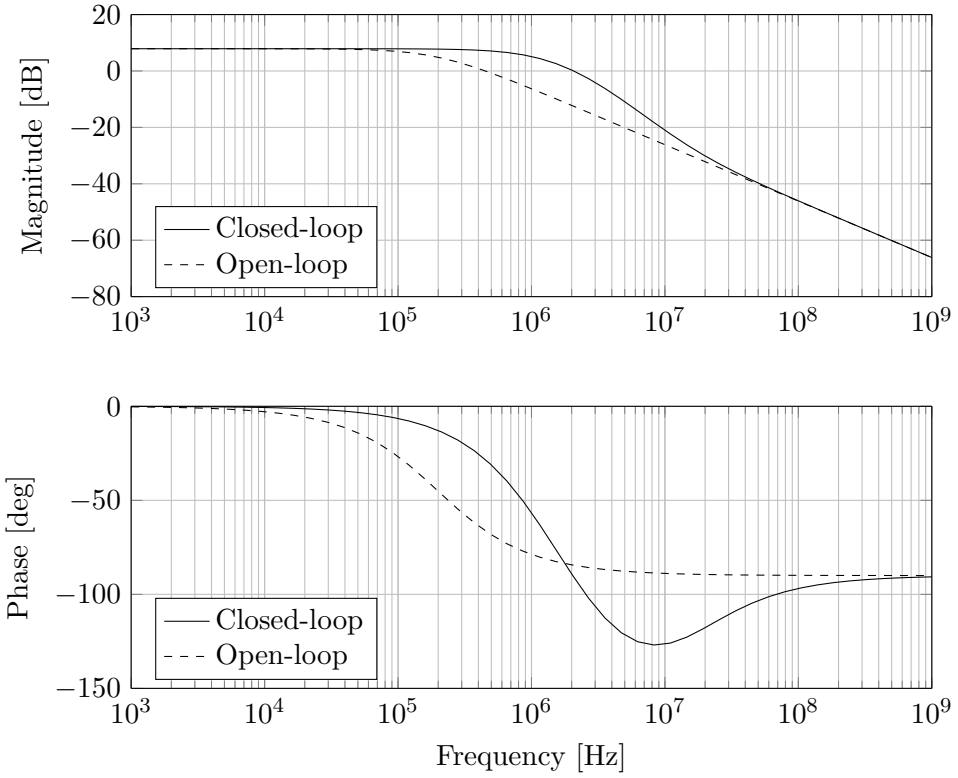


Figure 4.25: Control-to-output voltage transfer function

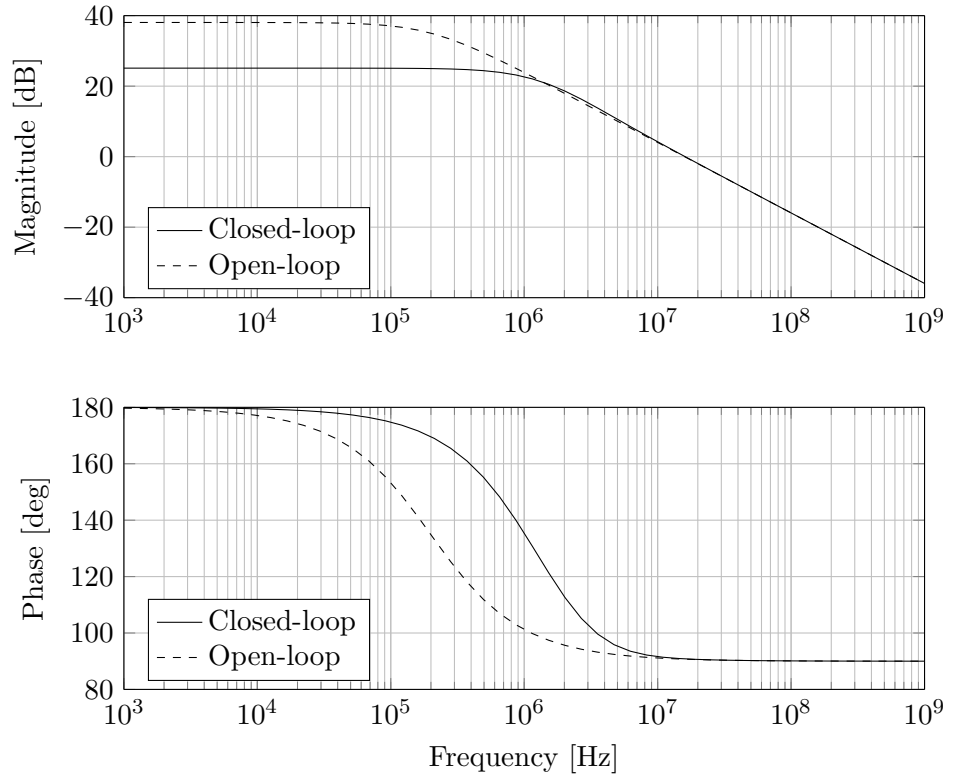


Figure 4.26: Load current-to-output voltage transfer function

where

$$p_1 = \left(\zeta_0 + \sqrt{\zeta_0^2 - 1}\right) \cdot \omega_0 \tag{4.75}$$

$$p_2 = \left(\zeta_0 - \sqrt{\zeta_0^2 - 1}\right) \cdot \omega_0 \tag{4.76}$$

Several compensation strategies are possible depending on the targeted closed-loop behavior. A PID implementation can be used to simplify the denominator of the plant transfer function by the numerator of the corrector and to set a second order behavior. When the frequency of the zero of the plant is much larger than the natural angular frequency of the plant, a simple PI can be used. Finally if the desired crossover frequency is set to a lower value than the one of the dominant pole of the plant, an integrator can achieve enough phase margin.
Fig. 4.25 shows that the zero has a large frequency and we propose to use a PI control and the open-loop is therefore:

$$H_{open}(s) = K_{vco} \cdot G_0 \cdot K_p \cdot \frac{\left(s + \frac{1}{\tau}\right)\left(s + \frac{1}{T_i}\right)}{(s + p_1)(s + p_2)\, s} \tag{4.77}$$

We can simplify the dominant pole, p_2 by the zero of the corrector with $T_i = \dfrac{1}{p_2}$ yielding:

$$H_{open}(s) = K_{vco} \cdot G_0 \cdot K_p \cdot \frac{s + \frac{1}{\tau}}{(s + p_1)\, s} \tag{4.78}$$

The value of K_p is now determined either by the open-loop phase margin or by the closed-loop behavior.

- The phase margin can be expressed as a function of the crossover frequency, ω_{0dB}, itself depending on K_p:

$$\omega_{0dB}(K_p) = \frac{\sqrt{2}}{2}\sqrt{p_1^2 - (\beta K_p)^2 + \sqrt{\left(p_1^2 + (\beta K_p)^2\right)^2 + \left(2\frac{\beta K_p}{\tau}\right)^2}} \tag{4.79}$$

  with $\beta = K_{vco}G_0$. Then the phase margin is a function of $\omega_{0dB}(K_p)$:

$$PM(\omega_{0dB}) = 90 - \left(\arctan\left(\frac{\omega_{0dB}}{p-1}\right) - \arctan\left(\omega_{0dB}\tau\right)\right) \cdot \frac{180}{\pi} \tag{4.80}$$

  By injecting (4.79) into (4.80) we obtain the phase margin as a function of K_p.

- The damping factor is determined by the closed-loop:

$$H_{closed}(s) = K_{vco}G_0K_p \frac{s + \frac{1}{\tau}}{s^2 + (K_{vco}G_0K_p + p_1)s + \frac{K_{vco}G_0K_p}{\tau}} \tag{4.81}$$

and the damping factor is a function of K_p

$$\zeta_0(K_p) = \frac{K_{vco}G_0K_p + p_1}{2\sqrt{\frac{K_{vco}G_0K_p}{\tau}}} \tag{4.82}$$

The phase margin and damping factor versus K_p are plotted in Fig. 4.27 and Fig. 4.28 respectively. The value of K_p required to achieve a phase margin of 60 ° is 0.7542 and 0.7406 to set a damping factor of 0.6. Both values are very closed because $PM \approx 100 \cdot \zeta_0$. The Bode diagram of the open-loop transfer function is plotted in Fig. 4.29 with the transfer function of the plant and the one of the PI controller. Transient simulations are performed. A current step of 5 mA is applied at 10 μs and relaxed at 20 μs in Fig. 4.30. The voltage undershoot in 5% of the voltage reference and the recovery is 500 ns. The solution offers a better cross-over frequency than previous controllers and the transient results are better (as compared to Fig. 4.9 for example). Fig. 4.31 and Fig. 4.32 show the dispersion of the control-to-output voltage transfer function for load range from 1 mA to 10 mA and a reference voltage range from 0.5 V to 0.8 V respectively. The load current variation has the same impact as in the voltage mode control. A phase margin degradation at low load current is expected. On the contrary the voltage reference has a strong impact. A resonance appears at the lowest voltage reference (0.5 V) meaning that the PI control strategy will be inefficient. A PID controller would be required to mitigate this effect. As a conclusion the control using a positive current feedback scheme is less robust than the voltage mode strategy. Nonetheless, robustness is similar regarding the load current.

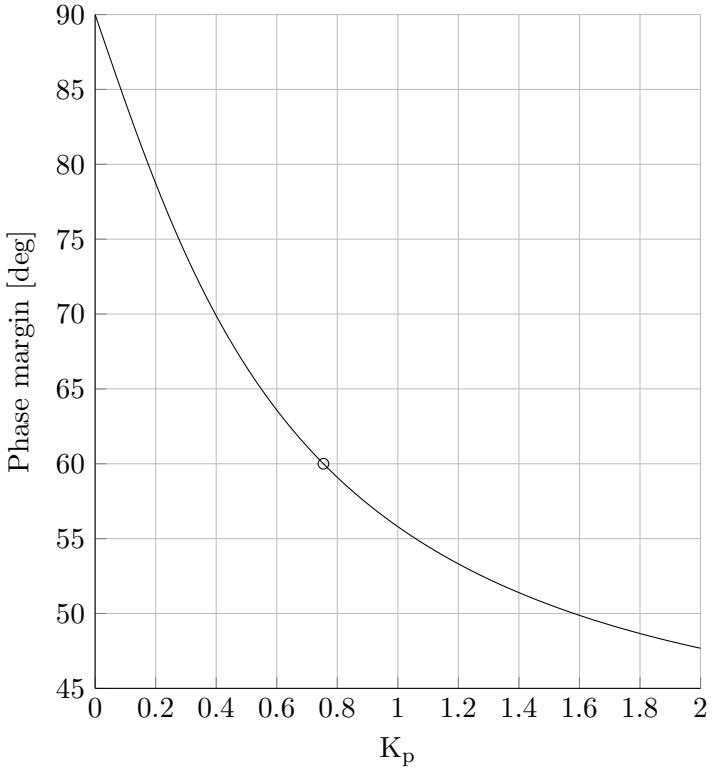


Figure 4.27: Phase margin of the open-loop as a function of K_p (targeted value is 60 $^\circ$)

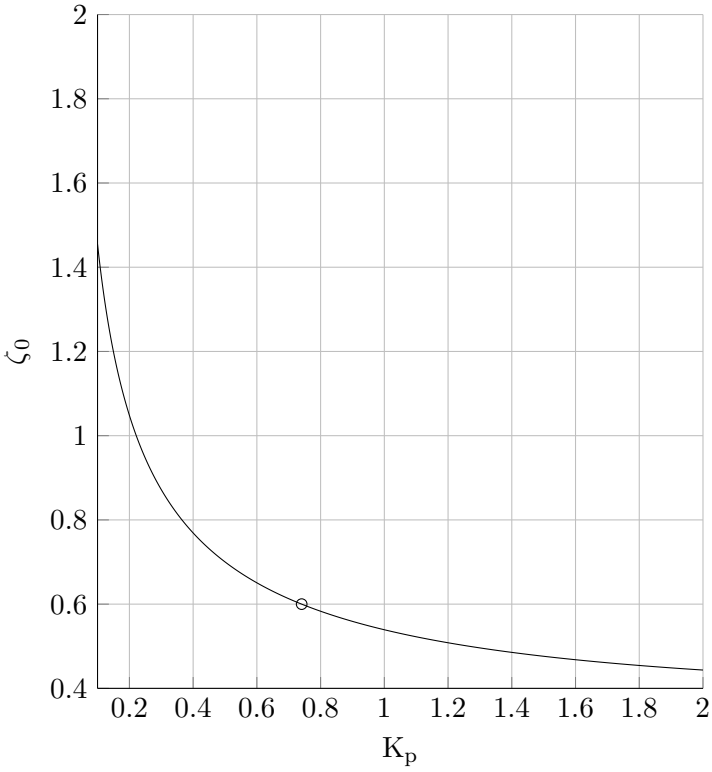


Figure 4.28: Damping factor of the closed-loop as a function of K_p (targeted value is 0.6

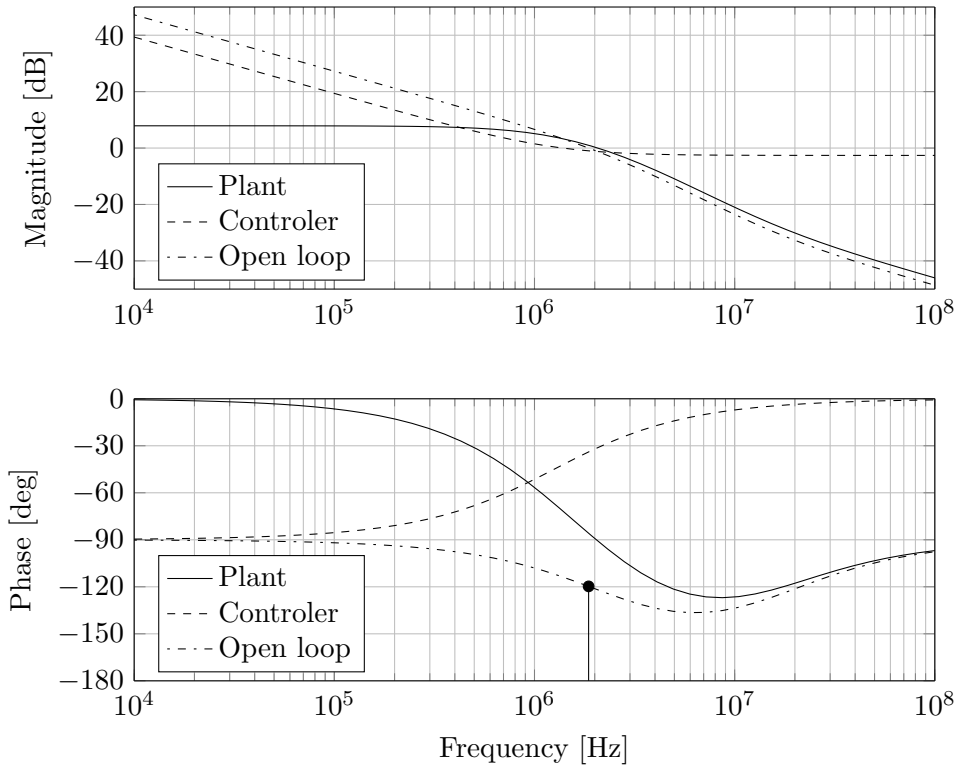


Figure 4.29: Bode diagram of the plant, the open-loop and the PI controller transfer function

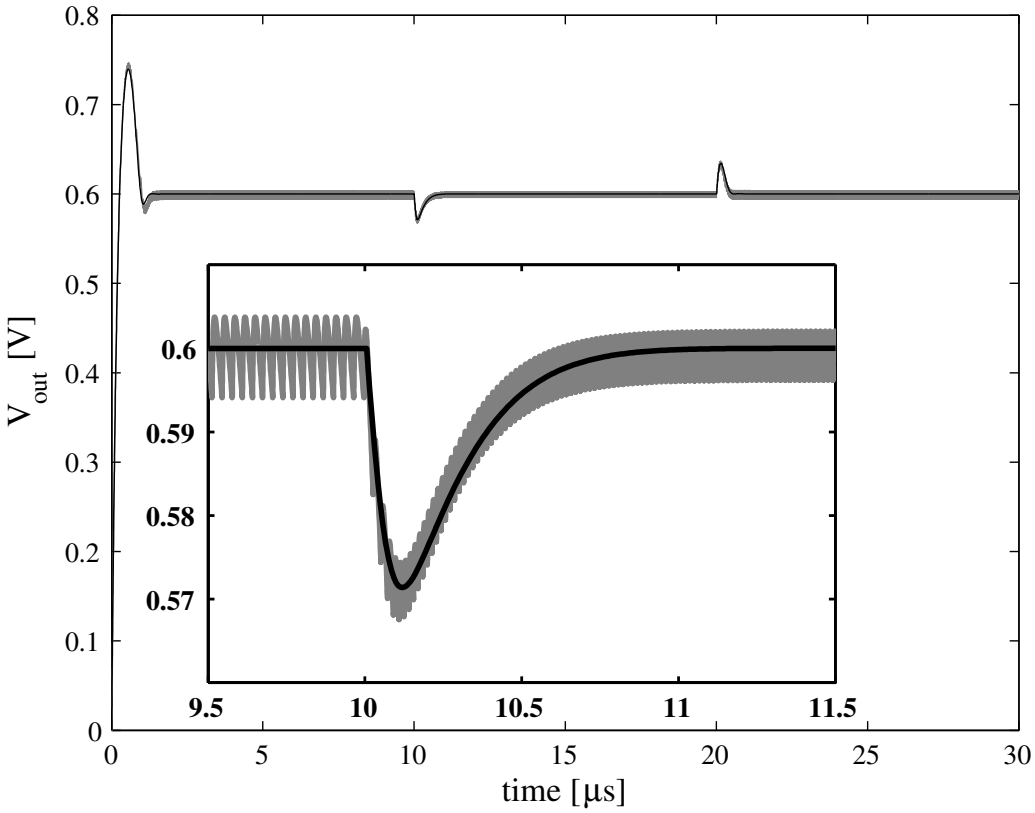


Figure 4.30: Load transient simulation

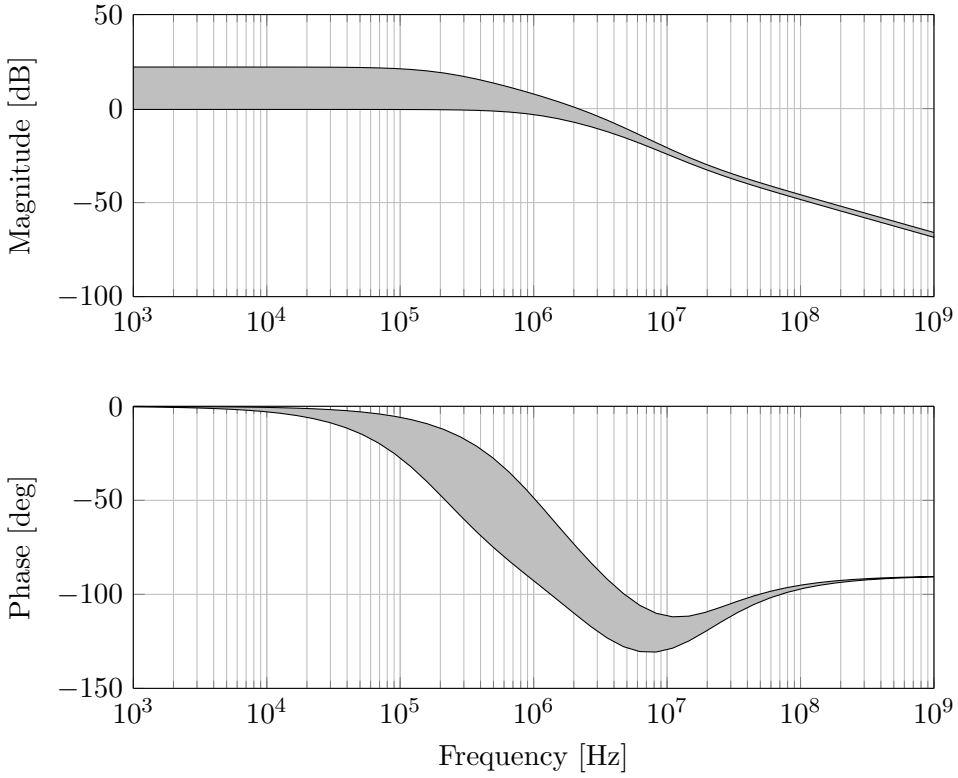


Figure 4.31: Variation of the control-to-output voltage transfer function in the load range from 1 mA to 10 mA

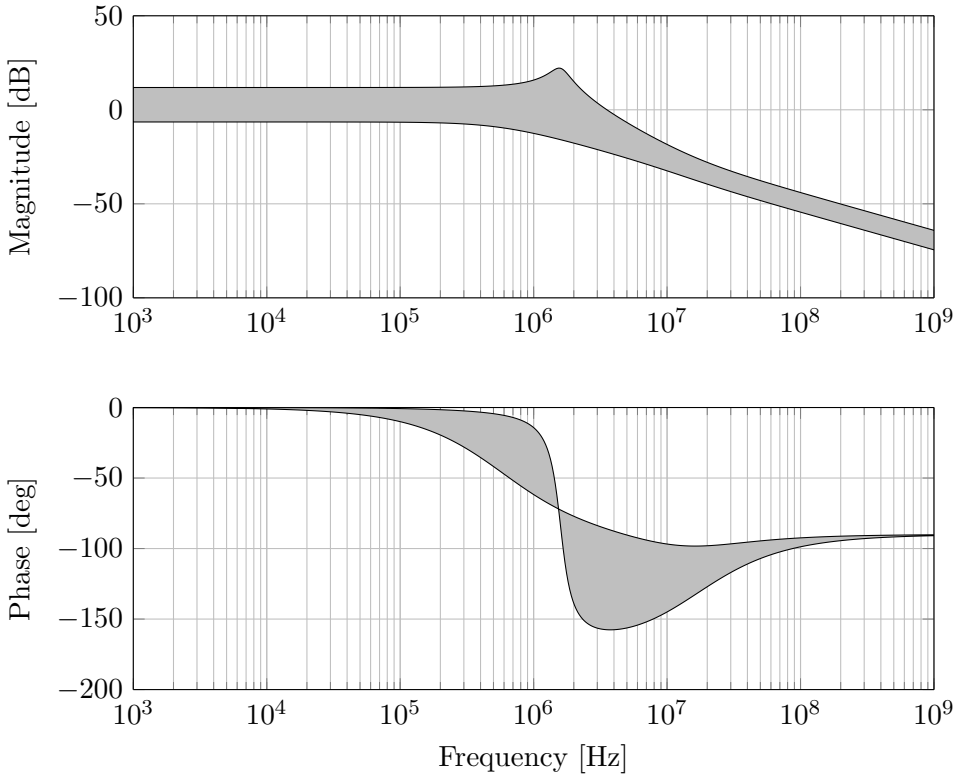


Figure 4.32: Variation of the control-to-output voltage transfer function in the reference voltage range from 0.5 V to 0.8 V

4.4 Sliding-mode with loop-delay modulation

Sliding mode controls are non-linear controls well known for their robustness and dynamic performances. Recently sliding-mode controls have been successfully introduced in inductive DC-DC converters because the switching control law can directly drive the power stage [102, 103]. Sliding-mode control operates at variable switching frequency by nature. This could be harmful to EMI sensitive load as RF circuits and switching frequency regulation has been introduced to address this issue. Sliding-mode control can thus be proposed for SC converters. To understand how sliding-mode can be applied to SC converters, let's analyze the voltage across the flying capacitor in a 2:1 SC converter. The steady-state operation is depicted in Fig. 4.33. The flying capacitor is ideally charged to $V_{in} - V_{out}$ and ideally discharged to V_{out} with exponential behavior. At the beginning of the charging phase, the voltage across the flying capacitor is V_{min}. The capacitor charges to $V_{in} - V_{out}$ yielding

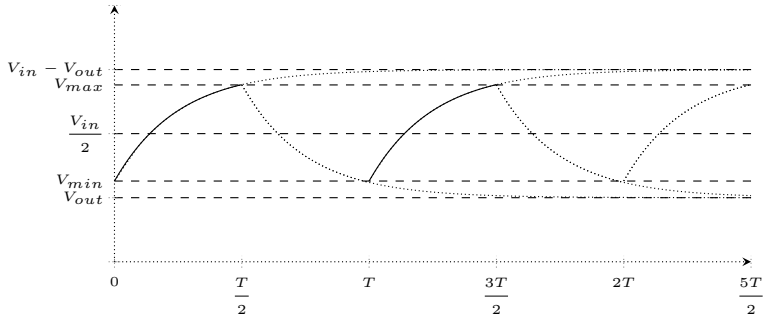


Figure 4.33: Steady-state voltage across the flying capacitor with sliding-mode control

$$V_{fly}^{(1)}(t) = V_{in} - V_{out} + (V_{min} - V_{in} + V_{out})e^{-t/(2R_{on}C_{fly})} \tag{4.83}$$

Then the system switches to the discharging phase at $t = T/2$. The initial voltage across the flying capacitor is V_{max}. The capacitor is thus discharged to V_{out}. The cycle finishes at $t = T$ and the voltage across the flying capacitor is now V_{min}. The equation of the voltage is

$$V_{fly}^{(2)}(t) = V_{out} + (V_{max} - V_{out})e^{-(t-T/2)/(2R_{on}C_{fly})} \tag{4.84}$$

Due to the continuity of the voltage across the flying capacitor, in steady-state, we can write

$$V_{fly}^{(1)}(1/(2f_{sw})) = V_{max} \tag{4.85}$$

$$= V_{in} - V_{out} + (V_{min} - V_{in} + V_{out})e^{-1/(4f_{sw}R_{on}C_{fly})} \tag{4.86}$$

$$V_{fly}^{(2)}(1/f_{sw}) = V_{min} \tag{4.87}$$

$$= V_{out} + (V_{max} - V_{out})e^{-1/(4f_{sw}R_{on}C_{fly})} \tag{4.88}$$

The voltage ripple across the flying capacitor is $\Delta_V = V_{max} - V_{min}$. (4.86) and (4.88) yields

$$\Delta_V(f_{sw}) = (V_{in} - 2V_{out})\frac{1 - e^{-1/(4f_{sw}R_{on}C_{fly})}}{1 + e^{-1/(4f_{sw}R_{on}C_{fly})}} \tag{4.89}$$

The flying capacitor voltage ripple is null when the converter operates at very high switching frequency. Let's compute the averaged voltage value across the flying capacitor during steady-state operation:

$$\overline{V_{fly}} = \frac{1}{T}\left[\int_0^{T/2} V_{fly}^{(1)}dt + \int_{T/2}^{T} V_{fly}^{(2)}dt\right] \tag{4.90}$$

$$= \frac{1}{T}\left[\frac{TV_{in}}{2} + 2R_{on}C_{fly}(1 - e^{(T/(4R_{on}C_{fly}))})(V_{max} + V_{min} - V_{in})\right] \tag{4.91}$$

from (4.86) and (4.88)

$$V_{max} + V_{min} = V_{in} \tag{4.92}$$

Thus (4.91) is

$$\overline{V_{fly}} = \frac{V_{in}}{2} \tag{4.93}$$

The averaged voltage value across the flying capacitor in steady-state does not depend on the switching frequency. We propose a sliding -mode control based on this statement. The SC converter and its variable state-space structure is represented in Fig. 4.34 with an hybrid automaton. State 1 corresponds to the charging phase and State 2 the discharging phase. The automaton switches from the charging phase to the discharging phase when the voltage across the flying capacitor is above $\frac{V_{in}}{2}$ and return to the charging phase when this voltage is bellow $\frac{V_{in}}{2}$. The converter motion is thus described by the following switching condition:

$$g(x) = x_1 - \frac{V_{in}}{2} \tag{4.94}$$

where x_1 is the voltage across the flying capacitor. The system is constrained on a surface in the state space, the sliding surface, $g(x)$. Considering the switching behavior, the system dynamics is represented by:

$$\dot{x} = \begin{cases} f_1(x) & \text{if } g(x) < 0 \\ f_2(x) & \text{if } g(x) > 0 \end{cases} \tag{4.95}$$

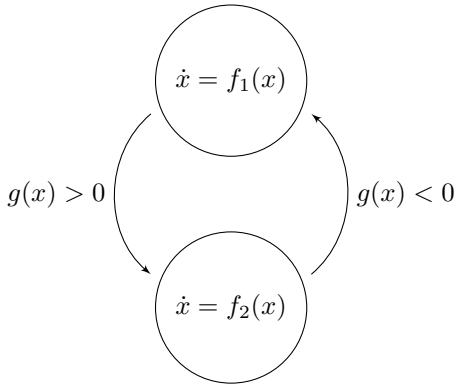


Figure 4.34: Hybrid automaton of the sliding mode

The existence of the sliding mode trajectory is verified if $\frac{\partial g}{\partial x} \cdot f_1(x) > 0$ and $\frac{\partial g}{\partial x} \cdot f_2(x) < 0$ meaning that the surface is attractive. The expression of f_1 and f_2 are derived from the state-space representation where x is the state-space vector, x_1 is the voltage across the flying capacitor and x_2 the voltage across the output capacitor:

$$f_1(x) = -\frac{x_1}{2C_{fly}R_{on}} - \frac{x_2}{2C_{fly}R_{on}} + \frac{V_{in}}{2C_{fly}R_{on}} \tag{4.96}$$

$$f_2(x) = -\frac{x_1}{2C_{fly}R_{on}} + \frac{x_2}{2C_{fly}R_{on}} \tag{4.97}$$

Since $\frac{\partial g}{\partial x} = 1$, it comes

$$\frac{\partial g}{\partial x} f_1(x) = f_1(x) \tag{4.98}$$

$$\frac{\partial g}{\partial x} f_2(x) = f_2(x) \tag{4.99}$$

The sliding motion implies for $g(x) < 0$

$$f_1(x) > 0 \tag{4.100}$$

$$-\frac{x_1}{2C_{fly}R_{on}} - \frac{x_2}{2C_{fly}R_{on}} + \frac{V_{in}}{2C_{fly}R_{on}} > 0 \tag{4.101}$$

$$V_{in} - x_1 - x_2 > 0 \tag{4.102}$$

$$x_1 + x_2 < V_{in} \tag{4.103}$$

and for $g(x) > 0$

$$f_2(x) > 0 \tag{4.104}$$

$$-\frac{x_1}{2C_{fly}R_{on}} + \frac{x_2}{2C_{fly}R_{on}} < 0 \tag{4.105}$$

$$x_2 - x_1 < 0 \tag{4.106}$$

$$x_2 < x_1 \tag{4.107}$$

These conditions are systematically verified during the operation of the converter because the output voltage is lower than the flying capacitor voltage and their sum is lower than the input voltage. The switching dynamics is now

$$\dot{x} = \begin{cases} f_1(x) & \text{if } g(x) < 0 \\ f_s(x) & \text{if } g(x) = 0 \\ f_2(x) & \text{if } g(x) > 0 \end{cases} \tag{4.108}$$

Regularization of the sliding mode implies to find the continuous vector function f_s such that the state trajectory remains on the switching surface. The application of the Filippov's continuation method [104] gives

$$f_s = \alpha f_1 + (1-\alpha) f_2 \tag{4.109}$$

$$\alpha \in [0,1] : \frac{\partial g}{\partial x} f_s = 0 \tag{4.110}$$

with

$$\alpha = \frac{\frac{\partial g}{\partial x} f_2}{\frac{\partial g}{\partial x}(f_1 - f_2)} = \frac{x_1 - x_2}{V_{in} - 2x_2} \tag{4.111}$$

$$1 - \alpha = \frac{\frac{\partial g}{\partial x} f_1}{\frac{\partial g}{\partial x}(f_1 - f_2)} = \frac{V_{in} - x_1 - x_2}{V_{in} - 2x_2} \tag{4.112}$$

and

$$\frac{\partial g}{\partial x} f_s = f_s \tag{4.113}$$

$$= \frac{x_1 - x_2}{V_{in} - 2x_2} \frac{V_{in} - x_1 - x_2}{2C_{fly}R_{on}} + \frac{V_{in} - x_1 - x_2}{V_{in} - 2x_2} \frac{x_2 - x_1}{2C_{fly}R_{on}} \tag{4.114}$$

$$= 0 \tag{4.115}$$

The hybrid automaton with the induced mode is given in Fig. 4.35. The switching frequency of the sliding mode control is infinite. However the delay of the loop limits the frequency value in practice. Since the switching frequency is very high the converter will operate in the FSL region. The output voltage will be closed to the ideal conversion ratio for small value of load current. The switching frequency of the sliding mode must be regulated to allow output voltage regulation. The switching frequency can be regulated with a controllable delay. This is called loop-delay modulation. Another technique is based on the ripple of the flying capacitor

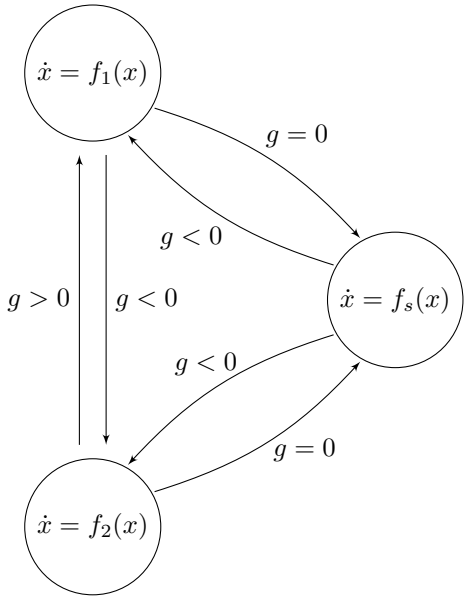


Figure 4.35: Hybrid automaton of the sliding mode with the induced mode

voltage. The ripple is a function of the switching frequency as demonstrated by (4.89). Therefore a constrained ripple value will result on a constrained switching frequency. This technique is detailed in Section 4.5.
The loop delay modulation principle is depicted in Fig. 4.36. The sliding mode control law is used to drive the power stage of the converter. The frequency modulation of the loop is achieved by the modulation of the sliding mode loop delay. A voltage reference, V_{ref}, is compared to the output voltage of the converter, V_{out}. The error signal is provided to a compensator to set the proper delay in the loop. The controllable delay is modeled by a linear function

$$\phi(t) = K_\phi \cdot V_{ctrl} + \phi_0 \tag{4.116}$$

where K_ϕ is the gain of the delay cell and ϕ_0 corresponds to the minimum delay when the control voltage, V_{ctrl} is null. Sampled-data modeling is used to determine the frequency response of the loop to a change in the loop-delay. The sliding motion imposes an infinite switching frequency and the switching instants are now determined by the delay of the loop. The dynamics over a state S_i from (3.31) including the loop delay, ϕ is

$$x_i(t, \phi) = \Phi_i x_0 + \Gamma_i u \tag{4.117}$$

with $\Phi_i = e^{(A_i \phi)}$ and $\Gamma_i = [e^{(A_i \phi)} - I] A_i^{-1} B_i$. The sampled-data model is built and linearized around a fixed point as in Section 3.6.2. The small-signal dynamics is

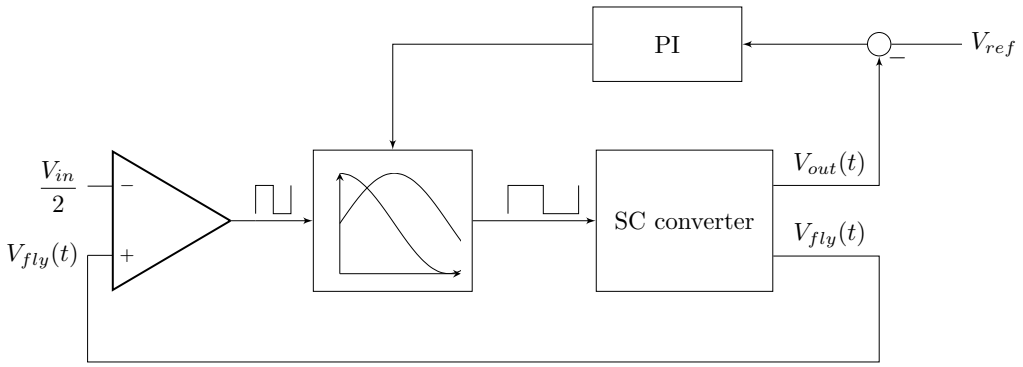


Figure 4.36: Diagram of the loop delay modulation of the sliding mode control

now

$$\hat{x}_{n+1} \approx \frac{\partial f}{\partial x_n}\hat{x}_n + \frac{\partial f}{\partial u_n}\hat{u}_n + \frac{\partial f}{\partial \phi_n}\hat{\phi}_n \tag{4.118}$$

$$\hat{x}_{n+1} \approx \Phi_0\hat{x}_n + \Gamma_u\hat{u}_n + \Gamma_\phi\hat{\phi}_n \tag{4.119}$$

$$\hat{v}_{out} \approx C\hat{x}_n + D\hat{u}_n \tag{4.120}$$

with

$$\frac{\partial f}{\partial x_n} = \Phi_0 = \Phi_1\Phi_2 \tag{4.121}$$

$$\frac{\partial f}{\partial u_n} = \Gamma_0 = \Phi_2\Gamma_1 + \Phi_2 \tag{4.122}$$

$$\frac{\partial f}{\partial \phi_n} = \Phi_2\left[(A_1 + A_2)\,x^0(d) + (B_1 + B_2)\,U\right] \tag{4.123}$$

The transfer function of the loop-delay-to-output voltage is

$$\frac{v_{out}(z)}{\phi(z)} = C \cdot (zI - \Phi_0)^{-1} \cdot \Gamma_\phi \tag{4.124}$$

$$\tag{4.125}$$

For illustration purpose, the model is derived for the 2:1 SC converter. The targeted output voltage is 0.6 V and the load current is 5 mA. The Bode diagram of the transfer function of the loop-delay-to-output voltage is shown in Fig. 4.37 in the s and z domain respectively. The transfer function has one pole and the PI controller must be selected similarly as for the linear frequency modulation. The design of the controller follows the same steps as in Section 4.2. The transfer function of the plant is

$$H(s) = K_{delay} \cdot \frac{v_{out}(s)}{\phi(s)} = \frac{G_0}{1 + \tau_0 s} \tag{4.126}$$

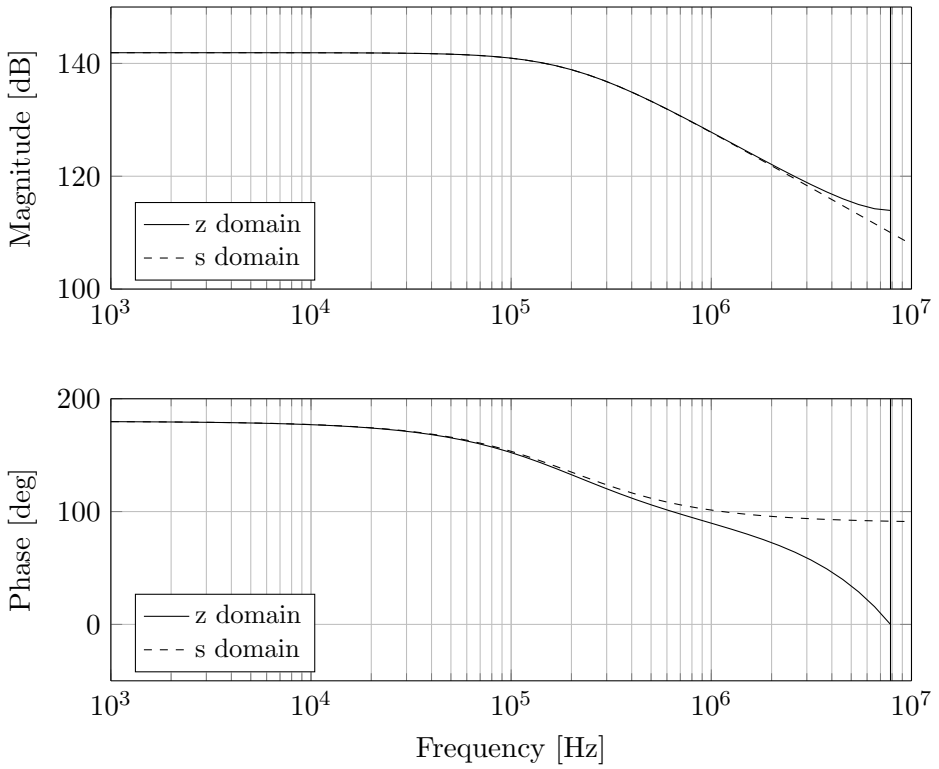


Figure 4.37: Bode diagram of the loop-delay-to-output voltage transfer function

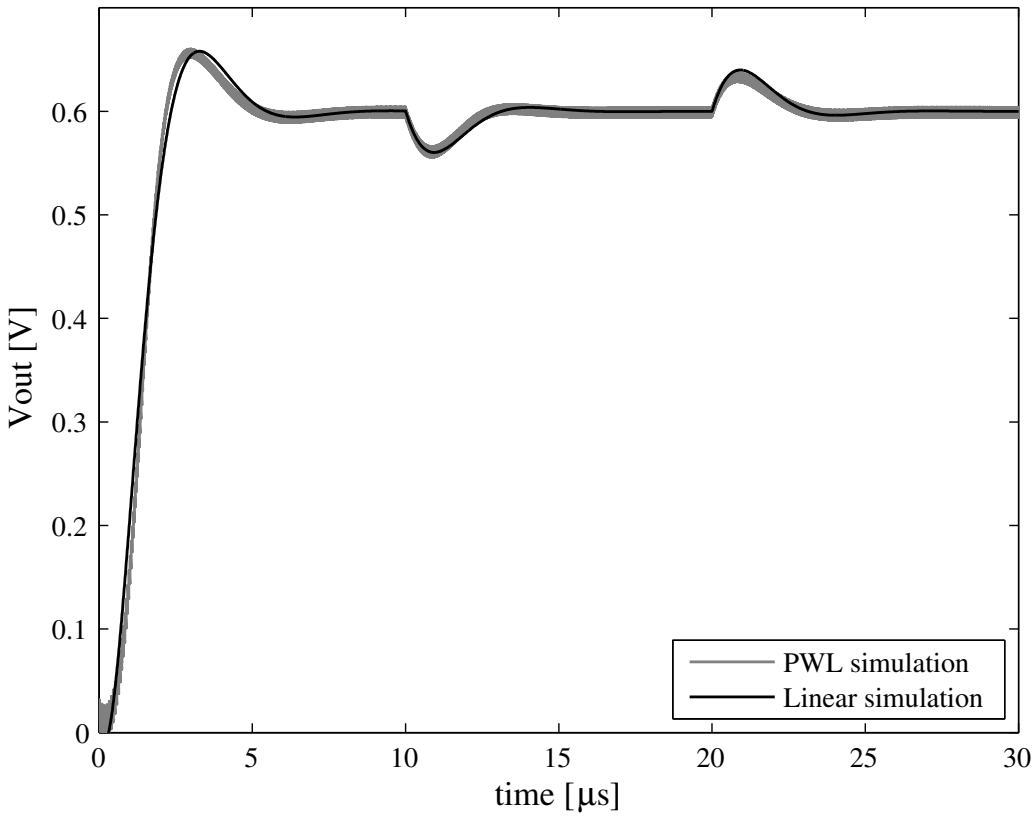


Figure 4.38: Transient simulation of the PWL and linear model of the loop-delay modulation

A second order behavior is selected with $\zeta_0 = 0.6$ and $\omega_0 = 1/\tau_0$. The parameter of the PI controller are evaluated with (4.21) and (4.20) yielding $K_p = 0.161$ and $T_i = 159\ ns$. The PWL model of the converter with the sliding mode control and the modulation is implemented in *Matlab/Simulink*. The simulation of the linearized model and the PWL model are presented in Fig. 4.38. A positive load transient of 1 mA is applied at 10 μs and a negative one at 20 μs. The linear model gives a good prediction of the PWL behavior with the sliding mode and the loop-delay modulation. This control does not show significant improvement compared to the linear frequency modulation. The sliding mode issues only the instantaneous frequency while its value is controlled by a linear loop. Another sliding mode control should be explored to take benefits of the sliding mode control.

4.5 Sliding-mode with comparator hysteresis band

The chattering effect of sliding mode can be addressed introducing an hysteresis band at the comparator output instead of a controllable delay. The control is redefined as follows

$$\dot{x} = \begin{cases} f_1(x) & \text{if } g(x) < -k \\ f_2(x) & \text{if } g(x) > +k \end{cases} \tag{4.127}$$

The value of k set the hysteresis band. The converter operates in the charging phase when $g(x) < -k$ and in the discharging phase when $g(x) > +k$. As a consequence no switching occurs in the region $-k < g(x) < +k$ and the converter remains in the previous state. The switching frequency is therefore defined by the hysteresis band. The relation between the switching frequency and the hysteresis band is developed in [104]. The operation of the sliding mode is represented in Fig. 4.39. The duration

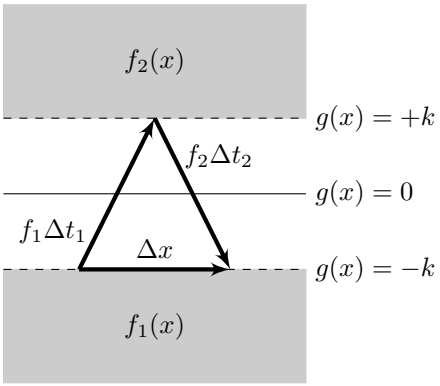


Figure 4.39: Diagram of the sliding mode operation with an hysteresis band

of the vector f_1 to move from the lower bound to the upper bound is Δt_1. In the

same way, Δt_2 is the duration of the vector f_2 to move from the upper bound to the lower bound. As demonstrated in [104] with $\nabla g = \dfrac{\partial g}{\partial x}$:

$$\Delta t_1 = \frac{2k}{\nabla g \cdot f_1} = \frac{-4R_{on}C_{fly}k}{x_1 + x_2 - V_{in}} \tag{4.128}$$

$$\Delta t_2 = \frac{-2k}{\nabla g \cdot f_2} = \frac{-4R_{on}C_{fly}k}{x_1 - x_2} \tag{4.129}$$

The average velocity in the sliding mode is given by

$$f^0 = \frac{\nabla g \cdot f_1}{\nabla g \cdot (f_1 - f_2)} f_1 - \frac{\nabla g \cdot f_1}{\nabla g \cdot (f_1 - f_2)} f_2 \tag{4.130}$$

$$= -\frac{(x_1 - x_2)(x_1 + x_2 - V_{in})}{R_{on}C_{fly}(V_{in} - 2x_2)} \tag{4.131}$$

At the equilibrium $f^0 = 0$ therefore

$$f^0 = 0 \begin{cases} x_1 = y,\ x_2 = y & \text{if } g(x) = -k \\ x_1 = V_{in} - y,\ x_2 = y & \text{if } g(x) = +k \end{cases} \tag{4.132}$$

Thus for a given value of k, the value of the flying capacitor, V_{fly} is equal to the output voltage, V_{out} near $g(x) = -k$ and to $V_{in} - V_{out}$ near $g(x) = +k$. At the end of each cycle, the output voltage reaches the value y demonstrating that the output voltage can be set despite a constraint on the flying capacitor voltage. The durations Δt_1 and Δt_2 are expressed as

$$\Delta t_1 = \frac{4R_{on}C_{fly}k}{V_{in} - 2y} \tag{4.133}$$

$$\Delta t_2 = \frac{4R_{on}C_{fly}k}{V_{in} - 2y} \tag{4.134}$$

The instantaneous switching frequency is

$$f_{sw} = \frac{1}{\Delta t_1 + \Delta t_2} = \frac{V_{in} - 2y}{8R_{on}C_{fly}k} \tag{4.135}$$

If $k = 0$, the converter will operate at an infinite switching frequency and the trajectory will be maintained on the sliding line $g(x) = 0$. The value of the switching frequency is decreased when the hysteresis window is increased. The control is implemented in *Matlab/Simulink* with a fixed hysteresis to evaluate the sliding mode behavior. The simulations are performed for $k = 0.4$. A load transient of 1 mA and 5 mA is applied at 1 μs and relaxed at 2 μs in Fig. 4.41 and Fig. 4.42 respectively. The output voltage is stabilized around 0.6 V after the reaching mode. In case of a small step of load current a very small undershoot is visible. However in the case of a larger step, an undershoot is visible and the output voltage exhibits a static error. The sliding mode is based on the flying capacitor voltage. When

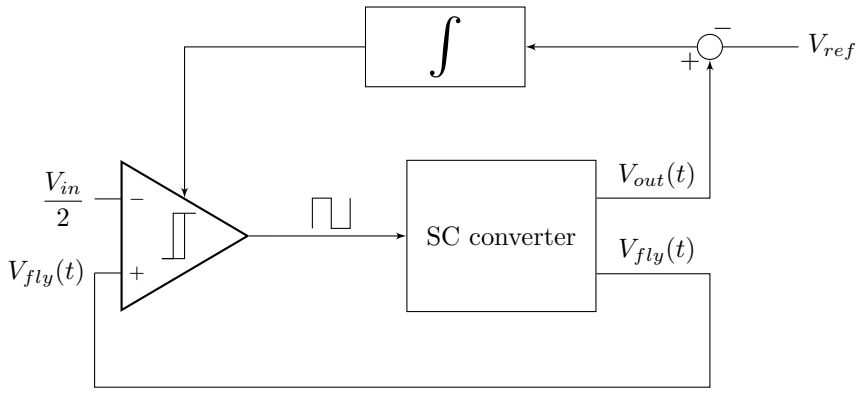


Figure 4.40: Diagram of the loop delay modulation of the sliding mode control with an hysteresis band and rejection of output voltage static error

the converter operates near the FSL region the capacitor voltage is well regulated but the resistive effect introduces more significant voltage drop. This drop is not compensated by the sliding mode. The hysteresis band must be adjusted and an integrator is introduced to address this issue. The diagram is shown in Fig. 4.40. We propose to use the sampled-data modeling to build the small-signal behavior of the control loop.

Let's consider the dynamics of the converter within the n-th cycle. The cycle duration is the switching period T_n. The switching instants between the charging and discharging phases is denoted $t_n + d_n$ and the switching instant between the discharging and charging phase is denoted $t_n + T_n$. The dynamics is given by the state-space model:

$$S_1 : \begin{cases} \dot{x} = A_1 x + B_1 u \\ v_{out} = Ex \\ v_{fly} = Cx \end{cases} \quad \text{for } t \in [t_n, t_n + d_n] \tag{4.136}$$

$$S_2 : \begin{cases} \dot{x} = A_2 x + B_2 u \\ v_{out} = Ex \\ v_{fly} = Cx \end{cases} \quad \text{for } t \in [t_n + d_n, t_n + T_n] \tag{4.137}$$

The switching instants are constrained by the hysteresis band and the sliding surface as follow

$$v_{fly}(t_n + d_n) = Cx(t_n + d_n) = \frac{V_{in}}{2} + k \tag{4.138}$$

$$v_{fly}(t_n + T_n) = Cx(t_n + T_n) = \frac{V_{in}}{2} - k \tag{4.139}$$

The sampled-data model is constructed by sampling the state x at t_n:

$$x_{n+1} = f\left(x_n, u_n, \tau_n\right) \tag{4.140}$$

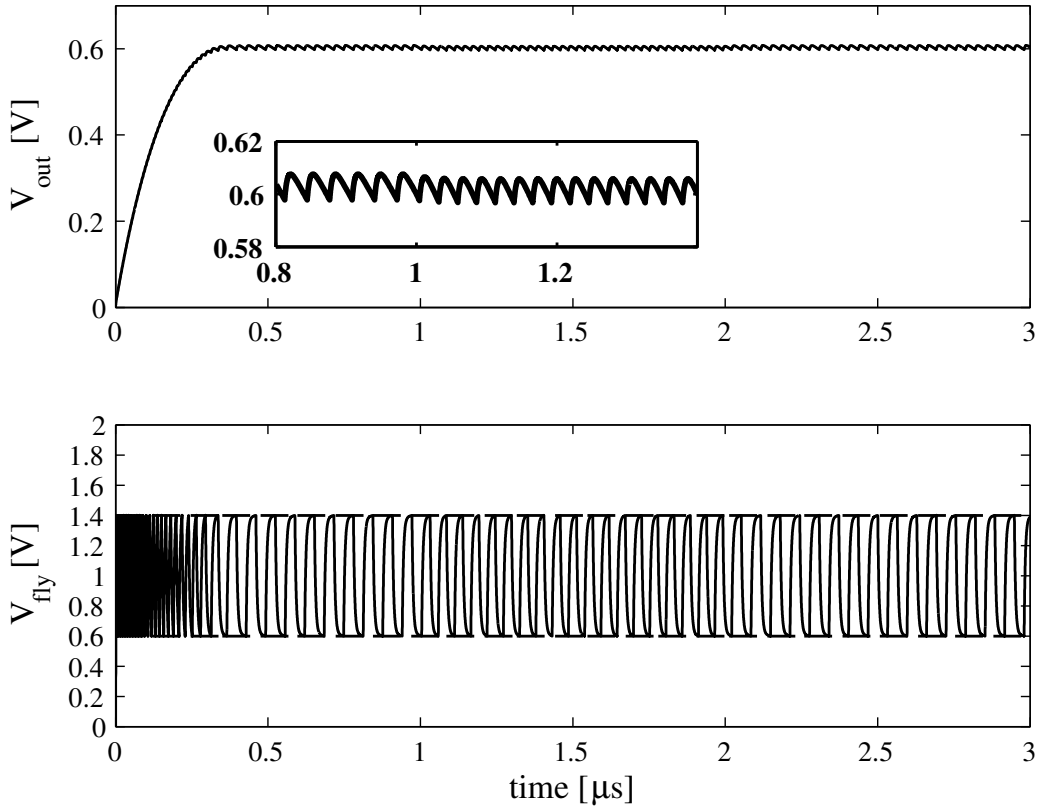


Figure 4.41: Transient simulation with a load transient of 1 mA

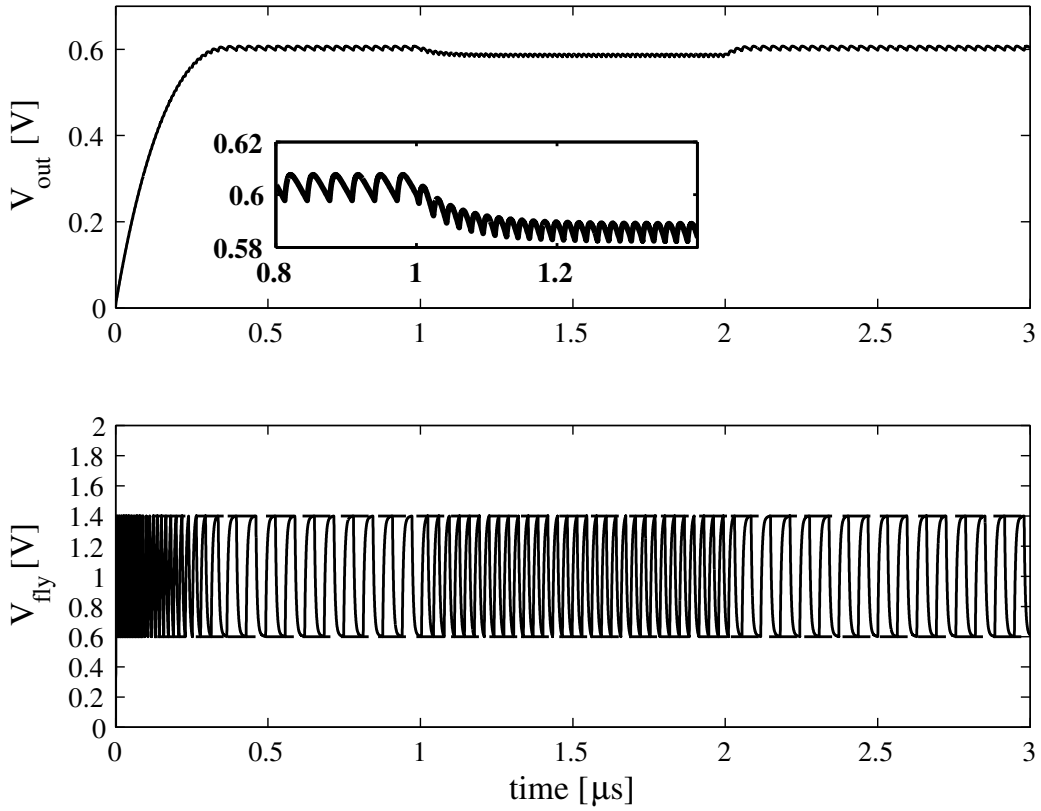


Figure 4.42: Transient simulation with a load transient of 5 mA

$$= \Phi x_n + \Gamma u_n \tag{4.141}$$

$$v_{out_n} = E x_n \tag{4.142}$$

$$v_{fly_n} = C x_n \tag{4.143}$$

The constraint equations are

$$g\left(x_n, u_n, \tau_n, k_n\right) = \begin{bmatrix} v_{fly}(t_n + d_n) - \frac{V_{in}}{2} - k \\ v_{fly}(t_n + T_n) - \frac{V_{in}}{2} + k \end{bmatrix} \tag{4.144}$$

$$= \begin{bmatrix} Cx(t_n + d_n) - \frac{V_{in}}{2} - k \\ Cx(t_n + T_n) - \frac{V_{in}}{2} + k \end{bmatrix} \tag{4.145}$$

$$= 0 \tag{4.146}$$

The fixed point is now $\left(x^0(0), U, (d, T)', k\right)$ and satisfies

$$x^0(0) = f\left(x^0(0), U, (d, T)'\right) \tag{4.147}$$

$$g\left(x^0(0), U, (d, T)', k\right) = 0 \tag{4.148}$$

The fixed point is determined for a targeted output voltage with

$$E x^0(0) - V_{target} = 0 \tag{4.149}$$

The equations (4.147), (4.148) and (4.149) are solved for a given value of U using the Levenberg-Marquardt algorithm implemented in *Matlab*. The solutions are:

$$x^0(0) = \begin{pmatrix} 0.6022 & 0.6 \end{pmatrix}' \tag{4.150}$$

$$d = 3.1824 \cdot 10^{-8} \tag{4.151}$$

$$T = 6.3649 \cdot 10^{-8} \tag{4.152}$$

$$k = 0.3978 \tag{4.153}$$

The system is now linearized around the fixed-point solution to obtain the small-signal model:

$$\hat{x}_{n+1} \approx \frac{\partial f}{\partial x_n}\hat{x}_n + \frac{\partial f}{\partial u_n}\hat{u}_n + \frac{\partial f}{\partial \tau_n}\hat{\tau}_n \tag{4.154}$$

$$0 \approx \frac{\partial g}{\partial x_n}\hat{x}_n + \frac{\partial g}{\partial u_n}\hat{u}_n + \frac{\partial g}{\partial \tau_n}\hat{\tau}_n + \frac{\partial g}{\partial k_n}\hat{k}_n \tag{4.155}$$

From (4.155), we have

$$\hat{\tau}_n \approx \left(-\frac{\partial g}{\partial \tau_n}\right)^{-1}\left[\frac{\partial g}{\partial x_n}\hat{x}_n + \frac{\partial g}{\partial u_n}\hat{u}_n + \frac{\partial g}{\partial k_n}\hat{k}_n\right] \tag{4.156}$$

and injecting (4.156) into (4.154)

$$\begin{aligned}\hat{x}_{n+1} &\approx \Phi_0\hat{x}_n + \Gamma_u\hat{u}_n + \Gamma_k\hat{k}_n \\ \hat{v}_{out} &= E\hat{x}_n \\ \hat{v}_{fly} &= C\hat{x}_n\end{aligned} \tag{4.157}$$

with

$$\Phi_0 = \frac{\partial f}{\partial x_n} - \frac{\partial f}{\partial \tau_n}\left(\frac{\partial g}{\partial \tau_n}\right)^{-1}\frac{\partial g}{\partial x_n} \tag{4.158}$$

$$\Gamma_u = \frac{\partial f}{\partial u_n} - \frac{\partial f}{\partial \tau_n}\left(\frac{\partial g}{\partial \tau_n}\right)^{-1}\frac{\partial g}{\partial u_n} \tag{4.159}$$

$$\Gamma_k = -\frac{\partial f}{\partial \tau_n}\left(\frac{\partial g}{\partial \tau_n}\right)^{-1}\frac{\partial g}{\partial k_n} \tag{4.160}$$

$$\frac{\partial f}{\partial x_n} = \Phi_2\Phi_1 \tag{4.161}$$

$$\frac{\partial f}{\partial u_n} = \Phi_2\Gamma_1 + \Phi_1 \tag{4.162}$$

$$\frac{\partial f}{\partial \tau_n} = \begin{bmatrix} \Phi_2(\dot{x}^0(d^-) - \dot{x}^0(d^+)) & \dot{x}^0(T^-) \end{bmatrix} \tag{4.163}$$

$$\frac{\partial f}{\partial k_n} = 0 \tag{4.164}$$

$$\frac{\partial g}{\partial x_n} = \begin{bmatrix} C\Phi_1 \\ C\Phi_2\Phi_1 \end{bmatrix} \tag{4.165}$$

$$\frac{\partial g}{\partial u_n} = \begin{bmatrix} C\Gamma_1 \\ C\left(\Phi_2\Gamma_1 + \Phi_1\right) \end{bmatrix} - \begin{bmatrix} 0 & 0.5 \\ 0 & 0.5 \end{bmatrix} \tag{4.166}$$

$$\frac{\partial g}{\partial \tau_n} = \begin{bmatrix} C\dot{x}^0(d^-) & 0 \\ C\Phi_2\left(\dot{x}^0(d^-) - \dot{x}^0(d^+)\right) & C\dot{x}^0(T^-) \end{bmatrix} \tag{4.167}$$

$$\frac{\partial g}{\partial k_n} = \begin{bmatrix} -1 \\ +1 \end{bmatrix} \tag{4.168}$$

The stability of the system is checked looking at Eigenvalues of Φ_0:

$$eig[\Phi_0] = \begin{pmatrix} 0.0118 \\ 0 \end{pmatrix} \tag{4.169}$$

The system is thus a first order system with an Eigenvalue module of 0.0118. This value is closed to zero leading to a fast transient behavior. The control-to-output voltage transfer function as well as the audio susceptibility and the output impedance are derived in the z-domain from (4.157)

$$T_{oc}(z) = \frac{\hat{v}_{out}(z)}{\hat{k}(z)} = E(zI - \Phi_0)^{-1}\Gamma_k \tag{4.170}$$

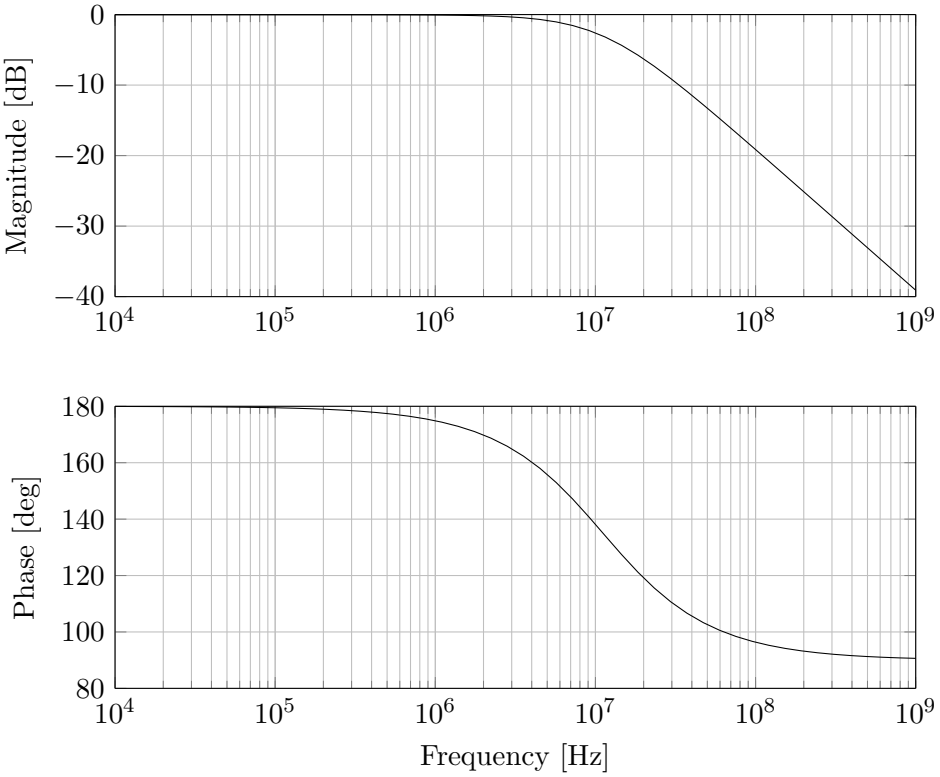


Figure 4.43: Control-to-output transfer function

$$T_{oi}(z) = \frac{\hat{v}_{out}(z)}{\hat{i}_{load}(z)} = E(zI - \Phi_0)^{-1}\Gamma_{u_{1,*}} \tag{4.171}$$

$$T_{ov}(z) = \frac{\hat{v}_{out}(z)}{\hat{v}_{in}(z)} = E(zI - \Phi_0)^{-1}\Gamma_{u_{2,*}} \tag{4.172}$$

Then the transfer functions are expressed in s-domain using the Zero Order hold method. The control-to-output transfer function is shown in Fig. 4.43. The audio susceptibility and the output impedance with the sliding-mode are compared to the open-loop case in Fig. (4.44) and Fig. (4.45) respectively. The pole in the sliding mode case is higher than in the open-loop one. The output impedance is much lower than in the open loop case but must be further reduced in DC to avoid the static error. Moreover the audio susceptibility has a higher bandwidth than in the open-loop case due the fast loop of the sliding-mode. Unfortunately this means that all perturbations from the input voltage will be found in the output voltage.

The control-to-output transfer function has a DC gain closed to zero and a high frequency pole. We propose to use a simple integrator with time constant, $T_i = 1\ \mu s$, significantly lower than the time constant of the control-to-output transfer function, $\tau_0 = 14.27\ ns$. The simulations of the strategy in Fig. 4.40 are performed in *Matlab* with the PWL model. A load transient of 5 mA is applied at 10 μs and relaxed

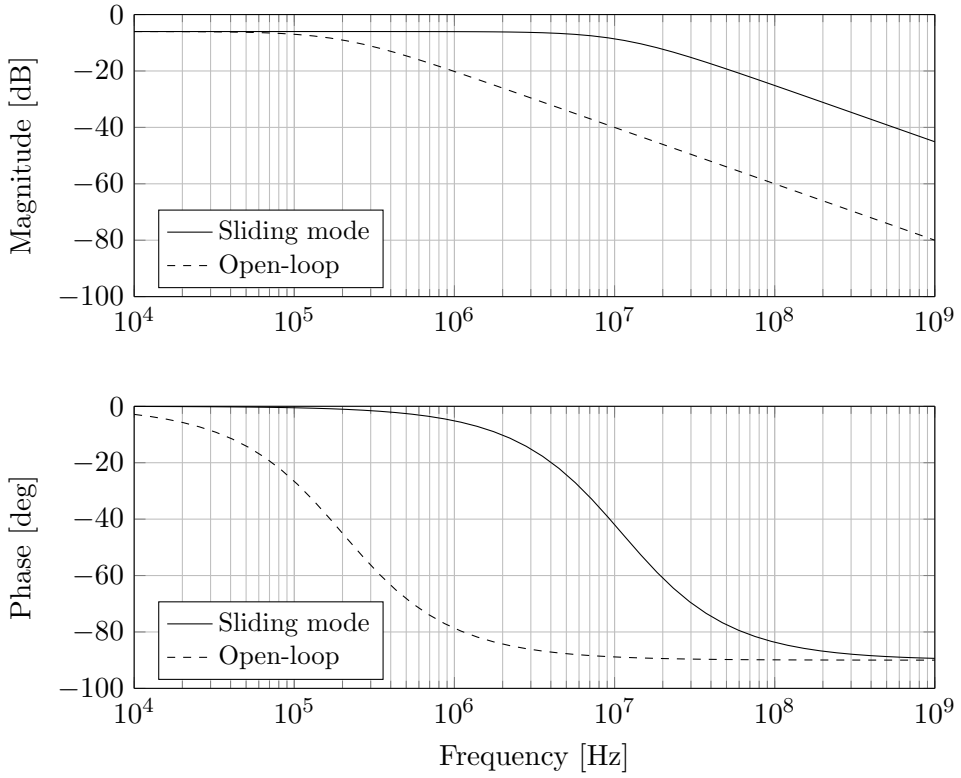


Figure 4.44: Audio susceptibility of the sliding-mode without the external loop and of the open-loop power stage

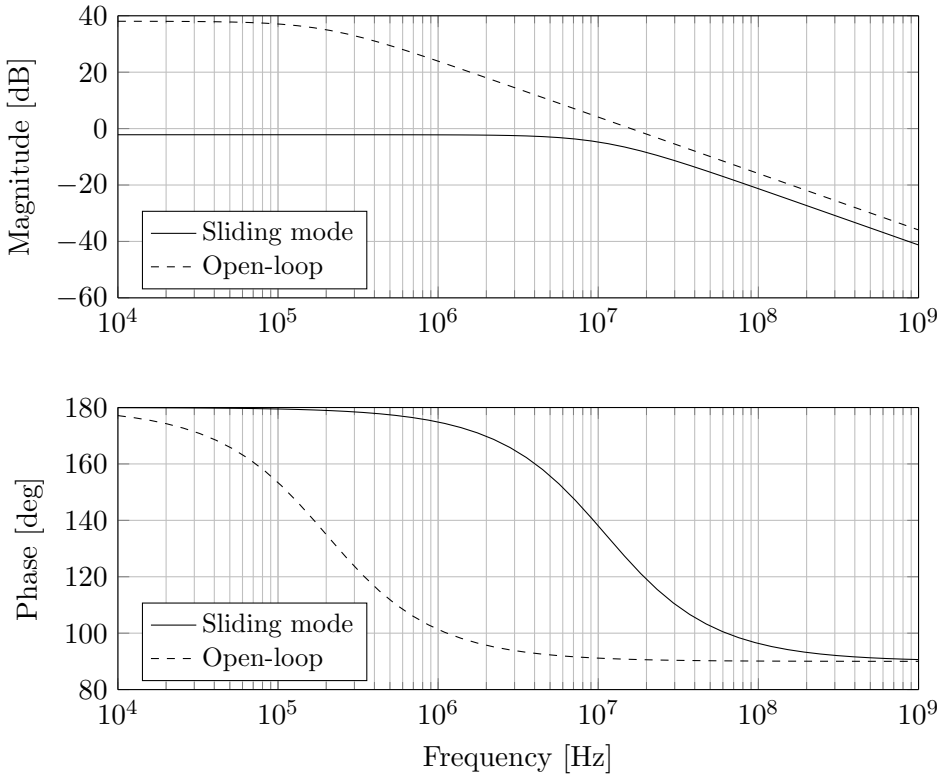


Figure 4.45: Output impedance of the sliding-mode without the external loop and of the open-loop power stage

at 15 μs as shown in Fig. 4.46. The voltage drop is not improved but the output voltage reaches the targeted value after a small recovery time depending on the integration time constant. At start up, the integrator value is null and the hysteresis window tends to zero. The controller is saturated to the minimum value of the hysteresis window and an overshoot appears on the output voltage. Line transient sensitivity is also evaluated in Fig. 4.47. The input voltage is increased to 2.2 V at 10 μs and decreases to 2 V at 15 μs. The sliding surface follows the perturbation as well as the hysteresis window. After the recovery time, the hysteresis window is corrected by the slow external loop in the controller.
Sliding mode control with hysteresis window modulation demonstrates good performances but the linear loop introduced to cancel the static error modifies the startup behavior and saturates the loop. An anti-windup is a possible solution to deal with the error accumulation during saturation. A lower integration time constant could help but the transient behavior would be slower. Moreover the sliding surface is defined for $V_{in}/2$ but it is usually implemented with a voltage reference. If this voltage reference is inaccurate the charging and discharging phases will not be balanced leading to more charge transfer losses. Another implementation is therefore proposed to address these issues.

4.6 Sliding-mode with relative hysteresis band

In the previous section the switching frequency of the sliding mode operation is modulated through the hysteresis of the comparator. The motion of the converter is defined with (4.132). The induced mode shows for a given value of k that:

$$V_{fly} = \begin{cases} V_{out} & \text{for } g(x) = -k \\ V_{in} - V_{out} & \text{for } g(x) = +k \end{cases} \tag{4.173}$$

As a consequence the voltage across the flying capacitor can be set by two independent boundaries, V_l and V_h to force the induced mode:

$$V_l = V_{ref} \tag{4.174}$$

$$V_h = V_{in} - V_{ref} \tag{4.175}$$

The schematic implementation of such a control is depicted in Fig. 4.48. The flying capacitor voltage, V_{fly}, is sensed by subtracting the top capacitor voltage, V_{top} and the bottom capacitor voltage, V_{bot}. Two comparators and an RS flip-flop are used to constrain the flying capacitor voltage. When the flying capacitor voltage reaches the lower bound, the flip-flop is reset and the converter goes in the charging phase. Similarly when the voltage reaches the upper bound, the flip-flop is set and

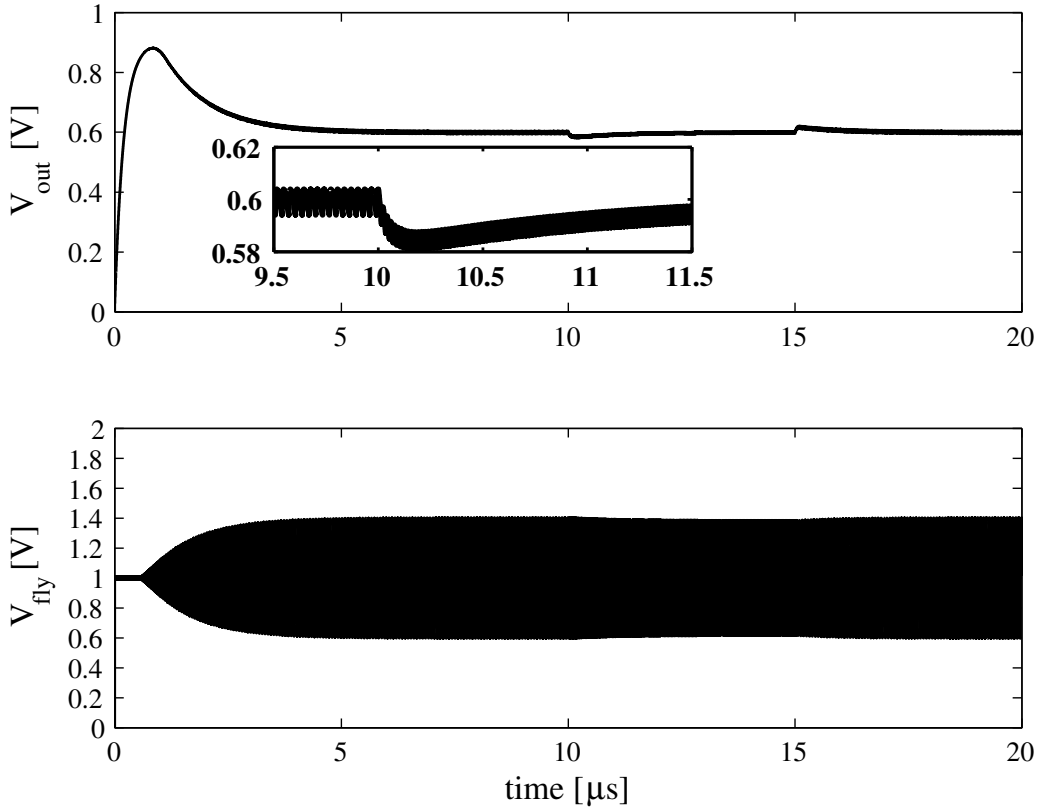


Figure 4.46: Load transient simulation (sliding mode in Fig. 4.40) with a 5 mA load step

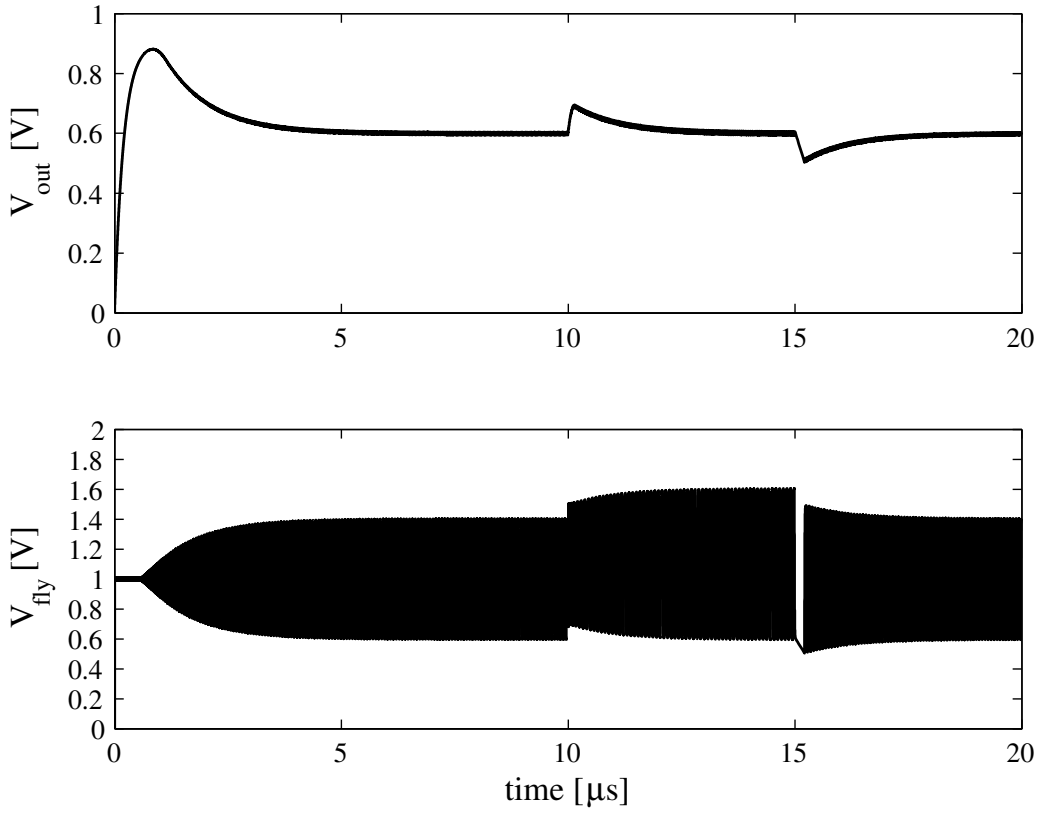


Figure 4.47: Line transient simulation (sliding mode in Fig. 4.40) with an input voltage step of 10%

the converter returns to the discharging phase. By this way the sliding surface is the same but the sliding mode operation is now independent of the averaged value of the flying capacitor. As well as in the previous Section, the converter can be

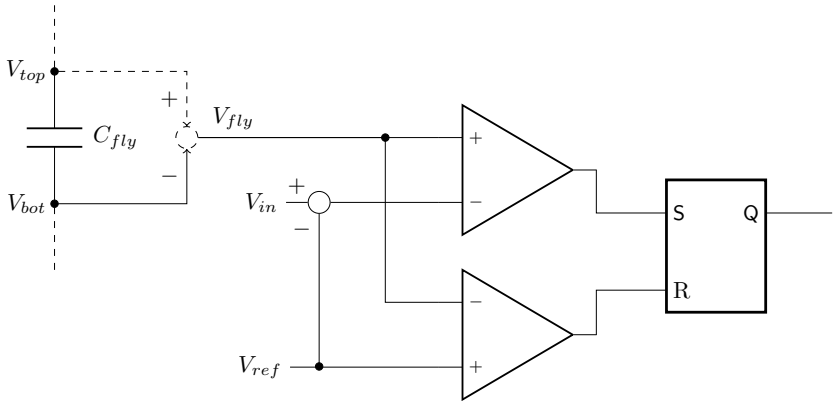


Figure 4.48: Diagram of control through the steady-state voltage across the flying capacitor

modeled with the sampled-data modeling approach. The dynamics of the variable state-space model is given by (4.136) and (4.137). The switching instants are now constrained as follows:

$$v_{fly}(t_n + d_n) = Cx(t_n + d_n) = V_{in} - V_{ref} \tag{4.176}$$

$$v_{fly}(t_n + T_n) = Cx(t_n + T_n) = V_{ref} \tag{4.177}$$

The sampled-data model is constructed by sampling the state x at t_n:

$$x_{n+1} = f\left(x_n, u_n, \tau_n, v_{ref_n}\right) \tag{4.178}$$

$$v_{out} = Ex_n \tag{4.179}$$

$$v_{fly} = Cx_n \tag{4.180}$$

the constraint equations are thus:

$$g\left(x_n, u_n, \tau_n, v_{ref_n}\right) = \begin{bmatrix} v_{fly}(t_n + d_n) - V_{in} + V_{ref} \\ v_{fly}(t_n + T_n) - V_{ref} \end{bmatrix} \tag{4.181}$$

$$= \begin{bmatrix} Cx(t_n + d_n) - V_{in} + V_{ref} \\ Cx(t_n + T_n) - V_{ref} \end{bmatrix} \tag{4.182}$$

$$= 0 \tag{4.183}$$

The fixed point, $\left(x^0(0), U, (d, T)', V_{ref}\right)$, is determined for a given targeted output voltage, V_{target}, by the following set of equations:

$$x^0(0) = f\left(x^0(0), U, (d, T)'\right) \tag{4.184}$$

$$g\left(x^0(0), U, (d,T)', V_{ref}\right) = 0 \tag{4.185}$$

$$Ex^0(0) - V_{target} = 0 \tag{4.186}$$

The Levenberg-Marquardt algorithm gives:

$$x^0(0) = \begin{pmatrix} 0.6022 & 0.6 \end{pmatrix}' \tag{4.187}$$

$$d = 3.1824 \cdot 10^{-8} \tag{4.188}$$

$$T = 6.3649 \cdot 10^{-8} \tag{4.189}$$

$$V_{ref} = 0.6022 \tag{4.190}$$

The solutions in (4.187) and (4.150) are identical, yielding to the same switching instant values. The system is linearized around the fixed-point solution:

$$\hat{x}_{n+1} \approx \frac{\partial f}{\partial x_n}\hat{x}_n + \frac{\partial f}{\partial u_n}\hat{u}_n + \frac{\partial f}{\partial \tau_n}\hat{\tau}_n \tag{4.191}$$

$$0 \approx \frac{\partial g}{\partial x_n}\hat{x}_n + \frac{\partial g}{\partial u_n}\hat{u}_n + \frac{\partial g}{\partial \tau_n}\hat{\tau}_n + \frac{\partial g}{\partial v_{ref_n}}\hat{v}_{ref_n} \tag{4.192}$$

Similarly as in the previous Section, (4.191) and (4.192) are combined giving:

$$\begin{aligned} \hat{x}_{n+1} &\approx \Phi_0\hat{x}_n + \Gamma_u\hat{u}_n + \Gamma_r\hat{v}_{ref_n} \\ \hat{v}_{out} &= E\hat{x}_n \\ \hat{v}_{fly} &= C\hat{x}_n \end{aligned} \tag{4.193}$$

The values of Φ_0, Γ_u, $\frac{\partial f}{\partial x_n}$, $\frac{\partial f}{\partial u_n}$, $\frac{\partial f}{\partial \tau_n}$, $\frac{\partial f}{\partial v_{ref_n}}$, $\frac{\partial g}{\partial x_n}$, $\frac{\partial g}{\partial \tau_n}$ are the same as in the previous Section and

$$\Gamma_r = -\frac{\partial f}{\partial \tau_n}\left(\frac{\partial g}{\partial \tau_n}\right)^{-1}\frac{\partial g}{\partial v_{ref_n}} \tag{4.194}$$

and

$$\frac{\partial g}{\partial u_n} = \begin{bmatrix} C\Gamma_1 \\ C\left(\Phi_2\Gamma_1 + \Phi_1\right) \end{bmatrix} - \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} \tag{4.195}$$

$$\frac{\partial g}{\partial v_{ref_n}} = \begin{bmatrix} +1 \\ -1 \end{bmatrix} \tag{4.196}$$

The audio susceptibility and the output impedance are given by (4.171) and (4.172) respectively and the control-to-output transfer function is

$$T_{oc}(z) = \frac{\hat{v}_{out}(z)}{\hat{v}_{ref}(z)} = E(zI - \Phi_0)^{-1}\Gamma_r \tag{4.197}$$

The Bode diagram of the control-to-output transfer function is shown in Fig. 4.49.

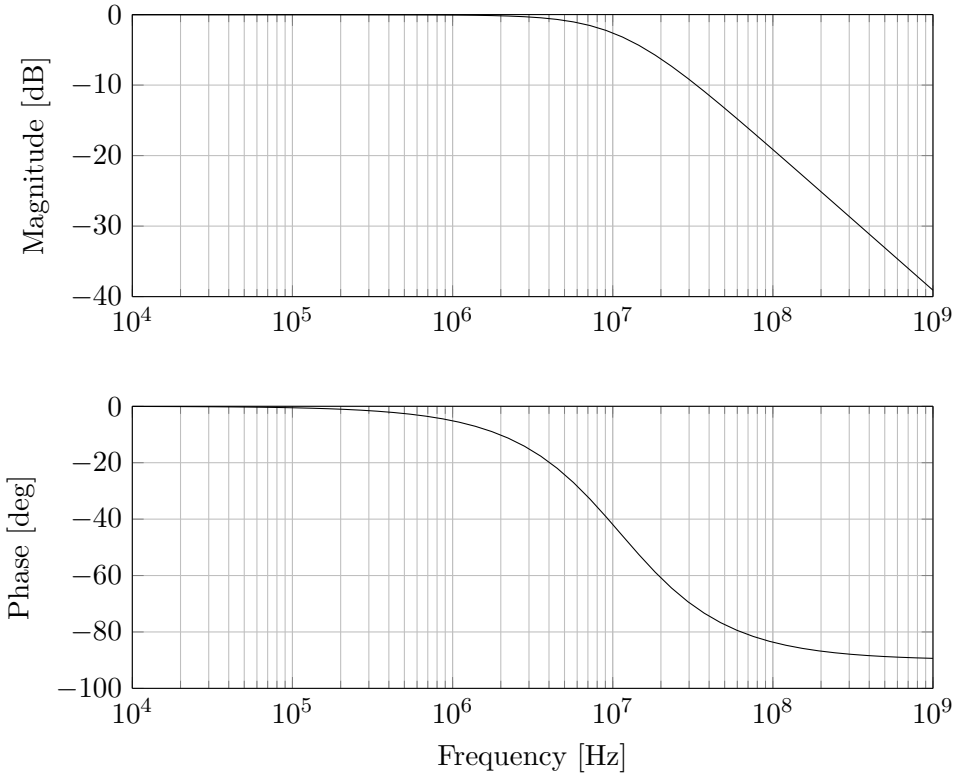


Figure 4.49: Control-to-output transfer function

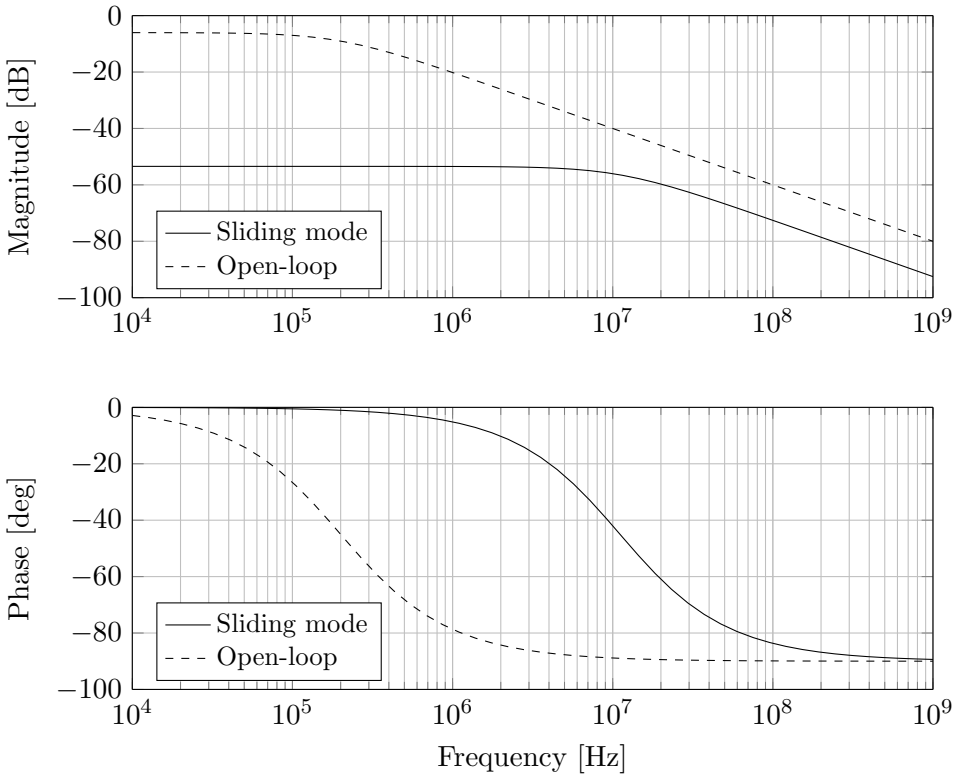


Figure 4.50: Audio susceptibility of the sliding-mode without the external loop and of the open-loop power stage

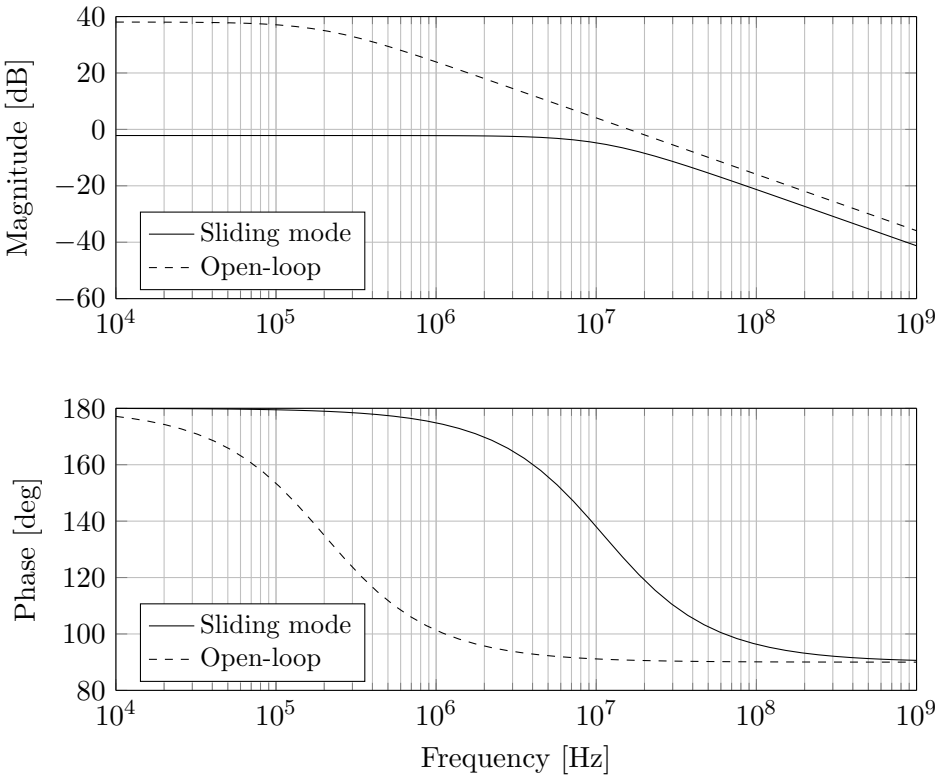


Figure 4.51: Output impedance of the sliding-mode without the external loop and of the open-loop power stage

The audio susceptibility and the output impedance are compared to the open-loop power stage in Fig. 4.50 and Fig. 4.51 respectively. The audio susceptibility has been significantly improved. The DC gain around -60 dB means that the input perturbation will be attenuated by a factor of 1000. The output impedance is the same as in Fig. 4.45 and a linear loop is also required to lower the DC value. The schematic of the proposed compensation technique is depicted in Fig. 4.52. The output voltage is subtracted to a voltage reference to produce an error signal. The error signal is integrated to provide the lower and upper bound references. The compensator function can be a simple integrator because the control-to-output transfer function has a DC gain near the unity and the pole is situated in high frequency. For example, the bandwidth of the open-loop is set to the same value as in the linear voltage loop in Section 4.2. The integration time constant is thus $T_i = \tau_0 = 796$ ns. Load transients are performed in *Matlab/Simulink* and the results are presented in Fig. 4.53. The startup is slower than in the case of the sliding mode without external loop but there is no overshoot on the output voltage. At startup the integrator output is null, the hysteresis window is wide and the converter starts slowly. One good practice to decrease the starting time is to use

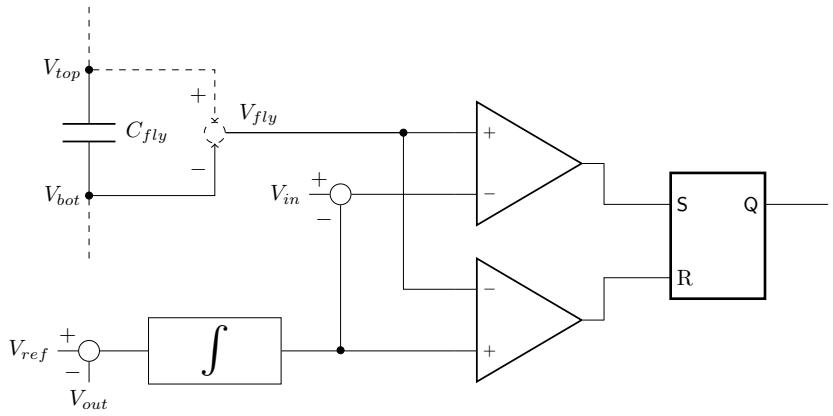


Figure 4.52: Diagram of control through the steady-state voltage across the flying capacitor with a linear loop

a compensator comprising a pole at the origin and a zero. At the beginning the output of the compensator will be the error signal that will set the output voltage near the desired value. The zero is placed at $1 \cdot 10^7\ rad/s$ to increase the phase in a reasonable amount and the transient simulation is presented in Fig. 4.54. Both the startup and recovery time are improved by this way. The line transient behavior is evaluated in Fig. 4.55 for the integral external loop. The input voltage is increased to 2.2 V at 10 μs. The lower bound remains to its value while the upper bound is immediately increased. No change is visible in the output voltage except the ripple value that has been increased since the switching frequency has decreased. At 15 μs the input voltage returns to 2 V. The output voltage is not perturbed as well. Thus the input voltage acts like a feed-forward and the converter becomes insensitive to the line perturbations.

4.7 Conclusion

Linear and non-linear control have been analyzed. Linear frequency modulation with a voltage loop is very simple to implement since it requires an operational amplifier and a VCO. The transient performances can be increased by adding a current loop. Nonetheless the current loop control is more difficult to design and the implementation is also complex. The robustness is therefore lower. Sliding mode control can drastically improve both transient behavior and robustness but requires a voltage observer for the flying capacitor. Finally voltage loop control works for an interleaving architecture when a multiphase VCO is considered while sliding mode control cannot address this need for now.

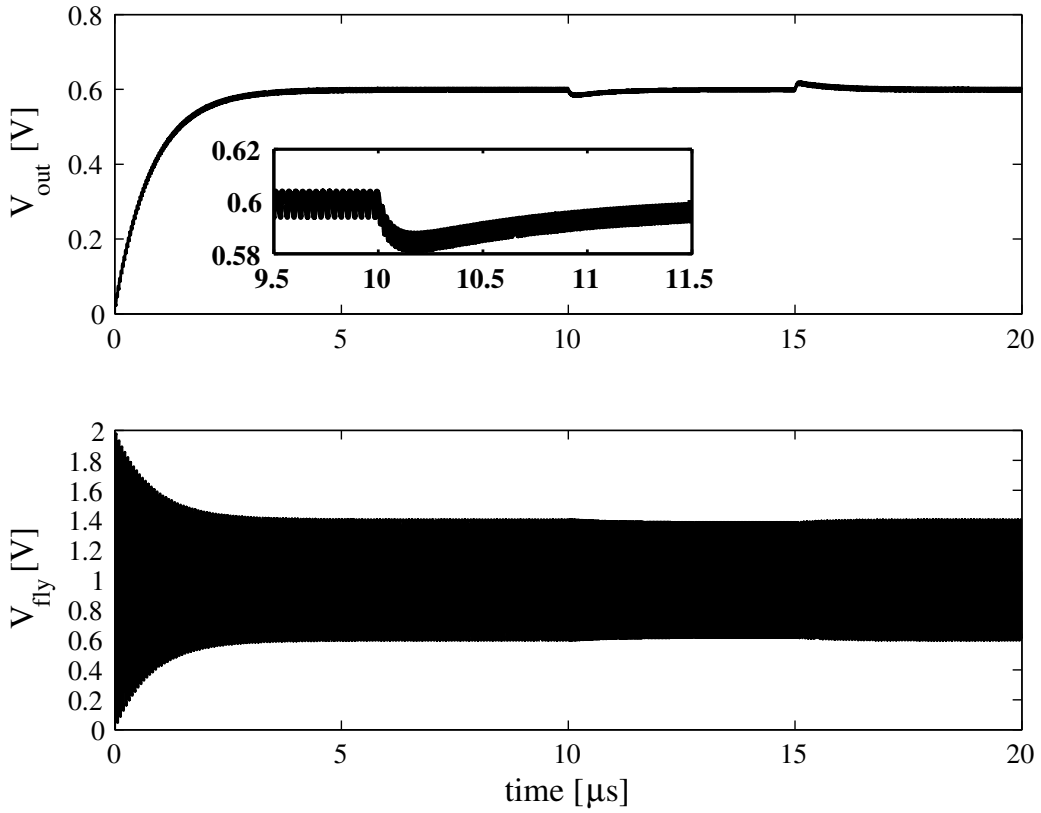


Figure 4.53: Load transient simulation with integral external loop

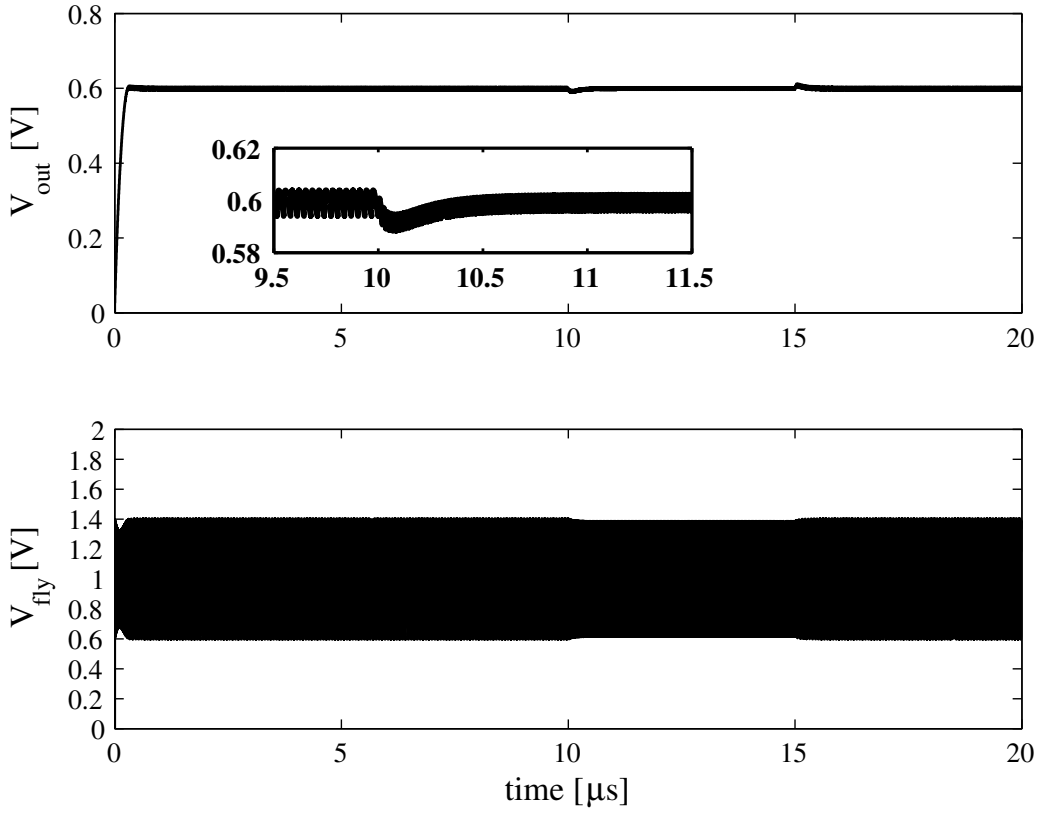


Figure 4.54: Load transient simulation with PI external loop

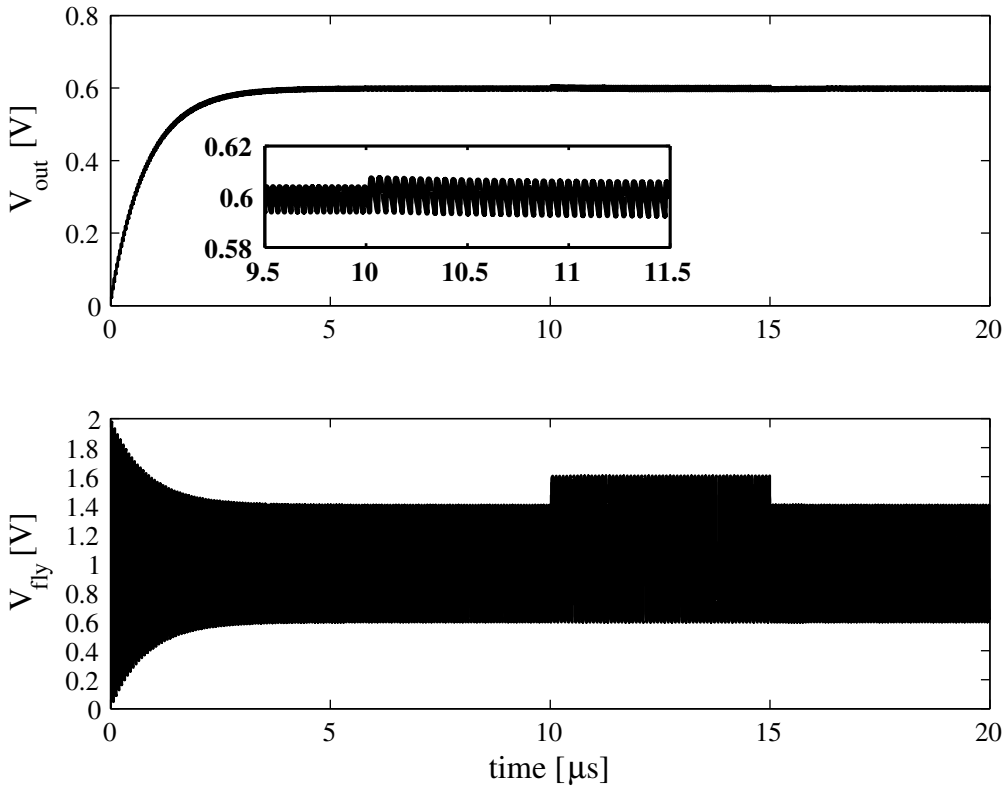


Figure 4.55: Line transient simulation with integral external loop

CHAPTER 5

Proprosed SC converter

5.1 FDSOI technology

UTBB[1] FDSOI technology has been introduced to reduce the manufacturing complexity from 28nm node and below while keeping the benefits of scaling. Unlike tri-gate process, the FDSOI technology does not change the genuine geometric dimension of the transistor. A thin layer of insulator is added below the channel that eliminates the need to add dopants in the channel. This layer is so-called the buried oxide. The silicon layer over the oxide is very thin and the channel is thus fully depleted. This approach is called the ultra thin body and buried oxide technology. The overview of a transistor in FDSOI in shown in Fig. 5.1. The effective length of

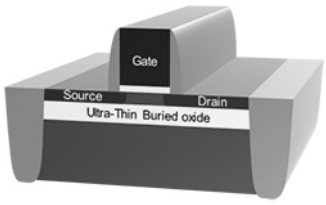


Figure 5.1: Overview of the FDSOI technology

the channel and the parasitic capacitors are reduced compare to the case of the bulk technology and enhance the performances of the transistor. In addition the thin oxide creates a buried gate below the channel acting like a second but less efficient gate. This second gate can be used for body-biasing as detailed in Chapter 6. The thin oxide also eliminates the latch-up issue.
The 28nm FDSOI technology offers both two voltage devices and two possible

[1]Ultra thin body & buried oxide

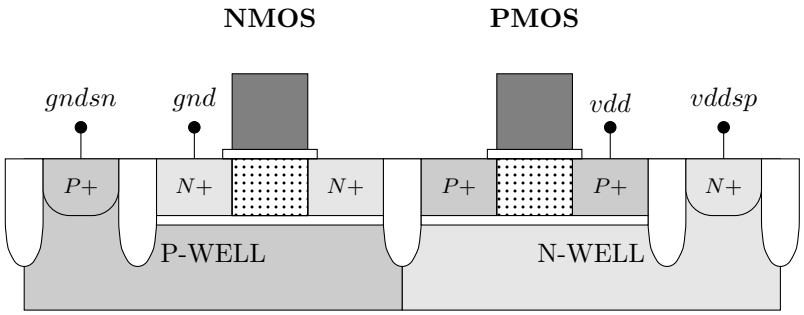


Figure 5.2: Regular threshold voltage architecture

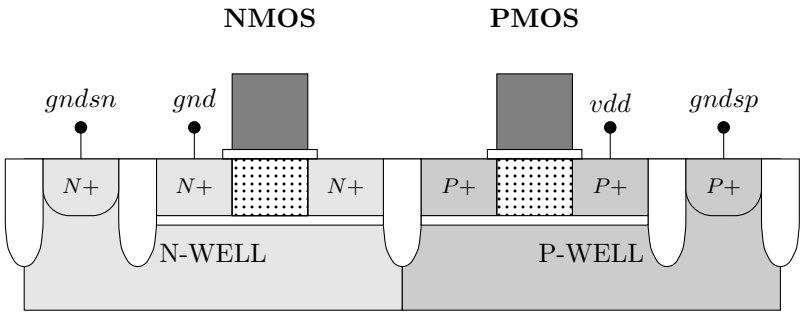


Figure 5.3: Low threshold voltage architecture

threshold voltages. The thickness of the gate oxide sets the voltage sustained by the device while the threshold voltage is controlled by the type of the well under the BOX. Thin oxide devices sustain voltage up to 1 V and thick oxide devices, 1.8 V. Regular threshold voltage devices are built with a P-well under the BOX of the NMOS transistor and N-well under the BOX[2] of the PMOS as depicted in Fig. 5.2. The P-well voltage is tied to ground and the N-well voltage is connected to the power supply in normal operation of the transistor. The wells are flipped in the low threshold voltage device architecture. A N-well is implemented under the BOX of the NMOS transistor and a P-well under the BOX of the PMOS transistor. P-well and the N-well voltages must be both tied to ground for normal operation of the transistors. This flexibility offers high voltage devices with low threshold voltage without any extra mask penalty unlike in bulk process.

5.2 Architecture description

The power supply strategy described in Section 2.8 calls for a modular architecture. Flexibility in the SC converter implementation relaxes the constraint on the digital block place & route and ensures maximum compatibility. The proposed architecture of the embedded SC converter in 28nm FDSOI technology is depicted in Fig. 5.4.

[2]Buried oxide

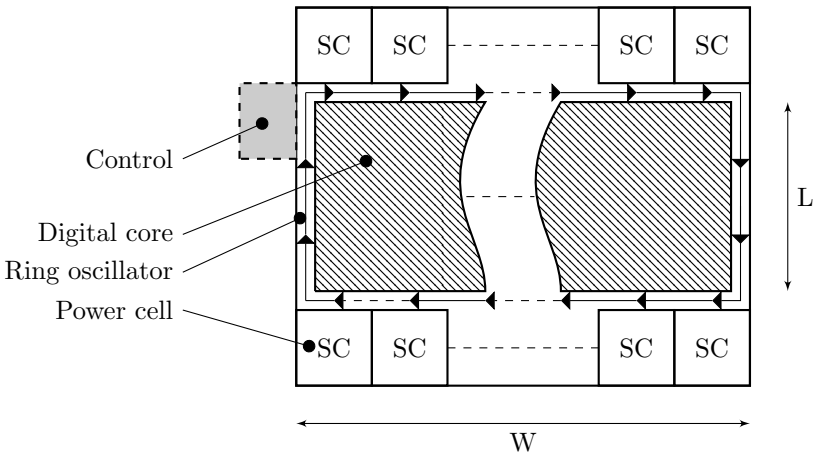


Figure 5.4: Diagram of the multiphase ring oscillator.

The flying capacitors using MIM devices are inserted with the local power grid just above the digital block to supply. The power switch cells are distributed horizontally on each side of the converter. A converter cell comprises a set of one or more flying capacitors depending on the requested voltage ratio. Cells can be abutted side by side in order to cover the entire digital block and interleaved to mitigate the output voltage ripple of the converter. The number of cells depends on the value of W in Fig. 5.4. A ring oscillator surrounding the digital area provides the interleaved clocks to the converter cells. The ring oscillator can easily be adjusted according to the number of converter cells to offer design flexibility. A linear frequency modulation with a voltage loop is selected. The switching frequency is controlled by the supply voltage of the ring oscillator and the controller can be inserted either on the left or the right side of the ring oscillator.

5.3 The power stage

5.3.1 Converter cell

A multi-ratio cell is necessary in order to maximize the efficiency over a wide range of output voltage and load current. Efficiency is always higher and the output resistance always lower for SC converters having a reduced number of flying capacitors. A large number of flying capacitors means a large number of switches to arrange the capacitors over the various ratios leading to more switching losses. Series-parallel topologies make better use of the capacitors than Ladder or Dickson structures [74]. Capacitor density is often the most important parameter in SC converter design and that is the reason why Series-parallel topologies are widely used. An output voltage range of 0 V to 1.2 V from an input voltage of 1.8 V requests four converter ratios:

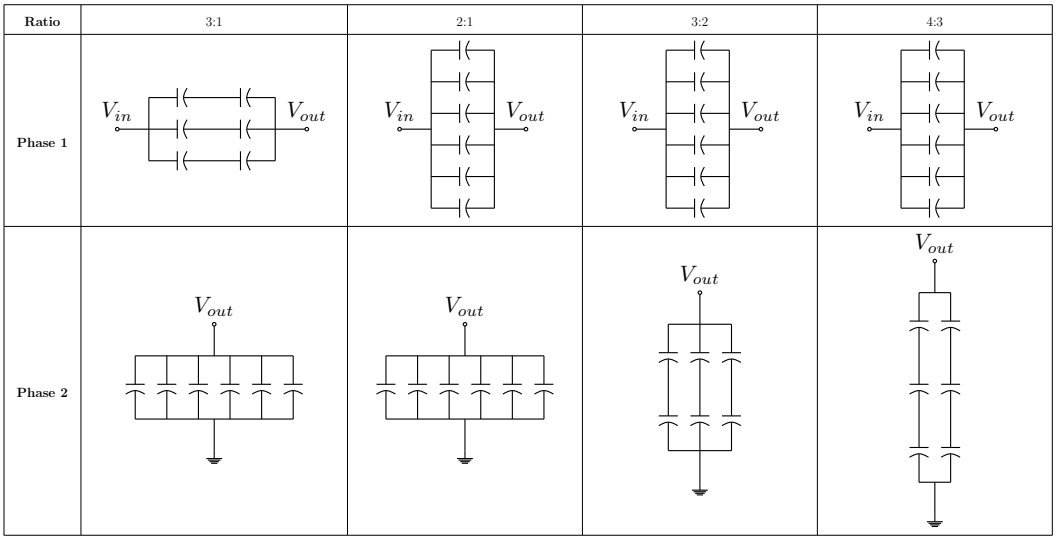


Figure 5.5: Configurations of the flying capacitor over the different ratio

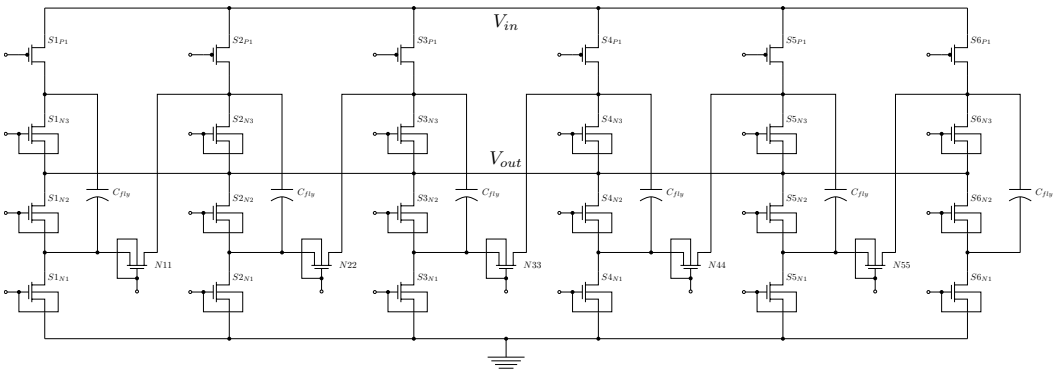


Figure 5.6: Converter cell with 6 flying capacitors and 29 switches

3:4, 2:3, 1:2 and 1:3 to provide an ideal output voltage of 1.35 V, 1.2 V, 0.9 V and 0.6 V respectively. The 2:3 ratio will deliver an output voltage less than 1.2 V under load condition and the 3:4 ratio will thus be used to provide this voltage. The Series-parallel implementation for the 2:3, 1:2 and 1:3 ratios needs two flying capacitors while the 3:4 ratio required an extra flying capacitor. As a consequence six flying capacitors are implemented and arranged to provide the various ratios while maximizing the capacitor usage as shown in Fig. 5.5. The flying capacitors are arranged through a set of 29 switches and the implementation of the unit cell in FDSOI is depicted in Fig. 5.6. The driving and the clocking schemes are challenging in SC converters. The gate voltage of some switches have to be boosted to ensure a proper operation. Unfortunately those particular driving schemes increase the complexity, the reliability issues and the power consumption. FDSOI technology offers more flexibility. Thick oxide devices are used to sustain a high input volt-

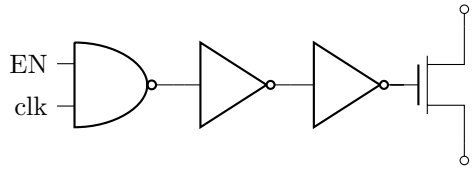


Figure 5.7: Converter cell with 6 flying capacitors and 29 switches

	I_{on}/I_{off}	R_{on}	C_{gate}
Normal	13.8 10^6	8.5 Ω	100 fF
Foward biasing	17.6 10^3	5.8 Ω	100 fF
DT scheme	17.3 10^6	5.8 Ω	128 fF

Table 5.1: I_{on}/I_{off} ratio, R_{on} and C_{gate} values comparison for the various configurations of the power switch with dynamic threshold in 28nm FDSOI

age up to 1.8 V with the flip-well architecture in Fig. 5.3. The high-side PMOS switches are easily controlled between 0 V and 1.8 V. The P-well is not isolated and directly tied to ground through the substrate for the sake of space. A special configuration is used for the N-well. The flip-well architecture is also selected to provide a low threshold voltage devices and the gate is connected to the back-plane. By the way when the transistor is turned-on, a voltage of 1.8 V is applied to the N-well. The transistor is forward-biased so that threshold voltage is lowered. On the contrary when the transistor is turned-off, the back-plane is tied to ground and the threshold voltage raises-up to the nominal value. This configuration is so-called the dynamic threshold scheme. Table 5.1 shows the performances of the switch configurations in terms of I_{on}/I_{off}, R_{on} and C_{gate} for the normal, forward biased and dynamic threshold voltage schemes. The results are extracted from circuit simulations for each configurations. The dynamic threshold voltage configuration exhibits the highest I_{on}/I_{off} ratio while maintaining a low on-state resistance of the switches. The forward-biasing technique is not suitable since the I_{on}/I_{off} ratio is degraded. The dynamic threshold voltage scheme increases the parasitic capacitance of the gate due to the BOX and the N-well and P-well junctions. C_{gate} increases by 28% while R_{on} decreases by 32% and the I_{on}/I_{off} ratio increases by 21% compared to normal voltage scheme. This implementation delivers an efficient switch with an ultra low-threshold voltage around 100 mV. Thanks to the flip-well architecture, no triple-well scheme is required and the silicon area is preserved. Moreover the floating switches can be driven between 0 V and 1.8 V without any special assist-circuit. The power switches are driven by an inverter chain. A nand gate enables or disables the switches depending on the selected ratio. The unit switch is depicted

in Fig. 5.7. Several units are associated in parallel to produce a discrete variable transistor width.

5.3.2 Power grid and MIM capacitor implementation

The MIM and the power grid routing are a major concern for this architecture. MIM capacitors are situated between the top thickest metal levels in the 28nm FDSOI process. The typical capacitor density is 20 $^{fF}/_{\mu m^2}$. The top metal levels exhibit a low sheet-resistance that is necessary to build the power grid of digital blocks. The plates of the MIM capacitors are connected only to the upper levels instead of both lower and upper level in order to save a mask. Since MIM capacitors are primarily used for decoupling strategy, it does not alter the power grid design. Unfortunately the usage is not exactly the same for the SC converter. The plates must be connected to switch cells instead to the power supply rail. The bottom plate exhibits a low sheet-resistance allowing connection at the edge of the capacitor close to the switch cell. This is not the case regarding the top plate sheet resistance. The large value of resistance requires an extra metal rail in the top level to maintain the ESR as low as possible. The insertion of the MIM capacitors modifies the sharing of the power grid metal resources. The selected power grid is shown in Fig. 5.8 and the MIM pattern in 5.9. The upper metal level is routed vertically and the lower metal level is routed horizontally. The MIM is thus regularly opened in order to connect the two metal levels. This degrades the MIM area and as a consequence the flying capacitor values. The assembly of the MIM capacitors and the power grid is presented in Fig. 5.10. This configuration allows fast routing because the MIM and the power switch cells have the same pitch. The width of MIM is fixed and determined by the pitch while the length depends on the value of L in Fig. 5.4. The performances of the converter depends on the ESR value of the MIM capacitors but also on the parasitic coupling. The value of the flying capacitors and the parasitic capacitances must be evaluated using *Q3D Extractor*, a 3D electromagnetic field simulator [105]. The coupling effect between the plate and the power grid is small because of the inter-metal dielectric value and thickness. A bottom plate parasitic capacitor between 1% and 3% has been reported for the process.

5.3.3 Frequency generation

The switching frequency is generated by a ring oscillator. The proposed diagram for the oscillator is given in Fig. 5.11. The delay cells are made of an inverter chain. The supply voltage of the delay cells control the time propagation and by this way the oscillator frequency. The ring oscillator naturally delivers multiple phases necessary for the interleaving strategy [51, 59, 60]. A nand gate enables or disables

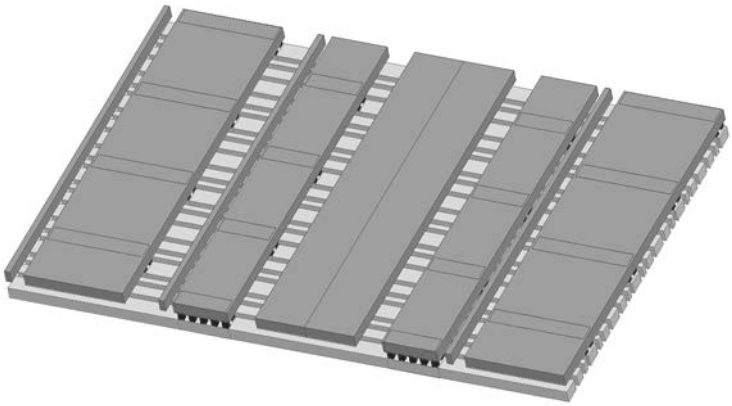


Figure 5.8: Layout of the power grid

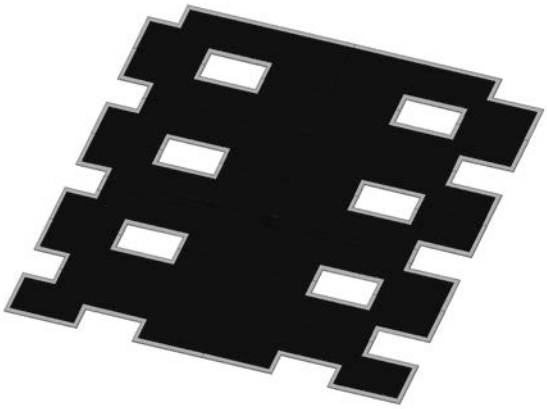


Figure 5.9: Layout of the MIM capacitor

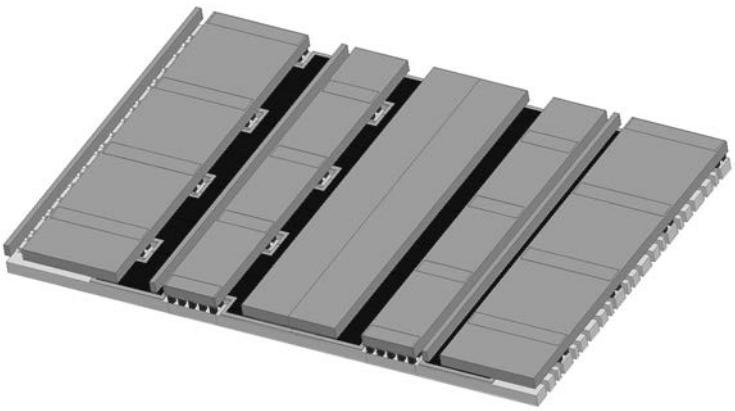


Figure 5.10: MIM capacitor and power grid assembly

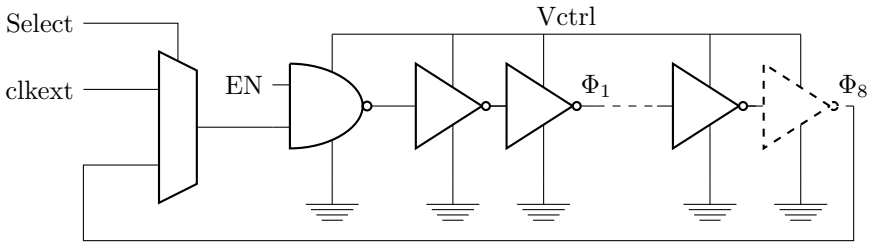


Figure 5.11: Diagram of the multiphase ring oscillator

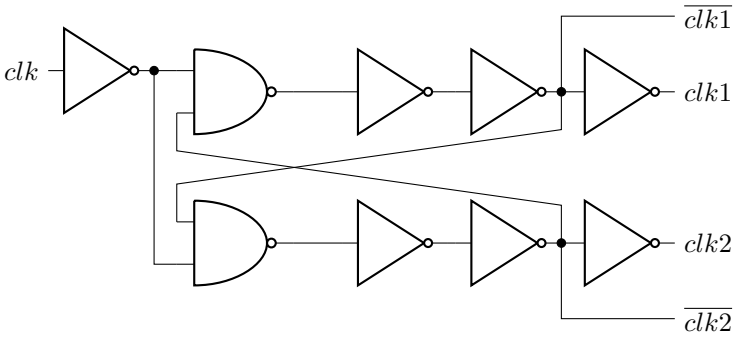


Figure 5.12: Diagram of the non-overlapping generator

the ring oscillator and ensures a proper operation. A multiplexer allows to open the ring oscillator and to feed it with an external clock. The ring acts as a buffer in this case. Thick oxide devices are selected to build the oscillator. The supply voltage varies what requires level-shifters to generate clock signal amplitudes in the full range of the power supply (1.8 V). These signals are propagated to each cells of the converter. Then a non-overlapping clock generator provides the necessary clock for the converter operation to avoid shoot-through current. The classical implementation of the non-overlapping generator is depicted in Fig. 5.12.

5.3.4 Prototype

A test-chip was designed to validate the power stage implementation. A SC converter with 8 interleaved multi-ratio cells is implemented to supply a digital area of 0.5 mm^2 for a nominal load of 250 mA. The diagram of the test-chip is given in Fig. 5.13. The input voltage and the supply voltage of the power switch drivers are separated in oder to isolate the switching losses. The converter is loaded with an off-chip load through output voltage pins. A bank of switches is made of three units with a binary weight of $\times 1$, $\times 2$ and $\times 4$. The width is selected and propagated to each cell using a bus. The supply voltage of the ring oscillator is externally controlled to adjust the switching frequency of the power stage. The switching fre-

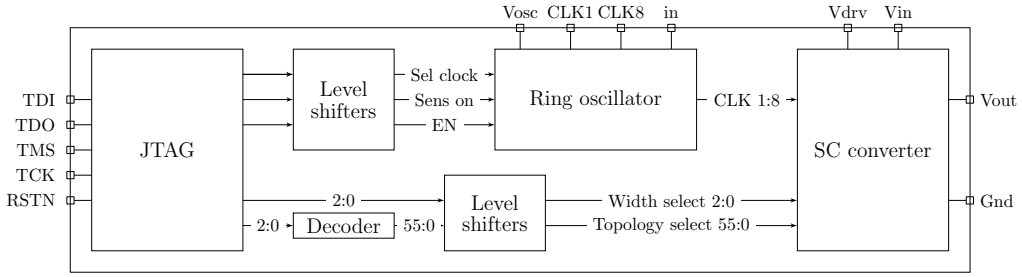


Figure 5.13: Diagram of the test-chip

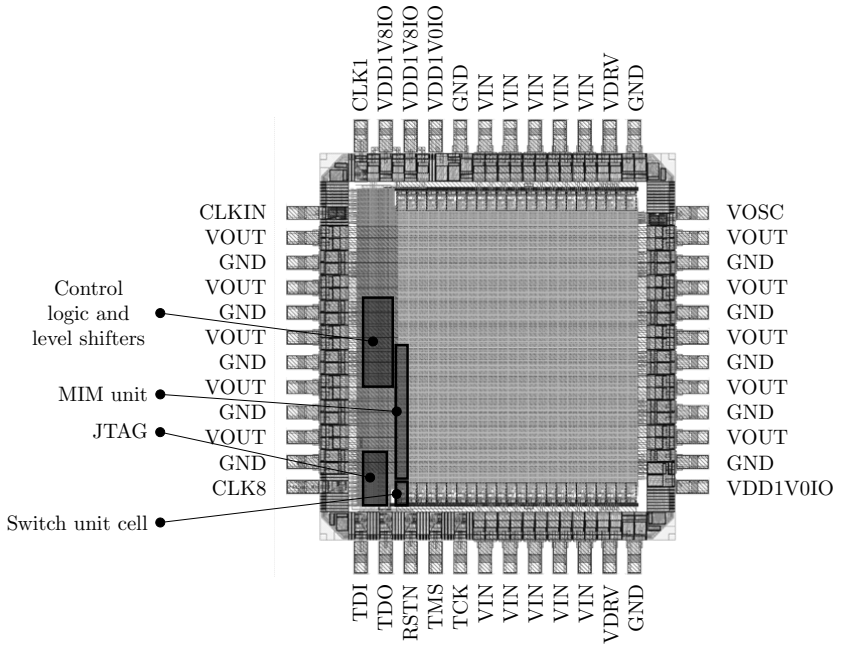


Figure 5.14: Layout and pin map of the test-chip

quency is monitored by probing the clocks at to adjacent phases. In case of failure, an external clock can be provided to the ring oscillator. A JTAG module enables the control of a large number of bits (up to 64) and consumes only 5 IOs. A decoder for the ratio selection also reduces the number of bits. The JTAG module and the topology decoder are implemented with low-voltage standard devices and need a 1 V voltage supply. Since other blocks use thick devices, level shifters are inserted to interface the two voltage domains.

The description of the layout and the pin mapping is given in Fig. 5.14. Table 5.2 gives a summary about resources and area. The ESD strategy is ensured by the IO ring. The IO ring is powered by 1 V and 1.8 V voltage levels. Those levels are also used for the thin and thick oxide logic respectively. Special care is brought for the power routing. The ground and the output voltage are connected to lateral pins using a strong horizontal Alu-cap grid. The digital power grid is thus connected

MIM cap area	0.4148 mm^2
PG area	0.5640 mm^2
Switch area	0.0420 mm^2
Total area	0.6363 mm^2
MIM effective density	73%

Table 5.2: Area summary

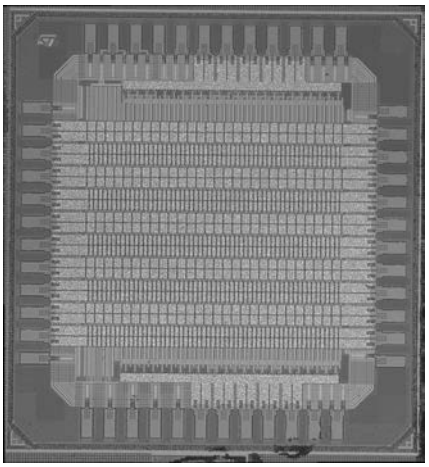


Figure 5.15: Pictures of the fabricated test-chip

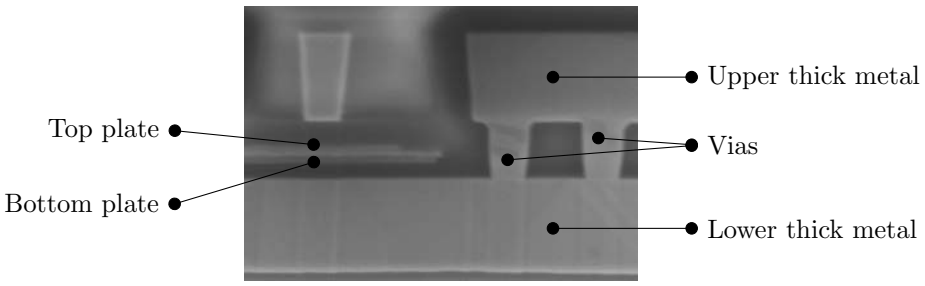


Figure 5.16: Cross section of the circuit

with a low impedance path similarly as in a flip-chip package. The input voltage is provided through out a set of pins at the top and the bottom of the chip. These pins are connected by a on board track. Finally the probing of clocks are buffered and then connected to the dedicated IOs. Otherwise a too large parasitic load due to probing would modify the targeted frequency of the oscillator. The test-chip has been fabricated and wire-bonded in a 48-LGA package for on-board characterization. A picture of the fabricated circuit is shown in Fig. 5.15. A cross section has been realized in Fig. 5.16 to show the MIM and the power grid processing.

5.3.5 Experimental validation

The test-chip is tested on a board presented in Fig. 5.17. A socket is used to allow quick and easy replacement of chips. Large tracks and bypass capacitors mitigate the inductive effects introduced by the package. The input and output clocks are adapted with 50 Ω lines and connected to SMA connectors. The test-bench is presented in Fig. 5.18. The clock frequency is measured through the oscilloscope. Source measurement units provide the necessary voltage levels and the external load current as well. High accuracy ampere meters monitor the input current, the driver current and the oscillator current. The voltage sensing employs four wire scheme to suppress the resistive drop impact. A computer configures the JTAG bus and the measurement unit through a GPIB bus. Measurements are automated with Python scripts based on PyVISA module and then processed in *Matlab*.
The oscillator is characterized first. The speed of the oscillator provides informations about process corners. The voltage supply of the ring oscillator is swept and the frequency and the current consumption are measured. The results are reported in Fig. 5.19 and Fig. 5.20 respectively. Post simulations of the oscillator are performed over process corners. The linear part in log scale in Fig. 5.19 indicates that the oscillator operates in the sub-threshold region. The measurements show that the inflection point occurs before the worst case simulation results. Above the sub-threshold region, the oscillation frequency fits with the slowest corner. Thereby the chip seems to be in a slow corner. The parametric tests performed during the fabrication confirm this observation. The threshold voltage of the NMOS transistors (RVT and LVT) is higher than expected. Regarding the PMOS transistors, the LVT devices are fast and RVT slow. Since the silicon results are out of the specifications for the worst case corner defined in the model, it is impossible to find more correlations between measurements and simulations. The same trend is observed for the current consumption measurement in Fig. 5.20. The maximal switching frequency of 123 MHz is measured at 1.8 V. The smallest switching frequency is 1.3 kHz and found at 0.4 V. Below this limit, the level shifter of the oscillator does not work

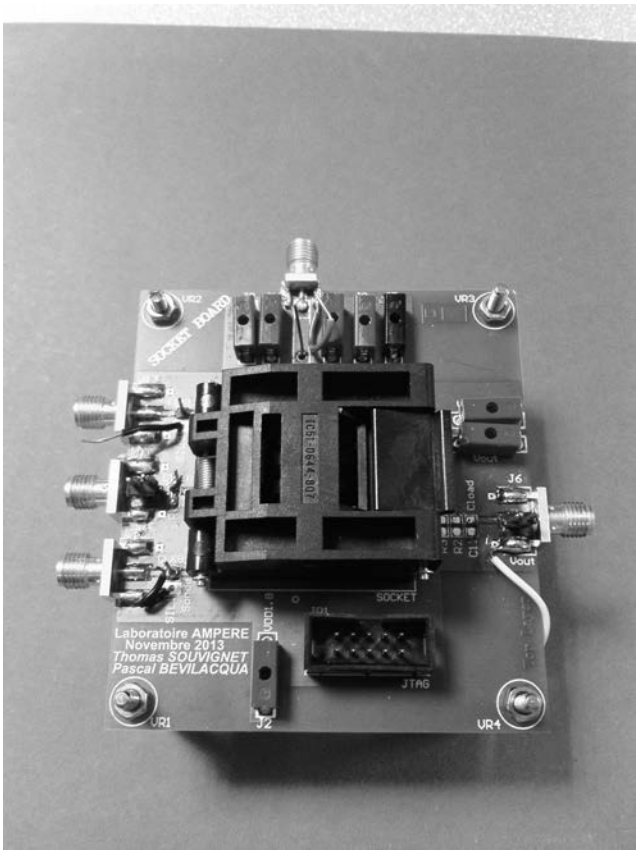


Figure 5.17: Board for chip testing

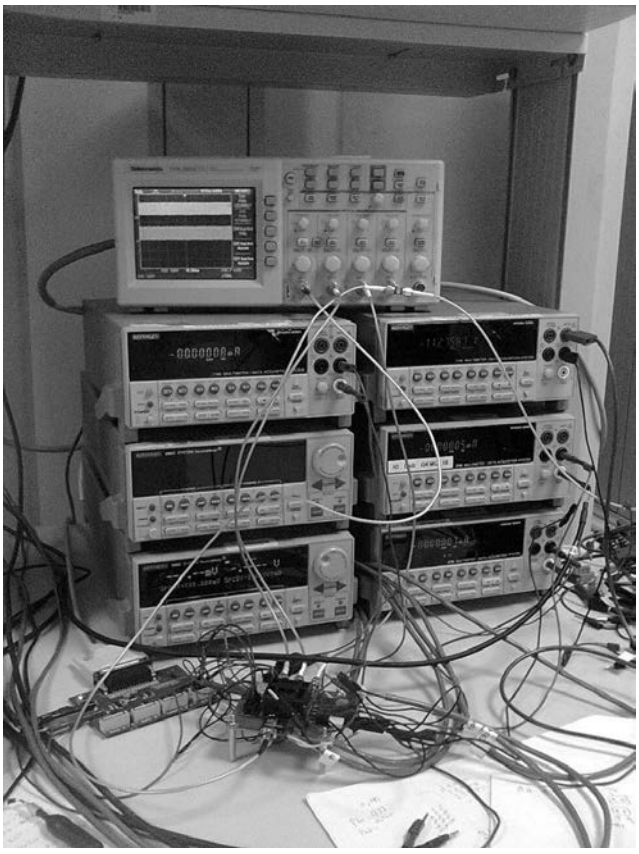


Figure 5.18: Test bench with the forest of cables

Table 5.3: Peak efficiency and output voltage over various load current

Ratio	1 mA	10 mA	100 mA	250 mA
3:1	51%@0.52 V	63%@0.49 V	56%@0.44 V	47%@0.35 V
2:1	70%@0.82 V	80%@0.81 V	78%@0.77 V	73%@0.74 V
3:2	72%@1.09 V	80%@1.08 V	75%@0.97 V	69%@0.91 V
4:3	73%@1.21 V	79%@1.2 V	71%@1.03 V	66%@0.97 V

anymore. At the maximal switching frequency the power consumption is 454 μA and only 3.5μA at the minimal switching frequency.

The efficiency of the power stage is then characterized for the various ratios and various load currents. The supply voltage of the ring oscillator is swept and the measurements are reported in Fig. 5.21, Fig. 5.22, Fig. 5.23 and Fig. 5.24. Table 5.3 presents the measured peak efficiency and the corresponding output voltage for the different ratios and over various output current values. Efficiency is lower at 1 mA than at 10 mA because the parasitic capacitor losses dominate at low power. At the maximal output current of 250 mA, efficiency is close to 70% for both the 2:1 and the 3:1 ratios. The converter cannot deliver more than 1 V at this current level even using the 4:3 ratio. This ratio is not efficient at high power due to the larger number of switches what increases the overall losses. The 3:2, 2:1 and 3:1 ratios are enough for applications requiring only voltages below 1 V.

Measurement results are compared to post layout simulation results. The expected corner has been found by the characterization of the ring oscillator but process deviation makes difficult the correlations. Moreover parasitic capacitors and the ESR values of the MIM capacitors are still undetermined. Various measurements are performed to find those values. The first measurement involves determining the effective corner of fabrication. The current consumption of the driver is extracted from post layout simulation and measured for the seven possible switch width. Indeed the switching losses induced by the gate of the transistors depend both on the corner and the size of the transistors. Iterative simulations allow to converge toward the measurement results by selecting different corners. The results are shown in Fig. 5.25. Simulations and measurements fit for the smallest size of switches and mostly at low switching frequency. The process deviation has altered the on-state current and the threshold voltage what is not sufficient to properly drive the switches at both high switching frequency and larger sizes. The degradation in the threshold voltage has been emulated by a reduction of the driver voltage rail by difference observed between the corner model and the parametric tests. The slow

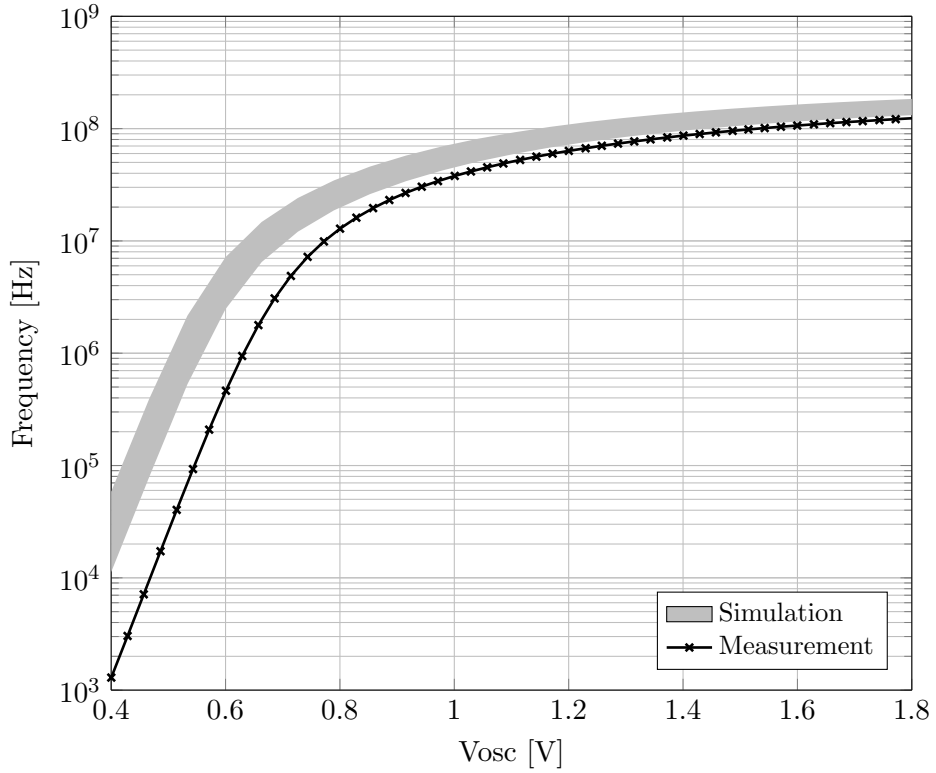


Figure 5.19: Oscillation frequency versus the voltage supply of the ring oscillator

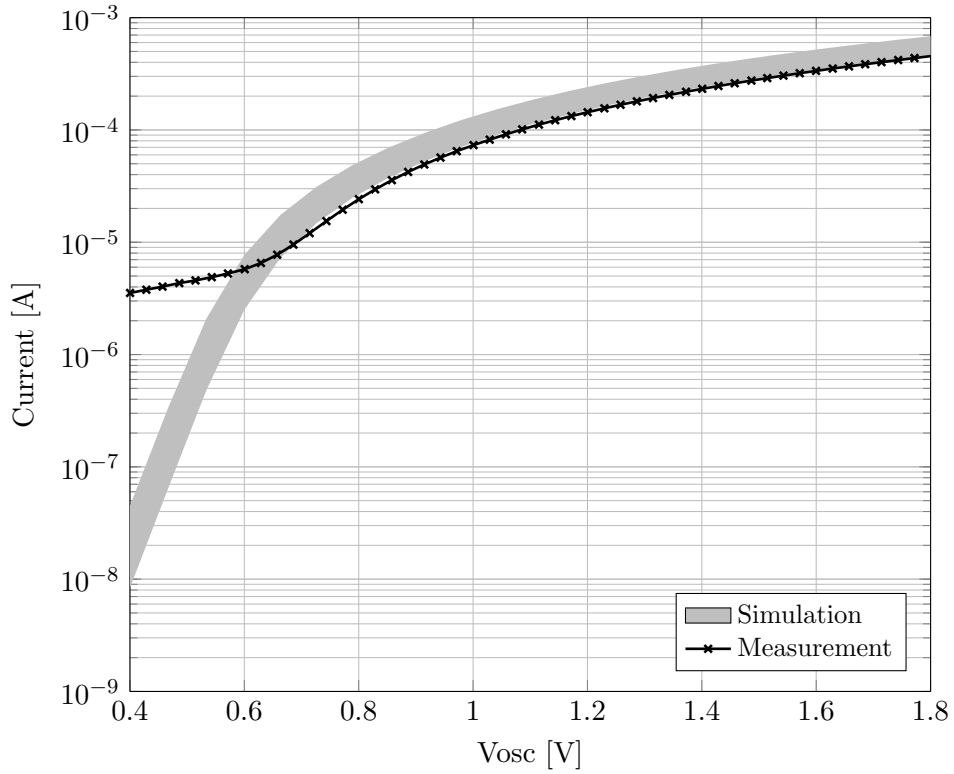


Figure 5.20: Current consumption versus the voltage supply of the ring oscillator

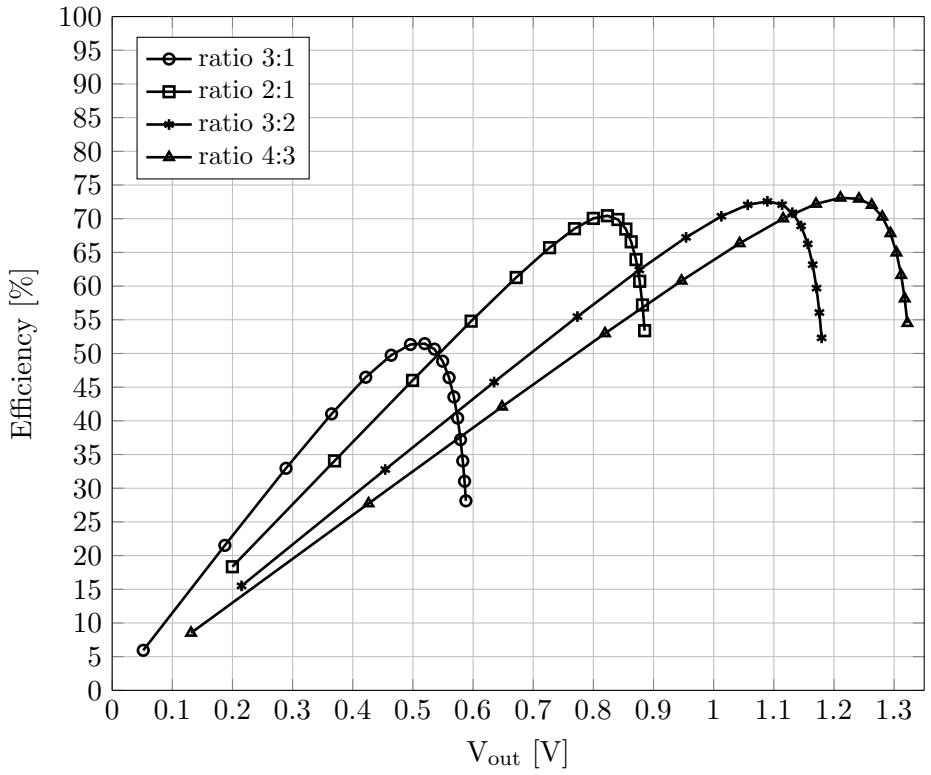


Figure 5.21: Efficiency measurement versus the output voltage at 1 mA load current

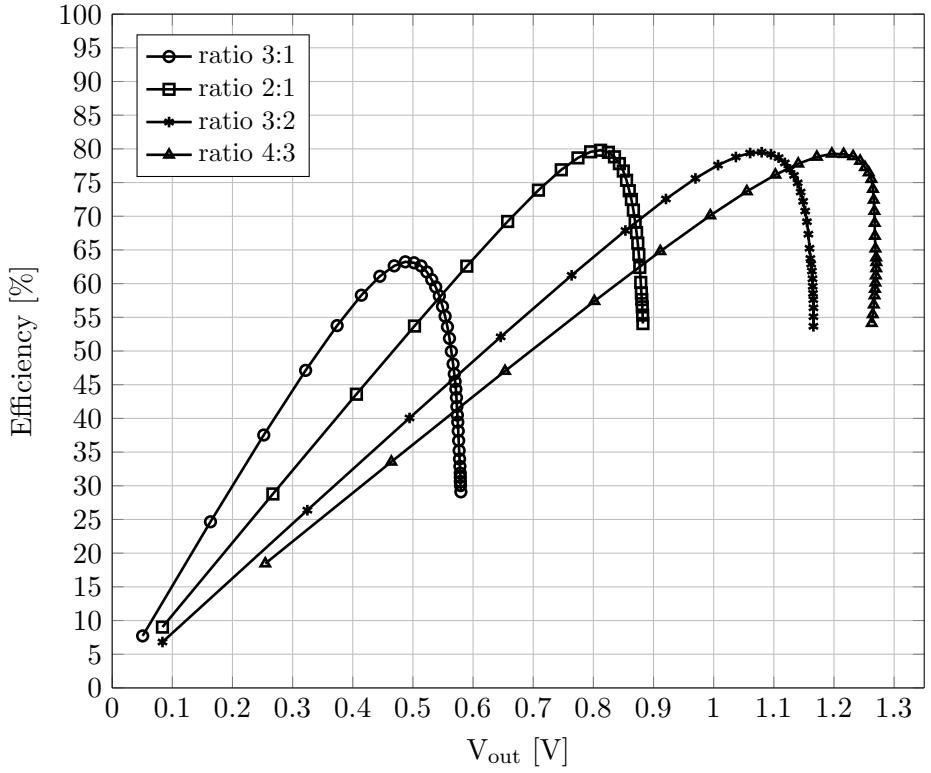


Figure 5.22: Efficiency measurement versus the output voltage at 10 mA load current

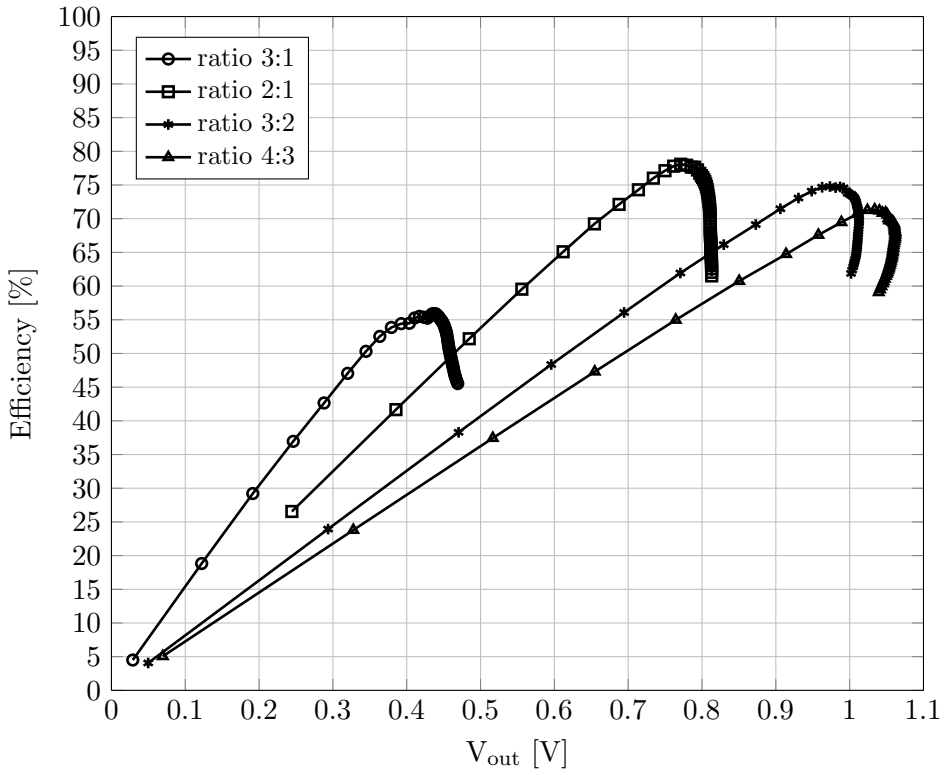


Figure 5.23: Efficiency measurement versus the output voltage at 100 mA load current

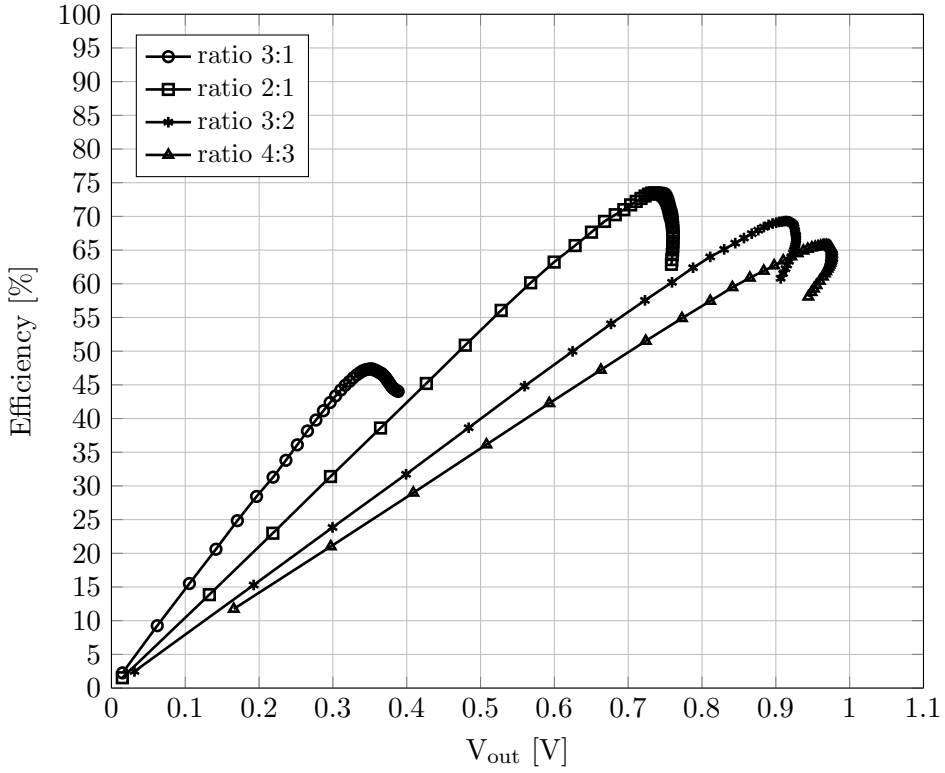


Figure 5.24: Efficiency measurement versus the output voltage at 250 mA load current

corner as identified confirm the previous observations.

The parasitic capacitors impact can be observed in the input current. The charging current of the bottom plate parasitic capacitor is indeed sunk from the input voltage rail. The value of the parasitic capacitor is swept in simulation for different load current until simulations fit with measurements. The results can be seen in Fig. 5.26 and the identified value of parasitic capacitor ratio is 3%. The initial value was 1% what was quite optimistic.

The last parameter to extract is the ESR value of the MIM capacitors. SC converters are sensitive to restive effect in the FSL region. In this region, the output voltage is almost constant while the frequency increases for a given load current. The process deviation degrades also the on-state switch resistance and it is difficult to separate its contribution in the FSL region. The characteristic that shows the resistive effect impacts is shown in Fig. 5.27. The load current is swept from 100 mA to 250 mA by step of 50 mA. After several iterative simulations the value of the resistance that fits with the measurement results is 8 Ω. The value extracted from the model was 6 Ω which was a good approximation considering its simplicity. The de-embedding of the parameter is also checked for the other ratios and confirm the results as shown in Appendix C.

5.4 The frequency modulation control

5.4.1 Control loop design

The PI controller is implemented using an operational amplifier and a feedback network (Fig. 5.28). The feedback components R_{11}, R_{21} and C_{21} are evaluated from (5.1):

$$R_{21} = \frac{T_i}{C_{21}} \qquad R_{11} = \frac{T_i}{K_p C_{21}} \tag{5.1}$$

The controller can be configured in follower mode when $F = 1$. This mode can be used for debugging and for the start-up of the converter. The converter enters in the regulation mode for $F = 0$. Programmable resistance are used to select various PI parameters. This is useful to compensate the process variation and uncertainty of the model.

The error signal is used to control the supply voltage of the ring oscillator. The error amplifier must be able to deliver enough current and to drive the equivalent capacitors of the oscillator. A rail-to-rail output stage is suitable to ensure a full swing of the error signal and control the oscillator in its whole range of switching frequency. The reference voltage varies from 0.1 V to 1.2 V what determines the input stage type. A bandwidth of 100 MHz is required to maintain a stable opera-

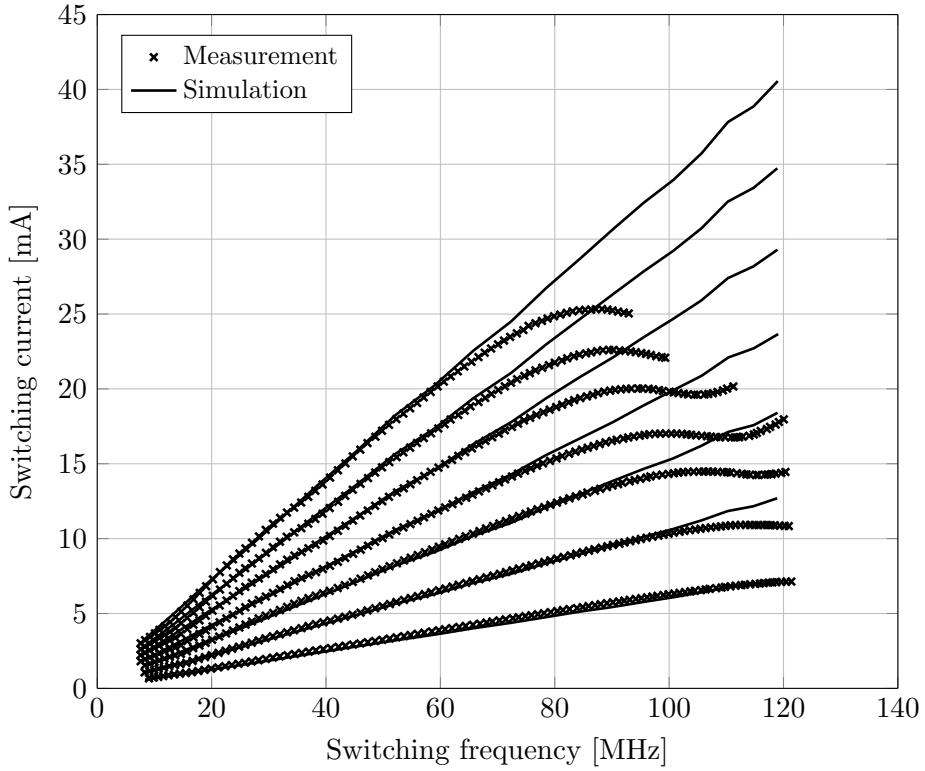


Figure 5.25: Switching current of the driver as a function of the switching frequency for various sizes of switch

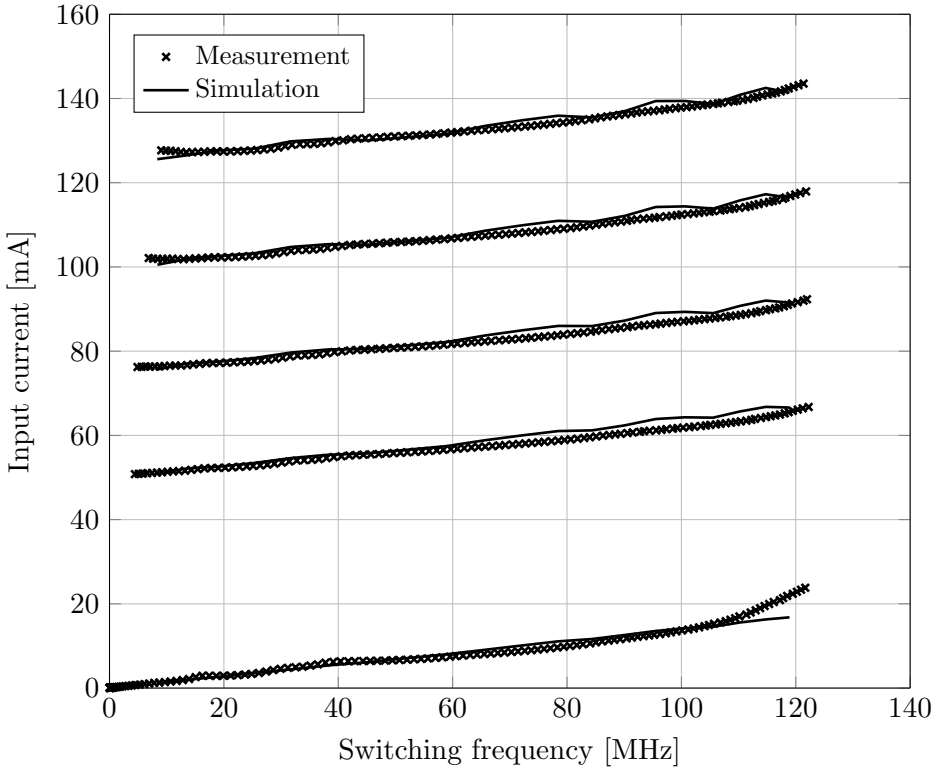


Figure 5.26: Input current as a function of the switching frequency for various load currents

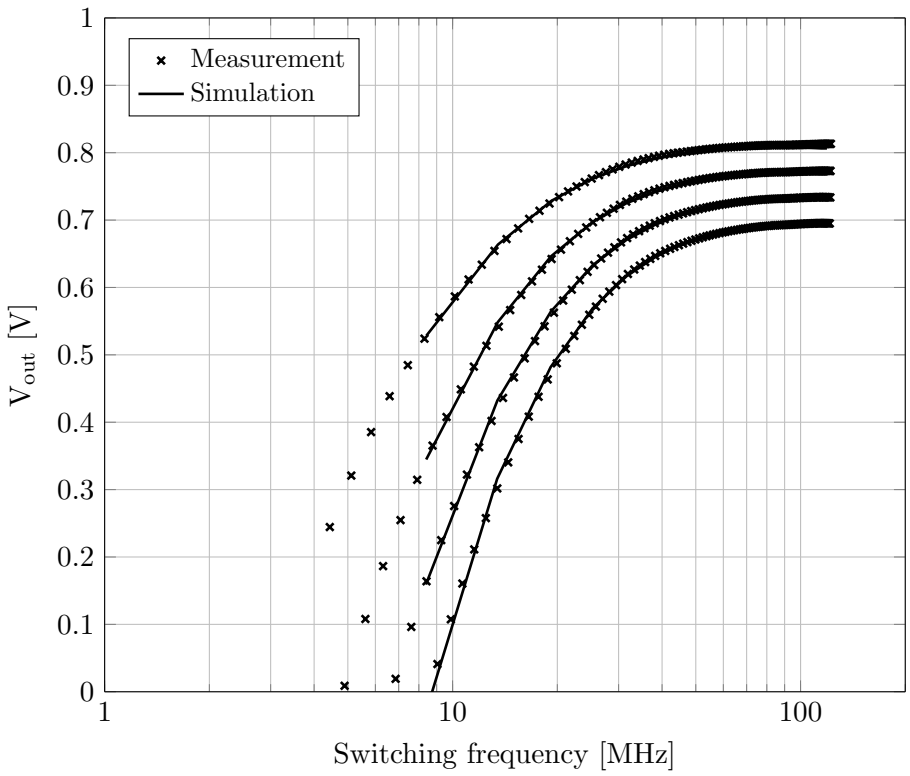


Figure 5.27: Efficiency versus switching frequency for various load currents

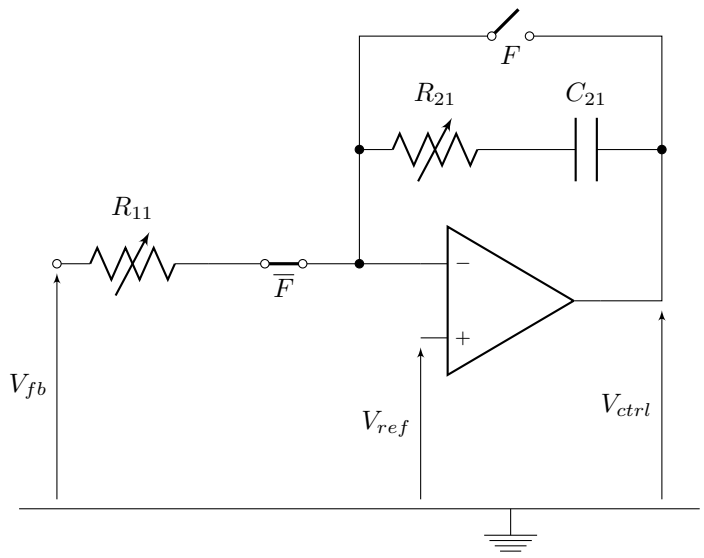


Figure 5.28: Diagram of the PI controller with programmable feedback network and follower mode

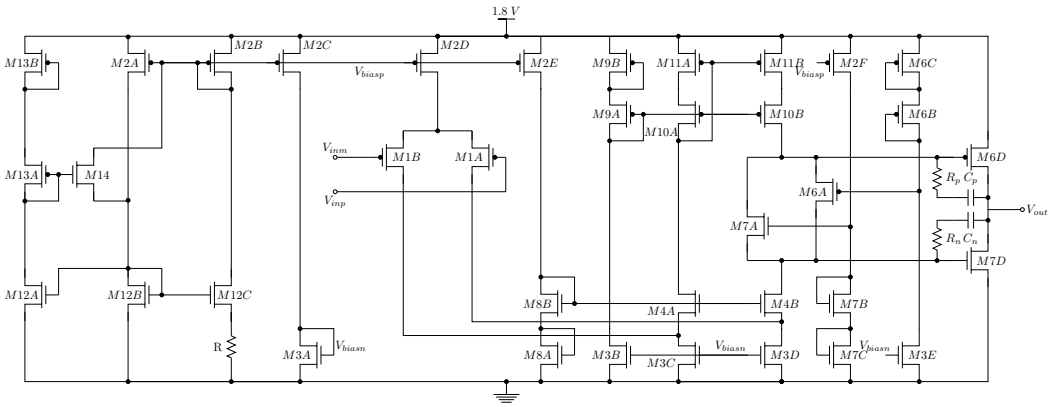


Figure 5.29: Schematic of the AB amplifier and its biasing circuit

tion of the closed-loop control. The slew-rate is also a major specification in order not to saturate the loop in case of large reference or load transients. The selected structure for the operational amplifier is given in Fig. 5.29. The OTA[3] comprises a PMOS differential pairs, a folded cascode stage, a class-AB output buffer and GmR block. Low threshold voltage and thick oxide devices are used and supplied from a 1.8 V voltage rail. The GmR scheme provides a biasing current proportional to temperature because the transconductance of the differential pairs decreases with temperature and the Miller compensation becomes inefficient. The transconductance of the input stage is therefore almost constant in the range from $-40\,^{\circ}C$ to $125\,^{\circ}C$ but the power consumption worsens with temperature increase.

5.4.2 Experimental validation

A second test-chip including the power stage, the controller and a digital load has been fabricated to evaluate the converter. The layout of this test-chip keeps the pin-to-pin compatibility with the board in Fig. 5.17. The supply voltage of the controller is isolated from the 1.8 V voltage rail used by the IO ring. A clock sensing has been replaced by a biasing input for the amplifier. The pin can be used to provide an external biasing current in case of a failure of the GmR structure. The other clock sensing is still available to monitor the switching frequency of the converter. In addition to the controller, a digital load has been implemented over the available area. This load comprises inverter chains distributed as programmable slices. An external clock toggles the inverters activated in a slice. The current consumption of the load is tuned by the JTAG and the external frequency. The JTAG module also configures the controller such as the feedback network and the amplifier mode. Pictures of the test bench and the test-board are shown in Fig. 5.31 and in Fig. 5.32

[3]Operational transconductance amplifier

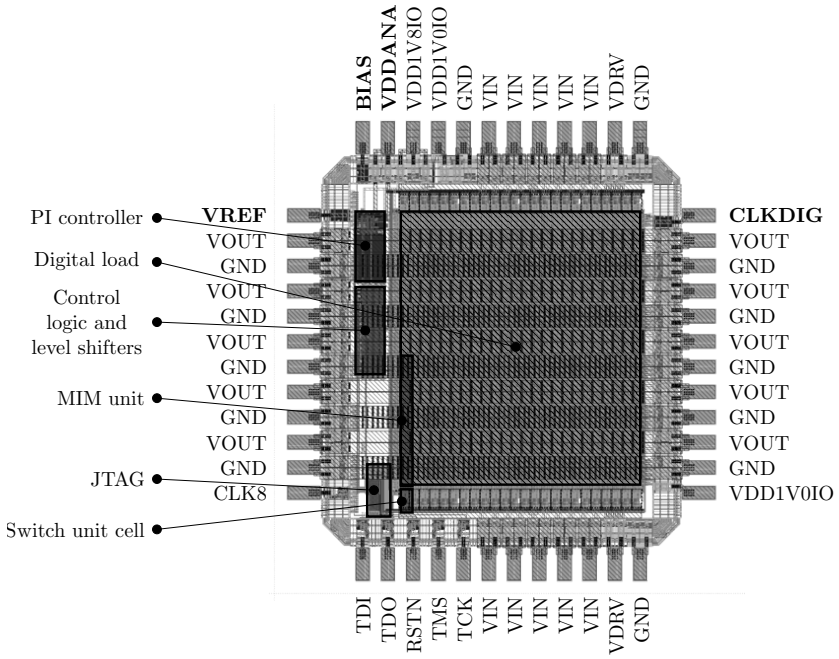


Figure 5.30: Layout and pin map of the second test-chip

respectively. The transient signal of the output voltage and the output clock are probed with low impedance oscilloscope probe (50 $k\Omega$) and monitored by an oscilloscope. Four wire measurement is extensively used and the ground is star-connected for accuracy measurement purpose. No bypass capacitor is connected to the output voltage. The converter can be loaded with an external current source or resistor if needed.

The oscillator is first characterized as it was the case for the previous test-chip. The amplifier is configured in the follower mode and the SC converter is disabled. The amplifier serves as a buffer which drives the oscillator according to the value of the reference voltage. The reference voltage is swept from 0.4 V to 1.8 V and the oscillator frequency is measured. 45 samples are evaluated and the results are presented in Fig. 5.33. The start-up of the bench follows a special sequence. The amplifier starts first and the oscillator is activated a few μs latter. Otherwise the oscillator can enter in an unstable operation with non-uniform square waves and a high frequency due to the propagation of a glitch through the ring.. The parametric tests indicate a typical trend of corner fabrication and the spread of the measurements can be interpreted as a mismatch. The measurement setup is simulated with a typical corner and post layout extractions (resistor and capacitor). The results are reported in Fig. 5.33. Simulations do not fit with the experimental results. The frequency is constant above a reference voltage of 1.6 V because the

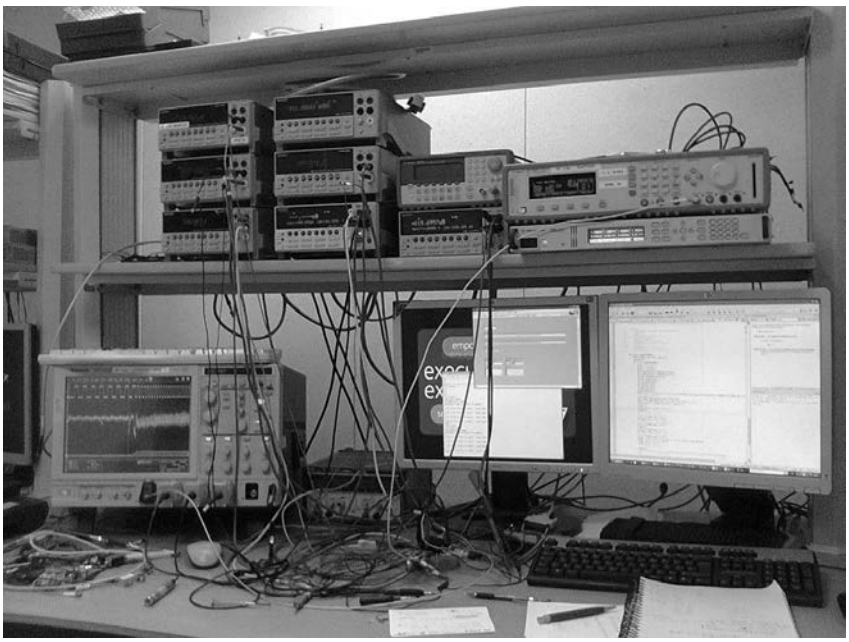


Figure 5.31: Picture of the second test-bench

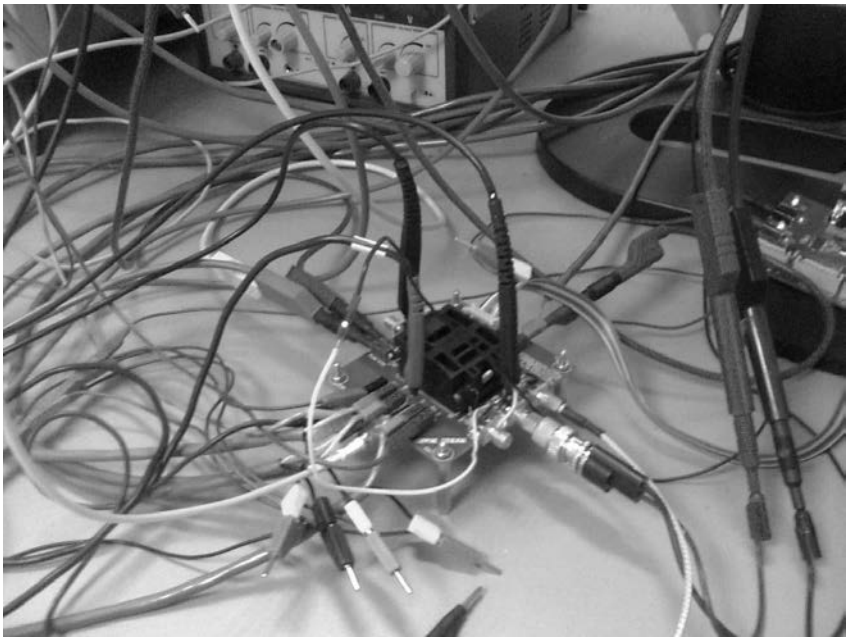


Figure 5.32: Picture of the board and the connections

MIM cap area	0.4148 mm^2
PG area	0.5640 mm^2
Core area	0.5224 mm^2
Switch area	0.0420 mm^2
AB area	0.0040 mm^2
Network area	0.0140 mm^2
Total area	0.6543 mm^2
MIM effective density	73%
$A_{switches}/A_{digital}$	8%
$A_{Active}/A_{digital}$	11.5%

Table 5.4: Area summary

amplifier operates near its supply voltage and requires at least a margin of 200 mV to maintain the output stage in the saturation region. This observation is true for both experimental and simulation results. The slope of the curves are different and the simulation of the previous test-chip is included to provide an extra comparative element. It is clear that this difference can come from the insertion of the amplifier but is not explained by post layout simulation. It would have been necessary to supply the oscillator with an external pin for further investigations.

The open-loop power stage is characterized in a second phase. The results are similar to those in Section 5.3.5 and are provided in Appendix C. The closed-loop measurements are then performed. Static measurements concern the efficiency and the DC regulation while dynamic measurements focus on load transient and reference tracking. Before measuring, the stability of the converter must be checked. An oscillation of the error voltage can be detected in the frequency measurement. The frequency is not constant in this case and statistical measurements provide such an information. A large σ in the statistical measurement will report an unstable operation and a small σ indicates a stable system. The maximal switching frequency of the oscillator is between 80 MHz and 100 MHz depending on the chip sample. The converter can not regulate if the selected reference voltage or/and load current require a larger frequency. These precautions allow successful measurement sequences. The efficiency and the regulated output voltage are measured over the different ratios and for various load currents. The load current value is determined by an external current source and the on-chip digital load is disabled. The leakage current of the digital load has been characterized but not subtracted from the load

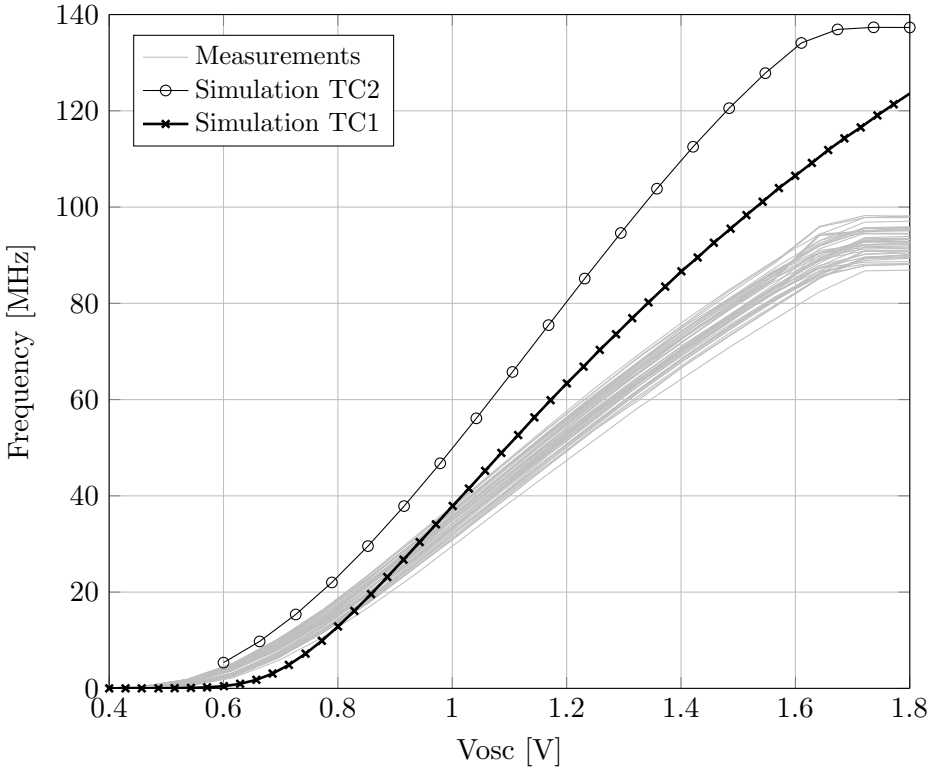


Figure 5.33: Frequency versus reference voltage

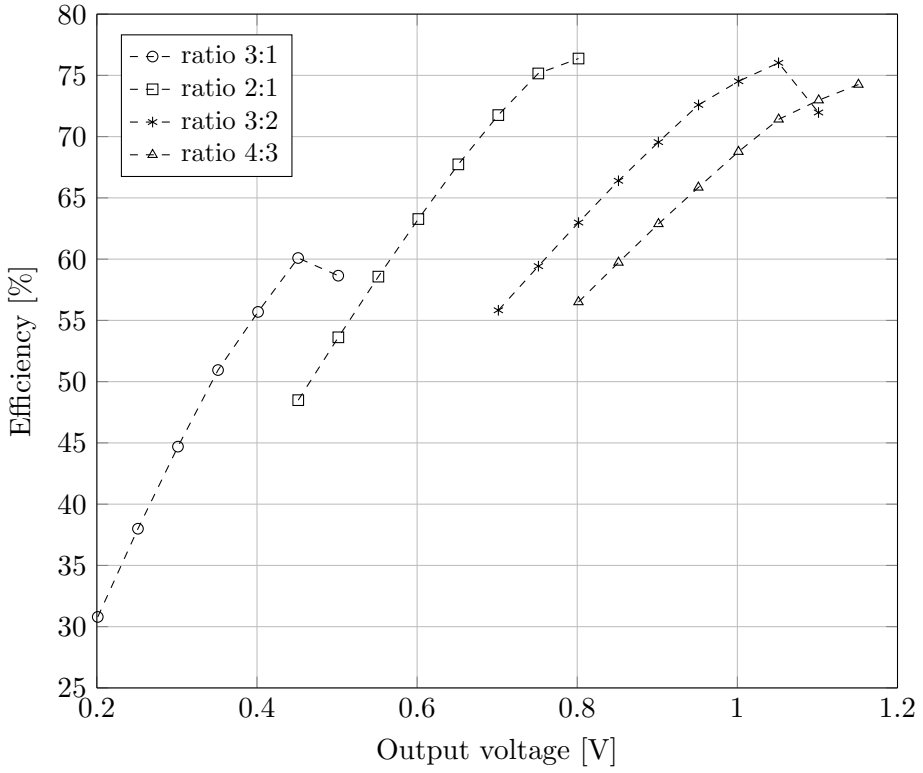


Figure 5.34: Efficiency versus output voltage over the various ratio for a load current of 50 mA

current due to its negligible value at enough high output current. Fig. 5.34 presents the results for a load current of 50 mA and Fig. 5.35 for a load current of 190 mA. Efficiency as function of the load current for various regulated output voltages is plotted in Fig. 5.36. The efficiency is almost constant over the current range but decreases at light load because of the leakage of the current source. The efficiency starts to decrease at larger value of load current for 0.4 V, 0.9 V, 1 V and 1.1 V because the converter operation get close to the FSL region. The switching frequency does not increase linearly and the switching losses drastically increase.

The accuracy of the regulated output voltage depends on the amplifier mismatch. More precisely a mismatch in the differential pairs introduces an offset. The mismatch is mitigated by a larger size of transistors and can be evaluated using statistical models. 1000 runs of Monte-Carlo simulations are performed on the converter for a reference voltage of 600 mV and a load current of 100 mA for the 2:1 ratio. The distribution of the output voltage is given in Fig. 5.37 and $\sigma = 0.8371$ mV. Simulations establish an accuracy of ± 2.5 mV. All chip samples (45) are then characterized for the same operating point. Repeatability of the measurement has been checked and measurements are performed one after another. The distribution is plotted in Fig. 5.38 and $\sigma = 2.005$ mV. The measured accuracy is ± 6 mV that is larger than the one obtained from simulation. The process support team has mentioned that the mismatch models were quite optimistic and some improvements are in progress.

Load transients are performed with the embedded digital load because current steps cannot be applied externally due to the inductive parasitics of the socket. Moreover this digital load allows to emulate the current surge of real digital core. The setup of a load transient is the following. For a negative load step, a constant current is applied with a current source and the sensing clock of the oscillator is disabled. A clock of 100 MHz is fed to the digital load but all the slices are disabled. The oscilloscope is set in the single acquisition mode. The sensing clock and the slices are turned-on simultaneously and the event is triggered on any sensing clock edge. For a positive load step, a constant current is applied and the digital load is on while the sensing clock is off. The slices are disabled and the sensing clock is enabled simultaneously. The event is also triggered on any sensing clock edge to capture the output voltage. Results for a negative and a positive load transient are given in Fig. 5.39 and Fig. 5.40 respectively. The constant current is set to 50 mA, the reference voltage to 600 mV and the digital load power consumption to 70 mA. An undershoot of 100 mV and an overshoot of 155 mV are observed in 5.39 and Fig. 5.40 respectively. The recovery time of the negative load transient is around 200 ns.

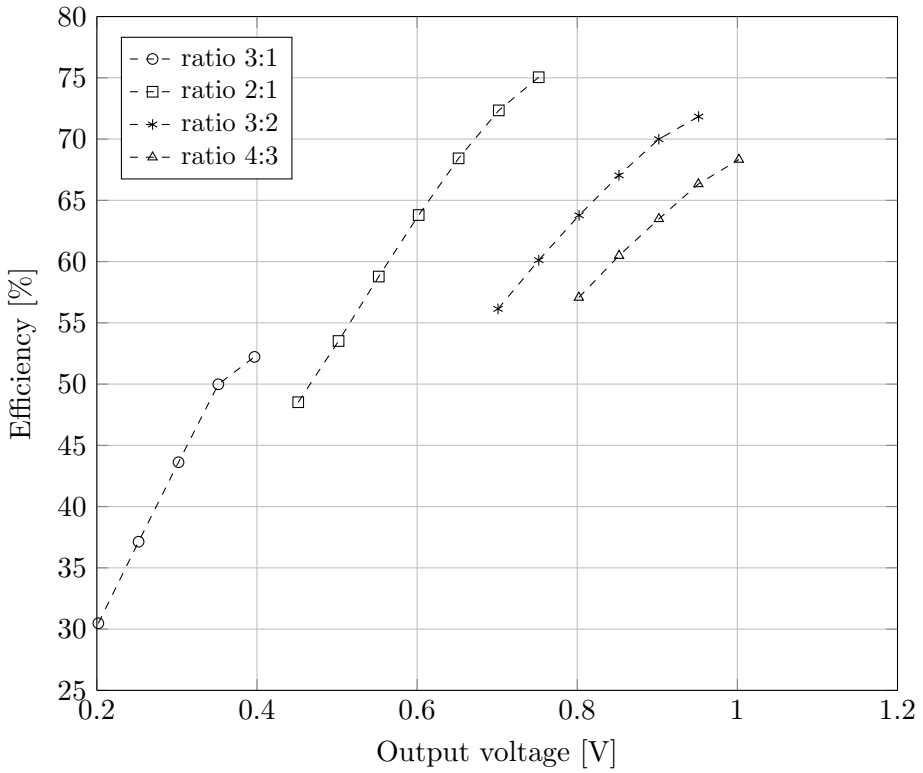


Figure 5.35: Efficiency versus output voltage over the various ratio for a load current of 190 mA

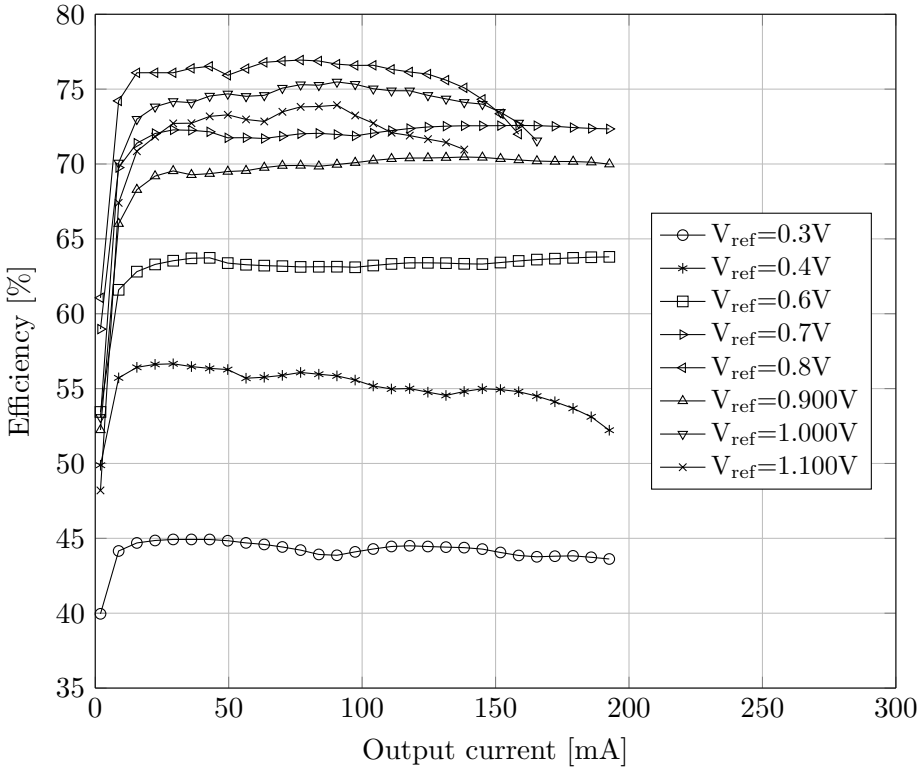


Figure 5.36: Efficiency versus output current for various voltage references

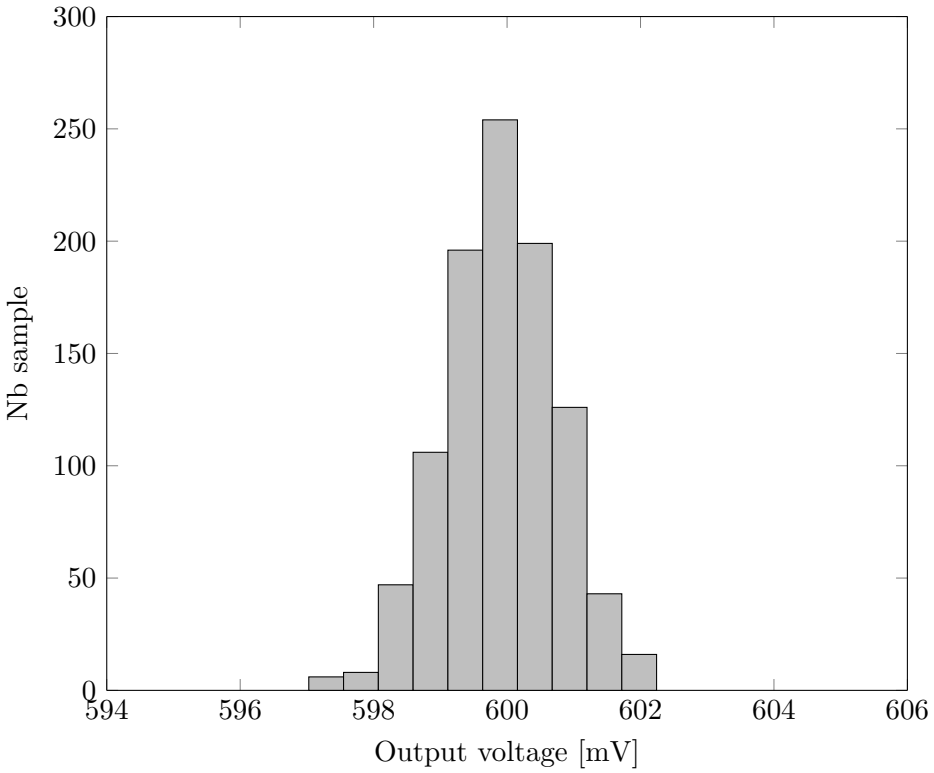


Figure 5.37: Distribution of the simulated output voltage for a voltage reference of 600 mV ($\sigma = 0.8371\ mV$)

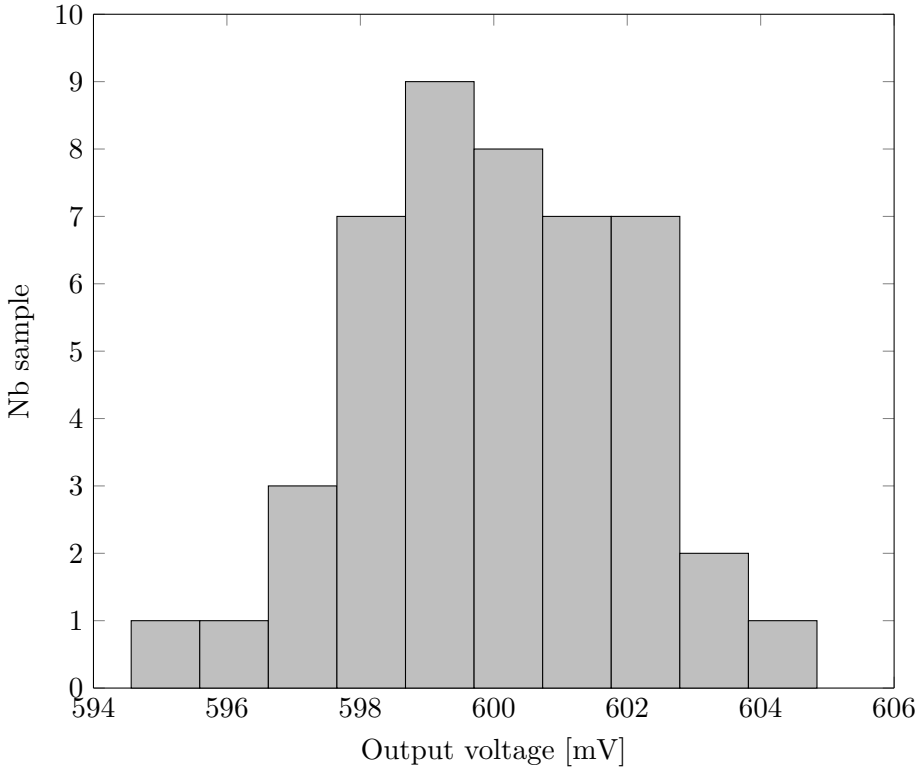


Figure 5.38: Distribution of the measured output voltage for a voltage reference of 600 mV ($\sigma = 2.005\ mV$)

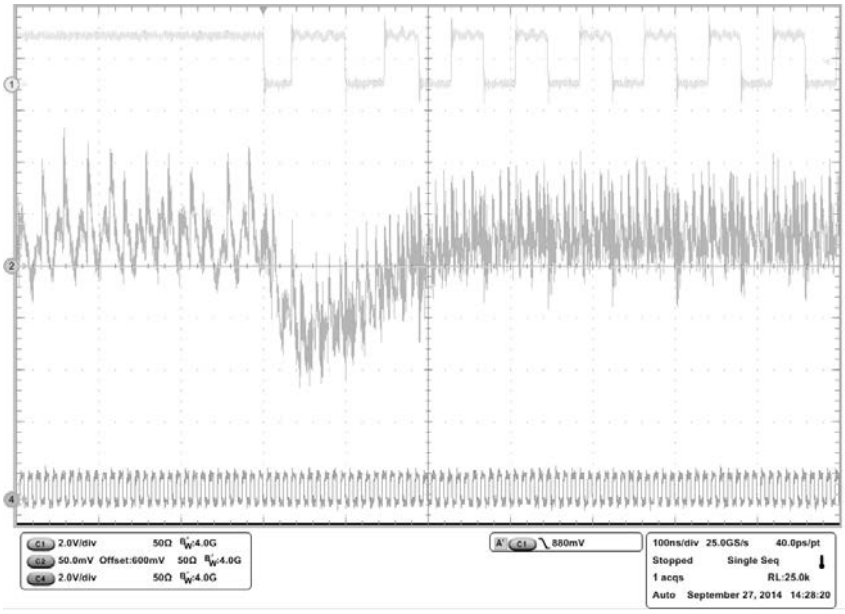


Figure 5.39: Negative load transient from 50 mA to 130 mA at V_{ref} = 600 mV, output clock (top), output voltage (middle) and digital clock (bottom)

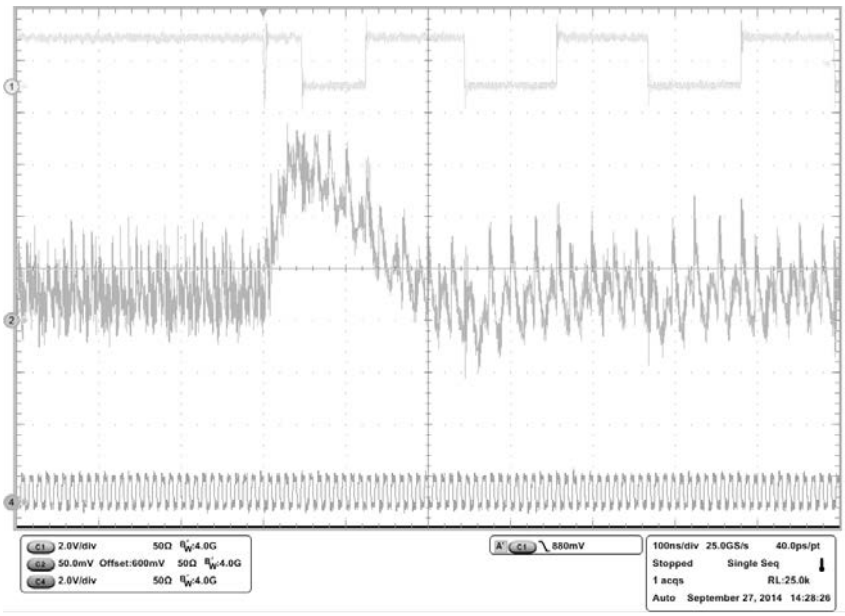


Figure 5.40: Positive load transient from 130 mA to 50 mA at V_{ref} = 600 mV, output clock (top), output voltage (middle) and digital clock (bottom)

The dynamic voltage scaling of the converter is evaluated with reference tracking measurements. Positive and negative reference trackings are presented for the 2:1 ratio at I_{load} = 100 mA in Fig. 5.41 and in Fig. 5.42 respectively. The reference raises from 500 mV to 800 mV for the positive case and falls from 800 mV to 500 mV for the negative case. The output voltage is averaged 16 times to limit

ripple noise and facilitate timing measurement. For the positive step, the rise time of the output voltage is 9.89 ns and the overshoot is 18%. In the negative step, the fall-time is 40.25 ns and the undershoot is 22%. The undershot is higher than the overshoot because the pole of the power stage moves in the low frequency slowing down the response. The fall-time depends on the output capacitor and the output current. The delay between the rising edge of the voltage reference and the output voltage is 12.63 ns. This delay corresponds to the time when the output voltage crosses the middle of the reference voltage swing. The dynamic voltage scaling is around 30 $^{V}/_{\mu s}$ in this case. More results are given in Appendix C.

A gear box will have to be implemented to automatically change the ratio on the fly. The ratio is selected in open-loop for now but the impact of dynamic change can still be evaluated. The reference voltage is set to 0.6 V, an intermediate point between the 3:1 ratio and the 2:1 ratio. The ratio is changed both ways and the event is triggered by the clock sensing signal. The digital load is activated to emulate the power consumption of 70 mA. The change from the 3:1 ratio to the 2:1 ratio is given in Fig. 5.43 and the change in the other direction in Fig. 5.44. No undershoot is observed in Fig. 5.43 because the frequency decreases as confirmed by the output voltage ripple increase. On the contrary, when a lower ratio is selected as in Fig. 5.44, the switching frequency must increase and an undershoot appears. As well as for load transient this undershoot can be mitigated by increasing the crossover frequency of the controller. Additional results are provided in Appendix C.

The ripple voltage is a sensitive specification in SC converter. The switching frequency, the load current and the output capacitor value are the major parameters. For instance, the voltage ripple value is 100 mV in the 2:1 ratio at 130 mA and for a reference voltage of 600 mV. The ripple measurement is partially polluted by inductive noise but most part of this large ripple value can be explained by the architecture implementation. The lateral length of the oscillator is larger than the horizontal length. It becomes quite complicated to maintain equal delays between cells while the spacing between some delay cells is different. In other words, the interleaving of the clock is not ideal. The charges are not delivered as uniformly as expected, causing an increase in the output voltage ripple. This ripple could also alter the stability of the loop because it can be found on the error signal which drives the oscillator. The impact of the ripple can be measured on the jitter of the clock. The jitter is measured for the 2:1 ratio at a load current of 50 mA and a voltage reference of 600 mV as shown in Fig. 5.45. The load current is increased to 150 mA in Fig. 5.46. In Fig. 5.45 the converter operates in the SSL region where the ripple is high and a peak-to-peak jitter value of 34.8 ns is measured for a period

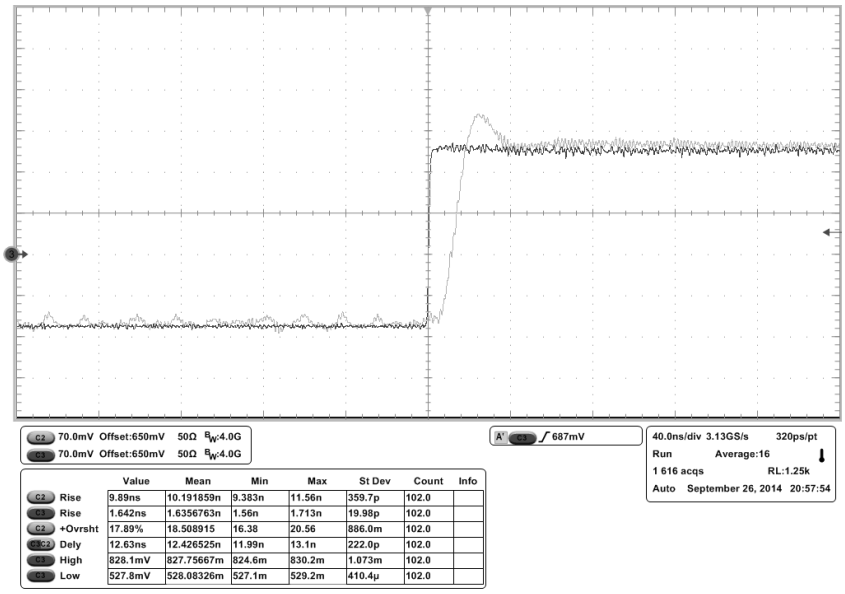


Figure 5.41: Rising reference tracking for the 2:1 ratio from 0.5 V to 0.8 V at $I_{load} = 100\ mA$, output voltage and reference voltage

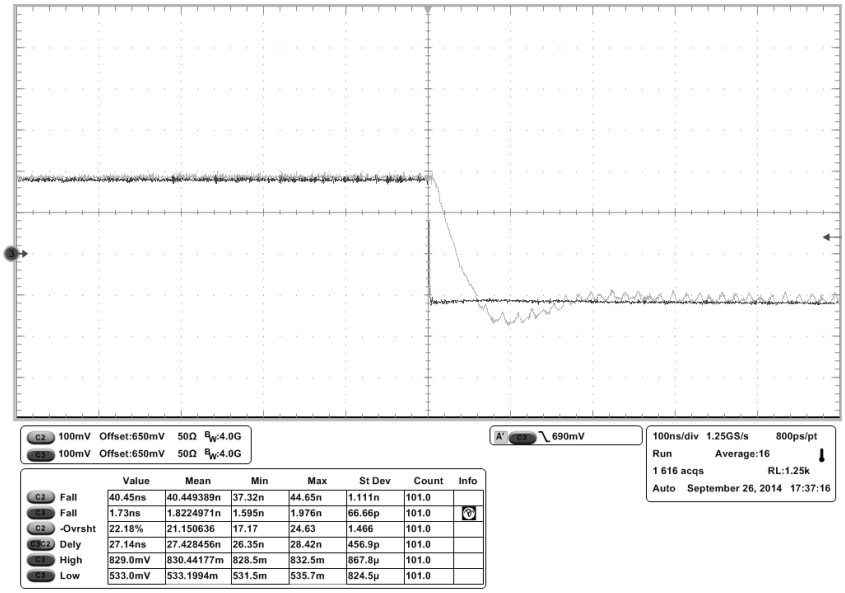


Figure 5.42: Falling reference tracking for the 2:1 ratio from 0.8 V to 0.5 V at $I_{load} = 100\ mA$, output voltage and reference voltage

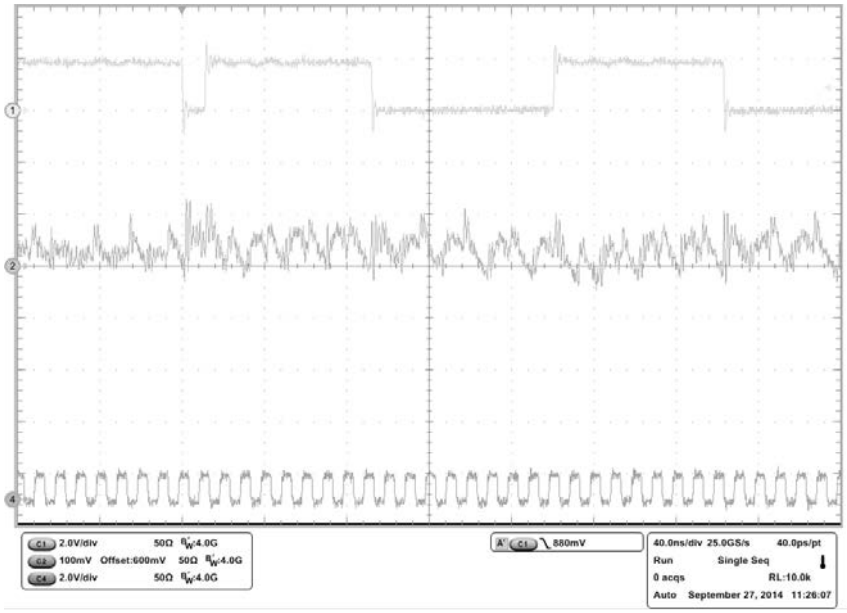


Figure 5.43: Ratio change from $2:1$ to $3:2$ with $V_{ref} = 600\ mV$, $I_{load} = 70\ mA$ and $V_{in} = 1.8\ V$, output clock (top), output voltage (middle) and digital clock (bottom)

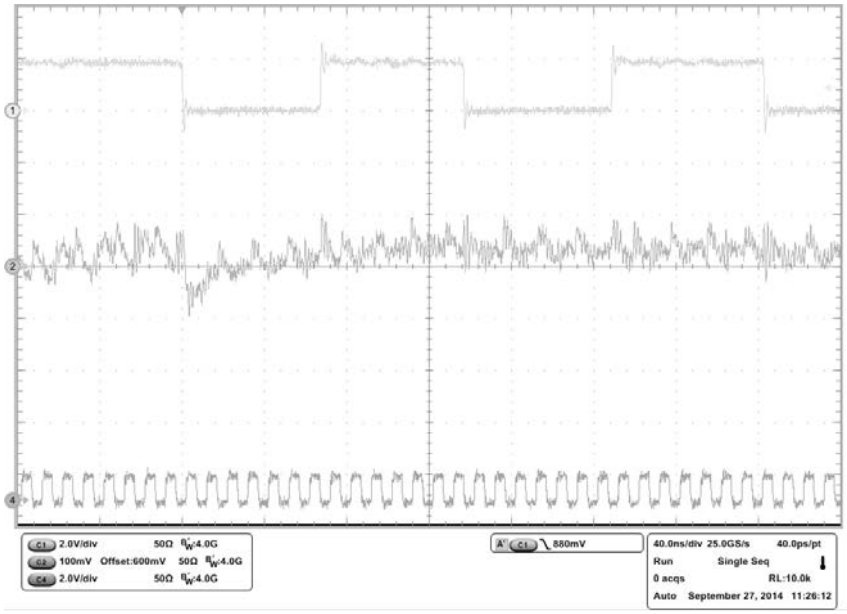


Figure 5.44: Ratio change from $3:2$ to $2:1$ with $V_{ref} = 600\ mV$, $I_{load} = 70\ mA$ and $V_{in} = 1.8\ V$, output clock (top), output voltage (middle) and digital clock (bottom)

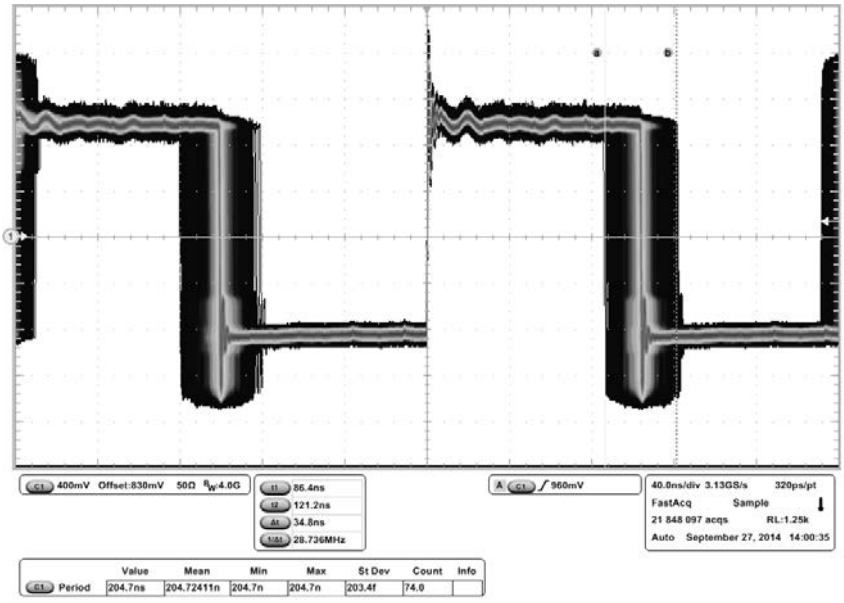


Figure 5.45: Measurement of the clock jitter at $I_{load} = 50\ mA$, $V_{ref} = 600\ mV$ and $V_{in} = 1.8\ V$

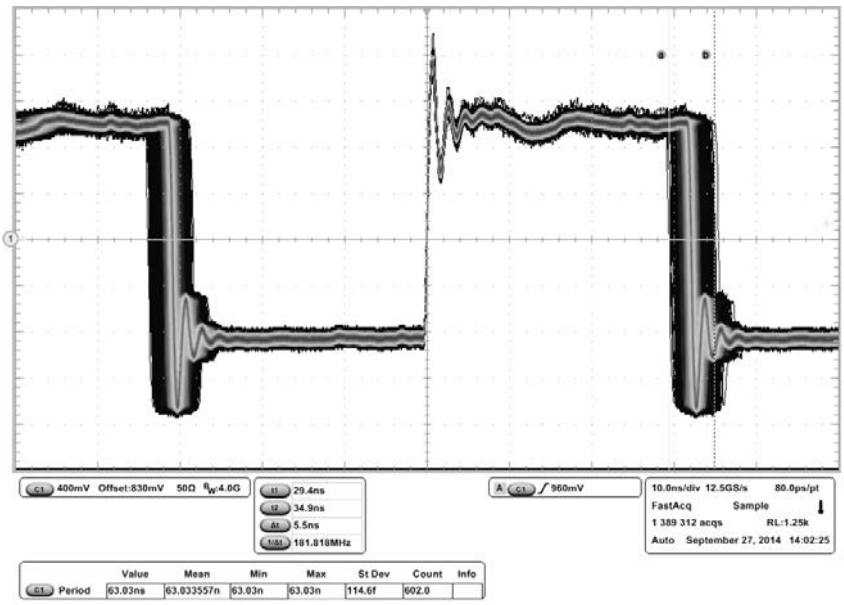


Figure 5.46: Measurement of the clock jitter at $I_{load} = 150\ mA$, $V_{ref} = 600\ mV$ and $V_{in} = 1.8\ V$

of 204.7 ns (17%). When the output current increases and the converter operates close to the FSL region, the peak-to-peak jitter value is 5.5 ns for a period of 63 ns (8.7%). If the jitter becomes too large, the output voltage can oscillate even if the loop has enough stability margin. No oscillations have been noticed in experiment what means the measured values of jitter are not critical so far.

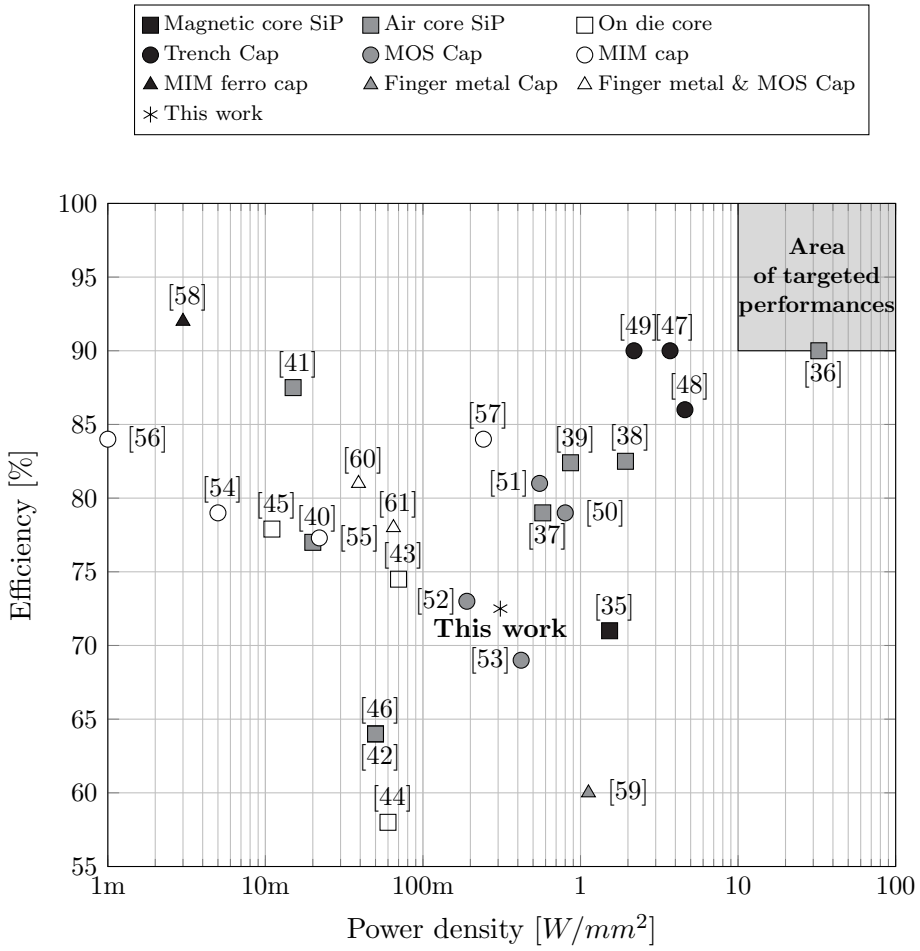


Figure 5.47: Peak efficiency vs power density of recent published integrated inductive and capacitive DC-DC converters

5.5 Discussion

The converter can be compared to previous art in terms of efficiency versus power density as shown in Fig. 5.47. A peak efficiency of 72.5% at the power density of 310 W/mm^2 is considered for the 2:1 ratio. This point is located on the trend of other SC converters and close to [57] for the same output voltage which also uses MIM capacitors above digital core. Those points are still far from deep trench capacitor based converters [47] or from the converter using only MOS capacitors as presented in [51]. This difference can be explained by the design constraints. The series resistance of MIM capacitors strongly limits both efficiency and power density. New form factor would improve the performances.

Table 5.5 gives some comparison points with relevant published works. The proposed solution exhibits the widest output voltage range $0.2 - 1.1\ V$ for an input

voltage of 1.8 V. Lower input voltage does not reduce significantly the input current. The DVFS capability is the highest reported and around ten times larger than [61]. However load transient performances are quite weak but the control strategy is promising regarding the performances in [61]. Higher crossover frequency for the PI controller could improve the undershoot and the recovery time. The large output voltage ripple is also an important issue. Design efforts in the ring oscillator design and higher interleaving level should address this issue. Besides the solution remains area efficient since the silicon area penalty is only 11.5% of the digital block area. This feature is larger than the 3.6% in [57] mainly because of the analog nature of the controller rather than an hysteretic one.

Ref	[106]	[61]	[47]	[57]	[52]	This work
Process	32nm SOI	65nm bulk	32nm SOI	22nm Tri-gate	65nm bulk	28nm FDSOI
Passive type	Deep trench	MOS MOM MIM	Deep trench	MIM	MOS	MIM
Input voltage	$1.8\ V$	$1.6 - 2.2\ V$	$1.8\ V$	$1.23\ V$	$3 - 4\ V$	$1.8\ V$
Output voltage	$0.7 - 1.1\ V$	$0.6 - 1.2\ V$	$0.7 - 1.1\ V$	$0.45 - 1\ V$	$1\ V$	$0.2 - 1.1\ V$
Interleaving	16	123	16	8	18	8
Current step	$335\ mA$ ($50\ ps$)	$100\ mA$ ($100\ ps$)	$335\ mA$ ($50\ ps$)	$15\ mA$ ($20\ \mu s$)	$162\ mA$ ($50\ ps$)	$70\ mA$ ($1\ ns$)
Droop voltage	$30\ mV$	$58\ mV$	$94\ mV$	$< 25\ mV$	$76\ mV$	$100\ mV$
Recovery time	$\approx 40\ ns$	$\approx 20\ ns$	$\approx 300\ ns$	$3\ ns$ to $5\ ns$	$\approx 20\ ns$	$200\ ns$
DVS speed Up	N/A	$2.5\ V/\mu s$	N/A	N/A	N/A	$30\ V/\mu s$
DVS speed Down	N/A	$0.9\ V/\mu s$	N/A	N/A	N/A	$7.4\ V/\mu s$
Output voltage ripple	$30\ mV$	$3.5\ mV$	$30\ mV$	$43\ mV$	-	$100\ mV$
Output capacitor	none	none	none	$100\ pF$	none	none
Peak efficiency	82.7%@1 V 85.1%@1.1 V	78.5%@1 V 77.5%@1.05 V 78%@1.1 V	86.4%@0.85 V 90%@1.1 V	68%@0.55 V 74%@0.7 V 71%@0.8 V 84%@1.1 V	71.5%@3.1 V 73%@3.6 V	45.5%@0.34 V 72.5%@0.72 V 68.5%@0.9 V 65%@0.96 V
Power density W/mm^2	1.9@1 V 3.2@1.1 V	0.06@1 V 0.062%@1.05 V 0.065%@1.1 V	2.17@0.85 V 3.71%@1.1 V	0.062@0.55 V 0.1@0.7 V 0.126@0.8 V 0.242@1.1 V	0.19@3.1 V 0.19@3.6 V	0.146@0.34 V 0.31@0.72 V 0.386@0.9 V 0.412@0.96 V
Area overhead 1 W/mm^2	31.2%	15×	26.9%	3.6%	5×	11.5%

Table 5.5: Comparison with state-of-the-art

CHAPTER 6

Body-bias generator

6.1 Motivations and context

Body-biasing has been introduced as an assist technique in Section 2.4.4. The body effect of the transistor is exploited to speed-up the digital block or to decrease the leakage current. The configuration of body-biasing in CMOS bulk technology is depicted in Fig. 6.1. NMOS and PMOS transistors are in a P-well and in an N-well respectively. The P-well is isolated from the substrate through a deep N-well to apply separated voltages to the NMOS P-well and to the grounded substrate. The deep N-well exhibits the same bias voltage as the one of the PMOS N-well. The body biasing voltage is denoted *vbb*.

When *vbb* is positive, transistors are forward-biased and when *vbb* is negative, transistors are reverse-biased. Since the substrate is grounded, the deep N-well bias voltage, denoted *vdds* must be always greater than 0 V to avoid any substrate current flow. However it is obvious that the junction formed between P-well and N-well layers on one hand, P-well and deep N-well layers on the other hand and the drain/source junction, will conduct during forward biasing. This current is significant on large circuit and limits the benefits of this technique. The value of forward biasing is commonly limited to 300 mV. Similarly reverse biasing is limited when the GIDL[1] becomes significant. The leakage current is reduced in reverse biasing except GIDL. When GIDL is the major contributor to leakage current, reverse biasing is not effective to reduce the leakage current. Moreover the range of *vbb* is limited by the voltage range sustained by the junctions ($\approx 6\ V$) and does not exceed $-3\ V$ in practice to keep safe margins in most bulk technologies. It is also important to note that body-biasing increases the latch-up sensitivity in bulk technology because

[1] Gate induced drain leakage

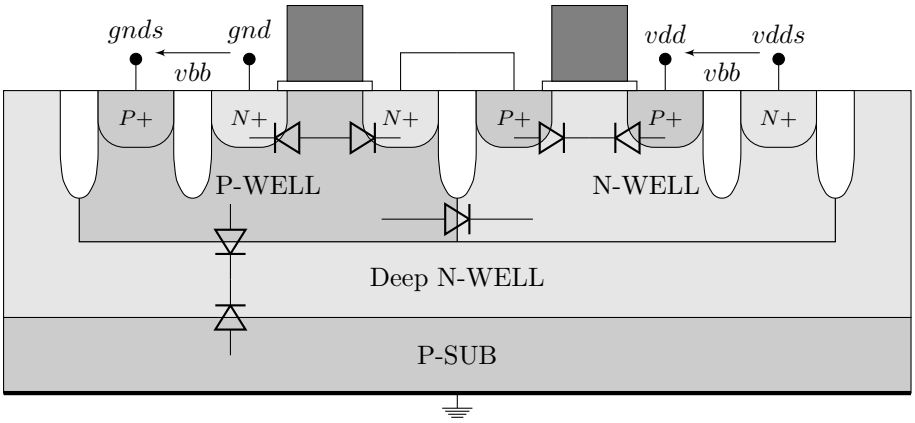


Figure 6.1: Cross section of a CMOS inverter in bulk technology.

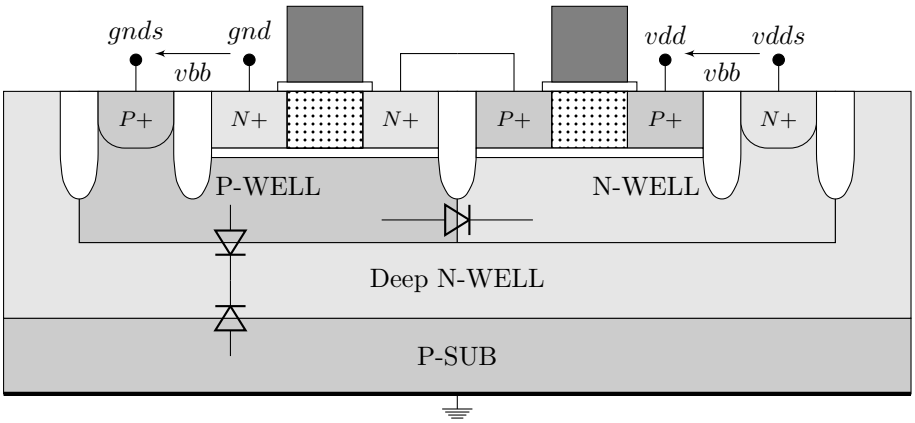


Figure 6.2: Cross section of a CMOS inverter using regular threshold voltage devices in FDSOI technology with regular well option.

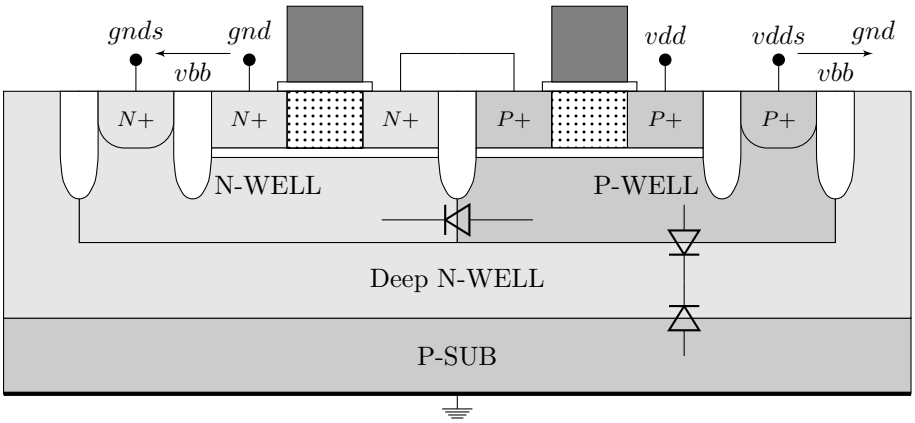


Figure 6.3: Cross section of a CMOS inverter using low threshold voltage devices in FDSOI technology with Flip-well option.

the carriers injected can turn-on the well known parasitic thyristor structure.
FDSOI technology has been recently introduced by STMicroelectronics in the 28nm node. An ultra thin non-doped body is isolated from the substrate by a thin buried oxide. This way the drain/source junctions are removed and the associated leakage current as well. P-well and N-well are implemented under the thin oxide of the NMOS and the PMOS respectively. The bias voltage of those wells can be used to control the threshold voltage of the transistors. It can be considered as a second gate, the so-called **back-gate**. The cross section of a CMOS inverter in FDSOI is shown in Fig. 6.2.
This device architecture constitutes the regular threshold devices of the technology. Similarly to bulk technology, a body-biasing strategy requires a deep N-well to isolate the P-well from the substrate. A wide reverse body-biasing schemes (up to $-3\ V$) can be applied until the breakdown voltage of the well junctions ($\approx 6\ V$). FDSOI reduces the GIDL because the channel is electrically isolated by the BOX. Forward-biasing is also extended but in a lower amount. The well junctions start to conduct for a voltage around 300 mV. This case occurs when vbb is equal to $\frac{vdd}{2} + 150\ mV$. The Flip-well architecture has been developed to offer full forward capability [7]. This architecture is presented in Fig. 6.3. A N-well is implemented under the NMOS transistor instead of a P-well and conversely for PMOS transistors. The devices exhibit a lower threshold voltage compared to the conventional architecture. Due to the well configuration, $vdds$ and $gnds$ are both tied to ground to keep all the junctions reverse-biased during normal operation. Body-biasing imposes $gnds = vbb$ and $vdds = -vbb$ to avoid substrate current flow. Reverse body-biasing is effective up to $vbb = -150\ mV$ because the voltage across the junctions is equal to 300 mV and the junction current starts to increase. In the forward mode, all the junctions are reversed biased and vbb is only limited by the breakdown voltage. The threshold voltage can be strongly reduced with the Flip-well architecture. The voltage range in the various cases and the operating regions are summarized in Fig. 6.4.

The challenge for the designer is to find voltage regulators that exploit the body-biasing capability. Voltage regulators with bipolar features are required regarding the body-bias range in Fig. 6.4. Moreover integration constraints and costs call for fully integrated solutions to apply the body-biasing techniques to a large number of blocks. A body-bias generator with reverse and forward capabilities is presented in [23]. Low output impedance DACs are used to provide the positive voltage and charge-pump level shifters are employed in reverse mode. Despite low silicon area overhead of the proposed solution, systems using a buffer amplifier are preferred for faster transient response [7, 107–109]. A modular output buffer is implemented

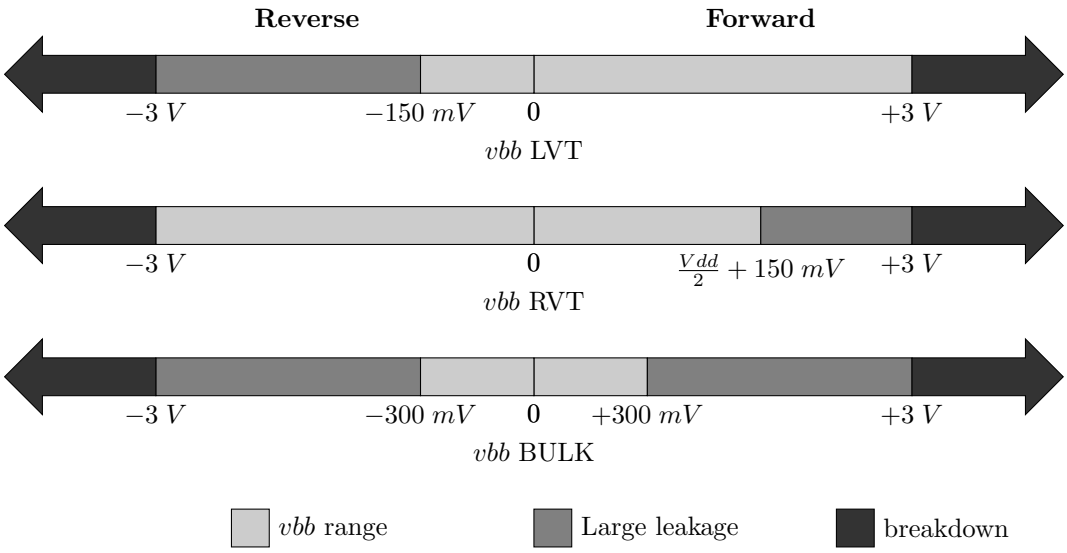


Figure 6.4: Body biasing range in bulk process (Fig. 6.1), FDSOI regular well (Fig. 6.2) and FDSOI Flip-well architectures (Fig. 6.3)

in [108] in order to address a wide range of digital circuit area. However the power consumption is critical for ultra low power purpose and a reverse-bias generator based on a low-drop out regulator and a negative SC converter is proposed in [110]. A current consumption of 350 nA is reported. We propose first to design the same architecture but dedicated to forward body-biasing scheme for Flip-well FDSOI technology instead of reverse scheme in bulk technology. The available generator for this purpose is detailed in [7] and the architecture is depicted in Fig. 6.5. Two class AB amplifiers are used to buffer the voltages coming from the two digital-to-analog converters. The voltage of the N-well is *gnds* and the voltage of the P-well is *vdds*. Since *vdds* is negative, a fully integrated SC converter is used to convert the main supply voltage level of 1.8 V to a negative rail of -1.8 V. A capacitor of 1 μF is implemented off-chip to hold the negative voltage during current surge. The negative converter is only designed to provide the static current consumed from the -1.8 V rail. This architecture is able to change the voltage level in less than 1 μs at the cost penalty of a large power consumption and a large silicon area. This architecture is not suitable for ultra low-power and low-cost circuit.

6.2 Proposed architecture

The negative SC converter in 6.5 is unregulated what imposes a large value of tank capacitor. This capacitor is thus off-chip due to its large value. The power delivery network, the board and package design is more complex. Moreover a part of the

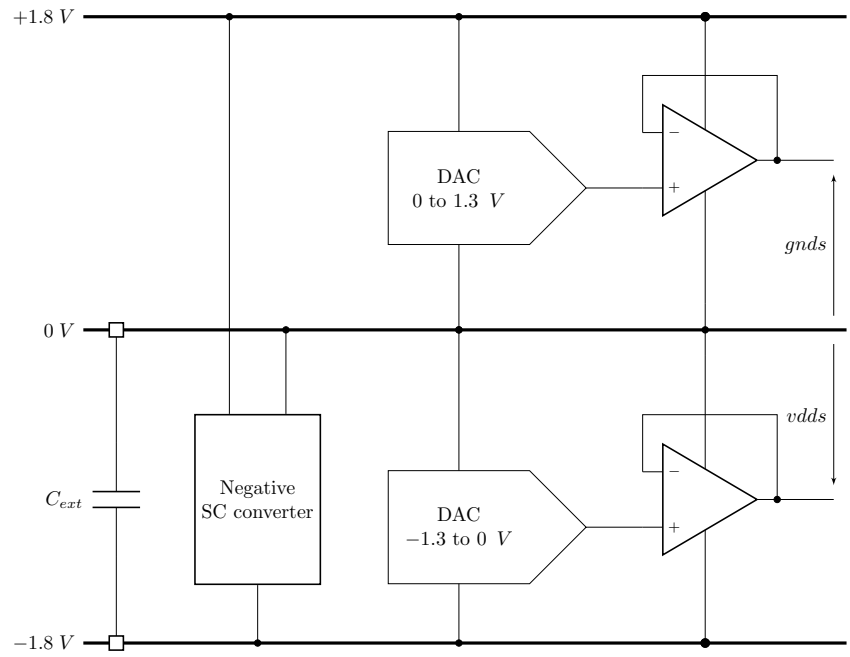


Figure 6.5: Possible architecture of a high performance body-bias generator in 28nm FDSOI [7]

power consumption comes from the transient requirements. Ultra low-power SoC exhibits less aggressive specification. We propose to design a fully integrated and regulated negative voltage regulator which will directly drive the P-well. By the way one of the main contributors to the power consumption, the class-AB amplifier in 6.5 is removed. The integration level is increased since the external capacitor is removed too. The positive generator can then be a simple low-drop out regulator as in [110].

The architecture of the proposed negative voltage regulator is depicted in Fig. 6.6. The output voltage is regulated using a frequency modulation voltage loop through a VCO and a PI controller. A bandgap reference voltage provides the reference level to the PI controller. Since the regulation must be performed in the positive domain, a voltage sensor is used to convert the negative output voltage to a positive voltage fed to the PI controller. The selection of the output voltage level is achieved with a programmable feedback network included in the voltage sensor. The common mode voltage of the PI controller is also maintained equal to the voltage reference level independently of the output voltage. This considerably simplifies the constraints on the design of the PI controller. In addition the digital-to-analog converter in 6.5 is not required. The architecture in Fig. 6.6 is therefore compact what is essential in order to achieve a low-power consumption and high integration factor.

The physical implementation of each blocks is detailed in the next Sections.

6.3 Programmable voltage sensor

The objective of the programmable voltage sensor is three-fold. It translates the negative output voltage into the positive domain. Second it is involved in the selection of the desired output voltage. Finally it ensures a minimal power consumption in the SC converter necessary to perform the control. This voltage sensor is based on a programmable resistive divider as depicted in Fig. 6.7. The intermediate node of the resistive divider is connected to the feedback node, V_{fb} using transmission gates. The expression of the voltage V_{fb} is:

$$V_{fb} = (1 - K) \cdot Vneg + K \cdot 1.8 \tag{6.1}$$

The value of K depends on the resistance values and the selected node in the divider. Each resistance comprises a set of unit resistance for matching purpose. The targeted value is achieved by placing the proper number of unit resistances in parallel. The unit resistance value determines the current consumed by the resistive divider. A large value results in a low consumption but the area overhead becomes more important. Unfortunately the current consumption depends on the negative voltage value and can be very small near the ground voltage. The values of K are given in Table. 6.1.

6.4 Negative SC converter

6.4.1 The power stage

Negative SC converters have been already reported in literature for audio power supply [111] and analog purposes [112]. The power stage chosen for the body-bias generator is implemented with a cross-coupled structure [113] as depicted in Fig. 6.8. In a first phase, the flying capacitor, C_A, is charged to the input voltage, V_{in}, through $P2A$ and $P1A$ while the flying capacitor, C_B, is connected between ground and the output node through $N2B$ and $N1B$. On the contrary, in a second phase, C_A is now discharged into the output node through $N1A$ and $N2A$ and C_B is charged to the input voltage through $P2B$ and $P1B$. The output voltage is negative because the polarity of the flying capacitors is inverted. The opposite switching actions of the subcells are ensured with two non overlapped clocks and their opposites. A deadtime guarantees that both switches are off between each transitions. No shout-through current occurs what increases the efficiency. The clock diagrams are shown in Fig. 6.9.
The choice of a cross-coupled structure is motivated by the driving challenge. The PMOS transistors $P1A$ and $P1B$ are used to implement the switches instead of

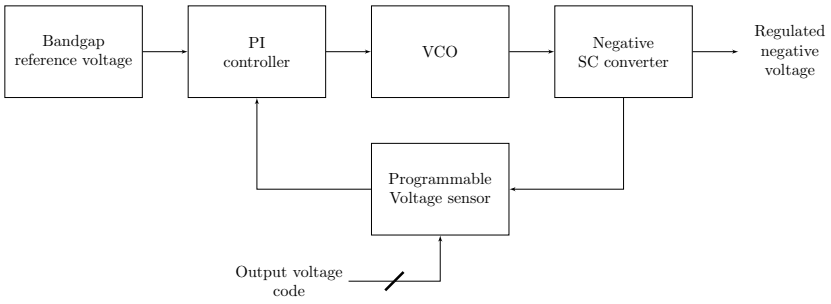


Figure 6.6: Diagram of the proposed architecture for a negative voltage regulator

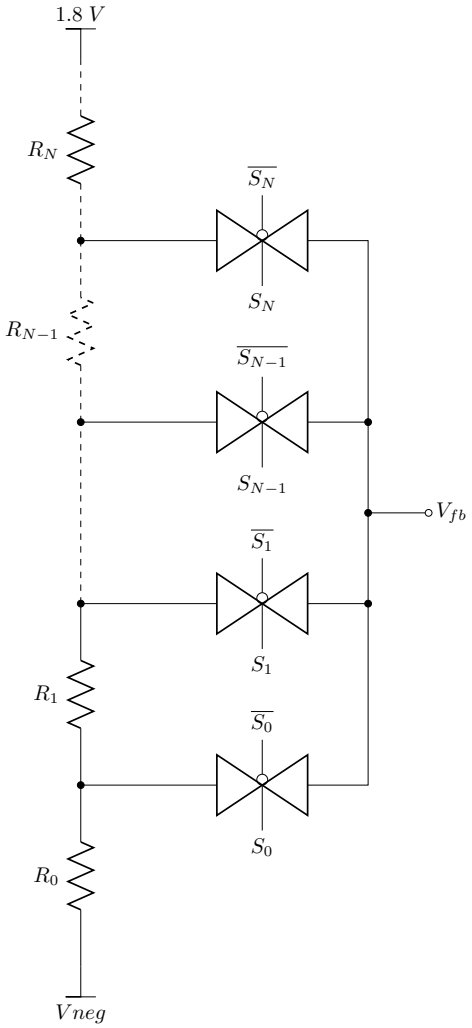


Figure 6.7: Schematic of the voltage sensor with a programmable resistive divider

	$Vneg\ [mV]$	K	$1-K$
1	-100	0.3158	0.6842
2	-200	0.3000	0.7000
3	-300	0.2857	0.7143
4	-400	0.2727	0.7273
5	-500	0.2609	0.7391
6	-600	0.2500	0.7500
7	-700	0.2400	0.7600
8	-800	0.2308	0.7692
9	-900	0.2222	0.7778
10	-1000	0.2143	0.7857
11	-1100	0.2069	0.7931
12	-1200	0.2000	0.8000
13	-1300	0.1935	0.8065

Table 6.1: Parameter values of the resistive divider

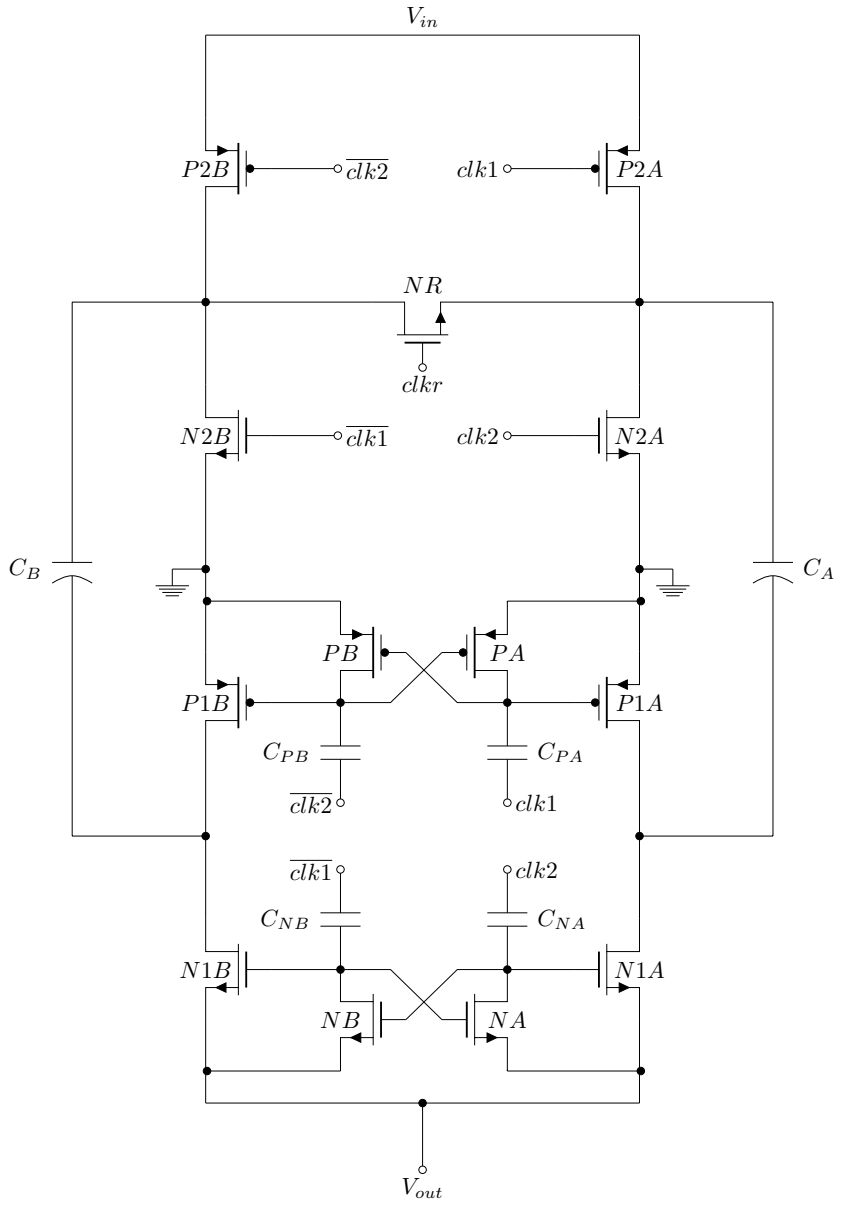


Figure 6.8: Schematic of the proposed architecture for the negative voltage regulator

NMOS transistors because NMOS transistors would be inappropriately turned on by the action of the low-side switches $N1A$ and $N1B$. Unfortunately the gate of the PMOS switches must be pulled to a negative value to fully turn them on. In the same time, the sources of the transistors $N1A$ and $N1B$ are connected to a negative node. A proper gate voltage is required for a reliable operation. That is the reason why a bootstrap structure is implemented.

The NMOS bootstrap driver is presented in Fig. 6.10. The capacitors Cg_{NA1} and Cg_{NB1} represent the equivalent capacitors of the gates of the transistors $NA1$ and

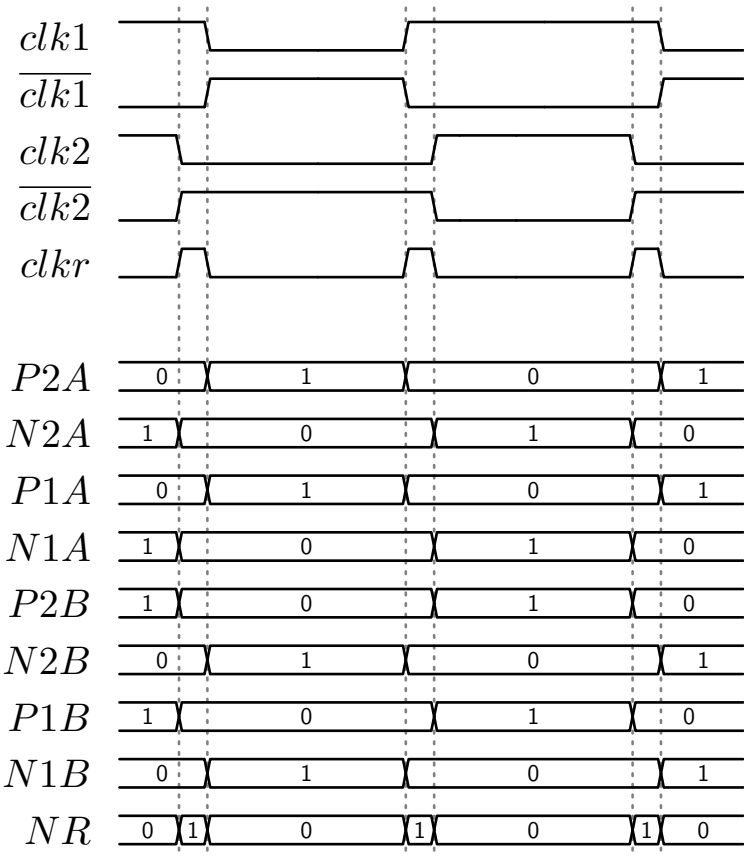


Figure 6.9: Timing diagram of the clocks and the transistor states in the negative SC converter in Fig. 6.8

$NB1$ respectively. Two extra capacitors Cg_{NB} and Cg_{NA} also symbolize the gate capacitors of transistors NA and NB respectively. The operation is separated into two phases. During the first phase, $\overline{clk1} = L$ (0 V) and $clk2 = H$ (1.8 V). At the startup of the converter, the output voltage is null. The source voltage, denoted V_s, is therefore equal to 0 V. The capacitors C_{NA} and C_{NB} are initially discharged. The transistor NB is thus turned on while NA remains off. The voltage at node B is equal to V_s if the transistors do not exhibit too large gate leakage current. The voltage at node A is 1.8 V. The equivalent schematic during this first phase is shown in Fig. 6.11. The transistor NB is replaced by its on-state resistance, R_{on} and the transistor NA by an ideal open-circuit in a first approximation. The resistance Rb is used to represent the output resistance of the clock buffer. The capacitor C_{NA} charges to V_s through Rb and R_{on}. Then in the second phase of operation, $\overline{clk1} = H$ (1.8 V) and $clk2 = L$ (0 V). The voltage across the capacitor C_{NA} is equal to Vs at the beginning of the second phase. The charges are distributed over the capacitors Cg_{NB1}, Cg_{NA} and C_{NA} as shown in Fig. 6.12 and the voltage at

node B is then

$$V_B = \frac{C_{NA}\,(Vs + 1.8) + (Cg_{NB1} + Cg_{NA})\,Vs}{C_{NA} + Cg_{NB1} + Cg_{NA}} \tag{6.2}$$

If $C_{NA} \gg Cg_{NB1} + Cg_{NA}$, the voltage at node B is equal to $V_s + 1.8\ V$ and the transistor NA is turned on. Similarly to the first phase of operation, the capacitor C_{NB} is charged to V_s though R_{on} and Rb. The voltage at node A is equal to V_s what maintains the transistor NB off. Thus the voltage at nodes A and B are alternatively switched between V_s and $V_s + 1.8\ V$, ensuring that transistors $N1A$ and $N1B$ are properly driven independently from the value of the output voltage.

The PMOS bootstrap driver depicted in Fig. 6.13 has a similar behavior. The capacitors C_{PA} and C_{PB} are initially discharged. The gate capacitors of transistors $P1A$, $P1B$, PA and PB are represented by Cg_{PA1}, Cg_{PB1}, Cg_{PA} and Cg_{PB} respectively. During the first phase of operation, $\overline{clk2} = H\ (1.8\ V)$ and $clk1 = L\ (0\ V)$. The voltage at node C is pulled to ground through the resistance of the clock buffer, Rb, as shown in Fig. 6.14. The voltage at node D is equal to $1.8\ V$ since C_{PB} is discharged. The transistor PB is thus turned-on imposing that the transistor PA remains off. The capacitor C_{PB} charges to $V_s - 1.8\ V$ through R_{on} and Rb. Then in the second phase of operation, $\overline{clk2} = L\ (0\ V)$ and $clk1 = H\ (1.8\ V)$. Similarly to node D in the first phase, the voltage at node C is tied to $1.8\ V$ since the capacitor C_{PA} is discharged. This causes the transistor PB to turn off. The voltage at node D is evaluated from the charge redistribution between Cg_{PB1}, Cg_{PA} and CPB as shown in Fig. 6.15 and

$$V_D = \frac{C_{PB}\,(Vs - 1.8) + (Cg_{PB1} + Cg_{PA})\,Vs}{C_{PB} + Cg_{PB1} + Cg_{PA}} \tag{6.3}$$

if $C_{PB} \gg Cg_{PB1} + Cg_{PA}$, the voltage at node D becomes $V_s - 1.8\ V$. The transistor PA is thus turned-on and the capacitor C_{PA} charges to $V_s - 1.8\ V$ through R_{on} and Rb. The voltage at node C is equal to V_s and the transistor PB remains off. The cycle is repeated and the transistors PA and PB are driven between V_s and $V_s - 1.8\ V$, independently of the value of V_s. The NMOS and PMOS bootstrap drivers require that the bootstrap capacitors are larger than the ones of the transistor gates. The on-state resistance, R_{on} and the output resistance of the buffer, Rb must be kept as low as possible. Small values will increase the tracking capability of V_s but too small values will result in large parasitic capacitors.

The bootstrap scheme allows a reliable operation of the power stage in Fig. 6.8. This power stage can be used as a voltage doubler without redesign. The source of the transistors $P1A$ and $P1sB$ becomes the output node while the previous one is put to ground. The power stage can be implemented with thin oxide devices if the clock signals ensure a proper voltage operation.

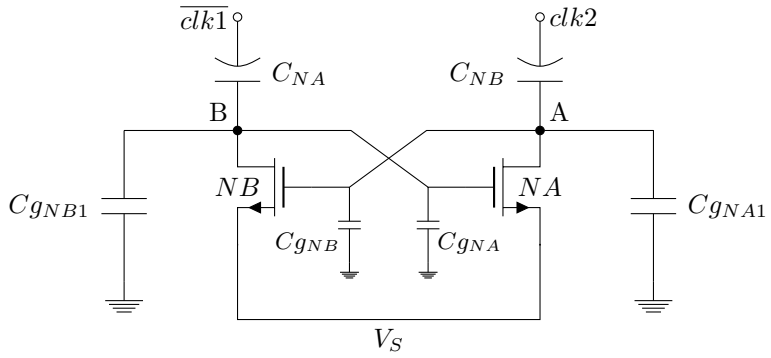


Figure 6.10: Diagram of the low-side NMOS driver

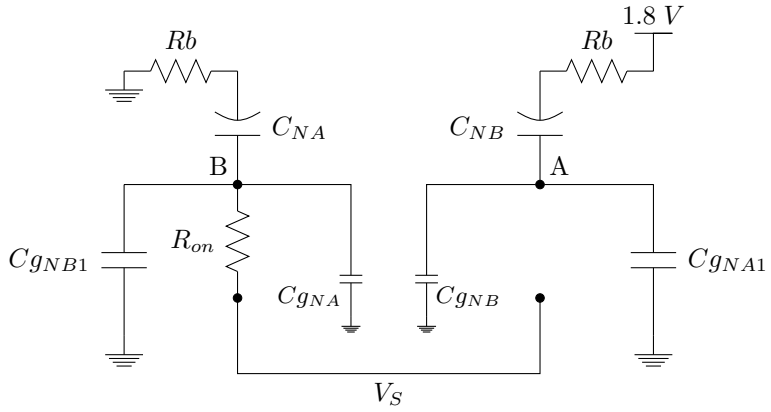


Figure 6.11: Equivalent circuit of the low-side NMOS driver during the first phase of operation

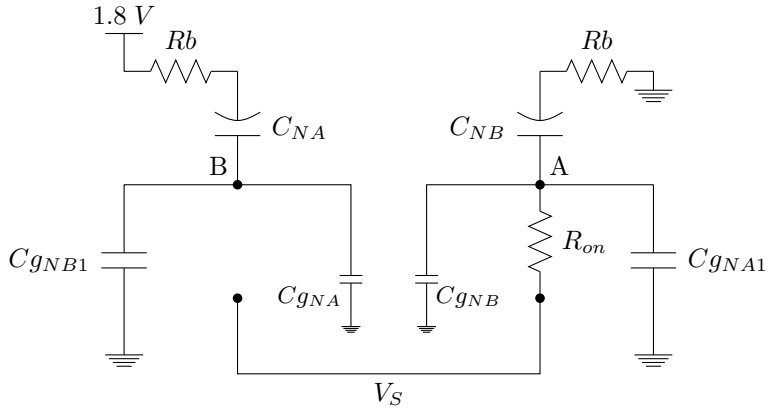


Figure 6.12: Equivalent circuit of the low-side NMOS driver during the second phase of operation

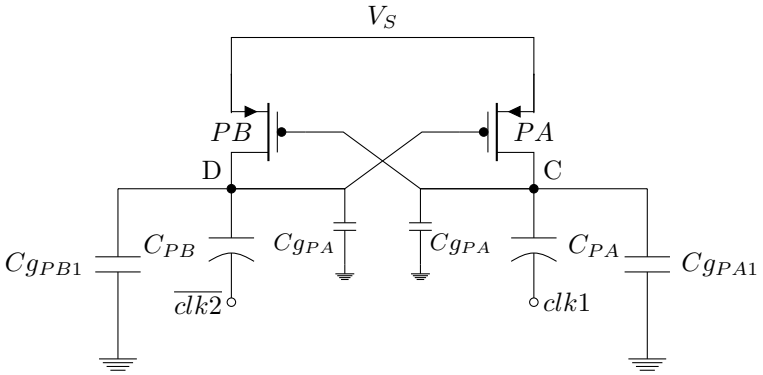


Figure 6.13: Diagram of the low-side PMOS driver

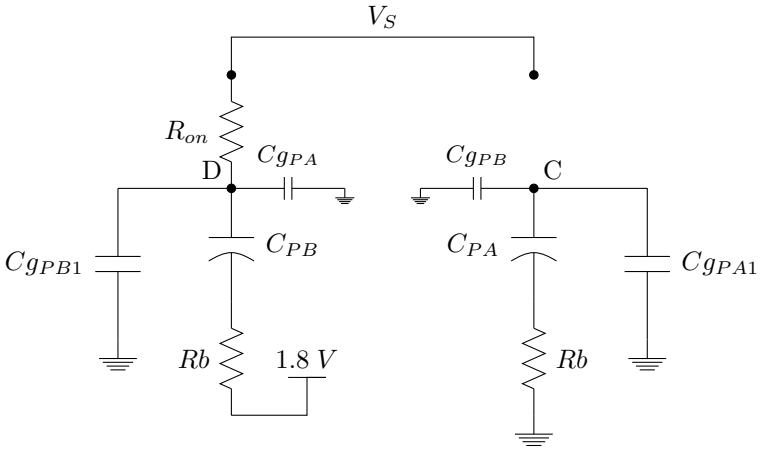


Figure 6.14: Equivalent schematic of the low-side PMOS driver during the first phase

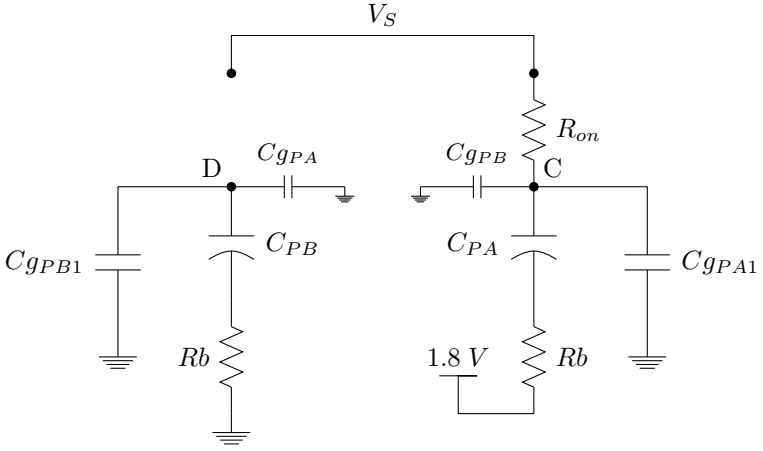


Figure 6.15: Equivalent schematic of the low-side PMOS driver during the second phase

6.4.2 Flying capacitor selection

The choice of the flying capacitors depends on the capacitor density and the parasitic capacitors. The FDSOI technology offers MOM[2] capacitors, MOS capacitors and MIM capacitors. MIM capacitors cannot sustain more than 1.4 V while the application requires 1.8 V. It is important to mention that MOS capacitors can be only used in strong inversion in FDSOI. A charge recycling scheme is applied to reduce the parasitic losses [48]. The transistor NR in Fig. 6.8 shorts the top plate of the flying capacitors during deadtimes. A similar scheme can be applied to the bottom plate of the flying capacitors but the control of the switch would therefore be more challenging and the complexity of the circuitry would result in a higher consumption than the saving in losses. Charge recycling of the bottom plate parasitic capacitance is useful for MOM capacitors since they exhibit the same parasitic coupling from the top and the bottom plates.
Various configurations are explored for the PMOS and the NMOS over regular and low-threshold voltage devices. The configurations are compared in terms of area, capacitor values and parasitics capacitors. The top plates and the bottom plates are respectively tied to 1.8 V and 0 V in the charging phase. In the discharging phase, the top plates are now connected to ground and the bottom plate to the negative voltage. For the NMOS, the top plates are thus connected to the gate and the bottom plates to the source/drain to maintain the transistor in strong inversion. For the PMOS, the top plates are connected to the source/drain and the bottom plates to the gate of the transistor. The results of the analysis are given in Table 6.2.
Each configuration is referenced to a figure: C denotes the value of the capacitor, Cp the parasitic capacitor. The most compact configurations correspond to the regular threshold voltage NMOS in Fig. 6.16a or the low threshold voltage PMOS in Fig. 6.17b. Their implementations require only a P well biased with the same voltage as the substrate what minimizes the area. The bottom plate parasitic capacitor is the BOX capacitor. The BOX capacitor can be added to the MOS capacitor by connecting the gate (top plate for NMOS and bottom plate for PMOS) to the back gate (bottom plate for NMOS and top plate for PMOS) as shown in Fig. 6.16d, Fig. 6.16f, Fig. 6.17c and Fig. 6.17e respectively. The configuration of the PMOS in Fig. 6.17c is not suitable because the junction formed by the substrate and the N-well conducts when the bottom plate is tied to the negative voltage. The same issue arises for the low threshold voltage NMOS transistor in Fig. 6.16e. In Fig. 6.17e and Fig. 6.16c, the parasitic capacitor is formed by the P-well-deep N-well junction and its value is minimized because the junction is reversed biased between $-1.8\ V$

[2]Metal oxide metal

and $-1.8\ V + V_{neg}$. The parasitic capacitors can be minimized by applying a floating voltage to the well [52]. Nonetheless this scheme is not explored due to ESD issues in SoC environment. Generally the BOX capacitor is very small compared to the MOS capacitor. Configurations with BOX capacitor as a parasitic capacitor are better and smaller. Schemes employing several wells always increase the area and the parasitic. A charge recycling scheme can be applied when the parasitic capacitor is connected to the top plate. It is tempting to use the configuration with the largest value of capacitor but the value of parasitic capacitors is also decisive.

The bottom parasitic capacitance has indeed a strong impact on the output resistance of the converter and its output voltage [114]. A sampled-data model of the negative SC converter with a bottom parasitic capacitance is derived and the different topologies are depicted in Fig. 6.18. The state-space model of the negative SC converter is given in Appendix B.2 and the model with a bottom plate parasitic capacitor in Appendix B.3. The flying capacitor is denoted C_{fly}, the bottom plate parasitic capacitance is C_{bot} and the on-state switch resistances are indicated as R_{on}. During the charging phase, in Fig. 6.18a, the flying capacitor charges to the input voltage and the bottom parasitic capacitor is discharged to ground. Then in the discharging phase, the flying capacitor is discharged to the output node. The charges are distributed over the output node, the flying capacitor and the bottom plate parasitic capacitor. All the charges are not transfered to the output node and a small amount is lost in the parasitic capacitors. The output impedance is increased compared to an ideal case [114].

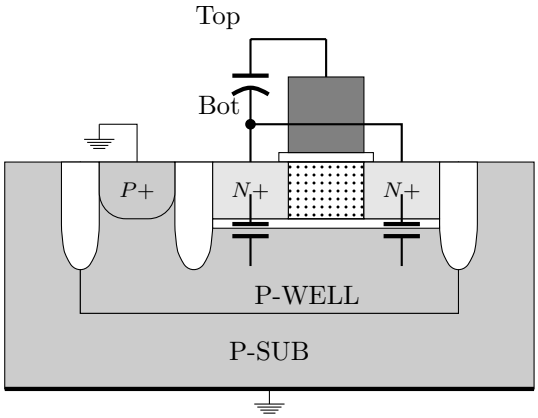
The output resistance is evaluated from the sampled-data model as shown in Fig. 6.19. The output voltage is computed and plotted in Fig. 6.20. The difference between the two curves in the SSL region is explained by the difference in the output resistances. However the difference increases significantly in the FSL region. An explanation is given in Fig. 6.21. The ratio of the SC converter is extracted from the sampled-data modeling using the DC value of the audio susceptibility (Section 3.6.2). A constant difference appears in the SSL region due to the charge redistribution. Under no load condition, the ratio n of the converter is given by:

$$n = \frac{C_{fly}}{C_{fly} + C_{bot}} \tag{6.4}$$

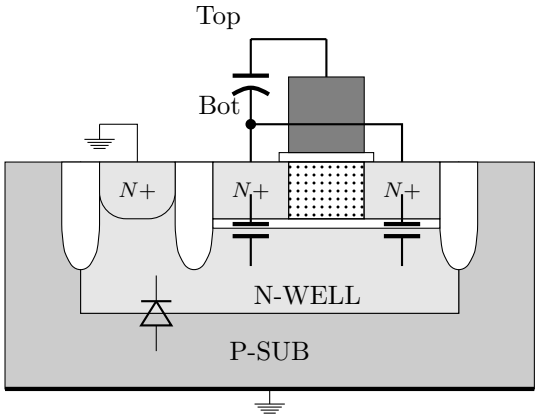
This expression is true in the SSL region where the charges are totally transfered. In the FSL region the converter ratio decreases. A current proportional to the switching frequency is wasted to ground. It has been introduced as an equivalent resistance in [114]. It is clear from Fig. 6.19 and Fig. 6.21 that the parasitic capacitance modifies the output resistance by a constant value and the converter ratio becomes frequency dependent. Therefore the bottom plate parasitic capacitor must

Configuration	Fig.	C	Cp	Area	Comments
NMOS RVT	6.16a	C_{MOS}	C_{BOX}	+	
NMOS LVT	6.16b	C_{MOS}	C_{BOX}	−	
NMOS RVT Bottom-back-gate	6.16c	C_{MOS}	P-well Deep N-well	−−	Junction highly reverse biased
NMOS RVT Top-back-gate	6.16d	$C_{MOS} + C_{BOX}$	P-well Deep N-well	−−	Charge recycling
NMOS LVT Bottom-back-gate	6.16e	C_{MOS}	P-sub N-well	−	Diode conduction
NMOS LVT Top-back-gate	6.16f	$C_{MOS} + C_{BOX}$	P-sub N-well	−	Charge recycling
PMOS RVT	6.17a	C_{MOS}	C_{BOX}	−	
PMOS LVT	6.17b	C_{MOS}	C_{BOX}	+	Charge recycling
PMOS RVT Bottom-back-gate	6.17c	$C_{MOS} + C_{BOX}$	P-sub N-well	−	Diode conduction
PMOS RVT Top-back-gate	6.17d	C_{MOS}	P-sub N-well	−	Charge recycling
PMOS LVT Bottom-back-gate	6.17e	$C_{MOS} + C_{BOX}$	P-well Deep N-well	−−	Junction highly reverse
PMOS LVT Top-back-gate	6.17f	C_{MOS}	P-well Deep N-well	−−	Charge recycling

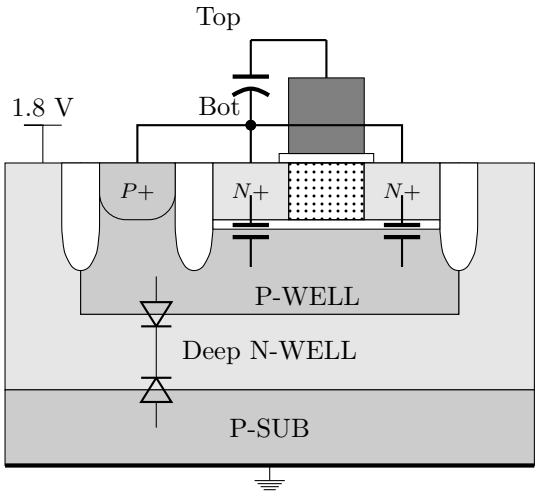
Table 6.2: Capacitor configurations



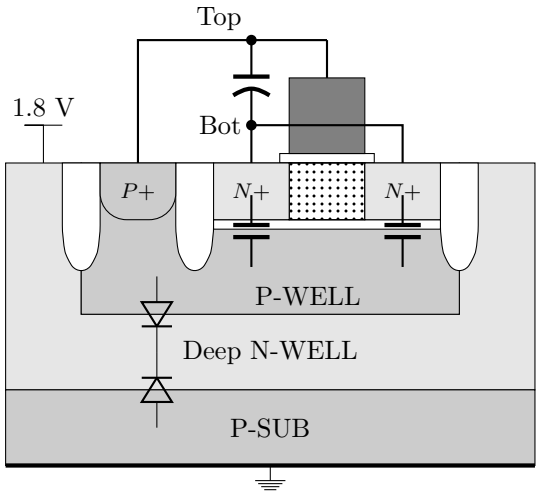
(a) NMOS regular threshold voltage capacitor



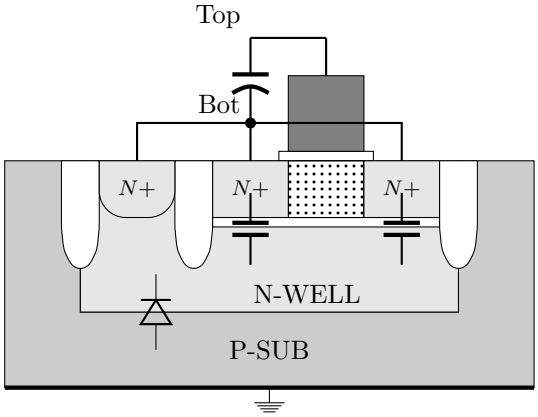
(b) NMOS low-threshold voltage capacitor



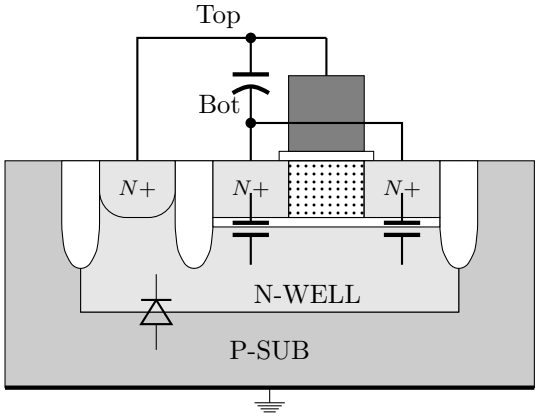
(c) NMOS regular threshold voltage capacitor: Bottom plate connected to the P-Well



(d) NMOS regular threshold voltage capacitor: Top plate connected to the P-Well

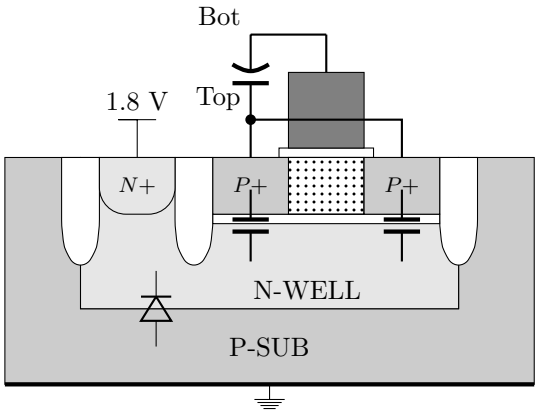


(e) NMOS low-threshold voltage capacitor: Bottom plate connected to the N-Well

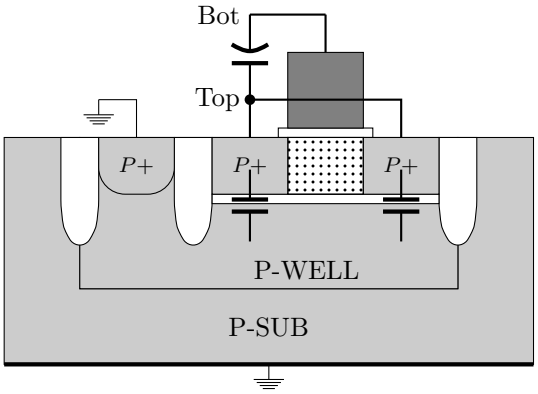


(f) NMOS low-threshold voltage capacitor: Top plate connected to the N-Well

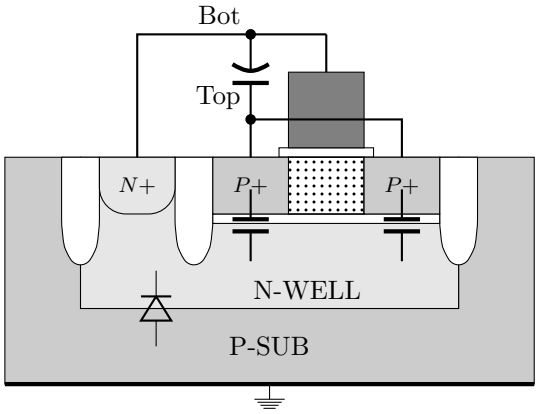
Figure 6.16: NMOS Capacitor configurations



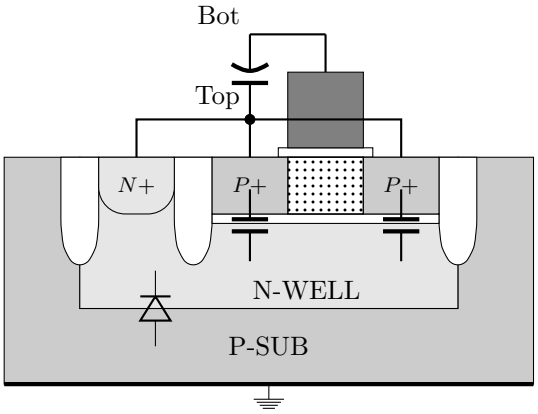
(a) PMOS regular threshold voltage capacitor



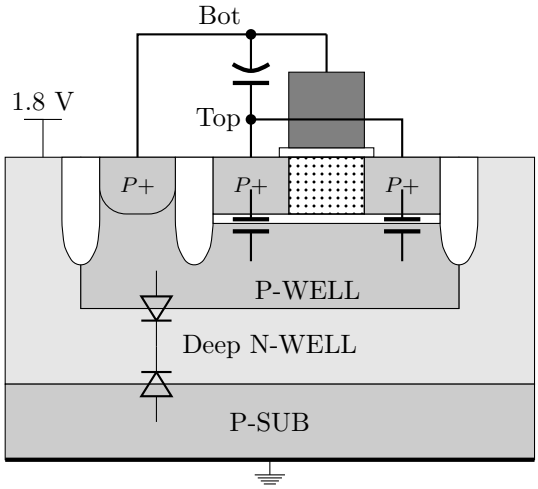
(b) PMOS low-threshold voltage capacitor



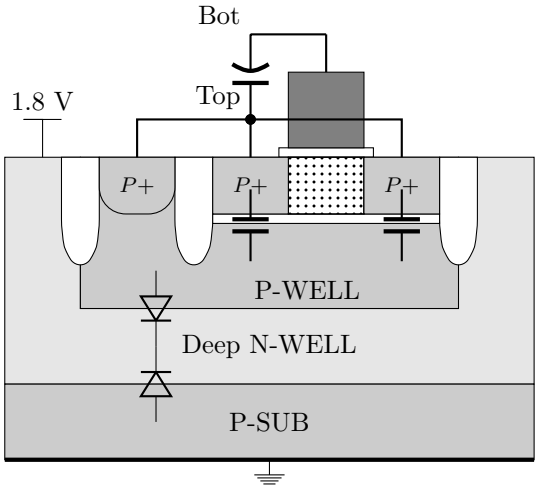
(c) PMOS regular threshold voltage capacitor: Bottom plate connected to the N-Well



(d) PMOS regular threshold voltage capacitor: Top plate connected to the N-Well

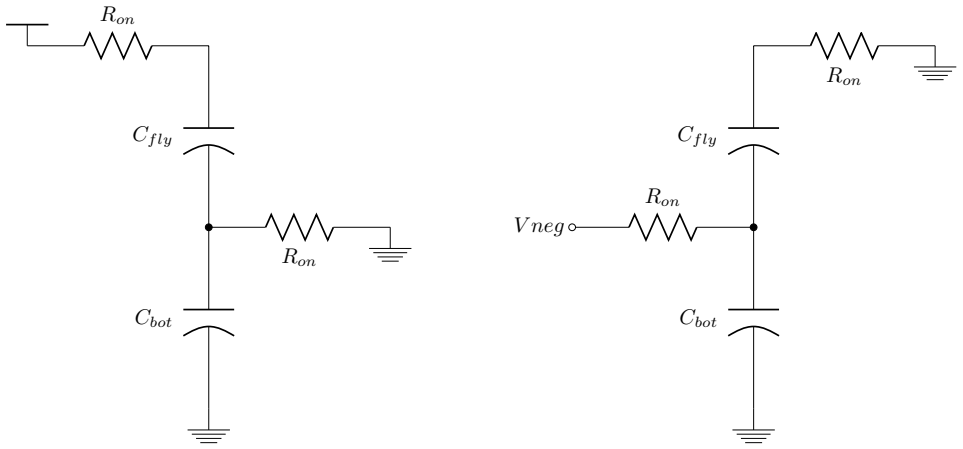


(e) PMOS low-threshold voltage capacitor: Bottom plate connected to the P-Well



(f) PMOS low-threshold voltage capacitor: Top plate connected to the P-Well

Figure 6.17: PMOS Capacitor configurations



(a) Phase 1: charging (b) Phase 2: discharging

Figure 6.18: Equivalent schematics of the negative SC converter with a bottom plate parasitic capacitance

be kept to a voltage as low as possible to enable frequency modulation. Otherwise unstable behavior could occur since the output voltage would decrease with the increase in the switching frequency. Moreover the parasitic capacitor value limits the output voltage range. Finally MOM capacitors exhibit a smaller parasitic ratio than the PMOS configuration in Fig. 6.17b. MOS capacitors are smaller but the MOM capacitor is preferred because of its linear value dependency with respect to the voltage across the device.

6.4.3 Load modeling

The load of the SC converter is represented by the diode of the various wells detailed in Fig. 6.3. The current consumption and the equivalent load capacitor varies with the voltage across the diodes. A model is built with proprietary CAD tools. The tools compute the area of the various diodes for a given size of digital block. The model is extracted for an area of 1 mm^2. This model takes into account the process corner and temperature variations to avoid over-designing. The leakage current and the equivalent capacitor are extracted with respect to the diode voltage over process and temperature variations in Fig. 6.23 and Fig. 6.22 respectively. The load capacitance mainly depends on the corner and always decreases when biasing voltage increases. The leakage current drastically increases at high temperature. The worst case corresponds to the fast corner and $T = 125\,^{\circ}C$. The best case appears with the slow corner and $T = -40\,^{\circ}C$. Modeling of the load is mandatory to latter size the loop behavior.

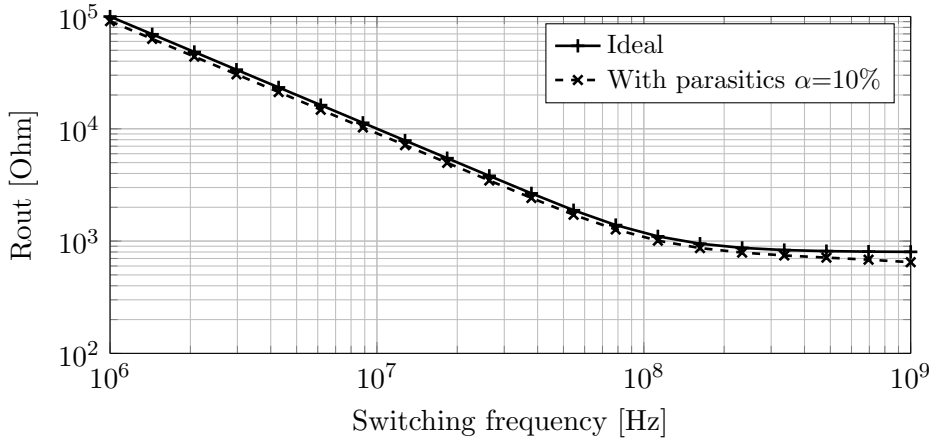


Figure 6.19: Output resistance of the ideal negative SC converter or with a bottom plate parasitic ratio of 10%

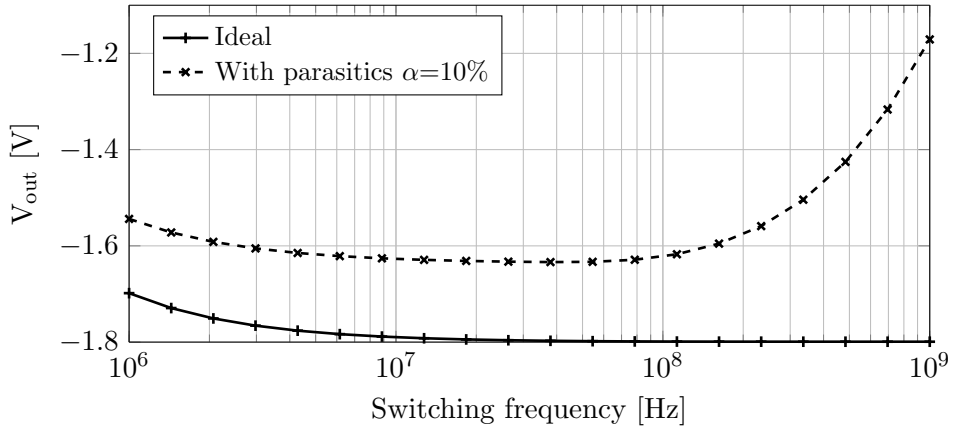


Figure 6.20: Output voltage of the ideal negative SC converter or with a bottom plate parasitic ratio of 10%, for a load current of 1 μA

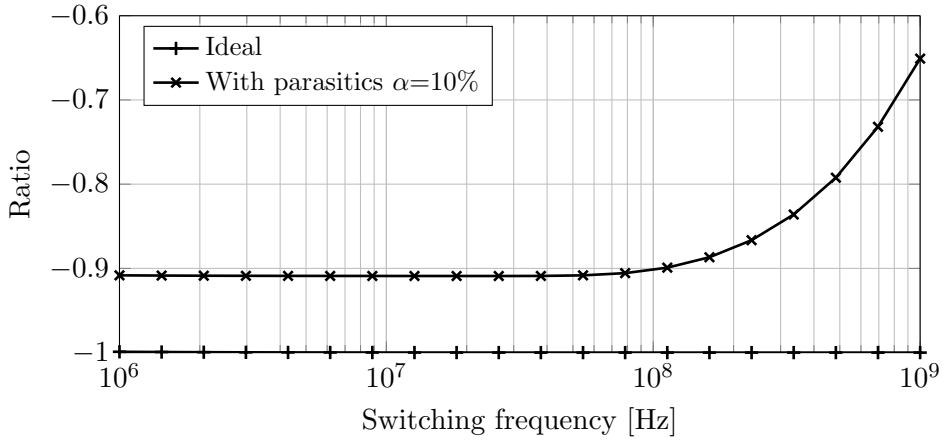


Figure 6.21: Voltage ratio of the ideal negative SC converter or with a bottom plate parasitic ratio of 10%, for a load current of 1 μA

The worst case load current represents a few μA. The size of the power switches can be very small and set to the minimal value available in the process. The value of one flying capacitor is 5 pF and the total resistance of the voltage sensor is 635 $k\Omega$. A simulation is performed to extract the switching frequency-to-output voltage characteristic as well as the current consumption of the SC converter with the load model and the resistance of the voltage sensor. The results are plotted in Fig. 6.24. The parasitic impact occurs behind 20 MHz. The power consumption increases and the output voltage starts to increase as well. The converter can deliver a voltage up to $-1.7\,V$ that easily meet the initial objective of $-1.3\,V$.

6.5 Voltage controlled oscillator

A current-starved VCO is chosen and the schematic is shown in Fig. 6.25. The transistors $N2*$ and $P2*$ form the classical chain of inverters. The transistors $N1*$ and $P1*$ act as controlled current sources depending on the source degenerated transistor NC. The inverter $N2D$-$P2D$ is used to buffer the output clock signal. As well as for a ring oscillator, an odd number of inverters is required to ensure oscillation operation. A chain of 3 inverters is chosen to minimize the power consumption. The oscillation frequency of the current-starved VCO is given by [115]:

$$f_{osc} = \frac{I_D}{N \cdot C_o \cdot V_{supply}} \tag{6.5}$$

Where I_D is the current provided by the current sources, C_o is the equivalent capacitance seen at the output node of each inverter, N is the number of inverters in the chain and V_{supply} is the supply voltage of the oscillator. A resistance, R, is inserted between the source of NC and ground to linearize the gain of the VCO. The frequency is indeed proportional to the current but this current is controlled by the gate voltage of the transistor NC. The current of a transistor is related to the square of the gate-source voltage and with a source resistance, the controlled current I_D becomes:

$$I_D = \frac{g_m}{1 + R \cdot g_m} \cdot V_{ctrl} \tag{6.6}$$

where g_m denotes the transconductance of the transistor NC. If $R \gg \frac{1}{g_m}$, (6.6) becomes:

$$I_D = \frac{1}{R} \cdot V_{ctrl} \tag{6.7}$$

The current is now proportional to the control voltage and the gain of the VCO is determined by the value of the resistance, R.
The frequency range of the VCO is imposed by the transfer characteristic of the SC

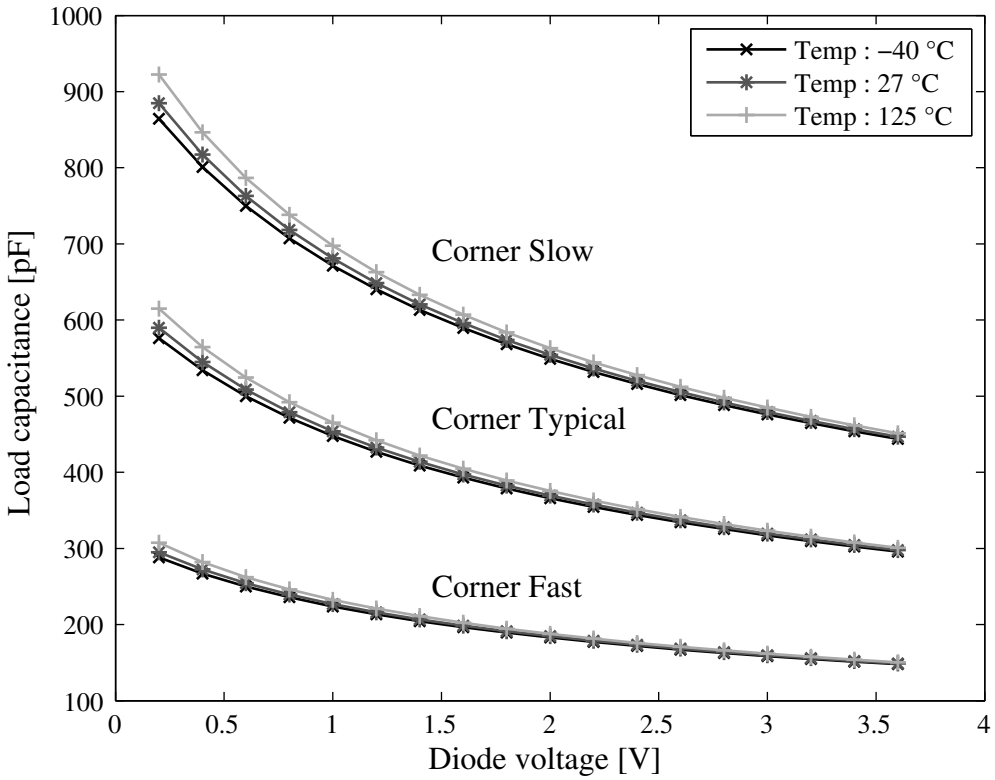


Figure 6.22: Equivalent capacitance of the converter load as a function of the diode voltage over process corner and temperature variations

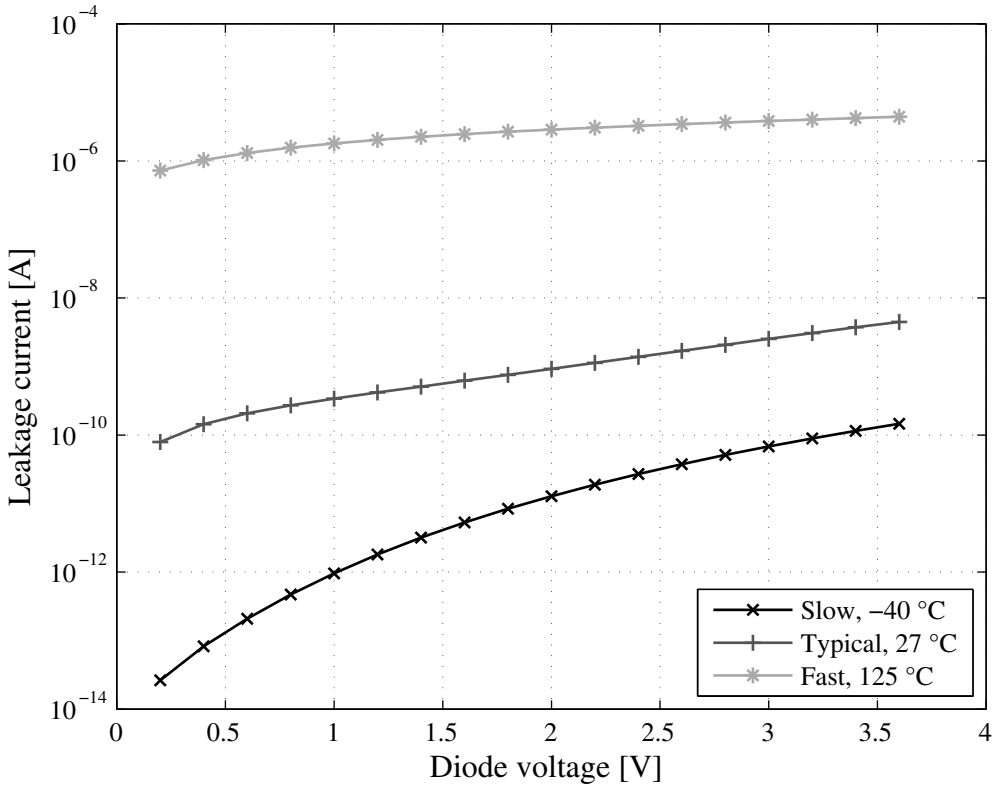


Figure 6.23: Current consumption of the converter load as a function of the diode voltage over process corner and temperature variations

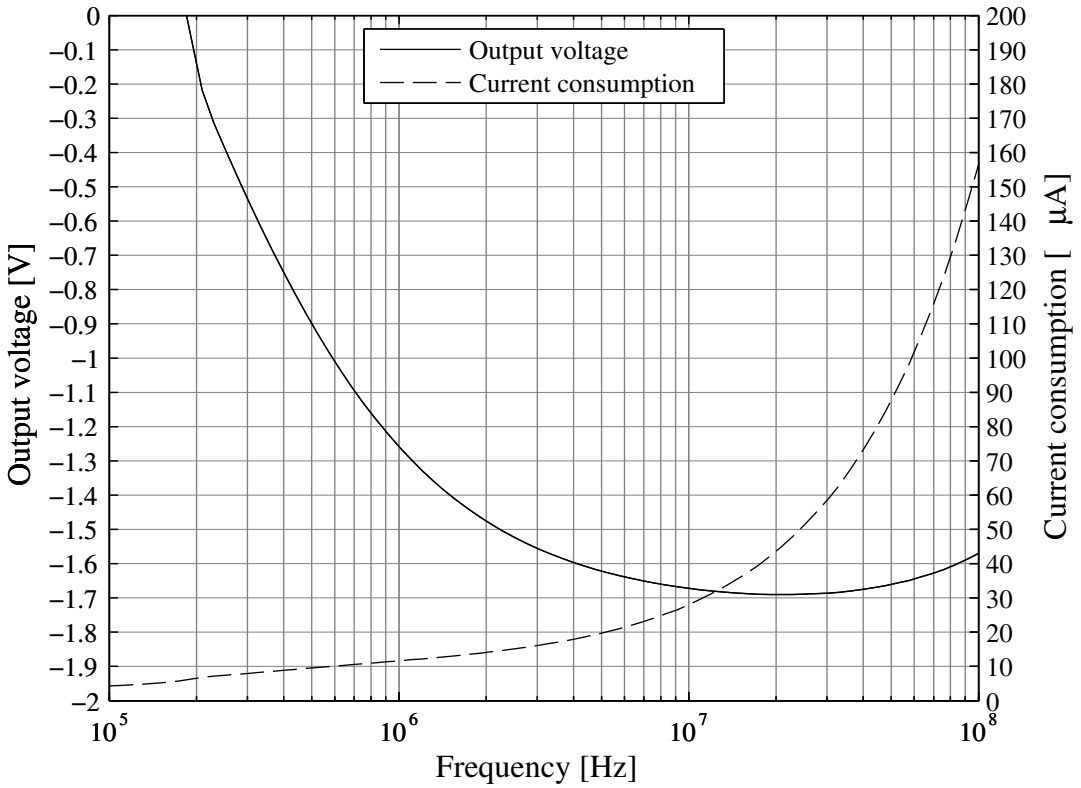


Figure 6.24: Output voltage and overall consumption of the negative SC converter as a function of the switching frequency

converter in order to reach the minimal and the maximal output voltage. According to Fig. 6.24, the minimal switching frequency is 200 kHz and the maximal switching frequency is 1 MHz. The VCO is therefore designed to meet these requirements and the results are shown in Fig. 6.26. The characteristic is also simulated for the worst case corner in order to evaluate the process variation impact. The gain of the VCO is almost linear in the frequency range of interest.

6.6 Voltage loop design

A frequency-modulation with a voltage-loop control is selected. A non-linear average model is build in order to determine and simulate the small-signal behavior of the loop. The output impedance of the converter as a function of the switching frequency is:

$$R_{out} = \frac{1}{2C_{fly}f_{sw}} \coth\left(\frac{1}{16R_{on}f_{sw}C_{fly}}\right) \tag{6.8}$$

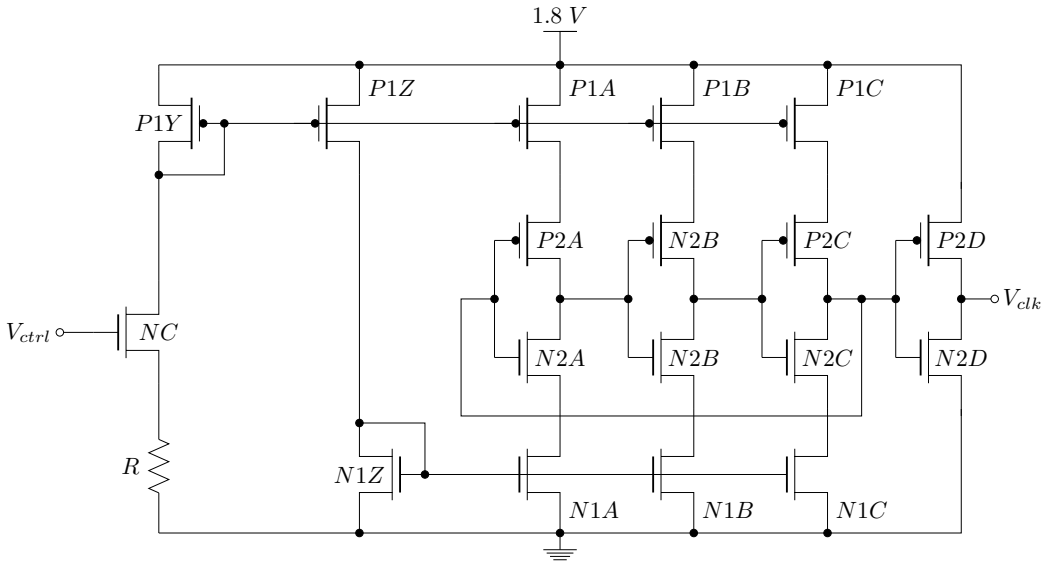


Figure 6.25: Schematic of the current-starved oscillator

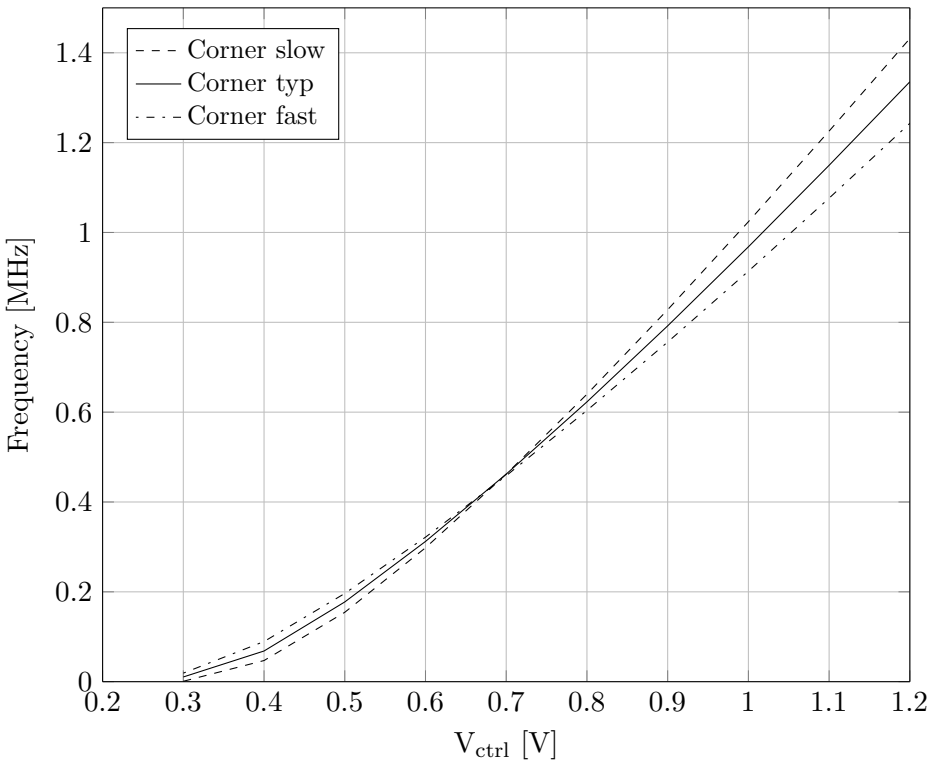


Figure 6.26: Transfer characteristic of the VCO over process variations

The switching limits are

$$R_{SSL} = \frac{1}{2C_{fly}f_{sw}} \tag{6.9}$$

$$R_{FSL} = \frac{1}{16R_{on}} \tag{6.10}$$

The output voltage evaluation including the impact of parasitics is

$$V_{neg} = -\frac{C_{fly}}{C_{fly} + C_{bot}}V_{in} + R_{out}(f_{sw}) \tag{6.11}$$

The VCO is linearized according to the characteristic in Fig. 6.26:

$$f_{sw} = 1.756 \cdot 10^6 \cdot V_{ctrl} - 729 \cdot 10^3 \tag{6.12}$$

The classical PI controller with an operational amplifier and a feedback network is shown in Fig. 6.27. The output of the controller drives the input of the VCO, V_{ctrl}. The feedback voltage is connected to the positive input while the reference voltage is fed to the input of the feedback network. The signals are inverted regarding the classical implementation because of the negative voltage. During the operation, if the negative voltage increases, the feedback voltage will increase. The error signal defined as $V_{fb} - V_{ref}$ will increase and by the way the switching frequency as well. The output voltage will decrease to reach the targeted value.

A bandgap voltage reference gives an nearly constant reference voltage of 1.2 V over temperature. This reference fixes the common mode voltage of the operational amplifier and calls for a NMOS input differential pair. The operational amplifier is depicted in Fig. 6.28. The differential pair NM and NP is cascaded with a simple common source amplifier $P3$. An RC network compensates the amplifier to ensure enough stability margin. The biasing is performed by transistors $N1$, $N2$ and $N3$ and the biasing current is determined by the resistance, R_{bias}. A large value is required to set a low biasing current but this solution avoids any complex biasing circuit at the expense of the silicon area for the resistance, R_{bias}.

The specification of the operational amplifier are determined by the performances the frequency modulation loop. The PI parameters are $K_p = 10.1$ and $T_i = 86.2\ \mu s$. The bandwidth of the amplifier is 10 MHz what ensures enough stability margin over process and temperature variations. The Bode diagram is shown in Fig. 6.29. The amplifier has a high DC gain to satisfy the output voltage accuracy better than $\pm 1\ mV$ over the various operating points and process and temperature variations. A slew-rate of 4 $^{V}/_{\mu s}$ is required to avoid the saturation of the loop during large reference tracking. The output stage of the amplifier is able to drive the VCO over its whole linear range. The compensation network and the slew-rate are carefully evaluated with the characterization of the input capacitance at the control voltage

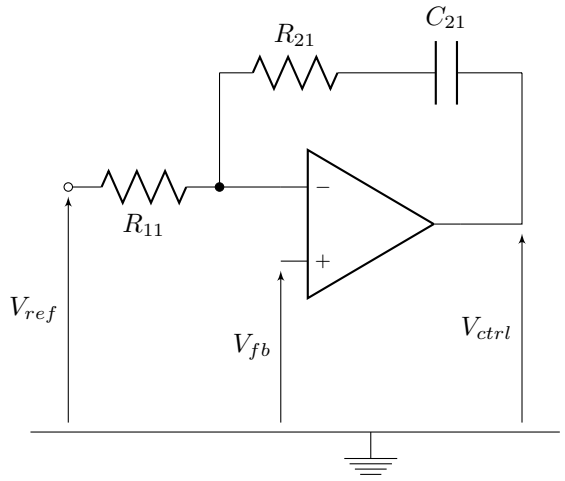


Figure 6.27: Schematic of the PI controller

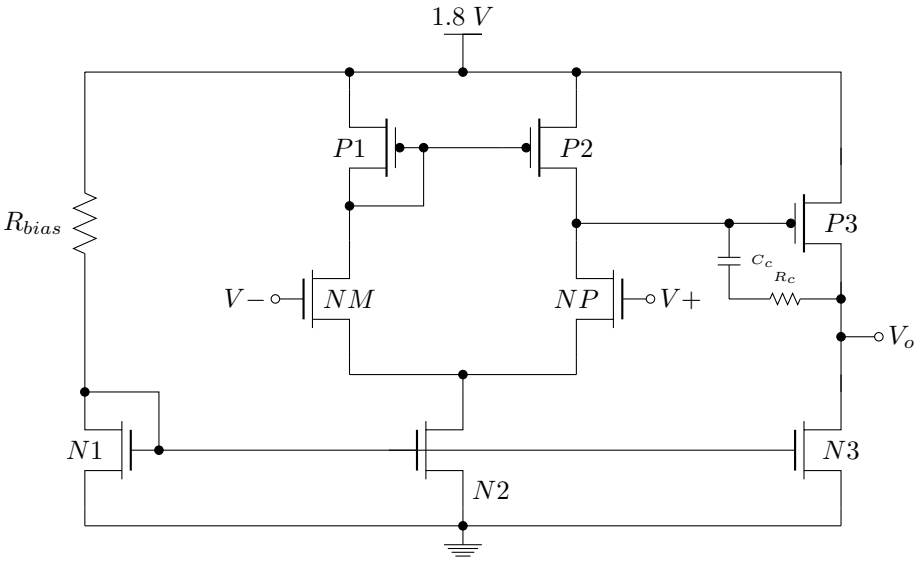


Figure 6.28: Schematic of the operational amplifier used for the PI controller

node. Finally the small-signal behavior of the loop is evaluated for the lower and upper operating point ($-0.1\ V$ and $-1.3\ V$ respectively) and the results are given in Fig. 6.30. Enough phase margin is maintained and the system remains stable over all operating points.

The transient simulation in Fig. 6.31 compares the CMOS Spice circuit simulations and the non-linear average simulation. The output voltage is programmed sequentially to verify all operating points. The accuracy of the linear model is good and can predict the transient results in less simulation time as for the corner characterization. The power consumption of each blocks are also extracted during the transient simulations and reported in Fig. 6.32. At the lowest operating point ($-0.1\ V$), the

power consumption reaches 11 μA while at the highest one (-1.3 V), the power consumption is around $20\mu A$. The power consumption of the operational amplifier is constant over the selected output voltage range. As expected the major contribution comes from the VCO, the SC converter and the voltage sensor. Nonetheless this consumption range is still satisfying for low power application.

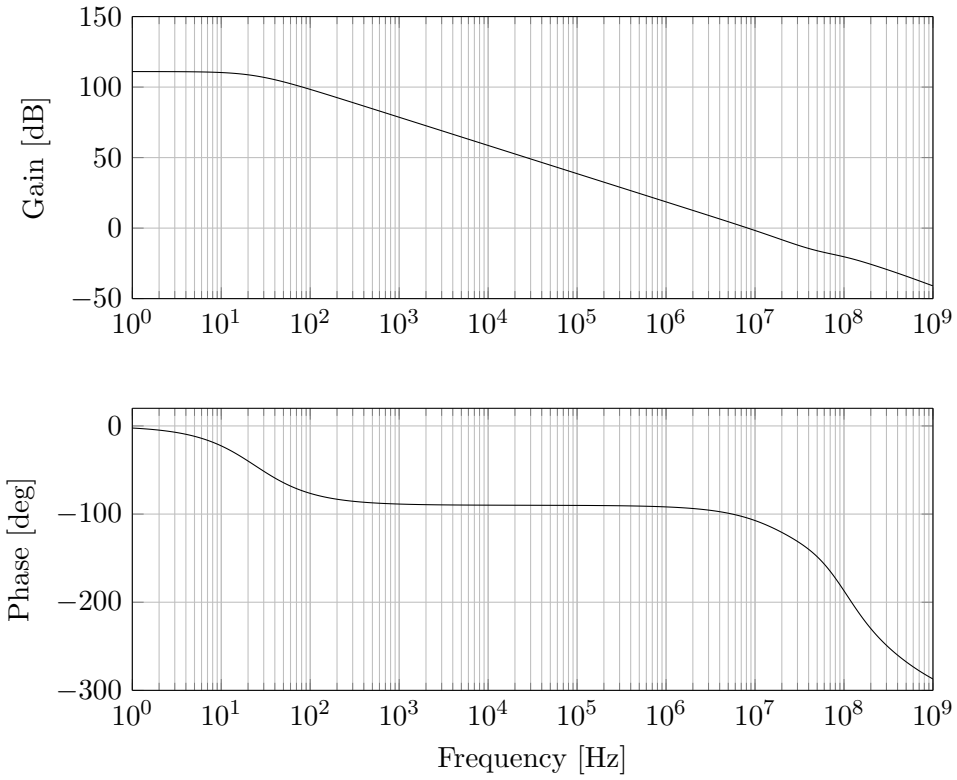


Figure 6.29: Bode diagram of the open-loop transfer function of the operational amplifier in Fig. 6.28 in follower configuration

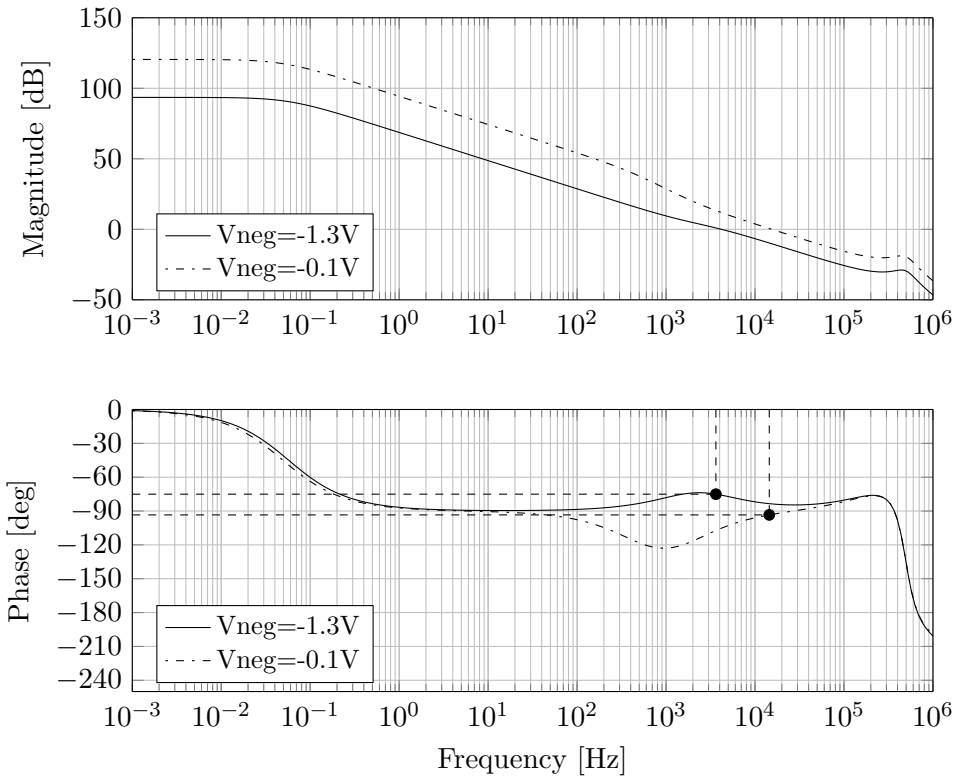


Figure 6.30: Bode diagram of the open-loop transfer function of the negative SC converter under frequency modulation control

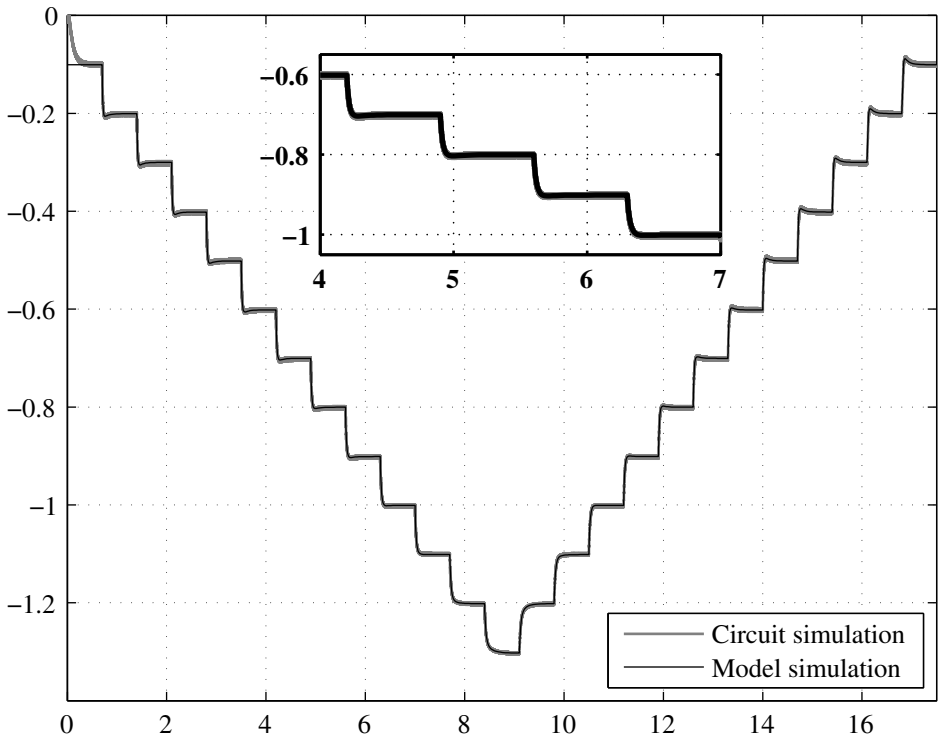


Figure 6.31: Output voltage for various operating points

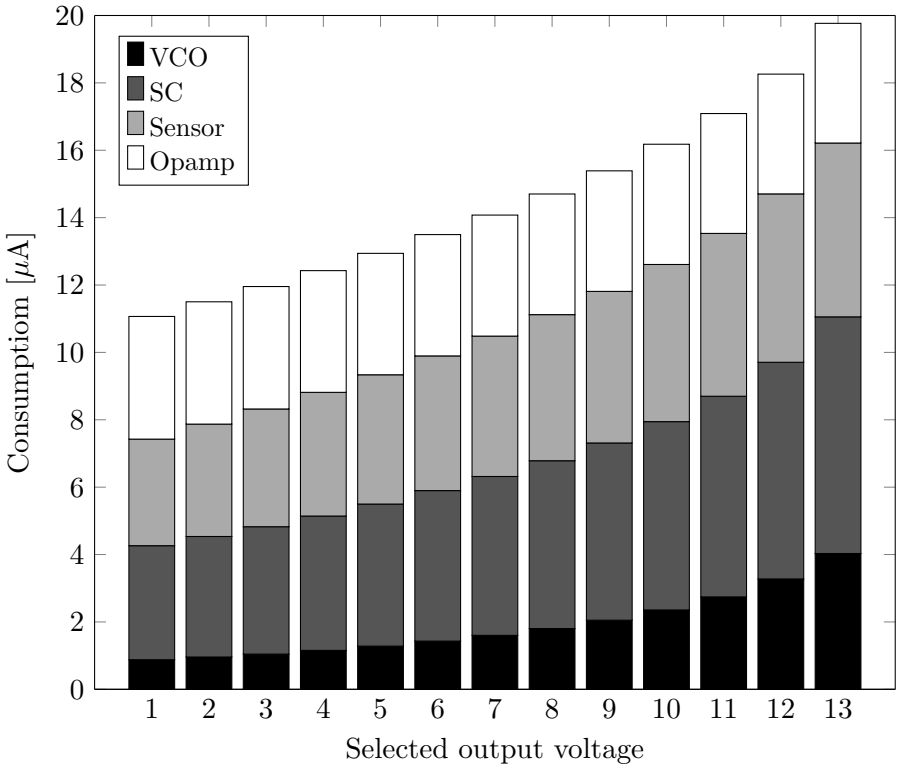


Figure 6.32: Current consumption of blocks depending on the selected negative output voltage

CHAPTER 7

Conclusion

The power supply scheme of complex digital SoCs is facing a wall. Implementation of DVFS scheme to increase the efficiency of the digital payload implies multiple power domains which cannot be addressed from outside the package. The increase in the number of IOs and the footprint of the external voltage regulators become prohibitive. The change of paradigm is to embed the power supply within a digital block where all resources operate at the same instantaneous voltage.
The challenge is then to embed a local and dedicated voltage regulator at no silicon penalty but mandatory performances to accommodate DVFS. The switched-capacitor DC-DC converter is by now the best candidate from integration and cost point of view. Better figure of power density may be achieved with inductive DC-DC converters but this calls for a very complex back-end technology. The choice here is to demonstrate the capability of a SC converter integration within the design flow of the digital block. The main stream idea is to stack the necessary capacitors on top of the digital gates. The active power switches must fit into a peripheral area to the digital gates where a standard approach consists to place the actuators of the power gating scheme.
From practical point of view, the job comprises the definition of a suitable SC elementary cell. A methodology must be selected to support the analyses necessary for the closed-loop design. Finally a practical demonstrator must be designed and the selected technology is CMOS FDSOI 28nm.

Chapter 2 has established the bottle neck of power supplying SoCs. Obviously the SC converter receives a lot of attention and a landscape describes the distribution of main literature results between efficiency and power density. There is a limit

in power density that cannot be overcome without a proper capacitor technology but with a huge cost penalty. This explains the difference between literature results based on trench capacitors and MIM capacitors. The former capacitors offer better results but the latter ones open many possibilities to low cost devices. This cost constraint explains the choice of MIM capacitors. As a consequence the maximum efficiency will be in the range of 75% to 80% for a successful design.

Chapter 3 summarizes the fundamentals of SC converters. Unlike most literature the sampled-data modeling is considered first to established a simulation model. Second a linearized small-signal model is systematically derived to represent the SC converter dynamics. The interests of the method are discussed. The models compare in a satisfying manner to the ones obtained from now well-known approaches. However sampled-data modeling offers more insights in the SC converter behavior in particular with respect to closed-loop control.

Chapter 4 details the closed-loop control of SC converter with frequency modulation. This scheme is compatible with a multiphase structure but this issue is not fully discussed. Various approaches of control are explored to establish the pros and cons of each methods for a final choice. Sampled-data modeling is extensively used as a uniform and systematic approach.

Chapter 5 is dedicated to the design of a SC converter power stage in CMOS 28nm FDSOI. The architecture is compatible with a digital design flow in the technology. Experimental results confirm the satisfying operation of the power stage and a good figure of efficiency. Then the implementation of a multiphase SC converter with a linear frequency-modulation voltage-loop control is covered. Experimental results confirm the theoretical statements and established satisfying transient behaviors.

Chapter 6 presents a side work to the PhD mainstream. The application of a dedicated SC converter to the body-biasing function is successfully demonstrated. Results are satisfying and highly promising for a low power implementation of the body-biasing function on a large scale implementation. Sampled-data modeling was used again to support the design.

As a conclusion the above-mentioned contributions validate the proposal of an original structure of SC converter compatible with a digital block design. The electrical performances are in line with the best-in-class results using MIM capacitors. An

underlying contribution is related to the successful application of sampled-data modeling to the case of the SC converters. A pertinent contribution is then established in CMOS 28nm FDSOI with respect to local power supply of large digital SoCs. The PhD results are scalable with silicon technology and capacitor technology.
Unfortunately the duration of the PhD work has let several issues unattended. The SC converter offers a multi-ratio cell that must be adequately selected depending on the instantaneous voltage reference and load current. A dynamic selector (gear box) is needed. From theoretical point of view, sampled-data modeling is useful to study the stability of a closed-loop system subject to bifurcation and chaos as the SC converter. It is important to be able to confront instable conditions to experimental confirmations what means to fabricate voluntarily badly designed converters.

Short-term perspectives :

- A more complete measurement campaign will cover a temperature dependency evaluation of the silicon test-chip.
- The gearbox concept must be applied with full respect of the digital design flow.

Long-term perspectives :

- The graal of this work is to verify the effectiveness of the multiphase SC converter to supply a genuine digital block. The digital block should be augmented to provide inputs to the DVFS scheme which is related to the gearbox. The measurement of the digital performances will ultimately confirm the proposal with respect to the new paradigm of power supply.

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APPENDIX A

HySim

HySim is a CAD tool developed by STMicroelectronics. Architectural simulation of switched structures through traditional spice simulator is not easy. Behavioral languages with mixed signal extension such as VHDL-AMS or Verliog-AMS are usually used to achieve fast and accurate modeling. Some behavioral tools like *Matlab/Simulink* or *Scilab* are sometimes preferred for architecture description. Hybrid simulations are available in such tools but the model descriptions based on state-space representation is still hard to derive. Manual derivation is also painful and is affected by many errors. HySim is a tool that provides a fully integrated simulation environment for switched systems accessible to electrical design community.
HySim is composed of several parts as described in Fig. A.1. The user starts with the schematic entry using HySim ideal switches and passive components in the Cadence environment. The HySim switches describe the switch closed state either by a short circuit or by a resistance. Likewise the open-state of the switches is described either by an open-circuit or by a resistance. The switches are used to determine all the possible circuit configurations. For example an inductive DC-DC converter under continuous conduction mode is described with two configurations while a discontinuous conduction mode exhibits three configurations. Then HySim generates a separate schematic for all the configurations and a graph view of the equivalent hybrid automaton. The user specifies the design parameters, the output vector of the state-space representation and other environment variables. Finally HySim creates symbolic netlist and transfer them to *Mapple* which creates the symbolic state-space matrices for all the configurations. A PWL model and an averaged model is also generated in Verilog-A. This model can be used for simulation purpose in Cadence environment. The user moves now to the *Matlab/Simulink* environment. The parameters of the models are loaded and the user can construct a *Simulink* schematic

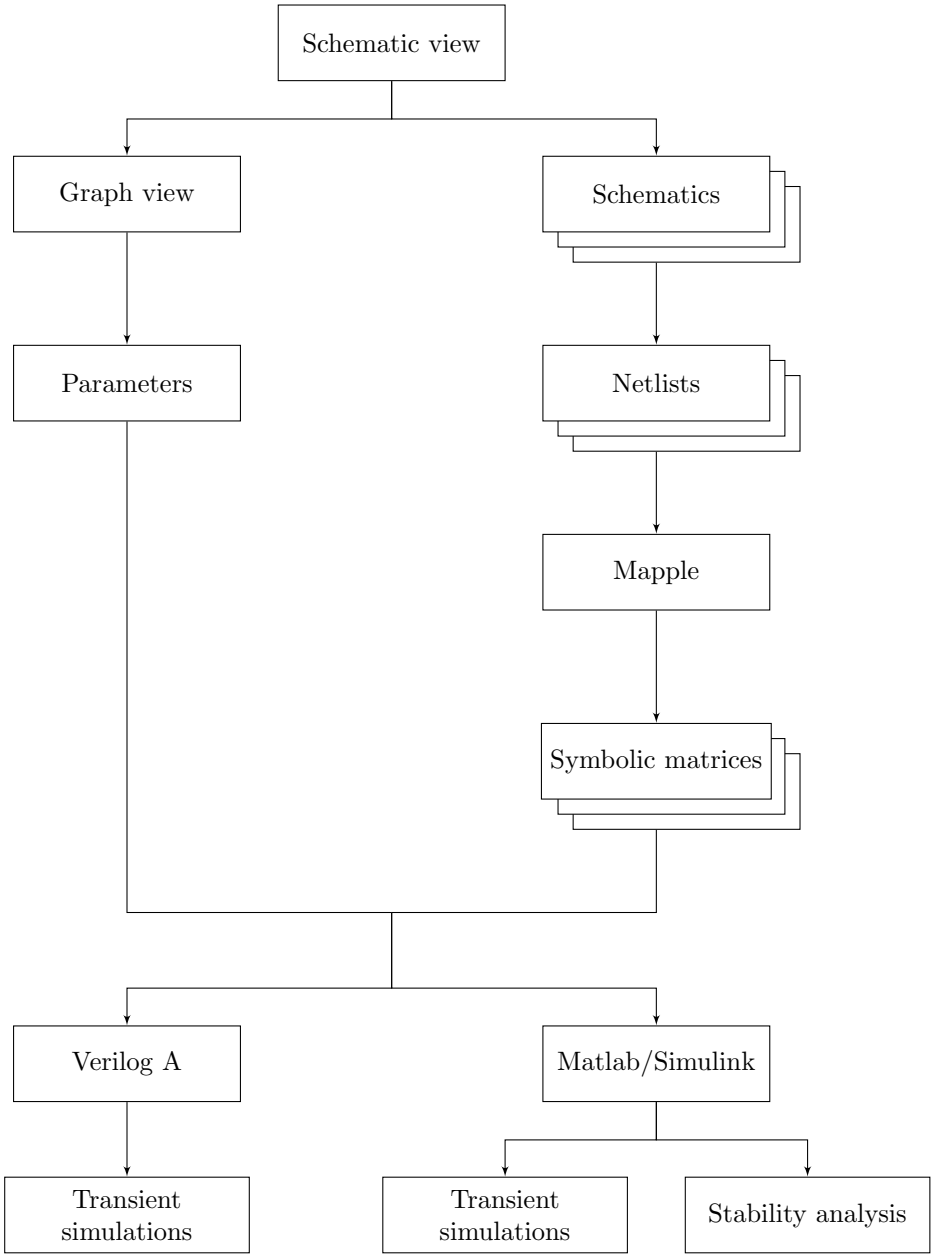


Figure A.1: HySim flow

thanks to a dedicated library. The user can also use the system description to perform stability analysis or control synthesis with *Matlab/Simulink* toolboxes.

APPENDIX B

State space model

B.1 Model of a 2:1 SC converter with off-state resistance

$$A_1 = \begin{bmatrix} -\dfrac{R_{off}+R_{on}}{2\,R_{off}\,\tau_1} & -\dfrac{R_{off}-R_{on}}{2\,R_{off}\,\tau_1} \\ -\dfrac{R_{off}-R_{on}}{2\,R_{off}\,\tau_2} & -\dfrac{R_{off}+R_{on}}{2\,R_{off}\,\tau_2} \end{bmatrix},\ A_2 = \begin{bmatrix} -\dfrac{R_{off}+R_{on}}{2\,R_{off}\,\tau_1} & \dfrac{R_{off}-R_{on}}{2\,R_{off}\,\tau_1} \\ \dfrac{R_{off}-R_{on}}{2\,R_{off}\,\tau_2} & -\dfrac{R_{off}+R_{on}}{2\,R_{off}\,\tau_2} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 0 & \dfrac{1}{2\,\tau_1} \\ \dfrac{-1}{C_{load}} & \dfrac{1}{2\,\tau_2} \end{bmatrix},\ B_2 = \begin{bmatrix} 0 & \dfrac{R_{on}}{2\,R_{off}\,\tau_1} \\ \dfrac{-1}{C_{load}} & \dfrac{R_{on}}{2\,R_{off}\,\tau_2} \end{bmatrix}$$

$$C_1 = \begin{bmatrix} -\dfrac{R_{off}+R_{on}}{2\,R_{on}\,R_{off}} & -\dfrac{R_{off}+R_{on}}{2\,R_{on}\,R_{off}} \\ 0 & 1 \end{bmatrix},\ C_2 = \begin{bmatrix} -\dfrac{R_{off}+R_{on}}{2\,R_{on}\,R_{off}} & \dfrac{R_{off}-R_{on}}{2\,R_{on}\,R_{off}} \\ 0 & 1 \end{bmatrix}$$

$$D_1 = \begin{bmatrix} 0 & \dfrac{1}{2\,R_{on}} \\ 0 & 0 \end{bmatrix},\ D_2 = \begin{bmatrix} 0 & \dfrac{1}{2\,R_{off}} \\ 0 & 0 \end{bmatrix}$$

$$U = \begin{bmatrix} I_{load} \\ V_{in} \end{bmatrix},\ x = \begin{bmatrix} v_{C_{fly}} \\ v_{C_{load}} \end{bmatrix}$$

With $\tau_1 = R_{on}\,C_{fly}$ and $\tau_2 = R_{on}\,C_{load}$.

B.2 Model of a negative SC converter

$$A_1 = \begin{bmatrix} -\frac{1}{2\,\tau_1} & 0 \\ 0 & -\frac{1}{C_{load}} \end{bmatrix},\ A_2 = \begin{bmatrix} -\frac{1}{2\,\tau_1} & -\frac{1}{2\,\tau_1} \\ -\frac{1}{2\,\tau_2} & -\frac{1}{\tau_2} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 0 & \frac{1}{2\,\tau_1} \\ \frac{1}{C_{load}} & \frac{1}{2\,\tau_2} \end{bmatrix},\ B_2 = \begin{bmatrix} 0 & 0 \\ \frac{1}{C_{load}} & \frac{1}{2\,\tau_2} \end{bmatrix}$$

$$C_1 = \begin{bmatrix} 0 & 1 \end{bmatrix},\ C_2 = \begin{bmatrix} 0 & 1 \end{bmatrix}$$

$$D_1 = \begin{bmatrix} 0 & 0 \end{bmatrix},\ D_2 = \begin{bmatrix} 0 & 0 \end{bmatrix}$$

$$U = \begin{bmatrix} I_{load} \\ V_{in} \end{bmatrix},\ x = \begin{bmatrix} v_{C_{fly}} \\ v_{C_{load}} \end{bmatrix}$$

With $\tau_1 = R_{on}\,C_{fly}$ and $\tau_2 = R_{on}\,C_{load}$.

B.3 Model of a negative SC converter with bottom plate parasitic capacitance

$$A_1 = \begin{bmatrix} -\frac{1}{\tau_1} & 0 & -\frac{1}{\tau_1} \\ 0 & 0 & 0 \\ -\frac{1}{\tau_3} & 0 & -\frac{2}{\tau_3} \end{bmatrix},\ A_2 = \begin{bmatrix} -\frac{1}{\tau_1} & 0 & -\frac{1}{\tau_1} \\ 0 & -\frac{1}{\tau_2} & \frac{1}{\tau_2} \\ -\frac{1}{\tau_3} & 0 & -\frac{2}{\tau_3} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 0 & \frac{1}{\tau_1} \\ \frac{1}{C_{load}} & 0 \\ 0 & \frac{1}{\tau_3} \end{bmatrix},\ B_2 = \begin{bmatrix} 0 & 0 \\ \frac{1}{C_{load}} & 0 \\ 0 & 0 \end{bmatrix}$$

$$C_1 = \begin{bmatrix} 0 & 1 & 0 \end{bmatrix},\ C_2 = \begin{bmatrix} 0 & 1 & 0 \end{bmatrix}$$

$$D_1 = \begin{bmatrix} 0 & 0 \end{bmatrix},\ D_2 = \begin{bmatrix} 0 & 0 \end{bmatrix}$$

$$U = \begin{bmatrix} I_{load} \\ V_{in} \end{bmatrix},\ x = \begin{bmatrix} v_{C_{fly}} \\ v_{C_{load}} \\ v_{C_{bot}} \end{bmatrix}$$

With $\tau_1 = R_{on}\, C_{fly}$, $\tau_2 = R_{on}\, C_{load}$ and $\tau_3 = R_{on}\, C_{bot}$.

APPENDIX C

Extra measurement results

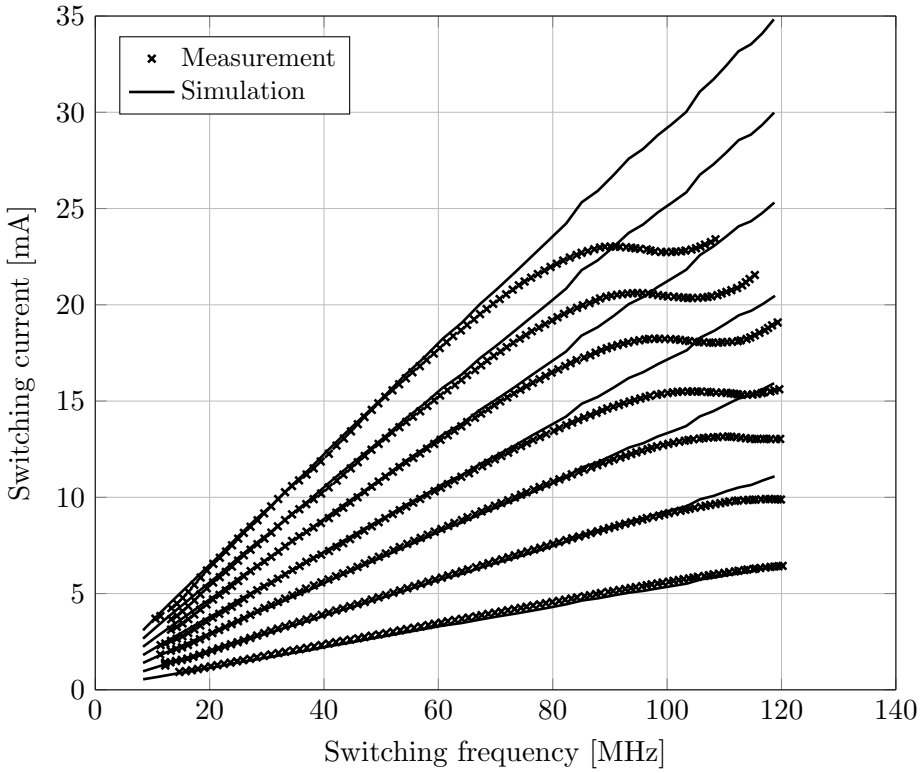


Figure C.1: Switching current of the driver as a function of the switching frequency for various size of switch: ratio 3:2

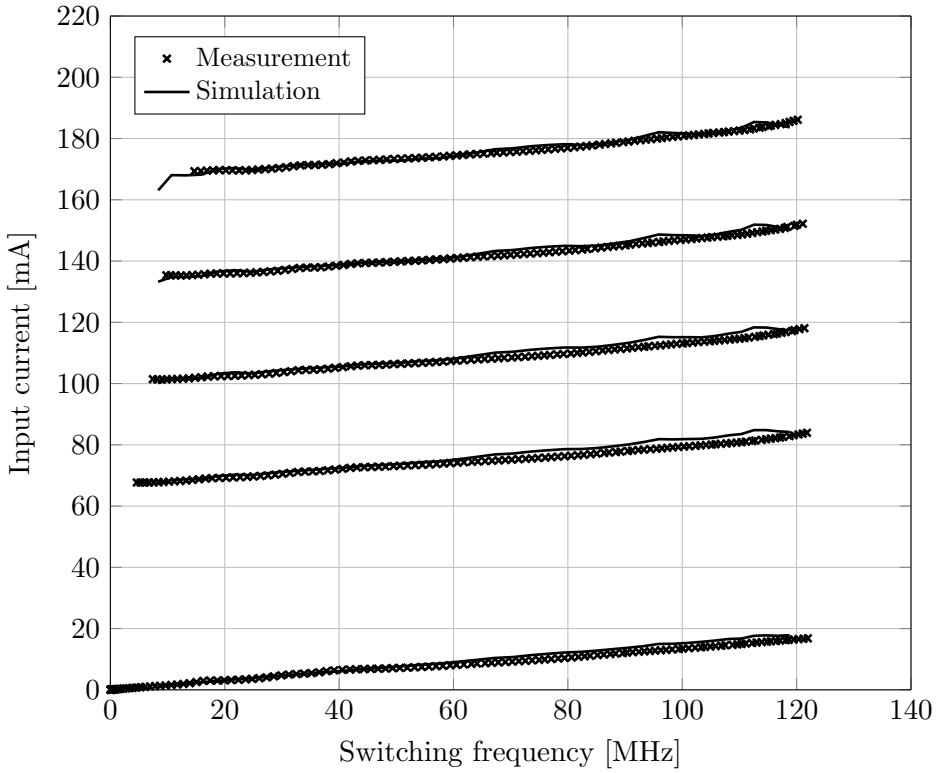


Figure C.2: Input current as a function of the switching frequency for various load current: ratio 3:2

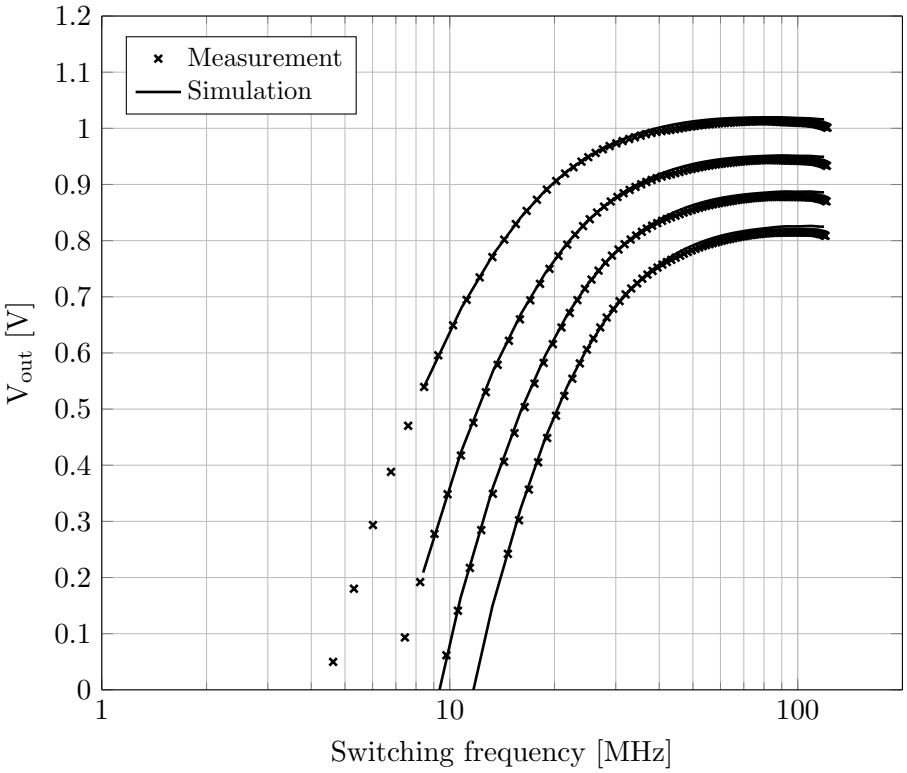


Figure C.3: Efficiency versus output voltage as a function of the switching frequency for various load current: ratio 3:2

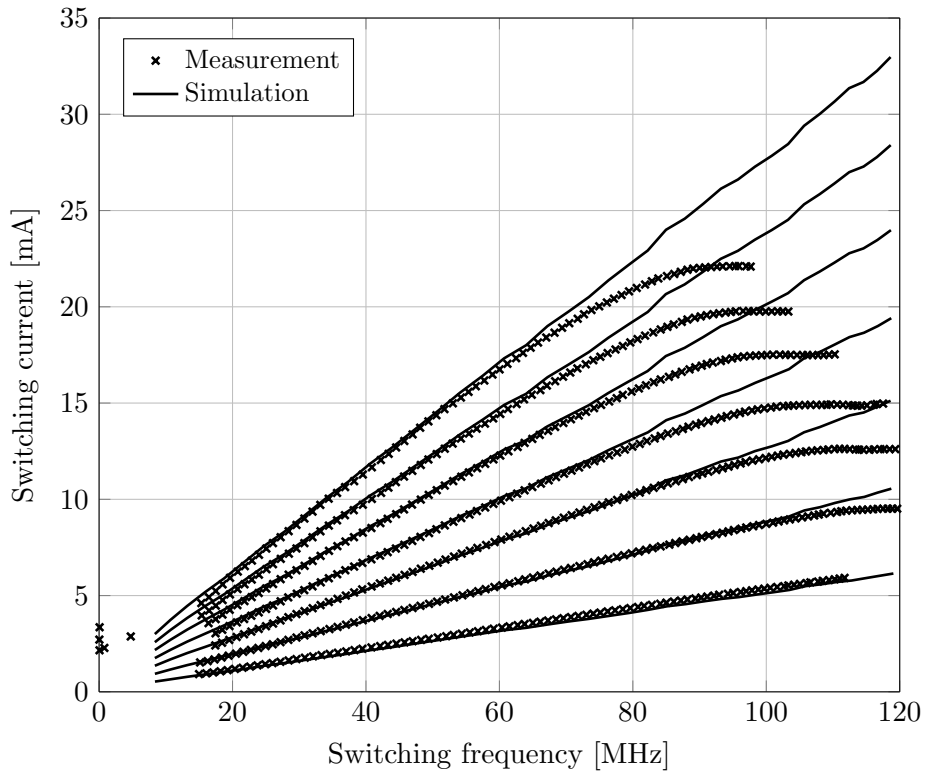


Figure C.4: Switching current of the driver as a function of the switching frequency for various size of switch: ratio 4:3

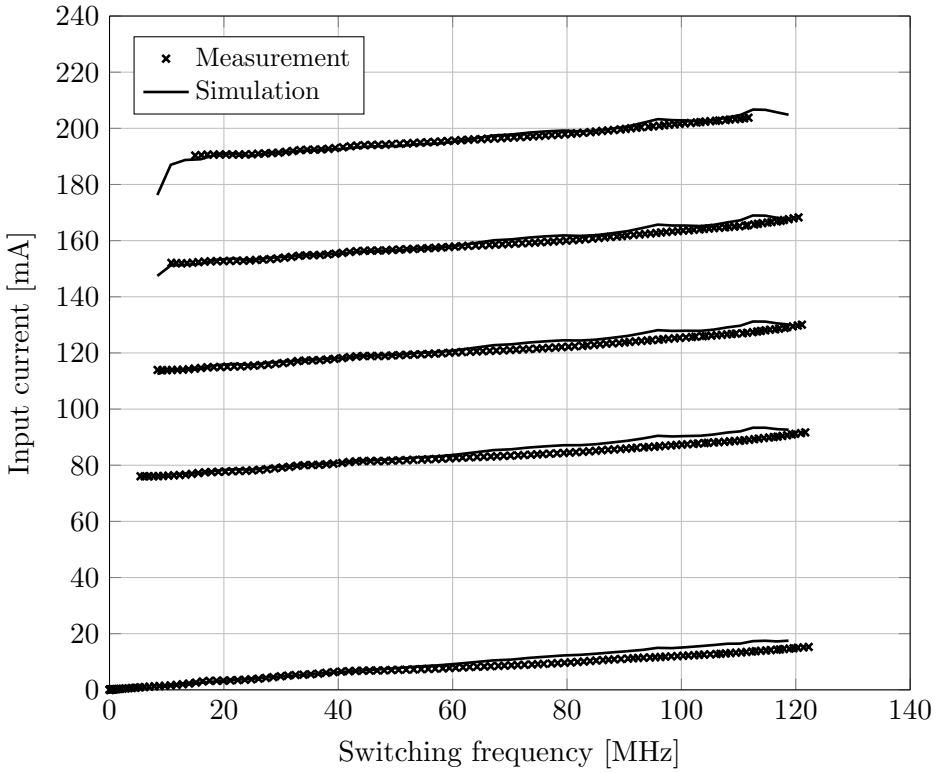


Figure C.5: Input current as a function of the switching frequency for various load current: ratio 4:3

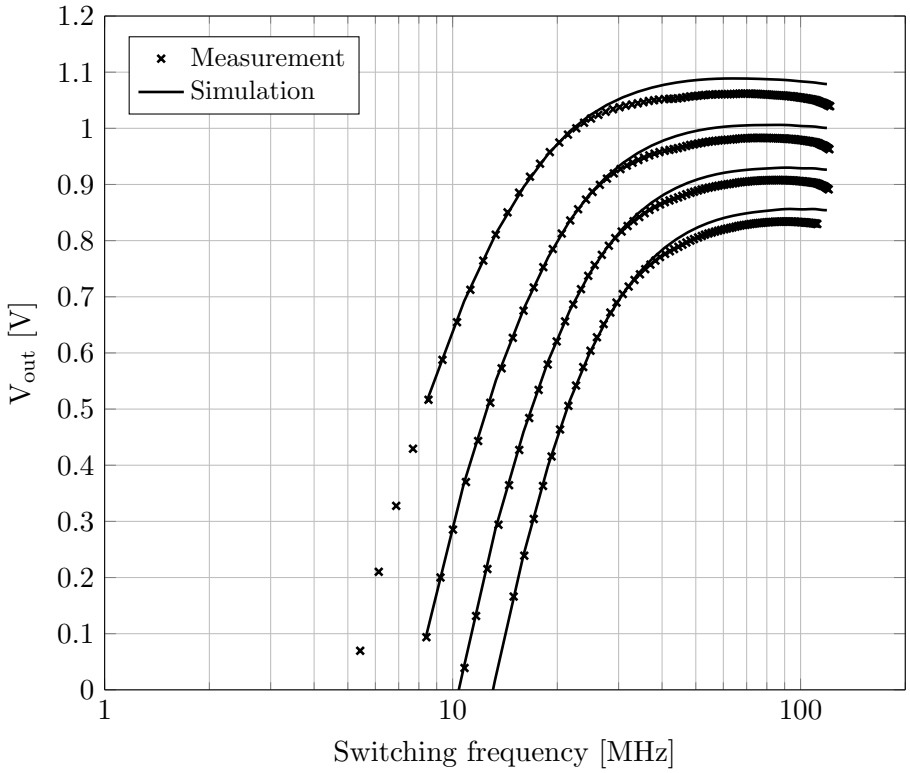


Figure C.6: Efficiency versus output voltage as a function of the switching frequency for various load current: ratio 4:3

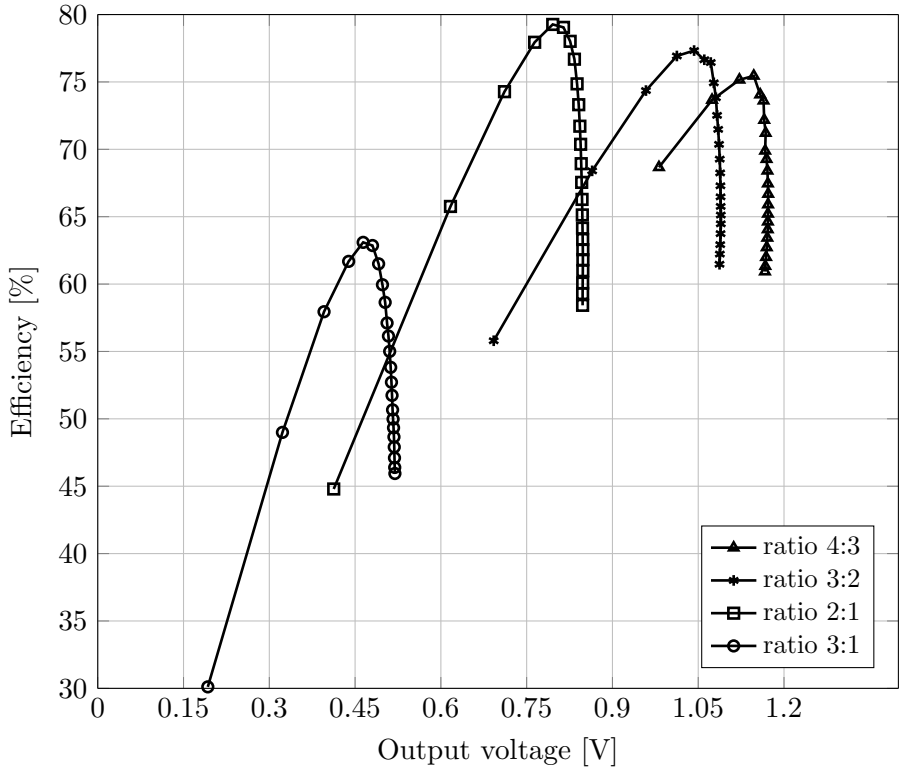


Figure C.7: Efficiency measurement of the second test-chip versus the output voltage at 50 mA load current in open-loop

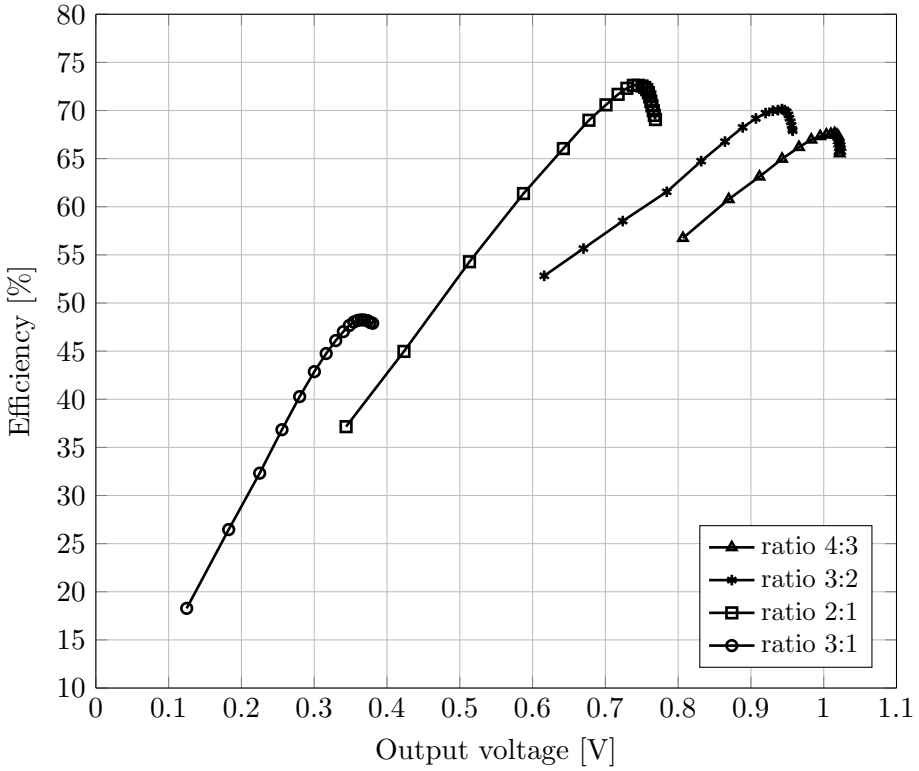
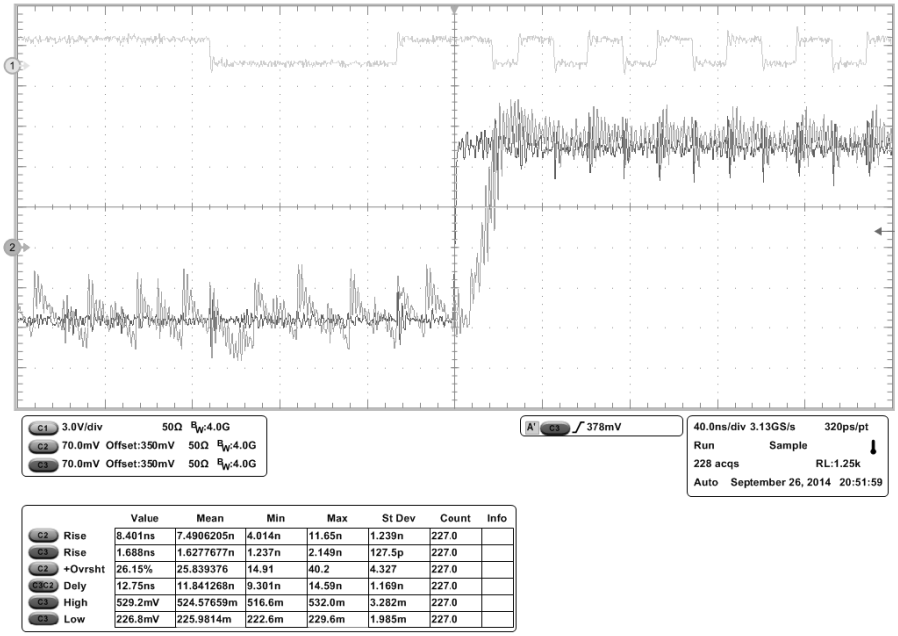
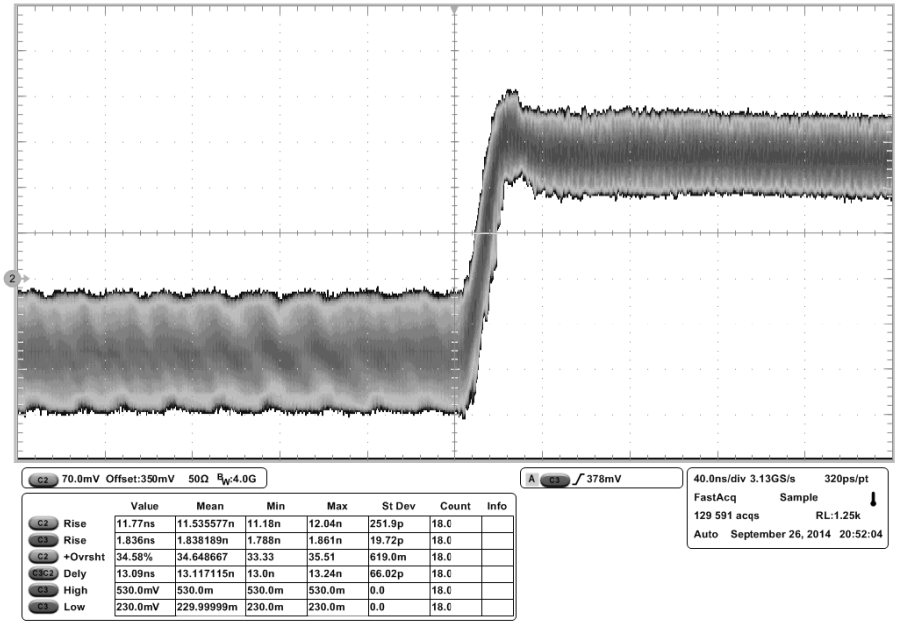


Figure C.8: Efficiency measurement of the second test-chip versus the output voltage at 250 mA load current in open-loop



	Value	Mean	Min	Max	St Dev	Count	Info
C2 Rise	8.401ns	7.4906205n	4.014n	11.65n	1.239n	227.0	
C3 Rise	1.688ns	1.6277677n	1.237n	2.149n	127.5p	227.0	
C2 +Ovrsht	26.15%	25.839376	14.91	40.2	4.327	227.0	
C3C2 Dely	12.75ns	11.841268n	9.301n	14.59n	1.169n	227.0	
C3 High	529.2mV	524.57659m	516.6m	532.0m	3.282m	227.0	
C3 Low	226.8mV	225.9814m	222.6m	229.6m	1.985m	227.0	

Figure C.9: Rising reference tracking for the 3:1 ratio from 0.2 V to 0.5 V at $I_{load} = 50\ mA$, output clock (top), output voltage and reference voltage (middle)



	Value	Mean	Min	Max	St Dev	Count	Info
C2 Rise	11.77ns	11.535577n	11.18n	12.04n	251.9p	18.0	
C3 Rise	1.836ns	1.838189n	1.788n	1.861n	19.72p	18.0	
C2 +Ovrsht	34.58%	34.648667	33.33	35.51	619.0m	18.0	
C3C2 Dely	13.09ns	13.117115n	13.0n	13.24n	66.02p	18.0	
C3 High	530.0mV	530.0m	530.0m	530.0m	0.0	18.0	
C3 Low	230.0mV	229.99999m	230.0m	230.0m	0.0	18.0	

Figure C.10: Output voltage with persistence acquisition on rising reference tracking for the 3:1 ratio from 0.2 V to 0.5 V at $I_{load} = 50\ mA$

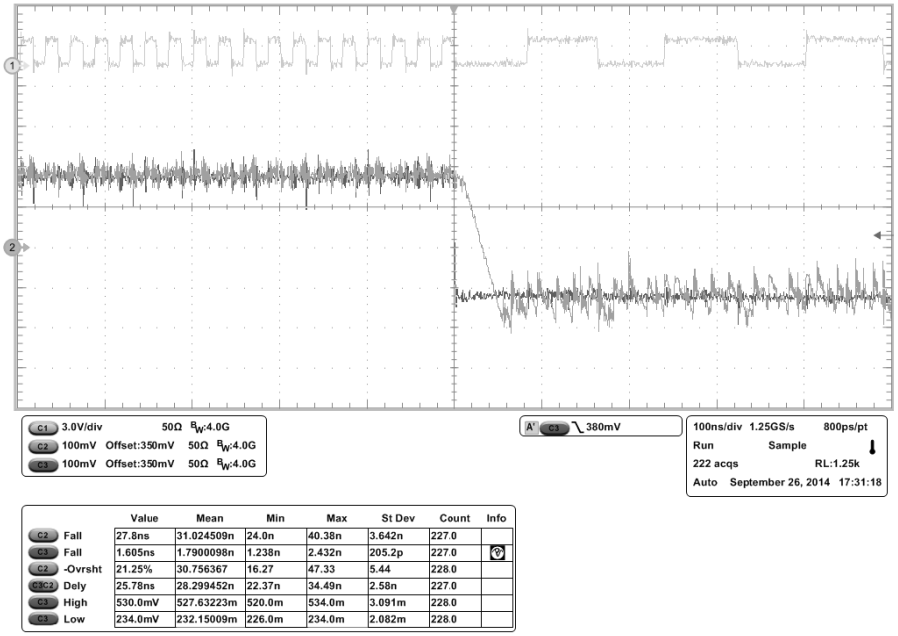


Figure C.11: Falling reference tracking for the 3:1 ratio from 0.5 V to 0.2 V at $I_{load} = 50\ mA$, output clock (top), output voltage and reference voltage (middle)

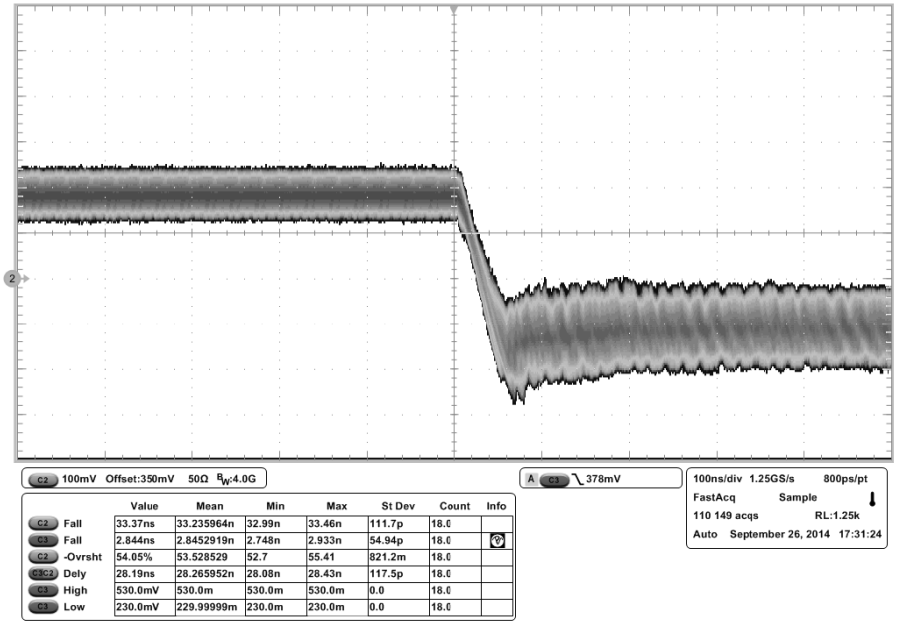
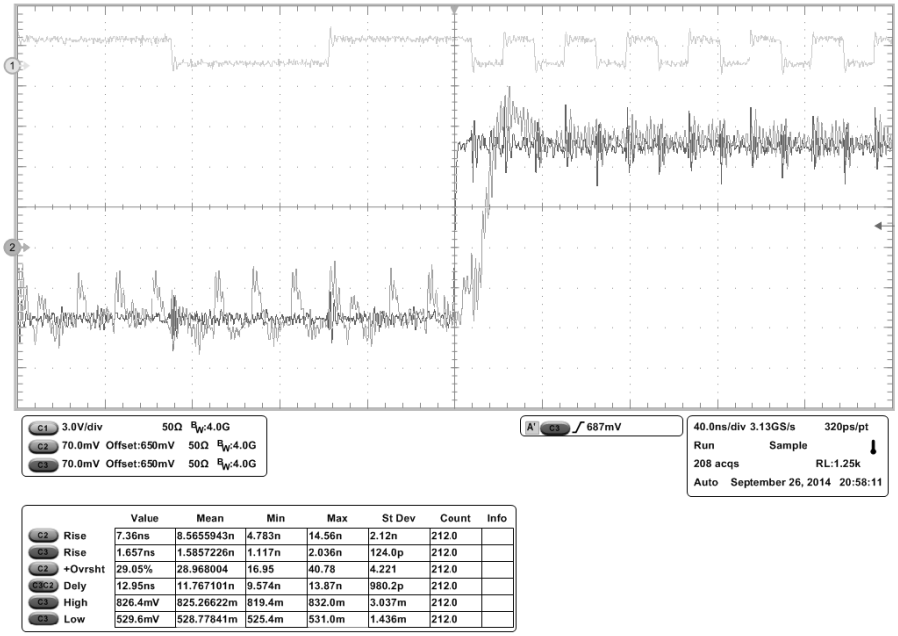
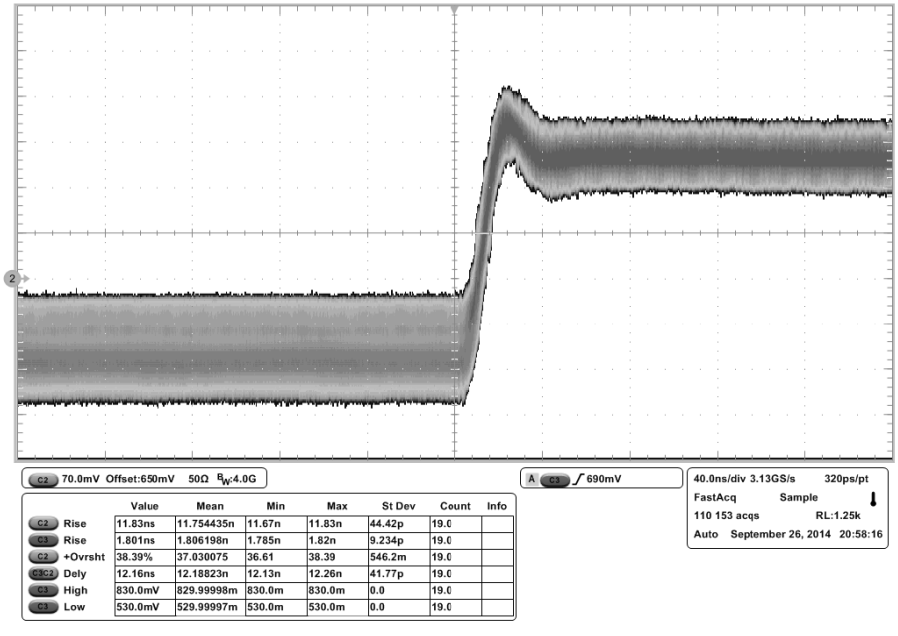


Figure C.12: Output voltage with persistence acquisition on falling reference tracking for the 3:1 ratio from 0.5 V to 0.2 V at $I_{load} = 50\ mA$



	Value	Mean	Min	Max	St Dev	Count	Info
C2 Rise	7.36ns	8.5655943n	4.783n	14.56n	2.12n	212.0	
C3 Rise	1.657ns	1.5857226n	1.117n	2.036n	124.0p	212.0	
C2 +Ovrsht	29.05%	28.968004	16.95	40.78	4.221	212.0	
C3C2 Dely	12.95ns	11.767101n	9.574n	13.87n	980.2p	212.0	
C3 High	826.4mV	825.26622m	819.4m	832.0m	3.037m	212.0	
C3 Low	529.6mV	528.77841m	525.4m	531.0m	1.436m	212.0	

Figure C.13: Rising reference tracking for the 2:1 ratio from 0.5 V to 0.8 V at $I_{load} = 100\ mA$, output clock (top), output voltage and reference voltage (middle)



	Value	Mean	Min	Max	St Dev	Count	Info
C2 Rise	11.83ns	11.754435n	11.67n	11.83n	44.42p	19.0	
C3 Rise	1.801ns	1.806198n	1.785n	1.82n	9.234p	19.0	
C2 +Ovrsht	38.39%	37.030075	36.61	38.39	546.2m	19.0	
C3C2 Dely	12.16ns	12.18823n	12.13n	12.26n	41.77p	19.0	
C3 High	830.0mV	829.99998m	830.0m	830.0m	0.0	19.0	
C3 Low	530.0mV	529.99997m	530.0m	530.0m	0.0	19.0	

Figure C.14: Output voltage with persistence acquisition on rising reference tracking for the 2:1 ratio from 0.5 V to 0.8 V at $I_{load} = 100\ mA$

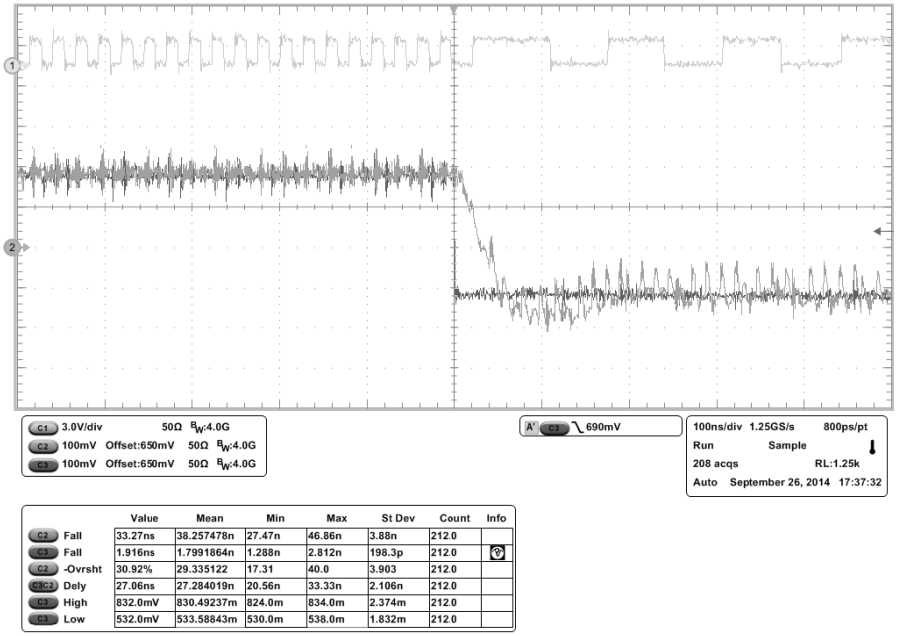


Figure C.15: Falling reference tracking for the 2:1 ratio from 0.8 V to 0.5 V at $I_{load} = 100\ mA$, output clock (top), output voltage and reference voltage (middle)

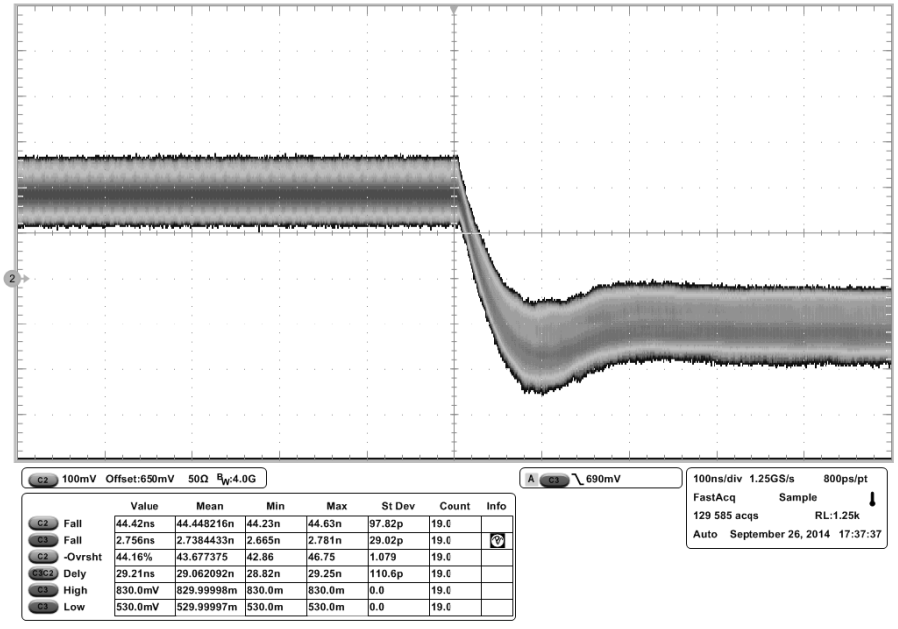
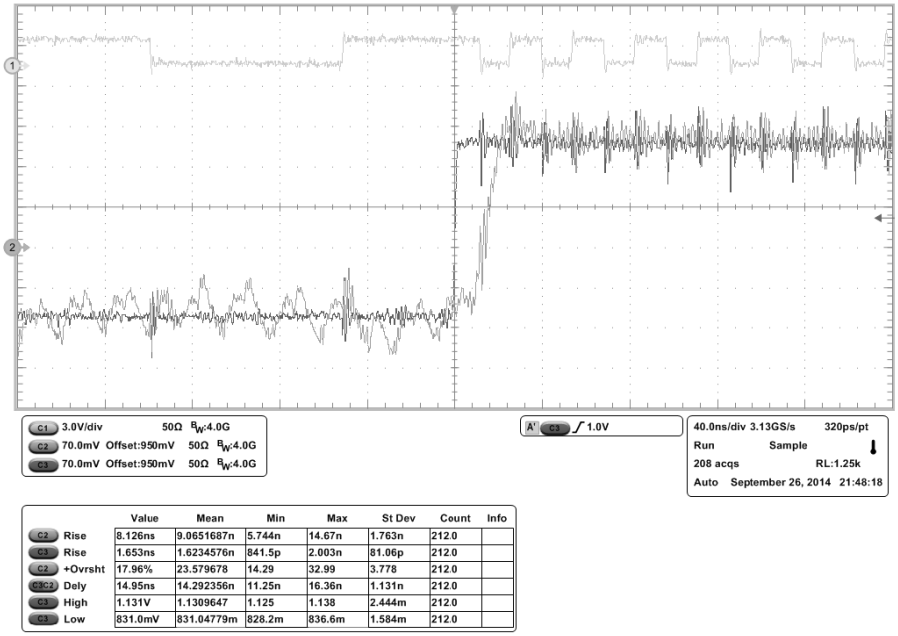
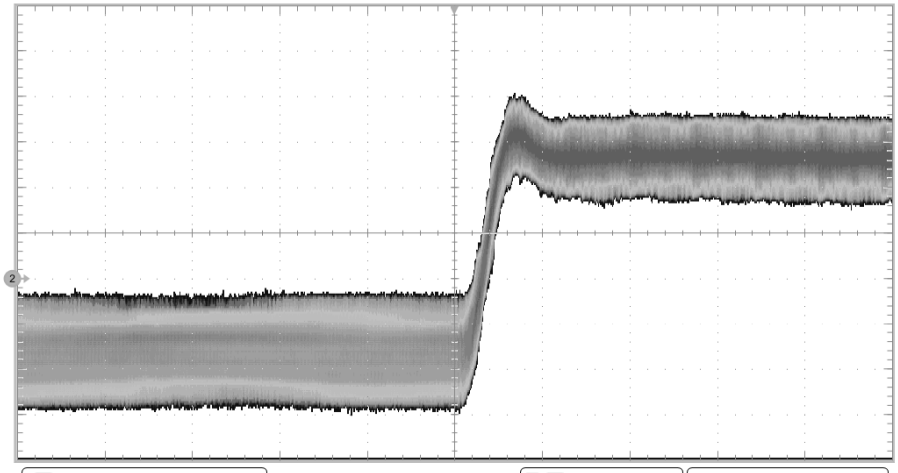


Figure C.16: Output voltage with persistence acquisition on falling reference tracking for the 2:1 ratio from 0.8 V to 0.5 V at $I_{load} = 100\ mA$



	Value	Mean	Min	Max	St Dev	Count	Info
C2 Rise	8.126ns	9.0651687n	5.744n	14.67n	1.763n	212.0	
C3 Rise	1.653ns	1.6234576n	841.5p	2.003n	81.06p	212.0	
C2 +Ovrsht	17.96%	23.579678	14.29	32.99	3.778	212.0	
C3C2 Dely	14.95ns	14.292356n	11.25n	16.36n	1.131n	212.0	
C3 High	1.131V	1.1309647	1.125	1.138	2.444m	212.0	
C3 Low	831.0mV	831.04779m	828.2m	836.6m	1.584m	212.0	

Figure C.17: Rising reference tracking for the 3:2 ratio from 0.8 V to 1.1 V at $I_{load} = 50\ mA$, output clock (top), output voltage and reference voltage (middle)



	Value	Mean	Min	Max	St Dev	Count	Info
C2 Rise	10.73ns	10.733715n	10.68n	10.91n	58.86p	18.0	
C3 Rise	1.795ns	1.793194n	1.771n	1.801n	8.166p	18.0	
C2 +Ovrsht	34.0%	34.29593	33.66	35.0	523.0m	18.0	
C3C2 Dely	15.02ns	15.045687n	14.97n	15.11n	37.26p	18.0	
C3 High	1.13V	1.13	1.13	1.13	0.0	18.0	
C3 Low	830.0mV	829.99998m	830.0m	830.0m	0.0	18.0	

Figure C.18: Output voltage with persistence acquisition on rising reference tracking for the 3:2 ratio from 0.8 V to 1.1 V at $I_{load} = 50\ mA$

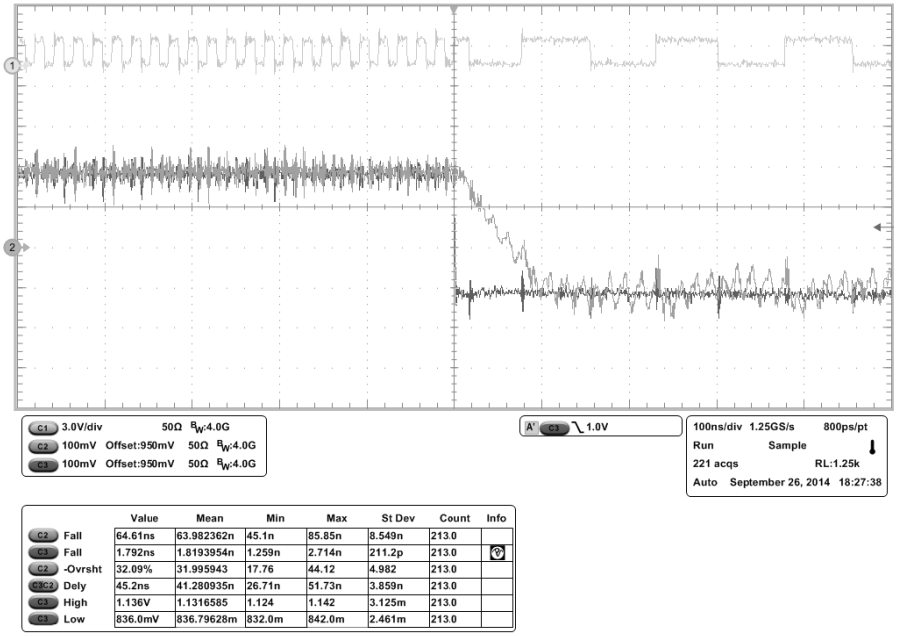


Figure C.19: Falling reference tracking for the 3:2 ratio from 1.1 V to 0.8 V at $I_{load} = 50\ mA$, output clock (top), output voltage and reference voltage (middle)

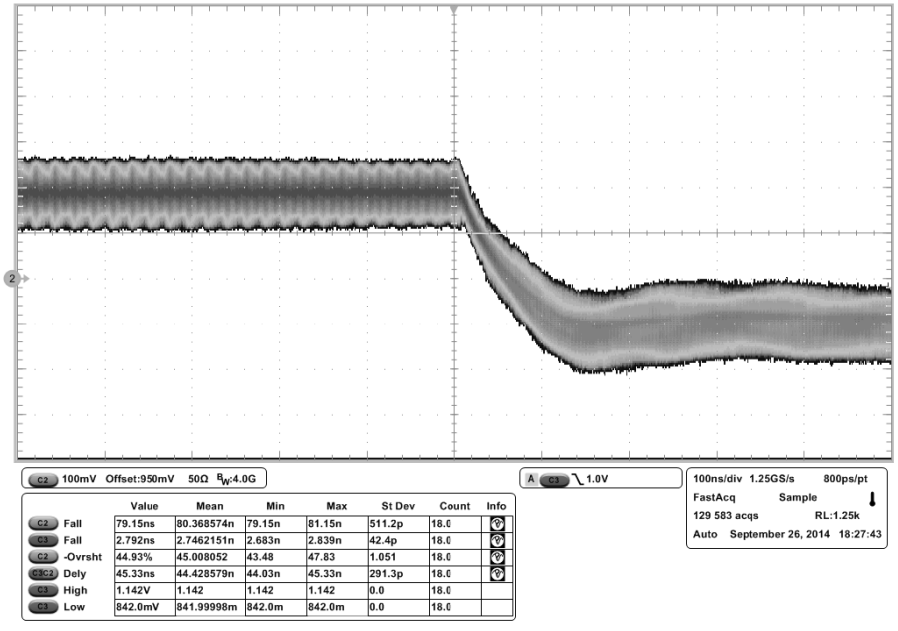


Figure C.20: Output voltage with persistence acquisition on falling reference tracking for the 3:2 ratio from 1.1 V to 0.8 V at $I_{load} = 50\ mA$

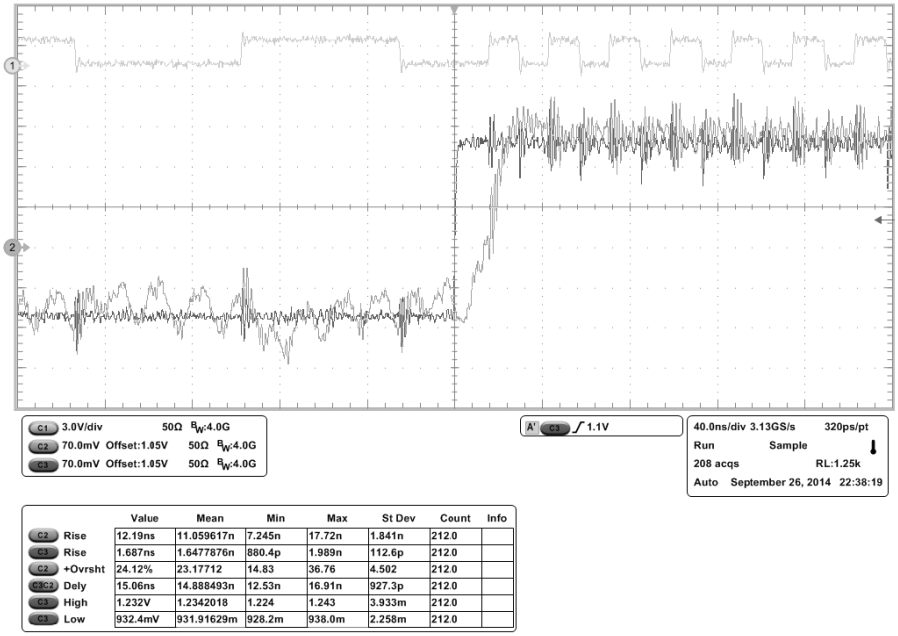


Figure C.21: Rising reference tracking for the 4:3 ratio from 0.9 V to 1.2 V at $I_{load} = 50\ mA$, output clock (top), output voltage and reference voltage (middle)

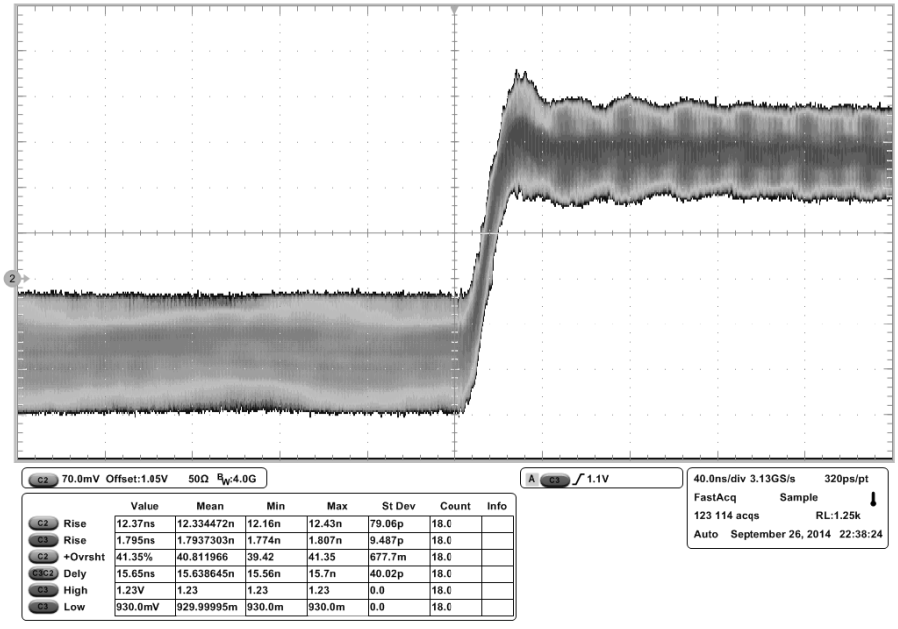


Figure C.22: Output voltage with persistence acquisition on rising reference tracking for the 4:3 ratio from 0.9 V to 1.2 V at $I_{load} = 50\ mA$

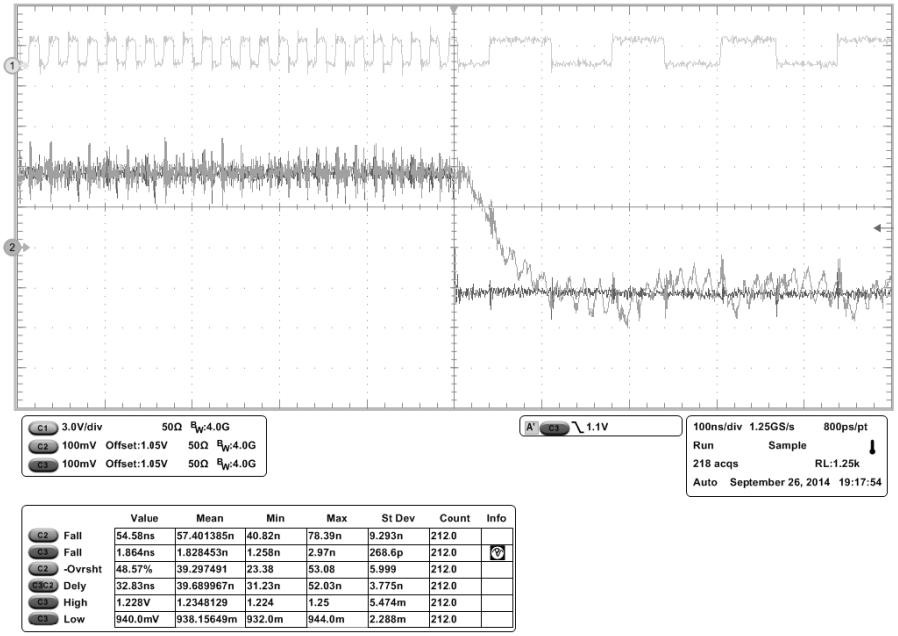


Figure C.23: Falling reference tracking for the 4:3 ratio from 1.2 V to 0.9 V at $I_{load} = 50\ mA$, output clock (top), output voltage and reference voltage (middle)

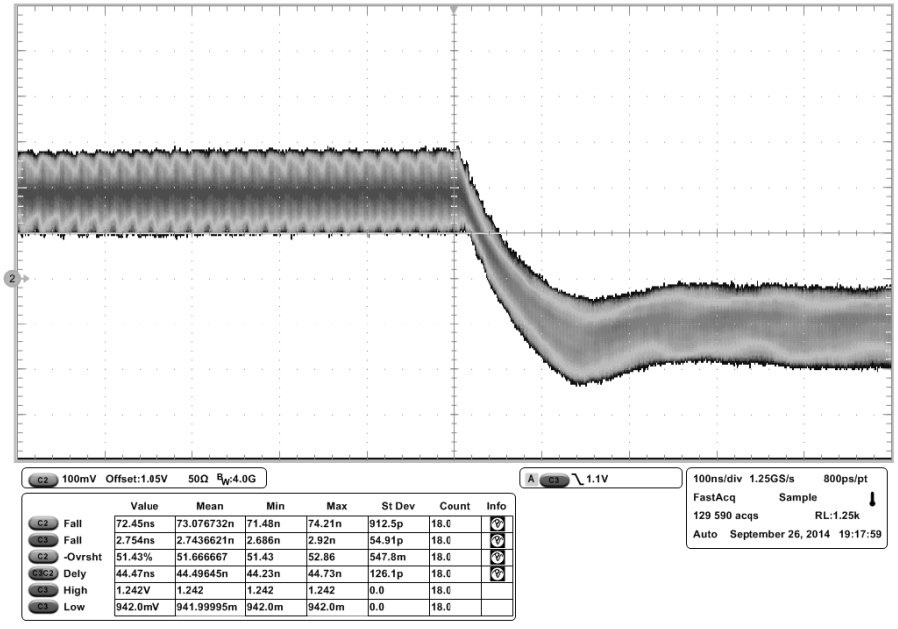


Figure C.24: Output voltage with persistence acquisition on falling reference tracking for the 4:3 ratio from 1.2 V to 0.9 V at $I_{load} = 50\ mA$

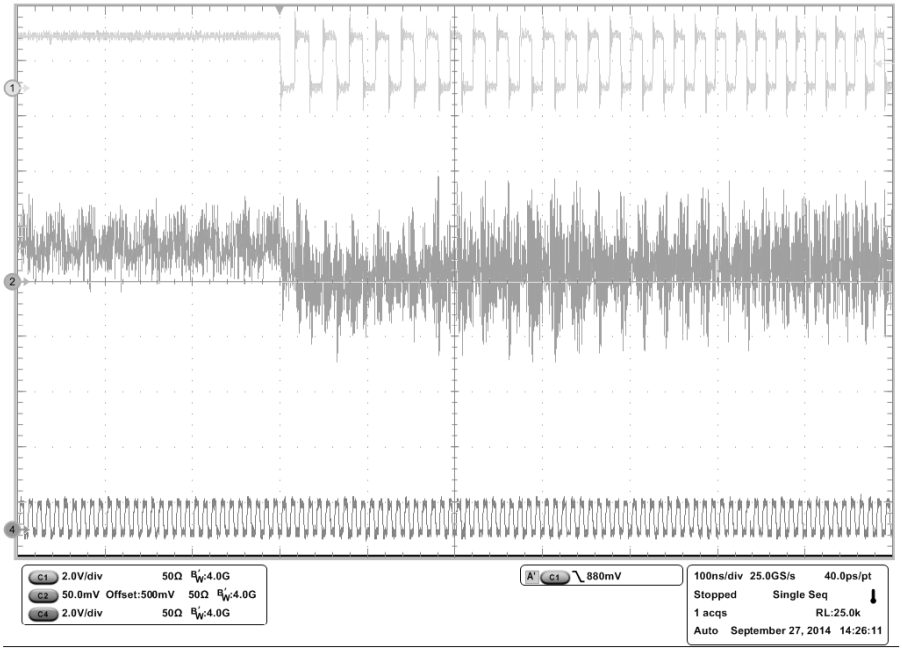


Figure C.25: Negative load transient for the 3:1 ratio from 60 mA to 120 mA at $V_{ref} = 500\ mV$, output clock (top), output voltage (middle) and digital clock (bottom)

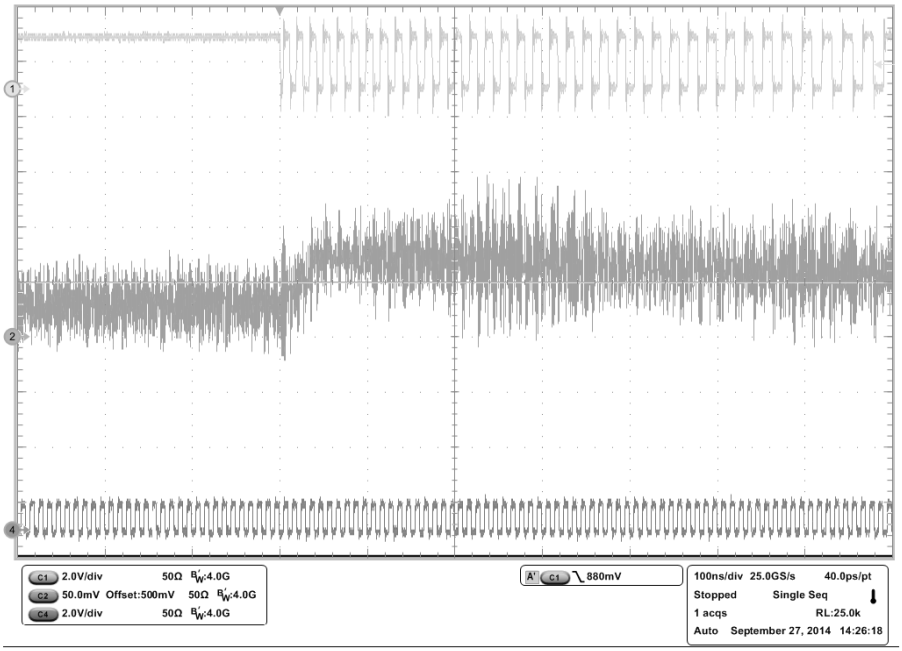


Figure C.26: Positive load transient for the 3:1 ratio from 120 mA to 60 mA at $V_{ref} = 500\ mV$, output clock (top), output voltage (middle) and digital clock (bottom)

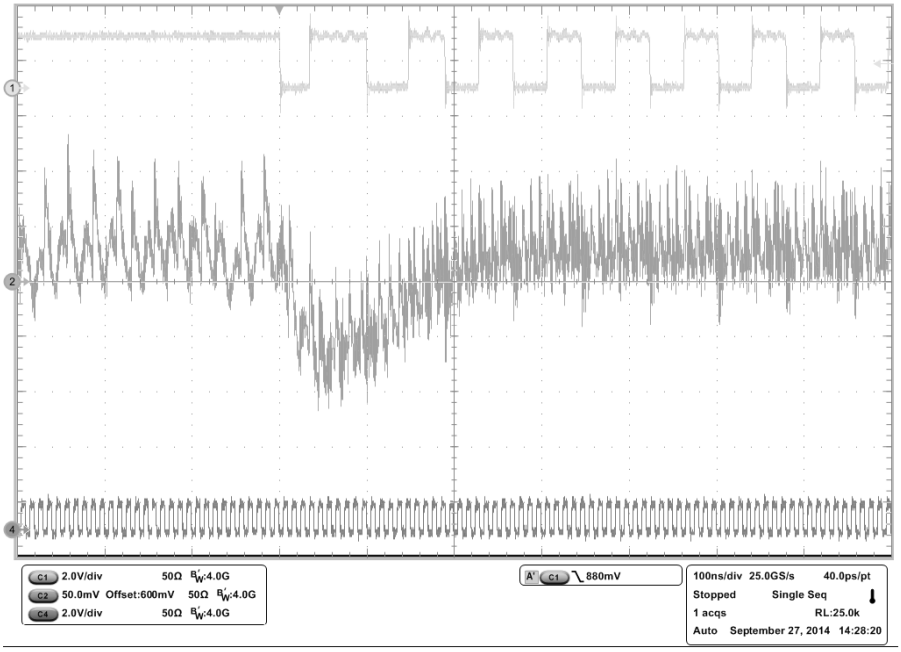


Figure C.27: Negative load transient for the 2:1 ratio from 50 mA to 120 mA at $V_{ref} = 600\ mV$, output clock (top), output voltage (middle) and digital clock (bottom)

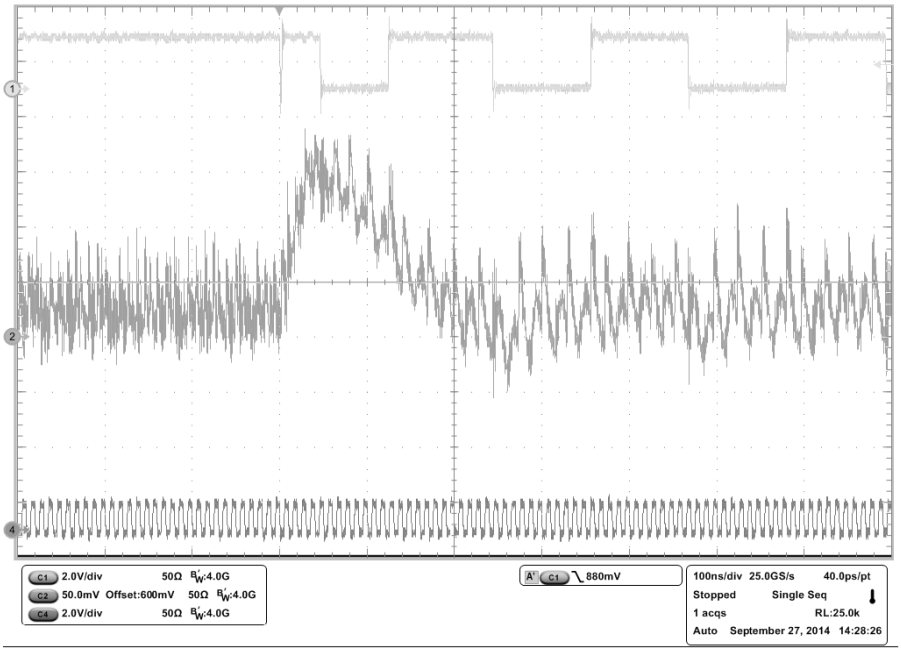


Figure C.28: Positive load transient for the 2:1 ratio from 120 mA to 50 mA at $V_{ref} = 600\ mV$, output clock (top), output voltage (middle) and digital clock (bottom)

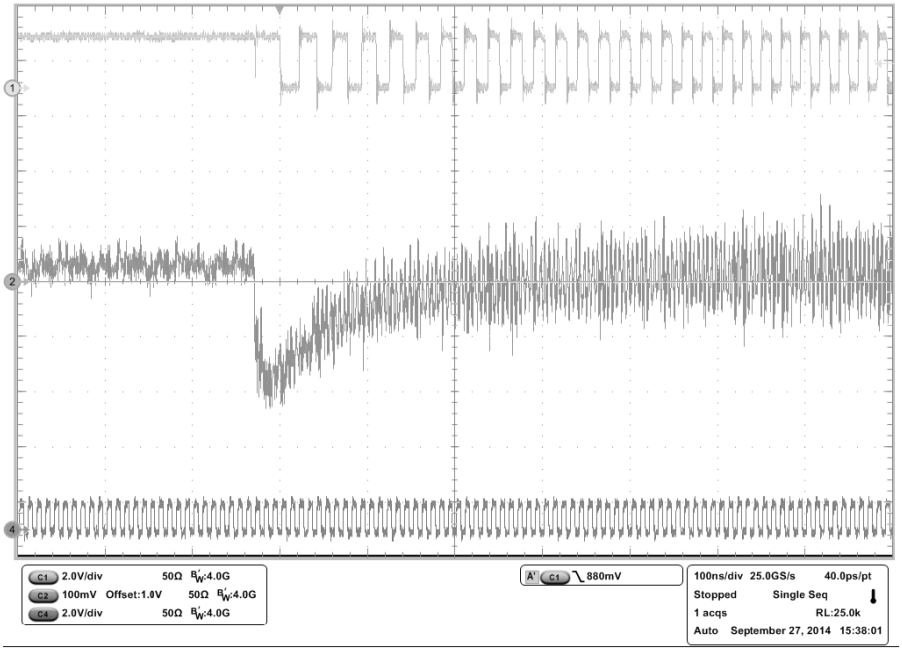


Figure C.29: Negative load transient for the 3:2 ratio from 50 mA to 177 mA at $V_{ref} = 1\,V$, output clock (top), output voltage (middle) and digital clock (bottom)

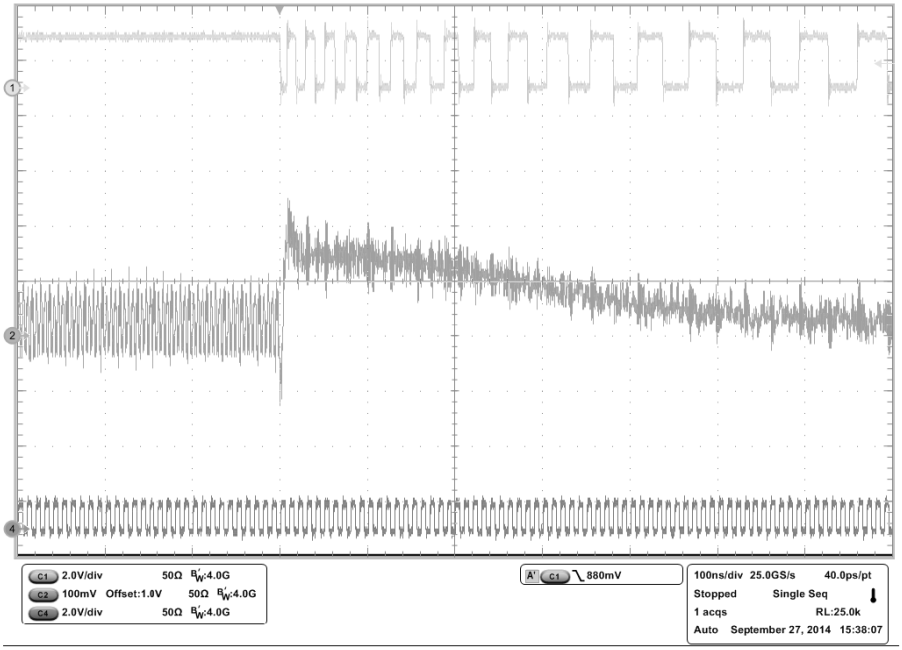


Figure C.30: Positive load transient for the 3:2 ratio from 177 mA to 50 mA at $V_{ref} = 1\,V$, output clock (top), output voltage (middle) and digital clock (bottom)

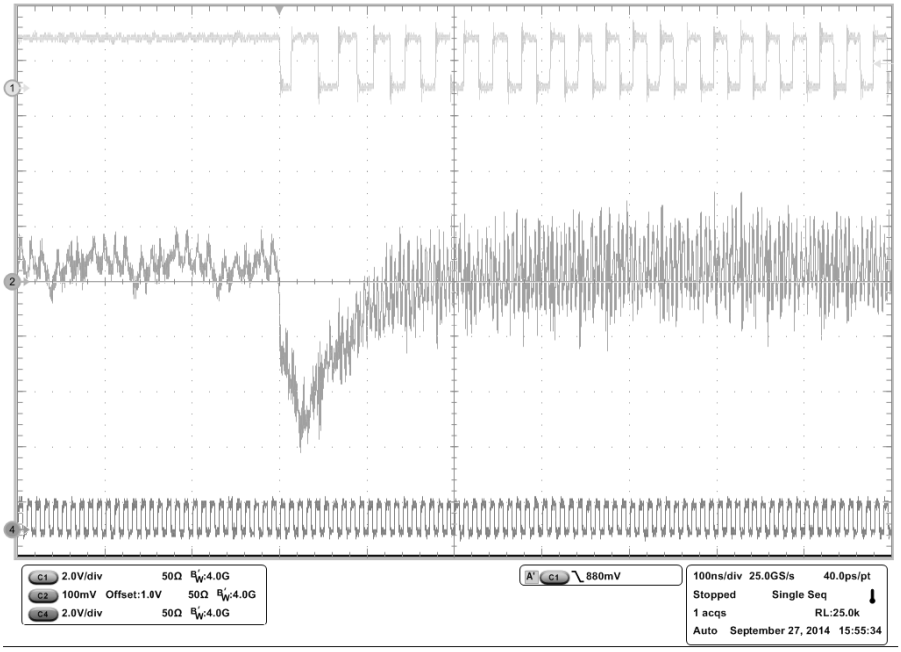


Figure C.31: Negative load transient for the 4:3 ratio from 52 mA to 172 mA at $V_{ref} = 1\ V$, output clock (top), output voltage (middle) and digital clock (bottom)

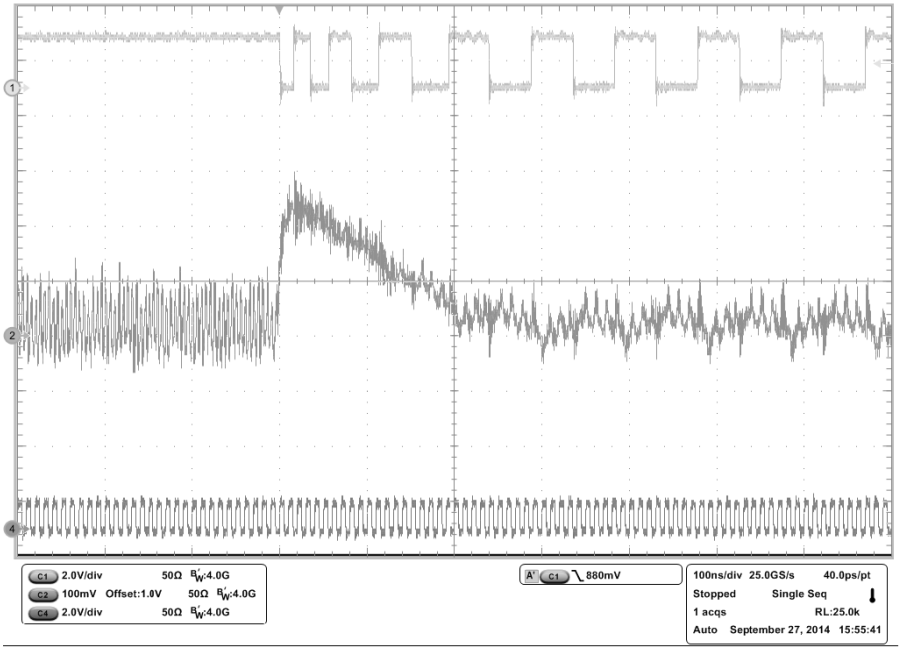


Figure C.32: Positive load transient for the 4:3 ratio from 172 mA to 52 mA at $V_{ref} = 1\ V$, output clock (top), output voltage (middle) and digital clock (bottom)

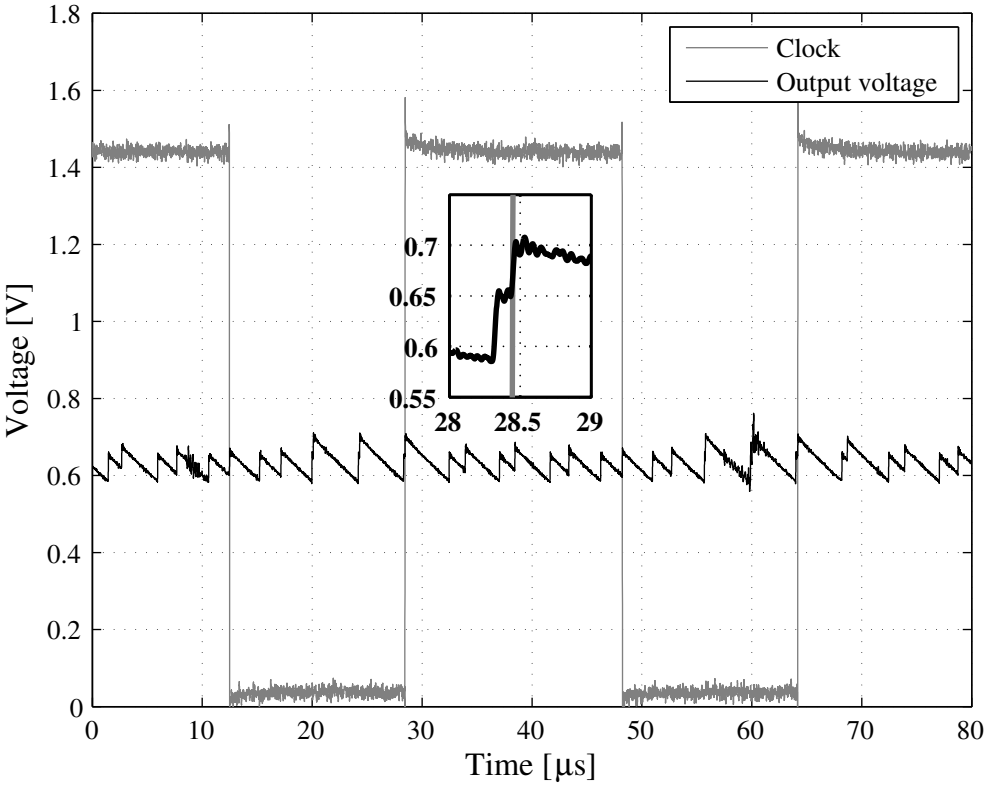


Figure C.33: Operation of the converter under no load condition: output voltage and clock

APPENDIX D

Résumé étendu

D.1 Introduction

Le marché des appareils multimédias ne cesse de croître et avec lui celui des circuits intégrés dédiés. L'évolution ces dernières années de la puissance de calcul est présentée en Fig. 1.1. Les systèmes récents utilisent des circuits issus des nœuds technologiques les plus avancés pour faire face aux contraintes d'intégration et de performances. Malheureusement la consommation de ces circuits croît rapidement alors que la capacité des batteries ne progresse pas aussi vite. La gestion de l'énergie dans ces produits est donc un enjeux crucial pour leur procurer une autonomie suffisante sans pour autant dégrader les performances.
Un carte électronique de *smart-phone* est présentée en Fig. 1.2. On peut différencier les systèmes-sur-puces rassemblant les fonctionnalités du téléphone de ceux qui assurent la gestion de l'énergie. Un grand nombre de composants externes est nécessaire pour proposer de large gamme de tension et de puissance à partir d'une seule source d'énergie: la batterie. Ces derniers occupent une place importante sur la carte et l'espace saturé limite malheureusement le nombre de convertisseurs. Dans le même temps les ressources d'entrées/sorties du boitier du circuit intégré sont aussi limitées. L'élargissement de la gamme de tension appelle clairement à un changement de paradigme. En lieu et place d'alimenter le circuit avec des convertisseurs externes comme présenté en Fig. 1.3, les convertisseurs sont directement intégrés dans le système-sur-puce. La tension de batterie est régulée à un niveau intermédiaire ($1.8\ V$) compatible avec la technologie de fabrication du circuit numérique. La conversion DC-DC à base de convertisseurs à capacités commutées est explorée par l'intermédiaire d'un démonstrateur industriel dans la technologie 28nm FDSOI de STMicroelectronics.

- Le chapitre 2 propose une revue de l'ensemble des techniques dédiées à la gestion d'énergie dans les systèmes-sur-puces. L'état de l'art des alimentations intégrées basées soit sur des inductances soit sur des capacités permet de dresser une figure de mérite pour juger de la pertinence des travaux.

- Le chapitre 3 présente les fondamentaux de la conversion DC-DC à capacités commutées. Les approches de modélisation sont étudiées à travers plusieurs exemples. Les mécanismes des pertes sont détaillés ainsi qu'une approche d'optimisation du rendement énergétique d'un convertisseur. Enfin le principe de régulation de tels convertisseurs ainsi que diverses stratégies de contrôle sont listés.

- Le chapitre 4 décrit l'implémentation de la régulation par modulation de fréquence sous deux approches, linéaire ou non-linéaire.

- Le chapitre 5 concerne la conception du convertisseur dans la technologie 28nm FDSOI. Un premier démonstrateur est fabriqué et caractérisé pour valider l'étage de puissance. Ensuite un deuxième démonstrateur comprenant un contrôleur est également fabriqué pour évaluer les performances de la stratégie de contrôle retenue.

- Le chapitre 6 détaille l'application de la méthodologie de conception à un régulateur de tension négatif dédiée à la polarisation de caisson pour les application basse consommation.

- Les conclusions et les perspectives de ce travail sont exposés dans le chapitre 7.

D.2 État de l'art

D.2.1 Les sources de consommation énergétique

La consommation d'un circuit numérique est séparée en deux composantes : statique et dynamique. La consommation dynamique provient de la commutation des transistors lorsque le circuit est en activité. Les capacités de grille sont chargées et déchargées induisant une consommation énergétique donnée par (2.2). A chaque transition un courant de court-circuit apparait car les transistors N et P conduisent en même temps durant une fraction de temps. Cette énergie perdue donnée par (2.4) contribue également à la consommation dynamique. La consommation statique provient quant à elle de l'ensemble des courants de fuite des transistors, principalement le courant de conduction sous le seuil, le courant de fuite de grille et les

courants de fuite des jonctions drain-source.
La réduction des consommations dynamique et statique entraîne une dégradation des performances du circuit numérique. Par exemple la diminution de la tension d'alimentation réduit la consommation mais diminue aussi le courant à l'état passant du transistor (2.9). Le courant de conduction sous le seuil peut être réduit en augmentant L ou V_t dans (2.6) mais varie à l'opposé de (2.9). Afin d'évaluer le compromis performance et consommation d'un process, on introduit le produit énergie-retard [2].
La mise à l'échelle de la technologie permet d'améliorer le facteur d'intégration mais aussi les performances du transistor. On différencie la technique qui consiste à garder le champ électrique constant dans le transistor de celle qui garde la tension d'alimentation constante [3]. La deuxième technique est préférée car elle permet de garder la compatibilité entre des puces issues de différentes générations. Malheureusement le champ électrique augmente: les effets dit de canaux courts apparaissent, entraînant une augmentation de la densité de puissance et des courants de fuite. Des matériaux à forte constante diélectrique sont donc utilisés pour réaliser les grilles des transistors. L'apparition des substrats sur isolant autorise également des facteurs d'amélioration. Néanmoins la proportion des fonctionnalités assurées par un circuit numérique sont telles que la majorité des progrès proviennent des méthodologies de conception orientées vers la basse consommation.

D.2.2 Les techniques orientées énergie

La problématique de la consommation est considérée très tôt dans la réalisation d'un circuit numérique. La consommation dynamique de l'arbre d'horloge est par exemple économisée grâce au *clock-gating*. Une simple instruction est ajoutée dans le code de la fonction pour suspendre l'activité de l'horloge quand la fonction n'est pas utilisée [1]. Les plateformes de fabrication disposent également de librairies de portes logiques avec différentes tensions de seuil. L'outil de synthèse peut donc sélectionner des portes à faible tension de seuil pour les chemins critiques et des tensions de seuil plus élevées pour économiser des fuites sur les chemins moins critiques [4, 5]. La longueur de grille des transistors peut également être ajustée en suivant les même consignes [6, 7]. Les fournisseurs de microprocesseur proposent également des architectures dédiées. L'architecture big.LITTLE de ARM co-intègre un processeur optimisé pour la consommation énergétique et un autre pour les performances [9]. Les tâches sont donc exécutées à bon escient sur l'un des deux processeurs. L'implémentation matérielle plutôt que logicielle est aussi privilégiée quand cela est possible car cela présente un meilleur compromis comme pour les accélérateurs graphiques.

La technique la plus rependue pour économiser la consommation statique est le *power-gating*. On utilise un interrupteur pour couper l'alimentation d'une fonctionnalité quand celle-ci n'est pas utilisée [10]. L'interrupteur est réalisé par un ensemble de transistors disposés soit en anneaux autour de la fonctionnalité (Fig. 2.2) soit directement distribués à l'intérieur de celle-ci (Fig. 2.3). La configuration distribuée est plus contraignante car elle doit être intégrée dès la conception de la fonctionnalité mais elle permet de limiter les chutes de tension dans la grille d'alimentation. La configuration en anneaux s'adapte elle à toutes les fonctionnalités déjà existantes mais présente un impact sur la surface de silicium beaucoup plus grand car elle ne limite pas autant les chutes de tension. Les principaux enjeux du *power-gating* concerne la conception d'interrupteurs efficaces tout en autorisant des temps de réveil et d'endormissement toujours plus faibles.
L'ajustement de la tension de l'alimentation est la technique la plus agressive car l'énergie décroît avec le carré de la tension. Malheureusement, la fréquence de fonctionnement doit être également diminuée car les transistors deviennent moins rapides. Afin de ne pas impacter tout le circuit, ce dernier est segmenté en différents domaines de tension [17]. La tension et la fréquence sont ajustées en fonction du besoin de chaque tâche. Le *Static Voltage Scaling* applique des niveaux de tension fixes avec des régulateurs placés la plus part du temps à l'extérieur de la puce (Fig. 2.4). Des valeurs discrètes peuvent être utilisées et on parle alors de *Multi-Voltage Scaling* (Fig. 2.5) [18]. La solution la plus aboutie est appelée *Dynamic & Adaptative Frequency Scaling* (Fig. 2.6). Des points de fonctionnement définis par une fréquence et un niveau de tension permettent d'adapter le besoin énergétique et celui de la performance de manière beaucoup plus fine. Les changements s'opèrent dynamiquement grâce à un contrôleur. La température et le type de process sont mesurés afin de sélectionner les points de fonctionnement. L'usage de cette technique est limité par les temps de transition entre chaque point et reste la plupart du temps utilisé pour les blocs qui consomment beaucoup. Plus généralement, ces techniques restent limitées par le nombre de régulateurs externes car le système peut rapidement devenir complexe.
Afin de réduire le courant de conduction sous le seuil ou d'augmenter le courant à l'état passant du transistor, les caissons des transistors peuvent être polarisés pour exploiter le *body effect*. Un exemple est donnée en Fig. 2.7. On considère la polarisation inverse quand $V_{bbp} > vdd$ et $V_{bbn} < gnd$. La tension de seuil des transistors est augmentée réduisant le courant de fuite et les performances. Cette technique s'utilise principalement dans les modes de non utilisation. Au contraire pour accroître la vitesse, la polarisation directe est utilisée: $V_{bbp} < vdd$ et $V_{bbn} > gnd$. La tension de seuil diminue et le courant à l'état passant augmente.

D.2.3 L'alimentation d'un circuit et ses défis

Le réseau de distribution de la puissance dans un système-sur-puce constitue une partie essentielle compte-tenu de l'augmentation significative de la densité de puissance. Ses performances dépendent de la conception de la carte électronique, du choix du boitier et de la stratégie d'alimentation. Une illustration est donnée en Fig. 2.8. La puissance est acheminée depuis la batterie jusqu'aux consommateurs par l'intermédiaire des régulateurs de tension, des pistes de la carte, des boules du boitier et de la grille de distribution dans le circuit. A chaque apparition d'une discontinuité, il y a des effets parasites de type résistifs et inductifs qui sont compensés par l'ajout de capacités de découplage. Le réseau de distribution de puissance est contraint par l'objectif d'impédance (2.10) imposé par les performances du circuit. Le choix du boitier est crucial car le nombre d'entrées/sorties conditionne le maximum de puissance admissible. Le choix d'une architecture hétérogène ou homogène ainsi que 3D se fait en fonction des performances et des coûts comme montré en Fig. 2.9.

Les vendeurs de système-sur-puce accompagnent toujours leurs circuits d'un circuit dédié à la gestion d'énergie. C'est le circuit compagnon. Il contient les régulateurs de tension nécessaires pour faire fonctionner le circuit sous n'importe quelle tension de batterie. L'autonomie de la batterie est également mesurée et un chargeur permet de lui restituer de l'énergie à partir d'une prise secteur. Un bus de communication lui permet de dialoguer avec le système-sur-puce notamment lors des requêtes de changement de niveau de tension. Parmi les régulateurs de tension, on retrouve principalement des convertisseurs inductifs pour les grosses puissances car ils assurent théoriquement un rendement de 100%. Dans la réalité le rendement chute à cause des effets résistifs et des pertes par commutation. Ces derniers permettent également d'élever la tension quand cela est nécessaire. Des régulateurs linéaires à faible tension de déchet sont utilisés pour les blocs sensibles tels que les fonctions analogiques et radio-fréquences. Ils se limitent aux petites puissances car leur rendement est limité par le rapport de la tension de sortie à la tension d'entrée (2.11). On retrouve parfois des convertisseurs capacitifs pour les applications audio mais leur usage reste minoritaire.

Continuer à améliorer le profil énergétique des systèmes-sur-puces avec ce type d'architecture semble difficile. D'abord il est compliqué d'augmenter le nombre de régulateurs externes alors même que la place disponible est de plus en plus réduite. Par ailleurs les ressources des boitiers ainsi que le réseau de distribution ne sont pas en mesure de délivrer tous les niveaux de tension requis et la complexité est telle que la réactivité de la chaîne d'alimentation se dégrade. Les avancés récentes dans le domaine des composants magnétiques et de mise en boitier ont permis d'augmenter

le facteur d'intégration des convertisseurs. Des stratégies d'alimentation avec de la conversion DC-DC intégrée ont également vu le jour comme dans le cas du processeur POWER8 d'IBM [69] où des régulateurs linéaires assurent l'ajustement de la tension d'alimentation. Malgré leur faible efficacité énergétique, ils contribuent à améliorer le profil énergétique du système. Des convertisseurs inductifs et capacitifs totalement intégrés apparaissent aussi dans l'état de l'art. La Fig. 2.13 donne le rendement en fonction de la densité de puissance pour les points de l'état de l'art les plus pertinents. D'autres figures de mérite peuvent être utilisées [71–73] mais celle-ci donne un bon critère d'évaluation en première approche. La densité de puissance de 1 $^{W}/_{mm^2}$ est régulièrement prise comme référence pour un système-sur-puce standard. Un convertisseur qui occuperait seulement 10% de la surface du circuit numérique doit donc présenter un densité de puissance de 10 $^{W}/_{mm^2}$. Il est à la fois difficile d'obtenir une densité de puissance et un rendement élevé. L'architecture Haswell d'Intel [36] est celle qui s'approche le plus de cet objectif avec un rendement supérieur à 90% grâce à des inductances à cœur magnétique directement fabriquées sur la puce. Les convertisseurs utilisant des inductances à air démontrent des résultats intéressants pour des densités autour de 1 $^{W}/_{mm^2}$ alors que les inductances sur silicium proposent de faible densité [43–46]. La densité de puissance des convertisseurs à capacités commutées est essentiellement définie par le type de composant passif utilisé [50–55, 58–60, 74]. Les capacités en tranchée étant les plus denses, elles donnent les meilleurs points dans l'état de l'art [47–49]. Une architecture basée sur des capacités MIM distribuées au dessus du cœur numérique présente un point intéressant [57]. L'état de l'art relate également des convertisseurs résonants [75, 76] et des architectures de convertisseurs cascadés notamment pour tenir de fortes tensions d'entrée [77].

Les convertisseurs à capacités commutées constituent le meilleurs compromis concernant le coût, l'intégration et la performance. La Fig. 2.14 illustre le choix d'implémentation. Les interrupteurs de puissance du convertisseur sont situés en périphérie du bloc à alimenter à la manière du *power gating* et les capacités sont situées au dessus du bloc grâce à l'utilisation de capacités MIM. Autant de convertisseurs que nécessaire peuvent être déployés grâce à une alimentation externe commune de 1.8 V.

D.3 Conversion DC-DC à capacités commutées

D.3.1 Principe et modélisation

Les convertisseurs à capacités commutées sont composés uniquement de capacités et d'interrupteurs. Un abaisseur par deux est décrit en Fig. 3.1. Les interrupteurs S_2

et S_4 sont allumés dans la première phase alors que les interrupteurs S_1 et S_3 sont éteints. La capacité volante se charge entre l'entrée et la sortie. Dans la seconde phase, les interrupteurs S_2 et S_4 sont éteints et S_1 et S_3 s'allument. La capacité volante est maintenant connectée en parallèle avec la sortie. Si l'entrée et la sortie sont interverties, le convertisseur devient un doubleur de tension. Le rendement de ce type de convertisseur ne peut pas idéalement atteindre 100% à cause des pertes par transfert de charge. En effet lorsque deux capacités initialement chargées à des valeurs différentes sont connectées en parallèle (Fig. 3.2), les charges sont réparties et l'énergie disponible est réduite. L'énergie perdue est donnée par (3.5). L'exemple de ce convertisseur abaisseur est utilisé tout au long du manuscrit. Les valeurs des paramètres sont donnés dans le tableau 3.1.

Un convertisseur à capacités commutées peut être représenté par un transformateur avec une résistance série à sa sortie (Fig. 3.3). Le ratio de transformation est donné par la topologie du convertisseur et la résistance de sortie symbolise la chute de tension à la sortie quand le convertisseur est chargé. La valeur analytique de cette résistance peut être calculée de différentes manières. La méthode décrite en [74] permet, grâce à l'analyse de la circulation des charges, de calculer le ratio de conversion et les deux limites asymptotiques de la résistance. On peut différencier deux limites de fonctionnement : la limite basse fréquence et la limite haute fréquence. On peut en effet représenter chaque phase par un circuit RC, correspondant à la résistance à l'état passant des interrupteurs et aux capacités volantes. Ainsi quand la période de découpage est faible devant la constante de temps ainsi formée, le convertisseur fonctionne dans la limite haute fréquence et, inversement, quand celle-ci est grande au regard de la période de découpage, le convertisseur opère dans la limite basse. Pour calculer la résistance dans la limite basse fréquence, on néglige tout les effets résistifs. On défini les multiplicateurs de charge des capacités (3.6) pour représenter la quantité de charge en transit quand les interrupteurs se ferment. On déduit ainsi le ratio de conversion (3.9) et l'expression de la résistance interne (3.10). Cette résistance symbolise les pertes par transfert de charge. Pour calculer la résistance dans la limite haute fréquence, on ne néglige plus cette fois-ci les effets résistifs. On introduit les multiplicateurs de charge des interrupteurs (3.11). Ils représentent les charges qui circulent dans les interrupteurs à chaque phase de fonctionnement. La valeur calculée est donnée par (3.12) et la résistance réunissant les deux composantes du convertisseur en fonction de la fréquence de découpage est donnée par (3.13). Le graphique en Fig. 3.4 donne l'allure de la résistance pour les paramètres du tableau 3.1.

L'équation (3.13) est une approximation de la résistance. Le modèle moyen proposé en [82] est plus précis. Les phases de charge et de décharge sont représentées par

un circuit RC et une source de tension (Fig. 3.7). La valeur de la source de tension dépend de la tension avant que les interrupteurs de chaque phase ne se ferment. En calculant la puissance instantanée dissipée dans chaque phase, on peut déduire la résistance équivalente par phase (3.23). La résistance en fonction de la fréquence est enfin la somme des résistances par phase (3.24). Le résultat est comparé avec le modèle précédent en Fig. 3.8 et montre clairement une meilleure précision.
La modélisation des convertisseurs à découpage est souvent très spécifique [83]. La modélisation échantillonnée a donc été introduite comme une approche uniforme et généralisée. Un convertisseur à découpage est en effet un système hybride (Fig. 3.9) où chaque état de l'automate peut être décrit par des équations différentielles. Une telle modélisation est détaillée en [86] et peut donc être appliquée aux convertisseurs à capacités commutées. On représente chaque état de l'automate avec la représentation d'état. En échantillonnant le système à chaque transition de l'automate, on peut déterminer la dynamique du système en temps discret (3.38). Connaissant le cycle de l'automate, on peut alors calculer la solution périodique en régime établi dite point fixe (3.44). Comme suggéré dans [87], on peut ainsi déterminer la résistance de sortie avec l'équation (3.47). L'extraction du modèle est faite grâce à un outil propriétaire appelé HySim (Annexe A). Cette méthodologie permet notamment de modéliser des convertisseurs entrelacés. Pour démontrer la pertinence de l'approche, nous avons extrait le modèle pour le convertisseur abaisseur simple, pour le convertisseur abaisseur entrelacé quatre fois avec des temps d'entrelacement égaux ou arbitraires. Les simulations de l'automate et du modèle échantillonné sont données en Fig. 3.11, Fig. 3.12 et Fig. 3.13. La résistance de sortie est comparée avec les autres modèles en Fig. 3.14. Le modèle échantillonné et moyen donnent les mêmes résultats.

D.3.2 Bilan des pertes et optimisation

Le bilan des pertes permet de calculer le rendement du convertisseur et par la suite de l'optimiser. Les pertes proviennent d'abord de la dissipation d'énergie dans la résistance de sortie. Ces pertes dépendent de la valeur de la résistance et croissent avec le carré du courant de sortie. Les principaux contributeurs dans la limite basse fréquence sont les valeurs des capacités volantes et dans la limite haute fréquence, ce sont les effets résistifs (résistance à l'état passant des interrupteurs et résistances séries des capacités) qui dominent. Les effets parasites dus à l'implémentation physique des capacités et des interrupteurs viennent s'ajouter. Les transistors introduisent des pertes en commutation par leurs capacités de grille. Ces pertes sont proportionnelles à la taille des transistors et à la fréquence de découpage. Les ca-

pacités présentent des couplages entre le substrat et leurs électrodes. Ces couplages sont pris en compte par des capacités parasites qui sont chargées et déchargées au cours du fonctionnement. Ces pertes sont proportionnelles à la taille des capacités et à la fréquence de découpage. Toutes les capacités ne présentent pas les mêmes couplages suivant le type d'implémentation. Le tableau 3.3 donne qualitativement la variation des pertes en fonction des dimensions et des paramètres de fonctionnement.
On peut ainsi optimiser le rendement du convertisseur pour un objectif de résistance de sortie donné. Cet objectif dépend de la valeur maximale du courant de sortie et de la tension de sortie désirée. Généralement on commence par fixer la valeur de la capacité volante car c'est elle qui détermine la surface occupée dans le cas d'un convertisseur entièrement intégré. On fait ensuite varier conjointement la fréquence de découpage et la taille des transistors pour atteindre le point optimal. Les implémentations de capacités peuvent être comparées en surface comme sur Fig. 3.17. Le convertisseur est optimisé pour plusieurs type de capacités et pour plusieurs valeurs de surface. La densité de puissance est aussi une figure de mérite très répandue car elle permet une comparaison et une mise en évidence des compromis. La Fig. 3.18 montre ainsi que la densité de la capacité est primordiale pour obtenir des rendements élevés à forte densité de puissance. En revanche à faible densité de puissance les couplages parasites deviennent prépondérants.

D.3.3 Réduction de l'ondulation de la tension de sortie

Les convertisseurs à capacités commutées sont bien connus pour leur forte valeur d'ondulation de la tension de sortie. Cette ondulation est due au caractère discret du convertisseur et au transfert de charge qui se fait dans la capacité de sortie. Les charges sont délivrées par paquet et ne correspondent pas aux besoins instantanés de la charge. Ce phénomène est donc lissé par l'ajout d'une capacité réservoir à la sortie. L'ondulation de la tension de sortie est inversement proportionnelle à sa valeur ainsi qu'à celle de la fréquence de découplage. L'augmentation du courant de charge, quant à lui, augmente la valeur de l'ondulation (3.70). Malheureusement dans les architectures intégrées, il est bien souvent prohibé d'intégrer une capacité réservoir pour des soucis d'encombrement. Dans ce cas là, on utilise l'entrelacement. Le convertisseur est divisé en N sous-cellules. Les tailles des capacités et des transistors sont divisées par ce même facteur et les sous-cellules sont connectées en parallèle. L'horloge de découpage est décalée dans le temps pour chaque sous-cellule de T_{sw}/N, où T_{sw} correspond à la période de découpage. Les charges sont ainsi délivrées par petites quantités mais plus régulièrement dans le

temps, ce qui minimise l'ondulation. La Fig. 3.23 donne son allure. De cette manière avec un entrelacement suffisant on peut réduire la valeur de la capacité réservoir ou même la supprimer. Le facteur d'entrelacement est limité par la complexité de l'implémentation et par la génération des horloges.

D.3.4 Contrôle et régulation

La tension de sortie d'un convertisseur à capacités commutées est fonction de sa résistance de sortie et du ratio de conversion comme le montre l'équation (3.71). La tension de sortie ne peut jamais atteindre le ratio idéal de conversion quand le convertisseur est chargé. On peut réguler de deux façons : soit on ajuste dynamiquement le ratio de conversion avec des topologies reconfigurables, soit on ajuste la valeur de la résistance de sortie. La première méthode constitue une régulation grossière et on préfère moduler la résistance de sortie pour un réglage plus fin. Cette technique introduit donc des pertes supplémentaires à la manière d'un régulateur linéaire. On peut donc réguler soit dans la limite basse fréquence soit dans la limite haute fréquence. Dans la limite basse fréquence, il faut changer la valeur de la capacité volante, par exemple de façon discrète [91]. On peut également jouer sur la valeur de la fréquence de découpage. Dans la limite haute fréquence, on peut utiliser la modulation de largeur d'impulsion [92] ou la modulation de la taille des transistors [90]. La modulation de fréquence est la méthode la plus simple et la plus avantageuse car la fréquence diminue avec le courant de charge. Les pertes par commutation sont ainsi réduites et le rendement est maximisé. La fréquence de découpage varie également sur une large plage de valeur, ce qui n'est pas le cas du rapport cyclique, de la taille de transistors et des capacités.
Afin d'établir une stratégie de contrôle, il faut modéliser en petits signaux le convertisseur. Le modèle continu dans le domaine de Laplace est construit à partir de (3.71) et donné en Fig. 3.24. On peut calculer la fonction de transfert de la tension d'entrée vers la tension de sortie (3.72) et celle du courant de charge vers la tension de sortie (3.73). Pour faire apparaitre la fonction de transfert indispensable au contrôle, il faut procéder à la linéarisation du système. Le modèle échantillonné est donc linéarisé comme décrit dans [86]. On obtient les fonctions de transfert du rapport cyclique vers la tension de sortie et celle de la fréquence de découpage vers la tension de sortie dans le domaine discret, (3.100) et (3.102) respectivement puis dans le domaine continue à l'aide de la transformation du bloqueur d'ordre zéro. On montre ainsi aisément que le système se comporte comme un première ordre avec un pôle dépendant de la capacité de sortie et de la valeur de la résistance de sortie. Ce pôle bouge donc lors de la régulation. La méthode de linéarisation est comparée entre le modèle échantillonné et le modèle de Laplace pour les différentes

méthodes de modélisation de la résistance de sortie. Les résultats sont donnés en Fig. 3.26, Fig. 3.27, Fig. 3.28 et Fig. 3.29.

D.4 Contrôle par modulation de fréquence

Il vient souvent à l'esprit d'utiliser des contrôleurs de type "marche/arrêt" pour réguler des convertisseurs à capacités commutées. Le convertisseur fonctionne à une fréquence maximale quand sa tension de sortie est en dessous de la référence de tension et il est désactivé quand elle est au dessus. Cependant cette approche reste empirique et ne permet pas d'obtenir des performances raisonnables aussi bien au niveau des performances transitoire que du rendement. Il existe deux approches dans le contrôle d'un convertisseur. Les approches linéaires basées sur l'analyse en petits signaux et le placement de pôle ainsi que les approches non-linéaires. Intel a breveté une solution non linéaire appelée "single bound hysteretic control" [99]. Un comparateur échantillonné délivre des impulsions à un registre à décalage rebouclé sur lui même comme montré en Fig. 4.1. Quand la tension de sortie est inférieure à la référence la sortie du comparateur commute. En revanche quand la tension de sortie est au dessus de cette référence, la sortie du comparateur est inactif. Cette méthode de contrôle permet de réguler la tension minimale et non la tension moyenne, ce qui est intéressant quand il y a beaucoup d'ondulation sur la sortie. Elle peut être également utilisée pour des convertisseurs multiphases. Le principal inconvénient est le recours à une horloge haute fréquence pour l'échantillonnage du comparateur. Il faut qu'elle soit suffisamment élevée pour éviter les oscillations avec des sous-harmoniques [94]. Un résultat de simulation est donné en Fig. 4.3.
Dans cette thèse, nous avons exploré des contrôles linéaires et en mode glissant. Le premier contrôle linéaire est un contrôle en tension comme montré en Fig. 4.5. La référence de tension est soustraite à la tension de sortie pour former un signal d'erreur. Ce signal d'erreur est utilisé par un compensateur qui vient contrôler un oscillateur. La fréquence de découpage est donc asservie. L'oscillateur et l'étage de puissance sont linéarisés pour dimensionner le contrôleur dans le domaine fréquentiel. Le système possédant un seul pôle, un compensateur de type proportionnel-intégral suffit. Les équations (4.15) et (4.16) permettent de déterminer respectivement K_p et T_i dans le cas d'un comportement en premier ordre et le comportement en deuxième ordre est donné par (4.21) et (4.20). Un diagramme de Bode est donné en Fig. 4.7 ainsi qu'un résultat de simulation d'un transitoire de charge en Fig. 4.8. Les performances de ce contrôle dépendent de la bande passante du contrôleur et de la capacité de sortie. On préfère augmenter la bande passante car on veut limiter l'usage de composant externe. La problématique avec cette

approche de conception réside dans les approximations due à la linéarisation. On propose donc de construire le modèle échantillonné du système en boucle fermée. Les instants de commutation sont donnés par la loi de contrôle et on ajoute donc une fonction contrainte (4.38) à la solution du vecteur d'état en régime établi (4.37). La linéarisation du modèle dynamique (4.39) et (4.40) donne la dynamique en petits signaux en boucle fermée dans le domaine discret (4.42). La stabilité et la robustesse du système peuvent être étudiées dans le cercle unité. Si les valeurs propres du système sont situées à l'intérieur du cercle, le système est stable. On peut évaluer la robustesse grâce aux contours des pulsations et des facteurs d'amortissement. La Fig. 4.16 montre par exemple la carte des valeurs propres pour des variations de tension de référence et la Fig. 4.18 pour des variations des paramètres du contrôleur. Cette stratégie de contrôle s'avère suffisamment robuste car le système reste stable mais les performances peuvent être dégradées.

La fréquence de découpage est proportionnelle au courant de charge. Nous proposons donc d'ajouter une boucle supplémentaire qui prend en compte la variation de courant. Le principe est donné en Fig. 4.19. Le courant est mesuré par un capteur et l'information est ajoutée au signal de contrôle de l'oscillateur. Ainsi dès que le courant de sortie augmente la fréquence de découpage augmente aussi. Il y a donc une boucle rapide en courant et une boucle plus lente en tension. Le capteur de courant peut être réalisé par une résistance série placée à la sortie du convertisseur comme en Fig. 4.20. La chute de tension aux bornes de cette résistance est mesurée par un amplificateur puis filtrée avec un filtre passe-bas. Le dimensionnement débute par l'étude de la boucle rapide. Si la bande passante du filtre est suffisamment élevée par rapport au pôle de l'étage de puissance, un contrôleur PI est suffisant pour la boucle en tension. Le diagramme de Bode de la Fig. 4.29 illustre le propos et les résultats de simulation de la Fig. 4.30 montrent l'intérêt de la boucle rapide. Cependant la sensibilité à la variation du courant de charge (Fig. 4.31) et de la tension de référence (Fig. 4.32) montre une robustesse plus faible. La robustesse et les performances transitoires peuvent être améliorées par l'utilisation d'un contrôle non linéaire dit en mode glissant. Ce type de contrôle est déjà appliqué aux convertisseurs inductifs avec succès car la loi de contrôle permet de commander l'étage de puissance directement [102, 103]. On peut appliquer un contrôle en mode glissant simplement en analysant la tension dans la capacité volante en régime établie. Son allure est donnée en Fig. 4.33. On montre aisément que dans le cas d'un convertisseur abaisseur par deux, la tension moyenne vaut $Vin/2$. L'ondulation de la tension en fonction de la fréquence de découpage est donnée par (4.89). Les phases de charge et de décharge sont donc délimitées par la tension moyenne dans la capacité et on peut alors décrire la surface de glissement avec l'équation (4.94).

Après vérification de l'existence du mode glissant, on obtient l'automate hybride de la Fig. 4.35. Quand la tension dans la capacité volante est supérieure à $Vin/2$ le convertisseur passe dans la phase de décharge et quand celle-ci est inférieure, il passe dans la phase de charge. La fréquence de découpage tend alors vers l'infini. Pour la réguler, on peut introduire un retard contrôlé par une boucle linéaire en tension (Fig. 4.36). Ce type de stratégie donne des résultats similaires à la boucle linéaire avec une modulation de fréquence comme le rapporte les simulations transitoires de la Fig. 4.38. Une approche beaucoup plus efficace consiste à contraindre l'ondulation dans la capacité avec une hystérésis. Le système décrit par l'équation (4.127) est illustrée en Fig. 4.39. Le convertisseur passe dans la phase de décharge quand la tension dans la capacité atteint la borne haute et dans la phase de charge quand elle atteint la borne basse. La modulation de l'hystérésis se fait en utilisant une boucle linéaire en tension comportant un intégrateur comme le montre la Fig. 4.40. Le mode glissant agit comme une boucle rapide et la boucle linéaire permet d'annuler l'erreur statique due notamment aux effets résistifs. La Fig. 4.46 montre d'excellentes performances en transitoire de charge mais les performances en transitoire de ligne montrés en Fig. 4.47 peuvent encore être améliorés. Les bornes hautes et basses peuvent être imposées non plus par une hystérésis dans le comparateur mais par les équations (4.174) et (4.175). Une boucle linéaire est aussi nécessaire pour les mêmes raisons qu'évoquées précédemment. Le schéma du contrôleur est donné en Fig. 4.52 et les simulations transitoires de ligne montre clairement le bénéfice de cette méthode Fig. 4.55.
En conclusion, les contrôleurs en mode glissant sont prometteurs car ils démontrent d'excellentes performances transitoires. Malheureusement ils ne sont, pour l'heure, pas extensibles pour des convertisseurs mutliphases. Les lois linéaires permettent de réaliser des contrôles à moindre coût et peuvent être appliquées à du multiphase en utilisant simplement des oscillateurs multiphases.

D.5 Démonstrateur

Pour répondre aux problématiques de la thèse nous avons proposé une architecture de convertisseur à capacités commutées, modulaire, dans la technologie 28nm FDSOI de STMicroelectronics. La vue en 3D d'un transistor MOS en FDSOI est donnée en Fig. 5.1. La technologie ne remet pas en cause les dimensions fondamentales du transistor. Une fine couche d'oxyde est ajoutée en dessous du canal du transistor. Ce canal n'est pas dopé et il est complètement isolé du substrat par l'oxyde enterré. La longueur effective du canal est réduite ainsi que les capacités parasites, ce qui permet au transistor de fonctionner plus vite. La tension de seuil

est contrôlée par l'implémentation des caissons, donnant pour des caissons opposés au type de transistor, des tensions de seuil standard et faibles si les caissons sont de même type que le transistor. Grâce à deux épaisseurs d'oxyde de grille, on dispose de transistor à faible tension (1 V) et à forte tension (1.8 V).

L'architecture proposée est décrite en Fig. 5.4. Les interrupteurs de puissance des cellules de conversion sont disposés côte à côte autour du cœur numérique. Les capacités volantes sont placées au dessus de ce cœur avec la grille d'alimentation grâce à l'utilisation de capacités MIM. Un oscillateur en anneau est propagé autour du cœur pour fournir la fréquence de découpage à chaque cellule en les entrelaçant. La longueur de l'anneau est ajusté avec le nombre de cellule en fonction de la taille du cœur. La fréquence de l'oscillateur en anneau est contrôlée par sa tension d'alimentation. Un contrôle linéaire avec une boucle en tension est choisi et le contrôleur peut être placé facilement prés de l'oscillateur, ce qui limite les contraintes de placement et routage. La cellule de conversion est composé de six capacités volantes et de 29 interrupteurs qui permettent de réaliser quatre ratios de conversion : 3:1, 2:1, 3:2 et 4:3. Le schéma électrique est donné en Fig. 5.6 et l'arrangement des capacités suivant les différentes phases et ratios, en Fig. 5.5. Les interrupteurs de puissance sont implémentés avec des transistors double oxyde et faible de tension de seuil. La grille et la face arrière sont connectés ensemble pour diminuer la tension de seuil quand le transistor est allumé et l'augmenter quand il est éteint. Les capacités volantes sont réalisées avec un motif compatible avec le pas de routage de la grille d'alimentation. La grille d'alimentation est fabriquée avec les métaux les plus épais et la capacité MIM est placée entre ces deux métaux. Des trous sont ménagés dans les électrodes des capacités pour connecter les niveaux de métaux de la grille d'alimentation. Ceci décroît la densité effective du dispositif. Les électrodes des capacités sont connectées sur les abords du domaine. Une ligne de métal est utilisée pour l'électrode supérieure car elle présente une forte résistance série. Une vue de l'assemblage en 3D est donné en Fig. 5.10. Un prototype a été réalisé dans un premier temps pour valider l'architecture et évaluer son rendement sans contrôleur. Un convertisseur comportant huit cellules entrelacées pour une surface de cœur numérique d'environ 1 mm^2 est implémenté dans un circuit de test montré en Fig. 5.14. La tension d'entrée est de 1.8 V pour générer des tensions de sortie allant de 0.2 V à 1.2 V pour un courant maximal de 250 mA. Malgré un déviation process significative, les mesures du rendement ont permis de démontrer un rendement pic de 75% sous le courant maximal (Fig. 5.24). Dans un deuxième temps, le contrôleur PI a été finalisé et embarqué dans un nouveau circuit de test donné en Fig. 5.30. Le compensateur est réalisé avec un amplificateur classe AB et un réseau de compensation (Fig. 5.28). Le contrôleur peut être configuré en mode

suiveur pour le déboguage du circuit. Les performances statiques et dynamiques du circuit ont été mesurées et les résultats sont comparés avec l'état de l'art dans le tableau 5.5. L'ondulation de la tension de sortie reste encore élevée principalement à cause de la distribution spatiale de l'oscillateur qui ne permet pas de garantir un entrelacement parfait. Les transitoires de charge peuvent être améliorés en agissant sur la bande passante du contrôleur. Malgré tout, la pénalité de surface représente seulement 11.5% de la surface du cœur, ce qui constitue la deuxième meilleure performance de l'état de l'art.

D.6 Générateur de tension pour caisson

La polarisation des caissons des transistors est utilisée pour réduire le courant de fuite ou pour accélérer le transistor. La technologie présente certains avantages comparés à la technologie bulk. Les vues en coupe d'un inverseur sont respectivement données pour la technologie bulk, la technologie FDSOI avec l'architecture standard et pour l'architecture à caissons inversés en Fig. 6.1, Fig. 6.2 et Fig. 6.3. Le substrat est isolé par un caisson profond de type N. L'oxyde enterrée permet d'isoler le canal du substrat contrairement au bulk. La plage de polarisation est donc plus importante pour le FDSOI et les comparaison sont données en Fig. 6.4.
Le défi est de concevoir les régulateur de tension capable de générer des tensions négatives. L'architecture de STMicroelectronics pour générer des tensions négatives est présentée dans [7] et détaillée en Fig. 6.5. La tension négative est produite grâce à un convertisseur à capacités commutées. Un amplificateur avec un étage de sortie de type classe AB adapte alors la tension fournie par le convertisseur numérique-analogique au caisson. L'inconvénient de cette architecture est que le convertisseur de tension négative n'est pas régulé, ce qui nécessite une forte valeur de capacité externe. Notre proposition consiste à réguler le convertisseur pour directement polariser les caissons. Il n'y a plus besoin d'amplificateur et de capacité externe. La consommation et le facteur d'intégration s'améliore. L'architecture est présentée en Fig. 6.6. Une boucle avec une modulation de fréquence est utilisée. Un capteur de tension permet de transformer la tension négative en tension positive pour faire la régulation à partir d'une référence positive. Un réseau programmable de résistances dans le capteur de tension (Fig. 6.7) permet de sélectionner les différentes tensions de sortie. L'équation (6.1) donne la relation pour la conversion de la tension négative suivant les valeurs du réseau programmable du tableau 6.1.
L'étage de puissance retenu est présenté en Fig. 6.8. Deux cellules sont entrelacées en paires croisées ce qui permet grâce à des translateurs de niveau capacitifs de faciliter la commande des transistors de puissance. Un transistor est utilisé pour recycler

les charges dans les capacités parasites. Le fonctionnement du convertisseurs assure l'absence de court-circuit entre chaque phase comme le détaille le chronogramme de la Fig. 6.9. La technologie FDSOI offre plusieurs types de capacité comme les capacités MOM et les capacités MOS en inversion. Les différentes configurations de la capacité MOS sont évaluées dans le tableau 6.2 pour déterminer le meilleur compromis en surface, en densité et en parasite. L'utilisation de la modélisation échantillonnée permet de montrer l'influence des parasites sur la tension de sortie notamment.
L'oscillateur contrôlé en tension est réalisé par la structure de la Fig. 6.25. La résistance permet de linéariser la caractéristique tension-fréquence comme le montre son extraction pour différents types de process en Fig. 6.26. Grâce à un modèle propriétaire de la charge formée par les caissons, la caractéristique de transfert fréquence de découpage vers tension de sortie est obtenue avec la consommation du convertisseur en Fig. 6.24. Le contrôleur PI est simplement réalisé avec un amplificateur à transconductance classique de la Fig. 6.28. La structure relativement minimaliste garantit un faible encombrement et une faible consommation. L'étage de puissance est modélisé pour dimensionner la boucle et garantir la stabilité sur les points de fonctionnement. Le résultat est donné par le diagramme de Bode de la Fig. 6.30. Les simulations de l'architecture globale établissent de bonnes performances transitoires (Fig. 6.31) tout en présentant une faible consommation (Fig. 6.32).

D.7 Conclusion

La complexité actuelle de l'alimentation d'un système-sur-puce comportant de nombreux domaines de tension avec des régulateurs externes n'est pas tenable. L'intégration de l'alimentation s'impose pour répondre au challenge de consommation et de performance. Les convertisseurs à capacités commutées sont d'excellents candidats grâce à leur potentiel d'intégration et leur faible coût, bien que les convertisseurs inductifs, qui nécessitent des technologies spécifiques, obtiennent de meilleurs rendements. L'architecture retenue consiste a placer les capacités volantes au dessus du cœur numérique et les interrupteurs de puissance autour, afin de limiter la surface de silicium consommée.
Le chapitre 2 dresse l'état de l'art des techniques à faibles consommations utilisées dans les systèmes-sur-puces. Il permet d'établir les problématiques mais aussi les défis quand à l'intégration d'une alimentation.
Le chapitre 3 expose les fondamentaux de la conversion à capacités commutés en allant de la modélisation du comportement jusqu'à l'analyse des pertes en passant

par l'analyse en petits signaux.
Le chapitre 4 détaille la régulation de tels convertisseurs. L'implémentation ainsi que les méthodologies de dimensionnement de régulations linéaires et en mode glissant sont présentées. La modélisation dites échantillonnée est largement utilisée pour les démonstrations.
Le chapitre 5 présente l'architecture du convertisseur dans la technologie 28nm FDSOI de STMicroelectronics. Des prototypes ont été fabriqués pour évaluer le rendement mais aussi les performances d'une régulation linéaire avec une modulation de fréquence.
Le chapitre 6 démontre l'application de la modulation de fréquence à un convertisseur à capacités commutées pour générer des tensions négatives pour des applications de polarisation de caisson en FDSOI. Les résultats de simulations établissent la pertinence de l'approche.
En conclusion, les contributions énoncées valident la proposition originale de l'architecture. Les performances sont en ligne avec l'état de l'art même s'il reste encore de nombreuses voies à explorer. Il reste notamment à concevoir un système de gestion et de sélection instantanée du ratio du convertisseur. Les caractérisations en température doivent aussi permettre de valider plus en profondeur la régulation analogique. Finalement, l'implémentation de cette architecture conjointement avec un vrai bloc numérique confirmerait définitivement la pertinence de la proposition.

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TITRE : Contribution to the design of switched-capacitor voltage regulators in 28nm FDSOI CMOS

Contribution à la conception de régulateurs de tension à capacités commutées en technologie 28nm FDSOI CMOS

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RESUME : Mobile and multimedia devices offer more innovations and enhancements to satisfy user requirements. Chip manufacturers thus propose high performances SoC to address these needs. Unfortunately the growth in digital resources inevitably increases the power consumption while battery life-time does not rise as fast. Aggressive power management techniques such as dynamic voltage and frequency scaling have been introduced in order to keep competitive and relevant solutions. Nonetheless continuing in this direction involves more disruptive solutions to meet space and cost constraints. Fully integrated power supply is a promising solution. Switched-capacitor DC-DC converters seem to be a suitable candidate to keep compatibility with the manufacturing process of digital SoCs. This thesis focuses on the design of an embedded power supply architecture using switched-capacitor DC-DC converters.Addressing a large range of output power with significant efficiency leads to consider a multi-ratio power stage. With respect to the typical digital SoC, the input voltage is 1.8 V and the converter is specified to deliver an output voltage in the 0.3-1.2 V range. The reference voltage is varying according to typical DVFS requirements. A modular architecture accommodates the digital design flow where the flying capacitors are situated above the digital block to supply and the power switches are located as an external ring. Such an architecture offers high flexibility. Interleaving strategy is considered to mitigate the output voltage ripple. Such a converter admits the switching frequency as a control variable and linear regulation and hysteretic control are analyzed. A prototype has been fabricated in 28nm FDSOI technology by STMicroelectronics. A power density of 310 mW/mm^2 is achieved at 72.5% peak efficiency with a silicon area penalty of 11.5% of the digital block area. The successful design methodology has been also applied to the design of a negative SC converter for body-biasing purpose in FDSOI. Simulation results demonstrate a strong interest for low power application.

MOTS-CLÉS : system on-chip, voltage regulator, switched-capacitor

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