Modeling and characterization of electrical effects of Ge integration in Metal/High-k/SiGe MOS structures

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UNIVERSITÉ DE GRENOBLE

THÈSE

Pour obtenir le grade de

DOCTEUR DE L'UNIVERSITÉ DE GRENOBLE

Spécialité : **Nano électronique et Nano Technologies**

Arrêté ministériel : 7 août 2006

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préparée au sein du **laboratoire IMEP-LAHC**, le **CEA-Leti** et de l'**entreprise STMicroelectronics**
dans **l'École Doctorale « Electronique, Electrotechnique, Automatique et Traitement du Signal »**

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Thèse soutenue publiquement le **« 03 Avril 2014 »**,
devant le jury composé de :

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This thesis is dedicated to
my parents,
my grandmother
and
persons who believe in me.

Acknowledgements

Writing this dissertation has been one of the most significant academic challenge I have ever had to face. Unless the support, encouragement and guidance of the following people, this thesis would not have been completed. It is a pleasure to thank them for their contribution and valuable assistance in the preparation and completion of this study.

Foremost, I owe my deepest gratitude to my supervisor Dr. Gérard Ghibaudo. Without your continuous optimism concerning this work, enthusiasm, encouragement and support this study would hardly have been completed. Your wisdom and immense knowledge inspired and motivated me. Despite your many other academic and professional commitments, you often have been present for discussion and have painstakingly e-mailed the information I needed. I consider it an honor to work with you and to present our methods to extract electrical parameters in MOSFETs in the ULIS conference. My sincere thanks also for offering me the three months opportunity in the IMEP lab and leading me finishing this manuscript in excellent atmosphere. I could not have imagined having a better advisor and mentor for my PhD study.

I would like to express my special appreciation and sincere gratitude to my co-advisor Dr. Charles Leroux. Over the past three years, you have been a tremendous mentor for me. I would like to thank you for encouraging my research and for allowing me to grow as a research scientist. Your good advice, excellent guidance, caring, kindness and continual support have been invaluable on both an academic and a personal level. During this thesis, you spent countless hours proofreading, listening to me talk about my research and patiently corrected my writing. You deserve very special thanks for believing in me.
I am deeply grateful to my second co-advisor Dr. Denis Rideau for his help and motivation. Your critiques helped to mold my analysis and always forced me to think beyond and improve things. Working with you is a priceless experience that has turned me from a young student into a professional in numerical simulation.

I would like to thank Professor Brice Gautier for serving as my committee member. I would also like to express my gratitude to Professor Pascal Masson and Dr. Daniella Muntenau for reviewing this thesis. Thank you for letting my defense be an enjoyable moment and for your brilliant comments and suggestions.

I am grateful to Dr. Gilles Reimbold and Ing. Clément Tavernier for making it possible to carry out this work in their teams.

My appreciation and thanks go also to Gregory Bidal, Olivier Saxod, Mustapha Rafik, Giovanni Romano, Alain Toffoli, Vincent Delaye, Philippe Blaise, Francois Bertin, Guillaume Audoit and Qentin Rafhay. Collaborations and discussions with you were always a great pleasure, and led to significant improvements in the content and exposition of this work. I have benefited from your priceless skills.

Special thanks goes to the members of my research group who have made working at CEA enjoyable and eventful: Sylvain, Jean, Alexandre, Xavier, Mikael, Masahiro, Carlos, Denis, Guillaume, Jonathan, Joanna, Rabah and Fabienne. I also thank Marie-anne, Pierrette, Sébastien

and François for thier encouragements. I am indebted to my many colleagues at ST-Crolles who supported me: Amina, Ben, Seb, Zahi, Joris, Floria, Frédéric, Gabriel, Olivier Nier, Sylvain, Yvan, Komiatchou, François, Fabio, Salim, Michel, Benoit Legoix, Vincent, Patrick, Xavier, Guillaume, Nayera, Emmanuel, Cheikh and Jérôme. I am also gratful to my colleagues at IMEP-LAHC Tapas and Ramin.

I would also like to thank all of my friends who supported me in writing, and incented me to strive towards my goal.

Finally, a special thanks to my family. Words cannot express how grateful I am to my parents for all of the sacrifices that you have made on my behalf.

Contents

General introduction

Contents

The downscaling of metal-oxide-semiconductor field-effect transistor (MOSFET) geometry has been a very successful process to improve the performances of CMOS devices. The guideline of the technology improvements in MOSFET fabrication is the International Technology Roadmap for Semiconductors (ITRS). According to the ITRS [1], devices which enter the mass production in 2014 should integrate further ultrathin EOT with higher-k materials as dielectrics. Table 1 reports the 2014 ITRS target of the physical gate length, equivalent oxide thickness and threshold voltage for bulk and fully depleted SOI (FDSOI) devices.

ITRS target	Bulk	FDSOI
Physical gate length (nm)	**18**	**18**
Equivalent oxide thickness (nm)	**1.04**	**1.2**
Threshold voltage (V)	**0.3**	**0.22**

Table 1: ITRS target of the physical gate length, equivalent oxide thickness and threshold voltage for bulk and fully depleted SOI (FDSOI) devices which enter the mass production in 2014 [1].

Nevertheless, conventional scaling down of MOSFET dimensions, according to aggressive ITRS requirements, faces physical and economical limits. Further CMOS scaling for sub-45nm node [2] relies on new materials integration such as metal gate electrode together with high-k dielectric and new channel materials, or alternative device structures, such as fully depleted SOI devices.

To be able to achieve the ITRS roadmap objectives, low threshold voltage metal gate MOSFETs, especially with small EOT, has been a challenging problem for implementation in the manufacturing CMOS flow at every new technological node. In practice, the threshold voltage of a MOSFET is controlled by the adjustment of two parameters: the work functions of the gate and substrate.

In this introduction, we firstly introduce high-k dielectrics integration, the MOS threshold voltage adjust and FDSOI structures. Then, we describe problems and explore the purpose of this thesis. Finally, the organization of the thesis is presented.

High-k dielectrics integration

As device scaling progresses, gate dielectric physical thickness becomes extremely thin. The oxide thickness shrinking leads to a leakage current increase because of the quantum mechanical tunnel effect (figure 1). In order to reduce the probability that an electron passes through the dielectric (tunneling between gate and channel), the potential barrier between channel and gate should be thicker in space or higher in energy. Silicon dioxide (SiO_2) has been widely used as

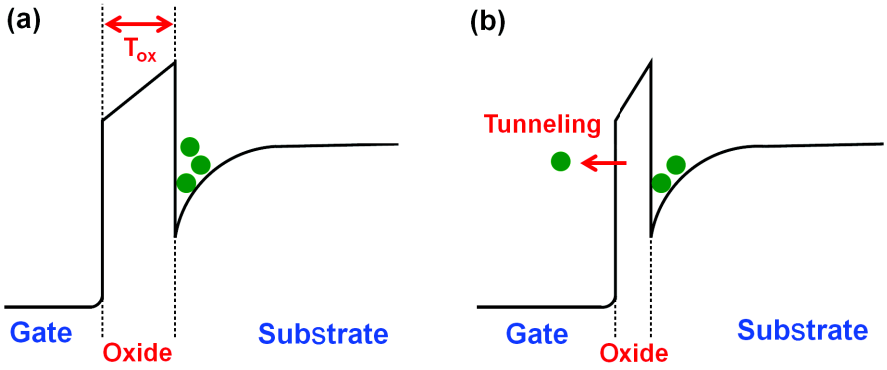


Figure 1: Band diagram of structures with a thick (a) and thin (b) gate dielectric. In the thin oxide structure, a leakage current increases because of the quantum mechanical tunnel effect.

gate dielectric because of its high insulation, passivation, and process compatibility with Si [1]. However, as device miniaturisation continues, physical thickness of SiO_2 gate insulator becomes ultrathin. This results in significant carriers tunneling from the MOSFET channel to the gate electrode leading to an undesired gate leakage current increase (figure 2). Therefore, scaling of MOSFETs with SiO_2 gate dielectrics reaches its limit. High-k materials have been promising candidates to substitute the SiO_2 dielectrics and break its limitation.

Indeed, high-k oxides have high dielectric constants. Thus, their introduction allows a dielectric thickness increase (which should decrease the gate leakage) for the same gate oxide capacitance (C_{ox}) (figure 3):

$$C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} \tag{1}$$

where ε_{ox} and T_{ox} are the dielectric constant and thickness.

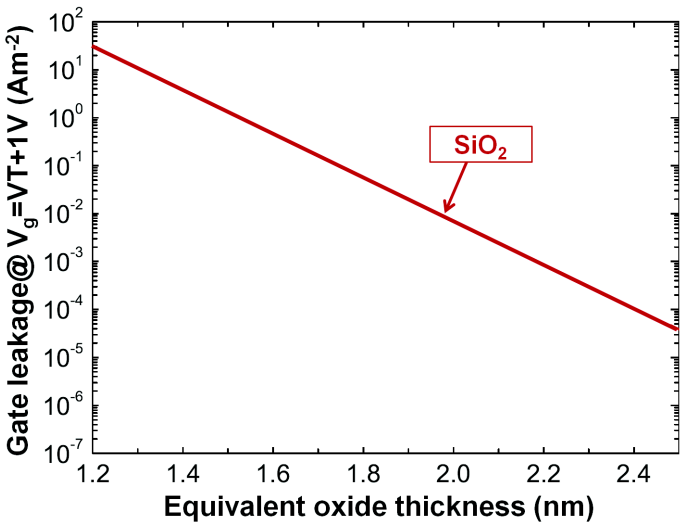


Figure 2: Inversion gate leakage as a function of equivalent oxide thickness for SiO_2 dielectric [3][4].

It is worth noting that the figure of merit which expresses scaling of high-k gate dielectrics is the equivalent oxide thickness (EOT), given by:

$$EOT = \frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}}.T_{high-k} \tag{2}$$

where ε_{SiO_2} and ε_{high-k} are the SiO_2 and high-k dielectric constants. T_{high-k} is the high-k physical thickness.

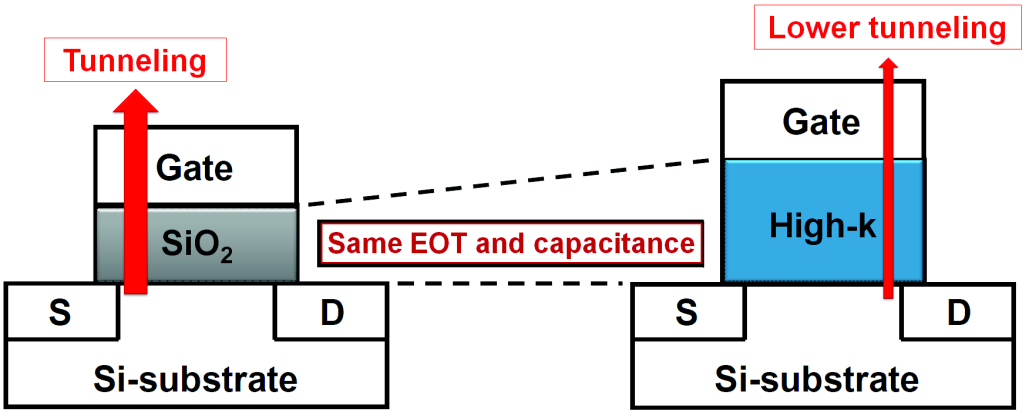


Figure 3: High-k gate dielectrics introduction allows the dielectric thickness increase and gate leakage decrease for a same gate oxide capacitance.

Equation 2 and figure 3 show that using a material with a dielectric constant n times larger than the SiO_2 one, gives the possibility to obtain the same C_{ox} with n times larger thickness. However, high-k dielectrics have a smaller potential barrier height than SiO_2 oxide (figure 4).

Thus, carriers in the inversion layer of a MOSFET featuring high-k dielectrics feel a thicker but lower potential barrier than in SiO_2 devices [5]. Anyway, despite of the lower potential barrier, high-k insulator MOSFETs outperform SiO_2 devices in terms of leakage [6][7].

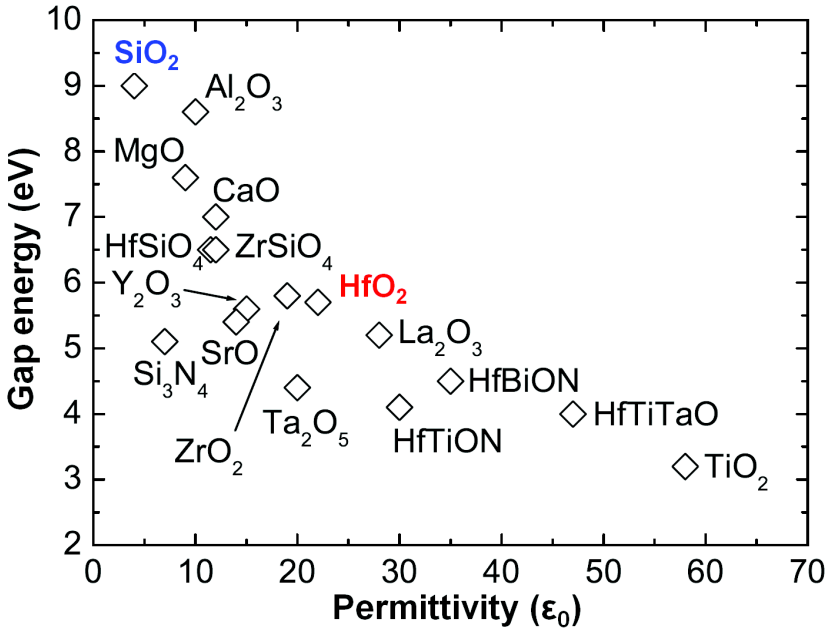


Figure 4: Band gap energy dielectrics as a function of the dielectric permittivity [8].

Threshold voltage adjust

Actually, the threshold voltage (VT) of MOSFETs is controlled by the adjustment of two parameters: the work functions of the gate (WFG) and of the substrate (WFS)($VT \sim WFG - WFS$).
In Poly-Si gate bulk MOSFETs, the work function of a polycrystalline-Silicon gate is adjusted by doping the gate p+ or n+ for p-channel and n-channel MOSFETs respectively. The channel work function is adjusted by appropriately doping the substrate to provide an acceptable work-function difference and charge depletion [9].
Beyond the 45nm node, the integration of high-k dielectrics and metal gates would be mandatory for high-performance and low-power advanced CMOS applications.
Indeed, introducing metal gates can:
(i) solve the problem of poly depletion in inversion. Poly-depletion effect adds an equivalent oxide thickness up to 0.5 nm to the gate stack, which is significant in front of the overall targetted EOT, around 1nm [2].
(ii) eliminate boron penetration from the p-doped polysilicon gate into the channel region in conventional CMOS.
(iii) avoid the high poly electrode resistance.

Selecting the metal gate material, the workfunction of the metal gate should be given a high consideration since it influences the MOSFET threshold voltage ($VT \sim WFG - WFS$).

A bandedge metal gate was reported to be the optimal choice for sub-45 nm high performance applications (about 4.2 eV for nMOS and 5.1 eV for pMOS) [10][11].
For conventional metal gate CMOS applications on Silicon, a p+ metal work function is required for the pMOS transistor. Whereas, an n+ metal work function is needed for the nMOS transistor. In order to satisfy the optimal n and pMOS threshold voltages, a dual metal gate solution would be ideal. But, it is difficult to identify, complicate and expensive to implement into devices [12]. Instead, a single midgap metal could be used. The VT could be therefore adjusted by suitable implants for n and p types MOSFETs.
Metal nitrides e.g. TiN are being considered as potential candidates for the mid-gap electrode due to their high thermal stability and compatibility with conventional CMOS processing [13]. Indeed, the Fermi level of the TiN gate (WFG$\sim$ 4.55-4.7 eV [14]) lies midway between the valence and conduction band edges of the Silicon, i.e., at midgap, assuming that the same gate material can be used for both p- and n-channel MOSFETs. In metal gate/high-k based MOSFETs, low threshold voltage is achieved by the incorporation of an interface dipole layer in the gate dielectric stack [15][16]. The interface dipole layer either increases, or decreases the effective gate work function by creating a localized electric field in the metal gate/high-k stack. The interface dipole layers are separately formed in n-channel and p-channel MOSFETs. LaOx and AlOx capping on high-k dielectrics have been shown to be effective in modulating the effective metal gate work function toward the n and p type band edge respectively [17][18][19][20].
The pMOS metal gate work function optimisation using AlOx capping is not sufficient to maintain low VT. The VT adjust can be tailored by accommodating the substrate work function. To this end, new materials e.g. $SiGe$ have been introduced in the channel of the pMOS. The large $SiGe$ valence-band offset with respect to Si allows the achievement of low pFET threshold voltage [21]. Moreover, the $SiGe$ is also an attractive channel material due to its high carrier mobility and compatibility with conventional CMOS processes [21]. The combination of high-k dielectric and $SiGe$ channel may present a practical device architecture to achieve high-performance and low-power application with low VT [8].

FDSOI structures

CMOS on thin-film Silicon-On-Insulator (SOI) is considered as a very attractive technology for further CMOS dimension downscaling and performance enhancement.

Figure 5 shows a cross-section of a SOI device. The advantages of SOI technology over conventional bulk Si CMOS come from its buried oxide layer (commonly called BOX). They consist of:
(i) lateral and vertical dielectric isolation providing reduced parasitic capacitances and leakage currents when compared to junction isolation [22],
(ii) thinned films and dielectric isolation offering tighter transistor packing density and simplified processing [23],
(iii) SOI devices yield improved switching speed and reduced power consumption. The operating speed is also improved since the isolated channel from substrate bias prevents the increase in a threshold voltage of stacked SOI transistors [23].

We distinguish between two types of SOI transistors. If the Silicon film (typically 100 nm or more) on the BOX layer is thicker than the body depletion region depth, the film is partially depleted (PD) SOI. This technology is called partially depleted (PD) SOI. However, if the

Silicon film thickness is thin enough (typically 50 nm or less) or the body doping concentration is low enough, the ultra thin film is fully depleted (FD). The obtained device is called fully depleted (FD) SOI. FD SOI transistors have more advantages than PD SOI transistors in terms of extremely low sub-threshold swing (<65 mV/decade), no floating-body effects, and low threshold voltage variation with temperature (2-3 times less). Moreover, undoped or very slightly doped UTB devices minimize impurity scattering and reduce threshold voltage variation resulting from random dopant fluctuation [23].

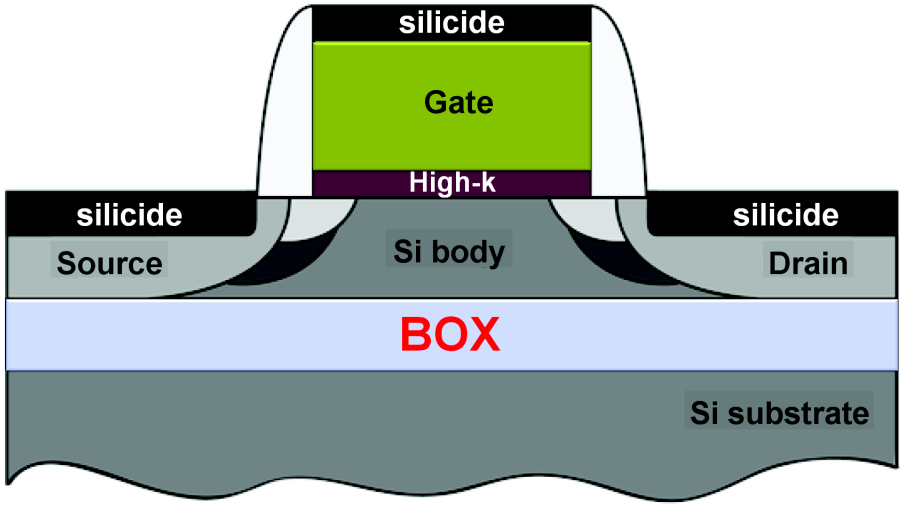


Figure 5: Cross-section of a SOI MOSFET.

Purpose of this thesis

To reduce the high bulk pMOS threshold voltage, strained Silicon Germanium on Silicon buffer layer has been successfully introduced in the 32-28nm industrial bulk process [21][24]. The threshold voltage reduction is achieved by narrowing the channel band gap on the valence band side. For this reason, recently $SiGe$ has been integrated also in the body of FDSOI pFETs [25].
Nevertheless, $SiGe$ incorporation in pMOS transistors generates problems. One of the problematics is that the simulation model for pure Si is not valid for $SiGe$ devices modeling. Moreover, before this thesis, electrical parameters (threshold voltage, flat band voltage (VFB) and EOT) were extracted using the extraction model on pure Si [26]. Figure 6 compares the measured capacitance versus gate voltage of the $SiGe$ bulk pMOSFET to the obtained curve using the extraction model on pure Si. It is clear from this figure that the extraction model is not relevant for $SiGe$ devices.
Another issue is to maintain good threshold voltage centering when introducing $SiGe$ in the pMOS. Figure 7 illustrates published reports on threshold voltage (VT) shift as a function of the Ge concentration. In this figure, data for both bulk and FDSOI pFETs are reported. Unexplained large discrepancy of VT shift is noticed making accurate VT centering very problematic. This justifies the investigation and results presented all along the manuscript.

The purpose of this thesis is to provide better insight on these issues. The first challenge is to find which simulation model should be used to predict the gate capacitance accurately. Furthermore, the problem is to find out how electrical parameters (threshold voltage, flat band voltage (VFB) and EOT) will be extracted when introducing $SiGe$ in the pMOS. The second problem is to understand the Ge impact on VT, VFB and EOT in $Si_{1-x}Ge_x$ pMOS for better VT contol.

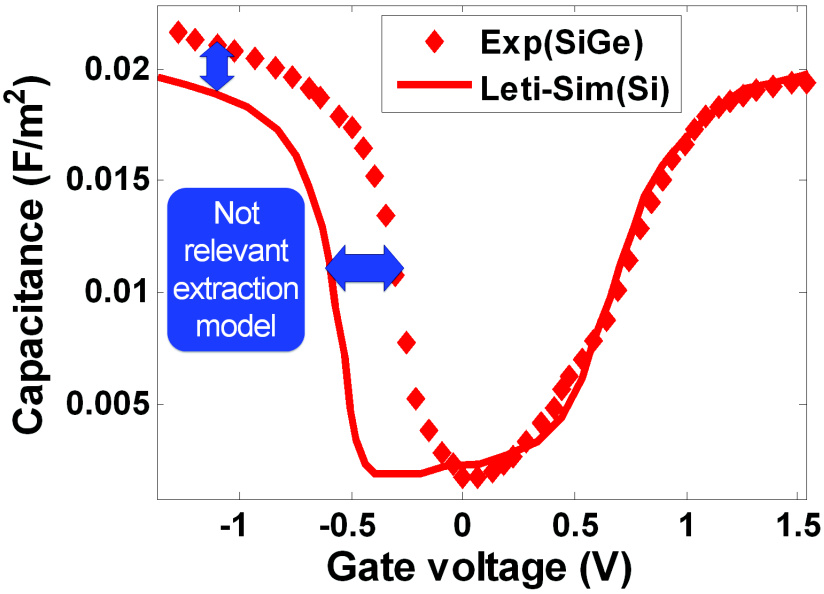


Figure 6: Measured (symbol) $SiGe$ bulk pMOSFET capacitance versus gate voltage compared to the obtained curve using the extraction model on pure Si (line) [26].

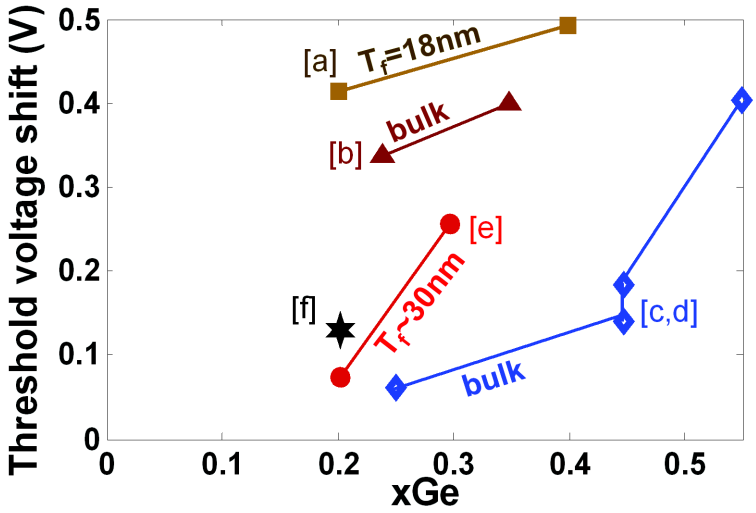


Figure 7: Published data of VT shift for $SiGe$ pMOS as a function of the Ge content.(References: [a]: [27]; [b]: [28]; [c]: [29]; [d]: [30]; [e]: [31]; [f]: [32].)

Organization of the thesis

The core of this document includes 4 chapters. The basic background of ideal and real MOS capacitors are presented in chapter 1. In this chapter, UTOXPP Poisson-Schrödinger simulation results are also validated. Chapter 2 focuses on strained $SiGe/Si$ heterostructure band structure modeling. This chapter discusses the theoretical impact of the $SiGe$ incorporation on the C-V characteristic. In chapter 3, we propose simple methods to extract VT, VFB and EOT parameters in $Si_{1-x}Ge_x$ pMOS. The extraction methods are first validated by simulations and then applied to C-V measurements. An investigation of the Ge integration electric impact in both pMOS bulk and FDSOI technologies is explored in chapter 4. In this chapter, evaluation of the role of Germanium on pMOS gate stack parameters (Effective work function and Equivalent oxide thickness) is presented. Finally, this document is finalized by conclusions and suggestions for future work.

Chapter 1

MOS capacitor C-V characteristic : basic principles and simulation

Contents

1.1 Introduction

Capacitance-voltage (C-V) characteristic offers a wealth of device and process information, including bulk and interface charges. It is commonly used for extracting common MOS device parameters such as oxide capacitance, oxide thickness, doping density, flat band voltage, threshold voltage, metal-semiconductor work function difference, etc..
This chapter will review basic principles of ideal and real MOS capacitors allowing threshold voltage and flat band voltage definition. Effects of oxide charges and interface traps on the C-V response will be investigated and testing C-V configuration will be explored.
In this thesis, C-V simulations have been performed using UTOXPP Poisson-Schrödinger solver. The second section of this chapter introduces the Poisson-Schrödinger solver and its enhancements implemented in UTOXPP simulator. The MOS-capacitor simulation results will be compared to the measured C-V characteristic in order to validate the C-V simulation model.

1.2 Basic principles of MOS capacitor

Before characterizing electrically the real MOS device by considering the defects contained in the oxide, at first, the ideal MOS structure will be studied. This section adresses the basic principles of MOS capacitor. The first part exposes the different MOS operation gate bias modes. The second part assesses the oxide defects and interface traps impact on the C-V characteristic and the flat band voltage in real MOS capacitor.

1.2.1 Ideal MOS capacitor

The metal-oxide-semiconductor (MOS) capacitor is the core of the MOS technology. Figure 1.1 presents a schematic MOS transistor of the actual C28nm node. In the z direction (perpendicular to the oxide/substrate interface), the charge concentration in the channel is modulated by a MOS capacitance between the semiconductor substrate and gate electrode located above an oxide layer. A voltage drop across the oxide induces a conducting channel between the source and drain contacts via the field effect.

The MOS structure is called ideal if the following two conditions are met:
(a) The work function of metal (WFM) and work function of semiconductor (WFS) are equal (WFM=WFS) when no voltage applied to the structure.
(b) Both the oxide and oxide/semiconductor interface are assumed to be free of charges and defect states. So, the electric field is zero everywhere in the absence of any applied voltage.
Depending on the applied gate voltage, the carrier concentration is changed due to the relative position of Fermi level versus conduction and valence bande edge. So, MOS capacitance will also vary with the applied gate to substrate voltage. In general, MOS capacitor operates at three different bias conditions. The three modes of operation, accumulation, depletion and inversion are represented by the behaviour of the capacitance with the gate voltage variation (C-V) (figure 1.2). The accumulation, flat bands, depletion, threshold voltage and inversion MOS regimes will now briefly be discussed for the case of the Si n-MOSFET ($T_{SiO2} = 2nm, N_A = 10^{17} cm^{-3}$).

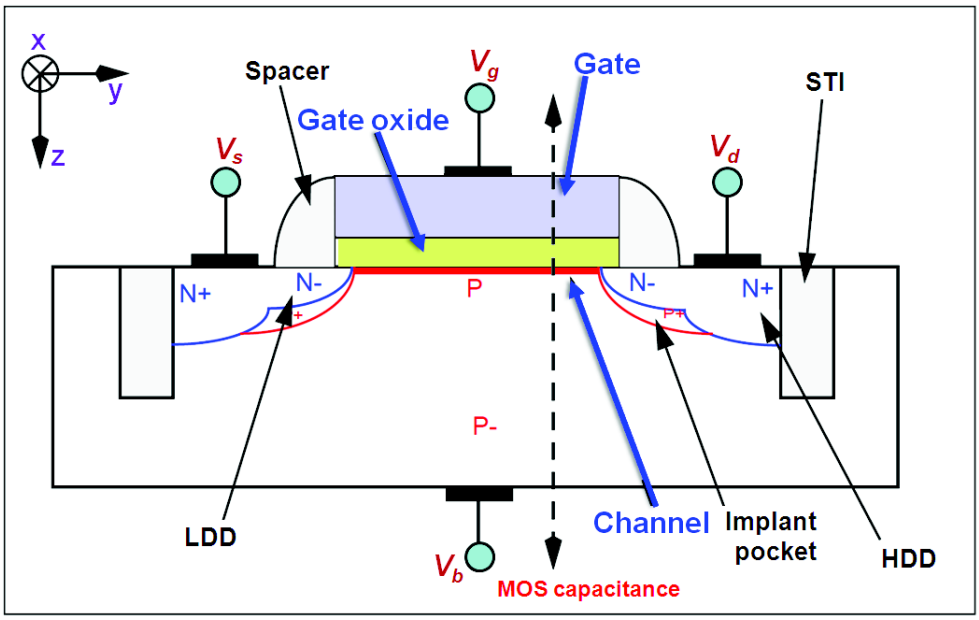


Figure 1.1: Schematic MOS transistor of the actual C28nm node.

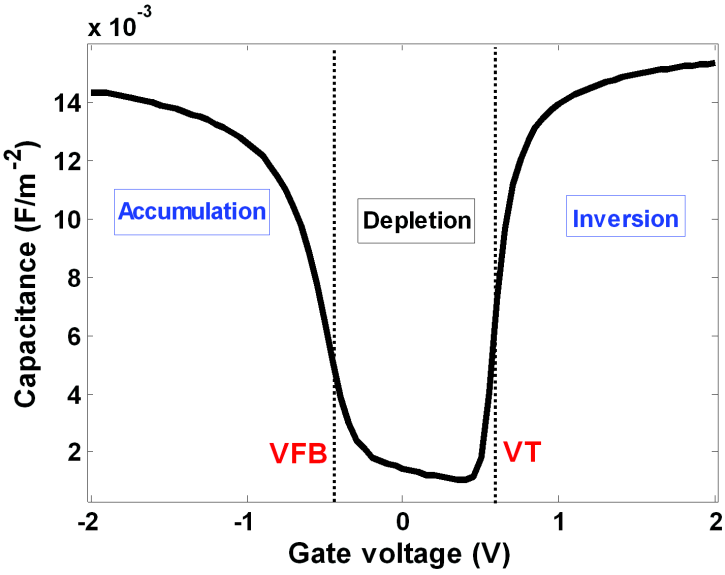


Figure 1.2: Simulated C-V characteristic of the Si n-MOSFET ($T_{SiO2} = 2nm, N_A = 10^{17}cm^{-3}$) showing the accumulation, depletion and inversion regimes.

1.2.1.1 Accumulation region

Figure 1.3 shows the conduction and valence bands bending, the Fermi level and the carrier concentration as a function of the distance along the z direction. When a negative voltage V_g is applied to the gate terminal of the MOS structure, the metal part becomes negatively charged and the semiconductor part becomes positively charged. Then, there occurs an internal electric field in the upwards direction from semiconductor to metal. This electric field piles up holes of

p-type semiconductor to the semiconductor/oxide interface, where an accumulation region of holes is obtained. The change in the free carrier concentration at the interface also affects the bands curve of the Si at the interface as shown in Figure 1.3.

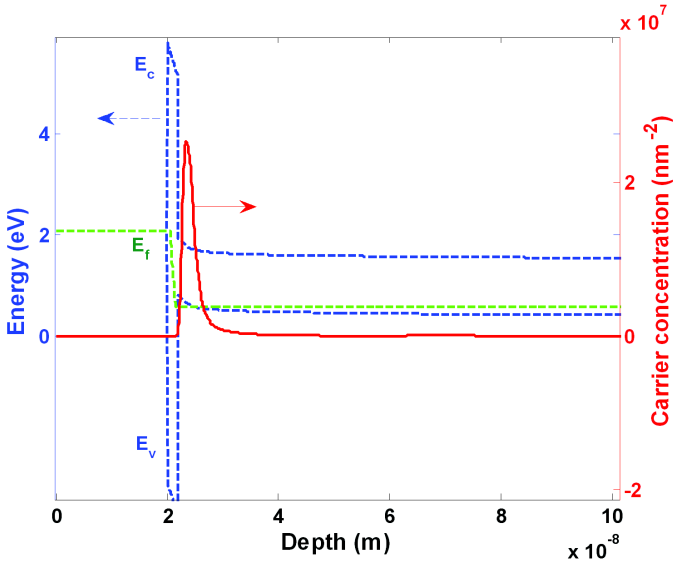


Figure 1.3: Energy bands structure and carrier concentration profile in the accumulation region.

1.2.1.2 Flat bands

The energy bands and the carrier concentration are plotted in the figure 1.4 as a function of the distance along the z direction. At $Vg = -0.47V$, the total charge in the MOS structure is zero. This corresponding applied gate voltage is called 'flat band voltage' (VFB).

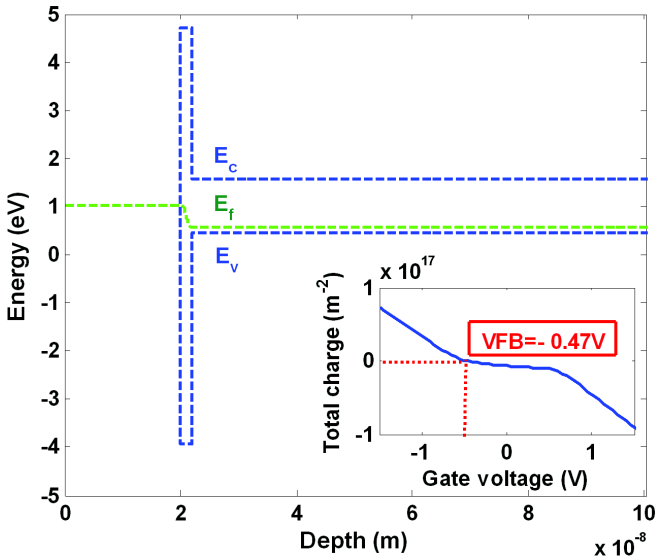


Figure 1.4: Energy bands structure in the Flat band voltage condition.

1.2.1.3 Depletion region

Figure 1.5 presents the energy bands structure and carrier concentration in the depletion regime. When a gate voltage $V_g > VFB$ (slightly positive) is applied to metal terminal of MOS structure, the metal part becomes positively charged and the semiconductor part becomes negatively charged. Under the influence of the electric field holes at the interface of semiconductor are pushed towards the bulk Silicon. So, majority carrier hole density decreases at the oxide/semiconductor interface. This surface region is the depletion region where only ionized acceptor atoms remain. Thus, the charge depletion is limited by the Si dopant concentration.

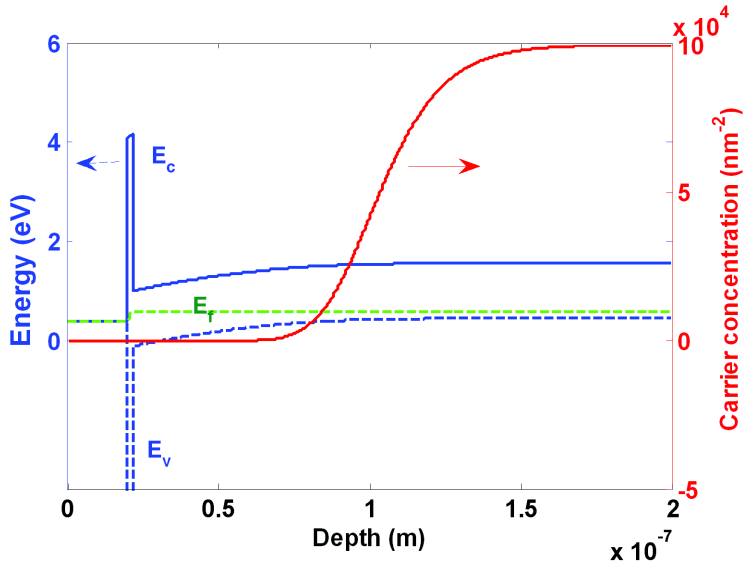


Figure 1.5: Energy bands structure and carrier concentration profile in the depletion region.

1.2.1.4 Threshold voltage

The turn-on region for a MOSFET corresponds to the inversion region on its C-V plot (figure 1.2). When a MOSFET is turned on, the channel formed corresponds to strong generation of inversion charges. It is these inversion charges that conduct current between source and drain electrodes. The threshold voltage (VT) can be commonly defined as the point on the C-V curve for which the electron concentration at the semiconductor interface equals the hole concentration in the bulk. This curve point corresponds to the onset of strong inversion where the device begins to conduct. This parameter, which is fundamental for MOSFET modeling and characterization, has been given several definitions [33][34]. There exist numerous methods to extract the value of threshold voltage [35][36]. Various extractor circuits have also been proposed [37][38] to automatically measure this parameter. But, it may be essentially understood as the gate voltage value at which the transition between weak and strong inversion takes place in the MOSFET channel. Different available methods have been reviewed and scrutinized in the litterature [39][40][41][42][43].
In this thesis, we have used three methods to extract the threshold voltage of the bulk MOSFET and FDSOI transistors:
(i) The first method consists of extracting the threshold voltage in MOS transistors biased in the

linear region. This extraction method is based on the measurement of the static drain current versus gate voltage characteristics. The VT extraction is done using low drain voltages (Vd) so that the device operates in the linear region [43][35][44]. VT is defined as the gate voltage corresponding to a certain predefined practical constant drain current (Icc). This method is widely used in industry because of its simplicity. The threshold voltage can be determined quickly with only one voltage measurement [43].
(ii) The threshold voltage is also extracted from the maximum of the gate capacitance derivative with respect to gate voltage (see chapter 3). In this method VT is defined from the commonly known "maximum of the transconductance derivative" method [45]. It is a conceptually correct method based on the transconductance (g_m) change [46] and consists of measuring the variation in g_m with respect to gate voltage and determining the maximum of this variation.
(iii) The threshold voltage is defined at 40% of $C^{max,inv}$, the gate capacitance maximum value at strong inversion (see chapter 4).

1.2.1.5 Inversion region

Figure 1.6 illustrates the energy bands structure and carrier concentration in the inversion regime. When a positive voltage V_g higher than the threshold voltage (VT) is applied, minority carrier electrons in the bulk of p-type Silicon are accumulated at the semiconductor surface under strong electric field. In this case electron concentration at the surface becomes higher than the hole concentration in the bulk Si. As a result, conduction and valence bands bend down at the semiconductor/oxide interface.

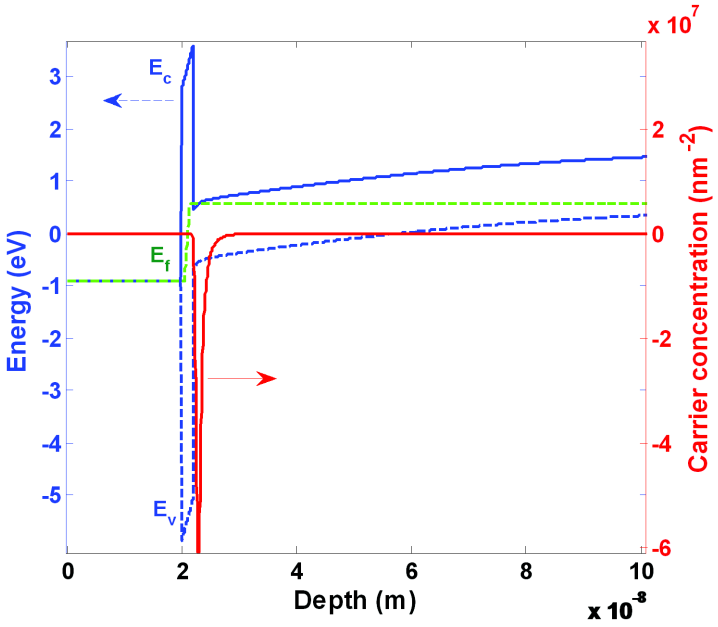


Figure 1.6: Energy bands structure and carrier concentration profile in the inversion region.

1.2.2 Real (Non-ideal) MOS capacitor

In the theoretical treatment of an ideal MOS capacitor, the metal work function (WFM) and semiconductor work function (WFS) are equal in the absence of an applied voltage (V_g=0). Moreover, oxide layers are treated as ideal insulators, where there are no traps or states at oxide/semiconductor interface. However, an ideal MOS device does not agree with experimental results. Actually, in real MOS devices, the metal and semiconductor work functions are different at (V_g=0). Besides, the oxide/semiconductor interface and bulk oxide are far from beeing electrically neutral. Some impurities or defects can be incorporated into the oxide during oxide growth or subsequent fabrication process steps. This results in the dielectric contamination with various types of charges and traps. The presence of oxide defects can strongly affect the threshold voltage and flat band voltage. As a result, the C-V characteristic in real MOS capacitor may be modified.
Four different types of oxide charges can be identified in real MOS devices [47]. These are shown schematically in figure 1.7. These are: oxide trapped charges (Q_{ot}), mobile ionic charges in the oxide (Q_m), interface fixed oxide charges (Q_f) and interface-trapped charges (Q_{it}). Each type of oxide charge can cause a shift (Q_{ot}, Q_m and Q_f) or deformation (Q_{it}) of the C-V curve.

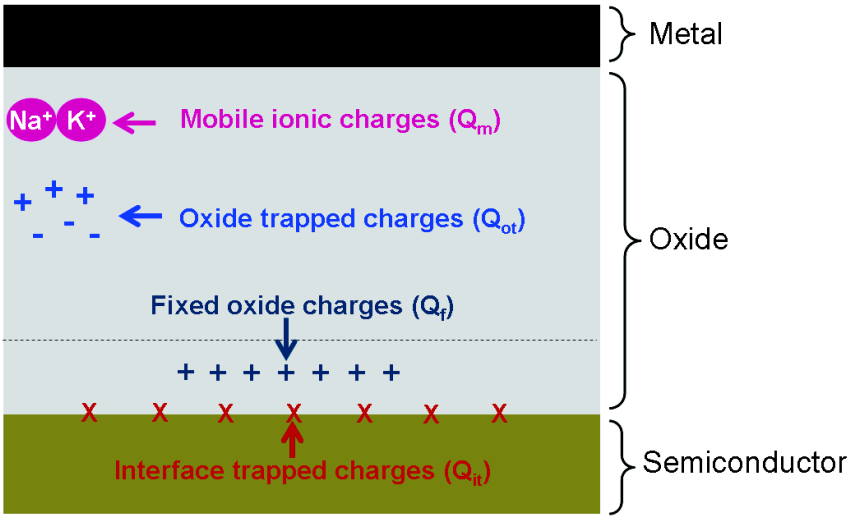


Figure 1.7: Distribution of charges inside the gate-oxide.

In this section, the main defects commonly observed in insulators will be briefly described. Their impact on the C-V characteristic will also be assessed.

1.2.2.1 Effect of the bulk oxide charges

The bulk oxide charges regroups:
(a) Mobile ionic charges which are due to alkali metal ions in the oxide such as Li^+, Na^+ and K^+ [47]. These impurities cause reliability problems under high temperature and high voltage operations. So, they can migrate from an interface to another under high bias-temperature conditions.

(b) The oxide fixed charges which may be positive or negative due to defects in the bulk of the oxide. Trapping may result from ionizing radiation, avalanche injection, or other similar processes [47].
These defects may be distributed unevenly in the bulk oxide. In that case, their charge density $\rho(z)$ varies with distance. The origin of the z-axis is taken at the metal/oxide interface as shown in figure 1.8. At the flat band condition, using Gauss's law and the superposition theorem, the effects of all oxide layers comprised between zero and T_{ox} are added. So, the gate voltage shift ΔVFB^{BOC}, which is necessary to ensure a flat band condition at the oxide/semiconductor interface, is found to be:

$$\Delta VFB^{BOC} = -\frac{1}{\varepsilon_0}\int_0^{T_{ox}} \rho(z) \int_0^{z} \frac{du}{\varepsilon_{ox}(u)} dz \tag{1.1}$$

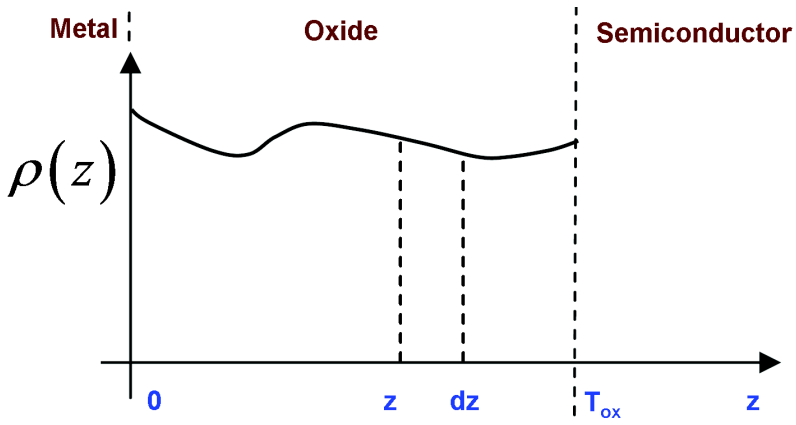


Figure 1.8: Oxide charges distribution as a function of distance.

The effect of each charge layer depends on its distance from the metal/oxide interface as given in equation 1.1. A layer has no effect if it is located at the metal/oxide interface (z=0) and has a maximum effect if it is located at the oxide/semiconductor interface.

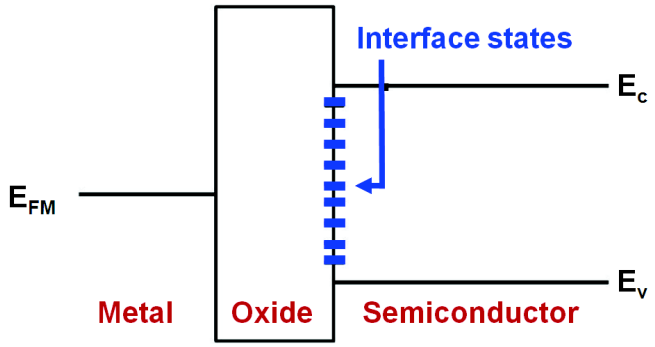
1.2.2.2 Effect of interface fixed oxide charges

Fixed oxide charges are positive or negative charges located near the oxide/semiconductor interface. They are due primarily to structural defects (ionized Silicon) in the oxide layer [48]. The density of this charge depends on oxidation process and temperature. Fixed oxide charge does not move and exchange charge with the underlying semiconductor. It is also insensitive to the applied electric field variation.
Fixed charges dispersed randomly across the oxide/semiconductor interface may cause a gate voltage shift of the real C–V curve with respect to the ideal one. The gate voltage shift ΔVFB^{FOC} is given by:

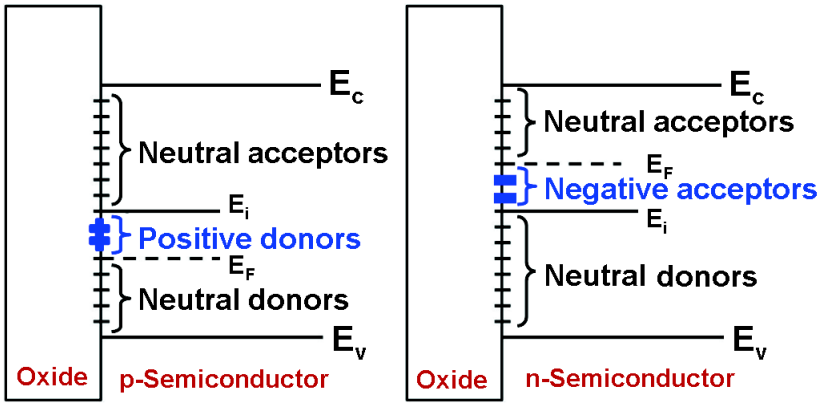
$$\Delta VFB^{FOC} = -\frac{Q_f}{\varepsilon_{SiO_2}\varepsilon_0} EOT \tag{1.2}$$

1.2.2.3 Effect of interface trapped charges

Interface trapped charges, also called as the interface states or traps are positive or negative charges located at or very close to the semiconductor/oxide interface. They are attributed to dangling bonds and other native defects at this interface. Unlike fixed charge or trapped charge, interface trapped charge is in electrical communication with the semiconductor. Indeed, they are distributed along the bandgap of the semiconductor (figure 1.9.a). Electrons or holes get trapped in these states and act like charges at the interface. The probability that an electron or hole occupies a given interface state depends on its energetic location relative to the Fermi energy.



(a)



(b)

Figure 1.9: (a) MOS structure Energy band diagram, depicting the distribution of interface states along the bandgap of the semiconductor at the semiconductor/oxide interface. (b) Schematic presentation of donors and acceptors distribution in the gap of p and n-type semiconductors in flat band condition.

Presumably, every interface has both kind of states, donor states and acceptor states. An acceptor state is neutral when it is not occupied. It becomes negatively charged when it captures an electron. However, a donor state is neutral when it traps an electron (or emits a hole). It becomes positively charged when it is not occupied. The sum of these states is the equivalent interface states density (D_{it}) distribution with a characteristic energy level called the charge-neutrality level E_i. The interface states which exist in the upper half of the semiconductor

band-gap (E> E_i) are acceptor states. Whereas, the interface states which exist in the lower half of the band-gap are donor states (E< E_i). Indeed, interface states are occupied only when these are below the Fermi level. The charge of the interface states is then a function of the substrate doping type and gate voltage applied across the MOS capacitor. Figure 1.9.b schematizes the interface traps distribution in the gap of p and n-type semiconductors in flat band condition. This figure shows that the trapped charges in the interface states are negative for the n-type substrate and positive in the case of p-type substrate.
The MOS structure bias variation induces the Fermi level change. Therefore, the interface states may be charged and neutralized during the C-V measurement (figure 1.9.b). These charges cause a flat band voltage shift ΔVFB^{IT} expressed as:

$$\Delta VFB^{IT} = -\frac{Q_{it}(\Psi_s)}{\varepsilon_{SiO_2}\varepsilon_0} EOT \tag{1.3}$$

1.2.2.4 Flat band voltage expression

Here, we describe first the flat band voltage expression in real MOS devices introducing mono-layer oxide. Then, the VFB expression will be explored for bilayer insulator. Given VFB expressions will be simplified under the assumption of a contant oxide charge distribution.

For a practical MOS structure integrating one oxide layer only, there exist oxide charges, interface traps and dipoles present at each gate stack interface. As shown in the subsection 1.2.2.1, defects are distributed unevenly in the bulk oxide. Whereas, interface fixed charges and interface traps are located close to the oxide/semiconductor interface. In order to express the flat band voltage in actual MOS devices, we have taken into account (see figure 1.10.(A)):
(i) the metal and semiconductor work functions difference ($WMS = WFM - WFS$). WFS is the Fermi level in the semiconductor at flat band condition. In FDSOI devices, the thin body is beeing undoped so there is neither depletion nor accumulation regimes. Therefore, it seems difficult to define VFB. Nevertheless, the VFB definition at zero charges (see subsection 1.2.1.2) can be conserved for FDSOI transistors.
(ii) the oxide charges density ρ_{ox} in the bulk of the oxide.
(iii) the interface oxide charges $Q_{f,ox}$.
(iv) the interface traps Q_{it}.
(v) the dipoles Δ_i at each oxide metal gate stack interface "i".

The flat band voltage can be expressed as a function of these quantities and oxide thickness (T_{ox}) as follows [49]:

$$\begin{aligned} VFB = WMS - \frac{1}{\varepsilon_{ox}\varepsilon_0}\left(\int_0^{T_{ox}} Q_{f,ox}\delta(T_{ox})zdz + \int_0^{T_{ox}} Q_{it}(\Psi_s)\delta(T_{ox})zdz\right) \\ -\frac{1}{\varepsilon_0}\int_0^{T_{ox}} \rho(z)\int_0^{z}\frac{du}{\varepsilon_{ox}(u)}dz + \sum_i \Delta_i \end{aligned} \tag{1.4}$$

where δ is the delta function ($\delta(z = T_{ox}) = 1$ and $\delta(z \neq T_{ox}) = 0$).
The formula 1.4 is valid for any charge distribution in the oxide. For a constant oxide charge density, it becomes:

$$VFB = WMS - \frac{Q_{f,ox} + Q_{it}(\Psi_s)}{\varepsilon_{SiO_2}\varepsilon_0} EOT - \frac{\rho_{ox} T_{ox}^2}{2\varepsilon_{ox}\varepsilon_0} + \sum_i \Delta_i \tag{1.5}$$

The oxide fixed charge is constant when appling an electric field whereas Q_{it} is a function of the surface potential (Ψ_s).

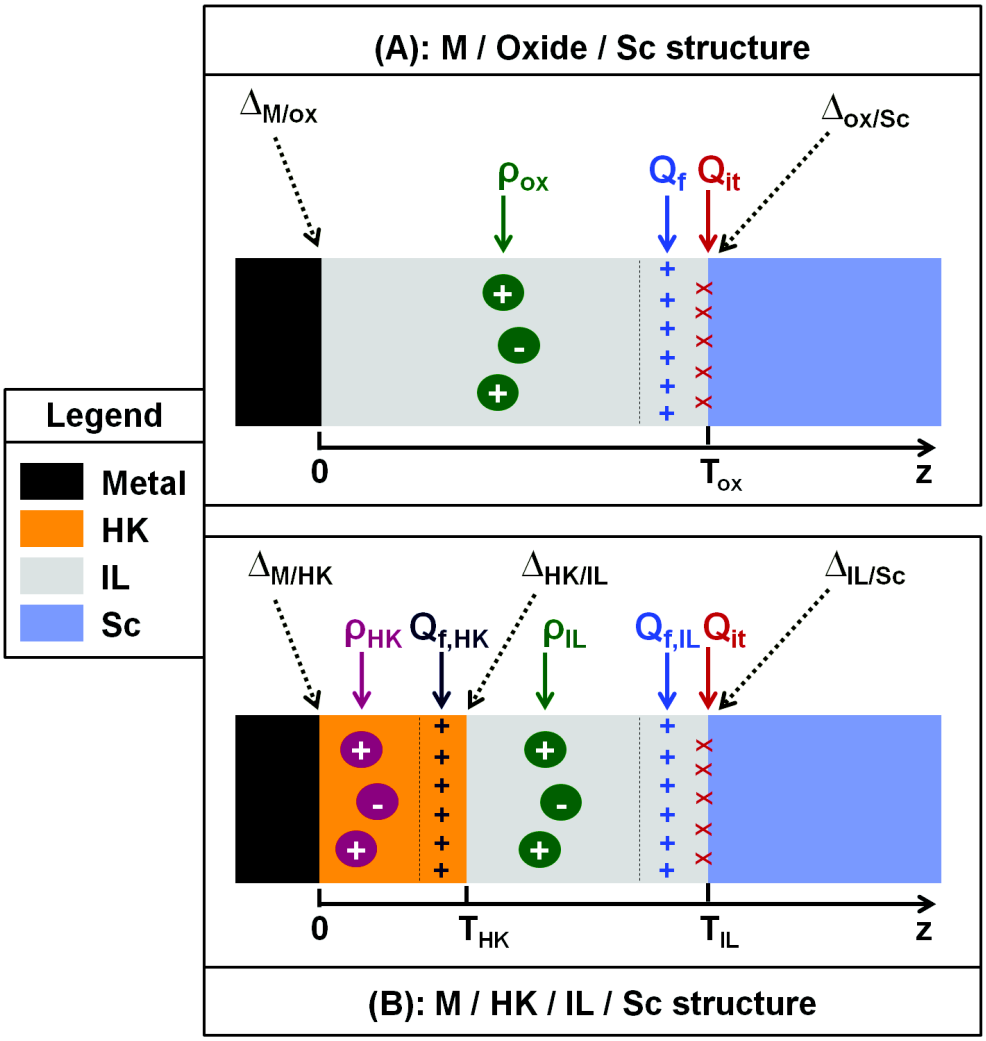


Figure 1.10: MOS capacitor cross sections. (A) metal gate (M) on oxide only and (B) metal gate on high-k (HK) and interfacial layer (IL). The various charges and dipoles at gate stack interfaces are indicated.

For two layers insulators (figure 1.10.(B)), consisting of a gate, a high-k dielectric (HK), an interfacial oxide (IL) and a substrate (Sc), the flat band voltage is written as:

$$VFB = WMS + \Delta VFB(HK) + \Delta VFB(IL) + \sum_i \Delta_i \tag{1.6}$$

where

$$\sum_i \Delta_i = \Delta_{M/HK} + \Delta_{HK/IL} + \Delta_{IL/Sc} \tag{1.7}$$

In equation 1.6, $\Delta VFB(HK)$ is the VFB shift due to the fixed charge density $Q_{f,HK}$ at the HK/IL interface ($\Delta^{Ch}_{HK/IL}$) and charge density $\rho_{IL}(z)$ in the high-k insulator (Δ^{Ch}_{HK}). The $\Delta VFB(HK)$ is given by:

$$\Delta VFB(HK) = \Delta^{Ch}_{HK/IL} + \Delta^{Ch}_{HK} = -\frac{T_{HK}}{\varepsilon_{HK}\varepsilon_0} Q_{f,HK} - \frac{1}{\varepsilon_{HK}\varepsilon_0} \int_0^{T_{HK}} \rho_{HK}(z) z dz \tag{1.8}$$

Tne $\Delta VFB(IL)$ is the VFB shift caused by: the interface traps Q_{it} (ΔVFB^{IT}), the fixed charge density $Q_{f,IL}$ at the IL/semiconductor interface ($\Delta^{Ch}_{SiGe/IL}$) and charge density $\rho_{IL}(z)$ in the IL (Δ^{Ch}_{IL}) (figure 1.10.(B)). The $\Delta VFB(IL)$ expression is:

$$\begin{aligned} \Delta VFB(IL) = \Delta VFB^{IT} + \Delta^{Ch}_{SiGe/IL} + \Delta^{Ch}_{IL} = & -\frac{Q_{it(\Psi_s)} + Q_{f,IL}}{\varepsilon_{SiO_2}\varepsilon_0} EOT \\ & - \int_{T_{HK}}^{T_{HK}+T_{IL}} \rho_{IL}(z) \left(\frac{T_{HK}}{\varepsilon_{HK}\varepsilon_0} + \frac{z - T_{HK}}{\varepsilon_{IL}\varepsilon_0} \right) dz \end{aligned} \tag{1.9}$$

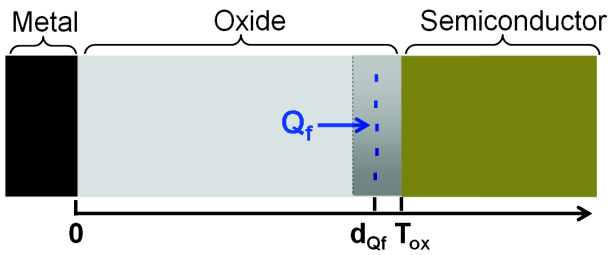
Under the assumption of a constant oxide charge distribusion, $\Delta VFB(HK)$ and $\Delta VFB(IL)$ VFB shifts become:

$$\begin{cases} \Delta VFB(HK) = -\dfrac{Q_{f,HK}}{\varepsilon_{HK}\varepsilon_0} T_{HK} - \dfrac{\rho_{HK}}{\varepsilon_{HK}\varepsilon_0} \dfrac{T^2_{HK}}{2} \\ \Delta VFB(IL) = -\dfrac{Q_{it(\Psi_s)} + Q_{f,IL}}{\varepsilon_{SiO_2}\varepsilon_0} EOT - \dfrac{\rho_{IL}}{\varepsilon_{IL}\varepsilon_0} \dfrac{T^2_{IL}}{2} + \dfrac{\rho_{IL}}{\varepsilon_{HK}\varepsilon_0} T_{IL} T_{HK} \end{cases} \tag{1.10}$$

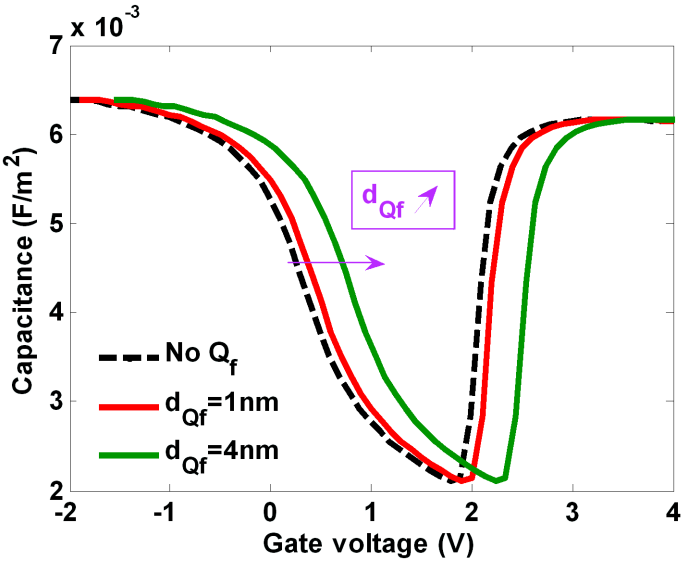
1.2.2.5 Electric effect of oxide charges

As shown in subsection 1.2.2.2, fixed charge in the oxide induces a gate voltage shift of the measured C–V curve. A negative (or positive) fixed charge at the oxide/semiconductor interface shifts the flat band voltage by an amount which equals the charge divided by the oxide capacitance (equation 1.2). The shift decreases linearly as the position of the fixed charge relative to the gate electrode is reduced. It becomes zero if the charge is located at the metal/oxide

interface. Figure 1.11 illustrates the impact of oxide fixed charge on C-V characteristic using UTOXPP simulations. Clearly, the C-V plot including -5×10^{19}cm^{-3} oxide fixed charge peak is shifted toward more positive bias voltage in comparison to the ideal C-V curve (with no oxide fixed charge). Moreover, it is important to notice that the C-V shift is higher when the negative fixed charge peak position being far from the gate (400mV C-V shift versus 100mV) (figure 1.11.b).



(a)



(b)

Figure 1.11: (a) Simulated MOS structure. (b) Simulated C-V curves of the Si nMOSFET (EOT=5nm) considering an ideal SiO_2 oxide (dashed curve) and -5×10^{19}cm^{-3} oxide fixed charge peak at d_{Qf} position (solid curves).

Charge due to interface states also yields a shift in flat band voltage (see subsection 1.2.2.3). However, as the applied voltage is varied, the Fermi energy at the oxide/semiconductor interface changes. This Fermi energy level evolution affects the occupancy of the interface states. The presence of the surface trapped charges are observable in the measured C-V characteristic. So, a distortion and bump is appeared in the C-V plot (figure 1.12).

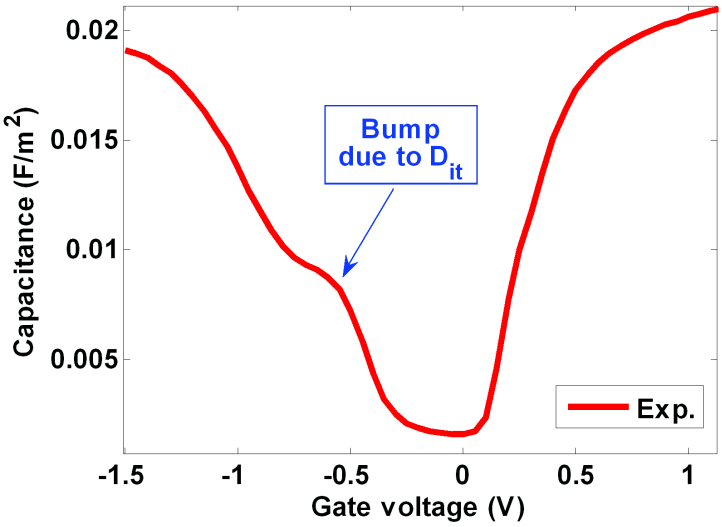


Figure 1.12: Distortion and bump of the measured *Si* nMOSFET C-V characteristic due to interface trapped charges.

1.2.3 Capacitance-voltage measurements

C-V testing is widely used to determine semiconductor parameters, particularly in MOS capacitor and MOSFET structures. C-V measurements can reveal for example oxide thickness, oxide charges, interface trap density [50][51], threshold voltage and flat band voltage.
The equivalent circuit of a MOSFET is shown in figure 1.13. In a real MOSFET there will also be parasitic capacitances between the gate and source/drain and between the substrate and source/drain. But, for a large area MOSFET, these are usually negligible. The total capacitance C is given by:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{sc} + C_{it}} \tag{1.11}$$

where C_{sc} is the semiconductor capacitance. C_{ox} and C_{it} being oxide and interface traps capacitances.

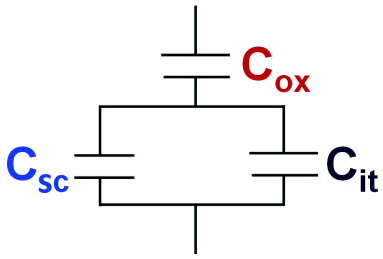
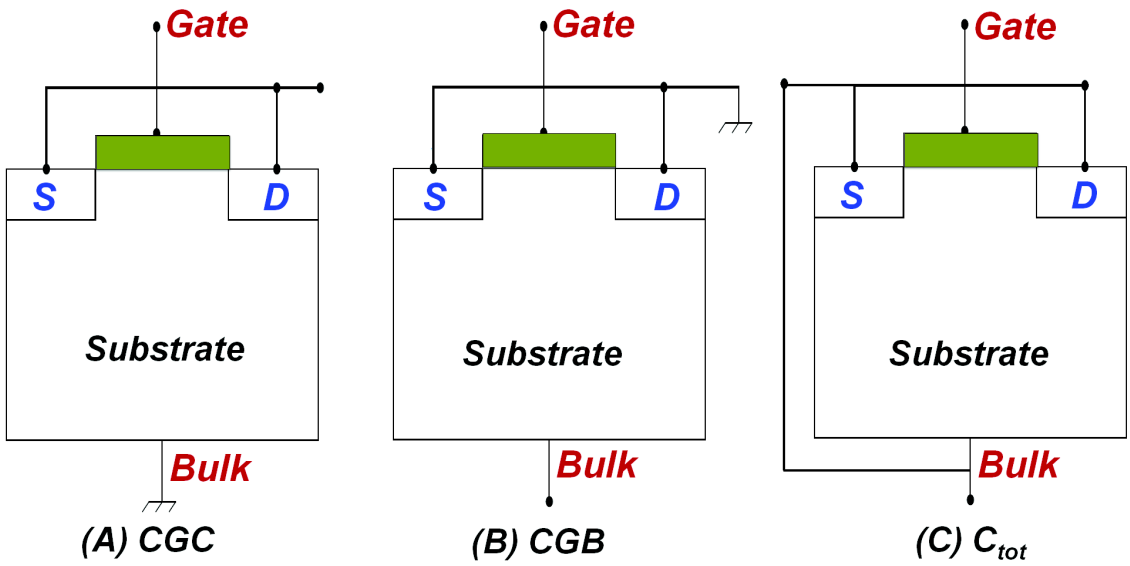
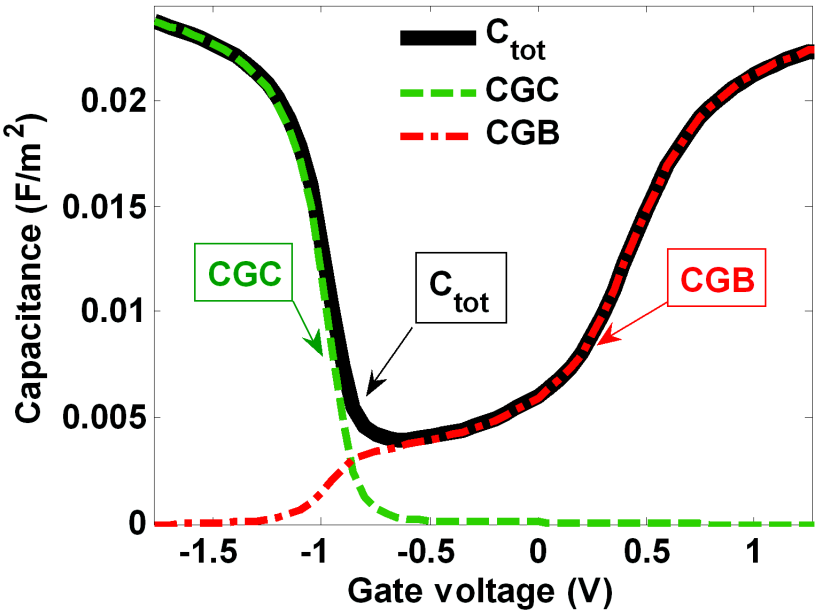


Figure 1.13: Equivalent circuit of a MOSFET. C_{ox}, C_{sc} and C_{it} are the dielectric, semiconductor and interface trap capacitances respectively.

Since the inversion charge is supplied by the source and drain and the depletion charge by the substrate, measurements of the inversion and depletion capacitances can be obtained separately. This is known as the split C-V technique [52][53]. Figure 1.14 reports the measurement configurations and examples of C-V measurement results of the *Si* pMOSFET.



(a)



(b)

Figure 1.14: (a) Measurement configurations for the gate-to-channel capacitance CGC (A), gate-to-bulk capacitance CGB (B) and total capacitance C_{tot} (C). (b) Measured CGC, CGB and C_{tot} characteristics for the *Si* pMOSFET.

In the gate-to-channel (CGC) configuration (figure 1.14.a(A)) the gate, drain and source are connected to the LCR meter while the bulk is tied to ground. This configuration measures the change in inversion charge with the applied voltage (figure 1.14.b):

$$CGC = \frac{\partial Q_{inv}}{\partial V_g} \tag{1.12}$$

The gate-to-bulk capacitance (CGB) is measured with the source and the drain terminals grounded (figure 1.14.a(B)). It approaches C_{ox} in accumulation and the series combination of C_{ox} and C_{dep} in depletion (figure 1.14.b).
The total capacitance C_{tot} (equation 1.11) is measured with the interconnected source, drain and bulk and gate connected to the LCR meter figure 1.14.b(C). The measured C_{tot} shows the inversion, depletion and accumulation regimes (figure 1.14.b).

1.3 MOS capacitance simulation

This section presents a validation of UTOXPP Poisson-Schrödinger simulation results by comparison to other solvers and literature results. In the second part, UTOXPP C-V simulations will be validated for Si nMOSFETs with Polysilicon and metal gate.

1.3.1 Modeling of quantum confinement

The trend toward smaller MOSFET devices with thinner gate oxide is resulting in the increasing importance of quantum mechanical effects. For actual device simulations, predicting these quantum effects requires solving the Schrödinger equation self-consistently with the Poisson equation. The coupled resolution of Poisson and Schrödinger equations computes the electrostatic potential and charge density distribution in the simulated structure for different gate voltages (V_g).
In this report, the electrostatic potential variation in the MOS structure is considered along the z direction (perpendicular to the oxide/substrate interface).

1.3.1.1 1D Poisson equation

The electrostatics within a MOS device are described by the Poisson equation [54]:

$$\frac{\partial}{\partial z}[\varepsilon_r(z)\frac{\partial}{\partial z}]\phi(z) = -\frac{q}{\varepsilon_0}\rho(z) \tag{1.13}$$

where q is the elementary electron charge, ε_r is the dielectric constant, ϕ is the electric potential and ρ is the charge density distribution. The dielectric constant $\varepsilon_r(z)$ depends to the relative material and z position.

The charge density $\rho(z)$ is decomposed into charge carrier densities of electrons $n(z)$ and holes $p(z)$ and the ionized dopant concentration of acceptor N_A and donator N_D atoms:

$$\rho(z) = p(z) + N_D(z) - n(z) - N_A(z) \tag{1.14}$$

1.3.1.2 1D Schrödinger equation

Within the effective mass approximation, for a particle of mass m under a potential $V(z)$, the one-dimensional, time independent Schrödinger equation is given by [54]:

$$-\frac{\hbar^2}{2}\frac{\partial}{\partial z}\left[\frac{1}{m_i(z)}\frac{\partial}{\partial z}\right]\psi_{i,v}(z) + V(z)\psi_{i,v}(z) = E^z_{i,v}\psi_{i,v}(z) \tag{1.15}$$

where m_i is the effective mass, $\hbar$ is the Planck constant h divided by 2π, $\psi_{i,v}$ is the wave function of the v-th subband of the i band, V is the potential energy determined by the Poisson equation resolution (1.13) and $E^z_{i,v}$ corresponds to the energy level.

The numerical resolution of the equation (1.15) computes the wave functions $\psi_{i,v}$ and eigenenergies $E^z_{i,v}$. The inversion layer electron density appearing in the 1D Poisson equation (1.14) is obtained by summing over all subbands to get [54]:

$$n(z) = \sum_{i,v}\frac{m^v_{xy}}{\pi\hbar^2}g_v k_B T \ln\left[1 + \exp\frac{E_F - E^z_{i,v}}{k_B T}\right]|\psi_{i,v}(z)|^2 \tag{1.16}$$

In (1.16), E_F is the Fermi level, k_B is the Boltzmann constant, T is the temperature, m^v_{xy} is the inplane effective mass of the v-th subband and g_i ($g_1 = 2$ for the Δ_2-band, and $g_2 = 4$ for the Δ_4-band) is the corresponding band degeneracy.

Thus, to calculate the charge density ρ given by (1.14) along the z direction in the MOS structure, the Shrödinger equation (1.15) should be numerically solved. To do so, the electrical potential is needed. It's determined by the Poisson equation solution (1.13). To this end, the charge density calculation is necessary. As a result, both Poisson and Shrödinger equations have common variables. That's why, these equations should be self consistently solved. The self-consistent calculation is carried out as described in the flow chart shown in Figure 1.15.

An initial classical solution of the Poisson equation in conjunction with the Fermi-Dirac distribution is given to the Schrödinger solver as an initial guess of the potential profile. Then, the carrier (electons and holes) concentration is derived from the obtained eigen energies and eigen wave functions. The second Poisson solver calculates the potential distribution with the knowledge of carrier concentration as a function of position.

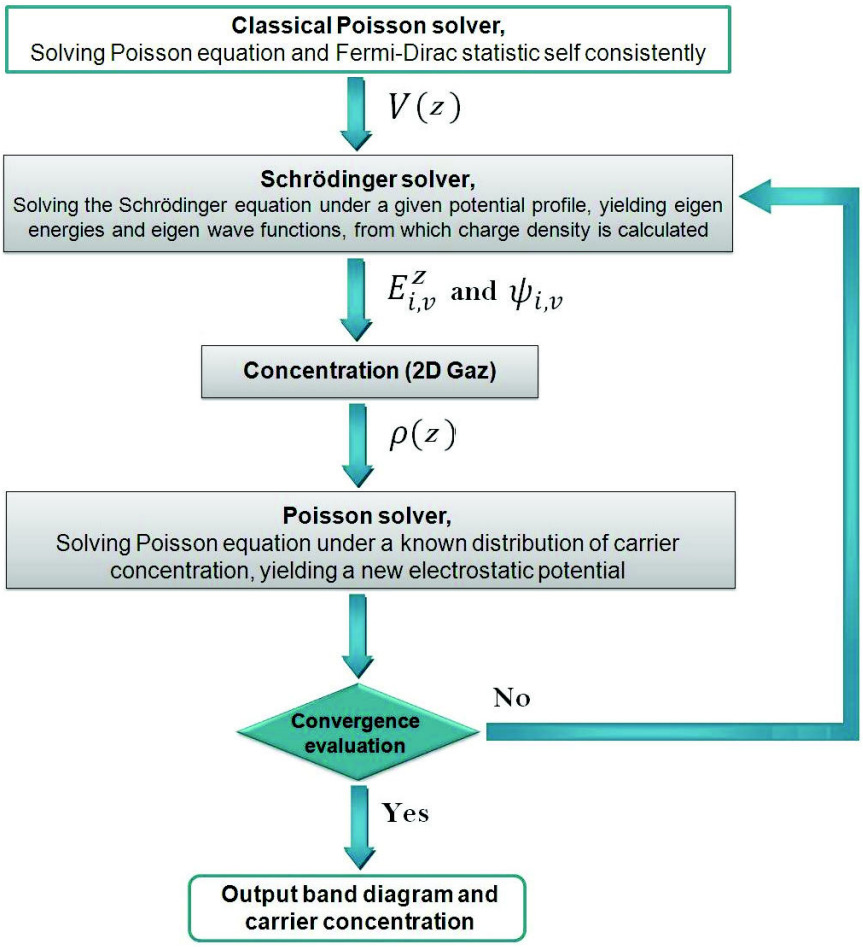


Figure 1.15: Flow chart of the Poisson-Schrödinger self-consistent solution.

1.3.1.3 Poisson-Schrödinger results validation

The simulated structure described in figure 1.16 consists of a TiN metal gate and a SiO_2 oxide on a p-doped Si substrate ($N_{Dop} = 10^{18}\text{cm}^{-3}$). Figure 1.17 compares the 1D self-consistent

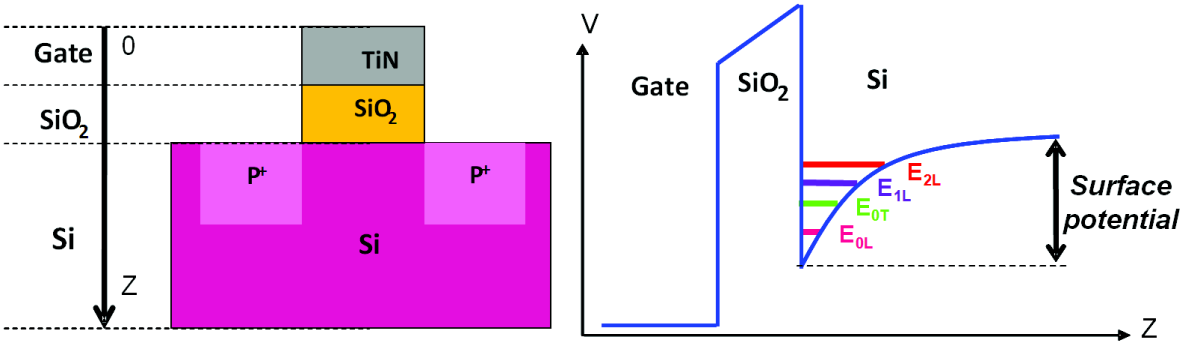


Figure 1.16: Simulated structure of the SiO_2/Si n-MOSFET.

Poisson-Schrödinger (PS) simulation results obtained using UTOXPP (PS.UTOXPP), the PS developed at Leti (PSL) and Synopsys Poisson-Schrödinger (PS.Synopsys). All simulations consider: the effective mass approximation (EMA), the wave functions penetration into the oxide and 20nm of quantum box. For the WFP, we used 3eV of oxide barrier height and $0.5m_0$ of effective mass.

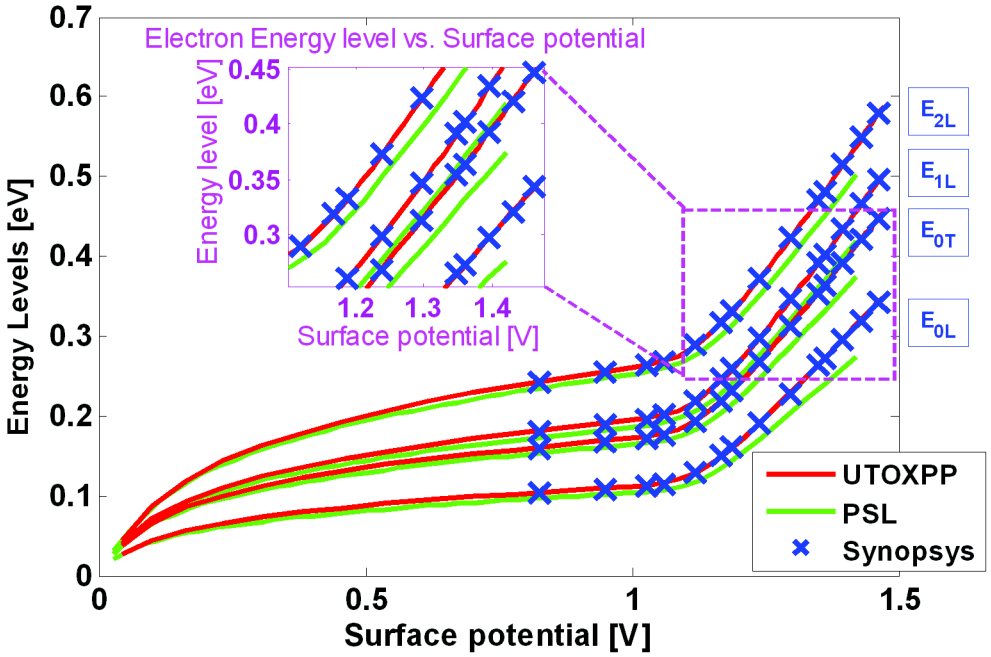


Figure 1.17: The first four energy levels obtained using PS.UTOXPP, PSL and PS.Synopsys for a different surface potentials in the inversion regime.

Very good agreement is noticed between the PS.UTOXPP and Synopsys results. Discrepancy is observed for PSL energy levels. Figure 1.18 reports the energy levels and electrostatic potential profile as a function of the z position at weak and strong inversion. The first two eigenenergies computed using UTOXPP are close to Synopsys results.

The PS.UTOXPP results were compared to data from literature for Si substrate doped at 5.10^{17}cm^{-3} in the inversion regime (see figure 1.19 and figure 1.20). Inspite of the global agreement observed for the different Si doping, it is recommended that the PS results comparison should be careful. Indeed, Poisson-Schrödinger results depend on different parameters such as the size of the quantum box (where the Poisson and Schrödinger equations are self-consistently solved), the number of energy levels taken into account to compute the charge comcentration and wave functions penetration into the oxide.

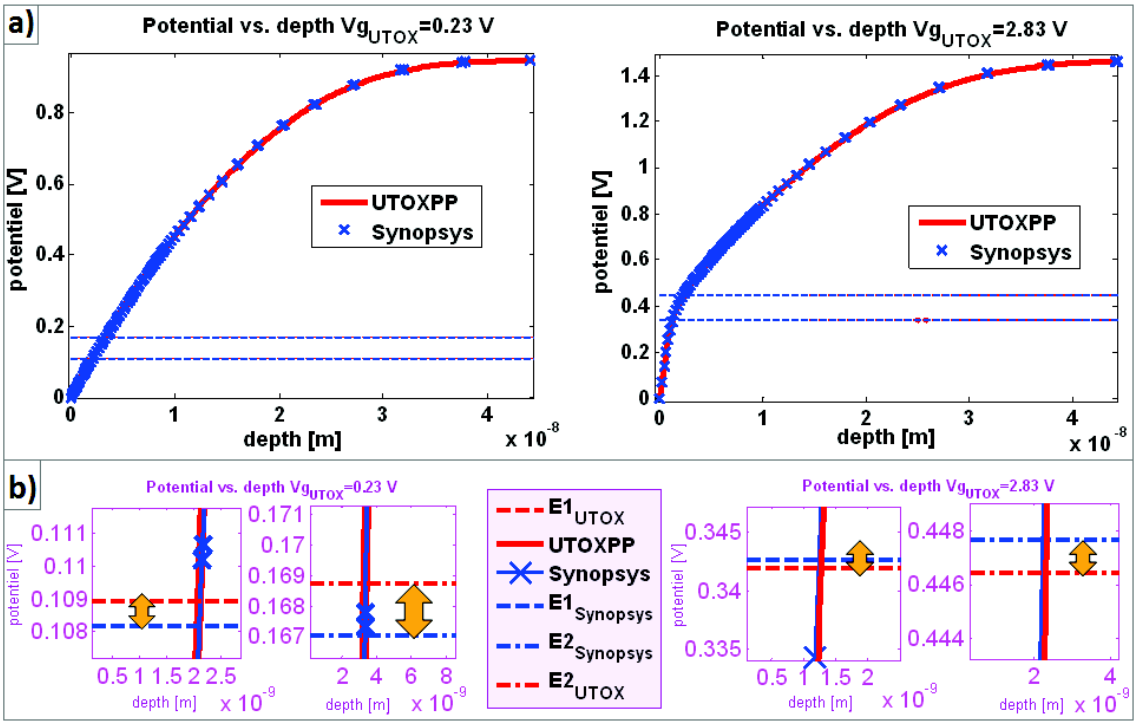


Figure 1.18: (a) The first two energy levels and electric potential profile as a function of the z position computed using the PS.UTOXPP and Synopsys at weak and strong inversion. (b) Zoom on the first two energy levels obtained using the PS.UTOXPP and Synopsys at weak and strong inversion.

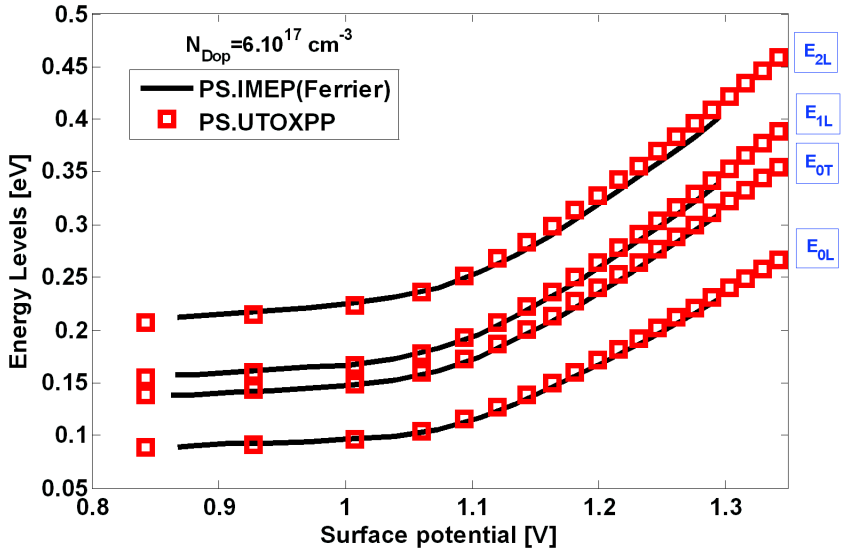


Figure 1.19: Comparison of the first four energy levels calculated using the PS.UTOXPP and PS.IMEP [55] for a different surface potentials in the inversion regime.

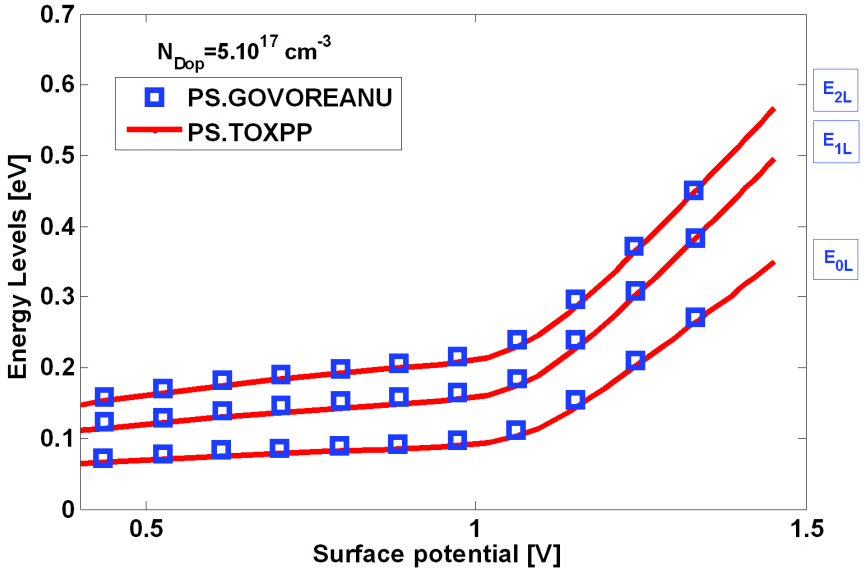


Figure 1.20: The first three Δ_2 subbands obtained using the PS.UTOXPP and PS.Govoreanu [56] for a different surface potentials in the inversion regime.

1.3.1.4 Analytical model analysis for SiO_2/Si bulk n-MOSFETs

Quantum confinement modeling at Silicon/oxide interface typically requires numerical self-consistent Poisson-Schrödinger simulations [57][58]. Analytical alternatives [59] such as the triangular well approximation and the variational approach are proposed to model the eigenenergies and wave functions. However, these analytical models are accurate enough to model only the charge located in the first subband [60]. This is satisfactory for charge and C-V modeling. Whereas, the tunneling current computation needs an accurate determination of the second subband which also have a significant contribution [60]. In order to calculate different energy levels with more precision, an improved triangular well approximation has been proposed by Ferrier et al. [55]. In this approach, the effective electric field for each subband is expressed by:

$$F_{i,v} = \frac{Q_{dep} + f_{i,v}.Q_{inv}}{\epsilon_s} \tag{1.17}$$

where ϵ_s is the substrate permitivity. Q_{dep} and Q_{inv} stand respectively for depletion and inversion charge expressed as:

$$Q_{dep} = \sqrt{2.q.N_a.\epsilon_s.V_s} \tag{1.18}$$

$$Q_{inv} = q.\sum_i n_{i,v} \tag{1.19}$$

where V_s is the band bending in the Si substrate (the surface potential), N_a the Si p-doping concentration and $n_{i,v}$ the electron concentration on the i^{th} subband of the v band.

In this model, the energy levels obtained using the conventional triangular well approximation ($E_{i,v}^{TWA}$) [61] has been corrected by the non-linearity potential well ($\Delta E_{i,v}^{NL}$) and the wave function penetration ($\Delta E_{i,v}^{WFP}$) corrections as:

$$E_{i,v} = E_{i,v}^{TWA} - \Delta E_{i,v}^{NL} - \Delta E_{i,v}^{WFP} \tag{1.20}$$

where

$$E_{i,v}^{TWA} = \left(\frac{\hbar^2}{2m_v}\right)^{1/3} . \left[\frac{3\pi.q.F_{i,v}}{2}.\left(i+\frac{3}{4}\right)\right]^{2/3} \tag{1.21}$$

$$\Delta E_{i,v}^{NL} = \frac{4q.N_a}{15.\epsilon_s}.\left(\frac{\hbar^2}{2.q.m_v.F_{i,v}}\right)^{2/3} . \left[\frac{3\pi}{2}.\left(i+\frac{3}{4}\right)\right]^{4/3} \tag{1.22}$$

$$\Delta E_{i,v}^{WFP} = \frac{\hbar.m_{ox}.F_{i,v}}{m_v.\sqrt{2.m_{ox}.\left(\phi_{ox} - E_{i,v}^{TWA}\right)}} \tag{1.23}$$

In the above equations, ϕ_{ox} is the oxide barrier height. m_{ox} and m_v are the oxide and Si effective masses.

Using the improved triangular well approximation model (Improved TWA), J. Coignus et al [60] have compared the obtained energy levels from (1.20) to those calculated using the Poisson-Schrödinger PSL simulator. The $f_{i,v}$ parameters introduced in the equation (1.17) to reproduce the numerical results have been found to be equal to $f_{0L} = 0.58$ and $f_{0T} = 0.47$ respectively for the Δ_2 and Δ_4 Si conduction bands.
A similar study has been achieved using Poisson-Schrödinger UTOXPP results. The figure 1.21 shows that the analytical model takes well into account the wave functions penetration into the oxide. We reproduce the PS.UTOXPP eigenenergies using $f_{0L} = 0.88$ and $f_{0T} = 0.73$ respectively for the Δ_2 and Δ_4 Si conduction bands in strong inversion. These $f_{i,v}$ values are similar to those found by B.Govoreanu et al [56] ($f_{0L} = 0.86$ and $f_{0T} = 0.61$).
Indeed, the $f_{i,v}$ parameters are extracted by comparing the eigenenergies calculated using the Poisson-Schrödinger simulator to the analytical one (equation (1.20)).
The Improved TWA estimates precisely the effective electric field for each subband. Nevertheless, the comparison of the different $f_{i,v}$ values corresponding to each PS simulator shows a discrepancy (see figure 1.22).
Furthermore, even if we obtain similar energy levels at the same surface potential (figure 1.19), the $f_{i,v}$ values extracted from the PS.IMEP ($f_{0L} = 0.65$ and $f_{0T} = 0.43$ respectively for the Δ_2 and Δ_4 Si conduction bands [55]) are different than those extracted from the PS.UTOXPP (table 1.1).

$f_{i,v}$ **comparison**	**PSL [60]**	**UTOXPP**	**PS.IMEP [55]**
f_{0L}	0.58	0.88	0.65
f_{0T}	0.47	0.73	0.43

Table 1.1: Comparison of first two $f_{i,v}$ values extracted from PSL, PS.UTOXPP and PS.IMEP.

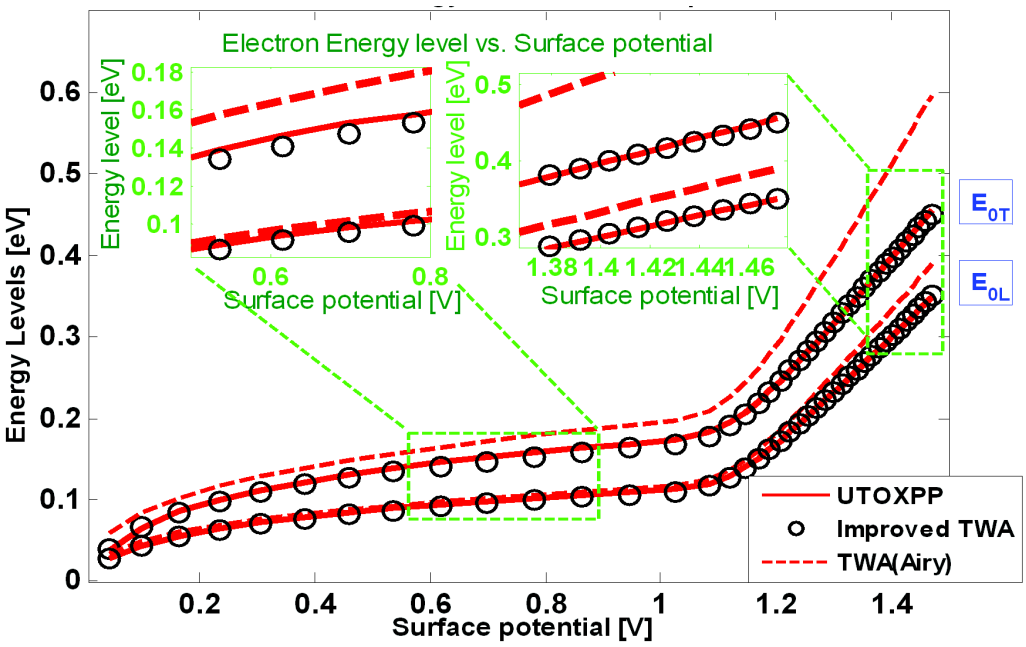


Figure 1.21: The first two subbands obtained using the PS.UTOXPP and Improved TWA model for a different surface potentials in the inversion regime.

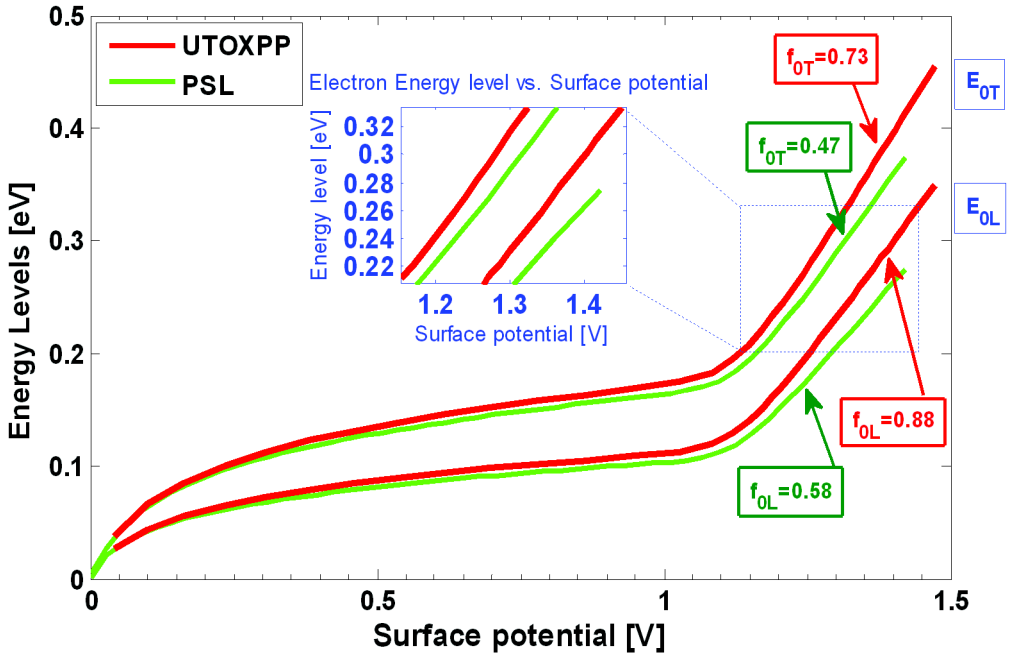
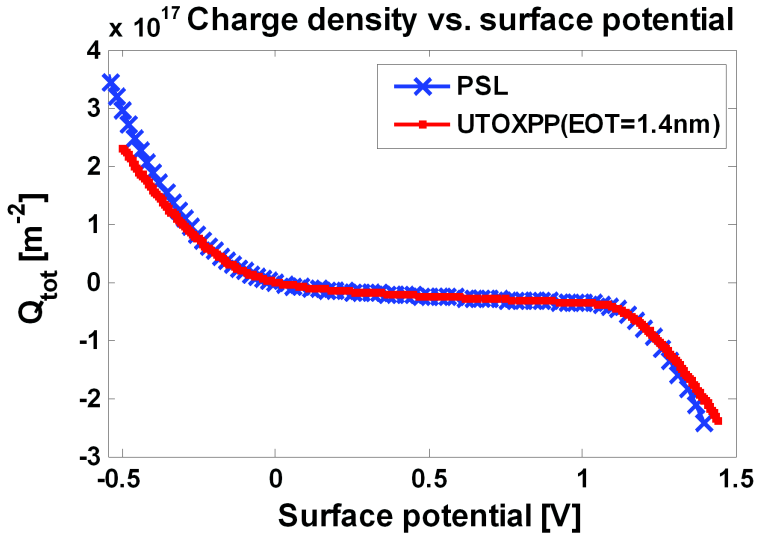


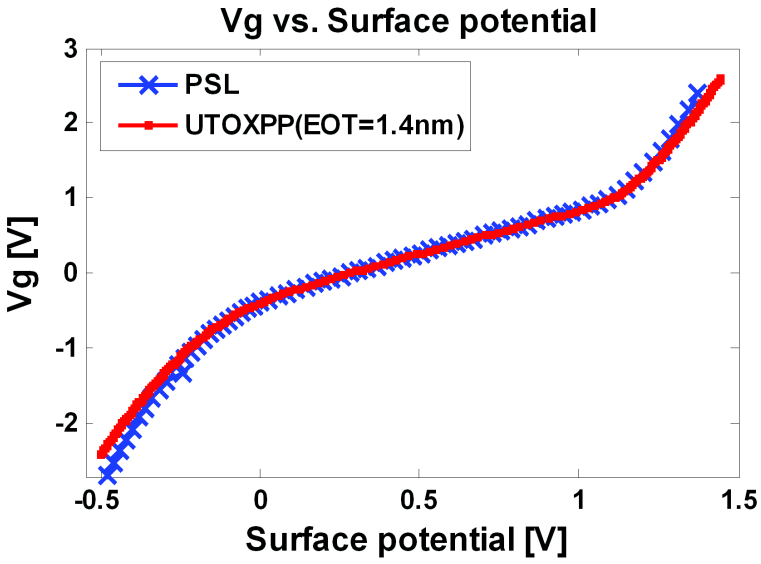
Figure 1.22: The first two subbands obtained using the PS.UTOXPP and PSL for a different surface potentials in the inversion regime.

As a conclusion, in order to compare the Poisson-Schrödinger simulator results, it is not relevant to compare the $f_{i,v}$ parameters of the effective electric field (equation 1.17). Besides,

it is important to investigate the impact of the simulation results discrepancy between the PS.UTOXPP and PSL simulator (shown in figure 1.22) on the C-V characteristic. Indeed, the observed eigenenergies discrepancy ($E_{0L}(UTOXPP) - E_{0L}(PSL) \approx 35meV$ at $V_s = 1.4V$) is also noticed in the evolution of the semiconductor total charge as a function of the surface potential ($Q_{tot}(UTOX) - Q_{tot}(PSL) = 4.08 \times 10^{16} m^{-2}$ at $V_s = 1.4V$) (figure 1.23.a). The gate voltages (V_g) computed using the PSL and UTOXPP are also slightly different (figure 1.23.b). However, the comparison of the obtained C-V characteristic shows no influence on the C-V response (figure 1.24).



(a)



(b)

Figure 1.23: The evaluation of the total charge (a) and gate voltage (b) as a function of the surface potential.

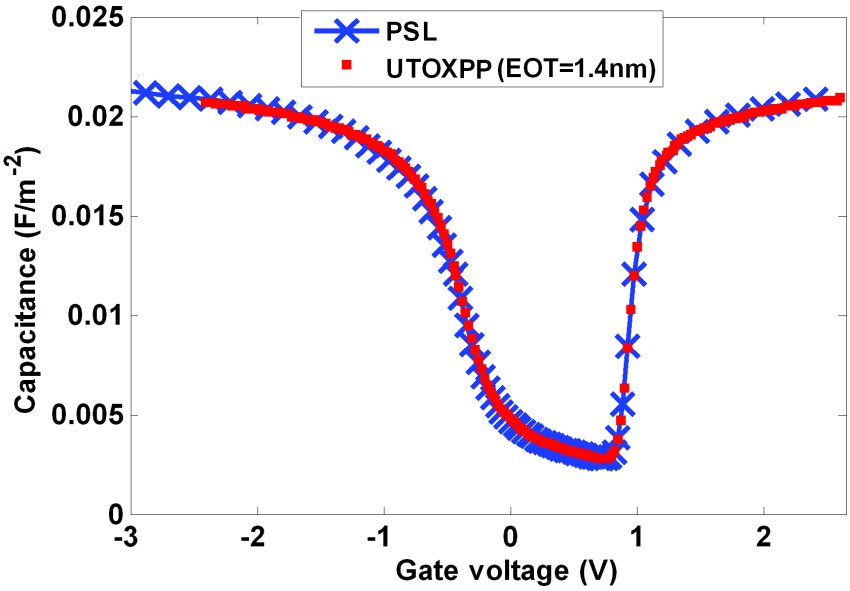


Figure 1.24: Comparison of the C-V calculated using UTOXPP and PSL simulators. (Si n-MOSFET with $T_{SiO2} = 0.8nm, T_{HfO2} = 3nm$).

1.3.2 C-V simulations of Si nMOSFETs

In this section, we validate the UTOXPP C-V simulations by comparison to measurements.

To this end, we have considered the N^+ polysilicon gate/SiO_2/Si nMOSFET. The SiO_2 insulator thickness was varied from 12$\mathring{A}$ to 35$\mathring{A}$. The C-V measurements for the different oxide thicknesses are plotted in figure 1.25. The gate capacitance increases for a thinner dielectric (see equation 1.11). A very good agreement is noticed between the simulated (lines) and measured C-V curves (symbols). Besides, a comparison between the simulation results using UTOXPP and PSL is also performed. A good matching is observed (figure 1.25).

The corresponding equivalent oxide thickness of each Si nMOSFET can be extracted thanks to C-V simulations. Indeed, it consists of determining the SiO_2 thickness, needed as C-V simulation input, to fit the measured C-V. Table 1.2 shows a very good adequacy between the EOT Ellipsometry measurements and values extracted using UTOXPP and PSL, evidencing the usefulness of the C-V simulation model.

Ellipsometry EOT ($\mathring{A}$)	**35**	**32**	**25.65**	**20.8**	**16.1**	**15.9**	**12.1**
PSL ($\mathring{A}$)	35	32	26.5	22	19	17.5	14.5
UTOXPP ($\mathring{A}$)	35	32	26.5	22	19.5	17.5	14.5

Table 1.2: Comparison of the measured EOT (by Ellipsometry) to values extracted from the PSL and UTOXPP.

In addition, UTOXPP C-V simulations of MOSFETs integrating a metal gate and bilayer insulators were also validated during this thesis. The C-V characteristic of the metal/$HfSiON/SiON/Si$

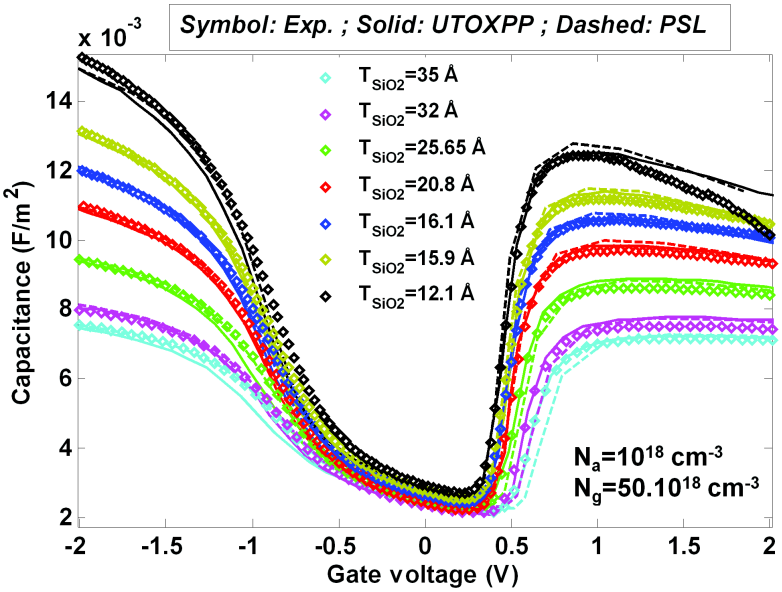


Figure 1.25: C-V simulations of N^+ polysilicon gate/SiO_2/Si nMOSFET using UTOXPP and PSL simulator. The SiO_2 thickness was varied from 1.2nm to 3.5nm.

nMOSFET has been simulated using UTOXPP. Figure 1.26 illustrates a very good fit of the measured C-V proving the validity of the C-V UTOXPP model.

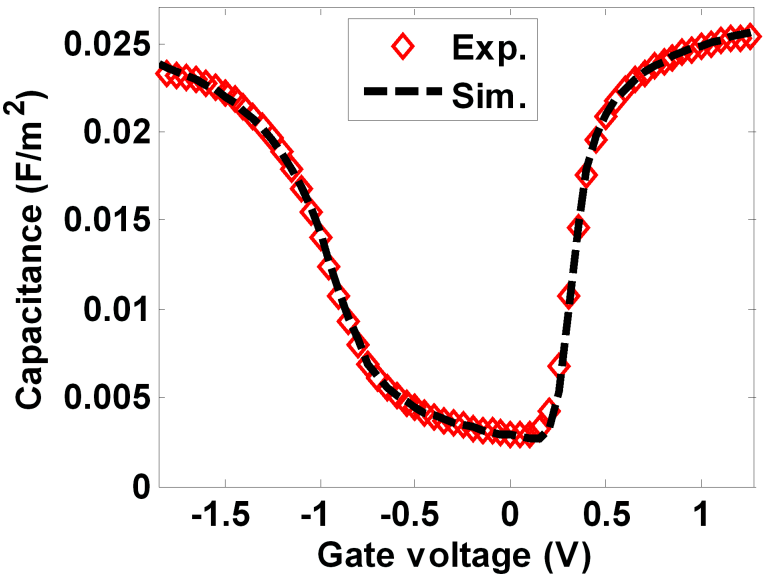


Figure 1.26: Measured and simulated C-V of Metal/HK/IL/Si nMOSFET. The HK and IL physical thicknesses are 1.4nm and 1.3nm respectively. The Si concentration doping is 4.10^{17}cm^{-3}.

1.4 Conclusion

In this chapter, basic principles of ideal and real MOS capacitors have been explored. The MOS capacitor evidences three different gate bias operation modes which are the accumulation, depletion and inversion regimes. In advanced CMOS technologies, oxide defects and dipoles at gate stack interfaces have a prominent influence on the C-V characteristic. Here, the oxide defects and interface traps impact on the C-V characteristic have been addressed evaluating the flat band voltage expression in the real MOS capacitor.
In actual ultra-thin devices, predicting the quantum effects requires Poisson-Schrödinger simulation. In the second section, UTOXPP Poisson-Schrödinger simulation results was validated by comparison to PSL solver and literature results. Afterwards, UTOXPP C-V simulation model is validated for Si nMOSFETs with polysilicon and metal gate.

Chapter 2

C-V simulations of SiGe devices

Contents

2.1 Introduction

An accurate simulation of the strained $SiGe/Si$ pFETs C-V characteristic needs a rigorous calculation of the strained $SiGe/Si$ bands structure and proper description of the charge density. This chapter focuses on strained $SiGe/Si$ heterostructure band structure modeling. Three solutions based on the effective mass approximation are proposed and compared to the accurate 6-level k.p model with an in-plane numerical integration in order to account efficiently for the hole density.
The $SiGe$ incorporation impact on the C-V characteristic of $SiGe$ pMOSFETs is investigated in section 2.4.

2.2 Strained SiGe/Si electrostatics modeling

In $SiGe/Si$ pMOSFETs, the $SiGe$ layer growth on Si substrate creates a conduction and valence bands discontinuity. Due to $SiGe$ and Si lattice constants mismatch, the $SiGe$ is biaxially strained to match the substrate in-plane lattice constant. Depending on the heterostructure type and Ge content, $SiGe/Si$ band offsets enable carrier confinement [62]. Besides, the biaxially strain causes band splitting and shifts affecting the effective mass and the density of states.

In order to understand the strain effects on the $SiGe$ band structures, we study in the following the band alignment and strain effects within the $SiGe/Si$ heterostructure. To this end, the deformation potential approximation will be explained and adopted for the effective mass approximation model (EMA). The 6-band k.p hamiltonian will be reported and strain component will be explored.

2.2.1 Strained $SiGe$ on Si

The elemental semiconductors Silicon (Si) and Germanium (Ge) are both from group IV of the periodic table. They are isoelectronic. As a result, their chemical and electronic properties are similar. Thus, it is possible to form a solid solution to obtain a Silicon Germanium ($SiGe$) alloy. The Ge concentration, (xGe) can be varied over the entire compositional range ($0 \leq xGe \leq 1$). So, obtained compositions can be Si-rich ($xGe < 0.5$) or Ge-rich ($xGe > 0.5$).

In $SiGe$ based pMOSFETs, the $SiGe$ layer is epitaxied on the Si buffer layer. The $SiGe$ epitaxy on Si induces a strained $SiGe$ on Si heterostructure. Indeed, the active channel material, $SiGe$, has a 4.2 % larger lattice constant than Silicon (table 2.1). Thus, $SiGe$ is compressively strained to match the lattice constant (parallel to the interface plane) of the unstrained Si substrate material. The lattice constant perpendicular to the interface also changes to compensate for this lateral strain in the $SiGe$ material (figure 2.1).

$a(Si) = a_{Si}$	$a(Ge)$	$a(Si_{1-x}Ge_x) = a_{Si_{1-x}Ge_x}$
5.431$\AA$	**5.66**$\AA$	$5.431 + 0.2x + 0.027x^2$

Table 2.1: Lattice parameters of the Si, Ge and $Si_{1-x}Ge_x$.

The difference in lattice parameters of Si and $SiGe$ causes a biaxial compressive strain within $Si_{1-x}Ge_x$ alloy layer with in-plane components $\varepsilon_{\parallel} = \varepsilon_{xx} = \varepsilon_{yy} = (a_{Si} - a_{SiGe})/a_{SiGe} \approx -0.04x$ ([63][64]). In the (001) growth direction, the $SiGe$ lattice parameter is further enlarged and

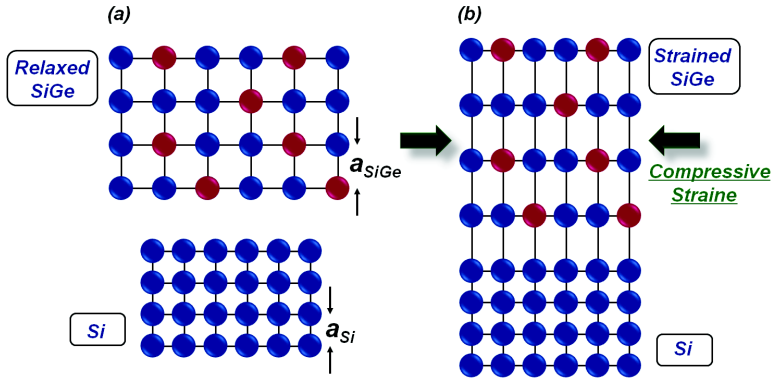


Figure 2.1: (a) A schematic diagram of the bulk lattice constant of a thin $Si_{1-x}Ge_x$ film to be grown on top of a thin bulk Silicon layer. (b) A schematic diagram showing the tetragonal lattice (perpendicular to the interface) distortion when the two films from (a) are placed together. The $Si_{1-x}Ge_x$ film is compressively strained.

depends on the elastic constants (table 2.2) as: $\varepsilon_\perp = \varepsilon_{zz} = -2\varepsilon_\parallel C_{12}/C_{11} = -0.77\varepsilon_\parallel \approx 0.03x$. Thus, the lattice constant in the growth direction in a pseudomorphic Ge layer on (001) Si is about 7% larger than in Si. In the case of epitaxial growth inducing biaxial strain, the strain tensor [1] of the strained $SiGe$ on (001) Si substrate is written as:

$$\begin{cases} \varepsilon_{xx} = \varepsilon_{yy} = \varepsilon_\parallel \\ \varepsilon_{zz} = -2\varepsilon_\parallel \dfrac{C_{12}}{C_{11}} \\ \varepsilon_{xy} = \varepsilon_{xz} = \varepsilon_{yz} = 0 \end{cases} \tag{2.1}$$

Material	$C_{11}(GPa)$	$C_{12}(GPa)$
Si	**165.8**	**63.9**
Ge	**131.8**	**48.3**

Table 2.2: Elastic constants C_{ij} of the Si and Ge [65].

In $SiGe/Si$ pMOSFETs, thin strained $SiGe$ ($T_{SiGe} \leq 12nm$) is grown on top of a bulk Silicon wafer substantially thicker than the epitaxial layer. The provided misfit between the epilayer and substrate is sufficiently small. So, the first atomic layers grown on the substrate will be strained and latticed matched to the substrate. Indeed, a coherent or pseudomorphic strained $SiGe/Si$ heterointerface will be formed where the strained layer is forced to have the substrates in-plane lattice constant and the epilayer becomes tetragonally distorted. As the epitaxial layer thickness is increased, there exists a maximum thickness, called the critical thickness (h_c) for which it costs too much energy to elastically strain additional heterolayers. In this case, misfit dislocations appear and act to relieve the strain in the epitaxial film. Different models have been developed to predict the critical thickness of the strained epitaxial layer [66][67][68]. This

[1] In all strained $SiGe$ UTOXXP Poisson-Schrödinger simulation results, the strain tensor 2.1 is solver input parameters.

critical thickness is plotted as a function of the Ge concentration in figure 2.2. Experimentally, it was observed that many pseudomorphic layers could be grown well above the critical thickness values predicted from the equilibrium theories. In part, this has been related to the difficulty in detecting low densities of dislocations, but is predominantly related to a kinetic barrier to the relaxation process allowing metastable layers to be grown [69]. This was first modeled by People and Bean [70] (figure 2.2).

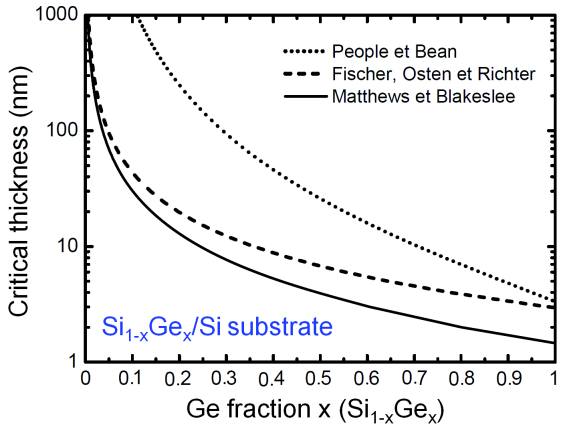


Figure 2.2: Critical thickness [67] versus Ge content for pseudomorphic $Si_{1-x}Ge_x$ layers grown on bulk (100) Si.

2.2.2 Strain effects on the $SiGe$ band structure

R. People [71] reported the first theoretical study of the Ge composition effects on the $SiGe/Si$ band structure. He showed that strain shifts and splits conduction and valence bands energy levels. Strain in the Si/Ge heterostructure was then studied theoretically by C. G. Van de Walle and R. M. Martin based on self-consistent calculations using ab initio pseudopotentials [72]. Further work on this heterostructure was done by M. M. Rieger and P. Vogl using an empirical pseudopotential method [73]. They concluded that the strain in strained layers has two main effects on the band structure: the hydrostatic strain shifts the energetic band position and the uniaxial strain component splits degenerate bands [74].
In this section, we investigate how the strain impact on the $SiGe$ material band structure is taken into account using EMA and 6-band k.p models in absence of an external applied potential.

2.2.2.1 EMA model and deformation potential

The band structure description refers to the eigenvalue determination from the Schrödinger equation:

$$H_{1e0}\phi_v(r) = E_v\phi_v(r) \tag{2.2}$$

Within the effective mass approximation, the single electron Hamiltonian is written in absence of an external confinement potential as:

$$H_{1e0} = \frac{p^2}{2m} \tag{2.3}$$

The resolution of the equation 2.2 for the relaxed $SiGe$ material gives the relaxed eigenvalues.

As mentioned in the previous section, homogeneous $Si_{1-x}Ge_x$ alloy layer pseudomorphically grown on (001) Si substrate is biaxially compressed by $\varepsilon_{\parallel} = -0.04x$. This biaxial compression can be described by a hydrostatic compression and a uniaxial tension along [001] direction. These strain components cause a shift of the average band energy level and a splitting of degenerate bands.
Using UTOXPP simulator within the effective mass approximation, they are calculated within the linear deformation potential approximation.
Here, we have used the symbol ΔE to denote the energy level shift induced by the strain $\Delta E = E(strained) - E(relaxed)$.
The hydrostatic strain shifts the valence and conduction band edge levels of the Si-like $SiGe$ fundamental bandgap by [72]:

$$\begin{cases} \Delta E_{hyd}^{VB} = a_v \left(2\varepsilon_{\parallel} + \varepsilon_{\perp}\right) \\ \Delta E_{hyd}^{\Delta} = a_c \left(2\varepsilon_{\parallel} + \varepsilon_{\perp}\right) \end{cases} \tag{2.4}$$

where a_c and a_v are hydrodynamic deformation potentials for the conduction and valence bands respectively.

The uniaxial strain component splits the $SiGe$ valence band states. The spin-orbit and strain splittings interact and produce a total splitting of the valence band (figure 2.3). Indeed, the light-hole (LH) band and spin-orbit split-off hole (SO) band interact with an anti-crossing-like behaviour while the heavy-hole (HH) band shifts linearly [75][76][72]. C. Y. P. Chao and S. L. Chuang [77] illustrated how the strain modifies the valence-band structure of semiconductors, with the emphasis on the coupling between the HH, LH bands and the SO bands. They have proposed a formulation based on the theory of Luttinger-Kohn and Bir-Pikus. This can be used to compute the $SiGe$ valence bands uniaxial strain component shifts with respect to their weighted average.
Thus, the $SiGe$ band-edge energies are expressed as [77]:

$$\begin{cases} \Delta E_{uni}^{HH} = -P_{\varepsilon} - Q_{\varepsilon} \\ \Delta E_{uni}^{LH} = -P_{\varepsilon} + \frac{1}{2}(Q_{\varepsilon} - \Delta + \sqrt{\Delta^2 + 2\Delta Q_{\varepsilon} + 9Q_{\varepsilon}^2}) \\ \Delta E_{uni}^{SO} = -P_{\varepsilon} + \frac{1}{2}(Q_{\varepsilon} - \Delta - \sqrt{\Delta^2 + 2\Delta Q_{\varepsilon} + 9Q_{\varepsilon}^2}) \end{cases} \tag{2.5}$$

where Δ is the spin–orbit split-off energy, $P_{\varepsilon} = -a_v(2\varepsilon_{\parallel} + \varepsilon_{\perp})$, $Q_{\varepsilon} = -b(\varepsilon_{\parallel} - \varepsilon_{\perp})$ and b is the uniaxial deformation potential of the valence band. Both the splitting of the conduction bands as a result of the uniaxial strain, and the shift of the weighted average with respect to the valence band can be also expressed in terms of deformation potentials.
The uniaxial part of the strain splits the degeneracy of the sixfold degenerate Δ valleys into two valleys Δ_2 in the [001]-direction and fourfold degenerate Δ_4 valleys within the layer plane (figure 2.3). The uniaxial induced energy shifts of the conduction bands are given by:

$$\begin{cases} \Delta E_{uni}^{\Delta_2} = +\frac{2}{3}\Xi_u^{\Delta} \left(\varepsilon_{\perp} - \varepsilon_{\parallel}\right) \\ \Delta E_{uni}^{\Delta_4} = -\frac{1}{3}\Xi_u^{\Delta} \left(\varepsilon_{\perp} - \varepsilon_{\parallel}\right) \end{cases} \tag{2.6}$$

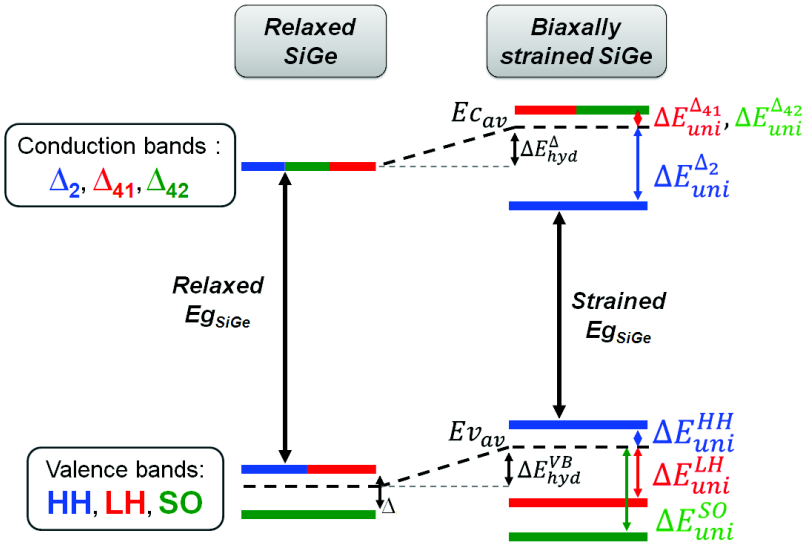


Figure 2.3: Schematic presentation of the strain impact on the *SiGe* conduction and valence bands.

where Ξ_u^{Δ} is the uniaxial strain deformation potential for the Δ conduction band.
Pure *Si* and *Ge* deformation potentials parameters are summarized in table 2.3 [72][78]. Values for $Si_{1-x}Ge_x$ alloys are linearly interpolated.

Si	**Exp.[72]**	**Present model (based on 30-k.p [79])**
a_v		**2**
a_c		**3.94**
b	**-2.1±0.1**	**-2.27**
Δ		**0.044**
Ξ_u^{Δ}	**8.6±0.4**	**9.01**
Ge	**Exp.[72]**	**Present model (based on 30-k.p [79])**
a_v		**2.1**
a_c		**3.83**
b	**-2.86±0.15**	**-2.8**
Δ		**0.29**
Ξ_u^{Δ}		**10**

Table 2.3: Deformation potentials of *Si* and *Ge* (eV).

The bandgap of strained $SiGe$ on (001) Si is so calculated by the difference of electron and hole energy shifts as (figure 2.3):

$$E_g^{sSiGe} = E_c^{\Delta}(rSiGe) + \Delta E_{hyd}^{\Delta} + \Delta E_{uni}^{\Delta_2} - \Delta E_{hyd}^{VB} - \Delta E_{uni}^{HH} \tag{2.7}$$

where $E_c^{\Delta}(rSiGe)$ is the conduction band level of the relaxed $SiGe$.

2.2.2.2 6-Band k.p model

For holes in $SiGe$ valence bands, the effective-mass approximation is usually not accurate enough, and a multi-band approach treating the three main valence bands simultaneously is needed. Since each of the three valence bands has two spin components, we need here the 6-band k.p-equation to model accurately $SiGe$ valence bands. In the k.p theory, the three top valence bands are typically considered. These are the heavy hole (HH), light hole (LH) and the split-off valence bands.
The k.p method was originally an application of the perturbation approach to study energy bands and wave functions around high-symmetry points in k space. G. Dresselhaus et al [80] established the k.p approach as a rigorous basis for the empirical determination of band structure. Extensive derivations and calculations using the k.p method, and many review papers by E.O. Kane [81][82][83][84][85][86] have transformed this perturbative approach into one of the main methods used in Solid State Physics.
In this part, we present a review of the k.p method implemented in the UTOXPP simulator to compute the strained $Si_{1-x}Ge_x$ valence band structure. We give the total k.p Hamiltonian expression of the valence bands of the relaxed (H_{6kp}^r) and strained (H_{6kp}^s) $SiGe$.

The k.p method can be derived from the time independent Schrödinger equation of the one-electron in a periodic ionic potential:

$$H_{1e0}\phi_v(r) = (\frac{p^2}{2m} + V_{ion}(r))\phi_v(r) = E_v\phi_v(r) \tag{2.8}$$

where H_{1e0} and $V_{ion}(r)$ are the one-electron Hamiltonian and the total ionic potential.
Using the Bloch theorem, the eigenenergy states solutions of equation 2.8 are expressed as:

$$\phi_{vk}(r) = exp(ik.r).U_{vk}(r) \tag{2.9}$$

where v is the subband index, k is the wave vector in the first Brillouin zone and $U_{vk}(r)$ denotes the periodic Bloch amplitude.
Substituting the wave functions (2.9) into the one-electron Hamiltonian, one arrives to the following equation:

$$\left[\frac{p^2}{2m} + V_{ion}(r) + \frac{\hbar}{m}k.p\right]U_{vk}(r) = \left[E_{vk} - \frac{\hbar^2k^2}{2m}\right]U_{vk}(r) \tag{2.10}$$

The solution of (2.10) can be obtained by developing a perturbation theory over $(\frac{\hbar}{m}k.p)$. It is due to this term that the method has the name k.p theory. In general, the method can be applied to calculate the band dispersion near any point k by expanding (2.10) around k point providing the wave functions and eigenenergies.

The k.p Hamiltonian is written for the three valence bands in the basis set $\mid e_i\rangle$ (i=1, 2, 3), which are the three Block wave functions at the Γ symmetry point. It is expressed as a function of Dresselhaus parameters [80] usually called L, M, and N in the form [87]:

$$H_{3\times3} = \begin{pmatrix} h_{xx} & h_{xy} & h_{xz} \\ h_{yx} & h_{yy} & h_{yz} \\ h_{zx} & h_{zy} & h_{zz} \end{pmatrix}$$

where

$$\begin{cases} h_{\alpha\alpha} = \dfrac{\hbar^2}{2m_0} + L.k_\alpha^2 + M.(k_\beta^2 + k_\gamma^2) \\ h_{\alpha\beta} = N.k_\alpha k_\beta \end{cases} \tag{2.11}$$

The Greek indices α, β and γ stand for the coordinates x, y and z in the principal coordinate system.

By including the spin degree of freedom $\xi = \uparrow, \downarrow$, the basis set $\mid e_i\rangle$ is extended to $\mid e_j, \xi\rangle$. So, the $H_{6\times6}$ Hamiltonian including spin is block-diagonal as:

$$H_{6\times6} = \begin{pmatrix} H_{3\times3} & 0_{3\times3} \\ 0_{3\times3} & H_{3\times3} \end{pmatrix}$$

In order to describe the valence band correctly, the spin-orbit interaction must be taken into account properly. The effect of spin-orbit coupling is considered by introducing an interaction term H_{so} written in the basis set $\mid e_j, \xi\rangle$ as:

$$H_{so} = -\frac{\Delta}{3} - \begin{pmatrix} 0 & i & 0 & 0 & 0 & -1 \\ -i & 0 & 0 & 0 & 0 & i \\ 0 & 0 & 0 & 1 & -i & 0 \\ 0 & 0 & 1 & 0 & -i & 0 \\ 0 & 0 & i & i & 0 & 0 \\ -1 & -i & 0 & 0 & 0 & 0 \end{pmatrix}$$

where Δ is the spin–orbit split-off energy.
The total k.p Hamiltonian of the relaxed $SiGe$ valence bands (H^r_{6kp}) including spin-orbit interaction is depending to γ_1, γ_2 and γ_3 Luttinger parameters as [88][89]:

$$H^r_{6kp} = -\begin{pmatrix} P+Q & -S & R & 0 & \frac{-1}{\sqrt{2}}S & \sqrt{2}R \\ -S^+ & P-Q & 0 & R & -\sqrt{2}Q & \sqrt{\frac{3}{2}}S \\ R^+ & 0 & P-Q & S & \sqrt{\frac{3}{2}}S^+ & \sqrt{2}Q \\ 0 & R^+ & S^+ & P+Q & -\sqrt{2}R^+ & \frac{-1}{\sqrt{2}}S^+ \\ \frac{-1}{\sqrt{2}}S^+ & -\sqrt{2}Q & \sqrt{\frac{3}{2}}S & -\sqrt{2}R & P+\Delta & 0 \\ \sqrt{2}R^+ & \sqrt{\frac{3}{2}}S^+ & \sqrt{2}Q & \frac{-1}{\sqrt{2}}S & 0 & P+\Delta \end{pmatrix}$$

Here

$$\begin{cases} P(k) = \dfrac{\hbar^2}{2m_0}.\gamma_1.(k_x^2+k_y^2+k_z^2) \\ Q(k) = \dfrac{\hbar^2}{2m_0}.\gamma_2.(k_x^2+k_y^2-2k_z^2) \\ R(k) = \dfrac{\hbar^2}{2m_0}.\sqrt{3}[-\gamma_2.(k_x^2-k_y^2)+2i\gamma_3 k_x k_y] \\ S(k) = \dfrac{\hbar^2}{2m_0}.2\sqrt{3}\gamma_3(k_x-ik_y)k_z \end{cases} \tag{2.12}$$

Measured and k.p model values of the Luttinger parameters γ_1, γ_2 and γ_3 for Si and Ge are summarized in table 2.4.

Si	**Exp.**	**Present model[f] (based on 30-k.p)**
γ_1	**4.26[a], 4.285[a], 4.23[b],4.22[c]**	**4.338**
γ_2	**0.38[a], 0.339[a], 0.31[b],0.39[c]**	**0.3468**
γ_3	**1.56[a], 1.446[a], 1.46[b], 1.44[c]**	**1.4451**
Ge	**Exp.[72]**	**Present model[f] (based on 30-k.p)**
γ_1	**13[d],12.8± 2.9[e], 13.25[a]**	**10.41**
γ_2	**4.4[d],4± 0.3[e], 4.2[a]**	**3.045**
γ_3	**5.3[d], 5.5± 0.3[e], 5.56[a]**	**4.313**

[a] Reference [90] [b] Reference [91] [c] Reference [92]
[d] Reference [80] [e] Reference [93] [f] Reference [79]

Table 2.4: Measured and k.p model values of the Luttinger parameters γ_1, γ_2 and γ_3 for Si and Ge.

Strain induced wrapping and splitting of $SiGe$ bands can be calculated within the k.p model. Actually, within the deformation potential theory the valence bands energy shifts are computed from the strain-dependent perturbation Hamiltonian δH_s added to the k.p Hamiltonian H^r_{6kp} [94][95]:

$$\delta H_s = \begin{pmatrix} \delta h_s & 0_{3\times3} \\ 0_{3\times3} & \delta h_s \end{pmatrix}$$

where

$$\delta h_s = \begin{pmatrix} l.\varepsilon_{xx} + m.(\varepsilon_{yy} + \varepsilon_{zz}) & n.\varepsilon_{xy} & n.\varepsilon_{xz} \\ n.\varepsilon_{xy} & l.\varepsilon_{yy} + m.(\varepsilon_{xx} + \varepsilon_{zz}) & n.\varepsilon_{yz} \\ n.\varepsilon_{xz} & n.\varepsilon_{yz} & l.\varepsilon_{zz} + m.(\varepsilon_{xx} + \varepsilon_{yy}) \end{pmatrix}$$

The three parameters l,m, and n denote valence band deformation potentials. They are computed as:

$$\begin{cases} l = a_v + 2b_v \\ m = a_v - b_v \\ n = 2\sqrt{3}d \end{cases} \tag{2.13}$$

where d is equal to $-4.36eV$ and $-5.5eV$ for Si and Ge respectively.
Consequently, the total 6×6 Hamiltonian of the valence band in strained $SiGe$ is the sum of $H_{6\times6}$, H_{so} and δH_s:

$$H^s_{6kp} = H_{6\times6} + H_{so} + \delta H_s \tag{2.14}$$

Diagonalization of the total Hamiltonian H^s_{6kp} gives the strained $Si_{1-x}Ge_x$ energy valence bands.

Figure 2.4 shows strained $Si_{1-x}Ge_x$ conduction and valence bands computed using the k.p model [79]. We notice that all valence band separation bandgaps in $SiGe$ are smaller than in Si. They monotonically decrease with increasing Ge content. Figure 2.4 illustrates also the strained $Si_{1-x}Ge_x$ bands evolution with xGe obtained using the deformation potential approximation (see subsection 2.2.2.1). Good agreement is noticed evidencing the validity of this approximation for $xGe < 0.5$.
The strained $SiGe$ effective masses are related to the Luttinger parameters γ_1, γ_2 and γ_3 as [77]:

$$\begin{cases} \dfrac{m^*_{HH}}{m_0} = \dfrac{1}{\gamma_1 + \gamma_2} \\ \dfrac{m^*_{LH}}{m_0} = \dfrac{1}{\gamma_1 - \gamma_2} \\ \dfrac{m^*_{SO}}{m_0} = \dfrac{1}{\gamma_1} \end{cases} \tag{2.15}$$

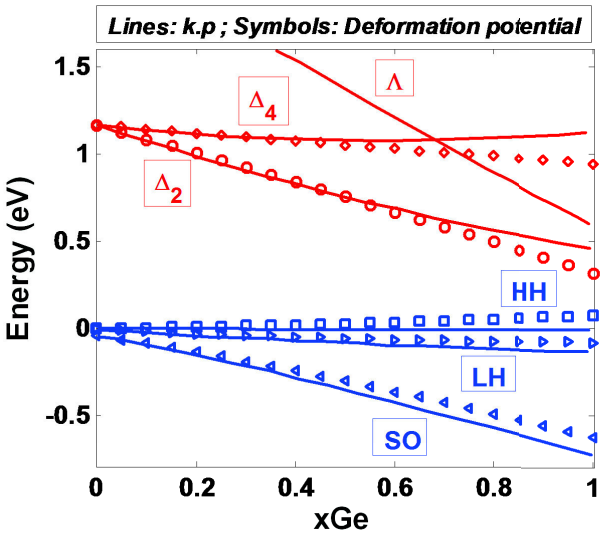


Figure 2.4: Strained $Si_{1-x}Ge_x$ on (001) Si conduction and valence bands computed using the k.p model (symbols) [79] and deformation potential approximation (lines) as a function of xGe. Here, the reported results correspond to low temperature band gap ($E_g(Si) = 1.17eV$).

2.2.2.3 Application to confined $SiGe/Si$

When an external electric field is applied or in presence of heterostructures, carriers confinement should be taken into account.
Indeed, the prediction of the heterostructure electronic properties is complex and needs an accurate treatment of the wave functions at interfaces [96]. When applying an external potential, a confinement potential term ought to be added to the total Hamiltonian. This term is the issue of the Poisson equation resolution. As a result, the Schrödinger equation of a confined electron gas is written as:

$$(H_{1e0} + U(r))\phi_v(r) = E_v\phi_v(r) \tag{2.16}$$

where H_{1e0} is the single electron Hamiltonian given in table 2.5 and $U(r)$ an external confinement potential.

Model	6-Band k.p	EMA
H_{1e}	$\frac{p^2}{2m} + V_{ion}(r)$	$\frac{p^2}{2m}$

Table 2.5: Single electron Hamiltonian in absence of a confinement external potential.

The Schrödinger equation should be self-consistently evaluated with the Poisson equation in order to describe the quantum charge redistribution at interfaces between two materials. For more details, the reader can be refer to [96][97].

2.2.3 Charge density

In 2D system, an electron is confined along one dimension but able to travel freely in the other two directions. Under the parabolic bands approximation, the constant energy surface is a

sphere. In this case, an analytical description of the 2D density of states (DOS) is possible. It is evaluated analytically as a function of the DOS mass (M_{DOS}) as:

$$g^{2D} = \frac{M_{DOS}}{\pi\hbar^2} \tag{2.17}$$

However, When the full band description is employed, the constant energy surfaces are more complicated. It is necessary to apply the general definition of the DOS function [98][99]:

$$g(E) = \sum_{\nu} \sum_{k \in BZ} \delta[E - E_\nu(k)] = \sum_{\nu} \frac{1}{(2\pi)^3} \cdot \oint_{S_k(E)} \frac{dS_k(E)}{|\nabla_k E_\nu(k)|} \tag{2.18}$$

where δ and S_k are Dirac distribution and constant energy surfaces.
The DOS function is obtained by summing and integrating over the constant energy surface $E_\nu(k) = E$ associated with the subband ν in the Brillouin zone (BZ). For the full band case, $E_\nu(k)$ is not available in an analytical form. It is in a numerical form obtained from the k.p model. Therefore, it is necessary to convert 2.18 from a continuous expression to a discrete expression which can be used to integrate the constant energy surfaces numerically. To do so, the Brillouin zone should be discretized into cubes. The DOS is obtained using the G. Gilat and L. J. Raubenheimer [100] approach.

Indeed, accurate description of the DOS is essential for a precise carrier density modeling [101].
The expression of the total hole density can be obtained by summing over in-plane wave vectors (k_x,k_y) for each subband level ν [102] to get:

$$p(z) = \sum_{\nu} \sum_{K=[k_x,k_y]} \delta[E - E_\nu^K].F(E_\nu^K - E_F). \mid \Psi_{\nu,K}(z) \mid^2 \tag{2.19}$$

Where Ψ_ν and E_ν are respectively the eigenstate and the eigenenergy of the k.p Schrodinger equation, E_F is the Fermi level and F is the Fermi-Dirac function.

In order to accurately model the density of states, equation 2.19 is integrated on a dense grid in K space of the first Brillouin zone. This method requires CPU resources since the charge density is self-consistently coupled with the 1D Poisson equation (See chapter 1 on page 17.).
Under the effective mass approximation, we have computed the dispersion relation as:

$$E_\nu^K = E_\nu^{K=0} + \frac{\hbar^2 K_\parallel^2}{2m} \tag{2.20}$$

where $\hbar$ is the reduced Planck's constant (h/2π), $K_\parallel$ is the wave vector in the (k_x, k_y) plane and m is the corresponding effective mass.
Thus, the hole density can be analytically integrated and written as:

$$p(z) = \sum_{\nu} g_{\nu} \frac{m^{\nu}_{DOS} k_B T}{\pi \hbar^2} . ln \left[1 + exp \left(\frac{E_{\nu} - E_F}{k_B T} \right) \right] . \mid \Psi_{\nu, K=[0,0]}(z) \mid^2 \tag{2.21}$$

where E_F is the Fermi level, k_B is the Boltzmann constant, T is the temperature, g_{ν} is the band degeneracy and m^{ν}_{DOS} is the in-plane (k_x, k_y) density of states effective mass of the ν-th subband (is not constant in the z-direction).
This approximation is valid only for the effective mass approximation (EMA) in the absence of a heterostructure.

2.2.4 Strained $SiGe/Si$ band structure

In $SiGe/Si$ pMOSFETs, $SiGe$ and Si are brought into physical contact by epitaxially growing the $SiGe$ on top of Si. The $SiGe$ epitaxy on Si induces a strained $SiGe$ on Si heterostructure. The magnitude of $SiGe/Si$ band offset depends on bandgap values of both materials and the valence band discontinuity between the two materials. The knowledge of these quantities makes the band structure construction possible.

2.2.4.1 $Si_{1-x}Ge_x$ band gap energy

The $Si_{1-x}Ge_x$ bandgap exhibits a Si-like $\triangle$ conduction band minimum when the Ge content is less than 0.85. For xGe>0.85, it has a Ge-like character with a Λ conduction band minimum [103]. The relaxed $SiGe$ energy band gap has been studied both theoretically and experimentally [104][65][105][103].
Figure 2.5 shows the relaxed $SiGe$ energy gap as a function of the Ge concentration (xGe) at low and room temperature. We notice a similar behaviour of the two temperatures data. The $Si_{1-x}Ge_x$ layer has a smaller bandgap than Silicon. 125meV decrease is noticed for xGe=0.3.

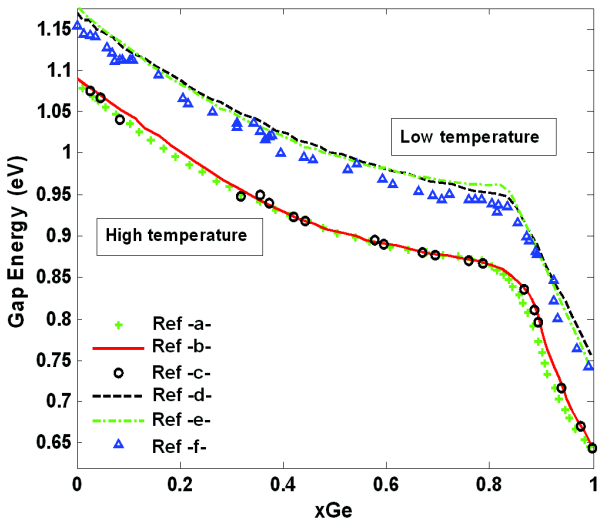


Figure 2.5: Relaxed $SiGe$ band gap energy as a function of Ge content at low and room temperature.(Ref -a-: [104]; Ref-b-: [103]; Ref -c-: [103]; Ref -d-: [73]; Ref -e-: [65]; Ref -f-:[105].)

In the UTOXPP Poisson-Schrödinger solver, the relaxed $Si_{1-x}Ge_x$ band gap energy is linearly interpolated:

$$E_g^{SiGe} = (1-x).E_g^{Si} + x.E_g^{Ge} \tag{2.22}$$

Indeed, this approximation is valid for Ge concentration less than 40%.

The well known measurements of the bandgap of coherently strained $Si_{1-x}Ge_x/Si$ heterosbructures were performed by D. V. Lang et al [106] utilizing photocurrent spectroscopy. Later, there have been many investigations of the bandgap of pseudomorphically grown strained $Si_{1-x}Ge_x$ on a relaxed Si substrate. Experimental data and some analytical results at low temperature have been reported in literature [107][106][65][107][108]. However, few results have been achieved at room temperature [104]. Therefore, we shall adopt strained low temperature $Si_{1-x}Ge_x/Si$ band gap data to estimate the bandgap at 300K. To do so, the bandgap temperature dependence relationship for Si may be used to estimate the bandgap of strained $Si_{1-x}Ge_x/Si$ at higher temperatures [74]:

$$E_g(x,T) = E_g(x,0K) - \frac{4.73 \times 10^{-4} T^2}{T + 636} \tag{2.23}$$

Figure 2.6 compares the obtained experimental data and some theoretical results of room temperature strained $Si_{1-x}Ge_x$ bandgap as a function of Ge content. For Ge contents up to 40%, there is a good agreement between the measured and computed band gap. We observe 60meV discrepancy between the analytical R. People band gap [104] (Theo2) and those calculated in [65] (Theo1). 240meV decrease is also noticed for 30% Ge evidencing 120mV drop of $SiGe$ band gap due to the strain effect. Besides, figure 2.6 shows the UTOXPP results obtained using C. Y. P. Chao and S. L. Chuang formulation [77] (see subsection 2.2.2.1). The UTOXPP energy band gap refers to the energy difference between the top of the valence band (HH) and the bottom of the conduction band (Δ_2). In fact, it is the equivalent of the energy gap difference reported in figure 2.4 at room temperature. The UTOXPP result matches the published data for $xGe \leq 0.4$ evidencing the band gap calculation validity.

Generally, the $SiGe$ band gap varies in presence of doping. The band gap dependency on the increase of the doping concentration is the "band gap narrowing" (BGN). It is one of the most important physical parameter variation encountered at medium and high dopings [109]. Figure 2.7 shows the band gap narrowing as a function of the Boron concentration for Si and $Si_{0.7}Ge_{0.3}$. The BGN boosts when the doping concentration increases. For impurity concentration less than 10^{18}cm^{-3}, an adequacy is observed between Si and $Si_{0.7}Ge_{0.3}$ and only 40mV BGN is estimated. However, 40mV discrepancy is observed at higher Boron concentration (10^{20}cm^{-3}).

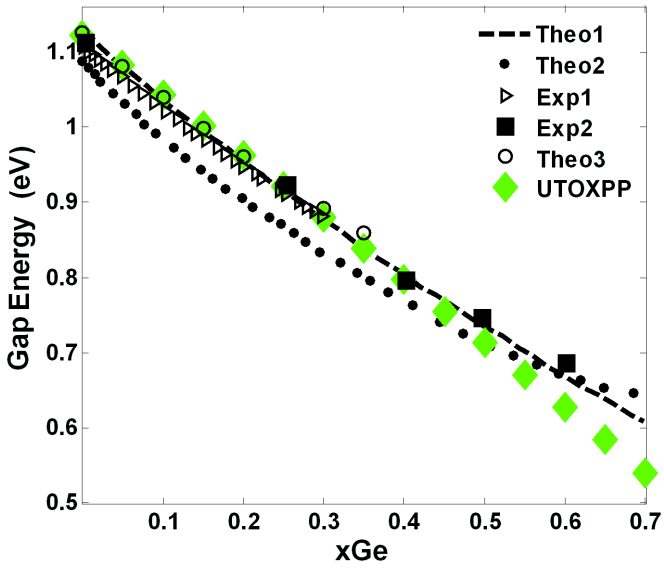


Figure 2.6: Strained $Si_{1-x}Ge_x$ band gap energy. Results of UTOXPP model are plotted in green symbol. Theoretical results and experimental data from literature are also shown: Exp1: [107]; Exp2: [106]; Theo1: [65]; Theo2: [104]; Theo3: [107].

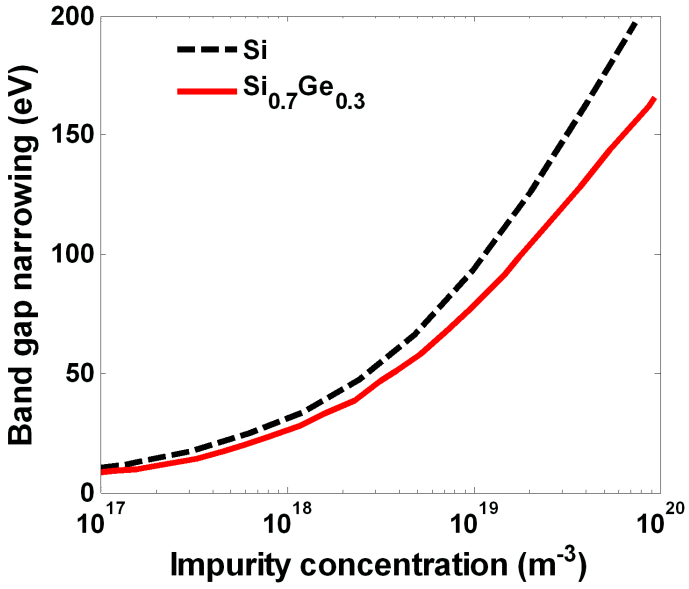


Figure 2.7: Band gap narrowing in n-doped Si and $Si_{0.7}Ge_{0.3}$ as a function of Boron doping concentration [109].

For doping concentrations less than 10^{18}cm^{-3}, the BGN for pure Si and Ge can be expressed as [110][111]:

$$\begin{cases} For\ n-type\ Si: BGN \sim 3.5\times10^{-11}.N_d^{1/3} \\ For\ n-type\ Ge: BGN \sim 8.67(N_d\times10^{-18})^{1/3}+8.14(N_d\times10^{-18})^{1/4}+4.31(N_d\times10^{-18})^{1/2} \end{cases} \tag{2.24}$$

where N_d is the doping concentration in cm^{-3}.
Because of the low BGN (up to 40mV), linear interpolation can be applied to compute the BGN of the medium doped $Si_{1-x}Ge_x$ ($N_d \sim 10^{18}\text{cm}^{-3}$).

2.2.4.2 $Si_{1-x}Ge_x/Si$ bands discontinuity

The relaxed and strained $SiGe/Si$ band alignment is illustrated in figure 2.8.

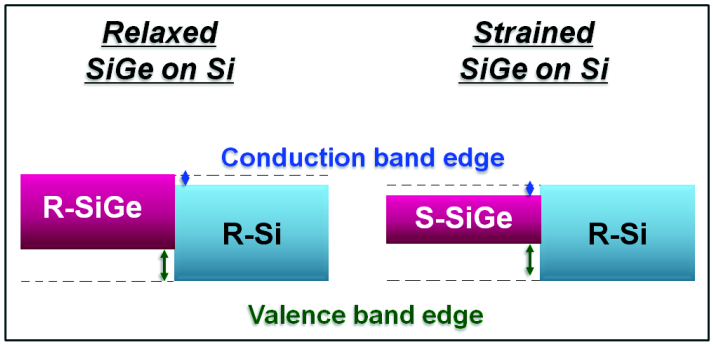


Figure 2.8: Schematics band alignment of relaxed (R) and strained (S) $SiGe/Si$.

The bands discontinuity of a Si-like biaxially strained $SiGe$ layer on unstrained (001) Si is of type I heterostructure [62]. It consists of a large valence band offset and a smaller conduction band offset.
Uptodate there are fewer reported results for the $SiGe/Si$ conduction band offset compared to the wide reporting of theoretical and experimental studies of valence band offsets [112][72].
Figure 2.9 shows good correlation between the theoretical valence band offset (ΔE_v) data and the measured one. A maximum discrepancy of 40meV around $xGe = 0.3$ is found with respect to valence band offset measurements. Figure 2.9 illustrates also the calculated valence band discontinuity of strained $Si_{1-x}Ge_x/Si$ using UTOXPP within C. Y. P. Chao and S. L. Chuang formulation [77]. The valence band offset used in UTOXPP simulations within EMA (green line) exhibits a linear behaviour with Ge content increase. This linearity is in good agreement with reported experimental and theoretical data. 240meV increase of the valence band discontinuity is noticed when integrating 30% of Ge.
The strained $Si_{1-x}Ge_x/Si$ conduction band offset (ΔE_c) is obtained by subtracting the Si bandgap from the sum of the calculated valence band offset ΔE_v and the strained $Si_{1-x}Ge_x$ bandgap (figure 2.6).
Figure 2.9 illustrates the conduction band offset variation with respect to xGe in the strained layer. The experimental results show that ΔE_c varies quasilinearly with Ge content. It is rather less than the valence band offset. Only 10meV shift is noticed for 30% Ge. Moreover, the strained $SiGe/Si$ conduction band discontinuity used in UTOXPP simulations within EMA

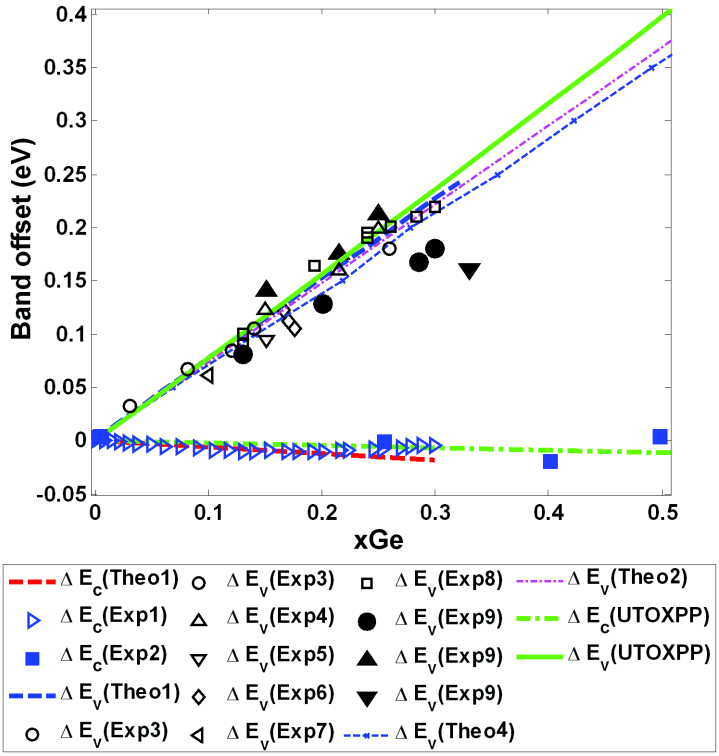


Figure 2.9: Valence and conduction band offsets of the highest valence band edge and lowest conduction band edge between the strained $Si_{1-x}Ge_x$ and Si. Results of UTOXPP model are plotted in green lines. Theoretical results and experimental data from literature are also shown: Exp1: [107]; Exp2: [106]; Exp3: [113]; Exp4: [114]; Exp5: [115]; Exp6: [116]; Exp7: [117]; Exp8: [118]; Exp9: [112]; Theo1: [65]; Theo2: [104]; Theo4: [73].

(green line) is in agreement with the reported results.

2.3 SiGe/Si heterostructure modeling

For a complete modeling of the present $SiGe/Si$ heterostructure in $SiGe$ devices, an accurate modeling of the charge density is needed.
In this part, the charge density in $Si_{1-x}Ge_x/Si$ is investigated using a 6-band k.p Poisson-Schrödinger solver. We also explore two faster solutions which will be compared to the accurate 6-level k.p model with an in-plane numerical integration in order to account efficiently for the hole density.
The simulated structure is the $SiGe/Si$ FDSOI pFET (figure 2.10). It consists of metal gate, SiO_2 gate oxide, biaxial strained $Si_{0.63}Ge_{0.27}$-layer with different thicknesses on relaxed Si ($T_{SiGe} + T_{Si} = 10nm$) and SiO_2 box on Si substrate.
In order to treat efficiently the $SiGe/Si$ heterojunction, the charge density is computed accord-

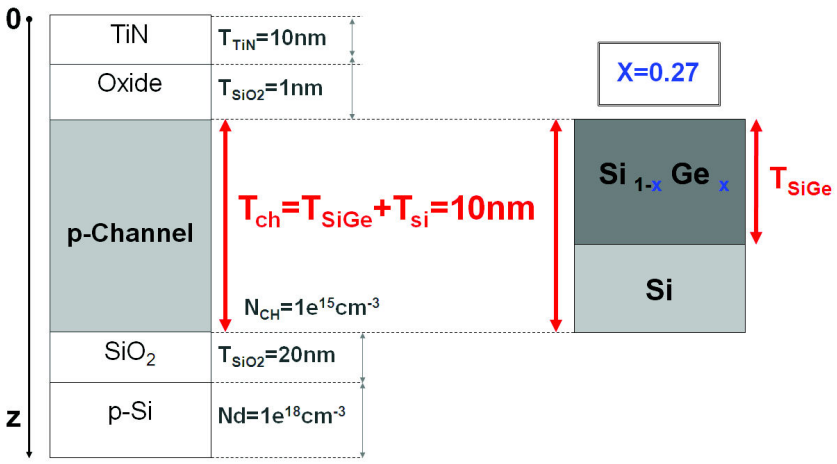


Figure 2.10: Device structure of strained $Si_{1-x}Ge_x/Si$ SOI pMOSFET.

ing to the different following methods:

(A) the 6-band k.p model with an in-plane numerical integration (exact formula). The expression of the total hole density is given by equation 2.19 on page 56.

(B) the effective mass approximation (EMA) including the effects of alloy composition and mechanical strain on the $SiGe/Si$ band structure (see subsection 2.2.2.1 on page 48). Under this approximation, the hole density is analytically integrated and written in equation 2.21 on page 57. The 2D density of states is so expressed as: $g^{2D} = \frac{M_{DOS}}{\pi\hbar^2}$. According to the used M_{DOS} value, we distinguish three methods based on the EMA:
(B1) the EMA using the 'local' DOS mass. We consider the DOS mass of $SiGe$ in the $SiGe$ and the DOS mass of Si in the Si material. The pure Ge and Si DOS masses of valence bands are given in table 2.6. $SiGe$ DOS masses are linearly interpolated.
(B2) the mean DOS mass (CEMA). Since, the Ge content varies along the device position (z), one defines a density of states mass for the v-th subband of the band "i" (M^v_{DOS}) that is calculated from the 'position dependent' in-plane DOS mass of the i-th band (table 2.6) as: $M^v_{DOS} = \frac{\int_{-\infty}^{+\infty} |\Psi_{v,i}|^2 M^i_{DOS}(z)dz}{\int_{-\infty}^{+\infty} |\Psi_{v,i}|^2 dz}$.
(B3) the mean DOS mass (CEMA (Fitted M_{DOS})) which matches the exact formula result (method (A)). In this method, the Silicon Heavy Hole M_{DOS} ($M_{DOS}(HH, Si)$) is adjusted to fit the C-V curve obtained using the exact formula method (method (A)). The HH and SO DOS masses are not modified. These are given in table 2.6.

Band	HH	LH	SO
$M_{DOS}(Si)$	$\mathbf{0.51}m_0$	$\mathbf{0.15}m_0$	$\mathbf{0.23}m_0$
$M_{DOS}(Ge)$	$\mathbf{0.042}m_0$	$\mathbf{0.042}m_0$	$\mathbf{0.042}m_0$

Table 2.6: Density of states mass (M_{DOS}) of the pure Ge and Si valence bands used in the 'EMA' simulation method.

Figure 2.11 shows the hole concentration obtained using the 6-band k.p model with a full (k_x,k_y) in-plane integration. The calculation of the hole density within the EMA using the 'local' DOS mass or the mean DOS mass (CEMA) (table 2.6), is also illustrated. Within the EMA using the 'local' DOS mass, we observe a charge discontinuity at the $SiGe/Si$ interface. The exact simulation (using exact formula (A)) of the hole density using the 6 band k.p resolution of the $SiGe/Si$ interface requires heavy CPU resources (10 hours for a full C-V curve on a 2 cores CPU INTEL i5M). Within the EMA using the mean DOS mass (CEMA method (B2)), we note that we can efficiently eliminate the heterojunction interface discontinuity. Nevertheless, the charge amplitude obtained using the CEMA method (B2) remains low compared to the exact formula result.

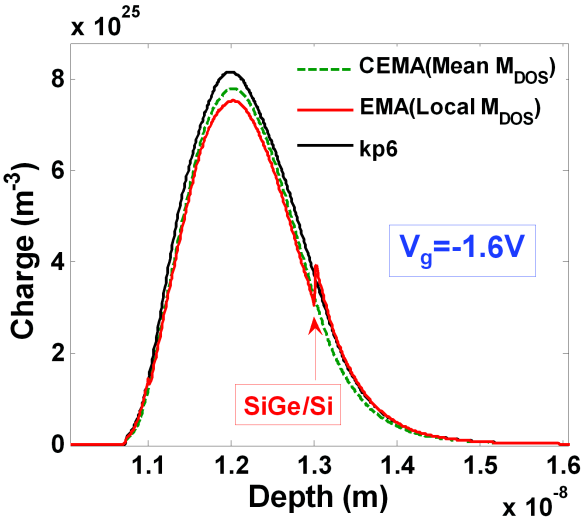


Figure 2.11: Hole density of 2nm thickness of $Si_{0.63}Ge_{0.27}$ calculated using: the 6-band k.p model with an in-plane numerical integration and EMA model using the mean DOS mass (CEMA method (B2)) and 'local' DOS mass.

In the rest of this section, we propose a simulation method based on the CEMA model to reproduce the exact formula result (method (B3)). First, the M_{DOS} will be modified in order to fit the C-V curve of the Si and $SiGe$ FDSOI pFETs. Then, the matching of the charge profile and inversion capacitance maximum value will be checked. Finally, the physical significance of the M_{DOS} adjust will be verified.
Figure 2.12 compares the simulated $Si_{0.63}Ge_{0.27}$ FDSOI pFET C-V characteristics within the exact formula and CEMA model (method (B2) using a Silicon Heavy Hole M_{DOS} ($M_{DOS}(HH, Si)$) equal to $0.51m_0$). Threshold voltage and inversion capacitance maximum values (C_{inv}^{max}) discrepancies are noticed for various T_{SiGe} thicknesses. In order to reproduce the C-V curves obtained within the exact formula, we use method (B3) with an adjusted $M_{DOS}(HH, Si)$. The exact formula C-V curve (method (A)) of pure Si is reproduced within CEMA using $2.5m_0$ $M_{DOS}(HH, Si)$. In addition, we match the exact formula result for $SiGe$ pMOS using $1.5m_0$ $M_{DOS}(HH, Si)$. Thus, increasing the $M_{DOS}(HH, Si)$ ($2.5m_0$ and $1.5m_0$ respectively for Si and $SiGe$) makes it possible to reproduce the capacitance given by the exact formula in only 20 minutes CPU time (see solid curves versus symbols).

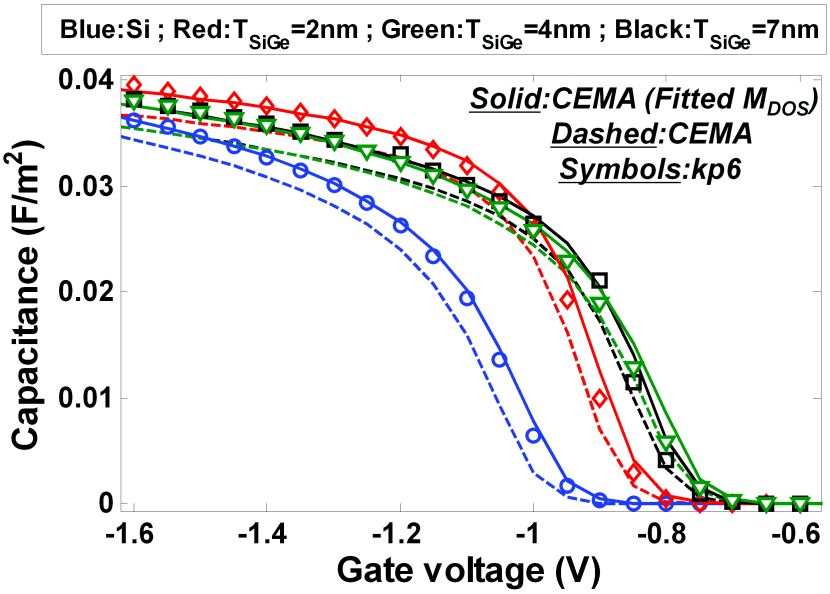


Figure 2.12: $Si_{0.63}Ge_{0.27}$ FDSOI pFET C-V computed using the exact formula and CEMA model with default ($0.51\mathrm{m}_0$) and fitted $M_{DOS}(HH, Si)$ ($2.5\mathrm{m}_0$ and $1.5\mathrm{m}_0$ respectively for Si and $SiGe$).

Figure 2.13 shows the hole density profile of the $Si_{0.63}Ge_{0.27}$ FDSOI pFET obtained using methods (A), (B2) and (B3). The result is coherent with figure 2.12. We reproduce the exact formula result (black curves) at strong inversion using the adjusted CEMA with $1.5\mathrm{m}_0$ $M_{DOS}(HH, Si)$.

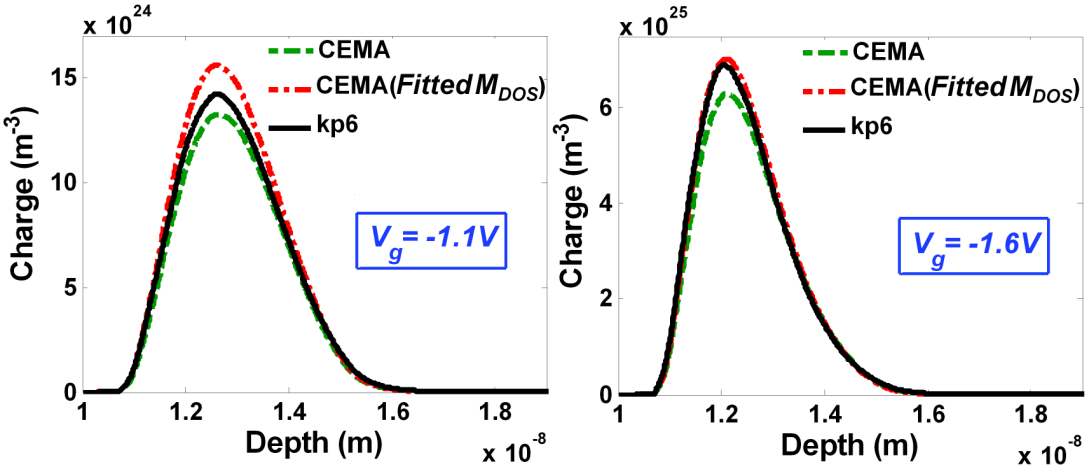


Figure 2.13: The hole density corresponding to 4nm $Si_{0.63}Ge_{0.27}$ FDSOI pFET calculated at $V_g = -1.1V$ (left figure) and $V_g = -1.6V$ (right figure) using: the 6-band k.p model with an in-plane numerical integration and CEMA with default ($0.51\mathrm{m}_0$) and fitted $M_{DOS}(HH, Si)$ ($2.5\mathrm{m}_0$ and $1.5\mathrm{m}_0$ respectively for Si and $SiGe$).

Figure 2.14 shows the inversion capacitance maximum value as a function of the $Si_{0.63}Ge_{0.27}$

thickness. We notice a good agreement between the C_{inv}^{max} computed within the exact formula and CEMA using the adjusted $M_{DOS}(HH, Si)$ (equal to $2.5m_0$ and $1.5m_0$ respectively for Si and $SiGe$). It is clear from this figure that the CEMA model with $M_{DOS}(HH, Si)$ equal to $0.51m_0$ is not efficient to predict the capacitance at strong inversion. $2\mathring{A}$ equivalent Si dark space (ε_{Si}/C_{inv}) increase is noticed proving that EOT extraction using this model should be carefully applied.
As a conclusion, in order to accurately simulate the C-V characteristic within the CEMA, the $M_{DOS}(HH, Si)$ should be increased. In the rest of this document, within the CEMA (Fitted M_{DOS}) method, $2.5m_0$ $M_{DOS}(HH, Si)$ will be used for pure Si pMOS simulations. $1.5m_0$ $M_{DOS}(HH, Si)$ will be used for all $Si_{1-x}Ge_x$ pMOS simulations in order to reproduce the exact formula C-V curve (method (A)).

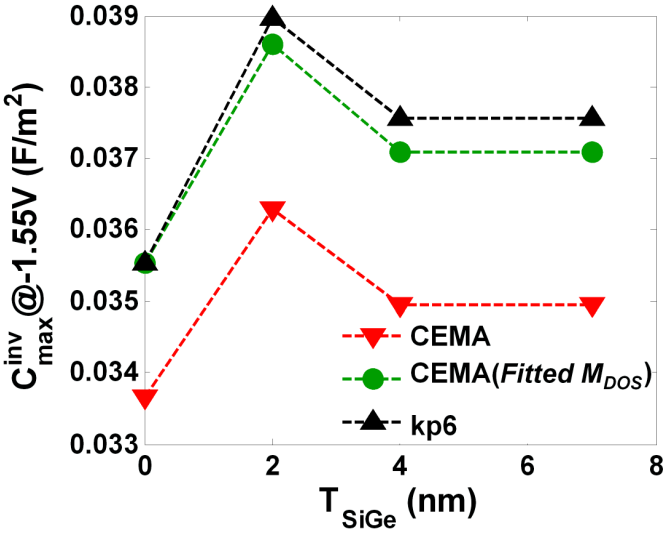


Figure 2.14: Inversion capacitance maximum values (C_{inv}^{max}) obtained using three models reported in figure 2.12.

In the following, the physical significance of the $M_{DOS}(HH, Si)$ adjust will be verified. We have compared the dispersion relation (E(k)) and DOS of the highest hole subband of the heavy hole (HH) computed for the three models reported in figure 2.12 for 10nm Si and $Si_{0.63}Ge_{0.27}$ pFETs FDSOI. Figure 2.15 shows the HH energy 3D-contour plots (obtained with the 6-bands k.p model) as a function of in-plane wave vectors for Si and $Si_{0.63}Ge_{0.27}$. The heavy hole subbands of Si and $SiGe$ are not parabolic. From this figure, we notice that 30% Ge integration affects the shape interface of the heavy hole band structure. The valence heavy hole subband energy dispersion relations, when $V_g = -2V$ is applied, is plotted in figure 2.16. We notice that using the CEMA model with $M_{DOS}(HH, Si)$ equal to $0.51m_0$ is not accurate to simulate the Si and $Si_{0.63}Ge_{0.27}$ devices. When increasing $M_{DOS}(HH, Si)$ (equal to $2.5m_0$ and $1.5m_0$ respectively for Si and $SiGe$), the CEMA model takes into account the curvature of the highest part of the heavy hole subbands. The validity of the CEMA model using the adjusted $M_{DOS}(HH, Si)$ is confirmed in figure 2.17, where the DOS computed for the first heavy hole subband is more in agreement with those obtained using the exact formula.

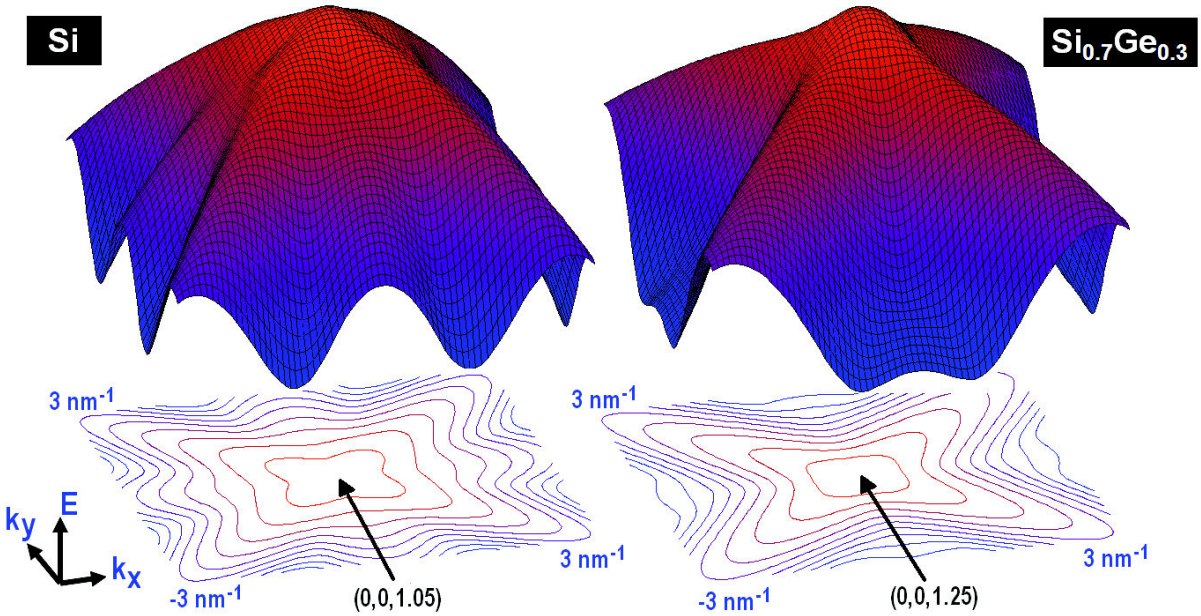


Figure 2.15: Si (right figure) and $Si_{0.63}Ge_{0.27}$ (left figure) heavy hole band structure and isoenergetic lines of the highest sub-band using the 6-band k.p model at $V_g = -2V$.

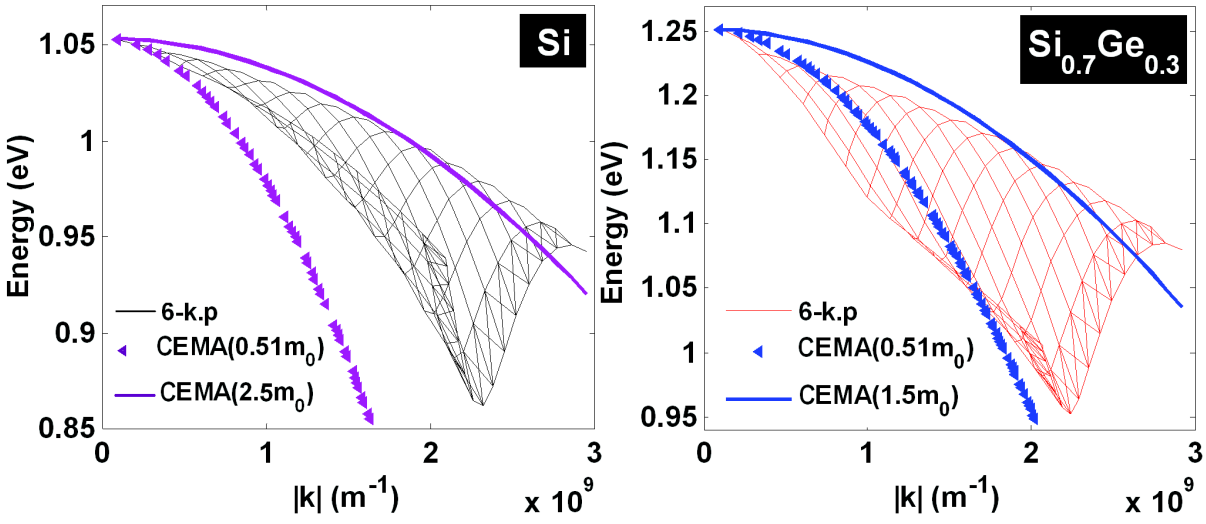


Figure 2.16: Highest hole subband energy as a function of the wave vector in Si (right figure) and $Si_{0.63}Ge_{0.27}$ (left figure) pFETs FDSOI at $V_g = -2V$.

The threshold voltage (VT) obtained from the gate capacitance (figure 2.12) is plotted as a function of the $Si_{0.63}Ge_{0.27}$ thickness in figure 2.18. Although, the CEMA with $M_{DOS}(HH, Si)$ equaling to 0.51m_0 (method (B2)) creates a different C_{inv}^{max} and charge density (as shown in figures 2.13&2.14), a relatively good agreement with the in-plane numerical integration VT is observed. However, for the pure Si, the VT obtained using (method (B2)) is shifted up to 30mV. This slight discrepancy is well explained by the nonparabolicity of the Si valence bands.

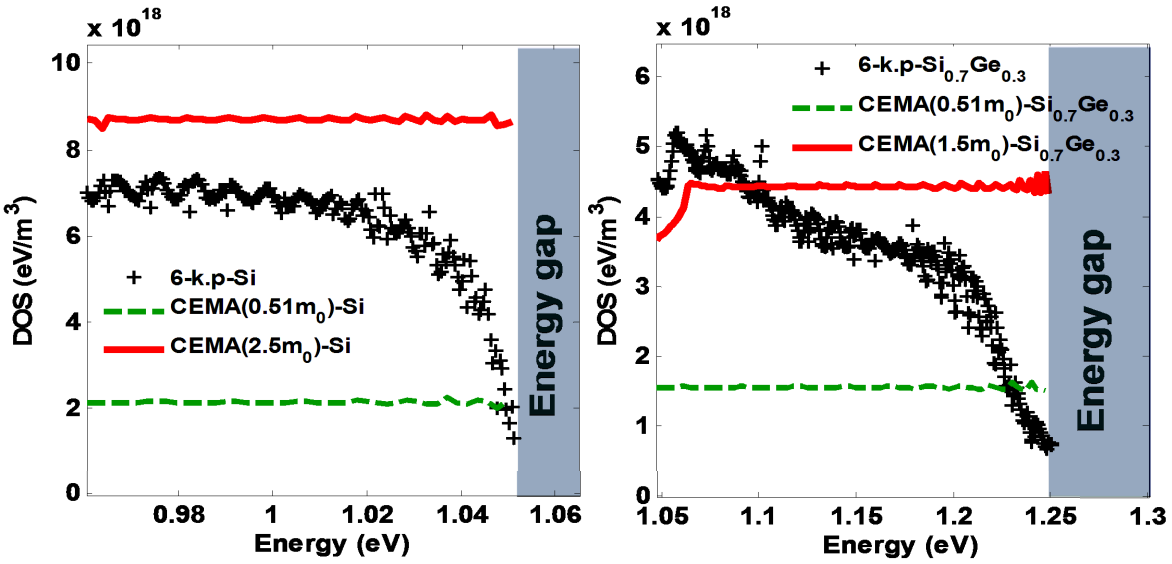


Figure 2.17: Hole DOS in the first hole subband of Si (right figure) and $Si_{0.63}Ge_{0.27}$ (left figure) pFETs FDSOI at $V_g = -2V$.

Figure 2.18 also shows the obtained VT within method (B3). The Si VT is well fitted when adjusting the $M_{DOS}(HH, Si)$ to 2.5m$_0$ (method (B3)). Increasing the $M_{DOS}(HH, Si)$ to 1.5m$_0$ allows only 15mV $SiGe$ VT discrepancy emphasizing the efficiency of this model.

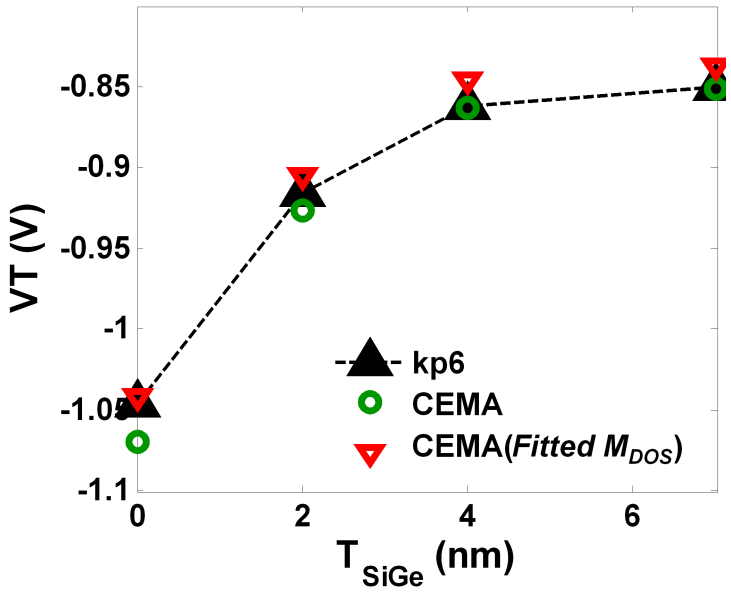


Figure 2.18: Threshold voltage (VT) of the Si ($T_{SiGe} = 0$) and $Si_{0.63}Ge_{0.27}$ obtained using the three models reported in figure 2.12.

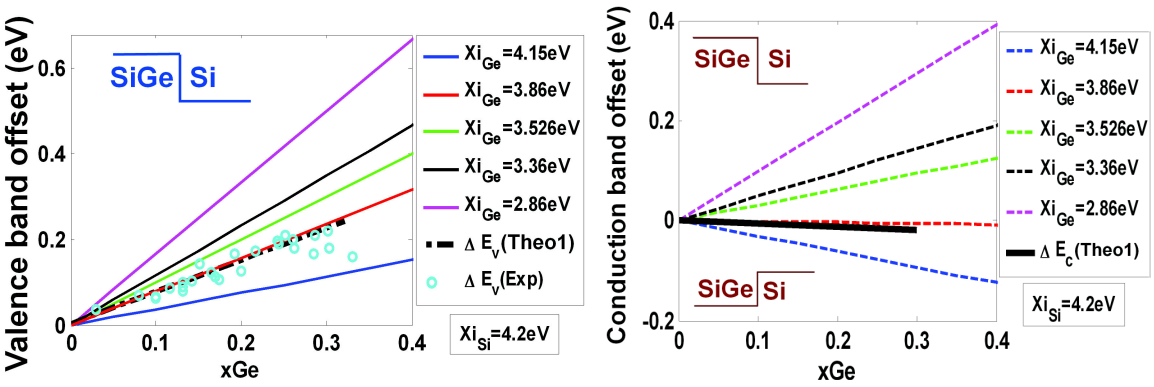
In this section, the C-V simulation of the $Si_{1-x}Ge_x/Si$ based pMOS has been investigated. Three methods based on the EMA have been compared to the 6-band k.p exact formula model (method (A)). Charge discontinuity at the $SiGe/Si$ interface and charge amplitude discrepancy proved that the EMA model (method (B1)) is not accurate to simulate the C-V of the $Si_{1-x}Ge_x/Si$ pMOS. The mean DOS mass CEMA model (method (B2)) eliminates the heterojunction interface discontinuity. Nevertheless, inversion capacitance difference is already observed. When adjusting the $M_{DOS}(HH, Si)$ to 2.5m$_0$ (method (B3)) for Si C-V simulations, we have obtained a good fit of the charge amplitude and C-V curve. The CEMA method with the $M_{DOS}(HH, Si)$ equal to 1.5m$_0$ (method (B3)) reproduces the $SiGe$ exact formula results (method (A)). The highest HH subband and the DOS obtained using method (B3) for the Si and $Si_{0.63}Ge_{0.27}$ are found in good agreement with the 6-band k.p result. This proves that increasing the $M_{DOS}(HH, Si)$ has a physical significance emphasizing the accuracy of the method (B3).

2.4 SiGe-based pFETs and C-V characteristics

Due to the efficient and fast way to treat the $SiGe/Si$ heterostructure, we will perform the rest of our study using the CEMA method (B3). In order to match the exact formula results, the $M_{DOS}(HH, Si)$ is taken equal to $2.5m_0$ and $1.5m_0$ respectively for Si and $Si_{1-x}Ge_x$ simulations. In this section, we investigate the $SiGe$ simulation parameters impact on the C-V characteristic. This investigation allows to determine the most important simulation parameters that should be carefully considered to accurately simulate the $SiGe$ C-V curve.
To this end, we vary the following $SiGe$ parameters: (a) ΔE_c and ΔE_v bands offset, (b) $SiGe$ strain, (c) Ge profile effects, (d) $SiGe$ dopant concentration and (e) Ge concentration and $SiGe$ thickness.

2.4.1 Bands offset effects

These were wide of published experimental and theoretical data of strained $SiGe$ energy band gap (see subsection 2.2.4.1). Thus, in this study the $SiGe$ band gap is keeped constant as plotted in figure 2.6. But, conduction and valence band discontinuity of $SiGe/Si$ are varied by Ge electron affinity modification.
Here we study the impact of the valence and conduction bands offset variation on the C-V characteristic of the $SiGe/Si$ pMOSFET. To do so, we consider the 8nm $Si_{0.7}Ge_{0.3}/Si$ pMOSFET. Keeping constant the $SiGe$ band gap energy (figure 2.6), we vary the Ge electron affinity (χ_{Ge}). This variation induces strained $SiGe/Si$ valence and conduction bands level modulation. ΔE_v is increased from 100meV to 500meV (figure 2.19.a). ΔE_c varies from -100meV to 300meV (figure 2.19.b). The obtained C-V curves are plotted in figure 2.20. The ΔE_v increase is illustrated by up to 400mV bias threshold shift of capacitance inversion. The ΔE_c increase induces an accumulation capacitance deformation. As a conclusion, the conduction and valence bands offset are key parameters to simulate the C-V of the $SiGe$ based devices.



(a) (b)

Figure 2.19: Keeping constant the $SiGe$ band gap energy (figure 2.6), the Ge electron affinity (χ_{Ge}) variation implies $SiGe$ bands level change. This figure shows the $Si_{0.7}Ge_{0.3}$ electron affinity variation impact on the valence (a) and conduction (b) bands offset. Here, the reported electron affinities correspond to relaxed values.

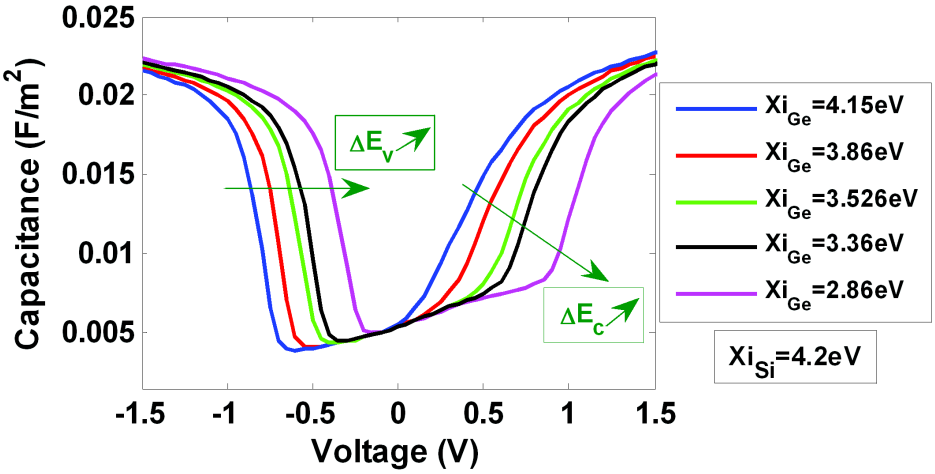


Figure 2.20: $Si_{0.7}Ge_{0.3}/Si$ valence and conduction bands offset variation (figure 2.19) impact on the 8nm $Si_{0.7}Ge_{0.3}$ pMOSFET C-V characteristic. Here, the reported electron affinities correspond to relaxed values.

2.4.2 *SiGe* strain effects

We have compared the simulated C-V response of the relaxed, partially strained (strained along one in plane axis) and biaxially strained $Si_{0.7}Ge_{0.3}$ pMOSFETs. The corresponding strain tensor of each simulation is given in table 2.7. Figure 2.21 shows the obtained C-V characteristics. Slight effect is noticed when the $SiGe$ is strained along the y axis only. In addition, applying biaxially strain on the $SiGe$ affects especially the accumulation capacitance. Whereas, the inversion capacitance and so the VT do not depend on the strain. This is coherent with the strain impact on the $SiGe$ conduction and valence bands offset illustrated in figure 2.22. It is clear from this figure that the strain decreases the $Si_{0.7}Ge_{0.3}$ conduction band offset up to

110meV. However, only 10mV increase is observed for the valence band offset.

	ε_{xx}	ε_{yy}	ε_{zz}
Relaxed SiGe	**0**	**0**	**0**
Partially strained SiGe	**0**	**-0.0112**	**0**
Strained SiGe	**-0.0112**	**-0.0112**	**0.0086**

Table 2.7: Strain tensor of the relaxed, partially strained and biaxially strained $Si_{0.7}Ge_{0.3}$ on Si.

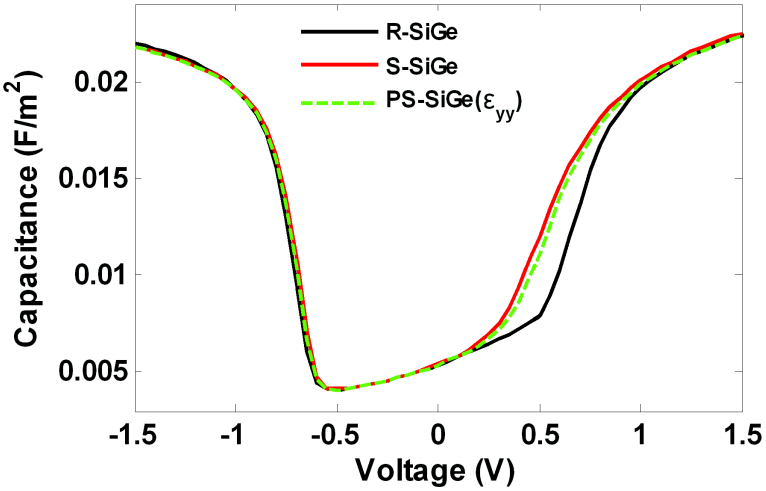


Figure 2.21: C-V of the relaxed (R), partially strained (PS) and strained (S) 8nm $Si_{0.7}Ge_{0.3}$ pMOSFETs.

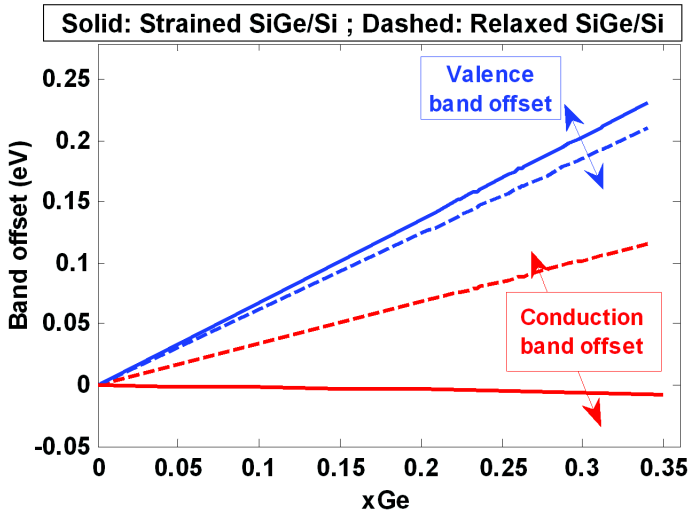


Figure 2.22: Strained (solid) and relaxed (dashed) $SiGe/Si$ conduction and valence bands offset.

2.4.3 *Ge* profile effects

Actually, in $SiGe/Si$ devices, the heterojuction is not abrupt. In fact, there is a Ge concentration gradient at the $SiGe/Si$ interface.
Here, we investigate the $SiGe/Si$ heterojunction impact on the C-V curve of the $Si_{0.7}Ge_{0.3}$ pMOSFET. Figure 2.23 illustrates the simulated Ge profile at the $SiGe/Si$ heterojuction. The resulting C-V are plotted in figure 2.24. We notice that the gradual $Si_{0.7}Ge_{0.3}/Si$ heterojunction variation slightly affects the C-V characteristic only in the accumulation regime. Besides, the inversion capacitance is independent of the Ge profile at the $SiGe/Si$ heterojunction. Thus, considering an abrupt $SiGe/Si$ junction is a valid approximation to efficiently simulate the C-V characteristic of the $SiGe/Si$ pFETs.

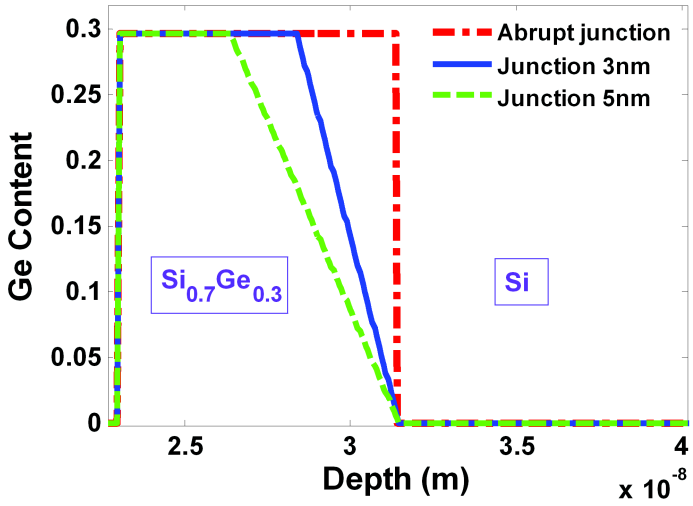


Figure 2.23: The the Ge profile at the $Si_{0.7}Ge_{0.3}/Si$ heterojunction.

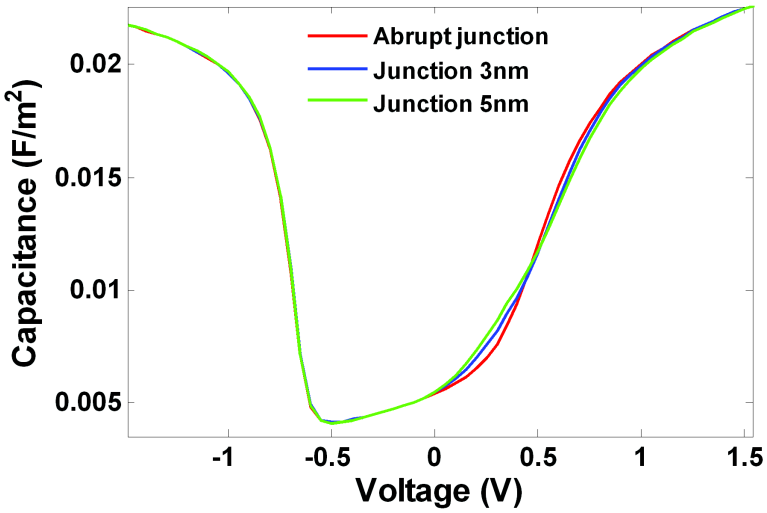


Figure 2.24: The $Si_{0.7}Ge_{0.3}/Si$ junction impact on the C-V characteristic of the 8nm $Si_{0.7}Ge_{0.3}$ pMOSFET.

2.4.4 *SiGe* dopant concentration effects

We consider a 8 nm $Si_{0.7}Ge_{0.3}$ pMOSFET. The *SiGe* is epitaxied on (100) *Si*. Indeed, the Boron implantation has a gaussian profile in the *Si* substrate. After the spike anneal, slight diffusion of dopant in the *SiGe* layer is expected. Here, we study the impact of the diffused Boron dopant (in the *SiGe* layer) on the C-V curve. To do so, we have considered three *SiGe* doping concentrations ($N1 < N2 < N3$) as shown in figure 2.25. The simulated C-V shows only 20mV VT decrease when we reduce the *SiGe* doping (from N1 to N2). Moreover, increasing the *SiGe* dopage to N3 concentration increases the VT up to 100mV.

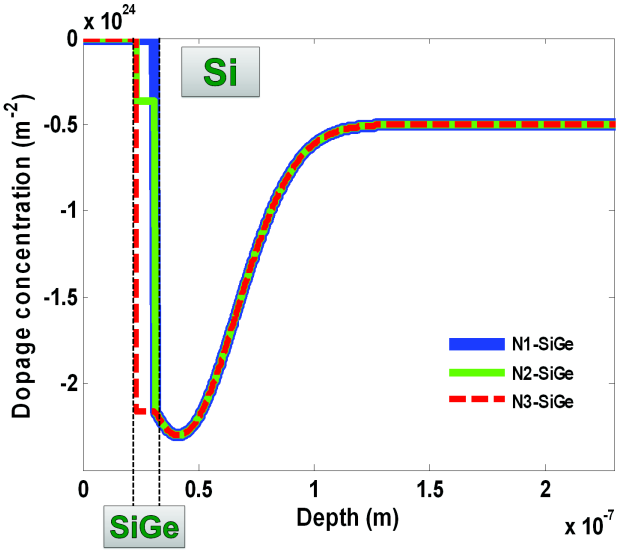


Figure 2.25: Dopant concentration profile.

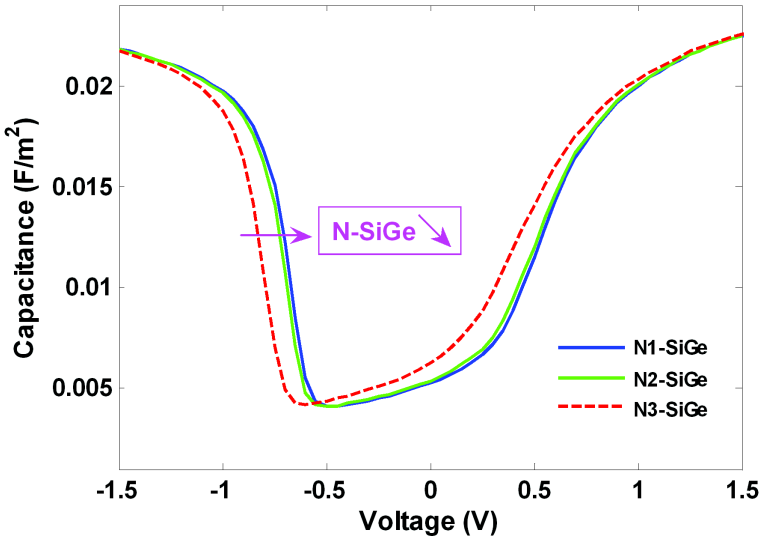


Figure 2.26: *SiGe* dopant concentration profile impact on the 8nm $Si_{0.7}Ge_{0.3}$ pMOSFET C-V.

2.4.5 *Ge* concentration and *SiGe* thickness effects

Figure 2.27 presents the gate capacitance as a function of the gate voltage for various *Ge* content (xGe= 0, 0.07, 0.17, 0.27, 0.37) of strained 7.5nm $Si_{1-x}Ge_x$ layer. From this figure, it can be seen that the threshold voltage is influenced by changing the *Ge* mole fraction. Since the valence band offset enhances as *Ge* content increases (see figure 2.9), holes are confined at the strained $Si_{1-x}Ge_x$ valence band. So, inversion can occur even at lower gate voltage. As a result, increasing *Ge* concentration shifts the VT up to 300mV for xGe=0.37. Whereas, the C-V seems insensitive to the xGe increase in the accumulation regim. This is consistent with the quasi constant conduction band offset variation with the *Ge* concentration (see figure 2.9).

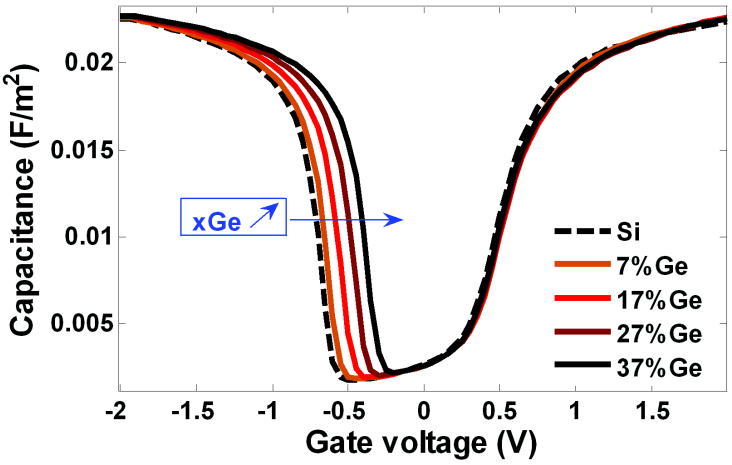


Figure 2.27: C-V of strained $Si_{1-x}Ge_x$/relaxed *Si* pMOSFET (0≤xGe≤0.37, T_{SiGe}=7.5nm).

Figure 2.28 shows a nearly linear variation of VT with the *Ge* content for the various *SiGe* layer thicknesses. This is consistent with the behaviour of the band offset with the *Ge* concentration.

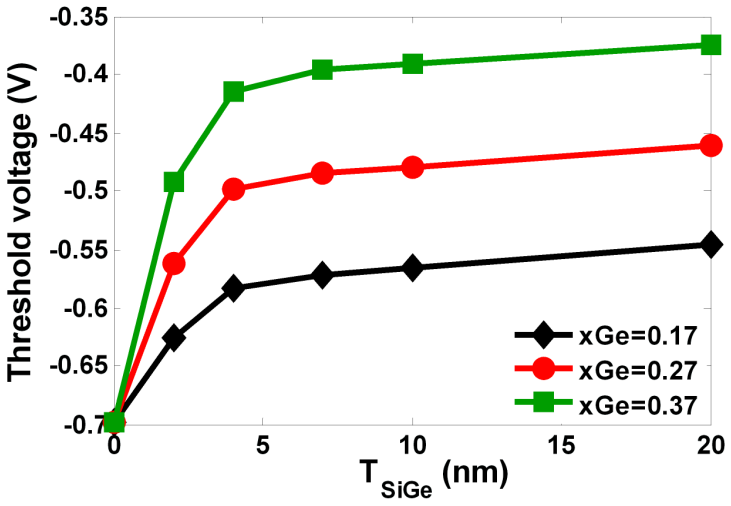


Figure 2.28: The threshold voltage as a function of the $Si_{1-x}Ge_x$ thickness.

As the $Si_{1-x}Ge_x$ layer thickness increases, the VT saturates to a constant for $T_{SiGe} \geq 5nm$ at a level corresponding to the valence band offset (see figure 2.9). This is clearly observed on the C-V curves (figure 2.29). Only 35mV inversion capacitance shift is noticed when increasing T_{SiGe} from 5nm to 20nm.

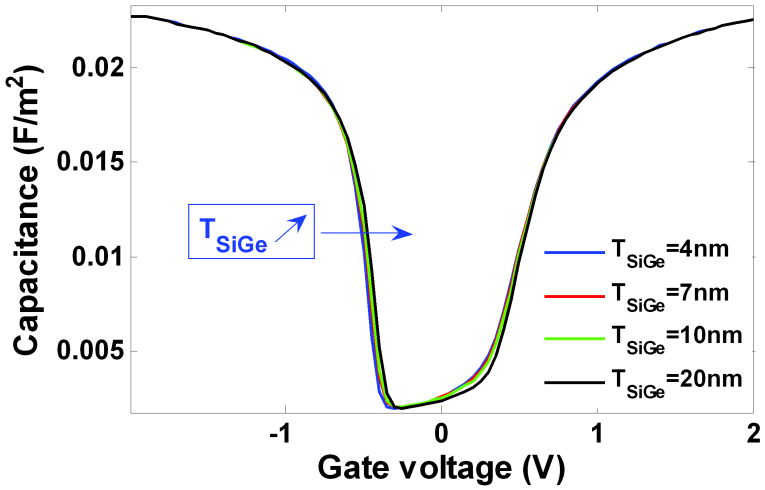


Figure 2.29: C-V of strained $Si_{0.73}Ge_{0.27}/Si$ pMOSFET for various T_{SiGe} thicknesses.

2.5 Conclusion

In this chapter, we have described the strained $SiGe/Si$ band structure in section 2.2. We have reported basic equations of the deformation potential approximation (implemented in the CEMA model) and the 6-band k.p model for the strained $SiGe$ valence bands. The strained $SiGe/Si$ conduction and valence bands computed using the deformation potential approximation (CEMA model) are in good agreement with the 6-k.p result validating such approximation. Moreover, strained $SiGe$ bands offset and energy band gap computed using UTOXPP solver are compared to published experimental and theoretical results. The comparison has proved that the strain is well taken into account in UTOXPP band structure models.
In order to account efficiently for the hole density, in section 2.3 we have compared three solutions based on the effective mass approximation to the accurate 6-level k.p model with an in-plane numerical integration (exact formula). The exact C-V is efficiently reproduced using the CEMA when increasing the $M_{DOS}(HH, Si)$ ($M_{DOS}(HH, Si)$ is equal to $2.5m_0$ and $1.5m_0$ respectively for Si and $SiGe$.).
Section 2.4 has investigated different $SiGe$ simulation parameters impact on the C-V characteristic of the $SiGe/Si$ pMOSFETs. It is clear from this study that considering an abrupt $SiGe/Si$ junction is a valid approximation to efficiently simulate the C-V characteristic of the $SiGe/Si$ pFETs. The strain affects especially the $SiGe/Si$ conduction band offset. Whereas, the valence band offset seems insensitive to the strain. As a result, the stress application modifies the C-V only in the accumulation regime. The variation of the Ge concentration for various strained $SiGe$ layer thicknesses shows a linear VT variation of the $SiGe$ pMOSFET. As the $Si_{1-x}Ge_x$ layer thickness increases, the VT saturates to a level corresponding with the valence band offset.

Chapter 3

VT, VFB and EOT parameters extraction

Contents

3.1 Introduction

Threshold voltage engineering is a key issue in bulk CMOS technology development. To optimize the bulk pMOS threshold voltage, strained Silicon Germanium on Silicon buffer layer has been successfully introduced in sub 32nm industrial process [21]. Recently, Fully Depleted (FD) SOI pMOSFETs has successfully integrated ultrathin $Si_{1-x}Ge_x$ layers in the channel [32]. The threshold voltage (VT) control in such devices firstly requires an accurate VT extraction.
Generally, in bulk structures, the threshold voltage and flat band voltage (VFB) parameters are extracted from capacitance versus voltage (C-V) characteristic in depletion to accumulation using e.g. the Maserjian function [119]. Recently, a new VT parameter extraction methodology using split C-V has been proposed for FDSOI MOS devices [120].
In the first part of this chapter, we dsicuss the applicability of the VT extraction method presented in [120] to extract VT and VFB parameters in $Si_{1-x}Ge_x/Si$ bulk pMOSFETs. A new EOT extraction technique based on the inversion capacitance versus inversion charge curve will be presented and suggested. The VT, VFB and EOT extraction methods will be first validated by PS simulations and then applied to C-V measurements.
The second part of this chapter mainly focuses on the EOT determination. To this end, the new EOT extraction technique, presented in the first part, will be generalized for FDSOI devices. Using Poisson-Schrödinger simulations, firstly the universal behaviour of the inversion capacitance as a function of inversion charge response will be verified for the Si and $InGaAs$ FDSOI nFETs. Basic priciples of $InGaAs$ C-V simulation will be also investigated. Secondly, the EOT extraction method will be validated by simulations for the Si and $Si_{1-x}Ge_x$ FDSOI pFETs. Finally, we will apply the extraction method to measured C-V of the FDSOI n and pFETs.

3.2 Validation of parameters extraction methods

In this part, we propose simple and efficient methods based on the split C-V to extract the VT, VFB and EOT in $Si_{1-x}Ge_x/Si$-based bulk pMOSFETs. To this end, first the VT extraction method proposed in [120] for FDSOI devices will be presented for bulk pMOSFETs and validated by PS simulations. Second, the Ge impact on the inversion capacitance will be investigated. Then, we will apply the VT and VFB extraction technique on the measured C-V of $Si_{1-x}Ge_x/Si$ bulk pMOSFETs. Finally, a new technique to extract the EOT will be presented and successfully applied to measurements.

3.2.1 Validation of VT and VFB extraction method

In this subsection, we will start by the discription of simulated structures and simulation models. The C-V simulations of the bulk pMOSFETs will be used first to validate the VT and VFB extraction method [120]. Then, simulations of the Si and $SiGe$ pMOSFETs will allow the investigation of the Ge impact on the inversion capacitance response.

3.2.1.1 Device structure

The general simulated $Si_{1-x}Ge_x/Si$ pMOSFET structure is presented in figure 3.1 (see structure -2-). It consists of metal gate with a fixed TiN work function ($WFM = 4.72eV$), a bilayer

dielectric composed of a beveled $SiON$ layer (with a T_{IL} thickness equal to 13.7$\mathring{A}$) above an $HfSiON$ dielectric and a biaxially strained $Si_{1-x}Ge_x$ layer (with variable T_{SiGe} thickness and xGe content) on relaxed n-doped Si substrate.
In this study, we will simulate two $Si_{1-x}Ge_x/Si$ pMOSFET structures with different $SiGe$ layers: the $Si_{0.7}Ge_{0.3}/Si$ bulk pMOSFET (Structure -2- with $T_{SiGe} = 80\mathring{A}$ and $xGe = 0.3$) and the pure Si pMOSFET (without $SiGe$ layer: $T_{SiGe} = 0\mathring{A}$, see structure -1-).

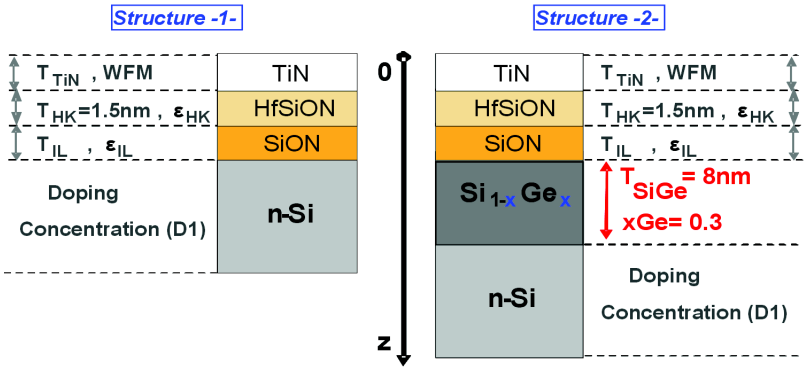


Figure 3.1: Device structure of the biaxially strained $Si_{1-x}Ge_x/Si$ pMOSFET.

3.2.1.2 Simulation Models

The simulations are based on the self-consistent solution of one dimensional Poisson and Schrödinger equations (PS.UTOXPP). In order to accurately model the charge distribution in z-direction (perpendicular to the $SiGe/Si$ interface), the charge density is computed according to the different following methods (see section 2.3 in chapter 2 on page 61 for more details):
(a) the 6-band k.p model with an in-plane numerical integration (exact formula),
(b) the effective mass approximation (CEMA) including the effects of alloy composition and mechanical strain on the $SiGe/Si$ band structure [72][77].

3.2.1.3 VT and VFB extraction method

Recently, a VT extraction method based on gate-to-channel capacitance has been proposed for FDSOI MOS devices [120]. Here, we assess the relevance of this method for bulk pMOSFETs. Simulations of the split C-V capacitance (the gate-to-channel and gate-to-bulk substrate capacitances) will be used to present and verify the extraction method of the VT and VFB of bulk pMOSFETs. In the following, the VT and VFB extraction method will be called "split C-V extraction technique".
Before applying the "split C-V extraction technique" to experimental C-V data, it will be verified by numerical simulation using the simulation methods described in the previous subsection ((a) and (b) simulation models). First, the "exact formula" result will be reproduced using the CEAM model with the adjusted MDOS(HH,Si) (see section 2.3 in chapter 2). Then, we will extract the VT and VFB parameters from the simulated split C-V of the Si and $Si_{0.7}Ge_{0.3}/Si$ bulk pMOSFETs. Finally, the extracted parameters will be validated by comparison to those

determined using commonly extraction methods.

Typical variation of the gate-to-channel capacitance (CGC) and gate-to-bulk substrate capacitance (CGB) with the gate voltage of the Si pMOSFET calculated using CEMA is compared to the split C-V computed using the "exact formula" (kp6 + Full Mesh) (figure 3.2.a). A slight difference between the capacitance obtained using the CEMA with a MDOS(HH,Si) equal to $0.51m_0$ (m_0 is the electron mass) and "exact formula" is observed in the inversion region. Increasing the MDOS(HH,Si) to $2.5m_0$ makes it possible to reproduce the CGC given by the "exact formula" in only 20minutes CPU time. This result confirms those obtained in section 2.3 (see page 61).
The derivative of CGC with respect to gate voltage (CGC') passes through a maximum, defining VT as for the usual definition of VT in MOSFETs from the derivative of the transconductance $g_m(V_g)$. The variation of the derivative of CGB with respect to gate voltage (CGB') has two maximums corresponding to VT and VFB. As can be seen from figure 3.2 (b and c), the simulated Si pMOS CGC' and CGB' enable to localize a VT value from the CGC' maximum peak position and a VFB value from the CGB' second peak location (for Si pMOS, VT_{Si}=-0.95V and VFB_{Si}=0.45V).

This extraction method has been applied to the $Si_{0.7}Ge_{0.3}/Si$ pMOSFET. The split C-V (CGC and CGB) obtained using the two simulation methods (CEMA and "exact formula") is reported in figure 3.3. The obtained CEMA CGC matches the exact CGC using MDOS(HH,Si) equal to $1.5m_0$. The $Si_{0.7}Ge_{0.3}/Si$ pMOS CGC' and CGB' are illustrated in figure 3.3.b. The CGC' maximum peak position gives the VT_{SiGe} ($VT_{SiGe} = -0.7V$). The VFB_{SiGe} is extracted from the CGB' second maximum peak location ($VFB_{SiGe} = 0.45V$). The extracted VT for Si and $Si_{0.7}Ge_{0.3}/Si$ pMOS is in good agreement with the VT obtained at 40% of $C_{max,inv}$, the maximum capacitance at strong inversion (see subsection 1.2.1.4 on page 21). The VT@40% of $C_{max,inv}$ is found equal to -0.95V and -0.7V, respectively for Si and $Si_{0.7}Ge_{0.3}/Si$ pMOS (This extraction method will be validated in subsection 4.2.1 in chapter 4.).
A shift up to 30mV is noticed between the VFB_{Si} and VFB_{SiGe} parameters given by the CGB' maximum peak location and the classical VFB extracted at zero substrate charge (VFB(Q=0)), found here at 0.45V and 0.42V, respectively for Si and $Si_{0.7}Ge_{0.3}/Si$ pMOS. This discrepancy is due to the simulation gate voltage step parameter (ΔV). It is reduced to 10mV with a 10mV ΔV ($VFB_{Si} = 0.44V$ and $VFB_{SiGe} = 0.42V$) (figure 3.4), confirming the consistency of the extraction method.

The simulation extracted parameters show that the inclusion of 30% of Ge in the channel reduces the VT of 0.3V. Whereas the VFB seems quite insensitive to the Ge content increase, VFB is shifted by only 20mV. Due to its efficient and fast way to simulate C-V, we will perform the rest of this study with the CEMA simulation method using the MDOS(HH,Si) equal to $2.5m_0$ and $1.5m_0$ respectively for Si and $Si_{0.7}Ge_{0.3}/Si$ pMOS.

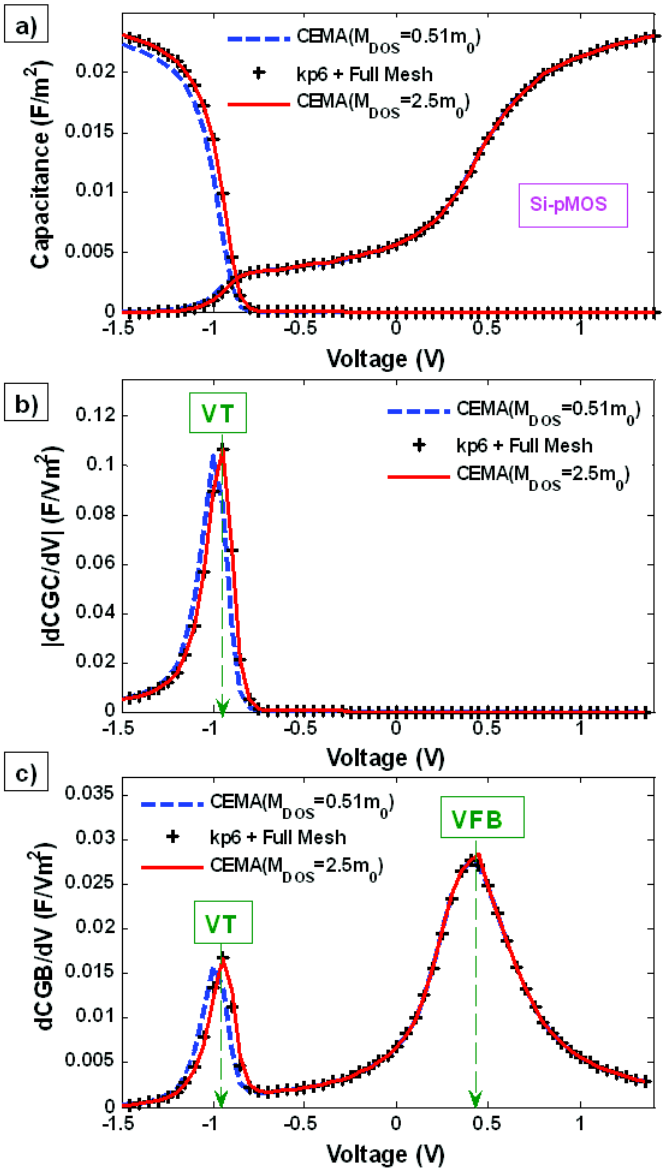


Figure 3.2: Simulated *Si* pMOS split C-V (a) leading to the VT and VFB extraction from CGC' (b) and CGB'(c).

3.2.1.4 Inversion layer capacitance and dark space

In this subsection, we investigate the inversion capacitance dependence on the *Ge* concentration. To this end, the simulated inversion capacitance of the *Si* and *SiGe* bulk pMOSFETs will be compared. The *Ge* impact on the equivalent Silicon dark space will be also studied.
The inversion layer capacitance is defined as:

$$C_{inv}(Q_{inv}) = \frac{\partial Q_{inv}}{\partial \psi_s} \tag{3.1}$$

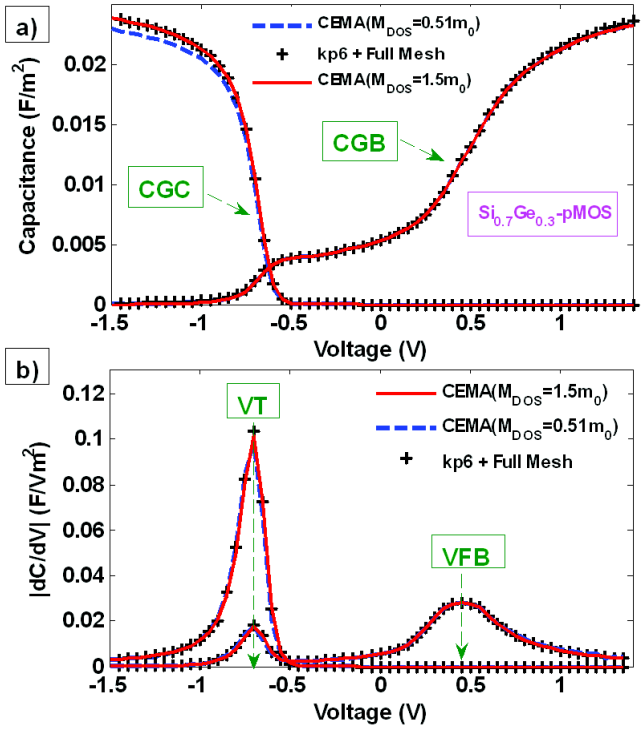


Figure 3.3: Simulated $Si_{0.7}Ge_{0.3}/Si$ pMOS split C-V (a) allowing the VT and VFB extraction from CGC' and CGB' (b).

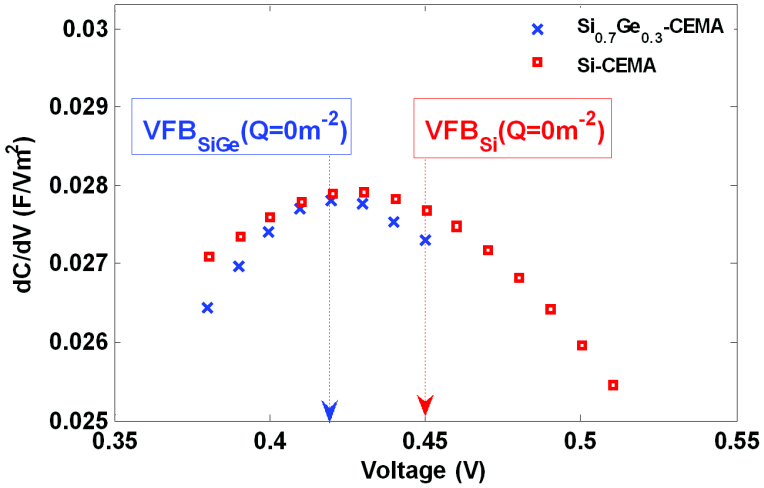


Figure 3.4: Comparison of the simulated CGB' maximum peak ($\Delta V = 10mV$) and the conventional VFB at zero substrate charge for Si and $Si_{0.7}Ge_{0.3}/Si$ pMOS.

where Q_{inv} is the inversion charge and ψ_s is the corresponding surface potential. The variations of the simulated semiconductor capacitance in the inversion regime (C_{inv}) with the inversion charge (Q_{inv}) of the Si and $Si_{0.7}Ge_{0.3}/Si$ pMOS are plotted in figure 3.5. It is clear from this figure that the obtained C_{inv} of the Si and $Si_{0.7}Ge_{0.3}/Si$ pMOS are very close. Introducing 30%

of Ge decreases C_{inv} by only 4% at strong inversion, whereas they are equal in weak inversion.

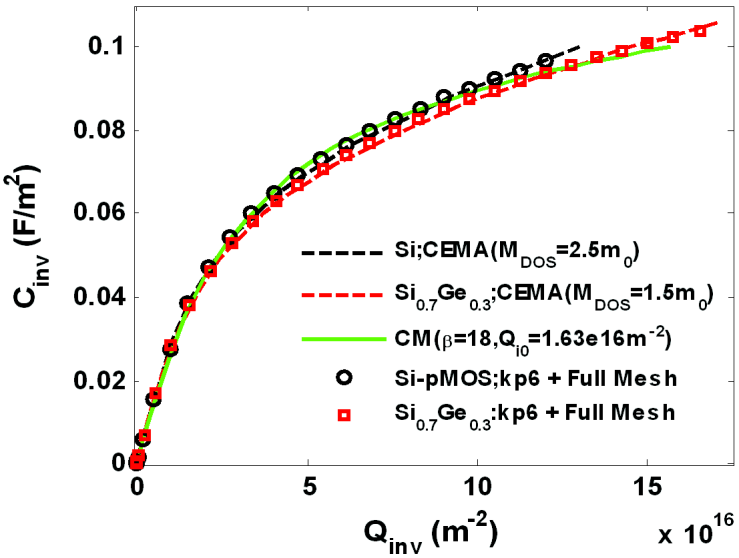


Figure 3.5: Simulated inversion capacitance (C_{inv}) versus Q_{inv} of the Si and $Si_{0.7}Ge_{0.3}/Si$ pMOS.

The 4% C_{inv} decrease is probably due to the dopage concentration discrepancy between the Si and $SiGe$ pMOSFETs. The comparison of the C_{inv} of the Si and $SiGe$ pMOSFETs doped at $10^{17}cm^{-3}$ and $10^{18}cm^{-3}$ shows that the curves for Si and $SiGe$ are close at the same dopage concentration (figure 3.6). It is clear from figure 3.6 that the impact of the doping concentration variation on the C_{inv} is more noticeable than the Ge integration one.
Here, we propose a simple analytical formula (CM) to model C_{inv} as a function of Q_{inv}:

$$C_{inv,CM}(Q_{inv}) = \beta.q.Q_{i0}.\sqrt{\log\left[1+\left(\frac{Q_{inv}}{Q_{i0}}\right)^2\right]} \tag{3.2}$$

where β and Q_{i0} are adjusted parameters. The obtained $C_{inv,CM}$ is reported in figure 3.5. The simulated $C_{inv}(Q_{inv})$ data are well fitted using the same adjusted value of β in the linear region ($\beta = 18/V$) for both Si and $Si_{0.7}Ge_{0.3}/Si$ pMOS. Since, the simulated C_{inv} are only slightly different in strong inversion, the same adjusted value of Q_{i0} ($Q_{i0} = 1.63 \times 10^{16}m^{-2}$) is used for both Si and $SiGe$ pMOS.
Now, we want to study the Ge impact on the equivalent Silicon dark space.
The equivalent Si dark space is calculated for the Si and $Si_{0.7}Ge_{0.3}/Si$ pMOS as:

$$DarkSpace(Q_{inv}) = \frac{\epsilon_{Si}}{C_{inv}(Q_{inv})} \tag{3.3}$$

The computed dark space is plotted as a function of Q_{inv} in figure 3.7. The incorporation of 30% of Ge increases the dark space by only 0.4$\mathring{A}$ at strong inversion. The dark space of the

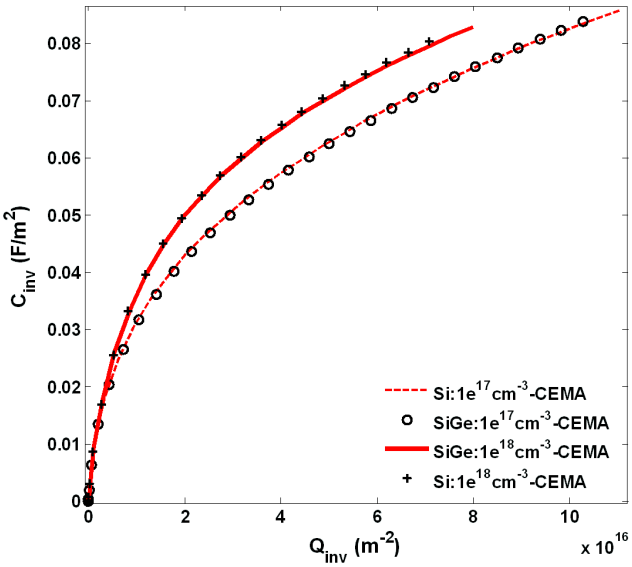


Figure 3.6: Simulated inversion capacitance (C_{inv}) versus Q_{inv} of the Si and $Si_{0.7}Ge_{0.3}$ pMOS doped at $10^{17}cm^{-3}$ and $10^{18}cm^{-3}$ (EOT=2nm).

$Si_{0.7}Ge_{0.3}/Si$ pMOS obtained without the Wave Function Penetration into the oxide (W/O WFP) is also reported in figure 3.7. A 1.7$\mathring{A}$ reduction of dark space is noticed, highlighting the impact of the WFP. It is also clear from this figure that the impact of the wave function penetration on the dark space is more noticeable than the Ge integration one.

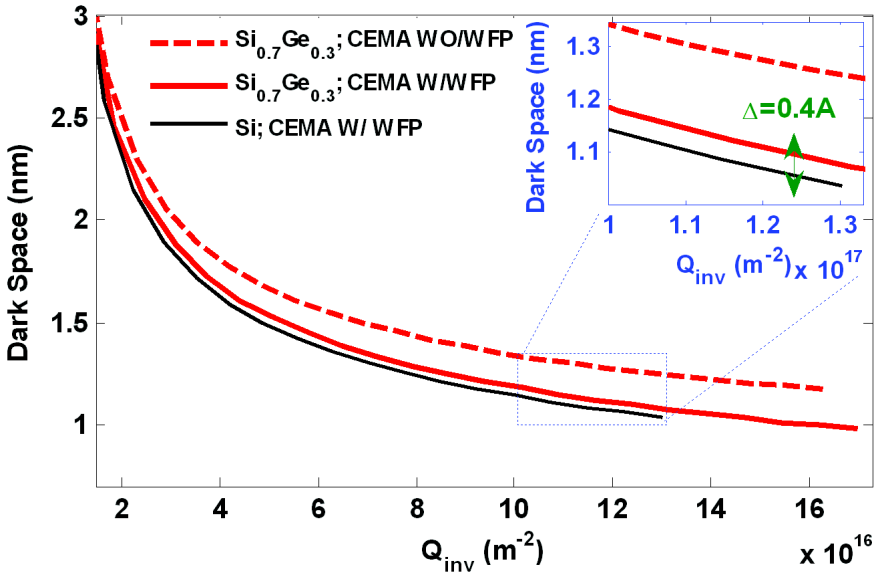


Figure 3.7: Equivalent Silicon dark space as a function of Q_{inv}.

As a conclusion, we have shown that the $C_{inv}(Q_{inv})$ curve is quasi universal for the Si and $Si_{0.7}Ge_{0.3}/Si$ bulk pMOSFETs. The impact of the doping concentration variation on the C_{inv} is more noticeable than the Ge integration one. Moreover, we have illustrated that the equivalent

Si dark space increases by only $0.4\mathring{A}$ at strong inversion when integration 30% of Ge in the channel. The wave function penetration on the dark space is more noticeable than the Ge integration one.

3.2.2 Application of parameters extraction methods on measurements

The VT and VFB extraction method has been applied to measured split C-V carried out on Si and $Si_{0.7}Ge_{0.3}/Si$ pMOS ($surface \geq 1\mu m^2$). Figure 3.8.a shows the measured CGC and CGB versus gate voltage. As indicated in the subsubsection 3.2.1.3, the derivative of the split C-V (CGC' and CGB') can further be used to determine VT and VFB. The measured VT and VFB are so extracted respectively from the measured CGC' and CGB' (figure 3.8.b). The extracted VT and VFB of the Si and $Si_{0.7}Ge_{0.3}/Si$ pMOSFETs are illustrated in table 3.1. We also report (in table 3.1) the obtained VT and VFB from the simulated CGC' and CGB' of the Si and $Si_{0.7}Ge_{0.3}/Si$ pMOSFETs (see subsection 3.2.1.3).

	Si	**$Si_{0.7}Ge_{0.3}/Si$**
Simulated VT	-0.95	-0.7
Simulated VFB	0.44	0.42
Measured VT	-0.95	-0.5
Measured VFB	0.42	0.67

Table 3.1: VT and VFB of the Si and $Si_{0.7}Ge_{0.3}/Si$ pMOSFETs extracted using the "split C-V extraction technique". Both simulated and measured values are reported.

A 0.45V of VT shift is noticed by introducing 30% of Ge in the channel. A 0.25V increase of VFB is observed between the Si and $Si_{0.7}Ge_{0.3}$ pMOS, evidencing discrepancy between measured and simulated extracted parameters (see table 3.1).
Match is obtained for pure Si whereas an additional 150mV shift is needed to reproduce the experimental VT and VFB parameters of the $Si_{0.7}Ge_{0.3}$ pMOS. This discrepancy is close to the shift obtained in chapter 4 using conventional VFB extraction technique, proving the validity of the "split C-V extraction technique". The understanding of this shift will be discussed in chapter 4 on page 107.
In general, the gate capacitance in strong inversion can be described as the series combination of the insulator capacitance (C_{ox}) and the inversion-layer capacitance (C_{inv}) (figure 3.9) [121] enabling the gate-to-channel capacitance to be derived as [120]:

$$CGC_M = \frac{C_{inv}C_{ox}}{C_{inv} + C_{ox}} \tag{3.4}$$

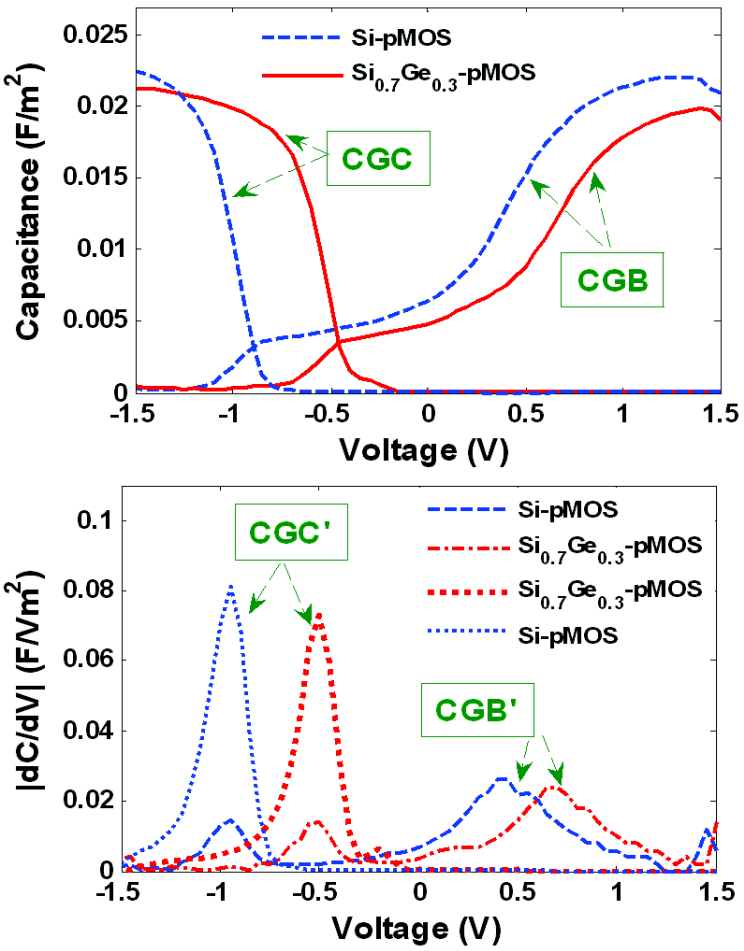


Figure 3.8: Measured $Si_{0.7}Ge_{0.3}$ pMOS split C-V (a) leading to the VT and VFB (b) extraction from CGC' and CGB'.

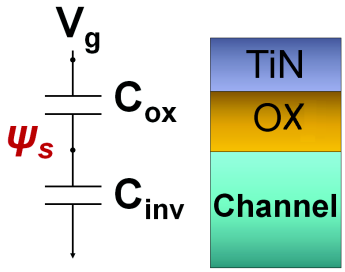


Figure 3.9: Equivalent gate capacitance circuit diagram.

The variation of the measured CGC of the Si and $Si_{0.7}Ge_{0.3}$ pMOS with Q_{inv} are plotted in figure 3.10. Experimental data have been reproduced using the CGC model described by equation 3.4 with an adjusted value of C_{ox} and the analytical model $C_{inv,CM}(Q_{inv})$ (equation 3.2) curve of figure 3.5. From the obtained C_{ox}, we extracted the equivalent oxide thickness EOT ($EOT = \frac{\epsilon_{ox}}{C_{ox}}$ being the SiO_2 permittivity) for the Si and $Si_{0.7}Ge_{0.3}$ pMOS. The estimated

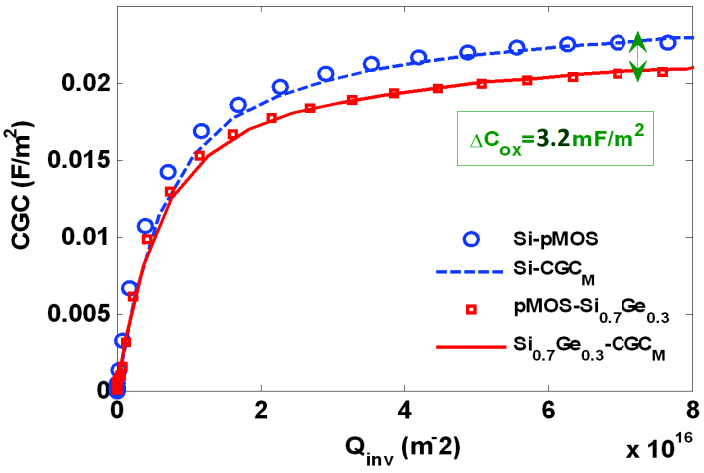


Figure 3.10: Variation of the measured CGC and computed CGC_M with the Q_{inv} of the Si and $Si_{0.7}Ge_{0.3}$ pMOS. The C_{ox} are found equal to 31.5mF/m^2 and 28.3mF/m^2 respectively for the Si and $Si_{0.7}Ge_{0.3}$ pMOS.

EOT are respectively equal to 10.9$\mathring{A}$ and 12.2$\mathring{A}$. The EOT increases up to 1.2$\mathring{A}$ by the inclusion of 30% of Ge in the pMOS. The Ge impact on the EOT will be analysed in the subsection 4.4 of chapter 4. Finally, we check the validity of the EOT extraction method. The measured C-V of the Si and $Si_{0.7}Ge_{0.3}/Si$ pMOS are compared to the PS simulated C-V using EOT values equal to 10.7$\mathring{A}$ and 12$\mathring{A}$ (figure 3.11). Note the very good agreement between the experimental data and the PS simulation results. In particular, the EOT values used for the PS simulation are very close to the extracted EOT obtained with the analytical CGC model of equation (3.4). An uncertainty of 0.2$\mathring{A}$ only is found, emphasizing the robustness of such EOT extraction method.

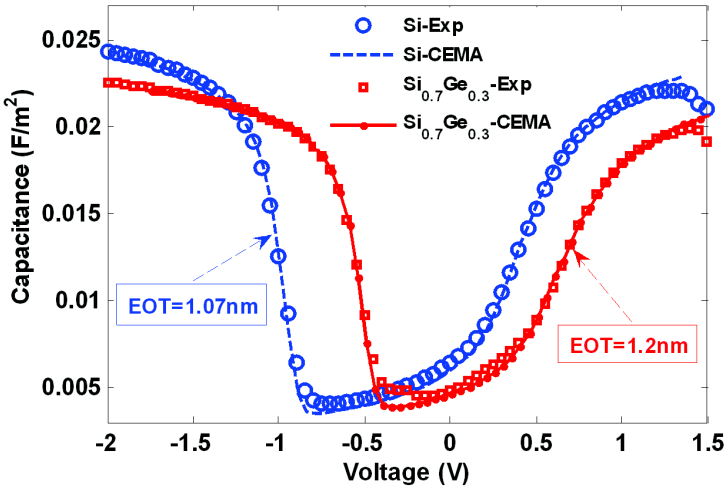


Figure 3.11: Measured and simulated C-V using the extracted EOT.

3.3 EOT extraction method in the FDSOI devices

In the previous section, we have proposed a new method to determine the EOT in Si and $SiGe$ bulk pMOSFETs. The EOT extraction method is based on the $C_{inv}(Q_{inv})$ response. We have shown that the $C_{inv}(Q_{inv})$ curve is equal for the Si and $Si_{0.7}Ge_{0.3}$ bulk pMOS. The $C_{inv}(Q_{inv})$ curve is not sensitive to the Ge integration. But, it depends to the doping concentration.
This section verifies the universality of the $C_{inv}(Q_{inv})$ characteristic. The extraction method proposed in the previous section 3.2.2 to determine the EOT will be generalized and applied to the FDSOI devices. The EOT extraction method will be first verified using the PS simulations of the Si and the Indium gallium arsenide ($InGaAs$) FDSOI nFETs. Then, it will be applied to the Si FDSOI pFET measurement. Similarly, for Si and $Si_{0.7}Ge_{0.3}$ FDSOI pFETs, the extraction method will be tested using UTOXPP simulations. Then, it will be applied to Si and $Si_{0.7}Ge_{0.3}$ measurements. The dependence on the body thickness will be also investigated in order to generalize the EOT extraction method.

3.3.1 EOT extraction in FDSOI nFETs

In this subsection, we simulate the Si and $In_{0.53}Ga_{0.47}As$ FDSOI nFETs using the UTOXPP solver. Simulations have the objective to check the universal behaviour of the $C_{inv}(Q_{inv})$ when varying the body thickness.

3.3.1.1 Device structures

Figure 3.12 illustrates the simulated FDSOI nFETs structures. The $In_{0.53}Ga_{0.47}As$ nFDSOI structure is presented by structure -a-. The Si nFDSOI structure is shown in structure -b-. Here, we study the film thickness variation impact on the C-V characteristic and the inversion layer capacitance ($C_{inv}(Q_{inv})$) of the Si and $In_{0.53}Ga_{0.47}As$ FDSOI nFETs. To do so, the thicknesses of the $In_{0.53}Ga_{0.47}As$ (T_{InGaAs}) and Si (T_{Si}) were varied from 2 to 20nm.

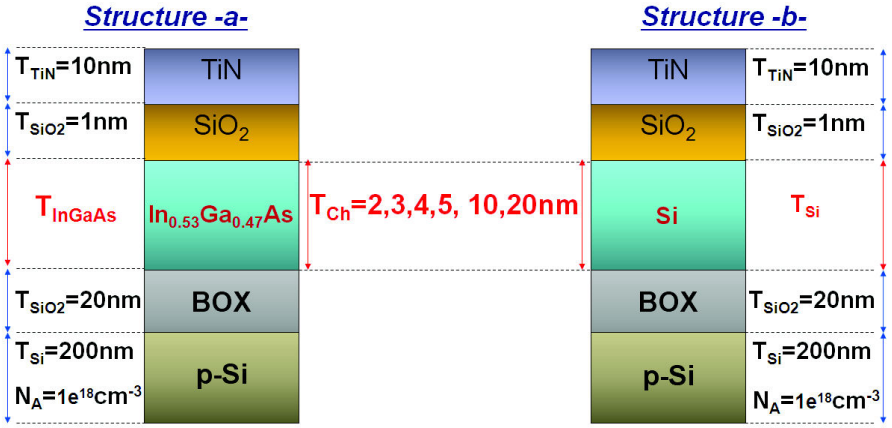


Figure 3.12: Device structures of the $In_{0.53}Ga_{0.47}As$ and Si FDSOI nFETs.

3.3.1.2 Modeling of the Si-FDSOI nFET

Using the UTOXPP similator within the EMA, we have simulated the C-V characteristic of the Si-FDSOI nFET with different T_{Si} thicknesses (figure 3.13). Increasing the T_{Si} from 2nm to 20nm shifts the C-V curves and decreases the VT of the Si-FDSOI nFET up to 90mV.

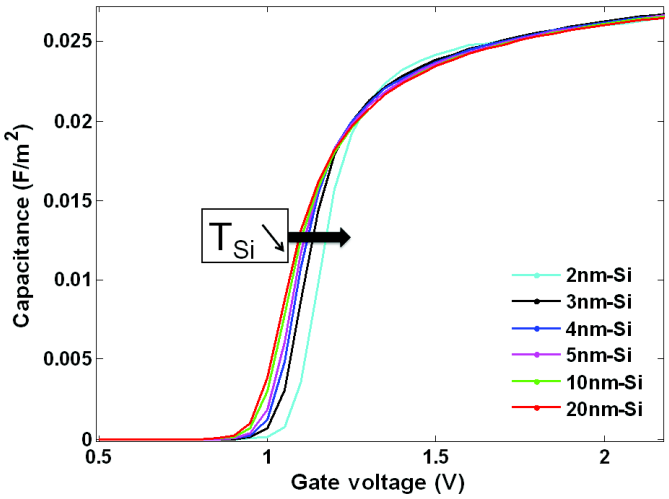


Figure 3.13: The gate capacitance versus the gate voltage of the Si FDSOI nFETs for various T_{Si} thicknesses.

Figure 3.14 highlights the T_{Si} variation impact on the $C_{inv}(Q_{inv})$ inversion capacitance. It is noticeable from this plot that the impact is not significant. Therefore, the $C_{inv}(Q_{inv})$ curve is rather quasi universal, especially from 3nm thick body and above.

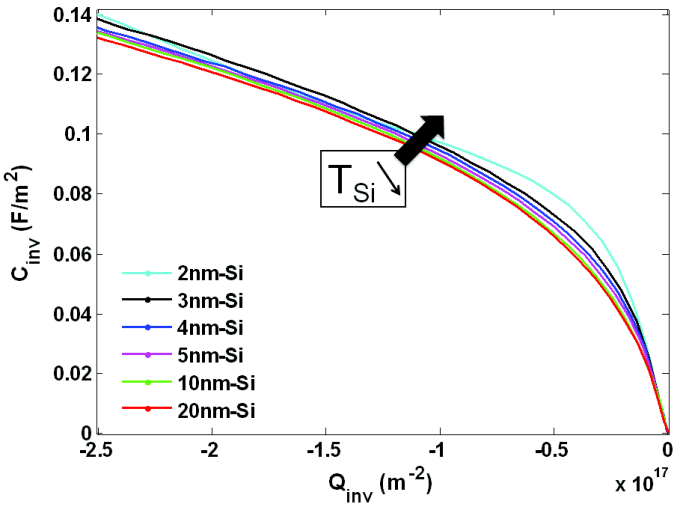


Figure 3.14: The $C_{inv}(Q_{inv})$ inversion capacitance of the Si FDSOI nFETs for various T_{Si} thicknesses.

3.3.1.3 Modeling of the InGaAs-FDSOI nFETs

In this subsection, we highlight the most important input parameters needed to model accurately the $InGaAs$ based devices. In order to validate the UTOXPP simulation model, the simulated C-V curve (using UTOXPP) is compared to published results of the bulk $In_{0.53}Ga_{0.47}As$ nMOSFET [122]. Finally, the C-V and $C_{inv}(Q_{inv})$ characteristics are simulated for the $In_{0.53}Ga_{0.47}As$ FDSOI nFETs. The body thickness is also varied to verify the universal behaviour of the $C_{inv}(Q_{inv})$.

A. **Simulation models of the InGaAs devices**

The InGaAs alloy is a key material for active regions of high-speed electronic devices [123]. It remains a direct-gap material over its entire composition range [124]. An accurate modeling of the gate capacitance of the $InGaAs$ devices requires information on four set of parameters: the gap energy of each valley, the electron effective masses, the nonparabolicity of the $InGaAs$ bands and the wave function penetration (WFP) into the oxide.

In this paragraph we address the impact of these set of parameters on the C-V characteristic of $InGaAs$ based devices. To this end, the bulk $In_{0.53}Ga_{0.47}As$ nMOSFET is considered as the simulated device structure of this study. The simulated device parameters are $N_A = 2.10^{17}cm^{-3}$ and the gate oxide is 2 nm of Al_2O_3 with $\varepsilon_{ox} = 9\varepsilon_0$. Simulations are performed using the UTOXPP Poisson-Schrödinger simulator within the EMA.

i *The $In_{0.53}Ga_{0.47}As$ gap energy and effective masses*
In the case of the $In_{0.53}Ga_{0.47}As$ material, each conduction band minima have specific energy gap with respect to the top of the valence band (figure 3.15).

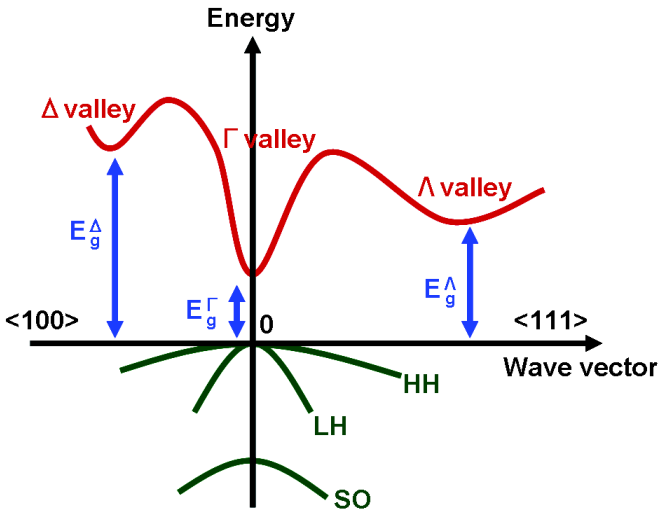


Figure 3.15: Schematic $In_{0.53}Ga_{0.47}As$ bands structure.

The literature reveals a wide range for the energy separations between the top of the valence band and the different conduction valleys-minima. For instance, [125]

suggests $E_g^\Gamma = 0.73eV$, $E_g^\Lambda = 1.2eV$ and $E_g^\Delta = 1.33eV$. Dittrich et al [126] calculates $E_g^\Gamma = 0.73eV$, $E_g^\Lambda = 1.29eV$ and $E_g^\Delta = 1.78eV$ and O'Regan et al [122] uses $E_g^\Gamma = 0.73eV$, $E_g^\Lambda = 1.49eV$ and $E_g^\Delta = 1.98eV$. The Λ-valley minimum has been consistently assumed to lie in the energy range of 0.4eV to 0.7eV above the Γ minimum. In the rest of this chapter, the E_g^Γ is fixed at 0.73eV.
In order to analyse the impact of this entire range of the energy separation on the C-V response, a comparison between the gate to channel capacitance obtained using the extreme values ($E_g^\Lambda = 1.2eV$, $E_g^\Delta = 1.33eV$ ([125]) and $E_g^\Lambda = 1.49eV$, $E_g^\Delta = 1.98eV$ ([122])) is plotted in figure 3.16. The simulations are performed using the UTOXPP Poisson-Schrödinger simulator with no wave function penetration into the oxide. The $In_{0.53}Ga_{0.47}As$ valleys are considered parabolic. It is clear from figure 3.16 that decreasing the E_g^Λ by 300meV shifts the resulting capacitance up to 600mV in strong inversion.

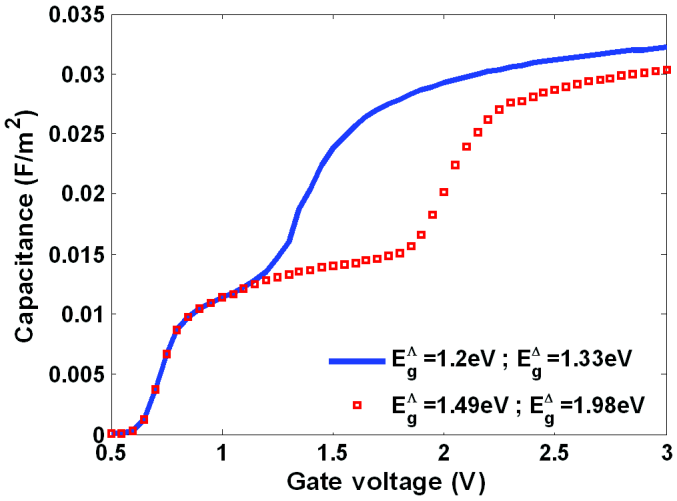


Figure 3.16: Conduction bands energy impact on the $In_{0.53}Ga_{0.47}As$ nMOSFET gate-to-channel capacitance.

The Γ electron effective mass of the $In_{0.53}Ga_{0.47}As$ has been studied both theoretically and experimentally and proposed to be equal to $0.041m_0$ [127] [128] [129] [124]. Concerning the Λ and Δ valleys electron effective masses, only few data exist in the literature. Reference [125] suggests $m_\Lambda = 0.29m_0$ and $m_\Delta = 0.68m_0$. The low Γ electron effective mass results in a small DOS of the $In_{0.53}Ga_{0.47}As$ when only the Γ-valley is occupied. This small DOS will directly result in a low sheet carrier concentration at a certain gate overdrive. Concerning the Λ valley, the m_Λ-valley variation is studied in figure 3.17. Decreasing m_Λ from $0.29m_0$ to $0.19m_0$ affects significantly the C-V response of the bulk $In_{0.53}Ga_{0.47}As$ nMOSFET at high gate voltage.
Let's notice the discrepancy between the C-V characteristic of the bulk $In_{0.53}Ga_{0.47}As$ nMOSFET (figures 3.16 and 3.17) and the common Si and $SiGe$ C-V responses studied in the section 3.2. It is noticeable that the gate capacitance of the $In_{0.53}Ga_{0.47}As$ nMOSFET is reduced at low gate voltage. In the following, we will attempt to un-

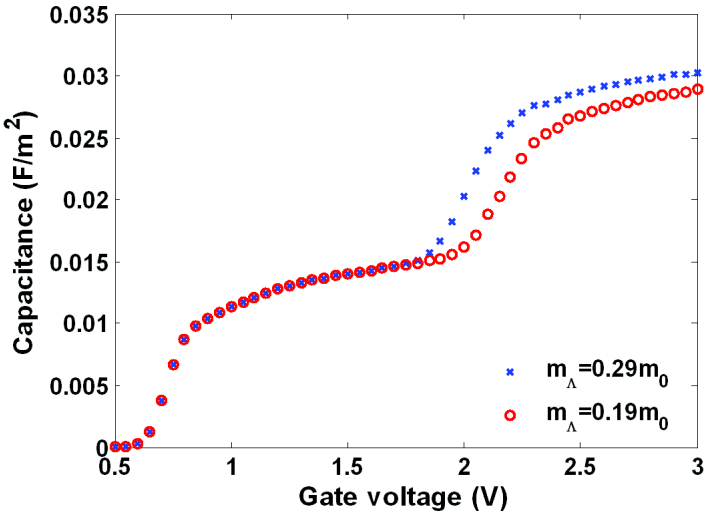


Figure 3.17: Impact of the Λ electron effective mass on the gate-to-channel capacitance of the $In_{0.53}Ga_{0.47}As$ nMOSFET. (The valleys are considered parabolic with $E_g^\Gamma = 0.73eV$, $E_g^\Lambda = 1.49eV$ and $E_g^\Delta = 1.98eV$. There is no wave function penetration into the oxide.)

derstand more precisely the reason leading to such C-V response for $In_{0.53}Ga_{0.47}As$ nFETs. The $In_{0.53}Ga_{0.47}As$ conduction bands are considered parabolic. The electron effective masses are respectively $m_\Gamma = 0.041m_0$, $m_\Lambda = 0.29m_0$ and $m_\Delta = 0.68m_0$ for the Γ, Λ and Δ valleys.

To analyse more precisely the origin of the C-V shape, reported in figure 3.16, we have investigated the $In_{0.53}Ga_{0.47}As$ valley occupation as a function of the total electron density for the two set of band gap parameters (figure 3.18). At low charge density (at low gate voltage), the low capacitance (figure 3.16) corresponds to the low DOS Γ-valley. In this region, only Γ-valley is populated (figure 3.18) and the inversion charge capacitance remains small (figure 3.19).

The limitation in overall gate capacitance comes from this finite inversion-layer capacitance in this gate voltage range (figure 3.20). As the electron charge increases (at high gate voltage), the part of electron density in Λ valleys is increased (figure 3.18). The significant occupancy of the Λ-valley leads to higher inversion charge and gate capacitance (figures 3.19 and 3.20). Figure 3.18 also illustrates that $In_{0.53}Ga_{0.47}As$ valleys occupation (dashed curves) shifts from Γ to Λ valley at lower charge density when using $E_g^\Lambda = 1.2eV$ and $E_g^\Delta = 1.33eV$. Consequently, the increase in the inversion charge capacitance and the overall capacitance are shifted to lower gate voltage (figures 3.19 and 3.20).

To conclude, the C-V curve of the $In_{0.53}Ga_{0.47}As$ presents a particular shape (two bumps). The C-V response is due to the valleys occupation when increasing the gate voltage. At low gate voltage, only the low DOS Γ-valley is populated. So, the inversion charge capacitance remains small (figure 3.19). Increasing the gate voltage, the part of electron density in Λ valleys boosts. Thus the capacitance enhances at high gate voltage.

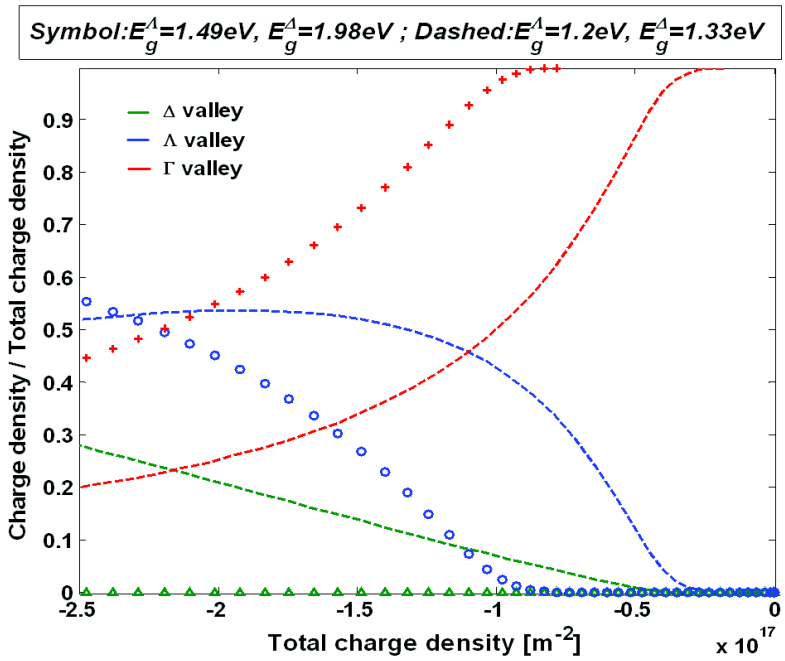


Figure 3.18: Electrons distribution in Γ, Λ and Δ valleys versus charge density for $In_{0.53}Ga_{0.47}As$ nMOSFET.

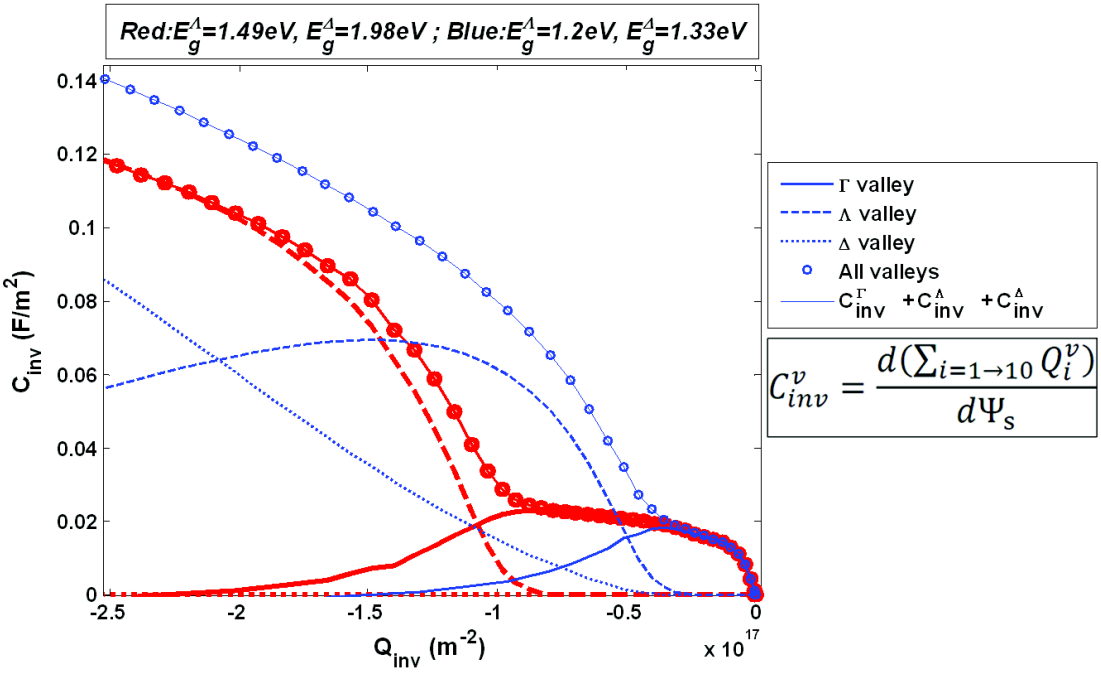


Figure 3.19: The $C_{inv}(Q_{inv})$ of the $In_{0.53}Ga_{0.47}As$ for the Γ, Λ and Δ electron valleys. (Q_i^v is the charge density of the i-th energy level of the v valley and Ψ_s is the surface potential.)

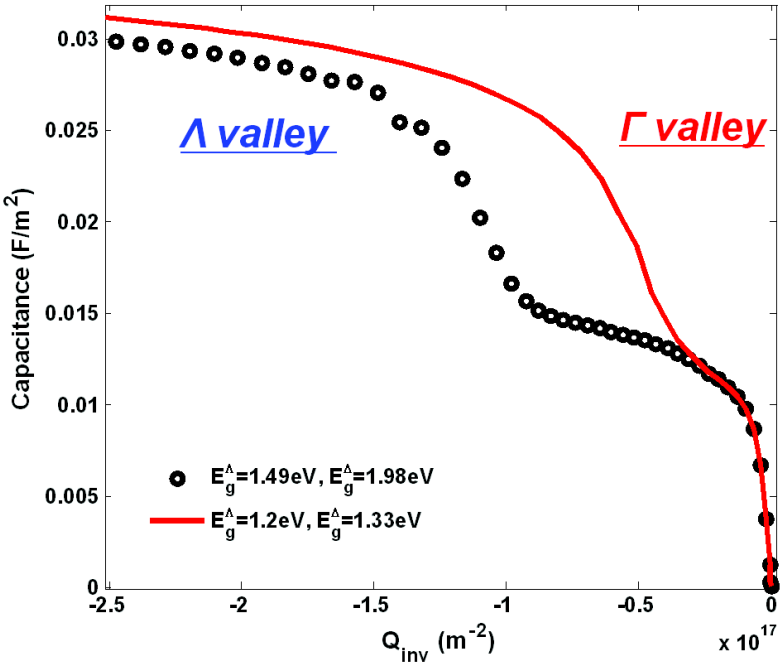


Figure 3.20: The gate capacitance as a function of the inversion charge of the $In_{0.53}Ga_{0.47}As$ nMOSFET.

ii *The nonparabolicity of the InGaAs bands*

For Silicon, the electron band structure consists of six equivalent valleys. The lowest conduction band Δ is well separated from the nearest second conduction band by the energy $\Delta_E = 0.53eV$ [130]. If we assume the effective mass approximation for the Si Δ conduction band, the dispersion relation $E(k)$ (for the Δ valley) is parabolic:

$$E(k) = \frac{\hbar^2 k^2}{2m} \tag{3.5}$$

F.Gilibert has compared the electron band structure $E(k)$ of the Si obtained using the parabolic approximation to those calculated using a full zone k.p model (figure 3.21). The parabolic approximation is valid for the Si conduction band for a large rang of energy [131].

Concerning the $InGaAs$ semiconductor, it is admitted that the Γ-valley exhibits a small effective mass and strong nonparabolicity [132][124]. The "heavier" satellite valley can play an important role, especially under strong quantization, making it necessary to include charge quantization and nonparabolic corrections to more accurately model the valley occupations and corresponding C-V characteristic [122]. Given the above arguments, it is quite clear that a self-consistent solver, which accounts for both non-parabolic conduction band and quantum confinement, must be in place to allow accurate evaluation of the gate capacitance. In order to provide appropriate DOS function for each subband, in the PS UTOXPP simulator, the

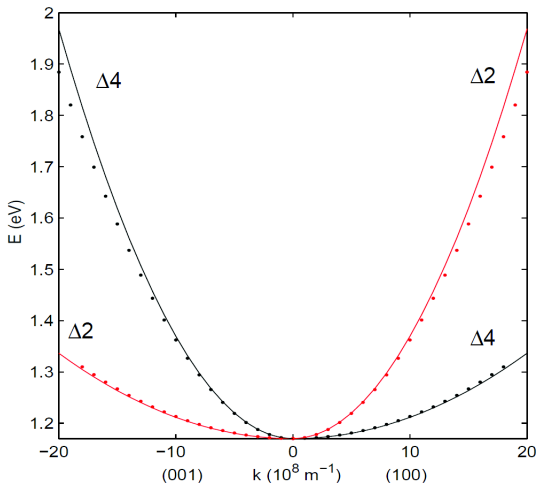


Figure 3.21: Comparison of the Si conduction band structure $E(k)$ obtained using the parabolic approximation (Line) to those calculated using a k.p model (Symbol) [131].

non parabolicity correction is taken into account in the quantum electron density computation as follows [133]:

$$n^{NP}(z) = \sum_{i,v} \frac{m_v^{xy}}{\pi\hbar^2} g_v KT. \left[\ln\left(1+e^{\eta}\right) + 2KT.\alpha_v.F_1(\eta)\right].|\psi_{i,v}(z)|^2 \tag{3.6}$$

Where F_1 is the Fermi-Dirac integral of order 1, $\eta = (E_F - E_{i,v}^z)/KT$, α_v is the nonparabolicity parameter, g_v and m_v are the degeneracy and DOS effective mass in the v band, and $\psi_{i,v}$ is the wave function of the i-th subband of the v band.

The nonparabolicity parameter for the $In_{0.53}Ga_{0.47}As$ Γ-valley is determined from [122] and fixed at $\alpha_\Gamma = 1eV^{-1}$. Because of a lack of data, the Si nonparabolicity parameters [134] are used for the valleys, $\alpha_\Lambda = \alpha_\Delta = 0.5eV^{-1}$ [122].

In order to check the validity of the PS simulation model, we have simulated the C-V characteristic of the bulk $In_{0.53}Ga_{0.47}As$ nMOSFET studied in reference [122]. The energy separations of the $In_{0.53}Ga_{0.47}As$ conduction bands are $E_g^\Gamma = 0.73eV$, $E_g^\Lambda = 1.49eV$ and $E_g^\Delta = 1.98eV$. The electron effective masses are respectively $m_\Gamma = 0.041m_0$, $m_\Lambda = 0.19m_0$ and $m_\Delta = 0.68m_0$ for the Γ, Λ and Δ valleys.

The simulated C-V using the UTOXPP simulator is compared to the C-V obtained by O'Regan et al [122] with and without considering the nonparabolic correction (figure 3.22). It is important to mention that the simulation model used in [122] includes not only the nonparabolic correction of the charge density but also the nonparabolic correction of the energy levels in the PS loop. Whereas, in UTOXPP model, the nonparabolic correction is only considered in the electron density expression as shown in equation 3.6.

In the case of parabolic valleys, a good agreement is noticed. Considering the DOS nonparabolicity correction, we notice a discrepancy for the Λ-valley capacitance response (at high gate voltage). This difference is probably due to the lack of the

nonparabolicity correction of the energy levels [134] in the UTOXPP model. Figure 3.22 illustrates the impact of the subband occupancy and valleys nonparabolicity on the resulting C-V curve. From this figure, the inclusion of the nonparabolic corrections results in a slight increase in the Γ capacitance and a shift of the Λ capacitance.

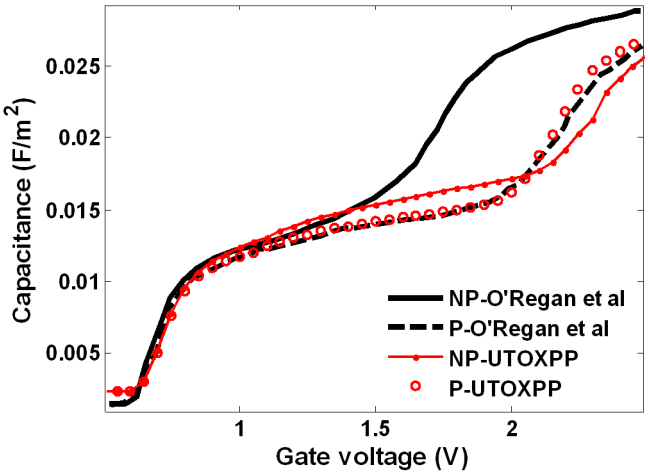


Figure 3.22: Comparison between the C-V characteristics obtained by O'Regan et al [122] and using the PS UTOXPP simulator in the case of the $In_{0.53}Ga_{0.47}As$ nMOSFET with parabolic (P) and nonparabolic (NP) bands. (Here, the wave functions penetration into the oxide is not considered.)

iii *The wave function penetration (WFP) into the oxide*

Figure 3.23 shows the simulated C-V characteristics of the $In_{0.53}Ga_{0.47}As$ bulk nMOSFET with and without taking into account the wave functions penetration (WFP) into the dielectric. The oxide capacitance is equal to $0.04F/m^2$ ($C_{ox} = \varepsilon_{ox}/T_{ox}$). The difference between the oxide capacitance value and the gate capacitance maximum value is due to the dark space. Figure 3.23 illustrates a decrease of the dark space when considering the WFP. This is also confirmed by the charge density profile at constant charge (Q) figure 3.24. Besides, taking into account the WFP increases the capacitance at weak inversion about 30%. At strong inversion, the WFP consideration slightly affects the C-V maximum and shifts the capacitance increase up to 200mV to high gate voltage. This discrepancy is noticed for both parabolic and nonparabolic $In_{0.53}Ga_{0.47}As$ valleys. The noticeable C-V response (figure 3.23) with the WFP is coherent with the charge profile presented in figure 3.24. Considering the WFP, we observe a higher dark space decrease (symbols versus lines in figure 3.24) at low gate bias. In conclusion, the C-V response depends significantly to the WFP parameter.

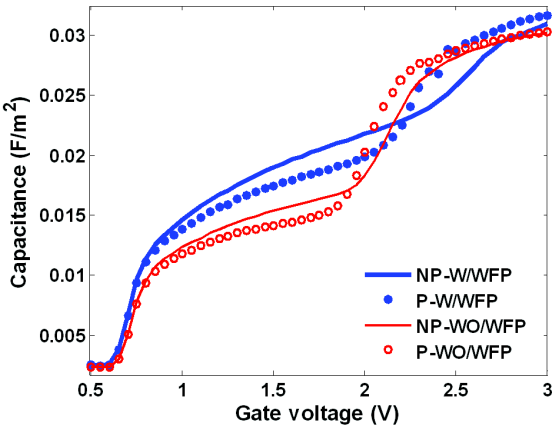


Figure 3.23: Simulated C-V caracteristics of the $In_{0.53}Ga_{0.47}As$ nMOSFET with (W) and without (WO) taking into accout the wave functions penetration (WFP) into the dielectric.

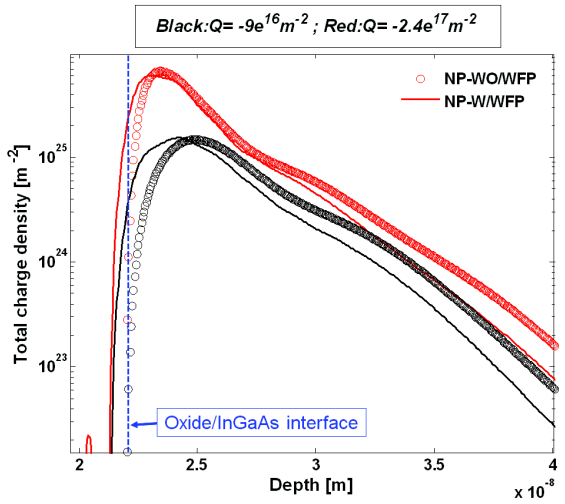


Figure 3.24: Charge density profile of the $In_{0.53}Ga_{0.47}As$ nMOSFET at high and low total charge (Q) with (W) and without (WO) taking into account the WFP into the dielectric.

iv *Recapitalisation of the paragraph*

In this paragraph, we have tested the validity of our PS UTOXPP model to simulate the C-V characteristic of the $In_{0.53}Ga_{0.47}As$ nMOSFET. A Very good agreement is noticed between the C-V curves obtained by O'Regan et al [122] and using the PS UTOXPP simulator proving the validity of our simulation model. We have investigated the impact of the four set of parameters reported in the following table on the C-V response:

The variation of each parameter affects the valleys charge density and the C-V response. An efficient modeling of the gate capacitance needs the knowledge and increasing of these parameters certainty (table 3.2).

Parameters	O'Regan et al [122]	PS UTOXPP
Electron effective masses	-	$m_\Lambda = 0.29m_0$ vs. $m_\Lambda = 0.19m_0$
Conduction bands energy separations	$E_g^\Lambda = 1.2eV$, $E_g^\Delta = 1.33eV$ vs. $E_g^\Lambda = 1.49eV$, $E_g^\Delta = 1.98eV$	$E_g^\Lambda = 1.2eV$, $E_g^\Delta = 1.33eV$ vs. $E_g^\Lambda = 1.49eV$, $E_g^\Delta = 1.98eV$
Nonparabolicity correction	Energy levels and charge density	Only charge density
WFP into the oxide	-	With and without WFP

Table 3.2: Recapitalisation of the studied parameters.

B. **Simulation results of the InGaAs-FDSOI nFETs**

In this paragraph, the universal behaviour of the $C_{inv}(Q_{inv})$ of the $In_{0.53}Ga_{0.47}As$ FDSOI nFET is verified by varying the body thickness.
The $In_{0.53}Ga_{0.47}As$ FDSOI nFET presented in figure 3.12 (structure -a-) was simulated using UTOXPP within the EMA. To highlight the impact of the bands nonparabolicity on the resulting C-V response, we plot in figure 3.25 the simulated C-V with and without taking into account the nonparabolicity correction of the charge density (equation 3.6). We notice that considering nonparabolic $In_{0.53}Ga_{0.47}As$ valleys increases the Γ capacitance and shifts the Λ capacitance to the high voltage. Moreover, the variation of the T_{InGaAs} from 2 to 20nm decreases the VT up to 240mV.

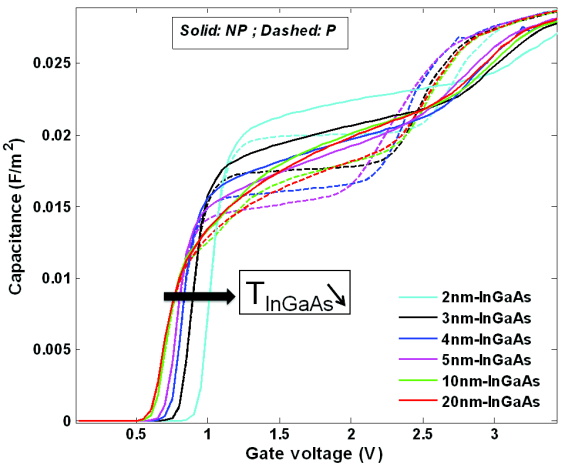


Figure 3.25: Simulated C-V characteristic of the $In_{0.53}Ga_{0.47}As$ FDSOI nFET considering parabolic (solid) and nonparabolic (dashed) bands.

Figure 3.26 illustrates the T_{InGaAs} variation impact on the $C_{inv}(Q_{inv})$ inversion capacitance. The resulting curves are similar for T_{InGaAs} thickness thicker than 5nm whereas discrepancy is noticed for 2nm and 3nm $In_{0.53}Ga_{0.47}As$ FDSOI nFET. As noticed on the C-V response (figure 3.25), taking into account nonparabolic valleys increases the inversion capacitance at low inversion charge and shifts the C_{inv} of the Λ-valley at strong inversion.

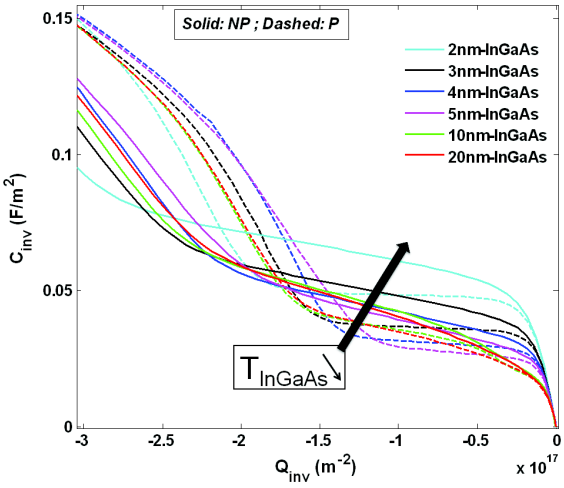


Figure 3.26: Simulated $C_{inv}(Q_{inv})$ inversion capacitance of the $In_{0.53}Ga_{0.47}As$ FDSOI nFET considering parabolic (solid) and nonparabolic (dashed) bands.

3.3.1.4 Inversion layer capacitance of the FDSOI nFET

In subsection 3.3.1.2 and previous paragraph B., we have shown that the $C_{inv}(Q_{inv})$ of the Si and $In_{0.53}Ga_{0.47}As$ FDSOI nFETs is insensitive to the body thickness change (from 3nm to 10nm).
Here, we check the universal behaviour of the $C_{inv}(Q_{inv})$ when changing the body material of the FDSOI nFET. To this end, the obtained $C_{inv}(Q_{inv})$ of the $In_{0.53}Ga_{0.47}As$ and Si FDSOI nFETs will be compared.
The simulated C-V curve of the $In_{0.53}Ga_{0.47}As$ (figure 3.25) and Si (figure 3.13) FDSOI nFETs are compared in figure 3.27.

The DOS electron effective mass of the Si is $1.07m_0$. On the other hand, the electron effective mass of the $In_{0.53}Ga_{0.47}As$ Γ-valley is so much lower ($0.041m_0$). Due to such a low DOS that this small effective mass implies, the gate capacitance is significantly reduced when only the Γ-valley is occupied (at low applied gate voltage). Thus, the Si FDSOI nFET gate capacitance remains higher than the capacitance of the $In_{0.53}Ga_{0.47}As$ FDSOI nFET at weak inversion. At strong inversion, the Λ-valley of the $In_{0.53}Ga_{0.47}As$ becomes occupied. As a result, the corresponding gate capacitance of the $In_{0.53}Ga_{0.47}As$ FDSOI boosts at high inversion charge (figure 3.28).

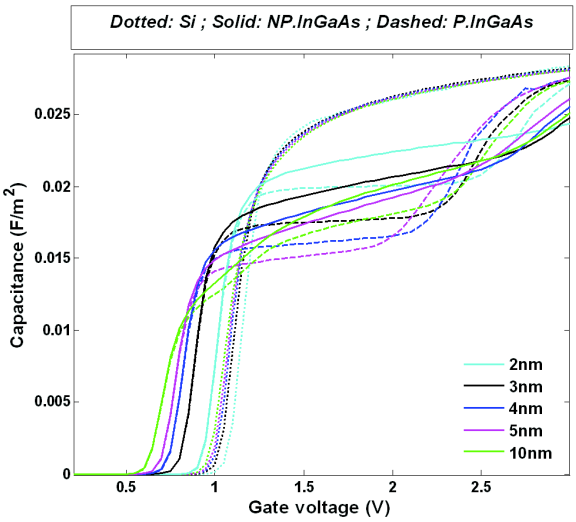


Figure 3.27: Simulated C-V characteristics of the Si and $In_{0.53}Ga_{0.47}As$ FDSOI nFETs considering parabolic (P) and nonparabolic (NP) bands.

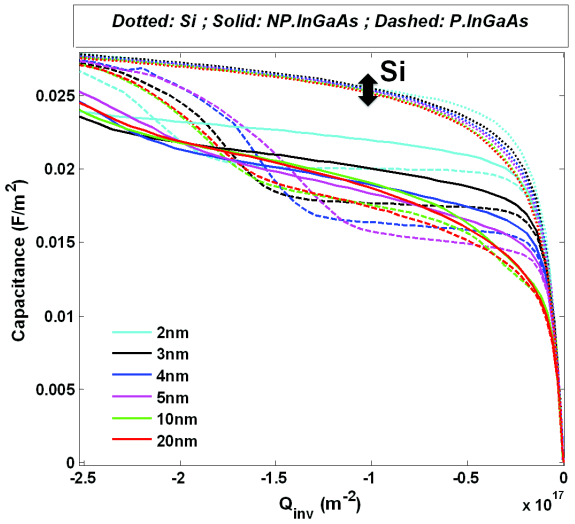


Figure 3.28: Simulated gate capacitance versus inversion charge of the Si and $In_{0.53}Ga_{0.47}As$ FDSOI nFETs considering parabolic (P) and nonparabolic (NP) bands.

Figure 3.29 compares the simulated $C_{inv}(Q_{inv})$ curve of the $In_{0.53}Ga_{0.47}As$ and Si FDSOI nFETs. As explained above, the position of the inversion capacitance of the $In_{0.53}Ga_{0.47}As$ FDSOI nFET in regard of the Si FDSOI nFET C_{inv} is a direct result of the occupation of the $In_{0.53}Ga_{0.47}As$ valleys and the low electron effective mass of the Γ-valley. It is important to mention that the variation of the $C_{inv}(Q_{inv})$ is very close for various T_{Si}. Whereas, a different $C_{inv}(Q_{inv})$ response (compared to those of Si) is noticed when the $In_{0.53}Ga_{0.47}As$ material is introduced in the body of the FDSOI nFET response. This result proves that the $C_{inv}(Q_{inv})$ is universal for Si FDSOI nFETs but it can not be used for $In_{0.53}Ga_{0.47}As$ based devices.

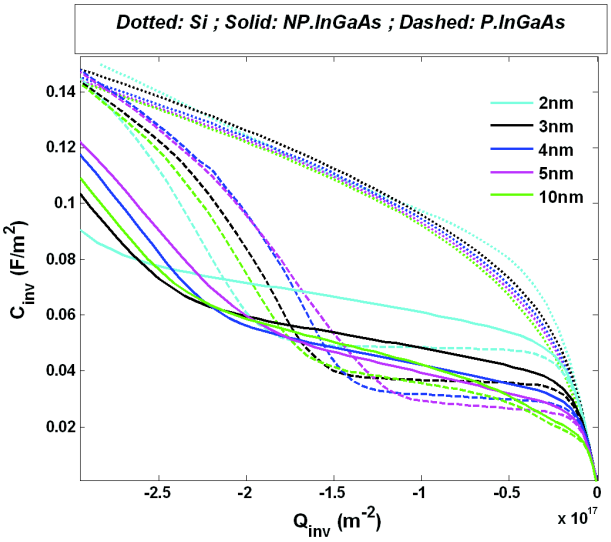


Figure 3.29: Simulated $C_{inv}(Q_{inv})$ inversion capacitance of the Si and $In_{0.53}Ga_{0.47}As$ FDSOI nFETs with (NP) and without (P) the DOS nonparabolicity correction.

3.3.1.5 EOT extraction of the Si-FDSOI nFET

We propose here a simple and efficient method to extract the EOT of the Si FDSOI nFET. Generally, the MOS capacitor can be described by two capacitors in series as:

$$\frac{1}{CGC} = \frac{1}{C_{ox}} + \frac{1}{C_{inv}} \tag{3.7}$$

We have demonstrated in subsection 3.3.1.2 on page 87 that the $C_{inv}(Q_{inv})$ is really independent to the T_{Si} variation. Thus, the EOT expression can be derived from equation 3.7 as:

$$EOT(Q_{inv}) = \varepsilon_{SiO_2}.\left(\left[CGC^{Exp}(Q_{inv})\right]^{-1} - \left[C_{inv}^{Sim}(Q_{inv})\right]^{-1}\right) \tag{3.8}$$

Figure 3.30 shows the measured gate-to-channel capacitance as a function of the inversion charge of the Si FDSOI nFET ($T_{Si} = 6.5nm$). In this figure, the sharp decrease of the capacitance in strong inversion is related to the gate leakage. The determination of the EOT in this region is problematic. Thus, to extract properly the EOT, we define an inversion charge margin (ICM) (figure 3.30) where the capacitance is not affected by the gate leakage.
Using equation 3.8, we have computed the corresponding EOT. Figure 3.31 shows the obtained EOT as a function of the inversion charge. The EOT passes through a plateau corresponding to the defined inversion charge margin (ICM). From this plateau, we extract the EOT (here EOT=0.84nm).
In order to verify the validity of the extracted method, we have simulated the C-V of the Si FDSOI nFET ($T_{Si} = 6.5nm$) using the extracted EOT value (EOT=0.84nm). Figure 3.32 illustrates the very good agreement between the experimental data and the PS simulation results proving the reliability of the EOT extraction method.

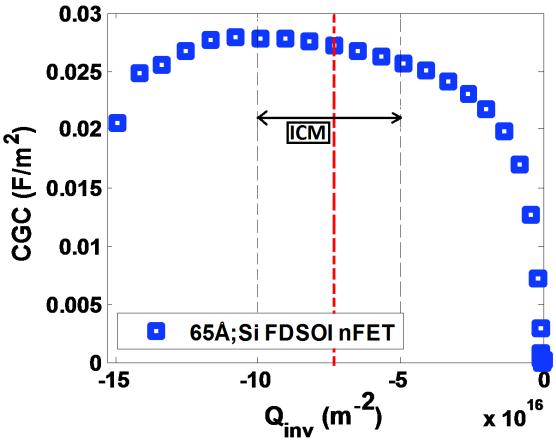


Figure 3.30: Measured CGC of Si FDSOI nFET ($T_{Si} = 6.5nm$, surface>$1\mu m^2$).

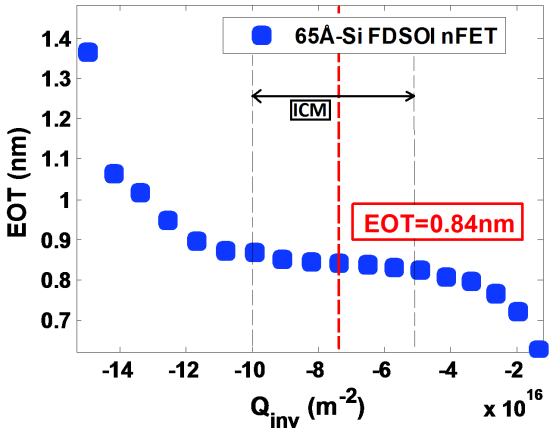


Figure 3.31: EOT extraction of the Si FDSOI nFET.

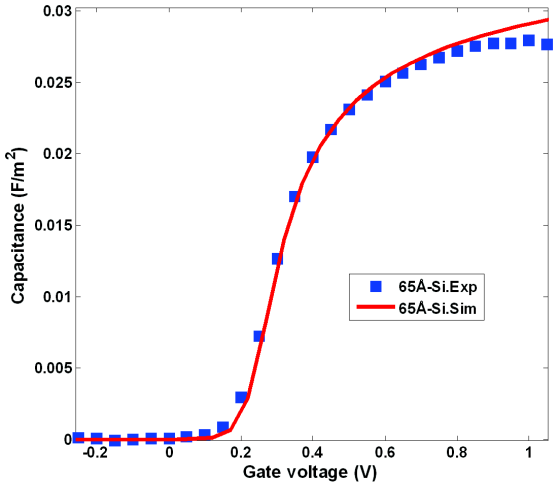


Figure 3.32: EOT extraction of the Si FDSOI nFET.

3.3.2 EOT extraction in FDSOI pFETs

We have shown in the previous subsection that the $C_{inv}(Q_{inv})$ capacitance is insensitive to the film thickness variation in the Si FDSOI nFET. In this subsection, we will check if this criterion is still verified for the Si and $SiGe$ FDSOI pFETs.

3.3.2.1 Device structures

Figure 3.33 shows the simulated FDSOI pFETs structures. The $Si_{0.7}Ge_{0.3}$ pFDSOI structure is presented by structure -c-. The Si pFDSOI structure is illustrated in structure -d-. The $Si_{0.7}Ge_{0.3}$ (T_{SiGe}) and Si (T_{Si}) thicknesses were varied from 2 to 20nm.

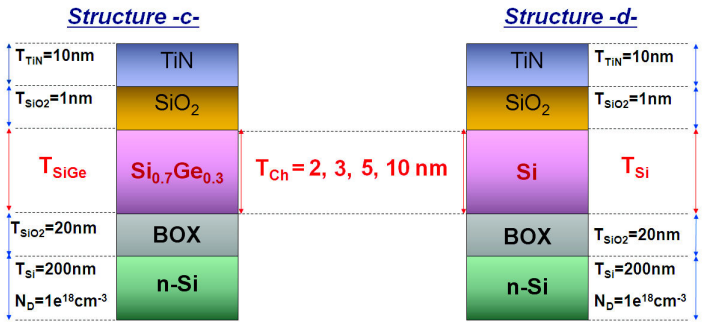


Figure 3.33: Device structures of the $Si_{0.7}Ge_{0.3}$ and Si FDSOI pFETs.

3.3.2.2 Modeling of the Si-FDSOI pFETs

Figure 3.34 compares the simulated C-V of the Si FDSOI pFET (structure -d-) obtained using the 6k.p model with an in-plane numerical integration (exact formula) and the CEMA with (MDOS(HH,Si)=$2.5m_0$). The gate capacitance calculated using the CEMA reproduces the gate capacitance maximum value computed using the "exact formula". Only 20mV of VT discrepancy is noticed. Decreasing the T_{Si} increases the VT of the Si FDSOI pFET up to 180mV.

The impact of the T_{Si} variation on the $C_{inv}(Q_{inv})$ inversion capacitance is shown in figure 3.35. The $C_{inv}(Q_{inv})$ of the Si FDSOI pFET are close up to $T_{Si} = 5nm$. A discrepancy is noticed when the T_{Si} is thinner than 5nm. This is explained by the high quantization effects in the sub-5nm films.

3.3.2.3 Modeling of the SiGe-FDSOI pFETs

The simulated C-V of the $Si_{0.7}Ge_{0.3}$ FDSOI pFET (structure -c-) computed using the 6k.p model with an in-plane numerical integration is illustrated in figure 3.36. The T_{SiGe} decrease increases the VT of the $Si_{0.7}Ge_{0.3}$ FDSOI pFET up to 185mV. Similarly to the Si FDSOI pFETs, we have verified that the C-V obtained using the CEMA with the adjusted MDOS(HH,Si) ($1.5m_0$) matches the "exact formula" simulated C-V.

The $C_{inv}(Q_{inv})$ inversion capacitance of the $Si_{0.7}Ge_{0.3}$ FDSOI pFET is plotted in figure 3.37. It's clear from this figure that T_{SiGe} variation impact is not significant when T_{SiGe} is thicker than 5nm. An increase of C_{inv} is noticed for thinner T_{SiGe}. The C_{inv} increase (from 10nm

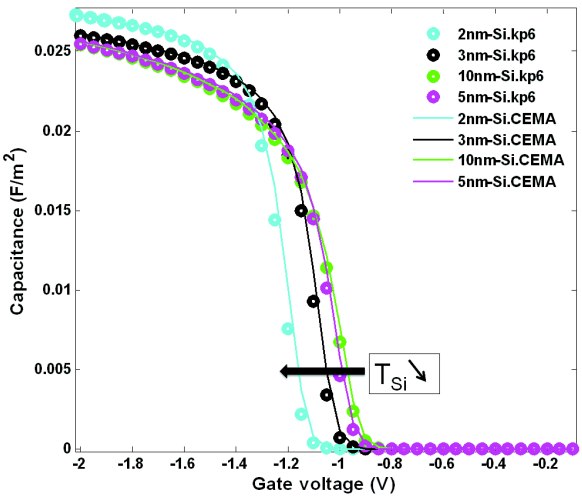


Figure 3.34: Comparison of the simulated C-V of the *Si* FDSOI pFET (structure -d-) obtained using the 6k.p model with an in-plane numerical integration (kp6) and the CEMA with (MDOS(HH,Si)=$2.5m_0$).

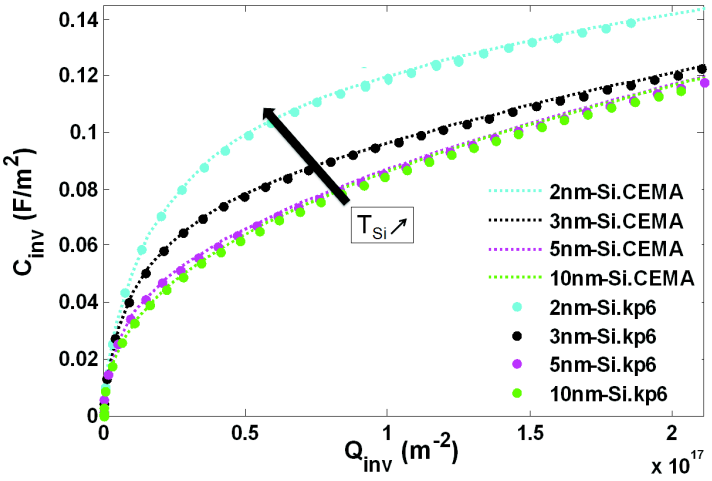


Figure 3.35: Simulated $C_{inv}(Q_{inv})$ of the *Si* FDSOI pFET (structure -d-) obtained using the 6k.p model with an in-plane numerical integration (kp6) and the CEMA with (MDOS(HH,Si)=$2.5m_0$).

to 2nm *SiGe*) reveals $2\mathring{A}$ dark space decrease and consequently a gate capacitance maximum value increase (figure 3.36).

3.3.2.4 Inversion layer capacitance of the FDSOI pFET

Here, we want to verify the universal behaviour of the $C_{inv}(Q_{inv})$ curve for the FDSOI pFETs. To this end, we compare in figure 3.38 the simulated $C_{inv}(Q_{inv})$ of the $Si_{0.7}Ge_{0.3}$ (figure 3.37) and *Si* (figure 3.35) FDSOI pFETs for various channel thicknesses (from 2nm to 10nm). The resulting $Si_{0.7}Ge_{0.3}$ and *Si* curves are very close. One can notice a change in the response for

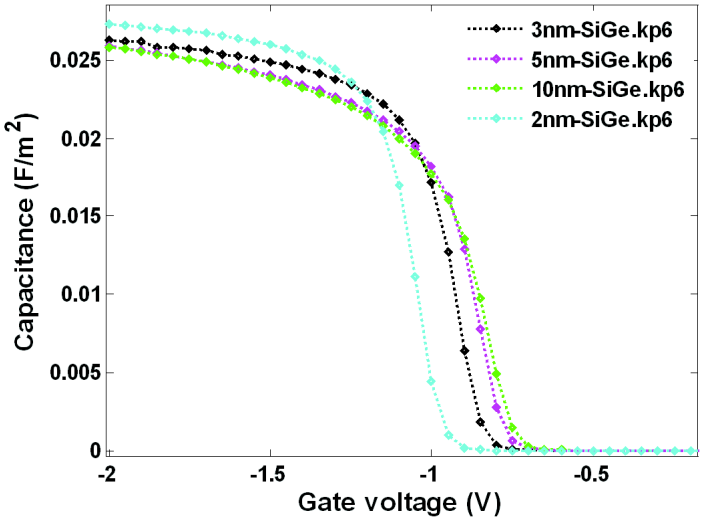


Figure 3.36: Simulated C-V of the $Si_{0.7}Ge_{0.3}$ FDSOI pFET (structure -c-).

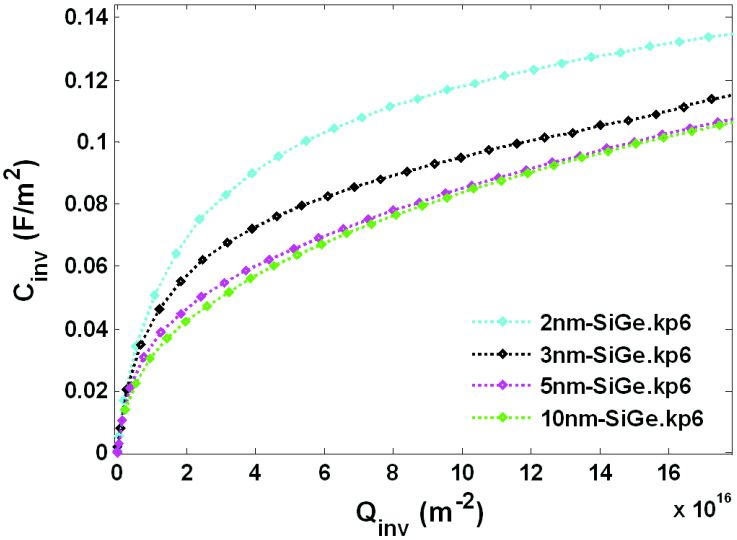


Figure 3.37: Simulated $C_{inv}(Q_{inv})$ of the $Si_{0.7}Ge_{0.3}$ FDSOI pFET (structure -c-).

very thin body thickness (2nm and 3nm), proving the universal behaviour of the $C_{inv}(Q_{inv})$ for the Si and $SiGe$ FDSOI pFETs with a body thickness larger than 3nm.

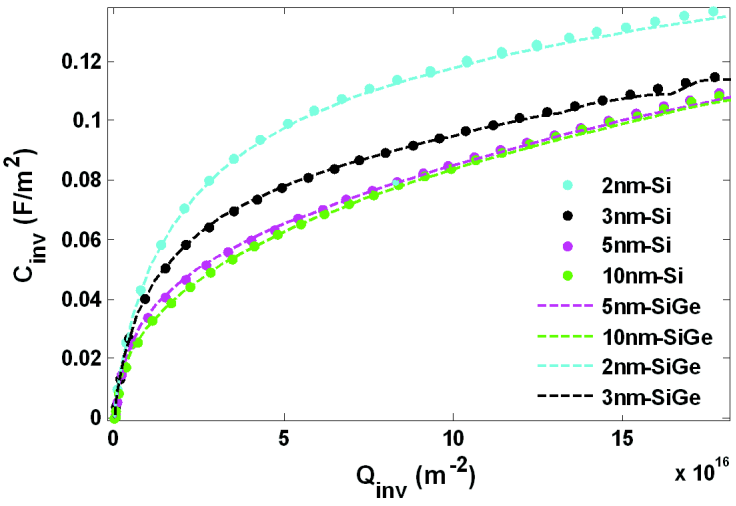


Figure 3.38: Comparison between the simulated $C_{inv}(Q_{inv})$ of the Si and $Si_{0.7}Ge_{0.3}$ FDSOI pFETs. Simulations are achieved using the CEMA using the adjusted MDOS(HH,Si) ($2.5m_0$ and $1.5m_0$ respectively for Si and $Si_{0.7}Ge_{0.3}$ FDSOI).

Concerning the C-V characteristic, the simulated C-V of the $Si_{0.7}Ge_{0.3}$ (figure 3.36) and Si (figure 3.34) FDSOI pFETs are compared in figure 3.39. The integration of 30% of Ge shifts the gate capacitance up to 180mV to the low gate voltage ($\mid V_g \mid$).

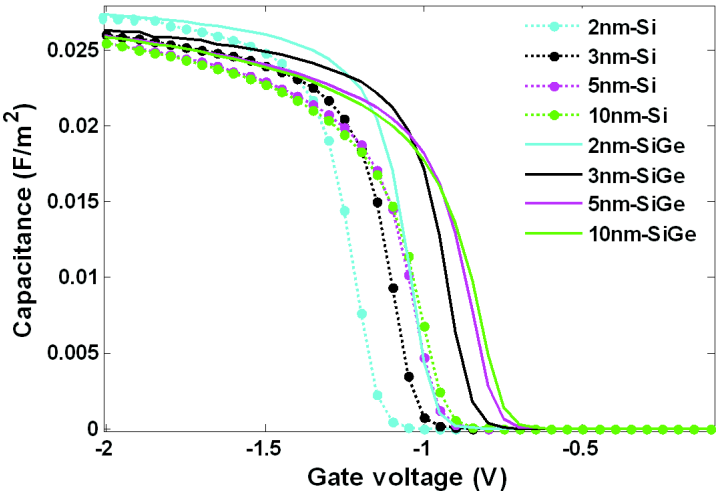


Figure 3.39: Comparison between the simulated C-V of the Si and $Si_{0.7}Ge_{0.3}$ FDSOI pFETs. Simulations are acheived using the CEMA using the adjusted MDOS(HH,Si) ($2.5m_0$ and $1.5m_0$ respectively for Si and $Si_{0.7}Ge_{0.3}$ FDSOI).

3.3.2.5 EOT extraction of the Si and SiGe FDSOI pFETs

We apply here the EOT extraction method proposed for the *Si* FDSOI nFET (subsection 3.3.1.5) to the measured *Si* and $Si_{0.7}Ge_{0.3}$ FDSOI pFETs C-V. Figure 3.40 shows the measured gate-to-channel capacitance as a function of the inversion charge of the *SiGe* FDSOI pFET with various *Ge* concentrations (from 0% to 38%) and T_{SiGe} thicknesses (from 6nm to 8nm). The extracted EOT of the *SiGe* FDSOI pFETs are plotted in figure 3.41. The comparison of the simulated C-V using such extracted EOT values (figure 3.42) shows a good matching emphasizing the validity of the extraction method. 400mV VT decrease is noticed when incorporating 38% of *Ge* in the FDSOI pFET channel (This decrease will be more discussed in chapter 4.).

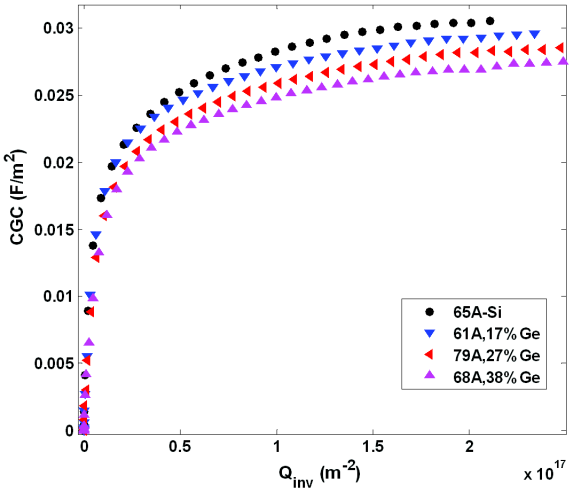


Figure 3.40: Measured CGC as a function of inversion charge of *SiGe* FDSOI pFETs with various *Ge* concentrations (from 0% to 38%) and T_{SiGe} thicknesses (from 6nm to 8nm).

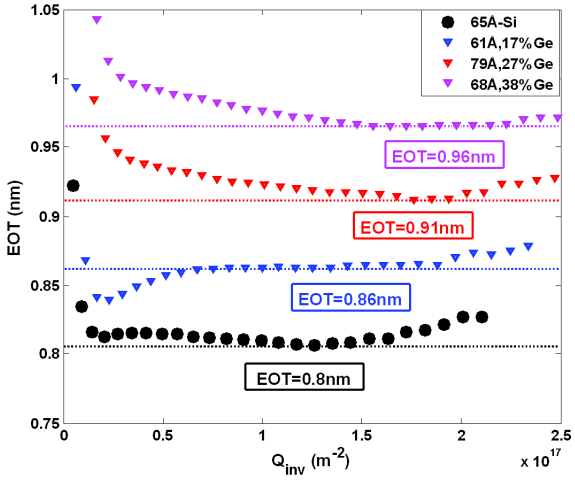


Figure 3.41: Extracted EOT of the the *SiGe* FDSOI pFETs with various *Ge* concentrations (from 0% to 38%) and T_{SiGe} thicknesses (from 6nm to 8nm).

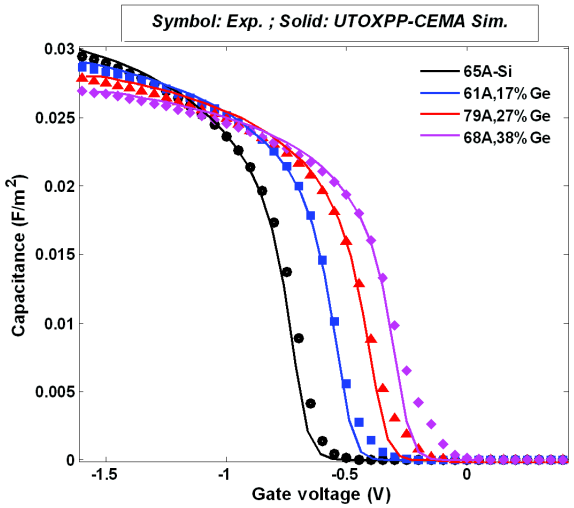


Figure 3.42: Comparison of measured and simulated C-V using extracted EOT values plotted in figure 3.41.

3.4 Conclusion

In the first part of this chapter, we have investigated that the VT extraction method using split C-V (presented in [120]) may be applied to extract VT and VFB parameters in $Si_{1-x}Ge_x/Si$ bulk pMOSFETs. The split C-V method has been validated by PS simulations, emphasizing its simplicity and robustness. The extraction method has been successfully applied to Si and $Si_{0.7}Ge_{0.3}/Si$ pMOS enabling the investigation of the Ge incorporation impact in bulk pMOSFETs. This chapter suggests also a new EOT extraction method based on the inversion capacitance versus inversion charge curve. The $C_{inv}(Q_{inv})$ curve is found equal for the Si and $Si_{0.7}Ge_{0.3}$ bulk pMOS. It is not sensitive to the Ge integration but it depends to the doping concentration.
In FDSOI devices, the body is undoped. Thus, the $C_{inv}(Q_{inv})$ dependence on the doping concentration limit can be prescinded. Therefore, the EOT extraction method may be generalized for FDSOI devices.
The second part of this chapter verifies the universal behaviour of the $C_{inv}(Q_{inv})$ of the FDSOI nFETs using UTOXPP simulations. Si and $In_{0.53}Ga_{0.47}As$ nFETs are simulated for different body thicknesses. The variation of the $C_{inv}(Q_{inv})$ is very close for various T_{Si} whereas a discrepancy is noticed for the $In_{0.53}Ga_{0.47}As$ FDSOI response. The combination to Si FDSOI nFET measurement allows the extraction of the EOT. Then, we have similarly checked the universal behaviour of the $C_{inv}(Q_{inv})$ of the Si and $Si_{1-x}Ge_x$ FDSOI pFETs. The EOT extraction method is tested using UTOXPP simulations for various body thicknesses. Finally, it has been successfully applied to Si and $Si_{0.7}Ge_{0.3}$ measurements proving the robustness of the extraction method.

Chapter 4

Germanium impact in $Si_{1-x}Ge_x$ pFETs gate stack

Contents

4.1 Introduction

Threshold voltage engineering is an essential issue in CMOS technology for device optimization. To reduce the high bulk pMOS threshold voltage, strained Silicon Germanium on Silicon buffer layer has been successfully introduced in the 32-28nm industrial bulk process [21]. The threshold voltage reduction can also be achieved by narrowing the channel band gap on the valence band side. For such a concern on VT and mobility, strained $SiGe$ is recently introduced in the 14nm node FDSOI pFET [25][32].
In this chapter, we investigate the electrical impact of Ge integration in both pMOS bulk and FDSOI technologies. Thus, we need to analyse the role of Germanium on gate stack parameters: the Effective work function ($WFeff$), equivalent oxide thickness (EOT), threshold voltage (VT) and flat band voltage (VFB). To this end, a comparison between experiments and simulations with various $SiGe$ thicknesses and Ge concentrations has been performed. A combination of electrical characterization, physicochemical analysis and Poisson-Schrödinger simulations is proposed to highlight and explain the impact of Germanium on the effective work function and EOT.

4.2 Measurements

Two based $SiGe$ pMOS technologies are selected to study the electric effect of Ge integration. They are the $Si_{1-x}Ge_x/Si$ bulk pMOSFETs and $Si_{1-x}Ge_x$ FDSOI pFETs. In this section, we describe both $SiGe$ pMOS devices.

4.2.1 $SiGe$ bulk pMOSFETs

The $SiGe/Si$ bulk pMOSFETs is described in figure 4.1.a. These correspond to a gate first integration scheme on an epitaxied $SiGe$ channel. Two different Interfacial Oxides (IL) are processed (figure 4.1.b & c).

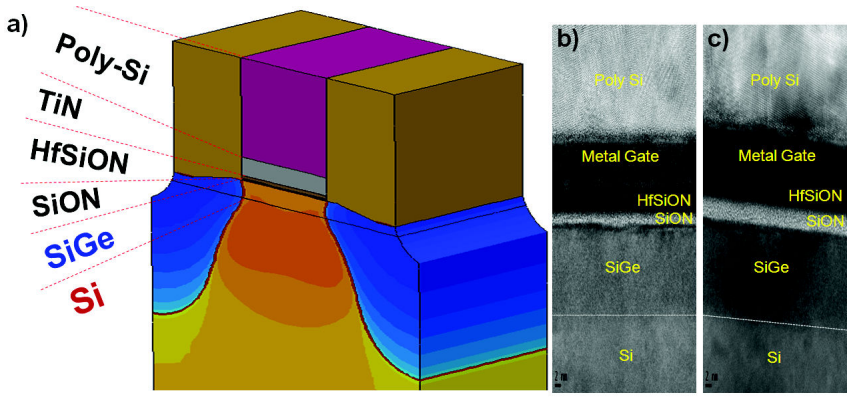


Figure 4.1: $SiGe/Si$ epitaxial-based pMOSFETs and TEM pictures for a $SiGe$ channel targeted at 12nm and 30% of Ge concentration. a) $SiGe/Si$ bulk pMOSFET scheme, b) $SiGe$ pMOSFET with a thin $SiON$ interfacial oxide, c) $SiGe$ pMOSFET with a thick $SiON$ interfacial oxide.

First, a SiO_x layer is deposited (4nm) and nitrided to get the thick $SiON$ interfacial oxide layer. Then, a local wet etch is realized to enable the thin IL patterning. The etching is followed by thermal oxidation (1.5nm) and nitridation. Following IL process, a high-k material is deposited and nitrided to fabricate a thin $HfSiON$ insulator. Finally, a TiN metal gate stack is deposited.
More than 16 different wafers with various Ge content (xGe) and $SiGe$ thickness (T_{SiGe}) have been analysed. Figure 4.2 reports their thicknesses and Ge contents extracted through ellipsometry measurements. Thus, the $Si_{1-x}Ge_x/Si$ pMOSFETs with Ge content varying from 20 to 34% are compared to pure Si pMOSFET reference. The pure Si pMOSFETs have followed the same $SiGe$ pMOSFETs process, except of course the $SiGe$ epitaxy step.

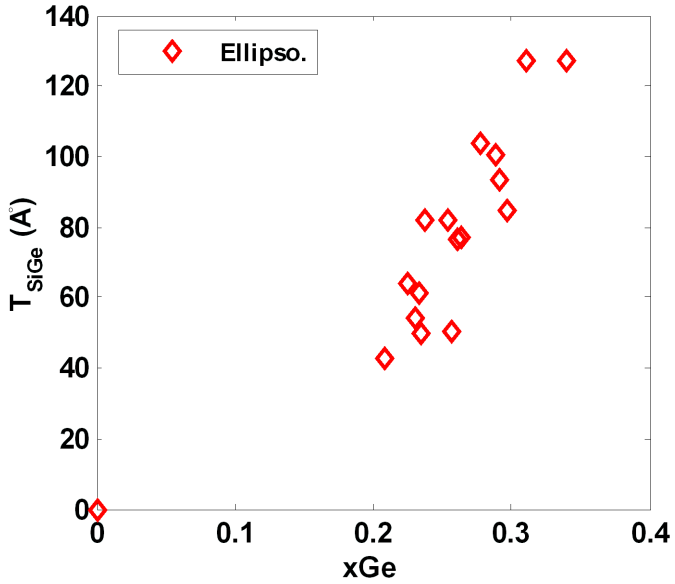


Figure 4.2: Ellipsometry measurements of $SiGe$ thickness and Germanium content for the different tested wafers.

On each wafer, three different pMOSFETs may be obtained thanks to threshold voltage adjust implant dose ($DC1$ and $DC2$) and $SiON$ thicknesses ($TIL1$ and $TIL2$) variations (table 4.1).

Bulk pMOSFET	SiON thickness	Si doping concentration
VT1	TIL1	DC1
VT2	TIL1	DC2<DC1
VT3	TIL2=3×TIL1	DC2<DC1

Table 4.1: Different pMOS architectures related to variation on interfacial oxide thickness (TIL) and Si substrate implant dose (DC).

Figure 4.3 shows the VT of pMOSFETs ($surface < 1\mu m^2$) measured in linear current region (see subsection 1.2.1.4 on page 21). This method is used in the industry to follow the technology

threshold voltage. For each MOS type, we evidence more than 0.4V variation on VT with xGe increasing up to 34%.
In order to investigate the impact of Ge on the VT, we extract the VT from C-V measurement at 40% of $C^{max,inv}$, the capacitance maximum value at strong inversion. The ΔVT obtained between the two extraction methods is very small (figure 4.4) confirming the validity of the extraction method based on C-V measurements.

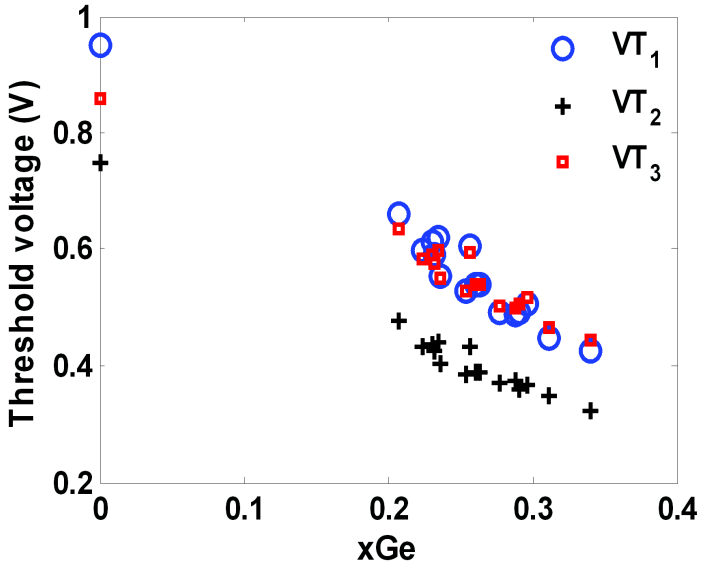


Figure 4.3: $SiGe/Si$ pMOSFETs VT in the linear current region as a function of xGe. This method is used in the industry to follow the technology threshold voltage (Vd=-50mV, Icc=70W/L nA with W being the gate width and L the gate length).

4.2.2 $SiGe$ FDSOI pFETs

The $Si_{1-x}Ge_x$ FDSOI pFETs with gate first integration scheme is presented in figure 4.5. For this technology, the $SiGe$ film is condensed. The high-k oxide consists of HfO_2 instead of $HfSiON$ for bulk pMOSFETs. Variation on IL oxide ($SiON$) thicknesses leads to 2 different VTFD FDSOI pFETs (table 4.2). Thus, as obtained for bulk pMOSFETs (VT1 and VT2 devices), we have two FDSOI pFETs corresponding to two IL thicknesses (T_1 and T_2). The IL variation allows the investigation of the Ge electrical effect in such devices. In particular, the comparison of the flat band voltage for two different IL thicknesses can evidence the impact of the fixed charge in the oxide.

FDSOI pFETs	SiON thickness
VTFD1	$\mathbf{T_1}$
VTFD2	$\mathbf{T_2 = 3 \times T_1}$

Table 4.2: FDSOI pFETs architectures related to variation on interfacial oxide thickness.

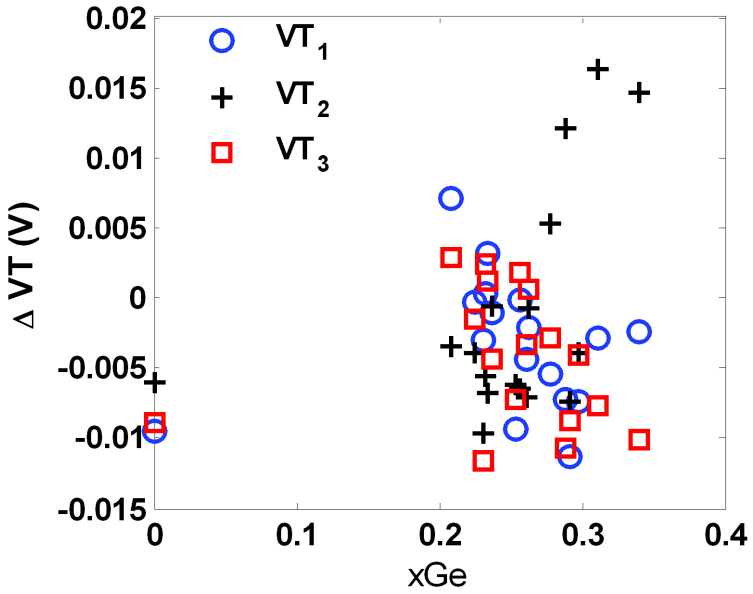


Figure 4.4: Discrepancy between pMOS inversion VT (figure 4.3) and capacitance VT at 40% of $C^{max,inv}$ as a function of xGe.

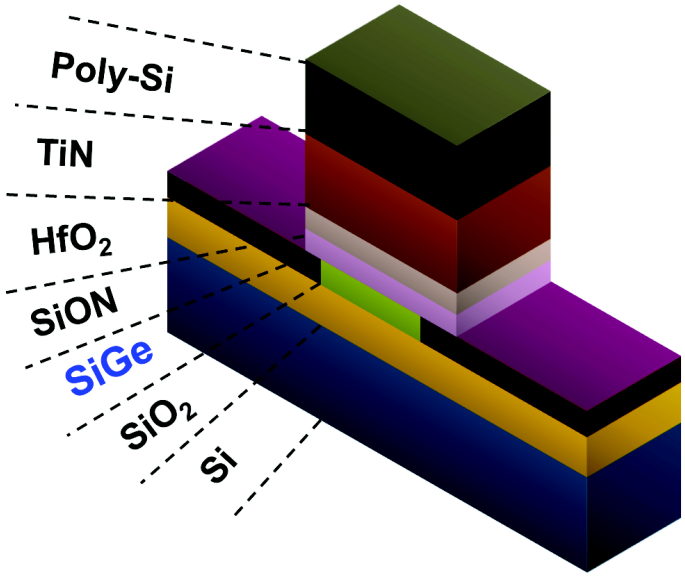


Figure 4.5: $SiGe$-based FDSOI pFETs.

Variation of Ge concentration and $SiGe$ thickness is studied on 4 wafers. Figure 4.6 illustrates their values obtained through ellipsometry measurement. The Ge concentration varies from 0% to 38%. The Si thickness is targeted at 65$\mathring{A}$. The $SiGe$ thickness varies from 61$\mathring{A}$ to 79$\mathring{A}$. Figure 4.7 shows FDSOI pFETs VT ($surface \geq 1\mu m^2$) extracted at 40% of $C^{max,inv}$. More than 0.4V linear VT variation with xGe is noticed.

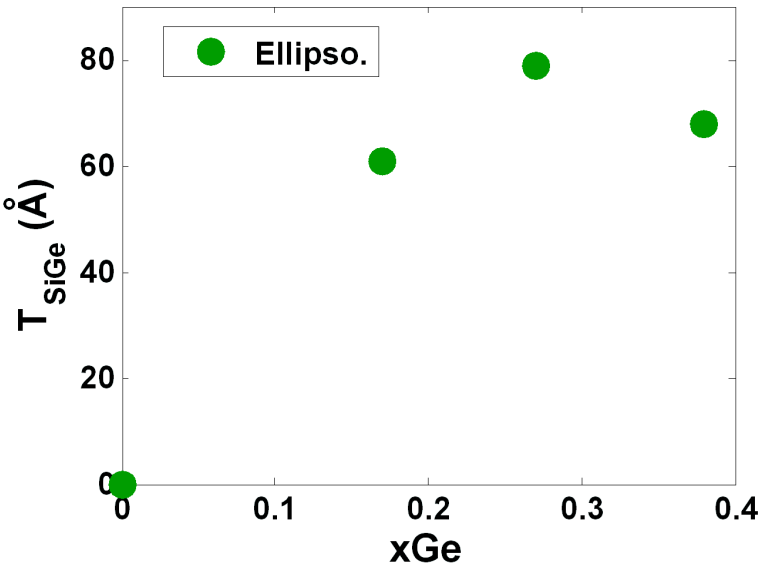


Figure 4.6: Ellipsometry measurements of $SiGe$ thickness and Germanium content for the different FDSOI tested wafers.

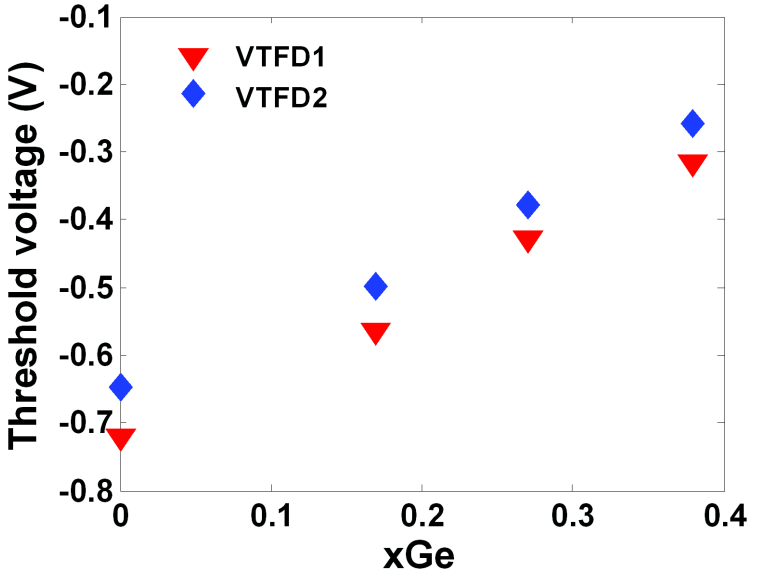
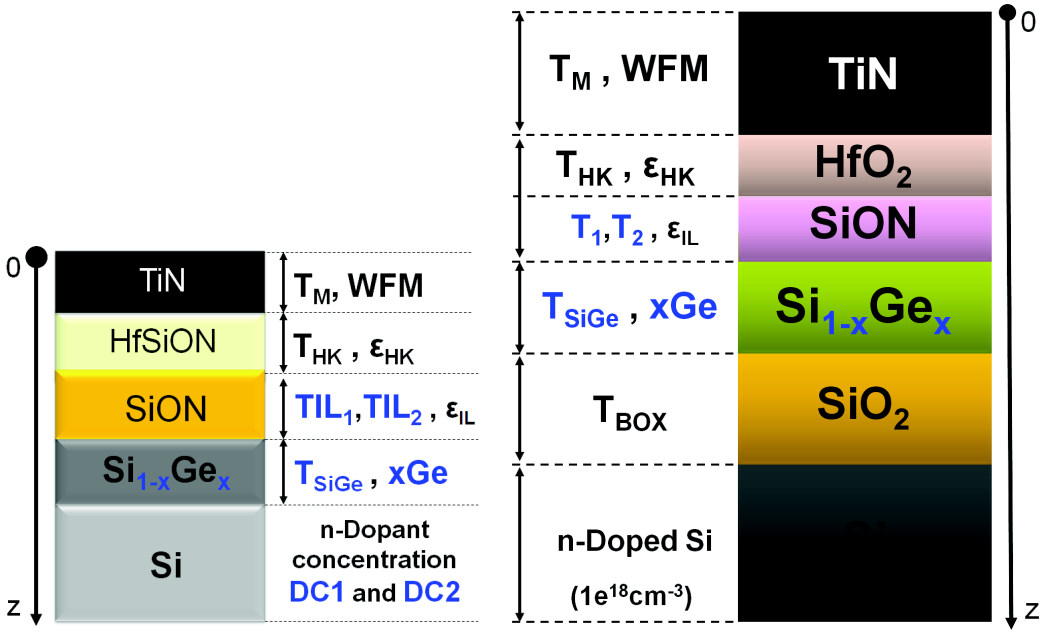


Figure 4.7: $SiGe$ FDSOI pFETs VT as a function of xGe (VT is extracted at 40% of $C^{max,inv}$).

4.3 Simulations

To analyse the impact of the Ge concentration on pMOS parameters, we have simulated the C-V characteristics of $Si_{1-x}Ge_x/Si$ bulk pMOSFETs and $Si_{1-x}Ge_x$ FDSOI pFETs. The simulated structures are presented in figure 4.8.a&b. They consist of various $Si_{1-x}Ge_x$ layers (figure 4.2 & 4.6). For bulk pMOSFETs, the variation on $SiON$ thickness ($TIL1$ and $TIL2$) and threshold adjust implant dose ($DC1$ and $DC2$) leads to the three different VT splits (table 4.1).

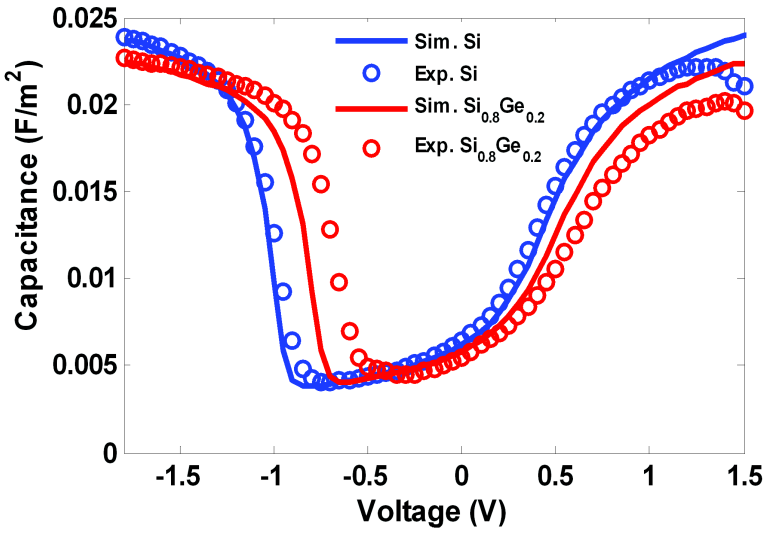
For FDSOI devices, we simulate the C-V of $Si_{1-x}Ge_x$ FDSOI pFETs with T_1 and T_2 $SiON$ thicknesses. The TiN work function is fixed at 4.67eV and 4.57eV, respectively, for bulk and FDSOI pMOS simulations in order to match the measured threshold voltage for Si VT1 and VTFD1 pFETs.
The simulations are based on self-consistently solving 1D Poisson and Schrödinger equations (PS) within the Effective Mass approximation (CEMA). Here, we have used the adjusted $M_{DOS}(HH, Si)$ ($2.5m_0$ and $1.5m_0$ respectively for Si and $SiGe$) to reproduce efficiently the C-V curves obtained using the 6-band k.p model with an in-plane numerical integration scheme (see chapter 2 on page 61). This model includes the effects of alloy composition and mechanical strain on $SiGe/Si$ band structure (see figure 2.22 on page 70).



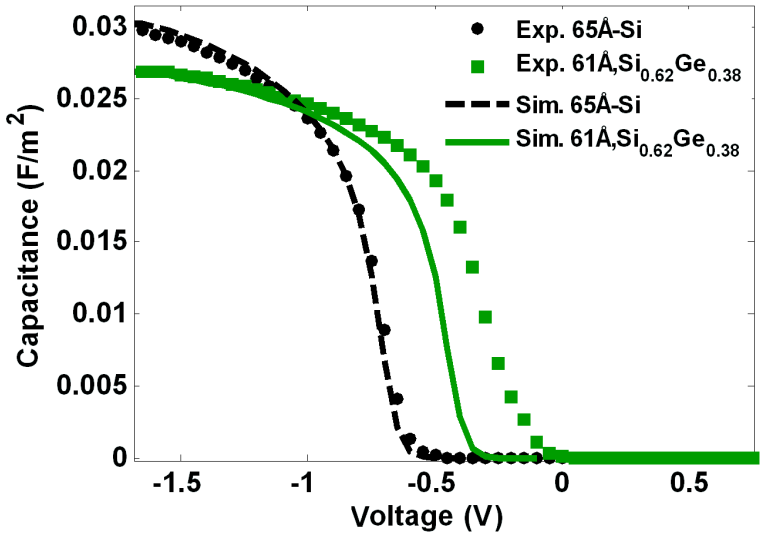
(a) (b)

Figure 4.8: The simulated $SiGe/Si$ pMOSFET (a) and $SiGe$ FDSOI pFET (b) structures. The metal gate work function is fixed at WFM=4.67eV and WFM=4.57eV for structure (a) and (b) respectively. The $Si_{1-x}Ge_x$ is biaxially strained with variable xGe and T_{SiGe} (see figure 4.2& 4.6).

Figure 4.9.a shows the simulated and measured C-V of the VT1 Si and VT1 $Si_{0.8}Ge_{0.2}/Si$ bulk pMOSFETs. A good fit is obtained for pure Si, whereas $Si_{0.8}Ge_{0.2}/Si$ evidences a 150mV shift. The comparison of measured and simulated C-V of the FDSOI pFET evidences a similar behaviour. Simulation matches the measured Si FDSOI pFET C-V. However, 160mV additional shift is needed to fit the measured $Si_{0.62}Ge_{0.38}$ FDSOI pFET C-V.



(a)



(b)

Figure 4.9: (a) The simulated C-V (Line) is compared to the measured C-V (Circle) of the VT1 Si and VT1 $Si_{0.8}Ge_{0.2}/Si$ bulk pMOSFETs. (b) The simulated C-V (Line) is compared to the measured C-V (Symbol) of the VTFD1 Si and VTFD1 $Si_{0.62}Ge_{0.38}$ FDSOI pFETs.

4.4 Ge impact on EOT parameter

An adjustment of the EOT of simulated structure is done to fit experiment in order to enable a reliable extraction of VT and VFB. For this purpose, EOT of $Si_{1-x}Ge_x/Si$ bulk pMOSFETs and FDSOI pFETs are extracted using the extraction method described in chapter 3 on page 86. Extracted EOT values are reported for the three different bulk pMOSFETs. For thick interlayer (figure 4.10) performed by oxide deposition, EOT is independent of Ge content. Whereas, it linearly increases for the two pMOSFETs with thin interlayer obtained by thermal oxidation

(figure 4.11). Up to 1.2$\mathring{A}$ EOT increase is noticed for 30% of Ge. Such observation is consistent with J. Huang et al. [8] result who showed that Ge in $SiGe$ plays a critical role in gate dielectric formation, causing a regrowth of the interfacial oxide layer [8].

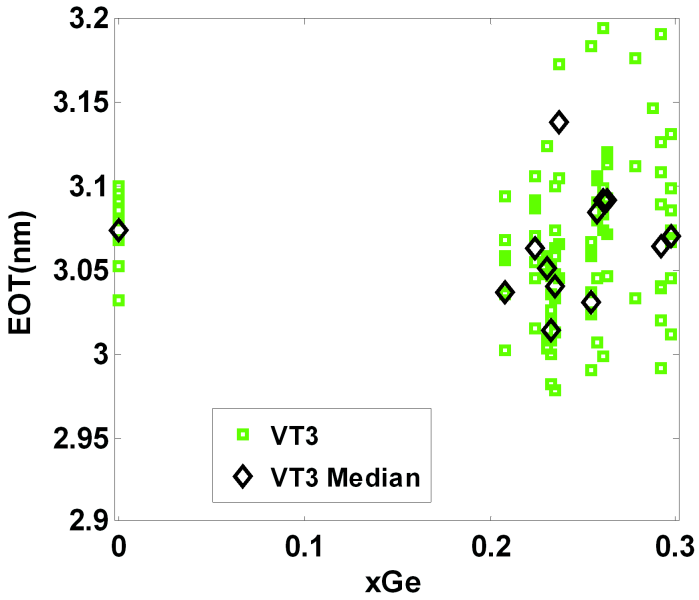


Figure 4.10: EOT estimation for pMOSFETs with thick interfacial oxide (VT3).

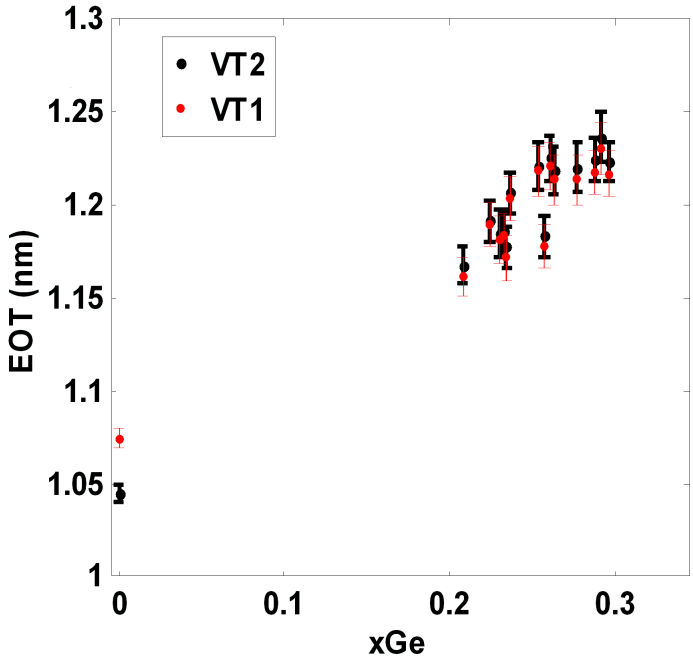


Figure 4.11: EOT estimation for pMOSFETs with thin interfacial oxide (VT1 & VT2).

4.5 $Si_{1-x}Ge_x$ material

In this section, we introduce the simulated $Si_{1-x}Ge_x$ material parameters: *Ge* concentration and *SiGe* thickness, *SiGe* doping concentration and band gap energy. These parameters are verified through comparison to C-V measurements and physico chemical characterizations.

4.5.1 *Ge* concentration and *SiGe* thickness

In UTOXPP simulations of strained *SiGe* based devices, three key parameters are needed: strain components, *Ge* concentration and *SiGe* thickness.
The *SiGe* is considered biaxially strained and the strain components are computed as in equation 2.1. The *Ge* concentration and *SiGe* thickness are measured by Ellipsometry on all samples. The *Ge* concentration Ellipsometry measurements are confirmed by Time of Flight Secondary Ion Mass spectroscopy (SIMS) [135][136] on two bulk pMOSFET samples (20.8% and 31.1% versus 17% and 30% measured by SIMS). Besides, *SiGe* thickness Ellipsometry measurements is inferred by STEM HAADF [137] (12.7nm to be compared to 12nm measured using STEM HAADF). Therefore, Ellipsometry measurements presented in figures 4.2&4.6 are considered in this chapter as *Ge* concentration and *SiGe* thickness inputs in UTOXPP simulations.

4.5.2 Doping concentration profile

VT1 and VT2 bulk pMOSFETs doping concentration profiles are simulated using Synopsis Sprocess TCAD tool. Then, they are reproduced by UTOXPP simulator. Figure 4.12 shows the simulation doping profiles in the *Si* and $Si_{0.68}Ge_{0.32}/Si$ VT1 and VT2 bulk pMOSFETs. It is important to notice that the *Si* doping concentration in VT1 pMOSFETs (solid curves) is 10 times higher than in VT2 (dashed curves) and VT3 bulk pMOSFETs. Moreover, the epitaxied *SiGe* layer on *Si* is undoped. After the final anneal, the Boron dopant in the *Si* substrate slightly diffuses in the *SiGe* layer. In subsection 2.4.4 of chapter 2, we have studied the impact of the diffused Boron dopant (in the *SiGe* layer) on the C-V curve. Slight impact of the *SiGe* doping is then noticed.

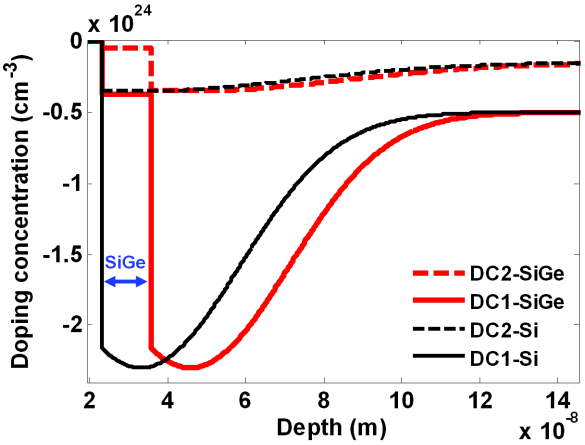


Figure 4.12: Doping concentration profiles in the *Si* and $Si_{0.68}Ge_{0.32}/Si$ VT1 and VT2 bulk pMOSFETs.

4.5.3 *SiGe* energy band gap

Using such doping concentration profile (figure 4.12), we calculate the band gap narrowing of the *Si* and *Ge* materials doped at DC1 and DC2 levels using equations 2.24 on page 60. For *SiGe* material, the BGN is linearly interpolated. Table 4.3 reports the obtained *Si* and *SiGe* band gap narrowing (ΔEg_{Si} and ΔEg_{SiGe} respectively) for the DC1 and DC2 *Si* dose implantations. A 47meV of DC1-*Si* band gap drop is expected. Whereas, 25meV band gap decrease only is estimated for the DC2-*Si*. The *SiGe* band gap narrowing seems to be not significant. Only 22meV is obtained for the DC1- $Si_{0.7}Ge_{0.3}$.

***Si* dose implantation**	**DC1**	**DC2**
$\Delta \mathbf{Eg}_{Si}$ **(meV)**	**47**	**25**
$\Delta \mathbf{Eg}_{SiGe}$ **(meV)**	**15.x+25.(1-x)**	**8.x+13.(1-x)**

Table 4.3: The estimated *Si* and *SiGe* band gap narrowing in the DC1 and DC2 *Si* dose implantations. The estimated *Si* and *Ge* BGN are computed using equations 2.24 on page 60. For *SiGe* material the BGN is linearly interpolated.

Actually, the C-V characteristic gives the possibility to determine the channel band gap energy (E_g) as explained in figure 4.13.
In this figure, (VT-VFB) is written as a function of the band gap, depletion charge (Q_{dep}), oxide capacitance (C_{ox}) and the position of the surface potential (at VT and VFB conditions) with respect to valence and conduction bands level. Thus, the comparison of the measured and simulated (VT-VFB) parameters allows the simulated band gap calibration. In fact, the given (VT-VFB) expression (figure 4.13) is valid for bulk material based devices. However, it becomes more complicated to express (VT-VFB) for *SiGe*/*Si* heterostructure based devices.

The purpose of the rest of this subsection is to determine which *Si* and *SiGe* band gap energies should be used in UTOXPP simulations to accurately simulate the C-V curve.
First the band gap narrowing is integrated for pure *Si* simulations at room temperature. Then, it will be calibrated by C-V comparison to experiments at different temperatures. The calibrated band gap (for which the simulated C-V matches the measured one) is compared to literature result. Second, for *SiGe*/*Si* simulations, we integrate the band gap narrowing in the bulk *Si* material. Because of the undoped *SiGe* layer, the *SiGe* band gap narrowing is considered negligible. Finally, the C-V simulation of the $Si_{0.8}Ge_{0.2}$/*Si* pMOSFET, taking into account the *Si* band gap narrowing in the bulk *Si*, is validated by comparison to the measured C-V at three temperatures.

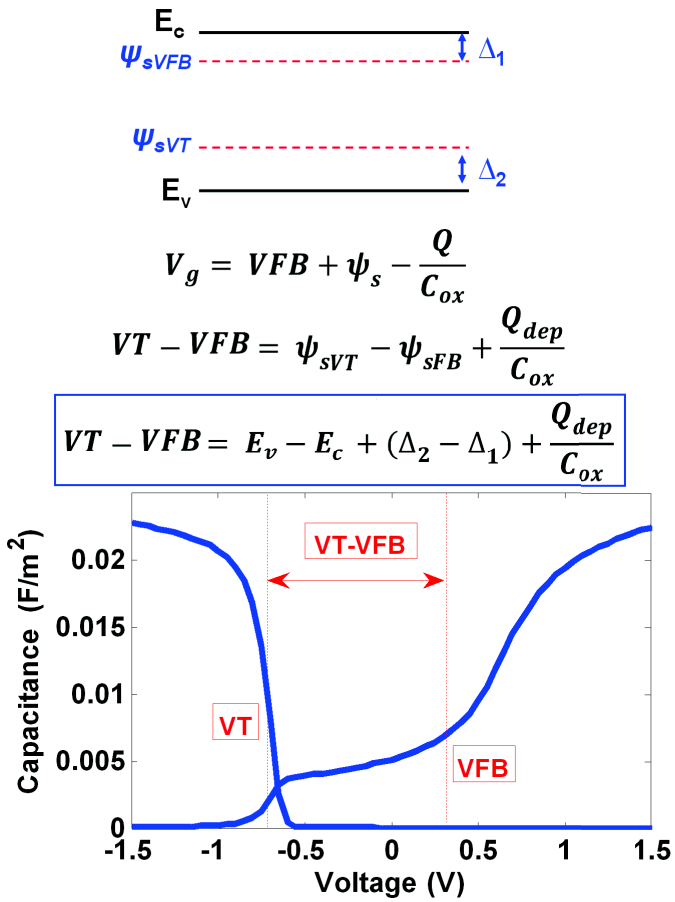


Figure 4.13: (VT-VFB) expression for channel band gap validation in bulk materials. Q and Q_{dep} are the total and depletion charges. Δ_1 and Δ_2 are the positions of the surface potential (at VT and VFB conditions) with respect to valence and conduction bands level. These are depending on the doping concentration.

The band gap narrowing of the Si doped at DC1 is estimated to be 47meV (see table 4.3). We have integrated this BGN value (∼50mV) in the simulated Si band gap at room temperature. Figure 4.14 compares the measured and simulated C-V characteristics of the VT1 Si pMOSFET with and without taking into account the band gap narrowing. A good C-V fit is observed when reducing the Si band gap by 50meV for DC1 Si pMOSFET. The same exercise is also applied to DC2 Si pMOSFETs (VT2 and VT3 pMOSFETs). A good C-V match between simulations and experiments is obtained when the Si band gap is decreased by 25mV.

In order to validate the simulated Si band gap, we have examined the (VT-VFB) response of the pure Si VT1 at various temperatures. The measured C-V at three tempratures (233K, 298K and 398K) has been compared to simulations. Figure 4.15 illustrates measured and simulated Si VT1 bulk pMOS at different temperatures.

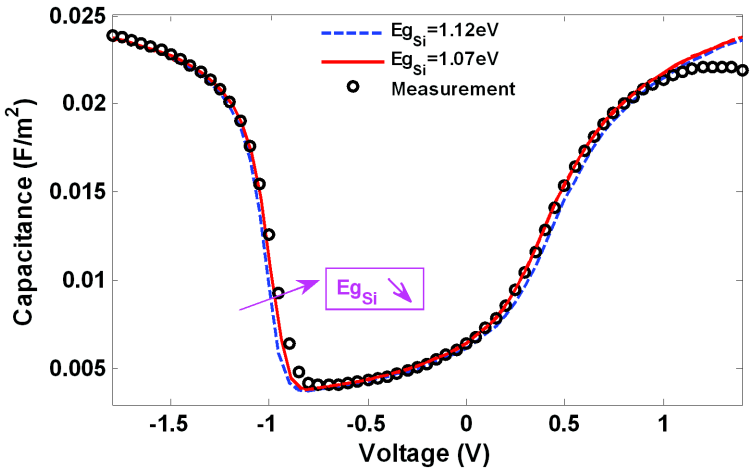


Figure 4.14: Comparison of measured and simulated C-V characteristic of the VT1 *Si* pMOSFETs with (solid line) and without (dashed line) taking into account the band gap narrowing.

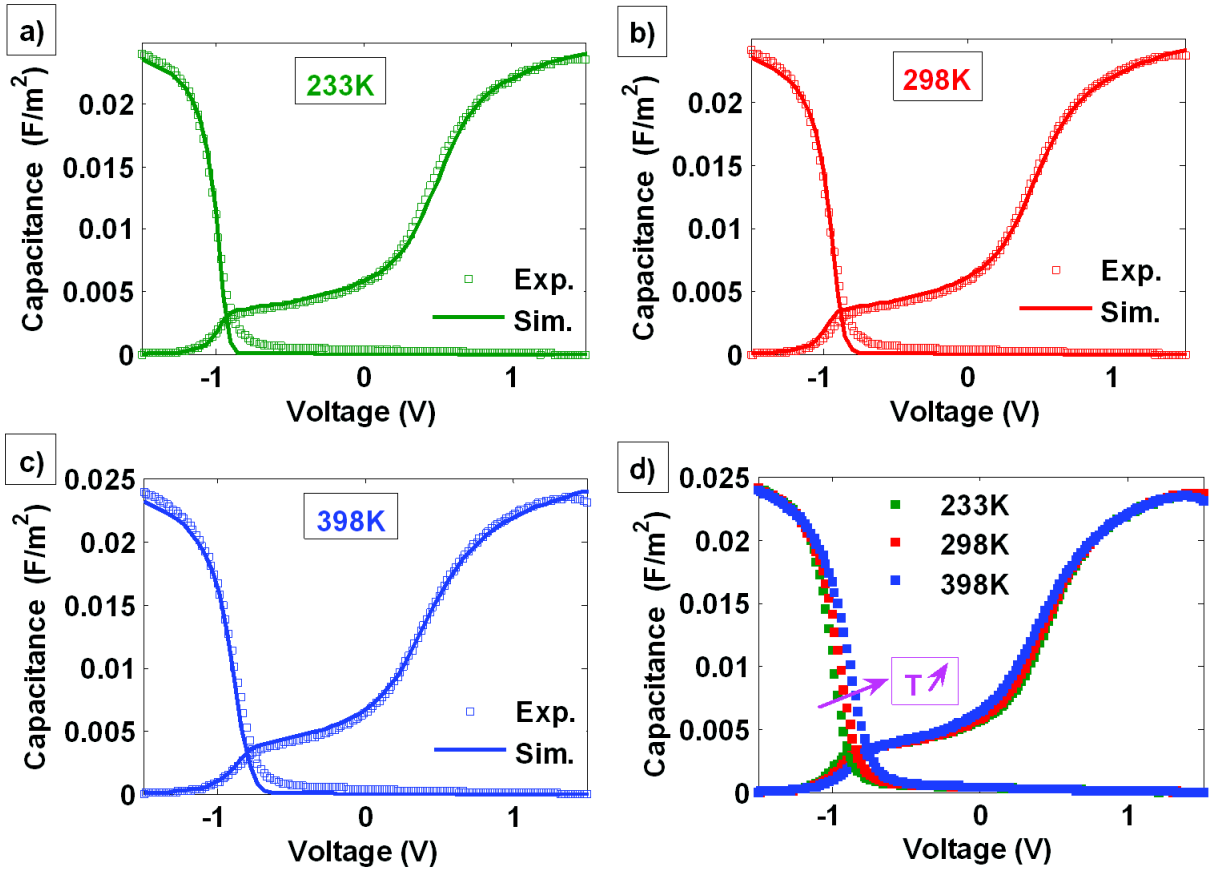


Figure 4.15: Comparison of measured and simulated C-V characteristic of the VT1 *Si* pMOSFETs at different temperatures (a&b&c). d) Measured VT1 *Si* pMOS C-V at various temperatures.

120mV VT decrease is noticed when increasing the temperature from 233K to 398K (figure 4.15.d). The comparison of measured and simulated split C-V shows a good fit (figure 4.15), confirming the Si band gap calibration. The simulated Si band gap energy corresponding to figure 4.15 is reported in figure 4.16. Linear drop, close to 80meV, is observed when increasing the temperature (from 233K to 398K.)
Figure 4.16 also reports the common undoped Si band gap empirically estimated as a function of temperature [138][139][140]. The simulated Si band gap (symbols), which considers the BGN, has the same behaviour than the empirical one (without BGN). At room temperature, we observe around 50mV discrepancy due to the BGN, confirming the validity of the simulated Si band gap.

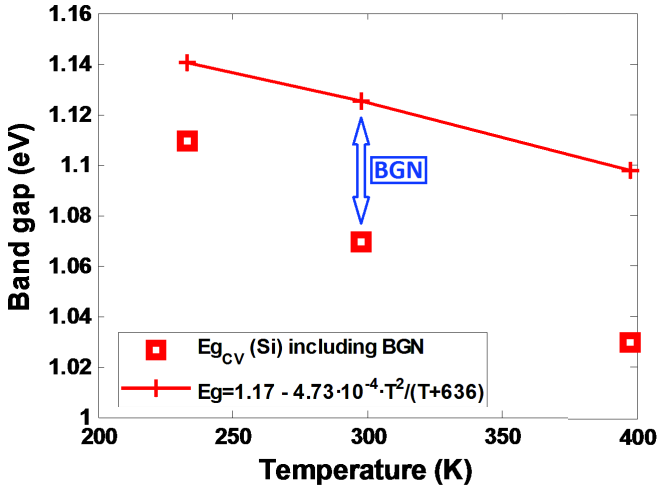


Figure 4.16: Si band gap energy including the BGN as a function of temperature.

For the $Si_{1-x}Ge_x/Si$ pMOSFETs, VT1 pMOSFETs split capacitance for $Si_{0.8}Ge_{0.2}$ has been measured at three different temperatures (T=233, 298, 398K). The validation of the simulated Si and $Si_{1-x}Ge_x$ band gap energy is assessed by comparing simulated VT1 $Si_{0.8}Ge_{0.2}$ C-V to measurements.
In all $Si_{1-x}Ge_x/Si$ C-V simulations, we have considered the Si band gap including the BGN (symbols in figure 4.16) in the pure Si substrate. The simulated biaxially strained $SiGe$ band gap energy is a quasi undoped layer (see the previous subsection). Thus, the BGN of the $SiGe$ is negligible (According to table 4.3, only 23meV is obtained for the DC1- $Si_{0.8}Ge_{0.2}$.). Therefore in $SiGe/Si$ simulations, the BGN is only considered in the Si substrate. The $Si_{0.8}Ge_{0.2}$ bandgap temperature dependence is computed using equation 2.23 on page 57.
The comparison of the measured and simulated VT1 $Si_{0.8}Ge_{0.2}$ pMOSFET C-V at various temperatures shows a good agreement, evidencing the validity of the simulated Si and $Si_{1-x}Ge_x$ band gap energy. Moreover, a similar C-V comparison at three temperatures (T=233, 298, 398K) is performed for the VT1 $Si_{0.74}Ge_{0.26}$ pMOSFET. The measured C-V is well reproduced when integrating the BGN only for the Si substrate, confirming the validity of the used band gap energies (for the Si and $Si_{1-x}Ge_x$ materials).

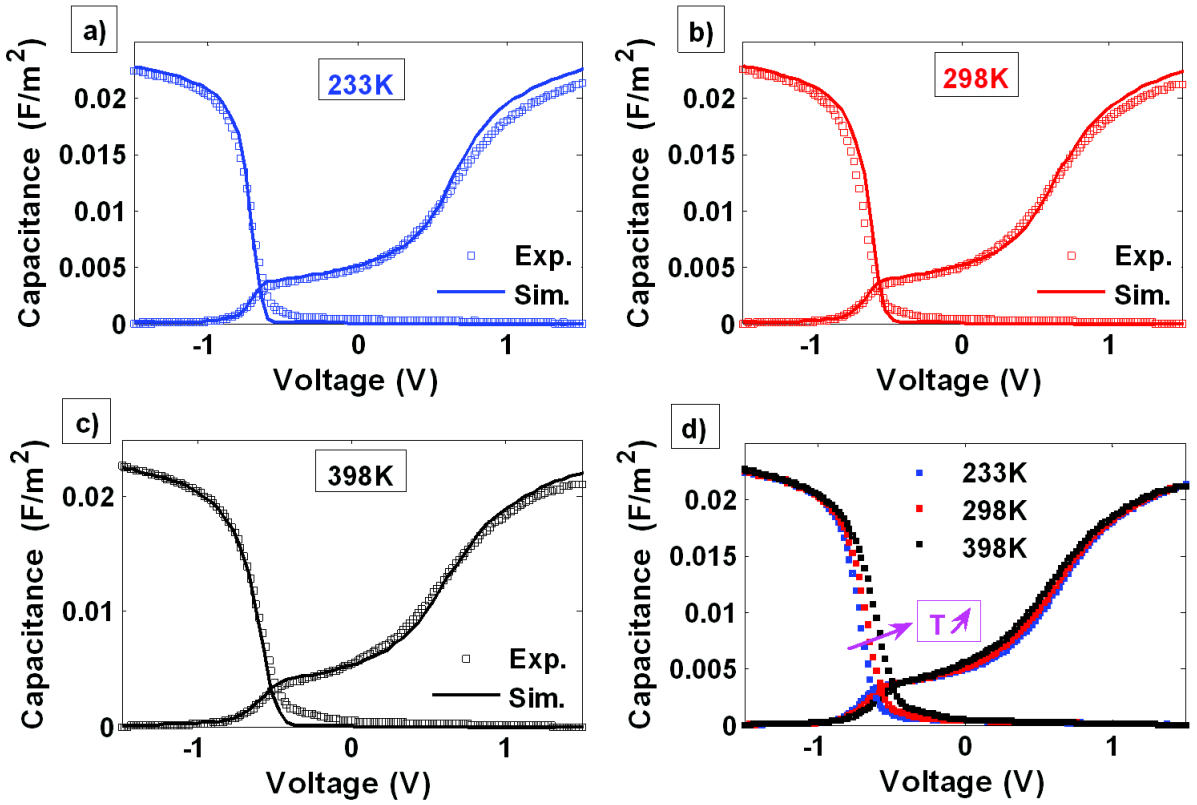


Figure 4.17: Comparison of measured and simulated C-V characteristic of the VT1 $Si_{0.8}Ge_{0.2}/Si$ pMOSFET at different temperatures (a&b&c). d) Measured VT1 $Si_{0.8}Ge_{0.2}/Si$ pMOS C-V at various temperatures.

4.6 Ge impact on C-V characteristic

To analyse the effect of Ge content on pMOSFETs parameters, experimental C-V characteristics have been compared to simulations. First (VT-VFB) parameter will be evaluated as Ge concentration increases. Then, effective metal gate work function variation will be assessed on all $SiGe$ pMOS bulk and FDSOI samples.
For the rest of this chapter, VFB corresponds to the gate bias at zero substrate charge and VT is estimated from 40% of $C^{max,inv}$ (see section 4.2.1 on page 108).

4.6.1 (VT-VFB) parameters

In this subsection, first the theoretical evolution of the VT and VFB electrical parameters as a function of Ge content is investigated. To this end, we will compare the surface potential at VFB and VT in $SiGe/Si$ pMOSFET to the conduction and valence band offsets evolution with xGe. Then, (VT-VFB) parameter dependence to the BGN is carried out. Finally, the simulated (VT-VFB) including the BGN is validated by comparison to the experiments.

We consider the $Si_{1-x}Ge_x/Si$ heterostructure based bulk pMOSFET. Figure 4.18 reports simulated surface potential (Ψ_s) at VFB and VT conditions for various xGe. In this figure, the surface potentials (at VFB and VT) of both strained and relaxed $SiGe$ on Si are compared to conduction (ΔE_c) and valence (ΔE_v) band offsets. At VT, it is important to notice that Ψ_s evolution follows ΔE_v variations. Whereas, at VFB, it remains very low compared to ΔE_c variations, especially for the noticeable variation of the ΔE_c with relaxed $SiGe$.

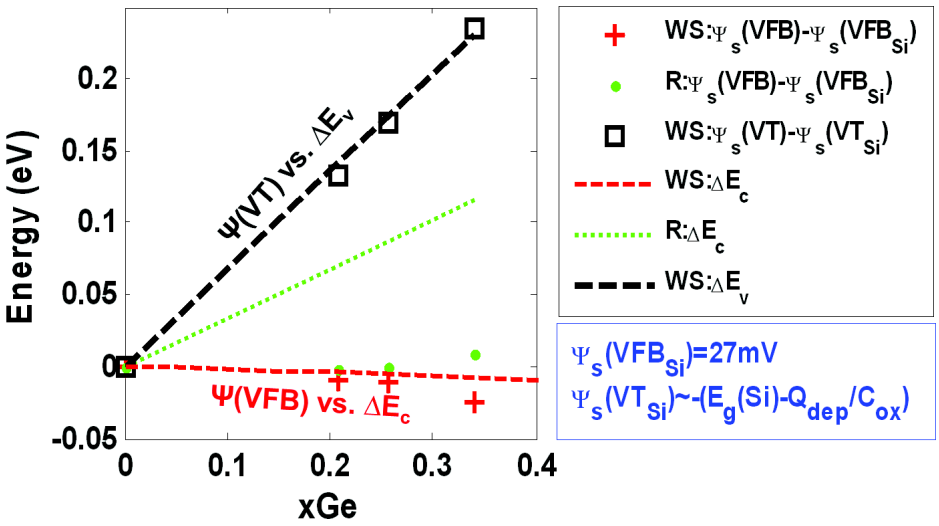


Figure 4.18: Simulated surface potential Ψ_s at VFB and VT versus band offsets, VT2 pMOS with (WS) or without (R) strain. Vg=$\Delta\Phi_{ms} + \Psi_s - \frac{Q_{dep}}{C_{ox}}$, $\Delta\Phi_{ms}$=0.45eV.

In figure 4.19, we study the variation of the surface potential at VFB ($\Psi_s(VFB)$) as a function of the strained $SiGe$ thickness (T_{SiGe}). The Si and $SiGe$ doping concentrations are varied and studied with a classical Poisson simulation tool using Boltzmann equation and expected strained band structure evolution with xGe (figure 2.9). As T_{SiGe} increases, we notice a $\Psi_s(VFB)$ evolution from value related to bulk doping level to surface doping level with a typical transition in the range of the extrinsic Debye length of the above layer doping level. Bold lines in figure 4.19 correspond to surface layer without Germanium. As Ge content increases, Ψ_s decreases due to ΔE_c between the Si and $SiGe$. The shift is also depending on T_{SiGe} with a characteristic length related then to the extrinsic Debye length of the bulk doping level. Such simulations confirm that the expected VFB should not significantly vary in the case of $Si_{1-x}Ge_x/Si$ heterostructure based bulk pMOSFET, confirming the simulation results of figure 4.18.
As a conclusion, for a $SiGe/Si$ heterostructure, VT follows the valence band offset variation with xGe. However, VFB seems quasi constant with Ge content variation even with noticeable variation of the conduction band offset with xGe.

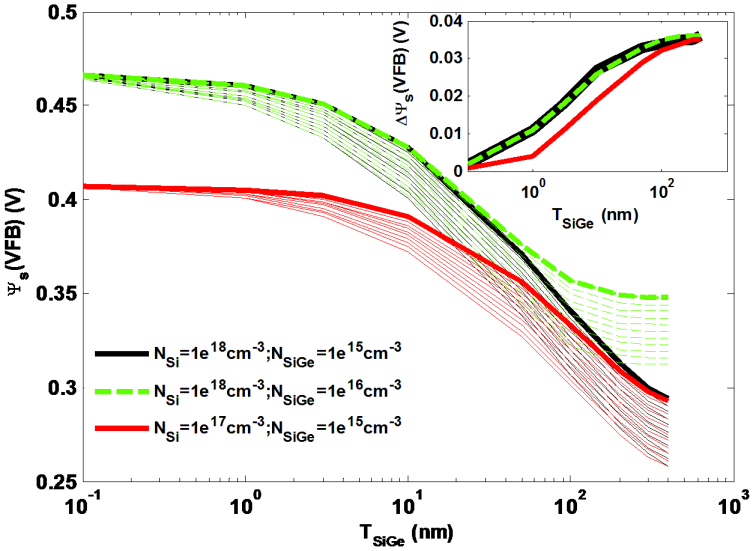


Figure 4.19: The variation of the surface potential at VFB as a function of the $SiGe$ thickness for different Si and $Si_{1-x}Ge_x$ dopant concentrations (xGe varies from 0 to 0.34). Inset: same for $\Delta\Psi_s(\text{VFB})=\Delta\Psi_s(\text{VFB})^{Si}$-$\Delta\Psi_s(\text{VFB})^{Si_{0.66}Ge_{0.34}}$.

$Si_{1-x}Ge_x$ bulk pMOSFETs presented in figure 4.8 are simulated using UTOXPP. For pure Si simulations, the EOT reported in section 4.4 is used to fit the measured C-V. For $SiGe$ simulations, only the EOT of the $Si_{0.78}Ge_{0.22}$ pMOS is adjusted to match the measured capacitance. Then, the EOT is considered constant for all $SiGe/Si$ C-V simulations.
In order to accurately simulate the C-V curves, we have integrated the band gap narrowing of the Si to simulate the C-V curve of the pure Si. Moreover, the BGN in the Si substrate is included for all $SiGe/Si$ simulations (see subsection 4.5.3). The simulated (VT-VFB) with (W) and without (WO) taking into account the band gap narrowing is plotted in figure 4.20. 100mV discrepancy is noticed for pure Si pMOSFET. Up to 60mV difference is also observed

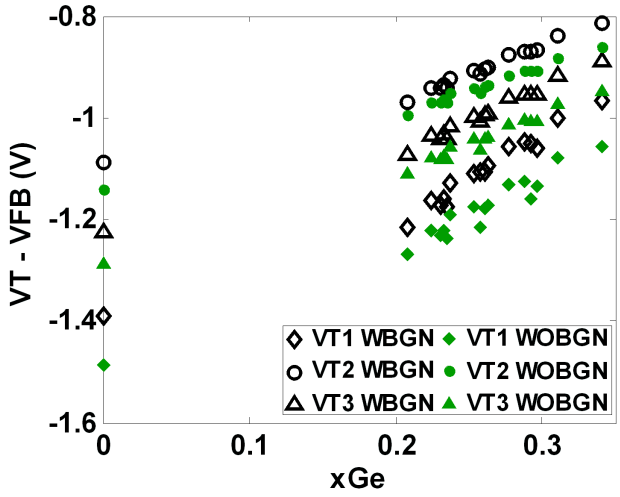


Figure 4.20: Simulated (VT-VFB) with (W) and without (WO) taking into account the BGN.

for $SiGe/Si$ pMOSFETs proving the necessity of considering the BGN in all simulations.
The validation of the simulated (VT-VFB) (figure 4.20) can be achieved by confrontation with the measured (VT-VFB). From C-V simulation at zero substrate charge, we get the simulated capacitance CFB_{Sim} at flat band VFB_{Sim}. A comparison between simulation and experiment for all samples evidences a slight discrepancy at strong inversion related to the EOT variation with xGe (see section 4.4). For a reliable measured VFB extraction, we calculate from $C^{max,inv}$ (maximum capacitance in strong inversion) the experimental capacitance CFB_{Exp} at VFB condition [141]:

$$\frac{1}{CFB_{Exp}} = \frac{1}{CFB_{Sim}} + \frac{1}{C_{Exp}^{max,inv}} - \frac{1}{C_{Sim}^{max,inv}} \tag{4.1}$$

where the measured and simulated $C^{max,inv}$ are defined at the same gate voltage in strong inversion. The CFB_{Exp} determination allows the measured VFB extraction. Concerning the threshold voltage, it is extracted from measured and simulated C-V (at 40% of $C^{max,inv}$). In C-V simulations, the EOT which matches the measured C-V of the $Si_{0.78}Ge_{0.22}$ VT_i pMOS is used to simulate all VT_i $SiGe$ bulk pMOSFETs. Thus, extracted VT may be slightly affected by the EOT increase with xGe, which is assumed to be around $0.5\mathring{A}$ for VT1 and VT2 (see section 4.4).
(VT-VFB) obtained from measured C-V are then compared to simulations including the BGN (figure 4.21). We notice that the BGN integration improves the simulated (VT-VFB) result (see figure 4.20). For pure Si, we reproduce the measured (VT-VFB). For $SiGe/Si$ pMOSFETs, we obtain a global agreement between the measured and simulated (VT-VFB), although the slight difference observed for $SiGe$ VT2 pMOSFETs.
As seen on figures 4.18 and 4.19, VFB should not significantly vary with xGe. On the contrary, VT follows the ΔE_v increase with xGe increase. Thus, (VT-VFB) should depend mainly on ΔE_v. The global agreement (figure 4.21) for the three different VT_i (see table 1) is noticeable and proves that the simulation tool accounts well for the relative evolution of valence band levels with Ge content. Remaining slight discrepancies could be explained by uncertainties on interface states and the EOT increase with xGe, which is not considered in the simulation of VT.
To conclude, we have shown that (VT-VFB) should depend mainly on ΔE_v. Including the BGN in all simulations ameliorates the simulated (VT-VFB). As a result, the measured (VT-VFB) are well reproduced for pure Si pMOSFETs. A global agreement is also noticed for the three different $SiGe$ VT_i pMOSFETs, confirming the validity of the simulated ΔE_v.

4.6.2 Effective metal gate work function

In this section, we focused our study on the C-V shift (figure 4.9) observed between simulations and measurements when introducing Ge in the pMOS channel (see section 4.3). First, we will investigate the effect of Ge concentration on the diferent VT_i bulk pMOSFETs. Then, the shift will be evaluated by comparing experiments and simulations of $Si_{1-x}Ge_x$ FDSOI pFETs technology.
ΔWF_{eff} (VFB_{Exp} - VFB_{Sim}) corresponds to the additional metal gate work function shift (ΔWFM) from reference simulation level (WFM=4.67eV) which is needed to match experi-

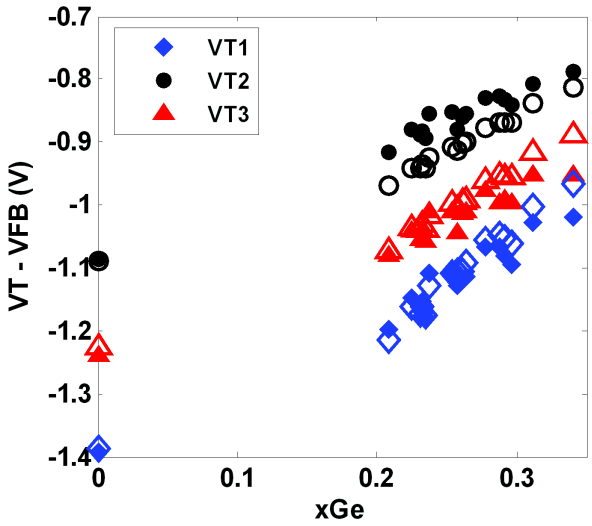
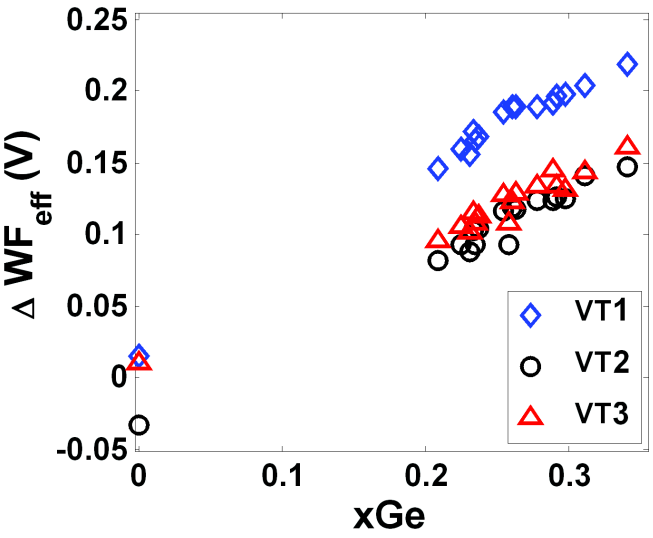
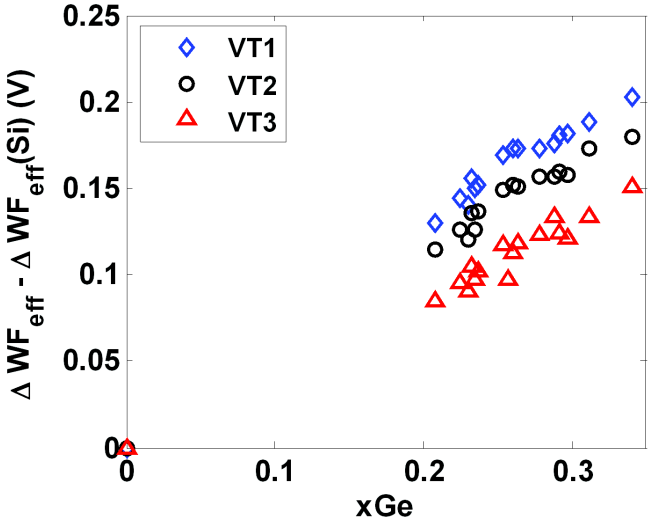


Figure 4.21: (VT-VFB) from measured (Filled symbols) and simulated C-V (Empty symbols).

mental C-V curves. Figure 4.22.a reports the ΔWF_{eff} shifts of the three different VT_i bulk pMOSFETs as a function of the *Ge* concentration.
For pure *Si*, unexpected 50mV shift is observed between the *Si* VT1 and VT2, which have a different *Si* implant dose. This discrepancy may be due to uncertainties on substrate doping profile. Moreover, close WFM values are expected for the same metal gate stack of the *Si* VT2 and VT3 (same doping profile and thicker oxide). 40mV increase from VT2 to VT3 is coherent with a roll-off effect at thinner EOT [14][142][143].
Referring to pure *Si* VT_i bulk pMOSFETs, $Si_{1-x}Ge_x$ VT_i ΔWF_{eff} are plotted in figure 4.22.b. The linear variations of ΔWF_{eff} with xGe are noticeable. Up to 200mV additional increase of the ΔWF_{eff} is observed for VT1 pMOSFETs when integrating 34% *Ge*.
In fact, *SiGe* band structure effects are taken into account via Ψ_s at VFB. As shown in figure 4.18, VFB should vary only slightly with *SiGe* conduction band offset. So, the observed ΔWF_{eff} levels implies an additional extrinsic cause.
The same study was performed on *SiGe* FDSOI pFETs (figure 4.8.b). Figure 4.23.a illustrates the ΔWF_{eff} (VT_{Exp} - VT_{Sim}) that we must add to the reference simulation level (WFM=4.57eV) to match measured C-V curves. It is clear from this figure that in addition to classical *SiGe* band structure effect (figure 4.18), we must account for an additional VT increase proportional to *Ge* contents. Figure 4.23.b shows that the FDSOI ΔWF_{eff} shift follows the same trend than bulk pMOSFETs (figure 4.8.a). This trend is also observed for the two different IL despite the difference in process between FDSOI and bulk technology. Indeed, the high-k dielectric is different (HfO_2 instead of HfSiON) as well as the *SiGe* process (condensation instead of epitaxy).
We need now to investigate the origin of this gate work function shift induced by Germanium. In the rest of this chapter, the different hypothesis will be considered in front of the global electrical measurements as well as physical characterizations.



(a)

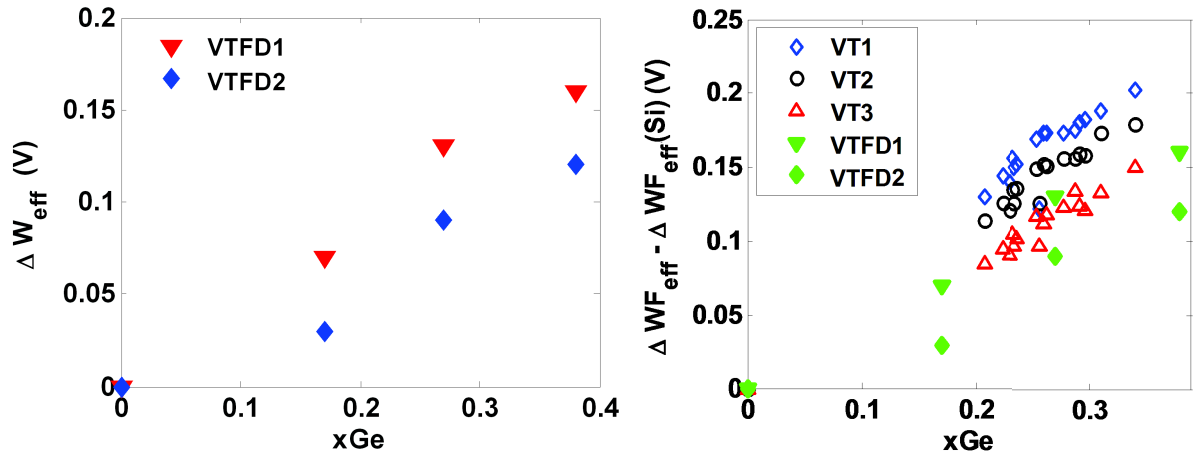


(b)

Figure 4.22: (a) $Si_{1-x}Ge_x$ bulk pMOSFETs effective work function shift with Germanium content. (b) ($\Delta WF_{eff}(Si_{1-x}Ge_x)$ - ΔWF_{eff} (Si)) as a function of the Ge content.

4.7 Effective metal gate work function shift

In fact, all simulated pFETs presented in section 4.3 are considered as ideal MOS devices. So, oxide layers are treated as ideal insulators, where there are no oxide defects. However, we have shown in chapter 1 that in real MOS devices, dielectrics may include various types of traps, charges and dipoles (see subsection 1.2.2 on page 23). That's why, an ideal MOS device does not agree with experimental results.
In the previous section, we have highlighted a gate work function shift (ΔWF_{eff}) that must



(a) (b)

Figure 4.23: (a) $Si_{1-x}Ge_x$ FDSOI pFETs effective work function shift with Germanium content. (b) (ΔWF$_{eff}(Si_{1-x}Ge_x)$ - ΔWF$_{eff}$ (Si)) as a function of the Ge content for bulk and FDSOI technologies.

be added to reference simulation level in order to reproduce the measured C-V curves. In fact, such simulated ΔWF$_{eff}$ shift (figure 4.23.b) accounts for oxide charges and dipoles effects in dielectrics as well as metal gate evolution. ΔWF$_{eff}$ can be written as:

$$\Delta WF_{eff} = \Delta WF_{eff}^{IT} + \Delta WF_{eff}^{Oxide.Ch} + \Delta WF_{eff}^{Dipoles} \tag{4.2}$$

where ΔWF_{eff}^{IT} is the part of metal gate work function shift due to the presence of interface trapped charges at the IL/$SiGe$ interface (see figure 1.10.(B)). The ΔWF_{eff}^{IT} expression was written in subsection 1.2.2.3 on page 25.
$\Delta WF_{eff}^{Oxide.Ch}$ and $\Delta WF_{eff}^{Dipoles}$ are the metal gate work function shifts due to the existence of dielectrics charges and dipoles in the oxide/metal gate stack. They can be expressed as:

$$\begin{cases} \Delta WF_{eff}^{Oxide.Ch} = \Delta_{HK}^{Ch} + \Delta_{HK/IL}^{Ch} + \Delta_{IL}^{Ch} + \Delta_{SiGe/IL}^{Ch} \\ \Delta WF_{eff}^{Dipoles} = \Delta_{M/HK} + \Delta_{HK/IL} + \Delta_{IL/SiGe} \end{cases} \tag{4.3}$$

where Δ_i is the part of metal gate work function shift caused by dipoles at 'i' interface. Δ_{HK}^{Ch}, $\Delta_{HK/IL}^{Ch}$, Δ_{IL}^{Ch} and $\Delta_{SiGe/IL}^{Ch}$ are metal gate work function shifts produced respectively by:
(a) oxide charges at the bulk of the HK insulator,
(b) oxide charges at the HK/IL interface,
(c) oxide charges in the bulk interfacial layer,
(d) a layer of fixed oxide charges at the $SiGe$/IL interface.
In chapter 1, we have schematized these oxide charges ((a), (b), (c) and (d)) in figure 1.10.(B). Their expressions are also given in equations 1.9 and 1.8 in subsection 1.2.2.4 on page 26.

4.8 Ge impact on VT and VFB understanding

In the previous section, we have shown in equation 4.2 that the gate work function shift induced by *Ge* can be attributed to the presence of charges in dielectrics or dipoles at oxide/gate stack interfaces. In this section, we focus to explain the origin of such observed metal gate work function shift (figure 4.23.b). To this end, first, effects of interface states and charges in dielectrics will be investigated. Then, the presence of dipoles at oxide/gate stack interfaces (TiN/HK or HK/IL or IL/SiGe) will be assessed using physicochemical characterizations.

4.8.1 Oxide charges and interface states effects

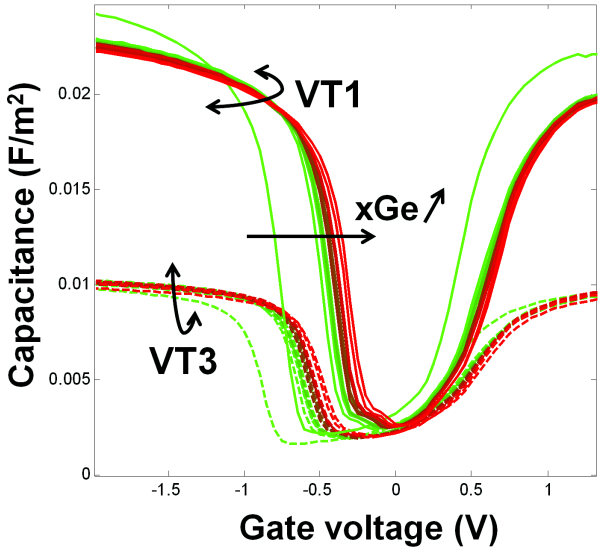
In this subsection, firstly, we report on the measurements of interface states for the *SiGe* bulk pMOSFETs and FDSOI pFETs. Measured equivalent interface states densities (D_{it}) for both bulk and FDSOI technologies will be estimated and their impact on the effective work function will be investigated. Secondly, we explore the expressions of the part of $\Delta\mathrm{WF}_{eff}$ shift caused by oxide charges in HK and IL dielectrics. These expressions are combined with the observed $\Delta\mathrm{WF}_{eff}$ (figure 4.23.b) for thin and thick IL in order to understand the cause of the metal gate work function shift in *SiGe* based devices.

4.8.1.1 Interface states effects

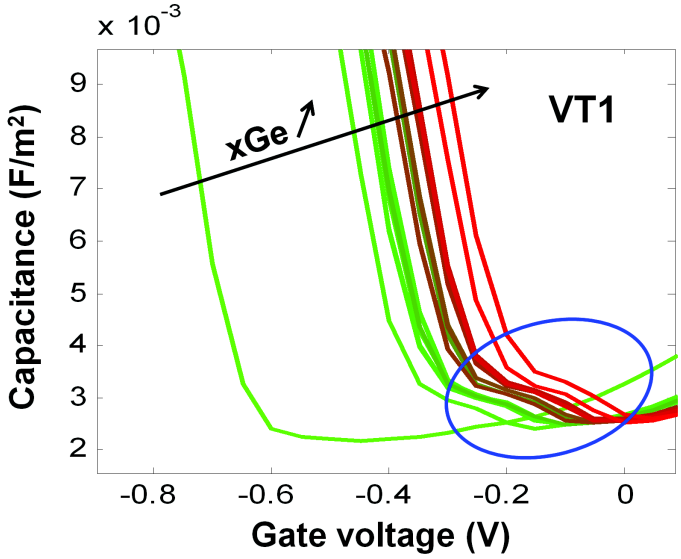
Here, we will start by studying interface states effects in bulk pMOSFETs. Then, we will investigate the part of the gate work function shift caused by interface states in the FDSOI pFETs.

Figure 4.24.a illustrates the measured C-V characteristics of the VT1 and VT3 pMOSFETs at 100khz frequency for the various *Ge* contents. For the VT1 pMOS, we notice a slight C-V "bump" at weak inversion (figure 4.24.b) which is observed for *SiGe* VT1 devices only. The occurred C-V "bump" in weak inversion seems to be insensitive to the *Ge* concentration increase. Besides, we have compared the gate-to-channel capacitance (CGC) of the *Si*, $Si_{0.8}Ge_{0.2}$ and $Si_{0.66}Ge_{0.34}$ VT1 pMOSFETs at 90khz and 30khz frequencies (figure 4.25). It is clear from figure 4.25 that the CGC of pure *Si* does not depend on the frequency (F). However, for the *SiGe* pMOSFETs, the observed C-V "bump" at weak inversion increases when decreasing the frequency. Thus, some interface traps can be suspected when integrating *Ge* in the channel of the pMOS.

C. Diouf [144] has evaluated the equivalent interface states density (D_{it}) on the $Si_{0.7}Ge_{0.3}$ VT1 pMOSFET. $5\times10^{11}\mathrm{cm}^{-2}$ D_{it} has been measured using the charge pumping method [145]. According to equation 1.3 (see subsection 1.2.2.3 on page 25), the part of metal gate work function shift ΔWF_{eff}^{IT}, due to the presence of the measured interface trapped charges, is 28mV only. The computed ΔWF_{eff}^{IT} (using equation 1.3) is too low compared to the 180mV $\Delta\mathrm{WF}_{eff}$ shift shown in figure 4.23.a. Thus, in bulk pMOSFETs, the presence of interface states in the IL/*SiGe* interface can not explain the totality of the observed metal gate work function shift induced by *Ge* (figure 4.23.a).



(a)



(b)

Figure 4.24: (a) VT1 and VT3 $Si_{1-x}Ge_x$ pMOSFETs measured C-V characteristics at 100khz frequency. (b) VT1 $Si_{1-x}Ge_x$ pMOSFETs measured C-V shows a slight "bump" at weak inversion.

Concerning FDSOI pFETs, interface states have been measured and their impact on VT estimated courtesy of CEA-Leti X. Garros. Four $Si_{1-x}Ge_x$ FDSOI pFETs have been considered with different IL nitridation:
A− the VTFD1 and VTFD2 nitrided at "N0" nitride concentration (see table 4.2).
B− the VTFD1-N1 and VTFD1-N2 with the same IL thickness (T_1), where N1 and N2 are respectively their nitride concentration in the IL dielectric (N0>N2>N1).

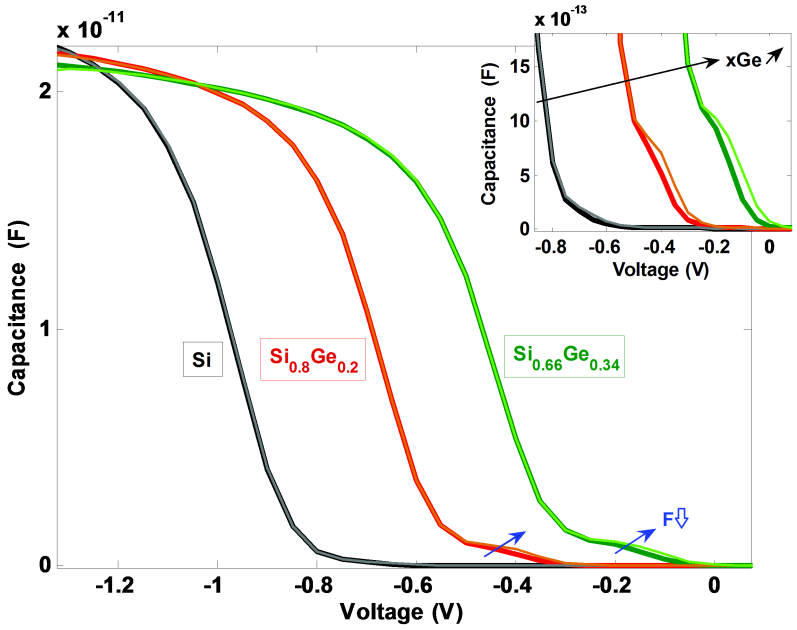
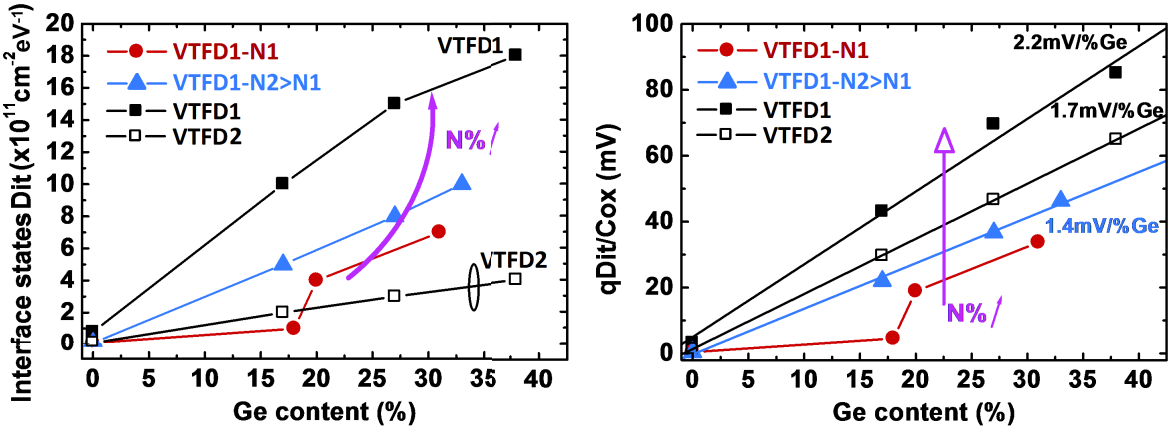


Figure 4.25: Gate-to-channel capacitance of the Si, $Si_{0.8}Ge_{0.2}$ and $Si_{0.66}Ge_{0.34}$ VT1 pMOSFETs at 90khz (dark curves) and 30khz (light curves) frequencies.

The Ge concentration varies from 17% to 38%. Pure Si FDSOI pFETs is chosen as reference. Figure 4.26.a reports the estimation of the interface traps density (D_{it}) using the conductance method [146]. It is important to mention that estimated threshold votage shift from D_{it} measurements assumes a constant level throughout all the band gap. In fact, conductance method only evaluates D_{it} at certain energy in band gap. So, extrapolating this value to the whole band gap may overestimate its influence.
Figure 4.26.a illustrates the increase of interface traps density with the Ge concentration. Concerning FDSOI with same IL thickness (T_1) and different nitride concentrations, discrepancy of the measured D_{it} is noticed for VTFD1, VTFD1-N1 and VTFD1-N2. The interface states density is reduced when the nitride concentration of the IL dielectric is decreased. Comparing VTFD1 and VTFD2 results (same nitridation and different IL thicknesses), better interface quality is expected for thicker EOT (VTFD2). The D_{it} of the VTFD2 are around the quarter of the VTFD1 results.
Obviously, such evaluated D_{it} (figure 4.26.a) are expected to induce a VT shift. If constant D_{it} level is assumed throughout all the band gap, it equals $(\frac{qD_{it}}{C_{ox}})$. Such induced VT shift is reported in figure 4.26.b. We notice that the VT shift depends on the IL nitridation and thickness. It increases when increasing the nitride content in the IL. The estimated interface states for the $Si_{0.62}Ge_{0.38}$ VTFD1 would result in 85mV shift. Moreover, the comparison of VTFD1 and VTFD2 results shows that it is reduced for thicker EOT.
Meanwhile, VT from measured capacitance of all FDSOI pFETs (VTFD1, VTFD2, VTFD1-N1 and VTFD1-N2) has been extracted. Figure 4.27 reports the measured $SiGe$ pFETs threshold voltage shift (ΔV_t), referred to pure Si VT (ΔV_t=VT($SiGe$)-VT(Si)). It is clear from this figure that VT shift is independent of the nitride content and IL thickness change. The ΔV_t

agreement for all *SiGe* FDSOI pFETs is noticeable. ΔV_t discrepancy is only observed on two *SiGe* VTFD1-N1.
Let's remember that the ΔWF_{eff}^{IT} shift, caused by the D_{it}, should depend on the IL nitridation and thickness (figure 4.26). However, the measured ΔV_t seems insensitive to the nitride content and IL thickness increase. The same ΔV_t is obtained with VTFD1-N1 having the lowest D_{it} density. Such different behaviour between the $(\frac{qD_{it}}{C_{ox}})$ shift and measured ΔV_t proves that interface states can not explain the totality of the ΔWF_{eff} shift induced by *Ge* (figure 4.23.b). Moreover, explaining ΔWF_{eff} shift with D_{it} can hardly assume a shift equalling $(\frac{qD_{it}}{C_{ox}})$. In most, identified defects trap are located in the half part of the band gap, usually donors near the valence band and acceptors near the conduction band [147][148]. Therefore, a maximum 42mV shift could be explained by interface states.



(a) (b)

Figure 4.26: (a) Measured density of interface states for the VTFD1, VTFD2, VTFD1-N1 and VTFD1-N2 FDSOI pFETs. (b) Estimated part of work function shift, due to the interface states presented in (a), for the VTFD1, VTFD2, VTFD1-N1 and VTFD1-N2 FDSOI pFETs.

As a conclusion, for bulk pMOSFETs, the measured C-V characteristics of the *SiGe* VT1 pMOS showed a slight C-V "bump" at weak inversion depending on the frequency. Thus, some interface states can be suspected when integrating *Ge* in the pMOSFETs. Such result is confirmed by D_{it} measurement using the charge pumping method. From this D_{it} estimation, only 28mV shift related to D_{it} is evaluated for the $Si_{0.7}Ge_{0.3}$ VT1 pMOSFET.
Besides, the investigation of interface states effects in *SiGe* FDSOI pFETs has shown a dependence with the IL nitridation and thickness. Therefore, VT shift $(\frac{qD_{it}}{C_{ox}})$, due to the interface states, should increase with the nitride content increase and decrease for thicker EOT. But, such $\frac{qD_{it}}{C_{ox}}$ dependence is not observed on the measured threshold voltage shift (figure 4.27). In fact, a noticeable agreement of ΔV_t for all *SiGe* FDSOI pFETs were observed. As a result, the ΔWF_{eff} shift induced by *Ge* for bulk and FDSOI pFETs (figure 4.23.b) can not be explained by the presence of interface states. In addition, interface states in the lower part of the band

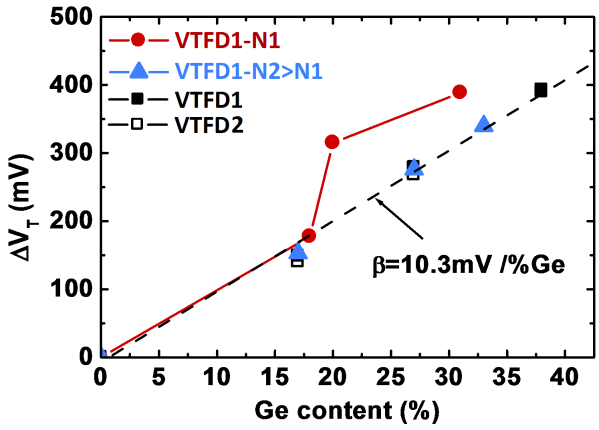


Figure 4.27: Measured VT shift (ΔV_t=VT($SiGe$)-VT(Si)) for the VTFD1, VTFD2, VTFD1-N1 and VTFD1-N2 FDSOI pFETs.

gap are expected to be donnors and would then lead to negative VT shift contrary to what is experimentaly obvserved [147][148].

4.8.1.2 Oxide charges effects

In figure 4.23.b, the linear variation of ΔWF_{eff} with Ge concentration increase is noticeable. This linear dependence suggests a Ge diffusion effect on gate stack effective work function. So, maybe Ge updiffuses into the oxide/gate stack and creates charges in the bilayer oxide (HK/IL) or dipoles at interfaces. In this subsection, we dicuss if oxide charges in the IL and HK dielectrics can explain the ΔWF_{eff} induced by Ge.

In chapter 1, we have given the part of metal gate work function shift ΔWF_{eff} due to the presence of charges in the HK (Δ^{Ch}_{HL} and $\Delta^{Ch}_{HK/IL}$) and IL (Δ^{Ch}_{IL} and $\Delta^{Ch}_{SiGe/IL}$) insolators (see subsection 1.2.2.4). Under the assumption of a constant oxide charge distribution, these are expressed as:

$$\begin{cases} \Delta^{Ch}_{HK/IL} = -\dfrac{Q_{f,HK}}{\varepsilon_{HK}\varepsilon_0} T_{HK} \\ \Delta^{Ch}_{HK} = -\dfrac{\rho_{HK}}{\varepsilon_{HK}\varepsilon_0}\dfrac{T^2_{HK}}{2} \\ \Delta^{Ch}_{SiGe/IL} = -\dfrac{Q_{f,IL}}{\varepsilon_{SiO_2}\varepsilon_0} EOT \\ \Delta^{Ch}_{IL} = -\dfrac{\rho_{IL}}{\varepsilon_{IL}\varepsilon_0}\dfrac{T^2_{IL}}{2} + \dfrac{\rho_{IL}}{\varepsilon_{HK}\varepsilon_0} T_{IL} T_{HK} \end{cases} \tag{4.4}$$

From these equations, we notice that $\Delta^{Ch}_{HK/IL}$ (due to the interface charges in the HK) varies linearly with the HK thickness (T_{HK}). Whereas, the Δ^{Ch}_{HK} (caused by charges in the bulk of the HK) is proportional to $(\frac{T^2_{HK}}{2})$. Concerning charges in the IL, the $\Delta^{Ch}_{SiGe/IL}$ (due to interface charges) should depend linearly on the EOT. Δ^{Ch}_{IL} (caused by charges in the bulk of the IL oxide) is related to $(\frac{T^2_{IL}}{2})$ and $(T_{IL} \times T_{HK})$.

Let's remember that the $HfSiON$ high-k dielectric is simultaneously deposited for all VT_i bulk pMOSFETs. Despite of the Ge concentration variation, $SiGe$ VT_i bulk pMOSFETs integrate the same HK oxide with an eqivalent HK thickness. According to expresssions of $\Delta^{Ch}_{HK/IL}$ and Δ^{Ch}_{HK}, if we suppose the presence of oxide charges in the HK, ΔWF_{eff} must be equal for VT1, VT2 and VT3 bulk pMOSFETs (with the same xGe). Moreover, a nearly similar ΔWF_{eff} is observed for VT1, VT2 and VT3 pMOSFETs (figure 4.23.a). Thus, perhaps, Ge updiffuses into the HK dielectric and causes charges at the HK/IL interface or in the bulk of the HK, which induces the ΔWF_{eff}. This htpothesis will be disproved in the next subsection using physicochemical analysis.
Concerning charges in the IL, the IL thicknesses in VT3 and VTFD2 pMOS are three times thicker than those in VT2 and VTFD1 (see table 4.1&4.2). From equations 4.4, $\Delta^{Ch}_{SiGe/IL}$ and Δ^{Ch}_{IL} are obviously related to EOT and IL thickness. As ΔWF_{eff} observed shifts are slightly reduced for an EOT three times larger (VT3 versus VT2 and VTFD2 versus VTFD1 in figure 4.23.b), charges at the IL dielectric cannot be suspected to explain such shifts.

In conclusion, the linear dependence of ΔWF_{eff} with Ge content suggests a Ge diffusion effect on gate stack effective work function. As the levels are similar for an EOT three times larger, charges at the IL oxide cannot be suspected. But only charges in the HK or dipoles at interfaces (figure 4.28) can be invoked to explain the additional ΔWF_{eff} shifts.

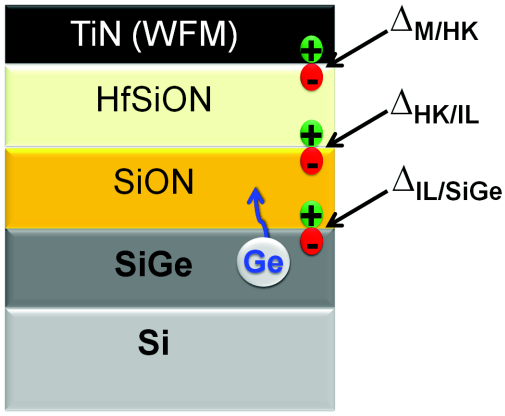


Figure 4.28: Schematic $SiGe$ pMOSFET showing dipoles at gate stack interfaces.

4.8.2 Physicochemical analysis of dipoles and charges at oxide/gate stack

In section 4.7, we have shown that the ΔWF_{eff} (figure 4.23.b) is composed of three parts of metal gate work function shifts caused by: interface states (ΔWF^{IT}_{eff}), oxide charges ($\Delta WF^{Oxide.Ch}_{eff}$) and dipoles at the oxide/gate stack ($\Delta WF^{Dipoles}_{eff}$).
The previous section has demonstrated that only interface states and charges in IL dielectric can not explain the totality of the ΔWF_{eff} induced by Ge. At most, only a quarter of ΔWF_{eff} shift should be related to the presence of interface states. Thus, according to equation 4.2, the ΔWF_{eff} shift is essentially caused by the presence of dipoles in the oxide/gate stack interfaces ($SiGe$/IL or IL/HfSiON or HfSiON/TiN) due to the Ge diffusion or charges in the HK oxide. In this subsection, physicochemical characterisations are analysed in order to discriminate between

these three interfaces (figure 4.28). Electron microscopy imaging and physicochemical characterisation methods will be briefly introduced. Physicochemical analysis of the $Si_{0.69}Ge_{0.31}$ VT1 and VT3 bulk pMOSFETs (T_{SiGe}=12nm) will be investigated to study the Ge diffusion in the oxide/gate stack. Finally, we will suggest an explanation of the ΔWF_{eff} shift induced by Ge.

4.8.2.1 Transmission Electron Microscopy (TEM)

In order to study the Ge diffusion in the oxide/gate stack, electron microscopy imaging and physicochemical characterisations were performed on two $SiGe$ pMOSFETs samples: the $Si_{0.69}Ge_{0.31}$ VT1 and VT3 bulk pMOSFETs (with T_{SiGe}=12nm and different IL thicknesses). For both samples, $330\times330\mu m^2$ square area was analysed.
To give good possibilities to interpret the physicochemical measurements and to identify the surface constituents, working with known samples is needed. First informations on the different layers and thicknesses of the analysed samples were given using Transmission Electron Microscopy (TEM) imaging. Before presenting the obtained results, we firstly briefly describe this electron microscopy imaging technique.
The TEM operates at high vacuum and high voltage conditions. Figure 4.29 shows a basic TEM scheme. Electrons are extracted from the tip of the gun and accelerated. Then, they are focused

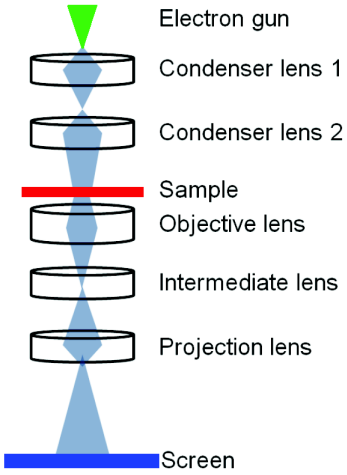


Figure 4.29: Basic scheme of the Transmission Electron Microscopy.

by electromagnetic lenses. First, the electron beam encounters the condenser lens system. This lens system is used to control the illumination of the sample (intensity and intensity spread). In the conventional TEM, the beam impinges on the top sample surface as a nearly planar wave. Interacting with the sample, the electrons are either transmitted or scattered. As the electrons emerge from the bottom sample surface they are focused again by the objective lens to form an image. This image is transmitted by the intermediate and projection lenses onto a fluorescent viewing screen or CCD camera [149].
Figure 4.29 depicts the obtained TEM pictures of the $Si_{0.69}Ge_{0.31}$ VT1 and VT3 bulk pMOSFETs. From these pictures, we distinguish the different layers in the direction perpendicular to the oxide/gate interface. Thicker SiON thichkness is noticed for the VT3 pMOS (right picture).

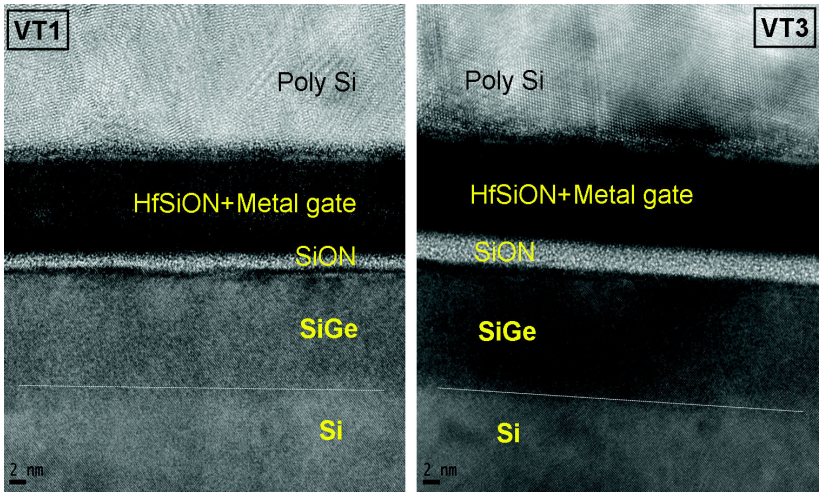


Figure 4.30: TEM pictures of the $Si_{0.69}Ge_{0.31}$ VT1 (left picture) and VT3 (right picture) bulk pMOSFETs.

4.8.2.2 HAADF-Scanning Transmission Electron Microscopy (STEM)

Once different layers of work samples were known, an atomic scale understanding of layers composition may be achieved. In the rest of this chapter, we want to qualitatively analyse the elemental distributions of structures presented in figure 4.30. To this end, we combine the scanning transmission electron microscopy, including high-angle annular dark-field, with electrons energy loss and secondary ion mass spectroscopies.
In this paragraph, we firstly describe the scanning transmission electron microscopy (STEM) technique. Then, we analyse the measured atomic resolution images of the $Si_{0.69}Ge_{0.31}$ VT1 and VT3 bulk pMOSFETs.
The STEM is another TEM mode in which a fine electron probe is formed and converged on the sample into a small point. The probe scans the sample in order to generate the image. As the scattered intensity at this point is recorded, each pixel of the STEM image is generated. Typically, STEM electron microscopy may include high-angle annular dark-field (HAADF) imaging. The atomic-resolution HAADF-STEM image is formed by scanning the small focused electron beam (1-2 $\AA$ in diameter) and collecting the electrons that are scattered to large angles (> 50 mrad) on an annular dark field (ADF) detector [149][137].
Atomic resolution HAADF images have several advantages over conventional TEM images. In particular, the contrast in HAADF-STEM images is highly sensitive to the atomic mass number (Z) of elements present in the area of interest. In fact, the scattering angle depends on the atomic number Z of the specimen material. For higher Z the scattering angle is larger (see figure 4.31). So, the intensity of the bright spots in the image can be related to the atomic composition of the corresponding column of atoms in the sample [150]. Thus, layers containing lighter atoms (such as interfacial SiO_2) can easily be distinguished from those containing heavier elements, such as Hf. For high-Z elements, the contrast in HAADF images is sensitive enough to detect very small quantities of Hf in amorphous SiO_2 [151][152].
Figure 4.32 shows the obtained cross-section HAADF-STEM images of the $Si_{0.69}Ge_{0.31}$ VT1 and VT3 bulk pMOSFETs. The atomic resolution HAADF images presents similar atomic

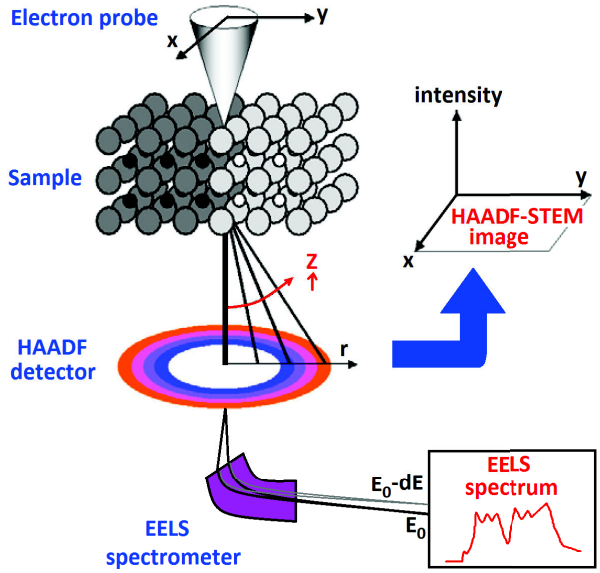


Figure 4.31: Image formation of HAADF-STEM contrast method. The scattering angle depends on the atomic number Z of the specimen material. For higher Z the scattering angle is larger.

number contrast for thin (left figure) and thick (right figure) IL pMOSFETs. Due to the strong atomic number contrast, the $HfSiON$ dielectric appears bright, while the interfacial $SiON$ layer is dark. As can be seen in this figure, abruptness of oxide/gate stack interfaces is noticeable, excepted the $Si/SiGe$ bottom interface. The HAADF-STEM pictures illustrate a gradual profile of Ge at $Si/SiGe$ bottom interface.
The impact of such gradual Ge profile on the C-V characteristic is investigated in subsection 2.4.3 (see page 71). We have shown that changing the Ge profile at the $SiGe/Si$ heterojunction slightly affects the C-V curve. This observation has validated the approximation of considering an abrupt $SiGe/Si$ junction in C-V simulations.

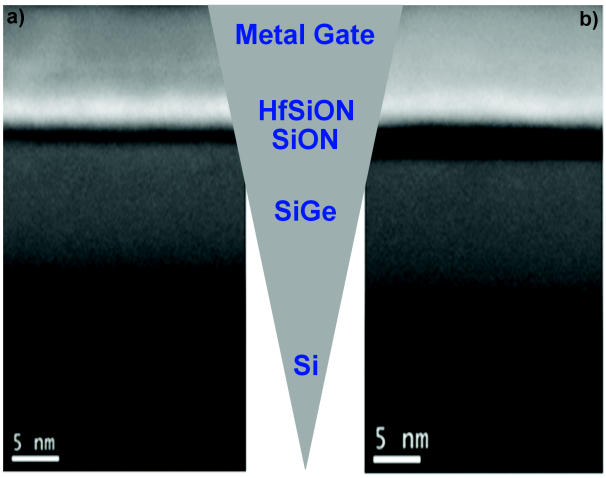


Figure 4.32: Cross-section HAADF-STEM images of the $Si/SiGe/SiON/HfSiON$/gate stack of the $Si_{0.69}Ge_{0.31}$ VT1 and VT3 bulk pMOSFETs: a) VT1, b) VT3.

4.8.2.3 Energy Loss Electrons Spectroscopy (EELS)

Electrons energy loss and secondary ion mass spectroscopies were performed in order to identify the elements present in the oxide/gate stack of $Si_{0.69}Ge_{0.31}$ VT1 and VT3 bulk pMOSFETs and assess their concentrations and spatial distribution.
In this subsection, we start by describing the energy loss electrons spectroscopy (EELS) technique. Then, Ge diffusion across interfaces will be investigated by EELS analysis of structures presented in figure 4.29.
In STEM, the beam of fast electrons interacts with the sample atoms and results different physical signals (see figure 4.33). Generally, not all of the signals are used. In STEM, the typi-

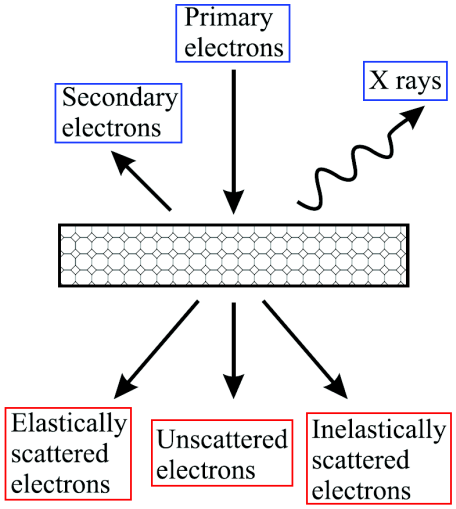
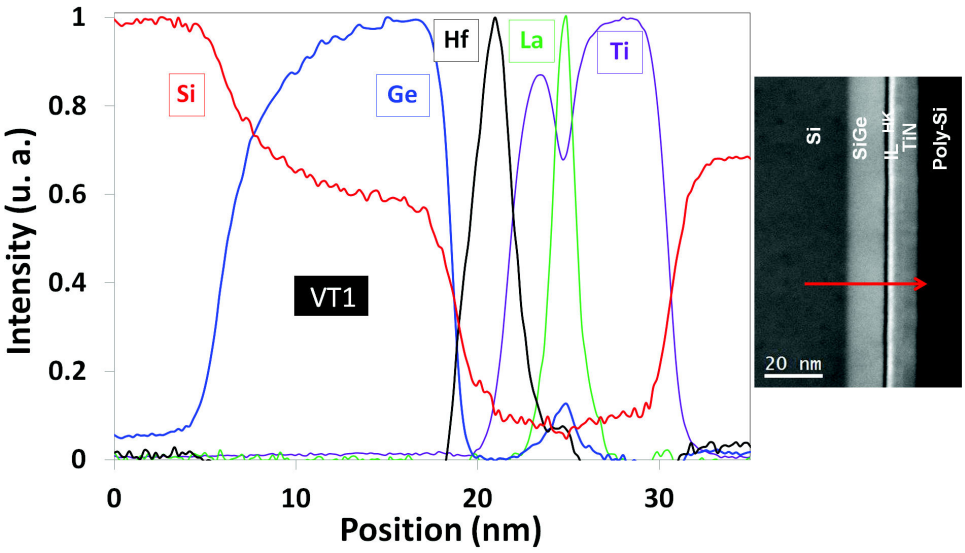
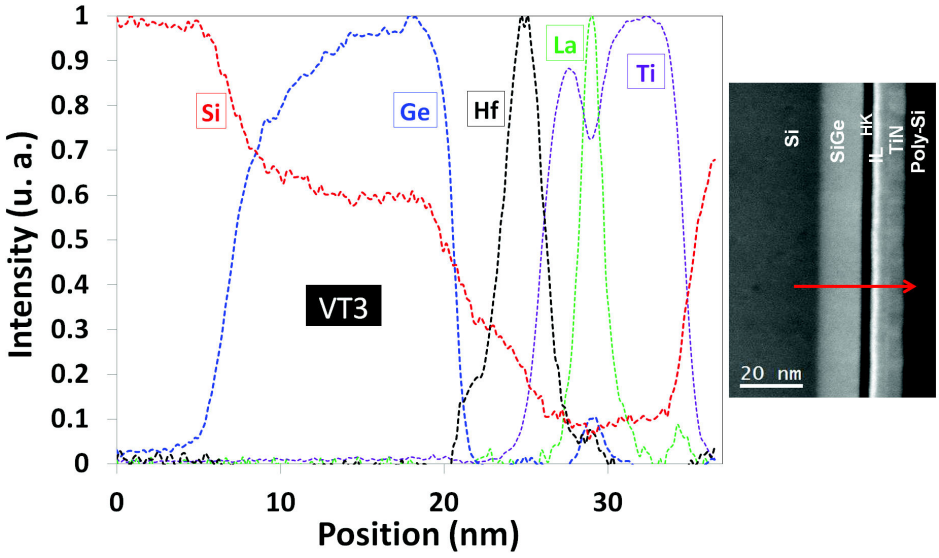


Figure 4.33: Schematic of possible interactions of the primary electron beam with a thin sample.

cal signal which is recorded is energy loss electrons (EELS). In fact, the inelastically scattered electrons that pass through the hole in the annular detector (HAADF) may be analysed via EELS spectometer (see figure 4.31). Electrons undergoing inelastic scattering are concentrated in a much narrower angular distribution compared to the elastically scattered electrons. With increasing electron energy loss the deflection angle increases.
The EELS is still sensitive to light elements and it can easily detect many of the transition and rare earth metals that may be used in novel gate dielectrics or electrodes. The sensitivity of EELS for light elements is typically around 1-2 atom% [153].
Figure 4.34 illustrates EELS characterizations of the VT1 and VT3 $Si_{0.7}Ge_{0.3}$ bulk pMOSFETs. EELS chemical profiles recorded across a $Si/SiGe/SiON/HfSiON/$gate stack with a poly-Si cap. The Si substrate is to the left and the Ge content is plotted with blue lines. Interfaces may be located around the half of the profile intensity of each element. 12nm of $SiGe$ is obtained by EELS, which is close to the value measured by ellipsometry.
From figures 4.34.a&b, firstly, we notice an abrupt Ge profile at the $SiGe$/IL interface. The difference is obvious compared to the $Si/SiGe$ bottom interface profil. More Ge diffusion is observed in the Si substrate than in the IL dielectric. This observation is consistent with the obtained atomic number contrast in figure 4.32. Besides, it seems that the Ge updiffusion does not reach the IL/HK interface, especially for the thick IL (figure 4.34.b).
Secondly, we remark an unintentional Ge peak localised in the TiN gate stack for both VT1 and



(a)



(b)

Figure 4.34: EELS analysis on the gate stack in directions shown in the TEM pictures (figure 4.29). (a) EELS characterizations performed on the VT1 $Si_{0.7}Ge_{0.3}$ bulk pMOSFET. (b) EELS characterizations performed on the VT3 $Si_{0.7}Ge_{0.3}$ bulk pMOSFET.

VT3 pMOSFETs. 10% Ge updiffusion at the TiN metal gate is shown in figure 4.34. Similar Ge peak was observed by J. Huang et al. [8]. He concluded that Ge in $SiGe$ plays a critical role in metal/$HfSiON$/$SiGe$ stacks by causing the Ge-enhanced Si oxidation and Ge updiffusion. This observation will be discussed in the following.

4.8.2.4 Secondary Ion Mass Spectrometry (SIMS)

In order to check precisely the presence of Ge in the oxide/gate stack interfaces, we need a more surface sensitive technique than EELS, which may give information from only the top one or two monolayers of the material. That's why, we had performed Secondary Ion Mass Spectrometry (SIMS) measurements, using an ION-TOF TOF-SIMS IV Time-of-flight (TOF) system, on the VT1 and VT3 bulk pMOSFETs. For SIMS analysis, both the $Si_{0.8}Ge_{0.2}$ and $Si_{0.7}Ge_{0.3}$ samples were analysed. Actually, TOF-SIMS presents a very high surface specific sensitivity. It may be applied on practically all type of materials. So, it can detect all elements in a very thin surface of sample.
This subsection is composed of two parts. Firstly, we briefly describe the Secondary Ion Mass Spectrometry technique. Secondly, we analyse the TOF-SIMS profiles obtained for the VT1 and VT3 bulk pMOSFETs ($Si_{0.8}Ge_{0.2}$ and $Si_{0.7}Ge_{0.3}$).
Figure 4.35 illustrates a schematic of the SIMS process. In SIMS, the primary beam removes

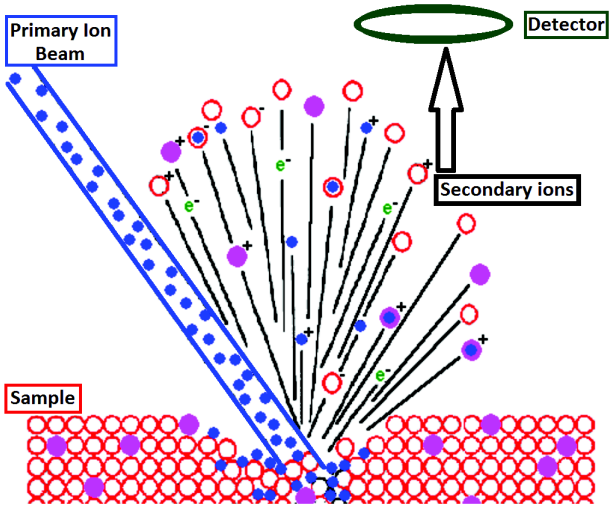


Figure 4.35: Schematic of Secondary Ion Mass Spectroscopy.

material by sputtering while a mass spectrometer analyses and identifies sputtered ions (called secondary ions). During SIMS analysis, the sample surface is slowly sputtered away. Continuous analysis while sputtering produces information as a function of depth, called a depth profile. To achieve a depth profile, the secondary ion intensity is monitored as a function of time, as the sample is sputtered by the primary beam. At the end of the measurement, the depth of the sputtered crater can be measured to convert the time scale to a depth scale, thus giving a secondary ion intensity versus depth profile [154]. The SIMS technique boasts excellent elemental sensitivity (as low as 10^{14} cm^{-3}) and a depth resolution on the order of few nanometers. This very high surface sensitivity is due to the low sputtering rates. In fact, the emitted particles originate from the 1-2 top-most monolayers (1nm) [39][155].
Before analysing the measured SIMS profiles, we want to mention that the SIMS characterization has a higher intensity resolution than EELS, whereas, EELS has the advantage of a high spatial resolution technique. As a result, depth scale of SIMS (x axis) analysis should be attentively treated and intensity scale of EELS (y axis) characterisations should be carefully analysed. Another difficulty with SIMS is its secondary ions production ratio. For each minor

element in a matrix, it depends on the matrix itself and this element. Therefore, the relative comparison of different elements intensities at a certain depth can not directly achieved. Finally, during primary ion beam sputtering process, secondary ions can be reinjected in the bulk of the sample.
Figure 4.36 depicts the TOF-SIMS depth profile analysis of the Ti, Al, Hf, Ge and Si substances for the VT1 $Si_{0.7}Ge_{0.3}$ pMOS. During SIMS analysis, the primary beam removes the surface material from the TiN gate to the Si substrate. So, if Ge exists in the oxide/gate stack, it will be straightforward detected by TOF-SIMS.

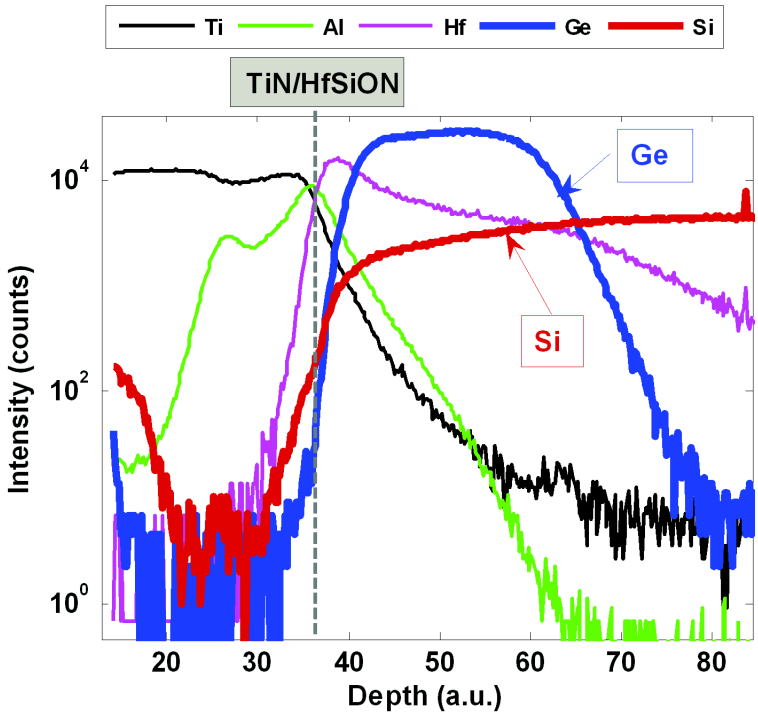


Figure 4.36: SIMS profiles with metal gate/high-K interface location and Ge profile (30% Ge, VT1). Depth in a.u. is proportional to abrasion time.

In figure 4.36, the relative position of Al additive, Ti and Hf enables an identification of the metal/$HfSiON$ interface. Let's remember that EELS measurements have shown a 10% Ge updiffusion at the TiN metal gate. Nevertheless, this result is not consistent with the TOF-SIMS characterised on the same samples (figure 4.36). No Ge in the TiN gate was detected by TOF-SIMS. This makes the observed Ge peak at the TiN gate by EELS (figure 4.34) not reliable. Moreover, Ge diffusion at TiN gate identifying by EELS was already suspect, because no Ge was seen between TiN gate and $SiGe$ layer in the dielectric (figure 4.34). The EELS Ge signal in TiN could also be related to La in TiN gate.

We have also compared for two xGe (20 and 30%) the relative position of Ge for VT1 and VT3 (figure 4.37). SIMS elements profile, reported in figure 4.37, shows that the presence of Ge at metal interface can be neglected, which proves that the observed Ge at TiN by EELS (figure 4.34) is a measurement artefact. For both xGe (20 and 30%) in figure 4.37, we notice parallel Ge profiles between VT1 and VT3 pMOSFETs. The shift along x axis is consistent with the IL thickness difference around 2nm. This result suggets a same abrupt diffusion profile

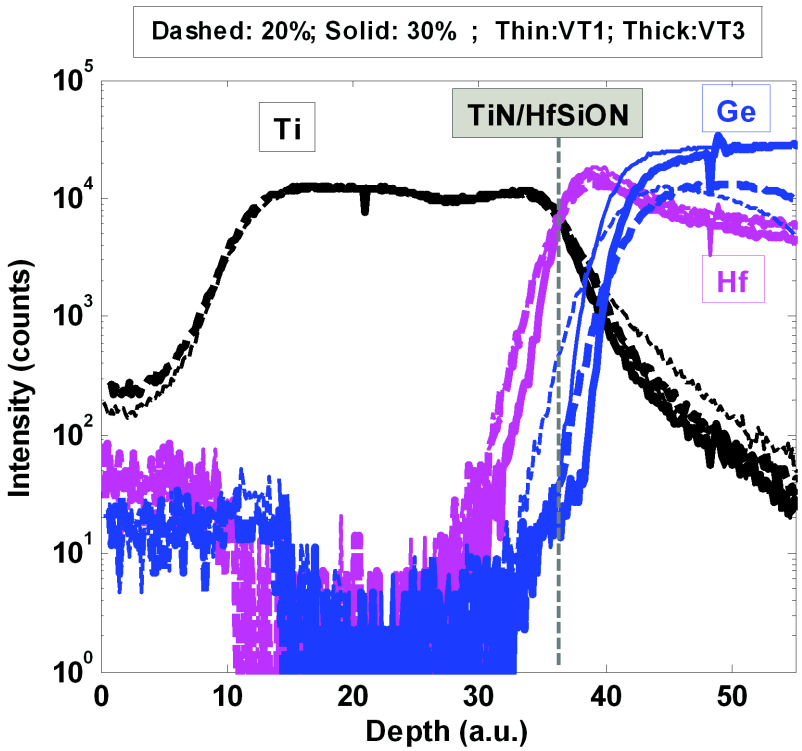


Figure 4.37: Comparison of SIMS profiles aligned on metal gate/high-K interface: Thin lines: VT1, Thick lines: VT3; Dashed: 20%, Solid: 30%.

of Ge in both IL, confirming the obtained HAADF-STEM and EELS analysis (figure 4.32). It is also clear from figure 4.37 that the Ge concentration at IL/$HfSiON$ interface is low, especially for VT3 compared to VT1 and VT2 pMOS. 10 times less Ge concentration at the IL/$HfSiON$ interface is noticed for the thicker EOT. Therefore, SIMS, EELS and STEM analysis imply that Ge diffusion in IL is very small. No significant level of Ge can be found in HK, HK/IL interface and even a significant part of IL for the 3nm thick IL.
The analysis of electrical results conduced to an impact of Ge in HK or a dipole at one of the various interfaces (figure 4.28). After these physical characterizations, the remaining solution is a dipole at the interface $SiGe$/IL. This conclusion is a novelty in the field of gate stack engineering, but we think that our experimental analysis coupled with simulations imply for it.

4.8.3 ΔWF_{eff} shift in the literature

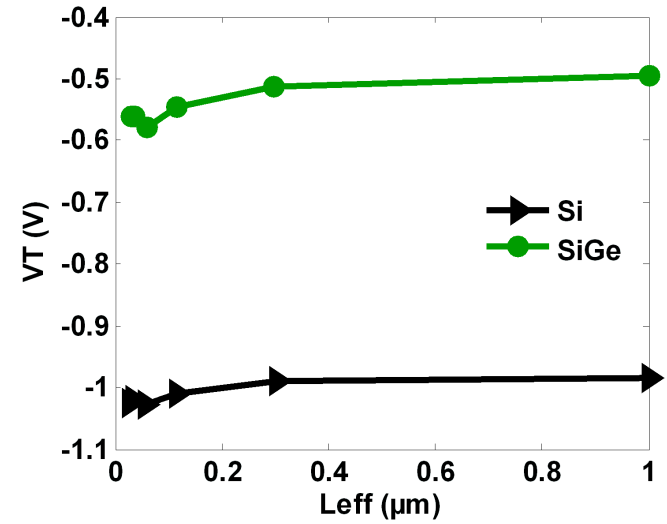
In the literature, deviations of the effective metal gate work function in Silicon MOS devices from the expected behaviour have been investigated. In addition to interface states and oxide charges effects, the effective work function change is suggested to stem from various contributions not related to the pure metal gate (defined and illustrated in [156]). These discrepancies were first described in terms of Fermi-level pinning [157][158][159]. Moreover, a threshold voltage roll-off effect for small EOT [160] was observed. Explanations to the effective work function shift were suggested to be ranged from: intrinsic metal-induced interface gap states at the metal/dielectric interface [161][162][163], defects in the dielectric such as Oxygen vacancies [164][165], Oxygen

vacancies transfer [166][167][168][169][170][171] and changes in the dipoles of the dielectric stack [14][172][20][173][174][175][176][177][178].

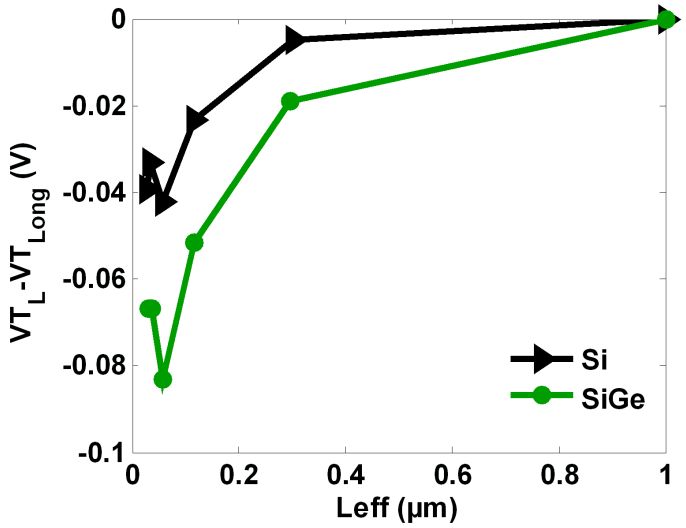
It is important to mention that all these studies were performed on Silicon based devices. Concerning, our study with $SiGe$ substrate, the above mentioned phenomena are expected but we must also account of a specific effect related to Germanium. Our electrical and physical analysis have led us to conclude to a dipole effect, similarly to the most accepted explanation for effective work function shift in high-k metal gate stack [14][172][20][173][174][175][176][177][178]. But, its originality consists in the role of Germanium and its location. Concerning the classical effective work function shift mentioned in literature and related to high-k metal gate stack, its part has been eliminated in our study by comparing all our results to the pure Si devices. Thus the ΔWF_{eff} (figure 4.23.b) observed when increasing the Ge concentration is independent of these effects. We would like also to discuss the role of Oxygen vacancies on the effective work function shift as it has been mentioned in some studies [169][171]. We must notice that similar ΔWF_{eff} has been obtained for both bulk and FDSOI technologies and with two different IL thicknesses. It means despite of differences in the HK (HfO_2 for FDSOI instead of $HfSiON$ for bulk pMOS) and IL.
In fact, C. H. Choi [179] has studied the electrical stability of CVD HfO_xN_y gate oxide. Compared with HfO_2 dielectric, the presence of in-situ-incorporated Nitrogen in the HfO_xN_y blocked Oxygen diffusion through HfO_xN_y during high-temperature annealing. CVD HfO_xN_y allowed not only significantly reduction in leakage current and boron penetration but also superior thermal and electrical stability. Besides, M. R. Visokay [180] has shown that the presence of Nitrogen in the $HfSiON$ film significantly improves the thermal stability relative to $HfSiO$. Such results prove the electrical and thermal stability of the $HfSiON$ dielectric in bulk pMOSFETs if compared to HfO_2. The incorporated Nitrogen in both HK and IL oxides of the bulk pMOSFETs should reduce significantly Oxygen diffusion through the dielectric, as well as Oxygen vacancy creation. Oxygen vacancies creation were also supposed to appear more specifically for thin IL [169]. The similar behaviour of ΔWF_{eff} shift with xGe for both bulk and FDSOI technologies (figure 4.23.b) but also with thick and thin IL lead us to think that the origin for this Ge related dipole is not related to Oxygen vacancy creation near this interface.

4.9 Impact of gate length reduction

In order to investigate the Ge integration impact on the VT of short channel pMOS, split C-V measurements were performed on VT1 Si and $Si_{0.7}Ge_{0.3}$ pMOSFETs with various channel lengths (Leff). Figure 4.38.a shows the extracted VT at 40% of the measured $C^{max,inv}$. Very slight VT decrease is noticed when reducing the channel length of the pMOS. 23mV and 50mV only is observed for the Si and $Si_{0.7}Ge_{0.3}$ pMOS respectively with 0.12μm channel length (figure 4.38.b). The integration of 30% Ge in the pMOS channel drops the |VT| up to 500mV. This VT shift seems insensitive to the pMOS channel length, indicating that VT engineering is still efficient at nominal gate length.



(a)



(b)

Figure 4.38: (a) Extracted VT at 40% of the measured $C^{max,inv}$ as a function of the channel length in the VT1 Si and $Si_{0.7}Ge_{0.3}$ bulk pMOSFET. (b) Channel length decrease impact on the measured VT in the VT1 Si and $Si_{0.7}Ge_{0.3}$ bulk pMOSFET.

4.10 Conclusion

In this chapter, we have evaluated the role of Germanium on pMOS gate stack parameters: the effective work function (WF_{eff}) and equivalent oxide thickness (EOT). The variation of the extracted EOT with Ge concentration is investigated for VT_i split bulk pMOSFET. Up to 1.2$\mathring{A}$ EOT increase is observed for 30% Ge for thinner IL. This can be explained by an increase of interfacial oxide in presence of Ge by thermal oxidation. Whereas, EOT is independent of Ge content for thick deposited interlayer.

In another hand, increasing Ge content shifts linearly (VT-VFB) in full agreement with PS simulation results accounting for adequate bands discontinuity and strain. The *Ge* impact was mainly studied from the measurement analysis of the threshold voltage (VT) and the flat band voltage (VFB) of *SiGe* pMOSFETs of the C28 Bulk technology. A comparison between experiments and simulations with various *SiGe* thicknesses and *Ge* contents demonstrated that to predict the pMOS threshold voltage, in addition to classical *SiGe* band structure effect, we must account for an additional effective metal gate work function ($\Delta\mathrm{WF}_{eff}$) increase proportional to *Ge* concentration, typically 6mV/%. The same analysis has been done on *SiGe* 14nm FDSOI pFETs. Similar *Ge* electric effect is noticed on this technology.
Characterizations of interface traps show that their density is too low (at most 1mV/%) to explain such observed $\Delta\mathrm{WF}_{eff}$. Moreover, the linear dependence with xGe suggests a *Ge* diffusion effect on effective work function of the gate stack. Comparison between pMOS transistors with two different oxide interlayer thicknesses (EOT is around 1.1 and 3.1nm) implies that this effect can not be attributed to charges in the IL. Eelectrical analysis have shown that $\Delta\mathrm{WF}_{eff}$ shift is due either to charges in the HK or dipole at one gate stack interface (SiGe/IL or IL/HfSiON or HfSiON/TiN).
In order, to investigate the origin of $\Delta\mathrm{WF}_{eff}$ increase, various physical characterizations have been performed. EELS in combination with SIMS as well HAADF-STEM analysis demonstrates that *Ge* diffusion is very low in the IL oxide. This result proves the absence of charges in the HK and demonstrates that dipole's modulation due to *Ge* presence probably occurs at *SiGe*/IL interface.

General conclusion

Contents

Thesis summary

In novel CMOS technology, maintaining good threshold voltage centering is a paramount challenge. The introduction of $SiGe$ in bulk pMOSFET and FDSOI pFET requires the VT control for such devices. To this end, we have to extract accurately electrical parameters (VT, VFB and EOT) and to understand the Ge integration effects in $SiGe$ based pFETs.
The purpose of this thesis was, first, to propose methods to determine electrical parameters when $SiGe$ is introduced in the pMOS. The second objective is to understand the electric impact of Ge in $Si_{1-x}Ge_x$ based pMOS for better VT contol.

In more detail, in the first part of chapter 1, we have reminded basic principles of ideal and real MOS capacitors. The real MOS devices may present oxide defects and dipoles at oxide/gate stack interfaces. The oxide defects and interface traps impact on the C-V characteristic has been addressed, evaluating the flat band voltage expression.
In the second part of chapter 1, we have validated the results of UTOXPP Poisson-Schrödinger simulator, by comparison to PSL (PS.Leti) solver and literature results. Furthermore, UTOXPP C-V simulation model has been compared to measurements for Si nMOSFETs with Polysilicon and metal gate, emphasizing the efficiency of the C-V simulation model.

In chapter 2, we began by describing the strained $SiGe/Si$ band structure. We have reported basic equations to model the strained $SiGe$ valence band using the deformation potential approximation (within the effective mass approximation model) and the 6-band k.p model. The strained $SiGe/Si$ bands structure computed using the deformation potential approximation (CEMA model) has been ascertained through comparison with the 6-k.p result. By comparing the $SiGe$ energy band gap and strained $SiGe$ bands offset obtained using UTOXPP solver to published experimental and theoretical results, we have proved that the strain is well taken into account in UTOXPP band structure models.
Afterwards, we were interested to the $SiGe/Si$ heterostructure modeling. We have compared three solutions based on the effective mass approximation to the accurate 6-level k.p model with an in-plane numerical integration (exact formula). We have shown that C-V, simulated

within the "exact formula", is efficiently reproduced using the CEMA when the $M_{DOS}(HH, Si)$ increases from $0.51m_0$ to $2.5m_0$ and $1.5m_0$ respectively for Si and $SiGe$.
In section 2.4, we have investigated the impact of five $SiGe$ simulation parameters on the C-V characteristic: (a) ΔE_c and ΔE_v bands offset, (b) Ge profile effects, (c) $SiGe$ strain, (d) $SiGe$ dopant concentration and (e) Ge concentration and $SiGe$ thickness.
From this study, we have shown that the modification of ΔE_c and ΔE_v bands offset induces a straightforward change respectively in the accumulation and inversion capacitance. Moreover, we have proved that considering an abrupt $SiGe/Si$ junction is a valid approximation to efficiently simulate the C-V characteristic of the $SiGe/Si$ pFETs. The strain affects especially the $SiGe/Si$ conduction band offset. Whereas, the valence band offset seems insensitive to the strain. Thus, the C-V is affected by the strain only in the accumulation regime. The Ge concentration variation for different strained $SiGe$ layer thicknesses shows a linear VT variation of the $SiGe$ pMOSFET. As the $Si_{1-x}Ge_x$ layer thickness increases, the VT saturates to a level corresponding with the valence band offset.

In chapter 3, we have dicussed the applicability of the VT extration method, using "split C-V" [120], to extract VT and VFB parameters in $Si_{1-x}Ge_x/Si$ bulk pMOSFETs. Firstly, we have validated this "split C-V" method via PS simulations, emphasizing its simplicity and efficiency. Then, it has been successfully applied to Si and $Si_{0.7}Ge_{0.3}/Si$ pMOS measurements, enabling the investigation of the Ge incorporation impact in bulk pMOSFETs.
Chapter 3 has suggested also a new EOT extraction method based on the inversion capacitance versus inversion charge curve. First, the $C_{inv}(Q_{inv})$ curve has been found not sensitive to the Ge integration, but depending on the doping concentration. Second, the new EOT extraction method has been generalized for FDSOI devices, where the body is undoped. The second part of chapter 3 has verified the universal behaviour of the $C_{inv}(Q_{inv})$ of the FDSOI nFETs using UTOXPP simulations. For different body thicknesses, the variation of the $C_{inv}(Q_{inv})$ is very close for various T_{Si} whereas a discrepancy is noticed for the $In_{0.53}Ga_{0.47}As$ FDSOI response. The measured C-V of the Si FDSOI nFET has been coupled to the simulated $C_{inv}(Q_{inv})$ to extract the EOT. Afterwards, we have similarly checked the universal behaviour of the $C_{inv}(Q_{inv})$ of the Si and $Si_{1-x}Ge_x$ FDSOI pFETs. The EOT extraction method has been validated using UTOXPP simulations for various body thicknesses. Finally, we have successfully applied it to Si and $Si_{0.7}Ge_{0.3}$ measurements, proving the robustness of the extraction method.

In chapter 4, we have studied the electric effect of Ge on pMOS gate stack parameters: VT, VFB, equivalent oxide thickness (EOT) and effective work function (WF_{eff}).
For thick interlayer performed by oxide deposition, EOT is independent of Ge content. However, it linearly increases for the two pMOSFETs with thin interlayer, obtained by thermal oxidation. This can be explained by fast growth of interfacial oxide in presence of Ge during the thermal oxidation.
In addition, we have shown that (VT-VFB) should depend mainly on ΔE_v. Including the BGN in all simulations, we have found a global agreement between the simulated and measured (VT-VFB), confrming the validity of the simulated ΔE_v.
Concerning the Ge impact on the effective work function, we have compared simulated and measured C-V of the $SiGe$ bulk pMOSFETs and FDSOI pFETs, with various $SiGe$ thicknesses and Ge contents. We have demonstrated that to predict the measured C-V, in addition to classical $SiGe$ band structure effect, we must account for an additional effective metal gate

work function (ΔWF_{eff}) increase proportional to Ge concentrations. The linear dependence with xGe suggests a Ge diffusion effect on effective work function of the gate stack. A detailed comprehension of the origin of such ΔWF_{eff} induced by Ge has been presented in section 4.8 of chapter 4.
According to the work function shift expression, the ΔWF_{eff} can be attributed to the presence of: interface traps or oxide charges or dipoles at one of the oxide gate stack interfaces. Firstly, density of interface states measurements on $SiGe$ bulk and FDSOI have proved that ΔWF_{eff} shift may not be explained by the presence of interface traps. Secondly, ΔWF_{eff} comparison between pMOS transistors with two different oxide interlayer thicknesses (EOT is around 1.1 and 3.1nm) implies that this effect may not be attributed to charges in the IL dielectric. Therefore, the analysis of electrical results reveals a Ge effect in the HK or a dipole like effect probably at one gate stack interface (SiGe/IL or IL/HfSiON or HfSiON/TiN). Thirdly, EELS in combination with SIMS and STEM analysis have demonstrated no significant level of Ge in HK and HK/IL interface. Besides, Ge diffusion is very low in the IL oxide. Such result implies that charges in the HK may not explain the ΔWF_{eff} induced by Ge. Finally, we have concluded that dipole's modulation due to Ge presence probably occurs at $SiGe$/IL interface. This effective work function engineering is still efficient at nominal gate length.

Future work and recommendation

Some suggested future works are as follows:
• The simulated C-V of the $In_{0.53}Ga_{0.47}As$ FDSOI nFET could be validated by comparison with measurements. Thus, the EOT extraction method proposed in chapter 3 may be applied to the measured C-V of the $InGaAs$ FSDSOI.
• X-Ray photoelectron spectrometry (XPS) analysis can be done to investigate chemical changes at the oxide/gate stack interfaces of $SiGe$ based pFET. It would also be interesting to compare the obtained $SiGe$ result by XPS with the pure Si one. In addition, the HK and IL electronic properties such as bandgap and electron affinity may be investigated combining ultraviolet photoelectron spectroscopy (UPS) and spectroscopic ellipsometry (SE), as studied in [181].
• During this thesis, ab-initio calculations were performed, courtesy of CEA-Leti P. Blaise, to analyse the electrostatic mechanism relevant for the IL/HK and $SiGe$/IL interfaces. DFT calculation including G0W0 corrections [175] have been performed on two interfaces: monoclinic $HfO_2(001)/\beta$-cristobalite $SiO_2(101)$ and $(100)Si/\beta$-cristobalite $SiO_2(101)$ interfaces. The, valence band offset (VBO) at material interface was calculated from Electrostatic Potential. The impact of Ge doping on the VBO was studied through the substitution of Si or Hf atoms at both interfaces. The obtained results do not lead a clear conclusion. That's why, they have not been reported in this document. Nevertheless, we recommend to continue ab-initio calculations for both IL/HK and $SiGe$/IL interfaces. More realistic configuration may be simulated e.g. including a Ge concentration in the substrate rather considering pure Si.

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Summary

Maintaining good threshold voltage (VT) centering is a paramount challenge for CMOS technology. The SiGe introduction in bulk and FDSOI pFETs requires VT control for such devices. To this end, we have to extract accurately electrical parameters and to understand Ge integration effects in SiGe based pFETs. In this thesis, first, we have proposed extraction methods to determine VT, flat band voltage (VFB) and equivalent oxide thickness (EOT) parameters in bulk and FDSOI transistors. The extraction methods have been validated via Poisson-Schrodinger (PS) simulations and successfully applied to measurements. Second, we have highlighted and explained electric effects of Ge on pMOS gate stack parameters. Electrical characterizations compared with PS simulations have evidenced an additional effective work function increase, induced by Ge, related to interfacial dipoles. STEM, EELS and SIMS characterizations have demonstrated that dipoles are located at SiGe/IL interface.

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Résumé

.1 Introduction et contexte

La miniaturisation du transistor MOS conventionnel sur silicium massif (bulk) a rencontré des limites importantes dans la dernière décennie, principalement liées aux courants de fuite de l'oxyde de grille (SiO_2), à la forte augmentation des effets parasites de canal court et à la réduction drastique de la mobilité dans les canaux de silicium fortement dopés utilisés précisément pour réduire ces effets de canal court. Des solutions technologiques pour remplacer l'architecture MOSFET bulk ont été proposées et largement étudiées dans la littérature récente. Parmi ces solutions, les diélectriques de grille à haute permittivité (high-k) sont largement utilisés actuellement pour remplacer efficacement le dioxyde de silicium SiO_2 dans l'empilement de grille. Ces diélectriques high-k, combinés avec l'utilisation des grilles métalliques, l'introduction de nouveaux matériaux de canal comme le SiGe et, éventuellement, de nouvelles structures telles que les dispositifs SOI complètement déplétés (FDSOI), permettent au transistor MOS ainsi amélioré d'atteindre les performances électriques requises pour les noeuds sub-22 nm.

Particulièrement, le SiGe a été introduit avec succès dans le canal des pMOS bulk et FD-SOI, entre autres, afin d'ajuster la tension de seuil. L'ajustement de la tension de seuil se fait en diminuant le gap de la bande interdite du canal de coté de la bande de valence. Cependant, l'intégration du SiGe dans les transistors MOS à canal p pose un certain nombre de problèmes, tels que l'inadaptation des modèles de simulation utilisés habituellement pour les canaux silicium pour extraire les paramètres électriques : tension de seuil (VT), tension de bandes plates (VFB) et épaisseur équivalente de l'oxyde (EOT). Avant cette thèse, le VT et VFB ne pouvaient être déterminer qu'en utilisant un outil d'extraction sur Si. La figure 39 compare le C-V du SiGe pMOSFET bulk mesuré et simulé en utilisant l'outil d'extraction sur Si du Leti [26]. On remarque que l'outil d'extraction est non pertinent pour des dispositifs intégrant du SiGe.
Un autre problème due à l'intégration du SiGe dans le calal des pMOS est de maintenir un bon contrôle du VT en introduisant du SiGe. La figure 40 illustre différentes tensions de seuil relevées de la littérature en fonction de la concentration de Ge (xGe). Une large dispersion de VT est observée relevant un défi du contrôle de VT pour des transistors bulk et FDSOI intégrant du SiGe.
Les objectifs de la thèse sont donc d'identifier les modèles de simulation pertinents pour les structures MOS Métal/high-k/SiGe, de proposer des méthodes d'extraction de paramètres adaptées à ces structures et de mieux comprendre l'impact du Ge sur ces paramètres afin d'optimiser le contrôle de la tension de seuil.

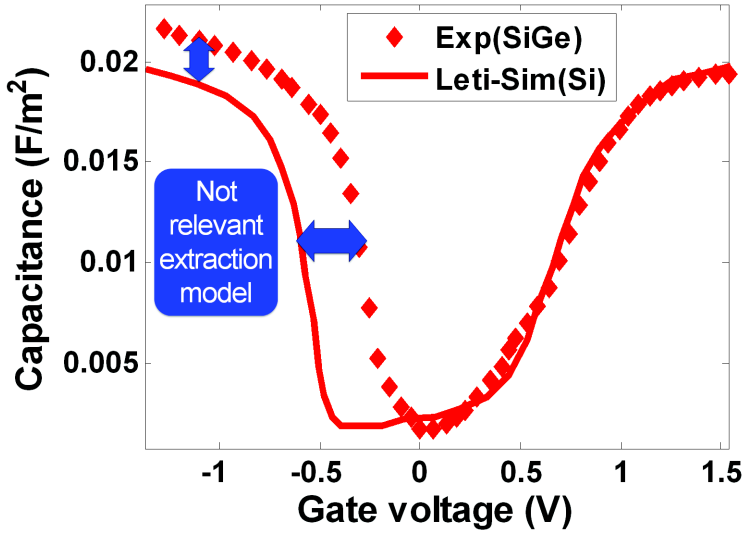


FIGURE 39 – Comparaison de la capacité en fonction de la tension de grille appliquée (C-V) mesurée (symbole) pour un *SiGe* pMOSFET bulk et simulée en utilisant l'outil d'extraction sur Si du Leti [26] (ligne).

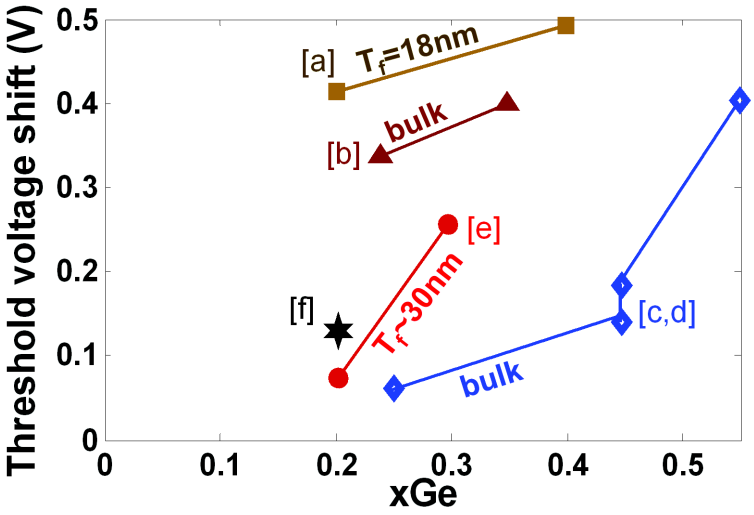


FIGURE 40 – Différents tensions de seuil relevés de la littérature en fonction de la concentration de Ge (xGe).(References : [a] : [27] ; [b] : [28] ; [c] : [29] ; [d] : [30] ; [e] : [31] ; [f] : [32].)

.2 Simulation des capacités MOS

Dans cette thèse, les simulations des caractéristiques C-V ont été effectuées à l'aide d'un solveur auto-consistant Poisson-Schrödinger (PS) nommé UTOXPP. Il s'agit d'une résolution auto-cohérente des équations de Poisson et de Schrödinger unidimensionnelles. Cette partie est dédiée à la validation des résultats de simulations PS.
D'abord, les résultats de simulation PS sont comparés à des résultats PS publiés dans la littérature. Ensuite, un modèle analytique basé sur une amélioration de l'approximation du

puits triangulaire est validé pour les structures SiO_2/Si bulk dans un n-MOSFET. Pour terminer, des résultats de simulations C-V sont validés avec des caractéristiques C-V expérimentales des transistors nMOSFET Si.

.2.1 Validation des résultats de simulation Poisson-Schrödinger

Les résultats du calcul self-consistant Poisson-Schrödinger de UTOXPP (PS.UTOXPP) ont été validés dans le cadre de l'approximation de la masse effective (EMA) avec les résultats issus du Poisson-Schrödinger de Synopsys (PS.Synopsys) et du Poisson-Schrödinger de Leti (PSL) (figure 41) pour un substrat de Silicium dopé p (N_{Dop}=10^{18}cm^{-3}) ainsi que des résultats existants dans la littérature [55][56] (figure 42 et figure 43) avec un dopage d'environ 5.10^{17}cm^{-3} en régime d'inversion. Malgré l'accord global observé entre les résultats comparés, il convient de

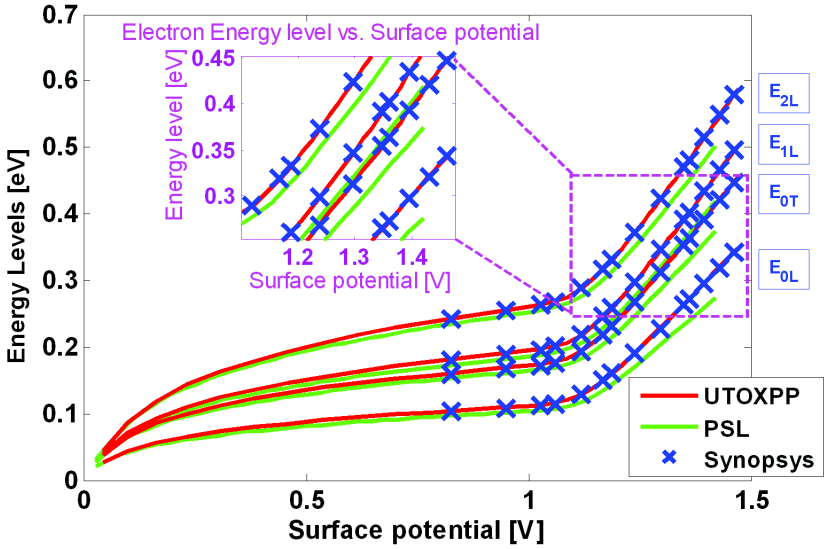


FIGURE 41 – Les quatre premiers niveaux d'énergie obtenus avec le PS.UTOXPP, PSL et PS.Synopsys pour différents potentiels de surface en régime d'inversion.

rester prudent sur la comparaison des résultats de simulateurs Poisson-Schrödinger (figure 41) puisque ceci dépend de plusieurs paramètres comme la taille de la boite quantique, le nombre des niveaux d'énergie pris en compte, la pénétration des fonctions d'onde etc...

.2.2 Analyse du modèle analytique et validation pour les structures SiO_2/Si Bulk dans un n-MOSFET

Dans un empilement métal - oxyde - semiconducteur (MOS), l'effet de champ exercé par la grille sur le substrat modifie la courbure de bandes à l'interface et l'énergie potentielle ne varie que dans une dimension perpendiculaire à l'interface oxyde/substrat. La modélisation de la quantification des porteurs à cette interface nécessite une simulation numérique Poisson-Schrödinger (PS). Des modèles analytiques [59] (comme l'approximation du puits triangulaire (TWA) et l'approche variationnelle) ont été proposés dans la littérature afin de calculer les niveaux d'énergie et les fonctions d'onde, respectivement valeurs et vecteurs propres de l'équation de Schrödinger. Néanmoins, ces modèles ne permettent pas de calculer avec précision que la charge localisée

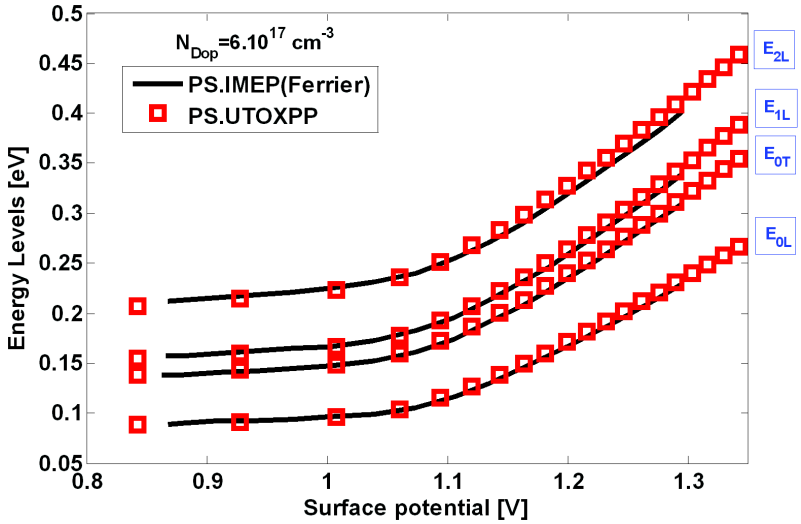


FIGURE 42 – Comparaison des quatre premiers niveaux d'énergie obtenus avec le PS.UTOXPP et PS.IMEP [55] pour différents potentiels de surface en régime d'inversion.

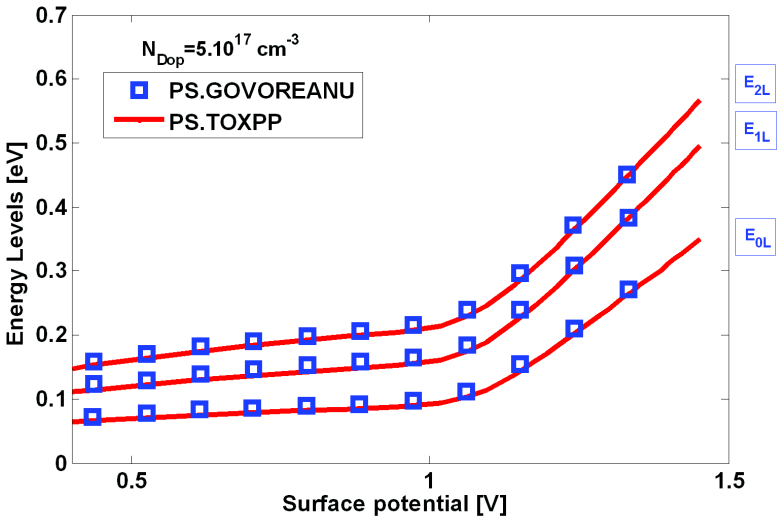


FIGURE 43 – Les trois premières sous-bandes Δ_2 obtenues avec le PS.UTOXPP et PS.Govoreanu [56] pour différents potentiels de surface en régime d'inversion.

sur le premier niveau d'énergie [60]. Ce qui est suffisant pour modéliser la capacité C-V. Cependant, la modélisation du courant de la grille nécessite une précision de calcul du deuxième niveau d'énergie puisque les porteurs localisés sur ce niveau contribuent dans le courant tunnel. Afin de calculer plusieurs niveaux d'énergie avec plus de précision, un modèle analytique basé sur une amélioration de l'approximation du puits triangulaire (TWA) a été proposé par Ferrier et al. [55]. Selon cette approche, le champ électrique effectif est égal à :

$$F_{i,v} = \frac{Q_{dep} + f_{i,v}.Q_{inv}}{\epsilon_s} \tag{5}$$

avec Q_{dep}, Q_{inv}, ϵ_s étant respectivement la charge de déplétion, la charge d'inversion et la permittivité du substrat.
En suivant ce modèle, J. Coignus et al [60] ont comparé les niveaux d'énergie calculés avec TWA améliorée (Improved TWA) en régime d'inversion avec ceux obtenus en utilisant le simulateur Poisson-Schrödinger PSL. Les paramètres $f_{i,v}$ du champ électrique effectif permettant de reproduire le résultat numérique sont f_{0L}=0.58 et f_{0T}=0.47 respectivement pour les sous-bandes Δ_2 et Δ_4. Un travail similaire est effectué avec les résultats de simulation du simulateur Poisson-Schrödinger UTOXPP. La figure 44 montre que le modèle analytique rend compte de l'effet de la pénétration des fonctions d'onde dans l'oxyde (dans ce cas il s'agit de SiO_2) et reproduit les résultats numériques des deux premiers niveaux d'énergie à forte inversion en utilisant comme paramètres $f_{i,v}$ du champ électrique effectif f_{0L}=0.88 et f_{0T}=0.73 respectivement pour les sous-bandes Δ_2 et Δ_4. Ces valeurs sont similaires à ceux trouvées par B. Govoreanu et al [56] (f_{0L}=0.86 et f_{0T}=0.61 respectivement pour les sous-bandes Δ_2 et Δ_4). Les paramètres $f_{i,v}$ sont

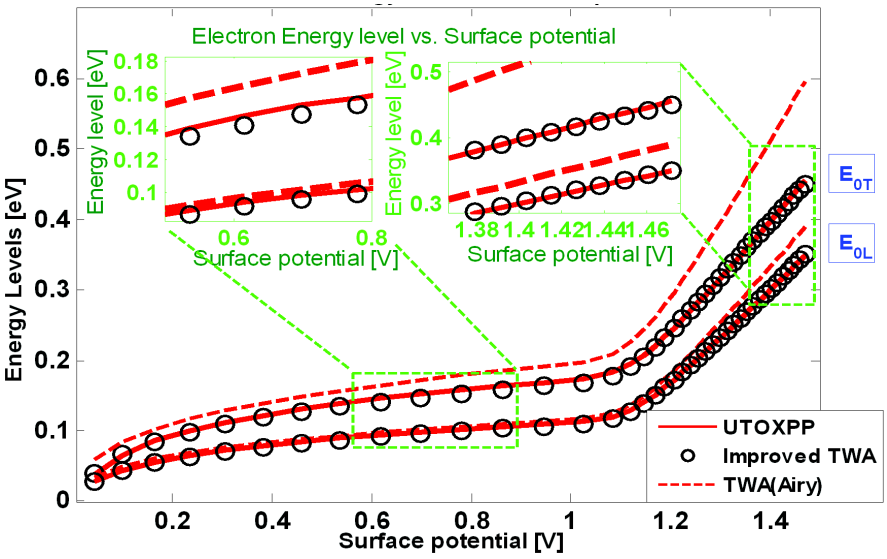


FIGURE 44 – Les deux premiers niveaux d'énergie calculés avec TWA améliorée et le PS UTOXPP pour différents potentiels de surface en régime d'inversion.

obtenus en comparant les niveaux d'énergie calculés analytiquement aux résultats de simulation Poisson-Schrödinger. Cette correction améliore la TWA en forte inversion et permet d'estimer avec précision le champ électrique effectif appliqué aux électrons de chaque sous-bande. Cependant, en comparant les différents paramètres $f_{i,v}$ correspondant à chaque simulateur PS, on note des différences de valeurs $f_{i,v}$ pour chaque sous-bande (figure 45). De plus, même si on obtient des niveaux d'énergie similaires à même potentiel de surface (figure 42), les paramètres $f_{i,v}$ correspondants au PS.IMEP (Ferrier) (f_{0L}=0.65 et f_{0T}=0.43 respectivement pour les sous-bandes Δ_2 et Δ_4 [55]) sont différents de ceux trouvés avec UTOXPP.
En conclusion, afin de comparer les résultats des simulateurs Poisson-Schrödinger, il n'est pas

pertinent de comparer les paramètres $f_{i,v}$ du champ électrique effectif.

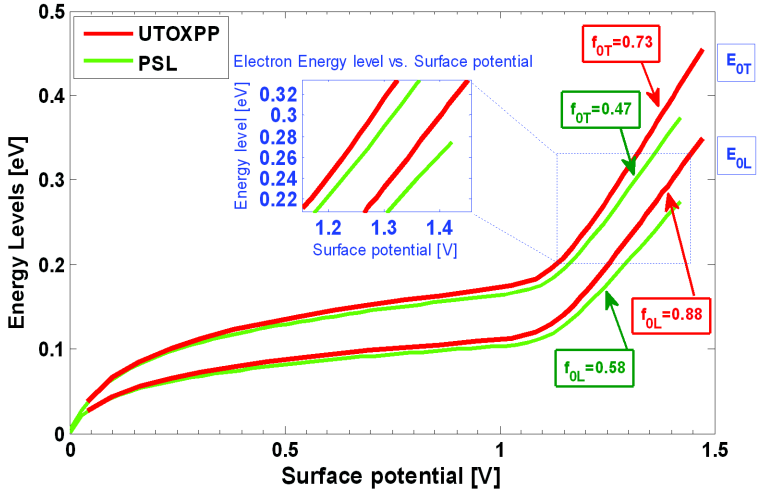
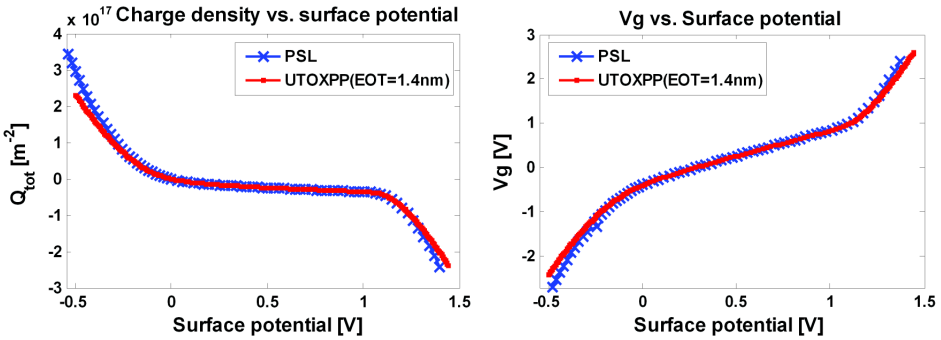


FIGURE 45 – Comparaison des paramètres f_i du champ électrique effectif des deux premiers niveaux d'énergie correspondant au PS.UTOXPP et PS.Leti (PSL).

Par ailleurs, il est important d'étudier l'impact de la différence des deux résultats de simulation d'UTOXPP et PSL (figure 45) sur le calcul de la caractéristique C-V. En effet, l'écart des niveaux d'énergie observé (E_{0L}(UTOXPP)-E_{0L}(PSL) $\simeq$35meV à Ψ_s=1.4V) se reproduit aussi sur l'évolution de la charge totale dans le semiconducteur en fonction du potentiels de surface (Q_{tot}(UTOX)-Q_{tot}(PSL)=4.08×10^{16} m^{-2} à Ψ_s=1.4V) (figure 46.a) et sur l'évolution de la tension de grille V_g calculée pour un Ψ_s donné (figure 46.b). Mais, aucune influence sur le calcul de la caractéristique C-V n'est observée pour la même EOT (figure 47).



(a) (b)

FIGURE 46 – Evolution de la charge totale et de la tension de la grille en fonction du potentiel de surface obtenues avec les deux simulateurs UTOXPP et PSL.

.2.3 Validation des simulations C-V du SiO_2/Si n-MOSFET

La figure 48 montre une bonne adéquation entre les simulations quantiques PS (UTOXPP et PSL) et les courbes expérimentales C-V pour un transistor nMOSFET (grille poly N^+ et un

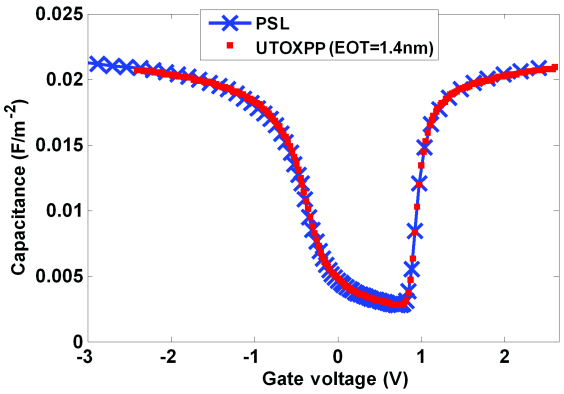


FIGURE 47 – C-V obtenus avec UTOXPP et PSL (nMOS : T_{SiO2}=0.8nm, T_{HfO2}=3nm).

substrat Si dopé p à 10^{18} m^{-3}). Un bon accord entre les valeurs d'épaisseur d'oxyde T_{ox} données par ellipsométrie et celles simulées par UTOXPP et PSL est résumé dans le tableau ci-dessous :

Ellipsometry EOT ($\AA$)	**35**	**32**	**25.65**	**20.8**	**16.1**	**15.9**	**12.1**
PSL ($\AA$)	35	32	26.5	22	19	17.5	14.5
UTOXPP ($\AA$)	35	32	26.5	22	19.5	17.5	14.5

TABLE 4 – Comparaison des valeurs d'épaisseur d'oxyde T_{ox} données par ellipsométrie et celles simulées par UTOXPP et PSL

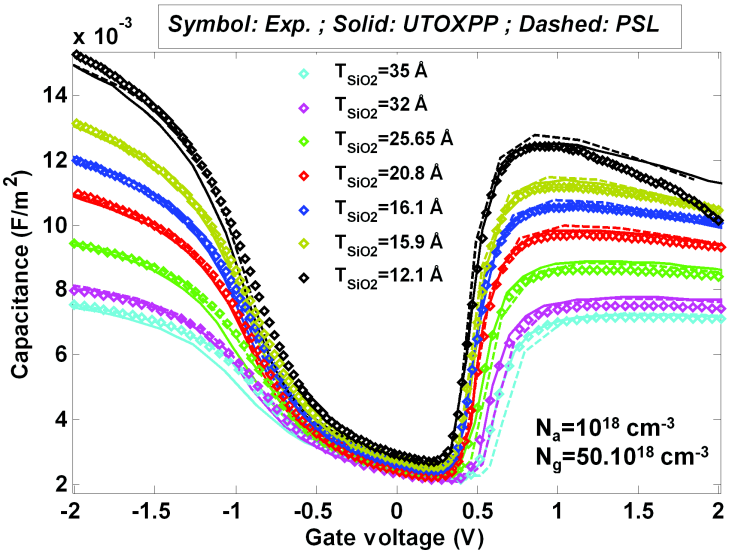


FIGURE 48 – Simulation de caractéristiques C-V expérimentales avec UTOXPP et PSL pour différentes épaisseurs de SiO_2 pour un transistor nMOS : grille poly N^+, un oxyde SiO_2 et un substrat Si. L'épaisseur de SiO_2 varie de 1.2nm à 3.5nm.

En utilisant UTOXPP, la courbe C-V du nMOSFET Si avec une grille métal a été aussi simulée et comparée aux mesures (figure 49). La simulation reproduit bien la mesure. Ce qui valide le résultat de simulation C-V de UTOXPP.

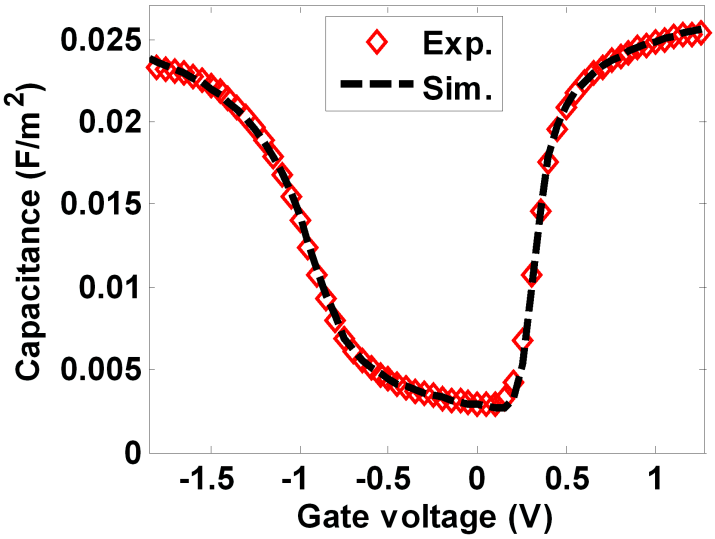


FIGURE 49 – C-V mesuré et simulé du nMOSFET : Metal/HK/IL/Si. Les épaisseurs physique des oxydes HK et IL sont respectivement 1.4nm et 1.3nm. Le substrat Si est dopé à 4.10^{17}cm^{-3}.

.3 Simulation des C-V des transistors intégrant du SiGe

.3.1 L'alliage Silicium Germanium

Le paramètre de maille de l'alliage $Si_{1-x}Ge_x$ dépend de la proportion de Ge introduit, selon la loi de Végard décrite par l'équation suivante,ou x représente le taux de Germanium :

$$a(Si_{1-x}Ge_x) = x.a(Ge) + (1-x).a(Si) \tag{6}$$

A température ambiante, la différence de maille entre le Si et le Ge est de 4.17 %. A cause de ce désaccord de maille, la croissance pseudomorphique d'une couche de SiGe sur un substrat de silicium crée une contrainte dans la couche de SiGe. La maille de l'alliage SiGe reproduit la maille plus petite du substrat dans le plan de l'interface et se déforme élastiquement dans la direction orthogonale (figure 50). La contrainte exercée sur la maille de SiGe dans les deux directions constituant le plan de l'interface est dite biaxiale.

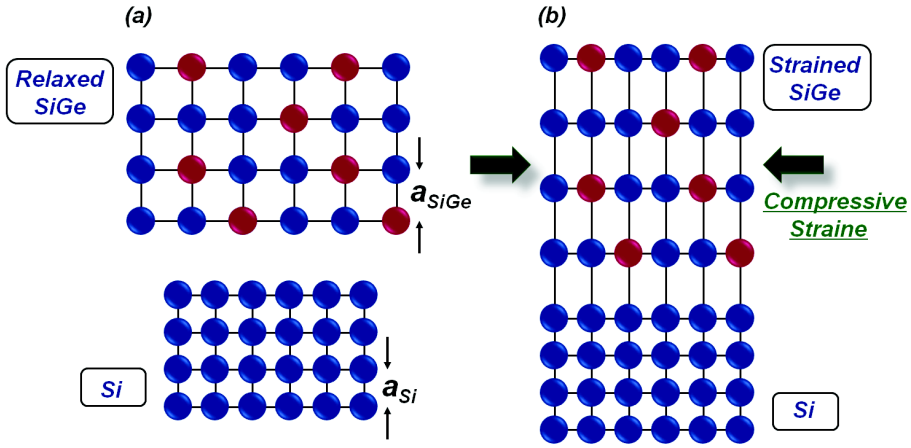


FIGURE 50 – (a) Une présentation schématique d'une couche de SiGe relaxé et d'un substrat Si. (b) Une présentation schématique d'une croissance pseudomorphique d'une couche de SiGe relaxé sur un substrat Si. La maille de l'alliage SiGe reproduit la maille plus petite du substrat dans le plan de l'interface et se déforme élastiquement dans la direction orthogonale.

.3.2 L'hétérojonction SiGe-contraint/Si

L'hétérojonction Si/SiGe contraint est de type I (voir figure 51) [62]. Les décalages des bandes sont telles que la discontinuité est reportée principalement en bande de valence. La figure 51 montre les décalages des bandes de conduction et de valence d'une couche de $Si_{1-x}Ge_x$ biaxiallement contraint sur un substrat de Si.
Les offsets des bandes de valence et de conduction de SiGe-contraint/Si sont calculés en utilisant le solveur UTOXPP selon l'approximation du potentiel de déformation. Ces données sont comparées avec des résultats théoriques et expérimentaux de la littérature avec un accord satisfaisant (figure 52), ce qui indique que la contrainte est bien prise en compte dans le modèle de structure de bande implémenté dans UTOXPP. En intégrant 30% de Ge, la discontinuité de bande de

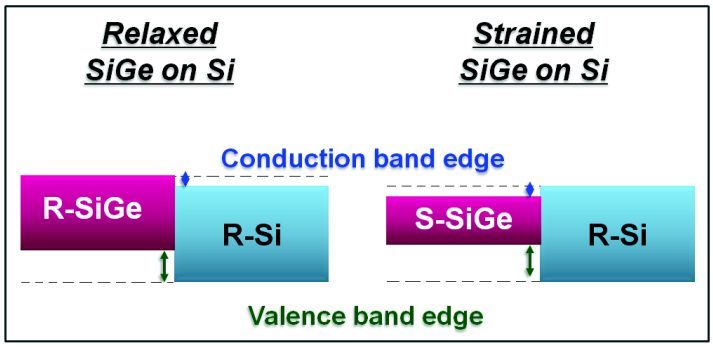


FIGURE 51 – Schéma de l'alignement de bandes entre le Si et le SiGe contraint sur Si.

valence (ΔE_v) augmente de 240mV. Tandis que la discontinuité de bande de conduction (ΔE_v) semble insensible à l'introduction du Ge dans le canal des pMOS.

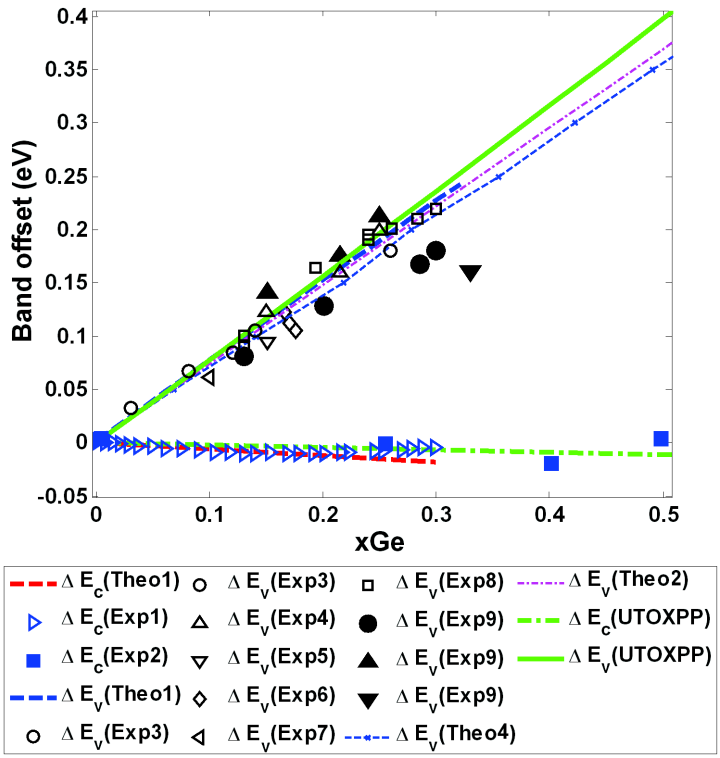


FIGURE 52 – Les offsets des bandes de valence et de conduction de $Si_{1-x}Ge_x$-contraint/Si. Les résultats calculés en utilisant le solveur UTOXPP selon l'approximation du potentiel de déformation (courbe vertes) sont comparés aux résultats théoriques et expérimentaux de la littérature : Exp1 : [107] ; Exp2 : [106] ; Exp3 : [113] ; Exp4 : [114] ; Exp5 : [115] ; Exp6 : [116] ; Exp7 : [117] ; Exp8 : [118] ; Exp9 : [112] ; Theo1 : [65] ; Theo2 : [104] ; Theo4 : [73].

.3.3 Simulation des C-V des pMOS à base de Si et SiGe

Afin de simuler un phénomène physique impliquant des particules évoluant dans un cristal, le premier élément à connaître est la fonction de dispersion de ces particules dans le milieu. Pour un semi-conducteur, l'ensemble de ces relations de dispersion des électrons E(k) constitue la structure de bande. Parmi les modèles qui ont été utilisés pour décrire la structure de bande au voisinage du centre de la zone de Brillouin, le modèle k.p se révèle comme étant efficace pour expliquer les effets délicats tels que le splitting de spin et la nonparabolicité des bandes. Prenant en compte l'interaction entre les bandes, un calcul de la structure de bande obtenue par le modèle k.p est recommandé pour modéliser les effets quantiques des hétérojonctions dans les dispositifs MOS avancés.
Dans cette partie, les C-V simulés avec le modèle k.p sont comparés aux résultats obtenus en utilisant l'approximation de la masse effective (CEMA) pour des pMOSFET à base de Si et SiGe.

La figure 53 illustre les deux structures simulées. Il s'agit du pMOSFET bulk à base de Si (structure -1-) et $Si_{0.7}Ge_{0.3}$-contraint/Si (structure -2-). Le travail de sortie de la grille métal est fixé à 4.72eV. Le diélectrique se compose de deux couches : un oxyde high-k (HK) $HfSiON$ et un oxyde interfacial (IL) $SiON$. Le SiGe est considéré biaxiallement contraint sur un substrat Si dopé n.

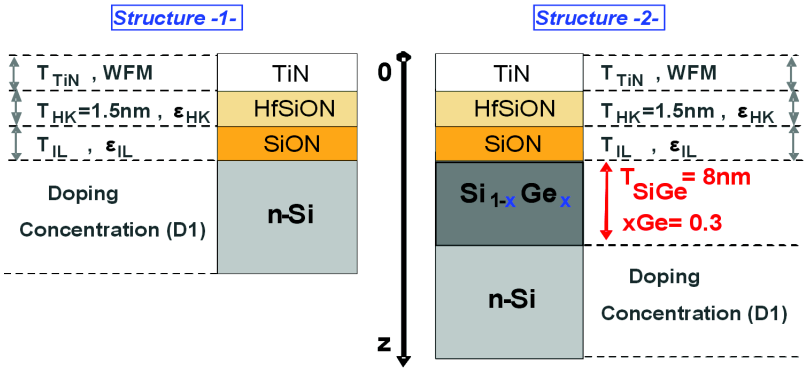


FIGURE 53 – Structures simulées du pMOSFET bulk à base de Si et $Si_{0.7}Ge_{0.3}$-contraint/Si.

La comparaison des C-V simulés pour du Si en utilisant le modèle k.p-6 bandes pour les trous et le modèle CEMA montre une légère différence en régime d'inversion (figure 54.a). En augmentant la masse de densité d'état de la bande "heavy hole" (HH) du Si (M_{DOS}), qui est égale initialement à $0.51m_0$, à $2.5m_0$ le modèle CEMA reproduit parfaitement le C-V calculé avec le modèle k.p-6. La figure 55.a compare les C-V simulés pour le pMOSFET SiGe en utilisant le modèle k.p-6 bandes pour les trous et le modèle CEMA. De la même manière que pour le Si, on observe aussi pour le SiGe une légère différence en régime d'inversion. En modifiant la M_{DOS} de la bande HH du Si à $1.5m_0$, un très bon accord est obtenu en utilisant les deux modèles. En effet, l'augmentation de la M_{DOS} a un sens physique. Ainsi, en modifiant la M_{DOS}, le modèle CEMA rend mieux en compte de la courbure des sous bandes de valence. La figure 56 compare la relation de dispersion E(k) calculée avec les modèles k.p-6 et CEMA pour la sous bande de valence la plus élevée (HH) du Si et du SiGe. Les sous bandes HH du Si et du SiGe ne sont pas paraboliques. En augmentant la M_{DOS}, nous observons que le modèle CEMA reproduit mieux la courbure de bande calculée par le modèle k.p-6.

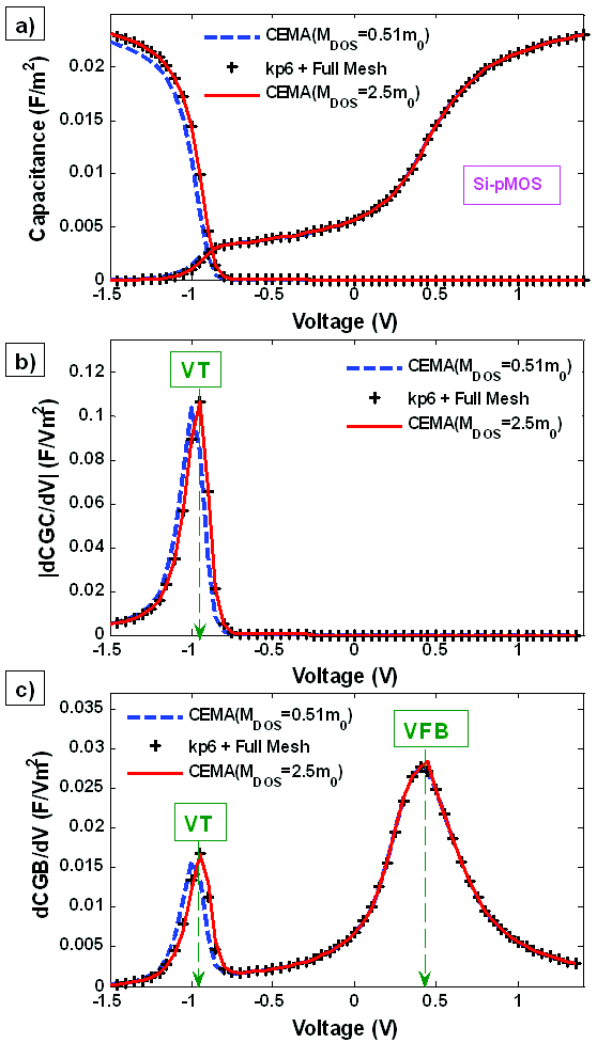


FIGURE 54 – Capacités grille-canal (CGC) et grille-bulk (CGB) simulées du pMOSFET bulk Si en utilisant les modèles k.p et CEMA.

En conclusion, en ajustant la M_{DOS} dans le modèle CEMA, les C-V simulés en utilisant le modèle CEMA reproduisent les caractéristiques C-V données en utilisant le modèle k.p-6. Cette méthode est utilisée dans la suite pour la simulation des courbes C-V.

.4 Méthodes d'extraction de VT, VFB et EOT

.4.1 Extraction de VT et VFB dans les pMOSFET $Si_{1-x}Ge_x$/Si

Récemment, une méthode pour extraire le VT et VFB dans les pFET FDSOI a été proposée. Il s'agit de déterminer VT et VFB à partir du maximum de la dérivée de la capacité grille canal par rapport à V_g. Cette partie discute la validité de cette méthode sur des transistors bulk. Elle sera d'abord vérifiée en utilisant la simulation puis appliquée au mesures de capacité CGC et CGB sur du pMOSFET bulk.

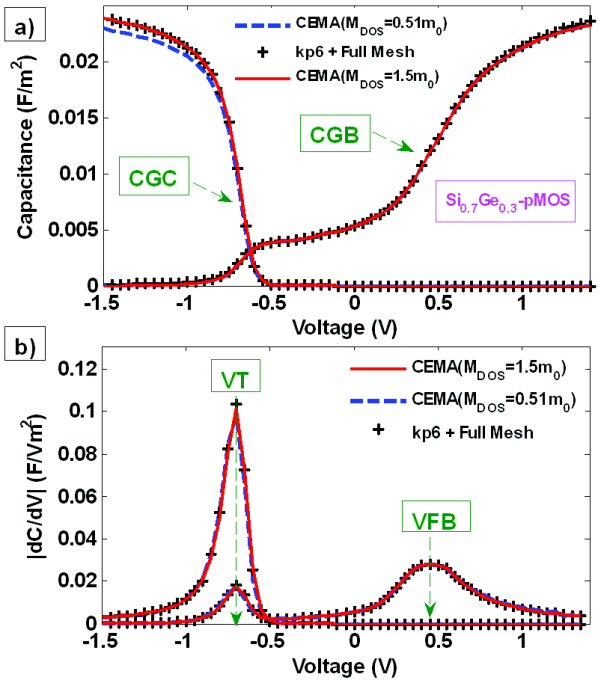


FIGURE 55 – Capacités grille-canal (CGC) et grille-bulk (CGB) simulées du pMOSFET bulk $Si_{0.7}Ge_{0.3}$-contraint/Si en utilisant les modèles k.p et CEMA.

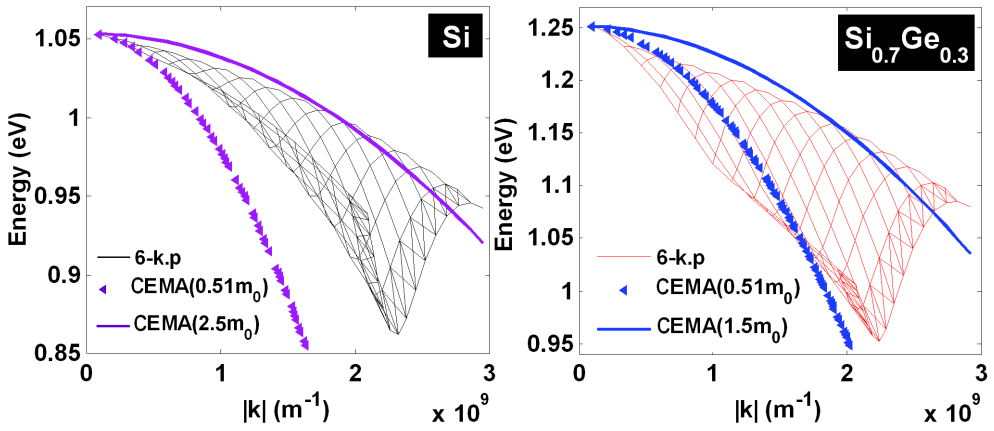


FIGURE 56 – Relation de dispersion E(k) calculée avec les modèles k.p-6 et CEMA pour la sous bande de valence la plus élevée (HH) du Si et du SiGe. Pour cette figure, la structure simulée est du FDSOI à base du Si et $Si_{0.63}Ge_{0.27}$. L'épaisseur de la couche de SiGe est de 10nm et la tension de grille appliquée est égale à -2V.

On considère alors les pMOSFET Si et SiGe présentés dans la figure 53. Pour le pMOSFET à base de Si, la dérivée de la capacité CGC simulée passe par un maximum donnant le VT (figure 54.b). La dérivée de la capacité CGB simulée passe par deux extrémum permettant de déterminer le VT et le VFB (figure 54.c).
De la même manière, pour le pMOSFET à base de SiGe le maximum de la dérivée de la capacité

CGC simulée donne le VT. La dérivée de la capacité CGB simulée passe par deux extrémum permettant d'extraire le VT et le VFB (figure 55.b).
Les VFB simulés extraits à partir de la dérivée des capacités CGB ont été validés en les comparant aux VFB déterminés à charge nulle (VFB(Q=0)). Les VT simulés extraits de la dérivée des capacités CGC ont été confirmés par les valeurs de VT extraites à 40% du maximum de la capacité.
La méthode d'extraction a été aussi appliquée au mesures de capacité sur Si et $SiGe$ (figure 57). A partir de la dérivée des capacités CGC et CGB, on détermine les VT et VFB mesurés. Les valeurs mesurées et simulées extraites sont illustrées dans le tableau 5. En intégrant 30% de Ge, on note un décalage de 0.45V de VT mesuré et une augmentation de 0.25V de VFB mesuré. Le tableau 5 montre aussi un bon accord entre simulation et mesure pour le pMOS Si. Tandis que pour le pMOS à base de SiGe, on remarque un décalage de 150mV entre simulations et mesures. Ce résultat coïncide avec le résultat trouvé dans la partie .5.2 et prouve la validité de la méthode d'extraction de VT et VFB proposée.

	Si	**$Si_{0.7}Ge_{0.3}$/Si**
VT simulé	-0.95	-0.7
VFB simulé	0.44	0.42
VT mesuré	-0.95	-0.5
VFB mesuré	0.42	0.67

TABLE 5 – VT et VFB simulés et mesurés des pMOSFET Si et $Si_{0.7}Ge_{0.3}/Si$ extraits à partir de la dérivée de la capacité.

.4.2 Extraction de l'EOT dans les pFET FDSOI $Si_{1-x}Ge_x$

Dans cette partie, on propose une nouvelle méthode d'extraction de l'EOT, basée sur la réponse du tracé de le capacité d'inversion en fonction de la charge d'inversion $C_{inv}(Q_{inv})$. La méthode d'extraction sera vérifiée par des simulations Poisson-Schrödinger puis appliquée aux mesures sur deux structures pFET FDSOI à base de Si et $SiGe$. La variation de l'épaisseur de film sera aussi étudiée.
En effet, la capacité MOS en inversion s'exprime en deux capacités en série : la capacité dans l'oxyde (C_{ox}) et la capacité dans le semi conducteur en inversion (C_{inv}). Ce qui permet l'EOT de s'écrire en fonction de la charge d'inversion sous la forme suivante :

$$EOT(Q_{inv}) = \varepsilon_{SiO_2}.\left(\left[CGC^{Exp}(Q_{inv})\right]^{-1} - \left[C_{inv}^{Sim}(Q_{inv})\right]^{-1}\right) \quad (7)$$

ou CGC^{Exp} est la capacité CGC mesurée.
La simulation a montré que la courbe $C_{inv}(Q_{inv})$ ne dépend pas de l'intégration de Ge dans le film mais du dopage de film (figure 58). De plus, le tracé de $C_{inv}(Q_{inv})$ n'est pas sensible à la variation de l'épaisseur du film dans les FDSOI Si. Ceci est également le cas pour les pFET FDSOI $Si_{0.63}Ge_{0.27}$, lorsque l'épaisseur du film est plus grande que 5 nm ; en dessous de cette épaisseur C_{inv} augmente (figure 58). En utilisant le tracé de $C_{inv}(Q_{inv})$ simulé, la méthode

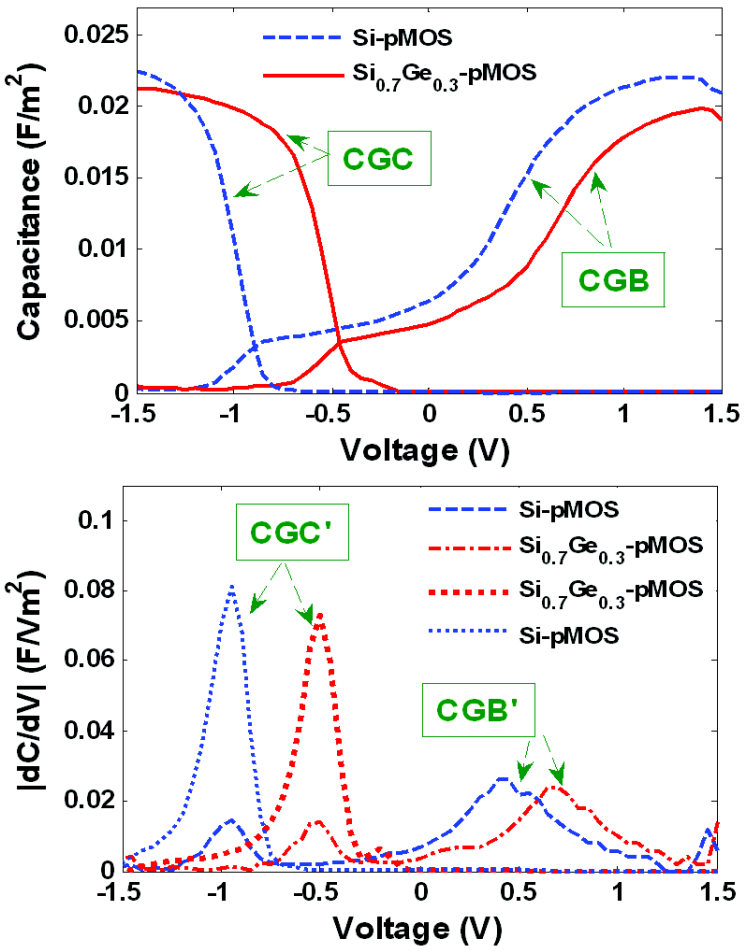


FIGURE 57 – (a) C-V mesurés des pMOSFET Si et $Si_{0.7}Ge_{0.3}$. (b) dérivée des capacités CGC et CGB mesurées (a) donnant les VT et VFB mesurés.

d'extraction de l'EOT a été appliquée aux mesures de CGC sur des pFET FDSOI à base de Si et SiGe intégrant différentes concentrations de Ge (figure 59). On remarque que la courbe de l'EOT passe par un plateau à forte inversion permettant de déterminer l'EOT correspondante. Afin de vérifier la méthode d'extraction de l'EOT, des courbes C-V sont simulées avec UTOXPP en utilisant les valeurs d'EOT extraites par la méthode proposée et comparées aux courbes expérimentales. Un très bon accord est obtenu. Ce qui confirme la fiabilité de la méthode d'extraction.

.5 Effet de l'intégration du Ge dans les structures MOS

.5.1 Dispositifs étudiés

Une étude de l'effet électrique de l'incorporation de Ge a été faite sur des pMOSFET SiGe bulk (figure 60.a) et pFET FDSOI SiGe (figure 60.b). Pour la technologie bulk, trois pMOSFET ont été analysés en faisant varier l'épaisseur de l'oxyde interfacial SiON et le dopage du substrat Si

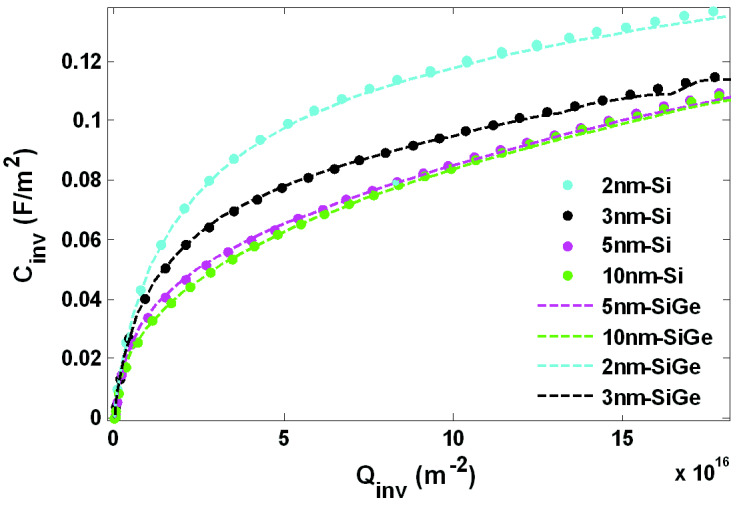


FIGURE 58 – Comparaison du tracé du $C_{inv}(Q_{inv})$ des pFET FDSOI Si et $Si_{0.7}Ge_{0.3}$.

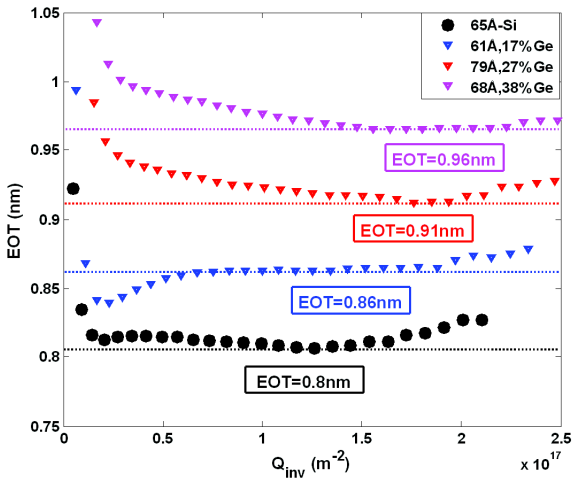


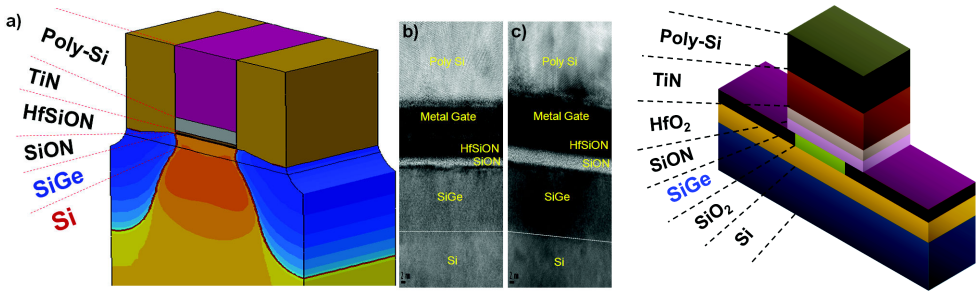
FIGURE 59 – Extraction de l'EOT des pFET FDSOI SiGe avec différentes concentrations de Ge (xGe varie de 0% à 38%) et d'épaisseurs de SiGe (T_{SiGe} varie de 6nm jusqu'à 8nm).

(tableau 6). Pour la technologie FDSOI, deux pFET FDSOI ont été étudiés en faisant varier l'épaisseur de l'oxyde interfacial SiON (tableau 7). Pour les deux technologies (bulk et FDSOI), on a étudié aussi la variation de la concentration de Ge et de l'épaisseur de la couche SiGe (figure 61).

La figure 62 illustre les tensions de seuil mesurées sur les pMOS bulk et FDSOI ($surface < 1\mu m^2$). 400mV de diminution de VT est observée en intégrant 38% de Ge dans le canal du pMOS FDSOI.

.5.2 Décalage de travail de sortie effectif de la grille

Afin d'étudier théoriquement l'effet du germanium sur les paramètres (travail de sortie effectif, EOT, tension de seuil et tension de bandes plates), les C-V de tous les pMOS bulk et FDSOI



(a) (b)

FIGURE 60 – Structure étudiée du pMOS SiGe bulk (a) et FDSOI (b).

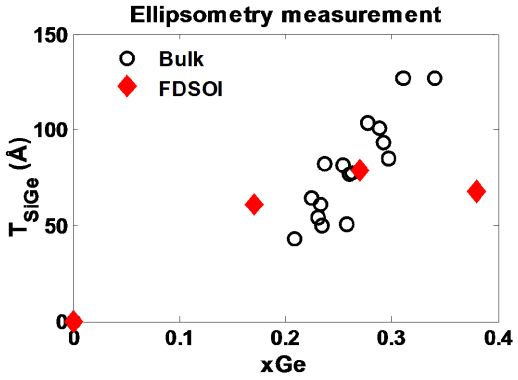


FIGURE 61 – L'épaisseur de la couche SiGe et la concentration de Ge mesurés par ellipsométrie des pMOS bulk et FDSOI étudiés.

Bulk pMOSFET	SiON thickness	Si doping concentration
VT1	TIL1	DC1
VT2	TIL1	DC2<DC1
VT3	TIL2=3×TIL1	DC2<DC1

TABLE 6 – Trois pMOSFET bulk analysés en faisant varier l'épaisseur de l'oxyde interfacial SiON (TIL) et le dopage du substrat Si (DC).

FDSOI pFETs	SiON thickness
VTFD1	T_1
VTFD2	$T_2=3 \times T_1$

TABLE 7 – Deux pFET FDSOI étudiés en faisant varier l'épaisseur de l'oxyde interfacial SiON.

ont été simulés en utilisant le simulateur UTOXPP puis comparés au mesures. Pour chaque technologie (bulk et FDSOI), un travail de sortie de la grille est considéré constant pour tous les pMOS est égale à WFM=4.67eV et WFM=4.57eV respectivement pour les pMOS bulk et

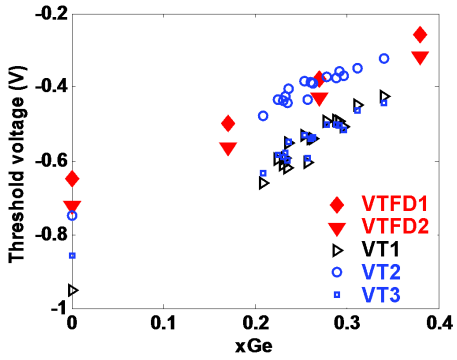


FIGURE 62 – Tensions de seuil mesurées à courant constant (Vd=-50mV, Icc=70W/L nA ou W et L sont respectivement la largeur et la longueur de la grille) des pMOS bulk et FDSOI étudiés.

FDSOI.
La figure 60 compare les C-V mesurés et simulés des pMOSFET bulk à base du Si et du SiGe. Nous observons un très bon accord entre simulation et mesure pour le pMOS Si pure (les courbes bleues). Pour le pMOSFET SiGe, nous observons également un bon accord entre le C-V simulé et mesuré, mais uniquement si on décale la courbe C-V simulée de 180mV. Un comportement similaire entre simulations et mesures est noté pour la technologie FDSOI. Ainsi, la simulation reproduit le C-V mesuré pour du Si pure. Tandis que pour les pFET FDSOI intégrant du Ge, nous observons un décalage entre simulation et mesure. Une incorporation de 38% de Ge induit un décalage de 150mV entre le C-V simulé et mesuré. Ce décalage est nommé "décalage de

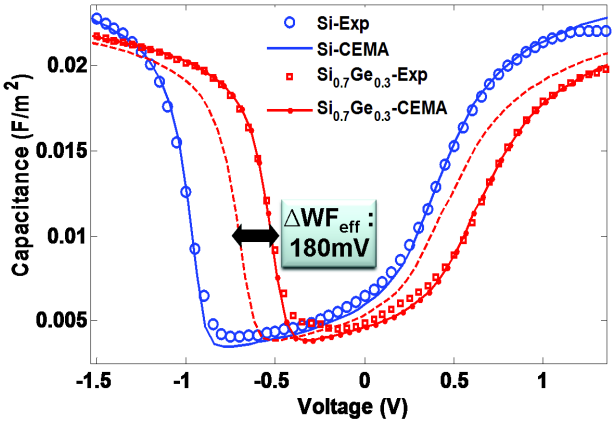


FIGURE 63 – C-V simulés et mesurés des pMOSFET bulk à base de Si et de $Si_{0.7}Ge_{0.3}$.

travail de sortie effectif de la grille" (ΔWFM). Il s'agit du décalage de travail de sortie de la grille qu'il faut ajouter au travail de sortie simulé WFM pour reproduire le C-V mesuré. La figure 64 illustre les ΔWFM obtenus pour les pMOS bulk et FDSOI à base de SiGe par rapport à une référence pMOS Si pure. Nous observons que ΔWFM est du même ordre de grandeur pour la technologie bulk et FDSOI. ΔWFM augmente linéairement avec la concentration de Ge pour atteindre 200mV en intégrant 34% de Ge dans le canal des pMOSFET bulk. La suite de ce résumé s'intéresse à la compréhension de l'origine de ce décalage de travail de sortie effectif de la

grille. En effet, les capacités MOS simulées sont considérées idéales. La présence des charges et

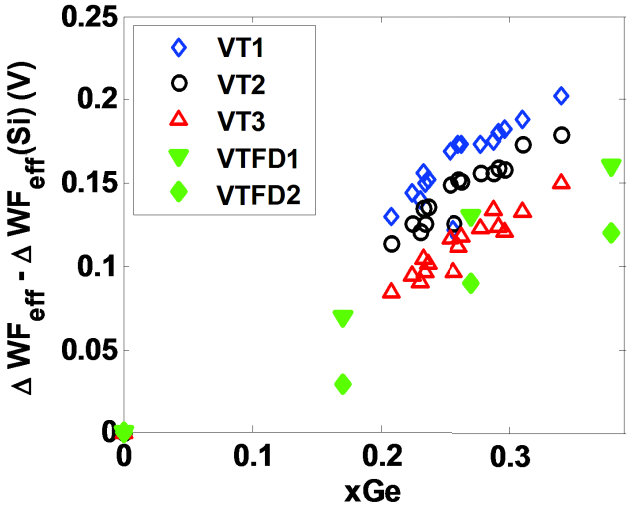


FIGURE 64 – Décalage de travail de sortie effectif de la grille ($\Delta\text{WF}_{eff}(Si_{1-x}Ge_x)$ - ΔWF_{eff} (Si)) des pMOS bulk et FDSOI à base de $Si_{1-x}Ge_x$ en fonction de la concentration de Ge (xGe).

des défauts dans l'oxyde est alors négligée. Néanmoins, dans les dispositifs réel, lors du procédé de fabrication on pourrait avoir des charges dans l'oxyde, des états d'interface et des dipôles qui peuvent affecter la capacité C-V mesurée. Un décalage de travail de sortie effectif de la grille a comme expression :

$$\Delta WF_{eff} = \Delta WF_{eff}^{IT} + \Delta WF_{eff}^{Oxide.IL} + \Delta WF_{eff}^{Oxide.HK} + \Delta WF_{eff}^{Dipoles} \quad (8)$$

Ou ΔWF_{eff}^{IT}, $\Delta WF_{eff}^{Oxide.IL}$, $\Delta WF_{eff}^{Oxide.HK}$ et $\Delta WF_{eff}^{Dipoles}$ présentent les parties de ΔWFM respectivement causées par la présence des états d'interface, des charges dans l'oxyde interfacial, des charges dans l'oxyde high-k et des dipôles dans l'empilement oxyde/grille. Dans la suite, l'origine du décalage ΔWFM observé entre simulation et mesure (figure 64) sera étudié en utilisant un ensemble de caractérisations électriques et d'analyses physicochimiques.

.5.3 Étude des états d'interface

Des mesures C-V à différentes fréquences ont été faites afin d'étudier les états d'interface dans les pMOSFET SiGe. Pour les dispositifs à base de SiGe, la figure 65 illustre une légère bosse à faible régime d'inversion. Ce qui prouve la présence des états d'interface dans ces pMOS. Des mesures de la densité des états d'interface (D_{it}) avec la méthode de pompage de charges [145] sur un pMOSFET VT1 bulk $Si_{0.7}Ge_{0.3}$ ont montré un niveau modéré des états d'interface (D_{it}=5×10^{11}cm^{-2} D_{it}) qui provoque uniquement 28mV [144] de décalage de VT. Ce qui est inférieur au 180mV de décalage ΔWFM noté dans la figure 64. Donc, la présence des états d'interface due à l'incorporation du Ge dans le canal ne suffit pas pour expliquer la totalité du décalage ΔWFM observé.

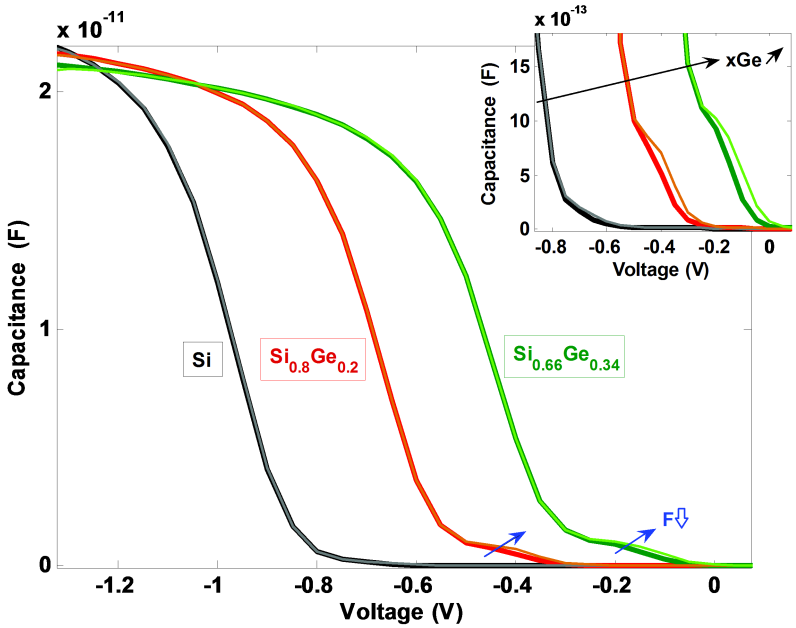


FIGURE 65 – Capacités CGC des pMOSFET VT1 bulk Si, $Si_{0.8}Ge_{0.2}$ et $Si_{0.66}Ge_{0.34}$ mesurées à deux fréquences : F=90khz (courbes foncés) et F=30khz (courbes claires).

.5.4 Étude des charge dans l'oxyde

La présence des charges dans l'oxyde interfacial crée un décalage de travail de sortie effectif proportionnelle à l'EOT. La figure 64 a montré un décalage ΔWFM du même ordre de grandeur pour un EOT mince (EOT autour de 1nm pour VT1, VT2 bulk et VTFD1 FDSOI) et un EOT trois fois plus épais (EOT autour de 3nm pour VT3 bulk et VTFD2 FDSOI). Ceci montre que la présence des charges dans l'oxyde interfacial ne peut pas expliquer le décalage ΔWFM observé.
De plus, la linéarité de ΔWFM en augmentant la concentration de Ge est notable. Cette linéarité suggère un effet de diffusion de Ge sur le travail de sortie effectif de la grille. D'après l'équation 8, le décalage ΔWFM causé par l'incorporation du Ge est donc probablement due à un effet de diffusion de Ge dans l'empilement oxyde/TiN qui crée des charges dans l'oxyde high-k ou des dipôles aux interfaces présentées dans la figure 66.

.5.5 Étude des charge dans l'oxyde high-k et des dipôles

Afin d'étudier la diffusion de Ge dans l'empilement oxyde/TiN dans les pMOS intégrant du SiGe, des mesures physicochimiques ont été effectuées sur deux pMOSFET SiGe bulk VT1 et VT3.
Des mesures "HAADF-Scanning Transmission Electron Microscopy" (STEM) [149][137], sensibles à la fraction molaire des matériaux [150], ont montré pour un pMOSFET $Si_{0.69}Ge_{0.31}$ (figure 67) des profils abrupts à chacune des trois interfaces présentées dans la figure 66. La faible diffusion de Ge est confirmée par de mesures "Energy Loss Electrons Spectroscopy" (EELS) [153] (figure 68) sur le pMOSFET bulk $Si_{0.69}Ge_{0.31}$ VT3. La figure 68 illustre un profil de diffusion de Ge (tracé en bleu) abrupt et qui n'atteint pas l'oxyde high-k. Les résultats STEM

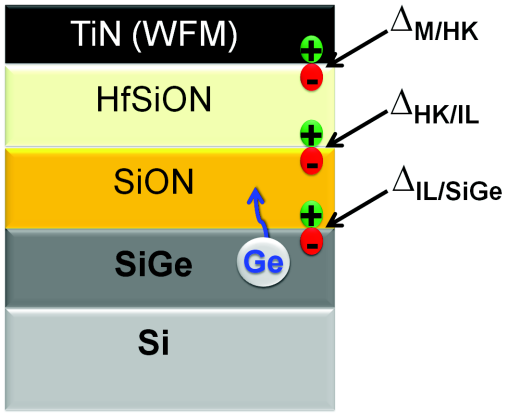


FIGURE 66 – Présentation schématique des dipôles aux interfaces de l'empilement oxyde/TiN dans un pMOSFET SiGe.

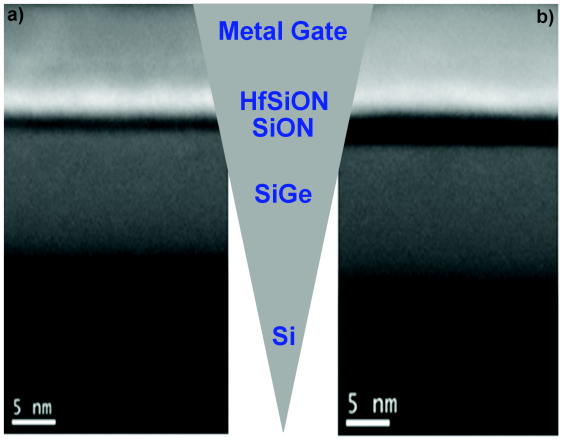


FIGURE 67 – Image HAADF-STEM de l'empilement $Si/SiGe/SiON/HfSiON$/grille du pMOSFET bulk $Si_{0.69}Ge_{0.31}$ VT1 et VT3 : a) VT1, b) VT3.

et EELS ont été vérifiés aussi avec des mesures "Time-of-flight Secondary Ion Mass Spectrometry" (TOF-SIMS) [39][155] sur deux pMOSFET bulk VT1 et VT3 intégrant du SiGe (avec 20% et 30% de Ge). La figure 69 ne détecte pas de Ge à l'interface TiN/high-k. Ce qui confirme les résultats STEM et EELS et prouve que la présence des dipôles à cet interface, causé par la diffusion du Ge, ne peut pas expliquer le décalage ΔWFM observé. De plus, les mesures SIMS ont démontré que le Ge diffuse de la même manière dans l'oxyde épais (VT3) et l'oxyde mince (VT1). Ainsi, les profils de diffusion de Ge analysés par SIMS sont parfaitement parallèles (figure 69). En comparant ces profils à même profondeur (à même abscisse), près de l'interface SiON/HfSiON, on remarque un faible niveau de Ge. Notamment, on observe 10 fois moins de Ge pour l'oxyde épais (VT3) que celui pour l'oxyde mince (VT1).
Nous rappelons que la figure 64 illustre un décalage ΔWFM similaire quelque soit l'épaisseur de l'oxyde (VT1 et VT3 par exemple). Ceci prouve que la présence des charges dans l'oxyde high-k et de dipôles à l'interface SiON/HfSiON ne peut pas expliquer le décalage ΔWFM. Donc la modulation des dipôles due à la diffusion de Ge ne peut se produire qu'à l'interface

SiGe/oxyde, ce qui explique l'augmentation du travail de sortie effectif de la grille ΔWFM.

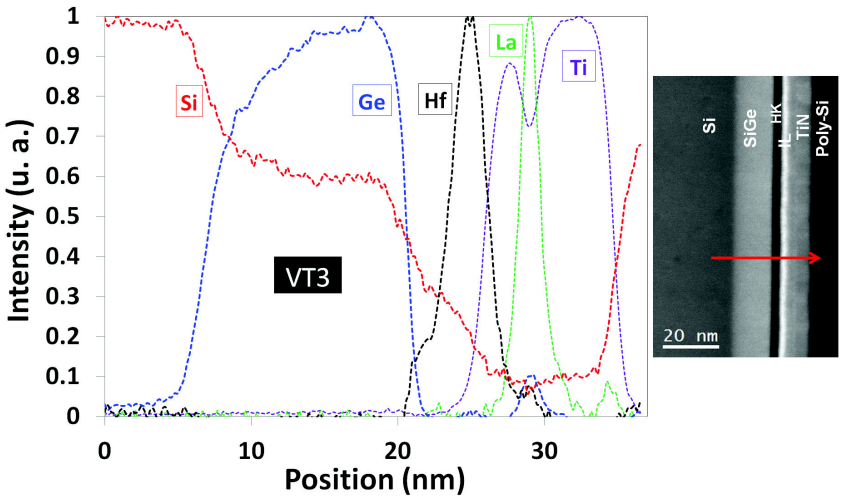


FIGURE 68 – Caractérisation EELS effectuée sur le pMOSFET bulk $Si_{0.7}Ge_{0.3}$ VT3.

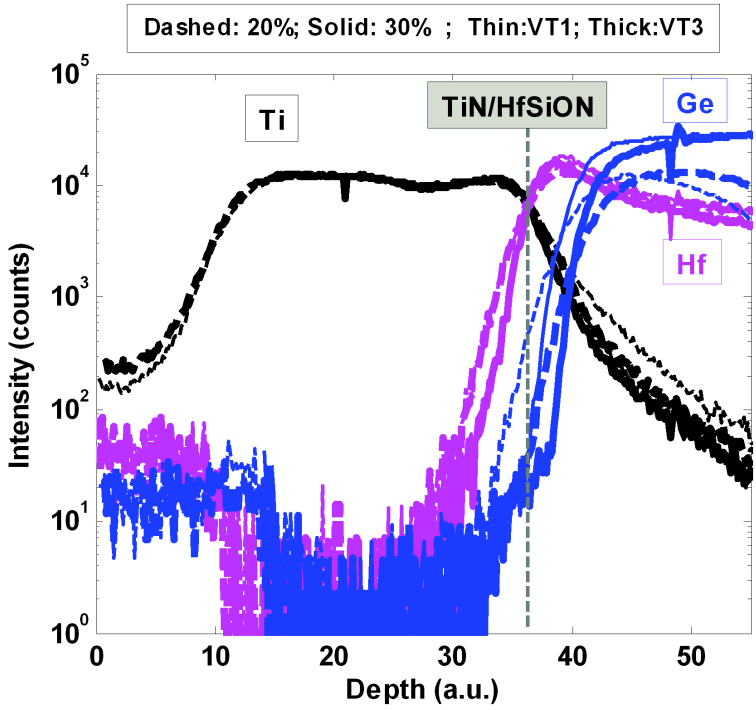


FIGURE 69 – Comparaison des profils SIMS (alignés par rapport à l'interface TiN/high-k) :Courbes épaisses : VT3, courbes minces : VT1 ; trait continu : 30%, pointillé : 20%.

.5.6 Conclusion

Après avoir rappelé une partie des contraintes liées à la réduction de la taille des transistors, l'introduction générale se focalise sur l'objectif de la thèse. L'intégration de SiGe comme canal de conduction des transistors pMOS nécessite : d'une part la proposition des méthodes d'extraction des paramètres électriques : VT, VFB et EOT ; d'autre part la compréhension de l'effet électrique de l'incorporation du Ge dans le canal.

La deuxième partie valide la simulation de la courbes C-V en utilisant le simulateur UTOXPP et en particulier de la prise en compte des effets quantiques. D'abord, une comparaison est ainsi effectuée entre 3 simulateurs Poisson-Schrödinger pour une structure composée d'une grille métallique TiN, d'un oxyde de grille SiO_2 et d'un substrat Si dopé p. : le simulateur développé par ST (UTOXPP), celui développé par le LETI (PSL) et Synopsis. Puis, les résultats de simulation C-V sont comparés aux données expérimentales sur un nMOSFET composé d'une grille polysilicium N+, d'un oxyde SiO_2 et d'un substrat Si, avec différentes épaisseurs de l'oxyde de grille. Enfin, des caractéristiques simulées et expérimentales d'une structure contenant un isolant double couche (nMOSFET métal/HfSiON/SiON/Si) sont comparées avec un très bon accord.

La troisième partie porte sur la prise en compte de la couche de SiGe contrainte dans la simulation de la courbe C-V. On débute par la description de la structure de bande de l'hétérostructure SiGe contraint/Si, qui doit être calculée rigoureusement pour une simulation précise des caractéristiques C-V des structures intégrant du SiGe. Le simulateur UTOXPP est alors modifié pour prendre en compte la présence de SiGe ainsi que la contrainte mécanique. Les offsets des bande de conduction et de valence du SiGe contraint/Si sont comparées avec des résultats théoriques et expérimentaux de la littérature avec un accord satisfaisant, ce qui indique que la contrainte est bien prise en compte dans le modèle de structure de bande implémentée dans UTOXPP.
Le solveur UTOXPP dispose de deux méthodes permettant de simuler la structure de bande de SiGe contraint sur Si : la méthode CEMA basée sur l'approximation de la masse effective et la méthode k.p-6 (full band). La simplification des calculs qui utilise le concept de la masse effective (la méthode CEMA) des porteurs donne une charge plus faible que le modèle exact (k.p-6). Les masses de densité moyennes sont alors ajustées pour que les courbes C-V soient identiques entre le modèle exact et le modèle CEMA. Cette solution est utilisée dans la suite pour la simulation des caractéristiques C-V.

La quatrième partie propose les méthodes d'extraction de VT, VFB et EOT en commençant par la validation de la méthode split C-V pour l'extraction du VT et VFB dans les pMOSFET SiGe/Si bulk par des simulations Poisson-Schrödinger avec le logiciel UTOXPP. Les paramètres sont extraits sur des transistors pMOS bulk dont le canal de conduction est en Si ou en $Si_{0.7}Ge_{0.3}$. Ensuite, cette méthode d'extraction du VT et VFB est appliquée aux caractéristiques C-V mesurées sur des pMOSFET Si et $Si_{0.7}Ge_{0.3}$/Si ; ceci permet également d'étudier l'impact du Ge dans les pMOSFET bulk. Dans un deuxième temps, une nouvelle méthode d'extraction du EOT est proposée. Elle est basée sur le tracé de la capacité de la couche d'inversion en fonction de la charge d'inversion. La simulation a montré que l'allure de ce tracé ne dépend pas du type de substrat mais du dopage. La capacité d'inversion n'est pas sensible à l'intégration

du Ge ni de la variation d'épaisseur du film dans une structure FDSOI, lorsque l'épaisseur du SiGe est plus grande que 5 nm ; en dessous de cette épaisseur la capacité d'inversion augmente. Cette partie se termine par l'extraction de l'EOT des transistors pFETs FDSOI à film mince Si et SiGe et la validation de la méthode proposée.

La dernière partie traite l'effet électrique du germanium dans les transistors pFETs Bulk et FDSOI dont l'empilement de grille est constitué de SiON/HfSiON/TiN et de SiON/HfO_2/TiN respectivement. La comparaison des caractérisations électriques (C-V) avec les simulations PS (pour différentes épaisseurs de SiGe et concentrations de Ge) démontre que pour prédire les C-V des pMOS SiGe, il est nécessaire, en plus de la structure de bande du SiGe, de tenir compte d'une augmentation supplémentaire du travail de sortie effectif de la grille métallique (ΔWFM) proportionnelle à la concentration de Ge. Cette augmentation ne peut pas être expliquée par des charges piégées à l'interface, car leur densité mesurée est très faible. La dépendance linéaire avec la concentration de Ge suggère un effet de diffusion de Ge sur le travail de sortie effectif de la grille. Diverses caractérisations physiques (EELS combinée avec SIMS et analyse HAADF-STEM) sont effectuées afin de déterminer l'origine de l'augmentation du travail de sortie ΔWFM. Les analyses STEM, EELS et SIMS démontrent que la diffusion de Ge est très faible dans l'oxyde interfacial, dans le high-k ou à l'interface high-k/IL. Par conséquent, la présence de charges dans le high-k n'explique pas l'augmentation du travail de sortie ΔWFM. En conclusion, la modulation du dipôle due à la présence de Ge pourrait se produire à l'interface SiGe/oxyde.