Development of TCAD modeling for low field electronics transport and strain engineering in advanced Fully Depleted Silicon On Insulator (FDSOI) CMOS transistors

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Development of TCAD modeling for low field electronics transport and strain engineering in advanced Fully Depleted Silicon On Insulator (FDSOI) CMOS transistors

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Abstract

The design of nanoscale CMOS devices brings new challenges to TCAD community. Indeed, nowadays, CMOS performances improvements are not simply due to device scaling but also to the introduction of new technology "boosters" such as new transistors architectures (FDSOI, trigate), high-k dielectric gate stacks, stress engineering or new channel material (Ge, III-V). To face all these new technological challenges, Technology Computer Aided Design (TCAD) is a powerful tool to guide the development of advanced technologies but also to reduce development time and cost. In this context, this PhD work aimed at improving the modeling for 28/14 and 10FDSOI technologies, with a particular attention on mechanical strain impacts. In the first section, a summary of the main models implemented in state of the art device simulators is performed. The limitations and assumptions of these models are highlighted and developments of the in-house STMicroelectronics KG solvers are discussed. In the second section, a "top down" approach has been set-up. It has consisted in using advanced physical-based solvers as a reference for TCAD empirical models calibration. Calibrated TCAD reproduced accurately split-CV mobility measurements varying the temperature, the back bias and the Interfacial Layer (IL) thickness. The third section deals with a description of the methodologies used during this thesis to model stress induced by the process flow. Simulations are compared to nanobeam diffraction (NBD) strain measurements. The use and calibration of available TCAD models to efficiently model the impact of stress on mobility in a large range of stress (up to 2GPa) is also discussed in this section. The last part deals with TCAD modeling of advanced CMOS devices for 28/14 and 10FDSOI technology development. Mechanical simulations are performed to model the stress profile in transistors and several solutions to optimize the stress configuration in sSOI and SiGe-based devices have been presented.

Contents:

Chapter III: Mechanical simulations of the process-induced stress in 14FDSOI MOSFETs and comparison with nanobeam diffraction strain measurements

Chapter IV: ST-oriented device applications

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List of abbreviations:

BOX; Buried OXide
BTE: Boltzmann Transport Equation
CBED: Convergent-Beam Electron Diffraction
CTE: Coefficient of Thermal expansion
DD: Drift Diffusion
EMA: effective mass approximation
EOT: Equivalent Oxide Thickness
FDSOI: Fully depleted Silicon On Insulator
GPN: Generalized Prange Nee
HP: High Power
HREM: High-Resolution Electron Microscopy
HoloDark: dark-field electron holography
LP: Low Power
LSTP: Low Stand-by Power (LSTP)
IL: interfacial layer
KG: Kubo-Greenwood
LCS: Local Coulomb Scattering
MC: Monte Carlo
MSMC: Multi-Subband Monte Carlo
NEGF: Non-Equilibrium Green Function
NBD: Nano-Beam Diffraction
PS: Poisson Schrödinger
RCS: Remote Coulomb Scattering
RTA: Relaxation Time Approximation
SCE: Short Channel Effects
SOI: Silicon On Insulator
STI: Shallow Trench Isolation
SR: Surface Roughness
sSOI: strained Silicon On Insulator
TEM: Transmission Electron Microscopy
TCAD: Technology computer-aided design
TDF: Tensorial Dielectric function

Introduction

Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) is the semiconductor industry key elementary device, enabling the development of the impressive number of electronic applications. The International Roadmap for Semiconductors (ITRS) [1], which is the guideline for the technology improvements in MOSFET fabrication, aims at anticipating risk factors in the developments of the microelectronic industry. The diversification of microelectronic application has led to a diversification of the ITRS for High Power (HP), Low Power (LP) and Low Stand-by Power (LSTP) roadmap. Nevertheless, regardless to the applications, the semiconductor industry has steadily scaled device dimensions to improve performance and to reduce cost [2]. From 20 µm to 90 nm technology nodes, performance improvements were essentially due to the scaling of transistors dimensions according to scaling rules (as illustrated in Figure 1 for gate oxide stack). Nevertheless, conventional scaling of MOSFET dimensions, according to ITRS requirements, faces physical and economical limits. Indeed, the scaling rules which have allowed for more than 30 years the semiconductor industry to constantly improve transistors performance while reducing their costs, faces increasing difficulties and limitations. These challenges are the control of leakage currents (short channel effects (SCE), tunneling current through the gate insulator …), the enhancement of transport properties within the channel, and the control of variability (due to process or doping fluctuations).

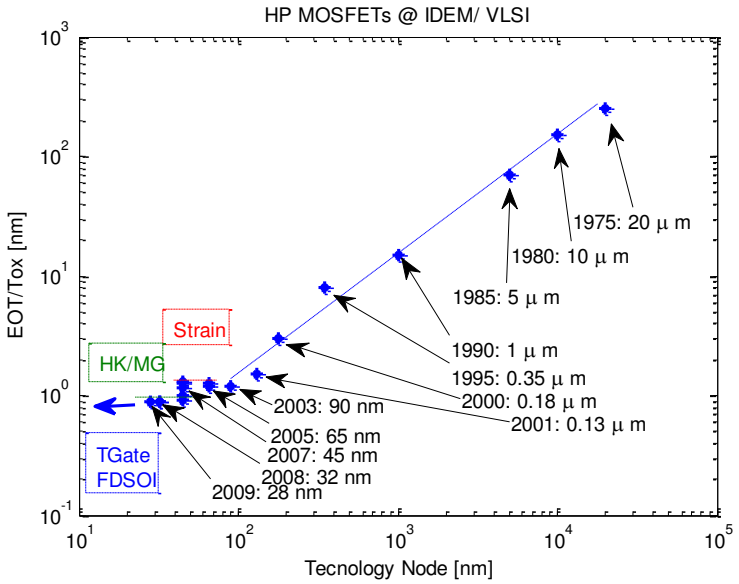

Figure 1 : Evolution of the gate stack dimension with the technology node at HP. Data are extracted from IEDM/VLSI presentations.

Nowadays, the ITRS performance requirement has led to the introduction of technology "boosters", such as the use of new transistors architectures (FDSOI, trigate), high-k dielectric gate stacks, stress engineering or new channel material (Ge, III-V). The diversity of technological solutions has induced different strategies in the industrial development, as illustrated in Figure 2 for STMicroelectronics and INTEL. From the 28 nm technology node, STMicroelectronics has started the development (from 2010 to 2015) of planar transistors on Silicon On Insulator (SOI) substrate. This architecture has many advantages, such as a better electrostatic control of the channel, leading to a reduction of SCE [3]. In addition, contrary to FinFET for instance, the dimensions of FDSOI planar transistors can be easily changed on the same circuit, as sometimes required in non-digital function, such as analog, RF, or I/O circuits. It also offers the possibility of adjusting the threshold voltage by applying a back bias (when thin buried oxide BOX are used), giving flexibility to circuit designers to combine high performance and low power transistors in the same technology. The use of lightly doped channel may also reduce

the issue of transistor matching in SRAM cells for instance. However, even ultra-power technology needs a constantly increasing circuit speed, which means that the use of stress engineering to enhance transport properties is mandatory in FDSOI technology, as it was before for bulk transistors previous nodes. This task is particularly challenging in fully depleted SOI transistors, due to the specific mechanical properties of nanometer thin silicon film on the top of an insulator.

In addition of conventional stressors, the 14DFSOI technology will include SiC (for nMOS) and SiGe (for PMOS) source and drain, as well as strained SiGe channel. Additional technological solutions must be found for the 10 nm FDSOI node. Many options are possible such as sSOI substrate [4], Germanium or III-V channel material [5].

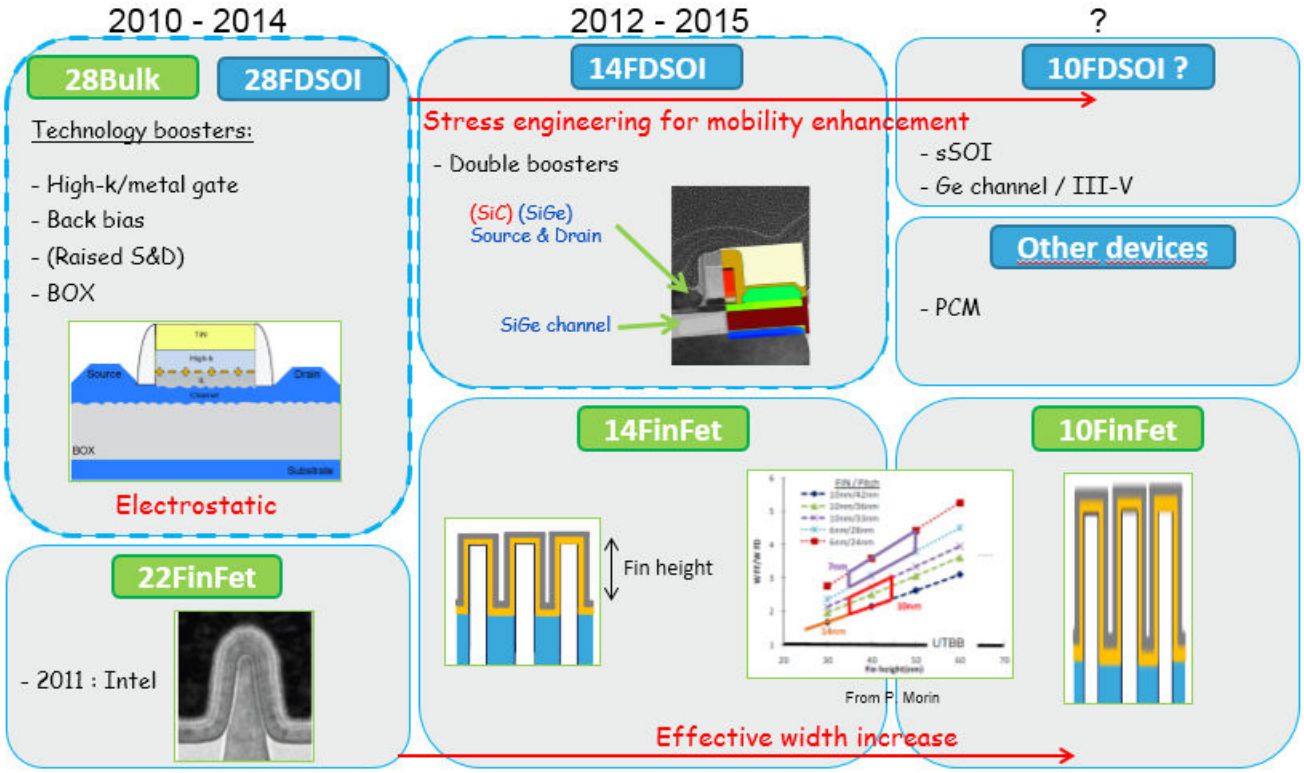

Figure 2 : STMicroelectronics and Intel roadmaps.

To face all these new technological challenges, Technology Computer Aided Design (TCAD) is a powerful tool to guide the development of advanced technologies. Indeed, TCAD support for FDSOI technology development can reduce cost and development time, but also secure technology choice. On line with STMicroelectronics technology development strategies, this PhD work aims at improving the modeling for 28/14 and 10FDSOI technologies, with a particular attention to the modeling of mechanical strain.

In this context, two main development axes have been identified, corresponding to process and electrical simulations. Concerning process simulation, the modeling of intentional or non-intentional process-induced stress is needed. Concerning electrical simulations, as many solvers can be used to model the transport in advanced structures, a benchmarking is needed. From a practical point of view, these solvers differ from 1/ the correctness of the model used, 2/ the CPU time needed to make it run, 3/ the time needed to calibrate the simulation on experiments (Figure 3). More specifically, Drift Diffusion based solvers have been extensively used in industry, essentially thanks to the simplicity of their use. However, the validity on advanced technologies of such model is more than questionable, and many parameters needed in the simulation are purely empirical models, requiring complex calibration procedure. In this context, many sophisticated solvers are now available, such as Kubo-

Greenwood (KG), Multi-Subband Monte Carlo (MSMC) or NEGF solvers, offering attractive alternative to Drift Diffusion. In addition, these tools can also be used to calibrate Drift Diffusion solvers, when users need to keep using it.

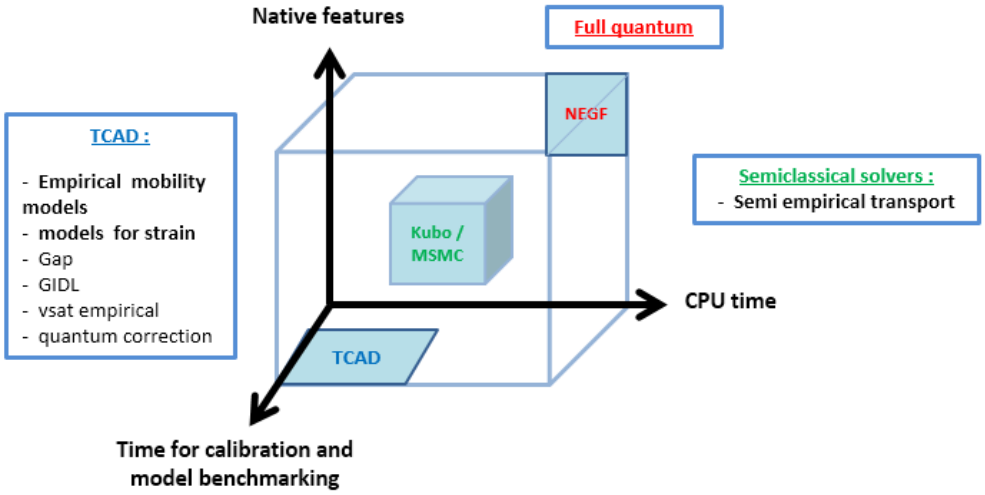

Figure 3 : List of available solvers used during this thesis to model transport in FDSOI devices.

Purpose and strategy of the thesis:

The main challenges of this PhD work are:

1/ to improve STMicroelectronics in-house advanced solvers and their use (range of validity and applicability to advanced technologies, advantages and drawbacks, comparison to other models …). In particular, one of this solver (UTOXPP) is a 1D Poisson-Schrodinger solver coupled with the Kubo-Greenwood (KG) formalism for mobility calculations. It can handle ultra-thin body n & p channels, most of the relevant scattering mechanisms and strain. It will be used as a reference tool for TCAD empirical mobility models validation and calibration. Despite several efforts along the last ten years, this topic still constitutes a research subject, as the capability of 1D KG solvers to reproduce n & p mobility experiments on a large set of sample with the same parameters (versus channel materials, strain, scattering mechanisms, front and back bias …) is still under debate.

2/ to develop an approach to simulate process-induced stress in state of the art MOS transistors. In such case, the industrial software Synopsys Sentaurus process (Sprocess) has been used as a "virtual fab" to simulate each process steps and to evaluate the level of mechanical stress. Technological solutions to enhance the stress configuration will also be addressed.

3/ to be able to reproduce the electrical characteristic of a complete set of 28 nm and 14nm FDSOI experimental data.

To investigate these three challenges, research collaborations between industrial and academic actors have been established (Figure 4). Thus this PhD thesis was carried out in collaboration between STMicroelectronics, IMEP-LAHC, CEA LETI and the university of Udine in the frame of several European and French projects (Places2be, Quasanova…). Internally to STMicroelectronics, a strong collaboration is established with the "physical characterization" team for stress/strain measurements, with the "electrical characterization" team and with the "process integration team" for the development of 28 and 14FDSOI technologies.

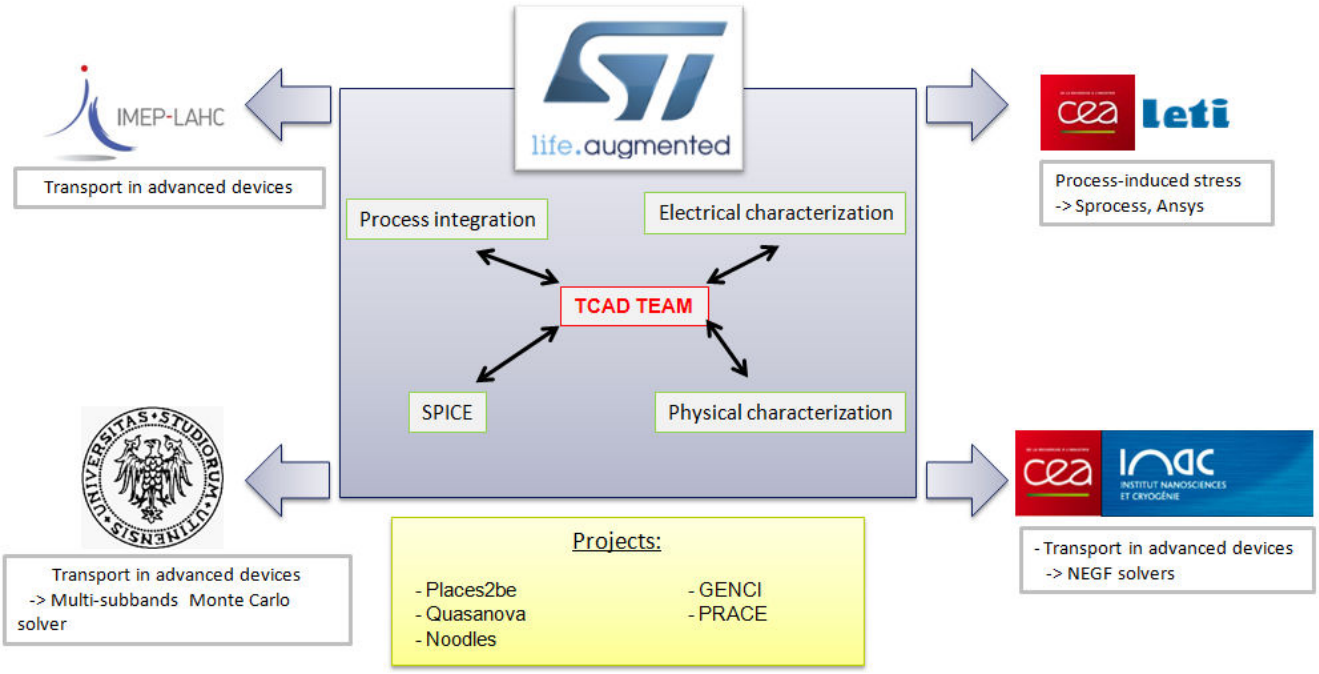

Figure 4 : Description of the internal and external collaborations during the thesis.

Organization of the thesis:

The manuscript is organized as follow:

- Chapter 1 summarizes the main models implemented in state of the art device simulators. The limitations and assumptions of these models are also highlighted and developments of the in-house STMicroelectronics KG solvers are discussed.

- Chapter 2 deals with a comparison of the different approaches currently available to model low field transport in advanced Fully Depleted SOI transistors. Simulations are then compared to split CV mobility measurements.

- Chapter 3 aims at describing the methodologies used during this thesis to model stress induced by the process flow. Simulations are compared to nanobeam diffraction (NBD) strain measurements. The use and calibration of available TCAD models to efficiently model the impact of stress on mobility in a large range of stress (up to 2GPa).

- Chapter 4 deals with TCAD modeling of advanced CMOS devices. Mechanical simulations are performed to model the stress profile in 14FDSOI transistors with an emphasis on the modeling of the relaxation of the stress during STI process steps and the impact of SiGe source and drain.

Chapter I:

Device modeling: physics and state of the art models description for advanced transport solvers

I.1 Introduction

Device modeling plays an important role in the development of advanced silicon technologies by allowing to reduce cost and development time but also secure technology choices. The term device modeling refers to a collection of models and methodologies describing carrier transport and other physical effects in semiconductor devices. The transport models range from the classical Drift Diffusion (DD) approach, which is widely used in industry due to its simplicity and efficiency, to more complex and computationally demanding ones such as semiclassical or quantum transport models. Among quantum and semiclassical models, the Non-Equilibrium Green's function (NEGF) formalism and the Monte Carlo (MC) method are commonly used techniques to solve respectively the Schrödinger and the Boltzmann transport equations (BTE) with few approximations or hypotheses. Advanced transport solvers such as NEGF, MC or KG solvers require an accurate description of the band structure of the semiconductor and also of the scattering mechanisms limiting the mobility in these devices. Moreover, after the emergence of stress engineering to enhance electrons and holes mobilities, the modeling and understanding of stress effect on band structure and mobility has become a predominant task of modern simulation tools. The aim of this first chapter is to review the main models implemented in the device simulators that have been used during this thesis. The limitations and assumptions of these models are also highlighted.
In the first part of this chapter, we briefly review the methodologies to calculate the band structure of semiconductors that have been used during this thesis and particularly the effective mass approximation (EMA) and the 6-bands k.p model. The second part is dedicated to the description of the main approaches for modeling carrier transport in semiconductor devices and their limits of applicability. Then, in the last part, we presented an accurate description of the approach used in semi-classical solvers to model the main scattering mechanisms responsible of the mobility degradation in UTBB FDSOI devices. We focused on the description of phonons, coulomb, surface roughness and alloy scattering mechanisms.

I.2 Band structures calculation

Band structure calculation methods can be split into two general categories [6]. The first category includes the ab initio methods, such as Hartree-Fock or Density Functional Theory (DFT), which calculate the electronic band structure from first principles, i.e., without the need for empirical fitting parameters. The second category regroups empirical methods such as the empirical pseudopotential method (EPM) [9], the tight-binding [7] [8], or the k.p method [10]. These techniques are based on the resolution of the one-electron Schrödinger equation and are computationally less expensive than ab initio calculations. In this thesis, the band structure has been calculated using 1) the effective mass approximation for electrons and 2) a 6-bands k.p model for holes. In this section we briefly review the principle of the k.p method and describe approaches used for the calculation of the conduction and the valence bands structure in silicon, germanium and silicon germanium alloy. The impact of strain and confinement (case of an inversion layer) on material band structure is also discussed.

1.2.1 The k.p method

The k.p is a general technique based on expansion of the Schrödinger equation of the crystal in the neighborhood of high symmetry points. This method allows to effectively obtain the band structure close to a given location in the reciprocal space provided that the eigenenergies and the eigenfunctions

are known at this point. The idea of the method was formulated in the fundamental work by Luttinger and Kohn [10] and is briefly reviewed in this part.

According to the Bloch theorem, the solution of the Schrödinger equation with the periodic potential $U_C(r)$

$$H_C\psi_v(r) = \left[-\frac{\hbar^2}{2m_0}\nabla^2 + U_C(r)\right]\psi_v(r) = E_B\psi_v(r) \tag{1.1}$$

is in the following form:

$$\psi_{vk}(r) = \exp(i\,k\,.\,r)\,u_{vk}(r) \tag{1.2}$$

Where k is the wave vector in the first Brillouin zone and $u_{vk}(r)$ is the periodic Bloch amplitude. Substituting the Bloch wavefunction (equation 1.2) into the Schrödinger equation (equation 1.1), and using the notation $p = -i\hbar\nabla$, one arrives at the following equation:

$$\left[\frac{p^2}{2m_0} + U_C(r) + \frac{\hbar}{m_0}\,k.p\right]u_{vk}(r) = \left[E_{vk} - \frac{\hbar^2k^2}{2m_0}\right]u_{vk}(r) \tag{1.3}$$

The term $\left[\frac{p^2}{2m_0} + U_C(r)\right]$ is the crystal Hamiltonian. If the eigenvalues and the wavefunctions at $k = 0$ are known, we can treat the term $[\frac{\hbar}{m_0}\,k.p]$ as a small perturbation.

1.2.2 The effective mass approximation for the conduction bands

For a bulk Si, the conduction band consists of six equivalent minima located symmetrically along the K_x (valleys Δ_x) , K_y (valleys Δ_y) and K_z (valleys Δ_z) directions at a distance $k_0 = 0.85\ (2\pi/a_0)$ from the corresponding $X-$point, where $a_0 = 0.54$ nm is the lattice constant of the relaxed lattice of silicon. Close to the minimum of the conduction band, the dispersion $E(k)$ can be described within a parabolic approximation [47]

$$E(k) = \frac{\hbar^2\left(k_x - k_{0,x}\right)^2}{2m_x} + \frac{\hbar^2\left(k_y - k_{0,y}\right)^2}{2m_y} + \frac{\hbar^2\left(k_z - k_{0,z}\right)^2}{2m_z} \tag{1.4}$$

Valleys	k_0	$m_x\ [m_0]$	$m_y[m_0]$	$m_z[m_0]$
Δ_x	$(\mp 0.85,0,0)$	m_l	m_t	m_t
Δ_y	$(0,\mp 0.85,0)$	m_t	m_l	m_t
Δ_z	$(0,0,\mp 0.85)$	m_t	m_t	m_l

Table 1 : Parameters used for the calculation of the conduction band structure with the effective mass approximation.

where the masses $m_l = 0.916\,m_0$ and $m_t = 0.19\,m_0$ are the longitudinal and transverse effective masses of silicon. To extend the validity of the purely parabolic dispersion to higher energy, an isotropic non parabolicity correction is introduced via the expression,

$$E(k)\left(1 + \alpha\,E(k)\right) = \frac{\hbar^2\left(k_x - k_{0,x}\right)^2}{2m_x} + \frac{\hbar^2\left(k_y - k_{0,y}\right)^2}{2m_y} + \frac{\hbar^2\left(k_z - k_{0,z}\right)^2}{2m_z}, \tag{1.5}$$

where $\alpha = 0.5\ \mathrm{eV}^{-1}$ is the non parabolicity parameter.

Equation 1.5 is the dispersion relation in the case of a three-dimensional (3D) electron gas. However, in an MOS transistor, the application of a gate bias can result in the formation of an inversion layer with significant quantization effects. Indeed, the electron energies are quantized in the confinement direction and the electrons occupy discrete subbands. Electrons are consequently free to move only in the plane perpendicular to the quantization direction forming a two-dimensional (2D) electrons gas. If we consider z as the quantization direction, in an inversion layer, the relation dispersion can be obtained from:

$$\mathrm{E(k)} = \varepsilon_{\mathrm{v,n}} + \frac{\hbar^2 (k_x)^2}{2m_x} + \frac{\hbar^2 \left(k_y\right)^2}{2m_y} \tag{1.6}$$

where $\varepsilon_{\mathrm{v,n}}$ are obtained by solving the Schrodinger equation

$$-\frac{\hbar^2}{2m_z}\frac{\partial^2 \psi_{v,n}}{\partial z^2} + U(z)\,\psi_{v,n} = \varepsilon_{\mathrm{v,n}}\,\psi_{v,n}, \tag{1.7}$$

with $U(z)$ the confining potential

The influence of axial strain components on the band structure is described using the linear deformation potential theory. Originally developed by Bardeen and Schockley [20] and generalized by Herring and Vogt [33], the theory relates the linear shift of the energy bands to small deformations of the crystal. For the Δz valley, the band shift is given by:

$$\delta \mathrm{E}_{\Delta \mathrm{z}} = \Xi_{\mathrm{d}}\left(\epsilon_{\mathrm{xx}} + \epsilon_{\mathrm{yy}} + \epsilon_{\mathrm{zz}}\right) + \Xi_{\mathrm{u}}\epsilon_{\mathrm{zz}} \tag{1.8}$$

Ξ_{d} and Ξ_{u} are the two deformation potentials relating the energy shift from axial stress and ϵ is the strain tensor. Shear stress components lead to reduction of the symmetry of the crystal affecting the lowest conduction band in three ways [35][47]: 1) The effective mass of the Δ_{z} valley changes; 2) the position of the Δ_{z} valley minima moves along the $\mathrm{K_z}$ –axis in the direction of the X-point and 3) it moves the Δ_{z} valleys with respect to Δ_{x} and Δ_{y} valleys. The two first points are not described in this manuscript, so the reader could refer to [35] or [47]. Concerning the band shift of the Δ_{z} valley, by considering shear strain components, the total band shift can be expressed as

$$\delta \mathrm{E}_{\Delta \mathrm{z}} = \Xi_{\mathrm{d}}\left(\epsilon_{\mathrm{xx}} + \epsilon_{\mathrm{yy}} + \epsilon_{\mathrm{zz}}\right) + \Xi_{\mathrm{u}}\epsilon_{\mathrm{zz}} + \Delta \mathrm{E}_{\Delta_{\mathrm{z}}}^{\mathrm{shear}}, \tag{1.9}$$

with $\Delta \mathrm{E}_{\Delta_{\mathrm{z}}}^{\mathrm{shear}} = -\frac{\Theta}{4\,\kappa^2}\,\epsilon_{\mathrm{xy}}^2$

Parameter	Value	Parameter	Value
Ξ_{u} [eV]	9.29	Θ [eV]	0.53
Ξ_{d}[eV]	1.1	κ	0.0189

Table 2 : Parameters for the conduction band structure calculation [47]

Similarly, the energy shifts for the Δx and Δy valleys can be written as

$$\delta \mathrm{E}_{\Delta \mathrm{x}} = \Xi_{\mathrm{d}}\left(\epsilon_{\mathrm{xx}} + \epsilon_{\mathrm{yy}} + \epsilon_{\mathrm{zz}}\right) + \Xi_{\mathrm{u}}\epsilon_{\mathrm{xx}} + \Delta \mathrm{E}_{\Delta_{\mathrm{x}}}^{\mathrm{shear}} \tag{1.10}$$

$$\delta \mathrm{E}_{\Delta \mathrm{y}} = \Xi_{\mathrm{d}}\left(\epsilon_{\mathrm{xx}} + \epsilon_{\mathrm{yy}} + \epsilon_{\mathrm{zz}}\right) + \Xi_{\mathrm{u}}\epsilon_{\mathrm{yy}} + \Delta \mathrm{E}_{\Delta_{\mathrm{y}}}^{\mathrm{shear}} \tag{1.11}$$

where $\Delta \mathrm{E}_{\Delta_{\mathrm{x}}}^{\mathrm{shear}} = -\frac{\Theta}{4\,\kappa^2}\,\epsilon_{\mathrm{yz}}^2$ and $\Delta \mathrm{E}_{\Delta_{\mathrm{y}}}^{\mathrm{shear}} = -\frac{\Theta}{4\,\kappa^2}\,\epsilon_{\mathrm{zx}}^2$

1.2.3 The 6-bands k.p model for the valence bands

As the effective-mass approximation is not accurate enough to calculate the valence band structure of silicon and germanium, the k.p method is commonly used. Typically, the three top valence bands are considered, namely the heavy hole (HH), the light hole (LH) and the split-off valence bands. Omitting the spin orbit interaction, the valence band can be described by a three-band effective Hamiltonian:

$$\mathrm{H}_{k.p}^{3\times3} = \begin{bmatrix} \frac{\hbar^2}{2m_0} + L\,k_x^2 + M(k_y^2 + k_z^2) & Nk_xk_y & N\,k_xk_z \\ N\,k_xk_y & \frac{\hbar^2}{2m_0} + L.k_y^2 + M.(k_x^2 + k_z^2) & N\,k_yk_z \\ N\,k_xk_z & N\,k_yk_z & \frac{\hbar^2}{2m_0} + L\,k_z^2 + M(k_x^2 + k_y^2) \end{bmatrix} \tag{1.12}$$

L, M and N are the band curvature parameters but other notations are commonly used such as the A, B, C parameters [15],

$$\mathrm{A} = \frac{1}{3}(\mathrm{L} + 2\mathrm{M})$$

$$\mathrm{B} = \frac{1}{3}(\mathrm{L} - \mathrm{M})$$

$$\mathrm{C}^2 = \frac{1}{3}[\mathrm{N}^2 - (\mathrm{L} - \mathrm{M})^2]$$

or the Luttinger parameters [16][6],

$$\gamma_1 = -\frac{1}{3}(\mathrm{L} + 2\mathrm{M})$$

$$\gamma_2 = -\frac{1}{6}(\mathrm{L} - \mathrm{M})$$

$$\gamma_3 = -\frac{1}{6}\mathrm{N}.$$

If we take into account the spin-orbit coupling, the resulting 6 × 6 k.p eigenvalue problem and the corresponding Hamiltonian matrix are the expressed as:

$$\mathrm{H}_{k.p}^{6\times6} = \begin{bmatrix} \mathrm{H}_{k.p}^{3\times3} & 0 \\ 0 & \mathrm{H}_{k.p}^{3\times3} \end{bmatrix} \tag{1.13}$$

The effect of spin-orbit coupling is considered by introducing an interaction term $\mathrm{H_{so}}$

$$\mathrm{H_{so}} = -\frac{\Delta}{3}\begin{pmatrix} 0 & \mathrm{i} & 0 & 0 & 0 & -1 \\ -\mathrm{i} & 0 & 0 & 0 & 0 & \mathrm{i} \\ 0 & 0 & 0 & 1 & -\mathrm{i} & 0 \\ 0 & 0 & 1 & 0 & -\mathrm{i} & 0 \\ 0 & 0 & \mathrm{i} & \mathrm{i} & 0 & 0 \\ -1 & -\mathrm{i} & 0 & 0 & 0 & 0 \end{pmatrix} \tag{1.14}$$

The total k.p Hamiltonian for non-stressed Si or Ge valence bands ($\mathrm{H}_{k.p}^{6\times6}$) including spin-orbit interaction is depending on $\gamma_1, \gamma_2 and\ \gamma_3$ Luttinger parameters as [17]:

$$H_{k.p}^{6\times6} = -\begin{pmatrix} P+Q & -S & R & 0 & -\frac{S}{\sqrt{2}} & \sqrt{2}R \\ -S & P-Q & 0 & R & -\sqrt{2}Q & \sqrt{\frac{3}{2}}S \\ R & 0 & P-Q & S & \sqrt{\frac{3}{2}}S & \sqrt{2}Q \\ 0 & R & S & P+Q & -\sqrt{2}R & -\frac{S}{\sqrt{2}} \\ -\frac{S}{\sqrt{2}} & -\sqrt{2}Q & \sqrt{\frac{3}{2}}S & -\sqrt{2}R & P+\Delta & 0 \\ \sqrt{2}R & \sqrt{\frac{3}{2}}S & \sqrt{2}Q & -\frac{S}{\sqrt{2}} & 0 & P+\Delta \end{pmatrix} \quad (1.15)$$

with

$$\begin{cases} P(k) = \frac{k^2}{3}\left[(L+2M) + \frac{3\hbar^2}{2m_0}\right] \\ Q(k) = \frac{1}{6}\left[(L-M)\left(k_x^2 + k_y^2 - 2k_z^2\right)\right] \\ R(k) = -\frac{1}{2\sqrt{3}}\left[(M-L)\left(k_x^2 - k_y^2\right) + i2Nk_xk_y\right] \\ S(k) = -\frac{N}{\sqrt{3}}(k_x - ik_y)k_z \end{cases} \quad (1.16)$$

Δ is the spin-orbit split-off energy.

Strain induced wrapping and splitting of SiGe bands can be calculated within the k.p model. The strain dependent perturbation Hamiltonian δH_s can be written as [17]:

$$\delta H_s = \begin{bmatrix} \delta h_s & 0 \\ 0 & \delta h_s \end{bmatrix} \quad (1.17)$$

where

$$\delta h_s = \begin{bmatrix} l.\epsilon_{xx} + m.(\epsilon_{yy} + \epsilon_{zz}) & n.\epsilon_{xy} & n.\epsilon_{xz} \\ n.\epsilon_{xy} & l.\epsilon_{yy} + m.(\epsilon_{xx} + \epsilon_{zz}) & n.\epsilon_{yz} \\ n.\epsilon_{xz} & n.\epsilon_{yz} & l.\epsilon_{zz} + m.(\epsilon_{xx} + \epsilon_{yy}) \end{bmatrix} \quad (1.18)$$

The three terms l, m and n are the valence band deformation potentials:

$$\begin{cases} l = a_v + 2b_v \\ m = a_v - b_v \\ n = 2\sqrt{3d} \end{cases} \quad (1.19)$$

$a_v, b_v \; and \; d$ are the Bir-Pikus deformation potentials.

The total 6×6 Hamiltonian of the valence band in strained Si or Ge can be expressed as:

$$H_{6k.p}^{s} = H_{k.p}^{6\times6} + H_{so} + \delta H_s \quad (1.20)$$

In inversion layer, considering z as the quantization direction, the three-band effective Hamiltonian (equation 1.12) becomes the operator [47]:

$$H_{k.p}^{3\times3} = \begin{bmatrix} \frac{\hbar^2}{2m_0} + L\,k_x^2 + M\,k_y^2 - M\frac{\partial^2}{\partial z^2} & Nk_xk_y & -iNk_x\frac{\partial}{\partial_z} \\ Nk_xk_y & \frac{\hbar^2}{2m_0} + L\,k_y^2 + M\,k_x^2 - M\frac{\partial^2}{\partial z^2} & -iNk_y\frac{\partial}{\partial_z} \\ -iNk_x\frac{\partial}{\partial_z} & -iNk_y\frac{\partial}{\partial_z} & \frac{\hbar^2}{2m_0} + -L\frac{\partial^2}{\partial z^2} + M\,k_x^2 + M\,k_y^2 \end{bmatrix} \quad (1.21)$$

The 6-bands k.p model can be used to model the valence band structure of the most widely used semiconductors, such as silicon, germanium, and $Si_{1-x}Ge_x$ alloys, which have a diamond crystal lattice. Therefore, the band parameters L, M, N, the spin-orbit splitting E_{so} and strain parameters l, m, n have to be determined for each material. One way to determine them is through measurement using cyclotron resonance measurements as done in [15]. Alternatively, the values can be obtained from other theoretical calculations based on other models, such as non-local EPM [18], or first principles calculations. Table 3 gives a list of parameters for the 6-bands k.p model for Si and Ge at room temperature.

Silicon	Si [14] / [12]	Ge [14]
L	-5.53 / -5.53	-30.44
M	-3.63 / -3.64	-4.73
N	-8.32 / -8.32	-33.93
Δ	0.044/0.044	0.29
a_v	2.46	1.24
b_v	-2.1	-2.9
d	-4.8	-5.3

Table 3 : Values of the Luttinger parameters $\boldsymbol{\gamma_1, \gamma_2 and\ \gamma_3}$ used in our simulations for silicon and germanium

1.2.4 Parameters for SiGe channel

To obtain the valence band parameters for a $Si_{1-x}Ge_x$ alloy as function of Ge content x_{Ge}, some kind of interpolation needs to be applied. Many authors have used a linear interpolation between silicon and germanium parameters [12]. However, it has been shown in [13] and [14] that the parameters L and N show a strong non linearity with $x_{Ge.}$ In Figure 5, we have plotted the dependence of the coefficients L, M and N with $x_{Ge,}$ extracted from literature. In this thesis, parameters from [13] have been used to simulate the band structure of $Si_{1-x}Ge_x$ alloy.

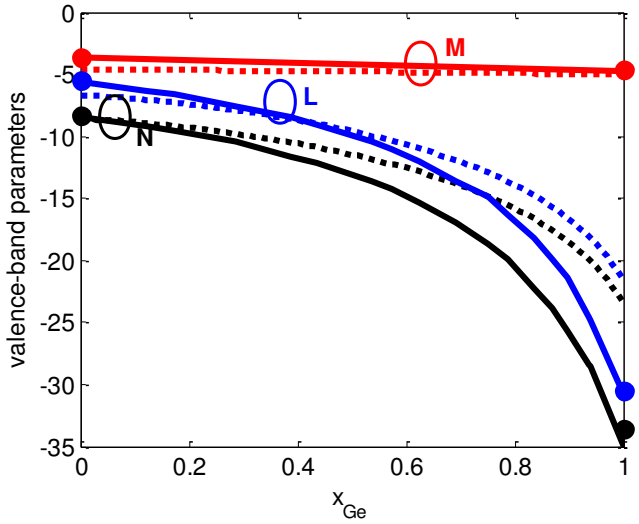

Figure 5 : Valence band parameters for $Si_{1-x}Ge_x$ alloy used in literature. Full lines are extracted from [14], dotted lines from [13] and symbols from [12] (linear interpolation).

I.3 Transport models

Simulation of carrier transport in semiconductor devices should, in principle, account for both the wave-like and the particle-like properties demanded by quantum mechanics [19]. The simulation of carrier transport in semiconductor is usually based on a semi-classical approach in which each carrier is assumed to behave like a classical electrically charged particle reacting to the electric field in accordance to the Newton's law. However, benefiting from recent advances in numerical methods and algorithms, quantum methods, such as NEGF are more and more used to study transport in advanced devices. In this section we reviewed the main approaches to model transport in semiconductor technology ranging from the classical drift diffusion approach to the NEGF method.

I.3.1 Semiclassical models

The fundamental semi-classical equation for modeling the carrier transport in semiconductor is the Boltzmann Transport Equation (BTE). The BTE describes the evolution of the distribution function $\mathrm{f}(\mathrm{r},\mathrm{k},\mathrm{t})$ in the real space, the momentum space and with time

$$\frac{\partial \mathrm{f}}{\partial \mathrm{t}} + v.\nabla_r f + \frac{E}{\hbar}.\nabla_k f = \left.\frac{\partial \mathrm{f}}{\partial \mathrm{t}}\right|_{Scatt} + s(r,k,t) \tag{1.22}$$

Here, $v = \nabla_k E(k)$ is the carrier velocity.

The first left-hand term represents the variation of the distribution function with time. The second term describes the displacement from equilibrium of the distribution function due to variations in real space. The third term is caused by the variations in momentum space due to external force F. The right term is composed of the variation due to scatterings (collision term) and by the generation recombination term s(r, p, t).

The collision term is a competition between two processes: 1) carriers with a wave vector k' can be scattered to k with a transition rate $S(k',k)$ increasing $\mathrm{f}(\mathrm{r},\mathrm{k},\mathrm{t})$; 2) carriers with a wave vector k can be scattered to k' with a transition rate $S(k,k')$ decreasing $\mathrm{f}(\mathrm{r},\mathrm{k},\mathrm{t})$:

$$\left.\frac{\partial \mathrm{f}}{\partial \mathrm{t}}\right|_{Scatt} = \int f(k',t)\big(1-f(k,t)\big)S(k',k)dk' - \int f(k,t)\big(1-f(k',t)\big)S(k,k')dk' \quad (1.23)$$

The BTE is based on some approximations and has intrinsic limitations [93]:

1. It is a single particle description of a many particle system of carriers, so the correlation between carriers is not treated;
2. carriers are considered as classical particles obeying to Newton's law;
3. scattering events are binary collisions occurring instantly in time, and localized in space;
4. BTE comes from a statistical approach, such a statistical description is valid when the number of the carriers is very large.

- **Relaxation time approximation (RTA)**

At low field, the collision term $\left.\frac{\partial \mathrm{f}}{\partial \mathrm{t}}\right|_{Scatt}$ can be simplified using the relaxation-time approximation that implies quasi-equilibrium condition and elastic or isotropic scattering mechanisms [93]:

$$\left.\frac{\partial \mathrm{f}}{\partial \mathrm{t}}\right|_{Scatt} = -\frac{f_i(k) - f_0(E_i(k))}{\tau(k)} \quad (1.24)$$

where f_0 is the equilibrium Fermi-Dirac distribution function and $\tau(k)$ represents a suitable average over energy of the relaxation time for the distribution function, determined by the rates of all the relevant scattering mechanisms involved [47]. A general definition for $\tau(k)$ can be written as [47]:

$$\frac{1}{\tau_i(k)} = \sum_{j,k'} S(k,k')\left[\frac{1-f_0(E_j(k'))}{1-f_0(E_i(k))}\right]\left[1-\frac{\tau(k')}{\tau(k)}\frac{v(k')}{v(k)}\right] \quad (1.25)$$

- **The Kubo-Greenwood formalism**

The Kubo-Greenwood formalism derived from the linearized Boltzmann transport equation in the presence of a uniform electric field along the transport direction within the relaxation time approximation [47]:

$$\mu_{ij}^{v} = \frac{e}{\hbar^2}\frac{1}{k_B}\frac{g_v}{TN_v}\int \frac{dk}{(2\pi)^2}\,\tau_{ij}^{v}\,\frac{\partial E_v}{\partial k_i}\,\frac{\partial E_v}{\partial k_j}\,f_0(E_v)[1-f_0(E_v)] \quad (1.26)$$

g_v is the degeneracy, N_v is the subband carrier density, τ_{ij}^{v} is the total momentum relaxation time for the subband v in directions (i,j), E_v, is the subband energy dispersion. This expression is widely used in the literature [34] [40] to evaluate the low field mobility in semiconductor devices.

- **Drift diffusion equations**

Assuming RTA simplifications, and assuming also that there is no temperature gradient in the devices and a weak carrier heating, the BTE reduces to the drift-diffusion equation (DD) using the methods of moments [21][22]. In this model, the hole and electron current densities are expressed as a combination of two components. The drift component is driven by the electric field and the diffusion component by the carrier density gradient:

$$\overrightarrow{J_n}(r,t) = |q|n(r,t)\mu_n\vec{E} + |q|D_n\vec{\nabla}n(r,t)$$
$$\overrightarrow{J_p}(r,t) = |q|p(r,t)\mu_p\vec{E} - |q|D_p\vec{\nabla}p(r,t) \quad (1.27)$$
$$D_n = \frac{kT}{|q|}\mu_n \, , D_p = \frac{kT}{|q|}\mu_p$$

D_n and D_p are the diffusivity coefficients of the electron or hole gas given by the Einstein relation.

As previously said, to support technology development, the drift diffusion model is still routinely used in industry due to its simplicity and efficiency. However, low-field mobility models are empirical and depend on a series of unknown parameters that have to be calibrated on advanced solvers. This point will be addressed in this manuscript. An extension of the drift diffusion model to high-field regime is generally realized by including a velocity saturation model [23], although controversial. Moreover, extensions have been developed taking into account higher moments of the BTE [24] [25] [26] [27] but it is not trivial to evaluate the advantage and drawback of each of them.

- **The Monte-Carlo method**

The Monte Carlo method, as applied to the charge transport in semiconductors, is a statistical numerical method for solving the semi-classical BTE. It consists in simulating the motion of particles in phase space either one by one (single particle MC) or as an ensemble (ensemble particle MC). This method was first used to study bulk material by Jacoboni and Reggiani [28] in 1983 and applied to devices about one decade later [29][30]. Several improvements to Monte Carlo device simulation technique have been introduced in the last 20 years, e.g. numerical description of the full band dispersion relationship [29], implementation of the self-consistency with the Poisson equation, simulation of "hot electron" phenomena (impact ionization, injection in the gate dielectric, etc.).

The Monte Carlo method is based on the generation of random numbers, which are used to determine in aleatory way free flights duration and to choose the states after the scattering. During the motion of a carrier the following fundamental steps are performed (Figure 6) [31]:

1. Scattering rates are evaluated; in order to know how often free flights have to be interrupted;
2. Free flight duration is determined in a random way;
3. Carrier motion starts, following classical laws of motion;
4. The free flight is interrupted by a scattering event. The scattering mechanism responsible for the free flight stop is chosen in an aleatory way, based on the scattering rate of the individual mechanism for that carrier state;
5. Once the scattering mechanism is known, the particle state is chosen in an aleatory way, i.e. the final momentum is finally established.

These steps are repeated until the end of the time step is reached, when a new guess for the population of the phase state is determined.

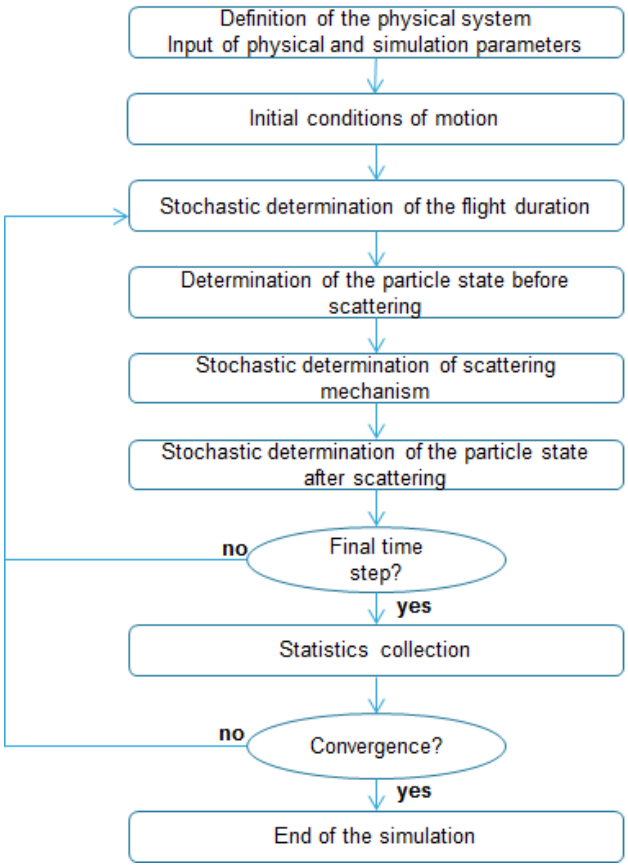

Figure 6 : Flowchart of a typical Monte Carlo program.

During my thesis, two different MC solvers have been used: 1) the multi-subband Monte Carlo (MSMC) solver from the University of Udine and 2) the commercial single particle MC solver from SYNOPSYS (SPARTA) [66].

The MSMC tool solves the multi-subband BTE by coupling four main steps [43] (Figure 7). The two dimensional structure is sliced in sections along the transport direction and in each section the 1D Schrödinger equation is solved to obtain the subband energies and wavefunctions (step 1). The scattering rates are then computed (step 2) and are used in the MC transport algorithm (step 3). A new potential profile is then computed by solving the 2D Poisson equation (step 4). These four steps are looped until convergence is reached.

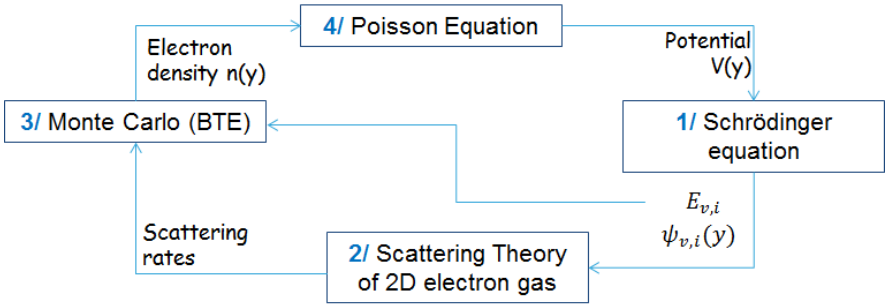

Figure 7 : Overall flowchart of the MSMC solver

The solver includes scattering with phonons [47], surface roughness (GPN model) [46], Coulomb and alloy scattering mechanisms (ionized impurities and remote Coulomb) [47].

However, to perform 1D simulations, only one slice (taken in the middle of the channel) with a low constant lateral field (E=1 kV/cm) is simulated and cyclic boundary conditions are applied to the MC solver. These conditions emulate an infinitely long device with stationary conditions along the channel.

I.3.2 Quantum model

There are a lot of books and publications dealing with the NEGF method, so the reader could refer to [32]. In this part, we provide a description of the method to calculate the effective mobility from NEGF simulations. The modeling of long channel transistor with NEGF is not straightforward [38]. Indeed, NEGF simulations require two reservoirs at equilibrium to emulate the source and the drain, so cyclic boundary conditions are not applicable. The method used during this thesis to calculate the mobility using NEGF calculations is discussed below.
In general, the low-field resistance of a channel with length L can be written as:

$$R(L) = \frac{V}{I} = R_c + R_0 + \frac{L}{n_{1d}\mu q}, \tag{1.28}$$

where V is the drain-source voltage, I is the current, n_{1d} is the carrier density per unit length, μ is the carrier mobility and q the charge. The term R_c is a contact resistance and R_0 is the ballistic resistance. Two techniques are generally used in the literature [32] to extract the low-field mobility with a NEGF code. 1) the ballistic resistance R_0 can be obtained independently from a purely "ballistic calculation (no scattering), and the mobility extracted from the data for a single length L using equation 1.28. This presumes that R_c is negligible and that the length L of the channel is well known. 2) The current can be computed in channels with various lengths L, then, $R_c + R_0$ and μ can be extracted from the $R(L)$ data. However, this method can be very noisy since different L usually correspond to different realizations of the disorders. An accurate extraction of the mobility requires averages over large numbers of samples. Moreover, in a disordered channel, the carrier density is intrinsically non uniform, hence not univocally defined. In this section, the newly developed methodology to extract the mobility from NEGF calculation (presented in [38]) is briefly summarized hereafter. This technique is developed in the view of reducing limitations coming from the contact resistance contamination, from the channel length misestimates, with minimal needs for ensemble averages and a well-defined prescription for the density. In this method, either SR or RC-limited mobility is obtained by means of geometrical fluctuations of the SiO_2/Si front and back interfaces and the inclusion of random Coulombic centers.

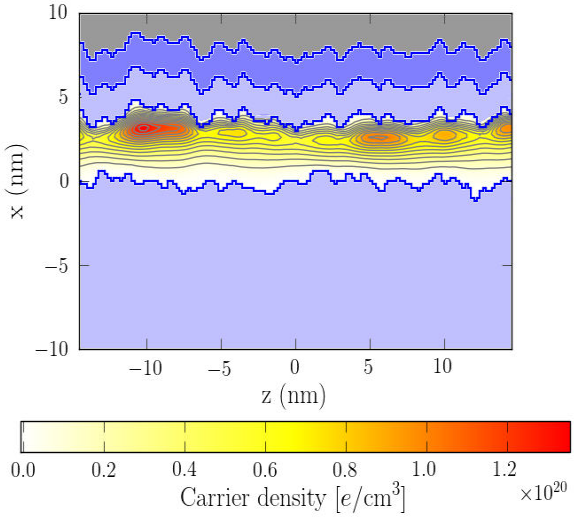

Figure 8 : Carrier density with NEGF in a 4 nm thick FDSOI film. Interface roughness generated with an *exponential autocorrelation function (Δ=0.47 nm and Λ=1.3 nm).*

Random samples of disorder with width W = 20 nm and length L = 30 nm are generated and then, we built devices made of these units repeated once, twice (L = 60 nm), and up to three times (L = 90 nm). Note that the samples are longer than the mean free path and much longer than the correlation length of the disorder. We next computed the resistance of the devices in a mode space approach [94], including electron-phonon scattering. As expected, in a long channel device (Figure 9) the resistance of the devices is proportional to their length, in agreement with equation 1.28.

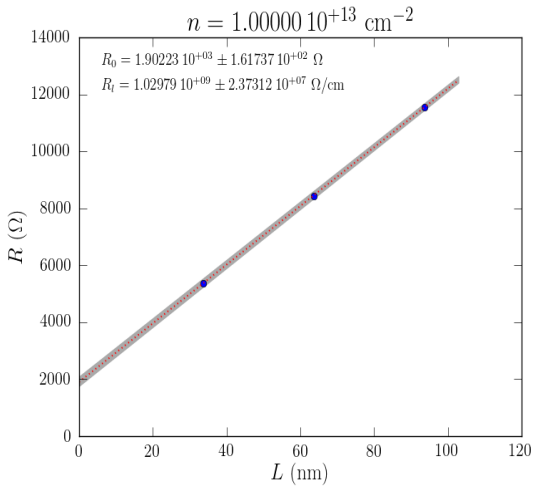

Figure 9 : NEGF resistance of the FDSOI film as a function of length. The slope gives the mobility, while the *intercept at L=0 is the quantum "ballistic" resis*tance.

I.4 Physics-based modeling of scattering mechanisms

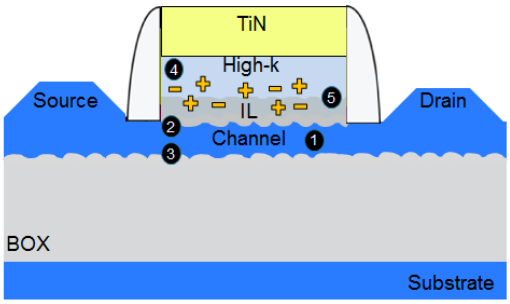

Figure 10 : Cross-section of a FDSOI MOSFET illustrating scattering mechanisms responsible of the mobility degradation: 1) is scattering with phonons, 2) and 3) are surface roughness scattering at the front and back interface, 4) is remote Coulomb scattering due to the presence of charge in the gate stack and 5) is remote surface roughness scattering.

In undoped-channel FDSOI devices, scattering with phonons and with the asperities of the silicon/IL interface are the main mechanisms limiting the carrier mobility. They are strongly dependent on the channel thickness (T_{SI}) [39] and on the voltage applied on the front and the back gate [39] [40]. However, at low effective field, other scattering mechanisms can affect the carrier mobility. Indeed, in devices featuring high-k dielectrics, strong degradations of the mobility have been reported in the literature compared to the universal curves [71] [72]. This mobility degradation has been ascribed to a very rough high-k/channel interface and has been limited by introducing a SiO_2 interfacial layer (IL) between the channel and the high-k. However, the mobility degradation still strongly depends on the thickness of the IL. Several scattering mechanisms can be responsible of the mobility degradation: remote Coulomb (charges in the gate stack) [76] [86] [87] [88], remote phonon [89] and remote surface roughness scatterings due to the rugosity of the high-k/IL interface [90]. However, as remote phonon and remote surface roughness scatterings are not significant for IL EOT > 1 nm [88] [90], it is not accounted for in all simulations in this manuscript. Consequently, we consider that the degradation of the mobility with the IL thickness is mainly due to remote coulomb scattering. In this section, the method used in semiclassical solvers to calculate scattering rates in a 2D electron gas is summarized.

I.4.1 Scattering in a 2D electron gas

The approach is based on Fermi's Golden rule [93] that relates the matrix elements $\left|M_{n,n'}(K,K')\right|$ to the transition rate $S_{n,n'}(k,k')$:

$$S_{n,n'}(k,k') = \frac{2\pi}{\hbar}\left|M_{n,n'}(k,k')\right|^2 \delta[E_{B,n}(k) - E_{B,n'}(k') \mp \Delta E] \tag{1.29}$$

The transition rate $S_{n,n'}(k,k')$ is the probability per unit of time for a carrier to scatter from state k to state k' with initial energy E and final energy $E' = E \mp \Delta E$. Let us discuss in detail the matrix elements for each scattering mechanisms.

I.4.2 Phonons scattering

- **Acoustic phonon scattering:**

Acoustic intravalley phonons scattering were treated as an elastic isotropic process within the energy equipartion approximation:

$$\left|M^{ac}_{v,nn'}\right|^2 = \frac{k_B T}{(v_l^{Si})^2\,\rho^{Si}} \left(D^{Si}_{ac}\right)^2 F_{v,n;v,n'} \tag{1.30}$$

Note that the matrix element for a SiGe layer is given by [100]:

$$\left|M^{ac}_{v,nn'}\right|^2 = \left\{(1-x_{Ge})\frac{k_B T}{(v_l^{Si})^2\,\rho^{Si}} \left(D^{Si}_{ac}\right)^2 + x_{Ge}\,\frac{k_B T}{(v_l^{Ge})^2\,\rho^{Ge}} \left(D^{Ge}_{ac}\right)^2\right\} F_{v,n;v,n'} \tag{1.31}$$

Where D^{Si}_{ac} and D^{Ge}_{ac} are the acoustic deformation potentials for silicon and germanium respectively, k_B is the Boltzmann constant, T is the lattice temperature, v_l^{Si} and v_l^{Ge} are the longitudinal sound velocity and ρ^{Si} and ρ^{Ge} are the semiconductor density. $F_{v,n;v,n'}$ is the form factor between the initial and the final subbands and is given by:

$$F_{v,n;v,n'} = \int_0^{\infty} \left|\psi_{v,n}(y)\right|^2 \left|\psi_{v',n'}(y)\right|^2 dz \tag{1.32}$$

- **Intervalley phonon scattering**

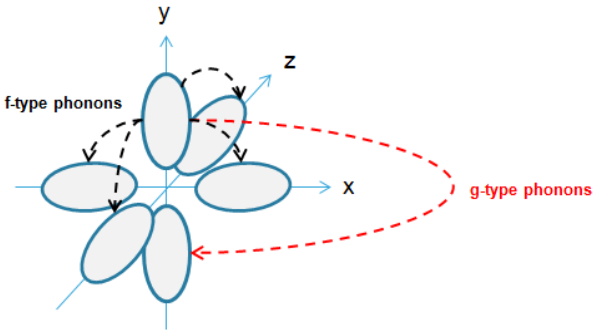

Figure 11 : Silicon intervalley phonons type: g-*type phonon goes in the opposite Δ valley with the same* orientation; f-*type phonon that scatters from one Δ valley to one of the four Δ valleys with different orientation.*

Intervalley transitions assisted by optical phonons were included by accounting for f- and g-type processes. Also in this case the scattering is isotropic, but not elastic [47] [100]. The matrix element is

$$\left|M^{opt}_{v,v';nn'}\right|^2 = \left\{(1-x_{Ge})\left|M^{Si}_{v,v';nn'}\right|^2 + x_{Ge}\left|M^{Ge}_{v,v';nn'}\right|^2\right\} F_{v,n;v,n'} \tag{1.33}$$

where

$$\begin{aligned}
\left|M^{Si}_{v,v';nn'}\right|^2 &= \frac{\hbar^2\pi\left(DtK^{Si}\right)^2}{2\rho^{Si}\hbar\omega^{Si}} \left[N\left(\hbar\omega^{Si}\right) + \frac{1}{2} \mp \frac{1}{2}\right] \delta\left(E_v(k) - E_{v'}(k') \pm \hbar\omega^{Si}\right) \\
\left|M^{Ge}_{v,v';nn'}\right|^2 &= \frac{\hbar^2\pi(DtK^{Ge})^2}{2\rho^{Ge}\hbar\omega^{Ge}} \left[N(\hbar\omega^{Ge}) + \frac{1}{2} \mp \frac{1}{2}\right] \delta\left(E_v(k) - E_{v'}(k') \pm \hbar\omega^{Ge}\right)
\end{aligned} \tag{1.34}$$

where $N(\hbar\omega) = 1/(e^{\frac{\hbar\omega}{k_B T}} - 1)$ is the phonon occupancy, DtK and ω are the deformation potential and the angular frequency listed in Table 7 for three f-type and three g-type optical phonon modes. In this notation, the upper and lower signs correspond to phonon absorption and phonon emission, respectively. This phonon scattering model, originally developed for bulk silicon simulations, is adapted to transport in inversion layer by tuning the model coefficients [28];

I.4.3 Surface roughness scattering

Interaction of carriers with the asperities of the interface between the semiconductor and the oxides is one of the main mechanism responsible of the mobility degradation in MOSFETs. This scattering is particularly dominant at high effective fields or inversion densities and is strongly dependent on the channel thickness [39]. The two main sources of scattering affecting the charge carrier's motion are 1/ the fluctuation of wavefunction due to asperities at the interface and 2/ the fluctuation of the potential energy (modification of the charge carrier densities and the image potential). The most dominant scattering source is due to the perturbations in wavefunctions [34] [56] and this term is commonly described by the Prange-Nee (PN) [45], the generalized Prange-Nee model [34] [46] or more recently using the new approach described by Lizzit et al. [54]. In the description below, SR is treated as an elastic and anisotropic process.

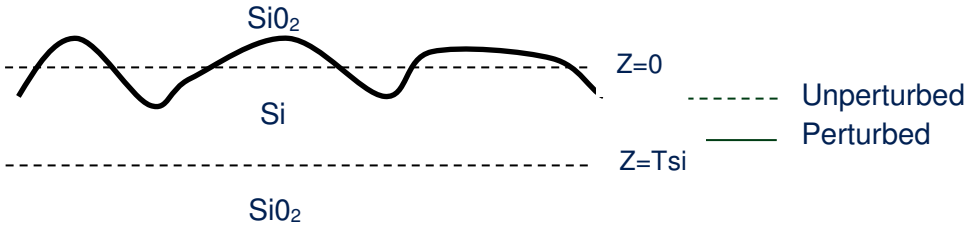

Figure 12 : Schematic of the Surface roughness at the semiconductor-oxide interface.

The general definitions of the matrix elements are [67]:

$$\mathrm{M}'_{\mathrm{nn}'}[\Delta(\mathrm{r})] = \int_{\mathrm{z}} \psi^{*}_{\mathrm{n}'}(\mathrm{z})[(\widehat{\mathrm{H}}_{\mathrm{P,r}} - \widehat{\mathrm{H}}_{0})\psi_{\mathrm{n}}(\mathrm{z})]\mathrm{dz} \tag{1.35}$$

and

$$\mathrm{M}'_{\mathrm{nn}}(\mathrm{q}) = \int_{\mathrm{A}} \mathrm{M}'_{\mathrm{nn}'}[\Delta(\mathrm{r})]\ \frac{\exp(-\mathrm{iq.r})}{\mathrm{A}}\ \mathrm{dr} \tag{1.36}$$

In the following equations, the SR at the two interfaces is considered as uncorrelated. The unperturbed $\widehat{\mathrm{H}}_0$ and the perturbed $\widehat{\mathrm{H}}_{\mathrm{P,r}}$ Hamiltonian of the SOI structure can be described as [47]:

$$\widehat{\mathrm{H}}_{0} = -\frac{\hbar^2}{2\mathrm{m}_{\mathrm{z}}(\mathrm{z})}\frac{\mathrm{d}^2}{\mathrm{d}_{\mathrm{z}}{}^2} - \mathrm{e}\phi(\mathrm{z}) + \phi_{\mathrm{B}}\mathrm{H}_{\nu}(-\mathrm{z}) + \phi_{\mathrm{B}}\mathrm{H}_{\nu}(\mathrm{z} - \mathrm{Tsi}) \tag{1.37}$$

$$\widehat{\mathrm{H}}_{\mathrm{P,r}} = -\frac{\hbar^2}{2\mathrm{m}_{\mathrm{z}}(\mathrm{z}')}\frac{\mathrm{d}^2}{\mathrm{d}_{\mathrm{z}}{}^2} - \mathrm{e}\phi(\mathrm{z}) + \phi_{\mathrm{B}}\mathrm{H}_{\nu}(-\mathrm{z} + \Delta(\mathrm{r})) + \phi_{\mathrm{B}}\mathrm{H}_{\nu}(\mathrm{z} - \mathrm{Tsi}) \tag{1.38}$$

with ϕ_{B} the potential energy barrier at the channel/dielectric interface, $\phi(\mathrm{z})$ the electrostatic potential and $\mathrm{H}_{\nu}(x)$ the step function.

- **Generalized Prange-Nee model:**

The matrix element reflecting the fluctuation of the wavefunction is still often expressed using the generalized Prange-Nee model. Contrary to the initial Prange-Nee model [45], it takes into account the wavefunction penetration into the oxide (open boundary).

Introducing the abscissa z' defined by:

$$z' = \frac{Tsi\,(z - \Delta(r))}{Tsi - \Delta(r)}, \tag{1.39}$$

and assuming that $\Delta(r)$ is small enough that the electrostatic potential can be linearized ($\phi(z) = \phi(z') + \Delta(r)\,\frac{d\phi(z')}{dz'}$, the unperturbed Hamiltonian can be expressed as

$$\hat{H}_{P,r} = \hat{H}_{0,z'} - \frac{\Delta(r)}{Tsi}\left(\hbar^2 \frac{d}{dz'}\frac{1}{m_z(z')}\frac{d}{dz'} - e\,z'\frac{d\phi(z')}{dz'}\right) - e\Delta(r)\frac{d\phi(z')}{dz'} \tag{1.40}$$

By keeping only the first order terms in $\Delta(r)$, we can obtain

$$\begin{aligned} M_{nn'}[\Delta(r)] = {} & \Delta(r)\left[-\int \psi_n e\frac{\partial\phi}{\partial z}\psi_{n'}dz + (\epsilon_n - \epsilon'_n)\int \psi_n \frac{\partial\psi_{n'}}{\partial z}dz\right] \\ & - \frac{\Delta(r)}{Tsi}\left[\int \psi_n \left(\hbar^2 \frac{\partial}{\partial z}\frac{1}{m_z(z)}\frac{\partial}{\partial z} - ze\frac{\partial\phi}{\partial z}\right)\psi_{n'}\,dz + (\epsilon_n \right. \\ & \left. - \epsilon_{n'})\int \psi_n z\frac{\partial\psi_{n'}}{\partial z}dz\right] \end{aligned} \tag{1.41}$$

In this expression, due to the assumptions introduced during the derivation of this model, the matrix elements $M'_{nn}[\Delta(r)]$ are directly proportional to $\Delta(r)$.

Using equation 1.36 and 1.41, we can express $M'_{nn}(q)$ as:

$$\begin{aligned} M'_{nn}(q) = \frac{1}{A}\int_A \Delta(r)\exp(-iq.r)\,dr\,.\Bigg[& \int \psi_n e\frac{d\phi}{dz}\psi_{n'}dz + (\epsilon_n - \epsilon'_n)\int \psi_n \frac{d\psi_{n'}}{dz}dz \\ & - \frac{1}{Tsi}\int\left[\psi_n\left(\hbar^2\frac{d}{dz}\frac{1}{m_z(z)}\frac{d}{dz} - ze\frac{d\phi}{dz}\right)\psi_{n'}\right]dz \\ & - \frac{1}{Tsi}(\epsilon_n - \epsilon_{n'})\int \psi_n z\frac{d\psi_{n'}}{dz}dz\Bigg] \end{aligned} \tag{1.42}$$

If we define $\mathfrak{M}_{nn'}$ as the term inside the square bracket:

$$\begin{aligned} \mathfrak{M}_{nn'} = {} & \int \psi_n e\frac{d\phi}{dz}\psi_{n'}dz + (\epsilon_n - \epsilon'_n)\int \psi_n \frac{d\psi_{n'}}{dz}dz - \frac{1}{Tsi}\int\left[\psi_n\left(\hbar^2\frac{d}{dz}\frac{1}{m_z(z)}\frac{d}{dz} - \right.\right. \\ & \left.\left. ze\frac{d\phi}{dz}\right)\psi_{n'}\right]dz - \frac{1}{Tsi}(\epsilon_n - \epsilon_{n'})\int \psi_n z\frac{d\psi_{n'}}{dz}dz\,, \end{aligned} \tag{1.43}$$

we can obtain the following expression:

$$\left|M'_{nn'}(q)\right|^2 = |\,\mathfrak{M}_{nn'}|^2 * \frac{S_R(q)}{A}, \tag{1.44}$$

where the spectrum of the surface roughness $S_R(q)$ is defined as:

$$S_R(q) = \frac{1}{A}\int_A |\Delta(r)\exp(-iq.r)\,dr|^2 \tag{1.45}$$

Two different models for $S_R(q)$ are commonly used in literature [53]:

- The Gaussian model:

$$S_R(q) = \pi\Delta^2\Lambda^2\exp(-q^2\Lambda^2/4) \tag{1.46}$$

- The Exponential model:

$$S_R(q) = \frac{\pi\Delta^2\Lambda^2}{\left[1+\frac{q^2\Lambda^2}{2}\right]^{\beta}} \tag{1.47}$$

Δ is the Root Mean Square (RMS) amplitude and Λ is the correlation length.

The GPN model is actually often used in advanced transport solvers such as MSMC [47] and KG [39] [40] solvers. One major drawback is that, to fit experimental data, the model requires to use high values of Δ and Λ compared to values measured by AFM or STM for Si/SiO_2 interfaces (Table 4).

Δ and Λ extracted from AFM and TEM measurements on Si-$Si0_2$ interface			
	Δ	Λ	Spectrum
O. Bonno et al. [48]	0.18	$\simeq$4.1	Exponential
A. Pirovano et al. [49]	0.18	1.8	Gaussian
T. Yamanaka [50]	0.21	-	-

Δ and Λ used to fit experimental mobility measurements using GPN			
	Δ	Λ	Spectrum
M. V. Fischetti [51]	0.48	1.3	Exponential
D. Esseni et al. [47]	0.62	1.0	Gaussian
O. Nier et al. [52]	0.62	1.3	Exponential

Table 4 : Comparison of SR spectrum parameters Δ and Λ measured by AFM or TEM with those used in the simulation (GPN model) to fit experimental mobility values.

- **Newly developed model by Lizzit et al. [54]:**

Lizzit et al. have recently proposed an alternative model to the GPN. The SR matrix elements by directly replacing equation 1.37 and 1.38 into equation 1.35:

$$M'_{nn}[\Delta(r)] = \mathrm{sign}(\Delta)\int_{z_{min}}^{z_{max}} \psi^*_{n'}(z)\left[\left(-\frac{\hbar}{2m_{ox}}+\frac{\hbar}{2m_{sc}}\right)\frac{d^2\psi_n(z)}{dz^2}+\phi_B\psi_n(z)\right]dz \tag{1.48}$$

Contrary to equation 1.41, in this new formulation, no approximation is made on the $\Delta(r)$ dependency of $M'_{nn}[\Delta(r)]$. To express $|M'_{nn}(q)|^2$, we must then calculate the power spectrum of $|M'_{nn}[\Delta(r)]|^2$.

Using [55] and assuming that $\Delta(r)$ has a Gaussian distribution function, Lizzit et al. have expressed the auto-correlation of $M'_{nn}[\Delta(r)]$ as:

$$C_{M_{nn'}} = \frac{1}{2\pi C_{\Delta}(0)\sqrt{1 - C^2_{\Delta,N}(r)}} \int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty} M_{nn'}[\Delta_1]\ M_{nn'}[\Delta_2] \exp\left[-\frac{\Delta_1^2 + \Delta_2^2 - 2C^2_{\Delta,N}(r)\Delta_1\Delta_2}{2C_{\Delta}(0)(1 - C^2_{\Delta,N}(r))}\right] d\Delta_1\, d\Delta_2 \qquad (1.49)$$

The square matrix element $|M'_{nn}(q)|^2$ is then given by:

$$|M'_{nn}(q)|^2 = \frac{1}{A}\int_0^{+\infty} C_{M_{nn'}}(r)[2\pi J_0(qr)]r\, dr \qquad (1.50)$$

I.3.2.a: Fluctuation of the potential energy:

In previous sections, matrix elements accounting for the fluctuation of the wavefunction due to asperities at the interface are discussed. This is the dominant SR scattering source affecting the carrier motion [34] [56] but other terms accounting for the fluctuation of the potential energy (density fluctuation and image charge effect) can be accounted for as done by S. Jin et al [34]. Mobility simulations of [34] will be discussed in section II.2.3.

I.4.4 Coulomb scattering

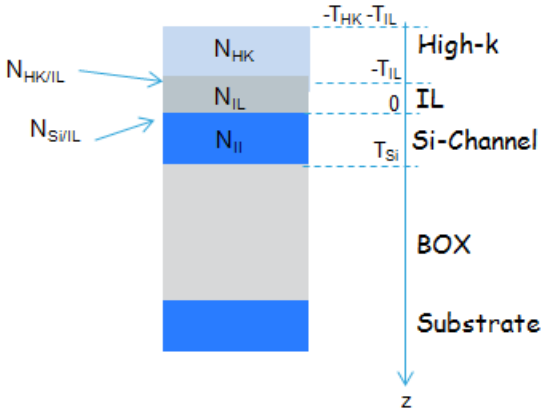

Figure 13 : Schematic of the different density of carriers affecting mobility through Local Coulomb or remote Coulomb scattering. The coordinate system (axe z) is also shown on this figure.

Ionized dopants in the channel (Local Coulomb Scattering: LCS) or charges in the gate oxide stack (Remote Coulomb Scattering: RCS) can effectively reduce the mobility in MOS transistors, especially at low effective field. Indeed, a Coulomb center produces a perturbation potential which can effectively scatter the carriers in the channel. The matrix element for LCS can be expressed as [47]:

$$\left|M_{n,n'(k,k')}\right|^2 = \frac{1}{A}\left[\int_0^{T_{Si}} \left|M^0_{n,n'}(k,k',z_0)\right|^2 N_{II}(z_0)dz_0 + \left|M^0_{n,n'}(k,k',z_0)\right|^2 N_{SI/IL}\right] \qquad (1.51)$$

where N_{II} and $N_{Si/IL}$ denote respectively the density per unit area of ionized impurities and Coulomb centers at the silicon-oxide interface.

In undoped channel FDSOI technology, various experimental studies [71] [72] and numerical calculations [79] [86] [87] [88] have demonstrated that the introduction of a high-k dielectric leads to strong degradation of the mobility through RCS. The squared matrix element due to Coulomb centers in the gate stack is given by:

$$\left|M_{n,n'(k,k')}\right|^2 \simeq \frac{1}{A}\left[\int_{-T_{HK}-T_{IL}}^{-T_{IL}} \left|M^0_{n,n'}(k,k',z_0)\right|^2 N_{HK}(z_0)dz_0 + \int_{-T_{IL}}^{0} \left|M^0_{n,n'}(k,k',z_0)\right|^2 N_{IL}(z_0)dz_0 + \left|M^0_{n,n'}(k,k',-T_{IL})\right|^2 N_{HK/IL}\right], \quad (1.52)$$

where N_{HK} and N_{IL} are the charge concentrations (per unit of volume) in the high-k layer and in the IL. $N_{HK/IL}$ is the charge densities (per unit area) of Coulomb centers at the high-k/IL. The matrix element produced by the Coulomb potential of a point charge located at z_0 is expressed as

$$M^0_{n,n'}(k,k',z_0) = \int_z \psi^*_{n'}(z)\,\psi_n(z)G(q,z,z_0)dz, \quad (1.53)$$

where $G(q,z,z_0)$ is the potential produced by a point charge located at z_0.

- **Determination of the potential produced by a point charge**

The potential produced by a point charge is obtained by solving the Poisson equation.

$$\left[\frac{\partial}{\partial z}\,\epsilon(z)\,\frac{\partial}{\partial z} - \epsilon(z).Q^2\right] G(q,z,z_0) = -e.\delta(z-z_0) \quad (1.54)$$

The finite difference method (described in Annex Ib) has been implemented for the resolution of this equation on a non-uniform grid [87]. Contrary to the analytic method, described in Annex Ia which is commonly used in literature [86] [77] [78], this method allows evaluating the scattering potential over more than three regions of varying dielectric constant. Moreover, using the finite difference method, the potential can be fixed to zero at the high-k/metal gate interface in order to account for the screening by the metal gate. The scattering potential obtained from the resolution of the Green's function by using the finite difference method is compared (Figure 14) to the analytical solution in [86] for a structure with three regions of different dielectric constants. Considering the two layers at each side (HfO_2 and Si) as infinitely thick, a very good correlation is obtained. From this figure, we can also see that a high value of high-k permittivity significantly reduces the perturbation. In Figure 15, the scattering potential is calculated in a FDSOI structure using two different boundary conditions: 1/ G=0 at high-k/metal gate interface and 2/ the thickness of the high-k layer is considered as infinite. The strong difference between the two resulting potentials highlights the importance to take account for the screening due to the metal gate, especially when charges are located in the gate stack. This makes the mobility dependent on the high-k thickness as proved in Figure 16.
In Figure 17, $G(q,z,z_0)$ is plotted for an arbitrary value of q= 2×10^8 m^{-1} showing that the scattering potential is maximum when charges are located in the channel.

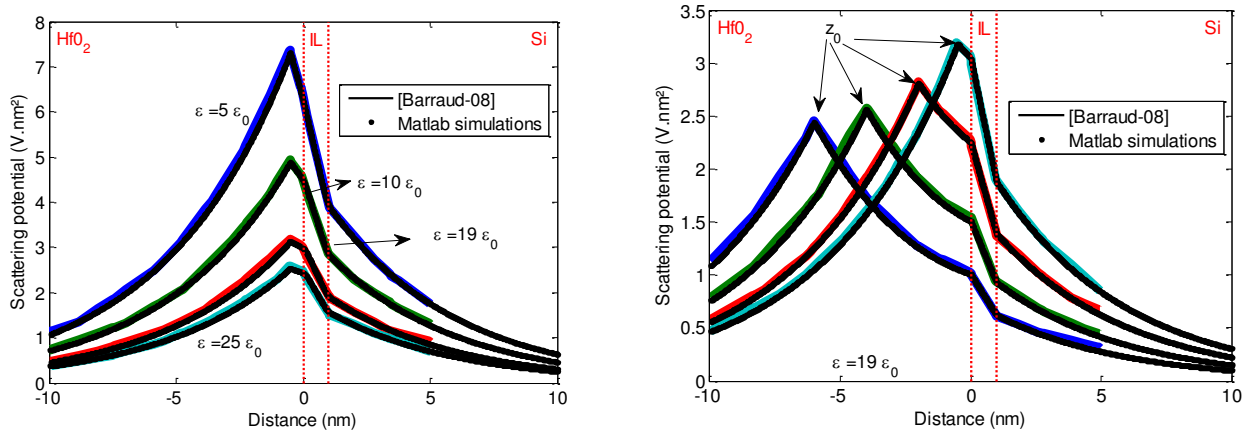

Figure 14 : Unscreened Coulomb scattering potential of a point charge a) located at 0.5 nm from the $Hf0_2/SiO_2$ interface calculated for different high-k permittivities b) located at different positions $\boldsymbol{z_0}$ inside the high-k dielectric. $q=2\times10^8$ m^{-1}.

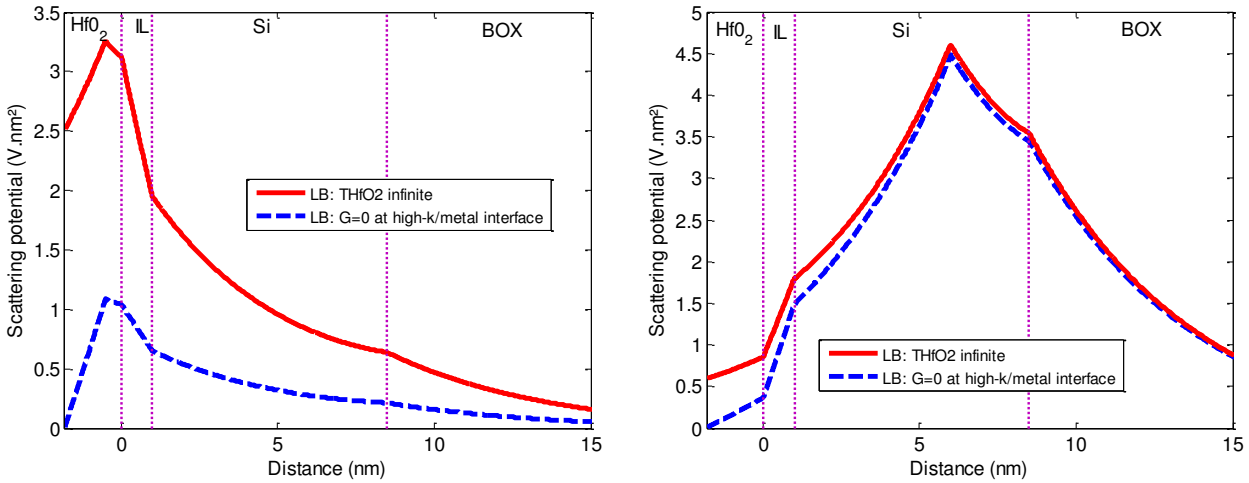

Figure 15 : Unscreened Coulomb scattering potential calculated using two different boundary conditions: 1/ by considering the thickness of the high-k as infinite (full lines) 2/ by fixing G=0 at high-k/metal interface (dashed line). The charge is located in the high-k a) or in the channel b). FDSOI device. T_{SI}=7.5 nm. SiO_2 BOX of 25 nm *(ε=3.9). The metal gate stack consists in a 1.8 nm thick high-k material (ε=20) on top of a* 1.0 nm thick SiO2 *layer (ε=3.9).*

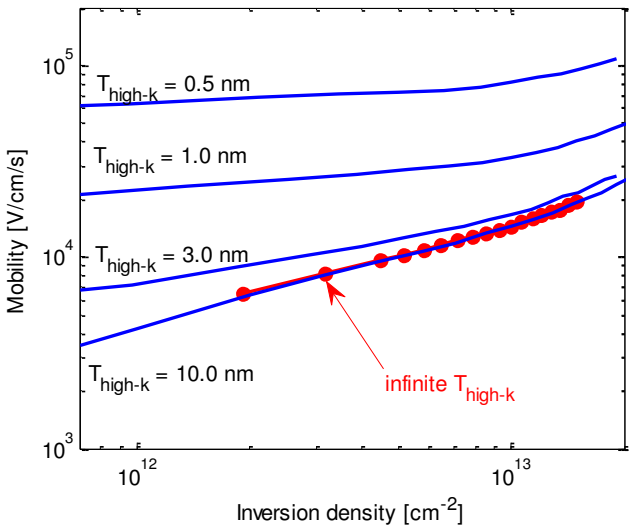

Figure 16 : Remote Coulomb-limited mobility as a function of the inversion density for various high-k thicknesses. $N_{it}=1\times10^{13}$ cm^{-2}. T_{SI}=7.5 nm. SiO_2 *box of 25 nm (ε=3.9). The metal gate stack cons*ists in a high-k *material with varying thicknesses (ε=20) on top of a 1.0 nm thick SiON layer (ε=5.2).*

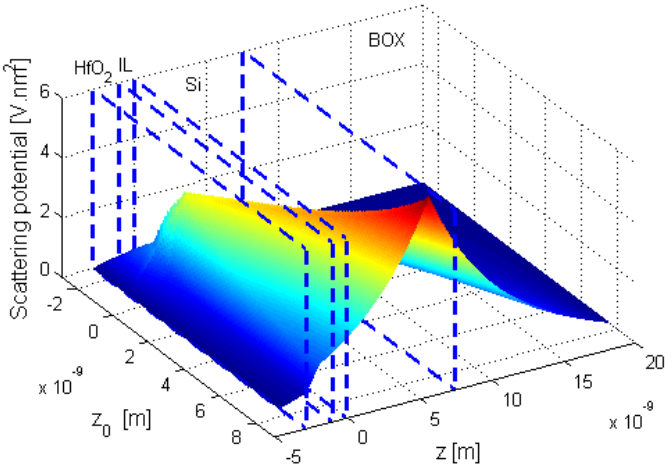

Figure 17 : Unscreened Coulomb scattering potential as a function of the position z for charges located at z_0. Boundary condition: G=0 at high-k/metal interface. Structure of Figure 15.

I.4.5 Alloy scattering

Alloy disorder is treated as an elastic isotropic scattering. For both electrons and holes, the matrix elements can be described as:

$$\left|M_{n,n'(k,k')}\right|^2 = \sum_l (1-x_l)\, x_l\, \frac{a_l^3}{8}\, U^2 F_{l,n,n'} \qquad (1.55)$$

a_l is the lattice constant, U is the deformation potential and F is the overlap form-factor defined in equation 1.32. Concerning the deformation potential, a wide range of values between 0.2 and 1.4 eV has been reported in the literature (Table 5).

Reference	U_{e^-} [eV]	U_{h^+}[eV]
Fischetti et al. [12]	0.7	0.9 ∓ 0.1
Hinckley et al. [80] Pham et al. [81]	-	0.2
Briggs et al. [83]	-	1.4
Mehrotra et al. [82]	$0.09.\ x_{Ge}{}^2 - 0.181.\ x_{Ge}{}^2 + 0.963$ ($x_{Ge} < 0.84$)	$0.777 - 0.006.\ x_{Ge}$
Lizzit et al. [84]	-	1.3
This work	-	0.8

Table 5 : Alloy scattering potential: data from literature and value used in our simulation for holes mobility.

We propose here to evaluate the SiGe alloy scattering potential for holes by comparing simulations and split-CV mobility measurements on structures presented in Table 6. This includes fully-depleted silicon or silicon germanium channels pMOSFET devices on SOI or strained SOI substrates (sSOI). To reproduce experiments, a value of $U_{h^+} = 0.8$ eV has been used for the alloy scattering potential (see Figure 18).

	SOI	sSOI	SGOI			sSGOI		
	SOI <100>	sSOI <110>	$Si_{1-x}Ge_x$ / SOI <110>			$Si_{1-x}Ge_x$ / sSOI <110>		
x (%)	0	0	22	34	43	22	34	43
ϵ (%)	0	0.75	-0.82	-1.3	-1.65	-0.08	-0.55	-0.9

Table 6 : Summary of the devices used for mobility measurements.

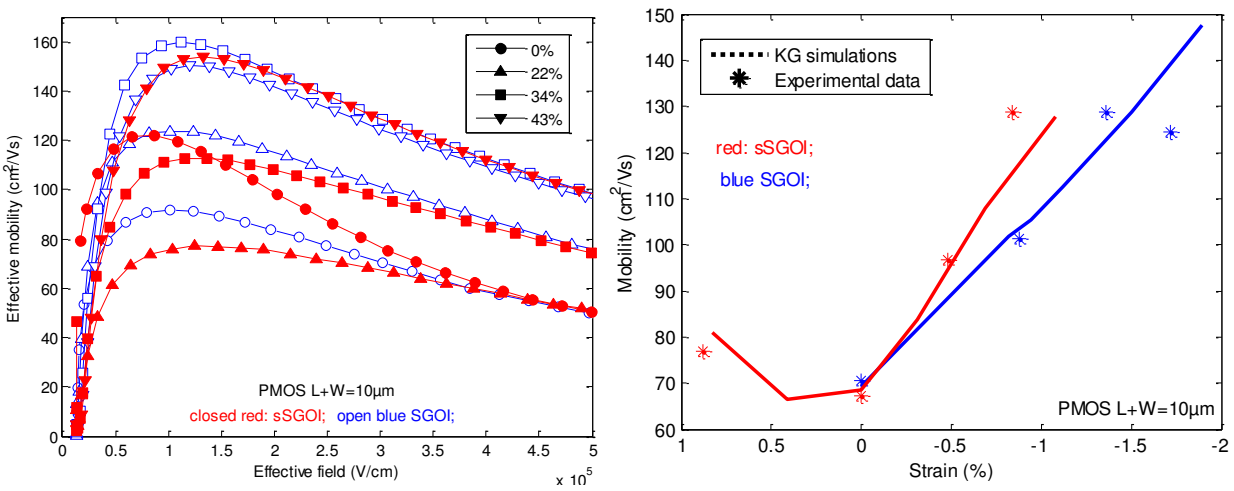

Figure 18 : a) Hole effective mobility as a function of the effective field for SGOI and sSGOI with varying channel germanium mole fraction. b) Hole effective mobility as a function of the strain extracted at E_{eff}=0.3 MV/cm.

I.4.6 Screening:

In MOS transistors, surface roughness and Coulomb scattering rates are strongly impacted by the screening produced by the carriers in inversion layers. Two different approaches are commonly used in the literature to compute the dielectric screening. The Tensorial Dielectric function (TDF) described in [37] is computationally very demanding so a simplified procedure has been derived from this model. In the Scalar Dielectric Function (SDF) approach [79], inter-subband matrix elements remain unscreened while intra-subband matrix elements are screened using:

$$\left|M_{vk,vk'}\right|^2 = \frac{\left|M^{unsc}_{vk,vk'}\right|^2}{\epsilon^2(q)} \tag{1.56}$$

with

$$\epsilon(\mathrm{q}) = 1 + \sum_{\mathrm{v}} \mathrm{F_{vv}(q)}\,\Pi_{\mathrm{vv}}(\mathrm{q}) \tag{1.57}$$

where the polarization factor $\Pi_{\mathrm{vv}}(\mathrm{q})$ is given by:

$$\Pi_{\mathrm{vv'}}(\mathrm{q}) = \frac{2\,g_v}{(2\pi)^2}\int \frac{f_0[E_v(k)] - f_0[E_{v'}(k+q)]}{E_{v'}(k+q) - E_v(k)} \tag{1.58}$$

g_v is the valley degeneracy, E_v is the subband dispersion and $f_0$is the Fermi-Dirac distribution function.

The screening form-factor is given by:

$$F^{vv'}_{\mu\mu'} = \int_{-\infty}^{\infty} dz \int_{-\infty}^{\infty} dz'\ \psi_\mu(z)\,\psi^*_{\mu'}(z) G(q,z,z')\psi_v(z').\psi^*_{v'}(z') \tag{1.59}$$

This approach is however valid in bulk and single gate FDSOI structure only. Indeed, it has been shown that the SDF approach fails to model the screening in Double-Gate SOI MOSFETs [37]. Consequently, the SDF cannot be used in the case of a FDSOI device when a back bias is applied.

Figure 19 shows the calculated unscreened and screened mobility for LC and SR scattering mechanisms in devices of Figure 15 by using the scalar approach.

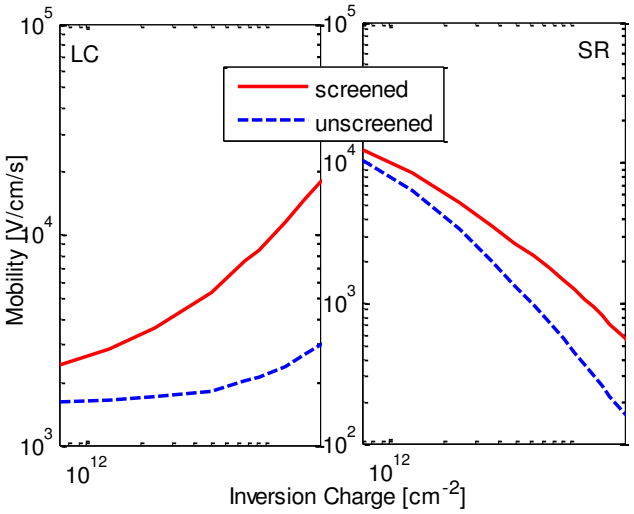

Figure 19 : *Δ=0.47 nm, Λ=1.3 nm, autocorrelation: exponential. Doping concentration=1*$\times 10^{18}$ cm^{-3}. Structure of Figure 15.

I.5 Conclusion:

In this chapter, the main models implemented in devices simulators that we used during the PhD work have been reviewed. First, a description of methodologies used to calculate the conduction and valence band structure of silicon, germanium and silicon germanium alloy is performed highlighting how stress and confinement are taken into account. Models based on the effective mass approximation for the conduction band and a 6-bands k.p for the valence band have been used during this work. In the second part we present a multi-scale strategy for MOSFET device modeling ranging from classical drift diffusion models to NEGF calculation. In the last part we have reviewed approaches to model the main scattering mechanisms in semi-classical solvers such as MSMC or KG. We focused on phonons, surface roughness, coulomb and alloy scattering mechanisms, highlighting their limits and the development performed in our STMicroelectronics in-house solvers (UTOXPP).

Chapter 2:

Physics-based modeling of low field transport in FDSOI transistors and comparison with experiments

II.1 Introduction

The aim of this chapter is twofold. In the first place, a comparison of the different approaches currently available to model low field transport in advanced Fully Depleted SOI transistors is performed. In the second place, the aim is to compare model accuracies to split CV mobility measurements. Semi-classical approaches based on the momentum relaxation time (such as KG) or based on the solution of the BTE (such as MSMC [46] [47]) have been widely used to calculate the long channel mobility in high-k metal gate FDSOI devices [29] [34] [39] [41]. However, there are only few examples in the literature of model comparisons on the same device [63]. Recently, P. Palestri and al. [62] compared the mobility calculated using transport models ranging from drift-diffusion to direct solutions of the BTE with the Monte Carlo method. Quite good agreements were found at large inversion N_{inv} charges but discrepancies appear at low N_{inv} due to the different treatment of phonon scattering in inversion layers. Moreover, a comparison between semi classical methods and calculations based on NEGF approach is still missing. In fact, there are no commercial versions of NEGF currently available including all scattering mechanisms. Moreover the modeling of long channel transistor with NEGF is not straightforward and a methodology has been developed for that purpose, as discussed later in this chapter. In consequence, in the first part of this chapter, the electron and hole mobilities have been calculated using four different solvers: the STMicroelectonics in-house solver (UTOXPP) [65], the commercial solver Sband from Synopsys [66], the MSMC solver from the University of Udine [67] and TB_SIM [68], the NEGF solver from the CEA. Phonon, surface roughness and coulomb (with charges at high-k/metal gate interface) limited mobilities have been considered. The second part of this chapter has been dedicated to the comparison between simulations and experiments, performed on state of the art FDSOI devices [69][70][75]. Using a large set of split-CV measurements, the impact of the Equivalent Oxide Thicknesses (EOT), the back voltage and the temperature have been investigated. We also reviewed important experimental and theoretical aspects of the universal behavior of the mobility with respect to the effective field in FDSOI MOSFETs. Last but not least, the capability of TCAD empirical models to reproduce theoretical and experimental results has been investigated. Indeed, Technology Computer Aided Design (TCAD) support for UTBB-FDSOI technology development can reduce cost and development time and also secure technology choices. For efficient TCAD purposes, a preliminary identification of the mechanisms responsible for transport degradation, as well as a calibration of empirical TCAD transport models, is mandatory. The challenge in this area is being able to propose a more rigorous calibration of TCAD mobility model on simulations rather than on experiments, while keeping the capability of reproducing experiments in all possible measurement configurations.

II.2 Advanced transport solvers comparison: Monte Carlo and Kubo Greenwood approaches compared to NEGF simulations.

The different methods to study the transport in advanced CMOS technology have been briefly descried in chapter I. Before comparing mobility calculations, we present here the different tools used during this thesis. All solvers are based on a multi-subbands (or quantum) approaches and this differs from other approaches such as drift diffusion solvers.

II.2.1 Solvers description

1) Multi-subbands Monte Carlo (MSMC):

The MSMC solver of the University of Udine includes scattering with phonons [47], surface roughness (GPN model), coulomb and alloy scattering mechanisms (ionized impurities and remote Coulomb) [47]. The screening can be accounted for using the scalar or the tensorial approach. Concerning band structure models, the EMA is used for the conduction band calculation.

2) UTOXPP

UTOXPP is a self-consistent 1D Schrödinger-Poisson solver developed at STMicroelectronics [66]. The mobility is calculated using the Kubo-Greenwood formula presented in chapter I (equation 1.26) for both electrons and holes. The solver includes scattering with phonons [47], surface roughness (GPN model) [46], coulomb and alloy scattering mechanisms (ionized impurities and remote Coulomb) [47]. The screening can be accounted for using the scalar or the tensorial approach. The band structure models range from the non-parabolic EMA to 30 band k.p, including 2 band k.p and 6 band k.p.

3) Sband

Sband is a commercial self-consistent 1D Schrödinger-Poisson solver from Synopsys [65] coupled with the Kubo-Greenwood formula to calculate the mobility for both electrons and holes. The solver includes the same scattering mechanisms as in UTOXPP. The screening can be accounted for using the scalar approach for surface roughness scattering and the scalar or tensorial approach for coulomb scattering. The band structure is calculated thanks to the non-parabolic EMA or 2 band k.p models for conduction band and 6 band k.p for the valence band.

4) TBSIM:

TB_SIM [68] is the NEGF solver from the CEA. In this code the NEGF equations are solved on a finite difference grid, in a coupled space mode approach. The solver include scattering with phonons using the Born approximation [38], “geometrical” surface roughness, local coulomb and remote coulomb scattering mechanisms. The band structure is calculated using EMA or 2 band k.p for conduction band and a 6 band k.p for the valence band.

II.2.2 Methodology of comparison of different approaches

Before starting the comparison between mobilities calculated with all solvers, let us put forth two important points. First we discuss about the methodology of extraction of single mechanism limited mobility, and then, the effective field definition in UTBB-FDSOI MOSFETs.

- **Extraction of phonon, coulomb, remote coulomb and surface roughness-limited mobility**

The Matthiessen’s rule states that the inverse total mobility is the sum of the inverse of the partial mobilities of each scattering mechanism:

$$\frac{1}{\mu_{tot}^{M}} = \frac{1}{\mu_{PH}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_{RCS}} \tag{2.1}$$

It can be proved that [38] this widely used equation is exact only if 1) the scattering rates of all mechanisms have the same dependence on energy, and 2) these mechanisms are independent one from each other (no spatial correlations). The second condition usually holds for phonons, SR and RCS, but the first one does not. Moreover, although the PH, RCS, LC and SR-limited mobilities can be calculated using KG solvers through equation 2.2, in NEGF or MSMC simulations, these mobilities cannot be extracted directly by turning off the phonon scattering mechanisms. As a consequence, an "effective" mobility μ_M, based on the Matthiessen's rule is defined and used for the comparison between the different solvers:

$$\mu_{A,eff}^{-1} = \mu_{A+PH}^{-1} - \mu_{PH}^{-1}, \tag{2.2}$$

A is the considered scattering mechanism: surface roughness or Coulomb scattering.

Quantitative errors, which compare the mobility directly extracted via KG simulations μ_A, and the effective mobility $\mu_{A,eff}$, have been calculated using the following expression [64]:

$$E = \frac{\mu_{A,eff} - \mu_A}{\mu_A} \tag{2.3}$$

An error ranging from 20 to 12% is observed (Figure 20) for phonons + SR scattering mechanisms which is consistent with simulations from Esseni et al. [64]. Concerning RC scattering, the error can reach 80% which is of the order of magnitude than the error reported for local coulomb scattering mechanism [64].

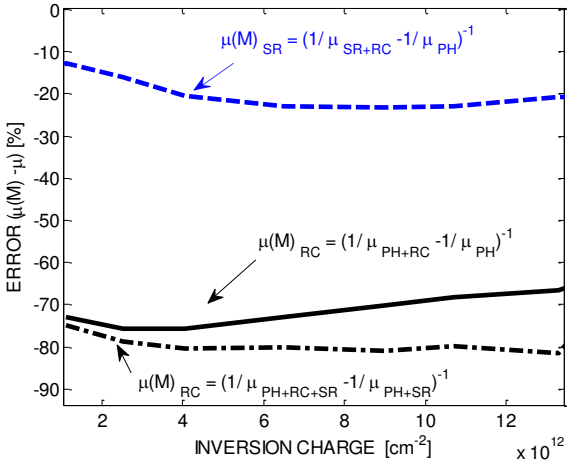

Figure 20 : Error E produced by the extraction of mobility components (surface roughness and remote *coulomb scattering) using the Matthiessen's rule.*

In Figure 21a, we can notice that the partial SR and RCS mobilities defined in equation 2.4 follow Matthiessen's rule much better than the usual, single mechanism partial mobilities (equation 2.1), as testified in [38]. Indeed, Matthiessen's rule holds within 1% in the whole density range (Figure 21b).

$$\frac{1}{\mu_{tot}^{M}} = \frac{1}{\mu_{PH}} + \frac{1}{\mu_{SR,eff}} + \frac{1}{\mu_{RCS,eff}} \tag{2.4}$$

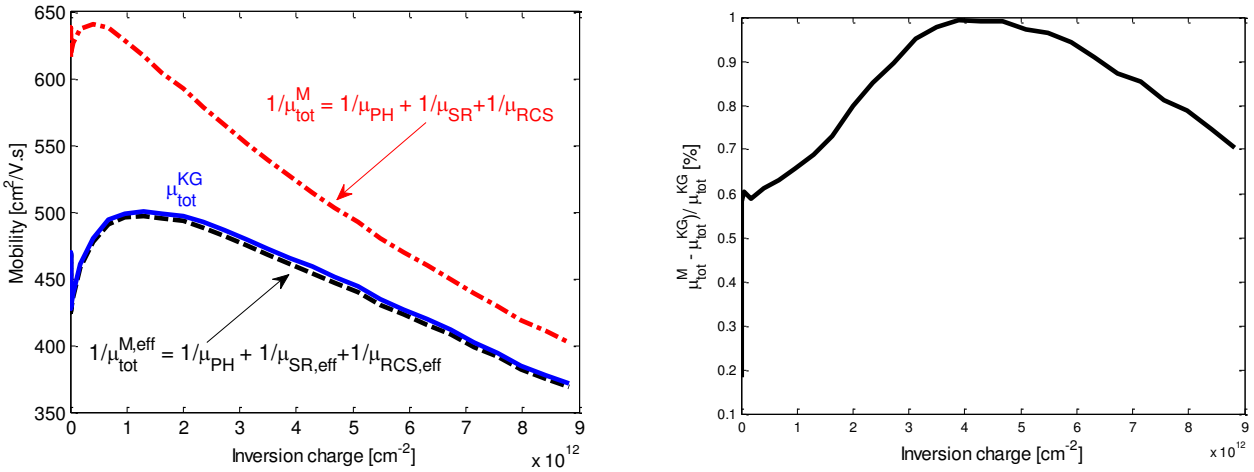

Figure 21 : (a) Total KG mobility $\boldsymbol{\mu_{tot}^{KG} = \mu_{PH+SR+RCS}^{KG}}$ ($\boldsymbol{n_{RCS} = 3.0 \times 10^{13} cm^{-2}}$) compared with Mat*thiessen's rule* $\boldsymbol{\mu_{tot}^{M}}$ from eq. 2.1 and $\boldsymbol{\mu_{tot}^{M,eff}}$ from eq. 2.2. (b) Error induced by the Matthiessen rule $\boldsymbol{\mu_{tot}^{M,eff}}$ on the total mobility.

Of course, Matthiessen's rule might still break down at low enough temperature and in specific systems, but its range of applicability is certainly broader using equation 2.4 as definition of the partial mobility rather than a direct, single mechanism calculation (equation 2.1). This opens the way for a more accurate modeling of the mobility in TCAD tools. Moreover it deserves to notice that TCAD mobility models are based on the Matthiessen's rule.

- **Discussion about the effective "mobility" field and the effective "electrostatic" electric field.**

Since the seminal work by Takagi, in bulk transistors, theoretical and experimental mobilities are usually shown as function of the effective field [44]. This representation has two main advantages. First, the mobility curve versus effective field is independent of the substrate doping (leading to the so called "universal mobility curve"). Second, it allows a simple comparison of different technologies and with experimental data found in house or reported in the literature. In bulk devices, an effective "mobility" field has been proposed:

$$E_{ave/eff}^{exp} = \frac{Q_d + \eta Q_i}{\epsilon_{Si}} \tag{2.5}$$

where the value of η (=0.5 for electrons, 0.3 for holes) has been taken from mobility experiments in order to obtain the "universal" behavior [44]. Interestingly, when η = 0.5, the effective field exactly coincides with the average transverse "electrostatic" field seen by electrons but also by holes in the channel, given by:

$$E_{ave}^{th} = \frac{\int_0^{T_{SI}} E_z(x) n(x) dx}{\int_0^{T_{SI}} n(x) dx} \tag{2.6}$$

In the case of UTBB-FDSOI MOSFETs, the definition of the effective field has to be modified, in order to take into account for the electric field at the back interface. The proper definition of an effective field in the case UTBB-FDSOI MOSFETs for all possible bias configurations (including volume inversion) is not easy and controversial [57] [58], especially in double gate device. However,

when the inversion layer is essentially produced by the front gate, the effective field is commonly defined as [59]:

$$E_{ave/eff}^{exp} = \frac{Q_d + \eta Q_i}{\epsilon_{Si}} - \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{VB}{T_{BOX}^{eff}} \quad (2.7)$$

with $T_{BOX}^{eff} = \frac{C_{Si}+C_{BOX}}{C_{Si}} T_{BOX} + \Delta$, Q_i the inversion charge, Q_d the depletion charge ($Q_d = q N_a T_{SI}$) and $\Delta \simeq 1.5$ nm accounts for the ground plane accumulation or depletion. In order to match equations 2.6 and 2.7, η has to be taken equal to $\eta = 0.5$ for both n- and pMOS devices in bulk [60] as well as in FDSOI structures [61].

The validity of equation 2.7 can be seen in Figure 22. Indeed, in this figure the inversion charge is plotted as a function of the average transverse field (calculated numerically) or as a function of the effective field defined by equation 2.7, showing an excellent agreement for all applied back bias (providing $\eta = 0.5$ for both electrons and holes).

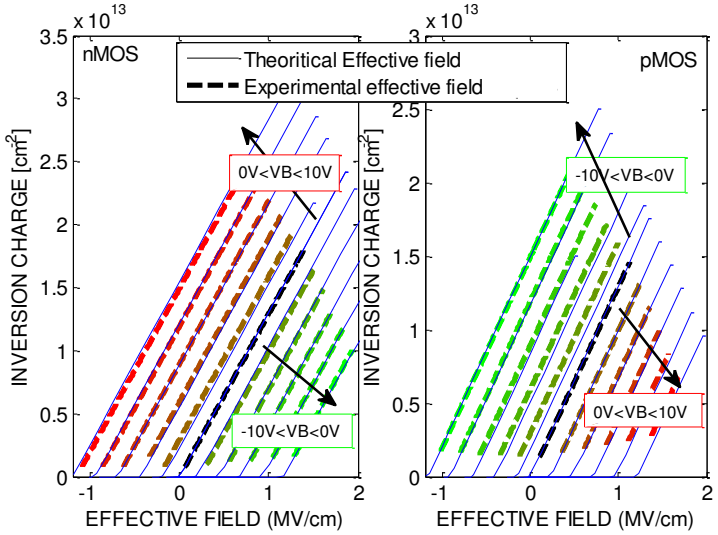

Figure 22 : n- (left) and p- (right) FDSOI experimental electric field (equation 2.7*) assuming $\eta = 0.5$ compared* to the simulated theoretical average field (equation 2.6). VB from -10 V to 10 V in steps of 2V. IL EOT = 1.8 nm; T= 300 K.

The concept of effective field will be used in the following section, to compare the different mobility models. It will be also reconsidered in the section dedicated to the comparison with experiments. In particular, the extraction of the η parameter for n- and p FDSOI devices will be discussed in part II.3.5.

II.2.3 Advanced solvers comparison

In order to compare the different solvers, the same device structure has been considered. This 1D structure of the long channel FDSOI device (and material properties), used for the comparison is illustrated in Figure 23. The device is essentially composed of an ultra-thin layer of silicon (10 nm or less thick), between a thin Buried Oxide (BOX) (25nm) and a high-k gate stack. This latter oxide includes an interfacial layer (of various thicknesses) and a thin layer of high-k (1.8 nm).

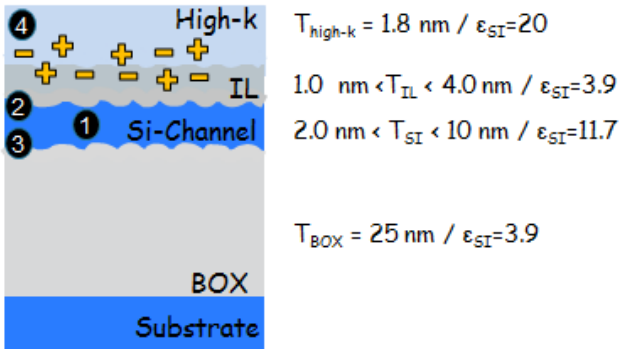

Figure 23 : Schematic of the simulated FDSOI devices. The comparison is done for surface roughness, phonons and remote Coulomb scattering

- **Electrons**

In this comparison a purely parabolic band has been considered for simplicity. Phonon scattering parameters are listed in Table 7.

Phonon	Type	Coupling constant	$\hbar\omega_{ph}$[meV]
intervalley	f-type	DtK= 0.3 10^8 eV/cm	18.96
intervalley	f-type	2.0 10^8	47.4
intervalley	f-type	2.0 10^8	59.03
intervalley	g-type	0.5 10^8	12.06
intervalley	g-type	0.8 10^8	18.53
intervalley	g-type	11.0 10^8	62.04
intravalley		DAC =14.6 eV	0

Table 7 : Phonons model parameters used for silicon taken from [85].

First of all, the phonon-limited mobility extracted at two different effective fields (0.08 and 0.6 MV/cm) is plotted in Figure 24 for silicon thicknesses varying from 2 nm to 10 nm. The expected non-monotonic behavior is observed [41] and can be explained by two counteracting effects [42]:
- the form factor defined in equation 1.32 increases with decreasing T_{Si} [42];
- below 10 nm, the electrons are progressively confined in the lowest unprimed subband which features a lower conduction mass [41].
In this case, an excellent agreement between all solvers is obtained.

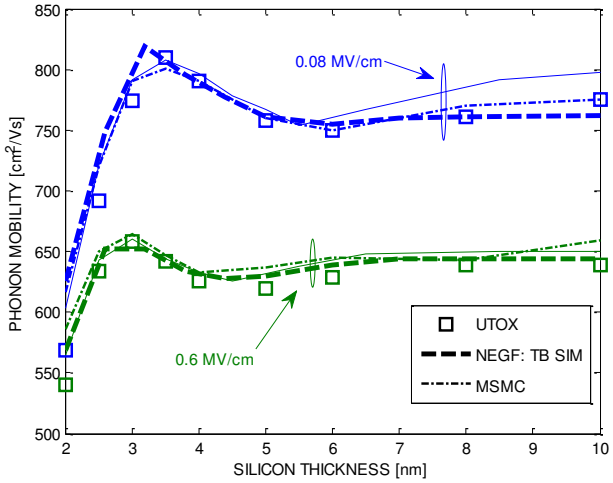

Figure 24 : Comparison of phonon-limited electrons mobility in FDSOI devices as a function of active layer thickness.

In Figure 25a, the calculated SR-limited mobility as a function of the effective field using all solvers has been reported for three different silicon thicknesses. The same parameters than in [34] have been used for comparison: an exponential SR autocorrelation with RMS amplitude of Δ=0.47 nm and a correlation length of Λ=1.3 nm. The mobility calculated with all solvers has been extracted using the same procedure (previously explained in part II.2.2) in order to avoid differences due to the extraction method. Results obtained by the semi-classical solvers (sband, UTOX and MSMC) have been found in good agreement, however not with the NEGF result. This is further depicted in Figure 25b, which represents the SR-limited mobility as a function of the silicon thickness. The results of S. Jin [34], also based on a semi-classical approach, but accounting for carrier density fluctuation and image charge effects, have also been added on this Figure 25b. The disagreement between semi-classical methods and NEGF might result from [38]: 1) the second-order perturbation theory (Fermi Golden Rule) behind KG and MSMC; and 2) the approximations made in the treatment of SR in KG. It has been shown in [38] that the Fermi Golden Rule seems to be valid for SR scattering so this overestimation of the mobility seems to be due to assumptions behind the implemented SR model (Generalized Prange Nee model) as described in Chapter I.

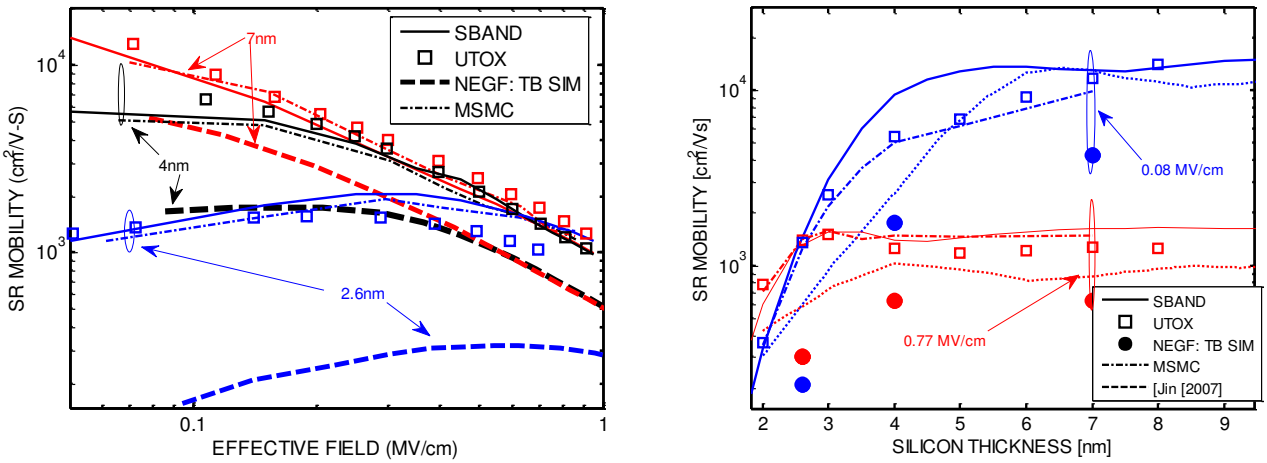

Figure 25 : Surface roughness-limited electrons mobility a) as a function of the effective field for T_{Si}=2.6 nm, 4.0 nm and 7.0 nm. b) as a function of T_{Si} extracted at E_{eff}= 0.08 and 0.77 MV/cm. (exponential SR *autocorrelation with Δ=0.47 nm; Λ=1.3 nm).*

In Figure 26, the SR-limited mobility is compared between UTOXPP and Sband for various doping concentrations at VB=0V and 8V. For high back biases (back gate inversion), a non-monotonic trend is observed (Figure 26*b* and Figure 27) which is a consequence of scattering with surface roughness at the back and front interfaces.

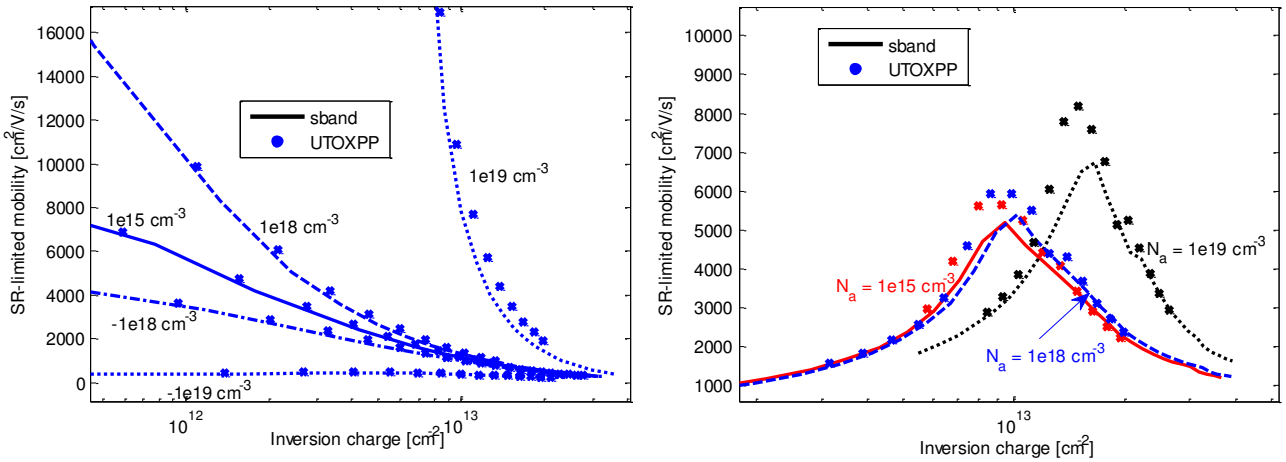

Figure 26 : SR-limited mobility as a function of the inversion charge calculated using Sband and UTOXPP for different channel doping concentrations at VB=0V (a) and VB=8V (b). (Exponential auto-correlation with *Δ=0.47 nm and Λ=1.3 nm).*

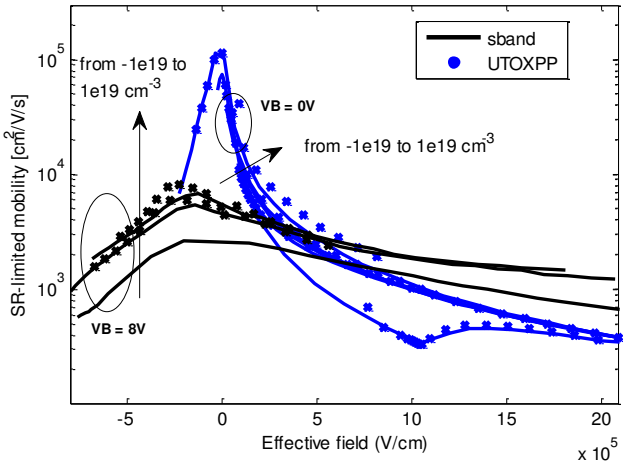

Figure 27 : SR-limited mobility as a function of E_{eff} calculated for different channel doping concentration at VB=0 and 8V.

In Figure 28, remote Coulomb scattering calculated with KG is compared to results obtained using NEGF at two different back voltages (VB=0V and VB=8V). In this case, a quite good agreement is found between the solvers.

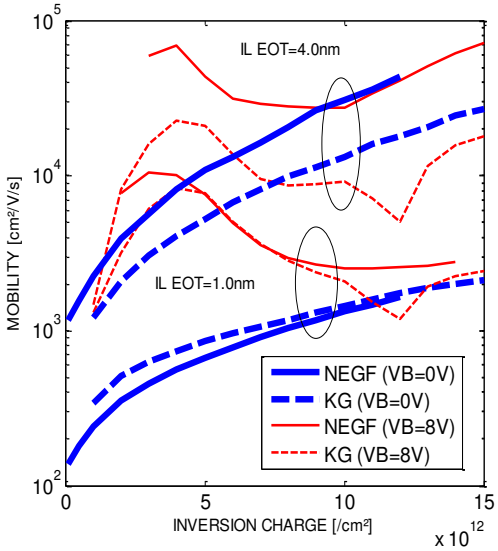

Figure 28 : Remote-Coulomb-limited electron mobility as a function of the inversion charge for devices with two different IL EOT: 1.0 nm and 4.0 nm. N_{it} = 5×10^{13} cm^{-2}

The Local Coulomb-limited mobility is compared between UTOXPP and Sband in Figure 29 for various doping concentration, for VB=0V and 8V. Excellent agreements are found between the two solvers.

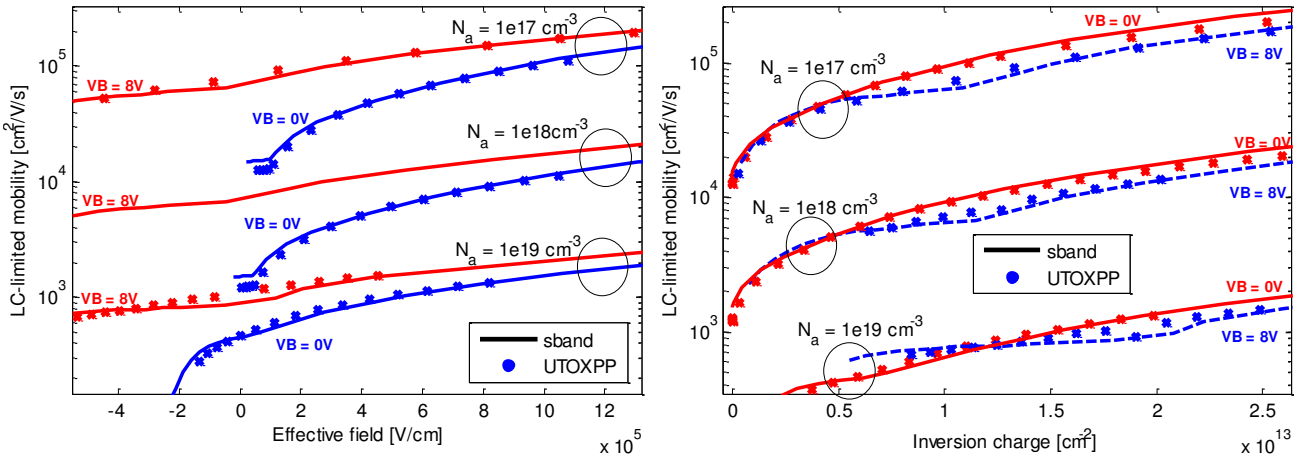

Figure 29 : Local-Coulomb-limited electron mobility as a function of a) the effective field and b) the inversion charge for various channel doping concentrations and for VB=0V and 8V. The metal gate stack consists in a 1.8 nm thick high-*k material (ε=20) on top of a 1.2 nm thick SiON layer (ε=6.6).*

- **Holes**

In this study, the hole band structure has been calculated using a 3 bands k.p model with L, M and N parameters from Table 3 (Δ=0). Parameters for the scattering mechanisms are listed in Table 8.

Phonon type	Coupling constant	$\hbar\omega_{ph}$[meV]
intravalley	DtK= 15.0 * 10^8 eV/cm	62.0
intravalley	DAC =10.2 eV	0

Surface roughness	*Δ [nm]*	*Λ [nm]*	Autocorrelation
	0.47	1.3	Exponential

Table 8 : Phonons and surface roughness mobility model parameters for holes.

The phonon-limited mobility is plotted as a function of the inversion charge for three different silicon thicknesses (3.0, 5.0 and 7.0 nm) in Figure 30. The mobility calculated with KG solvers presents a mobility compared to the results obtained with the NEGF solver.

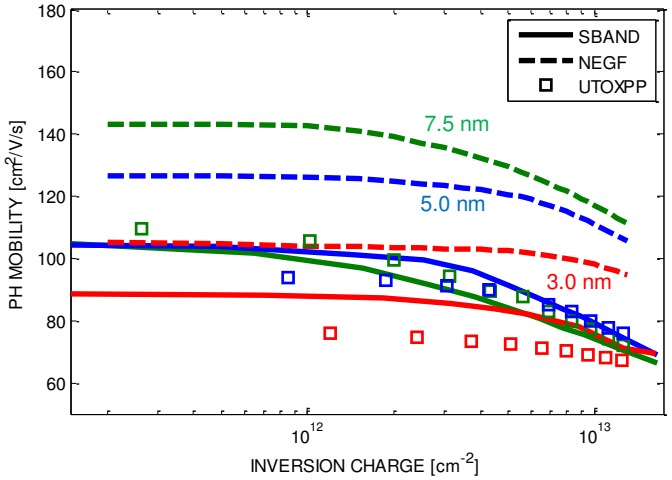

Figure 30 : Comparison of phonon-limited holes mobility in FDSOI devices as a function of the inversion charge for three different silicon thicknesses (3.0, 5.0 and 7.5 nm).

In Figure 31, we reported the SR-limited mobility as a function of the inversion charge for three different silicon thicknesses. A good agreement between UTOXPP, Sband and TBSIM can be observed for T_{Si}=7.5 nm. However, the conclusion is the same as for electrons: the mobility degradation with T_{Si}, observed with semi-classical solvers, is less pronounced compared to NEGF simulations.

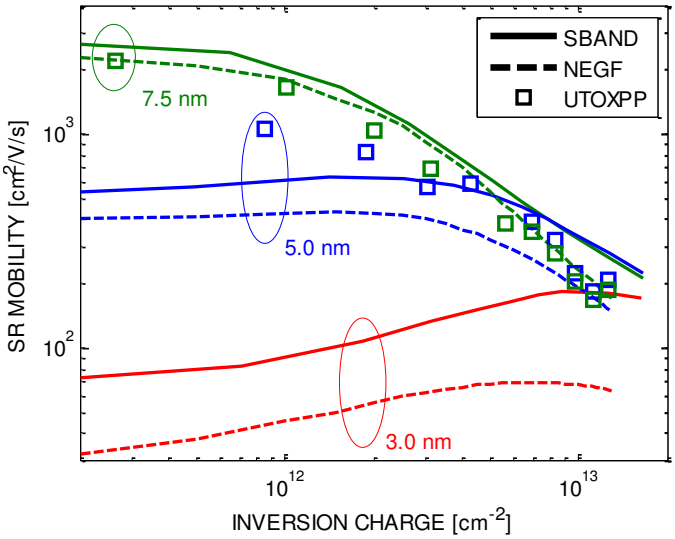

Figure 31 : Surface roughness-limited holes mobility as a function of the inversion charge for T_{Si}= 3.0 nm, 5.0 nm and 7.5 nm.

II.3 Split-CV mobility measurements in FDSOI structures: experimental results and calibration.

In the previous section, we have compared the mobility calculated using semi-classical solvers such as KG and MSMC to NEGF results. In the second part of this chapter, a comparison between simulations and experiments is performed on UTBB-FDSOI structures. Using a large range of split-CV measurements, the impact of the Equivalent Oxide Thicknesses (EOT), the back voltage and the temperature have been investigated. We also reviewed important experimental and theoretical aspects of the universal behavior of the mobility with respect to the effective field in FDSOI MOSFETs.

II.3.1 Sample processed

Devices have been processed on 300 mm SOI wafers with a 25 nm thick BOX (Figure 32). The oxide stack is made of a 1.8 nm thick layer of high-k oxide (HfSiON) deposited on top of an SiON interfacial layer (IL) with various EOT from 0.7 to 3.0 nm The final silicon channel thickness is 7.5 nm and the effective mobility was extracted using split-CV method on 0.9x0.9 µm² (WxL) devices corrected from access resistances R_{access}=2x60 Ω.µm. Measurements have been performed on n- and p-type devices.

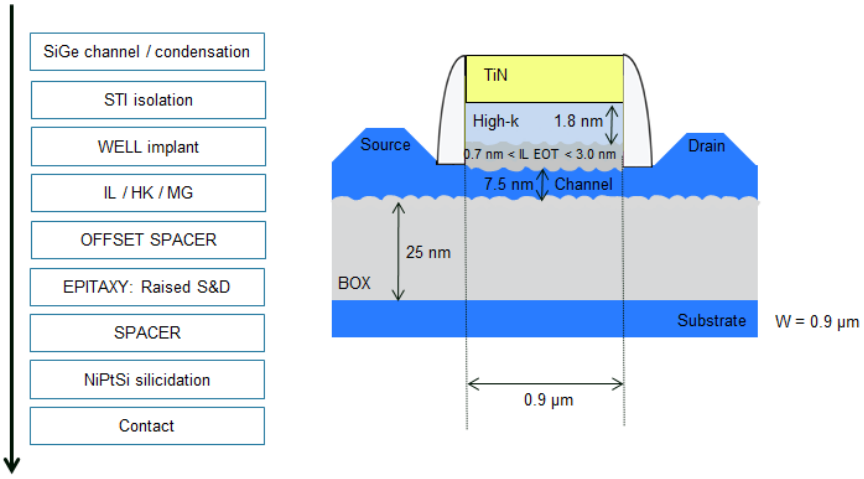

Figure 32 : a) Front-end process flow for 28FDSOI technology. b) Cross-section of a FDSOI MOSFET

II.3.2 Impact of the back bias

The impact of voltage VB, applied at the back terminal, on the gate capacitance is shown in Figure 33 for both n- and pMOS devices. As previously demonstrated in [42], in the reverse regime (back inversion), the capacitance is distorted and reaches a first level whose magnitude is related to the active layer capacitance C_{Si} in series with the oxide one C_{inv}. The capacitances obtained from all solvers (only TCAD results are shown here) are added on the figure allowing an accurate calibration of the EOT.

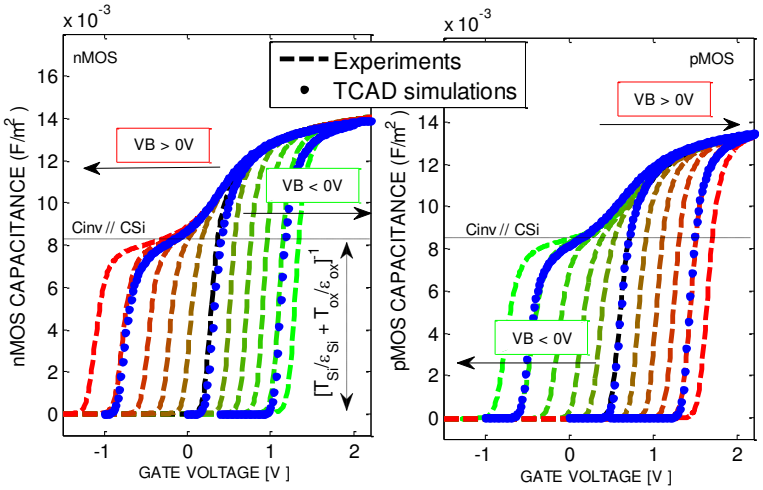

Figure 33 : Gate capacitance as a function of the gate voltage for various back biases ranging from -10V to 10V per steps of 2V in n- (a) and p-MOS (b) devices. T_{inv}=2.65 nm; T_{Si}=7.5 nm; T=300 K. TCAD calibration shown for VB=-8, 0 and 8V.

Figure 34a shows the threshold voltage (VTH) variation with VB for n- and pMOS devices. As can be seen, the VTH can be shifted by -1.5 V to 1 V for VB with ranging from -10 V to 10 V. The corresponding drain current measurement at various VB is shown in Figure 34b. We found out that the sub-threshold slope remains almost unchanged with back bias ($\Delta S/S<7\%$).

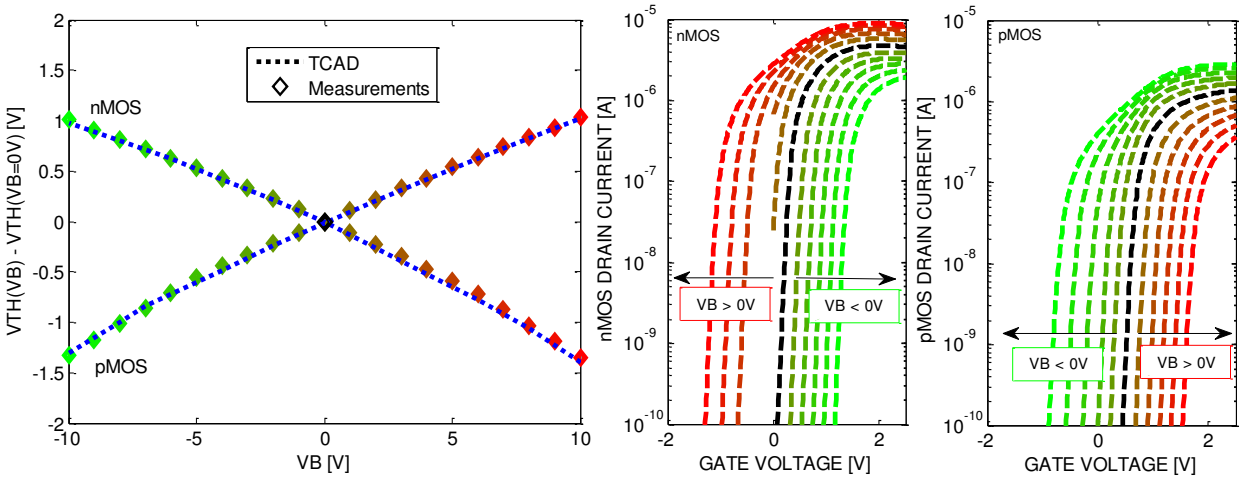

Figure 34 : Threshold voltage variation (reference at VB=0 V) as a function of the back bias in n- and pMOS devices. T_{inv}=2.65 nm; T_{Si}=7.5 nm; T=300 K.

The dependence of the mobility on inversion charge for various back biases for n- and pMOS is shown in Figure 35. For a given inversion charge, an increase of the mobility is observed for VB>0 V in nMOS and for VB<0 V in pMOS devices. In reverse region, a non-monotonic behavior of the mobility is shown (not to be confused with the RC-limited contribution observed at lower density). This is further depicted in Figure 36 which represents the mobility variation as a function of VB for fixed inversion charge for both devices.

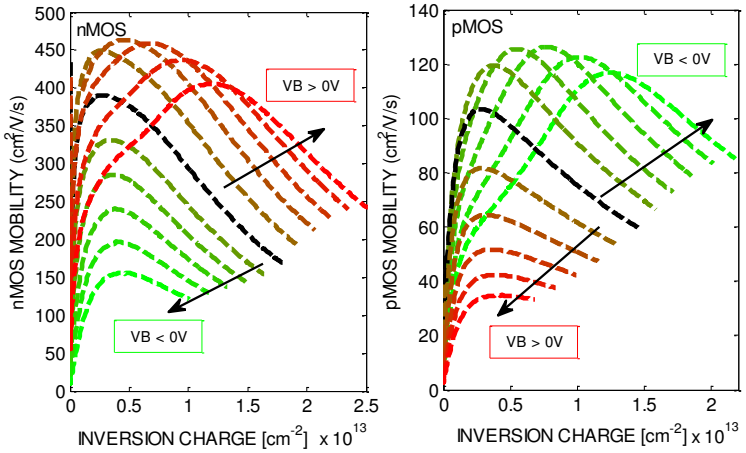

Figure 35 : Experimental effective mobility as a function of the inversion charge for various back biases ranging from -10V to 10V in steps of 2V, in n- (a) and pMOS devices (b). T_{inv}=2.65 nm; T_{Si}=7.5 nm; T=300 K.

Figure 37 shows the profile of the potential and the electron density in the channel simulated using Poisson-Schrödinger solver (PS) for three front and back gate voltage conditions specified in Figure 36 (N_{inv} = 1 ×10^{13} cm^{-2}). The application of a high positive VB induces a back gate inversion for nMOS devices. No clear "volume" inversion regime is however reached as the majority of carriers are still confined at front and back interfaces. This is expected since the silicon channel is too thick (T_{Si} = 7.5 nm) to reach this regime [95]. The mobility enhancement can be explained by the shift of the inversion charge centroid away from the front interface affecting surface roughness and the screening of the Coulombic effect at the high-k/IL interface [38].

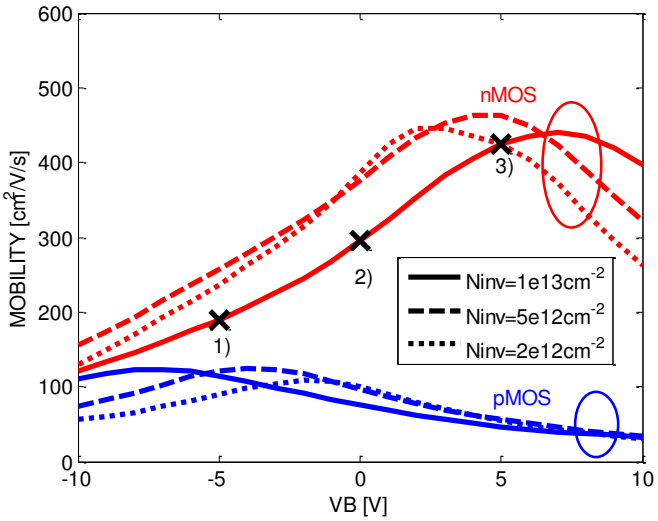

Figure 36 : Effective experimental mobility as a function of the back bias for various inversion densities: $N_{inv}=1\times10^{13}$, 5×10^{12} and 2×10^{12} cm^{-2}. IL EOT= 1.8 nm; T_{Si}=7.5 nm; T=300K. Symbols represent biases conditions whose density profiles are extracted in Figure 37: 1/ VB=-5 V, VG=2.0 V; 2) VB=0 V, VG=1.6 V; 3) VB=5 V, VG=1.2 V.

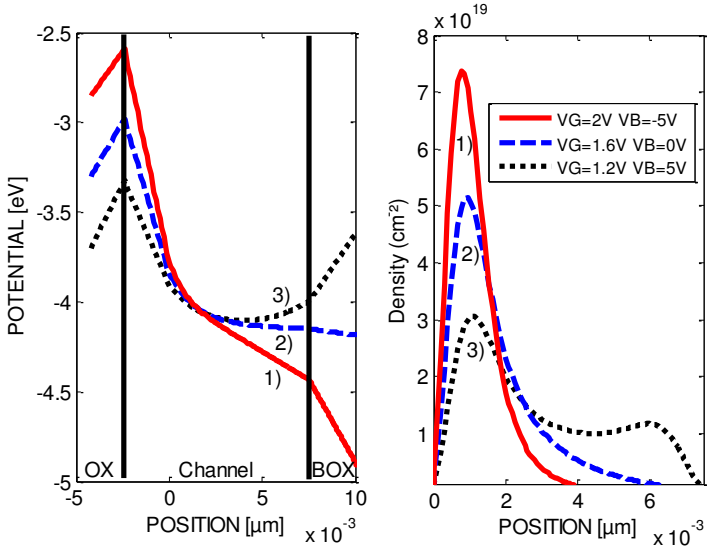

Figure 37 : Simulated profile of the potential (a) and the electron density (b) in the channel for various biases conditions using PS simulations): 1/ VB=-5 V, VG=2.0 V; 2) VB=0 V, VG=1.6 V; 3) VB=5 V, VG=1.2 V. nMOS device, IL EOT= 1.8 nm. T_{Si}=7.5 nm; T=300 K.

II.3.3 Impact of the interfacial layer thickness

The gate capacitance for three devices with physical IL thicknesses of 2.4 nm, 3.5 nm and 4.0 nm is shown in Figure 38. The capacitances calculated with all solvers (only TCAD results are shown here) are also added to the figure.

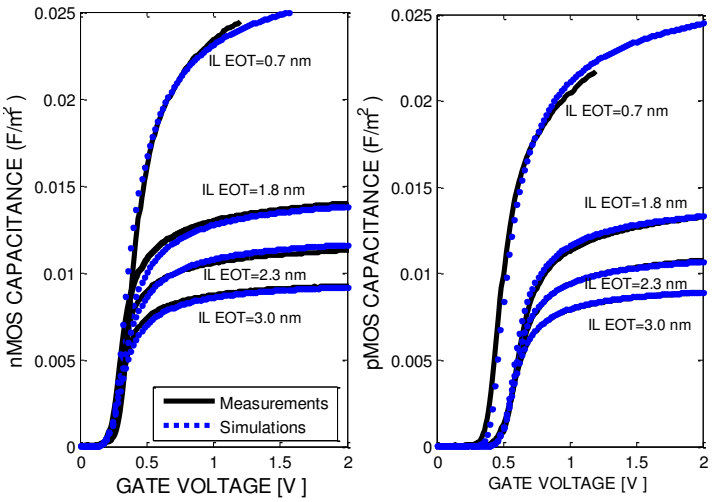

Figure 38 : Gate capacitance as a function of the gate voltage for devices with different IL EOT varying from 0.7 nm to 3.0 nm.

The mobility variation with respect to the inversion charge for four structures with different IL EOT (0.7, 1.8, 2.3 and 3.0 nm) is shown in Figure 39. A significant degradation of the mobility is observed with decreasing IL. The degradation of the mobility in presence of high-k oxide is well known and can be attributed to remote coulomb [76] [86] [87] [88], remote phonon [89] or remote surface roughness scattering [90]. These scattering mechanisms are strongly dependent on the thickness of the interfacial layer but it has been demonstrated in [88] that the remote phonon scattering mechanism is significant for IL EOT<1 nm only. Concerning remote surface roughness scattering, there is a controversial debate about its importance. Indeed, some groups suggest that it may degrade the mobility [91] [92] but there is no publication demonstrating it by means of experimental data. Moreover, for IL EOT>1 nm, our simulations suggest that RC is the main mechanism responsible for the mobility degradation (variation of the mobility with the IL EOT is well reproduced by considering RC only-Figure 53a).

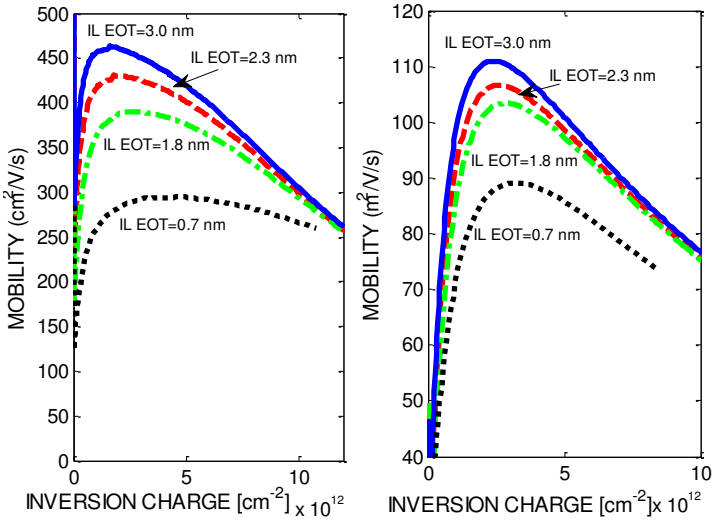

Figure 39 : n- (a) and pMOS (b) experimental effective mobility as a function of the inversion charge for structures with various IL physical thicknesses (VB=0 V).

II.3.4 Impact of the Temperature

The mobility has been plotted as a function of the inversion charge at various temperature for n- (Figure 40) and p-type (Figure 41) devices. As already observed in bulk devices, the mobility strongly decreases at high temperatures and it is mainly due to an increase of phonon scattering rates.

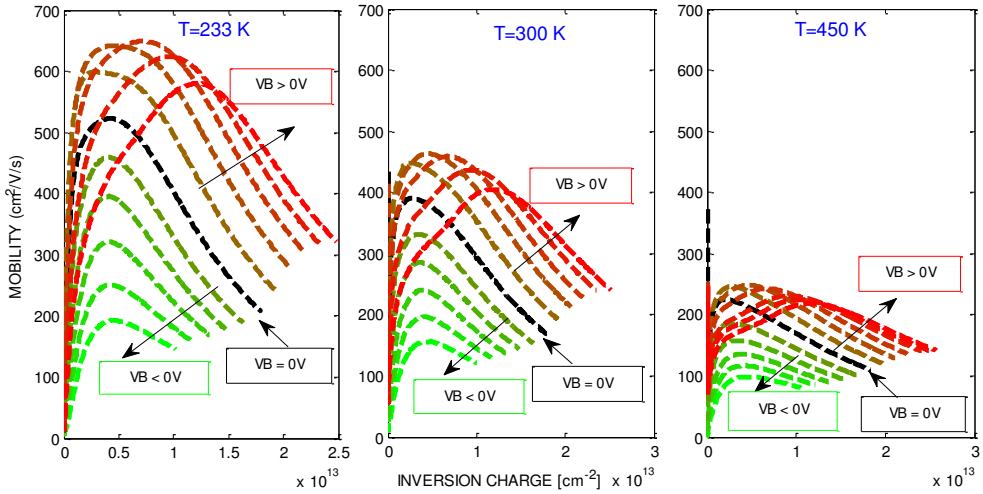

Figure 40 : Effective experimental mobility as a function of the inversion charge for various VB ranging from -10 V to 10 V in steps of 2 V. nFDSOI device : IL EOT= 1.8 nm. T=233, 300 and 450 K.

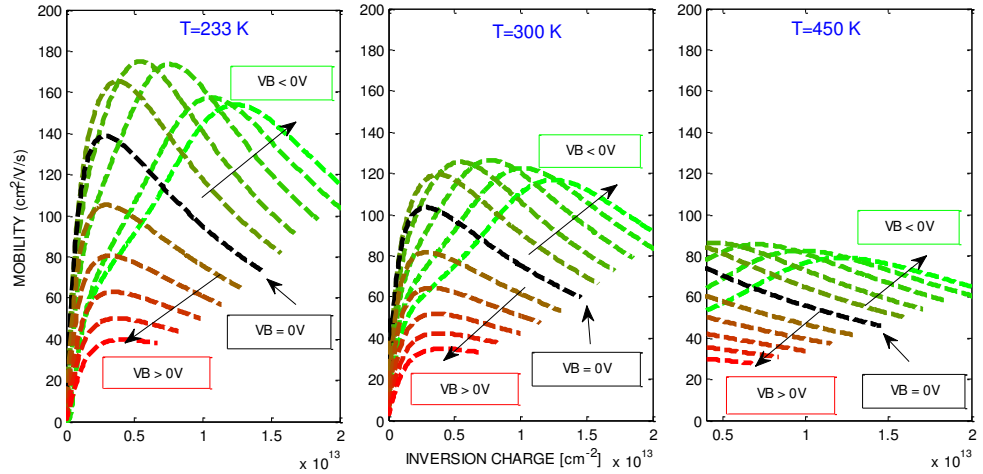

Figure 41 : Effective experimental mobility as a function of the inversion charge for various VB ranging from -10 V to 10 V in steps of 2 V. pFDSOI device : IL EOT= 1.8 nm. T=233, 300 and 450 K.

II.3.5 Universal behavior of the mobility: extraction of the parameter η in FDSOI devices

In previous part, the experimental mobility has been plotted as a function of the inversion charge. It is however more convenient, for technology comparison, to plot it as a function of the effective field using equation 2.7. This raises the question of the extraction of the parameter η. A recent paper has shown that the value of η in FDSOI devices may be different from bulk values [97]. Although, this parameter is usually extracted by adjusting experimental curves in order to get the best universal trend, an alternative technique has been recently proposed, deducing η from the following formula [98]:

$$\eta_{SiOI} = \frac{AC_{box}}{AC_B - C_{ox}} \text{ with } A = \frac{(\partial \mu_{eff}/\partial V_{fg})\big|_{V_{bg}}}{(\partial \mu_{eff}/\partial V_{bg})\big|_{V_{fg}}} \quad (2.8)$$

This method is used to extract η at VB=0 V for various temperatures (Figure 42a), leading to η = 0.42 and 0.36 for n- and p- FDSOI devices respectively. This can also be seen in Figure 42b where η has been characterized for devices with various IL EOT.

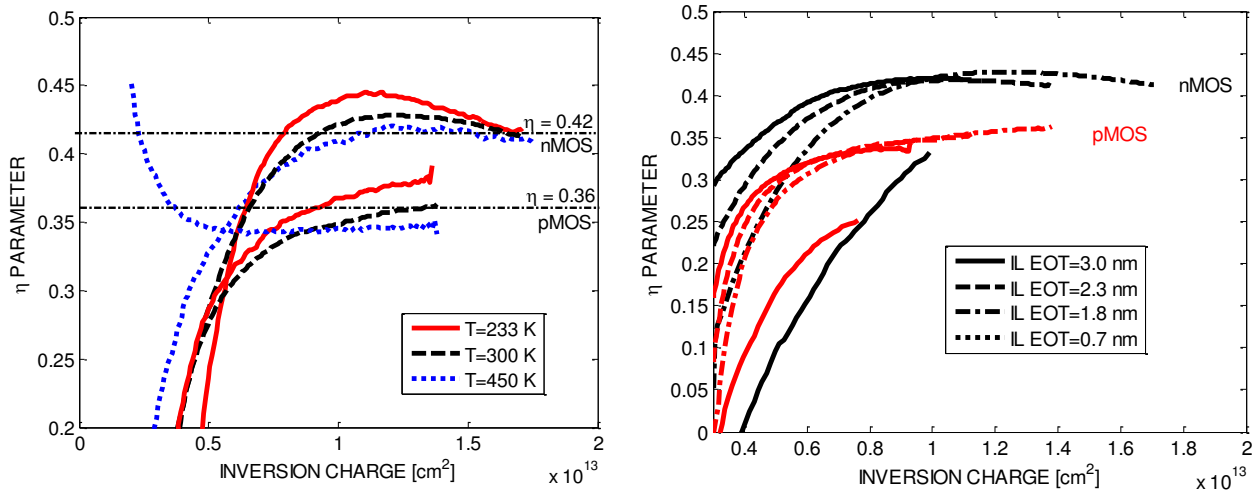

Figure 42 : Extracted value of parameter *η using Eq.* 2.8 in n- and pFDSOI devices for various temperatures (T=233, 300 and 450 K). nFDSOI device: IL EOT = 1.8 nm. The domain of validity corresponds to the strong front inversion regime. VB=0 V.

Using these extracted values η = 0.42 and 0.36, the experimental mobility has been plotted as a function of the effective field (Figure 43). It can be noticed that using these extracted parameters and equation 2.7 for the definition of the effective field, the universal trend cannot be obtained on the whole range of VB. Moreover, it ought to be noticed that equation 2.8 is valid only when the front interface is in the strong inversion regime [98]. However it can be interesting to apply this equation with reverse VB (VB>0 V for nFDSOI and VB<0 V for pFDSOI devices) since at high gate voltages the front channel is also inverted. In Figure 44, η has been extracted for VB varying from -10 V to 10 V in n- and p- FDSOI devices. In the front inversion regime, η converge to the previously extracted values while in the back inversion regime, an increase of the coefficients with VB can be observed. As expected when the front channel is not inverted, equation 2.8 is not valid and the extraction of η is not relevant.

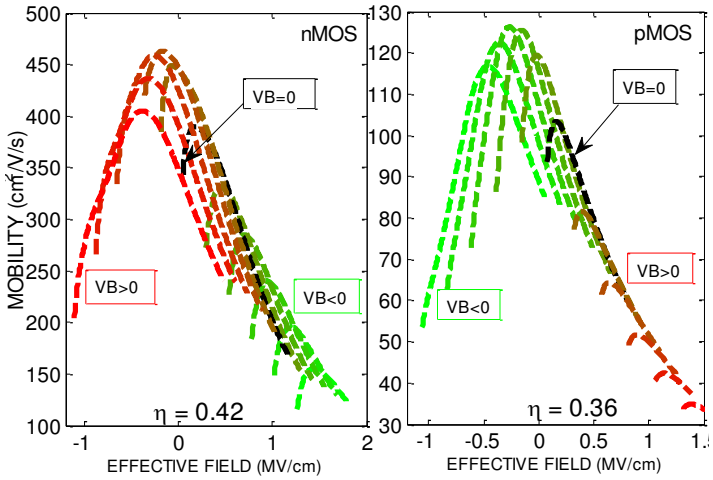

Figure 43 : n- (left) and p- (right) FDSOI experimental effective mobility as a function of the effective field. VB ranging from -10 V to 10 V in steps of 2 V. Effective field calculated using Eq. 2.7 *(η=0.42 for nFDSOI and η=0.36 for pFDSOI). IL EOT = 1.8 nm. T=300 K.*

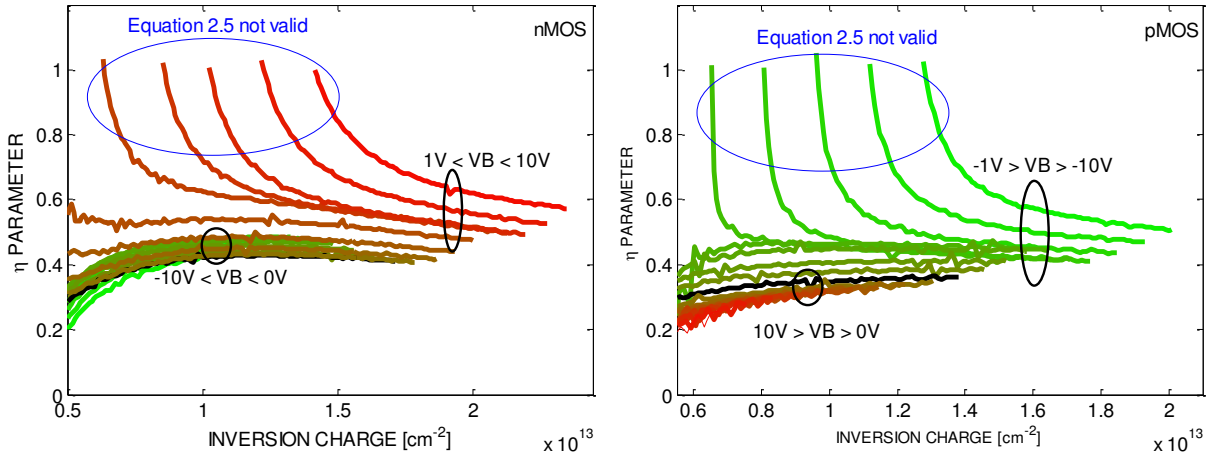

Figure 44 : *Extracted value of parameter η using Eq.* 2.8 in a nFDSOI device for various VB ranging from -10 *V to 10 V. IL EOT = 1.8 nm. T=300 K. In the front inversion regime (VB<0), η=0.42 while in the forward regime (VB>0), η varies significantly with VB.*

There is another aspect to mention concerning the key assumption behind equation 2.8. This equation is based on the assumption [98]:

$$(\partial\mu_{eff}/\,\partial E_{eff})|_{V_{bg}} = (\partial\mu_{eff}/\,\partial E_{eff})|_{V_{fg}} \qquad (2.9)$$

In order to check the validity of this formula, in Figure 45 the mobility has been plotted with respect to the effective field sweeping VB at fixed VG and sweeping VG at VB=0 V. The condition described in equation 2.9 is not satisfied at high E_{eff}. In order to get a better agreement, η also has been re-extracted by brute-force numerical fitting, leading to the value of η=0.62 for nFDSOI and η=0.5 for pFDSOI devices. Results are shown in Figure 46.

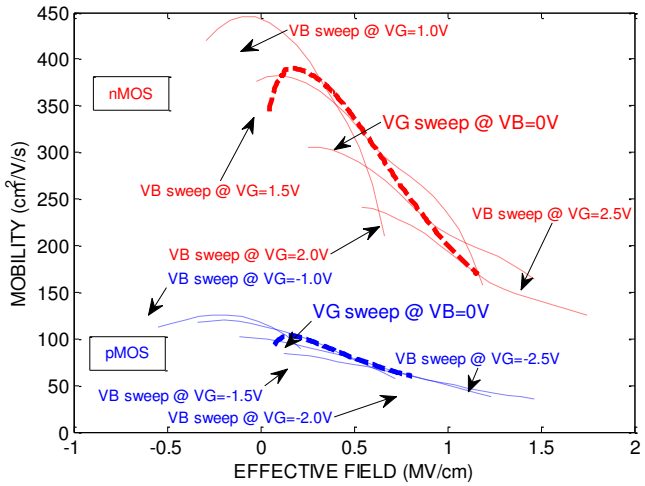

Figure 45 : n- and p- FDSOI experimental effective mobility as a function of the effective field sweeping the back terminal or the gate terminal. Eq.2.7 has *been used for the evaluation of the effective field with η=0.42 for nFDSOI and η*=0.36 for pFDSOI devices. IL EOT = 1.8 nm. T=300 K.

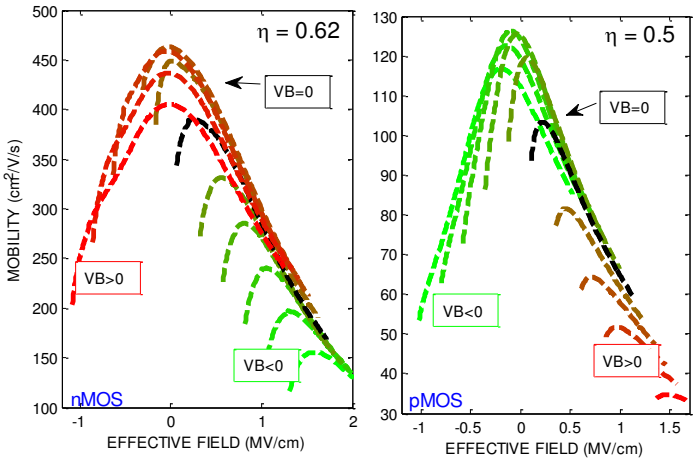

Figure 46 : n- (left) and p- (right) FDSOI experimental effective mobility as a function of the effective field. VB ranging from -10 V to 10 V in steps of 2 V. Effective field calculated using Eq. 2.7 *(η=0.62 for nFDSOI and η=0.5 for pFDSOI). IL EOT = 1.8 nm. T=300 K.*

A nearly universal trend for the mobility with respect to E_{eff} can be obtained only in a limited range of VB. Indeed, in reverse VB conditions, there is no single value of η resulting in universal mobility versus effective field curves. The coexistence of multiple channels and the difference of interfaces (front and back) quality make difficult to apply the same procedure than in bulk devices for the full range of gate and back voltages.

II.4 Calibration for empirical solvers and comparison to measurements

II.4.1 Process simulation in TCAD

An accurate description of the process steps is done using the commercial software Sentaurus Process [66] from SYNOPSYS (Figure 47). In a first step the stress is considered as negligible as there is no major stressor such as SiGe channel or SiGe source and drain, in 28FDSOI technology. The stress model calibration will be studied in a second time for the 14FDSOI technology.

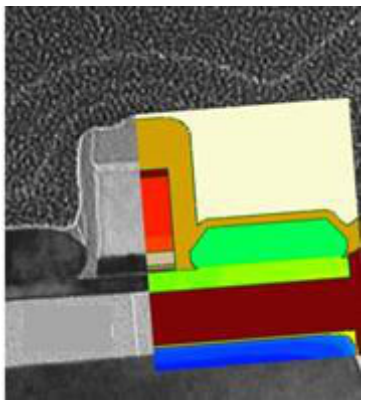

Figure 47 : TEM cross-section superimposed to a process simulation of a UTBB-FDSOI device.

II.4.2 TCAD empirical mobility model calibration

As already mentioned, carrier transport in TCAD softwares (all simulations shown here are performed with Sentaurus Device –Sdevice [66]) is determined using empirical models which depend on a series

of unknown parameters that have to be calibrated. Among electrostatic and transport models, one can mention: 1) the density gradient-based quantum correction; 2) the model accounting for saturation of carrier velocity with high fields and; 3) mobility models for each single scattering mechanisms (phonon, local coulomb, remote coulomb, surface roughness...) which are then combined using the Matthiessen's rule (The syntaxes for all mobility models is shown in Annex 2). It is important to notify that these mobility models depend on the "local" electric field or the "local" carrier density and neglect non local effects such as the channel thickness. Consequently, additional mobility models are introduced to emulate these non-local effects. A recent model accounting for the mobility degradation in thin channel at both front and back interfaces has been developed in [99]. Details about this model are well documented in [100] and the parameters have been carefully calibrated in [100]. This calibration is used in the present study. In the part below let us give details about some of the mobility models.

- The surface roughness-limited mobility is given by:

$$\mu_{SR} = \left(\frac{(F_{\perp}/F_{ref})^{A^*}}{\delta} + \frac{F_{\perp}^3}{\eta} \right)^{-1} \tag{2.10}$$

A calibration of the SR parameters was mandatory to better reproduce measurements ($\delta = 2.5 \times 10^{18}$ cm²/Vs, $\eta = 1 \times 10^{50}$ V²/cm/s for nMOS and $\delta = 4.10 \times 10^{15}$ cm^2/Vs, $\eta = 5.82 \times 10^{31}$ V²/cm/s for pMOS in equation 2.10).

- The remote Coulomb-limited mobility was modeled using the following equation [100]:

$$\mu_{RC} = \frac{\mu_1 (1 + (c/c_{trans})^{v})}{\left(\frac{N_C}{N_0}\right)^{\eta 2} . D} \tag{2.11}$$

with $D = \exp(-\frac{x}{l_{crit}})$. x is the distance from high-k/IL interface, N_C is the negative or positive interface charge density, c is the local carrier concentration in the channel and the other terms are fitting parameters.

- The carrier bulk mobility, i.e. phonon and coulomb-limited mobility is introduced through the Philips unified mobility model proposed by Klaassen [96]

$$\frac{1}{\mu_{Klaassen}} = \frac{1}{\mu_{ph}} + \frac{1}{\mu_{lc}}, \tag{2.12}$$

where the phonon component is expressed as:

$$\mu_{ph} = \mu_{max} \left(\frac{T}{300K} \right)^{-\theta_i} \tag{2.13}$$

Holes and electrons parameters are listed in Table 9. The local coulomb component may be further represented as a composition of two terms $\mu_{lc} = \mu_{IN} + \mu_{IC}$ with

$$\mu_{IN} = \frac{{\mu_{max}}^2}{\mu_{max} - \mu_{min}} \left(\frac{N_{REF,1}}{N_{II}} \right) \left(\frac{T}{300K} \right)^{-3\alpha - 1.5}, \tag{2.14}$$

and

$$\mu_{IC} = \frac{\mu_{max}\,\mu_{min}}{\mu_{max} - \mu_{min}} \left|\frac{n-p}{N_{II}}\right| \left(\frac{T}{300K}\right)^{0.5} \quad (2.15)$$

Parameter	Electrons (arsenic)	Electrons (phosphorus)	Holes (boron)	Unit
μ_{max}	1417	1414	470.5	cm^2/Vs
μ_{min}	52.2	68.5	44.9	cm^2/Vs
θ_i	2.285	2.285	2.247	1
$N_{REF,1}$	9.68×10^{16}	9.2×10^{16}	2.23×10^{17}	cm^{-3}
α	0.68	0.711	0.719	1

Table 9 : Parameters for Philips unified mobility model for electrons and holes [100].

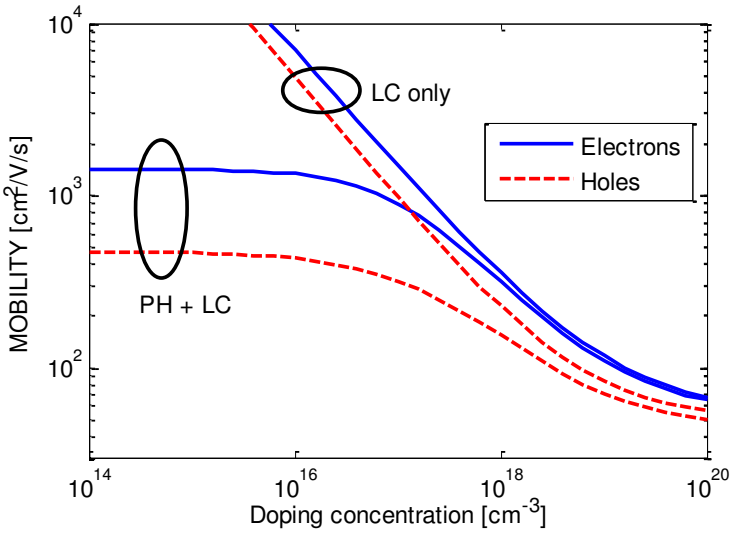

Figure 48 : PH + LC and LC-limited mobility determined using Philips unified mobility model.

The results for the model for local coulomb-limited mobility are illustrated as a function of the doping concentration in Figure 48. Then, the calibrated remote Coulomb-limited mobility model (equation. 2.11) is compared to KG results. Figure 49 shows the variation of the nMOS RC mobility with respect to the inversion charge for various high-k/IL interface charge densities (Figure 49a) and for various IL EOT (Figure 49b). The calibrated empirical model reproduces well the mobility determined with KG solvers. Similarly, RC-limited mobility has also been calibrated for pMOS in Figure 50.

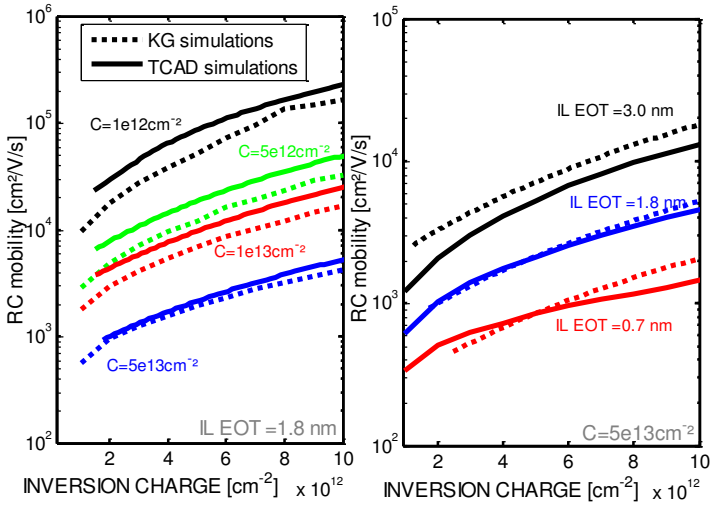

Figure 49 : nMOS effective remote Coulomb-limited electron mobility in FDSOI devices as a function of the inversion charge. KG and TCAD simulations are performed a) for various high-k/IL interface charge density in a device with IL EOT= 1.8 nm and b) for various IL EOT for a fixed interface charge density C=5× $\mathbf{10^{13}}$ cm-2. Tsi=7.5 nm; T=300 K. TCAD model parameters: $\mu_1 = \mathbf{493}$ cm²/V/s, $\boldsymbol{c_{trans}} = \mathbf{1 \times 10^{18}}$ cm^{-3},$\boldsymbol{\nu} = \mathbf{1.4}$, $\boldsymbol{\eta 2} = \mathbf{1}$, $\boldsymbol{l_{crit}} = \mathbf{1.25 \times 10^{-7}}$ $\boldsymbol{cm}$. Phonons parameters of Table 7 for KG solvers.

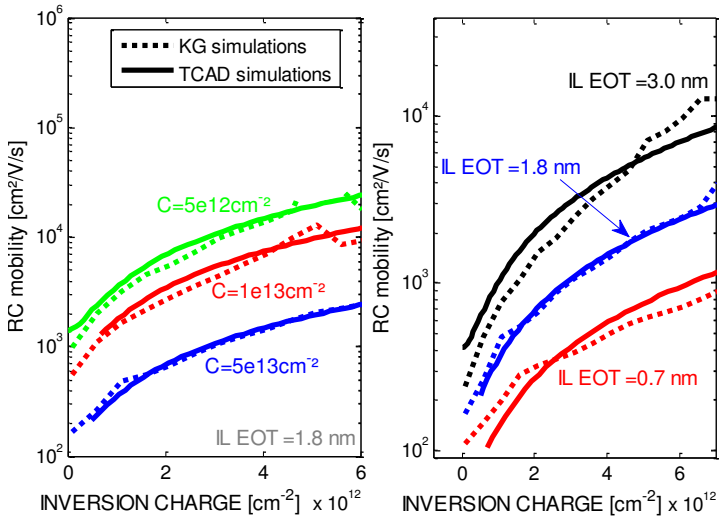

Figure 50 : Same as Figure 49 but for holes. TCAD models parameters: $\mu_1 = \mathbf{454}$ cm²/V/s, $\boldsymbol{c_{trans}} = \mathbf{1 \times 10^{18}}$ cm-3, $\boldsymbol{\nu} = \mathbf{1.6}$, $\boldsymbol{\eta 2} = \mathbf{1}$, $\boldsymbol{l_{crit}} = \mathbf{1.5 \times 10^{-7}}$ $\boldsymbol{cm}$.

II.4.3 Comparison to Experimental data

In order to investigate the accuracy of calibrated TCAD models, the total mobility for nMOS is then simulated using TCAD and KG solvers (parameters in Table 10) varying the IL EOT (Figure 51a) and the temperature of the device (Figure 51b).

	Band structure	**phonon**	**Surface roughness**	**Remote Coulomb**
Electron	parabolic band structure	Parameters of Table 7	Exponential Autocorrelation *Δ_{SR}=0.47 nm and Λ_{SR}*=1.3 nm. Scalar Lindhard screening.	Tensorial Lindhard screening. Charge density at high-k/IL interface: 3×10^{13} cm^{-2}.
Hole	six-bands k.p model	Parameters of Table 8	Exponential Autocorrelation *Δ_{SR}=0.40 nm and Λ_{SR}*=1.3 nm. Scalar Lindhard screening.	Tensorial Lindhard screening. Charge density at high-k/IL interface: 6×10^{13} cm^{-2}.

Table 10 : Simulation parameters for KG solvers.

Concerning nMOS, a charge density of 3×10^{13} cm^{-2} at high-k/IL interface is used to fit experimental data and excellent agreements are found between solvers and experimental data. This charge density theoretically leads [88] to a variation of VTH of nearly 0.45 V.

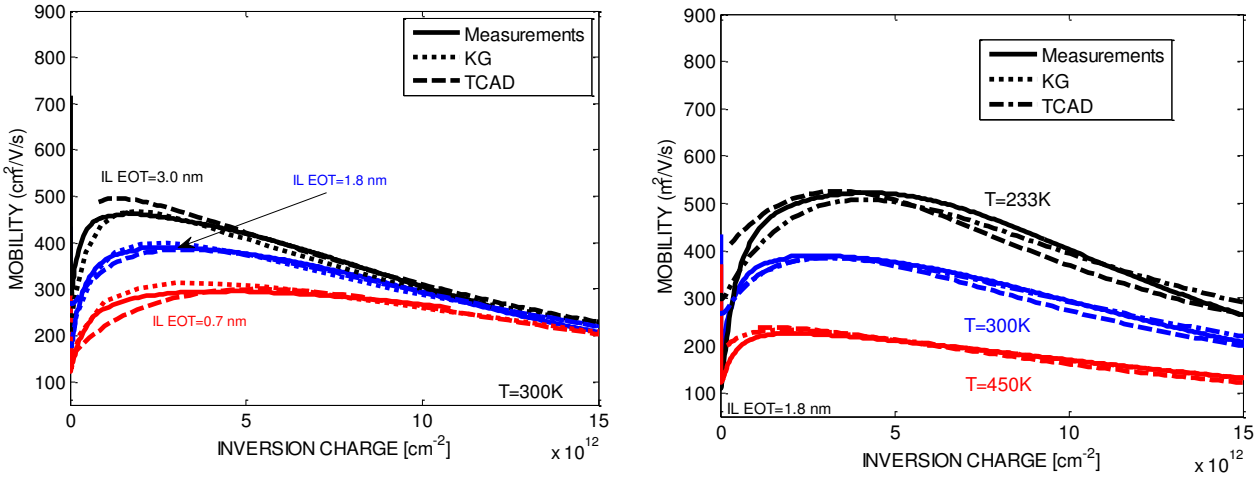

Figure 51 : n-MOS mobility as a function of the inversion charge a) for structures with various IL EOT or b) at different temperatures. Comparison between TCAD, KG solvers and experiments.

These simulations have been also performed for pMOS devices, see Figure 52, using a charge density of 6×10^{13} cm^{-2} at high-k/IL interface. In TCAD, the slight underestimation of the mobility variation with temperature can be due to the fact that our remote coulomb and surface roughness-limited mobility models neglect the variation with the temperature.

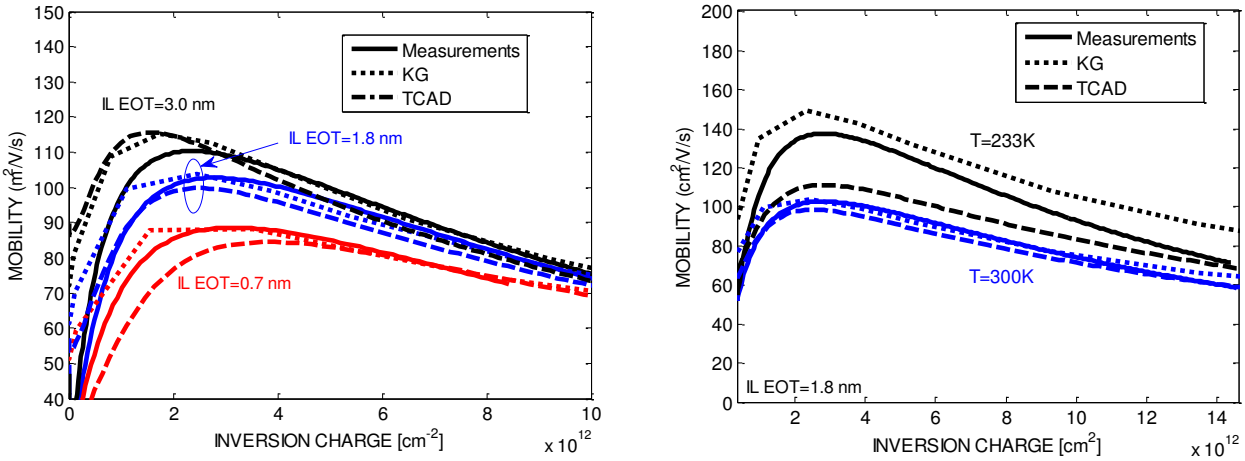

Figure 52 : p-MOS mobility as a function of the inversion charge for structures with various IL EOT a) or at different temperatures b) Comparison between TCAD, KG solvers and experiments.

The total mobility is then extracted as a function of the IL EOT, at $N_{inv} = 2\times 10^{13}$ cm^{-2} (Figure 53a). Good agreement is found for IL EOT>1 nm for both devices. The degradation of the mobility with the IL thickness is well captured by considering remote Coulomb scattering only. This tends to suggest that remote phonon and remote surface roughness have a negligible impact for IL EOT>1 nm.

Figure 53b illustrates the variation of the mobility with the temperature for various inversion charges and for n- and pMOS. The mobility degradation (due to the increase of phonon scattering) with increasing temperatures is well reproduced by simulations for both devices.
As an ultimate benchmark, the variation of the mobility with VB is accurately accounted for, as testified by Figure 54. As can be seen, the experimental behavior (depicted in Figure 36) is well captured by KG solvers but also by TCAD simulations.

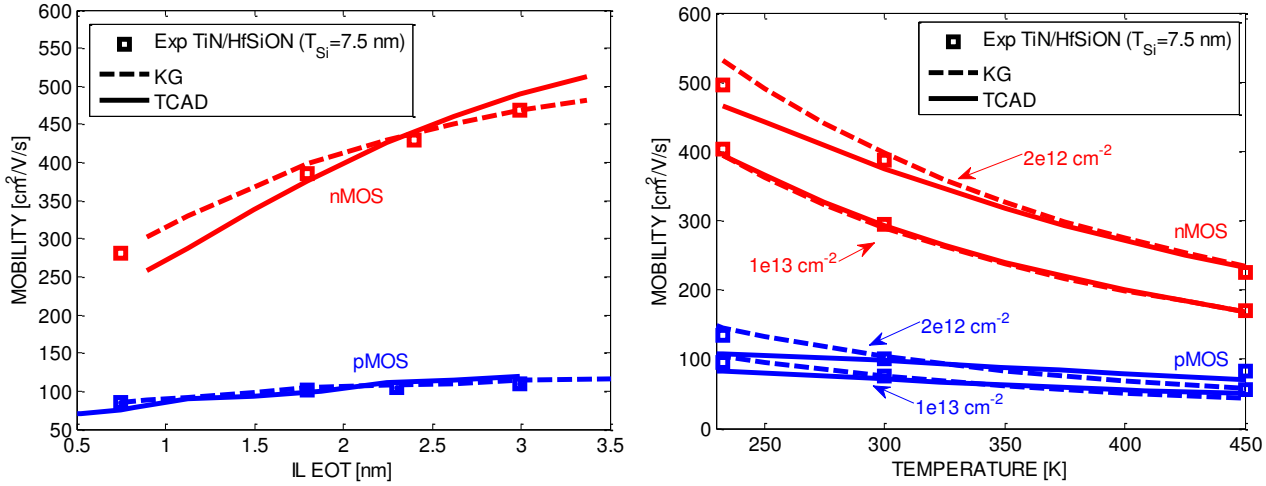

Figure 53 : n- and pMOS mobility extracted at fixed inversion density as a function of a) the IL EOT b) the Temperature. Comparison between TCAD, KG solvers and experiments.

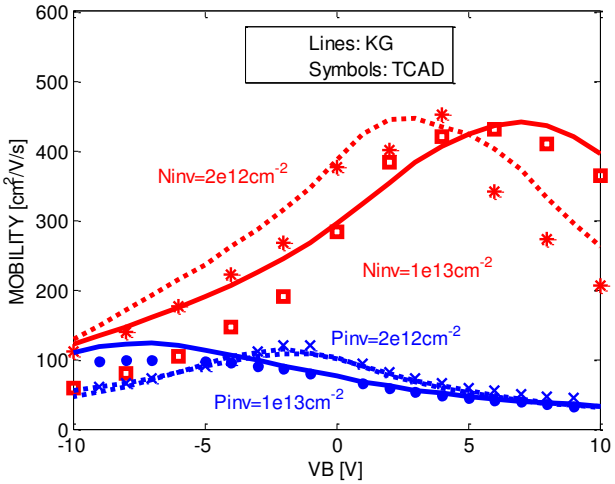

Figure 54 : Simulated effective mobility as a function of the back bias for various inversion densities: N_{inv}= 1× **10**^{13} and 2× **10**^{12} cm^{-2}. T_{inv}=2.65 nm; T_{Si}=7.5 nm; T=300 K.

II.5 Conclusion

In the first part of this chapter the electron and hole mobilities have been calculated using four different solvers: the STMicroelectonics in-house solver (UTOXPP), the commercial solver Sband from Synopsys, the MSMC solver from the University of Udine and TB_SIM, the NEGF solver from the CEA. Concerning electrons mobility, good correlations were found between all solvers comparing phonons and RC-limited mobilities. However, due to assumptions behind the GPN model, semi-classical solvers (KG and MSMC) strongly overestimate the SR-limited mobility compared to NEGF.
The comparison of holes mobility showed a clear underestimation of the phonon-limited mobility using KG solvers compared to NEGF and a different dependence of SR-limited mobility with the silicon thickness.

The second part of this chapter has been dedicated to the comparison between simulations and experiments, performed on state of the art FDSOI devices. Using a large range of split-CV measurements, the impact of the Equivalent Oxide Thicknesses (EOT), the back voltage and the temperature have been investigated. In the last part, we showed that, after being calibrated on advanced transport solvers, TCAD empirical models can accurately reproduce experimental results. This enables accurate and efficient TCAD simulations of UTBB FDSOI MOSFETs in state of the art CMOS technology.

Chapter III:

Mechanical simulations of the process-induced stress in 14FDSOI MOSFETs and comparison with nanobeam diffraction strain measurements

III.1 Introduction

As the happy scaling era is now finished since a long time, boosters have become more and more important in order to maintain the historical performance improvement. Providing a low-cost and low-risk solution, strain engineering is one of the dominant technique to enhance device performance maintaining the traditional MOSFET manufacturing process flow. The strain technologies can be divided into two groups (Figure 55): the global techniques where the stress is introduced into the whole wafer, and local techniques, where stress is delivered to each transistor separately and independently. Local stress techniques to enhance MOSFETs performance was first incorporated by Ito et al. [101] and Shimizu et al. [102] who used a contact etch-stop layer (CESL) or by Gannavaram et al. [103] who used SiGe source and drain region in the early 2000s. Since the 90-nm technology node, uniaxial stress was successfully integrated to the mainstream MOSFET process flow to improve device performance. Global stress techniques such as strained SiGe channel (epitaxied SiGe layer on Si substrate or SiGe layer formed by condensation [104]) or "strained Silicon On Insulator" (sSOI) [105], are also current technique to enhance carriers mobilities in MOSFETs. Combining these techniques, the stress in the channel can reach values between -1 and -2 GPa (uniaxial or biaxial) leading to drastic changes of the mobility (e.g. by a factor of 2.5 to 3 for <110> oriented-channel p-type MOSFET) [106]. Consequently, in TCAD, the prediction of the performance of strained-Si UTBB FDSOI MOSFETs requires an accurate modeling of the stress profile in the transistor but also of the impact of stress on transport properties. The aim of this chapter is twofold. First an accurate description of the methodologies used during this thesis to model stress induced by the process flow is performed. Simulations are compared to nanobeam diffraction (NBD) strain measurements. The second aim is to study and calibrate (on advanced transport solvers) available TCAD models to efficiently account for the influence of stress on mobility in a large range of stress (up to 2GPa).

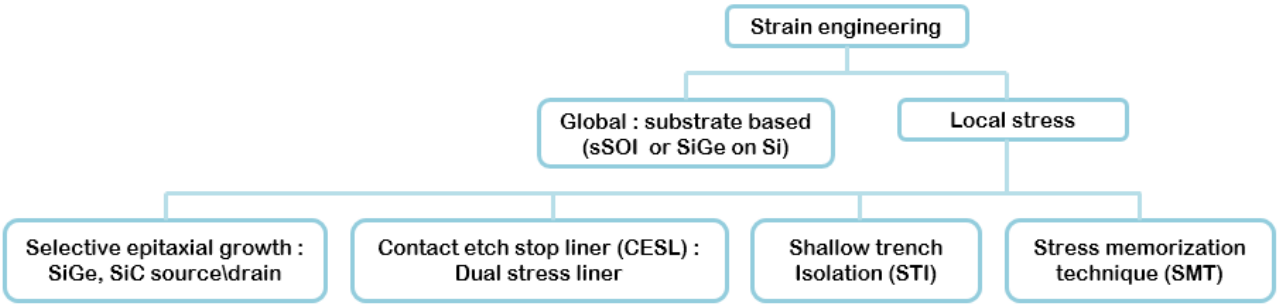

Figure 55 : Classification of stress techniques.

In the first part of this chapter, we review the methodologies to calculate the mechanical stress in FDSOI transistors using a solver based on the finite difference method (Sprocess from SYNOPSYS). We focus on the description of the boundary conditions, materials mechanical behaviors and the process-induced stress. Then, in the second part, we presented an accurate description, study and calibration of TCAD stress-dependent mobility models.

III.2. Methodology for mechanical stress modeling

The modeling of the mechanical stress using the finite difference method is usually performed in four different steps. First, the boundary conditions for the equations of mechanics are defined for each side of the simulation domain (Dirichlet or Neumann boundary conditions). Second, mechanical properties

and their rheological behaviors are fixed for each material. This mainly consists in setting the relationship between stresses and strains (elastic, viscous, plastic, viscoelastic laws). Third, all elementary steps of the process flow are described (epitaxy, deposit, etching, oxidation, thermal anneal…) and finally, the resolution of the equations of mechanics is done at each point of the simulation mesh. In this section, we review the main approaches used during this thesis for mechanical stress simulations in FDSOI devices.

III.2.1 Generality about stress and strain tensors

- **Expression of the stress tensor**

A mechanical stress represents a force per unit area and is expressed in Pa or N/m^2 in the international system. By convention, a tensile stress component is positive and a compressive stress component is negative. In an infinitesimal cubic volume element (represented in Figure 56), the stress is described by a second-rank stress tensor σ_{ij} which can be expressed as:

$$\sigma_{ij} = \begin{bmatrix} \sigma_{xx} & \sigma_{xy} & \sigma_{xz} \\ \sigma_{yx} & \sigma_{yy} & \sigma_{yz} \\ \sigma_{zx} & \sigma_{zy} & \sigma_{zz} \end{bmatrix} \quad (3.1)$$

Stress components σ_{ii} are normal stress components and stress σ_{ij} with $i \neq j$ are shear stress components.

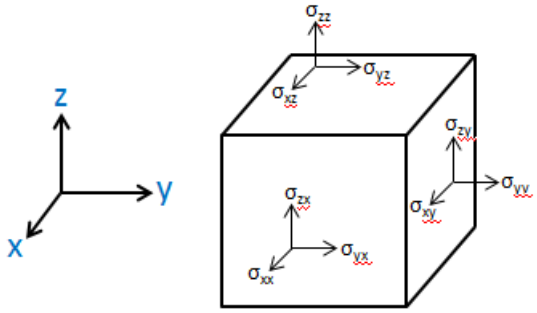

Figure 56 : Definition of the stress tensor components. The first subscript refers to the direction normal to the face on which the stress is applied. The second subscript corresponds to the direction of the stress.

At equilibrium, the stress tensor σ_{ij} is symmetrical ($\sigma_{ij} = \sigma_{ji}, \text{for } i \neq j$) [129] and reduces to six independent components. Thus, it can be simplified in the following vector:

$$\sigma_{ij} = \begin{Bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{xy} \\ \sigma_{yz} \\ \sigma_{xz} \end{Bmatrix} \quad (3.2)$$

Each tensor can be decomposed in a sum of two tensors: a hydrostatic part ($[\sigma_{ij}]^h$) which describes the material behavior in the case of a pure volume change and a deviatoric part ($[\sigma_{ij}]^d$) which describes an

arbitrary stress leading to the distortion of the material without volume change. These two tensors can be described as

$$\sigma_{ij}{}^{hyd} = \begin{bmatrix} \sigma_{hyd} & 0 & 0 \\ 0 & \sigma_{hyd} & 0 \\ 0 & 0 & \sigma_{hyd} \end{bmatrix} \text{ with } \sigma_{hyd} = \frac{tr(\sigma_{ij})}{3} = \frac{\sigma_{xx}+\sigma_{yy}+\sigma_{zz}}{3} \tag{3.3}$$

and $\sigma_{ij}{}^{dev} = \sigma_{ij} - \sigma_{ij}{}^{hyd}$

$$\text{so } \sigma_{ij}{}^{dev} = \begin{bmatrix} \frac{2\sigma_{xx}-\sigma_{yy}-\sigma_{zz}}{3} & \sigma_{xy} & \sigma_{xz} \\ \sigma_{yx} & \frac{2\sigma_{yy}-\sigma_{xx}-\sigma_{zz}}{3} & \sigma_{yz} \\ \sigma_{zx} & \sigma_{zy} & \frac{2\sigma_{zz}-\sigma_{xx}-\sigma_{yy}}{3} \end{bmatrix} \tag{3.4}$$

It is important to notice that the rheological behaviors of these two tensors can be treated differently in simulation as explained later in the manuscript.

- **Strain tensor:**

Identically to the stress tensor, the strain tensor can be defined as

$$\epsilon_{ij} = \begin{bmatrix} \epsilon_{xx} & \epsilon_{xy} & \epsilon_{xz} \\ \epsilon_{yx} & \epsilon_{yy} & \epsilon_{yz} \\ \epsilon_{zx} & \epsilon_{yx} & \epsilon_{zz} \end{bmatrix} \tag{3.5}$$

and simplified in a vector form as:

$$\epsilon_{ij} = \begin{Bmatrix} \epsilon_{xx} \\ \epsilon_{yy} \\ \epsilon_{zz} \\ \epsilon_{xy} \\ \epsilon_{yz} \\ \epsilon_{xz} \end{Bmatrix} \tag{3.6}$$

with $\epsilon_{ij} = \frac{1}{2}\left(\frac{\partial u_j}{\partial x_i} + \frac{\partial u_i}{\partial x_j}\right)$

∂u is an infinitesimal vector deformation due to the stress on a infinitesimal distance ∂x.

The strain tensor can also be decomposed in hydrostatic and deviatoric parts:

$$\epsilon_{ij} = \epsilon_{ij}{}^{hyd} + \epsilon_{ij}{}^{dev} \tag{3.7}$$

The modifications of the electrical properties of a material are governed by the strain tensor. In particular, concerning the band structure, a hydrostatic stress modifies the lattice parameter only leading to a uniform shift of all the energy bands as described in chapter I. This component does not modify the bands population neither their effective mass but can lead to modification of the band gap. In contrast, the deviatoric component breaks the symmetry of the crystal leading to strong modifications of the band structure (band population, effective mass…).

III.2.3 Boundary conditions

- **Boundary conditions for 2D simulations**

Common boundary conditions (BC) are of two types: Dirichlet and Neumann conditions. Dirichlet BC fixes the value of the unknown solution (i.e. the displacement) on the side where it is applied whereas Neumann BC forces the derivative of the solution (i.e. the velocity) to be constant.

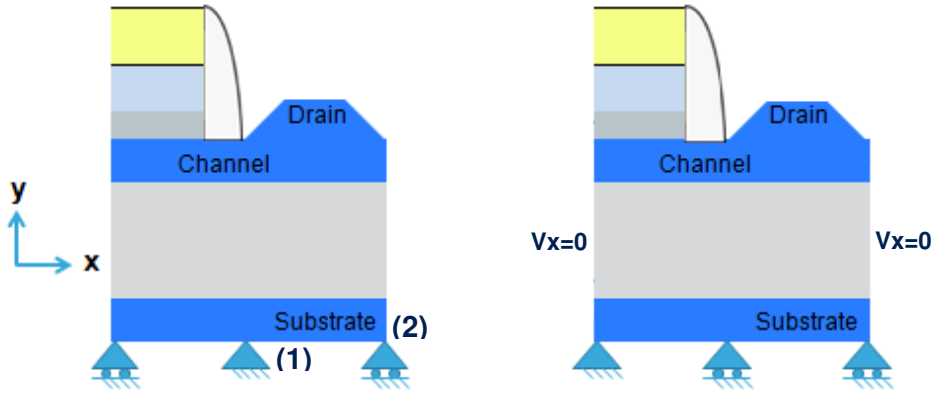

Figure 57 : Main boundary conditions (BC) in 2D. Left*) "Free" BC that implies a zero normal stress on each* side. Right) Dirichlet BC applied on each side of the simulation domain. (1) corresponds to a fixed point and (2) restricts the displacement to one direction.

Figure 57 shows two available configurations for BC. In the first case Neumann conditions are applied on the two sides of the simulation domain making them "free" (Figure 57a). This configuration is usable if the left and right sides of the simulation domain correspond to the physical limits of the structure. In the second case, Dirichlet conditions are applied on each side of the simulation domain (Figure 57cb). This condition imply a zero velocities in the direction perpendicular to the boundary planes. Note that all configurations require a fixed point as show in Figure 57. During this thesis, we applied the second configuration for all simulations.

- **Assumptions for 2D simulations:**

In FDSOI technology, due to the incorporation of SiGe alloy for pMOSFET channel, the stress is biaxial and can reach values between -1 and -2 GPa which can consequently change the mobility. Moreover, due to layout effects and stress relaxation (explained more in details in chapter IV), the stress in the width direction strongly depends on the dimension of the structure as testified in Figure 58. Thus, three-dimensional simulations should be performed to account for all these effects but are more CPU time consuming. In two-dimensional simulations, the third direction can be treated within two different approximations: a) in the "plane strain" analysis, the width is considered as infinite and no relaxation of the stress occurs; b) in the "plane stress" analysis, the width is considered as very small, so the stress component in this direction is null. Consequently, an intermediate solution is needed to emulate the stress relaxation due to layout effects in 2D. All 2D simulations are performed under plane strain assumption and the stress in the width direction is directly set to the "relaxed values" of Figure 58 (after Shallow Trench Isolation –STI- process steps) instead of the theoretical value given by the germanium concentration in the channel (equation 3.21 and red curve in Figure 58). This technique allows to emulate the relaxation of the stress in the width direction.

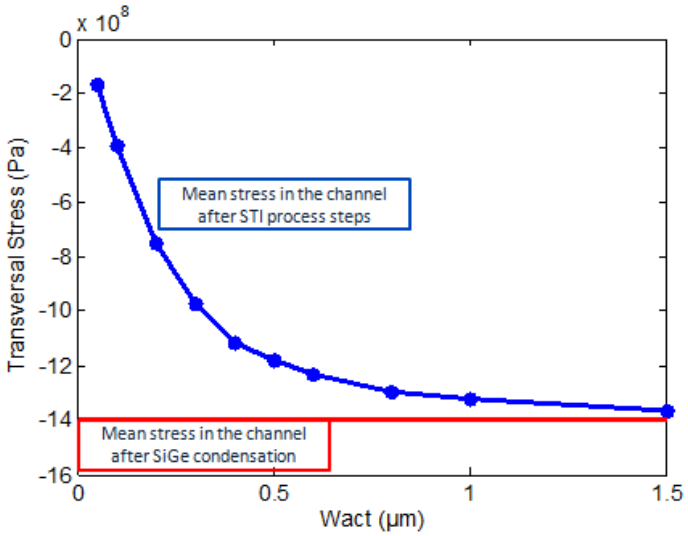

Figure 58 : Evolution of the stress with the width dimension. This stress value corresponds to the mean stress in the channel after the STI process steps.

This method assumes that the relaxation of the stress in the width direction do not influence the stress profile in the length direction: there is no or a low correlation between stress profiles in these two directions. To check this assumption, we performed 3D simulations on four different structures with varying dimensions as represented in Figure 59. A 2D cut in the plane perpendicular to the width direction is realized (Figure 60a) and then the longitudinal and transversal stresses are extracted along the channel direction (1D cut in the channel shown in Figure 60b). In Figure 61a, we can notice that a strong degradation of the transversal stress (σ_w) occurs for the two thinnest structures (W=0.06 µm). Figure 61b shows that this relaxation of the stress in the W direction has a low influence on the stress profile in the L direction, so the assumption is validated.

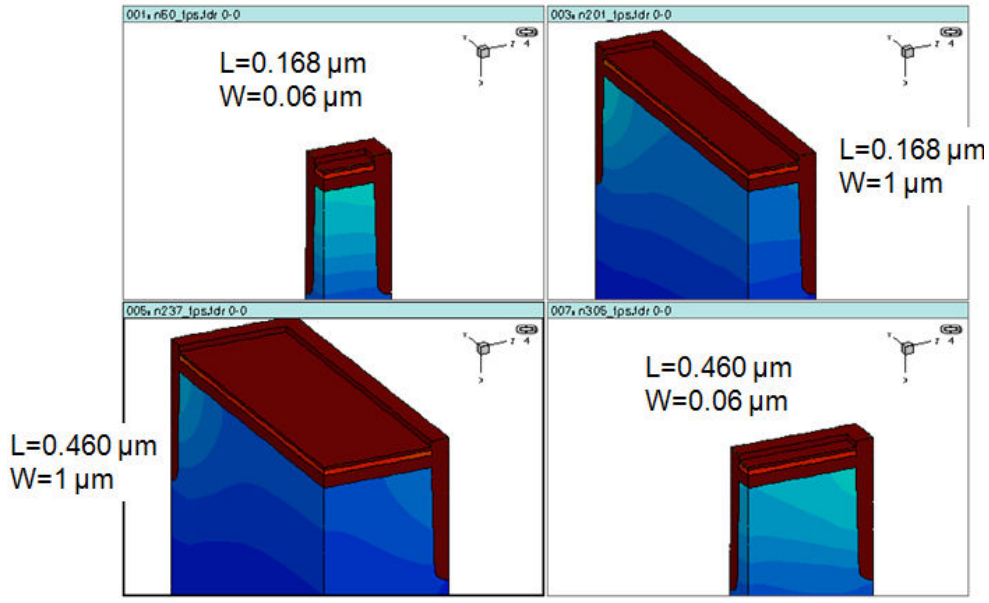

Figure 59 : 3D TCAD simulations of FDSOI devices with varying dimensions after STI process steps.

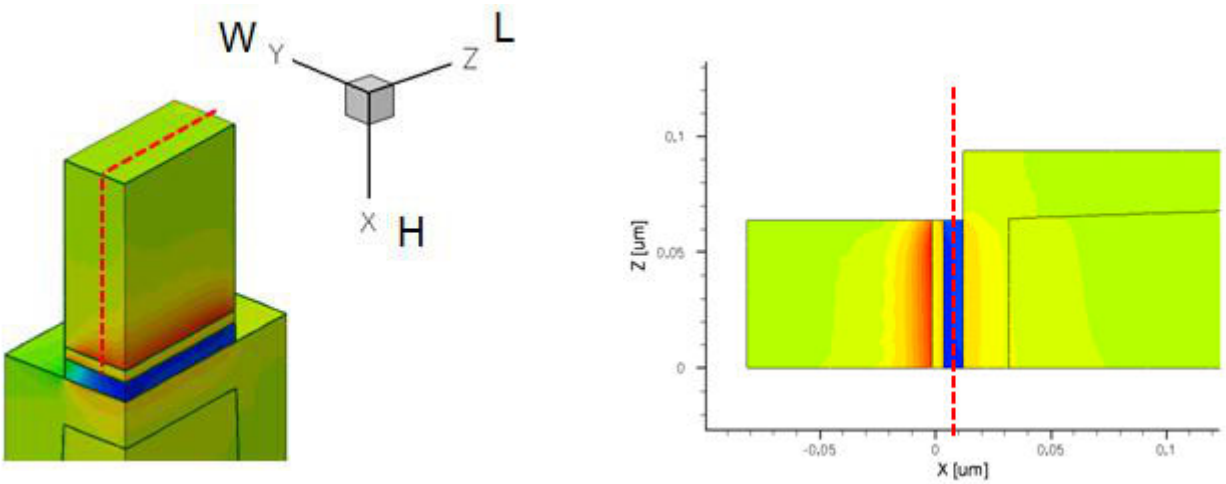

Figure 60 : a) 3D TCAD simulations of the longitudinal stress in the device. The dashed lines represent the different 2D cuts of the structure. (b) 2D cut of the device. The dashed line represents the 1D cut of the structure along the channel.

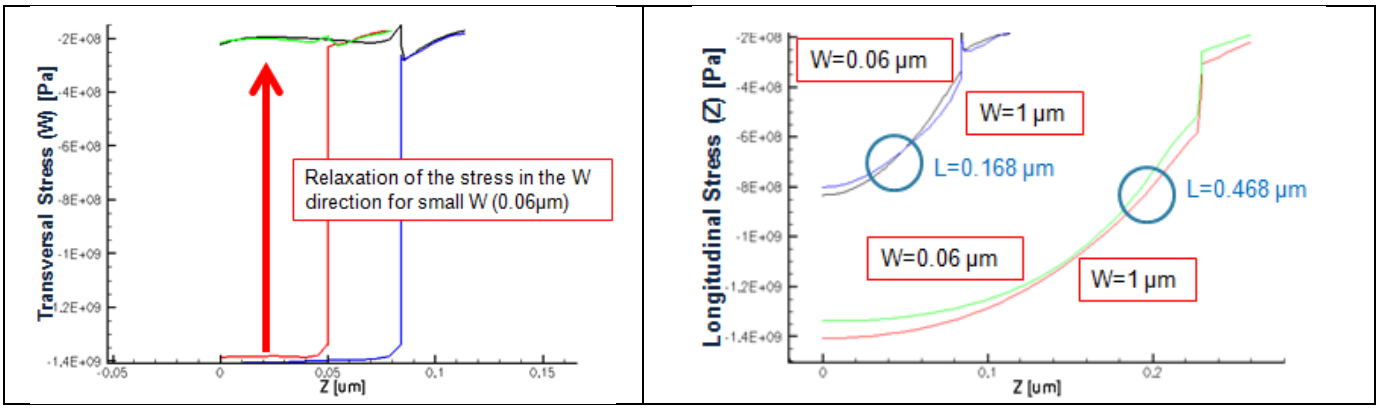

Figure 61 : Simulation of the (a) transversal and (b) longitudinal stress profile in the channel. Profile of Figure 60.

III.2.4 Material properties for mechanical stress simulations

State of the art semiconductors technologies require the use of several thin film materials with varying mechanical properties (semiconductor, oxides, metals…). The rheological behavior of these materials (i.e. the relation between stress and strain) and their mechanical properties must be described and defined before each simulation. In this part, we define the most widely encountered material rheological behaviors in microelectronics, namely elastic, viscoelastic and plastic laws.

- **Linear elasticity:**

A large number of materials follow the elasticity law at low stress value. This behavior results in a linear relation between the strain of the material and the applied stress. Usually represented as a spring with a rigidity E (Figure 62), for isotropic material such as amorphous materials (silicon oxide, silicon nitride), the Hooke's law is written as:

$$\sigma = E\,\epsilon \tag{3.8}$$

with E the Young modulus.

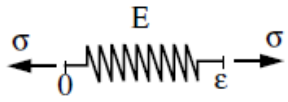

Figure 62 : Schematic of the uniaxial linear elasticity.

For anisotropic materials, such as silicon and germanium, the Hooke's law relates that the stress tensor is linearly related to the strain tensor trough the stiffness matrix C_{ij} :

$$\sigma_{ij} = C_{ijkl}\,\epsilon_{kl} \tag{3.9}$$

and in return, the strain tensor is related to the stress tensor through the compliance matrix S_{ijkl}:

$$\epsilon_{ij} = S_{ijkl}\,\sigma_{kl} \tag{3.10}$$

So, in the crystal coordinate system, the Hooke's law gives:

$$\begin{Bmatrix}\sigma_{xx}\\ \sigma_{yy}\\ \sigma_{zz}\\ \sigma_{xy}\\ \sigma_{yz}\\ \sigma_{xz}\end{Bmatrix} = \begin{bmatrix}c_{11} & c_{12} & c_{12} & 0 & 0 & 0\\ c_{12} & c_{11} & c_{12} & 0 & 0 & 0\\ c_{12} & c_{12} & c_{11} & 0 & 0 & 0\\ 0 & 0 & 0 & c_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & c_{44} & 0\\ 0 & 0 & 0 & 0 & 0 & c_{44}\end{bmatrix} \begin{Bmatrix}\epsilon_{xx}\\ \epsilon_{yy}\\ \epsilon_{zz}\\ \epsilon_{xy}\\ \epsilon_{yx}\\ \epsilon_{xz}\end{Bmatrix} \tag{3.11}$$

and

$$\begin{Bmatrix}\epsilon_{xx}\\ \epsilon_{yy}\\ \epsilon_{zz}\\ \epsilon_{xy}\\ \epsilon_{yx}\\ \epsilon_{xz}\end{Bmatrix} = \begin{bmatrix}S_{11} & S_{12} & S_{12} & 0 & 0 & 0\\ S_{12} & S_{11} & S_{12} & 0 & 0 & 0\\ S_{12} & S_{12} & S_{11} & 0 & 0 & 0\\ 0 & 0 & 0 & S_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & S_{44} & 0\\ 0 & 0 & 0 & 0 & 0 & S_{44}\end{bmatrix} \begin{Bmatrix}\sigma_{xx}\\ \sigma_{yy}\\ \sigma_{zz}\\ \sigma_{xy}\\ \sigma_{yz}\\ \sigma_{xz}\end{Bmatrix} \tag{3.12}$$

At room temperature, the elasticity constants have been determined experimentally and are summarized in Table 11 for silicon [122] and germanium. Concerning Si_xGe_{1-x} alloys, a linear interpolation is used.

Material	Stiffness ($\times 10^9$ Pa)			Compliance ($\times 10^{-13}\ Pa^{-1}$)		
	c_{11}	c_{12}	c_{44}	S_{11}	S_{12}	S_{44}
Silicon	165,7	63,9	79,6	76,8	-21,4	126,0
Germanium	129,2	47,9	67,0	96,4	-26,0	149,0

Table 11 : Compliance and stiffness constants for silicon and germanium [122] [129]

A linear dependence of these coefficients with the temperature has been observed for silicon in [130]:

$$\frac{dc_{11}}{dT} = -75.0 \times 10^{-6}\ {}^{\circ}K^{-1} \tag{3.13}$$

$$\frac{dc_{12}}{dT} = -24.5 \times 10^{-6}\,°K^{-1}$$
$$\frac{dc_{44}}{dT} = -55.5 \times 10^{-6}\,°K^{-1}$$

However, the variation with temperature is very low and is not taken into account in our simulations.

- **Viscoelastic materials**

Generally, amorphous material used in microelectronics (e.g. oxides and nitrides) are elastic at low temperature and become viscous at high temperature. These materials are viscoelastic and are modeled using the Maxwell formalism where a Hookean spring and a Newtonian dashpot are connected in series (Figure 63).

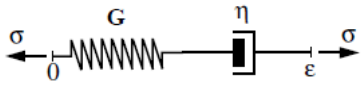

Figure 63 : Schematic of the viscoelastic material behavior corresponding to the Maxwell model.

The spring represents the elastic component of the response ϵ_e while the dashpot represents the viscous component ϵ_v. The total deformation is the sum of the two contributions:

$$\epsilon = \epsilon_e + \epsilon_v \tag{3.14}$$

The elastic part induces an instantaneous deformation of the material and the viscous part a temporal dependence of the response with a time constant of $\tau = \eta/G$. So the equation for the Maxwell element can be written as:

$$\dot{\epsilon} = \frac{\sigma}{G} + \frac{\sigma}{\eta} \tag{3.15}$$

with G the bulk modulus and η the viscosity.

The dependence of the viscosity with the temperature is accounted for using the following expression:

$$\eta(T) = \eta_0 . \exp\left(-\frac{\alpha}{k_B T}\right) \tag{3.16}$$

Parameter	Oxide	Nitride
η_0 [Poises]	5.25×4	2.3×6
α [eV]	-2.42	-2.42

Table 12 : Coefficients for the temperature dependent viscosity model for silicon dioxide and nitride [137].

Values of viscosity used in our simulations (parameters in Table 12) are compared to data from literature in Figure 64. It ought to be notified that these values are dependent on the material, the deposition technique and the presence of impurities in the material.

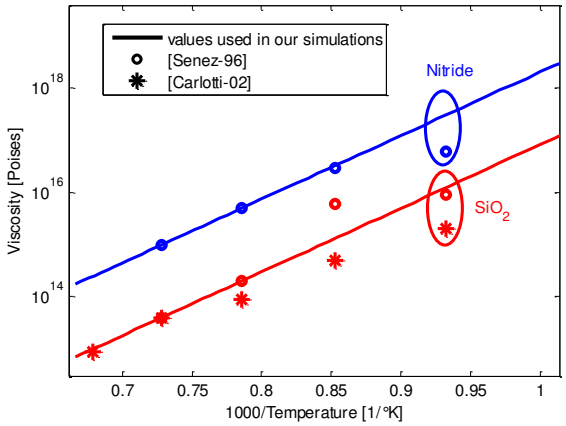

Figure 64 : Silicon oxide and nitride viscosity as a function of 1000/T. Comparison between the values used in our simulations and measurements from literature ([Senez-96]: [137] and [Carlotti-02]: [138]).

- **Plasticity of silicon**

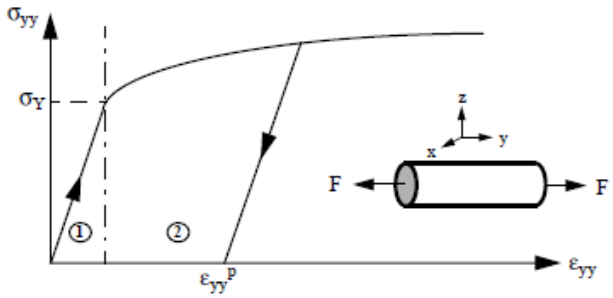

Figure 65 : Schematic of the stress/strain relation to illustrate the plastic regime. Extracted from [141].

When the applied stress crosses a critical value (yield stress: σ_y), the stress-strain behavior deviates from linearity (elastic regime) and enter into the plastic regime (Figure 65). In this regime, the strain introduced is irreversible. It means that when the stress is relaxed, the material does not go back to its original dimension. In Figure 66, the variation of the yield stress is plotted as a function of the germanium concentration. We must first notify that the values extracted from literature can be really different. Indeed, for a germanium concentration of 22%, the yield stress is nearly 10 nm and 30 nm according to People/BEAN [107] and Hartmann [108] respectively. To conclude, as the thickness of the SiGe layer in the 14FDSOI technology (~7.5 nm) is smaller compared to yield stress in literature, we do not consider the plasticity in our simulations.

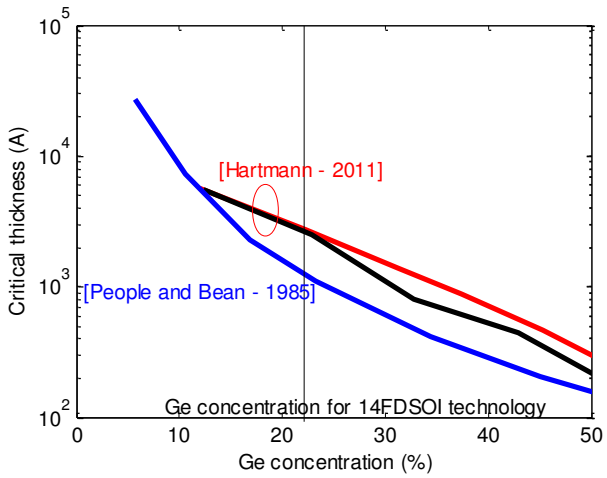

Figure 66 : Value of the yield stress for $Si_{1-x}Ge_x$ as a function of the Germanium concentration. [Hartmann – 2011]: [107], [People and Bean – 1985]: [108].

III.2.5 Process-induced stress

A large number of elementary steps such as epitaxy, deposit, etching, oxidation or thermal anneal can induce or modify the mechanical stress field in the structure. Thus, the prediction of the performance of devices requires an accurate simulation of the stress profile in the channel accounting for each elementary step. The aim of this part is to understand physical mechanisms responsible of the stress in the structure and how they are simulated in TCAD.

- **Stress caused by thermal mismatch**

High temperature deposition or thermal anneal during the process can lead to modification of the stress in the device. The thermal deformation coefficient of a material can be used to quantify its deformation ϵ_{th} induced by a temperature variation of ΔT:

$$\epsilon_{th} = \alpha\, \Delta T \tag{3.17}$$

If we consider temperature-dependent thermal deformation coefficient, the strain in a film deposited on a substrate can be expressed as:

$$\epsilon_{th} = \int_{T_O}^{T} \left[\alpha_f(T) - \alpha_S(T)\right] dT \tag{3.18}$$

$\alpha_f(T)$ and $\alpha_S(T)$ are the thermal deformation coefficients of the film and the substrate respectively. T and T_O are the final and initial temperature.

For silicon, a linear variation with temperature is taken into accounts and adjusted on measurements: $\alpha = 3.1 \times 10^{-6} + 1.24 \times 10^{-9}.\Delta T$ [°C^{-1}] [122]. Concerning silicon dioxide and silicon nitride their values are reported in Table 13.

Material	$\alpha°$ [C^{-1}]	ref
silicon	$3.1 \times 10^{-6} + 1.24 \times 10^{-9}$ [2.6 - 4.5]	[141]
SiO_2	0.5×10^{-6}	[100]
Silicon Nitride	2.8×10^{-6}	[100]

Table 13 : Values of thermal coefficients used in our simulations

- **Stress induces by lattice mismatch**

In SiGe channel based pMOSFET, the SiGe layer can be directly epitaxied on a Si buffer layer or can be formed by a condensation process. As the Germanium has a 4.2% larger lattice constant than silicon, to match the lattice constant of the unstrained Si substrate, the SiGe layer is compressively strained (Figure 67). The difference in lattice parameters of Si and SiGe causes a biaxial compressive strain and the in-plane components can be expressed as:

$$\epsilon_{xx} = \epsilon_{yy} = \frac{a_{Si} - a_{SiGe}}{a_{SiGe}} \simeq -0.04 * x_{Ge} \tag{3.19}$$

The lattice constant in the growth direction is

$$\epsilon_{zz} = -2\epsilon_{xx}C_{12}/C_{11} = -0.77\epsilon_{xx} \simeq 0.03 * x_{Ge} \tag{3.20}$$

And the strain tensor can be expressed as:

$$\begin{cases} \epsilon_{xx} = -0.04 * x_{Ge} \\ \epsilon_{yy} = -0.04 * x_{Ge} \\ \epsilon_{zz} = 0.03 * x_{Ge} \\ \epsilon_{xy} = 0 \\ \epsilon_{xz} = 0 \\ \epsilon_{yz} = 0 \end{cases} \tag{3.21}$$

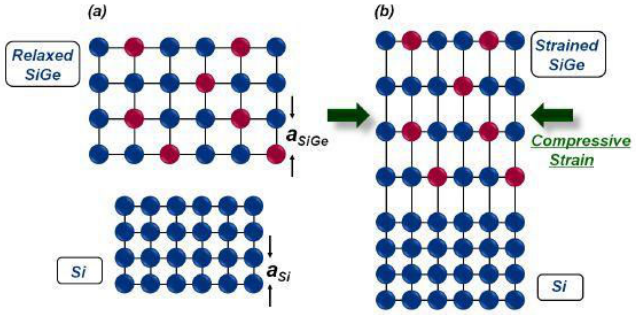

Figure 67 : (a) Schematic diagram of relaxed SiGe and silicon films. (b) Schematic diagram showing the lattice distortion when the SiGe film is growth on top of the silicon film: the SiGe film is compressively strained. Figure extracted from [140].

The SiGe channel for pMOS 14FDSOI technology (TEM cross-section shown in Figure 68) is formed using the germanium condensation process. As, in TCAD, this step cannot be directly simulated, a SiGe layer is deposited with a constant concentration of Germanium. We also assume that the level of strain in the channel corresponds to the theoretical one (described by equation 3.21) so that no relaxation has occurred during the condensation process. To validate these two hypotheses, an Electron Dispersive X-Ray spectroscopy and a NBD analyses have been performed. The Electron Dispersive X-Ray spectroscopy analysis along (Figure 69) the profile shown in Figure 68 highlights a nearly uniform distribution of germanium in the channel (25% in that case). The NBD study (Figure 70) along the same profile shows a relative deformation in the SiGe channel of roughly zero in the <110> direction. This indicates that the lattice parameter of the SiGe layer corresponds to the lattice parameter of the reference (non-stressed silicon) so the SiGe layer is fully stressed (nearly 1.5 GPa in this case). These two studies allow to validate the two simulation assumptions.

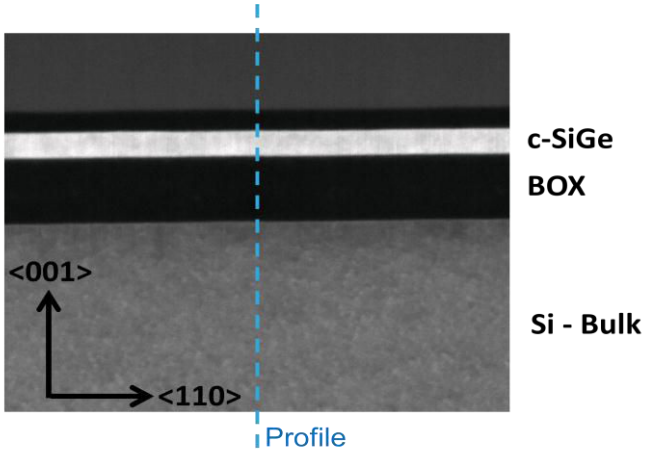

Figure 68 : TEM cross-section of the device after the formation of the SiGe channel by condensation. TEM study performed by the te*am "physical characterization"*.

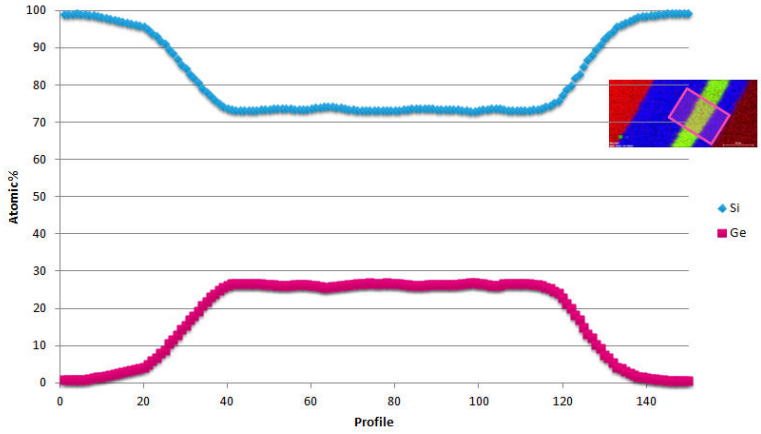

Figure 69 : Electron Dispersive X-Ray (EDX) Spectroscopy analysis along the profile shown in Figure 68. EDX analysis performed by the te*am "physical characterization"*.

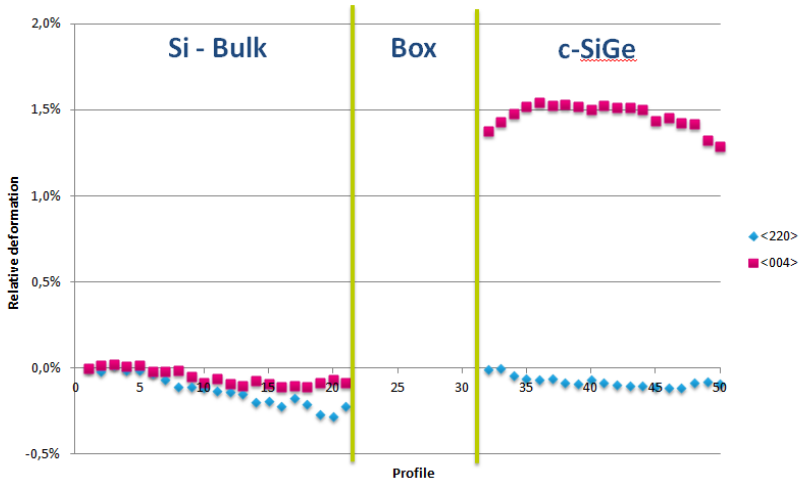

Figure 70 : Relative strain versus profile (shown in Figure 68) measured by NBD. NBD study performed by the *team "physical characterization"*.

- **Material densification: STI example**

High-density plasma (HDP) [107] [114] and high-aspect-ration process (HARP) [114] chemical vapor deposition processes are the two main techniques to deposit STI oxides. For both techniques, the deposited oxide is porous and a thermal heating is required to increase the density of the material. The volume shrinkage of the STI during the heating directly generates stress in the devices. Moreover, for 14FDSOI technology devices, STI are deposited at 540°C using HARP CVD technique and a second source of stress coming from the difference in CTE between the STI oxide and the substrate must be considered. Measurements have been performed by depositing the oxide directly on the substrate on a full wafer and a compressive stress of 220 MPa is measured in the STI layer. To take account for the oxide densification during the thermal anneal, in TCAD, we have simulated the deposition of the oxide on a full wafer (Figure 71). The stress induced by the difference in CTE between the STI oxide and the substrate is approximately -150MPa and to match measurements, during the thermal anneal (30min at 1050°C), a volume densification of 0.3% is added

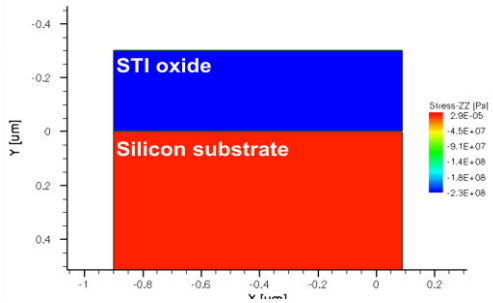

Figure 71 : TCAD simulation of the deposition of the STI (540°C) on a full wafer.

III.3 Strain measurement techniques

Accurate determination of strain in electronic devices has been the subject of intense work during the last decades. Techniques such as Raman [110] [111] [112] spectroscopy and X-Ray diffraction [113] can be used for strain measurements but actual devices require a nanoscale resolution which can only be obtained using transmission electron microscopy (TEM). TEM-based techniques can be divided into two categories: diffraction-based techniques such as convergent-beam electron diffraction (CBED) or nanobeam electron diffraction (NBD), and image-based techniques such as high-resolution electron microscopy (HREM) or dark-field electron holography (HoloDark). The characteristics of these techniques (e.g. the spatial resolution, the sensitivity …) are summarized in Table 14. It is important to notice that the use of TEM-based techniques to measure the strain in FDSOI devices require a thinning of the sample which is generally realized thanks to the focused ion beam (FIB) tool [121]. One major difficulty with the thinning of the sample is to avoid the relaxation of the stress during the preparation.

Strain measurement techniques	Spatial resolution [nm]	Sensitivity	Optimal thickness of the sample [nm]	Characteristics	References
High-Resolution Electron Microscopy (HREM)	~ 2-3	1×10^{-3}	~ 50	- Mode: image - Field of view : image 150 * 150 nm² - A close reference (unstrained Si) is required.	[115] [119]
Convergent-Beam Electron Diffraction (CBED)	2 , 5, 1	2×10^{-4}	> 300 -400	- Mode: probe	[115] [120] [116]
NanoBeam electron Diffraction (NBD)	5 , 2.7	6.0 × 10-4 1.0 × 10-3	~ 200	- Mode: probe	[116] [119]
Dark-field electron holography (HoloDark)	~ 4	2.5×10^{-4} 2×10^{-4}	~ 150	- Mode: image - Field of view : image 500 * 1500 nm² - A close reference (unstrained Si) is required.	[115] [119]

Table 14 : Comparison of TEM-based strain measurement techniques.

During my thesis, strain measurements have been performed thanks to the NBD and the dark-field electron holography techniques by the "physical characterization" team.

III.4 TCAD Stress-dependent mobility models.

Modeling of the mobility change with strain for drift diffusion device simulations usually falls into two different categories of models. In the first one, analytical physics-based models have often been developed for special stress configurations such as uniaxial longitudinal stress [117], biaxial stress [118], or are restricted to silicon channel. The second category regroups mobility models such as the linear and non-linear piezoresistive approach. The linear piezoresistive theory can be written as [123]:

$$\Delta\mu_{kl} = \sum_{ij} \Pi_{klij}\sigma_{ij} \tag{3.22}$$

Where $\Delta\mu_{kl}$ is the mobility variation, Π_{klij} the piezoresistive tensor, σ_{ij} the stress tensor and i,j,k,l the coordinates. In crystals with cubic symmetry such as silicon, the number of independent coefficients of the linear piezoresistance tensor reduces to three resulting in the following tensor for a (100)-oriented channel (001) wafer (case where the crystallographic coordinate systems CCS coincide with the device coordinate system CDS):

$$\Pi_{ij} = \begin{pmatrix} \Pi_{11} & \Pi_{12} & \Pi_{12} & 0 & 0 & 0 \\ \Pi_{12} & \Pi_{11} & \Pi_{12} & 0 & 0 & 0 \\ \Pi_{12} & \Pi_{12} & \Pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \Pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \Pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \Pi_{66} \end{pmatrix} \tag{3.23}$$

For a (001)-oriented wafer device with a (110)-oriented channel, a rotation of 45° is applied around the (001) axis leading to the following tensor:

$$\Pi_{ij} = \begin{pmatrix} \Pi_L & \Pi_T & \Pi_{12} & 0 & 0 & 0 \\ \Pi_T & \Pi_L & \Pi_{12} & 0 & 0 & 0 \\ \Pi_{12} & \Pi_{12} & \Pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \Pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \Pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \Pi_{11} - \Pi_{12} \end{pmatrix} \quad (3.24)$$

Where Π_L and Π_T are the longitudinal and transversal piezoresistance coefficients and are given by:

$$\Pi_L = \frac{\Pi_{11}+\Pi_{12}+\Pi_{44}}{2} \text{ and } \Pi_T = \frac{\Pi_{11}+\Pi_{12}-\Pi_{44}}{2} \quad (3.25)$$

The bulk piezoresistive approach (equations 3.22) exploits silicon crystal symmetries to reduce the piezoresistive tensor into four independent coefficients: Π_{11}, Π_{12} and Π_{44} and Π_{66} (equation 3.23 for a (100)-oriented channel (001) wafer). As demonstrated in [127], this approach, despite the fact that it is widely used in the electronic device community, is only valid at low stress values and in bulk silicon crystal. Indeed, in silicon inversion layers, due to quantum confinement, the piezoresistive tensor symmetries are reduced, and the number of independent coefficients increases up to six. The piezoresistive tensor can now be written as:

$$\Pi_{ij} = \begin{pmatrix} \Pi_{11} & \Pi_{12} & \Pi_{13} & 0 & 0 & 0 \\ \Pi_{12} & \Pi_{11} & \Pi_{13} & 0 & 0 & 0 \\ \Pi_{13} & \Pi_{13} & \Pi_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & \Pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \Pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \Pi_{66} \end{pmatrix} \quad (3.26)$$

Moreover, as the inversion potential well is modulated by the normal electric field, piezoresistance coefficients therefore depend on the effective electric field as mentioned in [127].

This latter behavior is clearly visible in Figure 72, where electron piezoresistance coefficients are plotted versus effective field. At low effective field, Π_{12} and Π_{13} take approximately the same value, as expected from the bulk theory. Moreover, the calculated Π_{11}, Π_{12} and Π_{13} are in good agreement with the experimental results obtained in bulk silicon [123]. However, at higher effective field (i.e. E_{eff} > 0.1 MV/cm), the piezoresistance coefficients differ from their bulk values. In particular, Π_{12} and Π_{13} are no longer equal, and can even change sign. This behavior can explain the large difference between published coefficients for MOSFETs (Table 15), in particular for the coefficient Π_{12}. The holes piezoresitance coefficients variations with the effective field are shown in Figure 73. A good correlation is observed between simulation, data from literature and our simulations.

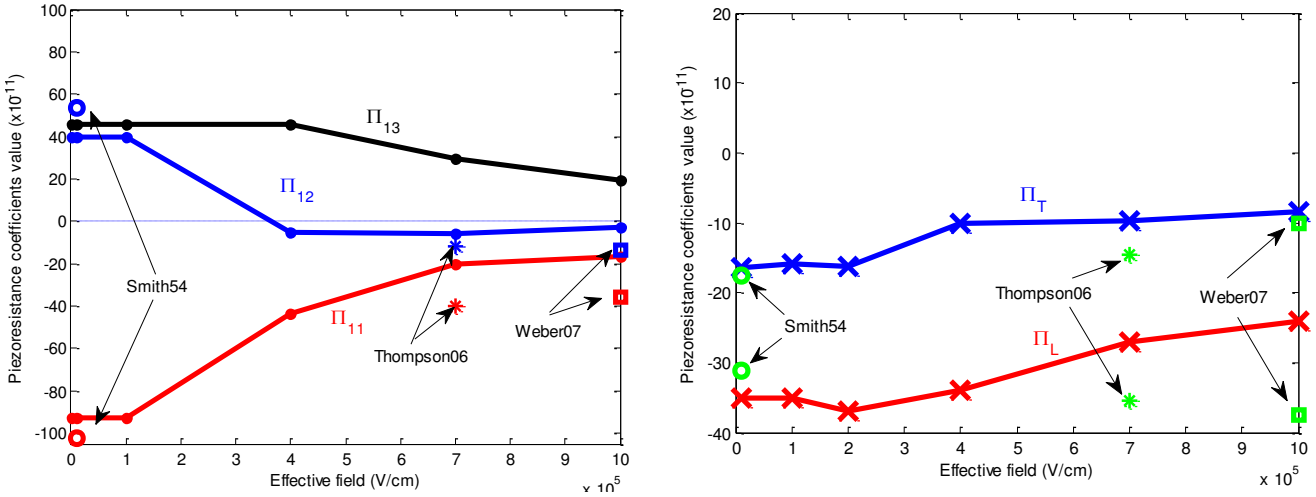

Figure 72 : nMOSFET piezo coefficients calculated using a KG solver and compared to literature. ***a*) $\Pi_{11}, \Pi_{12}, and\ \Pi_{13}$** are obtained by applying a longitudinal, transversal and vertical stress on a <100>-oriented channel MOSFET. ***a*) Π_L *and* Π_T** are obtained by applying a longitudinal and transversal stress on <110>-oriented channel MOSFET. Smith54: [123], Thompson06: [132], Weber07: [106].

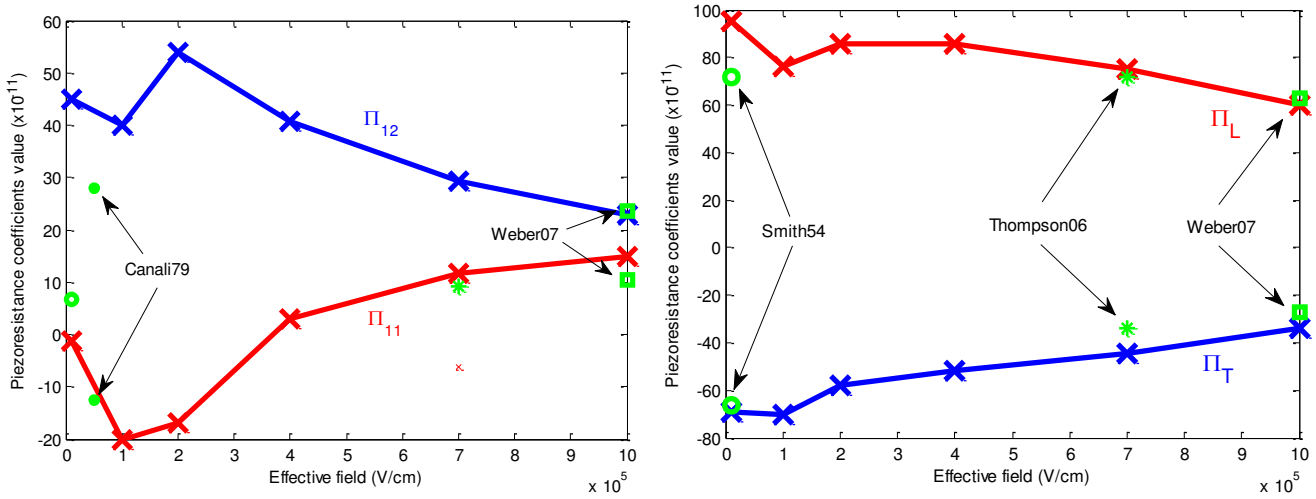

Figure 73 : Same as Figure 72 but for pMOSFETs. PI1. Canali79: [125].

Piezoresistive coefficients (× 10^{-11} Pa-1)	Bulk silicon		Inversion layer			
	Electrons	Holes	Electrons		Holes	
Π_{11}	-102.2 [123]	6.6 [123][126]	-42.6 [132] -84 [125] -38.6 [124]	E_{eff}=0.7MV/cm E_{eff}=0.05MV/cm E_{eff}=0.7MV/cm	9.1 [124] -12.5 [125] -1.0	E_{eff}=0.05MV/cm
Π_{12}	53.4 [123]	-1.1 [123][126]	-20.7 34 [125] -18.7 [124]	E_{eff}=0.7MV/cm E_{eff}=0.05MV/cm E_{eff}=0.7MV/cm	-6.2 [124] 28.0 [125] 23.8 [126]	E_{eff}=0.05MV/cm
Π_{44}	-13.6 [123]	138.1 [123][126]	-21 -17 [125]	E_{eff}=0.7MV/cm	105.5 [124] 105.0 [125] 91.7 127.8 [126]	E_{eff}=0.05MV/cm

Piezoresistive coefficients ($\times 10^{-11}$ Pa-1)	Bulk silicon		Inversion layer			
	Electrons	Holes	Electrons		Holes	
Π_L	-31.2 [123] -26.0 [131]	71.8 [123] 53.5 [131]	-35.5 [132][124] -48.5 [133] -31.5 [134] -30.0 [135]	E_{eff}=0.7MV/cm	71.7 [132][124] 60 [133] 71.8 [134] 59.0 [134]	
Π_T	-17.6 [123] -12 [131]	-66.3 [123] -58.5 [131]	-14.5 [132][124] -21.2 [133]	E_{eff}=0.7MV/cm	-33.8 [132][124] -38.3 [133]	

Table 15 : Piezoresistive coefficients values for bulk silicon and in the case of an inversion layer.

- **Piezoresistance coefficients measurement**

The piezoresistance coefficients have been extracted using the 4 points wafer bending technique on 28FDSOI technology devices. Figure 74 shows the 4 points the bender used for piezoresistive coefficients measurements.

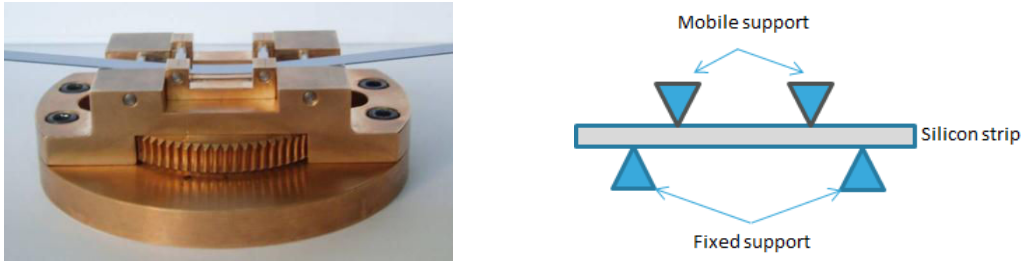

Figure 74 : Picture (a) and schematic diagram (b) of the 4 points the bender used for piezoresistive coefficients measurements

The curvature radius of the strip is measured thanks to a CCD camera and linked to the uniaxial stress thanks to the expression

$$\sigma = -\frac{eE}{2R} \tag{3.27}$$

with E the Young modulus ($E_{<110>} = 168\ GPa$, $E_{<100>} = 128\ GPa$), e the strip thickness and R the curvature radius. A uniaxial stress ranging from -150 MPa to 150 MPa is applied to the strip thanks to the bender and the mobility variation is measured at VG=1.5V Figure 75a, and Figure 75b show the measured mobility variation as a function of the applied stress for n-type (a) <100>-oriented and b) <110>-oriented channel and p-type MOSFET (Figure 76). The extracted coefficients are listed in Table 16 and are similar to coefficients found in literature (Table 15).

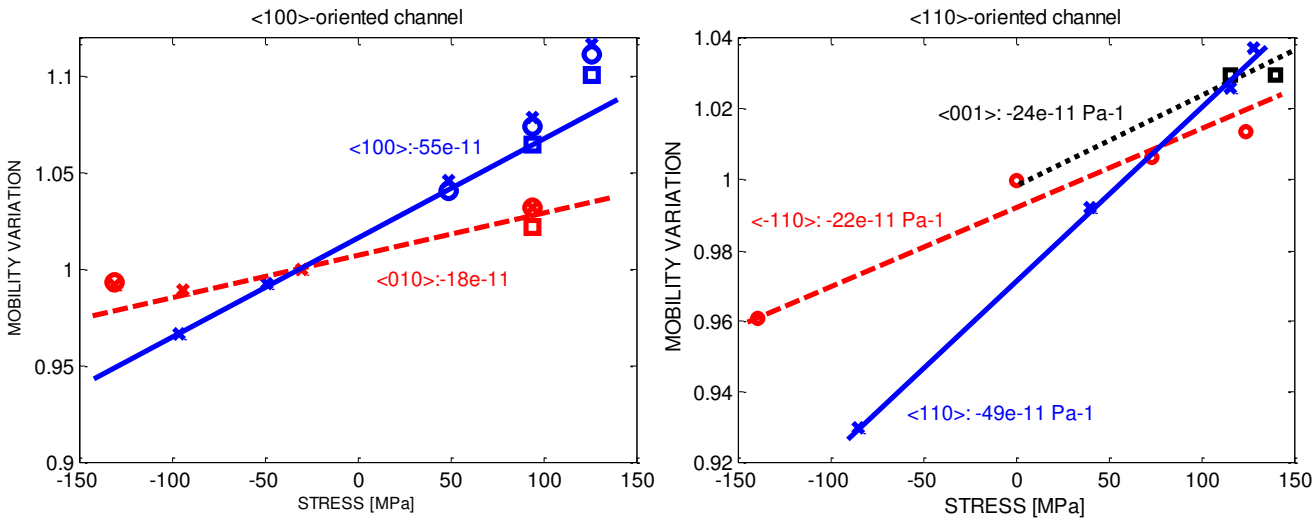

Figure 75 : Mobility variation with stress for a) <100>-oriented and b) <110>-oriented channel nFDSOI devices. The extracted piezoresistance coefficients are listed in Table 16. Measurements are performed on 28FDSOI technology (device described in part II.3).

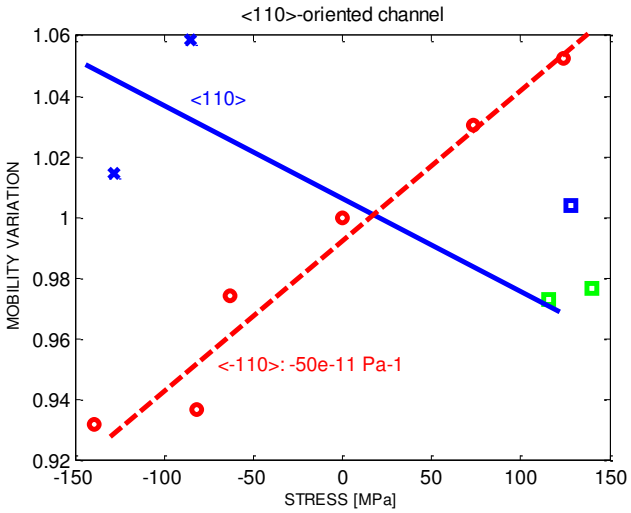

Figure 76 : Mobility variation with stress for <110>-oriented channel pFDSOI devices. The extracted piezoresistance coefficients are listed in Table 16.

NMOS		PMOS	
Channel <110>		**Channel <110>**	
Stress Direction	**Piezo Coeff [Pa^{-1}]**	**Stress Direction**	**Piezo Coeff [Pa^{-1}]**
<110>	-49e-11	<110>	
<-110>	-22e-11	<-110>	-50e-11
<001>	-24e-11	<001>	
Channel <100>		**Channel <100>**	
<100>	-55e-11	<100>	Low value
<010>	-18e-11	<010>	Low value

Table 16 : Piezoresistance coefficients extracted from wafer bending measurements

- **Validity of the piezoresistive theory:**

The linear piezoresistive theory is valid only in a limited range of stress as already highlighted in [127]. Indeed, for high stress values (> 300 MPa), the mobility variation can exhibit a large nonlinear dependence with stress. In Figure 77, a linear and an exponential piezo model is compared to KG calculations applying a longitudinal uniaxial stress on a <110>-oriented channel device. In that case, we can notice that these two models are not able to reproduce the mobility variation for stress up to 300 MPa.

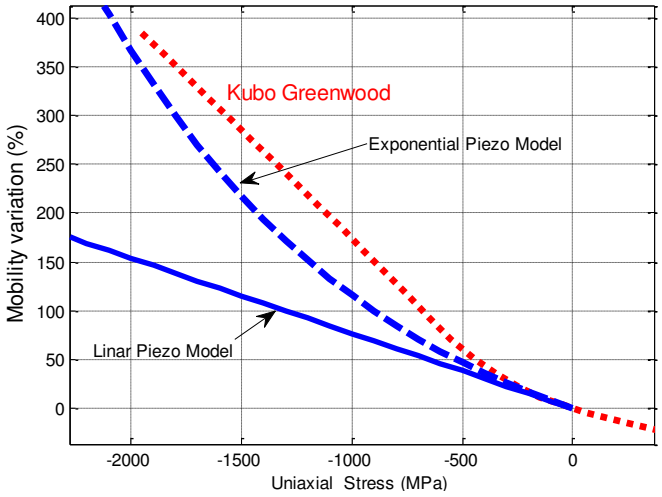

Figure 77 : Hole mobility variation (extracted at E_{eff}=1 MV/cm) in <110>-oriented silicon channel pMOSFETs as a function of the longitudinal uniaxial stress (stress applied in the <110> direction).
Linear model: $\boldsymbol{\Delta\mu/\mu = -\Pi_L \times \sigma}$. Exponential model: $\boldsymbol{\Delta\mu/\mu = exp(-\Pi_L \times \sigma)}$ with $\boldsymbol{\Pi_L = 77 \times 10^{-11}\ Pa^{-1}}$

The linear piezoresistive theory has been widely used to evaluate the mobility variation with stress. However, in actual UTBB-FDSOI devices, the stress can reach values between -1 and -2 GPa and the linear piezoresistive theory is no longer valid. In the next section we present a TCAD mobility model which extends the piezoresistive approach.

- **Stress-dependent mobility model in TCAD: MCmob:**

MCmob is a stress-dependent mobility model for the commercial device simulator Sentaurus Device by Synopsys which extends the piezoresistive approach validity in the high stress range [100] [127]. The variation of mobility with stress is given by the two following models:

$$\frac{\Delta\mu}{\mu_c} = \sum_{i=1}^{6} a_{j,SiGe,K,L,i,c} \cdot \sigma_j^i \tag{3.28}$$

$$\frac{\Delta\mu}{\mu_c} = \frac{a_{j,SiGe,K,L,1,c} e^{a_{j,SiGe,K,L,2,c}*\sigma_j} + a_{j,SiGe,K,L,3,c} e^{a_{j,SiGe,K,L,4,c}*\sigma_j}}{a_{j,SiGe,K,L,5,c} e^{a_{j,SiGe,K,L,2,c}*\sigma_j} + a_{j,SiGe,K,L,6,c} e^{a_{j,SiGe,K,L,4,c}*\sigma_j}} \tag{3.29}$$

where j refers to the direction of the applied stress (c: channel, w: width or n: normal), SiGe is the germanium mole fraction, K and L are the wafer and channel orientations and i is the index of the coefficients c is the carrier type (h for holes and e for electrons)

The implemented expression (equations 3.28 or 3.29) depends on the carrier type (electrons or holes), the channel orientation (100 or 110) and the direction of the applied stress (c: channel, w: width and n: normal). Expressions for each condition are summarized in Table 17.

Holes		**Electrons**		
<100> Channel	**<110> Channel**	**<100> Channel**	**<110> Channel**	
Stress orientation (100) c / (010) w / (001) n	Stress orientation (110) c / (-110) w / (001) n	Stress orientation (010) w	Stress orientation (110) c / (-110) w	**Eq. 3.28**
		Stress orientation (100) c / (001) n	Stress orientation (001) n	**Eq. 3.29**

Table 17 : MCmob model description for uniaxial stress.

In order to improve interpolation in some specific stress conditions, e.g. biaxial stress, a cross terms correction is introduced:

$$\frac{\Delta\mu}{\mu_c} = \left(\frac{\Delta\mu}{\mu_c}\right)_{\text{Eq.3.28 or 3.29}} + C(\sigma_r) \tag{3.30}$$

The cross terms correction $C(\sigma_r)$ is the sum of nineteen coefficients multiplied by different combinations of uniaxial stress components σ_r. Such coefficients and their coupling stress components are listed in Table 18 in the case of a (K)-oriented wafer device with a <L>-oriented channel.

Coefficients	Coupling stress comp.	Coefficients	Coupling Stress comp.
as**K**c**L**1h	σc*σn	as**K**c**L**11h	σc*σw*σw*σw
as**K**c**L**2h	σc*σw	as**K**c**L**12h	σc*σn*σn*σn
as**K**c**L**3h	σn*σw	as**K**c**L**13h	σn*σc*σc*σc
as**K**c**L**4h	σc*σw*σw	as**K**c**L**14h	σn*σw*σw*σw
as**K**c**L**5h	σc*σn*σn	as**K**c**L**15h	σw*σc*σc*σc
as**K**c**L**6h	σn*σc*σc	as**K**c**L**16h	σw*σn*σn*σn
as**K**c**L**7h	σn*σw*σw	as**K**c**L**17h	σn*σn*σw*σw
as**K**c**L**8h	σw*σc*σc	as**K**c**L**18h	σc*σc*σw*σw
as**K**c**L**9h	σw*σn*σn	as**K**c**L**19h	σc*σc*σn*σn
as**K**c**L**10h	σc*σn*σw		

Table 18 : MCmob cross terms correction coefficients

The calibration of MCmob is performed using a Sband KG solver as a reference. The effective mobility variation with stress is calculated for three uniaxial and three biaxial conditions. MCmob model parameters have been determined using a mixed global-to-local optimization strategy to ensure accurate and robust solutions. Indeed, the large number of coefficients for each orientation can leads to complex structures of error minima. As a first step, a global parameter optimization, using DIRECT algorithm [128], is performed. Afterwards, a local optimization procedure is applied to increase the accuracy of the fit. Figure 78 and Figure 79 show good agreements between mobility variations calculated with MCmob and UTOXPP at E_{eff}=1 MV/cm for holes and electrons respectively. The major limitation of MCmob model is the non-dependence of the mobility variation with the effective field.

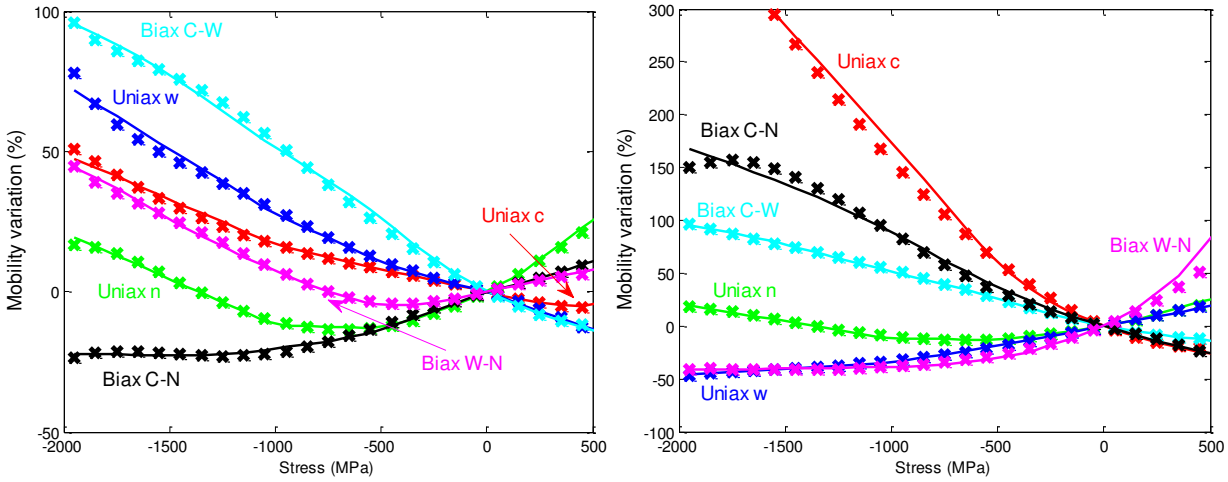

Figure 78 : Hole mobility variation (extracted at E_{eff}=1 MV/cm) in <100> (a) and <110> (b) silicon channel pMOSFETs as a function of stress for three different uniaxial stress direction and three biaxial stress types. Symbols are MCmob results and lines are UTOXPP results.

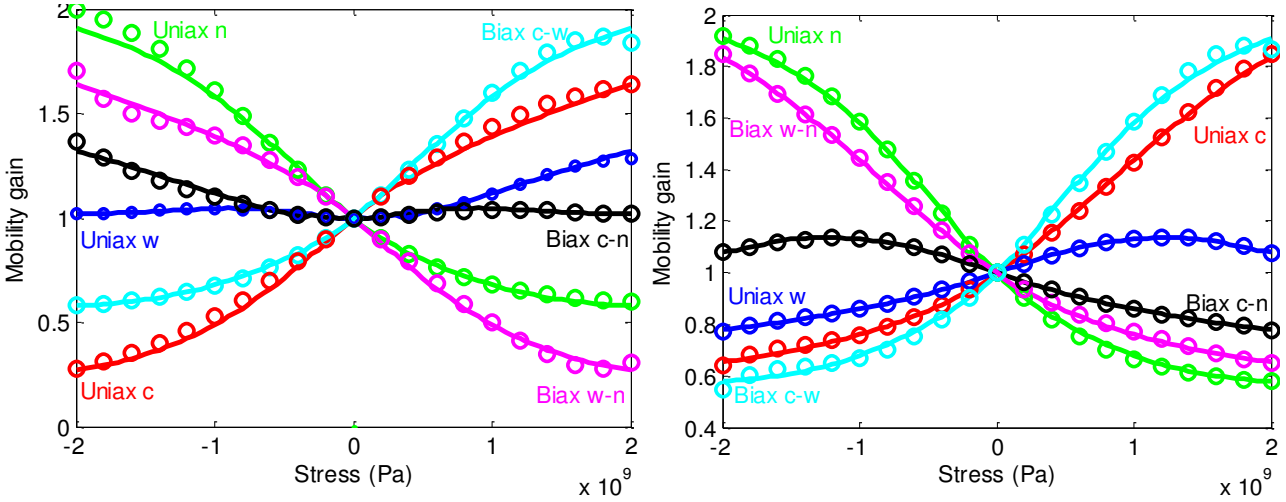

Figure 79 : Electron mobility variation (extracted at E_{eff}=1 MV/cm) in <100> (a) and <110> (b) silicon channel nMOSFETs as a function of stress for three different uniaxial stress direction and three biaxial stress types. Symbols are MCmob results and lines are UTOXPP results.

j	L	Optimized MCmob coefficients (×1e-2)					
channel		**X = 1**	**X = 2**	**X = 3**	**X = 4**	**X = 5**	**X = 6**
	100	0.7325	6.2327	16.4820	11.8435	0.8200	-16.7774
	110	0.5370	-0.0064	-0.0035	11.4204	82.3120	-84.9331
width		**X = 1**	**X = 2**	**X = 3**	**X = 4**	**X = 5**	**X = 6**
	100	6.0437	16.9149	1.5588	-25.5317	-7.8562	-20.715
	110	0.0010	0.6042	-2.0865	-10.3446	1.8354	42.7320
normal		**X = 1**	**X = 2**	**X = 3**	**X = 4**	**X = 5**	**X = 6**
	100	-0.6185	0.1487	0.0065	-5.9030	22.3297	37.9540
	110	0.093	1.7447	-0.0812	-7.3737	21.0577	36.6061
biaxial		**X = 1**	**X = 2**	**X = 3**	**X = 4**	**X = 5**	**X = 6**
	100	-34.7209	0.0907	-12.6382	0.0499	53.0111	-51.0818
	110	-86.9918	-56.4191	37.2739	-0.4888	- 1.990	-52.2115
		X = 7	**X = 8**	**X = 9**	**X = 10**	**X = 11**	**X = 12**
	100	-3.2647	0.0343	3.7745	0.0054	0.0719	103.3823
	110	47.4004	18.7120	-1.5840	0.0041	5.6679	21.3521
		X = 13	**X = 14**	**X = 15**	**X = 16**	**X = 17**	**X = 18**
	100	-32.8529	4.8661	-0.0093	-3.6551	0.4178	-0.2921
	110	-56.8440	123.1791	-0.0740	-101.4159	-8.8910	-0.7665
		X = 19					
	100	-65.7154					
	110	10.3690					

Table 19 : Calibrated MCmob parameters for holes

j	L	Optimized MCmob coefficients (×1e-2)					
channel		**X = 1**	**X = 2**	**X = 3**	**X = 4**	**X = 5**	**X = 6**
	100	0.0119	8.8275	-0.0119	10.1496	-0.0142	-0.0162
	110	-0.0023	0.0009	0.0009	-0.0154	0.0949	0.3489
width		**X = 1**	**X = 2**	**X = 3**	**X = 4**	**X = 5**	**X = 6**
	100	0.0021	-0.0061	-0.0221	0.0441	0.0965	-0.0042
	110	0.0000	0.0037	-0.0049	-0.0381	0.0006	0.1702
normal		**X = 1**	**X = 2**	**X = 3**	**X = 4**	**X = 5**	**X = 6**
	100	-0.0059	0.8026	0.0059	-0.8654	0.0140	0.0052
	110	0.0002	0.5980	-0.0002	-1.1025	-0.0004	-0.0002
biaxial		**X = 1**	**X = 2**	**X = 3**	**X = 4**	**X = 5**	**X = 6**
	100	-0.0706	0.0965	-0.3270	-0.6064	0.9640	-0.9834
	110	-0.2498	0.0457	-0.0240	-0.0297	0.0275	-0.0384
		X = 7	**X = 8**	**X = 9**	**X = 10**	**X = 11**	**X = 12**
	100	1.8577	0.5813	-1.8763	4.0001	2.0618	0.5179
	110	-0.0227	0.0174	0.0123	5.1177	-0.0533	0.0243
		X = 13	**X = 14**	**X = 15**	**X = 16**	**X = 17**	**X = 18**
	100	-1.5491	-2.7978	-1.9867	0.0314	2.8193	-0.0941
	110	0.0030	0.0043	0.0044	0.0066	0.0000	0.0400
		X = 19					
	100	1.0447					
	110	0.0000					

Table 20 : Calibrated MCmob parameters for electrons.

III.5 Conclusion

In the first part of this chapter, a review of the methodologies used during my thesis to model the mechanical stress in FDSOI structure is performed. After recalling some generalities about stress/strain tensors and simulations boundary conditions, a description of the widely encountered materials rheological behaviors is performed, namely elastic, viscoelastic and plastic laws. Then, the physical mechanisms responsible of the stress in the structure and their methodology of simulation are studied. We focused on the description of the main technology boosters to induce stress in 28 and 14 FDSOI technologies such as SiGe channel, SiGe source and drain, STI … The second part of this chapter has been dedicated to the description of strain measurements methods. During this thesis, strain has been measured thanks to nanobeam electron diffraction and the dark-field electron holography techniques. These two techniques have been used as references to validate our simulations (Chapter III and IV). Then, in the last part, we presented an accurate description, study and calibration of a TCAD stress-dependent mobility models (MCmob). Finally, in this chapter, we set up the methodology for process-induced stress simulations and to calculate its influence on electrical characteristics. This enables accurate and efficient TCAD simulations of strained-Si FDSOI MOSFETs in state of the art CMOS technology. The application of these methods to optimize STMicroelectronics devices is the topic of the fourth chapter.

Chapter IV:

ST-oriented device applications

IV.1 Introduction

FDSOI technology is considered as one of the best solution to keep increasing CMOS performances while scaling device dimensions, especially for low power applications [69] [70]. However the use of stress engineering to enhance electrons and holes transport properties is mandatory to reach ITRS [1] requirements for the 14 nm node and beyond. This is more critical in the case of advanced FDSOI technology, as high-k metal gate stacks [71] [72] and scattering with back interface [34] [46] both contribute to further degrade transport, as seen previously in chapter II. Moreover, in case of SiGe-based FDSOI devices, due to the specific mechanical properties of the ultra-thin active layer and the Buried Oxide (BOX), the solutions developed to strain bulk devices have to be reinvestigated. The development of 28 and 14FDSOI technologies requires accurate TCAD modeling of the stress profile in the transistor and its impact on the electrical performances (using for instance the approach described in chapter III). Consequently, a TCAD methodology to model the process flow has been developed during this thesis, specifically for the modeling of 14FDSOI and 10FDSOI technologies and aiming at supporting technology developments. The aim of this chapter is twofold. In the first place, mechanical simulations are performed to model the stress profile in 14FDSOI transistors (methodologies described in chapter III). A particular attention has been paid to the modeling of stress relaxation during STI process steps and to the impact of SiGe source and drain. In the second place, some electrical characteristics of these devices have been investigated more closely.
In the first part of this chapter, we perform a brief description of the developed TCAD approach to model 14/10FDSOI technology. Then, in the second part, a full mechanical study of the stress configuration in 14FDSOI technology has been performed through TCAD simulations and NBD measurements. Solutions to optimize the stress configuration in sSOI and SiGe-based devices are proposed. Finally, 14FDOI MOSFETs electrical performances have been investigated in more details

IV.2. Process flow description for 14FDSOI technology

The main process steps of 14FDSOI technology are listed in Figure 80 and the whole flow has been simulated using Sprocess (SYNOPSYS) tool. 14FDSOI devices are processed on 300 mm SOI wafers with a 25 nm thick BOX. The oxide stack is made of a 1.8 nm thick layer of high-k oxide (HfSiON) deposited on top of an SiON interfacial layer (IL) with various EOT from 0.7 to 3.0 nm The final silicon channel thickness is 7.0 nm and the p-type devices feature SiGe (x_{Ge}=22%) channel and source and drain (x_{Ge}=30%). Simulations are calibrated on TEM images to accurately reproduce the device topography (as shown in Figure 47).

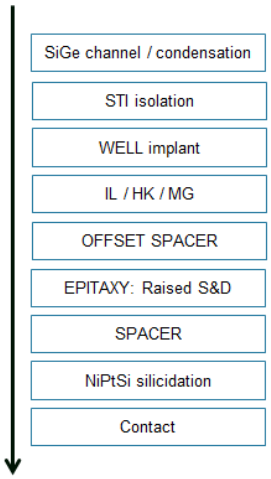

Figure 80 : Simplified description of the process flow for 14FDSOI technology.

In Figure 81, the result of TCAD process simulation of a p-type device is shown after STI isolation steps, gate stack deposition, spacer formation and SiGe S&D. It is important to notice that main steps leading to mechanical stress in p-type devices are: the SiGe channel formation, the SiGe source and drain and the high temperature material deposition (STI, Gate stack). Other sources of stress can come from contact silicidation but are not considered in our simulations.

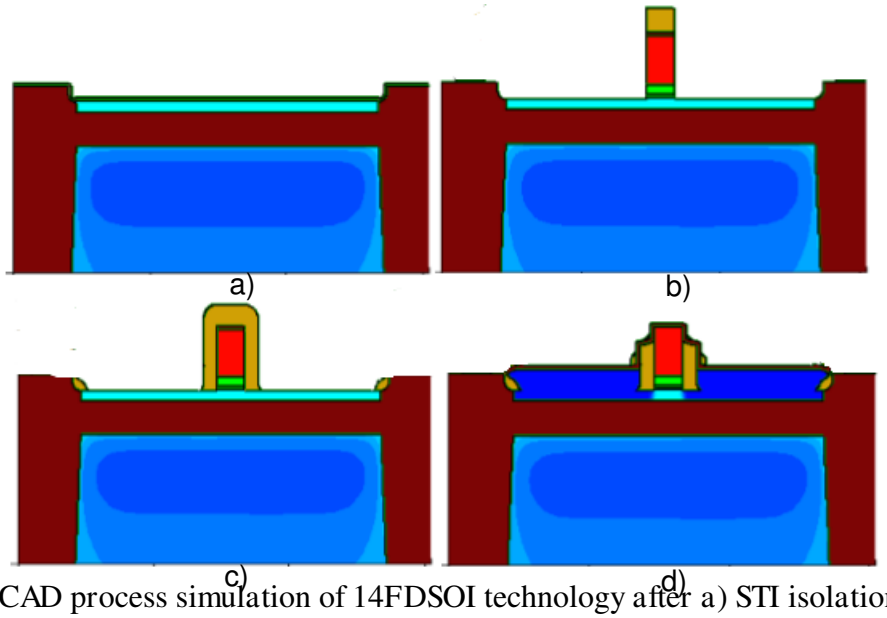

Figure 81 : TCAD process simulation of 14FDSOI technology after a) STI isolation steps, b) Gate stack deposition, c) spacer formation and d) SiGe S&D epitaxy.

Combining the methodologies described in chapter III and the accurate modeling of the process flow, mechanical stress studies can be performed, and are presented below.

IV.3 28FDSOI/14FDSOI mechanical stress study

As previously explained, global stress techniques such as strained SiGe channel or “strained Silicon On Insulator” (sSOI) [105], are current techniques to enhance carriers mobilities in MOSFETs. The resulting compressive or tensile biaxial stress is introduced into the whole wafer at the beginning of the process flow, it can undergo however several modifications during etching, deposition or thermal heating process steps. This part aims at studying the stress configuration and its evolution during the different process steps. It accounts for the main sources of stress for pMOSFETs, namely, strained SiGe channel, SiGe source and drain, STI and gate stack deposition. Simulations are compared to NBD strain measurements, and several simulations have been performed to optimize the stress configuration in the channel.

IV.3.1 STI process steps and layout effects.

The STI deposition requires several process steps (Figure 82) which are presented schematically in Figure 83. First of all, a hard mask is deposited on the surfaces that must be protected from etching. Then, the etching step allows to form the shape of the STI. Note that in this example, the two STI are dissymmetric, and are referred as shallow and deep STI. The STI is deposited at high temperature thanks to HDP [109] [114] or HARP [114] chemical vapor deposition techniques and a thermal anneal allows to make the STI denser. The simulations of the two last steps are described in part III.2. Finally, the hard mask is removed.

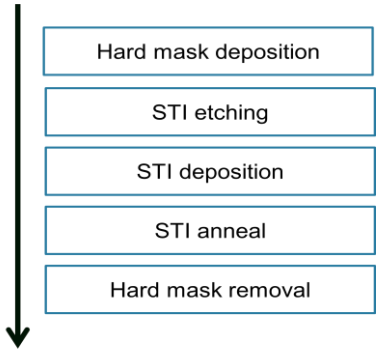

Figure 82 : STI process flow for 28/14 FDSOI technology.

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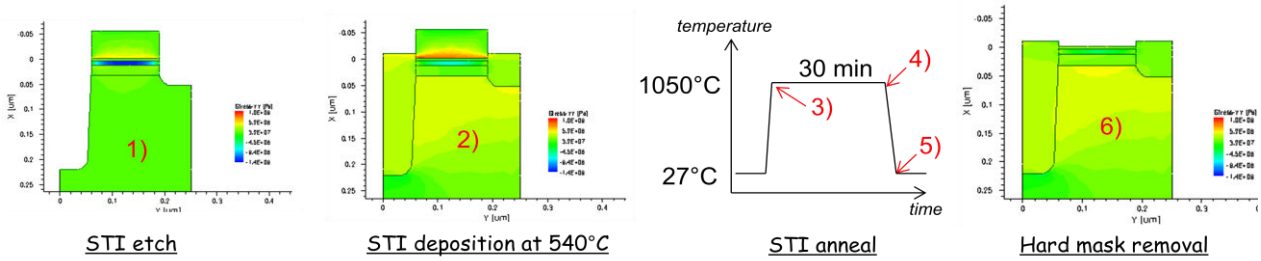

Figure 83 : Schematic description of the STI process steps. It can be noticed that a dual STI (deep and shallow STI) has been analyzed.

The evolution of the stress profile along the channel direction is shown in Figure 84. Initially the active layer is compressively stressed to 1.5 GPa, thanks to the use of an SiGe channel with xGe=22%. A first relaxation occurs due to the STI etch (step 1), reducing the stress to the value of 1.3 GPa at the center of the channel. This value further decreases close to the edge of the channel and is null at each sides (free surfaces). Represented by the step 2, the high temperature deposition of the STI adds a compressive stress in the channel due to the difference of CTE between oxide and silicon. During the STI anneal, a second important stress relaxation occurs, leading to a value of 800 MPa at the center of the channel. The high temperature anneal has indeed induced a decrease of the viscosity of the oxides and nitrides layers, facilitating the stress relaxation within the channel. However it is important to notice that this stress relaxation depends strongly on the value of the oxide viscosity (taken from [137]) which is not known with accuracy. Indeed, this property is significantly dependent on the oxide type, the temperature and composition (impurity). So a quantitative estimation of the contribution of both STI etch and STI anneal stress relaxations remains difficult in absence of calibration on measurements. Finally, the hard mask removal has not been found to impact significantly the stress profile in the channel.

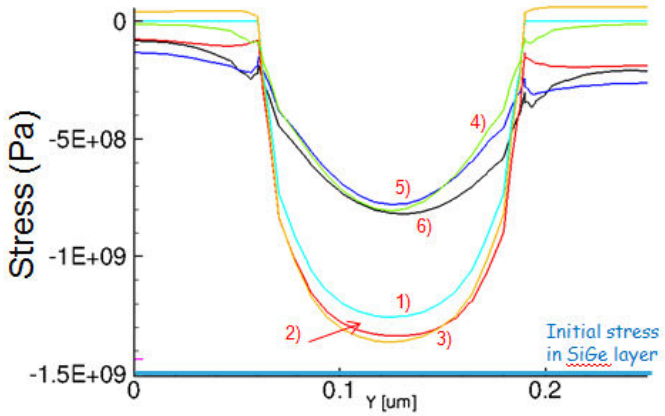

Figure 84 : Evolution of the stress profile along the channel direction during STI process steps. Numbers in in the figure corresponds to process steps described in Figure 83.

The process previously described is something called the "SiGe first" approach, as the SiGe channel is formed by condensation, before STI process steps. An alternative solution would consist in performing the condensation steps after the STI ("SiGe last"). This solution is expected to reduce the stress relaxation due to the STI etching. We have evaluated the stress profile in the channel resulting from these two methods (Figure 85). A strong reduction of the stress relaxation is indeed observed with the SiGe last method (σ_L = -1.35 GPa) compared to SiGe first (σ_L = -0.8 GPa).

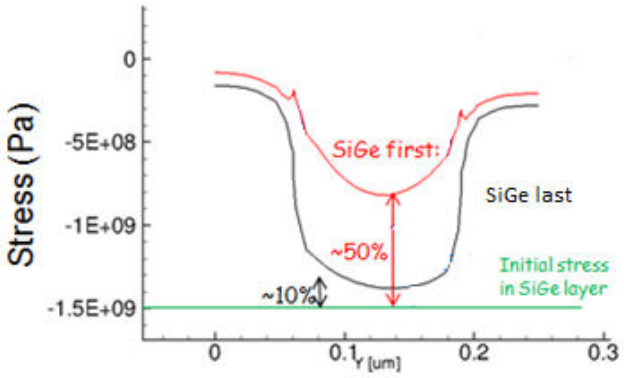

Figure 85 : Simulation of the evolution of the stress profile along the channel direction. Two cases have been considerate: SiGe first and SiGe last. L_{active}= 130 nm.

- **Stress dependence on layout dimensions: a difficult compromise between L_{active} and W_{active} effects.**

The relaxation of the SiGe channel stress during the STI process steps leads to "layout effects", which means that the mean longitudinal stress (σ_L) and transversal stress (σ_W) in the channel depend on the active layer dimensions namely L_{active} and W_{active} (as previously introduced in chapter III). Indeed, as shown in Figure 86a, a strong decrease of the mean longitudinal stress in the channel is observed for decreasing active length. Similarly, the mean transversal stress decreases with the active width. The difference between the two trends are simply due to the fact that the stress is averaged on the channel length for σ_L and over the whole width for σ_W. The resulting simulated channel mobility variations with the active length and width are shown in Figure 86b. Two different trends have been found: the reduction of L_{active} dimension induces a mobility reduction in the channel while the reduced of W_{active} leads to a mobility increase. Indeed, when the transversal compressive stress σ_W is relaxed, the channel mobility is enhanced. This highlights the fact that p-type devices are stressed in a non-optimal

way. To explain this behavior, the hole mobility variation with stress is shown for a (110)-oriented channel in Figure 87 on which three different stress configurations are represented: i) longitudinal uniaxial, ii) transversal uniaxial and iii) biaxial. We can notice that a longitudinal uniaxial stress improves the mobility much more than a biaxial stress, and that the relaxation of the transversal stress is favorable for p-type MOSFET performances.

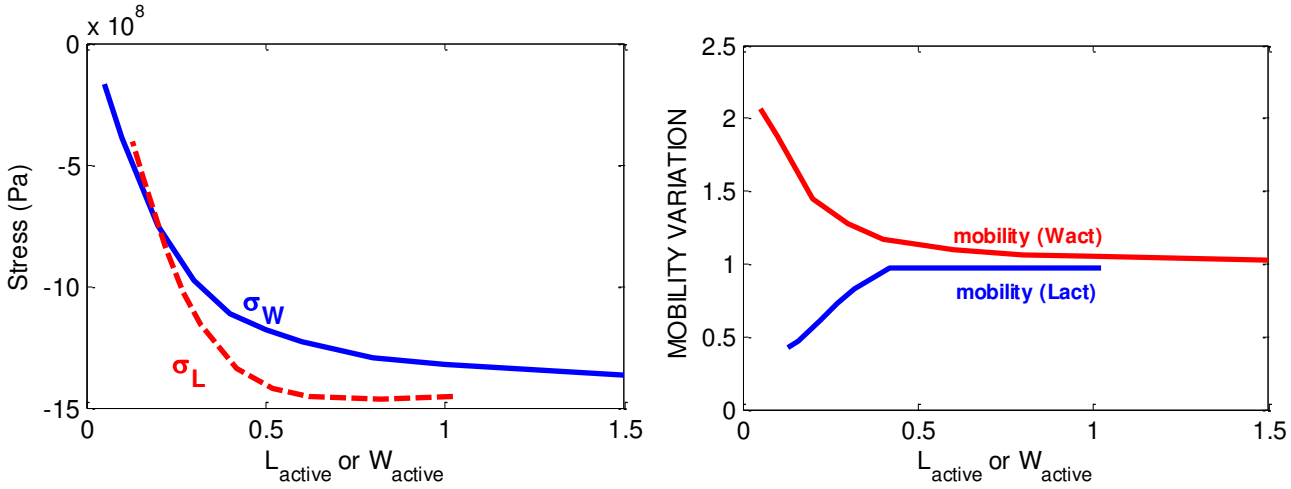

Figure 86 : Left) Simulated mean longitudinal stress (average on the channel region) with L_{active} and the mean transversal stress (average on the whole width) with W_{active}. Right) Simulated hole mobility variation with L_{active} and W_{active} using KG solver (channel wafer)

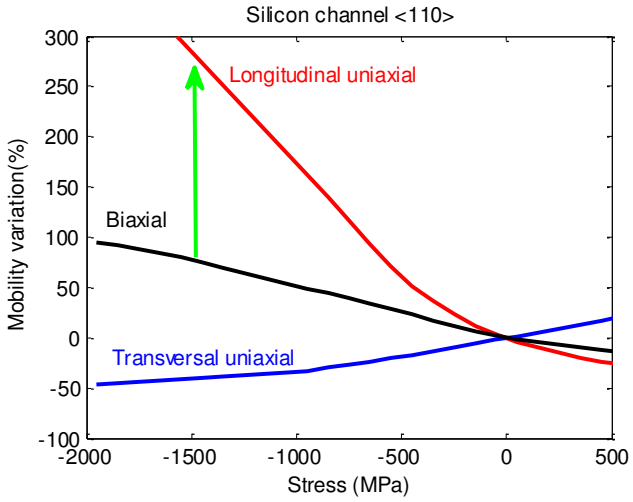

Figure 87 : Simulated (KG solver) hole mobility variation (extracted at E_{eff}= 1 MV/cm) in a) <100> and b) silicon channel pMOSFETs as a function of stress.

Actually, there is no differentiation between process steps forming the isolation trenches in L en W directions. Consequently the stress configuration in these directions are correlated and depends exclusively on the dimensions of the active layer (L_{active} for longitudinal stress and W_{active} for transversal stress). Propositions to optimize the stress configuration in the device are discussed in section IV.4.2.

These results are based on TCAD simulations and require a validation with experimental data.

IV.3.2 Stress relaxation during STI process steps: NBD Strain measurements.

The stress profile after STI process steps have been measured using the NBD technique on the TEM structure shown in Figure 88.

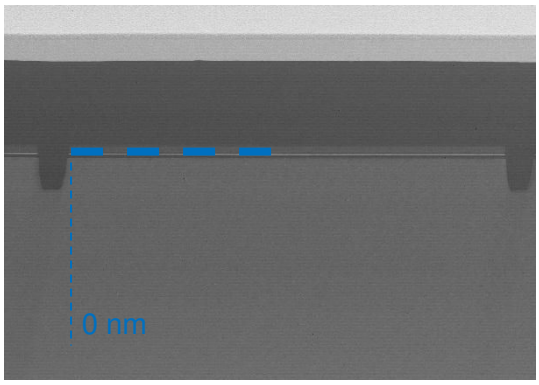

Figure 88 : TEM picture of the studied device. Measurements are performed after STI formation steps. The dotted line corresponds to the profile where NBD measurements have been performed.

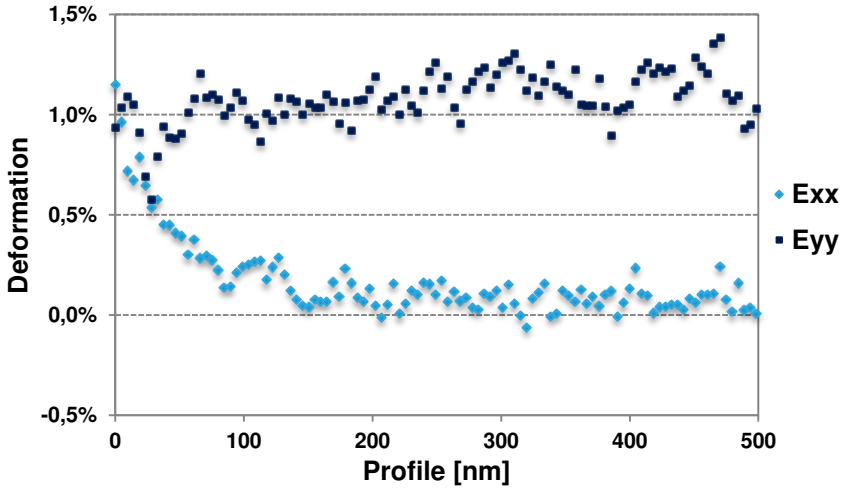

Figure 89 : *Measurements of the deformation profile (ε_{xx} and ε_{yy})* thanks to NBD measurements. Profile shown in Figure 88. x_{Ge} = 22%. Measurements have been performed before STI anneal.

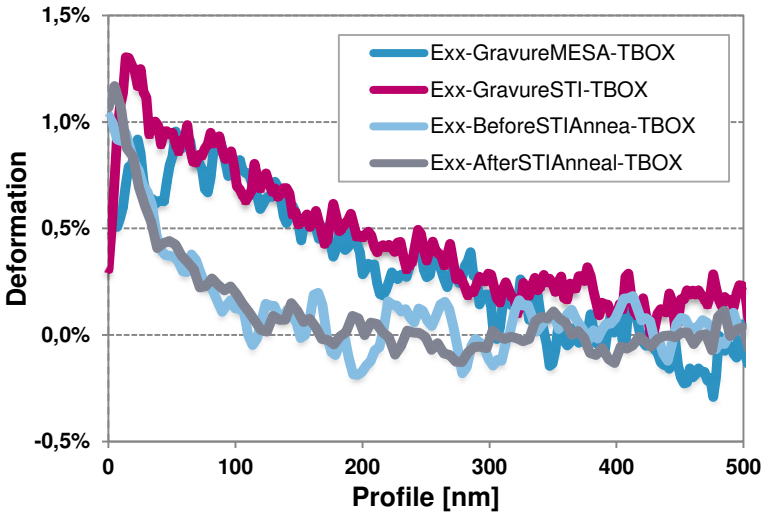

Figure 90 : *Measurements of the deformation profile ε_{xx}*

The longitudinal deformation ε_{xx} profile has been measured after four different steps (Figure 90): i) after "MESA" etching (corresponding to a deep etching), ii) after "STI" etching, iii) before STI anneal and iiii) after STI anneal. Initially, after Ge condensation process step, the lattice constant of the SiGe layer should match the one of the silicon reference, so the relative deformation should be null in

principle all along the profile. A first relaxation occurs due to the STI etch (also observed in Figure 89). The relative deformation is still null for distances up to 500 nm and increases close to the edge of the channel. This corresponds to a relaxation of the strain near the STI interface. Note that no significant difference has been found between the two etching types (MESA and STI). Then, the high temperature deposition adds a compressive strain in the channel, as previously shown in TCAD simulation (part IV.3.1). The last measurement is performed after STI anneal, and no significant influence of this step has been observed. This observation suggests that in the TCAD simulations, the relaxation of the longitudinal stress due to STI anneal has been overestimated (for this corresponding anneal temperature -1050°C-). Simulations and experiments are compared more accurately in the following part.

IV.3.3 TCAD calibration on NBD measurements

In Figure 91, NBD measurements after STI patterning have been compared to TCAD simulations. We can notice that the important relaxation of the SiGe film observed after STI patterning by NBD measurements (represented as points in the figure) can not be explained by a simple elastic theory used in the simulation (full red curve). Another phenomenon degrades the stress and is probably linked to the SiGe / BOX interface. Indeed, we suspect that the bonding between the SiGe layer and the BOX surface is weak and cannot hold the stress in the channel during STI patterning. As this phenomenon is not included in the simulation, artificial relaxations have been introduced in TCAD by adding additional anneal steps (dotted lines).

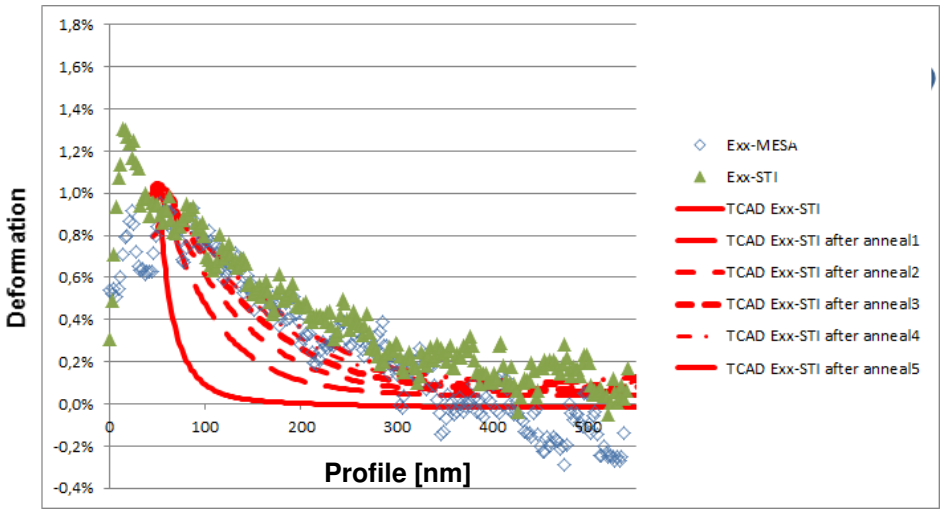

Figure 91 : *Relative longitudinal deformation* ε_{xx} measured by NBD, and comparison to TCAD simulations.

NBD measurements have then been performed after STI patterning and at the end of the process flow on structure presented in Figure 92. This structure is an interdigited PMOS with a large active length featuring a SiGe channel (x_{Ge}=22%) and source and drain (30%).

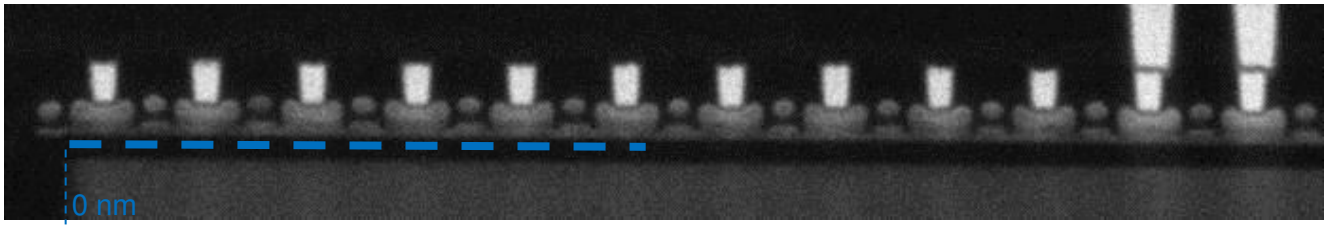

Figure 92 : TEM pictures of the simulated structure. The dotted line corresponds to the profile where NBD measurements have been performed.

Figure 93 shows that, after STI patterning, the relative deformation is null for distances up to 500 nm indicating a fully stressed SiGe channel. Moreover, close to the edge of the channel, the relative deformation increases, indicating a relaxation of the strain (close to the STI edge). This behavior has already been observed in Figure 90. Concerning NBD measurements on the fully processed device, the relative deformation exhibits an oscillating behavior which is due to the presence of embedded SiGe sources and drains and gate stacks. Quite good agreement is found between TCAD simulation and NBD measurements.

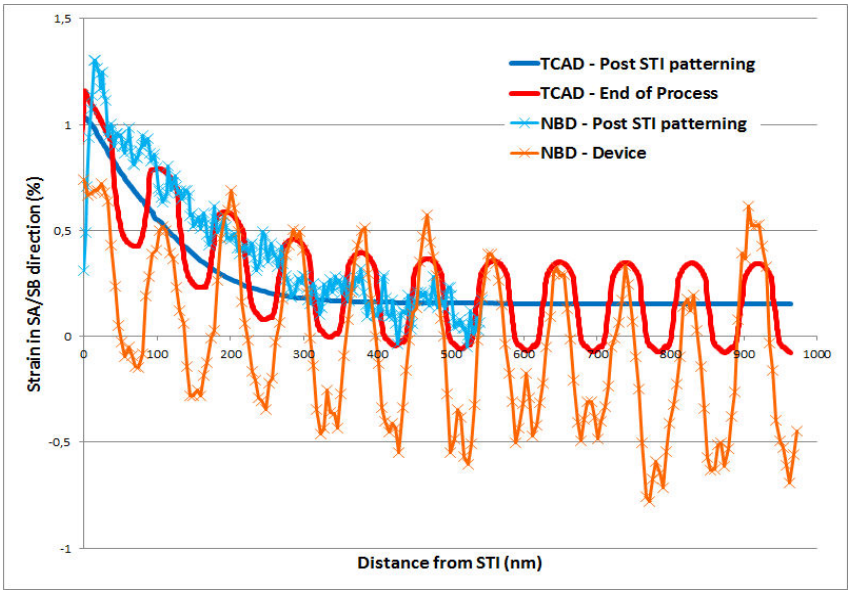

Figure 93 : *Comparison between TCAD simulations and NBD measurements of the deformation profile* ε_{xx} post STI patterning and at the end of the process. Device of Figure 92.

The dependence of the normalized (reference: long SA/SB) drain current (I_{odlin} corresponds to the drain current at $V_G=V_{TH}$ - 0.5V) as a function of SA/SB (L_{active} = SA + L_{ch} + SB; dimensions shown in Figure 94b) and compared to TCAD simulations. As previously observed in simulations, the decreases of the active length causes a relaxation of the longitudinal stress leading to a reduction of the mobility. Consequently, p-type performance (I_{odlin} in that case) are degraded for small SA/SB (~50%). Good agreement are found between TCAD and NBD measurements. Note that the variation of the width has a limited influence on I_{odlin} (SA/SB) characteristics. In Figure 95, the I_{odlin} variation is plotted as a function of the active width W_{active}. As previously observed in simulations, the decreases of the active width causes a relaxation of the transversal stress leading to an enhancement of the mobility. Consequently, p-type performance are improved for small SA/SB (~20%).

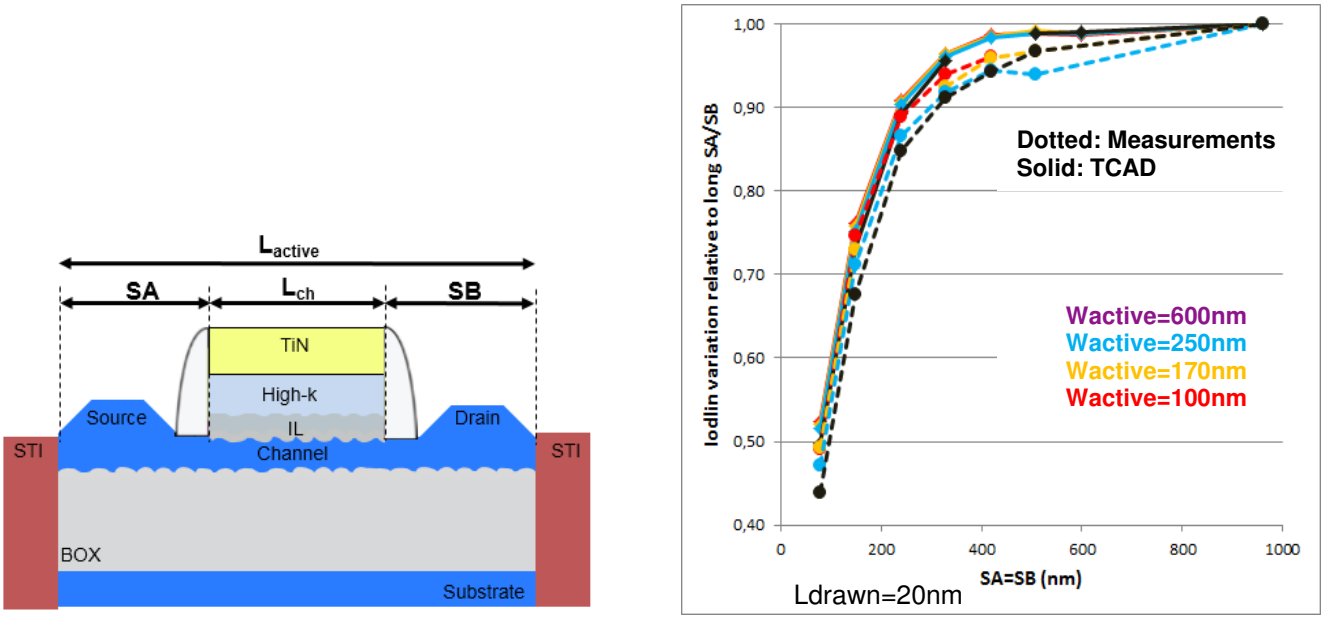

Figure 94 : Left: Definition of the notation SA and SB. Right: comparison between measured relative I_{odlin} variation (reference: long SA/SB) and TCAD simulations as a function of SA/SB

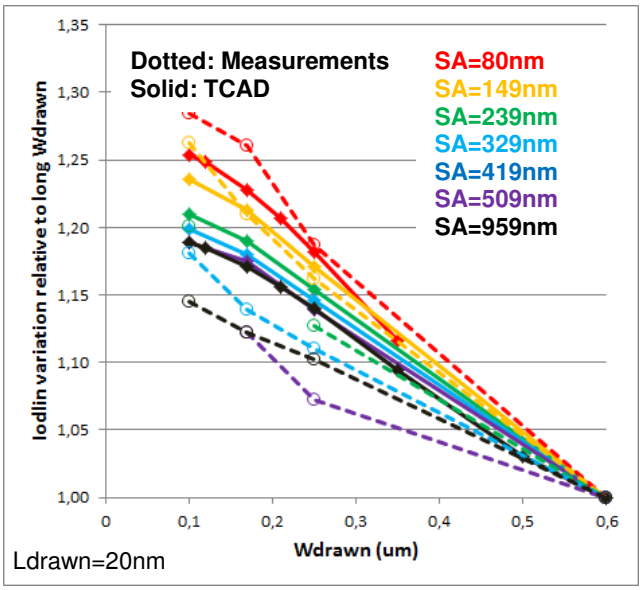

Figure 95 : Comparison between measured relative I_{odlin} variation (reference: long SA/SB) and TCAD simulations as a function of W.

- **Extraction of the relaxation length from measurements**

The aim of this study is to extract a characteristic strain relaxation length from current measurements. It consists in reducing the information contained in the current vs active length variation to a numeric characteristic distance. Two methods can be used: i) a direct extraction method where the stress relaxation length is obtained directly from the current variation as a function of the active dimension and ii) an extraction based on a more 'realistic' stress model. Using the direct extraction method, an estimation of the mechanical stress relaxation length Λ can be directly obtained from the following formula:

$$I = \frac{I_{max}}{1 + \Lambda/L_{act}} \rightarrow \left(\frac{I}{I_{max}}\right)^{-1} - 1 = \Lambda/L_{act} \qquad \text{(IV.1)}$$

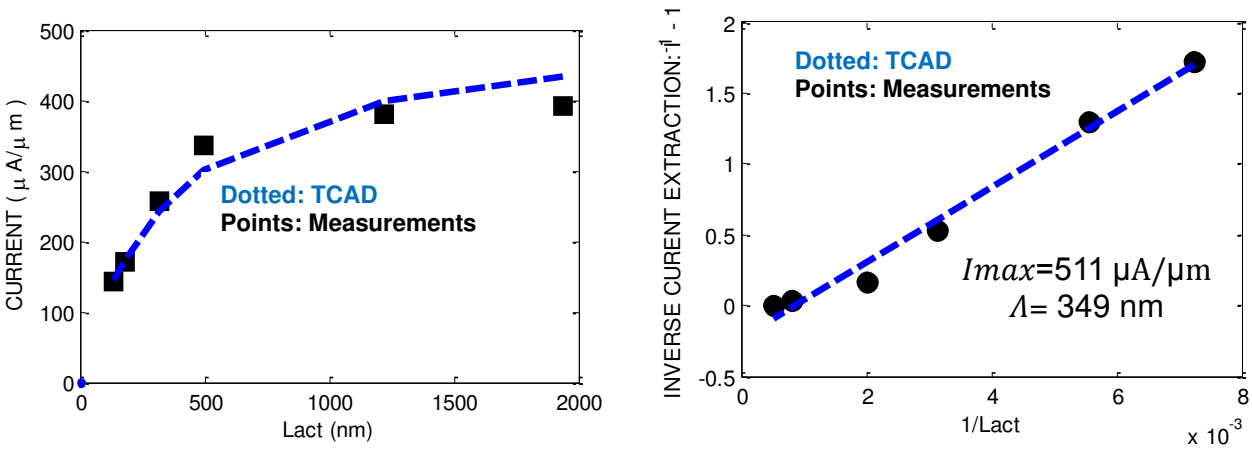

Figure 96 : a) variation of the current as a function of L_{active}. b) variation of the inverse current with $1/L_{active}$

In Figure 96a, the current variation is plotted as a function of L_{active}. Using Figure 96b, a relaxation length of Λ = 349 nm has been extracted. It represents approximately the distance in which the current decay by a factor 2. This 'direct' extraction method allows to do a linear extraction which greatly simplify the approach. However, a more 'realistic' method can be used allowing to directly compare the extracted values to TCAD stress calculation results. In this method, the stress relaxation length is obtained using a stress model combined with a current model. Two stress model have been used in this study:

- a polynomial stress model given by

$$\sigma = \frac{\sigma max}{1 + (\frac{\Lambda}{Lact})\alpha} \quad \text{(IV.2)}$$

- an exponential stress model expressed as:

$$\sigma = \sigma max.\ \exp[\left(\frac{\Lambda}{Lact}\right)\alpha] \quad \text{(IV.3)}$$

Concerning current variation with stress, three models are often used:

- a linear piezoresistive model:

$$I = Imax.(\text{-}\pi(\sigma - \sigma max) + 1) \quad \text{(IV.4)}$$

- an exponential model:

$$I = Imax.\exp(\text{-}\pi(\sigma - \sigma max)) \quad \text{(IV.5)}$$

- a model (MCmob) based on Kubo Greenwood (KG) approach and calibrated in chapter III:

$$I = Imax.\ (\text{MCmob}((\sigma - \sigma max)) + 1 \quad \text{(IV.6)}$$

Due to the limitations of the linear and exponential piezoresistive theory to capture mobility variation for high stress value (see Figure 77), the model MCmob, which is based in the KG simulations, is used in all this study to estimate the stress variation in the channel.

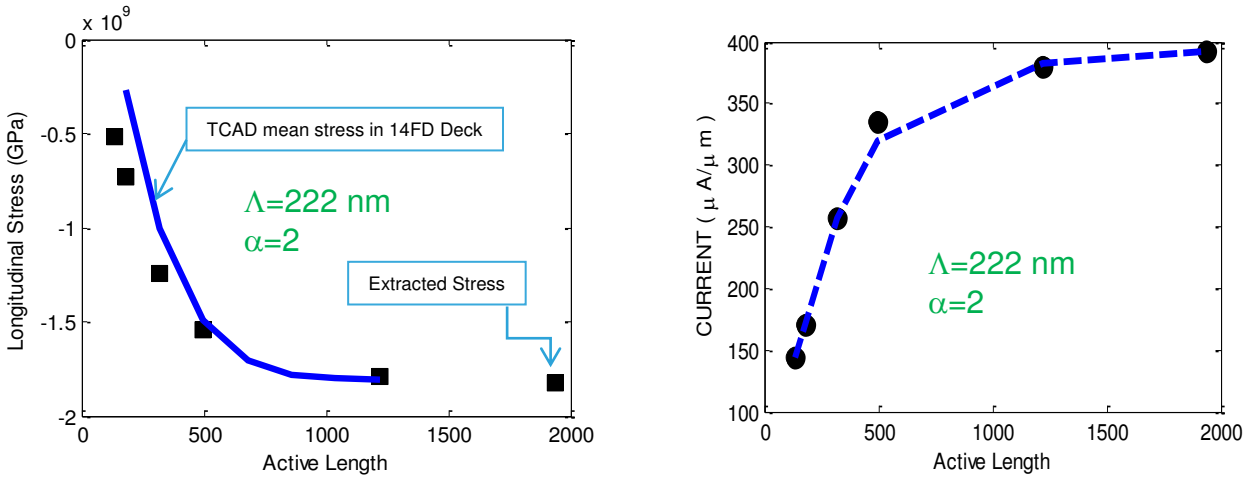

Figure 97 : a) variation of the extracted longitudinal stress (thanks to more realistic methods) as a function of L_{active} and comparison to TCAD simulations. b) variation of the current with active length using MCmob model.

In Figure 97, the longitudinal stress is extracted and then fitted with a polynomial stress model (equation IV.2). This results in a relaxation length parameters of nearly 220 nm (with α=2) representing the distance in which the longitudinal stress decay by a factor 2. In Figure 98, this method is applied to data coming from different wafers. A low variation of the extracted relaxation length is observed (from 195 nm to 230 nm). Note that TCAD simulations are closed to measurements.

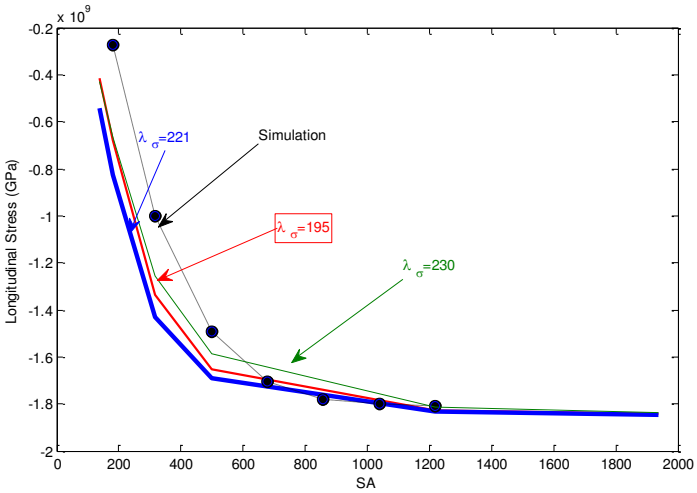

Figure 98 : *Evolution of the extracted longitudinal stress as a function of SA dimensions using the 'realistic method'.* TCAD simulations are added to the data from three different lots.

Then, a comparison between relaxation length extracted using the direct and the realistic methods have been performed on Figure 99. It shows that the value of this parameter is really different from one method to the other.

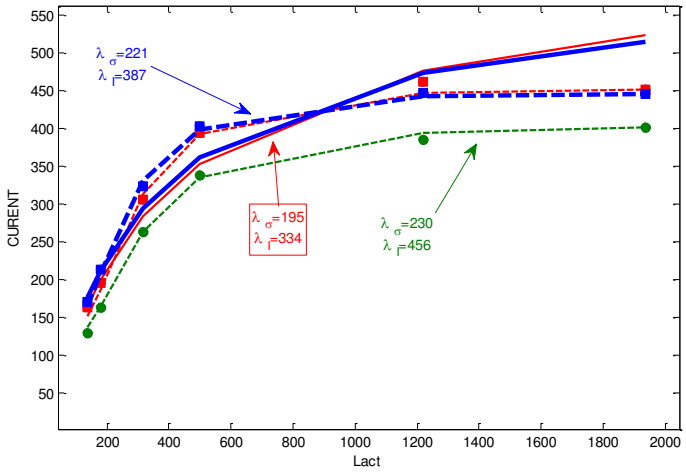

Figure 99: a) variation of the current as a function of L_{active}. Comparison between the direct approach (Full lines; *value λ_Γ) and the 'realistic* method (Dotted lines; *value λ_α*). Points are measurements.

To conclude, in this part, a 'realistic' method of extraction of the relaxation length has been proposed allowing a fast and robust way of comparison between split of different wafers and TCAD simulation.

IV.4.3 SiGe Source and Drain

28FDSOI and 14FDSOI technologies features raised SiGe source and drain as testified in the TEM picture of Figure 47 and simulated in Figure 100. In TCAD, using Sprocess (SYNOPSYS), the evaluation of the stress profile induced by the presence of the SiGe source and drain, requires a strong assumption. In fact, during the deposition of $Si_{0.7}Ge_{0.3}$ source and drain on a $Si_{0.78}Ge_{0.22}$ channel, we consider that the channel is fully stressed assuming that no relaxation has occurred (stress calculated from the difference in lattice parameters between these two materials). Although this assumption is valid for long channel devices, it may seems in contradiction with the important layout effects previously highlighted in this chapter. Considering the device of Figure 100, a uniaxial compressive stress of nearly 200 MPa is transferred to the channel from the source and drain, as shown in Figure 101.

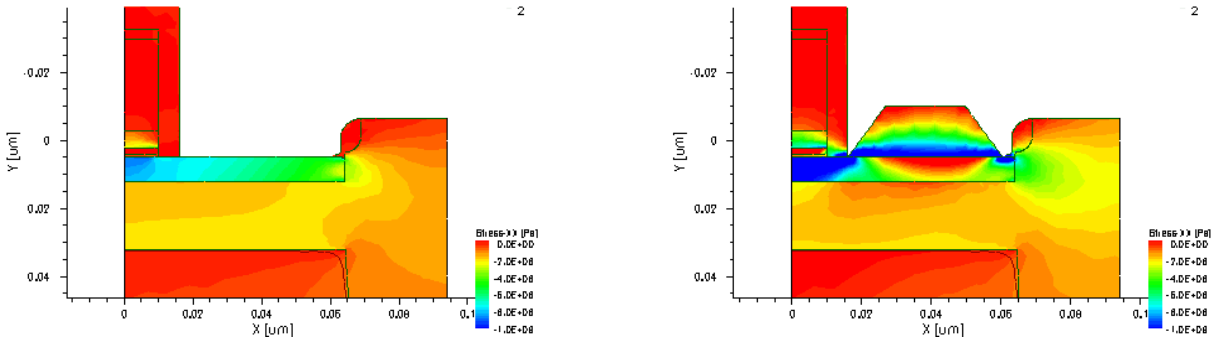

Figure 100 : Simulation of the deposition of SiGe source and drain for pMOSFET a) before and b) after the deposition of the $Si_{0.7}Ge_{0.3}$ S&D on top of the $Si_{0.78}Ge_{0.22}$ channel. Note that only the half of the structure is simulated. Device described in section IV.2.

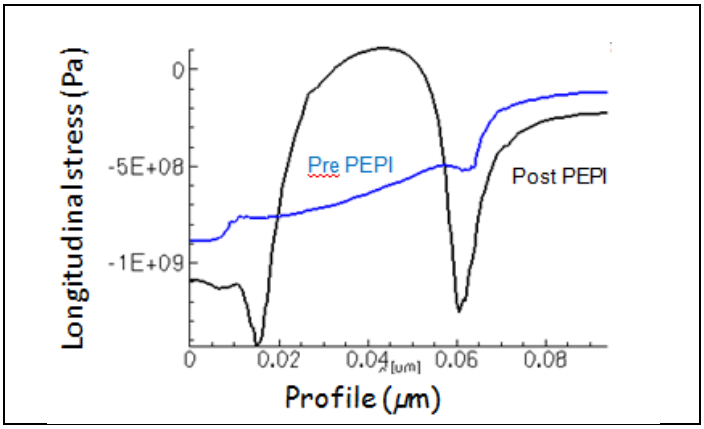

Figure 101 : Cut of the longitudinal stress profile in the channel. Devices of Figure 100. A uniaxial compressive stress of 200 MPa is added to the initially stressed $Si_{0.78}Ge_{0.22}$ channel.

The impact of the source and drain shape have been investigated to optimize the stress transfer to the channel. Facetted, semi-facetted and non-facetted source and drain have been compared (Figure 102) to the device with no S&D. A cut of the longitudinal stress in the channel is shown in Figure 103. The best configuration is obtained with facetted S&D which add a uniaxial compressive stress of nearly 200 MPa in the channel.

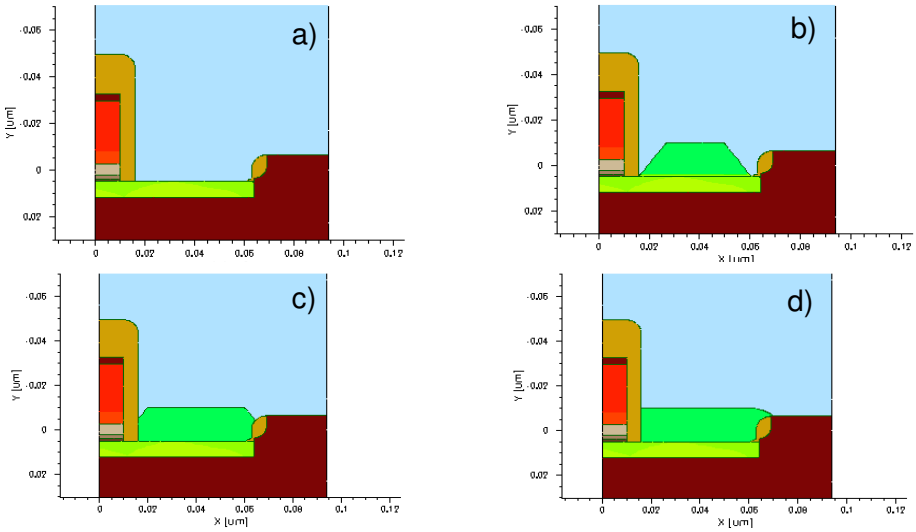

Figure 102 : Simulated structures for device performance optimization. a) no S&D, (b) facetted S&D, (c) semi-facetted and (d) non facetted.

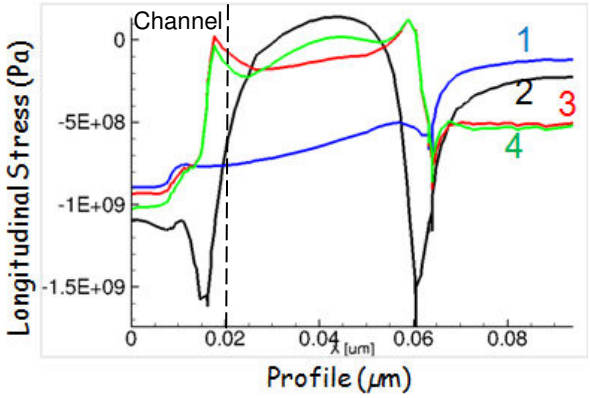

Figure 103 : Cut of the longitudinal stress profile in the channel. a) no S&D -> 1, (b) facetted S&D ->2, (c) semi-facetted -> 4 and (d) non facetted ->3. Devices of Figure 102.

- **Impact of an over-etch on the stress profile**

During spacer formation, an over-etch of the channel may appear before SiGe S&D epitaxy. This section addresses the impact of this over-etch on pMOS performances. The two studied structures have been considered (Figure 104). We consider a spacer recess from 0 to 2nm.

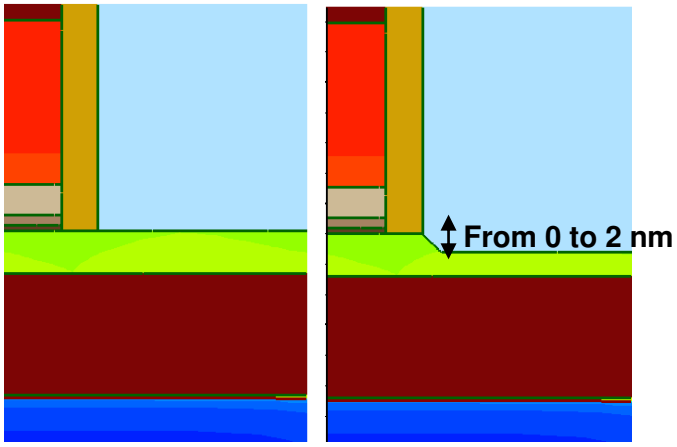

Figure 104 : TCAD pictures of the simulated structures. a) with and b) without spacer recess. Structures: L_{CH}=20 nm, L_{active}=130 nm, $xGe_{channel}$=22%.

After the step of spacer formation, a small decrease of the stress is observed in the channel (<50MPa) with increasing recess depth (Figure 105). However, on access region, the impact is stronger and can reach 200 MPa.

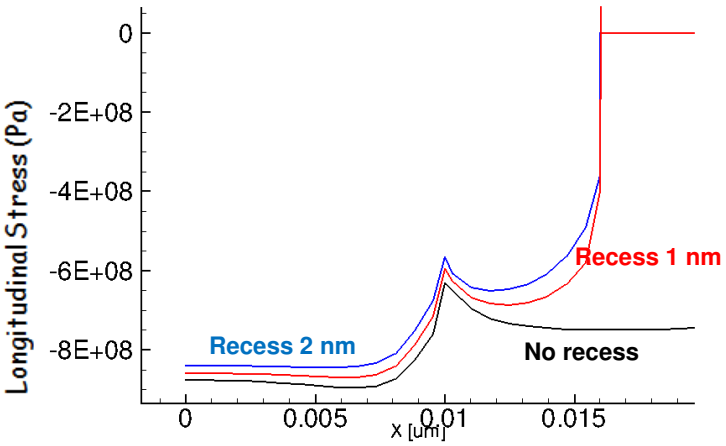

Figure 105 : 1D cut in the channel of the longitudinal stress with (1 nm and 2 nm) and without recess after spacer formation step.

The stress configuration in the channel has been simulated after source and drain epitaxy as shown in Figure 106a. No significant difference have been observed concerning the longitudinal stress with and without recess (Figure 106b). It highlights the fact that small recess can be tolerated (<2 nm) during the process flow without drastically changing the stress configuration.

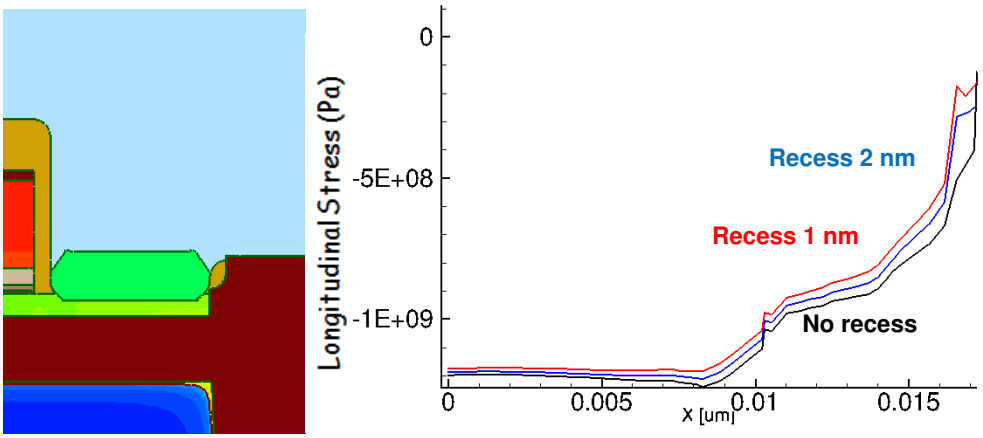

Figure 106 : a) TCAD pictures of the simulated structures. b) 1D cut in the channel of the longitudinal stress with (1 nm and 2 nm) and without recess after SiGe S&D epitaxy.

IV.4 Stress state optimization for 14FDSOI devices.

IV.4.1 Introduction of a piezoelectric layer

The integration of a piezoelectric layer to stress the channel in bulk as well as SOI transistors is an idea that has been extensively investigated in literature, and several patents on this topics have been deposited. It consists in adding a piezoelectric layer in the gate stack [142], or as capping layer [143] or under the channel [144], shown in Figure 107. However, few of them give details about the expected resulting stress in the channel.

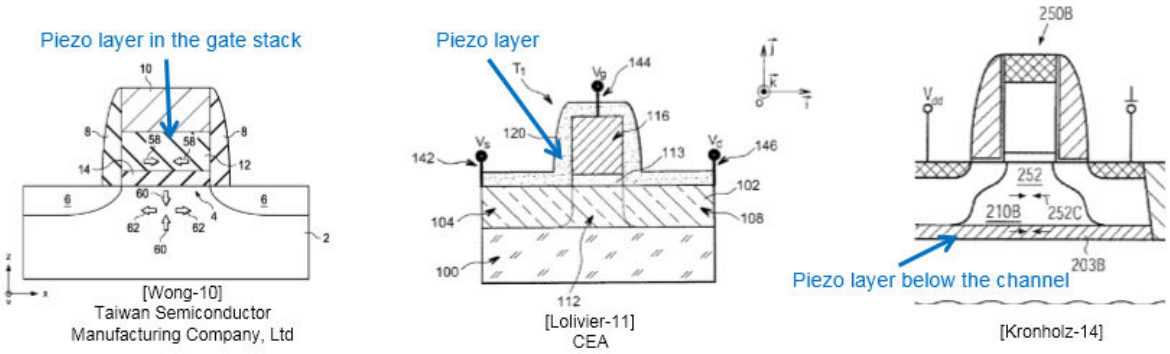

Figure 107 : Integration of a piezoelectric layer in the device: studied structures and patents in the literature. [Wong-10]: [142], [Lolivier-11]: [143] and [Kronholz-14]: [144].

The aim of this study was to investigate through simulation the idea of introducing a piezoelectric layer in the BOX, using the back bias to polarize it.

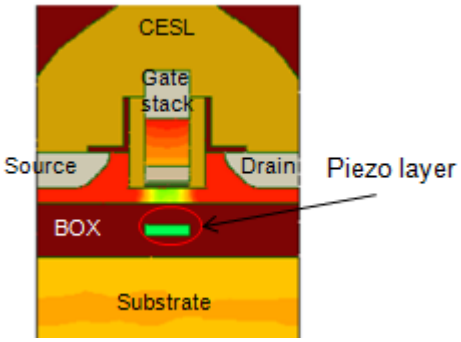

Figure 108 : TCAD simulation of a UTBB-FDSOI device. The layer in the BOX corresponds to the piezoelectric material

Typical properties of thin film piezoelectric material are summarized in Table 21. Note that these properties typically dependent on the layer thickness, which explain why so several different values can be found in the literature [145] [146] [147]. The material investigated here features both significant electromechanical d_{33} piezoelectric coefficient and dielectric constants. Other materials can be studied such as BaTiO3, LiNbO3 but they have poor d_{33} coefficients. Other material such as PMN-PT, PZN-PT (Lead magnesium niobate-lead titanate) have high d_{33} coefficients values, but also high values of dielectric constant epsilon (~5000). Recently, V-doped ZnO films have demonstrated an electromechanical d_{33} coefficient of pm/V [148] which is one order of magnitude higher than that of undoped samples.

Materials	ϵ_{33}	$d_{33}(pm/V)$
ZnO	10.9	5.9
AlN	10.5	3.9-5.5
GaN	~9	3.1

Table 21 : Piezoelectric material properties of ZnO, AlN and GaN.

As we cannot evaluate directly the strain/stress distribution induced by a piezoelectric layer, we did the study in three steps: 1) first, an evaluation of the electric field in the piezoelectric layer is performed, 2) then, we deduce the resulting strain/stress in this layer and 3) and finally we introduced the stress value in the simulation

Vertical electric field	Strain	Stress
Ey = 3.2*10^7 V/m	$\epsilon_T = 0.35\%$	$\sigma_T = 443\ MPa$
	$\epsilon_L = -0.17\%$	$\sigma_L = -160\ MPa$

Table 22 : Calculated values of strain and stress in V-doped ZnO films for an electric field of 3.2×10^7 V/m.

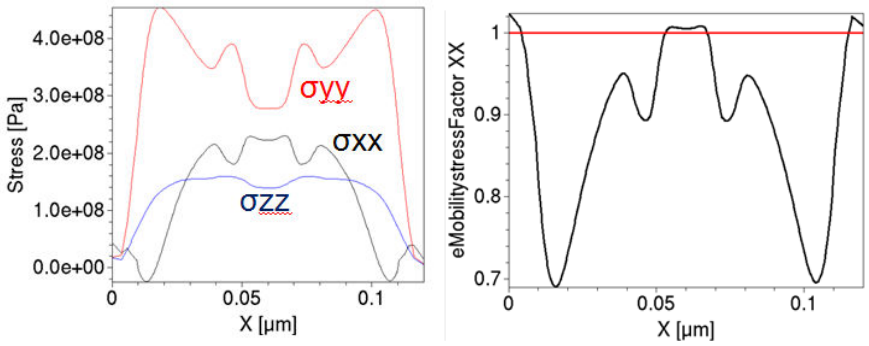

Figure 109 : a) Evolution *of the longitudinal* σ_{xx}, *transversal* σ_{yy} *and vertical* σ_{zz} stress component in the channel due to the introduction of a V-doped ZnO piezoelectric layer. b) corresponding mobility variation for electron.

To conclude, the stress transfer into the channel has been found weak, leading to modest mobility enhancement, even without considering all the process issues due to the integration of such a layer in a CMOS process. The dominant component is the vertical component (σ_{yy}) and decreases the electron mobility as shown in Figure 109.

IV.4.2 Stress configuration optimization for n- and p-type MOSFETs.

The use of global stress techniques such as strained SiGe channel or "strained Silicon On Insulator" (sSOI) leads to highly biaxially compressive or tensile channel respectively. Concerning p-type

14FDSOI technology, the SiGe channel is formed using the germanium condensation process and as described in chapter III, the resulting compressive stress is biaxial (can reach values up to 2 GPa). However, we have previously highlighted the fact that longitudinal uniaxial stress (σ_L) improves much better the hole mobility than biaxial stress. In other words, p-type transistors are stressed in a non-optimal way. Concerning n-type 14FDSOI technology, the channel stress configuration is mainly tensile and uniaxial. Indeed, the main stressors are SiC source and drain and STI. Next generations of n-type MOSFETs will be processed on sSOI substrate resulting in tensile biaxial stress but in that case, this configuration is favorable for the mobility (as shown in Figure 79). During this PhD, patents have been deposited concerning the optimization of the stress configuration aiming at improving p-type MOSFET performances. In this part, the different deposited patents are described.

- **Directional STI patterning to optimize the stress configuration in sSOI and SiGe-based devices**

The idea of these patents is to use a directional STI patterning to optimize the stress configuration in the channel. This directional selection is possible by means of the independent 'RX' end 'RC' masks (Figure 110 and Figure 111) which are used to form isolation trenches delimiting the width and the length of the SOI structure respectively.

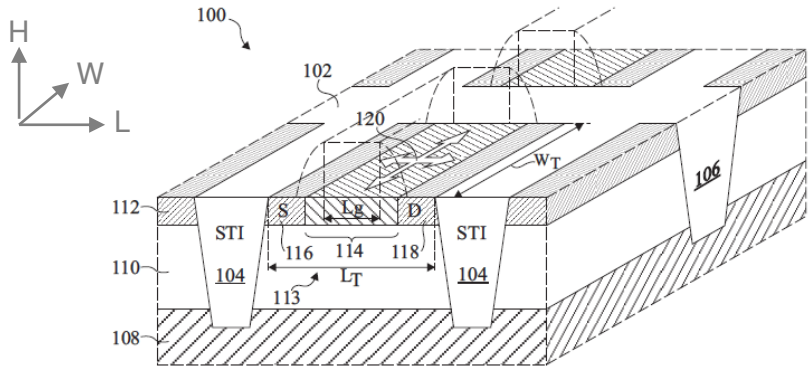

Figure 110 : 3D schematic of the SOI transistor. This figure is extracted from the deposited patent [150]. Concerning p-type MOSFETs, the performance improvement consists in relaxing the transversal stress value (W direction).

Actually, there is no differentiation between process steps forming the isolation trenches in these two directions (Figure 112a). Consequently, the STI delimiting the length and the width directions undergo the same process steps and the stress configuration in these directions depends exclusively on the dimensions of the active layer (L_{active} and W_{active} respectively). Note that the stress value depending on these dimensions is shown in section IV.3. Based on the differentiation between RX and RC masks (Figure 112b), we proposed in Table 23, several process steps solutions to optimize the stress configuration in p-type MOSFETs. All these solutions aims at decreasing the initial compressive transversal stress value (width direction).

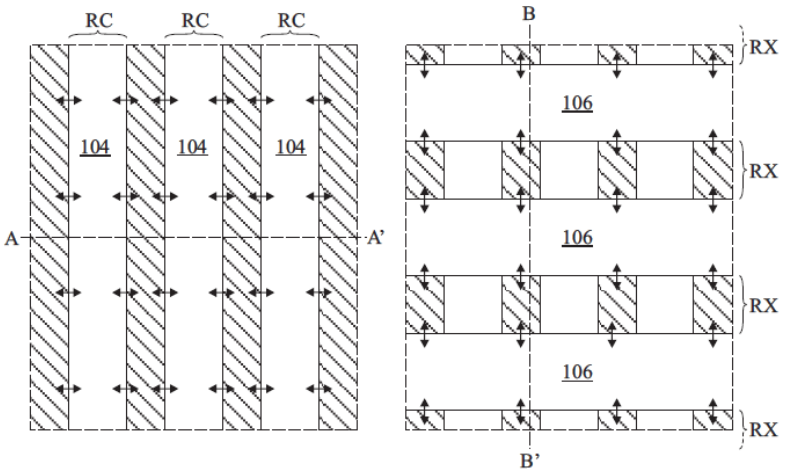

Figure 111 : a) Plan view of a RX mask used to form isolation trenches 106 delimiting the width of the SOI structure. a) Plan view of a RC mask used to form isolation trenches 104 (STI) delimiting the length of the structure. This figure is extracted from the deposited patent [150].

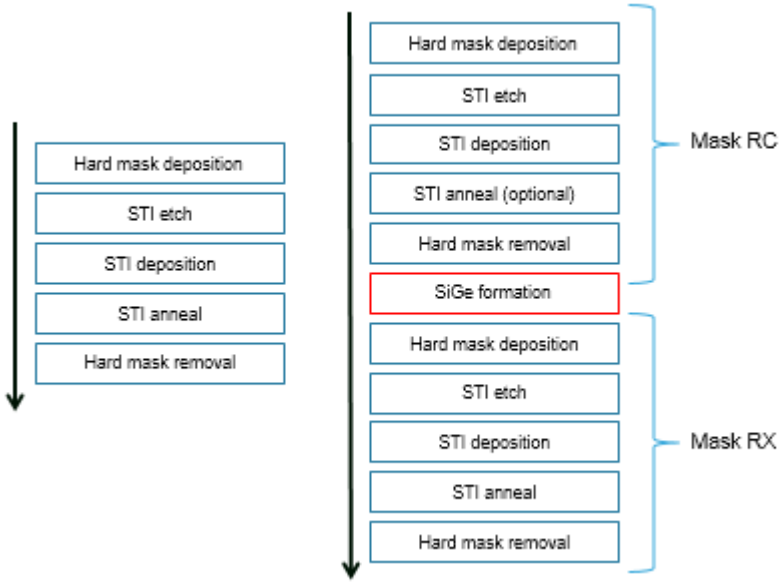

Figure 112 : Description of a) classical and b) proposed STI process steps.

Mask	Process steps	Comments
RX	SiGe channel (if SiGe first)	
	Hard mask deposition	
	STI etching	
	STI deposition	Material m_{RX}, deposition temperature Td_{RX}
	STI anneal	Temperature Ta_{RX}, time t_{RX}
	Hard mask removal	
	SiGe channel (if SiGe last)	
RC	SiGe channel (if SiGe first)	
	Hard mask deposition	
	STI etching	
	STI deposition	Material m_{RC}, deposition temperature Td_{RC}
	STI anneal	Temperature Ta_{RC}, time t_{RC}
	Hard mask removal	
	SiGe channel (if SiGe last)	

Table 23 : Description of the proposed STI process flow to optimize the stress configuration in MOSFETs

The first idea concerns the SiGe channel formation. In part III.3.1, we demonstrated a strong reduction of the stress relaxation when the channel is formed after STI process steps (SiGe last). Consequently, a first solution can be proposed. It consists in forming the SiGe channel after STI formation steps delimiting the length direction (Mask RC), as described in Figure 113. In this configuration, the longitudinal stress undergo a lower relaxation because STI are formed before SiGe channel formation (cf to part comparing SiGe first and last). Concerning the width direction, STI formation steps are done after channel formation and consequently, a strong relaxation of the transversal stress occurs.

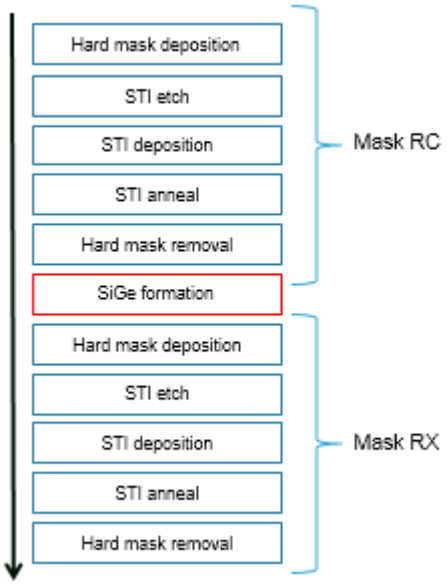

Figure 113 : Description of the proposed process flow to decrease the stress relaxation only in the length direction only.

The second proposition concerns the STI deposition step where two alternative solutions can be used: the deposited material and the temperature during the deposition can be different for trenches 106 and 104 (Figure 110). These two key parameters will influence the stress configuration through the thermal deformation coefficient of the deposited STI materials. Thus, the stress in the longitudinal and transversal directions can be adapted. The third idea deals with the STI anneal step. In that case, the temperature and the durations of anneals can be adapted to promote the relaxation in one direction.

- **Directional Implantation in STI for SiGe –based and sSOI-based devices.**

The proposition is to use the directional STI patterning explained in the previous section to selectively implant dopants in STI delimiting one direction and not in the second isolation trenches. The aim of this implantation is to alter the viscosity of the STI as described in [149]. In our case, STI delimiting the width are implanted to enhance the stress relaxation in this direction. An example of simplified process flow is presented in Figure 114.

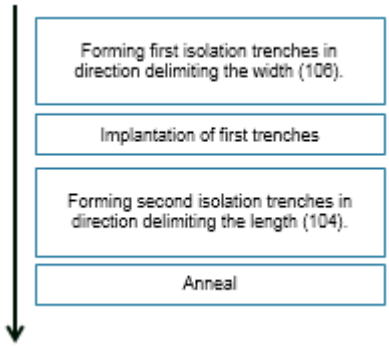

Figure 114 : Description of the proposed process flow to selectively implant trenches delimiting the width direction to enhance the relaxation.

- **Stress memory technique using directional STI masks for device performance improvement.**

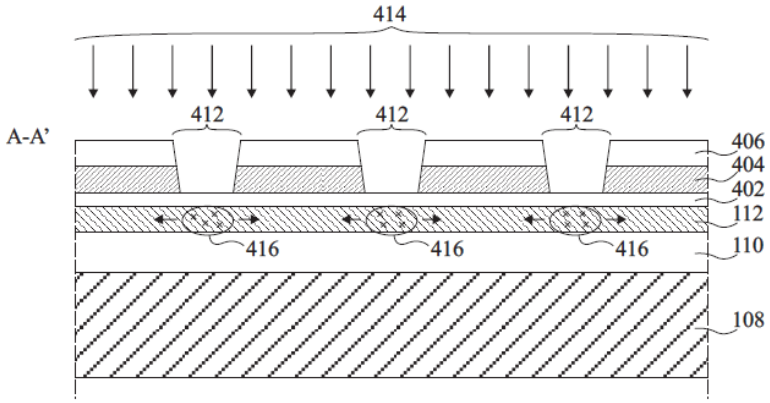

Figure 115 : Cross section of the SOI transistor. This figure is extracted from the deposited patent [152]. The step 414 corresponds to the implantation of Germanium atoms through trenches 412. Layer 112 is the semiconductor, layer 110 the insulator and 404 and 406 correspond to hard mask layers.

This idea consists in using the directional STI patterning explained in the first deposited patent to selectively amorphize the silicon region 416 (areas where STI will be formed). This amorphization can be performed by implanting germanium at high energy level and dose (for example between 30 KeV and 50 KeV, and at a density of between 10^{14} and $5x10^{14}$ atoms/cm^3). It would lead to a tensile stress being exerted by the regions 416 (Figure 15) into the portions of the semiconductor layer 112. The phenomenon of stress induced by amorphization has been for example discussed in more detail in [139]. While the stress is maintained in the semiconductor layer 112, an annealing operation is for example performed to temporally decrease the viscosity of the hard mask nitride and the BOX (corresponding to layer 110). By temporally decreasing the viscosity of the insulators, it relaxes such that, when it cools again and the viscosity is increased, the stress in the semiconductor layer 112 is maintained not only by the regions 416, but also by the underlying BOX layer and by the hard mask stack (layers 406 and 404). Then, the depth of the trenches 412 is extended by a further etching step to form the isolation trenches of Figure 106. In doing so, all or most of the germanium atoms implanted into the semiconductor layer 112 are removed, and some relaxation of the semiconductor layer 112 occurs. However, due the presence of the BOX and the hard mask stack, a certain level of stress should remain in the semiconductor layer 112.

In these part, we have explained the general content of the deposited patents. More details can be found in [150] [151] [152].

IV.5 Conclusion

In the first part of this chapter, a brief description of the developed TCAD deck to model 14FDSOI technology is performed. Then, in the second part, we present a full mechanical study of the stress configuration in 14FDSOI technology through TCAD simulations and NBD measurements. Solutions to optimize the stress configuration in sSOI and SiGe-based devices are proposed. We conclude that while the integration of a piezoelectric layer in the BOX remains technologically difficult for a low performance improvement, several solutions have been proposed to enhance devices performances. These solutions are all based on the use of a directional STI patterning to differentiate the length and the width directions. Thus, the stress in these two directions can be independently controlled by adapting process steps according to propositions developed in section III.4.2. Independently, in this chapter, we presented mechanical stress studies for 14FDSOI technology support such a as the impact of SiGe source and drain on channel stress configuration.

Conclusions

Thesis summary:

Technological computer-aided design (TCAD) is a powerful tool to support technological development within the industry. Indeed, TCAD support for FDSOI technology development can reduce cost and development time but also secure technology choices. Based on STMicroelectronics strategies, this PhD work aimed at developing the TCAD modeling for 28nm, 14nm and 10 nm FDSOI devices, with a particular focus on stress engineering. From a process point of view, it has consisted in developing a simulation methodology capable of reproducing accurately 14 nm FDSOI process flow and the final topography of the device. An approach to model process-induced stress has been set-up, focusing on the three main sources of stress in the device, namely SiGe channel, SiGe source and drain, and material deposited at high temperature (such as STI and gate stack for example). Concerning device simulation, a "top down" approach has been set-up. It has consisted in using advanced physical-based solvers as a reference for TCAD empirical model calibration.

In more detail, in the first part of chapter 1, the main models implemented in state of the art device simulators have been reviewed. First, a description of methodologies used to calculate the conduction and valence band structure of silicon, germanium and silicon germanium alloy has been performed, highlighting how stress and confinement are taken into account. In the second part, a multi-scale strategy for MOSFET device modeling ranging from classical drift diffusion models to NEGF calculation has been presented. In the last part, the models for the main scattering mechanisms in semi-classical solvers such as MSMC or KG has been reviewed. The assumptions and range of validity of these models have also been highlighted, and the developments of the in-house STMicroelectronics KG solvers have been discussed.

Chapter 2 deals with a comparison of the different approaches currently available to model low field transport in advanced Fully Depleted SOI transistors. Electron and hole mobilities have been calculated using four different solvers: the STMicroelectonics in-house solver (UTOXPP), the commercial solver Sband from Synopsys, the MSMC solver from the University of Udine and TB_SIM, the NEGF solver from CEA. Simulations are then compared to split CV mobility measurements performed on state of the art FDSOI devices. Using a large range of split-CV measurements, the impact of the Equivalent Oxide Thicknesses (EOT), the back voltage and the temperature have been investigated, leading to an extensive comparison between state of the art models and experiments.

Chapter 3 aimed at describing the methodologies used during this thesis to model intentional and non-intentional process induced stress. Simulations have been compared to nano-beam diffraction (NBD) strain measurements at the nanometer scale. The second objective is to analyze and calibrate (on advanced transport solvers) available TCAD models to efficiently account for the influence of stress on mobility in a large level of stress (up to 2GPa). Finally, in this chapter, a complete methodology for process-induced stress simulations and its impact on electrical characteristics has been set up. This enables accurate and efficient TCAD simulations of strained-Si FDSOI MOSFETs in state of the art CMOS technology.

Chapter 4 presents applications of the previously presented methodologies to model advanced CMOS devices. Mechanical simulations has been performed to model realistic stress profile in 14FDSOI

transistors from process simulation, with an emphasis on the modeling of the relaxation of the stress during STI process steps and the effect of SiGe source and drain. Solutions to optimize the stress configuration in sSOI and SiGe-based devices have been presented. These solutions are based on the use of a directional STI patterning to differentiate the length and the width directions. Thus, the stress in these two directions can be independently controlled by adapting process steps according to propositions developed in chapter III.

Future works and recommendations:

This work has been focused so far on 28 nm and 14 nm FDSOI technologies featuring SiC/SiGe source and drain and SiGe channel. However, additional technological solutions must be investigated for 10nm FDSOI technology such as sSOI substrate, Germanium or III-V channel material. From a process point of view, the stress configuration in the channel should be different and thus re-optimized. From an electrical point of view, new mechanisms and challenges will appears. Examples are listed below:

- Electrostatic and transport for III-V materials.
- Remote surface roughness scattering (with the high-k/IL interface).
- Remote phonon scattering.
- Source to drain tunneling.

Concerning the stress engineering, we highlighted in this manuscript that the strong stress relaxation observed during STI patterning cannot be explained only by an elastic relaxation. It suggests that another phenomenon further degrades the stress and is probably linked to the nature of the SiGe / BOX interface. We suspect that the bonding between the SiGe layer and the BOX surface is weak and cannot hold the stress in the channel during STI patterning. Further investigations concerning this hypothesis should be performed. Other sources of stress (such as induced by silicidation for instance) should also be considered.

Finally concerning the modeling of stress-induced mobility variation, a new model for surface roughness should be developed and calibrated for the full range of effective field.

Annexes

Annexe I: Determination of the potential produced by a point charge

a) Analytical solution

The equation to solve is the following:

$$\left[\frac{\partial}{\partial z}\,\epsilon(z)\,\frac{\partial}{\partial z} - \epsilon(z).Q^2\right] G(q,z,z_0) = -e.\delta(z-z_0) \tag{I.1}$$

In previous UTOX version, an analytical solution was implemented.

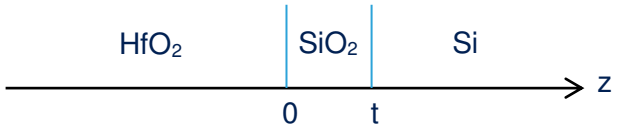

Figure a1: Schematic of the studied 1D device.

A general solution of (I.1) for the potential can be expressed in the three materials of Figure a1 in the form:

$$G(q,z,z_0) = -\frac{1}{2q} * \begin{cases} a_q e^{-Q|z-z_0|} + b_q e^{-Q|z+z_0|} & (z<0) \\ c_q e^{Q(z+z_0)} + d_q e^{-Q(z-z_0)} & (0 \le z \le t) \\ f_q e^{-Q(z-z_0)} & (z \ge t) \end{cases} \tag{I.2}$$

And the boundary conditions are:

$$\begin{cases} G_Q(z=0^-,z_0) = G_Q(z=0^+,z_0) \\ G_Q(z=t^-,z_0) = G_Q(z=t^+,z_0) \end{cases} \tag{I.3}$$

$$\begin{cases} \kappa \dfrac{dG_Q(z=0^-,z_0)}{dz} = \epsilon_i \dfrac{dG_Q(z=0^+,z_0)}{dz} \\ \epsilon_i \dfrac{dG_Q(z=t^-,z_0)}{dz} = \epsilon_s \dfrac{dG_Q(z=t^+,z_0)}{dz} \end{cases} \tag{I.4}$$

$$\frac{dG_Q(z={z_0}^+,z_0)}{dz} - \frac{dG_Q(z={z_0}^-,z_0)}{dz} = -1 \tag{I.5}$$

Eq. I.5 implies $a_q = 1$ and Eq. I.3 and Eq.I.4 gives:

$$\begin{cases} 1 + b_Q = c_Q + d_Q \\ c_q e^{Qt} + d_Q e^{-Qt} = f_Q e^{-Qt} \\ 1 - b_Q = \dfrac{\epsilon_i}{\kappa}(d_Q - c_Q) \\ c_Q e^{Qt} - d_Q e^{-Qt} = -\dfrac{\epsilon_s}{\epsilon_i} f_Q e^{-Qt} \end{cases} \tag{I.6}$$

$$\begin{pmatrix} 1 & -\kappa/\epsilon_i & -\kappa/\epsilon_i & 0 \\ 1 & -1 & 1 & 0 \\ 0 & e^{Qt} & e^{-Qt} & -\epsilon_i/\epsilon_s e^{-Qt} \\ 0 & e^{Qt} & -e^{-Qt} & e^{-Qt} \end{pmatrix} * \begin{pmatrix} b_q \\ c_q \\ d_q \\ f_q \end{pmatrix} = \begin{pmatrix} -1 \\ 1 \\ 0 \\ 0 \end{pmatrix} \quad \text{(I.7)}$$

In [86], this system is solved numerically to find coefficients b_q, c_q, d_q and f_q.

The calculation of the Green function using this method implies two major drawbacks. The first is that only three materials (with different ε) can be treated and consequently, our Green function is inaccurate in the case of high-k FDSOI devices (we actually treat only the three materials: high-k, IL and Si). The second drawback concerns the boundary conditions: layers at each sides of the simulation domain are considered as infinitely thick. It is however important in the case of high-k metal gate devices to set G to zero since the metal gate screens the potential.
In order to treat the general case, i.e. an infinite number of layers with different ε, we can use the finite difference method to solve the equation. In part II, this method is applied to a non-uniform grid.

b) Finite difference method

$$\left[\frac{\partial}{\partial z}\,\epsilon(z)\,\frac{\partial}{\partial z} - \epsilon(z).Q^2\right] G(q,z,z_0) = \delta(z-z_0) \quad \text{(II.1)}$$

$$\rightarrow\ G''(z)*\epsilon(z) + \epsilon'(z).G'(z) - \epsilon(z).Q^2.G(z) = \delta(z-z_0) \quad \text{(II.2)}$$

For non-uniform grid, G'' and G' can be expressed from Taylor expansion:

$$G(z_i+1) = G(z_i) + G'(z_i).h_i^+ + \frac{G''(z_i)}{2}.(h_i^+)^2 \quad \text{(II.3)}$$

$$G(z_i-1) = G(z_i) - G'(z_i).h_i^- + \frac{G''(z_i)}{2}.(h_i^-)^2 \quad \text{(II.4)}$$

After multiplying h_i^- to (II.3) and h_i^+ to (II.4), and summing:

$$G''(z_i) = 2.\frac{h_i^-.G(z_i+1) + h_i^+.G(z_i-1) - (h_i^+ + h_i^-)G(z_i)}{(h_i^-)^2.h_i^+ + (h_i^+)^2.h_i^-} \quad \text{(II.5)}$$

$$G''(z_i) = 2.\frac{\frac{h_i^-}{h_i^+}.G(z_i+1) + G(z_i-1) - \left(1+\frac{h_i^-}{h_i^+}\right)G(z_i)}{(h_i^-).(h_i^+ + h_i^-)} \quad \text{(II.6)}$$

And:

$$G'(z_i) = \frac{G(z_i+1) - G(z_i-1)}{h_i^+ + h_i^-} \quad \text{(II.7)}$$

$$G'(z_i) = \frac{h_i^-.G(z_i+1) - h_i^-.G(z_i-1)}{(h_i^-).(h_i^+ + h_i^-)} \quad \text{(II.8)}$$

Applying the approximations (II.6) and (II.8) to Eq.II.2, we can determine the finite difference equation:

$$2.\frac{\frac{h_i^-}{h_i^+}.G(z_i+1)+\ G(z_i-1)-\left(1+\frac{h_i^-}{h_i^+}\right)G(z_i)}{(h_i^-).(\ h_i^+ + h_i^-)}+\frac{\epsilon'(z_i)}{\epsilon(z_i)}.\frac{h_i^-.G(z_i+1)-h_i^-.G(z_i-1)}{(h_i^-).(\ h_i^+ + h_i^-)}-Q^2G(z_i)=\frac{\delta(z-z_0)}{\epsilon(z_i)}$$

Multiplying by $(h_i^-).\frac{h_i^+ + h_i^-}{2}$ gives:

$$\frac{h_i^-}{h_i^+}.G(z_i+1)+\ G(z_i-1)-\left(1+\frac{h_i^-}{h_i^+}\right)G(z_i)+\frac{\epsilon'(z_i)}{2.\epsilon(z_i)}.(h_i^-.G(z_i+1)-h_i^-.G(z_i-1))-\frac{Q^2.(h_i^-).(\ h_i^+ + h_i^-)}{2}.G(z_i)$$
$$=\frac{\delta(z-z_0)}{2.\epsilon(z_i)}.(h_i^-).(\ h_i^+ + h_i^-)$$

So:

$$\left(1-\frac{\epsilon'(z_i).h_i^-)}{2.\epsilon(z_i)}\right).G(z_i-1)-\left[\left(1+\frac{h_i^-}{h_i^+}\right)+\frac{Q^2.(h_i^-).(\ h_i^+ + h_i^-)}{2}\right].G(z_i)+\left[\frac{h_i^-}{h_i^+}+\frac{\epsilon'(z_i).h_i^-)}{2.\epsilon(z_i)}\right]G(z_i+1)$$
$$=\frac{\delta(z-z_0)}{2.\epsilon(z_i)}.(h_i^-).(\ h_i^+ + h_i^-) \qquad \text{(II.9)}$$

This equation has the form:

$$b_i.G(z_i-1)+d_i.G(z_i)+a_i.G(z_i-1)=\ \delta(z-z_0).f_i$$

$$\text{With}\begin{cases} b_i = 1-\frac{\epsilon'(z_i).h_i^-}{2.\epsilon(z_i)} \\ d_i = -\left(1+\frac{h_i^-}{h_i^+}\right)-\frac{Q^2.(h_i^-).(\ h_i^+ + h_i^-)}{2} \quad \text{and } f_i=(h_i^-).\frac{(\ h_i^+ + h_i^-)}{2.\epsilon(z_i)} \\ a_i = \frac{h_i^-}{h_i^+}+\frac{\epsilon'(z_i).h_i^-)}{2.\epsilon(z_i)} \end{cases}$$

So eq.II.1 takes the form:

$$AG=\delta.f \qquad \text{(II.10)}$$

$$\text{with } A=\begin{pmatrix} d_0 & a_0 & 0 & \cdots & \cdots & 0 \\ b_1 & d_1 & a_1 & \ddots & & \vdots \\ 0 & b_2 & d_2 & a_2 & \ddots & \vdots \\ \vdots & \ddots & \ddots & \ddots & \ddots & 0 \\ \vdots & & \ddots & \ddots & d_{N-2} & a_{N-2} \\ 0 & \cdots & \cdots & 0 & b_{N-2} & d_{N-1} \end{pmatrix} \qquad \text{(II.11)}$$

$$\text{and } \delta=(0 \quad \cdots \quad 0 \quad \delta_{ip} \quad 0 \quad \cdots \quad 0)^T$$

$$\delta_{ip}=(h_{ip}^-).\frac{\left(\ h_{ip}^+ + h_{ip}^-\right)}{2.\epsilon\left(z_{ip}\right)}$$

- <u>Boundary conditions:</u>

The Dirichlet boundary conditions are imposed by setting the two values of the potential at each extremity.

$$G(0) = g_0 \quad \text{and} \quad G(N-1) = g_{N-1}$$

In our case, the potential is fixed to zero at each sides.

- Matlab implementation:

Using Matlab, we can solve Eq.II.10 numerically ($G = \text{inv}(A) * \delta$). It is however CPU time consuming.
An analytical solution to inverse trigonal matrices has been developed in [El-Mikkawy-06] and applied to this equation in [87]. Three vectors are defined as:

$$\alpha_i = \begin{cases} 1 & \text{if } i = 0 \\ d_0 & \text{if } i = 1 \\ d_{i-1}\alpha_{i-1} - b_{i-1}a_{i-2}\alpha_{i-2} & \text{if } i = 2,3,4,\ldots.N \end{cases}$$

$$\beta_i = \begin{cases} 1 & \text{if } i = N \\ d_{N-1} & \text{if } i = 1 \\ d_i\beta_{i+1} - b_{i+1}a_i\beta_{i+2} & \text{if } i = N-2, N-3, \ldots \end{cases}$$

$$u_i = \begin{cases} \dfrac{\beta_1}{d_0\beta_1 - b_1a_0\beta_2} & \text{if } i = 0 \\ \dfrac{\alpha_{N-1}}{d_{N-1}\alpha_{N-1} - b_{N-1}a_{N-2}\alpha_{N-2}} & \text{if } i = N-1 \\ \dfrac{\beta_{i+1}\alpha_i}{d_i\beta_{i+1}\alpha_i - b_ia_{i-1}\beta_{i+1}\alpha_{i-1} - b_{i+1}a_i\beta_{i+2}\alpha_i} & \text{otherwise} \end{cases}$$

The Green's function is finally obtained by:

$$G_i = \begin{cases} \dfrac{\delta_{ip}\alpha_i u_{ip}(-1)^{ip-i}\prod_{k=0}^{ip-i} a_{ip-k}}{\alpha_{ip}} & \text{if } i < ip \\ u_{ip}\delta_{ip} \quad \text{if } i = ip & \text{if } i = ip \\ \dfrac{\delta_{ip}\beta_{i+1}u_{ip}(-1)^{i-ip}\prod_{k=0}^{i-ip} b_{ip+k}}{\beta_{ip+1}} & \text{if } i > ip \end{cases} \qquad \text{(II.12)}$$

Annexe 2: Sdevice syntax for TCAD drift diffusion device simulations

The syntax describing the physic models in the channel region is shown in figure a2. This includes:

- Generation recombination models (Shockley-Read-Hall and Auger mechanisms)
- A band gap model (EffectiveIntrinsecDensity)
- Density-gradient quantization model (eQuantumPotential hQuantumPotential)
- Mobility models accounting for bulk mobility (PhuMob corresponds to Philips unified mobility model [100]) for degradation of the mobility in thin films (ThinLayer), for mobility degradation due to charge at high-k/IL interface

```
Physics (Region= "R.SOI") {

        Recombination ( SRH(DopingDep) Auger )
        EffectiveIntrinsicDensity( Slotboom )
        Fermi
        eQuantumPotential hQuantumPotential
        Mobility (
                -ConstantMobility
                PhuMob
                ThinLayer
                Enormal(
                   InterfaceCharge(SurfaceName="S1")
                   Lombardi_highk)
                HighFieldSaturation(EparallelToInterface)
        )
```

Figure a2: Description of the Sdevice models describing the physics in the channel region.

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Résumé:

L'industrie des semi-conducteurs a réduit de façon constante les dimensions des transistors MOS pour améliorer les performances et réduire leurs coûts. Ainsi, à partir du nœud technologique 20µm jusqu'à 90 nm, les améliorations des performances étaient essentiellement dues à la réduction des dimensions des transistors selon des règles d'échelle (comme illustré sur la figure I pour l'oxyde de grille). Depuis le nœud 90 nm, la réduction classique des dimensions MOSFET fait faces à des limites physiques et économiques. En effet, les règles réduction des dimensions des dispositifs qui ont permis depuis plus de 30 ans, à l'industrie des semi-conducteurs, d'améliorer en permanence les performances des transistors tout en réduisant leurs coûts, ont rencontré des limites. Les défis liés à ces limites sont le contrôle des courants de fuite (effets de canal court (SCE), le courant de tunnel à travers l'isolant de grille ...), la mise en valeur des propriétés de transport dans le canal, et le contrôle de la variabilité (en raison des fluctuations processeur de dopage).

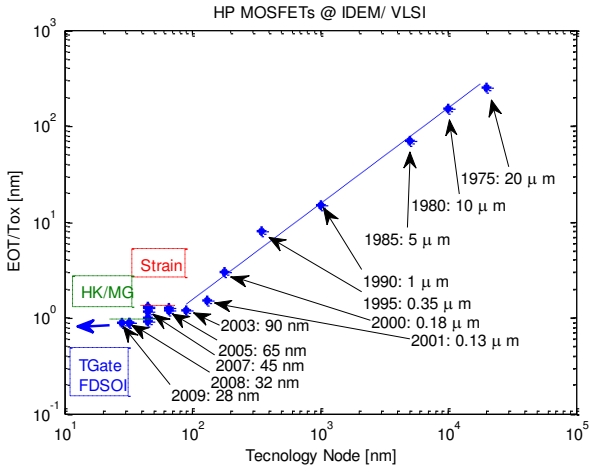

Figure I: Evolution des dimensions de l'oxyde de grille en fonction des *nœuds* technologiques à HP. Les données sont extraites de présentations IEDM/VLSI.

Ainsi, de nos jours, l'exigence de performance ITRS a conduit à l'introduction de «boosters» de technologie, tels que l'utilisation de nouvelles architectures de transistors (FDSOI, trigate), des diélectriques high-k, de l'ingénierie de stress ou de nouveau matériaux de canal (Ge, III- V). La diversité des solutions technologiques a mené les industriels à adopter différentes stratégies de développements comme illustré sur la figure II. Ainsi, STMicroelectronics a débuté le développement de la technologie planaire FDSOI. Cette architecture présente plusieurs avantages comme un meilleur contrôle électrostatique du canal, réduisant les effets de canaux court (SCE). La tension de seuil du transistor peut être ajustée en appliquant une tension sur la face arrière et ils présentent moins de variabilité (canal non dopé).

Pour faire face à tous ces défis technologiques, la TCAD (Technology Computer Aided Design), et un outil permettant de guider le développement des technologies avancées. En effet, le support TCAD pour le développement de la technologie FDSOI permet à la fois de réduire les coûts et les temps de

développement. En lien avec la stratégie de développement de STMicroelectronics, ce travail de thèse a pour objectif d'améliorer la modélisation pour les technologies 28/14 and 10FDSOI avec un intérêt particulier sur l'ingénierie de la contrainte. Dans ce contexte, deux axes de développement majeurs ont été identifié correspondant à la simulation du process et des performances électriques du transistor.

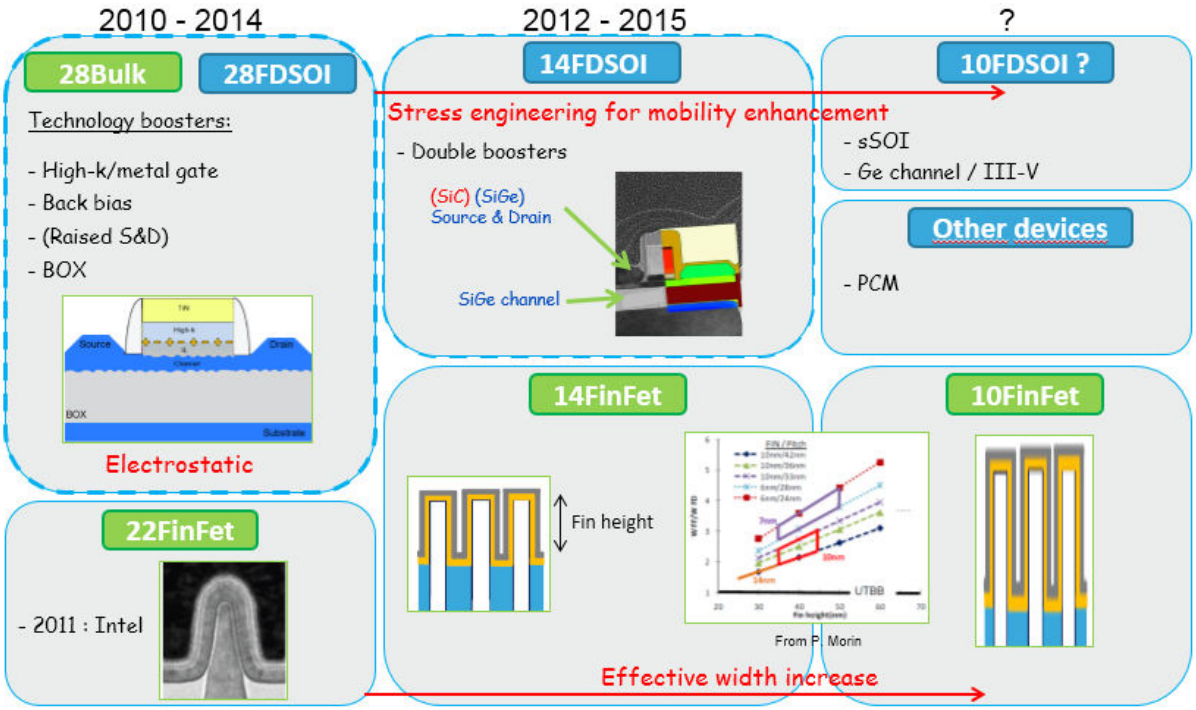

Figure II: Stratégies de développement des transistors à ST et INTEL.

Les principaux défis de ce travail de thèse sont:

- d'améliorer les outils de simulations internes à STMicroelectronics (domaine de validité et l'applicabilité aux technologies de pointe, des avantages et des inconvénients, par rapport aux autres modèles ...). En particulier, l'un de ce solveur (UTOXPP) est un logiciel de résolution 1D Poisson-Schrodinger couplé avec le formalisme de Kubo-Greenwood (KG) pour les calculs de mobilité. Il peut gérer les dispositifs ultra-minces, la plupart des mécanismes de diffusion pertinents et la contrainte. Il est utilisé comme un outil de référence pour la calibration de modèle TCAD empiriques et la validation des modèles de mobilité. Malgré plusieurs efforts le long des dix dernières années, ce sujet constitue encore un sujet de recherche, comme la capacité de solveurs 1D KG de reproduire la mobilité mesurée sur un grand nombre d'échantillons avec les mêmes paramètres.

- de développer une approche pour simuler le stress induit par les processus dans l'état des transistors MOS d'art. Dans ce cas, le processus Synopsys Sentaurus de logiciels industriels (Sprocess) a été utilisé comme une "fab virtuelle" pour simuler chaque étape du procédé et pour évaluer le niveau de stress mécanique. Les solutions technologiques pour améliorer la configuration de stress sont également abordées.

- d’être en mesure de reproduire la caractéristique électrique d'un ensemble complet de données expérimentales pour les technologies 28 nm et 14nm FDSOI.

Pour étudier ces défis, des collaborations de recherche entre les acteurs industriels et académiques ont été établies. Ainsi, cette thèse a été réalisée en collaboration entre STMicroelectronics, l’IMEP-LAHC, le CEA LETI et l'université d'Udine dans le cadre de plusieurs projets européens et français (Place2Be, Casanova ...). En interne à STMicroelectronics, une forte collaboration est établie avec l'équipe de caractérisation physique pour les mesures de contrainte / déformation, avec l'équipe de caractérisation électrique et avec « process integration » pour le développement de 28 et 14 FDSOI technologies.

De manière plus détaillée, dans la première partie du chapitre 1, les principaux modèles mis en œuvre dans l'état de l’art des simulateurs ont été examinés. En premier lieu, une description des méthodes utilisées pour calculer les bandes de conduction et de valence du silicium, du germanium et de l’alliage silicium-germanium a été réalisée, mettant en évidence comment le stress et le confinement sont pris en compte. Dans la deuxième partie, une stratégie multi-échelles pour la modélisation du dispositif MOSFET allant de modèles de type “drift diffusion” classiques jusqu’aux calculs NEGF est présenté. Dans la dernière partie, les modèles pour les principaux mécanismes de diffusion dans les solveurs semi-classiques tels que MSMC ou KG sont examiné. Les hypothèses et la gamme de validité de ces modèles ont également été mises en évidence, et les développements des solveurs internes à STMicroelectronics KG sont discutés.

Le chapitre 2 traite de la comparaison des différentes approches actuellement disponibles pour modéliser le transport à faible champ dans les transistors avancés de type FDSOI. Les mobilités des électrons et des trous ont été calculées en utilisant quatre solveurs différents: le solveur interne à STMicroelectonics (UTOXPP), le solveur commercial SBAND de Synopsys, le solveur MSMC de l'Université d'Udine et TB_SIM et le solveur NEGF du CEA (certains résultats sont présentés en figure III et IV). Les simulations sont ensuite comparées aux mesures de mobilité split-CV effectuées sur l'état des dispositifs de l'art FDSOI. L'utilisation d'une large gamme de mesures split-CV, l'impact de l’épaisseur équivalente d’oxyde (EOT), la tension face arrière et la température ont été étudiés, ce qui conduit à une vaste comparaison entre l'état des modèles d'art et des expériences (figure V).

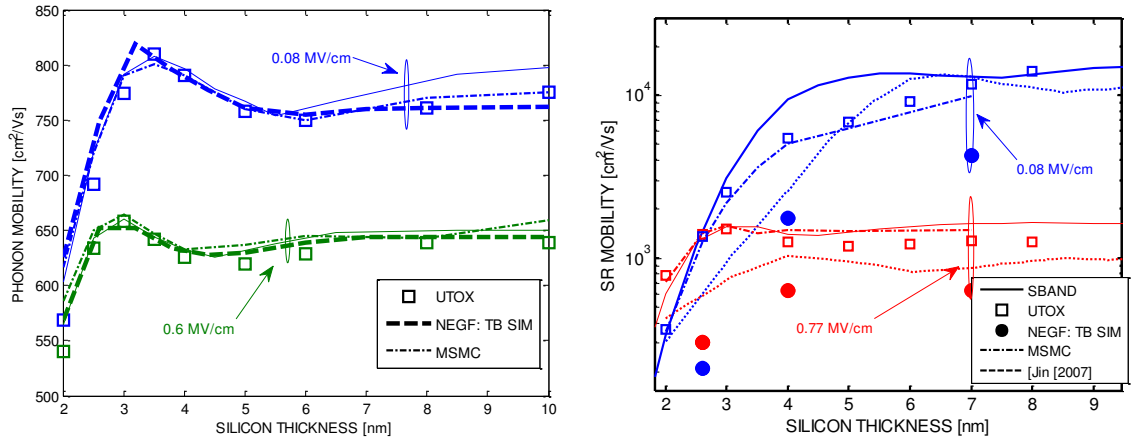

Figure III: Modélisation de la mobilité limitée par les phonons et la rugosité de surface en fonction de l'épaisseur du film. Comparaison entre les différents solveurs (SBAND, UTOX, MSMC, NEGF).

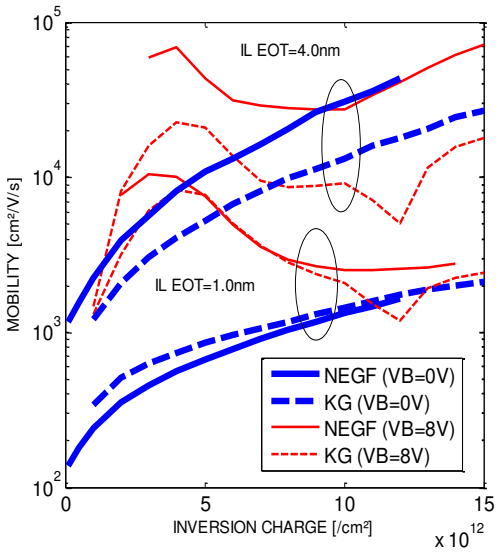

Figure IV: Modélisation de la mobilité limitée par le mécanisme de « remote Coulomb » en fonction de l'épaisseur du film. Comparaison entre les différents solveurs (SBAND, UTOX, MSMC, NEGF).

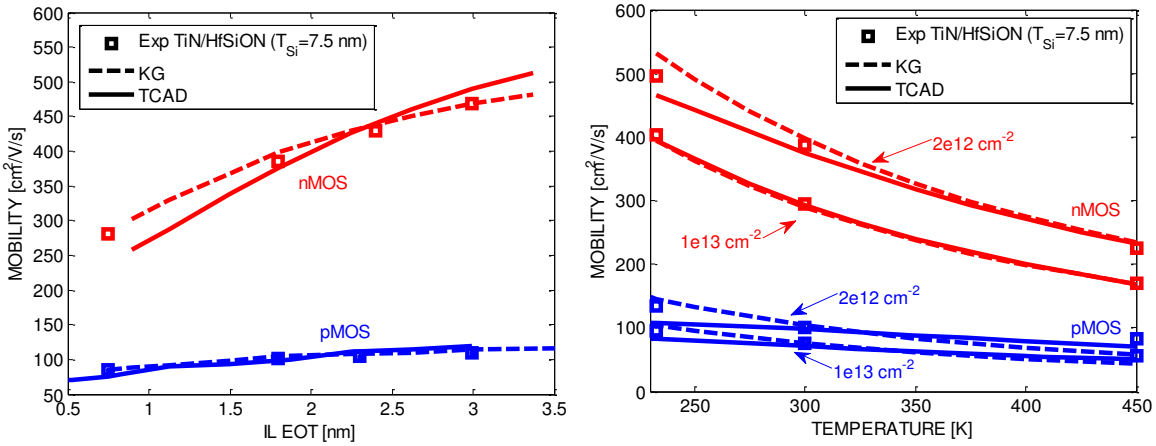

Figure V: Mobilité n- and pMOS simulé en TCAD et avec un solveur de type KG à charge d'inversion constant en fonction de a) l'EOT b) la température.

Le chapitre 3 vise à décrire les méthodes utilisées au cours de cette thèse pour modéliser les contraintes induites par le procédé de fabrication. Les simulations ont été comparées à des mesures de « nano-beam difraction » (NBD). Le deuxième objectif est d'analyser et de calibrer (sur solveurs de transport avancés) les modèles TCAD disponibles pour rendre compte efficacement de l'influence du stress sur la mobilité (jusqu'à 2GPa- figure VI). Enfin, dans ce chapitre, une méthodologie complète pour les simulations de stress induit par les processus et son impact sur les caractéristiques électriques a été mise en place. Cela permet à des simulations TCAD précises et efficaces tendues-Si FDSOI MOSFET à l'état de la technologie CMOS de l'art.

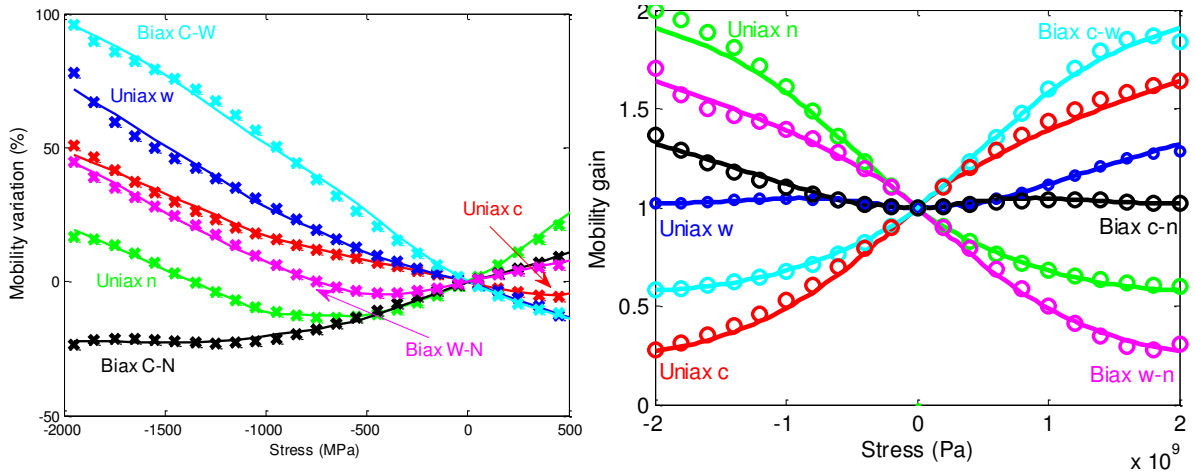

Figure VI: Variation de la mobilité es trous en fonction du stress. Canaux <100> (a) and <110> (b).

Le chapitre 4 présente les applications des méthodes présentées précédemment pour modéliser des dispositifs CMOS avancés. Des simulations mécaniques ont été réalisées pour modéliser le profil de stress dans les transistors 14FDSOI, en mettant l'accent sur la modélisation de la relaxation de la contrainte pendant l'étape STI (figure VII) et l'effet des source et drain SiGe. Des solutions pour optimiser la configuration de stress dans sSOI et dispositifs à base de SiGe-ont été présentés. Ces solutions reposent sur l'utilisation d'un motif STI directionnel pour différencier la direction de la longueur et celle de la largeur (figure VIII). Ainsi, le stress dans ces deux directions peut être contrôlé de façon indépendante en adaptant les étapes du processus selon les propositions développées dans le chapitre III.

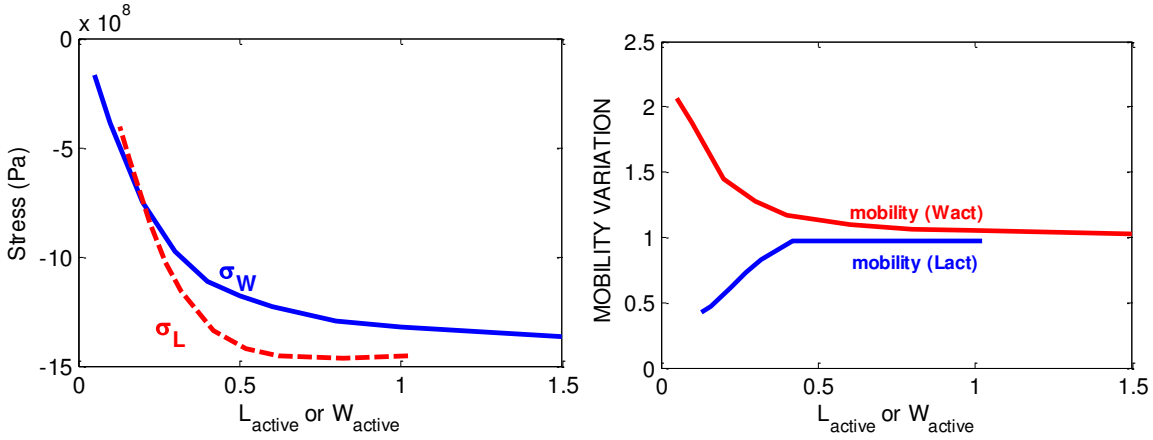

Figure VII: Modélisation de la a) contrainte moyenne dans le canal b) et de la mobilité en function des dimensions du transistor.

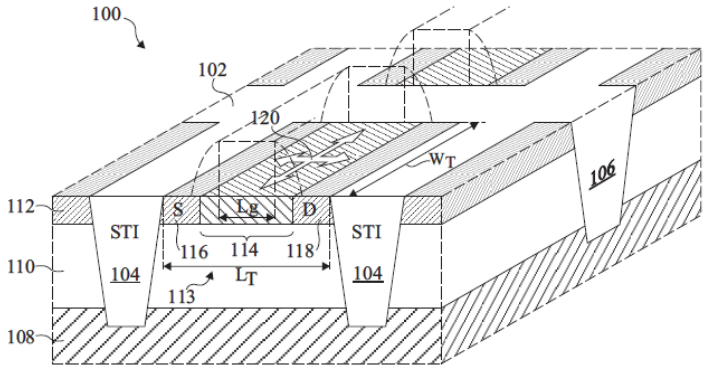

Figure VIII: Schéma 3D du transistor FDSOI.