Ultrasonic Generator for Surgical Applications and Non-invasive Cancer Treatment by High Intensity Focused Ultrasound

Xusheng Wang

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Par

Monsieur Xusheng WANG

Ultrasonic Generator for Surgical Applications and Non-invasive Cancer Treatment by High Intensity Focused Ultrasound

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Composition du Jury :

Madame, DESGREYS, Patricia	Professeur	ENST	Président
Monsieur, SOBOT, Robert	Professeur	ENSEA	Rapporteur
Monsieur, HEBRARD, Luc	Professeur	Université de Strasbourg	Rapporteur
Monsieur, MAUDUIT, Nicolas	Docteur	Société Vision Intégré	Examinateur
Madame, ZHANG, Ming	MCF (HDR)	Université Paris-Sud	Directeur de thèse

ABSTRACT

High intensity focused ultrasound (HIFU) technology is now broadly used for cancer treatment, because of its non-invasiveproperty. In a HIFU system, a phased array of ultrasonic transducers is utilized to generate a focused beam of ultrasound (1M~10MHz) into a small area of the cancer target locations within the body. Most HIFU system are guided by magnetic resonance imaging (MRI) in nowadays. In this paper, a half-bridge class D power amplifier and an automatic impedance tuning system are proposed. Both the class D power amplifier and the auto-tuning system are compatible with MRI system. The proposed power amplifier is manufactured by using of printed circuit board (PCB) and discrete components. According to the test results, the proposed power amplifier has a power efficiency of 82% with 3 W output power at 1.25 MHz working frequency. The automatic impedance tuning system proposed in this paper is designed in two versions: a PCB and an integrated circuit version. Unlike the typical auto-impedance tuning networks, it is no need of microprogrammed control unit (MCU) or computer in the proposed design. Besides, without using bulky magnetic components, this auto-tuning system is compatible with MRI equipment. The PCB version is designed to verify the principle of the proposed automatic impedance tuning system, and it is also used to help the design of the integrated circuit. The surface area of the PCB auto-tuning system is 110cm^2. The test results confirmed the expected performance. The proposed auto-tuning system can perfectly cancel the imaginary impedance of the transducer, and it can also compensate the impedance drifting caused by unavoidable variations (temperature variation, technical dispersion, etc.). The integrated auto-tuning system is realized by using CMOS process (C35B4C3) provided by Austrian Micro Systems (AMS). The die area of the integrated circuit is only 0.42 mm^2. This design provides a wide operation frequency range with a very low power consumption (137 mW). The power efficiency improved by using this auto-tuning circuit is 20% compared with the static tuning network.

Keywords: Ultrasonic transducer; HIFU; Automatic impedance tuning; Switched capacitor; Ultrasonic power supply; Half-bridgeClass D amplifier.

Résumé

La technique de haute intensité ultrasons focalisés (HIFU) est maintenant largement utilisée pour le traitement du cancer, grâce à son avantage non-invasif. Dans un système de HIFU, une matrice de transducteurs à ultrasons est pilotée en phase pour produire un faisceau focalisé d'ultrasons (1M ~ 10 MHz) dans une petite zone de l'emplacement de la cible sur le cancer dans le corps. La plupart des systèmes HIFU sont guidées par imagerie par résonance magnétique (IRM) actuellement. Dans cette étude de doctorat, un amplificateur de puissance de classe D en demi-pont et un système d'accord automatique d'impédance sont proposés. Tous deux circuits proposés sont compatibles avec le système IRM. L'amplificateur de puissance proposé a été réalisé par un circuit imprimé (PCB) avec des composants discrets. Le diagramme de l'amplificateur de puissance proposé est montré dans la Figure 1.

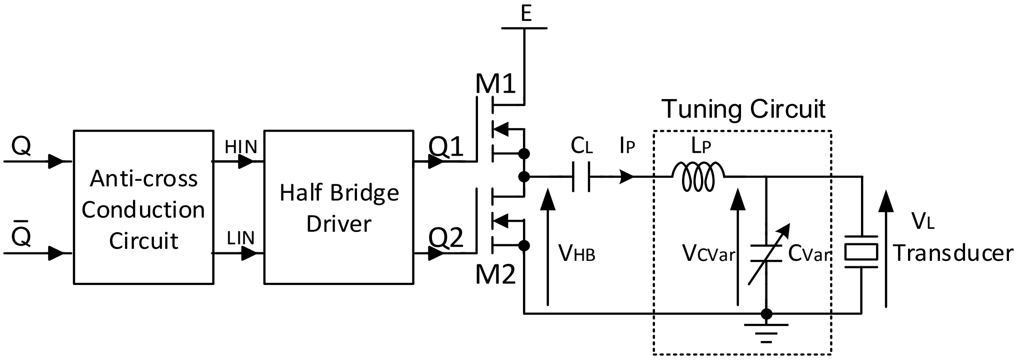

Fig.1 Le diagramme de la class D amplificateur de puissance en demi-pont proposé.

La Figure 2 montre un prototype de l'amplificateur de puissance proposée. L'amplificateur de puissance est situé dans la zone délimitée par la ligne en pointillé.

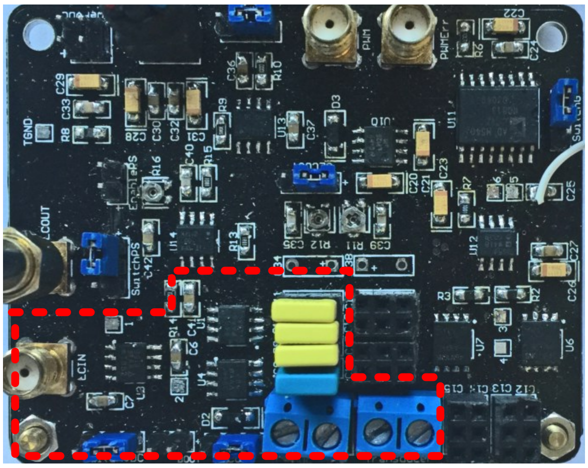

Fig.2 Prototype de l'amplificateur de puissance classe D proposée.

Les chronogrammes de sortie de demi-pont V_{HB} et sortie de l'amplificateur de puissance V_{OUT} sont démontrés dans la Figure 3.

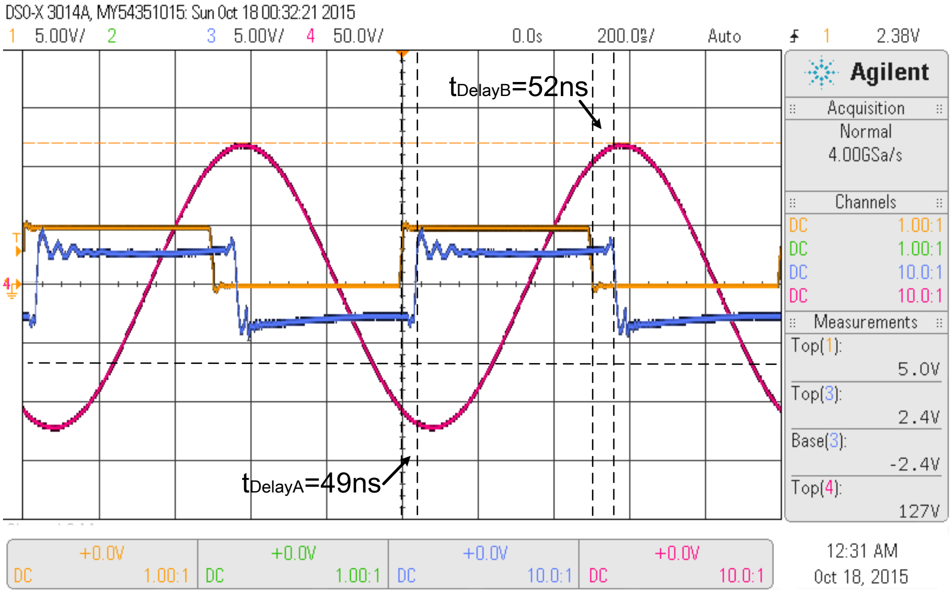

Fig.3 Chronogrammes de sortie de demi-pont V_{HB} et sortie de l'amplificateur de puissance avec 1.25 MHz, 5V de signal d'entrée.

Ch1 (*orange*): Tension du signal d'entrée du circuit de demi-pont V_{IN}: 5V/div.

Ch3 (*bleu*): Tension du signal de sortie du circuit en demi-pont V_{HB}: 10V/div.

Ch4 (*Rose*): Tension du signal de sortie de l'amplificateur de puissance V_{OUT}: 50V/div.

Les retards entre le d'entrée V_{IN} et V_{OUT} sont 49 ns au bord montant et 52 ns au bord tombant. Le voltage maximum de V_{OUT} est 127 V. L'efficacité de puissanc mesurée de l'amplificateur proposé est décrite par,

$$\eta_{Eff} = \frac{P_{OUT}}{P_{IN}} = \frac{P_{Piez}}{P_{IN}} = \frac{P_{Piez}}{V_{DC} \cdot I_{DC}} = \frac{3W}{5V \times 726mA} \simeq 82.6\% \qquad (1)$$

Selon les résultats du test, il a rendement de conversion en puissance de 82%, quand le circuit est bien accordé, pour une puissance de sortie conçue de 1.25W avec une fréquence de travail de 3MHz.

Le système d'accord automatique d'impédance proposé a été conçu en deux versions: une version en PCB et une version en circuit intégré (IC). Contrairement aux systèmes d'accord automatique proposés dans la littérature, il n'y a pas besoin de l'unité de microcontrôleur (MCU) ou de l'ordinateur dans la conception proposée. D'ailleurs, sans l'aide de composants magnétiques volumineux, ce système d'auto-réglage est entièrement compatible avec l'équipement IRM.

Le schéma de principe de systèmes d'accord automatique, qui est basé sur le condensateur commute synchrone, est représenté dans la Figure 4. La variation de capacité est obtenue en faisant varier le rapport cyclique de conduction d’un interrupteur bidirectionnel (AC switch) en respectant les conditions de synchronisation indiquées dans les chronogrammes représentés Figure 5.

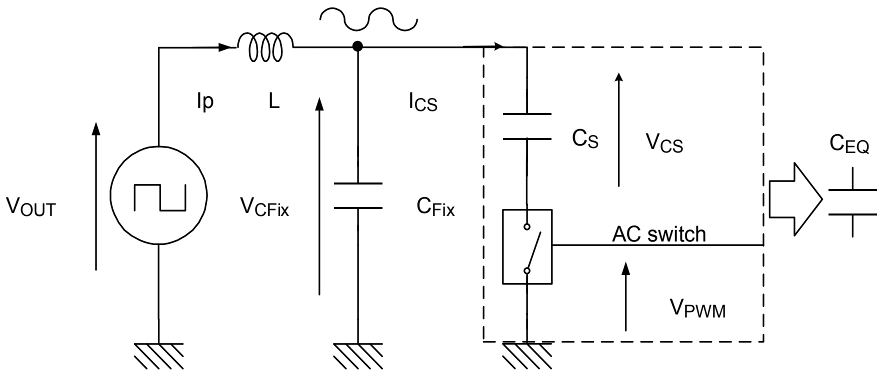

Fig.4 Schéma de principe de systèmes d'accord automatique, qui est basé sur le capacité commute synchrone.

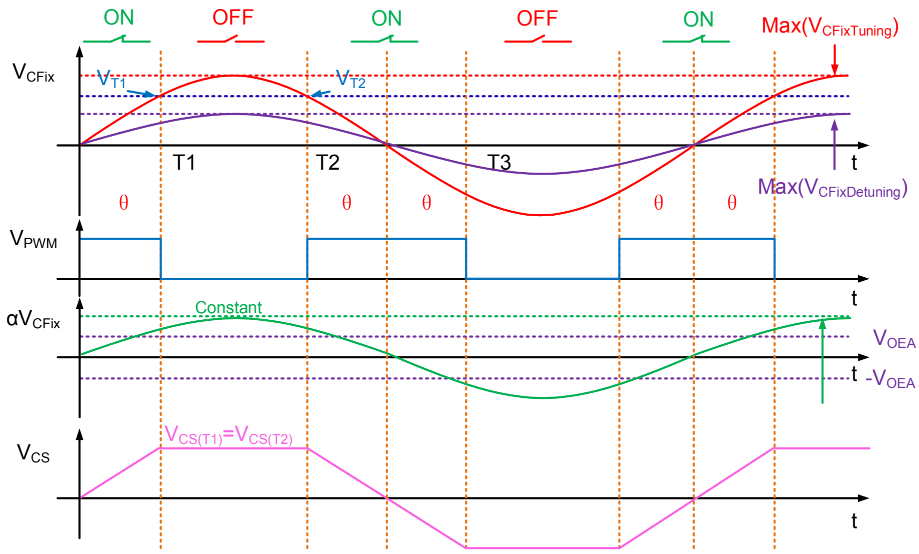

Fig.5 Formes d'ondes théoriques du systèmes d'accord automatique basé sur le capacité commute synchrone

Si ces conditions sont respectées, on montre alors que la fonction de transfert de la capacité commutée s'écrit :

$$C_{EQ} = C_S \cdot sin[\frac{\pi V_{OEA}}{2Max(V_{Trig})}] \tag{2}$$

Avec V_{OEA} = tension de commande, αV_{CFix} = amplitude de le signal utilisée pour générer la commande PWM. Pour garantir la stabilité du système, αV_{CFix} est un signal sinusoïdal avec l'ampleur constant. Il a aussi la même phase et la fréquence que le signal de sortie de l'amplificateur de puissance. En portant ce résultat dans l'expression (2), on obtient finalement une fonction de transfert linéaire de la forme:

$$C_{EQ} = C_S \, V_{OEA}/[\alpha Max(V_{CFix})] \tag{3}$$

Contrairement à la solution traditionnel, cette méthode de linéarisation a permis de réaliser un système d'accord automatique relativement simple et performant.

Le schéma de système à condensateur commuté synchrone pour l'exécution de l'auto tuning est illustré dans la Figure 6. Le système de syntonisation automatique à l'aide d'un condensateur commuté synchrone est délimité par le polygone de vert. Afin de faciliter son analyse, l'auto-réglage system a été partitionné en pointillés. Comme il peut être vu de cette figure, l'auto-réglage système proposé dans ce document se compose de cinq blocs fonctionnels: Bloc de réglage, bloc de commande automatique de gain, bloc de détection d'erreur de phase, bloc de génération d'un signal d'interrupteur et bloc de commutateur AC.

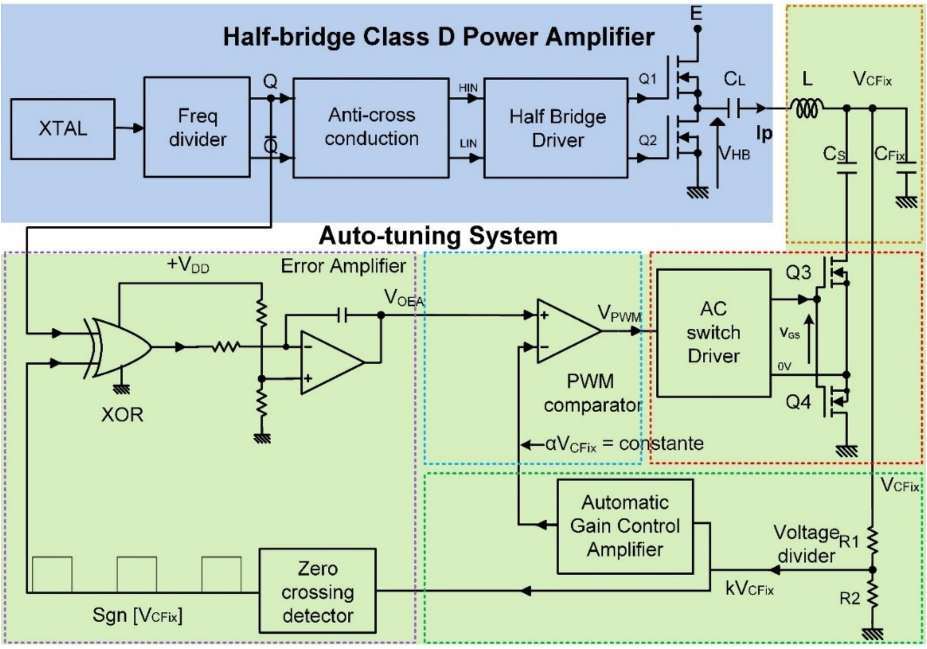

Fig.6 Diagramme de la réalisation d'auto-réglage system basé sur condensateur commuté synchrone.

La version en PCB a été conçue pour vérifier le principe du système proposé, et il est également utilisé pour guider à la conception du circuit intégré. La réalisation en PCB occupe une surface de 110cm^2. Le prototype de l'auto-réglage system est illustré dans la Figure 7.

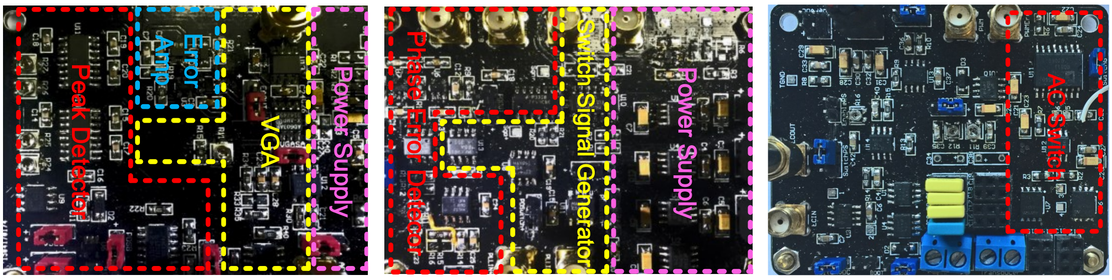

Fig.7 Prototype de l'auto-réglage system en circuit électrique imprimé.

Le circuit équivalent du circuit de test est illustré dans la Figure 8. On utilise un condensateur d'erreur C_{Error} (15%C_S), qui est contrôlé par un signal à onde carrée de 5 kHz, pour simuler le plus mauvais état d'impédance le drift.

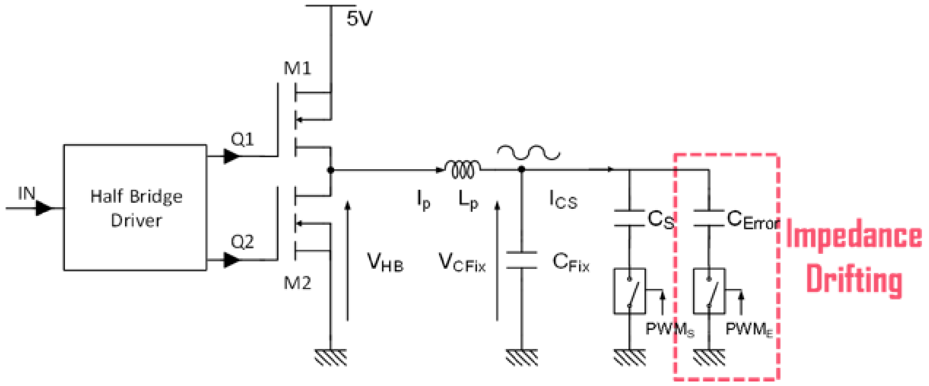

Fig.8 Essai équivalent circuit du générateur d'ultrasons avec l'auto-réglage circuit en circuit électrique imprimé.

Les résultats des tests du générateur d'ultrasons avec le carte du circuit d' auto-réglage est illustré dans la Figure 9.

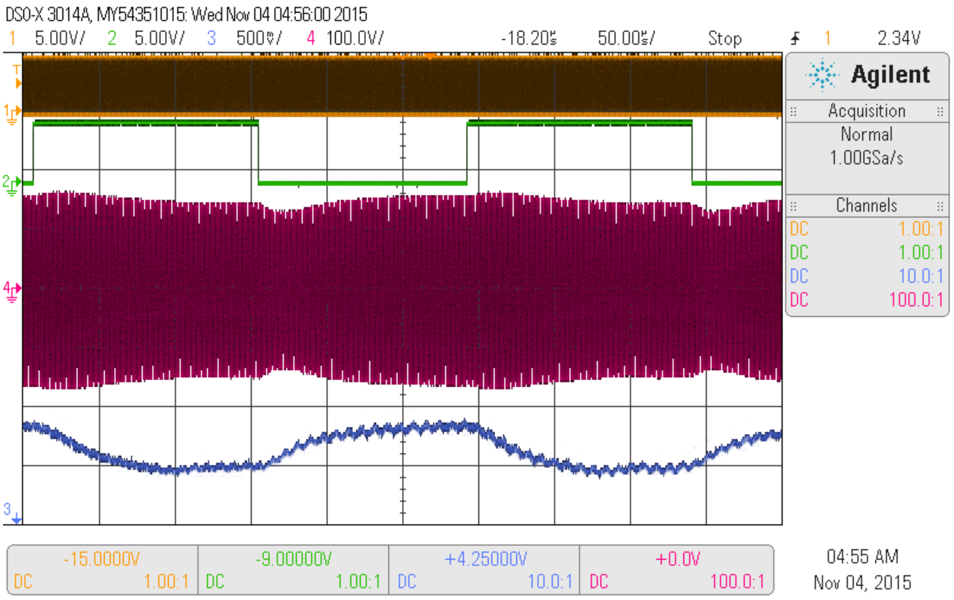

Fig.9 Les résultats des tests du générateur d'ultrasons avec l'auto-réglage circuit en circuit électrique imprimé.

Ch1 (*orange*): Signal de sortie du circuit en demi-pont V_{HB}: 5V/div.

Ch2 (*vert*): Erreur signal de commande du condensateur PWM_E: 5V/div.

Ch3 (*bleu*): Erreur de phase de tension V_{OEA} générée par le bloc deteciotn: 500mV/div.

Ch4 (*rose*): Signal de sortie de l'amplificateur de puissance V_{CFix}: 100V/div.

Les résultats des tests ont confirmé la performance attendue. Le système d'auto-réglage proposé peut parfaitement annuler l'impédance imaginaire du transducteur, et il peut également compenser l'impédance de la dérive causée par les variations inévitables (variation de température, dispersion technique, etc.).

La conception du système d'auto-réglage en circuit intégré a été réalisé avec une technologie CMOS (C35B4C3) fournies par Austrian Micro Systems (AMS). La surface occupée par le circuit intégré est seulement de 0,42mm^2. Le post-layout de l'auto-réglage system en circuit intégré est illustré dans la Figure 10.

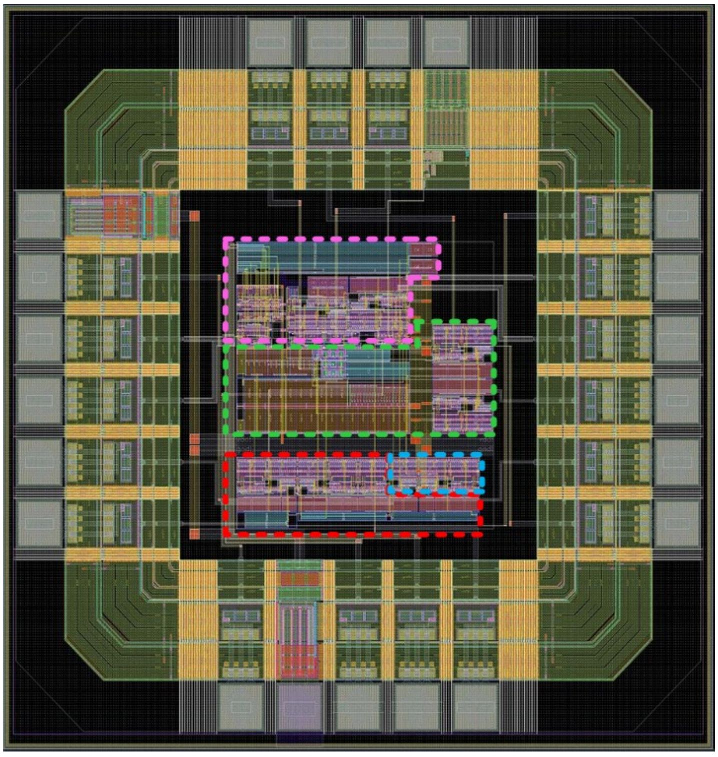

Fig.10 Post-layout de l'auto-réglage system en circuit intégré.

Le circuit équivalent du circuit de test est illustré dans la Figure 11. On utilise un condensateur d'erreur C_{Error} (15%C_S), qui est contrôlé par un signal à onde carrée de 16.7 kHz, pour simuler le plus mauvais état d'impédance le drift. Pour la version d'IC, pour simplifier et accélérer la simulation de l'ensemble du système, nous avons utilisé un amplificateur de puissance équivalente et circuit de l'interrupteur de AC au lieu de la vraie.

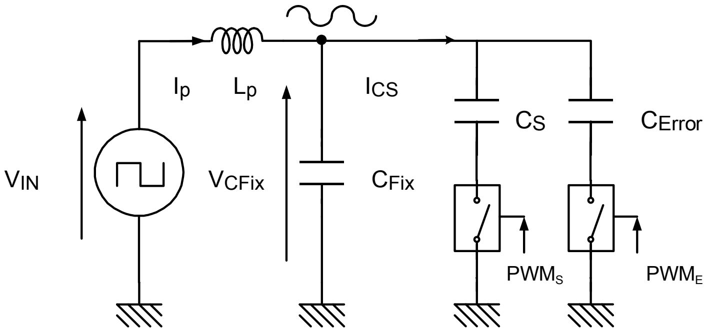

Fig.11 Essai équivalent circuit du générateur d'ultrasons avec l'auto-réglage circuit en circuit intégré.

Les résultats des tests du générateur d'ultrasons avec l' auto-réglage circuit en circuit intégré est illustré dans la Figure 12.

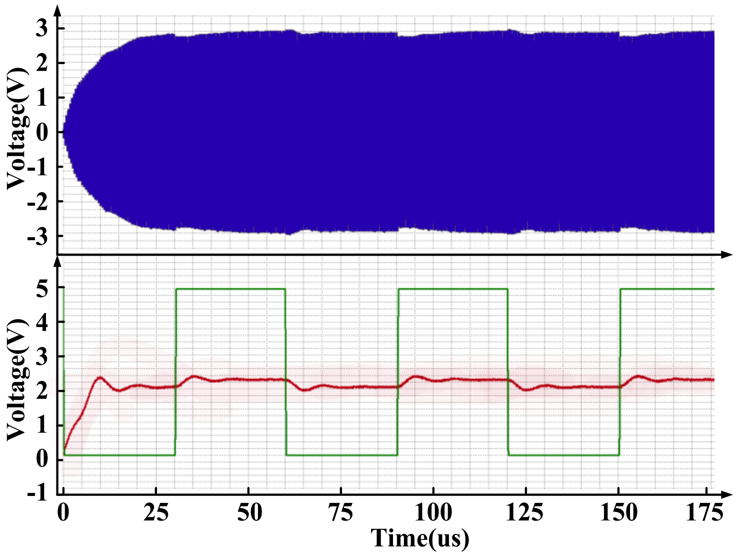

Fig.12 Résultats de simulation de l'auto-réglage circuit en circuit intégré.

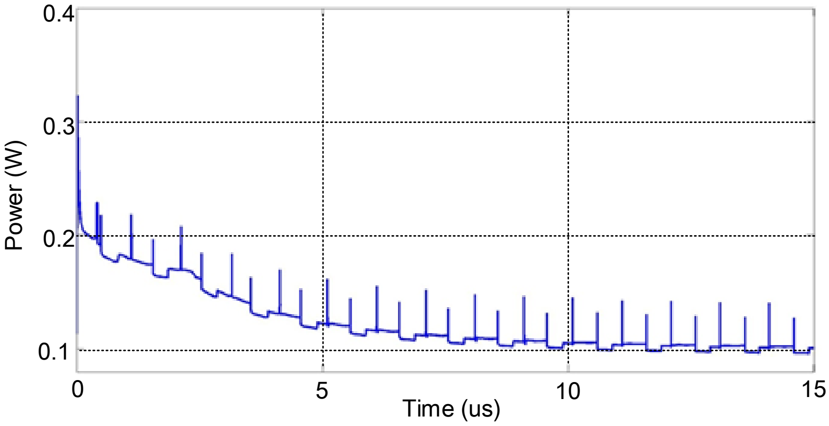

Fig.13 Résultat de la simulation de la consommation électrique.

Figure 13 est le résultat de la simulation de la consommation électrique de l'auto-réglage circuit en circuit intégré. Les économies d'énergie contre les erreurs de phase avec ou sans circuit de réglage automatique est illustré dans la Figure 14.

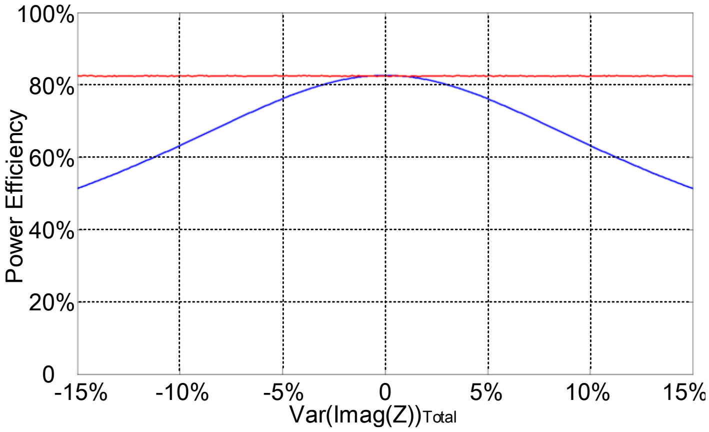

Fig.14 économies d'énergie contre les erreurs de phase avec ou sans circuit de réglage automatique en circuit intégré.

Selon les résultats, le circuit intégré conçu est capable de fonctionner à une large gamme de fréquence tout en conservant une consommation d'énergie très faible (137 mW). D'après les résultats de la simulation, le rendement de puissance de ce circuit peut être amélioré jusqu'à 20% comparant à celui utilisant le réseau d'accord statique.

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Xusheng WANG

Orsay

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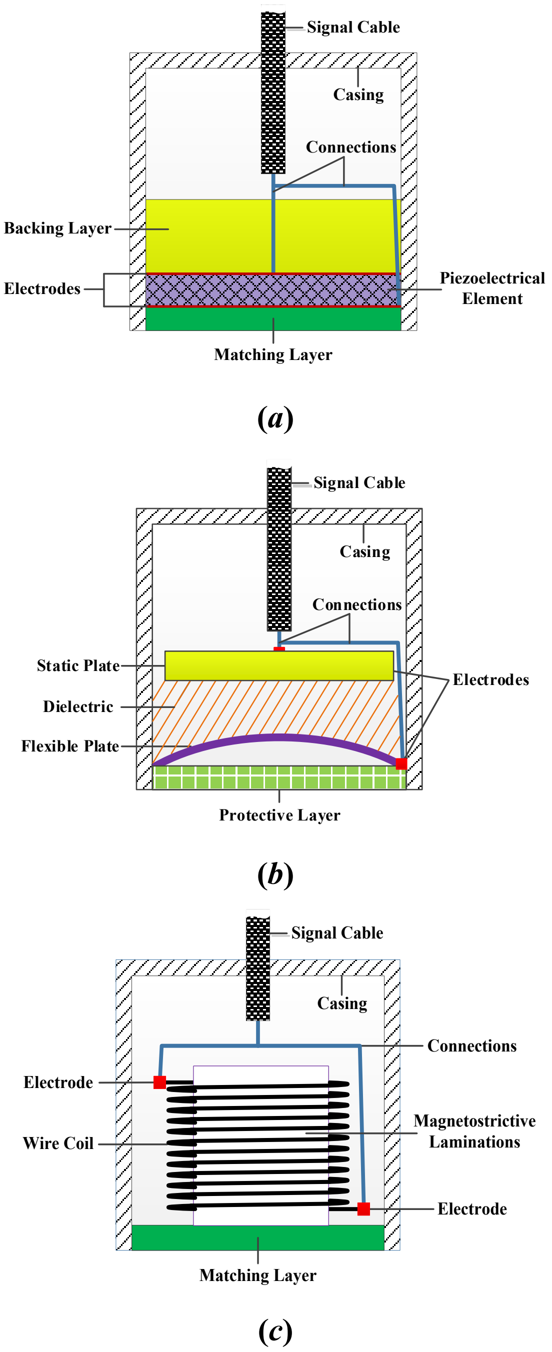
Chapter 1

Introduction

1.1 Background

1.1.1 Ultrasonic Transducer

Ultrasonic transducers play a very important role in the study and application of ultrasonics. The ultrasonic transducer is a kind of transducer that converts electrical signals to ultrasound waves or vice versa [NK2012]. Ultrasonic transducers can be divided into three types based on the method of operation: active transducer, passive transducer, and ultrasonic transceiver. Active transducers can generate ultrasonic sound waves upon the application of an AC voltage. Passive transducers comprise an ultrasound microphone that can detect ultrasound signals and transform them to electrical signals. Ultrasonic transceivers can not only generate but also receive ultrasound signals [SN1993]. There are several types of ultrasonic transducers. These are piezoelectric transducers, capacitive transducers, and magnetostrictive transducers [JMG2005]. Piezoelectric transducers are made of piezoelectric crystals that can change size and shape when an AC voltage is applied. The electrical signals cause the crystals to oscillate at a specific frequency and produce an ultrasound [NK2012, JMG2005]. Capacitive transducers use variable electrostatic fields between a conductive diaphragm and a backing plate. The varying electrostatic field can cause the conductive diaphragm to vibrate. When the electrostatic field changes at high frequencies, the vibration of the conductive diaphragm will generate an ultrasound [JMG2005]. Magnetostrictive transducers utilize the principle that iron-rich metals (iron, nickel, or Terfenol-D) expand and contract when placed in a changing magnetic field [JMG2005, MOE2013]. Diagrams of these three different types of ultrasonic transducers are shown in Figure 1.1.



(a)

(b)

(c)

Fig.1.1 Diagrams of piezoelectric transducer (*a*), capacitive transducer (*b*) and magnetostrictive transducer (*c*).

Currently, piezoelectric transducers are more widely used than the other two types of transducers. The advantages [BK2007] of the piezoelectric transducer are as follows:

1. It can reach power efficiencies as high as 80%.
2. It is easily fabricated into different shapes (e.g., round, ring, and rectangle)
3. It has a stable performance and is very cheap for large-scale applications.

The ultrasonic transducers that were studied and used in this paper are piezoelectric transducers.

1.1.2 Ultrasonic Power Supply

An ultrasonic power supply, or ultrasonic generator, is a device that can provide a suitable power supply for ultrasonic transducers [DS2011]. Generally, an ultrasonic power supply consists of three parts: a signal generator, power amplifier, and an impedance-tuning network. The signal generator is used to produce a signal with a specific frequency which is equal to the working frequency of the transducer. Then this signal is amplified by the power amplifier. And the amplified signal is applied to the ultrasonic transducer, which is well matched by the impedance tuning network. The signal used in an ultrasonic power supply is usually a sinusoidal or a pulse signal.

Currently, there exist two types of ultrasonic power supply, namely separate excitation and self-excitation [YY2014]. The difference between these two types of power supply is capability of frequency tracking. The separate-excitation ultrasonic power supply is composed of an oscillator circuit and a power amplifier [YY2014, HE2013], while the self-excitation ultrasonic power supply consists of an oscillator circuit, a power amplifier, a frequency-tracking circuit, and a power-control circuit. The transducer can reach its highest efficiency in its resonant state. However, unavoidable variations (temperature drifting, load variation, etc.) change the resonance frequency of the transducer. The frequency-tracking circuit is used to guarantee that the transducer is functioning at resonance. Moreover, the power-control circuit is applied to stabilize the output power of the transducer [HE2013].

The development of a power amplifier, which is used in ultrasonic generators, has gone through two phases: analog power amplifier and switched power amplifier.

Analog amplifiers, such as class A, class B, and class AB amplifiers, are all suitable for ultrasonic power supplies. However, several disadvantages limit their usage [RJW2014]:

1. Low power efficiency: The maximum theoretical efficiencies of class A, B, and AB amplifiers are 50%, 78.5%, and 78.5%, respectively.
2. High working temperature: There must be a cooling facility for the amplifier.
3. Hard to control: Because they are all analog amplifiers, it is difficult to control the output power and frequency.

Switched-mode amplifiers, such as class D, class E, and class DE amplifiers, are also suitable for transducers. The efficiencies of switched-mode amplifiers are all higher than those of analog amplifiers. The theoretical efficiencies of class D, E, and DE amplifiers are all 100%. Besides, the output power of switched amplifiers can be controlled very easily [BB2006]. The topologies of analog amplifiers and switched amplifiers will be discussed in chapter 3.

1.1.3 Impedance-tuning Network for Transducers

Impedance-tuning networks are required in ultrasonic applications because the output impedance of an ultrasonic power supply and the characteristic impedance of parallel coaxial lines are all pure resistive. Further, ultrasonic transducers are usually reactive components [GRM2010]. If a transducer is driven directly by ultrasonic power, there will be a reflected power that will cause an increase in the temperature of the transducer. When the temperature exceeds a certain value, the transducer will encounter unrecoverable damage. Therefore, in an ultrasonic power supply, the impedance-tuning network should be properly designed to resolve the mismatch between the power supply and transducer.

Two main kinds of impedance-tuning techniques are used for ultrasonic transducers, namely static tuning and dynamic tuning. The static impedance-tuning technique uses a vector network analyzer to measure the impedance value of the transducer. Then, based on the impedance characteristic of the transducer, the parameters of the components used in the static-tuning network are selected based on the measured impedance [HH2011]. These parameters will remain constant during its operation. The static impedance-tuning network can be subdivided into three types based on the form: inductor-tuning network, capacitor-tuning network and inductor-capacitor tuning network. The static-tuning method has a very simple structure and is very easy to implement. However, this method cannot compensate for the impedance and resonance-frequency drifting of the transducer during operation. These unavoidable fluctuations will lead to an impedance mismatch, which can result in an increase in the temperature and damage to the transducer. In addition, the parameters of the tuning network are calculated based on the approximate model of the transducer. Therefore, these calculated parameters may deviate far from the theoretical value. To adjust the tuning parameters, the dynamic impedance-tuning network uses a feedback signal, which is generated by an impedance-detector circuit [MGJF2012, DDR1998]. In this way, the transducer can always work under its resonance state.

The topologies of impedance-tuning networks for transducers will be discussed in chapter 2.

1.1.4 History of HIFU

The use of high-intensity focused ultrasound (HIFU) technology as a therapeutic modality can be traced back to the 1920s. Robert Woods and Alfred Lee Loomis found that high-power ultrasound beams have the capability of killing cells and tiny fish [WRW1927]. In 1942, John Lynn discovered that focused ultrasound can result in localized tissue damage [LJG1942]. In the late 1950s, the Francis Fry group commenced research into the use of HIFUs on animals and humans [FWJ1953, FWJ1955]. During the 1950s and 1960s, the number of experiments showed significant promise with respect to HIFU technology. It was used to treat patients having Parkinson's disease in combination with craniotomy and local anesthesia [MR1959, BJW1956]. However, the long treatment times and the absence of a high-precision imaging technique HIFU was instead used based on neurological medicinal treatments during the 1970s [ZYF2011]. In this period, HIFU technology has started to ebb.

During the 1980s and 1990s, with the development of medical imaging technology, HIFU underwent a period of rapid development. The high-resolution medical imaging and monitoring technique, which improved the identification and visualization of internal tissue, gave the HIFU larger development space. The technique used for the production of ultrasound transducers also simultaneously underwent significant improvements. This improvement enabled the development of more powerful and smaller HIFU systems. Then, in the late 1990’s the phased-array technique was first applied for use in HIFU technology [EES1991, USI1989]. Using a suitable control system, this phased-array HIFU (pHIFU) can generate more than one focal point, and the location of the focus can be easily controlled [EES1989-CE2009]. During this period, HIFU was used in many human trials for the treatment of diseases and disorders including uterine fibroids, essential tremors, and cancers of the bladder, kidney, liver, brain, pancreas, and breast [HK2007-QB2010]. These treatment attempts have met with various degrees of success, and the FDA has approved HIFU for the treatment of prostate cancer [HGR2009].

Fig.1.2 Pictures of a real USgFUS (*Left*) and MRgFUS (*Right*).

Nowadays, two types of imaging techniques are used to guide HIFU operations, namely diagnostic ultrasound and magnetic resonance imaging (MRI). The diagnostic ultrasound technique uses the high frequency sound waves that travel from the ultrasound probe through human tissue. Some of the sound waves bounce back to the transducer. This reflected sound is used by a computer to form the ultrasound image. And MRI is one of the newest and most technically elegant examinations ordered. The scan relies on the use of a large magnet and radio transmitters and receiver to visualize the atoms of the body. Ultrasound-guided focused ultrasound (USgFUS) was the most popular method for HIFU operation. The photo of a real USgFUS is shown in Figure 1.2 (*left*). It can provide anatomical imaging during surgery, and can offer a rough figure of temperature. And the using of diagnostic ultrasound makes the system very cheap and easy to realize. However, the motion of the tissue that is illustrated by diagnostic ultrasounds is degraded, and because of interference between the diagnostic system and HIFU, the real image of the tissue component is covered by fog artifacts [BJ2004-LD2008]. This leads to a negative effect on the safety and effectiveness of HIFU therapy. Currently, the most innovative area of HIFU research is MRI-guided focused ultrasound (MRgFUS). The picture of an MRgFUS is shown in Figure 1.2 (*Right*). MRI systems can offer excellent soft-tissue contrast, 3D imaging capabilities, and real-time temperature measurement [CHE1995].

1.2 Motivation and Objective

In a HIFU system, the designed transducer array is utilized to focus a beam of ultrasound (1 MHz ~ 10 MHz) energy into human organs with small tissue volumes, such as the breast, kidney, and liver. The focused beam causes localized high temperatures (45 ~ 90°C) in a small region, which will ablate the target tissues without the need for an incision [ZYF2011].

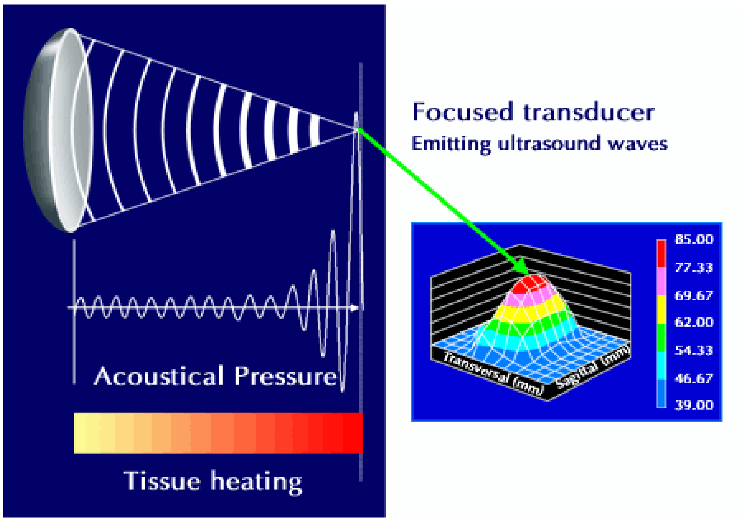


Fig.1.3 The temperature characteristics and pressure sound wave of HIFU.

The temperature characteristics and pressure sound wave of a HIFU system are illustrated in Figure 1.3. The focused zones usually have a width of 1 – 3 mm, length of 8 – 10 mm, and height of 1 – 3 mm [DTJ2008].

Ultrasonic power generators are the most important components in a HIFU system. Power generators should have the capability to generate enough power for the transducers. In this case, the energy at the focal point can kill the target cancer in a very short time without causing damage to the transducer for long-term treatment. Moreover, sophisticated multi-element ultrasound transducer arrays usually have over a hundred elements, and the size of the ultrasonic generator should be considered. Therefore, the design of ultrasonic power generators for HIFU systems has become a very interesting area of study.

The objective of this thesis is to design a power amplifier and a novel automatic impedance tuning network for transducers in MRgFUS. The main challenges of this thesis are as follows:

1. The size of the power amplifier and the automatic impedance tuning network should be as small as possible.
2. MRgFUS is an MRI-guided HIFU. Therefore, the use of large magnetic components, such as a ferromagnetic-core or iron-core inductors and transformers, should be eliminated in both the power amplifier and the

impedance-tuning network.

3. To avoid overheating, the amplifier must have a very high efficiency, and the automatic impedance-tuning network should have a high accuracy.
4. The power that is required by the transducer is 3 W, and the peak-to-peak voltage of the power supply is required to be about 260 V.
5. The resettling time of the automatic impedance-tuning network should be as small as possible to eliminate the reflected power and protect the transducer.

1.3 Outline

This thesis consists of eight chapters:

In chapter 1, we introduce the background, the motivation, and the objective of this thesis. In the first section, we describe the concept of the ultrasound transducer, ultrasonic power supply, and impedance-tuning network. We also present a historical review of HIFU in this section. Then, we present the research purpose and the main goals of this thesis in the second section. Finally, we present the organization of this thesis.

Chapter 2 presents a model of the transducer that we used in our project, and it reviews several existing impedance-tuning techniques. The characterization of the ultrasound transducer and the equivalent circuit are given in the first section, while details regarding several existing impedance-tuning techniques will be introduced in the second section.

In chapter 3, we present an analysis of the topologies of existing power amplifiers that can be used in HIFU applications, and explain the theory and the circuit design of the power amplifier proposed in this thesis. It begins with the principles of five typical power amplifiers. Then, it focuses on the presentation of the published works involving these power amplifiers. Finally, we present a half-bridge class D amplifier with a square-wave input. The simulation and the test results of the power amplifier are also presented in this chapter.

Chapter 4 covers the theory of the automatic impedance-tuning network that was designed in this thesis. In this chapter, we also explain the impact of temperature drifting and technological dispersions on transducer's impedance. The diagram of the proposed realization is also given in this chapter. In this thesis, we present two versions of circuit design: the discrete-component circuit version and the integrated-circuit version. In chapter 5, we focus mainly on the discrete version of the auto-tuning network. Then, in chapter 6, we explain the integrated-circuit design.

Chapter 5 mainly focus on the printed circuit design of the auto-tuning system. The automatic impedance-tuning system proposed in this thesis consists of three parts: an automatic gain amplifier, a phase-error detector, and a pulse-width modulation (PWM) signal generator. Circuit designs of the sub-blocks are presented in the first section. Then test results of the designed circuit are presented in the second section. The stability analysis is also presented in this chapter.

In chapter 6, we present the integrated-circuit design of the auto tuning system. In the first section, we present an integrated automatic gain amplifier that is suitable for our application. Then, we introduce a phase-error detector, which is realized by using integrated circuit. Finally, we present an integrated switched signal generator. The simulation results and the test results of the integrated circuits are also presented in this chapter. At the end of this chapter, the layout design and the post-layout simulation results are given out.

Chapter 7 shows the test and simulation results of the ultrasonic power supply obtained using the different versions of auto-tuning systems presented in this thesis. We also discuss the experimental environment that was used to test or simulate the circuit.

In chapter 8, we conclude this thesis and present a summary of the contributions that were realized from this thesis. Future research goals are also presented in this chapter.

Chapter 2

Transducer Modeling and Tuning

2.1 Introduction

High-power ultrasonic piezoelectric transducers are used in the development of ultrasound generators in HIFU applications. In ultrasonic applications, there usually exist detuning problems. The output impedance of the ultrasonic power supply and the characteristic impedances of parallel coaxial cables are all purely resistive. However, ultrasonic transducers are usually reactive components. Therefore, the design of an ultrasonic power supplies should include an impedance-tuning network to solve these problems.

In this chapter, we describe the modeling of the piezoelectric transducer. We also present the equivalent circuit for the transducer used in our project. Then, after modeling the transducer, we review the impedance-tuning topologies and several existing automatic impedance-tuning theories.

2.2 Modeling of Ultrasonic Transducer

2.2.1 Structure of Ultrasonic Transducer

Figure 2.1 shows a simple structure of the ultrasonic transducer [QZ2014], which has the similar structure as the transducer used in our project. The transducer consists of four parts: piezoelectric active element, transducer casing, backing layer, and coaxial cable. The ultrasound signal is generated by the piezoelectric active element in the transducer. This element is enclosed within a casing. For transducers used in medical applications, the piezoelectric active element is usually made of lead zirconate titanate. Two electrodes are applied to the top and bottom surfaces of the element. Coaxial cable is connected to the electrodes of the piezoelectric element to transmit signals from the power amplifier to the piezoelectric element. The piezoelectric element and the internal connections are protected by the outer case, which can also provide air backing for the piezoelectric element. As opposed to other ultrasonic transducers, the transducers used in the HIFU application have no matching layers in front of the piezoelectric elements.

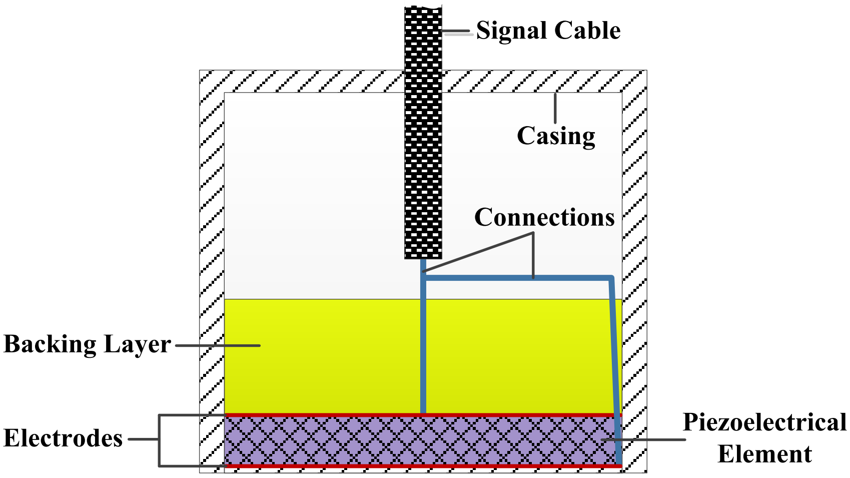


Fig.2.1 Structure of the ultrasonic transducer used in HIFU applications.

A backing layer, which comprises an epoxy loaded with powder, is applied behind the piezoelectric active element. The density and acoustic impedance of the backing layer can be adjusted by using different materials [NVMD2003].

2.2.2 Mathematical Model

Because the most important part of an ultrasonic transducer is the piezoelectric active element, the modeling of ultrasonic transducer can be simplified as a model of a piezoelectric active element. And the piezoelectric element can be considered as an electromechanical vibration system [GM1997]. The well-known equivalent model of a piezoelectric transducer, which is based on its electrical and mechanical characteristics, is depicted in Figure 2.2.

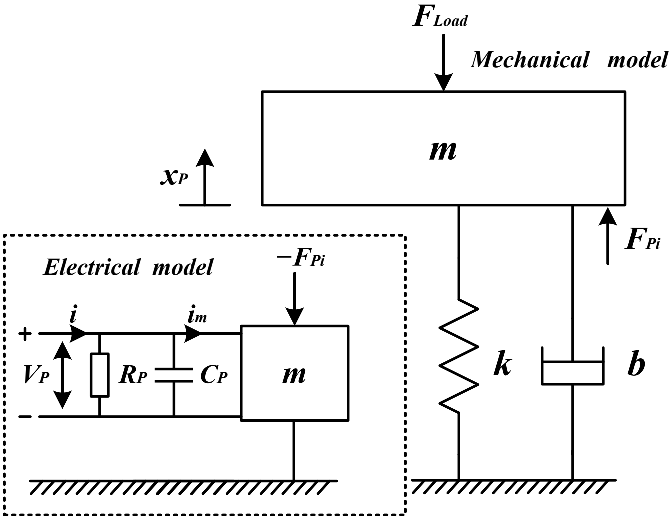


Fig.2.2 Model of the ultrasonic transducer. [GM1997]

As can be seen from this model, the capacitance caused by the piezoelectric material is represented as C_p. In addition, the dielectric losses formed by the oxides are given as R_p. Usually, R_p can be neglected because of its very high value. The equivalent electrical model of the current flows through C_p can be described as

$$C_P \frac{dV_P}{dt} = i - \frac{V_P}{R_P} - i_m \qquad 2.1$$

i is the current generated by the external applied voltage V_P. And i_m is the current flowing through the mass m. The mechanical model of the piezoelectric element is described by,

$$F_{Pi} = V_P \cdot Q_{Force} \qquad 2.2$$

$$i_m = \frac{dx_P}{dt} \cdot Q_{Force} \qquad 2.3$$

$$m\frac{d^2x_P}{dt^2} + b\frac{dx_P}{dt} + kx_P + F_{Pi} = F_{Load} \qquad 2.4$$

where F_{Pi} is the force of the piezoelectric active element excited by the voltage V_P, and the external load is defined as F_{Load}. Q_{Force} is a coefficient to link the applied voltage to the equivalent mechanical force. We can also call it a force factor between the electrical model and the mechanical model. The Simulink model of the piezoelectric active element, which is shown in Figure 2.3, can be obtained from Equations 2.1~2.4.

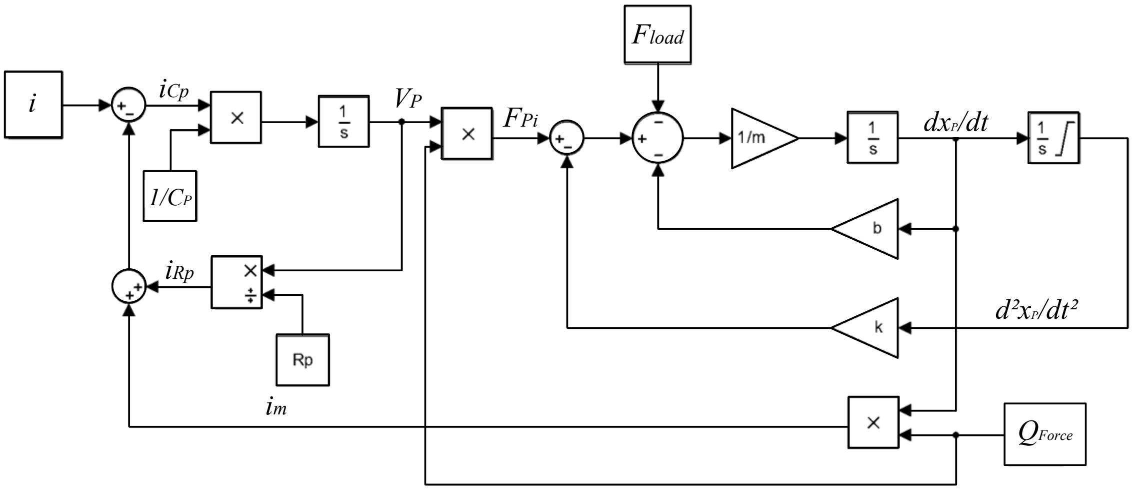


Fig.2.3 Simulink model of the ultrasonic transducer. [SM2008]

In order to realize an equivalent circuit based on the electrical model and mechanical model, the mechanical parameters are transferred to equivalent electrical components. The transformation formulas are tabulated in Table 2.1.

Table 2.1 Transformation formulas for the electrical and mechanical models. [GM1997]

Mechanical Parameters	*Electrical Parameters*	*Relation*
Mass m	*Inductance L_m*	$L_m = m/Q_{Force}^2$
Damping b	*Resistance R_m*	$R_m = b/Q_{Force}^2$
Stiffness k	*Capacitance C_m*	$C_m = Q_{Force}^2/k$
Force F_{Pi}	*Voltage V_P*	$F_{Pi} = Q_{Force} \cdot V_P$
Displacement x_P	*Charge q_m*	$\frac{dq_m}{dt} = i_m = Q_{Force} \cdot \frac{dx_P}{dt}$

Assuming no external load, the model of the piezoelectric element can be replaced by an equivalent circuit, as shown in Figure 2.4.

As can be seen from this figure, the piezoelectric element can be described by two parallel branches of R_P and C_P, and several series resonant branches of L_{mn}, C_{Mn}, and R_{mn}, which represent the mass parts (m) of the model. R_p can be neglected because of its very high resistance.

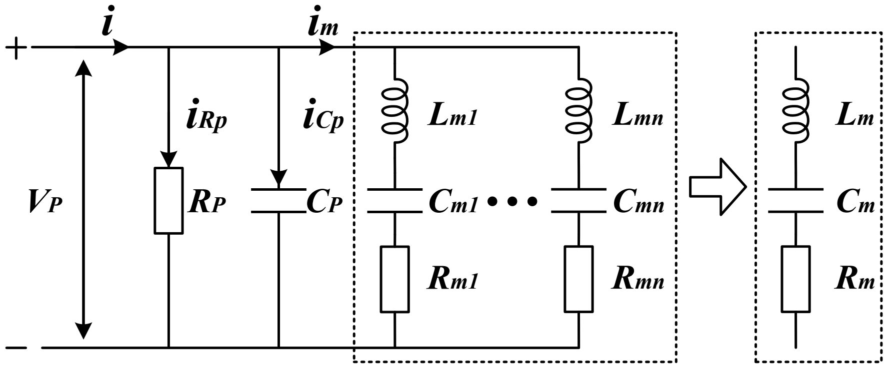


Fig.2.4 Equivalent circuit of the piezoelectric element near its resonance frequency. [VAA2008]

Therefore, the equivalent circuit is described by the following equations:

$$V_P = L_m \frac{d^2 q_m}{dt^2} + R_m \frac{dq_m}{dt} + \frac{q_m}{C_m} \qquad 2.5$$

$$i = C_P \frac{dV_P}{dt} + \frac{dq_m}{dt} + \frac{V_P}{R_P} \qquad 2.6$$

Then, the impedance of the series resonant branches can be obtained by

$$Z_m(jw) = jwL_m + \frac{1}{jwC_m} + R_m \qquad 2.7$$

If the frequency of the driving signal V_P equals the mechanical resonance frequency of the piezoelectric element, the series resonant branches behave as a purely resistive load R_m. The mechanical resonance frequency f_m is calculated by

$$f_m = \frac{1}{2\pi\sqrt{L_m C_m}} \qquad 2.8$$

Thus, the impedance of the equivalent circuit at its mechanical resonance frequency ($Z_m//C_P//R_P$) is described by

$$Z_{Eq}(jw)|_{w=w_m} = \frac{R_m}{1+jw_m C_P \cdot R_m} \qquad 2.9$$

Solving for R_m and C_P,

$$R_m = \frac{\left|Z_{Eq}(jw)|_{w=w_m}\right|^2}{real\left(Z_{Eq}(jw)|_{w=w_m}\right)} \qquad 2.10$$

$$C_P = \frac{-imag\left(Z_{Eq}(jw)|_{w=w_m}\right)}{2\pi f_m \left|Z_{Eq}(jw)|_{w=w_m}\right|^2} \qquad 2.11$$

and the admittance of the equivalent circuit is defined by

$$Y_{Eq}(jw) = jwC_P + \frac{1}{Z_m(jw)} = jwC_P + \frac{1}{jwL_m + \frac{1}{jwC_m} + R_m} \qquad 2.12$$

The admittance at the mechanical resonance frequency can be simplified as,

$$Y_{Eq}(jw)|_{w=w_m} = jw_mC_P + \frac{1}{R_m} \qquad 2.13$$

In order to obtain the general frequency characteristic of the piezoelectric active element, as well as simplify the calculation, we introduce a normalization $\Omega = w/w_m$ into Equation 2.12 as follows.

$$Y_{Eq}(j\Omega) = \frac{\Omega}{\beta\cdot\sqrt{L_m/C_m}} \cdot \frac{(\alpha\beta^2\Omega + j\cdot((\alpha\beta\Omega)^2 + (1-\Omega^2)\cdot(1+\beta-\Omega^2)))}{(\alpha\beta\Omega)^2 + (\Omega^2-1)^2} \qquad 2.14$$

where α and β are defined as the admittance ratio and capacitance ratio, respectively.

$$\alpha = R_mC_Pw_m \qquad 2.15$$

$$\beta = C_m/C_P \qquad 2.16$$

By solving Equation 2.14, the series and parallel resonance frequencies of the equivalent circuit can be obtained as

$$f_s = f_m = \frac{1}{2\pi\sqrt{L_mC_m}} \qquad 2.17$$

$$f_p = f_s \cdot \sqrt{1+\beta} = \frac{1}{2\pi\sqrt{(L_mC_mC_P)/(C_m+C_P)}} \qquad 2.18$$

Then, formulas for C_m and L_m can be obtained as follows.

$$C_m = C_P \cdot \left(\left(\frac{f_p}{f_s}\right)^2 - 1\right) \qquad 2.19$$

$$L_m = \frac{1}{(2\pi f_s)^2C_m} \qquad 2.20$$

2.2.3 Calculations of the Model Parameters

Usually, ultrasonic transducers have several resonance frequencies. In other words, the series resonant branch of the equivalent circuit consists of several subordinate branches. Moreover, it can be observed that excitations at frequencies that are even multiples of the natural vibrating fundamental frequency, i.e., $\omega_{2n} = n\omega_o = n2\pi f_o$, where n is even and f_o is the first resonance frequency, do not cause a displacement at the ends of the piezoelectric material [VAA2008]. Thus, the series resonant branches can be simplified by removing all of the even branches.

Equations 2.10, 2.11, 2.19, and 2.20 are applied at the series and parallel resonance frequencies, which are given by the transducer manufacturer, to calculate the value of the electrical components of the equivalent circuit. In our study, the operation frequency is less than 2 MHz. Therefore, we calculated the equivalent circuit of the piezoelectric transducer up to the third harmonic.

However, additional resonant frequencies can be found during the measurement because a piezoelectric resonator is a three-dimensional (3D) object [VAA2008]. These non-harmonic frequencies do not correspond to harmonics or multiples of the fundamental frequency. In order to obtain a more accurate model, we use the Matlab program to approach the measurements. Although other kind of software can be used here to perform the approaching, the Matlab provides the simplest way of approaching. The equivalent circuit and values of the components are shown in Figure 2.5.

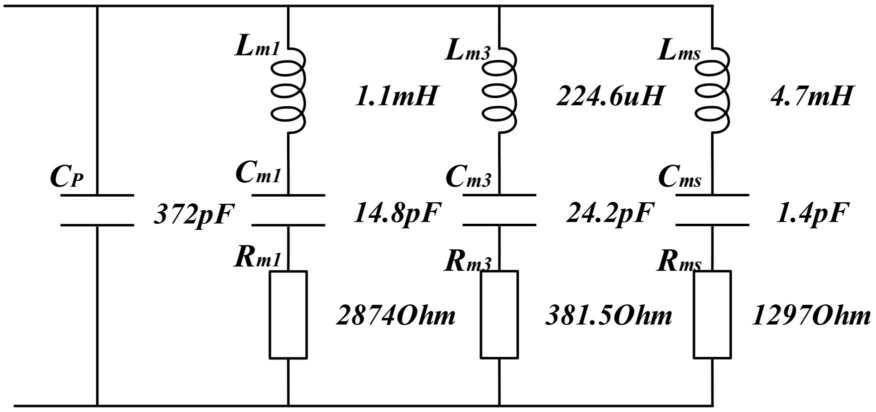


Fig.2.5 Equivalent circuit of the ultrasonic transducer used in this thesis.

The odd harmonics are a set of resonant frequencies that are based on odd multiples of the fundamental resonant frequency, and depend on the thickness and physical properties of the piezoelectric material [GTR1985]. As shown in Figure 2.5, the variable C_P denotes the static capacitor. Components L_{m1}, C_{m1}, and R_{m1} comprise the fundamental branch. Similarly, L_{m3}, C_{m3}, and R_{m3} represent the third harmonic branch, and L_{ms}, C_{ms}, and R_{ms} represent the non-harmonic frequency branch.

Based on the equivalent circuit shown in Figure 2.5, the impedance of the equivalent circuit at the working frequency (1.25 MHz) of the transducer can be described as

$$Z_{Eq}(jw)|_{w=w_{working}} = \frac{1}{jwC_P+\frac{1}{Z_{m1}(jw)}+\frac{1}{Z_{m3}(jw)}+\frac{1}{Z_{ms}(jw)}} \quad 2.21$$

It is known that $Z_{m1}(jw) = 1/R_{m1}$, so $Z_{Eq}(jw)$ can be rewritten as

$$Z_{Eq}(jw)|_{w=w_{working}} = \frac{1}{jwC_P+\frac{1}{R_{m1}}+\frac{1}{Z_{m3}(jw)}+\frac{1}{Z_{ms}(jw)}} \quad 2.22$$

By introducing the values of the components in the equivalent circuit into Equation 2.22, the equation becomes,

$$Z_{Eq}(jw)|_{w=w_{working}} = 36.65 - 308.2j \quad 2.23$$

The equivalent circuit of the transducer can be simplified, as shown in Figure 2.6.

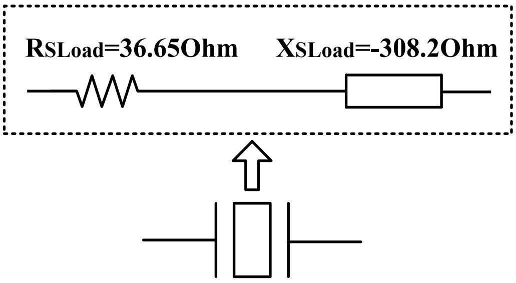


Fig.2.6 Simplified equivalent circuit of the ultrasonic transducer at its operational frequency.

2.2.4 Model Verification

We verified the Model by performing measurements of the transducer using a vector network analyzer (VNA) (Agilent N3382A). The calibration method used here is the short open load thru (SOLT). It is used to remove the parasitic effects introduced by the Bayonet Neill Concelman (BNC) connectors.

The measured impedance of the transducer and the equivalent circuit on the Smith chart are shown in Figure 2.6.

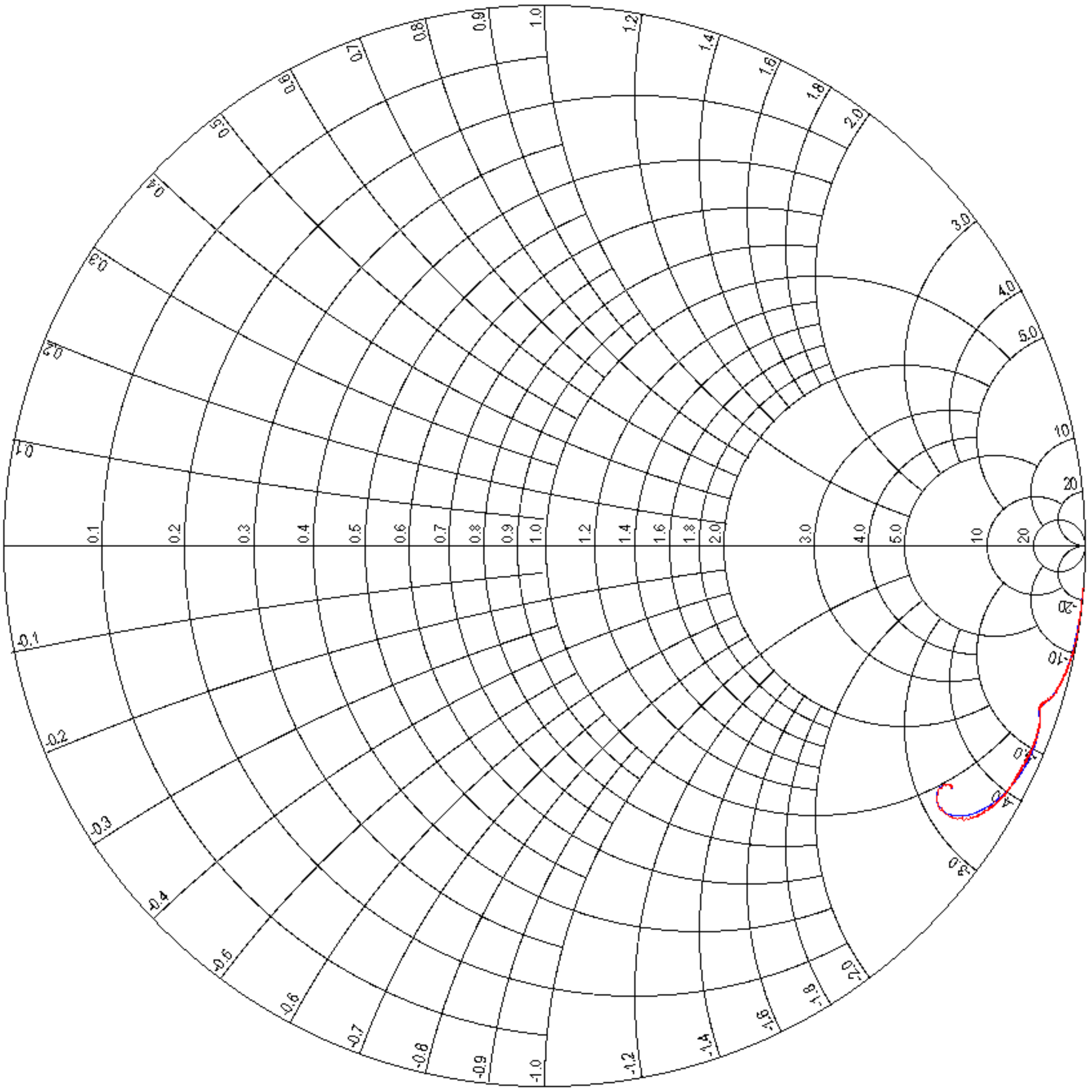
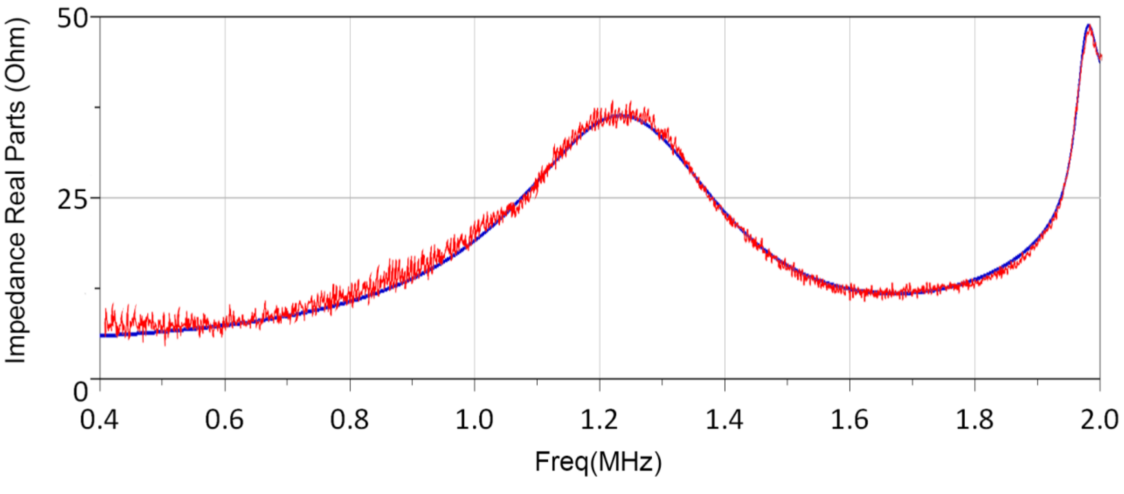
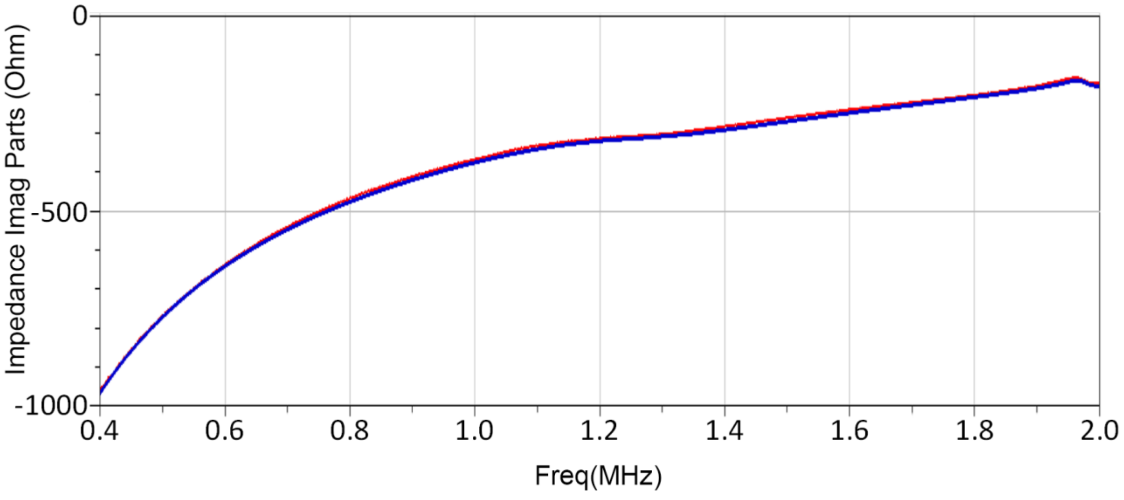


Fig.2.7 Measured impedance of the transducer (*Red*) and the impedance of the equivalent circuit on the Smith chart (*Blue*).

The measured impedance of the transducer versus frequency, and the impedance of the equivalent circuit as a function of frequency are illustrated in Figure 2.8. Figure 2.9 (*a*) shows impedance phase curves of the measured data and the equivalent circuit. And the module value of the measured impedance and the equivalent impedance is ploted in Figure 2.9 (*b*).

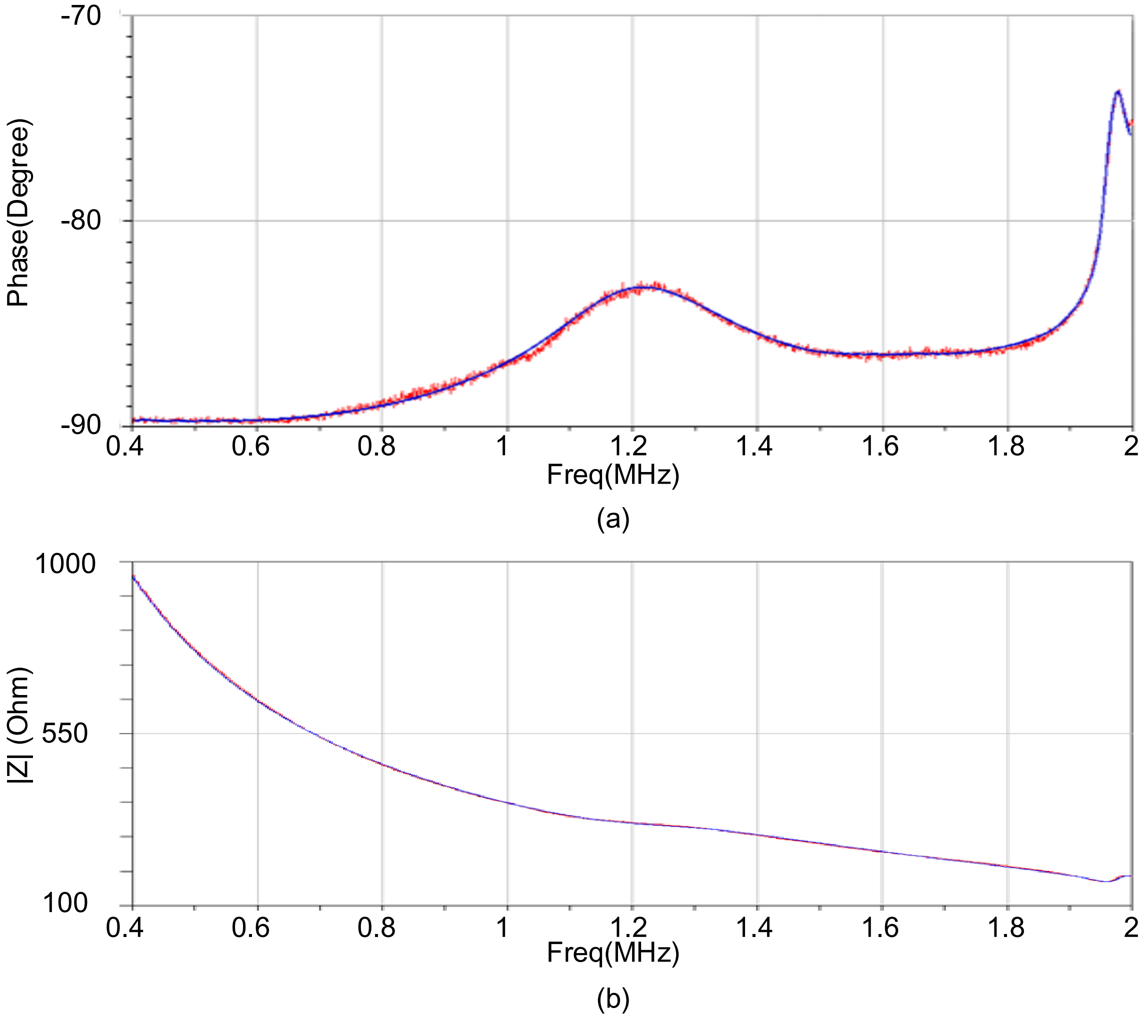


(***a***)



(***b***)

Fig.2.8 (*a*) Real parts of the measured impedance (*Red*) and the equivalent impedance (*Blue*). (*b*) Imaginary parts of the measured impedance (*Red*) and the equivalent impedance (*Blue*).



(a)

(b)

Fig.2.9 (a) Phase curves of the measured impedance (*Red*) and the equivalent impedance (*Blue*). (*b*) Module value of the measured impedance (*Red*) and the equivalent impedance (*Blue*).

As can be seen from Figures 2.7 and 2.8, the equivalent circuit of the transducer has nearly the same impedance characteristics as the measurement values.

2.3 Impedance-tuning Topologies

Based on the modeling of the transducer in section 2.2, ultrasonic transducers can be considered as reactive components. Further, the impedance of an ultrasonic power supply is pure resistive. If the transducer is driven directly by the ultrasonic power supply, the output power P_{OUT} can be described by

$$P_{OUT} = V_{Piez} \cdot I_{Piez} \cos \varphi \qquad 2.24$$

where V_{Piez} and I_{Piez} are the driving voltage and current, respectively. φ is the phase angle between the driving voltage and the current. We can determine that the output power reaches its maximum value when φ equals to 0. φ can be defined by

$$\varphi = tan^{-1}(B_{Piez}/G_{Piez}) \tag{2.25}$$

Where B_{Piez} and G_{Piez} define the electrical susceptanc and the conductance of the transducer. If $B_{Piez}/G_{Piez} = 0$, the power supply can provide the maximum power. Otherwise, there will be a reflected power that will cause a temperature rise or even unrecoverable damage to the transducer. Therefore, impedance-tuning topologies are required to balance out the susceptance of the transducer.

The impedance-tuning network can be classified as a static-tuning network and variable-tuning network based on the structure that they use [VBA2011]. For static-tuning networks, the calculated reactive components, such as the capacitor and inductor, are used to cancel the reactance part of the transducer, so the impedance of the transducer combined with the tuning network become pure resistive. The variable-tuning network is based on the static-tuning network. However, it uses a variable inductor or capacitor instead of the static ones to cancel the reactance part of the transducer, and it has a feedback signal that is used to change the value of the inductor or capacitor. The feedback signal is usually generated by an impedance-detector circuit. The variable-tuning network can solve the impedance-drifting problem of the transducer. The analysis of these two different tuning networks is presented in this section.

2.3.1 Basic Impedance-tuning Network

Figure 2.10 shows the simplified diagram of the static impedance-tuning network for ultrasonic transducers.

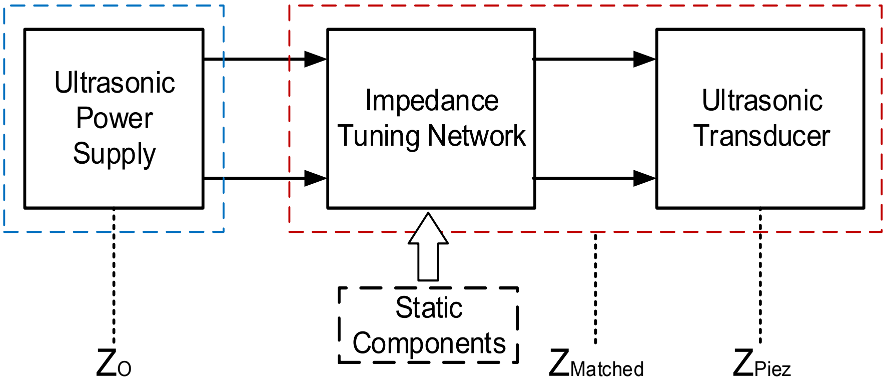


Fig.2.10 Simplified diagram of the static impedance tuning network ultrasonic transducer.

The output impedance of the ultrasonic power supply, the impedance of the transducer, and the matched impedance are defined as Z_O, Z_{Piez}, and $Z_{Matched}$, respectively. Z_O is usually purely resistive, so it can be described by $Z_O = R_O$, where R_O is the output resistance of the power supply. Based on the modeling of the transducer in section 2.2, Z_{Piez} can be defined by $Z_{Piez} = R_{Piez} + jX_{Piez}$, where R_{Piez} is the resistance of the transducer and X_{Piez} is the reactance of the transducer. $Z_{Matched}$ is defined as $Z_{Matched} = R_{Matched} + jX_{Matched}$, where $R_{Matched}$ defines the resistance of the matched transducer, and $X_{Matched}$ is the reactance of the matched transducer. The ideal matching condition can be obtained when $R_O = R_{Matched}$ and $X_{Matched} = 0$.

The static impedance-tuning network can be divided into two types, series-tuning networks and parallel-tuning networks [VBA2011]. Based on the analysis in section 2.2, the equivalent circuit of the transducer can be simplified as either parallel or series. Figure 2.11 shows the simplified equivalent circuit of the transducer.

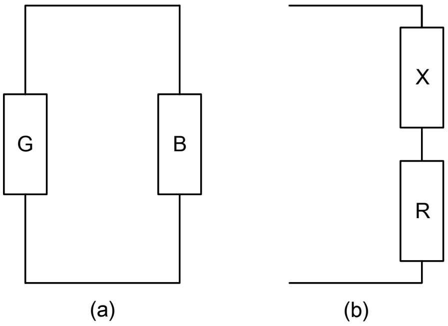


Fig.2.11 Simplified equivalent circuits of the transducer.

The corresponding tuning network is shown in Figure 2.12. The parallel-tuning network uses a shunted reactive component to cancel the susceptance part of the transducer. In addition, the reactive component, which has an opposite reactance to that of the transducer, is used in the series-tuning network.

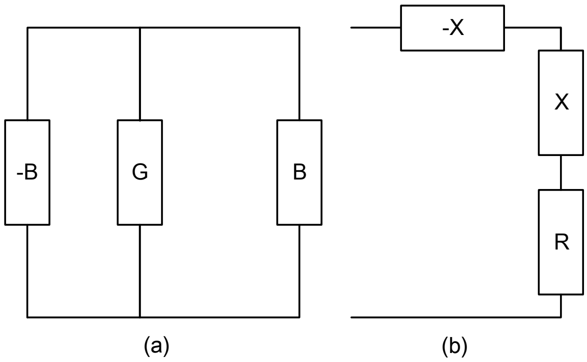
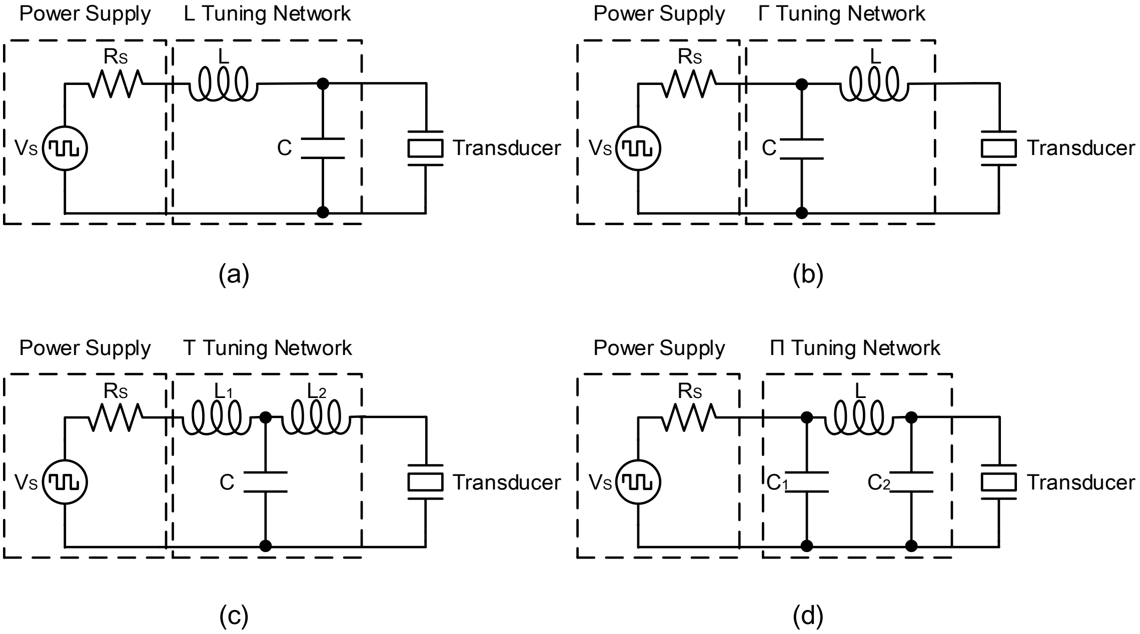


Fig.2.12 Parallel tuning network of the transducer (*a*) and series tuning network of the transducer (*b*).

The parallel-tuning network is usually used for high output-impedance power supplies [VAA2008]. In addition, the introduction of a parallel-tuning network positively affects the receive voltage sensitivity (RVS), yet it has no effect on the transmitting voltage response (TVR) [SCH2007]. The series-tuning network is commonly used for low output-impedance power supplies. The use of series-tuning networks causes an increase in the TVR, while not affecting the RVS [VAA2008, SCH2007]. In our case, to ensure the power efficiency, the output impedance of the power supply is required to be as low as possible, and the transducer is used to emit acoustic waves which usually has high impedance. Therefore, in this thesis, we used the series-tuning network. The above-mentioned tuning networks usually use a single inductor or a capacitor to compensate the susceptance or reactance of the transducer. However, the tuning network cannot match the resistance part of the transducer to the output resistance of the power supply. In order to match both the resistance part and reactance part of the transducer, we introduce a tuning circuit that consists of an inductor and capacitor. There are several different basic inductor-capacitor tuning networks, such as the L match, Γ match, T match, and Π match. Figure 2.13 presents schematics of the different inductor-capacitor tuning networks.



(a) (b) (c) (d)

Fig.2.13 Schematics of the L tuning network (*a*), Γ tuning network (*b*), T tuning network (*c*) and Π tuning network (*d*).

V_S is the power supply and R_S is the output resistance of the power supply. The characteristics of these tuning networks are shown in the following table.

Table 2.2 Characteristics of the different static tuning networks. [VBA2011]

Power Supply	***Transducer***	***Tuning network***
Low Impedance	*High Impedance*	*L Tuning Network*
High Impedance	*Low Impedance*	*Γ Tuning Network*
Low Impedance	*Low Impedance*	*T Tuning Network*
High Impedance	*High Impedance*	*Π Tuning Network*

In our thesis, the impedance of the power supply is chosed to be less than 10 mΩ to obtain a high power efficiency. From section 2.2, we know that the impedance of the transducer is much greater than the output impedance of the power supply. The circuit can be seen as a high-low-impedance transform system. Thus, the L tuning network is suitable for our application. In this thesis, we focus mainly on the analysis of the L tuning network.

The reactance of the inductor *L* and the susceptance of the capacitor *C* in the

L-type tuning network are defined as X_L and B_C, respectively. The schematic of the L tuning network can be simplified as the diagram shown in Figure 2.14.

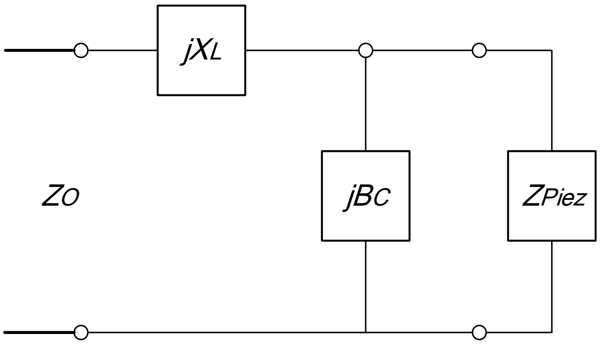


Fig. 2.14 Diagram of the L tuning network for the transducer.

Z_{Piez} is the impedance of the transform and Z_O is the output impedance of the power supply. To ensure that the impedance of the transducer is well matched to the power supply, the following equation must be true.

$$Z_O = jX_L + \frac{1}{jB_C + 1/(R_{Piez} + X_{Piez})} \tag{2.26}$$

By solving this equation, we can obtain the following formulas:

$$B_C(X_L R_{Piez} - X_{Piez} Z_O) = R_{Piez} - Z_O \tag{2.27}$$

$$X_L(1 - B_C X_{Piez}) = B_C Z_O R_{Piez} - X_{Piez} \tag{2.28}$$

Introducing Equation 2.25 into Equation 2.26, X_L and B_C can be rewritten as

$$B_C = \frac{X_{Piez} \pm \sqrt{R_{Piez}/Z_O}\sqrt{R_{Piez}^2 + X_{Piez}^2 - Z_O R_{Piez}}}{R_{Piez}^2 + X_{Piez}^2} \tag{2.29}$$

$$X_L = \frac{1}{B_C} + \frac{X_{Piez} Z_O}{R_{Piez}} - \frac{Z_O}{B_C R_{Piez}} \tag{2.30}$$

We can see that there are two solutions for X_L and B_C. When $B_C > 0$, it is a capacitor, and where $B_C < 0$, it is an inductor. With respect to X_L, when it is greater than 0, it is an inductor, whereas when it is less than 0, it is a capacitor. In our case, the output of the power supply is a square wave. A low-pass filter is required to compensate the higher harmonics of the square wave. Thus, only the solution $X_L > 0$ and $B_C > 0$ can be used in our project. In other words, the LC-type L tuning network is suitable for our transducer.

As far as the variable-tuning network is concerned, it contains the components with variable values against those with constant values used in static tuning network. In addition, we applied a feedback loop to control the variation of these components. During the working period, the temperature drift or the changing of the working medium will cause fluctuations in the transducer impedance. The feedback loop of the variable-tuning network can measure this variation, and it can generate a control signal for the variable components. In this way, we can solve the impedance mismatch that is caused by transducer impedance drifting. The diagram of the variable-tuning network is illustrated in Figure 2.15.

The most important part of the variable-tuning network is the impedance measurement circuit. The impedance of the matched transducer $Z_{Matched}$ is measured using this circuit. The control-signal generator circuit usually consists of a microprogrammed control unit (MCU) or a computer. Based on the measured $Z_{Matched}$, we used the MCU to calculate the parameters of the impedance-tuning network. Finally, the control voltage V_{ctr} is generated by the MCU to control the variable components in the impedance-tuning network. After this operation, $Z_{Matched}$ is tuned to equal the output impedance of the power supply Z_O. The impedance drift of the transducer is cancelled by changes in the tuning network parameters.

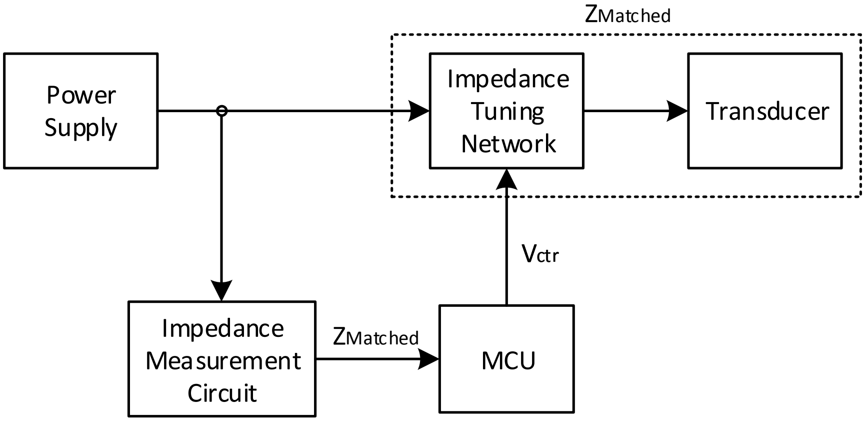


Fig.2.15 Diagram of the variable-tuning network for the transducer.

The impedance-measurement circuit is divided into three different types according to the topologies: bridge method, I-V method, auto-balancing bridge method, and resonance method [NI2007].

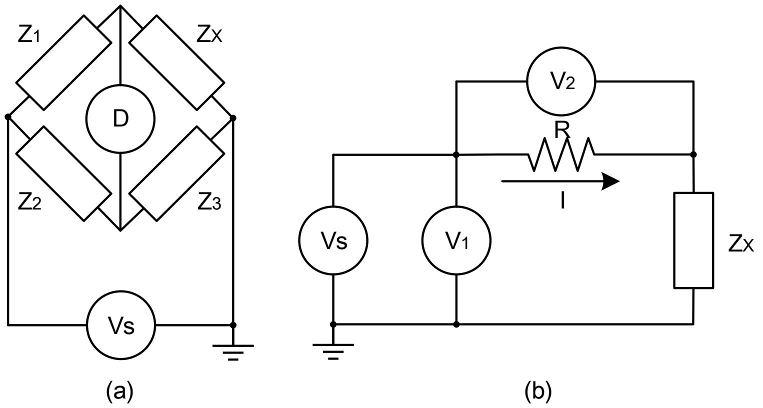


Fig.2.16 Equivalent circuits of (a) the bridge method and (b) the I-V method.

Figure 2.16(*a*) presents the equivalent circuit of the bridge method. Z_X is the unknown impedance and Z_1, Z_2, and Z_3 are the known impedances. If there is no current flow through the detector *D*, the value of Z_X can be obtained by

$$Z_X = \frac{Z_1}{Z_2} \cdot Z_3 \tag{2.31}$$

The advantages of the bridge method are as follows [NI2007]: High accuracy (0.1% error); wide frequency coverage by using different types of bridges (0~300MHz); low cost. However, four disadvantages make it unsuitable for our application: Needs to be manually balanced; narrow frequency coverage with a signal instrument; unfit for the grounded devices; MCU or computer is required to calculate the impedance.

The equivalent circuit of the I-V method is demonstrated in Figure 2.16(*b*). In a real case, the resistor *R* is usually replaced by a low-loss transformer to reduce the effects caused by *R* [NI2007]. However, the use of a transformer limits the frequency range. As can be observed from this figure, Z_X can be calculated by the values of the voltage and current. The equation of Z_X can be written as

$$Z_X = \frac{V_1}{I} = \frac{V_1}{V_2} R \tag{2.32}$$

I-V method is suitable for the grounded devices. And it can also provide a real time measurement of the impedance. But the using of the transformer leads to a compatibility problems with MRI system. And the same as the bridge method, it needs MCU or computer to obtain the impedance.

Figure 2.17(*a*) shows the equivalent circuit of the auto-balancing bridge method. By tuning the parameter of the R and V_R, the current I_X, which flows through the unknown impedance Z_X, can be made equal to the current that flows through the resistor R. Then, the potential at the L point is kept at 0 V (which is called virtual ground). The impedance of Z_X can be obtained by measuring the voltage at point H (V_X) and the voltage applied across R (V_R).

$$Z_X = \frac{V_X}{I_X} = \frac{V_X}{V_R} R \qquad 2.33$$

Compared with the previous methods, the auto-balancing bridge method can provides good compatibility with grouded devices and high accuracy over a wide impdance measurement range. There is no large magnetic component used in this method. So it is well suited for the MRgFUS. However, by using this method, the unknown impedance Z_X is still need to be calculated by using other parameters. In other word, a MCU is required to calculate the impedance of Z_X.

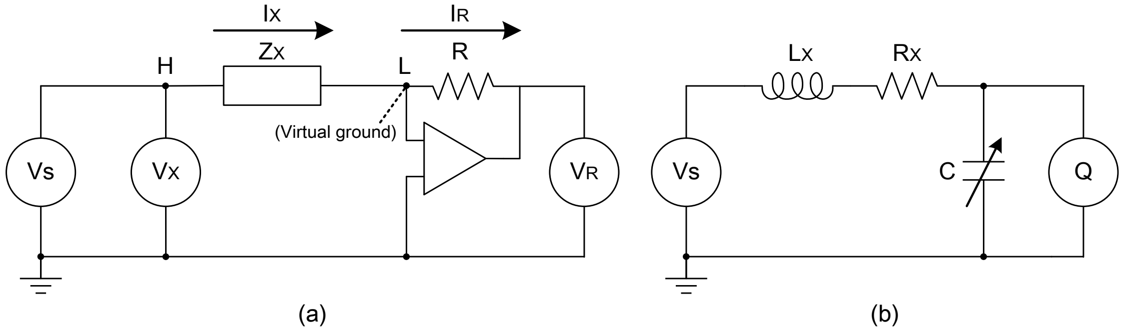


Fig.2.17 Equivalent circuits of the auto-balancing method (a) and resonance method (b).

The equivalent circuit of the resonance method is presented in Figure 2.17(b). When the circuit was adjusted to resonance by adjusting a tuning capacitor C, we obtained the unknown impedance values L_X and R_X from the test frequency, C value, and Q value. Q can be obtained by measuring the voltage applied across the tuning capacitor. Other than the direct connection shown here, series and parallel connections are possible for a wide range of impedance measurements.

For the resonance method, it has a simple structure. The measured devices is a part of the resonance circuit. And the resonance circuit can be a part of the tuning circuit. Therefore, it can achieve an auto tuning system based on this method by adding a feedback control signal on the tunable capacitor or inductor. This method is based on the topology of resonance circuit, so the impedance of the measured components can be obtain by detecting the phase difference between the input signal and output signal of the resonance circuit. The disadvantage of the resonance method is the low impedance measurement accuracy at high operating frequency. If the operating frequency is high, there will be a distortion of the output signal. This unavoidable distortion will cause a low impedance measurement accuracy. And MCU is also required in the existing resonance impedance measurement circuits.

2.3.2 Summary of the Basic Impedance Tuning Networks

Although the basic impedance tuning networks provide valuable information and techniques for designing tuning network for our application, none of the existing tuning networks can offer a comprehensive solution to resolve our challenges, such as elimination of large magnetic components; compensation of impedance drifting caused by temperature, aging; small circuit surface. Hence, another approach is needed. Tables 2.3 gives out the comparation of the basic impedance tuning networks.

As analyzed in section 2.3.1, the L tuning network is suitable for our applicaton. But it can not solve the impedance drifting of the transducer. And for the dynamic tuning networks, the resonance method is more suitable for our application than others. It has a simple structure and the impedance measurement circuit of this method can be a part of the tuning circuit for the power amplifier. And it is suitable for realizing an auto tuning system based on this method by adding a feedback control signal on the tunable capacitor or inductor. The maximum working frequency of the resonance method is usually tens of megahertz [NI2007], which is much larger than the working frequency of the tranducer (1.25MHz). Thus, the accuracy of this method is acceptable. The only disadvantages of this method is the requirement of the MCU. So a novel auto impedance tuning system based on the resonance method will be presented in chapter 4.

Table 2.3 Comparison of the basic tuning networks.

Topologies		***Impedance Transformation (Power-Load)***	***Comments***
Static Tuning Network [VBA2011]	*L Tuning Network*	*Low-High Impedance*	*Simple structure*
	Γ Tuning Network	*High-Low Impedance*	*Simple realization*
	T Tuning Network	*Low-Low Impedance*	*Cannot eliminate*
	Π Tuning Network	*High-High Impedance*	*the impedance drifting*

Topologies		***Working Frequency***	***MRI Compatibility***	***Comments***
Dynamic Tuning Network [NI2007]	*Bridge Method*	*0~300MHz*	*No*	*Non-real time* *Unfit for grounded devices*
	I-V Method	*10k~100MHz*	*No*	*Real time* *Needs transformer*
	Auto-balancing	*20~110MHz*	*Yes*	*Real time* *Complex structure*
	Resonance Method	*10k~70MHz*	*Yes*	*Real time* *Simple structure*

Chapter 3

Power Amplifier Design

3.1 Introduction

Design of a power Amplifier for the ultrasonic transducer used in HIFU application is one of the objectives of this thesis. In this chapter, the principles of the existing power amplifiers are explained. Furthermore, the former articles about the amplifier for HIFU are reviewed and discussed. A comparison between these amplifiers is also presented in this chapter. At last, the circuit design and analysis of the power amplifier used in our project is presented. This chapter is organized as follows: Section 3.2 has a review of some typical amplifiers that can be used for our project. Section 3.3 presents several published works that relate to the design of power amplifiers for ultrasound therapy. In Section 3.4, we present a comparison of these amplifiers. Section 3.5 describes the circuit design and analysis of the proposed power amplifier. Section 3.6 gives out the prototype of the power amplifier, and the test results of this prototype is also presented in this section. Finally, a summary of the proposed power amplifier is given out in Section 3.7

3.2 Theory of Typical Power Amplifiers

3.2.1 Current-source Amplifiers

Current source-based power amplifiers can be classified as A, B, AB, and C based on the conduction angle and the bias. Due to the strongly non-linear behavior of the class C amplifier, it is unsuitable for our application. Therefore, it will not be discussed in this thesis. The configurations of the other three amplifiers (class A, B, AB) used for MRgFUS are usually a single transistor amplifier with an impedance-tuning network. Simplified schematics of the class A, B, and AB amplifier are shown in Figure 3.1.

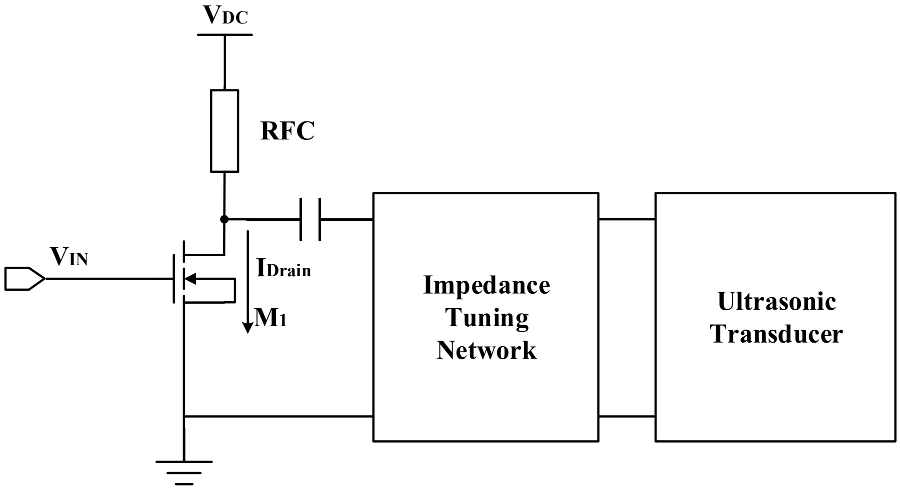


Fig.3.1 Simplified schematic of class A, B, and AB power amplifiers.

The relationships between the drain to source voltage V_{DS} and the drain current I_{Drain} of the class A, B and AB power amplifiers operating point are plotted in Figure 3.2

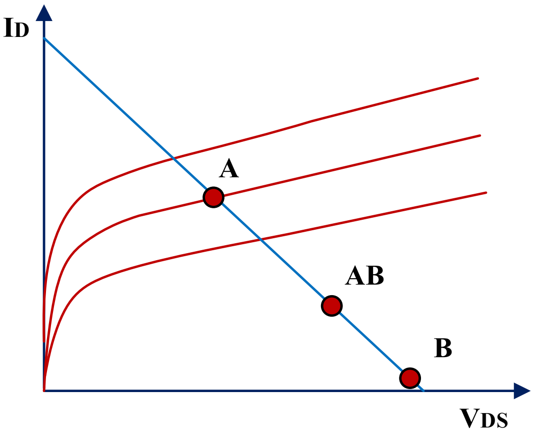


Fig.3.2 Operating points of class A, B and AB amplifiers. [VAA2008]

The waveform of the drain current in the frequency domain is illustrated in Figure 3.3. [VAA2008]

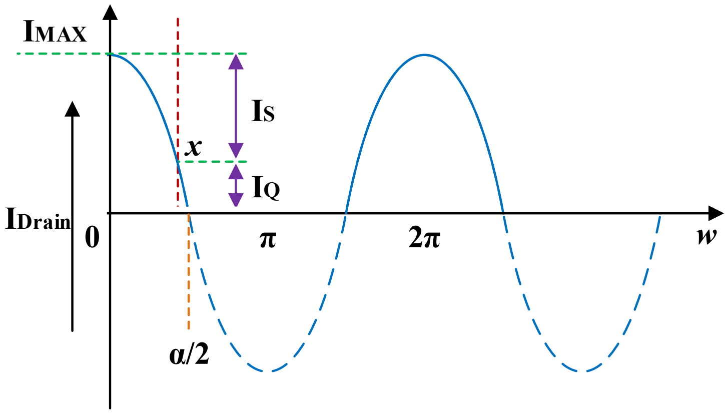


Fig.3.3 Waveform of the drain current in time domain.

Using θ and α as the drain current angle at point x and the conduction angle, respectively, the drain current I_{Drain} at point x can be described as in Equation 3.1.

$$I_{Drain}(\theta) = I_Q + I_s \cdot cos\,\theta \quad (-\alpha/2 < \theta < \alpha/2) \qquad 3.1$$

And the following equations can also be easly obtained,

$$cos(\alpha/2) = -\left(I_Q/I_s\right) \quad and \quad I_s = I_{\mathrm{MAX}} - I_Q \qquad 3.2$$

By substituting Equation 3.2 into Equation 3.1, $I_{Drain}(\theta)$ can be rewritten as

$$I_{Drain}(\theta) = \frac{I_{MAX}}{1-cos(\alpha/2)} \cdot [cos\,\theta - cos(\alpha/2)] \qquad 3.3$$

The DC current I_{DC} during the conduction period can be defined as

$$I_{DC} = \frac{1}{2\pi} \cdot \int_{-\alpha/2}^{\alpha/2} I_{Drain}(\theta) d\theta \qquad 3.4$$

By solving this equation, I_{DC} can be rewritten as Equation 3.5.

$$I_{DC} = \frac{I_{MAX}}{2\pi} \cdot \frac{2\,sin(\alpha/2) - \alpha \cdot cos(\alpha/2)}{1-cos(\alpha/2)} \qquad 3.5$$

The first harmonic I_1 of current I_{Drain} is shown in Equation 3.6.

$$I_1 = \frac{1}{\pi} \cdot \int_{-\alpha/2}^{\alpha/2} I_{Drain}(\theta) \cdot cos\,\theta\, d\theta \qquad 3.6$$

which can be rewritten as

$$I_1 = \frac{I_{MAX}}{2\pi} \cdot \frac{\alpha - \sin\alpha}{1-cos(\alpha/2)} \qquad 3.7$$

Based on Equation 3.5 and 3.7, the fundamental output power P_{OUT} and the average DC power P_{DC} can be described as follows.

$$P_{OUT} = P_1 = \frac{V_{DC} \cdot I_1}{2} = \frac{V_{DC}}{2} \cdot \frac{I_{MAX}}{2\pi} \cdot \frac{\alpha - \sin\alpha}{1 - \cos(\alpha/2)} \tag{3.8}$$

$$P_{DC} = V_{DC} \cdot I_{DC} = V_{DC} \cdot \frac{I_{MAX}}{2\pi} \cdot \frac{2\sin(\alpha/2) - \alpha \cdot \cos(\alpha/2)}{1 - \cos(\alpha/2)} \tag{3.9}$$

Thus, the power efficiency of the current source-based amplifier is as follows.

$$\eta_{OUT} = \frac{P_{OUT}}{P_{DC}} = \frac{\alpha - \sin\alpha}{2 \cdot [2\sin(\alpha/2) - \alpha \cdot \cos(\alpha/2)]} \tag{3.10}$$

Class A Amplifier

Class A amplifier is a very simple amplifier with a very good linearity, but its power efficiency is low.

The gate-to-source voltage V_{GS} of the transistor *M1* is greater than V_{TH} (the threshold voltage of *M1*). The current flows through M1 during the whole waveform cycle, even if there is no signal being amplified. This continuous biasing method causes a loss of power and overheating. The conduction angle of a class A amplifier is 2π. Therefore, the power efficiency of class A is

$$\eta_{OUT(\text{Class}A)} = \frac{2\pi - \sin 2\pi}{2 \cdot [2\sin(\pi) - 2\pi \cdot \cos(\pi)]} = 50\% \tag{3.11}$$

To achievement its theoretical efficiency, the amplifier must have a maximum signal swing without compression [LG2005]. The waste power of the amplifier changes into thermal energy. If there is no cooling facility in the amplifier, the over heating will cause a severely damage to the circuits.

Class B Amplifier

The bias point of the class B amplifier is set to the transistor's threshold voltage V_{TH}. Thus, the drain current only flows during a half cycle of the waveform.

The transistor only turns on during the positive half cycle, so the efficiency of the class B amplifier is higher than that of a class A amplifier. The conduction angle of the class B amplifier is π. The power efficiency of class B is shown in Equation 3.12

$$\eta_{OUT(ClassB)} = \frac{\pi - \sin\pi}{2 \cdot [2\sin(\pi/2) - \pi \cdot \cos(\pi/2)]} = 78.5\% \tag{3.12}$$

The DC power that is consumed in a class B amplifier is less than that of a class A amplifier with a decreased signal amplitude. No DC current is drawn in class B as long as there is no input signal. Consequently, the degradation of the efficiency at low-signal amplitudes is not as significant as for the class A amplifier. Moreover, the energy dissipation and the heating are reduced.

Class AB Amplifier

The transistor in a class AB amplifier has a conduction angle that ranges from π to 2π. The bias point for this kind of amplifier is greater than V_{TH}, and is lower than the bias point of the class A amplifier. Therefore, the power efficiency of a class AB amplifier is between that of a class A and a class B.

The output signal of a class AB amplifier is more than a half cycle. This type of amplifier provides a better efficiency than that of a class A amplifier, and has a smaller distortion compared with that of a class B amplifier.

3.2.2 Switched-mode Amplifiers

Current-based amplifiers, which are discussed in a former section, all have low power efficiency. The dissipated power is converted into thermal energy, and can severely affect the circuit. These disadvantages limit the usage of these amplifiers in current HIFU applications, such as phased-array HIFU systems. In this section, we discuss different types of switched-mode amplifiers that are suitable for HIFU applications. The switched-mode amplifier uses a transistor, which enables instantaneous switching between on and off states [VAA2008]. Figure 3.4 illustrates the switching method of the transistor in a switched-mode amplifier.

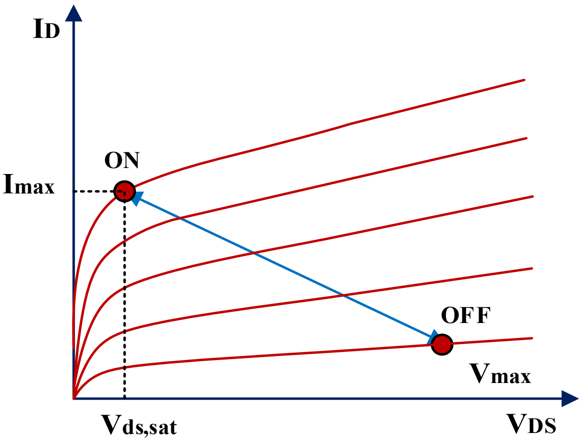


Fig.3.4 Switch method of the transistor in a switched-mode amplifier. [VAA2008]

Ideally, the output impedance R_{Switch} of the switched-mode amplifier is zero when the switch turns on. Moreover, when the switch turns off, R_{Switch} changes to infinity. Thus, both of the current flows through the switch I_{Switch} and the voltage applied across the switch V_{Switch} are zero in the ideal case. The theoretical power efficiency of the switched-mode amplifier can reach 100%. However, the actual resistance of R_{Switch} is limited. The actual power efficiency of the switched-mode amplifier is about 90%.

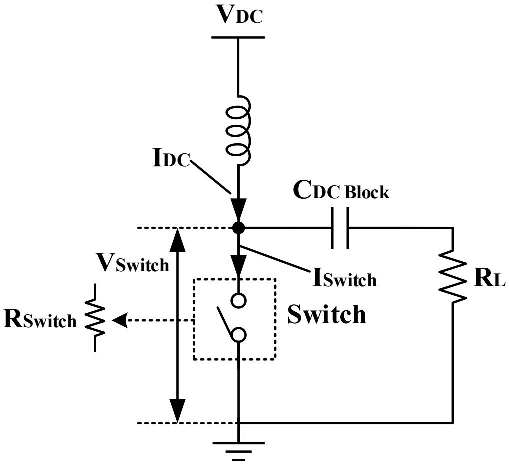


Fig.3.5 Simplified schematic of the basic switched-mode amplifier.

A simplified schematic of the switched-mode amplifier is demonstrated in Figure 3.5. To ensure that the transistor works in switch mode, the input signal of the amplifier must be large enough to drive the transistor into its saturation region. This leads to nonlinear input and output characteristics. Moreover, the output waveform of the switched amplifier is square wave. In order to reduce the waste power caused by the harmonics, a tuning network is required at the output stage of the switched-mode amplifier. Two primary kinds of tuning networks can be applied to the switched-mode amplifier. The simplified schematics of these two tuning networks are shown in Figure 3.6.

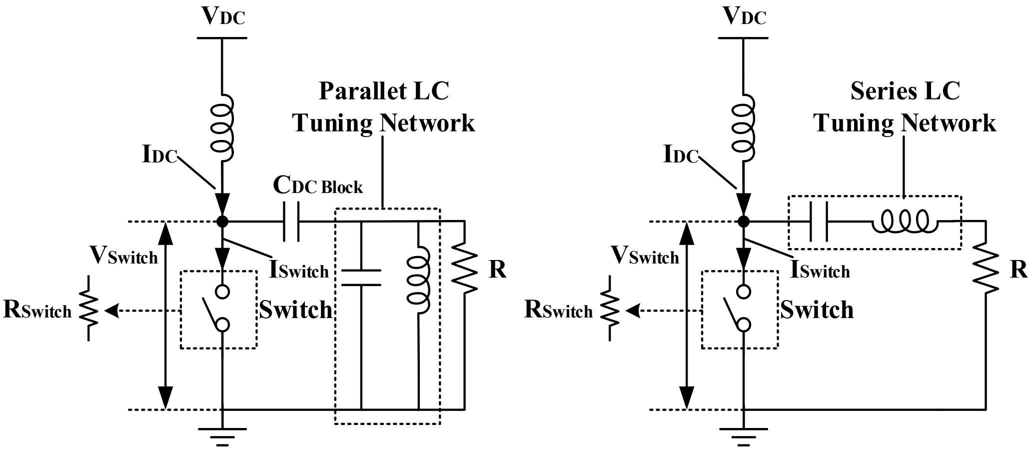


Fig.3.6 Simplified schematics of the parallel LC tuning network (left) and the series LC tuning network (right).

In many applications, several tuning networks with very complex structures are applied to achieve very few harmonics in the output signal.

Currently, there are many kinds of switched-mode amplifier, such as class D, class E, and class DE amplifiers. In this thesis, we focus mainly on the switched-mode amplifier that is suitable for HIFU systems.

Class D Amplifier

Based on the structure, there are two types of Class D amplifiers, namely the class D half-bridge voltage-switched amplifier and the full-bridge voltage-switched amplifier [NMA2007]. There are currently many different operating methods for class D amplifiers. In this thesis, we focus on the class D amplifier with a duty cycle of 50%. The schematic and equivalent circuit of the half-bridge class D amplifier are illustrated in Figure 3.7 (*left*) and (*right*), respectively.

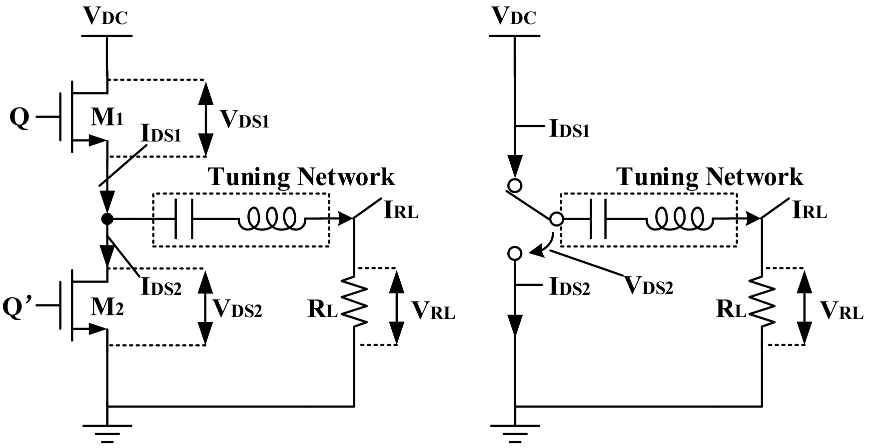


Fig.3.7 Simplified schematic of half-bridge class D amplifier with a duty cycle of 50% (*left*), and the equivalent circuit of this amplifier (*right*).

The transistors *M1* and *M2* turn on alternately at a half duty cycle to charge or discharge the tuning network. Based on the Fourier analysis, the drain-to-source voltage of *M2* (V_{DS2}) can be described by the following equation.

$$V_{DS2} = V_{DC}\left(\frac{1}{2} + \frac{2}{\pi}\sin\theta + \frac{2}{3\pi}\sin 3\theta + \cdots\right) \qquad 3.13$$

The tuning network that is used in this class D amplifier is the LC tuning network. By supposing that the LC resonance has a reactance of zero at the fundamental frequency and a high impedance at the harmonics, the harmonics of the current can be ignored. In this condition, the voltage and current of R_L can be written as follows,

$$V_{RL} = V_{DC}\cdot\frac{2}{\pi}\sin\theta \qquad 3.14$$

$$I_{RL} = \frac{V_{DC}}{R_L}\cdot\frac{2}{\pi}\sin\theta \qquad 3.15$$

Therefore, the maximum output power P_{RL} can be achieved when θ equals π/2.

$$P_{RL} = \frac{2}{\pi^2}\frac{{V_{DC}}^2}{R_L} \qquad 3.16$$

The DC current I_{DC} is given by the average of I_{RL} [VAA2008]. Since the associated Fourier transformation of a sinus function adds a factor of 1/π, we get

$$I_{DC} = \mathrm{Max}(I_{RL})\frac{1}{\pi} = \frac{2}{\pi^2}\frac{V_{DC}}{R_L} \qquad 3.17$$

The average DC power consumption P_{DC} can be defined as

$$P_{DC} = V_{DC} \cdot I_{DC} = \frac{2}{\pi^2}\frac{V_{DC}^2}{R_L} \tag{3.18}$$

Finally, in the ideal case, the power efficiency of this half-bridge class D amplifier is given by

$$\eta_{out} = \frac{P_{RL}}{P_{DC}} = 100\% \tag{3.19}$$

However in real cases, the tuning net-work can not eliminate all of the harmonics. Further, the characteristics of transistors *M1* and *M2* are not perfect as the ideal ones, so there will be power losses. The actual power efficiency of the class D amplifier is nearly 90%.

The schematic of the full-bridge class D amplifier, with a duty cycle of 50%, is demonstrated in Figure 3.8. The power efficiency analysis of this amplifier is nearly the same as that of the half-bridge one. The full-bridge class D amplifier can offer two times peak to peak output voltage compared with the half-bridge one. However, it has two more transistors than the half-bridge class D amplifier. The power efficiency of the full-bridge class D is lower than the half-bridge one. And the control signals of the full-bridge class D amplifier are more complex than the half-bridge ones.

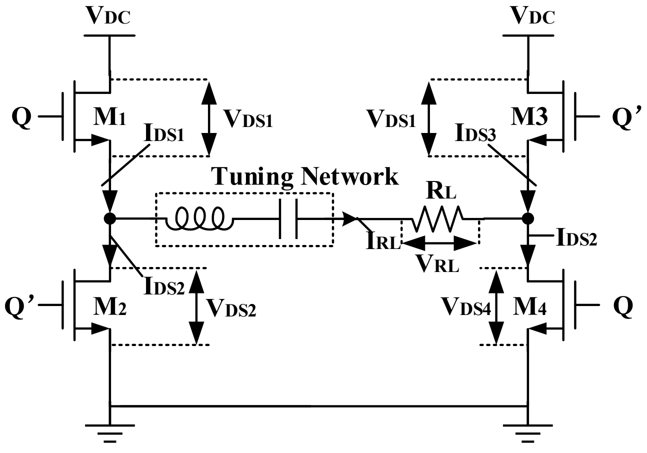


Fig.3.8 Simplified schematic of half bridge class D amplifier with a duty cycle of 50%.

Class E Amplifier

The Class E amplifier is another type of switched-mode amplifier that can achieve a theoretical power efficiency of 100%. However, as opposed to the class D amplifier, only one transistor is used in the class E amplifier. The simplified schematic and the equivalent circuit of the class E amplifier are presented in Figure 3.9 (*left*) and (*right*). The current flows through the L_{RFC} is controlled by the switching state of transistor *M1*. *L* and *C* comprise the tuning network that is used to filter out the harmonics.

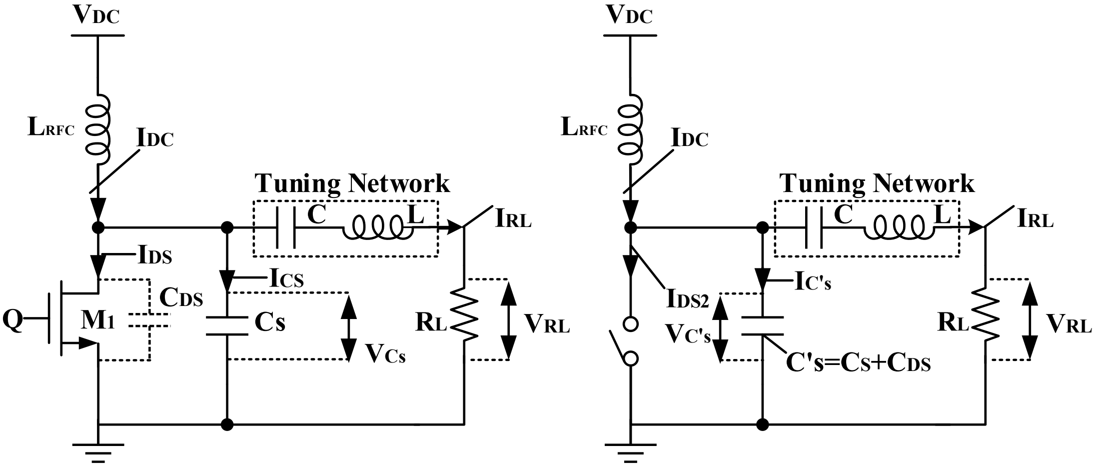


Fig.3.9 Simplified schematic of class E amplifier (*left*) and the equivalent circle of this amplifier (*right*).

There are two important rules that need to be satisfied in the class E amplifier: ZVS (zero-voltage switching) and ZDS (zero-derivative switching) [AM2001]. Because of these two rules, there will be no overlap between I_D and V_{DS}. In other words, there are no power losses. Therefore, the theoretical power efficiency can reach 100%.

Based on the analysis presented in [VAA2008], the voltage applied across the load R_L at the fundamental frequency can be defined as

$$V_{RL} = \sqrt{1 + \frac{\pi^2}{4}} \cdot I_{DC} \cdot R_L \qquad 3.20$$

Therefore, the output power of the amplifier can be described as in Equation 3.21.

$$P_{RL} = \frac{{V_{RL}}^2}{2R_L} = \left(1 + \frac{\pi^2}{4}\right) \cdot \frac{{I_{DC}}^2 \cdot R_L}{2} \qquad 3.21$$

The power efficiency of the class E amplifier can be defined as

$$\eta_{out} = \frac{P_{RL}}{P_{DC}} = \frac{\left(1+\frac{\pi^2}{4}\right) \cdot \frac{{I_{DC}}^2 \cdot R_L}{2}}{{I_{DC}}^2 \cdot R_{DC}} \qquad 3.22$$

If $(1+\pi^2/4)R_L=2R_{DC}$, the power efficiency can reach to 100%, which is the theoretical power efficiency of the class E amplifier.

The major drawback of a class E amplifier is the need for an RF choke, which is used to limit the current ripples generated by switching. For a 10% current ripples, the minimum inductance of the choke is approximately 8.7 times the series resistance Rs, divided by the switching frequency.

Other Types of Switched-mode Amplifier for Transducers

Besides the basic switch-mode amplifiers that were previously analyzed, there are several switched-mode amplifiers with other topologies, such as step-up driving, flyback, and push-pull topologies [WKC2005].

The schematic of the amplifier that uses the step-up driving topology is demonstrated in Figure 3.10.

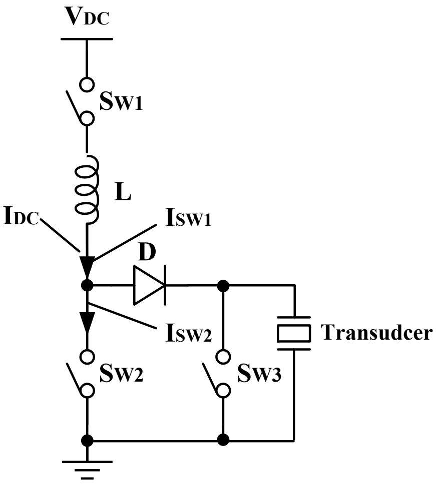


Fig.3.10 Schematic of switched-mode amplifier with step-driving method.

There are three working periods for this amplifier. In the first period, switches S_{w1} and S_{w2} turn on, and S_{w3} turns off. The inductor L is charged, and the transducer is shorted by S_{w2}. Then, S_{w2} switches off, and the transducer is charged by the energy stored in L. In the last period, S_{w1} turns off and S_{w3} turns on, and the transducer is discharged. The step driving power amplifier do not need of tuning circuit, which makes it easy to realize. However, the use of three switches leads to a requirement of a very complex control circuit, and the switching times of the switches must be chosen carefully to avoid overlaps. Moreover, the use of a diode *D* leads to additional power losses. Afterall, it is unsuitable for our application.

Figure 3.11 shows the schematic of the amplifier using the flyback method. The flyback topology uses a transformer with a signal switch to amplify the signal. The switch is connected to the primary coil, and the transducer is connected to the secondary coil.

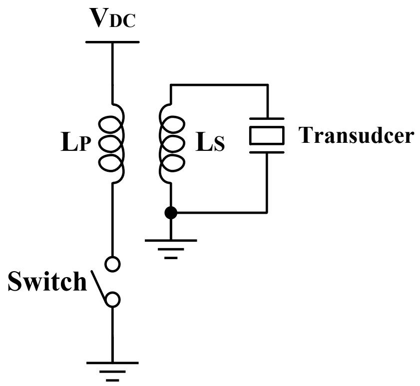


Fig.3.11 Schematic of switch-mode amplifier using flyback topology.

The flyback switched-mode amplifier is also no need of tuning network. Although, this amplifier has a very simple structure, the capacitive components of the transducer and the secondary coil can create an oscillation loop. And due to the use of transformer, this amplifier is unsuitable for MRgFUS.

The push-pull switched-mode amplifier is illustrated in Figure 3.12, and appears to be an upgraded version of the flyback amplifier. S_{w1} and S_{w2} turn on and off in a half cycle alternately. The transformer also plays a part in the impedance tuning of the transducer. The push pull switched-mode amplifier can provide very large output power. And it has a very simple structure. However, the same as the flyback switched-mode amplifier, the use of the transformer makes it incompatible with MRI. And the working frequency is limited by the transformer.

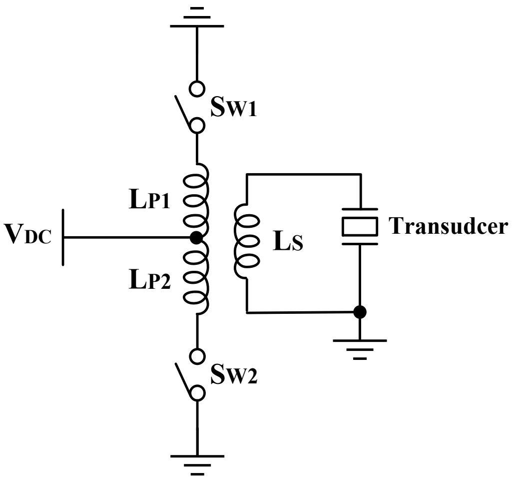


Fig.3.12 Schematic of switch-mode amplifier using push-pull driving method.

3.3 Review of Existing Power Amplifiers

After the discussion about different amplifier topologies, in this section, we present a review of existing power amplifiers for ultrasound therapy. As discussed in the previous section, power amplifiers can be classified as current source-based amplifiers and switched-mode amplifiers. Therefore, in this section, we separately review these two types of amplifiers. First, we discuss the current source-based amplifiers, after which we review switch-mode amplifiers.

3.3.1 Existing Current-source Amplifiers

Shyr-Long Jeng and Yung-Cheng Tung [TYC2008] presented a multicell linear power amplifier for piezoelectric transducers by using discrete components. The circuit can provide a ±200 V output swing with a corner frequency of 100 kHz and an output current as high as 2.5A. The amplifiers used in the output stage are LM4700, which is a class AB amplifier. Although, this amplifier offers a very high output power, its low efficiency, and narrow bandwidth make it unsuitable for our application. Figure 3.13 shows the schematic of this amplifier.

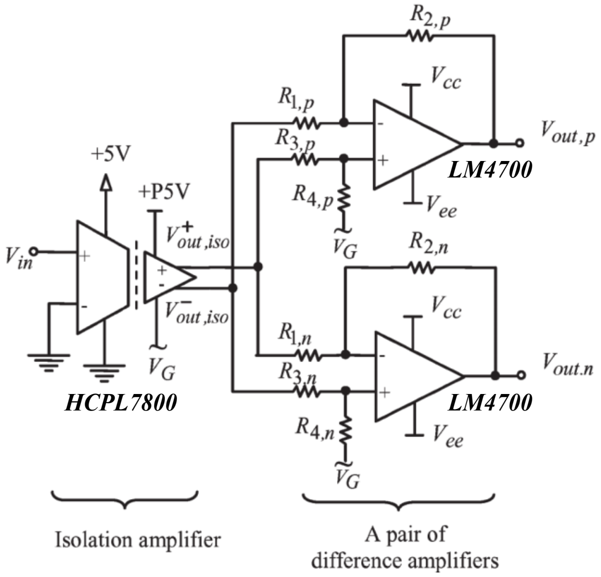


Fig.3.13 Schematic of the multicell linear-power amplifier. [TYC2008]

Kexu Sun, Zheng Gao, et al. [SK2015] proposed a class AB power amplifier with a digital feedback predistortion system to improve the power efficiency. The amplifier can drive a load of 300 pF in parallel with a 100 Ω resistor with a power efficiency of 44% and a signal swing up to 180 V_{p-p}. This amplifier is more efficient than the former one, and it is realized using integrated circuits (ICs). However, its efficiency is still lower than our required value, and the output swing of this amplifier is limited by the silicon-on-insulator (SOI) process used to fabricate the circuit. The diagram of this amplifier is illustrated in Figure 3.14.

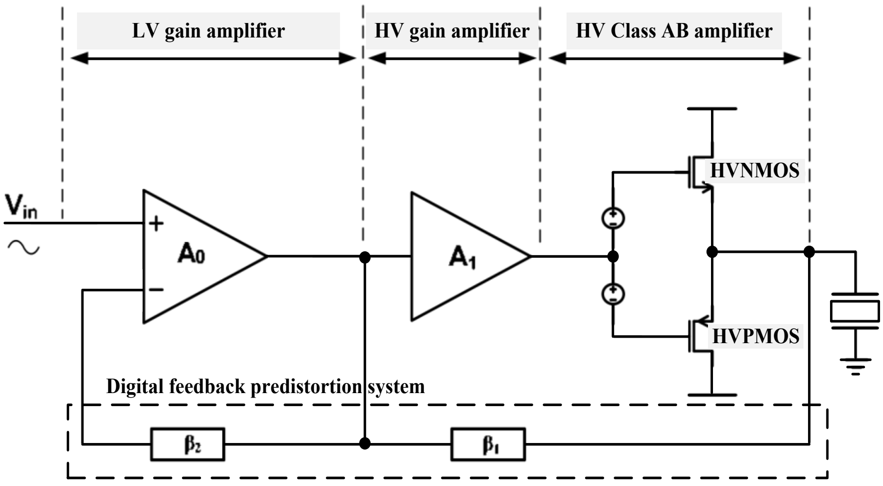


Fig.3.14 Diagram of the class AB power amplifier with predistortion system [SK2015].

A high-voltage linear amplifier for integrated two-dimensional (2D) ultrasound transducer array was introduced in [GSH2013]. It is a class B amplifier with a ±25 V output swing and 6.2 MHz bandwidth. However, this amplifier was designed using a CMOS process, which limits its output power.

Dario Bianchi et al. also designed a class B amplifier for transducers [BD2014], which was realized using BCD6-SOI technology. Its performances are as follows: output swing 90 V_{p-p}, power efficiency of 60% and 6.5 MHz bandwidth (80 V_{p-p}). The output swing and power efficiency of this amplifier is better than that in [GSH2013]. However, the required output swing is around 350 V_{p-p}, and the power efficiency still does not meet our requirement.

3.3.2 Existing Switched-mode Amplifiers

Hall and Cain [HT2006] proposed a 20 W, 1 MHz class D power amplifier for a 512-channel transducer array for transcutaneous ultrasound surgery. The efficiency of each amplifier is 90%. Figure 3.15 shows the schematic diagram of one channel.

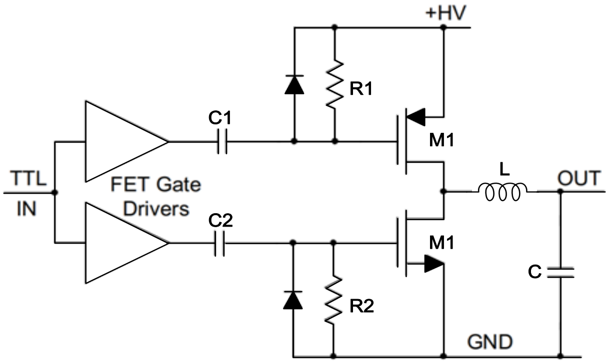


Fig.3.15 Schematic of the class D power amplifier with an inverter MOSFETs [HT2006].

In this amplifier, a PMOS and a NMOS are driven separately by their gate drivers. The on-off cycle of MOSFETs *M1* and *M2* will still be determined by the TTL signal. As a result, the output signal is a square wave. Capacitors *C1* and *C2* and resistor *R1* and *R2* are responsible for the shifts in the levels of the gate signal. The tuned filter inductor *L* and capacitor *C* filter out the higher harmonics in the output signal. The advantage of this design is that it is simple and very cost effective. However, the differential drain-to-source resistance of the NMOS and PMOS may cause some distortion in the output signal.

Cheng et al. [CHL2009] proposed a 41 kHz, 42 W single-switch class E amplifier combined with a flyback converter and a power-factor correction for ultrasonic cleaning applications. Figure 3.16 shows the schematic of this amplifier. The overall efficiency of the inverter is 90%. As mentioned earlier in the section that focused on the class E amplifier, the radio-frequency choke (RFC) is an inductor with very high inductance. This high inductance will cause compatibility problems with MRI. Therefore, this topology is not suitable for our application.

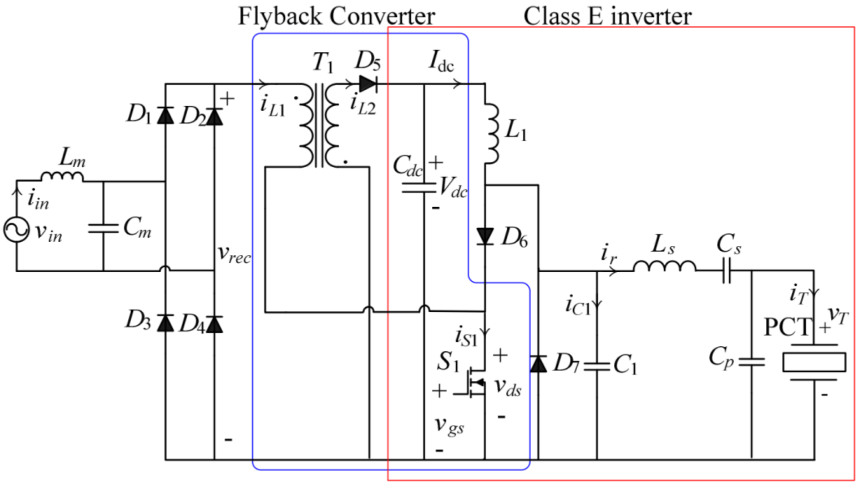


Fig.3.16 Schematic of class E amplifier combined with a flyback converter [CHL2009].

Lewis and Olbricht [LJGK2008] developed a 48-W, 1.54-MHz high-intensity ultrasound system for military, medical, and research applications. The efficiency of the amplifier is 99%, as reported by the authors. Its schematic is shown in Figure 3.17. In order to achieve maximum power transfer from a standard 50 Ω power supply to a 50 Ω transducer probe, the output impedance of the amplifier must be as low as possible. The authors reported that if 99% of the voltage from the power supply must be transferred to the load, the output impedance of the power amplifier should not be greater than 0.05 Ω. Their design was implemented using discrete components. Multiple power transistors are connected in parallel with each other to achieve very low output impedance.

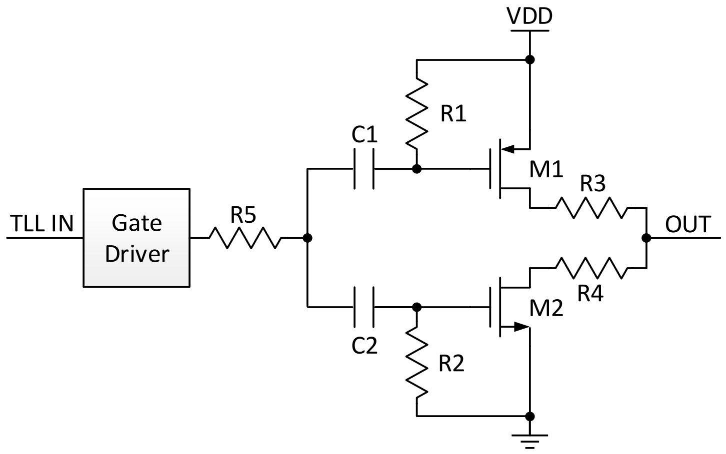


Fig.3.17 Schematic of Class D amplifier for military applications [LJGK2008].

An RC network handles level shifting for MOSFETs. The overall design is lightweight, small, and cost effective [LJGK2008]. Its topology is similar to that in [VAA2008] without a tuned LC harmonic filter connecting the amplifier output to the transducer. Because the driver is a class D amplifier, the output waveform of the amplifier is a square wave. Driving an ultrasound transducer with a square wave will cause the acoustic pressure field to contain harmonics; therefore, this solution cannot be directly adapted to HIFU applications.

Yang and Xu [YL2007] proposed a class D full-bridge amplifier for an Audio Beam system which is made with piezoelectric transducers. The switching frequency is 600 kHz. The schematic of its output stage is shown in Figure 3.18. Resistors *R1* and *R2* and an operational amplifier are part of the circuitry that cooperates with the gate driver IC to provide over currentprotection to the MOSFETs at the output stage. Inductors L_Q and L_P reduce the instantaneous current that goes to the transducer.

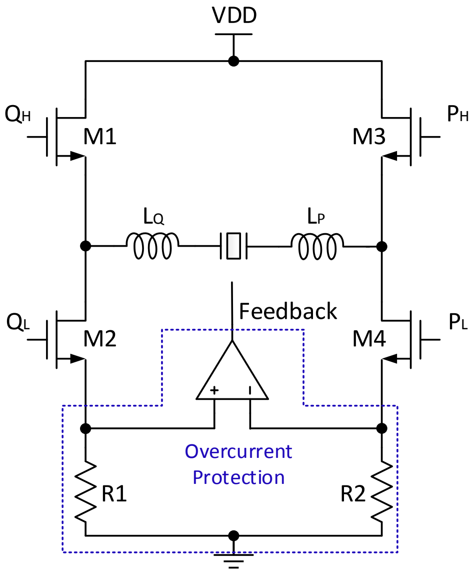


Fig.3.18 Schematic of the full-bridge class D amplifier for Audio Beam [YL2007].

The output stage of this amplifier consists of four transistors and two inductors. It is not economical to implement our design with this topology because four transistors occupy more space and inductors have to be mounted externally.

Low-intensity pulsed ultrasound (LIPUS) is an emerging technique that uses ultrasound for bone healing, dental-tissue formation, and tooth-root healing. Ang et al. [AWT2010] fabricated a 0.8 W, 1.5 MHz integrated amplifier chip for LIPUS applications. Its schematic is shown in Figure 3.19, and it was fabricated using a DALSA 0.8 μm HV CMOS process. The overall efficiency, including the pulse generator and amplifier, is 70%.

Depending on the impedance characteristics of the piezoelectric resonator, an ultrasound transducer usually requires a high voltage and high current to produce enough acoustic power for healing purposes. In order to mitigate the electrical requirements, an external tuned LC tuning network that matches the impedance of the transducer at resonance frequency is inserted in between the output of the amplifier and the transducer. This LC filter boosts the output voltage form 2.53 V peak to 7.6 V peak and eliminates higher harmonic contents from the output signals. A level shifter was used as the power output stage as shown in Figure 3.19. The generation of pulse modulated signals is realized using a digital block. In our case, an efficiency of 70% is not acceptable, and the use of NMOS and PMOS in the amplifier will cause distortion of the output signal, which is the same as in [HT2006] and [LJGK2008].

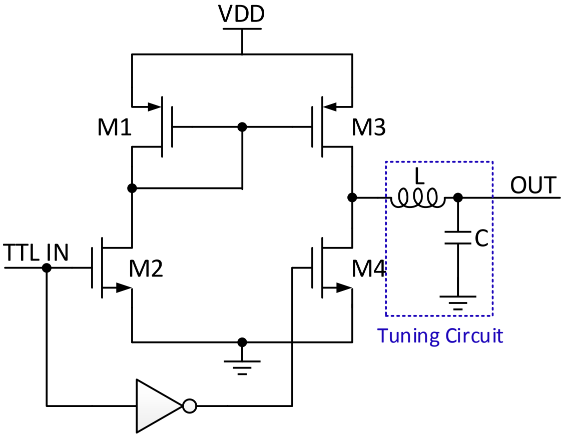


Fig.3.19 Schematic of the class D amplifier for LIPUS [AWT2010].

3.4 Comparison of Power Amplifiers

Based on the analysis in the former sections, a comparison of different existing amplifiers is shown in Table 3.1.

The typical power amplifier and the published works provide valuable information and techniques for designing piezoelectric power ampliers. But none of the existing power amplifier can perfectly match our application, such as elimination of huge inductors and transformers; high working frequency; high power efficiency; small circuit surface. Therefore, a half-bridge class D power amplifier is designed in section 3.5.

Table 3.1 Comparisions of existing power amplifiers for ultrasound applications

Ref	***Class***	***Output Waveform***	***Working Frequency***	***Power Efficiency***	***Output Power***	***Comments***
[TYC2008]	*Class AB*	*Sinusoidal*	*20kHz*	*32%*	*330W*	*Low efficiency, needs cooling facility*
[SK2015]	*Class AB*	*Sinusoidal*	*3MHz*	*44%*	*30W*	*Low efficiency, needs cooling facility*
[GSH2013]	*Class B*	*Sinusoidal*	*1~6MHz*	*57%*	*<1W*	*Acceptable efficiency, low output power*
[BD2014]	*Class B*	*Sinusoidal*	*3MHz*	*>60%*	*20W*	*Needs tuning network, acceptable efficiency, needs cooling facility*
[HT2006]	*Class D*	*Sinusoidal*	*1MHz*	*>90%*	*20W*	*Needs tuning network, needs MOSFETs with same R_{dson}*
[CHL2009]	*Class E*	*Sinusoidal*	*40kHz*	*93%*	*42W*	*Needs tuning network, needs high inductance choke*
[LJGK2008]	*ClassD*	*Square wave*	*1.5MHz*	*90%*	*48W*	*Square output waves needs MOSFETs with same R_{dson}*
[YL2007]	*ClassD*	*Sinusoidal*	*20~60kHz*	*91%*	*44W*	*Needs four transistors, needs tuning network*
[AWT2010]	*ClassD*	*Sinusoidal*	*1.5MHz*	*>70%*	*<1W*	*Needs tuning network needs MOSFETs with same R_{dson},*

3.5 Proposed Power Amplifier

The circuit design and analysis of the power amplifier used in our project is presented in this section. As discussed in previous sections, many basic power amplifiers can be used to drive ultrasound transducers. However, considering the power efficiency, the working frequency, and the compatibility with MRI, in this thesis, we present a half-bridge class D power amplifier with a square waveform input and a sinusoidal output. The diagram of the designed class D power amplifier is shown in Figure 3.20.

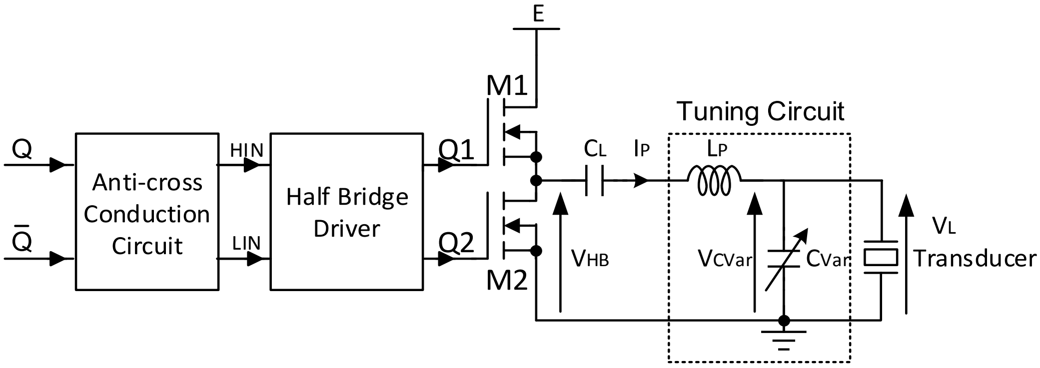


Fig.3.20 Diagram of the half-bridge class D power amplifier proposed in this thesis.

As can be seen from this figure, the amplifier consists of four parts: an anti-cross conduction circuit, a half-bridge MOSFET driver, two MOSFETs, and an automatic impedance-tuning circuit. This section focuses mainly on the amplifier parts. The principle of the proposed automatic impedance-tuning network and its circuit design will be given in chapters 4, 5 and 6.

3.5.1 Principle of the Proposed Class D Half-bridge Power Amplfier

As shown in Figure 3.20, the proposed amplifier consists of four parts. The half-bridge driver is used to generate a large current supply for the transistors. To achieve a high power efficiency, $R_{ds(on)}$ of the MOSFETs *M1* and *M2* are required to be as small as possible. Compared with PMOSs, NMOSs always have smaller $R_{ds(on)}$. Therefore, in the proposed amplifier, we use two NMOSs. Except the high power efficiency, high charging speed can also be achieved by using transistors with small $R_{ds(on)}$. And by using the same type NMOSs, the following equation can be realized,

$$R_{ds}(on)_{M1} = R_{ds}(on)_{M2} \tag{3.23}$$

Therefore the charging and discharging of the half-bridge is completely matched. NMOSs can also provide lower threshold voltage which makes it switch faster than PMOSs.

The transistors are driven by two out-of-phase signals, which means only one transistor turns on during the operation period. Because, the output of the half-bridge V_{HB} is a square wave signal. A LC tuning circuit is used to filter the harmonics of V_{HB}. After the tuning circuit, the ouput signal V_{CFix} is a sinusoidal signal.

As discussed in previous sections, the overlap of the transistors' control signal will cause energy loss. Therefore, we applied an anti-cross conduction circuit to solve the overlap problem.

The operation of the circuit can be described as follows:

The operation waveform of the proposed amplifier is illustrated in Figure 3.21. In order to simplify the analysis of the amplifier, we made several assumptions: $R_{ds(on)} = 0$; $I_P(t = 0) = 0$; $V_{CFix}(t = 0) = 0$. As discussed in chapter 2, the switched mode power amplifiers used for HIFU applications must have impedance tuning networks, so we introduce a static L-type impedance-tuning network to enable us to perform a complete analysis of the power amplifier. Details of the proposed automatic impedance tuning system and circuit design will be presented in the following chapters.

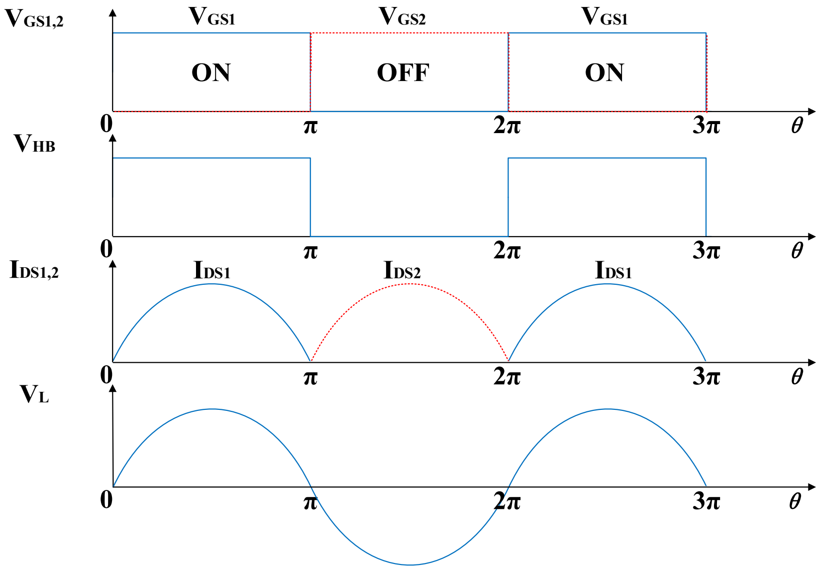


Fig.3.21 Operation waveform of the proposed half-bridge class D power amplifier.

The simplified schematic of the half-bridge class D power amplifier with a static impedance tuning network is illustrated in Figure 3.22.

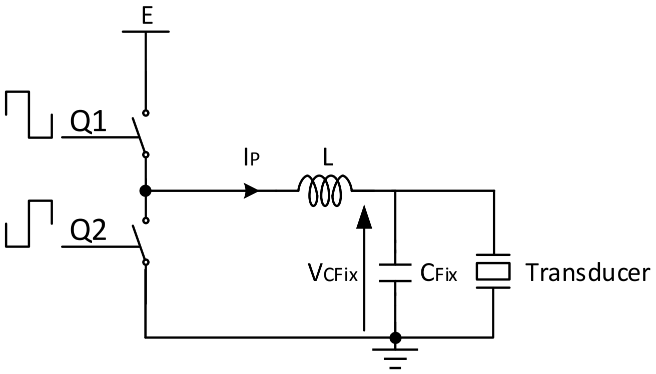


Fig.3.22 Simplified schematic of the proposed half-bridge class D power amplifier with a static impedance tuning network.

The operation analysis of the proposed half-bridge class D power amplifier is as follows.

According to Figure 3.22, the following equation can be obtained.

$$E = LC_{Fix}\frac{d^2V_{CFix}}{dt^2} + V_{CFix} \tag{3.24}$$

Then, Equations 3.25 and 3.26 can be obtained by solving Equation 3.24.

$$V_{CFix} = E + [V_{CFix}(t=0) - E]cos\omega t + I_P(t=0)\sqrt{\frac{L}{C_{Fix}}}sin\omega t \quad 3.25$$

$$I_P = I_P(t=0)cos\omega t + [E - V_{CFix}(t=0)]\sqrt{\frac{C_{Fix}}{L}}sin\omega t \quad 3.26$$

First operation cycle:

During the first half of the operation cycle ($0 \leq t < \pi/\omega$), *M1* turns on and *M2* turns off. The LC tuning network is charged by the current flow though *M1*. The equivalent circuit of the amplifier during this period is shown in Figure 3.23.

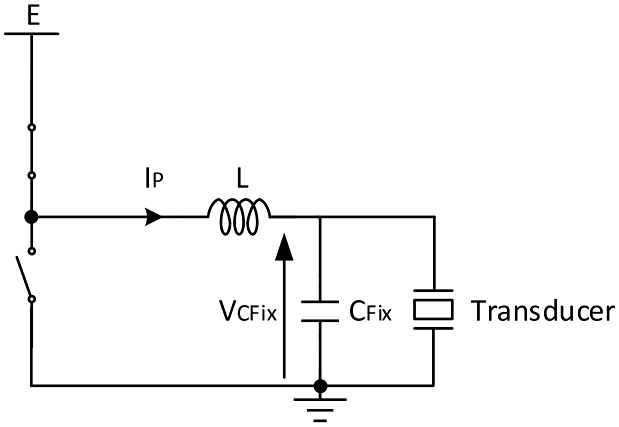


Fig.3.23 Equivalent circuit of the amplifier during the first operating cycle ($0 \leq t < \pi/\omega$).

Substitute $V_{CFix}(t=0)=0$, $I_P(t=0)=0$ into Equations 3.25 and 3.26, respectively. Then, $V_{CFix}(0 \leq t < \pi/\omega)$ and $I_P(0 \leq t < \pi/\omega)$ can be written as:

$$V_{CFix} = E - Ecos\omega t \quad 3.27$$

$$I_P = E\sqrt{\frac{C_{Fix}}{L}}sin\omega t \quad 3.28$$

Second operation cycle:

During the second half cycle ($\pi/\omega \leq t < 2\pi/\omega$), *M1* turns off and *M2* turns on. The LC tuning network is discharged. The equivalent circuit of the amplifier during this period is shown in Figure 3.24.

The initial condition of the amplifier is changed to

$$V_{CFix}\left(t=\frac{\pi}{\omega}\right)=E-Ecos\omega\left(\frac{\pi}{\omega}\right)=2E \qquad 3.29$$

$$I_P\left(t=\frac{\pi}{\omega}\right)=E\sqrt{\frac{C_{Fix}}{L}}sin\omega\left(\frac{\pi}{\omega}\right)=0 \qquad 3.30$$

Therefore, during this period, V_{CFix} $(\pi/\omega \leq t < 2\pi/\omega)$ and I_P $(\pi/\omega \leq t < 2\pi/\omega)$ can be defined as

$$V_{CFix}=2Ecos\omega t \qquad 3.31$$

$$I_P=-2E\sqrt{\frac{C_{Fix}}{L}}sin\omega t \qquad 3.32$$

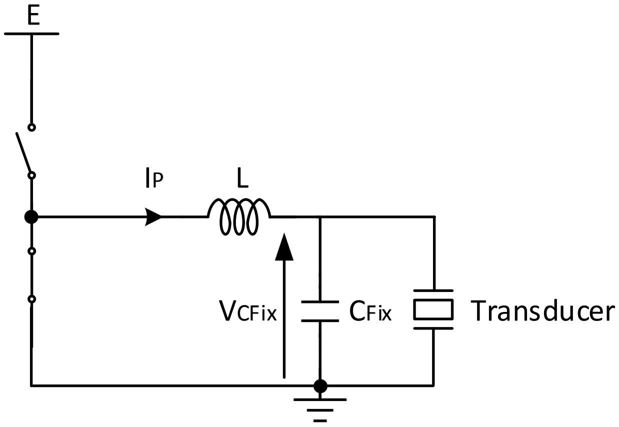


Fig.3.24 Equivalent circuit of the amplifier during the second cycle ($\pi/\omega \leq t < 2\pi/\omega$).

By performing the same calculation for the following half periods, we can obtain the waveforms of the voltage applied across C_{Fix} (V_{CFix}) and the current flows through L (I_P) as shown in Figure 3.25.

The following information can be obtained from the previous analysis.

1. V_{CFix} increases by $2E$ during each period.
2. After numbers of periods V_{CFix} reaches its maximum value. The energy supplied in each cycle is all dissipated in the resistance of the tuning circuit (characterized by its quality factor Q_{Load}), when V_{CFix} reaches its maximum value $Max(V_{CFix})$. The relationship between $Max(V_{CFix})$ and Q_{Load} is governed by

$$Max(V_{CFix}) = \frac{2E}{\pi} \cdot Q_{Load} \qquad 3.33$$

3. To maintain resonance, and to ensure that the transistors switch at zero current, two rules must be observed: The phase difference between V_{HB} and I_P equals zero, and the phase difference between V_{CFix} and V_{HB} is $\pi/2$, only possible with suitable tuning network.

The energy losses are unavoidable because the actual value of $R_{ds(on)}$ is not zero. These energy losses can be reduced by using NMOSs, which have small $R_{ds(on)}$. The most important losses are caused by the time of commutations of the transistors if these overlap. Another possible reason for energy losses is the overlap between the switching times of the two MOSFETs. Moreover, a short circuit, which is caused by the overlap, will cause circuit damage. Therefore, during the working period, we should ensure that only one of the transistors is open at a given time. In other words, there must be a dead time between two control signals ($Q1$, $Q2$).

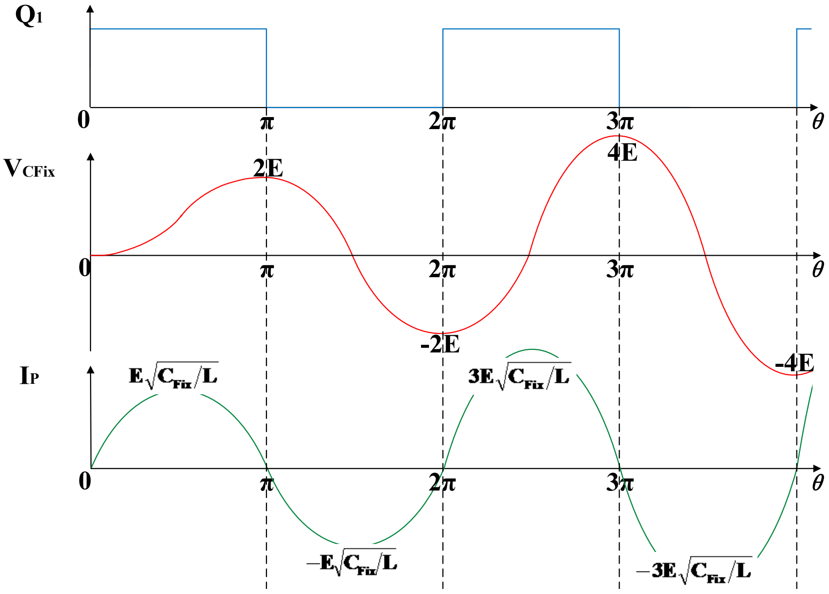


Fig.3.25 Chronogram of output voltage of half-bridge (V_{HB}), voltage applied across C_{Fix} (V_{CFix}) and the current flows through L (I_P).

3.5.2 Parameters of the Ultrasonic Transducer

Based on the datasheet that is provided by the foundry and the modeling of the ultrasonic transducer in chapter 2, the parameters of the ultrasonic transducer are presented in Table 3.2.

Table 3.2 Parameters of the ultrasonic transducer used in this thesis.

Working Frequency	*Rated Power*	R_{SLoad}	X_{SLoad}
1.25MHz	*3W*	*36.65 Ω*	*-308.2 Ω*

Figure 3.26 shows the series impedance of the ultrasonic transducer at its working frequency. R_{SLoad} is the resistance and X_{SLoad} is the reactance. Therefore, the equivalent circuit of the ultrasonic transducer at its working frequency can be described as Figure 3.27.

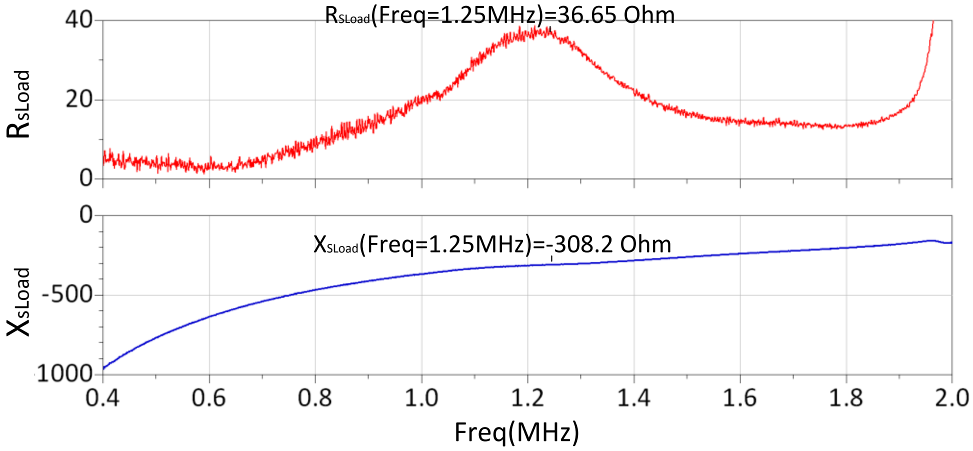


Fig.3.26 Measurements of the series impedance of the ultrasonic transducer.

Therefore, the quality factor of the transducer is described as

$$Q_{Piez} = \left|\frac{X_{SLoad}}{R_{SLoad}}\right| = \frac{308.2}{36.65} \simeq 8.41 \qquad 3.34$$

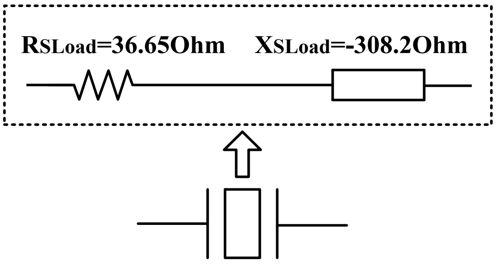


Fig.3.27 Series equivalent circuit of the ultrasonic transducer at its working frequency.

3.5.3 Calculation of the Circuit Parameters

As shown in previous section, the series impedance of the transducer Z_S at its working frequency can be described as

$$Z_S = R_s + jX_s = 36.65 - 308.2j \qquad 3.35$$

Therefore, the parallel impedance of the transducer Z_P is described by

$$Z_P = R_P + jX_P \qquad 3.36$$

$$R_P = R_s\left(1 + {Q_{Piez}}^2\right) \simeq 2628.4\ \Omega \qquad 3.37$$

$$X_P = -X_s\left(1 + 1/{Q_{Piez}}^2\right) \simeq 312.6\,\Omega \qquad 3.38$$

Then, the parallel equivalent circuit of the transducer at its working frequency can be obtained as shown in Figure 3.28

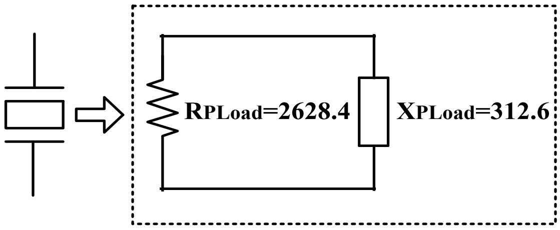


Fig.3.28 Parallel equivalent circuit of the ultrasonic transducer at its working frequency.

As the rated power of the transducer is 3W, so the required voltage supply of the transducer can be obtained as follows

$$V_{supply(RMS)} = \sqrt{P_{out} \cdot R_{PLoad}} = \sqrt{3 \times 2628.4} \simeq 88.8V_{RMS} \qquad 3.39$$

$$V_{supply(peak)} = \sqrt{2}V_{supply(RMS)} \simeq 125.6V \qquad 3.40$$

where $V_{supply(RMS)}$ is the rms supply voltage and $V_{supply(peak)}$ is the peak-to-peak supply voltage.

The working frequency of the transducer is 1.25 MHz, and from Figure 3.28, we can see that the equivalent capacitance C_{Piez} of the transducer can be described by,

$$C_{Piez} = \frac{1}{2\pi f_S X_P} \simeq 407.3\,pF \qquad 3.41$$

Based on the analysis in section 2.3, we know that the reactance of the inductor L

and the susceptance of the capacitor C_{Fix} in the static L-type tuning network can be calculated by the following equations.

$$B_{CFix} = \frac{X_{Piez} + \sqrt{R_{Piez}/Z_O}\sqrt{R_{Piez}^2 + X_{Piez}^2 - Z_O R_{Piez}}}{R_{Piez}^2 + X_{Piez}^2} \tag{3.42}$$

$$X_L = \frac{1}{B_{CFix}} + \frac{X_{Piez} Z_O}{R_{Piez}} - \frac{Z_O}{B_{CFix} R_{Piez}} \tag{3.43}$$

where $X_{Piez}=X_{SLoad}$ and $R_{Piez}=R_{SLoad}$, and Z_O is the output impedance of the power amplifier which equals the value of R_{dson} of the power transistor. In this thesis, we choose NMOS transistors with R_{dson} less than 0.04 Ω to reduce the energy losses of the power amplifier. By solving Equations 3.42 and 3.43,

$$B_{CFix} \simeq 0.091 \tag{3.44}$$

$$X_L \simeq 10.61 \tag{3.45}$$

Then, we can obtain the values of the inductor and capacitor of the tuning network.

$$C_{Fix} = \frac{B_{Fix}}{2\pi f} \simeq 11.6\, nF \tag{3.46}$$

$$L = \frac{X_L}{2\pi f} \simeq 1.35\, \mu H \tag{3.47}$$

The inductance and resistance of L at 1.25 MHz were chosen to be 1.35 μH and 0.183 Ω, respectively, and it is an aircore inductor. It was developed in our laboratory. The resistance of the inductor is much lower than the resistance of the transducer which can achieve a high power efficiency.

The resonance frequency f_{LC} of the LC circuit can be described by

$$f_{LC} = \frac{1}{2\pi\sqrt{L(C_{Fix} + C_{Piez})}} \simeq 1.25 MHz = f_{working} \tag{3.48}$$

Then, we obtain the quality factor Q_{Load} of the LC tuning network using

$$Q_{Load} = \frac{2\pi f_{working} L}{R_L + Z_O + 1/\left(R_{Piez}\left(2\pi f_{working} C_{\mathrm{Piez}}\right)^2\right)} \simeq 39.46 \tag{3.49}$$

By substituting $V_{supply(peak)}$ and Q_{Load} into Equation 3.33, we can obtain the value of E.

$$E = \frac{\pi \cdot V_{supply(peak)}}{2Q_{Load}} = \frac{125.6 \times \pi}{2 \times 39.46} \simeq 5 \tag{3.50}$$

3.5.4 Circuit Design

We implemented the power amplifier using a printed circuit board (PCB) and discrete devices. The software used to design the power amplifier is *Altium Designer Release 10*. The details of the circuit and PCB will be presented in this section.

Based on the circuit calculation, we designed the schematic of the proposed power amplifier. Figure 3.29 shows the schematic of the proposed class D power amplifier with a static L-type tuning network.

The half-bridge is composed of two NMOSs (SI4178). The value of $R_{DSon}(max)$ for the chosen MOSFET is less than 0.033 Ω when $V_{GS} = 4.5$V [Si4178DY], which meets our requirement. Further, the rated power of SI4178 is 5 W, which exceeds the rated power of the transducer.

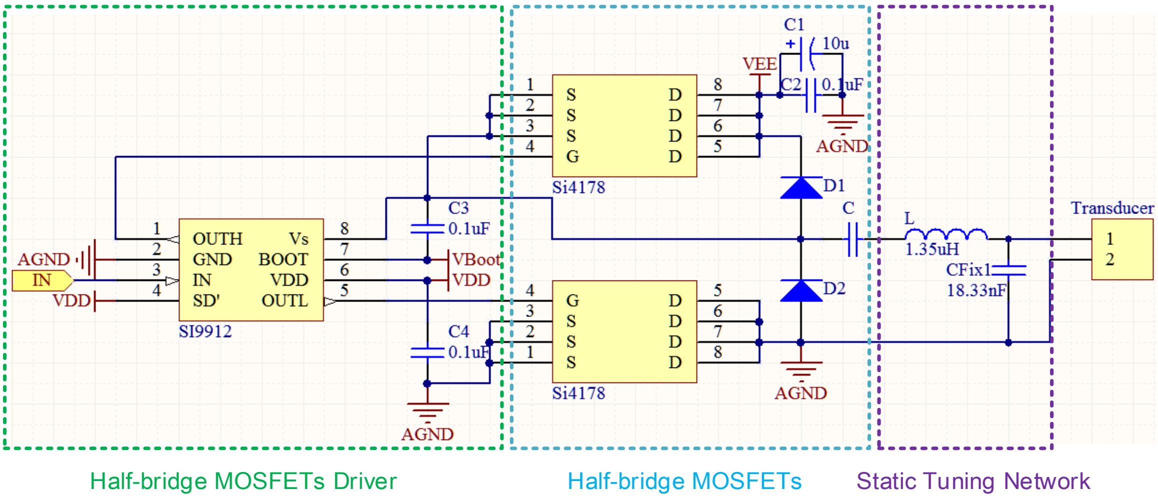


Fig.3.29 Schematic of the proposed class D power amplifier with a static L-type tuning network.

The gate-source threshold voltage $V_{GS(th)}$ and input capacitor C_{iss} of the MOSFET are 2.8 V and 405 pF, respectively, according to the datasheet. Because of the input capacitor C_{iss}, we require a MOSFET driver circuit that is capable of providing sufficient current to the transistors. In this thesis, we use the half-bridge MOSFET driver SI9912 to drive the transistors. The switching frequency of this driver can reach

1.25 MHz, and the drive current I_{Drive} can reach 1 A [Si9912]. Therefore, the switching time of the transistors t_{Switch}, which is realized by using this driver, can be calculated using

$$t_{Switch} = C_{iss}\frac{V_{GS(th)}}{I_{Drive}} = 1.134ns \tag{3.51}$$

where t_{Switch} is much less than half of the period of the input signal (0.5 µs). In addition, SI9912 can offer a 25 ns dead time between the gate-control signals OUT_H and OUT_L [Si9912]. The dead time is larger than the switching time of the MOSFETs. Therefore, there is no cross-conduction problem, which means that the MOSFETs of the half-bridge will never conduct at the same time.

3.5.5 Printed Circuit Board Design

The designed printed circuit board of the power amplifier is illustrated in the area bounded by the red dotted line in Figure 3.30. This board is a 1.6 mm double-side fiberglass PCB, and the copper foil on the printed circuit board is chosen to be 105 µm. The area of the proposed power amplifier is only 10 cm^2.

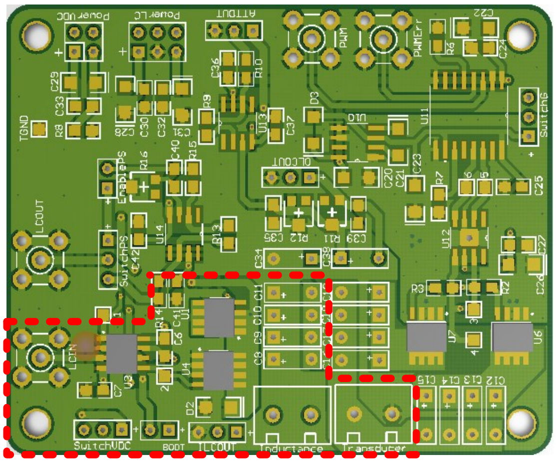


Fig.3.30 Designed printed circuit board of the proposed class D power amplifier.

3.6 Prototype and Test Results of Power Amplifier

Figure 3.31 shows a prototype of the proposed power amplifier. The power amplifier is located in the area bounded by the dotted line. We tested and verified the operation of the proposed amplifier, and the test results are as follows. The test results of the gate-control signal OUT_H and OUT_L generated by the half-bridge driver is illustrated in Figure 3.32.

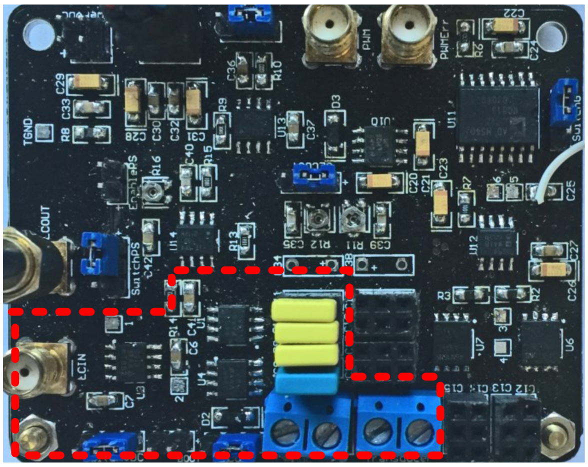


Fig.3.31 Prototype of the proposed class D power amplifier.

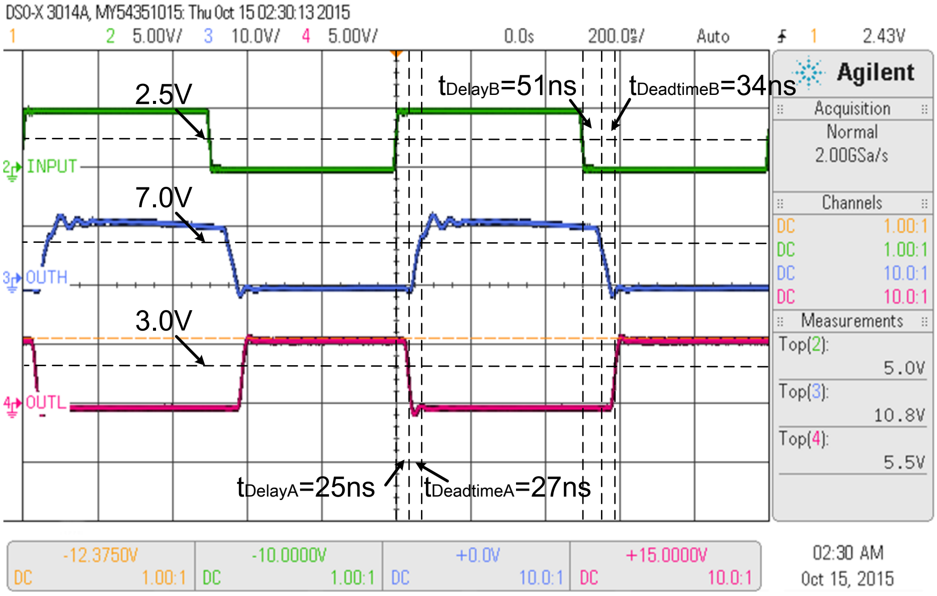


Fig.3.32 Chronograms of the gate-control signal OUT_H and OUT_L generated by the half-bridge driver with a 1.25 MHz, 5 V input signal.

Ch2 (*green*): Voltage of the input signal of the half-bridge driver V_{IN}: 5V/div.

Ch3 (*blue*): Voltage of the gate-control signal OUT_H: 10V/div.

Ch4 (*pink*): Voltage of the gate-control signal OUT_L: 5V/div.

$V_{GS(th)}$ of the MOSFETs is 3 V. Therefore, as observed in this figure, the dead times between OUT_H and OUT_L are 27 ns and 34 ns, respectively. The maximum switching time of the transistor is 20 ns, which is less than the measured dead times. Therefore, we can deduce that the cross conduction of the half-bridge was eliminated, and the delays between the input signal and OUT_H, OUT_L are 25 ns and 51 ns, respectively.

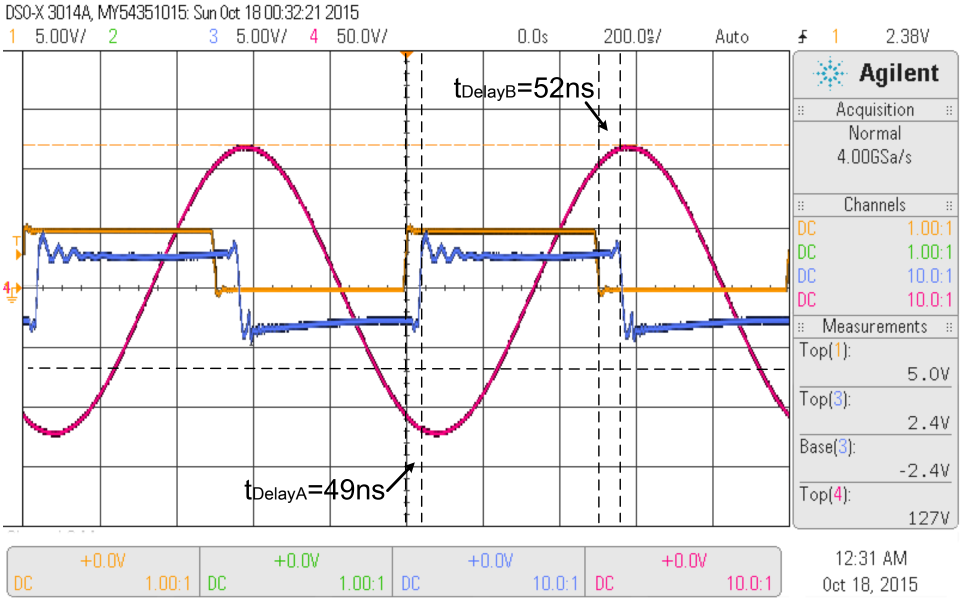


Fig.3.33 Chronograms of the half-bridge output signal V_{HB} and the output of the power amplifier with a 1.25 MHz, 5V input signal.

Ch1 (*orange*): Voltage of the input signal of the half-bridge circuit V_{IN}: 5V/div.

Ch3 (*blue*): Voltage of the output signal of the half-bridge circuit V_{HB}: 10V/div.

Ch4 (*pink*): Voltage of the output signal of the power amplifier V_{OUT}: 50V/div.

The chronograms of the half-bridge output signal V_{HB} and the output V_{OUT} of the power amplifier are demonstrated in Figure 3.33. The delays between the input signal and V_{OUT} are 49 ns at the rising edge and 52 ns at the falling edge. The maximum voltage of V_{OUT} is 127 V. The measured power efficiency of the proposed class D power amplifier is described by

$$\eta_{Eff} = \frac{P_{OUT}}{P_{IN}} = \frac{P_{Piez}}{P_{IN}} = \frac{P_{Piez}}{V_{DC} \cdot I_{DC}} = \frac{3W}{5V \times 726mA} \simeq 82.6\% \tag{3.52}$$

3.7 Summary of the Proposed Half-bridge Class D Amplifier

In this section a half-bridge class D power amplifier for our application is presented. The performance of the proposed power amplifier is shown in Table 3.3.

The power supply of the proposed amplifier is 5V. It can offer 3W output power with working frequency of 1.25MHz. And the output waveform of the amplifier is sinusoidal signal that meets our requirement. In the circuit, there is no bulky magnetic compont thanks to the L-type tuningnetwork and small value air-core inductor. Therefore, it is compatibility with MRI. The surface of the circuit is only 10cm^2. Moreover, the power efficiency of the presented amplifier is 82.6% which is very suitable for our application. The circuit is realized by using printed circuit board and discrete component that makes it very cheap and easy to fabricate. In other words, it has a very good cost performance ratio.

Table 3.3 Performance of the proposed power amplifier.

Power Supply	***Transducer***
Power Supply	*5V*
Working Frequency	*1.25MHz*
Output Power	*3W*
Ouput Waveform	*Sinusoidal*
Power Efficiency	*82.6%*
Total Price	*Less than 10€*

Chapter 4

Proposed Impedance Auto-tuning

4.1 Introduction

In order to create a focused ultrasound, the HIFU system uses different numbers of piezoelectric elements, which have the property of mechanical deformation as a function of the supply voltage. To deal with all types of tumors, it is necessary to move the focus point within the space. By using a transducer array consisting of many small independent transducers (mono-elements), it is possible to modify the spatial position of the focus point by changing the phases of the supply voltage for each element.

However, the electrical impedances of piezoelectric elements are complex, while the output impedance of power amplifiers is purely resistive. If we connect power amplifiers directly to the transducers, the reflected power will cause a defocusing of the ultrasound, increasing the temperature of the transducers or even causing unrecoverable damage to the transducer. Therefore, the impedances of the transducers must be tuned to make them purely resistive. Moreover, temperature variations, ageing, and different working mediums can cause changes of the impedance, and this impedance variation makes static impedance-tuning networks unsuitable for our application. In addition, as discussed in chapter 2, most existing variable-impedance-tuning networks require an MCU or computer to achieve automatic tuning. The use of an MCU or computer leads to a complicated and expensive tuning system. For saturable reactor auto-tuning network, the use of a bulky magnetic component cannot satisfy both the weight and miniaturization constraints of HIFU systems, and furthermore, they cannot comply with the MRI compatibility regulations.

In this chapter, a novel automatic impedance tuning system without using of MCU or computer and bulky magnetic components is presented to solve the impedance tuning and impedance drifting problems at the same time. The structure of this chapter is as follows: Section 4.2 presents the influences of the temperature and technological dispersions on the impedance of the chosen transducer. Besides, the impact of impedance variation on the power efficiency of the ultrasonic generator is also presented in this section. A recall of existing auto-tuning techniques is illustrated in section 4.3. In Section 4.4, we describe the principle of this novel automatic impedance-tuning system. Section 4.5 gives out the diagram of the proposed realization and its working operation. At last, the stability analysis of the proposed auto-tuning system will be given out in Section 4.5.

4.2 Impedance Variation of the Transducer

4.2.1 Impact of Temperature Drifting on Transducer's Impedance

The impedance variation of the transducer is caused mainly by fluctuations in the temperature. In this section the relationship between the temperature variation and the imaginary impedance of the transducer is studied. The schematic of the measurement circuit is presented in Figure 4.1.

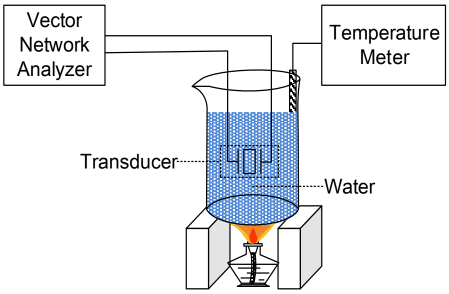


Fig.4.1 Schematic of the impedance-measurement circuit.

In practice, during clinical treatment, the use of a transducer phased array at full power can cause a significant temperature rise, which, according to the experimental results, will lead to a significant change in the transducers' impedance. The measured imaginary impedances of the chosen transducers are shown in Figure 4.2, with temperatures ranging from 25ºC to 55ºC. As can be seen from this figure, the variation of the imaginary impedance of the transducer is less than 5%.

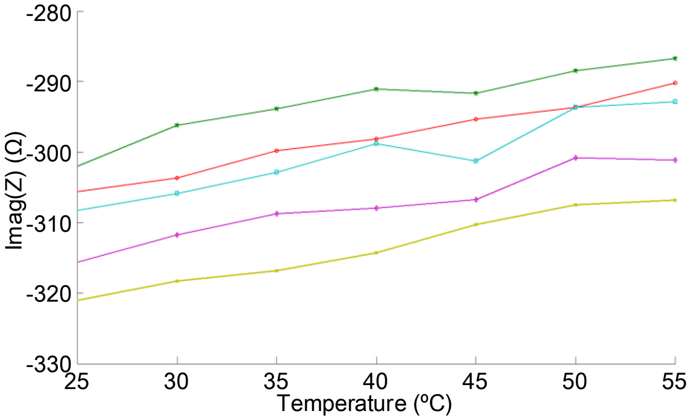


Fig.4.2 Measured curves of the imaginary part of the transducer's impedance versus temperature.

Figure 4.3 shows the simulation results of the tuned transducer obtained using the static-tuning network presented in Chapter 3. From this figure, we can clearly see that the static-tuning network cannot solve the problem of the impedance drift of the transducer that is caused by the increased temperature. The imaginary part of the impedance remains, and the output power does not reach its maximum value.

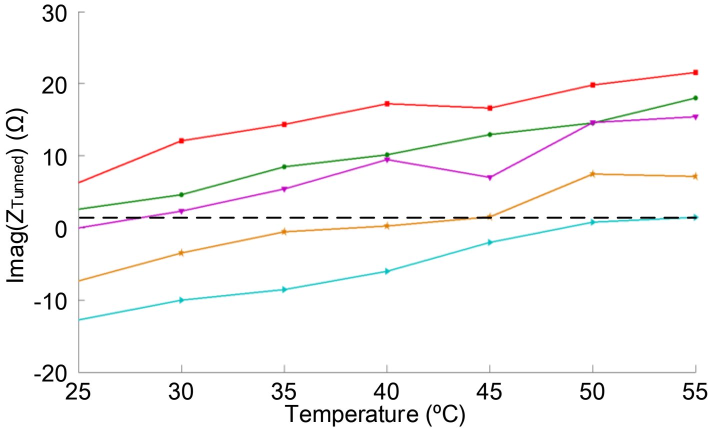


Fig.4.3 Imaginary impedances of transducers that are tuned by a static-tuning network.

4.2.2 Impact of Technological Dispersions on Transducer's Impedance

The impedance of the transducer is also influenced by the technological dispersions during the manufacturing process. Imaginary impedances of 256 different mono-elements in the phased-array used in our application are shown in Figure 4.4. These impedances are measured at 25 ºC. The imaginary impedances of these transducers is ranging from -346.5 ($Imag(Z)_{min}$) to -267.8 Ω ($Imag(Z)_{max}$).

As can be known from the measured data, the average imaginary impedance $Imag(Z)_{average}$ is equal to -308 Ω, and the variation of the imaginary impedance caused by the technological dispersion is obtain by

$$Var\big(Imag(Z)\big)_{Tech} = \left|\frac{Imag(Z)_{max}-Imag(Z)_{min}}{Imag(Z)_{average}}\right| \cdot 100\%$$

$$= \left|\frac{-267.8+346.5}{-308}\right| * 100\% \simeq 25\% \qquad 4.1$$

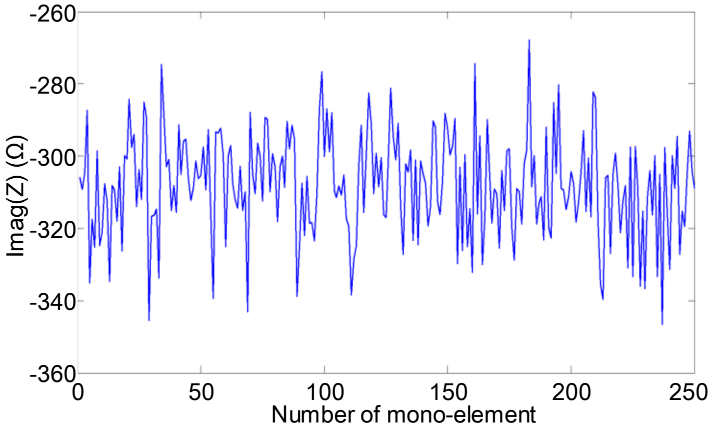


Fig.4.4 Imaginary impedances of different mono-elements in the phased-array used in this thesis.

Figure 4.5 shows the histogram of these different imaginary impedances. The imaginary impedances of these mono-elements are mainly between -310 and -300 Ω.

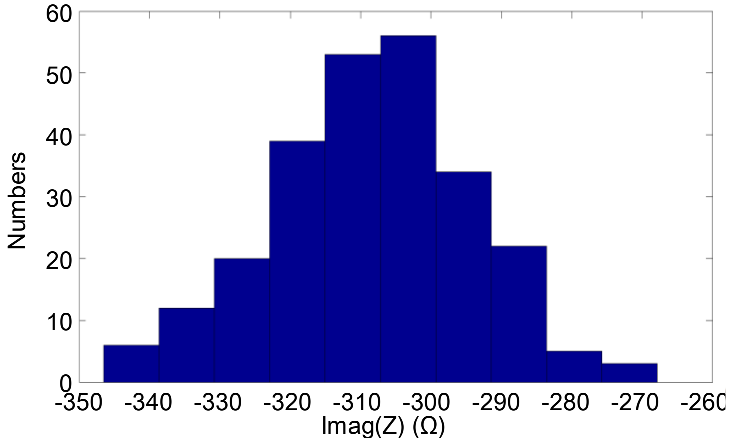


Fig.4.5 Histogram of the measured imaginary impedances.

4.2.3 Impact of Impedance variation on Power Efficiency

In sections 4.2.1 and 4.2.2, we obtained that the variations of imaginary impedance caused by temperature drifting and technological dispersion are 5% and 25%, respectively. Therefore, if both cases happen in the same time, the maximum variation of the imaginary impedance in the worst case can reach 30%.

According to Equations 2.24 and 3.52, the power efficiency of the power amplifier (η) with a static tuning network can be rewritten as,

$$\eta = cos(\varphi) \cdot \eta_{Eff} = cos(\varphi) \cdot 82.6\% \qquad 4.2$$

where η_{Eff} is the power efficiency of the power amplifier without impedance drifting, and $cos(\varphi)$ is the power factor. Based on Equation 2.25, we can know that

$$\varphi = tan^{-1}(B_{Tunned}/G_{Piez}) \qquad 4.3$$

where B_{Tunned} is the tuned susceptance of the transducer, and G_{Piez} is the conductance of the transducer.

We define B_{TN} as the susceptance that can be compensated by the static tuning network. B_{Piez} is the suspectance of the transducer, and ΔB_{Piez} is the variable suspectance of the transducer. It can be known that $B_{Tunned} = \Delta B_{Piez} + B_{Piez} + B_{TN}$. We know that $\Delta B_{Piez} + B_{Piez} = Imag[(Z_{Piez} + \Delta Z_{Piez})^{-1}]$. By substituting these two equations and Equation 4.3 into Equation 4.2, we can describe the relationship between the power efficiency of the power amplifier with a static tuning network and the variation of the imaginary impedance of the transducer by

$$\eta = 0.826 \cdot cos\left(tan^{-1}\left(\frac{Imag[(Z_{Piez}+\Delta Z_{Piez})^{-1}]-B_{TN}}{G_{Piez}}\right)\right) \quad 4.4$$

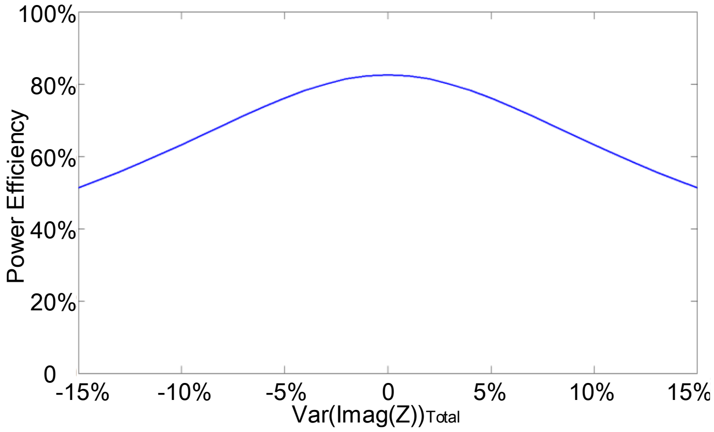


Fig.4.6 Power efficiency curve of the power amplifier with a static tuning network

The power efficiency curves of the power amplifier with a static tuning network is presented in Figure 4.6. As it can be seen from this figure, the impedance drifting of the transducer leads to a great reducing of the power efficiency, if we use a static tuning network. Thus, a novel auto-tuning network is presented to solve this problems in the following sections.

4.3 Recall of Existing Auto-tuning Techniques

In this section, we recall the existing auto-tuning techniques used for ultrasound therapy. A summary about these different auto-tuning techniques is also given out in this section.

Hui Xu, Erzhen Gao, and Q.Y.MA [XH2001] present a variable electrical tuning network consisting of a fixed inductor with a variable capacitor. Although, this paper is mainly focused on the piezoelectric oscillator, fundamentally this technique employed to shift the driven resonance of a piezoelectric element remains the same. It can automatically tune the imaginary impedance of the transducer over a range of 34% by varying the capacitance of the driving circuit.

The variable capacitor used in this paper is realized by using a movable metal plate and a fixed plate. When we apply different control voltages to the capacitor, the movable part changes its position accordingly, the value of the capacitance between the fixed and the movable parts also changes. However, it is difficult to achieve a high accuracy moving of the movable plate, which means the accuracy of this capacitor is low. Therefore, the accuracy of this tuning circuit is badly limited.

A switched-capacitor based auto-tuning network is presented by Si et al. [SP2005]. This tuning network was introduced for the bio-implanted application. Figure 4.7 shows the simplified configuration of this tuning system. The test results showed a power efficiency of 80% at 1 cm gap demonstrating that the proposed method is very effective in stabilizing the operating frequency, while maintaining the zero voltage switching operation. However, the working frequency of the tuning network presented in this paper is less than 100 kHz, which is much lower than the working frequency of our application (1.25 MHz). Besides, the transfer function of this tuning network is strongly non-linear, and this non-linear characteristic may lead to a stability problem.

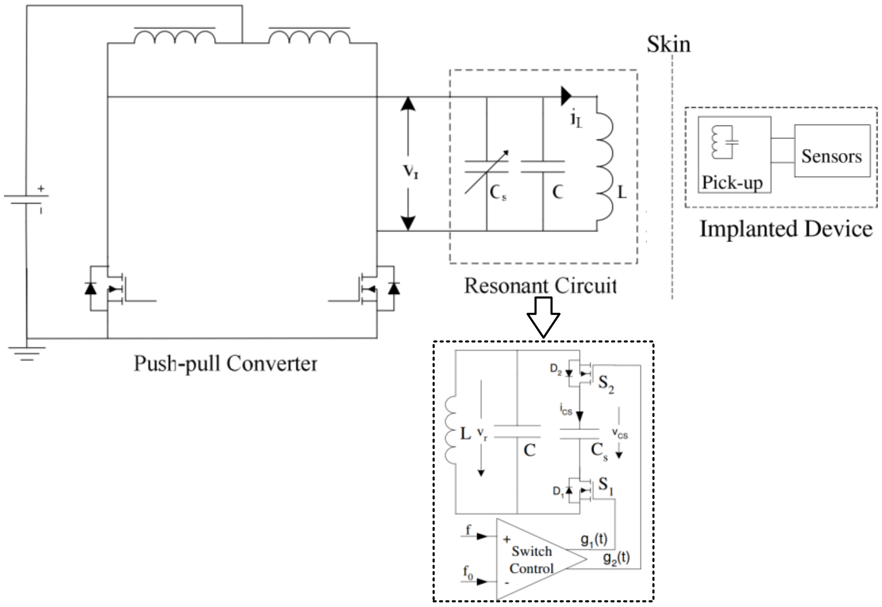


Fig.4.7 Simplified configuration of the auto-tuning network proposed in [SP2005].

P. Lourenc¸o de Oliveira, F. Rodes, et al presentes an adjustable impedance tuner specially designed for high intensity focused ultrasound phased-array transducers in [DOPL2009]. It has been designed around digital variable reactances made with binary switched capacitance ladders. Diagram of this adjustable impedance tuner is illustrated in Figure 4.8.

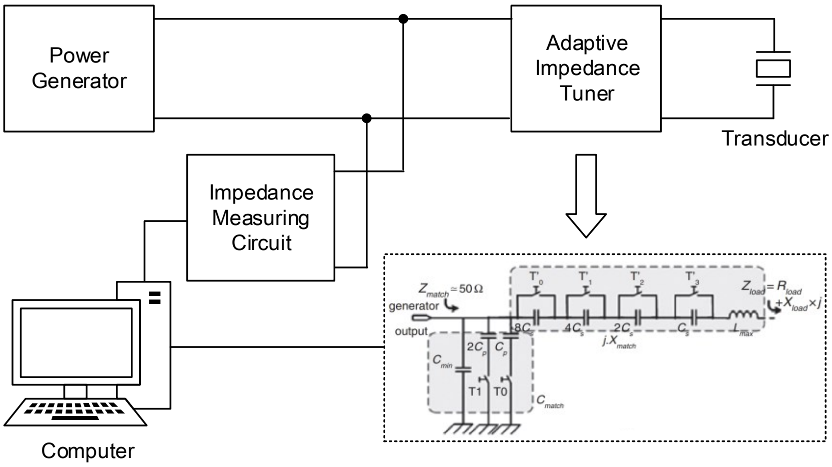


Fig.4.8 Diagram of the adjustable impedance tuner for HIFU applications [DOPL2009].

Compared with the static tuning method, this adjustable impedance tuner can offer an improvement of 1.7 dB is made in the mean power losses, and an improvement of 5.2 dB is made by considering the highest reflection. It solves the imaginary impedance and the real impedance drifting at the same time. However, this adjustable tuner needs a real-time impedance measuring circuit and a computer to generate the switch control signal. The large surface of the circuit and expensive equipments lead to a very low cost performance ratio.

An adaptive tuning network for class D amplifier is introduced by Mohamed Gamal EI Din, et. al [EDMG2010]. Combined with the proposed adaptive tuning network, the class-D amplifier can achieve an efficiency improvement of more than 25% over an 8 dB output dynamic range in comparison with a similar amplifier with fixed matching. Although, this tuning network is compatible with our application, the complex structure makes it hard to implement and manufacture. In our application, there are 256 mono-transducers in the phased array, therefore, this tuning network is also not suitable for our project.

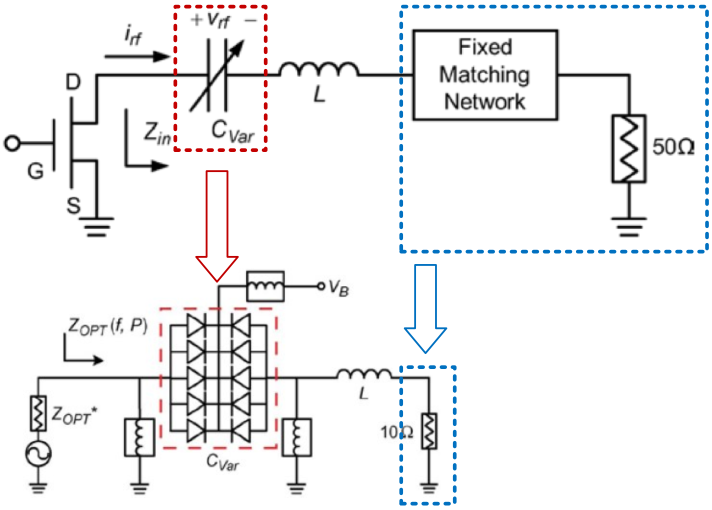


Fig.4.9 Simplified schematic of the adjustable impedance tuning network presented in [CK2012].

Kenle Chen, et al [CK2012] introduce an auto-tuning network for GaN power amplifier. It is a varactor-based tuning network which is controlled by a DSP module. The simplified schematic of the tuning network is shown in Figure 4.9. The power amplifier with this tuning network achieves a substantial operating frequency band from 1–1.9 GHz, with 10 W peak power, and 64%–79% peak power efficiency. However, the use of varactor diodes limits the maximum output voltage of the system. In our project, the required output voltage is 126V, which greatly exceeds the break down voltage of the varactor diodes. And the use of DSP module makes this circuit low cost performance ratio.

In the master thesis of Hayden N. Radke [RHN2013], he presents an auto-tuning system for piezoelectric transducer. This tuning system consists of switching inductor network and a control loop. Flow chart of the tuning system is demonstrated in Figure 4.10.

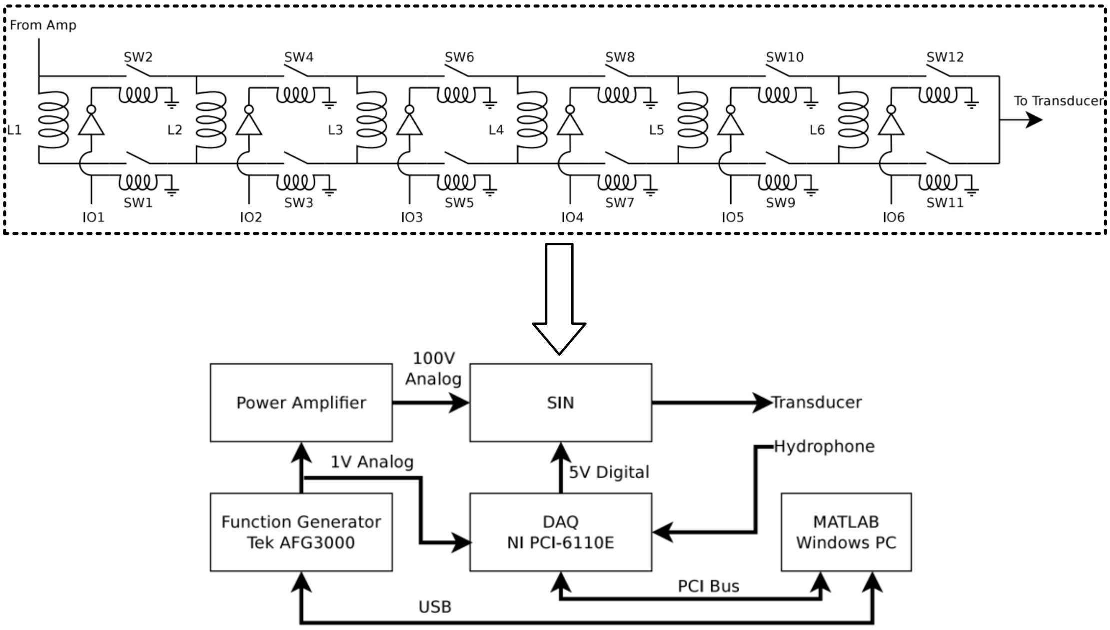


Fig.4.10 Flow chart of the auto-tuning network presented in [RHN2013].

The working frequency of this tuning network is limited by the using of relays in the switching inductor network. And a computer and MCU are needed in this tunning network. Therefore, it can not meet our requirement.

F. J. Arnold, et al. [AFJ2015] develop a circuit for a laboratory bench. The operation of this circuit is based on detection of magnitude of current in the transducer. A microcontroller and Labview are used to obtain the impedance of the transducer based on the detected current. The deviations from original impedance are corrected by using a feedback network that evaluates amplitude of impedance. A class D MOSFET amplifier is used for exciting the transducer. Also, a microcontroller system controls the feedback network. Experiments with variation of mechanical loads have shown the effectiveness of the system. The main limitation of this method is the using of bulky magnetic component in the detection circuit. This method is not compatible with MRI system.

Summary of frequency, improved power efficiency, and tuning range for the existing auto-tuning networks are shown in Table 4.1.

Table 4.1 Summary of existing auto-tuning networks suitable for ultrasonic transducer.

Ref	***Working Frequency***	***Improvement of the Power Efficiency***	***Tuning Range***	***Comments***
[XH2001]	*17.7~20MHz*	-	*34%*	*Low accuracy*
[SP2005]	*69.5~-87kHz*	-	*20%*	*Low working frequency*
[DOPL2009]	*1.5MHz*	-	*28.9%*	*Needs Computer and external impedance measuring circuit*
[EDMG2010]	*1GHz*	*25%*	-	*Complex structure Hard to implement and manufacture.*
[CK2012]	*1~1.9GHz*	*15%*	-	*Maximum output voltage is limited by using of varactor diodes.* *Needs DSP module*
[RHN2013]	*15~20kHz*	-	-	*Needs computer and external impedance measuring circuit*
[AFJ2015]	*28~30kHz*	-	-	*Needs bulky magnetic components in the impedance detecting circuit.* *Needs MCU*

The published auto-tuning circuit provide valuable information for designing impedance auto-tuning system. However, none of the existing auto-tuning circuit can perfectly match our application, such as, high cost performance ratio, MRI compatibility, high tuning accuracy, etc. A novel auto-tuning network is proposed in this thesis to solve these problems, and the principle of the proposed auto-tuning network is presented in section 4.4.

4.4 Proposed Auto-tuning Network

Based on the review of the existing auto-tuning networks, a novel auto-tuning network for imaginary impedance cancelling of the transducer is proposed in this section. The proposed auto-tuning network is no need of MCU or computer and bulky magnetic components. Besides, this auto-tuning network achieves very high accuracy and proper working frequency.

4.4.1 Principle of the Proposed Auto-tuning Network

The simplified circuit of the proposed auto-tuning network, which is named as synchronous-switched capacitor, is presented in Figure 4.11.

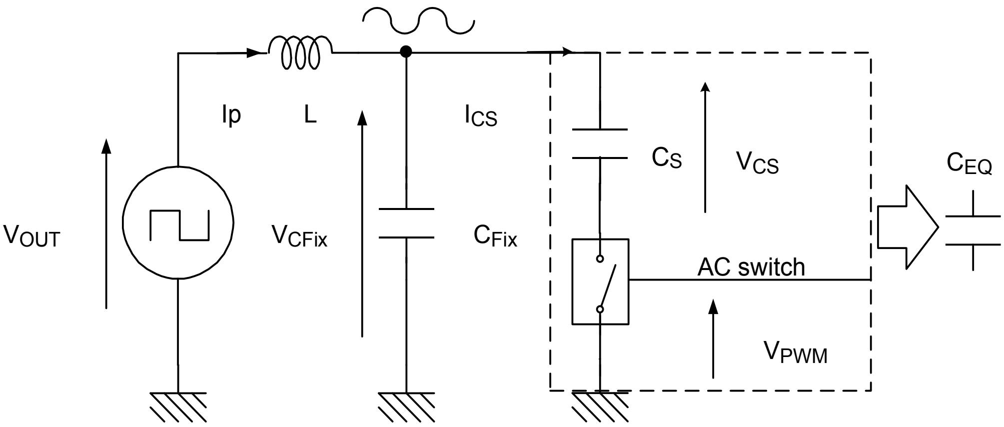


Fig.4.11 Simplified circuit of the proposed synchronous switched capacitor.

The proposed auto-tuning technique is a variable-capacitor-based approach. But instead of using a varactor, which is voltage-limited as mentioned previously, a capacitor with a fixed value Cs is used and it is added in parallel with the fixed capacitor used in the static resonant circuit, as shown in Fig. 4.11. The connection of the added capacitor Cs to the circuit is synchronoursly controlled by a signal that has the same frequency as the input signal of the circuit. As it can be observed from Figure 4.11, the equivalent capacitance C_{EQ} of the switched capacitor C_S can vary between two limits:

$$Max\ (C_{EQ}) = C_S \text{ (AC switch turns on)} \qquad 4.5$$

$$Min\ (C_{EQ}) = 0 \text{ (AC switch turns off)} \qquad 4.6$$

However, in order to perform accurate tuning, C_{EQ} must have a continuous capacitance variation between the extreme values 0 and C_S. This continuous variation can be realized by acting on the conduction duty cycle of the AC switch. Nevertheless, when applying this switching technique, some physical impossibilities may occurs if some synchronization conditions are overlooked. The waveform of the synchronous switched capacitor is illustrated in Figure 4.12. As can be seen from Figure 4.11 and Figure 4.12, each time the AC switch is closed, it connects the fixed capacitor C_{Fix} driven by a sinusoidal voltage to the switched capacitor C_S. C_S is previously charged to a constant voltage V_{CS}. Consequently, if no specific synchronization is performed, when the AC switch is closed, the instantaneous voltage across the fixed capacitor C_{Fix} will randomly differs from the one that was applied across the switched capacitor C_S. This situation, produces the physical impossibility of over current spikes (having theoretically an infinite intensity) flowing through the AC switch. In order to avoid this issue it is mandatory to synchronize the conduction time of the AC switch in such a way that when the switch is driven on, the instantaneous voltages across the capacitors C_{Fix} and C_S are identical. This objective constitutes the principle of the synchronization condition that is detailed in the next section.

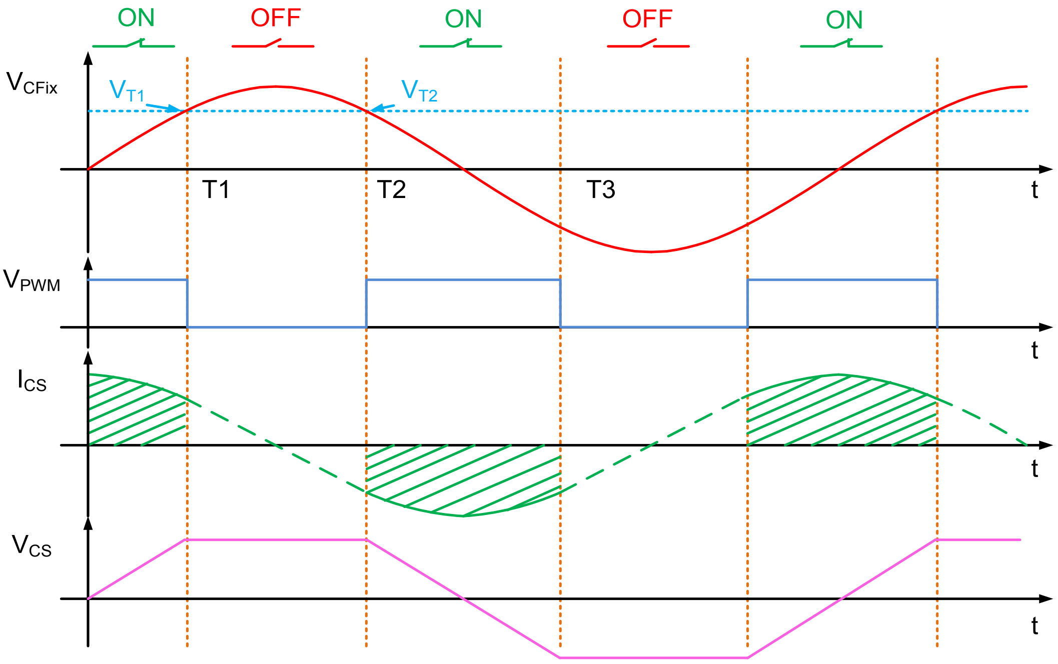


Fig.4.12 Waveform of the synchronous switched capacitor.

4.4.2 Synchronization Condition of the Proposed Auto-tuning Network

To achieve the synchronization objective, it is necessary to know the values of the voltages V_{CFix} and V_{CS} across the capacitors C_{Fix} and C_S, respectively, just before the conduction of the AC switch. These values can be found after an examination of the first half period of the chronograms of V_{CFix} and V_{CS} as shown in Figure 4.12. As shown in this figure, the value of V_{CS} at which the switched capacitor C_S is charged is imposed by the instantaneous value taken by the input voltage V_{CFix} just at the opening time of the AC switch (corresponding in Figure 4.12 to the time T_1). The switched capacitor C_S is charged to a voltage given by

$$V_{CS}(T_1) = Max(V_{CFix}) \cdot sin(wT_1) \qquad 4.7$$

As long as the AC switch is open, the voltage across the switched capacitor C_S stays constant and equal to the value given by Equation 4.7, and the voltage (V_{CFix}) applied on the fixed capacitor (C_{Fix}) vary sinusoidally.

The instantaneous voltage applied across C_{Fix}, when the AC switch is turned on again (at a time corresponding in Figure 4.12 to the time T_2), can be described by

$$V_{CFix}(T_2) = Max(V_{CFix}) \cdot sin\left[w\left(\frac{T_{Period}}{2} - T_2\right)\right] \qquad 4.8$$

where T_{Period} defines the period of V_{CFix}. We know that the synchronization condition can be found when $V_{CS}\ (T_1) = V_{CFix}\ (T_2)$. By substituting Equations 4.7 and 4.8 into this equation, we can get Equation 4.9.

$$T_1 = \frac{T_{Period}}{2} - T_2 \qquad 4.9$$

In other words, the synchronization condition can be achieved, when Equaton 4.9 is true. This synchronization condition can be translated into several design rules that should be followed. First, the PWM signal that is applied on the AC switch must have a conduction angle, which is always symmetrical with respect to the zero-crossing points of the sinusoidal voltage V_{CFix} applied across the fixed capacitor C_{Fix}. Second, the electrical charge of the switched capacitor C_S should not be affected by any external cause (e.g., leakage resistances and switching-charge injection).

Being a symmetry condition, this synchronization condition will allow some simplifications in the derivation of the transfer function that follows.

4.4.3 Transfer Function of the Proposed Auto-tuning Network

As mentioned in Section 4.2, several unavoidable variations can cause a detuning of the tank circuit, and the detuned tank circuit will cause a variation of V_{CFix}. Therefore, we cannot generate the PWM by using V_{CFix} directly. In order to obtain a symmetrical PWM signal for the switched capacitor, we apply here an external triangular wave V_{Trig} with the same phase and frequency as V_{CFix} and a constant amplitude. The waveforms of the auto-tuning system that we obtained using a triangular wave are illustrated in Figure 4.13.

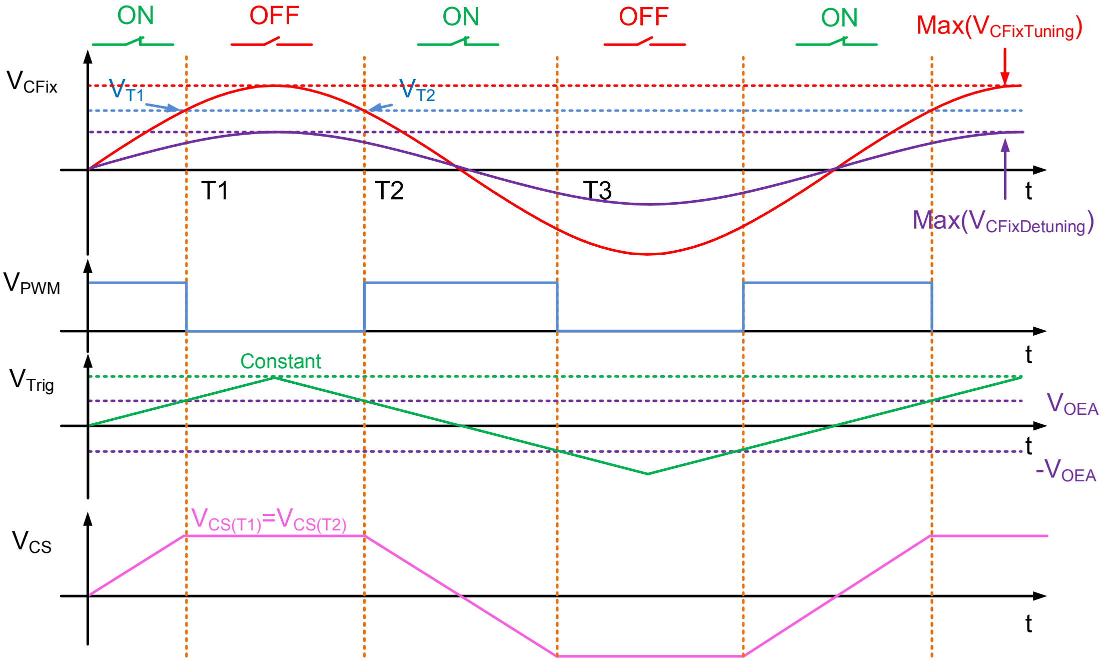


Fig.4.13 Waveform of the auto-tuning system with a non-linear transfer function.

The equivalent capacitance C_{EQ} of the synchronous-switched capacitor can be determined by:

$$C_{EQ} = \Delta Q / \Delta V_{CS} \tag{4.10}$$

where ΔQ is the total electrical charge transferred to C_S during the conduction time interval of the AC Switch. Therefore, ΔQ can be computed using the integral

$$\Delta Q = \int i_{CS} dt \tag{4.11}$$

Taking into account the symmetry property in Equation 4.9 and according to the waveforms shown in Figure 4.13, when $0 < T < T_{Period/4}$, this quantity of electrical charge can be simplified as,

$$\Delta Q|_0^T = \int_0^T i_{CS} dt \tag{4.12}$$

where i_{CS} is the current flowing through C_S. In addition, the voltage variation across C_S during this period is

$$\Delta V_{CFix}|_0^T = Max(V_{CFix}) \tag{4.13}$$

In this integral, i_{CS} is imposed by the voltage waveform applied on C_S according to the classic relation:

$$i_{CS} = C_S\, dV_{CFix}/dt = C_S w Max(V_{CFix}) \cdot coswt \tag{4.14}$$

Therefore, ΔQ can be rewritten as follows:

$$\Delta Q = C_S Max(V_{CFix}) \cdot sinwT \tag{4.15}$$

Substituting Equations 4.13 and 4.15 into Equation 4.10, we finally obtain the equivalent capacitance:

$$C_{EQ} = C_S \cdot sinwT = C_S \cdot sin\theta \tag{4.16}$$

where $T = \theta/\omega$, $(0 < \theta < \pi/2)$, and θ is the half-conduction angle. In order to determine the transfer function of the synchronous-switched capacitor, we need to know the conversion function of the PWM that links the phase-error voltage V_{OEA} to the half-conduction angle (θ).

$$\theta = f(V_{OEA}) = \frac{\pi}{2Max(V_{Trig})} \cdot V_{OEA} \tag{4.17}$$

Finally, substituting Equation 4.17 in Equation 4.16 yields the complete transfer function of the synchronous-switched capacitor.

$$C_{EQ} = C_S \cdot sin[\frac{\pi V_{OEA}}{2Max(V_{Trig})}] \tag{4.18}$$

Because of the strongly nonlinear characteristic of this transfer function, it may be the source of instabilities in the auto-tuning feedback loop. To ensure the stability of the auto-tuning feedback loop, the transfer function of the auto tuning system must be a linear function. Therefore, we need the conversion function of the PWM for the AC switch to verify the linearity of the transfer function. Figure 4.14 presents the waveform of the auto-tuning system, which was obtained using a linear transfer function.

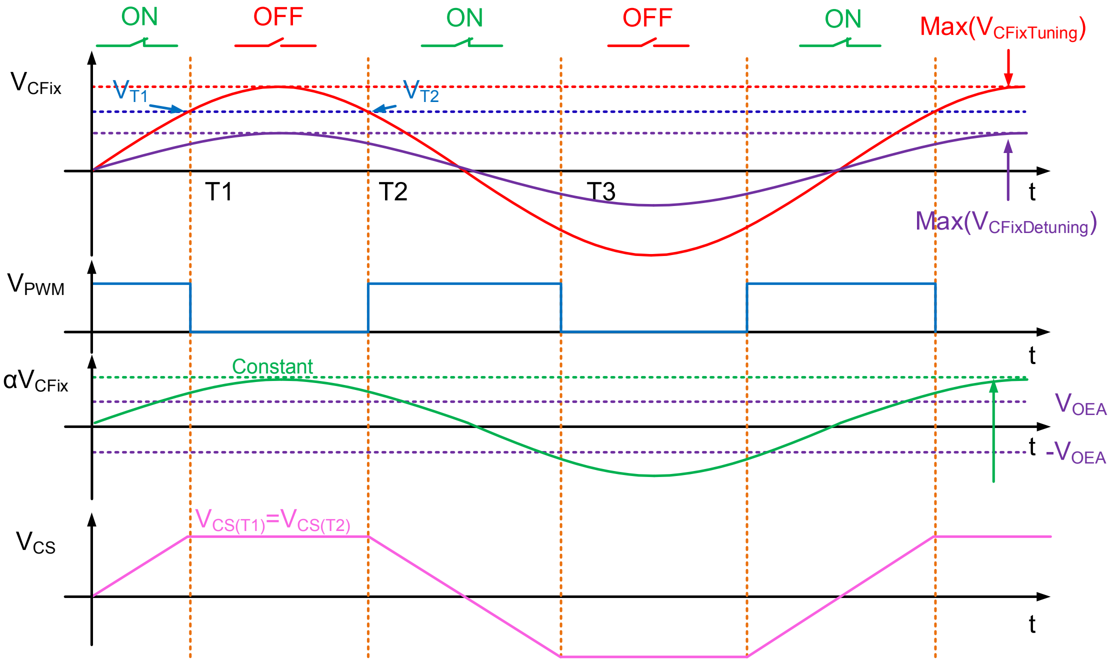


Fig.4.14 Waveform of the auto-tuning system with a linear transfer function.

As seen in this figure, the triangular signal V_{Trig} is replaced by a sinusoidal waveform αV_{CFix}, which has a constant amplitude and the same phase as V_{CFix}. Therefore, the conversion function of the PWM converter becomes

$$\theta = Arcsin\{V_{OEA}/[\alpha Max(V_{CFix})]\} \tag{4.19}$$

Substituting Equation 4.19 into Equation 4.16 yields the linearized transfer function of the synchronous switched capacitor:

$$C_{EQ} = C_S\, V_{OEA}/[\alpha Max(V_{CFix})] \tag{4.20}$$

The solving of the nonlinear problem allows the design of the complete auto-tuning system, which will be described in the next section.

4.4.4 Diagram of the proposed realisation

The diagram of the proposed synchronous switched capacitor system for performing the auto tuning is shown in Figure 4.15. The proposed auto-tuning system using a synchronous switched capacitor is bounded by the green polygon. In order to facilitate its analysis, the auto-tuning system has been partitioned by dotted lines. As it can be seen from this figure, the auto-tuning system proposed in this paper consists of five functional blocks: tuning block, automatic gain control block, phase error detection block, switch signal generation block and AC switch block. These functional blocks implement all the functions presented in previous sections. This auto-tuning system does not require MCU or computer and bulky magnetic components. Therefore, it is perfectly suitable for our application.

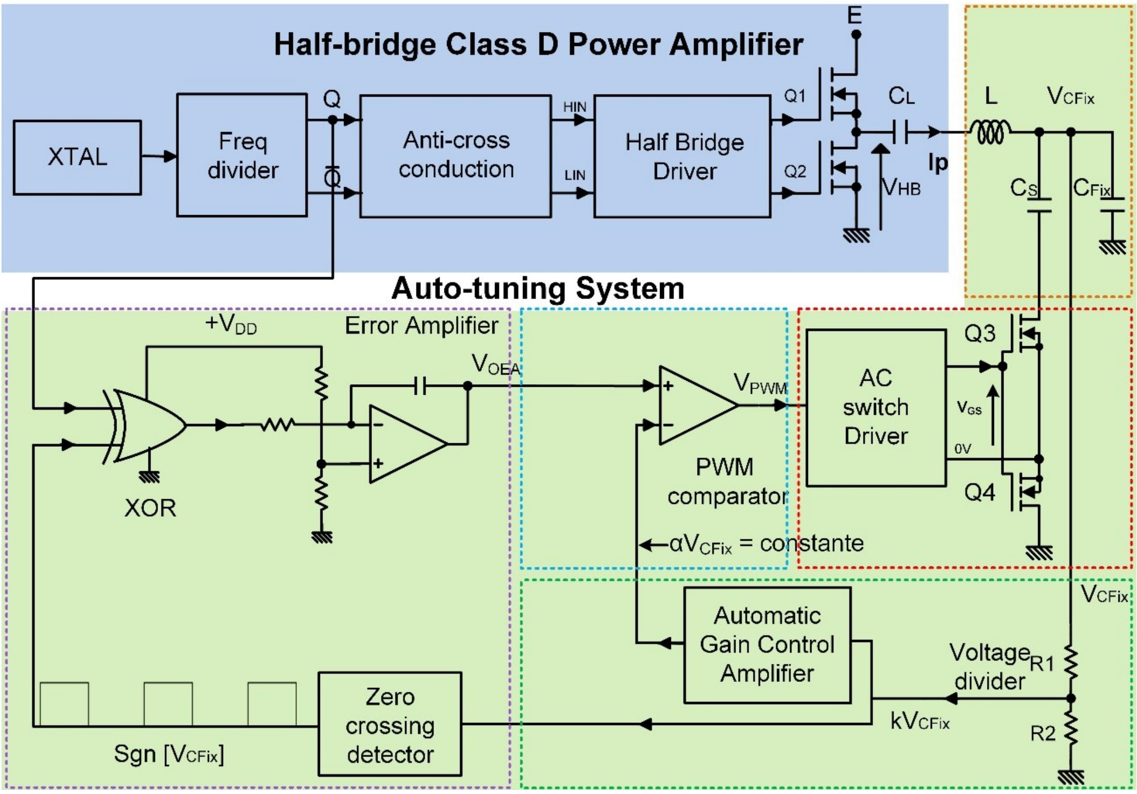


Fig.4.15 Diagram of the realization of the proposed auto-tuning system based on synchronous switched capacitor.

Tuning Block

The tuning block is bounded by the orange dotted line in Figure 4.15. It consists of a static L-type tuning network and a switched capacitor C_S which is connected in parallel with the capacitor C_{Fix} used in the L-type tuning network. This switched capacitor is used to compensate the imaginary impedance drifting of the transducer.

AC Switch Block

The AC switch block is shown in the red dotted rectangle in Figure 4.15. It is used to control the connection status of C_S. The AC switch block used in this thesis is realized with the classical structure [CS1994] by using two identical power MOSFETs N channel (Q3, Q4). As it can be seen from Figure 4.15， the Gate/Source voltage of the transistors used in this topology are floating, the AC switch driver used in this block is consequently realized with an isolated AC switch drive circuit. Moreover, in order to achieve a full output duty cycle, the working frequency of the isolated AC switch drive circuit is required to be much larger than the working frequency of the tuning system.

Automatic Gain Control Block

The automatic gain control block is shown in the area bounded by the green dotted line in Figure 4.15. As known in Section 4.4.3, the linearization of the transfer function is performed by comparing the output of the phase error detection block (V_{OEA}) to a constant amplitude waveform αV_{CFix}, which has the same phase as the voltage across the fixed tuning capacitor (V_{CFix}). This function makes the automatic gain control block becoming one of the most important blocks in the proposed auto-tuning system. The proposed automatic gain control block is composed by a voltage divider and an automatic gain control amplifier. The output voltage of the tuning circuit is more than 100 V that greater exceeds the input range of the automatic gain control amplifier. Therefore, a voltage divider is introduced in this block to attenuate the output voltage of the tuing circuit.

Phase Error Detection Block

The proposed phase error detection block is bounded by the purple dotted line in Figure 4.15. It consists of a phase difference detector and an error amplifier. The proposed phase difference detector is realized by using an exclusive-OR gate (XOR). Therefore, it allows the tuning of the system by controlling a phase difference ($\Delta\varphi = \pi/2$) between the half bridge output voltage (V_{HB}) and the voltage across the tuning capacitor (V_{CFix}). The proposed error amplifier is based on the basic integrator circuit. This error amplifier is used to transfer the phase difference signal into the relevant phase error voltage (V_{OEA}). First, the error amplifier filters the phase difference signal to generate a phase difference voltage. Then, this phase difference voltage is compared with a reference voltage to generate the phase error voltage (V_{OEA}). If the phase difference between V_{HB} and V_{CFix} is π/2, the output signal of phase error detector V_{OEA} is equal to $2.5\ V$.

Switch Signal Generation Block

The proposed swtich signal generation block is illustrated in the area bounded by the purple dotted line in Figure 4.15. As known in Section 4.4.1, the switch signal generation block must ensure that the conduction angle of its output signal is always symmetrical with respect to the zero-crossing points of V_{CFix}. We use two comparators and an inverter to satisfy this criterion. The equivalent capacitance of the switched capacitor is control by the output signal of this block. Therefore, the accuracy of the proposed tuning system is mainly influenced by the accuracy of this block. Besides, the symmetry switching condition of the AC switch is also influenced by this block.

Operation Chronograms

The operation chronograms of the proposed auto-tuning system are shown in Figure 4.16. V_{CFix} is the output voltage of the tuning network, and kV_{CFix} is the attenuated V_{CFix}. αV_{CFix} defines the output signal of the automatic gain control block.

$Sgn[V_{CFix}]$ is the sign signal of V_{CFix}. V_{XOR} is the output signal of the XOR gate. Output signals of the phase error detection block and the switch signal generation block are defined by V_{OEA} and V_{PWM}, respectively.

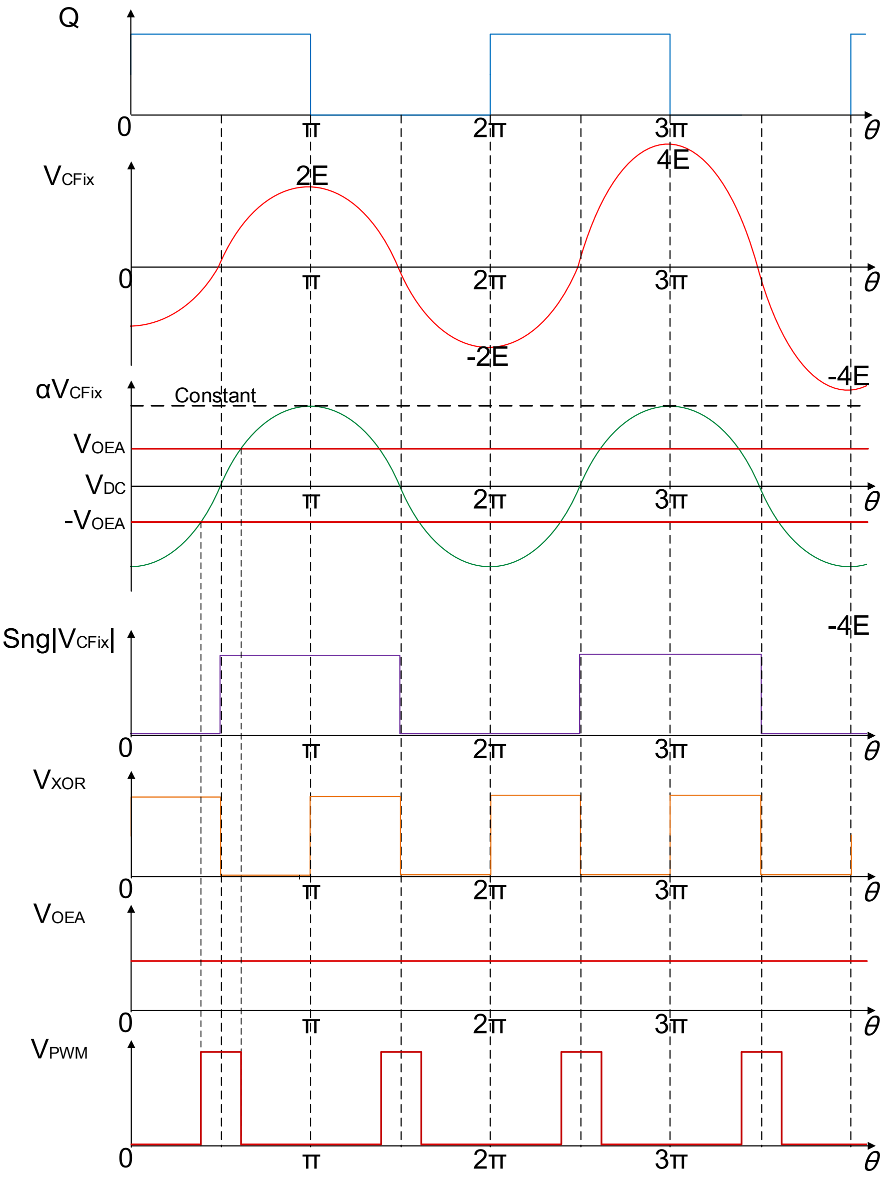


Fig.4.16 Chronograms of the proposed auto-tuning system.

4.5 Stability Analysis of the Proposed Auto-tuning System

The proposed auto-tuning system can be considered as a PLL system, and the study of the stability and speed of this auto-tuning system can be changed to the study of the stability and speed of the equivalent PLL system. The equivalent PLL circuit of the auto-tuning system is shown in Figure 4.17.

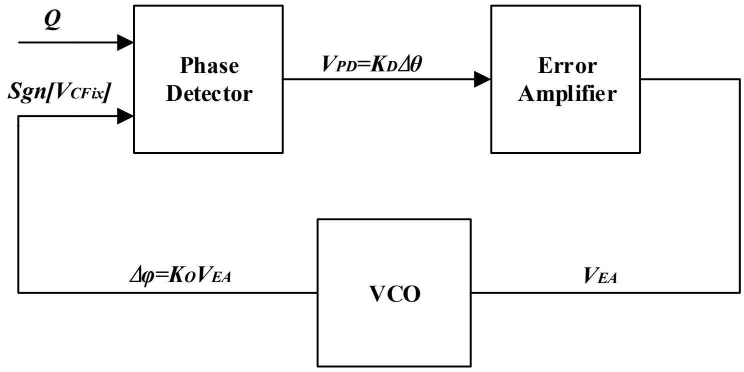


Fig.4.17 Equivalent PLL circuit of the auto-tuning system.

The equivalent PLL circuit contains three parts: a phase detector, error amplifier, and voltage-controlled oscillator (VCO). The transfer function analyses for the three part are as follows:

Phase detector

The phase detector used in our auto-tuning system is an exclusive-OR gate (XOR). Therefore, the transfer function of this phase detector can be written as

$$V_{PD} = \frac{V_{DD}}{\pi}\Delta\theta \qquad 4.21$$

where $\Delta\theta$ is the phase difference between Q and $Sgn[V_{CFix}]$. Therefore, the discriminator sensitivity of the phase detector (K_D) is equal to V_{DD}/π. Figure 4.18 shows the relationship between $\Delta\theta$ and V_{PD}.

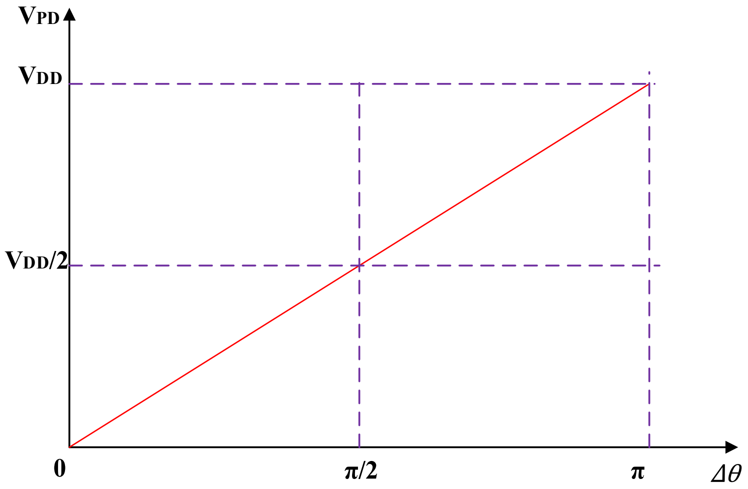


Fig.4.18 Relationship between the phase difference $\Delta\theta$ and the phase error voltage V_{PD}.

Error Amplifier

The error amplifier used in the proposed auto-tuning system is an integrator. The transfer function of this error amplifier is described by

$$G_{PDEA}(jw) = \frac{1}{jwR_2C_1} \tag{4.22}$$

Voltage-controlled Oscillator (VCO)

Assume that the settling time of the VCO is zero, the transfer function of the VCO can be written as $\Delta\varphi = K_O V_{EA}$, where K_O is the modulation sensitivity of the VCO. In addition, K_O can be calculated by

$$K_O = \frac{\Delta\varphi_{EAmax} - \Delta\varphi_{EAmin}}{Max(V_{EA}) - Min(V_{EA})} \tag{4.23}$$

The proposed impedance tuning circuit is a LC circuit and the resistance of the inductor is defined as r. Then, the phase difference between the ouput of the tuning network V_{out} and the input V_{in} can be written as,

$$\Delta\varphi = Arg\left|\frac{V_{out}}{V_{in}}\right| = -\frac{\pi}{2} - \tan^{-1}\frac{wL - 1/wC}{r} \tag{4.24}$$

Therefore, the open loop transfer function of the equivalent PLL circuit is described by the following equation.

$$\begin{aligned} G_{PLL}(jw) &= K_D \cdot K_O \cdot G_{PDEA}(jw) \\ &= \frac{V_{DD}}{\pi} \cdot \frac{\Delta\varphi_{EAmax} - \Delta\varphi_{EAmin}}{Max(V_{EA}) - Min(V_{EA})} \cdot \frac{1}{jwR_2C_1} \end{aligned} \tag{4.25}$$

According to this equation, this PLL system has just one pole, the phase of the system is always equal to $\pi/2$, which means that it is a stable system. In real case, the settling time of VCO is equal to the settling time of the automatic gain control amplifier used in the proposed tuning system. Therefore, the stability of the proposed auto-tuning system is only influenced by the settling of the VCO. In other words, in order to realize a stable tuning system, the pole of the error amplifier used in the phase error detection block is required to be much less than the pole of the automatic gain control amplifier.

In this chapter, the principle of the proposed auto-tuning system for imaginary impedance of the transducer is presented. As can be seen from Figure 4.15, the proposed impedance auto-tuning network has a simplier structure than the existing auto-tuning systems. And the whole system does not require bulky magnetic components that makes it compatible with MRI system. Besides, due to lack of MCU or computer, the cost of this auto-tuning system is much less than the existing tuning systems. In this thesis, the proposed auto-tuning system is realized in two versions: printed circuit board and integrated circuit. The design of these two different versions are presented in chapter 5 and chapter 6, respectively.

Chapter 5

PCB Design of the Proposed Auto-tuning

5.1 Introduction

In this chapter, printed circuit board design (PCB) of the proposed auto-tuning system used to solve the imaginary impedance tuning and impedance drifting problems of the ultrasonic transducer, is presented. This printed circuit board version is used to verify the principle and the operation of the proposed auto-tuning system, and it also helps the design of the integrated auto-tuning system that is presented in chapter 6. This chapter is organized as follows: The proposed auto-tuning system is composed of five functional blocks. In section 5.2, the schematics of the sub-functional blocks used to realize the proposed auto-tuning system are presented, and explanations of the designs are also given out in this section. Section 5.3 presentes the test results of the printed circuit boards of each sub-functional blocks, and the stability analysis of the proposed auto-tuning system is also proposed in this section. Finally, in section 5.4, a conclusion of the printed circuit design of the proposed auto-tuning system is given out.

5.2 PCB Design of the Proposed Auto-tuning System

Figure 5.1 shows the diagram of the proposed synchronous-switched capacitor system in order to perform the auto tuning of a 1.25 MHz power supply for the ultrasound transducer.

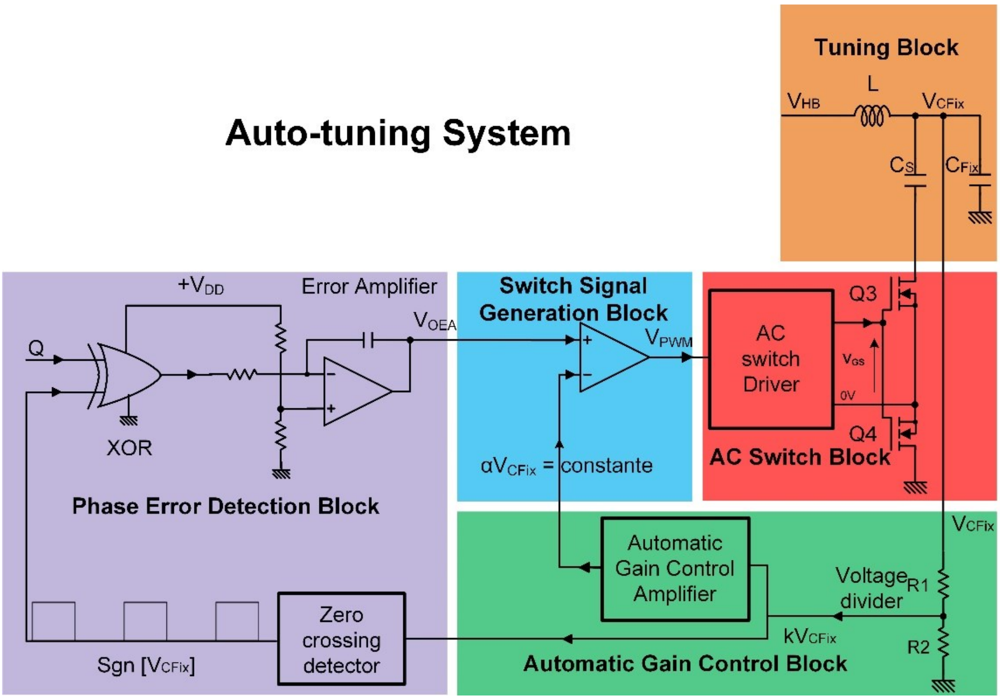


Fig.5.1 A half bridge class D amplifier tuned by a synchronous switched capacitor.

The proposed auto-tuning circuit is composed of five functional blocks:

1) AGC block, which is used to generate a value of αV_{CFix} that has a constant peak value.
2) Phase-error detection block, which is used to obtain the phase-error voltage signal V_{OEA}.
3) Switch signal generation block, which is used to obtain the AC switch control signal.
4) AC switch block, which is used to switch the capacitor.
5) Tuning Block, which is composed of a static LC tuning network and a switched capacitor.

The software used to design the printed circuit board of the proposed auto-tuning system is *Altium Designer Release 10*. The schematics and PCB designs of each functional blocks will be presented in the following sections.

5.2.1 Automatic Gain Control Block

The automatic gain control (AGC) amplifier can be classified as feedforward and feedback AGCs based on their structures [PJPA2011]. The diagrams of these two different AGCs are illustrated in Figure 5.2. As presented in the figure, the input signal V_{IN} is amplified by a variable-gain amplifier (VGA), which can offer a variable gain. The gain of the VGA is controlled by a gain-control voltage V_{CTR}, which is generated by the feedforward or feedback loop. First, the feedforward or feedback loop detects the amplitude level of the input or output signal V_{in}/V_{out} by using a peak detector. Then, it compares the amplitude voltage with a reference voltage V_{REF}, after which we used a loop filter or error amplifier to filter and generate the required gain-control voltage.

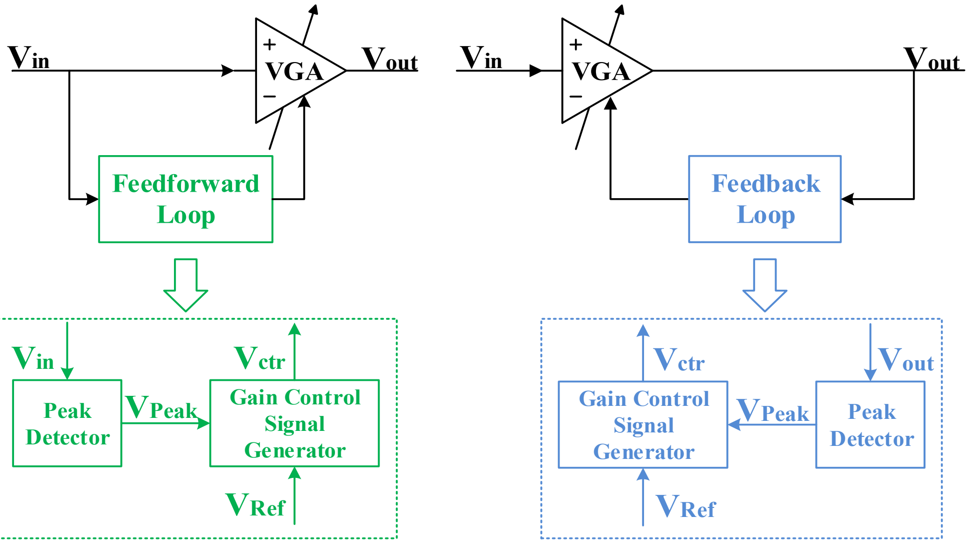


Fig.5.2 Simplified diagram of feedforward (*left*) and feedback (*right*) AGC circuit.

Both of these architectures have their own advantages and disadvantages, as illustrated in Table 5.1.

Table 5.1 Summary of main AGC loop control characteristics.

	Advantages	***Disadvantages***
Feedforward AGC	*The settling time only depends on the peak detector response.* *It has no instability problems.*	*The loop must has high linearity.* *Wide input dynamic range of the peak detector is required.*
Feedback AGC	*Inherently higher linearity* *Lower input dynamic range required by peak detector.*	*Settling time is higher than feedforward AGC.* *Bandwidth is limited.*

The variation of the output voltage, which is caused by the impedance detuning, has a ratio of about 20. Therefore, the designed AGC are required to have an input dynamic range of about 26 dB. In order to satisfy the required input dynamic range, the dynamic input range of the peak detector in the AGC must be greater than 26 dB, which is hard to realize with an analog circuit. To solve this problem, we can use a digital circuit to detect the amplitude level of the input signal [PJPA2011]. However, by using this solution, we need a digital signal processor (DSP) in the feed-forward loop, which will be used to generate the gain-control voltage. The use of DSP will increase the cost, and will also increase the circuit complexity. For feedback AGC, a lower input dynamic range is required by the peak detector. In other words, there will be no need of a high input dynamic-range peak detector.

For our project, the gain error is required to be lower than 1%. As is commonly known, the feedforward AGC must have a high linearity in order to verify the accuracy of the gain. This means that the loop must be well designed to meet our requirement for the gain error. For the feedback case, the AGC loop has an inherently higher linearity. As a result, there is no need to perform a complex analysis to verify the high linearity of the AGC loop.

The gain error of the feedback AGC is only related to the error amplifier. In our study, considering the requirements of variable gain range, bandwidth, settling time, and cost performance ratio, the feedback loop AGC is chosen for our application. Therefore, in this paper, we focus on the design of a feedback AGC for our application. The diagram of the proposed AGC is illustrated in Figure 5.3.

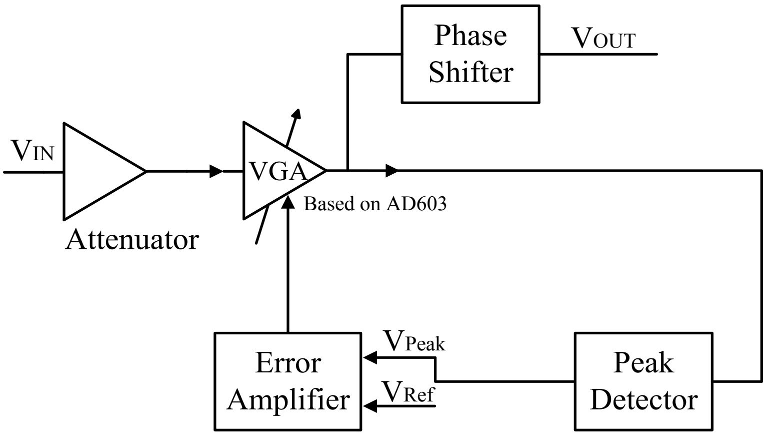


Fig.5.3 Diagram of the proposed automatic gain congrol amplifier.

The output signal of the power amplifier is as high as 125 V, which exceeds the input range of the VGA chip. Therefore, there is a need for an attenuator in the AGC. The schematic of the attenuator is illustrated in Figure 5.4.

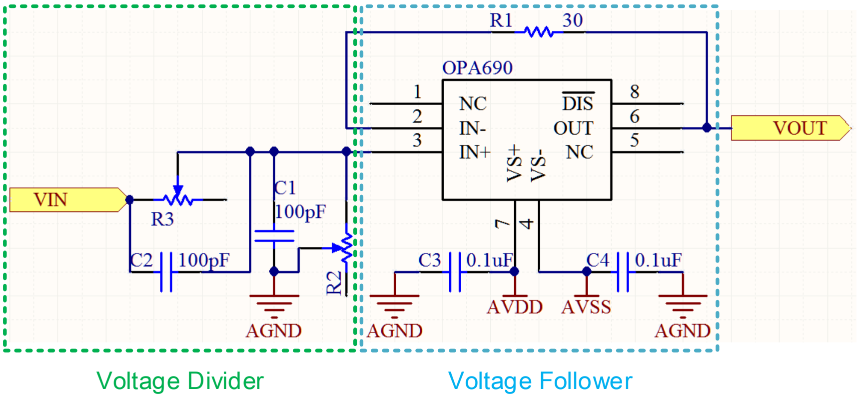


Fig.5.4 Schematic of the output signal attenuator.

The input signal of the attenuator is divided by the series connected resistors (R_2 and R_3). In order to minimize the influence of this divider, two capacitors C_1 and C_2 are separately shunted to the resistors R_2 and R_3. A voltage follower is used in the attenuator to eliminate the effects of loading because the input impedance is infinite and the output impedance is finite for an ideal amplifier. The transfer function of the attenuator is defined by

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2}{R_2+R_3}\frac{1+jwC_1R_2}{1+jwC_2R_3} = \frac{C_2}{C_1+C_2}\frac{1+jwC_1R_2}{1+jwC_2R_3} \tag{5.1}$$

Therefore, we see that the attenuation provided by this circuit is constant regardless of the frequency if the condition $R_2C_1 = R_3C_2$ is satisfied. The voltage follower is realized using an operational amplifier (OPA690), which has a 10 µA input bias current according to its datasheet. This operational amplifier is chosen due to its wide bandwidth (500 MHz), high slew rate (1800V/µs) and large output swing (4V) [OPA690]. In order to reduce the effect of the attenuator, the current flows through R_2 and R_3 (I_{Res}) are required to be much larger than the bias current of the voltage follower. In this thesis, we set $I_{Res} = 100\ \mu A$. Then, we obtain the following equation.

$$R_2 + R_3 = \frac{Min(V_{IN})}{I_{Res}} = \frac{6.35}{100\times10^{-6}} = 63.5k\Omega \qquad 5.2$$

According to the datasheet [OPA690] of OPA690, if the amplifier is directly connected as a voltage follower, there will be self-excitation problem. Therefore, a small resistor R_1 (30 Ω) is applied to avoid the self-excitation of the amplifier.

The maximum input voltage for the VGA amplifier used in our application is 1.4 V. The attenuation of this circuit must be greater than $Max(V_{IN})/1.4 = 90$. Thus, we obtain Equation 5.3.

$$\frac{R_2}{R_2+R_3} = \frac{1}{90} \qquad 5.3$$

By substituting Equation 5.3 into Equation 5.2, we obtain the values of R_2 and R_3 as follows:

$$R_2 = 706\Omega \qquad R_3 = 62.8k\Omega \qquad 5.4$$

The capacitance of C_1 is required to be much larger than the input capacitance of the voltage follower. Here, we chose $C_1 = 1\ nF$. Therefore, the capacitance of C_2 can be calculated by

$$C_2 = \frac{C_1}{\left(\frac{R_2+R_3}{R_3}-1\right)} = \frac{C_1}{89} \simeq 11pF \qquad 5.5$$

The time response of the AGC is determined by its gain-control function. There are two kinds of gain-control functions for the variable-gain-control amplifier used in the AGC: a linear gain-control function and an exponential gain-control function. The Simulink models of the AGCs with these two different gain-control functions are demonstrated in Figures 5.5 and 5.6, respectively.

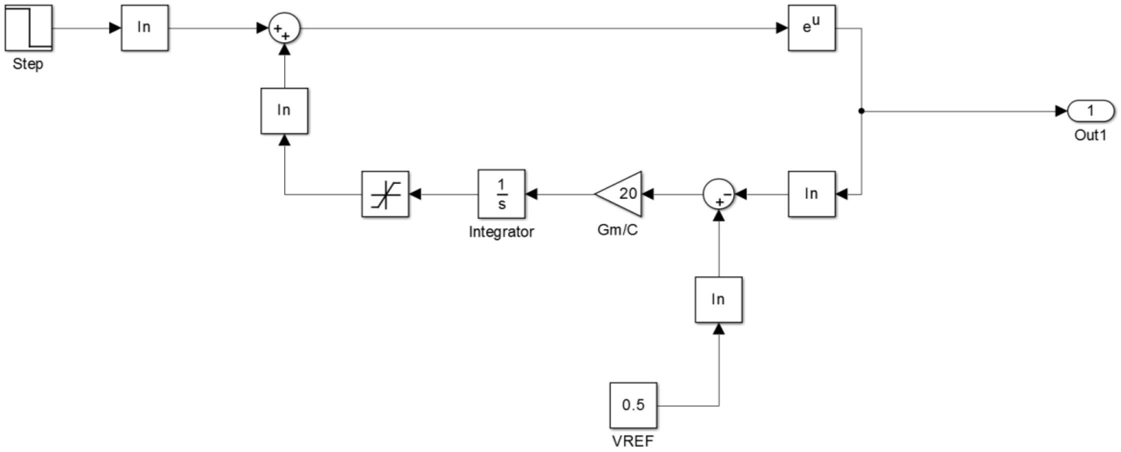


Fig.5.5 Simulink model of AGC with linear gain function [PJPA2011].

As known from [PJPA2011], the time response of the AGC with the linear gain-control function is described by:

$$\tau = \left[\frac{1}{V_{CTR}} \frac{G_{Filter}}{C} K\right]^{-1} \tag{5.6}$$

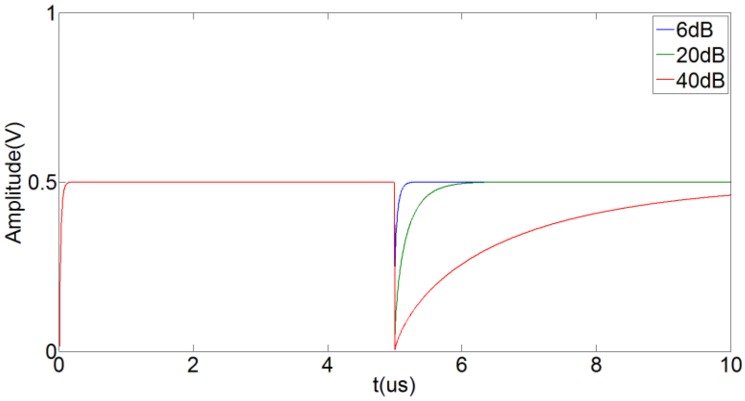


Fig.5.6 Time response of linear AGC for diffrent stepwise functions.

where K is a constant, G_{Filter} is the gain of the error amplifier, and C is the capacitor used in the error amplifier. According to this figure, the settling time of this AGC should increase as the input signal decreases. Thus, as expected, the output transient response shown in Figure 5.6 validates the expected result for the linear AGC. As a result, τ depends on the input signal strength because V_{CTR} is inversely proportional to the input level. In our project, the input dynamic range is required to be 30 dB. This means that the time constant for small signals would be about 32 times longer than the minimum τ.

As a result, the auto-tuning circuit must wait until the output of AGC is constant, the time performance of the synchronous-switched capacitor control circuit would be degraded.

The second approach employs an exponential function [PJPA2011] $G(V_{CTR})$, which is given in Equation 5.7 to obtain a constant settling time, as shown in Equation 5.8. The Simulink model of the AGC with exponential gain control function is shown in Figure 5.7.

$$G(V_{CTR}) = N_2 e^{N_1 V_{CTR}} \tag{5.7}$$

$$\tau_{exp-log} = \frac{C}{G_{Filter} N_1 N_2} \tag{5.8}$$

where N_1 and N_2 are constants, and G_{Filter} and C are fixed.

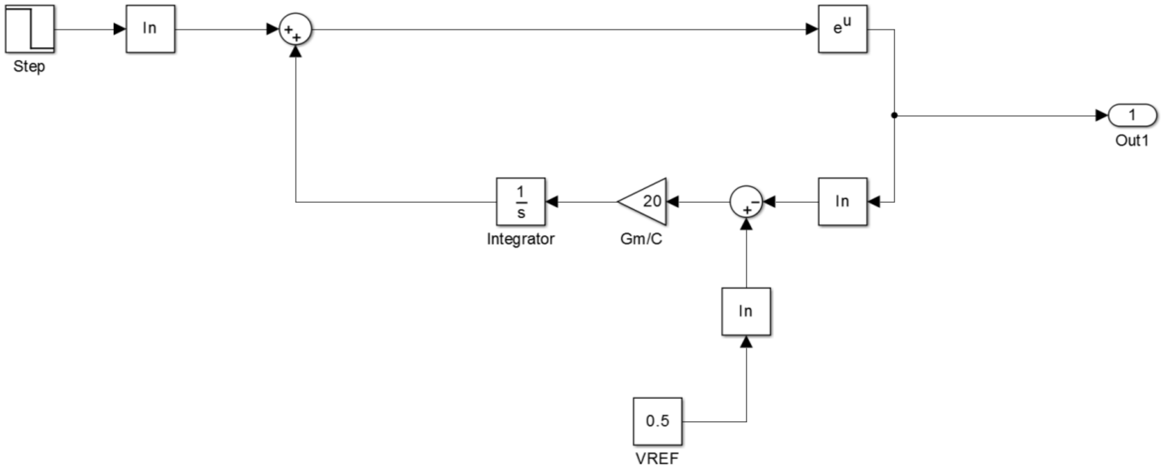


Fig.5.7 Simulink model of AGC with exponential gain function [PJPA2011].

The same simulation conditions were employed as in the previous model.

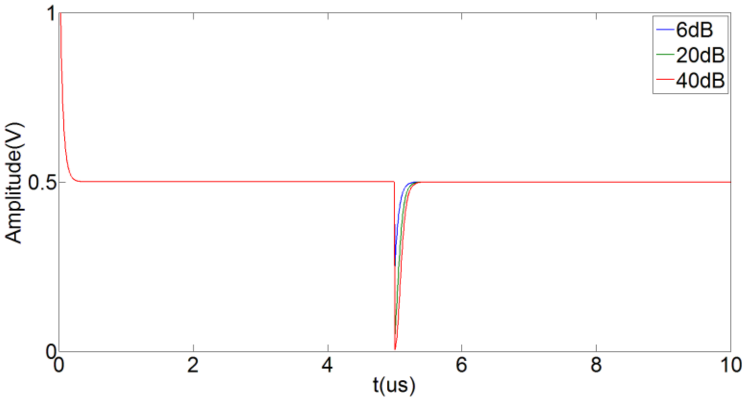


Fig.5.8 Time response of exponential AGC with different stepwise functions.

The results are shown in Figure 5.8. We observed that the settling time is almost constant and independent of any external parameter. For this reason, we chose this gain control function in this paper.

Therefore, the proposed AGC is based on the AD603, which has an exponential gain-control function. In addition, the schematic of the proposed VGA is presented in Figure 5.9.

The gain range of the AD603 is from −11 dB to +31 dB with a bandwidth of 90 MHz or +9 dB to +51 dB with a bandwidth of 9 MHz [AD603]. In our application, we chose the −11 dB to +31 dB gain range. The gain is controlled at a high impedance (50 MΩ) and low bias (200 nA) differential input; the scaling factor is 25 mV/dB, requiring a gain-control voltage of only 1 V to cover the 40 dB of the gain range that fulfills our requirements.

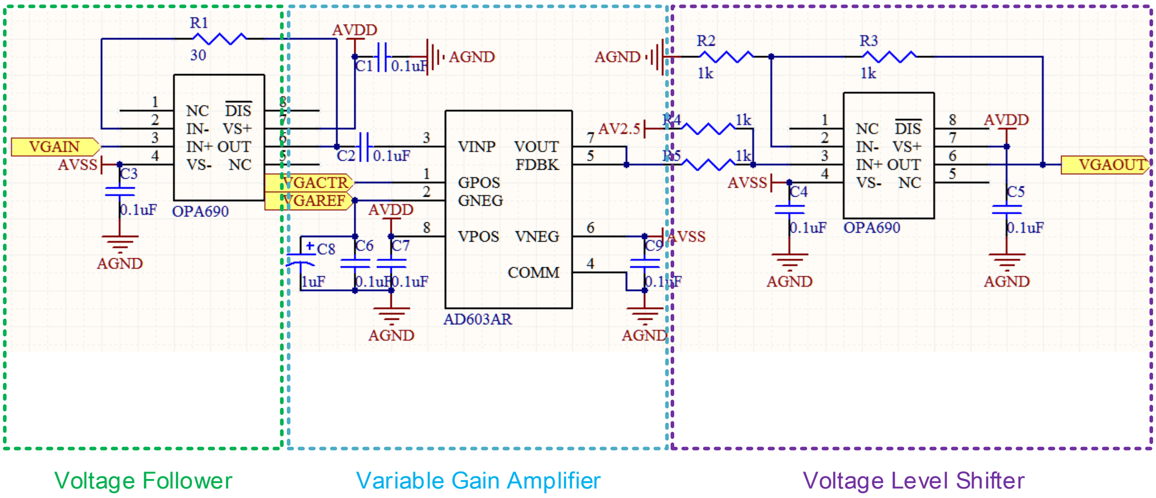


Fig.5.9 Schematic of the proposed variable gain amplifier.

According to the datasheet of the AD603, to prevent self-excitation, it requires a voltage follower at the input of the AD603 [AD603]. In our application, most of the chips used in phase error detection block and switch signal generation block have a 5 V single power supply. Therefore, the output of the AGC needs to have a 2.5 V DC voltage. We applied a level shifter at the output of the AD603.

The transfer function of the VGA can be defined by Equation 5.9.

$$G_{VGA}(jw) = e^{4.6V_{CTR}-1.38} \cdot \frac{1}{1+\frac{f}{f_{BWAD603}}} \cdot \left(\frac{1}{1+\frac{f}{f_{BWOPA690}}}\right)^{2} \qquad 5.9$$

The settling time of the auto-tuning system is limited by the settling time of the AGC. Moreover, for the AGC, its settling is limited mainly by the detected speed of the peak detector. Therefore, we need a fast peak detector to reduce the settling time of the auto-tuning system. In this thesis, we use a reset and write peak detector. The schematic of the proposed peak detector is illustrated in Figure 5.10.

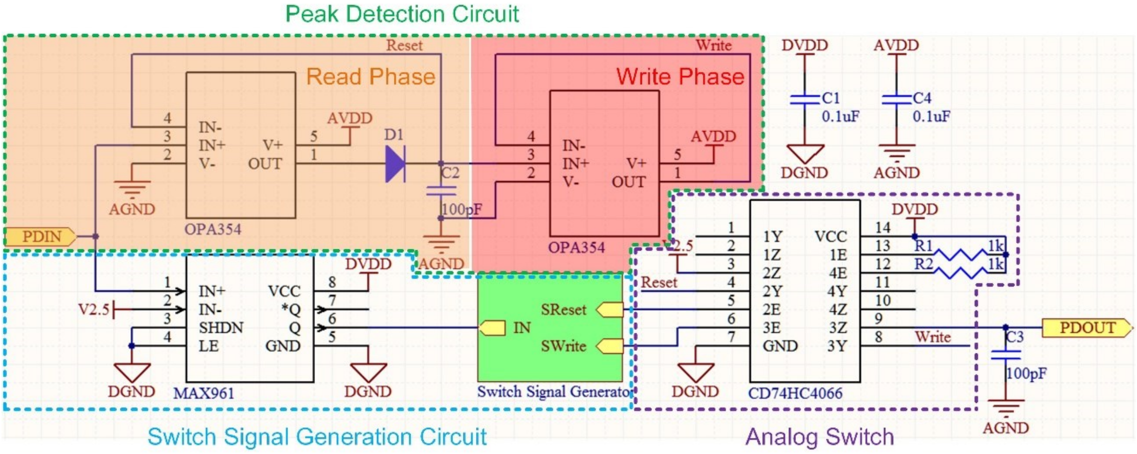


Fig.5.10 Schematic of the proposed peak detector.

The chronogram of this peak detector is illustrated in Figure 5.11.

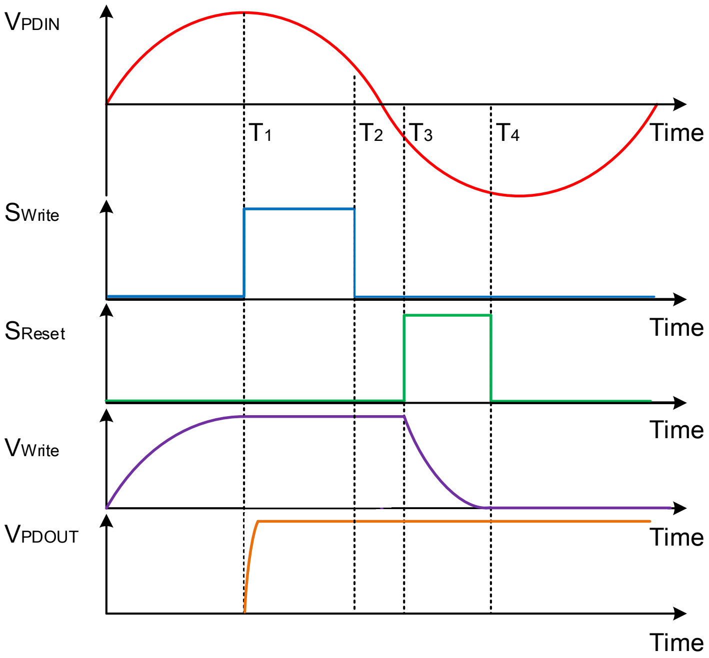


Fig.5.11 Chronogram of the proposed peak detector.

Phase ($0 \leq t \leq T_1$): S_{Write} and S_{Reset} are off. The equivalent circuit during this period is illustrated in Figure 5.12. The voltage applied across C_2 (V_{C2}) is charged to follow the input voltage V_{PDIN}.

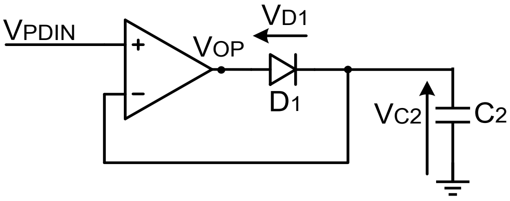


Fig.5.12 Equivalent circuit of the peak detector during period ($0 \leq t \leq T_1$).

From this figure, we can obtain the following equations:

$$V_{OP} = V_{C2} + V_{D1} \qquad 5.10$$

$$V_{OP} = A(V_{PDIN} - V_{C2}) \qquad 5.11$$

By combining these two equations, we get

$$V_{C2} = \frac{A}{1+A} V_{PDIN} - \frac{1}{1+A} V_{D1} \simeq V_{PDIN} \qquad 5.12$$

Phase ($T_1 \leq t \leq T_2$): S_{Write} turns on, and S_{Reset} is still off. The equivalent circuit during this period is shown in Figure 5.13. C_3 is connected to a voltage follower that is used to follow V_{C2}. In this period C_3 is charged to $Max(V_{C2})=V_{Peak}$.

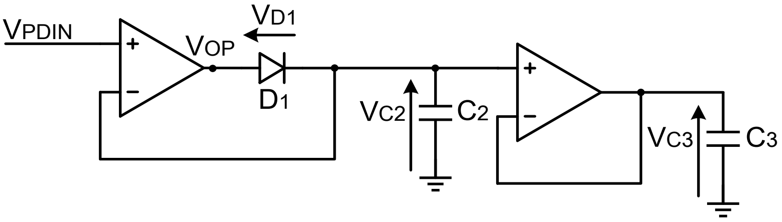


Fig.5.13 Equivalent circuit of the peak detector during period ($T_1 \leq t \leq T_2$).

Phase ($T_2 \leq t \leq T_3$): S_{Write} turns off and S_{Reset} is still off. The voltages applied across C_2 and C_3 remain unchanged. The simplified circuit during this period is shown in Figure 5.14.

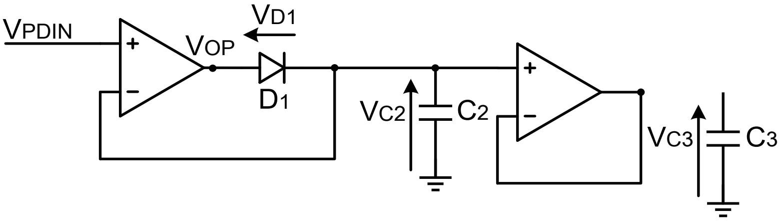


Fig.5.14 Equivalent circuit of the peak detector during period ($T_2 \leq t \leq T_3$).

Phase ($T_3 \leq t \leq T_4$): S_{Write} is off and S_{Reset} turns on. C_2 is connected to the DC voltage of the input signal and discharged. The equivalent circuit during this period is shown in Figure 5.15 as follows.

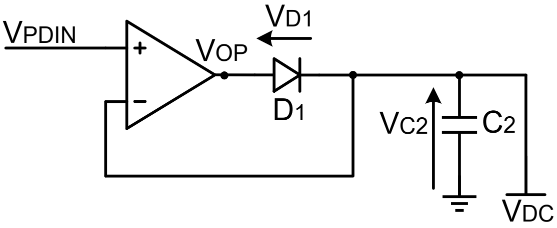


Fig.5.15 Equivalent circuit of the peak detector during period ($T_3 \leq t \leq T_4$).

The peak detector is used to capture the crest of the sinusoidal signal and then keep it constant. In other words, the gain of this circuit is equal to one. In addition, the designed peak detector has a delay of about half period of the input signal. Then, the transfer function of the peak detector is described by

$$G_{PD}(jw) = e^{-jw\tau_{PD}} \quad 5.13$$

$$Arg\left|\frac{V_{Peak}}{V_{OP}}\right| = -\frac{180\tau w}{\pi} = -57.3 \cdot \frac{T_{Period}}{2} \cdot w \quad 5.14$$

where $T_{Period} = 1/f = 0.8\ \mu s$. Figure 5.16 shows the schematic of the switch-signal generator of the peak detector. It is composed by two CMOS logic dual retriggerable precision monostable multivibrators (74HC4538). 74HC4538 is selected due to its high operation speed and high accuracy [74HC4538].

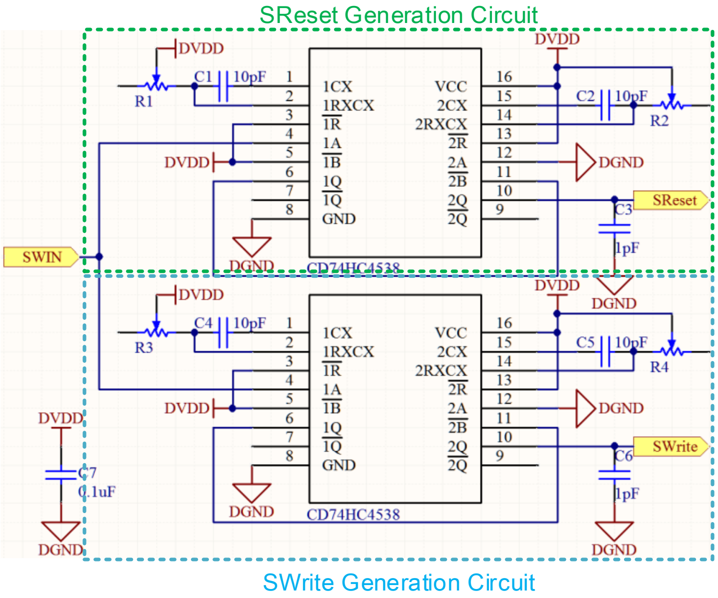


Fig.5.16 Schematic of the switch signal generator of the peak detector.

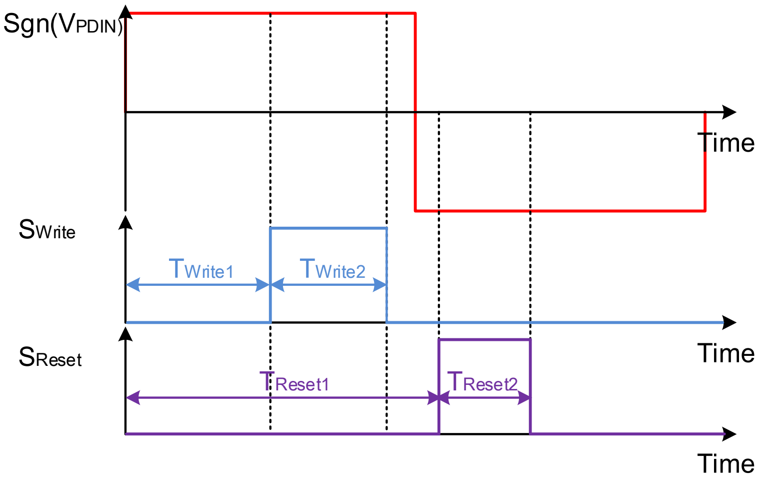


Fig.5.17 Chronogram of the switch-signal generator.

The chronogram of the switch-signal generator is illustrated in Figure 5.17. According to the datasheet [74HC4538], T_{Reset1}, T_{Reset2}, T_{Write1}, and T_{Write2} can be calculated by

$$T_{Reset1} = 0.7R_1C_1 \qquad T_{Reset2} = 0.7R_2C_2 \tag{5.15}$$

$$T_{Write1} = 0.7R_3C_4 \qquad T_{Write2} = 0.7R_4C_5 \tag{5.16}$$

where $R_{1,2,3,4} \geq 5\ k\Omega$ and $C_{1,2,4,5} \geq 0\ pF$. By setting $T_{Reset1} = 562.5\ ns$, $T_{Reset2} = 187.5\ ns$, $T_{Write1} = 250\ ns$, and $T_{Write2} = 187.5\ ns$, the values of $R_{1,2,3,4}$ and $C_{1,2,4,5}$ can be obtained as follows: $R_1 = 8\ k\Omega$, $R_2 = 2.7\ k\Omega$, $R_3 = 3.6\ k\Omega$, $R_4 = 2.7\ k\Omega$, $C_1 = 100\ pF$, $C_2 = 100\ pF$,

$C_4 = 100\ pF$, $C_5 = 100\ pF$.

The schematic of the error amplifier in the proposed AGC is shown in Figure 5.18. The transfer function of the error amplifier can be written as

$$G_{EA}(jw) = \frac{V_{EAOUT}-V_{ref}}{V_{Peak}-V_{ref}} = -\frac{1}{jwR_2(C_1+C_2)}\frac{1+jwR_1C_1}{1+jwR_1(C_1C_2/C_1+C_2)} \qquad 5.17$$

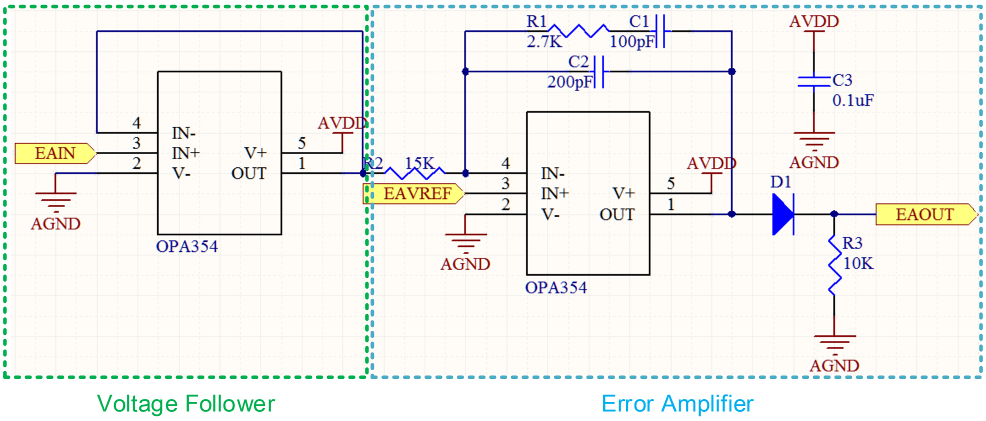


Fig.5.18 Schematic of the error amplifier in the proposed AGC.

A voltage follower is applied before the error amplifier to minimize the influence of the error amplifier on the former circuit. As shown in Figure 5.3, the proposed AGC circuit is a closed-loop system, it is therefore necessary to study its stability and speed. By multiplying the transfer functions of the VGA, peak detector, and error amplifier together, we can obtain the transfer function of the AGC as follows:

$$G_{AGC}(jw) = G_{AGC}(jw) \cdot G_{PD}(jw) \cdot G_{EA}(jw) \qquad 5.18$$

Substituting the maximum gain of the VGA into this transfer function, we can get the gain of the system in decibels.

$$|G_{AGC}(jw)| = 30db + 20log(|G_{EA}(jw)|) \qquad 5.19$$

and the phase of the AGC system is described by

$$Arg|G_{AGC}(jw)| = -tan^{-1}\left(\frac{f}{90MHz}\right) + \left(-57.3 \cdot \frac{T_{Period}}{2} \cdot 2\pi f\right) + Arg|G_{EA}(jw)|$$

5.20

According to the principle of stability of the system, we use MATLAB to determine the frequency of a unity gain of $G_{AGC}(jw)$ by changing the parameters of the error amplifier. Then, we calculate the phase margin of the AGC at this frequency. When the phase margin is greater than 0, the system will be stable. The results of this operation were as follows: $R_1 = 2.7\ k\Omega$, $R_2 = 15\ k\Omega$, $C_1 = 100\ pF$, and $C_2 = 200\ pF$. The frequency response of the error amplifier is illustrated in Figure 5.19.

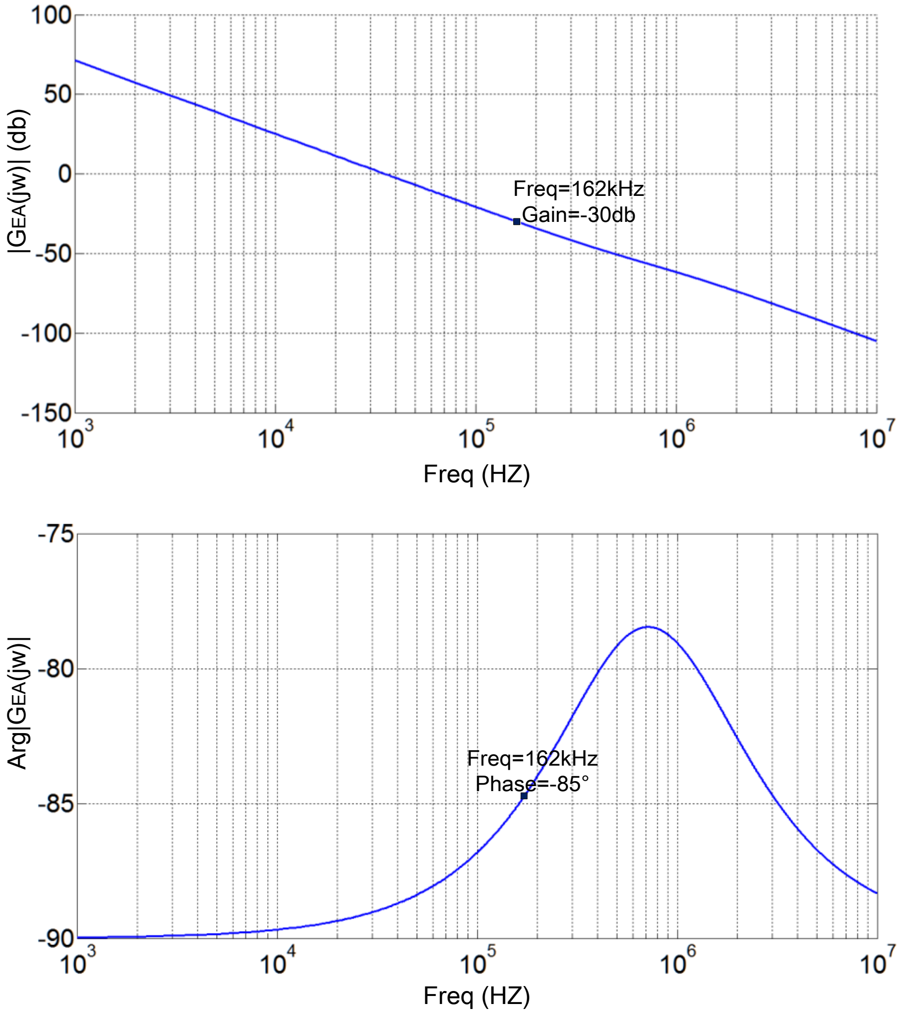


Fig.5.19 Frequency response of the error amplifier in the proposed AGC.

As can be seen from this figure, when $f = 162\ kHz$, $|G_{AGC}(jw)| = 0\ db$, and the phase margin of the AGC is calculated by

$$\varphi_{AGC} = 180\,^{\circ} - Arg|G_{AGC}(jw)| = 180\,^{\circ} - 0.1\,^{\circ} - 23.3\,^{\circ} - 85\,^{\circ} = 71.6\,^{\circ} \qquad 5.21$$

Obviously, the AGC system is stable. In addition, the speed of the AGC can be increased by adjusting the values of the elements of the error amplifier, but the stability of the system will be reduced.

The designed PCB of the AGC is illustrated in Figure 5.20. This board is a 1.6 mm double-side fiberglass PCB, and the copper foil on the PCB is chosen to be 105 µm. The dimensions of the proposed AGC are 7.2 cm × 5.5 cm.

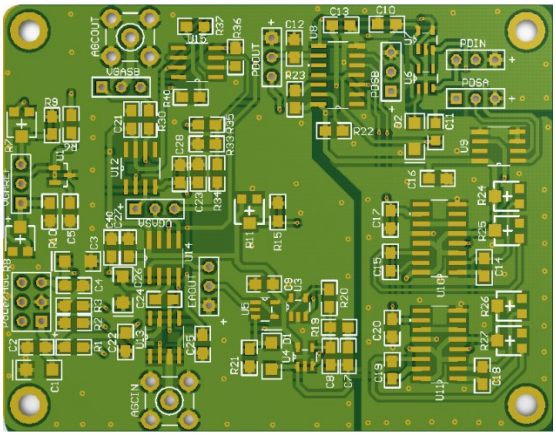


Fig.5.20 Printed circuit board of designed AGC.

5.2.2 Phase Error Detection Block

The schematic of the proposed phase-error detector is shown in Figure 5.21. The phase-error detector consists of a phase shifter, an XOR gate, an integrator, and an inverter.

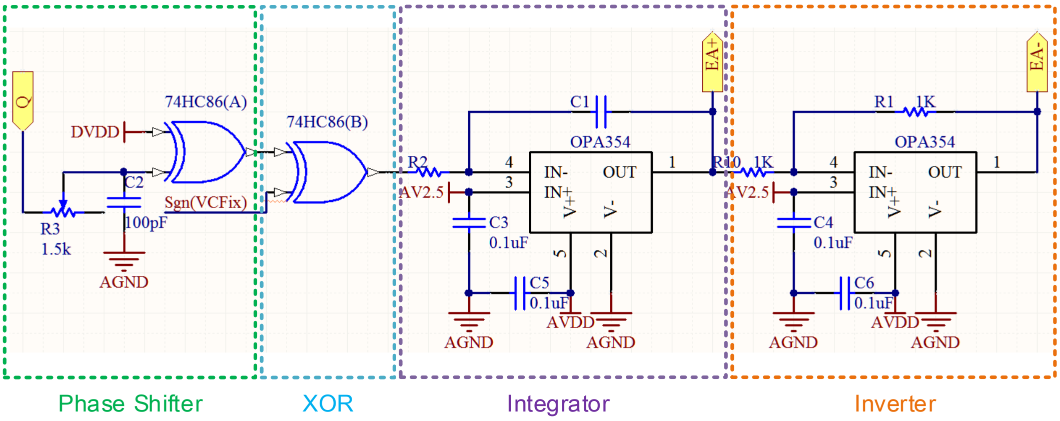


Fig.5.21 Schematic of the proposed phase error detector

The phase error should be measured between the voltage (V_{CFix}) across capacitor C_{Fix} and the output of the half-bridge circuit (V_{HB}), but we want to prevent the connections between the high-power output signal and low-power devices. We use the switch signal of the half-bridge circuit to replace V_{HB}. As discussed in section 3.6, there is a delay of about 50 ns between the output of the half-bridge and its input signal. Therefore, we applied a phase shifter to cancel this delay. The capacitor C_2 used in this phase shifter is 100pF. The resistor used in this phase shifter is a variable resistor which has a maximum resistance of 1.5 kΩ. The minimum delay of the phase shifter is zero, and the maximum delay that can be offered by this phase shifter is calculated by

$$T_{Delay} = Max(R_3) \cdot C_2 \cdot ln(2) \simeq 104ns \qquad 5.22$$

After the cancelling of the undesired delay by the phase shifter, an XOR gate is used as a phase comparator. We applied an integrator to change the phase difference signal into a phase-error voltage. Besides, this integrator can also filter the phase-difference signal generated by XOR gate, and compare phase difference voltage with a desired reference voltage. The transfer function of this integrator is described by

$$G_{PDEA}(jw) = \frac{1}{jwR_2C_1} \qquad 5.23$$

To achieve a stable tuning system, the following inequation should be true.

$$\tau_{PDEA} > Max(\tau_{AGC}) = 7 \times 0.8us|_{f=1.25MHz} \qquad 5.24$$

Therefore, we chose $\tau_{PDEA} = 3 \times Max(\tau_{AGC}) = 16.8\ \mu s$ and $R_2 = 15\ k\Omega$. Then, C_1 can be calculated by

$$C_1 = \frac{\tau_{PDEA}}{2\pi R_2} \simeq 180pF \qquad 5.25$$

The simulation results of the frequency response of the proposed error amplifier is illustrated in Figure 5.22.

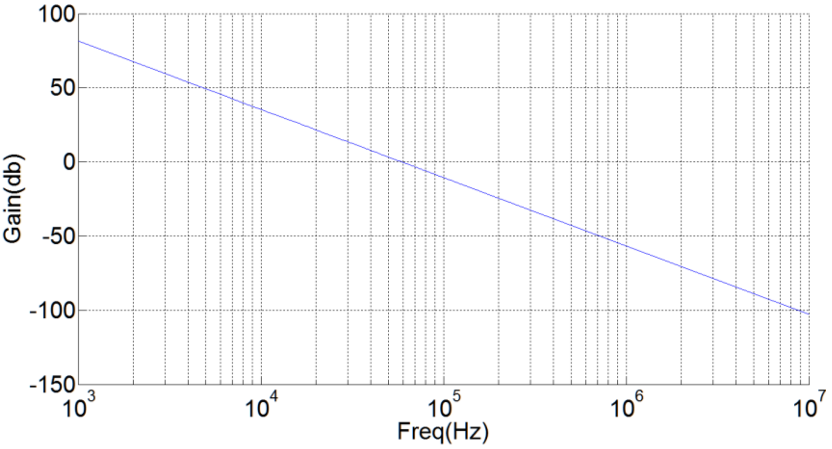


Fig.5.22 Frequency response of the error amplifier in the phase-error detector.

In order to make sure the generated switch signal has a conduction angle, which is always symmetrical with respect to the zero-crossing points of V_{CFix}, we need a symmetrical phase error signal. Therefore, an inverter is added at the output stage of the phase error detection block.

5.2.3 Switch Signal Generation Block

The schematic of the proposed switch-signal generator is shown in Figure 5.23. As analyzed in section 4.4.2, the switch signal applied on the switch capacitor must has a conduction angle, which is always symmetrical with respect to the zero-crossing points of V_{CFix}. In this paper, we used two comparators to make sure the symmetrical conduction. The output signal of the proposed AGC is compared with the phase-error voltage (V_{EA+} and V_{EA-}) in order to obtain PMW_+ and PWM_-. Then, we applied a NOR gate to combine these two signals in order to generate the switch control signal. In this way, the generated switch control signal is always symmetrical with respect to the zero-crossing points of the V_{CFix}, which is applied across the fixed capacitor C_{Fix}.

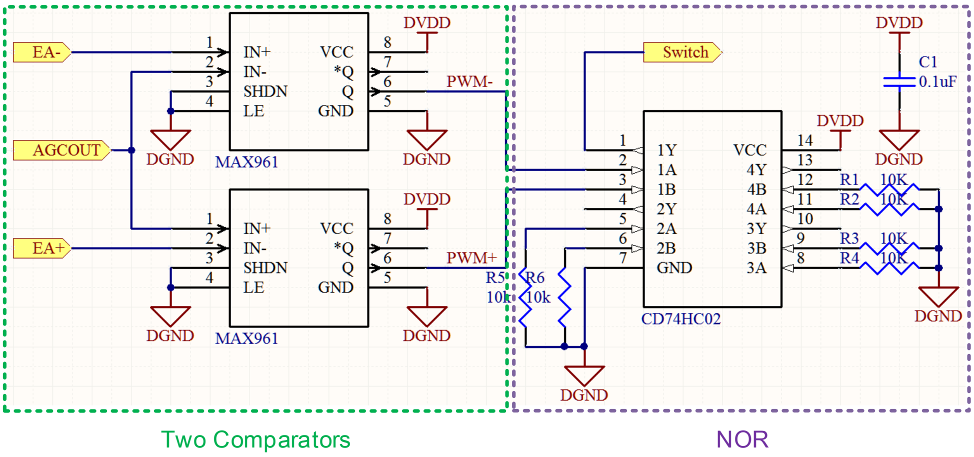


Fig.5.23 Schematic of the switch-signal generator of the proposed auto-tuning system.

The accuracy of the tuning system is affected by the accuracy for the switch control signal. As can be seen from the schematic, the accuracy of the proposed switch-signal generator relates mainly to the parameters of the comparator. The comparator used in this circuit is the MAX961, which can provide a settling time of less than 2.3 ns with a resolution of 4 mV by using 5V power supply [MAX961]. The propagation delay of MAX961 is only 8.5 ns in the worst case [MAX961]. The analysis of the phase error caused by the resolution V_R of the comparator is shown in Appendix I.

The designed PCB of the phase-error detector combined with the switch-signal generator is presented in Figure 5.24. The dimensions of this PCB are 7.2 cm × 5.7 cm.

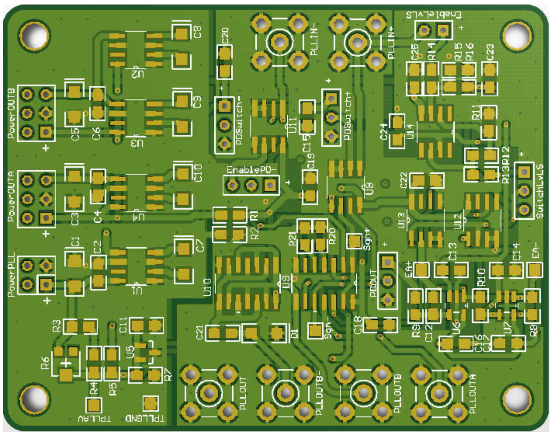


Fig.5.24 Printed circuit board of designed phase-error detector combined with switch signal generator.

5.2.4 AC switch Block

To minimize the effect of the AC switch and to isolate the drive circuit and the auto-tuning system, we used an isolated AC switch that consists of two NMOSs in a totem-pole configuration (source-to-source connected) and an isolated AC switch driver. The schematic of the designed AC switch is illustrated in Figure 5.25.

We implemented the isolated AC switch driver using a 2.5 kV isolator, ADuM5401, and a 4 A MOSFET driver, ADP3654 [ADP3654]. The maximum operation frequency of ADuM5201 is 12.5 MHz, which is higher than the working frequency (1.25 MHz) of the proposed auto-tuning system [ADuM5401]. In addition, it contains an integrated DC-to-DC converter that can provide an isolated ground to the MOSFETs. The MOSFET used in the AC switch is SI4472, which has an ultrasmall output capacitance (160 pF).

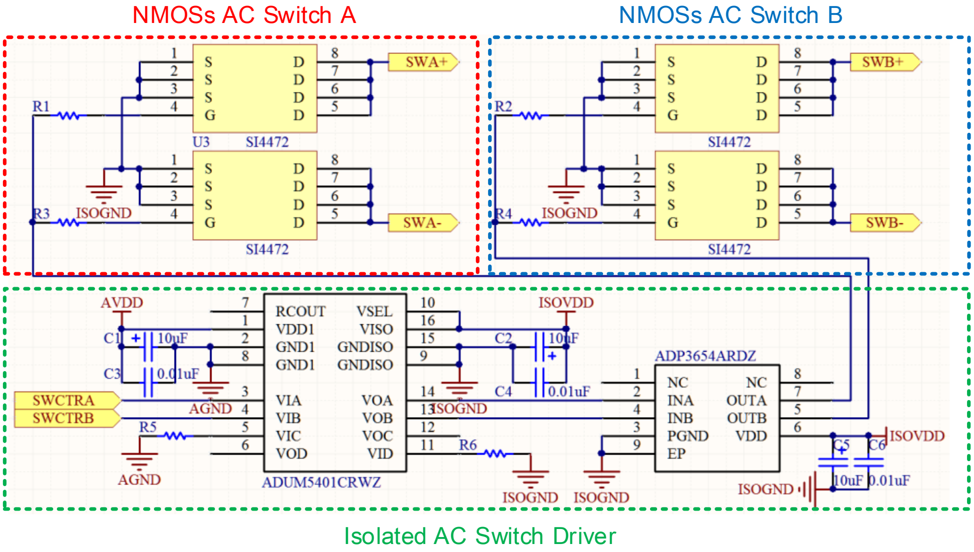


Fig.5.25 Schematic of the proposed isolated AC switch.

The PCB of the AC switch is shown in the area bounded by the blue dotted line in Figure 5.26. The proposed AC switch block contains two isolated switchs (SW_A and SW_B). SW_A is used to control the switched capacitor in the auto-tuning system, and SW_B is used to control the error capacitor used in the testing-circuit proposed in Chapter 7.

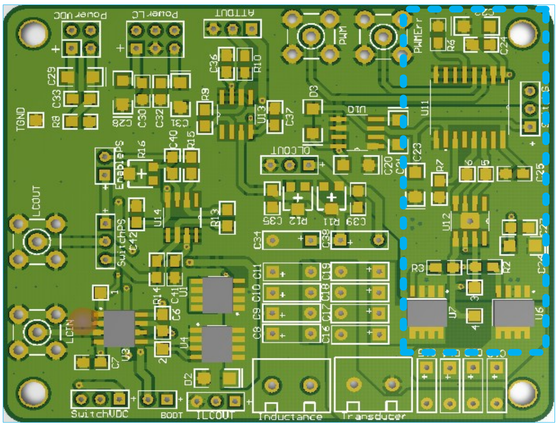


Fig.5.26 Printed circuit board of the AC switch in the area bounded by blue dotted line.

5.3 Test Results and Stability Analysis

In this section, we present the test results of each block of the auto-tuning system. Then, we also present the stability of the system.

5.3.1 Test Results of the Functional blocks

Automatic Gain Control Block

Figure 5.27 is a prototype of the AGC. We tested and verified the proposed AGC, and the test results are as follows.

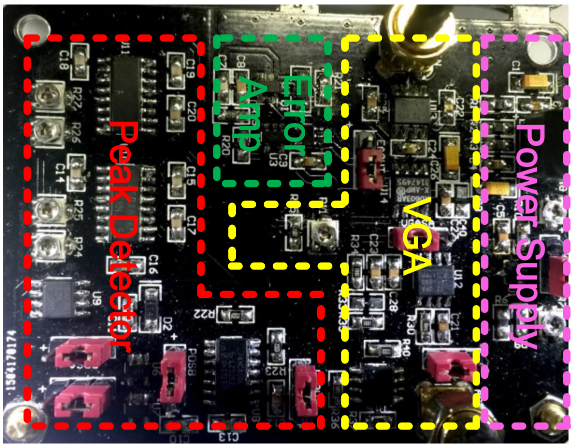


Fig.5.27 Prototype of the proposed AGC.

A recall of the Schematic of the proposed AGC with the zoom of peak detector is shown in Figure 5.28.

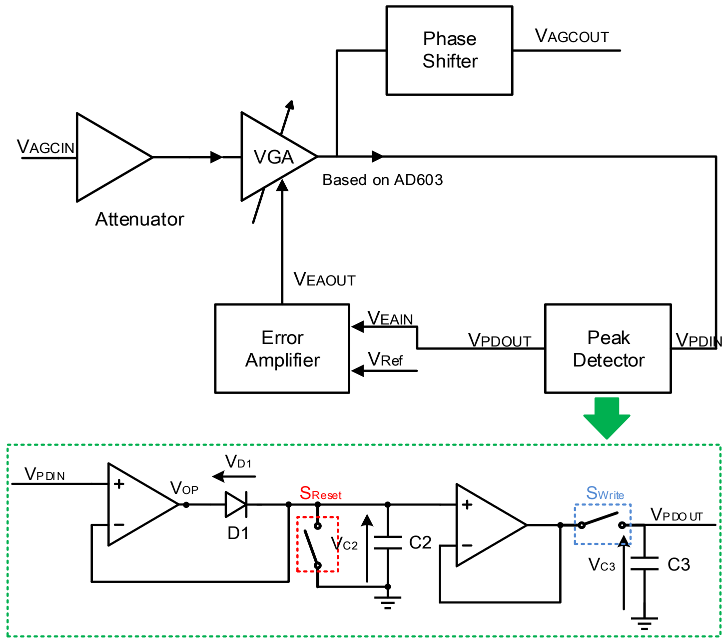


Fig.5.28 Schematic of the proposedAGC with the zoom of peak detector.

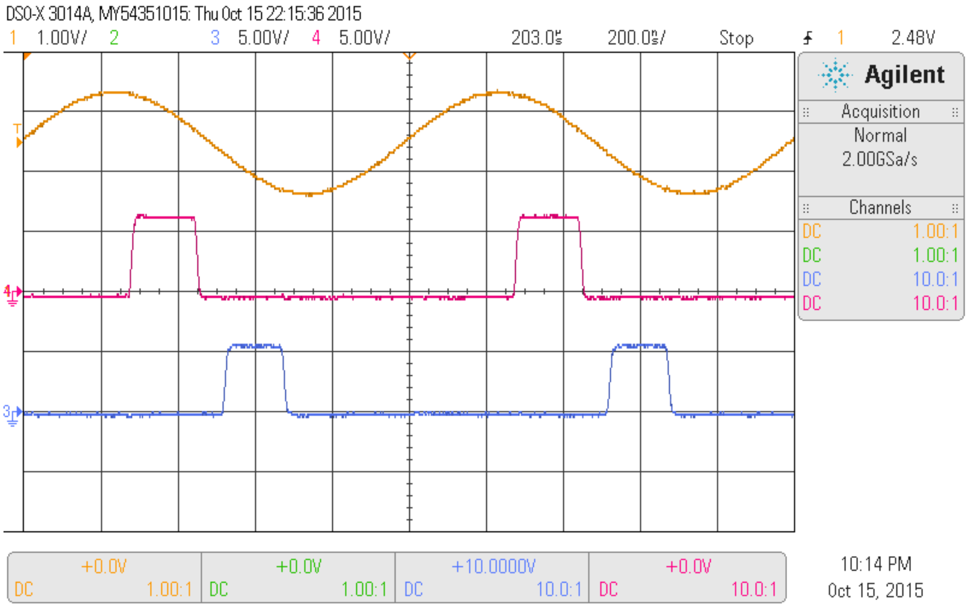


Fig.5.29 Chronograms of the switch-signal generator circuit in the peak detector.

Ch1 (*orange*): Input signal of the switch signal generator V_{PDIN}: 5V/div.

Ch3 (*blue*): Reset signal generated by the switch signal generator S_{Reset}: 5V/div.

Ch4 (*pink*): Write signal generated by the switch signal generator S_{Write}: 5V/div.

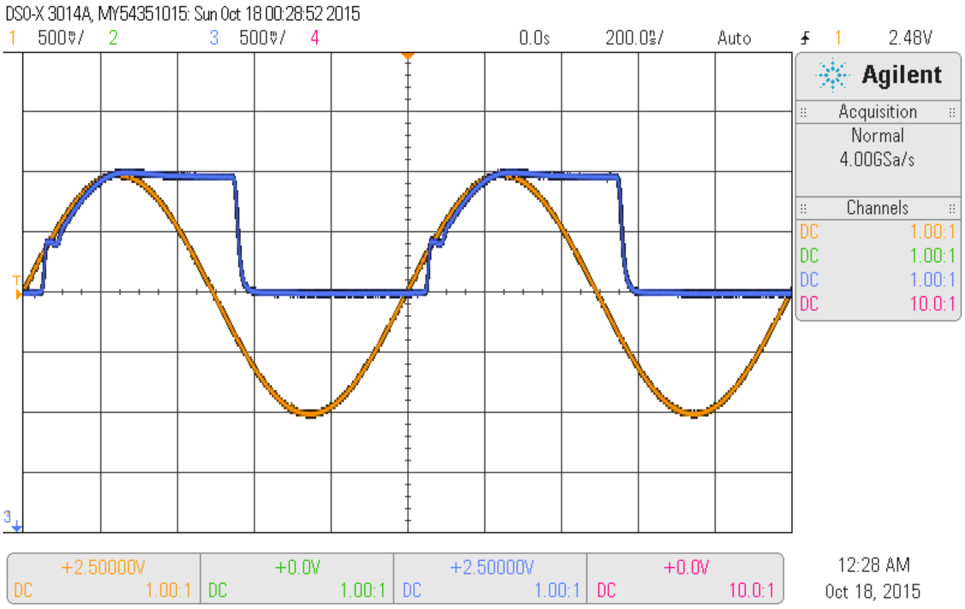


Fig.5.30 Waveform of V_{C2} in the switch signal generator.

Ch1 (*orange*): Input signal of the switch signal generator V_{PDIN}: 500mV/div.

Ch3 (*blue*): Voltage applied across capacitor (C_2) V_{C2}: 500mV/div.

Figure 5.29 shows the test results of the switch signal generator circuit in the peak detection block with a 2 V peak-to-peak input signal. The orange line is the input signal. S_{Write} is the pink line and S_{Reset} is the blue line. The orange line in Figure 5.29 is the input signal of the peak detection block, and the blue line is the voltage applied across capacitor C_2 in Figure 5.10. Figure 5.30 shows the tested waveform of V_{C2}.

Figure 5.31 is the output of the peak detector with a modulated input signal. The minimum and maximum peak-to-peak voltages of this input signal are 0.1 V and 2 V, respectively. The orange line is the input signal, and the blue line is the output signal. Two zoomed views of Figure 5.31 are demonstrated in Figures 5.32 and 5.33. By performing calculations, we found the error of the peak detector to be less than 1.5%.

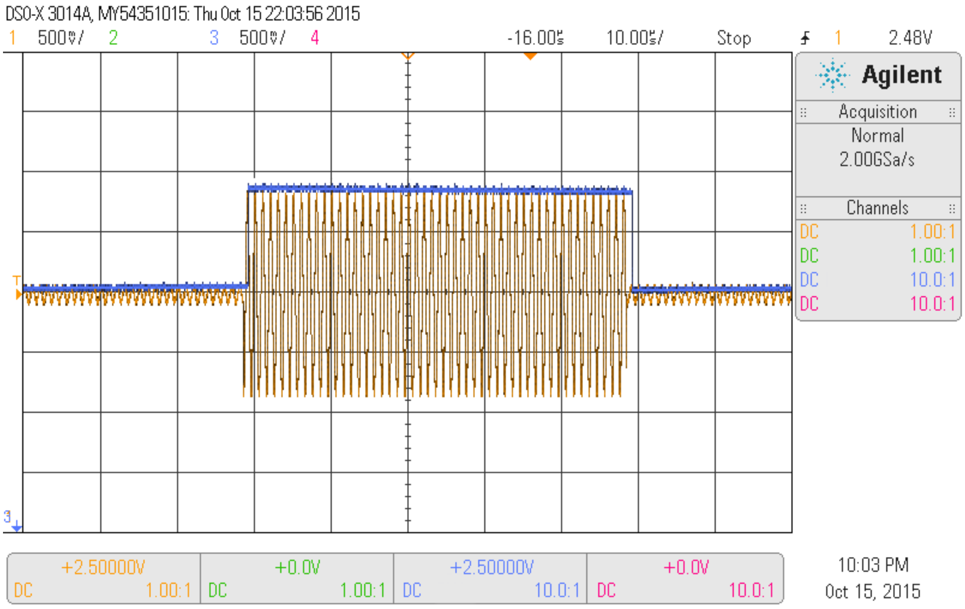


Fig.5.31 Output signal of the peak detector with a modulated input signal.

Ch1 (*orange*): Input signal of the switch signal generator V_{PDIN}: 500mV/div.

Ch3 (*blue*): Output voltage of the proposed peak detector V_{PDOUT}: 500mV/div.

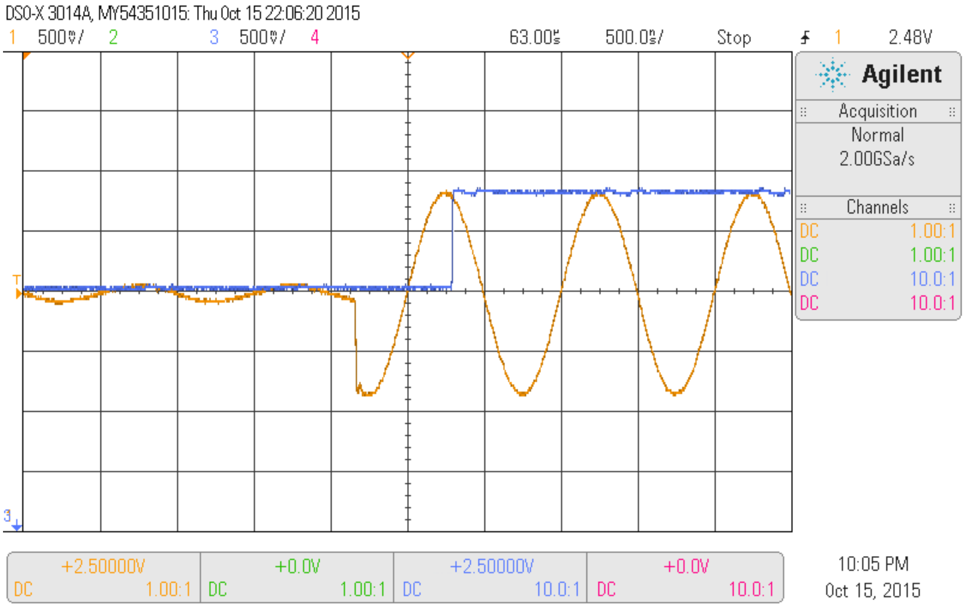


Fig.5.32 Zoomed view of the output signal of the peak detector at the rising edge.

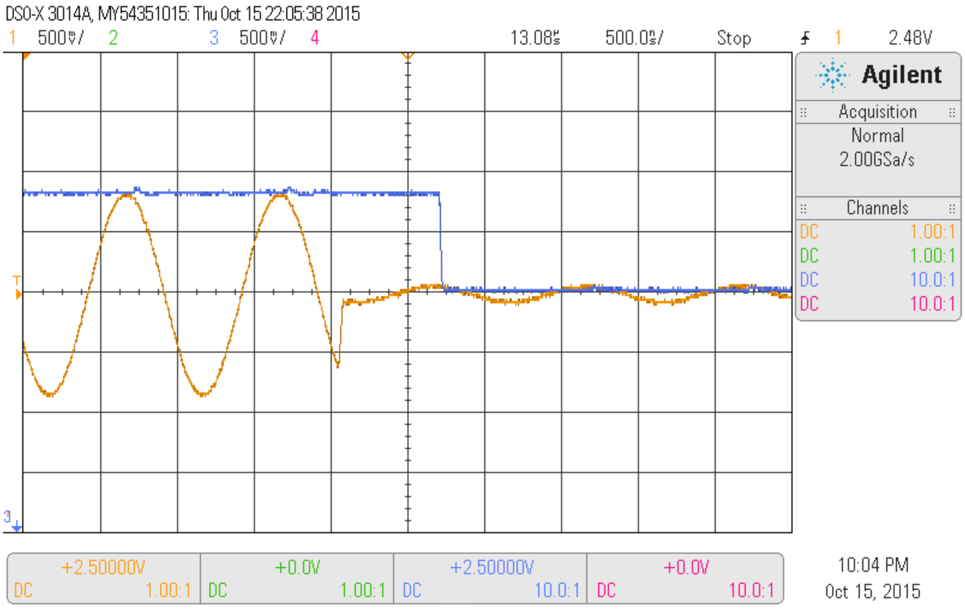


Fig.5.33 Zoomed view of the output signal of the peak detector at the falling edge.

The test result of the error amplifier in the AGC circuit is shown in Figure 5.34. The orange line is the modulated input signal and the blue line is the output signal of the error amplifier. The output voltage of the error amplifier V_{EAOUT} has a range of about 653 mV. According to the datasheet of AD603, the gain controlled by the output voltage of the error amplifier has a range of 26.12 dB. This gain tuning range is fulfil with the 20 times input ratio in our applicaton.

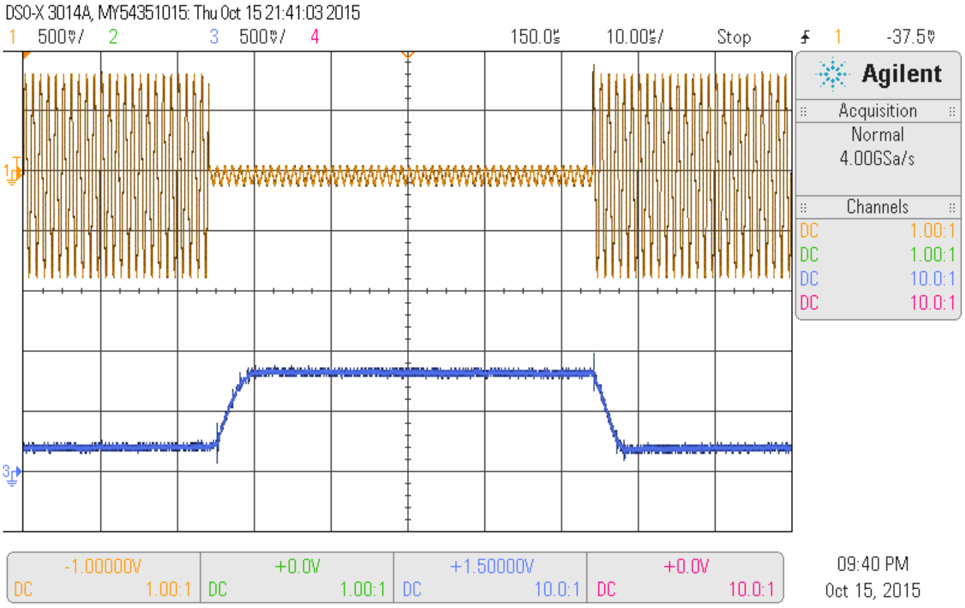


Fig.5.34 Test result of the error amplifier with a modulated input signal.

Ch1 (*orange*): Input signal of the proposed AGC V_{AGCIN}: 500mV/div.

Ch3 (*blue*): Output signal of the error amplifier used in AGC V_{EAOUT}: 500mV/div.

Figures 5.35, 5.36, and 5.37 show the test results of the AGC circuit. The blue line is the output signal of the AGC, and the pink line is the output waveform of the peak detector. The input signal of the AGC is shown as the orange line.

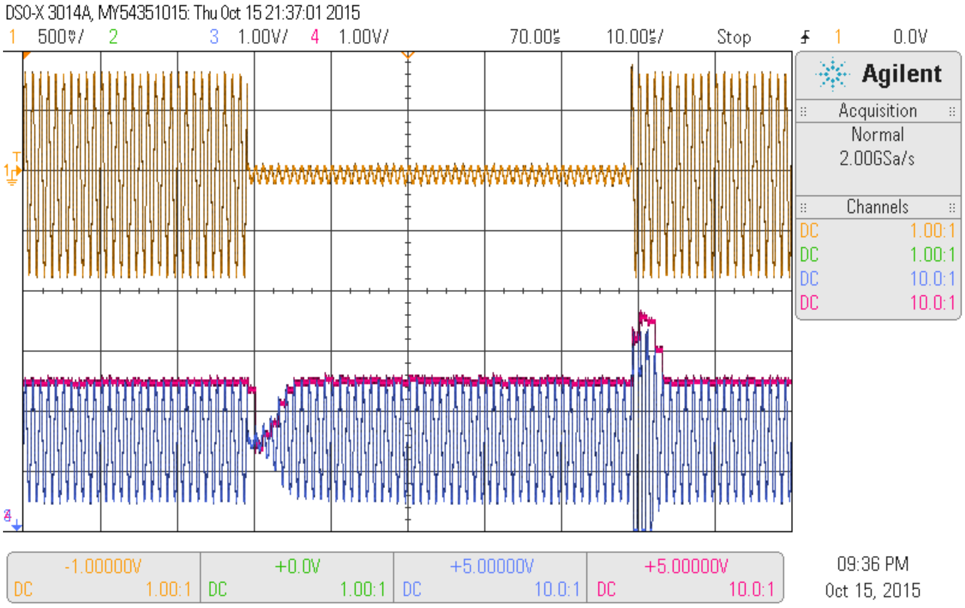


Fig.5.35 Test results of the AGC circuit with a modulated input signal.

Ch1 (*orange*): Input signal of the proposed AGC V_{AGCIN}: 500mV/div.

Ch3 (*blue*): Output voltage of the proposed AGC V_{AGCOUT}: 1V/div.

Ch4 (*pink*): Output voltage of the proposed peak detector V_{PDOUT}: 1V/div.

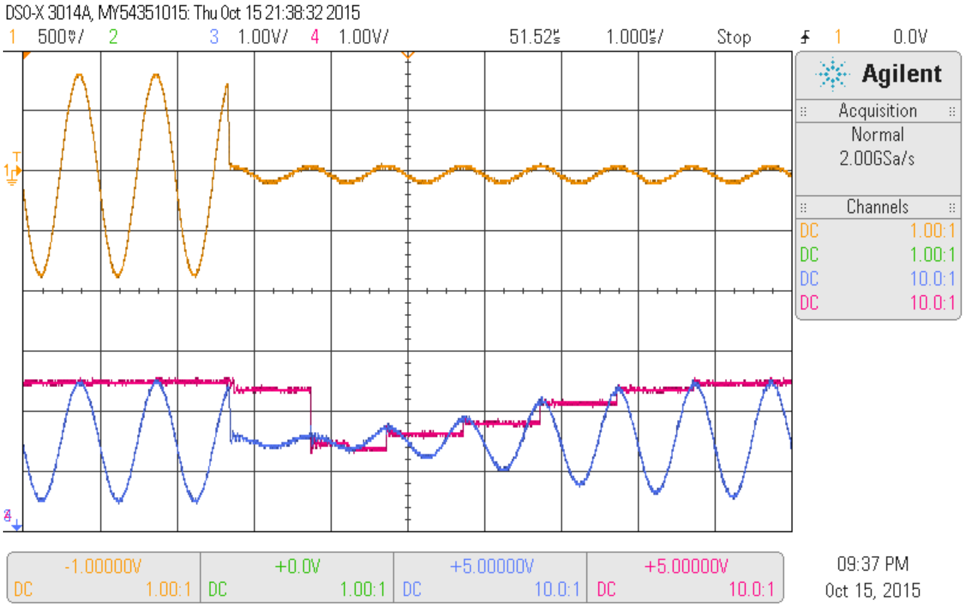


Fig.5.36 Zoomed view of test results of the AGC at the falling edge.

From Figure 5.36, we see that the settling time of the designed AGC at the falling edge of the modulated input signal equals seven periods of the input signal.

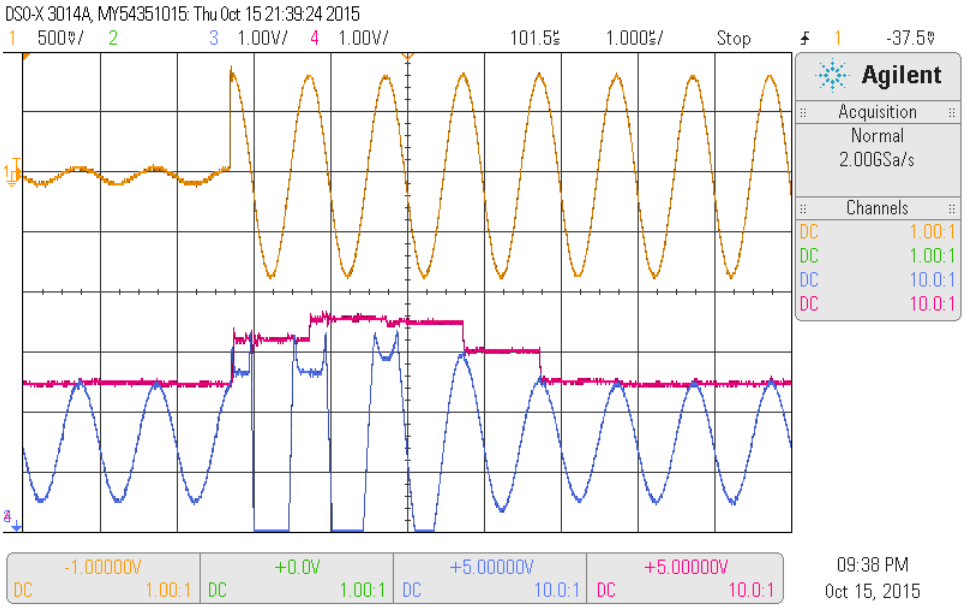


Fig.5.37 Zoomed view of test results of the AGC at the rising edge.

From Figure 5.37 we can see that the settling time of the designed AGC at the rising edge of the modulated input signal is about five periods of the input signal.

Phase Error Detection Block Combined with Switch Signal Generation Block

Figure 5.38 is a picture of the prototype of the phase-error detector combined with the switch-signal generator.

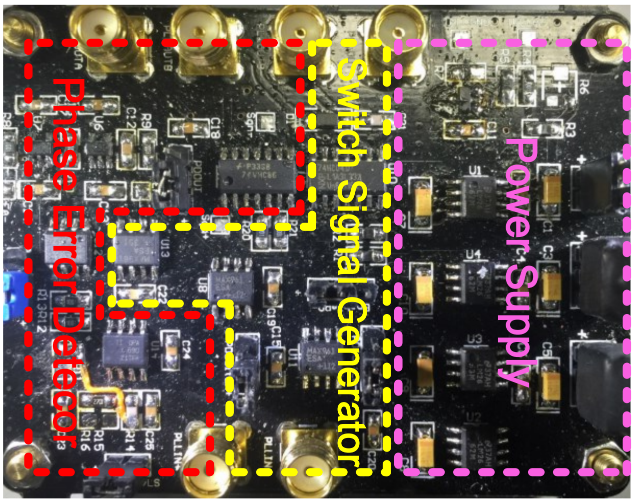


Fig.5.38 Prototype of the phase-error detector combined with switch signal generator.

A recall of the simplified schematic of the proposed phase error detection block is shown in Figure 5.39.

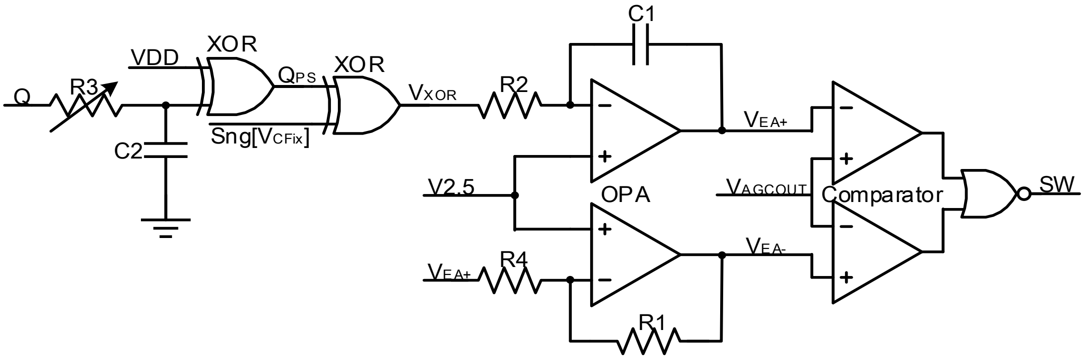


Fig.5.39 Simplified schematic of the proposed phase error detection block combined with switch signal generator.

The test results of this printed circuit board are as follows. Figure 5.40 illustrates the test results of the phase-error detector, and Figure 5.41 shows the results of the switch-signal generator.

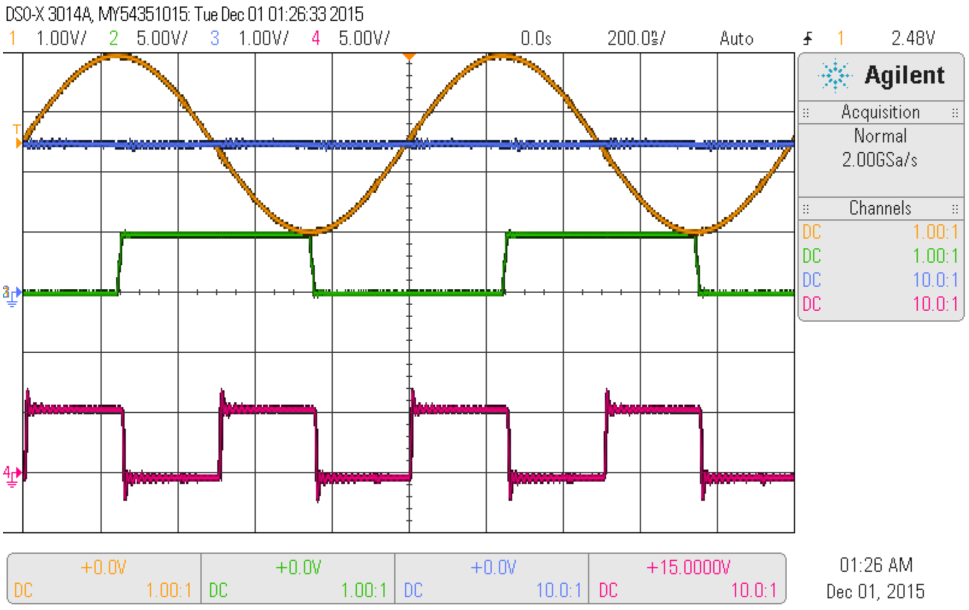


Fig.5.40 Test results of the phase-error detector.

Ch1 (*orange*): Output voltage of the proposed AGC V_{AGCOUT}: 1V/div.

Ch2 (*green*): Output voltage of the proposed phase shifter Q_{PS}: 5V/div.

Ch3 (*blue*): Output voltage of the error amplifier V_{EA+}: 1V/div.

Ch4 (*pink*): Output voltage of the XOR gate V_{XOR}: 5V/div.

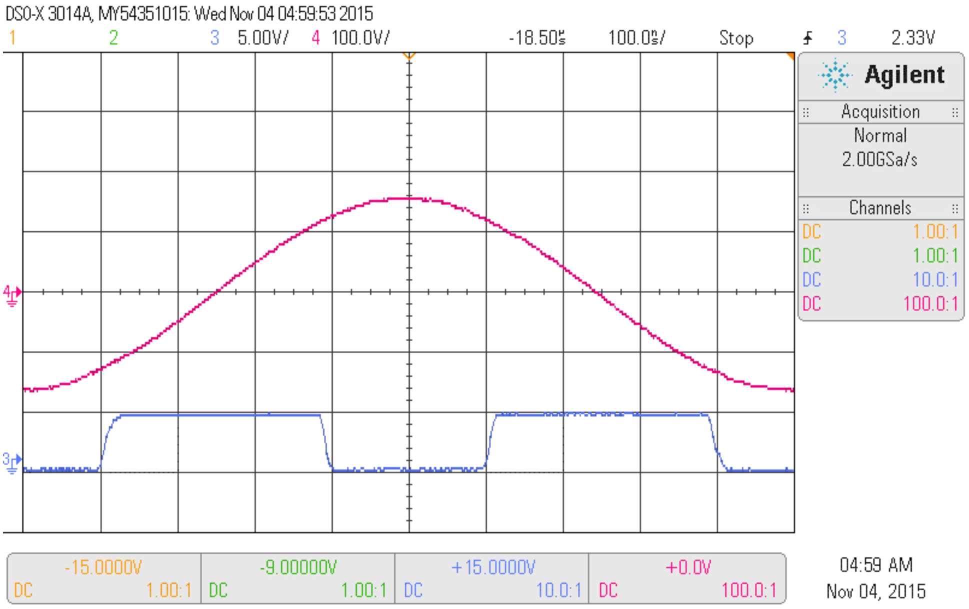


Fig.5.41 Test result of the switch-signal generator.

Ch3 (*blue*): Control signal of the switched capacitor *SW*: 5V/div.

Ch4 (*pink*): Output voltage of the power amplifier V_{CFix}: 100V/div.

As can be seen from Figure 5.40, the phase-error detector can detect the phase difference between the input signal and the output signal of the class D amplifier, and this phase difference is converted into a phase-error voltage. The phase-error voltage is equal to 2.5 V when the phase difference is $\pi/2$. From Figure 5.41, we see that the output signal of the switch-signal generator is symmetrical with respect to the zero-crossing points of the sinusoidal input voltage.

AC Switch Block

Figure 5.42 shows a picture of the prototype of the isolated AC switch bounded by the blue dotted line.

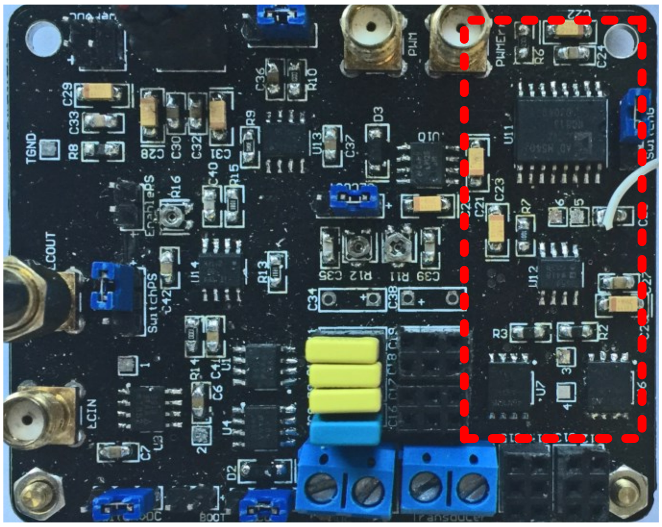


Fig.5.42 Prototype of the AC switch in the area bounded by the blue line.

The test result of the isolated switch driver is illustrated in Figure 5.43. As can be seen from this figure, the isolated switch driver has a very small delay. The delay is less than 12ns.

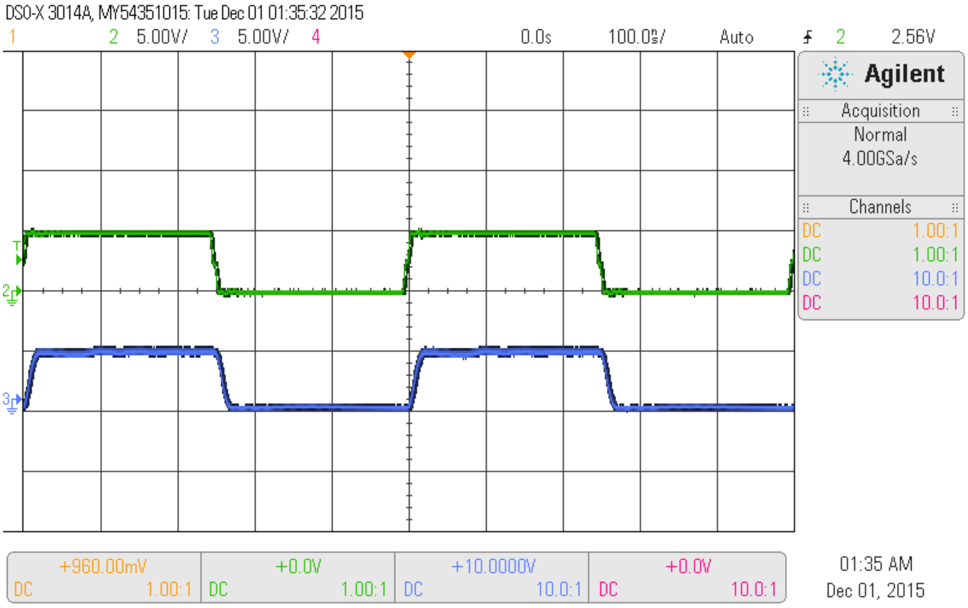


Fig.5.43 Test result of the isolated switch driver of the AC switch.

Ch2 (*green*): Control signal of the switched capacitor *SW*: 5V/div.

Ch3 (*blue*): Output voltage of the proposed isolated AC switch driver: 5V/div.

5.3.2 Stability Analysis

Based on the analysis in Section 4.2, the imaginary part of the transfer impedance has a variation of about 30%. In other words, the transducer can be considered as a constant resistor shunted with a variable capacitor. Figure 5.44 shows the equivalent circuit of the transducer.

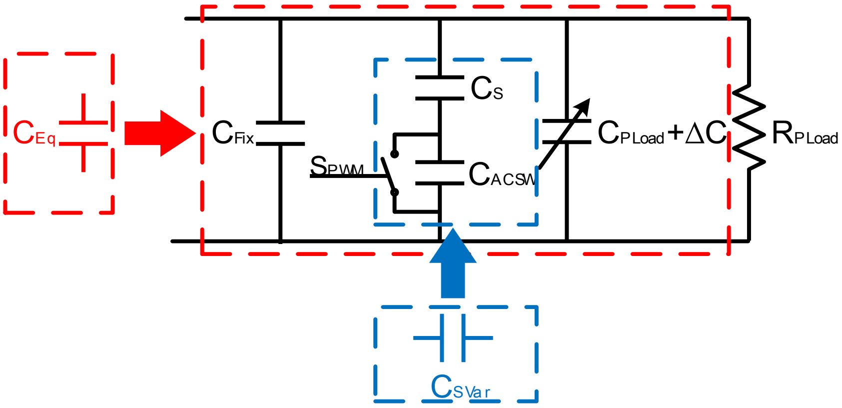


Fig.5.44 Equivalent circuit of the auto-tuning system with a variable-impedance transducer.

According to this figure, we can represent the equivalent capacitance (C_{Eq}) of the auto-tuning system combined with the transducer using the equation

$$C_{Eq} = C_{SVar} + C_{Fix} + C_{PLoad} + \Delta C \qquad 5.26$$

where

$$\frac{C_s C_{ACSW}}{C_s + C_{ACSW}} \leq C_{SVar} \leq C_s \qquad 5.27$$

As discussed in section 3.5, $C_{PLoad} = 407.3\ pF$, and we obtain the variable capacitance of the transducer as $\Delta C = 40\% \times C_{PLoad} \approx 163\ pF$. Therefore, the variable capacitance of ΔC_{SVar} must obey the following equation.

$$\Delta C_{SVar} = C_s - \frac{C_s C_{ACSW}}{C_s + C_{ACSW}} = \Delta C \qquad 5.28$$

The equivalent capacitance of the AC switch $C_{ACSW} = 2C_{OSS} = 320\ pF$. By substituting C_{ACSW} into Equation 5.28, we obtain the value of C_S as

$$C_s \simeq \frac{485+163}{2} = 324pF \qquad 5.29$$

Because of the proposed auto-tuning network is based on LC tuning circuit, we obtain the following equations.

$$f_{Working} = \frac{1}{2\pi\sqrt{L \cdot C_{Eq}}} \tag{5.30}$$

$$C_{Eq} = \frac{1}{2}\left(C_S + \frac{C_S C_{ACSW}}{C_S + C_{ACSW}}\right) + C_{Fix} + C_{PLoad} \tag{5.31}$$

In our application, $f_{Working}$ = 1.25 MHz and C_{PLoad} = *407.3 pF*; therefore, we obtain the values of C_{Fix} using

$$C_{Fix} = \frac{1}{L\left(2\pi f_{Working}\right)^2} - \frac{1}{2}\left(C_S + \frac{C_S C_{ACSW}}{C_S + C_{ACSW}}\right) - C_{PLoad} \simeq 11.36\text{n} \tag{5.32}$$

As analyzed in section 4.5, the proposed auto-tuning system can be considered as a PLL system, and the study of the stability and speed of this auto-tuning system can be simplified to a study of the stability and speed of the equivalent PLL system. The equivalent PLL circuit of the auto-tuning system is shown in Figure 5.45.

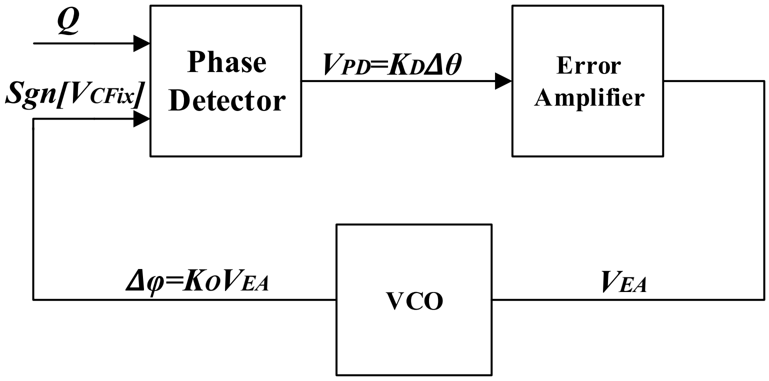


Fig.5.45 Equivalent PLL circuit of the auto-tuning system.

The open-loop transfer function of the equivalent PLL circuit is described by the following equation. The details of the derivation is presented in Appendix II.

$$G_{PLL}(jw) = K_D \cdot K_O \cdot G_{PDEA}(jw) = \frac{5}{\pi} \cdot \frac{\pi}{30} \cdot \frac{1}{jwR_2C_1} = \frac{1}{6jwR_2C_1} \tag{5.33}$$

According to this equation, this PLL system is just has one pole, the phase of the system is always equal to *π/2*, which means that it is a stable system. However, in real case, the settling time of VCO is equal to the settling time of the automatic gain control amplifier used in the proposed tuning system. In order to realize a stable tuning system, the settling time of the PLL is required to be much larger than the settling time of proposed the automatic gain control amplifier. The settling time of the proposed AGC is 6 µs which is much less than the settling time of the PLL 16.8 µs. Therefore, the proposed auto-tuning system is a stable system.

5.4 Summary of the Proposed PCB Circuits

The power supply of the proposed automatic gain control amplifier is ±5 V. The variable gain of this amplifier has a range of 26.12 dB, with a working frequency of 1.25MHz. The settling time of the proposed automatic gain control amplifier is less than 7 periods of the input signal, and its gain error is less than ±1.5 dB.

The proposed phase error detection block, switch signal generation block and AC switch use 5 V single power supply. The proposed phase error detection block allows the tuning of the system by controlling a phase difference ($\Delta\varphi = \pi/2$) between the half bridge output voltage (V_{HB}) and the voltage across the tuning capacitor (V_{CFix}). It also has the capability of transforming the phase difference between V_{HB} and V_{CFix} into a relevant voltage.

The output signal of the proposed switch signal generation block is kept symmetrical with respect to the zero-crossing points of the V_{CFix} across the fixed capacitor C_{Fix} thanks to the phase shifter and the proposed switch signal generation block. In other words, the physical impossibility of over current spikes (having theoretically an infinite intensity) flowing through the AC switch is perfectly eliminated by using the proposed circuit. Moreover, the phase error of the switch signal is less than 4 degree.

At last, for the AC switch block, a high frequency isolated AC switch is realized. The working frequency of the proposed AC switch can achieve 1.25 MHz, which fulfils our requirement.

All of the functional blocks realized by using printed circuit board meet the requirements of the proposed auto-tuning system and our application. Test results of this auto-tuning system combined with the proposed half-bridge class D amplifier will be presented in chapter 7.

Chapter 6

IC Design of the Proposed Auto-tuning

6.1 Introduction

For general HIFU applications, there are often more than 100 ultrasonic generators in a phased array. In our application, the ultrasonic phased array consists of 256 transducers. In other words, 256 auto-tuning feedback loops are required for our HIFU system. Therefore, the surface of the AGC should be designed to be as small as possible. The surface area of the PCB version of the auto-tuning system that was presented in Chapter 4 is about 110 cm^2, which is much less than that of existing auto-tuning systems. However, in our application, the need for 256 auto-tuning feedback loops implies that 256 PCBs are needed, which is still too many for our project. Further, the use of discrete components also results in wasted power. In this case, there is a real need for the design of an auto-tuning system in integrated circuits (ICs). Except the smaller circuit dimension, the using of the integrated circuit can also reduce the power consumption of the proposed auto-tuning system and enhance the performance of the circuit.

In this chapter, we present the design of an integrated automatic impedance-tuning circuit to minimize the surface area of the auto-tuning system and to reduce the power consumption. This chapter is organized as follows: In Section 6.2, we present the design of the integrated AGC circuit. In Section 6.3, we show the design of the phase-error amplifier. In Section 6.4, we illustrate the PWM circuit that was used to generate the AC switch-control signal. The design of the bandgap reference circuit is discussed in

Section 6.5. Finally, we present the pre-layout simulation results and the post-layout simulation results of the proposed integrated circuits in Sections 6.6 and 6.7 respectively. And a conclusion of this chapter is given out in Section 6.8.

6.1.1 CMOS Technology

We implemented the design of the integrated auto-tuning circuit using the 0.35 µm CMOS process 5 V kit (C35B4C3) developed by Austrian Micro Systems (AMS). In our application, the input range of the automatic gain control amplifier used in the Auto-tuning system is required to have a ratio of 20. To achieve this goal, as well as the high accuracy, we need 5 V transistors to implement the circuit. Also, taking into account the maturity of the CMOS 0.35µm and its acceptable price, we have chosen this CMOS technology.

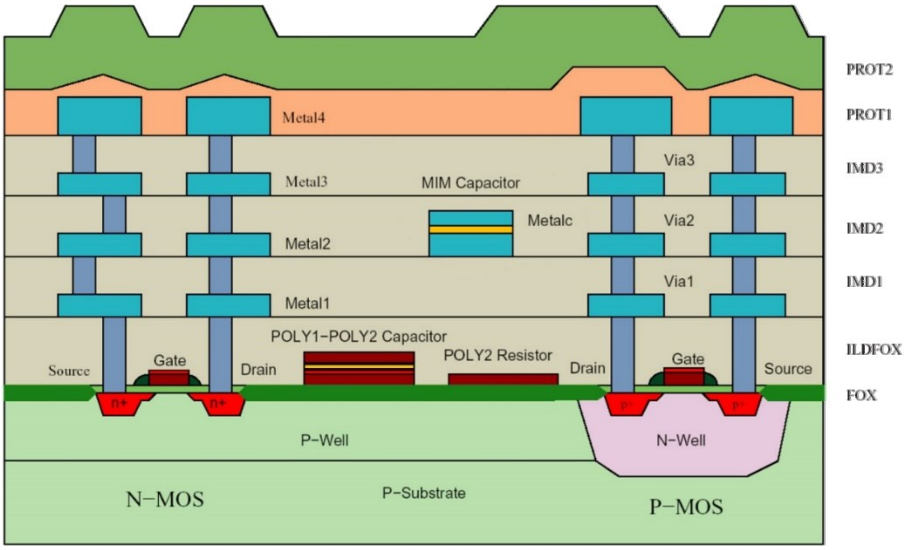


Fig.6.1 AMS C35B4C3 process (NMOS, PMOS, Capacitors, Resistors). [CMP2015]

This process is a mixed-signal CMOS process that can offer two polysilicon layers, four metal layers, 5 V transistors, and highly resistive poly. The process is demonstrated in Figure 6.1.

Table 6.1 shows parameters of the transistors, which were obtained from the datasheet.

Table 6.1 Parameters of the 5 V transistors in AMS CMOS C35B4C3 Hitkit. [CMP2015]

Parameter	*NMOS*	*PMOS*
Gain Factor	$K_N=100\mu A/V^2$	$K_P=31\mu A/V^2$
Threshold Voltage(W/L=10/10)	$0.7V$	-0.97
Threshold Voltage(W/L=10/0.5)	$0.7V$	-0.97
Body Effect Factor(W/L=10/10)	$1.05V^{0.5}$	$-0.63V^{0.5}$
Saturation Current(0.5μm)	$470\mu A/\mu m$	$-200\mu A/\mu m$

6.1.2 Development Environment

The software tools that were used to design and simulate the integrated circuit are Cadence Virtuoso® AMS Designer Environment, Spectre® Circuit Simulator and Assura® Physical Verification.

6.2 Design of the Integrated AGC

In this section, we present an integrated AGC circuit that was used for the auto-tuning system. As mentioned in the previous chapter, we have chosen a decibel linear AGC, it can therefore offer a constant settling time. As a result, the auto-tuning system can have a good response time and an excellent stability. The diagram of the proposed AGC is presented in Figure 6.2.

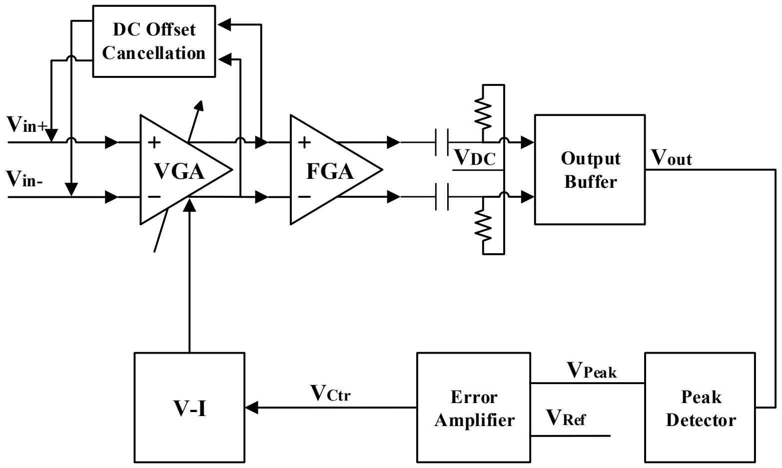


Fig.6.2 Diagram of the proposed AGC.

The proposed AGC consists of six parts: a VGA, a fixed-gain amplifier (FGA), an output buffer, a peak detector, an error amplifier, and an exponential voltage-to-current converter. The VGA and FGA are used to provide a suitable variable gain. The output buffer is applied to transfer the differential output to single-ended output, and it is also used to make sure the DC voltage of the output signal is constant. Then, we used a peak detector to detect the amplitude of the input signal. We used an error amplifier to compare this amplitude voltage with a reference voltage V_{Ref} to generate the gain-control voltage V_{Ctr}. As mentioned before, the proposed AGC must has a dB linear gain control function. Therefore, an exponential voltage to current converter is introduced to obtain a dB linear gain control function. In reality, nominally identical devices suffer from an unavoidable mismatch due to uncertainties at each step of the manufacturing process. As a result, there would be a DC-offset voltage at the outputs of the amplifier, especially in the high gain setup. The large DC-offset voltage results in signal saturation at the outputs, which prevents us from successfully obtaining the desired signal. The DC offset can also be introduced by the input signal. Therefore, there must be a DC-offset cancelling circuit for the VGA and FGA.

6.2.1 Design Specifications of AGC

In this design, the objective of the proposed AGC is to achieve a large variable-gain range with a suitable bandwidth and dB linear gain control function.

As mentioned previously, the input dynamic of the automatic gain control voltage has a ratio of 20, which means the proposed AGC is required to have a variable gain range of more than 26 dB. Moreover, the working frequency of the proposed auto-tuning system is fixed by the transcuder used, i.e. 1.25 MHz. By taking into account of these design conditions and design margin, we fixed the following specifications for the design of the AGC, as shown in Table 6.2.

Table 6.2 Design specifications of the automatic gain control amplifier.

Parameter	***Value***
Process	*AMS HitKit C35B4C3 COMS process*
Power Supply	*5 V*
Input Range	*50mV~1.5V (30 Times ratio)*
Gain Range	*0~30 dB*
-3dB Bandwidth	*5 MHz*

6.2.2 Variable Gain Amplifier (VGA)

The core cell of an automatic gain-control system is the VGA, which provides a variable gain for the AGC circuit. The diagram of the proposed VGA is illustrated in Figure 6.3. This VGA consists of three parts: an attenuation circuit, a Gilbert cell, and a DC-offset cancellation circuit.

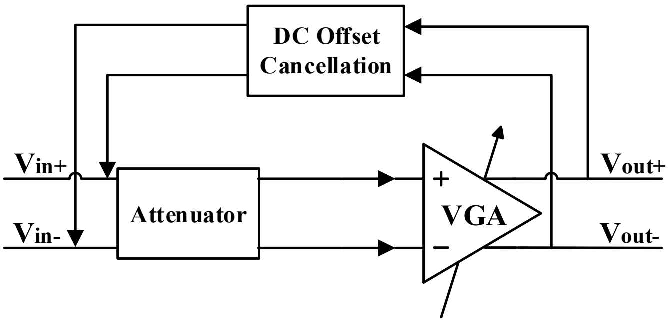


Fig.6.3 Diagram of the proposed variable gain amplifier.

The linear input range of the Gilbert cell is usually of the order of several hundreds of millivolts, and for our application, the amplitude of the input signal ranges from 50 mV to 1.5 V, which significantly exceeds the input range of the Gilbert cell. In order to fit the linear input range of the Gilbert cell, we added an attenuation block to reduce the input signal. In addition, we used a DC-offset cancellation circuit to minimize the DC offset that is caused by the mismatch of the input transistors or introduced by the input signals.

The schematic of the attenuation block is illustrated in Figure 6.4. The transistors

M9, *M10, M13*, and *M14* comprise two active attenuators. This active attenuator has a simple structure and small circuit area. *M9* and *M13* are operated in the ohmic region, and *M10* and *M14* are operated in the saturation region. If the channel-length modulation and body effect are ignored, the currents that flow through *M9* and *M10* can be described by

$$I_{M9} = \frac{1}{2}K_P\left(\frac{W}{L}\right)_{M9}\left[2(V_{in+} - V_{DD} - V_{TP})V_{DS9} - V_{DS9}^2\right] \qquad 6.1$$

$$I_{M10} = \frac{1}{2}K_P\left(\frac{W}{L}\right)_{M10}(V_{in+} - V_{o+} - V_{TP})^2 \qquad 6.2$$

where K_P and V_{TP} are the gain factor and the threshold voltage of the PMOS transistors, respectively. $(W/L)_{M9}$ and $(W/L)_{M10}$ are the width-to-length ratio of *M9* and *M10*, respectively. It can also be shown that $I_{M9} = I_{M10}$ and $V_{DS9} = VDD - V_{O+}$. By solving these equations, V_{O+} can be obtained as

$$V_{o+} = \left(1 - \sqrt{\frac{W_9L_{10}}{W_9L_{10}+W_{10}L_9}}\right)(V_{in+} - V_{DD} - V_{TP}) + V_{DD} \qquad 6.3$$

So the attenuation factor (η) of the active attenuator is described by,

$$\eta = 1 - \sqrt{\frac{W_9L_{10}}{W_9L_{10}+W_{10}L_9}} \qquad 6.4$$

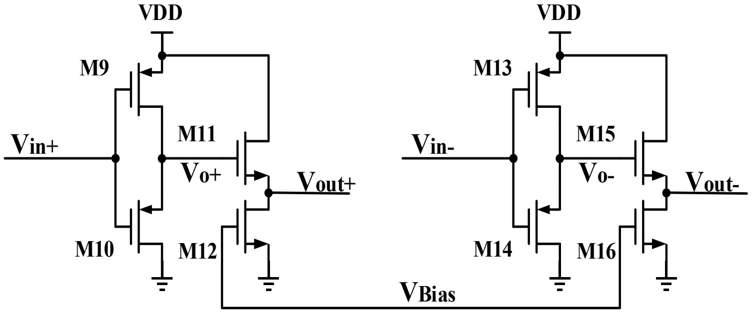


Fig.6.4 Schematic of the attenuation block.

Two NMOS source followers, which are composed of *M11*, *M12*, *M15* and *M16* are applied after the attenuators to ensure that the DC levels of V_{out+} and V_{out-} are equal to 2.5 V. The current of transistor M11 can be defined by

$$I_{M11} = \frac{1}{2}K_N\left(\frac{W}{L}\right)_{M11}(V_{o+} - V_{out+} - V_{TN})^2 \qquad 6.5$$

By solving this equation, the output voltage of the attenuation block V_{out+} is obtained as

$$V_{out+} = V_{o+} - V_{TN} - \sqrt{\frac{I_{M11}L_{11}}{K_N W_{11}}} \tag{6.6}$$

The analysis of V_{out-} is the same as that of V_{out+}, and it can be defined by

$$V_{out-} = V_{o-} - V_{TN} - \sqrt{\frac{I_{M15}L_{15}}{K_N W_{15}}} \tag{6.7}$$

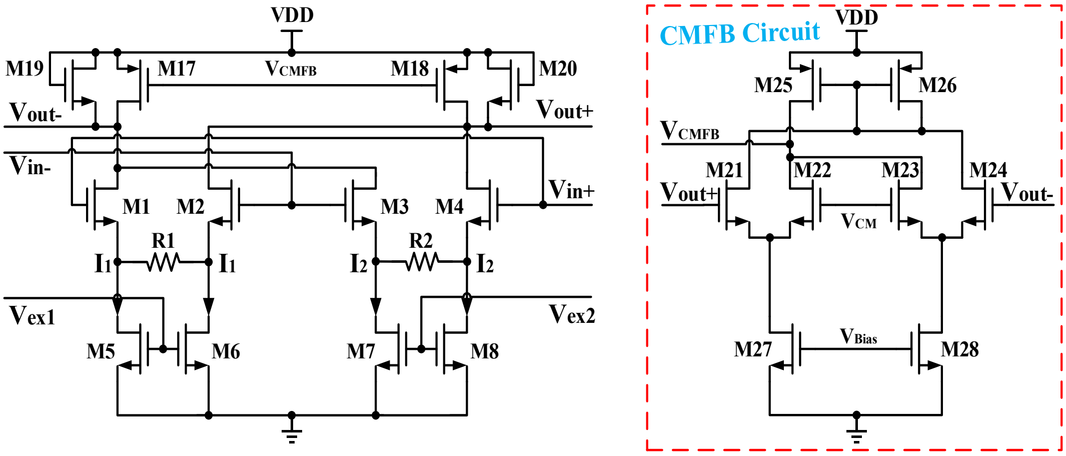


Fig.6.5 Schematic of the proposed Gilbert cell.

The core of our VGA is a Gilbert cell consisting of four identical cross-connected NMOS's (*M1, M2, M3, and M4*) as amplifying components, and two identical diode-connected NMOS's (*M19, M20*) as the load. *M1* and *M2* are driven by the same current *I1*; similarly, *M3* and *M4* are driven by *I2*. The total current is then divided equally between *M19* and *M20*. By a rough calculation, the gain of this cell is

$$A_v = \sqrt{\frac{(W/L)_{1,2,3,4}}{(W/L)_{19,20}}}\frac{1}{\sqrt{I_1 - I_2}}\left(\sqrt{2I_1} - \sqrt{2I_2}\right) \tag{6.8}$$

Therefore, it can be deduced that

$$A_v \propto \frac{1}{gm_{19,20}} \quad and \quad gm_{19,20} \propto \sqrt{I_{19,20}} \tag{6.9}$$

In order to further increase the gain, we added two constant-biased PMOS loads (*M17*, *M18*) to remove a large portion of current flowing through *M19* and *M20*. In this thesis, the currents that flow through *M17* (I_{M17}) and *M18* (I_{M18}) are chosen such that they are three times the value of the currents that flow through *M19* and *M20*. In this way, A_V is doubled.

The small dimensions of *M1~M4* and *M19* and *M20* were chosen carefully to ensure that we obtain a desired bandwidth (at least 5 MHz in our case). The pole associated with PMOS loads (*M17* and *M18*) is critical for determining the bandwidth [LTH2004]. By performing open-circuit time constant (OCTC) calculations,

$$w_P = \frac{1}{C_{gd_{(M17,18)}} \cdot r_{o(M17,18)}} \qquad 6.10$$

The resistors $R_{1,2}$ were utilized to increase the linear input range of the VGA [TCM2005]. In this way, we can improve the linearity of the VGA without losing any headroom.

The output DC level of the VGA should be stable in order to properly drive the next stage. Therefore, we require a common-mode feedback (CMFB) circuit. The schematic of the CMFB circuit for the proposed VGA is illustrated in the area bounded by the red dotted line in Figure 6.5. In the CMFB circuit, the four transistors *M21~M24* have the same width-to-length ratio. For the differential-mode input signals, the currents that flow through *M21* (I_{M21}) and *M24* (I_{M24}) have the same value, but opposite directions. Therefore, the currents of *M22* (I_{M22}) and M23 (I_{M23}) are constant, and the output voltage of the CMFB circuit V_{CMFB} is also constant. For the common-mode input signal, when the common-mode output level (V_{CMFB}) of the VGA increases, I_{M21} and I_{M24} also increase, which will lead to an increasing of the currents flowing through *M25* (I_{M25}) and *M26* (I_{M26}). However, I_{M22} and I_{M23} will decrease, which will result in an increase in the output of the CMFB circuit. Then, V_{CMFB} will decrease and vice versa. It can be seen that this common-mode signal of the VGA can be balanced with almost no effect on the differential-mode signal.

Figure 6.6 shows the DC-offset cancellation circuit used to minimize the DC offset that was caused by the mismatch of the input transistors or that was introduced by the input signals. It utilizes a feedback path from the outputs of the amplifier to its inputs with an RC low-pass filter. In order to prevent the signal from serious distortion, a much lower cut-off frequency should be designed for the low-pass filter, which requires a large capacitor in the circuit. In our thesis, we used an external capacitor to realize the low-pass filter.

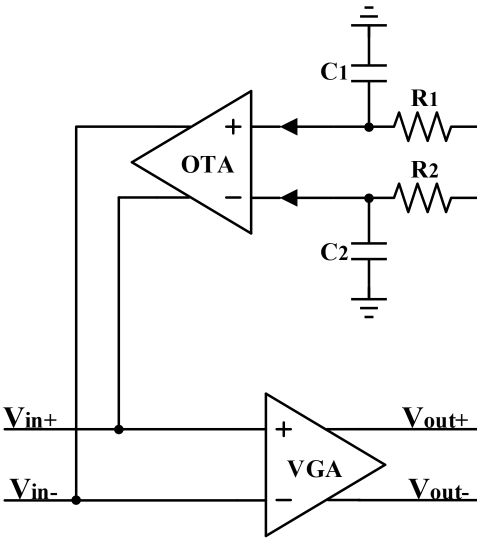


Fig.6.6 Diagram of the DC-offset cancellation circuit.

The gain of the VGA and the gain of the transconductance amplifier are defined as A and B, respectively. The transfer function of this loop can be obtained as

$$G_{DCOC}(jw) = \frac{V_{out}}{V_{in}} = \frac{1+jwRC}{1+jw\frac{RC}{1+AB}} \tag{6.11}$$

Therefore, the high-pass cutoff frequency can be written as

$$w_{HPCP} = \frac{1+AB}{RC} \tag{6.12}$$

The schematic of the differential transconductance amplifier used in the DC-offset cancellation circuit is demonstrated in Figure 6.7. It is a single-stage differential amplifier with current source loads. The CMFB circuit used in this amplifier has the same structure as the one used in the Gilbert cell. The gain of the amplifier is obtained as

$$A_v = g_{M1} r_{o1} r_{o3} \tag{6.13}$$

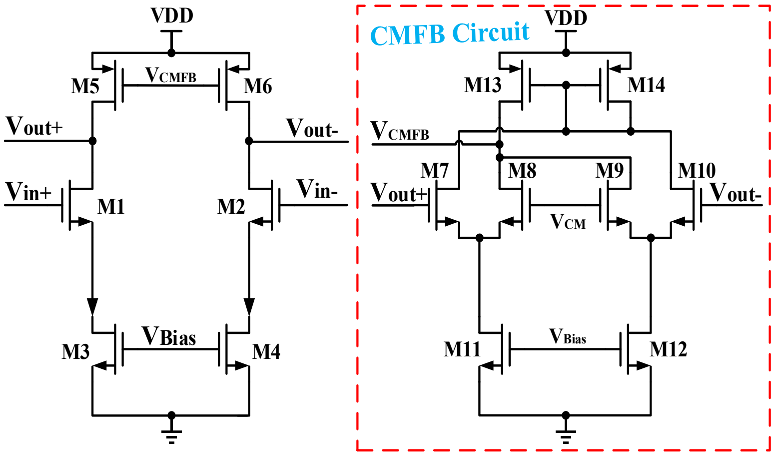


Fig.6.7 Schematic of the differential-transconductance amplifier used in the DC-offset cancellation circuit.

The layout of the proposed variable gain amplifier is presented in Appendix III.

6.2.3 Fixed Gain Amplifier (FGA)

The output range of the proposed VGA circuit is very limited because the use of the attenuator in the proposed VGA. Therefore, a FGA is necessary to enable us to amplify the output signal to the required level. To do so, we proposed an FGA with a very simple structure, as shown in Figure 6.8. The proposed FGA is an open-loop amplifier with a CMFB circuit. Although it is simple, it can provide a sufficient voltage gain for the proposed VGA to reach the required target output voltage. The width-to-length ratio of the transistors were set to $(W/L)_{M1} = (W/L)_{M2}$, $(W/L)_{M3} = (W/L)_{M4}$, and $(W/L)_{M5} = (W/L)_{M6}$, for $R_1 = R_2 = r_o$. Therefore, the gain of FGA can be written as:

$$A_v = r_o\sqrt{2I_s\mu_n C_{cox}\,(W/L)_{M1}} \qquad 6.14$$

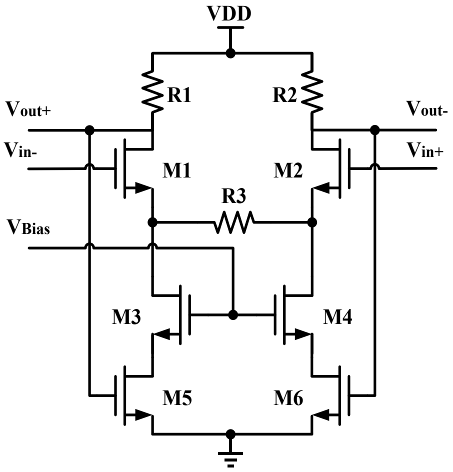


Fig.6.8 Schematic of proposed FGA.

The variable gain of the proposed VGA was set from -45.82 dB to -7.03 dB. The designed FGA has a 25 dB output gain. The gain-adjustment range of the proposed VGA combined with the FGA is from -20.82–17.97 dB. After the FGA stage, we used an AC coupling circuit to cancel the DC offset of the FGA. The layout of the proposed fixed gain amplifier is also illustrated in Appendix III.

6.2.4 Exponential Voltage to Current Converter

For our application, the amplitude of the input signal varies over a wide range. Therefore, the settling time of the AGC circuit is required to be constant. The most popular solution is the introduction of an exponential gain controller in the AGC loop.

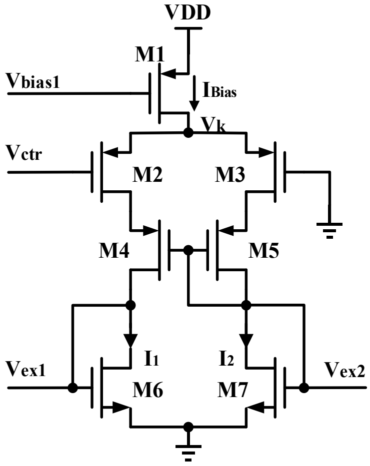


Fig.6.9 Schematic of the exponential V/I converter.

As discussed in section 5.2.1, in order to make sure the stability of the proposed auto-tuning system, the AGC circuit is required to have a dB linear gain control function. There are several existing principles to achieve the dB linear gain control function [TCM2005~CHY2001]. In this design, we use the principle proposed in [CHY2001]. It is an exponential voltage to current converter. The schematic of the circuit is shown in Figure 6.9. This circuit is chosen due to its structure and capability to tune the gain of the Gilbert cell linearly from -45.82 dB to -16.27 dB. *M3* operates in the linear region can be seen as a resistor, V_{ctr} is the input control voltage, *I1* and *I2* are the converted currents, and will be mirrored at the tail current by *M6* and *M7*. From our analysis, the relation between V_k and V_{ctr} can be roughly described as

$$V_k = k_1 V_{ctr} + k_2 {V_{ctr}}^2 \qquad 6.15$$

Therefore, when *M3* operates in the linear region, the voltage V_{SD3} can be depicted by

$$V_{SD3} = \frac{I_{Bias}}{2K_p\left(k_1 V_{ctr} + k_2 V_{ctr}^2 - |V_{Tp}|\right)} + \alpha V_{ctr} \qquad 6.16$$

where K_P is the transconductance parameter of *M3*, and α, k_1, and k_2 are proportionality factors. The currents *I1* and *I2* flowing through *M2* and *M3* can be derived by

$$I_1 = I_b/2 - \alpha K_p |V_{Tp}| V_{ctr} + \alpha k_1 K_p V_{ctr}^2 + \alpha k_2 K_p V_{ctr}^3 - V_{sd2}^2/2 \qquad 6.17$$

$$I_2 = I_b/2 + \alpha K_p |V_{Tp}| V_{ctr} - \alpha k_1 K_p V_{ctr}^2 - \alpha k_2 K_p V_{ctr}^3 + V_{sd2}^2/2 \qquad 6.18$$

Equations 6.17 and 6.18 contain Taylor's series expansion form when α, k_1, k_2, and K_P are proper. According to the Taylor theory, I1 and I2 are approximated as exponential functions with V_{ctr} [CHY2001]. The layout of the proposed fixed gain amplifier is demonstrated in Appendix III.

6.2.5 Two Phase Peak Detector

Figure 6.10 shows the schematic of the peak detector used in this paper, and which was proposed in [DGG2002P. 1, DGG2002P. 2]. It is a negative peak detector. The core of this peak detector is a current-mirror-based peak detector. However, the structure can cancel the offset of the operational amplifier (OPA) and the subsequent speed of this peak detector can be very fast.

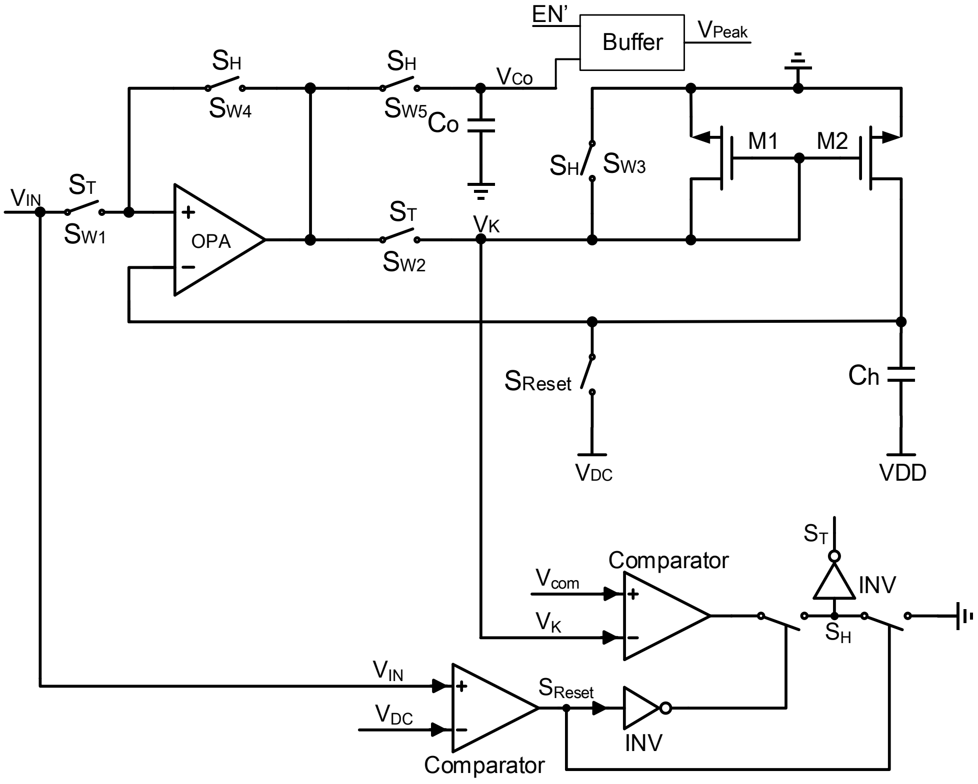


Fig.6.10 schematic of the two phase peak detector used in the proposed AGC.

This peak detector has two working phase: tracking phase and holding phase. The working principle of the two-phase peak detector can be described briefly as follows. During the tracking phase, switches S_T turn on and the other switches turn off, which makes the peak detector function as the equivalent circuit shown in Figure 6.11. The operational transconductance amplifier (OTA) supplies current to the current mirror $M1$ and $M2$. The capacitor C_h is then discharged by the current mirror. In this configuration, the circuit provides tracking, peak detection, and hold functions. The offset of the OPA is described as V_{offset}, and the stored peak voltage on C_h can be expressed as

$$V_{ch} = V_{offset} + V_{peak} \tag{6.19}$$

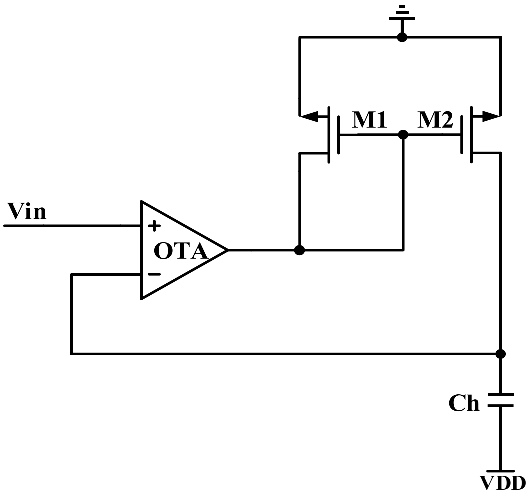


Fig.6.11 Equivalent circuit of the two phase peak detector during the tracking phase.

During the holding phase, switches S_H turn on and the other switches turn off. The equivalent circuit of the peak detector during this phase is shown in Figure 6.12. The peak detector is isolated from the input signal V_{in}. Switch S_{W3}, which is shunted with *M1*, is closed. The transistor *M1* is shorted by this switch to ensure that no leakage current flows through C_h. In this way, the voltage V_{Ch} remains unchanged. In addition, the OTA is connected as a voltage follower, with V_{Ch} as its input signal. As a result, C_o will be charged to V_{Ch}. Further, during this phase, because the OTA is used again as a voltage follower, the offset of the OTA is cancelled. The output voltage can be written by

$$V_{co} = V_{ch} - V_{offset} = V_{offset} + V_{peak} - V_{offset} = V_{peak} \quad 6.20$$

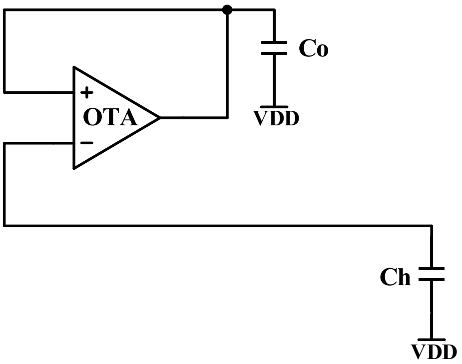


Fig.6.12 Equivalent circuit of the two phase peak detector during holding phase.

After the holding phase, a reset signal is sent to switch S_{Reset}, and the voltage of C_h is quickly reset to V_{DC}, which means that V_{Ch} is reset to V_{DC} after each period. This will give the peak detector a very fast following speed.

The switch-control signals of this two-phase peak detector are generated automatically using the voltage at the point V_k that is shown in Figure 6.10. The schematic of the switch-control signal generator is presented in Figure 6.13.

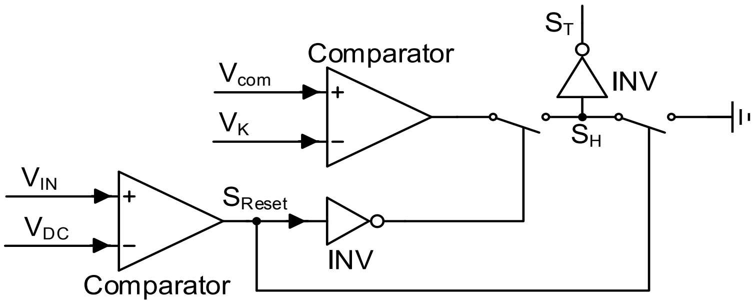


Fig.6.13 Schematic of the switch control signals generator designed for the peak detector.

Based on the analysis of the operation of the proposed two-phase peak detector, we can obtain the its chronograms, which are shown in Figure 6.14.

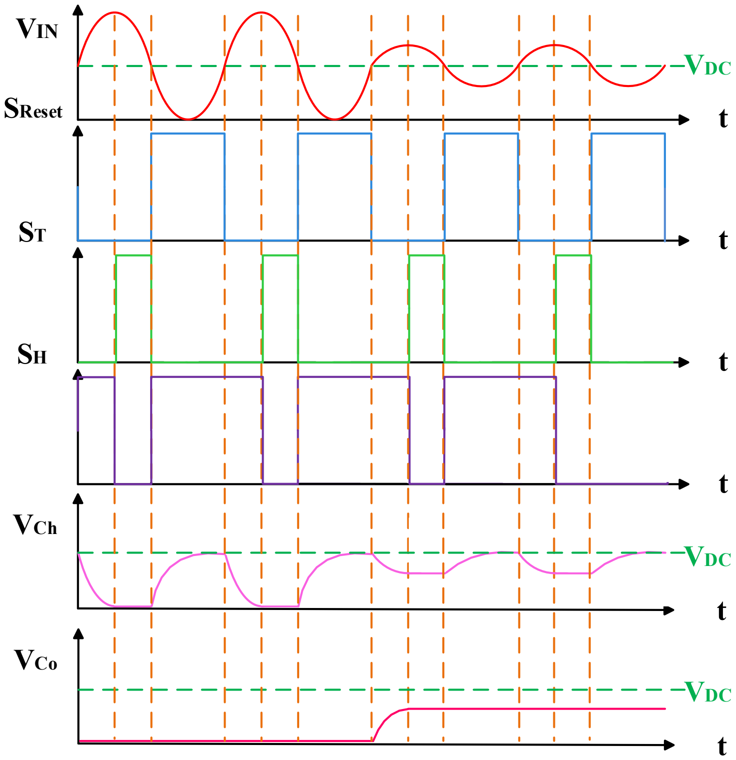


Fig.6.14 Chronograms of the two phase peak detector used in the proposed AGC.

Figure 6.15 shows the schematic of the comparator used in the switch-control signal generator. As observed from the schematic, it is a two-stage comparator with an internal hysteresis. The trip point of this comparator is

$$V'_{Trip} = V_{GS2} - V_{GS1} = \sqrt{\frac{2i_{M2}}{\mu_p C_{cox}(W/L)_{M2}}} - \sqrt{\frac{2i_{M1}}{\mu_p C_{cox}(W/L)_{M1}}} \qquad 6.21$$

By substituting $(W/L)_{M2} = (W/L)_{M1} = (W/L)$ into Equation 6.21, V'_{Trip} can be rewritten as

$$V'_{Trip} = V_{GS2} - V_{GS1} = \frac{\sqrt{2i_{M2}}-\sqrt{2i_{M1}}}{\sqrt{\mu_p C_{cox}(W/L)}} \qquad 6.22$$

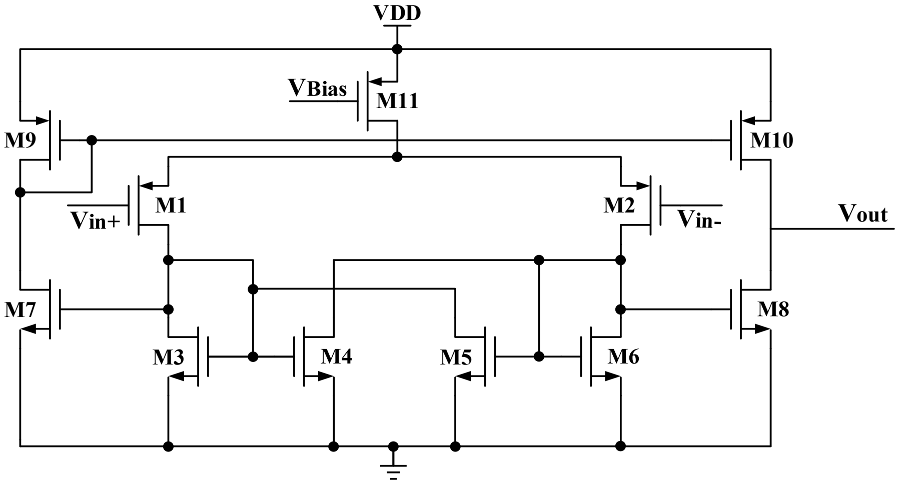


Fig.6.15 Schematic of the comparator used in the switch control signals generator of the peak detector.

The output stage of this comparator is composed of transistors M7~M10. In this way, the designed comparator can provide a class AB-type of driving capability.

The schematic of the OTA used in this peak detector is illustrated in Figure 6.16. The OTA uses the folded cascode structure because it can offer a high output gain with a wide input and output range. Moreover, this amplifier can achieve a wide bandwidth. The poles of the OTA are described by

$$P_1 = \frac{1}{C_L R_{out}} = \frac{1}{[(g_{M9}\, r_{o9}\, r_{o3})\|(g_{M7}\, r_{o7}\, r_{o1} \| r_{o5})]C_L} \qquad 6.23$$

$$P_2 = \frac{g_{M7} + g_{Mb7}}{C_{Folding}} = \frac{g_{M7} + g_{Mb7}}{C_{db1}+C_{db5}+C_{gd5}+C_{sb7}+C_{gs7}} \qquad 6.24$$

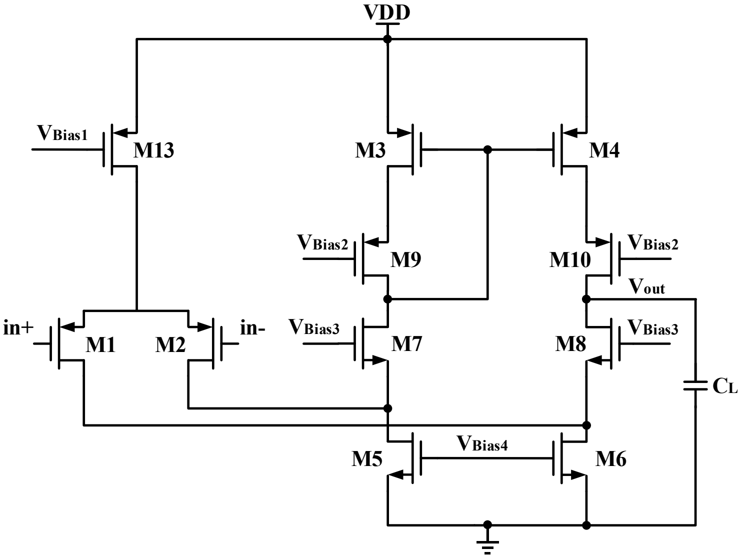


Fig.6.16 Schematic of the OTA used in the designed peak detector.

where R_{out} is the output impedance and C_L is the load capacitor of the OTA. $C_{Folding}$ defines the capacitance of the folding stage. To achieve a high-frequency characteristic, the second pole of the OTA must be far from the first pole. The gain of the amplifier can be described by

$$A_v = G_M R_{out} \simeq g_{M1}\,[(g_{M9}\, r_{o9}\, r_{o3}) \parallel (g_{M7}\, r_{o7}\, r_{o1} \parallel r_{o5})] \qquad 6.25$$

The input common-mode range is defined by the following equation.

$$V_{DS6} + V_{TN} \leq V_{IN} \leq V_{DD} - V_{SG13} - V_{SG2} - V_{TP} \qquad 6.26$$

and this amplifier has an output swing of this amplifier that presented in Equation 6.27.

$$V_{DS6(sat)} + V_{DS8(sat)} \leq V_{OUT} \leq V_{DD} - V_{DS4(sat)} - V_{DS10(sat)} \qquad 6.27$$

Depending on the bandwidth and slew rate requirements, the current flowing through each branch can be estimated. Based on the estimated current, the width-to-length ratios of the transistors can be calculated by

$$I_D = \frac{1}{2}\mu_n C_{cox}\frac{W}{L}(V_{GS} - V_{TH})^2 \qquad 6.28$$

The layout of the proposed peak detecotr is shown in Appendix III.

6.2.6 Output Buffer

Because the output signal of the FGA is a differential signal, we require an output buffer to transfer this differential output into a single ended output. The diagram of the output buffer is illustrated in Figure 6.17.

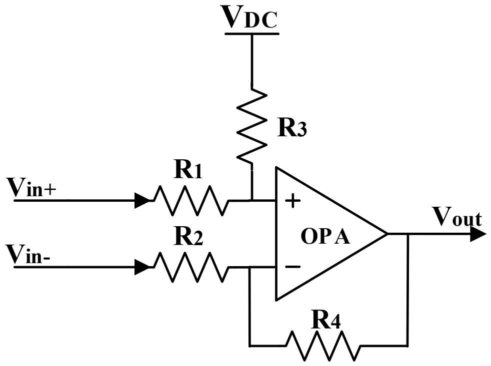


Fig.6.17 Diagram of the output buffer.

The DC level of the output signal is fixed by V_{DC}, which in our case is equal to 2.5 V. In this output buffer, $R_1 = R_2 = r$, and $R_3 = R_4 = 4r$. Therefore, this output buffer can also provide a 12-dB output gain. The total gain of the AGC then ranges from -8.82 dB to 29.97 dB.

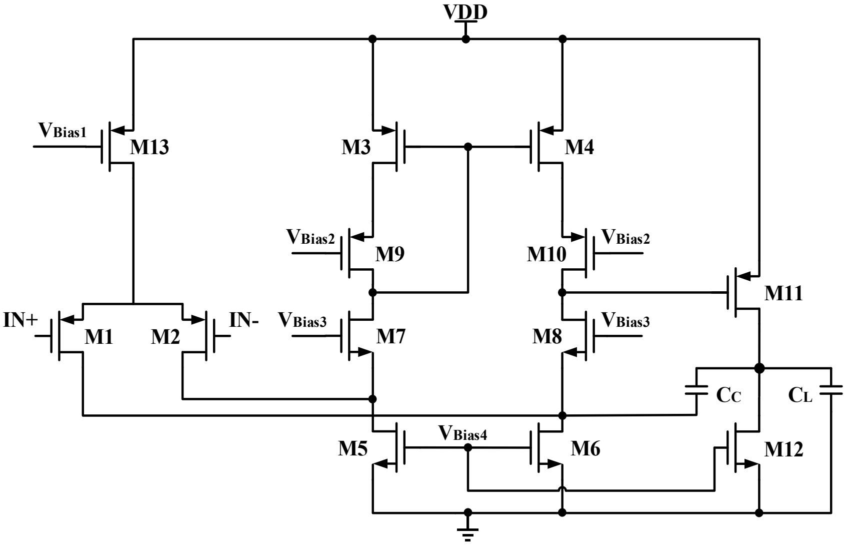


Fig.6.18 Schematic of the OPA used in the output buffer.

The schematic of the OPA used in the output buffer is presented in Figure 6.18. It is a two-stage folded cascade amplifier. The first stage of this OPA has the same structure as the OTA used in the designed peak detector. Further, the analysis of the first stage is the same as discussed in Section 6.25. The second stage of the amplifier is a common-source PMOS amplifier with an NMOS current source load. The gain of the second stage can be described by

$$A_{v2} = G_M R_{out} = g_{M11}\,(r_{o11} \parallel r_{o12}) \qquad 6.29$$

The output swing of this stage can be written as

$$V_{DS12(sat)} \leq V_{OUT} \leq V_{DD} - V_{DS11(sat)} - V_{DS12(sat)} \qquad 6.30$$

In order to ensure the stability of the amplifier, we added a Miller capacitor *Cc* between the first and second stages in order to improve the phase margin of the amplifier. The poles of the designed OPA can be described by

$$P_1 = \frac{1}{[(g_{M9}\, r_{o9}\, r_{o3}) \parallel (g_{M7}\, r_{o7}\, r_{o1} \parallel r_{o5})] C_c A_{v2}} \qquad 6.31$$

$$P_2 = \frac{g_{M12}}{C_L} \qquad 6.32$$

The layout of the proposed output buffer is presented in Appendix III.

6.2.7 Error Amplifier of the AGC

The simplified schematic of the error amplifier used in the proposed AGC is shown in Figure 6.19. The peak detector used in the AGC is a negative peak detector, and therefore, the error amplifier designed for the AGC is a positive integrator. In this integrator, $R_1 = R_2 = R$ and $C_1 = C_2 = C$.

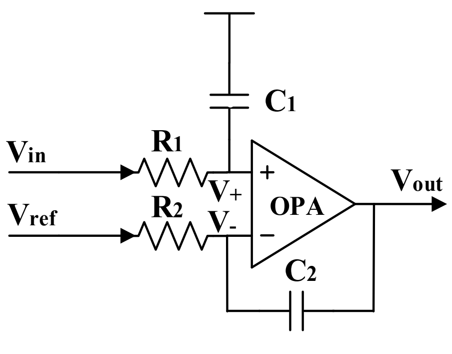


Fig.6.19 Simplified schematic of the error amplifier used in the AGC.

The voltage of the capacitor C_1 is defined as V_{C1}. If the input signal V_{in} is not equal to V_{ref}, C_1 is charged by the current (I_{R1}) that flows through R_1. I_{R1} can be described by

$$I_{R1} = \frac{V_{in} - V_{C1}}{R_1} \qquad 6.33$$

Then, the equation of V_{C1} can be obtained as

$$V_{C1} = \frac{1}{C_1}\int I_{R1}dt = \frac{1}{R_1C_1}\int (V_{in} - V_{C1})dt \qquad 6.34$$

and this equation can be rewritten as

$$V_{C1} + \frac{1}{R_1C_1}\int V_{C1}dt = \frac{1}{R_1C_1}\int V_{in}dt \qquad 6.35$$

According to the "virtual short" of the amplifier, $V_- = V_+ = V_{C1}$. The current flowing through R_2 (I_{R2}) is equal to $(V_{C1} - V_{ref})/R_2$. The voltage across C_2 is defined as

$$V_{C2} = \frac{1}{C_2}\int I_{R2}dt = \frac{1}{R_2C_2}\int \left(V_{C1} - V_{ref}\right)dt \qquad 6.36$$

The output voltage of the error amplifier is obtained as

$$V_{out} = V_+ + V_{C2} = V_{C1} + \frac{1}{R_2C_2}\int \left(V_{C1} - V_{ref}\right)dt \qquad 6.37$$

By substituting Equation 6.33 into Equation 6.35, V_{out} can be redefined as

$$V_{out} = \frac{1}{RC}\int \left(V_{in} - V_{ref}\right)dt \qquad 6.38$$

The output voltage of the error amplifier is related to the difference between its input signal and the reference voltage. As discussed in our analysis in chapter 5, the values of R and C must be carefully chosen to guarantee the stability of the AGC circuit. As calculated in section 5.2.2, the capacitance of C is about few nF, which is too large to be realized by using integrated circuit. Therefore, this capacitor is realized by using out-chip component.

The layout of the proposed error amplifier used in the AGC is shown in Appendix III.

6.3 Integrated Phase-error Detector

6.3.1 Design of the Phase-error detector

As shown in Figure 6.20, the phase-error detector circuit consists of two parts: a phase-difference detector circuit and an error amplifier. In the phase-difference detector circuit, we first use a comparator to compare the input signal with its DC voltage V_{DC} in order to obtain its sign signal. Then, we used an XOR gate to obtain the phase difference of this sign signal and the clock signal.

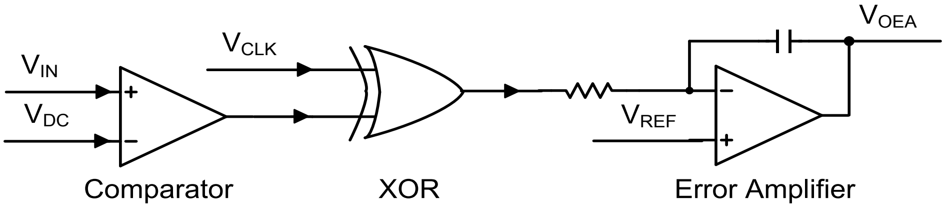


Fig.6.20 Diagram of the phase error detect circuit.

Next, to generate a phase error signal, we used an error amplifier to compare the phase-difference signal with a reference voltage, which represents a $\pi/2$ phase difference.

To guarantee the stability of the system, the error amplifier needs to be carefully designed. The settling time of the phase-error amplifier needs to be larger than the settling time of the AGC. Based on the calculation, the capacitance of the capacitor used in the error amplifier is a few nF, which is too large to be realized using an IC, so we used an out-chip capacitor here. The comparator used in this circuit is the same as that used in the switch-control signal generator of the two-phase peak detector. The layout of the phase error detector is shown in Appendix III.

6.4 Integrated Switch Signal Generator

6.4.1 Schematic Design of the Switch Signal Generator

The diagram of the switch signal generator of the auto-tuning system is presented in Figure 6.21.

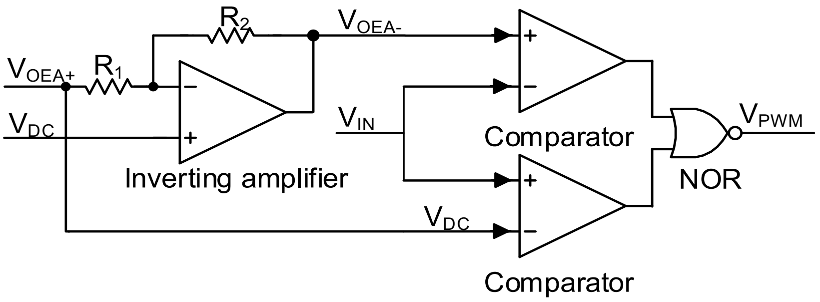


Fig.6.21 Diagram of the Switch signal generator.

The proposed Switch signal generator is composed of two comparators and a unity-gain voltage inverter. In this circuit, we used the comparator proposed in [FPM2004] because of its small delay, high resolution, and simple structure.

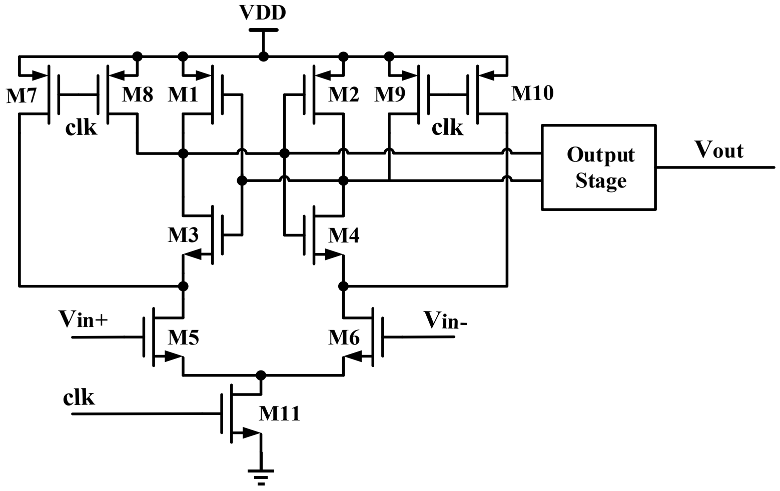


Fig.6.22 Schematic of comparator used in this paper.

As can be seen from Figure 6.22, the comparator is composed of three stages, a preamplifier, latch stage, and output stage. The maximum clock frequency of the comparator used in this paper can reach 100 MHz, and the transit delay is approximately 2.5 ns; its resolution is 0.5 mV. Therefore, by using this comparator, the auto-tuning circuit can have a very high accuracy. The phase error caused by the resolution of the comparator is presented in Appendix I. In this thesis, we use an external clock signal as the control signal (clk) of the latch stage, the frequency of the external signal is chosed to be ten times as the output signal of the AGC.

6.5 Bandgap Voltage and Current Reference Circuit

6.5.1 Schematic Design of the Bandgap Reference Circuit

We used the bandgap reference circuit to provide a temperature-independent power supply to the designed IC. The principle of the bandgap voltage reference is to balance the negative temperature coefficient of the temperature PN junction (V_{BE}) with the positive temperature coefficient of the thermal voltage, $V_t = kT/q$. Figure 6.23 illustrates the general principle of the bandgap reference circuit. The reference voltage of the bandgap circuit is described by

$$V_{Ref} = V_{BE} + KV_t \qquad 6.39$$

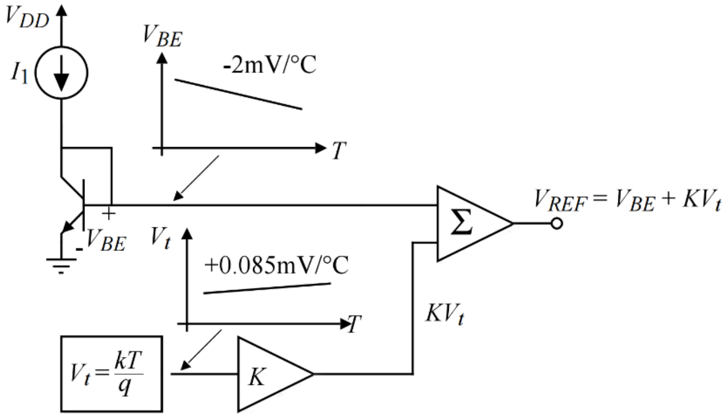


Fig.6.23 General principle of the bandgap reference circuit [RB2002].

The CMOS technology that was used in our project has only a substrate PNP bipolar-junction transistor (BJT). The schematic of the CMOS bandgap reference that used this kind of bipolar transistor is shown in Figure 6.24.

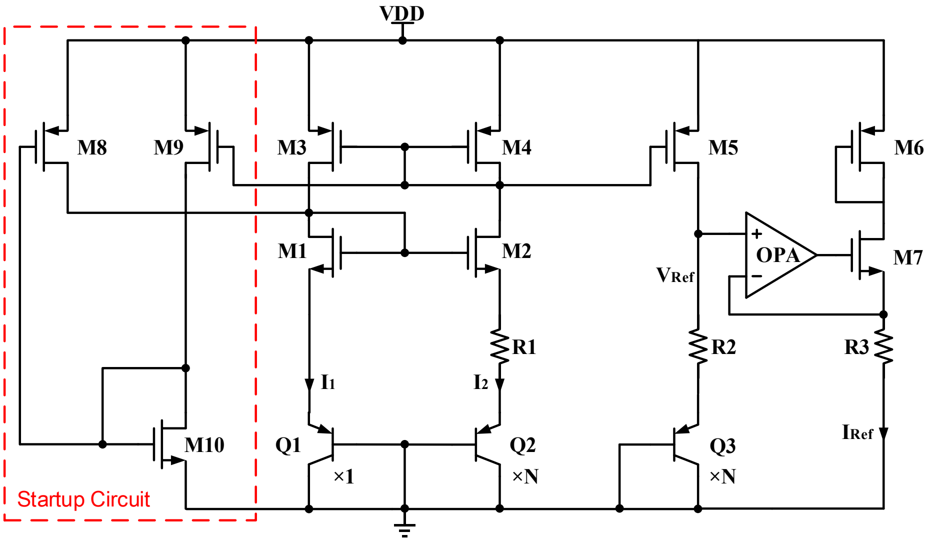


Fig.6.24 Schematic of the bandgap voltage and current reference circuit.

The current mirror (*M3*, *M4*) maintains the identical currents in BJTs *Q1*, *Q2*, and *Q3*. Thus, we obtain the following equations:

$$V_{BE1} = I_2 R_1 + V_{BE2} \qquad 6.40$$

$$I_2 = \frac{V_t}{R_1} ln(N) \qquad 6.41$$

Therefore, the output reference voltage (V_{Ref}) of this bandgap circuit can be written as

$$V_{Ref} = V_{BE3} + I_2 R_2 = V_{BE3} + \frac{R_2}{R_1} V_t ln(N) \qquad 6.42$$

The desired value of *K* in Equation 6.39 can be achieved by carefully designing R_1, R_2, and *N*. Then, we used an OPA to generate I_{Ref} from V_{Ref}. The equation of I_{Ref} is

$$I_{Ref} = \frac{V_{Ref}}{R_3} \qquad 6.43$$

The OPA used in this circuit is the same as the one used in the output buffer. The bandgap circuit requires a startup circuit to ensure that the circuit is not stuck at its “zero” operating point. The designed startup circuit is presented in the area bounded by the red dotted line in Figure 6.24. The designed bandgap voltage and current reference circuit can operate with a supply voltage between 3 V~5 V, and at temperatures between -20°C and 100°C. The designed circuit can generate a 1.222-V reference voltage and a 50-µA reference current with a maximum temperature coefficient of 15 ppm/°C.

6.6 Pre-layout Simulation Results

The proposed auto-tuning system was designed using AMS CMOS 0.35 μm technology. For a voltage supply of 5 V, the simulation results are given below.

6.6.1 Automatic Gain Control Circuit

The DC characteristics of the proposed Gilbert cell without the attenuation block are illustrated in Figure 6.25. As observed in the figure, the linear input range of the VGA without the attenuation block is -150 mV to 150 mV.

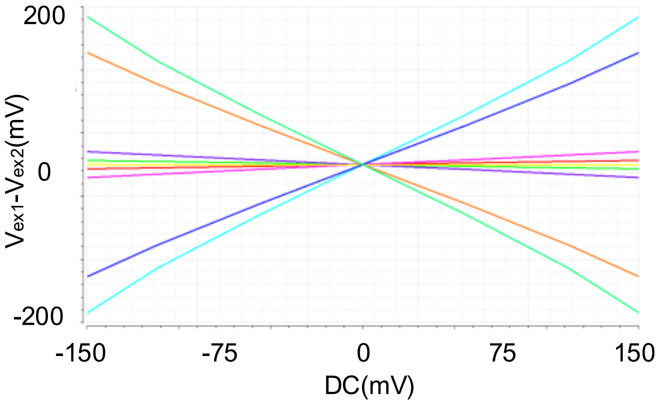


Fig.6.25 Direct transfer characteristics of the designed VGA without attenuators.

Figure 6.26 shows the DC characteristics of the VGA with the attenuation block, and we can see that the linear input range of the VGA is further extended by the attenuation block, which ranges from -1.5 V to 1.5 V.

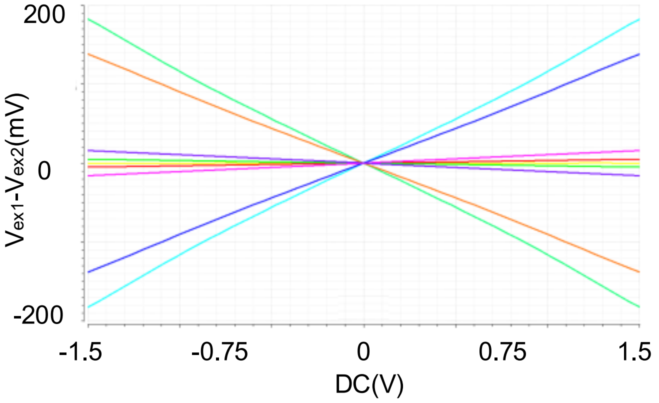


Fig.6.26 Direct transfer characteristics of the designed VGA combined with attenuation block.

The frequency response of the proposed VGA with the DC-offset cancellation (DCOC) circuit is illustrated in Figure 6.27. As can be seen from this figure, the VGA provides a variable gain that ranges from -45.82 dB to -7.03 dB with a -3 dB bandwidth from 37 kHz ~ 54 MHz. In addition, the DC gain of the VGA is from -52 dB to -36 dB, which means that the DC offset is well decayed by the DCOC circuit.

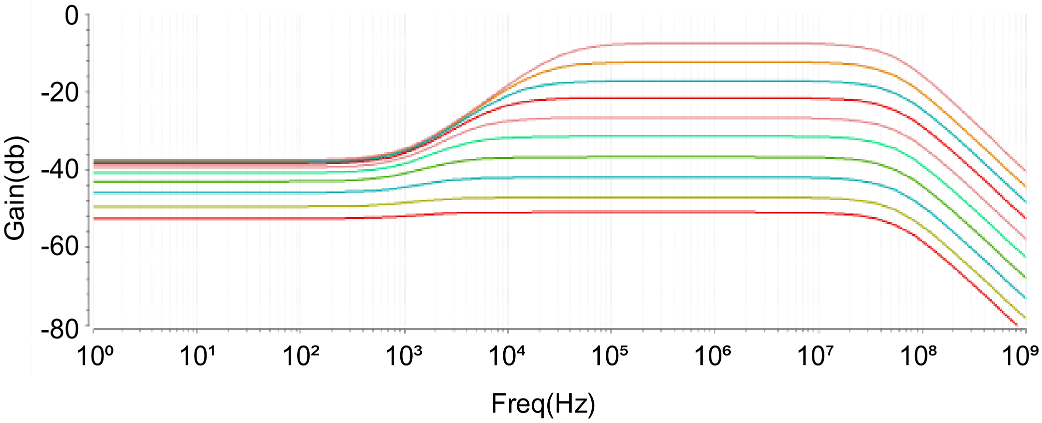


Fig.6.27 Frequency response of the designed VGA with the DCOC circuit.

Figure 6.28 shows the frequency characteristics of the proposed FGA. The bandwidth of this FGA is 2.79 GHz with a 78° phase margin. It can offer a 25 dB fixed gain.

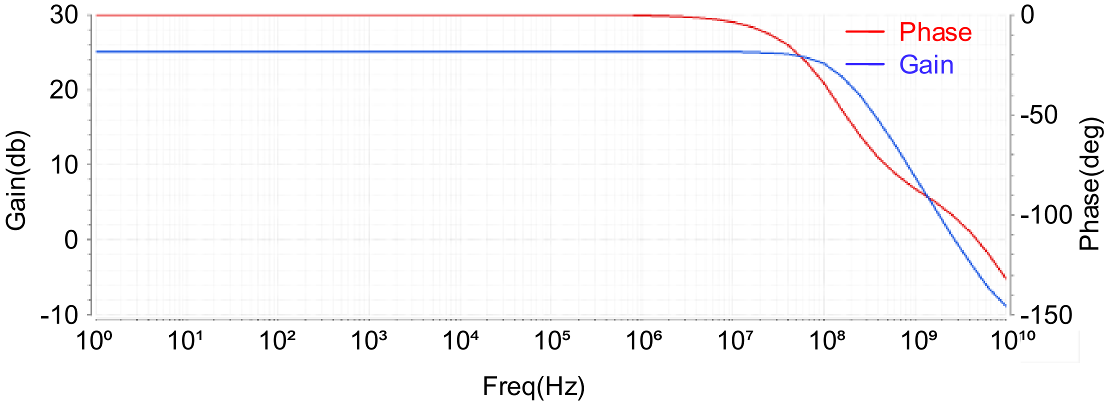


Fig.6.28 Frequency response of the proposed FGA.

Figure 6.29 shows the frequency response of the VGA combined with this FGA. The gain adjustment range of the proposed VGA with the FGA is from -20.82 dB to 17.97 dB with a -3 dB bandwidth of 36 kHz ~ 51 MHz.

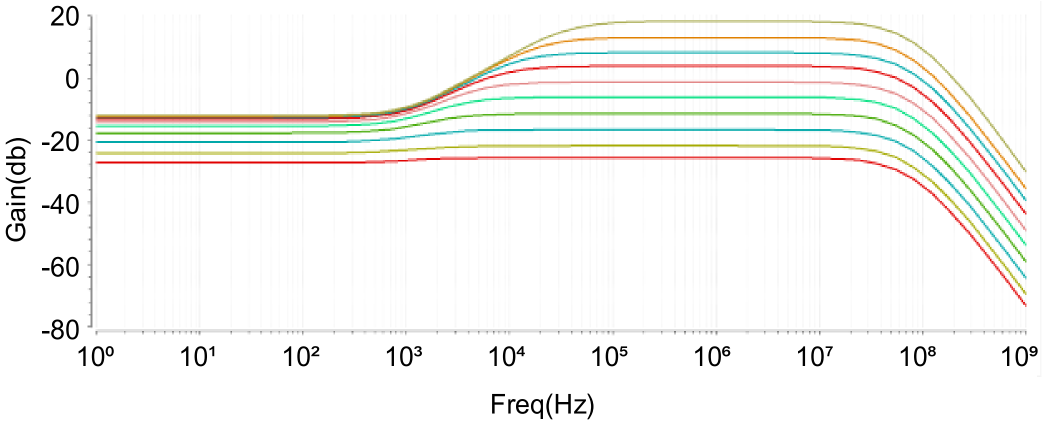


Fig.6.29 Frequency response of the proposed VGA combined with FGA.

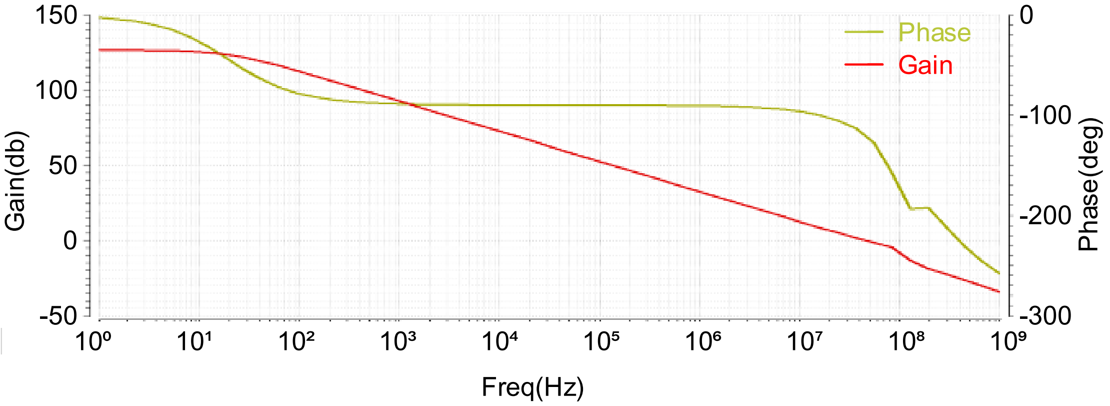


Fig.6.30 Frequency response of the proposed OPA.

The frequency response of the proposed OPA used in the output buffer is shown in Figure 6.30. This OPA can offer a gain of 126.5 dB with a 48-MHz bandwidth and 59° phase margin. The simulated slew rate of the designed OPA is presented in Figure 6.31. The slew rate of the proposed OPA is 169.6 V/μs.

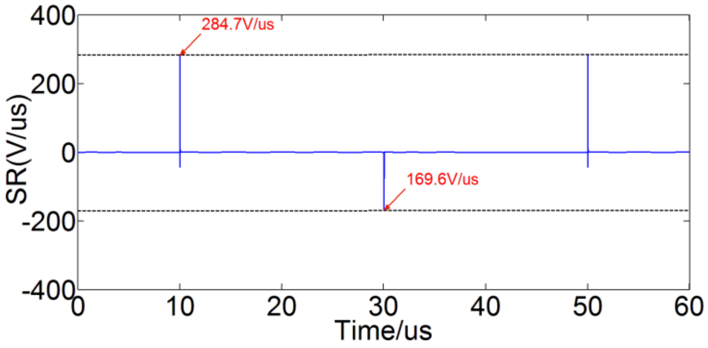


Fig.6.31 Simulated slew rate of the designed OPA.

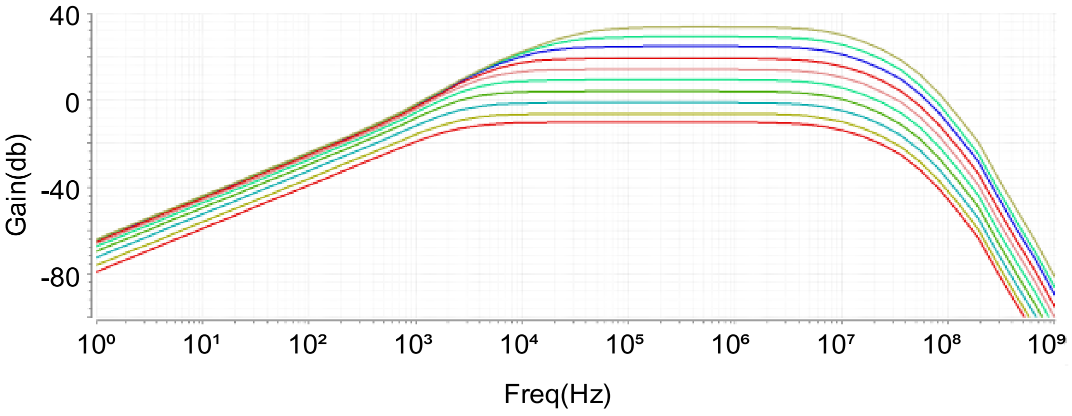


Fig.6.32 Frequency response of the proposed VGA combined with FGA and output buffer.

Figure 6.32 is the frequency response of the proposed VGA combined with the FGA and output buffer. There is an AC coupling circuit between the FGA and the output buffer, and the DC offset introduced by the mismatch in the FGA and the input signal is cancelled. However, the bandwidth is limited by this AC coupling circuit. The total gain output gain of the AGC now ranges from -8.82 dB ~ 29.97 dB. In addition, the -3 dB bandwidth of the AGC is from 36 kHz to 8.75 MHz.

The relationship between the gain-control signal V_{ctr} and the output signals V_{ex1} and V_{ex2} is demonstrated in Figure 6.33. As observed from this figure, V_{ctr} has a linear relationship with $ln(V_{ex1}-V_{ex2})$ in the range from 0.3 V to 3.7 V.

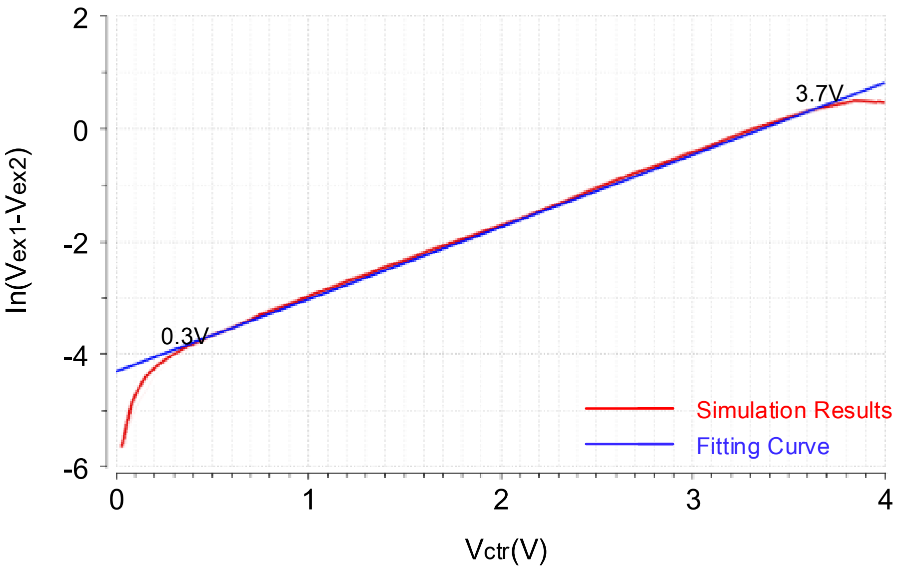


Fig.6.33 Relationship between the gain control voltage V_{ctr} and $ln(V_{ex1}-V_{ex2})$.

The gain-tuning curve of the proposed AGC is illustrated in Figure 6.34. The gain of the AGC can be tuned linearly by the exponential voltage-to-current converter from -8.82 dB to 29.97 dB.

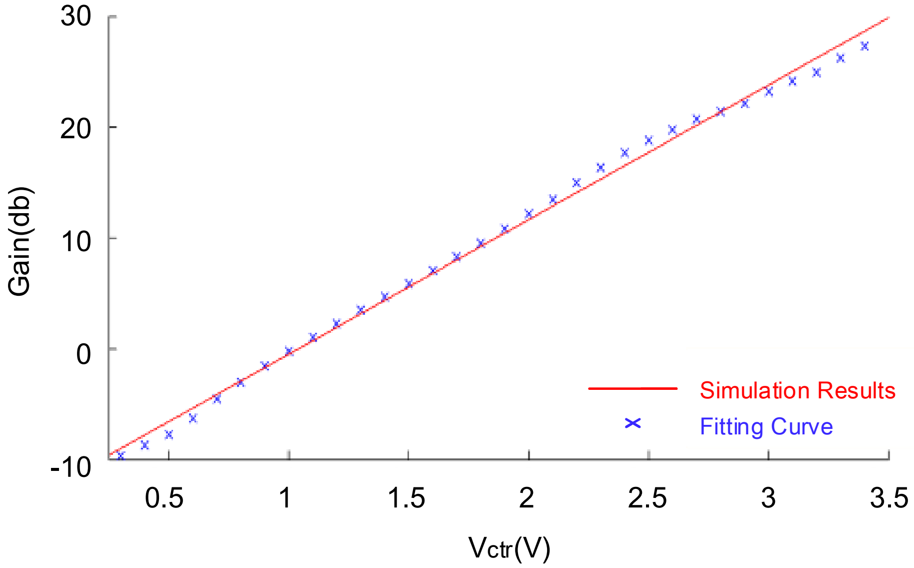


Fig.6.34 Gain tuning curve of the proposed AGC.

The linear error of the gain-tuning curve is shown in Figure 6.35. It can be seen that the linear error of the gain-tuning curve is less than 1.5 dB.

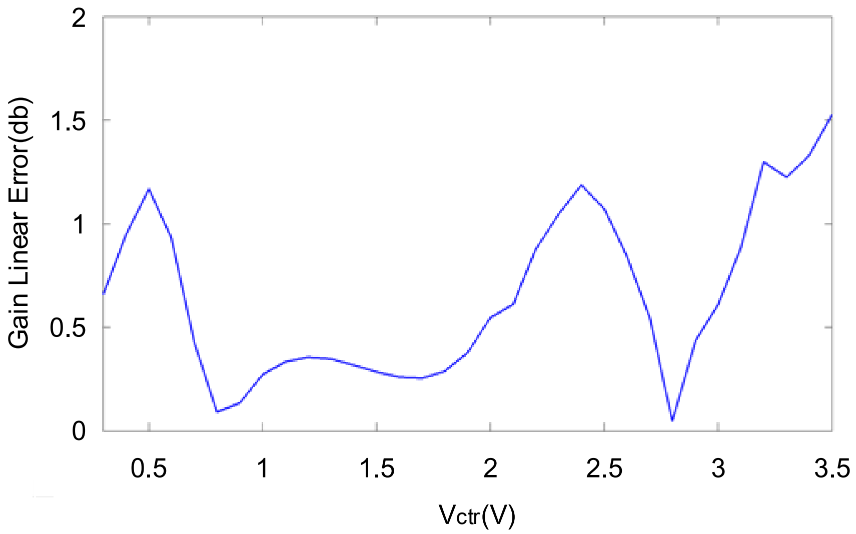


Fig.6.35 Linear error of the gain-tuning curve compared with the fitting curve.

The frequency response of the OTA used in the peak detector is shown in Figure 6.36. The designed OTA has a gain of 68 dB with 95 MHz bandwidth and a 69.5° phase margin.

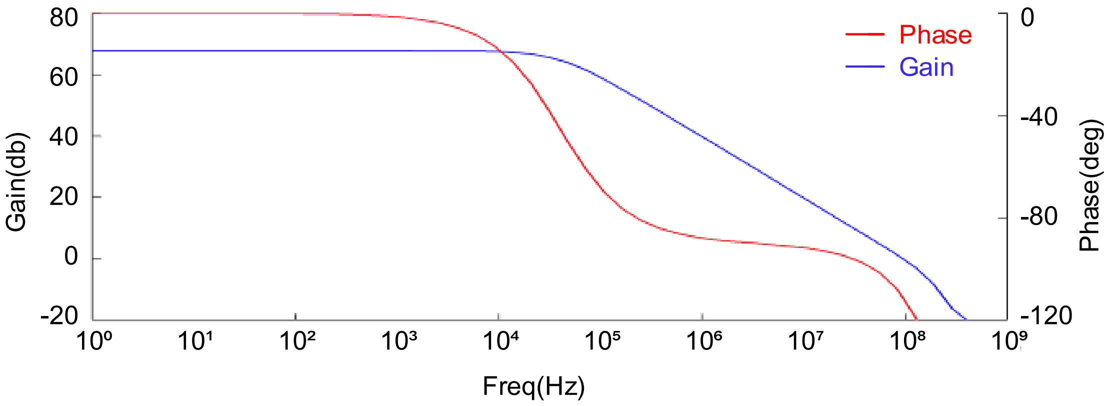


Fig.6.36 Frequency response of the proposed OTA.

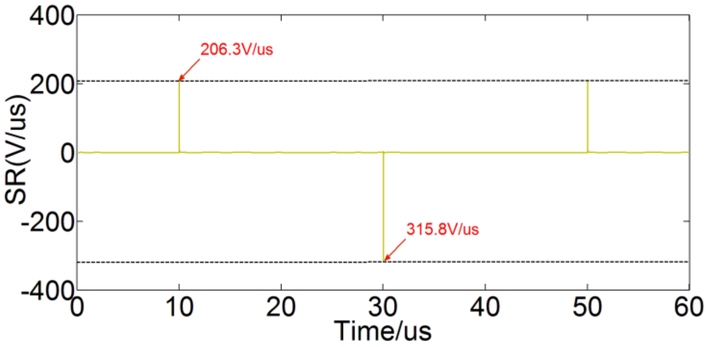


Fig.6.37 Simulated slew rate of the designed OTA.

The slew rate of this OTA is 206.3 V/µs. The simulation result of the slew rate is demonstrated in Figure 6.37.

Figure 6.38 shows simulation results of the peak detector with several sinusoidal input signals that have different frequencies and amplitudes. In our applicaton, the working frequency of the auto-tuning system is 1.25MHz, but the designed integrated AGC has a wide working frequency range, which is from 125kHz~3MHz. We can assume that if the proposed AGC works well in its working frequency range (125k~3MHz), it can also work well at 1.25MHz. Figure 6.38(a) shows the simulation result of the peak detector with a 125 kHz, 50 mV sinusoidal input signal, while Figure 6.38(b) shows the simulation result with a 125 kHz, 2 V sinusoidal input signal. The simulation result with a 3 MHz, 50 mV sinusoidal input signal is presented in Figure 6.38(c), and the result with a 3 MHz, 2 V sinusoidal input signal is shown in Figure 6.38(d).

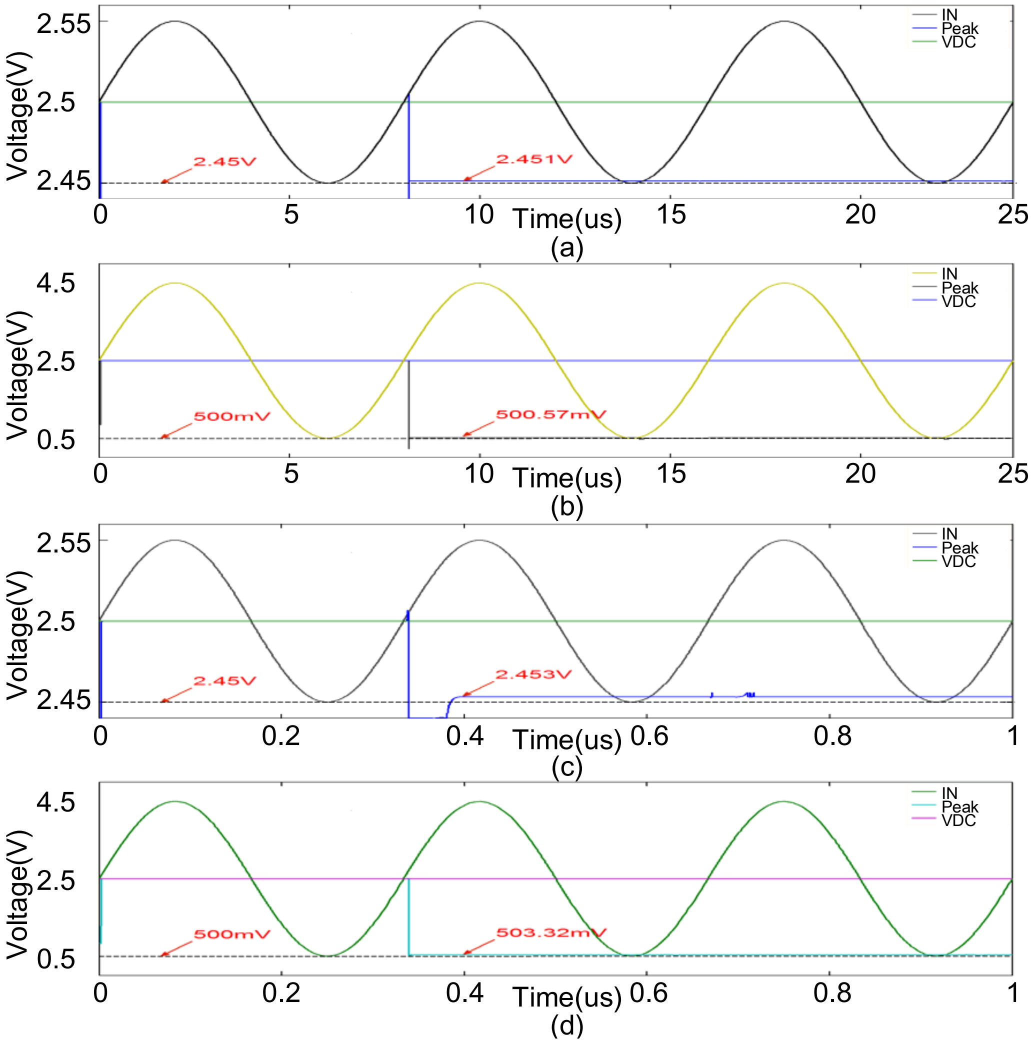


Fig.6.38 Simulation results of the proposed peak detector with different input signals: (a) f=125 kHz, V_{p-p}=0.1 V. (b) f=125 kHz, V_{p-p}=4 V. (c) f=3 MHz, V_{p-p}=0.1 V. (b) f=3 MHz, V_{p-p}=4 V.

As can be seen from this figure, the designed peak detector has a very good accuracy and speed. The error of the peak detector is less than 6% in the worst case, and the settling time of the proposed peak detector is less than one period.

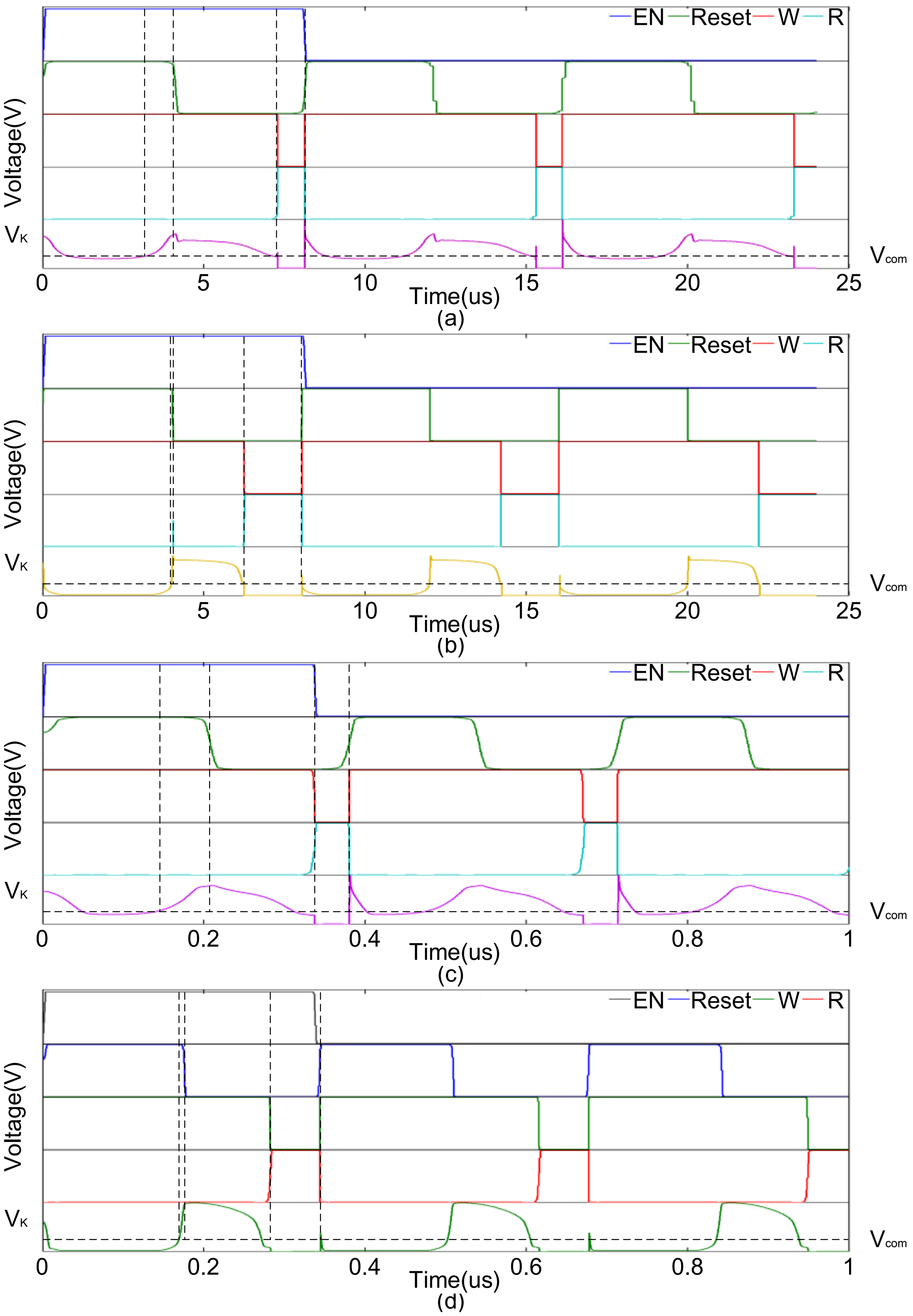


Fig.6.39 Simulation results of the switch control signal generator with different input signals: (a) f=125 kHz, V_{p-p}=0.1 V. (b) f=125 kHz, V_{p-p}=4 V. (c) f=3 MHz, V_{p-p}=0.1 V. (b) f=3 MHz, V_{p-p}=4 V.

The switch-control signals in the peak detector are generated automatically. The switch-control signals for the different input signals are shown in Figure 6.39. Figures 6.39(a)-(d) shows the simulation result of the generated switch control signals with the sinusoidal input signals 125 kHz/50 mV, 125 kHz/2V, 3 MHz/50 mV, and 3MHz/2V, respectively. The switch control signals are generated using the voltage at the point V_K.

The frequency response of the error amplifier designed for the AGC circuit is illustrated in Figure 6.40. For the 3 MHz input signal, the capacitances of *C1* and *C2* used in the error amplifier are chosen as 100 pF. The cutoff frequency of the error amplifier is 159.24 kHz. For the 125 kHz input signal, the capacitances are set to be equal to 1.6 nF. The cutoff frequency is now changed to 9.95 kHz.

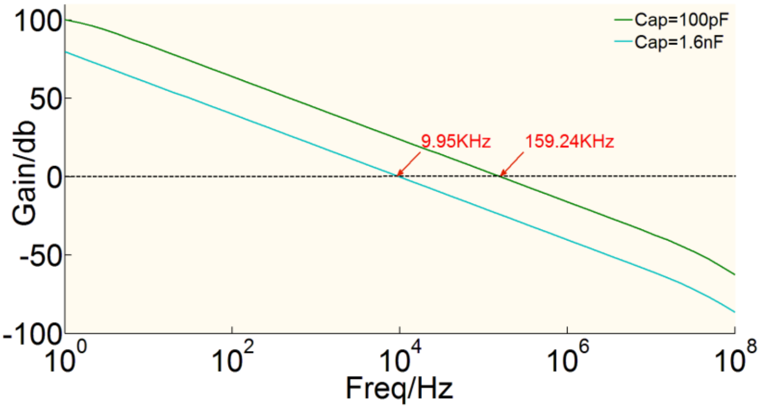
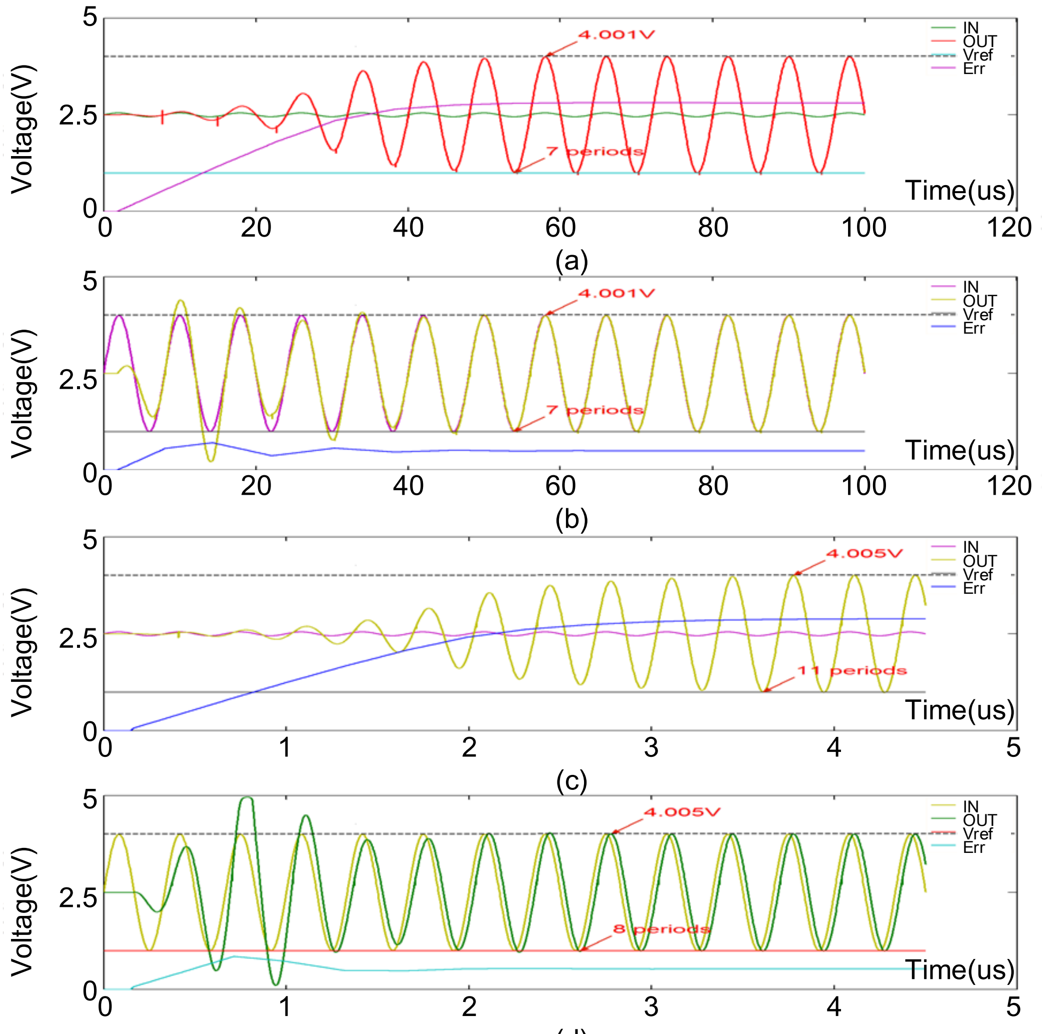


Fig.6.40 Frequency responses of the error amplifier designed for the AGC.

The simulation results of the proposed AGC with different sinusoidal input signals are shown in Figure 6.41. For the four sinusoidal input signals above, the simulation results are shown in Figure 6.41(a)~(d), respectively.



(a)

(b)

(c)

(d)

Fig.6.41 Simulation results of the proposed AGC with different input signals: (a) f=125 kHz, $V_{p\text{-}p}$=0.1 V. (b) f=125 kHz, $V_{p\text{-}p}$=4 V. (c) f=3 MHz, $V_{p\text{-}p}$=0.1 V. (b) f=3 MHz, $V_{p\text{-}p}$=4 V.

As can be seen from this figure, the proposed AGC can amplify the input signal to a target voltage V_{ref} = 1 V. The settling time of this AGC is less than 11 periods with a gain error of less than 0.25%.

6.6.2 Phase-error Detect Circuit

The frequency-response curve of the proposed phase-error detector circuit is illustrated in Figure 6.42. As analyzed in the former sections, the settling time of the phase-error amplifier needs to be greater than the settling time of the AGC. The maximum settling time of the proposed AGC circuit is 11 periods. Therefore, for a 1.25

MHz input signal, the cutoff frequency of the phase-error amplifier is set to 20 kHz.

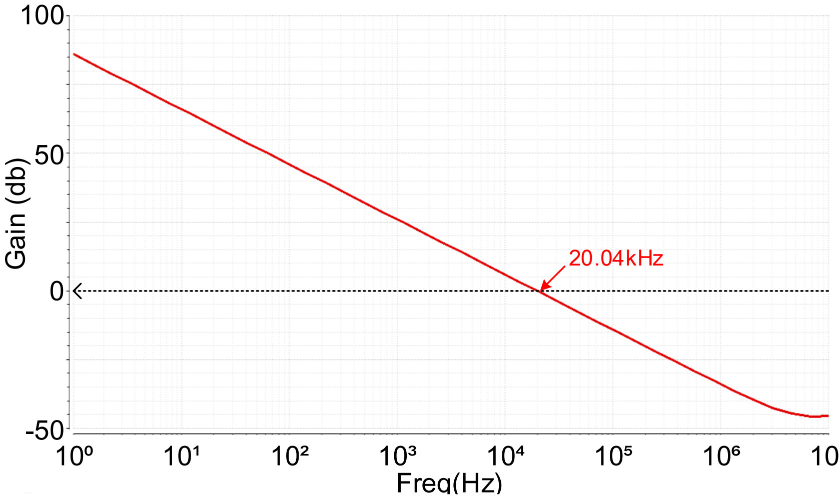


Fig.6.42 Frequency responses of the proposed phase error detector circuit

The simulation results of the phase-error detector are presented in Figure 6.43. The phase difference (π/2) between the input signals is converted into a corresponding voltage (2.5 V).

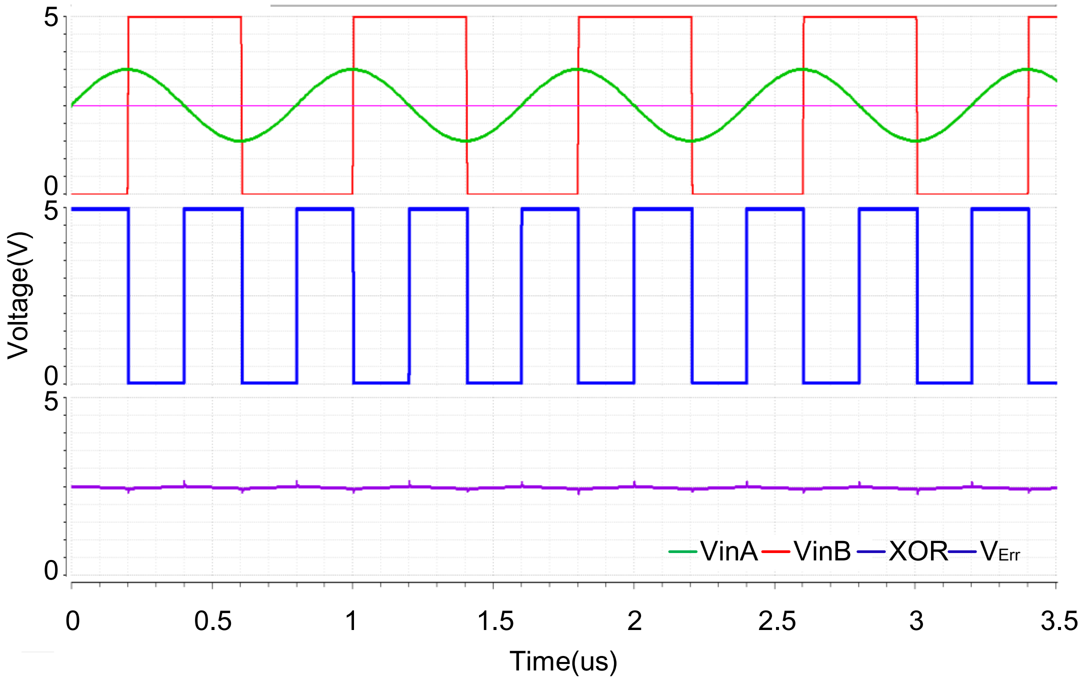


Fig.6.43 Simulation results of the proposed phase error detect circuit

6.6.3 Switch Signal Generator

Figure 6.44 (*top*) shows the simulation results of the comparator used in the Switch signal generator. The input signal is the green line illustrated in this figure. It is a 10 MHz sinusoidal signal with an amplitude of 1 V. The peak voltage of this signal is 3.5 V. The red line in this figure is the reference voltage, which is equal to 3.4995 V. The blue line is the output signal of the comparator. A zoomed view of the simulation results of the comparator is demonstrated in Figure 6.44 (*bottom*). The delay of the amplitude is less than 3 ns with a resolution of 0.5 mV.

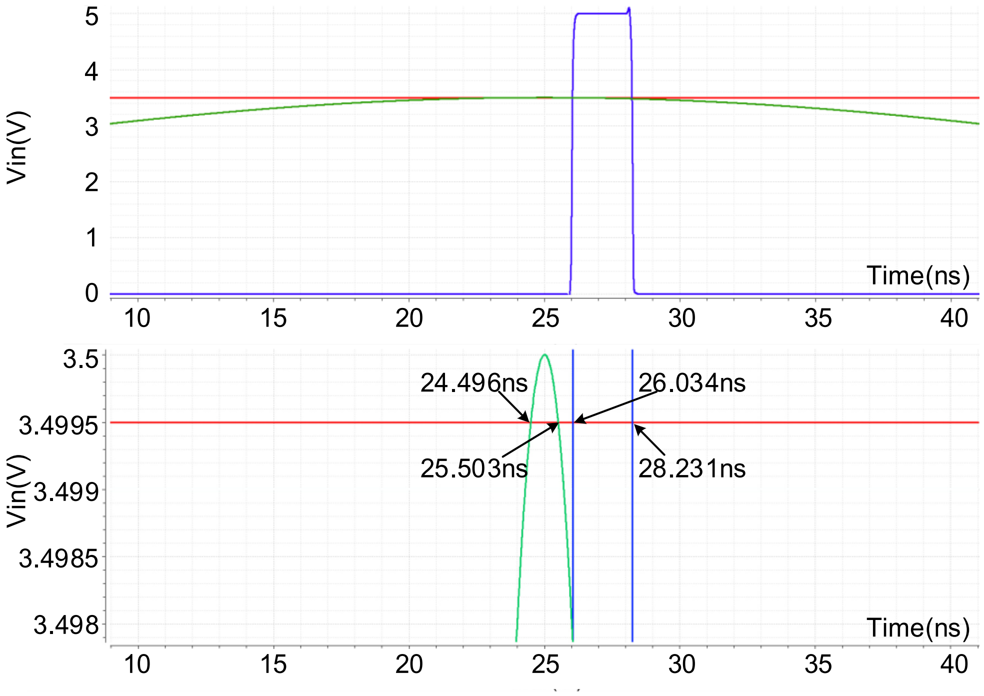


Fig.6.44 Simulation results for the comparator used in the Switch signal generator.

The simulation results of the proposed Switch signal generator are shown in Figure 6.45. In this figure, the orange line represents the input sinusoidal signal of the Switch signal generator, the red line and the purple line represent the phase error voltage, and the output control signal of the switched capacitor is represented by the green line. The output signal of this circuit has a conduction angle that is always symmetrical with respect to the zero-crossing points of the sinusoidal input voltage.

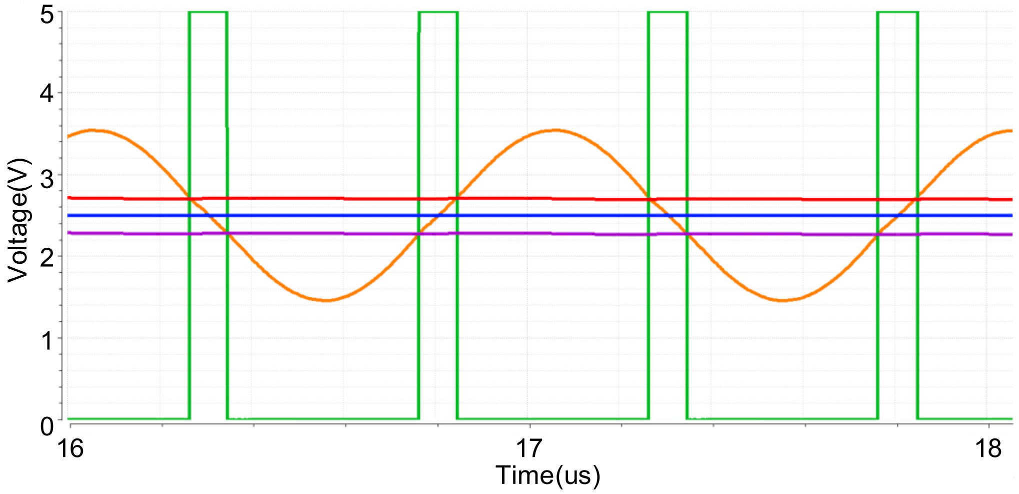


Fig.6.45 Frequency responses of the proposed phase error detector circuit

6.6.4 Bandgap Reference Circuit

The simulation results of the proposed bandgap reference circuit are illustrated in Figure 6.46. The supply voltage is set to 5 V with a temperature variation ranging from -20°C to 100°C. The designed temperature coefficients of the output reference voltage and current are 15.19 ppm/°C and 15.18 ppm/°C, respectively, and the output reference voltage is 1.222 V at a temperature of 27°C, while the output current is 50.08 μA at the same temperature.

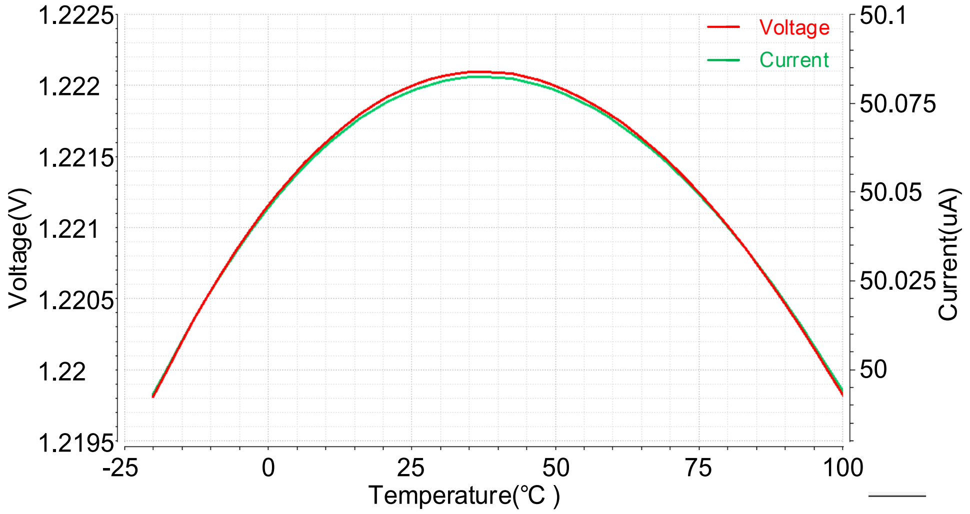


Fig.6.46 Simulation results of the bandgap reference circuit with a 5V power supply.

Figure 6.47 shows the simulation results of the bandgap reference circuit with different supply voltages, which range from 3–5 V. As can be seen from this figure, the designed bandgap reference circuit can adequately deal with a wide range of supply voltages.

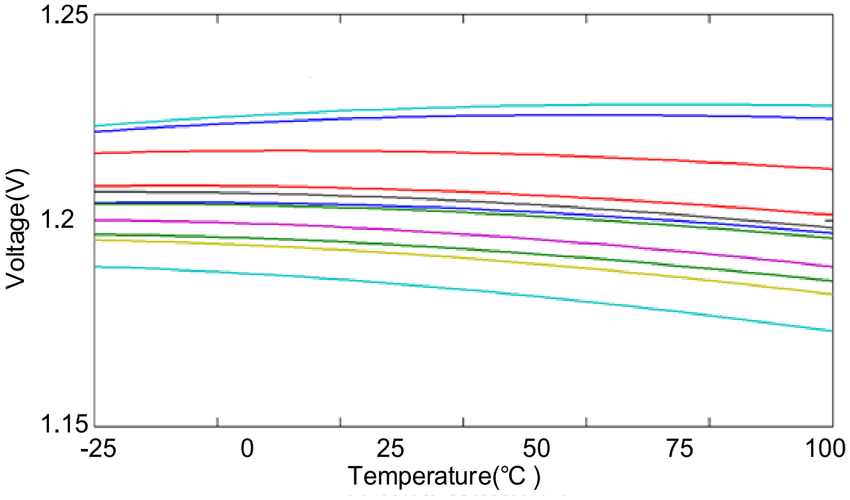


Fig.6.47 Simulation results of the bandgap reference circuit with different power supplies.

6.7 Post-layout Simulation

6.7.1 Automatic Gain Control Circuit

Figure 6.48 shows the post-layout simulation results of the DC characteristics of the proposed Gilbert cell combined with the attenuation block. From the figure, we see that the linear input range of the VGA is the same as in the pre-layout simulation (-1.5 V ~ 1.5 V).

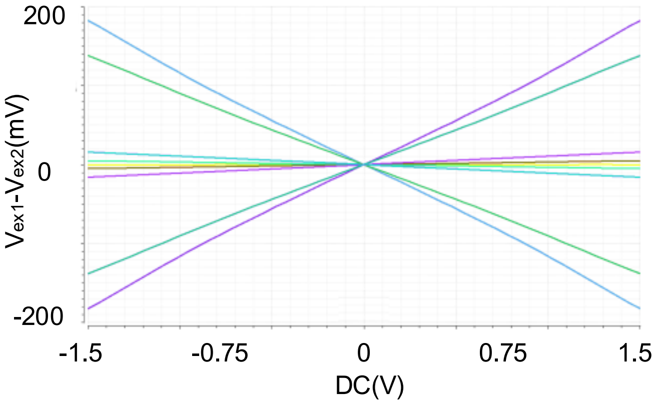


Fig.6.48 Post-layout simulated DC transfer characteristics of the proposed VGA.

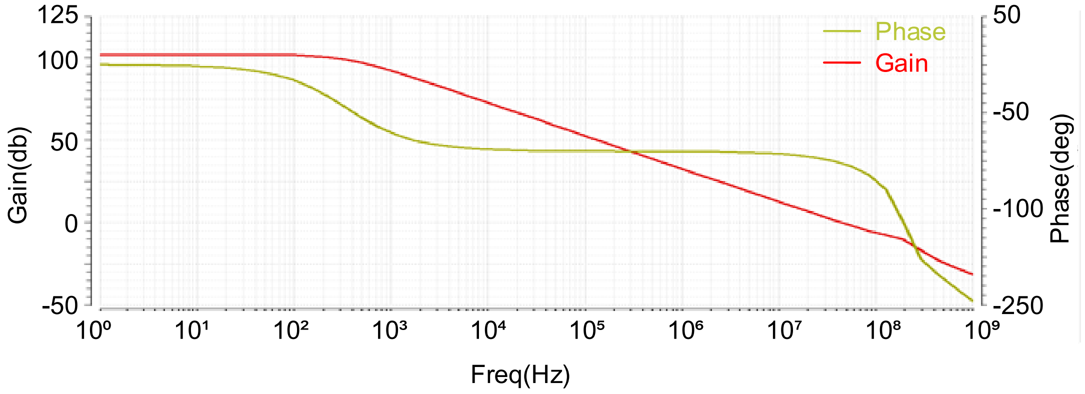


Fig.6.49 Post-layout frequency response of the OPA

The frequency response of the proposed OPA with the post-layout simulation is revealed in Figure 6.49. This gain of the OPA is changed to 102 dB with a 46 MHz bandwidth and 77.5° phase margin. The post-layout slew rate of this OPA is presented in Figure 6.50. The slew rate of the proposed OPA is 162.6 V/μs.

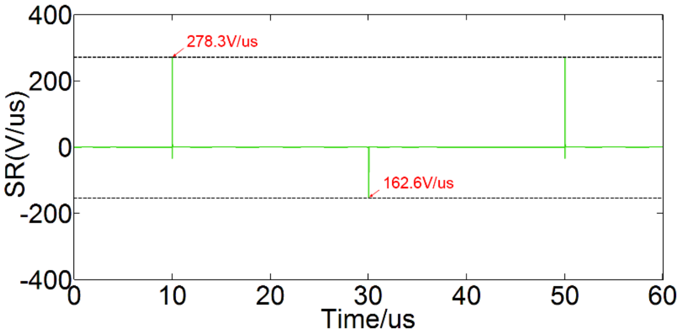


Fig.6.50 Post-layout simulated slew rate of the OPA.

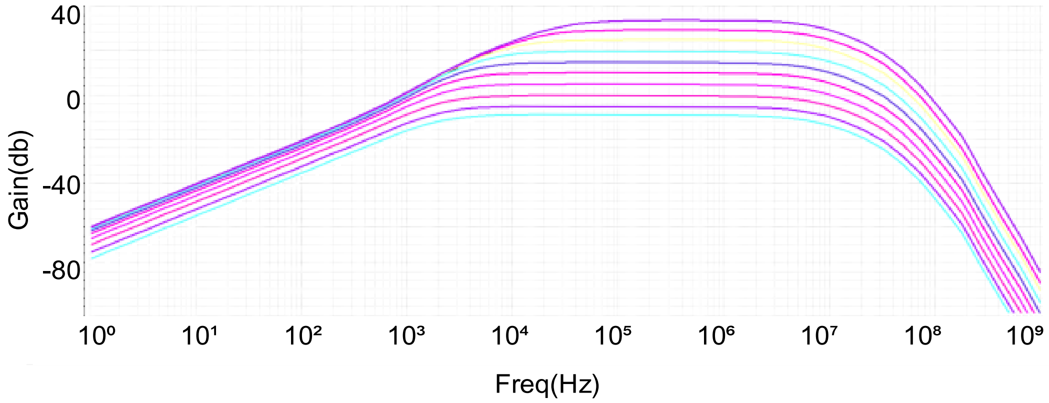


Fig.6.51 Post-layout simulated frequency response of the proposed VGA combined with the FGA and output buffer.

Figure 6.51 shows the post-layout frequency response of the proposed VGA combined with the FGA and output buffer. The total output gain of the AGC ranges from -9.04 dB to 29.47 dB, and the -3 dB bandwidth of the AGC ranges from 37.5 kHz to 8.36 MHz.

The post-layout simulation results of the gain-tuning curve are demonstrated in Figure 6.52. The same as the pre-layout simulation result presented in section 6.6.1, The proposed AGC has a approximately linearly gain tuning range of 39 dB with a gain control voltage ranging from 0.35 V to 3.5 V

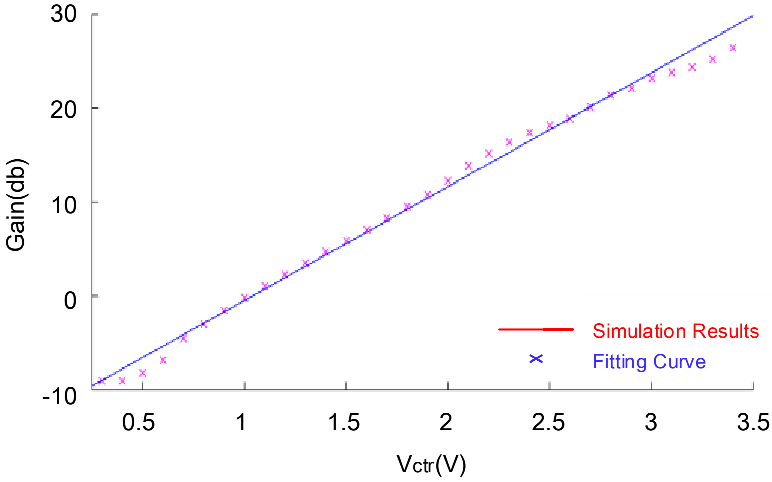


Fig.6.52 Post-layout simulated gain tuning curve of the proposed AGC.

The post-layout frequency response of the OTA used in the peak detector is presented in Figure 6.53. The designed OTA has a gain of 55.4 dB with a 91-MHz bandwidth and 70° phase margin.

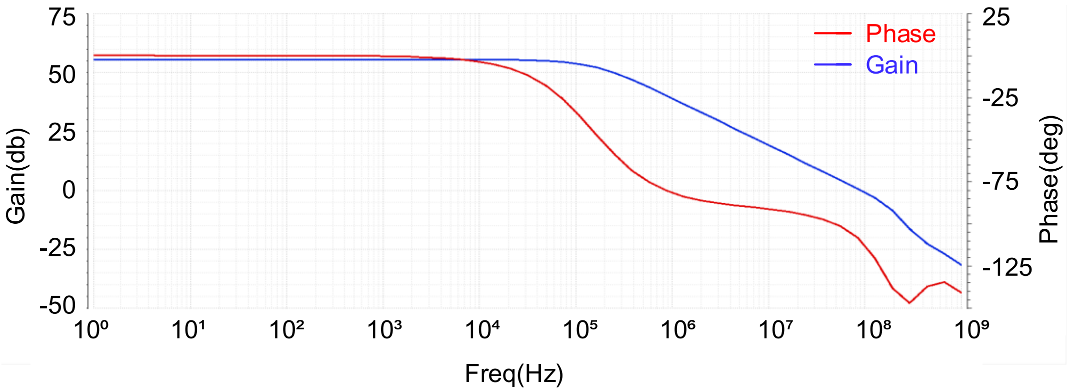


Fig.6.53 Post-layout frequency response of the proposed OTA.

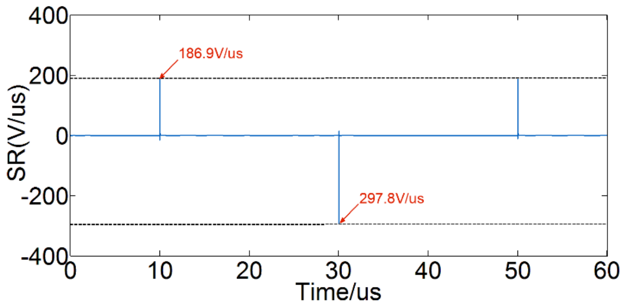


Fig.6.54 Simulated slew rate of the designed OTA.

The slew rate of the post-layout OTA is changed to 186.9 V/μs. The simulation result of the slew rate is demonstrated in Figure 6.54.

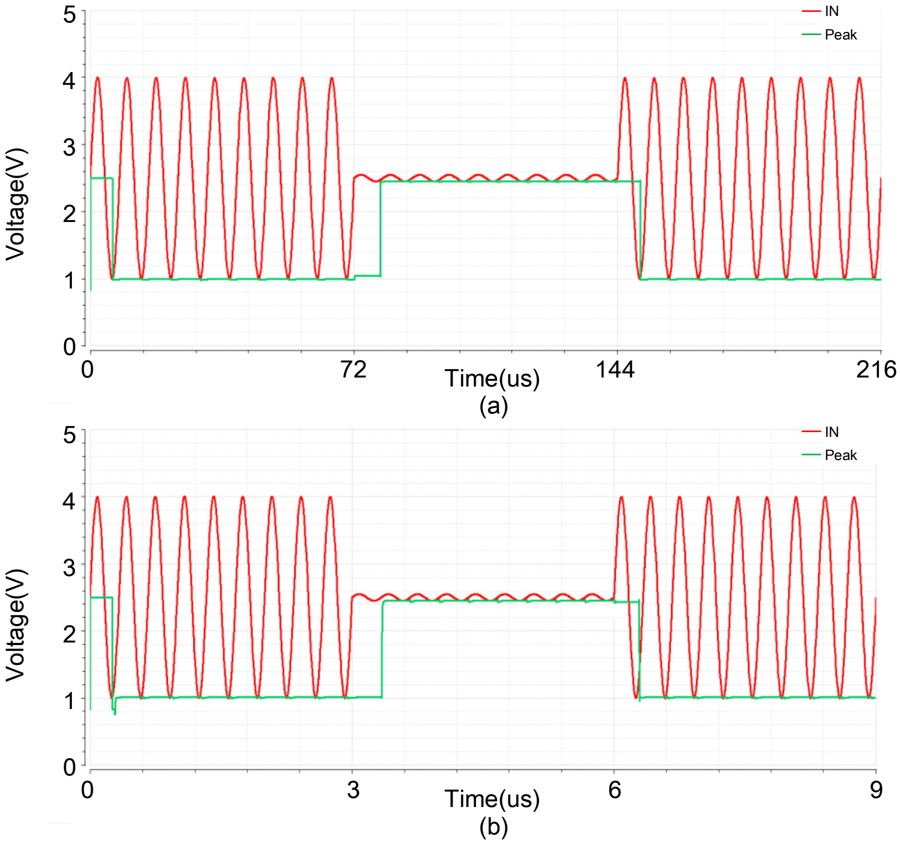


Fig.6.55 Post-layout simulation results of the proposed peak detector with different input signals (Max($V_{p\text{-}p}$)=3 V, Min($V_{p\text{-}p}$)=0.1 V): (a) f=125 kHz. (b) f=3 MHz.

Post-layout simulation results of the peak detector with two modulated sinusoidal input signals that have different frequencies are illustrated in Figure 6.55. Figure 6.55(a) shows the simulation result of the peak detector with a 125 kHz modulated sinusoidal input signal. The maximum amplitude of this input signal is 1.5 V, and the minimum amplitude is 50 mV. Figure 6.55(b) is the simulation result obtained using a 3 MHz modulated sinusoidal input signal. The amplitude range of the input signal is the same as the previous one.

As can be seen from this figure, the settling time of the proposed peak detector is less than one period for different input frequencies. The output error of this peak detector is shown in Figure 6.56. The maximum output error of the proposed peak detector is less than 16 mV.

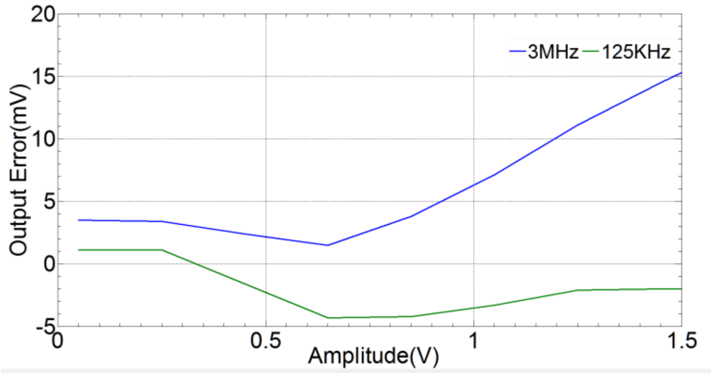


Fig.6.56 Post-layout simulated output error of the peak detector.

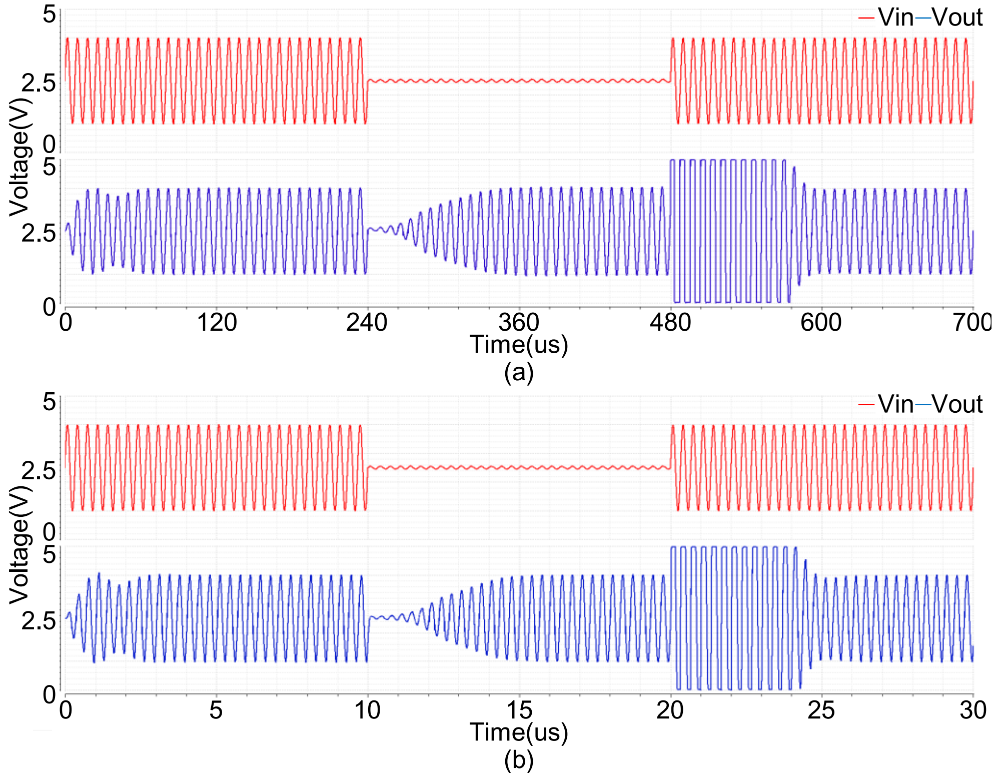


Fig.6.57 Post-layout simulation results of the proposed AGC with different input signals ($\text{Max}(V_{p\text{-}p})$=3 V, $\text{Min}(V_{p\text{-}p})$=0.1 V): (a) f=125 kHz. (b) f=3 MHz.

The post-layout simulation results of the proposed AGC with the same input signals as the peak detector are shown in Figure 6.57. The simulation results with the 125 kHz modulated sinusoidal input signal are shown in Figure 6.57(a), while Figure 6.57(b) presents the simulation results with a 3 MHz modulated sinusoidal input signal.

The proposed AGC can amplify the input signals with different amplitude to the target voltage V_{ref} = 1.5 V. The settling time of this AGC is less than 15 periods in the worst case.

We performed an output DC-offset analysis of the proposed AGC by using the Monte Carlo approach. The DC-offset voltage Monte Carlo histogram of the AGC is demonstrated in Figure 6.58.

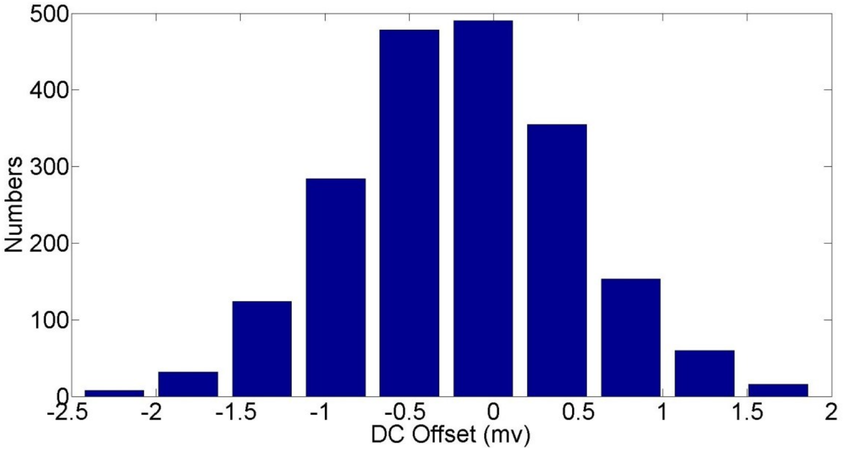


Fig.6.58 The DC offset voltage Monte Carlo histogram of the proposedAGC.

The offset of the AGC circuit is significantly reduced by the output DC-offset cancellation circuit, and the maximum output DC offset is only 3 mV.

6.7.2 Phase-error Detector

The post-layout simulation results of the phase-error detector are presented in Figure 6.59. The Simulation results is nearly the same as the pre-layout simulation results. The phase difference between the input signals V_{inA} and V_{inB} is detected and transferred into a relevant voltage. As shown in this figure, when the phase difference is π/2, the output phase error voltage V_{Err} is 2.5 V.

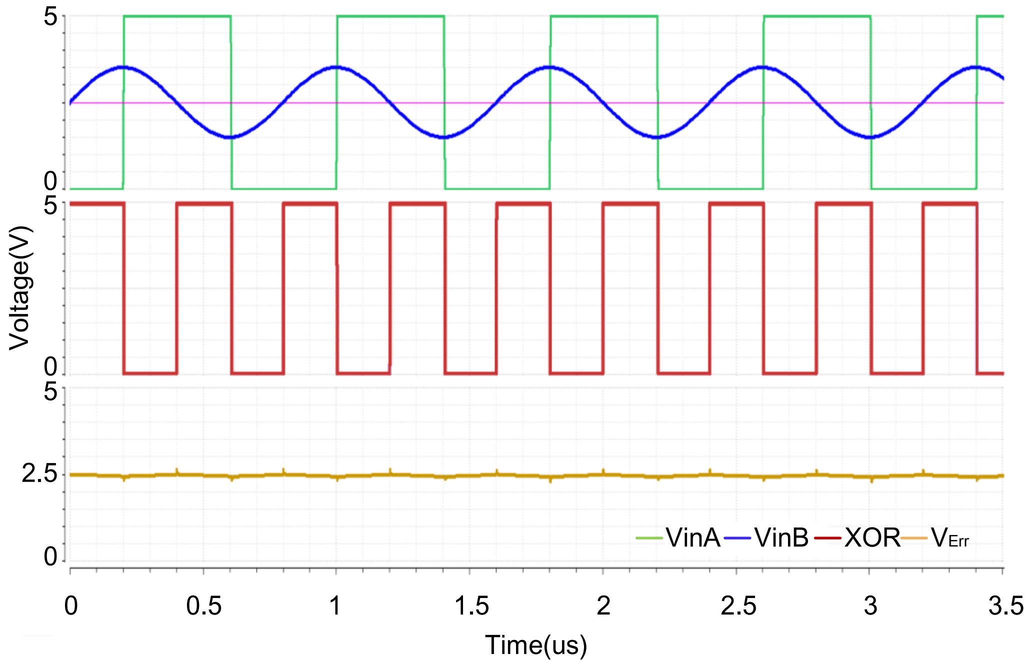


Fig.6.59 Post-layout simulation results of the proposed phase error detect circuit.

6.7.3 Switch Signal Generator

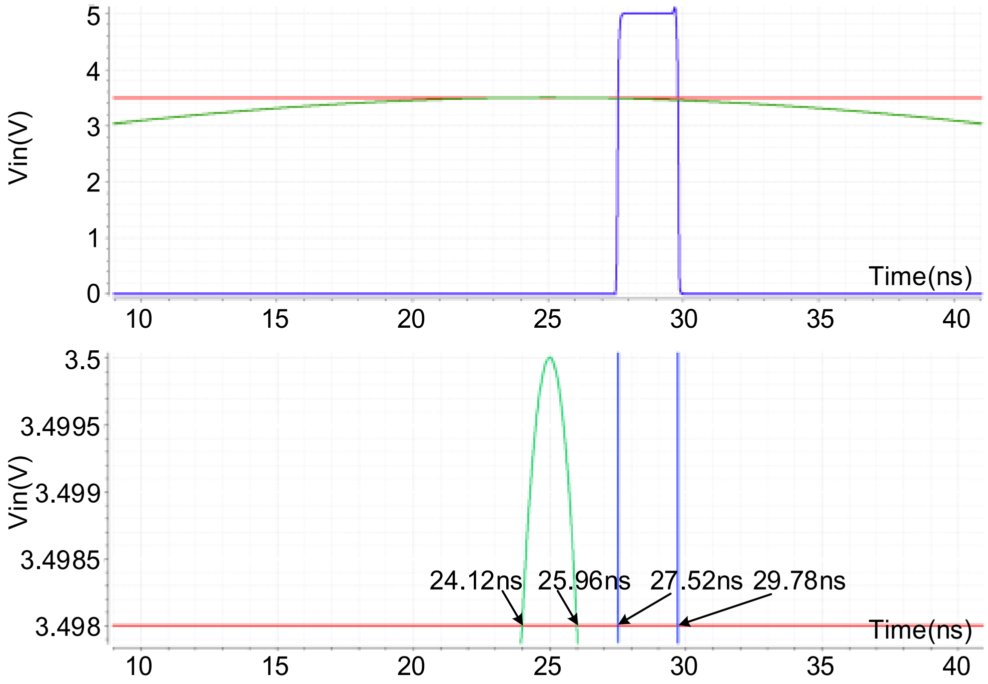


Fig.6.60 Post-layout simulation results of the comparator used in the Switch signal generator.

The post-layout simulation results of the comparator used in the Switch signal generator are shown in Figure 6.60 (upper). The input signal is shown by the green line in this figure, and it is a 10 MHz sinusoidal signal with a 1 V amplitude and 2.5 V DC voltage. The peak voltage of this signal is 3.5 V. The resolution of the comparator after post-layout is reduced to 2 mV. The blue line represents the output signal of the comparator. A zoomed view of the simulation results is demonstrated in Figure 6.60 (lower). The delay of the amplitude is changed to 3.5 ns.

6.7.4 Bandgap Reference Circuit

The post-layout simulation results of the proposed bandgap reference circuit are illustrated in Figure 6.61.

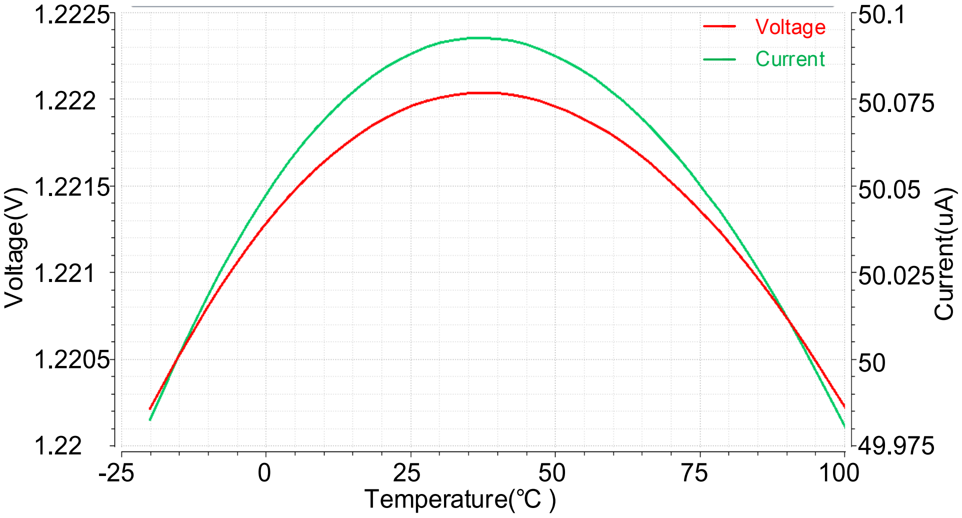


Fig.6.61 Post-layout simulation results of the bandgap reference circuit.

We set the supply voltage to 5 V with a temperature variation ranging from -20°C to 100°C. The designed temperature coefficients of the output reference voltage and current are 15.3 ppm/°C and 15.16 ppm/°C, respectively. The output reference voltage is 1.222 V at a temperature of 27°C, and the output current is 50.07 µA at the same temperature.

6.8 Conclusion of the Proposed Integrated Auto-tuning System

In this chapter, an integrated version of the proposed auto-tuning system is designed and presented. The surface area of the proposed integrated auto-tuning system is only 0.42 mm^2 without the out-chip components, which is much smaller than the PCB version (110 cm^2). Therefore, it is perfectly suitable for our HIFU application which needs 256 auto-tuning feed-back loops.

The proposed integrated AGC used for the auto-tuning system has a -3 dB bandwidth which is ranging from 37.5 kHz to 8.36 MHz. Because the proposed AGC has a dB-linear gain control function, the settling time of the AGC is nearly constant. According to the post-layout simulation results, the maximum settling time of the proposed AGC is less than 15 periods. Besides, it can provide 38.51 dB variable gain with a gain control voltage from 0.35 V to 3.5 V.

The same as the PCB version, the integrated phase-error detector designed in this chapter, allows the tuning of the system by controlling a phase difference ($\Delta\varphi = \pi/2$) between the half bridge output voltage (V_{HB}) and the voltage across the tuning capacitor (V_{CFix}). It also has capability of transform the phase difference between V_{HB} and V_{CFix} into a relevant voltage.

The latched comparator used in the the integrated switch signal generator achieves a resolution of 0.5mV, and the relevant phase error of the generated AC switch control signal is less than 0.4°. The output switch control signal of this integrated circuit is always symmetrical with respect to the zero-crossing points of the V_{CFix}, which is applied across the fixed capacitor C_{Fix}. In other words, the physical impossibility of over current spikes (having theoretically an infinite intensity) flowing through the AC switch is perfectly eliminated by using the proposed circuit.

Moreover, because all of the proposed integrated circuits have wide working frequency range, the proposed integrated auto-tuning system can be used HIFU applications with other working frequency. The close-loop test of the proposed auto-tuning system combined with the proposed power amplifier will be presented in chapter 7.

Chapter 7

Test and Simulation Results of the Ultrasonic Generator System

7.1 Introduction

In this chapter, we present the results of the complete ultrasonic generator system including the test of the PCB realisation and the simulation of the IC design and combining together the proposed power amplifier combined with the proposed auto-tuning system. The structure of this chapter is as follows: In Section 7.2, we present the test results of the ultrasonic generator with a PCB auto-tuning system. In Section 7.3, first, we show the simulation results of this generator with the integrated design of the auto-tuning circuit, and then, we then give the analysis of these results.

7.2 Test of Ultrasonic Generator with PCB Realisation

This sectin presents the test of the ultrasonic generator with PCB realisation. It consists of two parts: test conditon and test results.

7.2.1 Test Condition

To test the functionality of the auto-tuning system, we added a C_{Error}, which is controlled by PWM_E (5-kHz square wave).

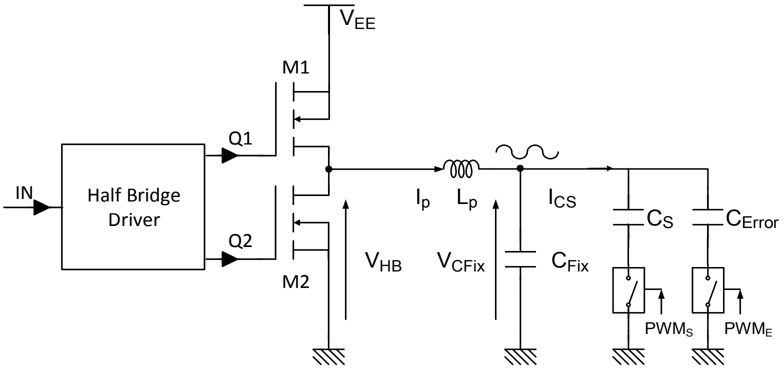


Fig.7.1 Equivalent test circuit of the ultrasonic generator with the proposed printed circuit board auto-tuning circuit.

The equivalent circuit of the test circuit is shown in Figure 7.1. The input signal of the half-bridge driver is a pulse signal with a 50% duty cycle and 5 V peak level, and the power supply of the half-bridge circuit is also 5 V. The frequency of the input signal is 1.25 MHz.

For an ultrasonic transducer, the variation of its imaginary impedance is usually a process of slow change, and this variation is hard to control. In this case, we use a switch controlled error capacitor C_{Error} in the test circuit instead of the real transducer. This error capacitor is controlled by a square wave signal (PWM_E). By this way, it provides a sudden changing of the imaginary impedance. In this thesis, we set the value of C_{Error} to 50 pF, and PWM_E used in this thesis is a 5 kHz square wave signal.

7.2.2 Test results

The test results of the proposed ultrasonic generator are shown in Figure 7.2. The orange line is the output signal of the power amplifier. The green line is PWM_E. The output signal is the pink line in this figure, and the phase-error voltage is shown as the blue line.

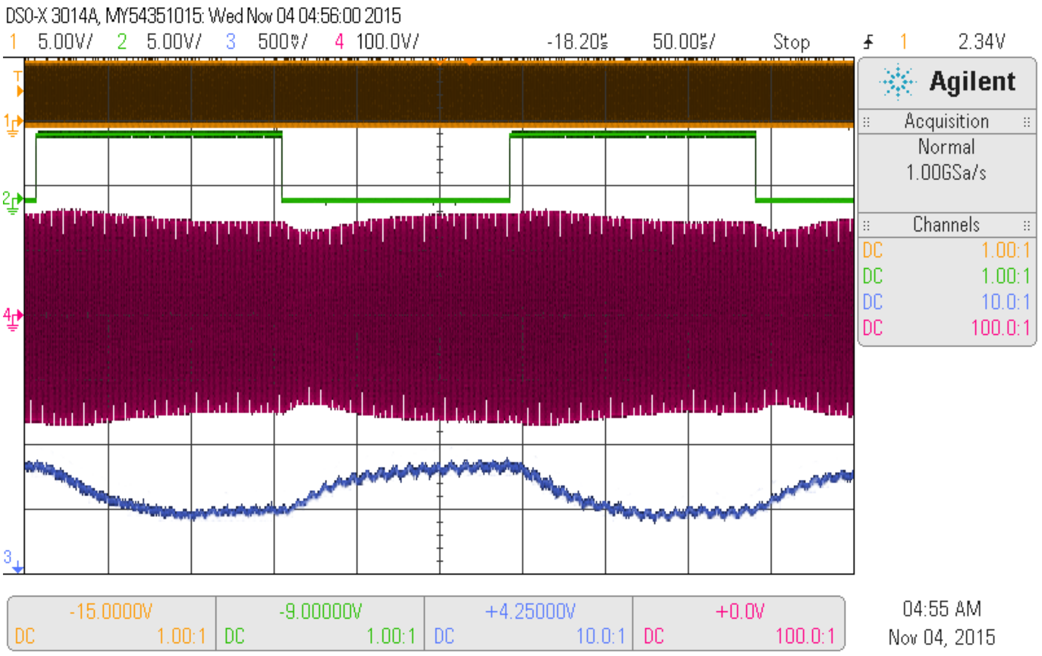


Fig.7.2 Test results of ultrasonic generator with the proposed printed circuit board auto-tuning circuit.

Ch1 (*orange*): Out signal of the half-bridge circuit V_{HB}: 5V/div.

Ch2 (*green*): Error capacitor control signal PWM_E: 5V/div.

Ch3 (*blue*): Phase-error voltage V_{OEA} generated by the deteciotn block: 500mV/div.

Ch4 (*pink*): Output signal of the power amplifier V_{CFix}: 100V/div.

Detailed views of the simulation results are presented in Figure 7.3. Figure 7.3 (*upper*) shows the detailed view of the test results when PWM_E is 0 V, and Figure 7.3 (*lower*) shows the test results when PWM_E is 5 V. The orange line represents the output signal of the power amplifier, and the green line represents the PWM_E signal. The output signal is the red line, and the switched-capacitor control signal PWM_S is shown as the blue line.

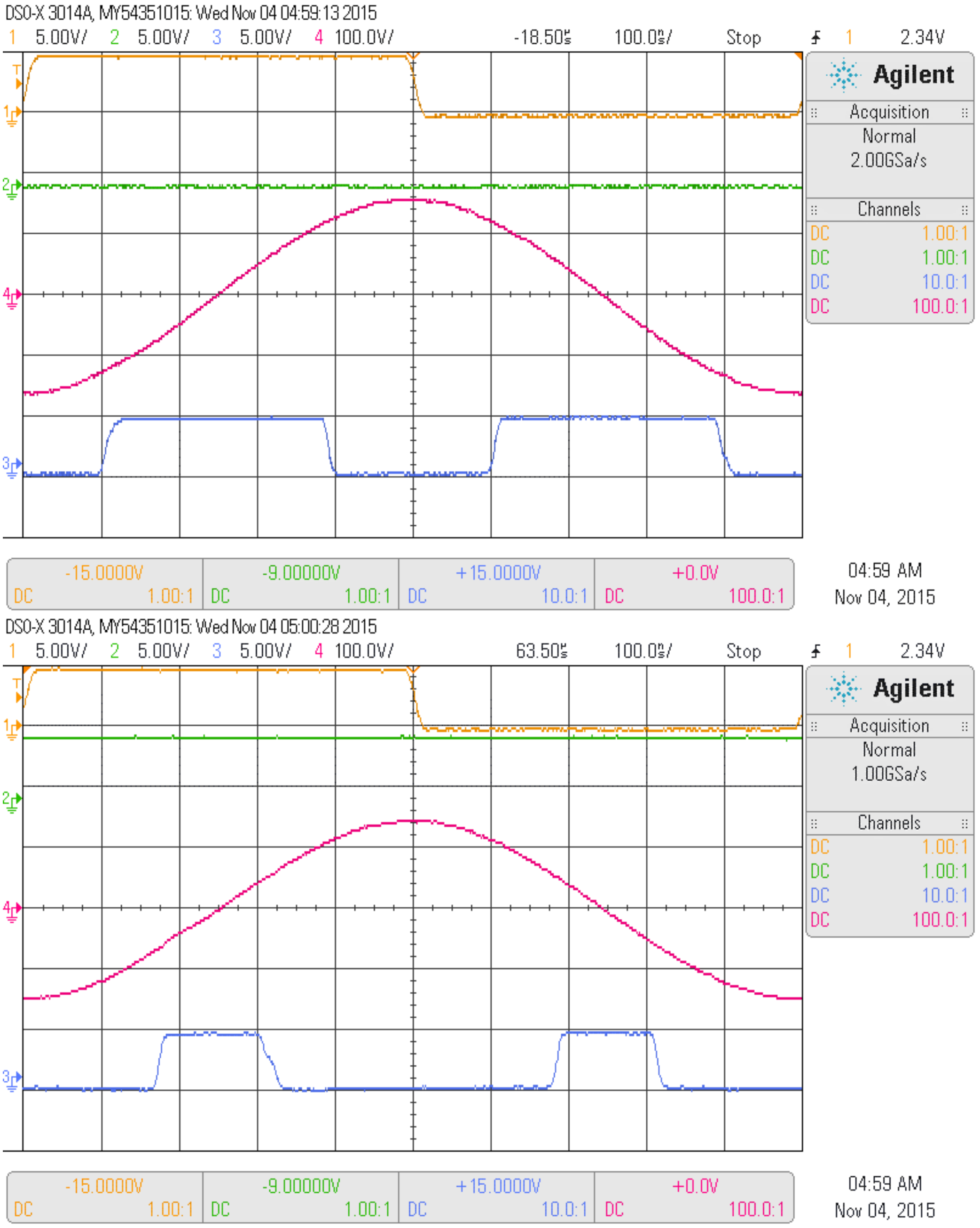


Fig.7.3 Zoomed views of the simulation results of ultrasonic generator with the proposed printed circuit board auto-tuning circuit.

Ch1 (*orange*): Out signal of the half-bridge circuit V_{HB}: 5V/div.

Ch2 (*green*): Error capacitor control signal PWM_E: 5V/div.

Ch3 (*blue*): Phase-error voltage V_{OEA} generated by the deteciotn block: 500mV/div.

Ch4 (*pink*): Output signal of the power amplifier V_{CFix}: 100V/div.

As can be seen from the figure, the phase error caused by C_{Error} is eliminated, and the phase difference between the output signal of the power amplifier and the output signal of the auto-tuning circuit is forced to π/2. In other words, the ultrasonic generator is well tuned.

7.3 Simulation Results of Ultrasonic Generator (IC)

In this section, we present the simulation results of the ultrasonic generator with an IC auto-tuning circuit. For the IC version, to simplify and accelerate the simulation of the whole system, we used an equivalent power amplifier and AC switch circuit instead of the real one. The equivalent circuit of the test circuit is shown in Figure 7.4. The input signal is a square signal (high level = 50 mV, low level = -50 mV). The frequency of the input signal V_{IN} is set to 1.25 MHz, and the frequency of PWM_E is equal to 16.7 kHz.

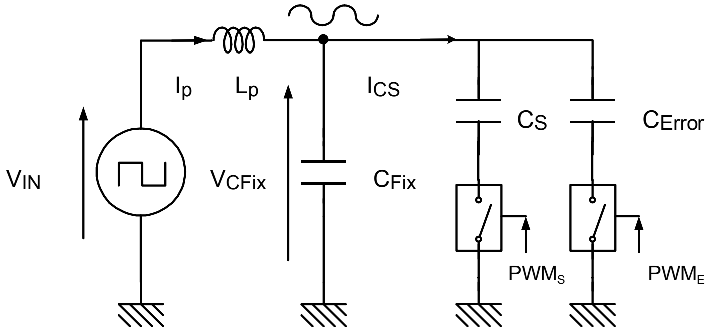


Fig.7.4 Equivalent simulation circuit of the ultrasonic generator with the proposed integrated auto-tuning circuit.

7.3.1 Pre-layout Simulation Results

The pre-layout simulation results of the proposed ultrasonic generator with the integrated auto tuning circuit are shown in Figure 7.5.

Figure 7.5 (*left*) shows the output of the voltage divider in the ideal case (The phase difference between V_{OUT} and V_{CFix} is π/2). Figure 7.5 (*right*) shows the simulation results in an actual situation. PWM_E is the red line, the orange line is the phase-error voltage, and the purple line is the output of the voltage divider in the actual case.

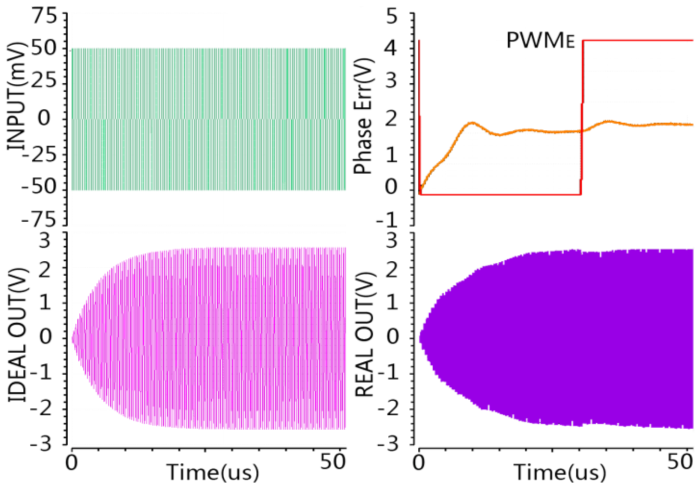


Fig.7.5 Input and output of the tuning circuit in the ideal case (*left*) and the simulation results in the real case (*right*).

As can be seen from this figure, the auto-tuning circuit can automatically tune the phase of the output signal, which will remove the phase error caused by C_{Error} and make the tank circuit nearly reach its theoretical efficiency.

Details of the simulation results are shown in Figure 7.6. The left waveform shows the result when PWM_E is disabled, and the right waveform shows the results when PWM_E is enabled. PWM_S is the pink line.

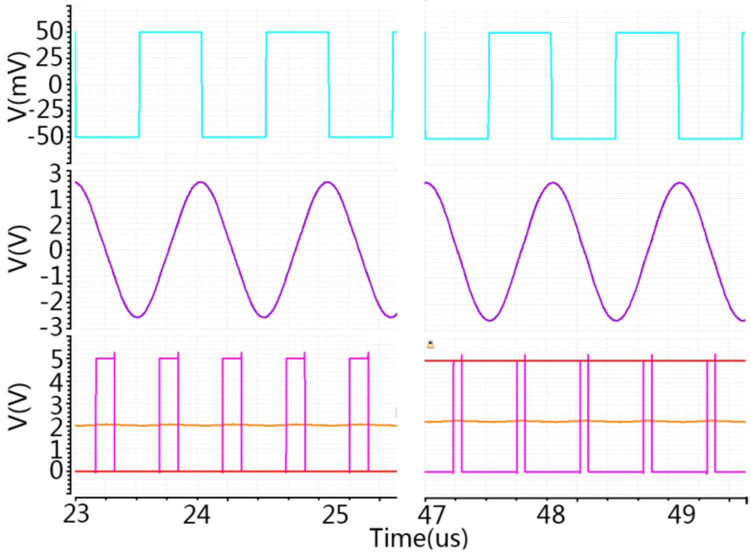


Fig.7.6 Details of the simulation results for the ultrasonic generator with the proposed integrated auto-tuning circuit.

7.3.2 Post-layout Simulation Results

The post-layout view of the auto-tuning system is demonstrated in Figure 7.7. The circuit in the purple dotted rectangle is the AGC part of the auto-tuning system, while the phase-error amplifier and PWM comparator are illustrated in the red dotted rectangle and blue dotted rectangle, respectively. The circuit illustrated by the green line is the biasing source. The surface area of the proposed AGC circuit is 0.13 mm^2. Other parts of the proposed auto-tuning system take up an area of 0.29 mm^2, and the total surface area of the proposed auto-tuning system is 0.42 mm^2.

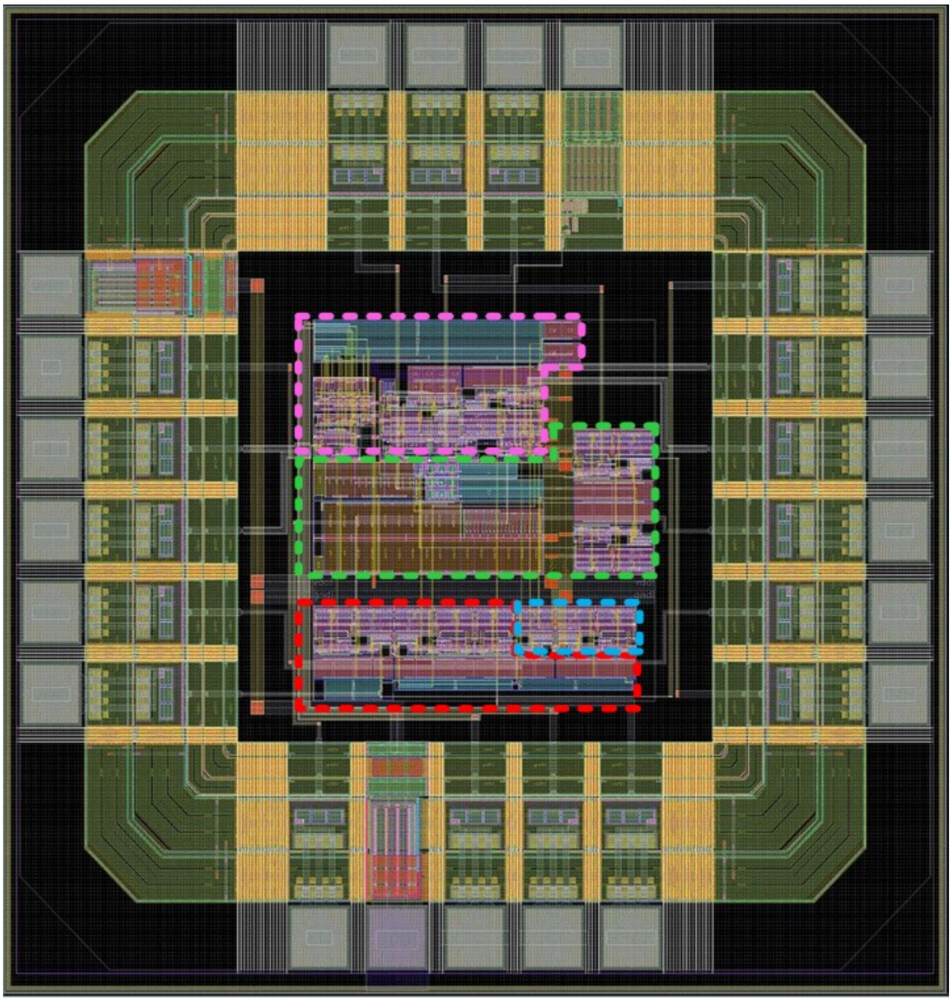


Fig.7.7 Post-layout view of the proposed auto-tuning system.

In Figure 7.8, we present transient post-layout simulation results PWM_E is the green line, the red line is the phase-error voltage, and the blue line is the output of the voltage divider in an actual situation.

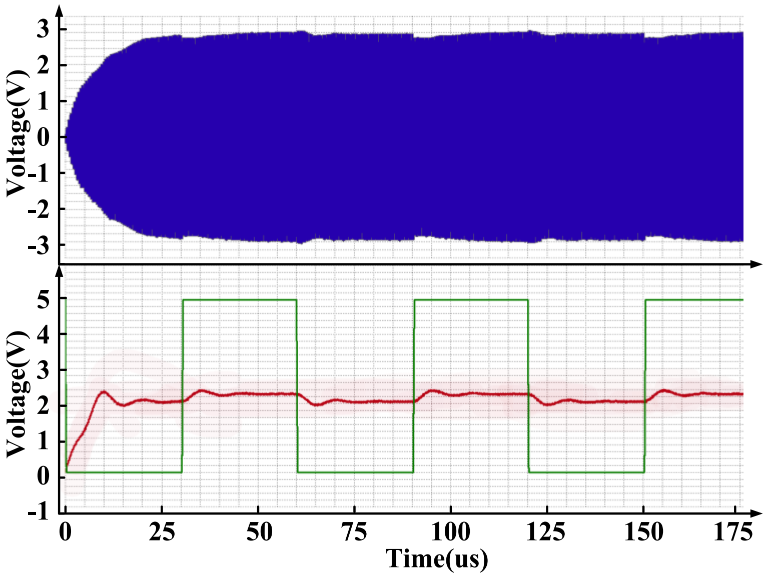


Fig.7.8 Post-layout simulation results of the auto-tuning system.

As can be seen from this figure, the post-layout simulation of the auto-tuning system is nearly the same as the pre-layout simulation results.

The curves of the power efficiency versus the phase error with or without the auto-tuning circuit are illustrated in Figure 7.9. As can be seen from this figure, the power efficiency can be greatly improved using our proposed auto-tuning system, which can result in an average power savings of nearly 20% compared to the power amplifier without the auto-tuning circuit. The power consumption curve of our circuit is shown in Figure 7.10. The average power consumption of the auto-tuning system in the worst case is only 137 mW, which is much smaller than the saved power and the power consumption of the PCB version (874 mW).

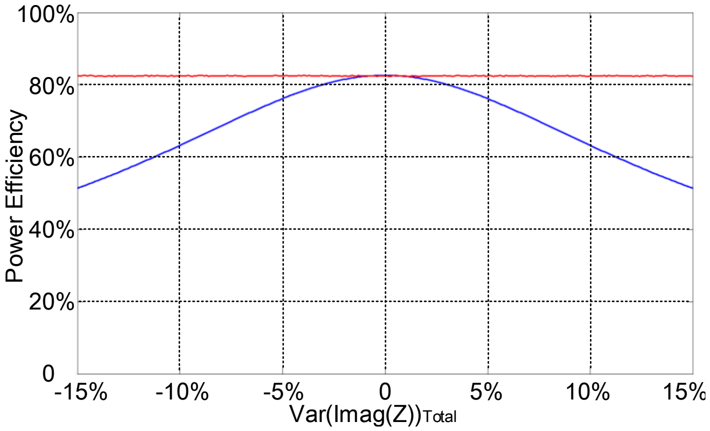


Fig.7.9 Power efficiencies versus phase errors with or without auto-tuning circuit.

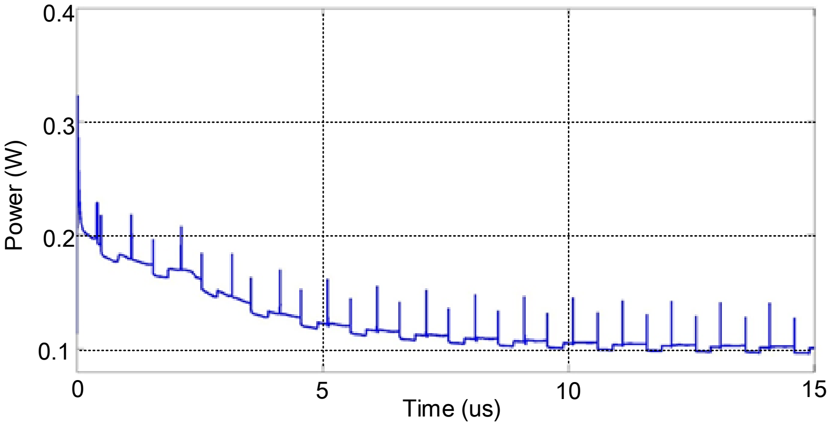


Fig.7.10 Power consumption of the proposed auto-tuning system.

Chapter 8

Conclusions and Future Work

8.1 Conclusions

The objective of this thesis was to design an ultrasonic generator for MRI-guided HIFU applications. The proposed ultrasonic generator is composed of a power amplifier and an auto-tuning system. There were several challenges in the design of the proposed ultrasonic generator:

1. In the real HIFU application, there usually 256 ultrasonic transducers in the phased array. Therefore, the area of the proposed ultrasonic generator needs to be as small as possible.
2. In this thesis, we mainly focus on the MRI guided HIFU system. MRI systems are not compatible with highly magnetic components, and therefore, the use of bulky magnetic components, such as transformers and large inductors, must be avoided.
3. A power amplifier is needed to realize a high efficiency because if the efficiency of the designed power amplifier is low, there will be an overheating problem.
4. The power that is required for the transducer is 3 W, and the peak-to-peak voltage of the power supply is required to be about 260 V. The working frequency of the transducer is 1.25 MHz, so the power amplifier is required to be sufficiently fast.

5. The resettling time of the automatic impedance-tuning network must be as small as possible in order to prevent the reflected power and protect the transducer.

In this thesis, we proposed a half-bridge class D amplifier, which is capable of providing 3 W power with a working frequency of 1.25 MHz and 5 V power supply. The power amplifier was fabricated by using printed circuit board and discrete components that makes it very cheap and easy to fabricate. In other words, it has a very good cost performance ratio. The total price of the proposed circuit is less than 10 €. The power efficiency of the presented amplifier is 82.6% with a total surface area of 10 cm^2. Without using of the bulky magnetic components, it is more compatible with MRI guided HIFU system than the traditional amplifiers.

Besides, we built an electrical model of the ultrasonic transducer, and based on this model we also realized a fast auto-tuning system. The proposed auto-tuning system is based on the topology of synchronous-switched capacitors instead of self inductors or self capacitors. In addition, the inductor used in this auto-tuning system is a small air-core inductor that is compatible with MRI systems. Moreover, this novel auto-tuning system does not require MCUs or PCs for the detection of the impedance variation of ultrasonic transducers.

We presented two versions of auto-tuning systems. The first version was realized using discrete components and a PCB. Test results confirm that this auto-tuning system can effectively compensate the variations of the imaginary part of the transducer's impedance. For this version, the working frequency can reach 1.25 MHz which is the working frequency of the transducer. However, because of the use of discrete components, the area required for the first version of auto-tuning system is 110 cm^2, which is unsuitable for the phased-array HIFU applications. In addition, the power consumption of this version is about half of the saved power, which is uneconomic for our application. Therefore, we designed a second version of the proposed auto-tuning system using an integrated circuit. The proposed integrated auto-tuning circuit consists of three parts: an AGC amplifier, a phase-error detector, and a switch-signal generator. It replaces the AGC board and the phase-error detector board in the first version.

The proposed AGC amplifier has a dB linear gain tuning function, and the variable gain is ranging from -8.82 dB to 29.97 dB with a -3 dB bandwidth from 36 kHz to 8.75 MHz. Moreover, the phase-error detection block combined with the switch signal generation block can transfer the phase error difference into a switch control signal. This switch control signal is always symmetrical with respect to the zero-crossing points of the output signal of the tuning circuit. In other words, the physical impossibility of over current spikes (having theoretically an infinite intensity) flowing through the AC switch is perfectly eliminated by using the proposed circuit.

The area of the proposed integrated auto-tuning circuit is only 0.42 mm^2 instead of 80 cm^2 in the first version. This chip can also offer a wide operation frequency range, which is from 125 kHz to 3 MHz. The power consumption of the IC is only 137 mW, which is also a significant improvement.

8.2 Future Work

The layout of the designed integrated auto-tuning system was sent to the AMS foundry for fabrication via CMP on September 14th, 2015, and the fabricated circuit is expected to be returned towards the end of 2015. The fabricated chip will be tested to verify its performance. In next step, we will optimize the design of the integrated circuit to minimize its surface as well as the power consumption. Moreover, to minimize the area of the whole ultrasonic generator, we will also design the power amplifier used in it by using integrated circuit. In addition to this, we will setup of the test bench in order to test the ultrasonic generator with the real transducer. After the test, if it is possible, we will make a prototype of the power supply to the phased-array HIFU system, and test it with the MRI equipment to verify the performance and compatibility.

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APPENDIX I.

For the PCB version phase error detector, the comparator used in it is MAX961 which has a resolution of 4 mV by using 5V power supply [MAX961]. So, we can known that the phase error caused by the resolution V_R of the comparator can be described by

$$\varphi_{Err} = 2(\sin^{-1}(V_{EA}) - \sin^{-1}(V_{EA} - V_R)) \qquad (1)$$

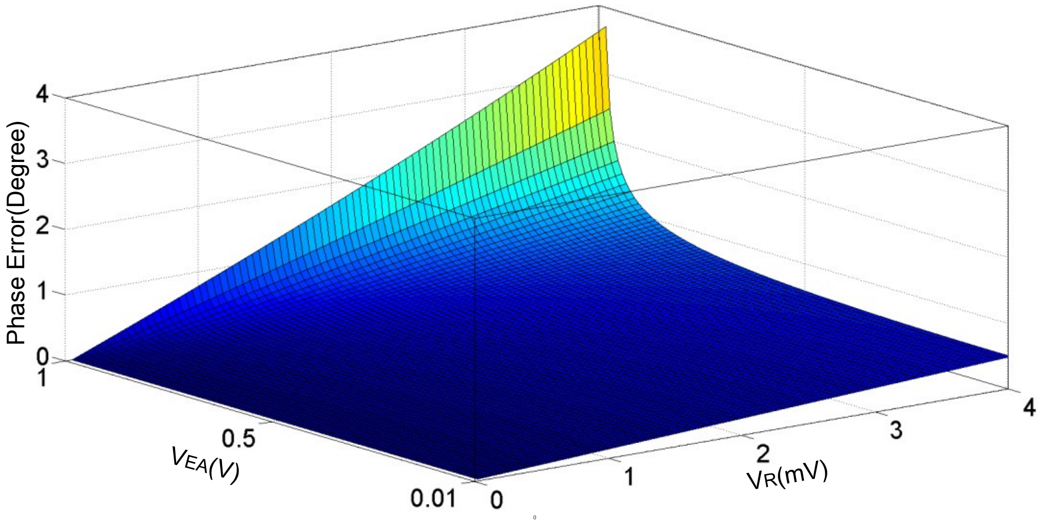

Fig.1 Curve of the phase error caused by the V_R with different V_{EA}.

where V_{PDErr} is the output signal of the phase-error detector. Figure 1 shows the curved surface of the phase error caused by the resolution of the comparator with a different V_{PDErr}. The maximum phase error of the switch-control signal is less than four degrees.

And for the integrated version phase error detector, the comparator used in it has a resolution of 0.5 mV. So, based on Equation (1), we can get the phase error curve caused by the resolution of the integrated comparator. Figure 2 shows the phase error curve. The maximum phase error of the switch-control signal is less than 0.4°.

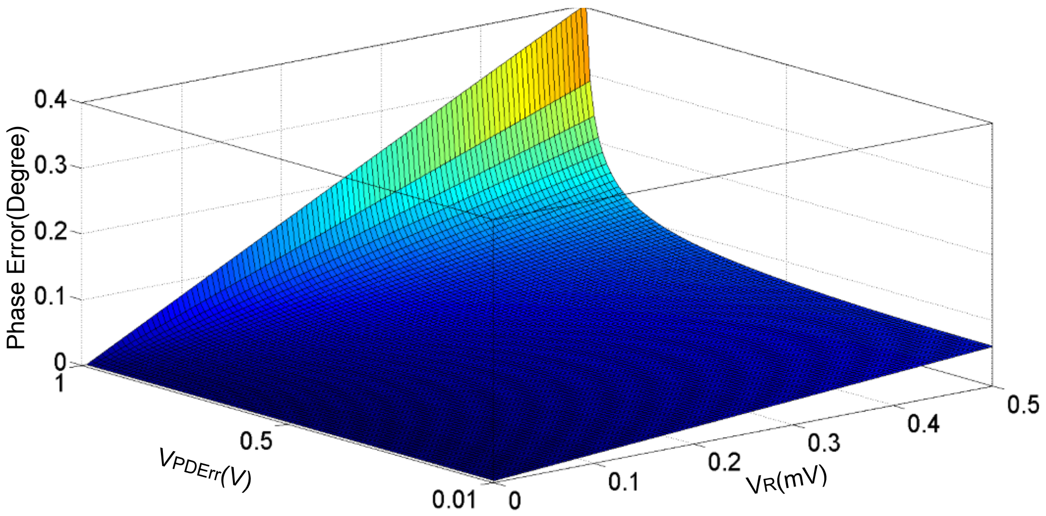

Fig.2 Curve of the phase error caused by V_R with different V_{PDErr}

APPENDIX II.

The phase detector used in our auto-tuning system is an exclusive or (XOR) gate. Therefore, the transfer function of this phase detector can be written as,

$$V_{PD} = \frac{V_{DD}}{\pi}\Delta\theta \tag{1}$$

Where $\Delta\theta$ is the phase difference between Q and $Sgn[V_{CFix}]$. So the discriminator sensitivity of phase detector (K_D) is equal to V_{DD}/π.

The error amplifier used in the proposed auto-tuning system is an integrator. The transfer function of this error amplifier is described by,

$$G_{PDEA}(jw) = \frac{1}{jwR_2C_1} \tag{2}$$

Assume that the settling time of the VCO is zero, the transfer function of the VCO can be described by $\Delta\varphi = K_O V_{EA}$, where K_O is the modulation sensitivity of the VCO. In addition, K_O can be calculated by

$$K_O = \frac{\Delta\varphi_{EA_{max}} - \Delta\varphi_{EA_{min}}}{Max(V_{EA}) - Min(V_{EA})} \tag{3}$$

$Max(V_{EA})=5V$ and $Min(V_{EA})=0$V. And the corresponding C_{SVar} are 324pF and 161pF, respectively. Considering that the proposed impedance circuit is an LC circuit, so the phase difference between the ouput of the tuning network V_{out} and the input V_{in} can be written as,

$$\Delta\varphi = Arg\left|\frac{V_{out}}{V_{in}}\right| = -\frac{\pi}{2} - \tan^{-1}\frac{wL - 1/wC}{r} \tag{4}$$

where $C = C_{Fix} + C_{PLoad} + C_{SVar}$, and r is the equivalent resistance of the tuning circuit. According to Equation 3.48, r can be described by,

$$r = R_L + Z_O + 1/\left(R_{Piez}\left(2\pi f_{working}C_{\mathrm{Piez}}\right)^2\right) = 0.268 \tag{5}$$

Then $\Delta\varphi_{EAmax}$- $\Delta\varphi_{EAmin}$ can be obtained as follows.

$$\Delta\varphi_{EA_{max}} - \Delta\varphi_{EA_{min}} \simeq (15.17° + 14.88°) \cdot \frac{\pi}{180°} \simeq \frac{\pi}{6} \tag{6}$$

Substitute Equation (6) and $Max(V_{EA})=5V$, $Min(V_{EA})=0$V into Equation (3), K_O is written by,

$$K_O = \frac{\pi}{6} \times \frac{1}{5} = \frac{\pi}{30} \tag{7}$$

APPENDIX III.

The proposed design has been implemented in a CMOS 0.35µm technology (C35B4C3) provided by Austrian Micro Systems. We have chosen this technology for its maturity, its accessibility by universities and its reasonable price of fabrication.

Automatic Gain Control Amplifier

The proposed AGC consists of six parts: a VGA, FGA, output buffer, peak detector, error amplifier, and exponential voltage-to-current converter. The layout design of the proposed VGA combined with the FGA, AC coupling circuit, and exponential voltage-to-current converter is illustrated in Figure 3.

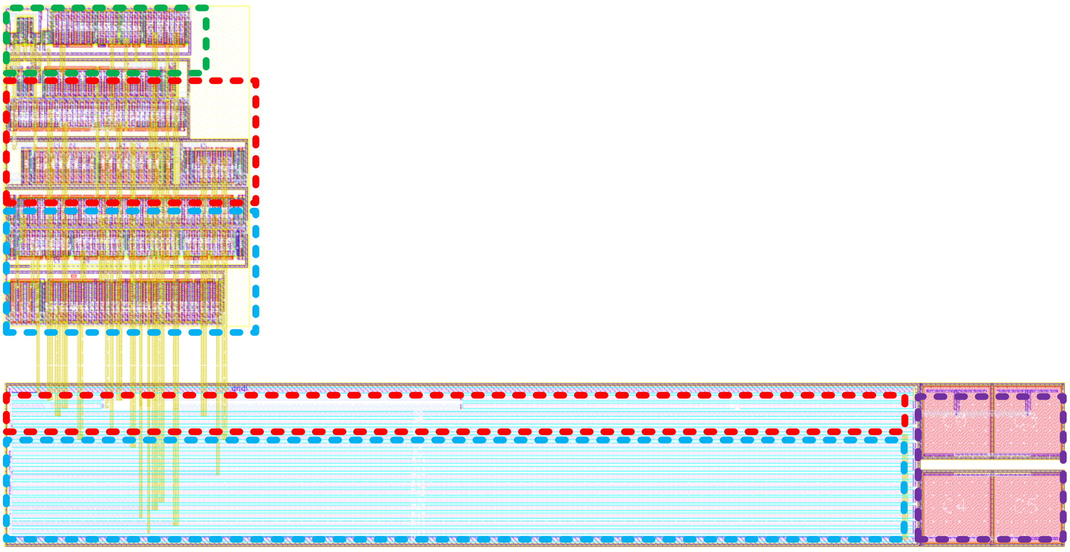

Fig.3 Layout of the proposed VGA combined with FGA and exponential voltage to current converter.

The layout of the proposed VGA is within the area bounded by the red dotted line, while the FGA is bounded by the blue dotted line. The area bounded by the purple dotted line is the AC coupling circuit, and the proposed exponential voltage-to-current converter is illustrated in the area bounded by the green dotted line. We matched the differential pairs and current mirrors used in the VGA, FGA, DCOC, and CMFB circuits by using the common-centroid layout technique [HA2006], and we added a connected dummy in order to obtain extra matching.

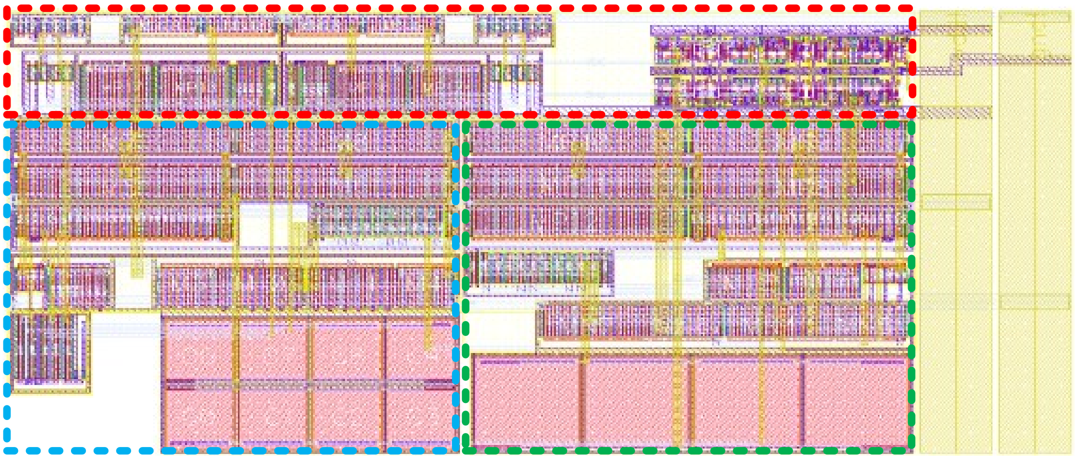

Fig.4 Layout of the proposed peak detector used in the proposed AGC.

Figure 4 is the layout of the designed peak detector. The area bounded by the blue dotted line shows the proposed OTA combined with the current mirror and the capacitors C_h used in the peak detector. The switch-control signal generator of the peak detector is illustrated by the red dotted line. The output buffer of the proposed peak detector is shown by the area bounded by the green dotted line.

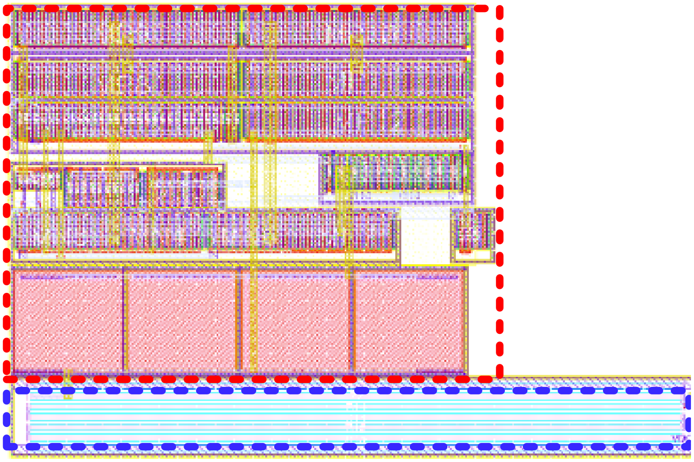

Fig.5 Layout of the output buffer used in the proposed AGC.

The layout of the output buffer designed for the AGC is demonstrated in Figure 5. The designed OPA is shown in the area bounded by the red dotted line, and the resistors used in this output buffer are located within the blue dotted line.

Figure 6 illustrates the layout of the error amplifier. The OPA is surrounded by the red dotted line. The resistors used in this error amplifier are illustrated in the area bounded by the blue dotted line. The capacitors of the error amplifier are realized using an external capacitor.

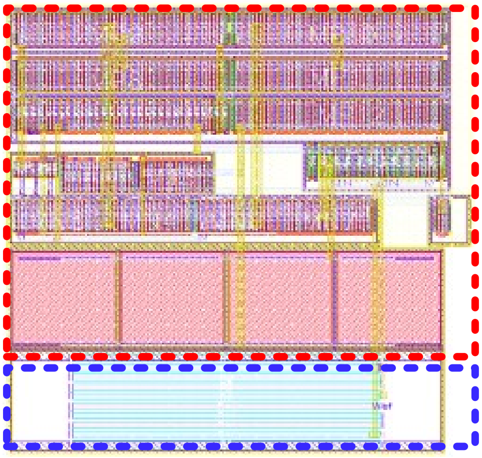

Fig.6 Layout of the error amplifier used in the proposed AGC.

Phase Error Detector

The phase-error detector of the auto-tuning system is composed of a phase detector and a phase-error amplifier. The layout of the phase-error detector is displayed in Figure 7. The designed comparator of the phase detector is shown by the red rectangle, and the XOR gate is shown in the blue rectangle.

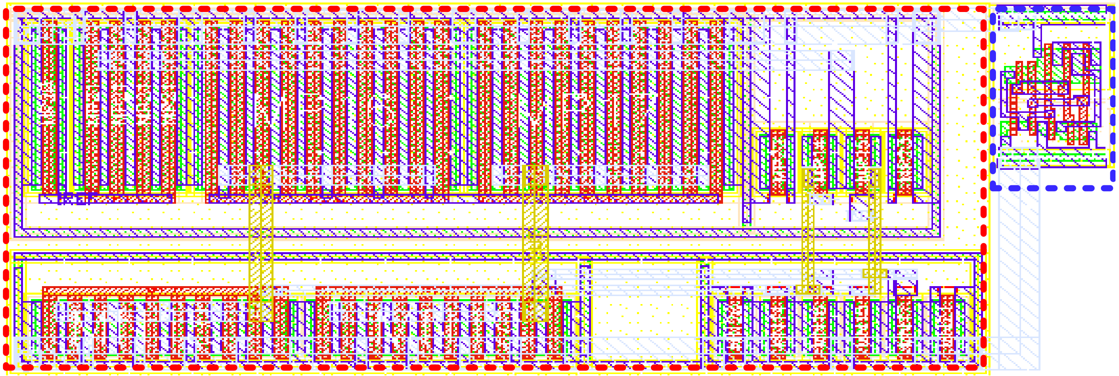

Fig.7 Layout of the phase detector.

The error amplifier of the phase-error detector is shown in Figure 8. The OPA used in this error amplifier is the same as the one used in the error amplifier of the peak detector. The resistors of this error amplifier are displayed by the blue dotted line. The capacitors used in this error amplifier are also out-chip capacitors.

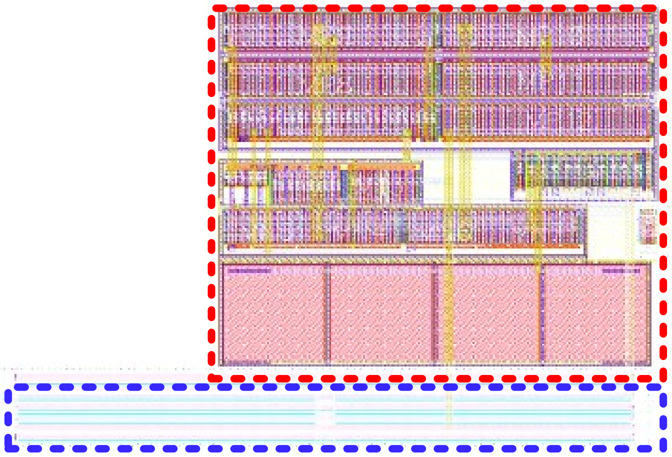

Fig.8 Layout of the error detector designed for the phase-error detector.

Switch Signal Generator

The layout view of the switch-signal generator of the auto-tuning system is shown in Figure 9. This circuit is composed of two comparators, a unity-gain inverting amplifier, and a NOR gate. The unity-gain inverting amplifier is demonstrated in the blue rectangle, and the comparators combined with the NOR gate are shown in the red rectangle.

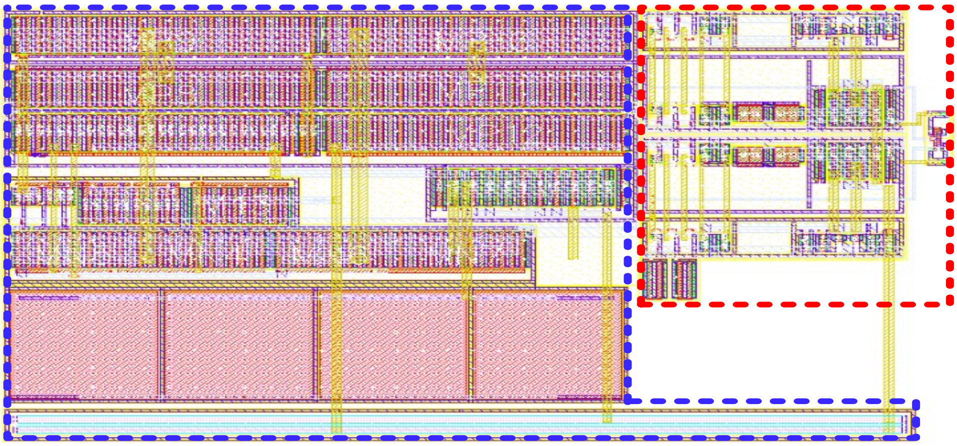

Fig.9 Layout of the error detector designed for the phase-error detector.

Bandgap Reference Circuit

The layout of the bandgap reference circuit is shown in Figure 10. The PNP BJTs used in the bandgap reference are centrosymmetric, and all of the current mirrors used in this bandgap circuit are matched by using the connected dummy.

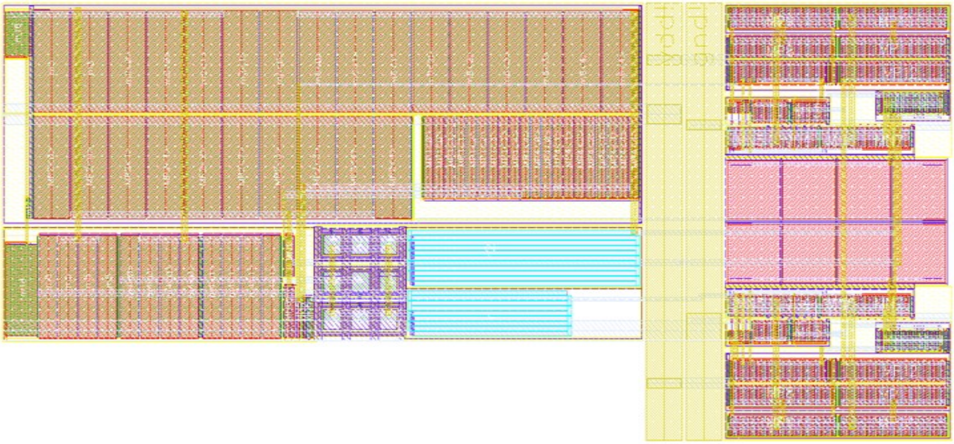

Fig.10 Layout of the proposed bandgap reference circuit.

ÉCOLE DOCTORALE
Physique et ingénierie :
électrons, photons,
sciences du vivant (EOBE)

Titre : Générateur d'ultrasons pour les applications chirurgicales et le traitement non-invasif du cancer par high intensity focused ultrasound

Mots clés : Transducteur ultrasonique ; HIFU ; réglage d'impédance automatique ; condensateur échangé ; alimentation électrique ultrasonique ; amplificateur de la Classe D de demi-pont.

Résumé : La technique de haute intensité ultrasons focalisés (HIFU) est maintenant largement utilisée pour le traitement du cancer, grâce à son avantage non-invasif. Dans un système de HIFU, une matrice de transducteurs à ultrasons est pilotée en phase pour produire un faisceau focalisé d'ultrasons (1M ~ 10 MHz) dans une petite zone de l'emplacement de la cible sur le cancer dans le corps. La plupart des systèmes HIFU sont guidées par imagerie par résonance magnétique (IRM) dans de nos jours. Dans cette étude de doctorat, un amplificateur de puissance de classe D en demi-pont et un système d'accord automatique d'impédance sont proposés. Tous deux circuits proposés sont compatibles avec le système IRM. L'amplificateur de puissance proposé a été réalisé par un circuit imprimé (PCB) avec des composants discrets. Selon les résultats du test, il a rendement de conversion en puissance de 82% pour une puissance de sortie conçue de 1,25W à une fréquence de travail de 3MHz. Le système d'accord automatique d'impédance proposé a été conçu en deux versions: une version en PCB et une version en circuit intégré (IC). Contrairement aux systèmes d'accord automatique proposés dans la littérature, il n'y a pas besoin de l'unité de microcontrôleur (MCU) ou de l'ordinateur dans la conception proposée. D'ailleurs, sans l'aide de composants magnétiques volumineux, ce système d'auto-réglage est entièrement compatible avec l'équipement IRM. La version en PCB a été conçue pour vérifier le principe du système proposé, et il est également utilisé pour guider à la conception du circuit intégré. La réalisation en PCB occupe une surface de 110cm^2. Les résultats des tests ont confirmé la performance attendue. Le système d'auto-tuning proposé peut parfaitement annuler l'impédance imaginaire du transducteur, et il peut également compenser l'impédance de la dérive causée par les variations inévitables (variation de température, dispersion technique, etc.). La conception du système d'auto-réglage en circuit intégré a été réalisé avec une technologie CMOS (C35B4C3) fournies par Austrian Micro Systems (AMS). La surface occupée par le circuit intégré est seulement de 0,42mm^2. Le circuit intégré conçu est capable de fonctionner à une large gamme de fréquence tout en conservant une consommation d'énergie très faible (137 mW). D'après les résultats de la simulation, le rendement de puissance de ce circuit peut être amélioré jusqu'à 20% comparant à celui utilisant le réseau d'accord statique.

ÉCOLE DOCTORALE
Physique et ingénierie : électrons, photons, sciences du vivant (EOBE)

Title : Ultrasonic generator for surgical applications and non-invasive cancer treatment by high intensity focused ultrasound

Keywords : Ultrasonic transducer; HIFU; Automatic impedance tuning; Switched capacitor; Ultrasonic power supply; Half-bridge Class D amplifier.

Abstract : High intensity focused ultrasound (HIFU) technology is now broadly used for cancer treatment, thanks to its non-invasive property. In a HIFU system, a phased array of ultrasonic transducers is utilized to generate a focused beam of ultrasound (1M~10MHz) into a small area of the cancer target within the body. Most HIFU systems are guided by magnetic resonance imaging (MRI) in nowadays. In this PhD study, a half-bridge class D power amplifier and an automatic impedance tuning system are proposed. Both the class D power amplifier and the auto-tuning system are compatible with MRI system. The proposed power amplifier is implemented by a printed circuit board (PCB) circuit with discrete components. According to the test results, it has a power efficiency of 82% designed for an output power of 3W at 1.25 MHz working frequency. The proposed automatic impedance tuning system has been designed in two versions: a PCB version and an integrated circuit (IC) version. Unlike the typical auto-impedance tuning networks, there is no need of microprogrammed control unit (MCU) or computer in the proposed design. Besides, without using bulky magnetic components, this auto-tuning system is completely compatible with MRI equipment. The PCB version was designed to verify the principle of the proposed automatic impedance tuning system, and it is also used to help the design of the integrated circuit. The PCB realization occupies a surface of 110cm^2. The test results confirmed the expected performance. The proposed auto-tuning system can perfectly cancel the imaginary impedance of the transducer, and it can also compensate the impedance drifting caused by unavoidable variations (temperature variation, technical dispersion, etc.). The IC design of the auto-tuning system is realized in a CMOS process (C35B4C3) provided by Austrian Micro Systems (AMS). The die area of the integrated circuit is only 0.42mm^2. This circuit design can provide a wide working frequency range while keeping a very low power consumption (137 mW). According to the simulation results, the power efficiency can be improved can up to 20% by using this auto-tuning circuit compared with that using the static tuning network.