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# Low temperature devices (FDSOI, TriGate) junction optimization for 3D sequential integration

Luca Pasini

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Communauté UNIVERSITÉ Grenoble Alpes

# THÈSE

Pour obtenir le grade de

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Présentée par


## Luca PASINI


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codirigée par **Perrine BATUDE et Mikael CASSE**

préparée au sein du **CEA LETI et STMicroelectronics**
dans **l'École Doctorale Electronique, Électrotechnique, Automation et Traitement du Signal**

# Optimisation des jonctions de dispositifs (FDSOI, TriGate) fabriqués à faible température pour l'intégration 3D séquentielle

# Low temperature devices (FDSOI, TriGate) junction optimization for 3D sequential integration

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# Introduction and context of this work

Since the introduction on the market of the first microprocessor by INTEL in 1971, the reduction of the MOSFET transistor dimensions has been the driving force of the growth of the semiconductor market. This scaling trend has followed the so called Moore's law [Moore 65], which predicts that the number of transistors per Integrated Circuits (IC) is doubled every 18 months. This prediction has been basically respected until nowadays, for example with the fabrication of the 28 nm technological node with the FDSOI planar technology by STMicroelectronics and even the 14 nm FinFET technology proposed by INTEL. These ultra-scaled dimensions are approaching to both technological and physical limits concerning the device fabrication and operation: the miniaturization of device feature requires more complex photolithography and etching systems, raising the production cost [Khorram12]. Reliability and variability [Kuhn 11], are also becoming serious concerns as device dimensions scale down. The scaling has also given rise to the increase of parasitic phenomena such as short channel effects (SCE). As a consequence, solutions have to be developed in order to overcome these problems. In particular, for actual technology nodes, new architectures have been introduced such as planar fully depleted Silicon on Insulator (FDSOI) devices or multiple gates FETs [Kuhn 11]. Planar FDSOI, TriGate and FinFET architectures are considered up to 10 nm node depending on the semiconductor company strategy. Beyond, multiple gates or gate all–around FET [Bangsaruntip 09] or even the introduction of non-based silicon technology such as III-V materials [Czornomaz 13], might be mandatory to ensure high performance and gate control of the channel.

In addition, with the increase of the number of transistor, the interconnection length increases more and more becoming one of the main sources of circuit performance limitation rather than the single transistor performance. Therefore, alternative solutions also have to be found in terms of circuit design.

## I.1 3D Sequential Integration

An alternative path to planar scaling can be brought by a 3D integration scheme which consists in stacking the transistor levels rather than reducing the devices dimensions. 3D integration can refer to 3D parallel integration, where different chips are processed independently and stacked vertically afterward as shown schematically in Figure I.1. The connection between the stacked layers can be, for example, Through– Silicon Vias (TSV).

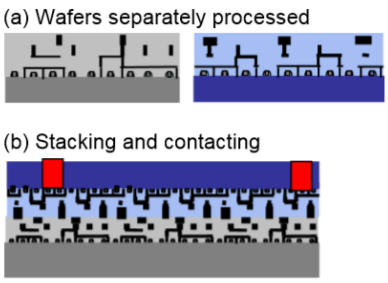



**Figure I.1: Description of parallel integration process flow. (a) Wafers are processed separately (b) stacked and the contacted afterwards.**

However, this method is limited to connecting blocks of a few thousands of transistors and the interconnection density is limited by the alignment precision of bonding [Koyanagi 09]. An alternative technique is represented by the 3D sequential integration [Batude 11a]. In this integration scheme, transistor layers are processed sequentially and the stacked layers can be connected at the transistor scale as shown schematically in Figure I.2. This integration offers higher integration density thanks to its much higher alignment accuracy (approximately 10 nm against 0.5 µm for parallel integration), making full use of the third dimension.

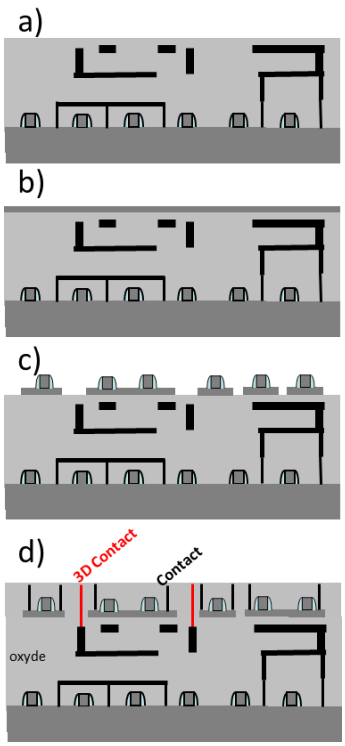



**Figure I.2: Description of 3D sequential integration process flow where transistor layers are processed sequentially. (a) The bottom transistor layer is processed, (b) top active zone is fabricated, (c) first lithographic pattern of the top layer (d) the layers are then contacted.**

One of the main challenges of the 3D sequential integration is the development of a low temperature process flow for the top transistor level in order to avoid the degradation of the bottom one. The most critical process step for the top transistor level fabrication is the dopant activation that is

conventionally performed by spike annealing at temperature higher than 1000 °C. This thermal budget is not acceptable for the integrity of the bottom level. In [Fenouillet 14] it is reported that bottom transistor performance stability is dependent on the considered technology and, for example, is maintained for annealings at 500 °C for 5 hours and 550 °C for 2 hours in the case of a 14 nm FDSOI. It is worth noticing that both temperature and time are important for the definition for the maximum thermal budget. Therefore, short anneals, such as DSA (Dynamic Surface Anneal) laser, shows negligible performance degradation at 800 °C for 0.3 ms [Batude 15]. For this reason, laser anneal in the range of nanoseconds appears a promising candidate for dopant activation of the top level even though the local temperature can reach 1200 °C.

One of the possible options considered is to activate the dopants through solid phase epitaxial regrowth (SPER), which mechanism will be described later, using annealing temperature below 600 °C instead of conventional spike anneals. This is compatible with a 3D sequential integration scheme as shown in Figure I.3. The work of this thesis will focus on low temperature dopant activation by SPER.

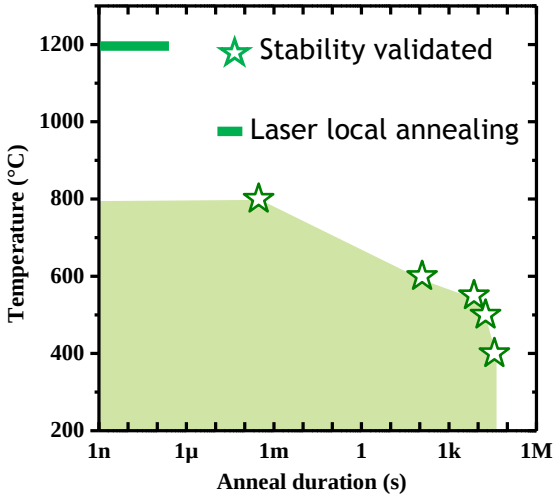



**Figure I.3: Summary of thermal budgets tested on 14nm FDSOI technology with preserved N &PFET $I_{ON}$-$I_{OFF}$ performance [Batude 15].**

CEA-LETI named the 3D sequential integration scheme with the low temperature process for the top transistor level as CoolCube technology. The simplified CoolCube process flow to integrate sequentially two transistor levels is illustrated schematically in Figure I.4. The bottom transistor is processed with a conventional high temperature thermal budget (Figure I.4a). Then, the top film layer is obtained via a low temperature direct bonding of an SOI substrate enabling the full transfer of a monocrystalline silicon layer (Figure I.4b). Finally, the top transistor is fabricated using a low temperature budget process (Figure I.4c). Figure I.5 shows a Transmission Electron Microscopy (TEM) cross-section image of two stacked transistors after the source and drain epitaxial growth of the top transistor level [Batude 15].

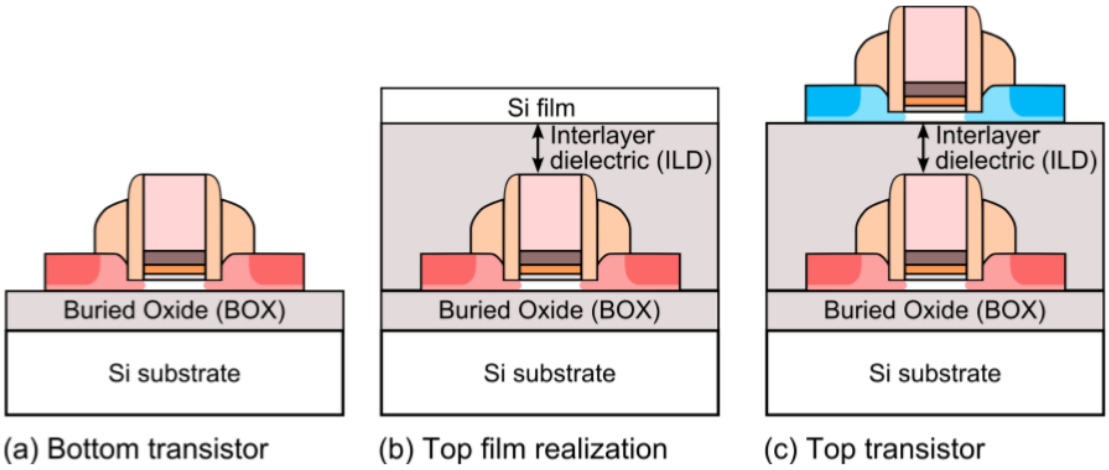



**Figure I.4: Description of the 3D sequential integration scheme process.**

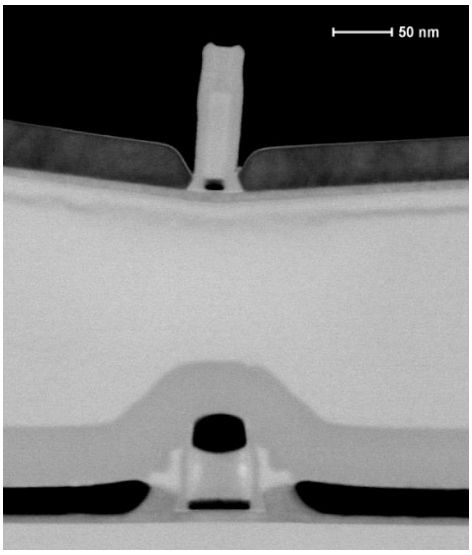



**Figure I.5: TEM observation of stacked transistors fabricated using the 3D sequential integration scheme [Batude 15].**

## I.2 Goals of this work

As discussed in the previous section, the most critical process step for the top transistor level in 3D sequential integration is the dopant activation. The goal of this thesis is to develop and integrate low temperature dopant activation in electrical devices and obtaining the same performance as devices fabricated using the Process Of Reference (POR) at high temperature.

In chapter one, the sheet resistance optimization on full sheet wafer after low temperature dopant activation is investigated. In order to reduce the thermal budget, the velocity of the dopant activation step is studied as well.

In the second chapter, the doping conditions optimization obtained in chapter one are integrated in FDSOI devices. A detailed analysis of electrical performance has been carried out with the support of TCAD simulation.

In chapter three, an alternative integration scheme, named extension first, is proposed for the low temperature device optimization. The technological challenges are first presented followed by the electrical characterization of advanced FDSOI devices fabricated with this integration scheme.

In chapter four, an alternative technique is used for the optimization of the low temperature devices: the heated implantation. First, a basic study is presented in order to familiarize with the properties of this technique. Then, heated implantation has been integrated on FDSOI devices process flow using the extension last integration scheme and in TriGate devices using the extension first integration scheme.

**References**

[Bangsaruntip 09] Bangsaruntip, S., et al. "High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling." Electron Devices Meeting (IEDM), 2009 IEEE International. IEEE, 2009.

[Batude 11] P. Batude, M. Vinet, B. Previtali, C. Tabone, C. Xu, J. Mazurier, O. Weber, F. Andrieu, L. Tosti, L. Brevard, B. Sklenard, P. Coudrain, S. Bobba, H. Ben Jamaa, P. Gaillardon, A. Pouydebasque, O. Thomas, C. Le Royer, J. Hartmann, L. Sanchez, L. Baud, V. Carron, L. Clavelier, G. De Micheli, S. Deleonibus, O. Faynot and T. Poiroux. Advances, challenges and opportunities in 3D CMOS sequential integration. In Electron Devices Meeting (IEDM), 2011 IEEE International, pages 7.3.1–7.3.4, 2011.

[Batude 15], Batude P., et al. "3DVLSI with CoolCube process: An alternative path to scaling." VLSI Technology (VLSI Technology), 2015 Symposium on. IEEE, 2015.

[Czornomaz 13], L., et al. "Co-integration of InGaAs n-and SiGe p-MOSFETs into digital CMOS circuits using hybrid dual-channel ETXOI substrates." Electron Devices Meeting (IEDM), 2013 IEEE International. IEEE, 2013.

[Fenouillet 14] Fenouillet-Beranger, C., et al. "New insights on bottom layer thermal stability and laser annealing promises for high performance 3D VLSI." Electron Devices Meeting (IEDM), 2014 IEEE International. IEEE, 2014.

[Khorram 12] H. R. Khorram, K. Nakano, N. Sagawa, T. Fujiwara, Y. Iriuchijima, T. Sei, T. Takahiro, K. Nakamura, K. Shiraishi, and T. Hayashi, “Cost of Ownership/Yield Enhancement of High Volume Immersion Lithography Using Topcoat-Less Resists,” IEEE Transactions on Semiconductor Manufacturing, vol. 25, pp. 63 -71, Feb 2012.

[Koyanagi 09] M. Koyanagi, “New 3D integration technology and 3D system LSIs”, Proceedings of the 2009 VLSI Technology Symposium, pp. 64 -67, 2009.

[Kuhn 11] K. J. Kuhn, M. D. Giles, D. Becher, P. Kolar, A. Kornfeld, R. Kotlyar, S. T. Ma, A. Maheshwari, and S. Mudanai, “Process Technology Variation,” IEEE Transactions on Electron Devices, vol. 58, pp. 2197 2208, Aug 2011.

[Moore 65] G. E. Moore, “Cramming More Components Onto Integrated Circuits”; Electronics Magazine; Vol. 38, No. 8, pp. 114-117; 1965.

# Chapter 1: Dopant activation optimization by SPER

In this chapter, the mechanism and properties of dopant activation by solid phase epitaxial regrowth at low temperature are introduced. The optimization of the doping profile in order to minimize the sheet resistance for a dopant activation at low temperature is presented in a second section. Finally, a study of the crystallization rate optimization will be proposed in order to reduce the annealing temperature of the dopant activation step.

## 1.1 Basic principles and definitions

### 1.1.1 Dopant implantation

One of the most common techniques to introduce dopant impurities into the silicon substrate is the ion implantation. This method consists in accelerating the ions in an electrical field in order to give them enough kinetic energy to make them penetrate into the solid target. The collision cascade resulting from the impact of the implanted atom with the target lattice creates crystalline damage, commonly named as defects. The concentration of these induced defects depends on the type of implanted species, its dose and its energy [Hobler 03].

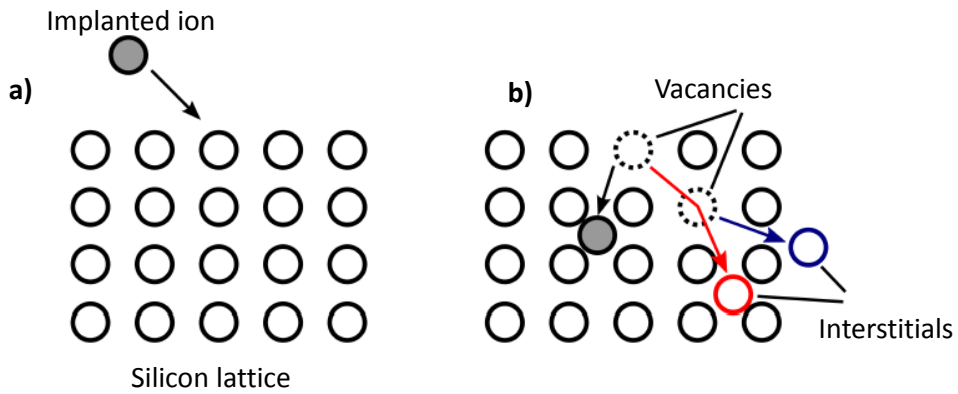



**Figure 1.1: Schematic representation of ion implantation. (a) An incident ion affects the silicon lattice. (b) The implanted ion can cause target atoms to be knocked out of their lattice position (interstitial) leaving a missing atom in the lattice (vacancy).**

Figure 1.1 shows a schematic representation of ion implantation. An incident ion affects the crystalline lattice (Figure 1.1a) causing a displacement of a silicon atom out of its lattice position (Figure 1.1b). Hence, there is a lattice site with a missing atom called vacancy (dotted circle) and an extra silicon atom called interstitial (colored circle). Interstitials and vacancies can be generally defined as punctual defects (contrarily than extended defects, consisting in stable agglomeration of punctual defects). The

interstitials move into the silicon lattice because of the kinetic energy that transferred during the collision. They can also knock out other crystal atoms and create further implant defects through collision cascades.

An empirical method to evaluate when crystalline materials turns into amorphous phase is related to the density of defects. [Sentaurus] considers a threshold value of $2x10^{22}$ $cm^{-3}$ for silicon. For a densisty of defects higher than this value the material can be considered as amorphous. However, the kinetic energy of the incident ion is dependent on the dopant specie through its atomic mass, i.e. the lighter the incident ion, the less lattice defects it will introduce. For the implantation conditions used in this work, boron implantation does not produce enough quantity of defects to turns the crystal silicon into its amorphous phase. Since amorphization is necessary in SPER to reach efficient dopant activation at low temperature annealings (as detailed in next sections), a pre-amorphization (PAI) step with a heavy specie is needed for boron doping. In this work, germanium has been chosen as the PAI specie.

### 1.1.2 Dopant activation

The crystalline character of the silicon can be recovered by the application of a thermal anneal after the implantation to drive the system to a thermodynamic equilibrium state. Two different mechanisms can lead to the crystallization of the amorphous region:

- **SPER (Solid Phase Epitaxial Regrowth)**: in the presence of a crystalline template the amorphous region is regrown epitaxially layer–by–layer from the amorphous/crystalline (a/c) interface as schematically reported in Figure 1.2. During the solid–solid transition from amorphous to crystalline phase, the dopant impurities can be substitutionally incorporated into the lattice positions where they are electrically active. SPER has been characterized by many authors [Skorupa 14] and it has been shown to follow an Arrhenius behavior, with an activation energy for intrinsic silicon of approximately 2.7 eV. The SPER rate dependence on temperature and impurities concentration will be extensively studied in section 1.3.
- **RNG (Random Nucleation and Growth):** re-crystallization may also occur inside the amorphous phase through random nucleation and growth, as illustrated in Figure 1.3. RNG consists in the nucleation of small agglomerates that further expand into crystallites. This crystallization mechanism leads to a polycrystalline silicon. As the solid phase epitaxy, random nucleation is governed by an Arrhenius behavior, with high activation energy of approximately 4 eV. Thus, if crystalline seed is present, the SPER will occur before RNG due to the lower activation energy.

At the thermodynamic equilibrium, there is a maximum quantity of dopants that can be incorporated into the silicon without the creation of a different phase. This maximum concentration is named solid solubility limit. Conventional dopants used in microelectronics have a relatively high solid solubility in silicon and tend to occupy substitutional site positions at equilibrium where they are electrically active. However, for some species, at a concentration below solubility limit, it becomes energetically more favorable to form electrically inactive dopant complexes. In that case, the solubility limit does not correspond to the maximum dopant activation. It has to be pointed out that this distinction may lead to some confusions in the literature since some authors consider the solubility limit as the activation limit. For the purpose of this work, the parameter of interest is the maximum active dopant concentration.

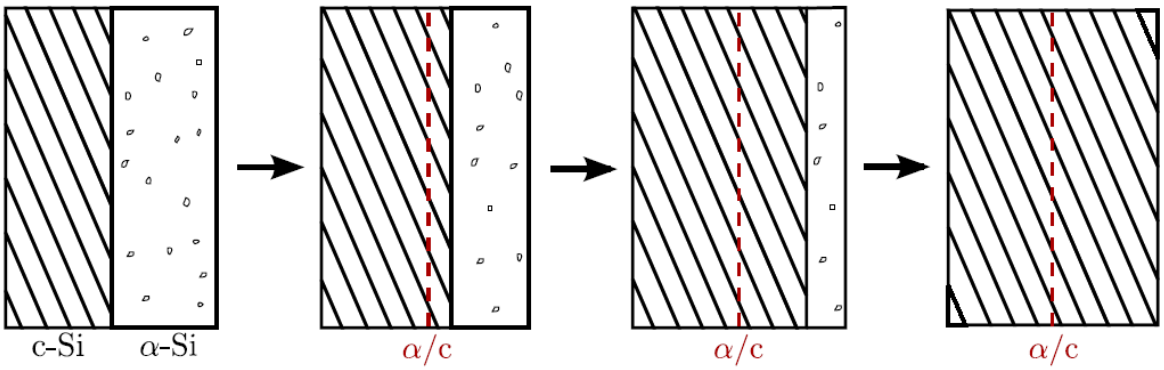



**Figure 1.2: SPER mechanism consists in a re-crystallization layer by layer starting from the crystalline seed.**

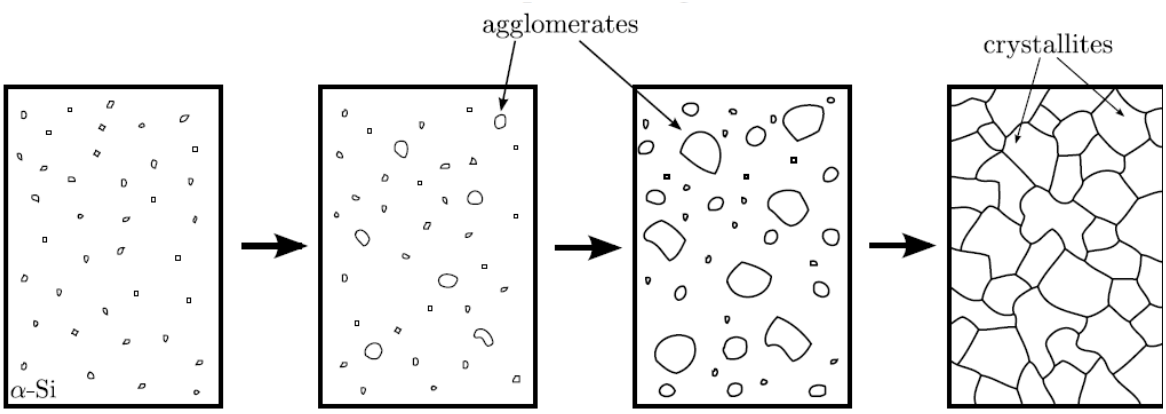



**Figure 1.3: RNG process consist in the nucleation of small agglomerates that further expand into crystallites.**

Maximum active dopant concentration can be empirically modeled by an Arrhenius behavior: $[Dopant]_{maxAct} = C_0 \cdot exp\left(-\frac{E_a}{KT}\right)$. Prefactor $C_0$ and activation energy $E_a$ have been extracted for boron [Solmi 90], phosphorus [Nobili 94] and arsenic [Nobili 94] obtaining the equations (1.1)-(1.3) reported below:

$$[B]_{maxAct} = 9.25 \cdot 10^{22} \cdot exp\left(-\frac{0.73}{KT}\right) \tag{1.1}$$

$$[P]_{maxAct} = 9.2 \cdot 10^{21} \cdot exp\left(-\frac{0.33}{KT}\right) \tag{1.2}$$

$$[As]_{maxAct} = 2.2 \cdot 10^{22} \cdot exp\left(-\frac{0.47}{KT}\right) \tag{1.3}$$

Figure 1.4 shows the maximum active concentration for boron, phosphorus and arsenic in function of the annealing temperature obtained using equations (1.1) - (1.3).

It is worth noticing that the concept of maximum active concentration (and solid solubility limit) is defined under the hypothesis of thermodynamic equilibrium.

During SPER, dopant atoms confined in the as–implanted amorphous layer are incorporated into crystal lattice sites at concentration levels exceeding the solid solubility of the impurity in silicon [Narayan 82], [Duffy 06]. Therefore, SPER allows reaching very high activation levels, which are particularly suitable for the junction formation of advanced electrical devices. In particular, high activation level is achievable at low temperature anneals (below 600 °C). The maximum achievable active concentration is often called metastable solubility. In this work it will be named clustering limit because for dopant concentration above this high activation level, dopants form inactive cluster. The situation corresponds to a metastable equilibrium and with further annealing the system returns to thermodynamic equilibrium (i.e. solid solubility).

In next sections, clustering limit for phosphorus, arsenic and boron will be extracted for SPER activation at 600°C. The effect of a subsequent applied thermal annealing will be studied as well.

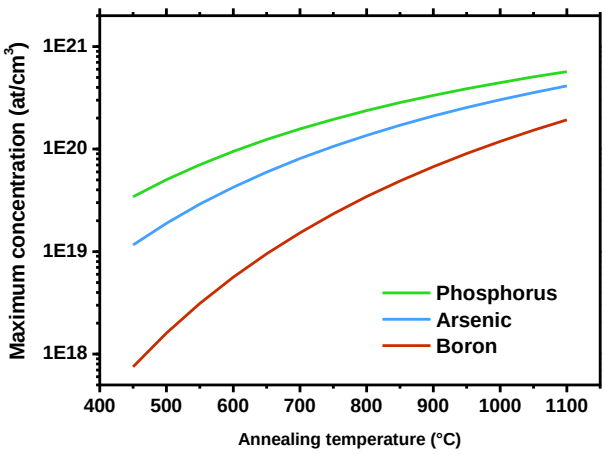



**Figure 1.4: Maximum active concentration for boron, arsenic and phosphorus as a function of annealing temperature.**

## 1.2 Optimization of doping activation level by SPER

In the previous section it has been noticed that SPER needs a crystalline template in order to promote the crystallization during the thermal anneal. For this reason, implant conditions have to be chosen in order to obtain a partial amorphization of the silicon substrate and preserving a crystalline region on the bottom edge, so-called crystalline seed. In this study, SPER activation will be used for the dopant activation on FDSOI devices. The characteristic thickness of the access regions for this kind of device is approximately 22 nm. So, blanket SOI wafers, with a 22.5 nm thick silicon film over a 145 nm thick buried oxide, were used to a first study on SPER characteristics. The wafer configuration is shown in Figure 1.5. At the moment of implantation step, a thin native oxide layer of approximately 1.5 nm is present at silicon surface, due to the natural silicon oxidation.

A simple technique used to characterize the efficiency of the doping activation after thermal anneal is the four-point probe method. This technique allows to obtain an extremely reliable (measurement incertitude below 1%) measure of sheet resistance ($R_{SHEET}$) value. Sheet resistance can be expressed by:

$$R_{sheet} = \frac{1}{\int_0^{x_j} \mu(x)C(x)dx} \quad (1.4)$$

Where C(x) is the active carrier concentration profile, μ(x) is the carrier mobility profile and $x_j$ is the thickness of the implanted region. In this work, the thickness considered as $x_j$ is equal to the amorphization depth after implantation. This choice rises from the fact that SPER mechanism leads to high dopants activation only in the amorphized region [Demenev 12], [Martinez-Limia 08]. This hypothesis neglects the active dopant presents in the crystalline seed.

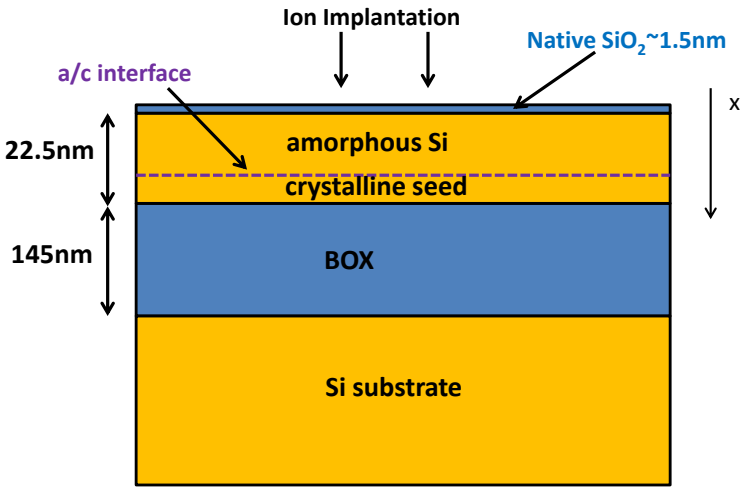



**Figure 1.5: Scheme of full sheet SOI sample used for SPER analysis.**

Equation (1.1) contains both carrier concentration and mobility factors. These two parameters are correlated by the behavior reported in Figure 1.6 extracted by [Masetti 83]. However, once again, this behavior corresponds to condition of thermodynamic equilibrium. Since SPER is a non-equilibrium process, this behavior can be different. This point will be discussed in the following sections.

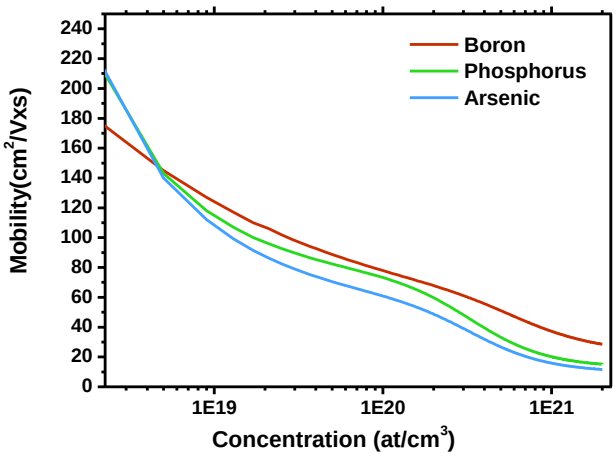



**Figure 1.6: Mobility-concentration behavior at thermodynamic equilibrium for boron, phosphorus and arsenic as a function of the concentration [Masetti 83].**

### 1.2.1 n-type doping implantation and SPER activation: sheet resistance analysis

So far, only few papers in the literature [Woodard 06] have analyzed the junction optimization activated by SPER in terms of implantation conditions and sheet resistance results. In particular, no detailed studies describing the challenges and solutions for Fully Depleted Silicon On Insulator (FDSOI) access optimization are available at our knowledge. The low temperature junction optimization is not straightforward and is far from standard FDSOI high temperature process of reference (POR), as it will be discussed and highlighted in this section.

Samples described in Figure 1.5 have been implanted with different conditions and then annealed to activate the dopants by SPER. The different implantation and annealing conditions are listed in Table 1.1. In order to verify experimentally the thickness of the crystalline seed $t_{seed}$ predicted by KMC simulations reported in Table 1, Transmission Electron Microscopy (TEM) measurement has been performed on the as-implanted sample 5 (S5). The TEM image in Figure 1.7 clearly shows a crystalline silicon seed with a thickness ranging from 3.5 to 5.5 nm. This thickness variation is due to the amorphous/crystalline (a/c) interface roughness. So, we can consider that $t_{seed}$ value extracted from KMC simulation is correct within a range of ±2 nm. For both first (S1) and second (S2) samples, the doping conditions correspond to the ones used in the Process Of Reference (POR) for the state of the art FDSOI technology. It consists of four different implantations combining phosphorus and arsenic with a total dose of $5.5 \times 10^{15}$ at/cm$^2$. After the implantation, S1 has been subjected to spike annealing at 1050 °C (POR activated anneal) while S2 was treated with a low temperature anneal at 600 °C for 2 minutes.

| Sample | S1 | S2 | S3 | S4 | S5 | S6 |
|---|---|---|---|---|---|---|
| Annealing | HT | LT | LT | LT | LT | LT |
| Dopant | As+P | As+P | As | As | P | P |
| Dose ($x10^{15}$ at/cm$^2$) | 5.5 | 5.5 | 3 | 1 | 1.7 | 1 |
| $t_{seed}$ layer (nm) | 5(*) | 5 | 5 | 5 | 5 | 7 |

**Table 1.1: Samples description with type of annealing, dopants implanted doses and crystalline seed thickness. (*)HT activation is not limited to the amorphized region.**

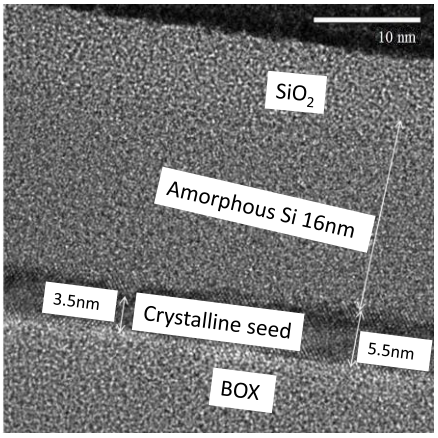



**Figure 1.7: TEM image of Sample 5 after phosphorus high dose implantation.**

Sheet resistance measurements have been performed on these six annealed samples and the results are reported in Figure 1.8. A significant degradation of 86% in sheet resistance is observed for S2 compared to S1. This clearly highlights that the process of reference implantation conditions that are optimized for the high temperature spike activation anneal (S1) are not adequate for low temperature SPER activation process (S2). In order to understand this effect, four different doping conditions (S3 to S6 in Table 1.1) have been tested. In samples S3 and S4, only arsenic implantations have been performed at different doses. Samples S5 and S6 have been implanted with phosphorus only, also varying the implantation dose. It was observed that reducing the total dose of dopants allows a great improvement of sheet resistance. Reducing the dose from $3\times10^{15}$ at/cm$^3$ (S3) down to $1\times10^{15}$ at/cm$^3$ (S4) leads to a 25% gain in sheet resistance. Similar improvement is observed in the sheet resistance value for phosphorus samples when implantation dose is reduced from $1.7\times10^{15}$ at/cm$^3$ (S5) to $1\times10^{15}$ at/cm$^3$ (S6). This last sample shows significant improvement (18%) of sheet resistance value even compared to S1, where process of reference implant conditions and spike annealing have been used. Finally, comparing phosphorus (S6) and arsenic (S4) low dose samples, phosphorus appears to lead to an additional gain but at this stage additional analysis is needed, as will be detailed in sections 1.2.2 and 1.2.3.

To fairly compare the activation levels, it is first necessary to take into account the specificity of SPER activation at temperature below 600 °C, i.e. where dopants are efficiently activated only in the former amorphized region.

Resistivity is the key parameter that allows a better comparison of the activation level. In fact, it depends on the carrier concentration and mobility and is independent of the junction depth, as shown in equation (1.5):

$$\rho(x) = \frac{1}{C(x)\mu(x)} \tag{1.5}$$

The obtained results are reported in Figure 1.9, where similar trends to sheet resistance behavior (Figure 1.8) are observed. Strikingly, it has to be noted that sample implanted with low dose phosphorus and activated at low temperature by SPER (S6) outperforms even more clearly the resistivity of the process of reference sample (S1). On the other hand, S2 still exhibits a higher resistivity (+25%) compared to S1.

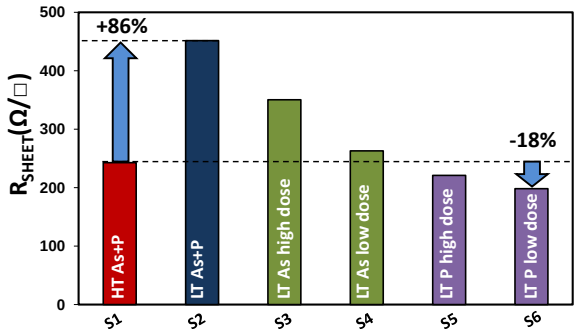



**Figure 1.8: Sheet resistance measurements for samples described in Table 1.1.**

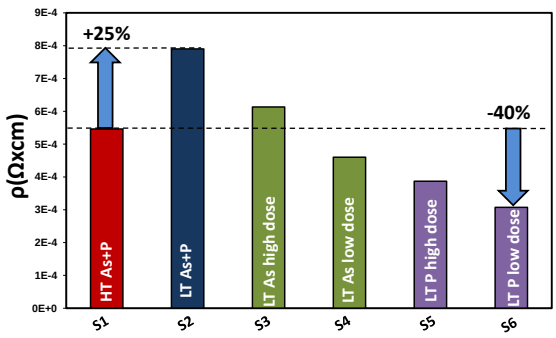



**Figure 1.9: Resistivity values for samples described in Table 1.1.**

In order to understand the resistivity trend shown in Figure 1.9, Hall effect measurements results will be presented in the next section. This experimental procedure allows quantifying the active carriers dose and mobility. In the next section, the measured active dose will be compared with the total implanted dose for arsenic and phosphorus.

### 1.2.2 Determination of the optimum P and As concentration for LT SPER activation

The comparison between active dose obtained by Hall effect measurements and chemical dose extracted by KMC simulations shown in Figure 1.10 for arsenic implanted samples, enables to estimate the fraction of active dopants. In this figure, the dashed lines correspond to the total dopant dose present in the amorphized region, obtained by integrating the chemical dopant profile from the silicon surface to the amorphous/crystalline interface. The dopant profiles of arsenic samples are reported in Figure 1.11. The points of Figure 1.10 correspond to electron mobility and active dose values extracted by the Hall measurements. The arrow indicating the distance between the measured active dose and the total implanted dose, represents a phenomenon of clustering, i.e., the formation of inactive agglomeration that makes the dopants electrically inactive.

For the arsenic high dose sample (S3), the activated dopants fraction in the amorphized region corresponds to 35% of the total implanted dose ($As_{TOT,Dose}$). It is worth noticing that $As_{TOT,Dose}$ for S3 obtained by this method is different from the value reported in Table 1.1 since a part of the implanted dose is trapped into the oxide present on the sample surface (as reported in Figure 1.7). Decreasing the implanted dose like in the case of S4, the activated dose fraction is estimated to be 96%. This value suggests that almost the total amount of arsenic implanted in the film has been efficiently activated by SPER. Thus, an optimal arsenic concentration that allows to full dopant activation can be extrapolated. Such value is found to be equal to $8x10^{20}$ at/cm$^3$. This concentration can be defined as

clustering limit since for higher dopant concentrations, the implanted atoms start to form inactive aggregates, also named clusters. As evidenced by the active concentration measured on sample S3 (Figure 1.10), for concentrations well above the clustering limit, an overall reduction of the activation level appears. For arsenic, the most stable cluster form reported in literature [Skarlatos 07], [Pinacho 05] are the $As_2V$, $As_3V$, $As_4V$ i.e. aggregates of two, three or four atoms of arsenic and one vacancy. In general, for concentrations higher than the clustering limit, arsenic has the tendency to aggregate with vacancies.

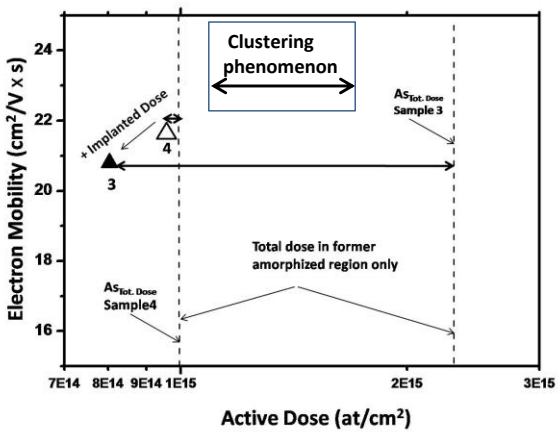



**Figure 1.10: Dose and mobility measurements results for As samples. Total dose is reported as well for comparison.**

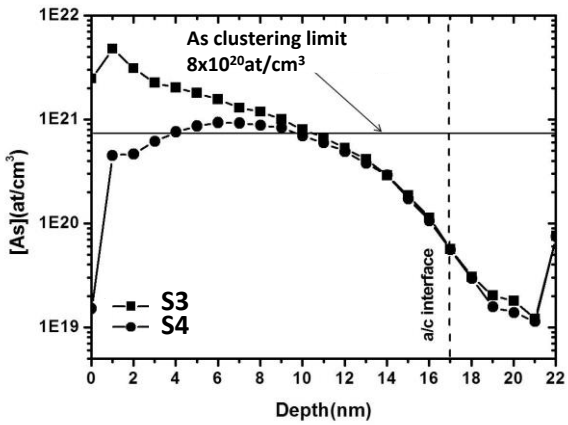
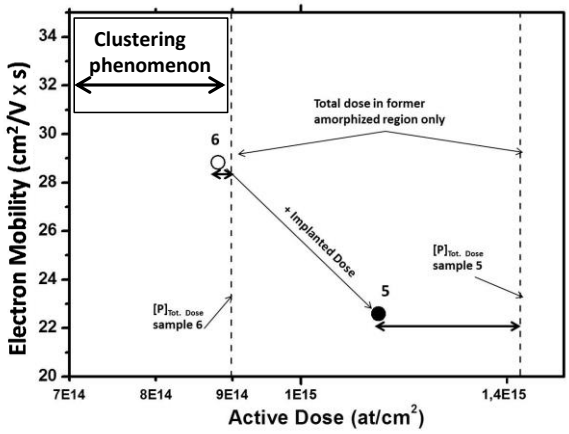



**Figure 1.11: Arsenic profiles after 2 minutes at 600°C annealing extracted by KMC simulation. Amorphous/crystalline (a/c) interface position is also reported.**

Similar analysis is now performed for phosphorus. Phosphorus mobility versus carrier active dose measurements are displayed in Figure 1.12. The total dopant dose present in the amorphized region calculated integrating the dopant profiles illustrated in Figure 1.13 is reported as well. For the high dose phosphorus sample (S5), 80% of the total implanted dose in the amorphized region has been activated. Once again, this means that the activation is limited by dopant clustering. Decreasing the phosphorus implantation dose (S6) results in an almost complete activation (98%). Using KMC profiles presented in Figure 1.13, the clustering concentration limit is estimated around $6x10^{20}$ at/cm$^3$.

Figure 1.12 shows that increasing the dose from quasi-ideal concentration (S6) to above clustering limit (S5) results in a dramatic mobility reduction. This affects directly the resistivity value (Figure 1.9), where $\rho_{S5} > \rho_{S6}$. However, while the clustering concentration limit is already reached for low dose sample (S6), a slightly higher activation is still observed for the higher dose (S5). In fact, the active dose increases from S6 to S5. This increase is explained by the fact that the amorphized depth in the S5 sample is thicker and that the concentration in this region is well below $6x10^{20}$ at/cm$^3$ (see Figure 1.13). This deeper region of dopants with concentration below the clustering limit allows sample S5 to have an overall active dose higher than S6.



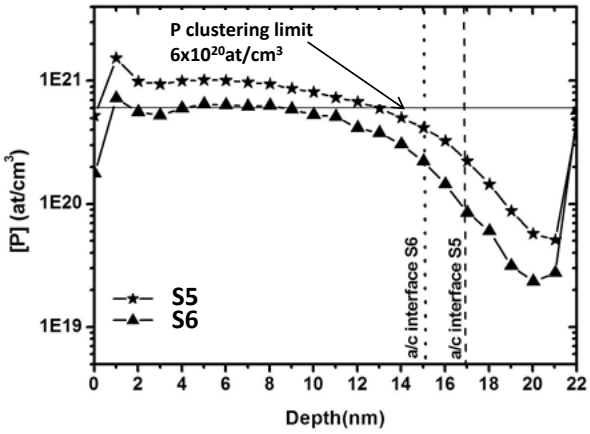




**Figure 1.12: Hall Mobility measurements results for P samples. Total dose is reported as well for comparison.**

**Figure 1.13: Phosphorus profiles after 2 minutes at 600°C annealing extracted by KMC simulation. Amorphous/crystalline (a/c) interface position is also reported.**

Even though clustering limit for arsenic ($8x10^{20}$ at/cm$^3$) is higher than for phosphorus ($6x10^{20}$ at/cm$^3$), better resistivity is shown for P implanted S6 (Figure 1.9). This can be explained by the mobility concentration curve at thermodynamic equilibrium [Masetti 84], where electron mobility for phosphorus is higher than for arsenic (see Figure 1.14). In addition, phosphorus is interesting for another aspect: since it has a smaller atomic mass compared to arsenic, it is possible to place a higher dose close to the BOX in a FDSOI access without full amorphization. This allows tuning a quasi-constant profile along the junction depth at concentration values close to the clustering limit extracted above.

In Figure 1.14, it is also evidenced that the low dose As (S4) and P (S6) samples show an activation level very close from the thermodynamic equilibrium at 1050 °C.

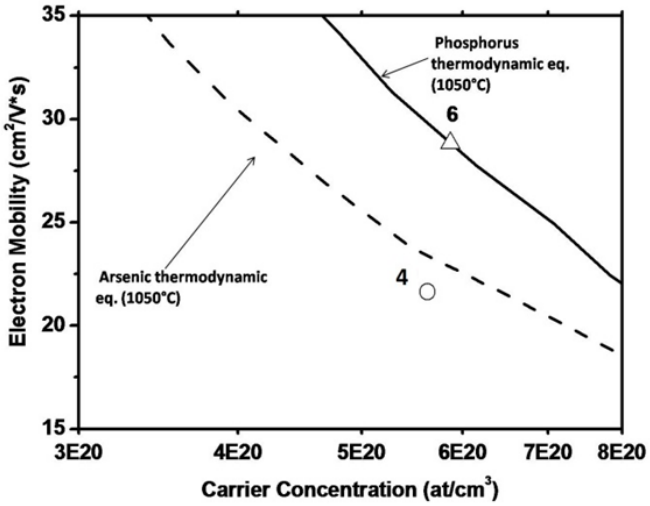



**Figure 1.14: Comparison between the electron mobility versus carrier concentration curves at 1050°C thermodynamic equilibrium [Masetti 84] and the experimental points at low dopant dose (S4 and S6). Carrier concentration of the experimental points is estimated using the measured active dose divided by the former amorphized region thickness.**

### 1.2.3 Dopant deactivation

Dopant activation by SPER drives the system to non-equilibrium state, so the application of a post annealing could lead to dopant deactivation phenomenon. Dopant deactivation arises from the high interstitial concentration left below the amorphous/crystalline interface after the implantation step. During subsequent thermal processing, these interstitials tend to interact to form bigger and more stable defects, the so–called end of range (EOR). They first form small interstitial clusters and further evolve towards {311} defects and dislocation loops. The presence of these defects generally has detrimental consequences for the device. During the activation process, EOR defects release interstitials that can interact with dopants in substitutional positions and cause deactivation. Similarly, vacancies can interact with active atoms and form electrically inactive clusters. Several study of deactivation phenomena are reported in literature especially for boron doping [Pawlak 04]

A post anneal of 30 minutes at 550 °C has been applied and the sheet resistance evolution of S1, S4 and S6 evaluated. However, in real device, the standard post activation anneal thermal budget, which is around 30 minutes at 400 °C, should provide even more stable activation. The aim of this section is to evaluate the evolution of sheet resistance values after post annealing for samples activated at high temperature and low temperature.

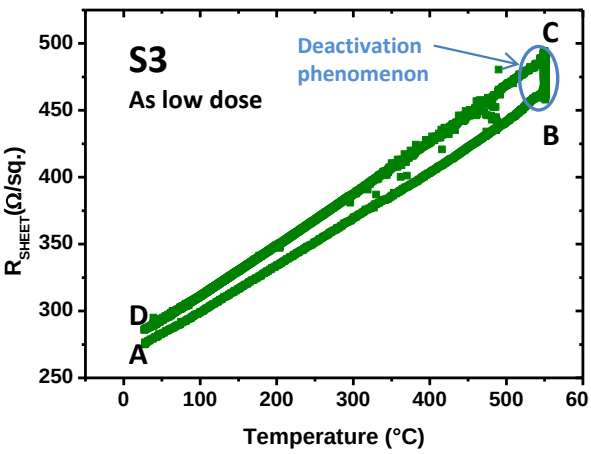



**Figure 1.15: Sheet resistance – temperature curve for the *in-situ* experimental test of post annealing on S3.**

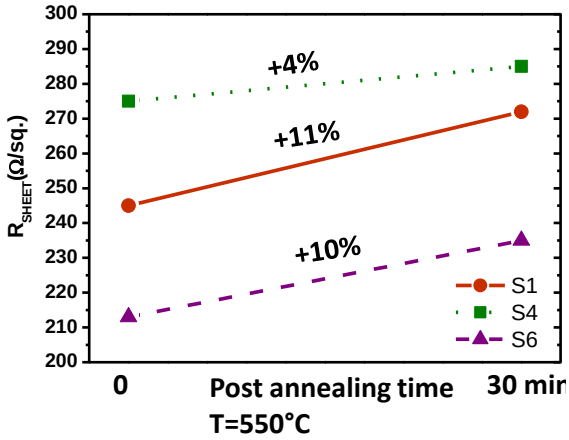



**Figure 1.16: Sheet resistance percentage variation after post annealing of 30 minutes at 550°C.**

Sheet resistance measurements have been performed during the anneal. As an example, the complete post-annealing curve of sheet resistance as a function of the applied annealing temperature is shown for S3 in Figure 1.15. The point A corresponds to the sample just after dopant activation by SPER. A temperature ramp of 100 °C/min is then applied and the sheet resistance value increase, following the linear law $R=R_0(1+\alpha T)$, up to point B. Then the sample is maintained for 30 minutes at constant temperature of 550 °C. Sheet resistance increases until it reaches point C. The dopant deactivation phenomenon mainly occurs during this phase. Finally, the temperature is moved down to 25 °C reaching the point D. The sheet resistance variation between the point A and the point D represents

the effect of the dopant deactivation phenomenon. Same *in-situ* $R_{sheet}$ measures are performed for samples S1, S4 and S6 and the final sheet resistance variation between points A and D is represented in Figure 1.16.

The smallest sheet resistance degradation (+4%) after post annealing is found for arsenic in S3. According to the present results, it appears that arsenic is the most stable dopant for a post annealing at 550°C. Similar $R_{sheet}$ degradation is observed for S1 (+11%) and S6 (+10%) samples. This means that similar sensitivity to post annealing is found for the best split at low temperature (S6) in comparison to the best split at high temperature (S1). Moreover, the values of 230 Ω/□ after post annealing reached by S6 is still comparable with the initial value of S1 (245 Ω/□), that is the target for low temperature activation.

### 1.2.4 Conclusion for $R_{SHEET}$ optimization for SPER activation at low temperature

In this section are summarized the challenges for the sheet resistance optimization in the case of low temperature activation by SPER.

**Seed preservation:** SPER activation is efficient only in the pre-amorphized and recrystallized areas. Outside this region, the activation level will be close to the solubility limit values reported in Figure 1.4. However, the preservation of a crystalline seed (with a thickness around 3 nm) is mandatory to obtain the access recrystallization during the SPER anneal. This quasi non-activated zone (3 nm) is a penalty in the sheet resistance value in the case of 22 nm thick raised source and drain (RSD). The situation is schematically represented in Figure 1.17a.

**Clustering phenomenon:** Above a certain dopants concentration at a given temperature, the activation limit is reached and part of the dopants within the recrystallized region forms inactive clusters (striped region in Figure 1.17b). To avoid this phenomenon, the ideal shape of the implanted profile has to be constant and below this clustering limit. Clustering limit has been estimated for arsenic at $8x10^{20}$ at/cm$^3$ and for phosphorus at $6x10^{20}$ at/cm$^3$, for an activation SPER process carried out at 600 °C.

**Deactivation:** Since SPER is a non-equilibrium mechanism, it leads to metastable activation. This means that subsequent anneals (e.g. back end thermal budgets) might affect the junction activation level after full circuit processing. Nevertheless, an acceptable sheet resistance degradation has been found for samples activated by SPER even with a thermal budget of 550 °C for 30 minutes.

**Reaching a constant concentration profile and a high dopant concentration close to the buried oxide is particularly complex for low temperature FDSOI devices:** The limited thickness of the silicon film, the negligible dopants diffusion at 600 °C and the relatively high mass of n-type dopants (P, As) leads to additional complexity. It is therefore problematic to obtain high dopant concentration close to the buried oxide (BOX) without amorphizing the full access. Kinetic Monte Carlo (KMC) simulations show that the maximal concentrations allowed to preserve a crystalline seed are [P]~$1\times10^{20}$ at/cm$^3$ and [As]~$5\times10^{19}$ at/cm$^3$. This issue is not observed on FDSOI devices fabricated at high temperature, where the 1050°C spike anneal enables dopants to diffuse and reach more ideal profile. Phosphorus is then preferable than arsenic since higher dopant concentration can be placed very close to the BOX interface without full amorphization of the film. The ideal configuration is schematically represented in Figure 1.17c.

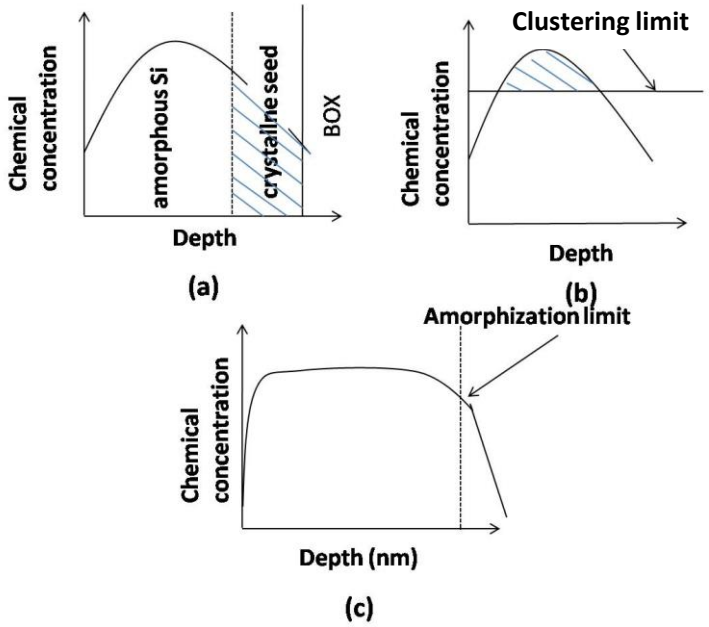



**Figure 1.17: SPER optimization challenges. (a) Seed control; (b) clustering phenomenon; (c) constant profile tuning. Striped areas indicate inactive dopant regions.**

### 1.2.5 Optimization of boron activation by SPER

In this section, similar analysis proposed for arsenic and phosphorus is carried out for boron. This dopant has been extensively studied in literature by several authors [Duffy 06], [Cristiano 13] and therefore no in-depth analysis is needed. This section aims at finding the optimum implant conditions in FDSOI accesses activated at low temperature.

Three samples have been analysed using the doping conditions reported in table 1.2.

| Sample | S7 | S8 | S9 |
|---|---|---|---|
| Annealing | HT | LT | LT |
| Dopant | $BF_2$+B | B | B |
| Dose ($x10^{15}$ at/cm$^2$) | 5.8 | 5.8 | 3 |
| $t_{seed}$ layer (nm) | 2.5$^{(*)}$ | 2.5 | 2.5 |

**Table 1.2: Samples description with type of annealing, dopants implanted doses and crystalline seed thickness. $^{(*)}$ High temperature activation is not limited to the amorphized region.**

Sample 7 (S7) has been implanted with the doping condition used in the process of reference and it has been annealed by spike at 1050 °C. In sample 8 (S8), same total dose has been implanted, but using only boron instead of the combination $BF_2$ and boron. This choice rises from the fact that fluorine is detrimental for the re-crystallization by SPER as reported in [Olson 88] since it slows down the SPER rate. In sample 9 (S9) boron dose is reduced. For S8 and S9 the dopants activation has been performed by SPER at 600°C for 2 minutes. As discussed in paragraph 1.1.1, boron implantation is not able to

create a density of defects such to create an amorphous region, so a pre-amorphization step is needed. Germanium implantation has been performed in order to create an amorphous region of 20 nm, according to the simulation prediction. Sheet resistance values for the three samples of Table 2.1 are reported in Figure 1.18. As for n-type case, it is evidenced that in order to optimize the sheet resistance value obtained by SPER at low temperature, the total doping dose has to be reduced compared to the conditions of the process of reference. Reducing the total dose, as reported in the doping profiles of Figure 1.19, the sheet resistance value goes from 399 Ω/□ (S8) down to 340 Ω/□ (S9), approaching the target value of 301 Ω/□ of the sample activated at high temperature (S7).

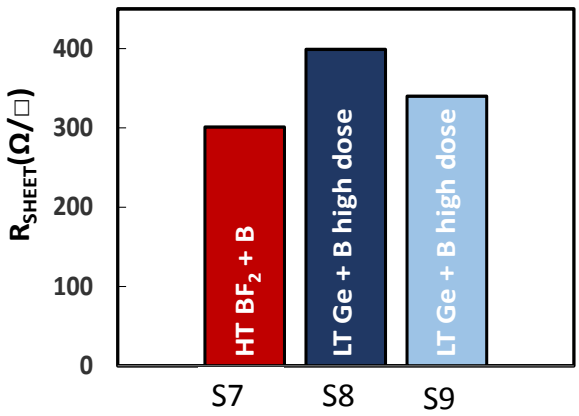



**Figure 1.18: Sheet resistance values measured on samples reported in Table 1.2 for p-type doping.**

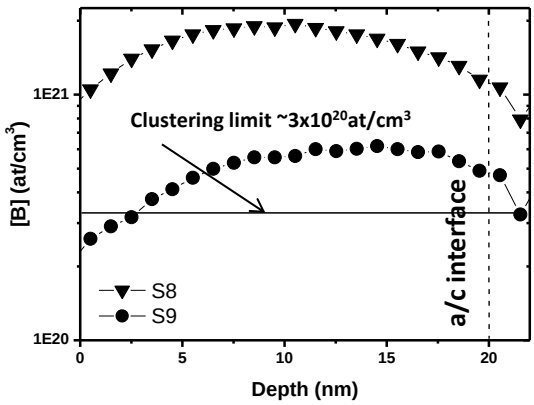



**Figure 1.19: Boron profiles after 2 minutes at 600°C annealing extracted by KMC simulation. Amorphous/crystalline (a/c) interface position is also reported.**

This confirms the results found on n-type doping: for low temperature activation by SPER, if the dopant concentration overcome a certain value, defined as the clustering limit, a sheet resistance degradation appears. For boron, clustering limit is reported to be around $3x10^{20}$ at/cm$^3$ from several authors [Cristiano 13], [Duffy 06]. The doping conditions optimization follows the criteria reported in section 1.2.4.

Concerning boron deactivation phenomenon after post-annealing, the reader can refer to detailed study reported in [Xu 12].

## 1.3 SPER rate optimization

SPER process is a thermally activated process and is well described by an Arrhenius-type expression:

$$v = v_0 exp(\frac{-E_a}{KT}) \tag{1.6}$$

where v is the SPER growth velocity (also named SPER rate), $E_a$ is the activation energy, k is the Boltzmann's constant and T is the annealing temperature. For intrinsic silicon, considering a re-crystallization of the (100) surface, according to several data in literature [Csepregi 78], [Olson 88], [Johnson 07], values of the pre-factor and the activation energy are found: $v_0$=0.46 nm/s; $E_a$=2.7 eV.

SPER rate is strongly dependent on different conditions and parameters:

- Substrate orientation: (110) and (111) surfaces recrystallize at a slower rate than (100) silicon [Csepregi 76].
- Strain conditions: uniaxial compressive strain is found to slow down the regrowth velocity while tensile strain does not impact the crystallization rate [Rudawski 08].
- Presence of impurities: dopants such as boron, aluminum, phosphorus and arsenic can enhance recrystallization rates [Johnson 07]. However, high dopant concentrations [Olson 88] and presence of non-dopant impurities such as fluorine, carbon, oxygen and nitrogen can retard recrystallization rate [Narayan 82].

In this work, the re-crystallization will be considered on (100) surface, without strain contribution and will be focused on the effect of the presence of impurities on SPER rate.

### 1.3.1 Optimal dopant concentration for SPER rate

At our knowledge, no works in literature study the effect of the dopants impurities on the crystallization velocity for the doping concentration and the temperature in the range of interest for this work. In particular, [Olson 88] studied a wide range of dopant concentration, but for annealing temperatures above 600 °C. The aim of this work is to reduce the temperature of dopant activation down to 450 °C and SPER rate behavior for temperature below 600 °C has to be explored. [Johnson 07] proposed a study on the impact of dopant impurities for a wide temperature range, but for a maximum dopant concentration of ~$1x10^{20}$ at/cm$^3$, which is too low for the optimization of the sheet resistance value corresponding to the zone of source and drain of a transistor device. In sections 1.2.2 and 1.2.5, it has been shown that the optimum dopant concentration is around $6x10^{20}$ at/cm$^3$ for phosphorus and $3x10^{20}$ at/cm$^3$ for boron. A complementary study of the SPER rate dependence with both high dopant concentration and low annealing temperature is needed.

To determine the optimal dopant concentration capable to enhance the recrystallization rate at low temperatures, full sheet 200 mm silicon bulk wafers were pre-amorphized with silicon implantations to form amorphous layer of approximately 200 nm. No specific cleaning has been made, thus a native oxide is present at the surface during the implantation. In such thick amorphous layer, the re-crystallization takes place in a permanent regime, i.e. the SPER rate is less influenced by the proximity with the sample surface, being mainly influenced by the concentration of dopants. Moreover, the SPER rate is not influenced by the early stages of the re-crystallization when it strongly dependent on the amorphous/crystalline interface roughness [El Farhane 05]. The pre-amorphized layers were implanted with phosphorus and boron ions along the entire thickness of the amorphous layer, with total concentrations up to $1.3x10^{21}$ at/cm$^3$. The dopant profiles obtained by KMC simulation are reported in Figure 1.20 and 1.21 for boron and phosphorus respectively.

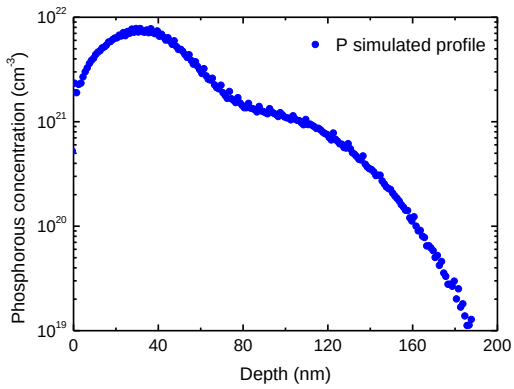



**Figure 1.20: Phosphorus concentration profile obtained by KMC simulations.**

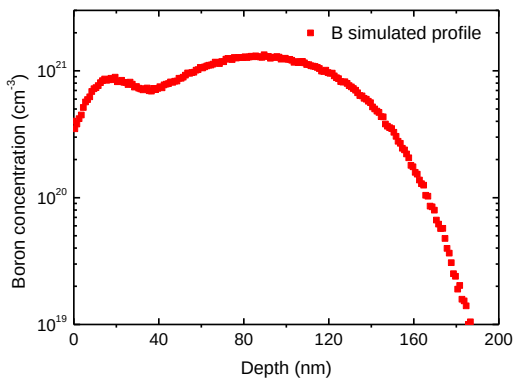



**Figure 1.21: Boron concentration profile obtained by KMC simulations.**

To follow in real time the recrystallization process and to obtain SPER rate values, phosphorus and boron as-implanted samples were analyzed by spectroscopic ellipsometry in an in-situ mode, i.e. the measures were made during the recrystallization annealing at different temperatures.

The in-situ experiment was performed using a heat cell mounted on an ellipsometer which acquires spectra from the ultraviolet to near infrared regions (193-1700 nm). The angle of incidence was set to 70°. The ellipsometric acquisition time was less than 2 seconds enabling to detect relatively fast phenomenon. The maximum ramping speed of 50 °C per minute was used to rapidly reach the targeted temperatures. The ellipsometric spectra were therefore analyzed as a function of time to extract the remaining amorphous thickness.

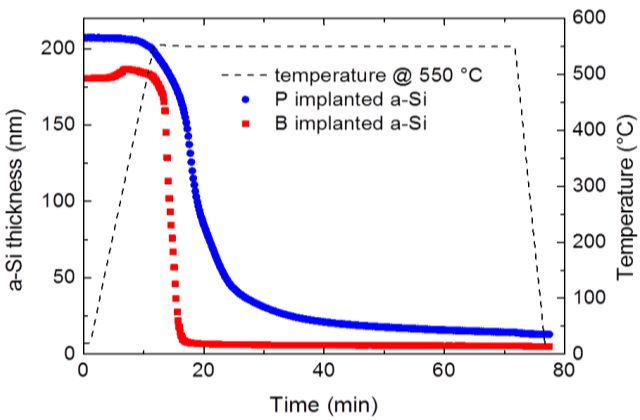



**Figure 1.22: Experimental results of the in-situ ellipsometry annealing showing the evolution of the amorphous silicon thickness as a function of annealing time for a 550 °C anneal.**

Using this in-situ ellipsometry technique, P and B as-implanted samples were annealed at temperatures between 450 °C and 600 °C while the annealing time was adapted for each sample in order to have a complete re-crystallization of the amorphous layer. As an example, the results

obtained after a 550 °C annealing are presented in Figure 1.22, where the evolution of the amorphous silicon thickness is plotted as a function of the annealing time and temperature for both phosphorus and boron implanted samples. After 60 minutes of annealing the amorphous layers were already completely recrystallized, but each dopant specie with a different SPER velocity as indicated by the curve slope.

Every point of measurement identifies a position of the amorphous/crystalline interface. Extracting the derivative of the amorphous/crystalline it is possible to extract the SPER rate for different depths of the sample. Since the concentration profile is known from Figure 1.20 and Figure 1.21, it is possible to plot the SPER rate for different doping concentration. The experiments have been repeated for three different annealing temperature and the SPER rate dependence with the doping concentration is plotted in Figure 1.23 and 1.24 for phosphorus and boron respectively.

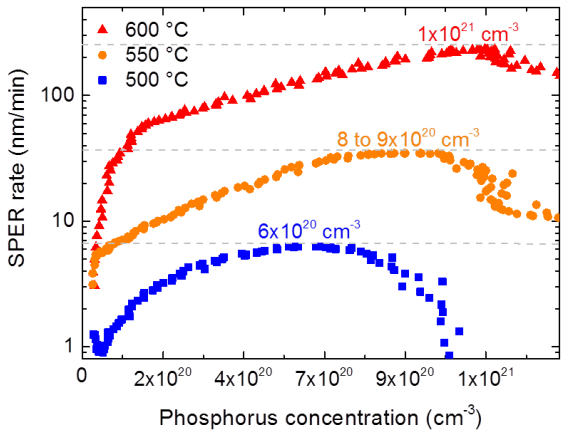



**Figure 1.23: Experimental SPER rates obtained from in-situ ellipsometry annealings performed at temperatures from 450 °C to 600 °C, as a function of the simulated phosphorus concentrations.**

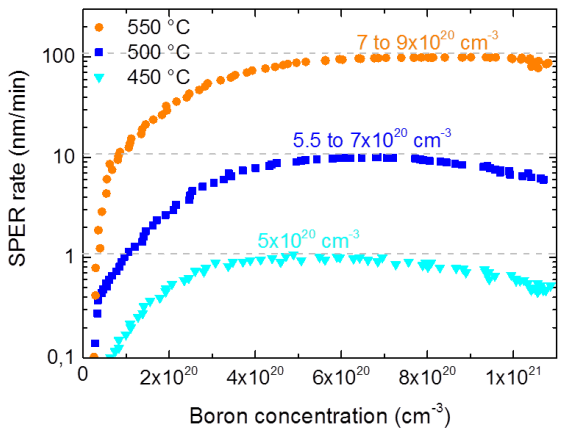



**Figure 1.24: Experimental SPER rates obtained from in-situ ellipsometry annealings performed at temperatures from 450 °C to 600 °C, as a function of the simulated boron concentrations.**

Generally, as the annealing temperature increases, the maximal value of SPER rate is higher and is reached for a slightly higher dopant concentration values. For example, at 500 °C the optimal phosphorus concentration leading to the 6 nm/min maximal SPER rate was about $6x10^{20}$ at/cm$^3$, while at 550 °C the 35 nm/min maximal SPER rate took place for a P concentration of about $8\text{-}9x10^{20}$ at/cm$^3$. As the dopant concentration continues to increase beyond those optimal values, the SPER rate diminishes and can eventually completely stop. Similarly, for B implanted samples, the SPER rate increases until it reaches a maximal value for each annealing temperature. At 500 °C, the optimal B concentration leading to the maximal 10 nm/min SPER rate is about $5.5\text{-}7x10^{20}$ at/cm$^3$, while at 550 °C a 100 nm/min maximal SPER rate is attained for a B concentration of about $7\text{-}9x10^{20}$ at/cm$^3$. As the B concentration augments, the SPER rate diminishes. As expected, all these recrystallization velocities are much higher than the ones obtained for the intrinsic silicon where, for example, at 500 °C the SPER rate is about 0.6 nm/min [Johnson 07].

A summary of the experimental results concerning the dependence of the optimal P and B dopant concentrations extracted at the maximal SPER rate for different annealing temperatures is reported in Figure 1.25. The dashed lines are a linear fit extrapolation of the experimental points and are not based on a model because we are not yet capable to explain the physical phenomenon responsible for it. Nevertheless, in practical terms, this linear approximation is useful to estimate the optimal P and B dopant concentration to enhance the SPER rate at different temperatures.

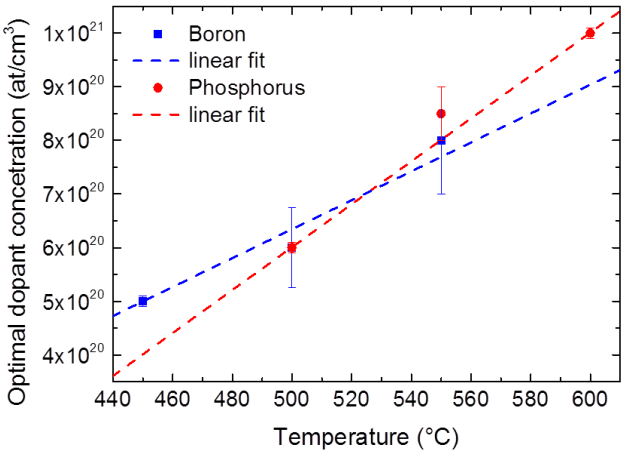



**Figure 1.25: Optimal boron and phosphorus concentrations to enhance the SPER rate as a function of the annealing temperature. The dashed lines are a simple linear fit of the experimental points.**

### 1.3.2 Limits of the analysis and open questions

The dopant concentrations leading to the best SPER rate for phosphorus and boron at different temperatures have been extracted using the simulated dopant profile.

Secondary ion mass spectrometry (SIMS) analysis have been performed on the samples annealed at 500 °C, in order to obtain the experimental profiles of phosphorus and boron. The experimental profiles are reported in Figure 1.26 and 1.27 for phosphorus and boron respectively in comparison with the simulated profiles. For the two dopants, good agreement between simulated and experimental profile is found in the first 100 nm starting from the surface. However, significant difference is found in the last 100 nm, corresponding to the beginning of the re-crystallized layer by SPER. This difference, impacts significantly the extraction of the SPER rate as a function of the doping concentration and the extraction of the optimum dopant concentration.

In phosphorus SIMS profile shown in Figure 1.26 a dopant peak segregation at 110 nm depth is observed. This corresponds to the position where the amorphous interface has stopped. This phenomenon is often referred in literature as snowplow, i.e. a dopant segregation at amorphous/crystalline interface during the re-crystallization. This phenomenon is not predicted by KMC simulation and different dopant repartition is then found in the amorphous and re-crystallized zone between the simulated and the experimental profile. At this stage it is not possible to conclude on the real profile for each temperature due to the too important numbers of SIMS profiles needed

due to the snowplow effect. The discontinuity at the remaining amorphous/crystalline interface could have influenced the interpretation of the spectroscopy signal and therefore the extraction of the experimental profile.

Boron SIMS and experimental profiles shown in Figure 1.27 present significant difference. In this case the re-crystallization was complete and no discontinuity between an amorphous and crystalline region was found. Furthermore, boron is not known to lead to snow plow during This difference will significantly influence the SPER rate extraction as a function of the concentration (in the half decade range for the concentration position)

At this stage, general answer cannot be provided on the dopant concentration for the SPER rate optimization at different temperatures. To do so, it would be necessary to go to in depth analysis of physical phenomena of the kinetic of re-crystallization during SPER, such as snowplow and dopants diffusion in the amorphous region. However, this is a fundamental material study far from the purposes of this thesis, which deals with optimization of electrical devices. The numerous data collected might be interesting for further study in order to better understand the SPER mechanisms in the presence of dopants.

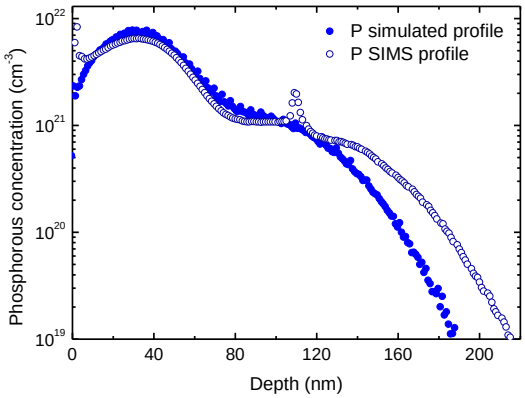



**Figure 1.26: Comparison between SIMS and simulation profile for phosphorus sample.**

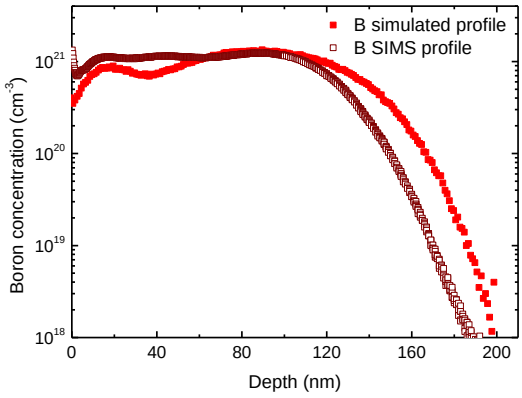



**Figure 1.27: Comparison between SIMS and simulation profile for boron sample.**

## 1.4 Temperature reduction for dopant activation down to 450°C

In section 1.2, it has been discussed how to define the dopant implantation conditions to optimize the activation at 600°C. In section 1.3, the dopant concentration that optimizes the crystallization speed for different annealing temperatures and dopant species has been found. The goal of this section is to reduce the annealing temperature of dopant activation down to 450°C, without degrading the sheet resistance value found for activation at 600°C. The reduction of the anneal temperature for dopant activation is crucial for the top level of the 3D sequential integration process flow.

Samples described in Figure 1.5 were used for different dopant implantation conditions and anneals temperature. For n-type doping, phosphorus ions were implanted inducing an amorphization of 17 nm of the top crystalline silicon film. For p-type doping, a pre-amorphization step using germanium implantation was made prior to boron implantation, leading to the formation of a 17 nm thick

amorphous silicon layer. The implantation conditions have been chosen in order to ontain a maximum concentration of $5x10^{20}$ at/cm$^3$ distributed throughout the amorphous region. To mimic source-drain implantation in real devices, P and Ge+B implantations were performed on SOI substrates with a $SiO_2$ native layer on top. However, the presence of this native oxide could influence the amorphization and recrystallization behavior of the crystalline silicon due to the recoil of oxygen during the implantation. Contrary to doping impurities that are known to enhance recrystallization velocity [Johnson 07], oxygen non-doping impurity could reduce the SPER rate [Kennedy 77], [Narayan 82]. To study the impact of this phenomenon on low temperature doping process of thin films, same P and Ge+B implantations were made on SOI wafers cleaned with hydrofluoric acid (HF) last step to remove the native oxide layer right before implantations. The wafers without native silicon oxide, are referred to w/o/$SiO_2$ while the ones with the native superficial oxide will be the w/$SiO_2$.

To evaluate the SPER process, w/o/$SiO_2$ and w/$SiO_2$ P and Ge+B as-implanted wafers were furnace annealed at different thermal budgets to promote the recrystallization of the 17 nm amorphous silicon layer: 600 °C for 2 min, 500 °C for 8 min and 450 °C for 60 min in $N_2$ atmosphere. The morphology of the as-implanted and annealed samples was characterized by cross-section transmission electron microscopy (TEM). Sheet resistance was measured using a four-point probe method. Recrystallization rates for all implanted samples were obtained by in-situ ellipsometry performed at different temperatures. The ellipsometric spectra were analyzed as a function of time to extract the a-Si thickness.

### 1.4.1 Sheet resistance results

The TEM image of the w/$SiO_2$ phosphorus-implanted wafer is presented in Figure 1.28, superimposed to the simulated concentration-depth profile of the implanted P ions. Simulations were made with the Sentaurus Process tool using the KMC method. As shown by the TEM picture, this implantation resulted in the formation of a 17 nm thick of amorphous silicon layer, leaving a crystalline silicon seed of approximately 4 nm that will be the seed for the recrystallization. A $SiO_2$ native layer of around 2 nm was also observed.

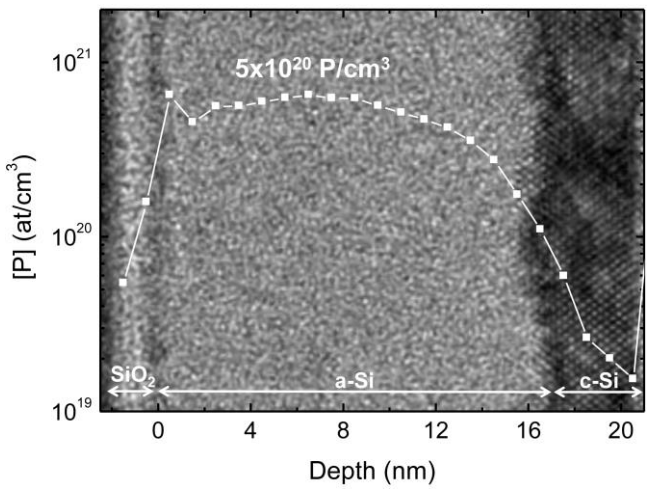


**Figure 1.28: Simulated concentration-depth profile of the as-implanted P ions superimposed to the TEM image of the w/$SiO_2$ sample. This implantation resulted in a ~17 nm thick amorphous silicon layer with by ~2 nm of native $SiO_2$, and 4 nm of crystalline seed.**

All as-implanted P and Ge+B samples were annealed at different thermal budgets and sheet resistance results are presented in Figure 1.29 and 1.30 respectively. The average sheet resistance values are plotted as columns graphs while the minimum and maximum values are represented by the vertical lines. Since this experimental measurement is really reliable, several points of measurement have been repeated on different spots over the sample. The variability corresponds to the thickness variability of the amorphized zone due to the a/c interface roughness (approximately 2 nm).

For the P samples (Figure 1.29) implanted without the native oxide (w/o/$SiO_2$), a constant $R_{SHEET}$ of ~200 Ω/□ was obtained for the three different thermal budgets. This result is really promising for the reduction of the thermal budget for dopant activation since, this sheet resistance value obtained by 450°C annealing clearly outperforms the one obtained with the process of reference (248 Ω/□) using spike annealing.

For the samples where P ions were implanted through the native oxide (w/$SiO_2$), an increase in $R_{SHEET}$ from 210 Ω/□ up to 270 Ω/□ was observed when the SPER annealing temperature was reduced from 600 °C down to 450 °C. Similar tendency was observed for the B samples (Figure 1.30 ).

For the substrates where the Ge+B implantations were performed without native oxide (w/o/$SiO_2$), $R_{SHEET}$ values remained constant at 330 Ω/□ for 500 °C and 600 °C anneals. However, an increase in $R_{SHEET}$ up to 370 Ω/□ was observed for the sample annealed at 450 °C. It is believed that this augmentation is a real effect and does not arise from measurement uncertainties. However, the reason for this is not yet clarified. For the case where the implantations were made through the $SiO_2$ native layer (w/$SiO_2$), sheet resistance degradation from 330 Ω/□ to 450 Ω/□ occurred as the SPER annealing temperature was reduced from 600 °C down to 450 °C. These results show that if the implantation is made without the presence of native oxide, the sheet resistance values obtained are independent of the annealing temperature.

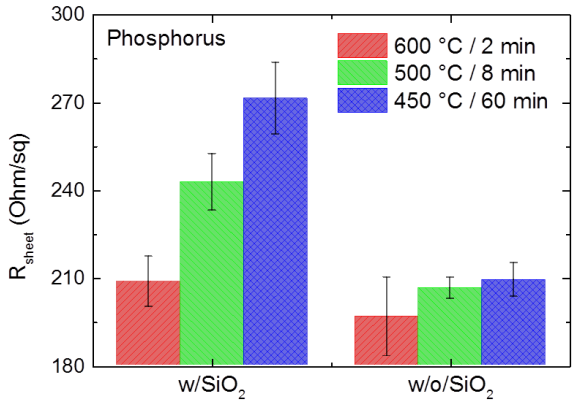



**Figure 1.29: Average sheet resistance values for both w/$SiO_2$ and w/o/$SiO_2$ phosphorus samples annealed at different thermal budgets.**

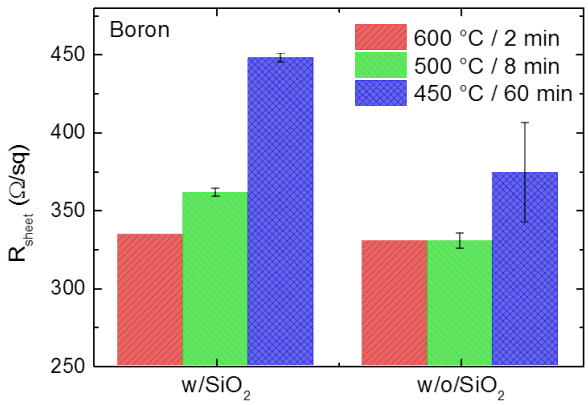



**Figure 1.30: Average sheet resistance values for both w/$SiO_2$ and w/o/$SiO_2$ boron samples annealed at different thermal budgets.**

The sheet resistance depends on the concentration-depth profile of active dopants C(x), the carrier mobility μ(x) and the junction depth xj, as expressed in equation (1.7):

$$R_{sheet} = \frac{1}{\int_0^{x_j} \mu(x)C(x)dx} \tag{1.7}$$

### 1.4.2 Impact of the presence of oxygen by recoil

As in the previous sections, $x_j$ is assumed to be the thickness of the recrystallized amorphous silicon film after SPER, i.e. the film thickness that contains active dopants. Concerning carriers mobility, these results indicate that the presence of a superficial $SiO_2$ layer does not cause mobility degradation since SPER annealing at 600 °C resulted in the same $R_{SHEET}$ value for both sets of samples (with or without native $SiO_2$). Thus, according to this equation, the two parameters that contribute to the $R_{SHEET}$ degradation observed for the w/$SiO_2$ phosphorus and boron samples are either: a reduction on the C(x) that is associated with a decrease in the dopant activation level; or a reduction of $x_j$ that corresponds to an incomplete recrystallization of the amorphous silicon layer. As dopant diffusion is negligible at these low temperatures, i.e. temperature below 600 °C, the concentration-depth profile of active dopants is not expected to change after activation anneals, hence being the same for all samples. Thus, our hypothesis is that the sheet resistance degradation observed for the w/$SiO_2$ samples is a consequence of an incomplete recrystallization of the amorphous layer during the SPER anneals at temperatures below 600 °C.

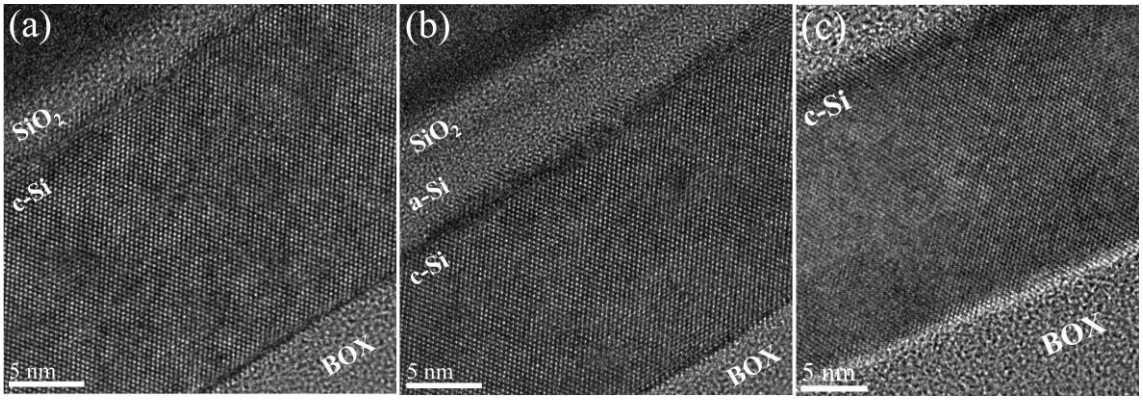



**Figure 1.31: Cross-section HRTEM images of samples annealed at 450 °C for 60 min. (a) The w/o/$SiO_2$ P sample had a ~21 nm crystalline Si layer with ~2 nm of native oxide. (b) The w/$SiO_2$ P sample had ~18 nm of crystalline silicon and ~3 nm of a non-recrystallized amorphous layer, with ~2 nm of native oxide. (c) The w/o/$SiO_2$ B sample had a crystalline Si layer of ~21 nm thick.**

To verify this assumption, both w/o/$SiO_2$ and w/$SiO_2$ P samples and w/o/$SiO_2$ B sample annealed at 450 °C were observed by TEM (Figure 1.31). For the samples where P implantation was made in w/o/$SiO_2$ wafers (Figure 1.31(a)), the amorphous layer was completely recrystallized after the annealing at 450 °C, resulting in a ~21 nm thick crystalline silicon layer with a 2 nm native oxide created at the surface after implantation. However, for the samples where the P implantation was performed through the native oxide, the 450 °C SPER annealing was not sufficient to completely recrystallize the amorphous layer. As observed in Figure 1.31(b), this w/$SiO_2$ sample has an ~18 nm thick crystalline layer and a residual 3 nm thick non-recrystallized amorphous silicon with approximately 2 nm of native oxide. For the samples where the Ge+B implantations were made in SOI wafers without oxide, the 450 °C annealing was enough to recrystallize the entire amorphous layer. A crystalline silicon layer of approximately 21 nm thick was obtained, as shown by the TEM image of this w/o/$SiO_2$ sample presented in Figure 1.31(c).

To investigate in real time the recrystallization of the amorphous layer, in-situ ellipsometry measurements were performed in both P and Ge+B samples implanted with and without the superficial $SiO_2$. Figure 1.32 and 1.33 shows the evolution of the amorphous thickness as a function of the annealing time for the w/$SiO_2$ and w/o/$SiO_2$ variants thermally treated at 450 °C. As indicated by the curve slope in Figure 1.32, the w/o/$SiO_2$ P doped wafer presents a quasi-constant recrystallization velocity of 0.4 nm/min during all the SPER annealing. After 60 minutes, the initial amorphous layer was completely recrystallized. For the sample where P ions were implanted through the native oxide, the recrystallization starts with the same 0.4 nm/min rate. However, after 40 minutes of annealing, a clear reduction in the SPER rate took place and continues up to the end of the annealing, after 140 minutes. At this moment, the SPER rate was reduced by a factor 20 compared to the initial rate and the ellipsometry measurement indicates a 3 nm thick non-recrystallized amorphous residual layer. Same behavior was observed for the Ge+B implanted samples. For the substrate implanted without the native $SiO_2$ (w/o/$SiO_2$), the 450 °C annealing induced a quasi-constant recrystallization rate of 0.9 nm/min, as shown in Figure 1.33. For samples where implantations were performed through the $SiO_2$ layer (w/$SiO_2$), a diminution on the recrystallization velocity occurred from 0.74 nm/min down to 0.06 nm/min at the end of the annealing. The 3 nm residual amorphous layer measured by ellipsometry is in good agreement with the TEM image in Figure 1.31(b).

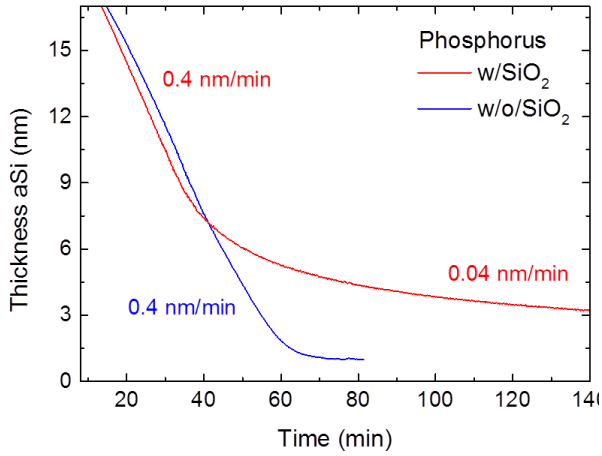



**Figure 1.32: In-situ ellipsometry 450 °C annealing of P implanted samples with (w/$SiO_2$) and without (w/o/$SiO_2$) the oxide layer. The amorphous silicon thickness is shown as a function of the annealing time.**

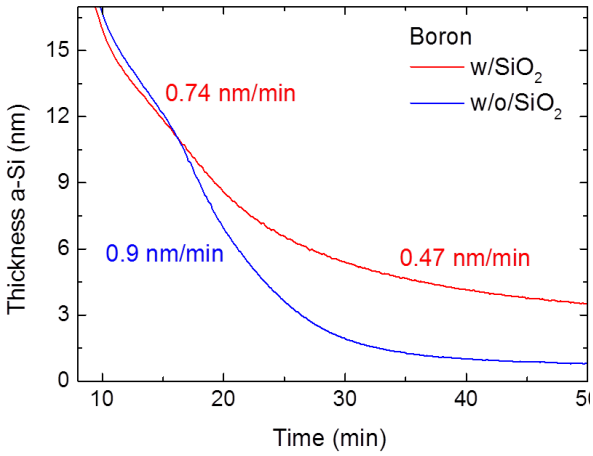



**Figure 1.33: In-situ ellipsometry 450 °C annealing of B implanted samples with (w/$SiO_2$) and without (w/o/$SiO_2$) the oxide layer.**

These results, i.e. incomplete recrystallization and reduction of the SPER rate, seem to be a consequence of oxygen atoms present in the silicon films. It is known that ion implantation through a superficial $SiO_2$ layer can insert oxygen atoms into the thin top silicon film by recoil implantation [Petkov 00], [Magee 81].

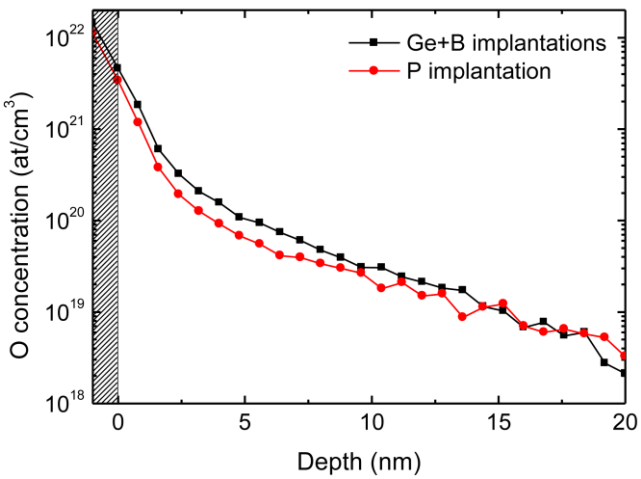



**Figure 1.34: Simulation of oxygen concentration inserted into the 22 nm Si top film by recoil due to the of Ge+B and P ion implantations. The shadowed region corresponds to the 1 nm thick $SiO_2$ that is assumed to be present on the sample surface.**

Figure 1.34 presents the results obtained by KMC simulation, where the recoiled oxygen concentration profiles resulting from Ge+B and P implantations are plotted as a function of depth. The oxygen

concentration in the first 5 nm of the amorphous layer are between $3x10^{21}$ and $6x10^{19}$ at/cm$^3$. These simulations were made considering the presence of 1 nm thick $SiO_2$ superficial layer (shadowed zone in the graph).

In the present study, a reduction of the SPER rate is observed in the last ~8 nm of the amorphous Si layer, as indicated by the ellipsometry results in Figure 1.32 and 1.33. As the amorphous/crystalline interface approaches the sample surface, it enters this oxygen-rich region causing a drastic reduction of the SPER rate. As the annealing elapsing time, the recrystallization was finally stopped and an amorphous silicon layer of about 3 nm remained as indicated by TEM (Fig. 3(b)) and ellipsometry (Figure 1.32 and 1.33) results.

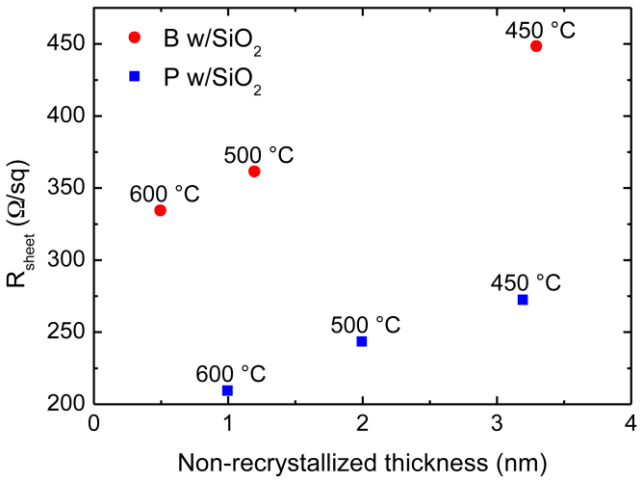



**Figure 1.35: Sheet resistance of B and P samples implanted with the $SiO_2$ superficial layer as a function of the non-recrystallized amorphous layer thickness measured by ellipsometry after SPER annealings at 600 °C, 500 °C and 450 °C.**

The consequence of this incomplete recrystallization is an increase in the sheet resistance of Si thin films activated by SPER at temperature below 600 °C, as presented in Figure 1.35. The reduction in SPER annealing temperature down to 500 °C and 450 °C resulted in thicker non-recrystallized amorphous layers, inducing an increase of 35% in the sheet resistance in comparison to the w/$SiO_2$ samples annealed at 600 °C, where the amorphous layer was almost entirely recrystallized.

Finally, these results sustain the hypothesis that the degradation of the sheet resistance is caused by the incomplete recrystallization of the amorphous layer that is probably a consequence of the insertion of oxygen atoms by recoil implantation. When the amorphous layer is completely recrystallized, the obtained sheet resistance values are comparable to the ones obtained with 1050 °C spike annealing.

The sheet resistance values of 200 Ω/□ for phosphorus obtained at 450 °C and 330 Ω/□ for boron at 500 °C are really promising for the 3D sequential integration process flow. The thermal budget reduction is crucial to conserve the performance and integrity of the bottom transistor level and the achievement of dopant activation below 500°C fully satisfies the thermal budget limitation even for the silicide stability that is considered the most critical parameter [Fenouillet 14] for bottom transistor level.

## 1.5 Conclusion of the chapter

In this chapter, basic principles of dopant activation by SPER have first been presented. Then, sheet resistance optimization of silicon implanted samples has been carried out. The first indication is that the n-type doping condition used in standard FDSOI lots with activation at high temperature, are not adapted for an activation at low temperature. In fact, using the standard condition (co-doping arsenic and phosphorus) with an activation at 600 °C for two minutes leads to high sheet resistance degradation of 86% compared with a spike anneal activation.

Single dopant arsenic or phosphorus implant with different doses on different samples have been tested. Experimental measurements show that the best sheet resistance value have been obtained for the lower implanted doses for both arsenic and phosphorus. This is due to the clustering phenomenon: SPER activation is really efficient in dopant activation until a certain value of dopant concentration corresponding to the clustering limit. Above this concentration level sheet resistance degradation appears. For arsenic, this phenomenon is related to an activation level degradation, while for phosphorus it is due to a mobility degradation. Phosphorus sample with low implanted dose and low temperature activation even outperforms of 18% the sheet resistance value of the process of reference, demonstrating the interest of dopant activation at low temperature by SPER.

Similar experiments have been carried out for boron, obtaining the same tendency. The total implanted dose has to be limited in order to avoid the clustering phenomenon, i.e., the formation of inactive agglomerations.

The clustering limit values have been extracted: for arsenic $8x10^{20}$ at/cm$^3$, for phosphorus $6x10^{20}$ at/cm$^3$. For boron the value is known in literature at $3x10^{20}$ at/cm$^3$. The ideal profile along the junction depth should be as constant as possible and close to this value.

After the definition of the optimized dopant profile for sheet resistance, another aspect has been analyzed: the re-crystallization velocity, also called SPER rate. This parameter is strongly dependent on the annealing temperature (following an Arrhenius's law) and the dopant concentration. SPER rate dependence with dopant concentration has been measured by in-situ ellipsometry for phosphorus and boron for different re-crystallization temperature (down to 450 °C), finding the optimal dopant concentration value to optimize the re-crystallization velocity. The limits of the analysis have been detailed as well.

Finally, sheet resistance measurement after low temperature activation by SPER have been carried out for thermal anneals at 500 °C and 600 °C. At first sight, sheet resistance degradation appeared for annealing at 500 °C and 450 °C for both phosphorus and boron compared to the values found at 600 °C. However, if the implantation step has been made before the removal of the $SiO_2$ native layer present in silicon surface, constant values of sheet resistance have been obtained for almost all the anneal temperatures. The sheet resistance degradation is due to the presence of oxygen introduced in the first nanometers of the silicon sample by recoil, which slows down the SPER rate until the re-crystallization stops. This is a really promising result since it demonstrates the feasibility of dopant activation by SPER down to 450°C for phosphorus and 500°C for boron.

**References**

[Cristiano13] Cristiano, Filadelfo. *Ion Implantation-Induced extended defects: structural investigations and impact on Ultra-Shallow Junction properties*. Diss. Université Paul Sabatier-Toulouse III, 2013.

[Csepregi76] L.Csepregi,J.W.MayerandT.W.Sigmon. Regrowth behavior of ion implanted amorphous layers on <111> silicon. Appl. Phys. Lett., vol. 29, no. 2, pages 92–93, 1976.

[Csepregi78] Csepregi, L., et al. "Substrate-orientation dependence of the epitaxial regrowth rate from Si-implanted amorphous Si." *Journal of Applied Physics* 49.7 (1978): 3906-3911.

[Demenev12] E. Demenev, D. Giubertoni, S. Gennaro, M. Bersani, E. Hourdakis, A. G. Nassiopoulou, M. A. Reading and J. A. van den Berg. Arsenic redistribution after solid phase epitaxial regrowth of shallow pre-amorphized silicon layers. AIP Conference Proceedings, vol. 1496, no. 1, pages 272–275, 2012.

[Duffy06] R. Duffy, T. Dao, Y.Tamminga, K. van der Tak, F. Roozeboom and E.Augendre. Groups III and V impurity solubilities in silicon due to laser, flash, and solid phase-epitaxial-regrowth anneals. Appl. Phys. Lett., vol. 89, no. 7, page 071915, 2006.

[El Farhane 05] El Farhane, Rebha. Contribution à l'étude et à l'intégration en technologie CMOS avancée de jonctions ultra minces et fortement dopées formées par des procédées à faible budget thermique. Diss. Toulouse 3, 2005.

[Fenouillet-Beranger 14] Fenouillet-Beranger, C., et al. "New insights on bottom layer thermal stability and laser annealing promises for high performance 3D VLSI." Electron Devices Meeting (IEDM), 2014 IEEE International. IEEE, 2014.

[Hobler03] G. Hobler and G. Otto. Status and open problems in modeling of as– implanted damage in silicon. Materials Science in Semiconductor Processing, vol. 6, no. 1–3, pages 1–14, 2003.

[Johnson07] Johnson, B. C., and J. C. McCallum. "Dopant-enhanced solid-phase epitaxy in buried amorphous silicon layers." *Physical Review B* 76.4 (2007): 045216.

[Kennedy77] Kennedy, E. F., et al. "Influence of 16O, 12C, 14N, and noble gases on the crystallization of amorphous Si layers." *Journal of Applied Physics* 48.10 (1977): 4241-4246.

[Magee81] Magee, T. J., et al. "Recoil oxygen implants and thermal redistribution of oxygen in through-oxide arsenic-implanted Si." *Applied Physics Letters* 39.7 (1981): 564-566.

[Martinez-Limia08] Martinez-Limia, A., et al. "Experimental investigations and simulation of the deactivation of arsenic during thermal processes after activation by SPER and spike annealing." *Materials Science and Engineering: B* 154 (2008): 211-215.

[Masetti83] Masetti, Guido, Maurizio Severi, and Sandro Solmi. "Modeling of carrier mobility against carrier concentration in arsenic-, phosphorus-, and boron-doped silicon." *Electron Devices, IEEE Transactions on* 30.7 (1983): 764-769.

[Narayan82] J. Narayan. Interface structures during solid-phase-epitaxial growth in ion implantedsemiconductorsand a crystallization model. J.Appl.Phys.,vol.53, no.12, pages 8607–8614, 1982.

[Nobili94] D.Nobili, S. Solmi, A. Parisini,M. Derdour, A. Armigliato and L. Moro. Precipitation, aggregation, and diffusion in heavily arsenic-doped silicon. Phys. Rev. B, vol. 49, pages 2477–2483, Jan 1994.

[Olson88] Olson, G. L., and J. A. Roth. "Kinetics of solid phase crystallization in amorphous silicon." *Materials Science Reports* 3.1 (1988): 1-77.

[*Pawlak 04] Pawlak, B. J., Surdeanu, R., Colombeau, B., Smith, A. J., Cowern, N. E. B., Lindsay, R., ... & Cristiano, F. (2004). Evidence on the mechanism of boron deactivation in Ge-preamorphized ultrashallow junctions. Applied physics letters, 84(12), 2055-2057.*

*[Petkov00] Petkov, Mihail P., et al. "A relation between surface oxide and oxygen-defect complexes in solid-phase epitaxial Si regrown from ion-beam-amorphized Si layers." Applied Physics Letters 76.11 (2000): 1410-1412.*

[Pinacho05] R. Pinacho, M. Jaraiz, P. Castrillo, I. Martin-Bragado, J. E. Rubio, and J. Barbolla, “Modeling arsenic deactivation through arsenic-vacancy clusters using an atomistic kinetic Monte Carlo approach,” Applied physics letters, vol. 86, pp. 252103 -252103-3, jun 2005.

[Rudawski08] N.G. Rudawski, K.S. Jones and R. Gwilliam. Stressed solid-phase epitaxial growth of ion-implanted amorphous silicon. Mater. Sci. Eng. R – Rep., vol. 61, no. 1–6, pages 40–58, 2008.

[Skorupa14] Wolfgang Skorupa, Heidemaire Schmidt. Subsecond Annealing of Advanced Materials : Springer Series in Materials Science 192, 2014.

[Solmi90] S. Solmi, E. Landi and F. Baruffaldi. High concentration boron diffusion in silicon: Simulation of the precipitation phenomena. J. Appl. Phys., vol. 68, no. 7, pages 3250–3258, 1990.

[Skarlatos07] D. Skarlatos and C. Tsamis, “Modeling of low energy-high dose arsenic diffusion in silicon in the presence of clustering-induced interstitial generation,” Journal of Applied Physics, vol. 102, p. 043532, 2007.

[Xu12] C. Xu, P. Batude, B. Sklenard, M. Vinet, M. Mouis, B. Previtali, F. Y. Liu, J. Guerrero, K. Yckache, P. Rivallin, V. Mazzocchi, S. Cristoloveanu, O. Faynot, and T. Poiroux, “FDSOI: A solution to suppress boron deactivation in low temperature processed devices,” Proceedings of the 12th International Workshop on Junction Technology (IWJT 2012), pp. 69 -72, 2012.

[Woodard06] E-M. Woodard, R-G. Manley, G. Fenger, R-L. Saxer, K-D. Hirschman, D. Dawson-Elli, J. G. Couillard; “Low Temperature Dopant Activation for Integrated Electronics Applications”; IEEE 16th Biennial University/Government/Industry Microelectronics Symposium, pp161 (2006).

# Chapter 2: Electrical results and optimization Guidelines for Low Temperature FDSOI devices

## 2.1 Definition and operation of a MOSFET transistor

In this section, a brief presentation of the structure and the basic principles of a MOSFET transistor are presented in order to understand the following part of the manuscript. For more details, the reader can refer to [Skotnicki 00], [Sakurai 06].

The metal–oxide–semiconductor field-effect transistor (MOSFET) is a type of transistor used for switching electronic signals. It is mainly made of three layers: a semiconductor substrate where the current flows between two regions called source and drain. The current flow is possible by a field effect via the polarization of a layer formed by a metal (gate) through a thin layer of dielectric material, typically named as gate oxide. The region below the gate, where the current conduction occurs is named channel. Two types of transistors can be defined depending on the sign of the gate polarity that determines the conductive state. If the source and drain regions are doped with n-type impurities (typically arsenic or phosphorus) the carriers conduction is made by electrons; this device is called nMOS. In case of holes conduction, where the source and drain regions are doped by p-type impurities (typically boron), the device is called pMOS.

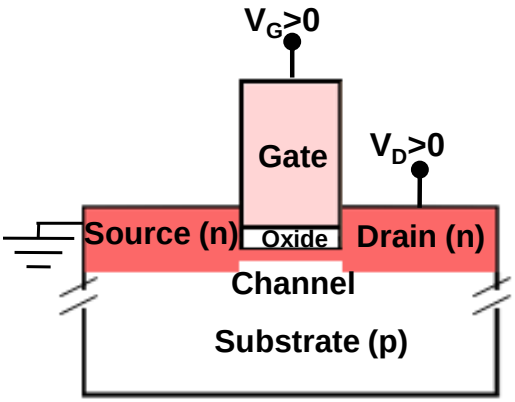



**Figure 2.1: nMOS transistor scheme in ON state.**

Figure 2.1 illustrates the main elements of a nMOS transistor. When $V_{GS}>0$ (so called inversion mode), an electron layer is formed below the gate stack, allowing the conduction between the source and the drain. The drain current characteristic ($I_{DS}$) as a function of $V_{GS}$ is illustrated in Figure 2.2. For $V_{GS}<0$ the transistor is not conductive (OFF state) since the inversion channel is not formed and for $V_{GS}=0$, $I_{DS}=I_{OFF}$ (leakage current). In order to have a sufficient number of carriers, $V_{GS}$ has to be higher than a value defined as threshold voltage ($V_T$). So, the transistor is in ON state when $V_{GS}>V_T$ (strong inversion mode). For $0<V_{GS}<V_T$ (weak inversion mode), the flowing current is defined as subthreshold current.

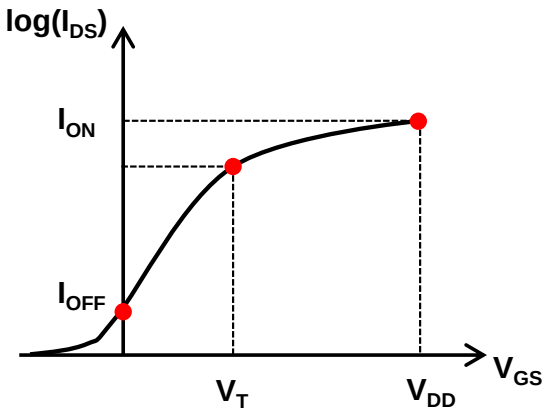



**Figure 2.2: $I_{DS}(V_{GS})$ nMOS characteristic.**

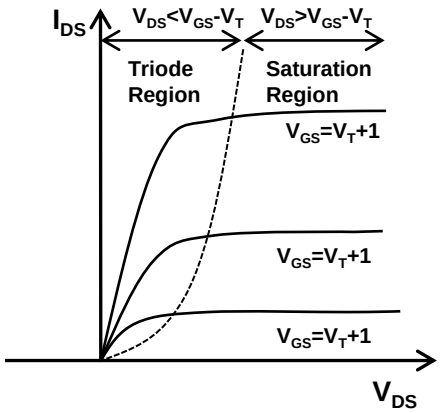



**Figure 2.3: $I_{DS}$ ($V_{DS}$) characteristic for nMOS. The line $V_{DS}=V_{GS}-V_T$ divides the triode mode from saturation mode.**

In strong inversion mode, there are two possible working regimes depending on $V_{DS}$ value: linear (or triode) mode and saturation mode. A typical $I_{DS}(V_{DS})$ characteristics for nMOS is illustrated in Figure 2.3. In linear mode drain current can be expressed by equation (2.1):

$$I_{D,lin} = \mu_{eff} C_{ox} \frac{W}{L} \frac{V_{GS}-V_T}{1+\theta_1(V_{GS}-V_T)} V_{DS} \tag{2.1}$$

Where $\mu_{eff}$ is the carrier mobility of the carriers into the channel, $C_{ox}$ is the gate oxide capacitance per unit area, W and L the width and the length of the transistor. $\theta_1$ represents the reduction factor of the mobility due to the scattering between the carriers and the phonons of the semiconductor lattice. In saturation mode:

$$I_{D,sat} = \mu_{eff} C_{ox} \frac{W}{2L} {V_{DS}}^2 \tag{2.2}$$

Equations (2.1) and (2.2) are valid for long channel transistors. For short channels transistors, due to higher longitudinal field (or at high $V_{DS}$ in sufficiently short transistor) the mobility saturates due to either (i) the velocity saturation due to optical phonon scattering, i.e. energy exchange with the lattice or (ii) to the ballistic limit where the mobility is no more limited by scattering. This leads to a saturation of the carrier the mobility that may be no longer constant. In linear mode, the mobility reduction is taken into account with the second attenuation factor $\theta_2$. This factor is not strictly related to short channel device, but can be related to surface roughness scattering in long device also. The reduction of short channel devices is either apparent (ballistic case and/or $V_G$ dependence of access resistance)

or due to some interaction at the proximity of S/D. Taking these considerations into account, drain current for linear and saturation mode can be expressed by equations (2.3) and (2.4) respectively.

$$I_{D,lin} = \mu_{eff} C_{ox} \frac{W}{L} \frac{V_{GS} - V_T - \frac{V_{DS}}{2}}{1 + \theta_1 (V_{GS} - V_T) + \theta_2 (V_{GS} - V_T)^2} V_{DS} \tag{2.3}$$

$$I_{D,sat} = I_{D,sat}(1 + \frac{V_{DS} - V_{DS,sat})}{\frac{L}{\lambda_0} V_{DS,sat}}, \text{ with } \lambda_0 = \sqrt{\frac{\varepsilon_s}{\varepsilon_{ox}} x_j t_{ox}} \tag{2.4}$$

Where $\varepsilon_s$ and $\varepsilon_{ox}$ are the permittivity of silicon and gate oxide; $x_j$ and $t_{ox}$ are the thicknesses of the inversion channel and of the gate oxide respectively.

Equation (2.1) assumes that the source and drain regions are perfectly conducting. In reality, as the current flows from the channel to the terminal contact, there is a small voltage drop in the source and drain regions due to the finite silicon resistivity and metal contact resistance. In a long channel device, the source and drain parasitic resistance is negligible compared to the channel resistance. However, in a short channel device, these two resistance become comparable and can therefore cause a significant current degradation.

Total transistor resistance is then defined as:

$$R_{TOTAL} = \left.\frac{V_{DS}}{I_{DS}}\right|_{V_{DLin}} = R_{ch} + R_{access} \tag{2.5}$$

Where, $R_{access}$ is the access resistance and $R_{ch}$ the channel resistance.

$R_{TOTAL}$ is often referred as $R_{ON}$ as well. It is worth noticing that $R_{ON}$=$R_{TOTAL}$ is extracted at $V_{DLin.}$ This can create confusion concerning the ON appellation: while ON current refers to the $I_{DS}$ at $V_{DS}$=$V_{DD}$, $R_{ON}$ is extracted at $V_{DLin}$.

Considering the source and drain resistance (also called access resistance) contribution, the drain current in linear mode is reduced compared to the intrinsic current of the transistor $I_{D0}$:

$$I_D = \frac{I_{D0}}{1 + \frac{R_{access}}{R_{ch}}} \tag{2.6}$$

## 2.2 Fully-Depleted Silicon On Insulator (FDSOI)

In order to continue delivering higher performance and keeping the leakage under control, especially regarding the short channel effects, bulk-silicon transistors have become more and more complex, adding additional manufacturing steps. More recently, it has been considered to move to new, expensive and complex, 3D architectures such as TriGate or FinFET devices.

Fully Depleted Silicon On Insulator (FDSOI) appears as one of the most interesting alternatives to sustain the scaling of microelectronics device dimensions keeping a relatively simple manufacturing process.

The key feature of the SOI structure is the $SiO_2$ layer just below the active semiconductor layer called Buried Oxide (BOX). The main advantage of SOI is the improved electrostatic control compared to bulk transistors. This is due to the thin silicon thickness of the channel below the gate that allows to limit short channel effects. Other interesting features of SOI transistors are: negligible drain to substrate capacitance, independent body bias and $V_T$ adjustment, ideal device isolation, smaller layout area and lower variability. More details about SOI devices can be found in [Sakurai 06], [Fenouillet 13].

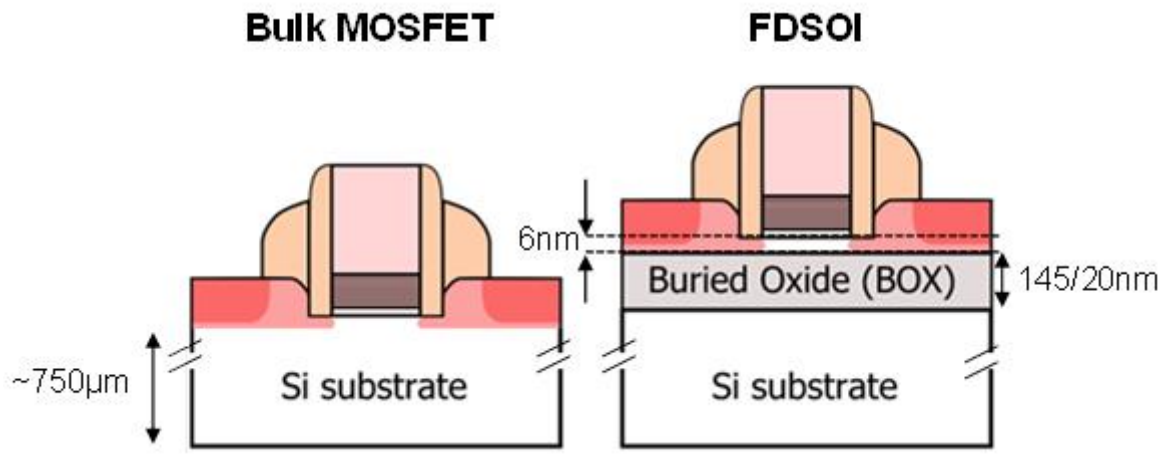



**Figure 2.4: Schematic representation of Bulk and FDSOI MOSFET devices. Typical dimensions of FDSOI device for 28nm node are reported as well.**

## 2.3 Process flow presentation

In this section, the process flow of the devices under study is presented. First, the process flow of the state of the art technology, considered as the benchmark reference for the low temperature devices, is detailed. Then, the process steps modification for low temperature process are highlighted.

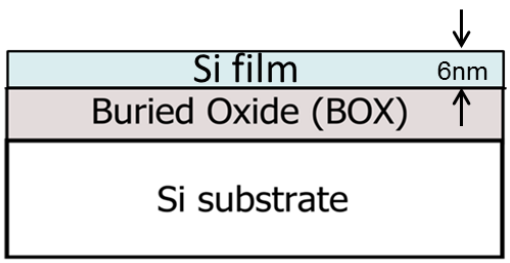
### 2.3.1 Process Of Reference description

The study proposed in this chapter has been carried out using devices based on the 28nm FDSOI technology developed by STMicroelectronics [Arnaud 15], [Golanski 13]. The Process Of Reference (POR), also called High Temperature process (HT) is described in Figure 2.5. Here is reported step by step:

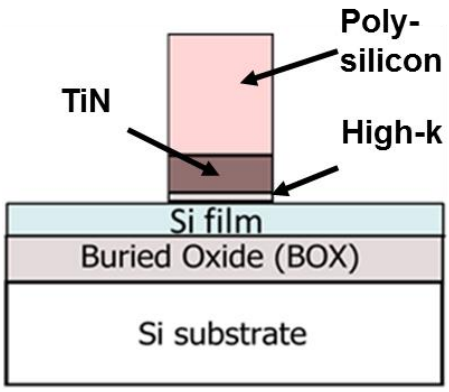
- **Active zone definition**: 6nm Silicon on 25 nm Buried Oxide is used.
- **Gate patterning**: gate stack is made by a deposition of three layers: HfSiON for the gate oxide; TiN used as the metal fixing the work function and defining $V_T$ . Finally, a layer of poly-silicon is deposited.

- **First spacer deposition**: 6 nm SiN layer deposition is made. An etching step is used to keep spacer on the gate edges only, removing the nitride from silicon film surface.
- **Raised source and Drain Epitaxy**: the source and drain regions are made by a silicon epitaxial growth of 16 nm.
- **Light Dose Doping (LDD)**: a first dopant implantation is made in the source and drain regions. arsenic and $BF_2$ are used for nMOS and pMOS respectively with an implanted dose of $1x10^{15}$ at/cm$^2$.
- **Second spacer formation.**
- **High Dose Doping (HDD):** a second doping step is performed; for nMOS a tri-implant phosphorus/arsenic/phosphorus is performed with a total dose of $4.5x10^{15}$ at/cm$^2$. For pMOS a bi-implantation boron/$BF_2$ is made with a total dose of $3.8x10^{15}$ at/cm$^2$.
- **Dopants activation:** high temperature spike annealing (1050 °C) is applied to recover defects due to ion implantation and to activate the dopants.
- **Silicidation:** silicidation process is performed, on transistor source, drain and gate in order to promote an ohmic contact with the later tungsten plug. Currently, nickel platinium (NiPt) alloy is used for the 28 nm FDSOI technology. NiPt salicidation process involves five steps: a NiPt deposition followed by a Titanium Nitride (TiN) hard mask deposition. TiN hard mask is ued to protect the alloy during subsequent annealing. Then, first Rapid Thermal Anneal (RTA) is performed to consume the entire alloy deposited. Third step, a selective etch removes the hard mask and the unreacted alloy. Before the last step, another RTA is performed to create the lowest resistive phase. Finally, a last selective etch is performed to remove the residual Pt.
- **Contact:** a metal, such as tungsten (W) is deposited on the silicide, in order to realize the source, drain and gate electrodes.
- **Back End of Line (BEOL):** Depending of the application, several metal levels can be built in order to connect the transistors with each other and to create the electrical circuits.

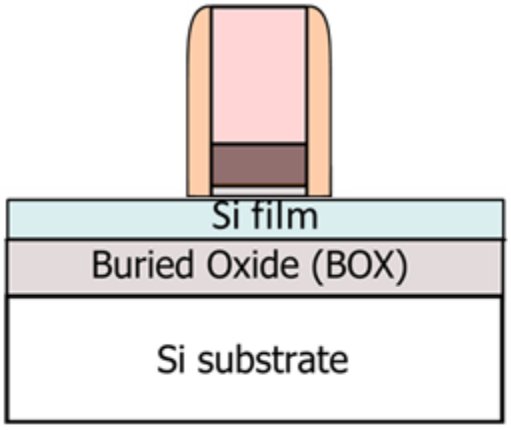
**1) Active Zone definition**



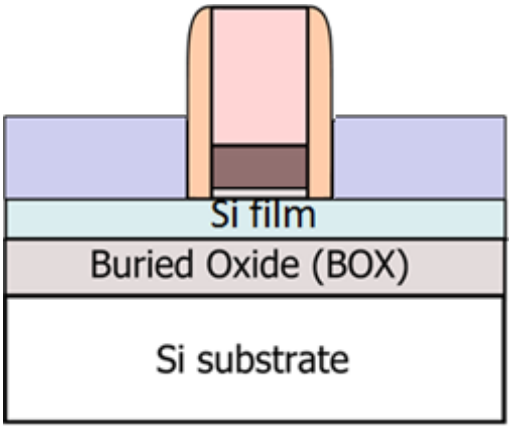

**2) Gate patterning**



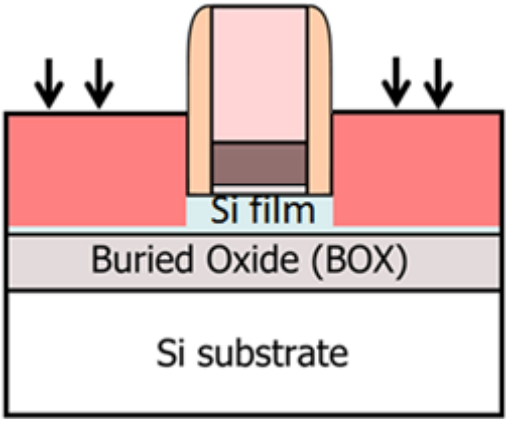
**3) First Spacer deposition**



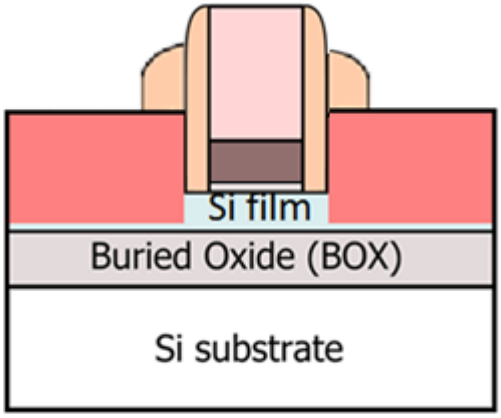

**4) Raised Source/Drain Silicon Epitaxy**



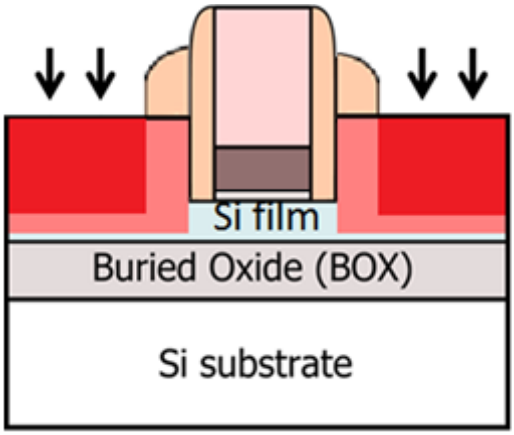

**5) LDD Implantation**



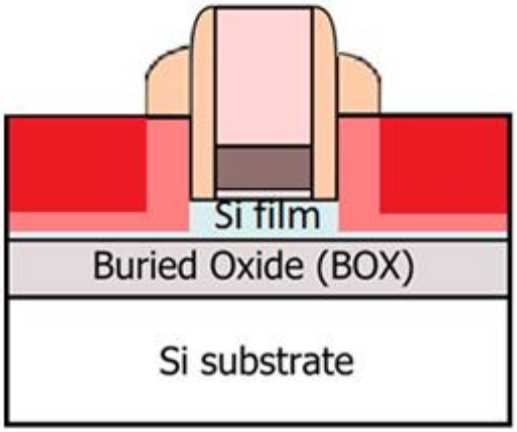

**6) Spacer 2 deposition**




**7) HDD Implantation**




**8) Dopant activation at 1050°C**



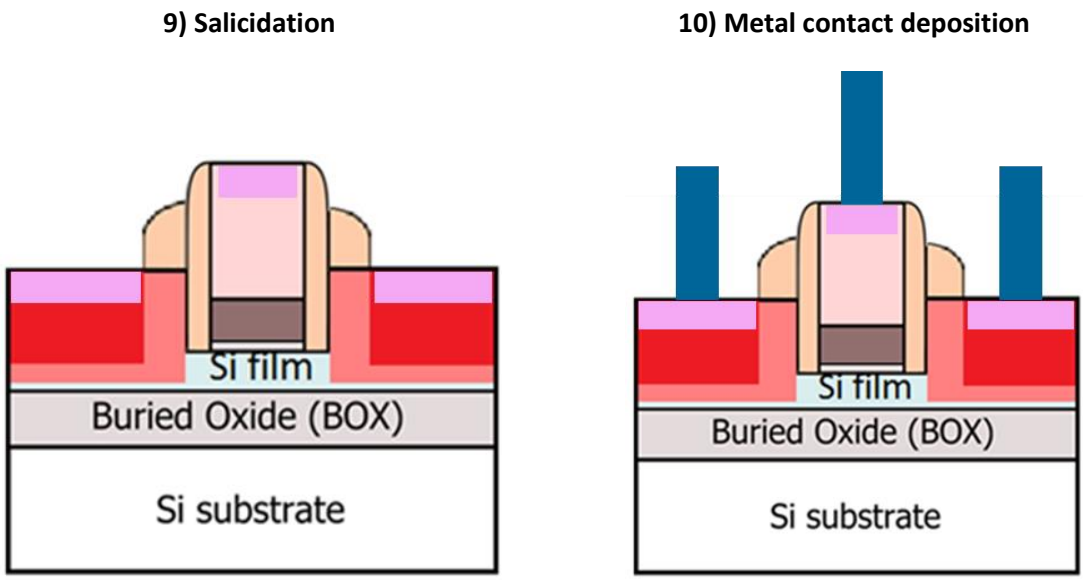



**Figure 2.5: Standard process flow for 28nm FDSOI technology.**

### 2.3.2 Low temperature process description

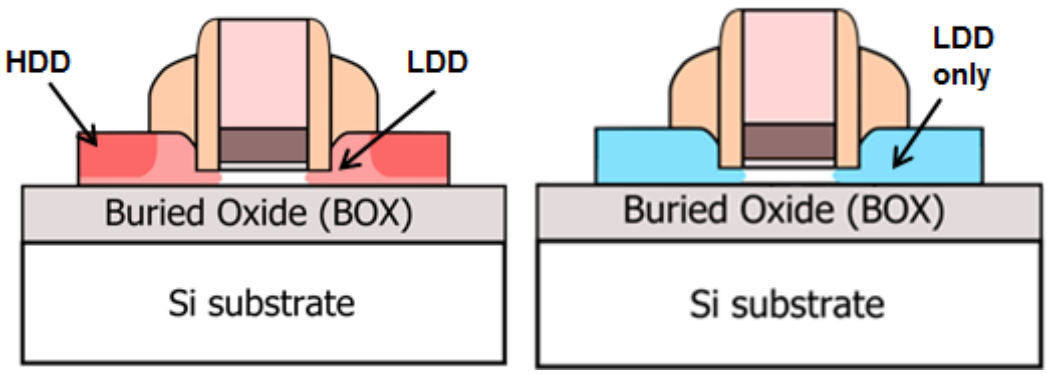



**Figure 2.6: Difference in doping strategy for high temperature and low temperature devices.**

The fabrication of low temperature devices studied in this work follows the process of reference until the raised source and drain epitaxial growth.

As presented in chapter one, for dopant activation by SPER, high dopant concentration (above the clustering limit) leads to $R_{SHEET}$ degradation. For this reason, in the low temperature process flow, only LDD doping step is performed, excluding HDD. The different doping strategies between high

temperature and low temperature devices are schematically shown in Figure 2.6 and the overall process flow comparison is reported in Figure 2.7.

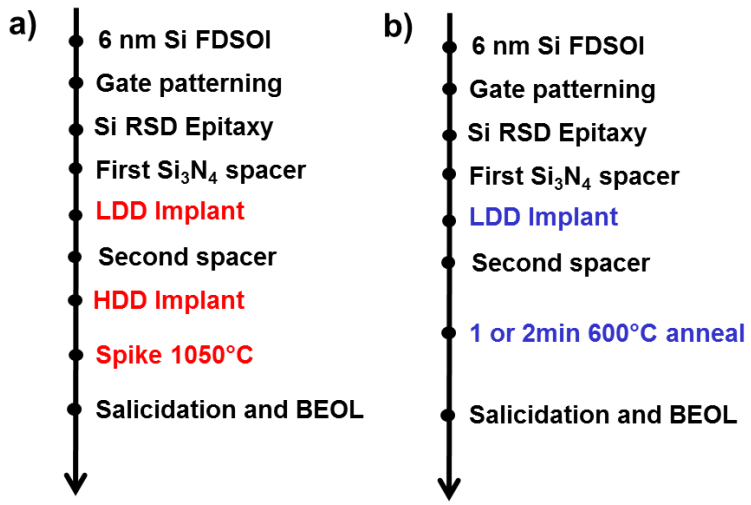



**Figure 2.7: Process flow comparison between high temperature (a) and low temperature (b) devices.**

Two doping conditions for LDD have been tested for low temperature devices. The two splits will be named LT Phosphorus and LT Arsenic in correspondence with the implanted specie. Here are the implantation conditions:

- LT Phosphorus: P 9 KeV $6x10^{14}$ at/cm$^2$ tilt 15°
- LT Arsenic: As 10 KeV $5x10^{14}$ at/cm$^2$ tilt 15° + As 3 KeV $3x10^{14}$ at/cm$^2$ tilt 0°

As explained in the first chapter, it is necessary to preserve a crystalline seed that can act as a pattern for the recrystallization by SPE. The choice of seed thickness is crucial, since a full amorphization would prevent the re-crystallization by SPE. However, a thick seed would mean a significant part of the source and drain regions with no active dopants (since activation by SPE is efficient in the amorphized region only). For low temperature devices, a seed thickness of 3 nm has been chosen, which corresponds to an amorphization depth of 19 nm.

The interest of testing phosphorus in LDD, instead of arsenic which is used in the process of reference is twofold: (i) as mentioned in chapter one, for the same dopant concentration, carrier mobility in phosphorus doped silicon is higher than with arsenic. This leads to a lower resistivity for phosphorus than arsenic for the same doping profile. Phosphorus is not used in POR because its high diffusion could lead to undesired doping into the channel region. This issue is not present for low temperature devices, since the diffusion is totally negligible for the thermal budgets considered. (ii) Arsenic atomic mass is higher than phosphorus ($m_{As}$=74.9 u, $m_P$= 30.9 u). It means that lower dopant concentration compared to phosphorus is necessary to reach the same amorphization depth. Simulation results show that with phosphorus implant it is possible to define a quasi-constant profile at concentrations suitable with the sheet resistance target (Figure 2.8), while for arsenic, if 3 nm of crystalline seed have to be preserved, concentration above $1x10^{20}$ at/cm$^3$ cannot be placed over 16 nm, since higher

concentration would lead to full film amorphization). Thus, the last 6 nm of the access regions would not be well.

Arsenic implant has been performed in two steps in order to obtain a constant profile, with a first step at high energy and low dose to try to place high dopant concentration in depth. However, non-uniform profile has been still obtained. The one-dimensional chemical profiles of LT Phosphorus and LT Arsenic are shown in in Figure 2.8 and 2.9 respectively.

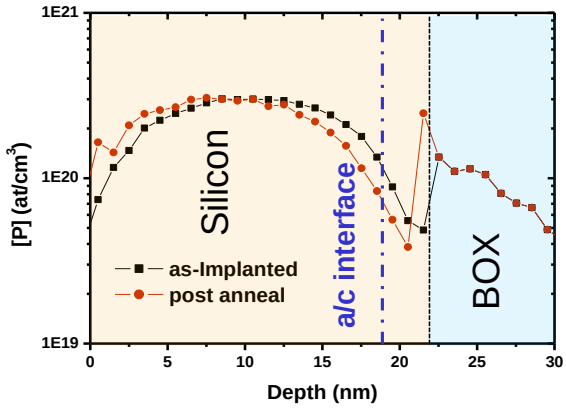



**Figure 2.8: One dimensional phosphorus chemical profile.**

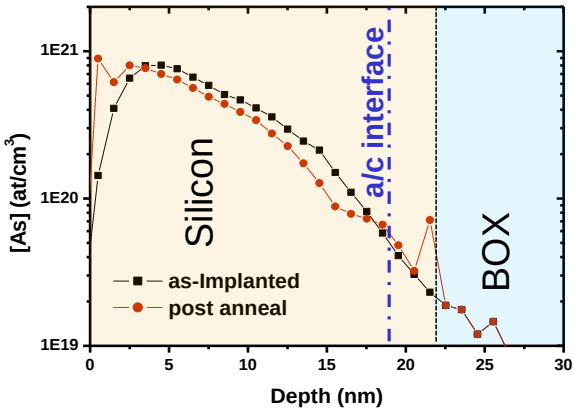



**Figure 2.9: One dimensional arsenic chemical profile.**

## 2.4 Low temperature nMOS electrical analysis

In this section, the electrical characterization of high and low temperature devices is shown. The analysis is supported by both process and device simulations in order to get better physical understanding.

Both high temperature and low temperature devices with width of 1 µm and channel lengths ranging from 26 nm to 1 µm have been characterized. $I_{ON}$-$I_{OFF}$ trade-off comparison between process of reference and low temperature with phosphorus or arsenic doping devices is shown in Figure 2.10. Working devices are demonstrated for both phosphorus and arsenic split at low temperature. However, at constant $I_{OFF}$ =$10^{-7}$ A/µm, a 20% $I_{ON}$ degradation is observed for the best low temperature device that corresponds to the phosphorus doping. Even higher performance degradation (44%) is observed for low temperature device with arsenic doping.

Considering equations (2.1)-(2.5) the parameters that can impact the $I_{ON}$ value are: the carrier mobility, the inversion channel thickness and the access resistance. In next sections, a detailed electrical characterization of the listed parameters is provided in order to explain this performance degradation for low temperature in comparison with high temperature devices.

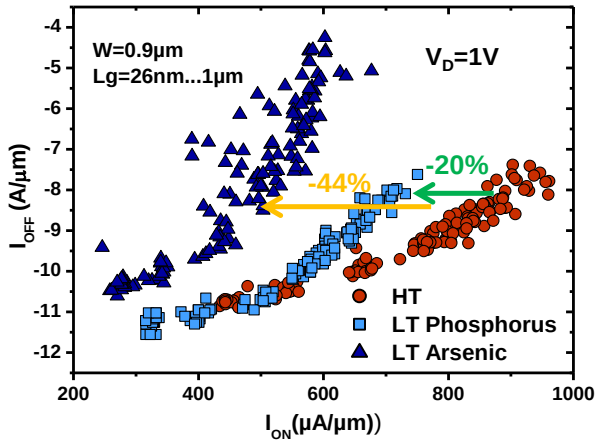



**Figure 2.10: $I_{ON}$-$I_{OFF}$ trade-off for nMOS high temperature device, considered as the reference and low temperature devices. Performance degradation is observed for low temperature devices.**

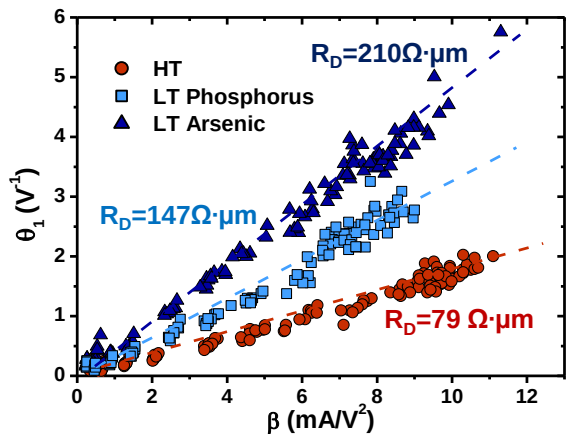



**Figure 2.11: Access resistance extraction by Y function method for high temperature and low temperature devices. The resistance values reported, correspond to half of the total access resistance (drain resistance).**

### 2.4.1 Access Resistance

In low temperature devices, the doping conditions and activations annealings have been modified with respect to the high temperature process of reference. The most suspected parameter responsible of performance degradation for low temperature devices is the access resistance, that is strictly related to the doping activation in the source and drain regions. This parameter, can be extracted by several methods [Chang 07], [Fleury 09]. However, Y function method [Ghibaudo 88], [Subramanian 10] is widely used for advanced devices and it will be used in this work as well. More details about the extraction method will be provided in section 2.6. In Figure 2.11 access resistance extraction is shown for high temperature and low temperature devices. It is worth noticing that the values reported in Figure 2.11 correspond to the half of the total access resistance, for example the drain region only. The corresponding parameter is then named drain resistance, $R_D$. This graph clearly evidences the correlation between performance degradation of low temperature devices (Figure 2.10) and access resistance degradation (corresponding to the slope increase for low temperature splits in Figure 2.11). Indeed, for the high temperature split, $R_D$=79 Ωxµm is found while for phosphorus $R_D$ increase to 147 Ωxµm. Even stronger degradation is observed for LT Arsenic where $R_D$ value is equal to 210 Ωxµm. These results appear contradictory with full sheet conclusions shown in the first chapter where SPER activation was observed to lead to equivalent (or even lower) sheet resistance than high temperature spike annealing. Deeper analysis on the composition of access resistance is needed.

Equation (2.6) defines the access resistance as the resistance corresponding to the voltage drop in the source and drain regions. Access resistance can be also decomposed in several resistance contributions corresponding to the different regions of the access. A simple definition, corresponding to the scheme proposed in Figure 2.12 is:

$$R_{access}=R_{co}+R_{sil}+R_{sil/dop}+R_{HDD}+R_{LDD}+R_{SPA} \quad (2.10)$$

where $R_{co}$ is the contact resistance, $R_{sil}$ the resistance corresponding to the silicided region, $R_{sil/dop}$ the interface resistance between silicided region and doped region, $R_{HDD}$ and $R_{LDD}$ the resistances related to higly and lightly doped region respectively and $R_{SPA}$ the resistance corresponding to the zone below the first spacer. The goal is to individuate which of these contributions is preponderant in the total access resistance degradation observed in Figure 2.11.

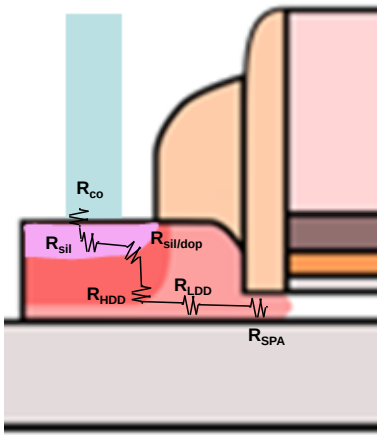



**Figure 2.12: Access resistance contributions scheme.**

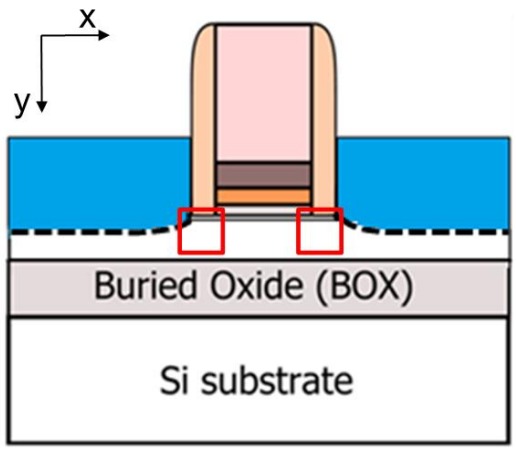



**Figure 2.13: The region below the first spacer is difficult to dope with low temperature dopants activation for two reasons: (i) difficulty in creating amorphous region and (ii) no dopant diffusion for low temperature activation.**

$R_{co}$, $R_{sil}$ and $R_{sil/dop}$ can be considered equivalent for high temperature and low temperature devices even though a small variation due to the different doping conditions could cause a second order variation. In chapter one, it has been shown that SPER activated films could lead to sheet resistance values similar to the one obtained by spike annealing. This corresponds to $R_{HDD}$+$R_{LDD}$ series resistances. However, the dopant conditions optimization has been carried out considering one-dimensional profile because by means of sheet resistance characterization only the information of the in depth direction can be investigate, while no information can be extracted on the lateral direction. In a real planar structure such as a FDSOI transistor, it is necessary to take into account the junction shape in two spatial directions: in depth direction (y axis in Figure 2.13) and lateral direction (x axis in Figure 2.13). So, a good sheet resistance value does not mean that a good junction shape is formed in the lateral direction in a real FDSOI device.

It is worth remembering two features of dopant activation by SPER:

I. The dopant activation is efficient in the amorphized region only;
II. For annealing temperature below 600°C, the dopant diffusion is negligible.

These two aspects make extremely complex to place activated dopant in the region below the first spacer (Figure 2.13).

In order to confirm these assumptions, the process flow of high temperature and low temperature devices have been simulated and the dopant concentration in the region below the spacer is shown in Figure 2.14, 2.15 and 2.16.

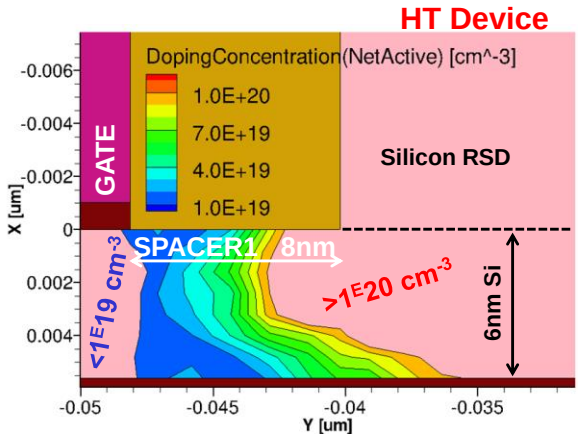



**Figure 2.14: Dopant concentration under first spacer extracted from KMC simulation for high temperature device.**

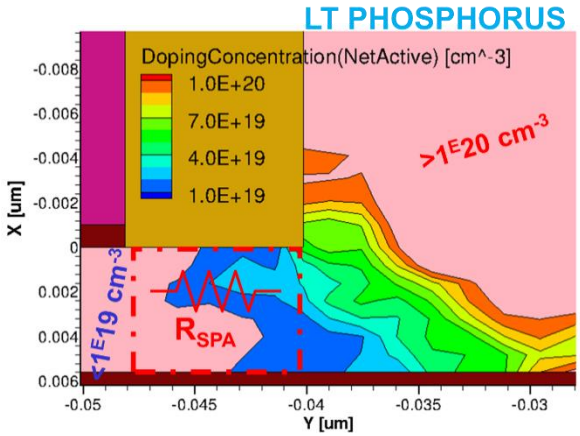



**Figure 2.15: Dopant concentration under first spacer extracted from KMC simulation for low temperature device with phosphorus doping device. $R_{SPA}$ is also defined.**

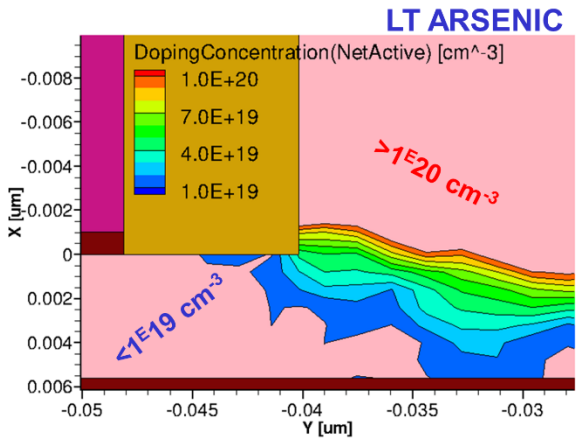



**Figure 2.16: Dopant concentration under first spacer extracted from KMC simulation for low temperature device with arsenic doping device.**

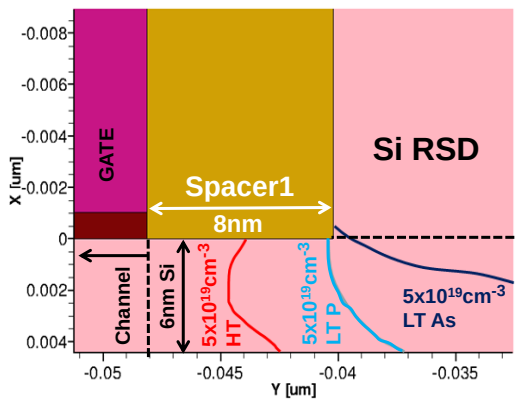



**Figure 2.17: $5x10^{19}$at/cm$^3$ iso-concentration evolution of high temperature and low temperature devices obtained by KMC simulation.**

It is clear that the dopant concentration below the first spacer is higher for high temperature device ($10^{20}$ at/cm$^3$ iso-concentration line is almost completely below the first spacer), than for low temperature devices (only concentration around $10^{19}$ at/cm$^3$ is reached below the first spacer). Figure 2.22 shows the $5x10^{19}$ at/cm$^3$ iso-concentration position and its evolution for the three devices. For high temperature device, the iso-concentration at $5x10^{19}$ at/cm$^3$ is near to the middle of the spacer thickness. For low temperature devices, all the 8 nm of the region below the first spacer contains a dopant concentration below $5x10^{19}$ at/cm$^3$. This lack of high active dopant concentration in the region below the spacer is translated into a $R_{SPA}$ degradation that could explain the access resistance degradation for low temperature devices.

In order to have a quantitative analysis, the $R_{SPA}$ values for the three devices under study have been extracted by means of SDEVICE simulation. The software considers the local variation of the quasi Fermi level in correspondence of the doping concentration. Defining a particular zone, in this case, the region below the first spacer, the quasi Fermi level variation can be translated in a voltage drop. From the simulated $I_{DS}(V_{GS})$ characteristic in linear region, it is possible to extract the corresponding resistance value of the defined zone. It is important to notice that the resistance value is influenced by the electric field created by the gate electrode. In fact, access resistance is well known to be dependent on the applied gate voltage, with the most sensitive part being the region close to the channel, defined as $R_{SPA}$. This point will be discussed in section 2.5.1. In the case under study, the $R_{SPA}$ values have been extracted at $V_{GS}$-$V_T$=0.7 V.

$R_{SPA}$ values extracted by SDEVICE simulations are reported in the histogram of Figure 2.18 for the three tested devices together with the total drain resistance experimental values reported in Figure 2.11. A significant part of the access resistance, comes from the $R_{SPA}$ contribution. In particular, $R_{SPA}$ contributes for 29% of the drain resistance for high temperature device growing to 56% and 68% for LT phosphorus and LT arsenic devices respectively. This means that the main part of the total drain resistance that suffers from degradation in the split comparison is $R_{SPA}$, while the rest, represented by the purple part is basically constant. The access resistance degradation trends between low temperature and high temperature devices shown in Figure 2.11 can be mainly explained by the $R_{SPA}$ degradation for low temperature devices.

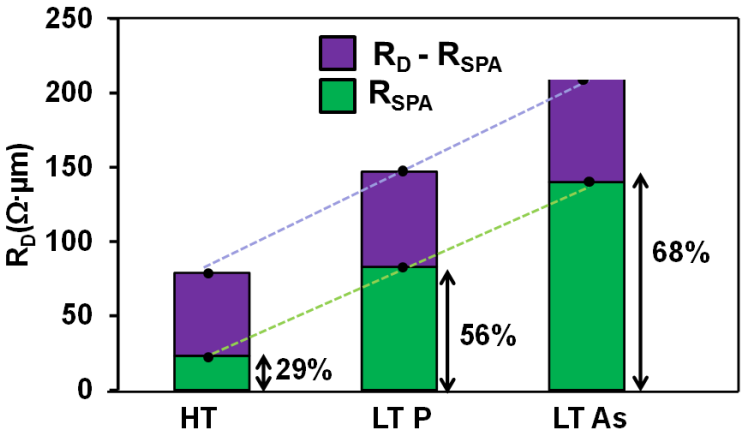



**Figure 2.18: $R_{SPA}$ contribution extracted by SDEVICE simulation. The percentage of $R_{SPA}$ on total drain resistance (experimentally measured) is also shown.**

An important consideration about the use of simulation tool has to be discussed at this point. Process simulation tool is well calibrated on physical phenomena related to the implantation step. Doping diffusion after spike annealing is correctly taken into account as well. However, dopant activation by SPER is based on different physical models which are not completely well calibrated yet. SPER annealing involves different phenomena such as dopant diffusion in amorphous or crystalline silicon at low temperature, doping activation, cluster formation, and crystallization rate. This makes complex, at this stage, a quantitative analysis. For these reasons, dopant concentration profile for low temperature annealing cannot be considered perfectly representative of the real device. However, since a good correspondence in $R_{SPA}$ extraction with electrical results is observed, it can be assumed that the trend on different splits is well predicted by simulation tool. As a conclusion, even

though $R_{SPA}$ value cannot be considered quantitatively correct, it will be considered as an important parameter for the implant conditions definition and optimization of the access resistance.

### 2.4.2 Electrical and Physical Gate Length

Generally, two parameters can be used to define the channel length:

- The **physical Gate length ($L_{phys}$):** the physical distance between the source and the drain regions. In this work it will be considered as the physical distance between the internal spacer edges.
- The **electrical channel length ($L_{elec}$):** the effective part of the channel controlled by the gate electrode. If a non-negligible dopant concentration is present into the channel edges, the creation of an inversion layer it will be possible only in a limited region of the channel.

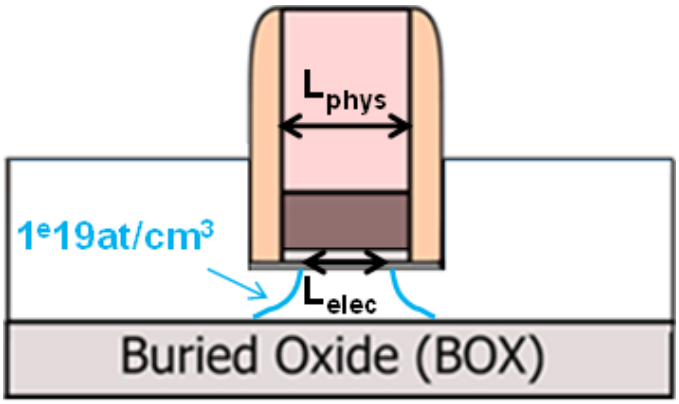



**Figure 2.19: Physical ($L_{phys}$) and electrical ($L_{elec}$) gate length definition.**

Ideally, a p-n junction is perfectly abrupt, but a dopant concentration gradient necessarily exists in a real device. In order to define the junction position, an iso-concentration value has to be chosen. Simulation results reported in Figure 2.20 show that dopant concentration below $1x10^{19}$at/cm$^3$ does not lead to any reduction of the electrical gate length. In Figure 2.19, the definition of physical and electrical channel lengths are illustrated. It is important to remark that the junction definition at $1x10^{19}$at/cm$^3$ of doping concentration is not a universal definition, but it is used in this work in agreement with simulation results of Figure 2.20.

Depending on the position of the $1x10^{19}$ at/cm$^3$ iso-concentration, two device configurations are possible:

- **Overlap configuration**, when higher dopant concentration than $1x10^{19}$ at/cm$^3$ is present into the channel region. In this case, the gate electrode does not control the whole physical channel length ($L_{phys}$). It can be defined an electrical channel ($L_{elec}$) length as:

$$L_{elec}=L_{phys}-\Delta L \qquad (2.9)$$

  Where $\Delta L$ is the part of the channel not controlled by the gate, due to higher dopant concentration above $1x10^{19}$ at/cm$^3$ coming from the accesses.

- **Underlap configuration**, when the dopant concentration in the channel region remains lower than $1x10^{19}$ at/cm$^3$ and ΔL=0.

Simulation results presented in Figure 2.14, 2.15 and 2.16 show that the three devices are in underlap configuration since no dopant concentration higher than $1x10^{19}$at/cm$^3$ is present into the channel region and ΔL=0 can be assumed. This is consistent with the DIBL (Drain Induced Barrier Lowering) behavior for the three devices shown in Figure 2.21. Small difference in DIBL between high temperature devices and low temperature devices are observed. So, fixing a DIBL value, no significant ΔL can be extracted.

As a conclusion, both simulation and electrical characterization suggest that both high temperature and low temperature devices are in underlap configuration. In this situation, even though difference in junction shape can appear, no significant variations in DIBL are evidenced.

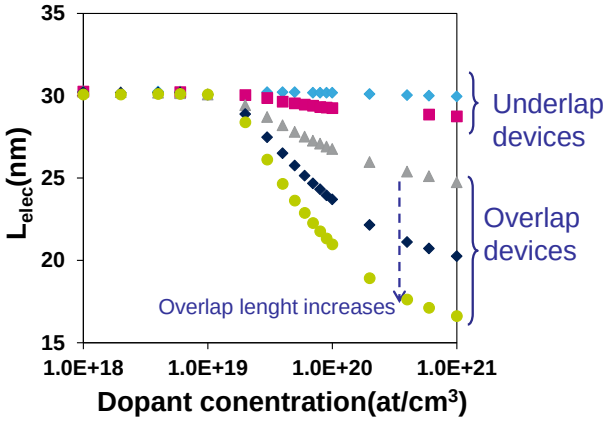



**Figure 2.20: Overlap/underlap configuration definition obtained by simulation results.**

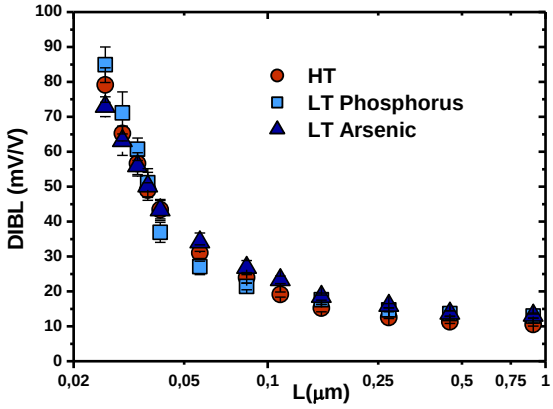



**Figure 2.21: DIBL behavior at different gate lengths for high temperature and low temperature devices.**

### *Carrier mobility*

Low field carrier mobility has been extracted by Y function method and the results are shown in Figure 2.22. For long channel length (L>50 nm) high temperature device shows higher mobility than low temperature devices. This can be attributed to a gate stack modification for low temperature devices compared to high temperature (for long channel length, junctions contribution is negligible). This behavior can be explained by the presence of dipoles at high-k/channel interface that can modify the apparent work function as reported in [Charbonnier 10]. However, for short channel lengths, no difference in mobility is observed between high temperature and low temperature devices, so low temperature activation does not influence the channel transport in scaled n-type FDSOI devices.

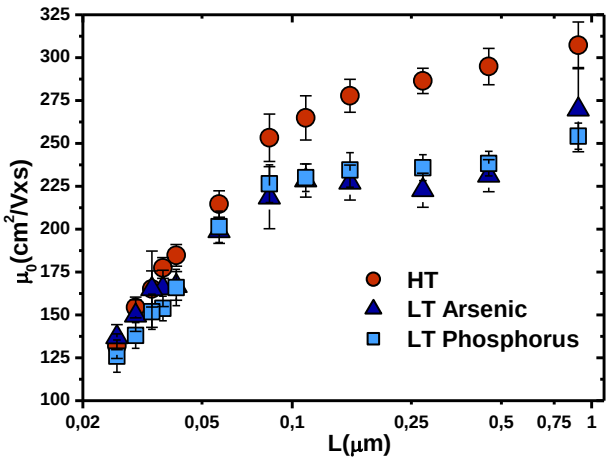



**Figure 2.22: Carrier mobility at low electric field for different gate lengths extracted for high temperature and low temperature devices.**

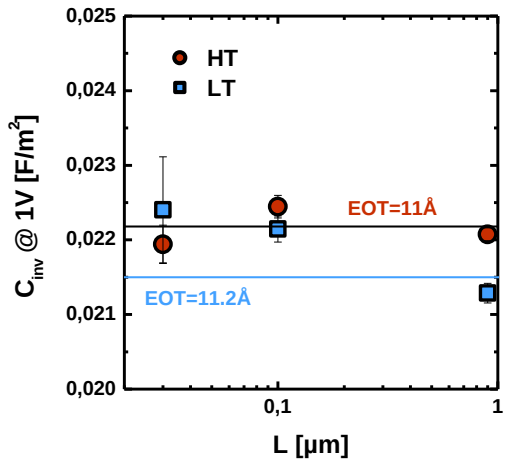



**Figure 2.23: EOT for different gate lengths extracted for high temperature and low temperature devices.**

### *Equivalent Thickness Oxide*

Equivalent thickness oxide (EOT) is used to compare performance of high-k dielectric and $SiO_2$ MOSFET gates. It is defined as:

$$EOT = \frac{\varepsilon_{SiO_2}}{\varepsilon_{HK}} t_{HK} = \frac{\varepsilon_{SiO_2}}{c_G} \tag{2.9}$$

Where $C_G$ is the gate to oxide capacitance and is measured using the C-V split method [Koomen 73], [Romanjek 04]. Figure 2.23 shows no significant difference in EOT between high temperature devices and low temperature devices. In addition, in both cases EOT is stable with channel length variation. This is translated in gate capacitance stability between high temperature and low temperature devices according to (2.9).

As a conclusion, the analysis carried out on this first shows that low temperature nMOS devices display a performance degradation compared to high temperature devices. This performance degradation is related to the difficulty to place active dopants in the region below the first spacer, leading to an access resistance degradation that explains the performance loss. In section 2.6 a first solution will be proposed in order to improve $R_{SPA}$ value and try to achieve high temperature device performance target.

## 2.5 Low temperature pMOS electrical results

FDSOI pMOS have been also tested. The main goal of this section is to highlight some issues related to the extraction method in use for the analysis of the electrical results. For this reason, the provided analysis cannot be considered totally reliable, but it demonstrates the necessity to develop alternative methods of characterization in some device configurations as it will be shown below.

Three different low temperature splits with different implant conditions are here analyzed in comparison with device fabricated following the process of reference that will be named high temperature devices. The total boron dose implanted for the three low temperature devices are:

- Low dose: $1x10^{15}$ at/cm$^2$;
- Medium dose: $1x10^{15}$ at/cm$^2$;
- High dose: $2.7x10^{15}$ at/cm$^2$.

In Figure 2.24 $I_{ON}$-$I_{OFF}$ trade-off comparison among high temperature and low temperature devices are shown. Performance degradation of 15% is shown for medium and high dose splits, while severe degradation of 45% is shown for low temperature low dose split.

As for nMOS case, the performance degradation can be ascribed to the access resistance degradation as reported in Figure 2.25. It is worth noticing that access resistance extraction by Y function is quantitatively complex, especially for the low temperature high dose doping in which a linear fit of the plot reported in Figure 2.25 appears approximate.

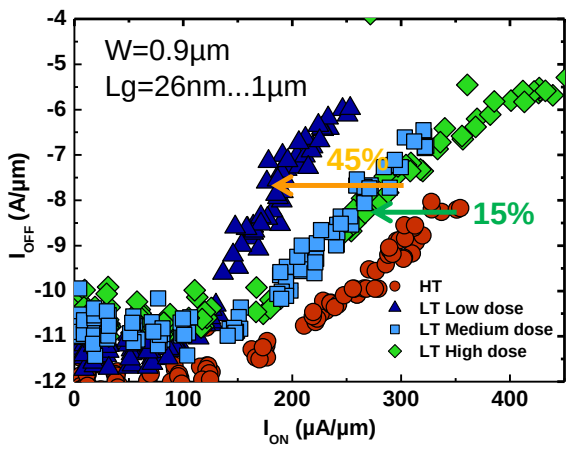



**Figure 2.24: $I_{ON}$-$I_{OFF}$ trade-off for pMOS high temperature device, considered as reference and low temperature devices. Performance degradation is shown for low temperature devices.**

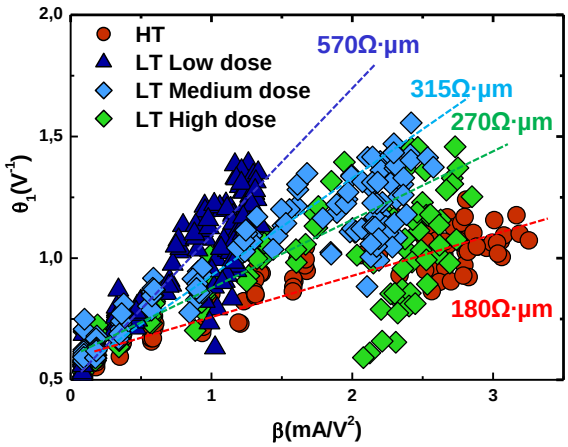



**Figure 2.25: Access resistance extraction by Y function method for high temperature and low temperature devices. The resistance values reported, correspond to the total access resistance (drain and source resistance).**

Figure 2.26 shows DIBL extraction for high temperature and low temperature devices. Contrarily than for nMOS, a significant difference between high temperature and low temperature is evidenced, especially for low temperature high dose split. Fixing a value of DIBL at 150 mv/V, a difference in electrical gate length between high temperature and low temperature device can be extracted. For L= 26 nm, $\Delta L_{HT/LT}$=8 nm.

This can be explained by a too high dopant concentration into the channel zone and an overlap configuration. The doping concentration in the region below the spacer obtained by KMC simulation is reported in Figure 2.27, 2.28 and 2.29 for the low temperature devices with low, medium and high doping dose respectively. In this case, the matching between the electrical and simulation results is not good since high overlap configuration is expected for the low temperature devices, but

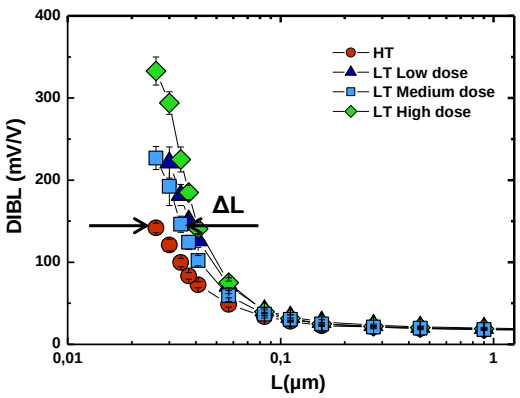



**Figure 2.26: DIBL at different gate lengths for high temperature and low temperature devices. High DIBL for low temperature devices indicates overlapped configuration.**

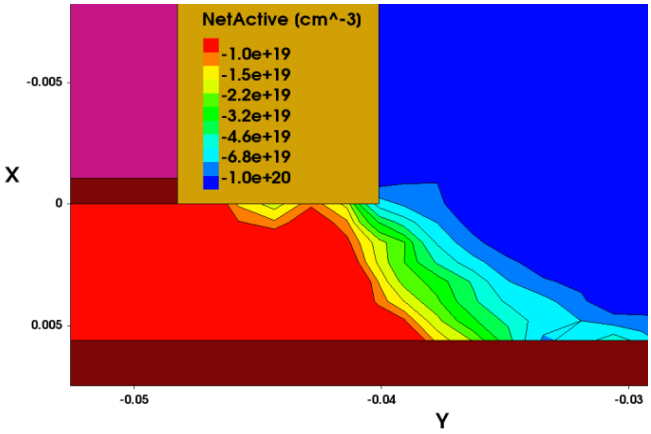



**Figure 2.27: Dopant concentration under first spacer extracted from KMC simulation for low temperature device with low doping dose.**

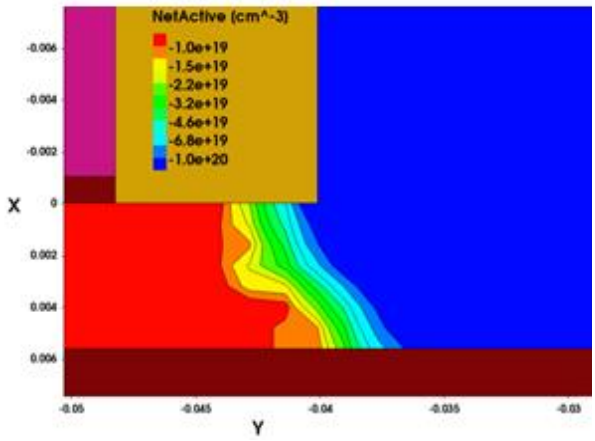



**Figure 2.28: Dopant concentration under first spacer from KMC simulation for low temperature device with medium doping dose.**

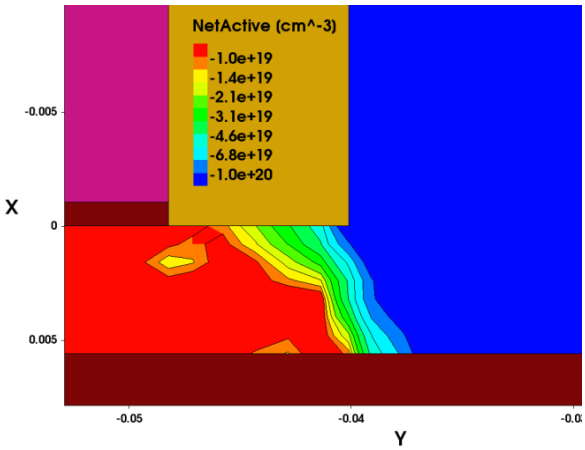



**Figure 2.29: Dopant concentration under first spacer extracted from KMC simulation for low temperature device with high doping dose.**

simulation results show that the dopant active concentration into the channel region is below $10^{19}$at/cm$^3$. This demonstrated that junction shape created by SPER in two-dimensional simulation is not completely reliable. However, interesting considerations can be extracted observing the trend of the simulation results for low temperature devices. For low dose split (Figure 2.27), the iso-concentration $10^{20}$ at/cm$^3$ is external to the first spacer and this lead to a severe degradation of $R_{SPA}$. This is consistent with the access resistance degradation shown in Figure 2.25. For medium dose (Figure 2.28) and high dose (Figure 2.29) splits, the iso-concentration $10^{20}$ at/cm$^3$ is completely below the first spacer leading to a better $R_{SPA}$ value and improving access resistance value of Figure 2.25. Iso-concentration at $10^{19}$ at/cm$^3$ for medium and low dose doping are approximately at the same place. This justifies similar DIBL for the two splits as reported in Figure 2.26. Finally, high junction abruptness degradation is shown for high dose split (Figure 2.29) in which $10^{19}$at/cm$^3$ iso-concentration is placed closer to the channel edge. This explains the higher DIBL values observed in Figure 2.26 for low temperature device with high dose. So, even though the junction position

obtained by simulation cannot be considered accurate, the split comparison can well explain the tendency found in the electrical results.

Holes mobility at low electric field is reported in Figure 2.30. Slight mobility degradation, at short channel appears for medium and high dose split compared to high temperature devices. However, correcting the gate length with the ΔL value extracted from Figure 2.26, mobility curves corresponding to the low temperature high dose and medium dose splits are now basically superposed to the high temperature split. On the contrary, severe mobility degradation, even after ΔL correction is observed for low temperature device with low dose doping. This behavior appears unusual since our work is focused on accesses region and no modification into the channel has been made. In addition, the mobility degradation appears for really long channel such as ~800 nm, where the contribution of the junctions on the carriers transport into the channel should be negligible. Since no physical phenomena seem to explain this mobility degradation at long channel, the extraction method could be inappropriate for the studied devices. The hypothesis and the limitation of the extraction method, so called Y function, are presented in the next section.

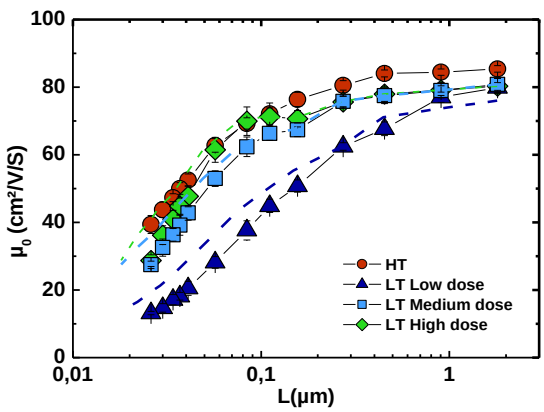



**Figure 2.30: Carriers mobility at low electric field for different gate lengths. High temperature devices and low temperature devices with medium and high dose show similar behaviors after ΔL correction. Strong degradation is shown for low temperature device with low dose split.**

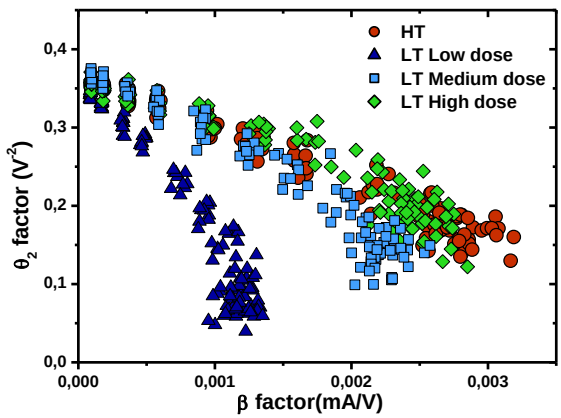



**Figure 2.31: $\theta_2$-β plot. Under the hypothesis of $R_{SD}(V_{GS})=R_0 + \lambda(V_{GS}-V_T)$, λ is represented by the slope of this graph.**

## 2.5.1 Y function method limitations

Y function [Ghibaudo88] is a standard method in use to extract carriers mobility in the inversion channel and access resistance of scaled transistors. It is based on the assumption that the drain current with a low applied drain voltage (linear regime) can be expressed by:

$$I_{DS} = \frac{\beta\, V_{gt}\, V_{DS}}{1+\theta_1 V_{gt}+\theta_2 V_{gt}^2} \tag{2.10}$$

Four fitting parameters are then used in a recursive algorithm in order to match the model with the $I_{DS}(V_{GS})$ experimental curve: the threshold voltage $V_T$, the mobility attenuation factors $\theta_1$, $\theta_2$ and $\beta$ defined as:

$$\beta = \frac{W}{L}\mu_0 C_{ox} \tag{2.11}$$

An intrinsic hypothesis of the Y function method is the linear dependence of the access resistance with the gate voltage that can be expressed as:

$$R_{SD}(V_{GS})=R_0 + \lambda(V_{GS}-V_T) \tag{2.12}$$

Where $R_0$ is the value extracted at $V_{GS}=V_T$ as in Figure 2.11 and 2.25.

Including equation (2.12) in (2.10):

$$I_{DS} = \frac{\beta\, V_{gt}\, V_{DS}}{1+\left[\theta_{1,0}+\beta\,(R_{SD0}+\lambda\, V_{th})\right] V_{gt}+\left[\theta_{2,0}+\beta\lambda\right]V_{gt}^{\,2}} \tag{2.13}$$

So, $\lambda$ can be extracted by the slope of $\theta_2$-$\beta$ plot that is shown in Figure 2.31 for the pMOS devices in course of analysis. $\lambda$ factors extracted for high temperature split and low temperature devices with high and medium dose are similar (approximately 70 Ω/V). However, for low temperature split with low doping dose, high $\lambda$ value (approximately 235 Ω/V) is extracted. The hypothesis of a linear behavior of the access resistance with the gate voltage variation deserves now a deeper focus.

Several paper in literature [Kwok 86], [Hu 87], [Kim 03], [Otten 91] discuss the effect of the gate voltage on the access resistance and a linear approximation is not always satisfying. An alternative model proposed by [Kim 02], [Monsieur 14] is:

$$R_{SD}(V_{GS}) = R_{\,0} + \frac{\sigma}{V_{GS}-V_T} \tag{2.14}$$

In particular, ~ $\frac{\sigma}{V_{GS}}$ behavior is more evident in underlap configuration. In fact, as reported in [Monsieur 14] the access resistance contribution that is strongly dependent on the applied gate voltage is the region closest to the channel ($R_{SPA}$ and $R_{OV}$ in Figure 2.12). If access resistance is strongly dependent on gate voltage, the $\frac{\sigma}{V_{GS}-V_T}$ behavior cannot be longer approximated by the linear behavior used in Y function and significant errors can arise.

Equation (2.14) has been included in (2.10) obtaining:

$$I_{DS} = \frac{\left(\frac{\beta}{1+\sigma\,\beta}\right) V_{GT}\, V_D}{1+\left(\frac{\theta_{1,0}+\beta\, R_0}{1+\sigma\,\beta}\right)V_{GT}+\left(\frac{\theta_{2,0}}{1+\sigma\,\beta}\right)V_{GT}^{\,2}} \tag{2.15}$$

Defining $B=\left(\frac{\beta}{1+\sigma\,\beta}\right)$, $\Theta 1=\left(\frac{\theta_{1,0}+\beta\, R_0}{1+\sigma\,\beta}\right)$ and $\Theta 2=\left(\frac{\theta_{2,0}}{1+\sigma\,\beta}\right)$ similar expression than equation (2.10) is obtained. In this case, the fitting parameters will be $V_T$, B, $\Theta_1$ and $\Theta_2$. It is important to remark that in this case, B depends directly on $\sigma$. So different $\sigma$ values affect directly the mobility extraction. The method has been applied for the devices under studied and the carrier mobility behavior under the hypothesis reported in (2.14) is shown in Figure 2.32. Low temperature split with high dose doping is not reported since it does not add any information to this point.

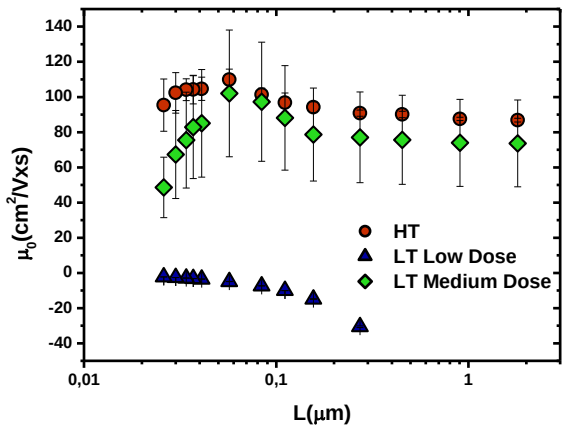



**Figure 2.32: Carrier mobility extraction considering ~$\frac{\sigma}{V_{GS}}$ behavior of the access resistance.**

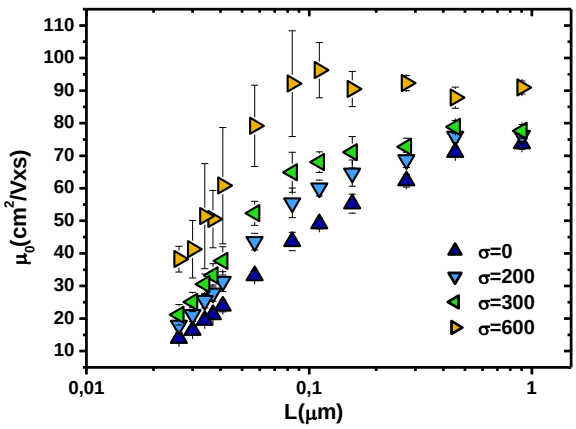



**Figure 2.33: Carrier mobility corresponding to low temperatures device with low dose doping for different values of $\sigma$.**

Figure 2.32 clearly show that the implementation of the hypothesis of ~$\frac{\sigma}{V_{GS}}$ behavior for access resistance lead to totally unattainable results (negative mobility) for low temperature device with low dose doping. For high temperature and low temperature devices with medium dose doping the mobility trend is significantly different from Figure 2.30. In particular, for high temperature devices a quasi-constant mobility with the gate length variation is found, while for low temperature split with high dose doping, a first increase of the mobility between 100 and 60 nm is observed. Finally, a severe decrease of the mobility is observed leading to a significant difference of the short channel mobility compared to the high temperature split. This difference is more pronounced compared to the results presented in Figure 2.30. It has been demonstrated that different hypothesis on the behavior of access resistance with the applied gate voltage can lead to difference in mobility extraction. This point highlights the unsuitability of Y function method for quantitative and satisfying electrical analysis of the devices in use. A new method has to be implemented considering the different configuration of the device (overlap/underlap) and the corresponding behavior of the access resistance with the applied gate voltage. As an example, in Figure 2.33 is reported the carrier mobility behavior for different $\sigma$ values in the case of access resistance ~$\frac{\sigma}{V_{GS}}$. Increasing the $\sigma$ value, the degradation mobility arises for smaller channel lengths. For $\sigma$=300 even the short channel mobility value is not degraded compared to the medium dose split reported in Figure 2.30. However, it has been demonstrated that extracting the correct value ($\sigma$ =6380) the extraction method completely fails, providing negative values of the mobility. This probably suggests that $\frac{\sigma}{V_{GS}}$ behavior for the access resistance is present but cannot completely represent the reality and a more complex model has to be defined. Since an exhaustive modeling work is out of the purpose of this activity, this point has to be addressed by a new study.

## 2.6 LT FDSOI device optimization

In section 2.4 and 2.5 the region below the first spacer has been identified as critical for low temperature device optimization due to the difficulty of positioning active dopants. This conclusion has been made on a first 28 nm lot, called thereafter Lot 1.

In order to increase the dopant concentration below the first spacer, a first idea is to increase the amorphization depth and to increase the implantation tilt. This solution is implemented in the low temperature devices in a second FDSOI lot (Lot 2). For low temperature devices two different tilt angle implantations have been tested for nMOS (15° and 25°) while for pMOS tilt 7° has been chosen. For the process of reference, the tilt is 15° and 7° for nMOS and PMOS respectively.

Low temperature nMOS device TEM observation is shown in Figure 2.34.

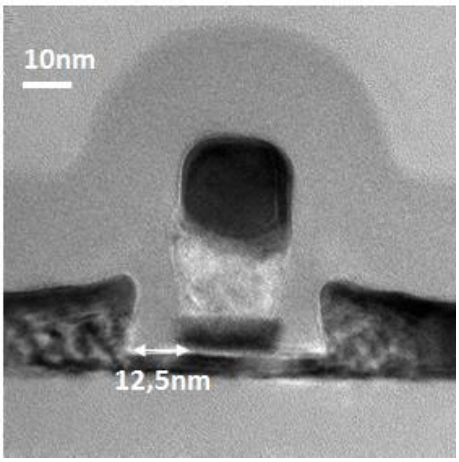



**Figure 2.34: TEM cross section of a tested low temperature FDSOI device.**

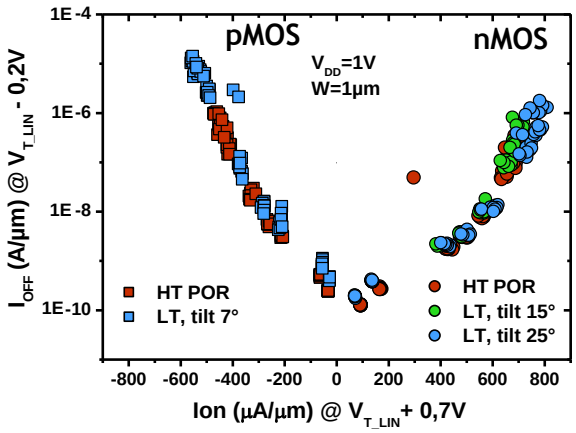



**Figure 2.35: Normalized $I_{ON}$.$I_{OFF}$ performance of LT FDSOI N- & P-devices compared with HT-POR, for different implantation tilt angle.**

The $I_{ON}$ - $I_{OFF}$ comparison between high temperature and low temperature device for both nMOS and pMOS is shown in Figure 2.35. In this case, low temperature devices achieve high temperature performance. It is worth noticing that the performance of the high temperature reference values is not so elevated ($I_{ON}$=800 µA/µm at $I_{OFF}$=$10^{-7}$ µA/µm for nMOS) compared to the state of art technology and are clearly degraded compared to lot 1 values (see Figure 2.36). This is explained by a too thick first spacer dimension which is measured at 12.5 nm (Figure 2.37) while it should be around 8 nm. This undesired morphological variation leads to strong underlap configuration ($R_{SPA}$ degradation) and then $I_{ON}$ reduction compared to the process of reference expected value. Since the first spacer thickness impact in the same way high temperature and low temperature devices, it can be concluded that high temperature and low temperature devices show similar $I_{ON}$-$I_{OFF}$ trade-off.

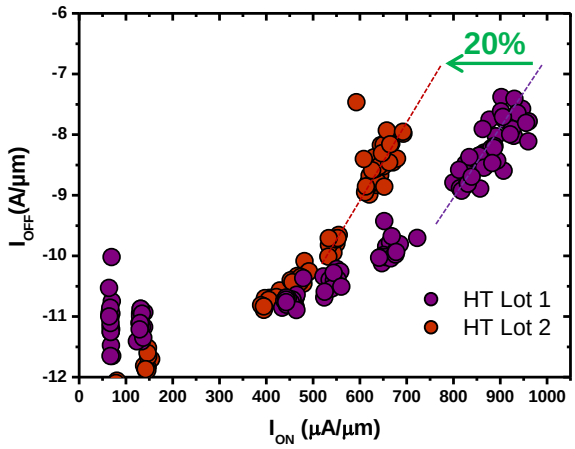



**Figure 2.36: Comparison of lot 1 and lot 2 nMOS performance for the HT reference.**

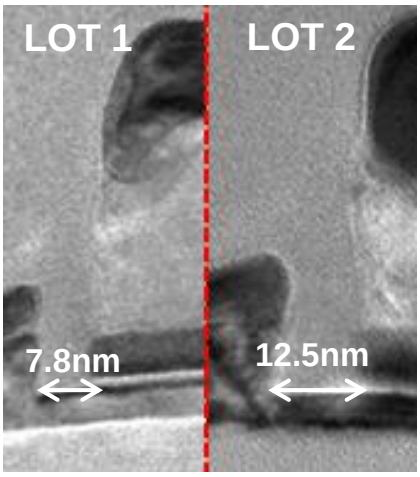



**Figure 2.37: TEM cross section of high temperature device for lot 1 and lot 2. The difference in first spacer thickness is highlighted.**

In Figure 2.38, $I_{ON}$-$I_{OFF}$ performance benchmark of low temperature planar devices with literature data is shown. The benchmark highlights that low temperature nMOS device outperforms the low temperature literature reference and pMOS is in the same performance range. In this benchmark SPER activated devices, junctionless and Schottky devices have been considered.

The discussion will be now carried out considering nMOS devices only. However, all the conclusions can be extended to pMOS, similarly to the discussion of section 2.5. In Figure 2.39 the $R_{ON}$-DIBL trade-off is shown for different gate lengths. In this figure, it is observed that low temperature devices with tilt 25° reach the high temperature reference $R_{ON}$ value but a DIBL degradation appears. While for low temperature devices with tilt 15°, $R_{ON}$ is higher than the POR value, but better DIBL than tilt 25° case is obtained. It is likely that the increase of tilt implantation leads to a better access resistance (in particular $R_{SPA}$ contribution) due to high dopant concentration below the first spacer, but this higher tilt also leads to a junction abruptness degradation. The abruptness degradation can be observed by simulation results shown in Figure 2.40. For high temperature split, one-decade variation ($10^{19}$-$10^{20}$ at/cm$^3$) in active doping concentration is distributed in approximately 4 nm from the channel edge below the spacer. For low temperature devices, the same concentration range is distributed along 8 nm below the spacer. The abruptness degradation is electrically translated into a DIBL degradation.

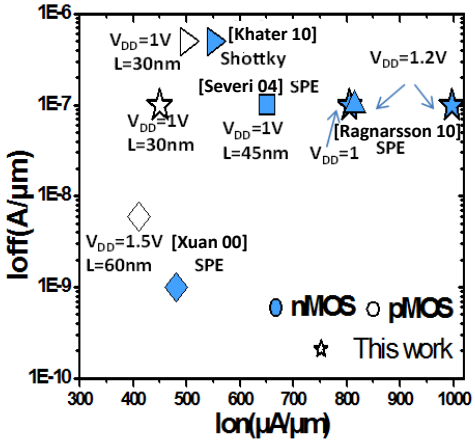



**Figure 2.38: $I_{ON}$-$I_{OFF}$ performance benchmark of LT planar devices with literature data (all LT activation methodologies confounded).**

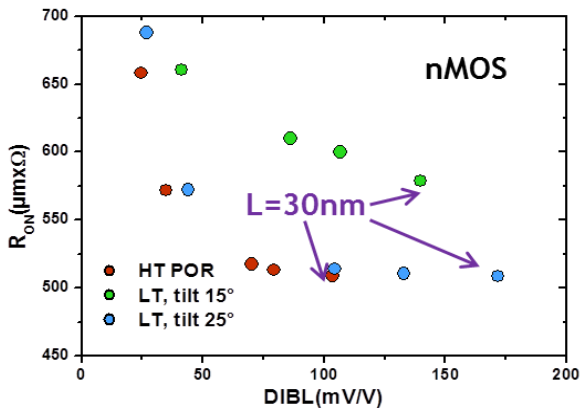



**Figure 2.39: $R_{ON}$ - DIBL measurements for high temperature and low temperature nMOS devices.**

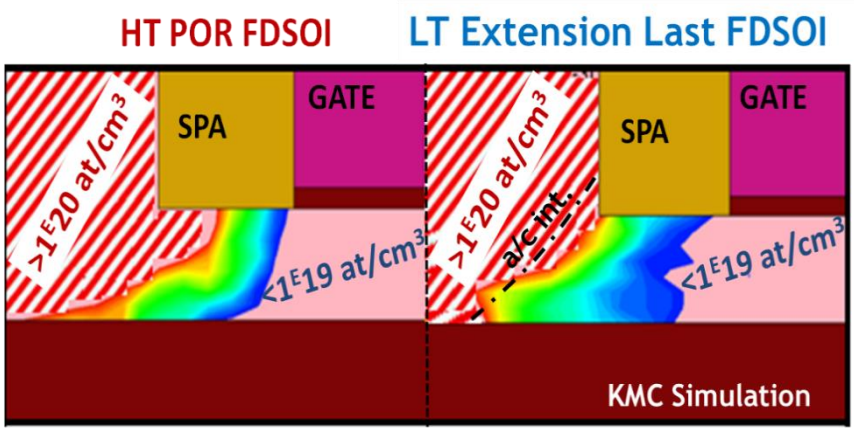



**Figure 2.40: Junction simulation by SPROCESS KMC.**

Moreover, for tilt 25° devices with implant conditions chosen (9 KeV, $1x10^{15}$at/cm$^3$), a full film amorphization is reached. In fact, It is schematically reported in Figure 2.40 that the amorphous/crystalline interface, extracted by KMC simulation touches the BOX. Full access amorphization can generate two consequences:

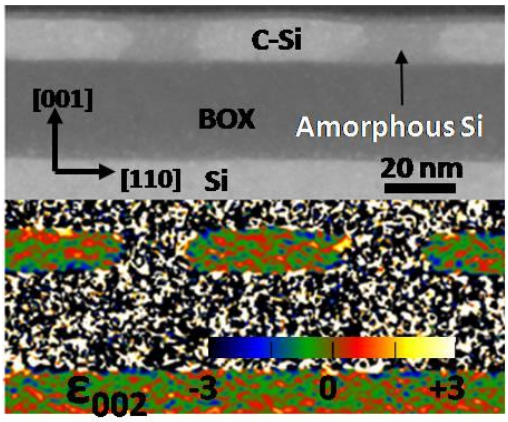



**Figure 2.41: TEM micrograph and a map of the out-of-plane component of strain on patterned sSOI substrate.**

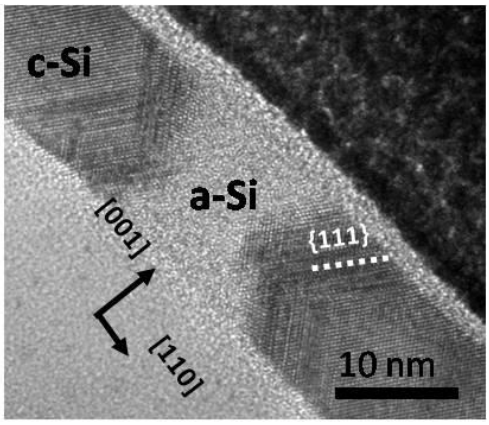



**Figure 2.42: TEM cross section showing lateral recrystallization at 550°C after patterned full film amorphization. Defective {111} recrystallization is observed.**

- **Strain relaxation**: Figure 2.41 shows TEM micrograph and a map of the out-of-plane component of strain obtained by geometrical phase analysis of a patterned sSOI wafer after full-depth film amorphization. Total relaxation of the strain in the implant-protected crystalline regions is observed. Strain relaxation is not compatible with advanced technological nodes, where strain boosters are included, for instance SiGe channel for pMOS in 14 nm FDSOI technology (the details of this technology will be presented in chapter three). However, this result has been obtained without taking into consideration the real structure of an electrical device in which the presence of the gate stack could introduce a shadowing effect during the implantation. As a consequence, a part of the crystalline seed could be preserved as well as the strain.
- **Defective re-crystallization**: In Figure 2.42 TEM cross section shows lateral recrystallization at 550 °C after patterned full film amorphization. Defective {111} recrystallization is observed

This integration scheme, in which the dopants are introduced into the access region after the raise source and drain epitaxial step, so called extension last ($X^{last}$) presents issues in both cases of partial or full amorphization. For partial amorphization, high active dopant concentration cannot be placed in the region below the first spacer leading to $R_{SPA}$ value degradation. Full amorphization leads to a defective lateral re-crystallization and strain relaxation that is not compatible with advanced technological nodes. Another integration scheme called extension first ($X^{1st}$) [Ponoth 11], in which the implantation step is made before the raised source and drain epitaxial growth is then proposed. In Table 2.1 are reported the pro and cons of the three integration schemes. For extension first the implantation can be made through a nitride capping liner. However, details about the extension first process flow will be discussed in chapter three.

## 2.7 Comparison of extension first and extension last integrations

In previous chapter some drawbacks of the use of extensions last integration have been mentioned. Extension first integration appears as an alternative solution. Comparing the two integration schemes another substantial difference arises in the definition of the amorphous/crystalline (a/c) interface.

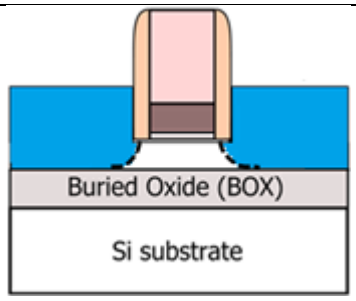
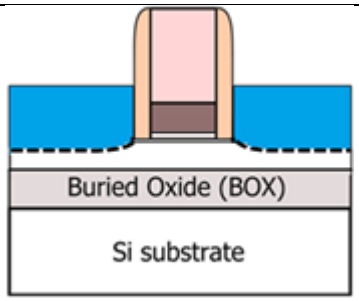
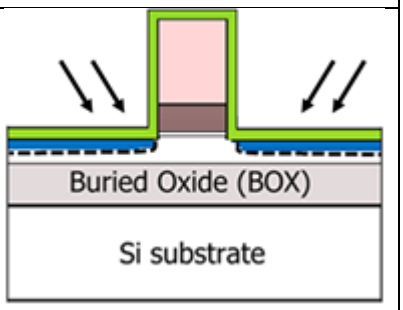
| **Extension Last ($X^{last}$), full amorphization** | **Extension Last ($X^{last}$), partial amorphization** | **Extension First ($X^{1st}$), partial amorphization** |
|---|---|---|
|  |  |  |
| Higher dopant concentration below spacer | Strain channel retention | Strain channel retention |
| Strain channel relaxation | Vertical re-crystallization | Vertical re-crystallization |
| Defective Lateral crystallization | No dopants below spacer | Higher dopant concentration below spacer |

**Table 2. 1: Summary of the advantages and disadvantages for $X^{last}$, full amorphization, partial amorphization and $X^{1st}$ integration.**

After the implant, the amorphous/crystalline interface is not sharp, but it shows a morphological spatial variation defined as roughness. A 3D simulation of the a/c interface roughness is shown in Figure 2.43. Simulation results show that the a/c roughness interface increases with the amorphization depth. This is valid for low temperature and room temperature implantations and for both germanium and phosphorus amorphization (Figure 2.44). Thus, the amorphization depth is higher for extension last than extension first integration in which a better control of the a/c interface roughness is possible and a thinner silicon seed can be achieved. It is important to keep in mind that the validity of these simulations results is not quantitatively demonstrated, but it shows a trend that can be used in the choice of the integration scheme.

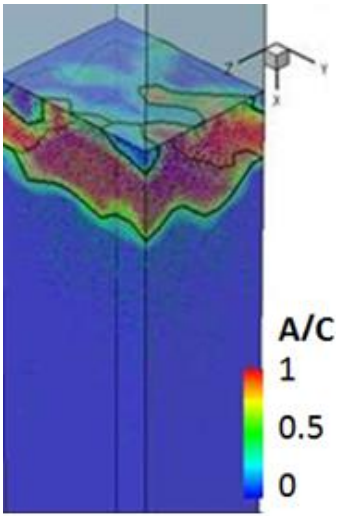



**Figure 2.43: Example of the amorphous/crystalline interface after dopant implantation obtained by 3D simulation.**

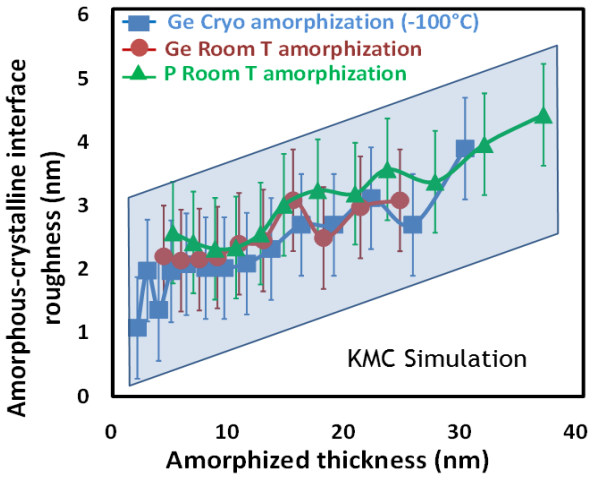



**Figure 2.44: Amorphous-crystalline interface roughness estimation versus amorphized thickness for different species (Ge and P) extracted by SPROCESS KMC simulation.**

Another point, concerning the extension last integration only, is related to the intrinsic variability of the raised source and drain epitaxial thickness. Epitaxy process is very sensitive to the density of pattern that leads to epitaxy thickness variation between large and narrow width or dense SRAM. Epitaxy variability is also dependent on the position on the wafer map. The epitaxy thickness range variation can be considered ±1.5 nm. Such thickness variability can lead to devices with partial or full amorphization and it appears evident that the definition of implant conditions using the extension last scheme is not suitable for a robust process. Considering both a/c interface roughness and raised source and drain thickness variability the minimum thickness seed ($T_{SEEDMIN}$) that allows partial amorphization can be defined as:

$$T_{SEEDMIN} = \sqrt{{T_{ROUGH}}^2 + {\Delta T_{EPI}}^2} \tag{2.16}$$

In Table 2.2, the minimum thickness seed values for FDSOI devices in case of both extension last and extension first integrations calculated by means of equation 2.11.

| Architecture | $T_{ROUGHNESS}$ | $\Delta T_{EPI}$ | $T_{SEED, MIN}$ |
|---|---|---|---|
| **FDSOI $X^{1st}$** | ≈3 nm (amo 3 nm out of 6 nm) | NA | **≈3 nm** |
| **FDSOI $X^{last}$** | ≈4 nm (amo 18 nm out of 22 nm) | 1.5nm | **≈4.3 nm** |

**Table 2. 2: Minimum thickness seed calculation for extension last and extension first integrations.**

### 2.7.1 $R_{SPA}$-$T_{SEED}$ trade-off

In the previous analysis two important parameters have been identified for the low temperature FDSOI optimization: $R_{SPA}$ value and $T_{SEEDMIN}$. Both of them have to be satisfied: the first one, to enable a good value of access resistance and therefore ON current; the second one to guarantee a crystalline seed that allow vertical re-crystallization during dopant activation by SPER. A figure of merit $R_{SPA}$-$T_{SEED}$ is reported in Figure 2.45, in order to visualize directly which implant conditions for extension last integration scheme can satisfy both criteria. Each point corresponds to a different implant condition. $R_{SPA}$ values have been extracted by means of device simulation while $T_{SEED}$ have been extracted by process simulations. The acceptable process window (white region) corresponds to the point with $R_{SPA}$<MAX $R_{SPA}$ and $T_{SEED}$>$T_{SEEDMIN}$. The maximum $R_{SPA}$ value, has been chosen at 30 Ωxμm corresponding to the $R_{SPA}$ value of high temperature device fabricated with the process of reference. $T_{SEEDMIN}$ has been calculated by equation (2.16). It is worth noticing that $T_{SEEDMIN}$ has two different values for the two integration schemes extension last and extension first, according to the difference values of roughness and thickness variability.

It can be observed that no extension last conditions can satisfy both criteria of $R_{SPA}$ and minimum seed thickness. As shown by electrical results, the only way to approach the $R_{SPA}$ target is the full amorphization of the access region, but this last configuration is not compatible for the advanced nodes as reported in section 2.6. For extension first integration (Figure 4.46), a process window satisfying both criteria can be found.

$R_{SPA}$ values have been extracted using SDEVICE simulation applying the gate electrode a voltage $V_{GS}$=$V_T$+0.7 V.

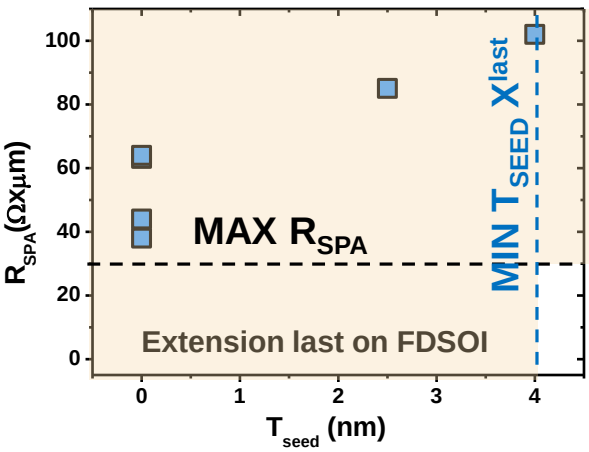



**Figure 2.45: $R_{SPA}$-$T_{SEEDMIN}$ trade-off for FDSOI device at low temperature with extension last integration.**

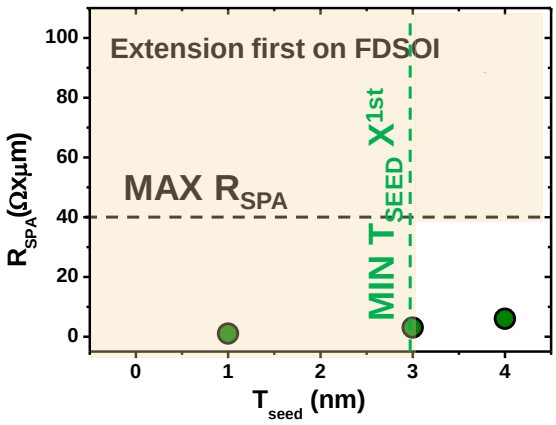



**Figure 2.46: $R_{SPA}$-$T_{SEEDMIN}$ trade-off for FDSOI device at low temperature with extension first integration.**

It can be concluded that the only acceptable integration scheme for low temperature FDSOI optimization is the extension first. In Figure 2.47 junction comparison obtained by simulation between extension last and extension first integration scheme is shown. This figure evidenced how easier it is to position dopants below the first spacer using the extension first scheme and obtain a significant

improvement of $R_{SPA}$ value compared to the extension last option. Moreover, since the extension first scheme is independent from the raised source and drain thickness variability and the a/c interface roughness is smaller, partial amorphization conditions can be defined, preserving channel strain retention as described in section 2.6.

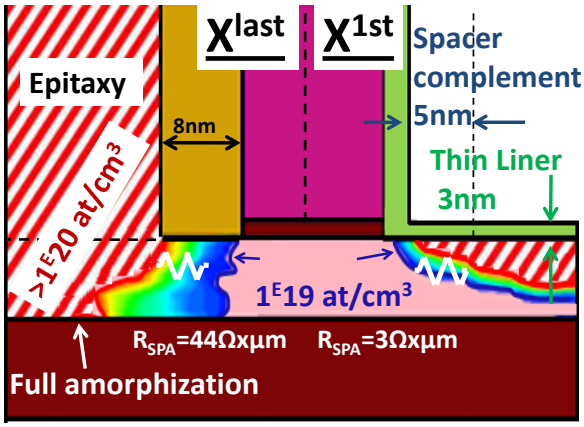



**Figure 2.47: KMC simulation of junction profile for extension last and extension first integration.**

## 2.8 Low temperature TriGate: electrical results and optimization

CoolCube integration is not strictly limited to the case of FDSOI devices. Different architectures of device can be stacked. Obviously, the limited thermal budget of the top transistor still has to be satisfied. In this paragraph, electrical results of TriGate transistors, where the dopant activation have been made by low temperature SPER are presented. Optimization guidelines are provided as well.

### 2.8.1 TriGate devices

TriGate transistor can be roughly considered as a SOI transistor with very small W dimension. This means that TriGate is no longer a planar device as SOI, but a three-dimensional device. A schematic 3D representation of a TiGate devices is reported in Figure 2.48.

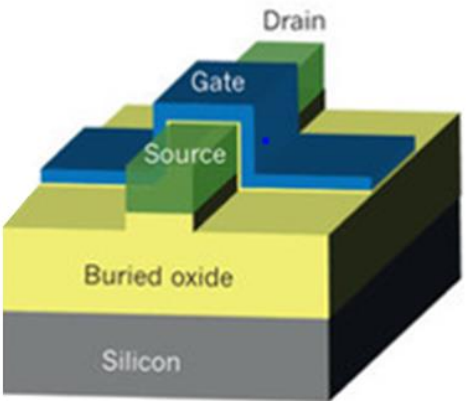



**Figure 2.48: 3D representation TriGate on insulator device.**

The tested devices proposed in this work have a W=15 nm. Another significant difference is the channel thickness which is is 6 nm and approximately 15 nm for TriGate. Some details of the process flow and electrical results of TriGate devices fabricated at LETI can be found in [Coquand 13]. The schematic representations of FD, TriGate and FinFET on insulator devices are reported in Figure 2.49 with the corresponding film thickness. The very small width dimension can lead to uncertain $I_{ON}$ extraction, since this value is usually proposed per area unit. In fact, a small width variation leads to a high variation of $I_{ON}/W$ ratio that can provide totally unreliable results. It is then mandatory to measure the dimensions of the width for each tested device, in order to avoid any error in the performance results. TEM observations of a TriGate device are reported in Figure 2.50a and 2.50b in the direction of the channel length and of the device width respectively.

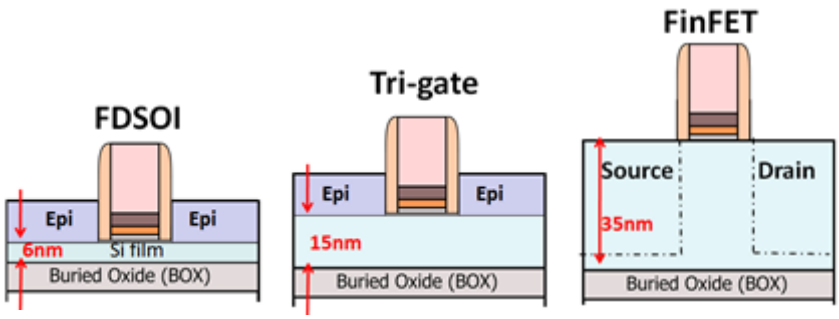



**Figure 2.49: Schematic representation of FD, TriGate and FinFet on insulator geometries.**

For TriGate devices, the width dimension is comparable with the gate height ($H_{NW}$), so the electrostatic control occurs in three dimensions. W normalization can be done considering or not the gate height. In the first case the width is defined as an effective width $W_{EFF}= W_{TOP} + 2xH_{NW}$. This takes into account the conduction of the TriGate edges. This first parameter enables to fairly compare the performance of a device. In the second case, the width is considered to be equal to the top transistor width neglecting the gate edges, so $W_{TOT}=W_{TOP}$. The normalization with $W_{TOP}$ allows to compare different device performance with the focus on the footprint of the device.

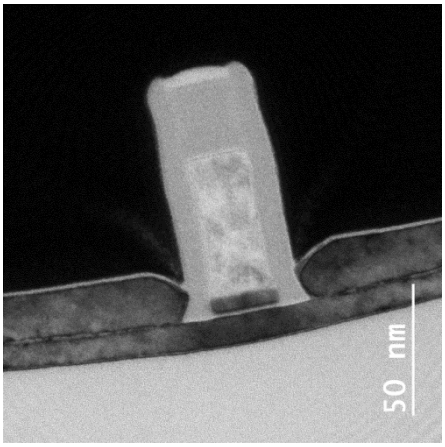



**Figure 2.50a: TEM cross section of low temperature TriGate device.**

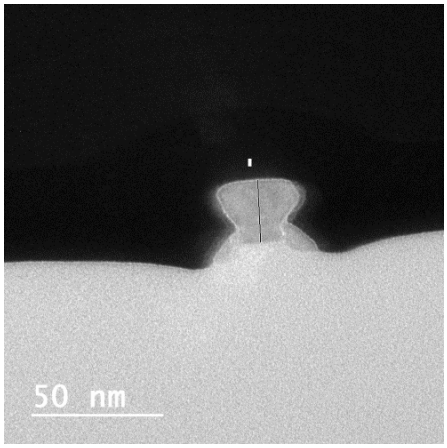



**Figure 2.51b: TEM cross section in lateral direction of low temperature TriGate device.**

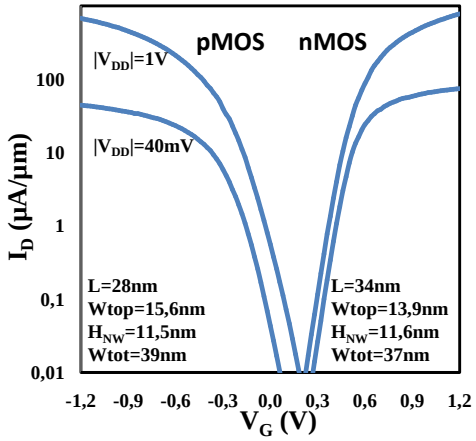



**Figure 2.51: $I_D$-$V_G$ characteristics of low temperature N&P-TriGate with extension last normalized by $W_{EFF}$= $W_{TOP}$+2×$H_{NW}$.**

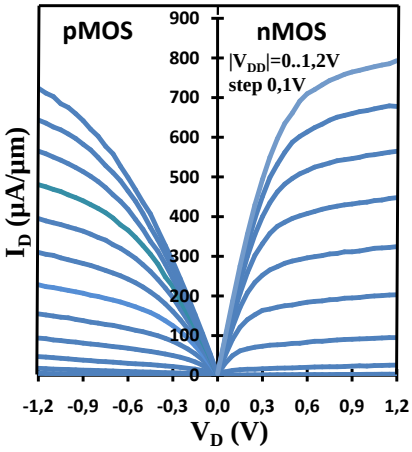



**Figure 2.52: $I_D$-$V_D$ characteristics of low temperature N&P-TriGate with extension last integration normalized by $W_{EFF}$= $W_{TOP}$+2×$H_{NW}$.**

Well-behaved $I_{DS}(V_{GS})$ (Figure 2.51) and $I_{DS}(V_{DS})$ (Figure 2.52) characteristics as well as very good $I_{ON}$-$I_{OFF}$ trend have been reached for both N&P- LT- TriGate considering width normalization with the full effective width $W_{EFF}$= $W_{TOP}$+2×$H_{NW}$. With $W_{TOP}$ only normalization, these devices would even reach $I_{ON}$=1320 µA/µm, $I_{OFF}$ =560 nA/µm for PMOS and $I_{ON}$ =1480 µA/µm, $I_{OFF}$ =0.055 nA/µm for nMOS at $V_{DD}$=1 V.

In Figure 2.53, $I_{ON}$-$I_{OFF}$ performance benchmark of low temperature TriGate with literature data is shown. The benchmark highlights that both nMOS and pMOS low temperature devices outperforms the low temperature literature reference.

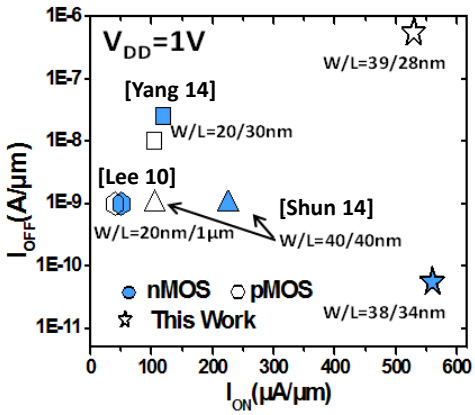



**Figure 2.53: $I_{ON}$-$I_{OFF}$ performance benchmark of low temperature TriGate N&P devices with literature data. $W_{EFF}$ normalization used for this work.**

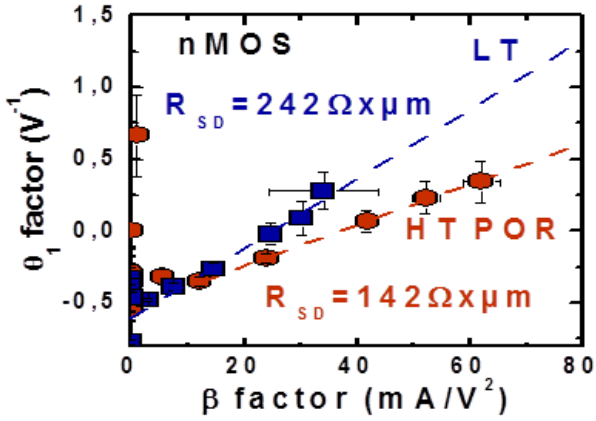



**Figure 2.54: Experimental extraction of access resistance for high temperature and low temperature TriGate devices.**

Figure 2.54 shows that the access resistance of low temperature is degraded compared to the access resistance of high temperature process of reference device. In fact, the total access resistance value is 142 Ωxµm for the high temperature device against 242 Ωxµm for low temperature device. Figure 2.55 showing KMC-simulated junction shapes underlines that in the high temperature devices, similarly than for FDSOI, diffusion drives the dopants in the critical region below the spacer, while in the low temperature device, the diffusion-less SPER activation and the efficient activation spatial restriction to the amorphized region lead to weak activation within the critical region below the offset spacer.

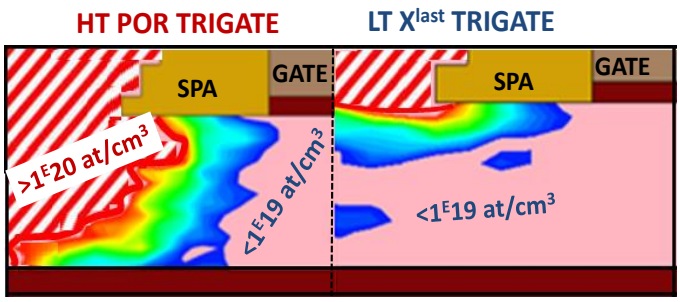



**Figure 2.55: Junction simulation by SPROCESS KMC for HT/LT Trigate devices.**

In conclusion, low temperature TriGate devices suffer the same issue than FDSOI devices: the difficulty of placing high active dopant concentration in the region below the first spacer. Similar to what presented for FDSOI, the figure of merit $R_{SPA}$-$T_{SEEDMIN}$ can be plotted for TriGate. The figures of merit are shown in Figure 2.56 and 2.57 for extension last and extension first integration respectively.

For TriGate devices, the points corresponding to extension last integration with full amorphization satisfy $R_{SPA}$ criteria. This is due to the thicker channel dimension than FDSOI and the possibility to have thicker zone with acceptable active dopant concentration below the first spacer. However, no process window can be defined in which both $R_{SPA}$ and $T_{SEEDMIN}$ criteria are respected. As for FDSOI, only $X^{1st}$ integration fulfills both $R_{SPA}$ and $T_{SEEDMIN}$ criteria.

The study has been extended to low temperature FinFET device. FinFET can be considered as a TriGate with a thicker channel film and gate height (Figure 2.48). In FinFET fabrication we considered that no raised source and drain epitaxies, so it does not make sense to talk about extension first or extension last integration scheme. Usually a recess is made on the semiconductor film and epitaxial in-situ doped is grown in order to create the access region. High temperature drive-in is performed to position active dopant in the region below the spacer. Since the drive-in anneal, usually performed at temperatures higher than 1000 °C, is not compatible with the low temperature process, an implantation step is necessary. In Figure 2.58 $R_{SPA}$-$T_{SEED}$ trade-off is shown for FinFET device, where the implantation step has been simulated before the recess creation, so when the film is 35 nm thick (Figure 2.48). The simulations show that there is a process window that satisfies both criteria of $R_{SPA}$ and minimum seed thickness.

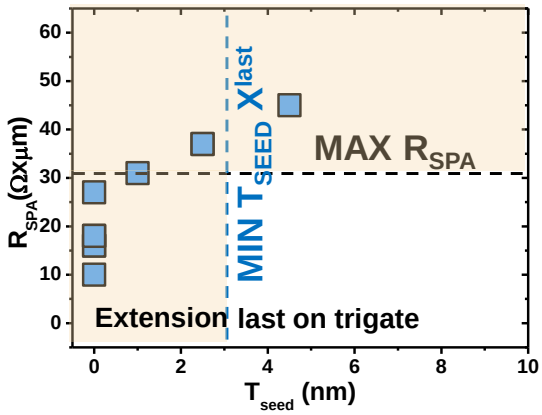



**Figure 2.56: TriGate low temperature junction figure of merit: $R_{SPA}$-$T_{SEED\ MIN}$ trade-off for extension last scheme.**

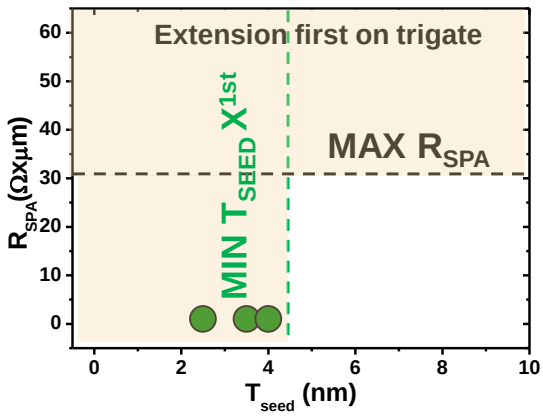



**Figure 2.57: TriGate low temperature junction figure of merit: $R_{SPA}$-$T_{SEED\ MIN}$ trade-off for extension first scheme.**

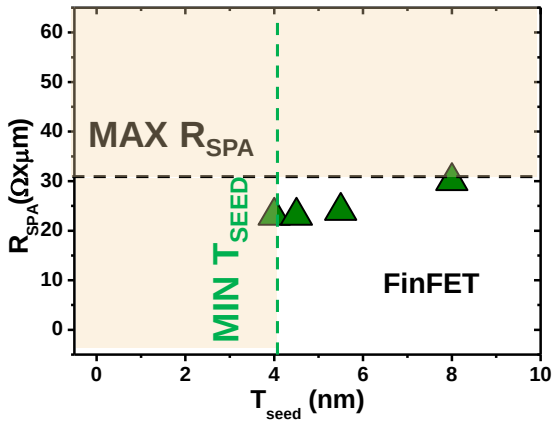



**Figure 2.58: FinFET low temperature junction figure of merit: $R_{SPA}$-$T_{SEED\ MIN}$ trade-off for.**

Regarding the challenge of low temperature junctions optimization, it can be concluded that FinFET is a promising candidate for CoolCube technology since no physical limit are evident in the achievement of $R_{SPA}$ target can be reached without the risk of a full amorphization post implantation.

## 2.9 Conclusion of the chapter

In this chapter, a detailed electrical characterization, supported by simulation results has been carried out on FDSOI devices activated at low temperature and fabricated with the extension last integration scheme.

First of all, the dopant condition optimized in chapter one have been used in the electrical devices. Best low temperature nMOS device shows a 20% of performance degradation compared to the process of reference which is attributed to access resistance degradation. Both process and device simulations show that the access resistance degradation can be mainly explained by the difficulty to place dopants in the region below the first spacer that leads to a degradation of the resistance component of that region, so named $R_{SPA}$.

pMOS device show similar results, with an anomalous carrier mobility degradation arising from long channel length for some splits. This appears more related to a bad extraction parameter by a method that is not suitable for device in underlap configuration.

A first idea to improve the dopant concentration below the first spacer, is to increase the amorphization depth and to increase the implantation tilt. With this modified implant conditions, low temperature devices achieved comparable performance with the process of reference, but with degradation of the DIBL, which was even more evident in pMOS devices. Moreover, the used implantation conditions lead to a full amorphization of the film and the re-crystallization has been obtained using the lateral direction. This leads to defective re-crystallization and strain retention, non-compatible with advanced node.

The most adapted integration scheme to use for FDSOI optimization fabricated at low temperature has been chosen defining two criteria: maximum $R_{SPA}$, corresponding to the resistance of the region below the first spacer of the process of reference; minimum crystalline seed that allows partial amorphization considering the amorphous/crystalline interface roughness and the thickness variability of the raised source and drain. Following these two criteria, the most adapted integration scheme is the extension first, in which the dopant implantation is made before the epitaxy of the raised source and drain.

TriGate device fabricated at low temperature using the extension last integration scheme have been characterized as well. Working devices have been obtained and, once again, the degradation compared to the process of reference can be explained by the not sufficient dopant concentration below the first spacer. The $R_{SPA}$-$T_{SEED}$ criteria shows that, also for TriGate, the most adapted integration scheme is the extension first.

The study has been extended to FinFET devices, where, simulation results show that both $R_{SPA}$ and $T_{SEED}$ criteria can be satisfied and FinFET architecture appears to be a promising candidate for CoolCube integration.

## References


[Arnaud 15] Arnaud, F. "Enhanced low voltage digital & analog mixed-signal with 28nm FDSOI technology." *SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2015 IEEE*. IEEE, 2015.

[Chang 07] Y. Chang, Y. Wu, and C. Ho, "A simple method to extract source/drain series resistance for advanced MOSFETs," in Proc. 37th ESSDERC, Dec. 2007, pp. 87–90.

[Charbonnier 10] Charbonnier, Matthieu, et al. "Measurement of dipoles/roll-off/work functions by coupling CV and IPE and study of their dependence on fabrication process."*Electron Devices, IEEE Transactions on* 57.8 (2010): 1809-1819.

[Coquand 13] Coquand, R., et al. "Scaling of high-κ/metal-gate TriGate SOI nanowire transistors down to 10nm width." *Solid-State Electronics* 88 (2013): 32-36.

[Fenouillet 13] Fenouillet, C. 2013. Le FDSOI de la physique du dispositif à l'intégration d'une technologie compétitive.

[Fleury 09] Fleury Dominique, et al. "A new technique to extract the source/drain series resistance of MOSFETs." *Electron Device Letters, IEEE* 30.9 (2009): 975-977.

[Ghibaudo 88] Ghibaudo, Gérard. "New method for the extraction of MOSFET parameters."*Electronics Letters* 24.9 (1988): 543-545.

[Golanski 13] Golanski, Dominique, et al. "First demonstration of a full 28nm high-k/metal gate circuit transfer from bulk to utbb fdsoi technology through hybrid integration." *VLSI Technology (VLSIT), 2013 Symposium on*. IEEE, 2013.

[Hu 87] Hu, Genda J., Chi Chang, and Yu-Tai Chia. "Gate-voltage-dependent effective channel length and series resistance of LDD MOSFET's." *Electron Devices, IEEE Transactions on* 34.12 (1987): 2469-2475.

[Khater 10] Khater, Marwan H., et al. "High-/Metal-Gate Fully Depleted SOI CMOS With Single-Silicide Schottky Source/Drain With Sub-30-nm Gate Length." *Electron Device Letters, IEEE* 31.4 (2010): 275-277.

[Kim 02] Kim, Seong-Dong, Cheol-Min Park, and Jason Woo. "Advanced model and analysis of series resistance for CMOS scaling into nanometer regime. I. Theoretical derivation." *Electron Devices, IEEE Transactions on* 49.3 (2002): 457-466.

[Kim 02] Kim, Seong-Dong, Cheol-Min Park, and Jason Woo. "Advanced model and analysis of series resistance for CMOS scaling into nanometer regime. II. Quantitative analysis." *Electron Devices, IEEE Transactions on* 49.3 (2002): 467-472.

[Kim03] Kim, D. M., H. C. Kim, and H. T. Kim. "Modeling and extraction of gate bias-dependent parasitic source and drain resistances in MOSFETs." *Solid-State Electronics* 47.10 (2003): 1707-1712.

[Koomen 73] Koomen, Jan. "Investigation of the MOST channel conductance in weak inversion." *Solid-State Electronics* 16.7 (1973): 801-810.

[Kwok 86] Ng, Kwok K., and William T. Lynch. "Analysis of the gate-voltage-dependent series resistance of MOSFET's." *Electron Devices, IEEE Transactions on* 33.7 (1986): 965-972.

[Lee 10] Lee, Chi-Woo, et al. "High-temperature performance of silicon junctionless MOSFETs." *Electron Devices, IEEE Transactions on* 57.3 (2010): 620-625.

[Monsieur 14] Monsieur F., et al. "The importance of the spacer region to explain short channels mobility collapse in 28nm Bulk and FDSOI technologies." *Solid State Device Research Conference (ESSDERC), 2014 44th European*. IEEE, 2014.

[Otten 91] Otten, J. A. M., and F. M. Klaassen. "Determination of the gate-voltage dependent series resistance and channel length in sub micron LDD-MOSFETs." *Solid State Device Research Conference, 1991. ESSDERC'91. 21st European*. IEEE, 1991.

[Ponoth 11] Ponoth, S., et al. "Implant approaches and challenges for 20 nm node and beyond ETSOI devices." *IEEE International SOI Conference (SOI)*. Vol. 1. 2011.

[Ragnarsson06] Ragnarsson, Lars-Åke, et al. "Electrical characteristics of 8-/spl Aring/EOT HfO/sub 2//TaN low thermal-budget n-channel FETs with solid-phase epitaxially regrown junctions." *Electron Devices, IEEE Transactions on* 53.7 (2006): 1657-1668.

[Romanjek 04], Romanjek K., et al. "Improved split CV method for effective mobility extraction in sub-0.1-µm Si MOSFETs." *Electron Device Letters, IEEE* 25.8 (2004): 583-585.

[Sakurai06], Takayasu, Akira Matsuzawa, and Takakuni Douseki. *Fully-depleted SOI CMOS circuits and technology*. Springer, 2006.

[Severi 04] Severi, Simone, et al. "Diffusion-less junctions and super halo profiles for PMOS transistors formed by SPER and FUSI gate in 45 nm physical gate length devices." *Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International*. IEEE, 2004.

[Shen 13] Shen, Chang-Hong, et al. "Monolithic 3D chip integrated with 500ns NVM, 3ps logic circuits and SRAM." *Electron Devices Meeting (IEDM), 2013 IEEE International*. IEEE, 2013.

[Skotnicki 00], Skotnicki Thomas. *Transistor MOS et sa technologie de fabrication*. Ed. Techniques Ingénieur, 2000.

[Subramanian1 0] Subramanian, Nachiappan, G. Ghibaudo, and M. Mouis. "Parameter extraction of nano-scale MOSFETs using modified Y function method." *Solid-State Device Research Conference (ESSDERC), 2010 Proceedings of the European*. IEEE, 2010.

[Xuan 00] Xuan, Peiqi, et al. "60 nm planarized ultra-thin body solid phase epitaxy MOSFETs." *Device Research Conference, 2000. Conference Digest. 58th DRC*. IEEE, 2000.

[Yang 13] Yang, Chih-Chao, et al. "Record-high 121/62 µA/µm on-currents 3D stacked epi-like Si FETs with and without metal back gate." *Electron Devices Meeting (IEDM), 2013 IEEE International*. IEEE, 2013.

# Chapter 3: Extension First Integration

In chapter two, it has been shown that extension first integration scheme is the mostly adapted for low temperature device optimization. This is valid for FDSOI, TriGate and FinFET devices.

In this chapter, the extension first flow is presented and implemented in the fabrication of low temperature FDSOI devices with the 14 nm technology. A detailed analysis of critical process steps concerning this integration is carried out as well.

Electrical results on 14 nm FDSOI technology with extension first integration at low temperature will be finally provided.

## 3.1 Process of Reference 14nm FDSOI process flow

The 14 nm FDSOI technology proposed by STMicroelectronics presents some relevant differences in the FEOL (Front End Of Line) transistor process flow compared to the 28 nm technology discussed in section 2.3.1. The main novel features in a 14nm FDSOI transistor are:

- The introduction of SiGe (25% Ge content) channel for pMOS: it allows lowering the threshold voltage of the pMOS, which is a key parameter in advanced CMOS processes where $V_{DD}$ is reduced, and also boosting the pMOS hole mobility [Haond 15].
- The use of SiGe 35% and SiC epitaxies for pMOS and nMOS, respectively, as raised source and drain.
- The doping step made by in-situ doped epitaxy.

The flow of the process of reference for 14 nm FDSOI technology is detailed in Figure 3.1. A brief description of the main process steps is here reported:

- **Active zone definition**: 6 nm of Si or SiGe film is used for nMOS and pMOS, respectively. A strained SiGe channel (cSiGe) is selectively formed in PMOS areas by SiGe epitaxy growth followed by a Ge condensation.
- **Gate patterning:** the gate stack is made by an interlayer (different between pMOS and nMOS) used to adjust the gate workfunction, the gate dielectric, the metal gate (TiN), poly-silicon, a thin film of $SiO_2$ USG (Undoped Silicate Glass) and SiN hard mask.
- **Spacers definition and raised source drain epitaxy**: these process steps are completely different from the 28 nm FDSOI integration and they deserve deeper focus:
    - **i)** **First spacer n deposition**: a nitride of 6 nm is deposited by ALD (Atomic Layer Deposition) on both pMOS and nMOS zones.
    - **ii)** **Photo resist deposition**: pMOS zone are protected by photo resistive material.
    - **iii)** **First spacer n etching**: the nitride is selectively etched from silicon film. The remaining nitride on the gate edges represents the first spacer for nMOS.
    - **iv)** **Stripping:** the photo resist is removed.
    - **v)** **n-type epitaxy:** SiC:P epitaxy is grown on n-zones (p-zones are protected by SiN liner). A pre-bake at 700 °C, useful for surface preparation, is applied. The

epitaxial growth consisting in a cyclic etching and deposition process is performed. The process temperature is around 630 °C.

vi) **Frist spacer p deposition**: 4 nm of nitride deposition is made on both pMOS and nMOS zones.

vii) **Photo resist deposition**: nMOS zones are protected by photo resistive material.

viii) **First spacer p etching**: the nitride is selectively etched from SiGe film. The remaining nitride on the gate etching represents the first spacer for pMOS that will be thicker (around 10 nm) compared to nMOS (6 nm).

ix) **Stripping:** the photo resist is removed.

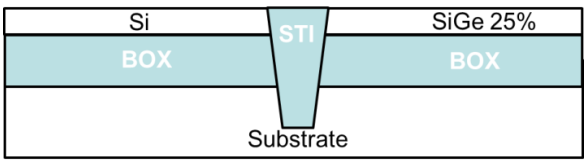
x) **p-type epitaxy:** SiGe:B epitaxy (35% Ge content) is grown on p-zones (n-zones are protected by SiN liner). SiGe:B growth is performed at 630 °C. The last ~10 nm of source and drain regions are growth with silicon epitaxy (so called silicon capping) at 700 °C. Silicon capping is used to preserve SiGe from future etching steps (such as SiN hard mask removal), since SiGe is more sensitive to nitride etching than silicon.

xi) **Nitride liner etching from n zones.**

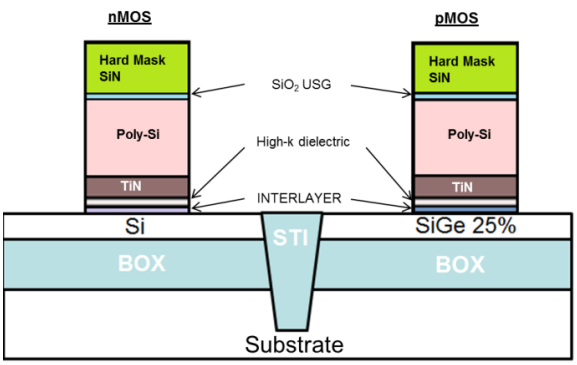
The process flow continues with the following steps:

- **Drive-in anneal:** spike annealing and DSA (Dynamic Surface Anneal) laser are used to improve dopant activation and positioning dopants below the gate spacers.
- **Hard mask removal.**
- **Salicidation**: NiPt15% is used as silicide alloy.
- **Metal contacts and BEOL**.

1) Active zone definition

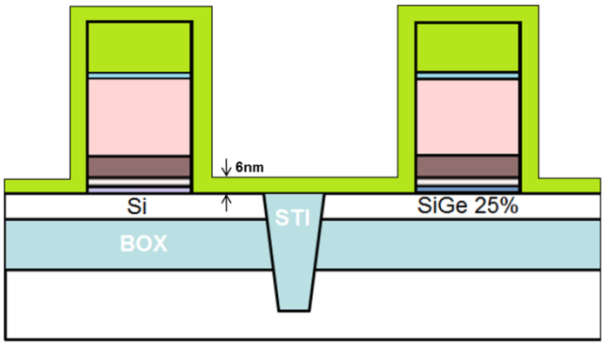



2) Gate patterning

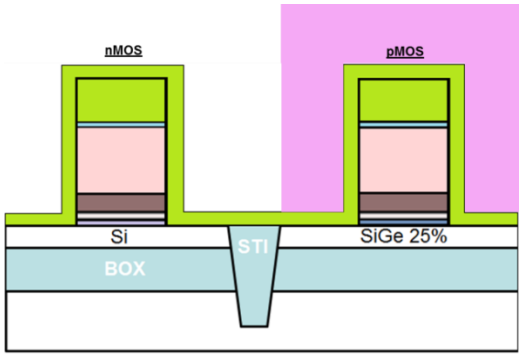



3) First spacer n deposition

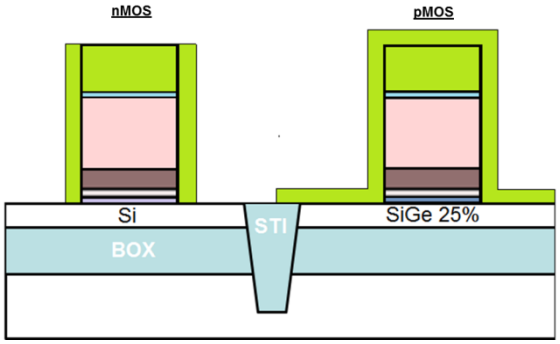
4) Lithography



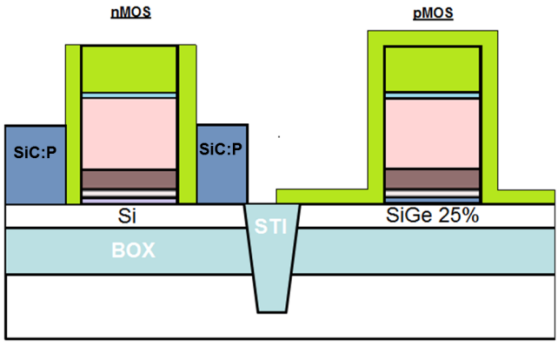

5) First spacer n etching



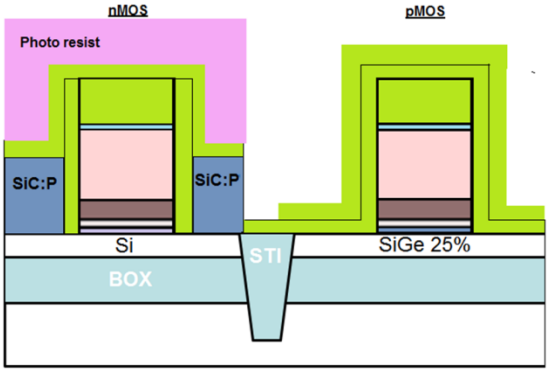

6) Raised Source Drain epitaxy n (SiC:P)



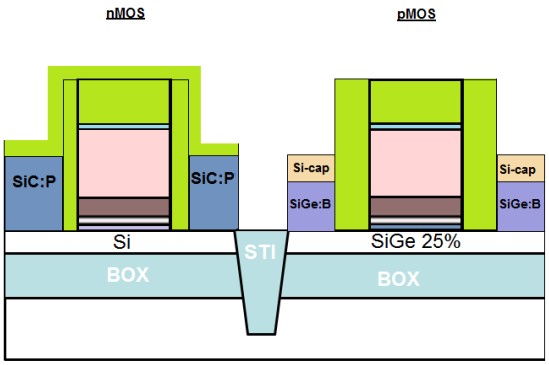

7) First spacer p deposition + lithography



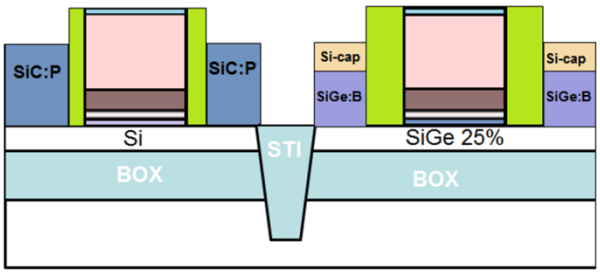

8) First space p etching + Raised Source Drain Epitaxy p (SiGe:B)

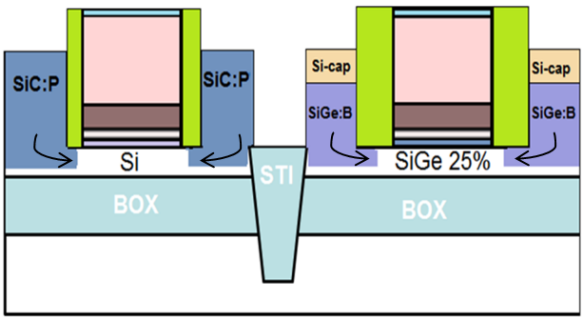



9) Hard mask removal




10) Drive-in anneal



11) Salicidation

12) Contact and BEOL

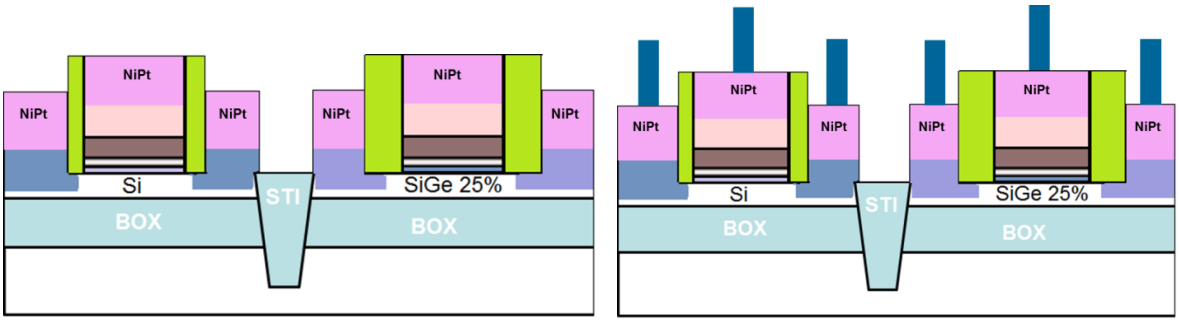



**Figure 3.1 : Process flow for 14nm FDSOI technology.**

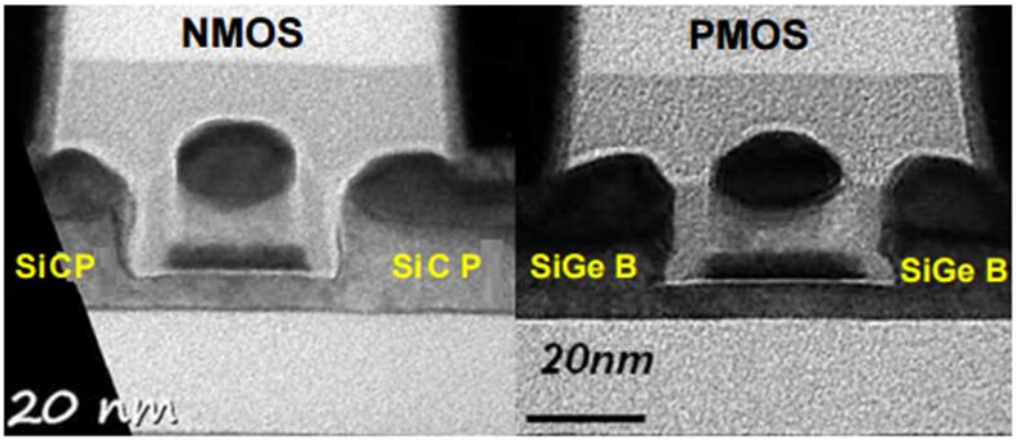



**Figure 3.2: TEM cross section images for nMOS and pMOS fabricated with the POR process 14nm FDSOI [Weber 15].**

In Figure 3.2 are reported the typical nMOS and pMOS transistor TEM cross sections fabricated with the process of reference of the 14 nm FDSOI technology detailed in Figure 3.1.

## 3.2 Low Temperature Extension First process flow

In the previous paragraph, the standard process flow for 14 nm FDSOI technology has been presented. In this section, the flow modifications necessary to integrate the low temperature extension first scheme are presented and schematically reported in Figure 3.3.

- **First spacer n deposition:** in this case, a nitride of 3 nm is deposited (instead of 6 nm).
- **Extension first implantation:** ion implantation is made through the 3 nm nitride. Germanium and phosphorus have been chosen for nMOS while germanium and boron for pMOS. Germanium is used to obtain pre-amorphization (PAI). The implantation is made through a thin 3 nm nitride for two reasons:

i) **A gate liner protection is necessary for CMOS integration:** If on the same wafer, nMOS and pMOS devices are desired, a photo resist deposition is necessary in order to protect pMOS zones at the moment of nMOS implant (and viceversa). During the stripping step a liner protection is mandatory in order to avoid gate stack degradation.

ii) **The energy process window for doping implant definition is more adapted for the available implantation tool if a SiN liner is present during the implantation step.** This point will be detailed in section 3.3.2.

- **Photo resist deposition**: pMOS zones are protected by photo resistive material.
- **Complement spacer:** a 3nm nitride is deposited in order to reach 6nm corresponding to the standard thickness of the first spacer for n-type devices. This process step is made with a thermal budget of 630 °C for 2 hours that is largely sufficient to re-crystalize the amorphous zone created by implantation.
- Same lithography and SiN etching techniques than in standard 14 nm FDSOI flow are used to nMOS and pMOS epitaxies. However, due to thermal budget limitations the following modifications have been introduced:
  i) For **n-type epitaxy**, no high temperature pre-bake has been applied. **SiCONi** surface preparation has been used.
  ii) For **p-type epitaxy**, no silicon capping layer has been growth. Only SiGe:B epitaxy has been made.

These two last modifications are necessary to be consistent with the thermal budget required by CoolCube integration.

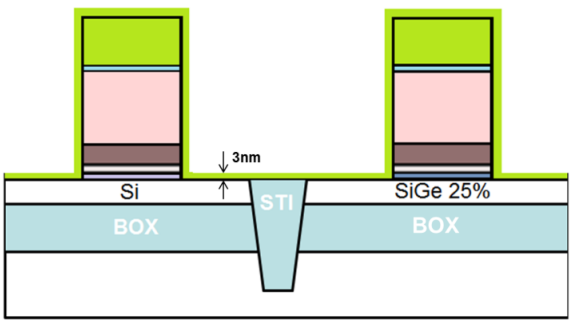
- **No drive-in anneal** has been performed: the dopants activation level in the RSD regions will be the one achieved just after the in-situ-doped epitaxy.

The process flow continues as the standard for 14 nm FDSOI technology.

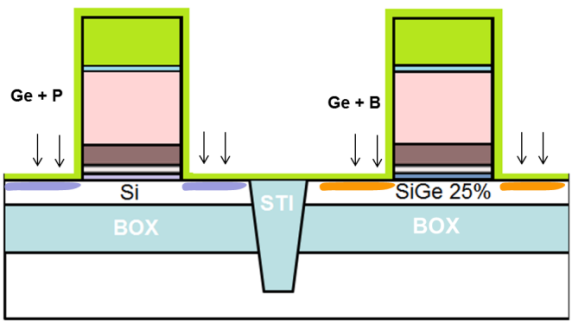
Low temperature extensions first process flow, presents two important technological challenges: the definition of implant conditions, where partial amorphization is needed, in a really thin film of 6 nm and the epitaxial regrowth on implanted (amorphized) films.

The solutions to these challenges are proposed in next sessions.

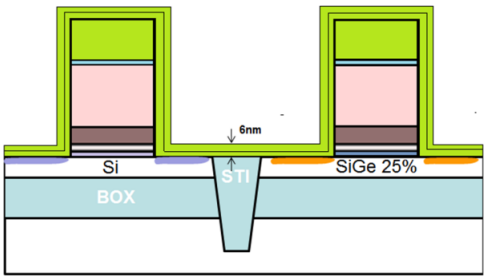
Thin SiN liner deposition




Extension First implant



Complement first spacer deposition




Raised Source Drain and Low Temperature Epitaxy

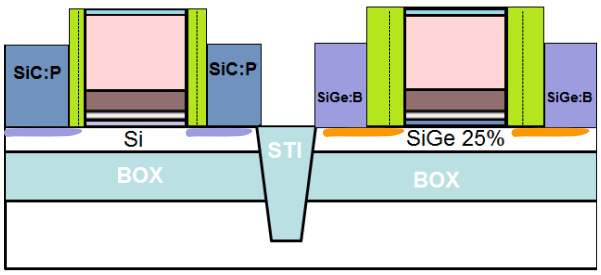



**Figure 3.3: Low temperature extension first scheme. Only the process steps that are different from standard flow presented in Figure 3.2 are here illustrated.**

## 3.3 Extension first implant condition definitions

The first challenge for the process flow presented in section 3.2 is the implant conditions definition. It is worth remembering that in order to get efficient doping activation by low temperature SPER, it is necessary to create an amorphous zone. This is not trivial in a 6 nm thin film; in fact, a very thin amorphous region (~3 nm) has to be defined in order to preserve the crystalline seed necessary for the re-crystallization by SPE.

The implant conditions have been defined by KMC simulation and validated by TEM observation on full sheet wafer of Si on Insulator and SiGe 25% on insulator, corresponding to nMOS and pMOS case respectively. Two different configurations have been tested: the implant is made directly into the silicon film or through thin silicon nitride capping of 3 nm. The second configuration will be the choice integrated in the electrical devices as reported on the process flow of Figure 3.3.

### 3.3.1 Extension First implant without nitride capping

The simulated structure used to study the effects of extension first implantations without the superficial nitride capping is illustrated in Figure 3.4. One nanometer of native oxide has been considered to be present on the surface at the moment of doping implantation. Even though p-type implant has been made on SiGe film, simulation has been carried out considering a silicon film. This is acceptable according to [Payet 16] where is reported that for low energy and low dose implantation the amorphization depths in Si and SiGe are comparable.

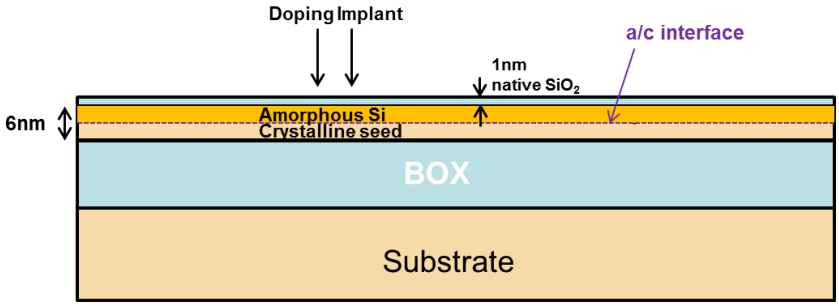



**Figure 3.4: Simulated structure for doping conditions definition in extension first scheme.**

Two aspects need to be optimized regarding the implant condition definition:

i) Doping profile;
ii) Amorphization depth.

First of all, the doping profile corresponding to the maximum concentration target (3-4x$10^{20}$ at/$cm^3$) has been defined with boron and phosphorus implant for p-type and n-type respectively. The doping profiles are illustrated in Figure 3.5 and 3.6.

However, according to simulation results, for the energy and dose chosen, boron and phosphorus implants do not lead to any silicon amorphization and a pre-amorphization step is necessary. Germanium has been chosen as pre-amorphizing specie. However, a low energy implantation value of 1 keV has to be defined in order to avoid total film amorphization. With such low energy, Figure 3.7 indicates that the phosphorus doping will need a Ge concentration of at least $10^{14}$ at/$cm^2$ to obtain good amorphization within the first 3 nm of the silicon film. For boron doping, the germanium pre-amorphization dose needs to be above 4x$10^{14}$ at/$cm^2$, as reported in Figure 3.8.

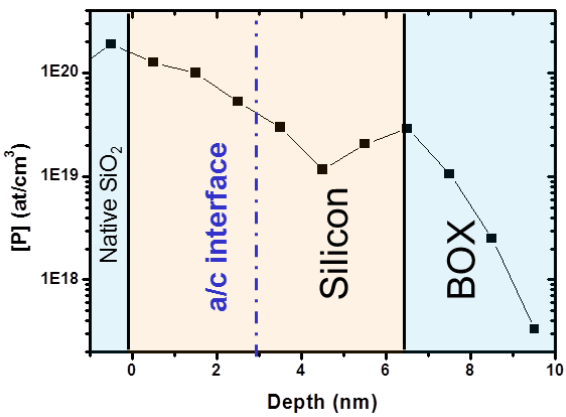



**Figure 3.5: Phosphorus 1D profile simulation, after xFirst implant.**

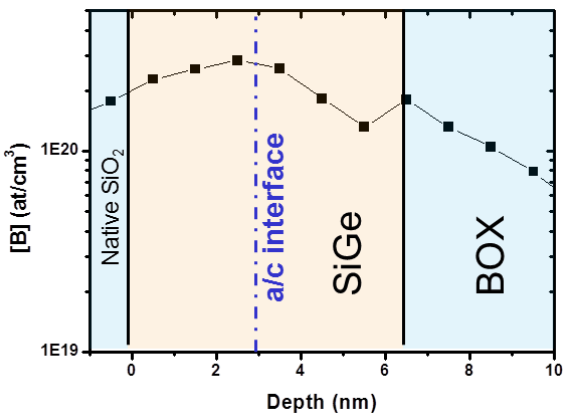



**Figure 3.6: Boron 1D profile simulation, after xFirst implant.**

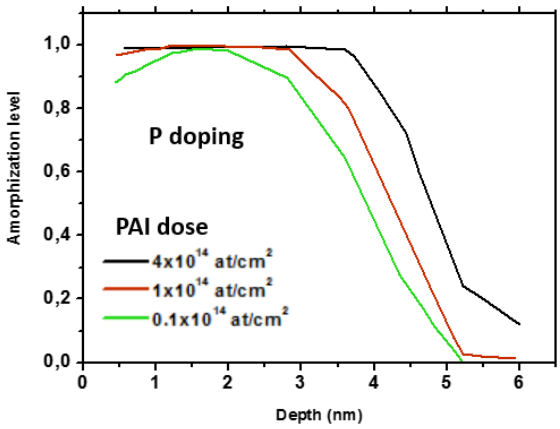



**Figure 3.7: Amorphization level for different germanium pre-amorphization doses and 1 KeV implantation energy, with phosphorus doping.**

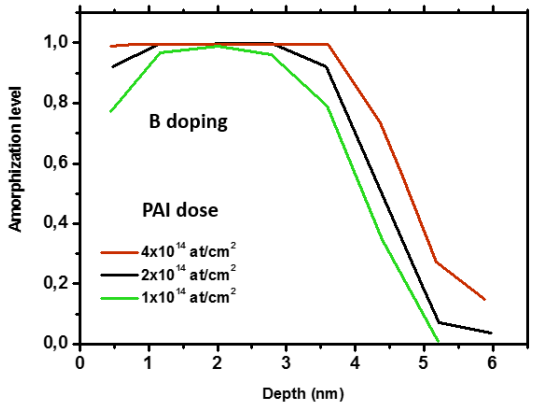



**Figure 3.8 : Amorphization level for different germanium pre-amorphization doses and 1 KeV implantation energy, with boron doping.**

The optimized implantation conditions determined by simulation have been tested on full sheet wafers. TEM cross sections are reported in Figure 3.9 and 3.10.

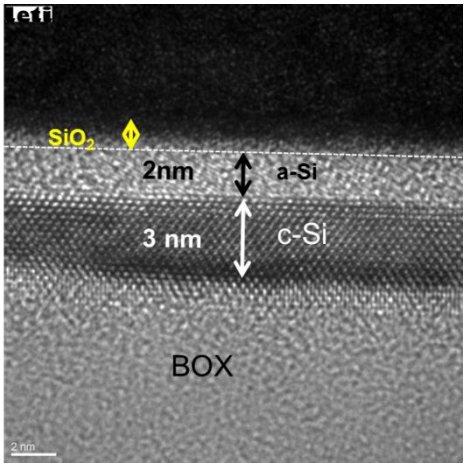



**Figure 3.9: TEM observation of amorphized region after Ge+P extension first implant.**

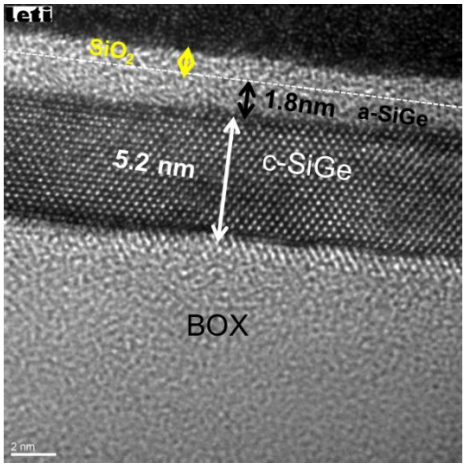



**Figure 3.10: TEM observation of amorphized region after Ge+B extension first implant.**

It is worth noticing that the optimum pre-amorphization conditions need an extremely low germanium energy of 1 KeV. This value is unusual for the available beam-line implantation tool due to the beam instability. However, other existing tools can perform the defined implantation conditions and this option of extension implantation directly into the silicon film has to be considered as a valid option. In order to develop the integration scheme with the available implantation tool, the doping conditions have been tested through a thin film of silicon nitride of 3 nm. In this case, higher pre-amorphization energies, that are more suitable for the implantation tool, can be used.

### 3.3.2 Extension First implant through nitride capping

A silicon nitride layer of 3 nm is deposited on SOI surface by Atomic Layer Deposition (ALD). The silicon nitride density ($d_{SiN}$=3.46 g/cm$^3$) is significantly higher than the silicon density ($d_{Si}$=2.57 g/cm$^3$). It means that silicon nitride will provide higher stopping power to the implanted species than silicon. TCAD simulations predict that in terms of amorphization depth, 3 nm of silicon roughly correspond to 1 nm of silicon nitride. For this reason, the presence of a nitride liner allows to doping condition definition with higher energy and dose.

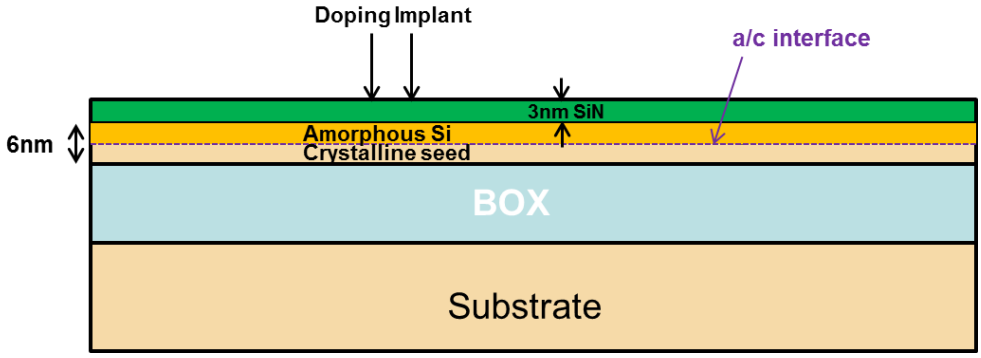



**Figure 3.11 : Simulated structure for doping conditions definition in extension first scheme with nitride capping.**

As for the previous case without nitride capping, the doping conditions (phosphorus for silicon film and boron for SiGe film) have been defined obtaining the doping profiles in Figure 3.12 and 3.13.

Then, germanium pre-amorphization conditions have been defined in order to obtain a 3 nm range of amorphization depth and 3 nm range of crystalline seed. The TEM observations after implantation are shown in Figure 3.14 and 3.15.

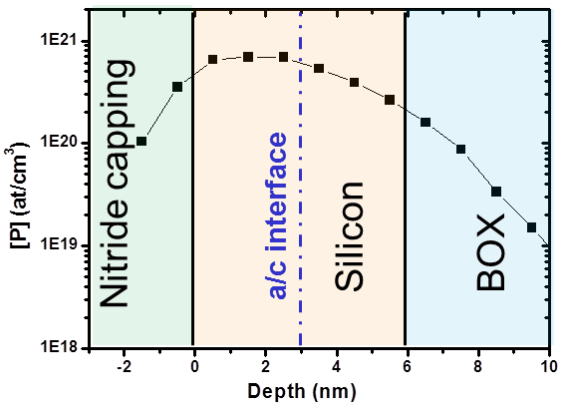



**Figure 3.12: Phosporus one-dimensional profile, after extension first implant through nitride capping liner.**

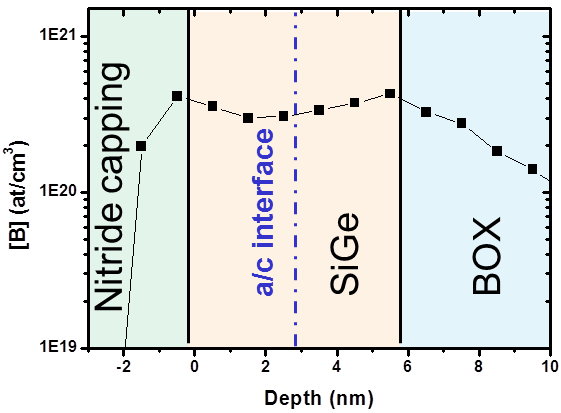



**Figure 3.13: Boron one-dimensional profile, after extension first implant through nitride capping liner.**

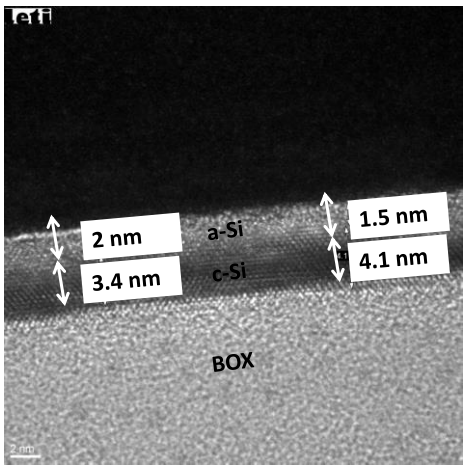



**Figure 3.14: TEM observation of the amorphized region after Ge+P extension first implant on Si film through SiN capping. SiN capping has been removed before the TEM observation.**

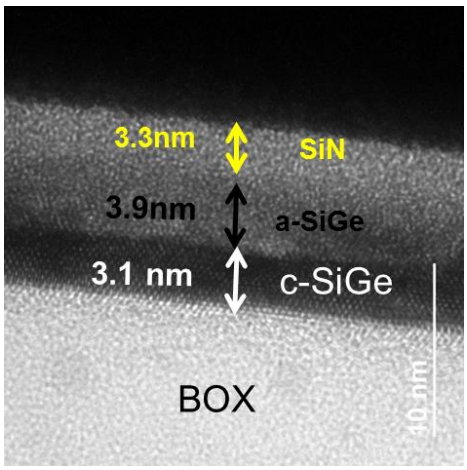



**Figure 3.15: TEM observation of the amorphized region after Ge+B extension first implant on SiGe film through SiN capping.**

## 3.4 Activation level measurement for Extension First doping

In the previous section, the doping conditions for extension first Integration have been defined. The doping profile and the amorphization depth have been taken into account as the key parameters for the optimization. However, the final demonstration of the doping efficiency is the activation level measurement. This evaluation is not trivial, since the really thin film used for the extension first doping step can lead to some difficulties in the experimental set up and results interpretation.

### 3.4.1 p-type doping

Firstly, boron doped SiGe film has been annealed for 5 minutes at 500 °C. This thermal budget is supposed to be largely sufficient to recrystallize the 3.9 nm of amorphized film, according to the SPER Rate reported in literature [Haynes 95]. However, as illustrated by the TEM cross section in Figure 3.16, only ~1.5 nm have been effectively recrystallized. In order to complete the re-crystallization, a further anneal of 10 min at 630 °C has been applied. This thermal budget is compatible to the SiGe epitaxial growth of raised source and drain region. As illustrated in Figure 3.17, a further recrystallization of ~1 nm occurred. However, amorphous/crystalline interface roughness has to be taken into account and the re-crystallized thickness, assumed as the active semiconductor film can be considered between 3.1 and 1.8 nm. The incomplete re-crystallization can be explained by the presence of nitrogen introduced by recoil during the implantation step. The presence of nitrogen is detrimental for re-crystallization rate similarly to the effect of oxygen discussed in section 1.4.2 [Kennedy 77]. Close to the sample surface, when the nitrogen concentration by recoil is high, the SPER rate decreases to values that do not allow the complete re-crystallization within a time that is compatible with industrial process.

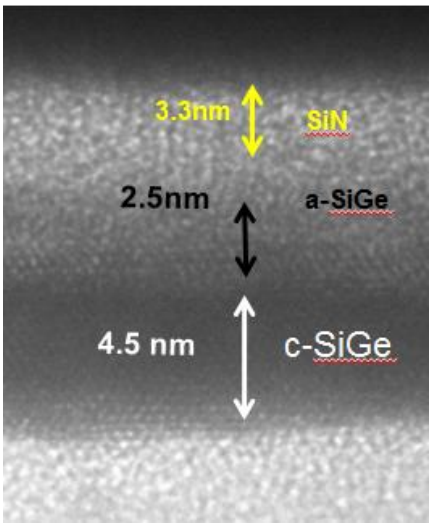



**Figure 3.16: TEM cross section of Boron doped SiGe film after 5 minutes at 500 °C.**

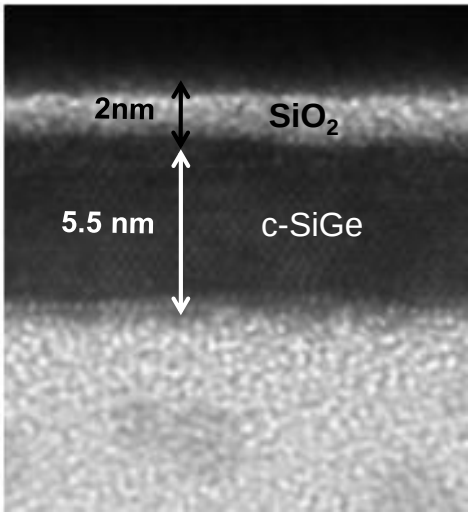



**Figure 3.17: TEM cross section of Boron doped SiGe film after 10 minutes at 640 °C. Nitride capping has been removed before TEM analysis.**

Boron activation level in SiGe 25% film is evaluated by $R_{SHEET}$ measurement using the four points probe method, Electrochemical Capacitance-Voltage (ECV) technique and effect Hall measurement.

**<u>Sheet resistance measurement</u>**

The simplest technique to evaluate the efficiency of the dopant activation after implantation and annealing is the sheet resistance measurement by 4 points probe method. In Figure 3.18, 50 points of sheet resistance are reported on 300 mm wafer. High-dispersed values in a range of 2.9 – 4.2 KΩ/□ are observed with a median value of 3.5 KΩ/□.

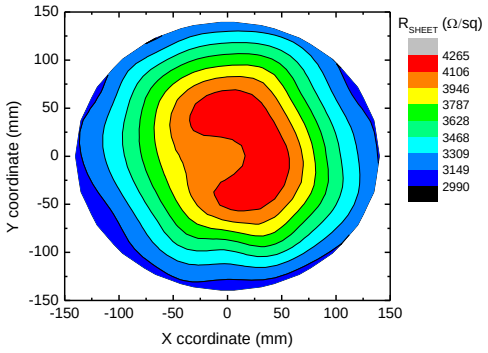



**Figure 3.18 : $R_{SHEET}$ measurement of boron implant on SiGe film onto 300 mm wafer.**

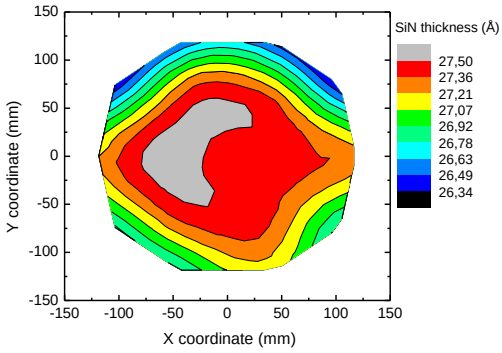



**Figure 3.19 SiN thickness variation on a 300 mm wafer measured by ellipsometry.**

The dopant implantation has been made through a thin SiN layer that is nominally 3 nm thick. However, depending on the lot, thickness variation has been observed. In the TEM observation reported in Figure 3.15, a SiN thickness of about 3.3 nm was measured. 2.7 nm was found in the ellipsometry measurements reported in Figure 3.19. A variability of approximately 0.1 nm is evidenced for the deposited SiN on a 300 mm wafer, with a clear dependence of the SiN thickness on the wafer diameter. Even though this value looks really small, it can lead to significant variation in amorphization depth and then to sheet resistance value after doping step. Indeed, KMC simulations indicate that, using the doping conditions Ge + B defined in section 3.3.2, with a SiN capping of 2.6 nm a sheet resistance value of 2.1 KΩ/□ is predicted, while with a SiN capping layer of 2.7 nm a sheet resistance value of 3.5 KΩ/□ is obtained. This range of sheet resistance variation obtained by varying of 0.1 nm the silicon nitride on the simulated structures is quite similar to the range found on the experimental results (2.9 – 4.2 KΩ/□). Even though simulation does not reproduce exactly the experimental values, the tendency seems to suggest that the variability found in sheet resistance measurement can be explained by a small variability thickness of the deposited nitride capping.

**<u>ECV Measurement</u>**

The Electrochemical Capacitance-Voltage (ECV) profiling technique is employed to measure the active carrier concentration profiles in semiconductor layers. The technique uses an electrolyte-semiconductor Schottky contact to create a depletion region, a region which is empty of conducting electrons and holes, but contain ionized donors and electrically active defects or traps. The depletion region with its ionized charges inside behaves like a capacitor. The measurement of the capacitance provides information of the doping and electrically active defect densities. Depth profiling is achieved by electrolytically etching the semiconductor between the capacitance measurements with no depth limitation [Probion].

The ECV profile has been carried out on boron doped SiGe sample and the result is shown in Figure 3.20 in comparison with the chemical doping profile obtained by KMC simulation. Good agreement between the two profiles with reasonable activation level of $3x10^{20}$ at/cm$^3$ for boron in SiGe is found. Moreover, the active doping concentration decreases after 3 nm, which correspond to the position of the former amorphous/crystalline interface. This is in agreement with the hypothesis of efficient dopant activation by SPER only in the amorphized region.

Integrating the ECV profile and using the equation:

$$R_S = \frac{1}{\int_0^t p(x)\mu(x)dx} \tag{3.1}$$

$R_{SHEET}^{ECV}$ is found to be equal to 1.5 kΩ/□, value out of the range of $R_{SHEET}$ measurements observed in Figure 3.18. $R_{SHEET}^{ECV}$ has been calculated considering the carrier mobility at the thermodynamic equilibrium in a bulk material [Masetti 88]. This last hypothesis could be not valid for really thin film where the surface scattering takes a significant role in the overall carrier mobility leading to a degradation compared to the values in bulk material. Another hypothesis for low $R_{SHEET}^{ECV}$ is that ECV technique overrates the active doping concentration. In order to validate these hypothesis Hall effect measurements have been carried out on boron doped SiGe film.

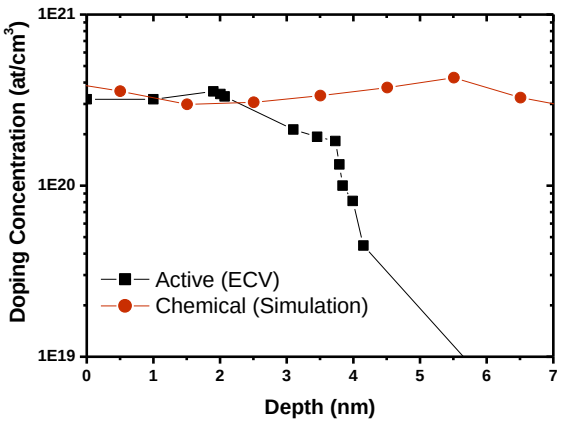



**Figure 3.20 : Active doping profile obtained by ECV technique in comparison to chemical profile (simulation).**

**<u>Effect Hall measurements</u>**

Hall dose and mobility have been measured leading the following results:

- $\mu_H$=11.4 cm²/V·s;
- $d_H$=1.3x10¹⁴ at/cm².

The measured values have to be corrected by the Hall factor $r_H$. For $Si_xGe_{1-x}$ with 20<x< 30, $r_H$ is assumed to be between 0.3 and 0.4 as reported in [Joelsson 97].

The effective active dose and mobility are then calculated as:

- $\mu = \frac{\mu_H}{r_H} = 28.4\ cm^2/\mathrm{V}\cdot\mathrm{s}$
- $d = d_H \cdot r_H = 5.3x10^{13}\ \frac{at}{cm^2}$

It is worth focusing on mobility-measured value. The value reported in literature for mobility at boron concentration of 3x10²⁰ at/cm³ is $46\ cm^2/\mathrm{V}\cdot\mathrm{s}$ [Masetti 88]. However, this value is extracted for silicon substrate and even higher mobility value is expected for SiGe25% as in our case of study, according to [Manku 93]. It means that high mobility degradation is observed in our case of thin film. Mobility degradation could be explained by high holes surface scattering that in this case of study is a first order phenomenon since the conduction is made in the first 2-3 nm below the surface.

Fixing the activation level at $3x10^{20}$ at/cm$^3$ as extracted by ECV measurement and sheet resistance between 4.2 and 2.9 KΩ/□ as measured in Figure 3.18, the active semiconductor thickness has been calculated using 3.1. Thickness range of 1.8 nm – 2.5 nm has been extracted in good agreement with re-crystallized thickness variability measured by TEM observations. This result shows the coherence among the three proposed techniques.

### 3.4.2 n-type doping

Phosphorus doped silicon film reported in Figure 3.14 has been annealed at 600 °C for 2 minutes in order to obtain the re-crystallization of the amorphized region and the sheet resistance measurement has been performed. High values in the range of 160 KΩ/□ have been found corresponding to an activation level below $1x10^{19}$ at/cm$^3$ considering 2 nm of active film. This high sheet resistance value can be explained by the presence of nitrogen introduced into the film by the dopant implantation that can lead to:

i) A significant slowdown of the SPER rate in the layer close to the surface. In this case the thickness corresponding to the active zone is smaller than the considered 2 nm of the amorphized region
ii) Nitrogen is known in literature [Chang 14] to form inactive agglomerates with n-type species.

A deeper analysis of sheet resistance measurements of phosphorus doped thin films is currently ongoing.

## 3.5 Epitaxial growth on implanted film

Once the extension implantation conditions have been defined and the doping activation have been demonstrated, the extension first integration presents another important challenge such as the epitaxial regrowth of raised source and drain on an implanted film. The epitaxial growth on implanted film has been studied by several works: [Pivac 92], [Maruno 01], [Gonzatti 10], [Morita 14]. All these works present some difficulties in the epitaxial regrowth on boron implanted film, while no particular issues are found on n-type implanted film. However, these works consider pure silicon epitaxial growth, while in our case SiC:P or SiGe:B epitaxy will be made.

### 3.5.1 n-type epitaxy on implanted film

For nFET devices, the raised source and drain epitaxy consists in silicon and carbon alloy (with 1% of Carbon) with phosphorus in-situ doping, so named SiC:P. Several implantation conditions have been tested, with different results on the epitaxial regrowth quality. In some cases, the epitaxy did not growth at all. Significant differences in the SiC:P epitaxial growth have been found using two different implantation tools, with the same implant conditions (Ge PAI with $1.2x10^{15}$ at/cm$^2$ dose and phosphorus implant with condition defined in Figure 3.12). This can be ascribed to the different machine parameters such as implantation current that can lead to different amorphization depth. Top

view observation on isolated active zones after SiC:P epitaxy are shown in Figure 3.21. In Figures 3.21a and 3.21b the same PAI conditions defined in section 3.3.2 (sample named High PAI) have been used with two different implantation tools. For tool 1 (Figure 3.20a), the epitaxial regrowth totally fails. Using tool 2, the epitaxial regrowth quality improves, but the crystalline character is not acceptable yet. Reducing the PAI dose to $5x10^{14}$ at/cm$^2$ (sample named medium PAI), the epitaxial quality substantially improves (Figure 3.21c). Even better epitaxy aspect is obtained if no PAI is performed (Figure 4d). It is worth noticing that for the four cases the phosphorus implant condition is the same. Similar results are observed on ring oscillators like structures displaying high gate density (Figure 3.22).

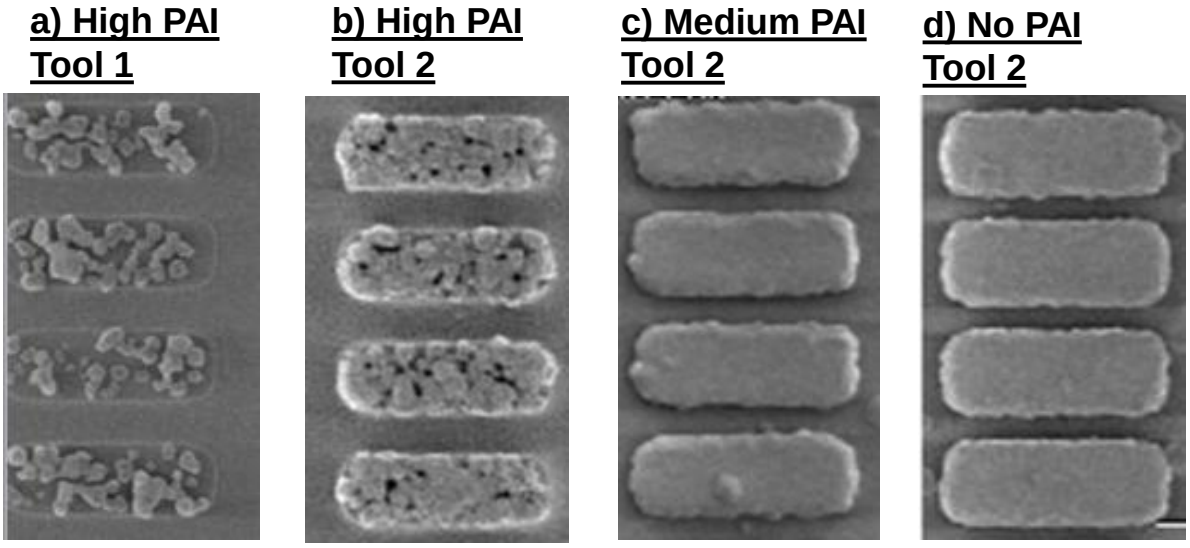



**Figure 3.21: Top view observation post SiC:P epitaxy for different PAI conditions on isolated structures. The epitaxial quality improves if the PAI dose is reduced.**

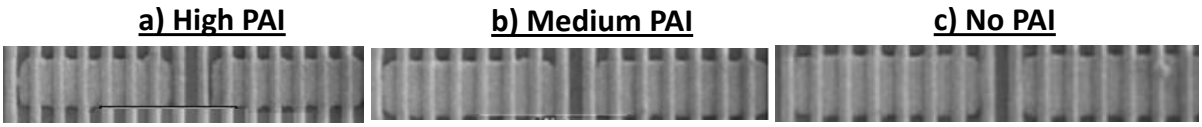



**Figure 3.22: Top view observation on ring oscillators structures after n-type epitaxy for different implantation conditions.**

Ellipsometry measurements carried out post SiC:P epitaxy presented in Figure 3.23, confirm the trend found on top view observations. The Goodness of Fitting (GOF) for the case without any PAI is acceptable, while it presents high degradation for high dose PAI as illustrated in Figure 3.24. Only some measurement sites present acceptable GOF value, while values of ~0.2 indicate bad epitaxy quality. Results of the epitaxial thickness measurements are presented in Figure 3.24. Following the same trend of the GOF and show extremely variable thickness epitaxy is observed for different sites. In some case it appears that epitaxy has not grown at all.

Useful indications on the epitaxial quality can be provided by sheet resistance measurements made on both SOI and bulk structures (Figure 3.25). In Table 3.1, the split details are reported. Significant $R_{SHEET}$ degradation appears only in case of high dose PAI. In addition, the sheet resistance degradation is evident only on SOI structures. On bulk structure, it can be considered that an infinite crystalline seed is always present while on SOI the crystalline seed is limited by the presence of the buried oxide. A

minimum crystalline seed (approximately 2 nm) has to be present at the moment of the epitaxial step in order to act as a pattern for a good crystalline quality epitaxial re-growth.

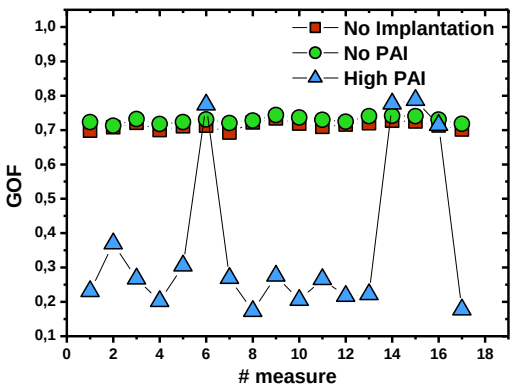



**Figure 3.23: GOF ellipsometry measurement post SiC:P epitaxy on 17 wafer sites.**

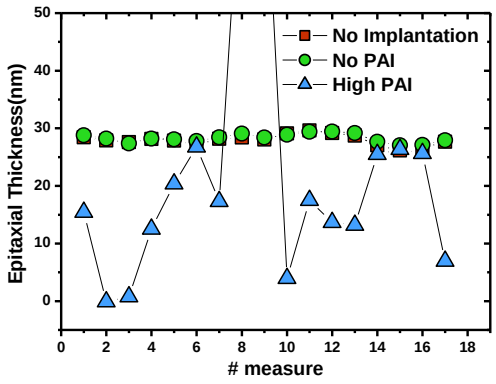



**Figure 3.24: SiC:P epitaxy thickness measured by ellipsometry.**

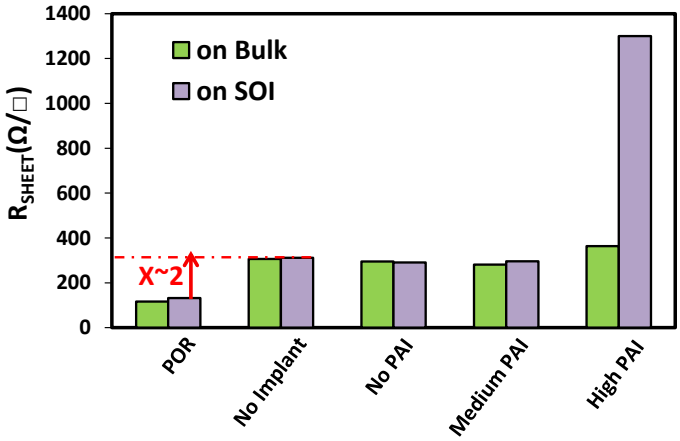



**Figure 3.25: RSHEET measurement on bulk and SOI structures for splits described in Table 3.1.**

| | PAI Dose | P Implant | Spike annealing |
|---|---|---|---|
| **POR** | no | no | Yes |
| **No Implant** | no | no | No |
| **No PAI** | no | yes | No |
| **Medium PAI** | $5x10^{14}$ at/cm$^2$ | yes | No |
| **High PAI** | $1.2x10^{15}$ at/cm$^2$ | yes | No |

**Table 3.1: Splits details of nMOS devices.**

Figure 3.14 show that the implantation conditions chosen, corresponding to the High PAI, does not lead to full amorphization, but a crystalline seed of approximately 3-4 nm is present, enough to

guarantee re-crystallization by SPER. So, the chosen condition does not lead to a full film amorphization that could justify the epitaxial growth failure as reported by the ellipsometry measurements (Figure 3.24) and sheet resistance (Figure 3.25). A possible explication is related to the silicon film consumption due to the particularity of the SiC:P process step. SiC:P epitaxy is made by cycles of deposition and etching step. In the case of High PAI, the sample surface is probably not crystalline or with high density of defects generated by the germanium implantation. The etching steps will lead to a partial consumption of the silicon film. So, following the amorphization depth variability, on certain wafer sites the crystalline seed is too thin to promote an epitaxial regrowth.

However, slight $R_{SHEET}$ degradation is observed in High PAI (364 Ω/□) sample compared to No PAI one (295 Ω/□) on bulk structures. This can be related to the bad epitaxial quality due to the highly defective silicon substrate created by the high dose germanium amorphization.

For no PAI and Medium PAI cases, $R_{SHEET}$ values are compatible with No Implant sample. This suggests a good epitaxial regrowth on implanted structures. Moreover, slight better $R_{SHEET}$ is found in case of Medium PAI (296 Ω/□) and no PAI (291 Ω/□) on SOI structures compared to the case of no implantation (312 Ω/□). This can be explained by additional 2 nm of activated region corresponding to the implanted zone before the epitaxial regrowth.

It is worth noticing how POR $R_{SHEET}$ value is at least a factor two lower than the cases where no spike annealing activation has been made (No implant split). It means that phosphorus in-situ doped activation level is improved if a thermal annealing is made after the SiC:P epitaxial growth.

### 3.5.2 p-type epitaxy on implanted film

For pFET devices, the raised source and drain epitaxy consists in silicon and germanium alloy (with 35% of germanium) with boron in-situ doping, so named SiGe:B. In this case, on ring oscillators like structures, top view observations post SiGe:B, show good quality epitaxy even with the most aggressive PAI conditions tested. A comparison for different PAI conditions is shown in Figure 3.26.

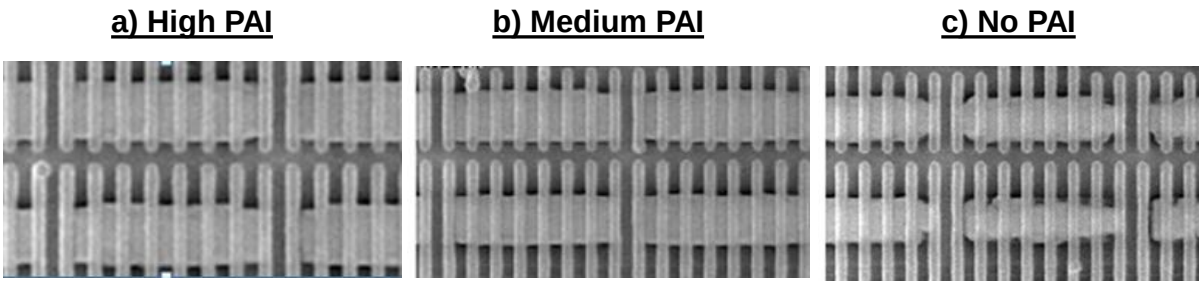



**Figure 3.26: Top view observation post p-type epitaxy on Ring Oscillator structures.**

Figure 3.26c, corresponding to the extension first implantation without PAI, shows a bad epitaxy quality compared to the cases with PAI. This could be explained by two hypotheses:

i) The role of pre-epitaxial cleaning: in the case of PAI, the film surface is highly damaged and the SPER re-crystallization is not able to recover completely the crystalline quality. The pre-cleaning can consummate a small layer of film surface, obtaining a good surface quality before the epitaxial step. In the case of no PAI, less damage is created at the surface and the pre-cleaning step probably does not etch away the first silicon surface layers. The remaining damaged surface film could have been led to a non-perfect epitaxial quality as observed in Figure 3.26c.

ii) In case of PAI, the film epitaxial quality is recovered by SPER. In case of no PAI, some defects will be created by the boron implantation that cannot be recovered by the application of a low temperature anneal at 630 °C. As a consequence, the SiGe:B takes place on a damaged film and the crystalline quality can be degraded.

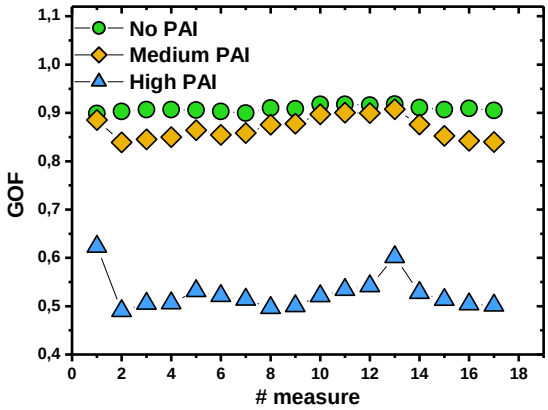



**Figure 3.27: GOF ellipsometry measurement post SiGe:B epitaxy on SiGeOI structures.**

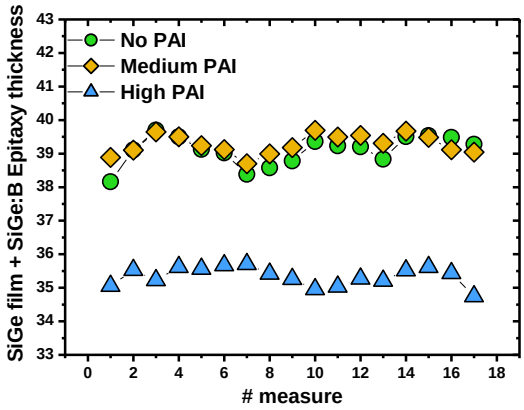



**Figure 3.28: Total SiGe:B epitaxy and SiGe film thickness by ellipsometry on SiGeOI structures.**

Interesting information can be extracted by ellipsometry measurements. Figure 3.27-3.28 show the GOF and the thickness of the total stack SiGe25% film and SiGe:B epitaxy. The bottom layer of the stack is the buried oxide (not included in the measurements). Acceptable GOF values are obtained even for medium dose PAI, while for High PAI dose evident degradation occurs. Moreover, the total thickness looks ~4 nm thinner compared to the case with no PAI. Ellipsometry measurements have been performed bulk silicon substrate (Figure 3.29-3.30). The GOF is slightly degraded for medium PAI dose case compared to no PAI. Unacceptable GOF values are reported for the case with high PAI dose. SiGe:B thickness reduction in the range of 4 nm, or higher, is observed on bulk structures. This shows that there is a growth delay on implanted film with high PAI dose. This can be explained by the fact that at early stages of the epitaxy step, the regrowth is not efficient due to bad quality of the film surface. So, at the end of the epitaxial step, the final thickness will be reduced.

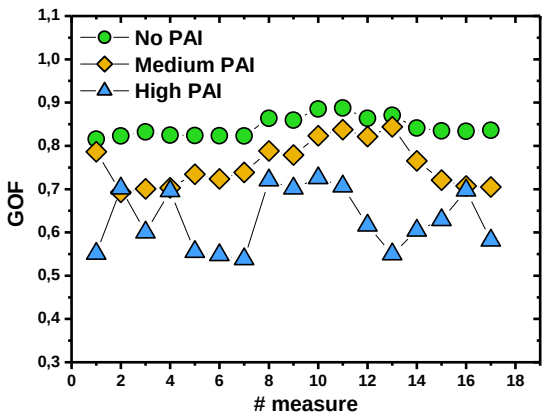



**Figure 3.29: GOF ellipsometry measurement post SiGe:B epitaxy on bulk structures.**

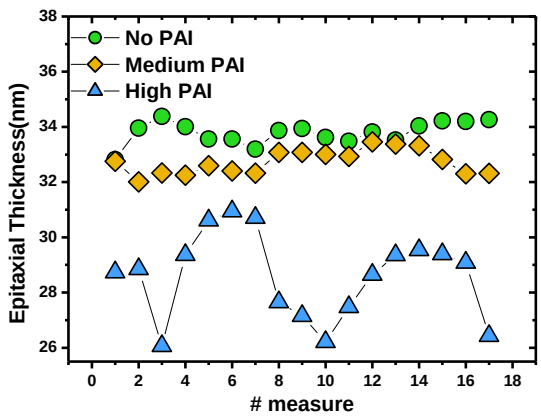



**Figure 3.30: SiGe:B epitaxy thickness by ellipsometry on bulk strcutures.**

Sheet resistance measurements on SOI and bulk devices after SiGe:B epitaxy on SIGe film are shown in Figure 3.31. For High dose PAI, significant sheet resistance degradation is found on both SOI and bulk structures. $R_{SHEET}$ degradation on bulk cannot be related to amorphization depth after implantation. $R_{SHEET}$ degradation can be explained by the defects incorporation during the epitaxial growth, due the high surface roughness caused by the extension first implantation. For all the other cases sheet resistance values are close the POR values. Except for the High PAI split where the epitaxy is defective, no modification of sheet resistance values are observed between the POR split and the low temperature splits indicating that boron in-situ doping is well activated during the SiGe:B epitaxial regrowth without the need of spike activation.

| | **PAI Dose** | **B Implant** | **Spike annealing** |
|---|---|---|---|
| **POR** | no | no | Yes |
| **No Implant** | no | no | No |
| **No PAI** | no | yes | No |
| **Medium PAI** | $5x10^{14}$ at/cm$^2$ | yes | No |
| **High PAI** | $1.2x10^{15}$ at/cm$^2$ | yes | No |

**Table 3.2: Splits details of pMOS devices.**

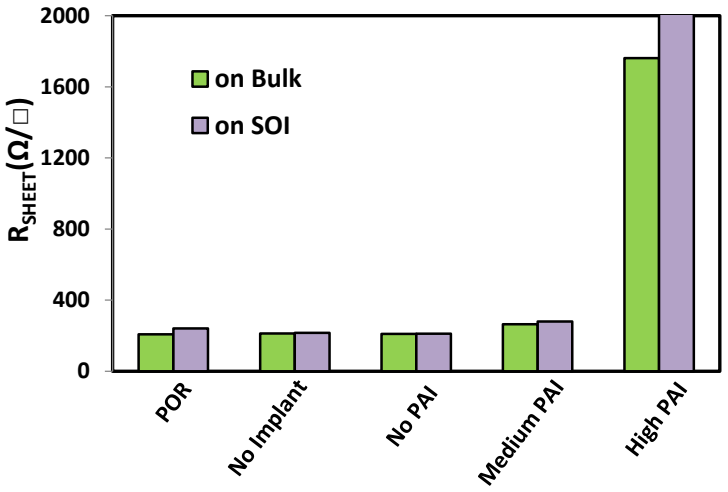



**Figure 3.31: $R_{SHEET}$ measurement on Bulk and SOI unsalicided structures for splits described in Table 3.1.**

## 3.6 Low temperature FDSOI with extension first scheme: electrical results

In this section, the electrical characterization of extension first low temperature devices is compared to the high temperature POR device. For the first time, working 14 nm FDSOI devices fabricated at low temperature with the extension first integration scheme have been obtained. FDSOI devices with width of 0.17 µm and channel length ranging from 20 nm to 1 µm have been characterized. Split details are reported in Table 3.1 and 3.2 for nMOS and pMOS respectively.

### 3.6.1 nFET electrical results

In Figure 3.32 is shown a TEM observation of an nMOS device fabricated with the extension first integration at low temperature. The physical gate length is L=20 nm and the width dimension is W=170 nm that corresponds to the smallest transistor device of the 14 nm FDSOI technology proposed by STMicroelectronics.

$I_{ON}$-$I_{OFF}$ trade-off for nFET devices detailed in Table 3.1 is shown in Figure 3.33. $I_{ON}$ is extracted in saturation regime at $V_{DS}$=$V_{GS}$=0.8 V. Best low temperature split corresponds to the case without PAI, showing 12% degradation compared to the POR. This result is really promising: this is a first test of the extension first integration at low temperature on an advanced technology such as the 14 nm FDSOI. Working devices with performance not so far from the process of reference target indicate a good starting point for the integration of this process.

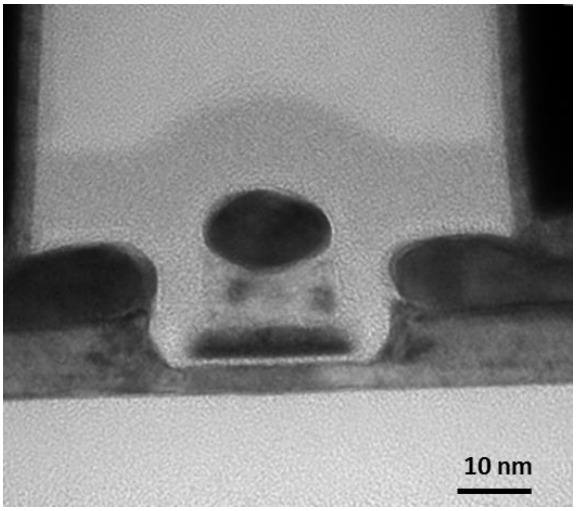



**Figure 3.32: TEM observation of nMOS FDSOI device fabricated with extension first integration.**

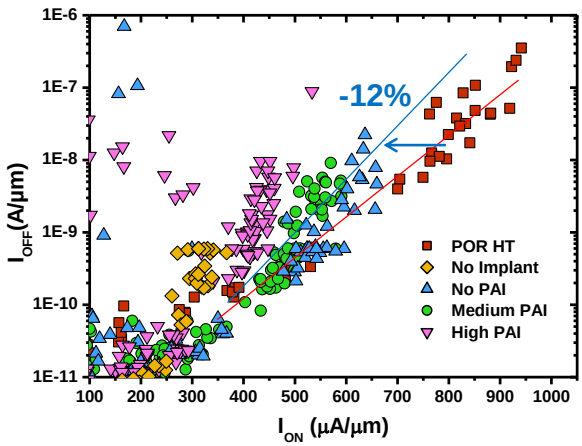



**Figure 3.33: $I_{ON}$-$I_{OFF}$ performance of low temperature Extension First nFET devices compared with HT-POR 14 nm FDSOI for different PAI conditions.**

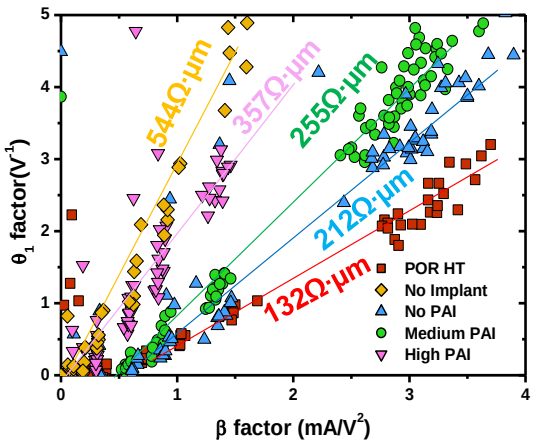



**Figure 3.34: $R_{SD}$ resistance extraction of nFET devices.**

Higher performance degradation (-22%) is observed for Medium PAI split and even higher (-38%) for High PAI split. Access resistance for different splits, extracted by Y function is shown in Figure 3.34. Same split tendency than in $I_{ON}$-$I_{OFF}$ trade-off can be found.

Access resistance degradation for High PAI split can be easily explained by the sheet resistance measurements reported in Figure 3.25 where high degradation was shown for high PAI split, due to the epitaxial quality degradation. However, at first sight, it is surprising that No PAI split exhibits the best performance for low temperature devices. Germanium pre-amorphization is supposed to increase the activation level and improve the $R_{SPA}$ value, leading to a better access resistance than the only phosphorus implantation. The implantation condition No PAI have been applied on full sheet wafer similarly to what reported in Figure 3.14 for High PAI conditions. Good crystalline quality is evidenced all along the film depth on the TEM cross-section reported in Figure 3.35.

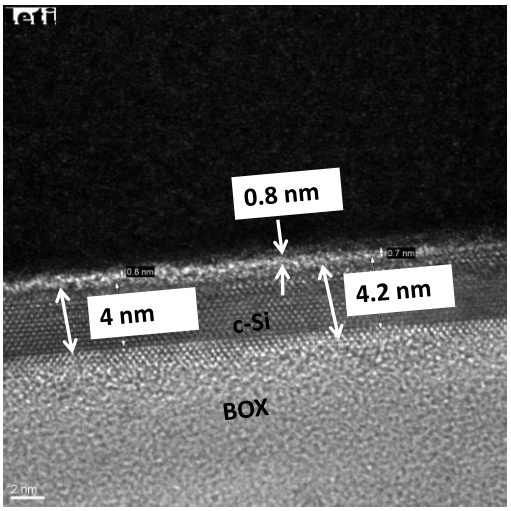



**Figure 3.35: TEM observation of full sheet samples implanted with phosphorus no PAI conditions.**

Sheet resistance measurement performed after anneal for 2 minutes at 600 °C, has been performed obtaining the value of 60 KΩ/□, that is significantly lower than the one obtained with pre-amorphization (160 KΩ/□). The better performance for no PAI split are then related to a better value of $R_{SPA}$ compared to the case of amorphization. This can be related to the presence of nitride introduced in the silicon film by recoil: higher nitrogen concentration will be introduced in the film if germanium PAI implantation is made. As reported in section 3.4.2, nitrogen atoms can interact with dopants creating inactive agglomerates that reduce the $R_{SPA}$ value. Even though the sheet resistance value of 60 KΩ/□ appears elevated (around one order of magnitude higher than in p-type case), good electrical performance has been obtained considering the small size of the first spacer (2 nm, as evidenced in Figure 3.32). For this reason, the phosphorus solubility limit value at 630 °C of $8x10^{19}$ at/cm$^3$ (Figure 1.4) is sufficient to have an acceptable value of $R_{SPA}$. All these considerations related to the sheet resistance measurements on full sheet wafers and the link with $R_{SPA}$ values and the electrical performance are currently ongoing in a dedicated work.

It is important to remark that No implant split experiences a severe performance degradation (-50%) compared to POR. This is related to the bad $R_{SPA}$ value since no active dopants are present in the region below the first spacer. This result demonstrates the necessity to position active dopants below the first spacer and the efficiency of the extension first implantations performed on the other three low temperature splits (No PAI, Medium PAI and High PAI).

Salicided sheet resistance values are reported in Figure 3.36. Small degradation for the low temperature split is shown compared to the process of reference. This can indicate that the salicided sheet resistance value is slightly better if the salicidation is made on a well doped epitaxy region (see Figure 3.23). However, salicided sheet resistance values do not impact significantly the electrical performance.

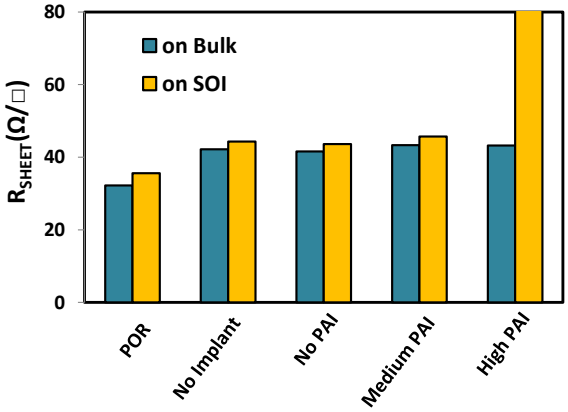



**Figure 3.36: $R_{SHEET}$ measurement on bulk and SOI salicided n-type structures for splits detailed in in Table 3.1.**

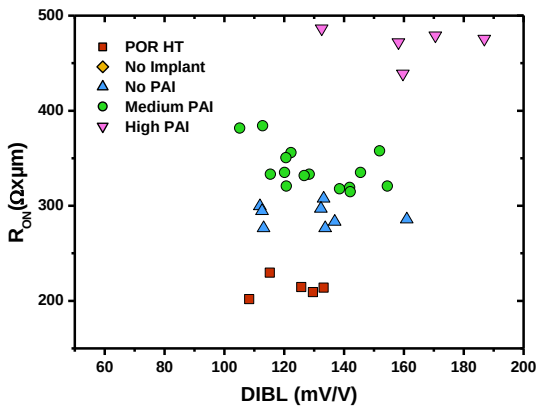



**Figure 3.37: $R_{ON}$ vs DIBL at 20 nm channel length for splits detailed in in Table 3.1.**

In Figure 3.37 $R_{ON}$-DIBL trade-off for 20 nm gate length devices is shown. $R_{ON}$ degradation with the increase of PAI dose confirms the access resistance trend. For No PAI and Medium dose PAI, DIBL is in target with POR value, indicating good channel control by the gate electrode for low temperature devices. No DIBL variation is observed between No PAI and Medium PAI splits indicating similar junction position below the spacer.

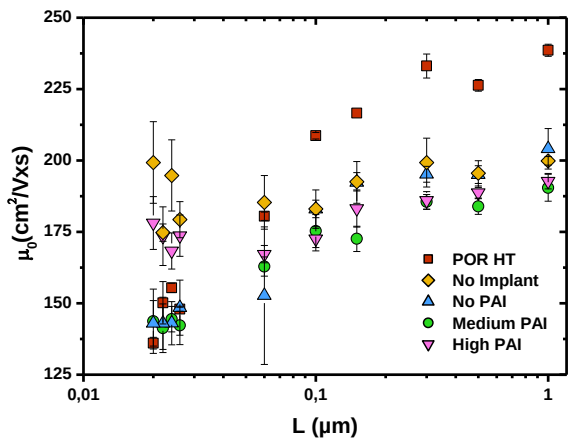



**Figure 3.38: Carrier mobility at low electric field versus gate length for nFET devices on Table 3.1.**

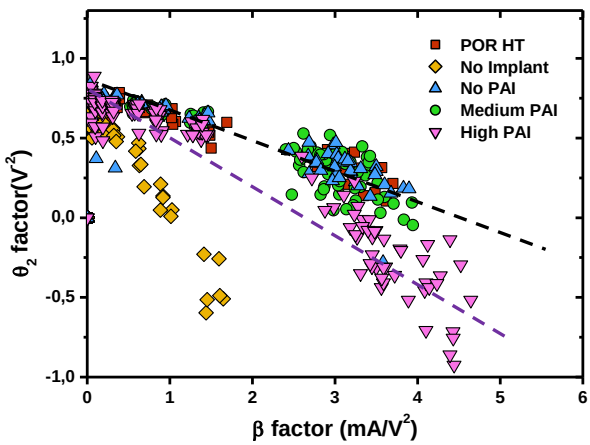



**Figure 3.39: $\theta_2(\beta)$ plot for nFET. The linear fit fails for High PAI and No implant split, leading to an incorrect interpretation of the mobility behavior shown in Figure 3.35.**

Carrier mobility at low electric field is extracted and shown in Figure 3.38. Typical mobility difference at long channel is observed between high temperature and low temperature devices linked to the gate stack modification as presented in chapter two. For short channel lengths, similar mobility values are observed for Medium PAI, No PAI split and POR. However, for High PAI and No Implant split, mobility

at short channel (L<60 nm) appears significantly higher than POR. This last result is completely unexpected, so the extraction method has been investigated in order to check its validity. As discussed in section 2.5.1, in a linear model like:

$$R_{SD}(V_{GS})=R_0 + \lambda(V_{GS}-V_T) \quad (2.11)$$

λ can be extracted by the slope of $\theta_2(\beta)$ plot, reported in Figure 3.39. It is evident that for POR, NO PAI and Medium PAI splits, a linear fitting can be extrapolated and a single value of λ can be extracted. However, the data corresponding to high PAI and No Implant splits, do not allow to any correct linear fit and the one extracted is not representative of plotted points. A correct fit should include two values of λ. It means that the hypothesis of linear dependence of access resistance from the gate bias is no longer valid, affecting the mobility extraction as well. Once again, Y function method appears not appropriated for some particular cases and alternative extraction method have to be developed depending of the device configuration (underlap, overlap and access resistance behavior with the gate voltage).

### 3.6.2 nFET conclusions and perspectives

For the first time, working devices fabricated at low temperature with the extension first process flow have been fabricated using the 14 nm FDSOI technology. Even though the best performance for low temperature devices has been obtained without the use of pre-amorphization, this does not appear the most interesting option for the device optimization. The thermal budget reduction aims to fabricate devices at temperatures around 500 °C. For this temperature, the maximum active concentration of phosphorus without pre-amorphization will be too low to reach the target of $R_{SPA}$. For this reason, pre-amorphization, and dopant activation by SPER is necessary. However, in order to avoid the presence of nitrogen introduced by recoil implantation, a promising option appears the extension first implantation without the presence of the nitride capping.

Another optimization lever for nMOS low temperature device is related to the phosphorus activation in SiC.P epitaxial regrowth. It has been shown that for high temperature device where spike anneal and a DSA activation are performed, the phosphorus activation level in SiC:P epitaxy is improved compared to low temperature devices. This leads to a significant salicide/semiconductor contact resistance degradation and then to an access resistance degradation. This issue can be solved by a SPER activation in the sources and drains region: an amorphizing specie can be implanted after the epitaxial regrowth followed by a low temperature anneal. Good phosphorus activation level can be obtained by SPER. Alternative annealing method such as DSA or nanosecond laser can be used for the dopant activation keeping the compatibility with the low temperature process limitations.

### 3.6.3 pFET electrical results

In Figure 3.40 is shown a TEM observation of a pMOS FDSOI devices fabricated with the extension first integration at low temperature. The channel length dimension is L=20 nm and the width dimension is W=170 nm.

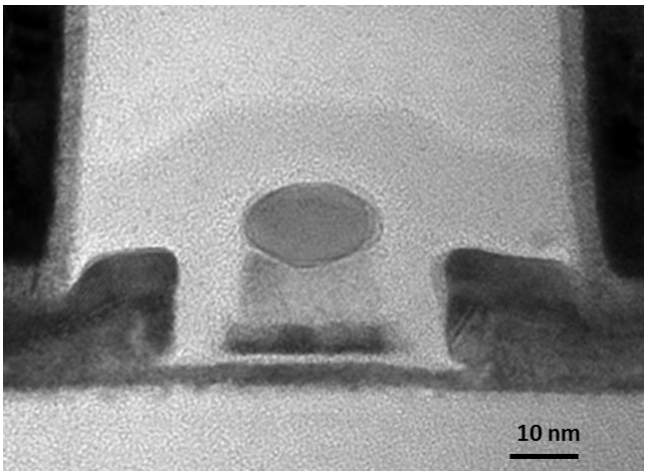



**Figure 3.40: TEM observation of pMOS FDSOI device fabricated with the extension first integration.**

$I_{ON}$-$I_{OFF}$ trade-off for pFET devices with the split table detailed in Table 3.1 is shown in Figure 3.41. In this case, best low temperature split corresponds to Medium PAI dose, showing a slight performance (-5%) degradation compared to the process of reference. Higher performance degradation (around -20%) is found for No PAI and High PAI. Extremely poor performance is observed for no Implant split. In the case of pFET the offset spacer is quite thick (around 10 nm), thus a higher performance degradation compared to the POR is expected compared to the nFET case. As for nMOS case, performance degradation is reflected in access resistance trend. However, for pMOS, as indicated in Figure 3.25, no significant variation in unsalicided $R_{SHEET}$ among POR and low temperature devices (except that for High PAI split) can justify the access resistance degradation highlighted in Figure 3.42.

Salicided sheet resistance values are then reported in Figure 3.43. High sheet resistance degradation for High dose PAI compared to POR is reported, consistent with the trend found on unsalicided $R_{SHEET.}$ However, around 30% degradation in salicided $R_{SHEET}$ value is obtained for No Implant, No PAI and Medium PAI cases with the respect to POR. It is worth remembering that for the POR, p-type epitaxy consist in SiGe:B and a silicon capping while low temperature splits SiGe:B epitaxy is only present. Salicided sheet resistance on SiGe is than higher than on silicon. However, no significant performance loss can be explained by the degradation of the salicided sheet resistance.

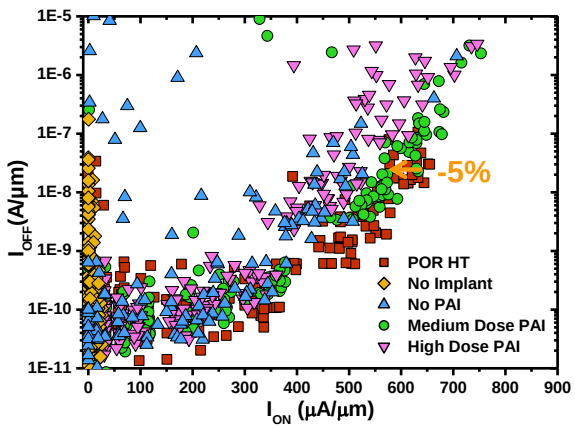



**Figure 3.41: $I_{ON}$-$I_{OFF}$ performance of low temperature extension first pFET devices compared with HT-POR 14 nm FDSOI for different PAI conditions.**

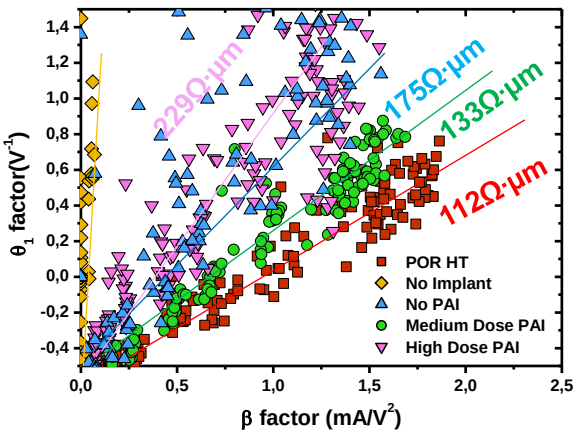



**Figure 3.42: $R_{SD}$ resistance extraction of pFET devices.**

$R_{ON}$-DIBL trade-off for 20 nm gate length devices is reported in Figure 3.44. Slight $R_{ON}$ degradation is shown for Medium PAI split compared to the high temperature device, consistent with access resistance trend of Figure 3.45. However, not negligible DIBL increase is evidenced for Medium PAI case. DIBL is then reported as a function of the gate length in Figure 3.44. For all the low temperature devices, the DIBL is found to be higher than the process of reference. For no implant split, the current values are so poor that no extraction is possible for this parameter. As discussed in chapter two, high DIBL values indicate overlapped junction, that means that too high active dopant concentration is present into the channel region, reducing the electrical gate length. From Figure 3.45, a difference in the electrical gate length of ΔL=2 nm is estimated for no PAI and Medium PAI splits compared to high temperature process of reference. Even higher ΔL=3 nm is extracted for High PAI split. It can be concluded that extension first conditions have not been well optimized considering the horizontal direction of the junction shape, obtaining devices in overlap configuration.

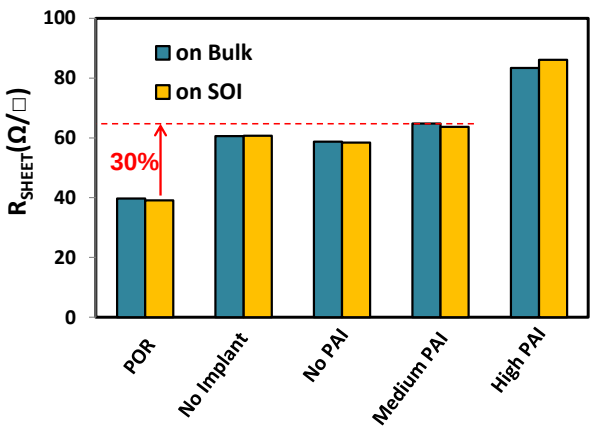



**Figure 3.43: $R_{SHEET}$ measurements on bulk and SOI salicided p-type structures for splits detailed in in Table 3.2.**

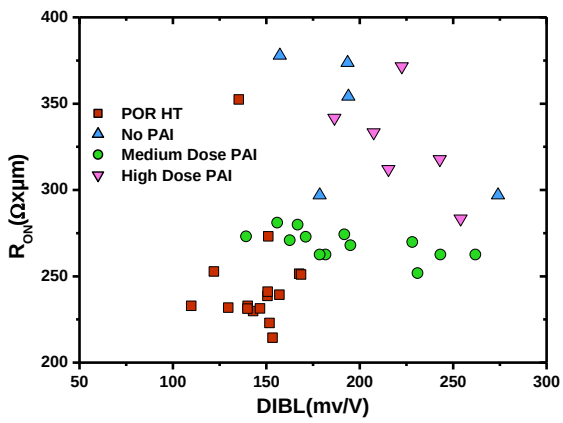



**Figure 3.44: $R_{ON}$-DIBL for pFET devices with 20 nm channel length. Split tables is detailed in Table 3.2.**

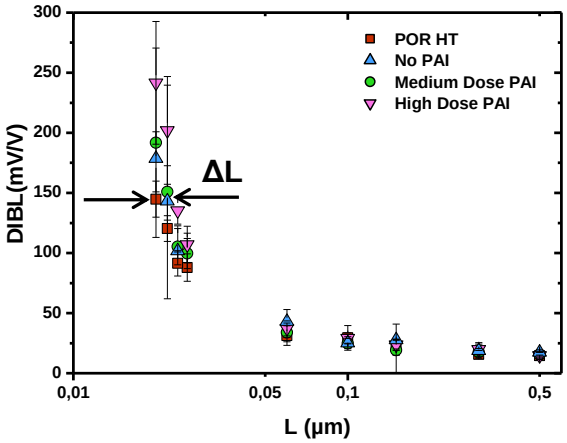



**Figure 3.45: DIBL for different channel lengths and ΔL extraction for pFET devices on Table 3.2.**

### 3.6.4 pFET conclusion and perspectives

High performance pFET device fabricated at low temperature with extension first scheme have been obtained. According to the high DIBL value, the main problem of pFET low temperature device appears to be related to the short channel effect. A possible solution could be the implantation without the use of the nitride capping. In this case, no implantation tilt is needed and more abrupt junctions can be obtained.

Since boron activation in SiGe.B is efficient even without subsequent spike and DSA anneals, the slight performance degradation looks related to the region below the spacer. A first idea to improve $R_{SPA}$ value is to position dopants all along the film depth, while with activation by SPER the doping activation is efficient only in the few amorphized nanometers. This can be made by the use of heated implantation technique in combination with anneals such as DSA. Heated implantation technique will be fully investigated in chapter four.

## 3.7 Conclusion of the chapter

In this chapter, extension first integration scheme for low temperature device optimization has been implemented on the 14 nm FDSOI technology.

First, the standard process flow of the state of the art technology has been presented. The modification related to the low temperature extension first implementation have been detailed as well.

The extension first integration faces to different technological challenges:

- The implantation conditions definition for the amorphization of an extremely thin region (around 3 nm) on a thin film of 6 nm. With the support of KMC simulation and the verification by TEM observation, extension first implantation conditions have been defined for phosphorus and boron using germanium as pre-amorphizing specie. Higher focus has been made on the

definition of doping conditions using a nitride capping of around 3 nm on the surface of silicon film. This allow to use higher implantation energy, compatible with the specification of the available implantation tool.

- The activation level of the thin implanted film has been evaluated. Consistent results have been found for SiGe film implanted with boron using different techniques such as four points probe method, Hall effect and ECV. High sheet resistance values have been obtained for phosphorus implanted film. The presence of nitrogen introduced by recoil could explain this unexpected value. A dedicated study is currently ongoing.
- The epitaxial growth on implanted film is another important challenge. Some issues have been found especially on the SiC:P growth on implanted film, related to the high pre-amorphization dose. However, the feasibility of the process step has been demonstrated for both n and p type.

Finally, electrical analysis of the FDSOI devices fabricated with the low temperature extension first process flow have been presented. High performance devices have been obtained for both nMOS and pMOS indicating the extension first integration as a promising candidate for the development of low temperature devices. Detailed conclusion and perspectives are discussed in sections 3.6.2 and 3.6.4.

## References


[Chang 14], R. D., & Lin, C. H. (2014). Deactivation of phosphorus in silicon due to implanted nitrogen. *physica status solidi (c)*, *11*(1), 24-27.

[Gonzatti 10] Gonzatti, Frederic, et al. "Plasma Implantation Technology for Upcoming Ultra Shallow and Highly Doped Fully Depleted Silicon On Insulator Transistors."*ION IMPLANTATION TECHNOLOGY 2101: 18th International Conference on Ion Implantation Technology IIT 2010*. Vol. 1321. No. 1. AIP Publishing, 2011.

[Haond 15] Haond, M. "Fully depleted SOI: Achievements and future developments."*Ultimate Integration on Silicon (EUROSOI-ULIS), 2015 Joint International EUROSOI Workshop and International Conference on*. IEEE, 2015.

[Haynes 95] T. E. Haynes, M. J. Antonell, C. Archie Lee and K. S. Jones. Composition dependence of solid-phase epitaxy in silicon-germanium alloys: Experiment and theory. Phys. Rev. B, vol. 51, pages 7762–7771, Mar 1995.

[Joelsson 97] Joelsson, K. B., et al. "Hall factor and drift mobility for hole transport in strained Si1− xGex alloys." *Journal of applied physics* 81.3 (1997): 1264-1269.

[Manku 93], Manku, Tanjinder, et al. "Drift hole mobility in strained and unstrained doped Si 1-x Ge x alloys." *Electron Devices, IEEE Transactions on* 40.11 (1993): 1990-1996.

[Maruno 01] Maruno, Shigemitsu, et al. "A Chemical Mechanism for Determining the Influence of Boron on Silicon Epitaxial Growth." *Japanese Journal of Applied Physics* 40.11R (2001): 6202.

[Masetti 83] G. Masetti, M. Severi, and S. Solmi. "Modeling of carrier mobility against carrier concentration in arsenic, phosphorus, and boron-doped silicon." Electron Devices, IEEE Transactions on 30.7 (1983): 764-769.

[Morita 14] Morita, Yusuke, et al. "Improvement of epitaxial channel quality on heavily arsenic-and boron-doped Si surfaces and impact on tunnel FET performance."*2014 44th European Solid State Device Research Conference (ESSDERC)*. 2014.

[Payet 16] Payet, Anthony, et al. "Damage accumulation during cryogenic and room temperature implantations in strained SiGe alloys." *Materials Science in Semiconductor Processing* 42 (2016): 247-250.

[Pivac 92] Pivac, B., et al. "Boron accumulation at epi-substrate silicon interface during epitaxial growth." *Materials Science and Engineering: B* 15.1 (1992): 32-36.

[Probion] Electrochemical CV Profiling tutorial, available at http://probion-analysis.com/en/94-tutoriaux/144-ecvp-tutorial.

[Weber 15], Weber O., et al. "14nm FDSOI upgraded device performance for ultra-low voltage operation." *VLSI Technology (VLSI Technology), 2015 Symposium on*. IEEE, 2015.

# Chapter 4: Heated Ion Implantation

As discussed in chapter 2, one of the main challenges for low temperature devices optimization is to place active dopants in the region below the first spacer. The solution proposed in chapter 3 is the extension first integration scheme, in which dopant implantation is performed directly into the thin semiconductor film before the epitaxy of the raised source and drain. This allows to avoid underlap devices, or full amorphization of the access regions. As explained in chapter one it is essential to avoid full access amorphization in order to preserve a crystalline seed that can act as a pattern for the recrystallization by low temperature solid phase epitaxy. An alternative way to place dopants in depth without full amorphization of the film is the heated ion implantation. In this chapter, literature review on hot implantation including basic physical mechanisms and applications is discussed. First, a study to evaluate the as-implanted dopant activation level and the activation with SPER is discussed. Finally, some electrical results will be provided using heated implantation in extension last integration on 28 nm FDSOI technology and extension first Integration on TriGate devices.

## 4.1 Literature review

For a given ion specie and temperature, a threshold dose is required to produce a continuous amorphous layer in the crystalline silicon. This dose is lightly sensitive to the implantation energy. A relationship between the threshold amorphization dose and the implantation temperature can be found on [Morehead 72] and [Onoda 14] for P, As, $BF_2$ and Sb. For the implantation dose range used for the purposes of this work (around $1x10^{15}$ at/cm$^2$) [Onoda 14] assumes that no amorphization is reached for temperature higher than 300 °C.

The heated implantation technique involves heating the substrate during implantation and is very effective for suppressing implant induced amorphous layer formation. The hot implant temperature increases the recombination of Frenkel pairs during the implantation step and therefore not much crystalline damage is produced. As an example, cross-sectional TEM observations of arsenic (20 KeV, $10^{15}$at/cm$^2$) as-implanted samples at room temperature, 300°C and 600°C are shown in Figure 4.1. Room temperature sample shows a thick amorphous silicon layer, which is absent in the 300°C and 600°C samples. Nevertheless, thick density of defects is formed instead. This indicates that silicon crystallinity is maintained during implantations over 300°C.

Recently, hot implants are gaining attention for FinFET technologies [Wood 13], [Khaja 14], [Mizubayashi 13], [Sasaki 15], [Togo 13]. In FinFET structures, high dose implantations are used in source drain extension formation. These implantations cause amorphization of the silicon fins, which, in turns, results into a difficult regrowth of amorphized silicon fins during successive activation annealing. For further scaling, fin width becomes narrower (dimension of 8 nm are approximately achieved for the 14 nm technological node), and regrowth from remained bottom crystal seed becomes challenging. Amorphized silicon fin cannot be easily regrown during activation annealing and regrowth from crystal channel regions produces defects in the fin, resulting in twin formation and/or poly crystals. This issue is particularly severe for SOI FinFETs. The implementation of heated implants suppresses fin crystalline damage and avoids fin amorphization maintaining fin crystallinity after

anneal when high dose implants are performed. Examples [Wood 13] of fin after room temperature and heated Implantation are shown in Figure 4.2a and 4.2b respectively.

The examples presented so far show the interest of hot implantation in introducing dopants without full amorphization of the access region is known in the literature. Before implementing similar concepts in electrical devices, a more elementary study is carried out in order to familiarize with the properties of heated implantation.

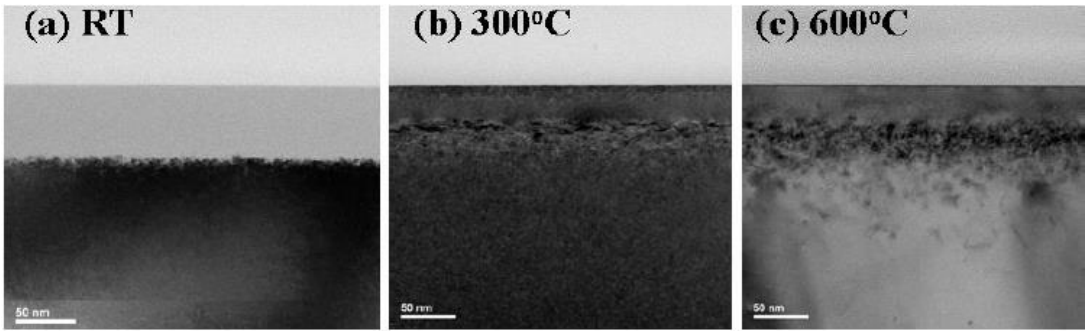



**Figure 4.1: Cross sectional TEM results of As implanted at (a) RT, (b) 300 °C and (c) 600 °C [Onoda 14].**

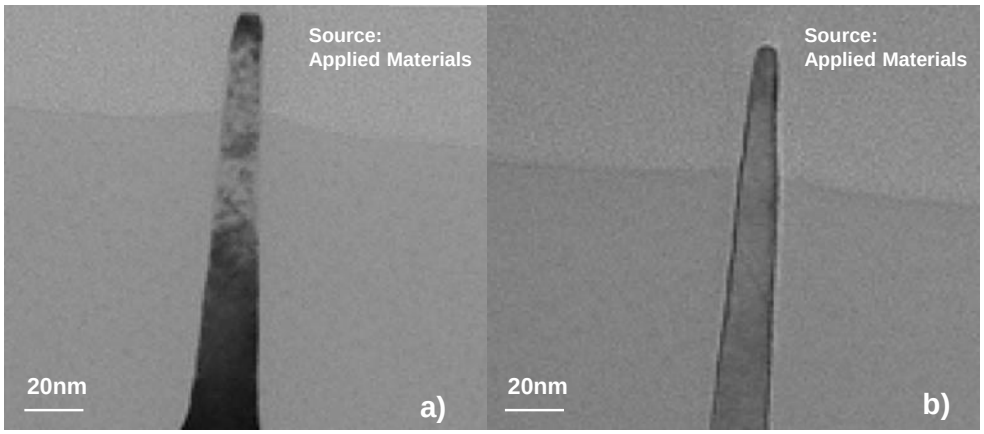



**Figure 4.2: TEM observation after a) room temperature implantation; b) heated implantation [Wood 13].**

## 4.2 Hot implant properties extraction

In this section, the results of a basic study on hot implantation of boron, phosphorus and arsenic are provided. Three main results are discussed: the validity of doping profile predicted by KMC simulations compared to experimental SIMS; the activation level for B, P and As as-implanted, the activation level after heated implantation with SPER activation.

### 4.2.1 Doping profile by Hot Implantation

The definition of doping conditions is commonly made by KMC simulation. A significant difference on the as-implanted profile is predicted by simulation depending on the implantation temperature as reported in Figure 4.3. Although the validity of KMC simulation in the prediction of doping profile for room temperature implant is well established, for the hot implantation technique no exhaustive information is yet available at our knowledge.

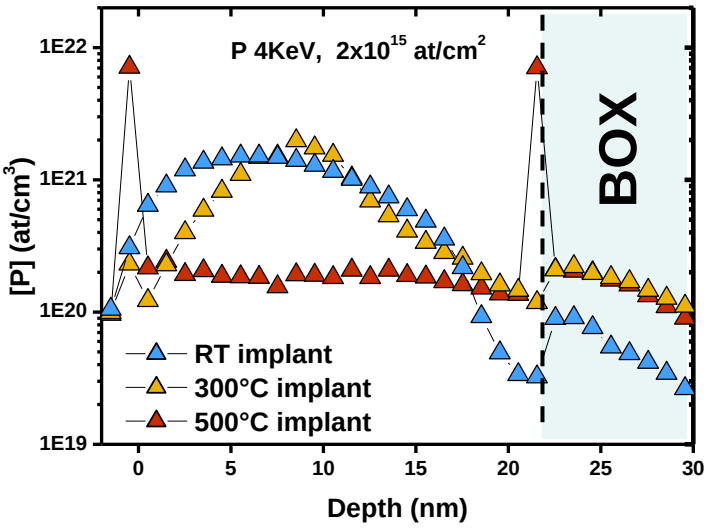



**Figure 4.3: Phosphorus profiles obtained by KMC simulation for different implantation temperatures (RT, 300 °C, 500 °C). Significant differences in profile shape are observed.**

For these reasons, a comparison between doping profile obtained by SIMS and simulation results has been carried out for hot implant using boron, phosphorus and arsenic. Ion implantations have been made in bulk blanket silicon wafers. Simulated and experimental doping profiles extracted by SIMS are reported in Figure 4.4 (a, b and c) for boron, phosphorus and arsenic respectively. For all three cases, simulation profiles are in acceptable agreement with experimental results. In particular, boron simulated profile describes quite well the one measured by SIMS in all the concentration range $10^{18}$ - $2x10^{21}$ at/cm$^3$. Phosphorus distribution tail is well represented by simulations, but SIMS result shows a significant surface segregation not predicted at all by simulation. For arsenic, distribution tail (< $10^{18}$ at/cm$^3$) is not well described by simulation results while minor difference is observed in the high concentration part of the distribution. In general, good agreement for all the three species is found in the concentration range $10^{19}$ - $2x10^{20}$ at/cm$^3$.

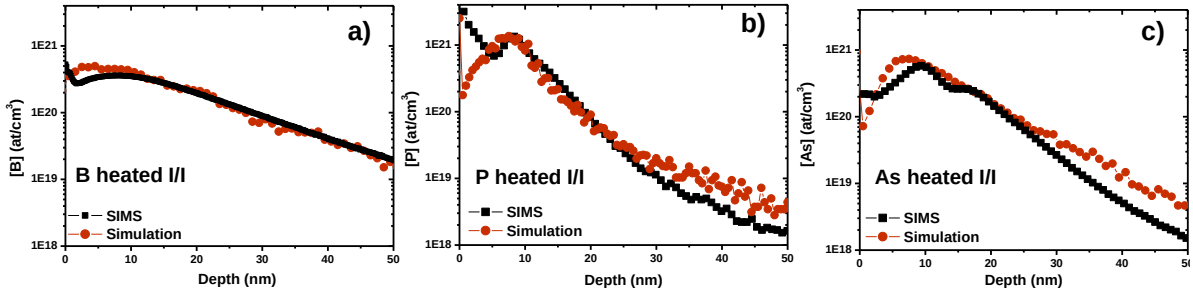



**Figure 4.4: Dopant profile comparison between SIMS and simulation for a) Boron; b) Phosphorus; c) Arsenic hot implantation (500 °C).**

### 4.2.2 Activation level post hot implantation

Even though the one-dimensional simulated doping profile does not perfectly match with the simulation results obtained by SIMS, for the purpose of this work, doping profile obtained by simulation can be considered reliable. In fact, in the doping concentration range $10^{19}$ - $2x10^{20}$ at/cm$^3$, that is the most important in terms of dopant activation and sheet resistance results, is well represented for all the dopant species discussed in this study.

Sheet resistance measurements by the four points method and Hall effect measurements have been performed on as-implanted samples with different implantation conditions. Hot implantations in bulk structures have been made in p-type wafers for arsenic and phosphorus doping and in n-type wafers for boron doping. For both n and p wafer type, the doping concentration is approximately $10^{15}$ at/cm$^3$. This choice is made to create a p-n junction that is required to isolate the contribution of the implanted zone from the substrate during the sheet resistance measurement.

| | Energy (KeV) | Dose (at/cm$^2$) |
|---|---|---|
| Condition 1 | 4 | $3x10^{14}$ |
| | 2 | $8\ x10^{14}$ |
| Condition 2 | 3 | $7\ x10^{14}$ |
| | 5 | $1\ x10^{15}$ |
| Condition 3 | 3 | $1.5\ x10^{15}$ |
| | 4 | $2\ x10^{15}$ |

**Table 4.1: Boron implantation conditions corresponding to doping profiles of Figure 4.2.**

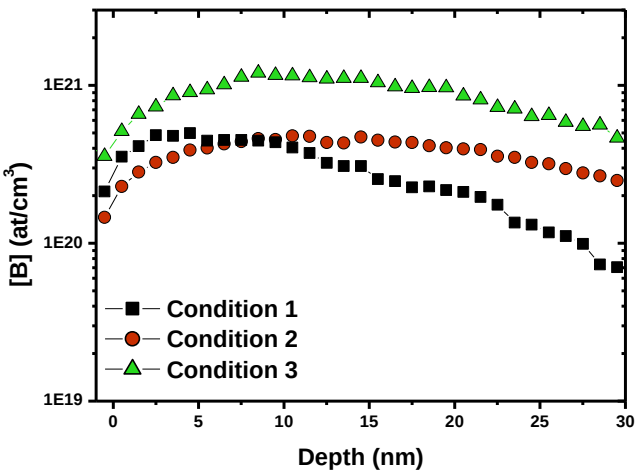



**Figure 4.5: Boron doping profiles of implant conditions detailed in Table 4.1.**

**Boron**

Implant conditions of the tested samples, corresponding to the doping profiles illustrated in Figure 4.5 are detailed in Table 4.1. For boron, all the implants have been made at 400 °C. Double boron implantation has been performed for the three cases in order to obtain a smooth profile along vertical direction. All simulation profiles have been extracted considering a bulk silicon substrate.

Sheet resistance measurements have been performed on bulk silicon wafer. Condition 3 has been tested on SOI substrate as well. However, $R_{SHEET}$ measurements failed for condition 1 and 2 and a really high value of 35 KΩ/□ (on bulk) and 24 KΩ/□ (on 16 nm SOI) is found for condition 3. Considering the SOI structure and assuming the junction depth as the total silicon thickness, an activation level of $1x10^{18}$ at/cm$^3$ is found, under the hypothesis that the carrier mobility corresponds to the one at thermodynamic equilibrium reported in [Masetti 83]. In order to verify this hypothesis, Hall effect measurements have been performed on the SOI sample. The sample thickness has been considered 16 nm according to the total silicon film thickness. Active dopant concentration and carrier mobility measured by Hall effect are compared to the values extracted by sheet resistance measurement under the hypothesis of thermodynamic equilibrium and are reported in Figure 4.6. Higher active concentration ($5x10^{18}$ at/cm$^2$) is measured compared to the previous estimation, but mobility measurements show significant degradation compared to the value at thermodynamic equilibrium. Mobility is probably affected by the presence of charged defects created by heated implantation that influences the carrier transport.

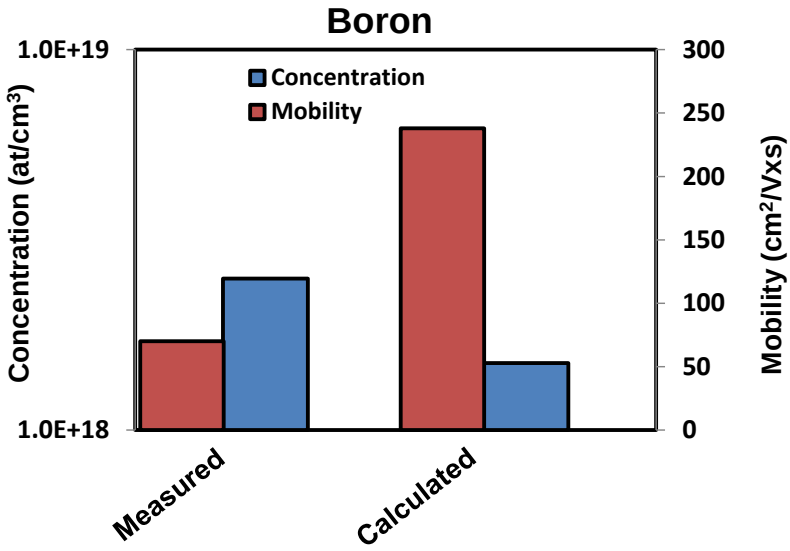



**Figure 4.6: Carrier concentration and mobility measured by Hall effect and deduced from sheet resistance measurement for SOI sample with boron heated implantation.**

**Phosphorus**

One single doping condition has been tested for phosphorus case. Phosphorus implant has been made with an energy of 5 KeV and a dose of $2x10^{15}$ at/cm$^2$ at 500 °C. The doping profile is reported in Figure 4.4b. In this case $R_{SHEET}$ is measurable with values reported in Figure 4.7. $R_{SHEET}$ value on bulk structure (733 Ω/□) is significantly lower than on SOI (1.3 KΩ/□). This can be easily explained by the tail profile

over 16 nm (corresponding to the thickness of the SOI wafer) that contributes to the reduction of $R_{SHEET}$ according to equation (3.1). Active concentration is extracted to $3.5x10^{19}$ at/cm$^3$, slightly smaller than the measured value $5x10^{19}$ at/cm$^3$. As in boron case, mobility appears to be slightly degraded compared to the thermodynamic value (Figure 4.8).

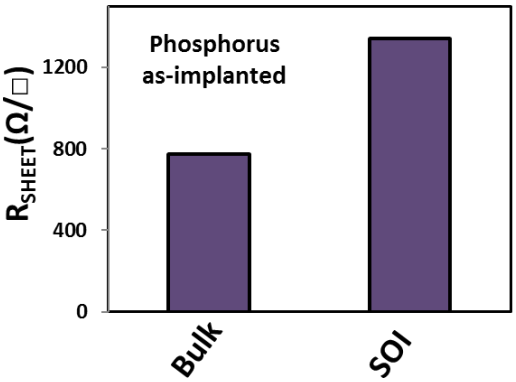



**Figure 4.7: Sheet resistance measurements post phosphorus hot implantation on bulk and SOI substrates.**

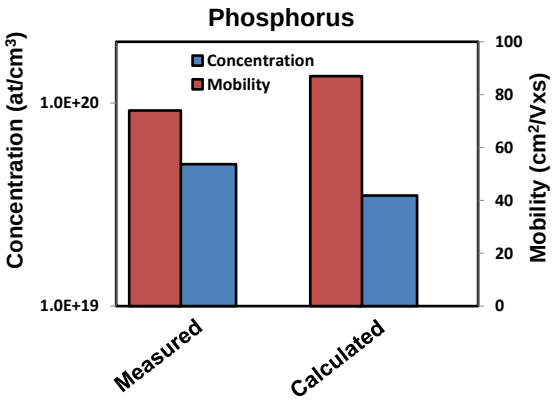



**Figure 4.8: Carrier concentration and mobility measured by Hall effect and deduced fropm sheet resistance measurement for SOI sample with phosphorus heated implantation.**

## Arsenic

Finally, similar tests have been carried out on arsenic implanted wafers. Three doping conditions have been tested on bulk structures (Table 4.2). Condition 3 has been tested on SOI wafer as well. The doping profiles have been simulated considering bulk substrate and are reported in Figure 4.9. All the implantations have been made at 450 °C.

| | Energy (KeV) | Dose (at/cm$^2$) |
|---|---|---|
| Condition 1 | 7.5 | $2x10^{15}$ |
| Condition 2 | 8 | $1x10^{15}$ |
| Condition 3 | 7 | $5x10^{14}$ |
| | 15 | $5x10^{14}$ |

**Table 4.2: Implant conditions details for arsenic hot implantations.**

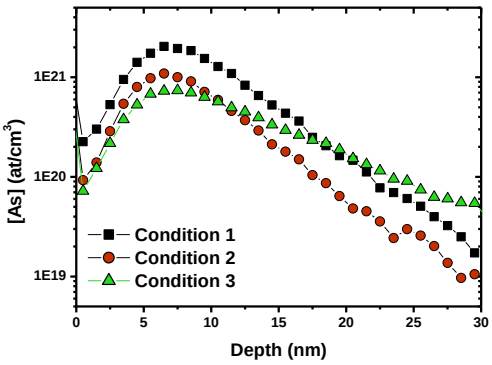



**Figure 4.9: Arsenic doping profiles of implant conditions detailed in Table 4.2.**

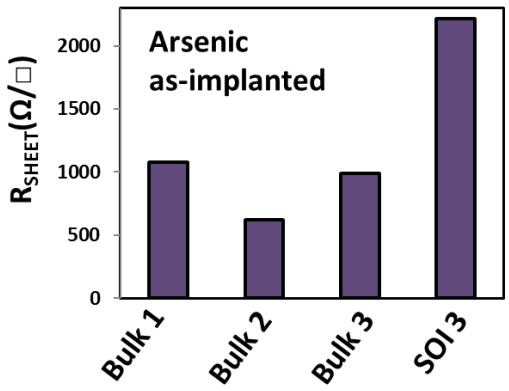



**Figure 4.10: Sheet resistance measurements post Arsenic hot implantation on Bulk and SOI substrates.**

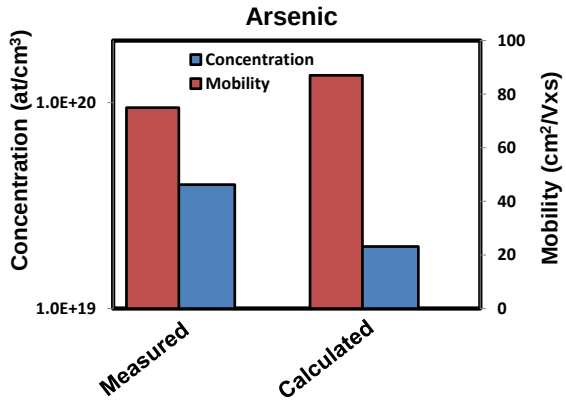



**Figure 4.11: Carrier concentration and mobility measured by Hall effect and deduced form sheet resistance measurement for SOI sample with arsenic heated implantation.**

Sheet resistance measurements could be performed and gave reliable results reported in Figure 4.10. Best sheet resistance value is found (619 Ω/□) for condition 2, which corresponds to the higher implanted dose. As for the phosphorus case, considering the SOI substrate, activation level for arsenic is extracted at $2x10^{19}$ at/cm$^3$, that is slightly lower than the one extracted for phosphorus. It seems that hot implantation leads to a better activation level for phosphorus compared to arsenic. As for the other dopants, experimental measurements (Figure 4.11) show a little higher concentration ($3x10^{19}$ at/cm$^3$) and a mobility degradation, suggesting, for all the dopants that the presence of charged defects due to the heated implantation could affects the carrier mobility.

### 4.2.3 SPER activation level of heated implantation

After evaluating the as-implanted activation level of hot implantation, the combination of SPER activation with hot implantation was studied. The interest of using hot implantation in combination with dopant activation by SPER will be clarified in the integration scheme proposed for FDSOI electrical devices discussed in section 4.3.

Bulk silicon substrates have been implanted with boron, phosphorus and arsenic at high temperature, with the conditions presented in the previous section. After the hot implantation, the wafers have been implanted with germanium 10 KeV-$5x10^{14}$ at/cm$^2$ in order to obtain 19 nm of amorphous silicon. Afterwards, a thermal annealing of 2 minutes at 600 °C has been applied in order to get re-crystallization and dopants activation by SPE.

Sheet resistance measurements have been performed on the re-crystallized wafers and the results are shown in Figure 4.12 and 4.13 for boron and arsenic respectively. For both boron and arsenic, sheet resistance values are consistent with the results reported in chapter one for SPER activation with room temperature implantations. The result is confirmed also for phosphorus obtaining a $R_{SHEET}$=200 Ω/□ after hot implant and SPER activation. Nevertheless, it is still interesting for the purpose of this work as will be explained in next sections. Figure 4.14 summarizes the sheet resistance values obtained by different methods. It can be concluded that the activation level after SPER is the same whatever the

temperature of implantation. Nevertheless, heated implantation remains interesting for the purpose o this work as will be explained in next sections.

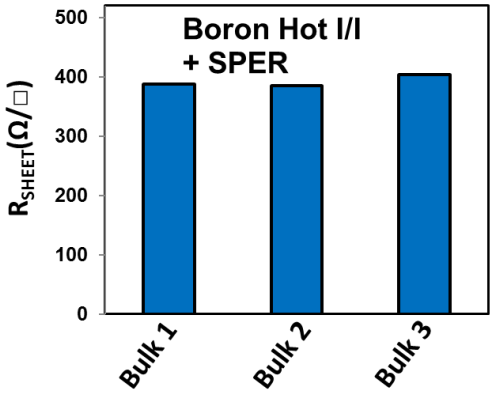



**Figure 4.12: Sheet resistance measurements post boron hot implantation and SPER activation.**

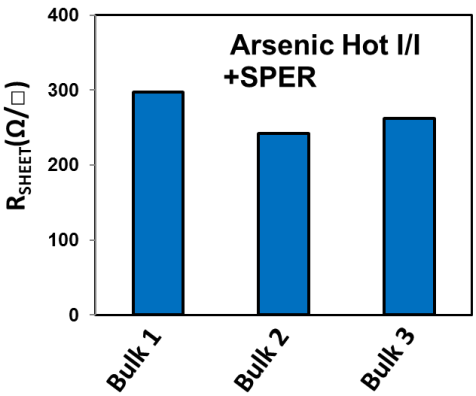



**Figure 4.13: Sheet resistance measurements post arsenic hot implantation and SPER activation.**

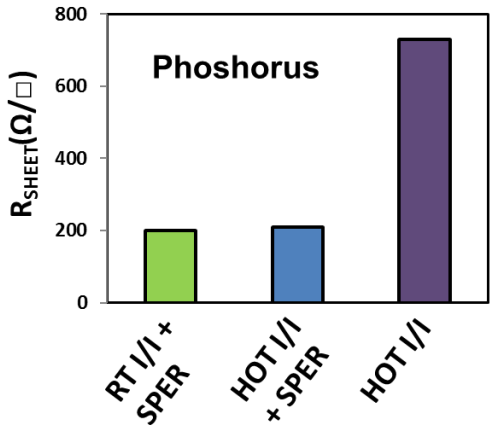



**Figure 4.14: Comparison of sheet resistance measurements on SOI substrate after SPER activation with room temperature implant, SPER with hot implantation and heated implantation only.**

## 4.3 Extension last integration on FDSOI and heated implantation

In chapter two, it has been shown that extension first is more adapted for the low temperature devices performance optimization. This is due to the difficulties found in placing active dopants below the gate spacer without full amorphization of the access regions. However, hot implantation represents an interesting solution if the extension last scheme wants to be maintained. In fact, since hot implantation does not lead to amorphization, dopants can be placed all along the access depth. However, in section

4.2.2 it has been shown that activation level is not in the target of the activation level required in source and drain regions of a transistor (> $2x10^{20}$ at/$cm^3$). In particular, as implanted activation level of $3.5x10^{19}$ at/$cm^3$ has been extracted for phosphorus and low activation level <$5x10^{18}$ at/$cm^3$ has been found for boron. Taking into account the advantageous feature of crystallinity preservation during heated implantation, together with the drawback of a bad doping activation level, an alternative process flow is proposed in order to integrate both the advantages of hot implantation and SPER dopants activation.

### 4.3.1 Process flow description

The following integration scheme, with the use of hot implantation, has been proposed and integrated on 28 nm FDSOI technology:

- The standard process flow is used up to silicon epitaxy for raised source and drain.
- Doping step is made by **hot implantation** (phosphorus for nMOS and boron for pMOS).
- **Germanium implant** is performed in order to obtain a 19 nm-thick **amorphous region** in the source and drain
- **Thermal annealing for 1 minute at 600 °C** to obtain re-crystallization and dopant activation by SPE.

A schematic representation of the proposed integration scheme is reported in Figure 4.13.

Two different regions are then created in the access:

- The first zone is the silicon layer of 3 nm at BOX interface (the former crystalline seed) where the doping activation level is equal to the one just after hot implantation. This allows to have some activated dopant without full amorphization in the critical region below the first spacer.
- The source and drain region where the dopants are introduced by hot implant and activated by SPER. In section 4.2.3 it has been demonstrated that activation level corresponds to the case of room temperature implant and SPER activation (discussed in Chapter 1).

A TEM cross section observation of FDSOI fabricated with the process flow proposed in Figure 4.13 is shown in Figure 4.16. It is worth noticing how source and drain region thickness (15.5 nm) is unexpectedly reduced with respect to the target (22.5nm). This aspect will be discussed in detail in section 4.3.4

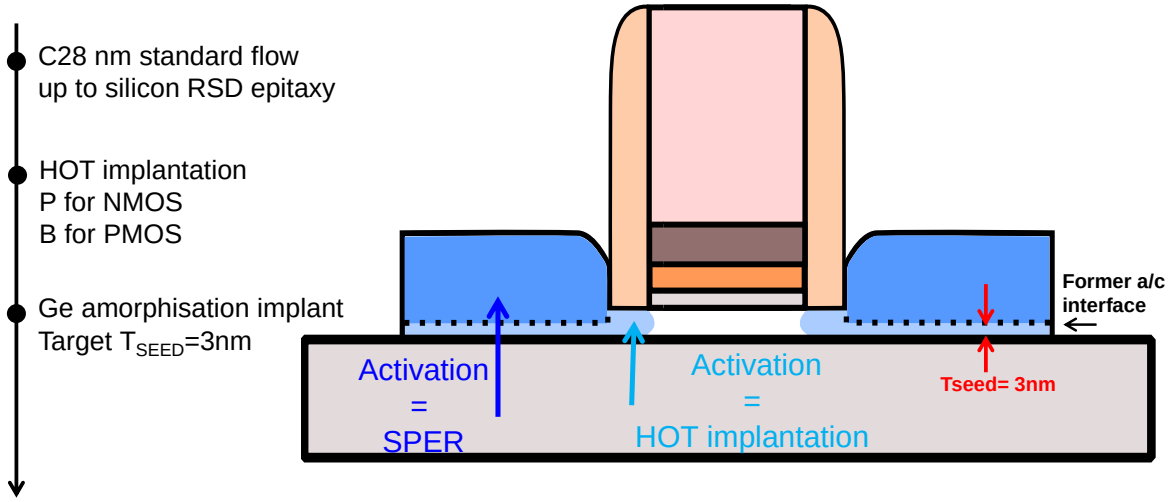



**Figure 4.15: schematic process flow of extension last with heated implantation in combination with amorphization and dopant activation by SPER.**

### 4.3.2 pMOS implant conditions definition

In this section, the electrical characterization of FDSOI pMOS fabricated with the integration scheme proposed in Figure 4.15 is discussed.

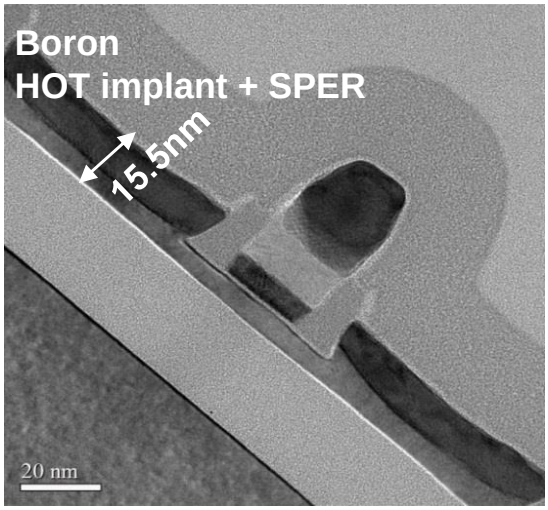



**Figure 4.16: TEM observation of a pMOS FDSOI fabricated using the process flow presented in Figure 4.13.**

The choice of implantation conditions have been carried out using two-dimensional process simulation focusing on the doping position and concentration in the junction zone, below the first spacer. It is important to keep in mind that no information about the calibration of the two-dimensional simulation

for hot implantation are available at our knowledge. As usual, simulation is an important tool that provides the tendency of phenomena instead of an accurate quantitative analysis.

First, same implantation conditions used at room temperature in pMOS low temperature devices shown in section 2.6 have been simulated. The total boron concentration obtained by KMC process simulation is shown in Figure 4.15. A non-negligible doping concentration (>$5x10^{19}$ at/$cm^3$) is present into the channel region. Since hot implantation is expected to activate a certain number of dopants just after the implantation step, the junction shape in Figure 4.17 is not acceptable. In fact, dopants into the channel region can lead to undesired short channel effects. Doping conditions have been modified in order to limit the dopant concentration into the channel region by reducing energy and dose conditions. The new proposed doping conditions correspond to the double boron implant reported below:

B 3 KeV $5x10^{14}$ at/$cm^2$ tilt 0° + B 3 KeV $8x10^{14}$ at/$cm^2$ tilt 0°

that leads to the junction shape represented in Figure 4.18. In this case, doping concentration below $10^{19}$ at/$cm^3$ is present into the channel. However, as exported in one-dimensional doping profile obtained by KMC simulation (Figure 4.19), total boron concentration has been kept around $3x10^{20}$ at/$cm^2$ all along the access depth according with the activation level target. Boron implants have been performed at 450 °C.

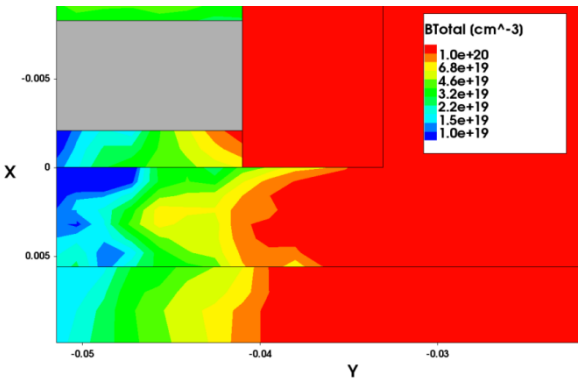



**Figure 4.17: Total boron concentration after heated implantation for the first simulated condition. It has been considered unsatisfying since high dopant concentration is present into the channel region.**

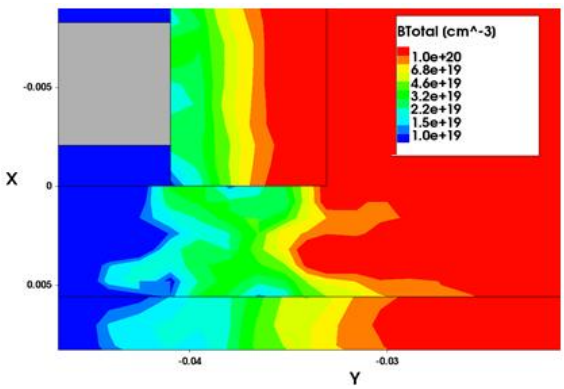



**Figure 4.18: Total boron concentration after heated implantation for the second simulated condition. The dopant concentration below the spacer appears satisfying (around $5x10^{19}$ at/$cm^3$) concentration below $10^{19}$ at/$cm^3$ is present into the channel. This condition is the one chosen for the electrical device.**

As remembered before, simulation results cannot perfectly match to real devices configurations. It is plausible that doping concentration position obtained by simulation and represented in Figure 4.17 and 4.18, does not perfectly describe the reality. Anyway, it has been chosen to reduce the depth of high doping concentration because low temperature devices with room temperature implantation presented in section 2.6 showed already significant short channel effects. The hot implantation can

only aggravate these effects by the as-implanted activation level and dopant diffusion during the implantation performed at 450 °C.

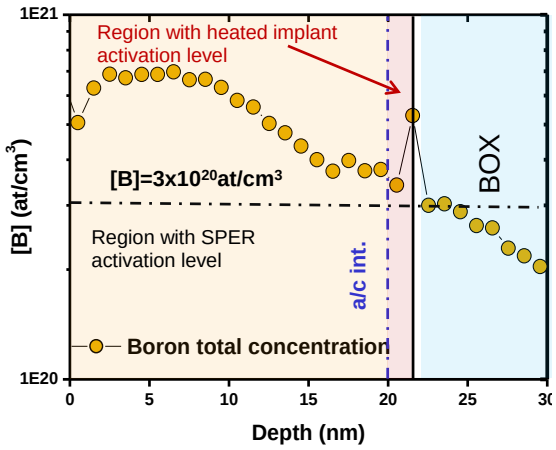



**Figure 4.19: One-dimensional profile of boron implantation conditions chosen for electrical device.**

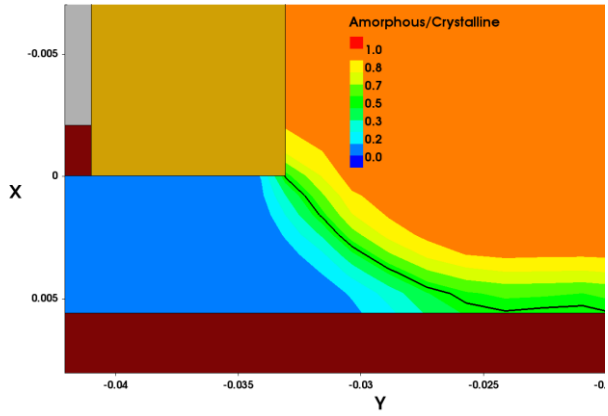



**Figure 4.20: Amorphous/crystalline zone obtained by simulation with the germanium implantation at 11KeV.**

After the boron implantation, germanium implantation with energy of 11 KeV, dose of $5x10^{14}$ at/cm$^2$ and tilt 0° is made to amorphize the access region, leading to the amorphous/crystalline interface position and shape reported in Figure 4.20. However, this condition looks risky in terms of amorphization depth since full amorphization is observed in a part of the access region (the amorphous/crystalline interface touches the BOX). It is worth remembering that if no sufficient crystalline seed is preserved, no crystallization will be achieved by SPE. Moreover, lateral re-crystallization can lead to defective crystalline quality as reported in Figure (2.41). In order to prevent this risk a second condition has been chosen reducing the implant energy from 11 KeV to 10 KeV while keeping the same dose. The two conditions have been used on the two halves of the wafers thanks to half wafer lithography. The impact of these process steps will be discussed in section 4.3.4.

### 4.3.3 pMOS electrical electrical characterization and analysis

In this section, heated implantation split behavior is compared to the high temperature process of reference and low temperature SPER device with room temperature implant. This last split corresponds to the devices analyzed in section 2.6. The tested devices have a width of W=1 µm and gate length ranging from 30 nm to 1 µm.

The $I_{ON}/I_{OFF}$ trade-off normalized at $V_G$-$V_T$ is shown in Figure 4.21. Hot implant split reveals significant performance degradation (-60%) compared to POR and low temperature split with room temperature implant. Access resistance is suspected to be the responsible of the performance degradation and the extraction by Y function is proposed in Figure 4.21. In this case, the extraction method completely fails since for the three cases, no linear fit on the $\beta(\theta_1)$ plot can be found. An alternative method has then

been used to extract the access resistance, so called $R_{TOT}(L)$ method [Chang 07]. It is based on the simple assumption that:

$$R_{TOT}(L)=R_{ACCESS}+R_{CHANNEL}(L) \quad (4.1)$$

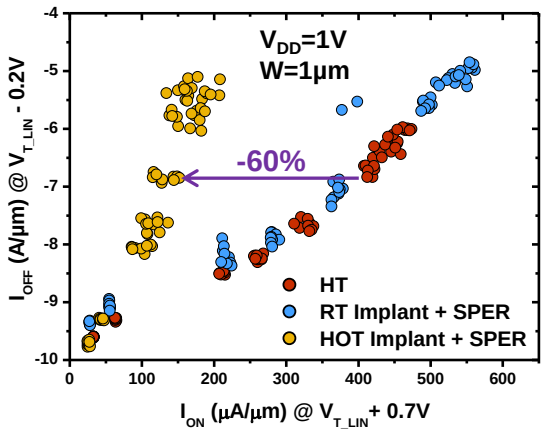



**Figure 4.21: $I_{ON}$-$I_{OFF}$ trade-off performance for hot implant split with respect to high temperature devices and low temperature devices with RT implant.**

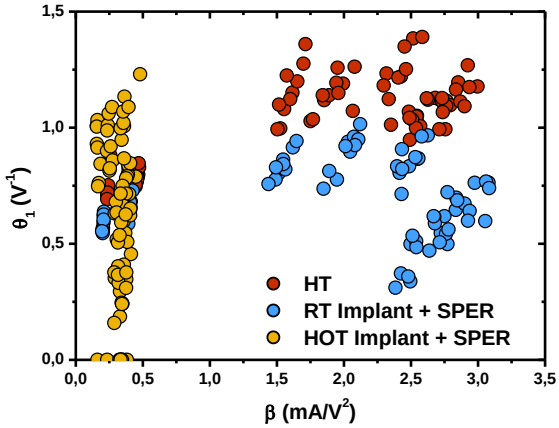



**Figure 4.22: Access resistance extraction by Y function method. In this case, the method completely fails.**

Where the channel resistance $R_{CHANNEL}(L)$ depends linearly on the gate length L. The access resistance $R_{ACCESS}$ is then the intercept of the $R_{TOT}$-L plot at a constant gate overdrive $V_{GS}$-$V_{TS}$=0.7 V. Using this method, an extremely high value of 5.3 KΩxµm is extracted for hot split implant. A typical value of 353 Ωxµm is extracted for low temperature devices with room temperature implant. On the other hand, an unexpected value of 824 Ωxµm is extracted for POR split. Since this access resistance degradation is not reflected in performance difference with room temperature SPER device, it appears more related to a bad fitting extraction. This highlights that the $R_{TOT}(L)$ method cannot be considered accurate. One of the main problem of this method is that no ΔL can be considered and the comparison between the splits is not accurate. However, what is interesting in this discussion is that $R_{ACCESS}$ value for hot implant split is about one order of magnitude higher than the typical values for a FDSOI device. This cannot be related to a bad parameter extraction, but it corresponds to a real degradation in access resistance for hot implant split.

The dopant activation in the source and drain region has been obtained by hot implantation in combination with SPER. In section 4.2.3 it has been verified that the combination of hot implantation and SPER does not lead to any difference in activation level compared to RT implant and SPER. So, the main responsible of access resistance degradation appears to be, most likely, the zone below the spacer where the dopants exhibit the activation level just post implantation, that for boron is really poor ($5x10^{18}$ at/$cm^3$).

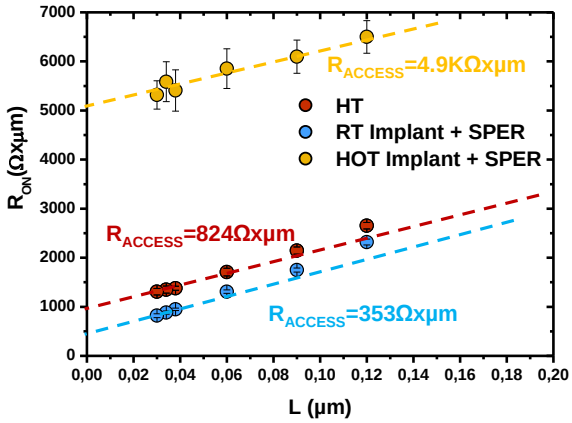



**Figure 4.23: Access resistance extraction by $R_{TOT}(L)$ method. Huge access resistance degradation if found for hot implant split.**

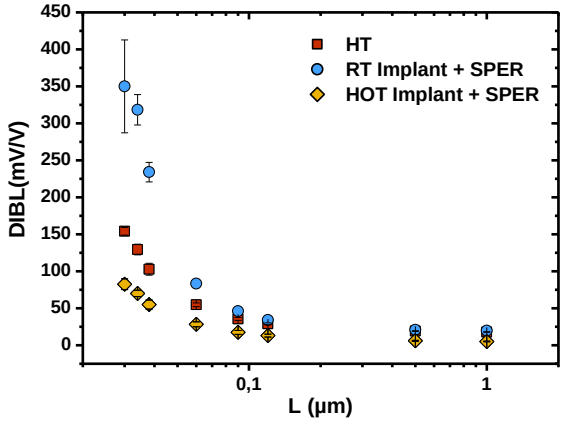



**Figure 4.24: DIBL behavior for different gate lengths. DIBL reduction for hot implant device indicates underlap configuration.**

For these reasons, hot implantation devices are expected to be in severe underlap configuration. This can be observed in DIBL trend, proposed in Figure 4.24. High ΔL of 16 nm can be extracted in comparison with POR.

In section 2.5 it has been shown how in the case of an underlapped device, access resistance has a really high dependence on the applied gate voltage and this leads to a bad extraction of the carrier mobility at low electric field. This is confirmed for the hot implant devices where (Figure 4.25) the carrier mobility starts its degradation at channel length higher than 1 µm. This mobility degradation at long channel does not seem to be a real effect, but a bad parameter extraction by a method that is not suitable for device in underlap configuration.

In conclusion, the bad performance of hot implant devices can be related to an insufficient active dopant concentration below the spacer. This is due to a non-optimized implant conditions used: in fact, in order to avoid the risk of active dopants into the channel, implantation depth was reduced. This has only led to an extremely underlap devices and then to access resistance degradation. The contribution of boron placed below the spacer by hot implantation is very negligible and it did not lead to any visible improvement in access resistance. This analysis is consistent with the low activation level for boron post hot implantation extracted in section 4.2.2.

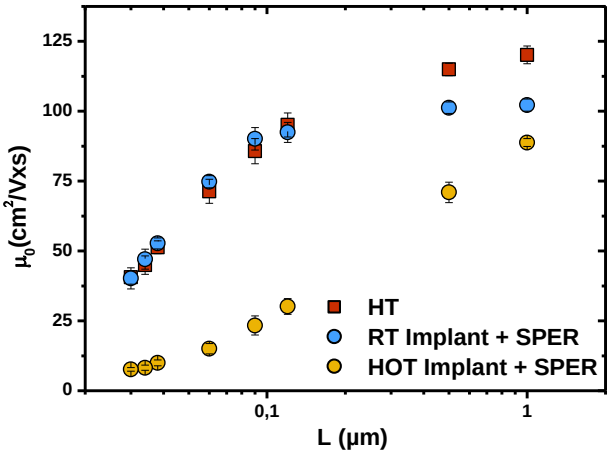



**Figure 4.25: Carrier mobility at low electric filed extraction.**

### 4.3.4 nMOS electrical characterization and analysis

The process flow presented in section 4.3.1 has been implemented to fabricate nMOS device as well. Doping implantation has been defined in order to place an acceptable dopant concentration below the first spacer and keeping the dopant concentration in the access region around 3x10$^{20}$at/cm$^3$.

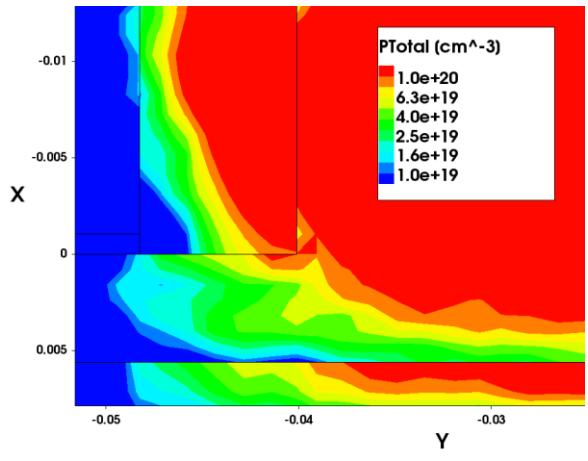



**Figure 4.26: Total phosphorus concentration obtained by simulation in the region below the first spacer.**

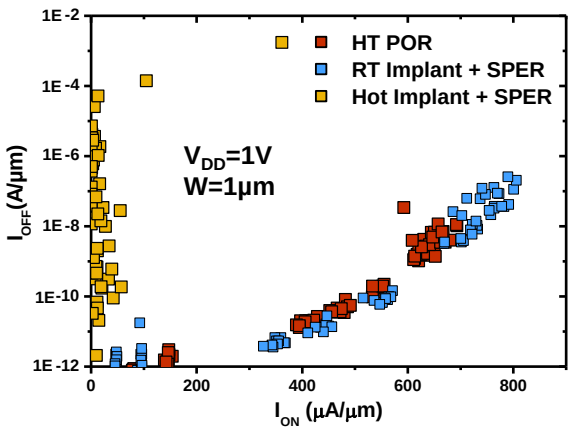



**Figure 4.27: $I_{ON}$-$I_{OFF}$ trade-off for low temperature devices with hot implantation in comparison with high temperature POR and low temperature device with RT implantation.**

In Figure 4.26 simulation results show total dopant concentration in the region below the spacer. nMOS results are expected to be better than pMOS since phosphorus activation level after hot implantation is acceptable for the $R_{SPA}$ target according to section 4.2.2. Unexpectedly, extremely poor results, i.e. low ON current values, for hot implant split are shown in $I_{ON}$-$I_{OFF}$ trade-off presented in

Figure 4.27 for hot implant devices. Further analysis has been carried out in order to explain these bad results.

Useful indications can be extracted by TEM observation on nMOS with heated implantation proposed on Figure 4.28b. After salicidation, the access thickness is 9.5 nm while it is observed at 22.5 nm in the reference case (Figure 4.28a). This silicon reduction gives rise to a full salicidation of the access region that it is evidenced on the TEM image of Figure 4.28b. Full access salicidation is detrimental for transistor performance because it leads to silicide/silicon contact resistance ($R_{CO}$) degradation. $R_{CO}$ degradation can be explained by two reasons:

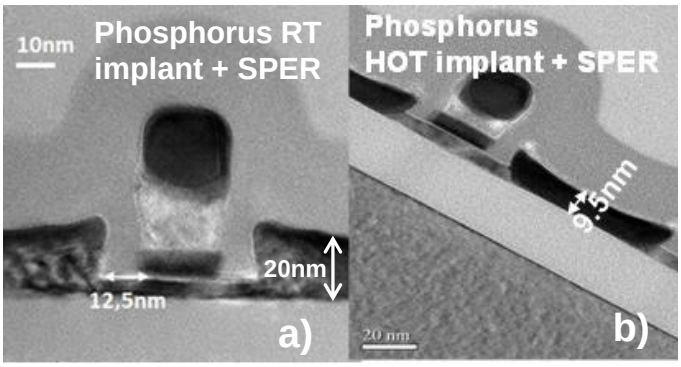



**Figure 4.28: TEM observation for nMOS fabricated by extension last integration and a) RT implantation b) hot implantation followed by SPER. In this last observation, full silicidation is evidenced.**

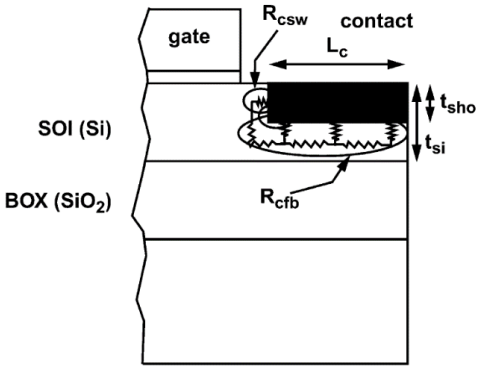



**Figure 4.29: Schematic representation of the two resistance components associated to the silicide/silicon contact resistance. $R_{cfb}$ and $R_{csw}$ are flat-bed and side-wall contributions, respectively [Dubois 02].**

i) The salicide/silicon interface is placed on silicon film at first spacer edge which is a not well doped silicon region. In fact, the activation level of the silicon film region corresponds to the one post hot implantation, extracted for phosphorus at $3x10^{19}$ at/cm$^3$. The silicide/silicon contact resistance is extremely dependent on the doping concentration of the semiconductor zone as reported in [Swirhun 88]. In particular, an order of magnitude reduction in the doping concentration can lead to up to three order of magnitudes of degradation on the contact resistivity.

ii) As reported in [Dubois 02] the contact resistance can be divided into two components associated in parallel named flat band $R_{cfb}$ and side-wall $R_{csw}$. The configuration is schematically represented in Figure 4.29. If the silicide completely consumes the silicon thickness as in the case of Figure 4.28b, no $R_{csw}$ contribution is present and the overall silicide/silicon contact resistance will be highly degraded.

The combination of these two effects can explain the poor ON current values shown in the $I_{ON}$-$I_{OFF}$ trade-off presented in Figure 4.27.

Another interesting feature can be observed on the $I_{ON}$-$I_{OFF}$ plot: some heated implant devices show quite high $I_{OFF}$ value (around $10^{-4}$ A/µm) inconsistent with a FDSOI transistor in MOSFET behavior. In

order to explain this effect of high leakage current, several devices have been tested singularly. In Figure 4.30 the $I_{DS}$-$V_{GS}$ characteristics of two transistors devices measured on different wafer locations, but with same geometry (W=1 µm and L=1 µm) are shown: in one case typical MOSFET behavior is observed, in the other case, symmetric behavior suggest that devices are in Schottky configuration. Schottky behavior explains the high $I_{OFF}$ value, in facts for $V_{GS}$=0 V, the transistor is on "ON state" for p-type conduction and the $I_{OFF}$ values is approximately 7 order of magnitudes higher than a standard MOSFET behavior. The two different behaviors can be explained by the different position of the silicide/silicon interface, due to the silicon thickness variability of the raised source and drain regions. If metal/semiconductor interface is far enough from the channel, a p/n junction is formed between access and channel and typical field effect transistor behavior appears. If salicide/silicon interface is so close to the channel that carrier injection is made by tunneling directly into the channel, Schottky behavior appears.

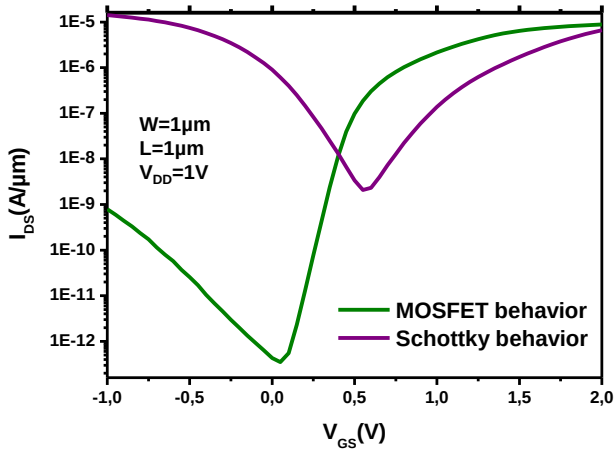



**Figure 4.30: $I_{DS}$ ($V_{GS}$) of two n-type device with same geometry on the same wafer. One first typical MOSFET behavior and the other Schottky behavior.**

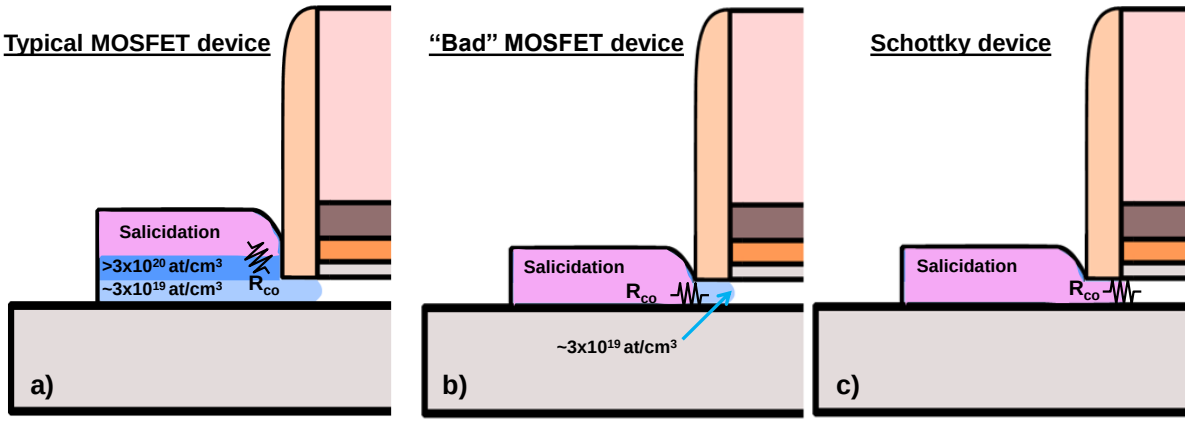



**Figure 4.31: Device configuration depending on the position of salicide/silicon interface: a) MOSFET device; b) MOSFET device with performance degradation due to high salicide/silicon contact resistance; c) Schottky device.**

Figure 4.31 schematically represents three different devices configuration depending on the salicide/silicon interface position. In case a) typical MOSFET behavior will be found. In case b) devices will show MOSFET behavior, but with low current value due to the high salicide/silicon contact resistance. In case c) typical Schottky device configuration is observed.

### 4.3.5 Si consumption by etching after hot implantation

Three full sheet SOI wafers have been implanted by heated implantation at 500 °C using threes difference dopant species: boron, phosphorus and antimony. The silicon film measures approximately 6.5 nm. The heated implantation has been made through a capping nitride layer of 7 nm. After the nitride removal, TEM observations have been performed on the implanted samples and the results are reported in Figure 4.32. Good crystalline quality is observed in the silicon film as expected after heated implantation. However, anomalous silicon consumption and significant oxidation is observed. In particular, 1 nm of silicon consumption is observed for boron implanted sample while a consumption of 2 nm and 4 nm are observed for phosphorus and antimony samples respectively. It seems that the silicon thickness consumption increases as the atomic mass of the implanted specie increases. This suggests that silicon oxidation is dependent on the density of defects created in surface by the heated implantation.

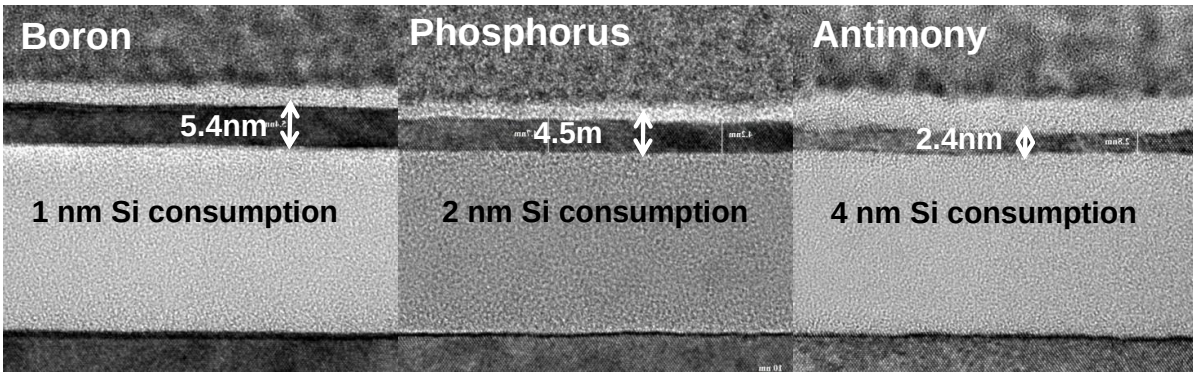



**Figure 4.32: Silicon consumption after nitride removal, for samples subjected to heated implantation.**

This oxidation phenomenon takes place after the nitride removal; in fact, no oxygen is detected between silicon film and nitride layer by EDX measurement, performed after the implantation step. The oxidation is then not due to the oxygen introduced by recoil. It appears that the nitride removal degraded the silicon film which was subjected to significant oxidation once exposed to air.

Nitride capping removal was done by a wet etching step. It is worth remembering that the electrical devices analyzed in sections 4.3.3 and 4.3.4 have been obtained with two different amorphization conditions on the two halves of the wafers. The resin stripping step, which uses similar wet etching chemical than for the nitride removal probably led to the silicon consumption observed in Figure 4.28b. This is an interesting phenomenon because it could limit the compatibility of heated implantation with some standard etching steps, and a detailed study about this point is currently ongoing.

## 4.4 Extension First on TriGate with Hot Implantation

Heated implantation technique appears even more suitable than room temperature implant for extension first Integration scheme in terms of device morphology. In fact, the hot implantation should lead to less surface damage on the film surface compared to room temperature implant and allowing an easier epitaxial regrowth on the implanted film. In chapter three, it has been shown that SiC:P epitaxial regrowth after extension first implantation can present some complications.

TEM cross section shown in Figure 4.33 shows an example of epitaxial regrowth after hot phosphorus implantation. This observation refers to n-type 14 nm FDSOI technology transistor with a SiC:P epitaxy. Good epitaxial quality is observed.

In this section, the use of hot implantation in combination with extension first integration is proposed on TriGate devices. A brief presentation of the implemented process flow is firstly provided and electrical results supported by simulations will be presented as well.

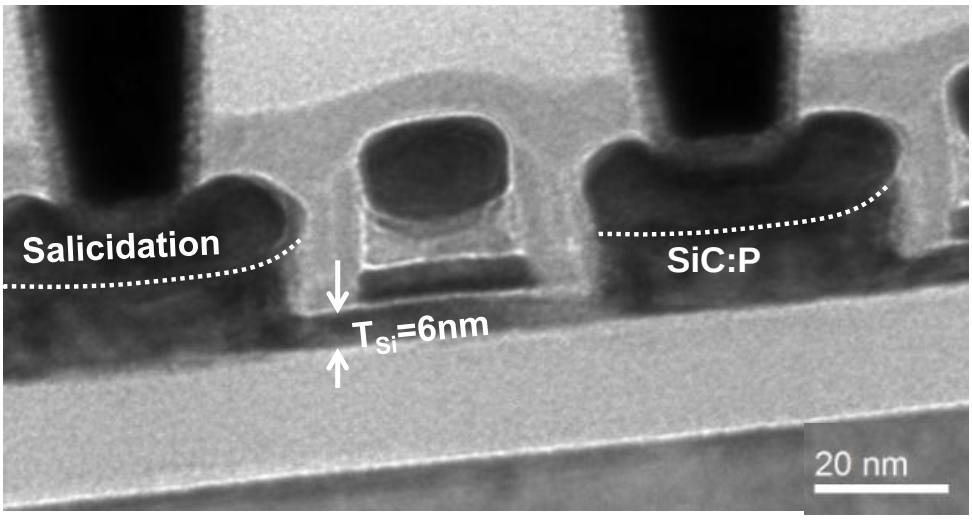



**Figure 4.33: TEM observation on n-type FDSOI with extension first integration and heated implantation.**

### 4.4.1 Process flow description

The process flow used is quite similar to the one presented in section 3.2 on FDSOI devices. The following figures summarize the principal process steps:

- After the gate patterning, a 4 nm nitride liner is deposited. In this case the silicon film has a thickness of 11 nm.
- The extension first implantation is made. The implant conditions are reported in Table 4.3.
- A second nitride deposition of 8 nm is made in order to reach the target dimension of the first spacer.
- The nitride liner is etched away from silicon surface to form the first spacer.

- Epitaxial regrowth for the raised source and drain is made. As for the FDSOI devices presented in chapter 3, the epitaxial materials are SiGe:B for pMOS and SiC:P for nMOS. The process temperature is maintained below 630 °C.
- The dopant activation by spike annealing is not performed. Two zones are then created: the raised source and drain regions in which the dopants show the activation level obtained by the in-situ epitaxy and the film silicon region in which dopant have the activation level post hot implantation.
- The process flow continues with access silicidation and standard BEOL.

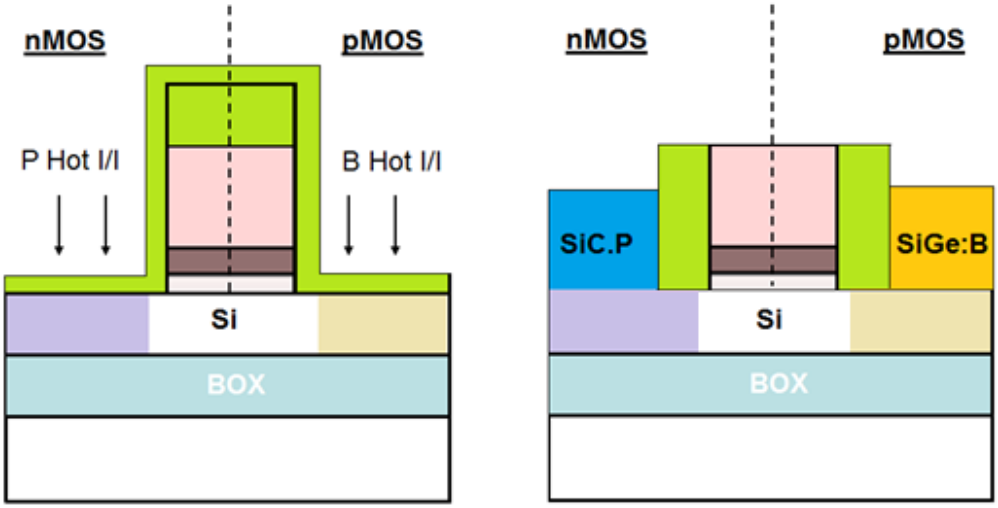



**Figure 4.34: Schematic process flow for implantation and epitaxial steps in the extension first integration applied on TriGate devices with hot implantation.**

A schematic process flow of extension first integration on TriGate devices is reported in Figure 4.34.

Figure 4.35 shows a TEM cross section observation of a n-type TriGate structure fabricated with extension first integration scheme with hot implantation. Good crystalline quality can be observed in the raised source and drain regions.

In the next two sections, the electrical results of low temperature devices fabricated with the process flow illustrated in Figure 4.42 are presented in comparison with the high temperature device made with the process of reference. However, some significant differences are present in the process of reference:

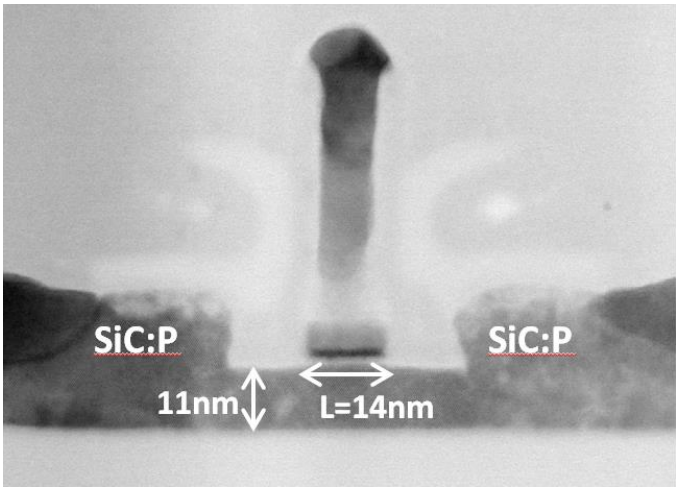



**Figure 4.35: TEM observation of an n-type TriGate device fabricated with the process flow illustrated in Figure 4.32.**

In the next two sections, the electrical results of low temperature devices fabricated with the process flow illustrated in Figure 4.42 are presented in comparison with the high temperature device made with the process of reference. However, some significant differences are present in the process of reference:

- The raised source and drain are made by silicon epitaxial growth. The use of silicon instead of SiGe:B or SiC:P as in the process flow of Figure 4.34 means that no strain effect will be provided by the source and drain region. This can modify the carrier transport behavior on the access and in the channel regions compared to an unstrained device. This point concerns pMOS devices only since no evidences of strain contribution are demonstrated with the use of SiC epitaxies instead of silicon.
- The doping of the access region is made by dopant implantation after the silicon epitaxial growth. Different dopant concentration is then present in the epitaxy regions compared to the low temperature process flow where the dopants have been introduced by in-situ doped epitaxies. As usual, for high temperature devices, the dopant activation has been obtained by spike annealing.

For these reasons, a fair comparison of electrical performance and parameters between low temperature and high temperature devices is not possible. However, the two type of devices have been reported in order to compare the electrical behavior of the low temperature device fabricated with extension first integration scheme in comparison with the state of the art TriGate technology fabricated at LETI considered as the target of performance.

| Dopant | Dose (at/cm$^2$) | Energy (KeV) | Tilt (°) | Temperature (°C) |
|---|---|---|---|---|
| Boron | $2x10^{14}$ | 1 | 0 | 500 |
| Phosphorus | $7x10^{14}$ | 4 | 0 | 500 |
| Arsenic | $7x10^{14}$ | 4 | 0 | 500 |

**Table 4.3: Implantation condition details for extension first integration on TriGate devices.**

### 4.4.2 pMOS results and analysis

Dopant implantation conditions have been defined by KMC simulation. In TriGate devices, three–dimensional effects play a fundamental role and a complete three-dimensional structure has been simulated as reported in Figure 4.36.

As in the previous sections, the goal of implantation condition definitions is to have active dopant concentration around $3x10^{20}$ at/cm$^3$ in the epitaxy region and around $5x10^{19}$at/cm$^3$ in the region below the spacer to reach an access resistance value similar to the high temperature device. A cross section of Figure 4.36, showing the total boron concentration with a focus on the region below the first spacer is reported in Figure 4.37.

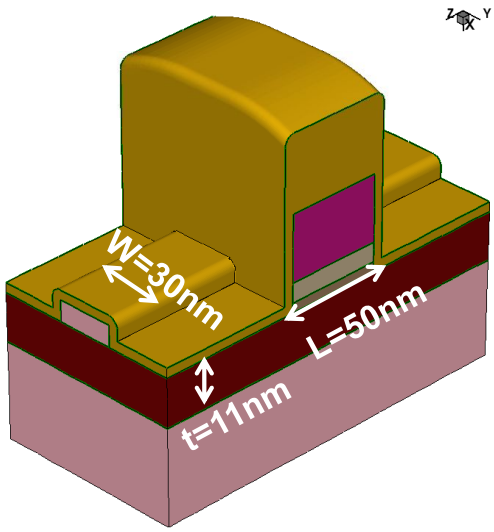



**Figure 4.36: Simulated structure of TriGate device.**

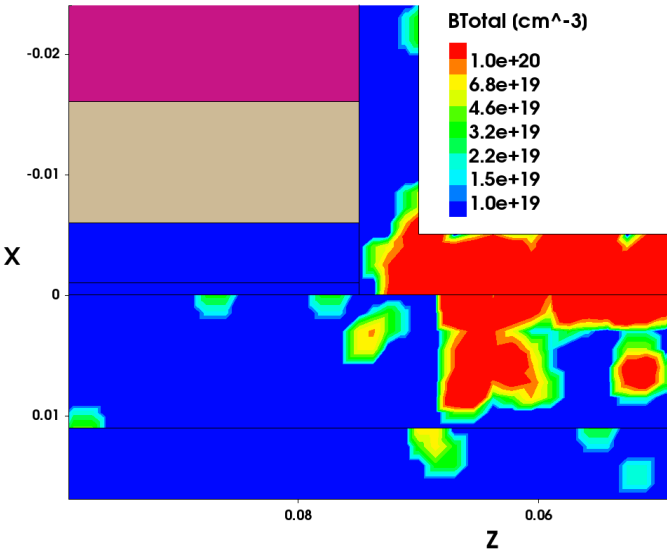



**Figure 4.37: Total boron concentration after hot implantation obtained by KMC simulation focusing on the region below the first spacer.**

Figure 4.38 shows $I_{ON}$-$I_{OFF}$ trade-off of heated implant split compared to the process of reference devices with dopant activation at high temperature. Every point of measurement corresponds to an array of ten devices with a 30 nm width dimension and a channel length ranging from 1 µm to 10 nm. In all the proposed electrical characterization, every device has been corrected in width and length using the top view SEM observation. The ON current value has been extracted at $V_{DS}$=$V_{GS}$=0.9 V. The current normalization considers the $W_{TOP}$ only. Some electrical parameters have been extracted on smaller devices with $W_{TOP}$=15 nm. These structures have more devices with different channel lengths and they allow to have more points of measurements and then more clear tendency of the parameter under study. The width dimension of the tested devices is reported on the corresponding figure.

For the first time, working devices with extension first integration scheme in combination with hot implantation have been obtained confirming the feasibility of the process flow proposed in section 4.4.1. Only 20% of performance degradation is found compared to the high temperature process of

reference. It is worth remembering that for extension last case with hot implantation, performance degradation of around 60% was observed compared to the process of reference (section 4.3.3).

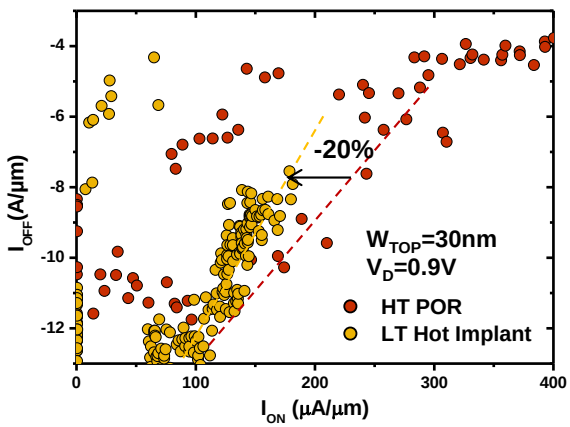



**Figure 4.38: $I_{ON}$-$I_{OFF}$ trade-off for p-type low temperature devices with hot implantation in comparison with high temperature process of reference.**

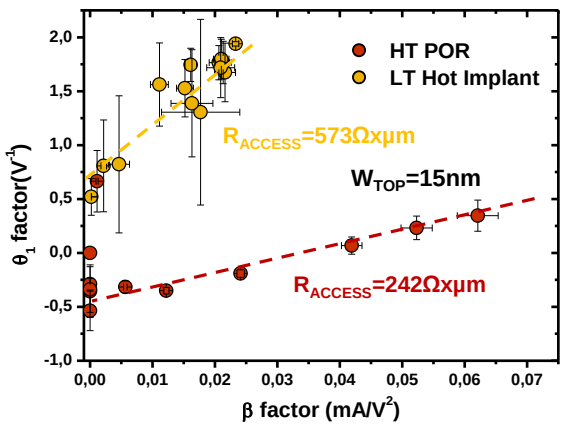



**Figure 4.39: Access resistance degradation for p-type hot implant split compared to process of reference.**

This result is surprising since, as demonstrated in section 4.2.2 and confirmed by electrical results on FDSOI of section 4.3.3, the activation level of boron post hot implant is really low (<5x$10^{18}$ at/$cm^3$) and this performance results are not so bad compared to the state of the art technology. High value of RSPA is expected and access resistance degradation is observed in Figure 4.39. In order to validate the hypothesis that access resistance degradation for hot implant split is related to $R_{SPA}$ degradation, the other contributions of access resistance have been evaluated. Sheet resistance measurements on Van der Pauw structures of silicided active zones have been performed. Slight sheet resistance variation is observed for hot implant split compared to POR as reported in Figure 4.40. This confirms the results found in section 3.6.3 showing that salicided sheet resistance on SiGe is higher compared to silicon. However, if contact resistance is also considered, no significant variation is found on hot implant split and POR as reported in Figure 4.40. In addition, it has been demonstrated in section 3.5.2 that boron activation level after SiGe:B epitaxy is as good as after spike annealing and unsilicided zone of the raised source and drain is expected to provide good values of sheet resistance. For these reasons, high value of access resistance for hot implant splits can be ascribed to the last contribution of access resistance, i.e, the zone situated below the first spacer, $R_{SPA}$. In order to confirm this hypothesis, DIBL is the parameter that allows to have an idea on the junction position, and then on the doping below the first spacer.

$R_{ON}$-DIBL trade-off is shown in Figure 4.41. As expected, $R_{ON}$ degradation is observed for hot implant split. On the other side, DIBL values are reduced compared to the high temperature POR. DIBL is then reported in Figure 4.40 as a function of gate length and evident reduction is found for low temperature with hot implant split.

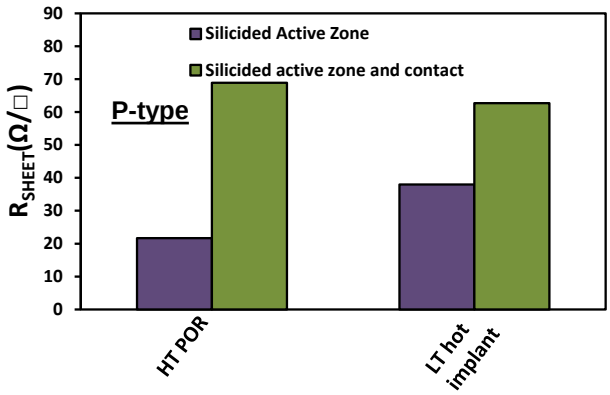



**Figure 4.40: Sheet resistance measurements on silicided active zone with and without contact resistance for hot implant split and POR.**

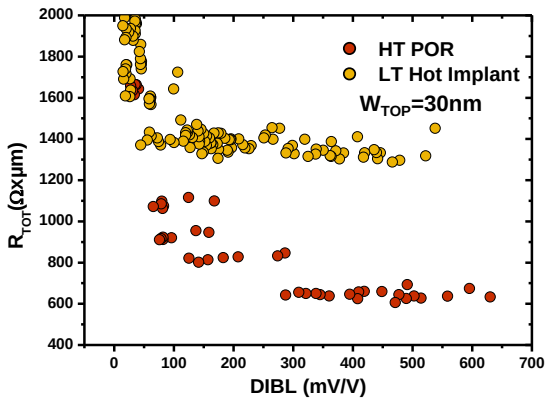



**Figure 4.41: $R_{TOT}$-DIBL trade-off for low temperature devices with hot implantation in comparison with high temperature POR. Same DIBL is shown while total resistance degradation is observed for hot implant split.**

DIBL variation indicates junction position variation. In particular, hot implant split appears in clear underlap configuration compared to high temperature device and ΔL=42nm can be extracted. It is worth noticing that such a value is really high and suggests that high temperature device is in a severe overlap configuration. This consideration is supported by enormous DIBL values (above 150 mV/V) for devices with channel length below 40 nm indicating that the gate electrode is completely unable to control the inversion channel.

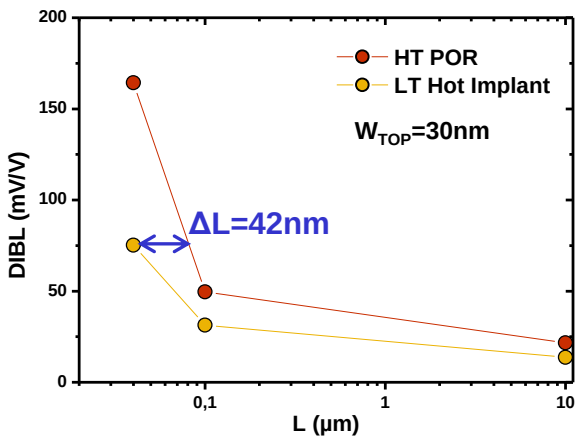



**Figure 4.42: DIBL at different gate lengths for low temperature devices with hot implantation in comparison with high temperature POR. High DIBL reduction for hot implantation devices demonstrates underlap configuration.**

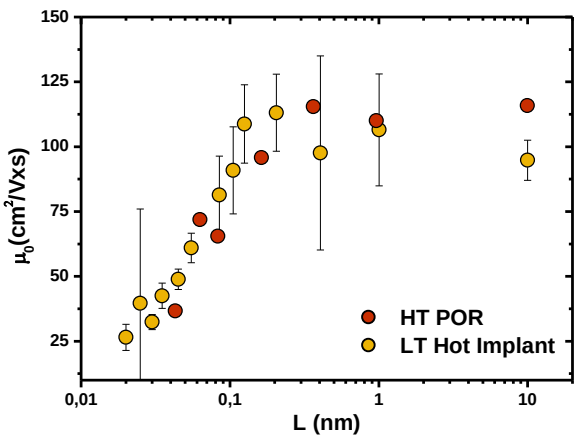



**Figure 4.43: Carrier mobility at low electric field. No variations are observed between high temperature device and low temperature with hot implant.**

Finally, carrier mobility at low electric field is plotted function of the gate length and reported in Figure 4.43. ΔL correction has been necessary to fairly plot the mobility behavior for different gate lengths.

However, at this stage, no clear conclusions can be provided: for low temperature split carrier mobility can be affected by the strain produced by the presence of SiGe:B raised source and drain while this effect is not present in the high temperature devices with silicon raised source and drain; the presence of defects due to the hot implantation could lead to mobility degradation; if the hypothesis of poor dopants concentration below the first spacer is confirmed as well as underlap configuration a mobility degradation at channel lengths shorter than 1 µm should appear for low temperature devices as in the cases discussed in Figure 2.30 and Figure 4.25. The quantification and the decorrelation of these three effects on the mobility is not trivial and further detailed analysis are necessary in order to have fulfill comprehension. Moreover, no typical increases of the mobility [Coquand 13] is observed as it should appear for a strained device. An open question is if after extension first implantation, the strain induced into the channel by the SiGe epitaxies is conserved.

At this stage, it can be only concluded that low temperature device with extension first heated implantation presents 20% degradation compared to the high temperature device. This is due to a high value of the access resistance probably due to the insufficient doping concentration below the spacer for the low temperature device that leads to an underlap configuration.

### 4.4.3 nMOS results and analysis

Similar analysis has been carried out for nMOS fabricated with the integration scheme illustrated in Figure 4.34. In Figure 4.44 is reported the total phosphorus concentration obtained by KMC simulations. Concentration above $10^{20}$ at/cm$^3$ is present below the spacer, so the activation level just after hot implantation should lead to an acceptable value of $R_{SPA}$.

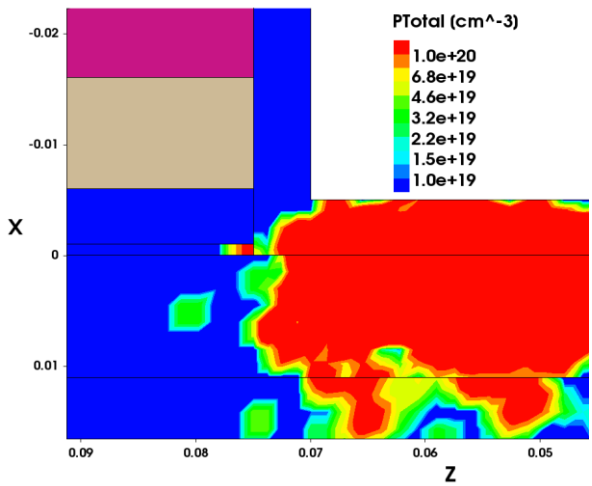



**Figure 4.44: Total phosphorus concentration after hot implantation obtained by KMC simulation focusing in the region below the first spacer.**

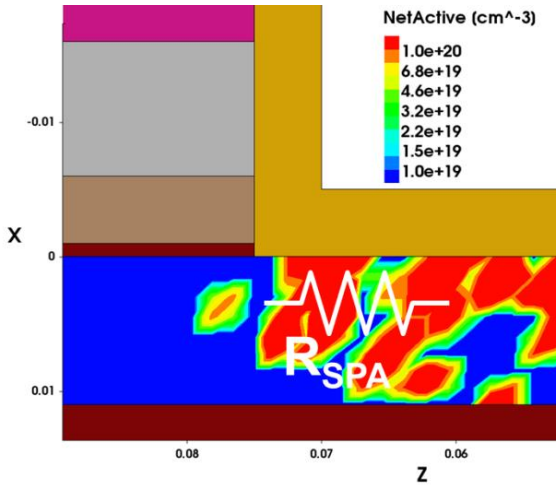



**Figure 4.45: Active phosphorus concentration after hot implantation obtained by KMC simulation focusing in the region below the first spacer.**

Even though the validity of the activation level after hot implantation obtained by simulation is unknown, $R_{SPA}$ values is extracted to 10 Ωxµm, quite below the target of 30 Ωxµm. However, the active doping concentration, extracted by KMC simulation (Figure 4.45) appears too high (above $10^{20}$ at/cm$^3$)

compared to the experimental results obtained on full sheet wafers presented in section 4.2.3 where the activation level is predicted to be around $5x10^{20}$ at/cm$^3$.

$I_{ON}$-$I_{OFF}$ trade-off is shown for low temperature device with hot implantation is reported in Figure 4.46 in comparison with high temperature fabricated with the process of reference. As for pMOS case the tested devices correspond to an array of ten devices with width dimension of W=30 nm and channel length ranging from 1 µm to 10 nm. 20% of performance degradation is shown for low temperature split with hot implantation that is explained by access resistance degradation observed in Figure 4.47.

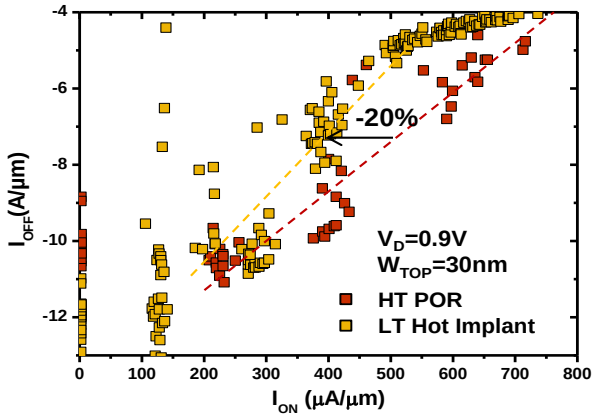



**Figure 4.46: $I_{ON}$-$I_{OFF}$ trade-off for n-type low temperature devices with hot implantation in comparison with high temperature POR.**

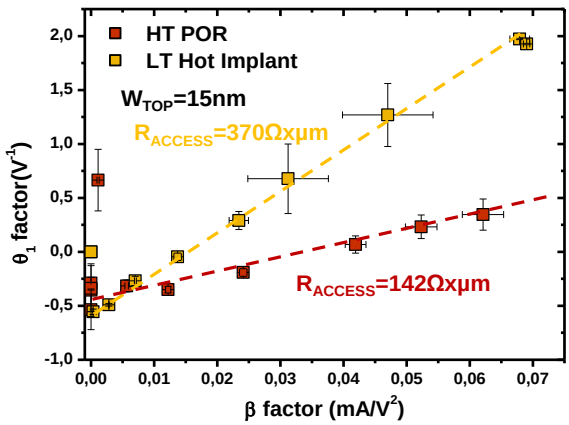



**Figure 4.47: Access resistance degradation for n-type hot implant split compared to POR.**

The goal is now to identify the contribution that mainly explains the access resistance degradation for low temperature devices. Sheet resistance measurements on Van der Pauw structures for the two considered splits are shown in Figure 4.48. No significant differences appear on silicided zones both with and without the contribution of the contact resistance.

However, it has been described in section 3.61, during the discussion of FDSOI devices with extension first integration scheme, that the phosphorus activation after the SiC:P epitaxy is not so efficient if spike annealing is not performed. Significant sheet resistance degradation (around 100%) was found on the unsilicided sheet resistance compared to the process of reference if spike annealing is not performed. Similarly, in this lot, the doping step has been made directly during the epitaxy of raised source and drain and no spike activation has been performed. So similar value (~300 Ω/□) can be assumed for unsilicided zone. The typical value of unsilicided resistance for the high temperature device with spike anneal activation is around 250 Ω/□. Such difference cannot fully explain the high difference in access resistance between low temperature and high temperature device (more than a factor 2). So, probably, the main contribution of the access resistance degradation comes from the region below the spacer.

In order to evaluate the junction position, DIBL behavior for different gate length is plotted in Figure 4.49. Low temperature devices exhibit a lower DIBL compared to high temperature device. In this case ΔL=15 nm can be extracted. For a gate length of 30nm, low temperature device shows a really low value of DIBL of 55 mV/V indicating a probable underlap configuration, while for high temperature device, this value is around 125 mV/V, showing still an acceptable electrostatic control, but a junction

position definitely closer to the channel compared to the low temperature split. This confirms that the heated doping implantation performed before the raised source and drain epitaxial step has not been efficient for the dopant activation and $R_{SPA}$ value is not in the target.

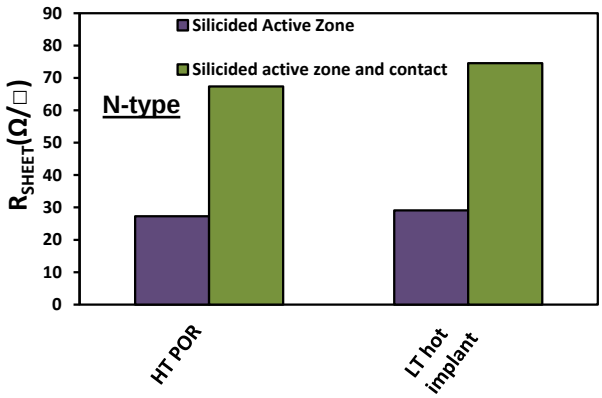



**Figure 4.48: Sheet resistance measurements on siliced active zone with and without contact resistance for hot implant split and POR.**

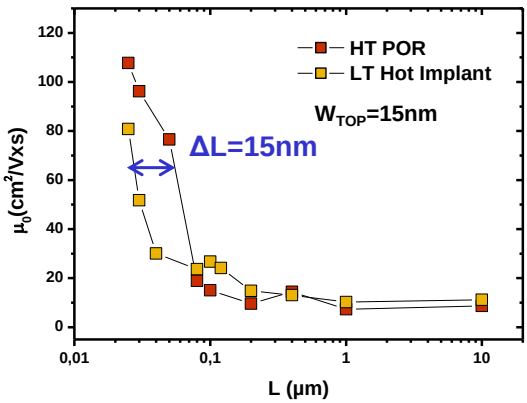



**Figure 4.49: DIBL behavior for different gate lengths for low temperature devices with hot implantation in comparison with high temperature process of reference.**

Finally, electron mobility at low electric field is shown in Figure 4.50 for low temperature and high temperature devices. In this case, the comparison can be considered correct since no strain contribution is made by the raised source and drain in SiC:P. No significant variations are evidenced in the mobility behavior at different channel lengths for the two splits, confirming that the performance mismatch is completely explained by an access resistance degradation for the low temperature devices.

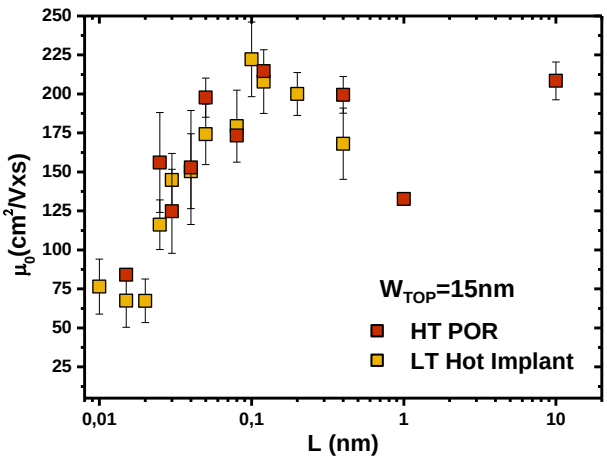



**Figure 4.50: Carrier mobility at low electric field. No variations appear between high temperature device and low temperature with hot implant.**

The electrical analysis presented so far indicates that, both pMOS and nMOS trigate fabricated with a low temperature process flow and the extension fist integration appear in underlap configuration. This

suggests that the use of hot implantation to place the dopants in the region below the first spacer is not sufficient to achieve the dopant activation level necessary to reach the $R_{SPA}$ target. Heated implantation technique needs a post activation annealing that can be, for example a laser activation, compatible with the CoolCube process flow. Preliminary work on the study of the activation level of the heated implantation with DSA (Dynamic Surface Anneal) and nanosecond laser, has been started. Promising results are expected by the combination of these two techniques.

## 4.5 Conclusion of the chapter

In this chapter, several aspects of the heated implantation technique have been investigated. First, it has been verified that the one-dimensional profiles obtained after heated implantation (500°C) correspond to the ones predicted by KMC simulations. Acceptable correspondences between simulated and experimental profiles have been found for boron, phosphorus and arsenic. This is important to be confident in the dopant profile obtained by simulation results.

After that, the as-implanted activation level of these three dopant species has been evaluated by sheet resistance measurements on full sheet wafers in combination with Hall effect measurements. Low activation level of $5x10^{18}$ at/cm$^3$ has been measured for boron while for arsenic and phosphorus it has been found around $5x10^{19}$ at/cm$^3$. However, carrier mobility degradation is measured compared to the value at thermodynamic equilibrium. This is probably due to the presence of defects not recovered after the heated implantation.

The activation level of boron, phosphorus and arsenic has been evaluated after heated implantation and activation by SPER. Same activation level of implantation made at room temperature and SPER activation, as in the examples discussed in chapter one, have been found for all the three dopant species.

Heated implantation has been implemented in two difference device architectures, for the optimization of low temperature process flow. First, it has been used in an extension last scheme on FDSOI devices. Heated implantation enables to position dopant in the access regions depth without full amorphization and it appeared useful to position dopant in the region below the first spacer and improve $R_{SPA}$ value. SPER activation has been used to activate the dopants in the raised source and drain regions. High performance degradation of approximately 60% has been found compared to the process of reference for pMOS devices. This is mainly ascribed to the poor as-implanted boron activation level and the underlap device configuration as confirmed by both electrical characterization and process simulation results. Once again, the extraction method shows a strong degradation of the carrier mobility for long channel length (1 µm) that does not appear related to a real phenomenon. Y function method does not provide reliable results when the tested devices are in underlap configuration.

nMOS devices fabricated with heated implantation show even worst electrical results. This is explained by an anomalous reduction of the raised source and drain thickness region and a full silicidation of the zones. This leads to a high degradation of the contact resistance between the silicided zone and the doped zone. Silicon thickness reduction is due to an anomalous oxidation appearing after wet etching step, after hot implantation. This oxidation is more important if the implanted specie is more massive.

Finally, heated implantation has been used in the extension last scheme on a TriGate device architecture. For the first time, working device have been obtained using this kind of integration obtaining for both pMOS and nMOS promising results with a 20% of degradation compared to the process of reference. However, in both cases, the devices still appear in underlap configuration suggesting that the activation level of heated implantation is not sufficient to reach the required target of $R_{SPA}$ and thus the target of performance.

Heated implantation appears a promising technique due to the possibility of position dopants in the whole access region without full amorphization. Morphological interest in the use of heated implantation is validated as well since epitaxial re-growth is not problematic. However, it appears that heated implantation alone does not satisfy the target of $R_{SPA}$ required for low temperature device optimization. Heated implantation should be used in combination with alternative dopant activation techniques such as nanosecond laser or DSA laser in order to improve the as-implanted activation and maintain the compatibility with CoolCube process flow that requires a low thermal budget (laser anneals used ultra-short process time) for the top transistor level.

## References

[Dubois 02] Emmanuel Dubois and Guilhem Larrieu. "Low Schottky barrier source/drain for advanced MOS architecture: device design and material considerations." Solid-State Electronics 46.7 (2002): 997-1004.

[Coquand 13] Coquand, R., et al. "Scaling of high-κ/metal-gate TriGate SOI nanowire transistors down to 10nm width." Solid-State Electronics 88 (2013): 32-36.

[Khaja 14] Khaja, Fareen Adeni, et al. "Bulk FinFET junction isolation by heavy species and thermal implants." Ion Implantation Technology (IIT), 2014 20th International Conference on. IEEE, 2014.

[Masetti 83] G. Masetti, M. Severi, and S. Solmi. "Modeling of carrier mobility against carrier concentration in arsenic, phosphorus, and boron-doped silicon." Electron Devices, IEEE Transactions on 30.7 (1983): 764-769.

[Mizubayashi 13] W. Mizubayashi,, et al. "Heated ion implantation technology for highly reliable metal-gate/high-k CMOS SOI FinFETs." Electron Devices Meeting (IEDM), 2013 IEEE International. IEEE, 2013.

[Morehead 72] F. F. Morehead, B. L. Crowder, and R. S. Title, ”Formation of Amorphous Silicon by Ion Bombardment as a Function of Ion, Temperature, and Dose”, Journal of Applied Physics 43, 1112 (1972).

[Onoda 14] H. Onoda, W. Mizubayashi, Y. Nakashima and M. Masahara, “Heated Ion Implantation Technology for FinFET Application ” International Workshop on Junctions Technology (IWJT) 2014.

[Sasaki 15] Sasaki, Y., et al. "A comparison of arsenic and phosphorus extension by Room Temperature and hot ion implantation for NMOS Si bulk-FinFET at N7 (7 nm) technology relevant fin dimensions." VLSI Technology (VLSI Technology), 2015 Symposium on. IEEE, 2015.

[Swirhun 88] S. Swirhun, Electrochem. Soc., Oct. 1988

[Togo 13] Togo, Mitsuhiro, et al. "Heated implantation with amorphous carbon CMOS mask for scaled FinFETs." 2013 Symposium on VLSI Technology. 2013.

[Wood 13] B. Wood, B. Colombeau, S. Sun, A. Waite, H. Chen, M. Jin, O. Chan, F. Khaja, T. Thanigaivelan, N. Pradhan, H.-J. Gossmann, S. Sharma, V. Chavva, M-P Cai, M.Okazaki, S. Munnangi, C-N Ni, W. Suen, C-P Chang, A. Mayur, “Fin Doping by Hot Implant for 14nm FinFET Technology and Beyond”, 224th ECS Meeting, 2013.

# Conclusion and perspectives

3D sequential integration is one the most promising candidate for the scaling sustainability for the future technological nodes. The main challenge of the 3D sequential integration is the development of a low temperature process flow for the top transistor level in order to avoid the degradation of performance and integrity of the bottom transistor level. One of the most critical process step is the dopant activation that is usually performed at temperature above 1000 °C. In this context, the work of this Ph.D. aimed to find solutions to implement a dopant activation step at temperature below 600 °C delivering same performance of the process of reference at high temperature. Solid Phase Epitaxial regrowth (SPER), that allows high dopant activation at low temperature, has been widely studied in this work.

In chapter one, basics principle of SPER has first discussed. The dopant conditions optimization for this activation technique has been studied for phosphorus, arsenic and boron. The first important result is that doping conditions optimization are different if the activation step is made by spike anneal at high temperature or low temperature SPER. The sheet resistance optimization for low temperature activation need a lower implanted dose compared to the spike activation. SPER activation is highly efficient in the dopant activation reaching values higher than solid solubility limit, only below a certain value of dopant concentration named clustering limit. Above this value, inactive agglomerations, called clusters, are formed, reducing the dopant activation or the carrier mobility, leading to a degradation of the resistivity. Clustering limit values have been extracted for arsenic and phosphorus for activation at 600 °C. Phosphorus appears more adapted for low temperature activation since it enables to obtain a quasi-constant profile all along the access depth without full amorphization. Another important point is the study of the SPER rate, i.e. the re-crystallization velocity. The optimum doping concentrations that maximize the SPER rate have been extracted for phosphorus and boron for anneal temperatures down to 450 °C. It has been demonstrated that dopant activation by SPER can be performed down to 450°C with time compatibles with industrial process (around one hour). The dopant activation by SPER has been tested at 500 °C and 450 °C. For phosphorus similar sheet resistance than at 600 °C has been found. For boron at 500 °C and 600 °C similar sheet resistance values have been obtained while slight degradation has been shown for 450 °C anneal. However, these results have been obtained by removing the native $SiO_2$ just before the implantation step. Incomplete re-crystallization and consequent sheet resistance degradation is shown in case of implantation through native $SiO_2$. These results are promising for the 3D sequential integration since they show that dopant activation by SPER can be efficient for temperatures down to 450 °C.

The optimum doping conditions defined in chapter one have been implemented in electrical FDSOI devices. A detailed electrical analysis has been proposed in chapter two. In nMOS devices, 20% degradation is obtained for best split fabricated at low temperature (phosphorus implantation) compared to the process of reference fabricated at high temperature. Both process and device simulation show that the access resistance degradation can be mainly explained by the difficulty to place active dopants in the region below the first spacer that leads to a degradation of the resistance component of that region, so named $R_{SPA}$. In order to improve the doping concentration below the spacer, the implantation energy and tilt have been increased. With the modified implantation conditions, low temperature devices performance achieves the process of reference, but with degradation of the short channel effects, more evident in pMOS devices. Moreover, it has been shown

that the implemented implantation conditions led to full amorphization and the re-crystallization has been obtained by lateral direction. This is not compatible with advanced technological nodes because the risk of the strain relaxation and defective crystallization. Two criteria have been defined to decide if the chosen integration scheme is acceptable for the optimization of the device fabricated at low temperature: the maximum acceptable value of $R_{SPA}$ and the minimum thickness of the crystalline seed. The first, refers to the quantity of active dopant concentration placed below the spacer and then to the access resistance value. The second is strongly dependent on the amorphous/crystalline interface roughness and the thickness variability and it needs to define a crystalline seed that allow to a vertical re-crystallization. These two parameters have to be satisfied at the same time. Simulation results show that the most adapted integration scheme for FDSOI devices is the extension first, in which the dopant implantation is made before the regrowth of the raised sources and drains. Similar study has been carried out on TriGate devices fabricated at low temperature. Working electrical devices that outperform results present in literature have been obtained. However, $R_{SPA}$ looks the most critical parameter for this kind of architecture as well. The $R_{SPA}$-$T_{SEED}$ criterion shows that, also for TriGate, the most adapted integration scheme is the extension first. The study has been extended to FinFET devices, where, simulation results show that both $R_{SPA}$ and $T_{SEED}$ criteria can be satisfied and FinFET architecture appears to be a promising candidate for CoolCube integration.

Extension first integration scheme has been studied in chapter three. The main technological challenges are: the definition of doping condition that allow to amorphize and place active dopants in a relay thin film (amorphization of around 3 nm on 6 nm is needed) and the epitaxial re-growth on implanted film. A study on the measurement of the dopants activation level on thin films has been carried out as well. The two challenges have been solved and the extension first scheme has been integrated for the first time in 14 nm FDSOI devices. Promising electrical results have been obtained: nMOS best low temperature device show 12% degradation from the process of reference while only 5% degradation is shown for best pMOS split compared to the process of reference. This indicates the extension first integration as a promising candidate for the development of low temperature devices

An alternative solution to place dopant in depth without full amorphization, which is needed for the region below the spacer, is represented by the heated implantation technique. First, the heated implantation has been studied in its basic features: the one-dimensional dopant profiles obtained by KMC simulations have been validated; the activation level after heated implantation for boron, phosphorus and arsenic has been measured, obtaining not-satisfying results according with $R_{SPA}$ target, especially for boron; finally, SPER activation has been applied on heated implanted samples obtaining similar activation levels than the room temperature implantation case. Heated implantation technique has been implemented on FDSOI devices using the extension last integration scheme. Working pMOS devices have been obtained, but with poor performance degradation. The heated implantation has been implemented on TriGate devices as well, using the extension first integration. Both nMOS and pMOS working device with 20% performance degradation compared to the high temperature target has been obtained. Once again, this is related to not sufficient active dopant concentration below the spacer. However, heated implantation appears a promising technique, especially for extension first integration. It allows to place dopant in the whole film depth without the risk of full amorphization and the epitaxial regrowth on heated implanted film is not problematic. The issue of low dopant activation level can be overcome by the use of alternative annealing technique such as DSA or nanosecond laser. These techniques allow to improve the dopant activation level of heated implanted dopant respecting the thermal budget limitation of CoolCube process flow.

# List of publication

Pasini, L., et al. "Insights in accesses optimization for nFET low temperature Fully Depleted Silicon On Insulator devices." *Junction Technology (IWJT), 2014 International Workshop on*. IEEE, 2014.

Pasini, L., et al. "nFET FDSOI activated by low temperature solid phase epitaxial regrowth: Optimization guidelines." *SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2014 IEEE*. IEEE, 2014. (Best student paper award)

Pasini, L., et al. "High performance low temperature activated devices and optimization guidelines for 3D VLSI integration of FD, TriGate, FinFET on insulator." *VLSI Technology (VLSI Technology), 2015 Symposium on*. IEEE, 2015.

Pasini, L., et al. "High performance low temperature CMOS activated devices." *VLSI Technology (VLSI Technology), 2016 Symposium*.

Luce, F. P, Pasini L. et al. "Methodology for thermal budget reduction of SPER down to 450° C for 3D sequential integration." *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms* 370 (2016): 14-18.

Batude, P., et al. "3DVLSI with CoolCube process: An alternative path to scaling." *VLSI Technology (VLSI Technology), 2015 Symposium on*. IEEE, 2015.

Fenouillet-Beranger, C., et al. "FDSOI bottom MOSFETs stability versus top transistor thermal budget featuring 3D monolithic integration." *Solid State Device Research Conference (ESSDERC), 2014 44th European*. IEEE, 2014.

Vinet, M., et al. "Monolithic 3d integration: a powerful alternative to classical 2d scaling." *SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2014 IEEE*. IEEE, 2014.

Brunet, Laurent, et al. "(Invited) Direct Bonding: A Key Enabler for 3D Monolithic Integration." *ECS Transactions* 64.5 (2014): 381-390.

Fenouillet-Beranger, C., et al. "New insights on bottom layer thermal stability and laser annealing promises for high performance 3D VLSI." *Electron Devices Meeting (IEDM), 2014 IEEE International*. IEEE, 2014.

Sklenard, B., et al. "Low temperature junction formation by solid phase epitaxy on thin film devices: Atomistic modeling and experimental achievements."*2014 International Workshop on Junction Technology (IWJT)*. 2014.

# Résumé en français

## Introduction

La fabrication des circuits intégrés nécessite la reduction des dimensions des dispositifs microélectroniques pour ameillorer les performances et augmenter la densité des composants. Au cours des 40 dernières années, la taille des transistors a été réduite de façon drastique en suivant la loi de Moore selon laquelle le nombre de transistors des microprocesseurs double tous les deux ans. Cela a contribué au développement de circuits de plus en plus performants. Néanmoins, les dimensions des transistors actuels approchent les limites physiques de miniaturisation. Au delà de cette limite, des alternatives doivent être introduites afin de remplacer l'architecture planaire sur substrat massif utilisée classiquement.

Une alternative à la réduction des dimensions tout en augmentant la densité des circuit intégrés est l'intégration 3D séquentielle (3D monolithique). Cette technique consiste à empiler successivement sur un même substrat plusieurs couches de transistors [Batude 11].

Cette techinque prévois d'être capable de fabriquer un transistor sur les étages supérieurs avec un budget thermique réduit (typiquement moins de 600 ◦C) pour reserver l'intgroté et les performances des transistors de l'étage inferieur.

L'activation des dopants, qui est classiquement réalisée à une température élevée (recuit spike de l'ordre de 1050 ◦C), devient l'étape plus critique pour le transistor de l'étage superieur.

Une techinque qui permets de obtenir l'actvation des dopantsà temperature entre 450°-600°C est dit de recristallisation par épitaxie en phase solide (Solid Phase Epitaxial Regrowth, SPER)

Le travail di cette thèse a comme objective la fabrication des dispositifs transistors avancés avec une activation des dopant à faible température par SPER en visant comme target de performance, les dispositifs fabriqués par un procédé standard à haute température.

# Chapitre 1: opimisation de l'activation des dopants par SPER

Une des techniques plus utilisées pour l'introduction des dopantes dans un film semiconducteur est l'implantation ionique. La collision des ions implantés porte au déplacement des atomes du réseau cristallin du semiconducteur et donc à la création de défauts ponctuels appelés interstitiels et lacunes. Pour récupérer l'ordre cristallin et donc les propriétés électriques il est nécessaire l'application d'un budget thermique. Cette étape est appelée activation des dopants. Dans un procédé standard sont utilisées températures jusqu'à 1050°C. Pour atteindre l'activation des dopants à faible température (<600°C) une possible technique est la re-cristallization par épitaxie en phase solide (SPER). Elle consiste dans l'implantation et conséquent amorphization de la couche de semiconducterur en gardent une partie cristalline appelée seed. En appliquant une température <600°C, on obtient une recristallisation à partir du seed (qu'il agit comme motif) et durant la re-cristalization on a l'activation des dopants (les impuretés prennent place les sites substitutionnelles de la maille). Cette technique d'activation se base sur l'hypothèse que la seule partie active est confinée dans la partie pre-amorphisées et recristallisée.

Il a été démontré que les conditions d'implantation qui optimisent le niveau d'activation (monitoré par mesure de résistance carré) ne sont pas le mêmes si l'activation est faite à haute température (spike 1050°C) ou par SPER (600°C 2 minutes). Deux effets expliquent ce phénomène :

- La diffusion des dopants n'apparaitre pas pour températures <600°C. On a donc que dans le cas d'activation à haute température la région active est la totalité de l'épaisseur de la couche (environ 22 nm pour les source/drain d'un transistor SOI) lorsque dans le cas d'activation par SPER la région active est limitée à la région amorphisée.
- La concentration de dopant active atteignable n'est pas la même pour les deux types d'activation.

La valeur de concentration active maximale, définie comme limite de clusterisation, a été mesuré par effet Hall en considérant le profil de dopant implanté dans une un substrat SOI pour As, P et B pour une activation à 600°C :

- $[As]_{cluster,600°C}$= $8x10^{20}$ at/cm$^3$
- $[P]_{cluster,600°C}$= $6x10^{20}$ at/cm$^3$
- $[B_{cluster,600°C}$= $3x10^{20}$ at/cm$^3$

Idéalement, le profil de dopant, doit être constant long la profondeur de la couche de semiconducteur aux valeurs reportées en-dessous.

Même si l'arsenic montre une limite de clusterisation supérieur à celui du phosphore, il est préférable d'utiliser le phosphore pour l'activation à faible température. Ça c'est dû au fait que le phosphore a une mass atomique plus faible de l'arsenic et il est donc possible de positionner une concentration plus élevées en profondeur, toujours en gardant un seed cristallin.

En optimisant les conditions d'implantation en visant un profile implanté le plus contant possible à la valeur de limite de clusterisation, meilleures valeurs de résistance carrée sur une couche de 22 nm ont été obtenues avec un activation par SPER à 600°C par rapport à l'activation standard par spike annealing.

Après avoir définie les conditions d'implant pour optimiser l'activation (à travers les mesures de résistance carrée) une deuxième partie de cet étude a concerné l'optimisation de la vitesse re-cristallisation. La vitesse de cristallisation (aussi appelée SPER rate) suive une loi de type Arrhenius, donc elle diminue de façon exponentielle avec la réduction de la température de recuit. La présence d'impuretés dopants peut augmenter la vitesse de cristallisation jusqu'à un certain niveau de concentration, au-délà, on aura une réduction de la vitesse.

Le target de réduction de la température pour le procédé du transistor supérieur dans une architecture CoolCube est 450°C. Il est essentiel comprendre si à 450°C les temps nécessaires à compléter la re-cristallisation sont toujours compatible avec des procédés industriels en gardant le même niveau d'activation obtenu à 600°C.

La vitesse de re-cristallisation a été investigué par mesures d'éllipsometrie avec recuit in-situ. Avec cette technique, est possible monitorer l'avancement de l'interface amorphe/cristal long le temps de recuit. Le dérivé de cette courbe représentés la vitesse de cristallisation.

En combinant mesures d'éllipsometrie in-situ avec images TEM, il a été montré que pour des films dopés phosphore et bore n'est pas possible compléter la re-cristallisation avec des recuit à 450°C, Avec des temps compatibles aux ceux montrés en littérature. Cela est dû à la présence d'atomes d'oxygène dans les premiers nanomètres de la couche de semiconducteur. Les dopants, en fait sont, introduits dans le film à travers l'oxyde native superficiel. Une concentration non-négligeable d'oxygène est donc insérés dans le film par recul qui ralentisse le SPER rate et donc ne rende pas possible une complète recristallisation. Si l'oxyde native est enlevé juste avant l'étape d'implantation, une re-cristallisation complète de la couche est obtenue (pour dopage B et P) et la vitesse de cristallisation est constante. Dans le cas d'implant sans la présence d'oxyde, les mesures de résistance carrée montrent que le niveau d'activation à 450°C est très similaire à celui obtenu à 450°C.

# Chapitre 2: Résultats électriques et guidelines pour l'optimisation de dispositifs FDSOI à faible température

Dans le chapitre 1, les conditions d'implantation, i.e, le profil de dopant 1D ont été optimisé pour l'activation par SPER à faible température. Ces résultats ont été intégrés dans des dispositifs MOS avancé FDSOI et TriGate.

Tout d'abord, on a fabriqué des dispositifs à faible température en utilisant une technologie FDSOI 28 nm. Les caractéristiques électriques des dispositifs à faible température (LT) sont comparées à ceux de la référence, i.e., les dispositifs fabriqués avec le flow standard FDSOI 28 nm à haut température (HT). L'analyse électrique présenté dans ce résumé concerne les dispositifs type n, mais elle est toutefois valable pour dispositifs type p. Les performances $I_{ON}$—$I_{OFF}$ montrent une dégradation du 20% pour le meilleur split LT (implant phosphore) par rapport à la référence HT. Dégradation encore plus évidente est montrée pour le split avec implant arsenic (44%). No différences entre les dispositifs LT et HT apparaitre sur les paramètres EOT, mobilité des porteurs dans le canal et DIBL. Par contre, l'évolution parmi les splits de la résistance d'accès (extraite par la méthode fonction Y) bien représente l'évolution de la performance $I_{ON}$—$I_{OFF}$. Pour comprendre la dégradation de la résistance d'accès sur les dispositifs LT, un travail de simulation a été proposé. En particulier, la concentration des dopant dans la région sous le spacer zero a été extraite par simulation KMC process (SPROCESS). Les résultats de simulation montrent qu'une concentration de dopant plus faible est présent sous le spacere pour les dispositifs à faible température. La contribution de la résistance d'accès liée à cette partie ($R_{SPA}$) a été extraite par simulation device (SDEVICE). L'évolution de $R_{SPA}$ explique de façon convainquant l'évolution globale de la résistance d'accès expérimentale.

La région sous le spacer est donc la plus critique pour l'optimisation des dispositifs à faible température. Ça c'est dû à deux raisons :

- L'activation par SPER nécessite d'une amorphisation : vu l'épaisseur du film très mince (6nm), dans la région sous le spacer, il est extrêmement compliqué de définir des conditions d'implant pour obtenir une amorphisation, toujours en gardant un seed cristallin (amorphisation partielle).
- Pour des températures de recuit en-dessous de 600 °C, on n'a pas le phénomène de diffusion des dopants. On ne peut donc pas compter sur la diffusion pour « driver » les dopants dans la région sous le spacer.

Pour ces raisons, la région sous le spacer dans les dispositifs LT ne contient qu'une très faible concentration de dopants. Ça va conduire une grosse pénalité sur la partie $R_{SPA}$ qu'on retrouve clairement dans les performances électriques du dispositif LT par rapport aux HT.

La première idée pour essayer de incrémenter la concentration de dopants dans la région sous le spacer est d'augmenter l'énergie et le tilt d'implantation. Avec les nouvelles conditions d'implant, les dispositifs à faible température arrivent à performance $I_{ON}$-$I_{OFF}$ très similaire au target des dispositifs s HT pour p et nMOS. Toutefois, l'utilisation d'un tilt élevé (25°) emmené à la dégradation du DIBL à faible température. Cet effet est plus évident pour les pMOS. La comparaison de la forme des jonctions entre les dispositifs HT (tilt 15°) et LT (tilt 25°) montre clairement une dégradation de l'abrupteté de la jonction lorsque le tilt est augmenté. Ça explique

la dégradation du DIBL pour les dispositifs LT. En plus, l'énergie d'implantation utilisée emmène à une amorphisation totale des accès. Une amorphisation totale est négative pour deux aspects :

i) La recristallisation latérale emmène à une densité élevée de défauts de re-cristallisation qui peuvent impacter la conduction.
ii) Une cristallisation totale peut conduire à une relaxation de la contrainte. Ceci n'est pas compatible avec les nœuds avancés qui prévoient l'introduction de la contraint pour augmenter la mobilité des porteurs dans le canal.

Pour ces deux raisons, l'amorphisation totale n'est pas une option acceptable. Une autre option d'intégration est donc considérée. Cela consiste dans l'implantation des dopants avant l'étape d'épitaxie poue le S/D surelevés. On appelle cet intégration extension first ($X^{1st}$) au contraire de l'intégration classique, extension last ($X^{last}$), où l'implant est fait après l'épitaxie.

Les conditions d'implant doivent être définies en considérant une amorphisation partielle des régions d'accès. Il faut donc définir une seed cristallin minimum. Ceci est défini par deux paramètres :

i) La rugosité de l'interface amorphe/cristalline obtenue après l'implant, I.e. la variation spatiale locale de l'interface. Cela peut être extraite par simulation atomistique. En plus, la simulation prédite que la rugosité augmente si la profondeur d'amorphisation augmente. La rugosité donc sera plus importante dans une intégration de type $X^{last}$ par rapport à $X^{1st}$.
ii) La variabilité de l'épaisseur intrinsèque liée au procès d'épitaxie. Cette duxième contribution apparaitre que dans le cas $X^{last}$.

C'est donc possible définir le seed cristallin minimum ($T_{SEEDMIN}$) en considérant les deux contributions en-dessus comme :

$$T_{SEEDMIN} = \sqrt{{T_{ROUGH}}^2 + {\Delta T_{EPI}}^2}$$

Une fois avoir défini le seed minimum, le deuxième critère à respecter pour l'optimisation des dispositifs à faible température est d'être capable de placer une concentration de dopants suffisant sous le spacer. Cela peut être monitoré par le paramètre $R_{SPA}$. Le maximum valeur de $R_{SPA}$ acceptable (MAX $R_{SPA}$) correspond à la valeur du POR extraite par simulation DEVICE. On peut donc définir la figure de mérite $R_{SPA}$ - $T_{SEED}$. Seulement les conditions d'implant qui respectent au même tempes les deux critères (MAX $R_{SPA}$ et $T_{SEEDMIN}$) peuvent être utilisées pour optimiser les dispositifs à faible température.

Les résultats de simulations montrent que pour une architecture FDSOI, la seule façon pour respecter les deux critères au même temps est l'intégration $X^{1st}$.

CoolCube ne concerne pas que l'empilement de FDSOI sur différent étage. L'architecture TriGate peut être également valide. Dispositifs TriGate à faible température ont été fabriqués avec l'intégration $X^{last}$ et amorphisation partielle. Dispositifs fonctionnels ont été obtenus avec performance $I_{ON}$-$I_{OFF}$ à l'état de l'art pour n et pMOS. Par contre, quand on compare l'extraction expérimental de la résistance d'accès entre dispositifs HT et LT, on voit une dégradation sur les dispositifs LT. Un fois de plus, les résultats de simulations nous indiquent que la dégradation de résistance d'accès est due principalement à la faible concentration des dopants dans la région sous le spacer. En utilisant la figure de mérite $R_{SPA}$ - $T_{SEED}$, on retrouve que même si dans le cas d'amorphisation partielle le critère MAX

$R_{SPA}$ est respecté pour les TriGates, la seule façon pour satisfaire au même temps les deux critères d'optimisation est, encore une fois, passer en intégration $X^{1st}$.

L'étude a été étendu à une architecture de type FinFET. Dans ce cas-là, on trouve également des conditions qui satisfaites les deux critères au même temps. Pour ce qui concerne la fabrication de la jonction à faible température, le FinFET apparaitre un bon candidat pour la technologie CoolCube.

# Chapitre 3: intégration extension first

Dans le chapitre 2, on a montré que la seule intégration qui peut optimiser les dispositifs FDSOI fabriqués à faible température est de type extension first. Le procès flow extension first a été utilisé pour la fabrication de FDSOI en technologie 14nm. Dans ce cas, les dopants sont introduites dans les accès par épitaxie dopées in-situ, SiGe:B et SiC:P pour le p et n MOS respectivement. Les dopants sont après activées par spike annealing et drivés dans la zone sous le spacer par recuit spike en combinaison avec un recuit laser DSA. Dans le cas des dispositifs FDSOI à faible températures, la région sous le spacer est dopée par implantation ionique et une reprise d'épitaxie dopée in-situ est faite pour la formation des S/D surélevés.

Conditions d'implantation pour l'amorphisation partielle d'un film de 6 nm pour les deux cas pMOS (film SiGe) et pMOS (film Si). Dans ce cas, même l'implantation type n (phosphore) nécessite une pre-amorphisation Ge. Un liner d'environ 3nm de SiN est utilisé au moment de l'implantation pour pouvoir utiliser des énergies d'implant (>1KeV) compatibles avec les équipements à disposition. Le niveau d'activation du film implanté a été mesuré par technique ECV, en obtenant une valeur pour le bore de $3x10^{20}$ at/cm$^3$, en accord avec l'activation par SPER. Les valeurs ont été confirmés par mesures Hall et résistance carrée.

Bonne qualité d'épitaxie sur films implantés a été obtenue pour p et nMOS. Par contre, une dose de pre-amorphisation trop importante conduits, dans les deux cas, à une mauvaise qualité de l'épitaxie, vérifié par mesure d'ellipsometrie (dégradation du GOF) et résistance carrée.

Les dispositifs électriques complets ont été fabriqués. Bonne morphologie a été obtenue pour nMOS et pMOS démontant une excellente qualité de la reprise d'épitaxie et une conservation de la cristallinité des zones implantées.

Pour le nMOS, les performance $I_{ON}$-$I_{OFF}$ montrent une modeste dégradation du 12% sur le meilleure split LT, par rapport au POR HT. Par contre, le meilleur split à faible températures correspond au cas d'implantation xFirst sans PAI, par rapport au cas de pre-amorphisation moyenne. Cela est étonnent car l'activation par SPER est prévue d'être plus efficace avec une pre-amorphisation. Avec le support de mesure résistance carrée sur film mince, on a vérifié que la perte de performance dans les cas avec PAI est dû à une désactivation du phosphore emmené par l'introduction de l'azote par recule. Cela est plus important dans le cas de PAI est donc la meilleure $R_{SPA}$ corresponds au cas sans PAI. Pour le dispositifs pMOS, que le 5% de dégradation a été obtenu sur le meilleur split à faible température (cette fois-ci avec une dose moyenne de PAI) par rapport à la référence à haute température.

Ces résultats sont très prometteurs. Pour la première fois, l'integration extension first a été démontré valable sur une technologie FDSOI 14nm pour pMOS et nMOS. Les résultats des dispositifs à faible températures sont à l'état de l'art et peuvent être améliorés avec une optimisation fin des conditions d'implant.

# Chapitre 4: implantation à chaud

Dans ce dernier chapitre, une technique alternative de dopage a été étudiée. L'implantation à chaud consistes dans l'effectuer l'étape d'implant à une température supérieur à RT. Cela peut être utile car pour la plupart des dopants, pour températures >350°C, le phénomène d'amorphisation est supprimé. Il est donc possible de positionner les dopants en profondeur des zones d'accès sans avoir une amorphisation totale. L'implantation à chaud est utilisé en littérature pour le dopage des FinFET, pour éviter l'amorphisation complète dans la direction latérale du film.

Les niveaux d'activation post implantation à chaud ont été mesurer par effet Hall :

- [P]= $5x10^{19}$ at/$cm^3$
- [As]= $3x10^{19}$ at/$cm^3$
- [B]< $2x10^{18}$ at/$cm^3$

SI les niveaux d'activation pour P et As semblent intéressent, au moins pour la partie sous le spacer, il apparaitre que pour le B, une activation trop faible est obtenue après implant à chaud.

Si une activation par SPER est effectuée après un implant à chaud, le niveau d'activation ne subit pas de différence par rapport à une implantation à RT.

L'implantation à chaud a été utilisée dans un flow extension last sur une technologie FDSOI 28nm. Après l'implantation à chaud, un amorphisation partiel est une recristallisation par SPER a été appliquée : la partie des accès aura donc le niveau d'activation de la SPER lorsque la région à l'interface avec le BOX (et onc sous le spacer) a le niveau d'activation as-implanted de l'implant à chaud.

Comme prévu, le pMOS montre de performance très dégradé (-60%() par rapport à la référence. Cela est dû au faible niveau d'activation du B et donc un forte $R_{SPA}$.

Performances encore plus dégradées ont été obtenues pour le nMOS. Cela est dû à un effet de consommation des accès qui emmène à une silicuration partiale des régions de S/D. Une siliciuration partiel a un effet néfaste sur la résistance de contact.

L'implant à chaud a été intégré aussi sur une technologie TriGate avec une intégration de type extension first. Le process flow prévois une implantation dans le film se silicium à travers un capping de nitrure et une reprise d'épitaxie avec dopage in-situ. La faisabilité morphologique du process flow a été démontré. Dispositifs fonctionnels avec le 20% de dégradation ont été obtenus pour pMOS et nMOS à faible température par rapport à une référence HT (état de l'art TriGate en Si au LETI).

L'implantation à chaud reste une option intéressent car permets de positionner les dopant dans tout la profondeur sans amorphiser. Par contre, les résultats obtenus, surtout dans le cas pMOS, nous indiquent qu'il est nécessaire de compléter l'activation des dopants avec une recuit alternative, par exemple l'activation laser.

# Conclusions

L'intégration 3D séquentielle représente une alternative potentielle à la réduction des dimensions afin de gagner encore en densité d'une génération à la suivante. Le principal défi concerne la fabrication du transistor de l'étage supérieur avec un faible budget thermique ; ceci afin d'éviter la dégradation du niveau inférieur. L'étape de fabrication la plus critique pour la réalisation du niveau supérieur est l'activation des dopants. Celle-ci est généralement effectuée par recuit à une température supérieure à 1000 °C. Dans ce contexte, cette thèse propose des solutions pour activer les dopants à des températures inférieures à 600 °C par la technique dite de recristallisation en phase solide. Les conditions de dopage ont été optimisées pour améliorer le niveau d'activation et le temps de recuit tout en réduisant la température d'activation jusqu'à 450°C. Les avancées obtenues ont été implémentées sur des dispositifs avancés FDSOI et TriGate générant des dispositifs avec des performances inférieures aux références fabriquées à hautes températures (supérieures à 1000 °C). En utilisant des simulations TCAD et en les comparant aux mesures électriques, nous avons montré que la région la plus critique en termes d'activation se trouve sous les espaceurs de la grille. Nous montrons alors qu'une intégration dite « extension first » est le meilleur compromis pour obtenir de bonnes performances sur des dispositifs fabriqués à faible température. En effet, l'implantation des dopants avant l'épitaxie qui vise à surélever les sources et drains compense l'absence de diffusion à basse température. Ces résultats ont par la suite été étendus pour des dispositifs TriGate et FinFETs sur isolants. Pour la première fois, l'intégration « extension first » a été démontrée pour des N et PFETs d'une technologie 14 nm FDSOI avec des résultats prometteurs en termes de performances. Les résultats obtenus montrent notamment qu'il est possible d'amorphiser partiellement un film très mince avant d'effectuer une recroissance épitaxiale sur une couche dopée. Finalement, une implantation ionique à relativement haute température (jusqu'à 500 °C) a été étudiée afin de doper les accès sans amorphiser totalement le film mince, ce qui est critique dans le cas des dispositifs FDSOI et FinFET. Nous montrons que les niveaux d'activation après implantation sont trop faibles pour obtenir des bonnes performances et que l'implantation ionique « chaude » est prometteuse à condition d'être utilisée avec un autre mécanisme d'activation comme le recuit laser.

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## Low temperature devices (FDSOI, TriGate) junction optimization for 3D sequential integration

3D sequential integration is a promising candidate for the scaling sustainability for technological nodes beyond 14 nm. The main challenge is the development of a low temperature process for the top transistor level that enables to avoid the degradation of the bottom transistor level. The most critical process step for the top transistor level fabrication is the dopant activation that is usually performed at temperature higher than 1000 °C. In the frame of this Ph.D. work, different solutions for the dopant activation optimization at low temperature (below 600 °C) are proposed and integrated in FDSOI and TriGate devices. The technique chosen for the dopant activation at low temperature is the solid phase epitaxial regrowth. First, doping conditions have been optimized in terms of activation level and process time for low temperatures (down to 450 °C) anneals. The obtained conditions have been implemented in FDSOI and TriGate devices leading to degraded electrical results compared to the high temperature process of reference (above 1000 °C). By means of TCAD simulation and electrical measurements comparison, the critical region of the transistor in terms of activation appears to be below the offset spacer. The extension first integration scheme is then shown to be the best candidate to obtain high performance low temperature devices. Indeed, by performing the doping implantation before the raised source and drain epitaxial growth, the absence of diffusion at low temperature can be compensated. This conclusion can be extrapolated for TriGate and FinFET on insulator devices. Extension first integration scheme has been demonstrated for the first time on N and PFETs in 14 nm FDSOI technology showing promising results in terms of performance. This demonstration evidences that the two challenges of this integration i.e. the partial amorphization of very thin films and the epitaxy regrowth on implanted access are feasible. Finally, heated implantation has been investigated as a solution to dope thin access regions without full amorphization, which is particularly critical for FDSOI and FinFET devices. The as-implanted activation levels are shown to be too low to obtain high performance devices and the heated implantation appears a promising candidate for low temperature devices if used in combination with an alternative activation mechanism.

## Optimisation des jonctions de dispositifs (FDSOI, TriGate) fabriqués à faible température pour l'intégration 3D séquentielle

L'intégration 3D séquentielle représente une alternative potentielle à la réduction des dimensions afin de gagner encore en densité d'une génération à la suivante. Le principal défi concerne la fabrication du transistor de l'étage supérieur avec un faible budget thermique; ceci afin d'éviter la dégradation du niveau inférieur. L'étape de fabrication la plus critique pour la réalisation du niveau supérieur est l'activation des dopants. Celle-ci est généralement effectuée par recuit à une température supérieure à 1000 °C. Dans ce contexte, cette thèse propose des solutions pour activer les dopants à des températures inférieures à 600 °C par la technique dite de recristallisation en phase solide. Les conditions de dopage ont été optimisées pour améliorer le niveau d'activation et le temps de recuit tout en réduisant la température d'activation jusqu'à 450°C. Les avancées obtenues ont été implémentées sur des dispositifs avancés FDSOI et TriGate générant des dispositifs avec des performances inférieures aux références fabriquées à hautes températures (supérieures à 1000 °C). En utilisant des simulations TCAD et en les comparant aux mesures électriques, nous avons montré que la région la plus critique en termes d'activation se trouve sous les espaceurs de la grille. Nous montrons alors qu'une intégration dite « extension first » est le meilleur compromis pour obtenir de bonnes performances sur des dispositifs fabriqués à faible température. En effet, l'implantation des dopants avant l'épitaxie qui vise à surélever les sources et drains compense l'absence de diffusion à basse température. Ces résultats ont par la suite été étendus pour des dispositifs TriGate et FinFETs sur isolants. Pour la première fois, l'intégration « extension first » a été démontrée pour des N et PFETs d'une technologie 14 nm FDSOI avec des résultats prometteurs en termes de performances. Les résultats obtenus montrent notamment qu'il est possible d'amorphiser partiellement un film très mince avant d'effectuer une recroissance épitaxiale sur une couche dopée. Finalement, une implantation ionique à relativement haute température (jusqu'à 500 °C) a été étudiée afin de doper les accès sans amorphiser totalement le film mince, ce qui est critique dans le cas des dispositifs FDSOI et FinFET. Nous montrons que les niveaux d'activation après implantation sont trop faibles pour obtenir des bonnes performances et que l'implantation ionique « chaude » est prometteuse à condition d'être utilisée avec un autre mécanisme d'activation comme le recuit laser.