Built-In Self-Test of Flexible RF Transmitters Using Nonuniform Undersampling

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To my parents ...

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Abstract

The advent of increasingly powerful Integrated Circuits (IC) has led to the emergence of the Software Defined Radio (SDR) concept, which brought the sector of secured mobile communications into a new era. The outstanding performance of these systems results from optimal trade-offs among advanced analog/Radio Frequency (RF) circuitry, high-speed reconfigurable digital hardware and sophisticated real-time software. The inherent sophistication of such platforms poses a challenging problem for product testing. Currently deployed industrial test strategies face rising obstacles due to the costlier RF test equipment, longer test time and lack of flexibility. Moreover, an SDR platform is field-upgradeable, which means it will support standards and scenarii not considered during the design phase. Therefore, an in-field test strategy is not anymore 'a nice to have' feature but a mandatory requirement. In this context, our research aims to invent and develop a new test methodology able to guarantee the correct functioning of the SDR platform post-fabrication and over its operational lifetime. The overall aim of our efforts is to reduce post-manufacture test cost of SDR transceivers by leveraging the reconfigurability of the platform.

For tactical radio units that must be field-upgradeable without specialized equipment, Built-in Self-Test (BIST) schemes are arguably the only way to ensure continued compliance to specifications. In this study we introduce a novel RF BIST architecture which uses Periodically Nonuniform Sampling (PNS2) of the transmitter (TX) output to evaluate compliance to spectral mask specifications. Our solution supports a stand-alone implementation, is scalable across a wide set of complex specifications and can be easily applied for in-field testing with small added hardware. Compared to existing analog/RF test techniques, this approach is not limited to a given TX architecture and does not rely on an ad-hoc TX model, which makes it ideal for SDR testing.

Keywords : RF BIST, Mixed-Signal/RF Test, In-Field Test, Software Radios, Periodically Nonuniform Sampling, Subsampling

Résumé

Le secteur de communications sécurisés et portables connait une véritable révolution avec l'apparition des plateformes dites radios logicielles (Software Defined Radios, SDRs). Les performances exceptionnelles de ces systèmes sont les résultats d'une interaction assez complexe et souvent peu évidente entre le logiciel embarqué, le circuit de traitement numérique et les blocs mixtes analogiques/RF. Cette complexité limite la testabilité du produit fini. La méthodologie de test utilisée actuellement a atteint ses limites dues au cout élevé, le long temps de test et le bas degré de généralisation. De plus, les plateformes SDRs peuvent évoluer sur le terrain et elles vont supporter des standards et des scénarios qui n'ont pas été considérés pendant le la phase de conception. Donc, une stratégie de test sur le terrain (en ligne) n'est plus une caractéristique optionnelle mais une nécessité. Dans ce contexte, le but de notre recherche est d'inventer et développer une méthodologie de test capable de garantir le bon fonctionnement d'une plateforme SDR après la production et pendant sa vie. Notre objectif final est de réduire le coût du test en profitant de la reconfigurabilité de la plateforme.

Pour les radios logicielles qui doivent être mises à jour sur le terrain sans équipement spécial, les stratégies Built-In Self-Test (BIST) sont, sans doute, le seul moyen de garantir la conformité aux spécifications. Dans ce mémoire, nous introduisons une nouvelle architecture de test RF BIST qui utilise la technique de sous-échantillonnage nonuniforme à la sortie de l'émetteur (TX) d'une SDR afin d'évaluer la conformité de la masque spectrale. Notre solution s'appuie sur une implémentation autonome, est modulable et peut être appliquée pour le test sur le terrain avec des modifications minimes. Par rapport aux autres techniques de test analogiques/RF, cet approche ne dépends pas de la architecture du TX, ni d'un modèle ad-hoc, ce qui est idéale pour le test des SDRs.

Mots clés : RF BIST, Test analogique mixt/RF, test sur terrain, radio logicielle, SDR, sous-échantillonnage nonuniform de deuxième ordre, sous-échantillonnage

Contents

Symbols & Abbrevations

$*$	Convolution operator
β	Kaiser window parameter
$\delta(t)$	Dirac impulse
$\hat{x}$	Estimate of parameter x
$\lceil * \rceil$	ceiling operation
$\lfloor * \rfloor$	floor operation
μ	Step parameter for LMS algorithm
ε_G	Gain mismatch between two channels
B	Signal Bandwidth
D	Phase delay between 2 ADCs
$f(\cdot)$	Continuous time function
$F(f)$	Frequency domain representation
$f[\cdot]$	Discrete time function
f_c	Career Frequency
f_l, f_H	RF signal position, $f_l = f_c - B/2$ and $f_H = f_c + B/2$
f_s	Sampling frequency
$J(\cdot)$	Quadratic cost function
k	$\left\lceil \frac{2f_l}{B} \right\rceil$
k^+	$k + 1$
n_w	Number of FIR taps
$P_{1\text{dB}}$	1dB Compression Point
ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter
AM	Amplitude Modulated
AMS	Analog and Mixed Signals
ATE	Automatic Test Equipment
auRX	auxiliary receiver
BER	Bit Error Rate
BIST	Built-In Self-Test
CBS	Charge-Based Sampling
DCDE	Digitally Controlled Delay Element
DfT	Design for Testability
DUT	Device Under Test
EVM	Error Vector Magnitude
FC	Fault Coverage
FIR	Finite Impulse Response

FM Frequency Modulated

FoM Figure of Merit

I/Q In phase: Quadrature

IC Integrated Circuits

IMD Intermodulation Distortion

IP3 Third Order Interception Point

LMS Least Mean Squares

LNA Low Noise Amplifier

LO Local Oscillator

MLMS Multivariable Least Mean Squares

OFDM Orthogonal Frequency-Division Multiplexing

PA Power Amplifier

PAE Power-Added Efficiency

PCB Printed Circuit Boards

PHY Physical layer

PNS2 Periodically Nonuniform Sampling of Second order

QAM Quadrature Amplitude Modulation

RF Radio Frequency

RMS Root-Mean-Square

RX Receiver

SDR Software Defined Radio

SNR Signal-to-Noise Ratio

SoC System on Chip

TIADC Time-Interleaved Analog-to-Digital Converter

TX Transmitter

VBS Voltage-Based Sampling

WCDMA Wideband Code Division Multiple Access

YL Yield Loss

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Chapter 1

Introduction

1.1 Background

The unabated improvement in speed and integration density of integrated circuits (IC) has made possible the Software Defined Radio concept proposed by Mitola [Mitola, 1993]. An SDR is a Radio in which some (or all) of the physical layer functions are programmable. The advent of the Software-Defined Radio (SDR) platform [Woh et al., 2011] can be traced back to the defense industry, motivated by the fact that the multitude of increasingly complex military digital communication standards could not coexist in the field without a novel, flexible radio architecture. Consequently to the introduction of the SDR paradigm, nowadays reliable and interoperable terminals spanning hand-held, vehicular, airborne and dismounted radios, as well as base-stations (fixed and maritime) are routinely deployed.

The benefits of SDR, compared to the traditional radio systems, are compelling:

- Traditional hardware based radio devices limit cross-functionality and can only be modified through physical intervention. By contrast, software defined radio technology provides an efficient and comparatively inexpensive solution to this problem, allowing multi-mode, multi-band and/or multi-functional wireless devices that can be enhanced using software upgrades.
- SDR enables a family of radio products to be implemented using a common platform architecture, allowing new products to be more quickly introduced into the market.
- SDR enables software to be reused across different radio products, reducing development costs dramatically.
- Remote reprogramming, allowing debugging to be carried out while a radio is in service, thus reducing the effort and costs associated with operation and maintenance.

The outstanding flexibility and performance of these radios result from careful trade-offs among advanced analog/RF circuitry, high-speed reconfigurable digital hardware and sophisticated real-time software (Fig. 1.1). However, the inherent adaptability of these multistandard platforms hinders the testability of the finished units. Established mixed-signal and RF test strategy are either too time-consuming (thus costly) or can't ensure compliance with several modulations standards, including those yet to appear. Unlike conventional transmitters, SDR

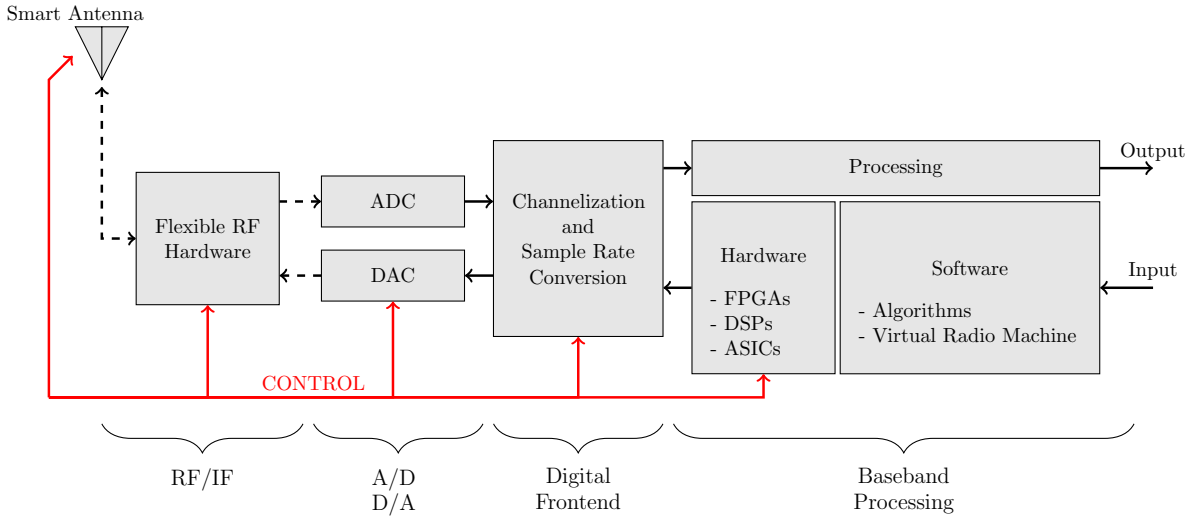


Figure 1.1: General architecture of an SDR

platforms must satisfy strict requirements under a wide variety of operating modes. Furthermore, rugged tactical radio units are expected to remain in service for many years, continuously evolving to support newer standards, through software-only field upgrades. Finally, an SDR tactical radio could possibly remain in storage or reserve for long periods, and then be reactivated, reprogrammed and put in active service in a matter of minutes. Ensuring the operational compliance of the terminal in such a dynamic situation over timespans of years is a vital concern. Thus, new test strategies must be invented, able to cover thoroughly and efficiently all key specifications of the radio unit. In this context, the aim of our work is to invent and develop a new test methodology able to guarantee the correct functioning of the SDR platform post-fabrication and over its operational lifetime

1.2 Previous Work

Over the past few years, analog and mixed-signal test and testability has been a subject of intense research. Traditional production testing of transceivers relies on specialized machines, known as Automated Test Equipment (ATE) units, [Wolf et al., 2006; Cruz et al., 2010]. ATEs are fast, accurate and reconfigurable, but also very expensive and hard to master. Besides, they are too cumbersome and fragile for the harsh conditions typical of tactical radio deployments. These shortcomings gave impulse to continuing research efforts for cost effective alternatives.

One such alternative, borrowed from digital testing research, is the idea of introducing Built-In Self-Test (BIST) techniques to eliminate or reduce the need for external instrumentation. Analog and mixed-signal (AMS) BIST techniques consist in placing the test circuitry directly on the same die (or on-board) as the desired Device Under Test (DUT) and generally entail additional circuitry and reuse of resources available (DSP, converters, memory). Compared to the digital test strategies that have matured to a high-level of automation (insertion of test ports and generation of test vectors), the test of AMS BIST strategies are still device (or architecture) specific. It could be argued that this is mainly because, contrariwise to digital circuits, truly generic analog faults model are yet to be defined.

Several AMS BIST techniques targeting specifically RF transceivers (RF BIST) have been proposed. The loopback approach is one of the most cited RF BIST technique [Onabajo et al., 2009; Negreiros et al., 2007; Dabrowski and Bayon, 2004; Nassery and Ozev, 2012; Haldes

et al., 2005]. In a nutshell, RF loopback consists in using the transmitting part (TX) to excite some parts or all of the receiver (RX) . The key feature is to add components that allow the reconfiguration of the on-board (or on-chip) resources to carry out some type of characterization.

Loopback BIST is an attractive proposition, although it has two major drawbacks. The first one is fault masking, a situation where a (non-catastrophic) failure of the TX is covered up by an exceptionally good RX, or the inverse. A marginal product could then go undetected (test escapes). The second drawback of BIST loopback is that it is not applicable directly to all transceivers architectures (e.g. [Dabrowski and Ramzan, 2010]). In spite of its shortcomings, loopback BIST has been often implemented and reported as effective: Onabajo et al. [2009]; Negreiros et al. [2007]; Dabrowski [2003]; Dabrowski and Bayon [2004]; Haldes et al. [2005]; Nassery and Ozev [2012]. The large number of publications shows the continuing interest in the topic.

Several sensitization techniques that aim to improve loopback observability (i.e. combat fault masking) have been proposed. In Erdogan and Ozev [2008]; Nassery and Ozev [2012] the authors rely on analytical behavioral models and simple input stimuli (sinusoid or multi-tone signals) to extract the most important nonlinearities and IQ imbalances in a quadrature transceiver (phase mismatch, gain mismatch, DC offset, and time-skew). This approach yields few test-escapes and demands low computational effort. However, it is limited by the completeness of the model. Under configurations unforeseen by the model, the entire test strategy will fail.

Another interesting RF BIST strategy is 'alternate test', in which the standard specifications are predicted from a set of 'easily' measurable parameters that are strongly correlated with the specifications one wishes to check [Natarajan et al., 2008; Halder et al., 2008; Haider et al., 2003; Maliuk et al., 2010]. The alternate tests are based on heuristic models, obtained a priori through simulations. These alternate tests are prone to errors such as test-escapes and yield loss, which are hard to predict. Test metrics coverage estimation techniques can help only if an extremely large number of units can be measured beforehand. Tactical radio unit production runs are far below these numbers.

It's evident that the SDR unit itself is a sophisticated RF instrument, i.e. a powerful platform that could be harnessed for test purposes, if some form of BIST strategy could be devised and implemented on it. However, the adoption of the previous mentioned RF BIST proposals for tactical SDR platforms is inherently hampered by the fact that RF systems BIST schemes generally target a fixed architecture, are optimized for a specific standard, or require very large training sets, and are, as such, better suited for factory test of mass market products. Test strategies that use a given fault model must necessarily hold assumptions on the operation modes of the radio, whereas in SDR platforms nearly all aspects are field-configurable. In this scenario, specification-based testing seems unavoidable. The outstanding challenge for SDR testing is then how to conduct specification testing without external equipment.

1.3 Our Work

The aim of our work is to propose and develop a new test methodology able to guarantee the correct functioning of the SDR platform. An example of such a platform, developed by Thales Communications & Security, is shown in Fig. 1.2. Our key idea is to use an alternate loopback path to observe the TX output signal just ahead of the antenna. The output waveform is routed back into the last stage of the main receiver (RX) chain (the ADCs), by using a small amount of analog circuitry, some digital control of clock delays, and a lot of complex signal processing. In effect, an auxiliary subsampling receiver (auRX) based on Periodically Nonuniform Sampling of second order (PNS2) provides an alternate demodulation path to characterize the main TX.

Figure 1.2: FlexNet. Vehicular wideband SDR platform sold by Thales Communications and Security.

This is feasible because the demodulation channel requirements in TX test mode are somewhat less stringent (i.e. no blockers) than during normal radio use.

We propose two similar implementations differing on how the sampling process is carried out: a voltage-based sampling (VBS) implementation and a charge-based sampling (CBS) implementation. The VBS BIST implementation places stringent requirements on the added undersampling circuitry, and suffers from jitter in the two clock signals driving them. The CBS implementation, lessens these burdens by means of charge-domain sampling. The effectiveness of the two BIST architectures was verified by way of simulations using a behavioral model of an homodyne transmitter written in `Matlab`. We conducted a theoretical analysis, built a model from analytical equations, and then ran extensive simulations. The two architectures were compared. The results of the comparison show that the CBS BIST architecture performs better, is more robust against clock jitter and is easier to implement. The CBS auRX loopback gives us an accurate estimate of TX performance across the whole output frequency range while relaxing the technological requirements on the added circuit blocks.

A crucial specification for TX compliance is the Adjacent Channel Power Ratio (ACPR), which is rarely addressed by existing BIST techniques [Halder et al., 2008] due to the complexity of the measurement. Our proposed BIST scheme aims to fill this gap and extract the ACPR accurately. It can also handle less demanding measurements, such as Third Order Interception Point (IP3) , gain, and I/Q imbalance without any hardware modifications, using existing signal processing algorithms.

Our test solution is scalable across a wide set of complex specifications and can be easily applied for in-field testing with modest additional cost. Compared to existing analog/RF test techniques, this approach is not limited to a given TX architecture and does not rely on an ad-hoc TX model, which makes it ideal for SDR testing. Interestingly, our approach can also be profitably applied in TX architectures that use pre-distortion compensation to improve power amplifier (PA) linearity, when the RX channel is idle.

1.4 Research Contributions

The overall objective of the research described in this dissertation is to develop an low-cost SDR BIST strategy for post-manufacturing and in-field test.

First, we invented a novel BIST architecture for SDR testing, aimed at specification test using loopback. The specification-based test strategy relies on the I/Q RX ADCs and PNS2 to characterize the TX path separately from the RX path. Our initial efforts target spectral

mask estimation at the output of the TX for any mode of operation and architecture. We show that this architecture lends itself well to a simple standalone implementation and can be wholly implemented within the SDR platform.

The main obstacle for the PNS2 reconstruction is to have an accurate estimate of an incrementally controlled delay element. We introduced an LMS-based estimation algorithm that addresses the uncertainties in our BIST architecture: time delay and gain mismatch. Our algorithm solves these issues robustly and opens the road for a complete self-calibrating BIST architecture.

Finally, we developed an improved implementation of the BIST architecture which uses CBS that is more robust and performs better.

1.5 Thesis Organisation

This dissertation is organized as follows. Chapter 3 briefly presents the most common architectures of an SDR platform. The fundamentals figures of merit that quantify the performance of an RF transceiver are quickly reviewed. The purpose of this section is to give a better understanding of the challenges faced by the test engineers when dealing with modern transceivers platforms.

The state of the art in the field of testability of RF systems is introduced in Chapter 4. The most frequently reported RF test strategies are discussed. As the field of SDR testing is relatively new, the literature is focusing mainly on the test of consumer products RF devices. The discussion is centered around the possibility of adjusting these techniques so they will meet the challenges introduced by the flexibility of an SDR platform.

Chapter 5 introduces the mathematical tools on which our proposed test strategy is based. The concept of periodically nonuniform sampling (PNS2) is explained by relating it with classic Nyquist sampling and undersampling. Then, we discuss the advantages of PNS2 over other possibilities and we motivate our choice. The most critical limitations of PNS2 are also given considerable attention.

Chapter 6 gives the implementation of our proposed test strategy. Two different architectures are discussed and compared. Here we examine the concerns and potential problems that could arise and we propose solutions to mitigate them. The models and the simulations parameters are also explained in here. Extensive simulations show the feasibility and the potential of the proposed technique.

The final chapter presents our conclusions and perspectives for future works. We list several directions of research that arose from this study.

Chapter 2

Résumé (Français)

2.1 Introduction

Le secteur des communications sécurisés et portables connait une véritable révolution avec l'apparition des plateformes dites radios logicielles (Software Defined Radios, SDRs). Dans ces plateformes, une grande partie des fonctionnalités de la radio sont obtenues grâce au logiciel et à des blocs électroniques numériques programmables. Ceci confère au produit fini une grande flexibilité pour s'adapter à une large gamme de modulations et scénarios d'utilisation, mais aussi la possibilité d'une économie d'effort de développement par l'utilisation du même code sur plusieurs générations de plateformes matérielles.

Les caractéristiques effectives du produit fini sont le résultat d'une interaction complexe et souvent peu évidente entre le logiciel embarqué, le circuit de traitement numérique et le bloc mixte RF/analogique (voir Fig. 2.1). Le développement de chacun de ces composants au niveau de l'état de l'art requiert des connaissances approfondies et des outils spécifiques.

Le SDR est une plateforme multifonctions flexible, configurable par logiciel et pouvant évoluer dans le futur. Actuellement, ces plateformes sont testées essentiellement par le bias des applications existantes, c.à.d. avec des montages ad hoc difficilement modifiables en utilisant des ATE (Automatic Test Equipments). Cette méthodologie a atteint ses limites dues au coût élevé de l'outillage RF externe, du long temps de test et du manque de flexibilité. Pour réduire le cout de test et par conséquence le coût du produit, l'industrie requiert des stratégies de test capables d'identifier rapidement les unités défectueuses de façon indépendemment de leur application. Dans ce contexte, le but de notre recherche est d'inventer et développer une méthodologie de test capable de garantir le bon fonctionnement d'une plateforme SDR après la production et sur le terrain.

Dans ce manuscrit, on introduit une nouvelle architecture de rebouclage qui est conçue pour éviter le masquage et pour permettre un test complet des transrecepteurs SDR en fin de production et sur le terrain. L'idée fondamentale de notre proposition est de tester d'abord l'émetteur en utilisant un circuit auxiliaire BIST. Le but de ce circuit est de sous-échantillonner le signal à la sortie de TX et de le transférer au processeur numérique à l'aide des deux convertisseurs CAN intégrés dans la chaine de réception. La conversion du signal RF est réalisée en utilisant une technique de sous-échantillonnage non-uniforme décrite plus en détail dans une section future. Cette approche permet d'éviter le masquage de défauts dans la technique de rebouclage

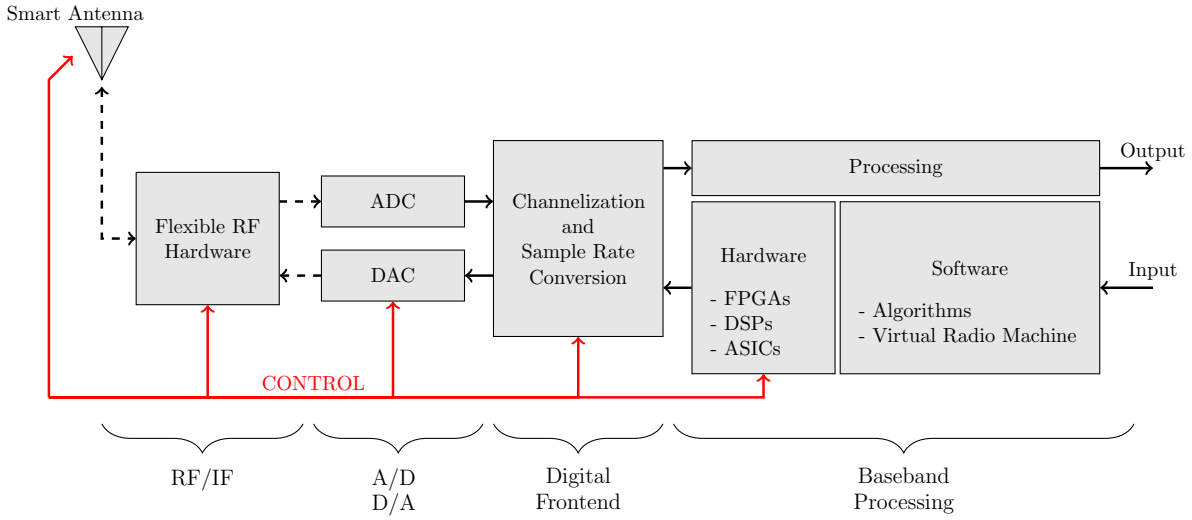


Figure 2.1: Architecture générale d'une SDR

classique, est flexible et supporte une implémentation simple.

Nos efforts initiaux se focalisent sur la caractérisation du masque spectral à la sortie du TX. Plus particulièrement, on s'intéresse à la mesure de la puissance dans les canaux adjacents (Adjacent Channels Power Ratio - ACPR) qui est très rarement adressé dans les BISTs existantes à cause de la complexité des leurs mesures. Néanmoins, notre technique peut mesurer des spécifications moins compliqués en utilisant des algorithmes de traitement de signal sans modifications hardware.

La contribution principale de nos travaux consiste dans la proposition d'une technique de test d'un émetteur SDR basée sur la technique de sous-échantillonnage nonuniforme. Celle ci permet la caractérisation de TX dans toutes les modes d'opération. Notre but final est d'éliminer les problèmes de masquage de défauts existants dans un rebouclage classique.

Ce chapitre consiste en un résumé du rapport en anglais et il est structuré comme suit. La première section résume les plus importantes caractéristiques qui définissent une radio logicielle. La section suivant décrite l'état de l'art du domaine de testabilité des systèmes mixtes RF/Analogiques en général, en se focalisant en particulier sur le cas des transceivers radio. Ensuite, notre architecture de test et des résultats obtenus en simulation sont présentés. La dernière section contient des conclusions et perspectives pour de futurs travaux.

2.2 Radio logicielle

Une radio logicielle est un émetteur/récepteur radio réalisé principalement par logiciel et dans une moindre mesure par matériel. Dans un système radio classique, l'émission/réception est assurée par des composants matériels (oscillateurs, filtres) spécifiques et adaptés aux systèmes auxquels il est destiné. Il n'est donc souvent pas possible d'utiliser d'autres systèmes sans changer le matériel et donc l'intégralité du récepteur. C'est l'avancement des plateformes (DSP, FPGA) et des algorithmes de traitement numériques qui a permis l'apparition des radios logicielles. Dans ces systèmes, les traitements réalisés classiquement par des circuits analogiques (filtrage, décimation, démodulation, décodage) peuvent être désormais réalisés de façon logicielle. Cela confère une universalité et une grande adaptabilité à l'émetteur/récepteur. En effet, il suffit de changer ou d'adapter le logiciel pour fonctionner avec un système radio différent.

Dans la littérature la radio logicielle a été présentée pour la première fois par Mitola dans Mitola [1993]. Aujourd'hui les radios logicielles sont utilisées par exemple dans les réseaux radio-mobiles (GSM, UMTS, etc.) au niveau des stations de base (BTS, Base Transceiver Stations) et comme systèmes de communications militaires. Les avantages d'une radio logicielle par rapport à une structure classique de transceiver RF sont :

- le développement de plusieurs produits radios en utilisant une seule architecture, ce qui écourte le délai de commercialisation
- permettre la réutilisation du logiciel par différents produits radios ce qui réduit le cout de développement
- la programmation à distance qui permet la mise-à-jour et la maintenance du produit à distance

Idéalement, une radio logicielle ne serait composée que par des unités de traitement numérique connectés par l'intermédiaire de CNAs et de CANs à l'antenne. Cependant, un schéma idéal n'est pas réalisable à cause des limites technologiques et on retrouve dans une radio logicielle des composants analogiques : amplificateurs de puissance, mélangeurs. Ils sont les composants analogiques/mixtes qui limitent la testabilité des plateformes SDRs qui constituent le coeur de notre recheche.

2.3 Test RF

Dans le chapitre précédent nous avons décrit la complexité et la flexibilité des plateformes SDR. Nous avons vu que, pour l'utilisateur final ceci confère au produit fini la possibilité pour s'adapter à une large gamme de formations et scénarii d'utilisation. De plus, pour le client s'ajoute la possibilité d'une économie d'effort de développement par l'utilisation du code sur plusieurs générations de plateformes matérielles.

Néanmoins, les caractéristiques effectives du produit fini sont le résultat d'une interaction complexe et souvent peu évidente entre le logiciel embarqué, le circuit de traitement numérique et le bloc mixte RF/analogique. Cette complexité rend le test du produit fini extrêmement compliqué et coûteux.

Dans cette section, on expose une vue d'ensemble des techniques de test des circuits électroniques les plus prometteuses. Ensuite, on analysera comment ces techniques peuvent être adaptées pour le test des plateformes radio logicielles.

2.3.1 Test et testabilité des systèmes électroniques

Réaliser le test d'un circuit signifie détecter qu'un circuit ne fonctionne pas conformément aux spécifications (pour des raisons de fonctionnalité logique, de vitesse de fonctionnement ou encore de niveaux électriques). Dans la majorité des cas, le test sert uniquement à distinguer les circuits « bons », c'est-à-dire pouvant être livrés au client, des circuits « mauvais » qui sont à éliminer. La cause exacte du mauvais fonctionnement n'a la plupart du temps pas à être analysée.

Dans certains cas cependant, la cause du mauvais fonctionnement doit être identifiée. C'est le cas d'une plateforme SDR qui est modulaire et où l'identification de la cause et du mauvais module est souhaitée. Dans ce cas, le test n'est plus suffisant ; il doit être complété par une phase de diagnostic, qui nécessite une analyse beaucoup plus longue et détaillée. La technique de test que l'on a proposé cible donc l'identification de la cause du mauvais fonctionnement.

Le mauvais fonctionnement d'un circuit peut provenir d'une erreur de conception, d'un problème lors de la fabrication ou d'un problème survenant pendant l'exécution de l'application, soit à cause du vieillissement du circuit, soit à cause de son environnement (radiations, particules, etc.). Dans cette recherche, on s'intéresse aux techniques de test qui ont pour objectif la détection de problèmes liés à la fabrication ou au vieillissement, mais pas à la conception. En fin de fabrication le circuit est supposé exempt d'erreur de conception.

On peut distinguer deux types de test : test hors ligne et test en ligne. Un test dit hors ligne correspond au test de fin de fabrication effectué lorsque le circuit n'est pas encore placé dans son environnement opérationnel. Par opposition, un test en ligne est un test exécuté par le circuit, alors qu'il est connecté dans son environnement opérationnel et que l'application est en cours d'exécution. Le test peut être effectué en parallèle de l'application (test en ligne continu) ou pendant certaines interruptions courtes (test en ligne périodique). Pour une radio logicielle qui est capable d'évoluer sur le terrain, le test en ligne est essentiel pour garantir le bon fonctionnement du système après une mise à jour. Pendant notre recherche nous nous sommes intéressés au test hors ligne ainsi que au test en ligne des ces plateformes.

Que le test de la fonction du circuit soit effectué en ligne ou hors ligne, il peut utiliser soit une approche fonctionnelle, soit une approche structurelle.

L'approche fonctionnelle consiste à définir des vecteurs de test permettant de parcourir tous les modes de fonctionnement possibles du circuit, tels qu'ils sont spécifiés dans la fiche technique (ou le cahier des charges). Un tel test est très proche des simulations faites par un concepteur pour vérifier l'absence d'erreur de conception. Dans le cas d'un circuit très simple, purement combinatoire, cette approche revient à vérifier la table de vérité de la fonction globale réalisée par le circuit. Une telle approche a deux inconvénients dans le cas d'un circuit complexe :

- tout d'abord, l'exhaustivité du test n'est généralement pas envisageable et la tentative de détecter le plus grand nombre de problèmes possibles conduit à des séquences de test excessivement longues ;

- peut-être encore plus important, aucune mesure fiable n'existe pour indiquer le niveau de qualité atteint par un jeu de vecteurs de test fonctionnels

L'approche structurelle consiste à partir de la structure interne du circuit et à vérifier le bon fonctionnement des éléments de base. L'objectif d'une approche structurelle n'est pas de détecter des erreurs de conception, une telle vérification se doit de permettre la validation de la fonctionnalité globale du circuit.

L'avantage de cette approche est de permettre l'obtention de séquences de test plus courtes et d'une quantification du niveau de qualité du test, pour des hypothèses de dysfonctionnement données. L'inconvénient est justement une efficacité limitée à ces hypothèses, c'est-à-dire au modèle de fautes choisi. Aujourd'hui l'approche structurelle est utilisée plutôt par les tests des circuits numériques. Ceci est possible parce que pour les circuits numériques il a été développé des modèles qui couvrent une bonne partie des défauts existants. Les circuits analogiques mixtes ne disposent pas de modèles suffisement généralisés et, pour l'instant, le test de ces circuits est basé presque complètement sur des approches fonctionnelles.

Enfin une stratégie de test n'est jamais parfaite. Ça signifie qu'il y a une probabilité finie qu'un circuit bon soit considéré mauvais où qu'un circuit mauvais passe le test. Aucune de ces situations n'est pas souhaitable. Afin de quantifier les performances d'une stratégie de test deux facteurs de mérite sont souvent utilisés Yield Loss (YL) et Fault Coverage (FC) qui sont

définis comme suit :

$$\begin{aligned} \text{YL} &= \frac{\text{number of healthy circuits that fail the test}}{\text{number of good circuits}} \\ \text{FC} &= 1 - \frac{\text{number of faulty circuits that pass the test}}{\text{number of faulty circuits}} \end{aligned} \tag{2.1}$$

L'objectif de chaque stratégie de test est donc de maximiser le FC et minimiser le YL.

2.3.2 Défis dans le test des systèmes RF

La croissance rapide de la complexité des circuits et l'évolution vers la haute intégration (VLSI – Very Large Scale Integration) rendent le test du circuit en production extrêmement difficile et couteux. En effet, il est estimé que le test des circuits AMS/RF peut couter jusqu'à 50 % du cout total de production. Afin de réduire ce coût il est donc indispensable de développer de nouvelles méthodologies de test plus efficaces. Dans cette section on analyse quels sont les défis rencontrées par le monde académique et industriel.

En parallèle de l'accroissement de complexité des circuits AMS, on remarque aussi une évolution vers la haute densité des circuits imprimés et des technologies d'encapsulation. Ceci fait apparaitre un problème de points d'accès et donc une accessibilité limité. Par contre, la capacité de contrôler et observer les sorties de chaque bloc est nécessaire pour la caractérisation complète d'un circuit. Afin d'améliorer l'observabilité et la contrôlabilité, une solution habituelle est d'ajouter circuits auxiliaires qui permettrons de générer de stimuli et de mesurer les performances du circuit à tester. Cependant, dans ce cas il faut faire attention de ne pas détériorer les performances du circuit à tester. Surtout la chaine RF qui est particulièrement sensible.

Malgré l'augmentation considérable de la complexité des circuits, la pression ne cesse de s'accroître pour diminuer les temps de conception et le coût de production. Comme le test est un facteur important dans le coût total de production, il est nécessaire que la stratégie de test soit à bas coût.

Comme déjà discuté dans la section précédente, si les circuits numériques bénéficient de modèles bien généralisés, ce n'est pas la même situation pour les circuits analogiques mixtes ou il manque des modèles universellement acceptés et rapide à simuler. Par conséquence les ingénieurs de test doivent attendre la fabrication du prototype pour pouvoir commencer à déboguer. Aujourd'hui, les experts sont d'accord que ce flux de production séquentielle/test n'est plus rentable et il doit être reconsidéré.

Ensuite, en plus des défis classiques précédemment rappelés, les plateformes SDRs introduisent de nouveaux challenges encore plus difficiles à respecter : les besoins de flexibilité. Par rapport aux systèmes de communication classiques, les radios logicielles sont capables de communiquer dans un spectre très large bande de fréquences et de standards de modulation. De même façon, une stratégie de test doit garantir que la plateforme fonctionne correctement dans tous ces scénarii.

Enfin, il faut noter que les SDRs sont utilisées dans un nombre croissant d'applications critiques, au niveau de vies humaines (comme par dans les applications militaires) ou au niveau financier (domaine bancaire). En parallèle, la probabilité de défaillances transitoires augmente avec l'évolution des technologies. Un aspect de test jusque-là méconnu dans la plupart des domaines commence donc à se démocratiser : réaliser un test du circuit pendant l'exécution normal de l'application et non pas seulement en fin de fabrication ou en maintenance. Un test en ligne est obligatoire pour les SDRs qui doivent garantir le bon fonctionnement du circuit pendant toute sa vie.

Pour résumer cette section, les chercheurs et les industriels n'ont pas encore convergé vers une stratégie de test AMS/RF généralisée. Toutefois, ils sont d'accord que la meilleure solution

Figure 2.2: Automated RF test equipment ATES500 developed by DiagnoSYS

pour remplir cet objectif est d'impliquer l'ingénieur de test aussi tôt possible dans le cycle de développement du produit. Ceci va permettre aux concepteurs et aux ingénieurs de test de partager leur expérience et de travailler ensemble pour trouver le meilleur compromis Cette paradigme est connue comme Design for Testability et elle s'est répandue dans la dernière décade. Dans la suite one verra quelles les techniques de test DfT pour les radios logicielles les plus prometteuses. La section suivante se constitue un point de départ qui nous permettra d'introduire notre stratégie de test.

2.3.3 Etat de l'art du domaine de testabilité des systèmes RF

Actuellement les plus utilisées solutions de test des circuits RF adoptées par l'industrie, les équipements ATEs (Fig. 2.2), donnent les informations les plus précises des circuits RF. Étant des montages ad-hoc difficilement modifiables et utilisant des équipements externes très coûteux, les ATEs sont devenus les plus grands consommateurs dans les processus de test (de point de vu coût et temps de test). Afin de minimiser les besoins d'équipement externes l'industrie commence à s'orienter vers des solutions plus flexibles telles que les circuits Built-In Self-Test.

Les BIST sont des circuits auxiliaires au circuit à tester (Device Under Test, DUT) qui permettent d'améliorer la mesure d'une certaine spécification en réduisant la nécessité des dispositifs externes. Pour les transcepteurs RF, les plus importantes stratégies de test utilisent la technique de rebouclage détaillée ensuite.

Pour les architectures présentant dans le même temps un émetteur et un récepteur l'idée de boucler les deux composants est apparue de manière naturelle et s'est avérée utile pour le test du circuit. Le principe de ce bouclage (représenté graphiquement dans la figure 2.3) est de générer le signal numérique dans le processeur, de le convertir à la haute fréquence par l'intermèdiaire de l'émetteur et ensuite de le router vers le récepteur par un circuit BIST. Le signal est après analysé par le processeur et les décisions sont prises. Dans la figure 2.3 la boucle couvre l'entier *transceiver* mais des autres points d'insertion peuvent être envisagés. Par exemple pour un test plus élaboré on peut envisager une méthodologie progressive : dans un premier temps on teste le *transceiver* sans considérer les amplificateurs (PA et LNA) qui d'habitude sont les plus problématiques. Dès que on caractérise le circuit de basse puissance on revient à l'architecture

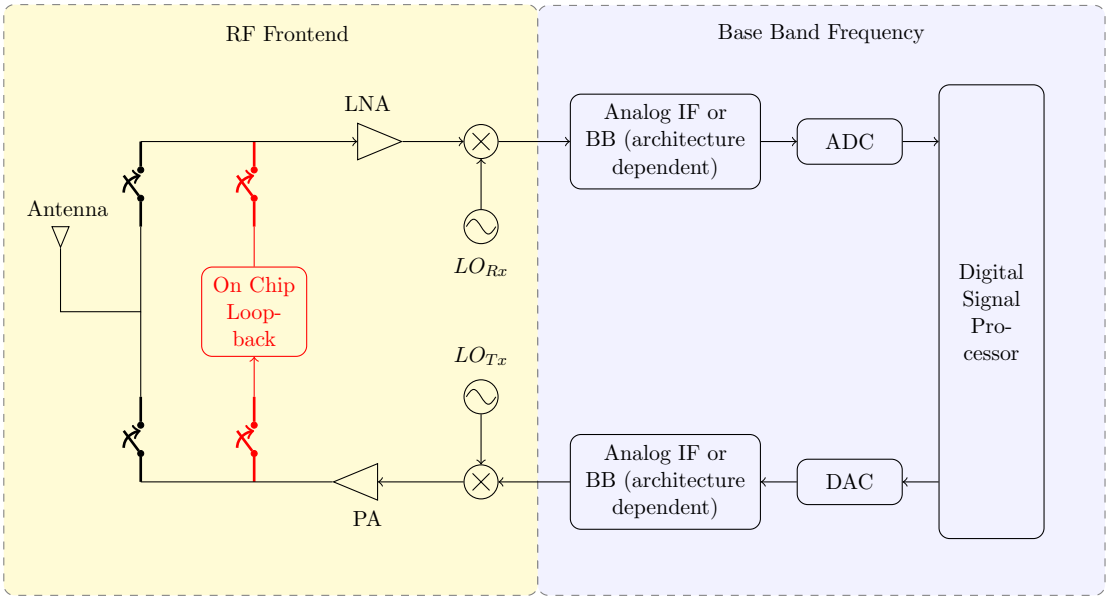


Figure 2.3: Principe du bouclage

de test présentée dans la figure 2.3 (voir Fan [2010]).

La technique de rebouclage a attiré l'attention dernièrement grâce à ses avantages :

- Eliminer et/ou réduire la nécessité d'utiliser des dispositifs de mesure RF externes
- Réduction du coût du test
- Réutilisation des ressources déjà existante dans le DUT (convertisseurs, mémoires, processeurs)
- Possibilité de l'adapter pour le test en ligne sur le terrain

Toutefois, la technique de rebouclage soufre par une limitation majeure. En effet, le test de l'émetteur-récepteur comme un entier (sans avoir accès à des points internes) réduit le niveau d'observabilité et de contrôlabilité du système et peut déterminer un certain degré de masquage de défauts. Par exemple, un défaut dans un émetteur peut être masqué par un récepteur très puissant et vice-versa.

Afin de minimiser les effets de cette observabilité réduite et de maximiser la contrôlabilité et l'observabilité du DUT, plusieurs techniques ont été proposées dans la littérature. Les plus intéressantes sont décrites ensuite.

Une première idée pour réduire les effets de masquage de défauts et d'ajouter des circuits de mesure ou des capteurs RF aux points vitales du DUT et après utiliser leur sorties pour récupérer plus d'informations. Parce qu'ils sont insérés directement dans la voie RF ces capteurs altèrent le signal et les circuits d'adaptation des impédances nécessitent une attention spéciale. Une investigation des trois capteurs qui a considéré une fois la précision de mesure et d'autre fois l'impact sur le DUT a été fait en Natarajan et al. [2008] et a montré que le détecteur d'enveloppe donne les meilleurs performances.

Une deuxième famille de solutions pour améliorer l'observabilité de la technique de rebouclage utilise des modèles comportementaux des circuits AMS/RF. Les modèles comportementaux sont préférés aux modèles à base des transistors qui, malgré le fait qu'ils soient plus précis, sont beaucoup plus lourds à simuler. C'est pour cela qu'on retrouve dans la littérature de

plus en plus des travaux qui utilisent des modèles comportementaux qui représentent un compromis entre précision et complexité de la simulation. Considérons les algorithmes d'optimisation qui apparaissent aujourd'hui dans toutes les branches de la science et qui d'habitude sont très coûteux du point de vue du temps de calcul. L'utilisation de ces types d'algorithmes pour optimiser la chaine RF est pratiquement impossible si on utilise les modèles à base de transistors.

En se basant sur ces modèles l'équipe d'Ozev propose plusieurs stratégies de test des transcepteurs RF. Par exemple, dans Acar and Ozev [2007] les auteurs montrent que la voie RF peut être caractérisée à partir des mesures IQ en utilisant un modèle analytique. Avec leur technique, les paramètres vitaux d'un circuit RF (le gain, l'IIP3, le bruit, déséquilibre en amplitude et phase de la voie en quadrature) sont déterminés à partir du diagramme IQ. La méthode a été testé pour un émetteur *homodyne*. On présente ensuite le modèle utilisé. Soient $I(t)$ et $Q(t)$ les signaux bande de base *in phase*(I) et quadrature (Q). La sortie du modulateur sera :

$$x_M(t) = G_I I(t)\cos(\omega_C t + \phi_I) + G_Q Q(t)\sin(\omega_C t + \phi_Q) \tag{2.2}$$

où ω_C est la fréquence du porteur, G_I et G_Q, les gains des canaux I et Q et ϕ_I et ϕ_Q sont les phases des canaux I et Q. Pour mettre en évidence le déséquilibre en amplitude et phase on peut réécrire l'équation 2.2 comme suite:

$$x_M t = G\{I(t)\cos(\omega_C t) + (1+p)Q(t)\sin(\omega_c + \phi)\} \tag{2.3}$$

avec: $G = G_i$ le gain commun, $p = G_Q/G_I - 1$ le déséquilibre en amplitude et $\phi = \phi_I - \phi_Q$ le déséquilibre en phase. Si on modélise l'amplificateur de puissance comme dans Eq. 4.2 en considérant l'offset DC nul :

$$x_{RF}(t) = \alpha_1 x_M(t) + \alpha_2 x_M^2(t) + \alpha_3 x_M^3(t) \tag{2.4}$$

et on ajout un bruit gaussien blanc $n(t)$, on obtient le signal final de sortie:

$$x(t) = x_{RF}(t) + n(t) \tag{2.5}$$

Enfin, on peut écrire le signal bande de base reçu comme:

$$\begin{aligned} \hat{I}(t) &= (\alpha_1 + \Delta)[I(t) + (1+p)Q(t)\sin(\phi)] + \hat{n}(t) \\ \hat{Q}(t) &= (\alpha_1 + \Delta)(1+p)Q(t)\cos\phi + \hat{n}(t) \\ \Delta &= \frac{3}{4}\alpha_3\{I^2(t) + [Q(t)(1+p)]^2 + 2I(t)Q(t)(1+p)\sin(\phi)\} \end{aligned} \tag{2.6}$$

où $\hat{I}(t)$ représente le signal bande de base I reçu, $\hat{Q}(t)$ représente le signal bande de base Q reçu et Δ est une terme de compression non-linéaire.

A partir du modèle analytique présenté précédemment et de mesures des signaux bande de base, I et Q, on peut calculer le gain, l'IIP3, le bruit et le déséquilibre en amplitude et phase des voies en quadrature d'un émetteur RF (pour plus de détails voir Acar and Ozev [2007]).

Du point de vue de test des systèmes SDRs les méthodologies basées sur les modèles comportementaux ont leurs lacunes. D'abord, elles sont limitées par le degré de complétude du modèle. Si un défaut non prévu apparait dans le système, la stratégie de test va probablement échouer. De plus, pour les SDRs capable d'évoluer dans le futur ces types de modèles n'ont pas encore été développés.

Les tests des circuits RF basés sur la mesure des spécifications sont robustes et performantes mais on a vu que la mesure directe de ces spécifications est difficile à faire. Dans leur travaux (Natarajan [2010]; Natarajan et al. [2008]; Halder et al. [2008]; Chatterjee et al. [2009]; Haider

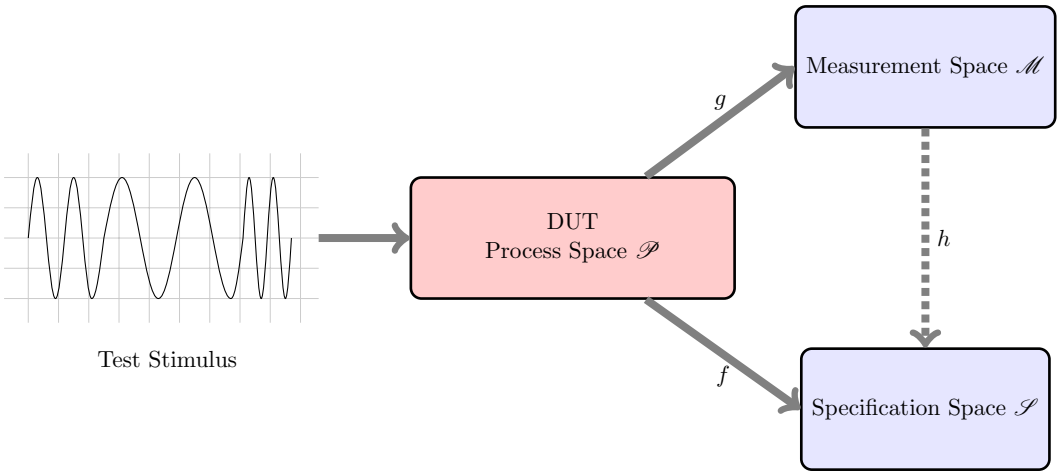


Figure 2.4: Principe des tests alternatifs

et al. [2003]), Chaterjee et son équipe ont introduit un nouveau paradigme dans le domaine de testabilité et de calibrage des circuits RF. Cette technique, appelée *tests alternatifs*, utilisent des algorithmes d'optimisation heuristiques (algorithmes génétiques, réseau neuronaux, ...) pour prédire les spécifications d'un circuit à partir d'un ensemble de paramètres plus facile à mesurer mais corrélés avec les spécifications.

Le principe de base (représenté graphiquement dans la figure 2.4) est décrit ensuite: une variation de n'importe quelle paramètre physique du DUT (largeur d'un transistor, une résistance, etc) dans l'espace des paramètres $\mathscr{P}$ affecte les spécifications du circuit $\mathscr{S}$ par une certaine facteur de sensibilité. Soit $\mathscr{M}$ l'espace des paramétrés mesurés qui est choisi tel que chaque variation d'un paramètre en $\mathscr{P}$ qui affecte l'espace $\mathscr{S}$ affecte aussi l'espace $\mathscr{M}$. Autrement dit il existe une forte corrélation entre l'espace $\mathscr{M}$ et $\mathscr{S}$. Pour chaque point en $\mathscr{P}$ on peut construire une fonction de mappage non-linéaire, $f : \mathscr{P} \rightarrow \mathscr{S}$. D'une manière similaire, on peut trouver une autre fonction de mappage $g : \mathscr{P} \rightarrow \mathscr{M}$. Enfin, dans Variyam and Chaterjee [1998] a été montré qu'on peut construire une fonction non-linéaire $h : \mathscr{M} \rightarrow \mathscr{S}$ en utilisant des méthodes de régression statistiques non-linéaires multivariées. A l'aide de h on peut maintenant prédire les spécifications d'un circuit $\mathscr{S}$ à partir de l'espace des mesures $\mathscr{M}$. Pour construire la fonction g la méthode *Multivariate Adaptive Regression Splines* (Mars) peut être utilisée.

Dans Haider et al. [2003] les spécifications d'un récepteur *heterodyne* (le gain et l'IIP3) sont obtenus en utilisant le paradigme de tests alternatifs. Pour exposer les non-linéarités du système les stimuli de test sont des sinusoïdes de large amplitude dont les paramètres (amplitude, fréquence) sont générés avec des algorithmes de recherche itératives. Les mesures sont faites avec un analyseur de spectre placé à la sortie du mixer. Les résultats montrent que le gain et le IIP3 peut être prédis avec une erreur de $\pm$1dB. De manière similaire, un émetteur *homodyne* est testé dans Natarajan et al. [2008]. Pour réduire la nécessité d'un dispositif de mesure externe, des trois capteurs intégrés sont utilisés.

Les stratégies de tests alternatifs basés sur des modèles statistiques commencent à être de plus en plus utilisées dans le test des systèmes fabriqués en masse. Cependant, pour les systèmes SDRs des modèles précises sont difficiles à obtenir.

2.3.4 Conclusions

Pour résumer cette section, actuellement on ressent le besoin d'une stratégie de test généralisé pour les systèmes AMS/RF. Plusieurs solutions ont été proposées (tests alternatifs, test à base

de modèles comportementaux) mais plus de recherche dans cette direction est nécessaire.

La complexité et la flexibilité des plateformes radio logicielles amènent encore plus de challenges pour le test du produit fini. Les stratégies utilisées actuellement basée sur des équipements externes ne sont plus faisables du point de vue économique. Comme alternative, plusieurs solutions BIST ont été proposées. Les BIST sont des circuits auxiliaires au circuit à tester qui permettent d'améliorer la mesure d'une certaine spécification en réduisant la nécessité des dispositifs externes.

Parmi les solutions BIST proposées, pour les transrecepteurs SDRs, la technique de rebouclage est, sans doute, la plus prometteuse. Quand même, cette technique est limitée par des problèmes de masquage de défauts. Afin de surpasser cette limitation, plusieurs techniques ont été proposées, dont les plus prometteuses rappelées dans ce chapitre.

L'étude bibliographique réalisée nous a permis de tirer quelques conclusions. D'abord, afin de simplifier le test d'un transrécepteur SDR des circuits BIST doivent être considérés. Le test de rebouclage constitue une solution viable si on adresse le problème de masquage de défauts. Enfin, pour l'instant, pour le test des transcepteurs qui ne bénéficient pas des modèles de défauts généralisés, les approches fonctionnelles sont inévitables. Comme tenu de ces conclusions, nous avons proposé et développé une stratégie de test flexible pour transcepteurs SDR. L'architecture est décrite dans la section suivante.

2.4 Application de la technique de sous-échantillonnage non-uniforme au test intégré des émetteurs RF flexibles

2.4.1 Introduction

Dans les sections précédentes nous avons discuté la complexité des architectures radios logicielles et nous avons montré les implications de cette complexité sur le test du produit final. Ensuite nous avons introduit les stratégies de test les plus prometteuse présentées dans la littérature. Parmi les techniques publiées, le technique de rebouclage s'est idéntifiée comme étant la plus apte à répondre à nos besoins. Cependant, la technique de rebouclage est affectée par des problèmes de masquage de défauts qui provoque une réduction des performances de test. Dans ce chapitre, on introduit une nouvelle architecture de rebouclage qui est conçue pour éviter le masquage et pour permettre un test complet des transcepteurs SDR en fin de production et sur le terrain.

L'idée fondamentale de notre proposition est de tester d'abord l'émetteur en utilisant un circuit auxiliaire BIST. Le but de ce circuit est de sous-échantillonner le signal à la sortie de TX et de le transferer au processeur numérique à l'aide des deux convertisseurs CAN intégrés dans la chaine de réception. La conversion du signal RF est réalisée en utilisant une technique de sous-échantillonnage non-uniforme décrite dans plus de détails dans une section future. Cette approche permet d'éviter le masquage de défauts dans la technique de rebouclage classique, est flexible et supporte une implémentation simple.

Nos efforts initiaux se focalisent sur la caractérisation du masque spectral à la sortie du TX. Plus particulièrement, on s'intéresse à mesurer la puissance dans les canaux adjacents (Adjacent Channels Power Ratio - ACPR) qui est très rarement adressé dans les BISTs existantes à cause de la complexité de leurs mesures. Néanmoins, notre stratégie peut mesurer des spécifications moins compliqués en utilisant des algorithmes de traitement de signal sans des modifications hardware.

Les avantages clés de la technique proposée sont :

- Flexibilité dans une large bande de fréquence. En effet la technique de test proposée

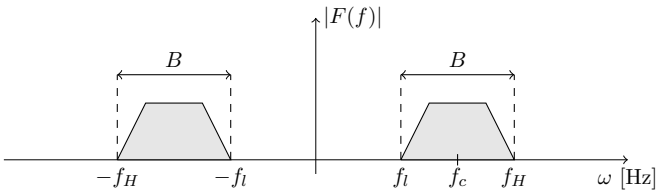


Figure 2.5: Bandpass Signal

peut caractériser le TX dans toutes les bandes de fréquence en modifiant seulement les coefficients d'un filtre numérique

- Un minimum d'extra hardware requis et la possibilité de réutiliser des ressources déjà existantes dans le circuit à tester.

- Permet d'éliminer les problèmes de masquages de défauts en testant d'abord l'émetteur indépendamment.

De plus notre architecture peut être utilisée aussi comme le circuit de feedback dans une stratégie de linéarisation de PA.

Pour résumer, la contribution principale de nos travaux consiste dans la proposition d'une stratégie de test d'un émetteur SDR basée sur la technique de sous-échantillonnage nonuniforme. Cette stratégie permet la caractérisation de TX dans toutes les modes d'opération. Notre but final est d'éliminer les problèmes de masquage de défauts existants dans une rebouclage classique.

Dans ce chapitre on introduit et on discute de la stratégie proposée. D'abord on commence par présenter quelques outils mathématiques qui constituent la base de cette stratégie. Ensuite, on montrera l'architecture générale du circuit BIST, on discutera des limitations principales et comment ces limitations ont été surpassées. A la fin, on verra les résultats obtenus en simulation nous allons tirer les conclusions et discuter des perspectives futurs.

Les travaux réalisés pendant cette thèse ont été publiés et présentés dans trois conférences internationales [Dogaru et al., 2013a,b, 2014].

2.4.2 Outil théoriques

Il est de notoriété publique qu'un signal continu $f(t)$ défini dans le domaine fréquentielle par sa transformée Fourier $F(f)$ et limité en fréquence $|f| < B$ peut être reconstruit à partir de ses échantillons discrets $f(nT/2)$ où $T = 1/B$. Cette technique s'appelle l'échantillonnage Nyquist. Il a été aussi démontré [Lin and Vaidyanathan, 1996; Kohlenberg, 1953] que, si le signal est limité dans une bande passante $f_l < |f| < f_l + B$ (voir Fig. 2.5), alors $f(t)$ peut être toujours reconstruit à une fréquence minimale $2B$ si le rapport f_l/B est un nombre entière. Cette technique est connue comme la technique de sous-échantillonnage uniforme. Si les contraintes précédentes ne sont pas respectées, Kohlenberg [Kohlenberg, 1953] a montré que le $f(t)$ peut être toujours reconstitué à une fréquence d'échantillonnage minimale à partir de deux jeux d'échantillons uniformément espacés $f(nT)$ and $f(nT + D)$ voir Fig. 2.6. Cette technique est connue comme sous-échantillonnage non uniforme de deuxième ordre (PNS2) et sera décrite ensuite.

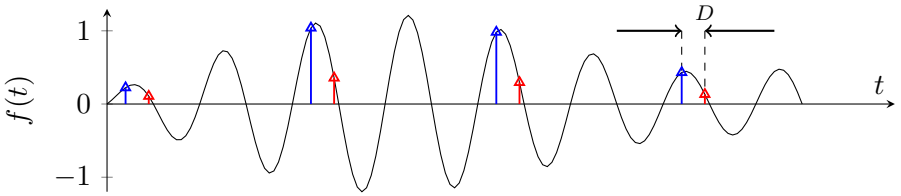


Figure 2.6: Time domain representation of PNS2 operation

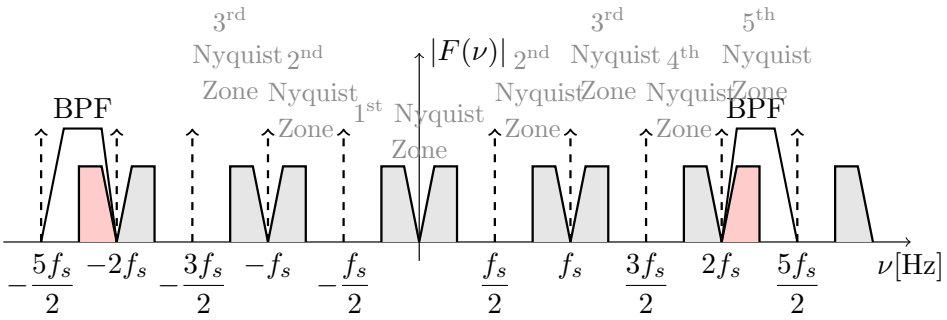


Figure 2.7: Frequency spectrum illustration of standard bandpass sampling

2.4.2.1 Sous-échantillonnage uniforme

Les avantages du sous-échantillonnage par rapport à l'échantillonnage sont évidents : la fréquence d'échantillonnage minimale nécessaire est corrélée à la largeur de bande du signal et pas à la position du signal. La technique d'échantillonnage est représentée graphiquement dans la Fig. 2.7. L'opération d'échantillonnage crée des copies du signal original dans chaque zone de Nyquist. Ensuite un filtre peut être utilisé pour récupérer une copie du signal à bande de bas.

Quand même, le choix du période d'échantillonnage f_s représente un souci. En effet, la relation entre f_s, la bande passante du signal B et la position du signal f_H est limité si on veut éviter le repliement spectral. Les combinaisons acceptable sont représentés graphiquement dans la Fig. 2.8a où f_s et f_H sont normalisés par rapport au B. Les régions en blanc representent des scénarios où le sous-échantillonnage peut être réalisé sans repliement spectral. Les régions en gris sont des régions qui doivent être évités pour n'avoir pas de repliement spectral.

On peut remarquer que la fréquence d'échantillonnage minimale est $f_s = 2B$, mais cette situations ne laisse pas de marges d'erreurs pour des imperfections de fabrication. Cette sensitivité augmente lorsque f_H/B augmente. Donc, l'implémentation pratique de la technique de sous-échantillonnage doit échantillonner plus rapidement que la fréquence théorique minimum. Même dans ce cas le repliement va apparaitre si le signal n'est pas bien positionné.

Prenons comme exemple le cas particulier d'un signal d'une bande passante de $B = 30$ MHz localisé au une fréquence de $f_l = 2$ GHz. Pour cet exemple, les périodes d'échantillonnage acceptées sont représentées par les régions blanches dans la Fig. 2.8b. Si on veut implémenter une période d'échantillonnage autour de valeur minimale $2B$, l'horloge d'échantillonnage doit avoir une précision de quelques KHz afin d'éviter le repliement spectral. La solution évidente pour relâcher ces contraints est d'augmenter la fréquence d'échantillonnage. Même dans cette situation pour l'exemple dans la Fig. 2.8b une fréquence autour de $f_s = 90$ MHz (plus grande que $2B$) nécessite une précision d'échantillonnage de quelques centaines de KHz.

Enfin, si la fréquence du signal change, les périodes d'échantillonnage changes aussi et doivent être recalculées.

Pour résumer, la technique de sous-échantillonnage est efficace, mais difficile à implémenter

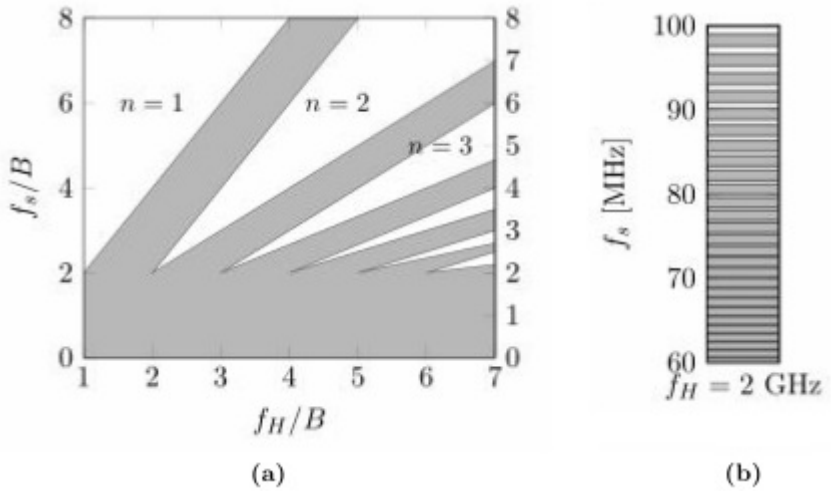


Figure 2.8: The constraints on the sampling rate f_s for undersampling [Vaughan et al., 1991]: 2.8a in general case and 2.8b a particular case where $f_H = 2.03$ GHz and $B = 30$ MHz. The white regions are situations where the undersampling will not result in aliasing. The gray regions represent conditions where alias is occurring.

sans entrainer des problèmes de repliement spectral.

2.4.2.2 Technique de sous-échantillonnage périodique non-uniforme de deuxième ordre (PNS2)

Les discussions précédentes suggèrent que la technique d'échantillonnage classique n'est pas adaptée pour le test des radios logicielles à cause de leur manque de flexibilité. En effet, une de plus importante caractéristique d'une radio logicielle est la flexibilité. Ça signifie que qu'elle est capable de fonctionner dans une gamme variée de point de fonctionnement (fréquence, débit, type de modulation, etc.). Une stratégie de test bien conçue devrait être capable de couvrir tous ces modes de fonctionnement avec un minimum d'effort. Ceci n'est pas le cas si la technique de sous-échantillonnage classique est utilisée.

Une alternative à la technique décrite est la technique de sous-échantillonnage périodique non-uniforme de deuxième ordre (PNS2). PNS2 permet la reconstruction d'un signal passe-bande à partir de deux jeux d'échantillons uniformément espacés à une fréquence Nyquist indépendante de la position du signal. PNS2 permet de surmonter les inconvénients de sous-échantillonnage classique et offre un niveau plus élevé de flexibilité.

PNS2 a été introduite par Kohlenberg [1953] et plus de résultats ont été présentés dans Lin and Vaidyanathan [1996]; Vaughan et al. [1991]. Kohlenber (Kohlenberg [1953]) a montré qu'un signal passband (Fig. 2.5) peut être reconstruit à partir de deux jeux d'échantillons uniformément espacés. La représentation graphique de PNS2 est donnée dans la Fig. 2.9. Fig. 2.9a représente le signal passband à récupérer. Fig 2.9b montre le spectre du premier train d'échantillons. Pour une meilleure visualisation ce spectre a été séparé entre le spectre positif (en haut) et le spectre négatif (en bas). De manière similaire on a tracé le spectre du deuxième train d'échantillons dans la Fig. 2.9c. Enfin, $S_A(\nu)$ et $S_B(\nu)$ dans la Fig. 2.9d représentent les interpolants (filtres de reconstruction) qui sont conçus pour récupérer le signal original. Ils sont calculés de façon que les composantes négatives de chaque spectre s'annulent dans la bande d'intérêt. Une analyse plus détaillée de comment ces interpolants sont calculés est donnée dans

le Chapitre 5.

On doit remarquer que notre but n'est pas de reconstruire le signal RF original mais de le décaler autour de 0 Hz (DC). Les spectres répétitives des $F_A(\nu)$ et $F_B(\nu)$ (voir Fig. 2.9) permet de récupérer pas seulement le signal original RF mais aussi un copie située autour de l'origine (DC). Donc, les spectres rouges dans la Fig. 2.9 représentent les interpolants qui reconstruisent le signal en bande de base. Considérons $f_{bb}(t)$ le signal à bande de base. La relation suivante peut être obtenue:

$$\begin{aligned} f_{bb}(t) &= s_A(t) * f_A(t) + s_B(t) * f_B(t) \\ &= \sum_{n=-\infty}^{+\infty} [f(nT)s_A(t-nT) + f(nT+D)s_B(t-nT-D)] \end{aligned} \tag{2.7}$$

où D est le retard entre les deux train d'échantillons, $s_A(t)$ et $s_B(t)$ sont définis par :

$$\begin{aligned} s_A(t) &= \frac{\mathrm{e}^{-j\pi BDk}(\mathrm{e}^{j2\pi f_1 t} - \mathrm{e}^{j2\pi f_0 t})}{2\pi Bt \sin \pi BDk} \\ &\quad + \frac{\mathrm{e}^{-j\pi BDk^+}(\mathrm{e}^{j2\pi (f_0+B)t} - \mathrm{e}^{j2\pi f_1 t})}{2\pi Bt \sin \pi BDk^+} \\ s_B(t) &= -s_A(t)\mathrm{e}^{-j2\pi BD(k-m)} \\ &\quad k = \lceil 2f_l/B \rceil \, , \, m = \lceil f_l/B \rceil \, , \, \gamma = \mathrm{e}^{-j2\pi BD} \end{aligned} \tag{2.8}$$

L'équation 2.7 est valable lorsque D respect les contraintes suivantes.

$$D \neq nT/k \tag{2.9a}$$

$$D \neq nT/(k+1), \forall n \in \mathbb{N} \tag{2.9b}$$

Les équations 2.8 ainsi que la Fig. 2.9d montrent que les fonctions utilisées pour reconstruire le signal $f_{bb}(t)$ ont des coefficients complexes. Dans la section suivante on montrera comment ces résultats théoriques peuvent être implémentés en pratique.

2.4.2.3 Implémentations hardware de la technique PNS2

Comme montré précédemment la technique PNS2 permet la reconstruction et le décalage d'un signal RF à partir de deux jeux d'échantillons uniformément espacés. Dans cette section on montre comment la technique PNS2 peut être implémentée en numérique à l'aide de deux filtres à réponse impulsionnel fini (FIR). Il existe plusieurs modalités de choisir les coefficients des FIRs, mais nous avons choisi d'utiliser une approche directe qui consiste en implémenter directement les équations 2.7 et 2.8.

Les interpolants à temps continu pourraient être implémentés à une période d'échantillonnage minimale de $2B$. Par contre, la discrétisation de ces fonctions ne peut pas être réalisée à un taux minimum sans déclencher du repliement spectral. En effet, on peut rémarquer facilement dans la représentation graphique dans la Fig. 2.9d que le signal d'intérêt occupe une bande de largeur B situé entre $-B$ et B en fonction de la position du signal original. Donc, afin d'éviter le repliement spectral on doit considérer un sur-échantillonnage de facteur deux. Compte tenu des remarques précédentes et à partir d'équation 2.8, les filtres FIRs sont exprimés comme suite:

$$f_{bb}(t) = \sum_{n=-n_w/2}^{n_w/2} f(t - nT/2)s_A^n + f(t - nT/2 - D)s_B^n \tag{2.10a}$$

$$s_A^n = s_A(t)\Big|_{t=nT/2} \tag{2.10b}$$

$$s_B^n = s_B(t)\Big|_{t=nT/2+D} \tag{2.10c}$$

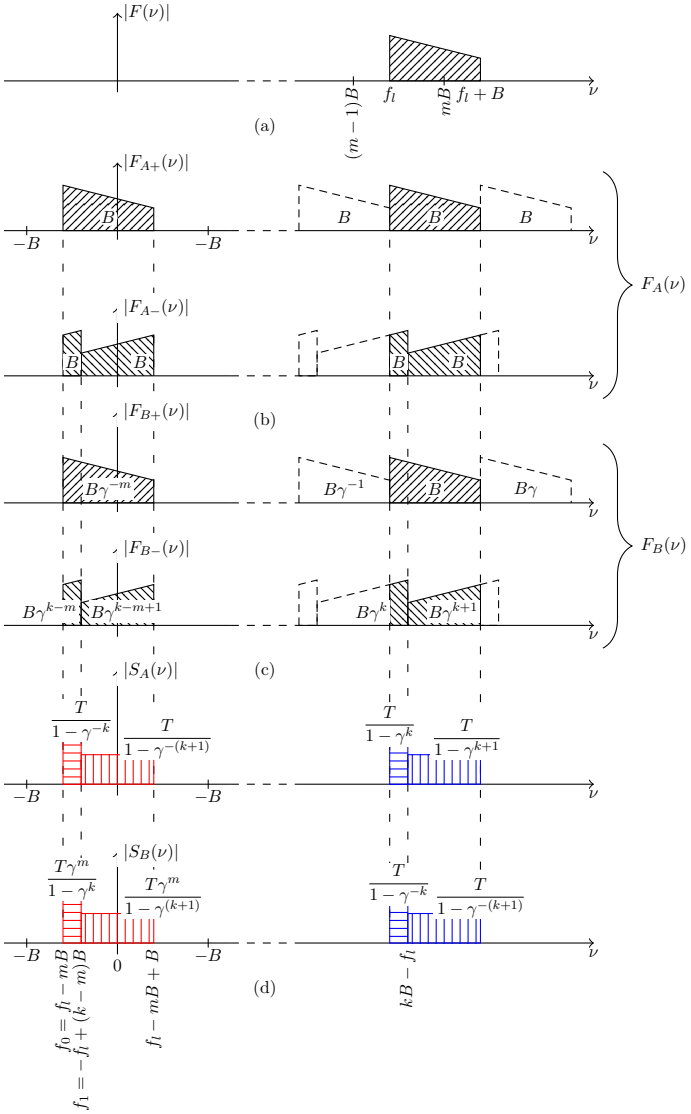


Figure 2.9: Periodically nonuniform bandpass sampling of second order. Fig. 2.9a represents the original passband signal to be reconstructed. Fig 2.9b sketches the spectrum $F_A(\nu)$ resulting from sampling by the sample set A. The top figure shows only the positive frequency components $F_{A+}(\nu)$ resulting from sampling, while the bottom figure shows only the negative frequency components $F_{A-}(\nu)$. The spectra of the set B is depicted as $F_{B+}(\nu)$ and $F_{B-}(\nu)$ in Fig. 2.9c. $S_A(\nu)$ and $S_B(\nu)$ in Fig. 2.9d represent the interpolants (reconstructing filters) which are designed to restore the original signal.

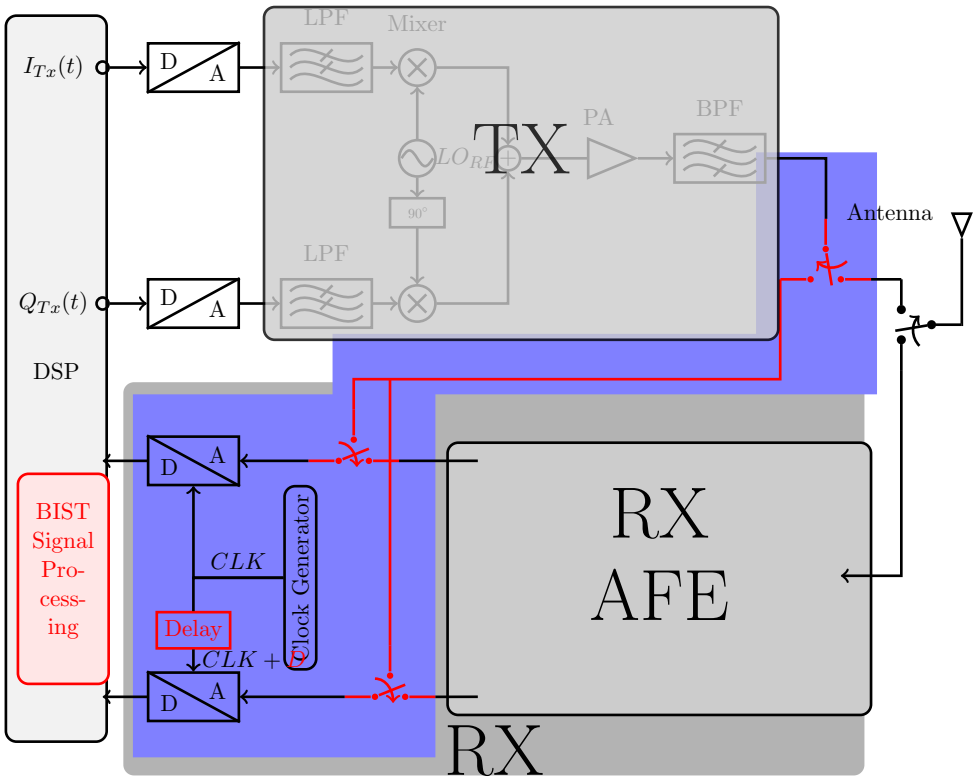


Figure 2.10: Block diagram of the proposed BIST architecture. The red blocks are the modification required to implement the loopback circuitry within the transceiver to enable self-test

Les coefficients des FIRs ont été obtenus en tronquant les fonctions continues 2.8. Dans ce contexte la troncation signifie qu'on a gardé un nombre fini de coefficients, n_w. Afin de minimiser les effets de la troncation, une fonction de fenêtrage Kaiser a été utilisée. D'autres fonctions auraient pu être choisies.

2.4.3 Description générale de l'architecture de test

L'architecture générale de la stratégie de test proposée est présentée dans la Fig. 2.10. L'idée de base est d'utiliser un circuit de rébouclage pour surveiller la sortie du TX. Le signal de sortie est rebouclé vers le dernier stage dans la chaine de réception en utilisant des circuits analogiques, un circuit de retard contrôlé en numérique et du traitement du signal complexe. En effet, le circuit BIST implémente la technique PNS2 décrite précédemment et fournit une chaine auxiliaire (plus simple) qui sert à caractériser l'émetteur. Ceci c'est faisable parce que les contraintes sur la chaine de démodulation durant le test sont moins fortes (pas de bloqueurs) que pendant l'opération normale.

Les blocs rouges dans la Fig. 2.10 sont les modifications nécessaires pour intégrer le circuit de test dans le transcepteur. Notre supposition fondamentale est que l'unité radio logicielle contient déjà des circuits qui peuvent être réutilisés pour le test. Notre idée est donc d'utiliser les plus des ressources possibles (RX ADCs, DSP, GPP, mémoires) afin d'implémenter la stratégie de test.

Le diagramme complet de la stratégie de test est montré dans la Fig. 2.11. Le signal RF

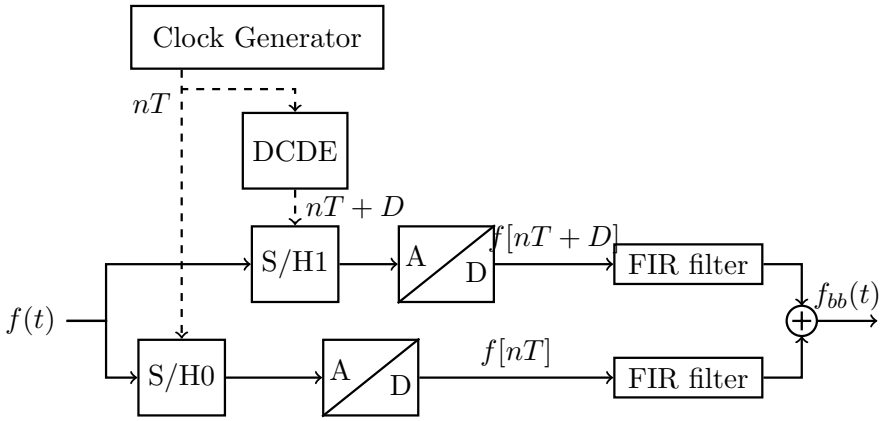


Figure 2.11: Complete block diagram of the proposed BIST architecture

à la sortie de l'émetteur est partagé entre deux échantillonneurs contrôlés séparément. Le bloc de retard variable (DCDE) introduit un retard entre les deux horloges. Les deux FIRs à coefficients complexes fournissent l'implémentation temps réel de la technique PNS2. Les deux échantillonneurs-bloqueurs sont nécessaires afin d'augmenter la bande passante des ADCs jusqu'aux fréquences RF. La vitesse d'échantillonnage des deux ADCs reste constante.

L'architecture de sous-échantillonneur est donc formée de trois blocs fondamentaux :

- Le bloc numérique qui sert à implémenter la technique PNS2 il est représenté par les deux filtres FIRs
- Les horloges et le générateur de retard variable (DCDE)
- Les échantillonneurs-bloqueurs (E/B) : sont les plus sensibles et difficiles à concevoir. Dans nos travaux nous avons montré que si on utilise deux E/B à l'intégration de charge on peut obtenir des meilleurs résultats et une robustesse améliorée.

Dans ce rapport nous avons discuté des meilleures architectures pour implémenter le circuit BIST proposé. Ensuite, nous avons montré les limitations les plus importantes et comment les surpasser. Dans la section suivante on va montrer les résultats les plus pertinents obtenus en simulation.

2.4.4 Résultats en simulation

L'analyse mathématique et les considérations pratiques discutées nous ont permis de développer une stratégie BIST complète qui contient des circuits hardware (analogiques, numériques et mixtes) et du logiciel. Nous avons modélisé tous ces aspects. Dans cette section nous montrons les modèles utilisés et les performances du BIST obtenues en simulation.

2.4.4.1 Paramètres générales de modélisation

La technique d'échantillonnage non-uniforme nécessite la simulation de chaque cycle de la porteuse. Afin de maintenir l'effort de calcul raisonnable les simulations présentées dans ce manuscrit utilisent de modèles temporels comportementaux en bande passante [Chen, 2005].

Dans une première étape le modèle d'un émetteur homodyne a été conçu en Matlab/Simulink. Le choix de l'architecture a été guidé par la flexibilité et le haut niveau d'intégrabilité de l'émetteur homodyne. Matlab a été choisi pour la richesse des bibliothèques fournies. Le diagramme de l'émetteur homodyne est montré dans la Fig. 2.12. La même figure contient aussi

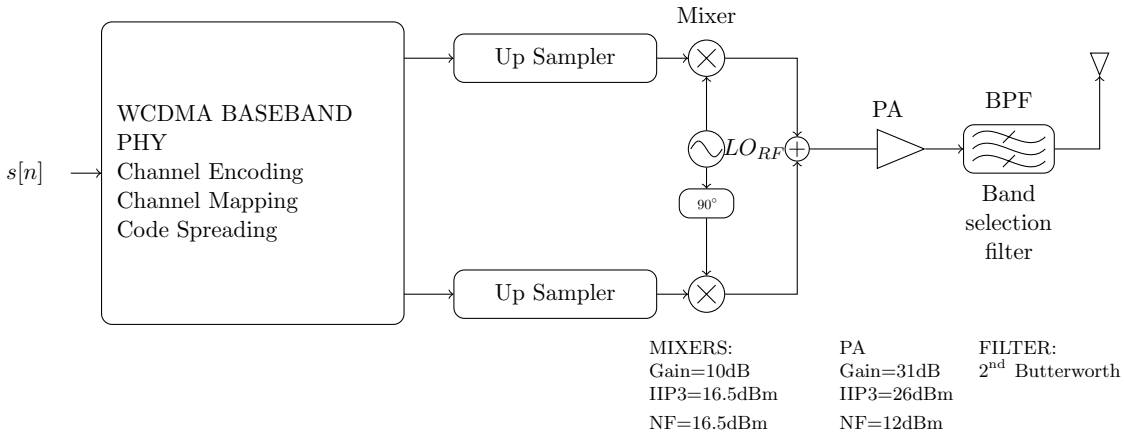


Figure 2.12: Block diagram of the simulated homodyne transmitter

les spécifications des blocs utilisées pendant la simulation. Le signal de test utilisé est un signal W-CDMA défini par le standard 3GPP ®TS 125.104 [Standard, 2013]. Il occupe une bande de fréquence de 5 MHz située à $f_c = 1890$ MH.

La modélisation passband suppose une période d'échantillonnage autour de 1 ps. Afin d'obtenir cette précision le signal bande de base à la sortie du bloc bande de base PHY a été sur-échantillonné. Nous avons aussi utilisé implémenté une technique d'interpolation linéaire. Cette période d'échantillonnage permet une simulation très précise du bruit d'horloge qui est un facteur important qui affecte les performances du BIST proposé. Considérant ces aspects, le temps de simulation de toute l'architecture reste raisonnable (quelques secondes).

Les deux ADCs composant le circuit BIST ont une résolution de 10 bits et une vitese d'échantillonnage de $T = 100$ MSamples/sec. Le choix a été imposé par les ADCs déjà présents dans la chaine de réception et qui on veut re-utiliser. Les deux filtres FIR sont implémentés en virgule fixe en utilisant le toolbox `Fixed Precision` sur Matlab.

2.4.4.2 Simulation de l'ACPR

La spécification ciblée dans ces travaux est la puissance dans les canaux adjacents (Adjacent Channel Power Ratio - ACPR) un paramètre vitale qui est rarement mesuré pas les autres techniques BIST. Pour l'émetteur, l'ACPR est parmi les plus importants facteurs de mérite au niveau du système. ACPR mesure la distorsion générée par le TX dans les canaux adjacents en fréquence et donne des informations précieuses sur les non-linéarités existants dans la chaine analogique.

Le standard W-CDMA défini l'ACPR comme le rapport entre la puissance dans le canal principal et les canaux adjacents. Le canal principal est considéré occuper une bande de 3.84 MHz autour de fréquence de porteuse f_c. W-CDMA impose la mesure d'ACPR pour quatre canaux adjacents situés à -10, -5, 5, 10 MHz du canal principal. Fig. 2.13 présente une représentation graphique de comment ACPR doit être estimer/mesurer et les positions de chaque canal. Ce signal sera utilisé dans la suite pour analyser les performances du BIST proposé.

Premièrement, on commence par analyser les effets de troncations dans l'implémentation des filtres FIRs. Pour ces simulations on considère que le jitter n'est pas présent. Fig. 2.14 montre l'évolution de l'estimation d'ACPR par rapport aux nombre des coefficients choisis. D'abord, on observe que la précision de la reconstruction dépend de la valeur du retard D. On a montré, en fait précédemment, que la valeur optimale pour le retard D est de $D = 1/(4f_c)$ (dans ce cas

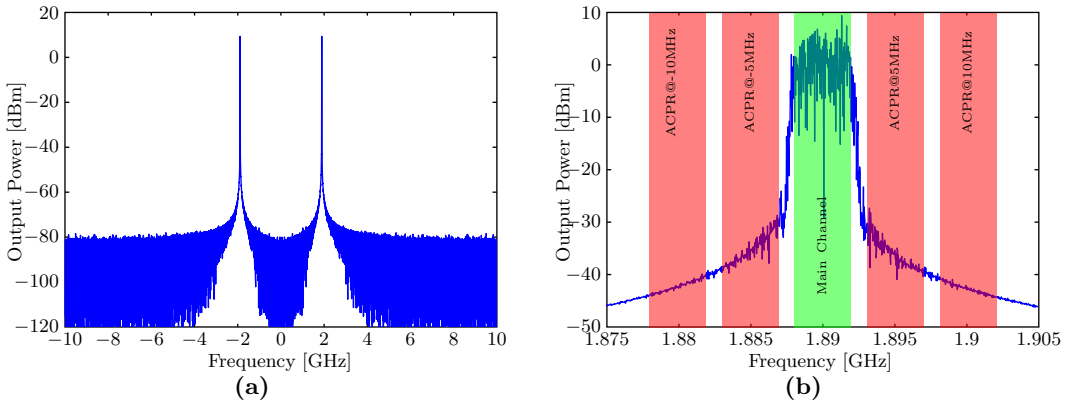


Figure 2.13: ACPR Measurement. Left figure shows the power spectrum of the signal at the output of the receiver. A FFT transform of 2^{19} points was used. The right figure shows the same spectrum around the center frequency f_c. The main channel and the adjacent channels used for ACPR calculation are highlighted.

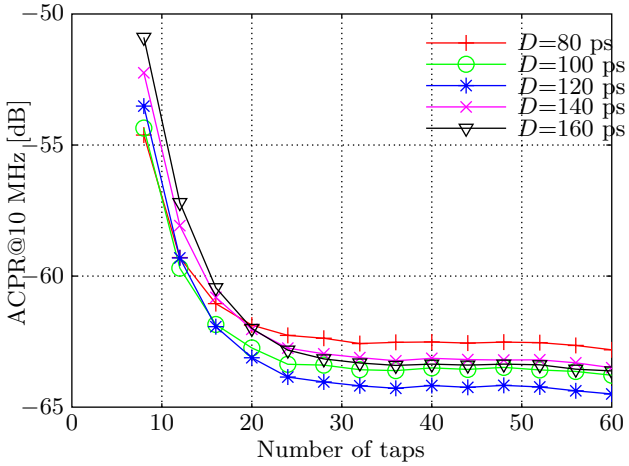


Figure 2.14: Evolution of the ACPR estimate w.r.t. the number of taps in FIR implementation and the value of D

particulier $D = 132$ ps). Il y a donc une marge suffisante pour le choix du D. Fig. 2.14 montre aussi que $n_w = 20$ coefficients pour les filtre FIRs offre un bon compromis entre complexité et performances.

Ensuite on impose $D = 100$ ps et $n_w = 30$ et on analyse les effets d'utilisation de la virgule fixe. Fig. 2.15 montre la dégradation de l'ACPR par rapport à la précision des filtres FIR. Les résultats confirment que 12 bits de précision sont suffisants pour implémenter la stratégie PNS2. Cette valeur sera utilisée dans la suite.

Jusqu'à maintenant on a considéré que les générateurs d'horloges sont idéaux et que les échantillonneurs/bloqueurs (E/B) sont basés sur le voltage. Dans la suite on présente les effets du jitter sur les performances du système BIST. Fig. 2.16 présente l'évolution de la dégradation d'ACPR par rapport au jitter de l'horloge. Les résultats montrent que l'architecture de test est sensible à jitter. L'architecture basée sur des E/B à l'intégration de charge reste plus robuste.

Considérons, par l'exemple le standard 3GPP qui spécifie des valeurs pour ACPR de moins -50 dBc à +/-10 MHz. Ça signifie que la première architecture peut vérifier la conformité au standard pour des valeurs de jitter jusqu'au 1.2 ps rms, lorsque l'architecture basée sur

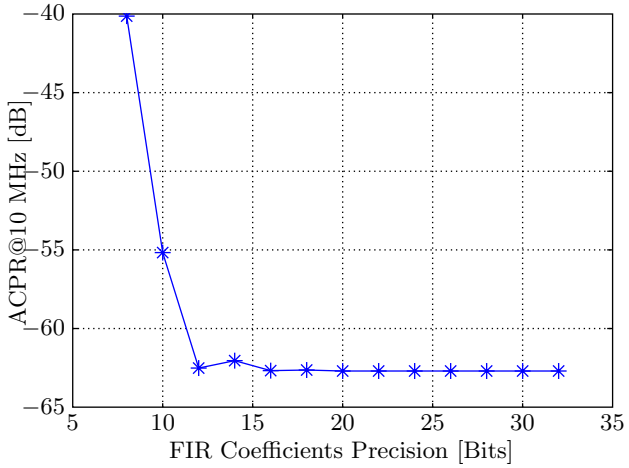


Figure 2.15: Evolution of the ACPR estimate w.r.t. FIR filters taps precision

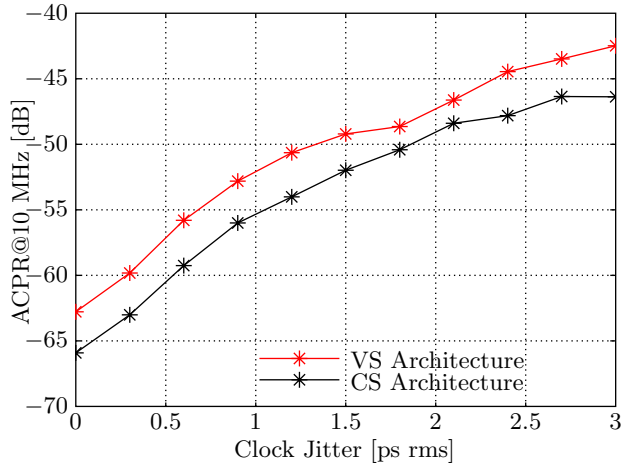


Figure 2.16: Evolution of the ACPR estimate w.r.t. jitter in the clock oscillator

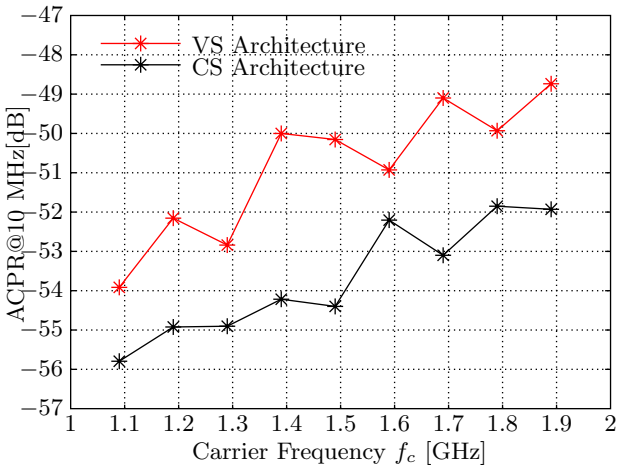


Figure 2.17: Evolution of the ACPR estimate w.r.t. carrier frequency

l'intégration de charge peut encore garantir la conformité pour des valeurs de jitter autour de 2ps rms. Les résultats sont très intéressants si on considère que les générateurs d'horloge fixes existants actuellement sur le marché peuvent générer des signaux à bas jitter (1 < ps rms, voir la famille CDC421AXXX [Texas Instrument] proposée par Texas Instrument).

Enfin, pour un jitter de 1.5 ps rms, nous avons étudié dans la Fig. 2.17 l'évolution d'ACPR pour plusieurs valeurs de la fréquence de porteuse f_c. Comme attendu, on remarque que les performances du BIST diminuent à une fréquence plus élevée. Cette dernière simulation est très intéressant car elle met en évidence la flexibilité de l'architecture de test proposée. En fait, pour changer la fréquence d'opération, il suffit de changer les coefficients des filtres et le retard D.

2.4.4.3 Conclusions

Dans cette section nous avons introduit une nouvelle architecture BIST conçue pour la caractérisation de systèmes d'émission flexibles. L'architecture BIST se comporte comme un récepteur complémentaire qui sert à minimiser les masquages des défauts de la technique de rebouclage. La stratégie proposée utilise une technique de sous-échantillonnage de 2ème ordre et cible l'estimation du masque spectral du récepteur. En fonction de comment l'échantillonnage est réalisé nous avons proposé deux architectures : une première qui utilise un échantillonnage classique et une deuxième qui est basée sur d'E/B à l'intégration de charge. La deuxième architecture est plus performant et réduit les contraintes liées au générateur d'horloge.

Nous avons modélisé le circuit de test et nous avons comparé les deux architectures. La stratégie proposée est flexible et robuste, a le potentiel de test en ligne et supporte une implémentation hardware simple.

2.4.5 Conclusions et perspectives

2.4.5.1 Conclusions

Ce mémoire adresse les défis dans le domaine de test RF. Une radio logicielle est un émetteur/récepteur radio réalisé principalement par logiciel et dans une moindre mesure par matériel. La flexibilité et la flexibilité exceptionnelles de ces systèmes limitent la testabilité du produit fini. La méthodologie de test utilisée actuellement a atteint ses limites dues au cout élevé, à long temps de test et à bas degré de généralisation. Dans ce contexte, le but de notre recherche est

d'inventer et développer une méthodologie de test capable de garantir le bon fonctionnement d'une plateforme SDR en fin de production et sur terrain.

L'étude présentée ici a été réalisée en deux étapes. Dans un premier temps, nous avons réalisé une recherche bibliographique approfondie sur le sujet de test RF et architectures radios logicielles. L'étude de complexité d'une plateforme SDR nous a aidé à comprendre les défis rencontrés par les ingénieurs de test. Un autre facteur limitant est la multitude des spécifications qui doivent être considérés. Pour les circuits RF, le seul moyen de garantir la conformité aux spécifications à bas cout sont sans aucun doute les techniques BIST. Parmi les stratégies BIST qui ciblent les SDRs, la technique de rebouclage est la plus prometteuse. Toutefois, cette technique peut être affectée par des masquages de défauts.

Dans un deuxième temps, nous avons introduit et discuté d'une nouvelle stratégie BIST conçue pour la caractérisation des systèmes d'émission flexibles. L'architecture BIST se comporte comme un récepteur complémentaire qui sert à minimiser les masquages des défauts de la technique de rebouclage. La stratégie proposée utilise une technique de sous-échantillonnage de 2ème ordre et cible l'estimation du masque spectral du récepteur. La stratégie proposé est flexible et robuste, a le potentiel de test en ligne et supporte une implémentation hardware simple.

2.4.5.2 Travaux futurs

La faisabilité et le potentiel de la technique proposé ont été prouvés en simulation. Par conséquence, la perspective la plus importante est de valider cette stratégie sur un banc de test conçu par Thales.

Un autre aspect qui a été discuté dans ce rapport, c'est la possibilité d'améliorer la stratégie BIST en développant un module d'autotest et auto-calibration. L'idée de base est d'utiliser des informations statistiques obtenues pendant les processus d'estimation du retard D.

L'étape de test et de calibration d'un transcepteur RF sont bien corrélées. Notre architecture pourrait être utilisée pour la calibration des PAs dans les émetteurs sans aucune autre modification.

Chapter 3

Software Defined Radio

Contents

3.1 Introduction

The Software Defined Radio (SDR) concept proposed by Mitola [Mitola, 1993] is a Radio in which some (or all) of the physical layer functions are programmable. The outstanding flexibility and performance of modern SDRs result from careful trade-offs among advanced analog/RF circuitry, high-speed reconfigurable digital hardware and sophisticated real-time software. Our works aims to develop an effective BIST strategy for highly-configurable high performance Software Defined Radio, such the one built and sold by Thales shown in Fig. 1.2.

Before starting to discuss potential test strategies, in the first part of this chapter we briefly introduce the most common architectures of an SDR platform. The second part of this chapter gives the figures of merits usually employed to asses the performance of an RF transceiver system. The purpose of this chapter is to give a better understanding of the challenges faced by the test engineers when dealing with modern transceiver platforms.

3.2 Some History

Engineers and scientists have been looking for innovative applications for RF technology ever since 1860s, when James Maxwell mathematically predicted the existence of electromagnetic waves capable of transporting energy across empty space. Following Heinrich Hertz's physical demonstration of radio waves in 1886, Nikola Tesla, Guglielmo Marconi, and others pioneered ways of manipulating these waves to enable long distance wireless communications. At the turn of the 19^{th} century, the radio had become the first commercial application of RF. Over the next three decades much effort was directed towards methods of transmitting and receiving signals, and later, due to WWII, to detect and locate objects at great distances.

Due in part to sustained growth in the radar and communications sectors, technological innovation in RF accelerated steadily throughout the remainder of the 20^{th} century and continues to do so today. The 21^{st} century is being arguably shaped by an incredible explosion in the evolution of communication systems. This technological progress coupled to the advent of DSP discipline and the availability of extremely compact DSP computing devices have led to the appearance of the Software Defined Radio.

3.3 What is an SDR

The term "Software Defined Radio"(SDR) was coined in 1991 by Joseph Mitola, who published the first paper on the topic in 1992 [Mitola, 1993]. Several definitions have been provided to describe SDR. The SDR Forum, working in collaboration with the Institute of Electrical and Electronic Engineers (IEEE) P1900.1 group define an SDR as a [SDR]: *"Radio in which some or all of the physical layer functions are software defined"*. In other words, an SDR refers to a radio communication system that can be configured to receive a wide range of modulated signals across a large frequency spectrum by means of a programmable hardware platform (see Fig. 1.1).

Compared to conventional systems where the radio communication is performed by hardware components (oscillators, filters) which are optimized for a specific protocol, in SDR the signal processing (filtering, decimation, demodulation, decoding) is implemented on general-purpose processors, a special-purpose processor(FPGA) or any combination of these. These characteristics give the SDR the flexibility to adapt to a wide range of usage scenarios. While the concept of SDR is not new, the rapidly evolving capabilities of digital electronics render practical many processes which used to be only theoretically possible.

To sum up, the benefits of an SDR w.r.t. to a conventional RF transceivers are:

- through replacement of software, the same equipment can be used to implement a range of radios for various application. In the the same time, this means a reduced development cost and faster time-to-market.

- improved flexibility

Because of their complexity, high cost of development and their novelty, the SDR are mostly employed in military applications and base stations of cellular infrastructure systems. Nonetheless, as the technology enabling the SDR platforms begins to mature, more and more commercial wireless communications providers will understand their advantages and start to use them in their devices.

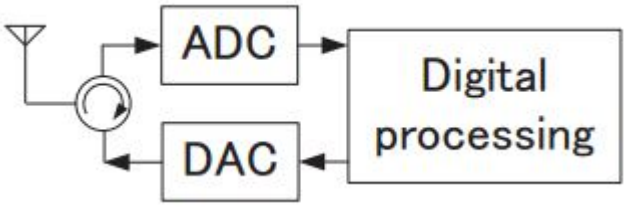


Figure 3.1: SDR concept as envisioned by Mitola [Mitola, 1993]

3.4 SDR Architectures

In order to understand the challenges of testing an SDR platform it is essential to examine the complexity and diversity of their design. In this section we discuss some of the most commonly deployed architectures and we show their advantages and limitations.

In Mitola's vision, the ideal SDR transceiver would be to attach an ADC and a DAC directly to an antenna as shown in Fig. 3.1. For the receiver side a DSP would read the converter, and then its software would transform the stream of data from the converter to any other form the application requires. For the transmitter side, the DSP would generate a stream of numbers that would be sent to a Digital-to-Analog Converter (DAC) connected to a radio antenna. Such a transceiver would provide maximum flexibility through the DSP.

Nonetheless, some limitations have to be considered. In many wireless applications the desired signal is accompanied by blockers which can be generated by nearby TX of the same communications standard (in-band blockers) or by any other TX (out-of-band blockers). Even more, for the reception side, the desired signal is usually very weak, whereas the blockers can be stronger by as much as 100 dB. Or, the ideal architecture from Fig. 3.1 offers equal fidelity for both the desired signal and the blockers, relying on ADCs to convert the entire signal. This imposes an impractical dynamic range for the ADC performances. Therefore, the ideal ideal scheme proposed by Mitola is not feasible w.r.t. practical constraints such as power consumption or ADC linearity, resolution and speed requirements.

For now, cutting-edge SDR platforms still rely on Analog Mixed-Signal (AMS) front-ends to filter the blockers and adapt the gain for reception and transmission. These AMS sections are much less flexible and have much lower scale of integration than the digital section [Razavi, 1997; Abidi, 1999]. It can be argued that the reconfigurability, adaptivity, performance, and scale of integration of modern SDRs are limited by their AMS portions [Poberezhskiy and Poberezhskiy, 2005]. The AMS portions of an SDR transceiver represent the focus of the section and of our research.

Depending on how the filtering and the amplification are done, several transceiver architectures have been proposed [Cruz and Carvalho, 2010; Mak et al., 2007; Cruz et al., 2010; Luzzatto and Shirazi, 2007]. The most representative are the homodyne and heterodyne architectures. Conceptually, the two architectures differs only by the number of stages used to modulate/demodulate the signal. In a heterodyne transceiver, two or more stages are used to modulate/demodulate the signal. A heterodyne transceiver is characterized by high performance with respect to the gain and interferers but has a lower flexibility and scale of integration. On the other hand, in a homodyne transceiver the signal is modulated in one stage. The homodyne architecture supports an IC realization but it is much more prone to non-idealities. In the case of the RX sections, bandpass RX are gaining ground steadily. These architectures are described and compared briefly in the following sections.

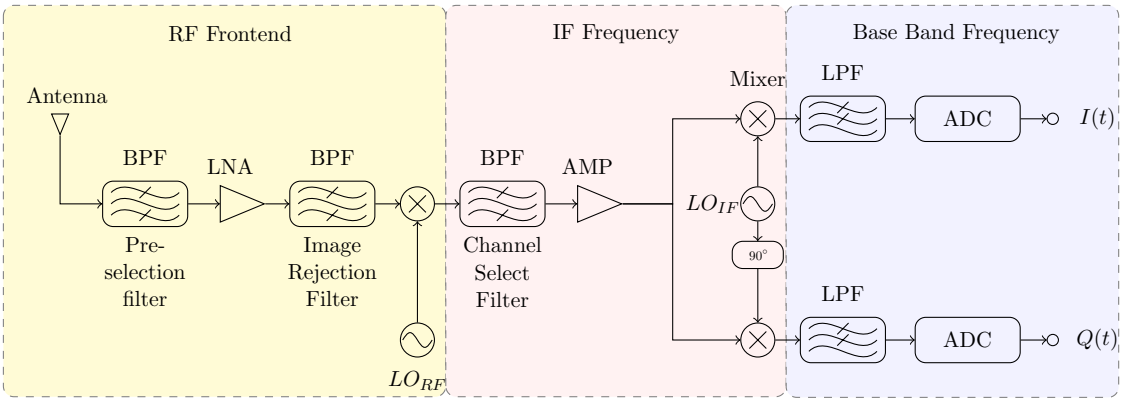


Figure 3.2: Architecture of a heterodyne receiver

3.4.1 Receiver Architectures

The receiver (RX) is a crucially sensitive part in a RF transceiver, making it likely the most challenging to design. The performance of the RX is set by the Signal-to-Noise ratio (SNR) at the input of the ADC. The SNR depends on the chain's gain, filters' performance and will ultimately determine the achievable Bit Error Rate (BER). Other aspects that have to be considered during the design process are: footprint size, production cost, power consumption, multiband capabilities, single-chip integration, etc. Each architecture represents a compromise between these different factors. In the following subsections, the main RX architectures are described.

3.4.1.1 Heterodyne Architecture

The heterodyne (or superheterodyne) architecture is often the best choice for delivering high performance and high gain (>75 dB, which is usually required by military applications). The idea behind the heterodyne RX chain is to amplify the desired RF band by as much as 120 dB, to recover the transmitting channel from noise and interference, through several stages. The first obstacle is to reject adjacent (and unwanted) signals known as blockers, by the use of a band-selection filter close to the antenna. At the output of this stage, there remains only the desired band, contaminated only by wideband noise. The heterodyne architecture is shown in Fig. 3.2. A band-selection filter rejects the out-of-band interferences and lets only in-band RF signals through the amplification stage done by a Low-Noise Amplifier (LNA).

The second down conversion to BB is done by means of two channels, Inphase (I) and quadrature (Q). The split is necessary because it is not possible to detect a general IF signal, simultaneously modulated in both amplitude and phase using a single path. The split IQ quadrature architecture is not mandatory for AM and FM signals. However, the flexibility and the control achievable with IQ channels, makes it desirable for most modern radio. The quadrature architecture is therefore a "de rigueur" for every SDR transceiver.

The advantages and the drawbacks of the heterodyne receiver are summed up in Table 3.1. What it is important to retain is that the heterodyne architecture can provide reliable performance at the expense of the high power, complexity and reduced flexibility.

3.4.1.2 Homodyne Architecture

The main concern of a heterodyne receiver is the management of the image frequencies spaced from the desired frequency by twice the IF. One possible solution is to set the IF to DC and

Table 3.1: Comparison of receiver architectures

Rx Architecture	Advantages	Drawbacks
Superheterodyne	• reliable • flexible frequency plan • able to receive weak signals, since higher gain is available • IF quadrature LO and mixer work at a fixed frequency, making it easier to obtain accurate I/Q balance • immune to DC-offset and 1/f noise	• more expensive (assembly of discrete components) • problems with image frequency rejection • complexity • high power (BjT, SiGe, HEMT stages, etc.) • several local oscillators are required • highly selective IF filters are mandatory, which makes it impractical for single-chip
Zero-IF	• simplicity • low cost • suitable for monolithic (IC) realization • no image frequency issue	• wideband (adjustable), accurately balanced Local Oscillator (LO) is required • wideband low-noise mixer is required • LO leakage in mixer must be minimal • suffers from DC-offset and 1/f noise problems • sensitive to I/Q mismatch
Low-IF	• avoids DC-offset and 1/f noise issues • low cost • well suited for monolithic CMOS implementation	• must deal with image frequency • greater performance requirements on ADCs
Bandpass Sampling	• flexibility • lower cost • simplicity	• requires low-jitter adjustable sampling clock • noise figure degradation • high power consumption • radiates sampling clock out of the antenna

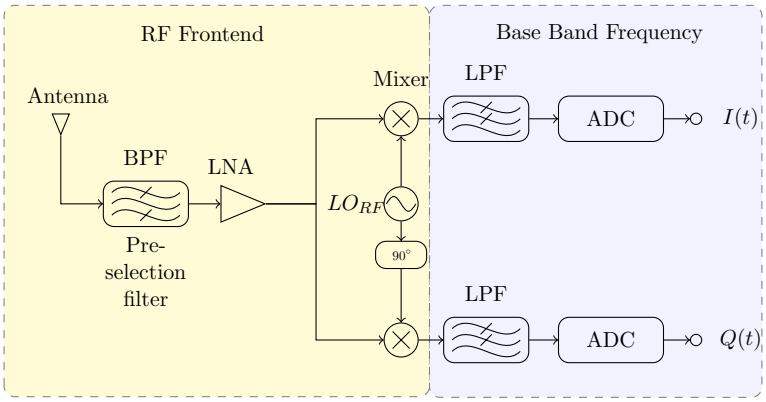


Figure 3.3: Architecture of a Zero-IF receiver

shift the desired channel directly to baseband.

Designed as a simplified version of the heterodyne receiver, the homodyne (or Zero IF) receiver translate the desired signal directly to BB through the I and Q channels (Fig. 3.3). This receiver consists of an LNA which provides modest RF gain at a low noise figure. The output of the mixer is filtered in a bandpass pre-selection filter, and down-converted in a complex IQ mixer. The IQ quadrature architecture is mandatory in the homodyne transmitter, since mixing a general RF signal signal to zero IF frequency with a single-channel architecture would produce non-recoverable aliasing [Schwartz, 1980].

As explained, the homodyne RX doesn't have to worry about image frequency interference, thus no highly selective bandpass filters are needed. It only requires Nyquist-band anti-aliasing LP filters ahead of the ADCs, a much simpler design problem. This makes the homodyne architecture suitable for IC integration. However, a whole new set of issues appear. Because the IF filter is absent, all the shielding from close interferers must come from the I and Q lowpass filters. Furthermore, the mixer needs to operate over a wide frequency band. In comparison, the heterodyne RX works at a fixed frequency.

Nonetheless, because of its flexibility and high level of integrability the homodyne architecture is suitable for applications that aim at multiband operation and can tolerate loss in sensitivity. The advantages and the drawbacks of the homodyne RX receiver are summarized in Table 3.1.

3.4.1.3 Low IF Receiver

A candidate architecture that tries to combine the advantages of the homodyne and heterodyne RX is the low IF RX [Adiseno et al., 2002], in which the RF signal is mixed to nonzero low or moderate IF (few hundreds of KHz to several MHz). Similarly to the homodyne structure, the RF signal is passed through a channel-selection filter and amplified by a LNA (Fig. 3.4). However, after this step, the signal is down-converted to low IF instead of zero IF. An image suppression bank of filters is used in order to cancel the negative effects from the frequency image. Finally, the ADCs convert the low IF signal to digital domain, where digital signal processing algorithms are used. In some low IF architectures the image suppression block is transferred to the digital domain.

The architecture still allows a high level of integration but does not suffer from DC problems, since the signal of interest is not situated around DC anymore. Nonetheless, the low IF architecture still suffers from the image frequency and I/Q mismatch problems. Further more, the ADC power consumption is increased since now a higher conversion rate is required. The

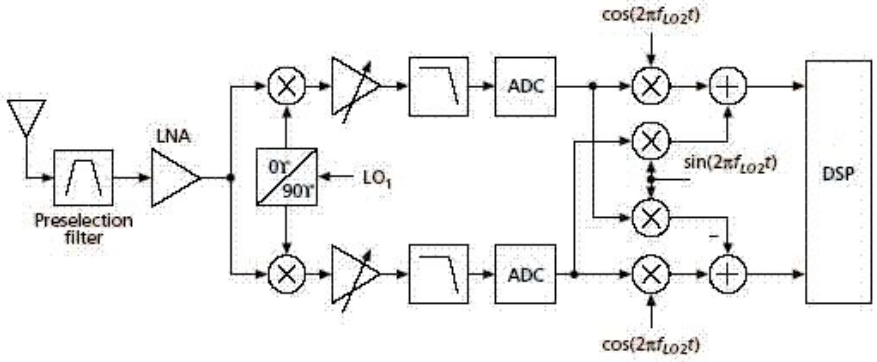


Figure 3.4: Architecture of a low IF receiver

advantages and the drawbacks of the low IF receiver are summarized in Table 3.1.

3.4.1.4 Receiver Architectures. Comparison and Conclusions.

Over the years, several RX architectures have been introduced, and this evolution has been guided by the fabrication technology available, the wireless standards addressed and the markets served. The spectacular gain in speed and level of integration is inexorably pushing the field to newer "digitally-assisted" architectures. Despite this trend, the best performing RX front-ends still fall in three types: heterodyne, homodyne, and low IF. Military radio units place range (i.e. sensitivity) above all else, making the heterodyne architecture the most common choice. Nonetheless, newer products must inter-operate with civilians wireless standard, such as 4G or 5G, so new "hybrid" designs are needed. These forthcoming products will need more sophisticated test strategies, covering all signal paths.

3.4.2 Transmitter Architectures

In comparison with the RX, the transmitter faces lesser obstacles. The design complexity is somewhat reduced by the absence of "unknowns" such as: variable incoming signal power, unknown-power in-band and out-of-band interferences. The design of the transmitter is mainly concerned with getting good power efficiency while minimizing spurious emissions at RF bands around the transmitted signal. This parameter is measured at the antenna port and is expressed by several figures of merit. At system-level, this unwanted emission is commonly quantified in terms of third-order intercept point (IP3) or Adjacent Channel Power Ratio (ACPR). These figures of merit are discussed in the next section.

Similarly to the receiver, the main difference between the main TX architectures is the kind of circuit employed to up-convert the BB signal, homodyne or heterodyne.

3.4.2.1 Heterodyne TX

Conceptually, the heterodyne TX is merely a reverse operation w.r.t. its RX counterpart. The RX ADCs replaced by the TX DACs, and the RX LNA is replaced by the TX Power Amplifier (PA). The signal is created in the digital domain using DACs and then modulated to an IF, where it is amplified and filtered to remove harmonics that were generated during modulation. Finally, the signal is up-converted to RF using an LO, filtered to remove unwanted image sidebands, amplified by an PA and applied to the transmit antenna. The I/Q modulator works

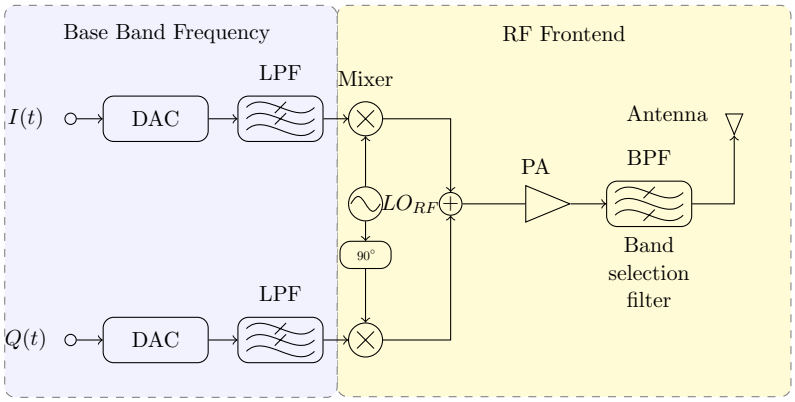


Figure 3.5: Architecture of a homodyne transmitter

at a fixed IF, which means the hardware components are easier to design. Similar to the receiver case, the heterodyne TX has a lot of limitations that limits their usage in SDR applications:

- low integration level
- highly linear PA required
- difficult to implement multimode operation.

3.4.2.2 Homodyne TX

The block diagram of a homodyne TX architecture is depicted in Fig. 3.5. As in the heterodyne TX, two DACs are used to convert the baseband digital I and Q signals to the analog domain. The low pass filters that follow eliminate Nyquist images and improve the noise floor. These signals are then directly modulated at RF by the means of two I/Q modulators. Finally, the signal is amplified by a PA and filtered by an bandpass filter.

Despite some important advantages, such as: reduced amount of circuitry and higher level of integration, the homodyne has also its limitation:

- carrier leakage appears when the signal at the output of the PA couples with local RX oscillator that runs at the same RF frequency (oscillator pulling). As the result the frequency of the LO signal may drift from the desired value.
- prone to I/Q mismatches
- a linear PA is required

Nonetheless, with careful design, the homodyne TX can be used in SDR applications.

Table 3.2 provides a detailed comparison between the two TX architectures listing their advantages and disadvantages. For much the same reasons as in the RX, the heterodyne TX gives the best performance at the cost of a bulkier (and power hungry) implementation, while the homodyne architecture offers greater flexibility, lower cost, more compact implementation and outputs a less clean signal.

3.4.3 State-of-Art SDR Transceiver Architectures

In the previous section, we presented some traditional RF transceiver architectures. These architectures are very well suited for standard RF applications and are optimized for only

Table 3.2: Comparison between the most common transmitter architectures

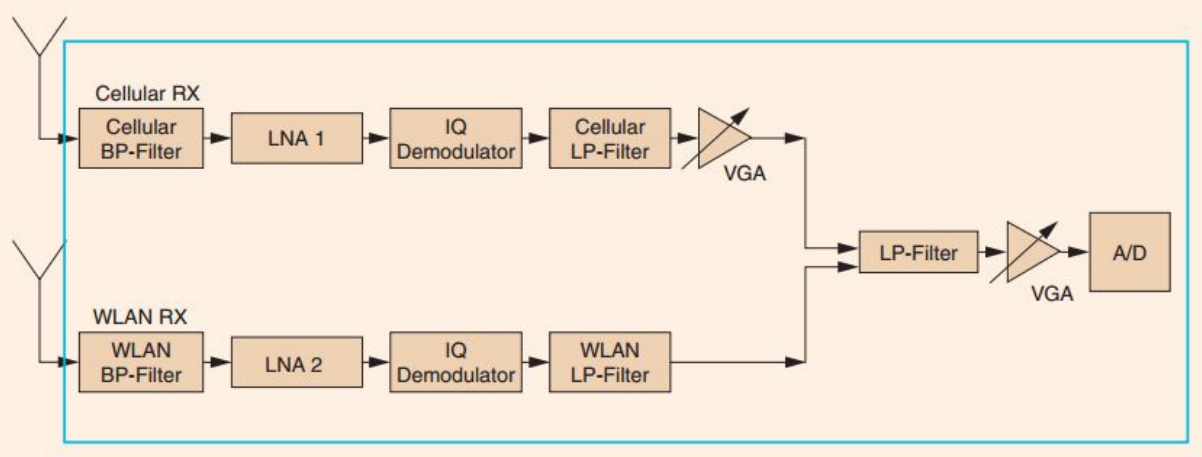
TX Architecture	Advantages	Disadvantages
Heterodyne	• reliable performances • flexible frequency plan • no LO leakage • DC offset cancellation in BB	• expensive • high power
Homodyne	• simplicity • low cost • no image problem • high integrability	• DC offset problem • LO leakage • oscillator pulling

one standard. Nonetheless, for SDR and multistandard terminals, these architectures cannot guarantee the required flexibility and performance. New architectures have to be proposed to satisfy these requirements. To address these challenges, new SDR architectures have been discussed in literature. In the following, we will present some of the most promising solutions that are paving the way to a fully reconfigurable SDR terminal.

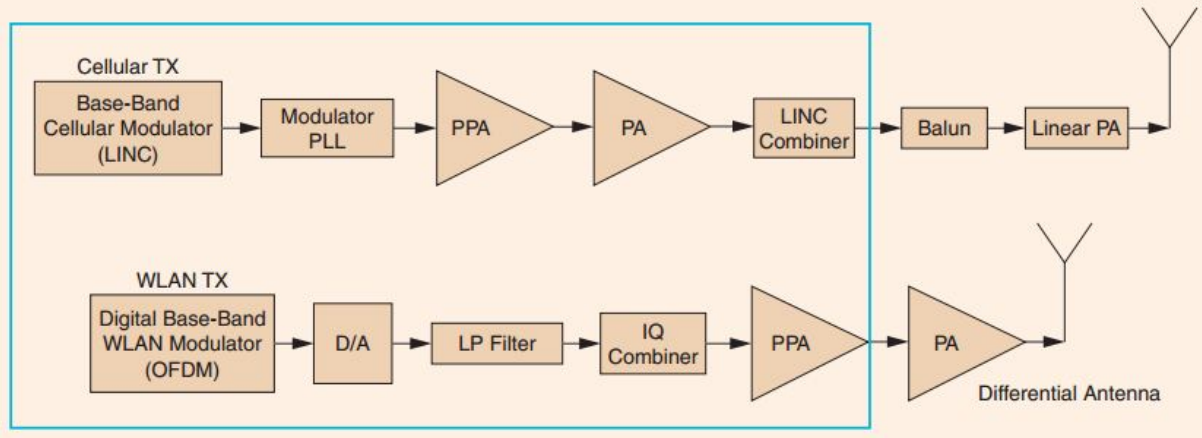
3.4.3.1 Multistandard Transceivers

A possible approach to ensure multistandard functionality is to employ parallel analog chains where every chain relies on traditional architectures. Of course this is not the ideal solution, but this approach has the advantage that several standards can operate concurrently. Such an implementation is given in Agnelli et al. [2006], where it is presented a fully integrating solution that covers four major communication standard families: GSM, WCDMA, Bluetooth and wireless LANs. The proposed solution consists of two chips, one including the TX and the other the RX for all the above standards. Each of the TX and RX integrates two parallel chains, one supporting all cellular standards plus Bluetooth and the other one supporting all WLAN standards plus Bluetooth. The diagram of the multistandard terminal is given in Fig. 3.6. The key point is silicon area minimization through maximum hardware sharing. We notice that the baseband blocks are shared among all standards, thanks to their high reconfigurability. The overall TX architecture is based on a zero-IF down conversion for UMTS and wireless LANs, and on a low-IF one for GSM. The cellular RX architecture is able to reconfigure between low-IF for GSM and direct conversion for UMTS and Bluetooth.

The study presented in Agnelli et al. [2006] describes some details of circuit implementation and proves that a multistandard terminal can be designed if several traditional architectures are combined together. From the point of view of test, it is important to note that the test strategy has to cover every analog/RF chain in the TX/RX path.



(a) Homodyne multistandard receiver architecture



(b) Homodyne multistandard transmitter architecture

Figure 3.6: Architecture of a multistandard terminal as proposed by Agnelli et al. [2006]

3.4.3.2 Noise-Canceling Receiver Architecture

The previous solution does not address the requirements of a fully reconfigurable SDR transceiver. The architecture provides a multistandard terminal, but it still relies on classic homodyne architecture and it makes use of RF filtering to prevent large out-of-band filters corrupting the wanted signal. The problem with RF filters is that they are almost always fixed, thus multiple frontends are required to cover a large number of frequency bands (as we saw in the previous approach). A first step to a fully configurable SDR architecture would be indeed to eliminate RF filtering.

Without fixed RF filtering, a single wideband receiver that is tunable over the entire spectrum of interest could be employed. Nonetheless, eliminating RF filtering can be challenging for several reasons. First, because the out-of-band blockers are not suppressed anymore, the LNA will amplify both the desired wanted signal and the blockers. Thus, a large blocker will cause the LNA to clip resulting in increased distortion and noise in the receiver. Secondly, since passive filtering has been ruled out, any blocker present will be downconverted along with the wanted signal. When the blocker mixes with the LO phase noise, it deposits additive noise in the receive channel proportional to the blocker amplitude.

The previous two remarks imply that a blocker-tolerant wideband receiver must avoid voltage gain at blocker frequencies and should generate LO signals with very low phase noise. A recent architecture that attempts to implement such a wideband receiver relies on noise canceling technique, which was first proposed in Klumperink [1991]; Bruccoleri et al. [2001]. After that, the noise-canceling architecture has been intensely studied, and several variations have been proposed and discussed [Borremans et al., 2011; Ru et al., 2009; Murphy et al., 2012]. The basic idea of the noise-canceling design is the following. First, it has been shown that the matching resistor noise can be nulled in an LNA by measuring the voltage at the RF node and the current flowing through the matching resistor [Borremans et al., 2011]. Then, a design that uses two separate passive-mixer-based downconversion paths is employed for frequency-translation of the RF signal [Murphy et al., 2012]. The new design tolerates large blockers by avoiding voltage gain at blocker frequencies. The architecture of a blocker-tolerant, noise canceling receiver has been introduced in Murphy et al. [2012]. The resulting prototype is functional from 80 MHz to 2.7 GHz and achieves a 2 dB noise figure and acts, thus as a fully reconfigurable SDR receiver.

3.4.3.3 Subsampling (Bandpass) Receivers

Every RX architecture previously presented relies on analog mixers to downconvert the RF signal to baseband. The mixers are driven by LOs that operate at RF frequency, thus the power consumption is not negligible. Moreover, for an SDR receiver that has to operate over a wide frequency range, a variable LO is required (such wide dynamics LOs and mixers that also perform well are difficult to design). In order to minimize the power consumption of the SDR RXs and to improve their reconfigurability, a new class of wideband receivers has been introduced. These receivers are known as undersampling receivers (or subsampling, or bandpass, or direct sampling receivers), and they rely on the undersampling technique [Barrak et al., 2009; Vaughan et al., 1991] and digital aliasing to downconvert the RF signal. The theory of undersampling is described in greater details in the next chapter as it will be used by our test strategy. Here, we present shortly the bandpass receiver architecture.

In this architecture (Fig. 3.7), the RF frontend, consisting of a bandpass filter followed by an LNA, supplies the signal directly to the ADC. The idea behind this approach is that a sparse spectrum does not need to be sampled at the Nyquist rate to be properly acquired. This configuration is based on the fact that all energy from DC to the input analog bandwidth will

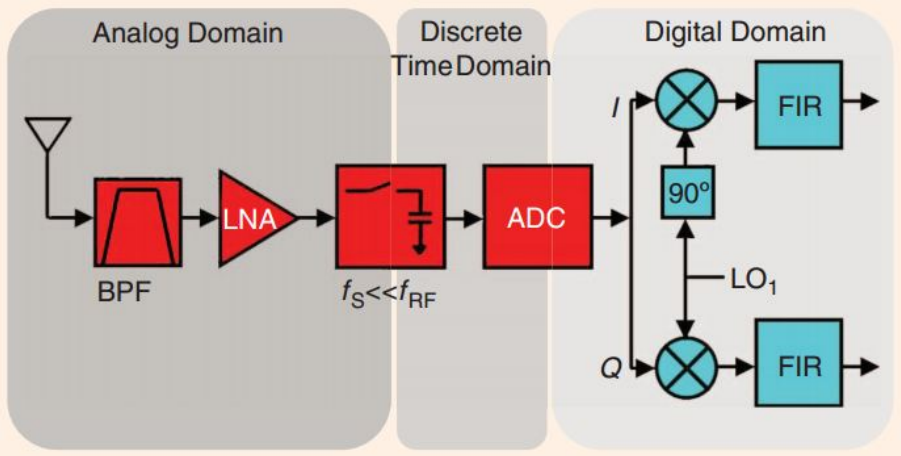


Figure 3.7: Architecture of a bandpass sampling receiver [Cruz et al., 2010]

be folded back to the Nyquist zone without any mixing down needed.

For this architecture, the bandpass filter plays an important role because it reduces all signal energy outside the band of interest. If not filtered, this energy is folded back to the first Nyquist zone together with the desired signal, producing a degradation of the SNR.

The advantage of the bandpass RX is that the sampling frequency needed is proportional to the signal bandwidth and not the carrier frequency, thus the number of components being reduced. The undersampling receiver is the closest architecture to the ideal SDR frontend proposed by Mitola. Nonetheless, some inherent limitations exist. First, the analog input bandwidth of the existing S/H stage of the ADC must cover the RF signal we want to monitor, which is a serious problem considering the performance of modern ADCs. Further more, the bandpass sampling technique is known to be sensitive to the phase noise of the sampling clock. Special attention has to be paid to the design of the sampling clock.

However, the bandpass receiver is a promising architecture, and a lot of efforts have been carried out, first, to analyze and define the requirements, and secondly, to surpass the limitations and meet these requirements.

The study presented in Rodriguez-Parera et al. [2007] provides an analysis of the ADC requirements for a bandpass sampling receiver. They use two different models, one based on cascade analysis and the other one on time-domain simulations, to derive the ADC requirements: sampling frequency, resolution and clock jitter. Their study shows that RF bandpass sampling has the potential of becoming a reality for low-power terminals. A similar analysis was presented in Kim et al. [2010]. Experimental results obtained in their research showed that only three degradation sources: clock jitter, ADC resolution and folding noise are sufficient to estimate the performance of an RF subsampling architecture.

As discussed before, the jitter is an important degrading factor in a bandpass receiver. To reduce the jitter introduced noise, a clock generator with low-jitter is needed. However, a low-jitter clock is not always available. As a result, several methods to mitigate the jitter introduced noise have been proposed. Nonetheless, the dejittering of a received signals is computationally expensive, especially for wideband communications signals, since the induced jitter on received signals varies as a function of RF signal frequency.

To overcome this limitation, a jitter compensation technique is introduced in Zhao et al. [2012]. The proposed architecture uses a reference signal that is injected into a secondary path which is subsequently sampled by the same sampling clock. In this way, since the sampling clocks for the two sampling branches are the same, the jitter information can still be estimated

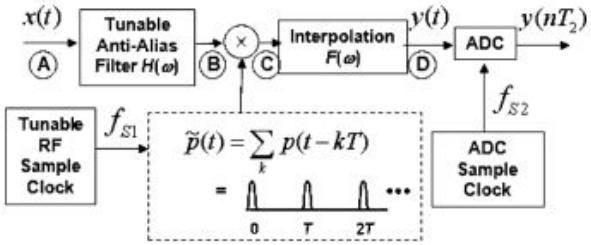


Figure 3.8: Two-stages bandpass receiver [Fudge et al., 2013]

from the reference without interfering with the wanted signals.

Also addressing the jitter sensitivity, the authors in Fudge et al. [2013] proposed a two-stages undersampling RX that has a stair-step jitter pattern as a function of RF signal frequency. In the first stage, the RF input is bandpass filtered and pulse sampled without quantizing the signal. The discrete-time analog signal is then interpolated with a continuous time lowpass filter, then sampled and quantized by a traditional ADC (Fig. 3.8). With this two-stage sampling circuit, the induced signal jitter from the RF sampling is identical for all in-band signals and is the same to within an integer scale factor for all signals, in-band or out-of-band. This key circuit property means that it is possible to remove jitter with low computational complexity. The proposed architecture is suitable for SDR applications.

Another approach to mitigate the noise in bandpass receiver consists on rethinking the sampler block. Indeed, it has been shown that, if the classic Sample&Hold stage is replaced by a charge integrating sampler the subsampling robustness w.r.t. jitter is greatly improved [Yuan, 2000; Carley and Mukherjee, 1995; Poberezhskiy and Poberezhskiy, 2007]. Furthermore, the proposed improvement has a simpler hardware implementation and it's more flexible. The charged-based sampling technique is discussed in more details in Chapter 6.

Employing charge-based sampling, several SDR RX architectures have been successfully reported. The study presented in Poberezhskiy and Poberezhskiy [2005] discusses a new heterodyne architecture in which the conversion from IF to BB is done using charge-based sampling. Multiple advantages of this approach are discussed. First of all, the charge-based samplers provide internal filtering, which allows removal of conventional antialiasing and reconstruction filters or their replacement by wideband filters realizable on a chip. Furthermore, the effect of jitter is minimized. To sum up, the use of charge-based sampling in SDRs radically increases reconfigurability, adaptivity and scale of integration of their frontends.

The previous approach still relies on a large AMS section, the first stage consisting of an analog mixer. The motivation is that for military applications a large gain is required in order to avoid jamming and this gain cannot be achieved in one stage. Nonetheless, for commercial wireless systems where the gain requirements can be relaxed, direct bandpass receivers have been proposed. Such a receivers is described and implemented in Chen and Hashemi [2014]. The proposed architecture leverages charge-based sampling and switched capacitor techniques at radio frequencies, thus providing a 0.5-3 GHz flexible SDR receiver.

Considerations and other successful implementations of a true SDR receiver based on charge-based bandpass sampling are reported in Chen et al. [2007]; Ru et al. [2010]; Staszewski et al. [2004]; Ru et al. [2010].

3.4.3.4 Conclusions

To sum up this section, several efforts have been made to design a fully reconfigurable SDR transceiver. Some architectures resulted from continuous improvement of the more traditional architectures (e.g. multistandard transceivers) while others have been invented from scratch (e.g. bandpass receivers). Amongst these new designs, the bandpass receivers seem to be the most promising architecture for RX SDR.

3.5 Transceiver Specifications

Given the large variety of RF transceiver architectures, it is essential to define Figures of Merit (FoM) that can be universally applied, independent of the architecture. For traditional all-analog narrowband transceivers these FoMs consisted of parameters like gain compression or intermodulation distortion that are measured with simple input signals, e.g. tones or multi-tones.

On the other hand, the more modern digital transceivers are ultimately judged on Bit Error Rates (BER) over signal to noise power for a given wireless standard. In addition, resiliency to nearby interferences (blockers), and clean transmission are the only specifications the end-users care about. These properties result from many factors, which make them unsuitable for guiding the design and diagnosis of problems. For modern architectures, it's hardly feasible to continue measuring simple parametrics and then try to correlate these characteristics to ultimate system performance for all possible waveforms, protocols and modes of operation. Issues such as gain, noise figure, third-order intercept point remain useful designer metrics, but what really counts in the field is that the radio functions reliably and complies to the standards.

This section presents a brief overview of FoMs commonly used for transceiver characterization. These FoMs can be categorized as:

1. Basic tests like:
    - Scattering parameters (S-parameters)
    - Frequency and gain measurements
    - Power and power efficiency measurements
2. Distortion measurements
3. Noise measurements
4. Digital figures of merit

In the following subsections the definitions of these specifications are listed accompanied by some sketches showing how this measurements are actually carried out.

3.5.1 Small-signal FoMs

The most common small-signal FoMs for RF blocks are the scattering parameters. In short, they express how much power is absorbed, reflected and transmitted as a function of frequency and they are measured in strictly linear conditions.

S-parameters are widely used during the design because they allow one to quickly compare and select components for an RF system, looking at each one as a black box. Nonetheless, they are less useful for test as they are difficult to measure and do not provide vital information about the DUT, outside the linear region.

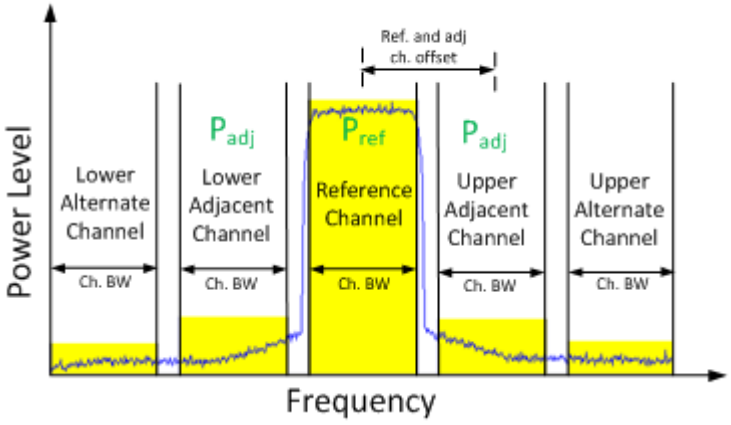


Figure 3.9: ACPR Definition

3.5.2 Signal Power FoMs

From the power point of view of the receiver side, a radio device is characterized by: minimum detectable RF power, maximum allowed input power and power level of interfering tones (at a given offset from the channel). Dynamic Range (DR) is defined as ratio of the maximum input level that the circuit can tolerate to the minimum input level at which the circuit provide a reasonable signal quality.

The transmitter side is defined by: maximum RF power output, RF power distribution over a frequency band, power-added efficiency (PAE) and Adjacent Channel Power Ratio (ACPR). Power-added efficiency of an RF amplifier is the ratio of RF power generated by the amplifier to the DC power supplied:

$$PAE = \frac{P_{RF_{out}} - P_{RF_{in}}}{P_{DC}} \tag{3.1}$$

and is a measure of heat generated in the amplifier, i.e., the battery power that is wasted.

For the RF TX the ACPR (Adjacent Channel Power Ratio) is one of the most important system-level figures of merit. It measures the amount of distortion generated by transmitter in the adjacent-frequency channel relative to the power in the main channel. It quantifies the effect of nonlinear distortions and is commonly specified for every digital transmission standard. It is usually defined as the ratio of the average power in the adjacent frequency channel to the average power in the transmitted frequency channel (Fig. 3.9) or:

$$ACPR\ [\text{dBc}] \ = 10 \log_{10} \left(\frac{P_{adj}}{P_{ref}} \right) \tag{3.2}$$

Our proposed test architecture aims to measure TX ACPR.

3.5.3 Distortion FoMs

Every electronic circuit exhibits some non-linearity, and should ultimately be modeled by a non-linear function. Non-linearity generates unwanted changes (distortion) in the signal shape. As an example, let us consider a memoryless time-invariant system defined by the following nonlinear third-order polynomial transfer function:

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{3.3}$$

where $y(t)$ is output signal, $x(t)$ the input signal, α_1 the small-signal gain and α_2, α_3 are non-linearity coefficients. This is a common generic model for communication circuit blocks.

3.5.3.1 Single-Tone FoMs

If a single-tone sinusoid $x(t) = A\cos(\omega t)$ is applied to the system defined by 3.3, the output will exhibit frequency components that are integer multiple of the input frequency:

$$\begin{aligned} y(t) \quad = \quad & \frac{\alpha_2 A^2}{2} \\ & + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos(\omega t) \\ & + \frac{\alpha_2 A^2}{2}\cos(2\omega t) \\ & + \frac{\alpha_3 A^3}{4}\cos(3\omega t) \end{aligned} \tag{3.4}$$

In the previous equation, the term with the input frequency ($\left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos(\omega t)$) is called 'the fundamental' and the higher-orders terms 'harmonics'. The propagation of the harmonics are a waste of power and obscure the useful signals. These effects are quantified by:

- Total Harmonic Distortion (THD) = the total power contained in all harmonics of a signal expressed as percentage of the fundamental signal power. It's usually enough to sum up to the 7th or 9th harmonic

  $$\text{THD}[\%] = \frac{P_2 + P_3 + \dots}{P_{fundamental}} \cdot 100$$

  where P_i is the power in watts of i^{th} harmonic and $P_{fundamental}$ is the fundamental signal power

- SIgnal to Noise And Distortion (SINAD) is defined as the ratio of the total power of the signal to the power of the noise and the distortion component:

  $$\text{SINAD} = \frac{P_{signal} + P_{noise} + P_{distortion}}{P_{noise} + P_{distortion}} \tag{3.5}$$

THD and SINAD are useful FoMs throughout the linear signal path of a transceiver. They are often given for a signal power close to the specified DR, or the DR is set w.r.t. to the maximum acceptable SINAD/THD. In the case of the output, the PA stage, the FoM used, called gain compression, is somewhat different.

Gain Compression Let us analyze the fundamental term in expression 3.4. If $A << \alpha_1$, the output follow a linear trajectory with a small gain of α_1. As input power increases, so does non-linearity and the amplifier gain is reduced. This phenomenon is known as gain compression. A standard measure of gain compression is 1dB compression point ($P_{1\text{dB}}$) defined as input/output signal level that causes the small-signal gain to drop by 1 dB (Fig. 3.10)

Fig. 3.11 shows two examples of non-linear distortion, to clarify gain compression. As long as the signal remains within the nominal operation range of the circuit, the output is a linear version of the input. Once the signal exceeds this range the output undergoes clipping and harmonics appear.

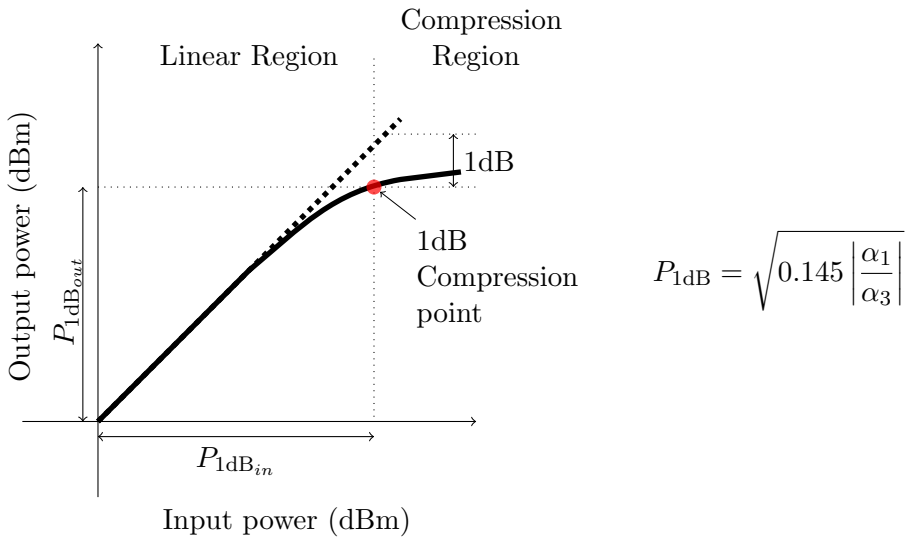


Figure 3.10: Definition of the 1 dB compression point

Gain compression is a form of distortion specification that is defined in terms of power reduction, and not harmonic content.

Evaluating this FoM requires signal sweeping and extrapolation. The following algorithm allows testing for gain compression.

1. Apply a single-tone input signal
2. Measure the gain at a power level where DUT is linear
3. Extrapolate the linear behavior to higher power levels
4. Increase input power in steps, measure the gain and compare to extrapolated values
5. Test is complete when the gain difference between steps 2 and 3 is 1dB

A faster way to test is to do a binary search for the red point (1 dB compression point) after step 2 or 4.

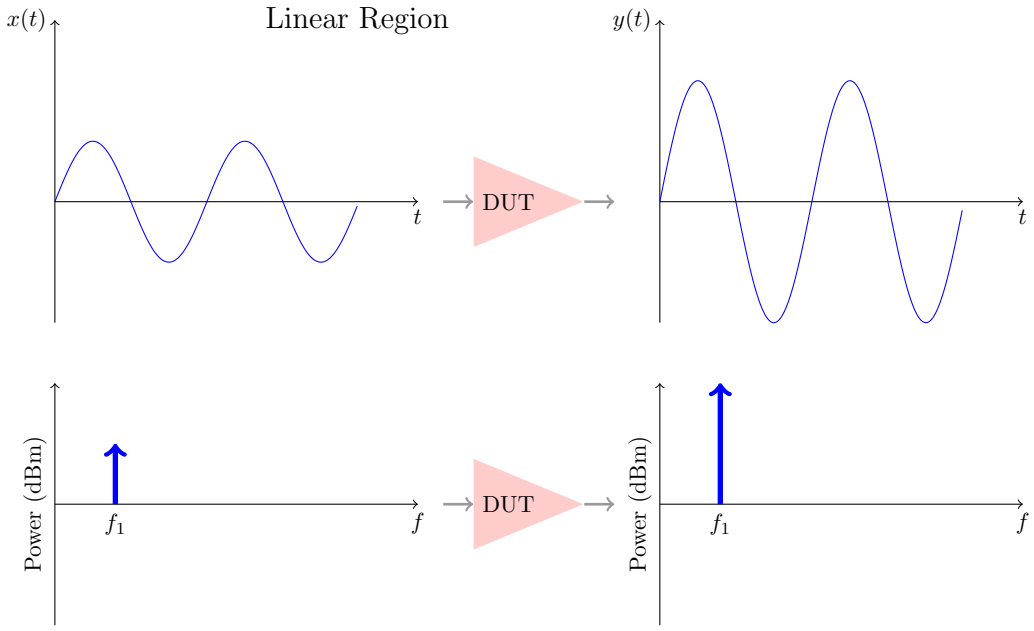
3.5.3.2 Multi-tone FoMs

When two signals with different frequencies are applied to a non-linear system, the output exhibits some components that are not harmonics of the input frequencies. To understand the phenomenon of intermodulation (IM) let us consider in 3.3 $x(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)$. The output will contain the following intermodulation terms:

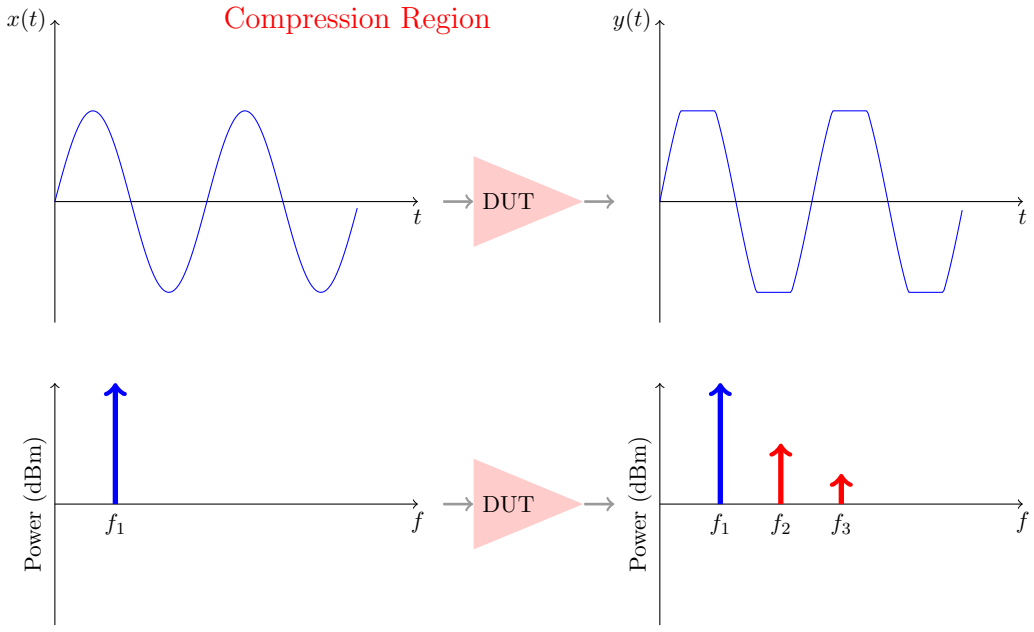
$$\begin{aligned} \omega \quad = \quad \omega_1 \pm \omega_2 \quad &: \quad \alpha_2 A_1 A_2 \cos(\omega_1 + \omega_2)t + \alpha_2 A_1 A_2 \cos(\omega_1 - \omega_2)t \\ 2\omega_1 \pm \omega_2 \quad &: \quad \frac{3\alpha_3 A_1^2 A_2}{4} \cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 A_1^2 A_2}{4} \cos(2\omega_1 - \omega_2)t \\ 2\omega_2 \pm \omega_1 \quad &: \quad \frac{3\alpha_3 A_2^2 A_1}{4} \cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 A_2^2 A_1}{4} \cos(2\omega_2 - \omega_1)t \end{aligned} \tag{3.6}$$

and these fundamental harmonics

$$\begin{aligned} \omega \quad = \quad \omega_1 \quad &: \quad (\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1^3 + \frac{3}{2}\alpha_3 A_1 A_2^2) \cos \omega_1 t \\ \omega_2 \quad &: \quad (\alpha_1 A_2 + \frac{3}{4}\alpha_3 A_2^3 + \frac{3}{2}\alpha_3 A_2 A_1^2) \cos \omega_2 t \end{aligned} \tag{3.7}$$



(a) Linear Behavior



(b) Nonlinear Behavior

Figure 3.11: Visualizing the effects of non-linearity.

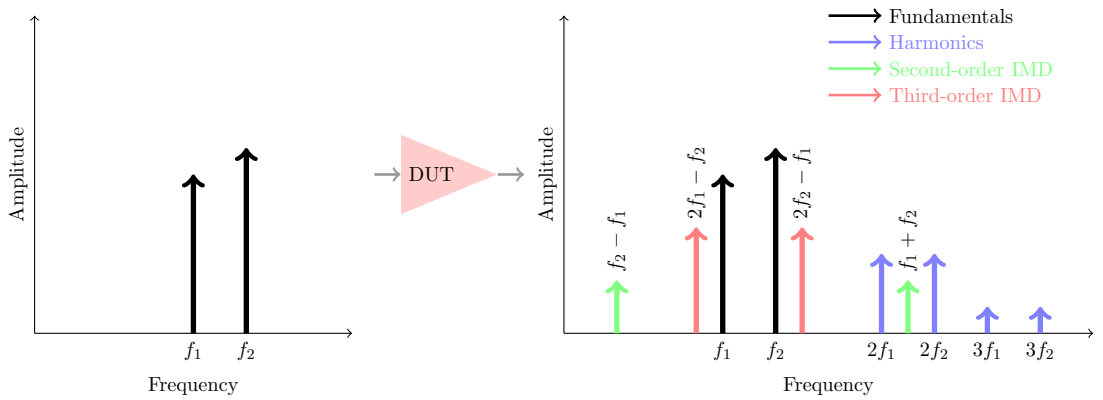


Figure 3.12: Intermodulation distortion - Graphical representation

In differential circuits, even-order products are inherently suppressed. Thus, of particular interest are the third-order IM products (IMD3) at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ as illustrated in Fig. 3.12. The key point here is that if the difference between ω_1 and ω_2 is small, the components $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ will be in vicinity of ω_1 and ω_2 and will overshadow the signal of interest.

The third-order intercept point (IP3) is a figure of merit that quantifies IMD3 and is defined as *the power level of the fundamental for which the output of each fundamental frequency equals the output of the closest third-order intermodulation frequency.* In a typical IMD test, $A_1 = A_2 = A$. Therefore, the output of each fundamental frequency, f_1 and f_2 is $\alpha_1 A + \frac{9}{4}\alpha_3 A^3$ and the output amplitude of each IM3 frequency will be $\frac{3}{4}\alpha_3 A^3$. Assuming that $\alpha_1 >> \frac{9}{4}\alpha_3 A^2$, IP3 can be calculated as:

$$\text{IP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{3.8}$$

The following algorithm is employed for IP3 testing:

1. Select 2 test frequencies, f_1 and f_2 of magnitude A and apply them to the input of DUT
2. Increase input power P_{in}[dBm] until the third-order products are well above the noise floor
3. Measure output power P_{out}[dBm] at each fundamental frequency and power at a third-order IM frequency P_3
4. Find output-referenced IP3: $\text{OIP3} = P_{out} + \frac{P_{out} - P_3}{2}$
5. Find input-referenced IP3: $\text{IIP3} = P_{in} + \frac{P_{out} - P_3}{2}$

A graphical representation of the IP3 calculation is depicted in Fig. 3.13

Conclusions The distortion FoMs discussed in this subsection are very well suited for narrowband transceivers. However, as the channel bandwidth of modern transceivers grows larger and larger, the wideband and time-variant effect cannot be neglected anymore. Thus the memoryless model presented in Eq. 3.3 is becoming insufficient.

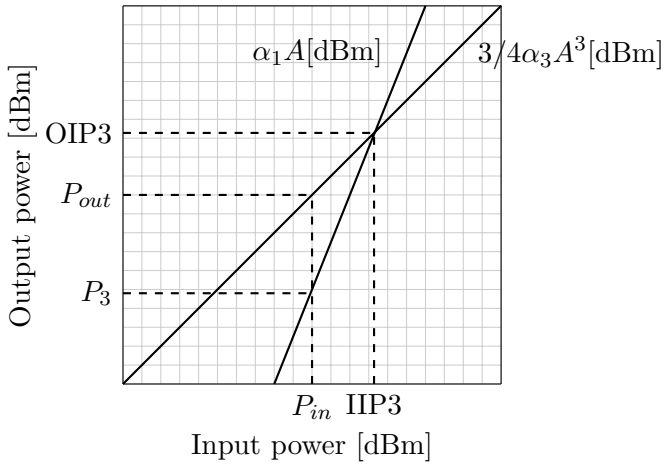


Figure 3.13: IP3 - Graphical representation

3.5.4 Noise Specifications

Noise is a natural unavoidable phenomenon, unlike interference. In RF systems, wideband (white) noise is often a concern as it is a very important limiting factor and it affects the dynamic range of circuit.

The main contributions of noise in an electronic circuit are resistors and semiconductor junctions. The noise power of a resistor obeys the following expression:

$$N = kTB[\text{W/Hz}] \tag{3.9}$$

where $k = 1.38 \cdot 10^{-23}$J/K is Boltzmann constant, T is absolute temperature in Kelvin and B is the circuit bandwidth. At $T_0 = 290$K, $kT_0 = -174$dBm/Hz. The thermal (or Johnson) noise is ubiquitous, and can only be reduced by band limiting (filtering). Semiconductor junctions have shot noise. MOS transistors exhibit another forms of noise, pink noise, usually disregarded at RF frequencies since it falls off steeply with frequency.

It is not straightforward to extract the noise characteristics of a circuit. Several figures of merit are used to describe the noise in an electrical circuit:

- Signal-to-Noise Ratio (SNR) is ratio of signal power to noise power
- Noise Factor (F) is the ratio of output SNR to input SNR

$$\begin{aligned} F &= \frac{SNR_{out}}{SNR_{in}} = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} \\ &= \frac{N_{out}}{GN_{in}} && \text{where } G \text{ is the DUT gain} \\ &= \frac{N_{out}}{kT_0BG} && \text{where } N_{in} = kT_0B \text{ is the input noise source} \end{aligned} \tag{3.10}$$

- Noise Figure (NF) is noise factor expressed in dB:

$$\begin{aligned} \text{NF} &= 10\log \text{F} \\ &= N_{out}[\text{dB}] - (-174[\text{dBm/Hz}]) - B[\text{dB}] - G[\text{dB}] \end{aligned} \tag{3.11}$$

As one can observe in Eq. 3.11 the NF can be determined by measuring the output power, the bandwidth and the gain of the DUT. This method is called 'Cold noise method'. A more practical method usually used in industrial applications is called Y-factor method and is presented in Wolf et al. [2006].

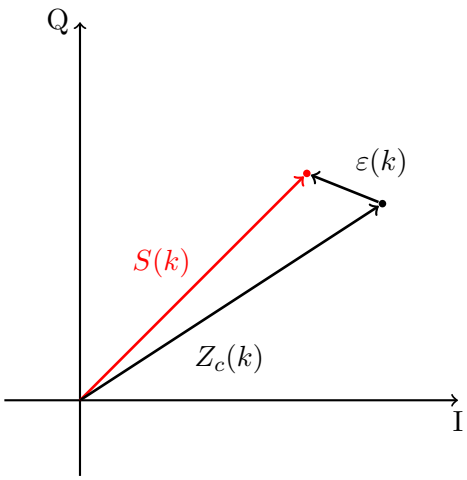


Figure 3.14: EVM definition. $S(k)$ represents the ideal location of the k^{th} constellation point, $Z_c(k)$ the real location and $\varepsilon(k)$ represent the error vector

Remarks Because it affects the dynamic range of the circuit, the Noise Figure must be considered during the test phase. For test purposes, the NF can be estimated by looking at other FoMs directly related and affected by the noise, e.g. BER, EVM.

3.5.5 Digital FoMs

The recent development of the digital modulation techniques has determined the introduction of new figures of merit capable to assess the overall performance of a digitally based radio system. Ultimately, the RF transceivers are judged on these FoMs, because they define the quality perceived by users.

One such common technique is the Bit Error Rate (BER) which represents the ratio of the number of erroneous data bits receiver to the total number of data bits transmitted. The BER test is rather limited because it does not provide much information on the sources of errors. In addition, it's difficult to asses realistically by simulating the complete system because it requires long streams of symbols to be encoded and decoded, an extremely time-consuming operation to compute when added noise must be considered.

To mitigate this problem, one usually evaluates another FoM, the Error Vector Magnitude (EVM). EVM is a measure of modulation and demodulation accuracy as well as channel impairments. A signal sent by a transmitter or received by a receiver will suffer from various imperfections that will cause the k modulated signal constellation points, $Z_c(k)$, to deviate from their ideal locations, $S(k)$ (see Fig. 3.14).

$$\text{EVM} = \sqrt{\frac{\frac{1}{N}\sum_{k=1}^{N}|Z_c(k) - S(k)|^2}{P_{avg}}} \cdot 100 \tag{3.12}$$

where P_{avg} is the value for average constellation power.

Fig. 3.15 shows the constellation diagram of a 16 QAM signal where two levels of noise power have been considered. One can easily notice the scattering effect in Fig. 3.15b which is caused by the noisy signal. The example in Fig. 3.15 underlines one of the most important reasons for which EVM preferred to BER: it provides information on the source of errors. In this case is a very noisy circuit, but other important defects can be diagnosed by looking at the diagram constellation: I/Q mismatch, third order non-linearity, etc.

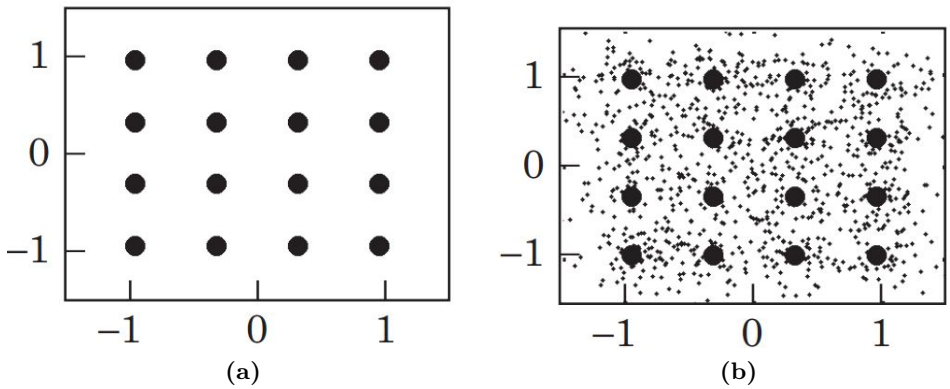


Figure 3.15: Constellation diagram of a 16QAM signal. Two levels of noise power have been considered.

3.5.6 Final Remarks on FoMs for RF Transceivers

In this section, we discussed the most common figures of merit employed to characterize/test an RF circuit. The complexity of the RF transceivers is reflected by the multitude of figures of merit needed to be measured. This means that a test strategy has to validate the DUT for every one of these specifications. This is even more complicated, if we consider that each specification requires different test set-ups and different measurements. In the next chapter we will discuss, how this limitations are addressed by the test community.

3.6 Conclusions

This chapter described the RX and TX architectures commonly used for SDR transceivers. Their relative merits were discussed, to bring to light the reasoning behind the choices taken in the design of tactical radio units. Afterwards, we gave an overview of figures of merit commonly used to evaluate RF systems and circuits. The purpose of the description is to put in context the test strategies described in the next chapter. An extensive and detailed description of the topic can be found in Razavi [1998]; McClaning [2012]

Chapter 4

RF Testing

Contents

In the previous chapter we described the underlying technology and common metrics of SDR transceivers. We saw that SDR development aims for increased speed and flexibility. Multi-mode wideband SDRs attempt to overcome harsh conditions and spectrum scarcity by dynamic sensing and adaptation to the environment. The advent of these system-level requirements on the physical layer (PHY) access hardware is leading to more complex receiver and transmitter architectures, which together with higher levels of integration pose a challenging problem for product testing.

In this chapter we discuss state of the art test strategies for RF systems. First, we introduce some generalities of electronic testing. Then we describe the challenges of AMS/RF testing and more important how these challenges are faced nowadays by the research community and industry. Finally, the most promising AMS/RF test strategies are introduced and analyzed.

4.1 Test & Testability of Electronic Systems

Before one can talk about testing, it is necessary to define the meaning of the term for us. Testing an electronic system is checking for the presence of failure mechanisms that can cause the system to deviate from its correct behavior [Bennetts, 1981]. Let's distinguish between the

terms: *error* and *fault*. An *error* is said to have occurred if the the system deviates from its specified behavior. An error is invariably caused by a *fault*, which is a hardware failure within the system. The difference between the two terms should be clear. A fault may or may not cause an error. However, the presence of an error implies the existence of some fault. In other words, the test of an electronic can defined as the process of detecting and locating errors. Diagnosis is the process of identifying and locating faults. The physical mechanisms (defects) behind the faults are often of little interest for test and diagnosis, so faults are assigned to classes of a given fault model. A fault model typically classifies defects w.r.t. a limited (but meaningful) set of observable behaviors. An example is the stuck-at-1, stuck-at-0, fault models for digital circuits.

One should note that a test strategy is never perfect. This means that there is a finite chance of faulty devices being passed as fault-free or the inverse, fault-free devices being rejected as faulty. To qualify the performance of a test strategy two figures of merit are commonly used: yield loss (YL) and fault coverage (FC) . YL and FC can be defined as follows:

$$\begin{aligned} \text{YL} &= \frac{\text{number of healthy circuits that fail the test}}{\text{number of good circuits}} \\ \text{FC} &= 1 - \frac{\text{number of faulty circuits that pass the test}}{\text{number of faulty circuits}} \end{aligned} \tag{4.1}$$

The fundamental aim of all test methodologies is to obtain the largest possible FC while minimizing YL. From an economical point of view, an interesting FoM is defined by the number of test escapes which is number of faulty devices that pass the test plus the number of healthy devices that fail the test.

4.1.1 Test Classification

Test strategies can be assigned to categories into several ways. For example, depending on the phase when the test is realized during its lifetime, the test can be classified as: design test (known as verification), manufacturing test and in-field test. Testing can and should be realized during each of these different stages of the product lifetime: design, production and operation. It is important to detect and locate the problems at each step of development, before the product reaches the next phase. If not, the fault will cascade to the next phase and it will become more difficult/costly to find and diagnose it.

During design phase, dominant error source includes misinterpretation of specifications and inaccurate translation of specifications into formal specifications. The process of looking for the errors in this step is usually known as verification. During the production phase, errors can occur due to malfunctioning in the manufacturing process. This step is known as manufacturing test. Finally, some errors can appear during normal operation of the system. In order to find, and, eventually correct them, an in-field (standalone) test strategies must be considered. For the majority of large scale manufactured communication products, in-field is not required as it is difficult and costly to implement reliably. Nonetheless, for critical systems such tactical platforms, in-field strategies are a mandatory requirement. Our research targets self-test manufacturing and in-field test.

Testing can also be split into go/no-go testing or diagnostic test. In go/no-go testing the Device Under Test (DUT) is checked for errors. If no errors are found, the device is shipped to the consumer. Otherwise, the device is thrown away and no information about the source of error is provided.

Compared to go/no-go test, the diagnostic test also checks for source of errors. For example, in a modular architecture the diagnostic test will point to the faulty chip or board. In this way only the faulty subsystems is replaced.

Structural Test There are arguably two fundamental test paradigms: *Specification-Based Testing* and *Structural Testing* [Akbay and Chaterjee, 2007; Cheng and Chang, 2010; Siewiorek and Lai, 1981]. The structural test approach is based on the presumption "innocent until proven guilty" [Bennetts, 1981]. That means the DUT is considered error-free and the test strategy tries to find any errors that could appear. The structural testing relies on fault models. The principle is the following. In the beginning a dictionary of faults models is defined. As discussed earlier, fault models are abstraction of defects. Then, an optimized input stimulus is obtained for every fault in the dictionary. During the test phase, the strategy checks to detect only the faults defined in the dictionary.

From the economical point of view, the structural test approach is really advantageous: it is fast and it avoids exhaustive measurements. However, a structural testing technique can only be as accurate as its models. An important tradeoff exists between the generality of a fault model and the complexity of running test for the faults modeled. The more general a fault model, the easier is to generate tests and the higher probability that a defect may go undetected. On the other hand, if the fault model is too specialized, an explosion in the number of measurements required and computational time of test vector generation renders the model unusable.

The structural test approach has been widely adopted for digital testing because nearly all manufacturing defects in digital systems map well to faults like stuck-at, shorts, opens [Siewiorek and Lai, 1981; Bennetts, 1981; Boyce, 1988; Agrawal et al., 1993]. Using these models, the digital domain test provides reliable, abstract and standard interfaces for powerful test algorithms to be performed and for their performances to be compared relative to each other. Thus, digital systems are nowadays routinely factory tested with standard methods, aided by software for automatic test pattern generation, scan-chains, and built-in self-test features, all of which have become mature and cost effective (e.g. the IEEE 1149.1 standard [IEE, 2001]).

Specification-Based Test Similar fault models for analog-mixed signal and RF (AMS/RF) testing have been proposed [Milor, 1998]; however, the degree of abstraction in these models has been mostly device specific (circuit block, component or integrated circuit), and consequently generic interfaces for test generation based on these models have not been developed.

Faults in analog circuits can also be classified into two categories: catastrophic and parametric [Maly et al., 1986]. Catastrophic faults include open nodes, shorts between nodes, and other topological changes in a circuit. For IC, they usually result from local defect mechanism like particle on the wafer surface generated by equipment during processing, particles that block exposure of a local area during masking, oxide defects which short out transistors, severe misalignment of layers. For Printed Circuit Boards (PCB), catastrophic faults can come from excess solder, resulting in bridging between pins, lack of solder, a broken pin, or use of a wrong component.

Parametric faults refer to defects in a circuit that do not impair its topology. They usually appear due to imperfect parametric control in IC manufacturing or to local defect mechanisms, like particles, which could modify a transistor's length or a capacitor's size. When these imperfections are too great, the fabricated circuits will not meet the datasheet specifications.

Catastrophic failure are easier to detect than parametric failures. In our research, we target both catastrophic and parametric failures.

Although a generic fault-based test methodology is still the holy grail of analog testing, these devices are almost always tested in production for their performance specifications.

Compared to the structural paradigm, the specification-based testing rely on the presumption "guilty until proven innocent". In effect, the DUT is not given a "pass" ticket until the measurement of every specification checks against the product data-sheet [Akbay and Chater-

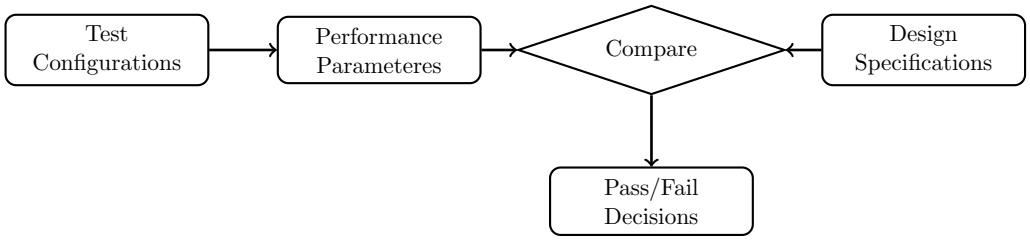


Figure 4.1: Specifications-based test strategy [Cheng and Chang, 2010]

jee, 2007; Cheng and Chang, 2010]. The specification-based diagram is illustrated in Fig. 4.1. Specification-based testing of analog devices is usually performed in a sequential manner, mimicking device characterization. For each specification the following procedure is followed:

1. initialize the measurement instrumentation and configure the DUT for the test
2. apply the predefined stimulus (input signals) and collect output (responses) at test points
3. using the digitized DUT response, extract the circuit performance w.r.t. the specification being checked

If all the extracted performances meet the specifications, it is considered that the DUT passed the test, otherwise the DUT is rejected. Considering the fact that this procedure is repeated for each specification and that direct measurements of the performance parameters of AMS/RF circuitry are usually time-consuming, the cost to test the analog portion of a mixed-signal device can account for up to 50% of total product cost [Mukherjee, 1997; Kupp et al., 2011].

From the point of view of SDR platforms, a common shortcoming of the structural tests is that the models are tied to specific operating modes (frequency, modulation, standard, etc.) and architectures, and cannot be applied easily to multi-mode tactical radio units. Test strategies that use a given fault model must necessarily hold assumptions on the operation modes of the radio, whereas in SDR platforms nearly all aspects are field-configurable. In this scenario, specification-based testing seems unavoidable. The outstanding challenge for SDR testing is then how to conduct specification testing without external equipment.

4.2 Challenges in AMS/RF Testing

In the previous section we saw that, while digital test techniques are mature and routinely applied by industry, the AMS/RF testing in manufacturing still relies on ad-hoc device-specific methods. This reflects into the burgeoning cost of the test, as high as 50% of the final part cost [Roberts and Dufort, 1999]). Test engineers agree that the gap between the digital and AMS/RF test is at least 30 years and it only seems to increase as the technology scales. In order to reduce the overall test cost and implicitly this gap, efficient AMS/RF tests are critically needed. In this section we cover the challenges that have to be addressed to narrow this gap.

The most fundamental challenge is that, in contrast to digital circuits, the functionality of an AMS/RF circuit cannot be well modeled by an exact closed form expression similar to a set of Boolean equations. In effect, an AMS/RF circuit has a nominal behavior and an uncertainty range (usually characterized by a normal variation). In these conditions, the definition of what constitutes an acceptable behavior is application dependent and it is impossible to generalize easily, such as logic operations.

Another key challenge in testing state-of-the art AMS/RF systems is the degraded accessibility of individual building blocks. The ability to control the inputs and to observe the

outputs of each building block is necessary for thorough characterization and for minimizing test escapes. A common measure to enhance the observability and the controllability consists in adding on-chip (on-board, on-unit, according to the level of integration) measurement and test stimuli generation circuitry. However, one has to be careful not to impair normal operations. For example, the RF path is sensitive to loading and mismatch and, thus, particular attention to impedance levels has to be paid.

Another obstacle is the lack of good AMS/RF simulation models that cover all the mode of operation and execute reasonably fast. The test engineer has to wait for the prototype in order to start the debugging of the production test program. It is now commonly thought that this sequential production/testing flow is not cost effective and it must be reconsidered.

In conclusion, an efficient test strategy should meet the following requirements:

- must not degrade the performances of the DUT
- must not interfere with the DUT during normal operation.
- must posses simple hardware/software implementation: low added footprint, minimum additional computing load
- must reduce test time on expensive equipment by incorporating some built-in self test-capabilities

Besides the previous challenges that are associated with the test of generic AMS/RF designs, the SDR platforms introduced new difficult challenges: the need for flexibility. Unlike conventional RF communication equipments, SDR platforms must satisfy strict requirements for a wide variety of modulation standards. The proposed test strategy must be able to cover thoroughly and efficiently all key specifications of the radio unit.

SDR platforms and tactical radio units are being developed to ensure that a device or system will never fail, or if it needs to fail, "gently" fail. These architectures implement various forms of error detection and correction to constantly monitor operation. If a fault is detected, the system can adjust to the fault by: correcting the error based on a correction algorithm; performing the operation again in hopes it was a onetime fault; changing the operational conditions of the functional block that experienced the error such that the functional block begins to operate correctly and yield a correct result; or disable the malfunctioning functional block and routing the information elsewhere for processing. Only when all possible options for recovery have been evaluated and failed, will the device or system fail. Fault tolerant devices represent a challenge to testing as they are architected to rarely if ever fail. In order to adequately determine if the device is functioning properly as it leaves the factory, test must be able to disable or reduce the capabilities of recovery mechanisms in order to evaluate the device or functional block for correctness.

Finally, in the military and defense sector we are talking about lifetime defect-free devices. Typically, these devices do not only require zero defects at the factory, but also need to guarantee fail free operations over the entire lifetime.

To sum up, industry and the researchers have not yet converged to a recognized widespread and unified AMS/RF test methodology. Nonetheless both agree that the path to this objective involves stronger (and earlier) involvement of a test engineer in the product development cycle. This will allow the designers and the test engineers to share their experience, their concerns and to work together toward the best compromise between functionality, performance and test. The paradigm of involving the test engineer and the test plan early on in the design cycle has been referred to as *Design for Testability* (DfT), and it became really popular in the last decade. The

Figure 4.2: Automated RF test equipment ATES500 developed by DiagnoSYS

DfT methodologies aim to reduce the test development effort and cost by building testability in the product. Every strategy that we'll discuss later aims to implement the DfT paradigm.

4.3 Automated Test Equipments

As mentioned, current industrial practice for production test containing AMS/RF circuitry is specification test. This entails the use of expensive, specialized equipment known as Automated Test Equipments (ATEs) [Wolf et al., 2006; Cruz et al., 2010]. ATEs are expensive, relatively brittle and hard to master tools. An example of an ATE marketed by DiagnoSYS is shown in Fig. 4.2. ATEs became a bottleneck for the large scale production of communication equipment. The challenges of AMS /RF testing using ATEs are detailed in Wolf et al. [2006] along with proposal for reducing test-time and complexity (hence cost).

In our case, production test of SDR platforms, there are complex interactions between AMS/RF circuitry, digital hardware, and software that compound the test problem. SDRs operate in both the analog and the digital domains, thus to verify their performances mixed-domain instrumentation is necessary, at least. Such an arrangement is proposed in Cruz et al. [2010] where the authors use logic analyzers, oscilloscopes and spectrum analyzers to evaluate the ACPR and the EVM of an homodyne transmitter (Fig. 4.3). Their work highlights the fact that while testing a AMS/RF signal, special attentions need to be paid to synchronization between the various instrumentation, as well as the memory size needed to extract a behavioral model.

Another example of set-ups for testing of SDRs is given in two application notes [Tektronix, 2008, 2006]. Tektronix summarizes the advancement in AMS/RF instrumentation and present some state-of-the-art instrument marketed for SDR testing such as: Real Time Spectrum Analyzer (RTSA), Arbitrary Waveform Generator (AWG), Oscilloscope and Logic Analyzer. These test set-ups match the flexibility of the SDR platform, but are too expensive and slow for large-scale test programs, where dedicated fixed-function ATEs are the norm.

To summarize, ATE and "ad-hoc" SDR test set-ups (rack & stack) can be purchased, but suffer from serious limitations:

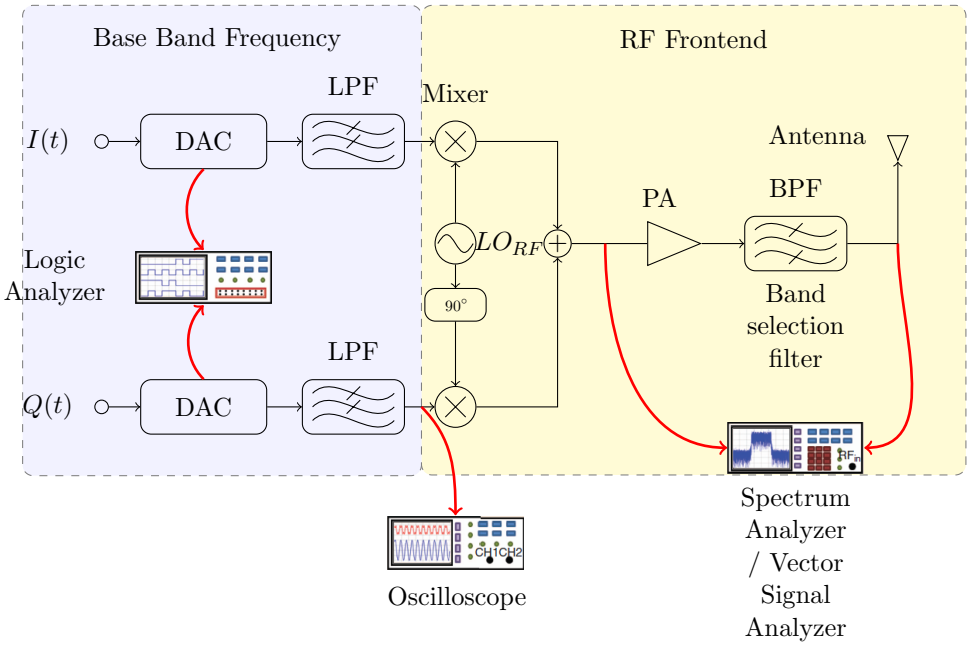


Figure 4.3: Instrumentation employed in testing a software defined radio transmitter where several instruments are combined. A logic analyzer acquires the digital logic bits at the output of the DSP section, an oscilloscope analyzes the analog signal after the digital-to-analog conversion (DAC) and low-pass filter (LPF) reconstruction, and a spectrum analyzer or a vector signal analyzer obtains the analog RF signal right after the quadrature modulator or after amplification [Cruz et al., 2010]

- without generalized fault models, AMS/RF test is mainly a matter of specifications checking. Nonetheless, direct measurement of performance specifications is lengthy, prone to handling mistakes and noise, and tedious. In addition, the test of RF transceivers may require the measurement of over one hundred parameters [Razavi, 1998].

- each specification requires different test set-ups. Load-board design might be as difficult as the design of the radio board itself. This will lengthen the test time, due to instrument settling and relay switching time, which may be longer than the actual test itself [Kramer, 2005; Acar and Ozev, 2007]

- accurate AMS/RF capable ATEs are extremely costly and hardly reconfigurable, which means that a test line must do with a small number of ATEs that can test a large number of devices only in a limited way. Amortizing their cost is problematic, opposing large production runs to per-unit test time.

- ad-hoc set-ups (as given in Fig. 4.3) are expensive and unsuited for large-scale automated test of finished products.

Due to the previous listed considerations, testing by ATEs became a bottleneck in the manufacturing process. To address this issue, research engineers have been searching for alternative (cheaper) techniques to extract circuit performance. These investigations have pursued many paths. The main venues of work will be reviewed in later sections: shortening measurement time, minimizing test sets, substituting expensive, calibrated test instruments by cheaper test equipment, or alleviate the need of external (off-chip, off-board, off-unit) instruments.

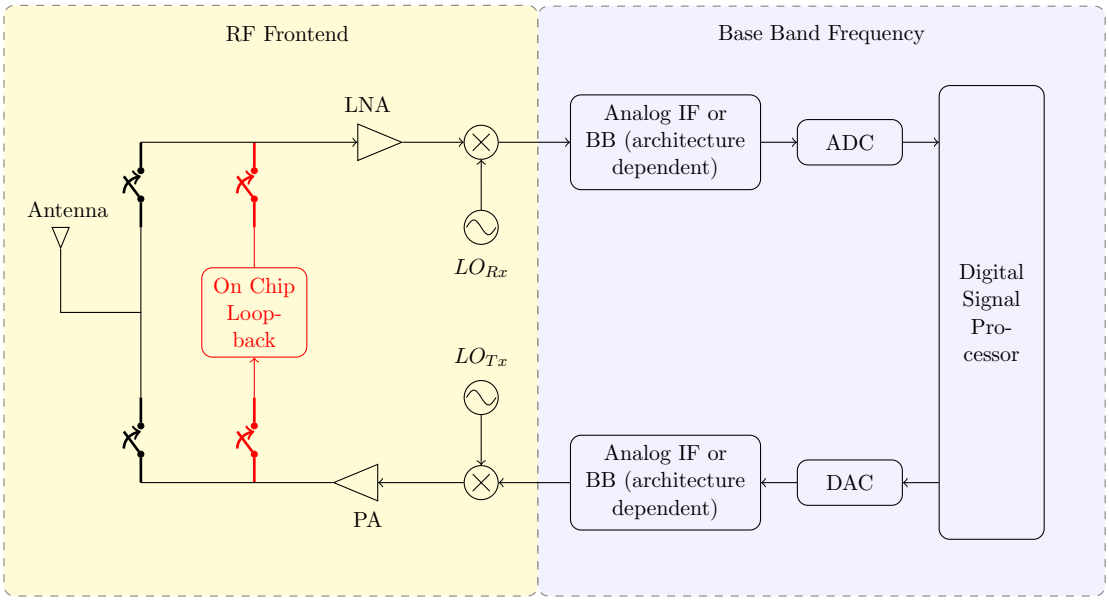


Figure 4.4: Loopback test architecture

4.4 Built-In Self-Test

Built-in Self-Test (BIST) schemes are arguably the most promising way to alleviate the need of external equipment. A BIST consists in placing the test circuitry directly on the same die as the desired DUT. This includes test stimulus, measurement circuitry, and interconnect and control circuits. Among test concepts, the most attractive is undoubtedly the BIST one, to forgo the use of external equipment for measurements. Accordingly, the use of built-in structures to facilitate or enable some form of self-test has been the focus of a large number of publications.

The advantages of having such an on-chip (on-board, on-system) system for measuring RF performance parameters are clear.

4.4.1 Loopback BIST

Among the efforts of alleviating the need sophisticated measurement equipment, the loopback approach is one of the most promising RF BIST technique for RF transceivers [Onabajo et al., 2009; Negreiros et al., 2007; Dabrowski and Bayon, 2004; Nassery and Ozev, 2012; Haldes et al., 2005].

In a nutshell, RF loopback consists in using the transmitting part to excite some parts or all of the receiver. The block diagram of a loopback test architecture is illustrated in Fig. 4.4. The key modification is to add components that allow the reconfiguration of the on-board (or on-chip) resources to carry out some type of characterization. An example is shown in Fig. 4.4 where the loopback circuit is inserted in the RF section frontend and the whole transceiver is thus tested. Other additional signal insertion nodes could be considered. For example, a sequential test program could be implemented thusly: first to test the transceiver without considering amplifiers (PA and LNA, whose test is usually the most challenging) by a loopback path excluding them. As soon as the low power circuit is fully characterized, use the configuration presented in Fig. 4.4 and test the two amplifiers (i.e. the full transceiver) [Fan, 2010].

Loopback BIST has attracted a lot of attention due to its potential advantages:

- avoids routing sensitive signals in and out, thus reducing cost and complexity of load

boards and ATE head

- could allow multi-site testing (simultaneous test of multiple DUTs)
- logical reuse of powerful signal processing resources already available in the DUT: data converters (ADCs, DACs), memory resources, specialized processors (DSP, GPP)
- could allow in-field self-test

Nonetheless, loopback BIST suffers from one major drawback: fault masking. Fault masking arises because RX and TX faults are not observable separately, which could lead to test escapes. Let's consider for example a transceiver with a highly nonlinear power amplifier that generates an unacceptable amount of distortion in the adjacent channels. If this transceiver is tested with a loopback approach, it might be possible that the filters in the receiver path will mask the TX fault. Or even if the fault is detected it would be almost impossible to locate the source. Thus, in its simplest form, loopback BIST is ideal for a go/no-go screening stage but not suitable for production test program, without further improvements.

One fundamental reason for the loopback fault-masking issue in the given example is that the RX is designed to operate in harsh environments, nearby strong interferers. They are constructed to filter out these interferences as much as possible. In a loopback configuration the interferer might in fact be an intermodulation product produced by a faulty TX or a carrier leakage, i.e. a fault symptom. The receiver will inherently filter these components and the fault will be covered up.

Let's analyze a second case: a transceiver in which the TX is too weak or too powerful. By design, the RX will compensate in the opposite sense. As result, the estimated SNR/BER of the combination is erroneous (too optimistic).

Another potential issue of the loopback strategy is the reduced observability. This situation occurs when a fault in the transceiver is detected but the error source cannot be distinguished. The reduced observability appears because of the high correlation between the TX and RX specifications. For example the IQ mismatches in the RX correlate with the IQ mismatches in the TX. In order to decorelate these specifications, and implicitly to improve the loopback observability, several sensitization techniques have been proposed. The most interesting are presented in later sections.

Finally, not all transceivers are compatible with a loopback test configuration. If the receiver and the transmitter communicate at different frequencies, or if they share the same oscillator, loopback circuit might be impractical [Dabrowski and Ramzan, 2010].

There are many published idea for applying loopback BIST to RF systems and circumvent fault masking. In Onabajo et al. [2009] an on-chip loopback containing a variable attenuator and a offset mixer and working in the 1.9- to 2.4-GHz range was designed. Several root-mean-square (RMS) power detectors were placed along the signal path to allow identification of fault locations. In Negreiros et al. [2007] a RF single-bit digitizer is used during loopback operation, allowing observation of spectral characteristics of the RF signal. But even in a loopback mode the BER and EVM measurement takes a long time because of the high performances required (in a modern transceiver BER are in the range of $10^{-12} - 10^{-15}$). To reduce this time several approach are proposed in Dabrowski and Ramzan [2010]; Dabrowski [2003] and Dabrowski and Bayon [2004]: intentionally inject a predetermined amount of noise to increase BER and thus to reduce the number of symbol needed or digital pre-distortion of the baseband signal.

In Haldes et al. [2005] a loopback BIST is used in an alternate test approach to predict all the linear and the nonlinear specifications of the transmit and the receive subsystems. Optimized periodic bit streams are used as test stimuli. In this approach the on-chip DSP is reused for

test stimulus synthesis and response analysis. A similar test plan is given in Nassery and Ozev [2012], where authors propose an analytical technique for characterization of transceiver IQ imbalances in the loopback mode.

Other successful application of the loopback technique are reported in Negreiros et al. [2007]; Onabajo et al. [2009]; Halder et al. [2008].

These applications of loopback paradigm are detailed in the following.

4.4.2 Behavioral RF Modeling

One way to enhance the fault-masking is to use a priori information about the DUT, such as models of the circuit. The idea isn't new, and is extremely attractive for RF systems where non-linearity offers the possibility of greatly amplifying the effects of a flaw. Transistor-level models would offer the most potential to explore, however simulation times are too long for the use of automatic optimization algorithms. Because of this, behavioral models are nearly universally used instead. For RF circuits, the behavioral models offer a very good trade off between accuracy and simplicity.

The behavioral models of some of the most important transceiver's blocks are listed in the following [Haider et al., 2003; Halder et al., 2008].

- **filters** are modeled typically in the S-domain, linear transfer functions relating magnitude and phase to frequency.

- **power and low-noise amplifiers** (LNA, PA) are modeled as non-linear transfer functions of the type:

$$y_A(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{4.2}$$

  where α_0 is the DC offset, α_1 is the small signal gain, and α_2, α_3 are non-linearity coefficients. These coefficients $(\alpha_0, \alpha_1, \alpha_2, \alpha_3)$ are computed from the simulation of a transistor level model that express real non-linear behavior.

- **mixers** are modeled in time-domain, by a product of non-linear transfer functions followed by an ideal multiplier:

$$\begin{aligned} y_A(t) &= \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \\ y_{mixer}(t) &= C \cdot y_A(t) \cdot x_{LO}(t) \end{aligned} \tag{4.3}$$

  where $x(t)$ is the signal at the input of the mixer and the x_{LO} is the clock generated by the local oscillator. The constant C represents the gain of the mixer. The non-linear behavior is characterized by the coefficients α_2 and α_3.

- **oscillators** The behavior model of the oscillator is defined in the frequency domain only, usually by a function relating output power versus frequency. Sometimes noise power vs frequency is also used.

These individual behavioral models are then cascaded in a simulation tool (often Matlab, Simulink, SystemVue, etc.) to model a given RX/TX architecture. This complete model can be used to observe the transceiver behavior, to optimize the input stimuli and to analyze the measurements.

4.4.3 Model-Based RF Test Strategies

Using the previous models, several attempts to improve the loopback approach have been attempted. An example of an approach that uses behavioral models to improve the loopback observability is given in Acar and Ozev [2007]. The overall idea presented is to use a behavioral model of the blocks to build an analytical function relating the power amplifier non-linearity to the I/Q signals at baseband. The initial proposal used a lower cost baseband test set-up to observe the RX I and Q waveforms and extract TX characteristics such as TX gain, TX IIP3, amplitude and phase I/Q mismatches. The most important advantage of measuring these non-idealities is that they can be corrected in baseband.

Experimental results and further improvements of this approach are presented in Nassery and Ozev [2012]; Erdogan and Ozev [2008, 2010] where, in order to alleviate the need of any external equipment, an analytical model of the entire transceiver in the loopback mode is proposed.

The authors demonstrate how several RF transceiver specifications (gain, IIP3, amplitude and phase mismatch) can be derived from the baseband I/Q streams. Their method is applied to an homodyne transmitter (as in Fig. 4.5). Their proposal works as follows. Let $I(t)$ and $Q(t)$ be the in-phase and quadrature baseband signal. The I/Q mixer output can then be expressed as:

$$x_M(t) = G_I I(t)\cos(\omega_C t + \phi_I) + G_Q Q(t)\sin(\omega_C t + \phi_Q) \tag{4.4}$$

where ω_C is the carrier frequency, G_I and G_Q are the gain of the I and Q channels, ϕ_I and ϕ_Q are the phases of the I and Q channels, respectively. To highlight the amplitude and phase mismatch, Eq. 4.4 can be rearranged as:

$$x_M t = G\{I(t)\cos(\omega_C t) + (1+p)Q(t)\sin(\omega_c + \phi)\} \tag{4.5}$$

where $G = G_i$ is the common gain of I and Q paths, $p = G_Q/G_I - 1$ is the gain imbalance and $\phi = \phi_I - \phi_Q$ the phase imbalance between I and Q paths. If the power amplifier is modeled as in Eq. 4.2 and setting DC offset to zero, one obtains:

$$x_{RF}(t) = \alpha_1 x_M(t) + \alpha_2 x_M^2(t) + \alpha_3 x_M^3(t) \tag{4.6}$$

Finally, zero-mean Gaussian white noise is added to Eq. 4.6:

$$x(t) = x_{RF}(t) + n(t) \tag{4.7}$$

After applying Eq. 4.4 to Eq. 4.6, expanding, and removing higer order terms, one can obtain the formulation of the I and Q symbols decoded at the receiver:

$$\begin{aligned} \hat{I}(t) &= (\alpha_1 + \Delta)[I(t) + (1+p)Q(t)\sin(\phi)] + \hat{n}(t) \\ \hat{Q}(t) &= (\alpha_1 + \Delta)(1+p)Q(t)\cos\phi + \hat{n}(t) \\ \Delta &= \frac{3}{4}\alpha_3\{I^2(t) + [Q(t)(1+p)]^2 + 2I(t)Q(t)(1+p)\sin(\phi)\} \end{aligned} \tag{4.8}$$

where $\hat{I}(t)$ is the received in-phase signal and $\hat{Q}(t)$ received quadrature signal and Δ is a non-linear compression term originating from the α_3 term. Eq. 4.8 provides an important relation between the baseband waveforms, sent and received, and that can be controlled or measured, and some of the non-idealities in the TX architecture. Using this analytical relation and a low-cost test set-up (typically used for EVM/BER measurement) several vital TX specifications are observed such as transmitter gain, IIP3, noise figure, and amplitude and phase mismatch (for experimental results see Acar and Ozev [2007]). Further improvements of this technique

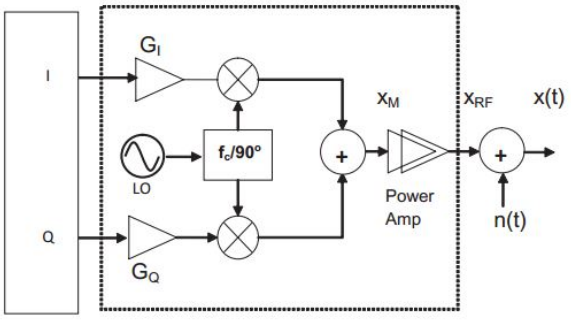


Figure 4.5: Model of an generic quadrature transmitter [Acar and Ozev, 2007]

are presented in Nassery and Ozev [2012]; Erdogan and Ozev [2008, 2010] where, in order to alleviate the need of any external equipment, loopback BIST configuration is proposed.

Besides extracting DUT specifications, behavioral modeling has been used in other test related applications. In Acar et al. [2008] the authors propose a method to reduce the time test for EVM measurement by optimizing the input sequence. The idea is to minimize the length of the input stimulus by selecting only the symbols that are most sensitive to impairments in the circuit. Transistor level simulations and and measurements on a prototype device show that the symbol sequence length for EVM testing can be reliable reduced.

Advancing these results, the authors in Nassery et al. [2013] present an analytical method for calculating the EVM of OFDM transmitters from already measured parameters. The work is motivated by the fact that EVM measurement usually is the most expensive (compared with other parameters like IIP3 or IQ imbalances). To achieve this cost reduction, the authors develop a mathematical relation between EVM and other less demanding measurements, such as IQ imbalances, noise, IIP3, AM/AM and AM/PM distortion. Using this model, it is shown possible to calculate EVM without making a single EVM measurement. The approach is validated in simulations and on a hardware platform (off-the-shelf components). The model is able to calculate EVM with less than 1% error. In this work the models used are ideals. If another nonlinearity or another architecture needs to be considered, it is possible that the complexity might not be handled analytically.

From the point of view of SDR testing, the techniques that relies on behavioral models to extract the most important nonlinearities and IQ imbalances in a quadrature transceiver (phase mismatch, gain mismatch, DC offset, and time-skew) have some shortcomings. First, they are limited by the completeness of the model. Under configurations unforeseen by the model, the entire test strategy will fail. Furthermore, for SDR platforms that are field-upgradeable through software, such simple models have not been developed yet.

Secondly, it's hardly feasible to continue measuring simple parametrics and then try to correlate these characteristics to ultimate system performance for all possible waveforms, protocols and modes of operation. Issues such as gain, noise figure, third-order intercept point remain useful designer metrics, but what really counts in the field is that the radio functions reliably and is not a source of spurious emissions.

Further complicating matters, cutting-edge radios support new multiple-in-multiple-out (MIMO) techniques, which allow antennae to process many incoming and outgoing signals simultaneously. Effective verification of these systems requires true duplex-functional radio tests. At a minimum, the test protocol for these platforms must include :

- Adjacent channel power ratio (ACPR) (also known as adjacent channel leakage ratio (ACLR)): the ratio of transmitted power to power in the adjacent radio channel

- BER : Bit Error Rate
- Error vector magnitude (EVM)

To conclude this section, test strategies based on behavioral models generally target a fixed architecture and are optimized for a specific standard and are, as such, better suited for factory test of mass market commercial products.

4.4.4 Alternate Tests

4.4.4.1 Basic Concepts

As mentioned, loopback BIST is often coupled to some strategies to expose faulty behavior through well chosen measurements. The test techniques mentioned above rely on direct measurement of some or all of the specifications. These techniques can be effective, but they still rely on reasonably precise measurements of quantities that are related to the test specification by some analytic formula. Even when several DfT techniques are employed, the test operation still takes significant time. A different paradigm, advanced by Chaterjee and his group, attempts to shorten test time and minimize equipment cost by giving up the extraction of characteristics from measurements. Instead of direct measure of the specifications, this technique (referred as *alternate testing*) take advantages of heuristic optimization algorithms (genetic algorithms, neural networks, etc.) to predict the DUT specifications from a set of parameters easier to measure but strongly correlated with the initial specifications [Variyam and Chaterjee, 1998; Natarajan, 2010; Natarajan et al., 2008; Halder et al., 2008; Chatterjee et al., 2009; Haider et al., 2003].

The basic principle of the alternate test is represented graphically in Fig. 4.6. Variations of any process or circuit parameter (such as width of a FET, value of a resistor) in the process space $\mathscr{P}$ affect the circuit specification space $\mathscr{S}$ by a corresponding sensitivity factor. Let $\mathscr{M}$ be the space of measurements (amplitude values of a subsystem output spectrum) selected such that each variation of a parameter in $\mathscr{P}$ that affects the space $\mathscr{S}$ also affects the space $\mathscr{M}$. In other words, the two spaces of measurements and specifications are strongly correlated. Given the parameter space $\mathscr{P}$, for any point in $\mathscr{P}$, can be computed a mapping non-linear function, $f : \mathscr{P} \rightarrow \mathscr{S}$. Similarly, for the same point, another mapping function onto the measurement space, $g : \mathscr{P} \rightarrow \mathscr{M}$, can be computed. Finally, as shown in Variyam and Chaterjee [1998], a mapping function $h : \mathscr{M} \rightarrow \mathscr{S}$ can be constructed from all the measurements in $\mathscr{M}$ using non-linear statistcal multivariate regression. Given the function h, an unknown specification of the DUT can be predicted from the measured data. The function h is usually constructed using Multivariate Adaptive Regression Splines (MARS).

The alternate test methodology is usually carried out in three steps:

- select an optimal test stimulus. The test stimulus selection uses behavioral models and optimization algorithms
- build the mapping function between the test response and the DUT specifications. During this step, specification measurements from a set of DUT circuits (training set) are required
- actual test. the trained models are used to predict the specifications of the DUT from the observed test response

In order to keep the alternate tests practical, the measurements must be taken by low-cost on-chip sensors. These sensors are in fact signal converters that translate some set of characteristics of high-frequency waveforms into low-frequency or DC signals for further analysis.

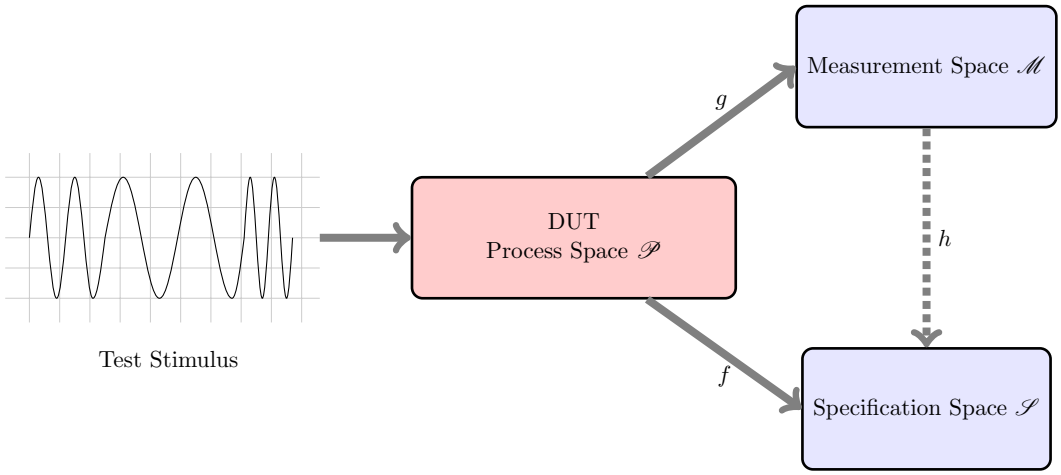


Figure 4.6: Principles of the alternate test paradigm

These sensors are placed in critical path points of the DUT. In addition to accurate conversion of a RF signal to a baseband signal, these sensors must meet the following constraints:

- a low area overhead
- an input impedance that minimizes the loading effect to the DUT
- a wide dynamic range
- reliability and reproducible behavior

Three such sensors are commonly used in published papers [Natarajan et al., 2008]:

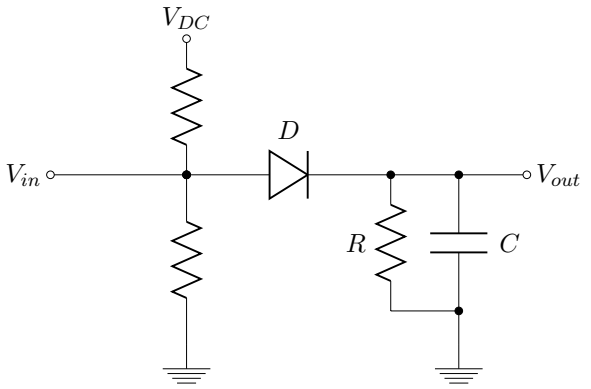
- **envelope detector** as shown in Fig. 4.7a, introduced in Bhattacharya and Chaterjee [2005]. Requisite envelope detection can properly be performed through proper adjustment of the RC constant value
- **peak detector** as shown in Fig. 4.7b, described by Natarajan et al. [2008].
- **Root Mean Square (RMS) detector** as shown in Fig. 4.7c, described in Han and Chaterjee [2006]. The DC output signal of this sensor is proportional to the RMS power amplitude of the RF signal

These sensors are connected to the main RF signal path, where impedance matching is a critical concern. Since they interfere with this aspect, the RF specifications may be degraded by their presence. Therefore careful judgement is need on how and where the sensors are placed.

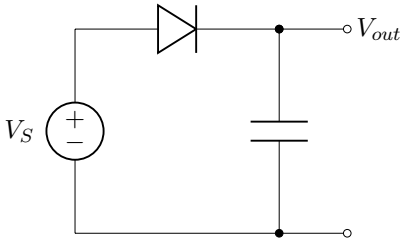
The advantages of the alternate tests are appealing:

- ability to measure multiple RF specifications of embedded devices using a single data acquisition (or few acquisitions)
- ability to perform test autonomously with little or no external RF test equipment support and minimal on-chip hardware overhead (and consequently minimal impact on device performance)

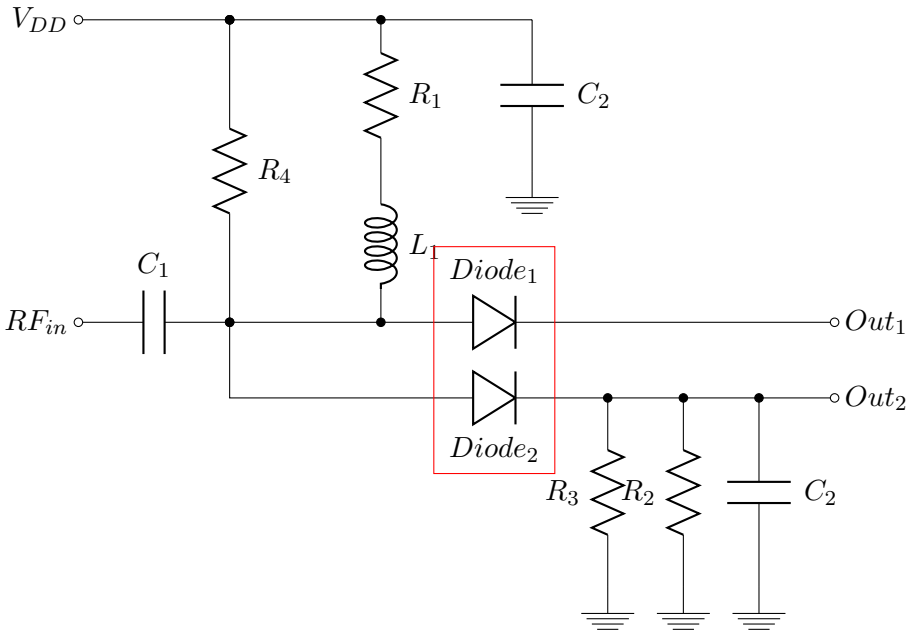
In the next section, we show several applications of the alternate test approach proposed in literature. We'll see that this paradigm can be used not only for AMS/RF test, but also for circuit calibration, test time reduction and input stimuli optimization.



(a) Envelope detector



(b) Peak detector



(c) RMS detector

Figure 4.7: Three on-chip circuits that can be used as RF sensors for alternate tests [Natarajan et al., 2008]

4.4.4.2 Alternate Test Applications

A lot of efforts have been made to improve and to prove the efficiency of the alternate test approach. For example, it has been shown in Natarajan et al. [2008] that the type of sensors and their placement have a large influence on the test performance. The study investigate the three sensors shown in Fig. 4.7 by taking into account the accuracy of the prediction and the impact of the sensors over DUT performance. They show that envelope detector gives the best performances.

However, the RF sensors previously presented degrade the overall performances of the DUT because of the electrical interaction with the RF path. Recognizing this problem, several researchers strived to apply alternate test using other sensing principles. In Abdallah et al. [2012] the authors propose a new set of RF temperature sensors. The key advantage of their proposal is that temperature sensors are less intrusive, and without electrical presence there is no loss of performance. The working principle is that a defect will shift the power dissipated in the DUT which, in turn, will produce a temperature change in the vicinity of the DUT that can be measured by the temperature sensor. The topology of their temperature sensor is based on an operational transconductance amplifier (OTA) whose differential pair is unbalanced due to the temperature difference between transistors. One of the transistor is placed in the vicinity of the DUT and the other one as far as possible. In addition to being non-intrusive, these sensors have the advantage that they can be tested themselves before use for RF fault detection. This sensor is employed in Abdallah et al. [2012] for defect detection, while additional process sensors are used in an alternate test approach to predict the performances of a 2.4 GHz LNA.

The alternate test approach has also been employed to estimate fundamental transmitter specifications such as gain and IIP3. In Haider et al. [2003] the authors have shown that the specifications of a homodyne receiver (gain and IIP3) can be predicted using the alternate test methodology. The test generator produces an optimized multi-tone test stimulus (alternate test) from which the subsystem test specifications can be simultaneously computed. To expose system non-linearity the test stimulus consists of large-signal sinusoidal multi-tones whose parameters (amplitudes and frequency) are generated using iterative search algorithms. The measurements are done placing a spectrum analyzer at mixer output, thus the amplitude spectrum is used as the measurement space. The experimental results show that the gain and the IIP3 can be predicted with a error of $\pm$1dB.

Nonetheless, the previous approach still relies in external measurements. Addressing this limitation, the authors in Haldes et al. [2005] go further and propose an alternate test of the entire transceiver in loopback mode. The input stimulus consist of optimized periodic bit-streams that are created at baseband. The signal is routed through the entire transceiver and the received baseband signal is used as measurement space. No additional sensors are used. The approach is validated on hardware setup consisting of an transceiver designed for the 900 MHz GSM band. Measurement results show that the RX and TX, gain and IIP3 can be estimated with a precision of $\pm$3 dB.

A similar approach for the test of the RF transceivers in loopback mode is presented in Onabajo et al. [2009]; Fan [2010]. Compared to the previous solution, the proposed test technique places several RMS detectors along the signal path to allow fault localization and improve test observability.

The main issue with the previous test strategies is that the estimate of the specifications is not accurate and is definitely under-performing w.r.t. manufacturing test norms. Addressing this issue, the authors in Maliuk et al. [2010] propose a different approach: they develop a go/no-go test classifier which relies on alternate test paradigm. Thus, instead of predicting the DUT specifications, the proposed strategy provides a classifier to draw out a straightforward go/no-go

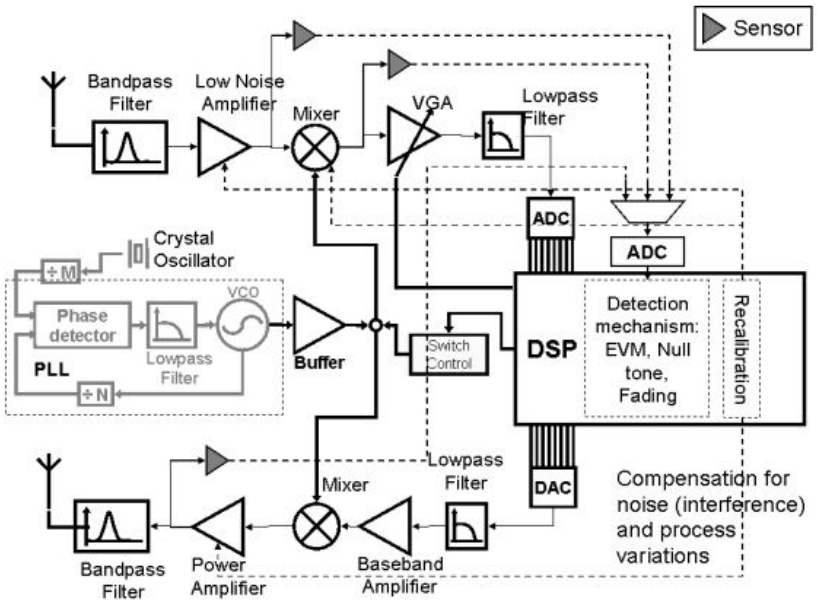


Figure 4.8: Alternate-test-based tuning and testing strategy [Chatterjee et al., 2009]

decision. The classifier consists of a neural network which is trained using genetic algorithms. In this case two different genetic algorithms are compared (k-Nearest-Neighbors and Ontogenic Neural Network). The test stimuli consist of single tone signals. Hardware measurements obtained from an LNA show that a relatively small number of non-RF specifications are sufficient to predict the correct pass/fail label. Quantitatively speaking, the proposed classifier is able to provide a correct go/no-go decision with a prediction error of 0.5%. The prediction error may change depending on the type of classifier, the number of hidden layers of the neural network, etc. For more details see Maliuk et al. [2010].

Besides being employed in specifications estimation and go/no-go testing of RF circuits, the alternate test paradigm has also been reported successful in other applications, such as tuning of AMS/RF systems. Nowadays, it is well known that variations in the manufacturing process, stemming from the used of scaled CMOS technologies, result in significant yield loss. To address this issue, post-manufacturing tuning strategies for yield recovery have been proposed. A procedure of testing and tuning an RF transceiver was introduced in Chatterjee et al. [2009]. The strategy is based on the alternate test paradigm and its block diagram is depicted in Fig. 4.8. The operating principle is similar to the test procedure. First, a statistic model able to extract DUT specification from the sensors response is created. One can see in Fig. 4.8 how the sensors are placed all along the signal path to improve loopback observability. Then, the model is used to estimate the DUT specification. If the specifications are outside the acceptable limits an iterative tuning procedure is started.

Another interesting application of alternate test consists in reducing ACPR measurement time by optimizing the input stimuli and is given in Bhattacharya et al. [2004]. The authors propose a novel algorithm for measuring ACPR that uses periodic bit-stream sequences as input stimuli. The periodic bit-sequence is optimized through an alternate test generation algorithm. Their experiments showed the number of measurement at the output of the TX was reduced by a factor larger than two while the accuracy respected a value of 0.2%.

Even if the alternate test started to show better performances, it is still a long way until this methodology will be adopted on large scale by the industry. And that is because compared to

specifications-measure-based techniques, the alternate test performances are lower (in terms of test-escapes and DUT specification estimation errors). During a tutorial at Design, Automation, and Test in Europe (DATE2012) conference, Gordon Roberts explained that, in his opinion, the alternate test techniques are not mature enough. The authors in Kupp et al. [2011] consider that the key to the success of the alternative test approach is estimation of test metrics (test escapes or yield loss) as early as possible in the test development process. Addressing this problem, they employ a test metrics estimation technique based on non-parametric kernel density estimation, and, demonstrate a real-world case study of test metric estimation efficiency at parts-per-million levels.

For the test of SDRs, the alternate do not seem an viable solution as they rely on models that are not available yet. Moreover, in order to obtain satisfactory performance, the alternate tests require an extremely large number of units to be measured beforehand. Tactical radio units production runs are far below these numbers.

4.5 Conclusions

To sum up, AMS/RF DfT and BIST techniques are lagging. No proven alternative to performance-based AMS testing exists and more research in this area is needed. Analog BIST is still an open problem and in need of more research. Fundamental research is needed to identify techniques that enable reduction of test instrument complexity, partial BIST or elimination of the need for external instrumentation altogether.

Alternative, alternate, loopack techniques have been published along with some BIST solutions, but not implemented as standard RF test strategies. This area is in need of new ideas on low-cost test implementations.

The complexity and flexibility of SDR systems gives rise to more complex implementations, which in exchange limit the testability. Current available industrial test strategies face important obstacles due to the costly RF test equipment, long test time and lack of flexibility. In order to reduce the test cost new strategies are needed and have been proposed by the research community. Built-in Self-Test (BIST) schemes are arguably the only way to address these efforts. A BIST consists in placing the test circuitry directly on the same die as the desired DUT. This includes test stimulus, measurement circuitry, and interconnect and control circuits.

Amongst the proposed BIST techniques, the loopback approach is undoubtedly one of the most promising. However, the loopback may be subject to fault-masking situations that will provoke reduction of the test performance (in terms of yield loss and fault coverage). To address the fault-masking issue several sensitization techniques have been proposed.

The bibliographical study lead us to several important conclusions. First, in order to reduce the test cost of RF/AMS circuitry a BIST strategy have to been considered. The loopback approach might be the solution to the cost test reduction problem. Due to the difficult RF modeling, the specification-based testing seems unavoidable. Considering these conclusions, we proposed and developed a flexible BIST strategy for SDR transmitters. The technique is described in the next two chapters.

Chapter 5

Undersampling

Contents

5.1 Introduction

During the past three decades, the rapid evolution of digital integrated circuit technologies has led to ever more sophisticated signal processing systems. The key enabling technology of this revolution are the Analog-to-Digital Converters (ADCs) which convert a continuous-time signal to a stream of numbers at finite resolution. At the heart of all practical ADC systems lies the Shannon-Nyquist theorem. Often attributed to Nyquist [1928]; Shannon [1949], but dating back to Whittaker [1915]; Kotelńikov [1933], the basic formulation of the Shannon-Nyquist theorem states that an analogue signal bandlimited to B Hz can be perfectly recovered from uniform samples if the sampling rate is at least $2B$ samples/sec.

However, even though the marketing people promise more and more (for less), conversion speeds that are related to the signal's maximal frequency component are not always achievable. This is specially true for RF communications waveforms that occupy a narrow bandwidth but at high frequency (up to 6 GHz for the majority of cases). In order to deal with this class of signals, several bandpass sampling techniques have been proposed and developed. These techniques aim to uncouple the information carrying bandwidth from the center frequency by control of the sampling period.

The best known bandpass sampling technique is undersampling (or subsampling). A lesser known one is periodically nonuniform sampling, which as we'll see, is a generalization of undersampling. A particular form, periodically nonuniform sampling of second order (PNS2), is well suited for the needs of advanced SDR platform testing. By choosing the right interpolants

(synthesis filters), generalized undersampling techniques can be employed to shift a bandpass signal to a lower band within the acquisition and conversion speeds of available ADCs. In this way, the signal can be processed at lower cost and using less power. This chapter describes undersampling techniques from the point of view of attractiveness and usefulness in an RF test strategy.

5.2 Nyquist Sampling

The Shannon-Nyquist theorem states that any continuous bandlimited signal can be exactly recovered from a set of sampled values if the sampling frequency is at least twice the signal's highest frequency component. The exact reconstruction formula is given by Shannon [1949]:

$$f(t) = \sum_n f[nT/2]\text{sinc}(2Bt - n) \tag{5.1}$$

where $f[nT/2] = f(t)\Big|_{t=nT/2}$ represent the discrete samples, $B = 1/T$ is the maximal frequency component of the lowpass signal (see Fig. 5.1a) and the $\text{sinc}(t) = \sin(\pi t)/(\pi t)$ interpolant is the time domain representation of an ideal brick-wall lowpass filter. In practice, the interpolant is implemented as a classic lowpass filter and it is introduced to recover the original signal from its samples.

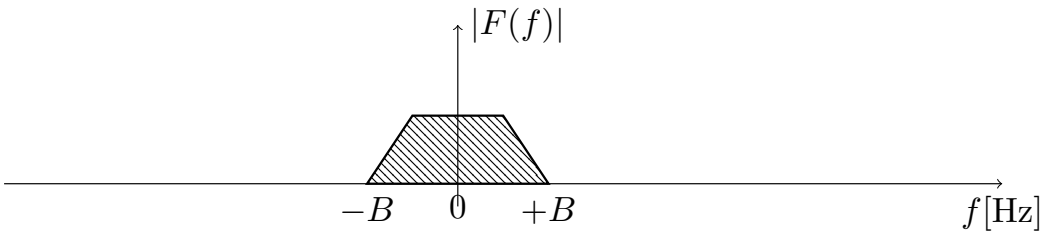
The bandlimited requirement is not strictly speaking a problem, as most signals can be frequency shaped to meet this property to a reasonable degree. In ADC systems this is ensured by the addition of a filter (usually a lowpass filter). The purpose is to reject thermal noise beyond Nyquist frequency as well as other interfering signals, and to avoid aliasing of unwanted frequency component.

When the signal is sampled at a frequency smaller than $2B$ aliasing occurs. The signal aliasing is depicted in the frequency domain in Fig. 5.1. The sampling operation creates replicas of the original spectrum in each Nyquist zone (represented by alternating gray areas in Fig. 5.1b). If the sampling frequency f_s is less than $2B$, then these replicas will overlap and the original signal cannot be uniquely reconstructed anymore. Obviously, when the signal of interest is located around DC (baseband), the occurrence of superposition with replicas of high frequency bands must be avoided. At the least, wideband noise will corrupt the desired baseband component. Thus, the minimum Nyquist frequency is imposed as a need to avoid aliasing.

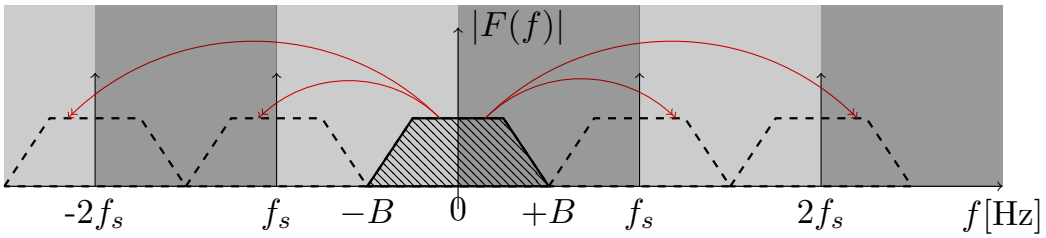
5.3 Bandpass Sampling Techniques

One of the major issues of baseband sampling is that the sampling frequency is related to the signal's highest frequency component and doesn't take into consideration information about signal position and occupied bandwidth. At the same time, modern communications systems almost always deals with sparse signals. For example, let's consider a bandpass signal that occupies a bandwidth of $B = 30$ MHz and is located at $f_c = 2$ GHz . For this signal to be Nyquist sampled, the minimum sampling frequency is $f_s = 2(f_c + B/2) = 4.03$ GHz, which is out of the reach for nearly all existing ADCs [Jonsson, 2010; Walden, 1999], even before considering the dynamic range (ENOB) required at the carrier frequency range. Thus, communications systems always resort to some form of frequency translation, and strive to digitize the signal at a sampling rate that is closer to the bandwidth of the information carrying signal.

One solution is to take advantage of the spectrum replication property to implement what is called bandpass sampling. The mathematical basis of this operation has been known for a



(a) Lowpass signal with a maximal frequency component at $B = 1/T$



(b) Aliasing in lowpass sampling

Figure 5.1: Sampling of a typical baseband signal.

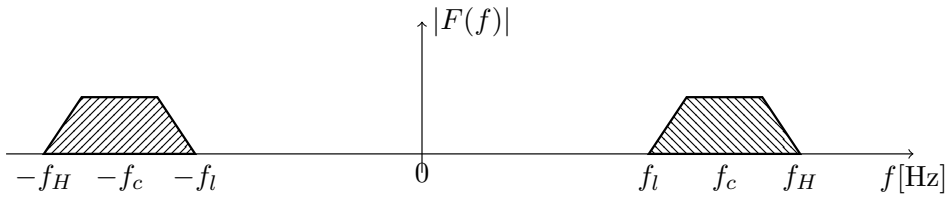


Figure 5.2: A bandpass signal occupying a bandwidth B and located around f_c

long time. Historically, Cauchy seems to have been the first to hypothesize the bandpass sampling requirements [Black, 1953]. Nyquist also alluded to the bandpass case [Nyquist, 1928]. Later, Kohlenberg introduced second order sampling [Kohlenberg, 1953] and provided basic interpolation formula. Afterwards, the idea of bandpass sampling was intensely studied [Vaughan et al., 1991; Lin and Vaidyanathan, 1996; Coulson et al., 1994], and over time, widely applied. Nowadays, bandpass sampling is commonly used in a variety of disciplines such as: radar [Munoz-Ferreras et al., 2013], optics [Bruckstein et al., 1997], biomedical systems [Langet et al., 2012] and general instrumentation such as sampling oscilloscopes.

In this section we are going to discuss both classic undersampling technique and periodical nonuniform sampling of second order. Beforehand, let us define some notions and notations that will be used throughout this report.

A bandpass signal $f(t)$ is defined as a signal whose frequency representation $F(f)$ is limited to the range $f_l < |f| < f_H = f_l + B$ (see Fig. 5.2).

The Fourier Transform and Inverse Fourier Transform will be used in our calculation:

$$F(f) = \int_{-\infty}^{+\infty} f(t)\mathrm{e}^{-i2\pi ft}\mathrm{d}t \tag{5.2a}$$

$$f(t) = \int_{-\infty}^{+\infty} F(f)\mathrm{e}^{i2\pi ft}\mathrm{d}f \tag{5.2b}$$

It will also be convenient to use $*$ as the convolution operator:

$$f(t) * g(t) = \int_{-\infty}^{+\infty} f(\tau)g(t-\tau)\mathrm{d}\tau \tag{5.3}$$

5.3.1 Classic Undersampling

The sampling operation can be regarded in the time domain as a multiplication of the original signal $f(t)$ by a train of uniform impulses:

$$f_{T_s}(t) = f(t) \sum_{n=-\infty}^{+\infty} \delta(t - nT_s) = \sum_{n=-\infty}^{\infty} f(nT_s)\delta(t - nT_s) \tag{5.4}$$

where T_s is the sampling rate, $f_{T_s}(t)$ is the signal sampled at a rate of T_s, and $\delta(t)$ is the Dirac impulse defined by:

$$\delta(t) = \begin{cases} 1 & \text{if } t = 0 \\ 0 & \text{if } t \neq 0 \end{cases}$$

The multiplication in the time domain corresponds to convolution in frequency domain, thus relation 5.4 leads to:

$$F_{T_s}(f) = F(f) * \sum_{n=-\infty}^{\infty} \frac{1}{T_s}\delta(f - n/T_s) = \sum_{n=-\infty}^{\infty} \frac{1}{T_s}F(f - n/T_s) \tag{5.5}$$

We can see from Eq. 5.5 that the spectra of the sampled signal $F_{T_s}(f)$ consists of replicas of the original signal $F(f)$ centered on the spectral lines as illustrated in Fig. 5.3. In order to be able to recover the the signal at the baseband frequency it's evident that the spectral replicas must not superpose (no aliasing).

In effect, the relationship among f_s, signal bandwidth B, and upper range limit f_H is constrained if spectral superposition must be avoided. The feasible combinations must satisfy the following relation:

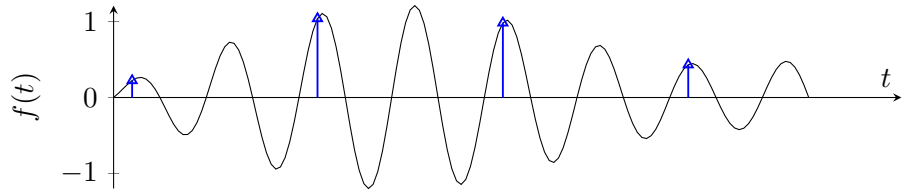
$$\frac{2f_H}{n} \leq f_s \leq \frac{2f_l}{n-1} \tag{5.6a}$$

$$1 \leq n \leq \left\lfloor \frac{f_H}{B} \right\rfloor \tag{5.6b}$$

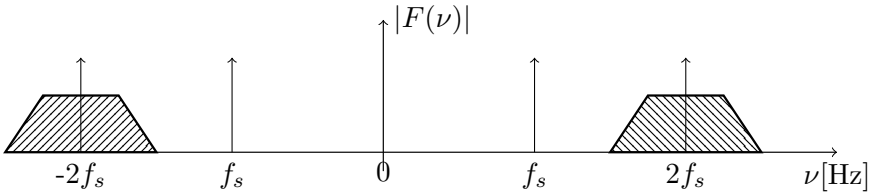
where $\lfloor * \rfloor$ is the floor operator. These constraints are depicted graphically in Fig. 5.4 [Vaughan et al., 1991], where f_s and f_H are normalized w.r.t. the signal bandwidth B. The white regions are the situations where the bandpass sampling will not result in aliasing. The gray regions represent conditions where alias is occurring.

One readily observes that the minimum allowed sampling rate is $f_s = 2B$, as expected, but there is little margin for imperfections in the actual implementation. This sensitivity worsens as f_H/B increases. Therefore, practical implementations of uniform bandpass sampling must sample faster than the theoretical minimum rate and even then, not all faster rates will avoid aliasing, if the signal band is not well positioned.

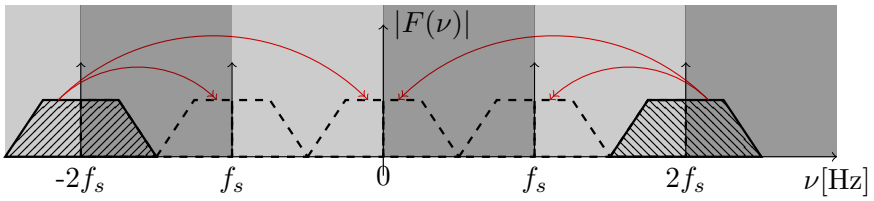
Without loss of generality, let's consider a bandpass signal with $B = 30$ MHz and located at $f_l = 2$ GHz. For this example the acceptable sample rates are within the white areas in Fig. 5.4b. If a sampling rate around the ideal minimum value $2B$ is desired, the subsampling



(a) Time domain representation of undersampling



(b) Spectral (frequency domain) view of signal $f(t)$ and impulse sampling operation.



(c)

Figure 5.3: Graphical representation of spectral replication of undersampling.

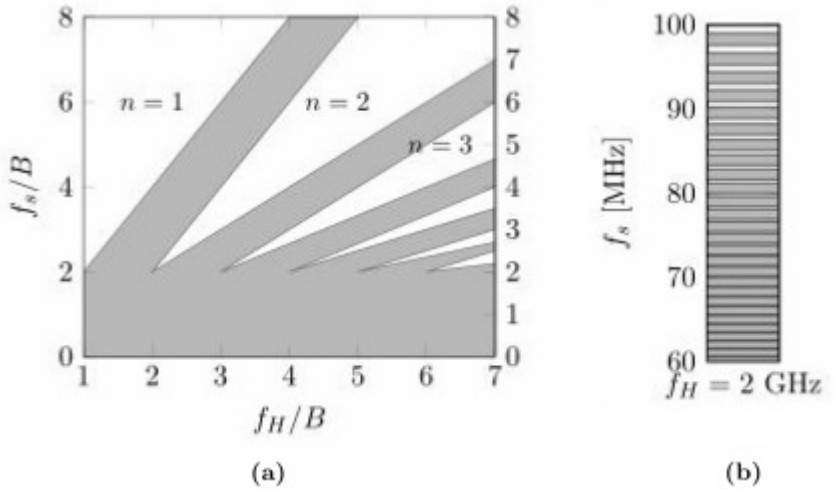


Figure 5.4: The constraints on the sampling rate f_s for undersampling [Vaughan et al., 1991]: 5.4a in general case and 5.4b a particular case where $f_H = 2.03$ GHz and $B = 30$ MHz. The white regions are situations where the undersampling will not result in aliasing. The gray regions represent conditions where alias is occurring.

clock should have a precision of few KHz in order to avoid aliasing. The most obvious solution to relax these constraints is to use guards bands (which is equivalent to sampling at nonminimum rates [Vaughan et al., 1991]). Even so, as shown in Fig. 5.4b, the sampling around $f_s = 90$ MHz (50% larger than $2B$) would still require sampling precision of few hundreds of KHz.

To sum up, uniform bandpass sampling is effective, but difficult to implement without incurring aliasing problems as the ratio f_H/B rises.

5.3.2 Periodical Nonuniform Sampling of Second Order (PNS2)

The discussions above suggest that the classic undersampling technique is not well suited for test of software radios due to the lack of flexibility. Indeed, one of the most important characteristics of a software radio is its flexibility. That means that it is capable to operate over a wide range of operating parameters (frequency, data rate, modulation type, etc.). A well designed test strategy should be able to cover all of these configurations, with minimum of effort and extra circuitry. This is hardly the case for an undersampling implementation, which would require adjustable and precise sampling rates.

Kohlenberg [1953] has shown that if two sets uniform samples are used, a bandpass signal can be sampled at the minimum Nyquist rate $2B$ (in the form of an average rate) independent of the signal position. This technique became known as Periodically Nonuniform Sampling of Second Order (PNS2). Further results on this technique were given in Lin and Vaidyanathan [1996] and Vaughan et al. [1991].

The time domain representation of PNS2 is depicted in Fig. 5.6. Let's denote by $f_A(t)$ and $f_B(t)$ the two sets of sampled functions:

$$\begin{aligned} f_A(t) &= \sum_n f[nT]\delta(t-nT) \\ f_B(t) &= \sum_n f[nT+D]\delta(t-nT-D) \end{aligned} \tag{5.7}$$

where D is the phase (time) delay between the sets of samples. We consider the sampling is done at the minimum Nyquist rate $2B$ (or B for each channel). The corresponding spectra are given by:

$$\begin{aligned} F_A(f) &= F(f) * \sum_n B\delta(f-nB) \\ F_B(f) &= F(f) * \sum_n B\mathrm{e}^{-j2\pi BDn}\delta(f-nB) \end{aligned} \tag{5.8}$$

and are depicted graphically in Fig. 5.5a and Fig. 5.5b, respectively. For improved clarity, the top figure shows only the positive frequency components resulting from sampling, while the bottom figure depicts only the negative frequency. First, it is important to note that both sets of sampled signals are affected by the aliasing and the original signal cannot be recovered. Nonetheless, if the spectra are combined through the means of two interpolants we can show that the original signal (the blue spectrum in Fig. 5.5d) or baseband shifted version (the red spectrum in Fig. 5.5d) can be reconstructed. In the following we discuss how the interpolants can be obtained in the two cases.

5.3.2.1 Signal Reconstruction Using PNS2

Let's now investigate how the two interpolants, $S_A(f)$ and $S_B(f)$, designed to restore the original signal, can be obtained. This problem can be defined as a problem of finding the two interpolants $S_A(f)$ and $S_B(f)$ for which the relation 5.9 holds:

$$F(f) = F_A(f)S_A(f) + F_B(f)S_B(f),\ f_l < f < f_H \tag{5.9}$$

and it is easier to formulate and solve in the frequency domain.

If we designate the positive and negative-frequency parts of $F(f)$ by $F_+(f)$ and $F_-(f)$ as depicted graphically in Fig. 5.5b and Fig. 5.5c one has in the interval $f_l < f < f_H$:

$$\begin{aligned} F_A(f) &= \begin{cases} BF_+(f) + BF_-(f + 2f_l - kB) & \text{if } f_l < f < kB - f_l \\ BF_+(f) + BF_-(f + 2f_l - k^+B) & \text{if } kB - f_l < f < f_l + B \end{cases} \\ F_B(f) &= \begin{cases} BF_+(f) + B\gamma^k F_-(f + 2f_l - kB) & \text{if } f_l < f < kB - f_l \\ BF_+(f) + B\gamma^{k^+} F_-(f + 2f_l - k^+B) & \text{if } kB - f_l < f < f_l + B \end{cases} \end{aligned} \tag{5.10}$$

where $\gamma = \mathrm{e}^{-j2\pi BD}$, k depends on the signal position $k = \lceil 2f_l/B \rceil$ and $k^+ = k+1$. Substituting this into Eq. 5.9, one obtains:

$$F(f) = \begin{cases} \left(BF_+(f) + BF_-(f + 2f_l - kB)\right) S_A(f) + \left(BF_+(f) + B\gamma^k F_-(f + 2f_l - kB)\right) S_B(f) \\ \qquad\qquad \text{if } f_l < f < kB - f_l \\ \left(BF_+(f) + BF_-(f + 2f_l - k^+B)\right) S_A(f) + \left(BF_+(f) + B\gamma^{k^+} F_-(f + 2f_l - k^+B)\right) S_B(f) \\ \qquad\qquad \text{if } kB - f_l < f < f_l + B \end{cases} \tag{5.11}$$

or after several manipulations:

$$\begin{aligned} F_+(f)\left[BS_A(f) + BS_B(f) - 1\right] + F_-(f + 2f_l - kB)\left[BS_A(f) + B\gamma^k S_B(f)\right] &= 0 \\ \text{if } f_l < f < kB - f_l & \\ F_+(f)\left[BS_A(f) + BS_B(f) - 1\right] + F_-(f + 2f_l - k^+B)\left[BS_A(f) + B\gamma^{k^+} S_B(f)\right] &= 0 \\ \text{if } kB - f_l < f < f_l + B & \end{aligned} \tag{5.12}$$

Since, in the general case there is no analytic relationship between $F_+(f)$ and $F_-(f + 2f_l - kB)$ or between $F_+(f)$ and $F_-(f + 2f_l - k^+B)$ one obtains the following systems of equations:

$$\begin{cases} BS_A(f) + BS_B(f) = 1 \\ BS_A(f) + B\gamma^k S_B(f) = 0 \end{cases} \quad f_l < f < kB - f_l \tag{5.13a}$$

$$\begin{cases} BS_A(f) + BS_B(f) = 1 \\ BS_A(f) + B\gamma^{k^+} S_B(f) = 0 \end{cases} \quad kB - f_l < f < f_l + B \tag{5.13b}$$

which yields a unique solution:

$$S_A(f) = \begin{cases} \dfrac{T}{1 - \gamma^k} & f_l < f < kB - f_l \\ \dfrac{T}{1 - \gamma^{k^+}} & kB - f_l < f < f_l + B \\ 0 & \text{otherwise} \end{cases} \tag{5.14a}$$

$$S_A(-f) = S_A^*(f) \tag{5.14b}$$

$$S_B(f) = S_A(-f) \tag{5.14c}$$

In the time domain, Eq. 5.9 can be expressed as a convolution:

$$\begin{aligned} f(t) &= s_A(t) * f_A(t) + s_B(t) * f_B(t) \\ &= \sum_{n=-\infty}^{+\infty} \left[f[nT]s_A(t - nT) + f[nT + D]s_B(t - nT - D)\right] \end{aligned} \tag{5.15}$$

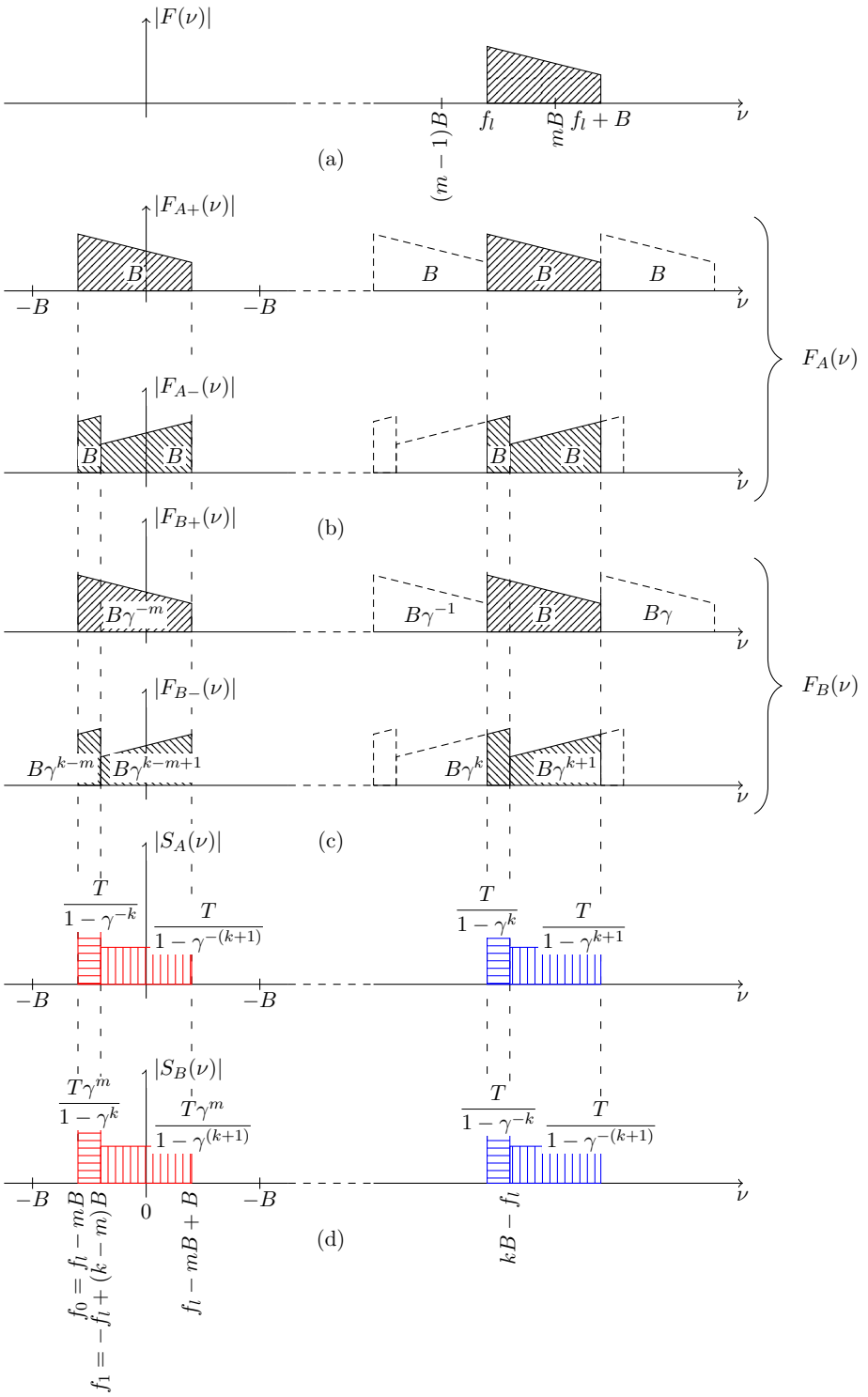


Figure 5.5: Periodically nonuniform bandpass sampling of second order. Fig. 5.5a represents the original passband signal to be reconstructed. Fig 5.5b sketches the spectrum $F_A(\nu)$ resulting from sampling by the sample set A. The top figure shows only the positive frequency components $F_{A+}(\nu)$ resulting from sampling, while the bottom figure shows only the negative frequency components $F_{A-}(\nu)$. The spectra of the set B is depicted as $F_{B+}(\nu)$ and $F_{B-}(\nu)$ in Fig. 5.5c. $S_A(\nu)$ and $S_B(\nu)$ in Fig. 5.5d represent the interpolants (reconstructing filters) which are designed to restore the original signal.

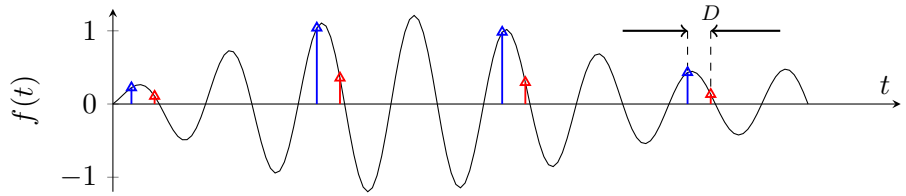


Figure 5.6: Time domain representation of PNS2 operation

Using the Inverse Fourier Transform (IFT), the time domain representation of the two interpolants can be derived from Eq. 5.14 as:

$$s_A(t) = \int_{-\infty}^{\infty} S_A(f) \mathrm{e}^{j2\pi ft} \mathrm{d}f$$

or after several manipulations

$$\begin{aligned} s_A(t) &= \frac{\cos[2\pi(kB - f_l)t - k\pi BD] - \cos[2\pi f_l t - k\pi BD]}{2\pi Bt \sin k\pi BD} + \\ &+ \frac{\cos[2\pi(f_l + B)t - k^+\pi BD] - \cos[2\pi(kB - f_l)t - k^+\pi BD]}{2\pi Bt \sin k^+\pi BD} \end{aligned} \tag{5.16a}$$

$$s_B(t) = s_A(-t) \tag{5.16b}$$

As we can see, the two interpolants, s_A and s_B, designed to implement PNS2 reconstruction are real functions (of time) that resemble a passband sinc function and depend on the signal position (through f_l and k), signal bandwidth, B and the delay D. Of particular interest is the influence of the D on the interpolants values. This influence and further considerations are discussed in greater details in the next Chapter. Here we present some general remarks. Indeed, Eq. 5.15 and Eq. 5.16 are valid provided that D meets the following constraints:

$$D \neq nT/k \tag{5.17a}$$

$$D \neq nT/(k+1), \forall n \in \mathbb{N} \tag{5.17b}$$

If D assumes values which violate the conditions 5.17 then the reconstruction filter becomes unstable. There are no other constraints for the choice of D, but as we will see later, the implementation cost (in terms of number of bits and filter length) of PNS2 reconstruction is directly affected by D.

5.3.2.2 Frequency Shifting Using PNS2

The interpolants from Eq. 5.16 were constructed to recover the original signal. However, the repetitive nature of the spectra $F_A(f)$ and $F_B(f)$ from Fig. 5.5 offers the possibility to recover not only the original function, but a frequency-translated version of it. In our case, the most useful option is to recover the baseband translated version $f_{bb}(t)$ of the original signal (see the red spectrum in Fig. 5.5d). This choice will allow signal conversion at minimum rates.

In this section we show how the interpolants that allow the reconstruction of $f_{bb}(t)$ may be computed. The procedure is similar to that leading to Eq. 5.16. The new problem can be defined as a problem of finding two interpolants $S_A^{bb}(f)$ and $S_B^{bb}(f)$ for which the relation 5.18 holds:

$$F_{bb}(f) = F_A(f)S_A^{bb}(f) + F_B(f)S_B^{bb}(f), \;\; f_0 < f < f_0 + B \tag{5.18}$$

where $f_0 = f_l - mB$ represents the baseband new signal position and $m = \lceil f_l/B \rceil$ is directly related to the signal passband position.

Following the same reasoning as before, the following results are derived and indicated in Fig. 5.5d in red:

$$S_A^{bb}(\nu) = \begin{cases} \dfrac{T}{1-\gamma^{-k}} & \text{if } f_0 < f < f_1 \\ \dfrac{T}{1-\gamma^{-k^+}} & \text{if } f_1 < f < f_0 + B \\ 0 & \text{otherwise} \end{cases} \tag{5.19a}$$

$$S_B^{bb}(\nu) = \begin{cases} \dfrac{T\gamma^m}{1-\gamma^{k}} & \text{if } f_0 < f < f_1 \\ \dfrac{T\gamma^m}{1-\gamma^{k^+}} & \text{if } f_1 < f < f_0 + B \\ 0 & \text{otherwise} \end{cases} \tag{5.19b}$$

In time domain Eq. 5.18 can be expressed as a convolution:

$$\begin{aligned} f_{bb}(t) &= s_A^{bb}(t) * f_A(t) + s_B^{bb}(t) * f_B(t) \\ &= \sum_{n=-\infty}^{+\infty} \Big[f[nT] s_A^{bb}(t-nT) + f[nT+D] s_B^{bb}(t-nT-D) \Big] \end{aligned} \tag{5.20}$$

The time domain interpolants are obtained by applying an IFT to the frequency responses in Eq. 5.19:

$$s_A^{bb}(t) = \frac{e^{-j\pi BDk}(e^{j2\pi f_1 t} - e^{j2\pi f_0 t})}{2\pi Bt \sin \pi BDk} + \frac{e^{-j\pi BDk^+}(e^{j2\pi (f_0+B) t} - e^{j2\pi f_1 t})}{2\pi Bt \sin \pi BDk^+} \tag{5.21a}$$

$$s_B^{bb}(t) = - s_A^{bb}(t) e^{-j2\pi BD(k-m)} \tag{5.21b}$$

As one can notice the interpolants in Eq. 5.21 are similar to the ones in Eq. 5.16. The constraints of Eq. 5.17 also apply to Eq. 5.20. The most significant difference between the interpolants from Eq. 5.21 and the ones from Eq. 5.16 is that the baseband interpolants are complex while the original interpolants are real. As will see in the next chapter, this aspect will raise the computing cost for the actual implementation.

5.3.3 Noise Degradation in Undersampling Techniques

In this section we discuss the effects of some of the most difficult issues in any undersampling architecture: wideband noise folding and clock jitter. When available, we present also the solutions that can be used to surpass these limitations.

5.3.3.1 Aliasing Effect

One of the most difficult issues in any undersampling architecture is the Signal-to-Noise Ratio (SNR) degradation. Because of the periodicity of the sampled signal the wideband noise will be folded in each Nyquist zone. Therefore, when applying bandpass sampling to shift a bandpass signal to a lowpass position, the SNR will be poorer w.r.t. the SNR of an equivalent frequency translating analog system (i.e. a mixer with filters), in which the SNR is unaffected, at least potentially.

Let's consider a bandpass signal of spectral power density S, in-band noise of N_i, and out-of-band noise power density N_o. The analog SNR is given by $SNR = S/N_i$. After sampling

the SNR will be degraded by at least the noise aliased from the bands between DC and the passband, as given in Vaughan et al. [1991]:

$$SNR_T = \frac{S}{N_i + (k-1)N_o} \tag{5.22}$$

where k is related to the ratio of the signal position f_c to the sampling rate f_s (see Eq. 5.10, $k = \lceil 2f_l/B \rceil$). When $N_i >> N_o$ the SNR is already limited before sampling. However, if $N_i \approx N_o$, then the degradation of the SNR can be estimated by:

$$D_{SNR}[\text{dB}] = 10\log_{10} k \tag{5.23}$$

For example, the SNR of a baseband signal located at $f_l = 2$ GHz and subsampled at sampling rate $f_s = 100$ MHz will be degraded by at least $10\log_{10}(2 \cdot 100\text{e}6/2\text{e}9) = 10$ dB. In order to limit this SNR degradation, in many cases a passband filter is added. This runs counter to our objective of wideband operation.

5.3.3.2 Clock-Jitter Considerations

The sampling instant in the undersampling circuit is controlled by the sampling clock. Although the sampling period T, is usually considered as constant in the system, this is not the situation in practice. The sampling period has time variations caused by the uncertain sampling clock (jitter), or the sampling switch that does not open or close in the precise time instance (aperture jitter). This jitter is responsible for SNR degradation.

Commonly, the clock jitter is modeled as additive Gaussian distributed noise. Let's consider τ_J the standard deviation of the combined clock jitter [rms] that affects a subsampling circuit. The SNR degradation expected in this condition is given by the following relation [Fudge et al., 2013; Sun and Signell, 2004; Kiyono et al., 2004]:

$$D_{SNR_{Jitter}}[\text{dB}] = 10\log_{10}(2\pi f_c \tau_J)^2 \tag{5.24}$$

Eq. 5.24 shows that the sample clock jitter results in SNR degradation that increases log linearly with RF signal frequency. In RF subsampling, where the input signal frequency is very high, the sampling jitter is one of the major sources of noise in the sampled signals.

To reduce the jitter induced noise in practical applications that use subsampling, a clock generator with low jitter is needed. However, a low jitter clock is not always available. As result, several attempts to mitigate the jitter noise have been developed. A first class of this methods relies on injecting a known reference into the signal path [Rutten et al., 2008; Zhao et al., 2012]. The jitter information can be estimated from the sampled output and then used to compensate the wanted signal. Although these methods can effectively reduce the jitter, they are very complicated to implement in hardware and require additional overhead.

Another approach to mitigate the introduced noise consists on rethinking the sampler block. Indeed, it has been shown that, if the classic Sample&Hold stage is replaced by a charge integrating sampler the subsampling robustness w.r.t. the jitter is greatly improved [Yuan, 2000; Carley and Mukherjee, 1995; Poberezhskiy and Poberezhskiy, 2007]. Furthermore, the proposed improvement has a simpler hardware implementation which makes it ideal for its use for a test strategy. Thus we decided to employ this technique in our strategy. The charged-based sampling technique is discussed in more details in the next chapter.

5.4 Conclusions

In this chapter we described two subsampling techniques designed to recover/frequency-shift a passband signal at a sampling rate related to the signal bandwidth and independent of signal position. We discussed classic undersampling and we saw that its limited flexibility is not suitable for a non-intrusive SDR test strategy. Afterwards, we presented a more generalized undersampling technique, Periodically Nonuniform Sampling of Second Order (PNS2), that uses two set of uniform samples and avoids some of the limitations of classic undersampling. We showed how the two interpolants (reconstruction filters) are derived. Finally, we evoked one of the most undesirable effects in any undersampling technique: the folding of the wideband noise that will cause degradation of the SNR. We presented a formula that can give a rough estimation of the SNR degradation.

Given these theoretical results, it appears that PNS2 is an attractive choice for implementation of a loopback strategy for SDR platforms, since one can translate any signal band to baseband, by adjusting the delay between two phases at the same fixed frequency. There remains a number of implementation problems to be solved, which are treated in the next chapter.

Chapter 6

SDR Test Architecture Based on Nonuniform Subsampling

Contents

6.1 Introduction

In the previous chapters we have shown the sophisticated communication architectures found in SDR platforms and we have discussed the implications of this for the test strategy. Afterwards,

we evaluated RF test strategies in order to determine the most promising ones for production and in-field test of SDRs. Amongst the published techniques, the loopback BIST stood out as the most-likely answer to our needs. However, loopback BIST approach is subject to the fault-masking problem that will provoke reduction of the test performance (in terms of yield loss and fault coverage). In this chapter we introduce a novel RF loopback BIST architecture that is designed to avoid fault-masking and enable fully testing of SDR transceivers.

The overall idea of the proposed test strategy is to first test the TX in loopback manner, but not using the yet untested main RX channel to recover the output signal. Instead, our proposal uses relatively simple BIST circuitry to subsample the TX output and feed it to the DSP using the two RX ADCs. Our initial efforts are focused on the characterization of the TX chain with respect to compliance to the spectral mask, the most vexing post-manufacture test issue for tactical radio units. The bandpass conversion of the output stage waveforms using nonuniform sampling allow us to surmount this problem. This approach is scalable across a wide range of complex specifications without incurring additional hardware or performance cost.

From the point of view of SDR units, the most prominent advantage of PNS2 w.r.t. traditional undersampling band translation is the relaxation of the constraints on the sample rates as depicted in Fig. 5.4. Indeed, as already observed, that for traditional undersampling, the acceptable sampling rates are constrained (Fig. 5.4a), in order to avoid aliasing. This restriction on signal band does not exist for PNS2 (Fig. 5.4b) where the bandpass signal can be recovered anywhere within the full extent of the Nyquist frequency interval independent of the signal position. This mathematical property was worked out into a practical BIST architecture, with added features to address practical obstacles. However, for a correct PNS2 reconstruction, it is assumed that the output waveform of the TX is shaped by a bandpass filter that is functional, i.e. the RF signal is limited to a roughly defined frequency range. This assumption is realistic, and does not impose any new constraints on the TX architecture, as some form of bandpass filtering is always present just ahead of the antenna.

Our efforts are fueled by the new challenges posed by the very nature of SDR platforms for established product test protocols. It's hardly feasible to continue measuring simple parametrics and then try to correlate these characteristics to ultimate system performance for all possible waveforms, protocols and modes of operation. Issues such as gain, noise figure, third-order intercept point remain useful designer metrics, but what really counts in the field is that the radio functions reliably and is not a source of spurious emissions. Further complicating matters, cutting-edge radios support new multiple-in-multiple-out (MIMO) techniques, which allow antennae to process many incoming and outgoing signals simultaneously. Effective verification of these systems will require true duplex-functional radio tests. At a minimum, the test protocol for SDR platforms must include :

- Adjacent channel power ratio (ACPR) (also known as adjacent channel leakage ratio (ACLR)): the ratio of transmitted power to power in the adjacent radio channel
- BER : Bit Error Rate
- Error vector magnitude (EVM)

Our proposed BIST scheme aims to check ACPR TX compliance, which is rarely addressed by existing BIST techniques due to the complexity of the measurement. Nonetheless, it can also handle less demanding measurements, such as IP3, gain, I/Q imbalance without any hardware modifications, using existing signal processing algorithms.

The key advantages of our proposed strategy are:

- flexibility over a wide range of operating modes. In effect, the PNS2-based BIST strategy is able to characterize the TX across all frequency bands simply by updating the coefficients of two digital filters, as we'll see in the following.

- minimum of extra hardware requirements. In the best case, only a digitally controlled delay element and two FIR filters are needed.

- removes fault-masking prior to loopback test of RX because it allows complete characterization of the TX channel.

Our proposed architecture can also be advantageously applied in TX architectures that use RF output performance estimation to carry-out pre-distortion compensation to improve power amplifier (PA) linearity.

The main contribution of this research consists in proposing a practical loopback-BIST architecture based on periodical nonuniform bandpass sampling, PNS2, that allows testing the SDR TX for any mode of operation and architecture. Our final intent is to release RF loopback BIST from the yoke of fault masking, hence clearing the way to a full compliance in-field test of tactical radio-units.

In this chapter we introduce and discuss the proposed test strategy. We start by giving a general description and some details on the implementations. Next, we discuss the most important limitations and how they can be addressed. Finally, we present the results obtained through simulation.

The results of this research have been published and presented in Dogaru et al. [2013a,b, 2014].

6.2 General Description of the Proposed Test Architecture

The block diagram of the proposed TX BIST architecture is presented in Fig. 6.1. The key idea is to use an alternate loopback path to observe the transmitter output signal just ahead of the antenna. The output waveform is routed back into the last stage of the main receiver chain (the analog-digital converters, ADCs), by using a small amount of analog circuitry, some digital control of clock delays, and a lot of complex signal processing. In effect, an auxiliary subsampling receiver (auRX) based on PNS2 provides an alternate demodulation path to characterize the main TX. This is feasible because the demodulation channel requirements in TX test mode are somewhat less stringent (i.e. no blockers) than during normal radio use.

The red blocks in Fig. 6.1 are the modifications required to implement the test path within the transceiver. They are the realization of the PNS2 technique described in the previous chapter. Our basic assumption is that the SDR unit itself contains all the other blocks, and that they can be harnessed for test purposes. Thus, we reuse as many available resources as possible (RX ADCs, DSP, GPP) in order to implement the PNS2 loopback BIST architecture.

The block diagram of the entire PNS2 architecture is presented in Fig. 6.2. The RF signal at the output of the SDR TX $f(t)$ is fed into two identical samplers driven separately. The Delay Controlled Delay Element (DCDE) block introduces a controlled delay D between the two sampling clocks. The two complex coefficients FIR filters provide real-time implementation of the Eq. 6.1 and Eq. 6.2. The fast Sample and Hold (S/H) blocks are needed in order to raise the tracking speed and sampling aperture performance of the ADCs to the levels of the RF carrier frequency. The conversion rate of these two baseband ADCs remains unaffected.

Thus, the PNS2 subsampler architecture consists of three fundamental blocks:

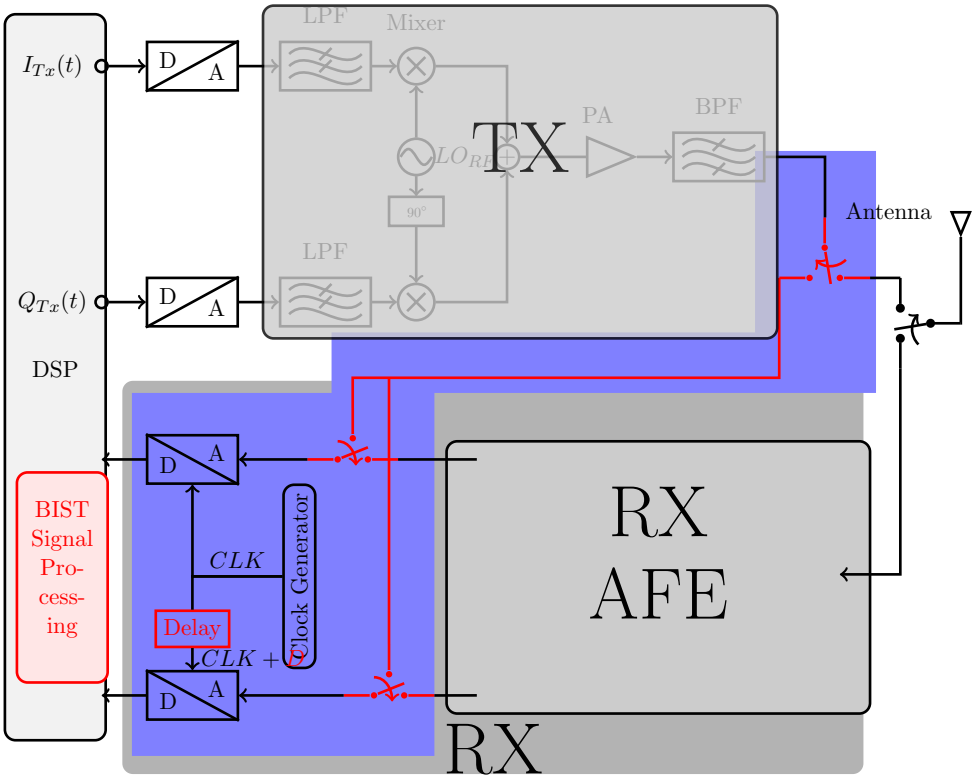


Figure 6.1: Block diagram of the proposed BIST architecture. The red blocks are the modification required to implement the loopback circuitry within the transceiver to enable self-test

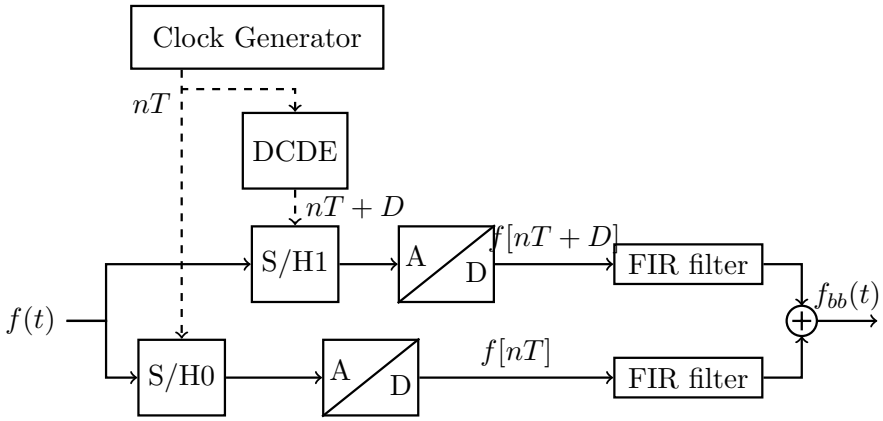


Figure 6.2: Complete block diagram of the proposed BIST architecture

- **PNS2 digital reconstruction block** is represented by two complex coefficients FIR filters whose coefficients are calculated to implement PNS2 reconstruction. This step can also be carried out externally by some auxiliary equipments. However, we have determined that reconstruction is feasible using only two FIR filters with complex coefficients, making it worthwhile to pursue an on-board (standalone) implementation. Further details on how to derive the filters coefficients and on the associated computational effort are presented in Section 6.3.

- **Delay generation block, (DCDE)**: a variable delay block that provides a relatively high resolution time delay. This topic is discussed in details in Section 6.4

- **Sampling blocks** the most sensitive and thus, challenging to design. The purpose of this block is to realize the sampling operation. The PNS2 sampling process and its limitations are discussed in Section 6.5

We will describe each one of this block in details in the succeeding sections. We will show what are the main difficulties and give solutions on how to surpass them.

6.3 Digital PNS2 Reconstruction

As we discussed in the previous section the heart of our new loopback BIST technique is PNS2 sampling and reconstruction. Here we investigate the possibility to implement digitally PNS2 reconstruction. Our final goal is to implement PNS2 sampling and reconstruction while reusing as much as possible the resources available on the DUT. Indeed, we shall show that PNS2 reconstruction is feasible using only two FIR filters with complex coefficients.

First, let's recall the idea of PNS2. A continuous band limited function $f(t)$ can be reconstructed at baseband position from two sets of uniform sets of uniform samples $f[nT]$ and $f[nT + D]$ (see Fig. 5.6) using the formula derived in Eq. 5.20 and resumed in the following for convenience:

$$f_{bb}(t) = \sum_{n=-\infty}^{+\infty} \Big[f[nT] s_A^{bb}(t - nT) + f[nT + D] s_B^{bb}(t - nT - D) \Big] \tag{6.1}$$

where D represents the time delay between two samples and s_A^{bb} and s_B^{bb} are two complex

coefficients interpolants defined by:

$$s_A^{bb}(t) = \frac{e^{-j\pi BDk}(e^{j2\pi f_1 t} - e^{j2\pi f_0 t})}{2\pi Bt \sin \pi BDk} + \frac{e^{-j\pi BDk^+}(e^{j2\pi (f_0+B)t} - e^{j2\pi f_1 t})}{2\pi Bt \sin \pi BDk^+} \tag{6.2a}$$

$$s_B^{bb}(t) = -s_A^{bb}(t) e^{-j2\pi BD(k-m)} \tag{6.2b}$$

$$k = \left\lceil \frac{2f_l}{B} \right\rceil, k^+ = k+1, m = \left\lceil \frac{f_l}{B} \right\rceil \tag{6.2c}$$

As we can see, the two interpolants, s_A^{bb} and s_B^{bb}, designed to implement PNS2 baseband shifting and reconstruction are complex time functions that depend on the signal position (through f_l, k and m), signal bandwidth, B and the delay D. Their practical implementation in digital domain is described in the following section.

6.3.1 FIR Implementation

Let's now suppose that the RF signal $f(t)$ was accurately sampled and the samples $f[nT]$ and $f[nT+D]$ are available. We are now looking for a solution to implement the interpolants s_A^{bb} and s_B^{bb} in Eq. 6.2 in digital domain. A quick analysis of the form of Eq. 6.1 indicates the simplest approach is based on implementing the equations using FIR filters with complex coefficients.

The time-continuous interpolants could be implemented at the theoretical minimum sampling rate (on average) of $2B$. Unfortunately, in the general case, the discretization of these interpolants cannot be done at the minimum sampling-rate without causing aliasing. In fact, it can be readily observed from the geometrical representation in Fig. 5.5d that the signal of interest occupy a band of B Hz, and lies somewhere between $-B$ and B, depending on the original signal position. Therefore, to preclude aliasing, the baseband signal must be oversampled by a minimum factor of two. Considering this and the Eq. 6.2, the FIR filters can be expressed as:

$$f_{bb}[iT/2+\delta] = \sum_{n=-n_w/2}^{n_w/2} f[(i-n)T/2] s_A^{bb}[nT/2+\delta] + f[(i-n)T/2+D] s_B^{bb}[nT/2+\delta-D] \quad \forall i \in \mathbb{N}, i > n_w/2 \tag{6.3}$$

where $\delta \in [0, T/2]$ can be arbitrarily chosen. Eq. 6.3 is explained graphically in Fig. 6.3, where the blue signal represent the RF signal to be sampled, $f(t)$, and the red signal, $f_{bb}(t)$, represents its baseband shifted version to be reconstructed. One can notice that the two FIRs filters taps, $s_A^{bb}[nT/2+\delta]$ and $s_B^{bb}[nT/2+\delta-D]$, do not depend on i thus PNS2 reconstruction can be implemented using constant coefficients FIR filters.

The FIR taps in Eq. 6.3 were obtained by truncating the continuous-time interpolants 6.2. In this context, truncating means choosing a finite number (n_w+1) of coefficients. In order to minimize the effects of truncation, a window function should be applied to the coefficients. In our work we have chosen a Kaiser window.

6.3.2 Kaiser Window

The Kaiser window is a family of window functions fully adjustable using a single parameter β. The Kaiser window is useful because it provides a solution to achieve any desired side lobe size and accordingly any desired stopband attenuation for the filter response. Moreover, the order n_w can be adjusted to obtain the desired width of the transition band. By setting all of these parameters, the Kaiser window provides a flexible tool to design a practical implementation

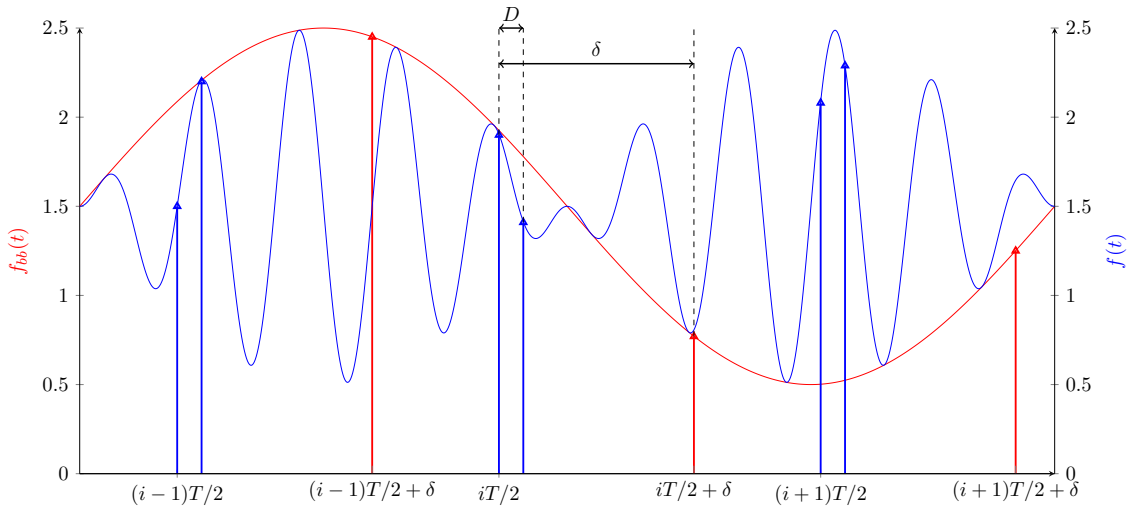


Figure 6.3: Graphical representation of the sampling process for digital PNS2 reconstruction

for the ideal filters in Fig.5.5d. The Kaiser window was preferred to the rectangular window because the last one minimizes the width of the main lobe without any regard to the side lobe.

The Kaiser window is given by [Farhang-Boroujeny, 2009]:

$$v[n] = \begin{cases} I_0\left(\beta\sqrt{1-(2n/n_w)^2}\right)/(I_0(\beta)), & -\frac{n_w}{2} \leq n \leq \frac{n_w}{2} \\ 0, & \text{otherwise} \end{cases} \tag{6.4}$$

where $I_0(x)$ is the modified zeroth order Bessel function:

$$I_0(x) = 1 + \sum_{k=1}^{\infty}\left[\frac{(x/2)^k}{k!}\right]^2 \tag{6.5}$$

The following simple formula can be used to determine the value of β for a minimum stopband attenuation α dB.

$$\beta = \begin{cases} 0.1102(\alpha - 8.7), & \alpha > 50 \\ 0.5842(\alpha-21)^{0.4} + 0.07886(\alpha-21), & 21 \leq \alpha < 50 \\ 0, & \alpha < 21 \end{cases} \tag{6.6}$$

Also, to achieve a transition width of Δf, one should choose :

$$N \approx \frac{\alpha - 7.95}{14.36\Delta f} \tag{6.7}$$

After applying the Kaiser window, the interpolants coefficients in Eq. 6.3 become:

$$s_A^{bb}[\cdot] = v[n] \cdot s_A^{bb}[\cdot] \tag{6.8a}$$
$$s_B^{bb}[\cdot] = v[n] \cdot s_B^{bb}[\cdot] \tag{6.8b}$$

In our simulations, we noticed that $\alpha = 60$ dB of stopband attenuation gives satisfactory results. Similarly, good results were obtained for n_w varying within the interval: $n_w \in [20, 30]$. These results are presented in Section 6.6.

6.3.3 Alternatives & Other Considerations

Alternatively to Kaiser windowing, one could adopt a conceptually different approach, as proposed in Johansson and Lowenborg [2006]. There, the reconstruction issue is posed as a filter bank design problem. The filters coefficients are analytically obtained using least-squares formulation. One of the advantages of this alternate approach would be that it allows one to choose the level of approximation error with respect to the length of the filter through the optimization criterion. We did not pursue this method because our previous (simpler) method resulted in filter coefficients that yielded good results.

Even if the theoretical minimum sampling rate for PNS2 is $2B$, we have shown that for a practical digital implementation the original signal must be oversampled by a factor of two (i.e. $4B$ for the overall system or $2B$ for each of the ADC). Interestingly, digital implementations using minimum-rate sampling are possible in few particular cases: when the signal is integer positioned ($f_l = nB + B/2, n \in \mathbb{N}$) or half-integer positioned ($f_l = nB, n \in \mathbb{N}$). These cases are treated in Linden [1959]. In these situations, the practical implementation is simplified and the cost is reduced. Depending on the level of flexibility required by the test technique and on the available digital resources, one could choose either to implement the general PNS2-based sampling and reconstruction adopted by us and presented in this section or to go with the simplified version.

Finally, examining Fig. 5.5, one can observe that the baseband-shifted signal is not centered around DC (0 Hz), but around $f_l - mB + B/2$. A digital frequency-shifting could be considered but, here our objective is spectral mask estimation. Hence, this feature isn't warranted and it will not be further discussed.

6.4 Delay Generation Block

We concluded that a digital implementation of the PNS2 reconstruction is possible as long as the necessary samples are available. In this section we analyze the delay generation block: the Digitally Controlled Delay Element (DCDE). The DCDE shown in Fig. 6.2 is designed to delay one of the path by D in order to create the second set of samples $f[nT + D]$ needed for PNS2 reconstruction. Before analyzing a possible implementation of this block we discuss first the constraints and the specifications that should be met. Afterwards, we present some novel solutions to surpass the main difficulties related to this block.

6.4.1 Choice of D

One can notice from Eq. 6.1 and Eq. 6.2 that the choice of D affects the two interpolants s_A^{bb} and s_B^{bb}. In fact, relation 6.1 is valid provided that D meets the following constraints:

$$D \neq nT/k \tag{6.9a}$$

$$D \neq nT/(k+1), \forall n \in \mathbb{N} \tag{6.9b}$$

where $k = \left\lceil \frac{2f_l}{B} \right\rceil$ is related to the signal frequency position. If D assumes values which violate the conditions 6.9 then the reconstruction filter becomes unstable (the denominator of one of the terms in Eq. 6.2 will equal to 0). One can observe that if D approaches the right-hand values given in Eq. 6.9, the coefficients of the reconstruction interpolants rise progressively toward infinity. Unduly large values complicate the practical realization, since more terms will have significant values and will have to be computed.

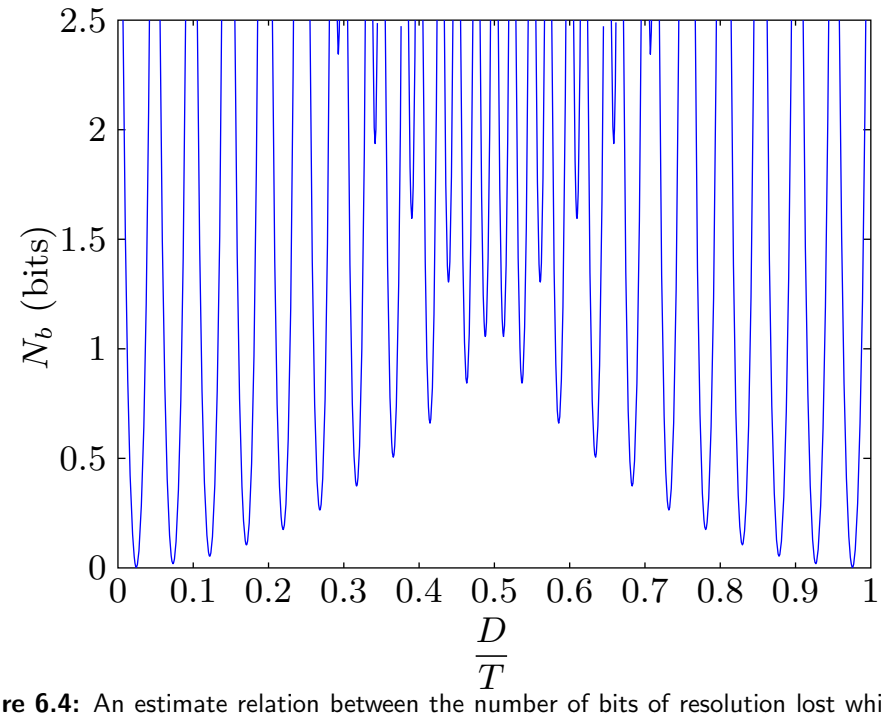


Figure 6.4: An estimate relation between the number of bits of resolution lost while interpolating a bandpass signal and the value of D. A particular case: $k = 20$ and $\Delta k = 0.5$.

To quantify how the choice of D will affect the sensitivity of the reconstruction, the authors in Vaughan et al. [1991] provided an relation between the value of D and the number of bits, N_b of resolution lost in reconstructing $f(t)$:

$$N_b = \log_2 \left(\frac{\Delta k}{\sin^2 \pi B D k} + \frac{1 - \Delta k}{\sin^2 \pi B D (k+1)} \right)^{1/2} \tag{6.10}$$

where

$$\Delta k = k - \frac{2 f_l}{B} \tag{6.11}$$

In terms of practical implementation, Eq. 6.10 indicates how the errors in the sample data (quantization noise, wideband noise, clock jitter) magnify during the reconstruction of $f(t)$. Eq. 6.10 is represented graphically in Fig. 6.4 for an example where $k = 20$ and $\Delta k = 0.5$. The function is periodical of period T and symmetrical with respect to $D = T/2$. It has be shown that the optimum values for D are:

$$D = \pm \frac{1}{4 f_c} \tag{6.12}$$

These results show that in order to reduce the sensitivity of the signal construction with respect to the uncertainty in data measurement, and thus to minimize the computing cost, D should be chosen as close as possible of $D = \pm \frac{1}{4 f_c}$.

Let's see the implications of the previous result for the example presented in Figure 6.4 where $f_l = 975$ MHz, $B = 100$ MHz, $f_c = f_l + B/2 = 1025$ MHz, $k = \lceil 2 f_l / B \rceil = 20$ and $\Delta_k = k - f_l/B = 0.5$. In this case the ideal value for D would be $D = 232$ ps. However a value of D between 150 ps $< D <$ 332 ps will guarantee that the reconstruction would be carried on with a precision loss of less than 0.5 bits compared with the ideal value. This loss is affordable as will be shown later. Moreover, current IC technology allows us to select delay with steps of approximative 2 ps, hence circuit realization of a delay in the range given is entirely feasible.

6.4.2 Reconstruction Robustness w.r.t. Uncertainties in D

Once we know that is feasible to design delay element DCDE with enough accuracy to keep the reconstruction coefficients values bounded, there remains the question on how much the actual delay must match the mathematical D used in Eq. 6.3. Because the interpolants in Eq. 6.3 depend directly on the value of D, it is important to study how the uncertainty in the value of D will affect the performance of the reconstruction. To do this, let's consider that instead of knowing the true value of D, only an estimate $\hat{D} = D + \Delta D$ is available.

Vaughan et al. [1991] have shown that the relative difference between the reconstructed spectrum $\hat{F}(f)$ and the actual spectrum $F(f)$ can be approximated as:

$$\Delta F = \left| \frac{\hat{F}(f) - F(f)}{F(f)} \right| \approx \pi B(k+1)\Delta D \tag{6.13}$$

Eq. 6.13 shows that, as the ratio between the signal frequency position ($k = \lceil 2f_l/B \rceil$) and the signal bandwidth B increases, the acceptable values for the difference ΔD between the true delay D and the delay $\hat{D}$ uses to reconstruct the signal, become very small. Moreover, the precision of reconstruction depends also on the signal frequency f_l, and not only on the signal bandwidth B, as it would be desirable. This means that for a higher carrier frequency, the estimate of delay D should be more accurate in order to keep the reconstruction error small.

For example, for a bandpass signal at $f_c = 1$ GHz to be recovered from the samples of two ADCs running at $f_s = B = 80$ MHz with a precision of $\Delta F = 1\%$, ΔD must satisfy:

$$\Delta D \leq \frac{1}{25} \frac{0.01}{\pi 80 \cdot 10^6} \approx 2 \text{ ps} \tag{6.14}$$

The result above is significant because it shows that a robust bandpass reconstruction with PNS2 is possible even if only an estimate of D ($\hat{D}$) is available. Indeed, there are several hardware implementations reported [Camarero et al., 2008; Jamal et al., 2004] that can estimate and correct the time-skew between two ADCs with a granularity of few ps. In conclusion, Eq. 6.13 and the example from Eq. 6.14 establish that a critical point while reconstructing a bandpass signal using nonuniform sampling is the accurate knowledge of D. In the next section we focus our attention on this aspect and we discuss two delay estimation techniques.

6.4.3 DCDE Practical Implementation

The theoretical analysis previously presented revealed that for a signal positioned within the [500 MHz, 2 GHz] frequency interval to be bandpass shifted using PNS2, the DCDE should be able to generate a delay between 125 ps and 500 ps with a precision of at least 2 ps. This is not such a hard requirement and several DCDE architectures that meet these constraints have been reported in literature [Haftbaradaran and Martin, 2008; Lei et al., 2014; Camarero et al., 2008].

Such an architecture is described in Haftbaradaran and Martin [2008]. The 6-bit DCDE presented achieves an average of 0.86 ps resolution with a maximum of 1.2 ps (the DCDE resolution is defined as the DCDE delay change for one LSB change in the input digital code). The circuit presented in Haftbaradaran and Martin [2008] consists of a primary inverter in parallel with an inverter matrix which together operate as an equivalent inverter (Fig. 6.5). By applying a specific binary code to the inverter matrix, a combination of secondary inverters is turned on, resulting in the change of the W/L ratio of the equivalent inverter. Changing the W/L ratio causes the delay of the equivalent inverter to change. Experimental results show

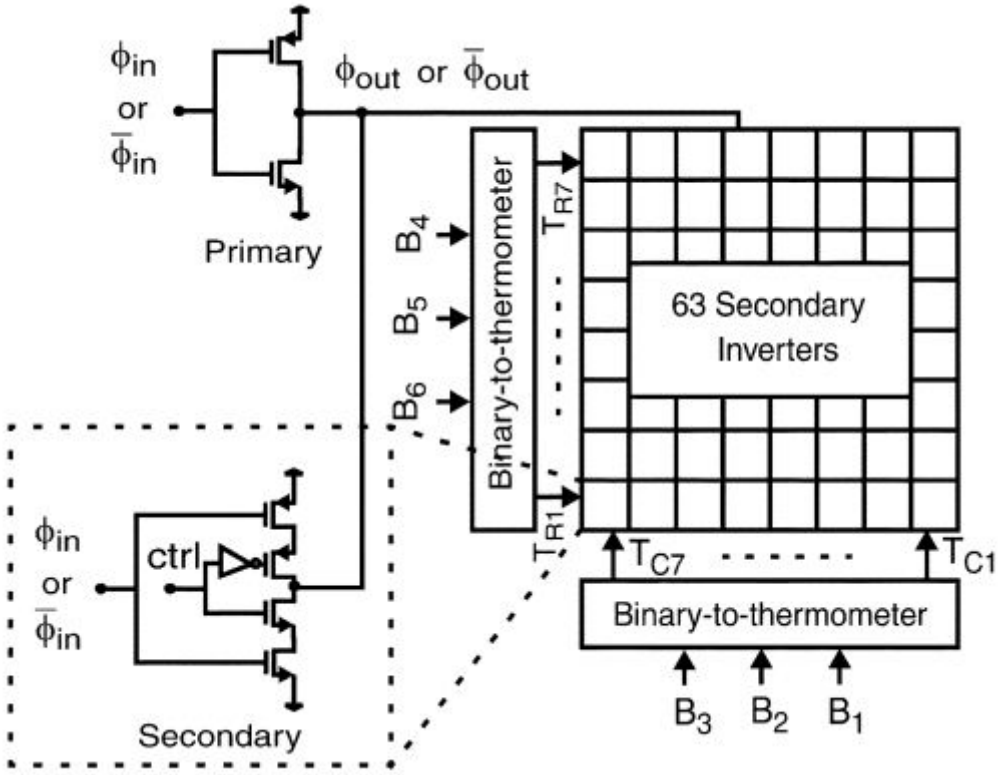


Figure 6.5: Architecture of 6-bit DCDE [Haftbaradaran and Martin, 2008]

that the circuit achieves a very low jitter: 1.2 ps rms for an input having 0.86 ps rms at 200 MHZ frequency.

A similar DCDE circuit is used in Camarero et al. [2008]. This time, the block achieves a resolution of 1.8 ps which is still sufficient for our needs.

Considering their specifications and performance, the DCDEs discussed here can be used in our PNS2 sampler without any other modifications or improvements. We can safely assume that the precision of the DCDEs is not going to be an issue for the future hardware implementation of our PNS2 sampler. Nonetheless, there is another aspect that has to be considered. Due to different imperfections in the manufacturing process, the variation of the generated delay from its nominal value can be significant. In fact, for the circuit described in Haftbaradaran and Martin [2008]; Camarero et al. [2008] this variation can reach ±0.5 ps. This implies that the true delay introduced by the DCDE cannot be assumed equal to the nominal design values. Thus, further estimation techniques have to be employed. In the next section we focus our attention on this aspect and we discuss two delay estimation techniques.

6.4.4 Delay Estimation

The analysis carried out previously revealed that a robust reconstruction using PNS2 hinges on a good estimate of the true delay D. We will now introduce and evaluate two alternative ways to obtain an estimate $\hat{D}$ that can satisfy our needs. The two methods do not involve additional hardware. In effect, it's possible to obtain $\hat{D}$ by running estimation algorithms on the data streams coming out of the I/Q ADCs.

The first algorithm adapts a technique presented in Camarero et al. [2008]; Jamal et al. [2004], originally in the scope of calibrating a time-interleaved ADC (TIADC). Our key obser-

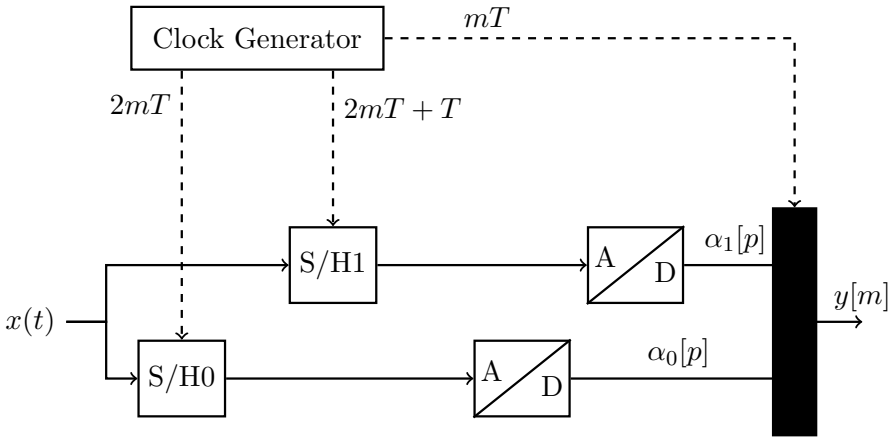


Figure 6.6: Block diagram of two channel time-interleaved ADC architecture

vation is that the structure depicted in Fig. 6.2 is similar to a two-channel TIADC. In the scope of TIADCs, the delay D is interpreted as a deviation of the sampling interval from the ideal one. This time-skew degrades the distortion specifications of high-speed TIADCs. By monitoring this degradation, the time-skew can be estimated.

We also developed another novel way to estimate the delay D. It follows a completely different strategy, relying on monitoring the quality of the PNS2 reconstruction itself. We were able to estimate time-skew accurately using an LMS algorithm, together with PNS2 reconstruction function. Later, we extended our method to the estimation of gain mismatch.

Both of the previous time-skew estimation algorithms assume that the two channels aren't affected by any other mismatches or that those mismatches were previously corrected by a separate calibration step. While calibrating strategies for the gain error and offset error exist, their implementation would require additional hardware overhead and spend more resources (time, etc.). In this section we show that our LMS algorithm implementation can be further extended, so that another mismatch, the gain error, is taken into consideration and corrected. The gain error is indeed considered the second most difficult nonideality to be detected and corrected.

6.4.4.1 Time-Interleaved ADC (TIADC)

To understand the first delay estimation algorithm it is necessary to analyze the architecture of a time-interleaved ADC (TIADC) and its similarities with our proposed BIST solution. Fig. 6.6 shows a simplified block diagram of a two channel time-interleaved ADC. It consists of two ADCs operating in parallel at half of the overall sampling rate [Singer et al., 2000; Wang and Razavi, 2000; Dyer et al., 1998; Bright, 1998]. During conversion, the analog multiplexer selects each channel in a ping-pong manner. The result is a conversion rate two times greater than the speed of the individual ADCs (at twice the power dissipation).

Theoretically, this interleaved structure would allow to multiply the overall sample rate achieved by the number of conversion channels ADC without degrading the converted signal (distortion, etc.). This is not the case. The combined conversion results worsen due to unavoidable mismatches between different channels. The most important are offset error, gain error, and time-skew. The offset errors appear when the center of the conversion range differs between channels. The gain errors are defined by different conversion ranges between channels. The time-skew appears when the time interval between the different sampling instants are not equal. The sampling period is not constant, which will result in distortion of the recovered

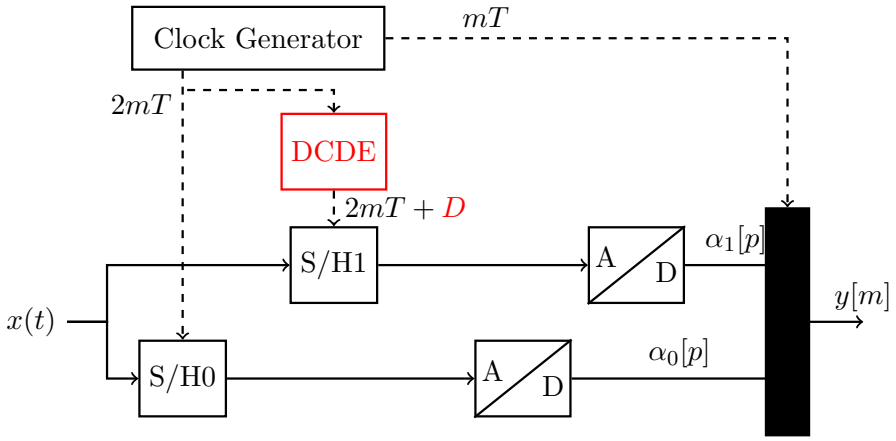


Figure 6.7: Block diagram of the proposed BIST architecture. The difference between this architecture and the one presented in Figure 6.6 is the Digitally Controlled Delay Element (DCDE)

signal.

These limitations were recognized from the outset, and channel mismatch calibration strategies have been continuously introduced. The offset and the gain error calibrations are relatively simple to implement [Conroy et al., 1993; Fu et al., 1998; Sumanen et al., 2001], and will not be discussed further here. Time-skew calibration, on the other hand, is a more, challenging task. It requires estimation and correction of sample time error across channels. Time-skew calibration can be performed separately (offline) or concurrently (online) with the normal use of the TIADC.

Offline (foreground) calibration typically injects specially crafted waveforms at the input, collects the conversion results and then computes some adjustment parameter that corrects the skew. There are many proposed techniques, with multiple variations on waveforms (sine, ramp, pseudo-random noise) and output analysis (time, or frequency domain) [Jeng, 1988; Jin and Lee, 2000; Fu et al., 1998]. Foreground calibration techniques are effective, but they aren't appropriate if the TIADC must remain online continuously or for extended lengths of time. In this case, temperature and aging variations across channels won't be tracked.

Background (online) calibration aims to run concurrently with the normal use of the TIADC, either by only observing the output (blind calibration) or by provoking slight perturbations in the conversion process and observing the effects on the outputs. Background calibration works in terms of statistical signal processing, thus it is usually much slower than foreground calibration.

Comparing Fig. 6.7 and 6.6 one can easily notice that our proposed BIST block differs from a TIADC only through the adjustable delay element. This element can be interpreted as a time-skew error between the channels. Therefore, every time-skew detection technique developed for TIADC could in principle be adapted to our purpose of estimating the delay for PNS2 reconstruction. Nonetheless, one should note that the time-skew calibration in standard TIADC architectures is a more difficult endeavor, since one must estimate the delay across channels and then suppress it. The critical path is often this correction, which typically hits the ultimate limits of the underlying technology. This is not the case for our subsampler, where a null (or exact) adjustment of time-skew is not necessary. Our challenge is only to estimate it accurately. The time-skew estimation methods will be studied in the following sections.

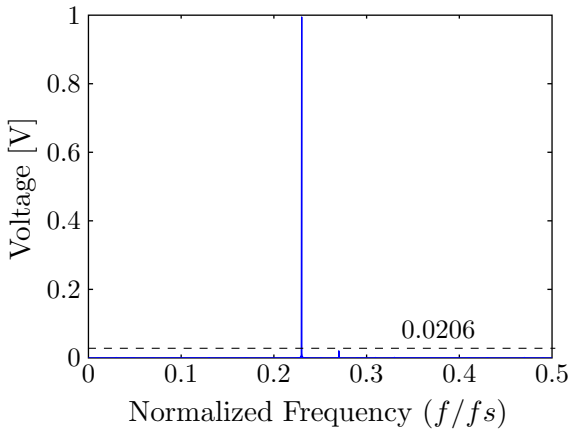


Figure 6.8: Frequency spectrum at the output of a two channel TIADC affected by a time-skew of $d = 172$ ps, for an input sinewave of amplitude 1 and frequency $0.23f_s$. As predicted by Eq. 6.16, an image frequency is produced due to the time-skew

6.4.4.2 Sinusoid-Based Time-Skew Detection Technique

Let's consider for now, only the sample acquisition block of the proposed BIST architecture. The block diagram is presented in Fig. 6.7.

The first delay-estimation technique we study is the one proposed in Camarero et al. [2008]; Jamal et al. [2004], a foreground calibration technique. The choice is motivated by the high performance achieved by this technique, while keeping a simple practical implementation.

Let us consider the two channels TIADC from Fig. 6.6. Ideally, each channel should sample T seconds after the previous channel. If a time-skew mismatch appears, the upper channel will sample at a time $T+d$ after the lower channel (Fig. 6.7 can be interpreted as a model of TIADC with a time-skew error). The ADC output with a sinusoid input $x(t) = \cos(\omega_0 t), 0 < \omega_0 < \omega_s/2$ is:

$$y[m] = \cos(\omega_0 t)|_{t=mT+\frac{d}{2}-(-1)^m\frac{d}{2}} \tag{6.15}$$

or after several manipulations:

$$\begin{aligned} y[m] \quad = \quad & \cos\left[\frac{\omega_0 d}{2}\right]\cos\left[\omega_0 mT + \frac{\omega_0 d}{2}\right] \\ & -\sin\left[\frac{\omega_0 d}{2}\right]\sin\left[(-\omega_0 + \frac{\omega_s}{2})mT - \frac{\omega_0 d}{2}\right] \end{aligned} \tag{6.16}$$

where $\omega_s = 2\pi/T$.

In Eq. 6.16 the first term is the sampled input (scaled by $\cos(\omega_0 d/2)$ and phase shifted by $\omega_0 d/2$), and the second term is the image of the input due to time-skew mismatch. Therefore, in the frequency domain, the time-skew error produces an image that is located at $\omega_s/2 - \omega_0$ and has a amplitude approximately proportional with the delay d and the input frequency ω_0 (if $d << T$ then $\cos(\omega_0 d/2) \approx 1$ and $\sin(\omega_0 d/2) \approx \omega_0 d/2$).

Fig. 6.8 shows the simulated digital output voltage spectrum for a sinusoid entering a two channels TIADC, where $\omega_0 = 0.23\omega_s$, $\omega_0 d/2 = 0.02$ rad and $f_s = 160$ MHz. We considered that there are no gain or offset mismatches. As predicted by theory, the spectrum presented in Figure 6.8 shows a spurious signal of amplitude $\approx \omega_0 d/2$.

Using the previous observations, the authors in Jamal et al. [2004] proposed the architecture depicted in Fig. 6.9 as a technique to identify the delay between the two ADCs. The estimator is based on the fact that if the TIADC input contains a frequency component at ω_0, an image appears at $\omega_s/2 - \omega_0$. The image has an amplitude that is related to the delay d and, after

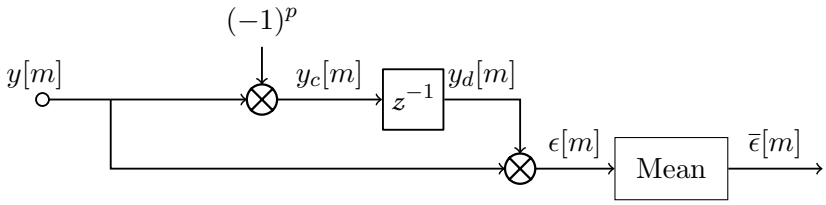


Figure 6.9: Block diagram of the time-skew detector as proposed by Jamal et al. [2004]. $y[m]$ is the output of the TIADC shown Fig. 6.7.

chopping, the image is 90° out of phase with a phase that caused it. The detection can be implemented in foreground using an appropriate input signal.

In the following, we will present succinctly the technique. The output of the TIADC, $y[m]$ is chopped to produce $y_c[m]$ and then is passed through a delay filter to produce $y_d[n]$. $y[m]$ and $y_d[m]$ are then multiplied. The chopped signal $y_c[m]$ can be written as:

$$\begin{aligned} y_c[m] &= (-1)^m y[m] \\ &= a\cos\left[\left(\frac{\omega_s}{2}-\omega_0\right)mT-\frac{\omega_0 d}{2}\right] \\ &\quad +b\sin\left[\omega_0 mT+\frac{\omega_0 d}{2}\right] \end{aligned} \tag{6.17}$$

where $a=\cos(\omega_0 d/2)$ and $b=\sin(\omega_0 d/2)$

The chopped signal goes through a delay filter, z^{-1} to produce :

$$\begin{aligned} y_d[m] &= a\cos\left[\left(\frac{\omega_s}{2}-\omega_0\right)(m-1)T-\frac{\omega_0 d}{2}\right] \\ &\quad +b\sin\left[\omega_0(m-1)T+\frac{\omega_0 d}{2}\right] \end{aligned} \tag{6.18}$$

Then $y[m]$ and $y_d[m]$ are multiplied, the product having a dc that is equal to:

$$\begin{aligned} \bar{\epsilon} &= \overline{y_d \cdot y} = -ab\sin(\omega_0 T) \\ &= -\cos\left(\frac{\omega_0 d}{2}\right)\sin\left(\frac{\omega_0 d}{2}\right)\sin(\omega_0 T) \end{aligned} \tag{6.19}$$

If we replace d with $D-T$, Eq. 6.19 becomes:

$$\bar{\epsilon} = -\sin(\omega_0 D-\omega_0 T)\sin(\omega_0 T) \tag{6.20}$$

If $|\omega_0 D| << 1$, Eq. 6.20 can be simplified to:

$$\bar{\epsilon} \approx -\frac{\omega_0 D}{4}\sin(2\omega_0 T)+\frac{\sin^2(\omega_0 T)}{2} \tag{6.21}$$

Eq. 6.21 indicates that the block presented in Fig. 6.9 outputs a value that can be used for identification of the time-skew D.

Conclusions In this section we have presented a digital technique for time-skew estimation between two ADCs in parallel. The technique is designed for foreground implementation. While having a simple practical implementation, this technique has some limitations. First of all, the input signal has to be known and bandlimited to less than $\omega_s/2$ and should not have a frequency component at $\omega_s/4$ (for a proof see Jamal et al. [2004]; Camarero et al. [2008]). Moreover, the technique is sensitive to the input frequency. Indeed, it can be shown from Eq. 6.20 that $\bar{\epsilon}$ peaks when the input frequency, ω_0 is near $\omega_s/4$ and decreases at higher input frequencies. The sensitivity of time-skew detection will follow the same trend.

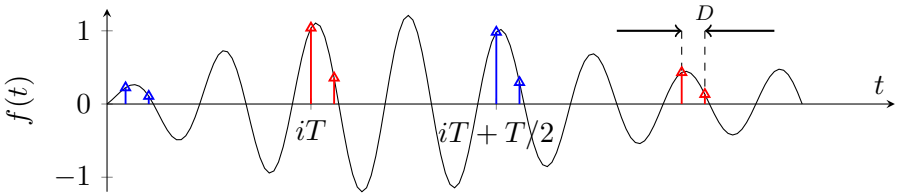


Figure 6.10: Time domain representation of PNS2 sampling

6.4.4.3 LMS-Based Time-Skew Detection Technique

Given the limits and restrictions of the previous technique, we decided to develop a new method, taking advantage of the mathematical properties of PNS2 reconstruction. We coupled our mathematical model to a Least Mean Squares (LMS) algorithm to obtain an accurate estimate of the time delay between the two sample streams.

The key idea is to use the intrinsic mathematical properties of PNS2 sampled signals as presented in the following. In the beginning, we define a quadratic cost function $J(\hat{D})$ that uses the difference between the actual measured values of a set of samples and the reconstructed values of the same set. The reconstructed values are obtained using the PNS2 reconstruction formula shown in Eq. 5.16. Notice that we are using the reconstruction formula of $f(t)$ (original passband signal) from Eq. 5.16 and not of $f_{bb}(t)$ (baseband shifted version) from Eq. 5.20. This is valid only for the estimation step. For the TX test, Eq. 5.20 will be implemented.

Secondly, an LMS algorithm is employed to minimize the cost function $J(\hat{D})$ and accurately estimate the value of the delay D. We prove that the delay estimation is correct as long as an initial estimate is available. Finally, we extend the LMS algorithm for gain error compensation.

The LMS technique presented here can be used for foreground estimation. Nonetheless, if the input signal satisfies some conditions given at the end of this section, the proposed technique can be implemented in background. The technique is described in the following.

Consider the time domain representation of PNS2 sampling in Fig. 6.10. Let's suppose that the signal is sampled at twice the minimum sampling frequency. That means the blue samples in Fig. 6.10 can be fully reconstructed from the red samples. In other words, for every sample $f[iT + T/2]$ and $f[iT + T/2 + D]$ we have the actual value measured by the ADC and an estimate given by:

$$f[iT + T/2] = \sum_{n=-n_w/2}^{+n_w/2} [f[iT + nT]s(T/2 - nT) - f[iT + nT + D]s(T/2 - nT - D)] \quad \forall i \in \mathbb{N}, i > n_w/2 \tag{6.22}$$

and

$$f[iT + T/2 + D] = \sum_{n=-n_w/2}^{+n_w/2} [f[iT + nT]s(T/2 + D - nT) - f[iT + nT + D]s(T/2 - nT)] \quad \forall i \in \mathbb{N}, i > n_w/2 \tag{6.23}$$

where Eq. 6.22 and Eq. 6.23 have been obtained from Eq. 5.16 by replacing t with $iT + T/2$ and $iT + T/2 + D$, respectively.

Let's denote $\hat{f}[i, D] = f[iT + T/2 + D]$ and by $\tilde{f}[i, D]$ the measured valued of the sample $f[iT + T/2 + D]$ which might be affected by noise and nonlinearities of the ADC. We can define

now the following cost function:

$$J(\hat{D}) = \frac{\sum_{i=n_w/2}^{N+n_w/2} (\hat{f}[i,\hat{D}] - \tilde{f}[i,D])^2}{N} \tag{6.24}$$

$J(\hat{D})$ is a quadratic cost function that gives us information about how close is the estimate $\hat{D}$ from the real value D. We consider N samples in order to mitigate the effects of noise measurements and other nonidealities. The time-skew estimation problem can be defined as the following minimization problem: having an initial estimate $\hat{D}^0$, find $\hat{D}$ that minimizes the cost function $J(\hat{D})$.

$$\min_{\hat{D}} J(\hat{D}) \tag{6.25}$$

Least-Mean Squares (LMS) Algorithm The minimization problem defined by the Eq. 6.25 can be solved with an LMS algorithm. The Least Mean Squares (LMS) algorithm Haykin [2002] is an adaptive algorithm, which uses a gradient-based method of steepest decent. LMS incorporates an iterative procedure that makes successive corrections to the weight vector in the direction of the negative of the gradient vector which eventually leads to the minimum mean square error. Compared to other searching algorithms, LMS algorithm is relatively simple; it does not require correlation function calculation nor does it require matrix inversions.

In the initialization phase, the user needs to provide an estimate $\hat{D}^0$ and a step size parameter μ. At each step the LMS algorithm will adapt the estimate $\hat{D}$ according to Eq. 6.27. We have selected a normalized LMS algorithm to simplify the choice of μ. The choice of step size μ reflects a trade off between the convergence time and the residual error in the estimate: as μ is larger the convergence time is reduced but the residual error grows. Thus, we consider two approaches for the choice of μ:

- μ remains constant for every iteration. This will result in a better stability of the algorithm but a longer convergence time
- μ is adapted every iteration. The value of μ at each iteration varies according to an estimate of the distance to the mean-square-error minimum, thereby providing faster convergence [Harris et al., 1986; Dennis and Schnabel, 1983]. At every iteration k, the value of μ is calculated as following. If the gradient of the cost function ∇J alternates sign on m_0 (here we chose $m_0 = 2$) successive samples the value of μ is decreased. Conversely, the value of μ is increased if ∇J has the same sign for m_1 (here we chose $m_1 = 2$) successive samples. However, μ is allowed to vary between the values μ_{max} and μ_{min}. The selection of μ_{max} is based on stability considerations, while μ_{min} is chosen to provide the desired residual error after the algorithm converged.

The analytical derivative of the gradient $\nabla J(\hat{D}^k)$ is too complicated for efficient computation. We have chosen to substitute it by a finite difference approximation. The adaptive LMS algorithm we use is summarized in Algorithm 1.

Until now, we devised an adaptive algorithm to estimate the delay between the two channels of the proposed BIST architecture. There remains the question on the convergence properties of out algorithm, for arbitrary inputs. This subject is discussed in the next section.

Proof of LMS convergence In our DCDE block, we can set a nominal delay D^* and we wish to know the actual D in order to calculate the correct coefficients for the reconstructing filters. We have shown that we can use the mathematical properties of the two sample streams

Algorithm 1 Time-skew identification based on LMS algorithm

initialization

- Choose N
- Collect the samples $\tilde{f}[i,0], \tilde{f}[i,D], \tilde{f}[i,T/2+D], i \in \overline{0, N+n_w}$
- Choose $\rho_0 > 1, \rho_1 > 1, \mu_{min}, \mu_{max}$
- Provide initial estimates for μ and $\hat{D}^0$

repeat

1. Calculate $\hat{f}[i, T/2+\hat{D}^k], i \in \overline{n_w/2, N+n_w/2}$ using relation 6.23
2. Calculate the gradient $\nabla J(\hat{D}^k)$ numerically:

$$\nabla J(\hat{D}^k) = \frac{J(\hat{D}^k) - J(\hat{D}^{k-1})}{\hat{D}^k - \hat{D}^{k-1}} \tag{6.26}$$

3. (for variable step size algorithm only)
   if $\text{sign}(\nabla J(\hat{D}^k) \cdot \text{sign}(\nabla J(\hat{D}^{k-1}) > 0$ **then**
   3.1. $\mu = \mu \cdot \rho_0$
   3.2. $\mu = \min(\mu, \mu_{max})$
   else
   3.1. $\mu = \mu / \rho_1$
   3.2. $\mu = \max(\mu, \mu_{min})$
   endif
4. Update the parameter estimates:

$$\hat{D}^{k+1} = \hat{D}^k - \mu \frac{\nabla J(\hat{D}^k)}{\max \left| \nabla J(\hat{D}^k) \right|} \tag{6.27}$$

5. $k = k + 1$

until k is greater than a maximum limit or $J(\hat{D}^k) - J(\hat{D}^{k-1})$ is sufficient small

to obtain an estimation of the delay D. The adaptive LMS algorithm was chosen, since it's fast and robust, but one interrogation concerns its absolute convergence when applied to our estimation technique. Here we prove that, if we set an actual delay $D \in]0, \frac{1}{k^+B}[$, the problem defined by Eq. 6.25 has only one minimum in the interval $\hat{D} \in]0, m = \frac{1}{k^+B}[$ (where $k^+ = k+1$ and k represents the signal position, $k = \lceil 2f_l/B \rceil$) which will occur when $\hat{D} = D$. To do that, we first redefine the minimization problem in the frequency domain, and then we show that the derivative of the cost function w.r.t. $\hat{D}$ has only one zero in the interval $]0, m = \frac{1}{k^+B}[$.

For the sake of simplicity, the demonstration will be presented in the frequency domain. Eq. 6.25 is equivalent to:

$$\min_{\hat{D}} J_F(\hat{D}) \tag{6.28}$$

where

$$J_F(\hat{D}) = \left\| \hat{F}(\hat{D}, f) - F(f) \right\| \tag{6.29}$$

where $\hat{F}(\hat{D}, f)$ is frequency spectrum reconstructed with the estimated value of the delay, $\hat{D}$,

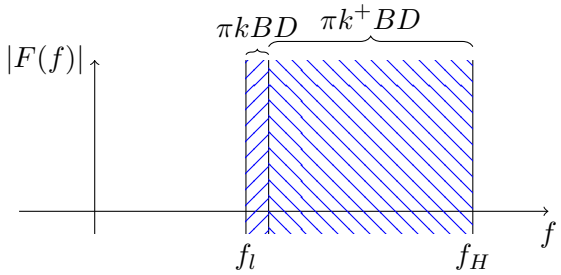


Figure 6.11: Frequency domain operation of the PNS2 technique

and $\|\cdot\|$ is the euclidean norm. In fact, $\hat{F}(\hat{D}, f)$ is the frequency representation of $\hat{f}[i, \hat{D}]$

As derived in Fig. 5.5, the frequency spectrum resulting from combining two sampling sequences, $f[nT]$ and $f[nT + D]$ is divided in two regions: $R_1 = [f_l, f_l + \pi BkD]$ and $R_2 = [f_l + \pi kBD, f_H]$. The separation is depicted in a simplified way in Fig. 6.11. Let's say that instead of knowing the real value of D, only an estimate $\hat{D} = D + \Delta D$ is available. The deviation from the ideal known delay D will affect the reconstruction of $F(f)$ according to the following relation:

$$\hat{F}(\hat{D}, f) = \begin{cases} e^{-j\pi kB\Delta D} F(f) & \text{if } f \in R_1 \\ e^{-j\pi k^+ B\Delta D} F(f) & \text{if } f \in R_2 \end{cases} \tag{6.30}$$

We continue the demonstration only for the zone R_1. For the other zone the demonstration gives similar results. For the zone R_1 we can write:

$$\begin{aligned} J_F(\hat{D}) &= \left\| \mathrm{e}^{-j\pi kB\Delta D} F(f) - F(f) \right\| \\ &= \|F(f)\| \cdot \|\mathrm{e}^{-j\pi kB\Delta D} - 1\| \\ &= \|F(f)\| \cdot \|\cos \pi kB\Delta D - 1 - j \sin \pi kB\Delta D\| \\ &= \|F(f)\| \cdot \left((\cos \pi kB\Delta D - 1)^2 + \sin^2 \pi kB\Delta D \right) \\ &= \|F(f)\| \cdot (2 - 2\cos \pi kB\Delta D) \end{aligned} \tag{6.31}$$

The derivative of $J_F(\hat{D})$ with respect to $\hat{D}$ is:

$$\frac{\partial J_F(\hat{D})}{\partial \hat{D}} = \|F(f)\| 2\pi kB \sin \pi kB\Delta D \tag{6.32}$$

Eq. (6.32) shows that the cost function $J_F(\hat{D})$ has only only minimum in the interval $\Delta D \in \left]\frac{-1}{kB}, \frac{1}{kB}\right[\Rightarrow \hat{D} \in \left]D - \frac{1}{kB}, D + \frac{1}{kB}\right[$. But, we have seen that the cost function goes toward to $+\infty$ when the $\hat{D} = 0, \frac{1}{kB}, \frac{2}{kB}, \ldots$ Those values should be avoided. Thus, we should impose that the search of $\hat{D}$ is limited to the interval: $\left]0, \frac{1}{kB}\right[$, where the cost function has only one minimum that appears at $\hat{D} = D$.

Following the same reasoning for the region $R_2 = [f_l + \pi kBD, f_H]$, it can be shown that the cost function $J_F(\hat{D})$ has only one minimum in the interval $\left]0, \frac{1}{k^+B}\right[$.

Putting the previous results together, we can state that the problem defined by Eq. 6.28, and equivalent with Eq. 6.25, has only only minimum in the interval $\left]0, \frac{1}{k^+B}\right[$ which occurs when $\hat{D} = D$. Thus, the problem can be solved with an LMS algorithm, such as the one presented in Algorithm 1.

Remarks The results presented previously are indeed very useful. In fact, we have proved that the delay D between the channels in the BIST architecture can be accurately estimated using an LMS algorithm. The proposed algorithm does not require a particular input stimuli. The only constraint is that the test signal has a bandwidth limited to half of the ADCs sample rate. More important, the input signal doesn't have to be known. We rely on the underlying mathematical properties of the PNS2 reconstruction formula itself. We will show later in the simulations section, that any digital communication waveform can serve as input stimuli. Such waveforms are the ones the TX channel is intended for.

Another aspect that should be highlighted is the simple DSP-only implementation. In fact, the proposed LMS skew estimation can be run concurrently with the PNS2 reconstruction for BIST with very little hardware overhead. If we analyze Algorithm 1 again we can see that the most time consuming operation is the computation of the gradient. Or, we can use the existing FIRs to realize that operation.

Finally, the dynamic of the evolution of the cost function or the step size uncovers essential information about the state of the BIST block. We didn't pursue this idea further, but we believe that a statistical analysis of these functions (time to converge, final value, step size evolution) could provide valuable information about the functionality of the PNS2 subsampler, opening the way to a fully self-tested self-calibrated loopback test. We will present later some results that support our supposition.

6.4.4.4 A Multivariable LMS (MLMS) Algorithm

While time-skew uncertainty is a key concern for our PNS2 reconstruction, gain error is also a major concern. In the realm of TIADC, it's the second most difficult nonideality to correct by digital calibration. Indeed, in our mathematical developments of PNS2 reconstruction, we considered that the two ADCs had no discernible gain mismatch. This is not entirely true and imperfections in the manufacturing process will deviate the ideal gain by as much as $\pm 10\%$.

Let's analyze now the impact of gain mismatch in our mismatch in our PNS2 reconstruction. Let G be ideal designed gain for each of the ADCs and let's consider that the second ADC will deviate by ε_G from this value. Without loss of generality, let's set $G = 1$. Thus, the first ADC will have a gain of 1 and the second one a gain of $1 + \varepsilon_G$. Taking all this into account, we can now rewrite the PNS2 reconstruction of the sample $f[iT + T/2 + D]$ as:

$$\begin{aligned} f[iT + T/2 + D] \quad = \quad & \sum_{n=-n_w/2}^{+n_w/2} [f[iT + nT]s(T/2 + D - nT) \\ & -(1 + \varepsilon_G) f[iT + nT + D] \frac{s(T/2 - nT)}{1 + \varepsilon_G}] \forall i \in \mathbb{N}, i > n_w/2 \end{aligned} \tag{6.33}$$

where $(1 + \varepsilon_G) f(iT + nT + D)$ is the sample train coming out of the second ADC. The term $(1 + \varepsilon_G)$ is added to model the deviation from the ideal gain. One should also notice the term $\frac{1}{1 + \varepsilon_G}$, that has to be added to correct the gain deviation. However, to correct this deviation, ε_G must be known.

We show in the following a multivariable LMS (MLMS) algorithm designed to estimate D and ε_G. The MLMS approach is similar to the single variable LMS algorithm discussed previously. In the beginning we define a multivariable cost function $J(\hat{D}, \widehat{\varepsilon_G})$ that quantifies the distance between the estimates $\hat{D}$ and $\widehat{\varepsilon_G}$ and their true values, D and ε_G. Afterwards, an LMS algorithm is used to minimize the cost function $J(\hat{D}, \widehat{\varepsilon_G})$ w.r.t. to the vector of estimates and the best estimate is provided.

In order to define the MLMS problem let's denote by $\hat{f}[i,\hat{D},\widehat{\varepsilon_G}]$ the reconstruction of the sample $f[iT+T/2+D]$ using the estimates $\hat{D}$ and $\widehat{\varepsilon_G}$:

$$\begin{aligned}\hat{f}[i,\hat{D},\hat{\varepsilon_G}] &= \sum_{n=-n_w/2}^{+n_w/2} [f[iT+nT]s(T/2+\hat{D}-nT) \\ &\quad -(1+\varepsilon_G)f[iT+nT+D]\frac{s(T/2-nT)}{1+\widehat{\varepsilon_G}}]\forall i\in\mathbb{N}, i>n_w/2\end{aligned} \tag{6.34}$$

The following quadratic cost function is defined:

$$J(\hat{D},\widehat{\varepsilon_G}) = \frac{\sum_{i=n_w/2}^{N+n_w/2}(\hat{f}[i,\hat{D},\widehat{\varepsilon_G}]-\tilde{f}[i,D])^2}{N} \tag{6.35}$$

and the problem of finding D and ε_G can be defined as: find $\hat{D}$ and $\hat{\varepsilon_G}$ that minimize the cost function:

$$\min_{\hat{D},\widehat{\varepsilon_G}} J(\hat{D},\hat{\varepsilon_G}) \tag{6.36}$$

The problem defined in Eq. 6.36 is a multivariable optimization problem that can be solved with a LMS algorithm. To formulate this problem, we adopt the following notations: X^k is a vector that contains the estimates of the parameters at the k^{th} iteration:

$$X^k = \begin{bmatrix} \hat{D}^k \\ \widehat{\varepsilon_G}^k \end{bmatrix} \tag{6.37}$$

W^k is diagonal matrix of the step size parameters at k^{th} iteration:

$$W^k = \begin{bmatrix} \mu_D^k & 0 \\ 0 & \mu_\varepsilon^k \end{bmatrix} \tag{6.38}$$

Similarly, we define W_{min} and W_{max} as diagonal matrix containing the maximum and the minimum step size parameters.

The gradient $\nabla J(\hat{D},\widehat{\varepsilon_G})$ is calculated as:

$$\nabla J(\hat{D}^k,\widehat{\varepsilon_G}^k) = \begin{bmatrix} \frac{\partial J(\hat{D}^k,\widehat{\varepsilon_G}^k)}{\partial \hat{D}^k} & \frac{\partial J(\hat{D}^k,\widehat{\varepsilon_G}^k)}{\partial \widehat{\varepsilon_G}^k} \end{bmatrix} \tag{6.39}$$

where the partial derivatives are calculated through finite difference approximation:

$$\begin{aligned}\frac{\partial J(\hat{D}^k,\widehat{\varepsilon_G}^k)}{\partial \hat{D}^k} &= \frac{J(\hat{D}^k,\widehat{\varepsilon_G}^k)-J(\hat{D}^{k-1},\widehat{\varepsilon_G}^k)}{\hat{D}^k-\hat{D}^{k-1}} \\ \frac{\partial J(\hat{D}^k,\widehat{\varepsilon_G}^k)}{\partial \hat{D}^k} &= \frac{J(\hat{D}^k,\widehat{\varepsilon_G}^k)-J(\hat{D}^k,\widehat{\varepsilon_G}^{k-1})}{\widehat{\varepsilon_G}^k-\widehat{\varepsilon_G}^{k-1}}\end{aligned} \tag{6.40}$$

Our complete multivariable LMS algorithm is listed in Algorithm 2.

6.5 Sample and Hold Elements

Up to this point we have shown that PNS2 reconstruction of any bandpass signal is feasible. We also devised a practical realization using complex coefficients windowed FIR filters. Later, we took into account uncertainties and mismatches in the acquisition and conversion channels,

Algorithm 2 Multivariables LMS algorithm

initialization

- Choose N
- Collect the samples $\tilde{f}[i,0], \tilde{f}[i,D], \tilde{f}[i,T/2+D], i \in \overline{0, N+n_w}$
- Choose $\rho_0 > 1, \rho_1 > 1, W_{min}, W_{max}$
- Provide initial estimates for W^0 and X^0

repeat

1. Calculate $\hat{f}[i, \hat{D}^k, \widehat{\varepsilon_G}^k], i \in \overline{n_w/2, N+n_w/2}$ using relation (6.34)
2. Calculate the gradient $\nabla J(\hat{D}^k, \widehat{\varepsilon_G}^k)$ using (6.39)
3. **if** $\text{sign}\left(\frac{\partial J(\hat{D}^k, \widehat{\varepsilon_G}^k)}{\partial \hat{D}^k}\right) \cdot \text{sign}\left(\frac{\partial J(\hat{D}^{k-1}, \widehat{\varepsilon_G}^{k-1})}{\partial \hat{D}^{k-1}}\right) > 0$ **then**
   - 3.1. $\mu_D^k = \mu_D^{k-1} \cdot \rho_0$
   - 3.2. $\mu_D^k = \min(\mu_D^k, \mu_{D,max}^k)$

   else
   - 3.1. $\mu_D^k = \mu_D^{k-1} / \rho_1$
   - 3.2. $\mu_D^k = \max(\mu_D^k, \mu_{D,min}^k)$

   endif
4. **if** $\text{sign}\left(\frac{\partial J(\hat{D}^k, \widehat{\varepsilon_G}^k)}{\partial \widehat{\varepsilon_G}^k}\right) \cdot \text{sign}\left(\frac{\partial J(\hat{D}^{k-1}, \widehat{\varepsilon_G}^{k-1})}{\partial \widehat{\varepsilon_G}^{k-1}}\right) > 0$ **then**
   - 4.1. $\mu_\varepsilon^k = \mu_\varepsilon^{k-1} \cdot \rho_0$
   - 4.2. $\mu_\varepsilon^k = \min(\mu_\varepsilon^k, \mu_{\varepsilon,max}^k)$

   else
   - 4.1. $\mu_\varepsilon^k = \mu_\varepsilon^{k-1} / \rho_1$
   - 4.2. $\mu_\varepsilon^k = \max(\mu_\varepsilon^k, \mu_{\varepsilon,min}^k)$

   endif
5. Update the parameter estimates:

$$\hat{X}^{k+1} = \hat{X}^k - W^k \nabla^T J(\hat{D}^k, \hat{\varepsilon_G}^k) ./ \max \left| \nabla J(\hat{D}^k, \hat{\varepsilon_G}^k) \right| \tag{6.41}$$

6. $k = k + 1$

until k is greater than a maximum limit or $J(\hat{D}^k)$ is sufficient small

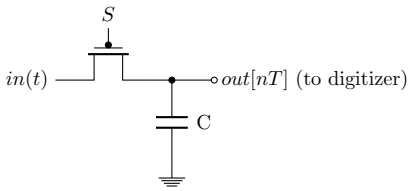


Figure 6.12: Typical voltage sampling circuit

which were also solved. However, we cannot escape the fact that an RF analog signal must be accurately sampled. For example in the architecture in Fig. 6.2 we considered that those samples can be obtained by two ADCs preceded by two Sample and Hold (S/H) blocks. These S/H blocks from the BIST architecture where introduced in our loopback BIST proposal to improve the analog input bandwidth of the I/Q ADCs. These circuit blocks are arguably the weakest point of the proposed implementation because they are required to have a very wide bandwidth (>2 GHz) to follow the RF waveform and simultaneously to impart low distortion. Furthermore, the undersampling operation convolves the clock signal with the input waveform, hence it requires a very low jitter clock to avoid corrupting the output waveform.

Hence, the adoption of PNS2 was a first step towards relaxing the clock generator requirements. Indeed, uniformly spaced undersampling across the whole band would demand a high-quality adjustable clock generation block, while PNS2 requires a single high-quality fixed frequency clock source (presumably already used for the I/Q ADCs) as shown in Fig. 5.4. Our next step in the same direction consisted in replacing the S/H block by charge-domain samplers. The underlying principles of this kind of signal sampling are described in this section.

6.5.1 Charge-domain sampling

Voltage-domain sampling is nearly universally used for discrete-time processing and analog to digital conversion. Conceptually, a switch (often MOS transistors) is placed between the signal source and a capacitor (see Fig. 6.12), and the capacitor voltage is allowed to track the input signal. At the sampling moment, the switch S is turned off, and the voltage signal is held in the output capacitor. The track and hold operation becomes increasingly less precise as the signal frequency increases [Yuan, 2000; Carley and Mukherjee, 1995]. Moreover, the finite turning-off speed (nonzero sampling aperture) and the clock jitter can severely degrade the stored voltage sample. Thus, accurate voltage sampling of RF waveforms is hard to realize.

In order to overcome the limitations of voltage sampling, newer multistandard transceiver architectures process the signal in the charge domain, as proposed in [Yuan, 2000; Carley and Mukherjee, 1995; Poberezhskiy and Poberezhskiy, 2007]. Charge based processing has gained considerable attention for the design of highly flexible SDR receivers [Mirzaei et al., 2008; Geis et al., 2010; Staszewski et al., 2004]. This interest is fueled by its many advantages : dramatically reduced sensitivity to clock jitter, relaxed circuit implementation requirements and inherent anti-aliasing or blocker suppression filtering. Our BIST auRX channel is similar to a discrete-time mixer, inspiring us to adopt charge-domain processing for band translation and filtering. Since the auRX channel is not required to meet specifications as demanding as the main RX channel, we have selected a robust and simple charge-domain architecture : a charge-integrating sampler (CBS). This choice has the advantage of minimizing the extent and the complexity of the hardware added for BIST purposes.

The operating principle of an open-loop CBS is depicted in Fig. 6.13a [Karvonen et al., 2005]. For clarity, a single-ended version is presented. Of course, actual implementation uses a fully differential circuit. The input voltage v_{in} is converted into a current by a transconduc-

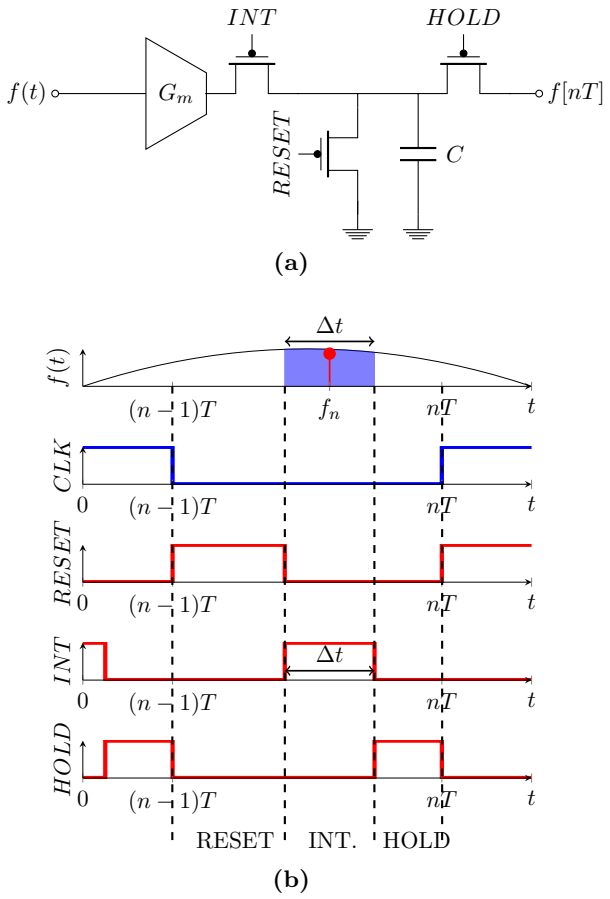


Figure 6.13: Circuit diagram and operating principle of a charge-domain sampler

tance amplifier G_m. The output of the transconductance stage is integrated into the sampling capacitor C during a period Δt. At the end of Δt, integration is stopped and the resulting signal is made available at the output. The integration node is reset (discharged) before a new sample is acquired. The CBS operating sequence is presented in Fig. 6.13b.

The choice of integration period, Δt depends on the kind of waveform to be sampled. If the signal $f(t)$ is a baseband waveform, Δt should not exceed the time during which $f(t)$ can be considered to vary linearly. Thus, the result of the integration represents the value of the function in the middle of this interval. If $f(t)$ is a bandpass signal centered around f_c, the integration period can be chosen as large as $0.5T_c = 0.5/f_c$, i.e. half the carrier frequency period. In this case, the value of the integration represents the value of the function in the middle of the interval multiplied by a time-independent (constant) coefficient.

It is important to notice that Δt shapes the transfer function of the CBS circuit. Indeed, if all the nonidealities are neglected, the transfer function of CBS from Fig. 6.12 is given by:

$$H(f) = \frac{G_m}{C} \frac{\sin(\pi f \Delta t)}{\pi f} \tag{6.42}$$

which is a lowpass sinc filter with nulls at $1/\Delta t$ and its integer multiples, a main lobe at DC, and a set of lobes rolling off at -20 dB/dec (see Fig. 6.14). The impact of this shaping on the signal waveform is minimal in our architecture (PNS2), because the sampling period T is at least one order of magnitude larger than the integration period Δt.

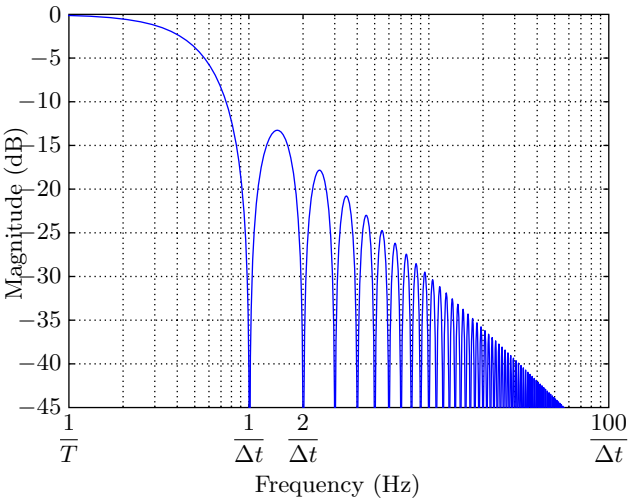


Figure 6.14: Transfer function of an ideal CBS circuit. Δt is the period of integration

Circuit imperfections (i.e., finite output resistance) limit the depth of the nulls of the frequency response. It has been proven that by choosing $\Delta t = 1/(2f_c)$ one obtains the best noise suppression, while $\Delta t = 1/(3f_c)$ provides the best rejection of the 3rd order intermodulation product [Xu and Yuan, 2003]. In our case, PNS2 BIST, we seek greater wideband noise suppression, so we chose $\Delta t = 1/(2f_c)$.

6.5.2 Improved BIST Architecture Based on CBS

Several circuit-level implementations of charge-domain sampling have been reported in literature [Mirzaei et al., 2008]. The significant obstacles addressed are transconductor finite output resistance, switch resistance, non-zero clock transition , charge injection, clock jitter and wideband noise. CBS was demonstrated to be little affected by all these, with the exception of finite output resistance. Nonetheless, in Karvonen et al. [2005] a closed-loop circuit-level (active integrators-based) realization is shown to be relatively robust against finite output resistance. Experimental measurements confirmed that CBS to be superior to VBS w.r.t. wideband noise and clock jitter.

These properties make integrating charge-based sampling well suited for surmounting the stringent S/H specifications required by our previous PNS2 BIST architecture. CBS removes these constraints, simultaneously enhancing the overall performance and robustness. The improved architecture is presented in Fig. 6.15. In comparison with the one shown in Fig. 6.2, the key modification is the replacement of the voltage-domain S/H blocks by charge-domain samplers. This solution requires little additional hardware

We will show on the next section that CBS always result in better estimates of the spectral mask than VBS.

6.6 Simulation Results

Our mathematical analysis and practical considerations resulted in a complete RF BIST strategy containing hardware (analog, digital, mixed-signal) and software (DSP blocks, GPGA or GPP). We modeled and simulated all aspects. In this section we discuss the details of this modeling and comment the results obtained.

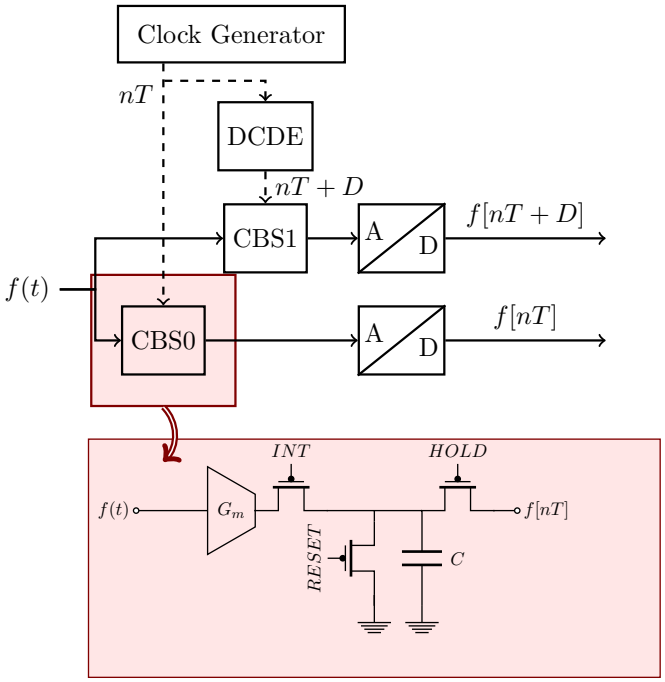


Figure 6.15: Block diagram of the improved BIST architecture

6.6.1 General Simulation Parameters

The periodically nonuniform technique, on which the entire framework is based, requires an explicit simulation of each carrier cycle. To keep the computational effort reasonable, the simulations presented in this paper are based on time-domain behavioral passband models [Chen, 2005]. The behavioral models of the most common RF block were described in Section 4.4.2.

In a first step the behavioral model of an homodyne transmitter was constructed in `Matlab / Simulink`. Our architecture choice was guided by the flexibility, high level of integrability and good performance of the homodyne transmitter. `Matlab` was chosen because the completeness of libraries provided. The block diagram of our homodyne transmitter is depicted in Fig. 6.16. The figure also presents some of the block nominal specifications used during simulation.

The targeted waveform is an one code-channel wideband code division multiple access (WCDMA) signal used in third generation communication devices and described by the 3GPP ®TS 125.104 standard [Standard, 2013]. It occupies a 5 MHz band at $f_c = 1890$ MHz. The block Baseband Physical Layer (PHY) is in charge of channel encoding, multiplexing, channel mapping and code spreading. The details of this block implementation are not discussed here as they are standard and do not affect in any way the proposed test strategy. The block Baseband PHY takes as input a stream of symbols (in our case randomly generated) and output an analog baseband signal that will be modulated by the succeeding RF blocks. This block was built using `Communications System Toolbox/Matlab` as defined by the 3GPP standard.

The I/Q mixers have the purpose of modulating the baseband signal to the carrier frequency f_c. Our model is able to simulate gain and phase mismatches between the I/Q branches but it can also consider mixer nonlinearity and LO jitter.

The power amplifier is modeled by a third order non-linear transfer function according to the Eq. 4.2. The IIP3 parameter of PA was one of the instrument used to inject faults in our transmitter.

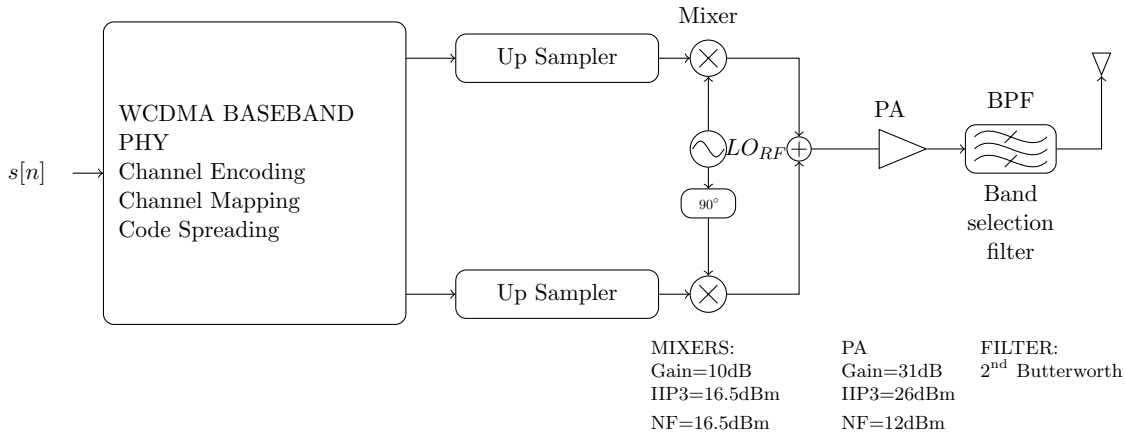


Figure 6.16: Block diagram of the simulated homodyne transmitter

Finally, the bandpass filter is defined in the S-domain as a linear transfer function. We used a second order Butterworth analog filter.

The passband models and our proposed strategy require a sampling time around 1 ps. To obtain this precision, the baseband signal at the output of the BASEBAND PHY block was oversampled. For even more accuracy, linear interpolation is employed. This small sample time allows a very accurate simulation of the jitter in the sampling process, which is a very important performance affecting factor in our loopback-BIST architecture. Given these requirements, the run time to simulate the passband behavior of the entire transmitter remains reasonable (few seconds) because we don't usually need to simulate more than few hundred's symbols.

6.6.1.1 BIST Architecture Simulation Parameters

The block diagram of the VBS based BIST architecture is presented in Fig. 6.2 while the model of the CBS architecture is given in Fig. 6.15. The block is excited with the signal obtained at the output of the TX bandpass filter in Fig. 6.16.

The model of the clock generator supports clock-jitter simulation. The small sample time (around 1 ps) coupled with the linear interpolation allows the simulation of any delay between the two ADCs.

The two type of samplers (charge based and voltage based) are considered ideal. For the charged based samplers a integration period $\Delta t = 0.5 f_c$ was chosen as this value provides greater wideband noise suppression.

The two ADCs used for our proposed BIST architecture have a resolution of 10-bits and sample at a rate of $T = 100$ MSamples/s. The choice was been imposed by the existing ADCs in the RX path, that we want to reuse. The model we developed also supports injection of gain mismatch and offset error between the two branches in the BIST architecture.

Finally, the two FIR filters are implemented with fixed precision using the `Fixed Precision` toolbox in Matlab. The number of taps and taps precision varies depending on simulation and are detailed in a later section.

6.6.2 Adjacent Channel Power Ratio estimation

The specification targeted here is the Adjacent Channel Power Ratio (ACPR) measurement, a key parameter that is hardly verified by BIST techniques. ACPR is one of the most important system-level figures of merit. It measures the amount of distortion generated by transmitter

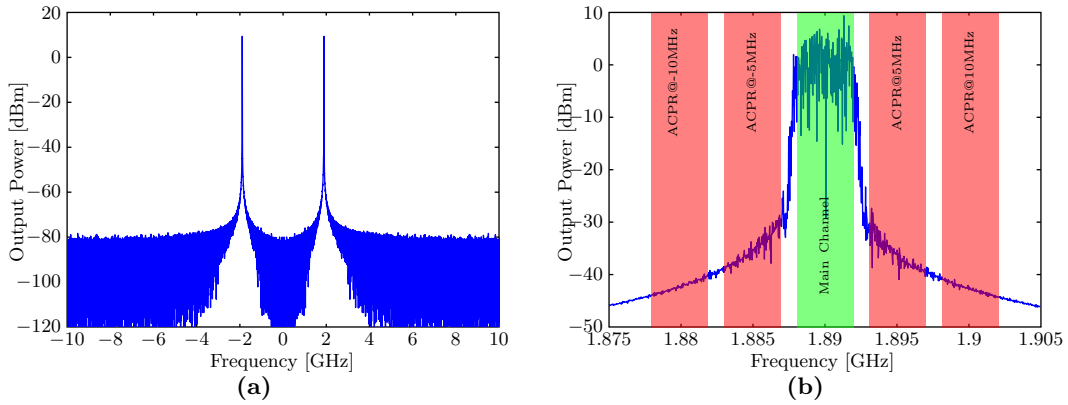


Figure 6.17: ACPR Measurement. Left figure shows the power spectrum of the signal at the output of the receiver. A FFT transform of 2^{19} points was used. The right figure shows the same spectrum around the center frequency f_c. The main channel and the adjacent channels used for ACPR calculation are highlighted.

in the adjacent-frequency channel relative to the power in the main channel. It quantifies the effect of nonlinear distortions and is commonly specified for every digital transmission standard.

The ACPR also gives valuable information for the designer about the influence of nonlinearities in the analog path on the quality of the modulated signal. Together with the modulation scheme, the ACPR sets the maximum allowable nonlinearity of the power amplifier, the last active circuit block before the antenna. Moreover, ACPR measurement is required by any stringent final product qualification procedure. In most BIST strategies the ACPR measurement is replaced by a simpler figure of merit: the third-order interception point (IP3). IP3 is calculated using simple input stimulus (sinusoid or multi-tone signals) and it cannot guarantee the DUT behavior in realistic scenarios, particularly for wide-bandwidth modulation schemes. On the other hand, ACPR measurements are conducted while the DUT is driven by complex digitally modulated waveforms.This characteristic makes the ACPR a realistic and highly desirable measurement for a BIST architecture, and is the target of our efforts.

The W-CDMA standard defines the ACPR as the ratio of the average power in the main channel and any adjacent channels. The main channel has a bandwidth of 3.84 MHz centered around the carrier frequency. W-CDMA requires ACPR measurement for four adjacent channels, located at -10, -5, 5, 10 MHz away from the main channel center frequency. In all cases, the adjacent channel power is obtained using a 3.84-MHz bandwidth. Fig. 6.17 presents a graphical representation of how ACPR is measured/estimated and the position of the adjacent channels. The left figure shows the power spectrum of the signal at the output of the receiver. A FFT transform of 2^{19} points was used. The right figure shows the same spectrum zoomed around the center frequency f_c. The main channel and the adjacent channels used for ACPR calculation are highlighted. This signal will be used in the following simulations to analyze the performance of the our BIST strategy.

6.6.3 Digital PNS2 Reconstruction

In this section we evaluate the digital implementation of the interpolants s_A^{bb} and s_B^{bb}. First we look for the optimal number of taps n_w to be used by the FIR implementation. Fig. 6.18 and 6.19 shows 30 taps of the two interpolants for two values of D, $D = 10$ ps and $D = 100$ ps. The complex coefficients have been separated into their real part (left subfigures) and imaginary

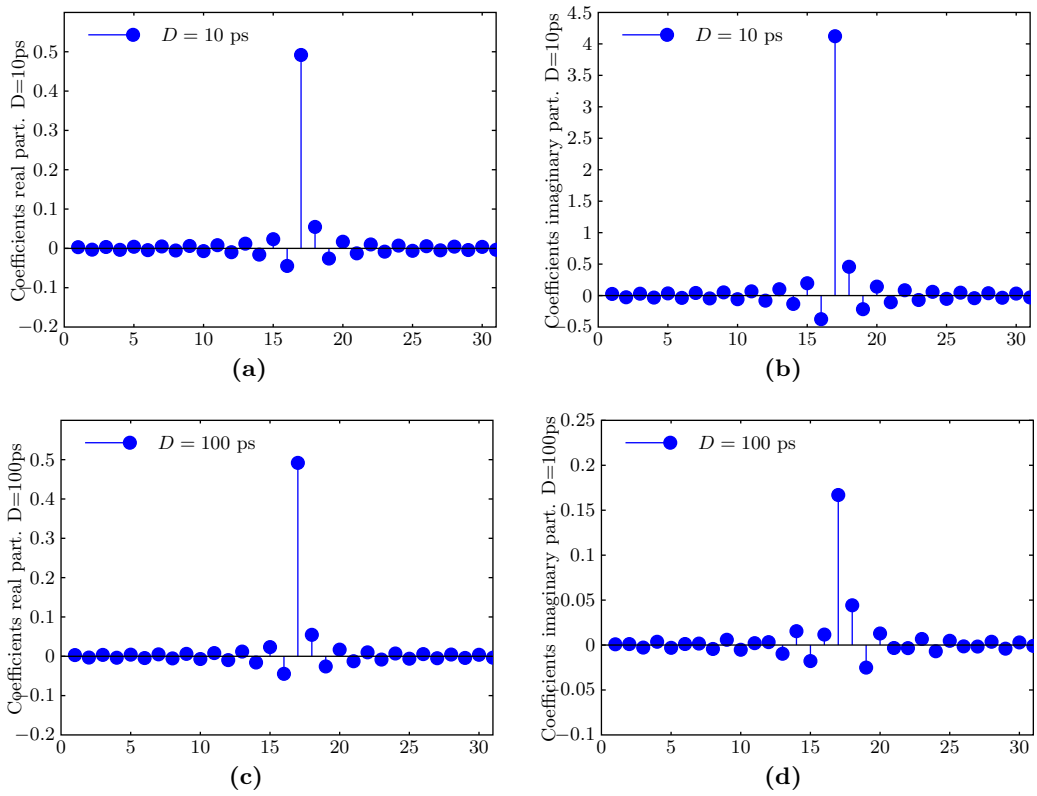


Figure 6.18: Influence of the value of D on the magnitude of the first FIR coefficients.

part (right subfigures). These results strongly suggest that it's safe to ignore the continuous interpolants after $n_w = 30$ taps. The same conclusion will be reached later by simulations.

By analyzing Fig. 6.18 and Fig. 6.18 one can observe another important aspect: the effects of the value of the delay D on the magnitude of the interpolants coefficients. We have shown in Section 6.4, relation 6.12, that the optimal value for D is $D = 1/(4f_c)$ (here $= 1/(4 \cdot 1890[\text{MHz}]) = 132$ ps). Indeed, we can see in Fig. 6.18 and 6.18 that as D is set further from the optimal value the magnitude of the FIR taps rises. In fact, for the value $D = 10$ ps the coefficients are almost 10 times larger than for the value $D = 100$ ps. This aspect will affect the cost of the practical implementation as larger values of the coefficients require more digits and more taps.

The previous results show that two complex coefficients FIR filters are sufficient for a reasonable implementation of the continuous PNS2 interpolants. Nonetheless, it is good idea to set the delay between the two channels as close as possible to the optimal value, in order to further reduce the implementation cost.

In the following, we realize an analysis of the frequency response of the two complex coefficients filters. Fig. 6.20 plots the frequency response of the first FIR filter when no windowing is used. Fig. 6.21 the frequency response of the same filter when a Kaiser window with a $\beta = 6$ parameter is used. The Kaiser window minimizes the effects of truncation by smoothing the frequency response.

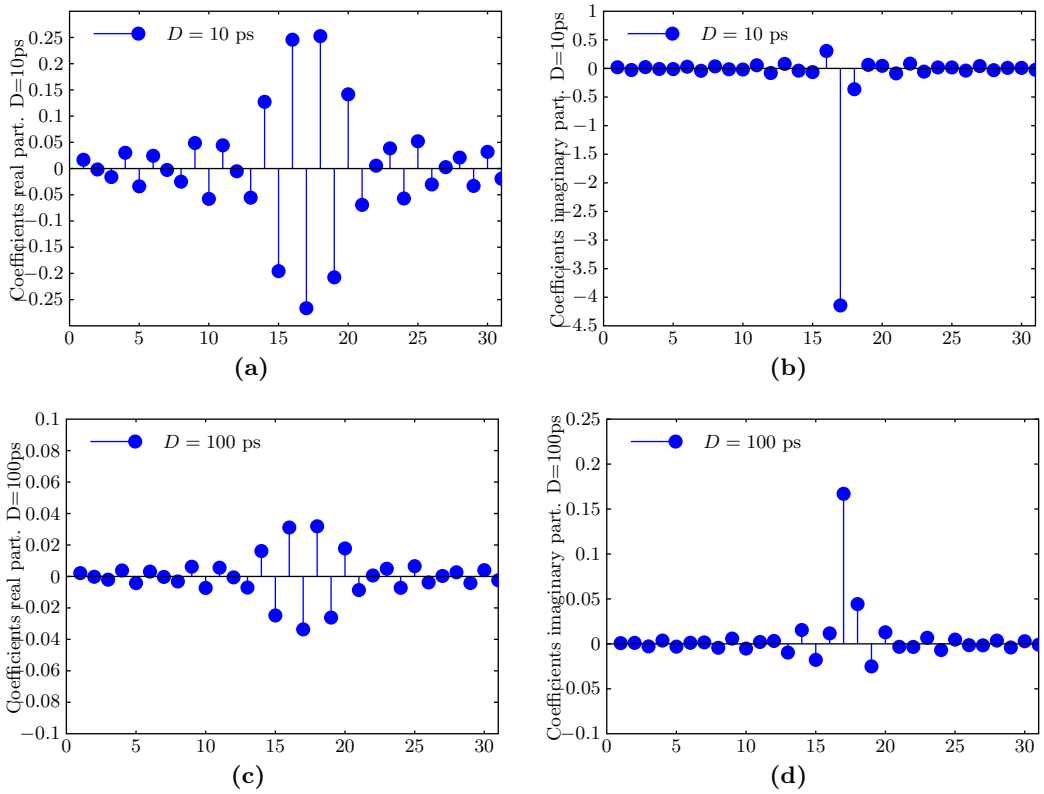


Figure 6.19: Influence of the value of D on the magnitude of the second FIR coefficients.

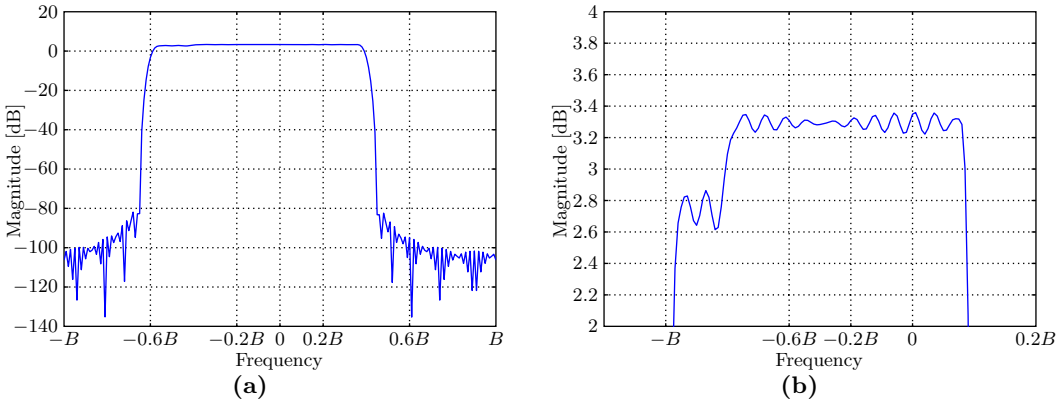


Figure 6.20: Frequency response of the first interpolant when no Kaiser windowing is used

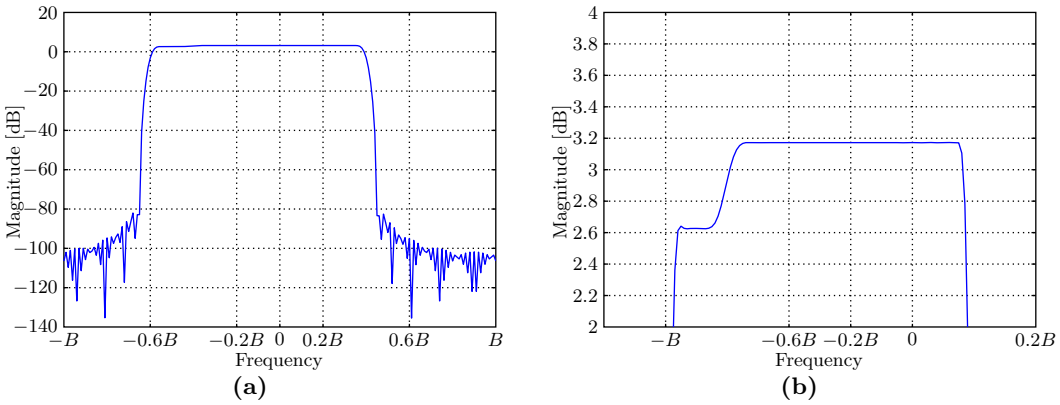


Figure 6.21: Frequency response of the first interpolant when a Kaiser window with a $\beta = 6$ parameter is used

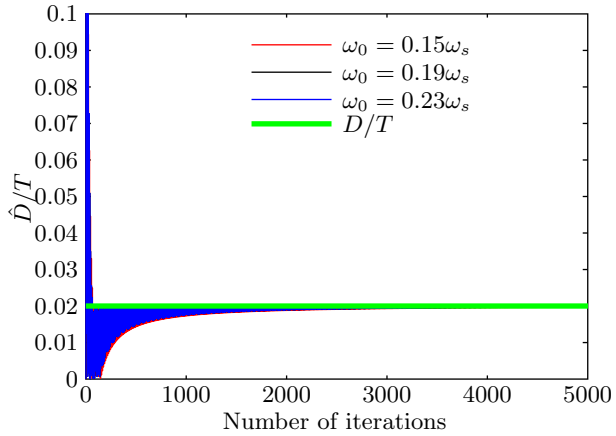


Figure 6.22: Time-skew estimation over time. It can be observed that the estimations $\hat{D}/T$ converge to ideal value of D/T every time. However the quality of the estimation peaks when $\omega_0 = \omega_s/4$ and worsens at higher input frequency.

6.6.4 Analysis of Time-Skew Detection Techniques

This section provides the simulations of the two time-skew detection techniques presented in Section 6.4.4. In the end, a detailed comparison and our conclusions are presented.

For this part, the test circuit from Figure 6.7 is composed of two 10-bits ADC, each one operating at $B = 1/T = 100$ MHz. For now, we consider that the clock generator is ideal and that there are no gain or offset mismatch between the two ADCs. For these values of f_c and B, the first forbidden value for D is $T/(k+1) = 263$ ps. Therefore, delay D is fixed to 100 ps ($D/f_s = 2d/T = 0.02$).

6.6.4.1 Sinusoid-Based Time-Skew Detection Technique

To evaluate the performances of the first time-skew detection technique presented in Section 6.4.4.2, several simulations for different values of $\omega_0 \in [0.15\omega_s, 0.23\omega_s]$ were carried out. Fig. 6.22 shows the estimation $\hat{D}/T$ over time as obtained from the output $\bar{\epsilon}$ of the time-skew detector presented in Fig. 6.9 and from Eq. 6.21 for several values of ω_0. It can be observed that the estimations $\hat{D}/T$ converge to ideal value of D/T every time.

From now on, for each ω_0 only the last estimation $\hat{D}$ will be kept and analyzed. Table 6.1

Table 6.1: Time-skew estimation analysis

	$\lvert\hat{D}-D\rvert$	$\lvert 1-\hat{D}/D\rvert$	$\varepsilon(\hat{D})$
$\hat{D}=D$	0	0 %	1.2%
$\omega_0=0.15\omega_s$	3.2 ps	3.2%	2.9%
$\omega_0=0.19\omega_s$	1.2 ps	1.2%	1.8%
$\omega_0=0.23\omega_s$	0.3 ps	0.3%	1.3%

presents a more detailed analysis of the results. Three metrics of interest are calculated. The second column represents the absolute difference between the value of D and the estimation $\hat{D}$, while the third column shows the relative differences between the same variables.

Because the estimated value of D will be used for PNS2 reconstruction, a much more useful metric is similar to the cost function defined in Section 6.4.4.3:

$$\varepsilon(\hat{D})=\frac{\sum_{i=n_w/2}^{N+n_w/2}(\hat{f}[i,\hat{D}]-\tilde{f}[i,D])^2}{\sum_{i=n_w/2}^{N+n_w/2}\tilde{f}[i,D]^2} \tag{6.43}$$

where $\hat{f}[i,\hat{D}]=f[iT+T/2+\hat{D}]$ is the reconstructed value and $\tilde{f}[i,D]$ the measured valued of the sample $f[iT+T/2+D]$.

$\varepsilon(\hat{D})$ is a measure of how close to $\tilde{f}(i,D)$ is the reconstruction $\hat{f}(i,\hat{D})$. In order to calculate this metric, we chose $N=1000$ values and we calculated $\hat{f}(i,\hat{D})$ using Eq. 6.23 and then the metric $\varepsilon(\hat{D})$ is calculated using Eq. 6.43. This metric is presented in the fourth column of Table 6.1.

As proved in Section 6.4.4.2, the digital time-skew detection technique manages to offer a good estimate for D. Moreover, the estimates, $\hat{D}$ for the last two rows in Table 6.1 satisfy the requirements imposed by Eq. 6.13 and Eq. 6.14. This means that, because $\Delta D=D-\hat{D}<2$ ps, the expected estimation error is around 1%.

It can be seen from the Table 6.1 that the sensitivity of time-skew detection increases as ω_0 approaches $0.25\omega_s$. Finally, one can note that this detection technique is sensitive to the value of ω_0, as expected, which is a drawback.

6.6.4.2 LMS-Based Time-Skew Detection Technique

In order to apply the LMS algorithm presented on the Page 98, the signal presented in Fig. 6.17 is used to excited the BIST circuit. The same values for the delay, $D=100$ ps and ADCs sampling speed $B=100$ MHz are kept. For these values, the cost function $J(\hat{D})$ should have only on minimum in the interval $]0,\frac{1}{k^+B}[=]0,263$ ps[.

Fig. 6.23 plots the cost function $J(\hat{D})$ versus several values of $\hat{D}$ in this interval. As expected, the cost function has only one minimum that appears when $\hat{D}=D$. The cost function was calculated using $N=50$ points. In all simulations the reconstruction filter has 21 taps ($n_w=20$) and is windowed by a Kaiser window. It is considered that the ADCs are not affected by any other mismatches.

The two monovariable LMS algorithms are then run for several values of $\hat{D}^0$ spaced between $\hat{D}^0\in]0\text{ps},260\text{ps}[$. The initial value for μ was chosen equal to 10e-12. Fig. 6.24 plots the evolution of cost function for several values of $\hat{D}_0$. The fixed step size algorithm is presented in

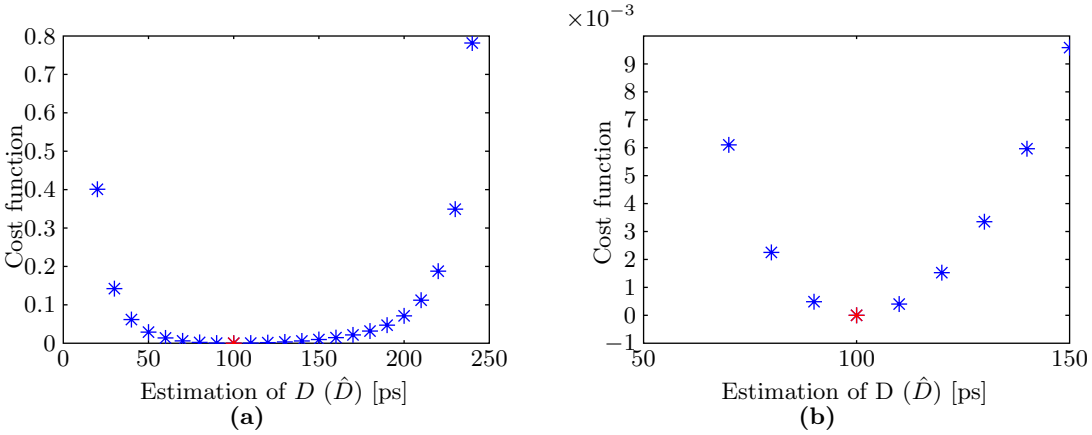


Figure 6.23: Cost function for several values of $\hat{D}$. Fig. 6.23b plots a zoom of the left figure around $\hat{D} = D$

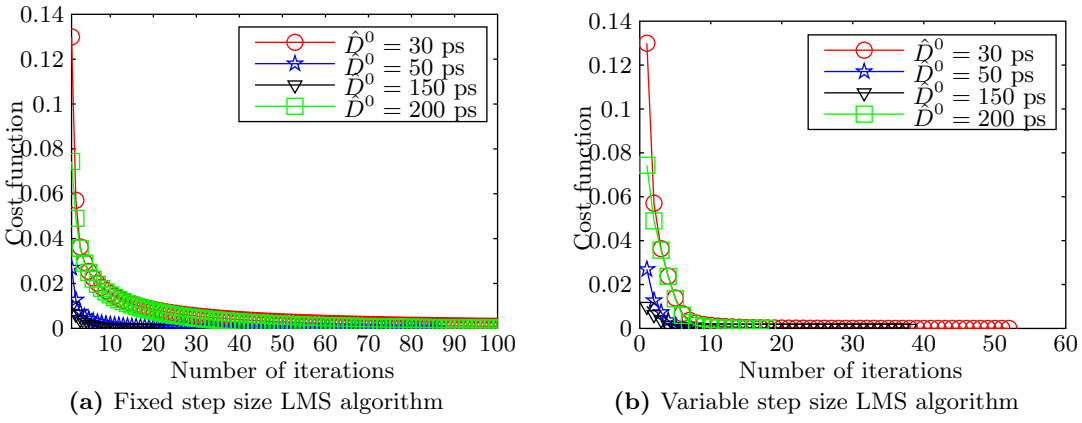


Figure 6.24: LMS algorithm: evolution of cost function for several values of $\hat{D}_0$

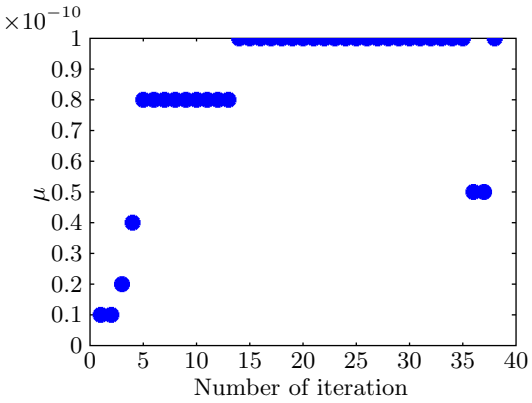


Figure 6.25: Evolution of the step size parameter for an initial value of $\hat{D}^0 = 150$ ps

Fig .6.24a. The algorithm is able to accurately estimate D and converges, every time. However, the convergence time is large. For $\hat{D} = 30$ ps it goes beyond 400 iterations. This makes the estimation process lengthy and thus costly for calibration purposes. Furthermore, the dynamic of the convergence depends strongly on the initial estimate and the value of the step size μ.

Therefore, we moved to the variable step size LMS algorithm. Fig. 6.24b plot the evolution of the cost function for several values of $\hat{D}_0$ when the variable step size algorithm is used. The following parameters have been used:

$$\begin{aligned} \mu^0 &= 10e-12 \\ \mu_{min} &= 0.1e-12 \\ \mu_{max} &= 100e-12 \\ \rho_0 = \rho_1 &= 2 \end{aligned}$$

One should note the correlation between the values of μ and the values of $\hat{D}$ which made it easier to choose good starting values. This is made possible because we use a normalized gradient.

Again, the algorithm is able to accurately estimate D and converges, every time. As we expected, it can be noticed the algorithm converges faster than the fixed step size previously presented. The evolution of the step size parameter for an initial value of $\hat{D}^0 = 150$ ps is presented in Fig. 6.25.

6.6.4.3 Comparison between the two algorithms

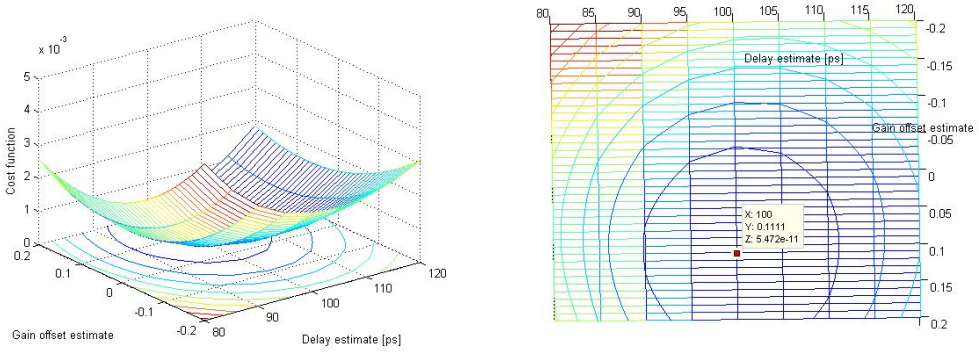
The performance of the LMS-based technique is summarized in Table 6.2. For a fair comparison, the same three metrics as before are calculated: the absolute (second column) and the relative (third column) difference between the real D and its estimated value, and the normalized relative error between the real signal and the reconstructed values (fourth column). The first two rows recall the results obtained with the previous technique for two values of ω_0. The last two rows present the results of the LMS-based technique for two values of $\hat{D}_0$.

It can be seen that both techniques offer good estimates of D, but the first technique is sensitive w.r.t. the frequency of the input test signal ω_0. The LMS-based technique we propose performs better, doesn't need known test signal, and extracts the time-skew between two ADCs in a robust way. In addition, our LMS technique offers a robust mechanism to stop the algorithm when the needed performance are met.

Between the fixed step size LMS and the variable LMS it is clear that the later is faster at the cost of a more costly implementation (up to 30%). Nonetheless, the fixed step size LMS

Table 6.2: Comparative time-skew estimation analysis

	$\lvert\hat{D}-D\rvert$	$\lvert 1-\hat{D}/D\rvert$	$\varepsilon(\hat{D})$
$\omega_0 = 0.3B$	3.2 ps	3.2%	2.9%
$\omega_0 = 0.46B$	0.3 ps	0.3%	1.3%
$\hat{D}_0$=50 ps	< 0.1ps	<0.1%	0.84%
$\hat{D}_0$=150 ps	< 0.1ps	<0.1%	0.84%



(a) **(b)**

Figure 6.26: Cost function $J(\hat{D}, \widehat{\varepsilon_G})$ for several values of $\hat{D} \in [80\,\text{ps}, 120\,\text{ps}]$ and $\widehat{\varepsilon_G} \in [-0.2, 0.2]$

could be a good choice if we trust the initial estimate of the delay D (which we expect to be the case for the hardware implementation).

6.6.4.4 Multivariable LMS Algorithm

Let's now consider that the ADCs composing the BIST architecture are affected by a mismatch varying between $\varepsilon_G \in]-20\%, 20\%[$. In this section we aim to prove that the multivariable LMS algorithm is able to correct the gain mismatch. We use the same simulation parameters as in the monovariable LMS algorithm, except for the gain mismatch which is considered here to be $\varepsilon_G = 11\%$.

The cost function $J(\hat{D}, \widehat{\varepsilon_G})$ for several values of $\hat{D} \in [80\,\text{ps}, 120\,\text{ps}]$ and $\widehat{\varepsilon_G} \in [-0.2, 0.2]$ is presented in Fig. 6.26. Fig. 6.26b represents a projection of the cost function on the 2D space determined by $\hat{D}$ and $\widehat{\varepsilon_G}$. We can notice that the cost function has only one minimum that appears when $\hat{D} = D$ and $\widehat{\varepsilon_G} = \varepsilon_G$. This shows that simultaneous estimation of the two parameters can be carried out by an LMS algorithm, such as the one presented in Section 6.4.4.4, on Page 102.

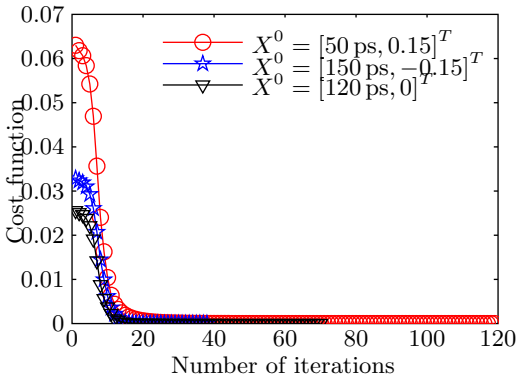
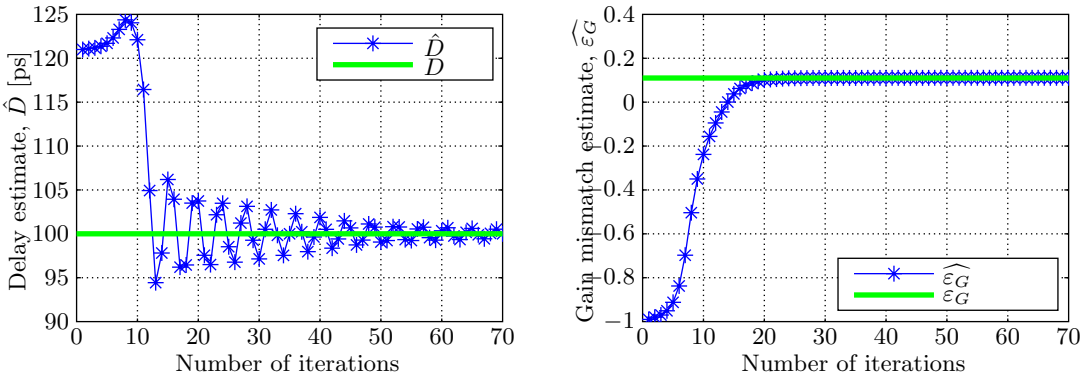


Figure 6.27: Multivariable LMS: evolution of the cost function for several value of X^0



(a) Delay estimate evolution

(b) Gain mismatch estimate evolution

Figure 6.28: Multivariable LMS: evolution of the estimates X

A variable step size MLMS is then run with the following initializations parameters:

$$\begin{aligned} N &= 50 \\ W^0 &= \begin{bmatrix} 2e-12 & 0 \\ 0 & 0.01 \end{bmatrix} \\ \rho_0 = \rho_1 &= 2 \\ \mu_{D,min} &= 0.1e-12 \\ \mu_{D,max} &= 100e-12 \\ \mu_{\varepsilon,min} &= 0.005 \\ \mu_{\varepsilon,max} &= 0.25 \end{aligned}$$

Fig. 6.27 depicts the evolution of the cost function for several initialization points, X^0. We observe that the algorithm converges every time. For an initial value of $X^0 = [120\,\text{ps}, 0]^T$ the evolution of the delay and the gain mismatch is presented in Fig. 6.28. We see that the MLMS algorithm is able to estimate the two parameters with under-ps precision for the delay D and very good precision for the gain mismatch ($< 1\%$). Compared to the monovariable LMS, the algorithms needs more iterations to converge.

6.6.4.5 Conclusions and Perspectives

In this section, we saw that the PNS2 reconstruction can be carried out even if some uncertainties affects the BIST architecture. We have evaluated two techniques to estimate the delay between

the channels, which is a vital parameter in PNS2 reconstruction. Furthermore, we've extended the LMS algorithm so it can take into account another inescapable imperfection in the BIST architecture: the gain mismatch.

We concluded that the LMS algorithm performs better, is more robust and supports a relatively simple digital implementation. So we decided to use it for all future improvements and development.

6.6.5 ACPR Simulation

Up to this point we discussed a digital implementation of the PNS2 reconstruction technique. We, then, proposed and analyzed several strategies to improve the robustness of the proposed algorithm against uncertainties in the test architecture. However we have not yet evaluated the limitation imposed by the analog sampling block. In this section we analyze these aspects and investigate the overall performance of the BIST architecture.

We decided to quantify the performance of the entire BIST system by the means of Adjacent Channel Power Ratio (ACPR). ACPR is a pertinent figure of merit as it quantifies the effect of nonlinear distortions and is commonly published for every digital transmission system. ACPR is sensitive to any imperfections in (noise, distortion, etc.) introduced by the added high-speed samplers.

The test signal is a WCDMA signal, frequently used in modern digital communications. It occupies a 5 MHz band at $f_c = 1890$ MHz and it has the power frequency spectrum depicted in Fig. 6.17.

6.6.5.1 Impact of Fixed-Point Implementation of the FIR Coefficients

First, we analyze how the FIR implementation affects the performance of the proposed BIST strategy. The FIR are implemented as described in Section 6.6.3. A Kaiser windows with β parameter of 6 has been used to minimize the effects of truncation.

Fig. 6.29 shows the evolution of ACPR estimate w.r.t. number of taps n_w of FIR filters for different values of the delay D. First, it can be noticed that the precision of the reconstruction depends on the value of D. These results support the discussions presented in Section 6.4, where it is shown that the optimal value of D is $D = 1/(4f_c)$ (in this case $D = 132$ ps). However, one can notice that we have a large margin of choosing D, Finally, Fig. 6.29 shows that $n_w = 20$ taps is a good trade off between complexity and performance.

For $D = 100$ ps and $n_w = 30$ taps we used Matlab toolbox *Fixed Precision* to simulate the fixed point implementation. Fig. 6.30 plots the ACPR degradation w.r.t. to the FIR taps precision. The results prove that 12 bits of precision are enough for implementing the PNS2 reconstruction. This value will be used for the rest of the simulations.

6.6.5.2 Clock-Jitter Effect

The previous simulations were ran considering that the clock generator is ideal (not affected by jitter) and the S/H blocks are ideal voltage samplers. In the following we present the effect of jitter on the two BIST architectures. Fig. 6.31 shows the evolution of the ACPR degradation w.r.t. jitter of clock generator. The graphic shows that the BIST architecture is really sensitive to clock generator jitter. However, the charge sampling based architecture is much more robust than the voltage sampling based architecture. Even, when no jitter is involved the performance is better (this is due to the extra-filtering provided by the charge-sampling amplifier).

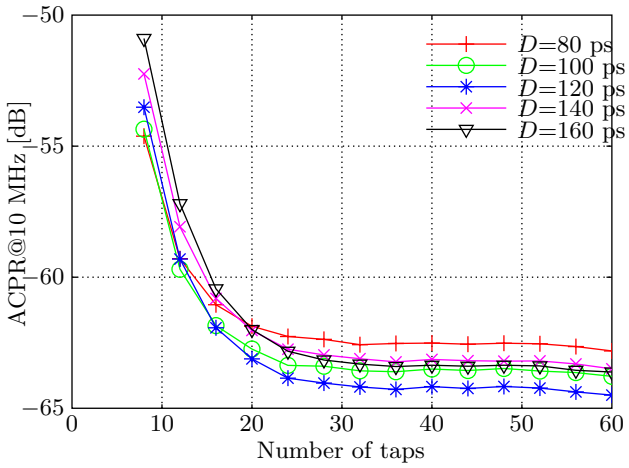


Figure 6.29: Evolution of the ACPR estimate w.r.t. the number of taps in FIR implementation and the value of D

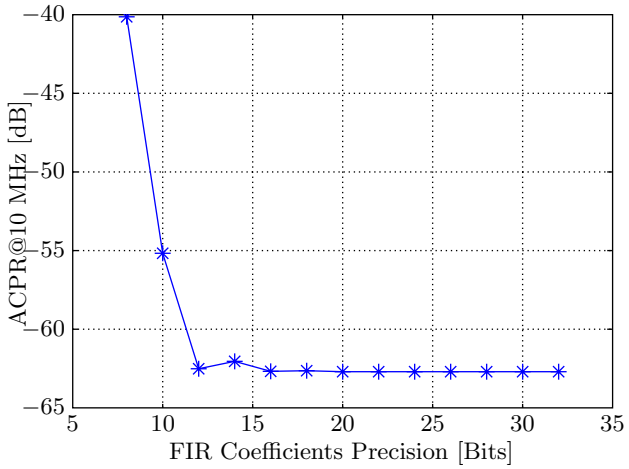


Figure 6.30: Evolution of the ACPR estimate w.r.t. FIR filters taps precision

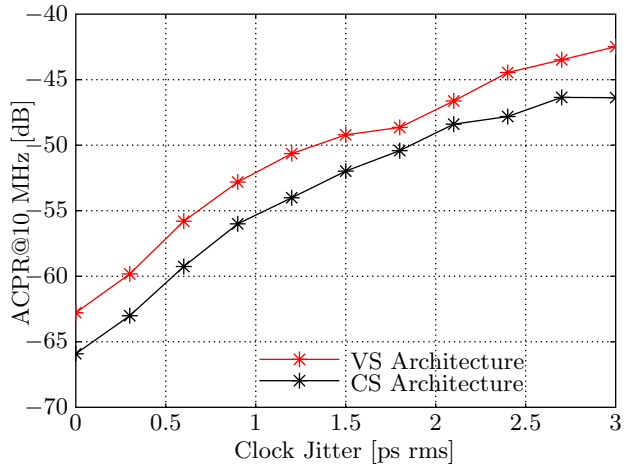


Figure 6.31: Evolution of the ACPR estimate w.r.t. jitter in the clock oscillator

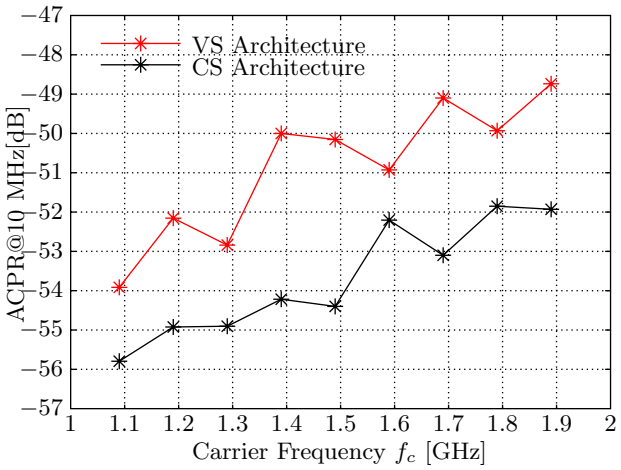


Figure 6.32: Evolution of the ACPR estimate w.r.t. carrier frequency

6.6.5.3 Remarks

Let's consider for the example the 3GPP [Standard, 2013] standard that specifies ACPR values below -50 dBc at +/- 10 MHz. That means the VS-based BIST architecture should be able to check compliance with the standard for clock jitter values up to 1.2 ps rms while the CS-based can still guarantee compliance at @2ps rms clock jitter values. These results are indeed interesting considering that existing fixed-frequency clock generators can provide low-jitter signal (<1 ps rms) at relatively low-cost (see the CDC421AXXX [Texas Instrument] family proposed by Texas Instrument).

Finally, for a clock jitter value of 1.5 ps rms we studied the evolution of ACPR for different values of the carrier frequency in Fig. 6.32. As expected, it can be noticed that the performance of the BIST architecture decrease as the test signal frequency increases. Also, one can notice that the CS-based BIST architecture performs better along the entire range of frequency. It is interesting to remark this last simulation because it shows the flexibility of the proposed test architecture. Indeed, in order to change the frequency operating point of the scenario, it suffices to update the filters taps and the delay D.

6.7 Conclusions

In this chapter we introduced a novel Built-In Self-Test strategy designed for the test/characterization of the output stage in a multistandard radio. The BIST architecture acts like an auxiliary receiver and is designed to address the fault-masking situation which affects the classic RF loopback test. The strategy is based on Periodically Nonuniform Sampling of second order and targets spectral mask estimation (ACPR estimation) at the output of the TX for any mode of operation and architecture. We proposed different implementations depending on how the sampling process is carried on: a voltage-based implementation and a charge-based implementation. The VB BIST implementations places stringent requirements on the added undersampling circuitry, and suffered from jitter in the two clock signals driving them. The second implementation, lessens these burdens by means of charge-domain sampling. These architectures are compared, and simulation results demonstrate that charge-based sampling solution performs better and is more tolerant of clock jitter.

We also show the impact of truncation errors arising out of the use of fixed-point operations in the computations of the complex finite impulse response (FIR) filters utilized to reconstruct

the waveforms using PNS2. We concluded that the cost of implementation is reasonable. Afterwards, we introduced two algorithms designed to estimate different uncertainties in circuitry, such as delay uncertainty and gain mismatch.

Finally, we performed a comparison between the two architectures, VBS and CBS, for ACPR estimation over a large frequency range. Our results demonstrate that charge-domain sampling always yields better results than voltage-domain sampling.

The proposed test strategy proves to be flexible and robust, provides in-field test capabilities, and it supports a simple hardware implementation, aspects that are essential for any SDR test strategy.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

This dissertation addresses the challenges in the field of RF and SDR test. An SDR is a Radio in which some (or all) of the physical layer functions are programmable. The outstanding flexibility and performance of these radios hinders the testability of the finished units. Established mixed-signal and RF test strategy are either too time-consuming (thus costly) or can't ensure compliance with several modulations standards, including those yet to appear. New test strategies must be invented, able to cover thoroughly and efficiently all key specifications of the radio unit. In this context, our research aims to invent and develop a new test methodology able to guarantee the correct functioning of the SDR platform post-manufacture and over its operation lifetime.

The presented study was carried out in two steps. The first step consisted in a extensive bibliographical research on the topic of RF testing and SDR architectures. The complexity of an SDR platform helped us to understand the challenges faced by the test engineers. The multitude of the figures of merit that define an SDR represents another factor that has to be considered and that was discussed here. For RF systems, Built-In Self-Test schemes are arguably the only way to ensure continued compliance to specifications. We presented the most promising RF BIST techniques for commercial transceivers. Most of them are not suitable for the test of flexible radios. However, the loopback approach caught our attention because of its simplicity and potential to be used as a low-cost test strategy. Nonetheless, it suffers from one major drawback: fault-masking. Fault masking arises because RX and TX faults are not observable separately.

In a second step, we introduced and discussed a novel Built-In Self-Test strategy designed for the test/characterization of the output stage in a multistandard radio. The BIST architecture acts like an auxiliary receiver and is designed to address the fault-masking situation which affects the classic RF loopback test. The strategy is based on Periodically Nonuniform Sampling of second order and targets spectral mask estimation (ACPR estimation) at the output of the TX for any mode of operation and architecture. The proposed test scheme can also handle less demanding measurements, such as IP3, gain, and I/Q imbalance without any hardware modifications, using existing signal processing algorithms.

We proposed different implementations depending on how the sampling process is carried on: a voltage-based implementation and a charge-based implementation. The VB BIST imple-

mentations places stringent requirements on the added undersampling circuitry, and suffered from jitter in the two clock signals driving them. The second implementation, lessens these burdens by means of charge-domain sampling. These architectures are compared, and simulation results demonstrate that charge-based sampling solution performs better and is more tolerant of clock jitter.

For digital PNS2 reconstruction, the main obstacle is to have an accurate estimate of an incrementally controlled delay element. We introduced an LMS-based estimation algorithm that addresses the uncertainties in our BIST architecture: time delay and gain mismatch. Our algorithm solves these issues robustly and opens the road for a complete self-calibrating BIST architecture.

The proposed test strategy proves to be flexible and robust, provides in-field test capabilities, and it supports a simple hardware implementation, aspects that are essential for any SDR test strategy.

7.2 Future Work

Extensive simulations show the feasibility and the potential of the proposed technique. In consequence, one of the most important perspectives is to experimentally validate the proposed test architecture on an SDR testbed designed by Thales Communications & Security. We already started to look for the components of the future BIST architecture.

Another aspect, that was just briefly discussed in this report, is the possibility to extend the BIST architecture by developing a fully self-tested self-calibrated loopback test. The key idea is the statistical analysis of the dynamics of the BIST during the LMS algorithm. This analysis could provide valuable information about the functionality of the PNS2 subsampler. However, further investigations are needed.

The LMS-based calibration algorithm can also be further improved by taking into account new mismatches and nonidealities.

Replacing the voltage-based samplers with charge-domain samplers was a step forward for the performances of the BIST strategy. Our choice for the simplest charge-domain sampler architecture was determined by the need to have a simple BIST circuitry. Nonetheless, it is worth to take a look into the research Poberezhskiy and Poberezhskiy [2009, 2005]; Karvonen et al. [2005] where more complex charge-domain samplers are presented. Adopting a more complex charge sampler would be motivated by possibility to integrate an antialising filter in the BIST circuitry itself. The price for this feature is, however, a complicate design, which should be avoided by a BIST architecture.

Testing and calibration of RF transceivers are strongly correlated. And the calibration is an essential step in today digitally assisted TX. A lot of research was done in this direction and a multitude of algorithms for power amplifier linearization have been proposed [Staszewski et al., 2008; Staszewski, 2011; Staszewski et al., 2007; da Mota and da Silva, 2011]. However, these researches focus more on the digital algorithms to realize the linearization and less on the feedback path required to route the signal of interest from the output of the PA to the DSP unit. For this step, they typically obtain parameters correlated to the signal of interest and not a true performance measurement. For example da Mota and da Silva [2011] uses a power detector while Bashir et al. [2005] employs an internal digital signal to calibrate an all-digital PLL-based transmitter. Our proposed BIST architecture can be used without any further modifications as the feedback path for any of the previous calibration algorithms. Even more, the performance of these algorithms are expected to increase as the characteristics of the PA are measured and not estimated.

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