Conception de circuits analogiques et numériques avec des transistors organiques flexibles

Miguel Angel Torres Miranda

Thèse de Doctorat de

l'Université Pierre et Marie Curie

École Doctorale Informatique, Télécommunications et Électronique (EDITE)

Présentée par :

Miguel Angel TORRES-MIRANDA

Pour obtenir le grade de :

Docteur de l'Université Pierre et Marie Curie

Sujet de la thèse :

Conception de Circuits Analogiques et Numériques avec des Transistors Organiques Flexibles

Date de soutenance : **1er Septembre 2015**

Le jury est composé de :

M. Hamid Kokabi	Président du Jury
M. Boris Murmann	Rapporteur
M. Hagen Klauk	Rapporteur
M. Lionel Hirsch	Examinateur
Mme. Barbara Stadlober	Examinatrice
M. Franck Wajsburt	Examinateur
M. Yvan Bonnassieux	Co-directeur de Thèse
M. Hassan Aboushady	Directeur de Thèse

Design of Analog & Digital Circuits using Flexible Organic Electronics

A dissertation by:

Miguel Angel TORRES-MIRANDA

Submitted to obtain the PhD degree from:

Université Pierre & Marie Curie (UPMC)

Defense date: **September 1st, 2015**

Committee in charge:

Mr. Hamid Kokabi	UPMC, France
Mr. Boris Murmann	Stanford University, U.S.A
Mr. Hagen Klauk	Max Planck Institute, Germany
Mr. Lionel Hirsch	University of Bordeaux, France
Mme. Barbara Stadlober	Joanneum Research, Austria
Mr. Franck Wajsburt	UPMC, France
Mr. Yvan Bonnassieux	Ecole Polytechnique, France
Mr. Hassan Aboushady	UPMC, France

Acknowledgements

I would like to thank my advisor Hassan Aboushady and co-advisor Yvan Bonnassieux for their time and their technical advices during my thesis.

I would like to thank the doctoral school EDITE: École Doctorale Informatique, Télécommunications et Électronique of Université Pierre et Marie Curie for funding this thesis work during 3 years. I was also partly funded by the European Institute of Technology (EIT), ICT Labs as a part of a program of Innovation and Entrepreneurship for PhD Candidates across Europe. I received several fundings, notably the one who allowed a research internship resulting in a collaboration (chapter 4 and 6) with the group of Dr. Barbara Stadlober, Joanneum Research, Weiz, Austria.

I would like to thank A. Al-Mutairi for his collaboration in the fabrication steps with the Orgatech Technology, Dennis Tondelier for his technical advices with the OTFT fabrication by shadow masks, Chang-Hyun Kim for his advices with modeling the experimental curves and the ORGATECH team at LPICM for the realization of a part of the experimental part in their facilities.

I would like as well to thank Andreas Petritz, Alexander Fian, Christine Prietl for helping me in the fabrication of the samples by photolithography, Herbert Gold for the mask layout design and the colleagues of the group of Micro and Nanostructuring of the Materials Department in the Joanneum Research center in Weiz, Austria, especially to Dr. Barbara Stadlober for being invited and funded for the realization of the experimental part in their facilities and the sample fabrication.

A big thank to Franck Wajsburt of LIP6/UPMC for his time and collaboration with the development of the Alliance CAD tools for the OTFT Technology.

I would like to thank as well Denis Crété of the Unité Mixte de Physique CNRS/Thales, Palaiseau, France and Jean-Charles Vanel of LPICM, Ecole Polytechnique, Palaiseau, France for helping him in the measurement process of the plastic circuits.

I would like to thank also to the master student Joao Cabral for his technical collaboration on the system level design of a sigma delta modulator and to all of the master students and colleagues at LIP6 which I work with during the thesis.

Finally I would like to thank my family and friends in Panama and in France for their patient and time during my long three years of thesis.

Miguel Angel TORRES-MIRANDA

Contents

List of Figures

List of Tables

Part I

Introduction to Electronics with Organics and Flexible Materials

1

Introduction

1.1 Introduction

Electronics circuits and sensors using flexible materials is the next big revolution in the large fields of materials, devices and information technology due to its low cost fabrication process and its compatibility with stretchable, conformal and biological materials.

In the era of “Internet of Things”, conventional expensive, bulky and rigid silicon is not the only answer for sensor interfaces. Electronic devices based on flexible materials are an interesting approach to interface with sensors connected to our everyday life, e.g.: clothes, packages, skin and into the human body.

In this thesis, we propose a formalization of the:

- Transistor fabrication process using organic and flexible materials.
- Analog and digital circuit design using these transistors.

The main contribution of this work can be summarized in the following:

- A design kit for two technologies: the first by shadow masks with an easy-to-fabricate procedure, the second by self-alignment and photolithography.
- Modeling and parameter extraction for process variation aware analog design.
- Customization of an open source VLSI CAD tools (Alliance©) for circuit design and layout of OTFT.
- Design, fabrication and measurement of OTFT analog front-ends (Voltage amplifiers, Comparators, Analog-to-Digital Converters) and basic digital circuits (Inverters, Logic Gates).

1.2 Outline

The thesis report is divided in 8 chapters of content and a final chapter of conclusion and perspectives. In this first chapter we present a brief summary of what is the subject about and the outline of each chapter.

Chapter 2 presents the motivation of this work, a summary of basic concepts not treated in the subsequent chapters and an extensive description of the State of the Art in the different fields of research involving devices with flexible and organic materials.

Chapter 3 presents a detailed description of one of the two technologies optimized in this work: Organic Thin Film Transistors (OTFTs) fabricated by means of thermal evaporation and shadow masks at Orgatech in LPICM/Ecole Polytechnique, France. An extraction of the parameters of several fabricated OTFTs is shown. The adapted a-Si TFT Spice Model present in commercial simulators is used to model the transistors. A mismatch model will be presented with an statistical analysis.

Chapter 4 presents the description of the second technology presented in this work and developed at Joanneum Research, Austria: OTFTs with channels patterned by contact photolithography and self-alignment of source and drain with the gate. An optimization of several process parameters is presented such as the dielectric thickness, the semiconductor layer and a reduction in the contact resistance. Finally, those parameters were extracted and the transistors modeled with the a-Si TFT Spice model as well.

Chapter 5 presents the design of different analog basic blocks with the OTFTs based on the adapted model presented in chapter 2 and 3. The simulation results of different analog basic blocks with the technology developed in chapter 3 and 4. An amplifier, a comparator and a sigma delta modulator are designed using few OTFTs. A comparison among them and with the state of the art is done.

Chapter 6 presents the measurement of several analog and digital circuits in order to evaluate the performances of the Joanneum Research technology presented already in chapter 4. Good circuit performances such as gain, bandwidth, power consumption and functional signals will be shown.

Chapter 7 presents the design of the layout of the sigma delta modulator developped in chapter 5, with the tools of a free and open source CAD system, Alliance ©. Simple standard circuit cells from the designed analog blocks will be shown.

Chapter 8 shows finally the conclusion of this work with the different results and a perspective of the future works in both groups.

2

Problem Definition and Motivation

2.1 Introduction

The Age of Internet of Things is here and is demanding us computational capability everywhere at anytime. Conventional silicon electronics has improved our lives in the last 40 years, however it has also arrived to a challenging period where people do not need only ultra low power and ultra fast devices, but also a close interaction with the technology. Bulky and rigid devices cannot accomplish these tasks because almost all of the objects around us, and moreover the human body are not hard but soft, conformal and mechanically dynamic. Electronics devices fabricated with flexible and stretchable materials looks forward to fill this gap. However the research field is also very challenging due to the lower electrical performances of the plastic materials compared to the crystalline semiconductors. It is necessary, as well, to differentiate both technologies not as competitors but as complementaries for the benefit of our everyday life.

Devices on plastic materials could be fabricated with organic and inorganic thin films deposited on top of a flexible substrate. Inorganic materials have better electrical properties because of the high temperature (and hence polycristalline structure) deposition process, however the most important disadvantages are the complex and expensive fabrication procedures which after all, make them a worse choice for commercialization. Organic materials on the contrary have at the moment of this thesis, lower performance properties than inorganic ones, however they could be deposited with low temperatures procedures, such as printing methods which makes a more interesting approach from an economic point of view. In fact, the possiblity of manufacture devices at a large scale and in large surfaces by conventional industrial process such as Roll to

Roll (R2R) and Sheet to Sheet (S2S) printing make organic thin film devices a better solution than inorganic ones. However some drawbacks need to be overcome to attain an industrial level of production compared to silicon electronics, for example the reliability of the devices, the increase in the amount of data driven and the decrease in the energy consumption.

In the last two decades, recent developments have shown the potential of these flexible devices which will be summarized in section 2.5. These connected devices with sensors on flexible materials need as well, signal treatment with at least a minimum of circuits serving as primary interfaces between them and a conventional electronic system. The state of the art in these basic signal treatment circuits will be shown in section 2.4. The OTFTs which are the base for those circuits and their models will be introduced in sections 2.3 and 2.2. A simple introduction to the manufacture process of those OTFTs is presented in the next section 2.1.1. Finally the principal contributions of this thesis work are presented in section 2.6.

2.1.1 Technology Process

In order to manufacture circuits and systems, sensors and transistors are needed for the signal treatment. A thin film transistor (TFT) is an stack of layers each one with an electrical property. In this work, a conventional Field Effect Transistor (FET) structure is fabricated with a gate electrode, a dielectric as a buffer layer, a semiconductor as the active layer, and 2 contacts to manage the charge carrier injection to the semiconductor layer. Each of these layers could be deposited by different methods: thermal evaporation, spin-coating, ink-jet printing, among others.

There are four basic OTFT structures presented in Fig. 2.1, explained in detail in [1] depending on the position of the gate and the contacts. In general when fabricating the transistor by shadow masks or photolithographic procedures it is important to reduce the overlap capacitances of the source and drain contacts with the gate. Therefore the gate is deposited as the first layer and then the rest of them, taking care to align the source and drain contacts with it.

The contact separation defines the channel length and its interface with the semiconductor determines the injection of charge carriers in the channel. As explained in [2], the contacts over the semiconductor layer allows a higher injection of those charge carriers in the channel compared to the coplanar structure with the contacts under the semiconductor layer. Therefore in

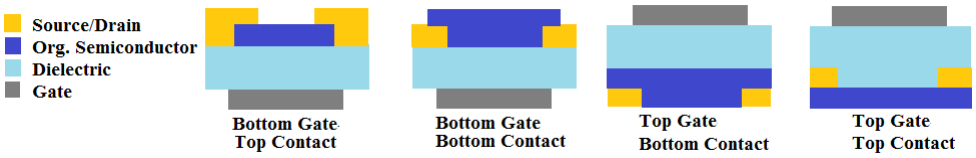


Fig. 2.1: Image of the four possible OTFT FET Structures.

order to reduce this contact resistance, in this work, the technology developed at LPICM-Ecole Polytechnique by shadow masks, is a bottom gate-top contact transistor structure. In the case where the contacts are defined by contact photolithography process as in Joanneum Research, the semiconductor has to be deposited at the end to avoid affecting this layer with other chemical or physical treatments. For this case, in this work, a bottom gate-bottom contact transistor structure is adopted.

The two basic deposition methods developped in this thesis are:

a)Physical Vapor Deposition (PVD) Process: is used to deposit solid materials such as the metals for the contacts (aluminium and gold) and the organic semiconductors in a high vacuum, typically with a pressure lower than 10^{-5}mbar without another agent in the vacuum chamber. There are different possibilities: The simplest one is a thermal evaporation where the material to be deposited is in a solid state and placed in a furnace to be sublimated and then directed towards a substrate where it desublimates. In Fig. 2.2, there is shown a figure representing this process where A) represents the vacuum chamber, B) the material to be sublimated, C) the furnace where it is placed, D) the shutter or valve that opens when the material arrive to the necessary sublimation temperature and is ready to be deposited. E) is the shadow masks that filters the materials to a particular shape needed to create a device. And F) is the substrate where the material is going to be deposited. A variation of this PVD procedure is when the material is not heated by a furnace, but by an electronic beam that breaks the surface and the material grains are thus ejected to the substrate to be deposited.

The Chemical Vapor Deposition (CVD) Process: is another process where the material to be deposited is in a chamber with the present of a precursor volatile agent which will react with the surface of the substrate in order to have an uniform layer. The most used CVD procedures are at

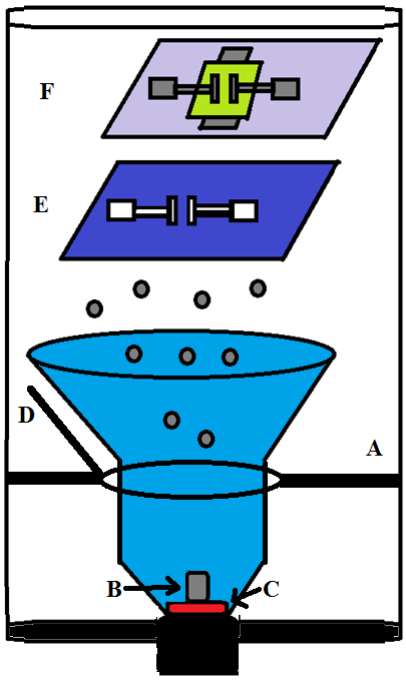


Fig. 2.2: Image of the thermal evaporation method with the different parts involved during the fabrication of thin film devices.

Low Pressure (LPCVD), Plasma Enhanced (PECVD), Atomic Layer (ALCVD),among others. This process is not used in this work.

b) Solution based deposition procedures: these deposition methods are used to deposite liquid or sol-gel state materials with the need of a baking step in order to harden and to dry the layer over the substrate. It is used conventionally for the dielectric and the photo resistive layers in the photolithography process. There are different possibilites: the spin-coating process is where the liquid solution of the material is deposited by a needle and then it is spreaded with a uniform layer over all of the sample by an spinning of the substrate at several hundreds or thousands of revolution per minutes (RPM). In reality the layer has some non-uniformities in the thickess under 100 nm that makes quite difficult to control with precision.

Another possibility not used in this thesis would be to ink-jet print the solution with a commercial printer. In this case, the solution is deposited over the substrate drop by drop with a precision pico litter ink-jet head. The advantage of this process is the high precision in the feature printed and the low cost of the overall process that is achieved, however a disadvantage is the viscosity of

the solution that is needed in order to avoid clogging of the print heads. The slow speed making those features which could extend till hours for a simple device is also a disadvantage.

The photolithographic procedures are also used in the fabrication of OTFTs and are further explained in chapter 4.

2.2 State of the Art of Compact Models for Circuit Design with Spice Simulators

Compact models are a set of one dimensional physical equations which describe the behaviour of a transistor in the different regions of operation following the classical procedure described for conventional MOSFET transistors, [3]. The idea is to describe the dependence of the drain source current equation in terms of the gate source and the drain source voltage with the least possible quantity of parameters. This is done in order to reduce the time of the simulations. The equations are thus implemented in an Spice-like simulator to obtain an electrical model with a discret device structure (resistors, capacitors, voltage and current dependent sources)

Two characteristics curves are needed to describe the DC behavior of a transistor, the transfer and the output curve. The transfer curve describe the transition of the drain source current from an Off state (or leakage regime) with almost no current in the channel to a subthreshold regime with a small drain source current in the channel and then to a linear above treshold regime with a considerable high current in the channel. The output curves however, describe the transition of a transistor from a linear resistor (voltage dependent) behavior to a current source (voltage independent) behavior.

A good model, thus, would need to fit in all of the above mentioned regimes, however in practice the lack of standards in the materials of the OTFTs and in the different parameter used to describe it, complicate the task. Several groups have reported functional models, (shown below), but the commercial simulators do not include all of them.

In order to have a compact model describing the transistor behavior, the first is to start from the definition of the mobility as the linear parameter that describes the speed of the charges v, in a solid as directly proportional to the electric field E applied to that solid:

$$v = \mu * E \tag{2.1}$$

The electric field E is in fact the voltage variation with the distance across the channel or dV/dx.

The current of charges traversing a unit square area with width W and thickness t, in the channel of a transistor named J is described following the classical Ohm's law. Where ρ is the charge per volume unity:

$$J = \rho * v \tag{2.2}$$

Or what is the same, the current density per width W, taking out of the equation, the thickness of the channel, as it is difficult to control it in practice:

$$K = \sigma * v \tag{2.3}$$

The charges per unit area in the channel of a FET structure σ are defined as the capacitance per unit area C_{ox} multiplied by the voltage across the capacitor structure. This voltage of course depends on the position of the charges in the channel, x and the charges increases (usually exponentially) if it surpasses a threshold called V_{Th}. $V_{GS} - V_{Th}$ it is often called the overdrive voltage.

$$\sigma = C_{ox}(V_{GS} - V_{Th} - V(x)) \tag{2.4}$$

Puting equation 2.4 and 2.1 in 2.3, and considering that K=I/W or the current definition in a typical Spice Model over the width, we have finally:

$$I/W = \mu * C_{ox}(V_{GS} - V_{Th} - V(x)) * \frac{dV}{dx} \tag{2.5}$$

Integrating x from 0 to L (the total channel length) and the voltage from source S to drain D (V_{DS}), we have at the end, the classical drain source current equation:

$$I = \frac{W}{L}\mu * C_{ox}[(V_{GS} - V_{Th})V_{DS} - \frac{V_{DS}^2}{2}] \tag{2.6}$$

Where if the drain source voltage is equal or higher than the overdrive voltage, the channel is pinched off anbd the transistor is in saturation:

$$I = \frac{W}{2L}\mu * C_{ox}[V_{GS} - V_{Th}]^2 \tag{2.7}$$

We can also add the channel modulation parameter in the case where the transistor channel is very short, and then even in saturation the transistor depends directly proportional to the drain source voltage. Which in our case using large area, longer channel OTFTs is not as important.

$$I = \frac{W}{2L}\mu * C_{ox}[V_{GS} - V_{Th}]^2(1 + \lambda * V_{DS}) \tag{2.8}$$

This is the traditional square model which describes the basic behavior of almost all of transistors with a FET structure. The principal point here is that we assumed that the mobility is not voltage dependent itself, which is the principal hypothesis in the amorphous materials (amorphous silicon and organic materials). There are basically thus, three type of models compatible with the OTFTs presented in this thesis work departing from a voltage dependent mobility: the model of the groups of Genoe [4], Deen [5], and Estrada [6].

Unfortunately as the equations are very general and every group fabricates its own transistor, some numerical parameters have to be added before a full physical explanation would be available or before the standards will be put in place. The drain source voltage is thus replaced by an effective V_{DS} equation 2.9 in order to have a better fit in the output curves. The impact of these numerical parameters are explained in Fig. 2.3. From a visual analysis, the threshold voltage, Vth shift up and down the straight line in the saturation regime and λ curve this straight line. The numerical parameters m tilt the curve in the linear regime and α_{sate} is the elbow between the linear and the saturation regime.

$$V_{ds\_eff} = \frac{V_{ds}}{\{1 + [V_{ds}/(\alpha_{sate}(V_{GS} - V_{Th}))]^m\}^{1/m}} \tag{2.9}$$

Where a full list of the parameters used in all the models are:

- $I_{aboveTh}$ is the drain-source current above threshold.
- W/L is the ratio width to length of the channel of the OTFT.
- C_{ox} is the dielectric capacitance.
- μ_{eff} is the mobility of the charge carriers.
- μ_0 is the assumed mobility.
- V_{GS} is gate source voltage.
- V_{DS} is the drain source voltage.

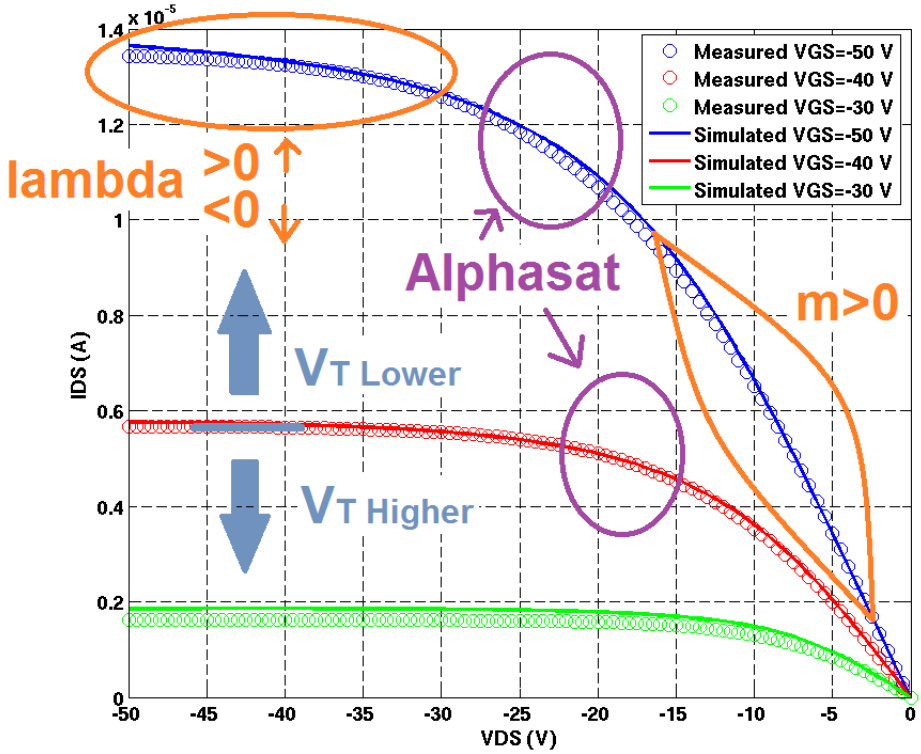


Fig. 2.3: Numerical parameters used to fit the models, in the output curve.

- VTh is the threshold voltage.

- R is the contact + access resistance for both contacts gate-drain and gate-source.

- λ is the parameter of the channel length modulation.

- m, γ, α_{sate}, V_{aa}, s and k are numerical parameters for adjusting the equation.

A) Genoe group model:

The effective mobility of the Genoe model is an empirical equation directly proportional to the intragrain mobility μ_0, and an exponential function of the gate source voltage of the form:

$$\mu_{eff} = \mu_0 exp\left(\frac{s}{V_{GS} - k}\right) \tag{2.10}$$

The drain source current equation is thus computed straightforward placing 2.10 for μ in 2.6 and replacing Vth for V_{ON}. This model does not make a separation between the subthreshold and above threshold regimes, instead the drain source equation is proposed to be valid in all of them.

The mobility equations of the Deen and Estrada model is gate voltage dependent with a γ power law function:

$$\mu_{eff} = \mu_0 \left(\frac{V_G - V_{Th} - V(x)}{V_{aa}} \right)^{\gamma} \tag{2.11}$$

Where V(x) could be the source voltage in the case of the Estrada model and in the case of the Deen model it is integrated to account for the total charge in the channel of the transistor.

B) Deen group model:

The integration of V(x) from Drain D to source S gives finally a 2+γ current equation:

$$I_{aboveTh} = \frac{\mu_0}{V_{aa}^{\gamma}} C_{ox} \frac{W}{L} \frac{(V_G - V_{Th} - V_D)^{2+\gamma} - (V_G - V_{Th} - V_S)^{2+\gamma}}{2+\gamma} \tag{2.12}$$

However this model has some fitting deffects in the subtreshold regime as explained in detail in [7].

C) Estrada group model:

The Estrada and Iniguez model is the one that is used in this work for modeling and circuit design, due to the fact that it is also present in the commercial Spice simulators for its similarity with the a-Si TFT model. In this model is implemented the same mobility equation 2.11 with a γ power law function, but replacing the variable voltage V(x) with the source voltage.

$$\mu_{eff} = \mu_0 \left(\frac{V_{GS} - V_{Th}}{V_{aa}} \right)^{\gamma} \tag{2.13}$$

The model will be developed in detail in chapter 3 and its discret device schematic is shown in Fig. 2.4. It takes in consideration the contact resistances in the interface with the semiconductor and both metallic contacts of the source and drain, RS_{EFF} and RD_{EFF} respectively. It is not easy to determine each one of them separately. As a first approach, they are considered physically symmetric to add as a one term in the equation 2.14, $R_{contacts\_d+s}$=RS_{EFF} + RD_{EFF}, becoming a voltage divisor for the applied drain source voltage. This model is present in several commercial Spice simulators such as [8] .

$$I_{aboveTh} = \left(\frac{1}{\frac{1}{g_{channel}} + R_{contacts\_d+s}} \right) V_{ds\_eff} \tag{2.14}$$

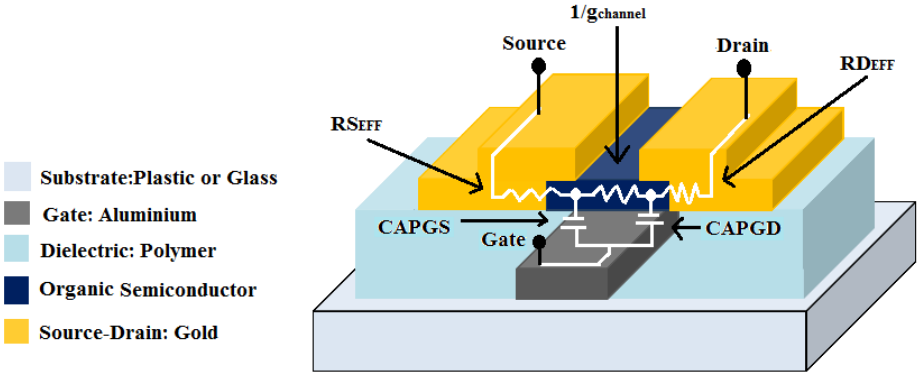


Fig. 2.4: a-Si TFT Small Signal Model used as our OTFT Model in ELDO Spice. Note the different thin films composed on an organic transistor.

Where $g_{channel} \approx g_{aboveTh}$ is the channel conductance parameter described above the threshold voltage and not taking into account the contact resistances and is dependent on the overdrive voltage, V_{GS}-V_{Th}:

$$g_{aboveTh} = \frac{\mu_0}{V_{aa}^{\gamma}} C_{ox} \frac{W}{L} (V_{GS} - V_{Th})^{1+\gamma} \tag{2.15}$$

If the inverse of the channel conductance parameter is bigger than the contact resistances, which is the case of the top contact transistor structure or bottom contact OTFTs with a SAM treatment as explained in the next chapters, one could neglect in a first approach this contact resistance and do hand calculations for circuit design using the simplified equation:

$$I_{aboveTh} = g_{aboveTh} V_{ds\_eff} = \frac{\mu_0}{V_{aa}^{\gamma}} C_{ox} \frac{W}{L} * A * \alpha_{sate} (V_{GS} - V_{Th})^{2+\gamma} \tag{2.16}$$

The fact that the power law is not squared but $2 + \gamma$ has an important effect on hand calculations, because γ is on the order of 0,5 and some approximations done for CMOS circuit design are not any more valid. This thesis work, shows in the next chapters some precise calculations of DC gain which were also succesfully verified by measurements.

The subthreshold and leakage regime are developed in detail in [9] with a mathematical model which fits very well the experimental values. This thesis work, is looking further to set the use of the model of Estrada and C.H.Kim as an de facto standard for circuit design at least at a research

Table 2.1: Organic thin film transistors already presented in our groups

References	**Diel./ Thickness(nm)**	**Semicond.**	**Voltage Range(V)**	**Mobility (cm^2/Vs)**	**$V_{Th}(V)$**
C.H.Kim [10]	SU-8/950	Pentacene	50	0,56	<abs(-15)
Zanella [11]	BASF Photoresist/200	Pentacene	10	0,5	<abs(-1)
Petritz [12]	PNDPE/48	Pentacene	5	0,8	<abs(-1)

level. This is the only way to advance in the field, when everybody could share and compare results at a more abstract design level as it is done with silicon-based circuits.

2.3 State of the Art of Organic Thin Film Transistors

This thesis departs from the previous works in OTFT fabrication and modeling of C. H. Kim [10] in Ecole Polytechnique, France, F. Zanella at CSEM, Switzerland and A. Petritz at Joanneum Research, Austria. A summary of the characteristics and performances of the differents OTFTs are presented in Table 2.1 and a description of what is proposed in this thesis:

A) Ecole Polytechnique Technology: Although the operating voltages are higher, this work proposes a lower cost and easy-to-fabricate technology by shadow masks of OTFTs and the design of several analog blocks. A spice model present in a commercial simulator would be adjusted. A mismatch model will be presented and a statistical description of the variations in the extracted parameters will be described.

B) Joanneum Research Technology: This thesis work presents an adaptation of the OTFT technology fabricated by shadow masks from the work of A. Petritz, to a contact photolithographic technology. Two analysis are presented: first, large width OTFTs (ideal for analog design) will be tested in order to be aware of gate leakage. And second, the source drain interface will be improved by the reduction in the injection barrier. The contact resistances was thus calculated and then the OTFT was modeled with the same adapted a-Si Spice model explained in this chapter. The model fitting presented by Zanella will be improved by this more developped model. This works targets also the reduction in its operating voltages, compared to his publication.

2.4 State of the Art of Circuits

Some companies such as Plastic Logic LTD, in England or ISORG, in France are going towards the goal of integrating sensors in a full system for commercialization. However as far as the author know, there are not yet applications in consumer electronics at an industrial level using flexible integrated circuits with an standardized model and a statistical extracted parameter analysis. The different research groups would rather present measurement results of well-working functional systems without a formalized approach between theory, simulation and tests, nor even a comparison of measurement and design calculations. The lack of standards are due to the fact that each academic group works with different materials and processes. This absence of a trustworthy model for circuit design has as a consequence, a slow process of application development.

There are few reproducible and functional circuits, where the flexible systems are just composed per pixel of a sensor and one or two OTFTs as row and column decoders such as in [13] and the rest of the sensor matrices in the Takao Someya's lab, one of the leaders in this field. Some applications showing several thousands of OTFTs are rare and there are no clear evidence of the reproducibility of them.

2.4.1 Amplifiers on Flexible Foils

This thesis works aims to improve the state of the art of amplifiers on flexible foils. In this field, several groups have been in a race to obtain the best performance on gain and bandwidth. Their peek performances are complementary, for example Maiellaro et al. [14] has shown the highest DC gain reported to date, but its bandwith is rather slow of several Hz, with a high power consumption using a 50 V supply voltage. On the contrary Marien et al. at IMEC [15] has shown a more complex amplifier with 3 stages using a lower power consumption but a larger bandwidth with several tenths of Hz. The fact that the mobility in the organic material is still poor and that the dielectric is thick, do not allow to have a high transconductance OTFT which is key in the design of amplifiers. Moreover, the bandwidth are rather short because the channel lengths are longer till several microns.

Table 2.2: State of the Art of amplifiers fabricated with flexible organic materials

References	**Maiellaro [14]**	**Marien [15]**	**Nausieda [17]**	**Guerin [18]**	**Gay [16]**
Fabrication Techno	20 μm Print	5 μm PL	5 μm PL	20 μm Print	5 μm PL
Transistor Type	C-OTFT	P-OTFT	P-OTFT	C-OTFT	P-OTFT
Amplifier Topology	Folded Casc.	3-stage	2-stage	Diff. Pair	Cascode
Supply Voltage(V)	50	15	5	40	40
Current Consump.(uA)	13	21	0,55x10^{-4}	1	n.a.
Power consump.(uW)	650	315	2,75x10^{-4}	40	n.a.
Open loop DC Gain(dB)	40	23	36	27/22	8
GBW/PM (Hz)/(°)	1500/58	500/70	7,5/n.a.	n.a.	1400/n.a.
Settling time (ms)	$<$1	n.a	n.a	n.a	n.a
Compensation Tech.	Dominant Pole	Miller Eff.	Uncomp.	Uncomp.	Uncomp.
Area (mm^2)	115	n.a.	n.a	n.a	1,5
Number of OTFTs	6	27	12	4	8

A summary of the performances are presented in 2.2. So far, Marien et al. [15] is one of the few to show simulated and measured comparisons in his designs of amplifiers. There are no yet statistical comparisons between process and performance parameters variations in the flexible electronic field. Finally, Gay [16] was the only one who showed the gain variations in an amplifier by Monte Carlo simulations, stating realistic results for low values under 10 dB.

2.4.2 Comparators

In this thesis work, a comparator with few organic transistors is intended to be designed working at higher input and clock frequencies compared to the state of the art. On Table 2.3, a summary of this state of the art is presented. The one presented in the work of Marien [19] is the most reliable result with a fully differential comparator based on his AC-coupled load amplifier. Maiellaro [14] and Abdinia [20] show well-working differential to single ended comparators with few OTFTs but at high voltages, difficult to be implemented in a low power sensor interface.

Table 2.3: State of the Art of comparators fabricated with flexible organic materials

References	**Maiellaro [14]**	**Marien [19]**	**Abdinia [20]**
Fabrication Techno	20 μm Print	5 μm PL	20 μm PL
Transistor Type	C-OTFT	P-OTFT	C-OTFT
Comparator Topology	Folded Casc.	AC-Coupled Load	Single Inverter
Number of OTFTs	12	11	8
Supply Voltage(V)	50	20	40
Current Consump.(uA)	13	9	n.a.
Power consump.(uW)	650	180	n.a.
Min. Input Signal (V)	1	0,2	0,4
Input Frequency (Hz)	50	40	DC
Clock Frequency (Hz)	120	1000	50
Area (mm^2)	232	2x3	n.a

2.4.3 Analog to Digital Converters

This thesis work has as a principal objective to develop an analog to digital converter (ADC) with the lowest number of OTFTs in order to avoid the intrinsic variations that a complex system could present. In this field, several contributions have been presented, although 2 of them were fully integrated on plastic foils: a 129 OTFT, 1 bit sigma delta modulator from Marien et al. at IMEC [21] (without a decimation filter) and a 106 OTFTs counter type ADC by Abdinia et al. at Technical University of Eindhoven [22]. In the other cases, Xiong et al. in Standford University and the Max Planck Institute showed a 6 bits successive approximation ADC [23], and Raitieri et al. [24] showed a 48 db SNR with 7,7 bits of resolution. None of them fully fabricated on flexible foils. In Table 2.4, is presented a full summary of their performances. However no one yet has integrated succesfully an ADC in a pixel with a sensor on a flexible foil. This is of course an interesting approach in the future for a full system design.

Table 2.4: Different Organic ADC specifications in the litterature. The ** means that the ADCs are not fully manufactured with OTFTs

Author	**Marien**	**Abdinia**	**Raitieri**	**Xiong**
Published	ISSCC 2012 [21]	ISSCC 2013 [22]	ISSCC 2013 [24]	ISSCC 2010 [23]
Technology	IMEC	TUE-CEA	TUE	Stanford-MPI
ADC Type	SD	Counter	VCO	SAR
Number of OTFTs	129	106	17(**)	53(**)
Supply Voltage (V)	15	40	20	3
Power consumption (uW)	1500	540	48	3,6
Vin, CM (V)	9	0	-	1,5
Vin, AC (V)	1	0,4	0-20	1,55
OSR	16	-	-	-
Bandwidth (Hz)	15,6	2	33,5	14,3
fin (Hz)	10	2	4-38	-
fs (Hz)	500	70	66	100
SNDR (dB)	24,5	19,6	48	-
ENOB (bits)	3,77	2,96	7,7	6
FoM (nJ/bits)	3524	17349	3,45	-

2.4.4 CAD Tools for Emerging Technologies

Computed Aided Design (CAD) tools are common for CMOS design and other industrial technologies. Adapted CAD tools for emerging technologies are rare as well, mainly due to the lack of the commercialization of the applications. According to the authors knowledge, Vila [25] at Universidad Autonoma de Barcelona is the only one who worked in CAD tools for printed electronics. In this thesis, a full CAD system of tools from LIP6-UPMC, is presented as a proof of concept including as well placement and routing tools (not presented in Vila's CAD system). This work, is thus a first approach to incorporate also in the future, the full physical model developed in LPICM-Ecole Polytechnique.

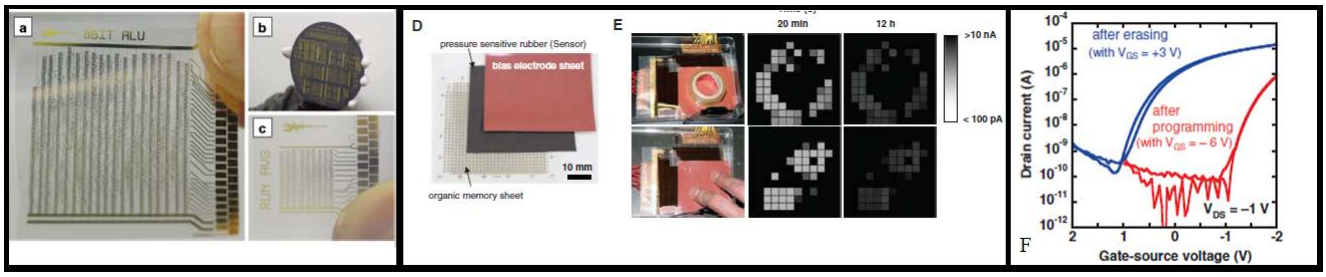


Fig. 2.5: Digital Systems with Flexible and Organic Transistors

2.5 State of the Art of Applications

This thesis work is not oriented to a particular application. From a pedagogical point of view and as an introduction for beginners in the field, CMOS designers and hardware engineers, a list of several applications realized with flexible and stretchable devices, is presented here.

2.5.1 Signal Treatment Systems

There are different applications concerning flexible digital circuits. Myny et al, [26] showed an 8 bit microprocessor with more than 4000 OTFTs, presented in a, b and c in Fig. 2.5, a memory was also shown by the group of Someya et al. [27] using an OTFT with an hysteresis behavior, as we can see in d, e and f in Fig. 2.5. The group of Someya also showed the possiblity of designing FPGAs [28], among other applications.

2.5.2 Pressure Sensors

This was the first classical application in the field in the group of Takao Someya, [13]. It is presented in A) in Fig. 2.6, where they describe a piezoresistive rubber sheet connected through vias to an active matrix with at least 2 OTFT per pixel in order to acces to the signals of every pressure dot sensor. In B) there is another type of capacitive pressure sensor demonstrated by Marien at IMEC [21]. The idea in this case was to include in every pixel a full analog to digital converter with a sigma delta modulator as explained subsection 2.4.3 of 24,5 dB SNDR, shown in [29], however both were done separately and it has not been tested yet.

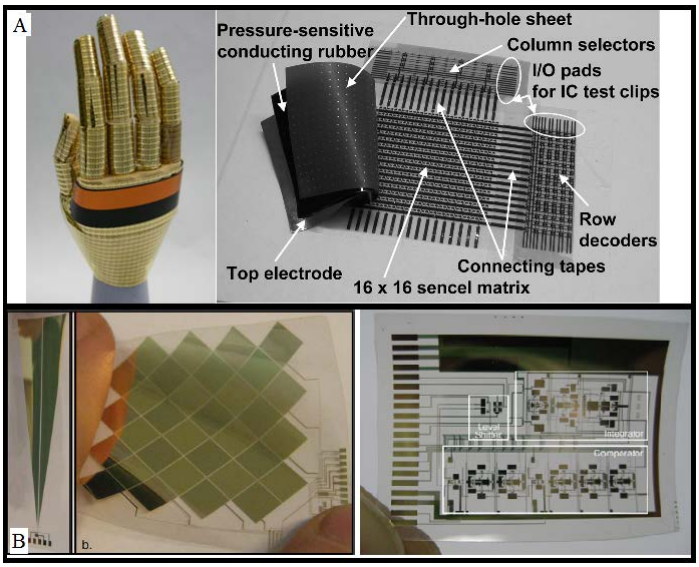


Fig. 2.6: Pressure sensor applications with flexible materials

Fig. 2.7: Displays with flexible materials

2.5.3 Flexible Displays

In this field, several groups proposed different types. One of the best developped displays at a pre-industrial level was done by Gelinck et al. [30] with an electrophoretic 64x64 pixels. It is shown in Fig. 2.7 with a simple level shifter and some addresing solution processable OTFTs in every pixel.

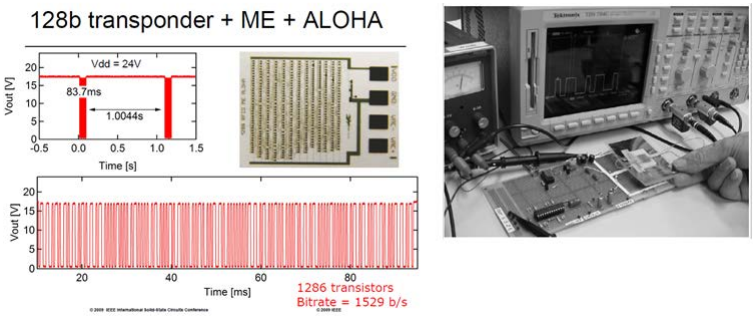


Fig. 2.8: RFID Tag with flexible materials

2.5.4 RFID Tags

This is one of the most promising field of research. Cantatore et al. at the Technical University of Eindhoven has improved very well this field. One of the first contributions was in 2006, [31] showing a 64 bit code, capacitively coupled tag for close proximity data transfer at the standard of 13,56 MHz. The application is presented in the right part of Fig. 2.8. Several improvements were done later, notably the one presented by Myny et al. at IMEC [32] and is shown in the left part of the figure, where he reduced the voltage of the transistors, increasing the memory to 128 bits and the data rate till 2kbits/s using more than 1000 OTFTs, which represents one of the more complex circuits reported to date.

2.5.5 Energy management for flexible devices

In this field several interesting applications have been presented. Energy production and harvesting is a key concept in todays electronic industry and there are promising approaches also for the flexible electronic world. One of the most remarkable applications from a practical point of view was the ultra flexible solar cell presented by Kaltenbrunner et al. [33] shown from a to e in Fig. 2.9 with a 10 W/g of specific weight higher than the 3W/g of a conventional CIGS cell, showing one of the highest efficiency per weight presented to date. The group of Someya showed wireless power transmitters, [34] using again its active matrix of OTFTs for addressing rows and columns, where a large area sheet of coils and MEMS was superposed and then it transfered energy to a group of LEDs at a short distance as presented in F of Fig. 2.9. The group of Prof. Bauer showed also flexible and stretchable batteries [35] with a 6,5 mA h and a 25% strain after 700 mechanical

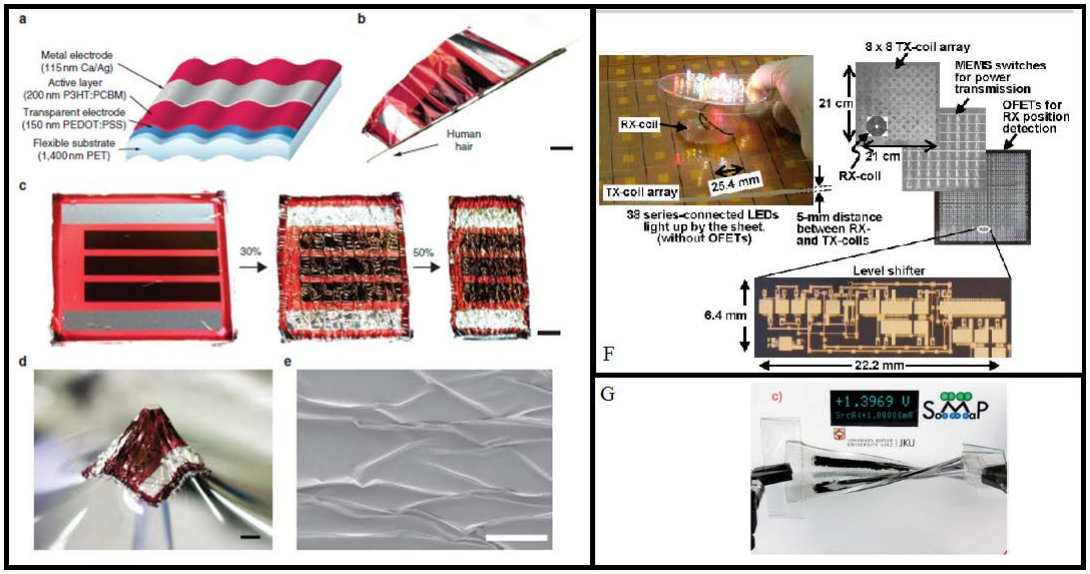


Fig. 2.9: Energiy Management Applications with Flexible and Organic Materials

stretch cycles, presented in G. The group of Someya also showed an energy harvesters with an insole pedometer in [36], using a PVDF piezoelectric sheet and the same concept of the active matrix already shown in other projects.

2.5.6 Smart Textiles

In the field of textile applications, Hamedi [37] proposes to put in every cross point of 2 threads for sewing a FET structure submerging the crosses in an electrolyte which work as a transistor as seen in Fig. 2.10. Although quite slow in the time response of several seconds, this is a first step towards placing signal treatment as close as possible of our bodies in clothes and our every day life.

2.5.7 e-Health applications with flexible and biocompatible materials

The last frontier in this field is to deliver signal treatment directly into our bodies to communicate with sensors in the outside to recover critical life signals and in chirurgical procedures. The group of John Rogers at the University of Illinois at Urbana-Champaign is one of the leaders in this field showing applications with biocompatible materials already implanted in the body of animals. As shown in Fig. 2.11, in A) an electroencephalogram for in Vivo brain signals sensing was tested on

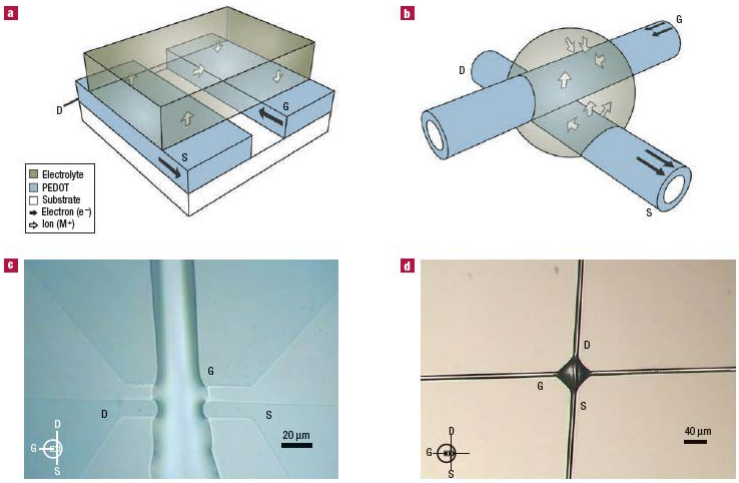


Fig. 2.10: Textile Applications with flexible materials

a rat in [38]. Another group who has succesfully tested implantable neural probes with OECTs is the Malliaras group, as presented in [39] with one of the highest transconductance transistors reported to date which enables higher SNR recovery of signals from the brain. Continuing in the figure in B) catheters with ablation properties for surgical procedures were succesfully tested in a rabbit heart in [40]. In C) several surgical devices were fabricated with sensors to be placed on the fingers in order to enhance the capabilites of a surgeon, presented in [41]. In D) and E) other epidermal sensors are presented in [42], where a set of coils, chemical and pressure sensors are implemented as an artificial skin or tattoos as a way to reconver important health information and send them to other conventional electronic devices which will analyze it.

2.6 Major Contributions

2.6.1 Technology Process

This thesis works aims to formalize a process of optimization of the fabrication and characterization of 2 technologies: The first at LPICM in Ecole Polytechnique with an easy-to-fabricate and low cost procedure developed using shadow masks. The second at Joanneum Research with a low power-higher performant technology developed by contact photolithography, self-aligning the source and drain contacts. A clear result of this optimization is the improvement in the dielectric

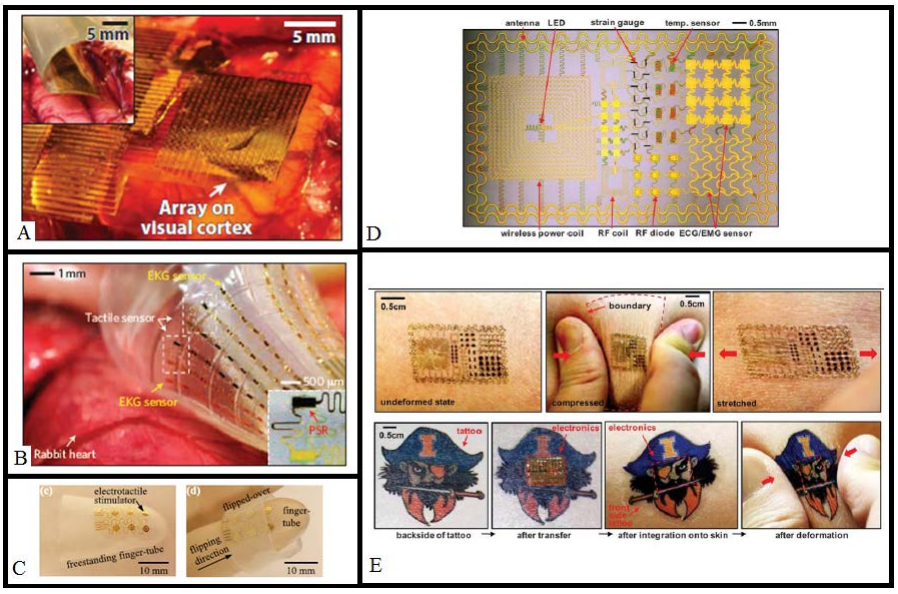


Fig. 2.11: e-Health Applications with flexible and biocompatible materials

and semiconductor layers of both technologies by increasing the size and reducing the number of grains in the channel of the transistor in order to obtain stable values of mobility. An in-house dielectric without pin-holes was implemented for the first time in the circuits tested in chapter 6. Both of the technologies were modeled as well, with an adapted a-Si TFT model with closer simulation and test comparisons with respect to other models. This work targets to set a de facto standard Spice model among different research groups.

In the case of the shadow masks OTFTs: a mismatch model was developed in order to quantify the variation of drain source currents in different OTFTs fabricated under the same conditions, and to quantify the physical parameters extracted, relating their variations with the yield of the designed circuits. This work is being submitted for publication. A part of this work is published in [43].

In the case of the photolithograpic OTFTs: this works describes a design tool kit composed of process parameters extracted and rules for layout design. A part of this work is published in [44]

2.6.2 Circuit Design

In the case of the Ecole Polytechnique Technology: A functional analog to digital converter was designed. It is composed of a sigma delta modulator with just 25 OTFTs with a simulated SNR of 30 dB, which is one of the highest SNR reported to date. As far as the authors know, this is the first time that a organized and formal procedure of parameter extraction and design analysis is done among the different organic transistors research groups. This work is being submitted for publication.

In the case of the Joanneum Research Technology: After a collaboration with the colleagues in process technology, the contact resistance was greatly reduced with the help of a SAM treatment. This helped to better model the DC behavior of the OTFTs. During this research work also several fast analog and digital circuits were succesfully tested with the design and measurement of a Transistor Evaluation Module (TEM). This mask will be used as a template to study the performances of different dielectrics and semiconductor layers. In particular, a state of the art differential voltage amplifier was measured, with the largest gain bandwidth reported to date (several KHz) and a functional comparator working at 10 and 100 KHz of clock and input frequencies. This work will be submitted for publication.

2.6.3 Layout Design Automation Tools

With a collaboration at LIP6-UPMC, this thesis work contributed to the elaboration of a design tool kit for the LPICM-Ecole Polytechnique Technology. A system of open source VLSI CAD tools (Alliance ©) was customized for the layout design and automation. A proof of concept was elaborated for the layout of a sigma delta modulator. Several place and route tools were implemented as well, for every cell in a predefined template of a shadow mask in order to design a layout and for technology migration from node to node. These customized tools could be extended for any other thin film transistors technology. This work is published in [45].

2.7 Conclusion

In this chapter, an introduction to the different fabrication procedures with OTFTs was shown. A brief summary of the principal compact models was developped showing the advantages of the a-Si TFT based Spice Model that we are using in the next chapters. It was presented a detailed state of the art summary. Finally, the principal contributions of this thesis were presented pointing out the vertical flow of this work from process optimization, modeling, parameter extraction statistics, circuit design and test and customized VLSI CAD tools for design automation of TFT circuits.

Part II

Technology Process

3

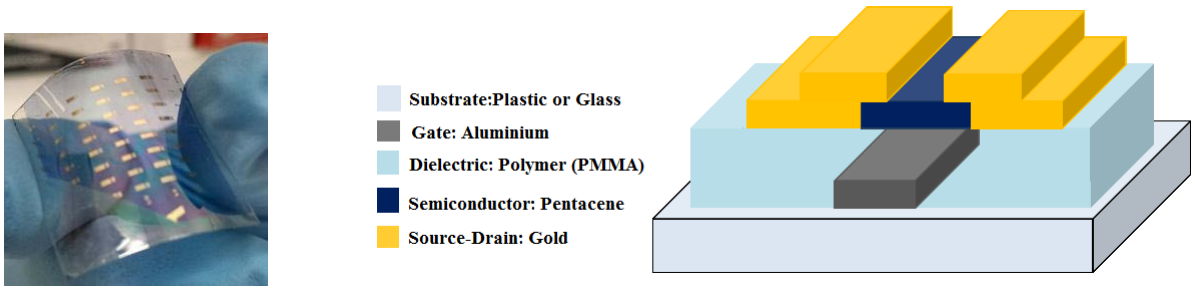
Systematic Parameter Characterization & Mismatch Model for Analog Design with Flexible Organic Transistors

3.1 Introduction

In this chapter, a straightforward fabrication process is presented, aiming to quantify and to reduce the large process parameters variation in organic transistors. In Fig. 3.1(b) is shown the manufactured flexible transistor structures done by shadow masks with the description of the different layers. For the semiconductor, a 50 nm thin film of a commercial small molecule P-type organic semiconductor, called pentacene is deposited. It is very well-known for its stability in air for several days outside a nitrogen glove box and its easier deposition process by low temperature thermal evaporation with good values for mobility (in the field of organic semiconductors) ranging from 0,01 to 1,0 cm^2/Vs, e.g: [46], [47], [48].

The selection of the gate dielectric is a broader and also complex decision because it affects the overall performance of the transistors [49], [50], [51] and [52]. In order to develop an easy and low cost process of fabrication of organic transistors, a commercial and well known polymer was used: PMMA (Poly Methyl Methacrylate) due to its low hysteresis behavior, easy deposition (e.g: by spin-coating) and its smoothness of the surface for the pentacene growth of large grains [53], [54], [55].

The gate is done with a 60 nm film of aluminum and the contacts of the source and drain are done with a film of 50 nm of gold which enables a better injection of charge carriers (holes) to the pentacene [9]. The bottom gate - top contact transistor structure was implemented, also shown in Fig. 3.1(b), for its lower contact + channel resistance with the semiconductor due to the grain morphology at this interface as was shown in [2]. The OTFTs were tested on glass. How-



(a) (b)

Fig. 3.1: a) Organic thin film transistor (OTFT) photography on a plastic substrate. b) A 3D structure showing the different materials and layers with a bottom gate-top contact structure

ever other commercial plastic substrates were also tested such as a 175 μm, PET (Polyethylene Terephthalate) from DuPont Teijin Films ^{TM}.

One of the main drawbacks of the organic technologies, is the lack of reliability and repeatability during the manufacturing of transistors and circuits. Academic contributions such as the ones presented in [29], [23], [24] are on the contrary focused on peak performances rather than a detailed analysis of results among a considerable quantity of devices manufactured. Therefore, this work is focused on the study of these parameter variations using statistical methods that relates the physical parameters to circuit design parameters. Following procedures described for the c-Si CMOS characterization and modelling [56], [57], important physical parameter variations are quantified by histograms and modeled by a normal distribution to find the expected values and the variance of them. Finally, the current dispersions in the transfer I-V curves of the fabricated transistors were measured with a simple mismatch model developed from the adapted a-Si TFT Spice Model used in this thesis work.

This mismatch model is presented on section 3.2, to quantify the aforementioned parameter variation of the process of manufacture of organic transistors presented in section 3.3. The measurements of transistors and the extraction of parameters using the a-Si TFT adapted Spice model is presented in section 3.4. This is a first step to improve systematically (from an analog designer point of view) the performance of the organic transistors from the present technology to future ones.

3.2 Mismatch Model Development

The extraction of parameters for an emerging technology is a procedure not always very well explained in the literature, due to the particular decision of the models used to describe the physics of transistors developed by each academic research group. However some groups have reported generalized models [9], [6], [58]. In this thesis work, from a practical point of view, the well-known amorphous Silicon (a-Si) TFT compact model is adapted for organic transistors. This model has the advantage that it is already available in many commercial SPICE circuit simulators, e.g: [8] and as it is reported elsewhere [9], it could be used as well, for organic transistors as the physics has been shown to be equivalent for the above threshold regime (3.2). The sub-threshold and leakage regimes are (as explained in all of this thesis work), for the moment, not interesting to us as currents are very low for analog circuit design. Moreover, this thesis work targets to formalize the design of robust circuits (e.g: ADCs integrated with sensors in flexible applications) by determining the process corners, which are useful for Monte Carlo simulations. In this way, the quantification of the parameter variations with a mismatch model are necessary. This generalized procedure could be thus, extended to other transistors fabricated with flexible emerging materials.

Using the fitting procedure of the a-Si TFT compact model presented in [6], and once the parameters are extracted, it is possible to do AC, DC and the above mentioned Monte Carlo circuit simulations with for example the commercial simulator ELDO [8], used in this work.

In chapter 2, it was explained that in a-Si TFTs and organic polycristalline TFTs, the effective mobility depends on the overdrive voltage with a gamma power law, (3.1). Its values depend strongly on the growth of larger and ordered Pentacene grains in the channel. This is obtained with a very smooth dielectric surface and a very slow deposition speed of the first layers (at least the first 5 nm) with a controlled temperature in the evaporation source.

The principal equations of the a-Si TFT model, briefly explained in chapter 2 in the above threshold regime are described below for clarity:

$$\mu_{eff} = \mu_0 \left(\frac{V_{GS} - V_{Th}}{V_{aa}} \right)^{\gamma} \tag{3.1}$$

The drain-source current equation is:

$$I_{aboveTh} = \left(\frac{1}{\frac{1}{g_{aboveTh}} + R_{contacts\_d+s}} \right) V_{ds\_eff}(1 + \lambda V_{ds}) \tag{3.2}$$

Where again from chapter 2 the effective drain source voltage and the channel conductance parameter are:

$$V_{ds\_eff} = \frac{V_{ds}}{\{1 + [V_{ds}/(\alpha_{sate}(V_{GS} - V_{Th}))]^m\}^{1/m}} \tag{3.3}$$

$$g_{aboveTh} = \frac{\mu_0}{V_{aa}^{\gamma}} C_{ox} \frac{W}{L} (V_{GS} - V_{Th})^{1+\gamma} \tag{3.4}$$

As explained in chapter 2, when using longer channel transistors (30 μm in this chapter) then $\lambda << 1$ and if the contact resistance is negligible in a first approach compared to the inverse of the channel conductance:

Then, simplifying:

$$I_{aboveTh} = g_{aboveTh} V_{ds\_eff} \tag{3.5}$$

Similar to the c-Si MOSFET, there are two regimes: -Saturation regime when:

$$V_{ds} >= (\alpha_{sate}(V_{GS} - V_{Th})) \tag{3.6}$$

Which simplifies to:

$$V_{ds\_eff} = A * (\alpha_{sate}(V_{GS} - V_{Th})) \tag{3.7}$$

According to:

$$A = \frac{1}{2} \Rightarrow V_{ds} = (\alpha_{sate}(V_{GS} - V_{Th})) \tag{3.8}$$

$$A = 1 \Rightarrow V_{ds} > (\alpha_{sate}(V_{GS} - V_{Th})) \tag{3.9}$$

Finally, the drain-source current equation in the above threshold regime simplifies to the following expression which takes into account several parameters extracted in this chapter:

$$I_{aboveTh} = \frac{\mu_0}{V_{aa}^{\gamma}} C_{ox} \frac{W}{L} (A\alpha_{sate})(V_{GS} - V_{Th})^{2+\gamma} \tag{3.10}$$

$$I_{aboveTh} = \beta_{sat}(V_{GS} - V_{Th})^{2+\gamma} \tag{3.11}$$

-In the case of the linear regime when:

$$V_{ds} < (\alpha_{sate}(V_{GS} - V_{Th})) \Rightarrow V_{ds\_eff} = V_{ds} \tag{3.12}$$

The equation simplifies to:

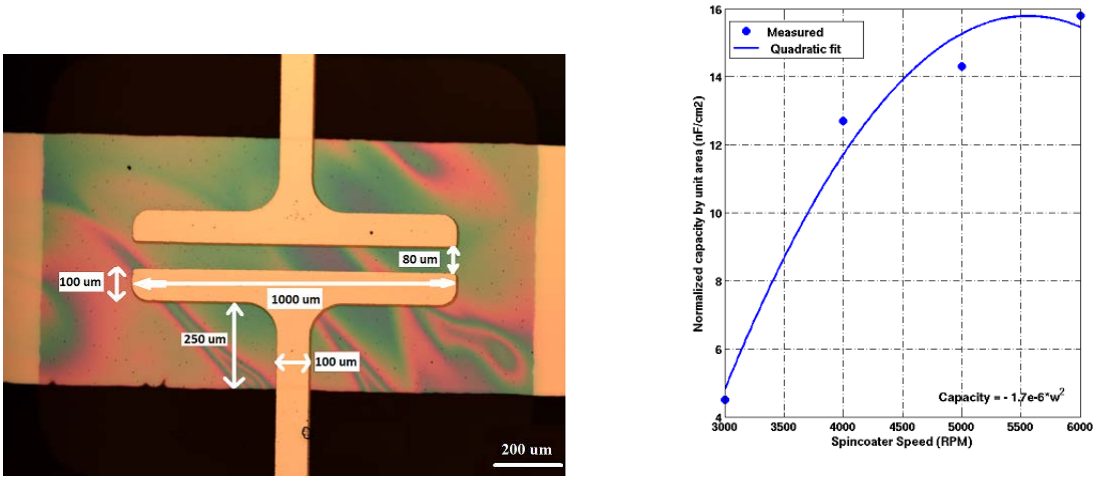
$$I_{aboveTh} = \frac{\mu_0}{V_{aa}^{\gamma}} C_{ox} \frac{W}{L} (\alpha_{sate})(V_{GS} - V_{Th})^{1+\gamma} V_{ds} \tag{3.13}$$

$$I_{aboveTh} = \beta_{linear}(V_{GS} - V_{Th})^{1+\gamma} V_{ds} \tag{3.14}$$

This work focuses in the saturation regime to obtain the highest output resistance of the transistor and higher drain source current values. The mismatches in these current values are a problem typical in organic transistors. Therefore, the variations of the most important physical parameters V_{Th} and β_{sate} were quantified. Computing a simple equation to state the link between process parameters and mismatch in current values in transistors is a key step to analyze performance in any new technology, following a similar work as the ones presented by Pelgrom and others in the 80s, in [59], [60], [61], [62]. Thus from equation (5.1):

$$\frac{\sigma^2_{I_{aboveTh}}}{\overline{I}^2_{aboveTh}} = \frac{\sigma^2_{\beta_{sat}}}{\overline{\beta}^2_{sat}} + (2+\gamma)^2 \frac{\sigma^2_{V_{Th}}}{(V_{GS} - \overline{V}_{Th})^2} \tag{3.15}$$

It is seen clearly, that working with a large gate-source bias allows the reduction of the dependency of the drain-source current with the variation in the threshold voltage. On the contrary, as it will be explained in the next sections, the drain-source current is a strong function of the variation of the trans conductance β_{sat} factor, which is also dependent on the mobility and thus the deposition of the semiconductor. In this technology and in future ones, a strict control of the deposition of the grains is a key factor to reduce at the minimum, the variation of the current in OTFTs.



(a) (b)

Fig. 3.2: a) Microscopic image of an OTFT. The changing colors are due to the light refraction in the inhomogeneous thickness of the dielectric. b) Experimental curve of the capacitance of the polymeric dielectric layer as a function of the spin-coater rotation speed.

3.3 Manufacturing Technology Process

In order to quantify the trans conductance parameter β_{sat}, one can identify in equation (3.10) the dielectric capacitance C_{ox} and the effective mobility as the 2 principal causes of variation. By this, the improvement of them is shown in this section, looking for a compromise between reliability and performance. The variation in the width and length due to irregularities in the shadow mask edges are not taken into account as OTFTs with large widths on the order of 1 mm and lengths of tenths μ m are being manufactured.

3.3.1 Engineering the Polymeric Gate Dielectric

For the gate dielectric layer, the polymer PMMA (Mw = 120 000 Da, from Sigma Aldrich ^{TM}) is deposited by a spin-coating process. In order to obtain very thin layers, the behavior of PMMA depending on the concentration in a solution and in the deposition speed were studied. Toluene was the solvent used (also from Sigma Aldrich ^{TM}).

In a first attempt, the concentration was fixed (7,3 % in our case) and the speed of the spin-coater was varied, keeping always a 1 step, and a time of 5 seconds for ramp acceleration from

0 rpm to the desired one. The films were cured always at 140 C for 1 hour and the capacitance measurement was performed with a 50 nm gold contact layers. As shown in Fig. 3.2(b), the capacity varies approximately with the square of the spin coater rotation speed (w) in this work, for the considered speed range. Other groups have also expressed similar experimental equations with also a monotonic increase in the capacity, but with square root of w [53], [54]. The maximal speed of our spin-coater is 6000 rpm, thus unfortunately we could not test thinner dielectric layers with this technique, however very thin layers of about $16nF/cm^2$ or what is the same 180 nm of thickness are obtained. In this thesis work, a thick dielectric layer of about 550 nm and about $5nF/cm^2$ was implemented in order to have a quite homogenous and dense layer over all of the substrate. On Fig. 3.2(a), the sizes of the parasitic overlap capacitance are shown accounting for a total 6,25 pF for the gate-source and gate-drain, as the OTFT is symmetric. It is important to remark that the parasitic capacitances in the shadow masks technologies depends on the minimum possible length value which could be aligned by mechanical procedures. Therefore several microns of overlap lengths are normal compared to a photolithographic technology where it is possible to reduce them to some hundreds of nanometers, as explained in the next chapter.

3.3.2 Engineering the Semiconductor Pentacene Layer

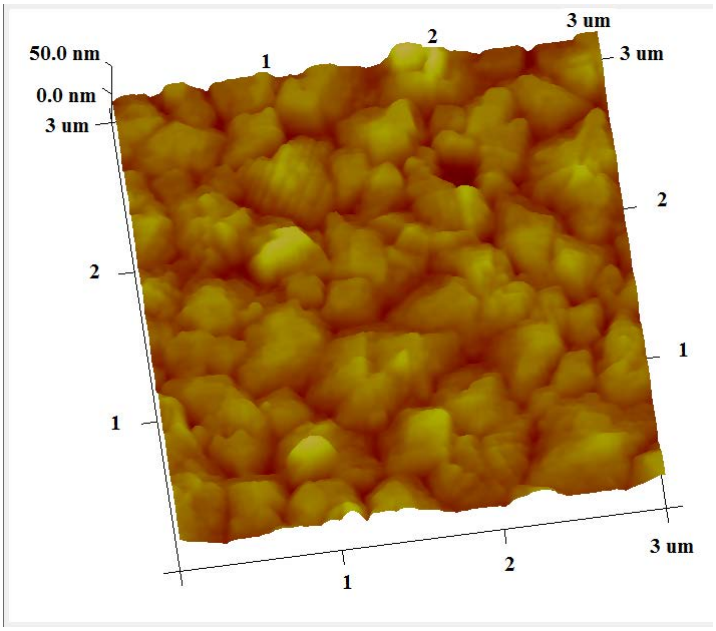
The semiconductor used was pentacene from Sigma-Aldrich ^{TM} with (according to the manufacturer) a 99,9 % purity. A 50 nm thickness layer is deposited by vacuum evaporation (1,0 X 10^{-6} mbar) in a very low O_2 concentration < 10 ppm and with a control, during the deposition, of the source temperature variation: 200 C +/- 3 C. Depositions speeds are approximately 1 nm/min or 0,167 A/s. The morphology of the different pentacene grains has an important influence on the charge carrier mobility. In the best case, the pentacene molecules adhere to the surface upon evaporation and arrange almost perpendicular to the dielectric surface in a herringbone order thus maximizing the overlap of neighboring π-electron orbitals and forming a delocalized π-electron system. Neighboring molecules pack and build stable islands which are the nucleation centers for the pentacene grains. Upon increasing coverage (during the continuous evaporation) these grains grow and coalesce and form polycrystalline pentacene films. From AFM height studies or microscopy images it is not possible to deduce the ordering of the different grains, it is only

Table 3.1: Mean, standard deviations and percentage of variations of samples presented in Fig.3.3 and Fig.3.4

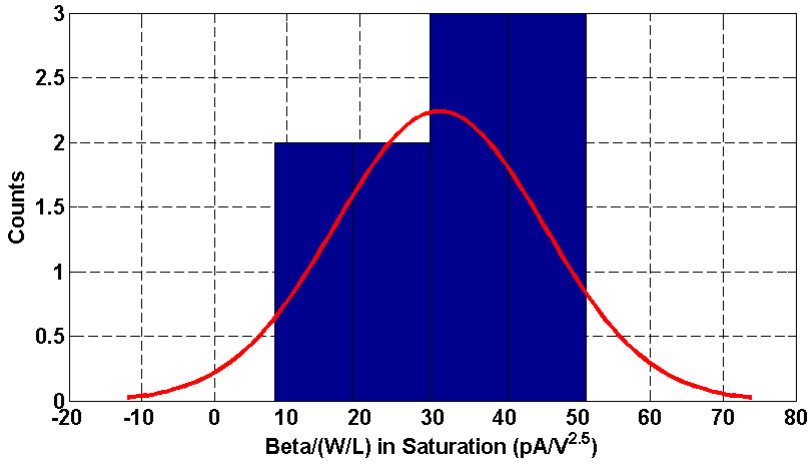
Sample	β_{sat} **mean**	β_{sat} **std.dev**	**%** β_{sat}
Tsubstrate=25 C	3,10E-11	1,43E-11	46,2
Tsubstrate=50 C	2,05E-11	8,59E-12	41,8

possible to determine the average grain size and the nucleation density. Both are mainly defined by the surface properties (surface energy and roughness) of the dielectric interface and they are decisive for the quality of the transport, the latter being confined to the first monolayers (roughly determined by the Debye length of 3 monolayers) [63]. However, AFM studies performed of the 50 nm thick pentacene layer will only deliver a rough estimation of the nucleation density and the grain size in the critical first monolayers. As explained in Ref. [63], the higher the nucleation density, the smaller the grain size and the more boundaries exist between the grains. Grain boundaries always limit the intergrain charge carrier transport since forming a potential barrier and therefore the intergrain mobility will be smaller than the intragrain one. Fig.3.3 and Fig.3.4, present Atomic Force Microscope (AFM) images of 2 typical OTFTs of 2 different samples in the channel area of a 30μm channel length and a width of 1000μm (in this chapter the shadow masks used for the test, have every OTFT with a width of 1000μm). On the bottom of each one, there are as well, the histogrammes of the calculated trans conductance parameter β_{sat} for 15 OTFTs on each case.

The extraction of the β_{sat} parameter was done with the classical method using the linear slope of the transfer curve in saturation, equation (5.1). The power coefficient γ as explained later, was previously extracted and calculated to be about 0,5. The substrate of the one of Fig.3.3 was heated during deposition at 25 C and the other of Fig.3.4 at 50 C. As explained in the litterature [63], higher substrates temperatures indicate larger grains presented in the channels reducing by this, the number of grain boundaries, which is one of the principal causes of mobility degradation, lower ON drain-source currents and 1/f noise in OTFTs [47], [64]. That is also one of the reasons to consider working with OTFTs with shorter channel lengths. At 50 C, the chosen substrate heating temperature for the following electrical characterization, the grain size was



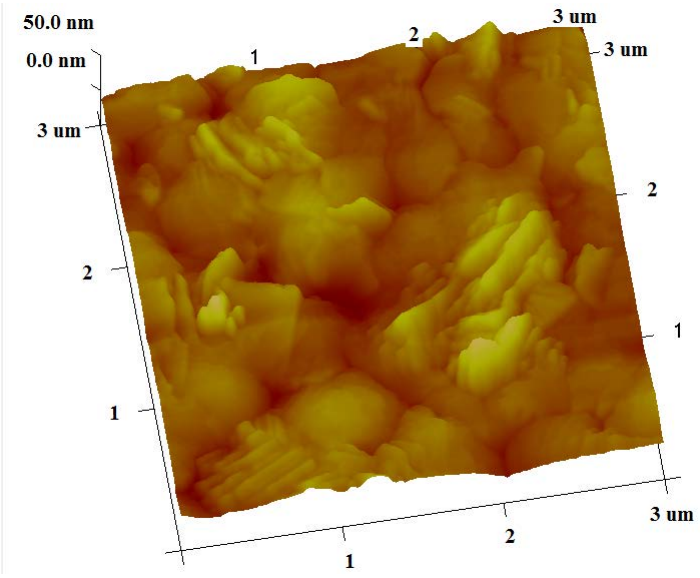
(a)



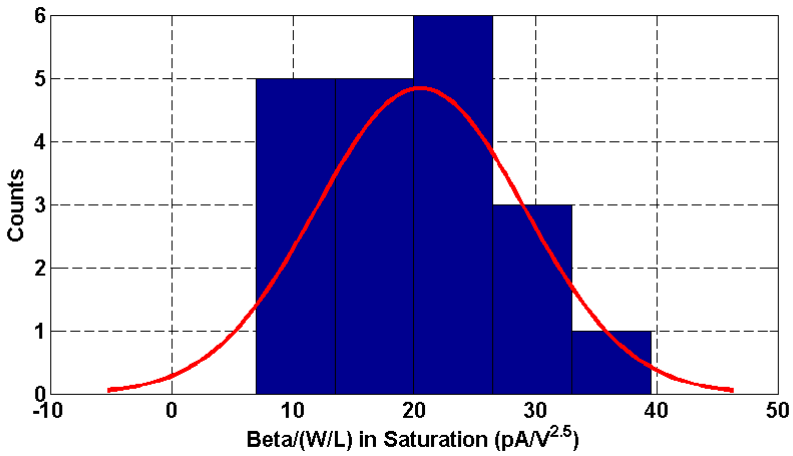
(b)

Fig. 3.3: a) Typical AFM images of Pentacene grains in the channel of an L=30μm OTFT with the substrates at T=25 C, during its deposition. The grains diameters are in average 0,5 μm. b) Histogram of the beta factor in saturation.

doubled attaining in average 1 μm x 1 μm of surface area and no more than 30 grains aligned in a 30 μm channel. The improvement in mobility was validated by the fitting of the histograms with a normal distribution, where it is seen on Table 3.1, that the percentage of variation is reduced. Unfortunately, a 40 % of variation is still large compared to c-Si MOSFETS, but normal for organic



(a)



(b)

Fig. 3.4: a) Typical AFM images of Pentacene grains in the channel of a L=30μm OTFTs with the substrates heated to T=50 C, during its deposition. b) Histogram of the beta factor in saturation. The diameter of the grain domains is doubled till 1μm, doubling the substrate heating temperature. Note that the parameter beta has less variation compared to Fig.3.3

transistors, however the principal objective of this work, is to quantify the current variation in percentage from one OTFT to the other, and to relate the principal parameters involved in the process (mobility, dielectric capacity, threshold voltage) to an electrical compact model for circuit design.

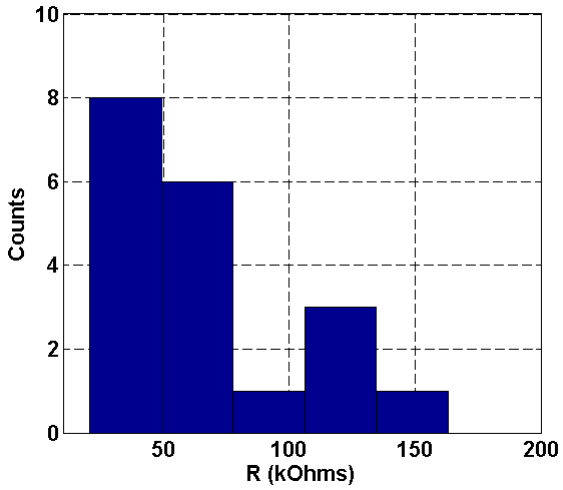


Fig. 3.5: Histogram of the computed source and drain contact resistance for several measured OTFTs.

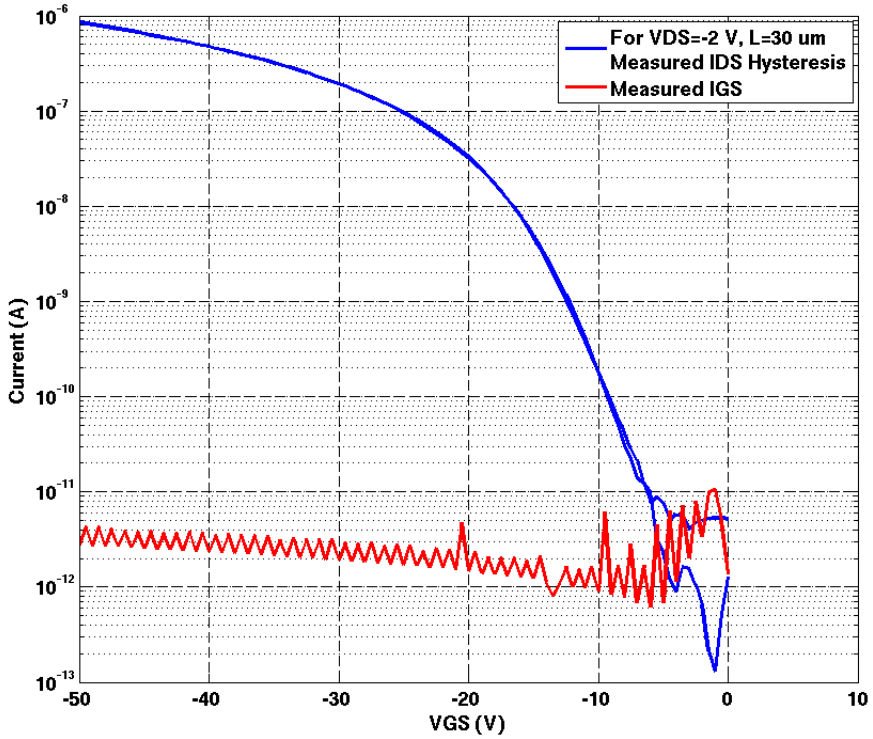
3.3.3 Source and Drain Metal Deposition and Contact Resistance Calculation

The metal layers are also deposited by thermal vacuum evaporation. Special attention is put for the gold deposition because of the critical interface with the pentacene. A good interface lower the contact resistance and facilitates the hole injection. At a gold source deposition temperature of 1500 C the speed of deposition is about 1 nm/min. Evaluating equation (3.2) with a V_{DS} in saturation, it is possible to compute the values of the contact resistance $R_{contacts\_d+s}$, for a group of OTFTs fabricated under the same conditions. On Fig.3.5, the histogram of these calculated values are shown where the majority of them are between 25 to 75 kΩ per 1 mm width or 2,5 to 7,5 kΩ-cm. As presented in the next section, the channel conductance parameter $g_{above-Th}$ is in the same order of magnitude as the transconductance Fig.3.13, which is about 1 μA/V, thus for a 5% error, the contact resistance could be neglected in the computation of the simplified equation (3.5).

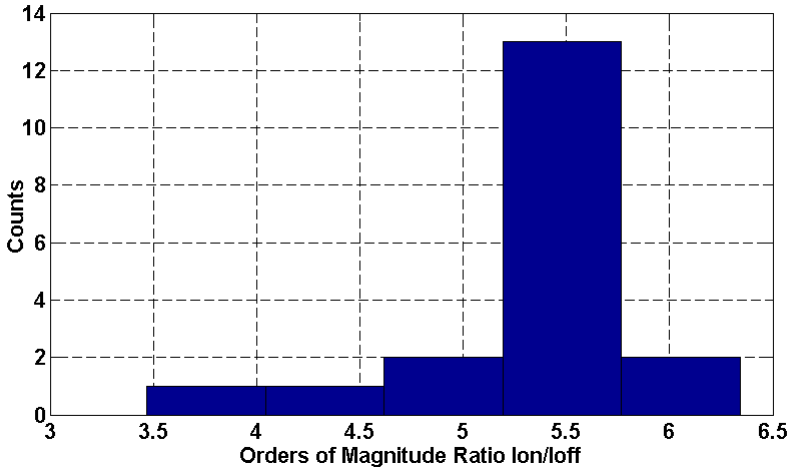
3.4 Electrical & Mismatch Characterization

3.4.1 Characteristics I-V Curves, Mobility and Ageing Effects

Fig.3.6(a) shows the transfer curve of a typical OTFT with an L=30μm and W=1000μm, with almost no hysteresis. Very low currents under 1 nA are obtained at a gate bias of 15 V, so this



(a)



(b)

Fig. 3.6: a) Transfer curve of hysteresis in blue and gate leakage current in red. b) Histogram of the ratio between the ON and the OFF drain source current

point is close to the subthreshold regime of the OTFTs. A typical curve of gate leakage current on red color is shown where values are very low, around 1 pA. The lack of hysteresis behavior, tells that a good polymeric gate dielectric layer with almost none trapped charges is deposited. Fig.3.6(b), shows the quantification of the ON/OFF drain source current ratio, where 5 to 6 orders of magnitude are clearly seen. This fact allows the simplification of the full a-Si TFT model in hand calculations, taking into account just the above threshold regime and neither the leakage, nor the subthreshold regime.

In one sample, under the same manufacturing conditions, 10 OTFTs were measured as shown in Fig.3.7 with the respective computation of the mobility dependence with the overdrive voltage. Values around 0,1 cm^2/Vs are clearly seen at higher gate source voltages. This is an important proof of the deposition of a good pentacene layer due to the presence of large grains and an stable source temperature during thermal evaporation. It is obvious that the mobility depends on the gate source voltage as often observed in polycrystaline organic transistors (not in OFETS based on organic single crystals).

On Fig.3.8, the ageing effects of the OTFTs in this technology are presented, where typical transfer curves of 2 OTFTs with L=30μm and 60μm were measured 2,5 and 5 months after manufacture. Although they were stored in a nitrogen glove box, they were exposed to air during the different measurement and handling conditions for a period of 2 hours during each measurement and repeated for several months. The ageing effects are presents, degrading the beta saturation factor by one order of magnitude after 2,5 months; however the OTFTs are still functional, which is in general positive, knowing that these transistors do not have yet a passivation layer against environmental degradation. This is an important point in the process of organic transistors and circuits because of the long-term reliability searched for industrial applications. The pentacene transistors functional after 5 months are a reliable result considering that other groups using experimental semiconductors, degradations are after hours of fabrication, e.g: [65]. A more detailed theoretical analysis and experiments will be needed in the future to quantify the mobility degradation in time to include in this compact model, similar to the ones done for c-Si CMOS transistors [66], [67].

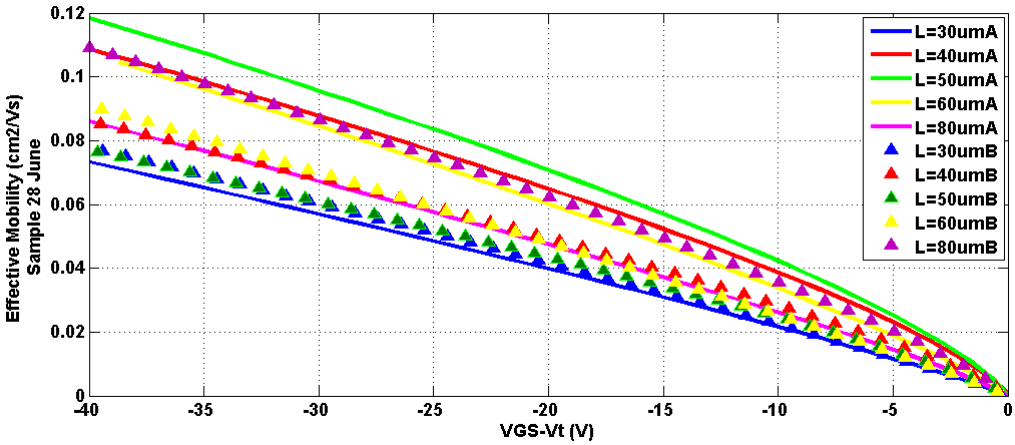
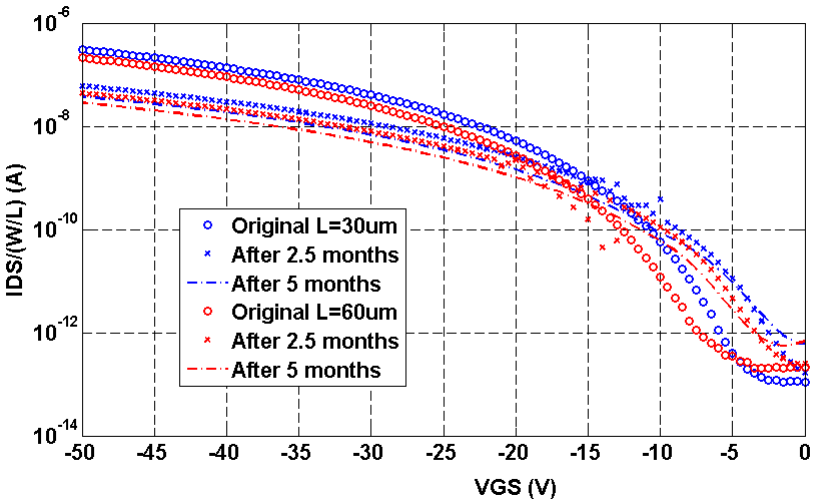


Fig. 3.7: Effective mobility vs. Overdrive voltage for 10 measured OTFT.

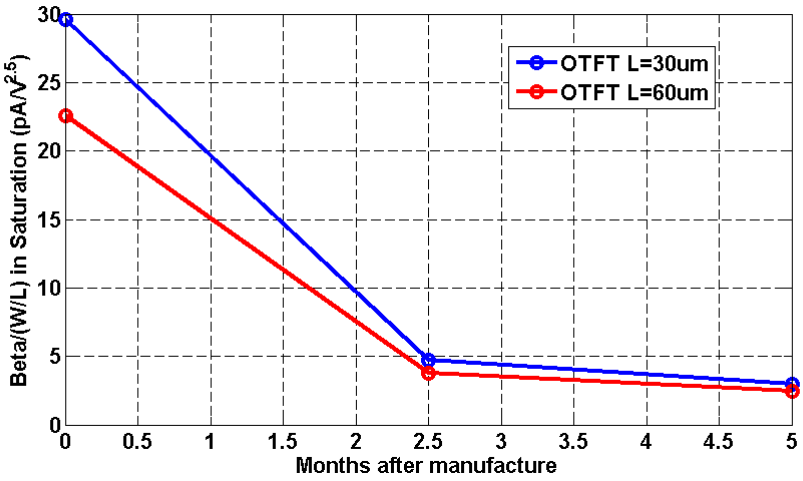
3.4.2 Modeling and Mismatch of Extracted Parameters in OTFTs

Fig.3.9 shows the fitted transfer and output curves (lines) and the experimental curves (circles) of a particular OTFT chosen (L=30μm). As stated before the width is always 1000μm for the masks used. Moreover, the fitting is almost perfect for the considered regime, which validates again the proposed model and which is useful for our purposes of circuit design. In the case of the non-fitted regimes, the transistors will be biased always in the above threshold regime to reduce at the minimum differences between simulation and real curves. On the next figures, the parameters extracted from the model are shown for several transistors, to quantify the performance of the technology. Similar to the procedure with the β_{sat} factor, a normal distribution was fitted with the histogram of the threshold voltage to quantify the variation of it. On Fig.3.10, the values of the threshold voltage are presented with a mean of -11 V and a standard deviation of 3,3 V. Fig.3.11, presents the power law factor of this technology, which demonstrates that the square law is present plus a dependency of the mobility with the square root of the overdrive voltage (γ parameter in the model) for a final power of 2,5.

The parameter λ (the channel modulation parameter) has a typical value of 0,006 V^{-1} thus it could be neglected too, considering that this technology uses longer channel OTFTs. The other parameters presented in the model: m (the linear slope of the output characteristic curves), and α_{sate} (the knee between the linear regime and the saturation regime of the output curves) have



(a)

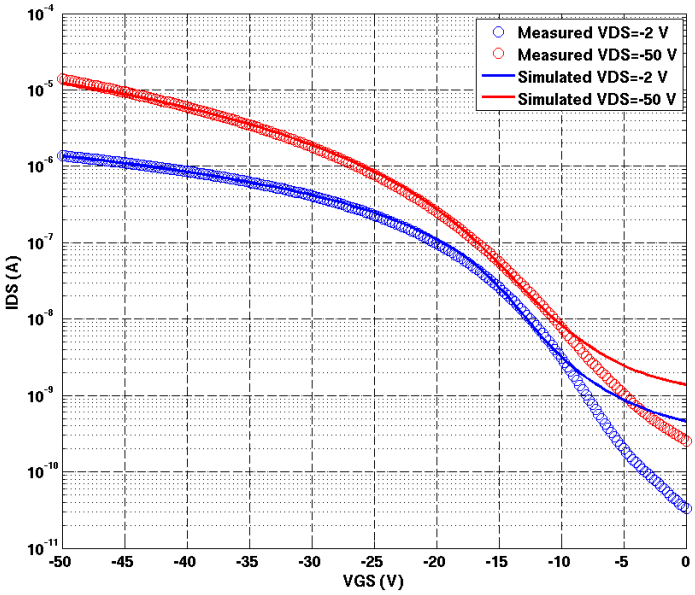


(b)

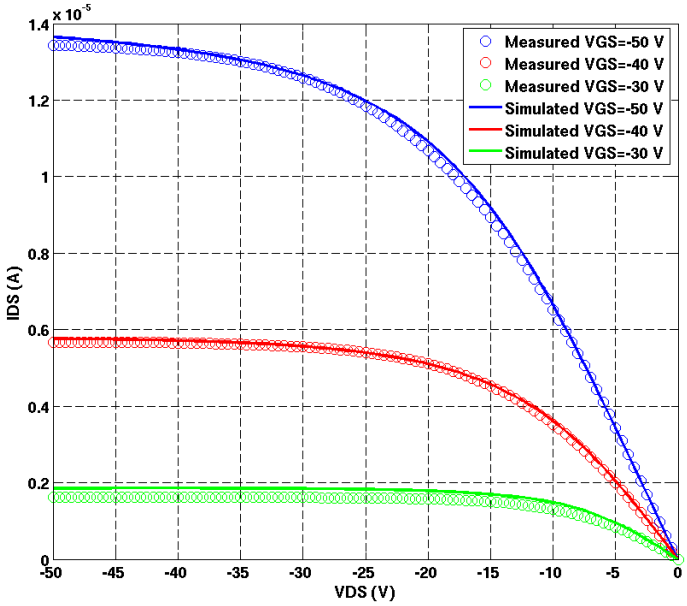
Fig. 3.8: a) Transfer curves in the linear regime for typical 30μm and 60μm channel length OTFT measured in the saturation regime, several months later. b) Degradation of beta factor in saturation with time.

been calculated. However in particular, these are numerical parameters which depend on each experimental curve and thus, they are not suitable in practice to take their average for Monte Carlo simulations in circuit analysis. Therefore typical values for the simulations are taken.

Fig.3.12 shows a superposition of the transfer curves in the saturation region of 15 OTFTs measured and normalized by their size ratio. The widths are in all the same (1mm), thus the contact resistance are of the same order of magnitude with the values mentioned above. As a first



(a)



(b)

Fig. 3.9: Experimental and fitted curves of a typical OTFT with 30μm channel length and 1000μm channel width. a) Transfer curves in the linear and in the saturation regime.b) Fitted output curves.

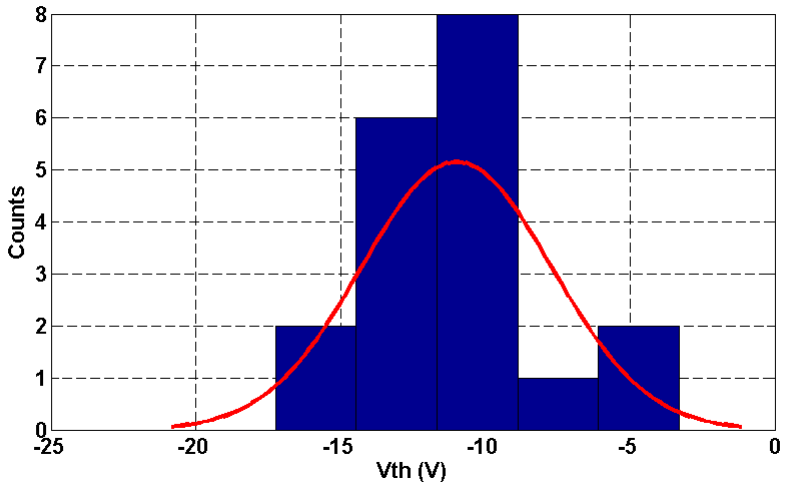


Fig. 3.10: Histogram of the threshold voltage for several measured OTFTs

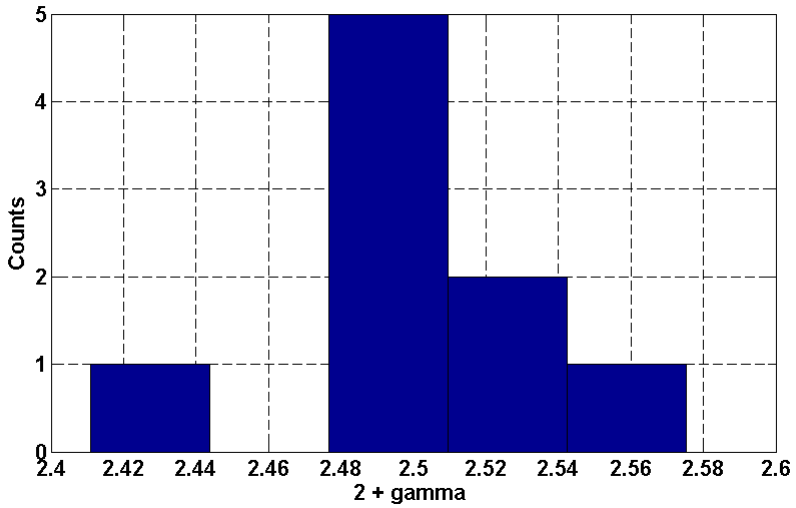


Fig. 3.11: Histogram of the 2+gamma power parameter

hypothesis and from a practical point of view, one can state that the physics is the same in all of them, without taking into account the different channel lengths. The samples were fabricated always with the same conditions, however as mentioned an intrinsic variation is observed, typical in organic transistors which disperses the transfer curves. Using the mismatch model (3.15) and the results for the parameters V_{Th}, γ and β_{sat}, it is possible to compute the percentage of variation in the drain source current:

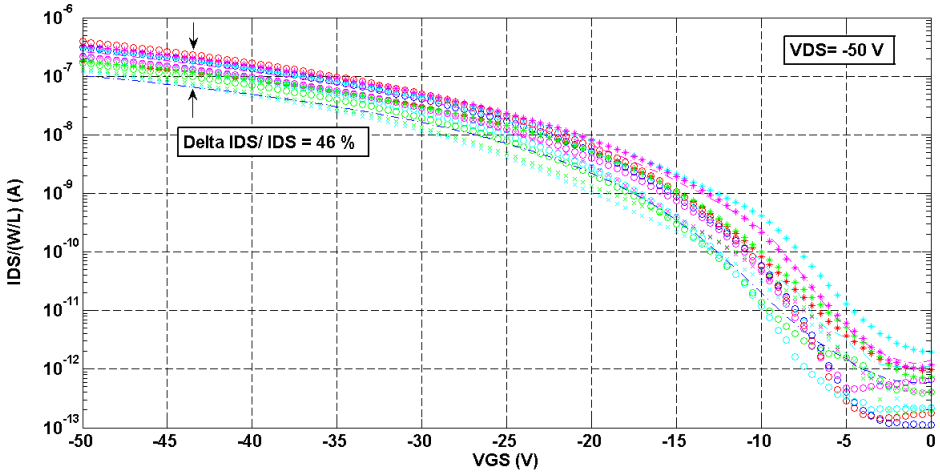


Fig. 3.12: Transfer curves for 15 OTFTs measured

$$\frac{\sigma^2_{I_{aboveTh}}}{\overline{I}^2_{aboveTh}} = (0.41)^2 + (2+0.5)^2 \frac{(3.3)^2}{[V_{GS} - (-11)]^2} \tag{3.16}$$

With a maximum bias V_{GS}=-50 V, we obtain:

$$\frac{\sigma_{I_{aboveTh}}}{\overline{I}_{aboveTh}} = 46,8\% \tag{3.17}$$

Although this current mismatch value is large for an analog designer; from a process point of view, it presents a real mapping from process to performance specifications for circuit design. It indicates also that the variation of threshold voltage could be a neglected quantity working at large gate bias (just 5% variation). However in order to improve even more the matching of OTFTs (e.g.: for mirror current sources or differential circuits), it is compulsory to reduce the spread pf values in the beta saturation factor by a SAM treatment in the dielectric-semiconductor interface, looking to reduce the grain boundaries across the channel. With the help of Monte Carlo simulations it is possible as well to determine the spread of the performance values (DC gain, frequency, etc.) in a simple circuit design, also similar to the procedures developped in [68].

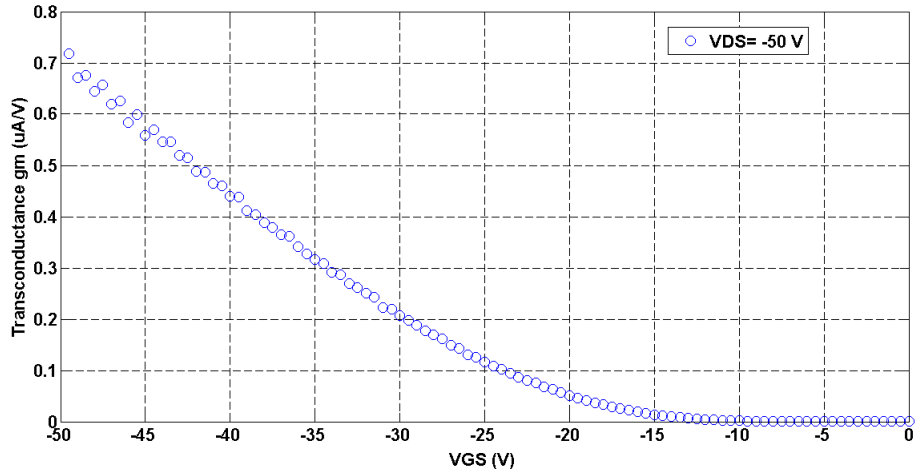
It is necessary in the future to develop a model which relates the threshold voltage and β_{sat} variations with more fundamental process parameters such as grain size and morphology, channel area, etc. In the case of organic transistors, the dependence of these variations with the square root of the inverse of the channel area is meaningless compared to the work developped by Pel-

grom [59] and Lakshmikumar [61]. In fact, there are no dopping steps in this process and by the contrary, when the channel is larger the presence of grain boundaries of the semiconductor are more important. As an hypothesis the Pelgrom's coefficient could be in the organic transistors directly dependent with the channel area W x L. However more theoretical work need to be done on this.

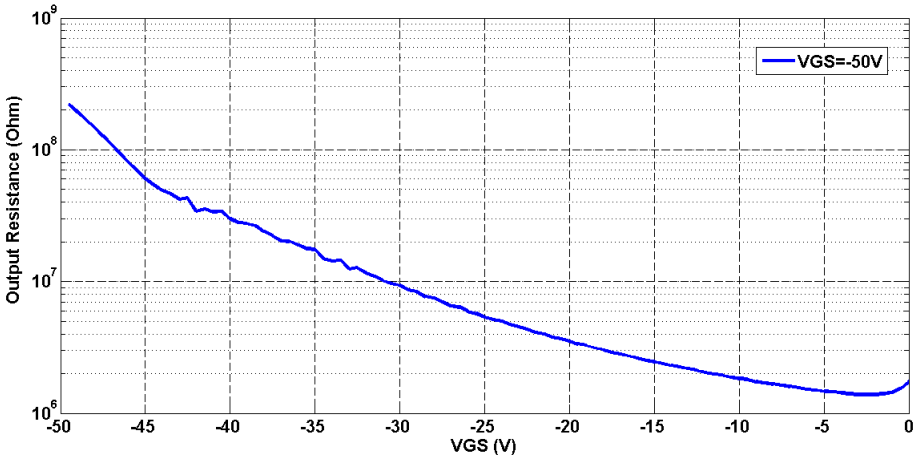
One can estimate the values of the transconductance g_m and the output resistance r_0, taking the slope of both transfer and output curves, on Fig.3.13. The values of the output resistance are around the order of magnitude of a typical c-Si CMOS transistor, however the values of the small signal transconductance (g_m) are quite low compared to them (3 orders of magnitude). These 2 values are important in the calculation of the intrinsic open loop gain of a transistor, $g_m r_0$ [3], as stated in the Table 3.2, where biasing the transistors at reasonables drain- and gate- source voltages of -35 V gives 3,6 V/V or 11 dB. A low DC gain. The low transconductance, which express literally the conversion of high values of gate-source voltage (tenths of volts) to low values of the drain-source current (about 1μA) is the principal reason of this low intrinsic gain in general, in organic transistors. In the case of c-Si transistors is the contrary, very low values of gate-source voltages (hundreds of milivolts) produce high values of drain-source currents (hundreds of μA). Finally, the transition frequency or frequency at 0 dB is roughly estimated according to typical values of mobility of 0,1 cm^2/Vs and overlap lengths of 30 μm after alingning shadow masks. As will be explained in chapter 5 with an organic transistor done by photolithography, the dynamic behavior in these transistors is still in research and the large variations of parameters such as mobility do not let to precise the values until the measurements will be done.

3.5 Conclusion

In this chapter, a procedure to engineer the manufacture of an experimental organic thin film transistor is presented. The characterization of important physical parameters such as the mobility and the ageing effects is also shown. A precise fit with the adapted a-Si TFT compact model already developed for SPICE simulators was demonstrated. A simple mismatch model developed from this Spice model was validated which allows to quantify the variation of drain source cur-



(a)



(b)

Fig. 3.13: a) Transconductance vs. Gate-source voltage. b) Output resistance vs. Drain-source voltage for an L=30μm OTFT.

rent values in different fabricated transistors. On Table 3.2 the summary of the parameters is presented which are also needed to be used in the Spice model for circuit design. These process corners, permits to analyze the impact of those intrinsic variations by Monte Carlo simulations in order to create more robust applications with organic transistors.

Table 3.2: Summary of parameters in the model for this OTFT technology

Parameter	**Mean (or nominal)**	**Std. Dev**
V_{Th} (V)	-11	3,3
β_{sat} $(pA/V^{2.5})$	2,05E-11	8,59E-12
γ	0,5	-
Max mobility(cm^2/Vs)	0,1+/-0,02	-
$C_{ox}(nF/cm^2)$	5+/-1	-
$R_{contact_d+s}$ (kΩ-cm)	2,5-7,5	-
λ (1/V)	0,006	-
Minimal L(μm)	30	-
g_m(μA/V)(V$_{GS} = -35V, V_{DS} = -35V$)	0,3	-
r_0(MΩ)(V$_{GS} = -35V, V_{DS} = -35V$)	12	-
$g_m r_0$(V/V)	3,6	-
f_t(kHz) (best case)	26,5	-

4

Low Power Organic Thin Film Transistors by Photolithography and Self-Alignment Process

4.1 Introduction

Organic Thin Film Transistors (OTFTs) are the basic building block of any active system implementing sensors, therefore in order to advance at the pace of the needs of the electronic industrial world four characteristic properties were improved in the course of this work. First of all that was the increase in the transition frequency of the transistors achieved by a decrease in the channel lengths down to 2 μm, (theory explained in section 4.1.1). This was obtained by fabricating our devices with a self-aligned photolithography process with reduced geometric overlap of the source and drain contacts with the gate to avoid parasitic capacitances, as will be explained in detail in section 4.2. Second, the decrease in the energy consumption by the decrease in the bias voltages achieved by reducing the dielectric thickness to the sub 100 nm range, as shown in section 4.2.3. Third, the increase in the gain bandwidth performance of the single transistors enabled by the improvement in the mobility of our semiconductor layer, by decreasing the grain density per channel length unit as it will be explained in 4.2.4. Finally it was necessary to increase the current levels at low voltages and to avoid any S-shape in the output curve in order to overcome the intrinsic noise of the devices. This was achieved by improving the charge carrier injection into the channel by using a Self Assembled Monolayer (SAM) treatment of the contacts. The electrical characteristics, demonstrating all these improvements are shown in section 4.3. Since the future goal was to develop circuits based on the aforementioned optimized OTFT technology, a modeling of the OTFTs transfer and output curves with an adapted a-Si TFT Spice model presented in commercial simulators (such as in [8]), was performed. The resulting parameter extraction is

described in section 4.3.3. Finally, the operating frequencies of the transistors are validated by the design and the electrical testing of different basic circuits.

4.1.1 Frequency Behavior of Transistors

Photolithography is not new for silicon electronics, however, there are few groups using it to pattern organic electronic devices e.g.: [69], [10]. As was explained in the introduction, the primary goal is the reduction of the channel length (L) and the nearly equally important secondary goal is to reduce the overlap lengths (represented by ΔL in Fig. 4.1) between the source and drain contacts to the gate contact as much as possible in order to decrease the parasitic overlap capacitances. Considering that in the saturation regime and in full accumulation (as the OTFTs do not have an inversion of the channel charges), the parasitic gate source capacitance is [70]:

$$C_{gs} = \frac{2W(L + \Delta L)C_{diel}}{3} \tag{4.1}$$

The 2/3 coefficient comes from the integration of the potential in the channel from the source to the drain during the accumulation of charges in the source side and the extinction of them in the drain side. Thus, the parasitic gate drain capacitance is just:

$$C_{gd} = \Delta L * W * C_{diel} \tag{4.2}$$

The transition frequency or frequency at 0 dB in a transistor is defined as :

$$f_t = \frac{g_{m-aboveTh}}{2\pi(C_{gs} + C_{gd})} \tag{4.3}$$

Replacing the parasitic capacitances equations in Eg. 4.3, we have:

$$f_t = \frac{\mu * C_{diel}\frac{W}{L}(V_{GS} - V_{Th})}{2\pi(\frac{2W(L+\Delta L)C_{diel}}{3} + \Delta L * W * C_{diel})} \tag{4.4}$$

Noting that in the saturation regime (and using the classical square power transistor model) $V_{DS,sat} >= V_{GS} - V_{Th}$, we have simplifying:

$$f_t <= \frac{3\mu}{4\pi}\frac{V_{DS,sat}}{L(L + \frac{5}{2}\Delta L)} \tag{4.5}$$

This equation shows that for small channel length devices the transition frequency is not only determined by L, but to an equal extent by the overlap length ΔL, which imposes a non-negligible gate capacitance. Therefore, it would be desirable to reduce the overlap length to about hundred nanometers in order to avoid additional limitation of the transition frequency. Zero overlap, on the other hand, is not recommendable since it would strongly deteriorate the charge carrier injection. It is important to note, that the transition frequency depends on the mobility as well. In fact, compared to crystalline silicon, organic semiconductors have very low charge carrier mobility values (around 1 cm^2/Vs in the best case). Even if the channel lengths were reduced to the nanometric scale, OTFTs will never work as fast as crystalline silicon ones. For example, for a VDS_{sat} = -3,5V, a typical low mobility of 0,01 cm^2/Vs, a channel length L = 2 μm and an overlap length of 0,25 μm, the transition frequency f_t would be no more than 159 kHz. It is important to note 2 points about this calculation, first: the dynamic behavior of organic transistors is still a matter of research and second: the large device-to-device variation of the mobility stemming from a lack of control of the dielectric interface properties and thus the grain morphology. This then induces a large variation in the transition frequency.

4.2 Manufacturing Technology Process

In this chapter, we are working with Organic Thin Film Transistors (OTFTs) with an aluminum gate, a dielectric fabricated with an experimental dense polymer called PNDPE, gold source and drain contacts and using also the commercially available organic semiconductor pentacene, because of its acceptable stability in air, its reasonable mobility 0,1 cm^2/Vs and because of the long term experience gained before [63] in controlling its deposition. The OTFTs described here have bottom gate and bottom source-drain geometry as shown in Fig. 4.1. Typically the electrodes of OTFTs are patterned by shadow masking with a minimum resolution of about 10 μm, however, since the idea of this work was to decrease the channel lengths to some μm, contact photolithography was used for the electrode definition. In the next section 4.2.1 a detailed introduction to the photolithographic process using plastic materials, the engineering of the dielectric and semiconductor layers is presented.

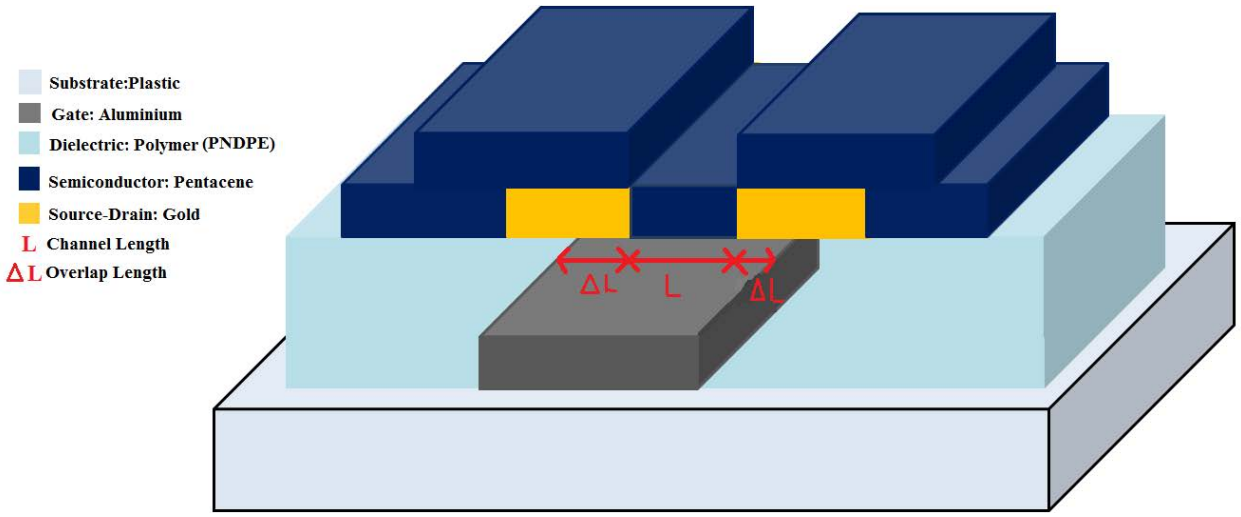


Fig. 4.1: 3D image of Joanneum Research?s Organic Thin Film Transistor layout with a bottom gate-bottom contact transistor geometry. Note the remark in red with the overlap and channel length.

4.2.1 Photolithography and Self Alignment Process Technology

Fig. 4.2 is an overview of the fabrication of organic transistors following the procedure described in Ref. [71]. The most important steps involved with the back and front patterning of the source and drain contacts, are presented. In order to produce mechanically flexible devices, a flexible and transparent 175 μm PET (Polyethylene Terephthalate) substrate foil was used with a smooth surface of less than 1 nm of roughness. The total sample size can be as large as 10 cm x 10 cm. The first step, A) in the figure shows the gate electrode which is the result of the photolithography patterning process. This process works as follows: First a two-layer resist, consisting of a sacrificial layer and a positive photoresist layer, is applied by spin-coating followed by a bake step. Next, the double resist layer is UV-exposed. A first phase of development will remove the exposed areas. Then upon further development, the sacrificial layer is removed from the opened areas and at the edges of the exposed photoresist, thus creating a resist edge with an undercut. After depositing a layer of Aluminum of 60 nm thickness all over the substrate the aluminum-coated photoresist is lifted-off from the non-exposed areas with a photoresist remover in an ultrasonic bath. In B), the dielectric layer is then deposited by spin coating an ultra-thin layer of 80 nm of a photosensistive polymer- poly ((+/-)endo,exobicyclo[2.2.1]hept-5-ene-2,3-dicarboxylic acid, diphenylester) (PNDPE) - and patterned directly by UV exposure. This dielectric layer is explained in detail in

Ref. [12]. After the UV exposure, the non-patterned areas are removed in solvent bath (few seconds). In C) the first step of the self-alignment procedure used for source and drain patterning is depicted, where a double layer resist consisting of a sacrificial layer (not shown in the figure) and a photoresist layer are deposited by spin-coating. In D) the substrate is subject to a UV-exposure through the reverse side of it where the gate is used as a UV-blocking exposure structure and therefore as an intrinsic photomask (to define and align the source and drain contacts with the gate). In reality, the overlap of the source and drain is still present as shown in Ref. [71] by FIB and TEM measurements, which could be due to the diffraction of the UV light through the different substrates materials or due to scattering. Then, another photolithography step is performed by UV-exposure from the front side of the substrate in order to define gate pads, crossings and vias to the gate electrode (this front side exposure step is not shown in the figure). In E) both the sacrificial plus the photoresist layer are developed thus resulting in a removal of the exposed photoresist areas and an undercut profile of the remaining photoresist areas (the undercut is a result of the development of the sacrificial layer, see A). In F) an adhesion layer of 2 nm of chrome (not shown in the figure) plus 50 nm of gold are deposited all over the substrate. In G) the photoresist layer, which remained in E) plus the overlaying gold layer are lifted off by a photoresist remover plus a hard solvent plus a water rinse [72]. The main risk in the lift-off step is the creation of a lift of the edges of the gold contacts (as we will see in the next section) that may deform the interface to the semiconductor and may increase the contact resistance. Next (not shown in the figure), after solvent-based cleaning of the source and drain gold contacts, the sample is submerged in a liquid solution containing the precursor of a Self-Assembled Monolayer (SAM), which grows to around 1-2 nm specifically over the gold surfaces. This (SAM) treatment, explained in detail in Ref. [73], [74] and [75], should enable the reduction of the contact resistance of the metal-semiconductor interface, enhancing the injection of charges into the channel. Finally in H), a 35 nm layer of the organic semiconductor pentacene from Sigma-Aldrich ™ (purified to 99,97 %) is deposited by PVD through a shadow mask. The first 5 nm were deposited at a very low and constant rate of 0,01 A/s to enable the growth of large semiconductor grains by a minimization of the nucleation density in the first monolayers. The next 25 nm of the OSC layer are deposited at a constant speed of 0,1 A/s.

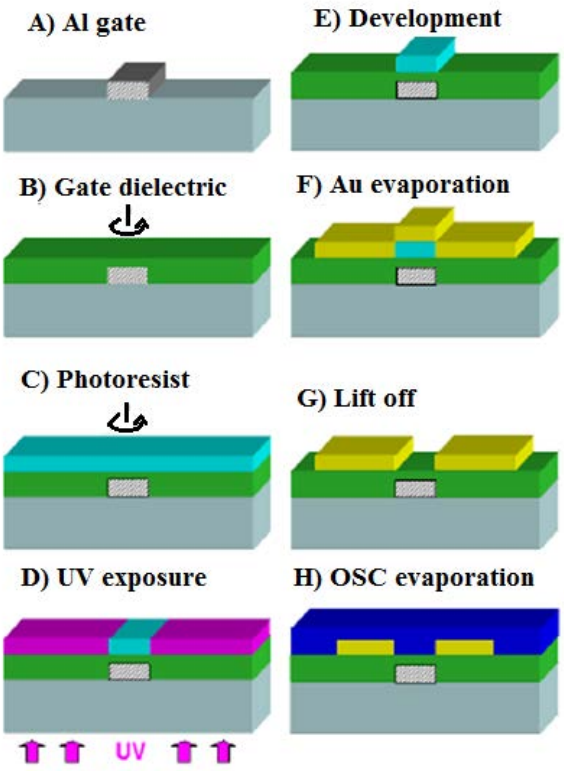


Fig. 4.2: Fabrication process of organic thin film transistors by photolithography, self-aligning the source and drain contacts with the gate.

4.2.2 Issues and Difficulties of Manufacturing Structures by Photolithography

There are several obstacles to surmount in order to allow for a commercialization of the OTFT technology based on the described self-aligned photolithography process. From Fig. 4.3, some of the principal causes of bad working devices or even killer defects can be identified. In A) a dust particle is present in a 5 μm long channel which cuts the interdigitated electrodes thus having a channel width reducing impact. The presence of smaller dust particles compared to the channel during all the steps could cause besides the reducing of the width, the localized increase of the current density till values which could break the transistor. Therefore an optimum clean room is necessary to avoid these particles. In B) a killer defect is shown, where the fingers of the contacts are almost completely lifted off. This is either due to an overdevelopment of the sacrificial layer or due to a lack of adhesion of the sacrificial layer to the substrate. After optimization of the development time of the layer, a better control of the sacrificial resist was obtained, sticking it

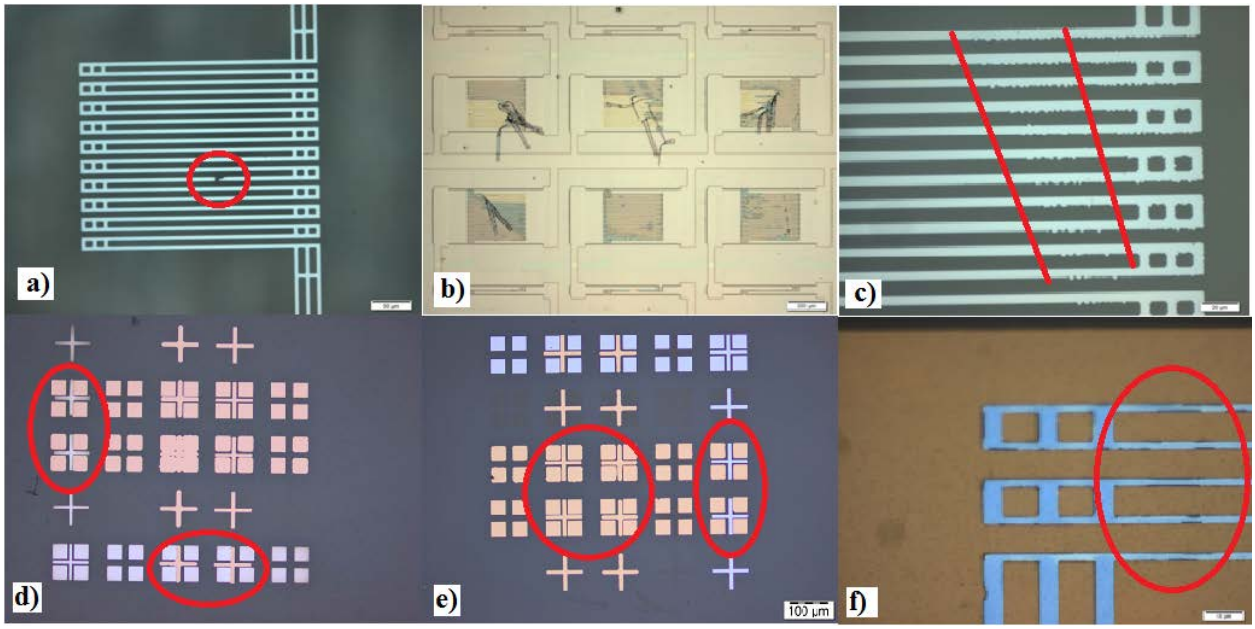


Fig. 4.3: Several typical defects occurring during the fabrication of organic thin film transistors by photolithography.

more to the dielectric. In C) the electrode edges (and therefore the channel lengths) are not well defined due to defects of the photo-mask. This would allow the exposure of a larger zone. In a first approach, these defects are not critical, due to the fact that they only induce a small variation of the channel lengths in the range of nanometers. This can be neglected as compared to the local variations in the charge carrier mobility. Another defect is shown in D), stemming from a misalignment of the front side exposure step to the reverse side exposure step, here represented by the crosses and the squares. The correct alignment is shown in E) The defects shown in F) are metal flags (called "batman ears") that are caused by a lack of undercut, most likely because the sacrificial layer was not sufficiently developed. They occur, because the metal has to break during the resist lift-off. With a proper undercut the evaporated metal becomes discontinuous at the edge of the resist, thus forming a predetermined breaking point. High "batman ears" at the gate electrode edges (as shown in the Figure F) may break the gate dielectric and may induce high leakage currents which are destroying the performance and integrity of the device. Metal flags at the edges of the source and drain electrodes most probably will increase the contact resistance and may deteriorate the IV-curves of the transistors by inducing a non-linear current contribution at low voltages (S-shape).

4.2.3 Engineering the Polymeric Gate Dielectric

As already mentioned an in-house developed ultra-thin and dense dielectric made of PNDPE was used [12]. The dielectric layer thickness was decreased to the thinnest acceptable and reproducible thickness in order to reduce the threshold-, gate-source and drain-source voltages and simultaneously keeping the currents at values of tenths of μA. It is important to note that the gate dielectric has to withstand all subsequent photolithographic steps without damage. In Ref. [12] a dielectric layer thickness below 50 nm was acceptable, because of the solvent-free shadow mask patterning of the channel contacts. This turned out to be not the case for OTFTs with self-aligned photolithographic patterning of the electrodes. Here a thicker dielectric layer resulted in higher reproducibility. In the microscope image in Fig. 4.4, the edge of an 80 nm PNDPE layer patterned around a capacitor structure is clearly visible. The current density of such a capacitor is presented in Fig.4.5. At voltages below 5V a current density below 0,1 nA per mm^2 was observed. Accordingly, for a 10 mm wide OTFT with an overlap of less than 500 nm, the leakage current from the gate through the dielectric would be less than 1 pA, which is an excellent performance given how thin the dielectric is.

Finally, several capacitors in different samples were characterized with an LCR meter, the results are summarized in Table. 4.1. Quite larger sizes of 0,08mm^2 were tested and a specific capacitance value between 20 to 30 nF/cm^2 was extracted. The phase angle of -90 degrees proves that there were almost no parasitic parallel resistances or leakage sources. Assuming a dielectric constant of 2,8 results in calculated thickness values between 80 and 130 nm and an average thickness of 100 nm with a variation of 20 nm (20%). From an electrical point of view the average capacitance is 25 nF/cm^2 with a variation of 5 nF/cm^2 (20%). Such a thickness variation is typical for spin-on processes of polymers.

4.2.4 Engineering the Semiconductor Pentacene Layer

The active layer in an OTFT is the semiconductor layer. Here the commercially available organic semiconductor pentacene is also used, which as explained in this thesis work, it is well known for its acceptable stability in air for hours or days, its reasonable mobility, in best case ranging

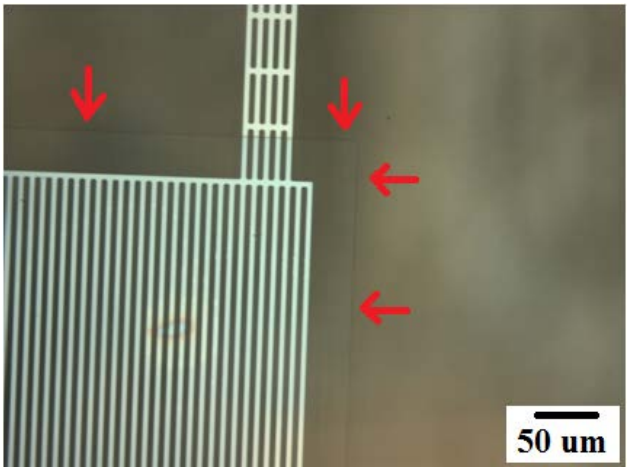


Fig. 4.4: Edge of the dielectric layer after precise patterning.

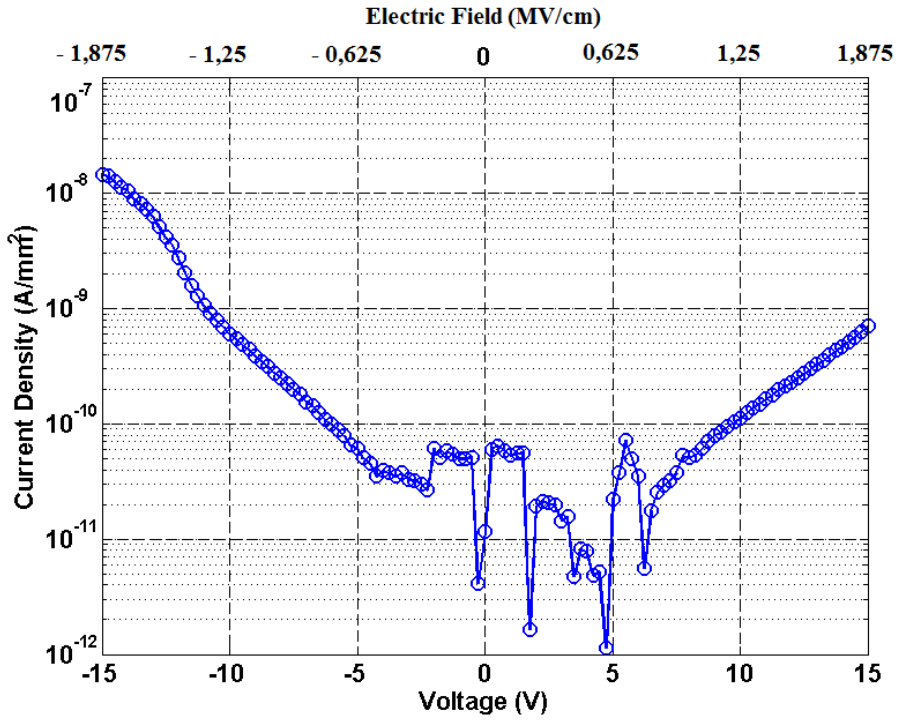


Fig. 4.5: Current density of a capacitor with 80 nm of thickness

from 0,1 cm^2/Vs to 1 cm^2/Vs, and its good interface to polymeric dielectrics such as SU-8 and PMMA [10], [53]. An optical microscopy image of the channel region of an OTFT with L = 5 μm reveals that only 2-3 grains are bridging the channel contacts (Fig. 4.6) probably due to very low deposition speed of 0,1 A/s. In Fig. 4.7 the gate voltage dependence of the charge carrier mobility

Table 4.1: Dielectric characterization of several capacitors

Sample size	Capacitor area (mm^2)	Phase angle ()	Capacitance (nF/cm^2)	Thickness (nm)
4 in x 4 in	0,04	-89,4	29,6	83,8
4 in x 4 in	0,04	-89,5	29,3	84,5
1 in x 1 in	0,08	-88,5	24,5	101,0
1 in x 1 in	0,08	-88,4	26,0	95,3
1 in x 1 in	0,08	-89,3	22,2	111,0
1 in x 1 in	0,08	-89,3	19,4	127,0

(as deduced from the transfer characteristics) of an OTFT with a 10 mm wide and 2 μm long channel is plotted, showing no hysteresis between forward and reverse gate voltage sweep. As explained in chapter 2, recent models such as [6] and [9] have described the voltage dependence of the effective mobility μ_{eff} according to $\mu_{eff} = \mu_0 ((V_{GS} - V_{Th})/V_{aa})^{\gamma}$, where again μ_0, V_{aa} and γ are numerical parameters of the model. Although mobility values around 0,01 cm^2/Vs seem to be rather low, these are typical values for an OTFT with a bottom contact structure (e.g.: [2]) where the injection barrier (or contact resistance) from the source to the semiconductor is much higher than for top contact devices.

4.3 Electrical Characterization

For the electrical characterization of the performance of a large number of OTFTs a special mask set was designed, the final sample is shown in Fig. 4.8. OTFTs with large widths up to 10 mm and 14 mm and short channel lengths down to 2μm and 5 μm were fabricated in order to maximize the transconductance which is an important parameter in the design of analog circuits.

4.3.1 Gate Leakage Current Voltage Curves

In order to test the integrity of the ultra-thin gate dielectric after the whole patterning process apart from large OTFTs also large area capacitors were included in the design. As shown in Fig. 4.9 the gate leakage currents of large OTFTs were as low as 15 to 20 pA at low voltages. The fact,

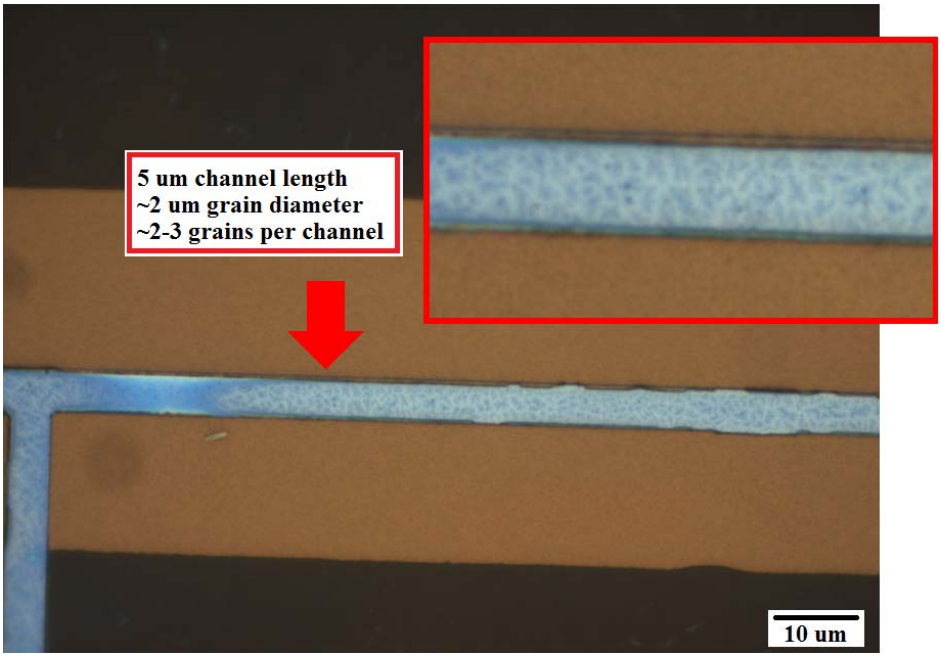


Fig. 4.6: Microscope image of the channel region of an OTFT with a channel length of 5 μm. Note, that in the zoomed image only 2-3 grains are present between the contact edges.

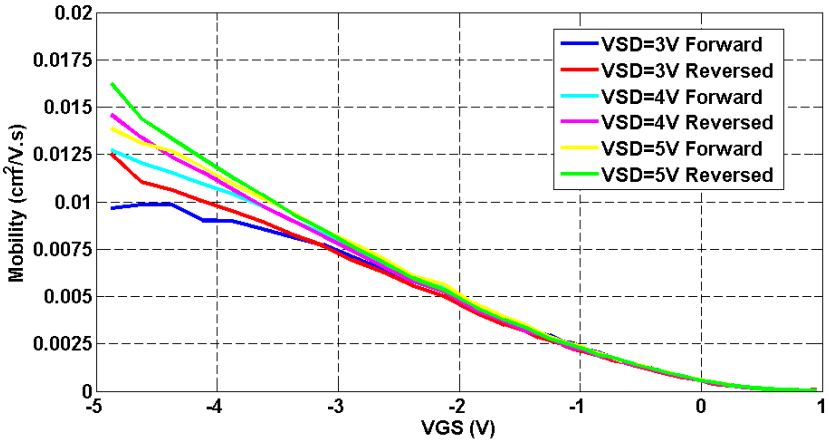


Fig. 4.7: Saturation mobility vs. gate-source voltage of a 10 mm wide and a 2 μm channel long OTFT in forward and reverse bias measurement.

that the curves have no spikes in all of the gate source voltage sweeps reflects that there are no pinholes in the dielectric layer.

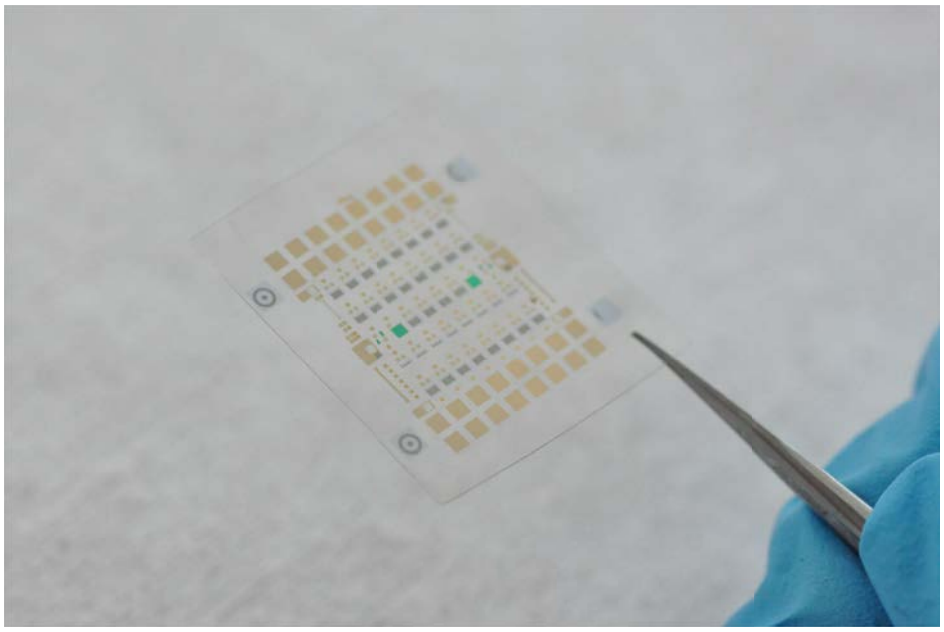


Fig. 4.8: Photo of the sample fabricated for testing OTFTs with very large widths and short channel length and large-area capacitors. Active area 1 inch square.

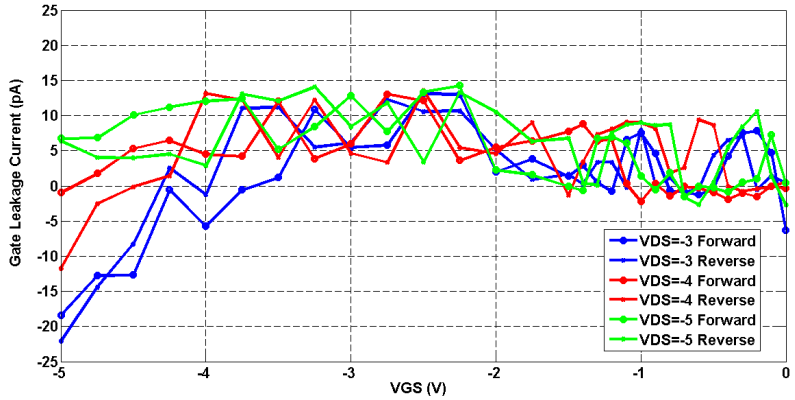
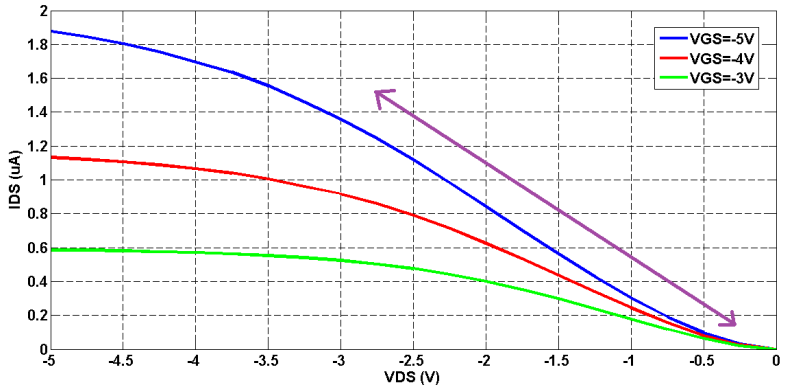


Fig. 4.9: Gate leakage current in an OTFT of width = 10 mm and length = 2 μm

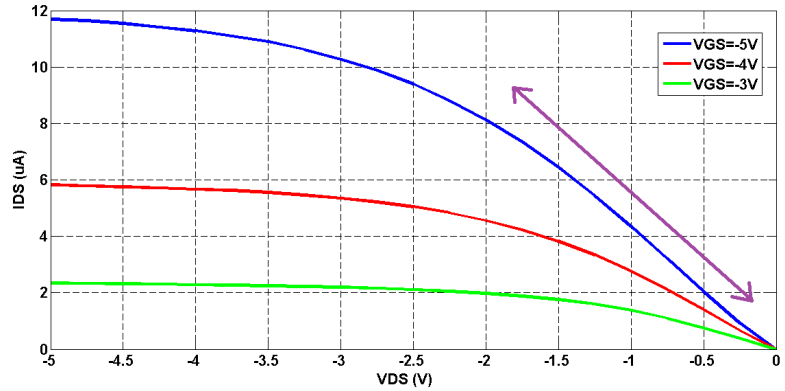
4.3.2 Engineering the Source and Drain Contact Resistance

The existence of a contact resistance in devices with bottom contact geometry (which cannot be avoided in OTFTs with photlithographically patterned contacts) is also well known from the classical semiconductor physics. Here the junction of a metal and a semiconductor creates a non-linear or diode-like behavior with the free charge carriers (holes in the case of pentacene OTFTs) being transported across the interface in one direction (from the metal to the semiconductor in

pentacene OTFTs) when there is a barrier lowering due to a voltage applied (forward bias) or due to the presence of another layer of material. The latter effect is enabled by an increase of the local doping concentration in inorganic semiconductors or by a SAM treatment in organic semiconductor devices. Accordingly, it is useless to compute the value of the contact resistance presented in some models such as in the adapted a-Si TFT when there is a non linear current voltage behavior present in the interface between the contacts and the semiconductor. Other models such as [6] allows modelling the devices with this non-vanishing contact resistance by introducing an inverted biased diode at the contact node. The output curves in Fig. 4.10(a) show a significant non linear behavior (called S-Shape and indicated with a violet arrow) at lower drain source voltage with almost a non saturation of the curves at higher drain source voltages values. After a collaboration with Andreas Petritz from Joanneum Research who was starting to develop this improvement in the process technology, the contact barrier was lowered significantly, and the hole injection was increased, by adding another material at the interface that enables an adjustment of the highest occupied molecular orbital (HOMO) levels of the pentacene to the work function of the gold contacts. Following a procedure described in citeDeBoer05 and in [74], the sample was placed in a liquid solution of a SAM of 3,3,4,4,5,5,6,6,7,7,8,8,9,9,10,10,10-heptadecafluoro-1-decanethiols (dissolved in alcohol) after the gold evaporation and lift off step, thus creating a dipole at the interface, which increases the work function of Au and decreases the HOMO levels of the semiconductor. In order to improve the growth of the SAMs (its thiol molecules are prone to grow just on the gold), a cleaning step ([75]) was added immediately after the lift off. For that the samples were submerged in an appropriate solvent solution plus an ultrasonic bath and then cleaned again with a solution composed of Potassium Hydroxide and Hydrogen Peroxide. This rigorous cleaning step removes any residual polymeric layer from the gold surfaces. The results are shown in Fig. 4.10(b), where one obtains a completely linear behavior in the output curves without any sign for S-shapes. The saturation region is also better visible as a flattening of the curves at higher drain source voltages compared to the ones in Fig. 4.10(a). This saturation is important because it demonstrates the increase in the output resistance of the transistor. Ideally, a fully saturated curve implies an infinite output resistance, which is beneficial for the use of OTFTs as a load in analog amplifiers.



(a)



(b)

Fig. 4.10: a)Measured output curves of the same OTFT. The violet arrow indicates the S-Shape characteristic of a non-linear contact resistance or injection in the channel. b) Measured output curves of the same OTFT. The violet arrow indicates the S-Shape characteristic of a non-linear contact resistance or injection in the channel.

4.3.3 Extraction of Parameters and Modeling of OTFTs

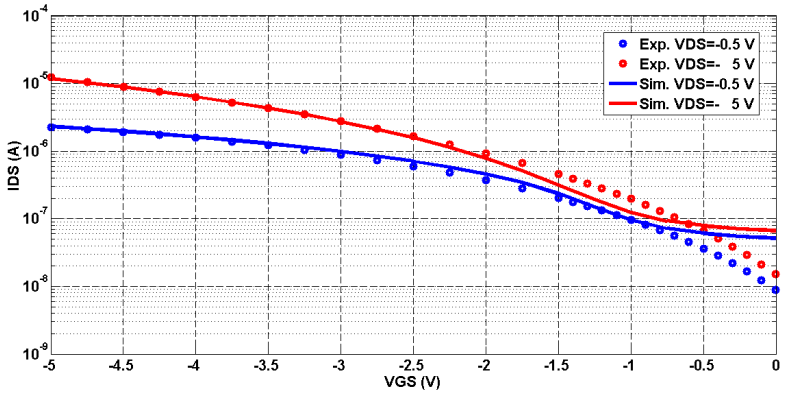
For circuit design based on the described self-aligned OTFTs, the electrical data have to be simulated by a Spice model. That was implemented by adapting an a-Si TFT model (as presented in some commercial Spice simulators [8]), where the physical equations in the regime above threshold are similar to the ones in organic transistors. In addition, the model prior developed in the research group [9] should be tested for analog design as well, where a precise fitting is necessary. The principal equation of the drain source current in the above threshold regime were already presented in chapter 2 and 3, for clarity, they are included here again. From Eq. 3.2, it is seen

Table 4.2: Summary of parameters in the model for our OTFT technology

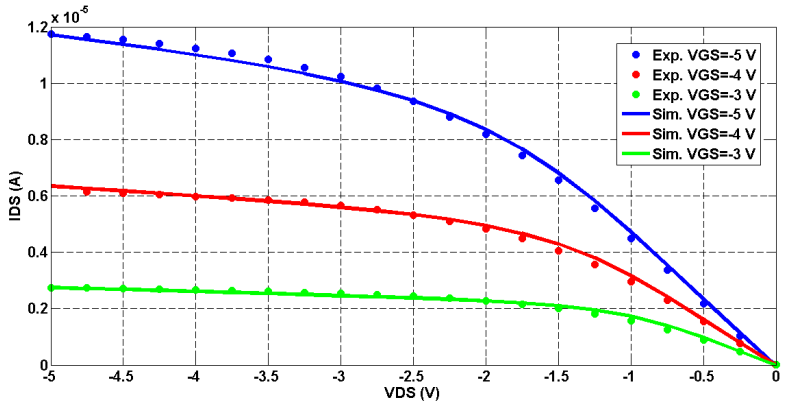
Parameter	**Nominal value**
V_{Th} (V)	-0,78
γ	0,61
$\mu_0(cm^2/Vs)$	0,0125+/-0,0025
$C_{ox}(nF/cm^2)$	25+/-5
$R_{contact,d-s}$ (kΩ-cm)	10,15
λ (1/V)	0,05
Minimal L(μm)	2
g_m(μA/V)(V_{GS}=-3V,V_{DS}=-5V)	3
r_0(MΩ)(V_{GS}=-3V,V_{DS}=-5V)	15
$g_m r_0$(V/V)	45
f_t(kHz) (best case)	159

that the current is linearly dependent on the drain source voltage and proportional to the parallel combination of the contact resistance in the drain and source and the inverse of the channel conductance parameter. This channel conductance parameter is dependent on the gate-source voltage. The critical physical parameters that were extracted according to a conventional process as described by Ref. [6] are compiled in Table 4.2. The exact value of the contact resistance is 7,25 kΩ (= 10,15 kΩ-cm, width normalized contact resistance). Although it is not straightforward to compare the values reported in the literature (due to the different methods used there and the different channel widths) the extracted resistance value on hand is almost 3 orders of magnitude lower than the one reported in Ref. [1] (based on an extraction with a more complex physical equation) and 2 orders of magnitude lower than values calculated previously in Ref. [6].

Again, it has to be stated that the numerical parameters A, V_{aa} and α_{sate} are just for a mathematical adjustment of the equation and are not of physical importance. They are not shown in the table, even if they are present in the model. These parameters need to be replaced in a future version of the model with physical ones. The γ parameter indicates as well in this case that



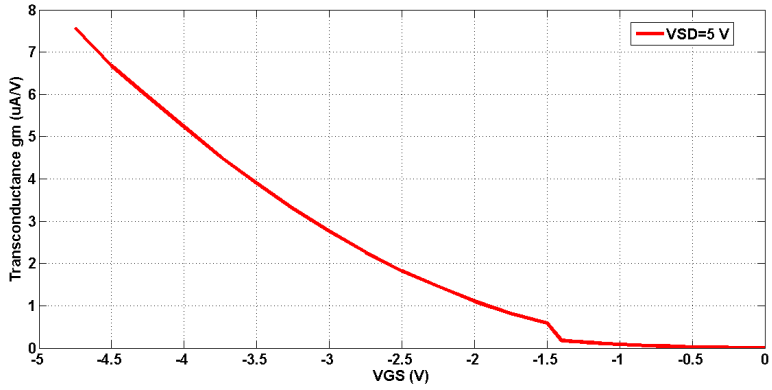
(a)



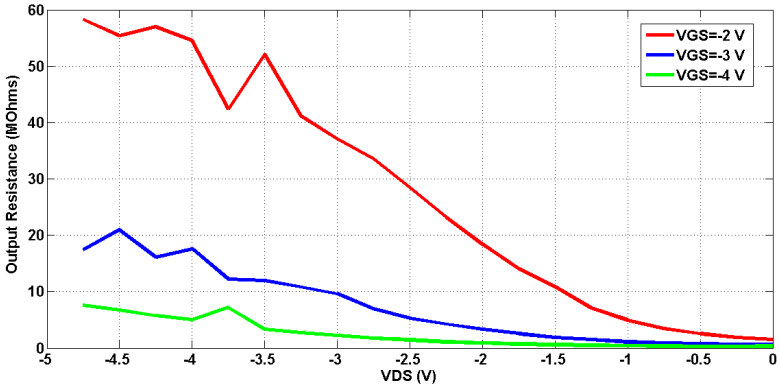
(b)

Fig. 4.11: a) Comparison of measured and modelled transfer curve of an OTFT with W = 14 mm and L = 2 μm. b) Comparison of measured and modelled output curves of the same OTFT.

the total power of the drain source equation is not squared, but 2,61 which is non-negligible in circuit design. The result of the adjustment is seen in Fig. 4.11, where the transfer and output curves measured are presented with dots and the lines represent the modeled ones. Again, it has to be emphasized that this model is physically valid only in the above threshold regime. Finally, from the curves in Fig. 4.11 the transconductance and the output resistance of the OTFTs were calculated and presented in Fig. 4.12. As stated before, these values depend on the bias and the transistor dimensions. An estimation of the intrinsic DC gain of a transistor from the last figures is presented in Table 4.2, where a value of 45 V/V or 33 dB at the best case.



(a)



(b)

Fig. 4.12: a) Calculated transconductance from the OTFT of Fig. 4.11(a) b) Calculated output conductance of the same OTFT.

4.4 Conclusion

This work demonstrates several important performance optimizations of self-aligned OTFTs. A photolithographic process for fabrication of short channel OTFTs (L = 2 μm), source and drain contacts self-aligned to the gate was successfully elaborated . The PNDPE-based dielectric was optimized towards an ultra-thin (80 nm), dense and pin-hole free gate dielectric layer, sufficiently robust against the subsequent steps of etching and lift-off thus showing reproducible integrity. The leakage currents are below 20 pA in OTFTs with large channel widths. The semiconductor evaporation process was optimized in order to have a small grain density in the channel with about 2 to 3 grains between the contacts. The mobility values are on the order of 0,01 cm^2/Vs,

which can be further improved by additional interface treatments of the dielectric. The source and drain contact interface with the semiconductor was improved by reducing the injection barrier through a combination of a cleaning step with a thiol SAM treatment. As a consequence, the contact resistance could be decreased to about 10,15 k-cm as calculated with an adapted a-Si TFT model thus delivering an S-shape-free output characteristics. This model was successfully fitted to the measured data in the above threshold regime and it will be further used for circuit design.

Part III

Circuit Design

5

Design of Functional Analog Circuits with Few Organic Transistors

5.1 Introduction

As mentioned in chapter 2, other groups have been working as well, with moderate resolution ADCs and DACs that have been succesfully tested [21], [23], [24] and functional amplifiers and comparators [19], [15], [17], [14].

In this chapter, the design of 2 simple and functional analog blocks with few OTFTs (two dozens) is presented, using the two technologies shown in chapter 3 and 4. The goal is to have well working circuits by construction with theoretical analysis and simulations with realistic parameter values. A fully differential voltage amplifier and a fully differential comparator are detailed on section 5.3 and 5.4, respectively. This thesis targets the design of an analog to digital converter (ADC) as a front-end for sensor signal processing working at low frequencies, < 1 KHz. The design of a first order Sigma Delta Modulator using these 2 blocks is presented in section 5.5. A final system of 25 OTFTs and 4 passive elements will be shown. The designs with both technologies are simulated and compared in this chapter in order to formalize a design procedure. The implementation in plastic electronics notably with the Joanneum Research Technology is shown in the next chapter.

The number of OTFTs is a key concept in the design philosophy of this thesis work: "simple designs equals minimal performance variations". This is due to the fact that organic transistors are not fully reliable due to the degradation in air of the semiconductor layer, the variation in the grain morphology and by consequence in the moblity, and the lack of uniformity of the dielectric thickness, all these facts explained in chapter 3 and 4. Therefore, Monte Carlo simulations were

done in section 5.6 to quantify the yield of well-working amplifiers with the help of the statistical analysis of the parameters extracted in chapter 3.

5.2 Gain Equations of a Diode Load Amplifier

As presented in chapter 3, the equation of the drain source current in the above threshold and saturation regime is:

$$I_{aboveTh} = \beta_{sat}(V_{GS} - V_{Th})^{2+\gamma} \tag{5.1}$$

Computing the transconductance and the output resistance of the OTFT is important to evaluate the DC gain of an amplifier. They were shown graphically in the last figures of chapter 3 and 4. The equation of the transconductance g_m, is:

$$g_{m-aboveTh} = \frac{\partial I_{aboveTh}}{\partial V_{GS}} = (2+\gamma)\beta_{sat}(V_{GS} - V_{Th})^{1+\gamma} \tag{5.2}$$

Or in terms of the drain source current:

$$g_{m-aboveTh} = (2+\gamma)\beta_{sat}^{\frac{1}{2+\gamma}}(I_{aboveTh})^{\frac{1+\gamma}{2+\gamma}} \tag{5.3}$$

The inverse of the output resistance is the output conductance $g_{ds} = \frac{1}{r_0}$. The equation of the output conductance is:

$$g_{ds} = \frac{\partial I_{aboveTh}}{\partial V_{DS}} = \beta_{sat}(V_{GS} - V_{Th})^{2+\gamma} * \lambda \tag{5.4}$$

From the transfer and output experimental curves of chapter 3 and 4 which presented OTFTs of particular sizes, it is possible also to calculate by a linear estimation, the transconductance and output conductance with the sizes for our designs:

$$g_{m-M1} = g_m * (W_{M1}/W) \tag{5.5}$$

$$r_{0-M1} = r_0 * (W/W_{M1}) \tag{5.6}$$

The simplest amplifier is a transistor used as driver or transconductor device and a resistor load. The equation of the small signal DC gain of this single stage amplifier shown in Fig. 5.1 is:

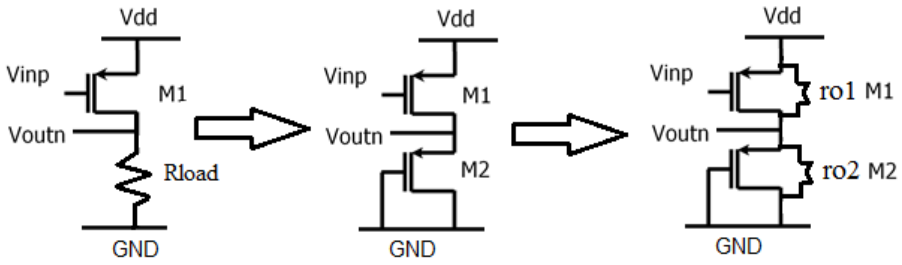


Fig. 5.1: Schematics of a single Input-Output amplifier with a resistance load, a diode connected transistor load and the output small signal resistances.

$$A_v = -g_m R_{load} \tag{5.7}$$

Unfortunately in the implemented organic technologies in this thesis work, resistors are not available. Similar to the Si MOSFET and using the small signal model presented in chapter 2, connecting the gate and the drain of an OTFT makes a transistor behaves as a nonlinear resistor equals to $R_{M2} = \frac{1}{g_m}||r_0$. The total load resistance is thus the parallel combination of the inverse of the transconductance of M2 with output resistance of both transistors:

$$R_{load} = \frac{1}{g_{m2}}||r_{01}||r_{02} \tag{5.8}$$

And thus the DC gain equation becomes:

$$A_v = -g_{m1}(\frac{1}{g_{m2}}||r_{01}||r_{02}) \tag{5.9}$$

If the values of the output resistances are higher compared to the values of the inverse of the transconductance, the simplified DC gain equation of the diode connected load amplifier is:

$$A_v \simeq -\frac{g_{m1}}{g_{m2}} = -\frac{(2+\gamma)\beta_{sat1}^{\frac{1}{2+\gamma}}(I_{aboveTh1})^{\frac{1+\gamma}{2+\gamma}}}{(2+\gamma)\beta_{sat2}^{\frac{1}{2+\gamma}}(I_{aboveTh2})^{\frac{1+\gamma}{2+\gamma}}} \tag{5.10}$$

Taking into account that the currents are the same in the branch, $I_{aboveTh1}$=$I_{aboveTh2}$ and that both devices have the same channel length and process parameters:

$$A_v = -(\frac{\beta_{sat1}}{(\beta_{sat2}})^{\frac{1}{2+\gamma}} = -(\frac{W_1}{W_2})^{\frac{1}{2+\gamma}} \tag{5.11}$$

5.2.1 Sizing OTFTs

The sizes W and L, of each OTFT could be calculated precisely with a Matlab code inverting the above threshold equation in the adapted model. However, one could apply rules of thumbs to size the OTFTs when doing hand calculations.

In fact, it was presented on Chapter 3, Fig. 9, and in Chapter 4, Fig. 11, that the OTFTs drive approximately a drain source current at higher V_{GS} of 10 μA, with a width of 1 mm and 10 mm, respectively. Oversizing OTFTs to obtain currents of several μA is an important factor, notably in the Joanneum Research Technology as mobilities are at least 10 times lower compared to the Orgatech Technology.

Knowing that the ratio of the widths of the driver transistor M1 compared to the load transistor M2 determines the DC gain, a simple way to obtain a higher gain would be to size one with respect to the other. By the contrary, it is important to take in consideration the input capacitance, the output DC offset voltage generated by over sizing M1 with respect to M2 and the reduction in the output voltage swing. Accordingly, sizing M1 20 times larger with respect to M2 and evaluating equation 5.11, will give a moderate DC gain of 10 dB.

In both technologies in this work, a minimum width for OTFTs is chosen as 500 μm. For the Orgatech load transistor M2, it is expected a current close to 5 μA. In the case of the Joanneum Research load transistor M2, a current close to 0,5 μA. Therefore, the input OTFT M1 is sized to 10 mm.

The width of the transistors M5 and M6 in the differential amplifier seen in the next section, have been chosen to 2000 μm to supply the above mentioned bias current of 5 and 0,5 μA and to saturate better these OTFTs. The better the saturation of M5, the closer the rail-to-rail operation in the output voltage is.

5.3 6 OTFT Fully Differential Voltage Amplifier

In order to design analog front-end for sensor read-out circuits, differential circuits looking to reduce common mode signals were designed. In Fig. 5.2 a fully differential voltage amplifier following our former single stage design, is presented with a mirror current source. The equation

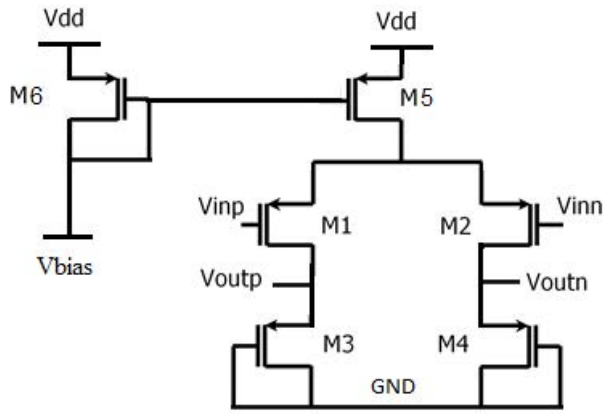


Fig. 5.2: Schematic of a fully differential voltage amplifier with diode load transistor and a current source

5.11 still holds for the DC open loop single ended gain due to the fact that the drain of M5 is considered an AC virtual ground. The node Vbias could be either biased with a current source or with a DC voltage source.

5.3.1 Simulation Results for the Orgatech Technology

For the Orgatech Technology with longer channel length OTFTs (L=30 μm) and high values of gate bias ($V_{SG} > 30V$), the output resistances are much higher (by 1 to 2 orders of magnitude) than the inverse of the transconductance of M2 (as seen on Fig.13 on Chapter 3), and as a first approach, they could be neglected.

The voltage supply was increased to 70 V in order to put in saturation all the transistors. The common mode input voltage is VDD/2=35 V. The simulations did not show a large output offset voltage, however these values need to be measured due to the mismatch present in the real circuits. In the mismatch model presented in chapter 3, a 46 % current variation is expected. A simple estimation of the maximum output offset voltage variation would be 35 +/- 16 V on one branch with respect to the other one. This value seems large, however the important point here is to gain experience in the quantification of every one of these circuit performance variations and to improve in the future the circuit design.

The exact value of the bias current is on the contrary, gate source and drain source voltage dependent. The simulation gives us a value of 3,4μA. The phase margin is 100 degrees which makes

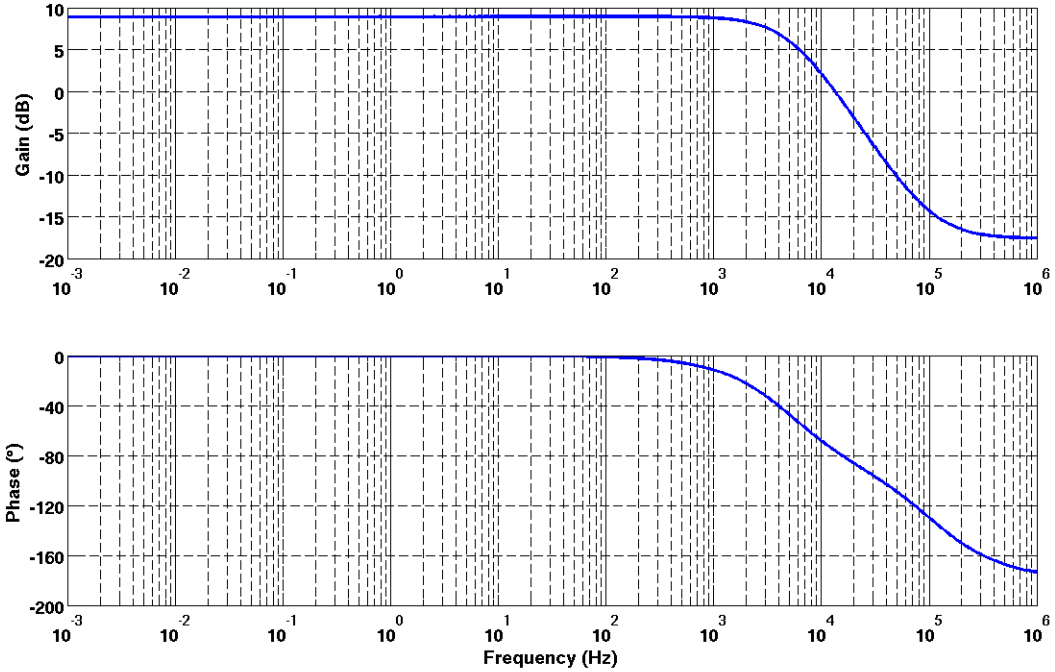


Fig. 5.3: Gain and phase bandwidth curves of the amplifier with the Orgatech Technology

it stable, but slightly slower for large signal processing. The specifications and performances of our differential amplifier are summarized in Table 5.1.

Concerning the dynamic behavior of the Orgatech Technology, the parasitic capacitance corresponding to the overlap of the gate with the source and drain are layout dependent in the case of shadow masks. A minimum overlap of several μm is normal. On chapter 3 this parasitic capacitances were 6,25 pF, in this case the simulations were done with a 5 pF capacitance in the source and in the drain. The result of the Spice AC simulation of the differential voltage amplifier is presented in Fig. 5.3. The DC open loop single ended gain is exactly as was expressed by hand calculations. Using a rough approximation, a $g_{m-aboveTh}$=0,7 μA/V obtained from Fig. 13 a) at a V_{GS} of -50 V, V_{DS} of - 50 V and using Eq. 4.3 presented in chapter 4, the calculated frequency at 0 dB is 11,1 KHz. A similar value is shown also in Fig. 5.3 with 13,4 KHz.

Table 5.1: Fully differential voltage amplifier specifications presented in Fig.5.2

Technology	**X-LPICM Orgatech**
Number of OTFTs	6
Length (μm)	30
Input OTFT W M1,2 (μm)	10 000
Load OTFT W M3,4 (μm)	500
Current Source W M5(μm)	2 000
Supply Voltage: VDD (V)	70
Vin, CM (V)	35
Vbias (V)	40
Ibias (μA)	3,4
Vout, CM (V)	34,8
Power consumption (μW)	238,0
DC Gain (dB)	9
Bandwidth (Hz)	5000
Frequency at 0 dB (Hz)	13400
Phase margin (degrees)	100

5.3.2 Simulation Results for the Joanneum Research Technology

The simulations results for the differential amplifier using the Joanneum Research Technology are presented in Fig.5.4. As a first approach, the output resistances are not taken into account and the DC open loop single ended gain is similar to the one for the Orgatech Technology, 9,6 dB. The voltage supply was 10 V as currents tends to be lower in this technology, with a total bias current of 1,3 μA. The common mode input voltage is VDD/2=5 V. The simulations showed an output offset voltage of 0,7 V however due to the lack of a mismatch model in this technology the real offset could be larger.

In the next chapter the implementation of the inverter in plastic electronics gives a slightly higher DC gain, therefore more precise hand calculations will be shown there. The amplifier

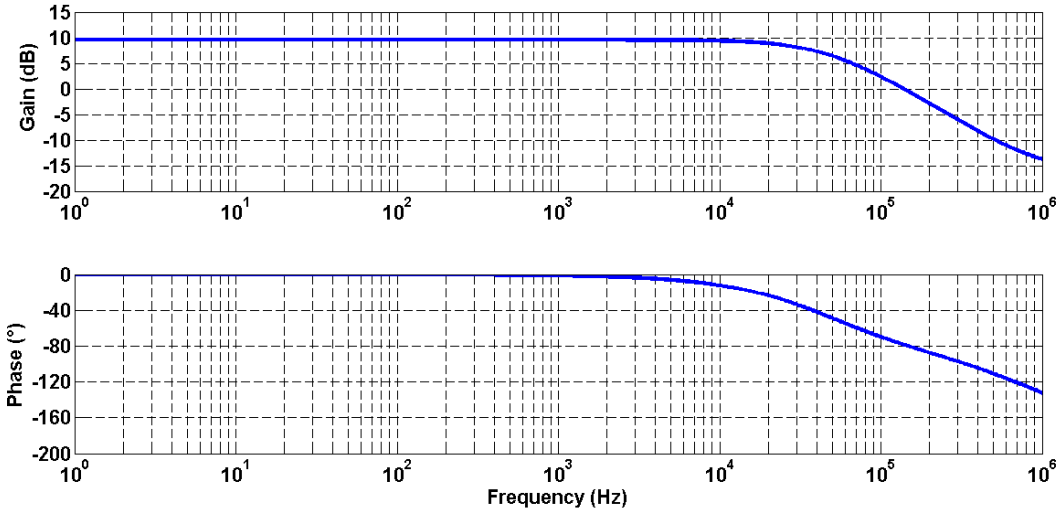


Fig. 5.4: Gain and phase bandwidth curves of the amplifier with the Joanneum Research Technology

was simulated with a mobility, μ of 0,01cm^2/Vs which makes it quite fast in simulations with a bandwidth of 47 KHz and a frequency at 0 dB of 139 KHz. On chapter 4, the computation of the frequency at 0 dB was 159 kHz. As explained there, the reason for these higher values are: the smaller channel lenghts of 2μm and the smaller overlap capacitances in the Eq. 4.5. These frequencies above 100 KHz although higher for an organic transistor are normal in this technology. In fact as explained in a former contribution from the Joanneum Research group, higher frequencies at 0 dB of 400 KHz have already been measured with a similar type of single OTFTs having a channel length of 4,8 μm and 0,01cm^2/Vs of mobility, [71].

5.3.3 Comparison of Performances of Both Technologies

A comparison of both differential amplifiers simulated with each technology is presented in Table 5.3 along with the state of the art already presented in chapter 2. Although the DC gains are lower, the goal with these designs is to obtain the largest Gain-Bandwidth compared to the state of the art. Both technologies presents good results concerning low power consumption and low number of OTFTs compared to the other ones. Again, it is important to remark the fact that with this topology, moderate to low DC gains are unavoidable, however a large bandwidth till KHz is targeted. This is the principal differences compared to the other designs in the state

Table 5.2: Fully differential voltage amplifier specifications presented in Fig.5.2

Technology	**Joanneum Research**
Number of OTFTs	6
Length (μm)	2
Input OTFT W M1,2 (μm)	10 000
Load OTFT W M3,4 (μm)	500
Current Source W M5(μm)	2 000
Supply Voltage: VDD (V)	10
Vin, CM (V)	5
Vbias (V)	5
Ibias (μA)	1,3
Vout, CM (V)	5,7
Power consumption (μW)	13
DC Gain (dB)	9,6
Bandwith (KHz)	47
Frequency at 0 dB (KHz)	139
Phase margin (degrees)	100

of the art, where the bandwidths are shorter. The Orgatech technology which is fabricated by shadow masks is more performant regarding the easier fabrication process and thus the reduced parameter variation with respect to the photolithographic ones. The amplifier with the Joanneum Research Technology has in principle the largest GBW reported to date (as will be tested in the next chapter, but with a lower mobility compared to the simulation). Guerin [18] is using the lowest number of OTFTs (4), however the supply voltage is 40 V and some parameters have not been tested such as its stability. Finally, none of them is giving a clear result on the mismatch in the currents of the different branches in the amplifiers. The only one stating a clear variation in its gain and bandwidth is Gay [16], although he used a mathematical model to express the physics

Table 5.3: State of the Art of amplifiers fabricated with flexible organic transistor technologies. PL stands for photolithography and SM for shadow mask. 1S for 1-stage, 2S for 2-stage, 3S for 3 -Stage. And L. for load. The (*) means that these are simulation results.

References	**This work*, Orgatech**	**This work*, JR**	**Maiellaro [14]**	**Marien [15]**	**Nausieda [17]**	**Guerin [18]**	**Gay [16]**
Fabrication Techno	30 μm SM	2 μm PL	20 μm Print	5 μm PL	5 μm PL	20 μm Print	5 μm PL
Transistor Type	P-OTFT	P-OTFT	C-OTFT	P-OTFT	P-OTFT	C-OTFT	P-OTFT
Amplifier Topology	1S Diode L.	1S Diode L.	1S Folded	3S	2S	Diff. Pair	Cascode
Supply Voltage(V)	70	10	50	15	5	40	40
Current Consump.(μA)	3,4	1,3	13	21	0,55x10^{-4}	1	n.a
Power consump.(μW)	238	13	650	315	2,75x10^{-4}	40	n.a
Open loop DC Gain(dB)	9	9,6	40	23	36	27/22	8
GBW/PM (Hz)/()	13400/100	139000/100	1500/58	500/70	7,5/n.a.	n.a.	1400/n.a.
Number of OTFTs	6	6	6	27	12	4	8

of the transistor. In this work, a more formal approach to the variation of performances and yield with a more physical model was presented in chapter 3 and in section 5.6.

5.4 9 OTFT Source Coupled Latch Comparator

A source coupled latch (SCL) comparator is shown in Fig. 5.5 a). This schematic is a modification from the one introduced by Marien et al. [19]. It is composed of a pre-amplifier or track phase with the diode connected load differential amplifier and a hold phase consisting of a cross-coupled pair of OTFTs which have the same widths of the input transistors in the pre-amplifier. The glitches present in the comparator of Marien are due to the switch connecting and disconnecting both complementary outputs. This topology improves that fact by placing the switches M7 and M8 controlling the bias currents during each phase. In order to increase the gain, another source coupled latch comparator could be connected in cascade, but with inverted clock phases, in Fig. 5.5 b). However the connection of both SCL comparator blocks depends on the offset voltages in the inputs/outputs of each one. For simplicty if the offsets are too high, one SCL compartor is

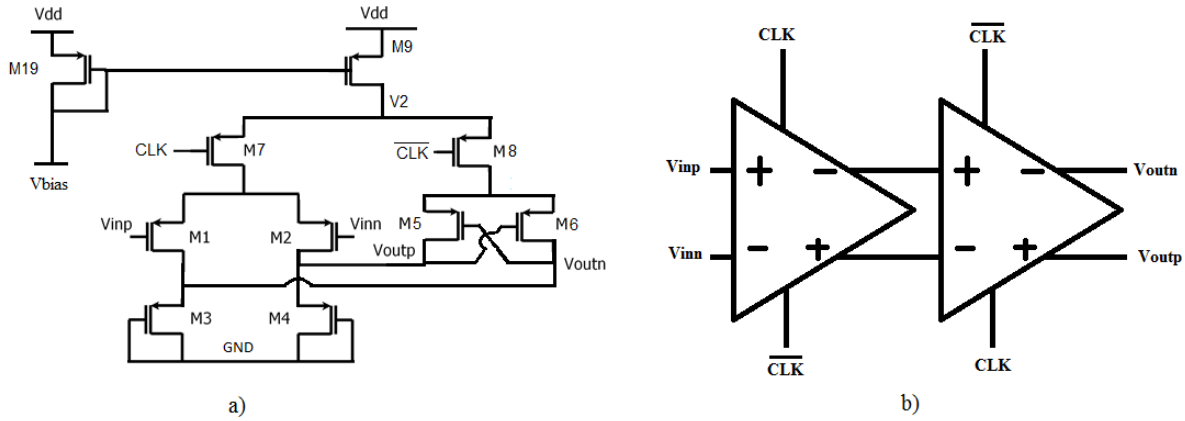


Fig. 5.5: a) Schematics of a source coupled latch(SCL) comparator. b) 2-stage SCL comparator with inverted clocks.

enough. The transistors in the mirror current source and the switches M7 and M8 were chosen again with a width of 2000 μm.

5.4.1 Simulation Results for the Orgatech Technology

In Fig. 5.6 the results of the transient Spice simulations with the Orgatech Technology are presented where the clock switches at 1 KHz. The input positive signal oscillates at a lower frequency of 100 Hz and around the common mode voltage of 30 V. The total bias current of the 2-stage source coupled latch is 7μA. The rise and fall times from the simulations were 12 and 14 ms respectively, although a 46 % of mismatch in the currents in one branch with respect to the other, could make the rise and fall time varies to 12 +/- 5,5 and 14 +/- 6,4 ms, respectively. Due to the larger parasitic capacitance, the longer channel length and the low mobility, the comparator is slow and by consequence, it is intended to work in low frequency analog front-end circuits. A summary of the specifications and performances of the fully differential comparator is in Table5.4.

5.4.2 Simulation Results for the Joanneum Research Technology

The results for the SCL comparator with the Joanneum Research Technology are shown in Fig. 5.7. The input frequencies is 1 KHz and the simulated delay times are under 1 ms, therefore the comparator is also intended to work at low-medium frequencies ADCs. Notably, the variations

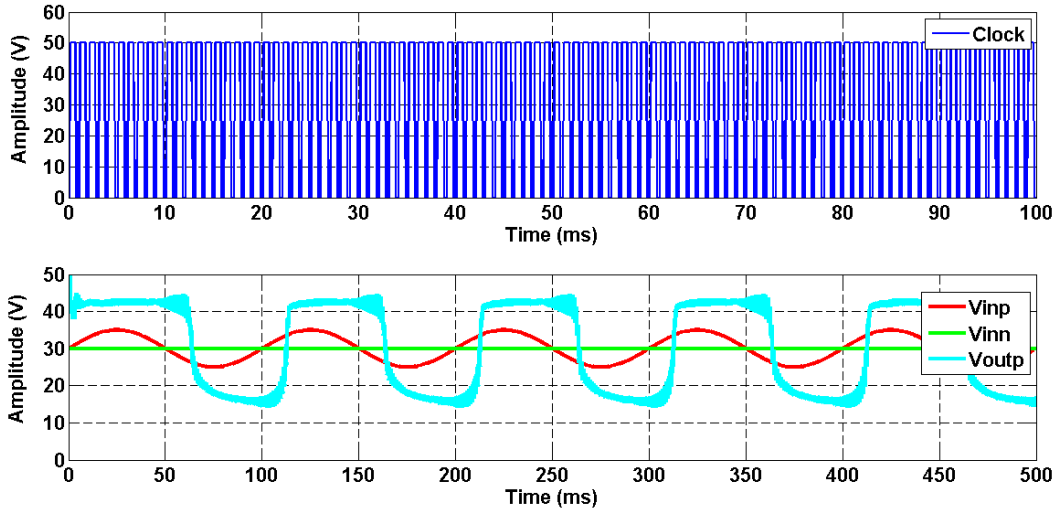


Fig. 5.6: Simulations results for the comparator with the conditions on Table 5.4

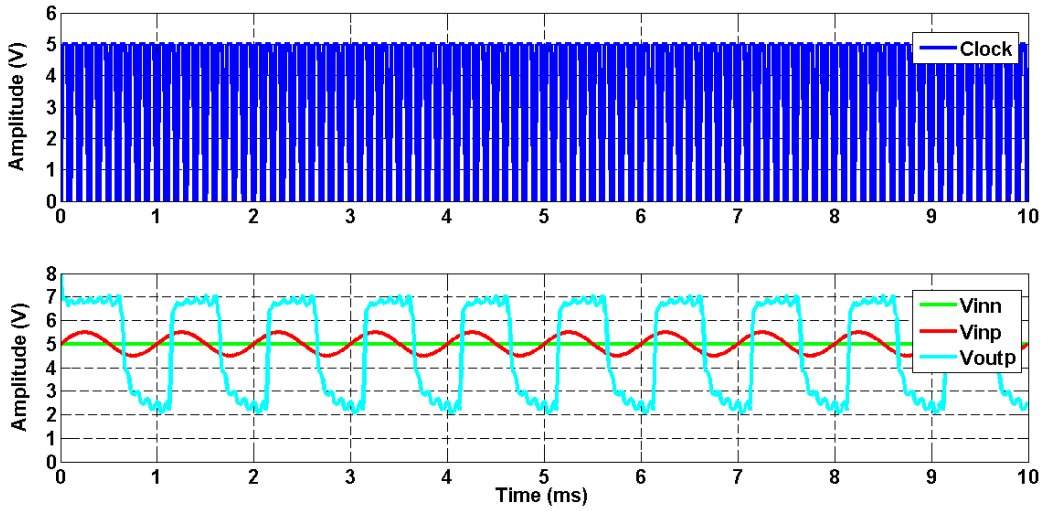


Fig. 5.7: Simulations results for the comparator with the conditions on Table 5.5

in mobility in this technology from 0,001 to 0,01 cm^2/Vs make it difficult to predict the AC behavior. Again in this case, the most important point that the simulations are not predicting are the variations in the offset voltages due to the mismatches in both branches as it will be seen in the implementation in plastic electronics in the next chapter. Nevertheless, it is functional with a low power consumption and it is as fast as the other ones shown in the state of the art in the next subsection.

Table 5.4: Fully differential comparator specifications presented in Fig.5.5

Technology	**X-LPICM Orgatech**
Number of OTFTs	19
Length (μm)	30
Input OTFT W M1,2,10,11 (μm)	10 000
Cross Coupled OTFT W M5,6,14,15 (μm)	10 000
Load OTFT W M3,4,12,13 (μm)	500
Current Source W M9,18,19 (μm)	2 000
Clock OTFTs W M7,8,16,17 (μm)	2 000
Supply Voltage: VDD (V)	70
Vin, CM (V)	30
Vin (V)	5
Vbias (V)	40
Ibias (μA)	7
Power consumption (μW)	490
Rise time (ms)	12
Fall time (ms)	14

5.4.3 Comparison of Performances of Both Technologies

In Table 5.6, the state of the art of the comparators is shown. The comparators designed in this chapter are intended to work at clock frequencies of 1 KHz making them the fastest ones. Again, the simplicity of the fabrication by shadow masks make the Orgatech technology more reliable and a good approach to overcome the parameter variations. On the contrary, the Joanneum Research comparator is intended to work at input and clock frenquencies higher than 1 KHz, which make it more useful for its integration with medium frequencies ADCs.

Table 5.5: Fully differential comparator specifications presented in Fig.5.5

Technology	**Joanneum Research**
Number of OTFTs	19
Length (μm)	2
Input OTFT W M1,2,10,11 (μm)	10 000
Cross Coupled OTFT W M5,6,14,15 (μm)	10 000
Load OTFT W M3,4,12,13 (μm)	500
Current Source W M9,18,19 (μm)	2 000
Clock OTFTs W M7,8,16,17 (μm)	2 000
Supply Voltage: VDD (V)	10
Vin, CM (V)	5
Vin (V)	0,5
Vbias (V)	5
Ibias (μA)	1,2
Power consumption (μW)	12
Rise time (ms)	0,2
Fall time (ms)	0,5

5.5 25 OTFT, 1-Bit 1st Order Sigma Delta Modulator

A simple analog to digital converter (ADC) is developed in this section using the aforementioned 2 analog blocks, as a front-end for flexible sensors at low frequencies. Considering the complexity, several ideas are explored in the literature such as: sigma delta modulators presented in [21], successive approximation ADCs [23], and VCO based ADCs [24].

In this work, the objective is to simplify the designs reducing the number of OTFTs compared to the reports in the literature and to relate performance to process variations in order to obtain functional systems. Accordingly, a 1 bit-sigma delta modulator is the simplest possible design composed of 3 basic blocks, shown in Fig.5.8:

-A loop filter (such as an active RC analog filter with an amplifier).

Table 5.6: Comparison of the tested comparator with the State of the Art. SM stands for shadow masks fabracation and PL for photolithography. L stands for transistor load. Sw.Cap stands for switched capacitors. The (*) means that these are simulation results.

References	**This Work*, Orgatech**	**This Work*, JR**	**Maiellaro [14]**	**Marien [19]**	**Abdinia [20]**
Fabrication Techno	30 μm SM	2 μm PL	20 μm Print	5 μm PL	20 μm PL
Transistor Type	P-OTFT	P-OTFT	C-OTFT	P-OTFT	C-OTFT
Comparator Topology	Diode L.	Diode L.	Folded Casc.	AC-Coupled L.	Sw.Cap.Inverter
Number of OTFTs	19	19	12	11	8
Supply Voltage(V)	70	10	50	20	40
Current Consump.(μA)	7	1,2	13	9	n.a.
Power Consump.(μW)	490	12	650	180	n.a.
Min. Input Signal (V)	5	1	1	0,2	0,4
Input Frequency (KHz)	0,1-0,01	1	0,050	0,040	DC
Clock Frequency (KHz)	1,0	10	0,120	1,0	0,070

-An ADC as a quantifier block (or a clocked comparator in the case of a 1-bit).
-A DAC in the feedback loop.

The sigma delta modulation consists in the conversion of an analog signal to a frequency modulated signal (s(n) in Fig.5.8), which could be processed by a digital circuit. The modulator filters the high frequency components of the input signal to avoid aliasing and shapes (or pushes to high frequencies) the quantization noise introduced by a clocked quantizer block with sampling frequency fs.

The sigma delta modulator could be designed in continuous or discrete time according to the loop filter. In this work, an active RC filter is implemented for a continuous time sigma delta modulator. The filter is a low-pass first order filter. The modulator is 1-bit because one comparator is used as an ADC or quantizer block which adds quantization noise. The comparator could be modeled also as a non return to zero (NRZ) track & holder block, because it holds the signal over 1 period of the clock. The digital to analog converter could be implemented using a simple resistor. As a first approach, the digital decimator would be done by a conventional Si CMOS digital signal

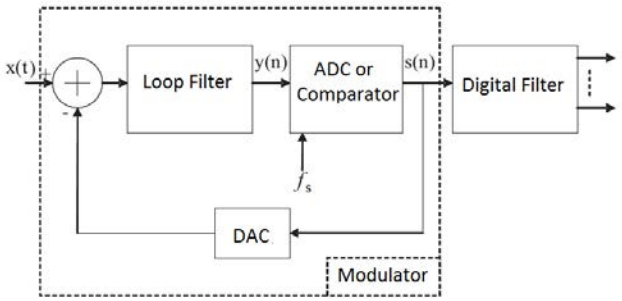


Fig. 5.8: Block model of a Sigma Delta Analog to Digital Converter

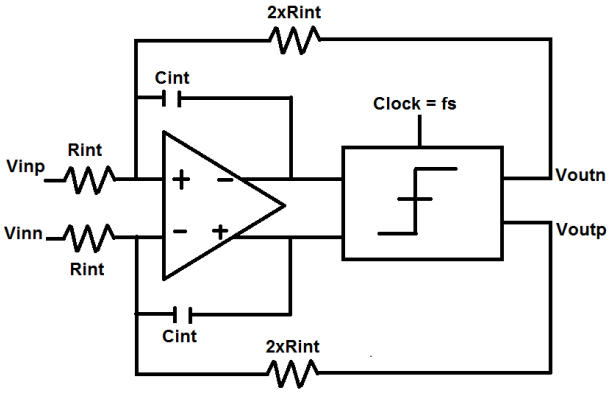


Fig. 5.9: Schematic of the Sigma Delta Modulator

processor, therfore this work focuses on the analog part of the read-out circuitry. A theoretical description of ADCs and sigma delta modulators is presented in Appendix A.

In Fig. 5.9 the sigma delta modulator is depicted, with the functional blocks designed in the last sections. The resistors and capacitors are expected to be implemented by discrete external devices.

5.5.1 System Level Modeling

For proper operation of a sigma delta modulator, the DC gain of the op-amp is usually taken to be equal to the OSR [76]. In Fig.5.10, the loop filter H(s) is designed as an active RC integrator with the presented fully differential voltage amplifier. In order to overcome the low DC gains of the amplifiers, a theoretical analysis concerning the system level modeling of the modulator is introduced in this thesis work thanks to the internship thesis of Cabral-Moraes [77], where the

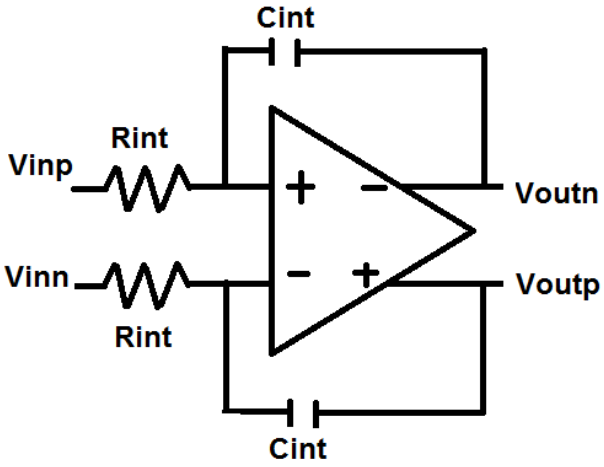


Fig. 5.10: Schematic of the RC active integrator

RC integration factor is increased till the noise transfer function is reduced to its lowest possible values, and it is shown below.

The transfer function of this amplifier with a 1 dominant pole is:

$$G_{amp}(s) = \frac{A_o}{1 + \frac{s}{p_1}} \tag{5.12}$$

Thus, the transfer function of the loop filter in the s-domain becomes:

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{1}{C_{oeff2}s^2 + C_{oeff1}s + C_{oeff0}} \tag{5.13}$$

Where the coefficients are:

$$C_{oeff2} = \frac{RC}{p_1 * A_o} \tag{5.14}$$

$$C_{oeff1} = -RC + \frac{RC}{A_o} + \frac{1}{p_1 * A_o} \tag{5.15}$$

$$C_{oeff0} = \frac{1}{A_o} \tag{5.16}$$

The DAC is represented in the circuit in this chapter with a zero-order hold transfer function:

$$H_{DAC}(s) = \frac{1 - e^{-T_s * s}}{s} \tag{5.17}$$

The loop filter transfer function in the Z-domain becomes:

$$H(z) = Z\{H(s)H_{DAC}(s)\} = (1 - z^{-1})Z\{\mathcal{L}^{-1}\frac{H(s)}{s}\} \tag{5.18}$$

Putting Eq. 5.13 in Eq. 5.18 one obtain, [77]:

$$H(z) = \frac{(z-1)}{C_{oeff2}}(\frac{k_2}{z-1} + \frac{k_1}{z - e^{r_1 T_s}} + \frac{k_0}{z - e^{r_2 T_s}}) \tag{5.19}$$

With:

$$k_2 = \frac{1}{r_1 r_2}; k_1 = \frac{1}{r_1(r_1 - r_2)}; k_0 = \frac{1}{r_2(r_2 - r_1)} \tag{5.20}$$

And:

$$r_{1,2} = \frac{-C_{oeff1} \pm \sqrt{C_{oeff1}^2 - 4C_{oeff2}C_{oeff0}}}{2C_{oeff2}} \tag{5.21}$$

As mentioned in the appendix A, the idea is to maximize Eq. 5.19 across the frequency range f/f_s (the phase in the z domain unity circle) to minimize the noise transfer function NTF(z), Eq. 5.22:

$$NTF(z) = \frac{1}{1 + H(z)} \tag{5.22}$$

It is possible, as well, to choose the RC time constant of the analog filter in order to have practical values for the design. The ratio of the sampling period with the RC time constant of the filter: $A_{int} = \frac{1}{f_s RC}$ will be used to evaluate Eq. 5.19 for the parameters of the blocks simulated in Spice. A DC gain for the amplifier A_0 of 9 dB is chosen with a pole p_1 of 5 kHz and a sampling frequency f_s equals to 1024 Hz which is a typical clock frequency for the comparator. In Fig.5.11 the results of the evaluation of the equation 5.19 in Matlab ©are presented, where for lower values of the parameter A_{int} (or larger values of the time constant RC), one could minimize, at least in theory, between -60 dB to -80 dB the NTF.

In the following transistor level simulations, the parameter A_{int} has been chosen to 0,025 in order to have practical values for the resistor R_{int} and the capacitor C_{int} which are 98 MΩ and 400 pF, respectively. The sampling frequency f_s, was chosen to 1024 Hz

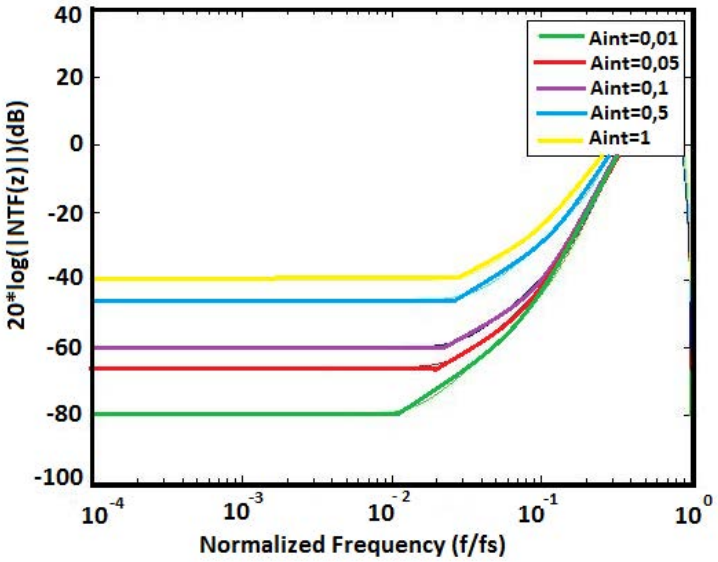


Fig. 5.11: Graphic of the Noise Transfer Function (NTF) vs. the normalized frequency for different Aint=1/f_sRC values, a DC gain of 9 dB and a f_s of 1024 Hz.

5.5.2 Transistor Level Simulation Results for the Orgatech Technology

In Fig. 5.12, the PSD of the sigma delta modulator is presented implementing the analog blocks designed in this chapter with the adapted a-Si TFT model. For an OSR of 32 and a bandwidth of 16 Hz, an SNR of 30 dB is obtained. There is a considerable higher frequency noise introduced with the slow organic comparator, which affects the typical noise shaping effect of sigma delta modulators PSDs curves. The ENOB calculated is 4,72 bits and the Figure of Merit equals 86,3 nJ/bits.

5.5.3 Transistor Level Simulation Results for the Joanneum Research Technology

In Fig. 5.13, the PSD of the sigma delta modulator with the blocks of the Joanneum Research Technology, is presented. As a matter of comparison of both technologies, a sampling frequency f_s of 1024 Hz was chosen, with an OSR of 32 and a bandwidth of 16 Hz, an SNR of 28 dB is obtained with an ENOB calculated of 4,36 bits and a Figure of Merit which equals 105 nJ/bits.

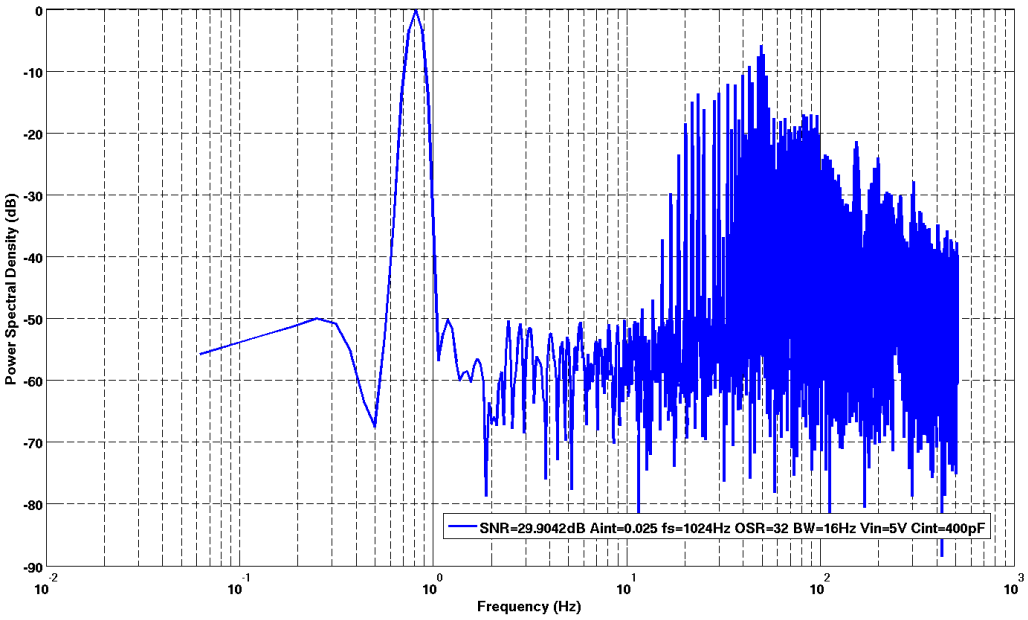


Fig. 5.12: Power Spectral Density versus Frequency with organic transistor-level simulations of the proposed Sigma Delta Modulator with the Orgatech Technology.

5.5.4 Comparison of Performances of Both Technologies

Table 5.7 summarizes all of the design parameters and performances for the 25 OTFT 1 Bit Sigma Delta Modulator. A comparison with other ADCs is presented where the designed ones in this chapter show good performances compared to the State of the Art with a higher sampling frequency, larger bandwidth, more ENOBs and better SNR with respect to the other 2 full OTFT ADCs. The Orgatech sigma delta modulator as it is the only one fabricated by shadow masks with just 4 layers and top contact transistors, is intended to be the most robust, and the one with the least variations in performances. The Joanneum Research sigma delta modulator is focused to be the one with the lowest power consumption for an ADC developped with just OTFTs and the one with (in practice) the highest sampling frequency and largest bandwidth. Both modulators show the highest ENOBs compared to the other full OTFTs ADCs. In the case of Raitieri [24], he is showing a higher number of bits, but a part of its ADC was not implemented in OTFTs. Xiong [23] had a similar case, where the SAR logic was implemented off chip.

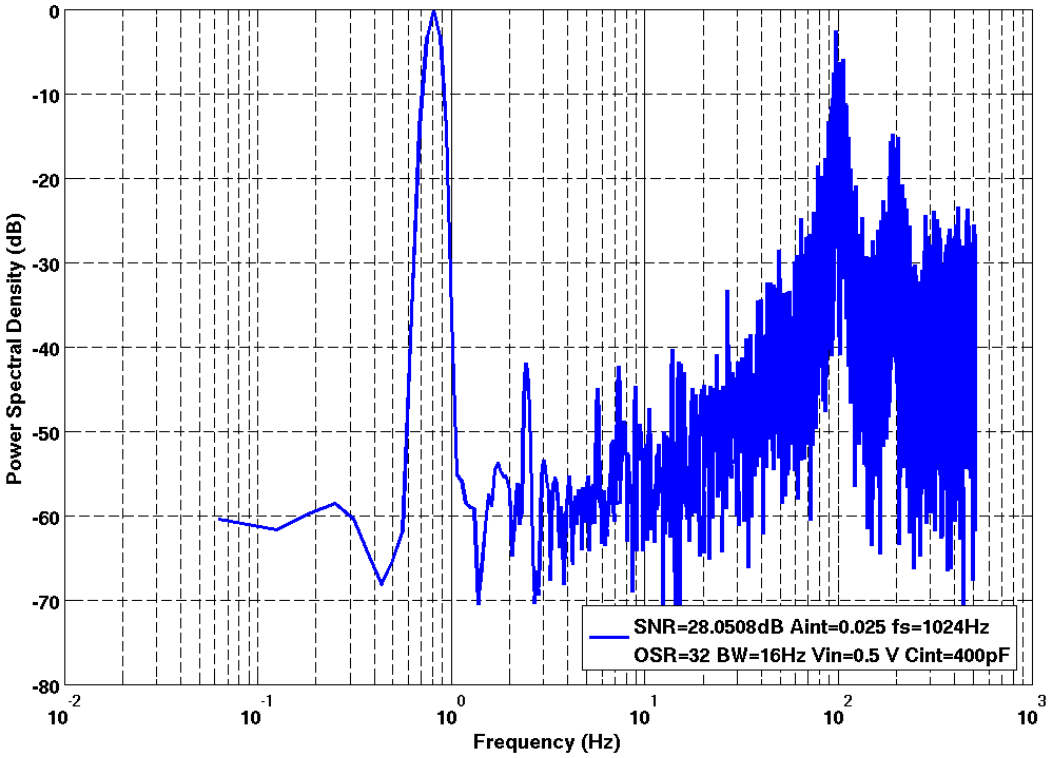


Fig. 5.13: Power Spectral Density versus Frequency with organic transistor-level simulations of the proposed Sigma Delta Modulator with the Joanneum Research Technology

5.6 A Discussion on Yield with Monte Carlo Simulations

In this section, Monte Carlo simulations with normal distributions were done with the Orgatech/Ecole Polytechnique Technology to determine the values of the variations of process parameters β_{sat} and threshold voltage V_{Th}, where the degradation of circuit performances is considerable. Accordingly, the β_{sat} variations are due moreover to mobility variations. The V_{Th} ones are dependent moreover in the dielectric thickness accross the different OTFTs in the circuit. It is important to remark the fact that the results of the Monte Carlo simulations in this section do not indicate that the circuits are not going to work, but that the yield of the well-working ones will be reduced. Fig. 5.14 presents the normal distribution for a mean μ = 0 and standard deviation σ=1. The standard deviation of the threshold voltage (presented in chapter 3) is $\sigma_{V_{Th}}$ = -3,3 V. This graphic means, for example that considering the yield: 68 % of OTFTs have a threshold voltage

Table 5.7: Different Organic ADC specifications in the literature. The * means that this work is based for the moment on simulations results. The ** means that the ADCs are not fully manufactured with OTFTs. JR stands for Joanneum Research and MPI for the Max Planck Institute.

Published	**This work***	**This work***	**Marien [21]**	**Abdinia [22]**	**Raitieri [24]**	**Xiong [23]**
Technology	Orgatech	JR	IMEC	TUE-CEA	TUE	Stanford-MPI
ADC Type	SD	SD	SD	Counter	VCO	SAR
OTFTs number	25	25	129	106	17(**)	53(**)
Supply Voltage (V)	70	10	15	40	20	3
Power consumption (μW)	728	69	1500	540	48	3,6
Vin, CM (V)	30	5	9	0	-	1,5
Vin, pp (V)	10	1	1	0,4	0-20	1,55
OSR	32	32	16	-	-	-
Bandwidth (Hz)	16	16	15,6	2	33,5	14,3
fin (Hz)	0,80	0,80	10	2	4-38	-
fs (Hz)	1024	1024	500	70	66	100
SNDR (dB)	30	28	24,5	19,6	48	-
ENOB(or bits)	4,72	4,36	3,77	2,96	7,7	6
FoM (nJ/bits)	863	105	3524	17349	3,45	-

varying from -11 +/- 3,3 V, while the V_{Th} of 38 % of them varies between -11 +/- 1,65 V. Finally, the V_{Th} of 20 % of them varies between -11 +/- 0,83 V.

5.6.1 Monte Carlo Simulations for the Differential Amplifier

An example on the reduction of yield is presented with the differential amplifier. Fig.5.15, presents the impact of V_{Th} variatons. In order to have around 50 % of yield, a value of +/- 2 V was chosen. These variations are uncorrelated among the different OTFTs in the circuit due to the differences in the dielectric thickness on each one. The best and worst case are shown, where notably the DC gain of the amplifier varies from 5 to 11 dB. The phase margin stays stable in any case between 50 and 90 degrees. The value of 2 V represents a normalized sigma (2/3,3) of 0,61 in Fig. 5.14 which

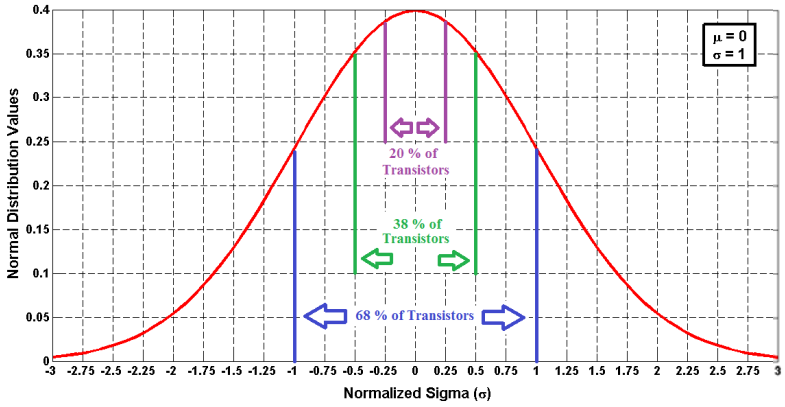


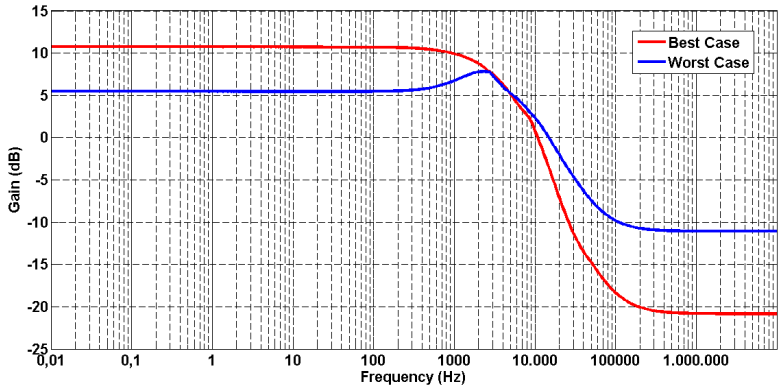
Fig. 5.14: Graphic of the normal distribution with mean μ = 0 and standard deviation σ=1

means 46 % of yield or in other terms, almost half of the fabricated amplifiers will have a gain between 5 and 11 dB.

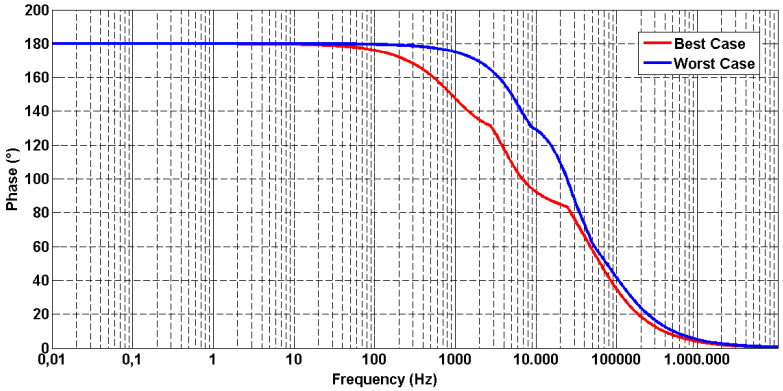
On Fig.5.16, the impact of the mobility is pictured with a 41% variation (or 1 sigma, calculated on chapter 3) and a correlated variation due to the fact that all the OTFTs are fabricated with the same process of deposition of the semiconductor. The impact of these variations are on the bandwidth of the amplifier. The best and worst case show that 68 % of the fabricated ones will have a bandwidth between 5 and 3 kHz respectively. Summarizing, the variations are divided in 2 categories: threshold voltage (or dielectric thickness/capacitance) impacts the DC gain and mobility (morphology of the semiconductor during deposition) impacts the bandwidth of the amplifier.

5.7 Conclusion

In this chapter, an organized design procedure for analog circuits is shown, using the adapted a-Si TFT model developed in chapter 2 and 3 and the parameters extracted for both technologies of Orgatech (chapter 3) and Joanneum Research (chapter 4). A differential amplifier with both technologies was designed with a hand calculated gain and transition frequency. The comparator was designed in order to be functional at low frequencies. The system level design of a 1-bit 1st order Sigma Delta Modulator showed that it is possible theoretically to overcome the low DC gain of the amplifier, reducing the noise power by increasing the RC time constant, and present



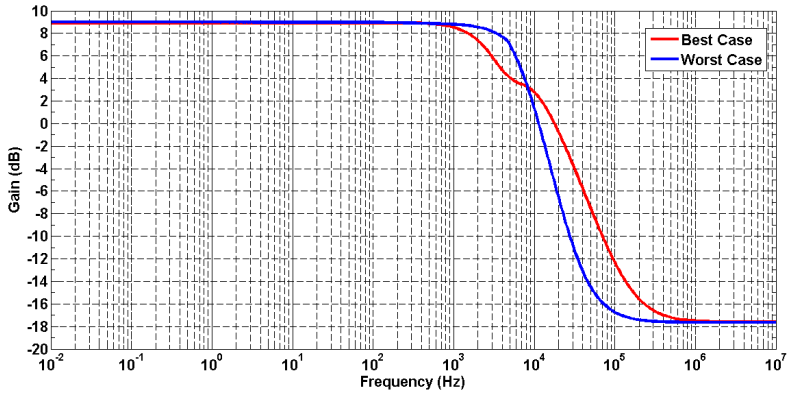
(a)



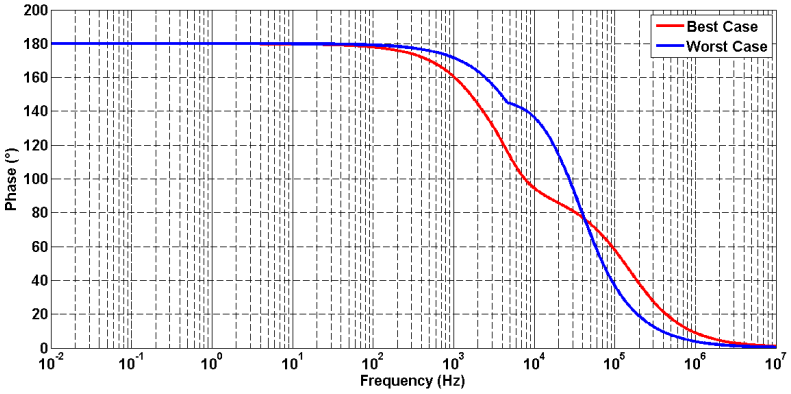
(b)

Fig. 5.15: Monte Carlo Simulations with a variation of 2V on the V_{Th} with an uncorrelated variation in each OTFT in the circuit. a) Best and worst case of the gain bandwidth curve. b) Best and worst case of the phase bandwidth curve.

moderate signal to noise ratios for the modulator. It was simulated at a transistor level with both technologies, using just 25 OTFTs and its performance notably, the SNR and the ENOB are better than the other ADCs done fully with OTFTS presented in the state of the art.



(a)



(b)

Fig. 5.16: Monte Carlo Simulations with a variation of 41% on the mobility with a correlated variation in all of the OTFT in the circuit. a) Best and worst case of the gain bandwith curve. b) Best and worst case of the phase bandwidth curve.

6

Implementation of Analog & Digital Circuits on Plastic on a "Low-Power, KHz Frequency" Technology

6.1 Introduction

In this chapter as a first approach the test of a Transistor Evaluation Module (TEM) fabricated by photolithography and self alignment procedures (as described in the chapter 4) is shown, using the technology developed at Joanneum Research. It includes functional circuit blocks with few OTFTs to analyze the performance of the OTFT technology. The final sample is fabricated on a 10 cm x 10 cm, thin (175 μm) flexible transparent poly-carbonate (PC) foil and is pictured in Fig. 6.1. The TEM mask is divided in 7 x 7 dies of 9 x 9 mm^2 areas. In principle this structure could be used as an active backplane to read out a suitable matrix of sensors. In fact, with a dedicated Design Rule Manual (DRM), it is determined, how many functional circuits with computational capability could be placed into these dies. The dies can be cut one by one by a scissor with 1 mm separation in order to allow for separate testing. Moreover, the TEM mask permits to test further developments of the OTFT technology based on higher mobility unipolar organic semiconductors. The TEM mask is divided in 4 basic test structures:

-Test structures for a layer-by-layer evaluation of the process.

-OTFTs and capacitors for individual tests.

-Digital circuits with inverters, ring oscillators and logic gates.

-Analog circuits with differential amplifiers and comparators.

It has to be emphasized that the main interest is dedicated to measure functional signals with the lowest possible quantity of OTFTs in order to scale up step by step avoiding poor functioning of sub-blocks and in order to obtain results as close as possible to simulations, notably in the case

of analog circuits. The section 6.2 explains the measurement principles of those thin film circuits. In section 6.3, the measurement results of different digital blocks are collected: inverters, and logic gates. Finally in section 6.4, the measurement results of the analog blocks such as fast differential amplifiers and comparators are described. These tests, die-by-die and circuit-by-circuit provides a basic knowledge for analyzing and deciding which blocks could be integrated functionally in a future design of a full system for applications such as a sensor matrix read-out. The basic interesting functions that are:

-DC and AC gains.

-Propagation delay of signals.

-Bandwidth and transition frequency.

-Comparators for analog signal treatment.

-Logic functions.

It is important to note that the semiconductor layer is not protected from air by a passivation layer. Unfortunately in all the measurements that are not carried out in inert atmosphere, some degradation with respect to the simulated performance, and some mismatch among devices in the same circuit and between different dies is observed. This is probably due to the degradation of the semiconductor in air (oxygen and humidity). On the other hand, thereby valuable information on changes of performance under normal pressure, temperature and air conditions is gained.

6.2 Testing Plastic Circuits

The dies in the TEM mask have different amounts of pads to test the signals. In fact they are divided in 2 groups. Firstly, the digital blocks, where the limited number of pads permits the measurement by needle probes (as in the case of the measurement of a single OTFT or capacitor), see Fig. 6.2(a). Secondly, the analog blocks or even connections of different blocks or dies (e.g.: a system), where the larger number of pads makes it practically impossible to test by needle probes. Therefore a method of connecting or bonding wires (copper in this case) with the pads at the lowest possible temperature was developed. As can be seen in Fig. 6.2(b) single dies are cut from the substrate and placed in a conventional IC platform, a plastic leaded chip carrier (PLCC)

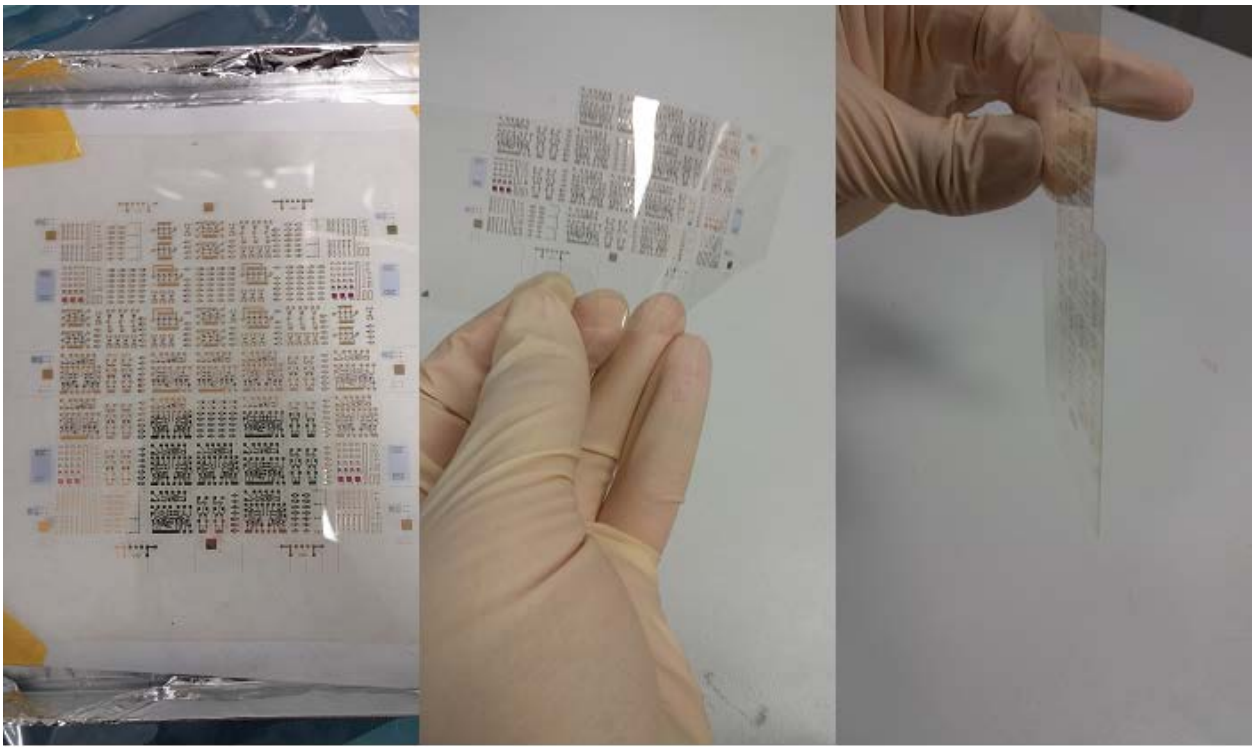
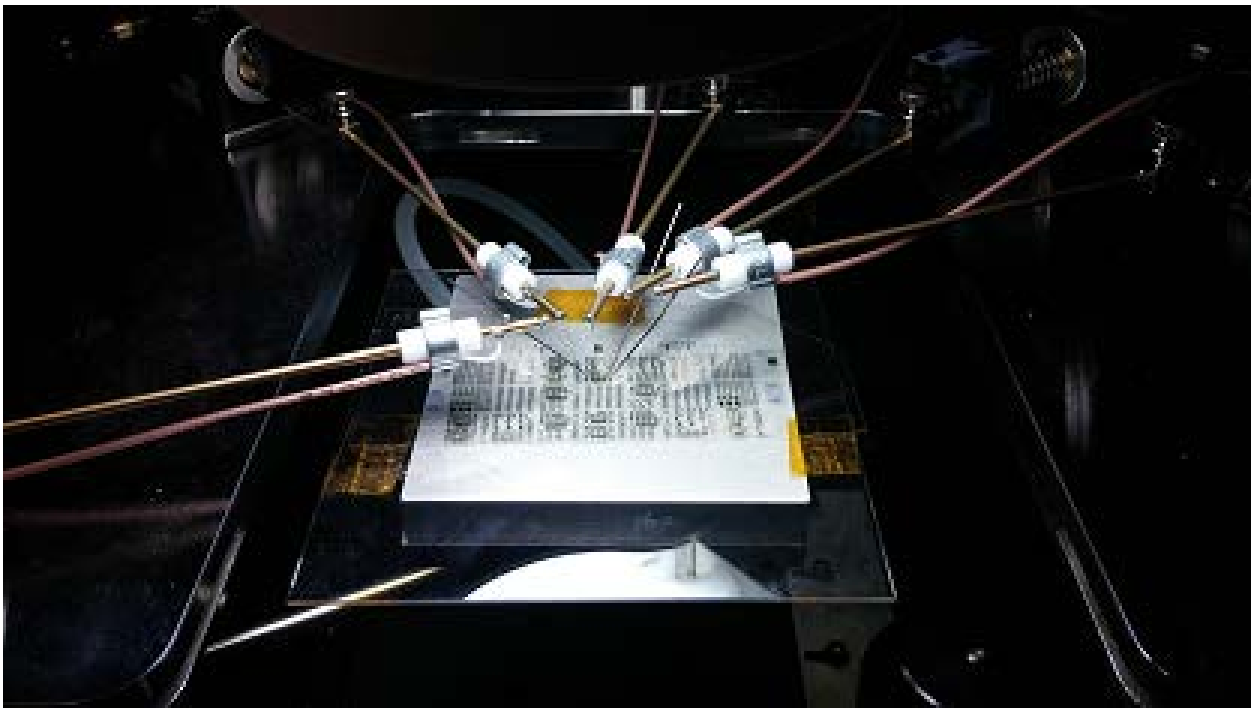
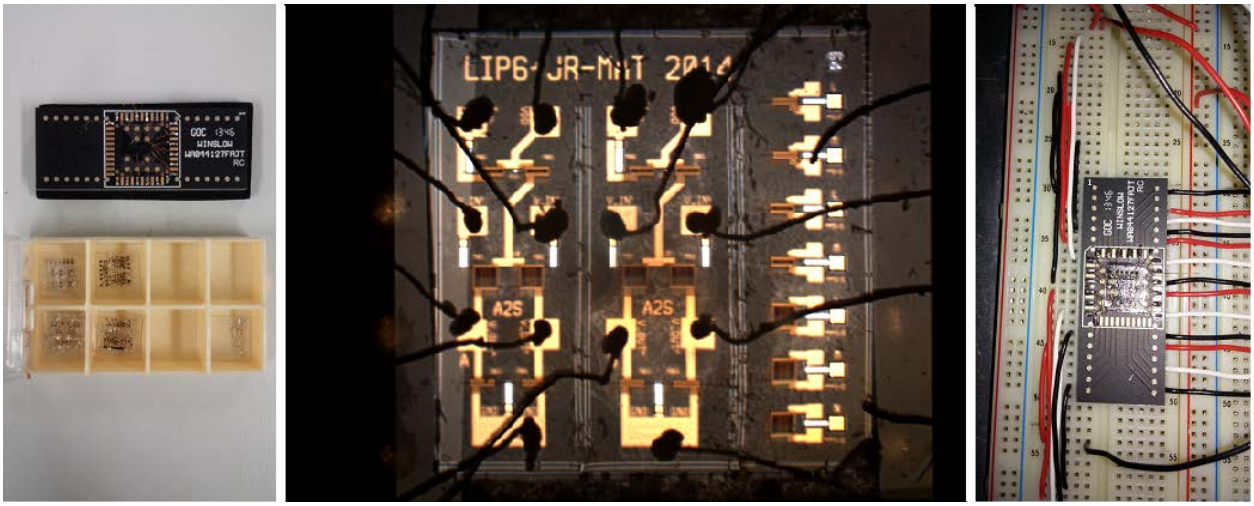


Fig. 6.1: Photos of the test sample fabricated to evaluate the performance of the different analog and digital basic circuits. Note how thin and flexible the sample is.

to Dual in Line (DIL) adapter, ideal to connect different dies and to test them on breadboards. In the center of the Fig. 6.2(b) one can see a die with two differential amplifiers (explained in section 6.4.1) where each 92 μm copper wire is soldered at one end to a gold pad of the IC platform with a conventional tin soldering process at 250 C and at the other end placed and pasted with a conductive glue (the EPO TEK H20E-PFC) over the 0,6 x 0,6 mm^2 gold pads of the plastic die. This process is critical, because heat is required in order to harden the conductive glue to the die pad. In our case, a plastic die has a substrate glass transition temperature of about 150 C and a melting temperature of 225 C. The semiconductor pentacene was evaporated on a substrate kept at ambient temperature (25 C). The robustness of the SAM-layer is also critical since it is a very thin organic layer of around 1 nm thickness which is well known to desorb and oxidize at higher temperatures. Therefore a maximum temperature of 80 C is used. The copper wires were thus placed carefully over the die gold pads with a small amount of glue that was baked at 80 C for 3 hours. As is seen in Fig. 6.2(b), all the wires were connected at these small areas of the pads with



(a)



(b)

Fig. 6.2: a) Photo of the measurement setup with needle probes for circuits with few pads. b) Photos of the low temperature bonding process to test circuits with many pads.

enough precision. The IC platform with the connected plastic die could be thus connected to a breadboard or printed circuit board (PCB) and is ready for an electrical test.

6.3 Characterization of Moderate Gain-Fast Inverters and Logic Gates

For the digital circuits, it was the goal to measure overall two performance indicators of this OTFT technology: the DC gains and the maximum delay of the signals of the inverters and logic gates. In addition, it was important to obtain functional signals at the output of digital circuit blocks such as a logic gates. The inverter already presented in chapter 5, was tested in this technology, and is shown in Fig. 6.3. As explained in the introduction, each die is cut one by one and tested. For guidance there are visible frames around each die forming a total gap between active areas of 1 mm to cut them by scissors. Using the equations already developped in chapter 5, good estimations of all the parameters and of an approximated DC gain for the inverter, are presented in this chapter.

In this chapter, to calculate with precision the maximum DC gain that is possible to obtain in the measurements, the output resistances are taken into account. As seen in Fig. 12 in chapter 4, the output resistance of the transistors r_0 are of the same order of magnitude as the inverse of the transconductance. Therefore applying a supply voltage V_{DD} of 7 V, an input voltage of 3,5 V, and considering that there are no DC offsets, would result in an output of 3,5 V, too. The VGS and VDS of M1 and M2 are thus -3,5 V. As seen in the figure 11 of chapter 4, the transconductance and output resistance were calculated for an OTFT of W=14 mm and L=2 μm. For these bias values approximately g_m= 4 μA/V and r_0=5MΩ results.

Taking into consideration the linear estimations of the transconductance and output conductance, presented in chapter 5 5.5 and 5.6, one obtain for the sizes of M1 in the inverter: g_{M1}=2,86 μA/V and r_{01}=7 MΩ and for M2: g_{M2}=0,14 μA/V and r_{02}=140 MΩ. Calculating the final value of the DC gain in equation 5.9, one obtains 10 units or 20 dB.

In order to measure the DC gain and the change in the output voltage for different supply voltages, an input voltage sweep was applied. The trip point (or the transition point from ON to OFF with the highest gain) has a considerable offset of about 1,5 V; it is near 4 V instead of being at 2,5 V. The fact that the trip point is shifted towards higher asymmetry of the inverter characteristics is an important issue to overcome. Such a pronounced asymmetry will induce a decrease of the noise margin thus degrading the signal integrity in a larger digital integrated

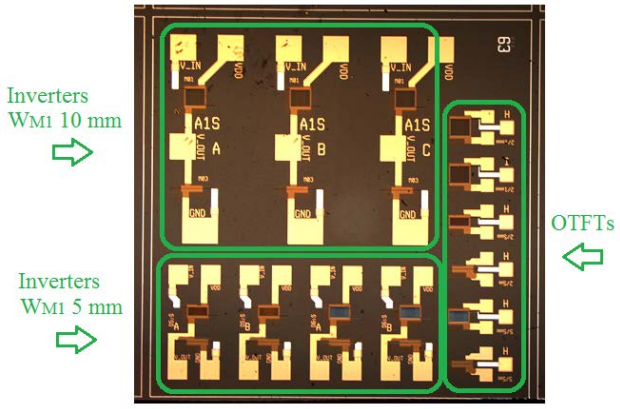
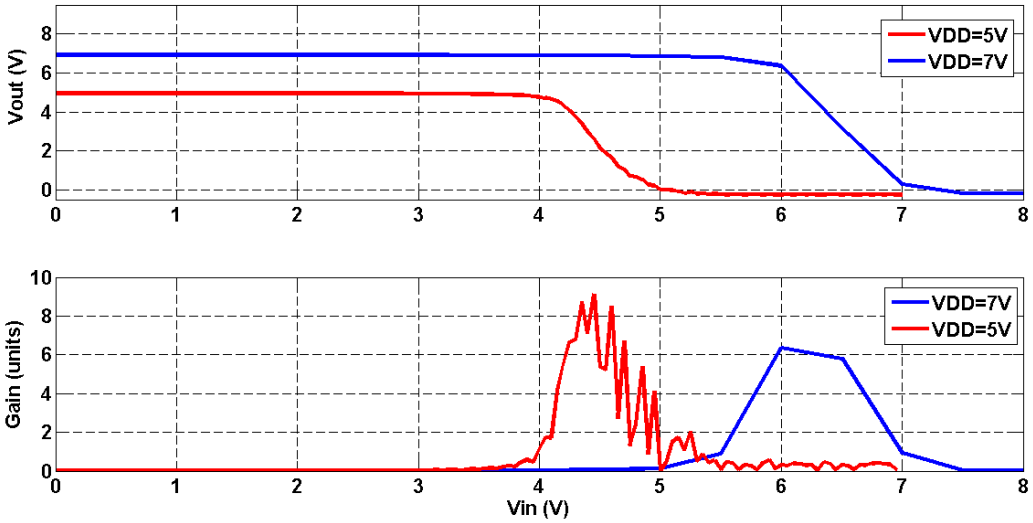


Fig. 6.3: Fabricated die of a total area of 9 x 9 mm^2 incorporating different inverters and single transistors.

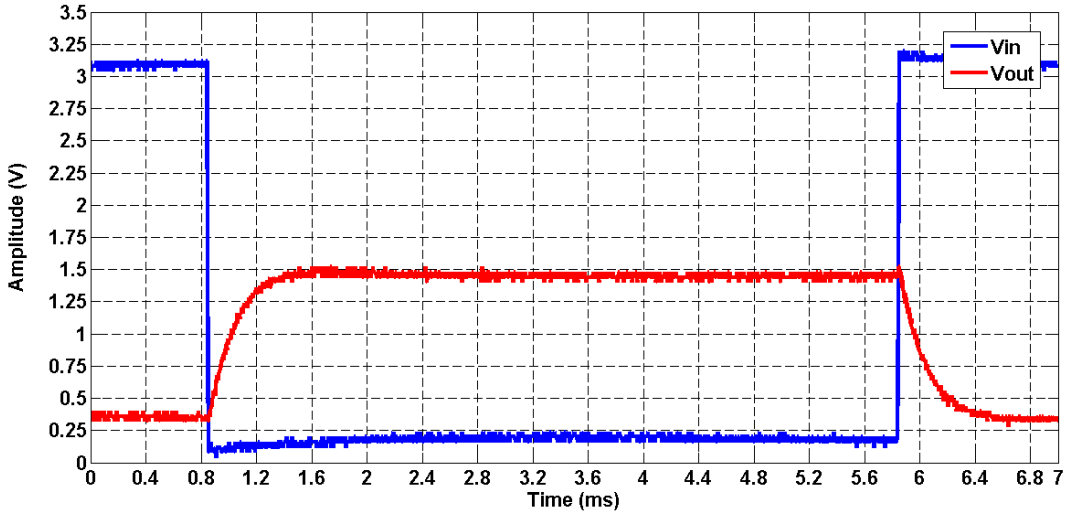
circuit. The static DC gain is finally determined from the derivative of the output voltage with respect to the input voltage and is shown in Fig. 6.4(a). A gain of 6 units (15,6 dB) and 9 units (19,1 dB) for supply voltages 5V and 7V, respectively, is obtained, which is very close to the calculated value of 10 units for VDD = 7V.

The samples with the inverters received for the test, had a nominal mobility of μ = 0,001 cm^2/Vs. Fig. 6.4(b) shows the measured delay time after a large signal input, without any buffer in the output; so a direct oscilloscope measurement delivered, 400 μs for the rise time and 500 μs for the fall time at -7,6 dB. The oscilloscopes and the coaxial cables during the measurements had about 5 pF of capacitance.

Similar to the chapter 5, a rough approximation of the delay time of the tested inverter (neglecting the capacitance during measurements) can be obtained by taking into account the transition frequency equation for short channel devices with small electrode overlaps, Eq.4.5. In fact, VDS_{sat} could be fixed to -3,5 V and L is fixed by the technology process to 2 μm, the overlap ΔL could be estimated in a worst case approximation to 250 nm. Calculating the transition frequency from the above values, one obtain f_t = 15,9 kHz or 63 μs. However, it is expected that at the moment of writing this report, in this technology, a variation of the mobility over one order of magnitude from sample to sample (e.g. from μ = 0,001 cm^2/Vs to μ = 0,01 cm^2/Vs), will change this value from tenths of kHz to hundreds of kHz. Therefore a better control of the mobility would be highly desirable which can be achieved by an improvement of the dielectric interface with re-



(a)



(b)

Fig. 6.4: a) DC transfer function of an inverter with the DC gain plotted in red. b) Transient input and output signals of the inverter.

gards to the surface energy and roughness resulting in a better morphology and by a passivation layer to protect the device from air.

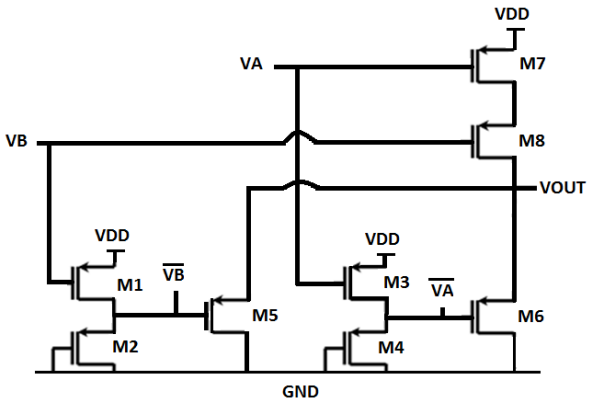
A summary of the specifications and performances of the inverter is given in Table. 6.1.

Next, a NOR Gate was tested in a configuration called a pseudo CMOS NOR gate, where the conventional NMOS transistors from a CMOS logic gate, [70] are replaced by p-type based invert-

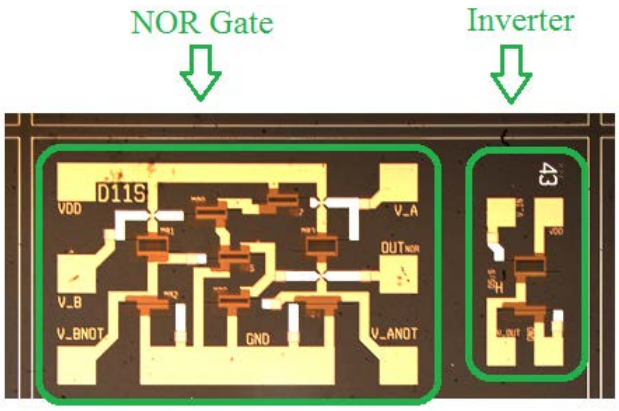
Table 6.1: Inverter specifications

Technology	**Joanneum Research**
Number of OTFTs	2
Length (μm)	2
Driver OTFT W M1 (μm)	10 000
Load OTFT W M3 (μm)	500
Supply Voltage: Vdd (V)	7
Trip point (V)	6,5
DC Gain (dB)	15,6 and 19,1
Rise time at -7,6 dB (μs)	400
Fall time at -7,6 dB (μs)	500

ers. The schematics are depicted in Fig. 6.5(a) with the corresponding implementation in plastic electronics in Fig. 6.5(b). In fact, with this NOR gate, as it is a universal logic gate, any logic function can be realized. The truth table is presented in 6.2 where logic '1' represents 7 V and a logic '0' represents 0 V, and it was successfully tested as shown in Fig. 6.6. In Fig. 6.6(a), we observe that applying a supply voltage of 7 V for VB with a logic '1' (7 V) and for an oscillating VA between logic 0 and 1, the output is at logic 0 (0 V), which is the correct behavior according to the truth table. In Fig. 6.6(b), when VB is a logic '0' (0 V), and VA is oscillating between 0 and 1 logic, Vout is oscillating as well. The output signal is attenuated at about -20 dB, since no buffer is connected to the output of the plastic sample, so the measurements were directly read out with the oscilloscope. The attenuation is due to the low input impedance (1 MΩ), which is much lower than the output impedance of the circuits (about 35 MΩ, calculated on the basis of equation 5.6 for OTFTs with W = 2000 μm. The full list of specifications are presented in Table 6.3, also including the rise and fall times of the output signal at 400 and 300 μs at the attenuated measured value, in accordance with those of the inverters. A NAND gate could also be designed with the NOR gate, one inverter at each input and one inverter at the output, plus several level-shifter stages in order to correct the offsets of the trip point of the inverter which degrades the noise margin.



(a)

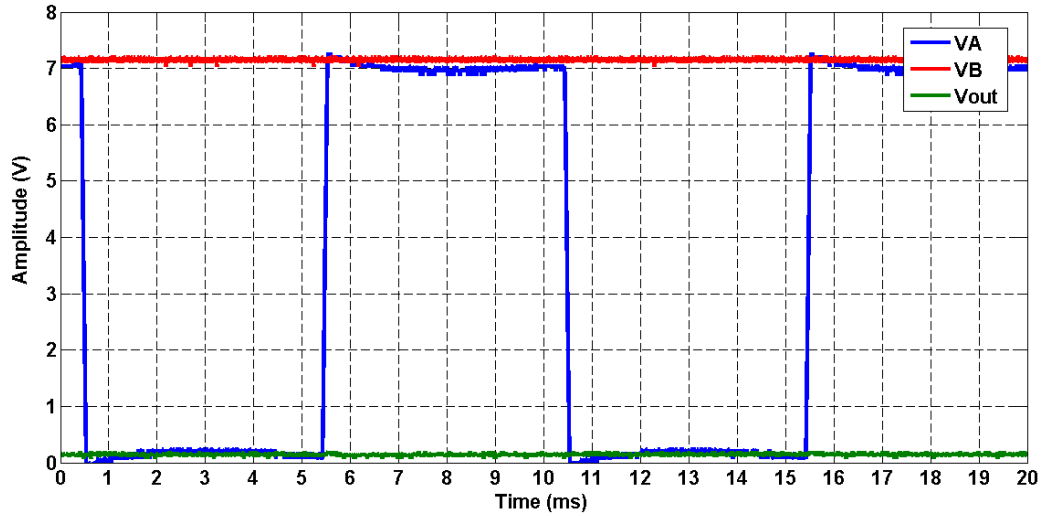


(b)

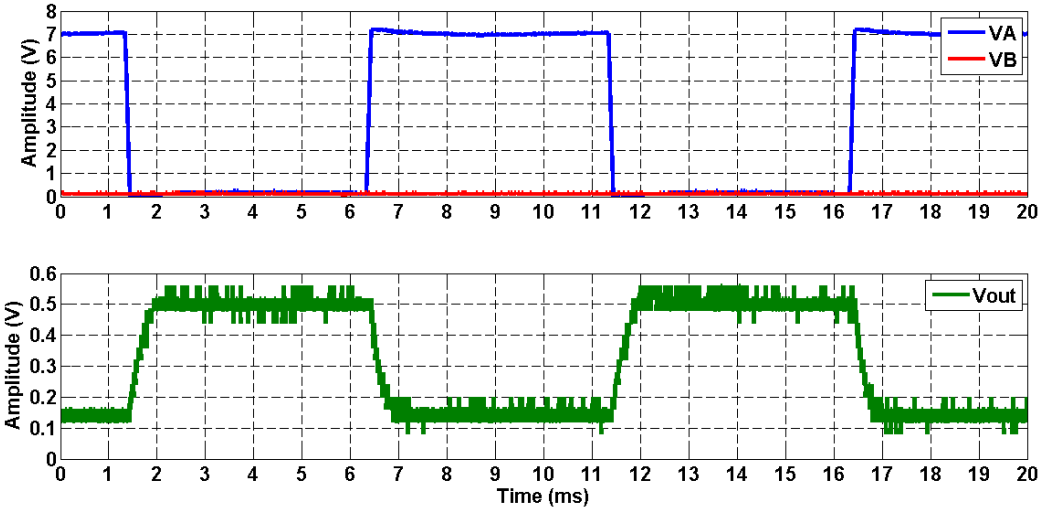
Fig. 6.5: a) Schematics of a NOR Gate. b) Implementation of the die with a total area of 4,5 x 9 mm^2 with a NOR logic gate in plastic electronics

Table 6.2: NOR Logic Gate Table

VB	VA	NOT (VA OR VB)
0	0	1
0	1	0
1	0	0
1	1	0



(a)



(b)

Fig. 6.6: a) Transient signals of a NOR Gate with VB ON. b) Transient signals of a NOR Gate with VB OFF

6.4 Characterization of Analog Circuits

The analog circuits were used to test the DC and AC gain of our designs, as well as the bandwidth, the transition frequency and the possibility of discriminating two signals or a threshold, as it is the case with the comparator. These circuits were tested with bonded wires mounted on an IC platform and connected to a breadboard with conventional operational amplifiers, TI LF353-N as

Table 6.3: NOR Gate specifications

Technology	Joanneum Research
Number of OTFTs	8
Length (μm)	2
Inv. Driver OTFT W M1,2 (μm)	5 000
Inv. Load OTFT W M3,4 (μm)	500
Other OTFT W M5,6,7,8 (μm)	500
Supply Voltage: VDD (V)	7
Rise time at -23 dB (μs)	400
Fall time at -23 dB (μs)	300

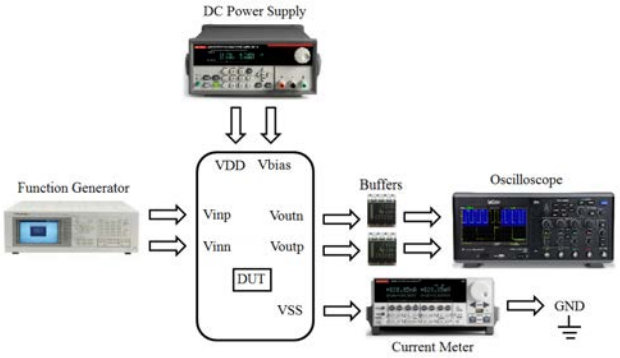


Fig. 6.7: Test Set-Up for the measurement of Analog Circuits.

buffers in each output with an input impedance of 1TΩ. The input signals were generated by a WaveTek ^{TM} 50 MHz Synthesized Arbitrary Waveform Generator Model 295, the bias currents in the circuits were measured with a Keithley 2612A System SourceMeter ^{TM} and the input and output voltage signals were measured with a 4-channel LeCroy WaveAce 2024 ^{TM} Oscilloscope. The set-up is presented in Fig. 6.7

6.4.1 Moderate Gain-Fast Differential Voltage Amplifier

A differential voltage amplifier was designed according to the theoretical analysis and the dimensions of the OTFTs presented in chapter 5. The implementation in plastic electronics is presented in Fig. 6.8.

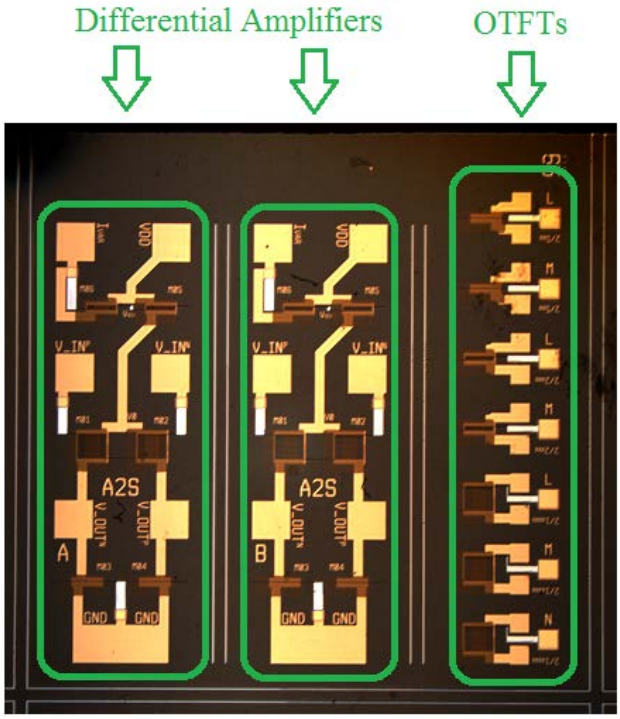


Fig. 6.8: Fabricated die of a total area of 9 x 9 mm^2 incorporating 2 differential amplifier (A2S) and single transistors with variable dimension.

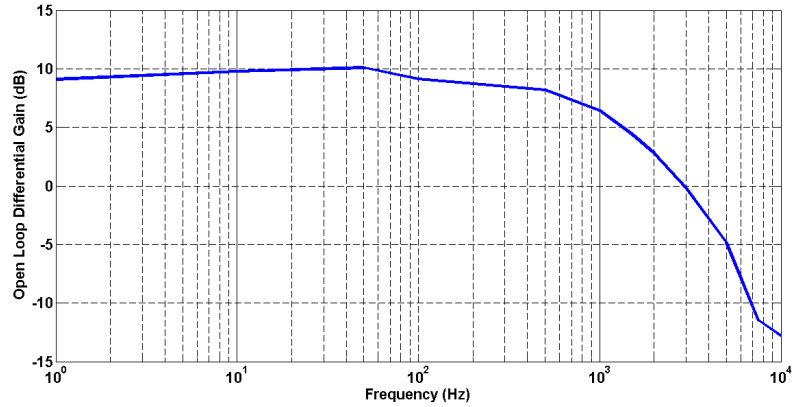
A supply voltage of 10V was applied, with an input common mode of 7 V in order to obtain the best operation point with the highest transconductance of the input transistors close to the threshold voltage. A small sinusoidal signal of 0,4 V pp was the input in M1 and the other input M2 was set at 0V pp. As a first approach, the objective was not to increase the complexity, adding a common mode feedback (CMFB) circuit. Therefore there will be a DC offset present in the outputs with respect to the input. The open loop differential gain and phase measured bode plots are traced in Fig. 6.9. A differential gain of 10 dB was measured at 50 Hz. From theory it is expected that the differential gain is doubled compared to the single ended gain presented in equation 5.9, however, two effects have to be taken into account: the electrical mismatch between the branches of the differential amplifier that has not yet been quantified and the degradation of the bias point due to a longer time of electrical stress for the OTFT (well known as the bias stress effect, see [78]). These effects were compensated by keeping the DC bias current at the same level. However, the DC gain of the inverters of 19 dB can be taken as an upper limit for the DC gain that would be

achievable by our topology. The bandwidth at -3 dB from the maximum is 800 Hz and the 0 dB frequency is almost 3 KHz. The phase margin is thus slightly higher than 90 degree, showing that the amplifier is stable. The performances and specifications are summarized in Table 6.4. The Vbias values presented with an (*) were adjusted during measurement between 0 and 4 V, in order to keep the DC bias current level at 4,9 μA, and a constant DC output level at 3,5 V. The power consumption was 49 μW. Concerning the rail-to-rail output, this topology is not the best due to the fact that one is losing at least a V_{th} in the load transistor (according to the diode load configuration) and also a VDS keeping saturated the mirror current source transistors. A possible way of improving this topology is to add an output second stage for rail to rail operation with 4 more transistors. A summary of the state of the art for different amplifiers is presented in Table 6.5, where PL stands for a photolithographic patterning technology. Although the DC gain of the OTFT technology on hand is lower compared to the other reported circuits, the amplifier in fact has the best performance reported to date, considering all key figures such as the Gain-Bandwidth (GBW), the speed, the power consumption, and the integrated die area.

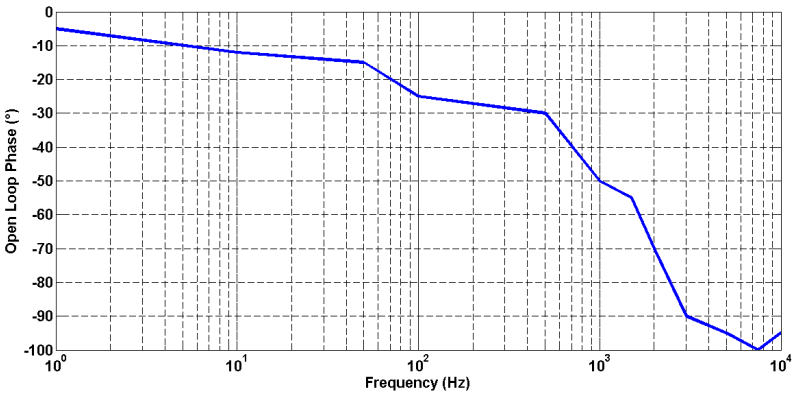
6.4.2 Fast Source Coupled Latch Comparator

A source coupled latch comparator was developed as well in this technology with the same dimensions for the width as the one in chapter 5, but a channel length for every OTFT also of 2μm. Again the idea is to compare the design kits of both technologies. The implementation of the comparator in plastic electronics is shown in Fig. 6.10. In this technology, one comparator was tested instead of 2 in cascade, due to larger variations in mobility and threshold voltage and therefore in offsets voltages in the input and outputs of each block.

The die area also includes the other identical comparator (to be connected in cascade) and a horizontal differential amplifier. This proves that about 25 OTFTs with pads and wirings (they had to be about 150 μm wide to keep the interconnect resistance below 150 Ω) can be integrated on an area of 1 cm^2 based on the self-aligned photolithography OTFT technology. In Fig. 6.11, it was successfully tested by applying a DC bias of 3,5 V as a reference to one input transistor and a triangular signal with a DC offset of 2 V and a 1 V pp AC signal to the other input transistor. There is an input referred offset voltage of 1,5 V due to the mismatch in both branches which



(a)



(b)

Fig. 6.9: a) Open loop differential gain versus frequency. b) Open loop phase versus frequency.

was difficult to predict due to the lack of a mismatch model. A future design would need to correct this mismatch with an input stage. The clocked current sources were generated with 2 complementary squared signals with an amplitude variation from 0-5 V p-p and a period of 10 μs, while the input signal frequency had a period of 100 μs. It has to be noted, that this sample had a semiconductor layer with an improved mobility of 0,01cm^2/Vs. This fact allowed for applying signals at a higher frequency. Accordingly, straight edges at each time the input signal passes the common mode voltage of 2 V were observed with squared signals in the negative output, once the threshold voltage of 2 V in the positive input was passed. The bias stress effect is present as well here, as a variation of the DC bias current during a long-time electrical stress. The Vbias of

Table 6.4: Fully differential voltage amplifier specifications

Technology	**Joanneum Research**
Number of OTFTs	6
Length (μm)	2
Driver OTFT W M1,2 (μm)	10 000
Load OTFT W M3,4 (μm)	500
Current Source W M5(μm)	2 000
Supply Voltage: VDD (V)	10
Vin pp (V)	0,4
Vin CM (V)	7
Vbias (V)	0-4 (*)
Ibias (μA)	4,9
Power consumption (μW)	49
Vout, CM (V)	3,5
Open Loop DC Gain (dB)	10
Bandwidth (Hz)	800
Frequency at 0 dB (Hz)	3000
Phase margin ()	90

the mirror current source was adjusted during measurement as well here, in order to obtain the stable value of 10 μA. This is indicated by an asterisk (*) in Table 6.6 summarizing the results.

This comparator outperforms the former ones in the state of the art as shown in Table 6.7 considering power consumption, input frequency and clock frequency. Although the comparator presented in this work shows a 1,5 offset voltage in the input which makes it less sensible compared to the other ones presented; those were either single ended or without clear results of the mismatch in the inputs/outputs. Notably the one of Marien [19] presents considerable glitches and was not implemented in the sigma delta modulator of the Ref. [29]. The ones of Abdinia and Maiellaro work at higher voltages, 40 and 50 V respectively, however the proposed comparator

Table 6.5: State of the Art of amplifiers fabricated with flexible organic transistor technologies.

References	This work, JR	Maiellaro [14]	Marien [15]	Nausieda [17]	Guerin [18]
Fabrication Techno	2 μm PL	20 μm Print	5 μm PL	5 μm PL	20 μm Print
Transistor Type	P-OTFT	C-OTFT	P-OTFT	P-OTFT	C-OTFT
Amplifier Topology	1-stage Diode load	1-stage Folded Casc.	3-stage	2-stage	Diff. Pair
Supply Voltage(V)	10	50	15	5	40
Current Consump.(μA)	4,9	13	21	0,55x10^{-4}	1
Power consump.(μW)	49	650	315	2,75x10^{-4}	40
Open loop DC Gain(dB)	10	40	23	36	27/22
GBW/PM (Hz)/()	3000/90	1500/58	500/70	7,5/n.a.	n.a.
Settling time (ms)	<1	<1	n.a	n.a	n.a
Compensation Tech.	Uncomp.	Dominant Pole	Miller Eff.	Uncomp.	Uncomp.
Area (mm^2)	24	115	n.a	n.a	n.a

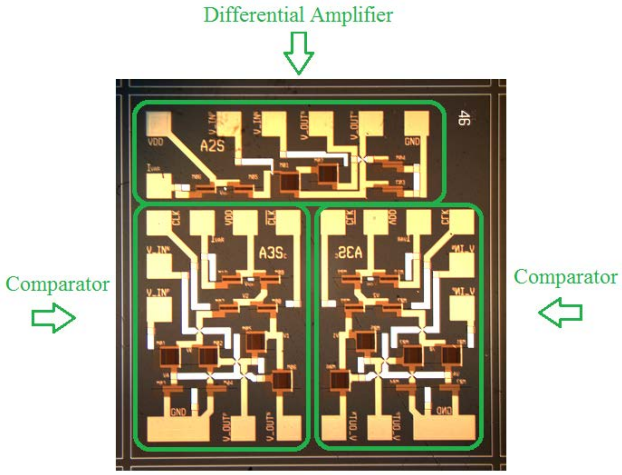


Fig. 6.10: Fabricated die of a total area of 9 x 9 mm^2 incorporating 2 source coupled latch comparators (A3S) and a differential amplifier (A2S). The comparator circuit occupies a relatively small area of 5 x 8 mm^2

in this case with a lower power and fast response technology presents a key advantage compared to them for the implementation in sensor read-out circuits.

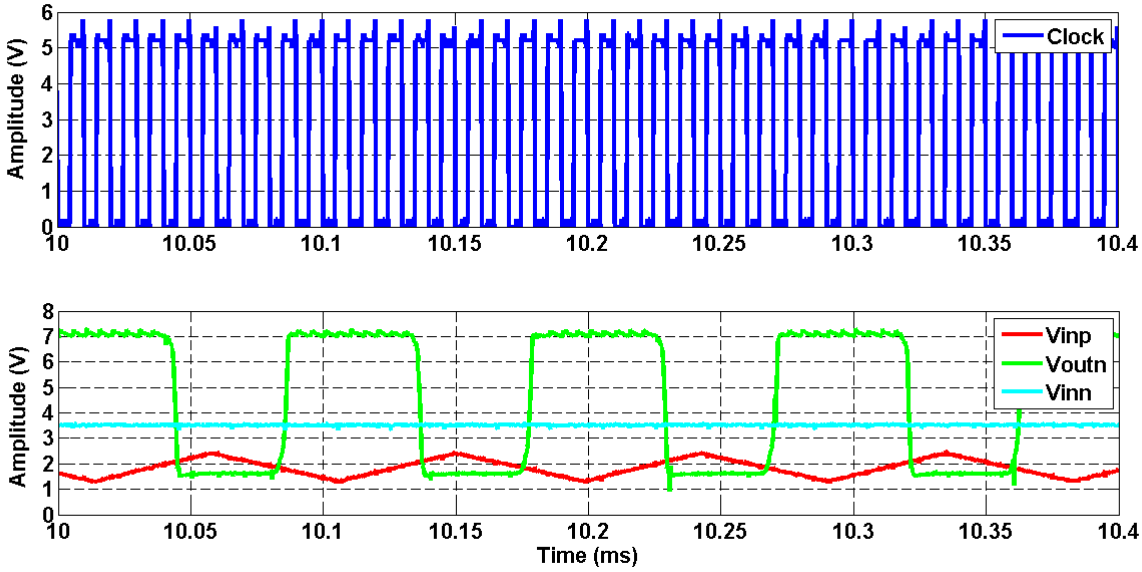


Fig. 6.11: The comparator transient signals.

Table 6.6: Fully differential comparator specifications

Technology	**Joanneum Research**
Number of OTFTs	10
Length (μm)	2
Driver OTFT W M1,2,5,6 (μm)	10 000
Load OTFT W M3,4 (μm)	500
Current Source W M9,19 (μm)	2 000
Clock OTFTs W M7,8 (μm)	2 000
Supply Voltage: Vdd (V)	10
Vin, pp (V)	1,0
Vbias (V)	0-2 (*)
Ibias (μA)	10,0
Period Input Signal (μs)	100
Power consumption (μW)	100

Table 6.7: Comparison of the tested comparator with the State of the Art

References	This Work, JR	Maiellaro [14]	Marien [19]	Abdinia [20]
Fabrication Techno	2 μm PL	20 μm Print	5 μm PL	20 μm PL
Transistor Type	P-OTFT	C-OTFT	P-OTFT	C-OTFT
Comparator Topology	Diode Load	Folded Casc.	AC-Coupled Load	Single Inverter
Number of OTFTs	10	12	11	8
Supply Voltage(V)	10	50	20	40
Current Consump.(uA)	10	13	9	n.a.
Power Consump.(uW)	100	650	180	n.a.
Min. Input Signal (V)	1	1	0,2	0,4
Input Frequency (KHz)	10	0,050	0,040	DC
Clock Frequency (KHz)	100	0,120	1,0	0,070
Area (mm^2)	5x8	232	2x3	n.a

6.5 Discussion of the Results

As explained in the last chapters, a 1 bit sigma delta modulator could be composed of an analog amplifier as a filter and a comparator. In this chapter both of them were tested successfully. On the contrary, three points are important to remark after their measurement, which avoids their integration for the moment: first the DC voltages in the inputs and outputs are not the same, (this point demands the improvement of the design by a dedicated common mode feedback circuit for each circuit block); second, the mismatch between the branches of the 2 differential blocks, as seen in Fig. 6.11 with a 1,5 V of mismatch in the inputs of the comparator; third, the difference between the real operating points and the simulated ones. This last point is unavoidable with this adapted model. A closer approach between design and measurements is needed in order to quantify all the issues already presented in this chapter, that the model cannot predict.

The approach in this chapter was to design and test several OTFT circuits in order to obtain a functional signal treatment for achieving the least possible mismatches between OTFTs within a die and between dies. The rise and fall times close to 0 dB in these digital circuits were well

below 1 ms and the bandwidth of the differential amplifier was 800 Hz with a Gain Bandwidth figure of merit of 3000 Hz, which is the best value reported so far. In addition, a fully functional source-coupled latch comparator was successfully demonstrated. The analog circuits power consumption is between 49 and 100 μW for the differential amplifier and the comparator, respectively. This is by far better than the other comparable organic circuits in literature. Other low power consumption circuits includes Guerin [18], although it shows an amplifier with a VDD of 40 V, and Nausieda [17], whose amplifier has very low gain-bandwidth of 7,5 Hz. The comparator presented in this chapter, works with a low number of OTFTs, a lower voltage compared to the others in the literature and at higher input and clock frequencies of 10 and 100 KHz, respectively. Nevertheless, a better control of the mobility is necessary in order to have a stable dynamic behavior of the circuits. A better modeling of the electrical bias stress is also needed in order to predict the variation of the DC bias current in the circuits.

6.6 Conclusion

In this chapter the first digital and analog circuits blocks were presented based on the 2 μm self-aligned OTFT technology. Both the DC gain of simple inverters and of differential amplifiers were measured with good matching according to the theoretical results. The output signals of a functional NOR logic gate and a comparator were also successfully tested. These basic circuit blocks are the first step of a long term process aimed at forming the interface between flexible sensors with fast responses and conventional electronics.

7

Open Source CAD Layout Tools for Thin Film Emerging Technologies

7.1 Introduction to Alliance CAD Tools

This work proposes to adjust, for emerging technologies, a process independent complete set of design tools with the Alliance team on LIP6 to design customized circuit level cell libraries for every thin film transistor technology in an easy-to-fabricate and low cost procedure. A list of the tools already developped in this chapter are presented in Table 7.1. On section 7.2 is presented the adaptation of the different Alliance ©tools. On section 7.3 a proof of concept is shown where the design rules to layout of thin film devices are implemented. Finally, different analog standard cells such as a differential amplifier and a comparator developed in chapter 5, are designed.

Alliance © is a set of open source, free CAD tools and portable libraries [79] developed at the laboratory of Informatics of Paris 6 (LIP6) of the University Pierre et Marie Curie (UPMC) for educational and research purposes on VLSI design with conventional Silicon CMOS Technologies, Fig. 7.1. Several characteristics describes the performances of the Alliance tools, which is why this work is implementing them: it is intended for process independence to port the library cells designed from one technology to the next one and from one foundry to another one. The most important VLSI standards are supported with it, such as: SPICE and VHDL codes, and CIF and GDSII layout formats. It is as well compatible with the CADENCE environment. Every one of these tools work as well independently, but communicates among them smoothly and the design flow of work has a top-down approach.

An explanation of the Alliance CAD tools for Si CMOS design is presented in Appendix B.

Fig. 7.1: Alliance Logo

Table 7.1: Alliance CAD Tools implemented for the Organic Transistor Technology

Tools	Description
Graal	Symbolic Layout Editor
Dreal	Real Layout Editor
S2R	Symbolic to Real Layout Conversion
Cougar	Netlist Extractor
genlib	Placement and routing.
DRUC	Design Rules Checker

7.2 Alliance Concept for Emerging Printed and Flexible Technologies

This thesis works focuses on the design of standard cell libraries with few transistors, having functional performances in the field of printed and large area electronics. Therefore, the interest of this chapter is to show briefly, the development of a design flow of work at a low level (transistor level). The use of high level tools mentioned before, are avoided for digital design as the TFT technologies in this thesis work are not yet oriented to the design of large digital systems. A new tool called GOT, has been implemented with a collaboration with Dr. Franck Wajsburt from LIP6, it is a layout generator of organic transistor based on the design rules developed in this thesis. With this tool, a transistor will be viewed as a 3 port cell (remembering that a bulk connection does not exist).

The layout space has been parametrized by a symbolic unit of measurement called λ, which in the particular case for the designs in the Orgatech/LPICM-Ecole Polytechnique technology equals 15 μm. The minimal channel length equals 2λ or 30μm. The tool GOT takes the sizes for the OTFTs used in the circuits designed in chapter 5 and generate the first cell of the flow. The

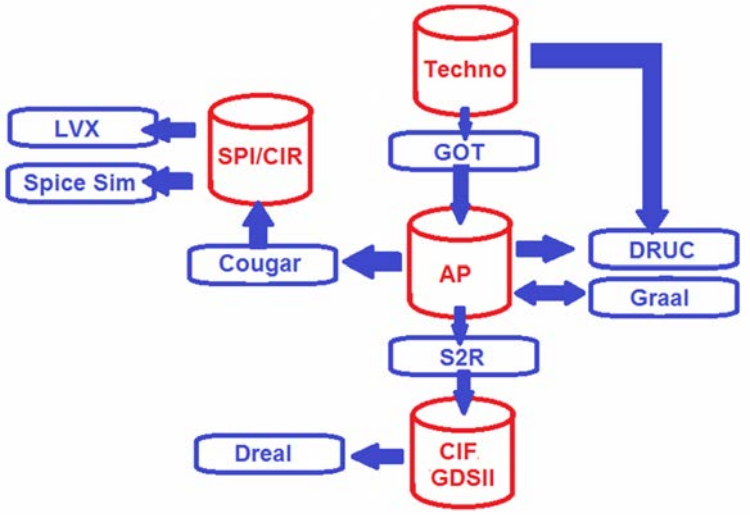


Fig. 7.2: Design Flow for the Organic Circuits with the Alliance CAD Tools

layout could be viewed by the symbolic layout editor Graal where every measurement is in λ as explained before. After a conversion of the data from symbolic layout to a real one by the tool S2R, the final masks could be viewed by another layout editor, Dreal.

The tool genlib placed each of the OTFT cells according: to the schematic designed and a set of design rules previously included as input data. With genlib, the connections were routed between the different OTFTs in the schematic design and to the pads placed in the border of the cell. This procedure creates another cell, a circuit. Each of the circuit cells are then placed in specific positions in the full layout.

An extraction of the netlist for an electrical verification with an Spice software is also possible by the tool Cougar.

This full layout in the case of the Orgatech/LPICM-Ecole Polytechnique represents the shadow masks which will be sent to a mask manufacturer. The flux diagram of the layout design is presented in Fig. 7.2. In blue are represented the tools and in red the files linking one tool with another. The first file is the Techno, having the design rules and parameter extracted from measured data. The file AP is the symbolic layout designed with Graal. The files SPI and CIR are the extracted netlists from the layout. Finally, the files CIF and GDSII contains the final IC layout format.

Table 7.2: Organic Thin Film Transistor Technology Layout Layers

Layout Layer	Description
Red	Gate (Metal1 or M1)
Cyan	Source/Drain (Metal2 or M2)
Gray	Organic Semiconductor
Dark Green	Dielectric
Black/Transparent	Substrate

7.3 Proof of Concept for a Layout of Integrated Circuits with Organic TFTs

In this section, a proof of concept is shown where the 2 principal blocks designed in chapter 5 are implemented cell by cell. The design rules and other constraints considering the technology are taken into account such as the fact that the dielectric is not yet able to be patterned and thus the input/output pads and other nodes, have to be connected in the border of the full mask.

7.3.1 Graal environment for symbolic layout design

First of all, the 5 layers implemented in the layout of a thin film transistor are shown in Table 7.2.

Fig. 7.3 shows the graphical user interface (GUI) for the Graal environment. In the center is the designed template of the shadow masks where each of the 8 standard cells will be placed, separated by metal guide lines in red (needed to cut the cells one by one for the measurement). The white lines are not a physical layer, but represent the exact axes where the genlib tool will place the cells. In the case of the technology used here, Orgatech/LPICM-Ecole Polytechnique, the big dark green square is the dielectric which will be spun over all the substrate and patterned just in the borders. There are also the different pads for the electrical tests composed of Metal1 (for the gate in red) and Metal2 (for the source and drain in cyan). The routing lines will go from the nodes in the circuit cells to those pads. The pads in pink color are a combination of the cyan and red color where there the 2 different metal lines 1 and 2 will encounter (it works as a via in our design).

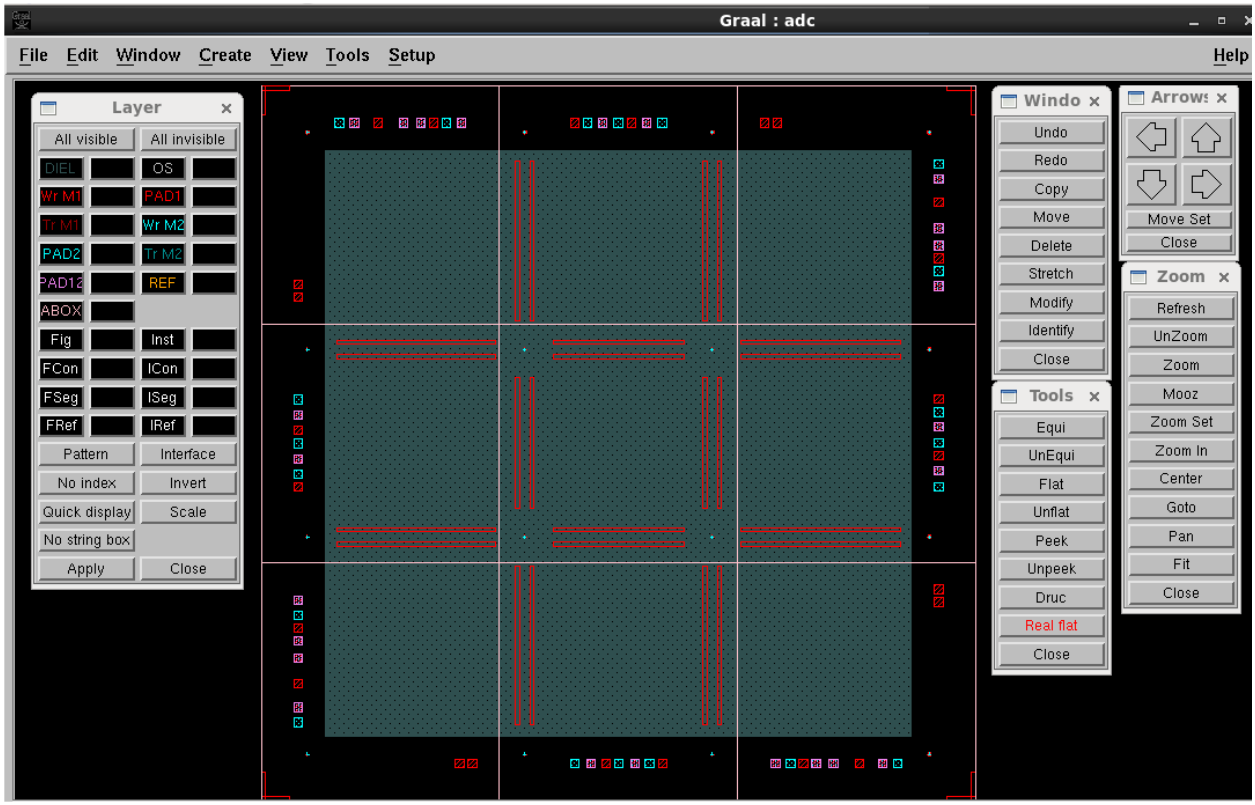


Fig. 7.3: Graal Design Environment

The alignment crosses with the minimal length needed for the shadow mask placement are not seen by the eye, however are represented by bright points in the cross area of the guide red lines. The Graal environment is also composed of several small windows. On the left of the layout we could see the different layers that we could enable or disable or even design by hand. On the right we show the windows to modify the layout, zoom, flatten the different cell views, among other things.

7.3.2 Design Rules for Organic Thin Film Transistor Technology

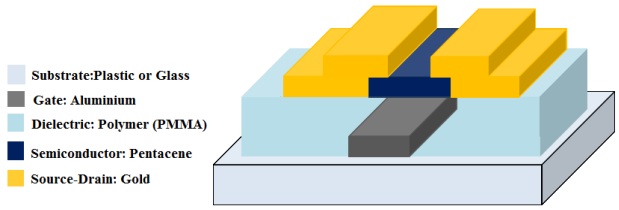
The second step is to define the layout design (or Process) rules for OTFTs and for the rest of the layout. Some of them are presented in Table 7.3 with the acronyms shown in the layout of an OTFT in Fig. 7.4(b). The sizes are shown in λ (L in the table) or symbolic unit of measurements. In the case of the Orgatech Technology, λ equals 30 μm. However, these design rules could be implemented with any other transistor having different channel lengths. The rules were imple-

Table 7.3: Design Rules for the Orgatech/LPICM-Ecole Polytechnique Technology

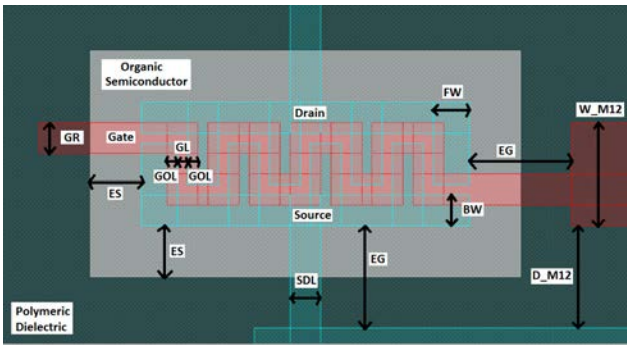
Name	Rules in λ	Description
FW	6	Finger Width
BW	6	Finger Base Width
GL	2	Gate Length
GR	6	Gate Real Length
EG	16	Extension Gate from DS (Drain/Source)
ES	10	Extension Semi-conductor from DS
EA	20	Extension Abutment box from DS
MAX_ OS	160	Org. semiconductor maximale size
W_M12	20	Metal1 and Metal2 width
D_M12	20	any M1 or M2 distance side to side
W_PAD	40	PAD size
DLX_SIZE	2730	Dielectric size in x axe
DLY_SIZE	2730	Dielectric size in y axe
C_NAME	74	Connector name size

mented in the code for the genlib tool, due to the fact that it will place the cells according to the full layout (e.g: the size of the total mask, the size of the dielectric, the length of the red guides lines,...). In addition, the layout will be macro generated from previously defined design rules (nothing will be designed by hand). By this, the layout will not have errors and the design rule checker tool, DRUC, will not be necessary.

The different polygons shown in Fig.7.4(b) are (for the reader not used to this type of transistor), openings in the metallic shadow masks. The grains of the different materials will be filtered with these masks and deposited on the substrate. Moreover, the source and drain contacts of the OTFT have been designed with an interdigitated structure to save space in the layout, due to the fact that the transistor in the organic technologies are wide. In this technology, a width of several thousand μm is normal.



(a)



(b)

Fig. 7.4: a) 3D image of the Organic Thin Film Transistor in the Orgatech/LPICM-Ecole Polytechnique technology. b) Top view of the OTFT with the design rules.

7.3.3 Differential Amplifier Layout

The third step is to use the already defined 3-port OTFT cells to place and route them together to create a circuit, for example the differential amplifier of chapter 5. A tool called genlib is implemented here in a collaboration with Dr. Franck Wajsburt from LIP6-UPMC, to place and route each OTFT and each circuit cell defined by a netlist as a black box with the specific ports. The layout of the differential amplifier cell is presented in Fig. 7.5. As explained before, the pads have to be placed in the border in order to reduce the complexity of the patterning of the dielectric in this technology. Nevertheless, if the dielectric is changed and patterned locally, it is possible to place the pads in a conventional design at each side of the cell.

The final fourth step is the extraction of the netlist and the electrical verification of a circuit cell. The code in Spice of the differential amplifier netlist in a .cir or .spi file is presented below with the comments within it:

```
  * Spice description of diffamp
* Name of the ports of the diff amp cell for pad connections:
```

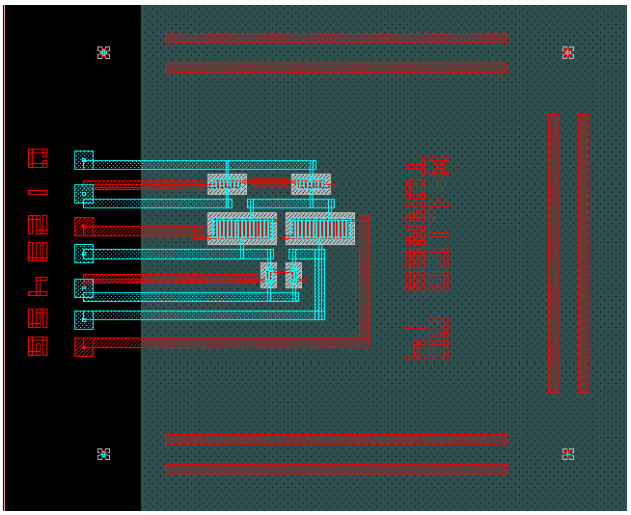


Fig. 7.5: Layout of the differential amplifier using Alliance CAD Tools.

```
* INTERF iss vdd vinn vinp voutn voutp vss

  * List of the included OTFTs already generated:
. INCLUDE otft_ g34f1dp0sp0.spi
. INCLUDE otft_ g670f8dm20sp0.spi
. INCLUDE otft_ g134f4dp0sp0.spi

  * Number of the ports of the diff amp cell for pad connections:
. subckt diffamp 8 6 30 13 19 25 23

  * List of all nodes in the circuit:
* NET 6 = vdd
* NET 8 = iss
* NET 12 = m1m2m5
* NET 13 = vinp
* NET 19 = voutn
* NET 23 = vss
* NET 25 = voutp
```

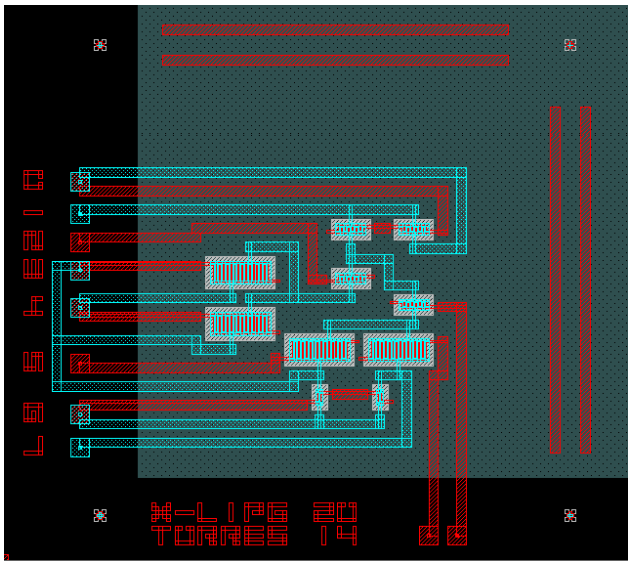


Fig. 7.6: Layout of the source coupled latch comparator presented in Chapter 5.

```
* NET 30 = vinn


  * List of OTFTs connected in the diff amp as 3-port cells:
xm3 19 23 23 otft_ g34f1dp0sp0
xm1 12 13 19 otft_ g670f8dm20sp0
xm6 6 8 8 otft_ g134f4dp0sp0
xm4 25 23 23 otft_ g34f1dp0sp0
xm2 12 30 25 otft_ g670f8dm20sp0
xm5 6 8 12 otft_ g134f4dp0sp0
. ends diffamp
```

7.3.4 Comparator Layout

The process is repeated for another circuit cell, the comparator. The source coupled latch comparator with the input/output pads is presented in Fig. 7.6 with its respective layout in Fig. 7.6.

7.3.5 Sigma Delta Modulator Layout

For the design of the full mask, every cell was placed in the correct part of the layout. In Fig. 7.3, the background of the full layout was presented without the circuit cells. In fact, the 2 designed layout of the differential amplifier and the source coupled latch comparator will be placed, in each of the spaces oriented in the peripheric of it with the pads placed outside of the dielectric squared layer. The tool genlib is also used to define each circuit cell as a blackbox with all of the inputs and outputs and then placed them where it is necessary. Finally, on Fig. 7.7 the full layout of the shadow masks is presented. Every cell is designed separately to be characterized by their single performances. After being cut and separated from the complete sample, the connections will be done with a process of low temperature bonding wires to a conventional IC platform. The Sigma Delta modulator as it is not integrated will be tested with a conventional connection scheme in a breadboard with each of the circuit cells connected on it.

7.4 Conclusion

A layout design flow of work of an Organic Thin Film Transistor technology was presented, using the CAD tools Alliance ©. This is an easy process independent approach which could be implemented with any thin film technology. This chapter showed the implementation of the layout editors: Graal for a symbolic representation of it, and Dreal for its view in real units of measurement. The design rules are introduced since the beginning and the cells are macro generated, first the OTFT and then the circuits. This work implemented also a netlist-oriented cell library for placement and routing called genlib in a collaboration with LIP6. This methodology allows to design a correct layout by construction without the need of a final verification by a design rule checker tool. The netlist could also be extracted from the layouts with the tool Cougar for an electrical verification. Finally, the layout of a full shadow mask was presented as the proof of concept placing the 2 analog standard cells designed in this thesis work.

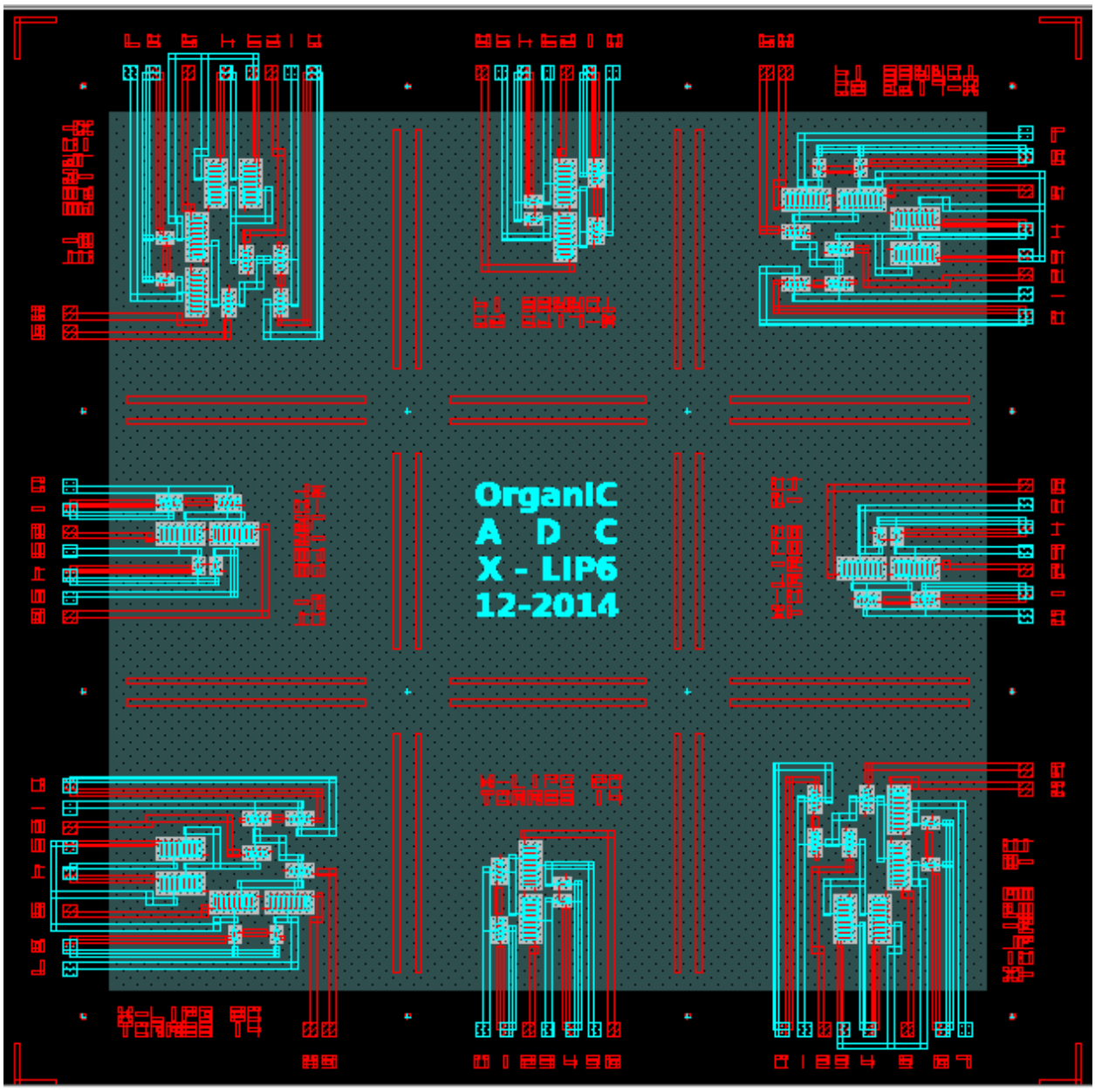


Fig. 7.7: Layout of the 2 diffrent cells that compose a Sigma Delta Modulator

Part IV

Conclusions

8

Conclusion and Future Work

8.1 Research Overview

8.1.1 Design Kit with Organic Transistors

In both technologies a design kit was elaborated comprising physical parameters extracted for circuit design and layout design rules. An a-Si TFT Spice model presented in commercial simulators was adapted and used to model the organic transistor DC behavior. The dielectric and the semiconductor layer were characterized till obtaining stable and reproducible layers. The physical parameters describing their behavior (dielectric capacitance, mobility) were quantified to be taken into account for circuit design.

Orgatech/Ecole Polytechnique Technology:

A mismatch model based on the above mentioned Spice model was calculated in order to quantify the variations of all the physical parameters. This model allows to compute the dispersion in the measured current curves. The percentage value is necessary for mismatch analysis in mirror current sources, differential circuits and in general for variation aware analog design. The model also was simplified for circuit design which extends the work of C.H.Kim [9]

Joanneum Research Technology:

Although the mismatch model was not implemented due to time constraints, a design kit for a low power technology fabricated by photolithography was developed. An ultra thin photo patternable dielectric layer with a thickness under 100 nm (no pin-holes) was used. The result is a transistor with an operating voltage of 5 V. The model implemented fits better the experimental curves and is more developped compared to the one presented by Zanella [11].

8.1.2 Circuit Design of Functional Analog and Digital Circuits on Plastic Foils

The Spice model was used to obtain by hand calculations the performances of both technologies (such as DC gain, frequency, etc). The simulations in a commercial Spice software, improved our analysis. These performances parameters were compared with measured values to test how close does the model describes the reality. In both technologies, a functional sigma delta modulator was designed, composed of 2 active blocks: a differential amplifier having 6 OTFTs and a 9 OTFT, 2-stage source coupled latch comparator, summarizing just 25 OTFTs. The simulation results showed with both modulators, the best ADC performances reported to date concerning low number of OTFTs, SNR and number of bits.

Orgatech/Ecole Polytechnique Technology:

A simulated SNR of 30 dB and 4,75 effective number of bits was obtained. The simplification of the fabrication process by shadow masks, make it an interesting approach compared to the other photolithographic ones which are complex and more expensive to fabricate. The statistical parameter extraction allowed to analyse the yield of circuits with Monte Carlo simulations. Dielectric thickness and mobility variations were found to affect the DC gain and frequency response of the designs respectively.

Joanneum Research Technology:

A Transistor Evaluation Module (TEM) was designed including analog and digital circuits. The digital circuits such as inverters and logic gates were functional with rise and fall times under 1 ms. A differential voltage amplifier was measured with the largest gain bandwidth reported to date of 3000 Hz and a functional source coupled latch comparator, both consuming 49 and 100 μW of power, respectively. A new bonding wire process at low temperature was developed, in order to test plastic circuit with numerous pads. Concerning the sigma delta modulator simulated, an SNR of 28 dB and 4,36 effective number of bits was obtained. However, the offset voltages and mismatches in the branches of the differential cells needs to be improved in order to connect the 2 above tested analog blocks.

8.1.3 Customization of the Alliance CAD Systems for Emerging TFT Technologies

A set of free open source VLSI CAD tools, Alliance ©, were customized for the automatization of layout design of circuits using organic transistors. The standard cells of the 2 analog blocks were designed as a proof of concept. As the layouts are symbolic, these standard cells could be reused with an improved technology node with a shorter channel length, just by setting the correct design rules manual (DRM). This work presents a free open source option with a more integrated environment compared to the work of [25] which used commercial and non-open source tools.

8.2 Future Work

In both research groups, this model has to be implemented as a de facto standard for circuit design with organic transistors. The adapted a-Si TFT model with the modifications for the sub-threshold and leakage regimes presented by C.H.Kim [9] has to be included in a commercial Spice simulator. The simplicity of this model allows to compare the design performances between the different research groups. In addition, some improvements have to be included concerning, first: a physical explanation of the β_{sat} and V_{Th} variations into the mismatch model, similar to the Pelgrom model for CMOS transistors. Second, to include a model which predicts the bias points variations in time for a better analog design.

Orgatech/Ecole Polytechnique Technology:

- To improve the technology process by fabricating organic transistors with a patternable dielectric with a sub 100 nm of thickness.
- To develop a passivation layer to protect the semiconductor from environmental degradation.
- To test of the simulated Sigma Delta Modulator.
- To design of digital circuits for the decimation filter of the sigma delta modulator.
- To develop an improved CAD system from Alliance © including all of the tools needed with a single interface.

Joanneum Research Technology:

- To improve the technology process by adding a passivation/dielectric interlayer (as a field oxide in silicon) for a third metal level and to protect the semiconductor layer.
- To test the Transistor Evaluation Module Mask with p-Type semiconductors having higher and stable mobility with at least 1,0 cm^2/Vs for faster circuits looking for delays as low as 1 μs.
- To design with the tested blocks (the amplifier, the comparator, and the logic gates) in this thesis, a full system with a sensor and a read out circuit. The tested blocks have to include notably, a common mode feedback circuit to adjust input and output offset voltages and mismatches.

9

List of Publications

- 2013

  M. Torres-Miranda, A. Al-Mutairi, H. Aboushady, Y. Bonnassieux, "Highly Reliable Fabrication & Modeling Process of Pentacene TFT for Analog Circuit Design" International Conference on Organic Electronics, ICOE13, France, Grenoble, June 2013.

- 2014

  M. Torres-Miranda, A. Al-Mutairi, H. Aboushady, Y. Bonnassieux, "Fabrication and Parameter Extraction of High Performing PMMA-Pentacene TFTs for Circuit Design" International Thin Film Transistor Conference, ITC2014, The Netherlands, Delft, January 2014.

  M. Torres-Miranda, F. Wajsburt, H. Aboushady, Y. Bonnassieux, "Full Customized Layout Design Environment for Integrated Systems with TFTs" International Thin Film Transistor Conference, ITC2014, The Netherlands, Delft, January 2014.

- 2015

  A. Petritz, A. Fian, T. Rothländer, M. Torres-Miranda, T. Grisser, M. Irimia-Vladu, B. Stadlober, "Photopatternable dielectrics for low voltage organic digital and analog circuits" International Conference on Organic Electronics, ICOE15, Germany, Erlangen, June 2015.

Appendices

A

ADC Theory

A.1 Analog to Digital Converters Principal Relations

The principal equations to determine the performance of a conventional oversampled Analog-to-Digital converter are listed below.

The oversampling ratio OSR (the ratio of the sampling frequency f_s to the useful frequency or bandwidth BW, in a low pass filter) taking into account the Nyquist criteria is:

$$OSR = \frac{f_s}{2BW} \tag{A.1}$$

The quantization noise variance is:

$$\sigma_q^2 = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} q^2 dq = \frac{\Delta^2}{12} \tag{A.2}$$

Where Δ is the quantization step which equals $\Delta = \frac{2A}{2^N}$, A is the voltage amplitude of the signal and N is the number of bits. The power of the signal is however the squared RMS value of the input signal or $\frac{A^2}{2}$. From a practical point of view, the $Power_{noise}$ implies not only the quantization noise, but also all of the noise components considered in the circuit.

The power spectral density of the quantization noise is:

$$Power_{noise}(f) = \frac{\sigma_q^2}{f_s} = \frac{\Delta^2}{12 f_s} = \frac{A^2}{2^{2N-2} 12 f_s} \tag{A.3}$$

The power of the signal is represented in the frequency domain with a graphic called the Power Spectral Density. The Signal to Noise Ratio (SNR) is calculated from the integration of the power of the signal minus the power of the noise in the useful band. This value allows the measurement of the Effective Number of Bits (ENOB):

$$ENOB = \frac{SNR(dB) - 1,76}{6,02} \tag{A.4}$$

Finally, a practical and useful figure of merit (FoM) of comparing the energy converted per bit among different ADCs is:

$$FoM = \frac{Power_{Consumption}}{2^{ENOB}2BW} \tag{A.5}$$

A.1.1 Conventional Oversampled Analog to Digital Converters Signal to Noise Ratio Relation

The power of the quantification noise is the integration in frequency of the power spectral density Eq. A.3:

$$Power_{noise} = \int_{-BW}^{BW} Power_{noise}(f)df = \frac{\Delta^2}{12OSR} = \frac{A^2}{2^{2N-2}12OSR} \tag{A.6}$$

Taking into account just the quantization noise for the power of the signal, the SNR in dB is:

$$SNR(dB) = 10log\frac{Power_{signal}}{Power_{noise}} = 10log\frac{\frac{A^2}{2}}{\frac{A^2}{2^{2N-2}12OSR}} \tag{A.7}$$

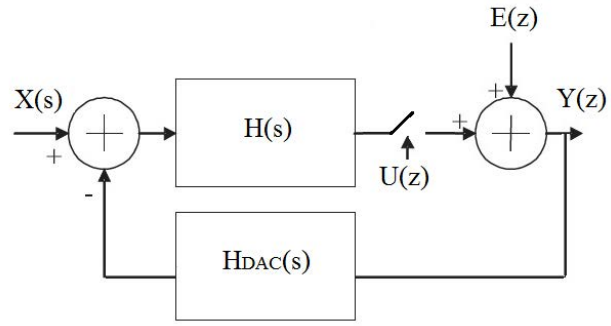
Simplifying:

$$SNR(dB) = 1,76 + 6,02N + 10log(OSR) \tag{A.8}$$

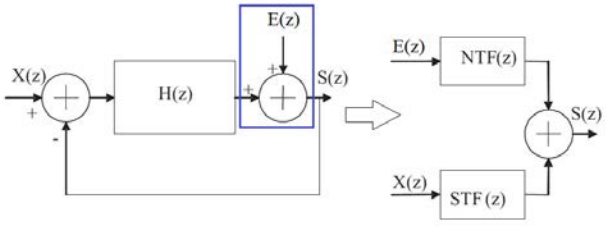
With a large OSR, the SNR could be increased, however as mentioned before the OTFTs work at frequencies around KHz. A large OSR would reduce the bandwith of the input signal. An OSR of 128 with a sampling frequency $f_s = 1024Hz$ implies a bandwith of 4Hz, with 6 bits the SNR=59 dB. However for a reasonable OSR of 32, the same f_s, a larger bandwidth of 16Hz and 5 bits, ideally an SNR of 53 dB is obtained losing 6 dB, but increasing by 4 the bandwith.

A.1.2 Analog to Digital Converters based on Sigma Delta Modulators Signal to Noise Ratio Relation

A sigma delta modulator could be represented in continuous time, Fig. A.1(a) or in discrete time, Fig. A.1(b). In this last case, it could be separated from a system level point of view in 2 functional blocks: a Signal Transfer Function block (STF) and a Noise Transfer Function block (NTF). Where X(z) is the input signal and E(z) is the added quantization noise, both in the Z-domain. In the most



(a)



(b)

Fig. A.1: a) Block model of a continuous time sigma delta modulator. b) Block model of a discrete time sigma delta modulator.

ideal case in system, the DAC is not considered to add an error, therefore its transfer function in continuous time $H_{DAC}(s)$ equals 1. In the figures, the first summing point recovers the feedback loop and the second summing point adds the quantization noise to the analog signal coming from the filter and then convert it to the digital output signal. The addition of quantization noise is a fundamental limit in every real ADC.

$$S(z) = STF(z)X(z) + NTF(z)E(z) \tag{A.9}$$

$$STF(z) = \frac{H(z)}{1 + H(z)} \tag{A.10}$$

$$NTF(z) = \frac{1}{1 + H(z)} \tag{A.11}$$

Maximizing H(z) will decrease the NTF(z) till getting closer to 0, and STF(z) will get close to unity. Therefore converting the input analog signal to the output digital signal adding minimal

noise to the system. The power spectral density of the quantization noise is thus shaped by the noise transfer function. Its integration in frequency, the power of the quantization noise is:

$$Power_{noise} = \int_0^{BW} Power_{noise}(f)|NTF(f)|^2 df = \frac{A^2}{2^{2N-2}12f_s} \int_0^{BW} |NTF(f)|^2 df \quad \text{(A.12)}$$

In the case of a 1st order sigma delta modulator with a delaying integrator having a transfer function in the Z-domain of the form:

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \quad \text{(A.13)}$$

The NTF transfer function becomes $NTF(z) = 1 - z^{-1}$ or in frequency $NTF(f) = 1 - e^{-j2\pi f/f_s}$. The power of the quantization noise is in this case:

$$Power_{noise} = \frac{A^2\pi^2}{2^{2N-2}36OSR} \quad \text{(A.14)}$$

The SNR of a Sigma Delta Modulator is thus:

$$SNR(dB) = 10log\frac{Power_{signal}}{Power_{noise}} = 6,02N + 1,76 - 5,17 + 30log(OSR) \quad \text{(A.15)}$$

In this case, for every doubling in the OSR, the SNR increases by 9,03 dB, which means that the ENOB increases by 1,5 bit. This is the most important advantage of the Sigma Delta Modulation.

B

Alliance Tools for CMOS Design

B.1 Alliance CAD Tools in CMOS Design

Alliance © is a set of open source, free CAD tools containing more than 600 000 lines of C code. Binaries, source code and cells libraries are freely available under the GNU General Public License (GPL). It includes a layout editor, a VHDL compiler and simulator, logic synthesis, automatic place and route, validation and formal proof tools, among other state of the art design tools. It has been used succesfully for many research projects such as a 875 000 transistors VLIW StaCS processor at LIP6, a 16 bits processor in the rohm 0.18 μm in 2010 from the Tokai University (Shimizu Lab) and a complete circuit in the xfab XH035 technology in 2014 from Smartlabs/Smarthome. Alliance ©CAD system is implemented to be used for a Unix system with just a C compiler.

In the case of CMOS digital design it starts from the capture and simulation of the behavioral view: where VHDL code is simulated and validated using a tool called Asimut. A pattern of stimuli generated is also used with another tool called genpat.

It continues with the capture and validation of the structural view where 2 tools are used, boog which enables a conversion of a behavioural VHDL description to a netlist of standard cells and genlib which enables the capture and placement of netlist-oriented standard cell libraries written in C language (this tool has been implemented in our design as we will see later).

For analog and mixed signal design it starts from the implementation of the physical design where the netlist resulting from the previous phase are assembled with a tool called ocp, routed together with a tool called nero and finally routed to the external pads with another tool called ring. The resulting layout which has symbolic unit of measurements till this phase, could be

viewed and edited with a tool called Graal. Then it is converted to a real unit of measurements corresponding to the technology of interested with a tool called s2r. The final layout could be viewed in the real unit of measurements with a tool called Dreal

Finally, the verification phase follows where the layout is verified with a design rules checker called Druc. The netlist is extracted with a tool called Cougar from the generated layout in order to verify it from an electrical point of view, where another tool called LVX is used, for a comparision between the layout and the schematic of the circuit.

The layout is then finished in order to be fabricated at a foundry.

Table B.1: Alliance CAD Tools implemented for conventional Si CMOS Technology. With an (*) the ones implemented for the Organic Transistor Technology

Tools	**Description**
Graal*	Symbolic Layout Editor
Dreal*	Real Layout Editor
S2R*	Symbolic to Real Layout Conversion
Cougar*	Netlist Extractor
genlib*	Netlist capture.
DRUC*	Design Rules Checker
LVX	Layout versus Schematic
Asimut	VHDL compiler and simulator
genpat	Patterns generator for VHDL
xpat	Graphical pattern viewer
ocp	Standard cell placer
nero	Over cell router
ring	Core to pads router
syf	Finite state machine synthesizer
boom	Boolean optimization of VHDL data flow
boog	Behavioral descrip. Map to Standard Cell lib
loon	Fanout optimizer and timing analyser
scapin	Scan Path insertion
xsch	Graphical schematic viewer

References

1. C. H. Kim, Y. Bonnassieux, and G. Horowitz, "Charge distribution and contact resistance model for coplanar organic field-effect transistors," *IEEE Transactions on Electron Devices*, vol. 60, no. 1, pp. 280–287, Jan. 2013.
2. ——, "Fundamental benefits of the staggered geometry for organic field-effect transistors," *IEEE Electron Device Letters*, vol. 32, no. 9, p. 1302–1304, Sep. 2011.
3. B. Razavi, *Design of Analog CMOS Integrated Circuits*. McGraw-Hill, 2001.
4. L. Li, M. Debucquoy, J. Genoe, and P. Heremans, "A compact model for polycrystalline pentacene thin-film transistor," *J. Appl. Physics*, vol. 107, no. 024519, pp. 1–3, Jan. 2010.
5. O. Marinov and M. J. Deen, "Quasistatic compact modelling of organic thin-film transistors," *Organic Electronics*, vol. 14, pp. 295–311, Jan. 2013.
6. M. Estrada, A. Cerdeira, J. Puigdollers, L. Resendiz, J. Pallares, L. Marsal, C. Voz, and B. Iniguez, "Accurate modeling and parameter extraction method for organic tfts," *Solid-State Electronics*, vol. 49, pp. 1009–1016, Mar. 2005.
7. C. Kim, Y. Bonnassieux, and G. Horowitz, "Compact dc modeling of organic field-effect transistors: Review and perspectives," *IEEE Transactions on Electron Devices*, vol. 61, no. 2, pp. 1136–1141, Feb. 2014.
8. "Eldo device equations manual, release ams version 2a," Mentor Graphics Release AMS Version 2a, 2008.
9. C. H. Kim, A. Castro-Carranza, M. Estrada, A. Cerdeira, Y. Bonnassieux, G. Horowitz, and B. Iniguez, "A compact model for organic field-effect transistors with improved output asymptotic behaviors," *IEEE Transactions on Electron Devices*, vol. 60, no. 3, pp. 1136–1141, Mar. 2013.
10. C. H. Kim, D. Tondelier1, B. Geffroy, Y. Bonnassieux, and G. Horowitz, "Characterization of the pentacene thin-film transistors with an epoxy resin-based polymeric gate insulator," *Eur. Phys. J. Appl. Phys.*, vol. 57, no. 20201, pp. 1–6, Jan. 2012.
11. F. Zanella, N. Marjanovic, a. H. G. R. Ferrini, A. Haase, A. Fian, B. Stadlober, R. Müller, J. Genoe, H. Hirshy, A. Drost, M. König, K.-D. Lee, J. Ring, R. Prétôt, C. Enz, and J.-M. Sallese, "Design and modeling of self-aligned nano-imprinted sub-micrometer pentacene-based organic thin-film transistors," *Organic Electronics*, vol. 14, p. 2756–61, Aug. 2013.
12. A. Petritz, A. Wolfberger, A. Fian, J. R. Krenn, and B. S. T. Griesser, "High performance p-type organic thin film transistors with an intrinsically photopatternable, ultrathin polymer dielectric layer," *Organic Electronics*, vol. 14, pp. 3070–3082, Jul. 2013.
13. H. Kawaguchi, T. Someya, T. Sekitani, and T. Sakurai, "Cut-and-paste customization of organic fet integrated circuit and its application to electronic artificial skin," *IEEE JSSC*, vol. 40, no. 1, pp. 177–185, Jan. 2005.

14. G. Maiellaro, E. Ragonese, A. Castorina, S. Jacob, M. Benwadih, R. Coppard, E. Cantatore, and G. Palmisano, "High-gain operational transconductance amplifiers in a printed complementary organic tft technology on flexible foil," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 12, Dec. 2013.
15. E. v. V. H. Marien, M. S. J. Steyaert and P. Heremans, "A fully integrated sigma delta adc in organic thin-film transistor technology on flexible plastic foil," *IEEE JSSC*, vol. 46, no. 1, pp. 276–284, Jan. 2011.
16. N. Gay, W.-J. Fischer, M. Halik, H. Klauk, U. Zschieschang, and G. Schmid, "Analog signal processing with organic fets," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2006 IEEE International*, Feb. 2006.
17. I. Nausieda, K. K. Ryu, D. D. He, A. I. Akinwande, V. Bulovic, and C. G. Sodini, "Mixed-signal organic integrated circuits in a fully photolithographic dual threshold voltage technology," *IEEE Transactions on Electron Devices*, vol. 58, no. 3, pp. 865–873, Mar. 2011.
18. M. Guerin, A. Daami, S. Jacob, E. Bergeret, E. Bènevent, P. Pannier, and R. Coppard, "High-gain fully printed organic complementary circuits on flexible plastic foils," *IEEE Transactions on Electron Devices*, vol. 58, no. 10, pp. 3587–3593, Oct. 2011.
19. H. Marien, M. Steyaert, N. van Aerle, and P. Heremans, "A mixed-signal organic 1 khz comparator with low vt sensitivity on flexible plastic substrate," in *Proceedings of the ESSCIRC09*, 2009.
20. S. Abdinia, M. Benwadih, E. Cantatore, I. Chartier, S. Jacob, L. Maddiona, G. P. M. R. F. T. G. Maiellaro, L. Mariucci, and A. van Roermund, "Design of analog and digital building blocks in a fully printed complementary organic technology," in *Proceedings of the ESSCIRC*, Sep. 2012, pp. 145–148.
21. H. Marien, M. Steyaert, E. V. Veenendael, and P. Heremans, "1d and 2d analog 1.5khz air-stable organic capacitive touch sensors on plastic foil," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, Feb. 2012, pp. 310–312.
22. S. Abdinia, M. Benwadih, R. Coppard, S. Jacob, G. Maiellaro, G. Palmisano, M. Rizzo, A. Scuderi, F. Tramontana, A. van Roermund, and E. Cantatore, "A 4b adc manufactured in a fully-printed organic complementary technology including resistors," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, Feb. 2013, pp. 106–107.
23. W. Xiong, U. Zschieschang, H. Klauk, and B. Murmann, "A 3v 6b successive-approximation adc using complementary organic thin-film transistors on glass," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*, Feb. 2010, pp. 134–135.
24. D. Raiteri, P. van Lieshout, A. van Roermund, and E. Cantatore, "An organic vco-based adc for quasi-static signals achieving 1lsb inl at 6b resolution," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, Feb. 2013, pp. 108–110.
25. F.Vila, J. Pallarès, L. Terés, J. Carrabina, and K. Sabine, "Physical design flow and eda open/free tools for printed electronics," in *International Conference on Organic Electronics, ICOE12, Tarragona, Spain*, 2013.
26. K. Myny, E. V. Veenendaal, G. H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, "An 8b organic microprocessor on plastic foil," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International*, Feb. 2011, pp. 322–324.
27. T. Sekitani, T. Yokota, U. Zschieschang, H. Klauk, S. Bauer, K. Takeuchi, M. Takamiya, T. Sakurai, and T. Someya, "Organic nonvolatile memory transistors for flexible sensor arrays," *Science*, vol. 326, pp. 1516–1519, Dec. 2009.
28. K. Ishida, N. Masunaga, R. Takahashi, T. Sekitani, S. Shino, U. Zschieschang, H. Klauk, M. Takamiya, T. Someya, and T. Sakurai, "User customizable logic paper (uclp) with organic sea-of-transmission-gates (sotg) architecture and ink-jet printed interconnects," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*, Feb. 2010, pp. 138–140.

29. H. Marien, M. Steyaert, N. van Aerle, and P. Heremans, "An analog organic first-order ct sigma-delta adc on a flexible plastic substrate with 26.5db precision," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*, Feb. 2010, pp. 136–138.
30. H. Gelinck, H. Huitema, E. V. Veenendaal, E. Cantatore, L. Schrijnemakers, J. V. der Putten, T. Geuns, M. Beenhakkers, J. Giesbers, B.-H. Huisman, E. Meijer, E. M. Benito, F. Towslager, A. Marsman, B. V. Rens, and D. D. Leeuw, "Active-matrix displays and shift registers based on solution-processed organic transistors," *Nature Materials*, vol. 3, pp. 106–110, Feb. 2004.
31. a. T. C. T. G. E. Cantatore, A. F. A. Gruijthuijsen, G. H. Gelinck, S. Drews, and D. M. de Leeuw, "A 13.56mhz rfid system based on organic transponders," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2009 IEEE International*, Feb. 2006.
32. K. Myny, M. Beenhakkers, N. van Aerle, G. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, "A 128b organic rfid transponder chip, including manchester encoding and aloha anti-collision protocol, operating with a data rate of 1529 b/s," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2009 IEEE International*, Feb. 2009, pp. 206–207.
33. M. Kaltenbrunner, M. S. White, E. D. Głowacki, T. Sekitani, T. Someya, N. S. Sariciftci, and S. Bauer, "Ultrathin and lightweight organic solar cells with high flexibility," *Nature Communications*, vol. 3, no. 770, pp. 1–7, Apr. 2012.
34. M. Takamiya, T. Sekitani, Y. Miyamoto, Y. Noguchi, H. Kawaguchi, T. Someya, and T. Sakurai, "Design solutions for a multi-object wireless power transmission sheet based on plastic switches," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2007 IEEE International*, Feb. 2007, pp. 362–364.
35. G. Kettlgruber, M. Kaltenbrunner, C. M. Siket, R. Moser, I. M. Graz, R. Schwodiauer, and S. Bauer, "Intrinsically stretchable and rechargeable batteries for self-powered stretchable electronics," *Journal of Materials Chemistry A*, vol. 1, no. 18, pp. 5505–5508, May 2013.
36. K. Ishida, T. Huang, K. Honda, Y. Shinozuka, H. Fuketa, T. Yokota, U. Zschieschang, H. Klauk, G. Tortissier, T. Sekitani, M. Takamiya, H. Toshiyoshi, T. Someya, and T. Sakurai, "Insole pedometer with piezoelectric energy harvester and 2v organic digital and analog circuits," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, Feb. 2012, pp. 308–310.
37. M. Hamedi, R. Forchheimer, and O. Inganäs, "Towards woven logic from organic electronic fibres," *Nature Materials*, vol. 6, pp. 357–362, May 2007.
38. D. Kim, R. Ghaffari, N. Lu, S. Wang, S. P. Lee, H. Keum, R. D'Angelo, L. Klinker, Y. Su, C. Lu, Y. Kim, A. Ameen, Y. Li, Y. Zhang, B. de Graff, Y. Hsu, Z. Liu, J. Ruskin, L. Xu, C. Lu, F. G. Omenetto, Y. Huang, M. Mansour, M. J. Slepian, and J. A. Rogers, "Electronic sensor and actuator webs for large-area complex geometry cardiac mapping and therapy," *PNAS*, vol. 109, no. 49, p. 19910–19915, Oct. 2012.
39. D. Khodagholy, T. Doublet, P. Quilichini, M. Gurfinkel, P. Leleux, A. Ghestem, E. Ismailova, T. Herve, S. Sanaur, C. Bernard, and G. Malliaras, "In vivo recordings of brain activity using organic transistors," *Nature Communications*, vol. 4, no. 1575, Mar. 2013.
40. D. Kim, N. Lu, R. Ghaffari, Y. Kim, S. P. Lee, L. Xu, J. Wu, R. Kim, J. Song, Z. Liu, J. Viventi, B. de Graff, B. Elolampi, M. Mansour, M. J. Slepian, S. Hwang, J. D. Moss, S.M.Won, Y. Huang, B. Litt, and J. A. Rogers, "Materials for multifunctional balloon catheters with capabilities in cardiac electrophysiological mapping and ablation therapy," *Nature Materials*, vol. 10, pp. 316–323, Apr. 2011.

41. M. Ying, A. P. Bonifas, N. Lu, Y. Su, R. Li, H. Cheng, A. Ameen, Y. Huang, and J. A. Rogers, "Silicon nanomembranes for fingertip electronics," *Nanotechnology*, vol. 23, no. 34, pp. 1–7, Aug. 2012.
42. D. H. Kim, N. Lu, R.Ma, Y. Kim, R. Kim, S. Wang, J. Wu, S. Won, H. Tao, A. Islam, K. J. Yu, T. Kim, R. Chowdhury, M. Ying, L. Xu, M. Li, H. Chung, H. Keum, M. McCormick, P. Liu, Y. Zhang, F. G. Omenetto, Y. Huang, T. Coleman, and J. A. Rogers, "Epidermal electronics," *Science*, vol. 333, no. 6044, pp. 838–843, Aug. 2011.
43. M. Torres-Miranda, A. Al-Mutairi, H. Aboushady, and Y. Bonnassieux, "Fabrication and parameter extraction of high performing pmma-pentacene tfts for circuit design," in *International Thin Film Transistor Conference, ITC2014, Deflt, The Netherlands*, 2014.
44. A. Petritz, A. Fian, T. Rothländer, M. Torres-Miranda, T. Grisser, M. Irimia-Vladu, and B. Stadlober, "Photopatternable dielectrics for low voltage organic digital and analog circuits," in *International Conference on Organic Electronics, ICOE15, Erlangen, Germany*, 2015.
45. M. Torres-Miranda, F. Wajsburt, H. Aboushady, and Y. Bonnassieux, "Full customized layout design environment for integrated systems with tfts," in *International Thin Film Transistor Conference, ITC2014, Deflt, The Netherlands*, 2014.
46. L. Gross, F. Mohn, N. Moll, P. Liljeroth, and G. Meyer, "The chemical structure of a molecule resolved by atomic force microscopy," *Science*, vol. 325, pp. 1110–1114, Aug. 2009.
47. H. Yanagisawa, T. Tamaki, M. Nakamura, and K. Kudo, "Structural and electrical characterization of pentacene films on sio2 grown by molecular beam deposition," *Thin Solid Films*, vol. 464, pp. 398–402, Jul. 2004.
48. O. Jurchescu, J. Baas, and T. T. M. Palstra, "Effect of impurities on the mobility of single crystal pentacene," *Applied Physics Letters*, vol. 84, no. 16, pp. 3061–3063, Apr. 2004.
49. M. Zirkl, A. Haase, A. Fian, H. Schön, C. Sommer, G. Jakopic, G. Leising, B. Stadlober, I. Graz, N. Gaar, R. Schwödiauer, S. Bauer-Gogonea, and S. Bauer, "Low-voltage organic thin-film transistors with high-k nanocomposite gate dielectrics for flexible electronics and optothermal sensors," *Advanced Materials*, vol. 19, no. 17, p. 2241–2245, Sep. 2007.
50. Y. Noh and H. Sirringhaus, "Ultra-thin polymer gate dielectrics for top-gate polymer field-effect transistors," *Organic Electronics*, vol. 10, pp. 174–180, Nov. 2008.
51. M. Yoon, H. Yan, A. Facchetti, and T. J. Marks, "Low-voltage organic field-effect transistors and inverters enabled by ultrathin cross linked polymers as gate dielectrics," *Journal of the American Chemistry Society*, vol. 127, pp. 10 388–10 395, Jun. 2005.
52. C. Kim, Z. Wang, H. Choi, Y. Ha, A. Facchetti, and T. J. Marks, "Printable cross-linked polymer blend dielectrics. design strategies, synthesis, microstructures, and electrical properties, with organic field-effect transistors as testbeds," *Journal of the American Chemistry Society*, vol. 130, pp. 6867–6878, May 2008.
53. C. B. Walsh and E. I. Franses, "Ultrathin pmma films spin-coated from toluene solutions," *Thin Solid Films*, vol. 429, pp. 71–76, Jan. 2003.
54. M. Na and S. Rhee, "Electronic characterization of al/pmma[poly(methyl methacrylate)]/p-si and al/cep(cyanoethyl pullulan)/p-si structures," *Organic Electronics*, vol. 7, pp. 205–212, Apr. 2006.
55. J. Park, L. Do, J. Bae, Y. Jeong, C. Pearson, and M. C. Petty, "Environmental effects on the electrical behavior of pentacene thin-film transistors with a poly(methyl methacrylate) gate insulator," *Organic Electronics*, vol. 14, p. 2101–2107, May 2013.
56. S. Nassif, K. Bernstein, D. Frank, A. Gattiker, W. Haensch, B. Ji, E. Nowak, D. Pearson, and N. Rohrer, "High performance cmos variability in the 65nm regime and beyond," in *Technical Digest International Electron Devices Meeting*, Dec. 2007, pp. 569–571.

57. B. Nikolic, J. Park, a. B. G. J. Kwak, Z. Guo, L. Pang, S., O. Toh, R. Jevtic, K. Qian, and C. Spanos, "Technology variability from a design perspective," *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol. 58, no. 9, Sep. 2011.
58. O. Yaghmazadeh, Y. Bonnassieux, A. Saboundji, B. Geffroy, D. Tondelier, and G. Horowitz, "A spice-like dc model for organic thin-film transistors," *Journal of the Korean Physical Society*, vol. 54, no. 1, pp. 526–526, Jan. 2009.
59. M. Pelgrom, A. Duinmaijer, and A. Welbers, "Matching properties of mos transistors," *IEEE Journal of Solid State Circuits*, vol. 24, no. 5, pp. 1433–1440, Oct. 1989.
60. M. Pelgrom, H. Tuinhout, and M. Vertregt, "Transistor matching in analog cmos applications," in *Technical Digest International Electron Devices Meeting*, Dec. 1998, pp. 915–918.
61. K. Lakshmikumar, R. Hadaway, and M. Copeland, "Characterization and modeling of mismatch in mos transistors for precision analog design," *IEEE Journal of Solid State Circuits*, vol. SC-21, no. 6, pp. 1057–1066, Dec. 1986.
62. J. Croon, M. Rosmeulen, S. Decoutere, W. Sansen, and H. Maes, "An easy-to-use mismatch model for the mos transistor," *IEEE Journal of Solid State Circuits*, vol. 37, no. 8, Aug. 2002.
63. B. Stadlober, U. Haas, H. Maresch, and A. Haase, "Growth model of pentacene on inorganic and organic dielectrics based on scaling and rate-equation theory," *Physical Review B*, vol. 74, no. 165302, pp. 1–9, Oct. 2006.
64. O. D. Jurchescu, B. H. Hamadani, H. D. Xiong, S. K. Park, S. Subramanian, N. M. Zimmerman, J. E. Anthony, T. N. Jackson, and D. J. Gundlach, "Correlation between microstructure, electronic properties and flicker noise in organic thin film transistors," *Applied Physics Letters*, vol. 92, no. 132103, Mar. 2008.
65. J. Park, L. Do, J. Bae, Y. Jeong, C. Pearson, M. C. Petty, J. E. Anthony, T. N. Jackson, and D. J. Gundlach, "Environmental effects on the electrical behavior of pentacene thin-film transistors with a poly (methyl methacrylate) gate insulator," *Organic Electronics*, vol. 14, pp. 2101–2107, May 2013.
66. E. Maricau and G. Gielen, "Transistor aging-induced degradation of analog circuits: Impact analysis and design guidelines," in *Proceedings of the ESSCIRC*, Sep. 2011, pp. 243–246.
67. W. Wang, V. Reddy, B. Yang, V. Balakrishnan, S. Krishnan, and Y. Cao, "Statistical prediction of circuit aging under process variations," in *IEEE Custom Integrated Circuits Conference*, Sep. 2008, pp. 13–16.
68. P. Kinget, "Device mismatch and tradeoffs in the design of analog circuits," *IEEE Journal of Solid State Circuits*, vol. 40, no. 6, pp. 1212–1224, Jun. 2005.
69. I. Nausieda, K. K. Ryu, D. D. He, A. I. Akinwande, V. Bulovic, and C. G. Sodini, "Dual threshold voltage organic thin-film transistor technology," *IEEE Transactions on Electron Devices*, vol. 57, no. 11, pp. 3027–3032, Nov. 2010.
70. R. J. Baker, *CMOS Circuit Design, Layout and Simulation, 3rd edition.* John Wiley and Sons, Inc, 2010.
71. U. Palfinger, C. Auner, H. Gold, A. Haase, J. Kraxner, T. Haber, M. Sezen, W. Grogger, G. Domann, G. Jakopic, J. R. Krenn, and B. Stadlober, "Fabrication of n- and p-type organic thin film transistors with minimized gate overlaps by self-aligned nanoimprinting," *Advanced Materials*, vol. 22, no. 5100, p. 15–19, 2010.
72. C. Auner, U. Palfinger, H. Gold, J. Kraxner, A. Haase, T. Haber, M. Sezen, W. Grogger, G. Jakopic, J. R. Krenn, G. Leising, and B. Stadlober, "High-performing submicron organic thin-film transistors fabricated by residue-free embossing," *Organic Electronics*, vol. 11, p. 552–57, Jan. 2010.
73. B. de Boer, A. Hadipour, M. M. Mandoc, T. van Woudenbergh, and P. W. M. Blom., "Tunning of metal work functions with self-assembled monolayers," *Advanced Materials*, vol. 17, no. 5, pp. 621–625, Mar. 2005.
74. K. Myny, S. D. Vusser, S. Steudel, D. Janssen, R. Muller, S. D. Jonge, S. Verlaak, J. Genoe, and P. Heremans, "Self-aligned surface treatment for thin film organic transistors," *Applied Physics Letters*, vol. 88, no. 222103, pp. 1–3, May 2006.

75. L. M. Fischer, M. Tenje, A. R. Heiskanen, N. Masuda, J. Castillo, A. Bentien, J. Émneus, M. H. Jakobsen, and A. Boisen, "Gold cleaning methods for electrochemical detection applications," *Microelectronic Engineering*, vol. 86, p. 1282–85, Jan. 2009.
76. S. Norsworthy, R. Schreier, and G. Temes, *Delta Sigma Data Converters*. IEEE Press, 1997.
77. J. Cabral-Moraes, *Realisation de un Convertisseur Analogique-Numerique Sigma-Delta a base de transistors organiques*. Internship Thesis, Ecole Polytechnique, 2014.
78. H. Sirringhaus, "Reliability of organic field-effect transistors," *Advanced Materials*, vol. 21, p. 3859–3873, Aug. 2009.
79. "Alliance cad system documentation," http://www-soc.lip6.fr/recherche/cian/alliance/.