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# Electro-thermal characterization, TCAD simulations and compact modeling of advanced SiGe HBTs at device and circuit level

Rosario d'Esposito

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# THÈSE

PRÉSENTÉE À

## L'UNIVERSITÉ DE BORDEAUX

ÉCOLE DOCTORALE DES SCIENCES PHYSIQUES ET DE L'INGÉNIEUR

Par **Rosario D'ESPOSITO**

POUR OBTENIR LE GRADE DE

**DOCTEUR**

SPÉCIALITÉ: ÉLECTRONIQUE

\*\*\*\*\*

**Electro-thermal characterization, TCAD simulations  
and compact modeling of advanced SiGe HBTs  
at device and circuit level**

\*\*\*\*\*

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*To Marco Di Rosa,  
a genius guy, a great friend*

*To all the people that supported me in this work*



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## Abstract

This work is focused on the characterization of electro-thermal effects in advanced SiGe hetero-junction bipolar transistors (HBTs); two state of the art BiCMOS processes have been analyzed: the B11HFC from Infineon Technologies (130nm) and the B55 from STMicroelectronics (55nm).

Special test structures have been designed, in order to evaluate the overall electro-thermal impact of the back end of line (BEOL) in single finger and multi-finger components. A complete DC and RF electrical characterization at small and large signal, as well as the extraction of the device static and dynamic thermal parameters are performed on the proposed test structures, showing a sensible improvement of the DC and RF figures of merit when metal dummies are added upon the transistor. The thermal impact of the BEOL has been modeled and experimentally verified in the time and frequency domain and by means of 3D TCAD simulations, in which the effect of the doping profile on the thermal conductivity is analyzed and taken into account.

Innovative multi-finger transistor topologies are designed, which allow an improvement of the SOA specifications, thanks to a careful design of the drawn emitter area and of the deep trench isolation (DTI) enclosed area.

A compact thermal model is proposed for taking into account the mutual thermal coupling between the emitter stripes of multi-finger HBTs in dynamic operation and is validated upon dedicated pulsed measurements and TCAD simulations.

Specially designed circuit blocks have been realized and measured, in order to verify the accuracy of device compact models in electrical circuit simulators; moreover the impact on the circuit performances of mutual thermal coupling among neighboring transistors and the presence of BEOL metal dummies is evaluated and modeled.

**Keywords:** Hetero-junction bipolar transistors (HBTs), electro-thermal effects, thermal resistance, thermal capacitance, thermal impedance, back end of line (BEOL), emitter-finger layout, SOA specifications, intra device mutual thermal coupling, circuits for model verification, device to circuit interactions, thermal TCAD simulations, doping profile thermal impact, semiconductor device characterization, pulsed measurements, load-pull characterization, HiCuM model, semiconductor device modeling.

## Résumé

Ce travail de thèse présente une étude concernant la caractérisation des effets électrothermiques dans les transistors bipolaires à hétérojonction (HBT) en SiGe. Lors de ces travaux, deux procédés technologiques BiCMOS à l'état de l'art ont été analysés: le B11HFC de Infineon Technologies (130nm) et le B55 de STMicroelectronics (55nm).

Des structures de test dédiées ont été conçues, pour évaluer l'impact électrothermique du back end of line (BEOL) de composants ayant une architecture à un ou plusieurs doigts d'émetteur. Une caractérisation complète a été effectuée en régime continu et en mode alternatif en petit et en grand signal. De plus, une extraction des paramètres thermiques statiques et dynamiques a été réalisée et présentée pour les structures de test proposées. Il est démontré que les figures de mérite DC et RF s'améliorent sensiblement en positionnant des couches de métal sur le transistor, dessinées de manière innovante et ayant pour fonction de guider le flux thermique vers l'extérieur. L'impact thermique du BEOL a été modélisé et vérifié expérimentalement dans le domaine temporel et fréquentiel et aussi grâce à des simulations 3D par éléments finis. Il est à noter que l'effet du profil de dopage sur la conductivité thermique est analysé et pris en compte.

Des topologies de transistor innovantes ont été conçues, permettant une amélioration des spécifications de l'aire de sécurité de fonctionnement, grâce à un dessin innovant de la surface d'émetteur et du deep trench (DTI).

Un modèle compact est proposé pour simuler les effets de couplage thermique en dynamique entre les émetteurs des HBT multi-doigts; ensuite le modèle est validé avec de mesures dédiées et des simulations TCAD.

Des circuits de test ont été conçus et mesurés, pour vérifier la précision des modèles compacts utilisés dans les simulateurs de circuits; de plus, l'impact du couplage thermique entre les transistors sur les performances des circuits a été évalué et modélisé. Finalement, l'impact du dissipateur thermique positionné sur le transistor a été étudié au niveau circuit, montrant un réel intérêt de cette approche.

**Mots-clés:** Transistors bipolaires à hétérojonction (HBTs), effets électrothermiques, résistance thermique, capacitance thermique, impédance thermique, back end of line (BEOL), layout des doigts d'émetteur, spécifications SOA, couplage thermique intra-device, circuits pour l'évaluation de modèles, interactions du composant au circuit, simulations thermiques TCAD, impact thermique du profil de dopage, caractérisation de composants à semi-conducteur, mesures pulsées, caractérisation load-pull, modèle HiCuM, modélisation de composants semi-conducteur.

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# Chapter 1

## General introduction

### 1.1 THz waves and applications

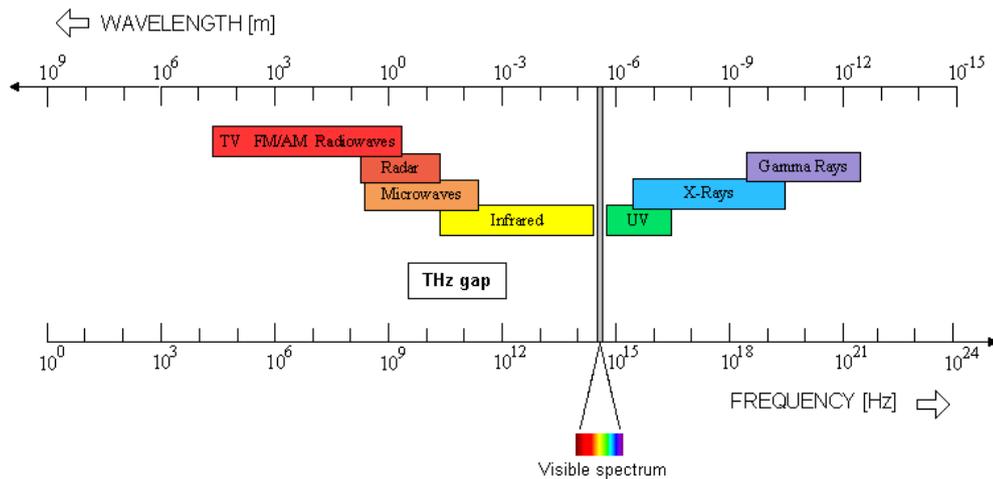


Figure 1.1: Overview of the electro-magnetic spectrum and related applications.

The terahertz (THz) region is a part of the electromagnetic spectrum lying between microwaves and infrared light, and is typically referred to frequencies from 300GHz up to 3THz [1], although there is no stated convention. Terahertz waves can penetrate various materials (clothing, plastic, ceramics, etc.) as well as tissues with low water content (millimeter wave dosimeters of human skin). Unlike X-rays, THz radiation is not ionizing, and, therefore, should cause no damage to live biological tissues. These characteristics allow a large number of new innovative applications [2] in the field of THz imaging and sensing for biology and medical sciences [3]–[5], non-destructive evaluation [6], [7], homeland security [8], [9]. Moreover, ultra-high-speed communication systems at THz frequencies [10], [11] can be attractive for the professional as well as the consumer market. However, with currently available and practical THz detectors and sources, measurements over distances larger than 20m are very difficult [12], besides, the attenuation level in the earth atmosphere for THz waves is higher than for the neighboring bands (see Figure 1.2). Obtaining THz signals with sufficient output power is exceptionally challenging and the lack of suitable devices to generate, detect, or properly process THz signals is the so called THz-gap. In fact, electronic sources, like transistors or multipliers, can go up to 1THz at room temperature [13], [14]; conventional laser diodes can easily generate signals at very high frequencies [15], but their use in the THz-gap region still appears impractical. For instance, free-electron lasers can generate electromagnetic radiation over a very wide range: from microwaves, through THz

radiation to X-ray. However, apart from being extremely expensive, they are bulky and not suitable for consumer applications.

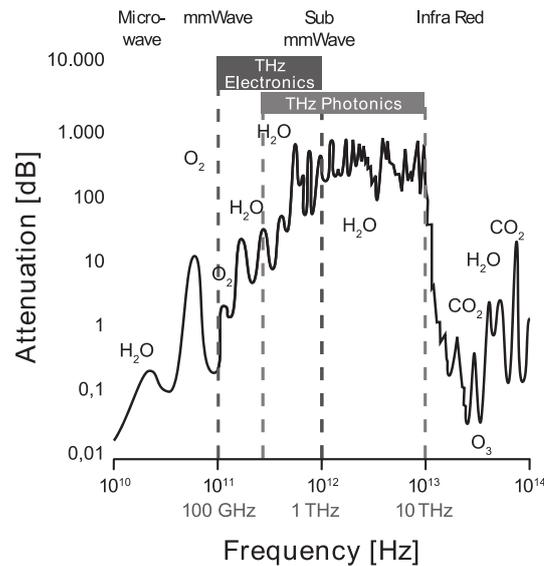


Figure 1.2: The atmospheric attenuation at terahertz frequencies shows the challenges of signal generation and detection for THz electronics and photonics [18].

## 1.2 SiGe BiCMOS technology

In millimeter wave applications, the III-V technologies have dominated the silicon technologies for many years. Performances of silicon technologies are still lower than GaAs, PHEMT and InP HBT HEMT. Devices fabricated in III-V technologies tend to have a superior performance compared to Si devices, due to higher carrier mobility. However, the high fabrication costs, due to expensive and small wafers and the poor reliability are not attractive for high volume applications. Moreover, due to their high thermal resistance, the integration level is much lower than for silicon. The power handling capability on Si is respectively 3.5 and 2.7 times as large as that on GaAs and InP substrates [16]. These arguments make silicon, even with lower performances, the favorable technology for large scale applications. High performance SiGe HBTs integrated in a BiCMOS technology seem to be a promising solution.

The acronym HBT stands for Heterostructure Bipolar Transistor, since in these devices one or both junctions are formed between dissimilar semiconductor materials, differently than the classical silicon based bipolar transistor, in which we talk about homojunctions (e.g. the junctions are formed by similar semiconductor materials). In fact, the silicon (Si) and the germanium (Ge) have different energy band-gaps ( $E_g$ ) between the conduction and the valence band ( $E_{g,Si}=1.12\text{eV}$  and  $E_{g,Ge}=0.66\text{eV}$  at 300K). For this reason, the  $\text{Si}_x\text{Ge}_{1-x}$  alloy has a smaller  $E_g$  than pure Si, which can be adjusted by tuning the percentage of Ge. The effect of this band-gap engineering is to ensure a high current gain ( $\beta$ ), while at the same time maintaining a high base doping [17], which in turn yields a

reduced base resistance and therefore improved high-frequency characteristics, needed to design performing RF circuits.

Thanks to these technological innovations, SiGe HBTs provide a higher current and voltage driving capability, higher linearity, larger transconductance ( $g_m$ ), lower  $1/f$  noise property, excellent reliability, better device matching and superior performance in comparison to standard silicon metal oxide semiconductor field effect transistors (MOSFETs). This makes them ideal devices for microwave power applications [18], [19]. Therefore, several companies have chosen to integrate their high performance SiGe HBTs in a lower cost CMOS process (BiCMOS) which allows an improved functionality, but at the same time increases process complexity, due to the HBT integration.

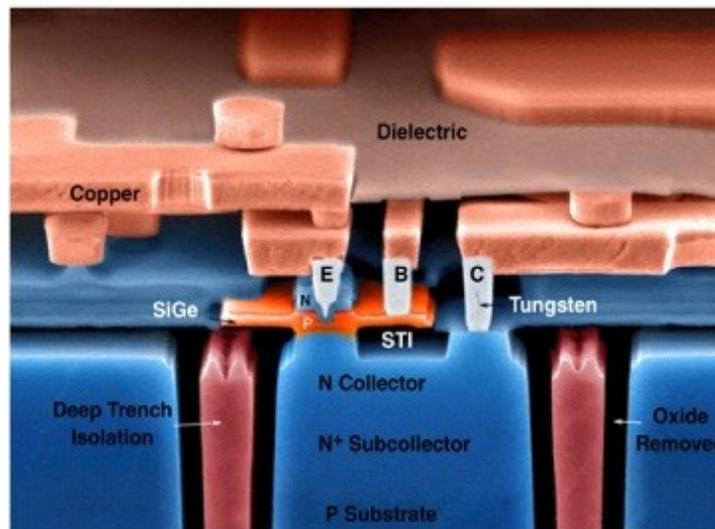


Figure 1.3: SEM cross sectional view of a SiGe HBT. (<http://users.ece.gatech.edu/cressler/>)

Moreover, SiGe HBT technology continues to gain momentum over CMOS process nodes, as shown in Figure 1.4; although the evolution of SiGe has been rather irregular, with missed technology nodes, a clear scaling law exists (as indicated by the trend in blue dashed line), which allows SiGe BiCMOS to retain an advantage of around 2 generations over CMOS in terms of  $f_T$  and  $f_{max}$ .

Optimized device structure along with aggressive scaling lead to comparable performance as III-V devices ( $f_T=300\text{GHz}$ ,  $f_{max}=500\text{GHz}$  [20]). The Seventh Framework Programme project DOTSEVEN has reached the development of SiGe:C HBTs technologies with cut off frequencies  $f_{max}$  of around 700GHz. This continuous improvement of the device performances allows the design of circuits for RF applications having outstanding performances. A power density of  $18.5\text{mW}/\mu\text{m}^2$  at 1dB compression was obtained at 94GHz in [21], which can be attractive for designing power amplifiers in W-band. In [22] a record gate delay of 1.65ps is demonstrated, which represents a record for a bipolar transistor based technologies. In [23] an 820GHz transceiver chipset for terahertz active imaging applications was fabricated using IHP technology. This scenario opens the doors for terahertz (THz) applications [24] that can be mass-produced in a cost-effective way.

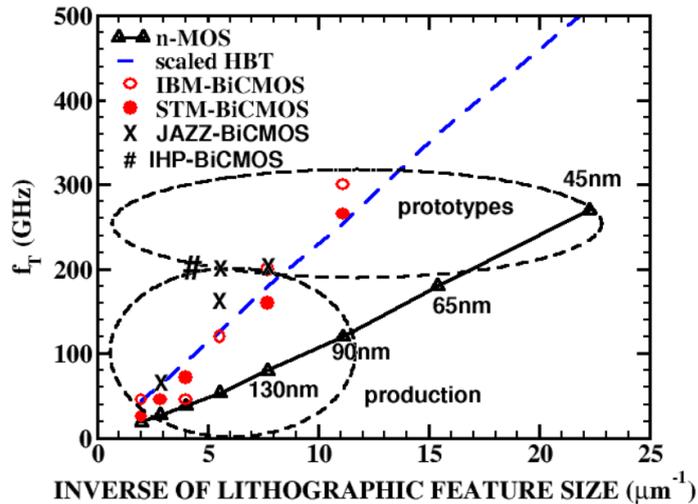


Figure 1.4: SiGe BiCMOS technology evolution over the inverse of the technology feature size. Comparison with CMOS technology trend [24]

### 1.3 Thermal issues in SiGe technologies

In advanced SiGe technologies, higher device performances are mainly achieved with downscaling of device dimensions and by improving the device architecture [25]–[27]. The higher is the speed of advanced HBTs, the higher are their current densities and internal electric fields, which lead to a continuous increase of the power dissipation per unit area [28]. In these technologies, structural innovation has contributed to reduce the parasitic elements and to decrease the transit time by introducing shallow trench, deep trench, and other technological process steps [29]. The key improvements, (which can have a strong impact on the electro-thermal behavior of the HBTs) are: (i) the introduction of the deep-trench isolation (DTI), which surrounds the whole device, thus helping to reduce the parasitic capacitances (see Figure 1.5); the drawback is that the DTI is mainly made of silicon dioxide ( $\text{SiO}_2$ ) having a very poor thermal conductivity and so its presence restricts the heat flow, resulting in larger thermal impedances  $Z_{\text{th}}$  [30]–[32]. (ii) In order to boost the transit frequency  $f_T$ , a lot of attention is paid to carefully design the base-collector (BC) junction and the epitaxial collector. This permits to push the Kirk effect to higher current densities, leading to higher  $f_T$  on the one hand, but on the other hand, it shifts the operating point to higher current densities [33] and thus to higher values of power dissipation. Both (i) and (ii) aspects result in a more pronounced self-heating effect, leading to higher device operating temperatures, which affect the circuit performances, the reliability and the packaging costs.

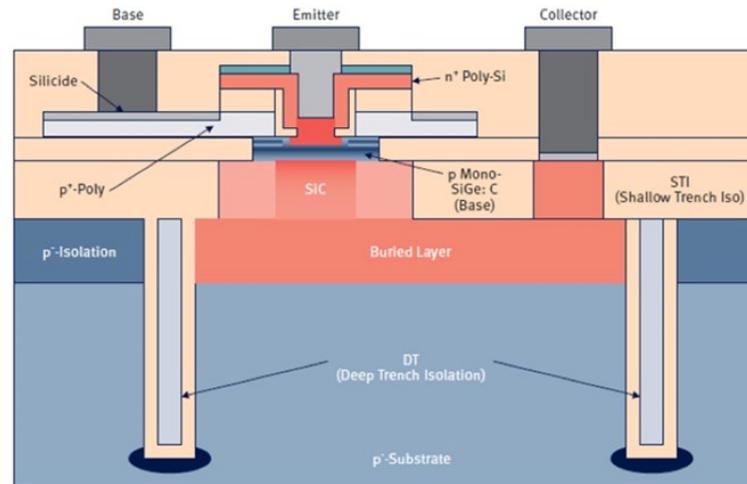


Figure 1.5: cross section of a SiGe HBT realized in the B7HF200 technology

In conventional approaches for the study of thermal phenomena arising in state of the art SiGe HBTs, it is assumed that the main part of the power dissipation occurs at the base-collector space charge region, due to the intense electric fields and the high current densities which are present in this region of the device [34]. In Figure 1.6 it is depicted the distributed power density obtained from simulation using a 2-D hydrodynamic model [34].

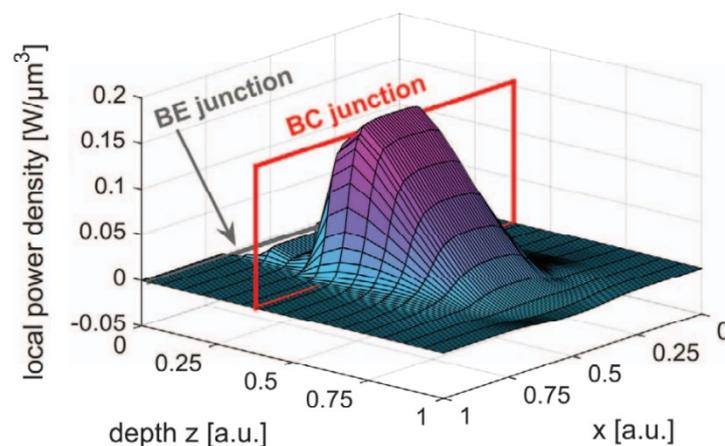


Figure 1.6: local power density dissipated in correspondence of the BC space charge region for a HBT in Infineon Technology (effective emitter area  $0.13 \times 2.73 \mu\text{m}^2$ ). The results are obtained from 2-D hydrodynamic model simulation [27].

Due to the complex architecture of state of the art components, which make use of doped materials, passivation layers and metallization, having very different thermal properties, the study and modelling of the thermal diffusion mechanism within the transistor is a challenging topic of increasing interest. In Figure 1.7 is shown the temperature profile simulated in Sentaurus TCAD for a five fingers transistor in ST B55 technology, when planar heat sources are considered at the BC junctions: it is clear how the presence of

## Chapter 1

### General introduction

different materials within the HBT yields thermal gradients; these temperature profiles propagate in different ways, according to the thermal conductivity of the different materials and thus an estimation of the temperature reached by the transistor requires a deep insight into the physics and the geometry of the component.

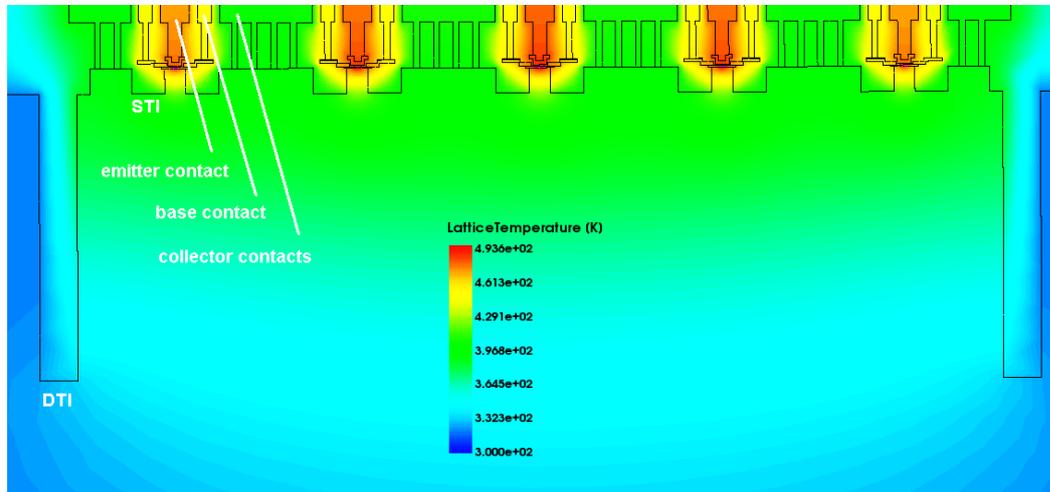


Figure 1.7: temperature profile simulated in Sentaurus TCAD for a five fingers SiGe HBT realized in ST B55 technology. The five heat sources are placed at the BC junction and the 3D transistor structure contains the different layers till the contacts at metal-1 level.

The determination of the temperature reached by the transistor is mandatory from a modelling point of view, since it impacts in a considerable way its electric behavior. When an HBT handles high levels of power dissipation, thermal instabilities can occur due to the positive feedback between the collector current and the device temperature [35], [36]. In fact, HBTs can be considered unconditionally stable when driven by a constant base current, but when biased with a constant base emitter voltage, the device shows a positive electro-thermal feedback; in this situation, in fact, the self-heating causes an increase of the collector current, which will determine an increase of the power dissipation, thus creating a positive feedback loop. This situation can cause the onset of the flyback behavior in the output characteristics, thus limiting the safe operating area (SOA) of the transistor in the region at high currents [37].

To mitigate the negative effects of self-heating, multifinger architectures can be used, which can have an increased power handling capability. These devices consist of multiple transistors in parallel, placed within the same DTI (as visible in Figure 1.7). Due to the close proximity of the different fingers, thermal coupling can cause the central emitter to reach the highest temperature and thus drive more current than the other emitters, starting the thermal instability mechanisms. This situation can lead to an uneven distribution of the currents among the different emitters, till reaching the situation where one finger tends to conduct the whole current (current hogging effect) [38], [39]. This unwanted focalization of the current in a single finger can lead to the generation of hot spots within the transistor and may eventually cause the device failure.

To overcome these thermal instabilities, properly designed ballasting resistors can be added at the emitter nodes and can limit the rapid current increase and the current hogging phenomenon [40], [41].

## 1.4 This work

### 1.4.1 Motivation

As underlined in the previous section, the thermal issue is one of the key factors limiting the performance and reliability of the devices and integrated circuits realized in SiGe technology.

For instance, it has been discussed how SiGe HBTs realized in multifinger architecture can suffer from thermal instabilities due to current hogging effect, which can eventually lead to device failure; one of the possible approaches to improve the thermal stability in these components, is to use ballasting resistors [41], [42], but this solution leads to degradation of the output power and of the power-added efficiency (PAE) of the transistor, so alternative transistor topologies can be helpful to extend the safe operating limits of the transistor without any loss in performance.

In general, due to the strong relationship between electrical and thermal effects in SiGe HBTs, an efficient characterization of the device is essential, in order to generate trustable compact models and thus allow precise electrical simulations for circuit designers. Consequently, a realistic modeling must provide an electrical representation, but also a precise and physics based reproduction of the thermal characteristics of the HBTs, which can be also helpful for thermal stability and reliability analysis. Besides, due to the intrinsic nonlinearity of the transistor, third-order intermodulation products, generated near its thermal time constant, can trigger low frequency variations of the junction temperature, which can affect the electrical behavior of the component [43], so a precise characterization of the thermal impedance is necessary and can help in the design of predistortion linearizers [44]. It must be taken into account, though, that external parasitic elements, like the metallization in the BEOL, can impact to a considerable extent the thermal impedance of the transistor [45] and so its impact should be analyzed and modeled.

Thermal interactions can take place not only at device level; in fact, transistors that are placed in close proximity can experience mutual thermal coupling [46], [47]. These effects have to be characterized to provide more accurate electrical simulations during the circuit design phase.

## *Chapter 1*

General introduction

### *1.4.2 Organization*

This thesis work is organized as follows:

#### *Chapter 2*

This chapter will be focused on the description of the measurement techniques adopted for the characterization of self-heating related effects in state of the art SiGe HBT technologies. The methodologies to extract the  $R_{th}$  and  $C_{th}$  are presented and the impact of thermal memory effect is discussed, with large signal two tones simulations, showing also the limitations in the use of a single pole thermal network.

#### *Chapter 3*

In this chapter it is presented an analysis of the impact of the BEOL on the electrical and thermal properties of a state-of-the-art SiGe HBT technology from Infineon (B11HFC); dedicated transistor structures are designed and the results of a complete DC and RF electrical characterization at small and large signal, as well as a thermal characterization are reported. A compact model is also proposed, to take into account the impact of the BEOL metallization on the thermal impedance and is validated with dedicated measurements in the time and frequency domain. Finally the variation of the thermal behavior with the doping concentration is analyzed by means of TCAD simulations and is compared to the experimental data obtained from measurements.

#### *Chapter 4*

In this chapter a set of alternative transistor topologies is presented, which can ensure an improved electro-thermal behavior and better SOA specifications; the test structures contain a multifinger HBT from the ST Microelectronics B55 process. The different methodologies proposed to yield better performances are: (i) exploiting the metal dummies in the BEOL, (ii) modifying the layout of the drawn emitter window, (iii) increasing the DTI enclosed area. For all the proposed test structures a complete DC and AC characterization, as well as an extraction of the  $R_{th}$  and  $Z_{th}$  is proposed.

#### *Chapter 5*

This chapter will focus on the mutual thermal coupling in multi-finger transistors in dynamic operation. A physics based approach is proposed to study and model the thermal coupling effect between the different emitter fingers and is validated upon TCAD simulations and dedicated on-wafer pulsed measurements. Then, with the help of TCAD simulations, the impact of the BEOL on the thermal dynamics has been analyzed, and a new method to evaluate the thermal coupling coefficients under the real operating conditions of the transistor is proposed.

*Chapter 6*

This chapter is dedicated to the study of thermal interactions at circuit level in different circuit topologies. The impact of thermal coupling is modeled for a differential pair and two versions of a cascode amplifier, in which different distances among the transistors are used. The calibrated thermal coupling model is used to simulate the impact of distance in a two stages Darlington amplifier. Moreover the  $R_{th}$  variation caused by the BEOL is modeled and its impact at circuit level is estimated for the VM multifinger transistors presented in Chapter 4.

## Chapter 2

# Device characterization in SiGe HBT technologies

### 2.1 Introduction

As already presented in Chapter 1, state of the art SiGe technologies are affected by serious thermal issues that can degrade the performances of the active components and eventually lead to their failure. A deep insight into the mechanisms of heat generation and diffusion at device level, as well as an accurate characterization and modelling of these phenomena is mandatory in order to allow a realistic circuit simulation during the design phase, but also to improve the performances and push the limits of a given technology.

This chapter will be focused on the description of the measurement techniques adopted for the characterization of self-heating related effects in state of the art SiGe HBT technologies. First the effect of self-heating on the electrical behavior of the transistor is shown by means of simulations for state of the art technology, secondly an overview of the methodologies to extract the static and dynamic thermal properties of the transistors is presented and finally the impact of thermal memory effect is discussed, with large signal two tones simulations, showing also the limitations in the use of a single pole thermal network.

### 2.2 Compact modeling: the HiCuM model

The main goal of compact modeling is to enable circuit design. A compact model should be a physics-based mathematical description of the electrical behavior of a device for use in a circuit simulator. There is a large demand for fast and reliable compact models that are accurate for a great variety of technologies. A trustable compact model provides high accuracy over a wide electrical (and temperature) range, geometrically scalable parameter calculation, numerical stability and fast execution time.

A compact model determines the specific electrical behavior of the component, while meeting the criteria of robustness, convergence of the simulator and simulation time. It is the key element on which the circuit designer can relay and, therefore, the model should provide an accurate picture of physical phenomenon that may affect the behavior of a circuit in the useful operating area of the transistor. Nowadays the main models for silicon-based bipolar transistors are: Gummel-Poon (SGP), VBIC, MEXTRAM, and HiCuM, which are physics based models.

In this work the HiCuM/L2 model is considered for all the electrical device simulations, which represents the most widespread model for the design of circuits using SiGe HBTs.

The HiCuM (High-Current Model) [48] is a scalable physics-based compact model for bipolar transistors, taking into account the high current effects which are significant for

certain high speed transistor applications. The first version was introduced in 1986 by H.M. Rein and M. Schröter and it is now a Compact Model Council (CMC) standard model [49] and integrated in a wide range of simulators like ADS, ELDO, SPECTRE, HSPICE, GoldenGate, etc. HiCuM is based on an extended and generalized integral charge-control relation (GICCR). However, in contrast to the (original) Gummel-Poon model, in HiCuM the GICCR concept is applied without simplifications and additional fitting parameters (such as the Early voltages). Therefore it allows a reliable design and circuit optimization.

The HiCuM large signal equivalent circuit is shown in Figure 2.1. The internal transistor has the four nodes  $E'$ ,  $B'$ ,  $B^*$  and  $C'$ . The internal circuit consists of the diode current  $i_{jBEi}$  and the depletion charge  $Q_{jEi}$  of the base-emitter (BE) junction, the diode current  $i_{jBCi}$  and the depletion charge  $Q_{jCi}$  of the base-collector (BC) junction, and the voltage controlled transfer current source  $i_T$ . Furthermore, the minority charge is represented by its forward and reverse component,  $Q_f$  and  $Q_r$ . In addition, breakdown in the BC space charge region is taken into account by the avalanche current source,  $i_{AVL}$ , and possible tunneling through the BE space charge region is represented by  $i_{BEti}$ . By comparing with the equivalent circuit of SGP, there are two additional nodes named  $B^*$  and  $S'$  in HiCuM. The node  $B^*$  has been added to separate the internal base resistance  $r_{Bi}$  (bias dependent) from the external component  $r_{Bx}$ . The internal substrate node  $S'$  is connected to the substrate network with the capacitance  $C_{Su}$  and the resistance  $r_{Su}$ . Moreover, an emitter-base isolation capacitance  $C_{BEpar}$  as well as a base-collector oxide capacitance  $C_{BCpar}$  is taken into account. More information about this compact model can be found in [48].

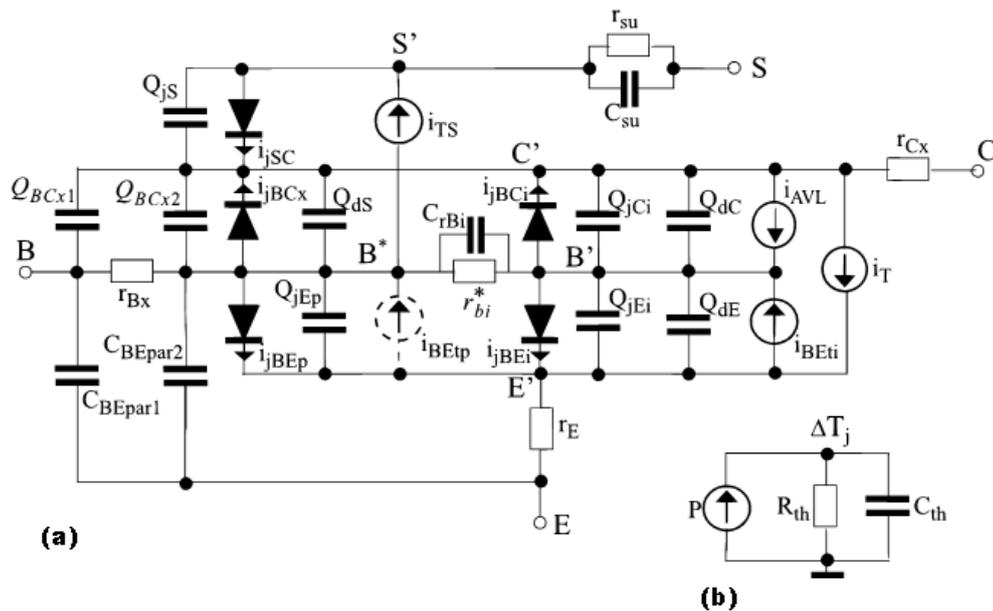


Figure 2.1: (a) Large-signal HICUM/L2 equivalent circuit. (b) Thermal network used for self-heating calculation (figure taken from [44]).

### 2.3 Modeling of device self-heating in compact simulators

Heat is generated in all active areas of a device which results in an increase of the device temperature. Self-heating leads to a shift in device characteristics and can be described with an equivalent electrical circuit. In fact, as shown in Figure 2.1, in the HiCuM/L2 compact model, a dedicated sub-circuit allows the calculation of the increase of the junction temperature ( $\Delta T_j$ ); it consists of one thermal resistance  $R_{th}$  and one thermal capacitance  $C_{th}$  in parallel, forming a single-pole circuit, which represents the simplest form of model for calculating the junction temperature evolution. The units for  $R_{th}$  and  $C_{th}$  are K/W and Ws/K, respectively. The voltage node in the thermal equivalent network corresponds to the temperature rise  $\Delta T$  experienced by the transistor:

$$\Delta T = T_j - T_{amb} = P_{diss} R_{th} \quad \text{Eq. 2.1}$$

where  $T_j$  and  $T_{amb}$  are the junction and ambient temperatures respectively. The current source corresponds to the dissipated power  $P_{diss}$  and represents the amount of heat that is generated by the device. In HiCuM/L2 the flag FLSH allows three different approximations for the calculation of  $P_{diss}$  [48]:

- If FLSH=0 the self-heating effect is not taken into account and the device temperature is constantly equal to the ambient temperature  $T_{amb}$
- If FLSH=1, only the most relevant dissipative elements are considered for the calculation of  $P_{diss}$ , as follows:

$$P_{diss} = |I_T V_{C'E'}| + |I_{AVL} V_{B'C'}| \quad \text{Eq. 2.2}$$

- If FLSH=2,  $P_{diss}$  is calculated from all relevant dissipative elements in the equivalent circuit:

$$P_{diss} = |I_T V_{C'E'}| + |I_{AVL} V_{B'C'}| + \sum \frac{|\Delta V_n^2|}{R_n} + |I_{TS} V_{B^*S}| \quad \text{Eq. 2.3}$$

with  $R_n = \{r_{Bi}, r_{Bx}, r_E, r_{Cx}\}$  as non-zero series resistances and  $\Delta V_n$  as the corresponding voltage drop across those resistances.

The thermal network and the electrical part of the transistor model are solved together for each DC and transient operation. The temperature dependent model parameters are calculated using the voltage at the temperature node. Furthermore (if the internal  $R_{th}$  and  $C_{th}$  are deactivated), the thermal node can be connected to more complex external thermal networks, in order to allow a more accurate simulations of specific thermal phenomena. For instance this option is later used in this work to consider the heat flow in the metallization upon the transistor or to account for intra-device thermal coupling within multifinger HBTs or to simulate inter-device thermal interactions at circuit level.

## 2.4 Self-heating effect on the device DC and AC characteristics

A detailed description of the different regions of operation of SiGe HBTs can be widely find in literature [17], [48], [50] and is not reported here. The attention will be focused on how the self-heating affects the electrical behavior.

Measurements for device characterization are normally conducted on-wafer, thanks to the use of automatic or manual probe stations; the transistor test structures are normally realized in common emitter configuration (a GSG arrangement for the pads is preferred to avoid possible oscillations and allow RF measurements): the base and the collector are connected to the source and monitor units (SMU) of a semiconductor parameter analyzer, which applies and measures voltages and currents directly on the transistor (see Figure 2.2). The parameter analyzer is connected via GPIB to a PC, and the desired voltage or current sweeps are controlled from a user interface allowing to collect and handle the measured data.

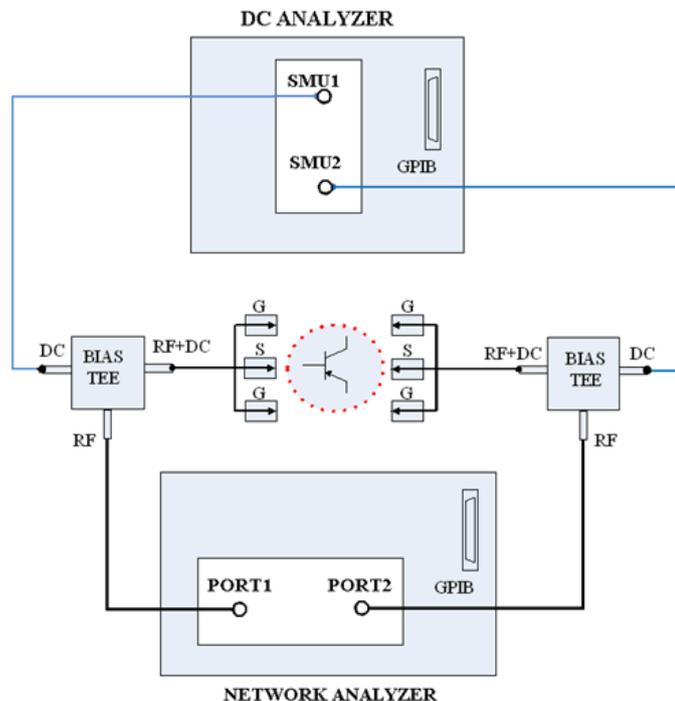


Figure 2.2: block diagram showing a typical measurement setup for the DC and AC characterization of active components on-wafer

The measurement of the  $I(V)$  current-voltage relationships is the most basic form for a DC characterization of the transistors: in Figure 2.3 (on the right) is reported the Gummel plot measured on a HBT realized in the Infineon B11HFC process ( $W_{EX}L_E=0.22 \times 5 \mu\text{m}^2$ ) for  $V_{CE}=1.5\text{V}$  when the transistor is driven by a constant  $V_{BE}$ . In this biasing condition the collector current  $I_C$  increases with increasing temperature [36]; since the temperature reached by the component  $T_j$  is directly proportional to the power dissipated  $P_{\text{diss}}$  (according to Eq. 2.1) and the  $P_{\text{diss}}$  is proportional to current flowing into the device

(following Eq. 2.2 or Eq. 2.3), it results that for this biasing condition, the  $I_C$  will experience an uncontrolled increase, as the  $P_{\text{diss}}$  increases (thermal runaway) [38], which can eventually lead to instability and device failure. In Figure 2.3 the measurements are also compared to the results from simulation using the HiCuM/L2 compact model, using a model card that has an  $R_{\text{th}}$  value of 3600K/W (red line). Two additional simulation results are added, using two lower values of the thermal resistance  $R_{\text{th}}$ : 3100K/W and 2600K/W, in order to evaluate the differences that can be expected in the electrical characteristics when the effects of self-heating are lower. It can be seen that, from around 850mV on and as the  $R_{\text{th}}$  is set to a smaller value, the simulated  $I_B$  decreases, whereas for what concerns the simulated  $I_C$ , the region where the maximum deviation is obtained is for  $V_{\text{BE}}=925\text{mV}$ . This can appear strange, since observing the temperature increase predicted by the compact model, (on the right in Figure 2.3) it is clear that the temperature difference among the 3 different model cards continues to increase for  $V_{\text{BE}}>925\text{mV}$ . It must be taken into account, in fact, that for higher values of  $V_{\text{BE}}$ , the increase of  $I_C$  is caused by a combination of other effects (mainly impact ionization and avalanche multiplication, and in particular the feedback role played by the emitter resistance) rather than solely by self-heating and thus the difference among the  $I_C$  obtained for the three  $R_{\text{th}}$  considered starts to decrease.

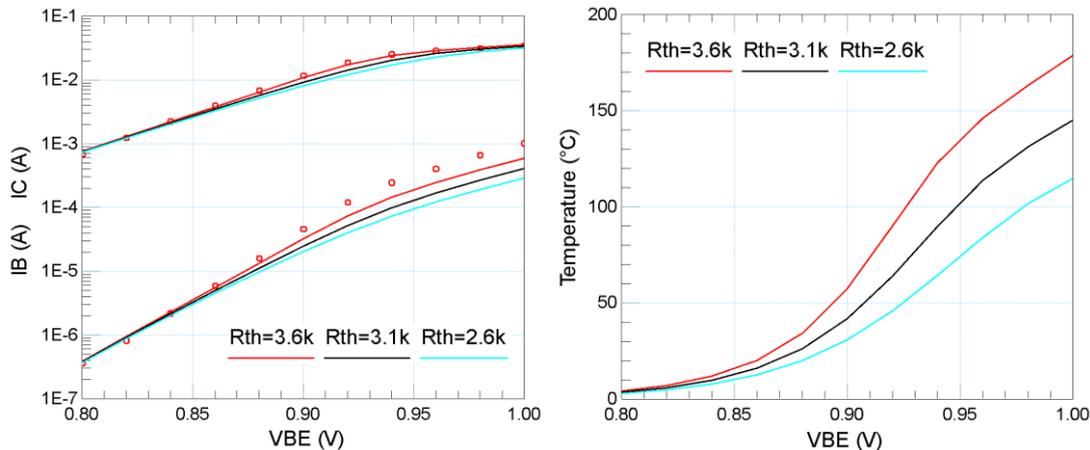


Figure 2.3: (left) forward Gummel plot at constant  $V_{\text{CE}}=1.5\text{V}$  for an Infineon B11HFC CBEB C HBT with  $A_{\text{E}}=0.22\times 5\mu\text{m}^2$ : comparison between measurements (symbols) and compact model simulations (solid lines) for different values of the  $R_{\text{th}}$ . (right) corresponding temperature increase simulated in HiCuM

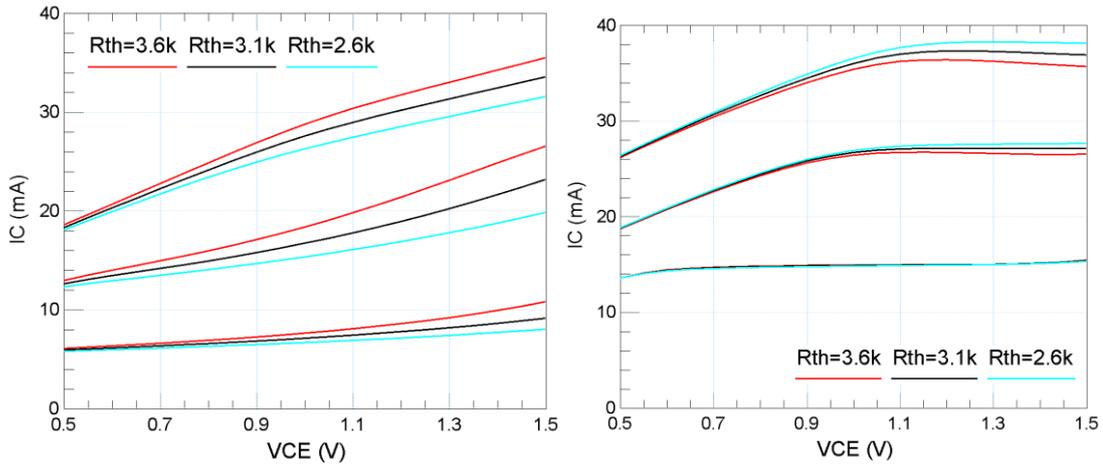


Figure 2.4: simulated output curves for an Infineon B11HFC CBEBC HBT with  $A_E=0.22 \times 5 \mu\text{m}^2$ : (left) the forced  $V_{BE}$  ranges from 0.9V to 1V; (right) the forced  $I_B$  ranges from  $60 \mu\text{A}$  to  $600 \mu\text{A}$ . Different values of the  $R_{th}$  are used in compact model simulations.

The effect of the positive electro-thermal feedback when forcing the device at constant  $V_{BE}$  is also visible on the output curves in Figure 2.4 (left), and the same considerations made for the Gummel plot still hold: among the different  $R_{th}$  considered, the bias condition at which the highest variation of  $I_C$  is observed is for  $V_{BE}=900\text{mV}$ ; in fact for  $V_{BE}=850\text{mV}$  the self-heating effects are less evident, since the temperature reached by the component is lower, whereas for  $V_{BE}=950\text{mV}$  the increase of  $I_C$  is caused by a combination of other effects, as previously discussed and thus the difference among the results obtained for the three  $R_{th}$  considered is lower.

On the right in Figure 2.4 another situation is presented, corresponding to the case where the transistor is driven by a current injected in the base terminal; in this scenario, instead, the self-heating causes the  $I_C$  current to drop when the high power dissipation region is reached and so the device is intrinsically stable.

For what concerns the AC characterization, one of the main figures of merit that is used for comparing the performances of a given transistor is the unity gain cut-off frequency ( $f_T$ ), which is defined as the frequency where the extrapolated small-signal current gain  $\beta_F$  equals one (Figure 2.5):

$$|\beta_F(f = f_T)| = \left. \frac{dI_C(f_T)}{dI_B(f_T)} \right|_{V_{CE}} = |H_{21}(f_T)| = 1 \quad \text{Eq. 2.4}$$

$$f_T = f_{meas} |H_{21}(f_{meas})| = \frac{f_{meas}}{\Im(Y_{11}/Y_{21})} \quad \text{Eq. 2.5}$$

where  $f_{meas}$  has to be chosen as a frequency at which  $\beta_F$  is rolling-off at a slope of  $-20\text{dB/dec}$ , whereas in Eq. 2.5 are reported two possible expressions to extract  $f_T$ . Another commonly used figure of merit is the  $f_{max}$ , defined as the frequency at which the unilateral power gain  $U$  (or Mason's invariant gain) becomes unity (Figure 2.5).

$$|U(f = f_{\max})| = \frac{|Y_{21} - Y_{12}|}{4(\Re(Y_{11})\Re(Y_{22}) - \Re(Y_{12})\Re(Y_{21}))} = 1 \quad \text{Eq. 2.6}$$

$$f_{\max} = f_{\text{meas}} \sqrt{|U(f_{\text{meas}})|} \quad \text{Eq. 2.7}$$

Eq. 2.7 is a commonly used expression to extract  $f_{\max}$  based on the definition of  $U$ .

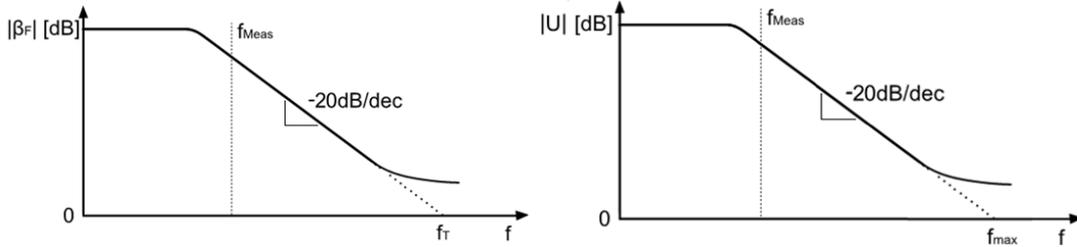


Figure 2.5: illustration of the small-signal current gain  $\beta_F$  (left) and Mason's gain (right) vs. frequency; the  $f_T$  and  $f_{\max}$  are extrapolated as the frequencies at which  $\beta_F$  and  $U$  respectively reach 0dB.

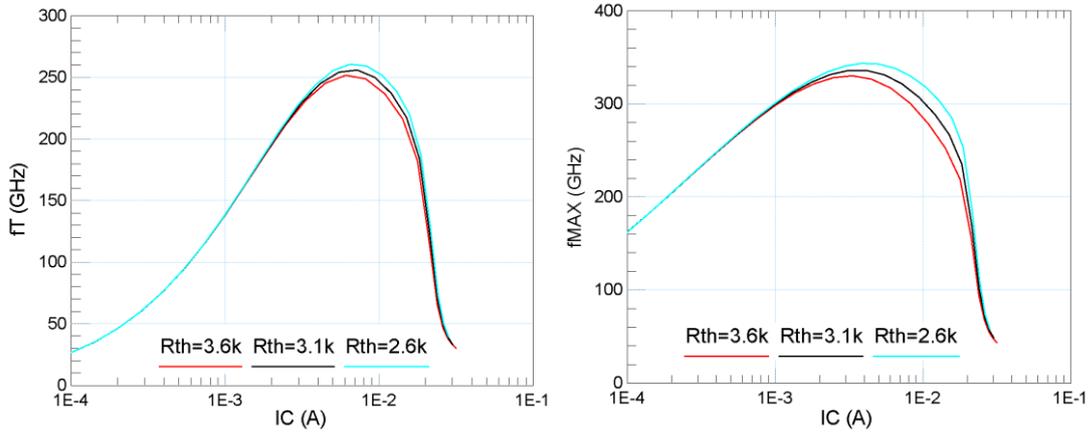


Figure 2.6: simulated  $f_T$  (left) and  $f_{\max}$  (right) plotted versus  $I_C$  for a constant  $V_{CE}$  of 1.5V; different values of  $R_{th}$  are used in compact model simulations.

In Figure 2.6 are shown the simulated  $f_T$  and  $f_{\max}$  as function of the  $I_C$  for the same transistor and the same values of  $R_{th}$  discussed above; it can be noticed that varying the  $R_{th}$  (and thus changing the amount of self-heating effect within the transistor) impacts the  $f_T$  and  $f_{\max}$  in the region around the peak and after (more precisely, in the  $I_C$  range that has been observed to vary with the  $R_{th}$  in Figure 2.3).

## 2.5 Extraction of the $R_{th}$

The extraction of the  $R_{th}$  is one of the long lasting challenges encountered for device characterization and several different methodologies have been proposed in literature in the last years [51]–[55]. In general, these methods consist in performing measurements at different chuck temperatures, in order to determine the thermal dependence of the electrical parameter which will be used as thermometer.

The  $R_{th}$  extraction procedure used in this work is based on the theory given in [52] and the necessary steps are reported for the case of a five fingers transistor realized in ST Microelectronics B55 process ( $0.18 \times 5 \mu\text{m}^2$ ).

This procedure uses the base-emitter voltage as the temperature sensitive parameter and consists in measuring the  $V_{BE}$  as function of the ambient temperature  $T_{amb}$  for constant collector currents  $I_C$  and different  $V_{CE}$ ; the approach used here is to measure  $I_C$  for swept  $V_{BE}$ , as done for Gummel plots and to determine  $V_{BE}$  as function of  $I_C$  by interpolation. In Figure 2.7 are shown the Gummel plots for different values of  $V_{CE}$  from 1V to 1.24V and for 4 values of the chuck temperature  $T_{chuck}$ , ranging from 300K to 380K. Three different values of  $I_C$  (5mA, 10mA and 20mA) are chosen for the extrapolation, and the related  $V_{BE}$  extracted are then plotted as function of the chuck temperature, as reported in Figure 2.8; this calibration curve shows a very linear relationship between  $V_{BE}$  and  $T_{chuck}$ .

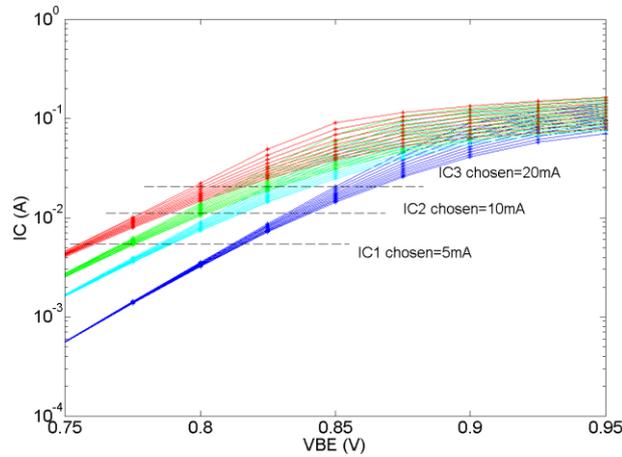


Figure 2.7: Gummel plot measured on a five fingers HBT in ST B55 technology; the  $V_{CE}$  ranges from 1V to 1.24V. The measurements are performed at different chuck temperature ranging from 300K (blue) to 380K (red). The values of  $I_C$  chosen for the  $R_{th}$  extraction are also shown.

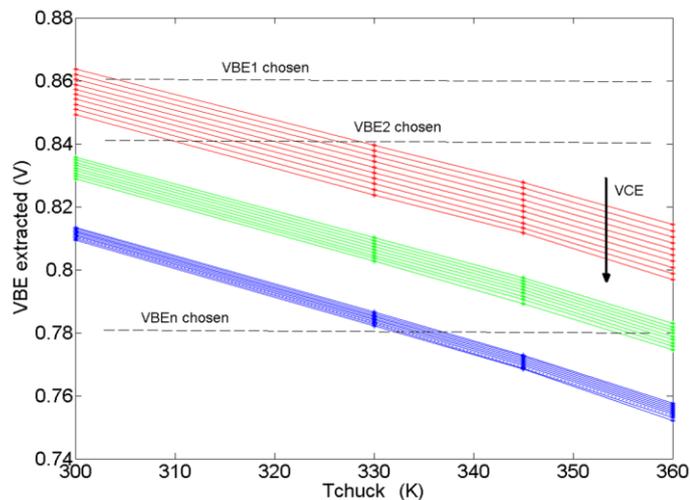


Figure 2.8:  $V_{BE}$  values extracted from the Gummel plot for the 3 values of  $I_C$  fixed (blue=5mA, green=10mA, red=20mA). The  $V_{BE}$  are plotted versus  $T_{chuck}$  for the different values of  $V_{CE}$  considered. The values of  $V_{BE}$  fixed to extract the corresponding  $T_{chuck}$  are also shown in the plot

As can be seen in Figure 2.8, for small values of  $I_C$  (e.g. at  $I_C$  chosen=5mA colored in blue), where the power dissipation and the thus self-heating is negligible, the extracted  $V_{BE}$  does not vary too much for the different  $V_{CE}$  values considered. However, if  $I_C$  is increased to 20mA (red curves), we observe that the  $V_{BE}$  values extracted start to vary if  $V_{CE}$  is swept; for this value of current,  $P_{diss}$  is significantly higher, and thus self-heating can be considered responsible for the change of  $V_{BE}$  with  $V_{CE}$  varying. Next, different values of  $V_{BE}$  (from  $V_{BE1}$  to  $V_{BE_n}$ ) are chosen and the corresponding  $T_{chuck}$  are extracted by interpolation. These points correspond to the determination of the ambient temperature for which the transistor exhibits a certain  $V_{BE}$  (which has been chosen) at an  $I_C$  of 20mA. These chuck temperatures are now plotted versus their corresponding dissipated power dissipation (which is approximated here as  $P_{diss}=I_C V_{CE}$ ).

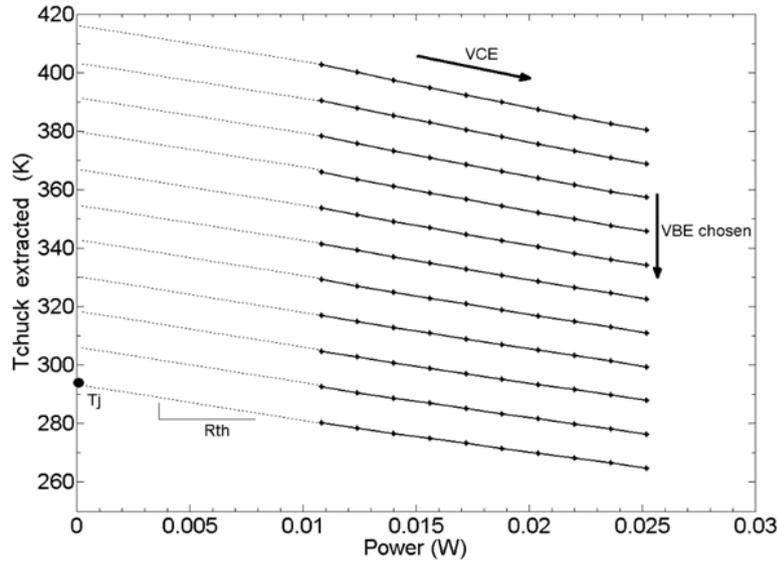


Figure 2.9: chuck temperatures extracted for the values of  $V_{BE}$  which have been fixed, plotted as function of the corresponding  $P_{diss}$ . This plot allows to extract, for each  $V_{BE}$  fixed, the corresponding values of the  $T_j$  and  $R_{th}$

Since the junction temperature  $T_j$  can be expressed as the sum of the ambient temperature and the temperature increase in the device caused by self-heating:

$$T_j = R_{th} P_{diss} + T_{chuck} \quad \text{Eq. 2.8}$$

it follows that  $T_j$  can be determined by extrapolation of the  $T_{chuck}$  at  $P_{diss}=0$ , as marked in Figure 2.9; moreover the  $R_{th}$  can be estimated as the slope of the  $T_{chuck}(P_{diss})$  curve. Repeating this procedure for all the values of  $V_{BE}$  which have been fixed leads to the results in Figure 2.10 (left), which represent the extracted  $R_{th}$  as function of the junction temperature  $T_j$ .

Since the  $T_j$  is extracted at fixed  $I_C$ , for every values of  $V_{BE}$ , the  $dV_{BE}/dT_j$  can be also determined using this technique (Figure 2.10 (left)); this parameter characterizes the technology and does not depend on the transistor layout.

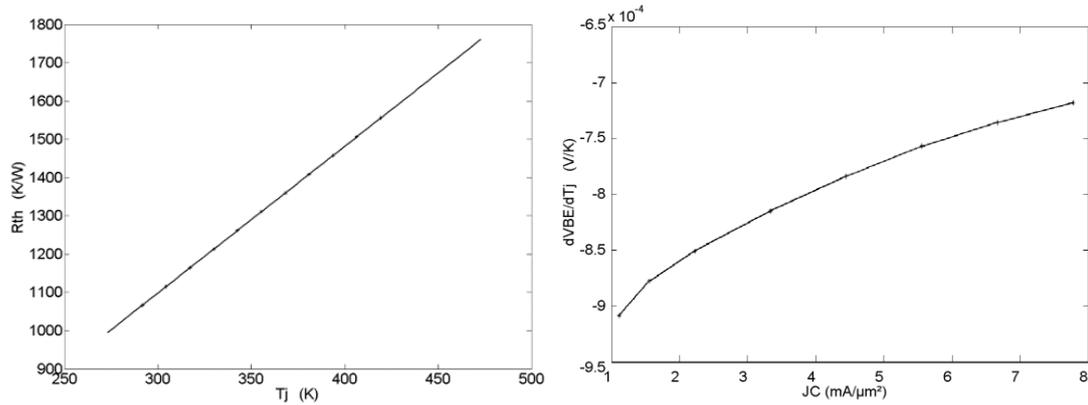


Figure 2.10: (left)  $R_{th}$  extracted as function of the  $T_j$  using the method described. (right)  $dV_{BE}/dT_j$  measured for the ST B55 technology.

## 2.6 Extraction of the $Z_{th}$

The characterization of dynamic electro-thermal self-heating inside SiGe HBTs remains an essential task for model developers in order to determine the device operating temperature in practical applications where a signal having a certain frequency bandwidth is fed at the input of the transistor. The dynamic behavior can be described by the thermal impedance  $Z_{th}$  which can be seen as the parallel of  $R_{th}$  and  $C_{th}$  in the thermal subcircuit in Figure 2.1b.

The device thermal response ranges from about few kilohertz to about 200MHz in SiGe HBTs [56], hence,  $Z_{th}$  is limited to low frequencies where it can be extracted. Low frequency S-parameter measurements are suitable since it is a relatively simple and precise measurement procedure. Several approaches have been presented in literature to provide an expression to determine the  $Z_{th}$  from dedicated measurements at low frequency. For example, generalized formulations for thermal impedance from  $y$ -parameters are proposed by Rinaldi [57] through a rigorous mathematical treatment. Also dynamic characterization of thermal effect, based on  $h$ -parameters has been proposed in [58], [59]. The dispersive phenomenon presented by the device at low frequencies is caused by dynamic self-heating effects: performing S-parameter measurements it is possible to observe a certain deviation of the  $S_{12}$  and  $S_{22}$  in the low frequency range; in Figure 2.11 (left) are reported the magnitude of the S-parameters measured in the frequency range 10kHz-3GHz for the bias point  $V_{BE}=0.9V$  and  $V_{CE}=1.25V$  at which a significant amount of self-heating can be expected. The measurements are performed on the low-frequency vector network analyzer (VNA) Agilent E5061B (5Hz-3GHz), making use of bias tees particularly developed to cover this specific frequency range. The VNA was calibrated on-wafer using SOLT method. The measured results were de-embedded using Open and Short test structures.

The measurements refer to a five fingers HBT fabricated in ST Microelectronics B55 technology ( $0.18 \times 5 \mu\text{m}^2$ ): it is possible to notice that the  $S_{12}$  and  $S_{22}$  exhibit the largest variation among the four S-parameters. If we analyze these parameters for different bias conditions, it is possible to identify the frequency range where dynamic self-heating affects is predominant; in Figure 2.11 (right) are plotted the  $S_{12}$  and  $S_{22}$  for different  $V_{BE}$  ranging from 0.75V to 0.9V: it is shown that as  $V_{BE}$  increases (and thus self-heating becomes more pronounced) it is possible to identify the frequency range till around 200MHz as the region where the S-parameters start to deviate. At these low frequencies, in fact, the junction temperature is able to follow the variations of power dissipation, thus affecting the S-parameters, whereas at higher frequencies, the junction temperature is not able to follow the evolution of power dissipation and thus just DC self-heating occurs, as will be also detailed in the next paragraph. The frequency that marks this difference in the thermal behavior will be referred to as thermal cutoff frequency. For the extraction of the  $Z_{th}$  the S-parameters are converted to Y-parameters, as will be described below.

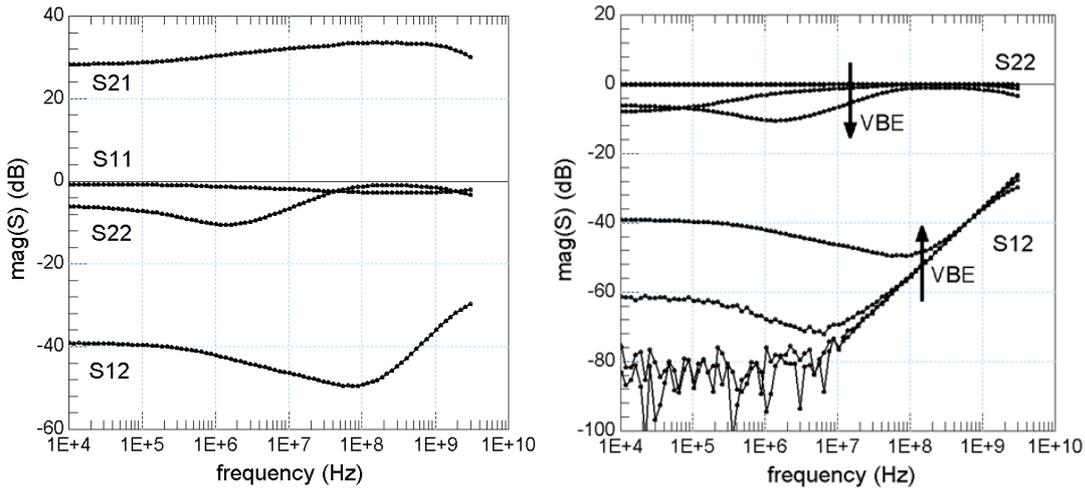


Figure 2.11: (left) measured low frequency S-parameters at  $V_{BE}=0.9\text{V}$  and  $V_{CE}=1.25\text{V}$  for the five fingers HBT from ST B55 technology. (right)  $S_{12}$  and  $S_{22}$  for  $V_{CE}=1.25\text{V}$  and  $V_{BE}$  ranging from 0.75V to 0.9V

### 2.6.1 Theoretical formulation

Collector current  $I_C$  and base current  $I_B$  are functions of the three independent variables: (i) the base-emitter voltage  $V_{BE}$  (ii) the collector-emitter voltage  $V_{CE}$  and (iii) the junction temperature  $T$ . To generalize the following equations  $V_{BE}$ ,  $V_{CE}$ ,  $I_B$  and  $I_C$  are replaced by  $V_1$ ,  $V_2$ ,  $I_1$  and  $I_2$ , respectively:

$$\begin{aligned} I_1 &= f_1(V_1, V_2, T) \\ I_2 &= f_2(V_1, V_2, T) \end{aligned} \quad \text{Eq. 2.9}$$

A linearization valid for small signal excitations at a constant bias condition leads to:

$$\begin{aligned} i_1 &= y_{11}v_1 + y_{12}v_2 \\ i_2 &= y_{21}v_1 + y_{22}v_2 \end{aligned} \quad \text{Eq. 2.10}$$

where each  $y$ -parameter is defined as:

$$y_{mn} = \frac{\partial f_m}{\partial V_n} \quad m = 1; 2 \quad n = 1; 2. \quad \text{Eq. 2.11}$$

Here, index 1 and 2 indicate the base and collector ports, respectively.

The following expression can be written for the  $Y$  parameters [60] (the bar indicates that the parameter is temperature dependent)

$$\bar{y}_{mn} = \left. \frac{dI_m}{dV_n} \right|_{V_m=const.} = \left. \frac{\partial f_m}{\partial V_n} \right|_{V_m, T=const.} + \frac{\partial f_m}{\partial T} \cdot \left. \frac{dT}{dV_n} \right|_{V_m=const.} = y_{mn\_iso} + \frac{\partial f_m}{\partial T} \cdot \left. \frac{dT}{dV_n} \right|_{V_m=const.} \quad \text{Eq. 2.12}$$

where  $y_{mn\_iso}$  is temperature independent. The temperature dependence is approximated for small signal excitations with:

$$\alpha_m = \left. \frac{\partial f_m}{\partial T} \right|_{V_m=const.} \quad \text{Eq. 2.13}$$

where  $\alpha_m$  is the relative change of  $I_m$  per degree temperature change at a constant voltage  $V_m$ . The junction temperature  $T$  is defined as:

$$T = T_{amb} + Z_{th} \cdot P_{diss} \quad \text{Eq. 2.14}$$

where  $T_{amb}$  is the ambient temperature (chuck temperature) and  $P_{diss}$  is the dissipated power in the device that results from

$$P_{diss} = V_1 I_1 + V_2 I_2 \quad \text{Eq. 2.15}$$

The change in dissipated power  $dP_{diss}$  with small signal excitation can be written as:

$$dP_{diss} = dV_1 I_1 + V_1 dI_1 + dV_2 I_2 + V_2 dI_2. \quad \text{Eq. 2.16}$$

From equation Eq. 2.14 and Eq. 2.15 it follows that:

$$\left. \frac{dT}{dV_n} \right|_{V_m=const.} = Z_{th} \left( I_n + V_n \left. \frac{\partial I_n}{\partial V_n} \right|_{V_m=const.} + V_k \left. \frac{\partial I_k}{\partial V_n} \right|_{V_m=const.} \right) \quad k = 3 - n \quad \text{Eq. 2.17}$$

which can be transformed to:

$$\left. \frac{dT}{dV_n} \right|_{\Delta V_m} = Z_{th} \left( I_n + V_n \bar{y}_{nn} + V_k \bar{y}_{kn} \right). \quad \text{Eq. 2.18}$$

Using the equations Eq. 2.12 and Eq. 2.18, the following expression for  $Z_{th}$  is obtained:

$$Z_{th} = \frac{\bar{y}_{nn} - y_{nn\_iso}}{\left( \frac{\partial f_m}{\partial T_j} \right) \left[ I_n + V_n \bar{y}_{nn} + V_k \bar{y}_{kn} \right]} \quad \text{Eq. 2.19}$$

Since in equation Eq. 2.12 the term  $dT/dV_n$  is greater for  $V_2$  ( $V_{CE}$ ) than for  $V_1$  ( $V_{BE}$ ),  $y_{12}$  and  $y_{22}$  are the most affected by self-heating, and therefore, should be the most suitable for the extraction of  $Z_{th}$ . In case of  $y_{22}$ ,  $Z_{th}$  would be:

$$Z_{th} = \frac{\bar{y}_{22} - y_{22\_iso}}{\alpha_2 [I_2 + V_2 \bar{y}_{22} + V_1 \bar{y}_{12}]} = \frac{\bar{y}_{22} - y_{22\_iso}}{\alpha_{IC} [I_C + V_{CE} \bar{y}_{22} + V_{BE} \bar{y}_{12}]} \quad \text{Eq. 2.20}$$

As expressed in Eq. 2.20 it is assumed that the measured Y-parameters contain two parts: one is an isothermal part where only DC self-heating effects are visible and which has been measured at high frequency (above thermal cut-off frequency) and the other is the thermal part (below thermal cut-off frequency) where both dynamic and DC self-heating effects are equally visible.

In Figure 2.12 (left) are plotted the measured  $Y_{22}$  parameters for different values of  $V_{BE}$  ranging from 0.75V to 0.95V and  $V_{CE}=1.25V$ . It can be seen that, as  $V_{BE}$  (and consequently the amount of self-heating) increases, the variation of  $Y_{22}$  at low frequency becomes always higher; in particular the highest deviation is observed at  $V_{BE}=0.9V$ . From Figure 2.12 (left) it looks evident the presence of two regions in the  $Y_{22}$  parameters: (i) the isothermal region (above 200 MHz) and (ii) the dynamic self-heating affected region or non-isothermal region (below 200 MHz). Once the cutoff frequency is determined, the  $Y_{22\_iso}$  necessary for the extraction of  $Z_{th}$  is calculated as an extrapolation of  $Y_{22}$ , starting from the highest frequency measured down till the cutoff frequency, as shown Figure 2.12 (right) for the bias point  $V_{BE}=0.9V$ .

In Figure 2.13 is reported the corresponding  $Z_{th}$  extracted, according to Eq. 2.20.

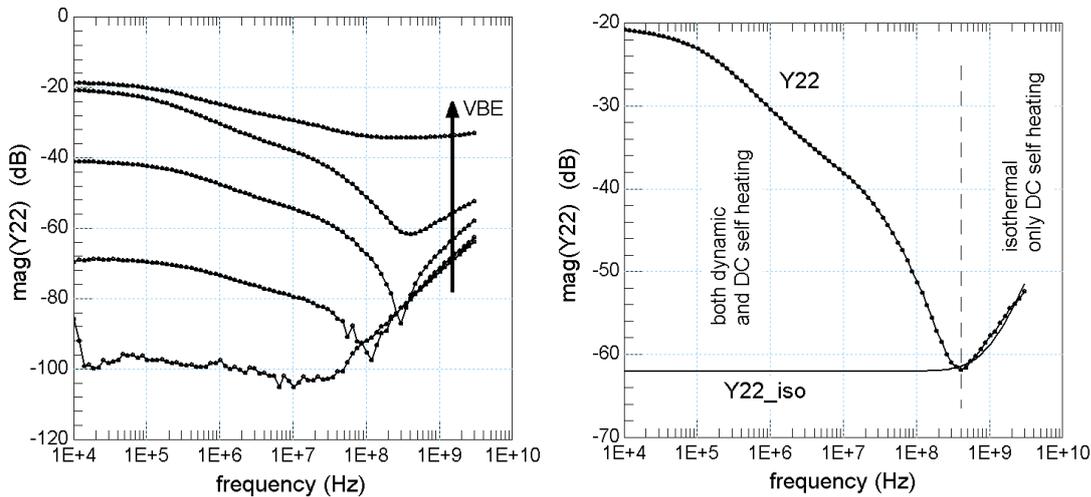


Figure 2.12: (left) variation of the low frequency  $Y_{22}$  parameter for  $V_{CE}=1.25V$  and  $V_{BE}$  ranging from 0.75V to 0.95V. (right)  $Y_{22}$  for  $V_{CE}=1.25$  and  $V_{BE}=0.9V$ : the calculated  $Y_{22\_iso}$  is shown.

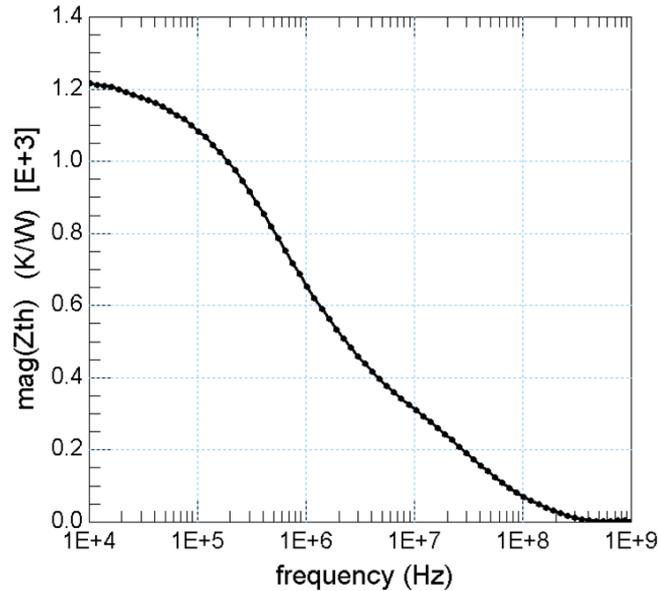


Figure 2.13: extracted  $Z_{th}$  versus frequency in the 10kHz-1GHz range, using the extraction methodology described

## 2.7 Recursive thermal network model

As already detailed in section 2.3, state of the art compact models (in this case HiCuM/L2) normally adopt a single pole network for the simulation of the junction temperature of the transistor  $T_j$ . This assumption represents the easiest model possible to reproduce the evolution of  $T_j$  when a dynamic power dissipation is present within the transistor, but it can show its limitations in specific conditions of operation of the component. In fact, the heat diffusion phenomena from the heat source to the heat sink show a distributed nature, and thus multiple time constant can be needed to approximate this thermal behavior. In literature different modeling approaches have been proposed to threat this problem, and mostly rely on the use of transmission line equivalent circuits, where a distributed RC network is used to model the diffusion of heat; more precisely a Cauer type network is normally chosen for this purpose, since it is more suitable as a thermal analogy from the physical point of view [61], [62]. Using these distributed approaches, the transistor structure can be divided in multiple volume elements [63] and each segment can be associated to its corresponding lumped  $R_{th}$  and  $C_{th}$ , as shown in Figure 2.14, making the following assumptions [63]:

- The graduation of layer thickness should be chosen so that progressively larger thermal time constants ( $\tau_{th} = R_{th} \cdot C_{th}$ ) are produced in the direction of the heat propagation.
- If the dimensions of the heat source are smaller than the cross section of the heat conducting material, the heat spreading region can be assumed to be confined within a spreading angle  $\alpha$ . For heat propagation in homogeneous media, a spreading angle  $\alpha$  of about  $40^\circ$  can be considered.

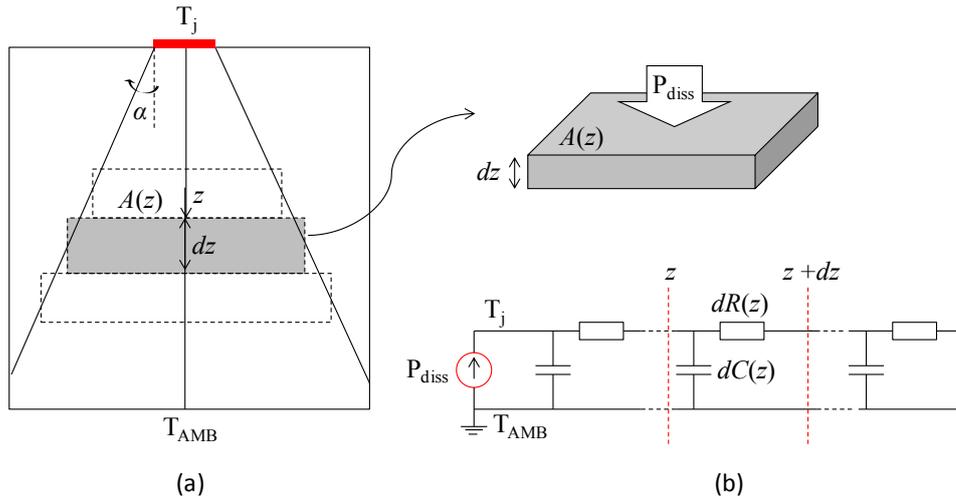


Figure 2.14: (a) Heat diffusion within spreading angle  $\alpha$  in a simple structure (b) electrical transmission line equivalent circuit diagram [10].

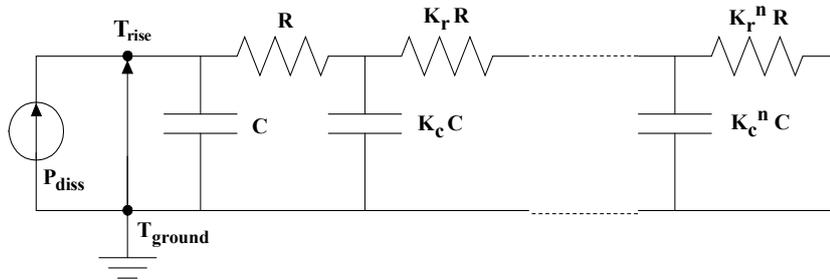


Figure 2.15: A Cauer type recursive network for the  $Z_{th}$  representation (the different elements of the network are in recursive order).

In this work a recursive thermal network will be mainly used, in which the lumped elements are scaled using two different recursive multiplication factors:  $K_r (<1)$  and  $K_c (>1)$  respectively for the  $R_{th i}$  and  $C_{th i}$  as shown in Figure 2.15. The elements of this network can be related to the different volumes in which the transistor structure is ideally subdivided according to the model in Figure 2.14.

Thermal TCAD simulations can help to identify the different volumes delimited by the isothermal contours created when a power source is applied to the transistor structure; in Figure 2.16 is reported the thermal profile simulated in TCAD Sentaurus for the five fingers HBT realized in ST Microelectronics B55 technology for which the  $Z_{th}$  extraction has been previously demonstrated ( $A_E=0.18 \times 5 \mu m^2$ ), in the case where a power dissipation of 30mW per finger is applied. The simulated structure does not include the BEOL and a zoom on just one finger is shown.

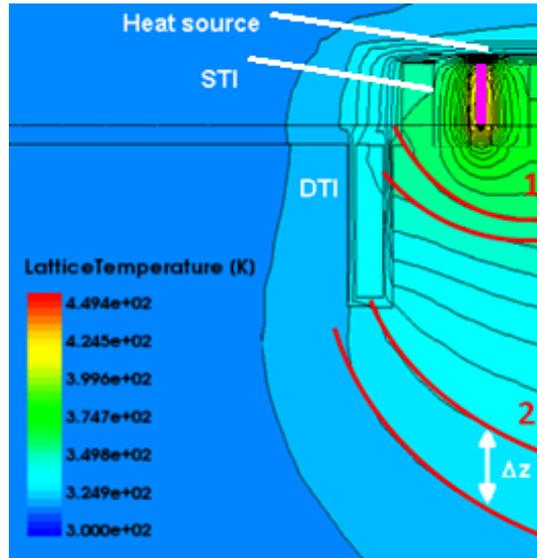


Figure 2.16: thermal TCAD simulations for a five fingers HBT in ST B55 technology. The image is zoomed on one finger, to show the isothermal contours that identify the different volumes in which the structure can be subdivided.

It can be observed in Figure 2.16 that the isothermal contours identify multiple regions in the simulated structure and that the distance between the isothermal contours (and thus the volume) increases as the distance from the heat source increases. The  $R_{th}$  and  $C_{th}$  related to these volumes can be expressed as:

$$\Delta R_{th} = \frac{\Delta z}{kA(z)} \quad \text{Eq. 2.21}$$

$$\Delta C_{th} = \frac{k A(z) \Delta z}{\alpha} \quad \text{Eq. 2.22}$$

where  $\Delta z$  represents the distance between two isothermal contours,  $A(z)$  the related local cross section area and  $k$  and  $\alpha$  are respectively the thermal conductivity and the heat diffusion coefficient of the material. If we compare the  $\Delta R_{th1}$  related to the volume number 1 to the number 2 in Figure 2.16, it will result  $\Delta R_{th1} > \Delta R_{th2}$  (this assumption can be considered valid within the DTI enclosed area, where  $A(z)$  is kept constant by the adiabatic wall created by the DTI), while the opposite will hold for the  $\Delta C_{th}$ , being  $\Delta C_{th1} < \Delta C_{th2}$ . So, as the distance from the heat source increases, the  $R_{th}$  of the discrete volumes decreases, while the related  $C_{th}$  increases; the same trend is obtained in the recursive thermal network in Figure 2.15, moving from the current source till the pole with index  $n$ .

This network architecture in Figure 2.15 ensures a particular behavior as the frequency of the heat source is swept: at low frequency the  $C_{th}$  can be seen as open circuits and thus the  $Z_{th}$  can be approximated as the series of all the  $R_{th}$ ; as the frequency increases, the high valued capacitances located far from the current source start to shunt to ground, thus short-circuiting the related  $R_{th}$ . As the frequency further increases, the smaller

capacitances located closer to the current source will start to shunt as well, thus yielding an equivalent  $Z_{th}$  which tends to 0 (compare to the  $Z_{th}$  versus frequency extracted in Figure 2.13).

In other words at low frequency the whole volume of silicon below the heat source participates to the  $Z_{th}$  and big valued  $C_{th}$  are thermally charged and discharged; as the frequency increases this big volume cannot participate to the thermal sinusoidal variations due to its inertia and so the AC dynamic phenomena can be approximated to happen in a smaller volume, located close to the heat source. It is then evident that the  $Z_{th}$  has a physically distributed nature.

To check the inaccuracies that are introduced in compact models considering a simple single pole thermal network, in Figure 2.17 it is shown the measured  $Z_{th}$  on the five fingers transistor under study and the results of simulation using a thermal network having respectively 1, 3 and 5 poles. The values of  $R_{th}$  and  $C_{th}$  are tuned to obtain the best fit and it is shown that using 3 poles can already lead to an acceptable accuracy in the frequency range measured.

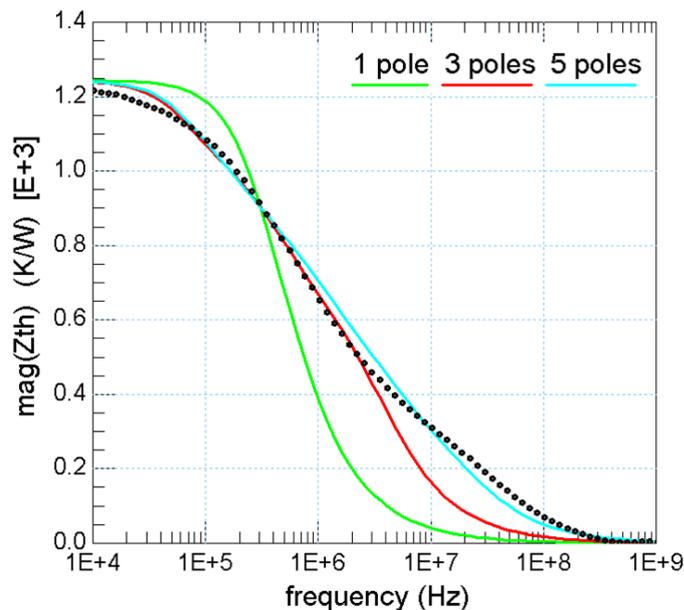


Figure 2.17: comparison of the measured and simulated  $Z_{th}$  using a thermal network having 1, 3 and 5 poles

An alternative way to characterize the distributed nature of the thermal impedance of state of the art transistors, is to perform pulsed measurements; in fact, when operated in pulsed conditions, SiGe HBTs show a transient variation of the junction temperature  $T_j$ , which can lead to a slow response in the  $I_C$  evolution; in fact, if a pulsed  $V_{BE}$  is applied to the transistor (see Figure 2.18), after a quick electrical response, the  $I_C$  will slowly reach its steady state value, over a time proportional to the thermal time constant of the component [64]–[66].

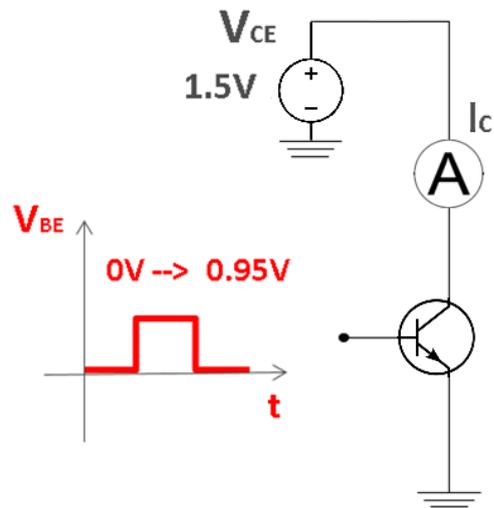


Figure 2.18: measurement setup to characterize the thermal response of the transistor under pulsed operation

In Figure 2.19 it is shown the  $I_C$  measured on a HBT realized in the B11HFC technology from Infineon ( $A_E=0.22 \times 5 \mu\text{m}^2$ ) for  $V_{CE}=1.5\text{V}$ , when a pulse of  $V_{BE}$  is applied, having an amplitude of 0.95V. It can be seen that the  $I_C$  reaches a stable value in around 27 $\mu\text{s}$ ; this thermal evolution is not representable with a good accuracy with a single pole thermal network (represented in the plot by a dotted line), whereas a 3 poles recursive network can provide a more realistic simulation of the pulsed  $I_C$ . The simulations using a single pole network can significantly deviate from the measurements in correspondence of the instant where the  $V_{BE}$  pulse is applied, especially in the case of large emitter area transistors, where the  $I_C$  can reach higher values [64].

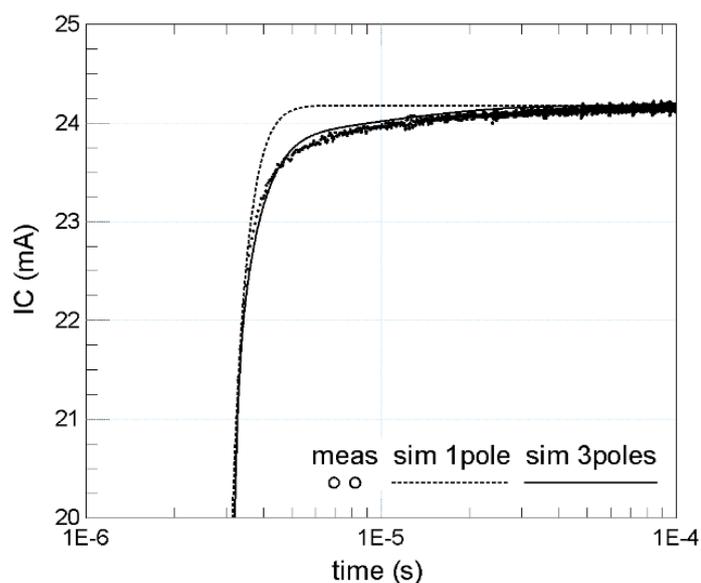


Figure 2.19: measured and simulated  $I_C$  in pulsed conditions using a thermal network having 1 and 3 poles on a HBT in B11HFC technology.

## 2.8 Behavior of the transistor under two tones excitation

As shown in section 2.6, the thermal impedance of state of the art SiGe HBTs has a cutoff frequency in the order of few hundreds of MHz; in other words, if a sinusoid at a given frequency  $f_{IN}$  is fed at the input of the transistor (and thus a sinusoidal power is dissipated within the component), the junction temperature  $T_j$  will experience a sinusoidal variation, synchronized with the time evolution of the power dissipation. This will happen till  $f_{IN}$  is lower than the thermal cutoff frequency of the transistor, whereas for higher frequencies the  $T_j$  will remain stable, due to the thermal inertia of the component [67].

Even if the thermal impedance of these components is mainly located in the low frequency range, it can affect the transistor behavior also when it is operated at much higher frequencies; in fact when a large-amplitude signal or a modulated input signal is put at the input of the transistor, due to its intrinsic non-linearities, inter modulation products are generated [68].

In power amplifier design, an important figure of merit used to characterize linearity is the intermodulation distortion (IMD), caused when multiple frequencies are mixed to form sum and difference products of the original signals; these signals occur as integer multiples of the input frequencies. It is possible to identify IMD of different orders, according to the frequencies which are mixed, however the intermodulation distortion from the third order (IMD3) is of particular importance in narrow band signals because its distortion is often in the signal band. In Figure 2.20 is represented the output spectrum of a transistor affected by intermodulation distortion products, when two frequency tones ( $f_1$  and  $f_2$ ) are put at its input.

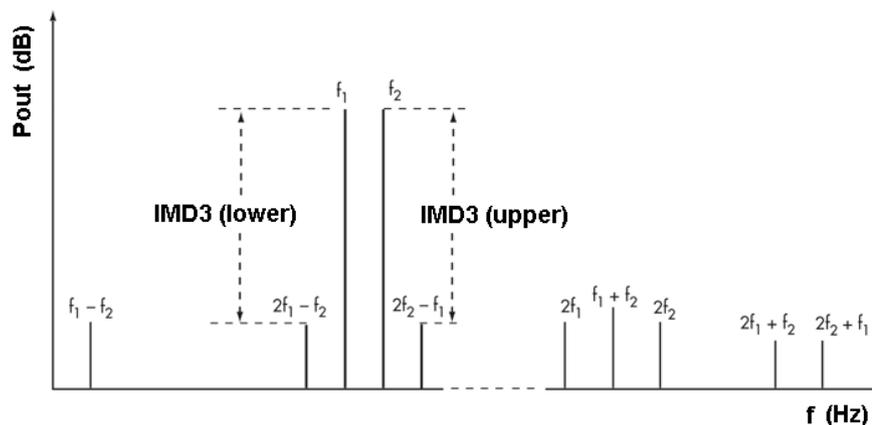


Figure 2.20: schematic representation of the different intermodulation products that can be generated when nonlinearities arise in a transistor.

In general these nonlinear phenomena can be caused by electrical effects, but can also come from thermal self-heating. The mechanism of IMD3 generation for a two-tone input signal is shown in Figure 2.21: there are two processes which lead to the generation of

IMD3 at the output: the first is related to the third-order nonlinear transfer function that directly generates IMD3 (the products depicted in green in Figure 2.21). The second is related to the nonlinear transfer functions of second-order named  $b$  and  $c$  in Figure 2.21: it has to be considered, in fact, that a nonlinear component, such as a transistor, generally has more than one nonlinear transfer functions; the IMD3 can thus be generated when a signal passes the second-order nonlinear transfer function twice. This second process is called the memory effect [69]. In the memory effect, the base-band signal ( $\omega_1 - \omega_2$  and  $\omega_2 - \omega_1$ ), and the second-order higher harmonic signals ( $2\omega_1$  and  $2\omega_2$ ) interact with the fundamental frequency tones ( $\omega_1$  and  $\omega_2$ ), as shown in Figure 2.21. Since the spectra of the thermal transient phenomena due to self-heating can be very close to the baseband components  $\omega_1 - \omega_2$  and  $\omega_2 - \omega_1$ , the thermal transient phenomenon modulates the electrical memory effect. This is the origin of the thermal memory effect [43], [67], [69], [70] (the frequency interactions leading to output intermodulation products affected by thermal memory effect are highlighted in orange in Figure 2.21).

Due to the complex nature of these phenomena, in order to test the linearity of power amplifiers, it is useful to drive them with a two-tone test signal with varying tone spacing and amplitudes, to check how intermodulation distortion mechanisms affect the transistor behavior. If the amplifier behaves properly for a wide range of tone spacings, it can be expected to behave correctly also in the case of wide-band signals.

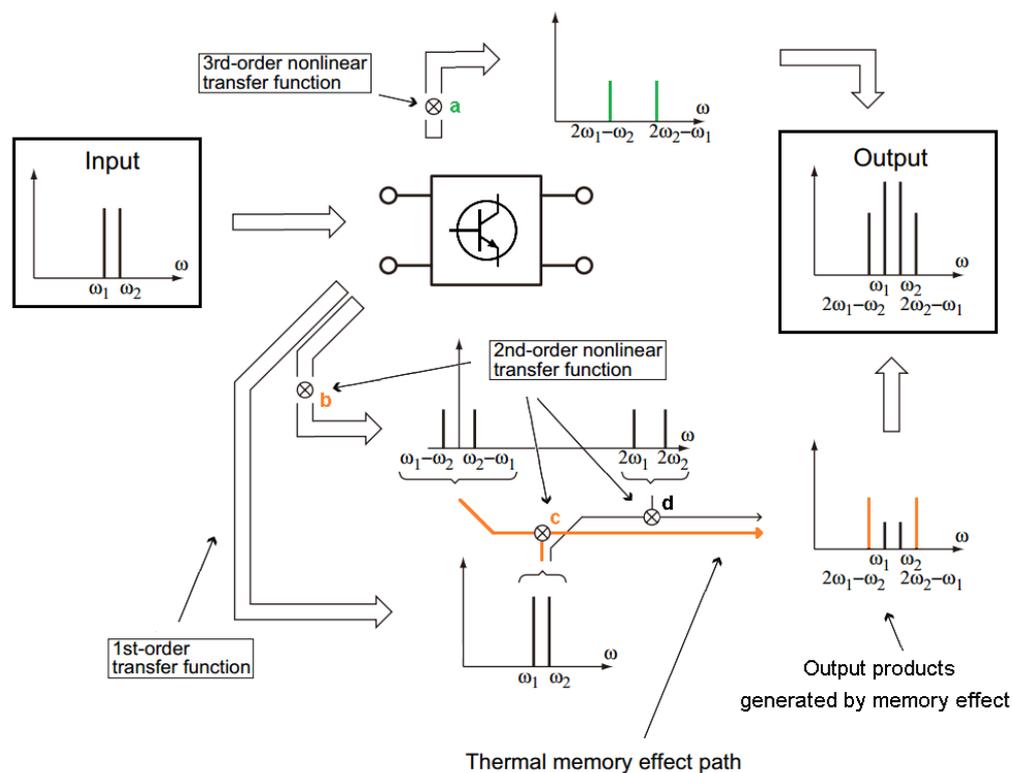


Figure 2.21: Mechanisms of third-order intermodulation distortion (IMD3) generation for a two-tone input signal [28]. The frequency interactions which lead to output intermodulation products affected by thermal memory effect are highlighted in orange.

## Chapter 2

### Device characterization in SiGe HBT technologies

In Figure 2.22 it is shown an ADS setup to simulate the effect of tone spacing on the time evolution of  $T_j$  predicted by the compact model. The transistor is biased at a  $V_{BE}=0.925V$  and  $V_{CE}=1.5V$ , at the input two sinusoidal tones are applied ( $f_1$  and  $f_2$ ), both having an amplitude of  $-20dBm$ . A three poles network is used for these simulations, which has been validated upon low frequency measurements (Figure 2.19 (right) shows the measured and simulated  $Z_{th}$  using the three poles network and a single pole network for the transistor under study).

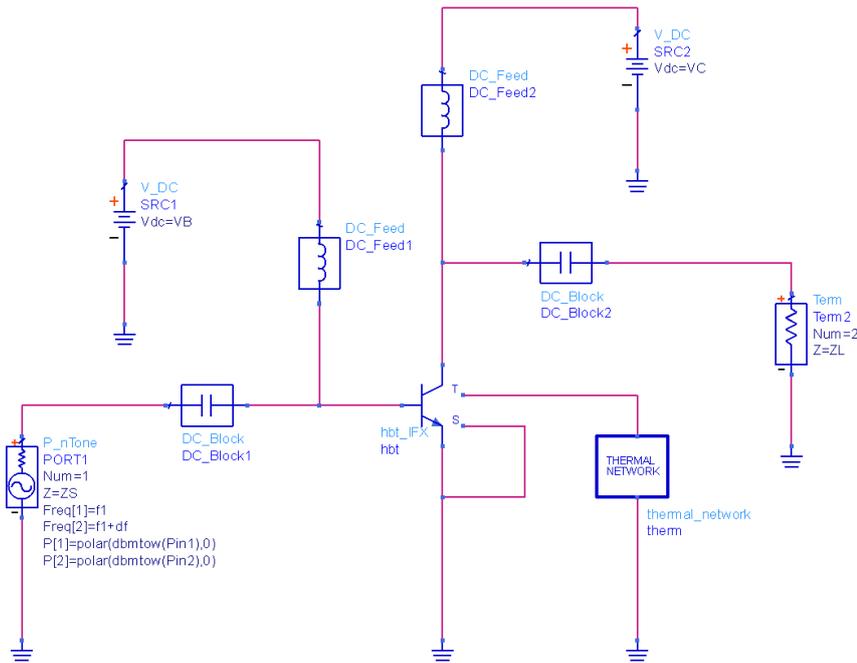


Figure 2.22: ADS schematic used to simulate the behavior of the transistor under a two tones large signal excitation

First of all it is shown in Figure 2.24 the evolution of temperature for a single frequency of operation: the  $f_2$  tone is switched off, while the frequency of  $f_1$  is set equal to 1MHz (left) and 10MHz (right); it is evident that, at low frequency, the  $T_j$  (in blue) is synchronized to the power dissipated in the transistor (in red) and a considerable temperature variation of around  $45^\circ C$  is predicted. If the frequency of the input signal is set to 10MHz instead, due to the reduced  $Z_{th}$ , the  $T_j$  responds to a lower extent to the power dissipation variations, resulting in an almost constant  $T_j$ . At this frequency of operation, the power dissipated in the transistor appears distorted due to a phase shift between the  $I_C$  and  $V_{CE}$  waveforms.

At this point a two tones signal will be applied; it must be taken into account that, when driven by a two tone input signal ( $\omega_1$  and  $\omega_2$ ), the baseband signals  $\omega_1-\omega_2$  and  $\omega_2-\omega_1$  generated by non-linearity (see Figure 2.21), act as a modulating signal on the carrier frequencies, and thus the transistor's current and voltage will follow the envelope of  $\omega_1-\omega_2$  and  $\omega_2-\omega_1$ , as shown in Figure 2.23.

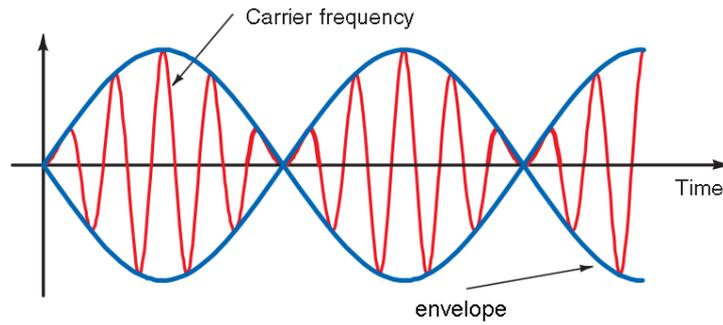


Figure 2.23: representation of the time evolution of a high frequency carrier modulated by a low frequency envelope

In Figure 2.25 it is shown the evolution of temperature when the transistor is stimulated with a two tones signal composed of  $f_1=1\text{GHz}$  and  $f_2=1\text{GHz}+df$ , where  $df$  represents the frequency shift between the two sinusoids, which is set to  $1\text{MHz}$  (left) and  $100\text{MHz}$  (right). It can be seen that when  $df=1\text{MHz}$ , the  $T_j$  evolves following the envelope of the power dissipated in the transistor, with a peak to peak simulated temperature of  $30^\circ\text{C}$ . In the other case, where the envelope of the power dissipation has a frequency of  $100\text{MHz}$ , the  $T_j$  can be approximated to be stable to  $85^\circ\text{C}$ , since its variations are negligible.

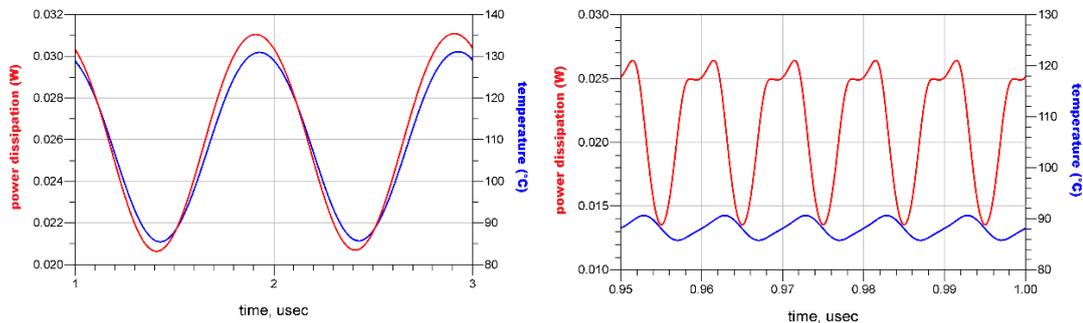


Figure 2.24: simulated power dissipation and junction temperature for a single frequency excitation at a bias point of  $V_{BE}=0.925\text{V}$  and  $V_{CE}=1.5\text{V}$ . The frequency is set to  $1\text{MHz}$  (left) and  $100\text{MHz}$  (right)

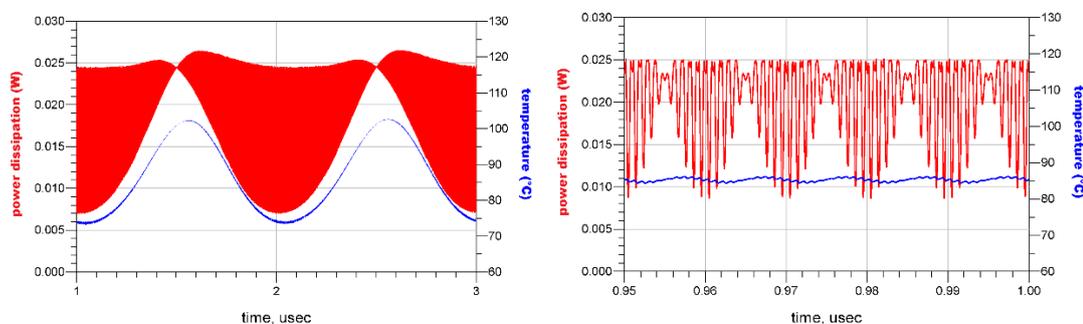


Figure 2.25: simulated power dissipation and junction temperature for a two tones excitation at a bias point of  $V_{BE}=0.925\text{V}$  and  $V_{CE}=1.5\text{V}$ . The frequency spacing is set to  $1\text{MHz}$  (left) and  $100\text{MHz}$  (right)

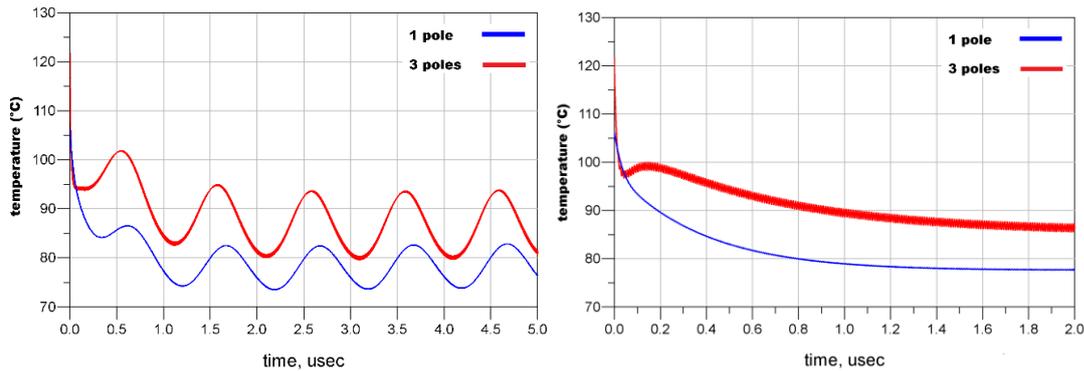


Figure 2.26: simulated power dissipation and junction temperature for a two tones excitation, comparison of the results obtained using a thermal network having a single pole or three poles. The frequency spacing is set to 1MHz (left) and 100MHz (right)

To conclude, in Figure 2.26 is reported a comparison of the temperature evolution that has been obtained for a tone spacing of 1MHz (left) and 100MHz (right) using a three poles and a single pole thermal network, which have been presented in Figure 2.19. It can be observed that a different thermal evolution is predicted by the compact model: in particular the temperature assessment follows a different evolution at the beginning of the simulation, corresponding to the moment at which the transistor is turned on. Also the sinusoidal temperature variation is different in the two cases, since the two models present two different dynamic behaviors. More precisely the single pole network exhibits a lower thermal cutoff frequency and so its thermal capacitance shunts to ground earlier in frequency, thus attenuating the dynamic self-heating; this is the reason for which the sinusoidal temperature variations predicted by the single pole network are smaller.

The temperature variations triggered by the thermal memory effect have to be correctly taken into account, since they can hugely impact the electrical behavior of transistor; at circuit level, it can be important to dispose of a transistor model that can accurately simulate these effects, in order to design predistortion linearizers [44], [69], [71].

## 2.9 Conclusion

In this chapter the basics of thermal characterization in SiGe HBTs are given.

First the effects of the self-heating effect are simulated in HiCuM/L2 using a model card calibrated upon measurements: it is shown that self-heating can affect the transistor behavior in both DC and AC operation.

Then the extraction methodologies used in this work to estimate the  $R_{th}$  and  $Z_{th}$  are presented and discussed with examples of application on the state of the art technologies which are characterized in this thesis.

The limitations of a conventional single pole thermal network are demonstrated, in the time and frequency domain; in particular the results of simulation using a single pole and

a recursive network are compared to the measurement of  $I_C$  affected by self-heating in pulsed operation and to the extracted  $Z_{th}$  in the low frequency range.

Finally the thermal memory effect is introduced and its impact is shown in the case of a two tones large signal simulation; the time evolution of the power dissipation and temperature is reported for different tone spacings and the different behavior obtained using a single pole or a three poles network are highlighted.

## Chapter 3

### Impact of BEOL in single finger devices

#### 3.1 Introduction

In Chapter 2 have been presented measurement and modeling techniques that provide accurate information about the static and dynamic self-heating effects inside the device. It has been discussed that the BC junction is thermally modeled as a heat source: the heat generated actually flows downwards towards the back of the wafer and is also conveyed upwards, in the BEOL, whose dimensions are not negligible compared to the active part of the device. This region is composed of metal and SiO<sub>2</sub> layers, having very different thermal properties, so its presence has a certain thermal impact [45]. In some recent works [72] [34], it has been demonstrated that the heat can find a preferential path through the metallization of the BEOL, and thus a thermal gradient can be observed through the metal layers, thanks to the higher thermal conductivity of copper compared to that of SiO<sub>2</sub> (refer to Figure 3.1).

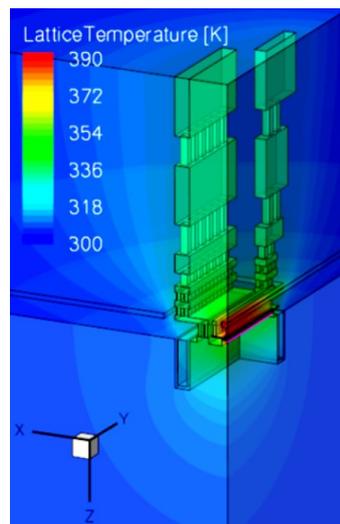


Figure 3.1: lattice temperature distribution inside an HBT with an applied power density of  $40\text{mW}/\mu\text{m}^2$  and a heat source having dimensions  $L_E \times W_E = (10 \times 0.27)\mu\text{m}^2$ ; the HBT has a CBEB configuration and only  $\frac{1}{4}$  of the complete structure is shown [1].

In this chapter we aim at studying and exploiting the thermal benefits of the metal in the BEOL, and propose some specifically designed transistor structures realized in a state-of-the-art SiGe BiCMOS HBT technology from Infineon (B11HFC) having an  $f_T=250\text{GHz}$ ,  $f_{\text{max}}=370\text{GHz}$  and 6 levels of metallization [73]. Different sets of test structures are presented and consist of a transistor cell containing specially designed metal stacks in the BEOL, which act as heat spreaders. Transistors having two different emitter widths are characterized:  $L_E=0.34\mu\text{m}$  and  $L_E=0.22\mu\text{m}$ . The first have the capability of driving higher currents, whereas the latter ensure less parasitic resistances and

capacitances; the choice of the geometry thus depends on the application. A complete DC and RF electrical characterization at small and large signal, as well as a thermal characterization are performed on the proposed test structures, in order to underline the performance improvements that are possible to achieve using these innovative topologies. A compact model is proposed to take into account the impact of the BEOL metallization on the thermal impedance; the model is validated for the  $0.22 \times 5 \mu\text{m}^2$  geometry (which is mainly used in RF design) and is based on a recursive RC network, which can be connected to the thermal node of the HiCuM model.

For this set of test structures, the variation of the thermal behavior with the doping concentration is also analyzed by means of TCAD simulations and compared to the experimental data obtained from measurements.

### 3.2 State of the art in the study of the BEOL impact

As previously stated, in this chapter it will be discussed the possibility to improve the thermal handling capability of SiGe HBTs of the most advanced technologies, by using the layers of metal in the BEOL. This approach has been also used in other state-of-the-art technologies, like three dimensional (3D) integrated circuits, which are also affected by serious self-heating and mutual-heating issues, due to an even increased density of the active components. To overcome these issues, that highly degrade the performances and reliability, thermal vias (made of copper or other materials with high thermal conductivity) are specifically designed and realized through the oxide, thus allowing a better handling and extraction of the power dissipated [74]–[76].

The same principle of exploiting the metallization of the back-end-of-line (BEOL) has been applied in some recent works [45], [72] that demonstrated a significant influence on the thermal behavior of SiGe HBTs of the most advanced technologies. In these works the impact of the BEOL on the thermal properties of HBTs has been analyzed by means of TCAD simulations. On the optimization of these back-end-of-line stacks, limited information is available in the literature. In [77], for instance, some innovative test structures are proposed to investigate the impact of the strain created by metal dummies on the bandgap inside the base of the transistors. The metal stacks are placed above the active part of the transistor and the result is a sensible increment of the  $I_C$  as well a higher transit frequency ( $f_T$ ). This improved electrical behavior is caused by a variation in the base bandgap structure, whereas no sensible improvement of the thermal properties has been reported. This is probably due to the fact that the metal dummies are not connected by vias to the emitter contact, which reaches high temperatures when the device is operated at high power dissipation [78].

### 3.3 Test structures in $0.34 \times 5 \mu\text{m}^2$ geometry

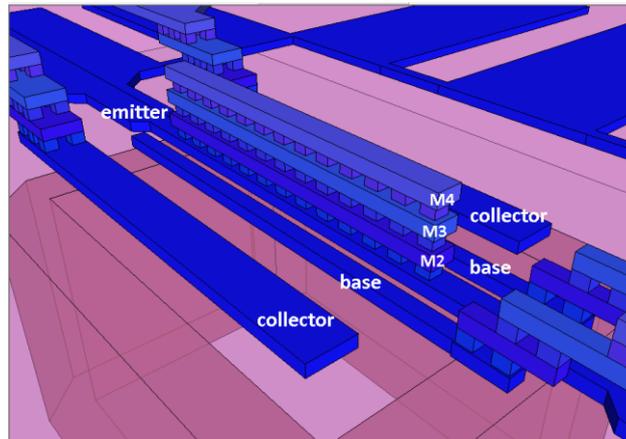


Figure 3.2: 3D representation of the  $E4_{\text{narr}}$  test structure

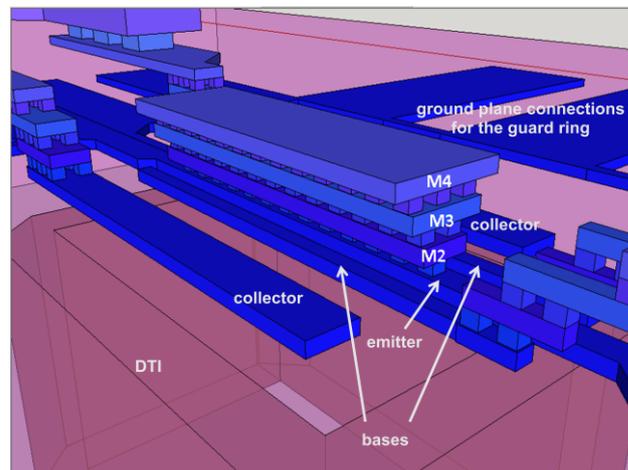


Figure 3.3: 3D representation of the  $E4_{\text{wide}}$  test structure.

The test-structures under study are designed in-house and consist of a single transistor having a CBEBE arrangement for the contacts and are connected in common emitter configuration. The reference test structure in our study consists of an HBT that has only metal-1 above all the contacts. For all the test-structures that will be here discussed, the drawn emitter window is  $5 \times 0.34 \mu\text{m}^2$ ; this transistor geometry yields high values of power dissipation and the addition of metal stacks above the heat source can thus show some sensible variation on the electro-thermal behavior.

Different approaches are used to design the BEOL metallization upon the active part of the component. For the first set of test structures the metal bars are stacked one on top of the other and connected by vias; all the metal layers have the same length and width ( $0.34 \mu\text{m}$ ). These structures are named  $E2_{\text{narr}}$ ,  $E3_{\text{narr}}$  and  $E4_{\text{narr}}$ , where the number stands for the level of the last metal stack that is added and E indicates that the metal dummies are placed above the emitter contact (refer to Figure 3.2). A second set is similar to the first, but this time the additional metal dummies have a gradually increasing width, as

shown in Figure 3.3: for this set of structures the overall volume of added metal is higher than the previously discussed set; these structures are named  $E2_{\text{wide}}$ ,  $E3_{\text{wide}}$  and  $E4_{\text{wide}}$  and the width of the metal bars upon the emitter is gradually increased till reaching  $1.52\mu\text{m}$  for the  $E4_{\text{wide}}$  structure. Finally a last set is characterized with metal stacks above the two base contacts, as shown in Figure 3.4; two versions are realized, named B2 and B3, whereas the reference structure will be referred to as B1E1 (in this case, as already mentioned, just metal-1 is present on both the base and emitter contacts).

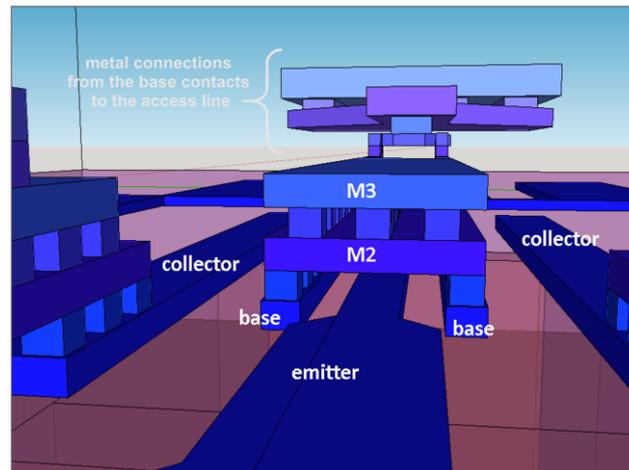


Figure 3.4: Schematic 3D representation of the B3 test structure.

The added metal stacks are designed in such a way that they do not impact the access lines compared to the reference structure B1E1, so the same contact resistance for all the test structures under study is guaranteed by contacting similarly all the transistor nodes through the same metal interconnections.

In Figure 3.5 we sketched the thermal resistances that are distributed along the BEOL for the test structure  $E4_{\text{narr}}$ . Since the BC junction is thermally modeled as a heat source, in the equivalent electrical circuit we represent it with a current source. In this schematic representation the heat actually flows downwards towards the back of the wafer through  $R_{\text{thFEOL}}$ , which models the thermal properties of the front-end-of-line part, and is also conveyed upwards through the metallization, which can be seen as a preferential path for the heat flux, thanks to the higher thermal conductivity of copper compared to that of  $\text{SiO}_2$  [45]. It has been shown in [45] by means of TCAD simulations that at a certain lateral distance from the metal stacks (that reach a temperature  $T_{\text{metal}}$ , higher than  $T_{\text{amb}}$ ) the structure presents an isothermal contour at ambient temperature; for this reason adding metal stacks results in adding T-networks (formed by  $R_{\text{th\_metal}}$  and  $R_{\text{th\_oxide}}$ ), thus allowing alternate paths for the heat flow to the thermal ground ( $T_{\text{amb}}$ ). At the same time, as more metal levels are stacked, the distance  $t_{\text{metal-air}}$  decreases, thus decreasing the corresponding  $R_{\text{th}}$  and contributing further to the diminution of the overall  $R_{\text{th}}$  of the component. If we want to represent a thermal model for test structure B1E1 instead, since the metal stacks from metal-2 to metal-4 are absent, we do not consider the thermal resistances of the metal layers in the region named “BEOL part” (see Figure 3.5).

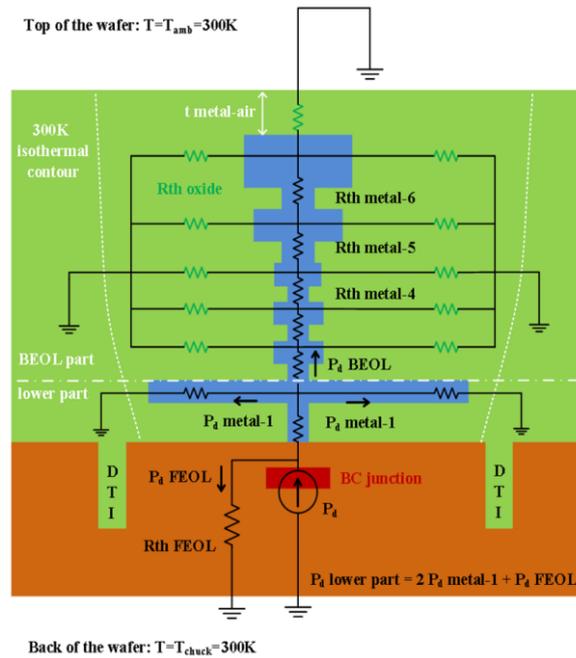


Figure 3.5: schematic representation of the thermal resistances distributed across the whole back end of line.

### 3.4 Test structures characterization

#### 3.4.1 DC characterization

A DC characterization of the structures has been done using a Keysight E5270B DC analyzer; the measurements are performed on a probe station equipped with a thermal chuck.

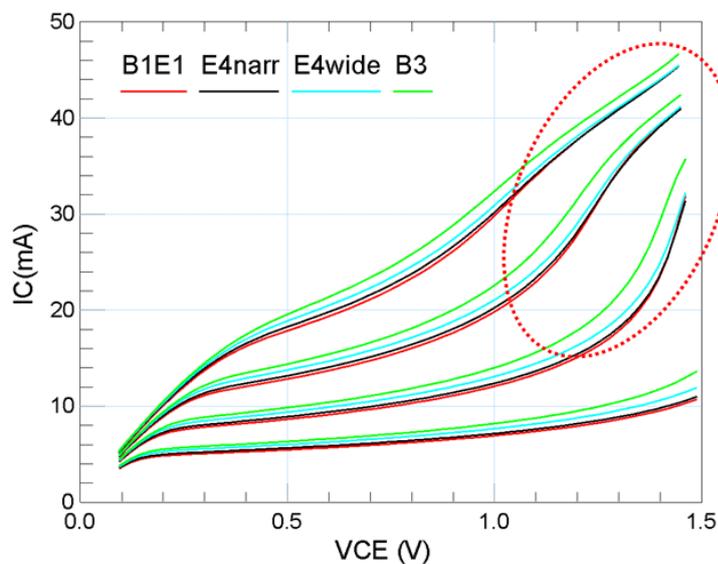


Figure 3.6: Output curves measured for different HBT test structures realized in the Infineon B11HFC process;  $V_{BE}$  ranges from 830mV to 890mV.

Figure 3.6 shows the output curves measured at a chuck temperature  $T_{\text{chuck}}=300\text{K}$ ; for sake of clarity, within each set of test structures only the ones having the highest level of metallization are shown. We can notice in Figure 3.6 that in the region at low  $V_{\text{CE}}$  of the output curves (where the power dissipation is quite low), the test structures that have metal dummies on top drain a slightly higher  $I_{\text{C}}$  than the reference B1E1 (the percentage variations observed at  $V_{\text{BE}}=0.83\text{V}$  and  $V_{\text{CE}}=0.5\text{V}$  are shown in Table 3.1). This variation is due to the mechanical strain effects of the metal dummies, that lead to a change in the band-gap structure of the HBT, as described in [77].

Test structures	$\Delta I_{\text{C}} \%$
<b>B1E1</b>	0.0%
<b>E2<sub>narr</sub></b>	1.8%
<b>E3<sub>narr</sub></b>	2.5%
<b>E4<sub>narr</sub></b>	3.4%
<b>E2<sub>wide</sub></b>	5.5%
<b>E3<sub>wide</sub></b>	9.0%
<b>E4<sub>wide</sub></b>	10.0%
<b>B2</b>	10.2%
<b>B3</b>	15.8%

Table 3.1:  $I_{\text{C}}$  variation at  $V_{\text{BE}}=0.83\text{V}$  and  $V_{\text{CE}}=0.5\text{V}$ .

As reported in Table 3.1, as the level of metal stacks and the width of metal dummies increases, the percentage increase in  $I_{\text{C}}$  ( $\Delta I_{\text{C}}\%$ ) tends to increase, in accordance to the results published in [77]. Furthermore it is noticeable that adding metal dummies on the base contacts results in a more pronounced strain effect and thus a higher  $\Delta I_{\text{C}}\%$ . From Figure 3.6 we observe that the  $I_{\text{C}}$  trend of the compared structures starts to be different if we get closer to the regions of high power dissipation ( $P_{\text{diss}}$ ), which are highlighted with a dashed circle, where a total  $P_{\text{diss}}$  is estimated to range between 30 mW and 70 mW. The different behavior of the test structures in the high power dissipation region is mostly related to a variation in the  $R_{\text{th}}$  and will be discussed below with more details.

In Figure 3.7 the output conductance  $g_{\text{out}}=\partial I_{\text{C}}/\partial V_{\text{CE}}$  is plotted as a function of the measured current in each structure. It is evident that, for a given  $I_{\text{C}}$ , higher than 15 mA, the structures containing metal dummies exhibit a lower  $g_{\text{out}}$  than the reference structure. It has been verified, by means of simulations using a HiCuM model of the transistors under study, that the decrease of  $g_{\text{out}}$  is caused by the combination of two different effects: (i) the increase of the saturation current (which is induced by the BEOL mechanical stress) and (ii) the decrease of the  $R_{\text{th}}$ . Regarding the latter, it must be pointed out that the self-heating effect (among other effects like avalanche multiplication) is responsible for the sudden increase of the  $I_{\text{C}}$  in the high power dissipation region (clearly visible in Figure 3.6 for  $V_{\text{BE}}=0.85\text{V}$ ).

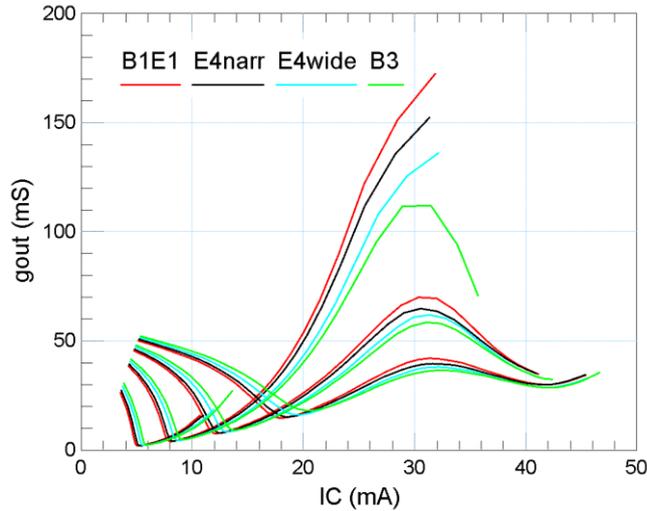


Figure 3.7: Output conductance for the same bias points and test structures shown in Figure 3.6.

As shown in Figure 3.7, the peak of  $g_{out}$  (or, equivalently, the maximum slope of  $I_C$  in the  $I_C(V_{CE})$  plane in Figure 3.6) is reached for all the test structures at an  $I_C$  value of around 30 mA. For this value of  $I_C$ , at  $V_{BE}=0.85$  V a maximum  $g_{out}$  variation of around 54% is found between the reference structure B1E1 and structure B3. For  $I_C$  values higher than 30 mA the  $g_{out}$  starts to decrease; this phenomenon is caused by the extrinsic emitter resistance of the HBT, which plays a feedback role, limiting the internal base-emitter voltage for high values of  $I_C$  and thus counterbalancing the  $I_C$  increase caused by the self-heating effect.

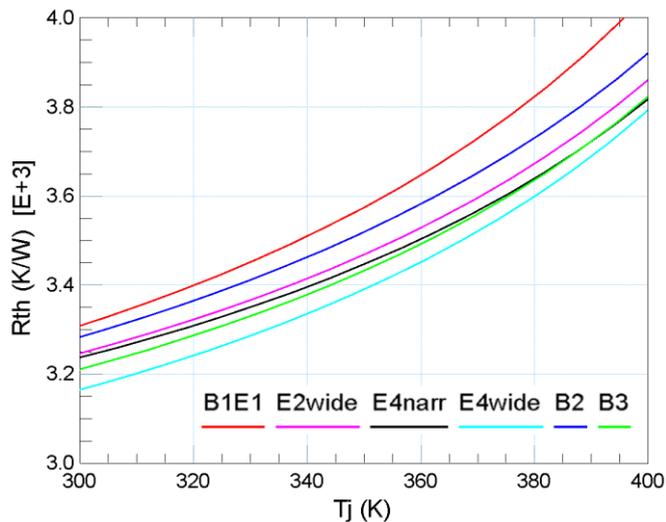


Figure 3.8: Extracted  $R_{th}$  versus  $T_j$  for some of the structures presented.

### 3.4.2 Thermal characterization

As already discussed in the introduction, we expect that the addition of metal stacks above the active part of the transistor allows an alternate path for the heat flow, thus lowering its  $R_{th}$ . An  $R_{th}$  extraction is realized performing DC measurements at constant  $I_B$  for

different values of  $T_{\text{chuck}}$ , to calibrate the  $V_{\text{BE}}$  as a function of the ambient temperature. Then, using an approach similar to the extraction method proposed in [52], the  $R_{\text{th}}$  is calculated and is plotted as a function of the junction temperature  $T_j$  in Figure 3.8 for some of the test structures under study. It is possible to see that all the test structures present an  $R_{\text{th}}$  that is lower than B1E1 and the best thermal behavior is realized for the test structure E4<sub>wide</sub>, which presents an  $R_{\text{th}}$  around 5% lower than B1E1. Comparing the  $R_{\text{th}}$  of test structure E4<sub>narr</sub> and E4<sub>wide</sub> it can be stated as well that increasing the width of the metal dummies yields an enhanced thermal behavior. A sensible  $R_{\text{th}}$  decrease is obtained also for the set of structures B2 and B3.

### 3.4.3 Small signal RF characterization

To continue our analysis a small signal RF characterization is proposed and the  $f_T$  and  $f_{\text{MAX}}$  of the transistors under study are extracted. For this purpose, S-parameters are measured at 35 GHz using a ZVA67 Rohde-Schwarz VNA and de-embedded using the same open and short structures for all the transistors under study. Also in this case, for sake of clarity, only the results for the most representative test structures having the highest level of metallization are reported and commented.

From the 3D images in Figure 3.3 and Figure 3.4 it is evident that the metal dummies that have been added are electrically connected to the emitter contact or to the base contact and could therefore add potential parasitic elements at high frequency and impact in a negative way on the RF figures of merit like  $f_T$  and  $f_{\text{MAX}}$ .

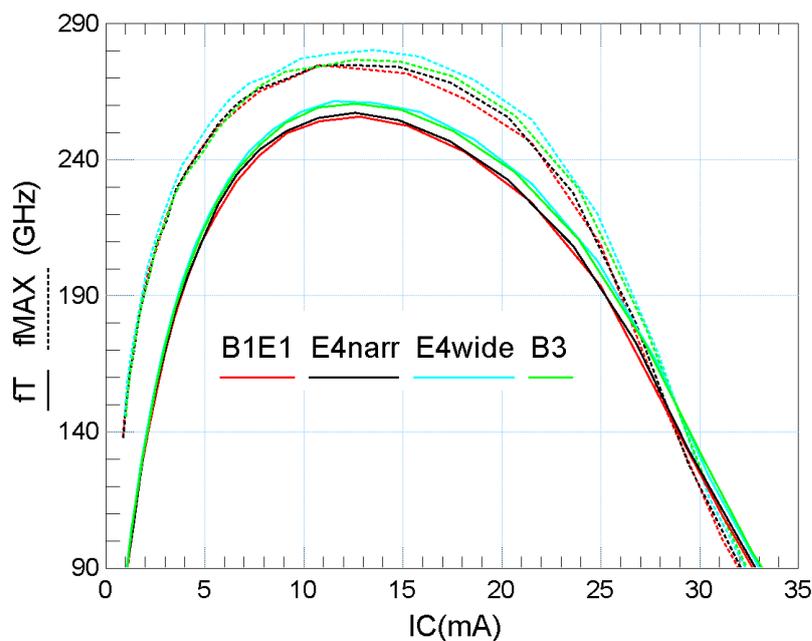


Figure 3.9:  $f_T$  (solid line) and  $f_{\text{MAX}}$  (dotted line) evaluated at  $V_{\text{CE}}$  of 1.5 V.

The extracted  $f_T$ , evaluated at an applied  $V_{\text{CE}}$  of 1.5 V is plotted versus the measured  $I_C$  in Figure 3.9 (solid line) and demonstrates instead that the presence of dummies does not

degrade this figure of merit. On the contrary, a sensible increment of the peak  $f_T$  is noticeable for the test structures E4<sub>wide</sub> and B3. For  $I_C$  higher than 10~15 mA the structures containing metal dummies perform better in terms of  $f_T$ , probably due to the effect of the mechanical stress and to the reduction of  $R_{th}$ , which plays a positive role in the electro-thermal behavior of the transistor when high levels of  $P_{diss}$  are reached. The same improvement is detectable on the  $f_{MAX}$ , which is extracted at the same bias conditions as the  $f_T$  and also shown in Figure 3.9 with dotted lines.

### 3.4.4 Large signal measurements

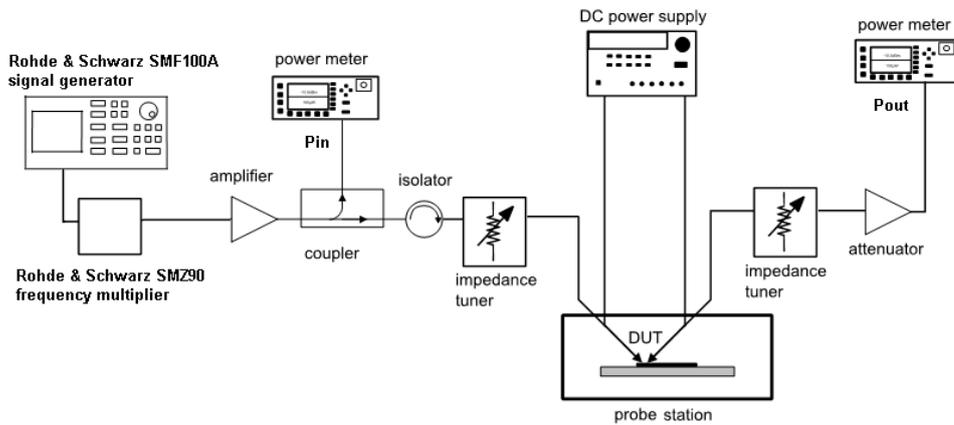


Figure 3.10: Load pull measurement bench

The behavior of the different transistor structures is finally tested under large signal conditions at 77 GHz on a single tone load-pull measurement system.

The passive load and source tuners (FOCUS CCMT) allow generating complex impedances between 57-90GHz. The Rohde & Schwarz SMF100A is used as a signal generator in combination with the SMZ90 frequency multiplier. A directional coupler divides the input signal into two parts: one is guided to the power meter for measuring the power delivered to the DUT and the other one is the actual input signal. The isolator prevents the reflected signal from returning in the coupler and the power meter at the output port allows to measure the  $P_{out}$ .

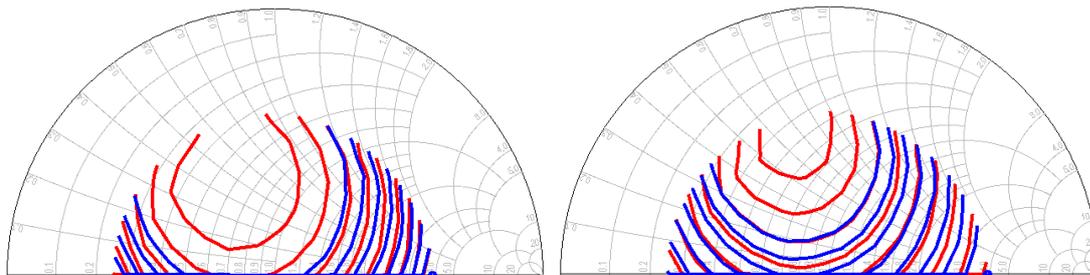
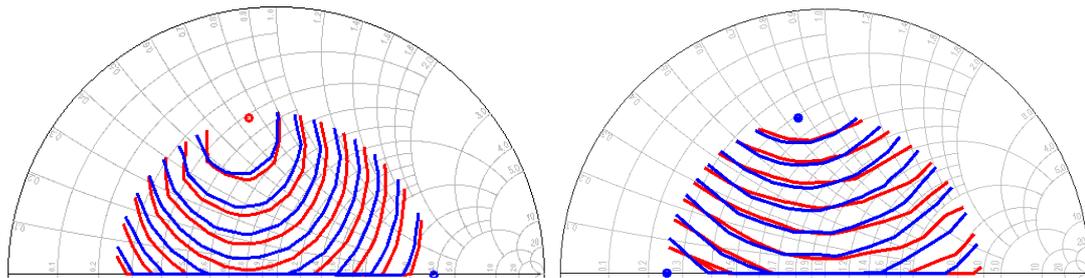


Figure 3.11:  $P_{out}$  (left) and  $\eta$  (right) contours for the bias point  $V_{BE}=835mV$  and  $V_{CE}=1.25V$  when a  $P_{avs}$  of 0dBm is applied. In red are shown the results for B1E1, whereas in blue E4<sub>wide</sub>. The  $P_{out}$  contours range from 1.2dBm to 4.5dBm, whereas the  $\eta$  contours range from 6.1% to 18.2%.



Test structure	Pout [dBm]	$\eta$ [%]
B1E1	from 0.8 to 4.4	from 5.8 to 19.7
E4 <sub>wide</sub>	from 1.2 to 5.9	from 6.1 to 23.1

Figure 3.12:  $P_{out}$  (top) and  $\eta$  (bottom) contours for the bias point  $V_{BE}=835\text{mV}$  and  $V_{CE}=1.25\text{V}$  when a  $P_{avs}$  of  $0\text{dBm}$  is applied. In red are shown the results for B1E1, whereas in blue E4<sub>wide</sub>. The ranges of the  $P_{out}$  and  $\eta$  contours are different than in Figure 3.11 and are reported in the table for the two test structures.

In Figure 3.11 are reported the output power ( $P_{out}$ ) and output efficiency ( $\eta=P_{out}/I_C V_{CE}$ ) contours obtained from a sweep of the output load over 70 complex impedances on test structures B1E1 and E4<sub>wide</sub>; in this plot, the measured  $P_{out}$  and  $\eta$  are reported using the same ranges for the two structures compared (from  $1.2\text{dBm}$  to  $4.5\text{dBm}$  for the  $P_{out}$  and from  $6\%$  to  $18\%$  for the  $\eta$ ). Although in this representation the B1E1 and E4<sub>wide</sub> contours seem to be different, it is to be noticed that the loads yielding the maximum values of  $P_{out}$  and  $\eta$  are located in the same regions of the Smith chart for the two test structures under comparison; this is shown in Figure 3.12, where the range limits for  $P_{out}$  and  $\eta$  are adapted to the minimum and maximum values measured on each of the two transistors. For all the Smith chart contours shown, the power available from the source ( $P_{avs}$ ) is  $0\text{dBm}$ , whereas the base and collector voltages are set respectively to  $835\text{mV}$  and  $1.25\text{V}$ , which corresponds to the bias conditions of peak  $f_T$ .

Next, the input impedance  $Z_S$  is fixed at  $50\Omega$ , whereas the output impedance  $Z_L$  is set respectively to  $50\Omega$  and to the load ensuring the highest  $\eta$ , which is found to be  $(20.7+j37.6)\Omega$ ; the power available from the source ( $P_{avs}$ ) is swept from  $-12\text{dBm}$  to  $7\text{dBm}$ . We report the results for the same bias point previously used:  $V_{BE}=835\text{mV}$  and  $V_{CE}=1.25\text{V}$ .

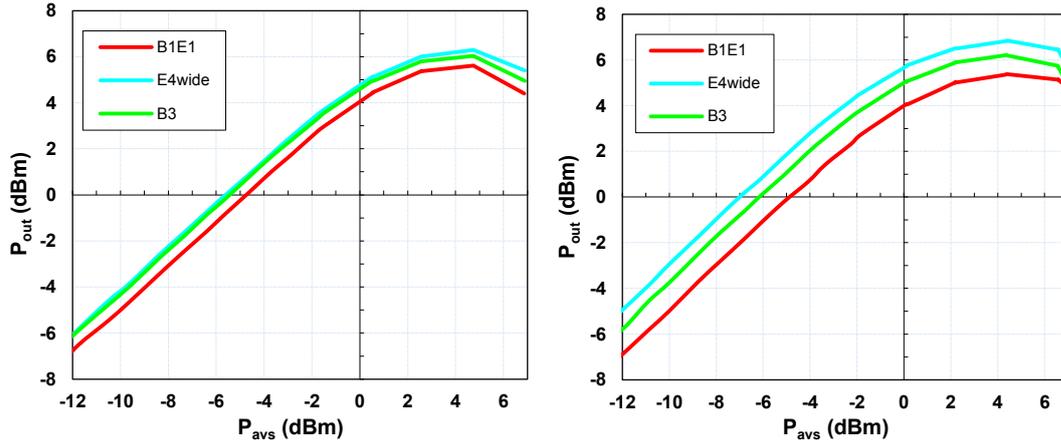


Figure 3.13: Output power plotted versus  $P_{avs}$  for  $V_{BE}=835$  mV and  $V_{CE}=1.25$  V; on the left for load impedance  $50\Omega$  and on the right for the load yielding maximum  $\eta$ :  $(20.7+j37.6)\Omega$ .

It is possible to see in Figure 3.13 that at  $Z_L=50\Omega$  the structure  $E4_{wide}$  is able to deliver around 0.5 dBm of additional power to the output over the whole range of swept  $P_{avs}$ ; when the output impedance is  $(20.7+j37.6)\Omega$  this difference can reach 2dBm, showing that the impact of the BEOL at large signal can be significant and that it is also function of the load conditions applied to the transistor.

Figure 3.14 shows the output efficiency for the three structures under study; it has been measured an  $\eta$  increase till 2.5% and 8.2% passing from test structure B1E1 to  $E4_{wide}$  for a  $Z_L$  of respectively  $50\Omega$  and  $(20.7+j37.6)\Omega$ .

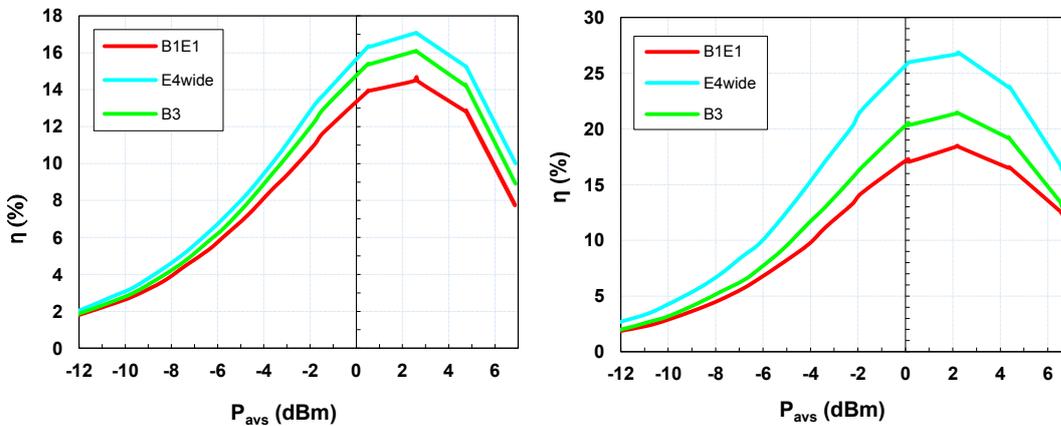


Figure 3.14: Output efficiency versus  $P_{avs}$  for  $V_{BE}=835$  mV and  $V_{CE}=1.25$  V; on the left for load impedance  $50\Omega$  and on the right for the load yielding maximum  $\eta$ :  $(20.7+j37.6)\Omega$ .

To explain this enhancement it is helpful to investigate the evolution of  $I_C$  as the input power increases (Figure 3.15): it is shown that for low  $P_{avs}$  it is the structure B3 that drains the highest  $I_C$ , due to the effect of mechanical stress already reported in Table 3.1. As  $P_{avs}$  increases, though, it is  $E4_{wide}$  that drains the lowest current, since it has the lowest  $R_{th}$  among the other structures. This lower  $I_C$  yields lower power dissipation and, together with the slightly higher  $P_{out}$  (Figure 3.13) implies a better  $\eta$  figure of merit.

Large signal measurements at different bias points show a similar behavior and are not reported here.

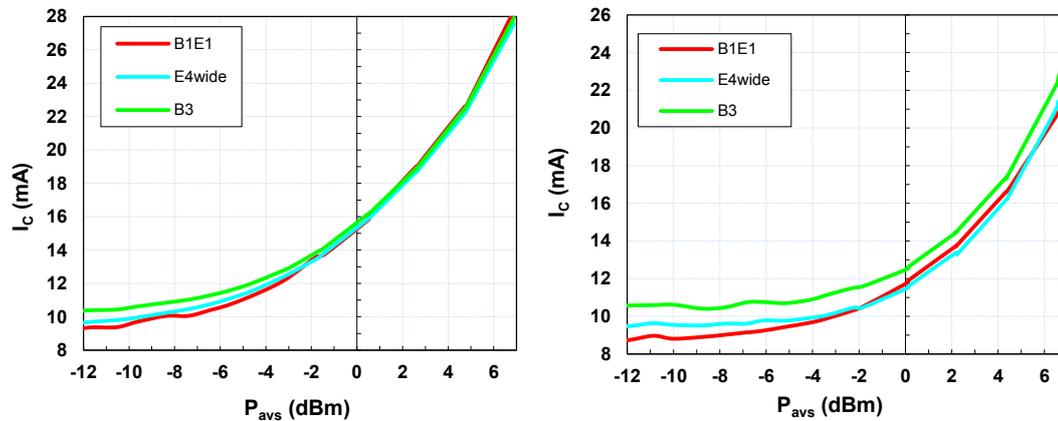


Figure 3.15: Collector current versus  $P_{avs}$  for  $V_{BE}=835$  mV and  $V_{CE}=1.25$  V; on the top for load impedance  $50\Omega$  and at the bottom for the load yielding maximum  $\eta$ :  $(20.7+j37.6)\Omega$ .

### 3.5 Test structures in $0.22 \times 5 \mu\text{m}^2$ geometry

After having presented in the previous sections a complete electrical characterization of the BEOL impact, the focus will be hereby on the possibility to take into account its thermal impact into compact models. It will be shown the results of test structures realized using a  $0.22 \times 5 \mu\text{m}^2$  geometry for the transistors and a CBEBE configuration for the contacts; this geometry ensures a lower  $R_B$  and  $C_{BC}$ , which result in a higher  $f_{MAX}$ , making it a good choice in circuit design where RF performances are important.

The test-structures consist of a single transistor cell in common emitter configuration and are realized on a different wafer than the ones presented in section 3.3. As it is possible to see in Figure 3.16b, metal stacks are placed above the emitter contact till metal-6. The colors of the metallization are: blue for the base connections, green for the collector, brown for the emitter; the active part of the device is placed below the BEOL, and is partially visible (in yellow), while silicon is colored in orange. At the metal-6 level the base and collector are then connected to transmission lines (not shown), while the emitter is connected to the guard ring, and then to a ground plane (not shown). This structure will be named M6 (Figure 3.16b) and is compared to a reference one, named M1, where just metal-1 is present above the emitter, to electrically connect it to ground, without other metal layers above (Figure 3.16a).

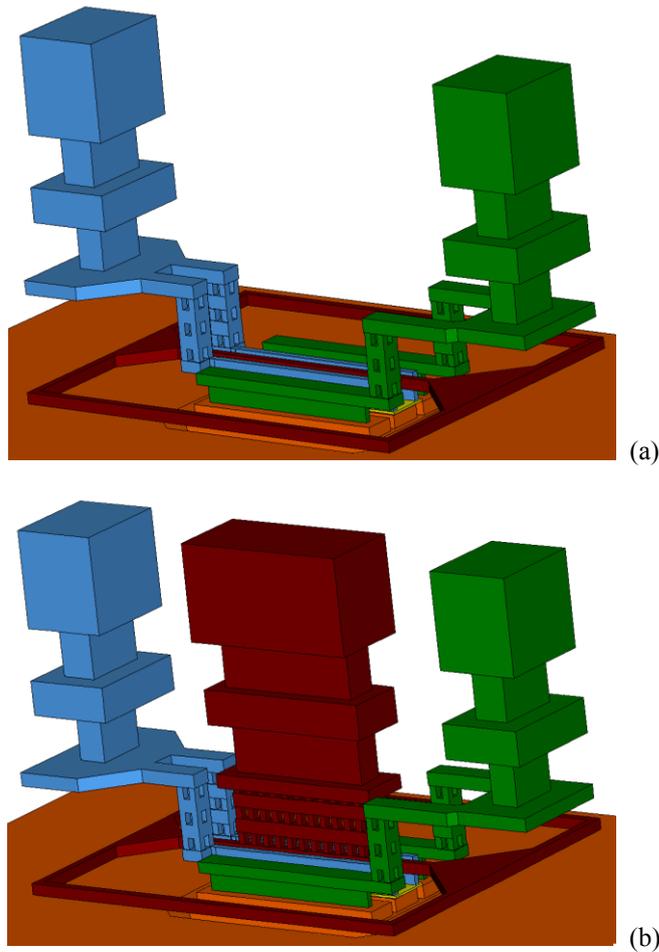


Figure 3.16: 3D images of the standard test-structure M1 (a) and test-structure M6 with metal stacks above the emitter (b). These test structures contain HBTs designed using the Infineon B11HFC process and having a drawn emitter area of  $0.22 \times 5 \mu\text{m}^2$

### 3.6 Thermal modeling of the BEOL metallization

In Figure 3.17 and Figure 3.18 we propose an equivalent electrical model to simulate the thermal behavior of the two test structures. Since the thermal impedances of these devices show a distributed nature [45], [79], [80], three-poles Cauer-type recursive networks are used. For structure M1 in Figure 3.17 just one network is used to model the lower part, which takes into account the thermal behavior of the device from the bottom of the wafer up to metal-1, then a second network is added in parallel to simulate the BEOL part (for the case of M6 shown in Figure 3.18). In the two proposed models the temperature dependency of  $R_{\text{th}}$  is also taken into account.

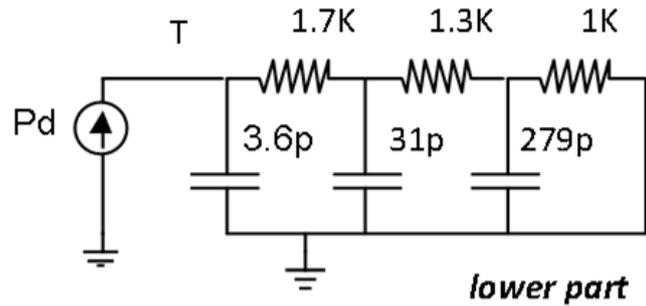


Figure 3.17: Cauer-type recursive network used to model the thermal impedance of the M1 structure; this network models just the thermal behavior of the lower part of the device up to metal-1.

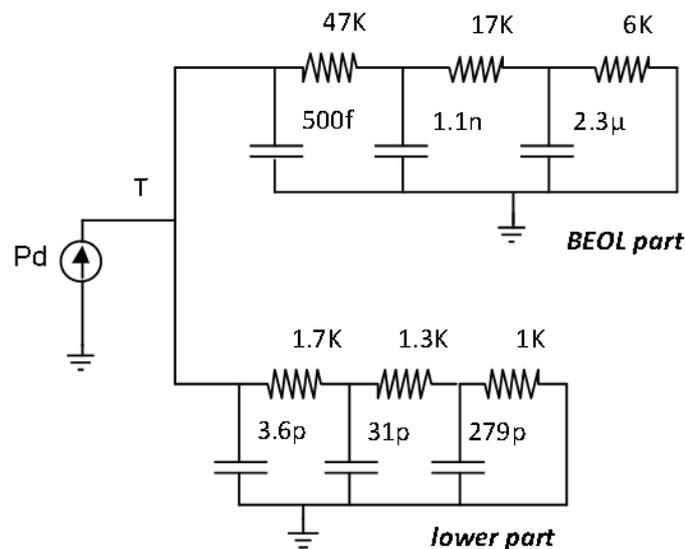


Figure 3.18: Cauer-type recursive network used to model the thermal impedance of the M6 structure. The dissipated power  $P_d$  flows in the lower part (that takes into account the thermal behavior of the device up to metal-1) and in the BEOL part (which models the thermal behavior of the metal stacks from metal-2 to metal-6).

### 3.6.1 DC measurements

To evaluate the thermal behavior of the two test structures under study, first of all a DC characterization is made on a probe-station equipped with a thermal chuck (that sets  $T_{amb}=300K$ ): as expected for the output characteristics (measured with an Agilent 4155A DC analyzer), the transistor in the M6 structure drains less collector current than M1 in the bias regions where high self-heating occurs (Figure 3.19): the bias point where this  $\Delta I_C$  is maximum is for  $V_{BE}=0.925V$  and  $V_{CE}=1.5V$ , for which passing from structure M1 to M6 gives an  $I_C$  drop from 18.5mA to 16.7mA (around 10% decrease, which is not negligible). The two thermal networks presented in the previous section are connected to the temperature node of a HiCuM model and the values of the different  $R_{th}$  are adjusted to fit the measured data; the output curves obtained from the simulations are represented with solid lines in Figure 3.19. For the highest power dissipation, the  $T_j$  predicted by the

simulator is 427K for M1 and 412K for M6. The equivalent  $R_{th}$  used in the thermal models drops from 3950K/W to 3739K/W (around 5%) passing from structure M1 to M6, in agreement with the results in [45]. According to the model shown in Figure 3.18, with a total  $P_d$  of 40mW, the amount of power that is dissipated in the lower part is 36mW, whereas 4mW will be dissipated in the BEOL part.

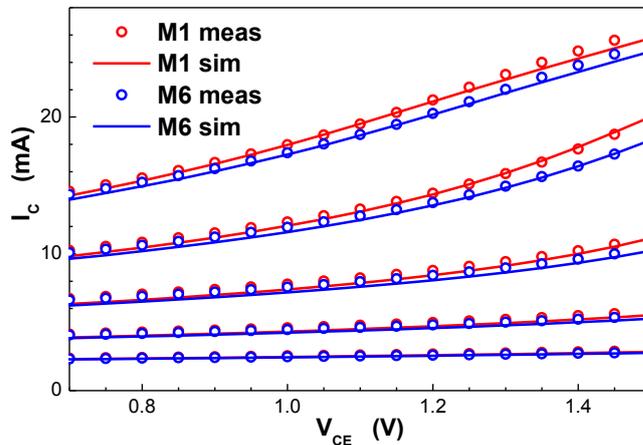


Figure 3.19:  $I_C(V_{CE})$  for different  $V_{BE}$  values: zoom on the output curve in the region where self-heating is more present;  $V_{BE}$  ranges from 850mV to 950mV.

### 3.6.2 Low frequency measurements

To evaluate the impact of the BEOL on the  $C_{th}$ , the device must be stimulated in dynamic operation. To extract the thermal cutoff frequency of these components, which is in the range of few MHz [80], the evolution versus frequency of the Y or H-parameters are commonly used as temperature sensitive parameters and therefore used in the  $Z_{th}$  calculation [57], [80], [81]. In our case  $Y_{22}$  is found to be among the most sensible temperature parameters and therefore chosen to tune the elements of the proposed three poles recursive networks (this parameter can be demonstrated to be directly proportional to  $Z_{th}$ , as detailed in section 2.6), obtaining all the values for  $R_{th}$  and  $C_{th}$  presented in Figure 3.17 and Figure 3.18.

In Figure 3.20, is shown the magnitude versus frequency of  $Y_{22}$  for the two test-structures under study at the DC bias point where the maximum variation of  $I_C$  was found: it is clear how the added metal stacks are able to lower  $|Y_{22}|$  as well as  $|Z_{th}|$  in the frequency range up to around 5MHz. The high frequency behavior is almost the same for the two test-structures, while the low frequency trend looks different: structure M6 has a lower cutoff frequency, so we can assume that some big thermal capacitances are added. From Figure 3.18 we see that the  $C_{th}$  of the BEOL part are much higher than those related to the lower part.

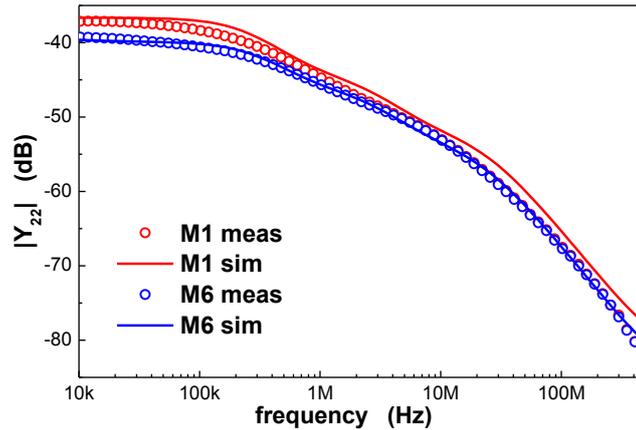


Figure 3.20: Magnitude versus frequency of the temperature sensitive  $Y_{22}$  parameter for  $V_{BE}=0.9V$  and  $V_{CE}=1.5V$ .

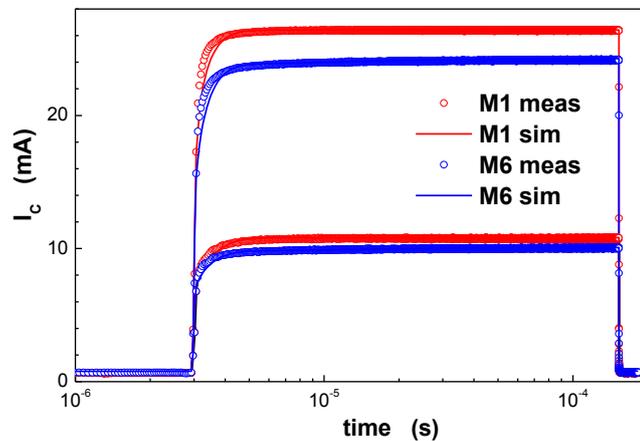


Figure 3.21: Measured and simulated  $I_C$  versus time for  $V_{CE}=1.5V$ ; on-voltages of the pulse signal  $V_{BE}$  are  $0.9V$  and  $0.95V$ ; x axis is in log scale to better evidence the evolution of  $I_C$  versus time.

### 3.6.3 Pulsed measurements

Time domain measurements are performed, to further verify the proposed model: the device is constantly biased on the collector, while on the base a voltage pulse is generated using a Keithley 4200 containing a 4225-SCS module. Figure 3.21 shows the  $I_C$  that is measured on test-structure M1 and M6 for different amplitudes of  $V_{BE}$ . At the instant when the pulse is applied,  $I_C$  exhibits a quick increase (corresponding to an initial fast electrical response) followed by a slow increment due to the much slower thermal time constant. We notice also that for test-structure M6 the  $I_C$  increase is much slower than M1, due to the big  $C_{th}$  that are added; besides the steady state  $I_C$  value is lower for M6 due to less self-heating (lower  $R_{th}$ ). The simulation provides a good reproduction of these thermal phenomena. The corresponding temperature evolution that is simulated using the HiCuM model connected to the proposed thermal network is shown in Figure 3.22. It can be observed that the simulated  $T_j$  follows the same evolution of the  $I_C$ , since it is the

device temperature itself which is responsible for the slow variation of  $I_C$  in pulsed operation.

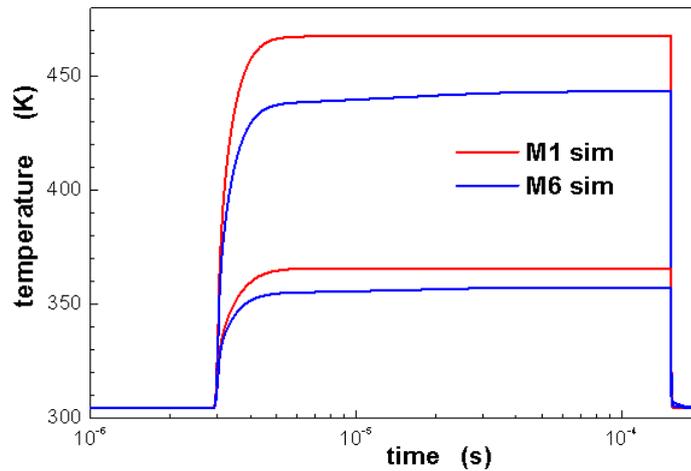


Figure 3.22: Resulting temperature evolution from the simulation of the HiCuM model using the proposed thermal networks in the same bias conditions detailed in Figure 3.21.

### 3.6.4 Large signal two tones simulations

Finally, once the thermal models have been calibrated upon measurements, they are used to simulate the behavior of the two transistor structures under a two tones excitation; the setup that is considered is the same which has been presented in section 2.8, where it has been discussed about how the low frequency envelope of the power dissipation can modulate the  $T_j$  of the transistor. The bias conditions are:  $V_{BE}=925\text{mV}$  and  $V_{CE}=1.5\text{V}$ , the two input frequencies are set to  $f_1=1\text{GHz}$  and  $f_2=1\text{GHz}+df$  and the power of both is  $-20\text{dB}$ .

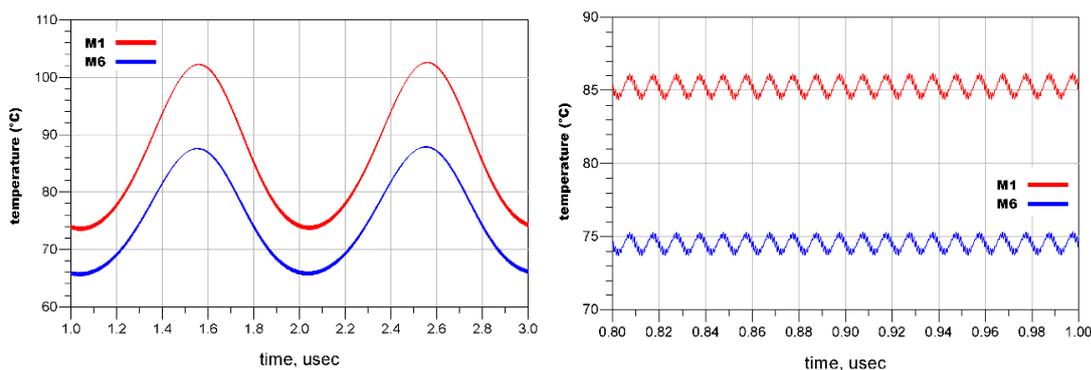


Figure 3.23: two tones large signal simulations on the M1 and M6 transistors for two different values of the tone spacing: (left) 100kHz and (right) 100MHz

In Figure 3.23 it is shown the temperature evolution simulated by the HiCuM model for both M1 and M6 when the frequency spacing between the tones ( $df$ ) is of 100kHz (left) and 100MHz (right). As it is expected, the temperature of M6 will be lower, due to the effect of the  $R_{th}$  decrease; moreover it can be noticed that, for  $df=100\text{kHz}$ , the temperature

excursion (the difference between the maximum and minimum temperature reached) caused by the envelope of the power dissipation is higher for M1 than for M6 (30°C versus 22°C respectively); in the case of  $df=100\text{MHz}$ , instead, the temperature excursion appears the same for both structures (around 2°C of excursion). This effect is justified by the fact that, when the structures are stimulated by a power dissipation envelope having a low frequency, the big thermal capacitances that are added due to the BEOL contribution help to keep the temperature of the transistor more stable; when instead the  $df$  increases, these high value  $C_{th}$  do not contribute any more. In this situation the dynamic thermal behavior in the two structures becomes comparable and a much smaller thermal variation of 2°C is simulated for both transistors; this is also confirmed by a comparison of the  $Z_{th}$  measured on the two transistors in Figure 3.25.

### 3.7 Static and dynamic thermal characterization

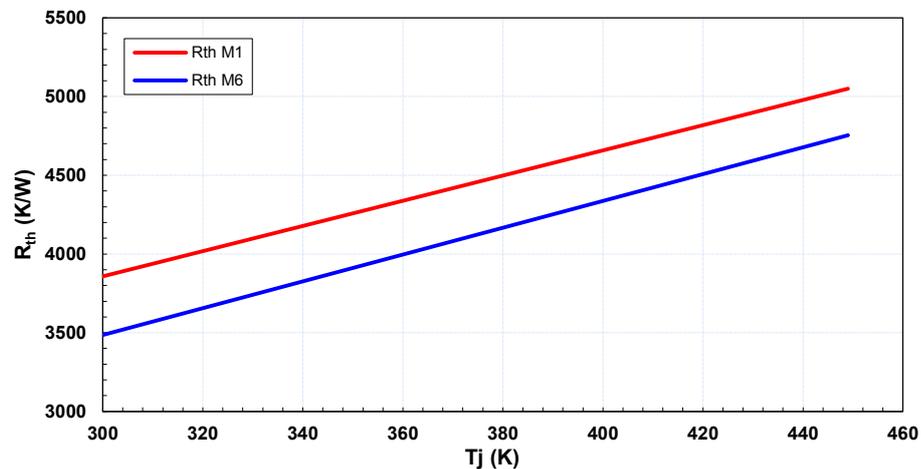


Figure 3.24:  $R_{th}$  versus  $T_j$  for the test structures M1 and M6.

For the two presented test structures an  $R_{th}$  extraction is performed, as described in section 2.5. The resulting  $R_{th}$  are plotted in Figure 3.24; it is shown that, for this geometry, the addition of metal-6 on the emitter contact leads to a decrease of the transistor  $R_{th}$  of around 10%. Regarding the dynamic thermal characterization, instead, the thermal impedance  $Z_{th}$  is extracted from low frequency S-parameters in the range from 10kHz-1GHz and is reported in Figure 3.25; it is shown that the  $Z_{th}$  of test structure M6 is lower at low frequency, but as the frequency increases, the difference among the two test structures is always lower, till around 3MHz, the frequency starting from which the  $Z_{th}$  shows the same trend for both M1 and M6. In fact, as shown in Figure 3.18, the presence of metal upon the emitter contact has been modeled with the addition of thermal capacitances of high value in parallel to the  $R_{th}$  and  $C_{th}$  that model the thermal behavior of the lower part of the transistor (which is the same for both the M1 and M6 test structures). These added capacitances are thus responsible for the thermal behavior at low frequency till around 3MHz, but increasing the frequency of the stimulus (represented, in our study, by the

power dissipated in the component) the metal in the BEOL does no more respond thermally, it is rather the silicon in the region of the FEOL surrounding the heat source that determines the  $Z_{th}$ . This justifies also the behavior observed when a two tones signal is applied to the two transistors: at 100kHz a significant difference is observed among the  $Z_{th}$  of the two HBTs, whereas at 100MHz the thermal impedance is the same.

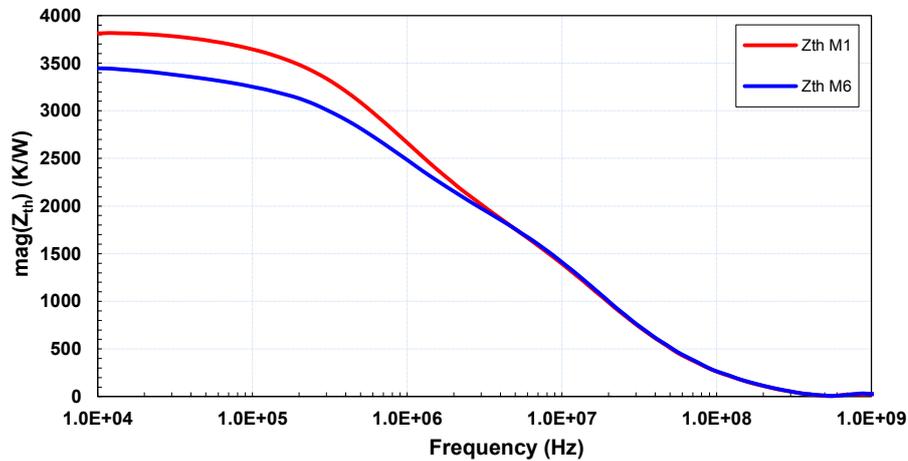


Figure 3.25: measured thermal impedance  $Z_{th}$  in the range 10kHz - 1GHz for the test structures M1 and M6.

To have an alternative insight in the dynamic spreading of the heat through the copper metallization, we can consider a very simplified situation: let us assume the case of a copper block having a sufficiently high thickness and an initial uniform temperature  $T_0$ ; when a power dissipation is applied at one side, eventually the whole material will reach a higher temperature  $T_1$ . But before this happens, that is, as long as the temperature of the other side of the block is still  $T_0$ , we can talk about thermal penetration. In thermoacoustics the thermal penetration depth ( $\delta$ ) can be defined as the distance that the heat diffuses through the material during a time  $1/f$  [82] and is approximated with the expression:

$$\delta = \sqrt{\frac{k}{\rho C_L \pi f}} \quad \text{Eq. 3.1}$$

where  $\kappa$ ,  $\rho$  and  $C_L$  are, respectively, the thermal conductivity, density and lattice heat capacity of the material. From Eq. 3.1, in the case of copper, we obtain a  $\delta$  of  $3.5\mu\text{m}$  at 3MHz, which means that, in this simplified hypothesis and at this frequency of operation, the thermal penetration corresponds approximately to the vertical abscissa of the metal-3 layer (in the case of the technology under study), whereas the volume of copper that is present above this layer does not participate in the dynamic thermal phenomena. As the frequency increases the  $\delta$  decreases further, and thus an always smaller volume of copper is involved in the determination of the  $Z_{th}$ .

### 3.8 3D TCAD thermal simulations

To evaluate the heat diffusion mechanisms in the proposed test structures, 3D numerical simulations are performed using Sentaurus device simulator. The temperature distributions due to device self-heating are calculated by solving the heat flow equation:

$$C_L \frac{\partial T}{\partial t} - \nabla \cdot k \nabla T = q \quad \text{Eq. 3.2}$$

where  $T$  represents the temperature and  $q$  is the power generated by the heat source. In the proposed simulations the heat source is placed at the BC junction of the device (the 3D TCAD simulator only allows the use of planar heat sources).

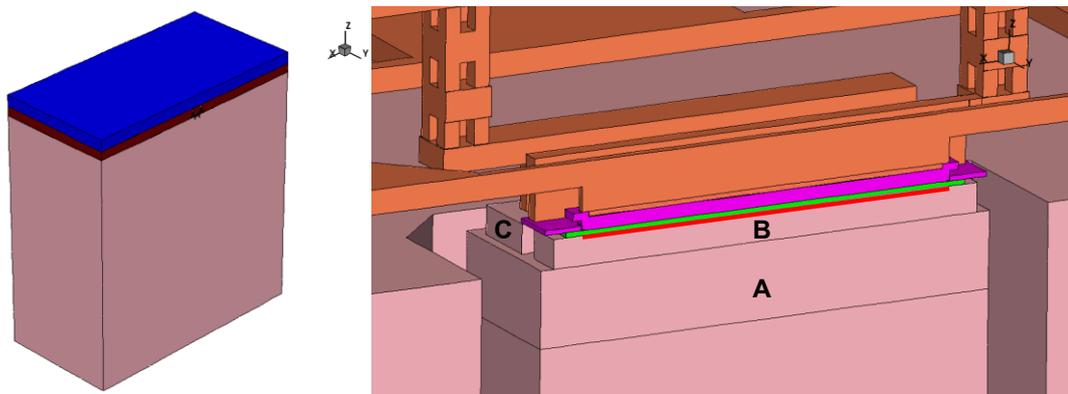


Figure 3.26: (left) the structure simulated in Sentaurus TCAD environment: silicon is represented in pink, SiO<sub>2</sub> in brown, copper in orange and the air layer is colored in blue. (right) zoom in the active part of the transistor: polysilicon is colored in magenta, SiGe in green and the heat source is highlighted in red, whereas SiO<sub>2</sub> is hidden for better visibility; the buried layer is indicated with the letter A, the selectively implanted collector (SIC) with B and the collector sinker with C.

The simulated transistor structure is placed on a silicon substrate which is 300μm thick; since the whole structure is symmetric with respect to the xz plane, only half of the device is considered (see Figure 3.26 and refer to Figure 3.16 for a more detailed reproduction of the metallization in the two test structures). To reproduce the same thermal conditions than during the measurements, the boundary conditions defined in the simulation environment are:

- The boundary surfaces of the silicon block are adiabatic, i.e. there is no heat flow to the surroundings.
- The wafer back-side is isothermal and initially kept at ambient temperature (300K). This is considered as the thermal ground.
- A thin air layer (15μm thick) is present above the oxide passivation. Within this layer there is no particle movement (laminar sub-layer) due to the fluid viscosity and the convection mechanisms can be neglected, considering just thermal conduction [83].
- An isothermal boundary condition is considered above the thin air layer; the temperature is set to 300K.

### 3.8.1 Thermal parameters and doping dependence

Thermal simulations are usually performed by setting the thermal conductivities  $k$  of the materials equal to the values measured from bulk undoped samples (listed in Table 3.2).

Material	Thermal conductivity (K) [W/cm K]	Heat capacity (C <sub>p,v</sub> ) [J/cm <sup>3</sup> K]
SiO <sub>2</sub>	0.014	1.67
Silicon	1.54 (at 300K)	1.63
Copper	3.85	3.42
Polysilicon	1.50	1.63
SiGe	Si:1.54; Ge:0.6	Si:1.63; Ge:1.67

Table 3.2: Thermal properties of the materials used for TCAD simulations in the case when the impact of doping is not considered

Region	Material	Doping considered [atoms/cm <sup>3</sup> ]	Thermal conductivity ( $k$ ) [W/cm K]
Y-shaped emitter	Polysilicon	$1 \cdot 10^{21}$ (Arsenic)	0.15
Base contact	Polysilicon	$6 \cdot 10^{20}$ (Boron)	0.5
Base	Si <sub>0.8</sub> Ge <sub>0.2</sub>	$6 \cdot 10^{20}$ (Boron) for Si	0.08
SIC	Silicon	$1 \cdot 10^{19}$ (Arsenic)	1.1
Buried layer	Silicon	$1 \cdot 10^{20}$ - $5 \cdot 10^{19}$ (Arsenic)	0.45 – 0.75
Collector sinker	Silicon	$1 \cdot 10^{21}$ (Arsenic)	0.15

Table 3.3: Thermal conductivity used in the regions of the transistor where a high doping concentration is present

However, in state of the art technologies, high values of doping are reached in some well-defined regions within the transistor and this can yield a local change of the thermal properties of the material, especially the thermal conductivity  $k$  [34]. It must be taken into account that the doping profile information is often protected by strict confidentiality and that few experimental data is available in scientific literature about the change of the thermal properties with the doping concentration. For this reason, a standard but realistic doping profile is assumed for the technology under study and the values of thermal conductivity  $k$  are modified according to the data published in [84] for what concerns silicon and in [85] for what concerns polysilicon; furthermore the same temperature dependency of  $k$  than undoped silicon is assumed in the regions where a lower  $k$  is considered due to the high doping concentration. At this point, to evaluate the impact of the doping profile on the thermal behavior of the transistor, three different cases are studied and compared to the measured results: (i) the default  $k$  used in Sentaurus

environment is employed for all the materials, without taking into account the thermal impact of the doping (as reported in Table 3.2); (ii) the  $k$  is changed in the regions of the transistor where a high level of doping concentration is present, according to the values shown in Table 3.3 and considering  $k=75$  W/cmK for the buried layer; (iii) the  $k$  in the different regions is changed according to the values shown in Table 3.3, using  $k=45$  W/cmK for the buried layer. The different regions of the transistor considered can be identified in Figure 3.26.

In Figure 3.27 and Figure 3.28 is reported the temperature profile and the heat flux in the two structures when a static power dissipation of 40mW is applied to the heat source (a  $k=45$  W/cmK is considered for the buried layer). It is clear how the metal stacks placed upon the transistor play an active role in its thermal behavior, allowing an alternative path for the heat flow and thus lowering the temperature that is reached in the active region.

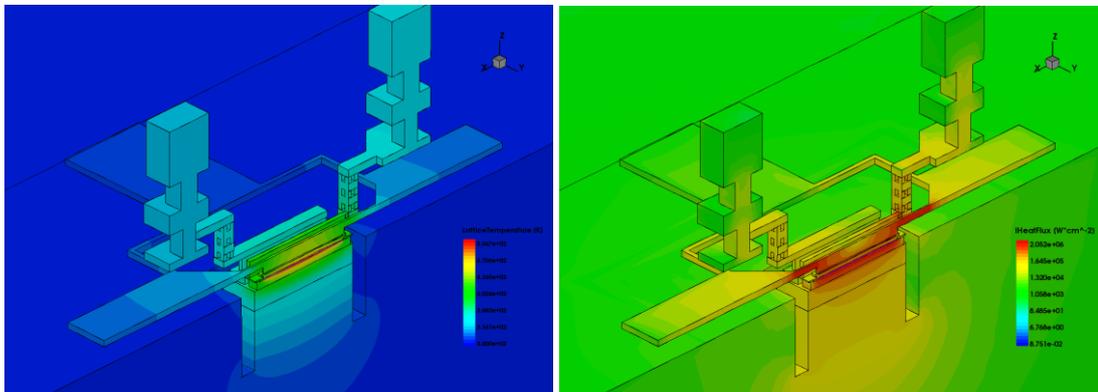


Figure 3.27: (left) thermal profile and (right) heat flux for the M1 structure when  $P_{\text{diss}}=40\text{mW}$  and the effect of the doping concentration on the thermal conductivity  $k$  is taken into account, considering  $k=45$  W/cmK for the buried layer.

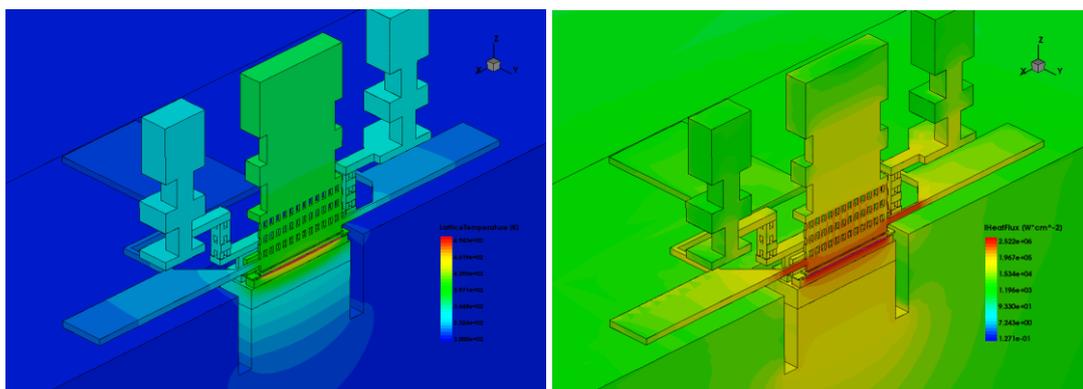


Figure 3.28: (left) thermal profile and (right) heat flux for the M6 structure when  $P_{\text{diss}}=40\text{mW}$  and the effect of the doping concentration on the thermal conductivity  $k$  is taken into account, considering  $k=45$  W/cmK for the buried layer.

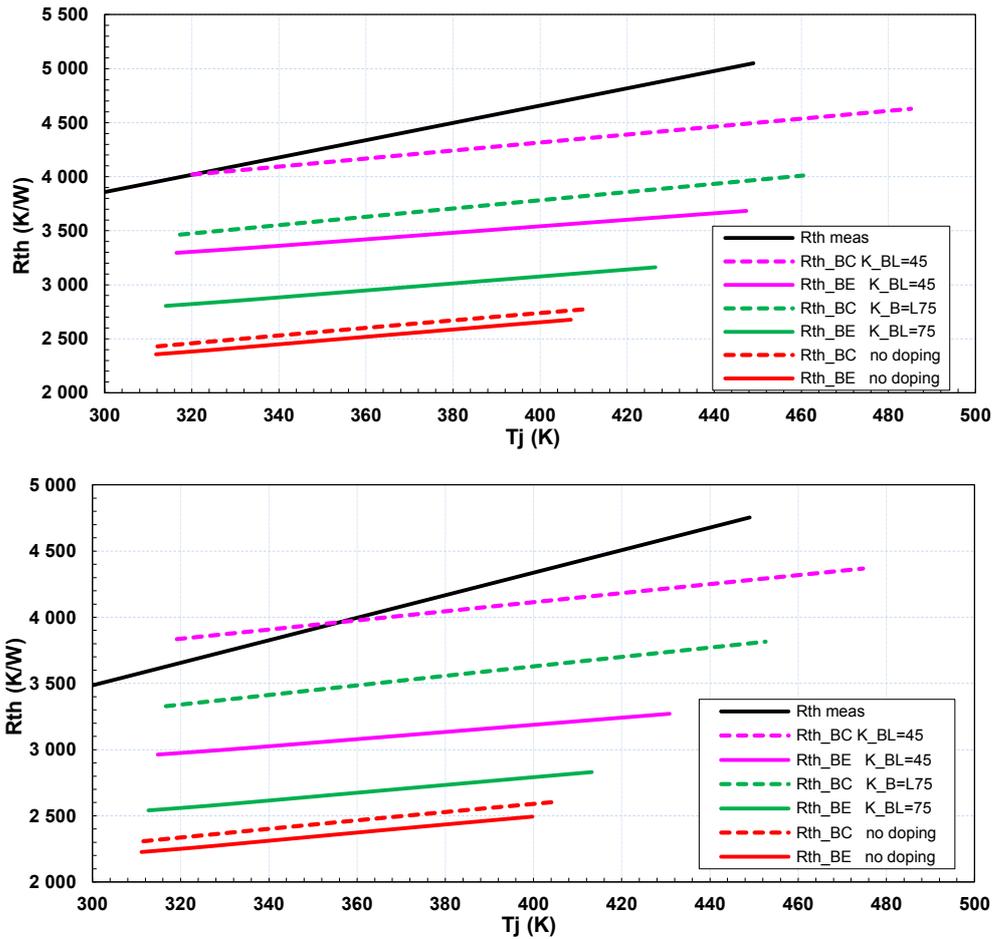


Figure 3.29: thermal resistance  $R_{th}$  for the test structures M1 (top) and M6 (bottom); comparison between measurements and TCAD simulations, for which the impact of the doping profile is taken into account. The dotted lines show the  $R_{th}$  evaluated considering as  $T_j$  an average temperature in a volume centered at the BC junction; the solid lines instead represent the case when a volume centered at the BE junction is considered.

In Figure 3.29 the measured  $R_{th}$  is compared to the results extracted from the TCAD simulations for test structure M1 and M6. The  $R_{th}$  is obtained by the simple expression  $P_{diss}/T_j$ , but two distinct cases are examined: in one case (i) the  $T_j$  is considered as the average temperature in a volume centered at the BC junction, which may seem the more obvious solution, since it is in this region that the heat source is placed. A rigorous extraction of the  $R_{th}$  from TCAD simulations, though, should consider that the temperature is evaluated as an average at the BE junction, since it is its temperature dependence which influences the electrical behavior of the transistor; so in the second case (ii) the  $T_j$  is considered as the average temperature in a volume centered at the BE junction. The comparison of the two different cases shows that, since a poor  $k$  is used for the SiGe layer, the  $R_{th}$  calculated with the two different methods can be quite different and thus the error introduced can be considerable.

It is evident how neglecting the impact of the  $k$  decrease in the regions with high doping concentration leads to an underestimation of the  $R_{th}$ ; furthermore a certain mismatch is observed in the slope of the  $R_{th}$  versus  $T_j$ , which can be attributed to a change in the

temperature dependency of  $k$  in the regions of the device which are highly doped. No experimental data seem to be available in literature about this phenomenon.

In order to simulate the  $Z_{th}$  as function of frequency in the TCAD Sentaurus, a sinusoidal power dissipation is applied to the heat source at different frequencies and the magnitude and phase shift of the temperature are evaluated after 10 complete cycles of the sinusoid, to attain a stable dynamic variation of temperature, as described in [86]. The results for the  $Z_{th}$ , normalized in the interval (0,1) are shown in Figure 3.30 for the M1 and M6 structures. It is shown that, considering a lower  $k$  for the highly doped regions of the transistor increases the overall  $Z_{th}$ , providing results closer to the experimental measurements.

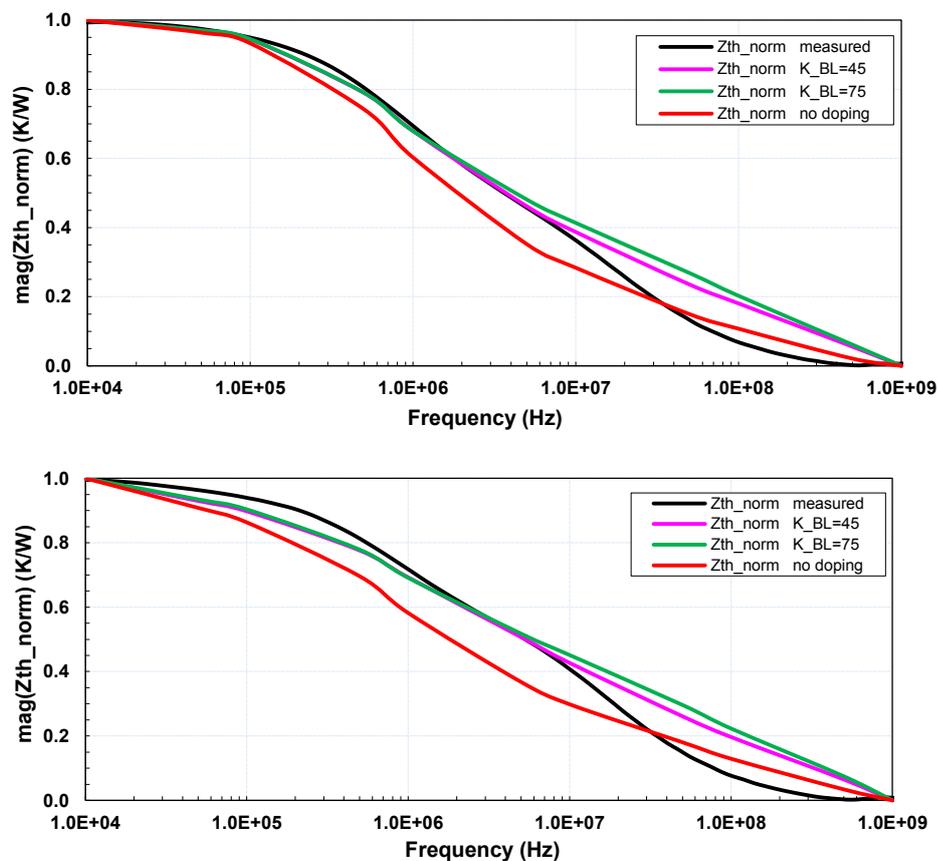


Figure 3.30: magnitude of the normalized thermal impedance in the range 10kHz - 1GHz for test structures M1 (top) and M6 (bottom); comparison between measurements and TCAD simulations

### 3.9 Conclusion

In this chapter we have presented a complete electro-thermal characterization of innovative transistor structures realized in a state of the art HBT process; the test structures are designed in a way to exploit the benefits of the metal in the BEOL. It has been demonstrated that the mechanical stress, as well as the positive thermal impact caused by the presence of additional metal stacks above the HBT are the main reasons for the enhanced DC and RF characteristics that have been reported at both small signal and

### *Chapter 3*

#### **Impact of BEOL in single finger devices**

large signal. Furthermore it has been shown that gradually increasing the width of the metal bars that are added upon the emitter can yield an overall increase of the aforementioned beneficial effects.

Moreover a compact model is presented to take into account the impact of the BEOL metallization on the thermal impedance; the model is based on a recursive RC network and can be connected to the thermal node of the HiCuM model. Its parameters have been calibrated with DC and low frequency S-parameters measurements. The model is validated with pulsed measurements and found to simulate with a good accuracy the time evolution of  $I_C$ . It has been also demonstrated by means of TCAD simulations and experimental dedicated measurements that the metallization in the BEOL has a significant impact on the  $C_{th}$  of the transistor, thus sensibly slowing down its thermal response; it could be of interest to take into account its impact into circuit simulators in the design phase in some circuit applications where the transistor is operated in pulsed conditions.

Finally, the doping dependency of the thermal behavior in different regions of the transistor is analyzed in Sentaurus TCAD simulator. It is shown that the high doping concentrations, which is present in some specific regions of the intrinsic part of the transistor can have a non-negligible impact on the simulated  $R_{th}$  and  $Z_{th}$  and is therefore recommended to take it into account to obtain more realistic results.

# Chapter 4

## Impact of BEOL and transistor layout change in multi-finger devices

### 4.1 Introduction

SiGe HBT of the most advanced technologies realized in a multifinger configuration are very attractive for the design of circuits for applications demanding high power at very high frequencies, due to the small base access resistance and since they allow a better current handling capability and an improved thermal dissipation. These active components, though, suffer from an uneven thermal distribution among the different emitters, when operated at high power, which can lead to thermal instability and eventually to the device failure, as will be further discussed.

It is therefore of interest to propose innovative transistor topologies, which can allow the transistor to withstand high powers without degrading its electrical performances, thus improving its safe operating limits; to achieve this, in this chapter some specially designed multifinger transistor topologies are presented. These test structures exploit the same benefits of a careful design of the BEOL metallization reported in Chapter 3; in addition the effect of modifying the layout of the drawn emitter window is analyzed. For this set of test structures a complete DC and AC characterization, as well as an extraction of the  $R_{th}$  and  $Z_{th}$  is proposed, using the same approach than in Chapter 3.

### 4.2 Improving thermal stability in multifinger transistors

Some recent works have been published on the study of inter-device thermal interactions in multifinger transistors of advanced state of the art technologies; in particular, the attention has been focused on mutual thermal coupling effects between the different fingers in static [87]–[89] and dynamic [65] operation, leading to an unbalanced thermal distribution in the structure, with the central fingers reaching the highest temperature [40]. Because of the positive electro-thermal feedback in these components, hotter fingers drive more current, inducing an electro-thermal loop, which (along with the impact ionization effect) degrades the performances and can eventually lead to instability and device failure. Instability is limited by the fly-back behavior of the collector current when biased in common emitter configuration and excited with a base-emitter voltage ( $V_{BE}$ ) [38], [90], [91].

One of the possible approaches to improve the thermal stability in multi-finger HBTs is the use of ballasting resistors [42], but this solution leads to degradation of the output power and of the power-added efficiency (PAE) of the transistor. Alternative techniques

that aim at a better thermal stability, avoiding the formation of hot spots have been proposed in literature [92], [93] and essentially advocates for increasing the spacing between the central emitter fingers to reduce their mutual thermal coupling or reducing the length of the central fingers, to yield a lower heat generation in that region.

The realization of heat spreaders in the BEOL is a commonly used technique in some silicon technologies, like in 3D integrated circuits [74], [94]. In Chapter 3 the possibility of improving the electro-thermal behavior of SiGe HBTs exploiting the benefits of the metallization in the BEOL has been already discussed; this can be seen as an interesting way of pushing the overall power handling capability of the transistor, without degrading its RF performances.

In this chapter, two different approaches are separately investigated, in order to improve the transistor's electro-thermal behavior, with an electrical and thermal characterization of a certain number of test-structures. We essentially propose some dedicated test-structures where the transistor is modified in the horizontal plane acting on the layout or in the vertical plane, adding metal dummies.

### **4.3 Description of the test structures**

We designed and realized seven different test structures in ST Microelectronics BiCMOS 55nm technology. Each structure consists of a five fingers SiGe HBT having a CBEBE arrangement for the contacts. The multi-finger transistors are connected in a common emitter configuration and the base and collectors are accessible from the pads that are realized in a GSG configuration to avoid oscillations.

As previously stated, two different approaches are adopted in order to observe a possible improvement in the thermal behavior of the transistors: (i) changing the emitter layout, that essentially modifies the structure of the transistor in the horizontal plane just below the metal-1 contact (referred to as HL transistors) and (ii) adding metal stacks in the vertical plane (referred to as VM transistors). In the former set, we modify the active part of the transistors, whereas the latter only implies a change in the metallization keeping the active transistor unaltered.

Figure 4.1 shows a 3D reproduction of the VM test-structures: the metal stacks placed above the emitters are up to metal-3 for test structure VM3 and are colored in violet; the metal stacks colored in red instead represent the metal dummies that have been added up to metal-8 (for structure VM8), while considering just the stacks up to metal-6 will represent structure VM6. For a more complete study on the impact of the BEOL another structure named VM1 has been also realized, where the metal stacks metal-2 and metal-3 have been removed, and so the emitter is electrically connected to ground by using just metal-1. The base and collector are represented by green and blue color on Figure 4.1, respectively, and they are connected at the metal-8 level to transmission lines (not shown

in the figure), while the emitter is connected to the guard ring, and then to a ground plane (partially visible).

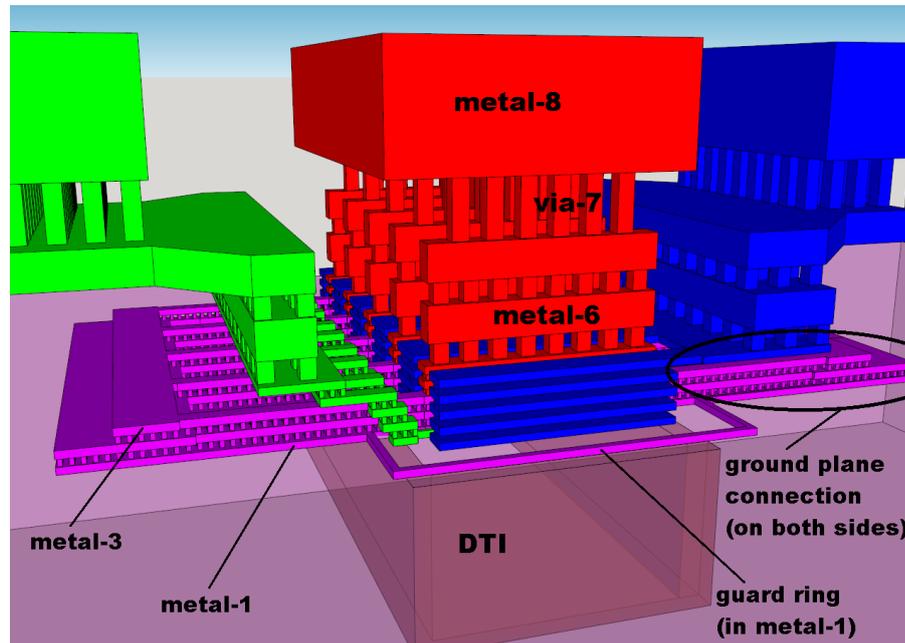


Figure 4.1: 3D image of the 5 fingers transistor in CBEB configuration. The colors of the metals are: green for the base connections, blue for the collector, violet for the emitter. The metal dummies are colored in red.

The principle behind these test structures is that the BEOL metallization located upon the emitter contacts can allow an alternate path for the heat flux. In fact, as showed in Table 1, copper has the highest thermal conductivity in a transistor structure, and its presence can help to vehicle the heat flux vertically, thus reducing the  $R_{th}$ .

Material	Thermal conductivity (K)	Heat capacity (Cp,v)
SiO <sub>2</sub>	0.014 W/cm K	1.67 J/cm <sup>3</sup> K
Silicon	1.54 W/cm K at 300K	1.63 J/cm <sup>3</sup> K
Copper	3.85 W/cm K	3.42 J/cm <sup>3</sup> K

Table 4.1: Comparison of the thermal properties of the materials that influence the most the thermal behavior of a transistor: silicon dioxide, silicon and copper.

For all the seven presented test-structures (except for VM1) metal-2 and metal-3 layers have been used in parallel to metal-1 to provide a more robust connection to ground for the emitter (according to the reliability rules specified in the B55 design manual). These connections participate also in a positive way in the thermal dissipation, as will be shown.

Test structures HL1, HL2 and HL3 aim at a more uniform temperature distribution across the emitter fingers using different strategies. In fact, multi-finger HBTs suffer from

thermal imbalance due to the thermal coupling between the heat sources and the presence of deep trench isolation (DTI) [40], [92].

In test structure HL1 (its finger layout is reported in Figure 4.2b) the three central fingers are designed shorter than the two side ones; in this way the thermal dissipation in the center of the structure is lower than in the sides, but the length of the emitters is non-uniformly distributed, so that the same total emitter area ( $A_E$ ) as that of the VM structures is guaranteed. This implies an enlargement of the DTI enclosed area ( $12.75 \times 6.81 \mu\text{m}^2$ ) compared to the VM structures ( $12.75 \times 5.63 \mu\text{m}^2$ ).

In test structures HL2 and HL3 (refer to Figure 4.2c and Figure 4.2d), the length of finger-1 and finger-5, is kept the same ( $5\mu\text{m}$ ) but the length of fingers 2, 3 and 4 is reduced to  $3.91\mu\text{m}$ , to yield less power dissipation and thus a lower temperature in the center of the structure. For this reason, the total  $A_E$  is slightly lower than the other structures ( $3.9\mu\text{m}^2$  instead of  $4.5\mu\text{m}^2$ ), but the DTI enclosed area is the same as that of the VM test structure. In the case of HL3, this reduction has been realized with emitter segmentation [38], [95]. Note that all the dimensions reported refer to the drawn emitter window.

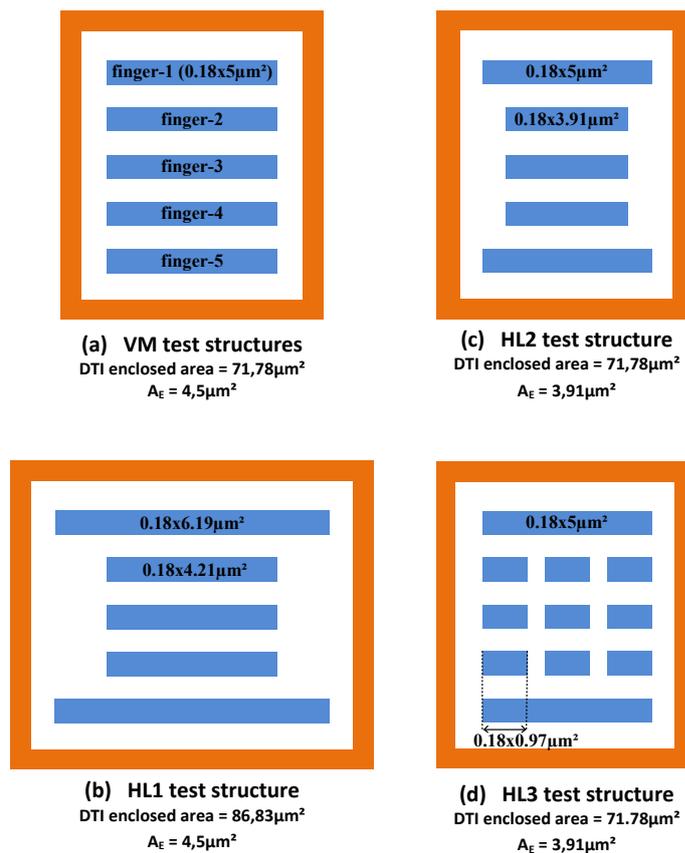


Figure 4.2: Finger layout of the test structures (the dimensions reported refer to the drawn emitter window). The DTI is depicted in orange, whereas the 5 drawn emitter windows are colored in blue.

## 4.4 DC electrical characterization

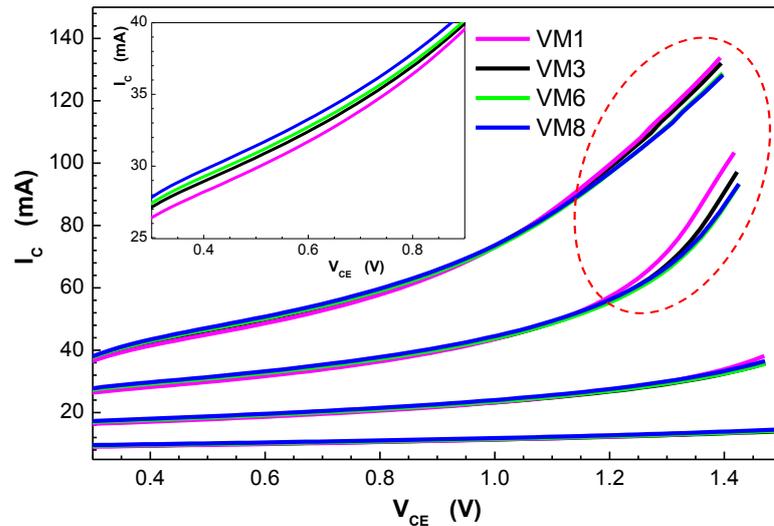


Figure 4.3 : Comparison of the output characteristics of the transistors VM. The  $V_{BE}$  is swept from 0.825V to 0.9V. The dotted circle highlights the region where power dissipation is more significant. The subplot shows a zoom-in in the medium  $V_{CE}$  range for  $V_{BE}=0.875V$  to show the impact of the mechanical stress.

A DC characterization of the structures has been done using a Keysight E5270B DC analyzer; the measurements are performed on a probe station equipped with a thermal chuck. Figure 4.3 shows the output curves measured at a chuck temperature  $T_{chuck}=320K$  for the VM test structures at different values of  $V_{BE}$ . The  $V_{CE}$  plotted on the x-axis takes into account the voltage drops on the parasitic resistances of the measurement setup, thus showing the effective output characteristic of the transistors. It is evident that, after a certain value of power dissipation ( $P_{diss}$ ), the transistors start to behave differently, due to a difference in the thermal resistances of each test structure. In fact, once a relatively high value of  $P_{diss}$  is reached (in the region of the plot highlighted with a dashed circle, where the total  $P_{diss}$  is estimated to range between 50mW and 190mW), a different value of junction temperature ( $T_j$ ) is reached, according to the thermal resistance of the component; once the  $T_j$  is high enough, it starts to affect with more intensity the electrical characteristics of the transistors. When driven by a base voltage (like in our measurement setup), the  $I_C$  of a transistor exhibits a positive electro-thermal feedback, thus increasing when more intense self-heating effects arise. This phenomenon is of course more intense if the  $R_{th}$  of the transistor has a high value. The value of  $V_{BE}$  for which the highest variation of  $I_C$  is noticed is for  $V_{BE}=0.875V$ ; if the base-emitter voltage is further increased other effects, like avalanche multiplication and impact ionization, as well as the feedback effect of the emitter resistance  $R_E$ , appear predominant with respect to self-heating effects, and so the observed  $I_C$  variations between the different test structures are smaller. The results we obtain for the  $I_C$  in the high power dissipation region show that passing from structure VM1 to structure VM8 leads to an  $I_C$  drop of around 12% at

the bias point  $V_{BE}=0.875V$  and  $V_{CE}=1.42V$ . This  $\Delta I_C$  is imputable to a lower  $R_{th}$  of transistor VM8 compared to VM1. No sensible  $I_C$  variation is noticed when passing from VM6 to VM8.

On the other hand we can notice in the sub-plot in Figure 4.3 that in the region at low  $V_{CE}$  of the output curves (where the power dissipation is quite lower), the test structure VM8 drains a slightly higher  $I_C$  than VM1 (an increase of 4.5% is observed at  $V_{BE}=0.9V$  and  $V_{CE}=0.6V$ ); this is due to the mechanical strain effects of the metal dummies, as described in [77]. In fact, the  $I_C$  variations caused by metal in the BEOL that are studied in [77] have been modeled as a change in the electronic bandgap structure (like that induced in the base by the germanium profile) and a bandgap energy variation  $\Delta E_g$  of around 9meV is showed when passing from a structure with no metal dummies to a structure with dummies up to metal-6. Making a similar comparison between our test structure VM1 and VM8 gives as a result a smaller variation of 2meV, but it must be considered that our proposed VM8 test structure has a less dense quantity of dummies when compared to the structures presented in [77].

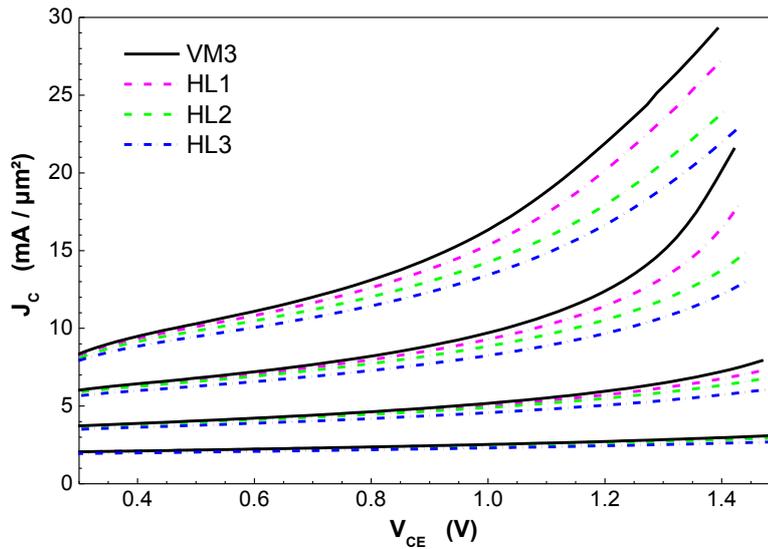


Figure 4.4 : Comparison of the collector current density  $J_C$  for the test structures HL; test structure VM3 is used as a reference. The  $V_{BE}$  is swept from 0.825V to 0.9V.

For what concerns the test structures HL, we will take into account transistors with two different  $A_E$ , so in Figure 4.4 we compare the measured current density  $J_C$  as a function of  $V_{CE}$  (the results for the reference structure VM3 are added as well). We see that, for the bias point corresponding to the highest  $P_d$  ( $V_{CE}=1.42V$  and  $V_{BE}=0.875V$ ), a  $J_C$  decrease of 18% is noticed passing from structure VM3 to HL1. At high power densities the structures HL2 and HL3 drain an even lower  $J_C$ , and so they seem to be favored from an electro-thermal point of view despite the fact that, because of their reduced  $A_E$  compared to VM3 they should have a higher  $R_{th}$ . This aspect will be further discussed in the following section.

An analysis of the output conductance ( $g_{out}$ ) is proposed in Figure 4.5, where it is plotted versus the measured  $I_C$ . We can deduce that, at high power dissipation, the value of  $g_{out}$  is lower as more metal stacks are added in the dummies above the emitters, thus ensuring an improved behavior for what concerns the safe operating area (SOA) specifications. In fact, in applications where the transistor must be operated in regions close to the edges of its SOA, it can be chosen to fix a maximum acceptable value for the  $g_{out}$  (corresponding to a maximum slope of the  $I_C$  in the output curves). Referring to Figure 4.5 it is easy to notice that, once a certain  $g_{out\_MAX}$  is fixed, the more we add metal stacks, the more it is possible to push the transistors with an extra  $V_{CE}$  (or, equivalently an extra  $I_C$ ).

For example if we fix  $g_{out\_MAX}=270\text{mS}$ , the maximum value of  $V_{CE}$  that we can apply to the transistor is 1.35V for VM1 and 1.43V for structure VM8, which allows an extra  $V_{CE}$  of around 6%. Instead if we consider  $g_{out}$  plotted as a function of  $I_C$  and we fix the same value for  $g_{out\_MAX}$ , an extra current of around 10mA (corresponding to an increase of 12%) can flow in the HBT of test structure VM8 compared to VM1.

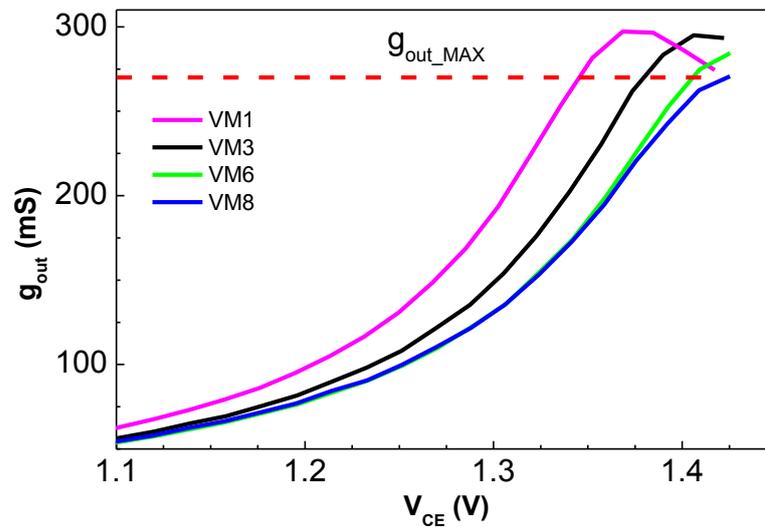


Figure 4.5: Measured output conductance ( $g_{out}$ ) as function of  $V_{CE}$  for the structures VM;  $V_{BE}=0.875\text{V}$ .

The results for the structures HL, as well as the reference structure VM3 are shown in Figure 4.6: in this case we compute the derivative of the  $J_C$  versus  $V_{CE}$  curve in Figure 4.4, obtaining

$$g_{out\_norm} = \frac{\partial J_C}{\partial V_{BE}} = \frac{\partial \left( \frac{I_C}{A_E} \right)}{\partial V_{BE}} = \frac{g_{out}}{A_E} \quad \text{Eq. 4.1}$$

In Figure 4.6 we also report as a reference  $g_{out\_norm\_MAX}$  corresponding to the  $g_{out\_MAX}$  shown in Figure 4.5. It is evident how the test-structure HL1 can improve the SOA specifications compared to the behavior of VM transistors; the test structures with reduced  $A_E$  can further improve this parameter.

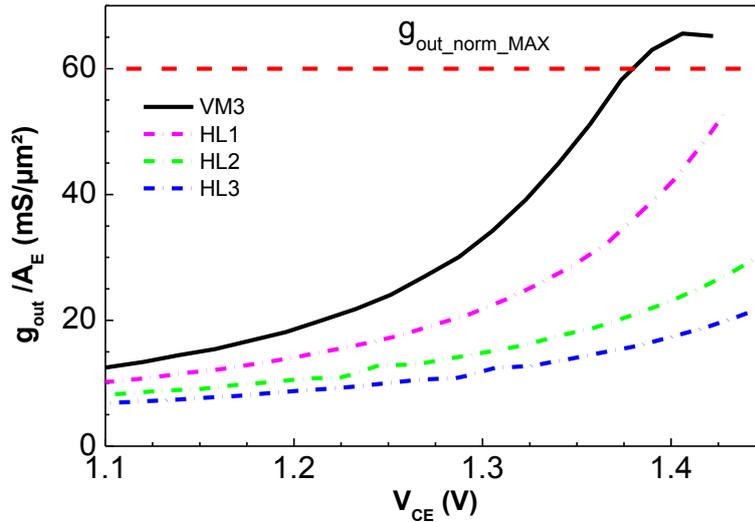


Figure 4.6: Measured  $g_{out\_norm}$  as function of  $V_{CE}$  for the structures HL;  $V_{BE}=0.875V$ .

A comparison of the  $I_B$  measured at different constant values of  $V_{BE}$  is presented in Figure 4.7 for the test structures having the same  $A_E=4,5\mu m^2$ : also in this case, in correspondence of the bias points suffering from intense self-heating, we notice an increase in the  $I_B$ , related to an increase of  $T_j$ . It is possible to notice that the increase of  $I_B$  due to self-heating is smaller as more layers of metal are added upon the emitter contacts; the lowest self-heating effect is found for test structure HL1.

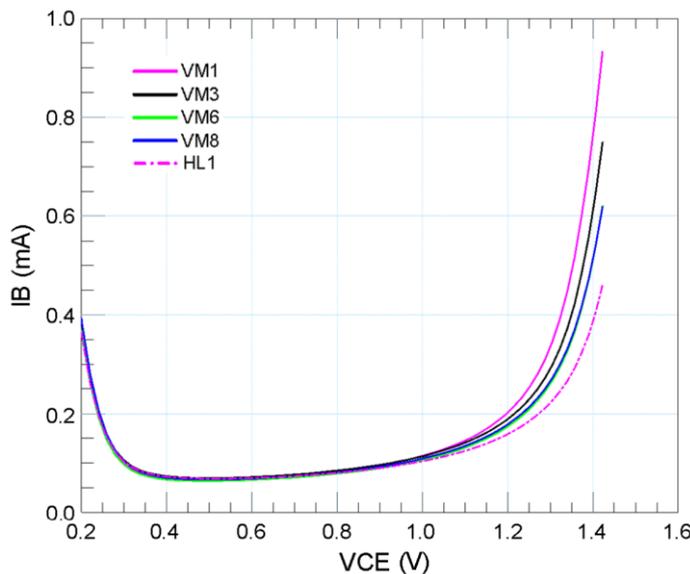


Figure 4.7: comparison of the  $I_B$  of the different transistors for  $V_{BE}=0.875V$ ; for clarity in this plot just 5 different test structures are compared. Refer to Table 4.2 for a complete comparison.

To conclude the DC analysis, the current gain  $\beta=I_C/I_B$  is plotted in Figure 4.8 for the same test structures presented in Figure 4.7; it is possible to notice that there is a sensible difference in  $\beta$  among the different transistors. As reported in [77], the  $\beta$  increase that is observed for the VM structures (especially for VM6 and VM8) is justified by the

mechanical stress of the metal dummies in the BEOL, which has been discussed above; on the other hand, when the devices are biased in the regions at high power dissipation, the higher  $\beta$  is also due to the effect of the  $R_{th}$  decrease, that will be discussed in the next section. This is visible also for test structure HL1, which presents the same  $\beta$  than VM3, except for the bias points at high  $P_{diss}$ , where it shows better performances due to its lower  $R_{th}$  (refer to Figure 4.11).

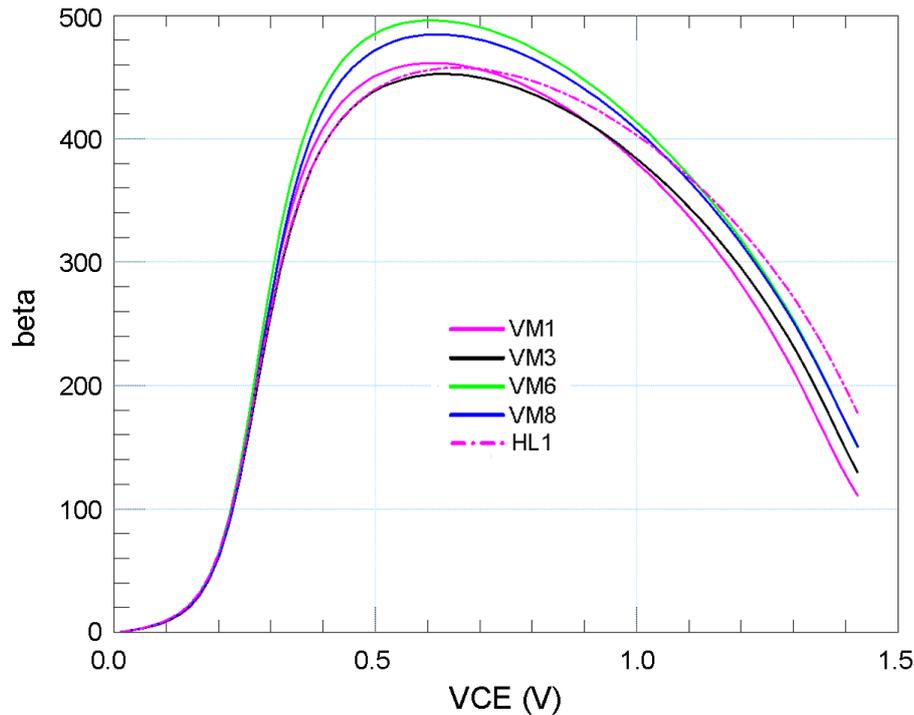


Figure 4.8: comparison of the current gain  $\beta$  between the test structures under study for  $V_{BE}=0.875V$ . Refer to Table 4.2 for a complete comparison between all the test structures.

Taking VM3 as a reference we deduce that if we move to structure VM1 (thus removing 2 metal stacks on top of the emitter) a higher  $T_j$  is reached for the transistor, thus increasing the measured  $I_C$  and  $I_B$ , but leading to a degradation of the current gain of around 18%. Adding metal stacks above metal-3 can improve this figure of merit by around 16%. No significant variation is noticed between test structure VM6 and VM8, since probably the thermal gradient that is obtained through the copper stacks above the emitter is not reaching the last levels of metal and so it does not lead to a sensible decrease of the thermal resistance of the transistor; this aspect will be further discussed in the next section. Among the test structures with  $A_E=4.5\mu m^2$  the more performing in the high power dissipation region is HL1, that presents a current gain around 42% higher than the test structure used as a reference VM3. In Table 4.2 it is presented an overview of the variations of the DC parameters among the different structures for  $V_{CE}=1.42V$  and  $V_{BE}=0.875V$  (the bias point where the maximum variation due to self-heating can be observed on the DC parameters); if the base voltage is further increased the effects of self-heating are less visible on the collector current, since other phenomena, like impact

ionization, avalanche multiplication and the feedback effect of the emitter resistance will be predominant.

Test structure	$A_E$	$\Delta J_c$ (%)	$\Delta I_c$ (%)	$\Delta I_b$ (%)	$\Delta \beta$ (%)
VM1	$4.5\mu\text{m}^2$	8.40	7.71	33.14	-17.85
VM3 (reference)	$4.5\mu\text{m}^2$	0.00	0.00	0.00	0.00
VM6	$4.5\mu\text{m}^2$	-4.72	-4.17	-17.86	16.30
VM8	$4.5\mu\text{m}^2$	-4.72	-4.17	-17.86	16.30
HL1	$4.5\mu\text{m}^2$	-18.40	-18.92	-42.14	42.52
HL2	$3.91\mu\text{m}^2$	-33.02	-42.35	-70.00	94.81
HL3	$3.91\mu\text{m}^2$	-41.04	-48.80	-75.71	113.33

Table 4.2 : comparison of the DC characteristics for  $V_{CE}=1.42\text{V}$  and  $V_{BE}=0.875\text{V}$ . All the relative variations have been calculated using VM3 structure as a reference. The structures highlighted in green have a reduced emitter area of  $3.91\mu\text{m}^2$  instead of the  $4.5\mu\text{m}^2$  of the other structures.

## 4.5 Thermal characterization

### 4.5.1 Thermal resistance extraction

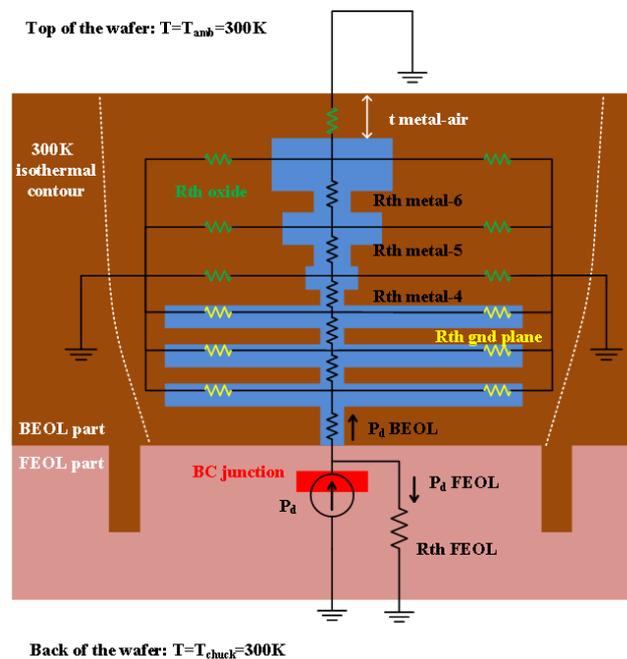


Figure 4.9: Schematic representation of the thermal resistances distributed across the whole back end of line; in this simplified representation just 6 levels of metal are shown.

In Figure 4.9 is represented how the  $R_{th}$  are distributed across the back end of line, to understand how the metallization can impact the thermal behavior of the transistor; regarding this aspect, for the VM transistors, the same considerations that have been made in section 3.3 apply here. An  $R_{th}$  extraction at constant  $I_C$  is realized using the method proposed in [52]. Figure 4.10 shows the extracted  $R_{th}$  as a function of the junction

temperature for the different test structures under study: all the resulting  $R_{th}$  increase linearly with  $T_j$  [96]. As expected, the VM1 structure exhibits the higher thermal resistance, besides we notice that its slope versus temperature is higher than the other structures. Furthermore, we can observe that the  $\Delta R_{th}$  between VM1 and VM3 is much higher than the  $\Delta R_{th}$  between VM3 and VM6 (see Figure 4.10).

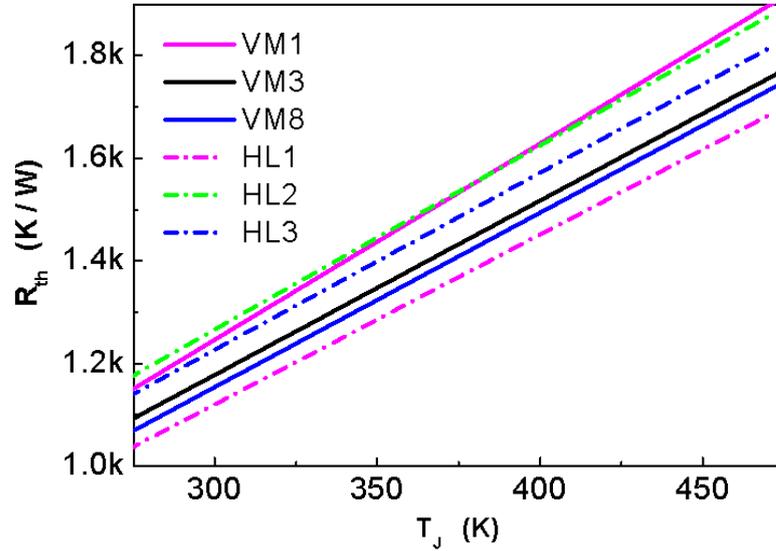


Figure 4.10:  $R_{th}$  extracted at constant  $I_C$  versus junction temperature for the different test structures under study.

This lets us deduce that most part of the thermal gradient is located in the first 3 levels of metal. The  $R_{th}$  of VM6 is found to be only slightly higher than VM8, and is therefore not shown for better visibility. This improvement of the thermal properties of the transistors VM explains the different electrical behavior observed in the regions of high power dissipation, as shown in Figure 4.3 to Figure 4.5. Test structure HL1 has the lowest  $R_{th}$  among the various structures compared: this is mainly due to the fact that the increase of the DTI enclosed area restricts the heat flux in a lower amount compared to the other structures.

From Figure 4.10, we see that test structures HL2 and HL3 show a higher  $R_{th}$  than the reference structure VM3 because their drawn  $A_E$  is smaller, as already discussed. To take into account the different  $A_E$  of the transistors under study we can consider, rather than the classical formulation for  $R_{th}$ :

$$R_{th} = \frac{T_j - T_{chuck}}{P_{diss}} = \frac{T_j - T_{chuck}}{V_{CE} \cdot I_C} \quad \text{Eq. 4.2}$$

an alternative formulation that considers power density as:

$$R_{th\_norm} = \frac{T_j - T_{chuck}}{\frac{P_{diss}}{A_E}} = \frac{T_j - T_{chuck}}{V_{CE} \cdot J_C} = R_{th} \cdot A_E \quad \text{Eq. 4.3}$$

The resulting  $R_{th\_norm}$  is reported versus  $T_j$  in Figure 4.11. Analyzing this parameter it comes out that the devices HL2 and HL3 can have better thermal properties than VM3, in fact for a fixed power density  $P_{diss}/A_E$  (or alternatively a fixed current density  $J_C$ ), devices with smaller  $A_E$  have a lower  $R_{th\_norm}$ . The reason is that the ratio between the DTI enclosed area (which represents the surface in which the heat flux is mostly confined) and the  $A_E$  (corresponding to the heat generation area) is larger for devices with a lower  $A_E$ . Instead when applying the same  $P_{diss}$ , devices with smaller  $A_E$  have a worse thermal behavior. Among the two proposed architectures with reduced  $A_E$  the emitter segmentation on the central fingers seems to yield better results than using a shorter length for the central fingers, confirming the results presented in [95].

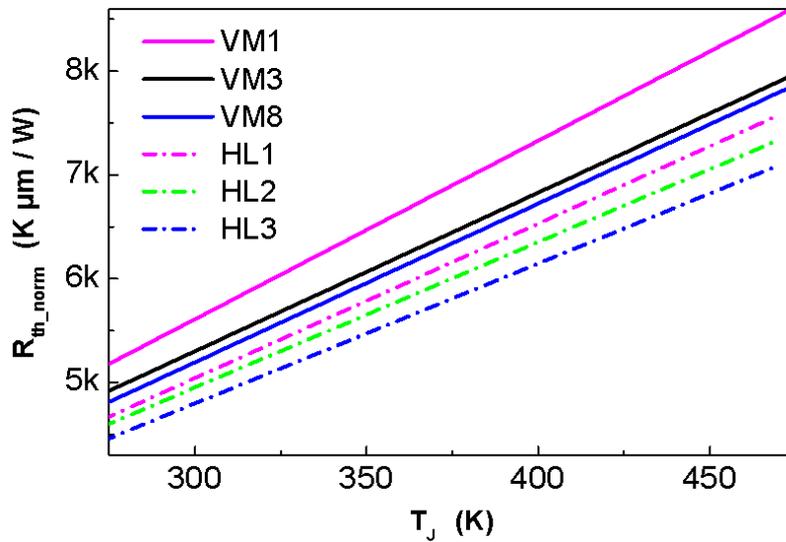


Figure 4.11:  $R_{th\_norm}$  versus junction temperature for the different test structures under study.

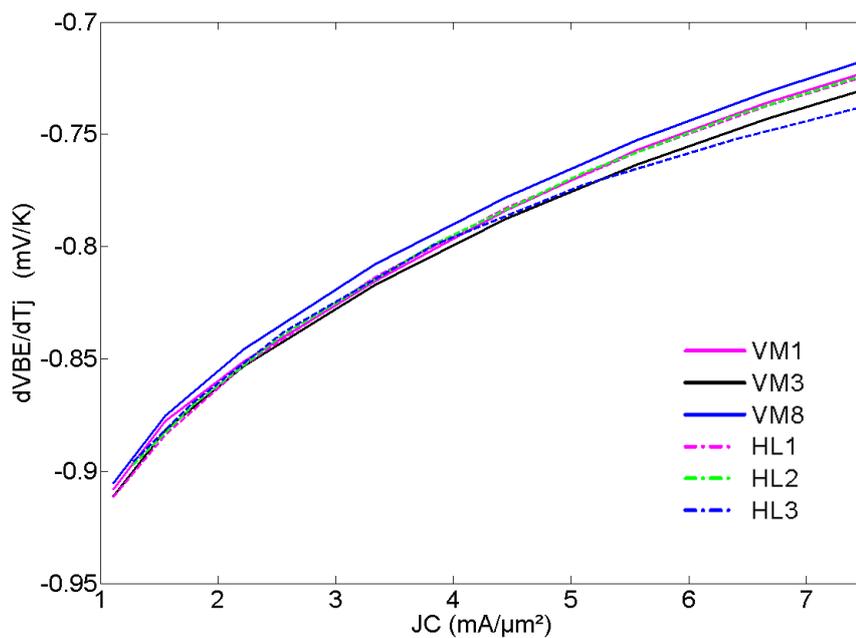


Figure 4.12:  $dV_{BE}/dT_j$  factor determined during the  $R_{th}$  extraction for the different test structures

It is also reported in Figure 4.12 the  $dV_{BE}/dT_J$  coefficient, which is determined during the  $R_{th}$  extraction procedure; this parameter characterizes the technology and does not depend on the transistor layout [52]. It is found, in fact, that this parameter does not vary (around 1% variation is observed) for the different transistor structures measured.

#### 4.5.2 Thermal impedance extraction

To evaluate the effects of dynamic self-heating the device must be stimulated using signals having a relatively low frequency. In fact, to extract the thermal cutoff frequency of these components, which is in the range of few MHz, the evolution versus frequency of the Y or H-parameters are commonly used as temperature sensitive parameters and therefore used in the  $Z_{th}$  calculation (refer to section 2.6). In Figure 4.14 are shown the extracted module of  $Z_{th}$  from low frequency S-parameters measurements in the range from 10kHz to 100MHz for the VM structures, whereas Figure 4.14 give the results for the HL structures. VM1 has a lower  $C_{th}$  than the others, but as we add more metal layers, an always higher capacitive effect is noted, till structure VM8, which has the highest  $C_{th}$ . It has been shown in [21] that the metal stacks of the BEOL are responsible for an increase of the  $C_{th}$  of the transistor, mainly caused by the higher heat capacity of copper compared to  $SiO_2$  (refer to Table 4.1).

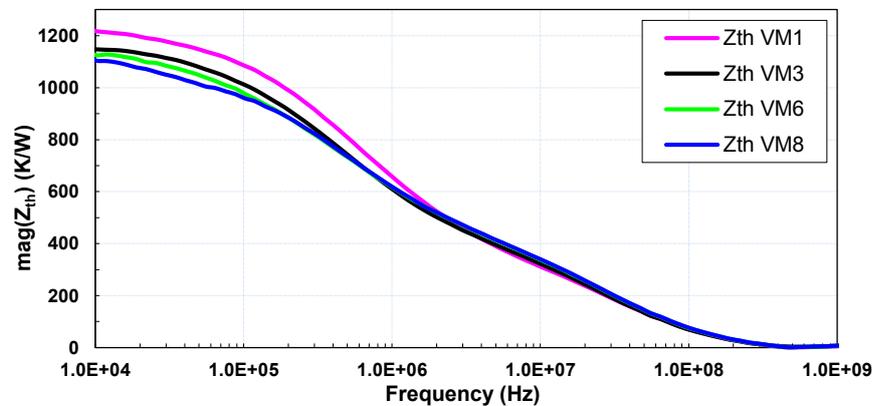


Figure 4.13: Extracted  $Z_{th}$  from low frequency S-parameters measurements for the VM test structures

By analyzing the behavior of the test structures versus frequency we can make some suppositions about how the heat flux is distributed in the different zones of the structures and the same considerations that have been made in section 3.7 for single finger transistors are valid also in this case. Because of the higher heat capacity of copper compared to  $SiO_2$ , the volume of metal that we put upon the heat source in our test structures VM3, VM6 and VM8 responds to thermal variations at low frequency, but when the frequency of the stimulus (represented, in our study, by the power dissipated in the component) increases, the copper does no more respond thermally, it is rather the silicon below the heat source that determines to the  $Z_{th}$ , and since the lower part of the device is the same for all the components considered, they tend to behave the same way

at frequencies above around 0.5~2MHz, as we can see in Figure 4.13. This behavior is comparable to what has been observed for the transistors that have been characterized in Chapter 3 (refer to Figure 3.25) and even the frequency at which the  $Z_{th}$  curves overlap is in the same order of magnitude.

For what concerns the thermal impedance of the HL structures (see Figure 4.14 on top), it is possible to notice that increasing the DTI enclosed area (case of the HL1 structure) yields a decrease of  $Z_{th}$  at low frequency; among the structures with reduced  $A_E$ , HL3 performs slightly better than HL2 from a thermal point of view and again their  $Z_{th}$  is shifted upwards compared to the other transistors, principally due to their increased  $R_{th}$ . If a normalization by the emitter area is again performed, the results in Figure 4.14 at the bottom, show that the behavior of all the structures becomes the same at frequencies higher than around 1MHz. Taking into account that  $Z_{th\_norm}$  corresponds to the thermal impedance determined for a constant power density, this behavior can be justified by the fact that, at low frequencies, the  $Z_{th\_norm}$  follows the trend imposed by the  $R_{th\_norm}$  (see Figure 4.11 and the relative assumptions made), with VM3 showing a higher  $Z_{th\_norm}$  than HL2 and HL3, since the ratio between the DTI enclosed area and the  $A_E$  tends to favor the devices with reduced  $A_E$ . But if the frequency increases, it is just the volume in close proximity of the heat sources that determines the  $Z_{th\_norm}$ , and it can be supposed that the volume affected by dynamic thermal variations is no more restricted by the DTI, so the condition that favors the devices with reduced  $A_E$  does not hold any more, and all the structures tend to behave the same way for frequencies higher than around 1MHz.

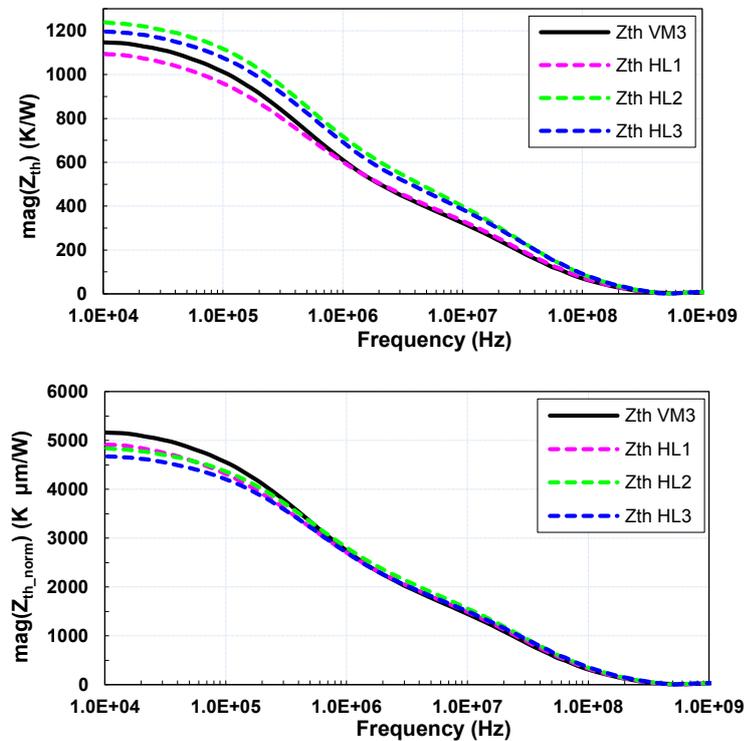


Figure 4.14: (top) Extracted  $Z_{th}$  from low frequency S-parameters measurements for the HL test structures; (bottom) normalized  $Z_{th}$ , obtained multiplying  $Z_{th}$  by the emitter area

## 4.6 Small signal AC characterization

### 4.6.1 $C_{BE}$ and $C_{BC}$ capacitances

In order to characterize the impact at small signal of the addition of metal in the BEOL and of the emitter layout modifications, first of all the  $C_{BE}$  and  $C_{BC}$  capacitances are measured. All the transistors are de-embedded using the same open and short structures, which are designed in such a way to remove the parasitic till the metal-1 level for the base and collector contacts and till the metal-3 level for the emitter contacts.

Figure 4.15 shows the measured  $C_{BE}$  capacitances extracted from cold S-parameter measurements at 10GHz for different  $V_{BE}$  values. As it is obvious, the structures with reduced area have the lowest  $C_{BE}$  value, whereas adding metal stacks on top of the emitter (starting from metal-1 up to metal-8) makes the overall  $C_{BE}$  increase (an increase of around 3fF over all the  $V_{BE}$  sweep is denoted when passing from VM1 to VM8).

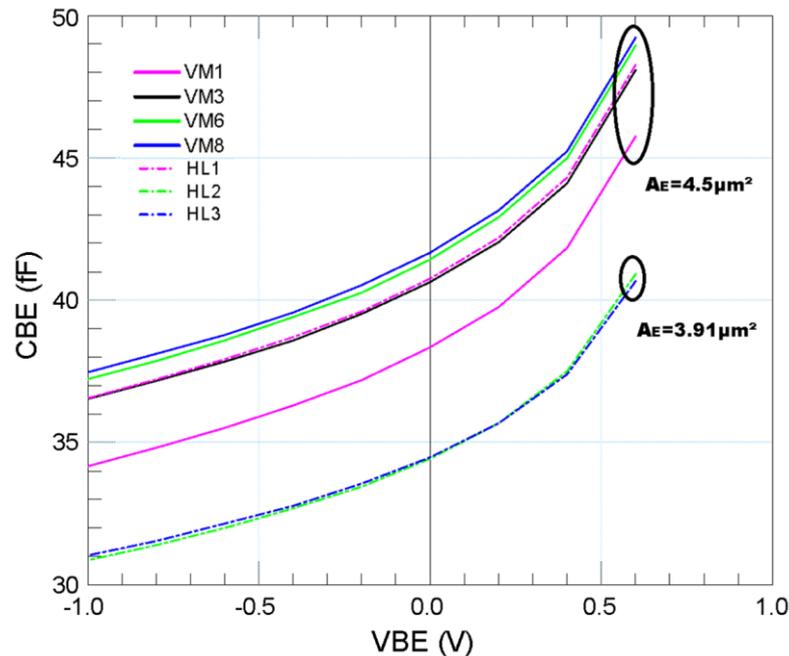


Figure 4.15: measured  $C_{BE}$  capacitance as a function of  $V_{BE}$

In Figure 4.16 is reported the  $C_{BC}$  capacitances extracted from cold S-parameter measurements at different  $V_{CE}$  values. Again the 2 structures with reduced emitter area present a lower capacitance, whereas this time we notice that adding metal stacks above the emitter has a positive effect on the  $C_{BC}$  capacitance, which drops of around 1fF over all the swept values of  $V_{CE}$  passing from test structure VM1 to VM8. This can be explained by the fact that the metal dummies present above the emitter in the VM structures are electrically connected to ground and they can provide a shielding effect that lowers the parasitic capacitance that is present between the base and collector contacts.

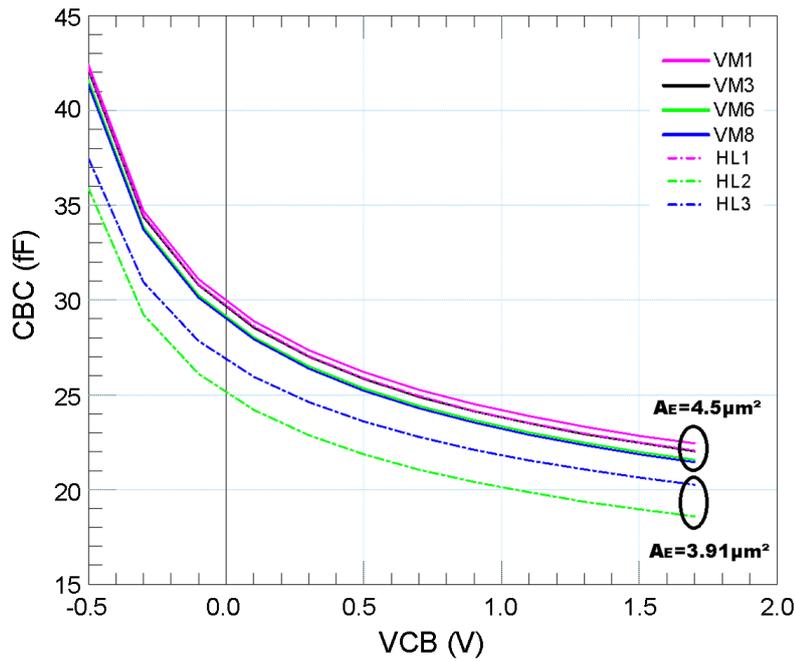


Figure 4.16: measured  $C_{BC}$  capacitance as a function of  $V_{CB}$

#### 4.6.2 Transit frequency

In the case of the test structures VM, it is easy to notice from Figure 4.9 that an electrical connection is implicitly realized between the emitter contact and the metal dummies, thus adding potential parasitic elements. To evaluate the impact of these parasitic elements on the dynamic performances, the proposed transistor topologies are measured in the frequency range from 1GHz to 110GHz in order to determine their transit frequency  $f_T$ . For the de-embedding the same approach described above for the determination of the  $C_{BE}$  and  $C_{BC}$  is used. Figure 4.17 reports the  $f_T$  versus the measured  $I_C$  for the test structures VM, evaluated at an applied  $V_{CE}$  of 1.5V: in contrast to what one could imagine, we notice that stacking more metal dummies above the emitters does not lead to a degradation in the RF performances. For values of  $I_C$  lower than 10mA, no significant difference is noticed among the 4 transistors. On the contrary, passing from structure VM1 to VM8 an improvement is found for  $I_C$  values in correspondence of the peak  $f_T$ , where the difference is around 5GHz; this difference increases till around 10GHz after peak  $f_T$ . This behavior is similar to what has been demonstrated in [77]; the VM structures presented in our work, though, differ from those analyzed in [77]: the latter consist of transistors having a high density of metal dummies above them, but the metal stacks are not electrically connected to any of the transistor contacts.

In Figure 4.18 is reported the  $f_T$  extracted on the test structures HL, plotted as a function of the current density  $J_C$ : they all exhibit a peak of  $f_T$  for the same value of  $J_C$  and the measured performances are almost unaltered. Transistor HL1 performs slightly better than the reference structure VM3, giving performances similar to VM8.

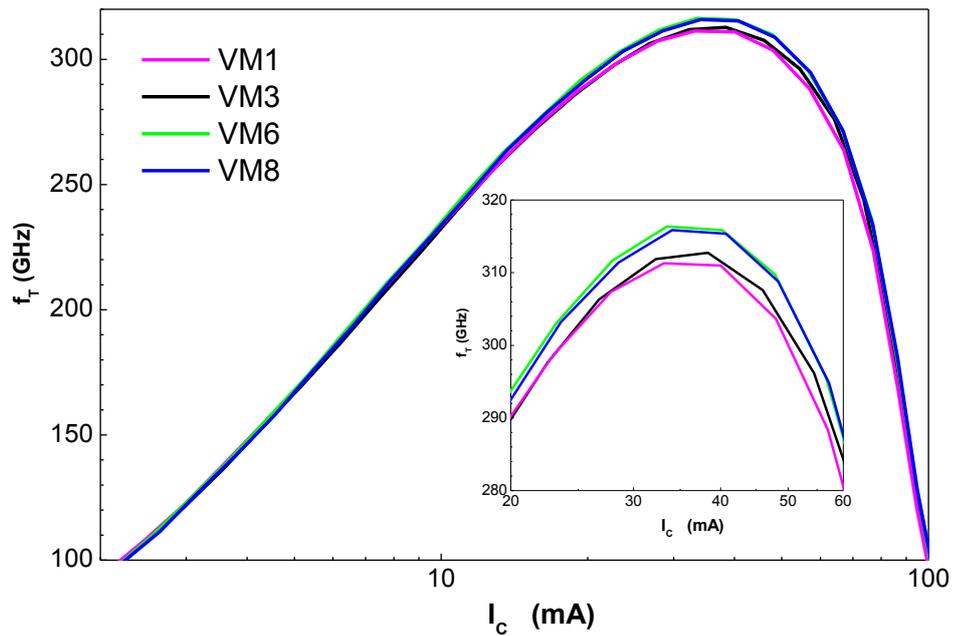


Figure 4.17: Extracted  $f_T$  versus  $I_C$  at 10GHz for test structures VM1 VM3 VM6 and VM8;  $I_C$  is plotted in linear scale to better evidence the different behavior of the test structures.

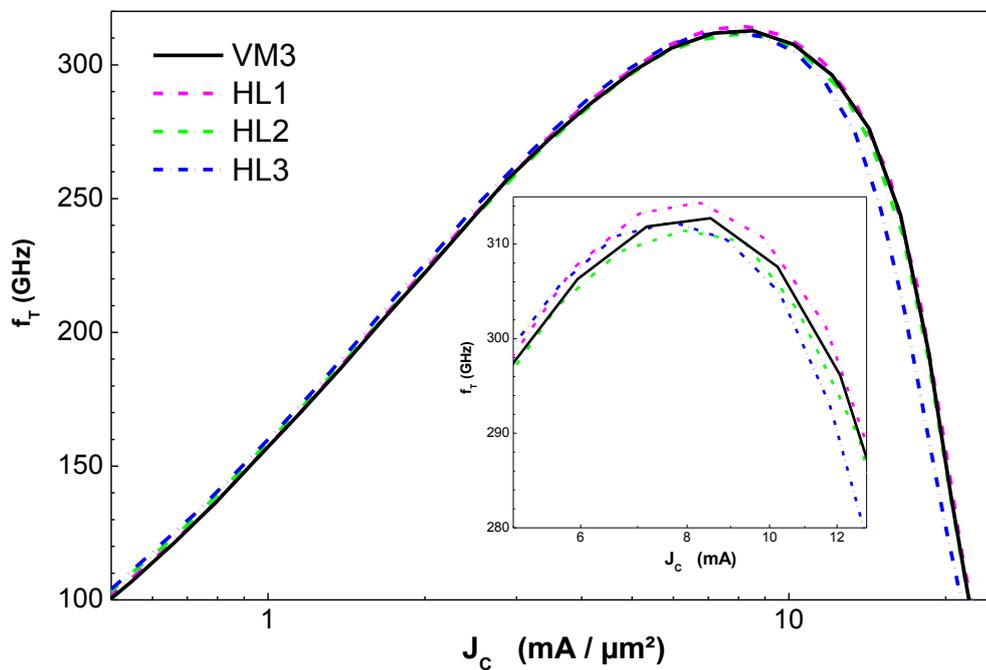


Figure 4.18: Extracted  $f_T$  versus  $J_C$  for test structures HL; the results of test structure VM3 are used as a reference.

The results obtained for the  $f_T$  in Figure 4.17 and Figure 4.18 show that the different HBT topologies with improved thermal behavior that have been proposed do not lead to a degradation of the RF characteristics, but rather can yield, for some structures, a slight performances improvement around peak  $f_T$ .

## 4.7 Conclusion

In this chapter we have proposed some alternative transistor topologies for high power applications with an improved thermal behavior; their electrical and thermal characteristics have been measured and reported.

Among all the proposed methodologies for improving the thermal behavior, the most efficient and interesting seems to be that of adding metal stacks above the active component, as well as increasing the DTI enclosed area (case of HL3 structure). If this approach is chosen, adding 8 levels of metal upon the emitter fingers leads to a diminution in the  $R_{th}$  of around 10% for the SiGe HBTs under study. These better thermal properties allow a sensible decrease of the  $g_{out}$ , thus ensuring an improvement of the SOA specifications and at the same time an increase of the DC current gain till around 34%. Regarding the RF performances, the  $f_T$  curve is observed to slightly shift up and the peak  $f_T$  increases up to 5GHz. The better performances achievable using this architecture, together with the ease of implementation in all the technologies make it the most suitable approach for circuit applications where high power handling is needed.

Among the HL test structures instead, HL1 allows a further extension of the SOA limits, mainly due to an enlargement of the DTI enclosed area. The two test structures with reduced  $A_E$  have been shown to ensure an even enhanced electro-thermal behavior for a given current density compared to the other structures. The approach used for the HL test structures does not lead to any degradation of the  $f_T$  figure of merit, though it requires a change in the layout of the active part of the transistor, which cannot be allowed for some technologies.

It can be also concluded, comparing the different VM test structures in Figure 4.1 and referring to the results obtained in Figure 4.3, that once a certain level of  $P_{diss}$  is attained, the metallization is not only a bare electrical connection, but also participates in a positive way in the heat dissipation, helping to evacuate the heat generated in the active part of the transistor. Its presence impacts in a sensible and positive way both the DC and AC performances of the transistor, and should therefore be modeled and considered into the circuit simulators to provide an improved accuracy in the circuit design phase.

# Chapter 5

## Thermal modeling of state of the art multi-finger SiGe HBTs

### 5.1 Introduction

In Chapter 2 some conventional measurement and modeling techniques were presented in order to verify a transistor compact model. However, these modeling approaches can present some limitations when applied to advanced state of the art technologies. The current trend in nanoelectronics to shrink device dimensions and increase the integration levels yields very high power densities and thus serious thermal issues; this aspect is of particular importance in multi-finger transistors (MFT), where the individual emitter fingers are put in close proximity and each one represents a source of power dissipation. The distributed nature of such components imposes an alternative physics-based modeling approach in order to have a more accurate reproduction of the different phenomena arising within these devices.

This chapter will focus on the mutual thermal coupling in multi-finger transistors in dynamic operation, proposing a distributed approach, which is physics based, in order to study and model the thermal interactions in these components. Firstly, a distributed thermal network is proposed to take into account for the thermal coupling effect between the different emitter fingers. Secondly, the model is validated upon TCAD simulations and dedicated on-wafer pulsed measurements. Finally, with the help of TCAD simulations, the impact of the BEOL on the thermal dynamics has been analyzed, and a new method to evaluate the thermal coupling coefficients under the real operating conditions of the transistor is proposed.

### 5.2 Intra-device thermal interactions in multi-finger HBTs

Multi-finger transistors are often used in PA cells since they are more suitable for high frequency combined with high power operation due to the small base access resistance and since they allow a better current handling capability and an improved thermal dissipation. In these devices, the center fingers are considered to be the most critical ones from an electro-thermal point of view, since, due to the thermal coupling with the neighboring fingers, they reach the highest temperature; this effect is made stronger by the presence of the DTI, which prevents the heat to flow laterally; an example of temperature distribution in a multifinger HBT can be found in Figure 5.1. These thermal inhomogeneities can be quite significant: as it has been previously shown by means of TCAD simulations in [87], a temperature difference of even 15K can be observed

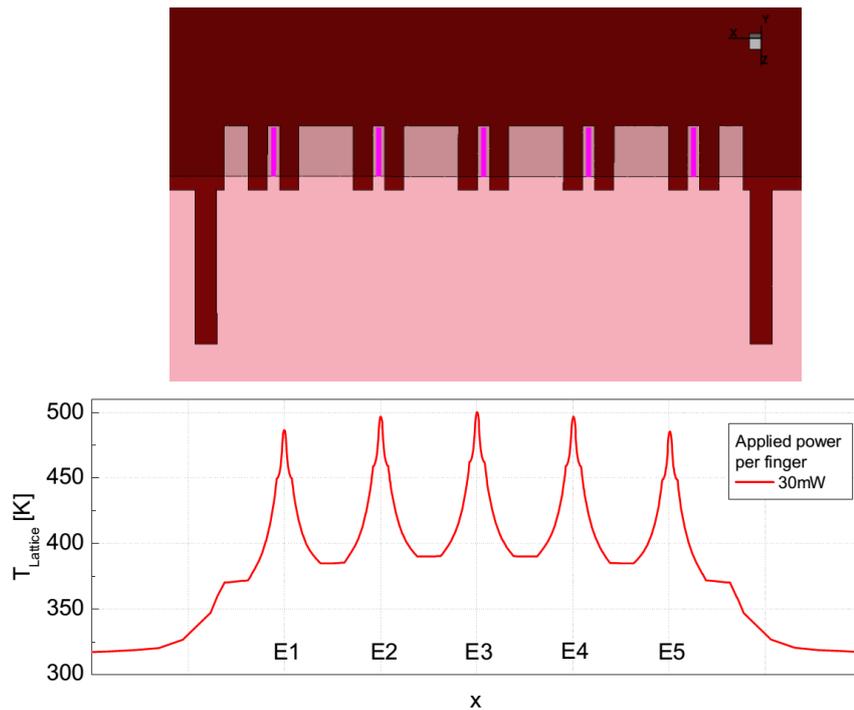


Figure 5.1: (top) 3D representation of a 5 fingers HBT (up to the BC junction), with geometry corresponding to the STMicroelectronics B55 process; silicon is colored in pink, SiO<sub>2</sub> in brown and the heat sources in violet. (bottom) cross section of the temperature along the heat source in the x direction, when a power of 30mW is applied to the five heat sources [1]. The structure is simulated in Sentaurus TCAD.

between center and side fingers when there is a power dissipation of 30mW (Figure 5.1). For these reasons, to avoid thermal runaway and subsequent destruction of the MFT component, it is necessary to simulate the right temperature distribution in the structure during the design process; to accomplish that, a distributed approach can be used, in which one transistor model per finger is considered and the thermal node is connected to a network that is able to predict the self and mutual heating effects arising in the device. Concerning a single finger transistor, several research studies were performed to study self-heating effects in steady-state, like [97] and [98] and in transient conditions [99], [100] to obtain thermal resistance  $R_{\text{th}}$  and thermal capacitance  $C_{\text{th}}$ . In [101] the mutual thermal coupling in multifinger SiGe:C HBTs is modeled under DC operation, using a distributed transistor model that considers self-heating as well as thermal coupling between the different fingers; the characterization of this intra-device thermal interactions can be extended to the dynamic case, studying the mutual thermal coupling taking place between the different emitter fingers during thermal transients. This can be of critical importance in cases of pulsed power dissipations (like in switching applications), where the transient temperature of the component doesn't reach the steady state value. In the following section a thermal model is proposed, in order to simulate these transient thermal interactions and can be applied to the case of multifinger transistors.

### 5.3 The model proposed for transient intra-device thermal coupling

In compact models a common way to take into account electro-thermal effects is to provide a representation of the device electrical characteristics as function of its operating temperature, while providing a prediction of its temperature according to the power dissipated in the device itself. To calculate the temperature of a single device due to self-heating, a simple parallel RC network is typically used, but when two devices are operating at the same time in close proximity, an additional temperature increase must be considered, due to thermal coupling. In fact the spread of the heat flux through the substrate causes device 1 to contribute in the increase of the temperature of device 2; an efficient way to take into account this thermal coupling effect can be found in [88]. If we consider self-heating and mutual thermal coupling, we can express the temperature rise above the ambient temperature for two active devices as shown in Eq. 5.1:

$$\begin{aligned} T_1 &= R_{th,1} P_{d,1} + R_{th,12} P_{d,2} = R_{th,1} P_{d,1} + c_{12} R_{th,2} P_{d,2} = R_{th,1} P_{d,1} + c_{12} \Delta T_2 \\ T_2 &= R_{th,2} P_{d,2} + R_{th,21} P_{d,1} = c_{21} R_{th,1} P_{d,1} + R_{th,2} P_{d,2} = c_{21} \Delta T_1 + R_{th,2} P_{d,2} \end{aligned} \quad \text{Eq. 5.1}$$

where  $R_{th,i}$  and  $P_{d,i}$  are respectively the thermal resistance and the power dissipated of each component; the terms  $c_{xy}$  instead are the thermal coupling coefficients between device  $x$  and device  $y$  and take into account how much of the temperature of device  $y$  is coupled to that of device  $x$  (see Figure 5.2). This coupled temperature can thus be simulated by the introduction of a voltage-controlled-voltage-source (VCVS) in series with the thermal resistance.

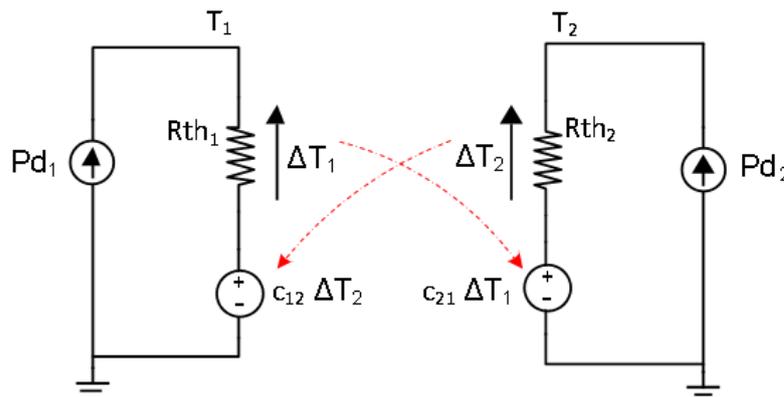


Figure 5.2: Extended thermal network for self-heating and DC thermal coupling for two heat sources [10].

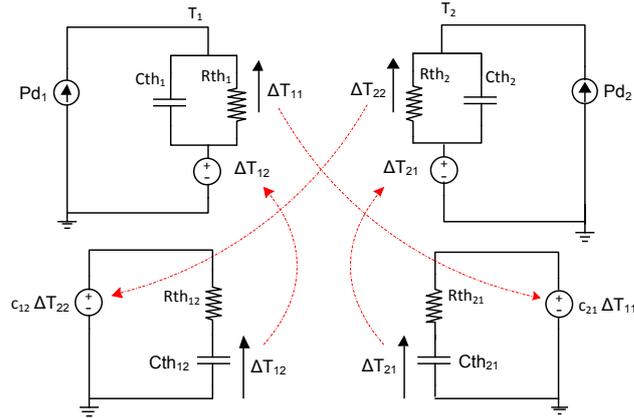


Figure 5.3: Extended thermal network for self-heating and transient thermal coupling for two heat sources [11].

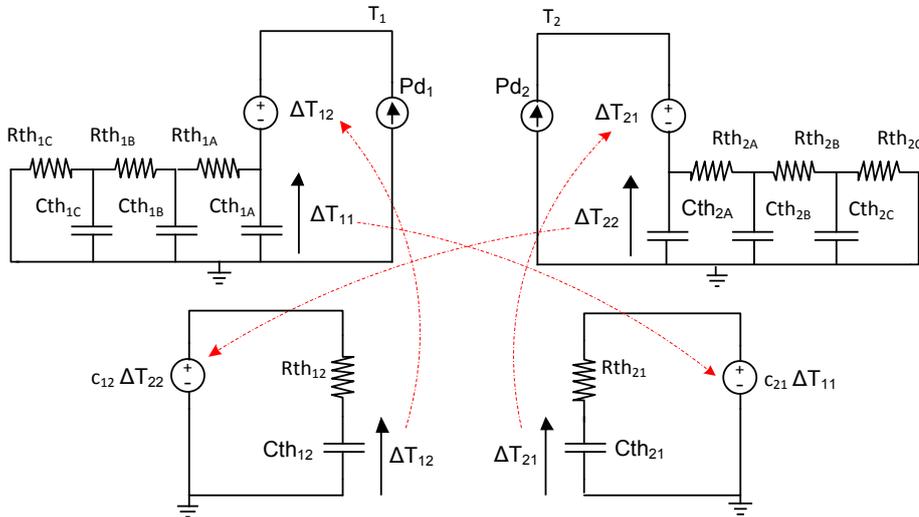


Figure 5.4: The proposed 3 poles thermal network for self-heating and transient thermal coupling considering two sources; the two networks at the bottom simulate the delay for the heat to spread from a given finger to a neighboring one.

In [102], this approach has been further extended to model the thermal coupling between two heat sources in case of transient operation. As it is possible to see in Figure 5.3, an additional separate RC network has been introduced, in order to take into account the delay in the time response. This concept can be easily extended to multiple devices and heat sources, in our case the fingers of a MFT. As already shown in [100] and [103] a single pole network is not able to approximate the actual thermal response to a step in power, however for compact modeling it is suggested to limit the number of RC subcircuit nodes for computational reasons. Hence a three time constants RC circuit has been chosen as a good compromise between accuracy to reproduce the transient thermal response and computational effort; besides it is usually possible to observe three main slopes in the measured  $Z_{th}$  of a state of the art SiGe HBT (refer to Figure 5.15). The  $R_{th}$  and  $C_{th}$  of each finger in Figure 5.3 have been replaced by a recursive Cauer type network (which has

already been demonstrated to give good accuracy in [86]); in this kind of network the different self-heating related  $R_{th}$  and  $C_{th}$  are scaled as follows:

$$\begin{aligned} Rth_{i,n} &= Rth_{i,A} K_R^n \\ Cth_{i,n} &= Cth_{i,A} K_C^n \end{aligned} \quad \text{Eq. 5.2}$$

Where  $i$  indicates the finger number, while  $n$  is an incremental number going from 0 to the order of the recursive network, as the distance from the power source increases (for example passing from  $Rth_{1,A}$  to  $Rth_{1,C}$   $n$  goes from 0 to 2);  $Rth_{i,A}$  and  $Cth_{i,A}$  represent the first elements of the recursive network, whereas  $K_R$  and  $K_C$  are fitting parameters. It is required that  $K_R < 1$  and  $K_C > 1$ , in order to ensure that the values of the thermal resistances in the thermal model will decrease as the distance from the heat source increases, while the opposite happens for the thermal capacitances, thus respecting the physical thermal behavior within the transistor.

Figure 5.4 presents the network that we propose to model the intra-device mutual thermal coupling inside multifinger SiGe HBTs in pulsed operation conditions (to simplify the image, just 2 heat sources are shown); in our case we will consider a five emitters component. The model takes into account the temperature dependence of the  $R_{th}$  as:

$$Rth(T) = Rth(T_0) \left( \frac{T}{T_0} \right)^\alpha \quad \text{Eq. 5.3}$$

where  $R_{th}(T)$  and  $R_{th}(T_0)$  are the thermal resistance at temperature  $T$  and at the reference temperature  $T_0$  respectively and  $\alpha$  is a model parameter.

## 5.4 The thermal coupling coefficients

As described in section 5.3, when two or more devices are operating in close proximity, an additional temperature increase needs to be considered due to thermal coupling. An efficient way to take into account this coupling effect into circuit simulators is given in Eq. 5.1. The thermal coupling factors  $c_{xy}$  estimate the amount of rise in temperature at finger- $x$  due to heating at finger- $y$ . A closed form empirical relation for  $c_{xy}$  has been proposed in [72] and is given by the expression:

$$c_{xy} = \frac{\Delta T_{xy}}{\Delta T_{yy}} = \frac{\Delta T_{xy}/P_{d,y}}{\Delta T_{yy}/P_{d,y}} = \frac{Rth_{xy}}{Rth_{yy}} = \frac{1}{\sqrt{\left(\frac{d_{xy}}{a}\right)^b + 1}} \quad \text{Eq. 5.4}$$

where  $P_{d,x}$ ,  $R_{th,xx}$  and  $\Delta T_{xx}$  represent the dissipated power, thermal resistance and rise in temperature due to self-heating at finger  $x$ , respectively, whereas  $R_{th,xy}$  and  $\Delta T_{xy}$  represent the mutual thermal resistance and the rise in temperature at finger  $x$  due to heating at finger  $y$ ; for what concerns the empirical relation proposed instead,  $d_{xy}$  is the distance of

the sensing finger  $x$  from the heating finger  $y$ , whereas  $a$  and  $b$  are fitting parameters. To test the validity of this formulation, the coupling coefficients have been measured on two different test structures consisting of a 5 fingers transistor realized in a STMicroelectronics BiCMOS 55nm process, where 2 different distances have been considered for the emitter spacing:  $2.49\mu\text{m}$  (the distance in the standard multifinger transistor, which is under study in this chapter and that will be referred to as HBT1) and  $1.79\mu\text{m}$ , which represent a laterally shrunk version (28%) of the standard transistor, and will be named HBT2.

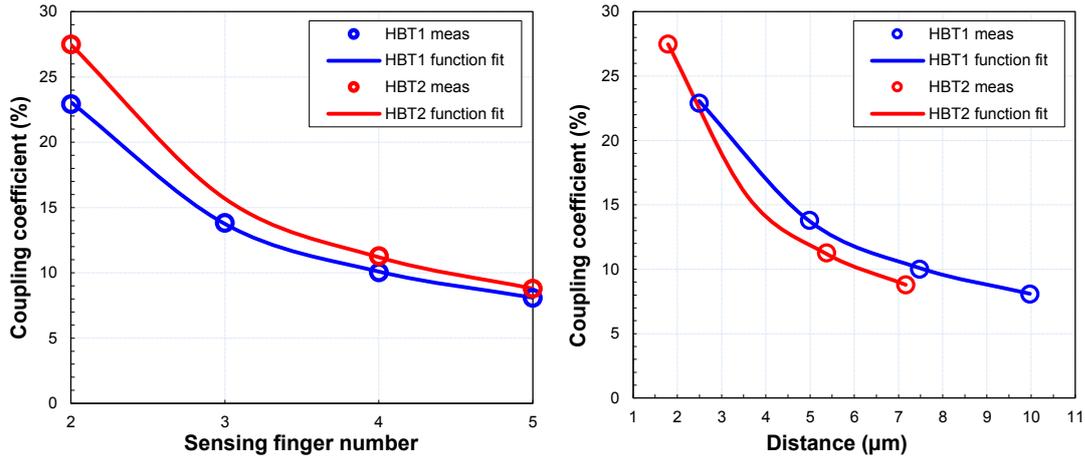


Figure 5.5: Coupling coefficients measured when finger 1 is heating ( $C_{i1}$ ); on the x axis it is reported the finger number (left) or the distance from the heating finger (right).

	Emitter to emitter spacing	$a$	$b$
<b>HBT1</b>	$2.49\ \mu\text{m}$	$124.40\ \text{E-12}$	1.545
<b>HBT2</b>	$1.79\ \mu\text{m}$	$14.95\ \text{E-12}$	1.694

Table 5.1: parameters used to fit the thermal coupling coefficients versus distance for two multifinger HBTs from the ST B55 technology having different spacing between the drawn emitter fingers. The empirical relation presented in Eq. 5.4 is used.

In Figure 5.5 it is reported the measured and simulated thermal coupling coefficients in HBT1 and HBT2 when just finger 1 is heating: of course the thermal coupling is higher for HBT2, in which the emitters are placed at a smaller distance. Using the formulation presented in Eq. 5.1 yields a good reproduction of the coupling coefficients in the two different test structures analyzed. It can be noticed that, when plotted as function of the distance, the coupling coefficients almost lay on the same curve. The values for  $a$  and  $b$  used to obtain the fit in Figure 5.5 from Eq. 5.4 are reported in Table 5.1.

## 5.5 Validation of the model with TCAD simulations

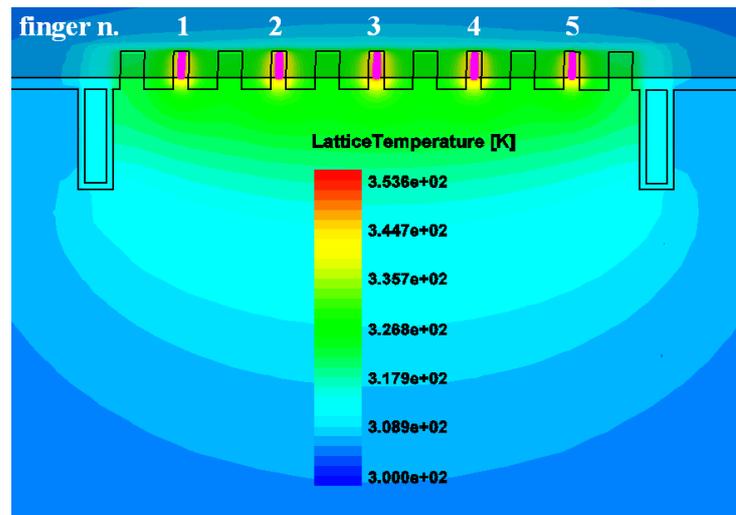


Figure 5.6: Thermal distribution in the five emitters HBT structure considered for a power dissipation of 10mW for each finger.

In order to test the validity of this substrate representation, a 3D TCAD electro-thermal simulation is realized on the structure in Figure 5.6, which reproduces a five-emitter SiGe HBT component. The 5 emitters are assumed to be the heat sources and each one has a drawn emitter area  $A_E = 5 \times 0.18 \mu\text{m}^2$ . The device was embedded on the top of a silicon substrate block  $300 \mu\text{m}$  thick, having lateral dimensions of  $500 \mu\text{m}$ , thus much higher than the transistor dimensions. This simplified structure only takes into account the region below the BC junction, neglecting the presence of the BEOL.

The thermal behavior of the component is first analyzed under DC conditions: a constant power is applied to the emitter stripes one at a time, to obtain the  $R_{th}$  of each finger and evaluate the coupling with the other fingers; besides it is also possible to evaluate the impact of the temperature dependent thermal conductivity. The results for different levels of power dissipation in the case where just finger 1 is heating are reported in Figure 5.7 (left); as expected a non-negligible temperature increase can be sensed on the neighboring fingers due to the thermal coupling phenomenon. The case where all the fingers are excited with the same level of power dissipation is also shown in Figure 5.7 (right); it is possible to notice that the temperature difference among the fingers is always higher as the power increases, since the effect of thermal coupling becomes always more pronounced. In both situations shown in Figure 5.7 the model is able to predict with a good accuracy the thermal distribution within the transistor structure.

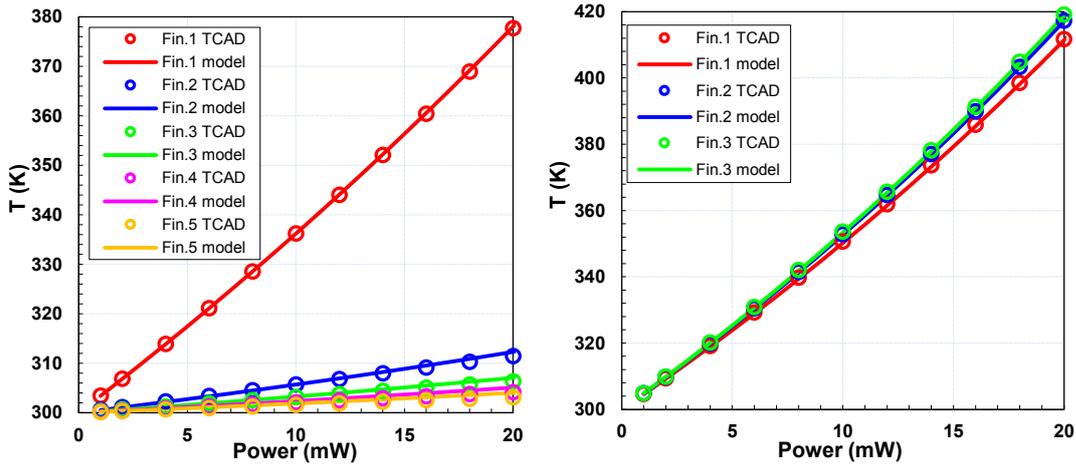


Figure 5.7: Temperature results from the TCAD simulation and the compact model for different values of power dissipation applied to finger 1 (left) and to all fingers (right).

Next, the transient thermal behavior of the structure is simulated by applying a pulse of 10mW per finger. The results from the proposed model are also presented in Figure 5.8, using a logarithmic scale on the time axis, to show the accuracy achieved during the transient (since the structure is symmetrical the temperature of finger 4 and 5 is the same as finger 1 and 2 respectively). The maximum deviation of the model from the TCAD results is around 1K. From the results of Figure 5.8 it is possible to notice that the thermal evolution of finger 1 and 5 during the transient differs from that of the other fingers due to the proximity of the DTI, acting as a vertical adiabatic surface. In fact, a lower temperature rise is expected because finger 1 and 5 have only one neighboring heat source. To further study the transient behavior of the component, another scenario is presented, where a pulse of 10mW is applied to just one emitter stripe.

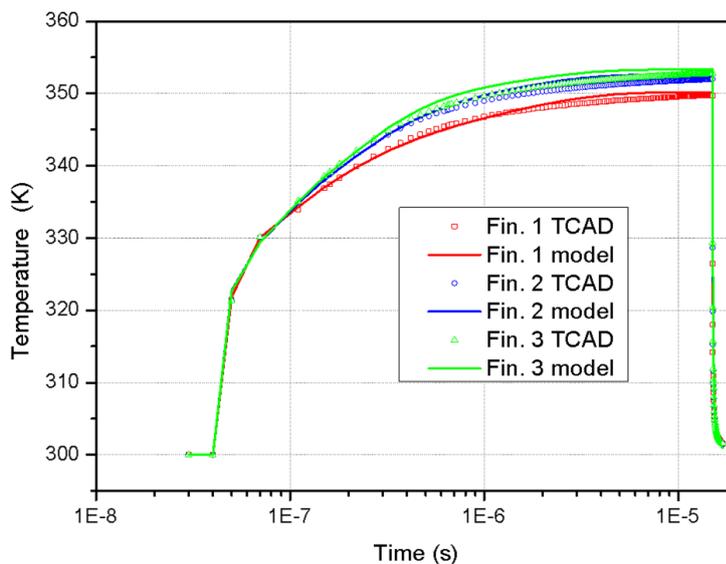


Figure 5.8: Temperature results from the TCAD simulation and the compact model (presented in Figure 5.4) of a 5 finger HBT when a pulse of 10mW power dissipation is applied to all fingers ( $T_{finger1}=T_{finger5}$ ,  $T_{finger2}=T_{finger4}$ ).

As expected, a lower temperature will be sensed on fingers that are placed at a larger distance from the heat source, as can be seen on Figure 5.9; in addition, it is possible to notice a slower time response when the distance between the heat source and the sensing finger increases, this is due to the longer time that the heat needs to propagate in the substrate (this effect is modeled by the delay RC network in Figure 5.4).

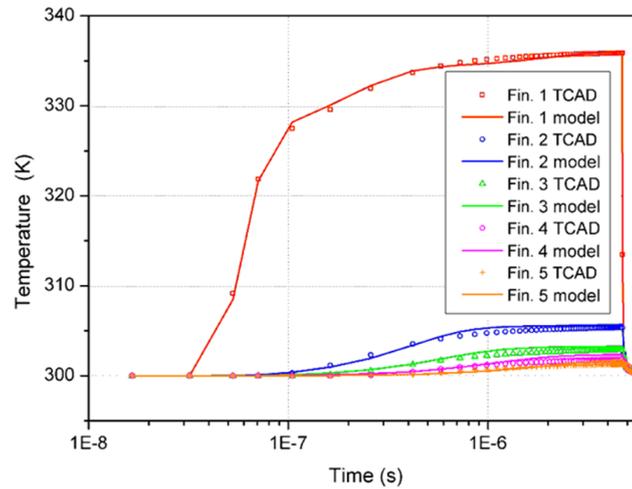


Figure 5.9: Temperature results from the TCAD simulation and the compact model (presented in Figure 5.4) of a 5 finger HBT when a pulse of 10mW power dissipation is applied at finger 1.

In Figure 5.10 we compare the time evolution of the temperature at finger 1 obtained from the TCAD simulator when a pulse of power dissipation of 30mW is applied to all the fingers or to just finger 1, to evaluate the effect of the thermal coupling between all the fingers in transient operation. It is clear how the mutual thermal coupling between the different heat sources in the multifinger transistor slows down the temperature evolution: the time needed to reach the 63% of the total temperature excursion is of  $0.10\mu\text{s}$  in the case where just finger 1 is heating and  $0.27\mu\text{s}$  when all the fingers are heating. Referring to the model considered (Figure 5.4) it can be seen that the thermal coupling phenomenon involves the use of different additional RC networks, thus introducing more thermal constants in the overall system and requiring a longer time to reach a steady temperature.

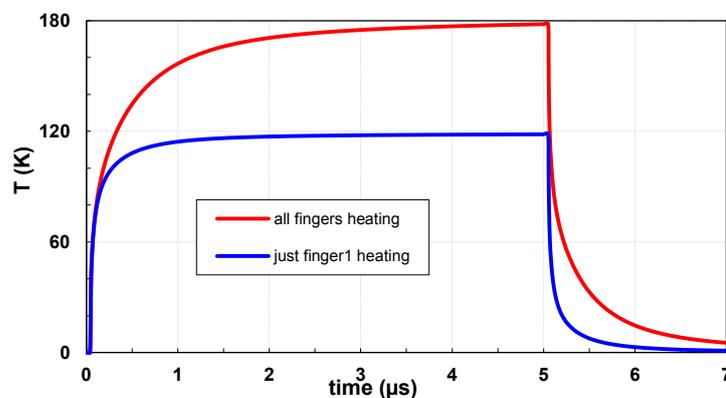


Figure 5.10: TCAD simulation of the temperature evolution on finger 1 when a pulse of 30mW is applied to all the fingers (red) and to just finger 1 (blue).

## 5.6 Model validation with on-wafer measurements

### 5.6.1 Pulsed measurements

To further evaluate the effect of the intra-device transient coupling, an on-wafer test structure (equivalent to the one already presented in [101]) has been measured in pulsed operation conditions. The test structure has been fabricated in STMicroelectronics B55 technology and consists of a 5 fingers SiGe HBT, where each finger is thermally coupled, but electrically separated; the 5 transistors have a common collector contact and each one of the 5 emitters is accessible, while the bases are all grounded (see Figure 5.11 and Figure 5.12).

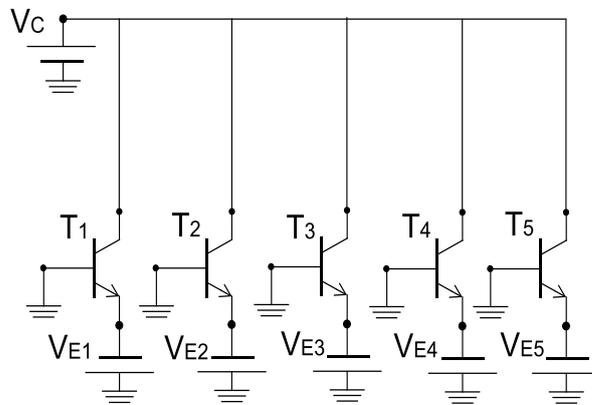


Figure 5.11: The equivalent schematic of the test structure used for the thermal coupling measurements.

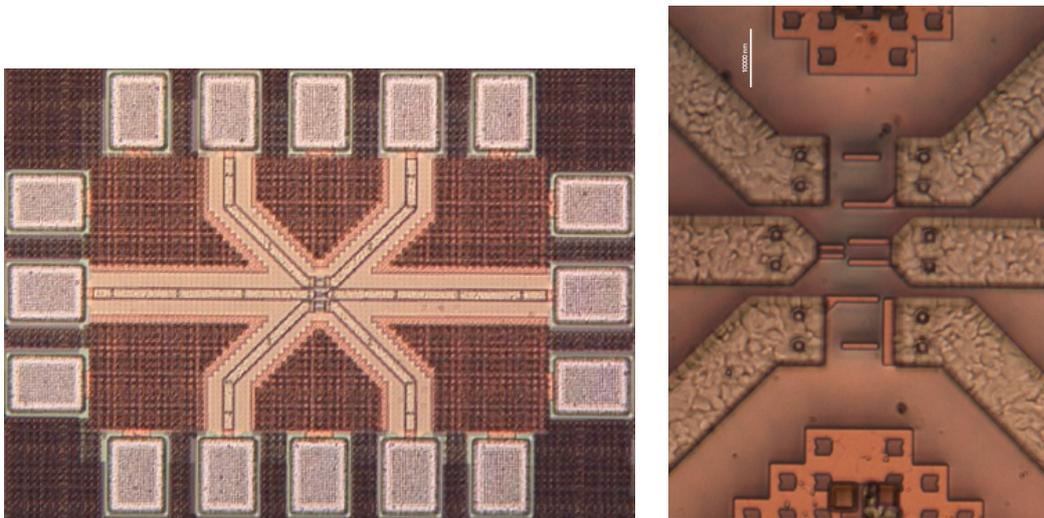


Figure 5.12: (left) micrograph photo of the dedicated test structure used for the pulsed measurements and (right) zoom in the area above the transistor, where the six transmission lines are connected to the emitter and collector stripes.

This configuration allows to use each finger as a heater, by simply turning it on, or as a temperature sensor, by measuring the shift in its  $I_E$  ( $V_{BE}$ ) characteristics. In [104] a measurement system has been presented that uses a low-distortion function generator, a

lock-in amplifier, and a parameter analyzer for the extraction of the thermal resistance and capacitance in bipolar devices. In this work instead, a new setup for the measurement of the thermal response is used, that allows to measure the response of each finger of the multifinger SiGe HBT to a voltage pulse applied to a neighboring finger.

The measurements were carried out on-wafer at 300K using a SUSS MicroTec probing station equipped with a thermal chuck. Probing was done with two differential GSGSG probes (SUSS MicroTec) and two GSG probes (Picoprobe). The DC analyzer Keithley 4200 containing a 4225-SCS module has been used to generate the pulses on the heating finger and measure the response on the sensing finger. While the common collector is constantly biased to 0.5V using the HP4155A DC analyzer, a negative pulse of -0.95V is applied to the emitter finger that acts as a heater, to forward bias its BE junction, while the emitter finger that senses the temperature is biased to a constant negative voltage of -0.85V; in these conditions a current increase can be noticed on the sensing finger, due to the temperature rise of the heater. In Figure 5.13 are shown the currents of the sensing fingers 1, 4 and 5 when finger 2 acts as a heater; the fingers are sensed one by one, while the heater is always finger 2. The compact model simulation results are also added. It can be noticed that, if the distance between heating and sensing finger increases, the variation of current that is measured on the sensing finger is smaller due to its lower temperature increase. This behavior is qualitatively similar to the TCAD results in Figure 5.9, but the simulation shows a faster time constant of a factor 2; the reason for this is that the simulated structure does not consider the back end of line (BEOL), which has an important impact on the thermal capacitance [45], as will be also discussed in section 5.7.

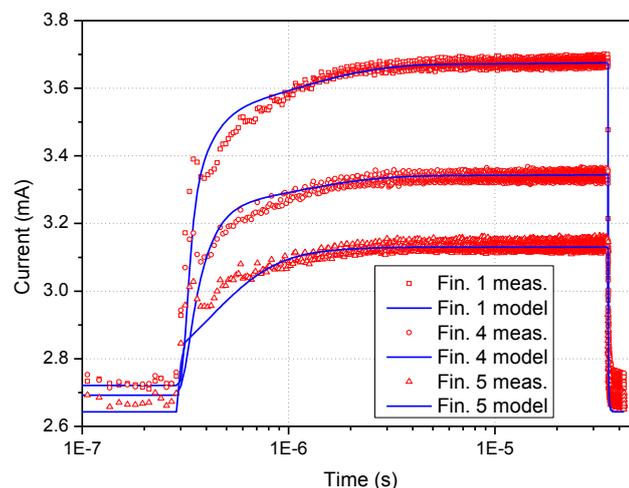


Figure 5.13: Measured current (red) and simulated current (blue) on the sensing fingers; from top: current sensed on finger 1, finger 4 and finger 5.

In Table 5.2 it is proposed a comparison of the main parameters used to fit the temperature evolution simulated in TCAD environment (Figure 5.8 and Figure 5.9) and the measured  $I_C$  in pulsed operation (Figure 5.13 and Figure 5.14) using the proposed three poles recursive network shown in Figure 5.3. It can be noticed that having neglected the region

Test structure	TCAD	measurements
$R_{th1}$ [W/K]	3.37k	2.70k
$R_{th2}$ [W/K]	3.21k	2.62k
$R_{th3}$ [W/K]	3.19k	2.61k
$C_{th1A}$ [J/K]	715f	3.1p
$C_{th2A}$ [J/K]	349f	3.0p
$C_{th3A}$ [J/K]	349f	3.0p
$K_R$	0.31	0.38
$K_C$	127	501

Table 5.2: comparison of the main parameters used in the thermal network in Figure 5.3 to fit the temperature evolution simulated in TCAD environment and the measured  $I_C$  in pulsed operation.

above the BC junction in the simulated TCAD structure results in a higher  $R_{th}$  and a lower  $C_{th}$ , in accordance with [45]. Furthermore, a much higher  $K_C$  coefficient is considered to fit the measured results, as a sign that the three self-heating related  $C_{th}$  in the thermal model increase rapidly as the distance from the heat source increases (as also discussed in section 3.4) and this effect is particularly evident in the BEOL metallization (as also shown in the thermal model for the BEOL in Figure 3.18), which is instead completely absent in the TCAD simulated structure.

It is also interesting to show the current measured on the heater, since it will have a small increase due to the power dissipation on the sensing finger (in our case no more negligible), which is constantly biased (see Figure 5.14). To simulate the electro-thermal behavior of the measured multifinger HBT, the thermal nodes of five lumped calibrated HiCuM transistor models are connected to the distributed thermal network proposed in section 5.3; the results of the simulation of the distributed model are compared to the measurements, showing a good agreement (Figure 5.13 and Figure 5.14).

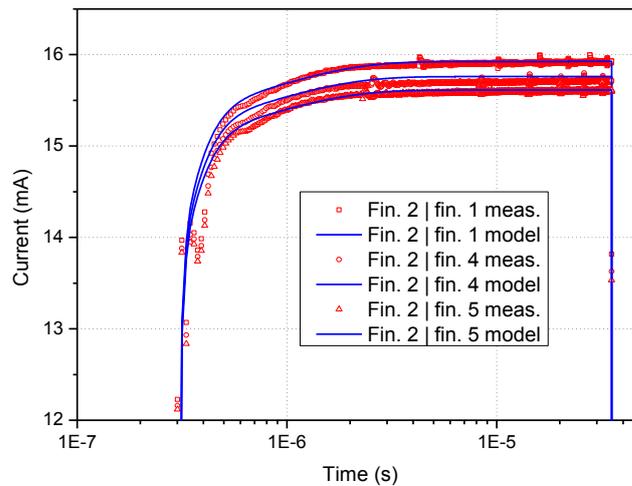


Figure 5.14: Measured current (red) and simulated current (blue) on the heating finger 2 in the case when (from the top): finger 1, finger 4 and finger 5 are sensing.

### 5.6.2 Low frequency measurements

To study the impact of the mutual thermal coupling between the emitter fingers on the thermal impedance, the behavior of the  $Y_{22}$  parameter versus frequency is analyzed; in fact, as discussed in Chapter 2, at low frequency this parameter is directly proportional to the  $Z_{th}$  of the component. In Figure 5.15 it is reported the amplitude of  $Y_{22}$  measured on the 5 fingers transistor in the range from 10kHz to 1GHz (these measurements have not been conducted on the dedicated test structure shown in Figure 5.11, but on a conventional test structure, where the transistor is connected in common emitter configuration). The  $Y_{22}$  obtained from simulation using the network of Figure 5.4 is also shown. To evaluate the impact of the thermal coupling on the overall  $Z_{th}$  of the transistor under study, different cases are shown: in red the case where only static and dynamic self-heating are considered, neglecting the effect of the mutual thermal coupling; in green just the static thermal coupling is added; in violet both static and dynamic thermal coupling are taken into account. In addition also the results for a single pole network are reported, considering static and dynamic coupling (blue line).

It is possible to notice, comparing the single pole network to the three poles network (blue and violet lines) that for the first just a single slope is observed (rolling off at -18dB/dec), whereas the latter shows three different decays in the frequency range between 100Hz and 20MHz (-1.8dB/dec, -4.6dB/dec and finally -18dB/dec where the first decay is not visible since the plot starts at 10kHz)

It is also evident how the dynamic thermal coupling provides an additional capacitive effect, decreasing the  $Z_{th}$  at high frequency (compare the green and violet curves in Figure 5.15), and this results in a globally slower thermal dynamics (as shown in Figure 5.10).

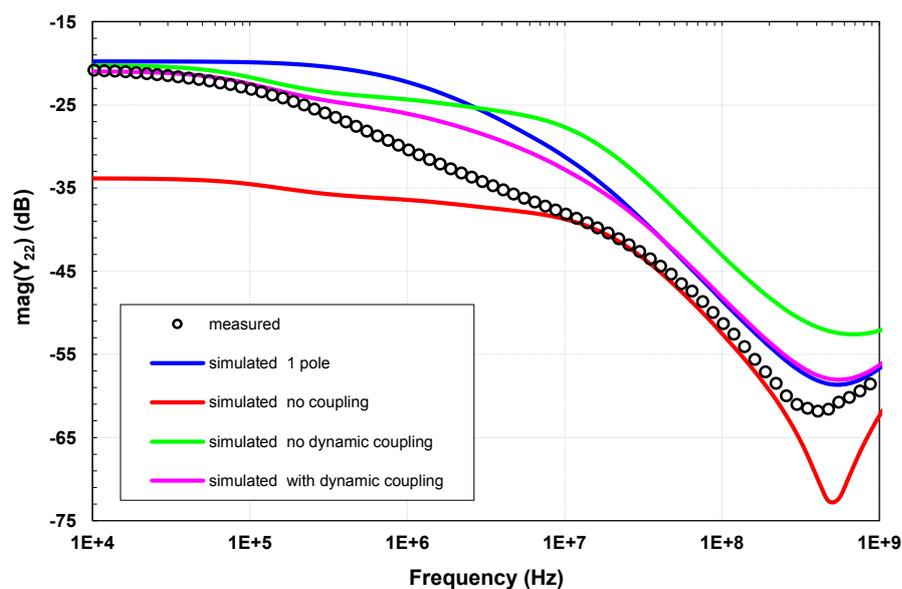


Figure 5.15: Measured and simulated  $Y_{22}$  on the 5 fingers transistor under study; different cases are proposed for what concerns the simulation results.

## 5.7 Thermal impact of the BEOL

With the help of the thermal TCAD simulations it is possible to evaluate the impact of the BEOL on the thermal coupling coefficients. Two different methods are used to extract the coefficients: (case A) a DC power dissipation of 20mW is applied on each finger one by one, so only one finger is heating at a time; this methodology is normally applied to obtain the coupling coefficients from measurements (like in Figure 5.5 and in [101]). In case-B instead, all the fingers are heated simultaneously with  $P_{\text{diss}}=20\text{mW}$  to emulate a real operating condition, while an additional perturbation of 1mW is applied to the individual fingers one at a time, to extract the coupling factors. For both the described approaches the TCAD simulations are performed with and without considering the BEOL layers from the BC junction up to metal-1.

Table 5.3 shows the thermal coupling factors between the five fingers at  $T_{\text{amb}}=300\text{K}$  for all the four cases and the results are restricted to the case when finger-1 is heating and all others are sensing. It is evident from the results that extracting the coupling coefficients under real operating condition (case B) gives higher coupling coefficients than in the case where only one finger is heating. This behavior can be justified by the fact that the lateral temperature gradient is less when all fingers are heating at the same time and the resulting overall temperature involved in the coupled thermal resistance is higher compared to that in case A. We can also deduce that the coupling factors are higher when the BEOL is taken into account: the  $c_{xy}$  are increased by around 15% if the BEOL region is included; in fact, when the BEOL is taken into account in the TCAD simulation, a wider lateral surface is considered, thus yielding a higher thermal coupling among the different heat sources.

	<b>c<sub>21</sub></b>	<b>c<sub>31</sub></b>	<b>c<sub>41</sub></b>	<b>c<sub>51</sub></b>
<b>Case A no BEOL</b>	14.7%	8.4%	5.6%	4.3%
<b>Case B no BEOL</b>	16.9%	9.7%	6.4%	4.9%
<b>Case A with BEOL</b>	17.7%	10.0%	6.7%	5.2%
<b>Case B with BEOL</b>	19.6%	11.2%	6.4%	4.9%

Table 5.3: Thermal coupling factors extracted from TCAD at  $P_{\text{diss}}=20\text{mW}$  and  $T_{\text{amb}}=300\text{K}$ .

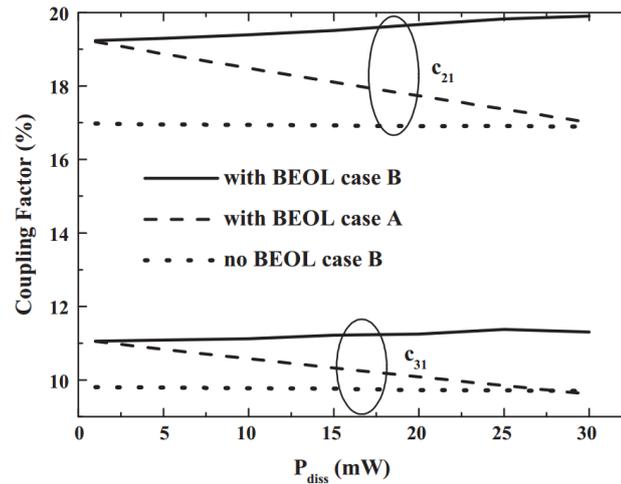


Figure 5.16: Dissipated power dependent thermal coupling factors,  $c_{21}$  and  $c_{31}$  under different conditions at  $T_{amb}=300K$ . The parameters are extracted from TCAD simulator.

Figure 5.16 shows the dissipated power dependence of the thermal coupling factors  $c_{21}$  and  $c_{31}$  at  $T_{amb}=300K$ . It is observed that the thermal coupling coefficients slightly decrease with increasing power in case A. Observing this decrease and Eq. 5.4, one may be tempted to conclude that the temperature dependent increase in the self-thermal resistance  $R_{th,yy}$  slightly dominates over the increase in the coupled-thermal resistance  $R_{th,xy}$ . However with case B (real operating condition), the coupling factors are independent of the dissipated power if the effects of BEOL are not considered as shown in Figure 5.16. In this case, the change in temperature of the silicon near to all the fingers are comparable; hence, the temperature-dependent thermal conductivity and the resulting self-heating and coupling thermal resistances vary in a similar way yielding almost power-independent coupling factors. Additional effects of BEOL are two-fold; it reduces the self-heating and increases the thermal coupling. Such effects are expected to be more pronounced with increased power dissipation resulting into slightly increasing coupling factors with dissipated power as shown in Figure 5.16 for case B with BEOL effects. This unique observation is in contrast with the ones reported in [89], [101]. Similar characteristics are also obtained for the other coupling coefficients.

The evolution of the junction temperature under pulsed operation is reported in Figure 5.17; a power pulse of 30mW with pulse width of  $5\mu s$  is applied at finger 1, with and without considering the BEOL (for clarity, the results are restricted to only finger 1 and 2). It is observed that the temperatures at the different fingers are overestimated if the effects of BEOL layers are not considered; moreover, the BEOL region consists of different materials, and their presence slows down the thermal response of around a factor 2 (this is particularly evident in the initial temperature evolution). The difference due to BEOL layers reduces as the distance of the sensing finger increases from the heating finger.

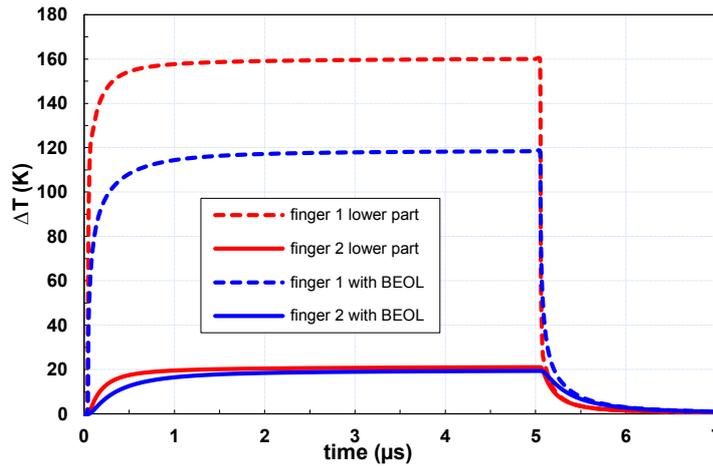


Figure 5.17: evolution of temperature increase from TCAD simulation on the fingers 1 and 2, when a pulsed of dissipation of 30mW is applied at finger 1. Two cases are compared: when just the lower part is simulated and when the BEOL up to metal-1 is considered.

## 5.8 Conclusion

In this chapter, the effects of intra-device transient thermal coupling in trench isolated SiGe HBTs have been characterized with the aid of thermal TCAD simulations and with on-wafer pulsed measurements. The model reported uses a simple netlist-based method, which allows to accurately reproduce the transient thermal effects described, by using an electrical simulator; for these reasons it can be useful to simulate in a more realistic way the behavior of multifinger SiGe HBTs during the design process. In addition, it can be used to choose the ballast resistors in a PA cell for a balanced heat distribution.

The effect of the mutual thermal coupling in dynamic operation has been analyzed in the time and frequency domain; it has been observed that it leads to an overall slowdown of the temperature evolution of the transistor fingers, which is taken into account by the delay networks shown in Figure 5.4.

The impact of the BEOL on the temperature evolution could be determined by means of TCAD simulations and it is found that the presence of the layers from the BC junction up to the first level of metal determine an increase of the  $C_{th}$  (together with a decrease of the  $R_{th}$ ), which leads to an overall slowdown of the temperature evolution of around a factor 2, for the technology under study. Moreover a method to evaluate the thermal coupling coefficients ( $c_{xy}$ ) from TCAD measurements has been proposed, which consists in evaluating the thermal coupling under the real operating conditions of the transistor (case B in Figure 5.16); the coefficients obtained with this method have a slight power dependency, but opposite to what published in [101], where the  $c_{xy}$  extraction is realized turning on the emitter fingers one at a time (case A in Figure 5.16), resulting in a biasing condition very different from the real operating conditions of the transistor.

# Chapter 6

## Modeling of thermal interactions at circuit level

### 6.1 Introduction

The previous chapters were mainly focused on the technology characterization at transistor level. In order to allow a successful circuit design and thus fully exploit the performances given by a certain technology, the limits of the device operation have to be explored and a modeling procedure has to be applied at circuit level [105].

To accomplish this, dedicated circuit blocks have been designed and measured; these circuits can be used for the verification of compact models to track back model inaccuracies and also allow a better technology characterization, considering and modelling additional effects arising, which normally are not taken into account in circuit simulators during the design process; recently some works have been published on the impact of electro-thermal coupling at circuit level, and the analysis have been carried with the help of electro-thermal simulators [106], [107] or thanks to dedicated circuit structures [46].

In this chapter the circuit modelling approach is presented and demonstrated for a differential pair fabricated in Infineon B11HFC technology; further the impact of inter-devices distance on the mutual thermal coupling is modeled on a dedicated cascode amplifier realized on-wafer and for a simulated Darlington amplifier. Finally the  $R_{th}$  variation caused by the BEOL is modeled and then its impact at circuit level is reported for the VM multifinger transistors presented in Chapter 4.

### 6.2 Differential pair for model verification

Differential pairs represent basic building blocks for circuit designers: they can be found in mixers, Gilbert cells, oscillators and amplifier stages. In fact, differential topologies have very interesting properties: (i) they provide immunity to common-mode noise coupling and crosstalk through the substrate and supply rails. (ii) They alleviate the negative impact of the bonding wire inductance on the gain, output power, and stability of amplifiers at microwave and mm-wave frequencies [108]. (iii) They reduce even-order distortion and the total harmonic distortion, resulting in higher linearity.

In [47] a detailed study on differential pairs subject to electro-thermal feedback has been presented, showing experimental results on dedicated circuit blocks; here the aim is to use differential pairs as demonstrator circuits for model verification, since they can be helpful in testing the compact model validity. In fact, from a DC point of view, fixing the operating point by a constant emitter current is not used during model parameter

## Chapter 6

### Modeling of thermal interactions at circuit level

extraction procedure; neither is the measurement of S-parameters in differential mode during the AC characterization.

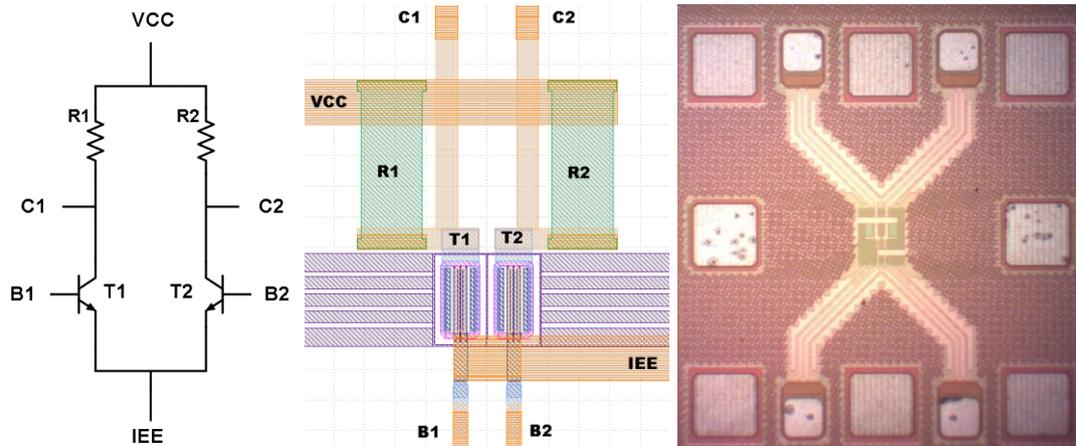


Figure 6.1: schematic representation, layout and photo of the differential pair

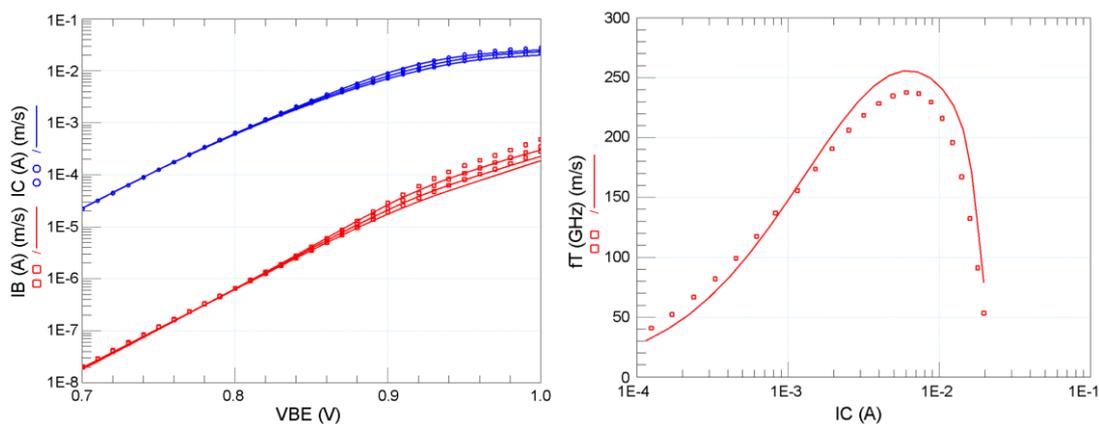


Figure 6.2: (left) Gummel plot measured on the transistor used for the differential pair; measurements are represented by symbols and solid lines are the simulation results using the model card.  $V_{CE}$  ranges from 0.8V to 1.2V. (right) Measured and simulated  $f_T$  for  $V_{BC}=0V$

A differential pair is realized using two SiGe HBTs of the same geometry than those that have been widely characterized in section 3.5 (drawn emitter area of  $0,2 \times 5 \mu\text{m}^2$ ).

A schematic of the circuit is proposed in Figure 6.1; the circuit is realized using a basic implementation: just two transistors and two resistances are used ( $30\Omega$ ), in order to reduce the modeling unknowns. The arrangement of the pads allows to bias the collector voltage and drain a constant current from the common emitters. The circuit is realized on the same chip as the transistor test structure, in order to reduce the possibility of inaccuracies due to process dispersion.

In Figure 6.2 are shown a comparison of the measurements and the compact model simulations of the  $0,2 \times 5 \mu\text{m}^2$  HBT; the model card has been developed by XMOD Technologies and it provides a good reproduction of the DC and RF behavior of the transistor over a wide range of bias conditions.

In Figure 6.3, instead, are shown the DC characteristics of the differential pair: the differential output voltage ( $V_{OUT1}-V_{OUT2}$ ) and the voltage at the emitter ( $V_{EE}$ ) are reported as a function of the differential input voltage ( $V_{IN1}-V_{IN2}$ ) for different values of the emitter current  $I_{EE}$ . For the AC characterization, the S-parameters have been measured in the frequency range between 200MHz and 40GHz in a 4 ports configuration. From these

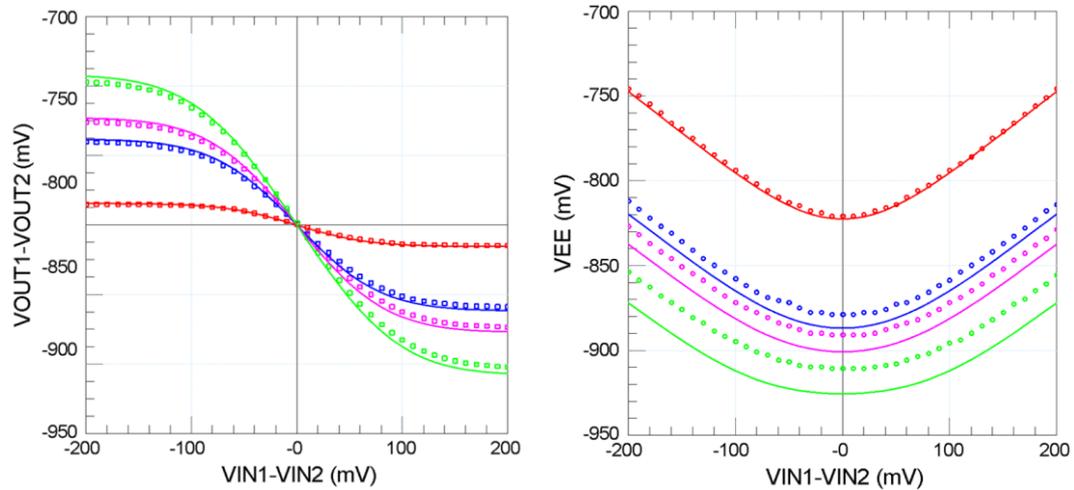


Figure 6.3: Measured and simulated differential output voltage (left) and emitter voltage (right) as a function of the differential voltage at the input, for  $I_{EE}$  ranging from 2mA (red) to 14mA (green)

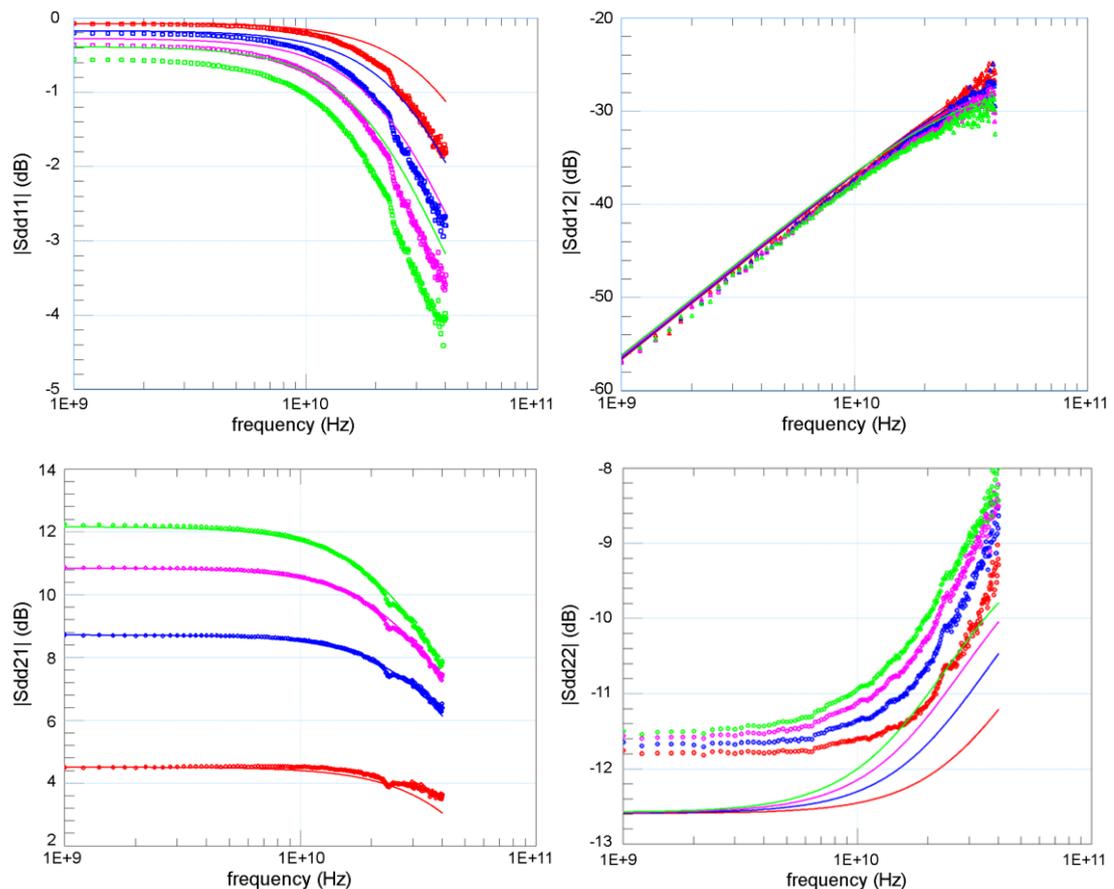


Figure 6.4: Measured and simulated differential small signal parameters for different values of  $I_{EE}$  (from red to green  $I_{EE}$  ranges between 4mA and 16mA)

measurements, the differential mode S-parameters are calculated and are reported in Figure 6.4 for different values of the emitter current  $I_{EE}$ , showing an excellent agreement with the simulation. The discrepancy that is observed in the  $S_{22}$  parameter is probably due to an issue in the deembedding test structures, which underestimate the parasitic contribution of the access lines at the output.

Observing the DC characteristics in Figure 6.3, it is noticed that a small deviation is obtained between the measured and simulated  $V_{EE}$  and this difference becomes higher as the value of the  $I_{EE}$  current increases; since the two transistors are placed in very close proximity (at the minimum distance possible), it can be supposed that thermal interactions may take place between the two devices, shifting their operating point in a higher amount as the value of current flowing in the differential pair increases. For this reason a simple thermal coupling network is inserted between the two thermal nodes of the transistor models, on the basis of the model shown in Figure 5.2, and can simulate the effect of a mutual thermal coupling between the devices. The coupling coefficient ( $c_{12}=c_{21}$ ) has been tuned to 23% to fit the measured  $V_{EE}$  and the simulated results are reported in Figure 6.5 (left), showing a better fit. In Figure 6.5 (right) it is shown the simulated temperature on one of the two transistors, in the case where the thermal coupling is taken into account or not: it can be noticed that, if the thermal interaction is considered, a temperature increase till  $15^{\circ}\text{C}$  is simulated by the compact model and is responsible for the bias point shift. This simulation shows that the  $V_{EE}$  of the circuit can be altered since the  $V_{BE}$  of the two transistors can be easily affected by temperature variations inducted by thermal coupling. The differential output voltage and the S-parameters have not been impacted by the introduction of the thermal coupling, and are therefore not shown.

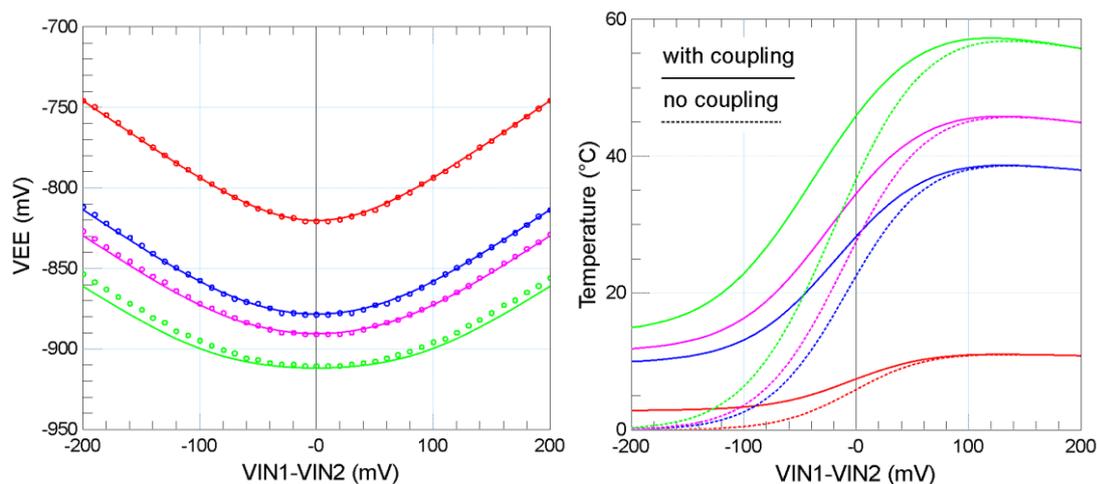


Figure 6.5: (left) measured and simulated emitter voltage as a function of the differential voltage at the input; going from red to green  $I_{EE}$  ranges from 2mA to 14mA. (right) simulated temperature on the T1 transistor for the same values of  $I_{EE}$ ; two cases are shown: without taking into account the thermal coupling and when the thermal coupling network is activated.

### 6.3 Dedicated circuits to study inter-device thermal coupling

#### 6.3.1 Cascode amplifier

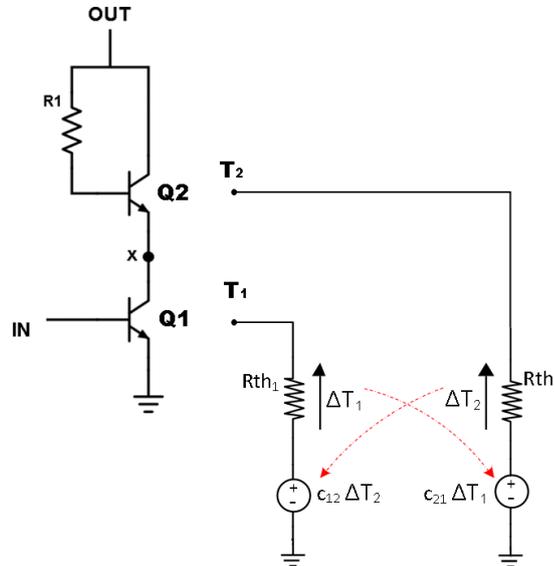


Figure 6.6: Schematic of the cascode amplifier; the external thermal network shows the mutual temperature coupling occurring among transistor  $Q_1$  and  $Q_2$

In the previous section it has been shown that inter-device thermal interactions can be the cause of bias point shifts at circuit level. In order to better investigate the impact of mutual thermal coupling between neighboring transistors, two versions of a cascode amplifier have been designed using wide emitter area transistors; the two circuits differ in the distance among the HBTs, as will be detailed below. The transistors used in this circuit have 2 collector, 3 base and 2 emitter contacts (in a CBEBEBC arrangement) and a total drawn emitter area of  $2 \times (0.2 \times 10) \mu\text{m}^2$ .

The circuit schematic is reported in Figure 6.6; it consists of two cascaded HBTs having the same geometry described above. The thermal network shows how the thermal interaction among  $Q_1$  and  $Q_2$  can be modeled, based on the theory given in [88]. The base of the upper transistor is biased thanks to the  $R_B$  resistance ( $50\Omega$ ), whereas during the measurements, two bias-T impose a DC bias point at the base of  $Q_1$  and at the collector of  $Q_2$ , while at the same time allowing to apply the AC stimulus for the measurement of the S-parameters.

The two circuit versions realized just differ in the distance among the transistors; in one case (referred to as D1 circuit) they have been placed at the minimal distance possible

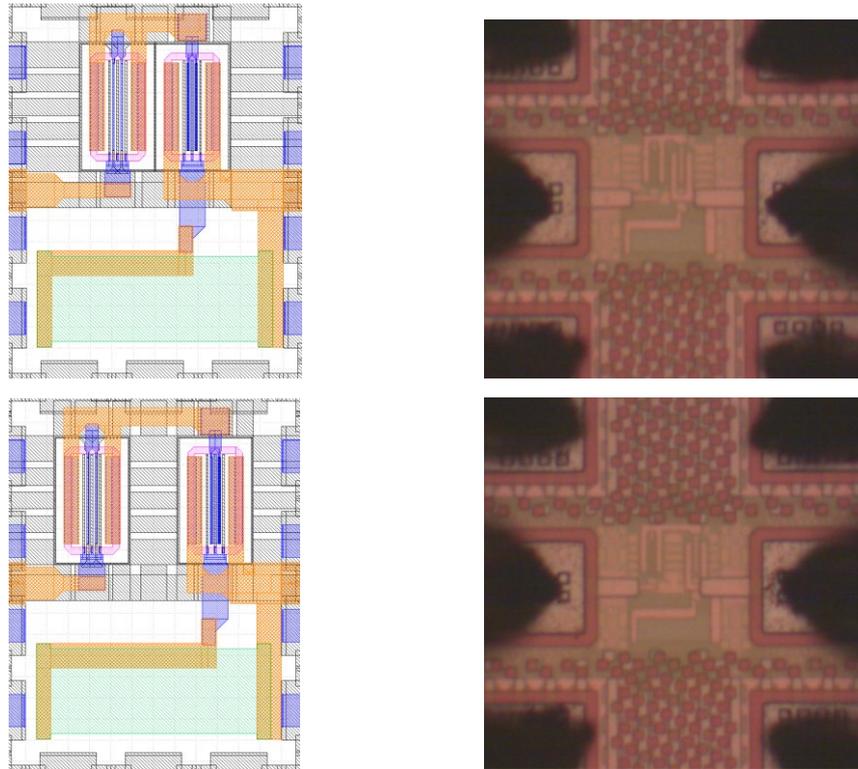


Figure 6.7: layout and microscope photo of the two different versions of the cascode amplifier: on top the D1 and at the bottom the D2.

(the spacing among the DTI of the transistors is  $2.28\mu\text{m}$ ), whereas in the other circuit, which will be named D2, the spacing among the components is increased of around 4 times, with a total distance among the DTI of the transistors of  $8\mu\text{m}$  (refer to Figure 6.7). D1 and D2 have been designed in such a way that the metal interconnections do not affect the electrical behavior in the two circuit implementations, so the differences that will be observed in the circuit performances can be only attributed to the mutual thermal heating between the transistors. Also in this case, the circuit layout is kept essential, and no matching networks are realized for the impedance matching, so that the attention is focused on the behavior of the active components.

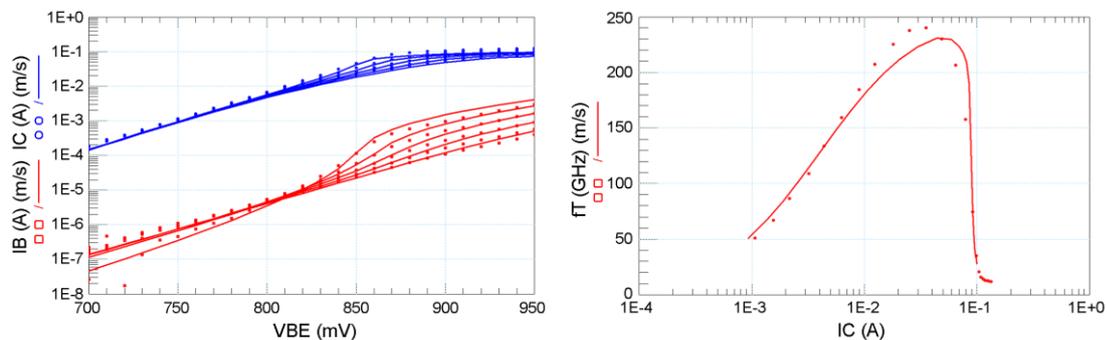


Figure 6.8: (left) Gummel plot measured on the transistor used for the differential pair; measurements are represented by symbols and solid lines are the simulation results using the model card.  $V_{CE}$  ranges from 0.8V to 1.5V. (right) Measured and simulated  $f_T$  for  $V_{BC}=-0.5V$

The model card of the transistor used in the circuit layout has been developed by XMOD Technologies. As reported in the case of the differential pair in paragraph 6.2, first of all a complete electrical characterization is performed in DC and AC on the transistor used in the circuits under study, in order to check the validity of the model card. The Gummel plot and  $f_T$  curve for the transistor used in the cascode amplifier are reported in Figure 6.8, showing an acceptable agreement between measurements and simulations. Performing measurements on different HBTs from the same wafer it has been observed that, due to process variations, the saturation current can vary from die to die, this is the reason why the model card simulates a slightly higher saturation current than what has been measured on our chip.

The measured output and input current are reported in Figure 6.10 and Figure 6.10 (left) for both D1 (in red) and D2 (in cyan); it is evident that for  $V_{IN}$  of around 820mV there is a significant decrease in the measured currents when the distance among the transistors increases (till 57% for the output current and 47% for the input current for  $V_{OUT}=2.7V$ ); this difference is not remarked at  $V_{IN}$  higher than 850mV or for bias points yielding low power dissipation. To simulate this effect, a basic thermal coupling network [88] is placed between the temperature nodes of the two transistor models, like the one shown in Figure 6.6: a coupling coefficient ( $c_{12}=c_{21}$ ) of 16.5% is used for the case of D1, whereas 8.8% is used for D2. Taking into account that the model card has an  $R_{th}$  value of 1700W/K, it can be estimated that the value of thermal coupling resistance (as given by Eq. 5.4:  $R_{th12}=R_{th21}=c_{12} R_{th22}=c_{21} R_{th11}$ ) among the two HBTs is around 280W/K for D1 and 150W/K for D2. The results from simulation using this thermal coupling model are shown in Figure 6.8 (right) and the same behavior than the measurements can be reproduced; due to the aforementioned variation of the transistor's saturation current, the measurements and simulations on the circuit will not be compared on the same plot.

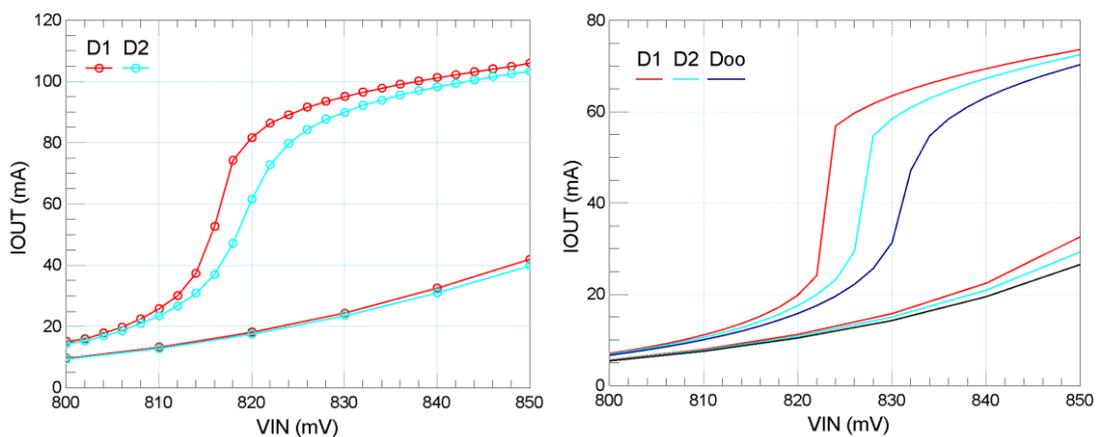


Figure 6.9: Measured (left) and simulated (right) output current for the circuits under study; the  $V_{OUT}$  is swept from 2.1V to 2.7V. Red: D1, blue: D2, black: no coupling ( $D_{\infty}$ )

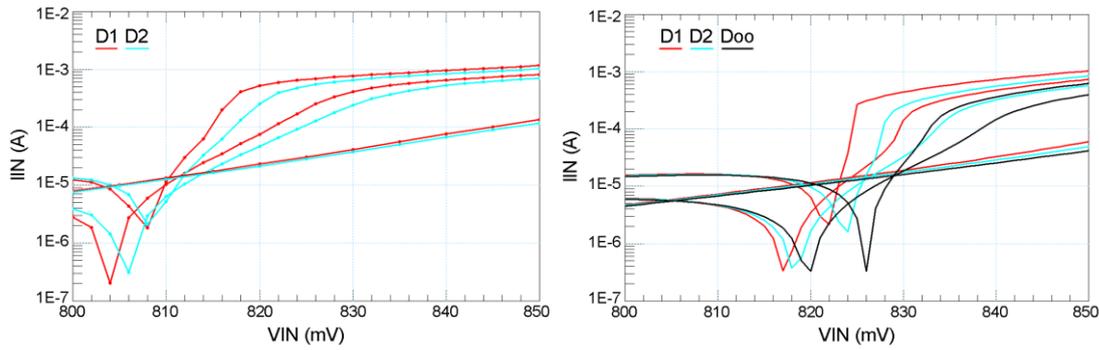


Figure 6.10: Measured (left) and simulated (right) input current for the circuits under study; the  $V_{OUT}$  is swept from 2.1V to 2.7V. Red: D1, blue: D2, black: no coupling ( $D_{\infty}$ )

A third ideal situation is simulated in black ( $D_{\infty}$ ), for which no thermal coupling is taken into account: in this case the sudden current increase obtained from the measurements is strongly reduced; the currents that are simulated in case  $D_{\infty}$  are much lower than what is obtained from the simulation of circuit D2, as a sign that even if the two HBTs are placed at a distance of  $8\mu\text{m}$ , thermal coupling still occurs. It must be underlined that normally the effect of mutual thermal coupling is not taken into account into circuit simulators, so this situation corresponds to the performances expected during the design phase.

The simulation results using the thermal coupling network allow a deeper insight in the circuit, making it possible to investigate the evolution of the potential at the central node  $x$  (refer to Figure 6.6) for different levels of thermal interaction; a higher voltage swing, and thus a higher dissipated power is found for the lower transistor  $Q_1$ . Observing the evolution of the temperature for the two transistors (Figure 6.11) it can be noticed that the sudden increase of current that is observed in Figure 6.8 is generated by the rapid temperature increase of  $Q_1$ , more precisely when it reaches around  $180^{\circ}\text{C}$ ; at this temperature a significant amount of heat couples to the  $Q_2$  transistor, thus shifting the bias point of the circuit. The thermal coupling model simulates that a maximum of around  $19^{\circ}\text{C}$  is coupled from  $Q_2$  to  $Q_1$ , while  $33^{\circ}\text{C}$  couple in the opposite direction.

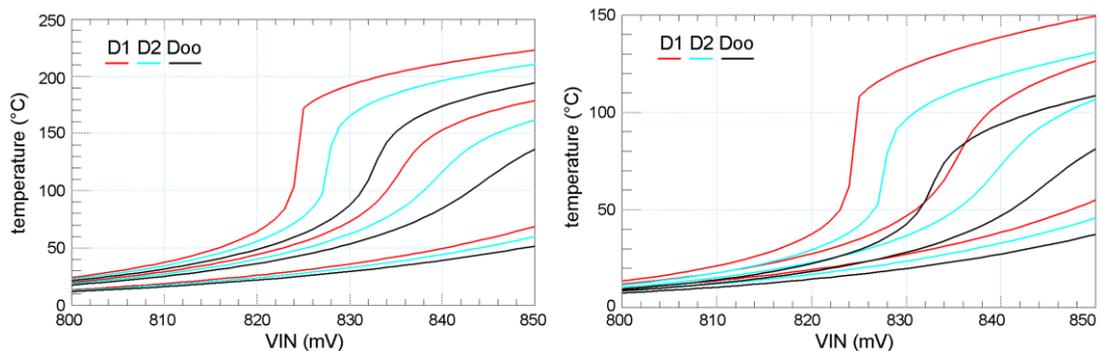


Figure 6.11: Simulated temperature increase for the  $Q_1$  (left) and  $Q_2$  (right) HBTs; the  $V_{OUT}$  ranges from 2.1V to 2.7V. Red: D1, blue: D2, black: no coupling ( $D_{\infty}$ )

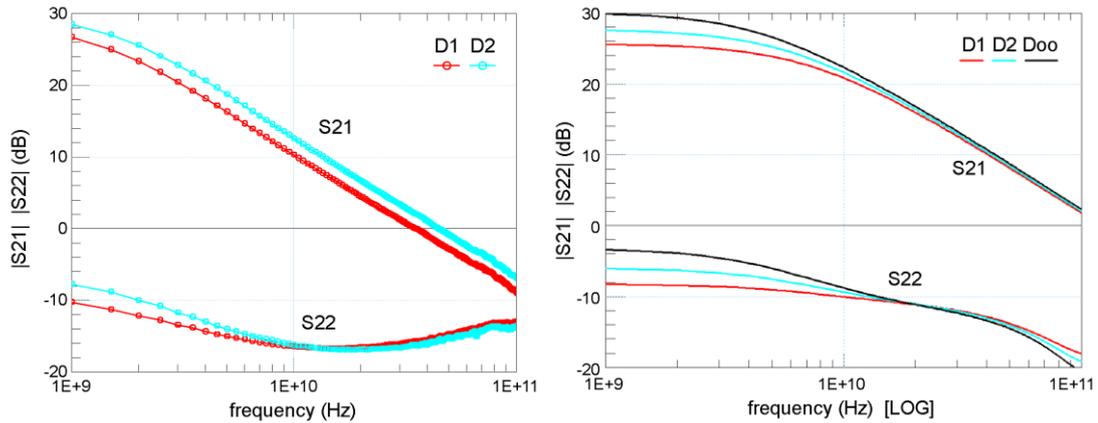


Figure 6.12: (left) Measured S-parameters for the bias point  $V_{IN}=850\text{mV}$  and  $V_{OUT}=2.5\text{V}$ ; (right) simulated S-parameters for the same bias point. Red: D1, blue: D2, black: no coupling ( $D_{\infty}$ )

Small signal measurements are also conducted on the circuit under study. The  $S_{21}$  and  $S_{22}$  parameters have been found to vary from circuit D1 to circuit D2 at the bias point  $V_{IN}=0.85\text{V}$  and  $V_{OUT}=2.5\text{V}$  and are reported in Figure 6.12 versus frequency. The D2 circuit shows a higher gain (more than 2dB higher) and a difference of around 2dB is also visible in the  $S_{22}$  parameter at low frequency; a similar behavior can be obtained from simulation, where the same difference in the S-parameters is observed. Comparing the simulation results of D1 with the case  $D_{\infty}$  an even higher difference till 4dB is found, showing that thermal coupling can degrade the small signal gain.

### 6.3.2 Two stages Darlington amplifier

Now that the mutual thermal coupling has been analyzed and verified for the two inter-device distances D1 and D2, the thermal network model can be used to evaluate the impact of the thermal interaction in other basic circuit topologies; a 2 stages amplifier having the transistors connected in Darlington configuration is proposed here and is designed using the same HBTs already studied (see Figure 6.13). Again three different circuits are considered and simulated, corresponding to the case where the HBTs are at a distance of  $2.28\mu\text{m}$  (case D1, with a coupling factor of 16.5%), at a distance of  $8\mu\text{m}$  (case D2, with a coupling factor of 8.8%) and finally the ideal case with no thermal coupling is studied ( $D_{\infty}$ ).

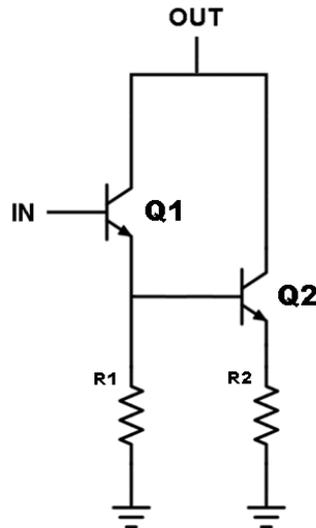


Figure 6.13: Schematic of the 2 stages amplifier; the  $Q_1$  and  $Q_2$  HBTs are connected in Darlington configuration.  $R1=15\Omega$  and  $R2=2.5\Omega$

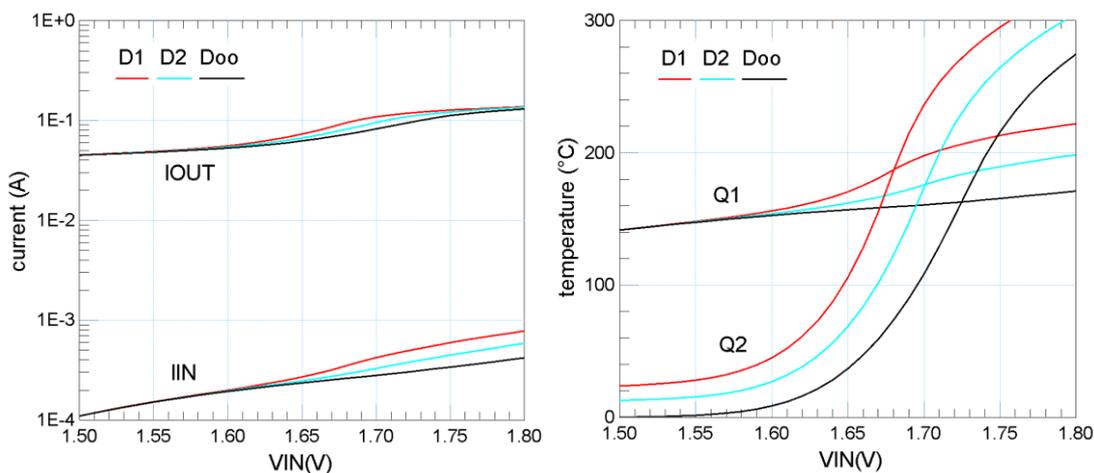


Figure 6.14: (left) Simulated input and output currents for the Darlington amplifier at  $V_{OUT}=2.5V$ ; (right) simulated temperature increase in the  $Q_1$  and  $Q_2$  transistors for the same bias points. Red: D1, blue: D2, black: no coupling ( $D^\infty$ )

In Figure 6.14 are reported the DC characteristics for  $V_{OUT}=2.5V$  and  $V_{IN}$  swept from 1.5V to 1.8V, as well as the temperature evolution of the two HBTs for the three circuit variants discussed. The current variations among the three circuits are smaller than in the case of the cascode, but still non negligible (25% difference for the  $I_{OUT}$  passing from D1 to  $D^\infty$ ). The simulation results reveal that the thermal unbalance among the two transistors can be higher than in the cascode circuit previously examined: at  $V_{IN}=1.8V$ ,  $Q_2$  reaches a much higher temperature than  $Q_1$ , for this reason up to  $47^\circ C$  are coupled from  $Q_2$  to  $Q_1$ , while up to  $28^\circ C$  couple in the opposite direction. For completion also the  $S_{21}$  is reported in Figure 6.15, showing again that the thermal coupling can be responsible of a degradation of the small signal gain (a deviation up to around 2.5dB is predicted from simulation).

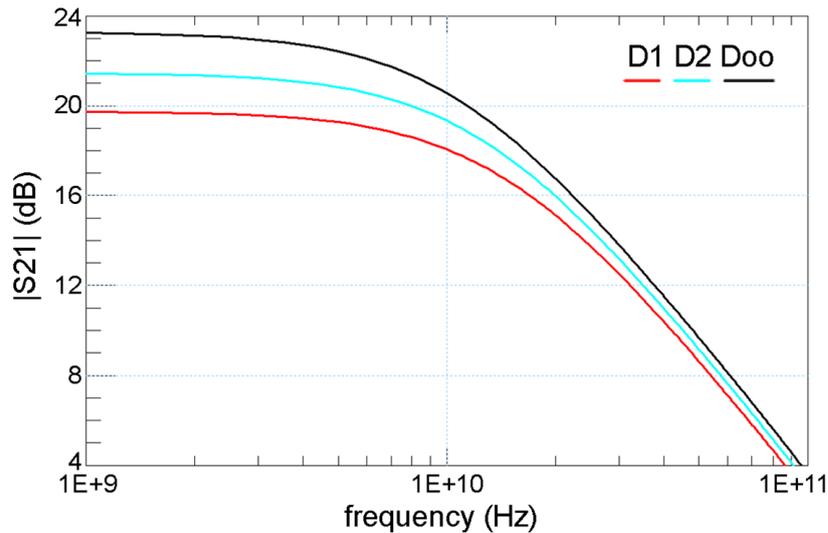


Figure 6.15: Simulated S-parameters for the bias point  $V_{IN}=1.75V$  and  $V_{OUT}=2.5V$ . Red: D1, blue: D2, black: no coupling ( $D_{\infty}$ )

The analysis of these dedicated circuits to evaluate the effects of thermal coupling as function of the distance between the transistors has revealed that thermal interactions can be responsible of performance degradation at circuit level; taking into account these effects in circuit simulators can be of help during the design phase, in order to understand till what extent the bias points of each transistor can be altered by the temperature increase of neighboring devices.

## 6.4 BEOL thermal impact at circuit level

In Chapter 3 and Chapter 4 it has been shown that the BEOL metallization has a certain impact on the electro-thermal properties of the transistor; as already demonstrated in section 3.4, this effect can be simulated in compact models by adding a parallel RC network to the intrinsic self-heating related  $R_{th}$ , thus allowing to take into account the heat diffusion in the copper of the metal interconnections (refer to Figure 3.19).

This modeling approach has been applied to the multifinger transistors realized in ST B55 technology which have been characterized in Chapter 4: in Figure 6.16 are reported the measured output curves for the transistors VM1, VM3 and VM8. As already said, to simulate the current decrease that is observed in the high power dissipation region, a resistor is put in parallel to  $R_{th}$ ; passing from test structure VM1 to VM8, the overall  $R_{th}$  seen at the temperature node of the compact model is decreased by around 10%, in line with the results obtained from the  $R_{th}$  extraction in Figure 4.10.

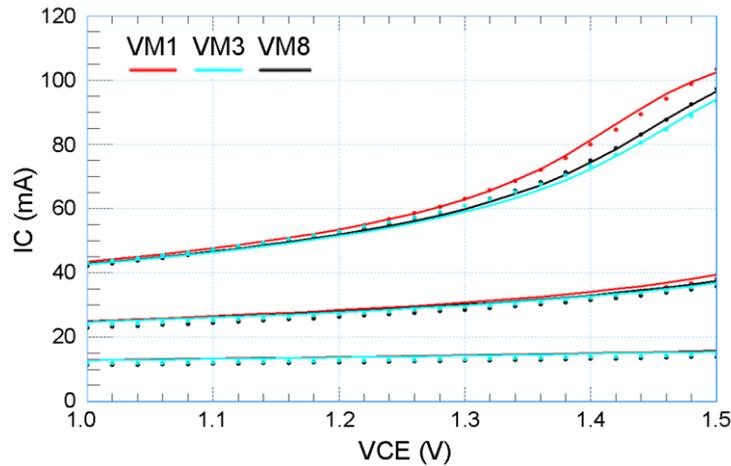


Figure 6.16: Measured and simulated output curves for the multifinger transistors containing metal dummies in the BEOL: VM1, VM3 and VM8

These transistor compact models can be used to design a circuit demonstrator and estimate the impact at circuit level. It has been chosen to implement a cascode amplifier having the same circuit topology reported in Figure 6.6 using the model card of the VM1, VM3 and VM8 HBTs. The model cards provide a good accuracy also for what concerns the AC behavior: in Figure 6.17 are reported the measured and simulated  $f_T$  for the VM1 and VM8 HBTs.

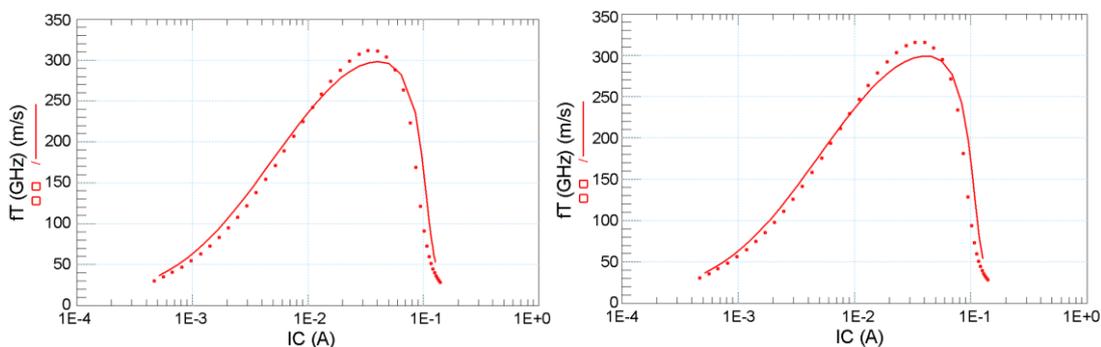


Figure 6.17: Measured and simulated  $f_T$  at  $V_{CE}=1.5V$  for the VM1 (left) and VM8 transistor (right).

At circuit level the thermal coupling among the two HBTs is not considered, in order to focus the attention on the effect of the  $R_{th}$  decrease caused by the BEOL; for the DC analysis it is found a similar behavior than what is observed in Figure 6.11: in the case where the VM1 transistor is used, the temperature reached by both  $Q_1$  and  $Q_2$  is higher than when VM8 is used, due to the difference in the  $R_{th}$  in the two devices (see Figure 6.18); a difference in the simulated  $T_j$  till  $46^\circ C$  is obtained.

The resulting DC characteristics are reported in Figure 6.19 and the output and input currents show a similar trend than in what has been reported for the previous circuits under study: in correspondence of the sudden increase of current (located at a  $V_{IN}$  of around  $860mV$ ) there is a significant deviation in the behavior of the 3 different circuits, which is caused by the different temperature reached by the HBTs.

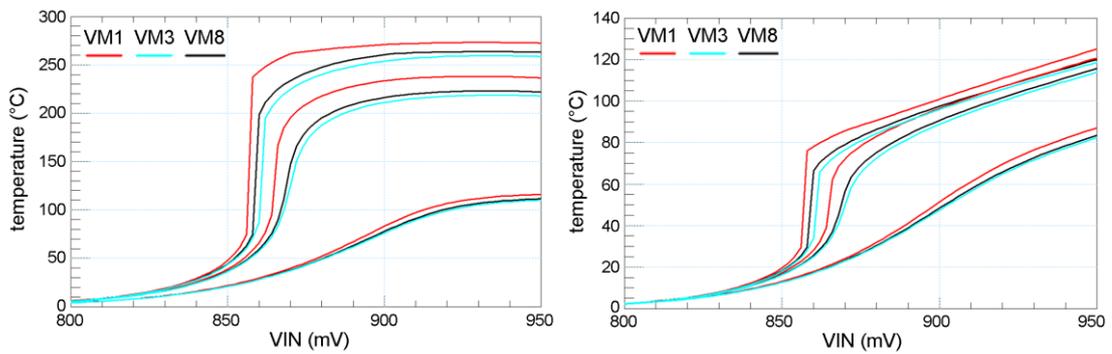


Figure 6.18: Simulated temperature increase for the  $Q_1$  (left) and  $Q_2$  (right) HBTs; the  $V_{OUT}$  ranges from 2.2V to 2.7V. The temperature is reported for the case where VM1, VM3 and VM8 are used.

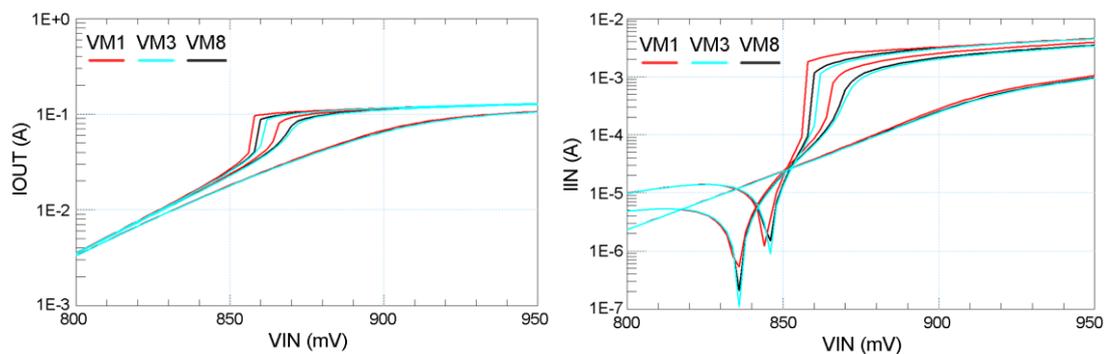


Figure 6.19: Simulated output current (left) and input current (right); the  $V_{OUT}$  ranges from 2.2V to 2.7V.

The S-parameters measurements show again that a higher small signal gain can be obtained if thermal related effects are mitigated (Figure 6.20); in this case, the  $R_{th}$  decrease due to the presence of the BEOL in VM8 can assure a higher  $S_{21}$  at circuit level (around 3dB higher than the circuit using the VM1 transistors).

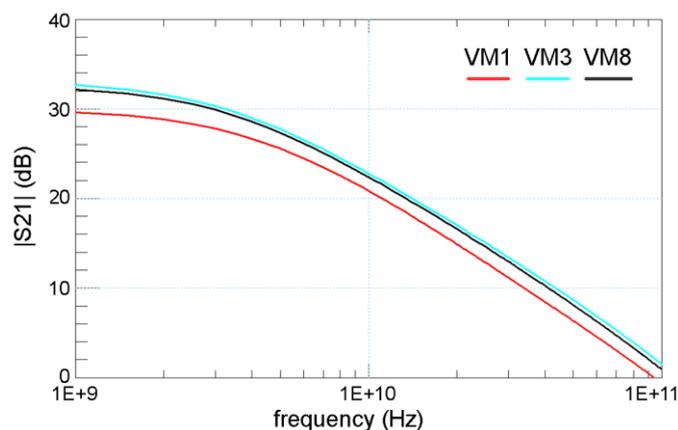


Figure 6.20: Simulated  $S_{21}$  parameters for the bias point  $V_{IN}=870\text{mV}$  and  $V_{OUT}=2.6\text{V}$  for the three different transistors considered

## 6.5 Conclusion

In this chapter a modeling approach based on dedicated circuits for the verification of compact models is presented and is applied to a differential pair block with good results. Further the effects of thermal coupling and of the BEOL are evaluated at circuit level; a cascode amplifier is presented, which is designed using large emitter area transistors, and the impact of inter device thermal coupling is analyzed and modeled for two different versions of the circuit having different distances among the transistors. It has been found that the effect of thermal coupling cannot be neglected and has a significant negative impact on the circuit performances in DC and AC operation; for the bias points at high power dissipation a difference of more than 50% is measured for the output current and around 2dB for the small signal gain among the D1 and D2 circuits. The same thermal coupling model has been used to simulate the behavior of a 2 stages Darlington amplifier for the same inter-device distances than the cascode amplifier, showing a similar impact. Finally, the electro-thermal impact of the BEOL metallization has been modeled for the multifinger transistor structures presented in Chapter 4 and the model cards have been used for the design of a cascode amplifier, showing significant differences in the DC performances, due to their reduced  $R_{th}$ ; furthermore the simulations have shown that the addition of metal dummies can slightly improve the circuit DC and AC performances, like the small signal gain.

The circuit demonstrators presented have shown that inter-device thermal interactions can have an important impact at circuit level for large emitter area transistors (Figure 6.9) as well as for smaller devices (Figure 6.5), according to the circuit topology which is implemented. In fact, for the differential pair circuit presented, it has been shown how the  $V_{BE}$  can be easily affected by temperature variations inducted by thermal coupling. The variation of the  $R_{th}$  caused by the BEOL can also lead to sensible performance variation at circuit level. Taking these effects into account into circuit simulators during the design phase can represent a useful tool for designers, allowing to estimate the DC and AC variations of each transistor due to the temperature increase of neighboring devices, and thus to find the optimal distance among the different devices which yields the desired circuit performances. It has been shown that completely neglecting these thermal effects at circuit level can lead to significant differences (refer to Figure 6.12) and thus the electrical performances measured on-wafer can be very different than the results obtained from simulation (for instance, up to 4dB of difference in gain are estimated for the cascode amplifier designed in Infineon technology).

## Summary of the work

### General conclusions

State of the art SiGe HBT technologies can ensure very good performances for high frequency transceivers for millimeter wave applications, moreover their rapid technology development at low cost has made them a good choice to open new applications in the consumer market.

The thermal issue is one of the key factors limiting the performance and reliability of the devices and integrated circuits. Self-heating has a huge impact in static and dynamic operation, and it can thus affect the transistor electrical behavior in the low frequency range (till few hundreds of MHz), since the thermal diffusion represents a distributed phenomenon, intrinsically slower than the electrical behavior. Due to intermodulation distortion arising at large signal operation and due to the use of wideband signals, thermal memory effects can take place and so self-heating can affect the transistor behavior even at very high frequencies. Consequently, a realistic thermal compact modeling is strongly mandatory, in order to obtain accurate simulation results that take into account the intrinsic operating temperatures of the active devices, as well as to provide a continuous improvement of the technology nodes. Modeling engineers need precise measurements to characterize the transistor thermal properties.

This thesis begins with an overview of extraction methodologies to estimate the thermal resistance ( $R_{th}$ ) and impedance ( $Z_{th}$ ), which are presented and discussed with examples of application on the state of the art technologies from ST Microelectronics (B55) and Infineon Technologies (B11HFC). The limitations of a conventional single pole thermal network are demonstrated with dedicated measurements in the time and frequency domain, as well as in the case of a two tones large signal simulation, for different values of the frequency tone spacing.

The main part of this work is dedicated to a complete electro-thermal characterization of SiGe HBT transistors in single finger as well as multifinger architecture and an effort has been done to design alternative architectures with an improved electro-thermal behavior, highlighting their performance differences.

Innovative transistor structures have been realized in the B11HFC process from Infineon: the test structures are designed in a way to exploit the benefits of the metal in the back end of line (BEOL). It has been demonstrated that the mechanical stress, as well as the positive thermal impact caused by the presence of additional metal stacks above the HBT are the main reasons for the enhanced DC and RF characteristics that have been reported at both small signal and large signal. Moreover a compact model is presented to take into account the impact of the BEOL metallization on the thermal impedance and its

## Summary of the work

parameters have been calibrated with DC and low frequency S-parameter measurements on dedicated test structures. The model is based on a recursive RC network and can be connected to the thermal node of the HiCuM model; a validation with pulsed measurements has demonstrated a good accuracy for the time evolution of the collector current  $I_C$ . It has been also evidenced by means of TCAD simulations and experimental dedicated measurements that the metallization in the BEOL has a significant impact on the thermal capacitance ( $C_{th}$ ) of the transistor, thus sensibly slowing down its thermal response; when excited with a two tones input signal, the increased  $C_{th}$  can play a positive role in keeping the device temperature more stable to the envelope of the power dissipation. In general it is found that the presence of carefully designed metal dummies in the BEOL impacts in a sensible and positive way both the DC and RF performances of the transistor, and should therefore be modeled and considered into the circuit simulators to provide an improved accuracy in the circuit design phase.

The study of the transistors realized in this technology is finalized with device simulations realized in Sentaurus TCAD, in which the thermal conductivity is varied according to the doping profile within the transistor structure. It is shown that the high doping concentrations, which are present in some specific regions of the transistor, can have a non-negligible impact on the simulated  $R_{th}$  and  $Z_{th}$  and is therefore recommended to take this effect into account to obtain more realistic results.

Further, some alternative transistor topologies have been designed in multi-finger configuration, using a HBT technology from STMicroelectronics (B55): the aim is to provide an improved electro-thermal behavior and ensure more robust SOA specifications.

Among all the proposed methodologies for improving the thermal behavior, the most efficient seem to be that of increasing the DTI enclosed area, as well as adding metal stacks above the active component. In fact, once a certain level of power dissipation is attained, the metallization is not only a bare electrical connection, but also participates in a positive way in the heat dissipation, helping to evacuate the heat generated in the active part of the transistor. For instance, adding 8 levels of metal upon the emitter fingers leads to a diminution in the  $R_{th}$  of around 10% for the SiGe HBTs under study. These better thermal properties allow a sensible decrease of the  $g_{out}$ , thus ensuring an improvement of the SOA and at the same time an increase of the DC current gain till around 34%. Regarding the AC performances, the  $f_T$  curve is observed to slightly shift up and the peak  $f_T$  increases up to 5GHz. With a proper variation of the DTI enclosed area even better performances have been observed. The better performances achievable using these methodologies, together with the ease of implementation in all the technologies make it the most suitable approach for circuit applications where high power handling is needed. The investigation of thermal interactions at device level is concluded with a study of intra-device dynamic thermal coupling in multifinger transistors; a netlist-based model is

proposed, to take into account the transient thermal coupling arising among the emitter fingers and to accurately reproduce it in electrical simulators. It can be useful to simulate in a more realistic way the behavior of multifinger SiGe HBTs during the design process or to choose the ballast resistors in a PA cell for a balanced heat distribution.

The effect of the mutual thermal coupling in dynamic operation has been analyzed in the time and frequency domain with the aid of thermal TCAD simulations and on-wafer measurements; it has been observed that it leads to an overall slowdown of the temperature evolution of the transistor fingers.

The impact of the BEOL on the temperature evolution has been simulated in TCAD and it is found that the presence of the layers from the BC junction up to the first level of metal determine an increase of the  $C_{th}$  (together with a decrease of the  $R_{th}$ ), which leads to an overall slowdown of the temperature evolution of around a factor 2, for the technology under study. Finally a method to evaluate the thermal coupling coefficients ( $c_{xy}$ ) from TCAD measurements has been proposed, which consists in evaluating the thermal coupling under the real operating conditions of the transistor.

The thesis is concluded by extending the study of thermal interactions at circuit level, with the help of dedicated circuit blocks, which have been designed in Infineon B11HFC technology.

First, a modeling approach for the verification of compact models is presented and is applied to a differential pair block, showing that thermal coupling can be responsible of simulation inaccuracies. Further, the effects of thermal coupling and of the BEOL are evaluated at circuit level; a cascode amplifier is presented, which is designed using large emitter area transistors, and the impact of inter device thermal coupling is analyzed and modeled for two different versions of the circuit having different distances among the transistors. It has been found that thermal coupling cannot be neglected and can considerably degrade the circuit performances in DC and AC operation; for the bias points at high power dissipation, a difference of more than 50% is measured for the output current and around 2dB for the small signal gain among the two versions of the circuit under study. The same inter-device thermal coupling model can be applied also for other circuit topologies: in particular a 2 stages Darlington amplifier has shown a similar negative impact on the overall AC and DC performances.

Finally, the electro-thermal impact of the BEOL metallization has been modeled for the multifinger transistor structures previously analyzed and the model cards have been used for the design of a cascode amplifier, showing that an improvement of the DC and AC performances can be obtained at circuit level using the innovative transistor topologies proposed.

The circuit demonstrators presented have shown that inter-device thermal interactions can have an important impact at circuit level for large emitter area transistors, as well as for smaller devices, according to the circuit topology which is implemented. In fact, for the

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differential pair circuit presented, it has been shown how the  $V_{BE}$  can be easily affected by temperature variations inducted by thermal coupling. The variation of the  $R_{th}$  caused by the BEOL can also lead to sensible performance variation at circuit level. Taking these effects into account into circuit simulators during the design phase can represent a useful tool for designers, allowing to estimate the DC and AC variations of each transistor due to the temperature increase of neighboring devices, and thus to find the optimal distance among the different devices which yields the desired circuit performances. If completely neglected, these thermal effects can lead to significant differences and thus the measured electrical performances can be very different than the results obtained from simulation (for instance, up to 4dB of difference in gain are estimated for the cascode amplifier designed in Infineon technology).

## Perspectives

This thesis work has presented a complete study of how electro-thermal interactions impact the characteristics of two state of the art SiGe HBT technology nodes, from device to circuit level. Alternative transistor topologies have been presented to mitigate these thermal issues and have been simulated at circuit level.

However it has to be pointed out that some aspects of the work need an improvement and a deeper study, as listed below.

### *TCAD analysis*

For a more realistic thermal simulation, a volumetric power source can be implemented into the transistor structures instead of the ideal planar source; ideally it could be chosen to change the volume of the power source according to the bias conditions, since the volume of the BC depletion region changes with the internal  $V_{BC}$ .

The sources of power dissipation have to be studied in deeper detail, in order to localize with precision the regions of the transistor where the heat is dissipated and understand the interactions with the thermal properties of the device; as shown in Chapter 3, this affects the resulting  $R_{th}$  extracted from TCAD.

Furthermore the impact of the doping profile on the thermal properties of the transistor has to be further investigated, together with its temperature dependency.

### *SOA investigation*

Some specially designed multifinger transistor structures have been designed in STMicroelectronics B55 technology, in order to improve the SOA specifications and make use of a combination of the different techniques that have been presented in Chapter 4: emitter finger segmentation, DTI area increase, use of BEOL metal dummies. For a deeper analysis of the SOA the snapback curves can be measured.

*Thermal memory effects*

The effect of the thermal impedance at low frequency can impact the behavior of the transistor when it is operated at large signal, due to the thermal memory effect. This phenomenon can be analyzed in detail with for the different transistor structures that have been presented in Chapter 3 and Chapter 4 thanks to two tones large signal measurements or measuring the output of the transistor when it is driven by a baseband signal having a bandwidth within the thermal cutoff of the transistor. An investigation of the thermal impedance below 10kHz can also be carried, using dedicated bias-T, allowing to measure in a lower frequency range, in order to explore the dynamic self-heating at very low frequencies.

*Thermal interactions at circuit level*

The basic thermal coupling model used for the simulation of the amplifiers in Chapter 6 can be extended to include the dynamic thermal interactions; the differential pair, as well as the two versions of the cascode amplifier, can be characterized at low frequency, to understand how the dynamic thermal coupling can affect circuit performances and how it varies with the distance. The study can be extended at large signal, for instance with pulsed measurements it would be possible to characterize the dynamic thermal response for the cascode amplifiers. The impact of thermal coupling at circuit level can be also evaluated designing dedicated circuits using multifinger transistors, which have a large area occupation and can thus yield more intense thermal interactions.

As it has been experimentally demonstrated in Chapter 3 and Chapter 4, it is possible to obtain better DC and RF device performances by making use of carefully designed metal dummies placed upon the transistor; moreover it has been shown from simulations in section 6.4 that this can impact the DC and AC characteristics at circuit level. Specific PA cells can be designed with and without making use of these metal dummies and the two versions of the circuit can be compared, including an experimental analysis of the main figures of merit at large signal.

In general, the impact of thermal effects at circuit level can be more deeply studied, taking into account the temperature rise generated by other dissipating elements, like the resistances which are present in the layout; moreover the impact of temperature coupling happening through the metal connections can be estimated. This can be accomplished with the aid of TCAD simulations or thanks to layout-based electro-thermal simulation tools, like Heatwave Thermal Simulator, integrated as part of ADS.

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## List of publications

### *International journals*

1. A. K. Sahoo, S. Fregonese, **R. D'Esposito**, K. Aufinger, C. Maneux, and T. Zimmer, "A Geometry Scalable Model for Nonlinear Thermal Impedance of Trench Isolated HBTs," *IEEE Electron Device Lett.*, vol. 36, no. 1, pp. 56–58, Jan. 2015.
2. A. K. Sahoo, S. Fregonese, **R. D'Esposito**, C. Maneux, and T. Zimmer, "Isothermal Electrical Characteristic Extraction for mmWave HBTs," *IEEE Trans. Electron Devices*, vol. 62, no. 1, pp. 232–235, Jan. 2015.
3. A. D. D. Dwivedi, A. Chakravorty, **R. D'Esposito**, A. K. Sahoo, S. Fregonese, and T. Zimmer, "Effects of BEOL on self-heating and thermal coupling in SiGe multi-finger HBTs under real operating condition," *Solid-State Electron.*, vol. 115, Jan. 2016.
4. A. D. D. Dwivedi, **R. D'Esposito**, A. K. Sahoo, S. Fregonese and T. Zimmer "A study on self-heating and mutual thermal coupling in SiGe multi-finger HBTs", *Journal of Electronic Materials*, 2016
5. **R. D'Esposito**, S. Frégonèse, A. Chakravorty, P. Chevalier, D. Céli and T. Zimmer, "Innovative SiGe HBT topologies with improved electro-thermal behavior", *IEEE Transactions on Electron Devices*, vol. 63, n. 7, pagg. 2677–2683, lug. 2016.
6. S. Balanethiram, **R. D'Esposito**, A. Chakravorty, S. Fregonese, D. Celi and T. Zimmer, "Efficient Modeling of Distributed Dynamic Self-Heating and Thermal Coupling in Multi-Finger SiGe HBTs", *IEEE Transactions on Electron Devices* (Accepted)
7. A. Chakravorty, **R. D'Esposito**, S. Fregonese and T. Zimmer, "Analytic Estimation of Thermal Resistance in HBTs", *IEEE Transactions on Electron Devices* (Accepted)

### *International conferences*

1. **R. D'Esposito**, M. Weis, A. K. Sahoo, S. Fregonese, and T. Zimmer, "A study on transient intra-device thermal coupling in multifinger SiGe HBTs," in *2014 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2014, pp. 179–182.
2. S. Fregonese, **R. D'Esposito**, M. D. Matos, A. Köhler, C. Maneux, and T. Zimmer, "Substrate-coupling effect in BiCMOS technology for millimeter

- wave applications,” in *New Circuits and Systems Conference (NEWCAS), 2015 IEEE 13th International*, 2015, pp. 1–4.
3. B. Ardouin, M. Schroter, T. Zimmer, K. Aufinger, U. Pfeiffer, C. Raya, A. Mukherjee, S. Malz, S. Fregonese, **R. D’Esposito**, and M. De Matos, “Compact Model Validation Strategies Based on Dedicated and Benchmark Circuit Blocks for the mm-Wave Frequency Range,” in *2015 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2015, pp. 1–4.
  4. S. Balanethiram, A. Chakravorty, **R. D’Esposito**, S. Fregonese, and T. Zimmer, “Efficient modeling of static self-heating and thermal-coupling in multi-finger SiGe HBTs,” in *2015 IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 68–71.
  5. **R. D’Esposito**, S. Fregonese, A. Chakravorty and T. Zimmer, “Dedicated test-structures for investigation of the thermal impact of the BEOL in advanced SiGe HBTs in time and frequency domain,” in *International Conference on Microelectronic Test Structures (ICMTS)*, 2016, pp. 28-31.
  6. M. Potéreau, A. Curutchet, **R. D’Esposito**, M. De Matos, S. Fregonese and T. Zimmer, “ A Test Structure Set for on-wafer 3D-TRL calibration,” in *International Conference on Microelectronic Test Structures (ICMTS)*, 2016, pp. 28-31.
  7. **R. D’Esposito**, M. De Matos, S. Fregonese, S. Balanethiram, A. Chakravorty, K. Aufinger and T. Zimmer, “Influence of the BEOL Metallization Design on the Overall Performances of SiGe HBTs”, 2016 IEEE *International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, 2016 (Accepted)
  8. S. Balanethiram, A. Chakravorty, **R. D’Esposito**, S. Fregonese and T. Zimmer “An Improved Scalable Self-Consistent Iterative Model for Thermal Resistance in SiGe HBTs” , *2016 IEEE Bipolar/BiCMOS Circuits and Technology Meeting* (Accepted)

### ***Workshops***

1. **R. D’Esposito**, M. Weiß, A. K. Sahoo, S. Fregonese and T. Zimmer, “Investigation of transient intra-device thermal coupling”, 27th BipAk Workshop, Crolles, France, 24 October 2014.
2. **R. D’Esposito**, M. Weiß, A. K. Sahoo, S. Fregonese and T. Zimmer, “Self Heating and Thermal Coupling in SiGe Multi-Finger HBTs“, HICUM Workshop, Boeblingen, Germany, 12-13 May 2015.

## Résumé substantiel

### Titre:

## **Caractérisation électrothermique, simulations TCAD et modélisation compacte de transistors HBT en SiGe au niveau composant et circuit**

Les applications du domaine Sub-THz s'avèrent de plus en plus nombreuses, notamment dans le domaine des télécommunications sans fils, mais aussi des technologies d'imagerie actives ou passives pour des applications médicales et biologiques ou de sécurité. La disponibilité de systèmes efficaces à bas coût nécessite le développement de technologies adaptées parmi lesquelles les technologies Silicium ont un rôle prépondérant à jouer pour la génération et la réception des signaux électroniques associés à ce type d'applications. La technologie Bipolaire à Hétérojonctions (HBT) Silicium /Silicium-Germanium (SiGe) est une candidate sérieuse à ce type d'applications du fait des fréquences de coupure très élevées associées à des tensions de collecteur élevées permettant des niveaux de puissance élevés à des fréquences Sub-THz. Néanmoins les structures HBT de ce type sont très sensibles aux effets thermiques, qu'il est nécessaire de maîtriser pour fiabiliser la conception des circuits.

Ce travail de thèse s'inscrit dans ce contexte et présente une étude concernant la caractérisation des effets électrothermiques dans les transistors bipolaires à hétérojonction (HBT) en SiGe. Lors de ces travaux, deux procédés technologiques BiCMOS à l'état de l'art ont été analysés: le B11HFC de Infineon Technologies (130nm) et le B55 de STMicroelectronics (55nm); pour ces composants, différentes techniques de mesure en régime continu, sinusoïdale et pulsé sont présentées et effectuées pour une évaluation approfondie du comportement électrothermique. En particulier, l'auto-échauffement des transistors unitaires et le couplage thermique avec leurs plus proches voisins périphériques sont caractérisés et modélisés. La rétroaction électrothermique intra-transistor et inter-transistor est largement étudiée. En outre, l'impact des effets thermiques est étudié au niveau circuit, en évaluant les performances de trois topologies de circuits analogiques.

Pour ce qui concerne la caractérisation des composants, grâce à une expression généralisée de l'impédance thermique, formulée dans le domaine fréquentiel, il a été possible d'extraire cette impédance en delà de la fréquence de coupure thermique. Les paramètres thermiques ont été extraits par des simulations compactes grâce au modèle compact de transistors auquel un modèle

électrothermique a été ajouté via le nœud de température. Les travaux théoriques développés à ce jour pour la modélisation d'impédance thermique ont été vérifiés avec les résultats expérimentaux. Il a été montré que, le réseau thermique classique utilisant un pôle unique n'est pas suffisant pour modéliser avec précision le comportement thermique transitoire et donc qu'un réseau plus complexe doit être utilisé. Le réseau récursif a été vérifié par des simulations TCAD, ainsi que par des mesures et celles-ci se sont révélées en excellent accord.

Des structures de test dédiées ont été conçues, pour évaluer l'impact électrothermique du back end of line (BEOL) de composants ayant une architecture à un ou plusieurs doigts d'émetteur. Une caractérisation complète a été effectuée en régime continu et en mode alternatif en petit et en grand signal. De plus, une extraction des paramètres thermiques statiques et dynamiques a été réalisée et présentée pour les structures de test proposées. Il est démontré que les figures de mérite DC et RF s'améliorent sensiblement en positionnant des couches de métal sur le transistor, dessinées de manière innovante et ayant pour fonction de guider le flux thermique vers l'extérieur. L'impact thermique du BEOL a été modélisé et vérifié expérimentalement dans le domaine temporel et fréquentiel et aussi grâce à des simulations 3D par éléments finis. Il est à noter que l'effet du profil de dopage sur la conductivité thermique est analysé et pris en compte.

Des topologies de transistor innovantes ont été conçues, permettant une amélioration des spécifications de l'aire de sécurité de fonctionnement, grâce à un dessin innovant de la surface d'émetteur et du deep trench (DTI).

Un modèle compact est proposé pour simuler les effets de couplage thermique en dynamique entre les émetteurs des HBT multi-doigts; ensuite le modèle est validé avec de mesures dédiées et des simulations TCAD.

Des circuits de test ont été conçus et mesurés, pour vérifier la précision des modèles compacts utilisés dans les simulateurs de circuits; de plus, l'impact du couplage thermique entre les transistors sur les performances des circuits a été évalué et modélisé, pour des topologies cascode et pour un amplificateur à deux étages de type Darlington. Finalement, l'impact du dissipateur thermique positionné sur le transistor a été étudié au niveau circuit, montrant un réel intérêt de cette approche.